SERVICE MANUAL

Z-49 Video Display Terminal

NOTE: This is a PRELIMINARY manual. This publication has not been through our normal testing phase; therefore, it may contain technical inaccuracies. You will receive a final version of the manual after our normal evaluation cycle is completed.

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860-38

ZENITH data systems

HEATH

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The purpose of this page is to make sure that all service bulletins are entered in this manual. When a service bulletin is received, annotate the manual and list the information in the record below.

Record of Service Bulletins

SERVICE BULLETIN NUMBER	DATE OF ISSUE	CHANGED PAGE(S)	PURPOSE OF SERVICE BULLETIN	INITIALS

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St. Joseph, Michigan 49085

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Abbreviations

ACIA	Asynchronous Communication Interface Adapter
ANSI	American National Standards Institute
AT	Attribute
ASCII	American Standard Code for Information Interchange
AVDC	Advanced Video Display Controller
AUX	Auxiliary
CMAC	Color/Monochrome Attributes Controller
CRTC	Cathode Ray Tube Controller
CTS	Clear to Send
CPU	Central Processing Unit
CR	Carriage Return
CRT	Cathode Ray Tube
DIN	German Industry Norm
DOS	Disk Operating System
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
DUART	Dual Asynchronous Receiver/Transmitter
EEROM	Electrically Erasable Read Only Memory
ESC	Escape
ESD	Electrostatic Sensitive Device
F-F	Flip-Flop
G0	User selected primary character set
G1	User selected alternate character set
IC	Integrated Circuit
LED	Light-Emitting Diode
LF	Line Feed
PAL	Programmable Array Logic
PIA	Peripheral Interface Adapter
PVTC	Programmable Video Timing Controller
RAM	Random Access Memory
RMS	Root Mean Squared
ROM	Read Only Memory
RTS	Ready to Send
RXD	Receive Data
SCS	Select Character Set
TLB	Terminal Logic Board
TXD	Transmit Data
VDC	Voltage Direct Current
XOFF	Transmit Off
XON	Transmit On

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Specifications

Video Display

CRT:	14″(35.5cm) diagonal, enhanced contrast, non-glare video screen. Z-49 screen: Chromogold™ screen (amber). Z-49G screen: P31 green phosphor.
Display Format:	25 rows of 80 characters or 25 rows of 132 characters.
Display Size:	6.75″(171mm) high × 9.25″(235mm) wide.
Character Type:	10 × 12 character cell for 80-column display. 8 × 12 character cell for 132-column display.
Character Size: (approximate)	.255″(6mm) high × .12″(3mm) wide for 80-column display. .255″(6mm) high × .07″(1.8mm) wide for 132-column display.
Character Set:	Normal: 128 characters; 95 printing ASCII, upper and lower case, numerics and punctuation, 33 Zenith graphic characters. Alternate: 128 characters; 32 graphic representation of non-printing ASCII 7 foreign character sets, 32 special Greek characters, and 32 graphic characters (VT-100).
Special Display Features:	Double-high double-wide characters per line, Double-wide characters, smooth scroll, and screen saver.
Video Attributes:	Normal or reverse character, normal or underlined character, variable intensity character and background, normal or blinking display.

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Specifications

Refresh Rate:	50 or 60 Hz.
Status Line:	25th line user programmable or indicates the terminal's status of: ON or OFF Line, Insert Mode, CAPS Locked, Printer Enabled.

Cursor

Type:	Underline or reverse (solid) video block.
Attributes:	On, Off, or blinking.
Addressing:	Direct or relative.

Communications

Type:	EIA RS-232C
Baud Rates:	50, 75, 110, 134.5, 150, 200, 300, 600, 1050, 1200, 1800, 2000, 2400, 4800, 7200, 9600, and 19200 baud. Different receive and transmit baud rates on the primary port, the same receive and transmit baud rates on the aux port.
Mode:	Half or full duplex on the primary port, full duplex on the aux port.
Code:	ASCII conforming to ANSI X3.4-1977.
Format:	Serial asynchronous.
Word Length:	7 data bits, 1 parity bit.
Stop Bits:	1 or 2.
Data Transmission Control:	Hardware and software (Auto XON and XOFF).
Parity:	Even, odd, mark, space, or none.

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Editing and Erasing Functions

Editing:	Insert or delete character. Insert or delete line.
Erasing:	Erase page, erase line, erase to end of line, erase to beginning of line, erase to beginning of page, and erase to end of page.

Printer Functions

Blind Mode:	Turns print controller on and off (echo from DTE port).
Auto Print:	Prints a display line after the cursor is moved off the line, using a form feed, line feed, vertical tab, or wraparound.
Print Cursor Line:	Prints displayed line with cursor.
Print Screen:	Prints the full screen or defined scrolling region.

Environment

Operation:	Temperature: 32 to 105 degrees Fahrenheit (0 to 40 degrees Celsius). Humidity: 10-90% (relative) noncondensing.
Storage:	Temperature: −40 to 150 degrees Fahrenheit (−40 to 66 degrees Celsius). Humidity: 0-95% (relative) noncondensing.

Power

Voltage Range:	105-127 VAC or 210-254 VAC.
Frequency:	50 or 60 Hz.

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Specifications

Fuse:	Video Display: 3 Ampere, slow-blow for 120 VAC operation; 1.5 Ampere, slow-blow for 240 VAC operation.
	Power Supply: 2 Ampere, 250 VAC.
Consumption:	73 Watts.

Dimensions

Monitor:	13.625″ high × 15.5″ wide × 14.25″ deep (34.6 cm × 39.4 cm × 36.2 cm).
Weight:	Monitor 22.8 pounds (10.37 kg).

Keyboard

Unit:	92-key, detached, low-profile, sculptured keys keyboard unit conforming to European DIN ergonomic standards with a 6-foot(182 cm) coiled cord.
Layout:	Split: 74-key QWERTY layout with 5 programmable special function keys, 8 indicators (LEDs), and an 18-key keypad with 14 numeric and 4 special programmable function keys.
Indicators:	Visual: POWER ON, KEYBOARD LOCKED, OFF LINE, CAPS LOCK, L1, L2, L3, and L4. Audible: Power on; beep. Print finished; beep. Margin bell; beep. Each key entry; click. Brightness high and low limits; beep. Save function; beep. Restore function; beep.

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Cursor Controls:	Up, down, left, right, backspace, tab, back tab, home, carriage return (CR), line feed (LF) and brightness.

Environment

Operation:	Temperature: 32 to 105 degrees Fahrenheit (0 to 40 degrees Celsius). Humidity: 10-90% (relative) noncondensing.
Storage:	Temperature: −40 to 150 degrees Fahrenheit (−40 to 66 degrees Celsius). Humidity: 0-95% (relative) noncondensing.

Dimensions

Keyboard:	1.35″ high × 18.25″ wide × 8″ deep (3.33 cm × 46.33 cm × 18.4 cm).
Weight:	Keyboard 3.8 pounds (1.73 kg).

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Introduction

The Zenith Data Systems Z-49 Terminal represents a truly state-of-the-art design capable of satisfying both business and personal needs. The many features include:

- Built-in power-up self check.
- Terminal emulation modes for both Zenith and ANSI (VT-100®/VT-102 compatible).
- Printing capabilities.
- Programmable character attributes and scrolling regions.
- Advanced keyboard features: automatic key repeat, status indicators, user defined function keys, and full cursor control keys.
- A height adjustable, detached, low-profile keyboard with sculptured keys and a six-foot coiled cable.
- All features are accessible through the keyboard, and a nonvolatile memory stores the settings.
- A professional 14-inch, non-glare screen with 24 rows of either 80 or 132 characters and a terminal 25th status line.
- Special attributes including double-high double-wide characters, double-wide characters, bold intensity, reverse video, blinking, underline capabilities and keyboard display brightness control.
- Character support for the following languages:

  DANISH

  FRENCH

  GERMAN

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ITALIAN

NORWEGIAN

SPANISH

SWEDISH

UNITED KINGDOM

USA

SPECIAL GREEK CHARACTERS

The built-in flexibility and ease of operation make the terminal one of the most versatile units available today. The terminal can serve as a remote unit of a powerful and expandable business automation package.

The SMZ-49 Manual

This manual is divided into the following sections:

Installation — Describes the hardware and provides information for configuration, interfacing, and power on.

Operation — Describes the keys, functions, and modes of the terminal.

Theory of Operation — Briefly describes the hardware theory of operation of the terminal.

Circuit Description — Provides detailed description of hardware circuitry.

Disassembly — Provides disassembly sequence and instructions to board level.

Service Procedures — Provides information on cleaning, inspection, testing, and troubleshooting to board level.

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Assembly — Provides reassembly instructions.

Parts List — Provides exploded views with part numbers, board component views, reference designator index to part numbers and semiconductor identification.

Data Sheets — Provides data for multifunctional integrated circuits.

Schematics — Provides a reference for circuit descriptions, testing, and troubleshooting.

Appendix A — Provides foreign keyboard information.

Appendix B — Provides escape sequence information.

List of Tools

1/4″ nut driver
4″ straight slot screwdriver
4″ #1 Phillips screwdriver
4″ #2 Phillips screwdriver
6″ diagonal cutters

Test Equipment

The following is a list of recommended test equipment for this unit. Equivalent test equipment may be substituted.

- Oscilloscope — DC to 100 MHz, dual trace, triggered sweep. Tektronics Model 465B.
- Logic Probe — DC to 20 MHz. Capable of detecting 10 ns single pulses, and indicating logic one, logic zeroes, and high impedance states. Heath Model IT-7410.
- Digital Voltmeter — High impedance input, zero to 1000 volts, zero to one megohm. Heath Model SM-2215.

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- Variable Power Supply — Zero to 120 VAC RMS, 3 amperes. Heath Model IM-5210.
- Low Capacitance Oscilloscope Probe — Input capacitance adjustable from 15 pf to 50 pf, 4 ns rise time. Heath Model PKW-105.
- Video Monitor — RGB color and monochrome composite wide band monitor. Zenith Model ZVM-135.
- High Voltage Probe — Zero to 40 kV. Heath Model IM5210.

List of Supplies

DESCRIPTION	PART NUMBER
Heat sink compound	205-00303
Cable ties	HE 354-5
Fuse 3AG slow blow	HE 421-6

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Chapter 1

Installation

Introduction

The Zenith Data Systems terminal has two main components: a video display and a detached keyboard. The two are connected to each other with a 6-foot coiled cord. In addition to this documenation and the above components, a *Programmer's Quick Reference Guide* and an RS-232C cable are included.

NOTE: If you use a printer, you must use a null modem cable, part number HE 134-1454. Verify that the printer is configurable with the null modem cable.

Refer to Figure 1.1 for a description of the plugs (connectors) on the video display and keyboard.

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Video Display

Refer to Figure 1.1.

The following is a rear view description of the video display. Be sure the video display power ON/OFF switch is in the OFF position and the line cord is unplugged from the AC power source. Turn the video display until the back is visible.

Power ON/OFF Switch — Turns the terminal ON or OFF.

WARNING: Be sure power is OFF when replacing the fuse.

FUSE — Provides circuit protection due to component failure and line voltage surges.

CAUTION: Replace only with a properly rated fuse.

Line Cord Connector — Connects power to the terminal.

Connector (AUX) — Connector for printer.

DTE Connector (MAIN) — Connector for computer or modem.

Keyboard Connector — Connector for keyboard cable.

Keyboard

Refer to Figure 1.1.

The following is a description of the keyboard unit.

Keyboard cable — Connects the keyboard to the video display.

Keyboard — The keyboard consists of 92 keys, a connector, eight visual indicators (LEDs), and is available in eight different languages.

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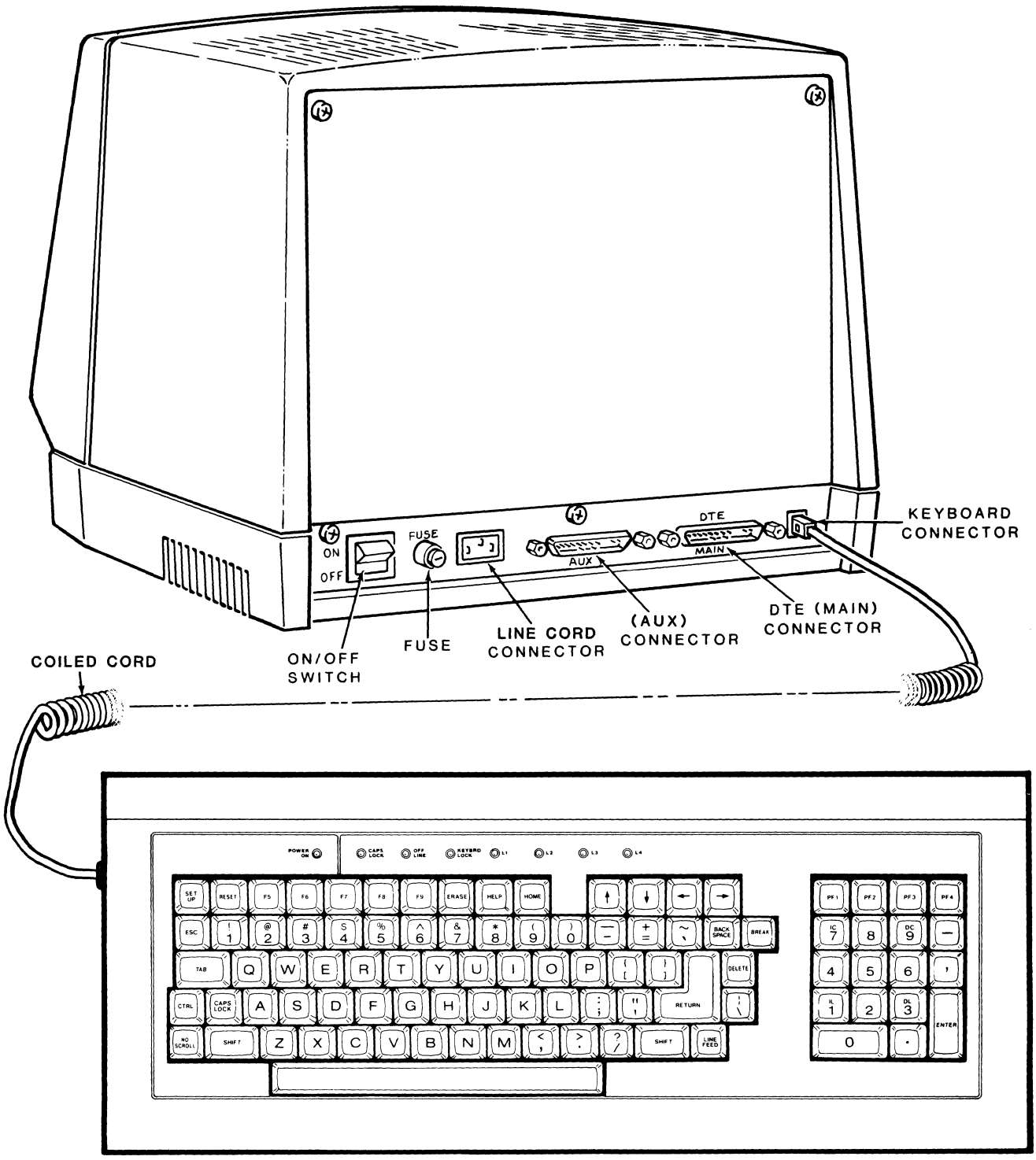

Figure 1.1. Rear Panel View

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Keyboard Indicators

Refer to Figure 1.2.

POWER ON — lights when power is on and the keyboard is properly connected.

CAPS LOCK — Lights when the CAPS LOCK function is on.

OFF LINE — Lights when the terminal is off line with the host computer.

KEYBRD LOCK — Lights when the keyboard unit is locked or the terminal is printing. The keyboard must be enabled to operate.

L1 through L4 — Lights when instructed, by a user program.

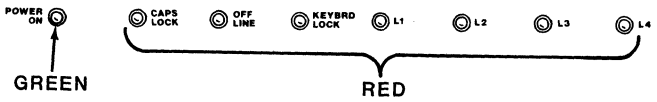

Figure 1.2. LED Indicators

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Keyboard Tilt Adjustment

Refer to Figure 1.3.

You can raise the tilt of the keyboard by pressing the two tabs located in back of the unit.

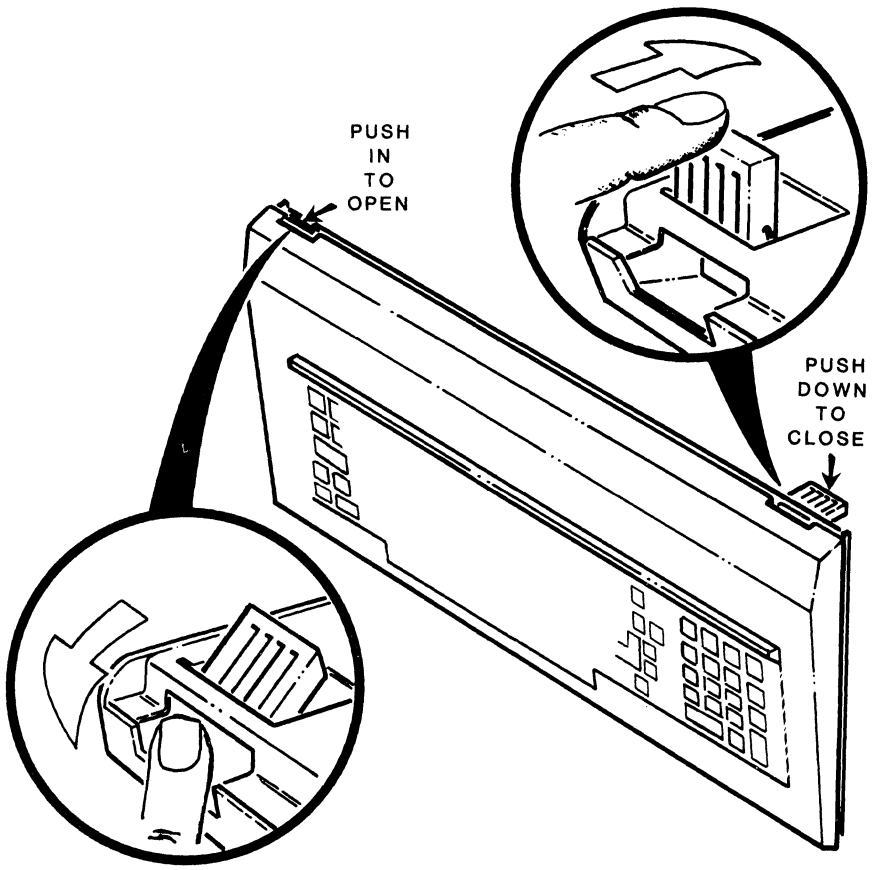

Figure 1.3. Tilt Adjustment

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Voltage Selection

Before connecting the terminal, make sure it is rated for the voltage available in your area. The terminal is wired for 120 VAC. To change the voltage rating to 240 VAC, refer to Figure 1.4 and perform the following six steps:

WARNING: This power supply contains lethal DC voltages. The line cord must be unplugged before proceeding with the following steps.

1. Place the terminal on a selected work surface so that the back is accessible.

2. Remove the two screws at point A and two screws at point B; then remove the back cover.

3. Remove two 6-32 × .375 screws (C) and the cover from the power supply.

4. Figure 1.4 (inset) depicts the jumper used to select either 115 VAC or 230 VAC operating voltage. Pull the jumper straight up and connect the jumper to the pins corresponding to the correct operating voltage.

5. Replace the power supply cover and the two screws that were removed in step 3.

6. Replace the back panel and the four screws that were removed in step 2.

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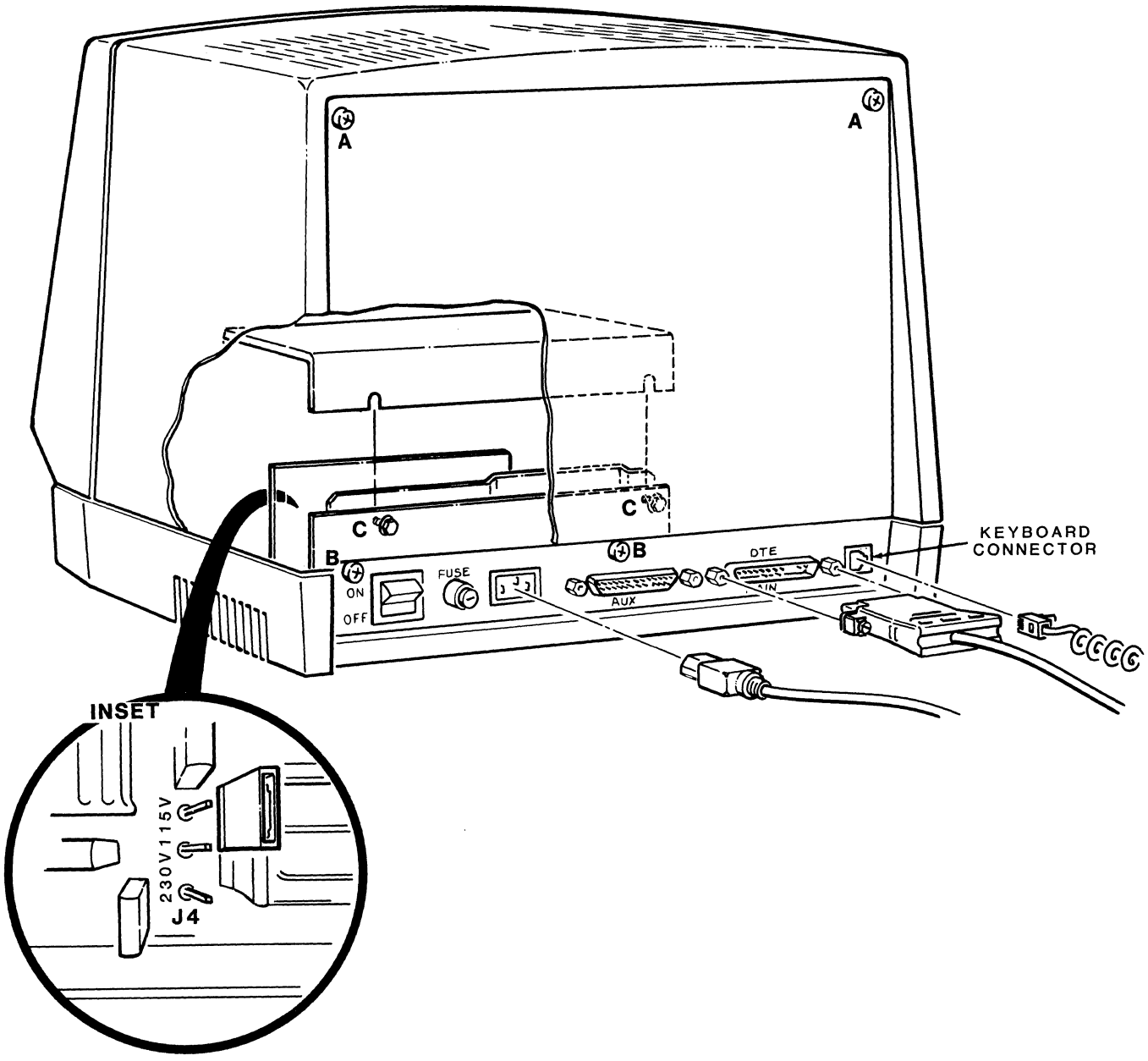

Figure 1.4. Voltage Adjustment

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Connections

To install and connect the terminal, refer to Figure 1.4 and complete the following procedure:

- Place the video display on a solid work surface and turn it until the back is facing you.
- Locate the coiled keyboard cable. Connect it to the keyboard connector on the back of the video display.

CAUTION: The coiled cable assembly resembles a conventional telephone cord. DO NOT attempt to connect the end to a telephone plug or keyboard damage could result.

- Connect the line cord to the line cord connector.

Interfacing

The terminal is designed to be used as an input/output (I/O) device for a computer system. The terminal may be connected directly or through telephone lines (via a modem) to any computer. The following discussion covers some of the considerations for proper installation with a computer.

CAUTION: A shielded cable must be used. A shielded cable is required for the terminal by FCC regulations.

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DTE Device

Refer to Figure 1.4.

On the back panel of the terminal, there are two standard connectors, marked AUX and DTE (MAIN). The DTE (MAIN) connects to the host computer or modem and AUX to the printer.

Table 1.1 provides information on the DTE connector, and Table 1.2 provides information on the AUX connector.

NOTE: The computer or modem used with the terminal must meet RS-232C standards or improper operation may result.

Table 1.1. Primary Serial Connector (DTE)

PIN #	SIGNAL NAME	INPUT/OUTPUT I/O	SIGNAL FUNCTION
1	GND	–	Protective Ground
2	TXD	O	Transmitted Data
3	RXD	I	Received Data
4	RTS	O	Request to Send
5	CTS	I	Clear to Send
6	DSR	I	Data Set Ready
7	GND	–	Signal Ground
8	CD	I	Carrier Detect
11	SS	O	Reserved
12	SI	I	Reserved
20	DTR	O	Data Terminal Ready
22	RI	I	Reseved

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Table 1.2. Aux Connector (Printer Port)

PIN #	SIGNAL NAME	INPUT/OUTPUT I/O	SIGNAL FUNCTION
1	GND	–	Protective Ground
2	TXD	O	Transmitted Data
3	RXD	I	Received Data
6	DSR	I	Data Set Ready
7	GND	–	Signal Ground
20	DTR	O	Data Terminal Ready

When connecting the terminal directly to a computer, connect the RS-232C cable into the DTE connector and the other end into the computer's DCE connector (refer to the computer hardware manual for the proper connector).

When connecting the terminal to a modem, connect the RS-232C cable into the DTE connector and the other end into the modem's (DCE) connector (refer to the modem hardware manual for the proper connector).

When you connect the terminal to a printer, you must use a null modem cable (HE 134-1454). Plug the printer cable into the AUX connector. The baud rate setting in AUX port parameters applies to both transmit and receive. Configure the terminal to the desired printer baud rate.

Make sure the power switch is OFF, then plug the power source into an AC outlet (wall plug).

Rotate the video display, so that the screen is facing you.

Press the power switch to ON.

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Self-Check Tests

As soon as you turn on the terminal, a series of internal self-check tests are performed to verify proper operation. If no faults are found, a beep will sound. If a problem is detected, an error message may be printed on the video display. Table 1.3 lists the tests performed and the corresponding error messages. Refer to Chapter 6, "Service Instructions," for further information and instructions.

Table 1.3. Self-Check Tests

TEST	ERROR MESSAGE
ROM	ROM Checksum
RAM	RAM Fault
CRT Controller	CRTC Error
Keyboard	Keyboard
Nonvolatile RAM	NVRAM Checksum
CPU Interrupt	CPUFIRQ ERROR
Communications Port	DUART Error

POWER ON Indicator

When you turn the terminal ON, the POWER ON indicator (LED) should light. If the POWER ON indicator is not lit, either the keyboard is not connected to the terminal correctly or the terminal is not connected to an acceptable power source.

After 10 to 30 seconds a cursor should appear in the upper left corner of the screen. The 25th line also may display one or more messages: CAPS Lock, OFF Line, or ON Line.

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Chapter 2

Operation

Introduction

The Z-49 Terminal uses the latest in solid-state technology for setting up and maintaining vital communication functions. You can enter these functions quickly and easily through the keyboard. This section covers the keyboard keys and setting up the features and functions of the terminal.

Alphabetic Keys

Refer to Figure 2.1.

The terminal's keyboard has the standard 26 letters of the alphabet arranged the same as a normal typewriter (QWERTY). The F and J keys are recessed to help determine the home row position. These keys will function in either upper or lower case. Press the SHIFT key or CAPS LOCK key to use upper case.

The CAPS LOCK key will light a keyboard indicator (CAPS LOCK) when enabled. If the status indicator line on the video display is on, a CAPS LOCK message will be displayed. The CAPS LOCK key affects only the alphabetic keys.

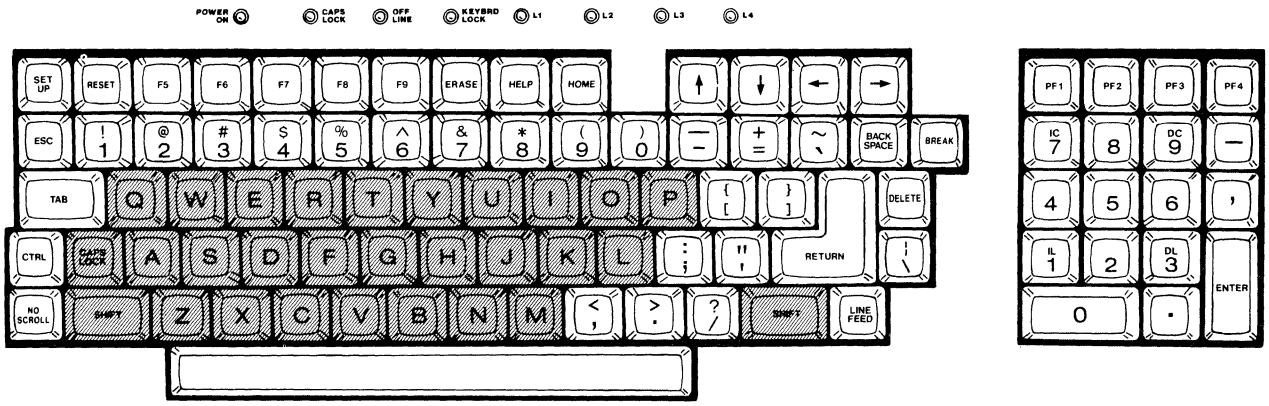

Figure 2.1. Alphabetic Keys

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Nonalphabetic Keys

Refer to Figure 2.2.

Nonalphabetic keys include the numbers 0 through 9, punctuation marks, and special characters. The lower marking on each key is generated when the SHIFT keys are not held down. The upper marking will be generated when either SHIFT key is held down. The CAPS LOCK key will not shift these keys.

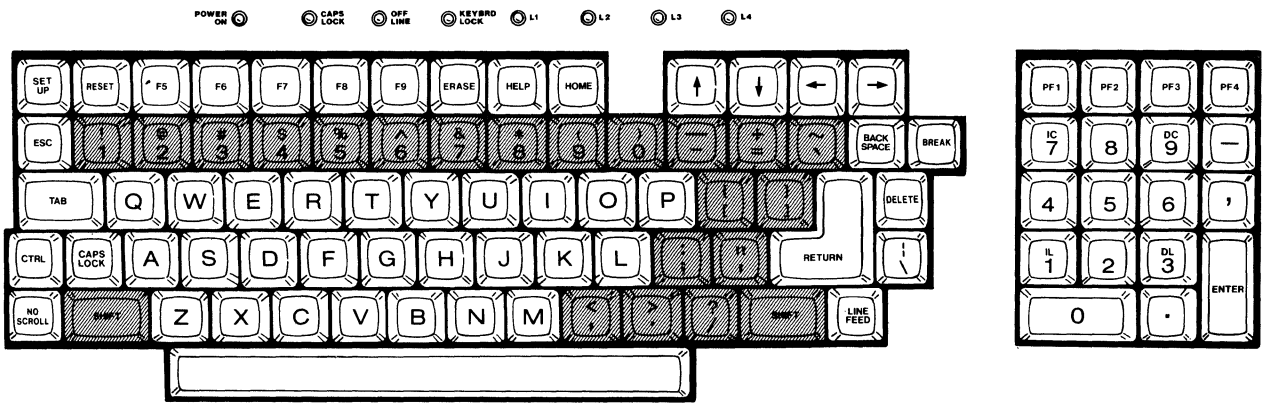

Figure 2.2. Nonalphabetic Keys

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Control Format Keys

Refer to Figure 2.3.

NOTE: The following discussions describe the most common function for each key. However, software may direct any key to cause some other function to take place. Any key that has a special function is usually described in the documentation for that program.

Space Bar — Functions the same as a typewriter. A blank character can be entered by pressing the space bar.

BACK SPACE — Functions the same as a typewriter. Pressing the BACK SPACE key moves the cursor one space to the left.

TAB — Positions the cursor to the next tab column as set by software or in the Setup mode. If you press either SHIFT key and the TAB key simultaneously, the cursor will move to the previous tab column.

RETURN — Returns the cursor to the first character on the left side of the display, not necessarily advancing to the next line.

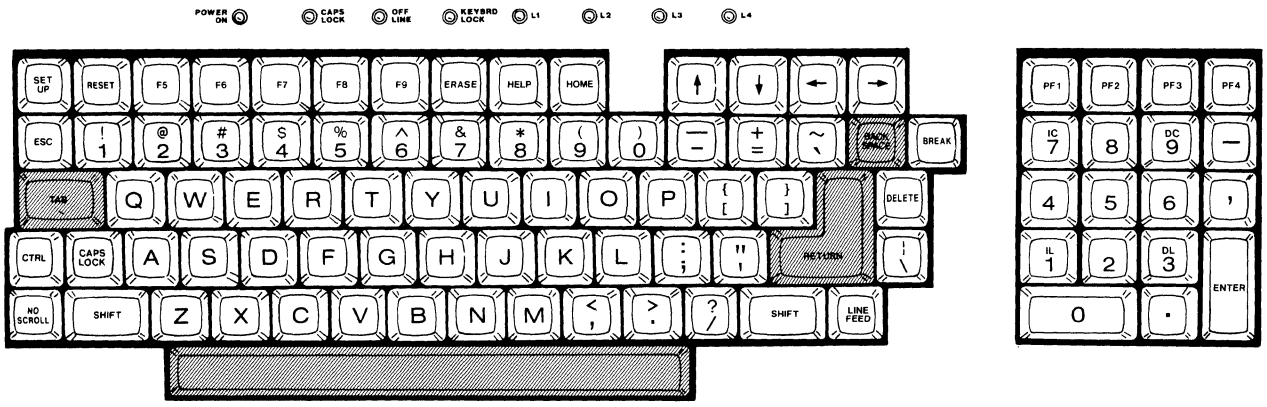

Figure 2.3. Control Format Keys

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Keypad Keys

Refer to Figure 2.4 for the following discussion of the keypad.

Calculator Style Keypad — The group of keys, located to the right of the main keyboard, is organized somewhat like a calculator and includes: numbers 0 through 9; a period for the entry of decimal points; a comma for data entry; a dash for the entry of negative numbers; and an ENTER key for signaling the computer that the entry has been completed.

The 5 key has a raised dimple to indicate the "home" position of the calculator keypad.

Four Keys: 1, 3, 7, and 9 are used for special insertion and deletion applications using the shifted mode. Key 1 (IL) is used to insert a line. Key 3 (DL) is used to delete a line. Key 7 (IC) is used to insert a character, and key 9 (DC) is used to delete a character.

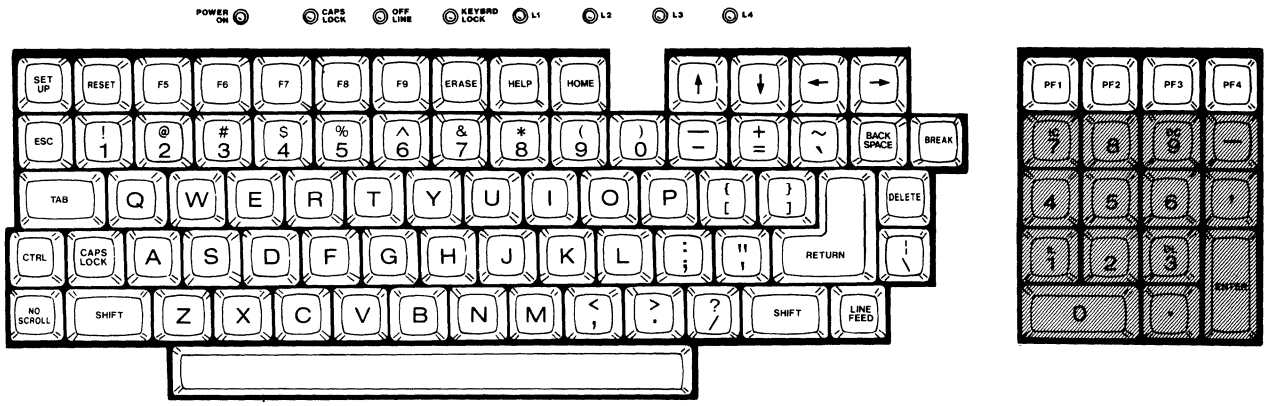

Figure 2.4. Keypad Keys

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Special Purpose Keys

Refer to Figure 2.5 for the following discussion of keyboard functions.

The following keys are used for special purposes and are nonrepeating. Instructions that tell you how to use them will appear with the software programs.

PF1 through PF4 and F5 through F9 — Special function keys used for special purposes by software, or may be user-defined.

RESET — This key is used with the right-hand SHIFT key to "hardware reset" the terminal.

ERASE — This key erases the screen from the cursor to the bottom of the screen. The ERASE key and either SHIFT key are used to erase the entire screen.

HELP — Used by software programs to provide special "prompts" or "helps."

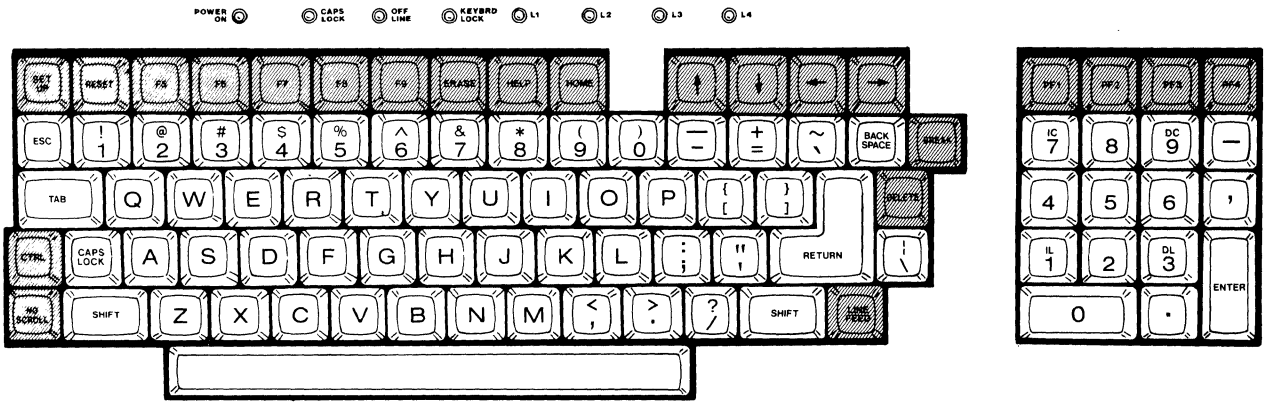

Figure 2.5. Special Purpose Keys

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HOME, ↑ (up arrow), ↓ (down arrow), ← (left arrow), → (right arrow) and **LINE FEED** are cursor control keys. These keys are used by some programs to control cursor movement and screen presentation.

BREAK — This key generates a 233.3 millisecond signal to interrupt (modem) communications. The BREAK key and either SHIFT key generate a 3.5 second signal for modem disconnect.

DELETE — Deletes one character to the left, or sometimes in software duplicates the BACK SPACE.

NO SCROLL —

Hold Screen enabled:

- Pressing the NO SCROLL key displays the next line of data.
- Pressing the NO SCROLL and either SHIFT key displays the next full page (24 lines).

Hold Screen disabled.

- Hardware and none-handshaking options disabled.
- Pressing the NO SCROLL key generates XON or XOFF commands.

NOTE: The following keys are used in a combination with other keys to perform a function.

ESC — The ESC (ESCAPE) key generates a control code for escape sequences.

EXAMPLE: ESCrA

In the above example, press and release the **ESC** key, press and release the lower case **r** key, and press and release the capital **A** key.

CTRL — Pressing the CTRL (CONTROL) key and another key at the same time performs a special function. Refer to Appendix B for more information.

Pressing the CTRL and ENTER will enter and exit auto print. Exiting or entering the Setup mode will terminate current printing.

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The CTRL and BREAK keys pressed at the same time generate a programmed answer-back message.

SHIFT — Pressing the SHIFT and ENTER keys will transmit the entire contents of the screen to the printer. Entering the Setup mode will terminate printing.

SET UP — Used to enter or exit the Setup mode. When printing, entering the Setup mode will terminate printing.

The terminal's functions are programmed in the Setup mode. To enter the Setup mode, press the **SET UP** key. The terminal will display the Main menu and be "off line".

NOTE: The terminal cannot communicate with the host computer until you exit the Main menu. The SET UP key sends an XOFF when entered and an XON when exited.

NOTE: Many of the setup procedures can be programmed by using software escape sequences. For more information about escape sequences, see Appendix B.

Brightness is controlled by pressing the **SET UP** key and then pressing either the up arrow (↑) key to increase contrast or the down arrow (↓) key to decrease contrast. A beep will sound whenever the high and low limits of brightness are reached.

The Main menu is shown in reverse, bold, and normal video on the bottom four lines of the screen (lines 22 through 25).

The selections displayed are: ON or OFF line, Primary port, Aux port, Display, Cursor, Keyboard, Set tabs, Monitor ON or OFF, Mode ANSI or ZENITH, Misc, Restore, Save, and Programmable keys.

Each function selected will display its status (current value). You may temporarily change or store the current value as explained in this section.

The cursor keys and auto repeat will be inoperative when you are in the Main menu, except for selected keys at selected times.

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Entering the Setup Mode

To enter the Main menu, press the **SET UP** key. The bottom four lines will indicate a display similar to this Main menu.

```
A ON line       D Display   G Set tabs       J Misc      PF1  PF4  F7
B Primary port  E Cursor    H Monitor ON     R Restore   PF2  F5   F8
C Aux port      F Keyboard  I Mode ANSI      S Save      PF3  F6   F9
  MAIN  MENU        (Press SETUP to exit)     Programmable keys
```

Main Menu Selection

To select a function or feature, press the corresponding key.

Each function or feature is associated with an alphabetical key. You can temporarily change the current value of the function by pressing the alphabetical key as many times as necessary until you obtain the desired configuration, and then exiting the Main menu, or a new submenu (feature) can be displayed by pressing the appropriate alphabetical key. To exit the Main menu, press the **SET UP** key.

To store a new current value, press the **CTRL** key and the **S** (SAVE) key while in the Main menu. The screen will display the message SAVING and a beep will sound. When SAVING disappears, a beep sounds, the screen will display the Main menu, and the new current value will be stored.To exit the Main menu, press the **SET UP** key.

NOTE: Entering and exiting the Setup mode will cancel the current print option without a termination character. When printing is resumed, the printer will start printing from the previous postion unless a termination character is sent.

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ON/OFF Line

The terminal is an input/output device for a computer whenever it is on-line.

When the terminal is off-line, it is controlled only through the keyboard, and no information can be received from or transmitted to the host computer.

When the OFF Line mode is selected, OFF LINE will be displayed on the terminal status line of the screen and the OFF LINE indicator will be lit. When the terminal is ON Line, the OFF LINE indicator will not be lit and the status line will display ON LINE.

You can change ON/OFF Line from the Main menu by pressing the A key. The ON/OFF Line selection will be effective upon exiting the Main menu.

Primary Port Parameters

To change the Primary port parameters in the Main menu, press the **B** key. The bottom four lines will indicate a display similar to:

```
A Rcv baud 9600      D Handshake SOFTWARE      G Stop bits  1
B Xmt baud 9600      E RTS/CTS busy LOW        H Parity EVEN
C Duplex   FULL      F DTR/DSR busy LOW
 PRIMARY PORT PARAMETERS     (Press SET UP to return to main menu)
```

Baud Rate

The terminal can use a variety of baud rates to communicate with the host computer. These rates are: 50, 75, 110, 134.5, 150, 200, 300, 600, 1050, 1200, 1800, 2000, 2400, 4800, 7200, 9600, and 19200 baud. The display shows a current value of 9600 baud.

The primary port can receive and transmit data at different baud rates.

- The receive baud rate can be changed by pressing the A key.

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- The transmit baud rate can be changed by pressing the B key.
- Pressing the up arrow (↑) key increases both the receive and transmit baud rates.
- Pressing the down arrow (↓) key decreases both baud rates.

Press the desired key(s) as many times as necessary until the desired baud rate(s) is displayed. The new baud rate will become effective when you exit the Main menu.

Duplex Mode

The terminal can communicate with the host computer in either the FULL or HALF Duplex mode.

- FULL duplex is simultaneous communication between the terminal and the host which displays the data returned from the computer.
- HALF duplex is one-way communication between the terminal and the computer, but not at the same time. The terminal will display the data from the keyboard.

You can change the Duplex mode between FULL and HALF Duplex by pressing the C key. The new Duplex mode will become effective when exiting the Main menu.

Handshaking

The terminal uses four methods of handshaking: Software, Hardware, Both, or None.

In the Software handshake mode, the terminal will automatically generate the XON or XOFF codes.

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Hardware handshaking is performed through the use of four control lines via the DTE (MAIN) connector. The four lines are: CTS (Clear to Send), RTS (Request to Send), DSR (Data Set Ready), and DTR (Data Terminal Ready).

Both handshaking is a combination of hardware and software handshaking.

The None option disables handshaking between the terminal and host computer.

You can change the Handshaking mode by pressing the D key until the desired mode is displayed. The new Handshaking will become effective when exiting the Main menu.

RTS/CTS Busy

The RTS/CTS function uses two methods of communication.

- Hardware handshaking must be enabled.
- RTS (Request to Send) is a signal from the terminal to the host computer.
- CTS (Clear to Send) is a signal from the host computer to the terminal (ignored).

The two signals are RTS/CTS busy LOW, and RTS/CTS busy HIGH. Normal RS-232 operation is RTS/CTS busy LOW.

If you change the above functions, the terminal can respond to either busy LOW or busy HIGH signals.

You can change this function by pressing the E key until the desired method of communication is displayed. RTS/CTS busy will become effective when exiting the Main menu.

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DTR/DSR Busy

The DTR/DSR function uses two methods of communication.

- Hardware handshaking must be enabled.
- DTR (Data Terminal Ready) is a signal from the terminal to the host computer.
- DSR (Data Set Ready) is a signal from the host computer to the terminal (ignored).

The two signals are DTR/DSR busy LOW, and DTR/DSR busy HIGH. Normal operation per RS-232 is DTR/DSR busy LOW.

If you change the above functions, the terminal can respond to either busy LOW or busy HIGH signals.

You can change this function by pressing the F key until the desired method of communication is displayed. The new DTR/DSR busy will become effective when exiting the Main menu.

Stop Bits

The terminal operating in the Zenith or ANSI modes uses one stop bit at all baud rates. When operating at 110 baud, some systems require two stop bits.

You can change stop bits by pressing the G key until the desired Stop bit option is displayed. The new Stop bits will become effective when exiting the Main menu.

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Parity

The available parity options are: ODD, EVEN, MARK, SPACE, and NONE. MARK and SPACE are used in modem communications. The data word with and without parity is outlined as below.

- Seven bits with parity; parity being EVEN, ODD, MARK, or SPACE. The eighth bit will be set according to the parity selected.
- Seven bits with no parity; the eighth bit will be forced to zero (no parity checking will be performed).

You can change the parity option by pressing the H key until the desired option is displayed. Parity will become effective when exiting the Main menu.

NOTE: The terminal has parity sensing capabilities. If the data received is the wrong polarity, the VT-100 graphic character for 61 HEX is displayed.

Aux Port Parameters

To change the Aux port parameters, in the Main menu press the **C** key. The bottom four lines will indicate a display similar to:

```
A R/T baud 9600      D Handshake SOFTWARE      G Stop bits  1
B Auto Print OFF     E End With Form Feed OFF  H Parity  EVEN
C Blind Print OFF    F DTR/DSR Busy LOW        I Extent  ENTIRE SCREEN
 AUX PORT PARAMETERS     (Press SETUP to return to main menu)
```

Baud Rate

The terminal can use a variety of baud rates to communicate with the printer. These rates are: 50, 75, 110, 134.5, 150, 200, 300, 600, 1050, 1200, 1800, 2000, 2400, 4800, 7200, 9600, and 19200 baud. The display shows a current value of 9600 baud.

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The receive and transmit baud rates can only be increased or decreased at the same time.

- You can increase the receive and transmit baud rates by pressing the A key or up arrow (↑).
- You can decrease the receive and transmit baud rates by pressing the down arrow (↓).

Press the desired key(s) as many times as necessary until the desired baud rate is displayed.

The new baud rates will become effective when exiting the Main menu.

Auto Print

Auto print prints a display line after the cursor moves to the next line via a line termination character (LF, CR, or VT).

- Prints during WRAP with a line termination character of CR or LF.
- Double-high/double-wide lines are converted to single-wide lines when printed.
- Double-wide characters are converted to single-wide characters followed by a space when printed.
- Exiting the Setup mode will terminate printing of the current line only.
- After Restore, the Auto print status remains until any type of reset is initiated.
- The terminal will automatically generate the proper GO character set to the printer.

The Auto print mode can be turned on or off by pressing the B key.

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Blind Print

Blind print enables the print controller. The terminal transmits received characters to the printer without displaying them.

- The terminal does not insert or delete spaces, provide line delimiters, or select character sets.
- Blind print has a higher priority than Auto print.
- During this operation, a print page can be initiated from the keyboard by pressing the SHIFT and ENTER keys simultaneously.
  - — A beep will sound after the print page is printed.
  - — Exiting the Setup mode will terminate printing.
  - — The terminal will automatically change the character set and then reset the character set to the original value, if the print page is initiated.
- After Restore, the Blind print status remains until any type of reset is initiated.

The Blind print mode can be turned ON or OFF by pressing the C key.

Handshaking

The two methods of handshaking are Software or Both.

In the Software handshake mode, the terminal will look for the XON or XOFF codes from the printer.

- The XOFF code tells the terminal that data transmission to the printer should cease.
- The XON code tells the terminal that data transmission to the printer can be resumed.

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Both handshaking is a combination of hardware and software handshaking.

NOTE: Software handshaking always is on.

Hardware handshaking is performed through the use of two control lines via the AUX connector.

The two lines are: DSR (Data Set Ready) and DTR (Data Terminal Ready).

You can change the Handshaking mode by pressing the D key until the desired mode is displayed. The new Handshaking mode will become effective when you exit the Main menu.

End With Form Feed

Screen print always ends with a line feed; also, it can end with a form feed. This option can be set to ON by pressing the E key.

DTR/DSR Busy

The DTR/DSR function uses two methods of communication.

- Both handshaking must be enabled.
- DTR (Data Terminal Ready) is a signal from the terminal to the printer.
- DSR (Data Set Ready) is a signal from the printer to the terminal.

The two signals are DTR/DSR busy LOW and DTR/DSR busy HIGH. Normal operation per RS-232 is DTR/DSR busy LOW.

You can change this feature by pressing the F key until the desired method of communication is displayed.

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Stop Bits

The terminal operating in the Zenith or ANSI modes uses one Stop bit at all baud rates. When operating at 110 baud some systems require two stop bits.

You can change Stop bits by pressing the G key until the desired Stop bit option is displayed. The new Stop bits will become effective when you exit the Main menu.

Parity

The available parity options are: ODD, EVEN, MARK, SPACE, and NONE. MARK and SPACE are used in modem communications. The data word with and without parity is outlined as below.

- Seven bits with parity; parity being EVEN, ODD, MARK, or SPACE. The eighth bit will be set according to the parity selected.
- Seven bits with no parity; the eighth bit will be forced to zero (no parity checking will be performed).

You can change the parity option by pressing the H key until the desired option is displayed. Parity will become effective when you exit the Main menu.

Extent

Extent is an option between printing the entire screen or the defined scrolling region.

The desired option can be selected by pressing the I key.

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Display Parameters

To change Display parameters, in the Main menu press the **D** key. The bottom four lines will indicate a display similar to:

```
A Wrap           OFF   D Screen saver   OFF  G Scroll       JUMP
B Auto LF on CR  OFF   E Status Line    ON   H Hold Screen  OFF
C Auto CR on LF  OFF   F Columns        80
 DISPLAY PARAMETERS       (Press SETUP to return to main menu)
```

Wrap

The Wrap (wraparound) is a feature that allows you to continue to enter data after reaching the end of a line, without a loss, by generating a CR or LF.

- Depending on the terminal's configuration, a line may be 80 or 132 characters.
- When Wrap is on, the next character you enter after you reach the end of a line, will start the next line.
- If the line is at the bottom of the screen, the screen will be scrolled (moved) up one line.
- When Wrap is off, the character at the end of the line will be over-printed.

You can turn the Wrap function on or off by pressing the A key. The Wrap function will become effective when exiting the Main menu.

Auto LF on CR

When Auto (Automatic) LF (Line Feed) on CR (Carriage Return) is ON, a line feed is generated whenever a carriage return is received.

You can turn the Auto LF on CR ON or OFF by pressing the B key. Auto LF on CR will become effective when exiting the Main menu.

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Auto CR on LF

When Auto (Automatic) CR (Carriage Return) on LF (Line Feed) is ON, a carriage return is generated whenever a line feed is received.

You can turn the Auto CR on LF ON or OFF by pressing the C key. Auto CR on LF will become effective when exiting the Main menu.

Screen Saver

The screen will be automatically "blanked out" if no key is pressed or no data is received by the terminal for 15 consecutive minutes. This function increases the life of the screen.

The screen can be restored by pressing any key, or reception of data from the host computer, or auxiliary port via the serial channels.

You can turn the Screen saver function ON or OFF by pressing the D key. The selection will become effective immediately.

Status Line

The terminal Status Line (25th) on the CRT displays the following information after you exit from the Main menu: CAPS LOCK if the CAPS LOCK is enabled, OFF LINE if the terminal is in the Off-Line mode or ON LINE if the terminal is On-Line, Printer if the printer line is enabled, and INSERT MODE if the terminal is in the Insert mode.

You can turn the Status Line ON or OFF by pressing the E key. The terminal Status Line is not displayed until exiting the Main menu.

Columns

This function allows you to select between 80- or 132-character Columns (characters per line).

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You can select the desired number of Columns by pressing the F key. The selection will become effective immediately.

NOTE: When you change the number of Columns, the display is cleared and the data previously displayed is lost.

Scroll

The terminal is capable of scrolling the screen up in two modes, JUMP and SMOOTH Scroll.

- JUMP Scroll moves one character line up at a time.
- SMOOTH Scroll improves readability from rapidly received data by scrolling part of a character line up, instead of a whole line.

You can select the Scroll function desired by pressing the G key. The Scroll selection will become effective when exiting the Main menu.

NOTE: Screen flicker may occur when you select SMOOTH Scroll.

Hold Screen

The Hold Screen function operates in the Zenith mode only.

- When you enable the Hold Screen function, pressing the NO SCROLL key displays a new line of received information.
- You can display an entire new page of received information by pressing the NO SCROLL key and either SHIFT key at the same time.
- When the Hold Screen function is OFF, the NO SCROLL key generates a software handshake. Refer to Appendix B for more information.

You can turn the Hold Screen function ON or OFF by pressing the H key. The new Hold Screen selection will become effective when exiting the Main menu.

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Cursor Parameters

To change the Cursor parameters, in the Main menu press the **E** key. The cursor will be disabled while in the Main menu. The bottom four lines will indicate a display similar to:

```
A Cursor   ON
B Blink    ON
C Shape    UNDERLINE
 CURSOR PARAMETERS            (Press SETUP to return to main menu)
```

Cursor

You can turn the Cursor ON or OFF by pressing the A key. The cursor selection will become effective when exiting the Main menu.

Blink

When the Blink function is OFF, the cursor is a steady solid character line or block. When the Blink function is ON, the cursor blinks.

You can turn the Blink function ON or OFF by pressing the B key. The Blink selection will become effective when exiting the Main menu.

Shape

The Shape function selects either an UNDERLINE or BLOCK cursor.

You can select the desired shape by pressing the C key. The Shape selection will become effective when exiting the Main menu.

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Keyboard Parameters

To change the Keyboard parameters, in the Main menu press the **F** key. The bottom four lines will indicate a display similar to:

```
A Key Click     ON        D Auto repeat   ON
B Keypad shift  OFF       E Margin Bell   OFF
C Keypad alt    OFF       F New Line      OFF
 KEYBOARD PARAMETERS    (Press SETUP to return to main menu)
```

Key Click

Key Click is an audible click indicating that a key entry has been made. Keys that modify other keys, such as SHIFT and CTRL, will not sound the click when pressed individually.

You can turn the Key Click function ON or OFF by pressing the A key. The Key Click selection will become effective immediately.

Keypad Shift

When the Keypad shift is OFF, the numeric characters on the keypad are transmitted by pressing the desired key. The shifted characters are transmitted by pressing the SHIFT and desired key.

When Keypad shift is ON, characters normally shifted are transmitted by pressing the desired key. The numeric characters are transmitted by pressing the SHIFT and the desired numeric key.

You can turn the Keypad shift ON or OFF by pressing the B key. The Keypad shift selection will become effective when you exit the Main menu.

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Keypad Alt

When Keypad alt is ON, the keypad transmits alternate function codes to identify keypad keys from keyboard keys.

You can turn Keypad alt ON or OFF by pressing the C key. The Keypad alt will become effective when exiting the Main menu.

Auto Repeat

When the Auto repeat function is ON, pressing and holding any key except the SHIFT, CAPS LOCK, SET UP, RESET, BREAK , RETURN, ENTER, HELP, ESC, TAB, NO SCROLL, and CTRL for more than one-half second will cause the key to be repeated.

- The longer the key is held down, the faster the repeat rate, until the maximum repeat rate is reached.
- The key will continue to repeat until released.

You can turn the Auto repeat function ON or OFF by pressing the D key. The Auto repeat selection will become effective immediately.

Margin Bell

The Margin Bell provides an audible right margin warning beep. The beep sounds eight columns before the end of either a 80- or 132-column line.

You can turn the Margin Bell ON or OFF by pressing the E key. The Margin bell selection will become effective when exiting the Main menu.

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New Line

The New Line feature generates a CR or CR and LF.

- A CR and LF is generated by pressing the RETURN or ENTER key when the New Line feature is ON.
- A CR is generated by pressing the RETURN or ENTER key when the New Line feature is OFF.

The selected mode of operation will become effective when exiting the Main menu.

Set Tabs

To enter the Set tabs mode, in the Main menu press the **G** key. The four bottom lines will indicate a display (either 80 characters or 132 characters) similar to:

```
   T  T     T         T T T          TT          T                T         T
12345678901234567890123456789012345678901234567890123456789012345678901234567890
SET TABS                          ( Press SETUP to return to main menu )
```

- Capital T's represent tab locations.
- You can set or clear the tabs by moving the cursor block left or right with the appropriate arrow keys to the desired location.
- Use the up arrow (↑) to set the tab.
- Use the down arrow (↓) to clear the tab.
- Press the upper or lower case **c** to clear all tabs.

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- Press the upper or lower case **t** to clear all tabs and automatically set the tabs every eight columns.
- When the TAB key is pressed, the cursor will move to the next tab location.
- When the RETURN key is pressed, the cursor will be moved to the next margin.

The tab selections will become effective when exiting the Main menu.

Monitor Mode

The Monitor mode displays the control character codes, as graphic characters in reverse video.

- Normal configuration is OFF.
- When you use the Monitor mode, the Wrap feature should be enabled to verify data transmitted to the terminal.
- The terminal will not respond to any control or escape codes while in this mode.

You can turn the Monitor function ON or OFF by pressing the H key. The Monitor selection will become effective when exiting the Main menu.

Mode ANSI/Zenith

The terminal emulates two modes of operation: ANSI X3.64-1979 (similar to the VT100) and Zenith. Each of the two modes respond differently to received codes.

You can change the mode of operation in the Main menu by pressing the I key. The selected Mode of operation will become effective when exiting the Main menu.

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Misc

To change the Misc parameters, in the Main menu press the **J** key. The bottom four lines will indicate a display similar to:

```
A Char Font  USA              D Self test, one pass
B Line Freq 60 Hz             E Self test, continuous
C Change answer back,      message=<current answer back message>
 MISC               (Press SETUP to return  to main menu)
```

Char Font

The terminal has available eight character font options. The options are: USA, Danish, French, German, Italian, Norwegian, Spanish, Swedish, and UK (United Kingdom).

You can change the Char Font feature by pressing the A key until the desired option is displayed. The active Char Font set (G0 or G1) will become effective when exiting the Main menu.

Line Frequency

The Line Frequency selects between 50 Hz or 60 Hz. If you live in an area where the line frequency is 50 Hz, be sure to change this function.

You can change the Line Frequency by pressing the B key. The new Line Frequency will become effective immediately.

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Change Answer Back Message

The maximum number of characters allowed is 40. You can change the answer back message by pressing the C key. The bottom four lines will indicate a display similar to:

```
Presently, Message=
New message =

MISC                    (Press SETUP to Finish/left arrow to delete)
```

Type the desired message. The answer back message will be displayed as it is typed. The left arrow key (←) will delete the last character typed and display the graphics dot character.

Press the **SET UP** key when finished; then press the **SET UP** key again to return to the Main menu. The Change answer back message will become effective immediately.

One Pass Self Test

The Self test, one pass is a test performed on the video RAM, EEROM, ROM, keyboard and display character set.

- The terminal will display random blocks of reverse video while performing this test.
- If a failure is detected, a message is displayed.

You can select one pass self test by pressing the D key. One pass self test will become effective immediately. Press the **SET UP** key to return to Main menu.

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Continuous Self Test

Self test, continuous tests the video RAM, EEROM, ROM, and displayed character set continuously.

- The terminal will display random blocks of reverse video while performing this test.
- If a failure is detected, a message is displayed.

You can select continuous self test by pressing the E key. Continuous self test will become effective immediately. Press the right **SHIFT** and **RESET** keys to discontinue the test.

Restore

The Restore function changes all temporary functions to the functions stored in nonvolatile memory without resetting the terminal.

EXAMPLE: The current value of receive baud rate is 9600 and you have temporarily changed it to 4800. You can change to the current value by pressing the SET UP key and then simultaneously press the **CTRL** key and the **R** key. A beep will sound and Restore will become effective immediately. The receive baud rate is now 9600.

Save

The Save function stores a selected value of a function. The selected value stored then becomes the new current value.

To use the Save function, enter the Main menu, then press the **CTRL** key and the **S** key simultaneously.

- A beep will sound.

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- A message SAVING will appear on the display for a short time.
- The information you desire to save will be effective when the message SAVING disappears, a beep sounds, and the Main menu is displayed.

Programmable Keys

To change the Programmable keys, in the Main menu press the desired function key. The bottom four lines will indicate a display similar to:

```
A Function type STANDARD
```

or

```
A Function type  USER              key= <current key function>
B Change user function

PROGRAMMABLE KEYS    (Press SETUP to return to main menu)
```

Function Type

The terminal provides for two Function types, STANDARD and USER.

- When you select the STANDARD Function, the menu will not display a message of the selected key. The STANDARD Function is either the ANSI or Zenith mode of operation.
- When you select the USER Function, the menu will display the user programmed mnemonic or graphic symbols for control characters of the selected key.

You can change Function type by pressing the A key. The selected Function type will become effective when exiting the Main menu.

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Change User Function

Change user function changes the user current key function. A maximum of 40 characters can be used.

To change the user function, press the **B** key. The bottom four lines will indicate a display similar to:

```
Presently key = (Current key function)
New key =

PROGRAMMABLE KEYS   (Press SETUP to finish/left arrow key to delete)
```

Type in the desired command. The left arrow will delete the last character typed and print the dot graphics character. Press the **SET UP** key when finished, then press the **SET UP** key to return to Main menu. Change user function will become effective immediately.

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Chapter 3

Theory of Operation

Introduction

This section provides a brief explanation on the theory of operation. If a more detailed theory of operation is desired, refer to "Detailed Circuit Description," Chapter 4 of this manual.

Refer to the block diagram, Figure 3.1, while reading the following.

Theory of Operation

The keyboard communicates serially with the terminal via an Asynchronous Communication Interface Adapter (ACIA).

The Central Processing Unit (CPU) clock is divided down from the video clock to provide the necessary timing for the ACIA, Peripheral Interface Adapter (PIA), and the CPU.

The CPU controls all the terminal functions. The CPU's program is stored in Read Only Memory (ROM), Random Access Memory (RAM), and Electrically Erasable Read Only Memory (EEROM). EEROM can be altered by the keyboard to change the status (default value) of a function or mode of operation. The address decoder provides enable signals for all memories and peripheral devices.

The terminal communicates serially with the host computer and printer by use of a Dual Asynchronous Receiver/Transmitter (DUART). A 3.68 MHz crystal provides a frequency source for baud rate generation.

The terminal uses a Peripheral Interface Adapter (PIA). PIA 1 is used for internal control signals such as contrast.

A buffer is used to interface between the main data bus and video bus. This allows simultaneous operation of the CPU and video sections.

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The video controller provides the addresses and signal conditioning necessary to access video memory.

The video RAM provides two pages of 80-character or 1.24 pages of 132-character wide text and attributes.

The character generator ROM combines the character codes from the video RAM and scan line settings from the video controller to generate the character to be displayed.

The video clock consists of 19.76 MHz and 24.8 MHz oscillators. The 19.76 MHz oscillator provides a dot clock for the 80-character video display, and is divided down to provide a baud rate frequency reference for the ACIA. The 24.8 MHz oscillator provides a dot clock for the 132-character video display and is divided down to provide the CPU clock.

The video attribute controller modifies the attributes (characteristics) of text and graphics according to instructions received from the video RAM. The attributes are used to modify normal display characteristics such as: double-wide, blink, underline, background intensity, and foreground intensity.

The video level control generates an analog signal using digital information received from the video attribute controller. This circuit controls contrast.

The video deflection circuit receives the analog and synchronization signals from the video level controller and generates the necessary waveforms for CRT deflection and brightness.

The power supply converts the AC line voltage to the DC voltage levels necessary for terminal operation.

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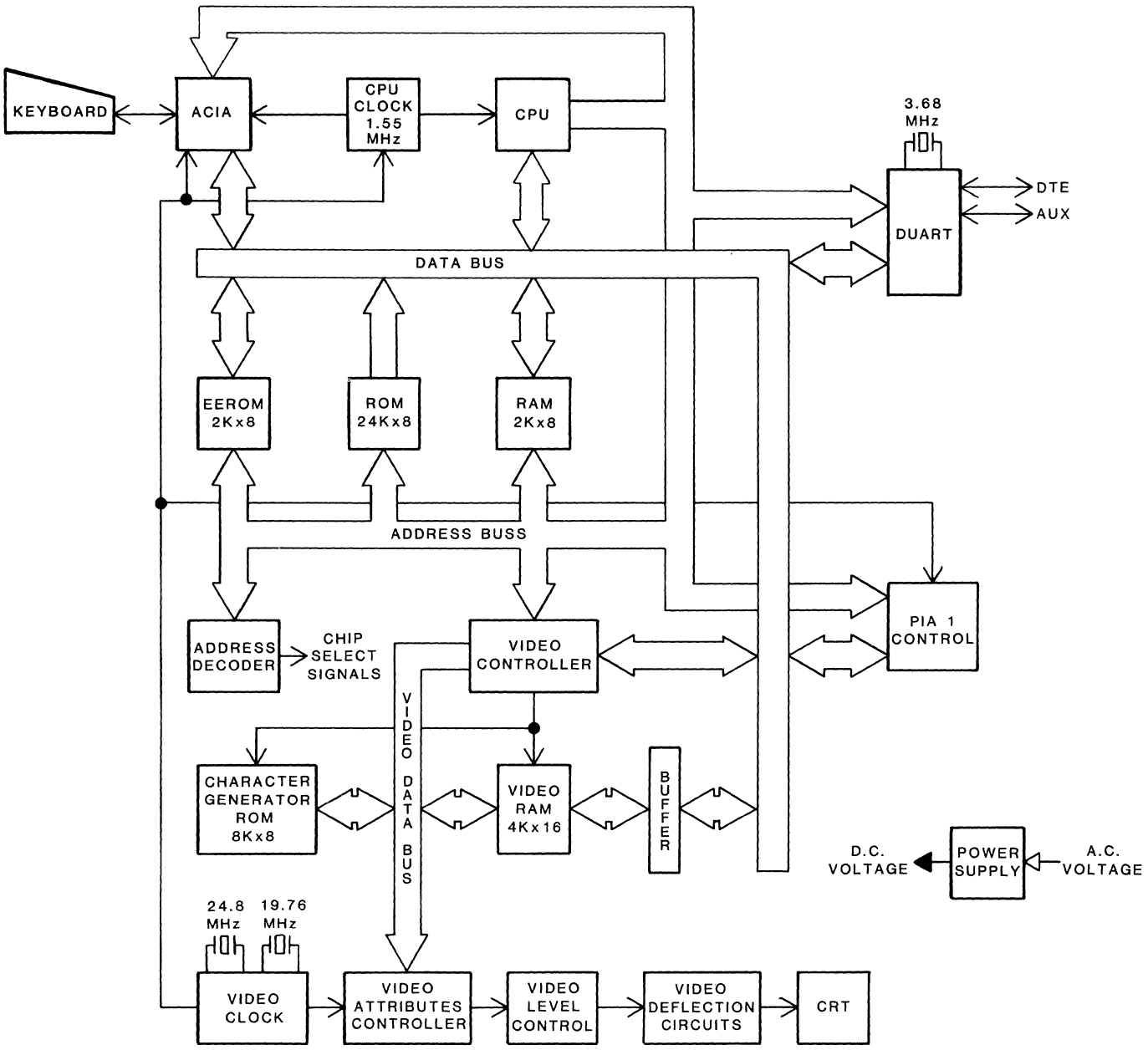

Figure 3.1. Block Diagram

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Chapter 4

Detailed Circuit Description

Introduction

This section provides a detailed circuit description of the keyboard assembly, terminal logic board, video circuit board, and power supply. Refer to the appropiate schematic diagram while you read the circuit descriptions.

Keyboard Assembly

Refer to the keyboard schematic as you read the following circuit description.

The keyboard is a strobe scanning keyboard, controlled by microprocesser U201 (refer to the data sheets on the 6805U2 in Chapter 9 for more information). U201 performs keyboard matrix scanning, setting and resetting of LEDs, actuation of the beeper, and serial communication with the terminal logic board.

All keys except SHIFT (L), SHIFT (R), RESET and ConTRoL are configured in a general matrix consisting of 12 scan lines and 8 sense lines. A keyswitch and diode are arranged at each crossover point. The diodes prevent the generation of phantom keys due to multiple closures.

Port bits PA0 (lsb) through PA3 (msb) of U201 control the scan lines. The port bits drive U203 (1 of 16 decoder) with the selected scan line being driven low. After setting a scan line, the sense lines are checked for a key closure.

Resistors R6 through R13 are used for pullups of the sense lines. The active-low sense lines are buffered by U202 to provide static immunity to the microprocesser which is an NMOS device. The sense lines are read by port bits PD0 through PD7.

The SHIFT (L), SHIFT (R), RESET, and ConTRoL keys are direct drive, active-low keys with pullup resistors R14, R15, R25, and R26. These keys all have special functions and may be used with other keys to send unique keycodes.

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Detailed Circuit Description

The SHIFT (L) and SHIFT (R) keys are ORed together and buffered by U207-11 into port bit PA6 of the microprocessor.

The SHIFT (R) and RESET keys are ANDed together by U206. the output of U206-3 is buffered by the network U206-11; R16 and C7 provide a minimum reset pulse width into RESET* resetting the microprocessor. The output of U206-3 is also buffered by U205-2, generating RES* to hardware reset the terminal. Capacitor C12 increases signal rise time.

The RESET key is also buffered by U207-3 into port bit PA4 of the microprocessor.

The ConTRoL key is buffered by U207-6 into port bit PA5.

The PI filter of C18, L6, and C19 provides the required filtering of the +5 VDC for the microprocessor U201.

U206-8 buffers the data stream input signal TXD (serial data sent to the keyboard) into port bit PA7. U206-3 buffers TXD and port bit PC into INT* for use as a start bit interrupt. R1 is the TXD line pullup resistor and C13 increases the signal rise time.

Port bit PC5 outputs the serial data generated by the keyboard (RXD) through buffer U205-4 to the terminal logic board. Capacitor C15 increases the rise time of the signal.

Port bit PC6 outputs the clear to send signal (CTS*), indicating that the keyboard is ready to receive another serial character, through buffer U205-6 to the terminal logic board. Capacitor C14 increases the signal rise time.

JP1 provides jumper selectability of either masked ROM or EPROM versions of U201. Production keyboards are jumpered for EPROMs.

JP2, JP3, and JP4 are read by port bits PC0, PC1, and PC2. These jumpers provide configuration information to U201 in order to select communication options.

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A 3.579 MHz crystal is connected between XTAL and EXTAL for the internal control and timing references of U201.

Port bit PB0 drives piezoelectric beeper BUZ, with U205-10 providing the current path. Diode D1 is used as a current shunt and R30 is the bias resistor.

Port bits PB1 through PB7 drive the LED indicators 1 through 7. Current drivers for the LEDs are U205-12 and U204. Resistors R17 through R23 are bias resistors. LED 8 (POWER ON) is driven from the 5-volt line with R24 as a bias resistor. LEDs 1 through 7 are turned on by U201 in response to commands from the terminal logic board. LED 8 is turned on by the application of power to the keyboard.

TIM is not used and is tied high through R5 to +5 VDC.

Power of approximately 8.5 VDC is applied to the keyboard through pin 1. A PI filter consisting of C16, L5, and C17 filters the input voltage and is used with diode D2 to provide 7.5 VDC to BUZ and the input to voltage regulator U208. U208 regulates the output to +5 VDC, with C2 used as a filter capacitor. The keyboard grounds are pins 7 and 8.

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Terminal Logic Board (TLB)

Refer to the terminal logic board (TLB) schematic as you read the following paragraphs.

The keyboard control and data signals are interfaced between the keyboard and UART (U140) by connector P105. The hardware reset signal (KRES*) is pulled up by R110 and filtered by L115 and C198 before being inputted to the hardware reset flip-flop (U152). The output data line (KTXD) to the keyboard is buffered by U150 pin 6 and filtered by L112 and C194. The input data line (KRXD) is pulled up by R128, filtered by L113 and C195, and buffered by U150 pin 8. The clear to send signal (KCTS) is pulled up by R127, filtered by L114 and C196, and buffered by U150 pin 11. The keyboard voltage of 8.5 VDC is reduced, regulated and filtered from 12 VDC by C185, U156, R129, R126, and C191.

UART (U140) transmits data to, and receives data from, the microprocessor (U119) via the data bus. Clock signals TXC and RXC generated from U147 control the baud rate of the UART. The reset (RS), interrupt (IRQ), and R/W* signals are generated directly from the microprocessor. The E signal is the peripheral clock generated by U151. The chip select signal KUART* is generated by PAL U109 (refer to the PAL equation located in Chapter 8).

Power supply voltages are supplied to the terminal logic board via connector P104. The voltages supplied are 12 VDC 1 amp, 12 VDC 2 amp, 5 VDC, and −12 VDC. The 5 VDC input is filtered by pi filter C187, L111, C188, and C186. Capacitor C186 is a filter for the −12 VDC. The TLB supplies the voltages to the keyboard and video circuit board.

The DTE signals (refer to Table 4.1) are interfaced between the output connectors and a DUART (U122) by connector P101. These input and output signals are buffered by U153, U123, U126, U141, and U128. Resistors R108 and R107 are pull up resistors. Pi filter C136, L106, and C137 provide the necessary filtering for U122. The chip enable signal DUART* is generated by PAL U109 (refer to the PAL equation located in Chapter 8). Input and output of data is via data lines D0-D7. Address lines A0-A3 select the address register to be read or programmed by the microproces-

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sor. The RD* signal is generated directly by the microprocessor, while the WR* signal is generated by U132. The DUART is reset by U135. Crystal Y100 is a 3.686 MHz series resonant crystal which provides a baud rate frequency reference for the host (primary) and auxiliary (printer) serial ports.

Table 4.1. DTE Signal Names

SIGNAL NAME	INPUT/OUTPUT I/O	SIGNAL FUNCTION
TXD	O	Transmitted Data
RXD	I	Received Data
RTS	O	Request to Send
CTS	I	Clear to Send
DSR	I	Data Set Ready
CD	I	Carrier Detect
SS	O	Speed Select
SI	I	Speed Indicator
DTR	O	Data Terminal Ready
RI	I	Ring Indicator

The microprocessor (U119) is an 8-bit 68B09E. This microprocessor controls the data/address bus, bus status, bus timing/control, and power/clock. For a more detailed description, refer to Chapter 9. Figure 4.1 depicts the memory map of the microprocessor.

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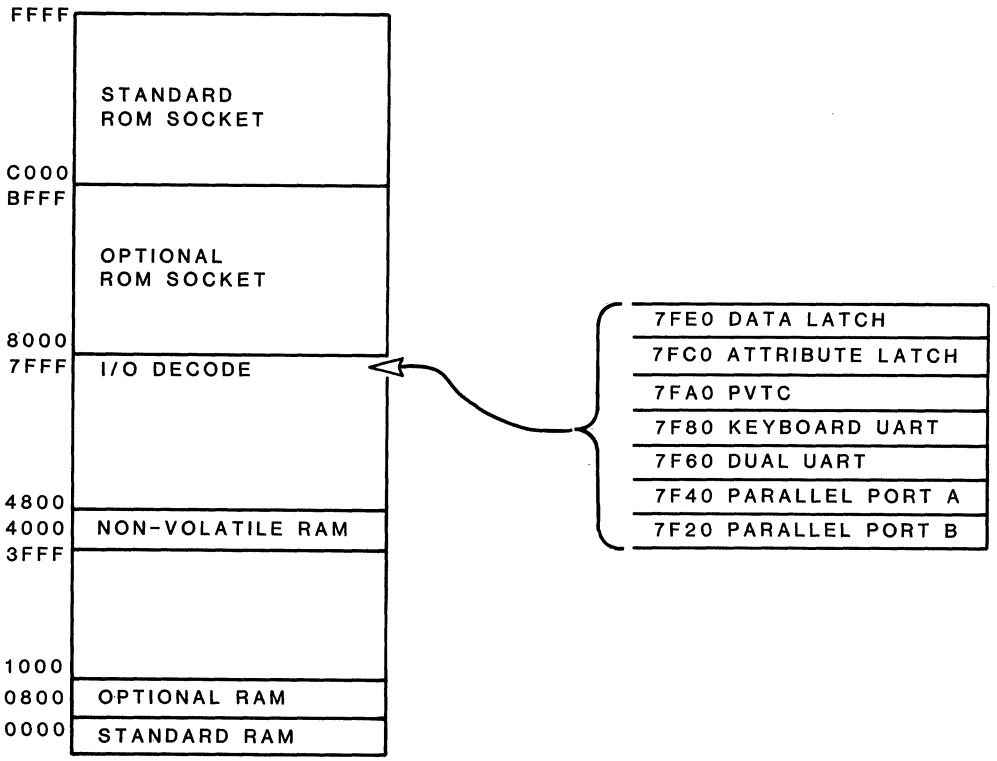

Figure 4.1. Z-49 Memory Map

U109 is a PAL that generates chip enable and select signals when addressed by the microprocessor (U119) and enabled by ADDVAL* generated by U151. Refer to the PAL equation in Chapter 8.

The power-up diagnostic routines are contained in the ROMs U104 and U105. The ROMs are selected by address lines A14 and A15, and ADDVAL* true during a read cycle by decoder U127.

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Crystal Y102 is a 24.8064 MHz oscillator. The output is buffered by U134 and when selected by CLKSEL not true, provides the dot clock reference for 132-character generation via U139. The frequency is divided by four by U136 and inputted to U151. The processor clock (PE) and associated clocks and timing signals are generated by U151 in combination with U135, U150, U149, and U146. The other clock and timing signals generated are: Quadurature (Q) clock, Peripheral (E) clock, an address valid signal (ADDVAL*), an EEPROM access timing phase signal (EEW*), and a gating signal for the RAM write strobe (PQ*).

Crystal Y101 is a 19.7676 MHz oscillator with the output buffered by U134. The output of U134 when CLKSEL is true provides the dot clock reference for 80-character generation via U139. U147 divides the frequency by 64 to provide the baud rate for the UART (U140).

The menus for the terminal are located in EEPROM (U103). The chip select signal E2* is generated by PAL U109 (refer to the PAL equation located in Chapter 8). The R/W* signal and EEW* timing signal are ANDed by U132, allowing the changing of the default values when W* is true. The R/W* is inverted by U135 to provide the output enable for a read cycle.

The RAMs (U111 and U112) are selected by the chip select signals RAM 1 or RAM 2, generated by PAL U109 (refer to the PAL equation located in Chapter 8). The PQ clock and the R/W* signal are ANDed by U132, determining whether the selected RAM is written to or read from. Switch SW 101 (refer to schematic for switch settings) provides the capability to change the 2KB $\times$ 8 RAMs to 8KB $\times$ 8 RAMs.

NOTE: 8KB $\times$ 8 RAMs require a different PAL (U109).

The PIA (U100) generates the board control signals which determine brightness (BRI), keyboard reset (KRES*), dot geometry (DOTS), dot clock source (CLKSEL), and screen luminance reset (VID BLANK). The PIA is selected by the chip select signal PORT A, generated by PAL U109 (refer to the PAL equation located in Chapter 8), and clocked by E clock. The output is determined by the R/W* signal. When U100 is interrupted or reset, all outputs go high.

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Detailed Circuit Description

The programmable video timing controller (U120) generates video display addresses, timing controls, and video driver board input vertical synchronization (V SYNC) and horizontal synchronization (H SYNC) signals. U120 is selected by the chip enable signal PVTC* generated by PAL U109 (refer to the PAL equation located in Chapter 8) and addressed by bits A0 through A3. U124 latches the line attributes double wide (DW) and line graphics (LG) when clocked by BLANK* generated by U120 and inverted by U135. U118 and U126 are the video RAM address latches enabled by CCLK via U145.

The CCLK and CTRL1 signals are NANDed together by U149 clocking U148 which generates the write signal (W*) to the video RAM and initiates the write sequence. The next CCLK cycle generates the PEW* signal which enables data latches U142 and U130, and is inverted by U135 to clock U133 providing an ENDW* signal. ENDW* and PEW* are ANDed together by U145 to provide a reset for the write cycle. The OE* signal generated from U145 provides a time delay of one-half of the character clock during the read cycle to prevent buffer clash between RAM banks. CCLK and LRDB* are ANDed by U145 to provide a read latch clock (RLC*) for latches U143 and U129.

Latches U143, U142, U130, and U129 allow the microprocessor and video controller to operate independently. The outputs of U131 determine which latch will be enabled or clocked. U129 and U143 read the data to the microprocessor; U130 and U142 write the data from the microprocessor onto the video data bus.

The video RAM (U107, U108, U116, and U117) contains character code and attribute information. Video address VA13 in conjunction with inverter U135 determine which bank of RAM is selected. Switch SW100 (refer to schematic for switch settings) provides the capability to increase RAM size from 2KB $\times$ 8 to 8KB $\times$ 8. The character and attribute data are passed through pipeline latches U125 and U106. The character code data is routed to the character generator ROM (U110) and the attribute data is routed to the video attribute controller (U115).

The terminal reset is generated by flip-flop U152. U152 pin 12 generates a 100 μs low pulse from the keyboard reset signal KRES*. U152 pin 4 generates a 30 ms hardware reset low pulse. Both signals are NORed by U137, outputting RESET* and inverted by U135, outputting RESET.

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Data from U120 is inputted to U121 to generate the line count for the character generator ROM (U110). U121 is selected by LACE* from U100 and clocked by BLANK from U120. The character data is passed through the pipeline latch U134 to the video attributes controller U115. U134 is enabled via U132 when LG (line graphics) is not true and SSBEN* generated by U133 is true.

The video attributes controller (U115) modifies the display characteristics of the ROM characters received according to the attributes received from the video RAM. These attributes are:

- AT0 — Low order foreground intensity.
- AT1 — High order foreground intensity.
- AT2 — Low order background intensity.
- AT3 — High order background intensity.
- AT4 — Underline.
- AT5 — Blink.
- AT6 — Double wide character.
- AT7 — Highest order address bit.

U138 is a pipeline latch which passes information to U139. U139 provides the necessary synchronization for blank, cursor, blink and underline attributes. U149, U144, and U137 gate the double wide attribute to the video attribute controller. U144 and U137 provide for the implementation of dot stretching.

The video data from U115 (output 1 and output 2) is passed through a digital to analog network consisting of U144, U155, and R120 through R123, developing character and intensity levels to the base of Q101. The output of Q101 (an emitter follower) is combined with the digital to analog contrast network consisting of U154 and R114 through R119 at the base of Q102. The video output of Q102 is filtered and sent with the other required signals to the video board via P102.

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Video Circuit Board

Refer to the video circuit board schematic as you read the following paragraphs.

The video circuit board converts TTL signals, coming from the terminal logic board, to the voltages necessary to drive the CRT. This circuit board contains the vertical circuits, horizontal circuits, video amplifier, and high voltage power supply.

Vertical Circuits

Capacitor C301 couples the vertical sync signal (from the TLB) to synchronize vertical oscillator transistors Q301 and Q302. Capacitor C303 shapes the 60 Hz output at the emitter of Q301 to help produce a linear sweep.

The shaped 60 Hz oscillator signal is applied to differential amplifier Q303, where the base is the inverting input and the emitter the noninverting input. Feedback from the collector is provided by R319 to the emitter, providing good linearity.

The output of Q303 drives Q304 (vertical driver), which in turn drives the complementary vertical amplifier Q306 and Q307. This stage develops the sweep current through the deflection yoke TX202A. Diodes CR302 and CR303 prevent crossover distortion. RC network R312, R313, R314, R316, R317, C307, C308, and C309 set the gain and frequency of the vertical amplifier.

Q308 generates a fast vertical retrace of 850 μs maximum when measured from the leading edge of the vertical sync pulse.

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Video Amplifier

Transistors Q401 and Q402 are connected in cascode to form the video amplifier. This circuit has high gain, low noise, and low input and output capacitance.

The positive video signal from the TLB is applied to the base of Q402. Transistors Q401 and Q402 conduct, driving the CRT cathode more negative. Resistor R412 determines the overall stage gain, while C403 and R413 determine the frequency response.

Horizontal Circuits

Capacitor C101 couples the positive horizontal sync pulse from the TLB to the base of Q101. Resistor R102 and capacitor C102 are an input impedance network. CR101 is a blocking diode allowing only the positive signal through. Transistor Q104 is normally conducting, biasing Q101 off. The horizontal sync pulse turns Q101 on, cutting off Q104 at a point on the slope of the pulse determined by the phase shift network R103, R104, and C103.

When Q104 cuts off, Q101 is cut off, turning Q104 on. This action produces an amplified sync pulse across capacitor C106 and blocking diode CR103 to the horizontal oscillator consisting of Q106 and Q107. The horizontal oscillator outputs an 18.6 KHz horizontal frequency to preamp Q108. Diodes CR113 and CR114, resistors R113, R114, R116, and R117 are discharge diodes and resistors. The output of Q108 drives the horizontal driver Q102. Resistor R127 and capacitor C114 form a wave shaping network. Transformer TX101 couples the signal from the horizontal driver to the horizontal output transistor Q103. Resistor R128 prevents transformer ringing.

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Horizontal Scan and Power Supplies

Transistor Q103 is used as an electronic switch which is on for approximately 60 to 70 percent of the horizontal scan period. Capacitor CX117 acts as a pseudo B+ for the horizontal deflection yoke TX202B. When Q103 is on, current flows out of CX117, through TX202B, LX102, LX101, and Q103 to ground. This action produces the right side of the scan. LX102 is a magnetically biased saturable reactor which provides left to right linearity. LX101 sets the horizontal scan width. The value of CX117 determines the parabolic waveform on the pseudo B+ which controls center to edge linearity. The network RX129, CR112, R131, and C118 provide suppression of spurious ringing which would cause black vertical lines at the left side of the raster.

When Q103 turns off, the resonant circuit of CX116 and LX101, LX102, and TX202B rings for one-half of a sine wave for a period of time equal to the LC time constant of the resonant circuit CX116 and LX101. This is the retrace pulse which moves the scanning beam from left to right side of the CRT and also provides a high amplitude pulse for use in developing the auxiliary power supplies. TX102 steps up the pulse to develop 12KV of high voltage. TX102 also inverts and steps down the pulse. The inverted pulse is rectified by CR111 to provide the video B+, clamped by C119 and CR107 to provide a negative voltage supply for the CRT, and rectified by CR106 to provide grid 2 bias for the CRT.

At the end of the retrace the sine wave goes negative, biasing the damper diode CR104 on. Current flowing through the yoke circuit into the damper diode provides the left side of the raster scan. The above cycle is then repeated.

The 12 volts for the horizontal scan is fed through diode CR109 into a tap on TX102 where transformer action increases the voltage to 20.5 for the pseudo B+ necessary for the horizontal deflection. Resistor R501 improves the high voltage regulation by lowering the supply's source impedance.

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The voltage parabola on CX117 is coupled through C134, and amplified and inverted by Q109. The output of Q109 is coupled through C136 to the focus grid of the CRT to provide dynamic focus across the screen. The dynamic focus circuit provides a sharper focus at the edges of the screen.

The positive pulse from Q103 saturates the flyback transformer TX102 and charges CX117 through width coil LX101, linearity coil LX102, and horizontal deflection yoke TX202B. When Q103 turns off, the magnetic field of TX102 collapses, generating the acceleration voltage to the CRT through an internal rectifier diode. Diode CR106 rectifies the focus voltage, charging C129 to a static level. Diode CR107 is the charge path for C126, which develops the brightness voltage; CR107 also provides the conduction path for Q109. C119 couples the positive pulse from Q103, causing CR107 to conduct cutting of Q109. CR104 and CX116 form a damper network to eliminate the ringing effect of flyback transformer TX102.

The width coil LX101 and linearity coil LX102 modify the sawtooth waveform generated by TX102 to provide a linear horizontal picture. Resistors RX129, R131, diode CR112 and capacitor C118 form an arc suppression network. Diode CR109 and capacitor C123 rectify and filter the 20.5 VDC from the primary of TX102. Diode CR111, C122, and R132 rectify and filter the 60 VDC from the secondary of TX102. Q109 is a dynamic focus correction circuit. This circuit provides a sharper focus on the outer edges of the horizontal scan. A higher voltage is applied to the focus grid synchronized by the output pulse coupled across C119 and the charging and discharging of CX117. R501 is a bleeder resistor used to discharge the high voltage to ground when the display is switched off.

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Power Supply

WARNING: The power supply contains lethal DC voltages. The line cord must be unplugged before removal or installation.

Due to the proprietary nature of the power supply, only a functional description is provided. No schematic or parts list is contained in this manual.

The power supply is an off line, voltage fed, half-wave bridge, switch mode power supply capable of 115 VAC or 230 VAC operation. The input voltage selection is internally jumper selectable.

The input voltage is filtered and converted to regulated and quasi-regulated output voltages. The regulated output voltages are +5 VDC, +12VDC, and +15VDC. The quasi-regulated voltages are +12 VDC and −12 VDC. This power supply contains overcurrent and overvoltage protection circuitry. Refer to Chapter 6, "Service Instructions," for the required load and pin number locations.

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Chapter 5

Disassembly

Introduction

The following information is provided to assist you in the removal of the back cover, cabinet top, power supply, terminal logic circuit board (TLB), video drive board, and cathode ray tube (CRT) for servicing.

WARNING: Be sure the line cord is disconnected from the terminal before continuing.

Figure 5.2 has the major units labeled which are referenced in the disassembly procedures. All components are numbered and may be identified in the "Parts List," Chapter 8.

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Cabinet Top

Refer to Figure 5.1 as you perform the following steps.

CAUTION: Be sure all interconnecting cables are disconnected from the back of the video display.

1. Position the video display as shown. Remove the two 6-32 × .875″ screws from the top side of the rear panel.

2. Remove the two 4-40 × .375″ screws from the bottom of the rear panel.

3. Carefully lower and lift the rear panel off the rear of the video display.

4. Lift the cabinet top up and off the video display.

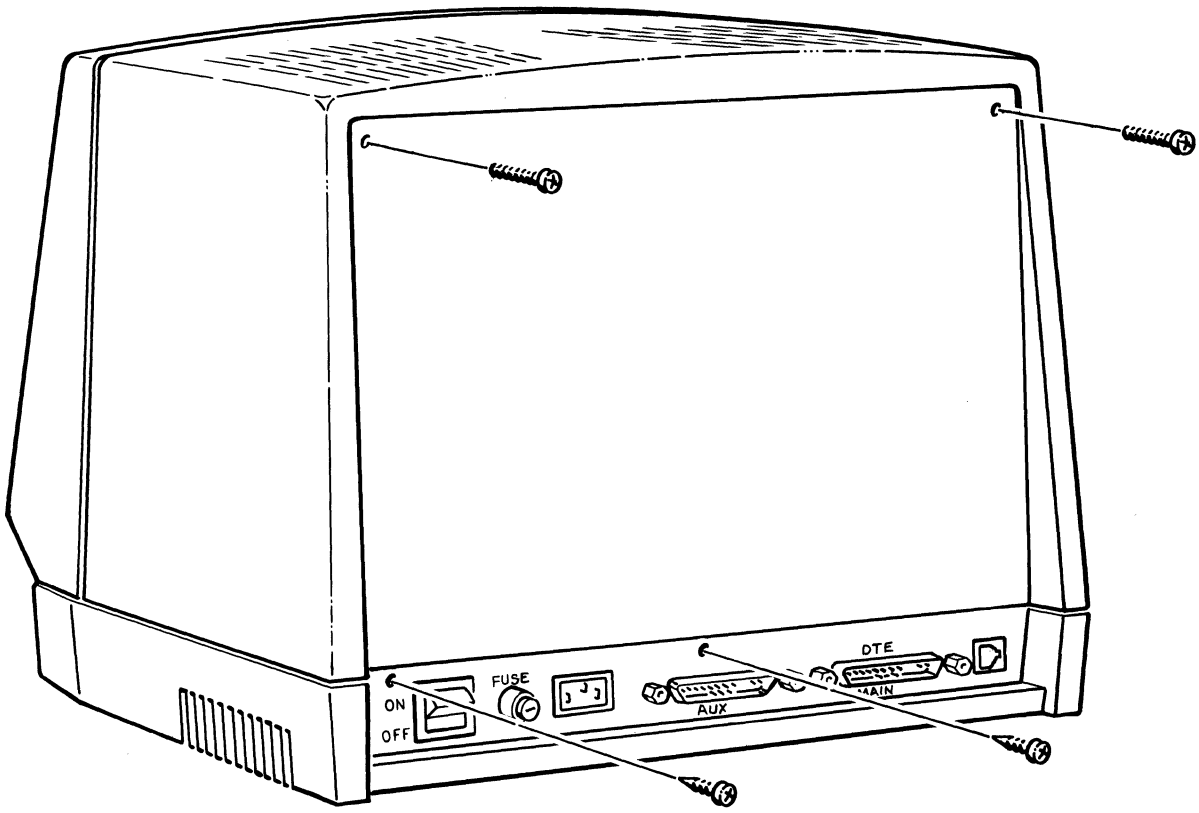

Figure 5.1. Cabinet Disassembly

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Terminal Logic Board (110)

To remove the terminal logic board for servicing, refer to Figure 5.2, the foldout at the end of this chapter, while performing the following steps.

CAUTION: Be sure all interconnecting cables are disconnected from the back of the video display.

1. Remove the back cover (265) as previously described.

2. Remove the cabinet cover (260) as previously described.

3. Cut the cable tie (280) securing the video circuit board ferrite bead to the top RFI shield (255).

NOTE: Note the location of the tie wrap on the top RFI shield.

4. Remove two screws (103), two screws (105) securing the top RFI shield (255) and the RFI shield.

5. Remove two 8-BT × .625″ self tapping screws (15) securing the lower left RFI guard (25) to the cabinet front (5).

6. Remove two 6-32 × .375″ screws (40) securing the side panel (100) to the chassis (170).

7. Carefully remove the side panel (100) with the terminal logic board and unplug plugs P101 (125), P102 (150), and P105 (75).

8. Remove the six 6-32 × .375″ screws (40) securing the terminal logic board to the side panel (100).

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Video Circuit Board (120)

To remove the video circuit board for servicing, refer to Figure 5.2 while performing the following steps.

CAUTION: Be sure all interconnecting cables are disconnected from the back of the video display.

1. Remove the back cover (265) as previously described.

2. Remove the cabinet cover (260) as previously described.

3. Cut the cable tie (280) securing the video circuit board ferrite bead to the top RFI shield (255).

NOTE: Note the location of the tie wrap on the top RFI shield.

4. Remove two screws (103), two screws (105) and the top RFI shield (255).

WARNING: High Voltage.

5. Refer to the inset drawing #1 on Figure 5.2 and discharge the CRT as shown.

6. Refer to the inset drawing #2 on Figure 5.2 and disconnect the anode lead from the CRT.

7. Carefully unplug the CRT socket from the neck of the CRT. Then disconnect the black ground wire from the CRT ground clip (85) at the upper right-hand corner.

8. Unplug the red/blue two-wire cable from VERT YOKE and the yellow/black two wire cable from HORIZ YOKE on the video drive board (120).

9. Loosen the two 6-32 × .375" screws (40) securing the lower right RFI guard (25) to the right side panel (115).

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10. Remove two 6-32 × .375″ screws (40) securing the side panel (115) to the chassis (170).

11. Carefully remove the side panel (115) with the video drive board and unplug the ten-pin plug (125).

12. Remove the four screws (132) securing the video display board to the side panel (115).

Power Supply (135)

WARNING: This power supply contains lethal DC voltages. The line cord must be disconnected before you remove the power supply.

To remove the power supply for servicing, refer to Figure 5.2 while performing the following steps.

CAUTION: Be sure all interconnecting cables are disconnected from the back of the video display.

1. Remove the back cover (265) as previously described.

2. Remove the cabinet cover (260) as previously described.

3. Remove the terminal logic board (110) as previously described.

4. Remove the video circuit board (120) as previously described.

5. Remove the two 6-32 × .375″ screws (40) securing the power supply cover (140) and solder lug (165) to the power supply.

6. Carefully remove the power supply cover (140), and unplug connectors P1 and P2 (150).

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7. Remove the four 6-32 × .375″ screws (40) securing the power supply chassis (155) to the main chassis (170).

8. Carefully remove the power supply chassis (155) from the terminal.

9. Remove the two 6-32 × .375″ screws (105) on the power supply chassis (155) bottom and the power supply.

Cathode Ray Tube (60)

To remove the CRT for servicing, refer to Figure 5.2 while performing the following steps.

CAUTION: Be sure all interconnecting cables are disconnected from the back of the video display.

1. Remove the back cover (265) as previously described.

2. Remove the cabinet cover (260) as previously described.

3. Remove power supply (135) as previously described.

4. Remove the terminal logic board (110) as previously described.

WARNING: High Voltage.

5. Refer to the inset drawing #1 on Figure 5.2 and discharge the CRT as shown.

6. Refer to the inset drawing #2 on Figure 5.2 and disconnect the anode lead from the CRT.

7. Remove the video display board (120) as previously described.

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8. Carefully place the cabinet front face (5) down on a smooth flat surface.

9. Remove one 8-32 × .375 screw (75), two #8 flat metal washers (80), and the CRT ground clip (85) from the upper right CRT bracket (55).

10. Remove three 8-32 × .375 screws (75), three insulated outside washers (65), and three insulated inside washers (70).

NOTE: Note the difference between the inside and outside insulated washers.

11. Carefully remove the CRT.

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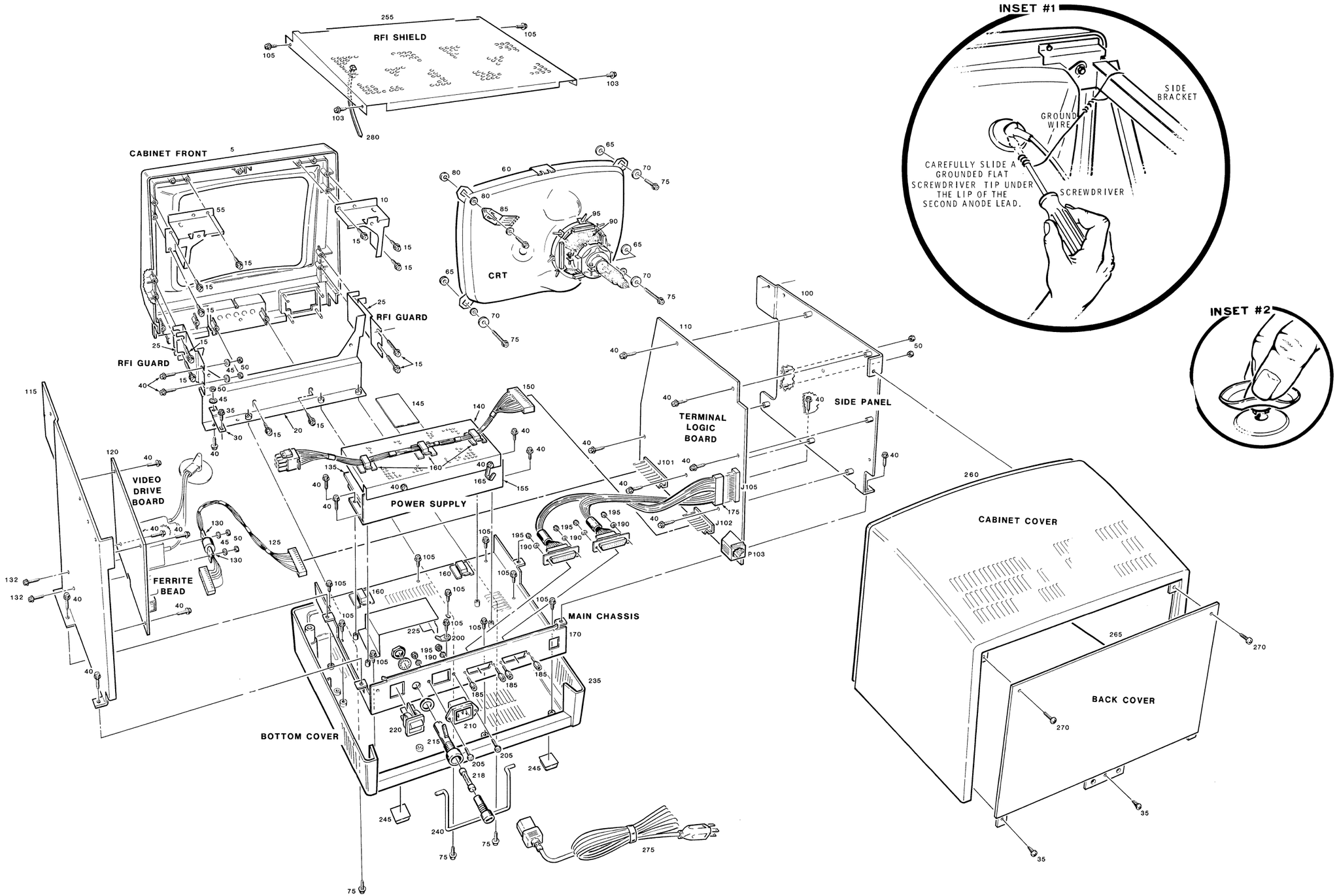

Figure 5.2. Disassembly

Chapter 6

Service Instructions

Introduction

This chapter provides servicing and troubleshooting information. Included are safety servicing guidelines, cleaning, adjustments, inspection, testing and troubleshooting. To aid in troubleshooting, Appendix B (escape sequences) is included in this manual.

Safety Servicing Guidelines

Warnings

The terminal contains an on-line DC switching mode power supply. This power supply contains lethal voltages. The line cord must be disconnected before servicing is attempted.

Do not work on any exposed chassis if you are not familiar with Zenith servicing procedures and precautions, or personal injury may result.

Do not attempt to modify any circuit, or injury to the user may result.

Always connect the terminal to an isolation transformer, or shock and/or injury may result.

Discharge the high voltage anode lead of the picture tube using a jumper lead connected between the chassis and a screwdriver, or personal shock and/or injury may result.

Be sure that a terminal with excessive high voltage is not operated longer than necessary, or x-radiation may result.

NOTE: Excessive high voltage produces x-rays from the picture tube.

Carefully handle and install the picture tube, or implosion injury may result.

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Service Instructions

To prevent electrical shock after reassembly, perform an AC leakage test on all exposed metal parts of the cabinet and screws. **DO NOT** use an isolation transformer during this test.

Refer to Figure 6.1 while reading the following.

- Use an AC voltmeter that has sensitivity of 5000 ohms per volt or greater.
- Connect a 1500-ohm, 10-watt resistor in parallel with a 0.15 μF 150 VAC capacitor.
- Connect the parallel network to a known good earth ground and the exposed metal parts, one at a time.
- Measure the AC voltage across the parallel combination, then reverse the AC plug and repeat the measurements.
- Any voltage reading exceeding 0.75 volts RMS (0.5 milliamps) constitutes a potential shock hazard and must be corrected immediately.

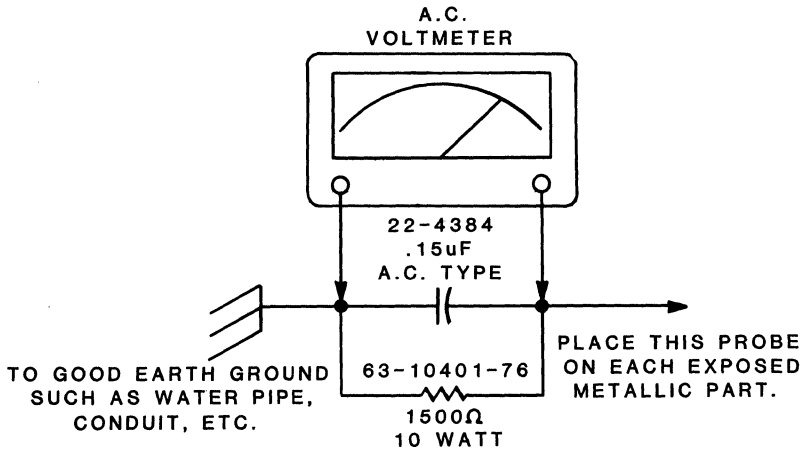

Figure 6.1. AC Leakage Test

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Cautions

Integrated circuits (ICs) are electrostatic sensitive devices (ESD). These devices can be damaged by static electricity. When removing an IC from its protective foam packing, do not lay the IC down or let go of it until after the IC is installed. When bending the leads, use a wrist grounding strap or hold the IC in one hand and touch your other hand to the work surface to equalize static electricity.

Be sure that all components are positioned in such a manner as to avoid the possibility of component shorts, or equipment damage may result.

Inspect soldering for cold solder joints, frayed leads, damaged insulation, solder splashes and sharp solder points, or faulty equipment operation may result.

Never release a repair unless all protective devices and other hardware have been installed, or faulty equipment operation may result.

Remove all loose foreign material, or equipment damage may result.

Follow original layout, lead length, lead dress and lead tension, or faulty equipment operation may result.

No lead or component should touch a resistor whose rating exceeds one (1) watt, or equipment damage may result.

Replace all components with exact Zenith replacement types, or equipment damage and/or faulty operation may result.

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Cleaning Procedures

Use the following suggestions to keep the terminal equipment clean.

WARNING: Be sure power is OFF.

- Clean the cabinet and keyboard with a clean lint-free cloth slightly dampened with a nondetergent cleaning solution.
- **DO NOT** use spray liquids or a soaking wet cloth.
- Dry the cabinet, keyboard, and screen with a clean lint-free cloth.
- Clean the screen of the terminal with a commercial nonabrasive window cleaner.
- Be sure the terminal is thoroughly dry before applying power.

Adjustments

Before you begin troubleshooting, make sure all adjustments are correct. Much time and effort has been spent on troubleshooting procedures when a mere adjustment is all that is needed to rectify the problem.

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Refer to Figure 6.2 while reading the following.

Horizontal Phase Control (PHASE)

Adjust the horizontal phase control (R103) to bring the video information into the center of the screen.

Brightness Control (BRITE)

Adjust the brightness control (R139) to cut off the screen.

Vertical Size Control (VERT)

Adjust vertical size control (R312) as required to provide normal picture height (6 inches).

Horizontal Width Control (WIDTH)

Adjust horizontal width control (LX101) as required to provide normal picture width (8.5 inches).

Focus Control (FOCUS)

Adjust the focus control (R148) until the video has maximum clarity of detail.

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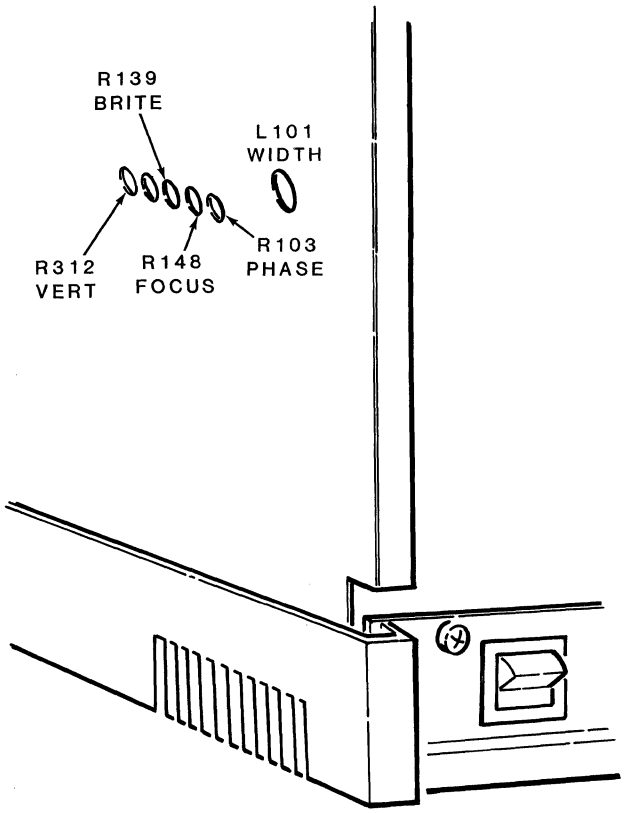

Figure 6.2. Service Adjustments

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Yoke Adjustments

Refer to Figure 6.2 while reading the following.

- Remove any foam magnets that may be present on the yoke.
- Loosen the clamp screw and rotate the deflection yoke until the display edges are vertical and horizontal, then tighten the clamp screw.
- Adjust the centering rings to the position that best centers the display.
- Select the least straight of the four displayed edges and install a foam magnet on the yoke post that is nearest the greatest bow. Rotate the magnet slowly until the display is as straight as possible.
- Repeat the foam magnet procedure as necessary around the yoke until a uniform rectangular shape is displayed.

NOTE: If only a small foam magnet effect is desired, reduce the size of the foam magnets by cutting them with a pair of diagonal cutters.

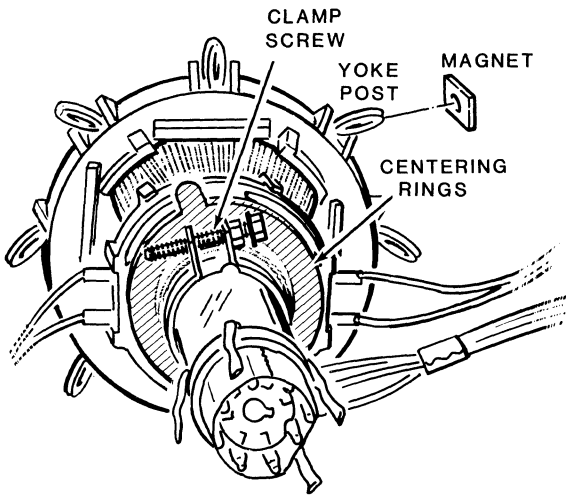

Figure 6.3. Yoke Adjustment

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Inspection

The following inspections will assist you in determining possible failures.

- Unplug the line cord and check for broken insulation, burn marks, and loose plug prongs.
- Test the wall outlet for the appropriate voltage.
- Check the terminal fuse (refer to Figure 1.1).
- Check connectors for proper electrical connections.
- Check all boards for broken, burnt, or arced-over components.
- Check all boards for heat darkened areas.

Testing and Troubleshooting

The testing and troubleshooting contained in this chapter consists of general troubleshooting, power supply, terminal logic board, video driver board, and keyboard.

General Troubleshooting

Refer to Table 6.1 for general troubleshooting.

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Table 6.1. General Troubleshooting

PROBLEM	POSSIBLE CAUSE	REMEDY
Nothing happens at turn on, and POWER ON indicator in the keyboard is not lit.	1. Line cord is not plugged in. 2. Power not on at wall plug. 3. Power switch is not ON. 4. Fuse is missing or blown. 5. Keyboard is not connected. 6. Power supply.	Plug in line cord. Use different receptacle. Press power switch to ON. Replace fuse (page 1.3). Connect keyboard (page 1.3). Replace power supply (page 5.5).
POWER ON indicator is not lit, but cursor is on screen. Screen displays `Keyboard error`	Keyboard cable not plugged into terminal.	Plug in keyboard cable.
POWER ON indicator is lit. No video.	1. Contrast turned down or Screen saver option on. 2. Terminal logic board. 3. Video driver board. 4. TLB to video driver cable not connected.	Refer to page 2.7 and page 2.19. Replace TLB. Replace video driver board. Connect TLB to video driver.
Insufficient brightness.	1. Contrast turned down. 2. Video driver board. 3. TLB video output circuit.	Refer to page 2.7. Replace video driver board. Replace TLB.
Terminal inadvertently resets to power on.	Loose line cord or keyboard cable wire broken.	Replace keyboard cable.
Display does not respond to the keyboard.	1. On line (under host computer control). 2. Keyboard locked. 3. Keyboard cable not connected.	Refer to page 2.9. Refer to pages 2.22 and 2.23. Connect keyboard cable.
Strange or wrong characters appear on the screen.	1. Wrong terminal mode. 2. Wrong communications mode (baud rate, parity, duplex). 3. Wrong character font. 4. Terminal in Monitor mode.	Refer to page 2.25. Refer to page 2.9. Refer to page 2.26. Refer to page 2.25.

Table 6.1 (continued). General Troubleshooting

PROBLEM	POSSIBLE CAUSE	REMEDY
NOTE: In order to communicate effectively with a host computer directly or via a modem, the baud rate, parity, and duplex characteristics must agree. Zenith software utilizes full duplex and does not check parity.		
Screen display wavers.	Terminal in the wrong line frequency option.	Refer to page 2.26.
Error message received during diagnostic test.	Terminal logic board.	Replace TLB.
Double-spaced lines.	AUTO LF on CR or AUTO CR on LF configured incorrectly.	Refer to pages 2.18 and 2.19.
No responses to ESC sequences.	1. Terminal mode incorrect. 2. Terminal in monitor operation.	Refer to page 2.25. Refer to page 2.25.

Power Supply Troubleshooting

WARNING: This power supply contains lethal voltages. The line cord must be unplugged before proceeding with the following steps.

NOTE: This power supply is not serviceable.

To test the power supply, refer to Figure 6.4 while reading the following.

WARNING: DO NOT touch the load resistors after power is applied. The resistors will become hot and may cause burns.

- Connect a 120 Ω dummy load resistor rated at 2 watts between pin 1 and pin 5 of the power supply connector.
- Connect a 6 Ω dummy load resistor rated at 5 watts or above between pin 2 and pin 3 of the power supply connector.

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- Connect a 6 Ω dummy load resistor rated at 25 watts between pin 2 and pin 4 of the power supply connector.
- Connect a 120 Ω dummy load resistor rated at 2 watts between pin 7 and pin 10 of the power supply connector.
- Connect a 6 Ω dummy load resistor rated at 5 watts or above between pin 8 and pin 9 of the power supply connector.
- Apply power and check the voltages at their respective pins.

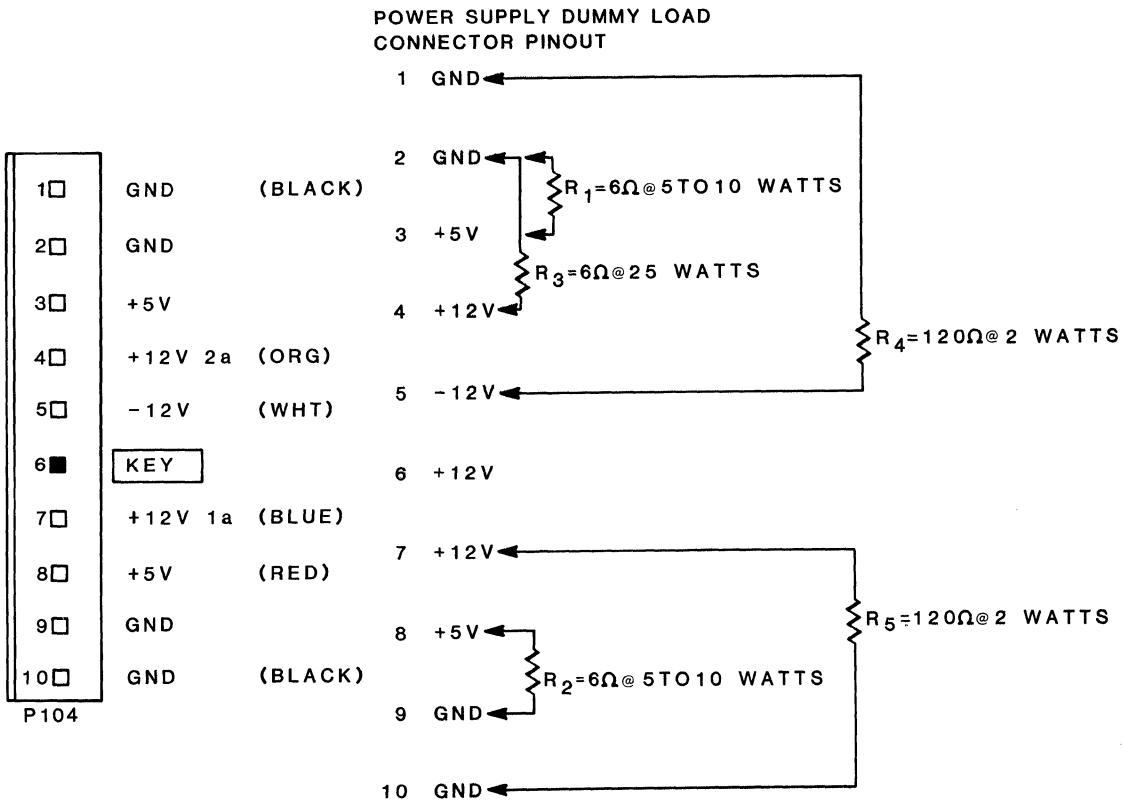

Figure 6.4. Power Supply Testing

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Terminal Logic Board Troubleshooting

Refer to Table 6.2 for terminal logic board troubleshooting when error messages appear.

Table 6.2. Terminal Logic Board Troubleshooting

ERROR MESSAGE	POSSIBLE CAUSE
ROM Checksum	U104, U105, U127, U136, U151
RAM Fault (Power up test)	U109, U111, U112, U132, U135, SW101
(One pass or continous test)	U107, U108, U116, U117, U118, U120, U121, U124, U125, U126, U129, U130, U131, U133, U135, U142, U143, U145, U148, U149, SW101
CRTC Error	U109, U115, U120, U132, U134, U139, U146, Y102, Y103
Keyboard	U109, U134, U140, U146, U147, U150, U151, Y103
NVRAM Checksum	U103, U109, U132, U135
CPUFIRQ Error	U109, U115, U119, U120, U132, U134, U139, U146, Y102, Y103
DUART Error	U109, U122, U123, U128, U132, U141, U153, Y100

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Terminal Logic Board Waveforms

The following waveforms were taken with the terminal off line and the screen filled with E's. The menu setups are supplied with the waveforms. Refer to Figure 6.5 for the video interconnect pinout. Refer to Figures 6.6 through 6.9 for waveforms.

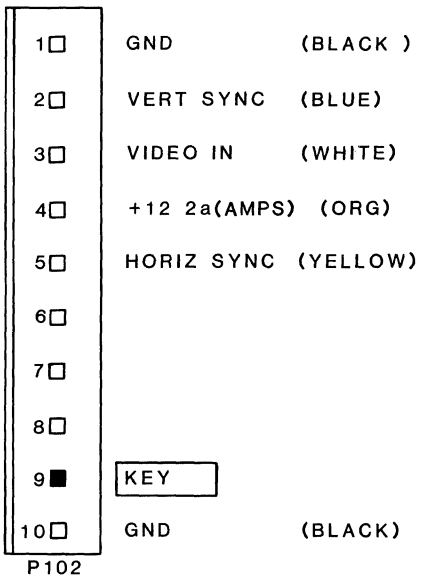

Figure 6.5. Video Interconnect

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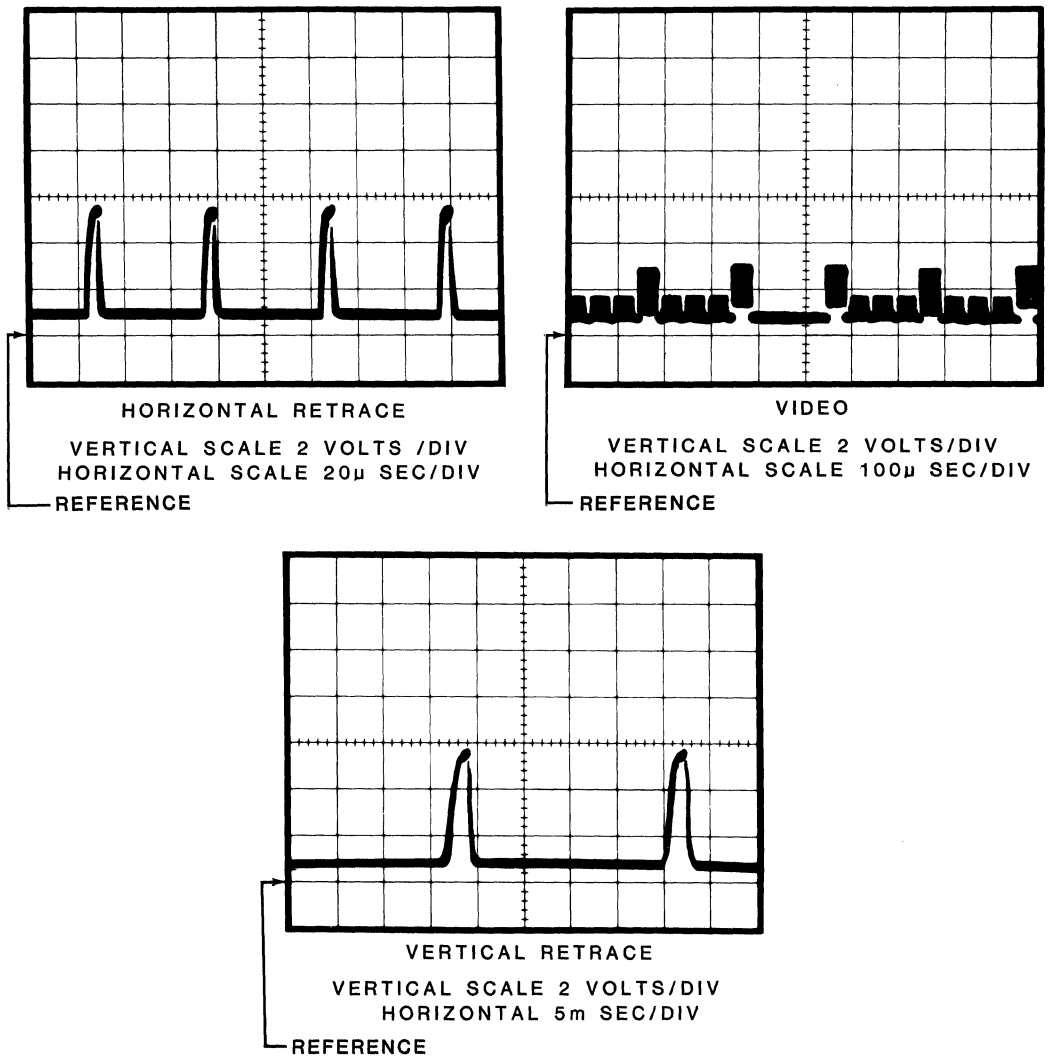

Figure 6.6. 60Hz Refresh, 80 Characters Per Line

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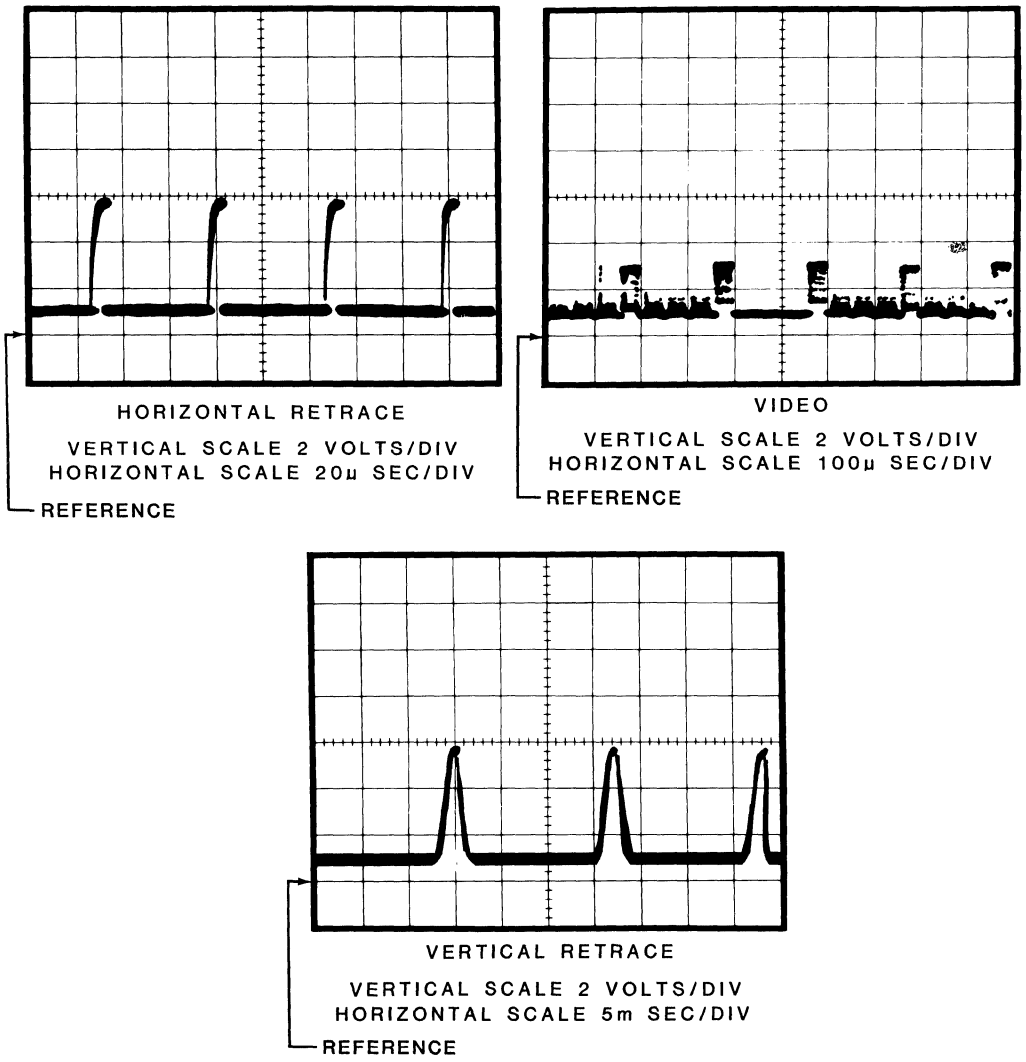

Figure 6.7. 50 Hz Refresh, 80 Characters Per Line

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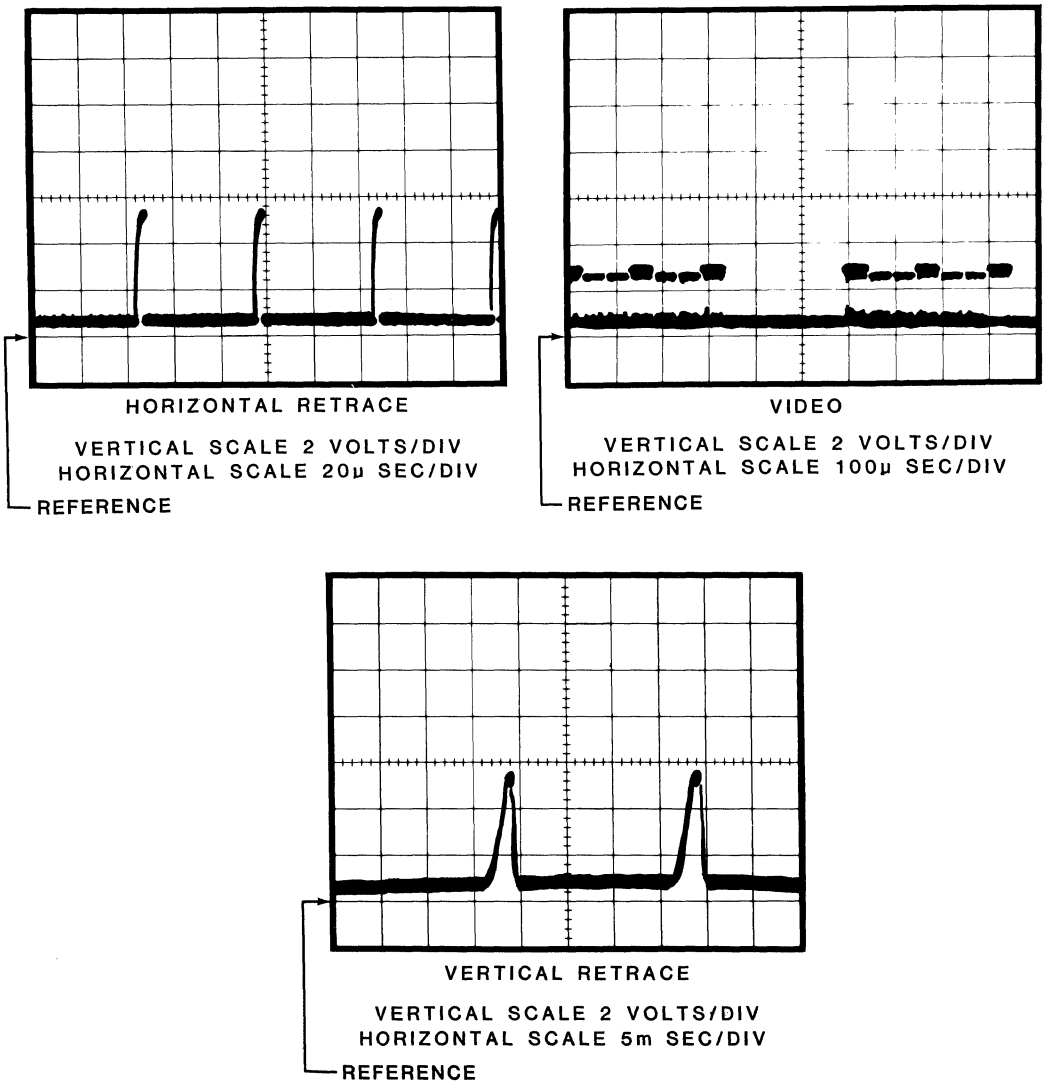

Figure 6.8. 60 Hz Refresh, 132 Characters Per Line

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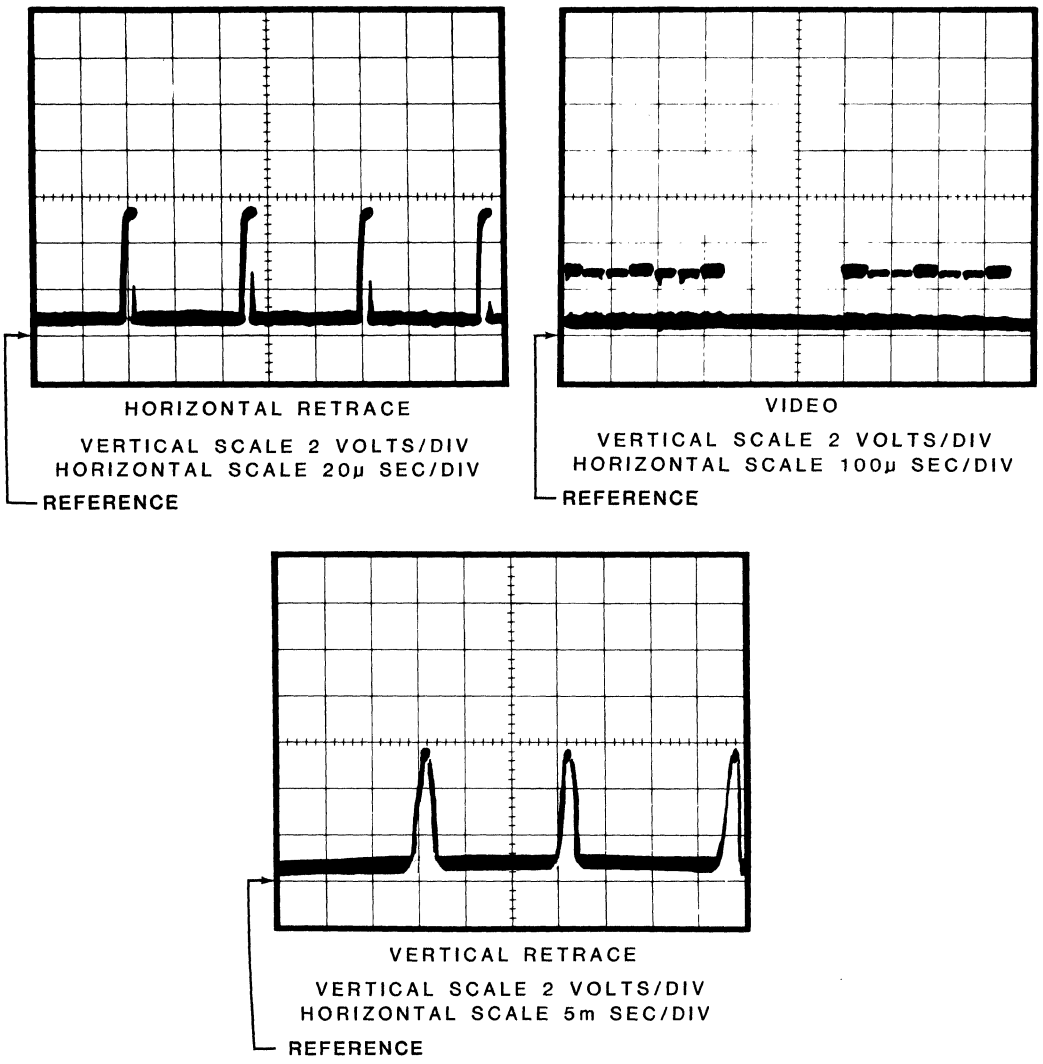

Figure 6.9. 50 Hz Refresh, 132 Characters Per Line

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Video Driver Board Troubleshooting

Refer to Tables 6.3, 6.4, 6.5, and waveforms Figures 6.10 through 6.12 for video driver board troubleshooting.

Table 6.3. Video Driver Board Troubleshooting

PROBLEM	POSSIBLE CAUSE
No Raster	Power supply, VX101, TX102. Check high voltage at the anode of the CRT. Check cathode to grid bias, Q102, Q103, CR104, TX202A, TX202B, R128, Q301, Q302.
Raster, No Video	Terminal logic board, Q401, Q402, VX101, CR401, CR111, CRT socket
No Vertical Deflection	R139, Q301, Q302, Q306, Q307
Vertical Off Frequency	Terminal logic board, Q301, Q302, C303
No Vertical Sync	Terminal logic board, C302, CRX301, C301, R301
Horizontal Off Frequency	Terminal logic board, Q106, Q107, Q108
No Horizontal Sync	Terminal logic board, Q101, R101, C101, R102, CR101
Horizontal Phasing	Q101, Q104, C103, R104, R105, R107, R103
Poor Horizontal Linearity or Foldover	TX102, LX101, LX102, CR104, TX202B, Q106, Q107, Q108, Q103, Q102
Narrow Picture	Q106, Q107, Q108, Q103, CR104, LX101, CR111
Edge of Screen Out of Focus	Q109, R155, R156, R153, R154, C137, C136, C134

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Video Driver Board Waveforms

The following waveforms are taken with the oscilloscope triggered at the beginning of the vertical sync pulse for vertical measurements, and the beginning of the horizontal sync pulse for horizontal measurements.

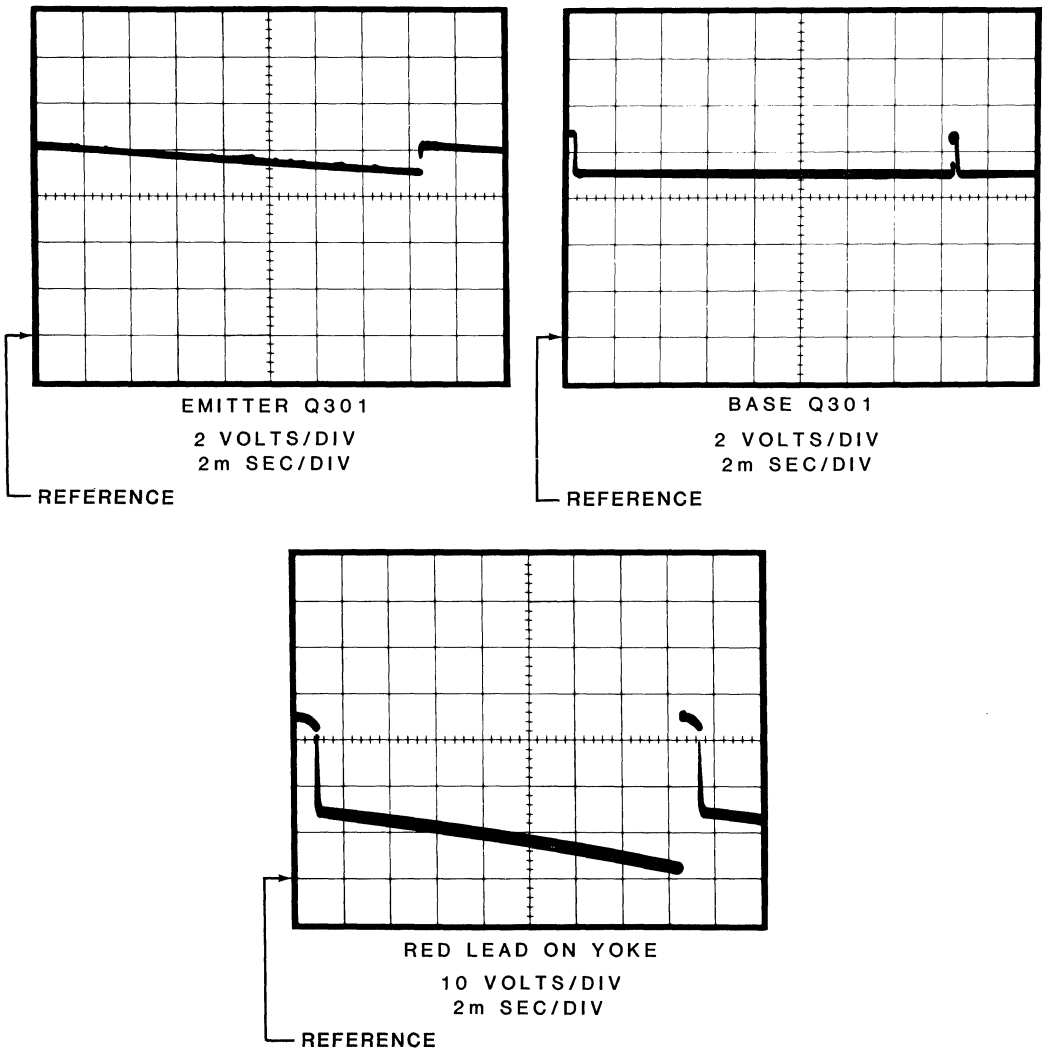

Figure 6.10. Vertical Circuit Waveforms

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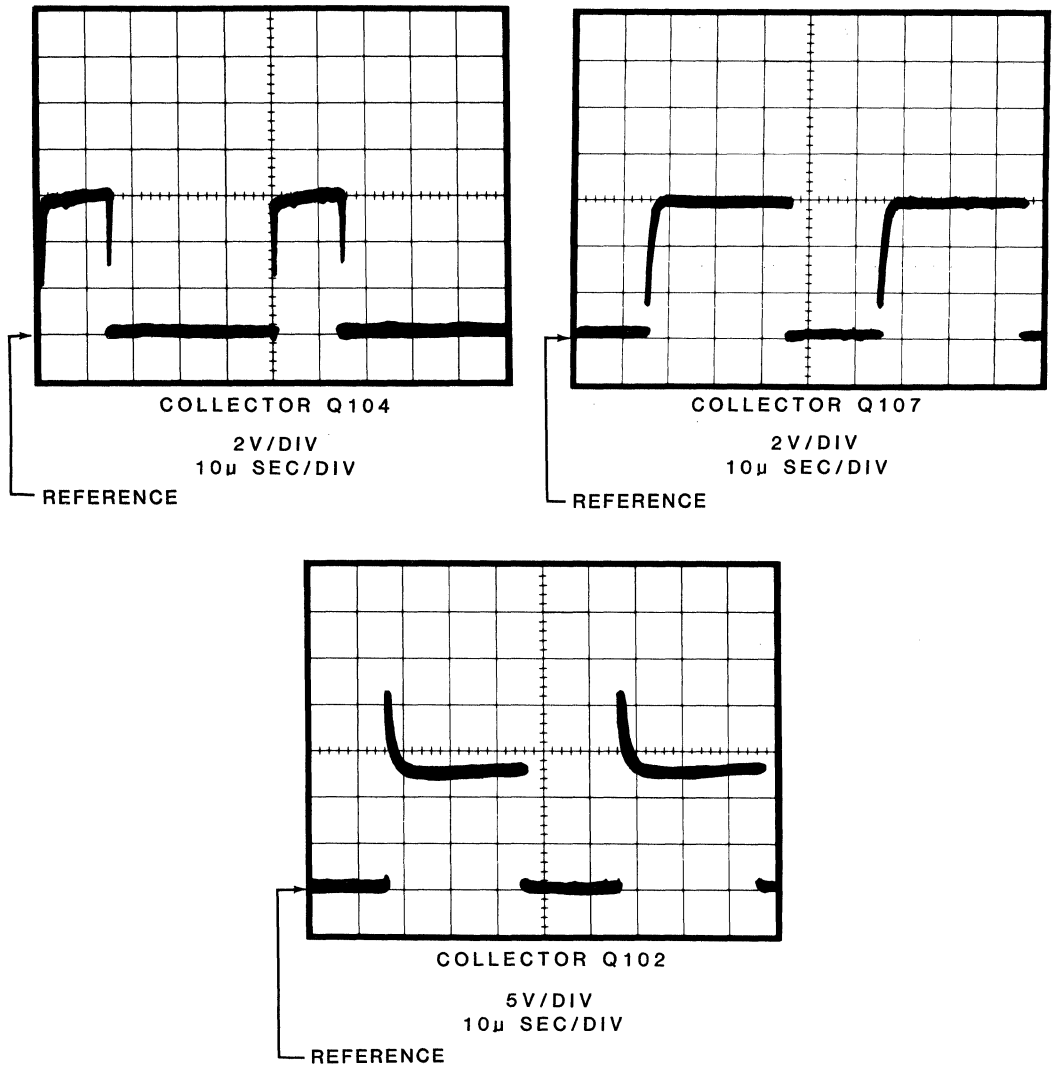

Figure 6.11. Low Voltage Horizontal Circuit Waveforms

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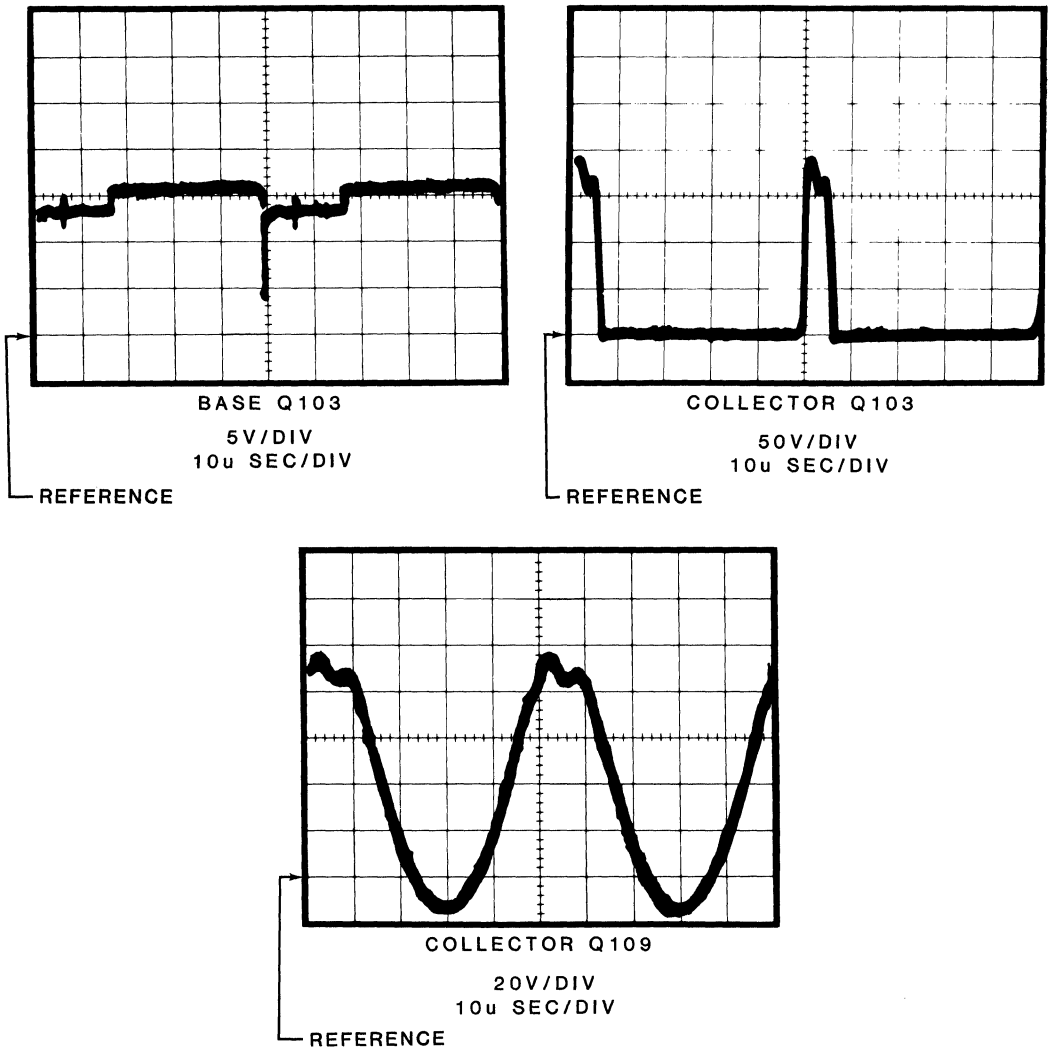

Figure 6.12. High Voltage Horizontal Circuit Waveforms

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Transistor Voltage Measurements

Refer to Table 6.4 for dynamic transistor voltage measurements.

Table 6.4. Transistor Voltage Measurements
(Reference Video Driver Board Ground)

TRANSISTOR	EMITTER	BASE	COLLECTOR
Q101	0 VDC	0.7 VDC	3.0 VDC
Q102	0 VDC	0.8 VDC	9.0 VDC
Q103	0 VDC	0.7 VDC	15.0 VDC
Q104	0 VDC	0.7 VDC	3.0 VDC
Q106	0 VDC	0.7 VDC	3.0 VDC
Q107	0 VDC	0.7 VDC	3.0 VDC
Q301	7.26 VDC	7.0 VDC	8.35 VDC
Q302	8.78 VDC	8.62 VDC	6.99 VDC
Q303	7.72 VDC	7.3 VDC	0.32 VDC
Q304	0 VDC	0.31 VDC	9.0 VDC
Q306	9.44 VDC	9.0 VDC	0 VDC
Q307	10.24 VDC	10.64 VDC	0 VDC
Q308	6.0 VDC	6.84 VDC	17.15 VDC
Q401	.03 VDC	0 VDC	6.5 VDC
Q402	6.5 VDC	7.2 VDC	50.0 VDC

Picture Tube Voltage Measurements

Refer to Table 6.5 for dynamic picture tube voltage measurements, and Figure 6.13 for picture tube socket pinout.

Table 6.5. Picture Tube Voltage Measurements
(Reference Video Driver Board Ground)

PIN	VOLTAGE
1	−50 TO 12 VDC
2	50 VDC
3	12 VDC
4	0 VDC
5	−50 TO 12 VDC
6	500 VDC
7	−50 TO 400 VDC
ANODE	12.5 KV (use high voltage probe)

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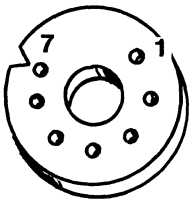

Figure 6.13. Picture Tube Socket Pinout

Keyboard Troubleshooting

If you suspect a problem with the keyboard, substitute a known good keyboard. If the problem remains, refer to Figure 6.13 and check the 8.5 VDC from the terminal logic board.

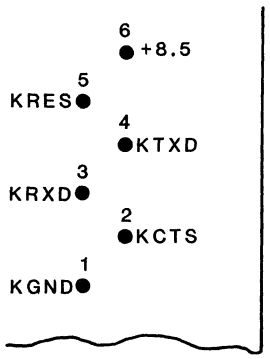

Figure 6.14. Terminal Logic Board to Keyboard Pinout (P103)

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Chapter 7

Reassembly

Cathode Ray Tube Installation (60)

To install the CRT, refer to Figure 7.1, the foldout at the end of this chapter.

1. Carefully place the cabinet front (5) face down on a smooth flat surface.

2. Carefully place and align the CRT (60) into the front mounting brackets (55, 10).

3. Install two #8 flat metal washers (80), the CRT ground clip (85), and one 8-32 × .375″ screw (75) into the upper right CRT bracket (55).

4. Install three insulated inside washers (70), three insulated outside washers (65), and three 8-32 × .375″ screws (75) into the remaining three locations.

5. Secure the power supply (140) to the power supply chassis (155) by installing two 6-32 × .375″ screws (105) into the bottom of the power supply chassis.

6. Carefully install the power supply chassis (155) and secure to the main chassis (170) using four 6-32 × .375″ screws (40).

7. Connect plugs P1 and P2 (150).

8. Install power supply cover (140) and solder lug (165) using two 6-32 × .375″ screws (40).

9. Secure the video circuit board (120) to the right side panel (115) using four 6-32 × .375″ screws (40).

10. Connect the 10-pin plug (125) to the video circuit board (120).

11. Secure the right side panel (115) to the chassis (170) using two 6-32 × .375″ screws (40), and tighten the two 6-32 × .375″ screws (40) securing the lower right RFI guard (25).

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Reassembly

12. Connect the yoke cables (90) (red/blue) to VERT YOKE and (yellow/black) to HORIZ YOKE on the video circuit board (120).

13. Connect the anode lead (Inset #2) to the CRT.

14. Carefully plug the CRT socket into the CRT.

15. Connect the black ground wire to the CRT ground clip (85).

16. Secure the terminal logic board (110) to the left side panel (100) using six 6-32 × .375″ screws (40).

17. Connect plugs P101 (125), P102 (150), and P105 (175).

18. Secure the left side panel (100) to the chassis (170) using two 6-32 × .375″ screws (40).

19. Secure the lower left RFI guard (25) to the front cabinet (5) using two 8-BT × .625″ screws (15).

20. Secure the lower left RFI guard (25) to the left side cover using two #6 washers (45) and two 6-32 × 250″ nuts (50).

21. Install top RFI shield (255) using two screws (103) and two screws (105).

22. Install a cable tie (280) to the video circuit board ferrite bead and route it (at the position previously noted) through the top of the RFI shield (255). Secure it in position using another cable tie. Cut off the excess ends of the cable ties.

23. Refer to Figure 7.2 and replace the cabinet top cover and rear panel using two 6-32 × .875″ screws in the top and two 4-40 × .375″ screws in the bottom of the rear panel.

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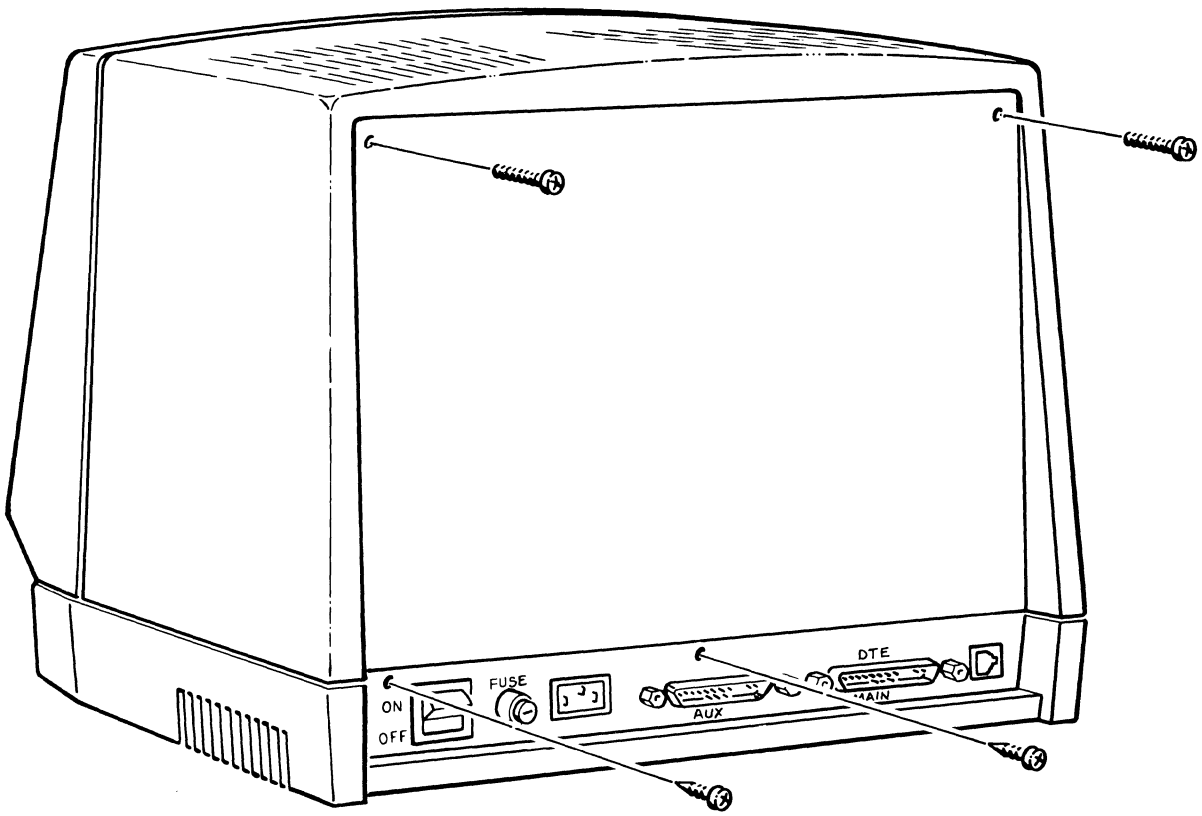

Figure 7.2. Cabinet Reassembly

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Power Supply Installation (135)

1. Secure the power supply to the power supply chassis by installing two 6-32 × .375″ screws (105) into the bottom of the power supply chassis (155).

2. Carefully install the power supply chassis (155) and secure to the main chassis (170) using four 6-32 × .375″ screws (40).

3. Connect plugs P1 and P2 (150).

4. Install power supply cover (140) and solder lug (165) using two 6-32 × .375″ screws (40).

5. Secure the video circuit board (120) to the right side panel (115) using four 6-32 × .375″ screws (40).

6. Connect the 10-pin plug (125) to the video circuit board (120).

7. Secure the right side panel (115) to the chassis (170) using two 6-32 × .375″ screws (40), and tighten the two 6-32 × .375″ screws (40) securing the lower right RFI guard (25).

8. Connect the yoke (90) cables (red/blue) to VERT YOKE and (yellow/black) to HORIZ YOKE on the video circuit board (120).

9. Connect the anode lead (Inset #2) to the CRT (60).

10. Carefully plug the CRT socket into the CRT (60).

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11. Connect the black ground wire to the CRT ground clip (85).

12. Secure the terminal logic board (110) to the left side panel (100) using six 6-32 × .375″ screws (40).

13. Connect plugs P101 (125), P102 (150), and P105 (175).

14. Secure the left side panel (100) to the chassis (170) using two 6-32 × .375″ screws (40).

15. Secure the lower left RFI guard (25) to the front cabinet (5) using two 8-BT × .625″ screws (15).

16. Secure the lower left RFI guard (25) to the left side cover (100) using two #6 washers (45) and two 6-32 × 250″ nuts (50).

17. Install top RFI shield (255) using two screws (103) and two screws (105).

18. Install a cable tie (280) to the video circuit board ferrite bead and route it (at the position previously noted) through the top of the RFI shield (255). Secure it in position using another cable tie. Remove cable tie excesses.

19. Refer to Figure 7.2 and replace the cabinet top cover and rear panel using two 6-32 × .875″ screws in the top and two 4-40 × .375″ screws in the bottom of the rear panel.

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Video Circuit Board Installation (120)

1. Secure the video circuit board to the right side panel (115) using four screws (132).

2. Connect the 10-pin plug (125) to the video circuit board.

3. Secure the right side panel (115) to the chassis (170) using two 6-32 × .375″ screws (40), and tighten the two 6-32 × .375″ screws (40) securing the lower right RFI guard.

4. Connect the yoke (90) cables (red/blue) to VERT YOKE and (yellow/black) to HORIZ YOKE on the video circuit board.

5. Connect the anode lead (Inset #2) to the CRT (60).

6. Carefully plug the CRT socket into the CRT (60).

7. Connect the black ground wire to the CRT ground clip (85).

8. Install top RFI (255) shield using two screws (103) and two screws (105).

9. Install a cable tie (280) to the video circuit board ferrite bead and route it (at the position previously noted) through the top of the RFI shield (255). Secure it in position using another cable tie. Cut off the excess ends of the cable ties.

10. Refer to Figure 7.2 and replace the cabinet top cover and rear panel using two 6-32 × .875″ screws in the top and two 4-40 × .375″ screws in the bottom of the rear panel.

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Terminal Logic Board Installation (110)

1. Secure the terminal logic board to the left side panel (100) using six 6-32 × .375″ screws (40).

2. Connect plugs P101 (125), P102 (150), and P105 (175).

3. Secure the left side panel (100) to the chassis (170) using two 6-32 × .375″ screws (40).

4. Secure the lower left RFI guard (25) to the front cabinet (5) using two 8-BT × .625″ screws.

5. Secure the lower left RFI guard (25) to the left side cover (100) using two #6 washers (45) and two 6-32 × 250″ nuts (50).

6. Install top RFI shield (255) using two screws (103) and two screws (105).

7. Install a cable tie (280) to the video circuit board ferrite bead and route it (at the position previously noted) through the top of the RFI shield. Secure it in position using another cable tie. Cut off the excess ends of the cable ties.

8. Refer to Figure 7.2 and replace the cabinet top cover and rear panel using two 6-32 × .875″ screws in the top and two 4-40 × .375″ screws in the bottom of the rear panel.

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Cabinet Top Installation

Refer to Figure 7.2 and replace the cabinet top cover and rear panel using two 6-32 × .875″ screws in the top and two 4-40 × .375″ screws in the bottom of the rear panel.

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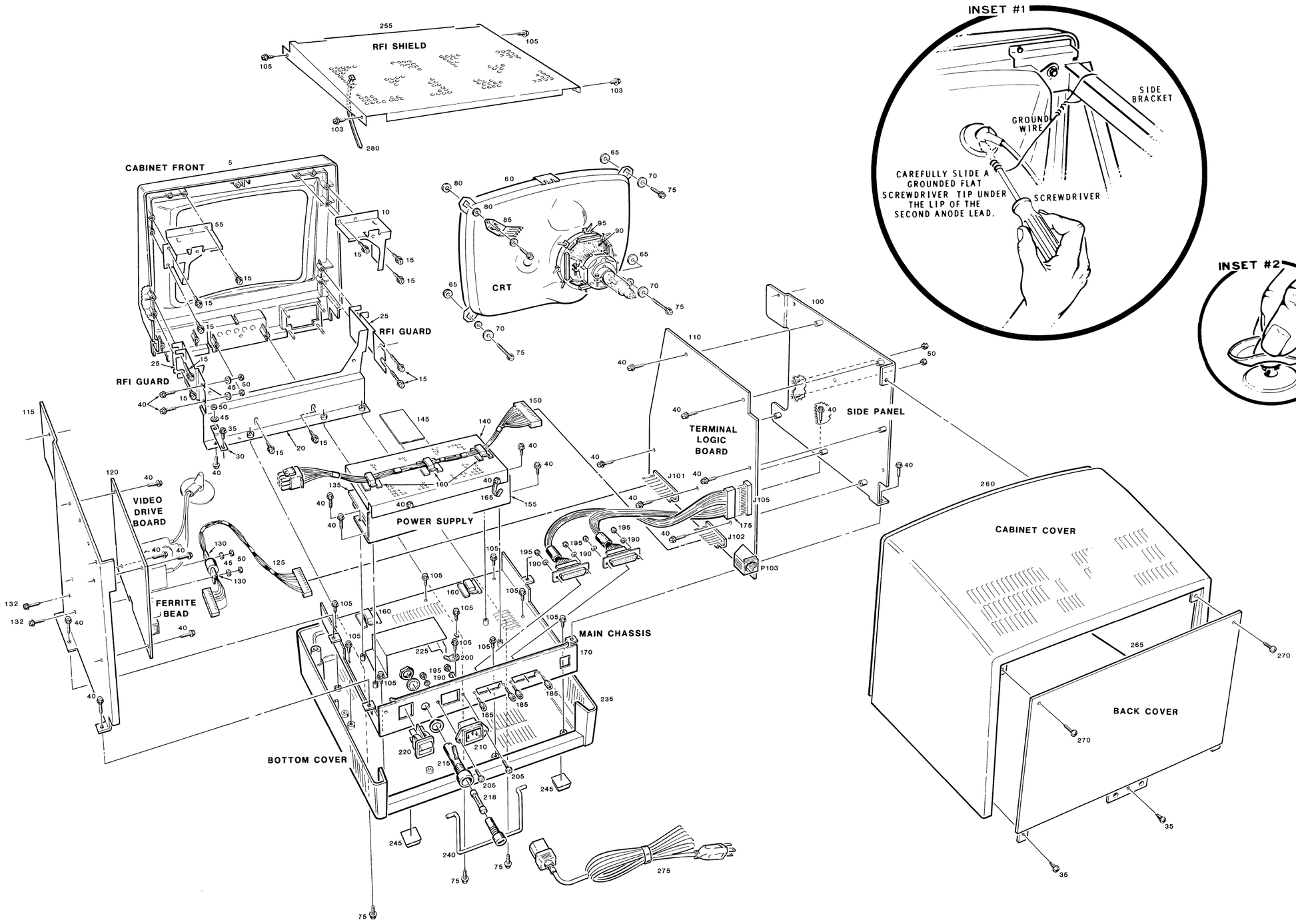

Figure 7.1. Reassembly

Chapter 8

Parts List

Introduction

This chapter provides an exploded view of the video display unit and keyboard. Component views of the terminal logic board, video circuit board, and keyboard circuit board are included to help you identify parts for replacement. Semiconductor identification also is included. No parts list or views are included for the power supply due to proprietary information.

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Video Display Unit

Refer to Figure 8.1, the exploded view of the video display unit, at the end of this chapter.

CAUTION: This unit contains ESD.

ITEM NUMBER	PART NUMBER	DESCRIPTION
5	HE 92-836-1	Cabinet, front panel
10	HE 204-2712	Bracket, top left
15	HE 250-1138	Screw, 8-BT × .625″
20	HE 204-2711	Bracket, CRT bottom
25	HE 204-2753	Bracket, RFI guard
30	HE 204-2714	Bracket, ground strap
35	HE 250-1307	Screw, 6-AB × .250″
40	HE 250-1264	Screw, 6-32 × .375″
45	HE 254-1	Washer, #6
50	HE 252-3	Nut, 6-32 × .250″
55	HE 204-2713	Bracket, top right
60	HE 234-612	Picture tube, amber
	HE 234-205	Picture tube, green
65	HE 253-748	Washer, shoulder, insulated
70	HE 253-747	Washer, flat, insulated
75	HE 250-1314	Screw, 8-32 × .375″
80	HE 253-45	Washer, #8
85	080-02377	CRT ground spring
90	A-08337	Yoke
95	149-00464-01	Magnet
100	HE 203-2209	Panel, left side
103	HE 250-83	Screw, 10-BT × .375″
105	HE 250-1232	Screw, 8-BT × .375″
110	HE 181-4501	Terminal logic board
115	HE 203-2208	Panel, right side
120	A10856	Video driver board assembly
125	HE 475-35	RF core
130	HE 207-5	Cable clamp
135	HE 234-429	Power supply
140	HE 203-2193	Panel, guard
145	HE 75-741	Insulator, fish paper
132	HE 250-1331	Screw

ITEM NUMBER	PART NUMBER	DESCRIPTION
150	HE 134-1400	Cable assembly
155	HE 203-2185	Panel, power supply mounting
160	HE 208-50	Clip
165	HE 259-29	Solder lug
170	HE 200-1449-3	Chassis, main
175	HE 134-1453	Cable assembly
180	HE 475-36	RF core
185	HE 255-757	Spacer, hex
190	HE 254-9	Washer, #4
195	HE 252-15	Nut, 4-40 × .187″
200	HE 259-1	Solder lug
205	HE 250-1412	Screw, 4-40 × .375″
210	HE 434-354	Line cord connector
215	HE 423-11	Fuse holder
218	HE 421-6	Fuse, 3AG slow blow
220	HE 61-43	Rocker switch, DPDT
225	HE 75-840	Insulator
230	Deleted	
235	HE 92-766	Cabinet, bottom
240	HE 266-1205	Wire tilt foot
245	HE 261-28	Foot
250	HE 134-1403	Cable assembly
255	HE 206-1480	Shield, top RFI
260	HE 92-765	Cabinet, top
265	HE 203-2182-3	Panel, rear
270	HE 250-1240	Screw, 6-32 × .875″
275	HE 89-60	Line cord
280	HE 354-5	Cable tie
	HE 354-7	
285	HE 391-648	ZDS logo nameplate

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Terminal Logic Board

Refer to Figure 8.2, the component view of the terminal logic board, at the end of this chapter.

CAUTION: This board contains ESD.

NOTE: Refer to semiconductor identification or the data sheets in Chapter 9 for a description of semiconductor devices.

CIRCUIT REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
Capacitors		
C100	HE 25-195	2.2 µF tantalum
C101	HE 25-195	2.2 µF tantalum
C102	HE 21-769	.01 µF ceramic
C103	HE 21-769	.01 µF ceramic
C104	HE 25-942	220 µF electrolytic
C105	Not used	
C106	Not used	
C107	Not used	
C108	Not used	
C109	Not used	
C110	HE 25-942	220 µF electrolytic
C111	HE 21-769	.01 µF ceramic
C112	HE 25-195	2.2 µF tantalum
C113	Not used	
C114	Not used	
C115	Not used	
C116	Not used	
C117	Not used	
C118	Not used	
C119	Not used	
C120	Not used	
C121	Not used	
C122	HE 21-762	.1 µF ceramic
C123	HE 25-195	2.2 µF tantalum
C124	Not used	
C125	Not used	

CIRCUIT REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
C126	Not used	
C127	Not used	
C128	Not used	
C129	HE 21-769	.01 µF ceramic
C130	HE 25-195	2.2 µF tantalum
C131	HE 25-195	2.2 µF tantalum
C132	HE 21-769	.01 µF ceramic
C133	Not used	
C134	Not used	
C135	HE 21-718	20 pF ceramic
C136	HE 25-195	2.2 µF tantalum
C137	HE 21-769	.01 µF ceramic
C138	Not used	
C139	Not used	
C140	HE 25-942	220 µF electrolytic
C141	Not used	
C142	Not used	
C143	Not used	
C144	Not used	
C145	Not used	
C146	Not used	
C147	Not used	
C148	Not used	
C149	Not used	
C150	Not used	

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Parts List

CIRCUIT REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
Capacitors (continued)		
C151	Not used	
C152	Not used	
C153	Not used	
C154	Not used	
C155	Not used	
C156	Not used	
C157	Not used	
C158	Not used	
C159	Not used	
C160	Not used	
C161	Not used	
C162	Not used	
C163	Not used	
C164	Not used	
C165	Not used	
C166	Not used	
C167	HE 25-195	2.2 µF tantalum
C168	HE 21-769	.01 µF ceramic
C169	HE 21-43	.001 µF ceramic
C170	HE 21-43	.001 µF ceramic
C171	HE 25-195	2.2 µF tantalum
C172	Not used	
C173	Not used	
C174	HE 21-172	100 pF ceramic
C175	Not used	
C176	HE 21-762	.1 µF ceramic
C177	Not used	
C178	HE 25-195	2.2 µF tantalum
C179	HE 21-762	.1 µF ceramic
C180	Not used	
C181	HE 25-195	2.2 µF tantalum
C182	HE 21-769	.01 µF ceramic
C183	HE 25-195	2.2 µF tantalum
C184	HE 25-195	2.2 µF tantalum
C185	Not used	
C186	HE 21-799	1 µF ceramic
C187	HE 21-799	1 µF ceramic
C188	HE 25-942	220 µF electrolytic
C189	HE 25-927	22 µF electrolytic
C190	HE 25-917	10 µF electrolytic
C191	HE 25-195	2.2 µF tantalum
C192	HE 21-769	.01 µF ceramic
C193	Not used	
C194	HE 21-769	.01 µF ceramic
C195	Not used	
C196	HE 21-769	.01 µF ceramic
C197	Not used	
C198	HE 21-769	.01 µF ceramic
C199	Not used	
C200	Not used	
C201	HE 25-841	4.7 µF tantalum
Diodes		
D100	Not used	
D101	Not used	
D102	Not used	
D103	Not used	
D104	Not used	
D105	Not used	
D106	Not used	
D107	Not used	
D108	HE 56-56	1N4149
D109	HE 56-56	1N4149
Inductors		
L100	HE 475-33	Ferrite bead
L101	HE 475-33	Ferrite bead
L102	HE 475-33	Ferrite bead
L103	HE 475-33	Ferrite bead
L104	HE 475-33	Ferrite bead
L105	HE 475-33	Ferrite bead
L106	HE 475-33	Ferrite bead
L107	HE 475-33	Ferrite bead
L108	HE 40-2120	25 µH fixed
L109	HE 475-33	Ferrite bead
L110	HE 475-33	Ferrite bead

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CIRCUIT REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
Inductors (continued)		
L111	HE 235-229	35 µH RF choke
L112	HE 475-10	Ferrite bead
L113	HE 235-229	35 µH RF choke
L114	HE 235-229	35 µH RF choke
L115	HE 235-229	35 µH RF choke
L116	HE 235-229	35 µH RF choke
Connectors		
P100	Not used	
P101	HE 432-1328	26-pin
P102	HE 432-1327	10-pin Molex
P103	Not used	
P104	HE 432-1327	10-pin Molex
P105	HE 434-362	Phone jack
Transistors		
Q100	Not used	
Q101	HE 417-875	2N3904
Q102	HE 417-875	2N3904
Resistors		
R100	HE 6-3169	31.6 Ω
R101	HE 6-103-12	10 kΩ
R102	HE 6-103-12	10 kΩ
R103	HE 6-103-12	10 kΩ
R104	HE 6-681-12	680 Ω
R105	HE 6-103-12	10 kΩ
R106	HE 6-103-12	10 kΩ
R107	HE 6-472-12	4.7 kΩ
R108	HE 6-472-12	4.7 kΩ
R109	HE 6-153-12	15 kΩ
R110	HE 6-471-12	470 Ω
R111	HE 6-104-12	100 kΩ
R112	HE 6-471-12	470 Ω
R113	HE 6-471-12	470 Ω
R114	HE 6-6040-12	604 Ω
R115	HE 6-2870-12	287 Ω

CIRCUIT REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
R116	HE 6-6040-12	604 Ω
R117	HE 6-3749-12	37.4 Ω
R118	HE 6-1241-12	1240 Ω
R119	HE 6-1300-12	130 Ω
R120	HE 6-1211-12	1210 Ω
R121	HE 6-2211-12	2210 Ω
R122	HE 6-4530-12	453 Ω
R123	HE 6-7150-12	715 Ω
R124	HE 6-101-12	100 Ω
R125	HE 6-303-12	30 kΩ
R126	HE 6-562-12	5.6 kΩ
R127	HE 6-471-12	470 Ω
R128	HE 6-471-12	470 Ω
R129	HE 6-102-12	1 kΩ
R130	HE 6-220-12	22 Ω
RP100	HE 9-133	4.7 kΩ resistor pack
RP101	Not used	
RP102	HE 9-133	4.7 kΩ resistor pack
RP103	HE 9-133	4.7 kΩ resistor pack
RP104	HE 9-133	4.7 kΩ resistor pack
Switches		
SW100	HE 60-644	Slide SPST
SW101	HE 60-644	Slide SPST
SW102	Not used	
Integrated Circuits		
U100	HE 443-1104	PIA
	HE 434-253	40-pin socket
U101	HE 443-863	F-F octal D tri-state
	HE 434-131	20-pin socket
U102	Not used	
	HE 434-131	20-pin socket
U103	HE 444-193	Nonvolatile RAM
	HE 434-312	28-pin socket
U104	HE 444-251-1	Program ROM
	HE 434-312	28-pin socket
U105	HE 444-212-1	Program ROM
	HE 434-312	28-pin socket

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Parts List

CIRCUIT REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
Integrated Circuits (continued)		
U106	HE 443-863	F-F octal D tri-state
	HE 434-131	20-pin socket
U107	HE 443-1027	RAM 2K × 8
	HE 434-312	28-pin socket
U108	HE 443-1027	RAM 2K × 8
	HE 434-312	28-pin socket
U109	HE 444-213	Memory select
	HE 434-368	24-pin socket
U110	HE 444-210-1	Character ROM
	HE 434-312	28-pin socket
U111	HE 443-1027	RAM 2K × 8
	HE 434-312	28-pin socket
U112	HE 443-1027	RAM 2K × 8
	HE 434-312	28-pin socket
U113	Not used	
U114	Not used	
U115	HE 443-1135	Attribute controller
	HE 432-253	40-pin socket
U116	HE 443-1027	RAM 2K × 8
	HE 434-312	28-pin socket
U117	HE 443-1027	RAM 2K × 8
	HE 434-312	28-pin socket
U118	HE 443-1070	Transparent latch
	HE 434-311	20-pin socket
U119	HE 443-1069	Microprocessor
	HE 434-253	40-pin socket
U120	HE 443-1134	Video display controller
	HE 434-253	40-pin socket
U121	HE 443-1103	Quad mux
	HE 434-299	16-pin socket
U122	HE 443-1136	DUART
	HE 434-253	40-pin socket
U123	HE 443-795	RS-232 receiver
	HE 434-298	14-pin socket
U124	HE 443-863	F-F octal D tri-state
	HE 434-131	20-pin socket
U125	HE 443-863	F-F octal D tri-state
	HE 434-131	20-pin socket
U126	HE 443-1070	Transparent latch
	HE 434-311	20-pin socket
U127	HE 443-877	Decoder
	HE 434-299	16-pin socket
U128	HE 443-794	Driver RS-232
	HE 434-298	14-pin socket
U129	HE 443-863	F-F octal D tri-state
	HE 434-131	20-pin socket
U130	HE 443-863	F-F octal D tri-state
	HE 434-131	20-pin socket
U131	HE 443-1072	Quad 2-input OR gate
	HE 434-298	14-pin socket
U132	HE 443-1072	Quad 2-input OR gate
	HE 434-298	14-pin socket
U133	HE 443-1051	F-F dual D
	HE 434-298	14-pin socket
U134	HE 443-1073	Quad 2-input AND gate
	HE 434-298	14-pin socket
U135	HE 443-755	Hex inverter
	HE 434-298	14-pin socket
U136	HE 443-1051	F-F dual D
	HE 434-298	14-pin socket
U137	HE 443-1073	Quad 2-input AND gate
	HE 434-298	14-pin socket
U138	HE 443-863	F-F octal D tri-state
	HE 434-131	20-pin socket
U139	HE 443-863	F-F octal D tri-state
	HE 434-131	20-pin socket
U140	HE 443-1129	ACIA
	HE 434-307	24-pin socket
U141	HE 443-794	Driver RS-232
	HE 434-298	14-pin socket
U142	HE 443-863	F-F octal D tri-state
	HE 434-131	20-pin socket
U143	HE 443-863	F-F octal D tri-state
	HE 434-131	20-pin socket
U144	HE 443-1137	Inverter
	HE 434-298	14-pin socket
U145	HE 443-1072	Quad 2-input OR gate
	HE 434-298	14-pin socket

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Parts List

CIRCUIT REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
Integrated Circuits (continued)		
U146	HE 443-728	Quad 2-input NAND gate
	HE 434-298	14-pin socket
U147	HE 443-973	Binary counter
	HE 434-298	14-pin socket
U148	HE 443-1051	F-F dual D
	HE 434-298	14-pin socket
U149	HE 443-779	Quad 2-input NOR gate
	HE 434-298	14-pin socket
U150	HE 443-891	Quad 2-input XOR
	HE 434-298	14-pin socket
U151	HE 443-1031	F-F octal D
	HE 434-311	20-pin socket
U152	HE 443-1008	Dual monostable
	HE 434-299	16-pin socket
U153	HE 443-795	RS-232 receiver
	HE 434-298	14-pin socket
U154	HE 443-1020	Hex buffer
	HE 434-298	14-pin socket
U155	HE 443-1128	2-input NAND open collector
	HE 434-298	14-pin socket
U156	HE 442-708	Voltage regulator
	HE 250-357	Screw
	HE 215-699	Heat sink
	HE 75-204	Insulator
	HE 254-1	Lockwasher
	HE 252-3	Nut
*U157	HE 443-1167	RS-422 Line driver
	HE 434-299	16-pin socket
Crystals		
Y100	HE 404-659	3.6864 MHz crystal
Y101	HE 150-139	19.7676 MHz oscillator circuit
Y102	HE 150-140	24.8064 MHz oscillator circuit

*NOTE: Installed in SW102 position.

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CRT Monitor/Video Driver

Refer to Figure 8.3, the component view of the video circuit board, at the end of this chapter.

NOTE: Refer to semiconductor identification or the data sheets in Chapter 9 for a description of semiconductor devices.

CIRCUIT REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
Capacitors		
C101	022-07742-04	330 pF ceramic
C102	022-07743-30	56 pF ceramic
C103	022-07773	.001 µF polyester
C104	022-07743-30	56 pF ceramic
C105	022-07773	.001 µF polyester
C106	022-07742-07	560 pF ceramic
C107	022-07615-08	.022 µF disc
C108	022-07859-07	35 µF electrolytic
C109	022-07773	.001 µF polyester
C110	Not Used	
C111	Not Used	
C112	Not Used	
C113	022-07860-08	47 µF electrolytic
C114	022-07615-08	.022 µF disc
C115	Not Used	
C116	Not Used	
C117	Not Used	
C118	022-07615-08	.022 µF disc
C119	022-07440	.0047 pF ceramic disc
C120	Not Used	
C121	022-00781	1000 pF ceramic disc
C122	022-07864-06	22 µF electrolytic
C123	022-07860-10	220 µF electrolyic
C124	022-07860-10	220 µF electrolyic
C125	Not Used	
C126	022-07371	1 µF electroylic
C127	022-07774-12	.01 µF polyester
C128	022-00781	1000 pF ceramic disc
C129	022-00781	1000 pF ceramic disc
C130	Not Used	
C131	Not Used	
C132	Not Used	
C133	Not Used	
C134	022-07371	1 µF electroylic
C135	Not Used	
C136	022-03512	.01 µF disc
C137	022-07742-12	1500 pF ceramic
C301	022-07742-12	1500 pF ceramic
C302	022-07742	150 pF ceramic
C303	022-07773-24	.1 µF polyester
C304	022-07859-07	33 µF electrolytic
C305	Not Used	
C306	022-07614-24	.01 µF disc
C307	022-07860-05	10 µF electrolytic
C308	022-07862-01	1 µF electrolytic
C309	022-07862-01	1 µF electrolytic
C310	Not Used	
C311	022-07860-08	47 µF electrolyic
C312	022-07860-08	47 µF electrolyic
C313	022-07860-05	10 µF electrolytic
C314	022-07615-08	.022 µF disc
C315	Not Used	
C316	022-07859-12	470 µf electrolytic
C317	022-07860-10	220 µf electrolytic
C401	022-07864-06	22 µf electrolytic
C402	022-07860-05	10 µf electrolytic
C403	022-07743-26	39 pf ceramic
C404	Not Used	
CX116	022-07798-02	.015 µF polypropylene
CX117	022-07892-04	6.8 µF electrolytic

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Parts List

CIRCUIT REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
Diodes		
CR101	103-00142-01	
CR102	Not Used	
CR103	103-00142-01	
CR104	103-00339-04	
CR105	Not Used	
CR106	103-00323-04	
CR107	103-00295-03	
CR108	63-07893	Resistor 390 kΩ
CR109	103-00339-02	
CR110	Not Used	
CR111	103-00323-03	
CR112	103-00252-01	
CR113	103-00142-01	
CR114	103-00142-01	
CR115	Not Used	
CR201	Not Used	
CR202	Not Used	
CR301	Not Used	
CR302	103-00142-01	
CR303	103-00142-01	
CR304	103-00142-01	
CR305	Not Used	
CR306	Not Used	
CR307	Not Used	
CR308	Not Used	
CR309	Not Used	
CR310	Not Used	
CR401	103-00254-01	
CR402	103-00295-03	
CR403	Not Used	
CR404	Not Used	
CRX301	103-00279-23	14 V zener
Inductors		
L101	Not Used	
L102	Not Used	
L103	Not Used	
L104	020-03907-05	2.7 μH coil
LX101	020-03943-04	Tunable coil
LX102	020-03906	Linearity coil

CIRCUIT REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
Transistors		
Q101	121-00975	
Q102	121-01040	
Q103	121-01070	
	126-02096	Heat sink
Q104	121-00975	
Q105	Not Used	
Q106	121-00975	
Q107	121-00975	
Q108	121-01093	
Q109	121-01058	
Q301	121-00975	
Q302	121-00699	
Q303	121-00699	
Q304	121-01040	
Q305	Not Used	
Q306	121-01036	
Q307	121-01035	
Q308	121-01040	
Q309	Not Used	
Q401	121-01088	
	126-01910	Heat sink
Q402	121-01090	
Resistors		
R101	063-10236	15 kΩ
R102	063-10235-66	560 Ω
R103	063-10651-02	2.5 kΩ phase control
R104	063-10236-04	22 kΩ
R105	063-10236-16	68 kΩ
R106	063-10235-72	1 kΩ
R107	063-10236-26	180 kΩ
R108	063-10235-96	10 kΩ
R109	063-10236-04	22 kΩ
R110	063-10235-72	1 kΩ
R111	063-10235-96	10 kΩ
R112	063-10235-72	1 kΩ
R113	063-10938-76	47 kΩ
R114	063-10234-23	130 kΩ
R115	Not Used	

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Parts List

CIRCUIT REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
Resistors (continued)		
R116	063-10234-35	430 kΩ
R117	063-10938-71	43 kΩ
R118	063-10183-48	100 Ω
R119	063-10235-72	1 kΩ
R120	063-10235-74	1.2 kΩ
R121	063-10236-02	18 kΩ
R122	Not Used	
R123	Not Used	
R124	Not Used	
R125	Not Used	
R126	Not Used	
R127	063-10183-54	180 Ω
R128	063-10235-46	82 Ω
R129	Not Used	
R130	Not Used	
R131	063-10235-68	680 Ω
R132	063-10236-04	22 kΩ
R133	Not Used	
R134	Not Used	
R135	063-10420-24	1 Ω
R136	Not Used	
R137	063-07799	2.2 kΩ
	103-00323-02	Diode
R138	063-10184-18	82 kΩ
R139	063-10651-12	100 kΩ brite control
R140	Not Used	
R141	Not Used	
R142	Not Used	
R143	Not Used	
R144	063-10184-18	82 kΩ
R145	Not Used	
R146	Not Used	
R147	063-10184-36	470 kΩ
R148	063-10651-14	2 MΩ focus control
R149	063-10184-32	330 kΩ
R150	Not Used	
R151	Not Used	
R152	Not Used	
R153	063-10235-80	2.2 kΩ
R154	063-10235-78	1.8 kΩ
R155	063-10236-20	100 kΩ

CIRCUIT REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
R156	063-10236-28	220 kΩ
R201	063-07968-40	3.3 Ω
R202	063-07763	330 Ω
R203	063-07799	2.2 kΩ
R204	063-07627	10 kΩ
R205	063-07855	47 kΩ
R301	063-10235-90	5.6 kΩ
R302	063-10236-04	22 kΩ
R303	063-10236-27	200 kΩ
R304	063-10183-40	47 Ω
R305	Not Used	
R306	063-10236	15 kΩ
R307	063-10235-92	6.8 kΩ
R308	063-10236-06	27 kΩ
R309	063-10236-52	2.2 MΩ
R310	Not Used	
R311	063-10236-48	1.5 MΩ
R312	063-10651-13	250 kΩ vertical control
R313	063-10183-48	100 Ω
R314	063-10235-98	12 kΩ
R315	Not Used	
R316	063-10236-06	27 kΩ
R317	063-10235-80	2.2 kΩ
R318	063-10183-48	100 Ω
R319	063-10236-12	47 kΩ
R320	Not Used	
R321	063-10235-80	2.2 kΩ
R322	063-10235-80	2.2 kΩ
R323	Not Used	
R324	063-10243-56	220 Ω
R325	Not Used	
R326	063-10235-45	75 Ω
R327	063-10235-84	3.3 kΩ
R328	063-10235-62	390 Ω
R329	063-10235-68	680 Ω
R330	Not Used	
R331	063-10235-10	2.7 Ω
R332	Not Used	
R333	Not Used	
R334	Not Used	

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CIRCUIT REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
Resistors (continued)		
R335	Not Used	
R336	Not Used	
R337	063-10183-48	100 Ω
R338	Not Used	
R401	Not Used	
R402	063-10428-86	390 Ω
R403	063-10235-72	1 kΩ
R404	063-10235-72	1 kΩ
R405	Not Used	
R406	063-10183-40	47 Ω
R407	Not Used	
R408	Not Used	
R409	063-10183-40	47 Ω
R410	Not Used	
R411	Not Used	
R412	063-10183-34	27 Ω
R413	063-10183-38	39 Ω
R414	063-10236	15 kΩ
R415	Not Used	
R501	063-10824	165 MΩ bleeder
RX122	063-10243-61	360 Ω
RX123	063-10836-44	68 Ω
RX124	Not Used	
RX134	Not Used	
RX323	063-10559-24	10 Ω
RX332	Not Used	
RX333	063-10832-40	47 Ω
RX416	063-10559-32	22 Ω
Transformers		
TX101	095-03136	Horizontal driver
TX102	095-03575-02	Sweep transformer
	019-00642	Anode clip and cap
TX201	Not Used	
TX202	095-03397-02	Deflection yoke
Vacuum Tube		
VX101	HE 234-533	CRT, amber
	HE 234-205	CRT, green

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Keyboard Unit

Refer to Figure 8.4, the exploded view of the keyboard unit, at the end of this chapter.

ITEM NUMBER	PART NUMBER	DESCRIPTION
5	HE 92-804	Cabinet
10	HE 134-1345	Cable assembly
15	HE 73-142	Foam
20	HE 950-31	Wired keyboard assembly
25	HE 250-365	Screw 6-AB × .250″
30	HE 205-1923-1	Plate
35	HE 266-1220	Support legs
40	HE 258-759	Leg return spring
45	HE 73-192	Foam
50	HE 75-109	Fish paper
55	HE 250-1434	6-BT × .375″
60	HE 75-138	Foot
65	HE 485-54	Plug

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Keyboard Assembly

Refer to Figure 8.5, the component view of the keyboard, at the end of this chapter. The wired and assembled keyboard part number is HE-181-4957.

NOTE: Refer to semiconductor identification or the data sheets in Chapter 9 for a description of semiconductor devices.

CIRCUIT REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
Buzzer		
BUZ	391R	Piezoelectric buzzer
Capacitors		
C1	Not Avail.	2.2 µF
C2	Not Avail.	1 µF
C3	Not Avail.	.01 µF
C4	Not Avail.	.01 µF
C5	Not Avail.	.01 µF
C6	Not Avail.	.01 µF
C7	Not Avail.	10 µF
C8	Not Avail.	22 pF
C9	Not Avail.	.01 µF
C10	Not Avail.	.01 µF
C11	Not Avail.	.01 µF
C12	Not Avail.	.01 µF
C13	Not Avail.	.01 µF
C14	Not Avail.	.01 µF
C15	Not Avail.	.01 µF
C16	Not Avail.	22 µF
C17	Not Avail.	.1 µF
C18	Not Avail.	2.2 µf
C19	Not Avail.	.01 µF
Diodes		
D1	Not Avail.	Not Avail.
D2	Not Avail.	Not Avail.

CIRCUIT REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
Inductors		
L1	Not Used	
L2	Not Used	
L3	Not Used	
L4	Not Used	
L5	Not Avail.	33 µH
L6	Not Avail.	33 µh
LEDs		
L1	Not Avail.	Red
L2	Not Avail.	Red
L3	Not Avail.	Red
L4	Not Avail.	Red
L5	Not Avail.	Red
L6	Not Avail.	Red
L7	Not Avail.	Red
L8	Not Avail.	Green
Resistors		
R1	Not Avail.	4.7 kΩ
R2	Not Avail.	4.7 kΩ
R3	Not Avail.	4.7 kΩ
R4	Not Avail.	4.7 kΩ
R5	Not Avail.	4.7 kΩ
R6	Not Avail.	4.7 kΩ
R7	Not Avail.	4.7 kΩ
R8	Not Avail.	4.7 kΩ
R9	Not Avail.	4.7 kΩ
R10	Not Avail.	4.7 kΩ

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Parts List

CIRCUIT REFERENCE DESIGNATOR	PART NUMBER	DESCRIPTION
Resistors (continued)		
R11	Not Avail.	4.7 kΩ
R12	Not Avail.	4.7 kΩ
R13	Not Avail.	4.7 kΩ
R14	Not Avail.	4.7 kΩ
R15	Not Avail.	4.7 kΩ
R16	Not Avail.	1 kΩ
R17	Not Avail.	150 Ω
R18	Not Avail.	150 Ω
R19	Not Avail.	150 Ω
R20	Not Avail.	150 Ω
R21	Not Avail.	150 Ω
R22	Not Avail.	150 Ω
R23	Not Avail.	150 Ω
R24	Not Avail.	180 Ω
R25	Not Avail.	4.7 kΩ
R26	Not Avail.	4.7 kΩ
R27	Not Avail.	4.7 kΩ
R28	Not Avail.	4.7 kΩ
R29	Not Avail.	4.7 kΩ
R30	Not Avail.	68 Ω
R31	Not Avail.	4.7 kΩ
R32	Not Avail.	4.7 kΩ
R33	Not Avail.	4.7 kΩ
R34	Not Avail.	4.7 kΩ
Integrated Circuits		
U201	HE 444-211	Keyboard encoder
	HE 434-253	Socket
U202	HE 443-791	Tri-state octal buffer
U203	Not Avail.	4 to 16 decoder (74HC154)
U204	HE 443-72	Hex buffer
	HE 434-298	Socket
U205	HE 443-72	Hex buffer
	HE 434-298	Socket
U206	HE 443-1072	Quad 2-input positive OR gate
U207	HE 443-1073	Quad 2-input positive AND gate
U208	Not Avail.	+5 VDC regulator (7805)
Crystal		
Y1	Not Avail.	3.579545 MHz
Wired Keyboard		
	HE 163-21	

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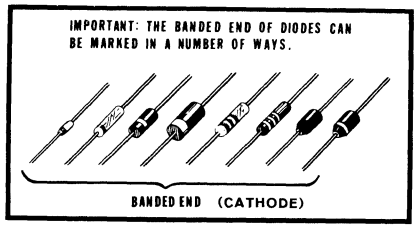
Semiconductor Identification

Semiconductor identification provides assistance with a cross-reference between part numbers and semiconductor part numbers. The part numbers are listed in numerical and then alphanumerical order with replacement part numbers (if available), description and reference designator, and lead configuration in adjacent columns.

PART NUMBER	REPLACEMENT NUMBER	DESCRIPTION	LEAD CONFIGURATION
103-142-01	None	Diode, Video board CR101, CR103, CR113, CR114, CR302, CR303, CR304	
103-252-01	None	Diode, Video board CR112	
103-254-01	None	Diode, Video board CR401	
103-279-23	None	Diode, Video board CRX301	
103-295-03	None	Diode, Video board CR107, CR402	
103-323-03	None	Diode, Video board CR111	



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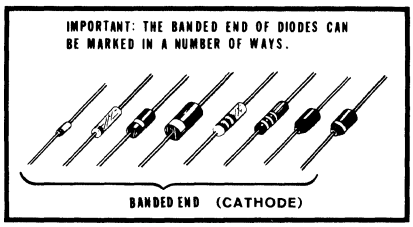
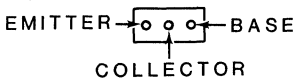
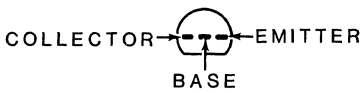
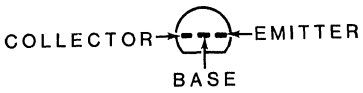
Parts List

PART NUMBER	REPLACEMENT NUMBER	DESCRIPTION	LEAD CONFIGURATION
103-323-04	None	Diode, Video board CR106	
103-339-02	None	Diode, Video board CR109	
103-339-04	None	Diode, Video board CR104	
121-1035	None	Transistor, Video board Q307	
121-1036	None	Transistor, Video board Q306	
121-1040	None	Transistor, Video board Q102, Q304, Q308	
121-1058	None	Transistor, Video board Q109	
121-1070	None	Transistor, Video board Q103	
121-1088	None	Transistor, Video board Q401	

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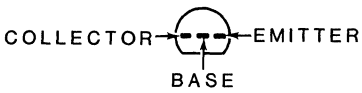
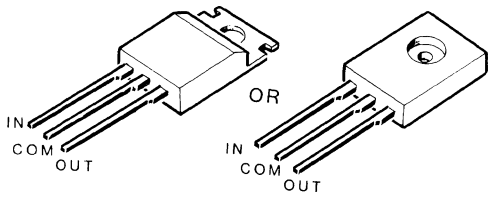
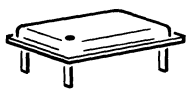
Parts List

PART NUMBER	REPLACEMENT NUMBER	DESCRIPTION	LEAD CONFIGURATION
121-1090	None	Transistor, Video board Q402	
121-1093	None	Transistor, Video board Q108	
121-699	None	Transistor, Video board Q302, Q303	
121-95	None	Transistor, Video board Q101, Q104, Q106, Q107, Q301	
63-789	None	Resistor, Video board CR108	
7805	None	+5 VDC regulator, Keyboard U208	
HE 150-139	None	19.7676 MHz oscillator circuit, TLB Y101	

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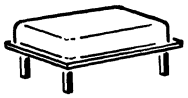
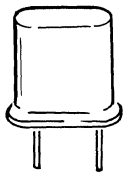
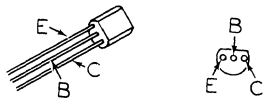
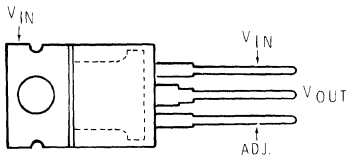
Parts List

PART NUMBER	REPLACEMENT NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 150-140	None	24.8064 MHz oscillator circuit, TLB Y102	
HE 404-659	None	3.6864 MHz crystal, TLB Y100	
HE 417-875	2N3904	Transistor, TLB Q101, Q102	
HE 442-708	LM317	Voltage regulator, TLB U156	

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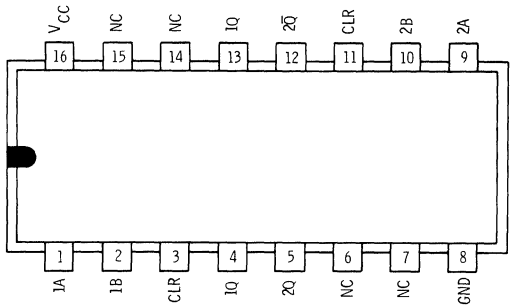
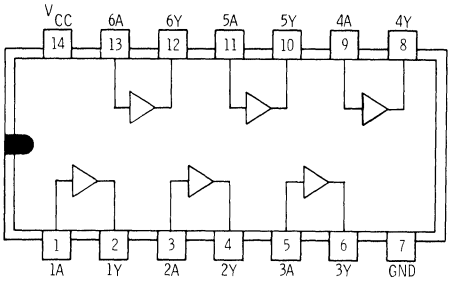
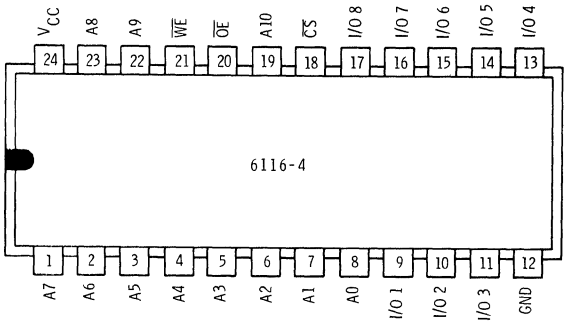
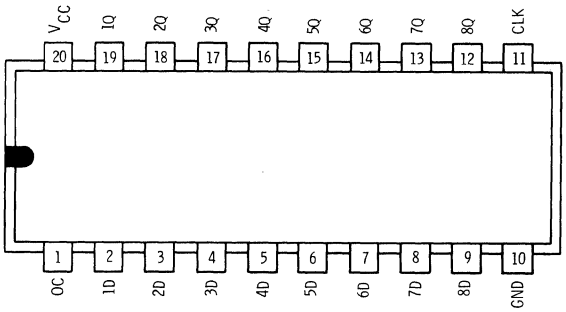
PART NUMBER	REPLACEMENT NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-1008	74LS221	Dual monostable, TLB U152	
HE 443-1020	7407	Hex buffer, TLB U154	
HE 443-1027	6116-P4	RAM 2K × 8, TLB U107, U108, U111, U112, U116, U117	
HE 443-1031	74ALS574	F-F octal D, TLB U151	

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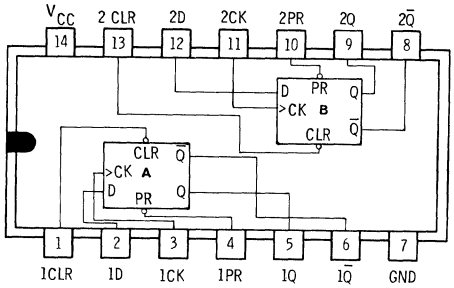
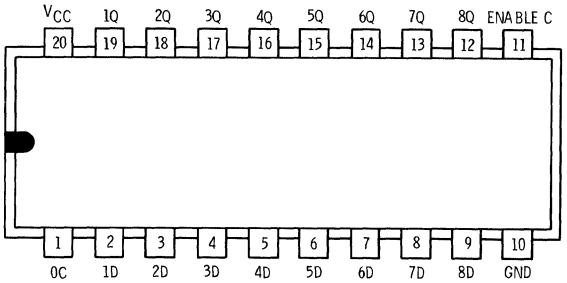
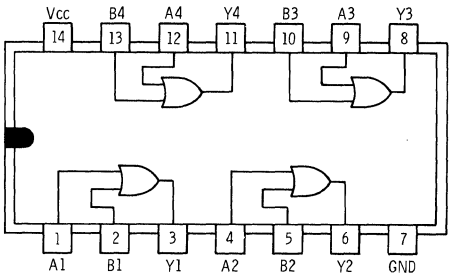
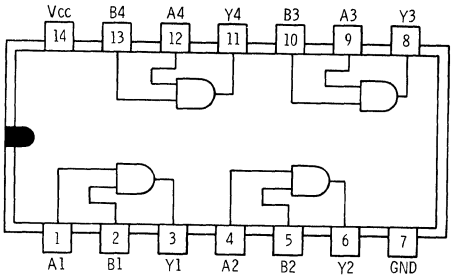
Parts List

PART NUMBER	REPLACEMENT NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-1051	74ALS74	F-F dual D, TLB U133, U136, U148	
HE 443-1070	74ALS573	Transparent latch octal D, TLB U118, U126	
HE 443-1072	74LS32	Quad 2-input OR gate, Keyboard U206 TLB U131, U132, U145	
HE 443-1073	74LS08	Quad 2-input AND gate, Keyboard U205 TLB U134, U137	

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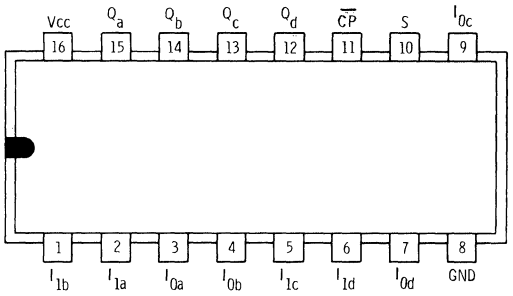
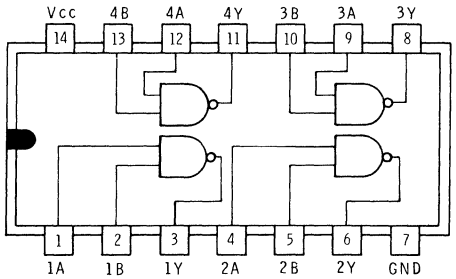
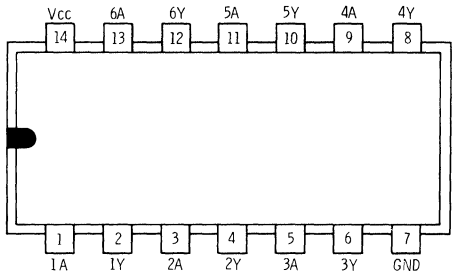
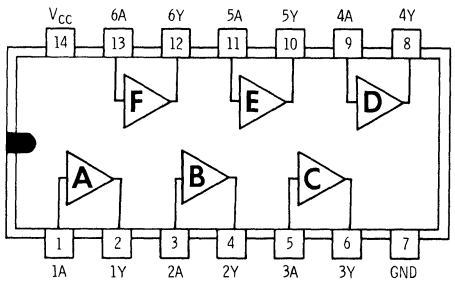
PART NUMBER	REPLACEMENT NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-1103	74LS298	Quad multiplexer, TLB U121	
HE 443-1128	74S03	2-input NAND open collector, TLB U155	
HE 443-1137	74F04	Inverter, TLB U144	
HE 443-72	7417	Hex buffer, Keyboard U204, U205	

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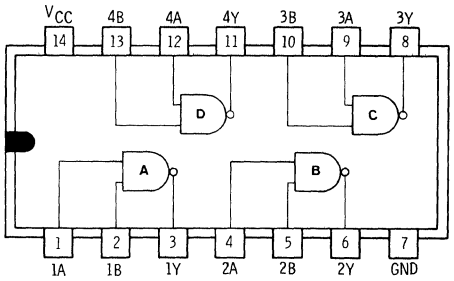
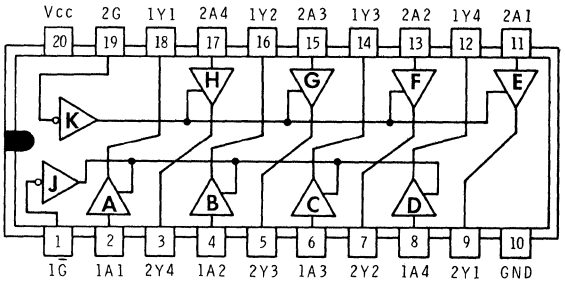
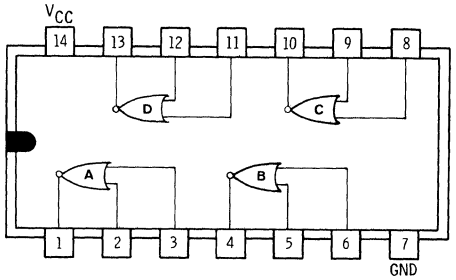
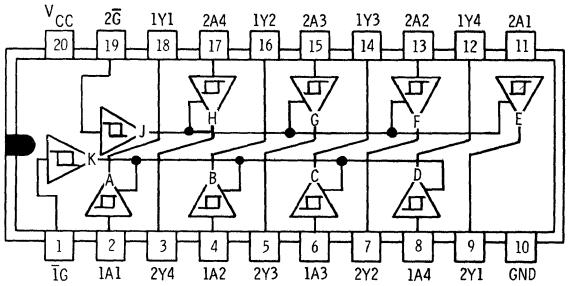
Parts List

PART NUMBER	REPLACEMENT NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-728	74LS00	Quad 2-input NAND gate, TLB U146	
HE 443-755	74LS04	Hex inverter, TLB U135	
HE 443-779	74LS02	Quad 2-input NOR gate, TLB U149	
HE 443-791	74LS244	Tri-state octal buffer, Keyboard U202	

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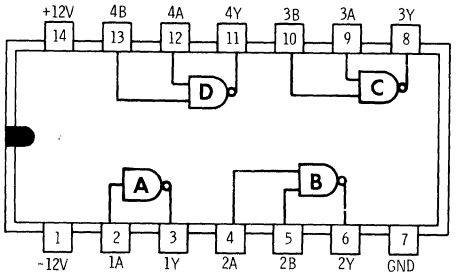
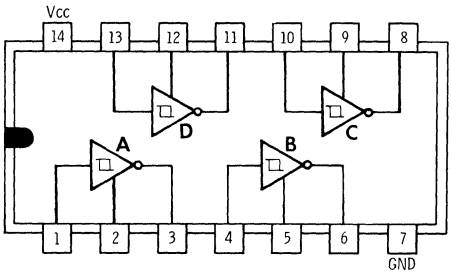
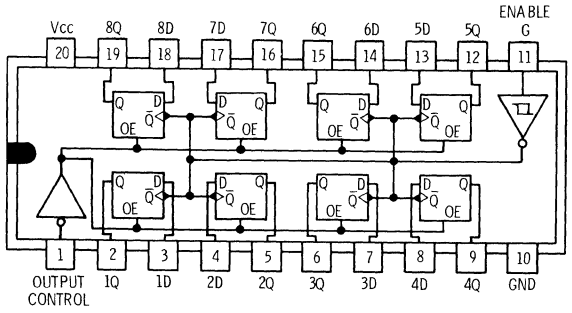
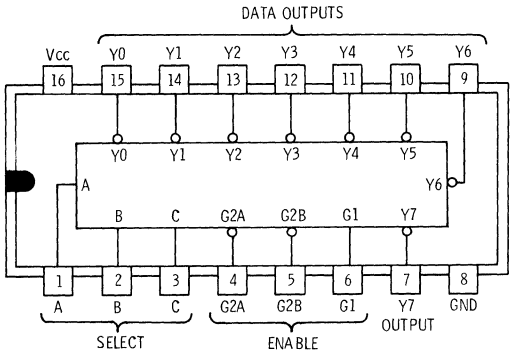
PART NUMBER	REPLACEMENT NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-794	75188	RS-232 driver, TLB U128, U141	
HE 443-795	75189	RS-232 receiver, TLB U123, U153	
HE 443-863	74LS374	F-F octal D tri-state, TLB U101, U106, U124, U125, U129, U130, U138, U139, U142, U143	
HE 443-877	74LS138	Decoder, TLB U127	

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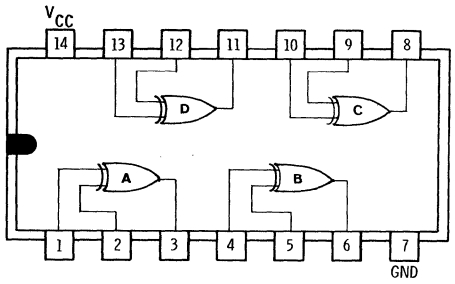
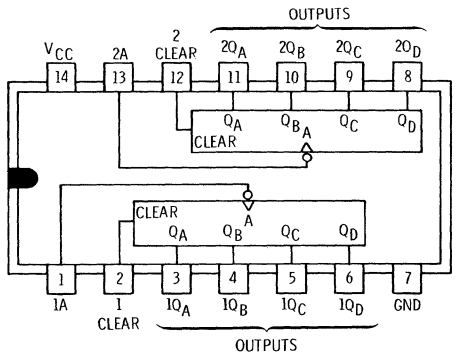
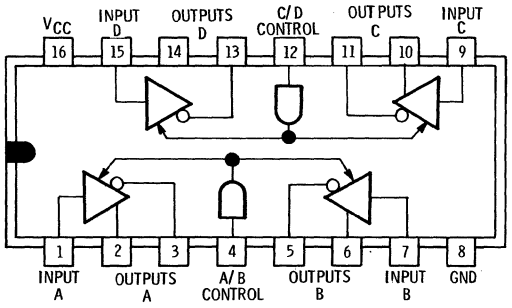
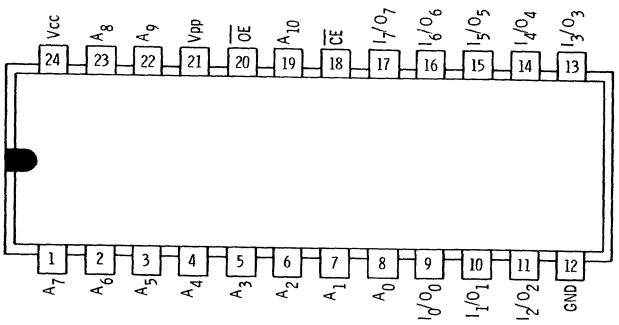
Parts List

PART NUMBER	REPLACEMENT NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-891	74LS86	Quad 2-input XOR, TLB U150	
HE 443-973	74LS393	Binary counter, TLB U147	
HE 443-1167	MC3487	RS-422 Line Driver	
HE 444-193	2816	Non-volatile RAM, TLB U103	

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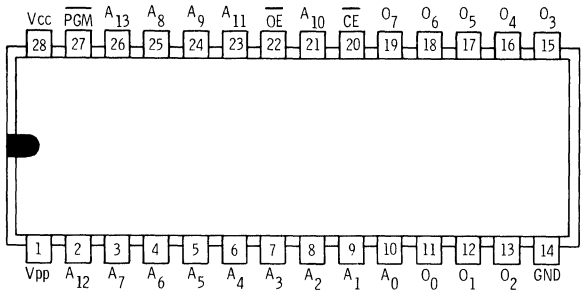
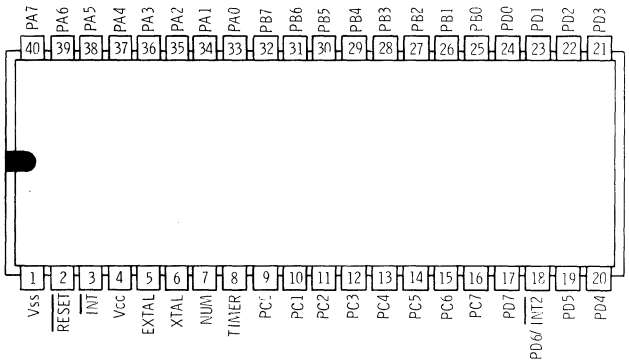
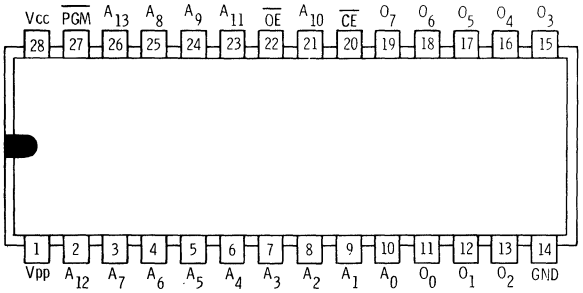
Parts List

PART NUMBER	REPLACEMENT NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 444-210	None	Character ROM, TLB U110	
HE 444-211	None	Keyboard encoder, Keyboard U201	
HE444-212	None	Program ROM, TLB U105	

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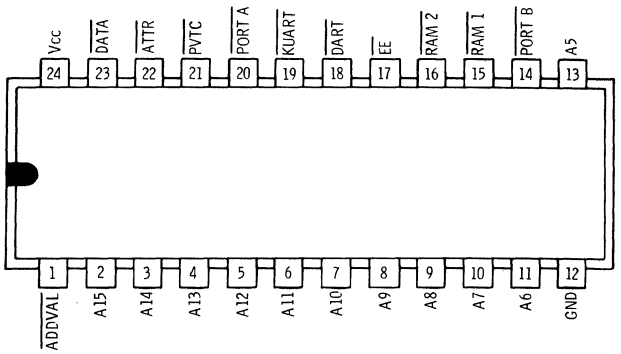
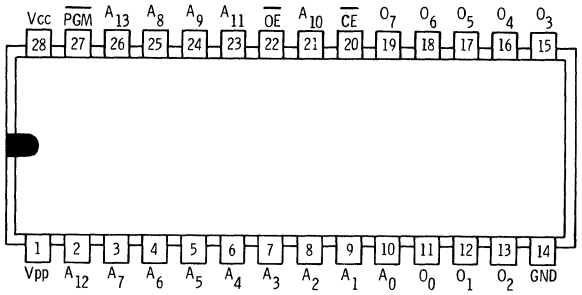
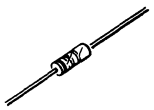
Parts List

PART NUMBER	REPLACEMENT NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 444-213	None	PAL memory select, TLB U109	
HE 444-251	None	Program ROM, TLB U104	
HE 56-56	1N4149	Diode, TLB D108, D109	

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PAL Equation

PAL equations are Boolean expressions where / equals a negated signal, * equals an AND function, and + equals an OR function.

PAL 12L10
HE 444-213
U109 Terminal Logic Board

/DATA = ADDVAL*/A15*A14*A13*A12*A11*A10*A9*A8*A7*A6*A5

/ATTR = ADDVAL*/A15*A14*A13*A12*A11*A10*A9*A8*A7*A6*/A5

/PVTC = ADDVAL*/A15*A14*A13*A12*A11*A10*A9*A8*A7*/A6*A5

/KUART = ADDVAL*/A15*A14*A13*A12*A11*A10*A9*A8*A7*/A6*/A5

/DART = ADDVAL*/A15*A14*A13*A12*A11*A10*A9*A8*/A7*A6*A5

/PORT A = ADDVAL*/A15*A14*A13*A12*A11*A10*A9*A8*/A7*A6*/A5

/PORT B = ADDVAL*/A15*A14*A13*A12*A11*A10*A9*A8*/A7*/A6*A5

/EE = ADDVAL*/A15*A14*/A13*/A12*/A11

/RAM 1 = ADDVAL*/A15*/A14*/A13

/RAM 2 = ADDVAL*/A15*/A14*A13

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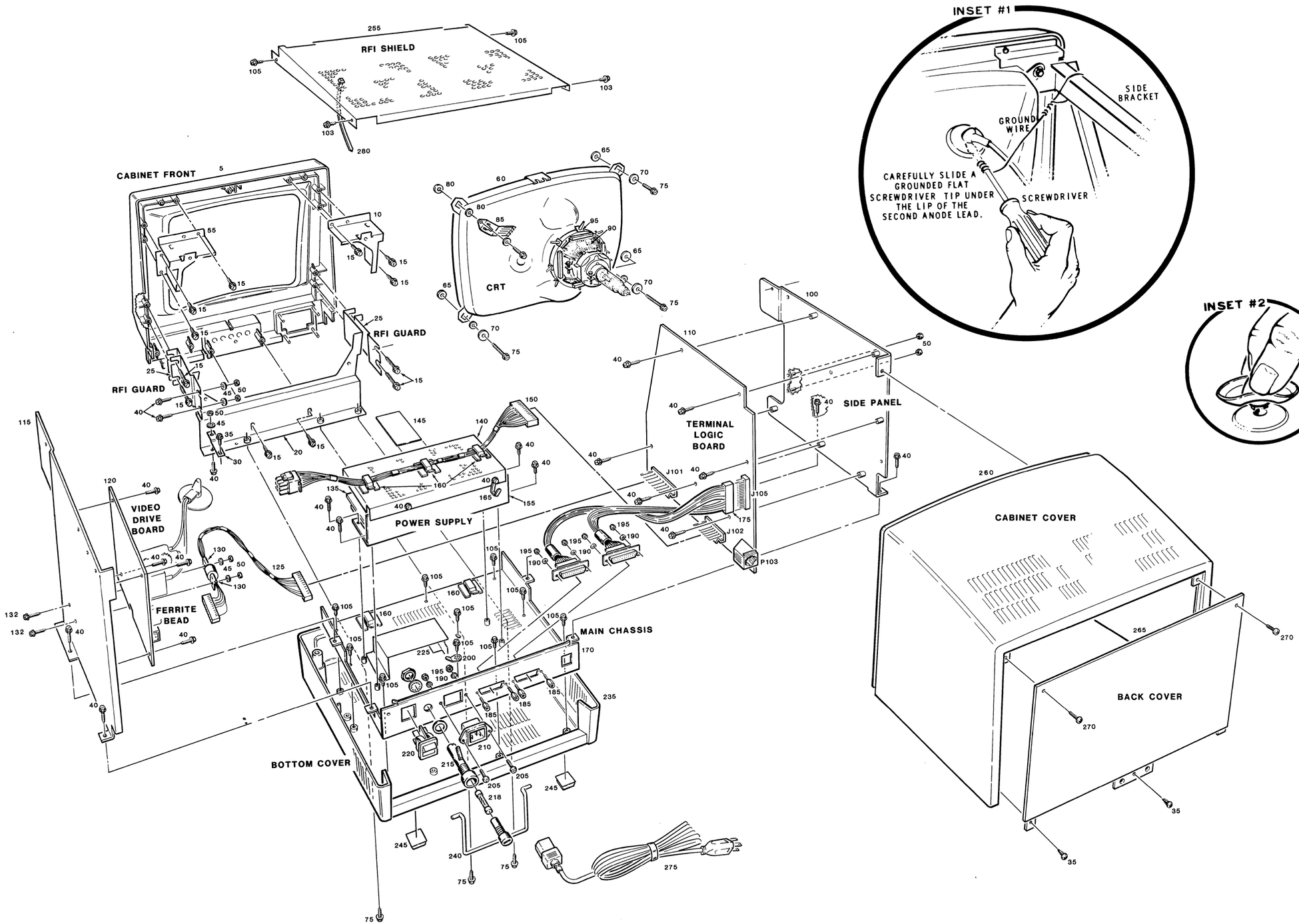

Figure 8.1. Z-49 Video Display Terminal Exploded View

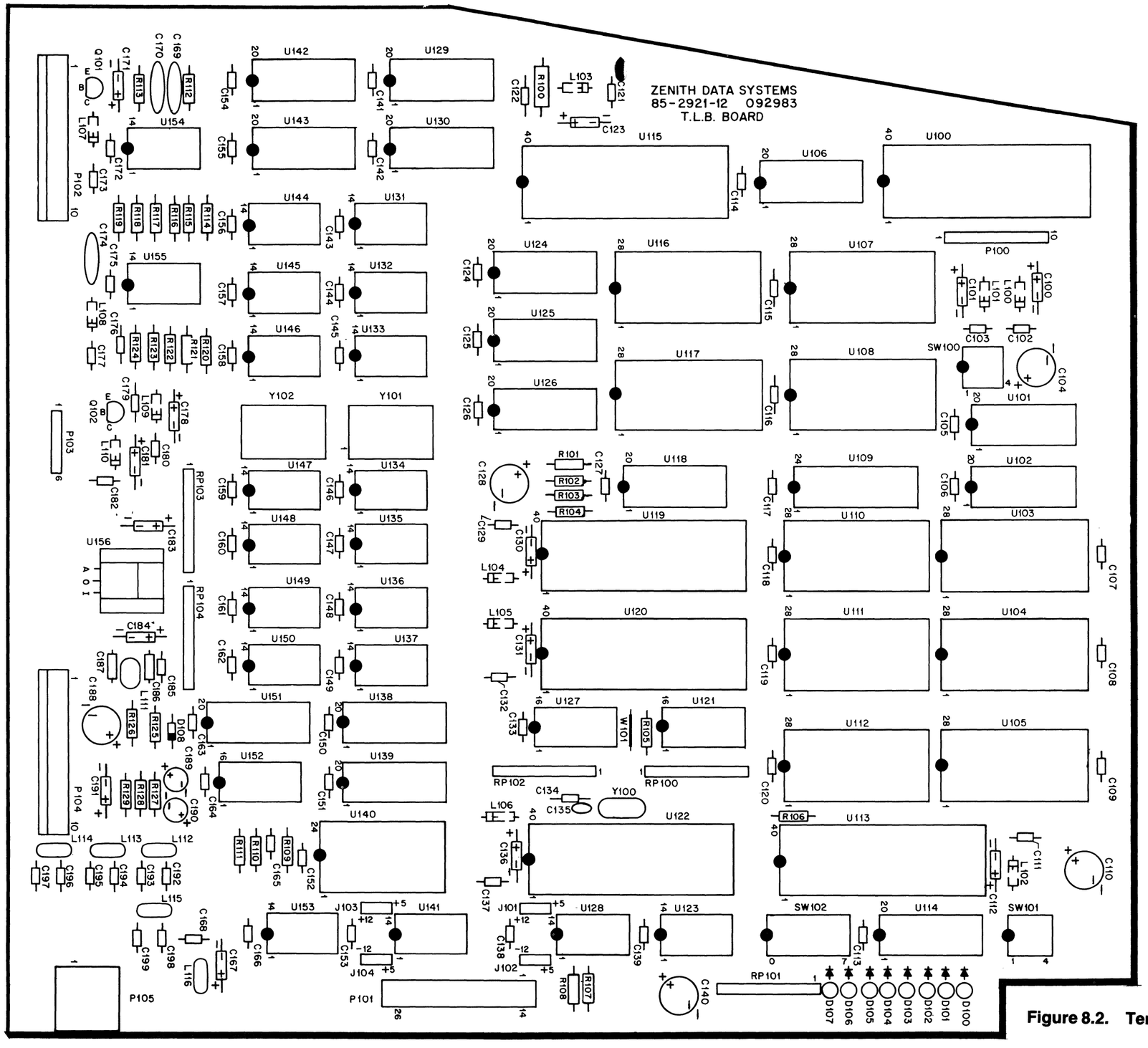

Figure 8.2. Terminal Logic Board Component View

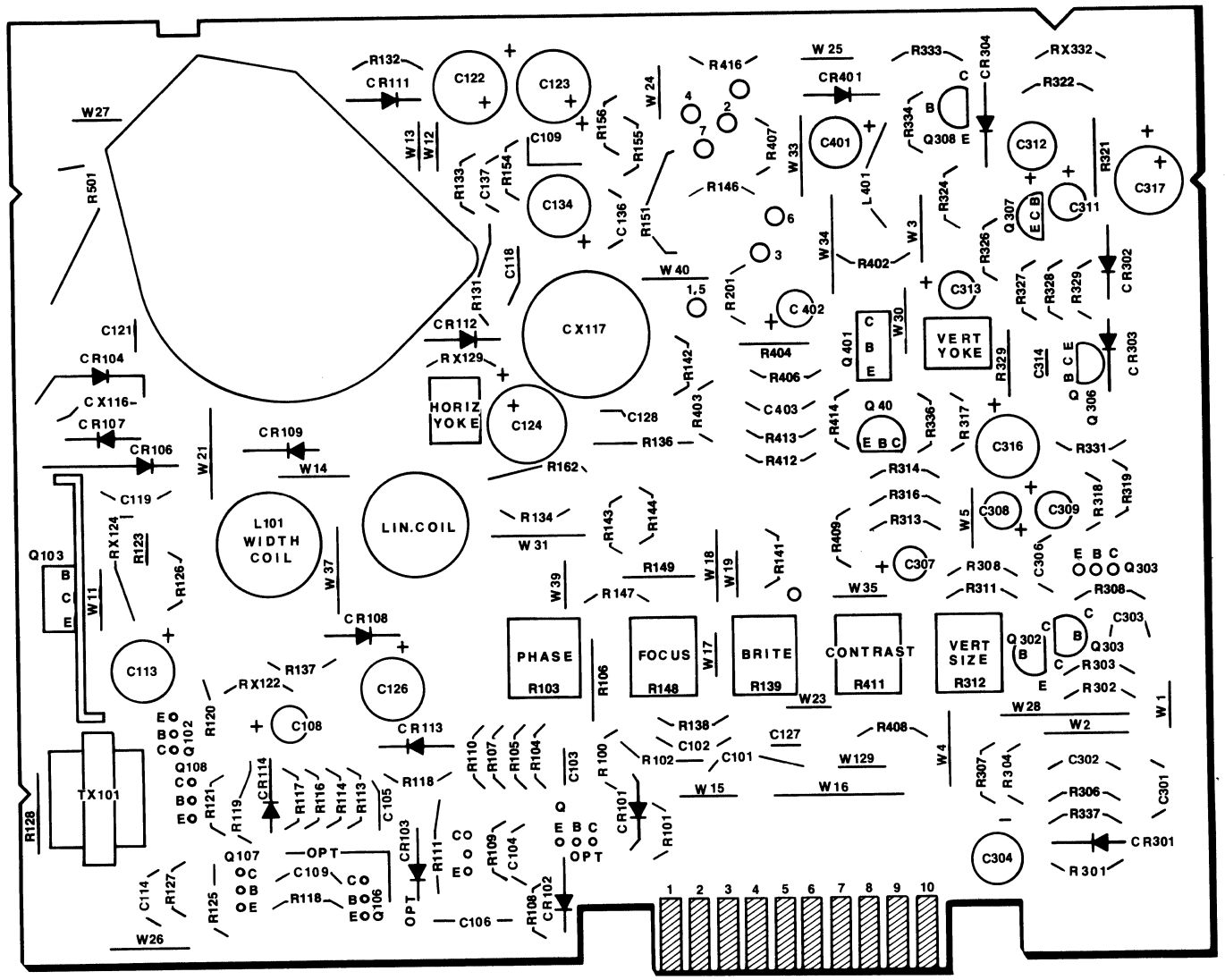

Figure 8.3. Video Circuit Board Component View

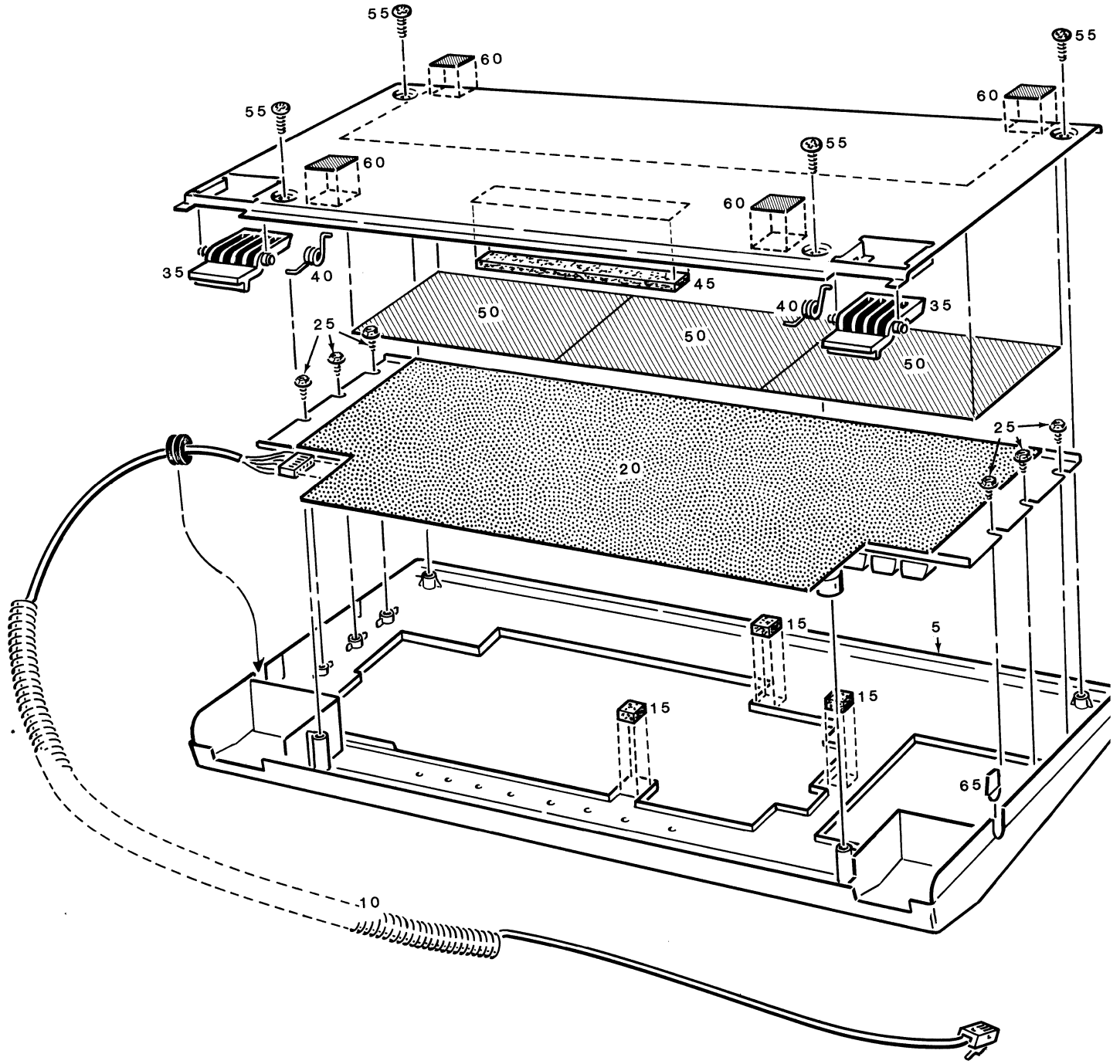

Figure 8.4. Keyboard Exploded View

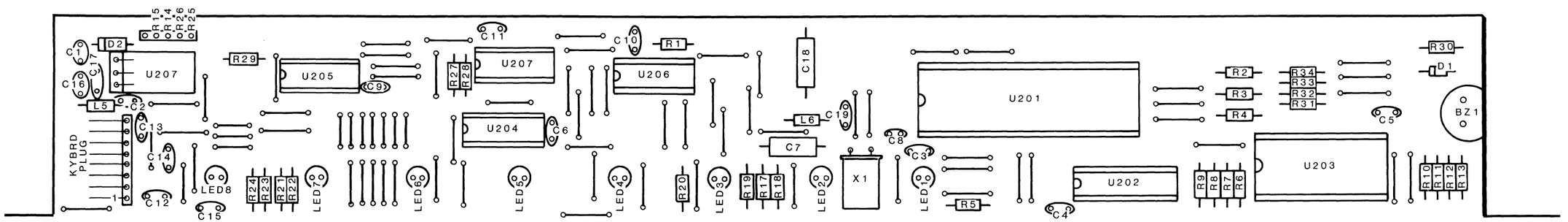

Figure 8.5. Keyboard Component View

Chapter 9

Data Sheets

Introduction

This chapter provides the necessary technical information to understand the PIA, ACIA, DUART, microprocessor, 4-line to 16-line decoder/multiplexer, attributes controller, and video display controller. The following pages are reprinted with the permission of Motorola Inc., Signetics Corporation and Texas Instruments Inc.

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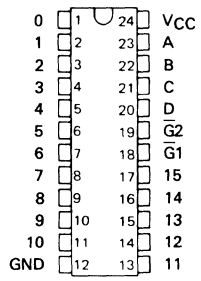
TYPES SN54154, SN54L154, SN74154
4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS

DECEMBER 1972—REVISED DECEMBER 1983

- '154 is Ideal for High-Performance Memory Decoding
- 'L154 is Designed for Power-Critical Applications
- Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Function by Distributing Data From One Input Line to Any One of 16 Outputs
- Input Clamping Diodes Simplify System Design
- High Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with Most TTL and MSI Circuits

SN54154 . . . J OR W PACKAGE
SN54L154 . . . J PACKAGE
SN74154 . . . J OR N PACKAGE

(TOP VIEW)



TYPE	TYPICAL AVERAGE PROPAGATION DELAY 3 LEVELS OF LOGIC	STROBE	TYPICAL POWER DISSIPATION
'154	23 ns	19 ns	170 mW
'L154	46 ns	38 ns	85 mW

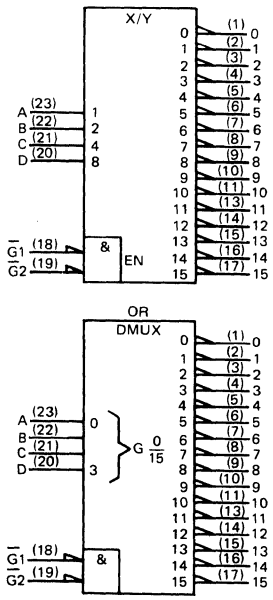
description

Each of these monolithic, 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, $\overline{G1}$ and $\overline{G2}$, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. For ultra-high speed systems, SN54S138/SN74S138 and SN54S139/SN74S139 are recommended.

These circuits are fully compatible for use with most other TTL circuits. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

The SN54154 and SN54L154 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74154 is characterized for operation from 0°C to 70°C.

logic symbol



Pin numbers shown on logic symbols are for J and N packages only.

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TYPES SN54154, SN54L154, SN74154
4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS

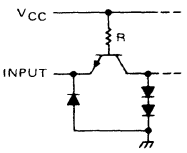
FUNCTION TABLE

INPUTS						OUTPUTS														
$\overline{G1}$	$\overline{G2}$	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

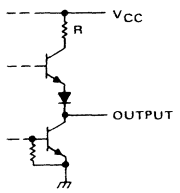
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



'154: R = 6 kΩ NOM
'L154: R = 8 kΩ NOM

TYPICAL OF ALL OUTPUTS



'154: R = 130 Ω NOM
'L154: R = 260 Ω NOM

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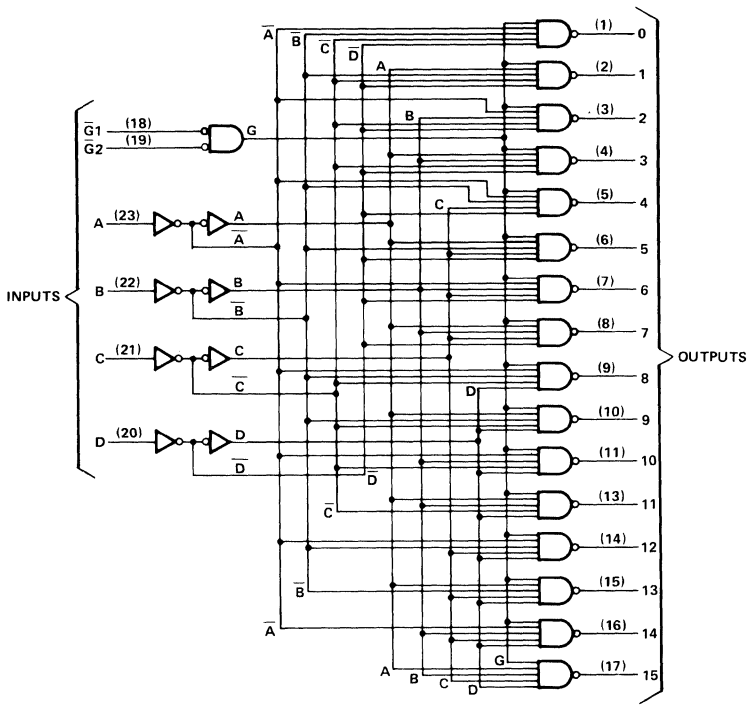
logic diagram



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TYPES SN54154, SN74154
4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54154 Circuits . . . . . −55°C to 125°C
SN74154 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54154			SN74154			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54154			SN74154			UNIT
			MIN	TYP	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−55	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		34	49		34	56	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from A, B, C, or D inputs through 3 levels of logic	C_L = 15 pF, R_L = 400 Ω, See Note 3		24	36	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from A, B, C, or D inputs through 3 levels of logic			22	33	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from either strobe input			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from either strobe input			18	27	ns

NOTE 3: Load circuit and voltage waveforms are shown on page

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TYPE SN54L154
4-LINE TO 16-LINE DECODER/DEMULTIPLEXER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54L154			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−0.4	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54L154			UNIT
		MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −0.4 mA	2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA		0.2	0.4	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−0.8	mA
I_{OS}§	V_{CC} = MAX	−9		−29	mA
I_{CC}	V_{CC} = MAX, See Note 2		17	25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open and all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, C, D	Any	R_L = 800 Ω, C_L = 15 pF		48	72	ns
t_{PHL}					44	66	ns
t_{PLH}	Strobe				40	60	ns
t_{PHL}					36	54	ns

NOTE 3: For load circuits and voltage waveforms, see page ____.

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MICROPROCESSOR DIVISION JANUARY 1983

COLOR/MONOCHROME ATTRIBUTES CONTROLLER (CMAC) SCB2675

Preliminary

DESCRIPTION

The Signetics SCB2675 Color/Monochrome Attributes Controller (CMAC) is a bipolar LSI device designed for CRT terminals and display systems that employ raster scan techniques. It contains a programmable dot clock divider to generate a character clock, a high speed shift register to serialize input dot data into a video stream, latches and logic to apply visual attributes to the resulting display, and logic to display a cursor on the display.

The CMAC provides control of visual attributes on a character by character basis for two operating modes: monochrome and color. The monochrome mode provides reverse video, blank, highlight and two general purpose user definable attributes. In this mode, the display characters can be specified to appear on either a light or dark screen background. Retrace video suppression can be automatically or externally controlled. The color mode provides eight colors for foreground (character) video and eight colors for background video together with a luminance output for external color set selection or to simultaneously drive a monochrome monitor. Additionally, both modes provide double width, underline, blink, dot stretching and dot width attributes. In monochrome mode, the SCB2675 emulates the attribute characteristics of Digital Equipment Corporation's VT100 terminal.

The horizontal dot frequency is the basic timing input to the CMAC. This clock is divided internally to provide a character clock output for system synchronization. Up to ten bits of dot data are parallel loaded into the video shift register on each character boundary. The two TTL video data outputs in monochrome mode are encoded to provide four video intensities (black, gray, white and highlight). The video data in color mode is encoded to provide eight foreground colors and shifted out on three TTL outputs, together with the luminance output.

FEATURES

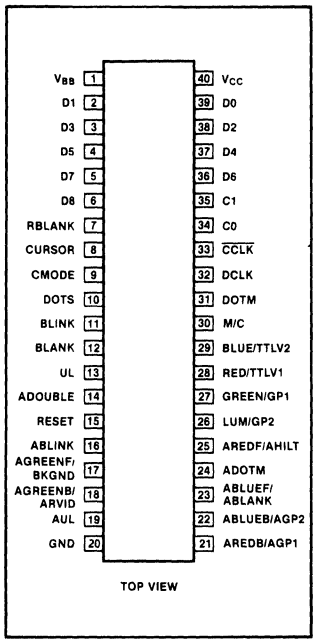
- **25 and 18MHz video dot rate versions***
- **Four video intensities encoded on two TTL outputs (monochrome mode)**
- **Eight foreground and background colors encoded on three TTL outputs (color mode)**
- **Internally latched character attributes:**
  - **Reverse video**
  - **Blank**
  - **Blink**
  - **Underline**
  - **Highlight**
  - **Two general purpose**
  - **Eight foreground colors**
  - **Eight background colors**
  - **Dot width control**
  - **Double width characters**
- **VT100 compatible attributes**
- **Reverse video cursor with optional white cursor in color mode**
- **Up to 10 dots per character**
- **Light or dark background in monochrome mode**
  - **Automatic retrace blanking**
- **Programmable dot stretching**
- **Compatible with SCN2674 AVDC and SCN2670 DCGG**
- **TTL compatible**
- **40-pin dual in-line package**

APPLICATIONS

- **CRT terminals**
- **Word processing systems**
- **Small business computers**

*For faster versions consult factory.

PIN CONFIGURATION



TOP VIEW

ORDERING CODE

PACKAGES	DOTS PER CHARACTER	$V_{CC} = 5V \pm 5\%$, 0°C to +70°C	
		25MHz	18MHz
Ceramic DIP Plastic DIP	7, 8, 9, 10	SCB2675BC5I40 SCB2675BC5N40	SCB2675BC8I40 SCB2675BC8N40
Ceramic DIP Plastic DIP	6, 8, 9, 10	SCB2675CC5I40 SCB2675CC5N40	SCB2675CC8I40 SCB2675CC8N40

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COLOR/MONOCHROME ATTRIBUTES CONTROLLER (CMAC) SCB2675

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PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
V_{CC}	40	I	**Power Supply:** +5VDC
V_{BB}	1	I	**Bias Supply:** See figure 5
GND	20	I	**Ground:** 0V reference
DCLK	32	I	**Dot Clock:** Dot frequency input. Video output shift rate.
$\overline{CCLK}$	33	O	**Character Clock:** An output which is a submultiple of DCLK. The period ranges from 7 to 10 DCLK periods per cycle and is determined by the state of the C0-C1 inputs.
RED/TTLV1	28	O	**Red/TTL Video 1:** In color mode, this output provides the red gun serial video. In monochrome mode, it should be used with the blue/TTL video 2 output to decode four video intensities.
BLUE/TTLV2	29	O	**Blue/TTL Video 2:** In color mode, this output provides the blue gun serial video. In monochrome mode, it should be used with the red/TTL video 1 output to decode four video intensities.
GREEN/GP1	27	O	**Green/General Purpose 1:** In color mode, this output provides the green gun serial video. In monochrome mode, it is a general purpose TTL output which is asserted if the AREDB/AGP1 input is asserted when the corresponding character dot data is loaded into the video shift register.
LUM/GP2	26	O	**Luminance/General Purpose 2:** In color mode, this output is the logical-OR of the RGB foreground video. It is low during a blanking interval and during the foreground portion of the cursor display. In monochrome mode, it is a general purpose TTL output which is asserted if the ABLUEB/AGP2 input is asserted when the corresponding character dot data is loaded into the video shift register.
UL	13	I	**Underline Timing:** Indicates the scan line(s) for the underline attribute. Latched on the falling edge of BLANK.
BLINK	11	I	**Blink Timing:** This input is sampled on the falling edge of BLANK to provide the blink rate for the blink attribute. Should be a submultiple of the frame rate.
BLANK	12	I	**Screen Blank:** When high, this input forces the video outputs to the specified background color in color mode and to the level specified by the BKGND input (either black or gray) in monochrome mode.
RBLANK	7	I	**Retrace Blank:** This input is used to force the video outputs to a low during retrace periods. If pulled high, it will automatically suppress video during the retrace periods when BLANK is high. The user may also pulse this input while BLANK is high to selectively suppress raster video.
AGREENF/BKGND	17	I	**Green Foreground/Background Intensity:** In color mode, this input activates the GREEN/GP1 output during the foreground (character video) portion of the associated character block. In monochrome mode, this input specifies gray or black screen background.
ABLUEF/ABLANK	23	I	**Blue Foreground/Blank Attribute:** In color mode, this input activates the BLUE/TTLV2 output during the foreground (character video) portion of the associated character block. In monochrome mode, this input generates a blank space for the associated character. The blank space intensity is controlled by the AGREENF/BKGND input, the reverse video attribute and cursor input.
AREDF/AHILT	25	I	**Red Foreground/Highlight Attribute:** In color mode, this input activates the RED/TTLV1 output during the foreground (character video) portion of the associated character block. In monochrome mode, this input highlights the associated character (including underline).
CURSOR	8	I	**Cursor Timing:** This input provides the timing for the cursor video. In color mode, with CURSOR and CMODE high, the RGB outputs are driven high (white cursor). If CMODE is low, or in monochrome mode, this input reverses the intensities of the video and attributes. Cursor position, shape, and blink rate are controlled by this input.
CMODE	9	I	**Cursor Mode:** Used in color mode only. When CURSOR and CMODE are high, the RGB outputs are driven high (white cursor). When CURSOR is high and CMODE is low, the RGB outputs are logically inverted (reverse video cursor).
AUL	19	I	**Underline Attribute:** Specifies a line to be displayed in the character block. The specific line(s) are specified by the UL input. All other attributes apply to the underline video.

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PIN DESIGNATION (Continued)

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
ABLINK	16	I	**Blink Attribute:** In color mode, this active high input will drive the foreground RGB combination to the background RGB combination. In monochrome mode, the associated character or background is driven to the intensity determined by BKGND, reverse video attribute and the cursor input.
ADOUBLE	14	I	**Double Width Attribute:** This active high input causes the associated character video to be shifted out of the serial shift register at one half the dot frequency (DCLK). The $\overline{CCLK}$ output is not affected.
AREDB/AGP1	21	I	**Red Background/General Purpose Attribute 1:** In color mode, this input activates the RED/TTLV1 output during the background portion of the associated character block. In monochrome mode, it activates the GREEN/GP1 output for the associated character block.
ABLUEB/AGP2	22	I	**Blue Background/General Purpose Attribute 2:** In color mode, this input activates the BLUE/TTLV2 output during the background portion of the associated character block. In monochrome mode, it activates the LUM/GP2 output for the associated character block.
AGREENB/ARVID	18	I	**Green Background/Reverse Video Attribute:** In color mode, this input activates the GREEN/GP1 output during the background portion of the associated character block. In monochrome mode, it causes the associated character block video intensities to be reversed.
D0-D8	36-39, 2-6	I	**Dot Data Input:** These are parallel inputs corresponding to the character/graphic symbol dot data for a given scan line. These inputs are strobed into the video shift register on the trailing (falling) edge of each character clock ($\overline{CCLK}$).
C0-C1	34-35	I	**Character Clock Control:** The states of these two static inputs determine the internal divide factor for the $\overline{CCLK}$ output rate.
RESET	15	I	**Reset:** This active high input initializes the internal logic and resets the attribute latches.
M/C	30	I	**Monochrome/Color Mode:** This input selects whether the CMAC operates in monochrome or color mode. A low selects color mode and a high selects monochrome mode.
ADOTM	24	I	**Dot Modulation Attribute:** When DOTM and this input are high, the active dot width of the associated character video is one DCLK. When DOTM is high and this input is low, the active dot width of the associated character video is two DCLKs.
DOTM	31	I	**Dot Width Modulation:** When this input is high, two DCLKs are used for each dot shifted through the shift register. When this input is low, one DCLK is used.
DOTS	10	I	**Dot Stretching:** Sampled at the falling edge of BLANK. When this input is high, one extra dot is appended to individual dots or groups of dots of the input parallel data and then transferred through the shift register. When this input is low, normal transfer of input parallel data results.

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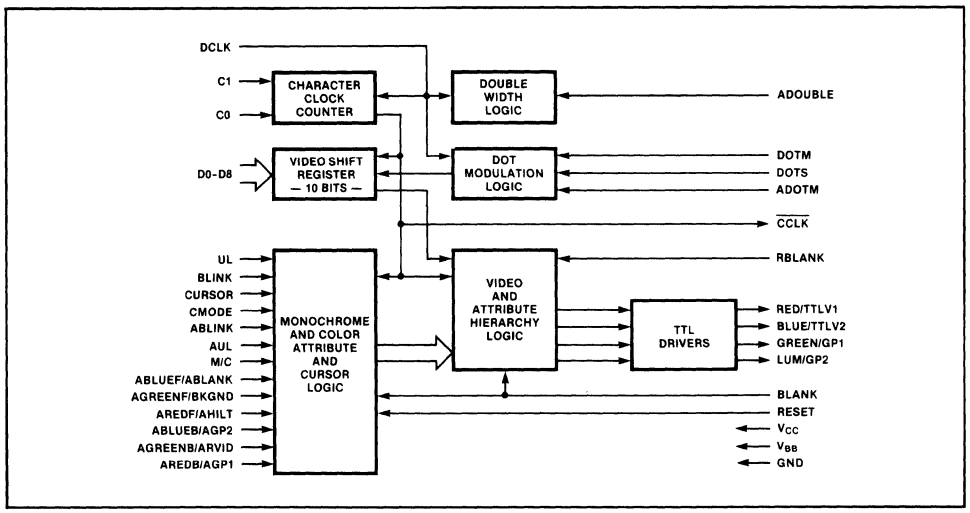
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The CMAC consists of seven major sections (see block diagram). The high speed dot clock input is applied to a programmable divider to provide a character clock output for system timing. Parallel dot data is loaded into the video shift register on character boundaries and shifted into the video logic block at the dot rate specified by the dot modulation section. The appropriate attribute control inputs are selected by the mode select logic, latched internally on character boundaries, and combined with the serial dot data to provide monochrome or color video outputs.

The BLANK input defines the active screen area. In color mode, the video outputs are forced to the specified background color when this signal is asserted; in monochrome mode the video outputs are forced to the states defined by the BKGND input, i.e., black if dark background is selected and gray if light background is selected. A separate RBLANK input allows the user to select the amount of border around the active area when operating in color mode or in monochrome mode with light background. This input can be tied high, in which case the area outside the active area will be dark, or it may be pulsed during BLANK periods to externally control the border widths.

In color mode, eight colors for the character (foreground) and eight colors for the background (area other than character) can be selected by the attribute inputs. In monochrome mode, the intensities of foreground and background are a function of the attribute and BKGND inputs, i.e., characters may be black, gray, white, or highlight (very white) while background may be black, gray, or white (see Table 1).

Table 1 MONOCHROME MODE ATTRIBUTE CHARACTERISTICS

REV[1]	AHILT	ABLINK[2]	FOREGROUND VIDEO	BACKGROUND VIDEO
0	0	0	W	B
0	0	1	W/G	B
0	1	0	H	B
0	1	1	H/W	B
1	0	0	B	G
1	0	1	B/W	G/B
1	1	0	B	W
1	1	1	B/H	W/B

NOTES

1. REV = (BKGND) XOR (ARVID):

BKGND	ARVID	REV
0	0	0
0	1	1
1	0	1
1	1	0

2. For blinking, the video outputs are shown as 0/1, where 0 and 1 are the blink timing input states.
3. Foreground includes underline when underlining is specified by AUL = 1.
4. When ABLANK = 1, foreground component becomes same as background component.
5. Codes for video outputs are as follows:

CODE	TTLV2	TTLV1	BEAM INTENSITY
B	0	0	Black
G	0	1	Gray
W	1	0	White
H	1	1	Highlight

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Character Clock Counter

The character clock counter divides the DCLK input to generate the character clock ($\overline{CCLK}$). The divide factor is specified by the clock control inputs (C1-C0) as follows:

C1	C0	SCB2675B	
		DOTS/ CHAR.	$\overline{CCLK}$ DUTY CYCLE*
0	0	10	5/5
0	1	7	4/3
1	0	8	4/4
1	1	9	5/4

*High/low

C1	C0	SCB2675C	
		DOTS/ CHAR.	$\overline{CCLK}$ DUTY CYCLE*
0	0	10	5/5
0	1	6	3/3
1	0	8	4/4
1	1	9	5/4

*High/low

The number of dot clocks/character is normally the number of dots/character as listed above. However, when dot width control is specified, the DCLK input is divided by two before it is applied to the character clock counter resulting in the number of dot clocks/character being double those listed above, although the number of displayed dots/character remains the same. See Dot Modulation section of this data sheet.

Video Shift Register

On each character boundary, the parallel input dot data (D0-D8) is loaded into the video shift register. The data is shifted out least significant bit first (D0) at the DCLK rate. If 10 dots/character are specified (C1-C0 = 00), the tenth dot will be the same as D8. The serial dot data from the video shift register is routed to the video logic where it is combined with the cursor and attribute control bits to produce the video data outputs.

Mode Select, Attribute and Cursor Control

The mode select logic multiplexes the monochrome and color attribute inputs and outputs as specified by the M/C input. The monochrome mode provides blank, reverse video, highlight and two general purpose attributes. The latter may be used, with external logic, to combine other attributes (e.g., overscore) into the video stream. The color mode provides RGB foreground and background color attributes. Both modes provide double width characters, blink, underline, dot width control and dot stretching.

The cursor and attribute inputs are pipelined internally to allow for system pipeline propagations. The cursor input signal is delayed internally by two $\overline{CCLK}$s (one for RAM and one for the character generator), while the attribute inputs are delayed for one $\overline{CCLK}$ to account for the delay of the character data through the character generator latches. The attribute timing inputs (BLINK, UL and DOTS) are clocked into the 2675 at the beginning of each scan line time by the falling edge of BLANK. Thus, these inputs must be in their proper state at the falling edge of BLANK preceding the scan line where they are required to be active. The BLANK signal itself is also delayed internally to provide for the RAM and character generator delays (see figures 6 and 7). Internal delays cause the video outputs to be delayed relative to $\overline{CCLK}$ as illustrated in figure 8.

Video Logic

Each character block consists of the three components shown in figure 1. Symbol video is generated from the dot data inputs D0-D8. Underline video is enabled by the AUL attribute and is generated during the scan lines for which the UL input is active. Underline and symbol video are always the same intensity or color, and other attributes (e.g., ABLINK) apply to them equally. The combination of underline and symbol video is also referred to as foreground video. Background video is the area of the character block corresponding to the absence of foreground video. The assertion of the non-display attribute (ABLANK) causes the entire character block to be displayed as background.

In monochrome mode, the serial dot data and pipelined cursor and attributes are combined to generate four video intensities (black, gray, white and highlight) which are encoded on the TTLV1 and TTLV2 outputs as follows:

TTLV2	TTLV1	VIDEO INTENSITY
0	0	Black
0	1	Gray
1	0	White
1	1	Highlight

Table 1 describes the relationship between attributes and video intensity of the foreground and background components of the character block in monochrome mode.

In color mode, the colors of the foreground and background components are specified by the corresponding attribute inputs; AREDF, AGREENF and ABLUEF dictate the color of the foreground component while AREDB, AGREENB and ABLUEB do the same for the background component. In this mode, the serial dot data and pipelined cursor and attributes are combined to generate four video outputs. The RED, GREEN and BLUE outputs separately contain the corresponding foreground and background components. The LUM output is the logical-OR of the foreground colors and can be used to drive a separate monochrome monitor or to select a different set of colors for the foreground.

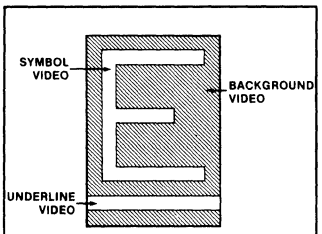

Figure 1. Character Block Definition

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Dot Modulation Logic

The dot modulation logic controls the video shift register to supply dot stretching and dot width control.

Dot stretching is controlled by the DOTS input which is sampled each scan line at the trailing (falling) edge of BLANK. If DOTS is asserted at that time, all characters on the following scan line will have dot stretching applied. Dot stretching causes an extra dot to be added to individual dots or groups of dots as shown in figures 2 and 3. Dot stretching can be used to:

1. Compensate for low video bandwidth monitors (since the minimum active displayed segment with dot stretching is two DCLKs).
2. Assure crisp black characters when operating in white background mode.
3. Provide thick characters as a means of distinguishing areas of the display.

Dot width is controlled by the DOTM and ADOTM inputs. DOTM is tied either high, which enables the feature on the entire display, or low, which disables the feature. With ADOTM high, the dot width of characters can be selectively controlled by assertion of the ADOTM attribute input. When operating in this mode, the dot clock input is divided by two before being applied to other circuits in the CMAC. This affects the $\overline{CCLK}$ output.

When dot width control is enabled as above, two DCLKs are used for each video dot period. Asserting ADOTM for a particular character will cause each active video dot of the displayed character to be turned on for one DCLK and off for the other DCLK, while if ADOTM is negated for that character, the active video dot for that character will be turned on (black background) or off (white background) for both DCLK times (see figures 2 and 4). Only the character video component of the character block is modulated. Underline video and background are not affected by on-time modulation. Width control can be used to:

1. Make horizontal lines and vertical lines appear the same brightness on the display.
2. Provide two different brightness levels for characters without requiring a monitor with analog brightness inputs.

However, note that the effects produced by this feature are highly dependent on the video amplifier characteristics of the monitor used.

Double Width Logic

The double width logic controls the rate at which dots are shifted through the video shift register. When the ADOUBLE input is asserted, the associated character video will be shifted at one half the DCLK rate, and the dot information for the next character will be loaded into the shift register two $\overline{CCLK}$s later. The $\overline{CCLK}$ output is not affected. If a double width character is specified at the last location of a character row, the second half of the double width character (one $\overline{CCLK}$) will extend into the horizontal front porch.

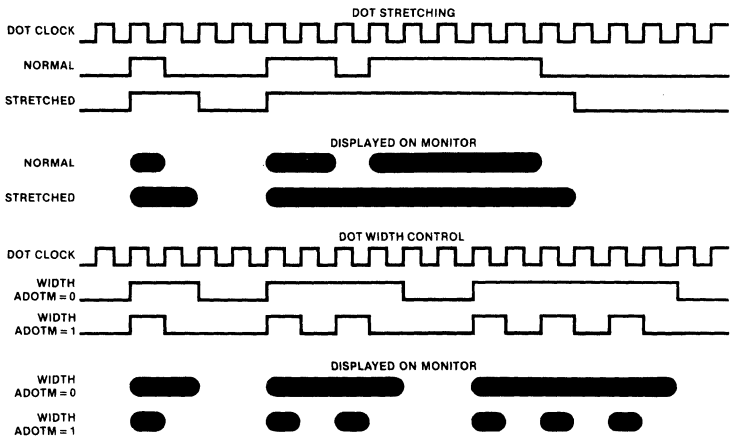

Figure 2. Dot Modulation Timing

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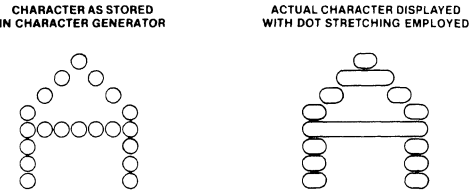

Figure 3. Dot Stretching

Figure 4. Dot Width Control

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	−65 to +150	°C
All voltages with respect to ground[3]	−0.5 to +6.0	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, V_{BB} = figure 5[4,5,6]

PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage		2.0			V
V_{OL}	Output low voltage	$I_{OL} = 4mA$			0.4	V
V_{OH}	Output high voltage	$I_{OH} = -400\mu A$	2.4			V
I_{IL}	Input low current	$V_{IN} = 0.4V$				
	DCLK				−800	μA
	All other inputs				−400	μA
I_{IH}	Input high current	$V_{IN} = 2.4V$				
	DCLK				40	μA
	All other inputs				20	μA
I_{CC}	V_{CC} supply current	$V_{IN} = 0V$, V_{CC} = max			80	mA
I_{BB}	V_{BB} supply current	Figure 5			120	mA

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AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, V_{BB} = figure 5[4,5,6]

PARAMETER		TEST CONDITIONS	TENTATIVE LIMITS				UNIT
			25MHz VERSION		18MHz VERSION		
			Min	Max	Min	Max	
Dot clock timing[7]							
f_D	Frequency			25		18	MHz
t_{DH}	High time		15		22		ns
t_{DL}	Low time		15		22		ns
Setup times[8]							
t_{SB}	BLANK to $\overline{CCLK}$		40		50		ns
t_{SA}	Attributes to $\overline{CCLK}$		40		50		ns
t_{SD}	D0-D9 to $\overline{CCLK}$		60		70		ns
t_{SK}	CURSOR to $\overline{CCLK}$		40		50		ns
t_{SC}	C0, C1 to DCLK		20		20		ns
t_{SR}	RBLANK to DCLK		20		20		ns
t_{SM}	BLINK, UL, DOTS to BLANK		20		20		ns
Hold times[8]							
t_{HB}	BLANK from $\overline{CCLK}$		20		20		ns
t_{HA}	Attributes from $\overline{CCLK}$		20		20		ns
t_{HD}	D0-D8 from $\overline{CCLK}$		30		30		ns
t_{HK}	CURSOR from $\overline{CCLK}$		20		20		ns
t_{HC}	C0, C1 from DCLK		20		20		ns
t_{HR}	RBLANK from DCLK		20		20		ns
t_{HM}	BLINK, UL, DOTS from BLANK		20		20		ns
Delay times[7]		$C_L = 50pF$					
t_{DC}	$\overline{CCLK}$ from DCLK			55		70	ns
t_{DV}	Other outputs from DCLK		30	60	35	70	ns

NOTES
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying voltages greater than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground. For testing, all input signals swing between 0.4V and 2.4V with a transition time of 3ns maximum. All time measurements are referenced at input voltages of 0.8V and 2.0V and at output voltages of 0.8V and 2.0V as appropriate.
6. Typical values are at +25°C, typical supply voltages and typical processing parameters.
7. See figure 8.
8. See figures 6, 7, 9, and 10.

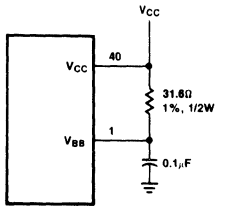

Figure 5.
Recommended V_{BB} Test Circuit

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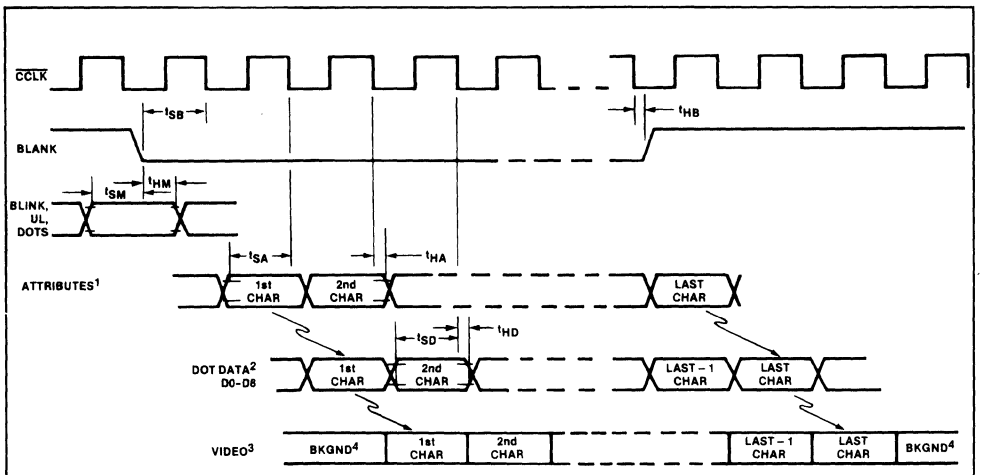

NOTES:
1. Attributes include: ABLINK, ABLANK, ARVID, AUL, AHILT, ADOUBLE, ADOTM, two general purpose, and foreground/background colors.
2. One $\overline{CCLK}$ delay for dot data (obtained from delay through character generator).
3. See figure 8 for detail timing of video outputs.
4. Non-active scan time. VIDEO reverts to polarity selected by the BKGND input in monochrome mode.

Figure 6. CMAC Pipeline Timing

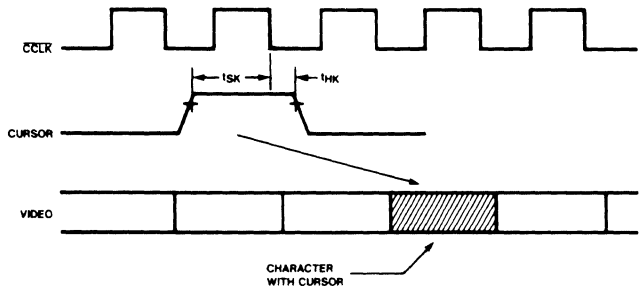

Figure 7. Cursor Pipeline Timing

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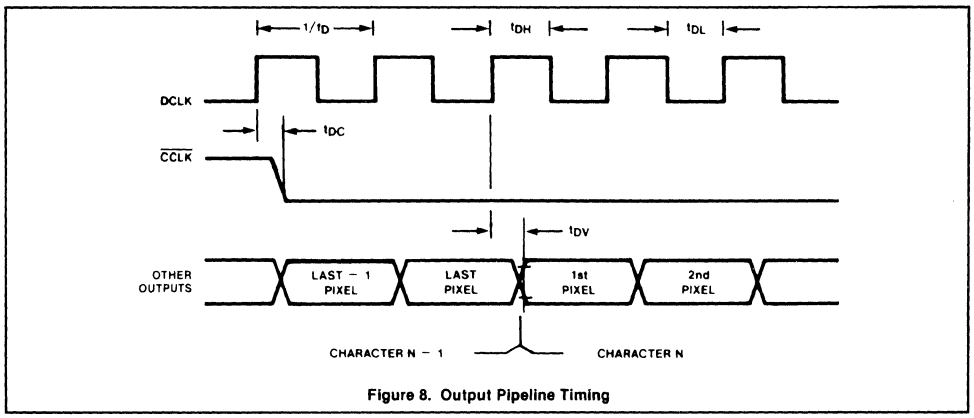


Figure 8. Output Pipeline Timing

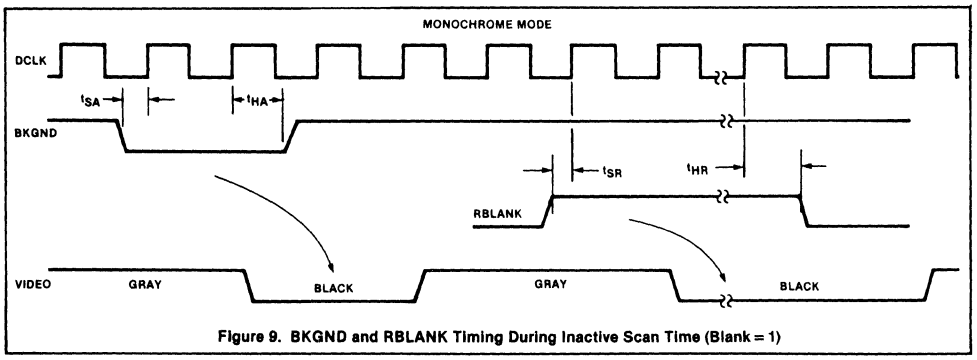
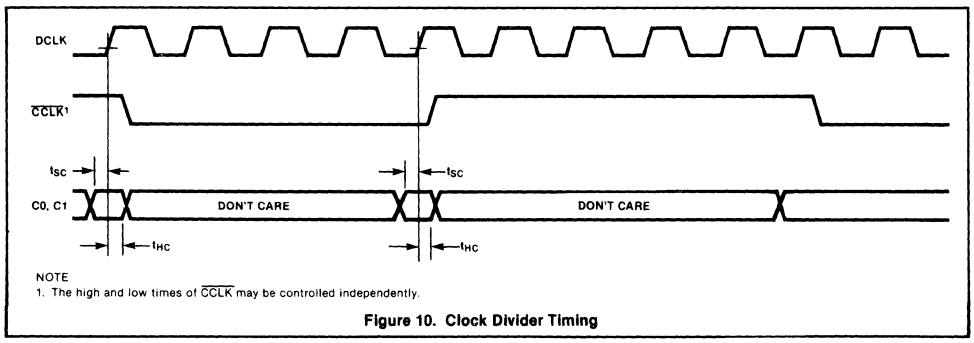


Figure 9. BKGND and RBLANK Timing During Inactive Scan Time (Blank = 1)



NOTE
1. The high and low times of $\overline{CCLK}$ may be controlled independently.

Figure 10. Clock Divider Timing

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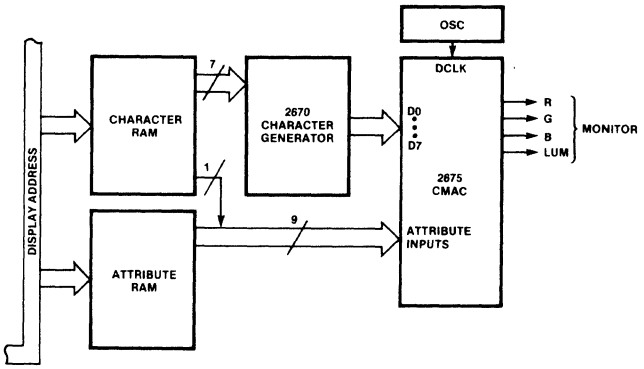

Figure 11. System Block Diagram of SCB2675 in Color Mode

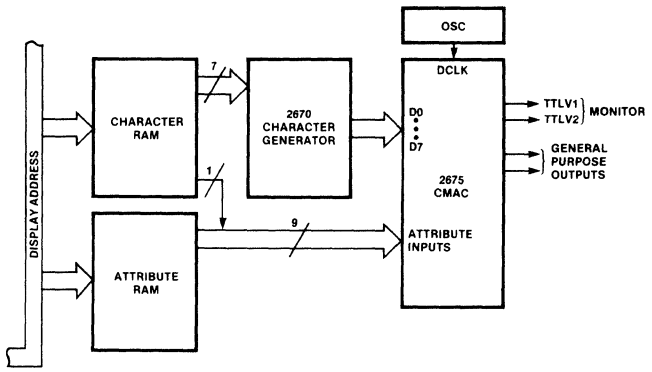

Figure 12. System Block Diagram of SCB2675 in Monochrome Mode

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MICROPROCESSOR DIVISION JANUARY 1983

ADVANCED VIDEO DISPLAY CONTROLLER (AVDC) SCN2674

Preliminary

DESCRIPTION

The Signetics SCN2674 Advanced Video Display Controller (AVDC) is a programmable device designed for use in CRT terminals and display systems that employ raster scan techniques. The AVDC generates the vertical and horizontal timing signals necessary for the display of interlaced or non-interlaced data on a CRT monitor. It provides consecutive addressing to a user specified display buffer memory domain and controls the CPU-display buffer interface for various buffer configuration modes. A variety of operating modes, display formats, and timing profiles can be implemented by programming the control registers in the AVDC.

A minimum CRT terminal system configuration consists of an AVDC, an SCN2671 Keyboard and Communication Controller (PKCC), an SCN2670 Display Character and Graphics Generator (DCGG), an SCB2675 Color/Monochrome Attributes Controller (CMAC), a single chip microcomputer such as the 8048, a display buffer RAM, and a small amount of TTL for miscellaneous address decoding, interface, and control. Typically, the package count for a minimum system is between 15 and 20 devices; system complexity can be enhanced by upgrading the microprocessor and expanding via the system address and data busses.

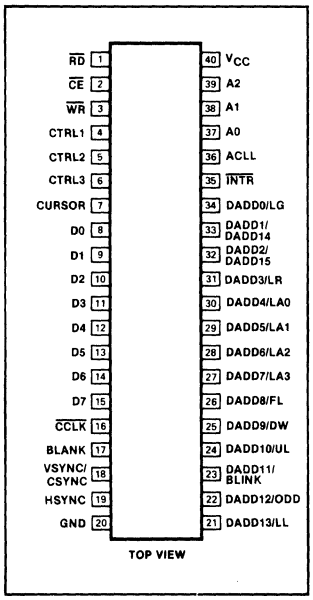
FEATURES

- 4MHz character rate
- 1 to 256 characters per row
- 1 to 16 raster lines per character row
- 1 to 128 character rows per frame
- Bit mapped graphics mode
- Programmable horizontal and vertical sync generators
  - RS170 compatible sync
- Interlaced or non-interlaced operation
- Up to 64K RAM addressing for multiple page operation
- Readable, writable and incrementable cursor
  - Programmable cursor size and blink
- AC line lock
- Automatic wraparound of RAM
- Automatic split screen
- Automatic bidirectional soft scrolling
  - Programmable scan line increment
- Row table addressing mode
- Double height tops and bottoms
- Double width control output
- Selectable buffer interface modes
- Dynamic RAM refresh
- Completely TTL compatible
- Single +5 volt power supply
- Power on reset circuit

APPLICATIONS

- CRT terminals
- Word processing systems
- Small business computers
- Home computers

PIN CONFIGURATION



ORDERING CODE

PACKAGES	V_{CC} = 5V ±5%, T_A = 0° to 70°C	
	4MHz	2.7MHz
Ceramic DIP	SCN2674BC4I40	SCN2674BC3I40
Plastic DIP	SCN2674BC4N40	SCN2674BC3N40

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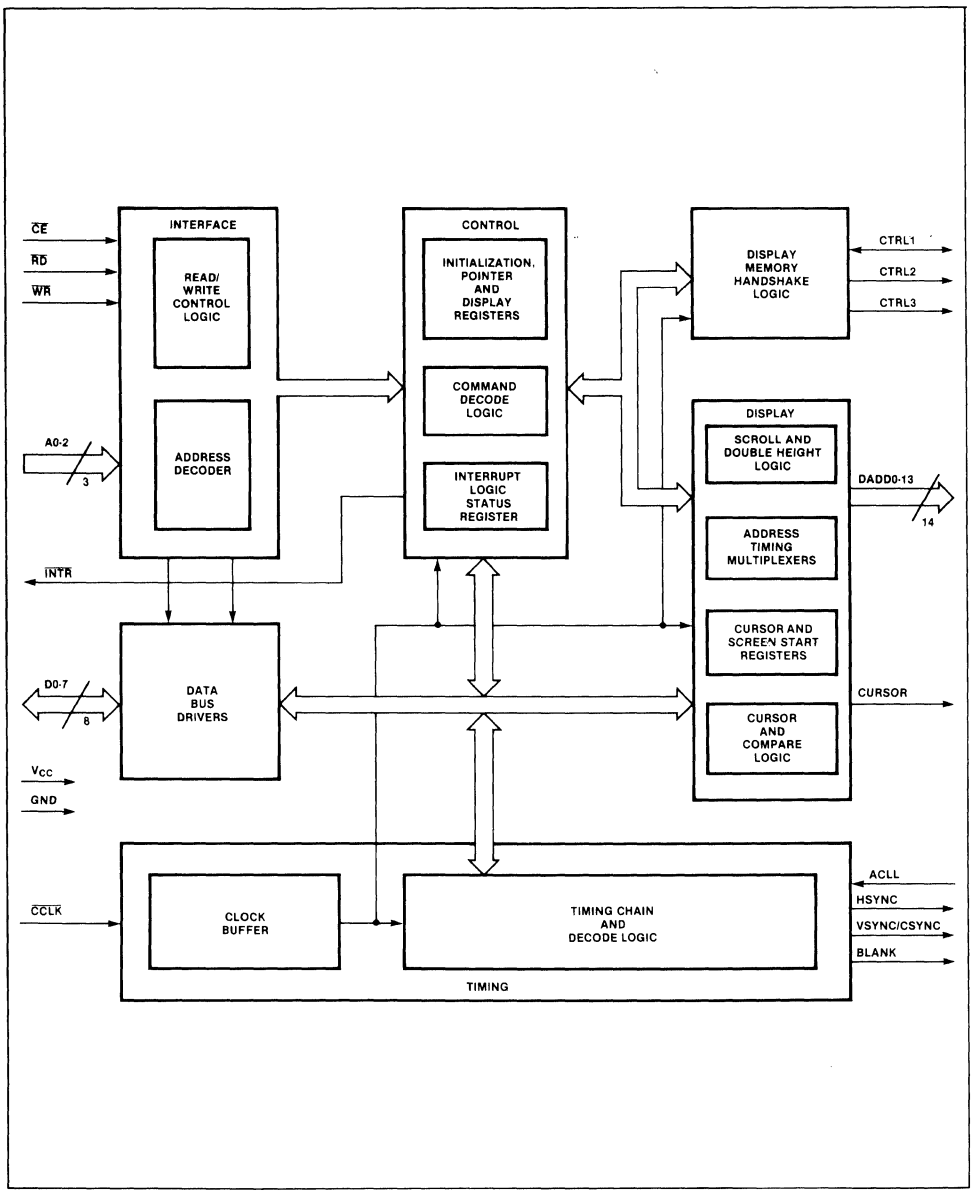
BLOCK DIAGRAM



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ADVANCED VIDEO DISPLAY CONTROLLER (AVDC) SCN2674

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PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
A0-A2	37-39	I	**Address Lines:** Used to select AVDC internal registers for read/write operations and for commands.
D0-D7	8-15	I/O	**8-Bit Bidirectional Three-State Data Bus:** Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the AVDC take place over this bus. The direction of the transfer is controlled by the $\overline{RD}$ and $\overline{WR}$ inputs when the $\overline{CE}$ input is low. When the $\overline{CE}$ input is high, the data bus is in the three-state condition.
$\overline{RD}$	1	I	**Read Strobe:** Active low input. A low on this pin while $\overline{CE}$ is low causes the contents of the register selected by A0-A2 to be placed on the data bus. The read cycle begins on the leading (falling) edge of $\overline{RD}$.
$\overline{WR}$	3	I	**Write Strobe:** Active low input. A low on this pin while $\overline{CE}$ is also low causes the contents of the data bus to be transferred to the register selected by A0-A2. The transfer occurs on the trailing (rising) edge of $\overline{WR}$.
$\overline{CE}$	2	I	**Chip Enable:** Active low input. When low, data transfers between the CPU and the AVDC are enabled on D0-D7 as controlled by the $\overline{WR}$, $\overline{RD}$, and A0-A2 inputs. When $\overline{CE}$ is high, effectively, the AVDC is isolated from the data bus and D0-D7 are placed in the three-state condition.
$\overline{CCLK}$	16	I	**Character Clock:** Timing signal derived from the video dot clock which is used to synchronize the AVDC's timing functions.
HSYNC	19	O	**Horizontal Sync:** Active high output which provides video horizontal sync pulses. The timing parameters are programmable.
VSYNC/CSYNC	18	O	**Vertical Sync/Composite Sync:** A control bit selects either vertical or composite sync pulses on this active high output. When CSYNC is selected, equalization pulses are included. The timing parameters are programmable.
BLANK	17	O	**Blank:** This active high output defines the horizontal and vertical borders of the display. Display control signals which are output on DADD0 and DADD3 thru DADD13 are valid on the trailing edge of BLANK.
CURSOR	7	O	**Cursor Gate:** This output becomes active for a specified number of scan lines when the address contained in the cursor register matches the address output on DADD0 through DADD13 for displayable character addresses. The first and last lines of the cursor and a blink option are programmable. When the row table addressing mode is enabled, this output is active for a portion of the blanking interval prior to the first scan line of a character row, while the AVDC is fetching the starting address for that row.
$\overline{INTR}$	35	O	**Interrupt Request:** Open drain output which supplies an active low interrupt request from any of five maskable sources. This pin is inactive after a power on reset or a master reset command.
ACLL	36	I	**AC Line Lock:** If this input is low after the programmed vertical front porch interval, the vertical front porch will be lengthened by increments of horizontal scan line times until this input goes high.
CTRL1	4	I/O	**Handshake Control 1:** In independent mode, provides an active low write data buffer ($\overline{WDB}$) output which strobes data from the interface latch into the display memory. In transparent and shared modes, this is an active low processor bus request ($\overline{PBREQ}$) input which indicates that the CPU desires to access the display memory.
CTRL2	5	O	**Handshake Control 2:** In independent mode, provides an active low read data buffer ($\overline{RDB}$) output which strobes data from the display memory into the interface latch. In transparent and shared modes, this is an active low bus external enable ($\overline{BEXT}$) output which indicates that the AVDC has relinquished control of the display memory (DADD0-DADD13 are in the three-state condition) in response to a CPU bus request. $\overline{BEXT}$ also goes low in response to a 'display off and float DADD' command. In row buffer mode, it is an active low bus request ($\overline{BREQ}$) output which halts the CPU during a line DMA.
CTRL3	6	O	**Handshake Control 3:** In independent mode, provides the active low buffer chip enable ($\overline{BCE}$) signal to the display memory. In transparent and shared modes, provides an active low bus acknowledge ($\overline{BACK}$) output which serves as a ready signal to the CPU in response to a processor bus request. In row buffer mode, this is an active high memory bus control (MBC) output which configures the system for the DMA transfer of one row of character codes from system memory to the row display buffer.

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MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
DADD0-DADD13	34-21	O	**Display Address:** Used by the AVDC to address up to 16K of display memory directly, or to 64K of memory by de-multiplexing DADD14 and DADD15. These outputs are floated at various times depending on the buffer mode. Various control signals are multiplexed on DADD0 through DADD13 and are valid at the trailing edge of BLANK. These control signals are: DADD0/LG **Line Graphics:** Output which denotes bit mapped graphics mode. DADD1/DADD14 **Display Address 14:** Multiplexed address bit used to extend addressing to 64K. DADD2/DADD15 **Display Address 15:** Multiplexed address bit used to extend addressing to 64K. DADD3/LR **Last Row:** Output which indicates the last active character row of each field. DADD4-DADD7/LA0-LA3 **Line Address:** Provides the number of the current scan line count for each character row. DADD8/FL **First Line:** Asserted during the blanking interval just prior to the first scan line of each character row. DADD9/DW **Double Width:** Output which denotes a double width character row. DADD10/UL **Underline:** Asserted during the blanking interval just prior to the scan line which matches the programmed underline position (line 0 thru 15). DADD11/BLINK **Blink Frequency:** Provides an output divided down from the vertical sync rate. DADD12/ODD **Odd Field:** Active high signal which is asserted before each scan line of the odd field when interlace is specified. Replaces DADD4/LA0 as the least significant line address for interlaced sync and video applications. DADD13/LL **Last Line:** Asserted during the blanking interval just prior to the last scan line of each character row.
V_{CC}	40	I	**Power Supply:** +5 volts power input.
GND	20	I	**Ground:** Signal and power ground input.

FUNCTIONAL DESCRIPTION

As shown in the block diagram, the AVDC contains the following major blocks:

- Data bus buffer
- Interface Logic
- Operation Control
- Timing
- Display Control
- Buffer Control

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data busses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the AVDC.

Interface Logic

The interface logic contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The functions performed by the CPU read and write operations are shown in table 1.

Operation Control

The operation control section decodes configuration and operation commands from the CPU and generates appropriate

Table 1 AVDC ADDRESSING

A2	A1	A0	READ ($\overline{RD}$ = 0)	WRITE ($\overline{WR}$ = 0)
0	0	0	Interrupt register	Initialization registers[1]
0	0	1	Status register	Command register
0	1	0	Screen start 1 lower register	Screen start 1 lower register
0	1	1	Screen start 1 upper register	Screen start 1 upper register
1	0	0	Cursor address lower register	Cursor address lower register
1	0	1	Cursor address upper register	Cursor address upper register
1	1	0	Screen start 2 lower register	Screen start 2 lower register
1	1	1	Screen start 2 upper register	Screen start 2 upper register

[1]There are 15 initialization registers which are accessed sequentially via a single address. The AVDC maintains an internal pointer to these registers which is incremented after each write at this address until the last register (IR14) is accessed. The pointer then continues to point to IR14 for additional accesses. Upon a power-on or a master reset command, the internal pointer is reset to point to the first register (IR0) of the initialization register group. The internal pointer can also be preset to any register of the group via the 'load IR address pointer' command.

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signals to other internal sections to control the overall device operation. It contains the timing and display registers which configure the display format and operating mode, the interrupt logic, and the status register which provides operational feedback to the CPU.

Timing

The timing section contains the counters and decoding logic necessary to generate the monitor timing outputs and to control the display format. These timing parameters are selected by programming of the initialization registers.

Display Control

The display control section generates linear addressing for up to 16K bytes of display memory. Internal comparators limit the portion of the memory which is displayed to programmed values. Additional functions performed in this section include cursor positioning and address comparisons required for generation of timing signals, double height tops and bottoms, smooth scrolling, and the split screen interrupts.

Buffer Control

The buffer control section generates three signals which control the transfer of data between the CPU and the display buffer memory. Four system configurations requiring four different 'handshaking' schemes are supported. These are described below.

SYSTEM CONFIGURATIONS

Figure 1 illustrates the block diagram of a typical display terminal using the Signetics SCN2670, SCN2671, SCN2674, and SCB2675 CRT terminal devices. In this system, the CPU examines inputs from the data communications line and the keyboard and places the data to be displayed in the display buffer memory. This buffer is typically a RAM which holds the data for a single or multiple screen-load (page) or for a single character row.

The AVDC supports four common system configurations of display buffer memory, designated the independent, transparent, shared, and row buffer modes. The first three modes utilize a single or multiple page RAM and differ primarily in the means used to transfer display data between the RAM and the CPU. The row buffer mode makes use of a single row buffer (which can be a shift register or a small RAM) that is updated in real time to contain the appropriate display data.

The user programs bits 0 and 1 of IR0 to select the mode best suited for the system environment. The CNTRL1-3 outputs perform different functions for each mode and are named accordingly in the description of each mode.

Independent Mode

The CPU to RAM interface configuration for this mode is illustrated in figure 2. Transfer of data between the CPU and display memory is accomplished via a bidirectional latched port and is controlled by read data buffer ($\overline{RDB}$), write data buffer ($\overline{WDB}$), and buffer chip enable ($\overline{BCE}$). This mode provides a non-contention type of operation that does not require address multiplexers. The CPU does not address the memory directly—the read or write operation is performed at the address contained in the cursor address register or the pointer address register as specified by the CPU. The AVDC enacts the data transfers during blanking intervals in order to prevent visual disturbances of the displayed data.

The CPU manages the data transfers by supplying commands to the AVDC. The commands used are:

1. Read/write at pointer address.
2. Read/write at cursor address (with optional increment of address).
3. Write from cursor address to pointer address.

The operational sequence for a write operation is:

1. CPU checks RDFLG status bit to assure that any delayed commands have been completed.
2. CPU loads data to be written to display memory into the interface latch.
3. CPU writes address into cursor or pointer registers.
4. CPU issues 'write at cursor with/without increment' or 'write at pointer' command.
5. AVDC generates control signals and outputs specified address to perform requested operation. Data is copied from the interface latch into the memory.
6. AVDC sets RDFLG status to indicate that the write is completed.

Similarly, a read operation proceeds as follows:

1. Steps 1 and 3 as above.
2. CPU issues 'read at cursor with/without increment' or 'read at pointer' command.
3. AVDC generates control signals and outputs specified address to perform requested operation. Data is copied from memory to the interface latch and AVDC sets RDFLG status to indicate that the read is completed.
4. CPU checks RDFLG status to see if operation is completed.
5. CPU reads data from interface latch.

Loading the same data into a block of display memory is accomplished via the 'write from cursor to pointer' command:

1. CPU checks RDFLG status bit to assure that any delayed commands have been completed.
2. CPU loads data to be written to display memory into the interface latch.
3. CPU writes beginning address of memory block into cursor address register and ending address of block into pointer address register.
4. CPU issues 'write from cursor to pointer' command.
5. AVDC generates control signals and outputs block addresses to copy data from the interface latch into the specified block of memory.
6. AVDC sets RDFLG status to indicate that the block write is completed.

Similar sequences can be implemented on an interrupt driven basis using the READY interrupt output to advise the CPU that a previously asserted delayed command has been completed.

Two timing sequences are possible for the 'read/write at cursor/pointer' commands. If the command is given during the active display window (defined as first scan line of the first character row to the last scan line of the last character row), the operation takes place during the next horizontal blanking interval, as illustrated in figure 3. If the command is given during the vertical blanking interval, or while the display has been commanded blanked, the operation takes place immediately. In the latter case, the execution time for the command is approximately five character clocks (see figure 4).

Timing for the 'write from cursor to pointer' operation is shown in figure 5. The memory is filled at a rate of one location per two character times. The command will execute only during blanking intervals and may require many horizontal or vertical blanking intervals to complete. Additional delayed commands can be asserted immediately after this command has completed.

Immediate commands can be asserted at any time regardless of the state of the ready status/interrupt.

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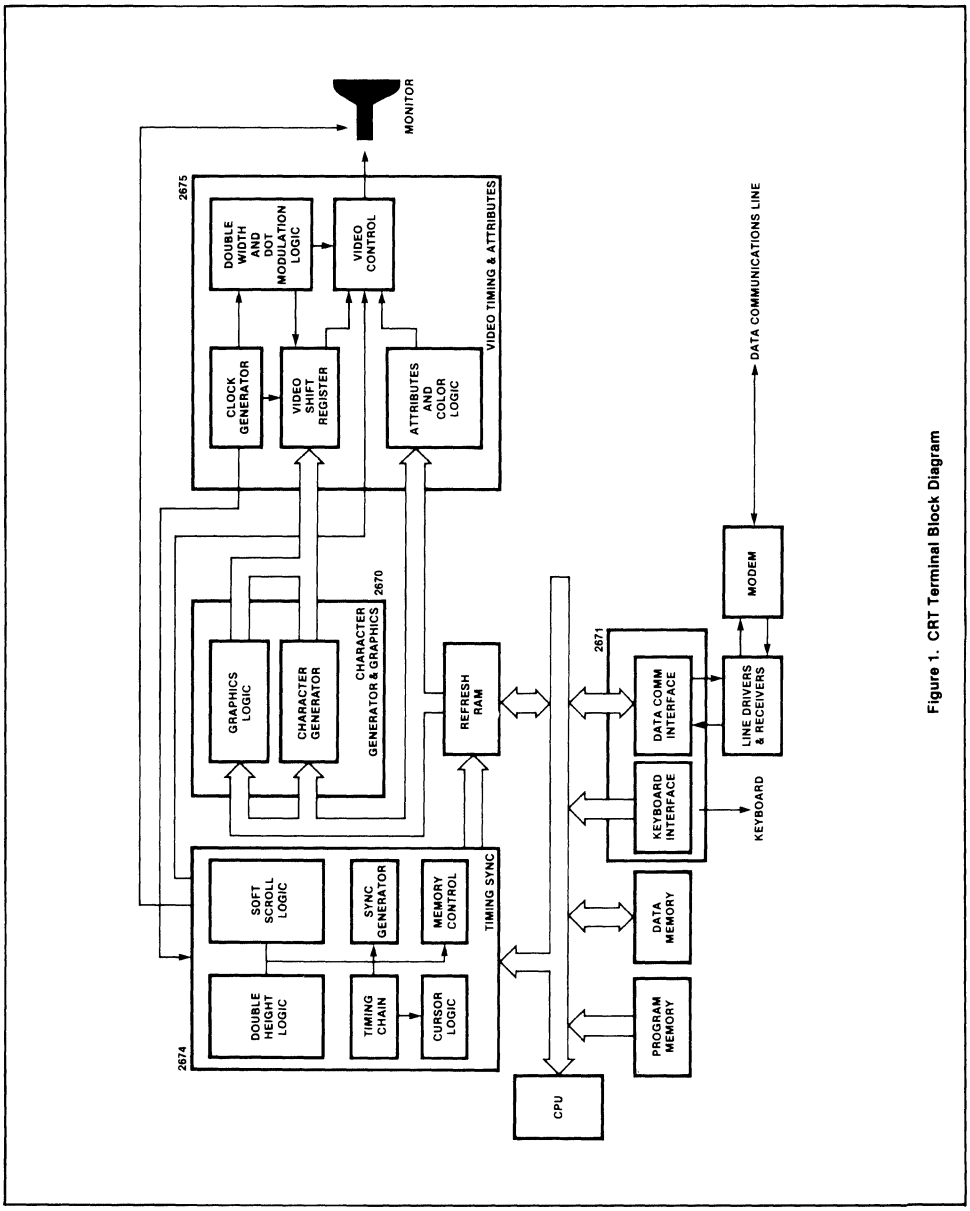

Figure 1. CRT Terminal Block Diagram

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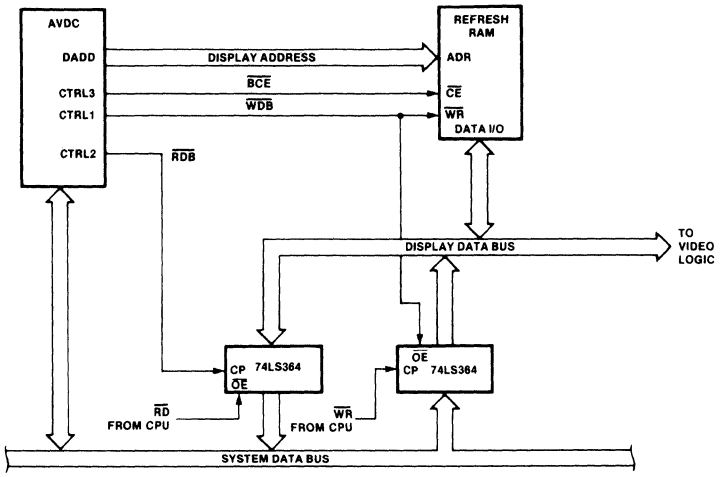
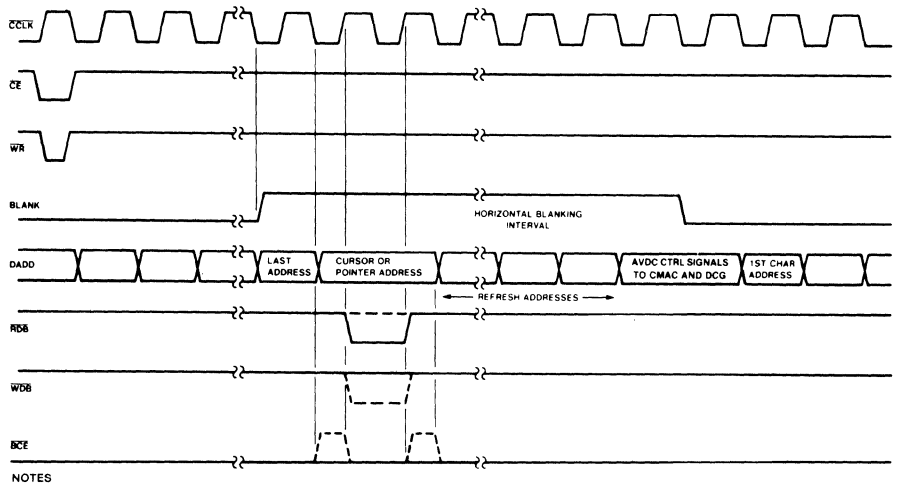


Figure 2. Indendent Buffer Mode Configuration



NOTES
1. Write waveforms shown in dotted lines.
2. If command execution occurs just prior to the first scan line of a character row and row table addressing mode is enabled, execution of the command is delayed by two character clocks from the timing illustrated.

Figure 3. Read/Write at Cursor/Pointer Command Timing (Command Received During Active Display Window)

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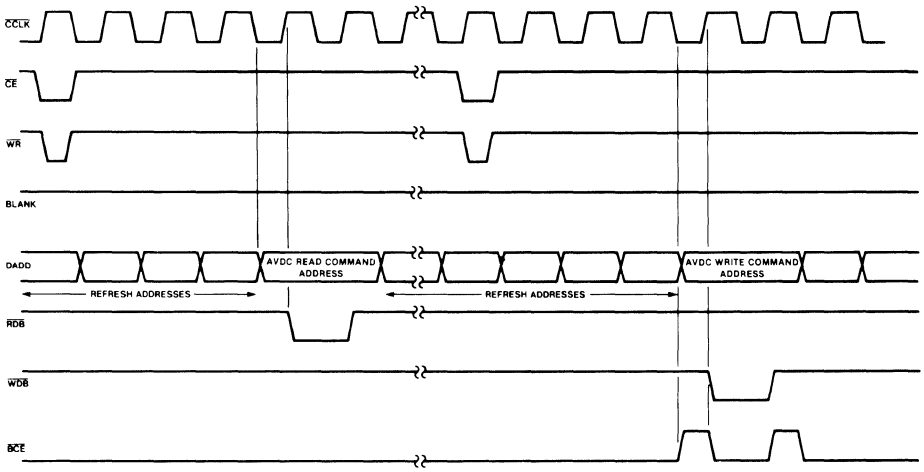

Figure 4. Read/Write at Cursor/Pointer Command Timing (Command Received While Display is Blanked)

Shared and Transparent Buffer Modes

In these modes, the display buffer RAM is a part of the CPU memory domain and is addressed directly by the CPU. Both modes use the same hardware configuration with the CPU accessing the display buffer via three-state drivers (see figure 6). The processor bus request ($\overline{PBREQ}$) control signal informs the AVDC that the CPU is requesting access to the display buffer. In response to this request, the AVDC raises bus acknowledge ($\overline{BACK}$) until its bus external ($\overline{BEXT}$) output has freed the display address and data busses for CPU access. $\overline{BACK}$, which can be used as a 'hold' input to the CPU, is then lowered to indicate that the CPU can access the buffer.

In transparent mode, the AVDC delays the granting of the buffer to the CPU until a vertical or horizontal blanking interval, thereby causing minimum disturbance of the display. In shared mode, the AVDC will blank the display and grant immediate access to the CPU. Timing for these modes is illustrated in figures 7, 8, and 9.

Row Buffer Mode

Figures 10 and 11 show the timing and a typical hardware implementation for the row buffer mode. During the first scan line (line 0) of each character row, the AVDC halts the CPU and DMA's the next row of character data from the system memory to the row buffer memory. The AVDC then releases the CPU and displays the row buffer data for the programmed number of scan lines. The control signal $\overline{BREQ}$ informs the CPU that character addresses and the MBC signal will start at the next falling edge of BLANK. The CPU must release the address and data busses before this time to prevent bus contention. After the row of character data is transferred to the CPU, $\overline{BREQ}$ returns high to grant memory control back to the CPU.

Row Table Addressing Mode

In this mode, each character row in the screen image memory has a unique starting address. This provides greater flexibility with respect to screen operations, such as editing, than the sequential addressing mode. The row table, figure 12, is a list of starting addresses for each character row and may reside anywhere in the AVDC's addressable memory space. Each entry in the table consists of two bytes: the first byte contains the 8 LSBs of the row starting address and the second byte contains, in its 6 least significant bits, the 6 MSBs of the row starting address. The function of the two MSBs of the second byte is selected by programming IR0[7]. They may be used either as row attribute bits to control double width and double height for that character row, or as an additional two address bits to extend the usable display memory to 64K.

The first address of the row table is designated in screen start register two (SSR2). If row table addressing is enabled via IR2[7], and the display is on, the ADVC fetches the next row's starting address from the table during the blanking interval prior to the first scan line of each character row, while simultaneously incrementing the contents of SSR2 by two so as to point to the next table entry. The fetching of the row starting address from the row table is indicated by the assertion of the CURSOR output during BLANK. The address read from the table by the AVDC is loaded into screen start register 1 (SSR1) for use internally. Since the contents of SSR2 changes as the table entries are fetched, it must be re-initialized to point to the first table entry during each vertical retrace interval.

Row table addressing is intended primarily for use in conjunction with the row buffer mode of operation and requires no additional circuitry in that case. It may

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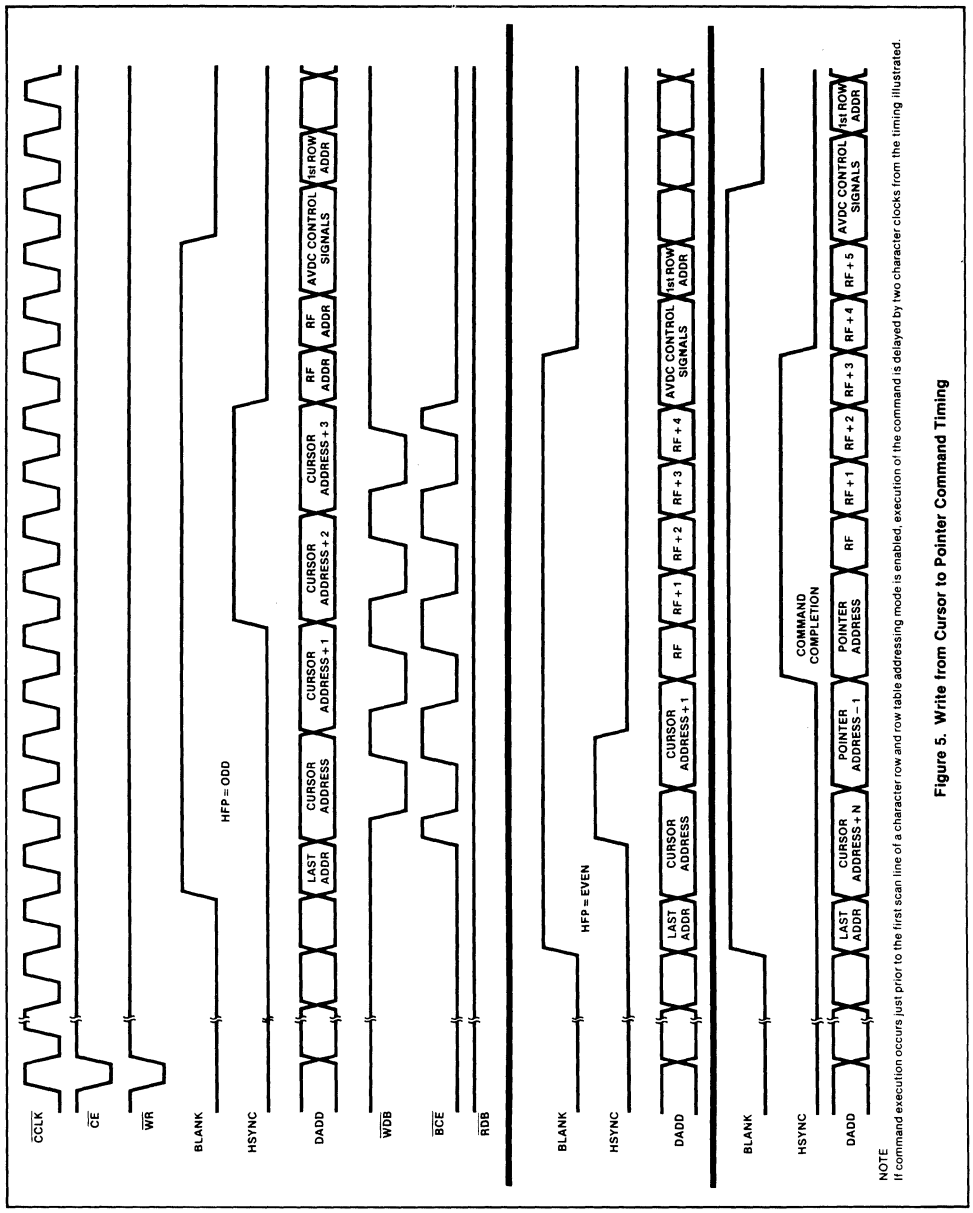

NOTE
If command execution occurs just prior to the first scan line of a character row and row table addressing mode is enabled, execution of the command is delayed by two character clocks from the timing illustrated.

Figure 5. Write from Cursor to Pointer Command Timing

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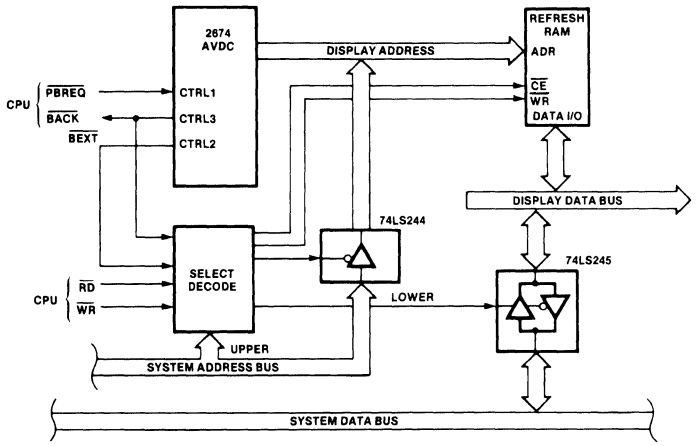
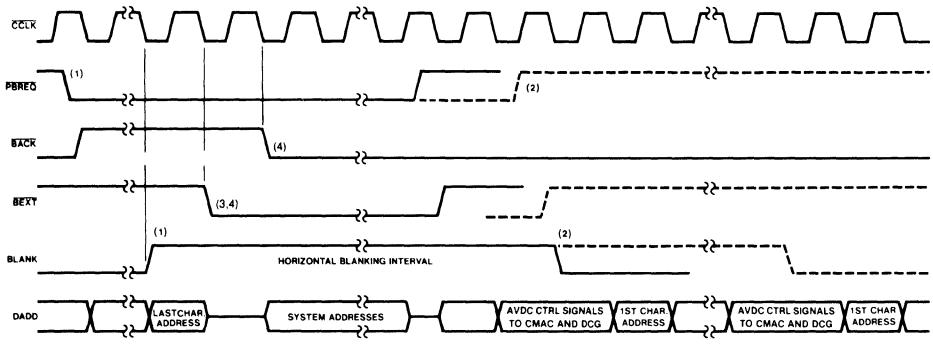


Figure 6. AVDC Shared or Transparent Buffer Modes



NOTES

1. $\overline{PBREQ}$ must be asserted prior to the rising edge of BLANK in order for sequence to begin during that blanking period.
2. If $\overline{PBREQ}$ is negated after the next to last $\overline{CCLK}$ of the horizontal blanking interval, the next scan line will also be blanked.
3. Accesses during vertical blank or "display off" are granted only at the beginning of the horizontal front porch.
4. If row table addressing is enabled, CPU access is delayed by two character clocks prior to the first scan line of each character row.

Figure 7. Transparent Buffer Mode Timing

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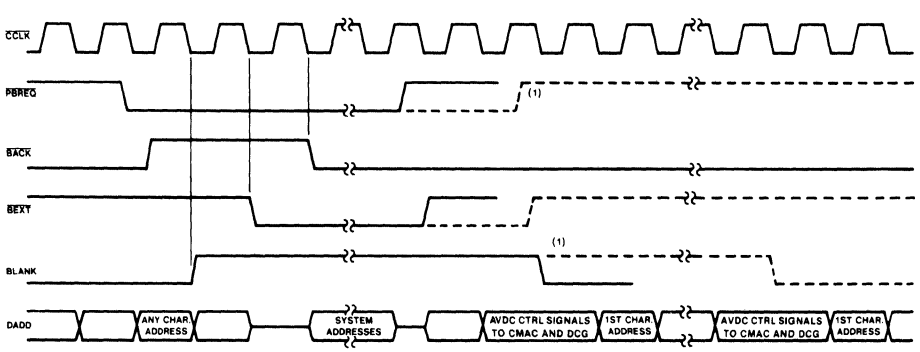
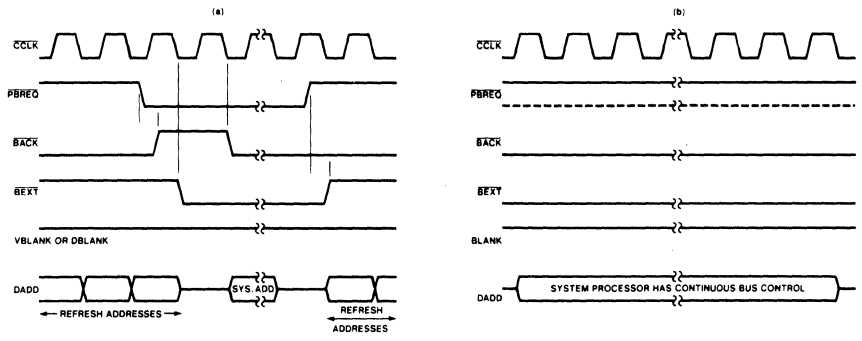


NOTE
1. If $\overline{PBREQ}$ is negated after the next to last $\overline{CCLK}$ of the horizontal blanking interval, the next scan line will also be blanked.

Figure 8. Shared Buffer Mode Timing



a) During Vertical Blank or after 'display off' command in shared mode only. See Figure 7 for transparent timing.

b) After 'display off and 3-state' command

Figure 9. Shared and Transparent Mode Timing

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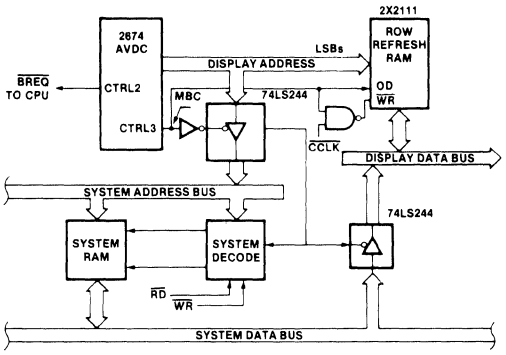
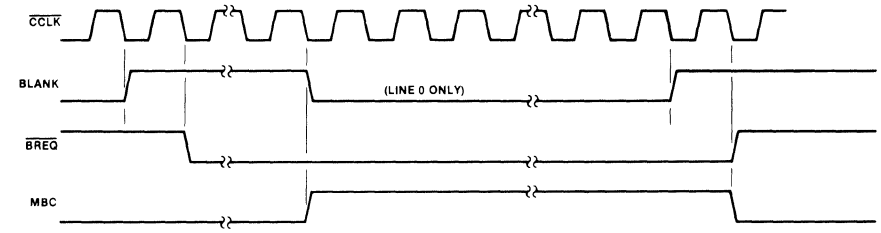


Figure 10. Row Buffer Mode Configuration



NOTE
If row table addressing is enabled, BREQ will be asserted at the middle of the last scan line of the prior row, and MBC will be asserted at the beginning of BLANK.

Figure 11. Row Buffer Mode Timing

also be used with the other modes, but circuitry must be added to route the data from the display memory to the data bus inputs of the AVDC. Additionally, when not operating in row buffer mode, care must be taken to assure that the CPU does not attempt to access the AVDC while it is reading the row table. One way of preventing this is to latch the last line output which is multiplexed on DADD13 and to test this latch prior to reading or writing the AVDC. The AVDC should only be accessed if the latch is low, indicating that the last line of the row is not active.

Figure 13 illustrates a typical hardware implementation for use in conjunction with independent and transparent modes, and figure 14 shows the timing for row table operation.

OPERATION

After power is applied, the AVDC will be in an inactive state. Two consecutive 'master reset' commands are necessary to release this circuitry and ready the AVDC for operation. Two register groups exist within the AVDC: the initialization registers and the display control registers. The initialization registers select the system configuration, monitor timing, cursor shape, display memory domain, pointer address, scrolling region, double height and width condition, and screen format. These are loaded first and normally require no modification except for certain special visual effects. The display control registers specify the memory address of the base character (upper left corner of screen), the cursor position, and the split screen addresses associated with the scrolling area or an alternate memory. These may require modification during operation.

After initial loading of the two register groups, the AVDC is ready to control the monitor screen. Prior to executing the AVDC commands which turn on the display and cursor, the user should load the display memory with the first data to be displayed. During operation, the AVDC will sequentially address the display memory within the limits programmed into its registers. The memory outputs character codes to the system character and graphics generation logic, where they are converted to the serial video stream necessary to display the data on the CRT. The user effects changes to the display by modifying the contents of the display memory, the AVDC display control and

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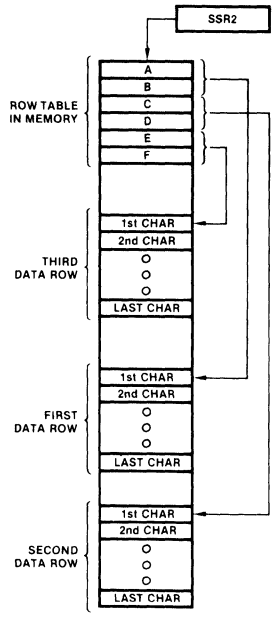

Figure 12. Row Table Address Format

command registers, and the initialization registers, if required. Interrupts and status conditions generated by the AVDC supply the 'handshaking' information necessary for the CPU to effect real time display changes in the proper time frame if required.

INITIALIZATION REGISTERS

There are 15 initialization registers (IR0-IR14) which are accessed sequentially via a single address. The AVDC maintains an internal pointer to these registers which is incremented after each write at this address until the last register (IR14) is accessed. The pointer then continues to point to IR14 for further accesses. Upon a power-on or a master reset command, the internal pointer is reset to point to the first register (IR0) of the initialization register group. The internal pointer can also be preset to any register of the group via the 'load IR address pointer' command. These registers are write only and are used to specify parameters such as the system configuration, display format, cursor shape, and monitor timing. Register formats are shown in figure 15.

IR0[7] — Double Height/ Width Enable

When this bit is set, the value in IR14[7:6] is used to control the double height and width conditions of each character row. Assertion of this bit also allows IR14[7:6] to be programmed in two ways:

1. By the CPU writing to IR14 directly.
2. When the contents of screen start register 1 (SSR1) upper are changed, either by the CPU writing to this register or by the automatic loading of SSR1 when operating in row table mode, the two MSBs of SSR1 upper are copied into IR14[7:6]. Thus, the MSBs of each row table entry can be used to control double height and double width attributes on a row by row basis.

IR14[5:4] are not active when this bit is set. When this bit is reset, the double height and width attributes operate as described in IR[14].

IR0[6:3] — Scan Lines per Character Row

Both interlaced and non-interlaced scanning are supported by the AVDC. For interlaced mode, two different formats can be implemented, depending on the interconnection between the AVDC and the character generator (see IR1[7]). This field defines the number of scan lines used to compose a character row for each technique. As scanning occurs, the scan line count is output on the LA0-LA3 and ODD pins.

IR0[2] — VSYNC/CSYNC Enable

This bit selects either vertical sync pulses or composite sync pulses on the VSYNC/CSYNC output (pin 18). The composite sync waveform conforms to EIA RS170 standards, with the vertical interval composed of six equalizing pulses, six vertical sync pulses, and six more equalizing pulses.

IR0[1:0] — Buffer Mode Select

Four buffer memory modes may be selectively enabled to accommodate the desired system configuration. See System Configurations.

IR1[7] — Interlace Enable

Specifies interlaced or noninterlaced timing operation. Two modes of interlaced operation are available, depending on whether L0-L3 or ODD, L0-L2 are used as the line address for the character generator. The resulting displays are shown in figure 16.

For 'interlaced sync' operation, the same information is displayed in both odd and even fields, resulting in enhanced readability. The AVDC outputs successive line numbers in ascending order on the LA0-LA3 lines, one per scan line for each field.

The 'interlaced sync and video' format doubles the character density on the screen. The AVDC outputs successive line numbers in ascending order on the odd and LA0-LA2 lines, one per scan line for each field.

IR1[6:0] — Equalizing Constant

This field indirectly defines the horizontal front porch and is used internally to generate the equalizing pulses for the RS170 compatible CSYNC. The value for this field is the total number of character clocks ($\overline{CCLKs}$) during a horizontal line period divided by two, minus two times the number of character clocks in the horizontal sync pulse:

$$EC = \frac{H_{ACT} + H_{FP} + H_{SYNC} + H_{BP}}{2} - 2(H_{SYNC})$$

The definition of the individual parameters is illustrated in figure 17. The minimum value of H_{FP} is two character clocks.

Note that when using the 2675 CMAC, it will delay the blank pulse three $\overline{CCLKs}$ relative to the HSYNC pulse.

IR2[7] — Row Table Mode Enable

Assertion/negation of this bit causes the AVDC to begin/terminate operating in row table mode starting at the next character row. See Row Table Addressing Mode section. By using the split interrupt capability of the AVDC, this mode can be enabled and disabled on a particular character row. This allows a combination of row table and sequential addressing to be utilized to provide maximum flexibility in generating the display.

IR2[6:3] — Horizontal Sync Pulse Width

This field specifies the width of the HSYNC pulse in $\overline{CCLK}$ periods.

IR2[2:0] — Horizontal Back Porch

This field defines the number of $\overline{CCLKs}$ between the trailing edge of HSYNC and the trailing edge of BLANK.

IR3[7:5] — Vertical Front Porch

Specifies the number of scan line periods between the rising edges of BLANK and VSYNC during the vertical retrace interval. The vertical front porch will be extended in increments of scan lines if the ACLL input is low at the end of the programmed value.

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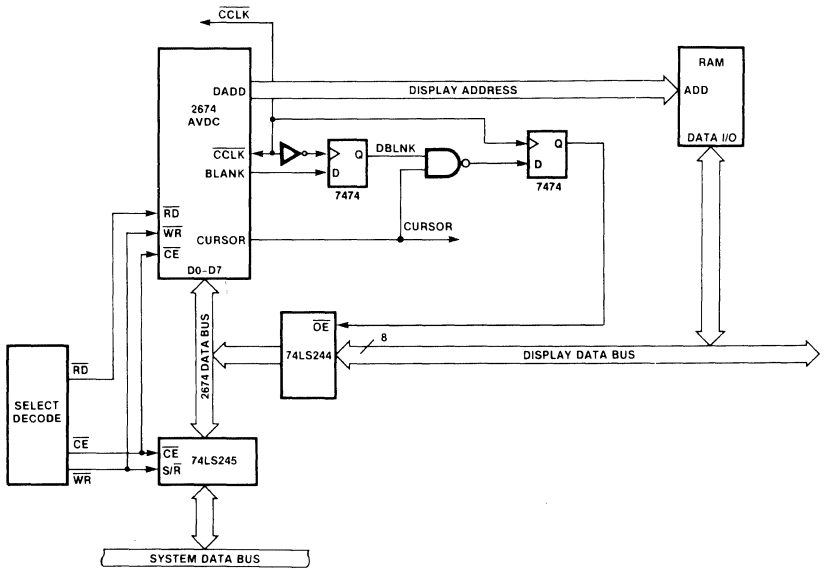

Figure 13. Row Table Mode Configuration (non-Row Buffer Modes)

IR3[4:0] — Vertical Back Porch

This field determines the number of scan line periods between the falling edges of the VSYNC and BLANK outputs.

IR4[7] — Character Blink Rate

Specifies the frequency for the character blink attribute timing. The blink rate can be specified as 1/64 or 1/128 of the vertical field rate. The timing signal has a duty cycle of 50% and is multiplexed onto the DADD11/BLINK output at the falling edge of each BLANK.

IR4[6:0] — Character Rows Per Screen

This field defines the number of character rows to be displayed. This value multiplied by the scan lines per character row, plus the vertical front porch, the vertical back porch values, and the vertical sync pulse width is the vertical scan period in scan lines.

IR5[7:0] — Active Characters Per Row

This field determines the number of characters to be displayed on each row of the CRT screen. The sum of this value, the horizontal front porch, the horizontal sync width, and the horizontal back porch is the horizontal scan period in $\overline{CCLK}$s.

IR6[7:4], IR6[3:0] — First and Last Scan Line of Cursor

These two fields specify the height and position of the cursor on the character block. The 'first' line is the topmost line when scanning from the top to the bottom of the screen.

IR7[7:6] — Vertical Sync Pulse Width

This field specifies the width of the VSYNC pulse in scan line periods.

IR7[5] — Cursor Blink Enable

This bit controls whether or not the cursor output pin will be blinked at the selected rate (IR7[4]). The blink duty cycle for the cursor is 50%.

IR7(4) — Cursor Blink Rate

The cursor blink rate can be specified at 1/32 or 1/64 of the vertical scan frequency. Blink is effective only if blink is enabled by IR7[5].

IR7[3:0] — Underline Position

This field defines which scan line of the character row will be used for the underline attribute by the 2675 CMAC. The timing signal is multiplexed onto the DADD10/UL output during the falling edge of BLANK.

IR9[3:0], IR8[7:0] — Display Buffer First Address
IR9[7:4] — Display Buffer Last Address

These two fields define the area within the buffer memory where the display data will reside. When the data at the 'display buffer last address' is displayed, the AVDC

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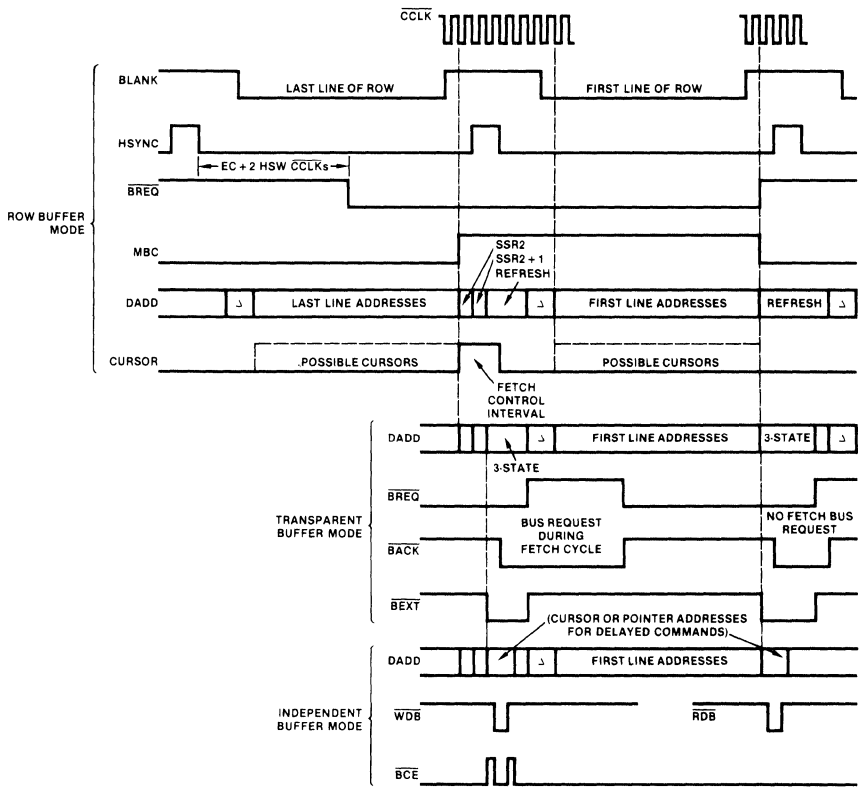

ↄ = MULTIPLEXED CONTROL SIGNALS
EC = EQUALIZING CONSTANT
HSW = HORIZONTAL SYNC WIDTH

Figure 14. Row Table Mode Timing

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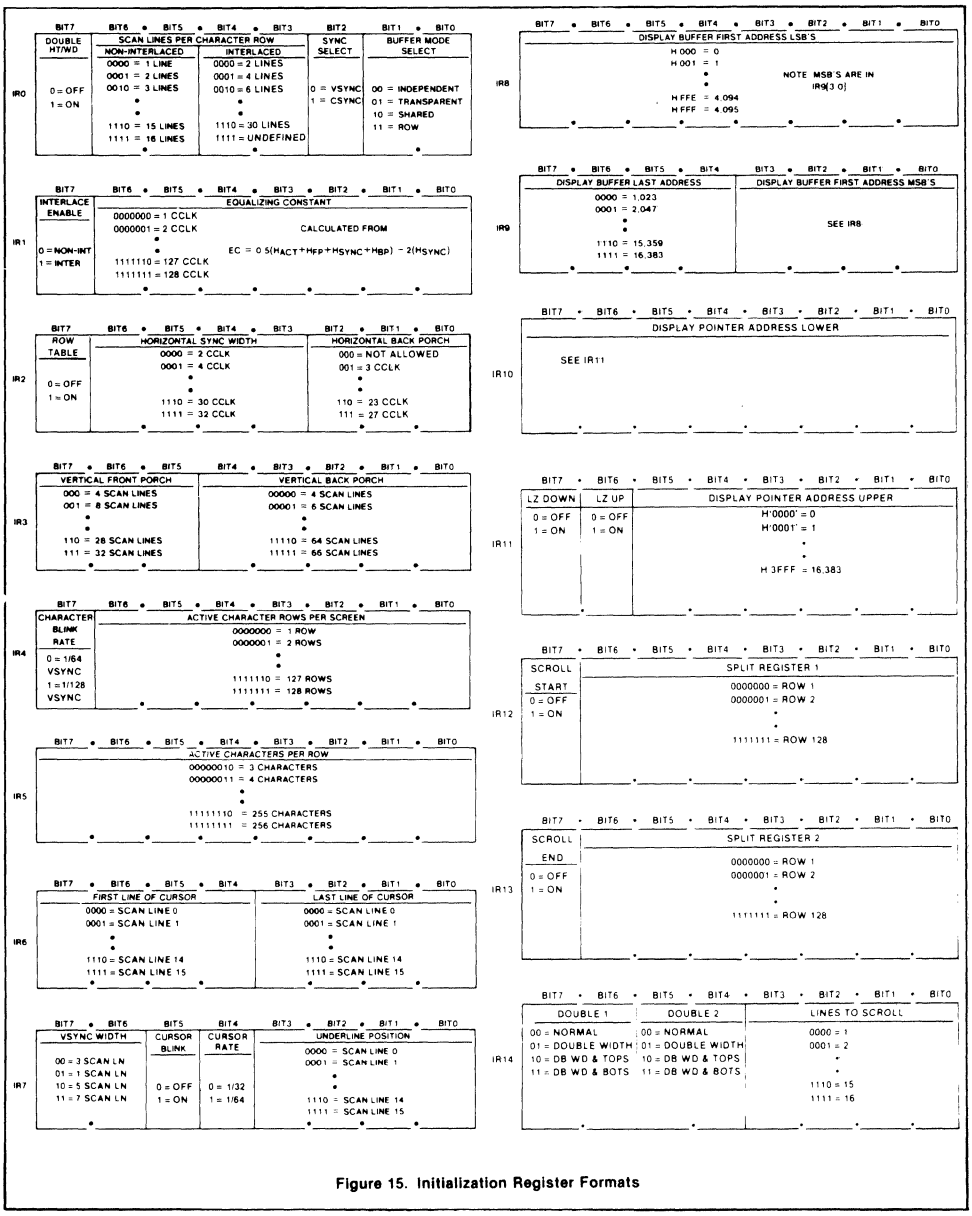

Figure 15. Initialization Register Formats

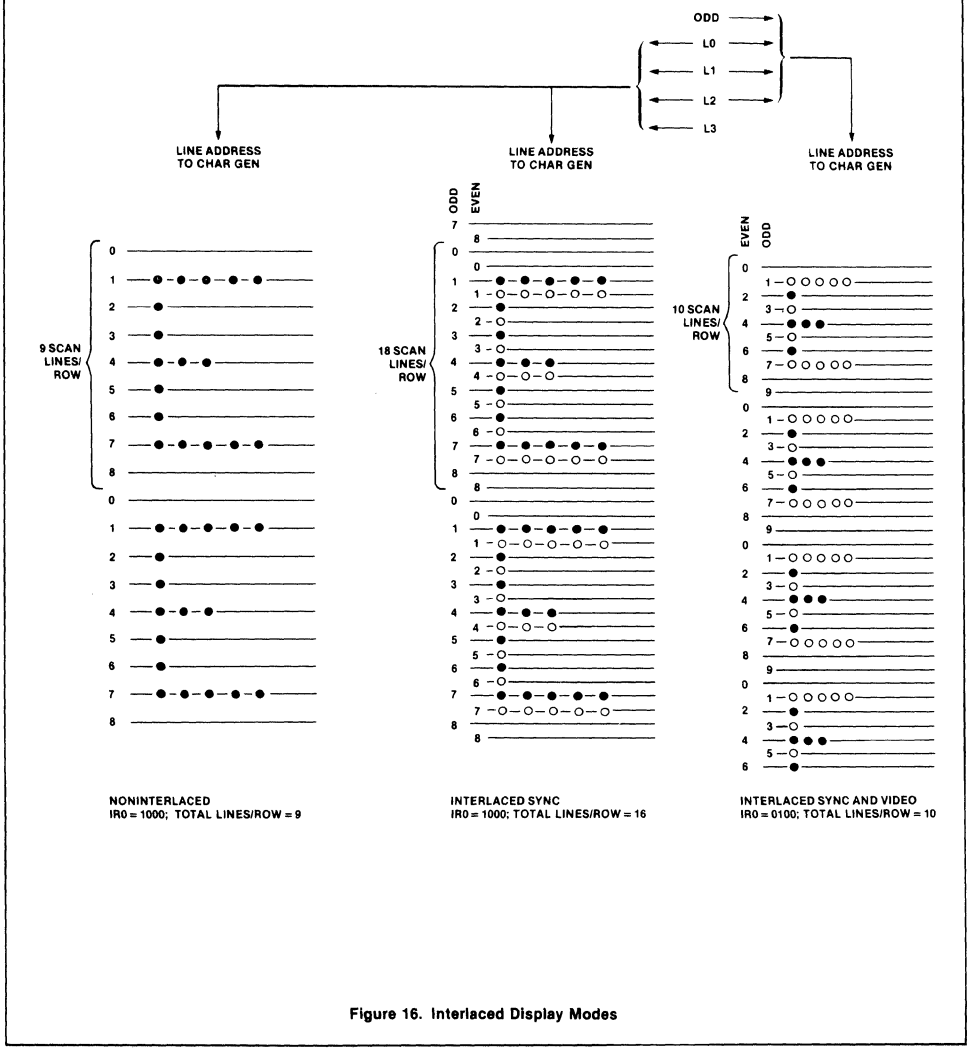

Figure 16. Interlaced Display Modes

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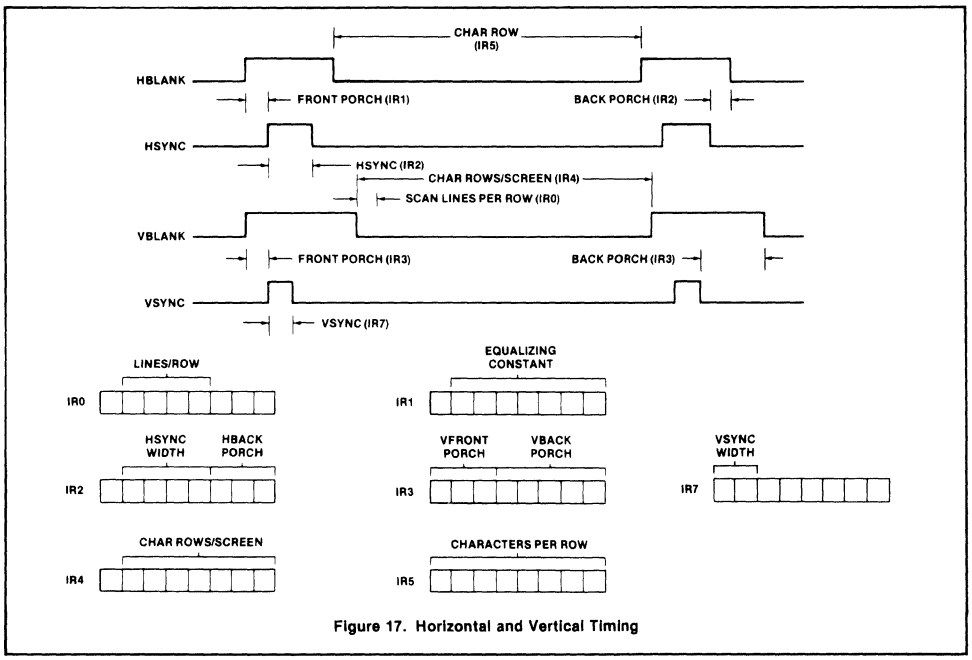

Figure 17. Horizontal and Vertical Timing

will wraparound and obtain the data to be displayed at the next screen position from the 'display buffer first address'. If 'last address' is the end of a character row and a new screen start address has been loaded into the screen start register, or if 'last address' is the last character position of the screen, the next data is obtained from the address contained in the screen start register.

Note that there is no restriction in displaying data from other areas of the addressable memory. Normally, the area between these two bounds is used for data which can be overwritten (e.g., as a result of scrolling), while data that is not to be overwritten would be contained outside these bounds and accessed by means of the automatic split screen or split screen interrupt feature of the AVDC.

IR10[7:0] — Display Pointer Address Lower

IR11[5:0] — Display Pointer Address Upper

These two fields define a buffer memory address for AVDC controlled accesses in response to 'read/write at pointer' commands. They also define the last buffer memory address to be written for the 'write from cursor to pointer' command.

IR11[7] — Scan Line Zero During Scroll Down

This field specifies normal scan line count of all scan line zero counts for the new character row that occurs at the top of the scrolling area during soft scroll down operation. If the character generator provides blanks during scan line zero, this will cause the new row to be automatically blanked on the display. This feature can be used, if necessary, to blank the new row until the CPU places 'blank data' into the display buffer.

IR11[6] — Scan Line Zero During Scroll Up

This field specifies normal scan line count of all scan line zero counts for the new character row that occurs at the bottom of the scrolling area during soft scroll up operation. See above.

IR12[7] — Scroll Start

This bit is asserted when soft scroll is to take place. The scrolling area begins at the row specified in split register 1 (IR12[6:0]). If set, the first row to scroll scan line count will be reduced by the value in the lines to scroll register (IR14[3:0]). The scan line count of this row will start at the programmed offset value. When this bit is asserted, scroll end IR13[7] must be set before split 2.

IR12[6:0] — Split Register 1

Split register 1 can be used to provide special screen effects such as soft (scan line by scan line) scrolling, double height/width rows, or to change the normal addressing sequence of the display memory. The contents of this field is compared, in real time, to the current row number. Upon a match, the AVDC sets the split screen 1 status bit, and issues an interrupt request if so programmed. The status change/interrupt request is made at the beginning of scan line zero of the split screen character row. If enabled by the SPL1 bit of screen start register 2, an automatic split screen to the address specified in screen

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start register 2 will be made for the designated character row. During a scroll operation, this field defines the first character row of the scrolling area.

IR13[7] — Scroll End

This field specifies that the row programmed in split register 2 (IR13[6:0]) is to be the last scrolling row of the scrolling area. Note that this bit must be asserted for a valid row only when the scroll start bit IR12[7] is also asserted.

IR13[6:0] — Split Register 2

This field is similar to the split register 1 field except for the following:

1. Split screen 2 status bit is set.
2. During a scroll operation, this field defines the last character row of the scrolling area. This row will be followed by a partial row. The LTSR (IR14) value replaces the normal scan lines/row value for the partial row, thus keeping the total scan lines/screen the same.
3. If enabled by the SPL2 bit of screen start register 2, an automatic split to the address contained in screen start register 2 will occur in one of two ways: a) If not scrolling an automatic split will occur for the next character row. b) If scrolling, the automatic split will occur after the partial row being scrolled onto or off the screen.
4. The specified double width and height conditions (IR14) are also asserted in two possible ways: a) Automatic split will assert the programmed condition for the current row. b) During soft scroll operation the programmed conditions are asserted for the partial row scrolling onto or off the screen.

IR14[7:6] — Double 1

This field specifies the conditions (double width/height or normal) of the row designated in split register 1 (IR12[6:0]). When double height tops or bottoms has been specified, the AVDC will automatically toggle between tops and bottoms until another split 1 or 2 occurs which changes the double height/width condition. If a double height tops row is specified, the scan line count will start at zero and increment the scan line count every other scan line. If a double height bottom row is specified, the AVDC will start at one half the normal scan line total. If double width is specified, the AVDC will assert the DADD9/DW output at the falling edge of blank. This condition will also remain active until the next split 1 or 2. When IR0[7] = 1, the values written into bits 7 and 6 of screen start 1 upper will also be written into IR14[7:6] and the automatic toggling between tops and bottoms is disabled.

IR14[5:4] — Double 2

This field specifies the conditions (double width/height or normal) of the row designated in split register 2 (IR13[6:0). Not used when IR0[7] = 1.

IR14[3:0] — Lines to Scroll

This field defines the scan line increment to be used during a soft scroll operation. This value will only be used when scroll start (IR12[7]) and scroll end (IR13[7]) are enabled.

Timing Considerations

Normally, the contents of the initialization registers are not changed during normal operation. However, this may be necessary to implement special display features such as multiple cursors and horizontal scrolling. Table 2 describes timing details for these registers which should be considered when implementing these features.

DISPLAY CONTROL REGISTERS

There are seven registers in this group, each with an individual address. Their formats are illustrated in figure 15. The command register is used to invoke one of 19 possible AVDC commands as described in the COMMANDS section of this data sheet. The remaining registers in the group store address values which specify the cursor location, the location of the first character to be displayed on the screen, and any split screen address locations. The user initializes these registers after powering on the system and changes their values to control the data which is displayed.

Screen Start Registers 1 and 2

The screen start 1 registers contain the address of the first character of the first row (upper left corner of the active display). At the beginning of the first scan line of the first row, this address is transferred to the row start register (RSR) and into the memory address counter (MAC). The counter is then advanced sequentially at the character clock rate for the number of times programmed into the active characters per row register (IR5), thus reaching the address of the last character of the row plus one. At the beginning of each subsequent scan line of the first row, the MAC is reloaded from the RSR and the above sequence is repeated. At the end of the last scan line of the first row, the contents of the MAC is loaded into the RSR to serve as the starting memory address for the second character row. This process is repeated for the programmed number of rows per screen. Thus, the data in the display memory is displayed sequentially starting from the address contained in the screen start register. After the ensuing vertical retrace interval, the entire process repeats again.

During vertical blanking, the address counter operation is modified by stopping the automatic load of the contents of the RSR into the counter, thereby allowing the address outputs to free-run. This allows dynamic memory refresh to occur during the vertical retrace interval. The refresh addressing starts at the last address displayed on the screen and increments by one for each character clock during the retrace interval. If the display buffer last address is encountered, refreshing continues from the display buffer first address.

The sequential operation described above will be modified upon the occurrence of any one of three events. First, if during the incrementing of the memory address counter the 'display buffer last address' (IR9[7:4]) is reached, the MAC will be loaded from the 'display buffer first address' register (IR9[3:0] and IR8[7:0]) at the next character clock. Sequential operation will then resume starting from this address. This wraparound operation allows portions of the display buffer to be used for purposes other than storage of displayable data and is completely automatic without any CPU intervention (see figure 19a).

The sequential row to row addressing can also be modified via split register 1 (IR12) and split register 2 (IR13), under CPU control, or by enabling the row table addressing mode. If bit 6 of screen start register 2 upper (SPL1) is set, the screen start register 2 contents will be loaded automatically into the RSR at the beginning of the first scan line of the row designated by split register 1 (IR12[6:0]). If bit 7 of screen start 2 upper (SPL2) is set, the screen start register 2 contents is automatically loaded into the RSR at the end of the last scan line of the row designated by split register 2 (IR13[6:0]). SPL1 and SPL2 are write only bits and will read as zero when reading screen start register 2.

If the contents of screen start register 1 (upper, lower, or both) are changed during any character row (e.g., row 'n'), the starting address of the next character row (row 'n + 1') will be the new value of the screen start register and addressing will continue

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Table 2 TIMING CONSIDERATIONS

PARAMETER	TIMING CONSIDERATIONS
First line of cursor Last line of cursor Underline line	These parameters must be established at a minimum of two character times prior to their occurrence
Double height character rows Double width character rows Rows to scroll	Set/reset prior to the row specified in split 1 or 2 registers
Cursor blink Cursor blink rate Character blink rate	New values become effective within one field after values are changed
Split register 1 Split register 2	Change anytime prior to line zero of desired row
Character rows per screen	Change only during vertical blanking period
Vertical front porch	Change prior to first line of VFP
Vertical back porch	Change prior to fourth line after VSYNC
Screen start register 1 Row table mode enable	Change prior to the horizontal blanking interval of the last line of character row before row where new value is to be used

sequentially from there. This allows features such as split screen operation, partial scroll, or status line display to be implemented. The split screen interrupt feature of the AVDC is useful in controlling the CPU initiated operations. Note that in order to obtain the correct screen display, screen start register 1 must be reloaded with the original (origin of display) value prior to the end of the vertical retrace. See figure 19b.

When row table addressing mode is enabled, the first address of the row table is designated in SSR2. The AVDC fetches the next row's starting address from the table during the blanking interval prior to the first scan line of each character row and loads it into SSR1 for use as the starting address of the next row. Since the contents of SSR2 changes as the table entries are fetched, it must be re-initialized to point to the first table entry during each vertical retrace interval.

The values in the two MSBs of SSR1 upper are multiplexed onto the DADD1/DADD14 and DADD2/DADD15 outputs during the

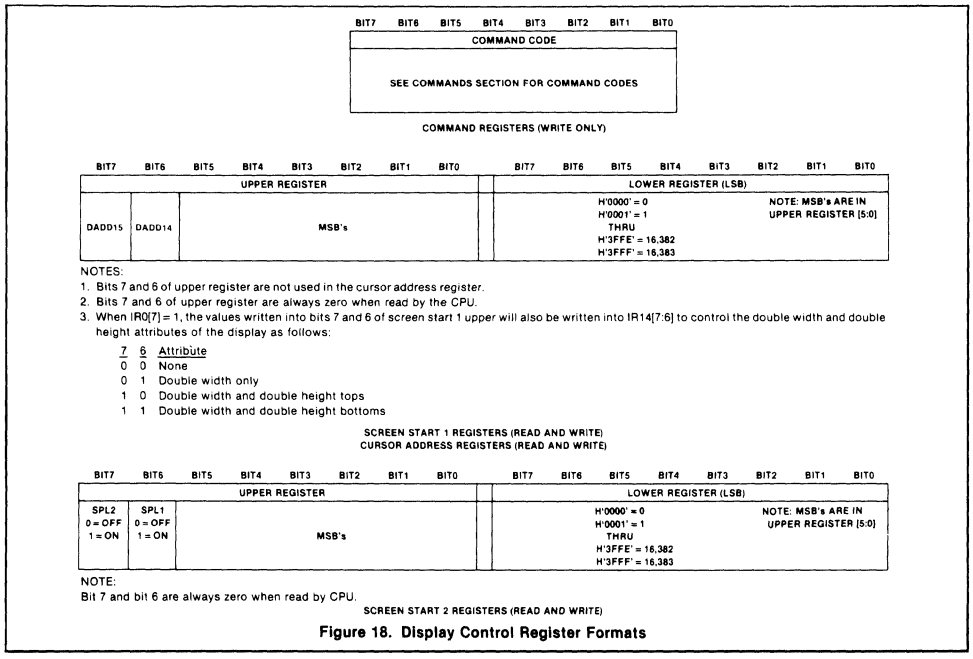

Figure 18. Display Control Register Formats

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falling edge of BLANK. If IR0[7] = 0, these two bits act as memory page select bits which may be used to extend the display memory addressing range of the AVDC up to 64K. In that case, these two bits act as a two-bit counter which is incremented each time that 'wraparound' occurs (see above). Note that the counter is incremented at the falling edge of BLANK and that for proper display operation the wraparound address should be programmed to occur at the last character position of a row. Also, the first address accessed in the new page will be the address contained in the display buffer first address register (IR9[3:0] and IR8[7:0]).

Cursor Address Registers

The contents of these registers define the buffer memory address of the cursor. The cursor output will be asserted when the memory address counter matches the value of the cursor address registers for the scan lines specified in IR6. The cursor address registers can be read or written by the CPU or incremented via the 'increment cursor address' command. In independent buffer mode, these registers define a buffer memory address for AVDC controlled access in response to 'read/write at cursor with/without increment' commands, or the first address to be used in executing the 'write from cursor to pointer' command.

INTERRUPT/STATUS REGISTERS

The interrupt and status registers provide information to the CPU to allow it to interact with the AVDC to effect desired changes that implement various display operations. The interrupt register provides information on five possible interrupting conditions, as shown in figure 20. These conditions can be selectively enabled or disabled (masked) from causing interrupts by certain AVDC commands. An interrupt condition which is enabled (mask bit equal to one) will cause the $\overline{INTR}$ output to be asserted and will cause the corresponding bit in the interrupt register to be set upon the occurrence of the interrupting condition. An interrupt condition which is disabled (mask bit equal to zero) has no effect on either the $\overline{INTR}$ output or the interrupt register.

The status register provides six bits of status information: the five possible interrupting conditions plus the RDFLG bit. For this register, however, the contents are not affected by the state of the mask bits.

Descriptions of each interrupt/status register bit follow. Unless otherwise indicated, a bit, once set, will remain set until reset by the CPU by issuing a 'reset interrupt/status bits' command. The bits are also reset by a 'master reset' command and upon power-up.

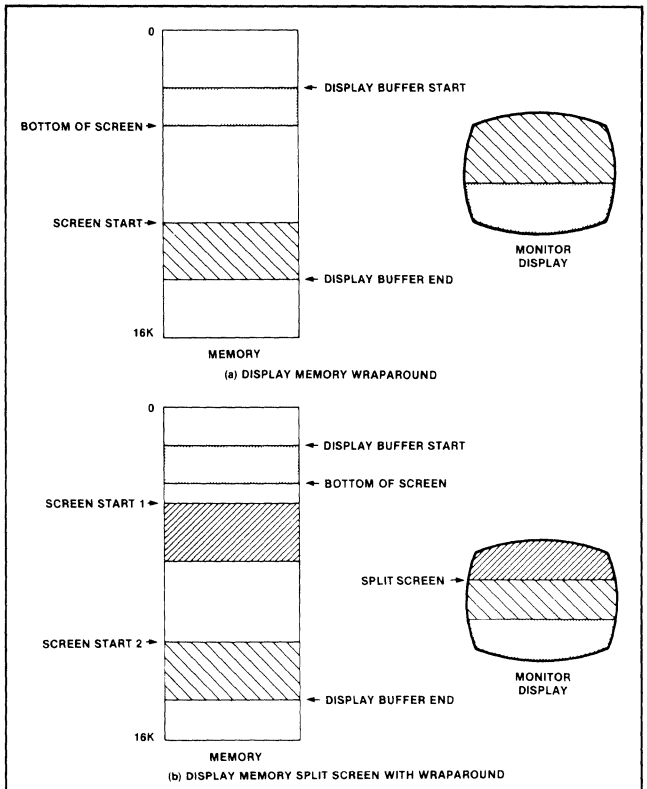

Figure 19. Display Addressing Operation

SR[5] — RDFLG

This bit is present in the status register only. A zero indicates that the AVDC is currently executing the previously issued delayed command. A one indicates that the AVDC is ready to accept a new delayed command.

I/SR[4] — VBLANK

Indicates the beginning of a vertical blanking interval. Set to one at the beginning of the first scan line of the vertical front porch.

I/SR[3] — Line Zero

Set to one at the beginning of the first scan line (line 0) of each active character row.

I/SR[2] — Split Screen 1

This bit is set when a match occurs between the current character row number and the value contained in split register 1, IR12[6:0]. The equality condition is only checked at the beginning of line zero of each character row.

I/SR[1] — Ready

The delayed commands affect the display and may require the AVDC to wait for a

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BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
NOT USED ALWAYS READ AS 0		RDFLG	VBLANK	LINE ZERO	SPLIT 1	READY	SPLIT 2
		0 = BUSY 1 = READY *	0 = NO 1 = YES	0 = NO 1 = YES	0 = NO 1 = YES	0 = BUSY 1 = READY	0 = NO 1 = YES

* STATUS REGISTER ONLY. ALWAYS 0 WHEN READING INTERRUPT REGISTER.

Figure 20. Interrupt and Status Register Format

blanking interval before enacting the command. This bit is set to one when execution of a delayed command has been completed. No other delayed command should be invoked until the prior delayed command is completed.

I/SR[0] — Split Screen 2

This bit is set when a match occurs between the current character row number and the value contained in split register 2 (IR13[6:0]) when you are not scrolling. It is set for the value contained in (split screen register 2) + 1 when scrolling.

COMMANDS

The AVDC commands are divided into two classes: the instantaneous commands which are executed immediately after they are invoked, and the delayed commands which may need to wait for a blanking interval prior to their execution. Command formats are shown in table 3. The commands are asserted by performing a write operation to the command register with the appropriate bit pattern as the data byte.

Instantaneous Commands

The instantaneous commands are executed immediately after the trailing edge of the $\overline{WR}$ pulse during which the command is issued. These commands do not affect the state of the RDFLG or READY interrupt/status bits and can be invoked at any time.

Master Reset

This command initializes the AVDC and can be invoked at any time to return the AVDC to its initial state. Upon power-up, two successive master reset commands must be applied to release the AVDC's internal power on circuits. In transparent and shared buffer modes, the CNTRL1 input must be high when the command is issued. The command causes the following:

1. VSYNC and HSYNC are driven low for the duration of the command and BLANK goes high. After command completion, HSYNC and VSYNC will begin operation and BLANK will remain high until a 'display on' command is received.
2. The interrupt and status bits and masks are set to zero, except for the RDFLG flag which is set to a one.
3. The row buffer mode, cursor-off, display-off, and line graphics disable states are set.
4. The initialization register pointer is set to address IR0.
5. IR2[7] is reset.

Load IR Address

This command is used to preset the initialization register pointer with the value 'V' defined by D3-D0. Allowable values are 0 to 14.

Enable Graphics

After invoking this command, the AVDC will increment the MAC to the next consecutive memory address for each scan line even if more than one scan line per row is programmed. This mode can be used for bit-mapped graphics where each location in the display buffer within the defined area contains the bit pattern to be displayed. This command is row buffered and should be asserted during the character row prior to the row where this feature is required. This allows the user to enter and exit graphics mode on character row boundaries.

To perform split screen operations while in graphics mode use SSR2 only.

DADD0/LG is asserted during the trailing edge of BLANK for each scan line while this mode is active.

Disable Graphics

Normal addressing resumes at the next row boundary.

Display Off

Asserts the BLANK output. The DADD0 through DADD13 display address bus outputs can be optionally placed in the three-state condition by setting bit 2 to a '1' when invoking the command.

Display On

Restores normal blanking operation either at the beginning of the next field (bit 2 = 1) or at the beginning of the next scan line (bit 2=0). Also returns the DADD0-DADD13 drivers to their active state.

Cursor Off

Disables cursor operation. Cursor output is placed in the low state.

Cursor On

Enables normal cursor operation.

Reset Interrupt/Status Bits

This command resets the designated bits in the interrupt and status registers. The bit positions correspond to the bit positions in the registers:

Bit 0 — Split 2
Bit 1 — Ready
Bit 2 — Split 1
Bit 3 — Line zero
Bit 4 — Vertical blank

Disable Interrupts

Sets the interrupt mask to zeros for the designated conditions, thus disabling these conditions from being set in the interrupt register and asserting the $\overline{INTR}$ output. Bit position correspondence is as above.

Enable Interrupts

This command writes the associated interrupt mask bits to a one. This enables the corresponding conditions to be set in the interrupt register and asserts the $\overline{INTR}$ output. Bit position correspondence is as above.

Delayed Commands

This group of commands is utilized for the independent buffer mode of operation, although the 'increment cursor' command can also be used in other modes. With the exception of the 'write from cursor to pointer' and 'increment cursor' commands, all the commands of this type will be executed immediately or will be delayed depending on when the command is invoked. If invoked during the active screen time, the command is executed at the next horizontal blanking interval. If invoked during a vertical retrace interval or a 'display off' state, the command is executed immediately.

The 'increment cursor' command is executed immediately after it is issued and requires approximately three $\overline{CCLK}$ periods for completion. The 'write from cursor to pointer' command executes during blanking intervals. The AVDC will execute as many writes as possible during each blanking interval. If the command is not completed during the current blanking interval, the command will be held in suspension during the next active portion of the screen and continues during the next blanking interval until the command is completed.

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In all cases, the AVDC will assert the READY/RDFLG status to signify completion of the delayed command. No other delayed command should be given until the previous delayed command has completed. Therefore, the READY interrupt or RDFLG status flag should be used for handshaking control between the AVDC and CPU when using the delayed commands.

Read/Write at Pointer
Transfers data between the display buffer and the bus interface latch using the address contained in the pointer registers.

Read/Write at Cursor
Transfers data between the display buffer and the bus interface latch using the address contained in the cursor registers.

Increment Cursor
Adds one (modulo 16K) to the cursor address registers.

Read/Write at Cursor and Increment
Transfers data between the display buffer and the bus interface latch using the address contained in the cursor registers and then adds one (modulo 16K) to the cursor address registers.

Write from Cursor to Pointer
Writes the data contained in the bus interface latch into the block of display memory designated by the cursor address and pointer address registers, inclusive. After completion of the command, the pointer address will be unchanged, but the cursor register contents will be equal to the pointer address.

Table 3 AVDC COMMAND FORMATS

D7	D6	D5	D4	D3	D2	D1	D0	Hex	COMMAND
Instantaneous Commands:									
0	0	0	0	0	0	0	0		Master reset
0	0	0	1	V	V	V	V		Load IR pointer with value V (V = 0 to 14)
0	0	1	d	d	d	1	0[1]		Disable graphics
0	0	1	d	d	d	1	1[2]		Enable graphics
0	0	1	d	1	N	d	0[1]		Display off. Float DADD bus if N = 1
0	0	1	d	1	N	d	1[2]		Display on: Next field (N = 1) or scan line (N = 0)
0	0	1	1	d	d	d	0[1]		Cursor off
0	0	1	1	d	d	d	1[2]		Cursor on
0	1	0	N	N	N	N	N		Reset interrupt/status: Bit reset where N = 1
1	0	0	N	N	N	N	N		Disable interrupt: Disable where N = 1
0	1	1	N	N	N	N	N		Enable interrupt: Enables interrupts where N = 1
			V B	L Z	S P 1	R D Y	S P 2		**Interrupt Bit Assignments**
Delayed Commands:								**Hex**	
1	0	1	0	0	1	0	0	A4	Read at pointer address
1	0	1	0	0	0	1	0	A2	Write at pointer address
1	0	1	0	1	0	0	1	A9	Increment cursor address
1	0	1	0	1	1	0	0	AC	Read at cursor address
1	0	1	0	1	0	1	0	AA	Write at cursor address
1	0	1	0	1	1	0	1	AD	Read at cursor address and increment address
1	0	1	0	1	0	1	1	AB	Write at cursor address and increment address
1	0	1	1	1	0	1	1	BB	Write from cursor address to pointer address
1	0	1	1	1	1	0	1	BD	Read from cursor address to pointer address

NOTES:
1. Any combination of these three commands is valid.
2. Any combination of these three commands is valid
3. d = don't care.

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to + 70	°C
Storage temperature	− 65 to + 150	°C
All voltages with respect to ground[3]	− 0.5 to + 6.0	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+ 70°C$, $V_{CC} = 5.0V \pm 5\%$[4,5,6]

	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage		2.0			V
V_{OL}	Output low voltage	$I_{OL} = 2.4mA$			0.4	V
V_{OH}	Output high voltage (except $\overline{INTR}$ output)	$I_{OH} = -200\mu A$	2.4			V
I_{IL}	Input leakage current	$V_{IN} = 0$ to V_{CC}	− 10		10	μA
I_{LL}	Data bus 3-state leakage current	$V_O = 0$ to V_{CC}	− 10		10	μA
I_{OD}	$\overline{INTR}$ open drain output leakage current	$V_O = 0$ to V_{CC}			10	μA
I_{CC}	Power supply current				160	mA

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AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ [4,5,6,7,8]

PARAMETER		TEST CONDITIONS	TENTATIVE LIMITS 2.7MHz Min	TENTATIVE LIMITS 2.7MHz Max	TENTATIVE LIMITS 4.0MHz Min	TENTATIVE LIMITS 4.0MHz Max	UNIT
Bus Timing (Fig. 21)[9]							
t_{AS}	A0-A2 setup time to $\overline{WR}$, $\overline{RD}$ low		30		30		ns
t_{AH}	A0-A2 hold time from $\overline{WR}$, $\overline{RD}$ high		0		0		ns
t_{CS}	$\overline{CE}$ setup time to $\overline{WR}$, $\overline{RD}$ low		0		0		ns
t_{CH}	$\overline{CE}$ hold time from $\overline{WR}$, $\overline{RD}$ high		0		0		ns
t_{RW}	$\overline{WR}$, $\overline{RD}$ pulse width		250		200		ns
t_{DD}	Data valid after $\overline{RD}$ low			200		200	ns
t_{DF}	Data bus floating after $\overline{RD}$ high			100		100	ns
t_{DS}	Data setup time to $\overline{WR}$ high		150		150		ns
t_{DH}	Data hold time from $\overline{WR}$ high		10		5		ns
t_{CC}	High time from $\overline{CE}$ to $\overline{CE}$						
	Consecutive commands		t_{CCP}		t_{CCP}		ns
	Other accesses		300		300		ns
CCLK Timing (Fig 22, 23, 24)							
t_{CCP}	CCLK period		370	10,000	250	10,000	ns
t_{CCH}	$\overline{CCLK}$ high time		125		100		ns
t_{CCL}	$\overline{CCLK}$ low time		125		100		ns
	Output delay from $\overline{CCLK}$ edge						
t_{CCD1}	DADD0-13, MBC		40	175	40	150	ns
t_{CCD2}	BLANK, HSYNC, VSYNC/CSYNC, CURSOR, $\overline{BEXT}$, $\overline{BREQ}$, $\overline{BACK}$, $\overline{BCE}$, $\overline{WDB}$, $\overline{RDB}$[10]		40	225	40	200	ns
Other Timings (Fig 23)							
t_{RDL}	READY/RDFLG low from $\overline{WR}$ high[9]			t_{CCP} + 30		t_{CCP} + 30	ns
t_{BAK}	$\overline{BACK}$ high from $\overline{PBREQ}$ low			225		200	ns
t_{BXT}	$\overline{BEXT}$ high from $\overline{PBREQ}$ high			225		200	ns
t_{IRL}	$\overline{INTR}$ low from $\overline{CCLK}$ low			225		200	ns
t_{IRH}	$\overline{INTR}$ high from $\overline{WR}$, $\overline{RD}$ high[9]			600		600	ns
t_{AC}	ACLL from HSYNC		$3xt_{CCP}$		$3xt_{CCP}$		ns
Row Table Input Timing (Fig. 24)							
t_{DSRT}	Data setup time to $\overline{CCLK}$ low		100		60		ns
t_{DHRT}	Data hold time from $\overline{CCLK}$ low		60		60		ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. All voltage measurements are referenced to ground (GND).
6. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
7. For testing, all input signals swing between 0.4V and 2.4V with a transition time of 20ns maximum. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V as appropriate.
8. Test condition for outputs: $C_L = 150pF$.
9. Timing is illustrated and specified referenced to $\overline{WR}$ and $\overline{RD}$ inputs. Device may also be operated with $\overline{CE}$ as the 'strobing' input. In this case, all timing specifications apply referenced to falling and rising edges of $\overline{CE}$.
10. $\overline{BCE}$, $\overline{WDB}$, and $\overline{RDB}$ delays track each other within 10nsec. Also, these output delays will tend to follow direction (min/max) of DADD0-13 delays.

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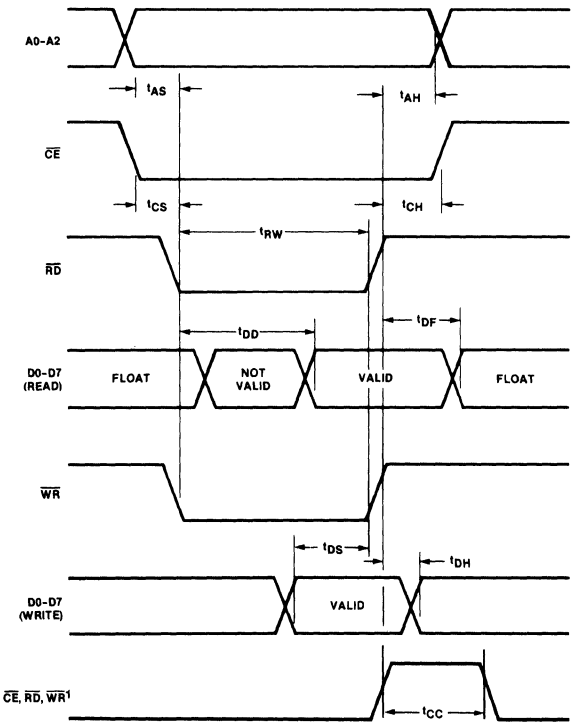
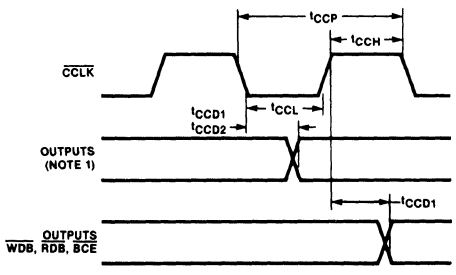


NOTE
1. Any two must be high for t_{CC}.

Figure 21. Bus Timing



NOTES
1. DADD0-DADD13, BLANK, HSYNC, CSYNC/VSYNC, CURSOR, $\overline{BEXT}$, $\overline{BREQ}$, $\overline{BCE}$, MBC, BACK.
2. $\overline{BCE}$ CHANGES STATE ON BOTH $\overline{CCLK}$ EDGES—(see Figures 3 and 4)

Figure 22. $\overline{CCLK}$ Timing

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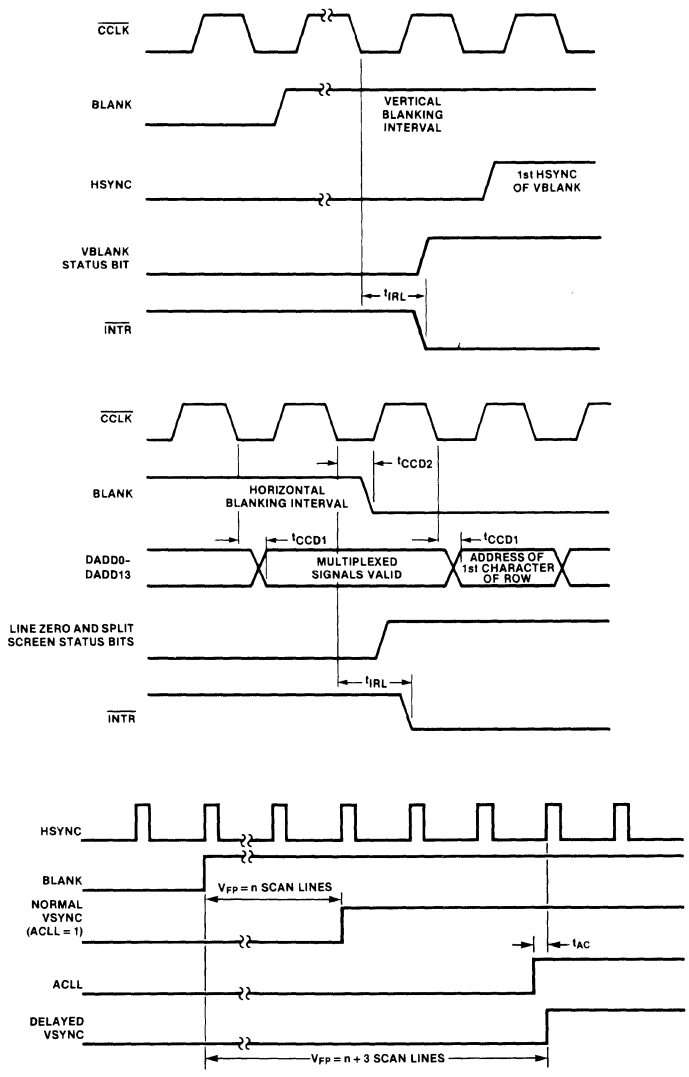

Figure 23. Other Timings

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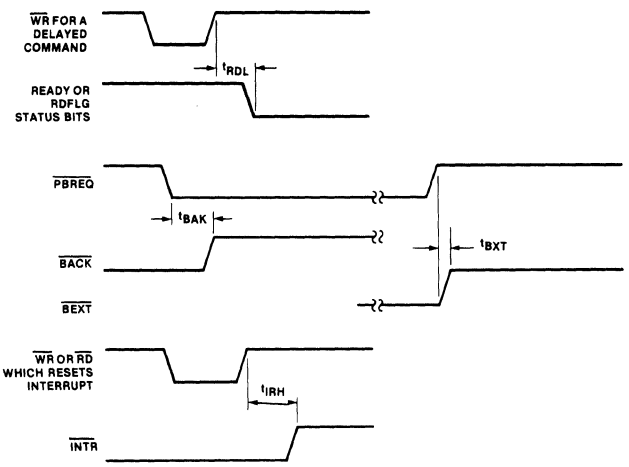

Figure 23. Other Timings (Continued)

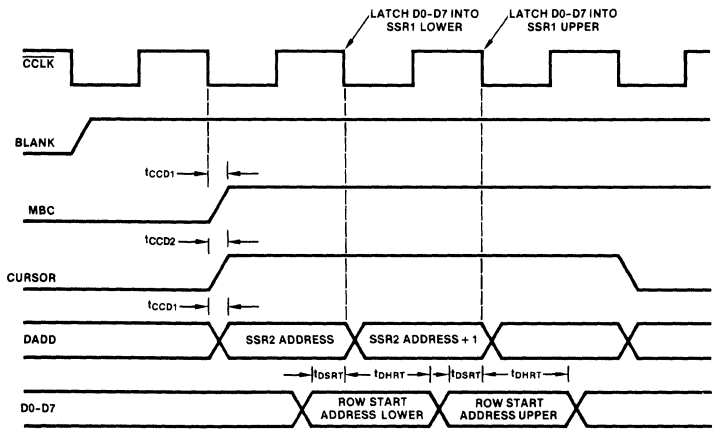

Figure 24. Row Table Fetch I/O Timing

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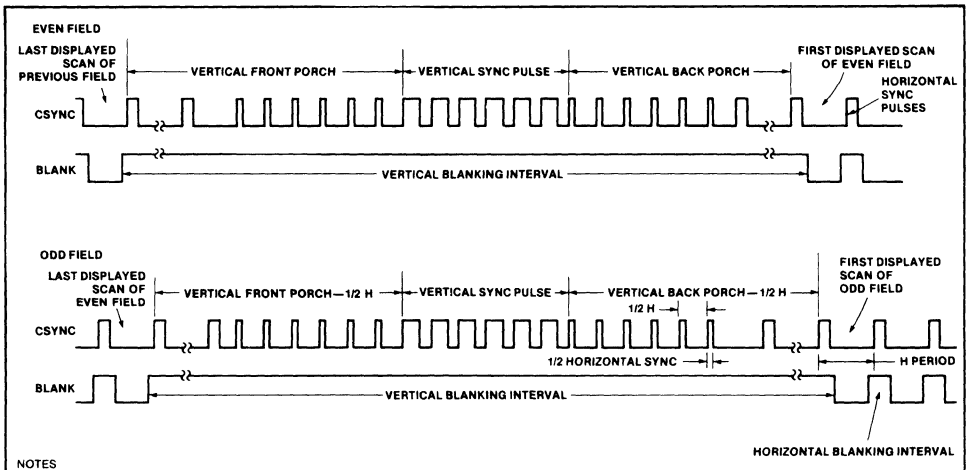
Preview



NOTES
1. In non-interlaced operation the even field is repeated continuously.
2. In interlaced operation the even field alternates with the odd field.

Figure 25. Composite Sync Timing

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DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER (DUART) SCN2681 SERIES

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DESCRIPTION

The Signetics SCN2681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16x clock derived from a programmable counter/timer, or an external 1x or 16x clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruply buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the buffer of the receiving device is full.

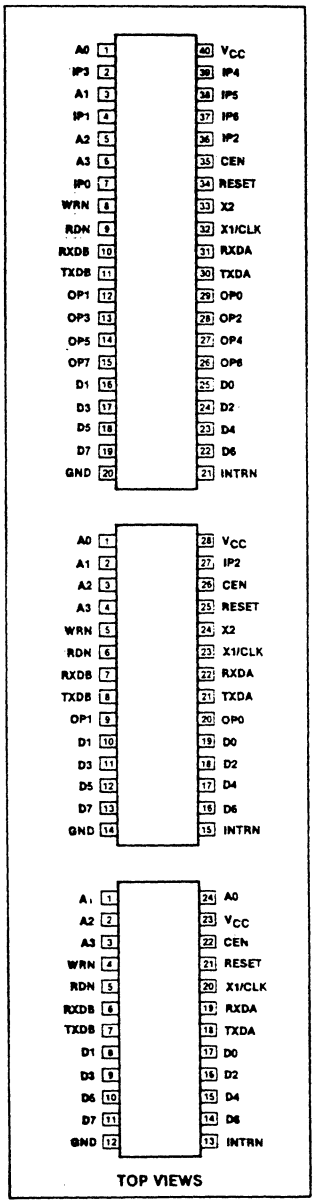
Also provided on the SCN2681 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SCN2681 is available in three package versions to satisfy various system requirements: 40-pin and 28-pin, both 0.6" wide DIPs, and a compact 24-pin, 0.4" wide, DIP.

FEATURES

- Dual full-duplex asynchronous receiver/transmitter
- Quadruple buffered receiver data registers
- Programmable data format
  - —5 to 8 data bits plus parity
  - —Odd, even, no parity or force parity
  - —1, 1.5 or 2 stop bits programmable in 1/16 bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - —18 fixed rates: 50 to 38.4K baud
  - —One user defined rate derived from programmable timer/counter
  - —External 1x or 16x clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - —Normal (full duplex)
  - —Automatic echo
  - —Local loopback
  - —Remote loopback
- Multi-function programmable 16-bit counter/timer
- Multi-function 7-bit input port
  - —Can serve as clock or control inputs
  - —Change of state detection on four inputs
- Multi-function 8-bit output port
  - —Individual bit set/reset capability
  - —Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - —Single interrupt output with eight maskable interrupting conditions
  - —Output port can be configured to provide a total of up to six separate wire-OR'able interrupt outputs
- Maximum data transfer: 1X — 1MB/sec, 16X — 125KB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- TTL compatible
- Single +5V power supply

PIN CONFIGURATION



ORDERING CODE

PACKAGES	V_{CC} = 5V ±5%, T_A = 0°C to 70°C		
	24 Pin[1]	28 Pin[2]	40 Pin[2]
Ceramic DIP	Not available	SCN2681AC1I28	SCN2681AC1I40
Plastic DIP	SCN2681AC1N24	SCN2681AC1N28	SCN2681AC1N40

[1] 400 mil wide DIP
[2] 600 mil wide DIP

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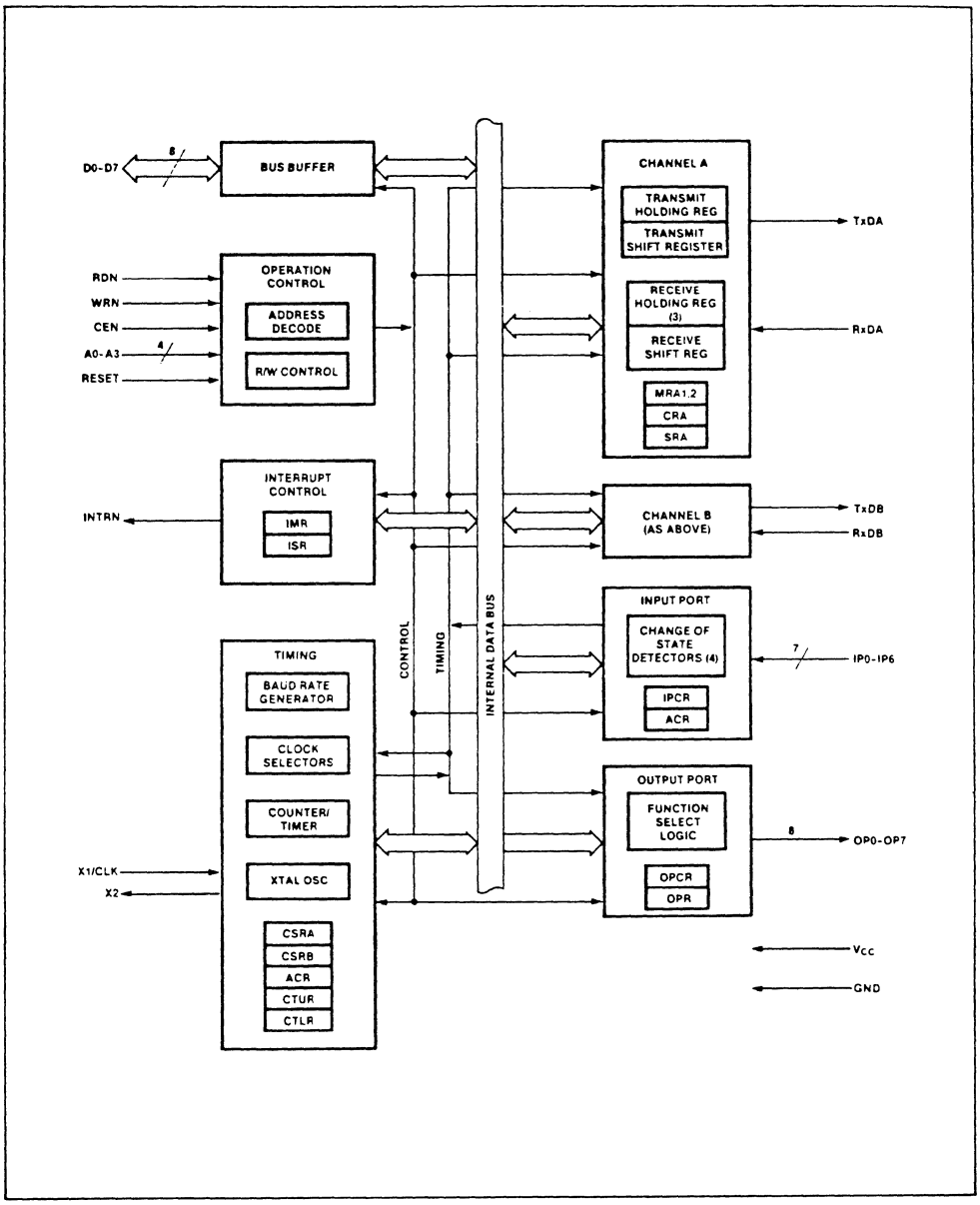
BLOCK DIAGRAM



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PIN DESIGNATION

MNEMONIC	APPLICABLE			TYPE	NAME AND FUNCTION
	40	28	24		
D0-D7	X	X	X	I/O	**Data Bus:** Bidirectional 3-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	X	X	I	**Chip Enable:** Active low input signal. When low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When high, places the D0-D7 lines in the 3-state condition.
WRN	X	X	X	I	**Write Strobe:** When low and CEN is also low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	X	X	I	**Read Strobe:** When low and CEN is also low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0-A3	X	X	X	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	X	X	X	I	**Reset:** A high level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0-OP7 in the high state, stops the counter/timer, and puts channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (high) state.
INTRN	X	X	X	O	**Interrupt Request:** Active low, open drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	X	X	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see figure 5).
X2	X	X		O	**Crystal 2:** Connection for other side of the crystal. Should be connected to ground if a crystal is not used. When a crystal is used, a capacitor must be connected from this pin to ground (see figure 5).
RxDA	X	X	X	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
RxDB	X	X	X	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
TxDA	X	X	X	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
TxDB	X	X	X	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
OP0	X	X		O	**Output 0:** General purpose output, or channel A request to send (RTSAN, active low). Can be deactivated on receive or transmit.
OP1	X	X		O	**Output 1:** General purpose output, or channel B request to send (RTSBN, active low). Can be deactivated on receive or transmit.
OP2	X			O	**Output 2:** General purpose output, or channel A transmitter 1X or 16X clock output, or channel A receiver 1X clock output.
OP3	X			O	**Output 3:** General purpose output, or open drain, active low counter/timer output, or channel B transmitter 1X clock output, or channel B receiver 1X clock output.
OP4	X			O	**Output 4:** General purpose output, or channel A open drain, active low, RxRDYA/FFULLA output.
OP5	X			O	**Output 5:** General purpose output, or channel B open drain, active low, RxRDYB/FFULLB output.
OP6	X			O	**Output 6:** General purpose output, or channel A open drain, active low, TxRDYA output.
OP7	X			O	**Output 7:** General purpose output, or channel B open drain, active low, TxRDYB output.
IP0	X			I	**Input 0:** General purpose input, or channel A clear to send active low input (CTSAN).
IP1	X			I	**Input 1:** General purpose input, or channel B clear to send active low input (CTSBN).
IP2	X	X		I	**Input 2:** General purpose input, or counter/timer external clock input.
IP3	X			I	**Input 3:** General purpose input, or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.

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PIN DESIGNATION (Continued)

MNEMONIC	APPLICABLE			TYPE	NAME AND FUNCTION
	40	28	24		
IP4	X			I	**Input 4:** General purpose input, or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	X			I	**Input 5:** General purpose input, or channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	X			I	**Input 6:** General purpose input or channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	X	X	X	I	**Power Supply:** +5V supply input
GND	X	X	X	I	**Ground**

BLOCK DIAGRAM

The 2681 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications channels A and B, input port and output port. Refer to the block diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data busses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer.

Interrupt Control

A single active low interrupt output (INTRN) is provided which is activated upon the occurence of any of eight internal events. Associated with the interrupt system are the interrupt mask register (IMR) and the interrupt status register (ISR). The IMR may be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions.

Outputs OP3–OP7 can be programmed to provide discrete interrupt outputs for the transmitters, receivers, and counter/timer.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the baud rate generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or an external timing signal.

The counter/timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the 2681 comprises a full duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

Input Port

The inputs to this unlatched 7-bit port can be read by the CPU by performing a read operation at address D_{16}. A high input results in a logic 1 while a low input results in a logic 0. D_7 will always be read as a logic 1. The pins of this port can also serve as auxiliary inputs to certain portions of the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1, and IP0. A high-to-low or low-to-high transition of these inputs lasting longer than 25–50μs will set the corresponding bit in the input port will change register. The bits are cleared when the register is read by the CPU. Any change of state can also be programmed to generate an interrupt to the CPU.

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Output Port

The 8-bit multi-purpose output port can be used as a general purpose output port, in which case the outputs are the complements of the output port register (OPR). OPR[n] = 1 results in OP[n] = low and vice-versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address E_{16} with the accompanying data specifying the bits to be set (1 = set, 0 = no change). Likewise, a bit is reset by a write at address F_{16} with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also individually assigned specific functions by appropriate programming of the channel A mode registers (MR1A, MR2A), the channel B mode registers (MR1B, MR2B), and the output port configuration register (OPCR).

OPERATION

Transmitter

The 2681 is conditioned to transmit data when the transmitter is enabled through the command register. The 2681 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the transmit holding register (THR), the above conditions are negated. Data is transferred from the holding register to the transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains high and the TxEMT bit in the status register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR. If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enabled, the CTSN input must be low in order for the character to be transmitted. If it goes high in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

Receiver

The 2681 is conditioned to receive data when enabled through the command register. The receiver looks for a high to low (mark to space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled high, the start bit is invalid and the search for a valid start bit begins again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and the parity bit (if any) have been assembled, and one stop bit has been detected. The least sigificant bit is received first. The data is then transferred to the receive holding register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than eight bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, overrun error and received break state (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a high condition for at least one-half bit time before a search for the next start bit begins.

The RHR consists of a first-in-first-out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected: the character previously in the shift register is lost and the overrun error status bit (SR[4]) will be set upon receipt of the start bit of the new (overruning) character.

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the

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receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

Multidrop Mode

The DUART is equipped with a wake up mode used for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for channels A and B respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wake-up' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, an address/data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data, while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receiver is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems. For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1x by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1x switches the pointer to MR2x. The pointer then remains at MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset to MR1x as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to table 2 for register bit descriptions.

MR1A — Channel A Mode Register 1

MR1A is accessed when the channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] — Channel A Receiver Request-to-Send Control — This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1A[6] — Channel A Receiver Interrupt Select — This bit selects either the channel A receiver ready status (RXRDY) or the channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

MR1A[5] — Channel A Error Mode Select — This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break) for channel A. In the 'character' mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these bits is the ac-

Table 1 2681 REGISTER ADDRESSING

A3	A2	A1	A0	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Reg. A (CSRA)
0	0	1	0	*Reserved*	Command Register A (CRA)
0	0	1	1	RX Holding Register A (RHRA)	TX Holding Register A (THRA)
0	1	0	0	Input Port Change Reg. (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Reg. (ISR)	Interrupt Mask Reg. (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Register (CTUR)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Reg. B (CSRB)
1	0	1	0	*Reserved*	Command Register B (CRB)
1	0	1	1	RX Holding Register B (RHRB)	TX Holding Register B (THRB)
1	1	0	0	*Reserved*	*Reserved*
1	1	0	1	Input Port	Output Port Conf. Reg. (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

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Table 2 REGISTER BIT FORMATS

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	RX RTS CONTROL	RX INT SELECT	ERROR MODE	PARITY MODE		PARITY TYPE	BITS PER CHAR.	
MR1A MR1B	0 = no 1 = yes	0 = RXRDY 1 = FFULL	0 = char 1 = block	00 = with parity 01 = force parity 10 = no parity 11 = multi-drop mode		0 = even 1 = odd	00 = 5 01 = 6 10 = 7 11 = 8	

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	CHANNEL MODE		Tx RTS CONTROL	CTS ENABLE Tx	STOP BIT LENGTH*			
MR2A MR2B	00 = Normal 01 = Auto echo 10 = Local loop 11 = Remote loop		0 = no 1 = yes	0 = no 1 = yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

*Add 0.5 to values shown for 0-7 if channel is programmed for 5 bits/char.

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CSRA	RECEIVER CLOCK SELECT				TRANSMITTER CLOCK SELECT			
CSRB	See text				See text			

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CRA CRB	not used— must be 0	MISCELLANEOUS COMMANDS			DISABLE Tx	ENABLE Tx	DISABLE Rx	ENABLE Rx
		See text			0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	RECEIVED BREAK	FRAMING ERROR	PARITY ERROR	OVERRUN ERROR	TxEMT	TxRDY	FFULL	RxRDY
SRA SRB	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes

*These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits (7:5) from the top of the FIFO together with bits 4:0. These bits are cleared by a 'reset error status' command. In character mode they are discarded when the corresponding data character is read from the FIFO.

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	OP7	OP6	OP5	OP4	OP3		OP2	
OPCR	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB (1X) 11 = RxCB (1X)		00 = OPR[2] 01 = TxCA (16X) 10 = TxCA (1X) 11 = RxCA (1X)	

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	BRG SET SELECT	COUNTER/TIMER MODE AND SOURCE			DELTA IP3 INT	DELTA IP2 INT	DELTA IP1 INT	DELTA IP0 INT
ACR	0 = set1 1 = set2	See table 4			0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	DELTA IP3	DELTA IP2	DELTA IP1	DELTA IP0	IP3	IP2	IP1	IP0
IPCR	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = low 1 = high	0 = low 1 = high	0 = low 1 = high	0 = low 1 = high

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Table 2 REGISTER BIT FORMATS (Continued)

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ISR	INPUT PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IMR	IN. PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CTUR	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CTLR	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

cumulation (logical OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for channel A was issued.

MR1A[4:3] — Channel A Parity Mode Select — If 'with parity' or 'force parity' is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR1A[4:3] = 11 selects channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] — Channel A Parity Type Select — This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] — Channel A Bits per Character Select — This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2A — Channel A Mode Register 2

MR2A is accessed when the channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] — Channel A Mode Select — Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held high.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is relocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.

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3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity bit is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected, the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop bit has been retransmitted.

MR2A[5] — Channel A Transmitter Request-to-Send Control — This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 causes OPR[0] to be reset automatically one bit time after the characters in the channel A transmit shift register and in the THR, if any, are completely transmitted, including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Assert RTSAN: OPR[0] = 1.
4. Send message.
5. Disable transmitter after the last character is loaded into the channel A THR.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

MR2A[4] — Channel A Clear-to-Send Control — If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IP0) each time it is ready to send a character. If IP0 is asserted (low), the character is transmitted. If it is negated (high), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character.

MR2A[3:0] — Channel A Stop Bit Length Select — This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16 bit. The receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled) in all cases.

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

MR1B — Channel B Mode Register 1

MR1B is accessed when the channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to the bit definitions for MR1A, except that all control actions apply to the channel B receiver and transmitter and the corresponding inputs and outputs.

MR2B — Channel B Mode Register 2

MR2B is accessed when the channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for this register are identical to the bit definitions for MR2A, except that all control actions apply to the channel B receiver and transmitter and the corresponding inputs and outputs.

CSRA — Channel A Clock Select Register

CSRA[7:4] — Channel A Receiver Clock Select — This field selects the baud rate clock for the channel A receiver as follows:

				Baud Rate CLOCK = 3.6864MHz	
CSRA[7:4]				ACR[7] = 0	ACR[7] = 1
0	0	0	0	50	75
0	0	0	1	110	110
0	0	1	0	134.5	134.5
0	0	1	1	200	150
0	1	0	0	300	300
0	1	0	1	600	600
0	1	1	0	1,200	1,200
0	1	1	1	1,050	2,000
1	0	0	0	2,400	2,400
1	0	0	1	4,800	4,800
1	0	1	0	7,200	1,800
1	0	1	1	9,600	9,600
1	1	0	0	38.4K	19.2K
1	1	0	1	Timer	Timer
1	1	1	0	IP4—16X	IP4—16X
1	1	1	1	IP4—1X	IP4—1X

The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.

CSRA[3:0] — Channel A Transmitter Clock Select — This field selects the baud rate clock for the channel A transmitter. The field definition is as per CSRA[7:4] except as follows:

				Baud Rate	
CSRA[3:0]				ACR[7] = 0	ACR[7] = 1
1	1	1	0	IP3—16X	IP3—16X
1	1	1	1	IP3—1X	IP3—1X

The transmitter clock is always a 16X clock except for CSRA[3:0] = 1111.

CSRB — Channel B Clock Select Register

CSRB[7:4] — Channel B Receiver Clock Select — This field selects the baud rate clock for the channel B receiver. The field definition is as per CSRA[7:4] except as follows:

				Baud Rate	
CSRB[7:4]				ACR[7] = 0	ACR[7] = 1
1	1	1	0	IP6—16X	IP6—16X
1	1	1	1	IP6—1X	IP6—1X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] — Channel B Transmitter Clock Select — This field selects the baud rate clock for the channel B transmitter. The field definition is as per CSRA[7:4] except as follows:

				Baud Rate	
CSRB[3:0]				ACR[7] = 0	ACR[7] = 1
1	1	1	0	IP5—16X	IP5—16X
1	1	1	1	IP5—1X	IP5—1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

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CRA — Channel A Command Register

CRA is a register used to supply commands to channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

CRA[6:4] — Channel A Miscellaneous Commands — The encoded value of this field may be used to specify a single command as follows:

CRA[6:4]	COMMAND
0 0 0	No command.
0 0 1	Reset MR pointer. Causes the channel A MR pointer to point to MR1.
0 1 0	Reset receiver. Resets the channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.
0 1 1	Reset transmitter. Resets the channel A transmitter as if a hardware reset had been applied.
1 0 0	Reset error status. Clears the channel A Received Break, Parity Error, Framing Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE, and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.
1 0 1	Reset channel A break change interrupt. Causes the channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.
1 1 0	Start break. Forces the TXDA output low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any others loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.
1 1 1	Stop Break. The TXDA line will go high (marking) within two bit times. TXDA will remain high for one bit time before the next character, if any, is transmitted.

CRA[3] — Disable Channel A Transmitter — This command terminates transmitter operation and resets the TxRDY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] — Enable Channel A Transmitter — Enables operation of the channel A transmitter. The TxRDY status bit will be asserted.

CRA[1] — Disable Channel A Receiver — This command terminates operation of the receiver immediately — a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] — Enable Channel A Receiver — Enables operation of the channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start-bit state.

CRB — Channel B Command Register

CRB is a register used to supply commands to channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, except that all control actions apply to the channel B receiver and transmitter and the corresponding inputs and outputs.

SRA — Channel A Status Register

SRA[7] — Channel A Received Break — This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line returns to the marking state for at least one-half a bit time (two successive edges of the internal or external 1x clock).

When this bit is set, the channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

SRA[6] — Channel A Framing Error — This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SRA[5] — Channel A Parity Error — This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multidrop mode the parity error bit stores the received A/D bit.

SRA[4] — Channel A Overrun Error — This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

SRA[3] — Channel A Transmitter Empty (TxEMTA) — This bit will be set when the channel A transmitter underruns, i.e., both the transmit holding register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled.

SRA[2] — Channel A Transmitter Ready (TxRDYA) — This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, viz., characters loaded into the THR while the transmitter is disabled will not be transmitted.

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SRA[1] — Channel A FIFO Full (FFULLA) — This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SRA[0] — Channel A Receiver Ready (RxRDYA) — This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR, if after this read there are no more characters still in the FIFO.

SRB — Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR — Output Port Configuration Register

OPCR[7] — OP7 Output Select — This bit programs the OP7 output to provide one of the following:

- The complement of OPR[7]
- The channel B transmitter interrupt output, which is the complement of TxRDYB. When in this mode OP7 acts as an open collector output. Note that this output is not masked by the contents of the IMR.

OPCR[6] — OP6 Output Select — This bit programs the OP6 output to provide one of the followng:

- The complement of OPR[6]
- The channel A transmitter interrupt output, which is the complement of TxRDYA. When in this mode OP6 acts as an open collector output. Note that this output is not masked by the contents of the IMR.

OPCR[5] — OP5 Output Select — This bit programs the OP5 output to provide one of the following:

- The complement of OPR[5]
- The channel B receiver interrupt output, which is the complement of ISR[5]. When in this mode OP5 acts as an open collector output. Note that this output is not masked by the contents of the IMR.

OPCR[4] — OP4 Output Select — This bit programs the OP4 output to provide one of the following:

- The complement of OPR[4]
- The channel A receiver interrupt output, which is the complement of ISR[1]. When in this mode OP4 acts as an open collector output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] — OP3 Output Select — This field programs the OP3 output to provide one of the following:

- The complement of OPR[3]
- The counter/timer output, in which case OP3 acts as an open collector output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains high until terminal count is reached, at which time it goes low. The output returns to the high state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
- The 1X clock for the channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] — OP2 Output Select — This field programs the OP2 output to provide one of the following:

- The complement of OPR[2]
- The 16X clock for the channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
- The 1X clock for the channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

ACR — Auxiliary Control Register

ACR[7] — Baud Rate Generator Set Select — This bit selects one of two sets of baud rates to be generated by the BRG:

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05K, 1.2K, 2.4K, 4.8K, 7.2K, 9.6K, and 38.4K baud.

Set 2: 75, 110, 134.5, 150, 300, 600, 1.2K, 1.8K, 2.0K, 2.4K, 4.8K, 9.6K, and 19.2K baud.

The selected set of rates is available for use by the channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in table 3.

Table 3 BAUD RATE GENERATOR CHARACTERISTICS CRYSTAL OR CLOCK = 3.6864MHz

NOMINAL RATE (BAUD)	ACTUAL 16X CLOCK (KHz)	ERROR (PERCENT)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2K	307.2	0
38.4K	614.4	0

NOTE:
Duty cycle of 16X clock is 50% ± 1%.

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ACR[6:4]—Counter/Timer Mode and Clock Source Select — This field selects the operating mode of the counter/timer and its clock source as shown in table 4.

ACR[3:0] — IP3, IP2, IP1, IP0 Change of State Interrupt Enable — This field selects which bits of the Input Port Change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state, the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7]= 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

Table 4 ACR [6:4] FIELD DEFINITION

ACR[6:4]	MODE	CLOCK SOURCE
0 0 0	Counter	External (IP2)
0 0 1	Counter	TXCA — 1X clock of channel A transmitter
0 1 0	Counter	TXCB — 1X clock of channel B transmitter
0 1 1	Counter	Crystal or external clock (X1/CLK) divided by 16
1 0 0	Timer	External (IP2)
1 0 1	Timer	External (IP2) divided by 16
1 1 0	Timer	Crystal or external clock (X1/CLK)
1 1 1	Timer	Crystal or external clock (X1/CLK) divided by 16

IPCR — Input Port Change Register

IPCR[7:4] — IP3, IP2, IP1, IP0 Change of State — These bits are set when a change of state, as defined in the Input Port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register.

The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] — IP3, IP2, IP1, IP0 Current State — These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR — Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR — the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to 00_{16} when the DUART is reset.

ISR[7] — Input Port Change Status — This bit is a '1' when a change of state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] — Channel B Change in Break — This bit, when set, indicates that the channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a channel B 'reset break change interrupt' command.

ISR[5] — Channel B Receiver Ready or FIFO Full — The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the channel B FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[4] — Channel B Transmitter Ready — This bit is a duplicate of TxRDYB (SRB[2]).

ISR[3] — Counter Ready — In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] — Channel A Change in Break — This bit, when set, indicates that the channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a channel A 'reset break change interrupt' command.

ISR[1] — Channel A Receiver Ready or FIFO Full — The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the channel A FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[0] — Channel A Transmitter Ready — This bit is a duplicate of TxRDYA (SRA[2]).

IMR — Interrupt Mask Register

The programming of this register selects which bits in the ISR cause an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3-OP7 or the reading of the ISR.

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CTUR and CTLR — Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs respectively of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is 0002_{16}. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. In this mode the C/T runs continuously. Receipt of a start counter command (read with A3–A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3–A0 = 1111). The command, however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count (0000_{16}), the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains high until terminal count is reached, at which time it goes low. The output returns to the high state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8-bits to the upper 8-bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	−65 to +150	°C
All voltages with respect to ground[3]	−0.5 to +6.0	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$[4,5,6]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)		2.0			V
V_{IH}	Input high voltage (X1/CLK)		4.0			V
V_{OL}	Output low voltage	$I_{OL} = 2.4mA$			0.4	V
V_{OH}	Output high voltage (except o.c. outputs)	$I_{OH} = -400\mu A$	2.4			V
I_{IL}	Input leakage current	$V_{IN} = 0$ to V_{CC}	−10		10	μA
I_{LL}	Data bus 3-state leakage current	$V_O = 0$ to V_{CC}	−10		10	μA
I_{OC}	Open collector output leakage current	$V_O = 0$ to V_{CC}	−10		10	μA
I_{CC}	Power supply current				150	mA

NOTES:
4. Parameters are valid over specified temperature range.
5. All voltage measurements are referenced to ground (GND). For testing, all input signals swing between 0.4V and 2.4V with a transition time of 20ns maximum. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V as appropriate.
6. Typical values are at +25°C, typical supply voltages, and typical processing parameters.

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DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER (DUART) SCN2681 SERIES

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AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$[4,5,6,7]

PARAMETER		TENTATIVE LIMITS			UNIT
		Min	Typ	Max	
Reset Timing (figure 1)					
t_{RES}	RESET pulse width	1.0			µs
Bus Timing (figure 2)[8]					
t_{AS}	A0–A3 setup time to RDN, WRN low	10			ns
t_{AH}	A0–A3 hold time from RDN, WRN high	0			ns
t_{CS}	CEN setup time to RDN, WRN low	0			ns
t_{CH}	CEN hold time from RDN, WRN high	0			ns
t_{RW}	WRN, RDN pulse width	225			ns
t_{DD}	Data valid after RDN low			175	ns
t_{DF}	Data bus floating after RDN high			100	ns
t_{DS}	Data setup time before WRN high	100			ns
t_{DH}	Data hold time after WRN high	20			ns
t_{RWD}	High time between READs and/or WRITEs[9,10]	200			ns
Port Timing (figure 3)[8]					
t_{PS}	Port input setup time before RDN low	0			ns
t_{PH}	Port input hold time after RDN high	0			ns
t_{PD}	Port output valid after WRN high			400	ns
Interrupt Timing (figure 4)					
t_{IR}	INTRN (or OP3–OP7 when used as interrupts) high from:				
	Read RHR (RXRDY/FFULL interrupt)			300	ns
	Write THR (TXRDY interrupt)			300	ns
	Reset command (delta break interrupt)			300	ns
	Stop C/T command (counter interrupt)			300	ns
	Read IPCR (input port change interrupt)			300	ns
	Write IMR (clear of interrupt mask bit)			300	ns
Clock Timing (figure 5)					
t_{CLK}	X1/CLK high or low time	100			ns
f_{CLK}	X1/CLK frequency	2.0	3.6864	4.0	MHz
t_{CTC}	CTCLK (IP2) high or low time	100			ns
f_{CTC}	CTCLK (IP2) frequency	0		4.0	MHz
t_{RX}	RxC high or low time	220			ns
f_{RX}	RxC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
t_{TX}	TxC high or low time	220			ns
f_{TX}	TxC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
Transmitter Timing (figure 6)					
t_{TXD}	TxD output delay from TxC low			350	ns
t_{TCS}	TxC output skew from TxD output data	0		150	ns
Receiver Timing (figure 7)					
t_{RXS}	RxD data setup time to RXC high	240			ns
t_{RXH}	RxD data hold time from RXC high	200			ns

NOTES:
4. Parameters are valid over specified temperature range.
5. All voltage measurements are referenced to ground (GND). For testing, all input signals swing between 0.4V and 2.4V with a transition time of 20ns maximum. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V as appropriate.
6. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
7. Test condition for outputs $C_L = 150pF$, except interrupt outputs. Test condition for interrupt outputs: $C_L = 50pF$, $R_L = 2.7K$ ohm to V_{CC}.
8. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the "strobing" input. In this case, all timing specifications apply referenced to the falling and rising edges of CEN.
9. If CEN is used as the "strobing" input, this parameter defines the minimum high time between one CEN and the next.
10. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.

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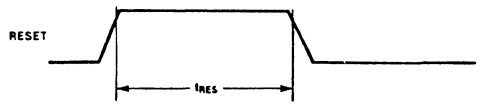

Figure 1. Reset Timing

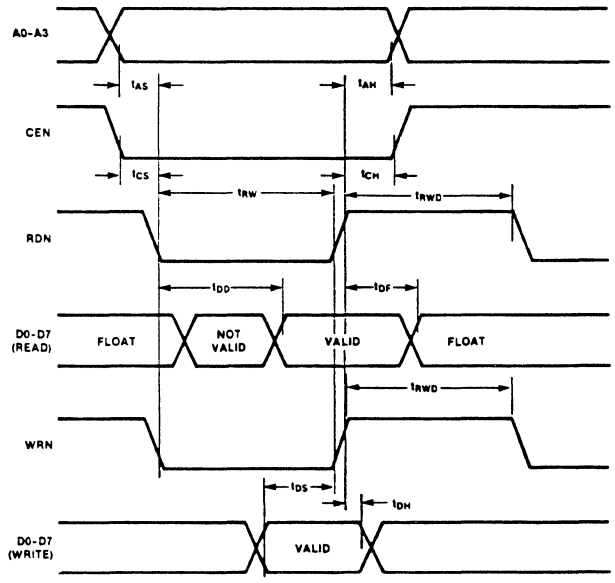

Figure 2. Bus Timing

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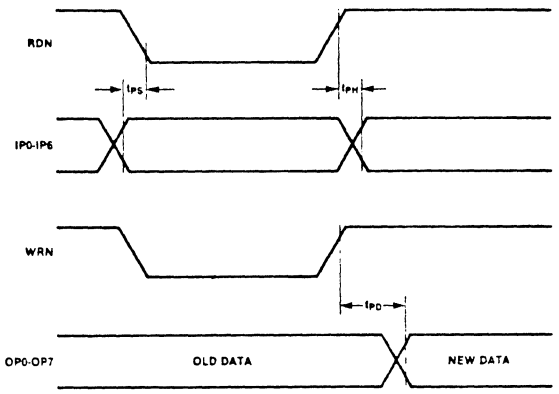

Figure 3. Port Timing

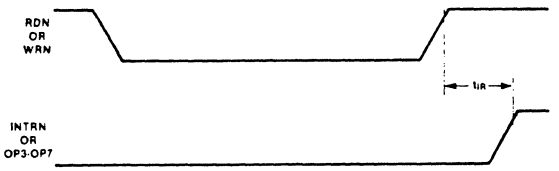

Figure 4. Interrupt Timing

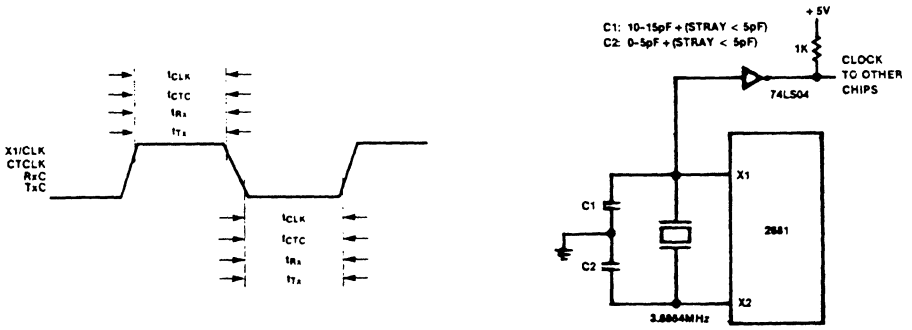

Figure 5. Clock Timing

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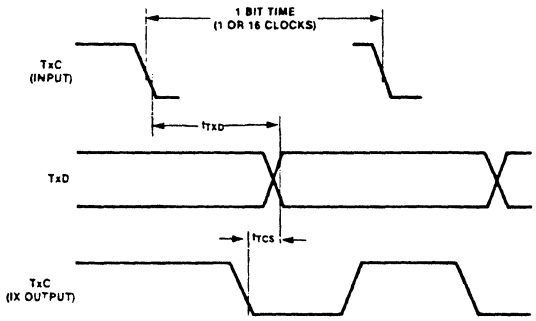

Figure 6. Transmit

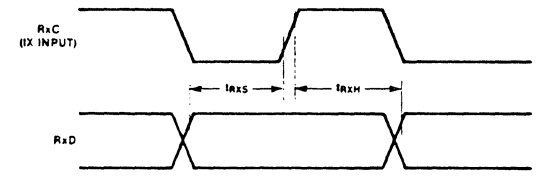

Figure 7. Receive

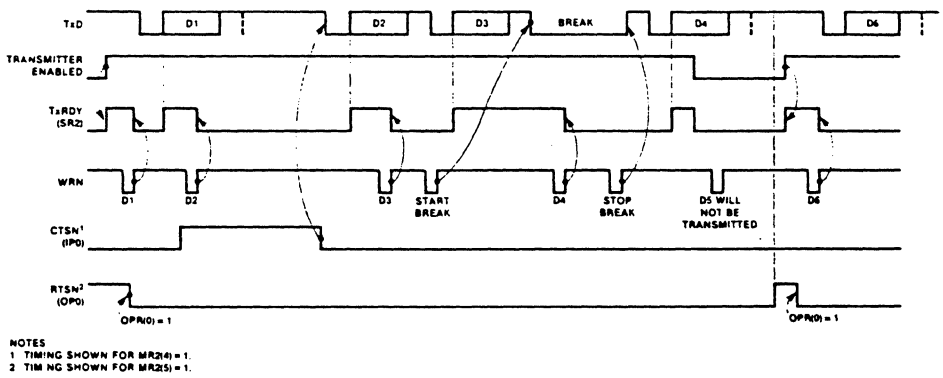

Figure 8. Transmitter Timing

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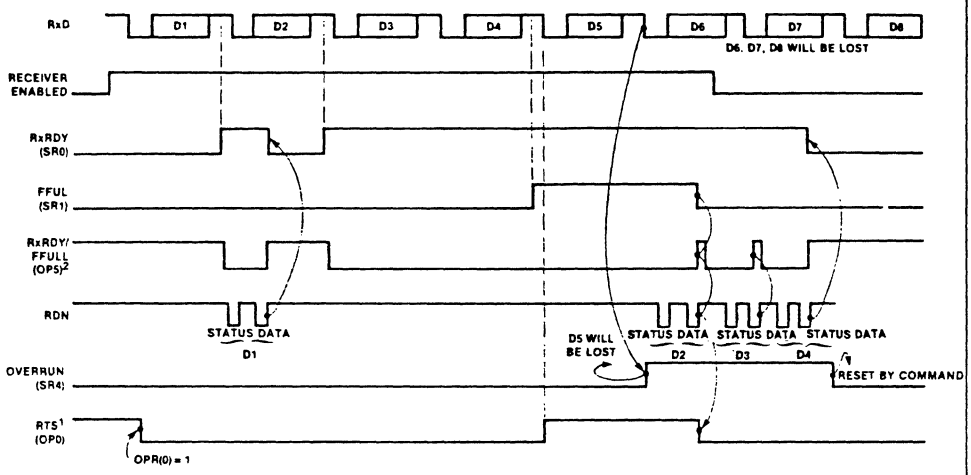

NOTES
1. TIMING SHOWN FOR MR1(7) = 1.
2. SHOWN FOR OPCR(4) = 1 AND MR(6) = 0.

Figure 9. Receiver Timing

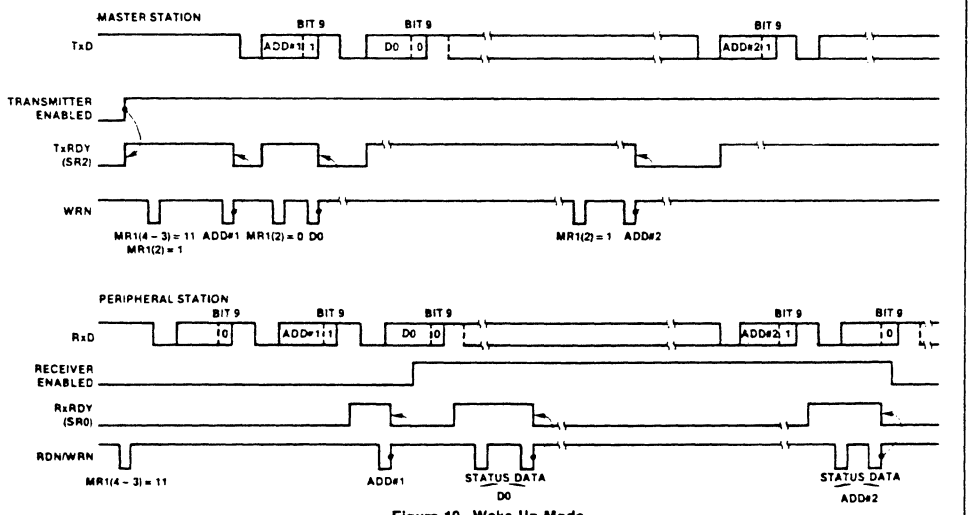

Figure 10. Wake Up Mode

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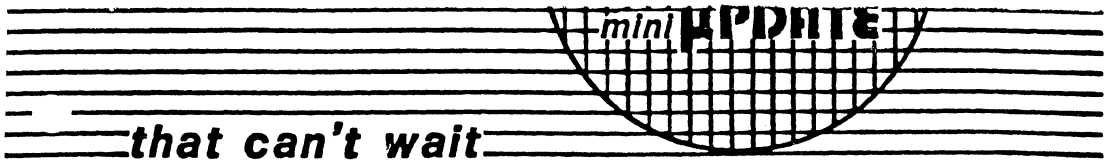

SCN2681/SCN68681

AC PARAMETER UPDATE

CHARACTERIZATION OF THE SCN2681 AND SCN68681 DEVICES INDICATES THAT MODIFICATIONS ARE REQUIRED TO THE AC ELECTRICAL CHARACTERISTICS FOR THESE DEVICES.

ATTACHED IS A SUMMARY OF THE PARAMETERS CHANGED AS WELL AS THE REVISED AC ELECTRICAL CHARACTERISTICS AS THEY WILL APPEAR IN THE NEXT PRINTING OF THESE DATA SHEETS AND IN THE 1983 DATA MANUAL.

PLEASE CONVEY THESE CHANGES TO YOUR CUSTOMERS. ALL FUTURE SHIPMENTS OF THESE DEVICES WILL BE GUARANTEED TO THESE SPECS ONLY.

ALSO ATTACHED IS AN APPLICATION BRIEF PERTAINING TO THE CRYSTAL OPERATION FOR THE SCN2681/SCN68681.

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MICROPROCESSOR DATA SHEET/MANUAL CHANGE NOTICE

DEVICE REFERENCE DOCUMENT	PAGE	CHANGE		
SCN2681 Data Sheet (7/82) and 1983 Data Manual	14 1-81	Parameter	From	To
		t_{DD} (max)	150	175
		t_{DH} (min)	10	20
		t_{PD} (max)	300	400
		t_{TXD} (max)	300	350
		t_{TCS} (max)	125	150
		t_{RXS} (min)	200	240
SCN68681 Data Sheet (4/82) and 1983 Data Manual	15 4-168	Parameter	From	To
		t_{DD} (max)	150	175
		t_{DF} (max)	90	100
		t_{DH} (min)	0	20
		t_{DCR} (max)	50	125
		t_{DCW} (max)	30	125
		t_{DAH} (max)	80	100
		t_{DAT} (max)	100	125
		t_{CSC} (min)	30	90
		t_{CTC} (min)	200	100
		f_{CTC} (max)	2.0	4.0
		t_{TCS} (min/typ/max)	-75/0/75	-/-/150
		t_{RXS} (min)	200	240

PRELIMINARY

DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER (DUART) SCN2681 SERIES

Preliminary

AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$[4,5,6,7]

PARAMETER		TENTATIVE LIMITS			UNIT
		Min	Typ	Max	
Reset Timing (figure 1)					
t_{RES}	RESET pulse width	1.0			µs
Bus Timing (figure 2)[8]					
t_{AS}	A0–A3 setup time to RDN, WRN low	10			ns
t_{AH}	A0–A3 hold time from RDN, WRN high	0			ns
t_{CS}	CEN setup time to RDN, WRN low	0			ns
t_{CH}	CEN hold time from RDN, WRN high	0			ns
t_{RW}	WRN, RDN pulse width	225			ns
t_{DD}	Data valid after RDN low			175	ns
t_{DF}	Data bus floating after RDN high			100	ns
t_{DS}	Data setup time before WRN high	100			ns
t_{DH}	Data hold time after WRN high	20			ns
t_{RWD}	High time between READs and/or WRITEs[9,10]	200			ns
Port Timing (figure 3)[8]					
t_{PS}	Port input setup time before RDN low	0			ns
t_{PH}	Port input hold time after RDN high	0			ns
t_{PD}	Port output valid after WRN high			400	ns
Interrupt Timing (figure 4)					
t_{IR}	INTRN (or OP3–OP7 when used as interrupts) high from:				
	Read RHR (RXRDY/FFULL interrupt)			300	ns
	Write THR (TXRDY interrupt)			300	ns
	Reset command (delta break interrupt)			300	ns
	Stop C/T command (counter interrupt)			300	ns
	Read IPCR (input port change interrupt)			300	ns
	Write IMR (clear of interrupt mask bit)			300	ns
Clock Timing (figure 5)					
t_{CLK}	X1/CLK high or low time	100			ns
f_{CLK}	X1/CLK frequency	2.0	3.6864	4.0	MHz
t_{CTC}	CTCLK (IP2) high or low time	100			ns
f_{CTC}	CTCLK (IP2) frequency	0		4.0	MHz
t_{RX}	RxC high or low time	220			ns
f_{RX}	RxC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
t_{TX}	TxC high or low time	220			ns
f_{TX}	TxC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
Transmitter Timing (figure 6)					
t_{TXD}	TxD output delay from TxC low			350	ns
t_{TCS}	TxC output skew from TxD output data	0		150	ns
Receiver Timing (figure 7)					
t_{RXS}	RxD data setup time to RXC high	240			ns
t_{RXH}	RxD data hold time from RXC high	200			ns

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DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER (DUART) SCN68681

Preliminary

AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$[4,5,6,7]

PARAMETER		TENTATIVE LIMITS			UNIT
		Min	Typ	Max	
Reset Timing (figure 1)					
t_{RES}	RESETN pulse width	1.0			µs
Bus Timing (figures 2, 3, 4)					
t_{AS}	A1-A4 setup time to CSN low	10			ns
t_{AH}	A1-A4 hold time from CSN low	0			ns
t_{RWS}	RWN setup time to CSN low	0			ns
t_{RWH}	RWN holdup time to CSN high	0			ns
t_{CSW}[8]	CSN high pulse width	160			ns
t_{CSD}[9]	CSN or IACKN high from DTACKN low	20			ns
t_{DD}	Data valid from CSN or IACKN low			175	ns
t_{DF}	Data bus floating from CSN or IACKN high			100	ns
t_{DS}	Data setup time to CLK high	100			ns
t_{DH}	Data hold time from CSN high	0			ns
t_{DAL}	DTACKN low from read data valid	0			ns
t_{DCR}	DTACKN low (read cycle) from CLK high			125	ns
t_{DCW}	DTACKN low (write cycle) from CLK high			125	ns
t_{DAH}	DTACKN high from CSN or IACKN high			100	ns
t_{DAT}	DTACKN high impedance from CSN or IACKN high			125	ns
t_{CSC}[10]	CSN or IACKN setup time to clock high	90			ns
Port Timing (figure 5)					
t_{PS}	Port input setup time to RDN low	0			ns
t_{PH}	Port input hold time from RDN high	0			ns
t_{PD}	Port output valid from WRN high			400	ns
Interrupt Reset Timing (figure 6)					
t_{IR}	INTRN, or OP3-OP7 when used as interrupts, high from:				
	Read RHR (RxRDY/FFULL interrupt)			300	ns
	Write THR (TxRDY interrupt)			300	ns
	Reset command (delta break interrupt)			300	ns
	Stop C/T command (counter interrupt)			300	ns
	Read IPCR (input port change interrupt)			300	ns
	Write IMR (clear of interrupt mask bit)			300	ns
Clock Timing (figure 7)					
t_{CLK}	X1/CLK high or low time	100			ns
f_{CLK}	X1/CLK frequency	2.0	3.6864	4.0	MHz
t_{CTC}	CTCLK high or low time	100			ns
f_{CTC}	CTCLK frequency	0		4.0	MHz
t_{RX}	RXC high or low time	220			ns
f_{RX}	RXC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
t_{TX}	TXC high or low time	220			ns
f_{TX}	TXC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
Transmitter Timing (figure 8)					
t_{TXD}	TXD output delay from TXC low			350	ns
t_{TCS}	TXC output skew from TXD output data			150	ns
Receiver Timing (figure 9)					
t_{RXS}	RXD data setup time to RXC high	340			ns
t_{RXH}	RXD data hold time from RXC high	200			ns

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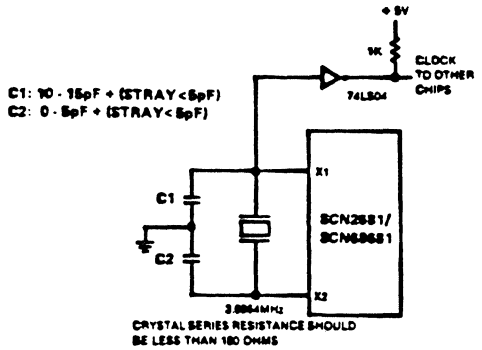
CRYSTAL FOR SCN2681/SCN68681

CHARACTERIZATION OF INITIAL PRODUCTION RUNS OF THESE CHIPS HAS INDICATED THAT THE CAPACITOR VALUES RECOMMENDED FOR THE CRYSTAL OSCILLATOR IN THE CURRENT DATA SHEET MAY NOT WORK FOR ALL DEVICES. THE NEXT REVISION OF THE DATA SHEET WILL SHOW THE FOLLOWING RECOMMENDED CIRCUIT:



NOTE THAT THE BOARD LAYOUT MAY AFFECT THE CAPACITOR VALUES. IT IS RECOMMENDED THAT THE CRYSTAL AND CAPACITOR(S) BE AS CLOSE AS POSSIBLE TO THE PINS OF THE DEVICE TO MINIMIZE STRAY CAPACITANCE.

THE RECOMMENDED CRYSTAL IS A STANDARD TYPE HC18 AVAILABLE FROM MANY MANUFACTURERS SUCH AS Q–MATIC, McCOY, M–TRON AND CRYSTEK.

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Reading of DUART Reserved Registers

In using the 2681/68681 the user should be careful to avoid reading any of the "reserved" registers - addresses '02', '0A' or '0C'. This will cause the device to enter a diagnostic mode in which the external device behavior appears to be erratic. Two common situations in which this can occur are the following:

Case I

The user software after any register write operation automatically performs a register read to verify the data written.

Case II

In a memory mapped I/O configuration, the user may attempt to perform a dump of a memory block. This can result in an inadvertent reading of the reserved registers.

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MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MC6809E

HMOS
(HIGH-DENSITY N-CHANNEL, SILICON-GATE)

8-BIT MICROPROCESSING UNIT

8-BIT MICROPROCESSING UNIT

The MC6809E is a revolutionary high performance 8-bit microprocessor which supports modern programming techniques such as position independence, reentrancy, and modular programming.

This third-generation addition to the M6800 Family has major architectural improvements which include additional registers, instructions, and addressing modes.

The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The MC6809E has the most complete set of addressing modes available on any 8-bit microprocessor today.

The MC6809E has hardware and software features which make it an ideal processor for higher level language execution or standard controller applications. External clock inputs are provided to allow synchronization with peripherals, systems, or other MPUs.

MC6800 COMPATIBLE

- Hardware — Interfaces with All M6800 Peripherals
- Software — Upward Source Code Compatible Instruction Set and Addressing Modes

ARCHITECTURAL FEATURES

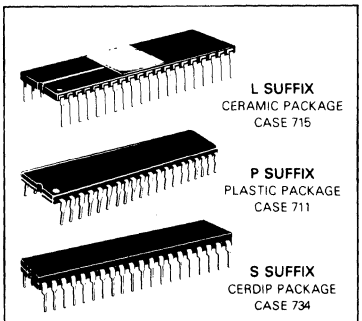
- Two 16-Bit Index Registers
- Two 16-Bit Indexable Stack Pointers
- Two 8-Bit Accumulators can be Concatenated to Form One 16-Bit Accumulator
- Direct Page Register Allows Direct Addressing Throughout Memory

HARDWARE FEATURES

- External Clock Inputs, E and Q, Allow Synchronization
- TSC Input Controls Internal Bus Buffers
- LIC Indicates Opcode Fetch
- AVMA Allows Efficient Use of Common Resources in a Multiprocessor System
- BUSY is a Status Line for Multiprocessing
- Fast Interrupt Request Input Stacks Only Condition Code Register and Program Counter
- Interrupt Acknowledge Output Allows Vectoring By Devices
- Sync Acknowledge Output Allows for Synchronization to External Event
- Single Bus-Cycle $\overline{\text{RESET}}$
- Single 5-Volt Supply Operation
- $\overline{\text{NMI}}$ Inhibited After $\overline{\text{RESET}}$ Until After First Load of Stack Pointer
- Early Address Valid Allows Use With Slower Memories
- Early Write Data for Dynamic Memories

SOFTWARE FEATURES

- 10 Addressing Modes
  - M6800 Upward Compatible Addressing Modes
  - Direct Addressing Anywhere in Memory Map
  - Long Relative Branches
  - Program Counter Relative
  - True Indirect Addressing
  - Expanded Indexed Addressing
    - 0-, 5-, 8-, or 16-Bit Constant Offsets
    - 8- or 16-Bit Accumulator Offsets
    - Auto-Increment/Decrement by 1 or 2
- Improved Stack Manipulation
- 1464 Instruction with Unique Addressing Modes
- 8 × 8 Unsigned Multiply
- 16-Bit Arithmetic
- Transfer/Exchange All Registers
- Push/Pull Any Registers or Any Set of Registers
- Load Effective Address

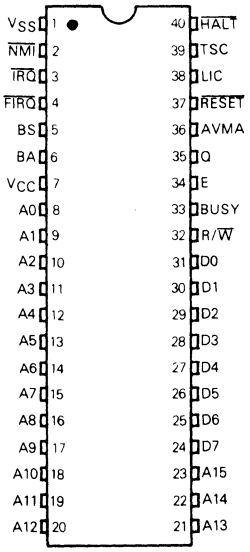


L SUFFIX
CERAMIC PACKAGE
CASE 715

P SUFFIX
PLASTIC PACKAGE
CASE 711

S SUFFIX
CERDIP PACKAGE
CASE 734

PIN ASSIGNMENT



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DS9846-R2

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range MC6809E, MC68A09E, MC68B09E MC6809EC, MC68A09EC, MC68B09EC	T_A	T_L to T_H 0 to +70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Ceramic Cerdip Plastic	θ_{JA}	 50 60 100	°C/W

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A ≡ Ambient Temperature, °C

θ_{JA} ≡ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{PORT}$

$P_{INT} \equiv I_{CC} \times V_{CC}$, Watts − Chip Internal Power

P_{PORT} ≡ Port Power Dissipation, Watts − User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage	Logic, Q,	V_{IH}	V_{SS} + 2.0	–	V_{CC}	V
	$\overline{RESET}$	V_{IHR}	V_{SS} + 4.0	–	V_{CC}	
	E	V_{IHC}	V_{CC} − 0.75	–	V_{CC} + 0.3	
Input Low Voltage	Logic, $\overline{RESET}$	V_{IL}	V_{SS} − 0.3	–	V_{SS} + 0.8	V
	E	V_{ILC}	V_{SS} − 0.3	–	V_{SS} + 0.4	V
	Q	V_{ILQ}	V_{SS} − 0.3	–	V_{SS} + 0.6	V
Input Leakage Current (V_{in} = 0 to 5.25 V, V_{CC} = max)	Logic, Q, $\overline{RESET}$	I_{in}	–	–	2.5	μA
	E		–	–	100	
dc Output High Voltage		V_{OH}				V
(I_{Load} = −205 μA, V_{CC} = min)	D0-D7		V_{SS} + 2.4	–	–	
(I_{Load} = −145 μA, V_{CC} = min)	A0-A15, R/$\overline{W}$		V_{SS} + 2.4	–	–	
(I_{Load} = −100 μA, V_{CC} = min)	BA, BS, LIC, AVMA, BUSY		V_{SS} + 2.4	–	–	
dc Output Low Voltage (I_{Load} = 2.0 mA, V_{CC} = min)		V_{OL}	–	–	V_{SS} + 0.5	V
Internal Power Dissipation (Measured at T_A = 0°C in Steady State Operation)		P_{INT}	–	–	1.0	W
Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	D0-D7, Logic Inputs, Q, $\overline{RESET}$	C_{in}	–	10	15	pF
	E		–	30	50	
	A0-A15, R/$\overline{W}$, BA, BS, LIC, AVMA, BUSY	C_{out}	–	10	15	pF
Frequency of Operation (E and Q Inputs)	MC6809E	f	0.1	–	1.0	MHz
	MC68A09E		0.1	–	1.5	
	MC68B09E		0.1	–	2.0	
Hi-Z (Off State) Input Current (V_{in} = 0.4 to 2.4 V, V_{CC} = max)	D0-D7	I_{TSI}	–	2.0	10	μA
	A0-A15, R/$\overline{W}$		–	–	100	

*Capacitances are periodically tested rather than 100% tested.

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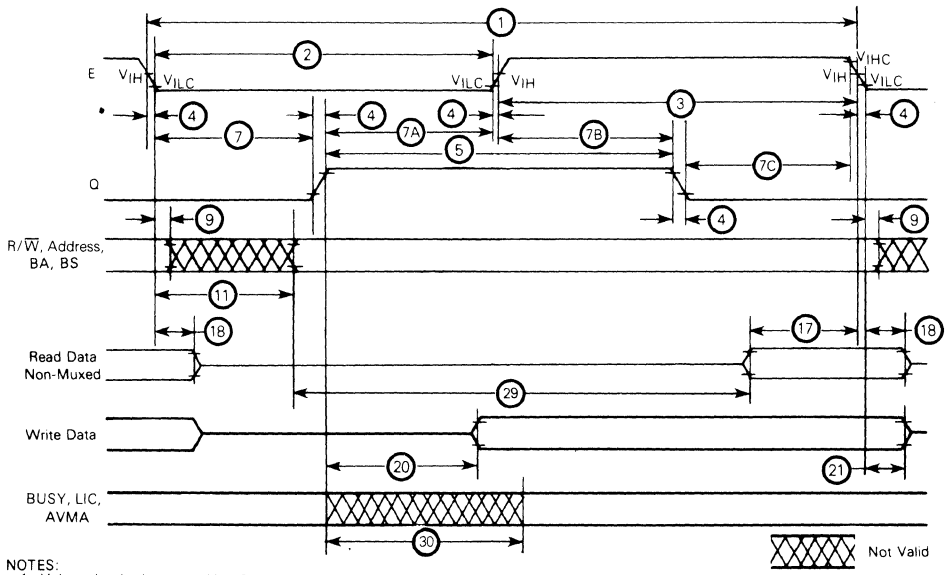
BUS TIMING CHARACTERISTICS (See Notes 1, 2, 3, and 4)

Ident. Number	Characteristics	Symbol	MC6809E		MC68A09E		MC68B09E		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1.0	10	0.667	10	0.5	10	µs
2	Pulse Width, E Low	PW_{EL}	450	9500	295	9500	210	9500	ns
3	Pulse Width, E High	PW_{EH}	450	9500	280	9500	220	9500	ns
4	Clock Rise and Fall Time	t_r, t_f	–	25	–	25	–	20	ns
5	Pulse Width, Q High	PW_{QH}	450	9500	280	9500	220	9500	ns
7	Delay Time, E to Q Rise	t_{EQ1}	200	–	130	–	100	–	ns
7A	Delay Time, Q High to E Rise	t_{EQ2}	200	–	130	–	100	–	ns
7B	Delay Time, E High to Q Fall	t_{EQ3}	200	–	130	–	100	–	ns
7C	Delay Time, Q High to E Fall	t_{EQ4}	200	–	130	–	100	–	ns
9	Address Hold Time	t_{AH}	20	–	20	–	20	–	ns
11	Address Delay Time from E Low (BA, BS, R/$\overline{W}$)	t_{AD}	–	200	–	140	–	110	ns
17	Read Data Setup Time	t_{DSR}	80	–	60	–	40	–	ns
18	Read Data Hold Time	t_{DHR}	10	–	10	–	10	–	ns
20	Data Delay Time from Q	t_{DDQ}	–	200	–	140	–	110	ns
21	Write Data Hold Time	t_{DHW}	30	–	30	–	30	–	ns
29	Usable Access Time	t_{ACC}	695	–	440	–	330	–	ns
30	Control Delay Time	t_{CD}	–	300	–	250	–	200	ns
	Interrupts, $\overline{HALT}$, $\overline{RESET}$, and TSC Setup Time (Figures 6, 7, 8, 9, 12, and 13)	t_{PCS}	200	–	140	–	110	–	ns
	TSC Drive to Valid Logic Level (Figure 13)	t_{TSV}	–	210	–	150	–	120	ns
	TSC Release MOS Buffers to High Impedance (Figure 13)	t_{TSR}	–	200	–	140	–	110	ns
	TSC Hi-Z Delay Time (Figure 13)	t_{TSD}	–	120	–	85	–	80	ns
	Processor Control Rise and Fall Time (Figure 7)	t_{PCr}, t_{PCf}	–	100	–	100	–	100	ns

FIGURE 1 – READ/WRITE DATA TO MEMORY OR PERIPHERALS TIMING DIAGRAM



NOTES:
1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.
3. Hold time (⑨) for BA and BS is not specified.
4. Usable access time is computed by: 1 – 4 – 11 max – 17.

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FIGURE 2 — EXPANDED BLOCK DIAGRAM

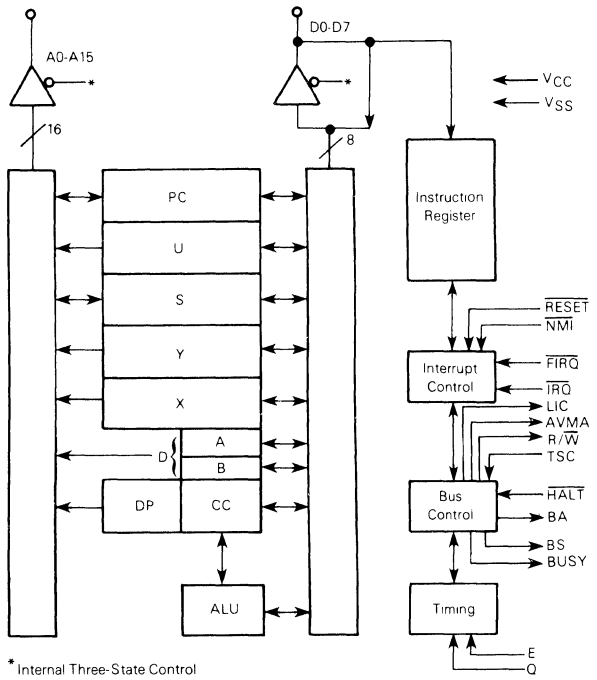
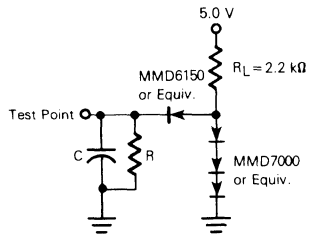


FIGURE 3 — BUS TIMING TEST LOAD



C = 30 pF for BA, BS, LIC, AVMA, BUSY
130 pF for D0-D7
90 pF for A0-A15, R/$\overline{W}$

R = 11.7 kΩ for D0-D7
16.5 kΩ for A0-A15, R/$\overline{W}$
24 kΩ for BA, BS, LIC, AVMA, BUSY

PROGRAMMING MODEL

As shown in Figure 4, the MC6809E adds three registers to the set available in the MC6800. The added registers include a direct page register, the user stack pointer, and a second index register.

ACCUMULATORS (A, B, D)

The A and B registers are general purpose accumulators which are used for arithmetic calculations and manipulation of data.

Certain instructions concatenate the A and B registers to form a single 16-bit accumulator. This is referred to as the D register, and is formed with the A register as the most significant byte.

DIRECT PAGE REGISTER (DP)

The direct page register of the MC6809E serves to enhance the direct addressing mode. The content of this register appears at the higher address outputs (A8-A15) during direct addressing instruction execution. This allows the direct mode to be used at any place in memory, under program control. To ensure M6800 compatibility, all bits of this register are cleared during processor reset.

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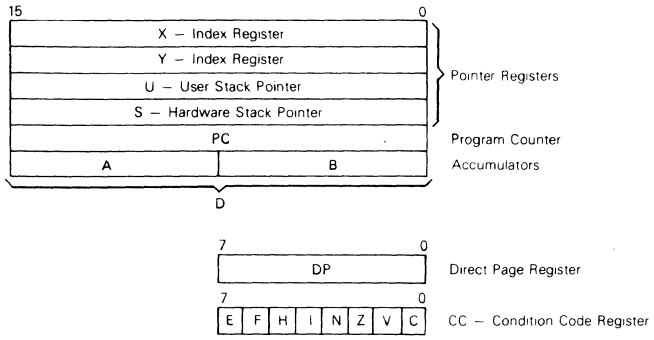
FIGURE 4 – PROGRAMMING MODEL OF THE MICROPROCESSING UNIT



INDEX REGISTERS (X, Y)

The index registers are used in indexed mode of addressing. The 16-bit address in this register takes part in the calculation of effective addresses. This address may be used to point to data directly or may be modified by an optional constant or register offset. During some indexed modes, the contents of the index register are incremented and decremented to point to the next item of tabular type data. All four pointer registers (X, Y, U, S) may be used as index registers.

STACK POINTER (U, S)

The hardware stack pointer (S) is used automatically by the processor during subroutine calls and interrupts. The user stack pointer (U) is controlled exclusively by the programmer. This allows arguments to be passed to and from subroutines with ease. The U register is frequently used as a stack marker. Both stack pointers have the same indexed mode addressing capabilities as the X and Y registers, but also support **Push** and **Pull** instructions. This allows the MC6809E to be used efficiently as a stack processor, greatly enhancing its ability to support higher level languages and modular programming.

NOTE

The stack pointers of the MC6809E point to the top of the stack in contrast to the MC6800 stack pointer, which pointed to the next free location on stack.

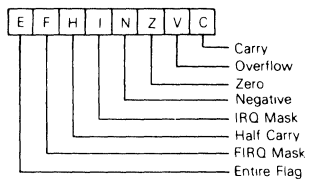
PROGRAM COUNTER

The program counter is used by the processor to point to the address of the next instruction to be executed by the processor. Relative addressing is provided allowing the program counter to be used like an index register in some situations.

CONDITION CODE REGISTER

The condition code register defines the state of the processor at any given time. See Figure 4.

FIGURE 5 – CONDITION CODE REGISTER FORMAT



CONDITION CODE REGISTER DESCRIPTION

BIT 0 (C)

Bit 0 is the carry flag and is usually the carry from the binary ALU. C is also used to represent a "borrow" from subtract like instructions (CMP, NEG, SUB, SBC) and is the complement of the carry from the binary ALU.

BIT 1 (V)

Bit 1 is the overflow flag and is set to a one by an operation which causes a signed twos complement arithmetic overflow. This overflow is detected in an operation in which the carry from the MSB in the ALU does not match the carry from the MSB-1.

BIT 2 (Z)

Bit 2 is the zero flag and is set to a one if the result of the previous operation was identically zero.

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BIT 3 (N)

Bit 3 is the negative flag, which contains exactly the value of the MSB of the result of the preceding operation. Thus, a negative twos complement result will leave N set to a one.

BIT 4 (I)

Bit 4 is the $\overline{IRQ}$ mask bit. The processor will not recognize interrupts from the $\overline{IRQ}$ line if this bit is set to a one. $\overline{NMI}$, $\overline{FIRQ}$, $\overline{IRQ}$, $\overline{RESET}$, and SWI all set I to a one. SWI2 and SWI3 do not affect I.

BIT 5 (H)

Bit 5 is the half-carry bit, and is used to indicate a carry from bit 3 in the ALU as a result of an 8-bit addition only (ADC or ADD). This bit is used by the DAA instruction to perform a BCD decimal add adjust operation. The state of this flag is undefined in all subtract-like instructions.

BIT 6 (F)

Bit 6 is the $\overline{FIRQ}$ mask bit. The processor will not recognize interrupts from the $\overline{FIRQ}$ line if this bit is a one. $\overline{NMI}$, $\overline{FIRQ}$, SWI, and $\overline{RESET}$ all set F to a one. $\overline{IRQ}$, SWI2, and SWI3 do not affect F.

BIT 7 (E)

Bit 7 is the entire flag, and when set to a one indicates that the complete machine state (all the registers) was stacked, as opposed to the subset state (PC and CC). The E bit of the stacked CC is used on a return from interrupt (RTI) to determine the extent of the unstacking. Therefore, the current E left in the condition code register represents past action.

PIN DESCRIPTIONS

POWER (V_{SS}, V_{CC})

Two pins are used to supply power to the part: V_{SS} is ground or 0 volts, while V_{CC} is +5.0 V ±5%.

ADDRESS BUS (A0-A15)

Sixteen pins are used to output address information from the MPU onto the address bus. When the processor does not require the bus for a data transfer, it will output address $FFFF_{16}$, R/$\overline{W}$ = 1, and BS = 0; this is a "dummy access" or $\overline{VMA}$ cycle. All address bus drivers are made high-impedance when output bus available (BA) is high or when TSC is asserted. Each pin will drive one Schottky TTL load or four LSTTL loads and 90 pF.

DATA BUS (D0-D7)

These eight pins provide communication with the system bidirectional data bus. Each pin will drive one Schottky TTL load or four LSTTL loads and 130 pF.

READ/WRITE (R/$\overline{W}$)

This signal indicates the direction of data transfer on the data bus. A low indicates that the MPU is writing data onto the data bus. R/$\overline{W}$ is made high impedance when BA is high or when TSC is asserted.

$\overline{RESET}$

A low level on this Schmitt-trigger input for greater than one bus cycle will reset the MPU, as shown in Figure 6. The reset vectors are fetched from locations $FFFE_{16}$ and $FFFF_{16}$ (Table 1) when interrupt acknowledge is true, ($\overline{BA}$•BS = 1). During initial power on, the reset line should be held low until the clock input signals are fully operational.

Because the MC6809E $\overline{RESET}$ pin has a Schmitt-trigger input with a threshold voltage higher than that of standard peripherals, a simple R/C network may be used to reset the entire system. This higher threshold voltage ensures that all peripherals are out of the reset state before the processor.

$\overline{HALT}$

A low level on this input pin will cause the MPU to stop running at the end of the present instruction and remain halted indefinitely without loss of data. When halted, the BA output is driven high indicating the buses are high impedance. BS is also high which indicates the processor is in the halt state. While halted, the MPU will not respond to external real-time requests ($\overline{FIRQ}$, $\overline{IRQ}$) although $\overline{NMI}$ or $\overline{RESET}$ will be latched for later response. During the halt state, Q and E should continue to run normally. A halted state (BA•BS = 1) can be achieved by pulling $\overline{HALT}$ low while $\overline{RESET}$ is still low. See Figure 7.

BUS AVAILABLE, BUS STATUS (BA, BS)

The bus available output is an indication of an internal control signal which makes the MOS buses of the MPU high impedance. When BA goes low, a dead cycle will elapse before the MPU acquires the bus. BA will not be asserted when TSC is active, thus allowing dead cycle consistency.

The bus status output signal, when decoded with BA, represents the MPU state (valid with leading edge of Q).

MPU State		MPU State Definition
BA	BS	
0	0	Normal (Running)
0	1	Interrupt or Reset Acknowledge
1	0	Sync Acknowledge
1	1	Halt Acknowledge

Interrupt Acknowledge is indicated during both cycles of a hardware vector fetch ($\overline{RESET}$, $\overline{NMI}$, $\overline{FIRQ}$, $\overline{IRQ}$, SWI, SWI2, SWI3). This signal, plus decoding of the lower four address lines, can provide the user with an indication of which interrupt level is being serviced and allow vectoring by device. See Table 1.

TABLE 1 – MEMORY MAP FOR INTERRUPT VECTORS

Memory Map For Vector Locations		Interrupt Vector Description
MS	LS	
FFFE	FFFF	$\overline{RESET}$
FFFC	FFFD	$\overline{NMI}$
FFFA	FFFB	SWI
FFF8	FFF9	$\overline{IRQ}$
FFF6	FFF7	$\overline{FIRQ}$
FFF4	FFF5	SWI2
FFF2	FFF3	SWI3
FFF0	FFF1	Reserved

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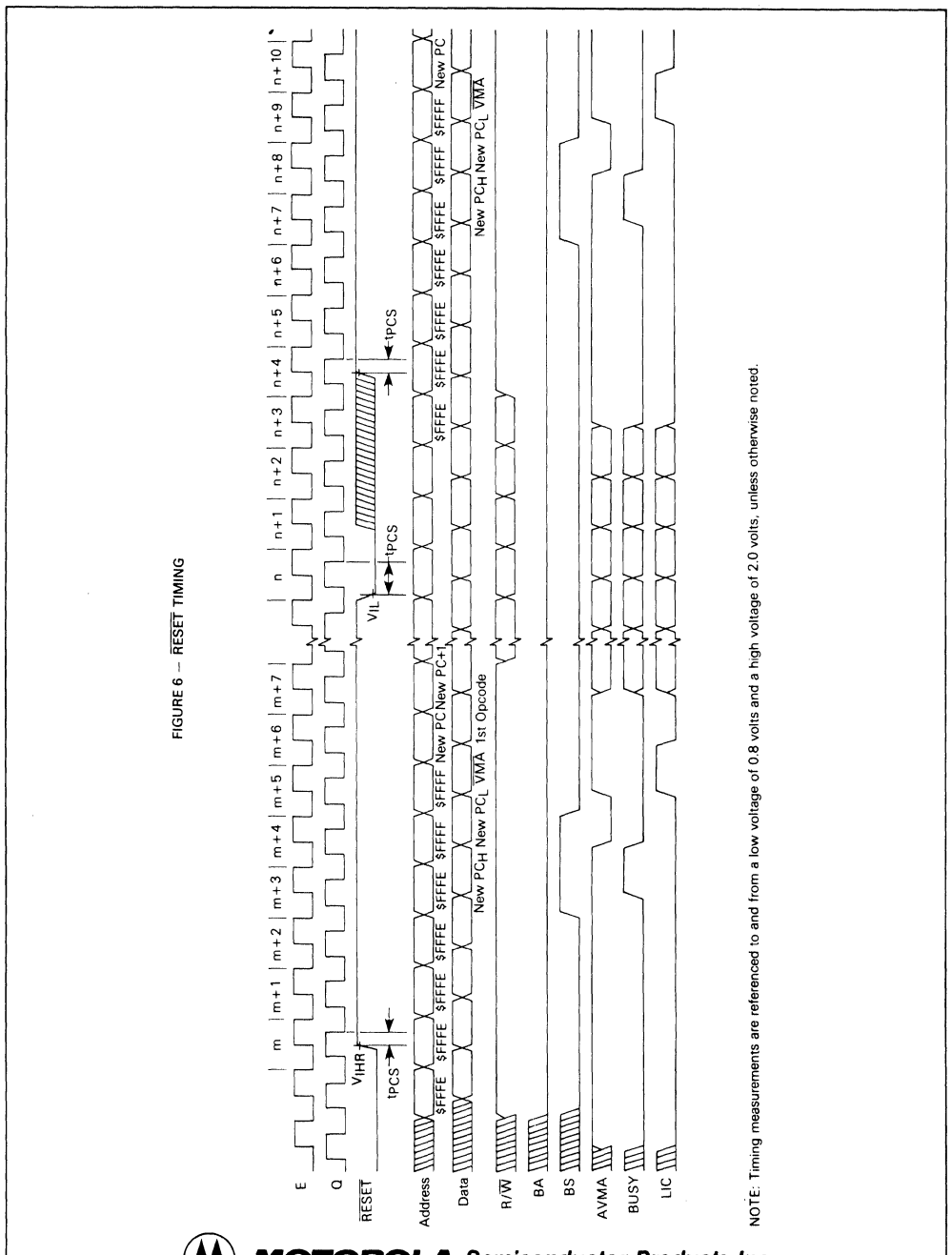

FIGURE 6 – $\overline{\text{RESET}}$ TIMING

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

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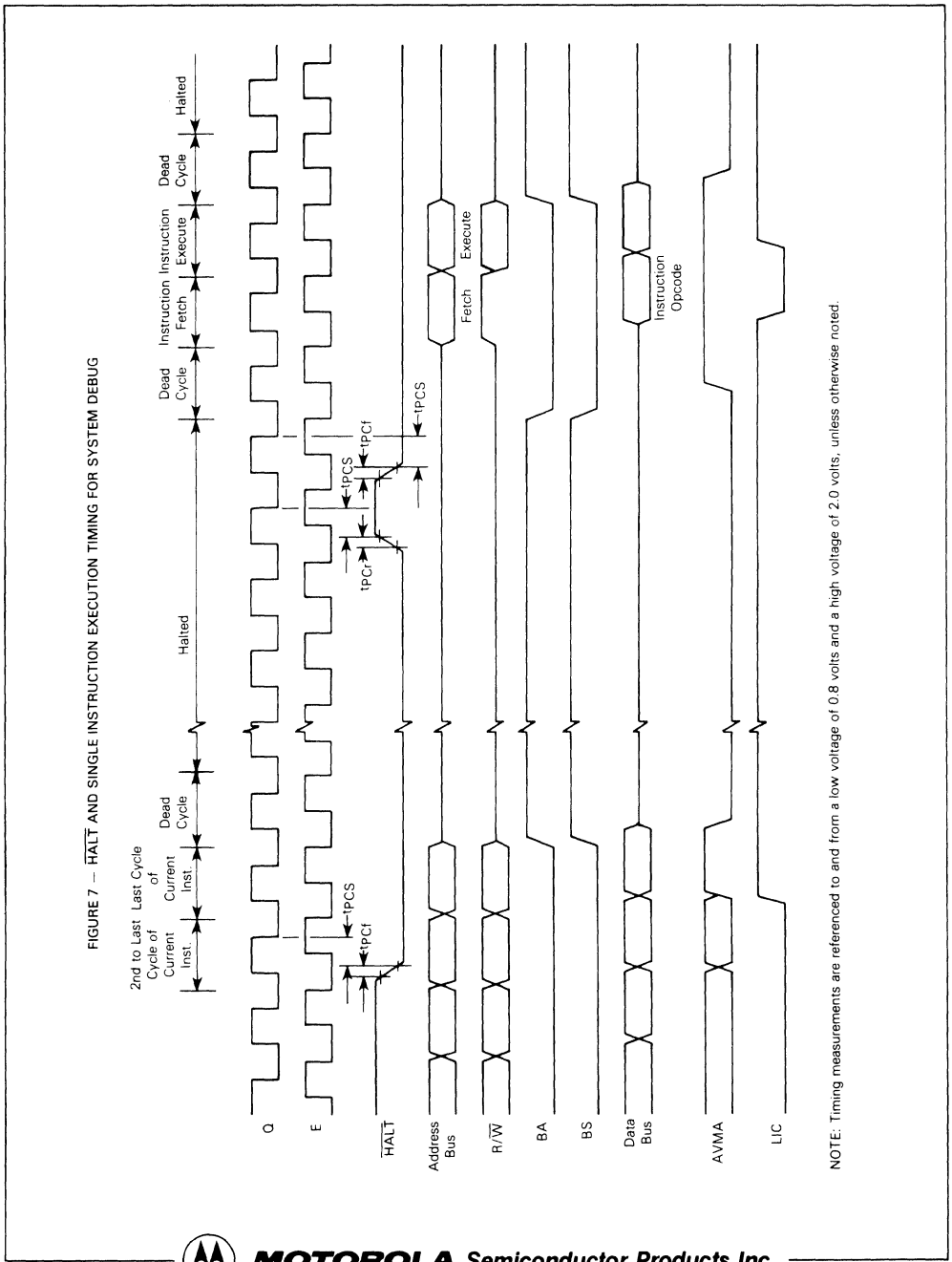

FIGURE 7 – $\overline{\text{HALT}}$ AND SINGLE INSTRUCTION EXECUTION TIMING FOR SYSTEM DEBUG

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

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Sync Acknowledge is indicated while the MPU is waiting for external synchronization on an interrupt line.

Halt Acknowledge is indicated when the MC6809E is in a halt condition.

NON MASKABLE INTERRUPT ($\overline{NMI}$)*

A negative transition on this input requests that a non-maskable interrupt sequence be generated. A non-maskable interrupt cannot be inhibited by the program and also has a higher priority than $\overline{FIRQ}$, $\overline{IRQ}$, or software interrupts. During recognition of an $\overline{NMI}$, the entire machine state is saved on the hardware stack. After reset, an $\overline{NMI}$ will not be recognized until the first program load of the hardware stack pointer (S). The pulse width of $\overline{NMI}$ low must be at least one E cycle. If the $\overline{NMI}$ input does not meet the minimum set up with respect to Q, the interrupt will not be recognized until the next cycle. See Figure 8.

FAST-INTERRUPT REQUEST ($\overline{FIRQ}$)*

A low level on this input pin will initiate a fast interrupt sequence, provided its mask bit (F) in the CC is clear. This sequence has priority over the standard interrupt request ($\overline{IRQ}$) and is fast in the sense that it stacks only the contents of the condition code register and the program counter. The interrupt service routine should clear the source of the interrupt before doing an RTI. See Figure 9.

INTERRUPT REQUEST ($\overline{IRQ}$)*

A low level input on this pin will initiate an interrupt request sequence provided the mask bit (I) in the CC is clear. Since $\overline{IRQ}$ stacks the entire machine state, it provides a slower response to interrupts than $\overline{FIRQ}$. $\overline{IRQ}$ also has a lower priority than $\overline{FIRQ}$. Again, the interrupt service routine should clear the source of the interrupt before doing an RTI. See Figure 8.

CLOCK INPUTS E, Q

E and Q are the clock signals required by the MC6809E. Q must lead E; that is, a transition on Q must be followed by a similar transition on E after a minimum delay. Addresses will be valid from the MPU, t_{AD} after the falling edge of E, and data will be latched from the bus by the falling edge of E. While the Q input is fully TTL compatible, the E input directly drives internal MOS circuitry and, thus, requires a high level above normal TTL levels. This approach minimizes clock skew inherent with an internal buffer. Refer to **BUS TIMING CHARACTERISTICS** for E and Q and to Figure 10 which shows a simple clock generator for the MC6809E.

BUSY

BUSY will be high for the read and modify cycles of a read-modify-write instruction and during the access of the first byte of a double-byte operation (e.g., LDX, STD, ADDD). BUSY is also high during the first byte of any indirect or other vector fetch (e.g., jump extended, SWI indirect, etc.).

In a multiprocessor system, BUSY indicates the need to defer the rearbitration of the next bus cycle to insure the integrity of the above operations. This difference provides the indivisible memory access required for a "test-and-set" primitive, using any one of several read-modify-write instructions.

BUSY does not become active during PSH or PUL operations. A typical read-modify-write instruction (ASL) is shown in Figure 11. Timing information is given in Figure 12. BUSY is valid t_{CD} after the rising edge of Q.

AVMA

AVMA is the advanced VMA signal and indicates that the MPU will use the bus in the following bus cycle. The predictive nature of the AVMA signal allows efficient shared-bus multiprocessor systems. AVMA is low when the MPU is in either a $\overline{HALT}$ or SYNC state. AVMA is valid t_{CD} after the rising edge of Q.

LIC

LIC (last instruction cycle) is high during the last cycle of every instruction, and its transition from high to low will indicate that the first byte of an opcode will be latched at the end of the present bus cycle. LIC will be high when the MPU is halted at the end of an instruction (i.e., not in CWAI or $\overline{RESET}$), in sync state, or while stacking during interrupts. LIC is valid t_{CD} after the rising edge of Q.

TSC

TSC (three-state control) will cause MOS address, data, and R/$\overline{W}$ buffers to assume a high-impedance state. The control signals (BA, BS, BUSY, AVMA, and LIC) will not go to the high-impedance state. TSC is intended to allow a single bus to be shared with other bus masters (processors or DMA controllers).

While E is low, TSC controls the address buffers and R/$\overline{W}$ directly. The data bus buffers during a write operation are in a high-impedance state until Q rises at which time, if TSC is true, they will remain in a high-impedance state. If TSC is held beyond the rising edge of E, then it will be internally latched, keeping the bus drivers in a high-impedance state for the remainder of the bus cycle. See Figure 13.

MPU OPERATION

During normal operation, the MPU fetches an instruction from memory and then executes the requested function. This sequence begins after $\overline{RESET}$ and is repeated indefinitely unless altered by a special instruction or hardware occurrence. Software instructions that alter normal MPU operation are: SWI, SWI2, SWI3, CWAI, RTI, and SYNC. An interrupt or $\overline{HALT}$ input can also alter the normal execution of instructions. Figure 14 is the flowchart for the MC6809E.

* $\overline{NMI}$, $\overline{FIRQ}$, and $\overline{IRQ}$ requests are sampled on the falling edge of Q. One cycle is required for synchronization before these interrupts are recognized. The pending interrupt(s) will not be serviced until completion of the current instruction unless a SYNC or CWAI condition is present. If $\overline{IRQ}$ and $\overline{FIRQ}$ do not remain low until completion of the current instruction, they may not be recognized. However, $\overline{NMI}$ is latched and need only remain low for one cycle. No interrupts are recognized or latched between the falling edge of $\overline{RESET}$ and the rising edge of BS indicating $\overline{RESET}$ acknowledge. See $\overline{RESET}$ sequence in the MPU flowchart in Figure 14.

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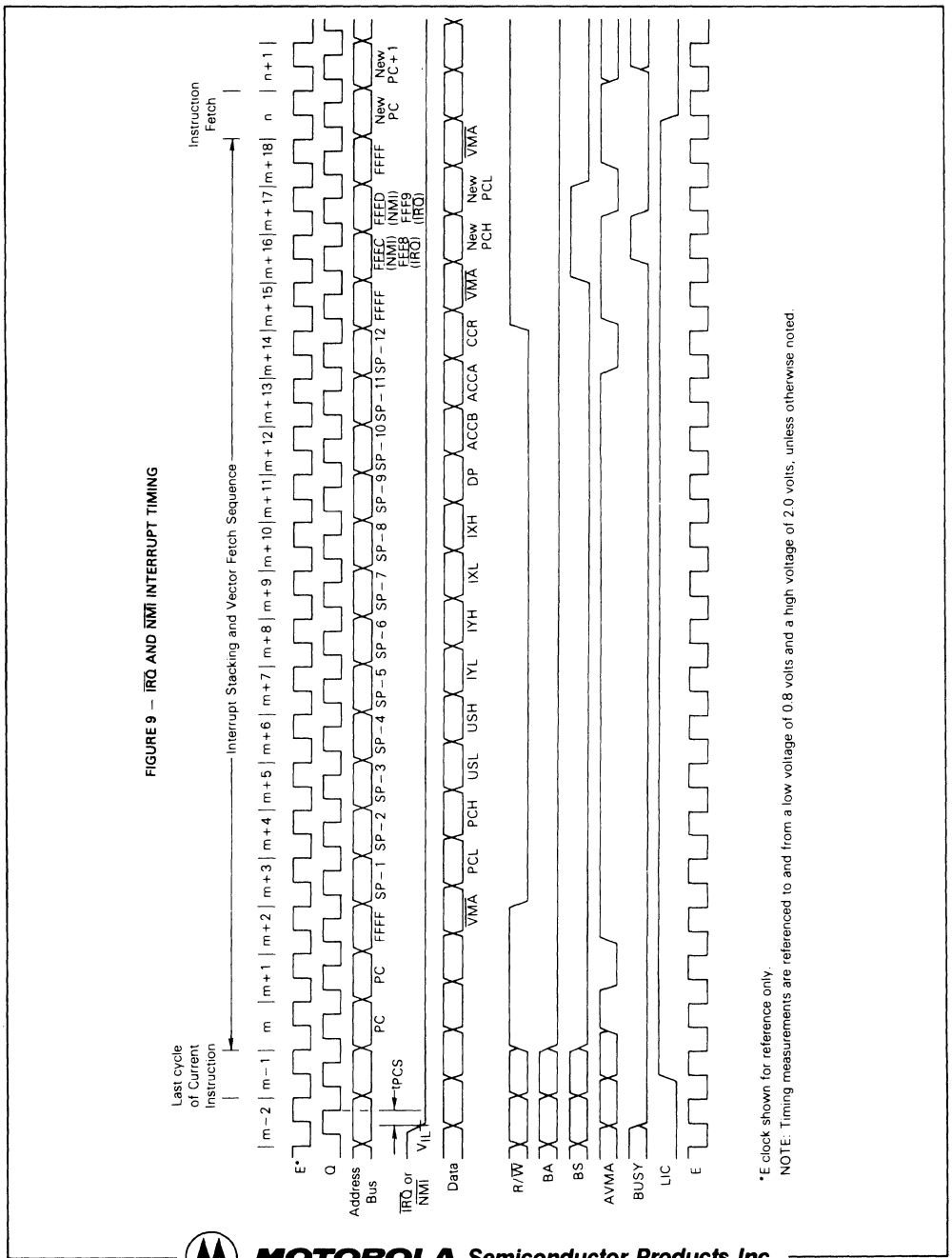

FIGURE 9 – $\overline{IRQ}$ AND $\overline{NMI}$ INTERRUPT TIMING

*E clock shown for reference only.

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

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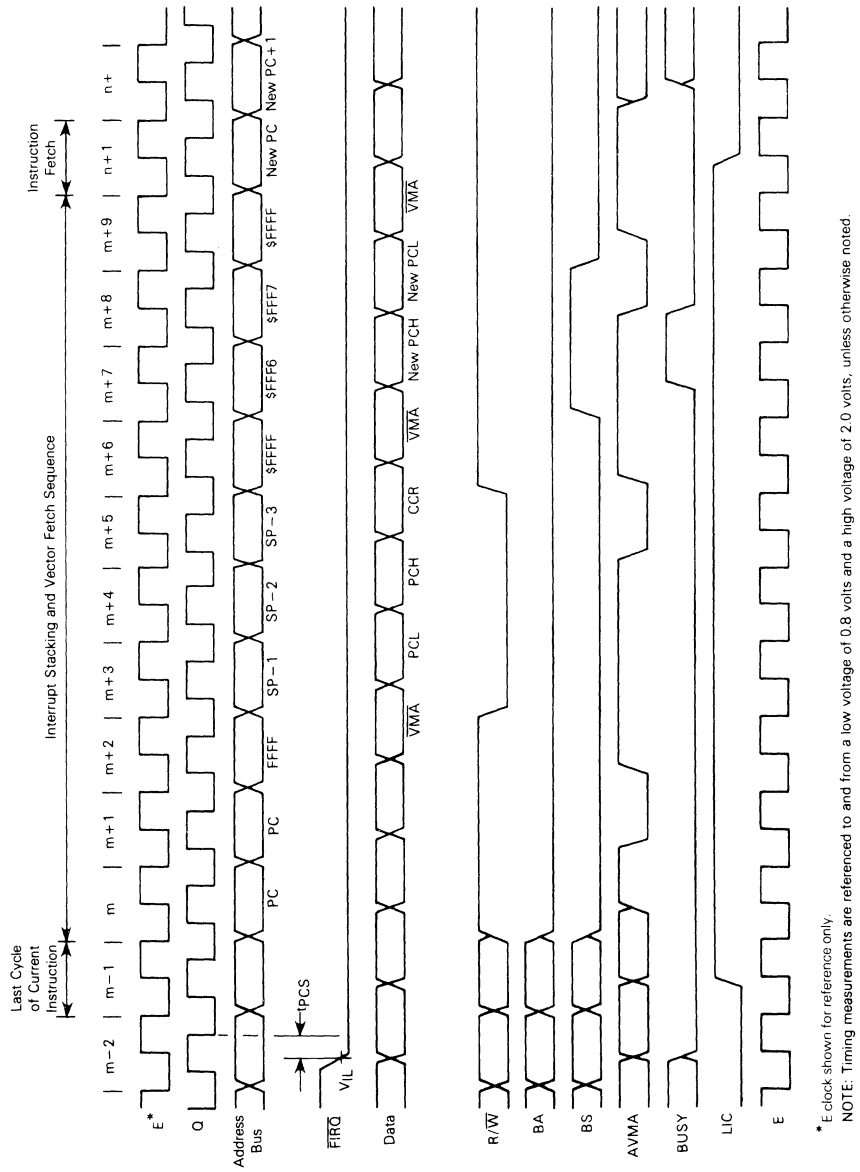
FIGURE 9 – $\overline{FIRQ}$ INTERRUPT TIMING



* E clock shown for reference only.

NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

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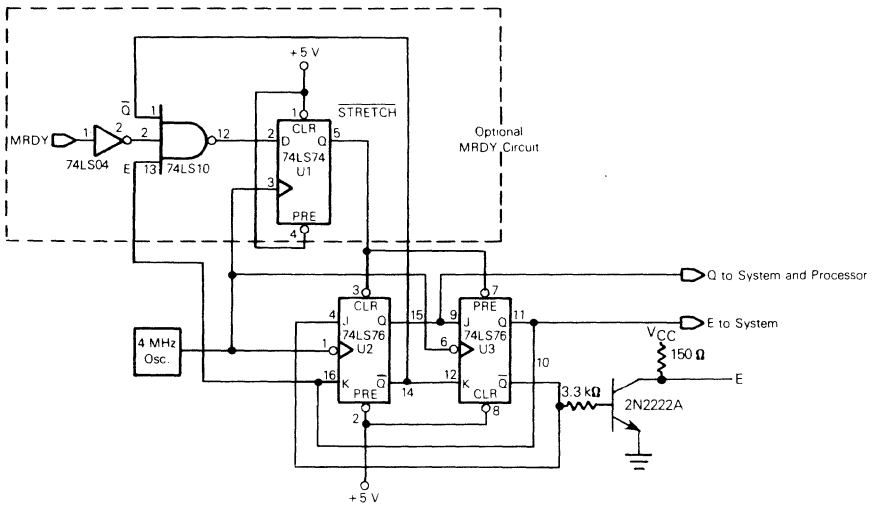
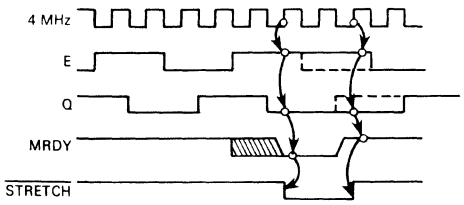
FIGURE 10 – CLOCK GENERATOR





NOTE: If optional circuit is not included the CLR and PRE inputs of U2 and U3 must be tied high.

FIGURE 11 – READ-MODIFY-WRITE INSTRUCTION EXAMPLE (ASL EXTENDED INDIRECT)

Memory Location	Memory Contents	Contents Description
PC → $0200	$68	ASL Indexed Opcode
$0201	$9F	Extended Indirect Postbyte
$0202	$63	Indirect Address Hi-Byte
$0203	$00	Indirect Address Lo-Byte
$0204		Next Main Instruction
$6300	$E3	Effective Address Hi-Byte
$6301	$D6	Effective Address Lo-Byte
$E3D6	$5C	Target Data

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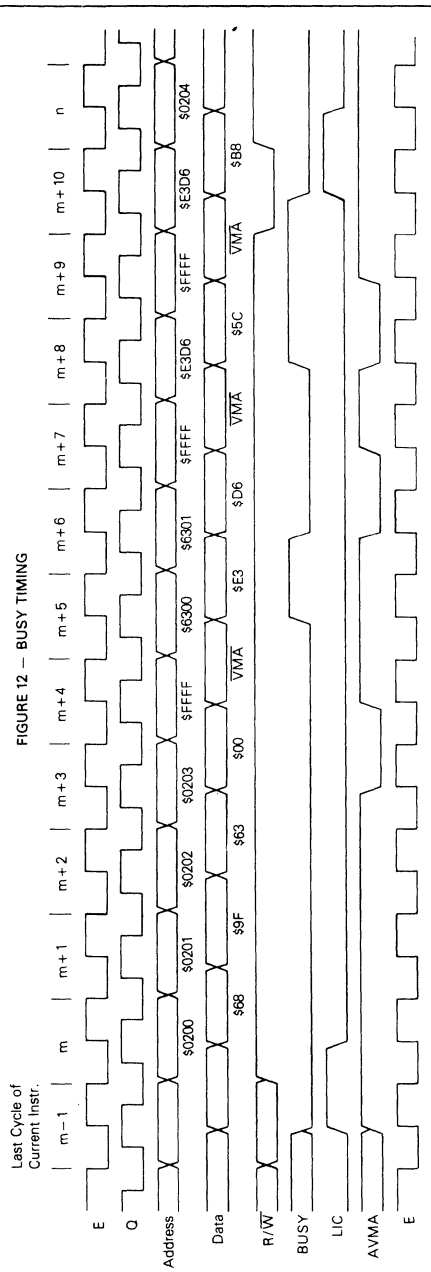

FIGURE 12 – BUSY TIMING

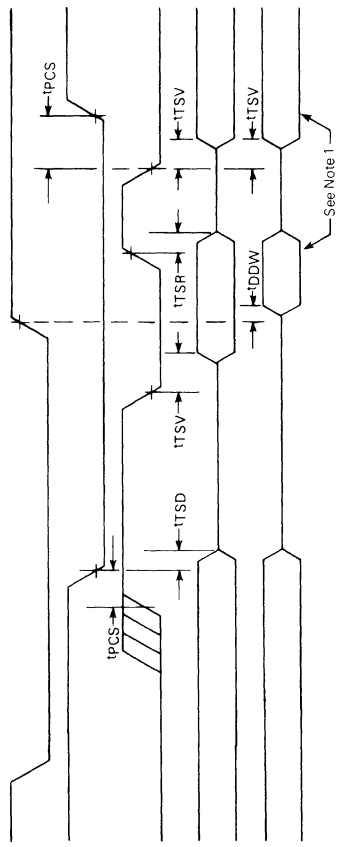

FIGURE 13 – TSC TIMING

NOTES:
1. Data will be asserted by the MPU only during the interval while R/$\overline{W}$ is low and (E or Q) is high. A composite bus cycle is shown to give most cases of timing.
2. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

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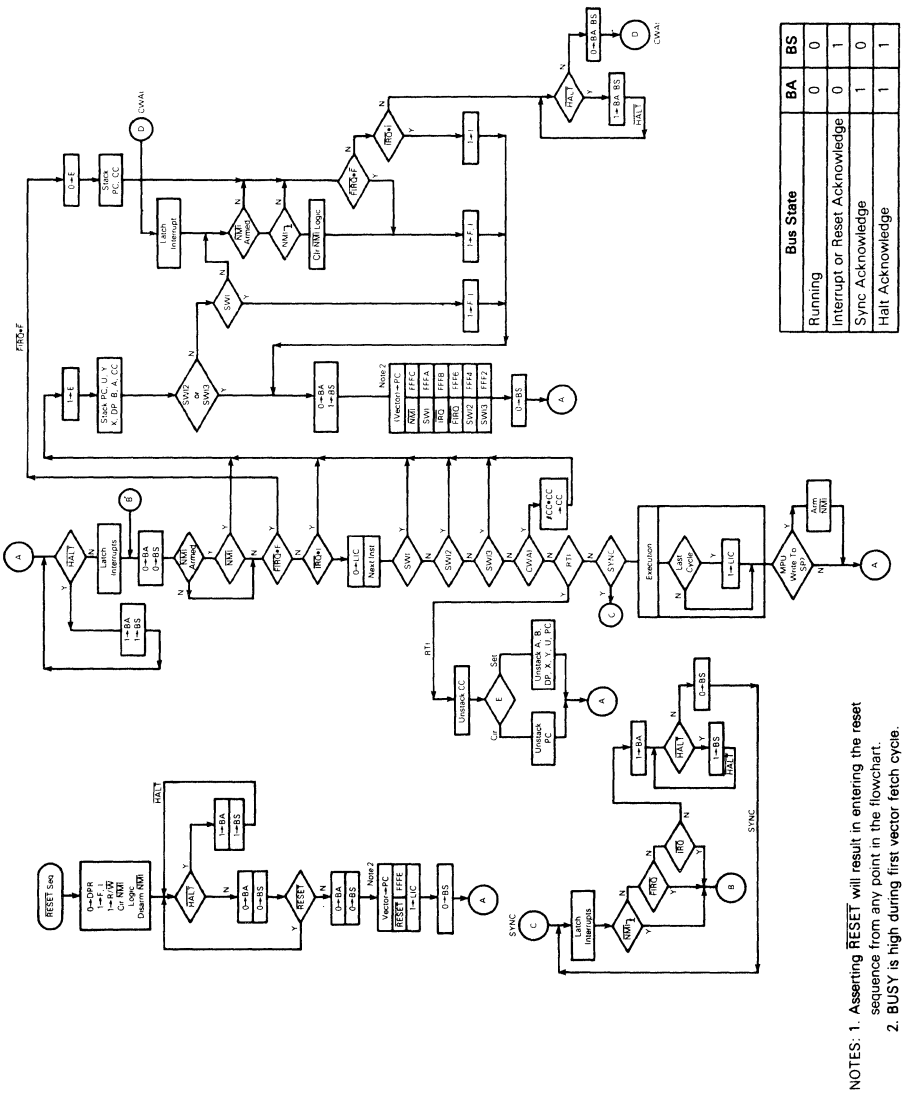

FIGURE 14 – FLOWCHART FOR MC6809E INSTRUCTIONS

NOTES: 1. Asserting $\overline{\text{RESET}}$ will result in entering the reset sequence from any point in the flowchart.
2. BUSY is high during first vector fetch cycle.

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ADDRESSING MODES

The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The MC6809E has the most complete set of addressing modes available on any microcomputer today. For example, the MC6809E has 59 basic instructions; however, it recognizes 1464 different variations of instructions and addressing modes. The addressing modes support modern programming techniques. The following addressing modes are available on the MC6809E:

- Inherent (Includes Accumulator)
- Immediate
- Extended
  - Extended Indirect
- Direct
- Register
- Indexed
  - Zero-Offset
  - Constant Offset
  - Accumulator Offset
  - Auto Increment/Decrement
  - Indexed Indirect
- Relative
  - Short/Long Relative Branching
  - Program Counter Relative Addressing

INHERENT (INCLUDES ACCUMULATOR)

In this addressing mode, the opcode of the instruction contains all the address information necessary. Examples of inherent addressing are: ABX, DAA, SWI, ASRA, and CLRB.

IMMEDIATE ADDRESSING

In immediate addressing, the effective address of the data is the location immediately following the opcode (i.e., the data to be used in the instruction immediately following the opcode of the instruction). The MC6809E uses both 8- and 16-bit immediate values depending on the size of argument specified by the opcode. Examples of instructions with immediate addressing are:

```
LDA   #$20
LDX   #$F000
LDY   #CAT
```

NOTE

signifies immediate addressing; $ signifies hexadecimal value to the MC6809 assembler.

EXTENDED ADDRESSING

In extended addressing, the contents of the two bytes immediately following the opcode fully specify the 16-bit effective address used by the instruction. Note that the address generated by an extended instruction defines an absolute address and is not position independent. Examples of extended addressing include:

```
LDA   CAT
STX   MOUSE
LDD   $2000
```

EXTENDED INDIRECT

As a special case of indexed addressing (discussed below), one level of indirection may be added to extended addressing. In extended indirect, the two bytes following the postbyte of an indexed instruction contain the address of the data.

```
LDA   [CAT]
LDX   [$FFFE]
STU   [DOG]
```

DIRECT ADDRESSING

Direct addressing is similar to extended addressing except that only one byte of address follows the opcode. This byte specifies the lower eight bits of the address to be used. The upper eight bits of the address are supplied by the direct page register. Since only one byte of address is required in direct addressing, this mode requires less memory and executes faster than extended addressing. Of course, only 256 locations (one page) can be accessed without redefining the contents of the DP register. Since the DP register is set to $00 on reset, direct addressing on the MC6809E is upward compatible with direct addressing on the M6800. Indirection is not allowed in direct addressing. Some examples of direct addressing are:

```
LDA   where DP = $00
LDB   where DP = $10
LDD   <CAT
```

NOTE

< is an assembler directive which forces direct addressing.

REGISTER ADDRESSING

Some opcodes are followed by a byte that defines a register or set of registers to be used by the instruction. This is called a postbyte. Some examples of register addressing are:

TFR	X, Y	Transfers X into Y
EXG	A, B	Exchanges A with B
PSHS	A, B, X, Y	Push Y, X, B and A onto S stack
PULU	X, Y, D	Pull D, X, and Y from U stack

INDEXED ADDRESSING

In all indexed addressing, one of the pointer registers (X, Y, U, S, and sometimes PC) is used in a calculation of the effective address of the operand to be used by the instruction. Five basic types of indexing are available and are discussed below. The postbyte of an indexed instruction specifies the basic type and variation of the addressing mode, as well as the pointer register to be used. Figure 15 lists the legal formats for the postbyte. Table 2 gives the assembler form and the number of cycles and bytes added to the basic values for indexed addressing for each variation.

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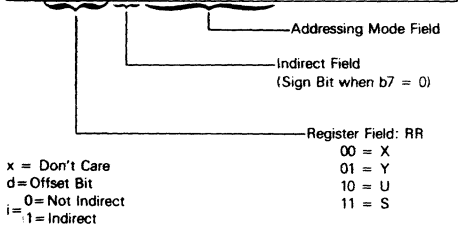
FIGURE 15 – INDEXED ADDRESSING POSTBYTE REGISTER BIT ASSIGNMENTS

Post-Byte Register Bit								Indexed Addressing Mode
7	6	5	4	3	2	1	0	
0	R	R	d	d	d	d	d	EA = ,R + 5 Bit Offset
1	R	R	0	0	0	0	0	,R+
1	R	R	i	0	0	0	1	,R+ +
1	R	R	0	0	0	1	0	,–R
1	R	R	i	0	0	1	1	,– –R
1	R	R	i	0	1	0	0	EA = ,R +0 Offset
1	R	R	i	0	1	0	1	EA = ,R + ACCB Offset
1	R	R	i	0	1	1	0	EA = ,R + ACCA Offset
1	R	R	i	1	0	0	0	EA = ,R +8 Bit Offset
1	R	R	i	1	0	0	1	EA = ,R +16 Bit Offset
1	R	R	i	1	0	1	1	EA = ,R +D Offset
1	x	x	i	1	1	0	0	EA = ,PC +8 Bit Offset
1	x	x	i	1	1	0	1	EA = ,PC +16 Bit Offset
1	R	R	i	1	1	1	1	EA = [,Address]



x = Don't Care
d = Offset Bit
i = 0 = Not Indirect, 1 = Indirect

ZERO-OFFSET INDEXED – In this mode, the selected pointer register contains the effective address of the data to be used by the instruction. This is the fastest indexing mode.

Examples are:

LDD 0, X
LDA ,S

CONSTANT OFFSET INDEXED – In this mode, twos complement offset and the contents of one of the pointer registers are added to form the effective address of the operand. The pointer register's initial content is unchanged by the addition.

Three sizes of offset are available:

5-bit (– 16 to + 15)
8-bit (– 128 to + 127)
16-bit (– 32768 to + 32767)

The twos complement 5-bit offset is included in the post-byte and, therefore, is most efficient in use of bytes and cycles. The twos complement 8-bit offset is contained in a single byte following the postbyte. The twos complement 16-bit offset is in the two bytes following the postbyte. In most cases the programmer need not be concerned with the size of this offset since the assembler will select the optimal size automatically.

Examples of constant-offset indexing are:

LDA 23,X
LDX –2,S
LDY 300,X
LDU CAT,Y

TABLE 2 – INDEXED ADDRESSING MODE

Type	Forms	Non Indirect				Indirect			
		Assembler Form	Postbyte Opcode	+ ~	+ #	Assembler Form	Postbyte Opcode	+ ~	+ #
Constant Offset From R (2s Complement Offsets)	No Offset	,R	1RR00100	0	0	[,R]	1RR10100	3	0
	5-Bit Offset	n, R	0RRnnnnn	1	0	defaults to 8-bit			
	8-Bit Offset	n, R	1RR01000	1	1	[n, R]	1RR11000	4	1
	16-Bit Offset	n, R	1RR01001	4	2	[n, R]	1RR11001	7	2
Accumulator Offset From R (2s Complement Offsets)	A Register Offset	A, R	1RR00110	1	0	[A, R]	1RR10110	4	0
	B Register Offset	B, R	1RR00101	1	0	[B, R]	1RR10101	4	0
	D Register Offset	D, R	1RR01011	4	0	[D, R]	1RR11011	7	0
Auto Increment/Decrement R	Increment By 1	,R+	1RR00000	2	0	not allowed			
	Increment By 2	,R+ +	1RR00001	3	0	[,R+ +]	1RR10001	6	0
	Decrement By 1	,–R	1RR00010	2	0	not allowed			
	Decrement By 2	,– –R	1RR00011	3	0	[,– –R]	1RR10011	6	0
Constant Offset From PC (2s Complement Offsets)	8-Bit Offset	n, PCR	1xx01100	1	1	[n, PCR]	1xx11100	4	1
	16-Bit Offset	n, PCR	1xx01101	5	2	[n, PCR]	1xx11101	8	2
Extended Indirect	16-Bit Address	–	–	–	–	[n]	10011111	5	2

R = X, Y, U or S
x = Don't Care

RR:
00 = X
01 = Y
10 = U
11 = S

$^{+}_{\sim}$ and $^{+}_{\#}$ indicate the number of additional cycles and bytes respectively for the particular indexing variation.

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ACCUMULATOR-OFFSET INDEXED – This mode is similar to constant offset indexed except that the twos complement value in one of the accumulators (A, B, or D) and the contents of one of the pointer registers are added to form the effective address of the operand. The contents of both the accumulator and the pointer register are unchanged by the addition. The postbyte specifies which accumulator to use as an offset and no additional bytes are required. The advantage of an accumulator offset is that the value of the offset can be calculated by a program at run-time.

Some examples are:

```
LDA   B, Y
LDX   D, Y
LEAX  B, X
```

AUTO INCREMENT/DECREMENT INDEXED – In the auto increment addressing mode, the pointer register contains the address of the operand. Then, after the pointer register is used, it is incremented by one or two. This addressing mode is useful in stepping through tables, moving data, or creating software stacks. In auto decrement, the pointer register is decremented prior to use as the address of the data. The use of auto decrement is similar to that of auto increment, but the tables, etc., are scanned from the high to low addresses. The size of the increment/decrement can be either one or two to allow for tables of either 8- or 16-bit data to be accessed and is selectable by the programmer. The pre-decrement, post-increment nature of these modes allows them to be used to create additional software stacks that behave identically to the U and S stacks.

Some examples of the auto increment/decrement addressing modes are:

```
LDA   ,X+
STD   ,Y++
LDB   ,-Y
LDX   ,--S
```

Care should be taken in performing operations on 16-bit pointer registers (X, Y, U, S) where the same register is used to calculate the effective address.

Consider the following instruction:

STX 0,X++ (X initialized to 0)

The desired result is to store a zero in locations $0000 and $0001, then increment X to point to $0002. In reality, the following occurs:

0→temp	calculate the EA; temp is a holding register
X+2→X	perform auto increment
X→(temp)	do store operation

INDEXED INDIRECT

All of the indexing modes, with the exception of auto increment/decrement by one or a ±5-bit offset, may have an additional level of indirection specified. In indirect addressing, the effective address is contained at the location specified by the contents of the index register plus any offset. In the example below, the A accumulator is loaded indirectly using an effective address calculated from the index register and an offset.

```
Before Execution
  A = XX (don't care)
  X = $F000

$0100   LDA [$10,X]     EA is now $F010

$F010   $F1             $F150 is now the
$F011   $50             new EA

$F150   $AA

After Execution
  A = $AA (actual data loaded)
  X = $F000
```

All modes of indexed indirect are included except those which are meaningless (e.g., auto increment/decrement by 1 indirect). Some examples of indexed indirect are:

```
LDA   [,X]
LDD   [10,S]
LDA   [B,Y]
LDD   [,X++]
```

RELATIVE ADDRESSING

The byte(s) following the branch opcode is (are) treated as a signed offset which may be added to the program counter. If the branch condition is true, then the calculated address (PC + signed offset) is loaded into the program counter. Program execution continues at the new location as indicated by the PC; short (one byte offset) and long (two bytes offset) relative addressing modes are available. All of memory can be reached in long relative addressing as an effective address interpreted modulo 2^{16}. Some examples of relative addressing are:

```
          BEQ     CAT     (short)
          BGT     DOG     (short)
CAT       LBEQ    RAT     (long)
DOG       LBGT    RABBIT  (long)
          •
          •
          •
RAT       NOP
RABBIT    NOP
```

PROGRAM COUNTER RELATIVE

The PC can be used as the pointer register with 8- or 16-bit signed offsets. As in relative addressing, the offset is added to the current PC to create the effective address. The effective address is then used as the address of the operand or data. Program counter relative addressing is used for writing position independent programs. Tables related to a particular routine will maintain the same relationship after the routine is moved, if referenced relative to the program counter. Examples are:

```
LDA   CAT, PCR
LEAX  TABLE, PCR
```

Since program counter relative is a type of indexing, an additional level of indirection is available.

```
LDA   [CAT, PCR]
LDU   [DOG, PCR]
```


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INSTRUCTION SET

The instruction set of the MC6809E is similar to that of the MC6800 and is upward compatible at the source code level. The number of opcodes has been reduced from 72 to 59, but because of the expanded architecture and additional addressing modes, the number of available opcodes (with different addressing modes) has risen from 197 to 1464.

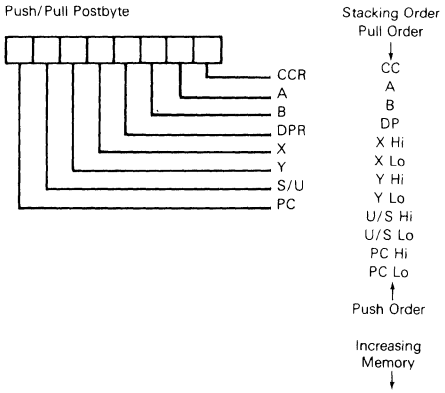
Some of the new instructions are described in detail below.

PSHU/PSHS

The push instructions have the capability of pushing onto either the hardware stack (S) or user stack (U) any single register or set of registers with a single instruction.

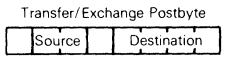
PULU/PULS

The pull instructions have the same capability of the push instruction, in reverse order. The byte immediately following the push or pull opcode determines which register or registers are to be pushed or pulled. The actual push/pull sequence is fixed; each bit defines a unique register to push or pull, as shown below.



TFR/EXG

Within the MC6809E, any register may be transferred to or exchanged with another of like size; i.e., 8-bit to 8-bit or 16-bit to 16-bit. Bits 4-7 of postbyte define the source register, while bits 0-3 represent the destination register. These are denoted as follows:



Register Field

0000 = D (A:B)	1000 = A
0001 = X	1001 = B
0010 = Y	1010 = CCR
0011 = U	1011 = DPR
0100 = S	
0101 = PC	

NOTE

All other combinations are undefined and INVALID.

LEAX/LEAY/LEAU/LEAS

The LEA (load effective address) works by calculating the effective address used in an indexed instruction and stores that address value, rather than the data at that address, in a pointer register. This makes all the features of the internal addressing hardware available to the programmer. Some of the implications of this instruction are illustrated in Table 3.

The LEA instruction also allows the user to access data and tables in a position independent manner. For example:

```
        LEAX    MSG1, PCR
        LBSR    PDATA (Print message routine)
        •
        •
MSG1    FCC     'MESSAGE'
```

This sample program prints: 'MESSAGE'. By writing MSG1, PCR, the assembler computes the distance between the present address and MSG1. This result is placed as a constant into the LEAX instruction which will be indexed from the PC value at the time of execution. No matter where the code is located when it is executed, the computed offset from the PC will put the absolute address of MSG1 into the X pointer register. This code is totally position independent.

The LEA instructions are very powerful and use an internal holding register (temp). Care must be exercised when using the LEA instructions with the auto increment and auto decrement addressing modes due to the sequence of internal operations. The LEA internal sequence is outlined as follows:

LEAa ,b+ (any of the 16-bit pointer registers X, Y, U, or S may be substituted for a and b.)

1. b → temp (calculate the EA)
2. b + 1 → b (modify b, postincrement)
3. temp → a (load a)

LEAa , – b

1. b – 1 → temp (calculate EA with predecrement)
2. b – 1 → b (modify b, predecrement)
3. temp → a (load a)

TABLE 3 – LEA EXAMPLES

Instruction	Operation	Comment
LEAX 10, X	X + 10 → X	Adds 5-Bit Constant 10 to X
LEAX 500, X	X + 500 → X	Adds 16-Bit Constant 500 to X
LEAY A, Y	Y + A → Y	Adds 8-Bit A Accumulator to Y
LEAY D, Y	Y + D → Y	Adds 16-Bit D Accumulator to Y
LEAU – 10, U	U – 10 → U	Substracts 10 from U
LEAS – 10, S	S – 10 → S	Used to Reserve Area on Stack
LEAS 10, S	S + 10 → S	Used to 'Clean Up' Stack
LEAX 5, S	S + 5 → X	Transfers As Well As Adds

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Auto increment-by-two and auto decrement-by-two instructions work similarly. Note that LEAX ,X+ does not change X; however LEAX, −X does decrement X.LEAX 1,X should be used to increment X by one.

MUL

Multiplies the unsigned binary numbers in the A and B accumulator and places the unsigned result into the 16-bit D accumulator. This unsigned multiply also allows multiple-precision multiplications.

LONG AND SHORT RELATIVE BRANCHES

The MC6809E has the capability of program counter relative branching throughout the entire memory map. In this mode, if the branch is to be taken, the 8- or 16-bit signed offset is added to the value of the program counter to be used as the effective address. This allows the program to branch anywhere in the 64K memory map. Position independent code can be easily generated through the use of relative branching. Both short (8 bit) and long (16 bit) branches are available.

SYNC

After encountering a sync instruction, the MPU enters a sync state, stops processing instructions, and waits for an interrupt. If the pending interrupt is non-maskable ($\overline{NMI}$) or maskable ($\overline{FIRQ}$, $\overline{IRQ}$) with its mask bit (F or I) clear, the processor will clear the sync state and perform the normal interrupt stacking and service routine. Since $\overline{FIRQ}$ and $\overline{IRQ}$ are not edge-triggered, a low level with a minimum duration of three bus cycles is required to assure that the interrupt will be taken. If the pending interrupt is maskable ($\overline{FIRQ}$, $\overline{IRQ}$) with its mask bit (F or I) set, the processor will clear the sync state and continue processing by executing the next in-line instruction. Figure 16 depicts sync timing.

SOFTWARE INTERRUPTS

A software interrupt is an instruction which will cause an interrupt and its associated vector fetch. These software interrupts are useful in operating system calls, software debugging, trace operations, memory mapping, and software development systems. Three levels of SWI are available on this MC6809E and are prioritized in the following order: SWI, SWI2, SWI3.

16-BIT OPERATION

The MC6809E has the capability of processing 16-bit data. These instructions include loads, stores, compares, adds, subtracts, transfers, exchanges, pushes, and pulls.

CYCLE-BY-CYCLE OPERATION

The address bus cycle-by-cycle performance chart (Figure 16) illustrates the memory-access sequence corresponding to each possible instruction and addressing mode in the MC6809E. Each instruction begins with an opcode fetch. While that opcode is being internally decoded, the next program byte is always fetched. (Most instructions will use the next byte, so this technique considerably speeds throughput.) Next, the operation of each opcode will follow the flowchart. $\overline{VMA}$ is an indication of $FFFF_{16}$ on the address bus, R/$\overline{W}$ = 1 and BS = 0. The following examples illustrate the use of the chart.

Example 1: LBSR (Branch Taken)
Before Execution SP = F000

```
                    •
                    •
                    •
$8000               LBSR    CAT
                    •
                    •
                    •
$A000   CAT         •
```

CYCLE-BY-CYCLE FLOW

Cycle #	Address	Data	R/$\overline{W}$	Description
1	8000	17	1	Opcode Fetch
2	8001	20	1	Offset High Byte
3	8002	00	1	Offset Low Byte
4	FFFF	*	1	$\overline{VMA}$ Cycle
5	FFFF	*	1	$\overline{VMA}$ Cycle
6	A000	*	1	Computed Branch Address
7	FFFF	*	1	$\overline{VMA}$ Cycle
8	EFFF	80	0	Stack High Order Byte of Return Address
9	EFFE	03	0	Stack Low Order Byte of Return Address

Example 2: DEC (Extended)

```
$8000   DEC     $A000
$A000   FCB     $80
```

CYCLE-BY-CYCLE FLOW

Cycle #	Address	Data	R/$\overline{W}$	Description
1	8000	7A	1	Opcode Fetch
2	8001	A0	1	Operand Address, High Byte
3	8002	00	1	Operand Address, Low Byte
4	FFFF	*	1	$\overline{VMA}$ Cycle
5	A000	80	1	Read the Data
6	FFFF	*	1	$\overline{VMA}$ Cycle
7	FFFF	7F	0	Store the Decremented Data

*The data bus has the data at that particular address.

INSTRUCTION SET TABLES

The instructions of the MC6809E have been broken down into five different categories. They are as follows:

8-bit operation (Table 4)
16-bit operation (Table 5)
Index register/stack pointer instructions (Table 6)
Relative branches (long or short) (Table 7)
Miscellaneous instructions (Table 8)

Hexadecimal values for the instructions are given in Table 9.

PROGRAMMING AID

Figure 18 contains a compilation of data that will assist you in programming the MC6809E.

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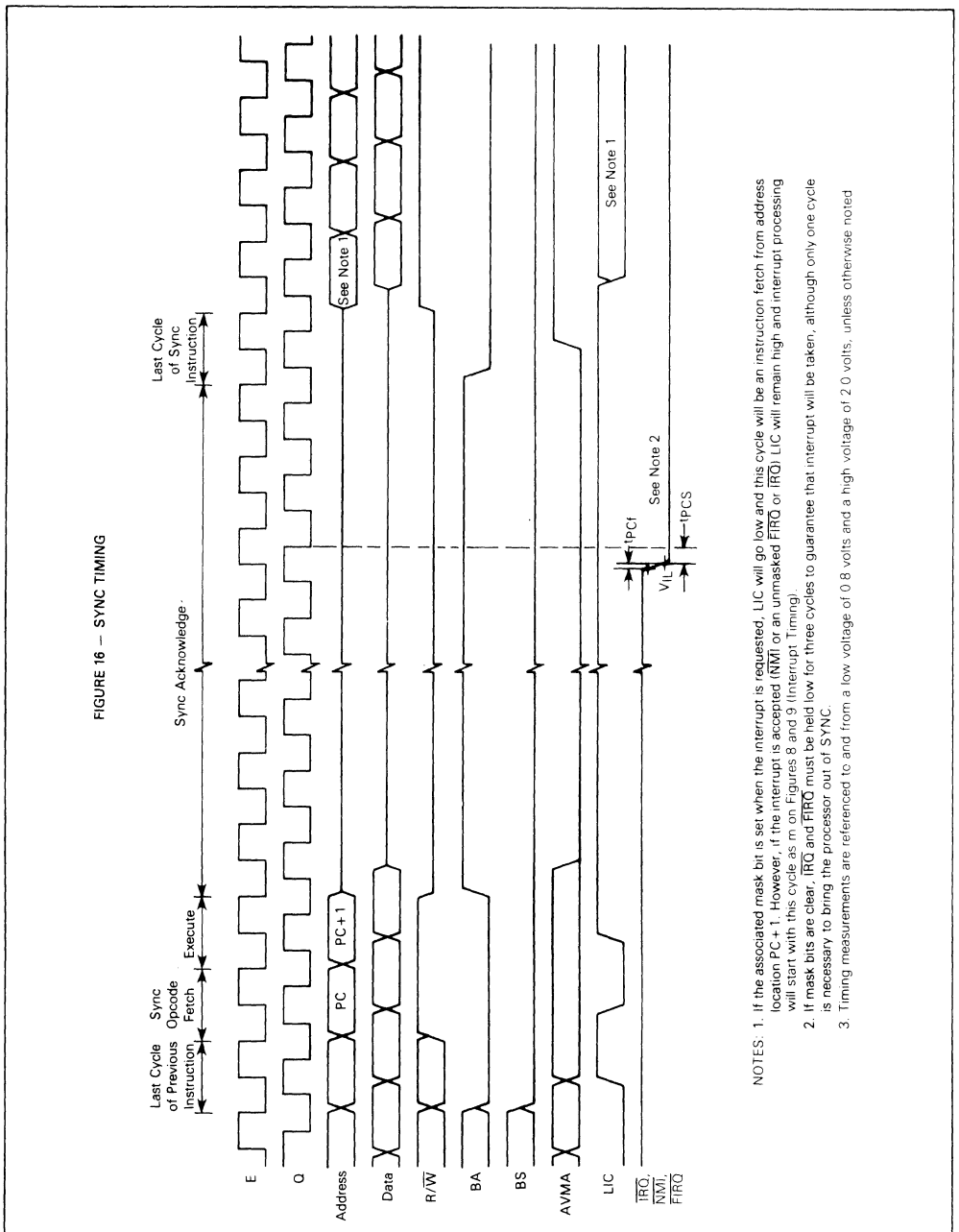

FIGURE 16 – SYNC TIMING

NOTES: 1. If the associated mask bit is set when the interrupt is requested, LIC will go low and this cycle will be an instruction fetch from address location PC + 1. However, if the interrupt is accepted (NMI or an unmasked FIRQ or IRQ) LIC will remain high and interrupt processing will start with this cycle as in on Figures 8 and 9 (Interrupt Timing).
2. If mask bits are clear, IRQ and FIRQ must be held low for three cycles to guarantee that interrupt will be taken, although only one cycle is necessary to bring the processor out of SYNC.
3. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted

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FIGURE 17 — CYCLE-BY-CYCLE PERFORMANCE (Sheet 1 of 5)

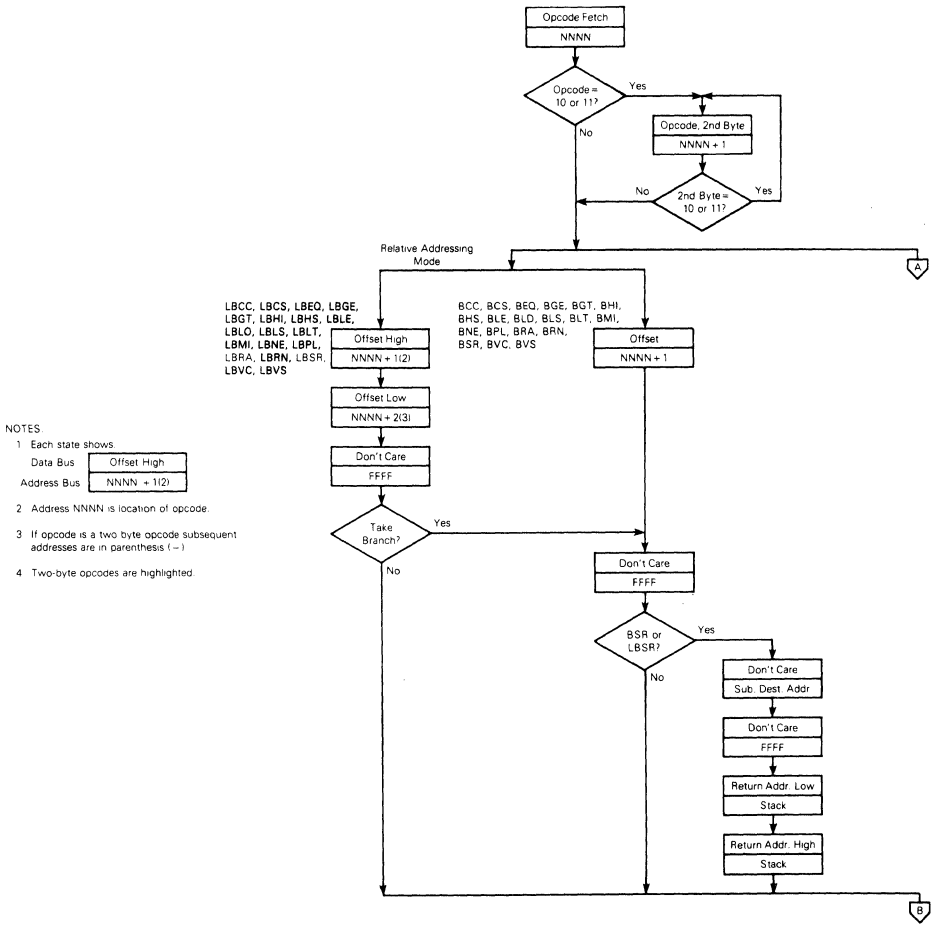

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FIGURE 17 — CYCLE-BY-CYCLE PERFORMANCE (Sheet 2 of 5)

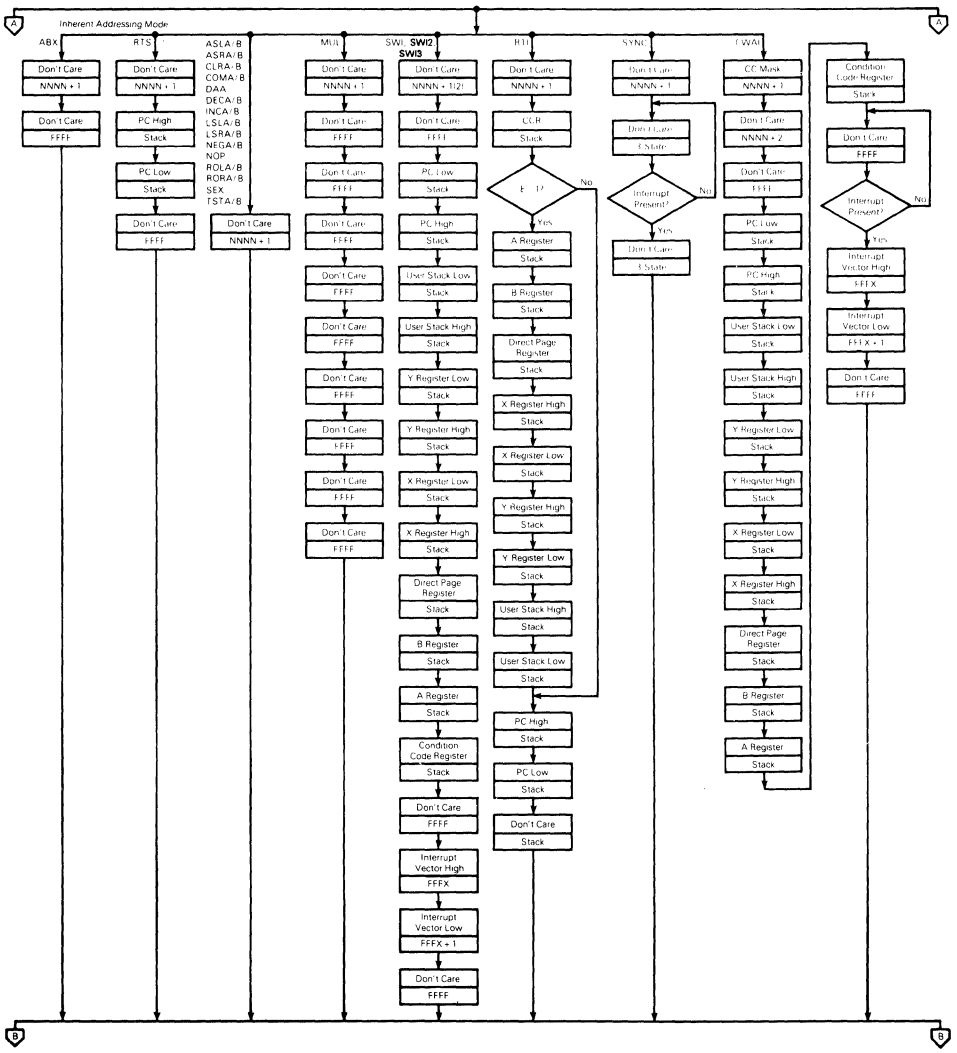

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FIGURE 17 — CYCLE-BY-CYLE PERFORMANCE (Sheet 3 of 5)

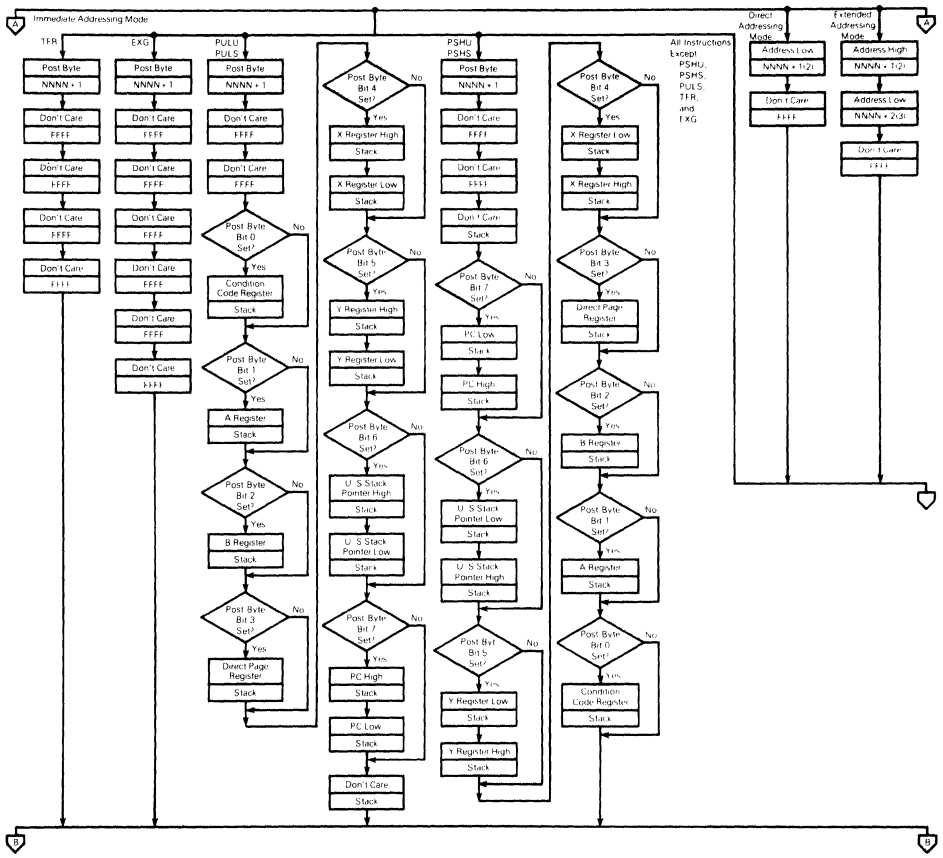

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FIGURE 17 — CYCLE-BY-CYCLE PERFORMANCE (Sheet 4 of 5)

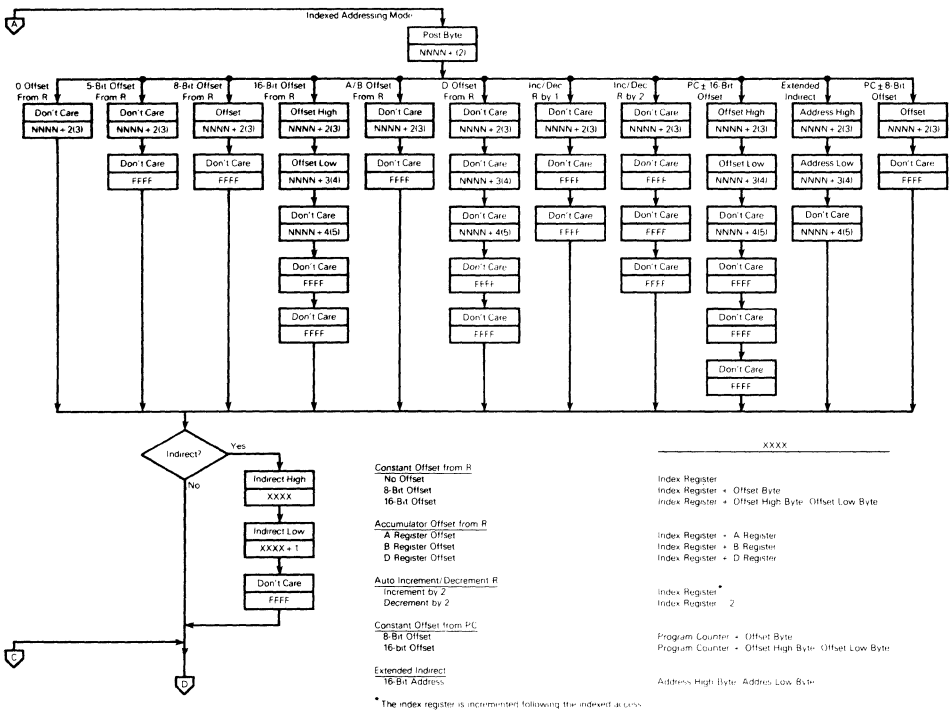

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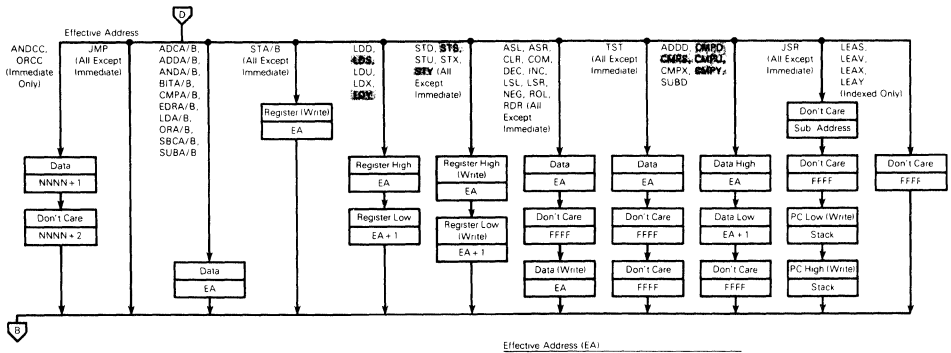
FIGURE 17 — CYCLE-BY-CYCLE PERFORMANCE (Sheet 5 of 5)



	Effective Address (EA)
Constant Offset from R	
No Offset	Index Register
5-Bit Offset	Index Register
8-Bit Offset	Index Register + Post Byte
16-Bit Offset	Index Register + Post Byte High Post Byte Low
Accumulator Offset from R	
A Register Offset	Index Register + A Register
B Register Offset	Index Register + B Register
D Register Offset	Index Register + D Register
Auto Increment/ Decrement R	
Increment by 1	Index Register*
Increment by 2	Index Register*
Decrement by 1	Index Register − 1
Decrement by 2	Index Register − 2
Constant Offset from PC	
8-Bit Offset	Program Counter + Offset Byte
16-Bit Offset	Program Counter + Offset High Byte Offset Low Byte
Direct	Direct Page Register Address Low
Extended	Address High Address Low
Immediate	NNNN + 1

*The index register is incremented following the indexed access

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TABLE 4 — 8-BIT ACCUMULATOR AND MEMORY INSTRUCTIONS

Mnemonic(s)	Operation
ADCA, ADCB	Add memory to accumulator with carry
ADDA, ADDB	Add memory to accumulator
ANDA, ANDB	And memory with accumulator
ASL, ASLA, ASLB	Arithmetic shift of accumulator or memory left
ASR, ASRA, ASRB	Arithmetic shift of accumulator or memory right
BITA, BITB	Bit test memory with accumulator
CLR, CLRA, CLRB	Clear accumulator or memory location
CMPA, CMPB	Compare memory from accumulator
COM, COMA, COMB	Complement accumulator or memory location
DAA	Decimal adjust A accumulator
DEC, DECA, DECB	Decrement accumulator or memory location
EORA, EORB	Exclusive or memory with accumulator
EXG R1, R2	Exchange R1 with R2 (R1, R2 = A, B, CC, DP)
INC, INCA, INCB	Increment accumulator or memory location
LDA, LDB	Load accumulator from memory
LSL, LSLA, LSLB	Logical shift left accumulator or memory location
LSR, LSRA, LSRB	Logical shift right accumulator or memory location
MUL	Unsigned multiply (A × B → D)
NEG, NEGA, NEGB	Negate accumulator or memory
ORA, ORB	Or memory with accumulator
ROL, ROLA, ROLB	Rotate accumulator or memory left
ROR, RORA, RORB	Rotate accumulator or memory right
SBCA, SBCB	Subtract memory from accumulator with borrow
STA, STB	Store accumulator to memory
SUBA, SUBB	Subtract memory from accumulator
TST, TSTA, TSTB	Test accumulator or memory location
TFR R1, R2	Transfer R1 to R2 (R1, R2 = A, B, CC, DP)

NOTE: A, B, CC or DP may be pushed to (pulled from) either stack with PSHS, PSHU (PULS, PULU) instructions.

TABLE 5 — 16-BIT ACCUMULATOR AND MEMORY INSTRUCTIONS

Mnemonic(s)	Operation
ADDD	Add memory to D accumulator
CMPD	Compare memory from D accumulator
EXG D, R	Exchange D with X, Y, S, U or PC
LDD	Load D accumulator from memory
SEX	Sign Extend B accumulator into A accumulator
STD	Store D accumulator to memory
SUBD	Subtract memory from D accumulator
TFR D, R	Transfer D to X, Y, S, U or PC
TFR R, D	Transfer X, Y, S, U or PC to D

NOTE: D may be pushed (pulled) to either stack with PSHS, PSHU (PULS, PULU) instructions.

TABLE 6 — INDEX REGISTER/STACK POINTER INSTRUCTIONS

Instruction	Description
CMPS, CMPU	Compare memory from stack pointer
CMPX, CMPY	Compare memory from index register
EXG R1, R2	Exchange D, X, Y, S, U or PC with D, X, Y, S, U or PC
LEAS, LEAU	Load effective address into stack pointer
LEAX, LEAY	Load effective address into index register
LDS, LDU	Load stack pointer from memory
LDX, LDY	Load index register from memory
PSHS	Push A, B, CC, DP, D, X, Y, U, or PC onto hardware stack
PSHU	Push A, B, CC, DP, D, X, Y, S, or PC onto user stack
PULS	Pull A, B, CC, DP, D, X, Y, U or PC from hardware stack
PULU	Pull A, B, CC, DP, D, X, Y, S or PC from hardware stack
STS, STU	Store stack pointer to memory
STX, STY	Store index register to memory
TFR R1, R2	Transfer D, X, Y, S, U or PC to D, X, Y, S, U or PC
ABX	Add B accumulator to X (unsigned)

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TABLE 7 — BRANCH INSTRUCTIONS

Instruction	Description
	SIMPLE BRANCHES
BEQ, LBEQ	Branch if equal
BNE, LBNE	Branch if not equal
BMI, LBMI	Branch if minus
BPL, LBPL	Branch if plus
BCS, LBCS	Branch if carry set
BCC, LBCC	Branch if carry clear
BVS, LBVS	Branch if overflow set
BVC, LBVC	Branch if overflow clear
	SIGNED BRANCHES
BGT, LBGT	Branch if greater (signed)
BVS, LBVS	Branch if invalid 2's complement result
BGE, LBGE	Branch if greater than or equal (signed)
BEQ, LBEQ	Branch if equal
BNE, LBNE	Branch if not equal
BLE, LBLE	Branch if less than or equal (signed)
BVC, LBVC	Branch if valid 2's complement result
BLT, LBLT	Branch if less than (signed)
	UNSIGNED BRANCHES
BHI, LBHI	Branch if higher (unsigned)
BCC, LBCC	Branch if higher or same (unsigned)
BHS, LBHS	Branch if higher or same (unsigned)
BEQ, LBEQ	Branch if equal
BNE, LBNE	Branch if not equal
BLS, LBLS	Branch if lower or same (unsigned)
BCS, LBCS	Branch if lower (unsigned)
BLO, LBLO	Branch if lower (unsigned)
	OTHER BRANCHES
BSR, LBSR	Branch to subroutine
BRA, LBRA	Branch always
BRN, LBRN	Branch never

TABLE 8 — MISCELLANEOUS INSTRUCTIONS

Instruction	Description
ANDCC	AND condition code register
CWAI	AND condition code register, then wait for interrupt
NOP	No operation
ORCC	OR condition code register
JMP	Jump
JSR	Jump to subroutine
RTI	Return from interrupt
RTS	Return from subroutine
SWI, SWI2, SWI3	Software interrupt (absolute indirect)
SYNC	Synchronize with interrupt line

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TABLE 9 — HEXADECIMAL VALUES OF MACHINE CODES

OP	Mnem	Mode	~	#	OP	Mnem	Mode	~	#	OP	Mnem	Mode	~	#
00	NEG	Direct	6	2	30	LEAX	Indexed	4+	2+	60	NEG	Indexed	6+	2+
01	*	↑			31	LEAY	↕	4+	2+	61	*	↑		
02	*				32	LEAS		4+	2+	62	*			
03	COM		6	2	33	LEAU	Indexed	4+	2+	63	COM		6+	2+
04	LSR		6	2	34	PSHS	Immed	5+	2	64	LSR		6+	2+
05	*				35	PULS	Immed	5+	2	65	*			
06	ROR		6	2	36	PSHU	Immed	5+	2	66	ROR		6+	2+
07	ASR		6	2	37	PULU	Immed	5+	2	67	ASR		6+	2+
08	ASL, LSL		6	2	38	*	–			68	ASL, LSL		6+	2+
09	ROL		6	2	39	RTS	Inherent	5	1	69	ROL		6+	2+
0A	DEC		6	2	3A	ABX	↑	3	1	6A	DEC		6+	2+
0B	*				3B	RTI		6/15	1	6B	*			
0C	INC		6	2	3C	CWAI	↓	≥20	2	6C	INC		6+	2+
0D	TST		6	2	3D	MUL	Inherent	11	1	6D	TST		6+	2+
0E	JMP		3	2	3E	*	–			6E	JMP	↓	3+	2+
0F	CLR	↓ Direct	6	2	3F	SWI	Inherent	19	1	6F	CLR	Indexed	6+	2+
10	Page 2	–	–	–	40	NEGA	Inherent	2	1	70	NEG	Extended	7	3
11	Page 3	–	–	–	41	*	↑			71	*	↑		
12	NOP	Inherent	2	1	42	*				72	*			
13	SYNC	Inherent	≥4	1	43	COMA		2	1	73	COM		7	3
14	*				44	LSRA		2	1	74	LSR		7	3
15	*				45	*				75	*			
16	LBRA	Relative	5	3	46	RORA		2	1	76	ROR		7	3
17	LBSR	Relative	9	3	47	ASRA		2	1	77	ASR		7	3
18	*				48	ASLA, LSLA		2	1	78	ASL, LSL		7	3
19	DAA	Inherent	2	1	49	ROLA		2	1	79	ROL		7	3
1A	ORCC	Immed	3	2	4A	DECA		2	1	7A	DEC		7	3
1B	*	–			4B	*				7B	*			
1C	ANDCC	Immed	3	2	4C	INCA		2	1	7C	INC		7	3
1D	SEX	Inherent	2	1	4D	TSTA		2	1	7D	TST		7	3
1E	EXG	Immed	8	2	4E	*				7E	JMP		4	3
1F	TFR	Immed	6	2	4F	CLRA	↓ Inherent	2	1	7F	CLR	↓ Extended	7	3
20	BRA	Relative	3	2	50	NEGB	Inherent	2	1	80	SUBA	Immed	2	2
21	BRN	↑	3	2	51	*	↑			81	CMPA	↑	2	2
22	BHI		3	2	52	*				82	SBCA		2	2
23	BLS		3	2	53	COMB		2	1	83	SUBD		4	3
24	BHS, BCC		3	2	54	LSRB		2	1	84	ANDA		2	2
25	BLO, BCS		3	2	55	*				85	BITA		2	2
26	BNE		3	2	56	RORB		2	1	86	LDA		2	2
27	BEQ		3	2	57	ASRB		2	1	87	*			
28	BVC		3	2	58	ASLB, LSLB		2	1	88	EORA		2	2
29	BVS		3	2	59	ROLB		2	1	89	ADCA		2	2
2A	BPL		3	2	5A	DECB		2	1	8A	ORA		2	2
2B	BMI		3	2	5B	*				8B	ADDA		2	2
2C	BGE		3	2	5C	INCB		2	1	8C	CMPX	Immed	4	3
2D	BLT		3	2	5D	TSTB		2	1	8D	BSR	Relative	7	2
2E	BGT		3	2	5E	*				8E	LDX	Immed	3	3
2F	BLE	↓ Relative	3	2	5F	CLRB	↓ Inherent	2	1	8F	*			

LEGEND:
~ Number of MPU cycles (less possible push pull or indexed-mode cycles)
# Number of program bytes
* Denotes unused opcode

MC6809E

TABLE 9 – HEXADECIMAL VALUES OF MACHINE CODES (CONTINUED)

OP	Mnem	Mode	~	#
90	SUBA	Direct	4	2
91	CMPA	↑	4	2
92	SBCA		4	2
93	SUBD		6	2
94	ANDA		4	2
95	BITA		4	2
96	LDA		4	2
97	STA		4	2
98	EORA		4	2
99	ADCA		4	2
9A	ORA		4	2
9B	ADDA		4	2
9C	CMPX		6	2
9D	JSR		7	2
9E	LDX		5	2
9F	STX	Direct	5	2
A0	SUBA	Indexed	4+	2+
A1	CMPA	↑	4+	2+
A2	SBCA		4+	2+
A3	SUBD		6+	2+
A4	ANDA		4+	2+
A5	BITA		4+	2+
A6	LDA		4+	2+
A7	STA		4+	2+
A8	EORA		4+	2+
A9	ADCA		4+	2+
AA	ORA		4+	2+
AB	ADDA		4+	2+
AC	CMPX		6+	2+
AD	JSR		7+	2+
AE	LDX		5+	2+
AF	STX	Indexed	5+	2+
B0	SUBA	Extended	5	3
B1	CMPA	↑	5	3
B2	SBCA		5	3
B3	SUBD		7	3
B4	ANDA		5	3
B5	BITA		5	3
B6	LDA		5	3
B7	STA		5	3
B8	EORA		5	3
B9	ADCA		5	3
BA	ORA		5	3
BB	ADDA		5	3
BC	CMPX		7	3
BD	JSR		8	3
BE	LDX		6	3
BF	STX	Extended	6	3

NOTE: All unused opcodes are both undefined and illegal

OP	Mnem	Mode	~	#
C0	SUBB	Immed	2	2
C1	CMPB	↑	2	2
C2	SBCB		2	2
C3	ADDD		4	3
C4	ANDB		2	2
C5	BITB	Immed	2	2
C6	LDB	Immed	2	2
C7	*	↑		
C8	EORB		2	2
C9	ADCB		2	2
CA	ORB		2	2
CB	ADDB		2	2
CC	LDD		3	3
CD	*	↓		
CE	LDU	Immed	3	3
CF	*			
D0	SUBB	Direct	4	2
D1	CMPB	↑	4	2
D2	SBCB		4	2
D3	ADDD		6	2
D4	ANDB		4	2
D5	BITB		4	2
D6	LDB		4	2
D7	STB		4	2
D8	EORB		4	2
D9	ADCB		4	2
DA	ORB		4	2
DB	ADDB		4	2
DC	LDD		5	2
DD	STD		5	2
DE	LDU	↓	5	2
DF	STU	Direct	5	2
E0	SUBB	Indexed	4+	2+
E1	CMPB	↑	4+	2+
E2	SBCB		4+	2+
E3	ADDD		6+	2+
E4	ANDB		4+	2+
E5	BITB		4+	2+
E6	LDB		4+	2+
E7	STB		4+	2+
E8	EORB		4+	2+
E9	ADCB		4+	2+
EA	ORB		4+	2+
EB	ADDB		4+	2+
EC	LDD		5+	2+
ED	STD		5+	2+
EE	LDU	↓	5+	2+
EF	STU	Indexed	5+	2+
F0	SUBB	Extended	5	3
F1	CMPB	↑	5	3
F2	SBCB		5	3
F3	ADDD		7	3
F4	ANDB		5	3
F5	BITB		5	3
F6	LDB		5	3
F7	STB		5	3
F8	EORB		5	3
F9	ADCB		5	3
FA	ORB		5	3
FB	ADDB	Extended	5	3
FC	LDD	Extended	6	3
FD	STD	↑	6	3
FE	LDU	↓	6	3
FF	STU	Extended	6	3

OP	Mnem	Mode	~	#
Page 2 and 3 Machine Codes				
1021	LBRN	Relative	5	4
1022	LBHI	↑	5(6)	4
1023	LBLS		5(6)	4
1024	LBHS, LBCC		5(6)	4
1025	LBCS, LBLO		5(6)	4
1026	LBNE		5(6)	4
1027	LBEQ		5(6)	4
1028	LBVC		5(6)	4
1029	LBVS		5(6)	4
102A	LBPL		5(6)	4
102B	LBMI		5(6)	4
102C	LBGE		5(6)	4
102D	LBLT		5(6)	4
102E	LBGT	↓	5(6)	4
102F	LBLE	Relative	5(6)	4
103F	SWI2	Inherent	20	2
1083	CMPD	Immed	5	4
108C	CMPY	|	5	4
108E	LDY	Immed	4	4
1093	CMPD	Direct	7	3
109C	CMPY	↑	7	3
109E	LDY	↓	6	3
109F	STY	Direct	6	3
10A3	CMPD	Indexed	7+	3+
10AC	CMPY	↑	7+	3+
10AE	LDY	↓	6+	3+
10AF	STY	Indexed	6+	3+
10B3	CMPD	Extended	8	4
10BC	CMPY	↑	8	4
10BE	LDY	↓	7	4
10BF	STY	Extended	7	4
10CE	LDS	Immed	4	4
10DE	LDS	Direct	6	3
10DF	STS	Direct	6	3
10EE	LDS	Indexed	6+	3+
10EF	STS	Indexed	6+	3+
10FE	LDS	Extended	7	4
10FF	STS	Extended	7	4
113F	SWI3	Inherent	20	2
1183	CMPU	Immed	5	4
118C	CMPS	Immed	5	4
1193	CMPU	Direct	7	3
119C	CMPS	Direct	7	3
11A3	CMPU	Indexed	7+	3+
11AC	CMPS	Indexed	7+	3+
11B3	CMPU	Extended	8	4
11BC	CMPS	Extended	8	4

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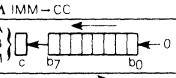
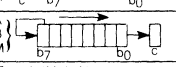
FIGURE 18 — PROGRAMMING AID

Instruction	Forms	Addressing Modes: Immediate Op	Immediate ~	Immediate #	Direct Op	Direct ~	Direct #	Indexed Op	Indexed ~	Indexed #	Extended Op	Extended ~	Extended #	Inherent Op	Inherent ~	Inherent #	Description	5 H	3 N	2 Z	1 V	0 C
ABX														3A	3	1	B + X → X (Unsigned)	•	•	•	•	•
ADC	ADCA	89	2	2	99	4	2	A9	4+	2+	B9	5	3				A + M + C → A	↕	↕	↕	↕	↕
	ADCB	C9	2	2	D9	4	2	E9	4+	2+	F9	5	3				B + M + C → B	↕	↕	↕	↕	↕
ADD	ADDA	8B	2	2	9B	4	2	AB	4+	2+	BB	5	3				A + M → A	↕	↕	↕	↕	↕
	ADDB	CB	2	2	DB	4	2	EB	4+	2+	FB	5	3				B + M → B	↕	↕	↕	↕	↕
	ADDD	C3	4	3	D3	6	2	E3	6+	2+	F3	7	3				D + M:M + 1 → D	•	↕	↕	↕	↕
AND	ANDA	84	2	2	94	4	2	A4	4+	2+	B4	5	3				A ∧ M → A	•	↕	↕	0	•
	ANDB	C4	2	2	D4	4	2	E4	4+	2+	F4	5	3				B ∧ M → B	•	↕	↕	0	•
	ANDCC	1C	3	2													CC ∧ IMM → CC					7
ASL	ASLA													48	2	1		8	↕	↕	↕	↕
	ASLB													58	2	1		8	↕	↕	↕	↕
	ASL				08	6	2	68	6+	2+	78	7	3					8	↕	↕	↕	↕
ASR	ASRA													47	2	1		8	↕	↕	•	↕
	ASRB													57	2	1		8	↕	↕	•	↕
	ASR				07	6	2	67	6+	2+	77	7	3					8	↕	↕	•	↕
BIT	BITA	85	2	2	95	4	2	A5	4+	2+	B5	5	3				Bit Test A (M ∧ A)	•	↕	↕	0	•
	BITB	C5	2	2	D5	4	2	E5	4+	2+	F5	5	3				Bit Test B (M ∧ B)	•	↕	↕	0	•
CLR	CLRA													4F	2	1	0 → A	•	0	1	0	0
	CLRB													5F	2	1	0 → B	•	0	1	0	0
	CLR				0F	6	2	6F	6+	2+	7F	7	3				0 → M	•	0	1	0	0
CMP	CMPA	81	2	2	91	4	2	A1	4+	2+	B1	5	3				Compare M from A	8	↕	↕	↕	↕
	CMPB	C1	2	2	D1	4	2	E1	4+	2+	F1	5	3				Compare M from B	8	↕	↕	↕	↕
	CMPD	10	5	4	10	7	3	10	7+	3+	10	8	4				Compare M:M + 1 from D	•	↕	↕	↕	↕
		83			93			A3			B3											
	CMPS	11	5	4	11	7	3	11	7+	3+	11	8	4				Compare M:M + 1 from S	•	↕	↕	↕	↕
		8C			9C			AC			BC											
	CMPU	11	5	4	11	7	3	11	7+	3+	11	8	4				Compare M:M + 1 from U	•	↕	↕	↕	↕
		83			93			A3			B3											
	CMPX	8C	4	3	9C	6	2	AC	6+	2+	BC	7	3				Compare M:M + 1 from X	•	↕	↕	↕	↕
	CMPY	10	5	4	10	7	3	10	7+	3+	10	8	4				Compare M:M + 1 from Y	•	↕	↕	↕	↕
		8C			9C			AC			BC											
COM	COMA													43	2	1	$\overline{A} \rightarrow A$	•	↕	↕	0	1
	COMB													53	2	1	$\overline{B} \rightarrow B$	•	↕	↕	0	1
	COM				03	6	2	63	6+	2+	73	7	3				$\overline{M} \rightarrow M$	•	↕	↕	0	1
CWAI		3C	≥20	2													CC ∧ IMM → CC Wait for Interrupt					7
DAA														19	2	1	Decimal Adjust A	•	↕	↕	0	↕
DEC	DECA													4A	2	1	A − 1 → A	•	↕	↕	↕	•
	DECB													5A	2	1	B − 1 → B	•	↕	↕	↕	•
	DEC				0A	6	2	6A	6+	2+	7A	7	3				M − 1 → M	•	↕	↕	↕	•
EOR	EORA	88	2	2	98	4	2	A8	4+	2+	B8	5	3				A ⊻ M → A	•	↕	↕	0	•
	EORB	C8	2	2	D8	4	2	E8	4+	2+	F8	5	3				B ⊻ M → B	•	↕	↕	0	•
EXG	R1, R2	1E	8	2													R1 ↔ R2[2]	•	•	•	•	•
INC	INCA													4C	2	1	A + 1 → A	•	↕	↕	↕	•
	INCB													5C	2	1	B + 1 → B	•	↕	↕	↕	•
	INC				0C	6	2	6C	6+	2+	7C	7	3				M + 1 → M	•	↕	↕	↕	•
JMP					0E	3	2	6E	3+	2+	7E	4	3				EA[3] → PC	•	•	•	•	•
JSR					9D	7	2	AD	7+	2+	BD	8	3				Jump to Subroutine	•	•	•	•	•
LD	LDA	86	2	2	96	4	2	A6	4+	2+	B6	5	3				M → A	•	↕	↕	0	•
	LDB	C6	2	2	D6	4	2	E6	4+	2+	F6	5	3				M → B	•	↕	↕	0	•
	LDD	CC	3	3	DC	5	2	EC	5+	2+	FC	6	3				M:M + 1 → D	•	↕	↕	0	•
	LDS	10	4	4	10	6	3	10	6+	3+	10	7	4				M:M + 1 → S	•	↕	↕	0	•
		CE			DE			EE			FE											
	LDU	CE	3	3	DE	5	2	EE	5+	2+	FE	6	3				M:M + 1 → U	•	↕	↕	0	•
	LDX	8E	3	3	9E	5	2	AE	5+	2+	BE	6	3				M:M + 1 → X	•	↕	↕	0	•
	LDY	10	4	4	10	6	3	10	6+	3+	10	7	4				M:M + 1 → Y	•	↕	↕	0	•
		8E			9E			AE			BE											
LEA	LEAS							32	4+	2+							EA[3] → S	•	•	•	•	•
	LEAU							33	4+	2+							EA[3] → U	•	•	•	•	•
	LEAX							30	4+	2+							EA[3] → X	•	•	↕	•	•
	LEAY							31	4+	2+							EA[3] → Y	•	•	↕	•	•

LEGEND:

OP Operation Code (Hexadecimal)
~ Number of MPU Cycles
# Number of Program Bytes
+ Arithmetic Plus
− Arithmetic Minus
• Multiply
$\overline{M}$ Complement of M
→ Transfer Into
H Half-carry (from bit 3)
N Negative (sign bit)
Z Zero result
V Overflow, 2's complement
C Carry from ALU
↕ Test and set if true, cleared otherwise
• Not Affected
CC Condition Code Register
: Concatenation
V Logical or
∧ Logical and
⊻ Logical Exclusive or

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FIGURE 18 — PROGRAMMING AID (CONTINUED)

Instruction	Forms	Addressing Modes: Immediate Op	Immediate ~	Immediate #	Direct Op	Direct ~	Direct #	Indexed[1] Op	Indexed[1] ~	Indexed[1] #	Extended Op	Extended ~	Extended #	Inherent Op	Inherent ~	Inherent #	Description	5 H	3 N	2 Z	1 V	0 C
LSL	LSLA													48	2	1	A, B, M } ← 0	•	↕	↕	↕	↕
	LSLB													58	2	1		•	↕	↕	↕	↕
	LSL				08	6	2	68	6+	2+	78	7	3				c b7 b0	•	↕	↕	↕	↕
LSR	LSRA													44	2	1	A, B, M } 0 →	•	0	↕	•	↕
	LSRB													54	2	1		•	0	↕	•	↕
	LSR				04	6	2	64	6+	2+	74	7	3				b7 b0 c	•	0	↕	•	↕
MUL														3D	11	1	A × B → D (Unsigned)	•	•	↕	•	9
NEG	NEGA													40	2	1	$\overline{A}$ + 1 → A	↕	↕	↕	↕	↕
	NEGB													50	2	1	$\overline{B}$ + 1 → B	↕	↕	↕	↕	↕
	NEG				00	6	2	60	6+	2+	70	7	3				$\overline{M}$ + 1 → M	↕	↕	↕	↕	↕
NOP														12	2	1	No Operation	•	•	•	•	•
OR	ORA	8A	2	2	9A	4	2	AA	4+	2+	BA	5	3				A V M → A	•	↕	↕	0	•
	ORB	CA	2	2	DA	4	2	EA	4+	2+	FA	5	3				B V M → B	•	↕	↕	0	•
	ORCC	1A	3	2													CC V IMM → CC					7
PSH	PSHS	34	5+[4]	2													Push Registers on S Stack	•	•	•	•	•
	PSHU	36	5+[4]	2													Push Registers on U Stack	•	•	•	•	•
PUL	PULS	35	5+[4]	2													Pull Registers from S Stack	•	•	•	•	•
	PULU	37	5+[4]	2													Pull Registers from U Stack	•	•	•	•	•
ROL	ROLA													49	2	1	A, B, M } ←	•	↕	↕	↕	↕
	ROLB													59	2	1		•	↕	↕	↕	↕
	ROL				09	6	2	69	6+	2+	79	7	3				c b7 b0	•	↕	↕	↕	↕
ROR	RORA													46	2	1	A, B, M } →	•	↕	↕	•	↕
	RORB													56	2	1		•	↕	↕	•	↕
	ROR				06	6	2	66	6+	2+	76	7	3				c b7 b0	•	↕	↕	•	↕
RTI														3B	6/15	1	Return From Interrupt					7
RTS														39	5	1	Return from Subroutine	•	•	•	•	•
SBC	SBCA	82	2	2	92	4	2	A2	4+	2+	B2	5	3				A − M − C → A	8	↕	↕	↕	↕
	SBCB	C2	2	2	D2	4	2	E2	4+	2+	F2	5	3				B − M − C → B	8	↕	↕	↕	↕
SEX														1D	2	1	Sign Extend B into A	•	↕	↕	0	•
ST	STA				97	4	2	A7	4+	2+	B7	5	3				A → M	•	↕	↕	0	•
	STB				D7	4	2	E7	4+	2+	F7	5	3				B → M	•	↕	↕	0	•
	STD				DD	5	2	ED	5+	2+	FD	6	3				D → M:M + 1	•	↕	↕	0	•
	STS				10 DF	6	3	10 EF	6+	3+	10 FF	7	4				S → M:M + 1	•	↕	↕	0	•
	STU				DF	5	2	EF	5+	2+	FF	6	3				U → M:M + 1	•	↕	↕	0	•
	STX				9F	5	2	AF	5+	2+	BF	6	3				X → M:M + 1	•	↕	↕	0	•
	STY				10 9F	6	3	10 AF	6+	3+	10 BF	7	4				Y → M:M + 1	•	↕	↕	0	•
SUB	SUBA	80	2	2	90	4	2	A0	4+	2+	B0	5	3				A − M → A	8	↕	↕	↕	↕
	SUBB	C0	2	2	D0	4	2	E0	4+	2+	F0	5	3				B − M → B	8	↕	↕	↕	↕
	SUBD	83	4	3	93	6	2	A3	6+	2+	B3	7	3				D − M:M + 1 → D	•	↕	↕	↕	↕
SWI	SWI[6]													3F	19	1	Software Interrupt 1	•	•	•	•	•
	SWI2[6]													10 3F	20	2	Software Interrupt 2	•	•	•	•	•
	SWI3[6]													11 3F	20	1	Software Interrupt 3	•	•	•	•	•
SYNC														13	≥4	1	Synchronize to Interrupt	•	•	•	•	•
TFR	R1, R2	1F	6	2													R1 → R2[2]	•	•	•	•	•
TST	TSTA													4D	2	1	Test A	•	↕	↕	0	•
	TSTB													5D	2	1	Test B	•	↕	↕	0	•
	TST				0D	6	2	6D	6+	2+	7D	7	3				Test M	•	↕	↕	0	•

NOTES:

1. This column gives a base cycle and byte count. To obtain total count, add the values obtained from the INDEXED ADDRESSING MODE table, Table 2.
2. R1 and R2 may be any pair of 8 bit or any pair of 16 bit registers.
   The 8 bit registers are: A, B, CC, DP
   The 16 bit registers are: X, Y, U, S, D, PC
3. EA is the effective address.
4. The PSH and PUL instructions require 5 cycles plus 1 cycle for each **byte** pushed or pulled.
5. 5(6) means: 5 cycles if branch not taken, 6 cycles if taken (Branch instructions).
6. SWI sets I and F bits. SWI2 and SWI3 do not affect I and F.
7. Conditions Codes set as a direct result of the instruction.
8. Vaue of half-carry flag is undefined.
9. Special Case — Carry set if b7 is SET.

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FIGURE 18 — PROGRAMMING AID (CONTINUED)

Branch Instructions

Instruction	Forms	Addressing Mode Relative OP	~	#	Description	5 H	3 N	2 Z	1 V	0 C
BCC	BCC	24	3	2	Branch C = 0	•	•	•	•	•
	LBCC	10 24	5(6)	4	Long Branch C = 0	•	•	•	•	•
BCS	BCS	25	3	2	Branch C = 1	•	•	•	•	•
	LBCS	10 25	5(6)	4	Long Branch C = 1	•	•	•	•	•
BEQ	BEQ	27	3	2	Branch Z = 1	•	•	•	•	•
	LBEQ	10 27	5(6)	4	Long Branch Z = 1	•	•	•	•	•
BGE	BGE	2C	3	2	Branch ≥ Zero	•	•	•	•	•
	LBGE	10 2C	5(6)	4	Long Branch ≥ Zero	•	•	•	•	•
BGT	BGT	2E	3	2	Branch > Zero	•	•	•	•	•
	LBGT	10 2E	5(6)	4	Long Branch > Zero	•	•	•	•	•
BHI	BHI	22	3	2	Branch Higher	•	•	•	•	•
	LBHI	10 22	5(6)	4	Long Branch Higher	•	•	•	•	•
BHS	BHS	24	3	2	Branch Higher or Same	•	•	•	•	•
	LBHS	10 24	5(6)	4	Long Branch Higher or Same	•	•	•	•	•
BLE	BLE	2F	3	2	Branch ≤ Zero	•	•	•	•	•
	LBLE	10 2F	5(6)	4	Long Branch ≤ Zero	•	•	•	•	•
BLO	BLO	25	3	2	Branch lower	•	•	•	•	•
	LBLO	10 25	5(6)	4	Long Branch Lower	•	•	•	•	•
BLS	BLS	23	3	2	Branch Lower or Same	•	•	•	•	•
	LBLS	10 23	5(6)	4	Long Branch Lower or Same	•	•	•	•	•
BLT	BLT	2D	3	2	Branch < Zero	•	•	•	•	•
	LBLT	10 2D	5(6)	4	Long Branch < Zero	•	•	•	•	•
BMI	BMI	2B	3	2	Branch Minus	•	•	•	•	•
	LBMI	10 2B	5(6)	4	Long Branch Minus	•	•	•	•	•
BNE	BNE	26	3	2	Branch Z = 0	•	•	•	•	•
	LBNE	10 26	5(6)	4	Long Branch Z = 0	•	•	•	•	•
BPL	BPL	2A	3	2	Branch Plus	•	•	•	•	•
	LBPL	10 2A	5(6)	4	Long Branch Plus	•	•	•	•	•
BRA	BRA	20	3	2	Branch Always	•	•	•	•	•
	LBRA	16	5	3	Long Branch Always	•	•	•	•	•
BRN	BRN	21	3	2	Branch Never	•	•	•	•	•
	LBRN	10 21	5	4	Long Branch Never	•	•	•	•	•
BSR	BSR	8D	7	2	Branch to Subroutine	•	•	•	•	•
	LBSR	17	9	3	Long Branch to Subroutine	•	•	•	•	•
BVC	BVC	28	3	2	Branch V = 0	•	•	•	•	•
	LBVC	10 28	5(6)	4	Long Branch V = 0	•	•	•	•	•
BVS	BVS	29	3	2	Branch V = 1	•	•	•	•	•
	LBVS	10 29	5(6)	4	Long Branch V = 1	•	•	•	•	•

SIMPLE BRANCHES

	OP	~	#
BRA	20	3	2
LBRA	16	5	3
BRN	21	3	2
LBRN	1021	5	4
BSR	8D	7	2
LBSR	17	9	3

SIMPLE CONDITIONAL BRANCHES (Notes 1-4)

Test	True	OP	False	OP
N = 1	BMI	2B	BPL	2A
Z = 1	BEQ	27	BNE	26
V = 1	BVS	29	BVC	28
C = 1	BCS	25	BCC	24

SIGNED CONDITIONAL BRANCHES (Notes 1-4)

Test	True	OP	False	OP
r > m	BGT	2E	BLE	2F
r ≥ m	BGE	2C	BLT	2D
r = m	BEQ	27	BNE	26
r ≤ m	BLE	2F	BGT	2E
r < m	BLT	2D	BGE	2C

UNSIGNED CONDITIONAL BRANCHES (Notes 1-4)

Test	True	OP	False	OP
r > m	BHI	22	BLS	23
r ≥ m	BHS	24	BLO	25
r = m	BEQ	27	BNE	26
r ≤ m	BLS	23	BHI	22
r < m	BLO	25	BHS	24

NOTES:
1. All conditional branches have both short and long variations.
2. All short branches are 2 bytes and require 3 cycles.
3. All conditional long branches are formed by prefixing the short branch opcode with $10 and using a 16-bit destination offset.
4. All conditional long branches require 4 bytes and 6 cycles if the branch is taken or 5 cycles if the branch is not taken.
5. 5(6) means: 5 cycles if branch not taken, 6 cycles if taken.

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INDEXED ADDRESSING MODES

Type	Forms	Nondirect Assembler Form	Nondirect Post-Byte Opcode	Nondirect + ~	Nondirect + #	Indirect Assembler Form	Indirect Post-Byte Opcode	Indirect + ~	Indirect + #
Constant Offset From R	No Offset	, R	1RR00100	0	0	[, R]	1RR10100	3	0
	5-Bit Offset	n, R	0RRnnnnn	1	0	defaults to 8-bit			
	8-Bit Offset	n, R	1RR01000	1	1	[n, R]	1RR11000	4	1
	16-Bit Offset	n, R	1RR01001	4	2	[n, R]	1RR11001	7	2
Accumulator Offset From R	A – Register Offset	A, R	1RR00110	1	0	[A, R]	1RR10110	4	0
	B – Register Offset	B, R	1RR00101	1	0	[B, R]	1RR10101	4	0
	D – Register Offset	D, R	1RR01011	4	0	[D, R]	1RR11011	7	0
Auto Increment/Decrement R	Increment By 1	, R+	1RR00000	2	0	not allowed			
	Increment By 2	, R + +	1RR00001	3	0	[, R + +]	1RR10001	6	0
	Decrement By 1	, -R	1RR00010	2	0	not allowed			
	Decrement By 2	, --R	1RR00011	3	0	[, --R]	1RR10011	6	0
Constant Offset From PC	8-Bit Offset	n, PCR	1XX01100	1	1	[n, PCR]	1XX11100	4	1
	16-Bit Offset	n, PCR	1XX01101	5	2	[n, PCR]	1XX11101	8	2
Extended Indirect	16-Bit Address	–	–	–	–	[n]	10011111	5	2

R = X, Y, U, or S
X = Don't Care

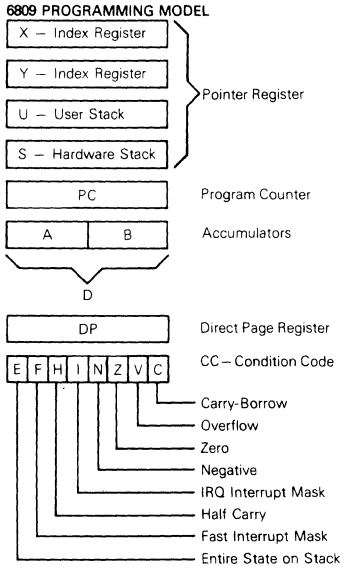
RR: 00 = X 10 = U
01 = Y 11 = S

INDEXED ADDRESSING POSTBYTE REGISTER BIT ASSIGNMENTS

Post-Byte Register Bit 7	6	5	4	3	2	1	0	Indexed Addressing Mode
0	R	R	x	x	x	x	x	EA = , R + 5 Bit Offset
1	R	R	0	0	0	0	0	, R +
1	R	R	I	0	0	0	1	, R + +
1	R	R	0	0	0	1	0	,- R
1	R	R	I	0	0	1	1	, -- R
1	R	R	I	0	1	0	0	EA = , R + 0 Offset
1	R	R	I	0	1	0	1	EA = , R + ACCB Offset
1	R	R	I	0	1	1	0	EA = , R + ACCA Offset
1	R	R	I	1	0	0	0	EA = , R+ 8-Bit Offset
1	R	R	I	1	0	0	1	EA = , R + 16-Bit Offset
1	R	R	I	1	0	1	1	EA = , R + D Offset
1	x	x	I	1	1	0	0	EA = , PC + 8-Bit Offset
1	x	x	I	1	1	0	1	EA = , PC + 16-Bit Offset
1	R	R	1	1	1	1	1	EA = [, Address]

Addressing Mode Field
Indirect Field
(Sign bit when b7 = 0)
Register Field: RR
00 = X
01 = Y
10 = U
11 = S
X = Don't Care

6809 PROGRAMMING MODEL



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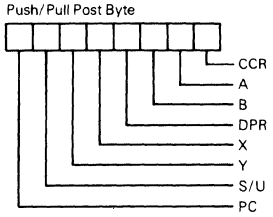
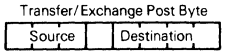
Push/Pull Post Byte



Transfer/Exchange Post Byte



Register Field

0000 = D (A-B)	0101 = PC
0001 = X	1000 = A
0010 = Y	1001 = B
0011 = U	1010 = CCR
0100 = S	1011 = DPR

6809 Stacking Order

Pull Order ↓
CC
A
B
DP
X Hi
X Lo
Y Hi
Y Lo
U/S Hi
U/S Lo
PC Hi
PC Lo
↑ Push Order
↓ Increasing Memory

6809 Vectors	
FFFE	Restart
FFFC	NMI
FFFA	SWI
FFF8	IRQ
FFF6	FIRQ
FFF4	SW12
FFF2	SW13
FFF0	Reserved

ORDERING INFORMATION

Package Type	Frequency	Temperature Range	Order Number
Ceramic L Suffix	1.0 MHz	0°C to 70°C	MC6809EL
	1.0 MHz	−40°C to 85°C	MC6809ECL
	1.5 MHz	0°C to 70°C	MC68A09EL
	1.5 MHz	−40°C to 85°C	MC68A09ECL
	2.0 MHz	0°C to 70°C	MC68B09EL
	2.0 MHz	−40°C to 85°C	MC68B09ECL
Plastic P Suffix	1.0 MHz	0°C to 70°C	MC6809EP
	1.0 MHz	−40°C to 85°C	MC6809ECP
	1.5 MHz	0°C to 70°C	MC68A09EP
	1.5 MHz	−40°C to 85°C	MC68A09ECP
	2.0 MHz	0°C to 70°C	MC68B09EP
	2.0 MHz	−40°C to 85°C	MC68B09ECP
Cerdip S Suffix	1.0 MHz	0°C to 70°C	MC6809ES
	1.0 MHz	−40°C to 85°C	MC6809ECS
	1.5 MHz	0°C to 70°C	MC68A09ES
	1.5 MHz	−40°C to 85°C	MC68A09ECS
	2.0 MHz	0°C to 70°C	MC68B09ES
	2.0 MHz	−40°C to 85°C	MC68B09ECS

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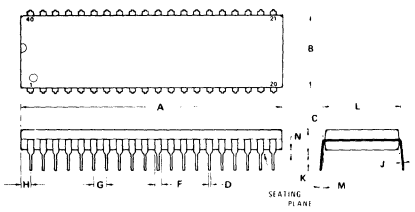
MC6809E

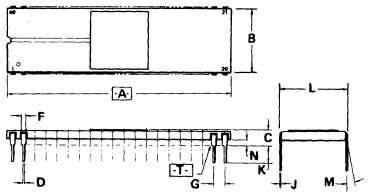
PACKAGE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

P SUFFIX
PLASTIC PACKAGE
CASE 711-03

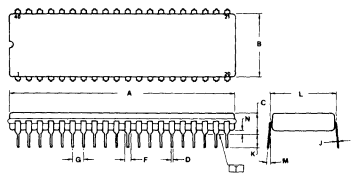


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	14.63	15.49	0.576	0.610
C	2.79	4.32	0.110	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.57	0.100	0.180
L	14.99	15.65	0.590	0.616
M	–	10°	–	10°
N	1.02	1.52	0.040	0.060

NOTES:
1. DIMENSION -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:

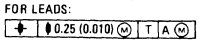
3. -T- IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

L SUFFIX
CERAMIC PACKAGE
CASE 715-05



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.31	53.24	2.020	2.096
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIMENSION ~~-A-~~ IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:



3. -T- IS SEATING PLANE.
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSION A AND B INCLUDES MENISCUS.

S SUFFIX
CERDIP PACKAGE
CASE 734-03

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MC6809E

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MC6850

ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

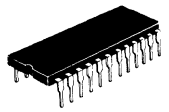
The MC6850 Asynchronous Communications Interface Adapter provides the data formatting and control to interface serial asynchronous data communications information to bus organized systems such as the MC6800 Microprocessing Unit.

The bus interface of the MC6850 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bidirectional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable Control Register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation, three control lines are provided. These lines allow the ACIA to interface directly with the MC6860L 0-600 bps digital modem.

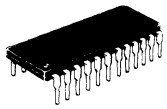
- 8- and 9-Bit Transmission
- Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Programmable Control Register
- Optional ÷1, ÷16, and ÷64 Clock Modes
- Up to 1.0 Mbps Transmission
- False Start Bit Deletion
- Peripheral/Modem Control Functions
- Double Buffered
- One- or Two-Stop Bit Operation

MOS
(N-CHANNEL, SILICON-GATE)

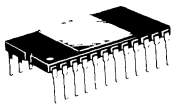
ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER



S SUFFIX
CERDIP PACKAGE
CASE 623

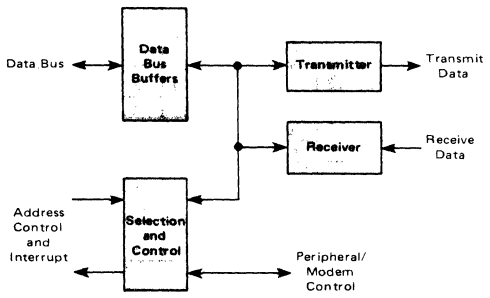


P SUFFIX
PLASTIC PACKAGE
CASE 709

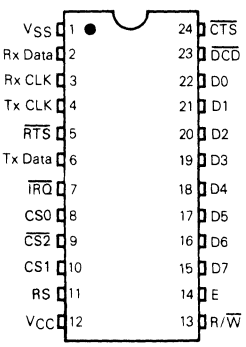


L SUFFIX
CERAMIC PACKAGE
CASE 716

MC6850 ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER BLOCK DIAGRAM



PIN ASSIGNMENT



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MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range MC6850, MC68A50, MC68B50 MC6850C, MC68A50C	T_A	T_L to T_H 0 to 70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Plastic Ceramic Cerdip	θ_{JA}	 120 60 65	°C/W

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A ≡ Ambient Temperature, °C

θ_{JA} ≡ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{PORT}$

$P_{INT} \equiv I_{CC} \times V_{CC}$, Watts — Chip Internal Power

P_{PORT} ≡ Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, $T_A = T_L$ to T_H unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	V_{SS} + 2.0	–	V_{CC}	V
Input Low Voltage		V_{IL}	V_{SS} − 0.3	–	V_{SS} + 0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V)	R/$\overline{W}$, CS0, CS1, $\overline{CS2}$, Enable RS, Rx D, Rx C, $\overline{CTS}$, $\overline{DCD}$	I_{in}	–	1.0	2.5	μA
Hi-Z (Off State) Input Current (V_{in} = 0.4 to 2.4 V)	D0-D7	I_{TSI}	–	2.0	10	μA
Output High Voltage (I_{Load} = −205 μA, Enable Pulse Width < 25 μs) (I_{Load} = −100 μA, Enable Pulse Width < 25 μs)	D0-D7 Tx Data, $\overline{RTS}$	V_{OH}	V_{SS} + 2.4 V_{SS} + 2.4	– –	– –	V
Output Low Voltage (I_{Load} = 1.6 mA, Enable Pulse Width < 25 μs)		V_{OL}	–	–	V_{SS} + 0.4	V
Output Leakage Current (Off State) (V_{OH} = 2.4 V)	$\overline{IRQ}$	I_{LOH}	–	1.0	10	μA
Internal Power Dissipation (Measured at T_A = 0°C)		P_{INT}	–	300	525*	mW
Internal Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	D0-D7 E, Tx CLK, Rx CLK, R/$\overline{W}$, RS, Rx Data, CS0, CS1, $\overline{CS2}$, $\overline{CTS}$, $\overline{DCD}$	C_{in}	– –	10 7.0	12.5 7.5	pF
Output Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	RTS, Tx Data $\overline{IRQ}$	C_{out}	– –	– –	10 5.0	pF

*For temperatures less than T_A = 0°C, P_{INT} maximum will increase.

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SERIAL DATA TIMING CHARACTERISTICS

Characteristic		Symbol	MC6850		MC68A50		MC68B50		Unit
			Min	Max	Min	Max	Min	Max	
Data Clock Pulse Width, Low (See Figure 1)	÷16, ÷64 Modes	PW_{CL}	600	–	450	–	280	–	ns
	÷1 Mode		900	–	650	–	500	–	
Data Clock Pulse Width, High (See Figure 2)	÷16, ÷64 Modes	PW_{CH}	600	–	450	–	280	–	ns
	÷1 Mode		900	–	650	–	500	–	
Data Clock Frequency	÷16, ÷64 Modes	f_C	–	0.8	–	1.0	–	1.5	MHz
	÷1 Mode		–	500	–	750	–	1000	kHz
Data Clock-to-Data Delay for Transmitter (See Figure 3)		t_{TDD}	–	600	–	540	–	460	ns
Receive Data Setup Time (See Figure 4)	÷1 Mode	t_{RDS}	250	–	100	–	30	–	ns
Receive Data Hold Time (See Figure 5)	÷1 Mode	t_{RDH}	250	–	100	–	30	–	ns
Interrupt Request Release Time (See Figure 6)		t_{IR}	–	1.2	–	0.9	–	0.7	μs
Request-to-Send Delay Time (See Figure 6)		t_{RTS}	–	560	–	480	–	400	ns
Input Rise and Fall Times (or 10% of the pulse width if smaller)		t_r, t_f	–	1.0	–	0.5	–	0.25	μs

FIGURE 1 — CLOCK PULSE WIDTH, LOW-STATE

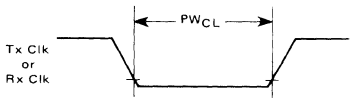


FIGURE 2 — CLOCK PULSE WIDTH, HIGH-STATE

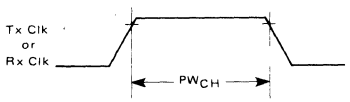


FIGURE 3 — TRANSMIT DATA OUTPUT DELAY

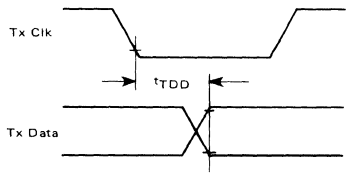


FIGURE 4 — RECEIVE DATA SETUP TIME (÷1 Mode)

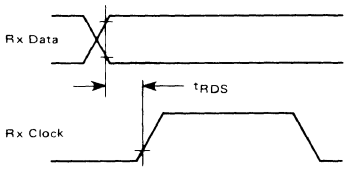


FIGURE 5 — RECEIVE DATA HOLD TIME (÷1 Mode)

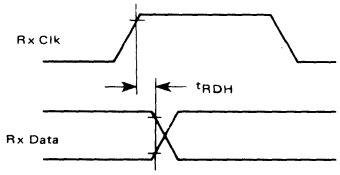
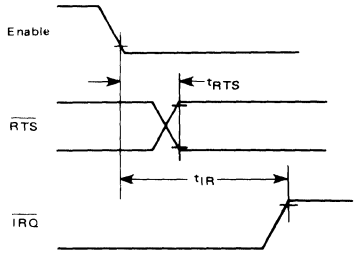


FIGURE 6 — REQUEST-TO-SEND DELAY AND INTERRUPT-REQUEST RELEASE TIMES



Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

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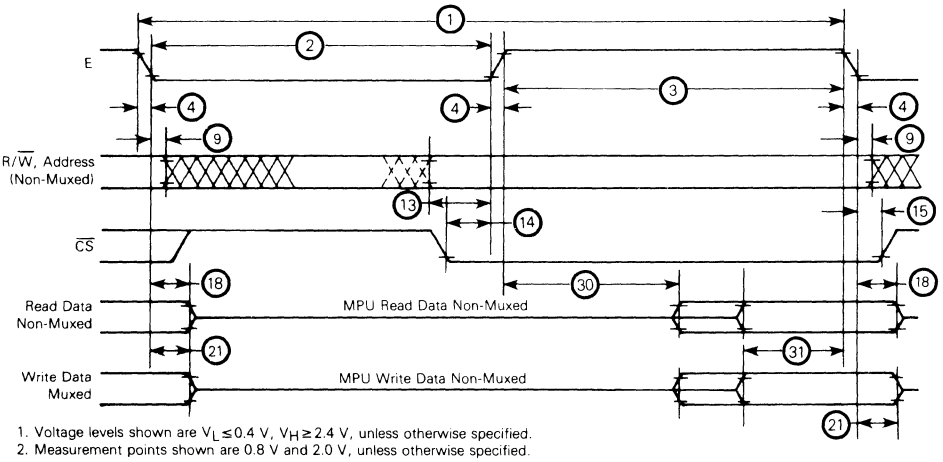
BUS TIMING CHARACTERISTICS (See Notes 1 and 2 and Figure 7)

Ident. Number	Characteristic	Symbol	MC6850		MC68A50		MC68B50		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1.0	10	0.67	10	0.5	10	μs
2	Pulse Width, E Low	PW_{EL}	430	9500	280	9500	210	9500	ns
3	Pulse Width, E High	PW_{EH}	450	9500	280	9500	220	9500	ns
4	Clock Rise and Fall Time	t_r, t_f	–	25	–	25	–	20	ns
9	Address Hold Time	t_{AH}	10	–	10	–	10	–	ns
13	Address Setup Time Before E	t_{AS}	80	–	60	–	40	–	ns
14	Chip Select Setup Time Before E	t_{CS}	80	–	60	–	40	–	ns
15	Chip Select Hold Time	t_{CH}	10	–	10	–	10	–	ns
18	Read Data Hold Time	t_{DHR}	20	50*	20	50*	20	50*	ns
21	Write Data Hold Time	t_{DHW}	10	–	10	–	10	–	ns
30	Output Data Delay Time	t_{DDR}	–	290	–	180	–	150	ns
31	Input Data Setup Time	t_{DSW}	165	–	80	–	60	–	ns

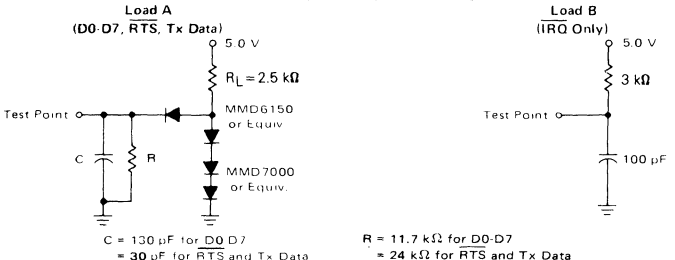
*The data bus output buffers are no longer sourcing or sinking current by t_{DHR}max (High Impedance).

FIGURE 7 – BUS TIMING CHARACTERISTICS



1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

FIGURE 8 – BUS TIMING TEST LOADS



C = 130 pF for D0-D7
= 30 pF for RTS and Tx Data

R = 11.7 kΩ for D0-D7
= 24 kΩ for RTS and Tx Data

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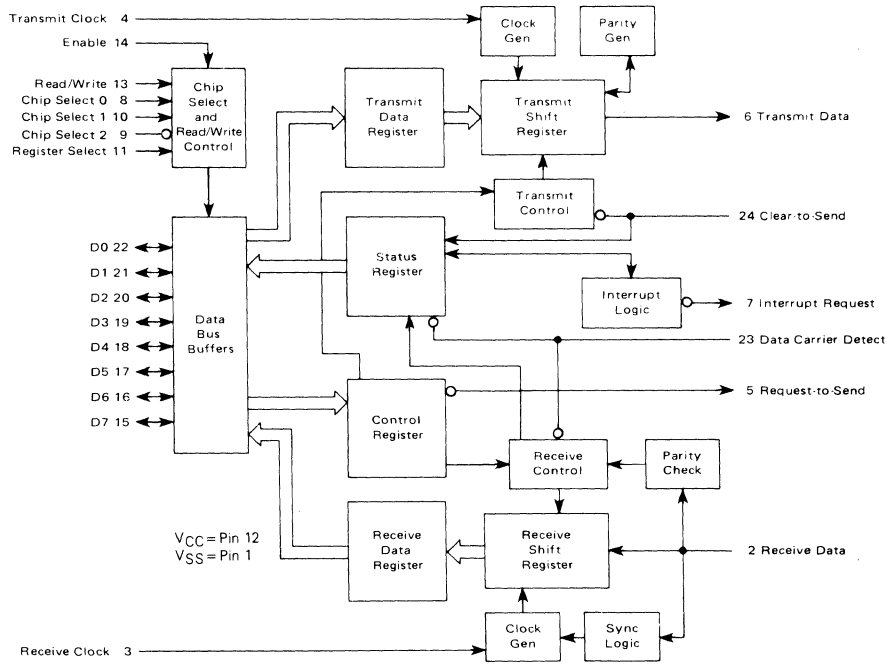
FIGURE 9 — EXPANDED BLOCK DIAGRAM



DEVICE OPERATION

At the bus interface, the ACIA appears as two addressable memory locations. Internally, there are four registers: two read-only and two write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and three peripheral/modem control lines.

POWER ON/MASTER RESET

The master reset (CR0, CR1) should be set during system initialization to insure the reset condition and prepare for programming the ACIA functional configuration when the communications channel is required. During the first master reset, the $\overline{IRQ}$ and $\overline{RTS}$ outputs are held at level 1. On all other master resets, the $\overline{RTS}$ output can be programmed high or low with the $\overline{IRQ}$ output held high. Control bits CR5 and CR6 should also be programmed to define the state of $\overline{RTS}$ whenever master reset is utilized. The ACIA also contains internal power-on reset logic to detect the power line turn-on transition and hold the chip in a reset state to prevent erroneous output transitions prior to initialization. This circuitry depends on clean power turn-on transitions. The power-on reset is released by means of the bus-programmed master reset which must be applied prior to operating the ACIA. After master resetting the ACIA, the programmable Control Register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none), etc.

TRANSMIT

A typical transmitting sequence consists of reading the ACIA Status Register either as a result of an interrupt or in the ACIA's turn in a polling sequence. A character may be written into the Transmit Data Register if the status read operation has indicated that the Transmit Data Register is empty. This character is transferred to a Shift Register where it is serialized and transmitted from the Transmit Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the Data Register, the Status Register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted (because of

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double buffering). The second character will be automatically transferred into the Shift Register when the first character transmission is completed. This sequence continues until all the characters have been transmitted.

RECEIVE

Data is received from a peripheral by means of the Receive Data input. A divide-by-one clock ratio is provided for an externally synchronized clock (to its data) while the divide-by-16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide-by-16 and 64 modes is initiated by the detection of 8 or 32 low samples on the receive line in the divide-by-16 and 64 modes respectively. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the Status Register along with framing error, overrun error, and Receive Data Register full. In a typical receiving sequence, the Status Register is read to determine if a character has been received from a peripheral. If the Receiver Data Register is full, the character is placed on the 8-bit ACIA bus when a Read Data command is received from the MPU. When parity has been selected for a 7-bit word (7 bits plus parity), the receiver strips the parity bit (D7 = 0) so that data alone is transferred to the MPU. This feature reduces MPU programming. The Status Register can continue to be read to determine when another character is available in the Receive Data Register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

INPUT/OUTPUT FUNCTIONS

ACIA INTERFACE SIGNALS FOR MPU

The ACIA interfaces to the M6800 MPU with an 8-bit bidirectional data bus, three chip select lines, a register select line, an interrupt request line, read/write line, and enable line. These signals permit the MPU to have complete control over the ACIA.

ACIA Bidirectional Data (D0-D7) — The bidirectional data lines (D0-D7) allow for data transfer between the ACIA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an ACIA read operation.

ACIA Enable (E) — The Enable signal, E, is a high-impedance TTL-compatible input that enables the bus input/output data buffers and clocks data to and from the ACIA. This signal will normally be a derivative of the MC6800 $\phi 2$ Clock or MC6809 E clock.

Read/Write (R/$\overline{W}$) — The Read/Write line is a high-impedance input that is TTL compatible and is used to control the direction of data flow through the ACIA's input/output data bus interface. When Read/Write is high (MPU Read cycle), ACIA output drivers are turned on and a selected register is read. When it is low, the ACIA output drivers are turned off and the MPU writes into a selected register. Therefore, the Read/Write signal is used to select read-only or write-only registers within the ACIA.

Chip Select (CS0, CS1, $\overline{CS2}$) — These three high-impedance TTL-compatible input lines are used to address the ACIA. The ACIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Transfers of data to and from the ACIA are then performed under the control of the Enable Signal, Read/Write, and Register Select.

Register Select (RS) — The Register Select line is a high-impedance input that is TTL compatible. A high level is used to select the Transmit/Receive Data Registers and a low level the Control/Status Registers. The Read/Write signal line is used in conjunction with Register Select to select the read-only or write-only register in each register pair.

Interrupt Request ($\overline{IRQ}$) — Interrupt Request is a TTL-compatible, open-drain (no internal pullup), active low output that is used to interrupt the MPU. The $\overline{IRQ}$ output remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set. The $\overline{IRQ}$ status bit, when high, indicates the $\overline{IRQ}$ output is in the active state.

Interrupts result from conditions in both the transmitter and receiver sections of the ACIA. The transmitter section causes an interrupt when the Transmitter Interrupt Enabled condition is selected (CR5•$\overline{CR6}$), and the Transmit Data Register Empty (TDRE) status bit is high. The TDRE status bit indicates the current status of the Transmitter Data Register except when inhibited by Clear-to-Send ($\overline{CTS}$) being high or the ACIA being maintained in the Reset condition. The interrupt is cleared by writing data into the Transmit Data Register. The interrupt is masked by disabling the Transmitter Interrupt via CR5 or CR6 or by the loss of $\overline{CTS}$ which inhibits the TDRE status bit. The Receiver section causes an interrupt when the Receiver Interrupt Enable is set and the Receive Data Register Full (RDRF) status bit is high, an Overrun has occurred, or Data Carrier Detect ($\overline{DCD}$) has gone high. An interrupt resulting from the RDRF status bit can be cleared by reading data or resetting the ACIA. Interrupts caused by Overrun or loss of $\overline{DCD}$ are cleared by reading the status register after the error condition has occurred and then reading the Receive Data Register or resetting the ACIA. The receiver interrupt is masked by resetting the Receiver Interrupt Enable.

CLOCK INPUTS

Separate high-impedance TTL-compatible inputs are provided for clocking of transmitted and received data. Clock frequencies of 1, 16, or 64 times the data rate may be selected.

Transmit Clock (Tx CLK) — The Transmit Clock input is used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock.

Receive Clock (Rx CLK) — The Receive Clock input is used for synchronization of received data. (In the ÷1 mode, the clock and data must be synchronized externally.) The receiver samples the data on the positive transition of the clock.

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SERIAL INPUT/OUTPUT LINES

Receive Data (Rx Data) – The Receive Data line is a high-impedance TTL-compatible input through which data is received in a serial format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used.

Transmit Data (Tx Data) – The Transmit Data output line transfers serial data to a modem or other peripheral.

PERIPHERAL/MODEM CONTROL

The ACIA includes several functions that permit limited control of a peripheral or modem. The functions included are Clear-to-Send, Request-to-Send and Data Carrier Detect.

Clear-to-Send ($\overline{CTS}$) – This high-impedance TTL-compatible input provides automatic control of the transmitting end of a communications link via the modem Clear-to-Send active low output by inhibiting the Transmit Data Register Empty (TDRE) status bit.

Request-to-Send ($\overline{RTS}$) – The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The RTS output corresponds to the state of the Control Register bits CR5 and CR6. When CR6 = 0 or both CR5 and CR6 = 1, the $\overline{RTS}$ output is low (the active state). This output can also be used for Data Terminal Ready (DTR).

Data Carrier Detect ($\overline{DCD}$) – This high-impedance TTL-compatible input provides automatic control, such as in the receiving end of a communications link by means of a modem Data Carrier Detect output. The $\overline{DCD}$ input inhibits and initializes the receiver section of the ACIA when high. A low-to-high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the Receive Interrupt Enable bit is set. The Rx CLK must be running for proper $\overline{DCD}$ operation.

ACIA REGISTERS

The expanded block diagram for the ACIA indicates the internal registers on the chip that are used for the status, control, receiving, and transmitting of data. The content of each of the registers is summarized in Table 1.

TRANSMIT DATA REGISTER (TDR)

Data is written in the Transmit Data Register during the negative transition of the enable (E) when the ACIA has been addressed with RS high and R/$\overline{W}$ low. Writing data into the register causes the Transmit Data Register Empty bit in the Status Register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within 1-bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

RECEIVE DATA REGISTER (RDR)

Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receive Data Register Full bit (RDRF) in the status buffer to go high (full). Data may then be read through the bus by addressing the ACIA and selecting the Receive Data Register with RS and R/$\overline{W}$ high when the ACIA is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receive Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

TABLE 1 – DEFINITION OF ACIA REGISTER CONTENTS

Data Bus Line Number	Buffer Address			
	RS • $\overline{R/W}$ Transmit Data Register (Write Only)	RS • R/$\overline{W}$ Receive Data Register (Read Only)	$\overline{RS}$ • $\overline{R/W}$ Control Register (Write Only)	$\overline{RS}$ • R/$\overline{W}$ Status Register (Read Only)
0	Data Bit 0*	Data Bit 0	Counter Divide Select 1 (CR0)	Receive Data Register Full (RDRF)
1	Data Bit 1	Data Bit 1	Counter Divide Select 2 (CR1)	Transmit Data Register Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Select 1 (CR2)	Data Carrier Detect ($\overline{DCD}$)
3	Data Bit 3	Data Bit 3	Word Select 2 (CR3)	Clear to Send ($\overline{CTS}$)
4	Data Bit 4	Data Bit 4	Word Select 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Transmit Control 1 (CR5)	Receiver Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Transmit Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7***	Data Bit 7**	Receive Interrupt Enable (CR7)	Interrupt Request ($\overline{IRQ}$)

* Leading bit = LSB = Bit 0
** Data bit will be zero in 7 bit plus parity modes.
*** Data bit is "don't care" in 7 bit plus parity modes.

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CONTROL REGISTER

The ACIA Control Register consists of eight bits of write-only buffer that are selected when RS and R/$\overline{W}$ are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send peripheral/modem control output.

Counter Divide Select Bits (CR0 and CR1) – The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the ACIA. Additionally, these bits are used to provide a master reset for the ACIA which clears the Status Register (except for external conditions on $\overline{CTS}$ and $\overline{DCD}$) and initializes both the receiver and transmitter. Master reset does not affect other Control Register bits. Note that after power-on or a power fail/restart, these bits must be set high to reset the ACIA. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	÷1
0	1	÷16
1	0	÷64
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4) – The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows:

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bits
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6) – Two Transmitter Control bits provide for the control of the interrupt from the Transmit Data Register Empty condition, the Request-to-Send ($\overline{RTS}$) output, and the transmission of a Break level (space). The following encoding format is used:

CR6	CR5	Function
0	0	$\overline{RTS}$ = low, Transmitting Interrupt Disabled.
0	1	$\overline{RTS}$ = low, Transmitting Interrupt Enabled.
1	0	$\overline{RTS}$ = high, Transmitting Interrupt Disabled.
1	1	$\overline{RTS}$ = low, Transmits a Break level on the Transmit Data Output. Transmitting Interrupt Disabled.

Receive Interrupt Enable Bit (CR7) – The following interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7): Receive Data Register Full, Overrun, or a low-to-high transition on the Data Carrier Detect ($\overline{DCD}$) signal line.

STATUS REGISTER

Information on the status of the ACIA is available to the MPU by reading the ACIA Status Register. This read-only register is selected when RS is low and R/$\overline{W}$ is high. Information stored in this register indicates the status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the ACIA.

Receive Data Register Full (RDRF), Bit 0 – Receive Data Register Full indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after an MPU read of the Receive Data Register or by a master reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE), Bit 1 – The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Data Carrier Detect ($\overline{DCD}$), Bit 2 – The Data Carrier Detect bit will be high when the $\overline{DCD}$ input from a modem has gone high to indicate that a carrier is not present. This bit going high causes an Interrupt Request to be generated when the Receive Interrupt Enable is set. It remains high after the $\overline{DCD}$ input is returned low until cleared by first reading the Status Register and then the Data Register or until a master reset occurs. If the $\overline{DCD}$ input remains high after read status and read data or master reset has occurred, the interrupt is cleared, the $\overline{DCD}$ status bit remains high and will follow the $\overline{DCD}$ input.

Clear-to-Send ($\overline{CTS}$), Bit 3 – The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low $\overline{CTS}$ indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master reset does not affect the Clear-to-Send status bit.

Framing Error (FE), Bit 4 – Framing error indicates that the received character is improperly framed by a start and a stop bit and is detected by the absence of the first stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receive data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN), Bit 5 – Overrun is an error flag that indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receive Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has

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been read. The RDRF bit remains set until the Overrun is reset. Character synchronization is maintained during the Overrun condition. The Overrun indication is reset after the reading of data from the Receive Data Register or by a Master Reset.

Parity Error (PE), Bit 6 – The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver partiy check results are inhibited.

Interrupt Request ($\overline{IRQ}$), Bit 7 – The $\overline{IRQ}$ bit indicates the state of the $\overline{IRQ}$ output. Any interrupt condition with its applicable enable will be indicated in this status bit. Anytime the $\overline{IRQ}$ output is low the $\overline{IRQ}$ bit will be high to indicate the interrupt or service request status. $\overline{IRQ}$ is cleared by a read operation to the Receive Data Register or a write operation to the Transmit Data Register.

ORDERING INFORMATION

Package Type	Frequency (MHz)	Temperature	Order Number
Ceramic	1.0	0°C to 70°C	MC6850L
L Suffix	1.0	−40°C to 85°C	MC6850CL
	1.5	0°C to 70°C	MC68A50L
	1.5	−40°C to 85°C	MC68A50CL
	2.0	0°C to 70°C	MC68B50C
Cerdip	1.0	0°C to 70°C	MC6850S
S Suffix	1.0	−40°C to 85°C	MC6850CS
	1.5	0°C to 70°C	MC68A50S
	1.5	−40°C to 85°C	MC68A50CS
	2.0	0°C to 70°C	MC68B50S
Plastic	1.0	0°C to 70°C	MC6850P
P Suffix	1.0	−40°C to 85°C	MC6850CP
	1.5	0°C to 70°C	MC68A50P
	1.5	−40°C to 85°C	MC68A50CP
	2.0	0°C to 70°C	MC68B50P

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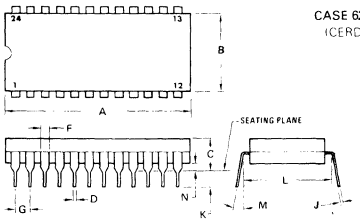
MC6850

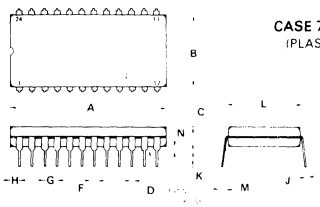
PACKAGE DIMENSIONS



CASE 623-03
(CERDIP)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.29	4.06	0.090	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

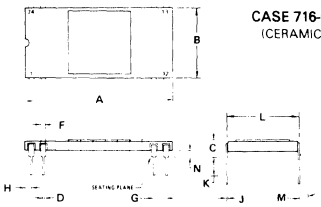
NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)



CASE 709-02
(PLASTIC)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D) SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.



CASE 716-06
(CERAMIC)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	27.64	30.99	1.088	1.220
B	14.73	15.34	0.580	0.604
C	2.67	4.32	0.105	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.57	0.100	0.180
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	1.02	1.52	0.040	0.060

NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

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MC6821

PERIPHERAL INTERFACE ADAPTER (PIA)

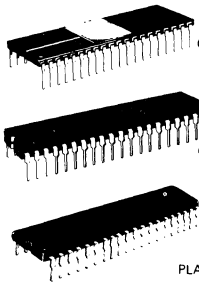
The MC6821 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the M6800 family of microprocessors. This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines; Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance Three-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Drive Capability on Side A Peripheral Lines
- Two TTL Drive Capability on All A and B Side Buffers
- TTL-Compatible
- Static Operation

MOS
(N-CHANNEL, SILICON-GATE, DEPLETION LOAD)

PERIPHERAL INTERFACE ADAPTER

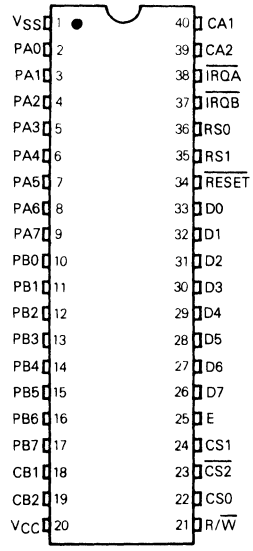


L SUFFIX
CERAMIC PACKAGE
CASE 715

S SUFFIX
CERDIP PACKAGE
CASE 734

P SUFFIX
PLASTIC PACKAGE
CASE 711

PIN ASSIGNMENT



ORDERING INFORMATION

Package Type	Frequency (MHz)	Temperature	Order Number
Ceramic L Suffix	1.0	0°C to 70°C	MC6821L
	1.0	−40°C to 85°C	MC6821CL
	1.5	0°C to 70°C	MC68A21L
	1.5	−40°C to 85°C	MC68A21CL
	2.0	0°C to 70°C	MC68B21L
Cerdip S Suffix	1.0	0°C to 70°C	MC6821S
	1.0	−40°C to 85°C	MC6821CS
	1.5	0°C to 70°C	MC68A21S
	1.5	−40°C to 85°C	MC68A21CS
	2.0	0°C to 70°C	MC68B21S
Plastic P Suffix	1.0	0°C to 70°C	MC6821P
	1.0	−40°C to 85°C	MC6821CP
	1.5	0°C to 70°C	MC68A21P
	1.5	−40°C to 85°C	MC68A21CP
	2.0	0°C to 70°C	MC68B21P

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MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range MC6821, MC68A21, MC68B21 MC6821C, MC68A21C	T_A	T_L to T_H 0 to 70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Ceramic Plastic Cerdip	θ_{JA}	 50 100 60	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, $T_A = T_L$ to T_H unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
BUS CONTROL INPUTS (R/$\overline{W}$, Enable, $\overline{RESET}$, RS0, RS1, CS0, CS1, CS2)					
Input High Voltage	V_{IH}	V_{SS}+2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}−0.3	–	V_{SS}+0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V)	I_{in}	–	1.0	2.5	μA
Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{in}	–	–	7.5	pF
INTERRUPT OUTPUTS ($\overline{IRQA}$, $\overline{IRQB}$)					
Output Low Voltage (I_{Load} = 1.6 mA)	V_{OL}	–	–	V_{SS}+0.4	V
Hi-Z Output Leakage Current	I_{OZ}	–	1.0	10	μA
Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{out}	–	–	5.0	pF
DATA BUS (D0-D7)					
Input High Voltage	V_{IH}	V_{SS}+2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}−0.3	–	V_{SS}+0.8	V
Hi-Z Input Leakage Current (V_{in} = 0.4 to 2.4 V)	I_{IZ}	–	2.0	10	μA
Output High Voltage (I_{Load} = −205 μA)	V_{OH}	V_{SS}+2.4	–	–	V
Output Low Voltage (I_{Load} = 1.6 mA)	V_{OL}	–	–	V_{SS}+0.4	V
Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{in}	–	–	12.5	pF

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DC ELECTRICAL CHARACTERISTICS (Continued)

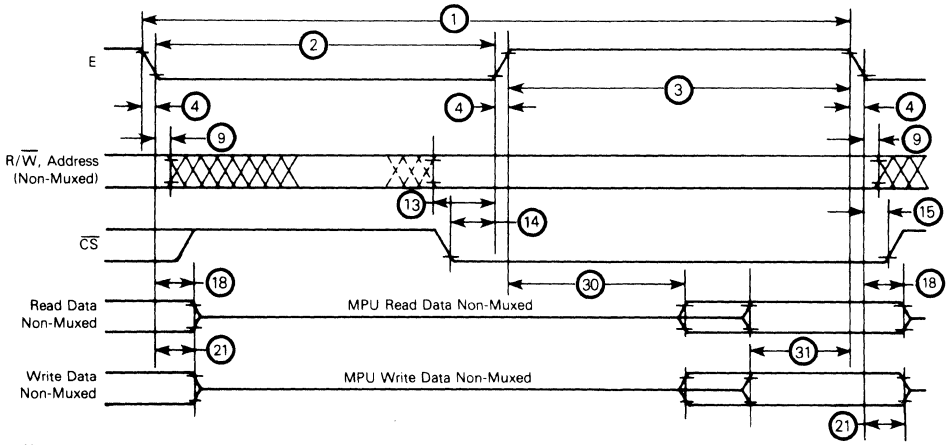
Characteristic		Symbol	Min	Typ	Max	Unit
PERIPHERAL BUS (PA0-PA7, PB0-PB7, CA1, CA2, CB1, CB2)						
Input Leakage Current (V_{in} = 0 to 5.25 V)	R/$\overline{W}$, $\overline{RESET}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1, Enable	I_{in}	–	1.0	2.5	μA
Hi-Z Input Leakage Current (V_{in} = 0.4 to 2.4 V)	PB0-PB7, CB2	I_{IZ}	–	2.0	10	μA
Input High Current (V_{IH} = 2.4 V)	PA0-PA7, CA2	I_{IH}	– 200	– 400	–	μA
Darlington Drive Current (V_O = 1.5 V)	PB0-PB7, CB2	I_{OH}	– 1.0	–	– 10	mA
Input Low Current (V_{IL} = 0.4 V)	PA0-PA7, CA2	I_{IL}	–	– 1.3	– 2.4	mA
Output High Voltage (I_{Load} = – 200 μA)	PA0-PA7, PB0-PB7, CA2, CB2	V_{OH}	V_{SS} + 2.4	–	–	V
(I_{Load} = – 10 μA)	PA0-PA7, CA2		V_{CC} – 1.0	–	–	
Output Low Voltage (I_{Load} = 3.2 mA)		V_{OL}	–	–	V_{SS} + 0.4	V
Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)		C_{in}	–	–	10	pF
POWER REQUIREMENTS						
Internal Power Dissipation (Measured at T_L = 0°C)		P_{INT}	–	–	550	mW

BUS TIMING CHARACTERISTICS (See Notes 1 and 2)

Ident. Number	Characteristic	Symbol	MC6821		MC68A21		MC68B21		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1.0	10	0.67	10	0.5	10	μs
2	Pulse Width, E Low	PW_{EL}	430	–	280	–	210	–	ns
3	Pulse Width, E High	PW_{EH}	450	–	280	–	220	–	ns
4	Clock Rise and Fall Time	t_r, t_f	–	25	–	25	–	20	ns
9	Address Hold Time	t_{AH}	10	–	10	–	10	–	ns
13	Address Setup Time Before E	t_{AS}	80	–	60	–	40	–	ns
14	Chip Select Setup Time Before E	t_{CS}	80	–	60	–	40	–	ns
15	Chip Select Hold Time	t_{CH}	10	–	10	–	10	–	ns
18	Read Data Hold Time	t_{DHR}	20	50*	20	50*	20	50*	ns
21	Write Data Hold Time	t_{DHW}	10	–	10	–	10	–	ns
30	Output Data Delay Time	t_{DDR}	–	290	–	180	–	150	ns
31	Input Data Setup Time	t_{DSW}	165	–	80	–	60	–	ns

*The data bus output buffers are no longer sourcing or sinking current by t_{DHR}max (High Impedance).

FIGURE 1 — BUS TIMING



Notes:
1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

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PERIPHERAL TIMING CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0 V, $T_A = T_L$ to T_H unless otherwise specified)

Characteristic	Symbol	MC6821		MC68A21		MC68B21		Unit	Reference Fig. No.
		Min	Max	Min	Max	Min	Max		
Data Setup Time	t_{PDS}	200	–	135	–	100	–	ns	6
Data Hold Time	t_{PDH}	0	–	0	–	0	–	ns	6
Delay Time, Enable Negative Transition to CA2 Negative Transition	t_{CA2}	–	1.0	–	0.670	–	0.500	µs	3, 7, 8
Delay Time, Enable Negative Transition to CA2 Positive Transition	T_{RS1}	–	1.0	–	0.670	–	0.500	µs	3, 7
Rise and Fall Times for CA1 and CA2 Input Signals	t_r, t_f	–	1.0	–	1.0	–	1.0	µs	8
Delay Time from CA1 Active Transition to CA2 Positive Transition	t_{RS2}	–	2.0	–	1.35	–	1.0	µs	3, 8
Delay Time, Enable Negative Transition to Data Valid	t_{PDW}	–	1.0	–	0.670	–	0.5	µs	3, 9, 10
Delay Time, Enable Negative Transition to CMOS Data Valid PA0-PA7, CA2	t_{CMOS}	–	2.0	–	1.35	–	1.0	µs	4, 9
Delay Time, Enable Positive Transition to CB2 Negative Transition	t_{CB2}	–	1.0	–	0.670	–	0.5	µs	3, 11, 12
Delay Time, Data Valid to CB2 Negative Transition	t_{DC}	20	–	20	–	20	–	ns	3, 10
Delay Time, Enable Positive Transition to CB2 Positive Transition	t_{RS1}	–	1.0	–	0.670	–	0.5	µs	3, 11
Control Output Pulse Width, CA2/CB2	PW_{CT}	500	–	375	–	250	–	ns	3, 11
Rise and Fall Time for CB1 and CB2 Input Signals	t_r, t_f	–	1.0	–	1.0	–	1.0	µ	12
Delay Time, CB1 Active Transition to CB2 Positive Transition	t_{RS2}	–	2.0	–	1.35	–	1.0	µs	3, 12
Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$	t_{IR}	–	1.60	–	1.10	–	0.85	µs	5, 14
Interrupt Response Time	t_{RS3}	–	1.0	–	1.0	–	1.0	µs	5, 13
Interrupt Input Pulse Time	PW_I	500	–	500	–	500	–	ns	13
$\overline{RESET}$ Low Time*	t_{RL}	1.0	–	0.66	–	0.5	–	µs	15

*The $\overline{RESET}$ line must be high a minimum of 1.0 µs before addressing the PIA.

FIGURE 2 – BUS TIMING TEST LOADS

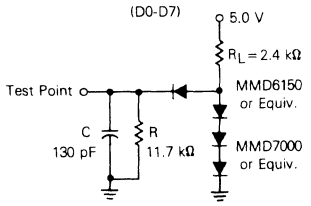

FIGURE 3 – TTL EQUIVALENT TEST LOAD

(PA0–PA7, PB0–PB7, CA2, CB2)

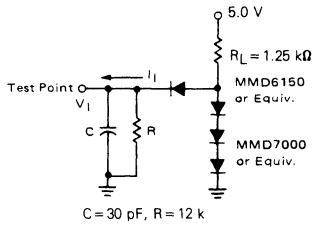

FIGURE 4 – CMOS EQUIVALENT TEST LOAD

(PA0-PA7, CA2)

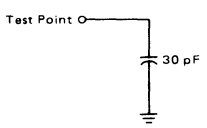

FIGURE 5 – NMOS EQUIVALENT TEST LOAD

($\overline{IRQ}$ Only)

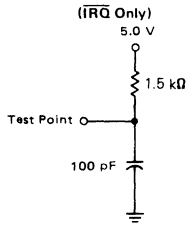

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FIGURE 6 — PERIPHERAL DATA SETUP AND HOLD TIMES
(Read Mode)

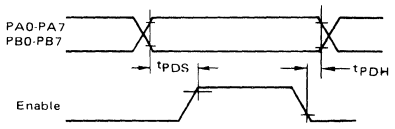
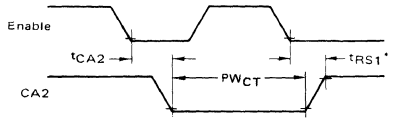


FIGURE 7 — CA2 DELAY TIME
(Read Mode; CRA-5 = CRA3 = 1, CRA-4 = 0)



*Assumes part was deselected during the previous E pulse.

FIGURE 8 — CA2 DELAY TIME
(Read Mode; CRA-5 = 1, CRA-3 = CRA-4 = 0)

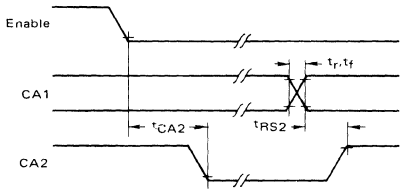


FIGURE 9 — PERIPHERAL CMOS DATA DELAY TIMES
(Write Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)

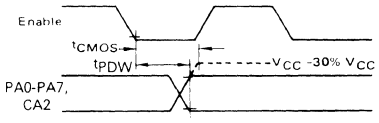
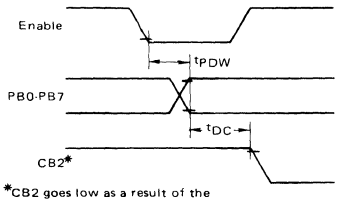
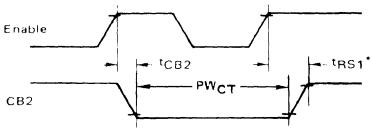


FIGURE 10 — PERIPHERAL DATA AND CB2 DELAY TIMES
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



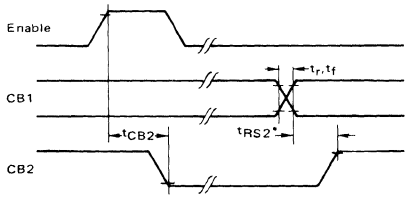
*CB2 goes low as a result of the positive transition of Enable.

FIGURE 11 — CB2 DELAY TIME
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



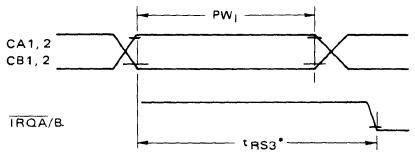
*Assumes part was deselected during the previous E pulse.

FIGURE 12 — CB2 DELAY TIME
(Write Mode; CRB-5 = 1, CRB-3 = CRB-4 = 0)



*Assumes part was deselected during any previous E pulse.

FIGURE 13 — INTERRUPT PULSE WIDTH AND $\overline{IRQ}$ RESPONSE



*Assumes Interrupt Enable Bits are set.

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

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FIGURE 14 – $\overline{IRQ}$ RELEASE TIME

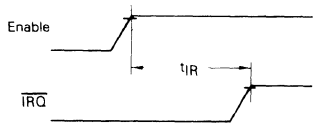
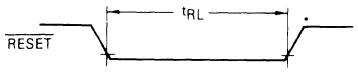


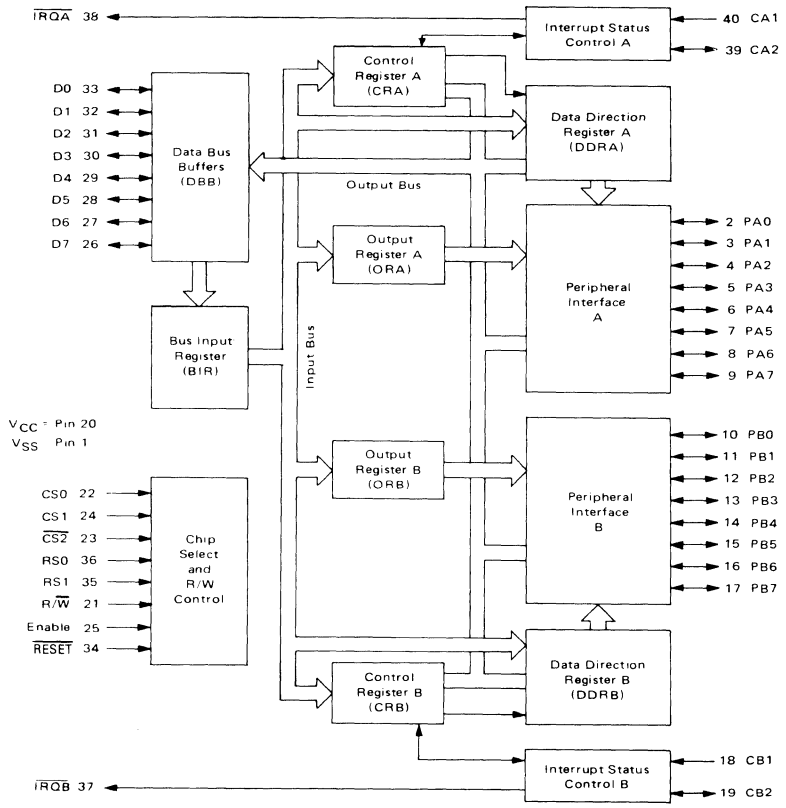
FIGURE 15 – $\overline{RESET}$ LOW TIME



*The $\overline{RESET}$ line must be a V_{IH} for a minimum of 1.0 μs before addressing the PIA.

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 16 – EXPANDED BLOCK DIAGRAM



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PIA INTERFACE SIGNALS FOR MPU

The PIA interfaces to the M6800 bus with an 8-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, a read/write line, an enable line and a reset line. To ensure proper operation with the MC6800, MC6802, or MC6808 microprocessors, VMA should be used as an active part of the address decoding.

Bidirectional Data (D0-D7) – The bidirectional data lines (D0-D7) allow the transfer of data between the MPU and the PIA. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs a PIA read operation. The read/write line is in the read (high) state when the PIA is selected for a read operation.

Enable (E) – The enable pulse, E, is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse.

Read/Write (R/$\overline{W}$) – This signal is generated by the MPU to control the direction of data transfers on the data bus. A low state on the PIA read/write line enables the input buffers and data is transferred from the MPU to the PIA on the E signal if the device has been selected. A high on the read/write line sets up the PIA for a transfer of data to the bus. The PIA output buffers are enabled when the proper address and the enable pulse E are present.

$\overline{RESET}$ – The active low $\overline{RESET}$ line is used to reset all register bits in the PIA to a logical zero (low). This line can be used as a power-on reset and as a master reset during system operation.

Chip Selects (CS0, CS1, and $\overline{CS2}$) – These three input signals are used to select the PIA. CS0 and CS1 must be high and $\overline{CS2}$ must be low for selection of the device. Data transfers are then performed under the control of the enable and read/write signals. The chip select lines must be stable for the duration of the E pulse. The device is deselected when any of the chip selects are in the inactive state.

Register Selects (RS0 and RS1) – The two register select lines are used to select the various registers inside the PIA. These two lines are used in conjunction with internal Control Registers to select a particular register that is to be written or read.

The register and chip select lines should be stable for the duration of the E pulse while in the read or write cycle.

Interrupt Request ($\overline{IRQA}$ and $\overline{IRQB}$) – The active low Interrupt Request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are "open drain" (no load device on the chip). This permits all interrupt request lines to be tied together in a wire-OR configuration.

Each Interrupt Request line has two internal interrupt flag bits that can cause the Interrupt Request line to go low. Each flag bit is associated with a particular peripheral interrupt line. Also, four interrupt enable bits are provided in the PIA which may be used to inhibit a particular interrupt from a peripheral device.

Servicing an interrupt by the MPU may be accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set.

The interrupt flags are cleared (zeroed) as a result of an MPU Read Peripheral Data Operation of the corresponding data register. After being cleared, the interrupt flag bit cannot be enabled to be set until the PIA is deselected during an E pulse. The E pulse is used to condition the interrupt control lines (CA1, CA2, CB1, CB2). When these lines are used as interrupt inputs, at least one E pulse must occur from the inactive edge to the active edge of the interrupt input signal to condition the edge sense network. If the interrupt flag has been enabled and the edge sense circuit has been properly conditioned, the interrupt flag will be set on the next active transition of the interrupt input pin.

PIA PERIPHERAL INTERFACE LINES

The PIA provides two 8-bit bidirectional data buses and four interrupt/control lines for interfacing to peripheral devices.

Section A Peripheral Data (PA0-PA7) – Each of the peripheral data lines can be programmed to act as an input or output. This is accomplished by setting a "1" in the corresponding Data Direction Register bit for those lines which are to be outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral data line to act as an input. During an MPU Read Peripheral Data Operation, the data on peripheral lines programmed to act as inputs appears directly on the corresponding MPU Data Bus lines. In the input mode, the internal pullup resistor on these lines represents a maximum of 1.5 standard TTL loads.

The data in Output Register A will appear on the data lines that are programmed to be outputs. A logical "1" written into the register will cause a "high" on the corresponding data line while a "0" results in a "low." Data in Output Register A may be read by an MPU "Read Peripheral Data A" operation when the corresponding lines are programmed as outputs. This data will be read properly if the voltage on the peripheral data lines is greater than 2.0 volts for a logic "1" output and less than 0.8 volt for a logic "0" output. Loading the output lines such that the voltage on these lines does not reach full voltage causes the data transferred into the MPU on a Read operation to differ from that contained in the respective bit of Output Register A.

Section B Peripheral Data (PB0-PB7) – The peripheral data lines in the B Section of the PIA can be programmed to act as either inputs or outputs in a similar manner to PA0-PA7. They have three-state capability, allowing them to enter a high-impedance state when the peripheral data line is used as an input. In addition, data on the peripheral data lines

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PB0-PB7 will be read properly from those lines programmed as outputs even if the voltages are below 2.0 volts for a "high" or above 0.8 V for a "low". As outputs, these lines are compatible with standard TTL and may also be used as a source of at least 1 milliampere at 1.5 volts to directly drive the base of a transistor switch.

Interrupt Input (CA1 and CB1) – Peripheral input lines CA1 and CB1 are input only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.

Peripheral Control (CA2) – The peripheral control line CA2 can be programmed to act as an interrupt input or as a peripheral control output. As an output, this line is compatible with standard TTL; as an input the internal pullup resistor on this line represents 1.5 standard TTL loads. The function of this signal line is programmed with Control Register A.

Peripheral Control (CB2) – Peripheral Control line CB2 may also be programmed to act as an interrupt input or peripheral control output. As an input, this line has high input impedance and is compatible with standard TTL. As an output it is compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch. This line is programmed by Control Register B.,

INTERNAL CONTROLS

INITIALIZATION

A $\overline{\text{RESET}}$ has the effect of zeroing all PIA registers. This will set PA0-PA7, PB0-PB7, CA2 and CB2 as inputs, and all interrupts disabled. The PIA must be configured during the restart program which follows the reset.

There are six locations within the PIA accessible to the MPU data bus: two Peripheral Registers, two Data Direction Registers, and two Control Registers. Selection of these locations is controlled by the RS0 and RS1 inputs together with bit 2 in the Control Register, as shown in Table 1.

Details of possible configurations of the Data Direction and Control Register are as follows:

TABLE 1 – INTERNAL ADDRESSING

		Control Register Bit		
RS1	RS0	CRA-2	CRB-2	Location Selected
0	0	1	X	Peripheral Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't Care

PORT A-B HARDWARE CHARACTERISTICS

As shown in Figure 17, the MC6821 has a pair of I/O ports whose characteristics differ greatly. The A side is designed to drive CMOS logic to normal 30% to 70% levels, and incorporates an internal pullup device that remains connected even in the input mode. Because of this, the A side requires more drive current in the input mode than Port B. In contrast, the B side uses a normal three-state NMOS buffer which cannot pullup to CMOS levels without external resistors. The B side can drive extra loads such as Darlingtons without problem. When the PIA comes out of reset, the A port represents inputs with pullup resistors, whereas the B side (input mode also) will float high or low, depending upon the load connected to it.

Notice the differences between a Port A and Port B read operation when in the output mode. When reading Port A, the actual pin is read, whereas the B side read comes from an output latch, ahead of the actual pin.

CONTROL REGISTERS (CRA and CRB)

The two Control Registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines CA1, CA2, CB1, and CB2. In addition they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on control lines CA1, CA2, CB1, or CB2. The format of the control words is shown in Figure 18.

DATA DIRECTION ACCESS CONTROL BIT (CRA-2 and CRB-2)

Bit 2, in each Control Register (CRA and CRB), determines selection of either a Peripheral Output Register or the corresponding Data Direction E Register when the proper register select signals are applied to RS0 and RS1. A "1" in bit 2 allows access of the Peripheral Interface Register, while a "0" causes the Data Direction Register to be addressed.

Interrupt Flags (CRA-6, CRA-7, CRB-6, and CRB-7) – The four interrupt flag bits are set by active transitions of signals on the four Interrupt and Peripheral Control lines when those lines are programmed to be inputs. These bits cannot be set directly from the MPU Data Bus and are reset indirectly by a Read Peripheral Data Operation on the appropriate section.

Control of CA2 and CB2 Peripheral Control Lines (CRA-3, CRA-4, CRA-5, CRB-3, CRB-4, and CRB-5) – Bits 3, 4, and 5 of the two control registers are used to control the CA2 and CB2 Peripheral Control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA-5 (CRB-5) is low, CA2 (CB2) is an interrupt input line similar to CA1 (CB1). When CRA-5 (CRB-5) is high, CA2 (CB2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA2 and CB2 have slightly different loading characteristics.

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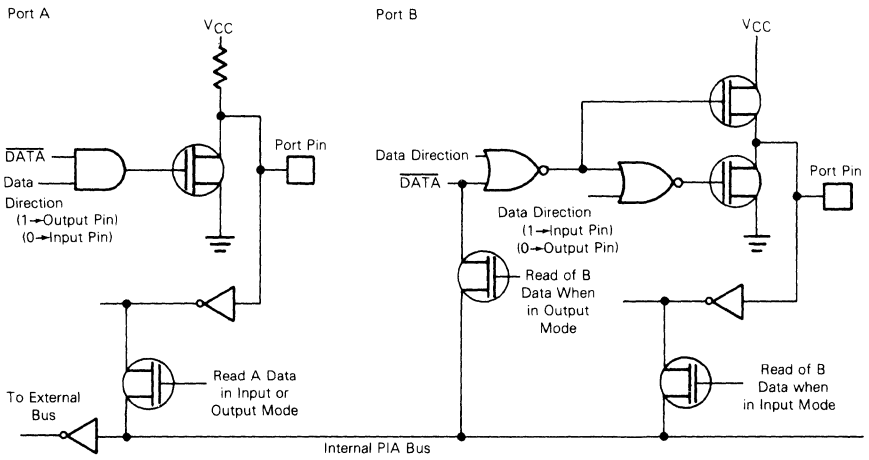
Control of CA1 and CB1 Interrupt Input Lines (CRA-0, CRB-0, CRA-1, and CRB-1) — The two lowest-order bits of the control registers are used to control the interrupt input lines CA1 and CB1. Bits CRA-0 and CRB-0 are used to enable the MPU interrupt signals $\overline{IRQA}$ and $\overline{IRQB}$, respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals CA1 and CB1.

FIGURE 17 — PORT A AND PORT B EQUIVALENT CIRCUITS



ORDERING INFORMATION

MC68A21CP

- Motorola Integrated Circuit
- M6800 Family
- Blanks = 1.0 MHz
- A = 1.5 MHz
- B = 2.0 MHz
- Device Designation In M6800 Family
- Temperature Range
  - Blank = 0° → +70°C
  - C = −40° → +85°C
- Package
  - P = Plastic
  - S = Cerdip
  - L = Ceramic

BETTER PROGRAM

Better program processing is available on all types listed. Add suffix letters to part number.

Level 1 add "S" Level 2 add "D" Level 3 add "DS"

Level 1 "S" = 10 Temp Cycles − (−25 to 150°C); Hi Temp testing at T_A max.
Level 2 "D" = 168 Hour Burn-in at 125°C
Level 3 "DS" = Combination of Level 1 and 2.

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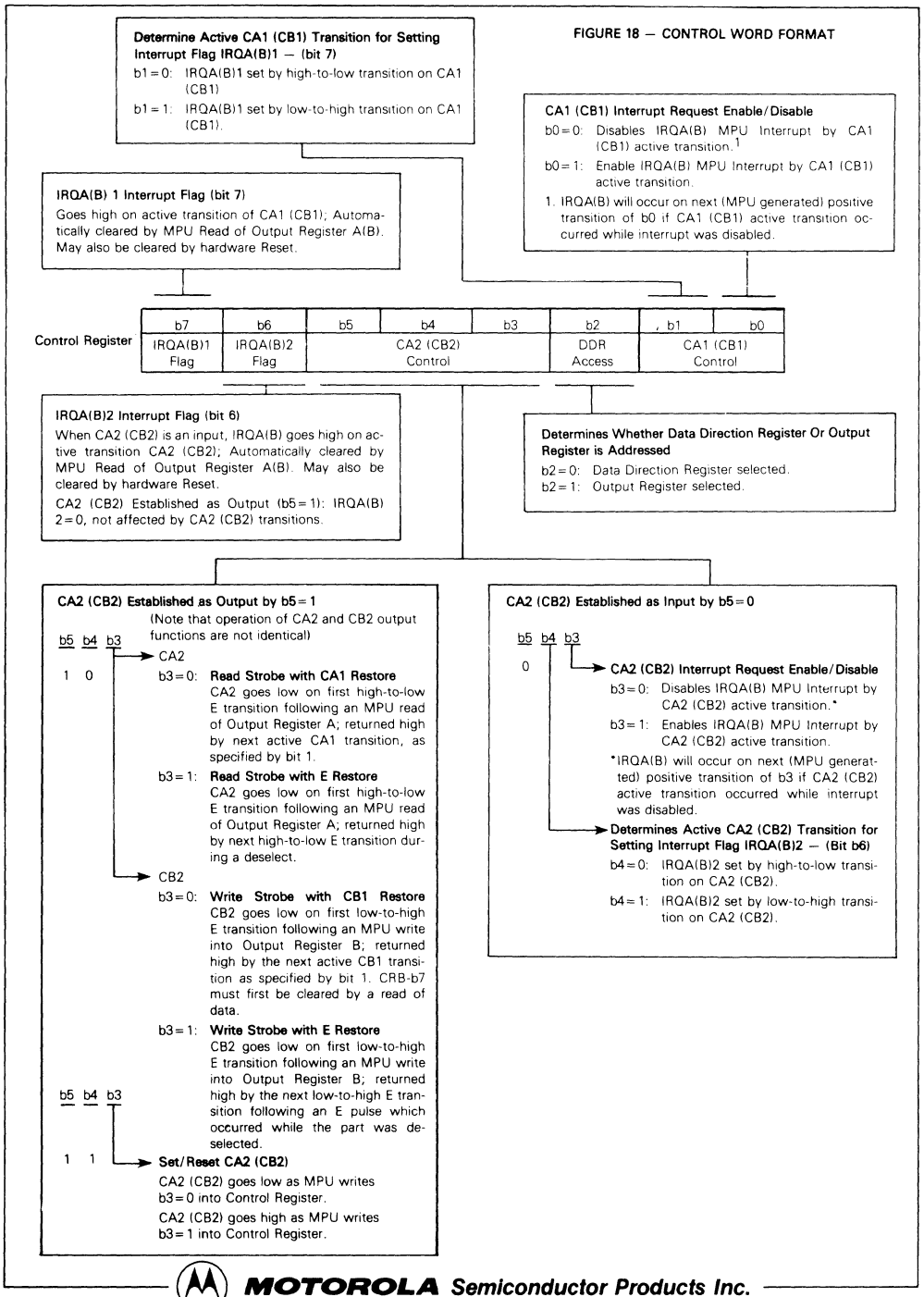
FIGURE 18 — CONTROL WORD FORMAT



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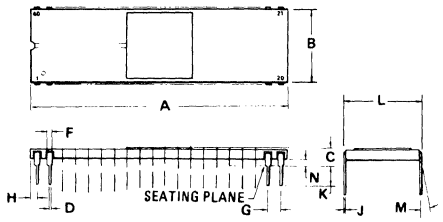
MC6821

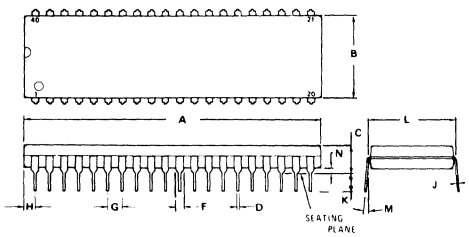
PACKAGE DIMENSIONS



L SUFFIX
CERAMIC PACKAGE
CASE 715-04

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.94	15.34	0.588	0.604
C	3.05	4.06	0.120	0.160
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	1.02	1.52	0.040	0.060

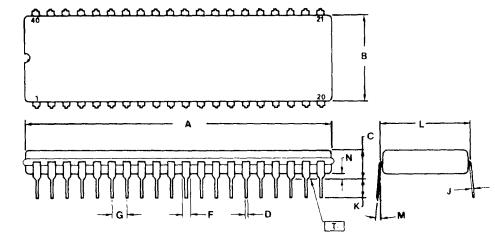
NOTES
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA (AT SEATING PLANE), AT MAX MAT'L CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.



P SUFFIX
PLASTIC PACKAGE
CASE 711-03

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.



S SUFFIX
CERDIP PACKAGE
CASE 734-03

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	51.31	53.24	2.020	2.096
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

NOTES
1. DIMENSION A IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS

3. T IS SEATING PLANE
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSION A AND B INCLUDES MENISCUS.

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MC6821

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Appendix A

Foreign Keyboards

United Kingdom

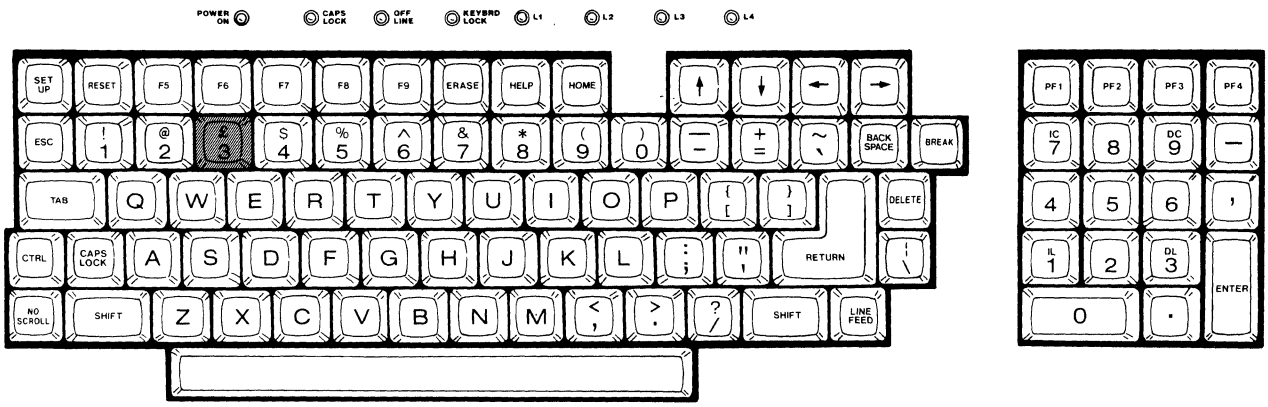

Figure A.1. United Kingdom (UK) Keyboard

NOTE: Shaded keys denote differences from USA Keyboard.

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Danish/Norwegian

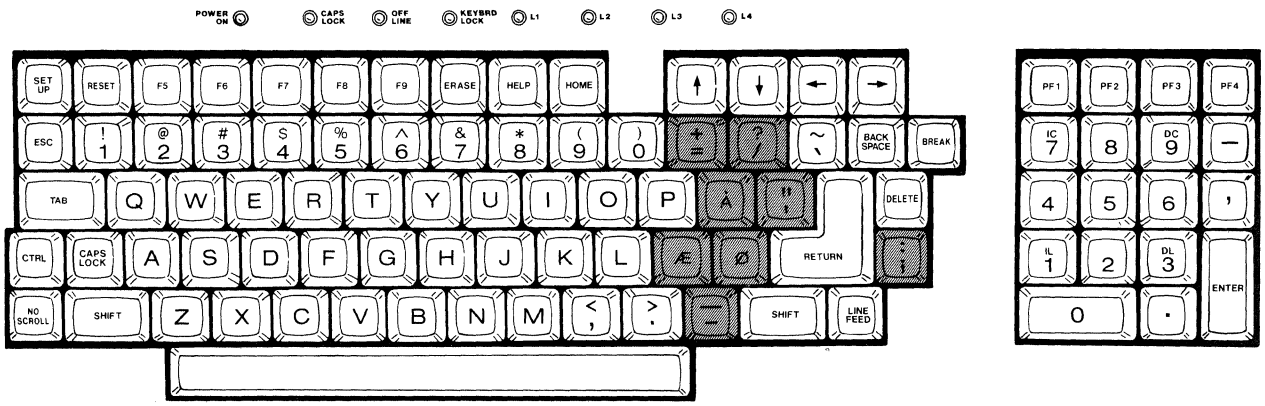

Figure A.2. Danish/Norwegian Keyboard

NOTE: Shaded keys denote differences from USA Keyboard.

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French

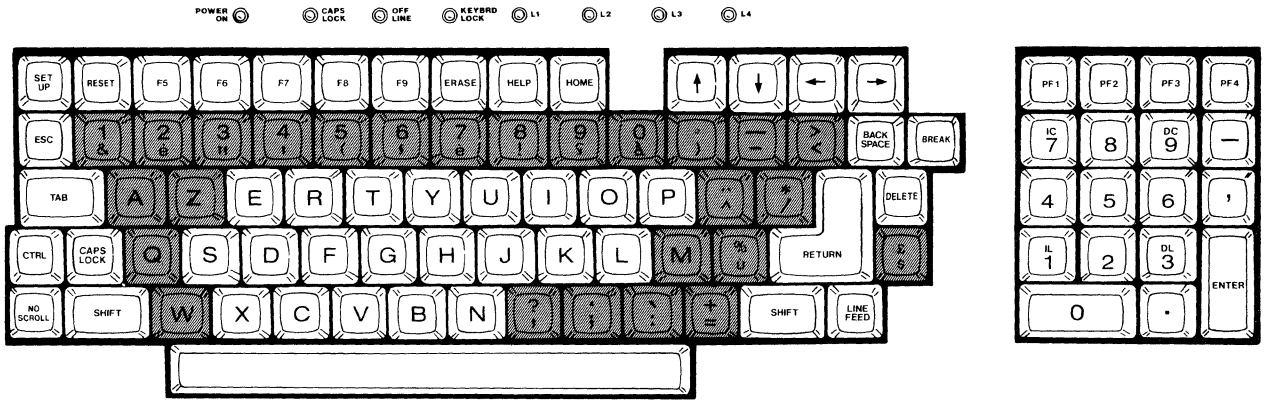

Figure A.3. French Keyboard

NOTE: Shaded keys denote differences from USA Keyboard.

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German

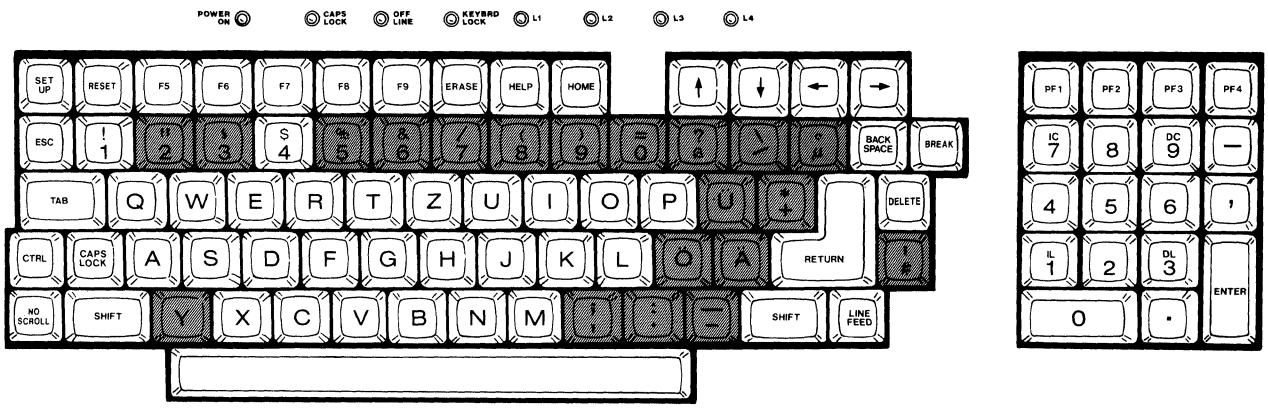

Figure A.4. German Keyboard

NOTE: Shaded keys denote differences from USA Keyboard.

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Italian

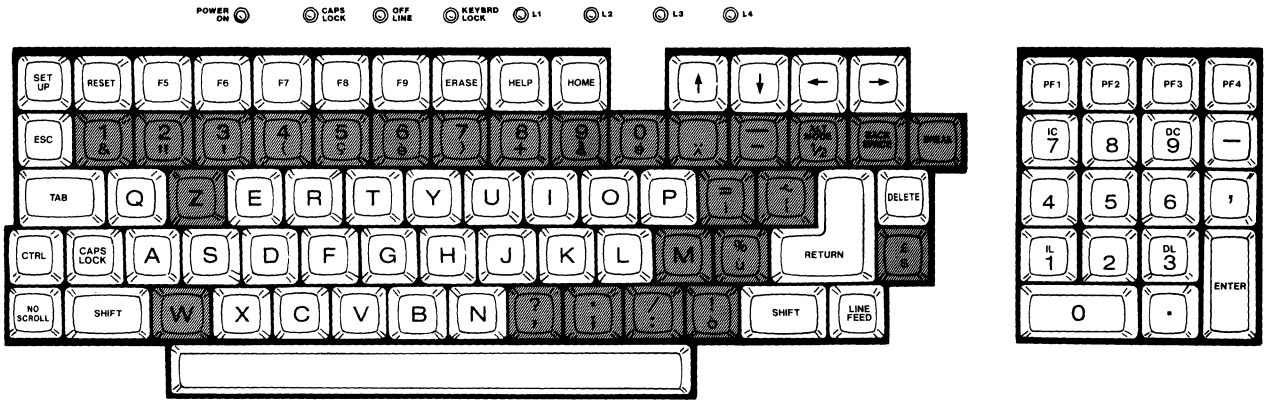

Figure A.5. Italian Keyboard

NOTE: Shaded keys denote differences from USA Keyboard.

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Spanish

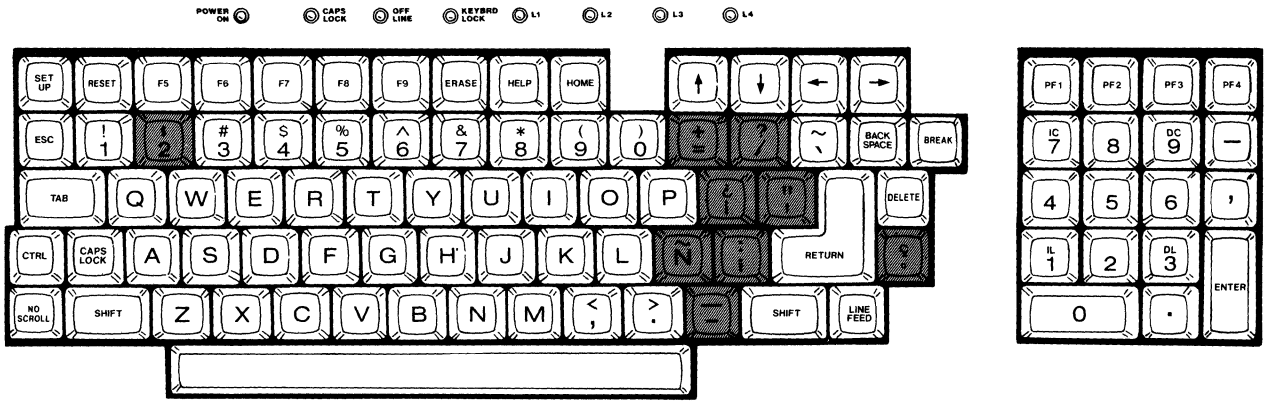

Figure A.6. Spanish Keyboard

NOTE: Shaded keys denote differences from USA Keyboard.

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Swedish

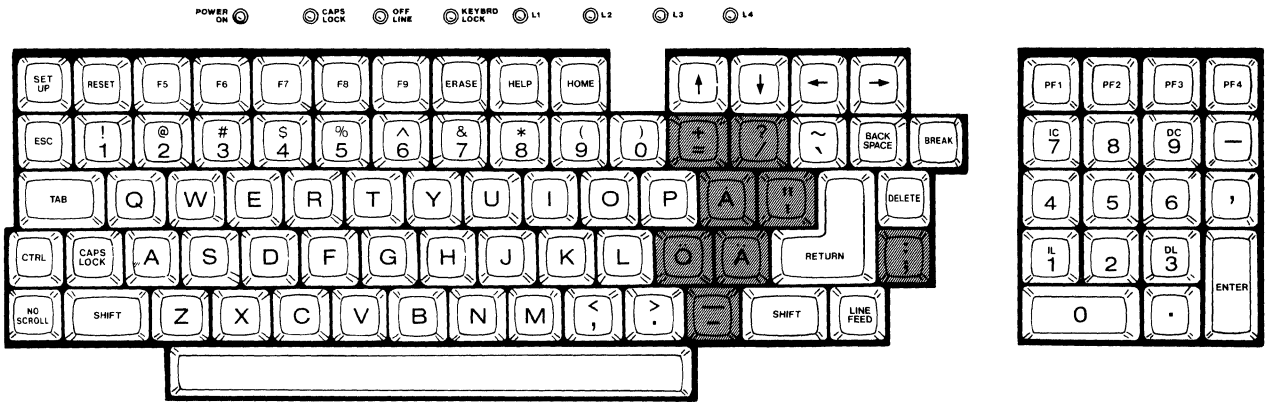

Figure A.7. Swedish Keyboard

NOTE: Shaded keys denote differences from USA Keyboard.

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Appendix B

Programming Information

Zenith

The terminal recognizes the following ASCII characters when operating in the Zenith mode.

DEC	OCT	HEX	CHR	CTRL CHR	FUNCTIONAL DESCRIPTION OR CHARACTER
7	007	7	BEL	G	Sounds bell tone.
8	010	8	BS	H	Back Space. Moves the cursor one position on the screen.
9	011	9	HT	I	Tab. Moves the cursor to the next tab stop.
10	012	A	LF	J	Line Feed. Advances the cursor to the next line. At the bottom of the screen, scrolls the text up one line.
11	013	B	VT	K	Vertical Tab (same as line feed).
12	014	C	FF	L	Form Feed (same as line feed).
13	015	D	CR	M	Carriage Return. Moves the cursor to the first character position in the current line. Nothing happens if the cursor is already at the first position.
17	021	11	XON	Q	Resume data transmission.
19	023	13	XOFF	S	Stops data transmission except codes XOFF and XON.
24	030	18	CAN	X	Cancel. Cancels the current escape sequence.
27	033	1B	ESC	[	Escape. Introduces a control sequence.

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Summary of Zenith Escape Sequences

A space has been included between the escape key (ESC) and the actual code for clarity. Do not include this space. The term "defined scrolling region" appears in the following listings and means lines 1-24 unless altered by the use of escape code sequences. An explanation for the codes is provided where necessary. The escape sequences are listed by function.

NOTES:

1. "Default" is the parameter assumed when no parameter, or a value of zero, is specified.
2. Pn – Numeric Parameter. Any decimal number that is substituted for Pn.
3. Bn – Alphanumeric Parameter. Any alphanumeric character selected from a list and used to select a subfunction.

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Cursor Functions

ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC H	ZCUH	Cursor home. The cursor to the first column, first line.
ESC A	ZCCU	Cursor up.
ESC B	ZCUD	Cursor down.
ESC C	ZCUF	Cursor forward (right).
ESC D	ZCUB	Cursor backward (left).
ESC I	ZRL	Reverse index. Moves the cursor to the same horizontal position on the preceding line. If the cursor is on the top line, the cursor will scroll down one line.
ESC n	ZCPR	Cursor position report. The terminal indicates the cursor position in the form ESC Y line# column# (ASCII character). Refer to direct cursor addressing for more information.
ESC j	ZSCP	Save cursor position.
ESC k	ZRCP	Return cursor to previously saved position.
ESC y	ZDCA	Direct cursor addressing. Moves the cursor to a position on the screen by entering the escape code, the ASCII character representing the line number, and the ASCII character representing the the column number. The first line and column number are both 32. Lines are numbered 1-25 top to bottom. Columns are numbered 1-80 (1-132) left to right. Add the line and column numbers to 31. Convert the numbers to the equivalent ASCII characters and enter in the following order: ESC Y line# (ASCII character) column# (ASCII character). The cursor will not move if the entered line number is too high. The cursor will move to the end of the line if the entered column number is too high. The 25th line must be enabled to move the cursor to the 25th line.
ESC –	ZCBT	Cursor backward tabulation-Moves cursor backwards to last tab set.
ESC .0	ZCTCP	Clear tab at cursor position.
ESC .3	ZCAT	Clear all tab positions.
ESC .8	ZSTCP	Set tabs at current cursor position.

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Editing and Erasing

ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC E	ZCD	Clear display.
ESC b	ZDB	Erase to beginning of display.
ESC J	ZEOP	Erase to end of display.
ESC l[1]	ZEL	Erase line.
ESC o	ZEBL	Erase to beginning of line.
ESC K	ZEOL	Erase to end of line.
ESC L	ZIL	Insert line. Inserts a new blank line by the line the cursor is on and all other lines, down one line.
ESC M	ZDL	Delete line. Deletes the line the cursor is on and moves all other lines up one line.
ESC N	ZDCH	Delete character. Deletes a character at the cursor position and shifts the text on the line, one character to the left.
ESC @	ZEIM	Enter character insert mode. Inserts characters or words into displayed text. As each new character is inserted the cursor is shifted to the right and the character at the end of the line is lost.
ESC O	ZERM	Exit insert character mode.

[1] Denotes lower case L.

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Configuration

ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC z	ZRAM	Reset to power up configuration.
ESC rBn	ZMBR	Modify baud rate. Bn = @ = 75 A = 110 B = 150 C = 300 D = 600 E = 1200 F = 1800 G = 2000 H = 2400 I = Not Used J = 4800 K = 7200 L = 9600 M = 19200 N = 50 O = 134.5 P = 200 Q = 1050 R = Not Used
ESC xPn	ZSM	Set mode(s). Pn = 1 = Enable 25th line 2 = Disable key click 3 = Enter hold screen mode 4 = Block cursor 5 = Cursor off 6 = Keypad shifted 7 = Enter alternate keypad mode 8 = Auto LF on CR 9 = Auto CR on LF
ESC yPn	ZRM	Reset mode(s). Pn = 1 = Disable 25th Line 2 = Enable key click 3 = Exit hold screen mode 4 = Underscore cursor 5 = Cursor on 6 = Keypad unshifted 7 = Exit alternate keypad mode 8 = No Auto LF on CR 9 = No Auto CR on LF

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Configuration (continued)

ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC <	ZEAM	Enter ANSI mode.
ESC 1	ZDWO	Double wide characters on. The cursor movement will follow as in the normal character operation. The double wide character can be turned on or off anywhere on the line. Thus a line can be mixed with both double wide and normal wide characters. If a double wide character is returned to normal, a space will be displayed following that character.

NOTE: If double high/double wide characters had been selected while in the ANSI mode and double wide characters are selected on the same line, the cursor will blank out.

ESC 2	ZDWF	Double wide characters off.

Modes of Operation

ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC [	ZEHS	Enter hold screen mode. Press the NO SCROLL key and a new line of information will be printed on the bottom line. Press the SHIFT and NO SCROLL keys and a new page of text will be displayed.
ESC [	ZXHS	Exit hold screen mode.
ESC p	ZERU	Enter reverse video mode. Displays dark characters on a light background.
ESC q	ZXRU	Exit reverse video mode.
ESC s <atr>	ZSA	Set attribute. The video attributes are: Alternate character font <132 character set>. Underline <undr>. Half intensity <half>. Blinking <blink>. Reverse video <rev>. The video attributes are set as follows: ESCs<alt><undr><half><blink><rev> Where <attributes> is the ASCII character formed when the ASCII value for 0 (30 hex, 48 decimal) is added to the binary value obtained from each bit position listed above. EXAMPLE: Underline and reverse video are desired. Binary = 01001 Decimal = 17 17+48=65 ASCII character for 65 = A Escape sequence would be ESCsA

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Modes of Operation (continued)

ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC ~	ZHLP	Help key.
ESC F	ZEGM	Enter Z-29 graphics mode.
ESC G	ZXGM	Exit Z-29 graphics mode.
ESC t	ZEKS	Entered keypad shifted mode. Inverts the normal and shifted functions of the keypad.
ESC u	ZXKS	Exit keypad shifted mode.
ESC =	ZAKM	Enter alternate keypad mode. Transmits the special escape codes used by software instead of normal characters.

KEY	ESCAPE CODE
0	ESC?p
1	ESC?q
2	ESC?r
3	ESC?s
4	ESC?t
5	ESC?u
6	ESC?v
7	ESC?w
8	ESC?x
9	ESC?y
–	ESC?m
.	ESC?n
,	ESC?l
ENTER	ESC?M

ESC >	ZEKS	Exit alternate keypad mode.

Additional Functions

ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC }	ZDK	Keyboard disabled.
ESC {	ZEK	Keyboard enabled.
ESC v	ZEWA	Wrap around at end of line.
ESC w	ZXWA	Discard at end of line.
ESC Z	ZID	Identify as VT52. Terminal responds to the interrogation with ESC/Z indicating performance as a DEC VT52.
ESC i0	ZRTT	Request terminal type. Terminal responds to the request with an ESC i B0.

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Print Functions

ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC ^	DAP	AUTO PRINT ON. Turns on auto print. A display line will be printed after moving the cursor off the line by using LF, CR, or vertical tab (also transmitted to the printer. The line also prints during an autowrap. Auto wrap lines end with a return. When double high/double wide lines are sent to the printer, they are converted to single wide lines. If double wide characters are sent to the printer, each character is followed by a space.
ESC –	DAPO	AUTO PRINT OFF. Turn media copy off.
ESC W	DPC	PRINTER CONTROLLER ON. Turns on printer controller (blind print). The printer transmits received characters to printer without displaying them. The terminal does not insert or delete spaces, provide line delimiters, or select the correct character set.
ESC X	DPCO	PRINTER CONTROLLER OFF.
ESC V	DPCL	PRINT CURSOR LINE. Prints line at cursor location. Keyboard locked indicator will be enabled. When double high/double wide lines are sent to the printer, they are converted to single wide lines. If double wide characters are sent to the printer, each character is followed by a space. A beep is sounded at the end of the printed line.
ESC]	DPS	PRINT SCREEN. Prints the full screen. Keyboard locked indicator will be enabled. When double high/double wide lines are sent to the printer, they are converted to single wide lines. If double wide characters are sent to the printer, each character is followed by a space. A beep sounds at the end of print screen.

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NOTE: The terminal transmits the following escape codes to perform a user-defined function. There is no response by the terminal.

TRANSMITTED CODE	MNEMONIC	KEY	**NOTE:** Z-29 keys
ESC P	ZF1	Function key (PF1)	(F6) Blue
ESC Q	ZF2	Function key (PF2)	(F7) Red
ESC R	ZF3	Function key (PF3)	(F8) Gray
ESC S	ZF4	Function key (PF4)	(F1)
ESC T	ZF5	Function key (F5)	(F2)
ESC U	ZF6	Function key (F6)	(F3)
ESC V	ZF7	Function key (F7)	(F4)
ESC W	ZF8	Function key (F8)	(F5)
ESC X	ZF9	Function key (F9)	(F9)

ANSI

The terminal recognizes the following ASCII characters when operating in the ANSI mode.

DEC	OCT	HEX	CHR	CTRL CHR	FUNCTIONAL DESCRIPTION OR CHARACTER
0	000	0	NUL	@ or SP	Used as fill character.
5	005	5	ENQ	E	Transmits answerback message.
7	007	7	BEL	G	Sounds bell tone.
8	010	8	BS	H	Back Space. Moves the cursor one position to the left except at left end of screen.
9	011	9	HT	I	Tab. Moves the cursor to the next tab stop.
10	012	A	LF	J	Line Feed. Advances the cursor to the next line. At the bottom of the screen, scrolls the text up one line.
11	013	B	VT	K	Same as Line Feed.
12	014	C	FF	L	Same as Line Feed.
13	015	D	CR	M	Carriage Return. Moves the cursor to the first character position in the current line. Nothing happens if the cursor is already at the first position.
14	016	E	SO	N	Selects the user-defined G1 character set by the select character set (SCS) sequence.
15	017		SI	O	Selects the user-defined G0 character set by the SCS sequence.
17	021	11	XON	Q	Resume data transmission.
19	023	13	XOFF	S	Stops data transmission except codes XOFF and XON.
24	030	18	CAN	X	Cancel. Cancels the current escape sequence.
26	032	1A	SUB	Z	Same as Cancel.
27	033	1B	ESC	[	Escape. Introduces a control sequence.
127	177	7F	DEL		Fill character.

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Summary of ANSI Escape Sequences

A space has been included between the escape key (ESC) and the actual code for clarity . Do not include this space. The term "defined scrolling region" appears in the following listings and means lines 1-24 unless altered by the use of escape code sequences. An explanation for the codes is provided where necessary. The escape sequences are listed by function.

NOTES:

1. "Default" is the parameter assumed when no parameter, or a value of zero is specified.
2. Pn – Numeric Parameter. Any decimal number that is substituted for Pn.
3. Ps – Selective Parameter. Any decimal number selected from a list and used to select a subfunction. Several subfunctions can be selected at once by putting one number after another and separating each number by a semicolon. A maximum of eight parameters may be selected.
4. Bn – Alphanumeric Parameter. Any alphanumeric character selected from a list and used to select a subfunction.
5. Sequences noted with a subscript "D" emulate the DEC model VT-100* terminal.

* DEC and VT100 are registered trademarks of Digital Equipment Co.

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Cursor Functions

ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC [H ESC [0;0H ESC [0;0f	CUP or	Cursor home. Moves cursor to the first line first column.
ESC [Pn;PnH	HVP	Direct cursor addressing. Moves the cursor to a position on the screen by entering the escape code, the ASCII character representing the line number, and the ASCII character representing the the column number. The first line and column number are both 32. Lines are numbered 1-25 top to bottom. Columns are numbered 1-80 (1-132) left to right. Add the line and column numbers to 31. Convert the numbers to the equivalent ASCII characters and enter in the following order: ESC[ASCII line character; ASCII column character H or ESC[ASCII line character; ASCII column character f Direct cursor addressing and the 25th line must be enabled to move the cursor to the 25th line. If the line number or column number is too high, the cursor will not move.
ESC[PnA	CUU	Cursor up. Moves the cursor up a number of lines determined by the value of Pn. A one or a zero moves the cursor up one line. The cursor stops at the top line of the scrolling region. The default value is zero.
ESC [PnB	CUD	Cursor down. Moves the cursor down a number of lines determined by the value of Pn. A zero or one moves the cursor down one line. The cursor will stop at the bottom line of the defined scrolling region. The default value is zero.
ESC [PnC	CUF	Cursor forward (right). Moves the cursor right the number of characters determined by the value of Pn. A zero or one moves the cursor one position. The cursor stops at the rightmost character position. The default value is zero.
ESC [PnD	CUB	Cursor backward (left). Moves the cursor left the number of characters determined by the value of Pn. A zero or one moves the cursor one position. The cursor stops at the leftmost position. The default value is zero.
ESC D	IND	Index. Moves the cursor down in the same manner as line feed.
ESC M	RI	Reverse index. Moves the cursor to the same horizontal position on the preceding line. If the cursor is on the top line of the defined scrolling region, the lines will move down, but the cursor will not move.

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Cursor Functions (continued)

ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC E	NLR	Cursor next line return.
ESC [6n	CPR	Cursor position report. The terminal indicates the cursor position in the form ESC[Pl; PcR where l = line and c = column. The positions are expressed in decimal. Refer to direct cursor addressing for more information.
ESC [s	PSCP	Save cursor position.
ESC [u	PRCP	Return cursor to previously saved position.
ESC 7	SVD	Save cursor position, attributes, and character set.
ESC 8	RSD	Return cursor to previously saved position, attributes, and character set.
ESC H	CHT	Cursor horizontal tab set. Sets horizontal tabs at cursor position.
ESC [PnZ	CBT	Cursor backward tabulation. Moves cursor backwards to previous tab set where Pn indicates the number of tabs back from cursor position.
ESC [Psg	CCT	Clear horizontal cursor tab stops. Ps = 0 = Clear horizontal tab at cursor. 3 = Clear all horizontal tab stops. The default value is the value saved in nonvolatile memory.

Screen Functions

ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC #3	DHT	Double height line (character top half).
ESC #4	DHB	Double height line (character bottom half).
ESC #5	SWL	Single width line.
ESC #6	DWL	Double width line.
ESC #8	ALN	Fill screen. Fills screen with E's for alignment.
ESC [?3h	NCH	132 characters per line. Selects 132 characters per line. When selected all screen data will be lost.
ESC [?3l[1]	NCL	80 characters per line. Selects 80 characters per line. When selected all screen data will be lost.
ESC [Pnv	SAR	Set blinking attributes. Pn = 0 = 1/64 of 50 or 60 Hz (field rates). 1 = 1/128 of 50 or 60 Hz (field rates). The default value is zero.

[1] Denotes a lower case L.

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Editing and Erasing

ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC [PnJ	ED	Erase display. Pn = 0 = Erase from cursor to end of page. 1 = Erase from cursor to beginning of display. 2 = Clear display. The default value is zero.
ESC [PnK	EL	Erase in line. Pn = 0 = Erase from cursor to end of line. 1 = Erase from cursor to start of line. 2 = Erase line. The default value is zero.
ESC [PnL	IL	Insert line. Inserts one or more blank lines depending on the value of Pn. The cursor is moved to the beginning of the new blank line.
ESC [PnM	DL	Delete line. Deletes one or more lines of characters depending on the value of Pn. The lines below the deleted area move up the number of deleted lines and the cursor is moved to the beginning of the next line.
ESC [Pn@	IC	Insert character. Inserts the number of characters depending on the value of Pn. Remaining characters move to the right.
ESC [PnP	DCH	Delete character. Deletes characters at the cursor position depending on the value of Pn. Remaining characters move to the left.
ESC [4h	IRM	Insert/Replacement mode on. Inserts characters or words into displayed text. As each new character is inserted the cursor and characters to the right are shifted to the right and the character at the end of the line is lost.
ESC [4l[1]	IRM	Insert/Replacement mode off.

[1] Denotes lower case L.

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Configuration

ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC c or ESC [z	PRAM	Reset to power up configuration.
ESC [Pnw	PMBR	Modify baud rate. Pn = 0 = 75 1 = 110 2 = 150 3 = 300 4 = 600 5 = 1200 6 = 1800 7 = 2000 8 = 2400 9 = Not Used 10 = 4800 11 = 7200 12 = 9600 13 = 19200 14 = 50 15 = 134.5 16 = 200 17 = 1050
ESC [>Pnh	SM	Set mode(s). Pn = 1 = Enable 25th line 2 = Disable key click 3 = Enter hold screen mode 4 = Block cursor 5 = Cursor off 6 = Keypad shifted 7 = Enter alternate keypad mode 8 = Auto LF on CR 9 = Auto CR on LF
ESC [>Pnl[1]	RM	Reset mode(s). Pn = 1 = Disable 25th line 2 = Enable key click 3 = Exit hold screen mode 4 = Underscore cursor 5 = Cursor on 6 = Keypad unshifted 7 = Exit alternate keypad mode 8 = No Auto LF on CR 9 = No Auto CR on LF
ESC [?2l[1]	PEZM	Enter Zenith mode.

[1] Denotes lower case L.

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ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC [20h	LNM	Enter new line mode.
ESC [20l[1]	LNM	Exit new line mode.
ESC [Pt;Pbr	SR	Define scrolling region. The scrolling region is equal to the values of Pt and Pb expressed in decimal numbers. Pt = Top of scrolling region. Pb = Bottom of scrolling region. Minimum size is two lines (top must be less than bottom).The cursor is placed in the HOME position.
ESC [?4h	SSC	Smooth scroll enable.
ESC [?4l[1]	JSC	Jump scroll enable.
ESC (Pn	SCS	Set character set G0. Character set G0 is set on terminal power up. To select G0 when in character set G1 type CTRL character for SI, and then the ESC sequence. Pn = A = United States (USACII) B = United Kingdom set C = Danish/Norwegian D = German E = Spanish F = Swedish G = Italian H = French 0 = VT-100 line graphics 1 = Undefined 2 = Z-29 block graphics 3 = Greek alphabet
ESC)Pn	SCS	Set character set G1. To select character set G1, type the CTRL character for SO and then the ESC sequence. Pn = A = United States (USACII) B = United Kingdom set C = Danish/Norwegian D = German E = Spanish F = Swedish G = Italian H = French 0 = VT-100 line graphics 1 = Undefined 2 = Z-29 block graphics 3 = Greek alphabet

[1] Denotes lower case L.

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ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC [c or ESC [0c	RDA	Report device attributes. VT100 responds ESC[?1;2c.
ESC [5n	DSR	Device status report. Response: ESC[0n = No malfunction. ESC[3n = Malfunction – Retry.

Modes of Operation

ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC [>3h	SM	Enter hold screen mode. Press the NO SCROLL key and a new line of information will be printed on the bottom line. Press the SHIFT and NO SCROLL keys and a new page of text will be displayed.
ESC [>3l[1]	RM	Exit hold screen mode.Pressing the CTRL and S keys generates a XOFF, pressing the S and NO SCROLL key generates a XON. Pressing the CTRL and Q keys generates a XON, pressing the NO SCROLL key generates a XOFF.
ESC [Pnm	SGR	Enter/Exit select graphic rendition mode. Pn = 0 = Exit all attributes. 1 = Bold Intensity. 2 = Enter 1/2 intensity. 4 = Enter underline. 5 = Enter blinking. 7 = Enter reverse video. 10 = Enter graphics mode. 11 = Exit graphics mode. The default value is zero.
ESC [?6h	DOMR	Origin mode relative. Positions the cursor at the upper left hand character position within the margin. line numbers are relative to current margin settings.
ESC [?6l[1]	DOMA	Origin mode absolute. Positions the cursor outside the margin settings through the use of CUP or HVP controls. Line numbers are independent of margin settings.
ESC [~	SS3	Help key

[1] Denotes lower case L.

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ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC [>6h	SM	Entered keypad shifted mode. Inverts the normal and shifted functions of the keypad.
ESC [>6l[1]	SM	Exit keypad shifted mode.
ESC = or ESC [>7h	SM	Enter alternate keypad mode. Transmits the special escape codes used by software instead of normal characters.
ESC [>7l[1]	RM	Exit alternate keypad mode.
ESC [?1h	DCKA	Cursor key mode set. This mode is only used in the application keypad mode. The four cursor keys send application functions.
ESC [?1l[1]	DCKC	Cursor key mode reset. This mode is only used in the cursor keypad mode. The four cursor keys send ANSI cursor control commands.
ESC >	DKNM	Keypad numeric mode. Sends ASCII codes corresponding to the engraved key characters.
ESC [Pnq	DLL	Load LEDs. Loads the four programmable LEDs. Pn = 0 = Clear all LEDs. 1 = Light L1 2 = Light L2 3 = Light L3 4 = Light L4

KEY	ESCAPE CODE
0	ESCOp
1	ESCOq
2	ESCOr
3	ESCOs
4	ESCOt
5	ESCOu
6	ESCOv
7	ESCOw
8	ESCOx
9	ESCOy
–	ESCOm
.	ESCOn
,	ESCOl
ENTER	ESCOM

[1] Denotes lower case L.

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Additional Functions

ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC [?8h	DRMO	Auto repeat mode on. Keyboard keys auto repeat.
ESC [?8l[1]	DRMF	Auto repeat mode off.
ESC [2h	SM	Keyboard disabled.
ESC [2l[1]	RM	Keyboard enable. Enables the keyboard output.
ESC [?7h	SM	Wrap around at end of line. A wrap around is performed when the first character of the next line is entered.
ESC [?7l[1]	RM	Discard at end of line.
ESC [<sol>c	DREQ	Request terminal parameters. The terminal reports the parameters as: ESC [<sol>;<par>;<nbits>;<xspeed>; <rspeed>;<clkmul>;<flags>x sol = 0 = Send unsolicited reports. 1 = Send reports upon request. 2 = Message is a report. 3 = Message is a report on request. par = 1 = No parity. 2 = Space parity. 3 = Mark parity. 4 = Odd parity. 5 = Even parity. nbits = 1 = 8 bits per character. 2 = 7 bits per character. xspeed/ = 0 = 50 baud. rspeed 8 = 75 baud. 16 = 110 baud. 24 = 134.5 baud. 32 = 150 baud. 40 = 200 baud. 48 = 300 baud. 56 = 600 baud. 64 = 1200 baud. 72 = 1800 baud. 80 = 2000 baud. 88 = 2400 baud. 96 = 3600 baud. 104 = 4800 baud. 112 = 9600 baud. 120 = 19200 baud. 128 = 1050 baud. 136 = 7200 baud. clkmul = 16 bit rate multiplier. flags = 0

[1] Denotes lower case L.

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Additional Functions (continued)

ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC [2;Psy	DTST	Confidence test. Ps = DECIMAL — TEST 0 — No test. 1 — Power up. 2 — Reserved. 4 — Reserved. 16 — Video RAM. 32 — Display character set. 64 — Keyboard. 128 — Reserved. To run the test continously add 8 to the number. EXAMPLE: To run the Video RAM test continously add 16 + 8, then enter ESC[2;24y.

Print Functions

ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC [?5i	DAP	Auto print on. Turns on auto print. A display line will be printed after moving the cursor off the line by using LF, CR, or vertical tab (also transmitted to the printer). The line also prints during an autowrap. Auto wrap lines end with a return. When double high/double wide lines are sent to the printer, they are converted to single wide lines. If double wide characters are sent to the printer, each character is followed by a space.
ESC [?4i	DAPO	Auto print off. Turn media copy off.
ESC [5i	DPC	Printer controller on. Enables Blind Print (printer controller). The printer transmits received characters to printer without displaying them. The terminal does not insert or delete spaces, provide line delimiters, or select the correct character set.
ESC [4i	DPCO	Printer controller off. Disables Blind Print.

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Print Functions (continued)

ESCAPE SEQUENCE	MNEMONIC	DEFINITION
ESC [?1i	DPCL	Print cursor line. Prints line at cursor location. KEYBOARD LOCKED is enabled. Cursor position does not change. Command ends when the line is printed. When double high/double wide lines are sent to the printer, they are converted to single wide lines. If double wide characters are sent to the printer, each character is followed by a space. A beep sounds at the end of the line.
ESC [i or ESC [0i	DPS	Print screen. Prints the full screen or selected scrolling region as determined by Printer Extent ESC [?19h or ESC [?19i. KEYBOARD LOCKED is enabled. When double high/double wide lines are sent to the printer, they are converted to single wide lines. If double wide characters are sent to the printer, each character is followed by a space. Print screen ends when the screen is printed and a beep will sound.
ESC [?19h	DPXF	Printer extent mode. Prints full screen when print screen selected. When double high/double wide lines are sent to the printer, they are converted to single wide lines. If double wide characters are sent to the printer, each character is followed by a space.
ESC [?19l[1]	DPXR	Printer extent mode. Prints scrolling region when print screen selected. When double high/double wide lines are sent to the printer, they are converted to single wide lines. If double wide characters are sent to the printer, each character is followed by a space.
ESC [?18h	DPTC	Print termination character. Prints termination character form feed (hex, E).
ESC [?18l[1]	DPT	Disable print termination character.
ESC [?15n	DPSR	Request printer status report. A cable must be connected between the terminal and printer, or an erronous report will be recieved. Response: ESC[?13n = Printer was off from power up ESC[?11n = Printer was on but is now off Esc[?10n = Printer ready

[1] Denotes lower case L.

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NOTE: The terminal transmits the following escape codes to perform a user-defined function. There is no response by the terminal.

TRANSMITTED CODE	MNEMONIC	KEY	Z-29 KEYS
ESC OP	SS3	Function key (PF1)	(F6) Blue
ESC OQ	SS3	Function key (PF2)	(F7) Red
ESC OR	SS3	Function key (PF3)	(F8) Gray
ESC OS	SS3	Function key (PF4)	(F1)
ESC OT	SS3	Function key (F5)	(F2)
ESC OU	SS3	Function key (F6)	(F3)
ESC OV	SS3	Function key (F7)	(F4)
ESC OW	SS3	Function key (F8)	(F5)
ESC OX	SS3	Function key (F9)	(F9)

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Software Handshake

The terminal operates up to 19,200 baud. Incoming characters are stored in a 128-character buffer and processed on a first in/first out (FIFO) basis. When the buffer contents reach 96 characters, the terminal transmits 13H (XOFF or DC3). The host computer will stop transmitting to the terminal, upon receipt of this signal. The terminal will continue to deplete the buffer.

When 32 characters are left in the buffer, the terminal transmits 11H (XON or DC1) signaling the host to resume transmission. If the host fails to respond to a XOFF from the terminal in a timely manner, the buffer will continue to fill. When the 128 character capacity is exceeded, a buffer overflow will occur. To determine when the buffer will overflow, use the following formula:

$$\text{Time to respond to XOFF} = \frac{[\text{buffer length-XOFF point-worst case(receive speed/transmit speed)}] \times [\text{bits per character} + \text{parity bits} + \text{stop bit} + \text{start bit}]}{\text{receive speed}}$$

Example:

The terminal is transmitting and receiving at 9600 baud, 8 bits per character, no parity, buffer length = 128, and XOFF point = 96. The terminal has just sent an XOFF which the host must respond to within ?.?? milliseconds.

$$\text{Time to XOFF} = \frac{[128\text{-}96\text{-}3(9600/9600)] \times [8+0+2]}{9600} = 30.208 \text{ millisecs.}$$

When the buffer overflows, the terminal discards the most recent character in the buffer and places the current character into the buffer.

Software that does not support receipt of the XOFF/XON signals can still use the terminal, provided the software never sends the ESC code to the terminal, the baud rate is limited to 4800 or less, and smooth scroll is not used.

Alternately, if XOFF/XON can not be used, a fill character such as NUL (00H) can be used following certain character strings which are sent to the terminal. Table 1 provides a list of fill character requirements.

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Fill Character Requirements

Fill characters are required to keep the terminal synchronized with the host computer when the XOFF/XON codes are not used. Table 5.1 shows the terminal fill character requirements for every terminal receive speed. No entry in a column indicates that fill characters are not required. All entries indicate the worst case. In some situations, the terminal can actually operate with less fill characters.

NUL characters take time for the computer to process, if a time delay is available from the host computer and inserted in place of a Nul character the time between characters at baud rates will be reduced.

Another way to transmit XOFF/XON is by using CTRL and S keys for XOFF and CTRL and Q keys for XON.The terminal coordinates the two sources so that the desired effect occurs. For example, if the buffer filling condition has sent a XOFF and the operator presses the CTRL and S keys, a second XOFF is not sent. When the buffer is empty an XON will not be sent until the operator presses the CTRL and Q keys.

In the Setup mode, XOFF is transmitted as soon as SETUP is entered and an XON is transmitted on exiting SETUP>

When hardware handshaking is used, the buffer filling condition does not transmit a XOFF, CTRL and S keys, and CTRL and Q keys are transmitted as typed.

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Table B.1. Fill Character Requirements

RECEIVE BAUD RATE	FUNCTION NUMBER						
	1	2	3	4	5	6	7
19200	2	90	243	243	4	384	60
9600	1	45	122	122	2	192	30
7200		34	92	92	2	144	22
4800		15	61	61	1	96	15
2400		11	30	30		48	7
2000		9	25	25		40	6
1800		9	23	23		36	6
1200		6	15	15		24	4
1050		5	14	14		21	4
600		3	8	8		12	2
300		1	4	4		6	1
200		1	3	3		4	1
150		1	2	2		3	
134.5		1	2	2		3	
110		1	1	1		2	
75			1	1		2	
50			1	1		1	

Explanation of Function Number:

1. All characters except those listed below.
2. Erase in Display.
3. Columns.
4. Alignment.
5. Erase in Line.
6. (Smooth Scroll) Line Feed, Reverse Index, Index, Next Line.
7. (Jump Scroll) Line Feed, Reverse Index, Index, Next Line.

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