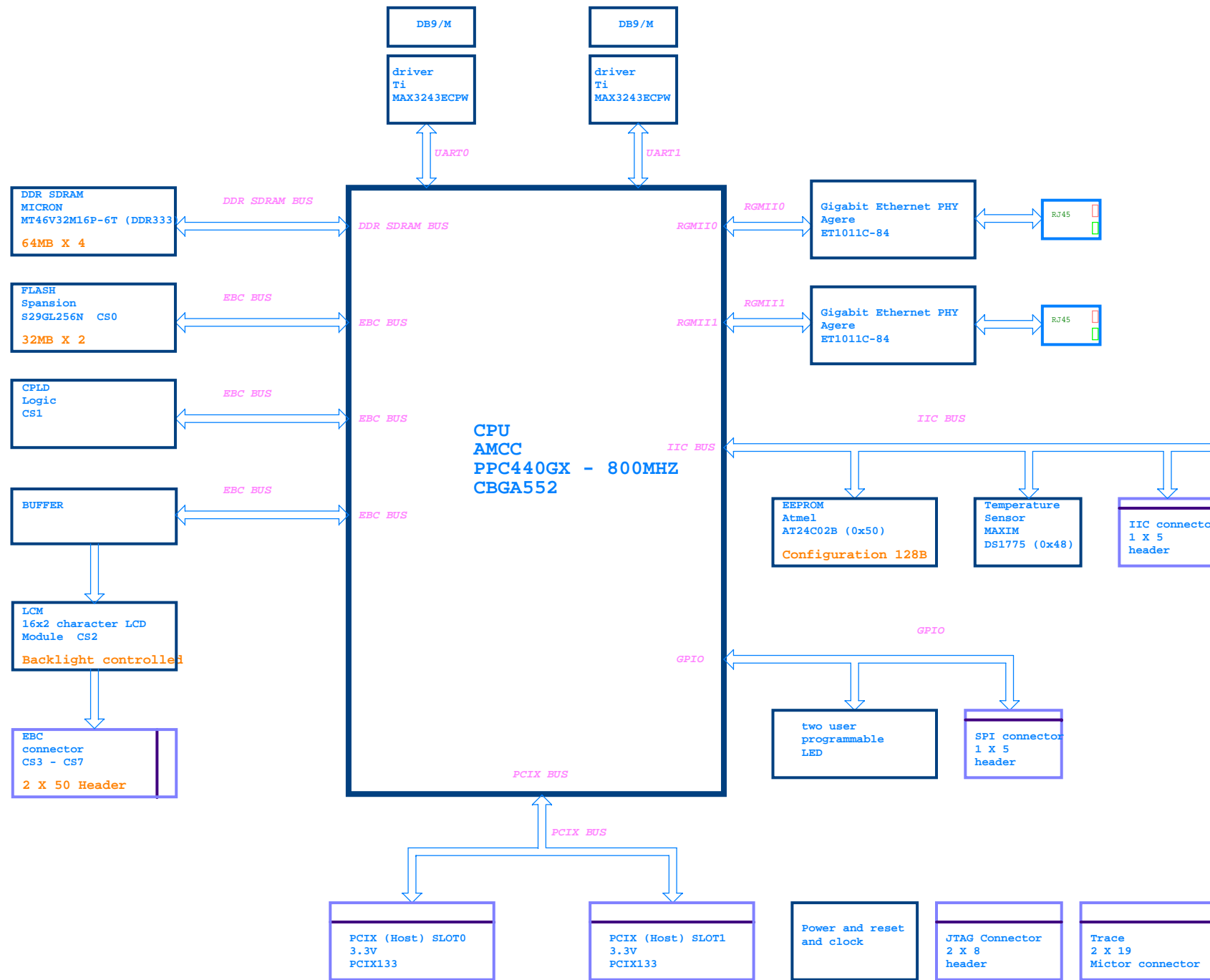
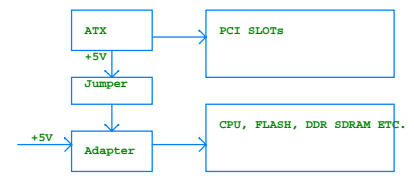
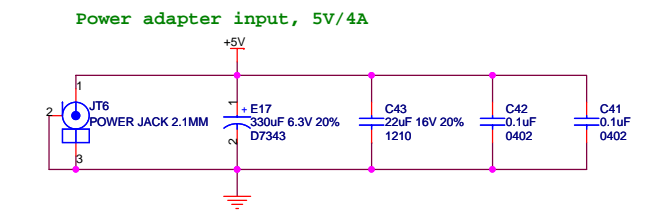
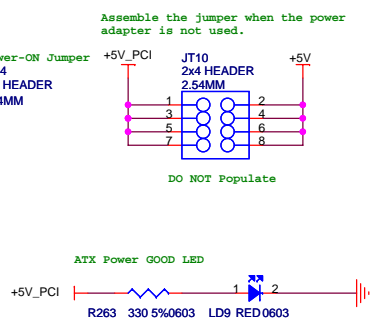
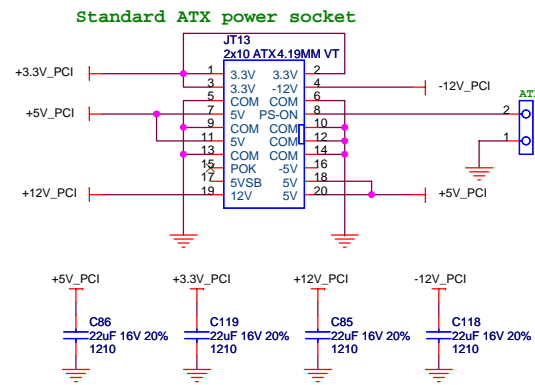


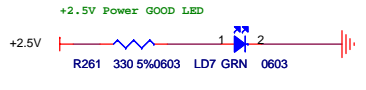
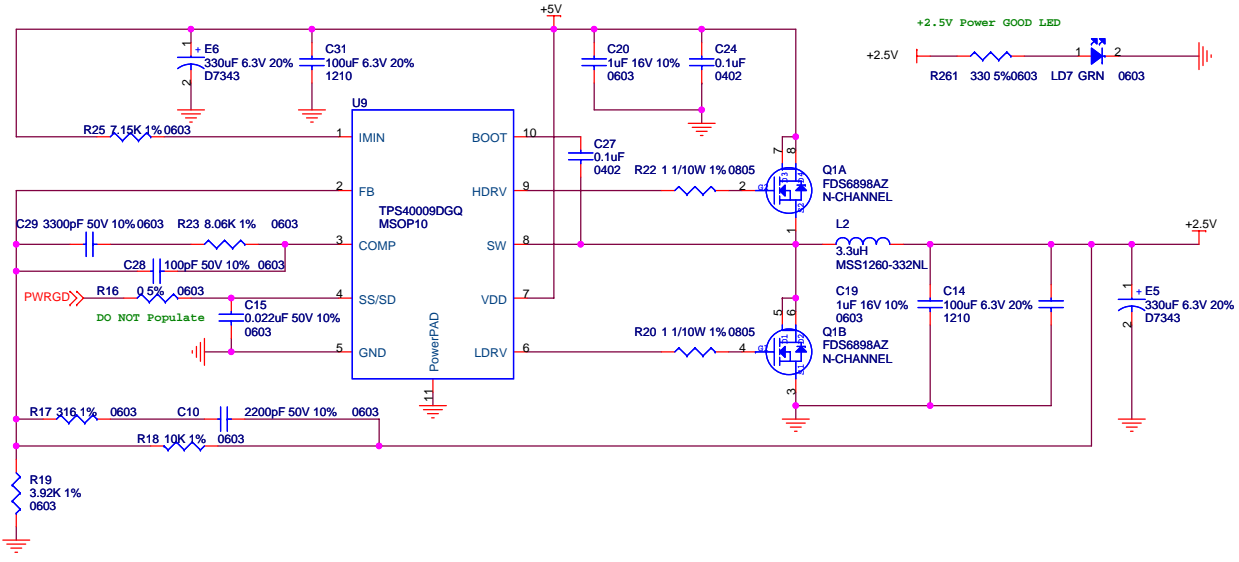
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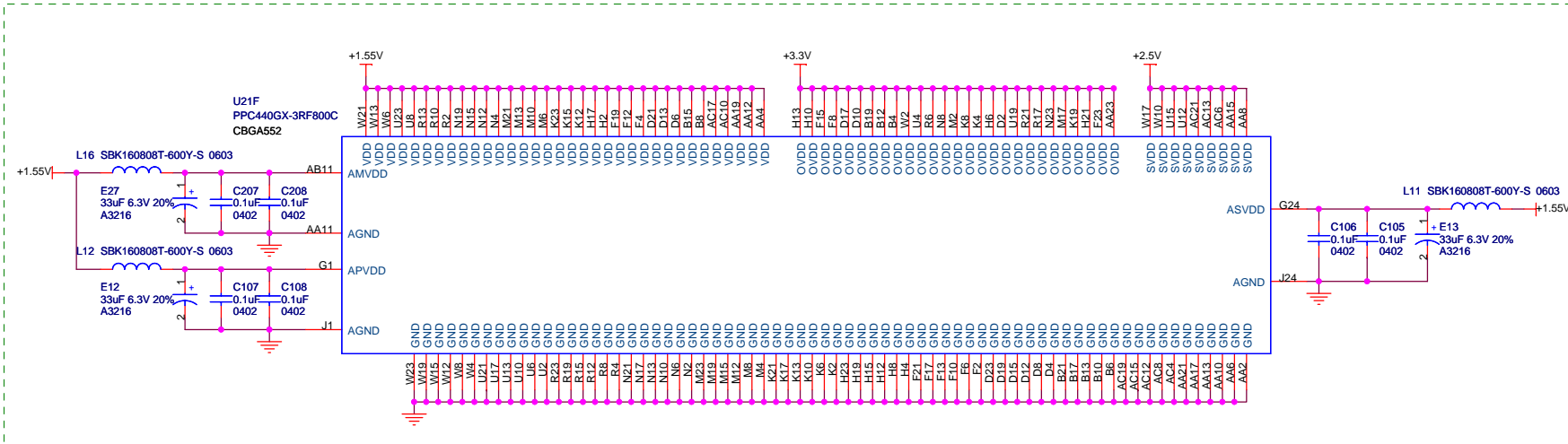
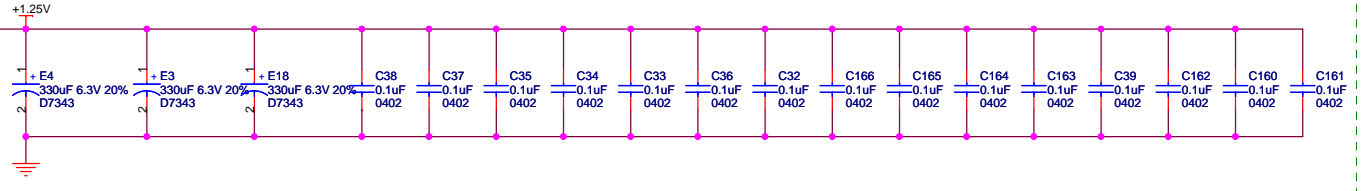
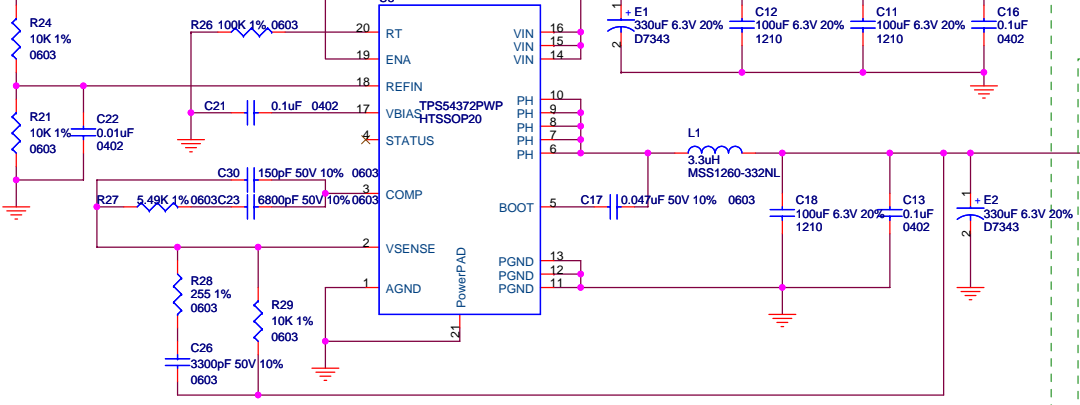




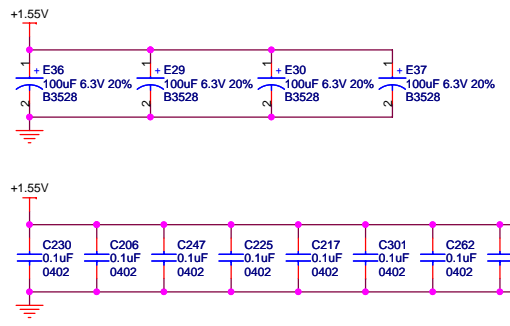
+2.5V Power Supply



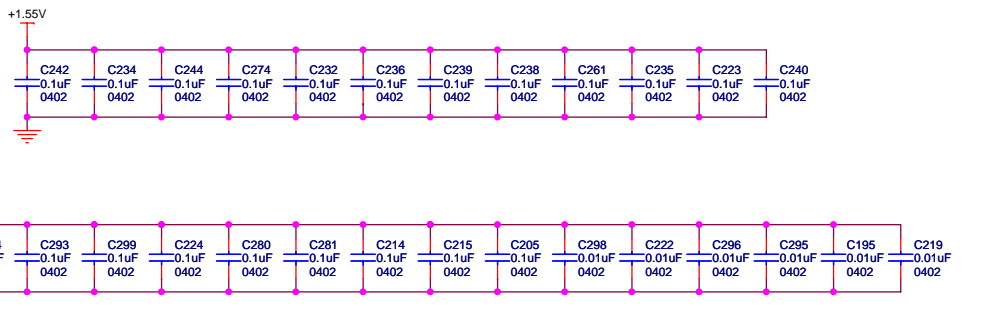
+1.25V Power Supply



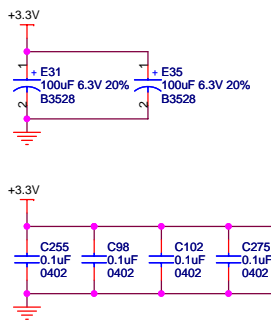
Bulk Decoupling: One cap in each corner of CPU



CPU Core by-pass caps place as close to CPU VDD pins as possible

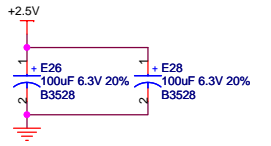


Bulk Decoupling: One cap in each corner of CPU

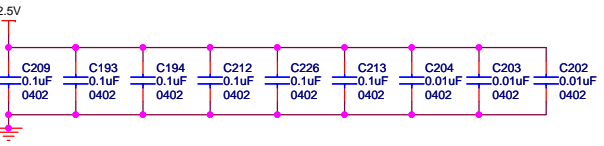



CPU I/O by-pass caps place as close to CPU OVDD pins as possible

Bulk Decoupling: One cap in each corner of CPU



CPU 2.5V I/O by-pass caps place as close to CPU SVDD pins as possible



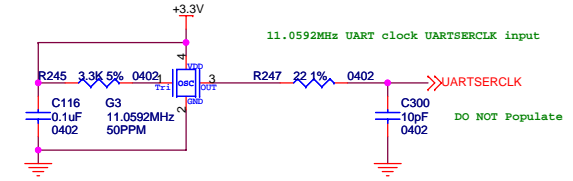
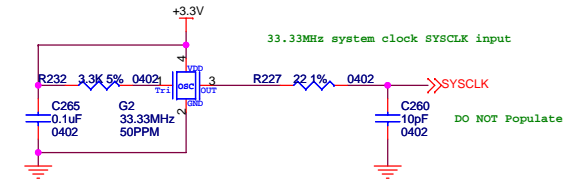
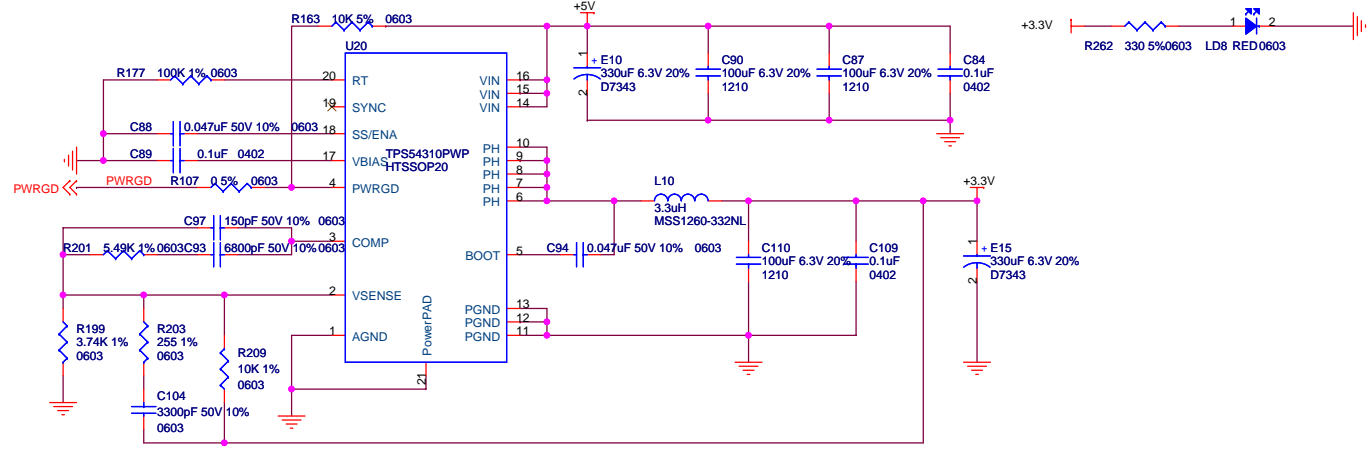


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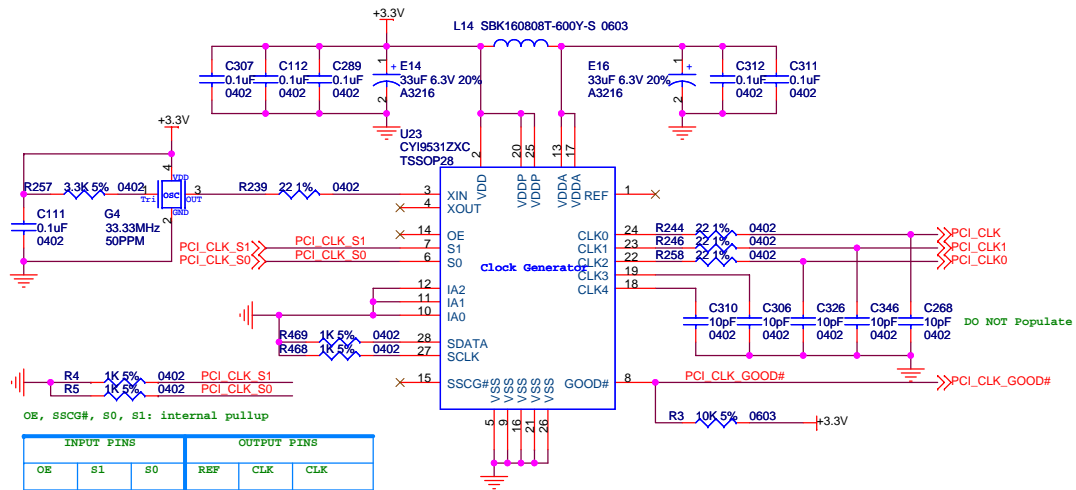
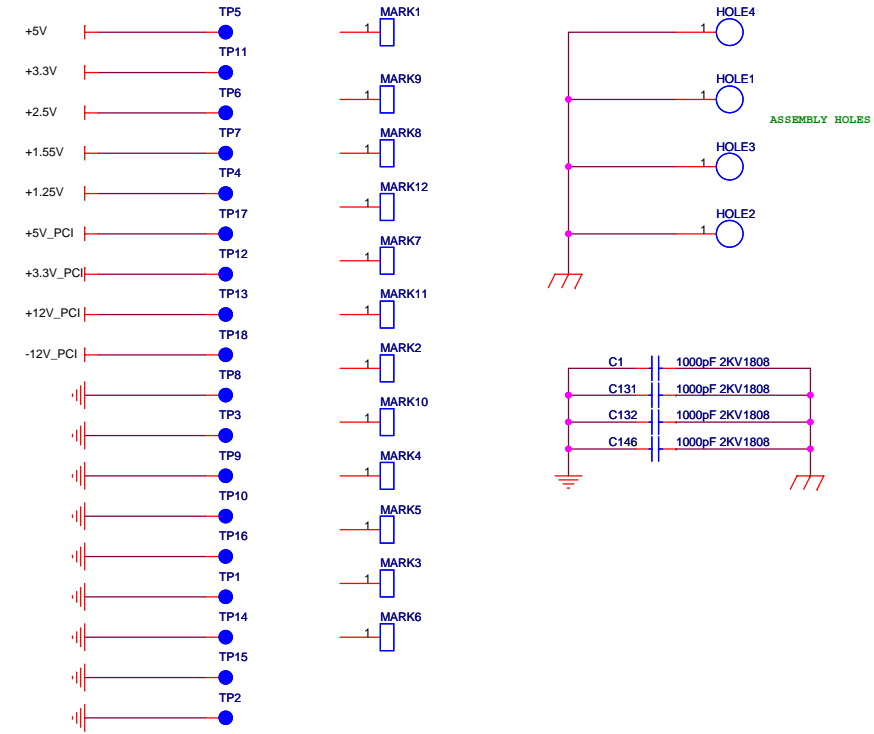
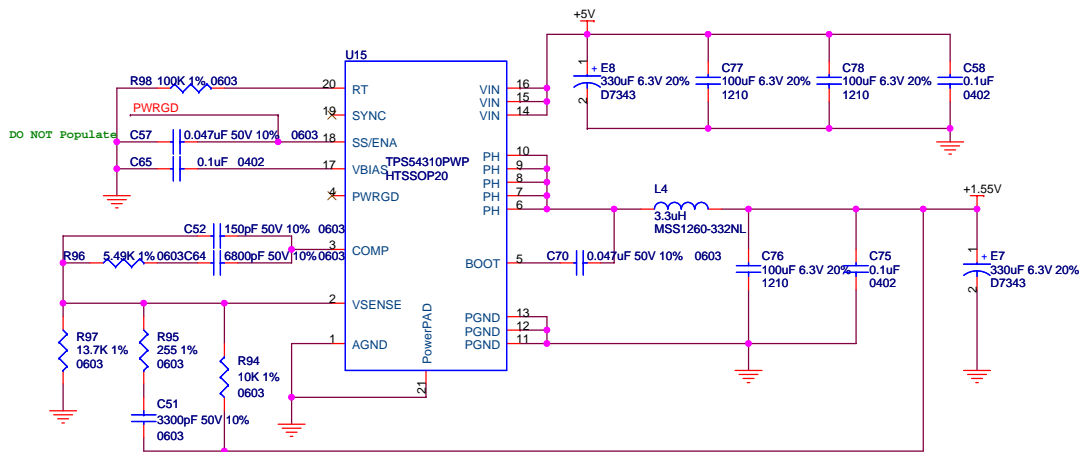
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Title: Power CPU, +2.5V, +1.25V		
Size: Custom	Document Number: Taishan440GX	Rev: 1.0
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+3.3V Power Supply



+1.55V Power Supply



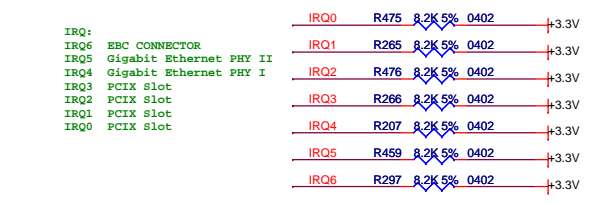
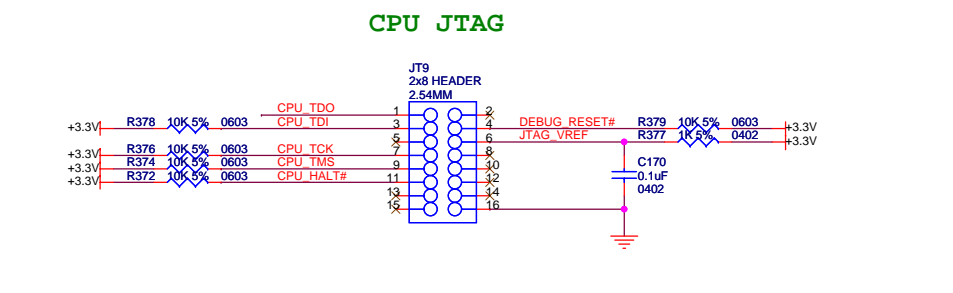
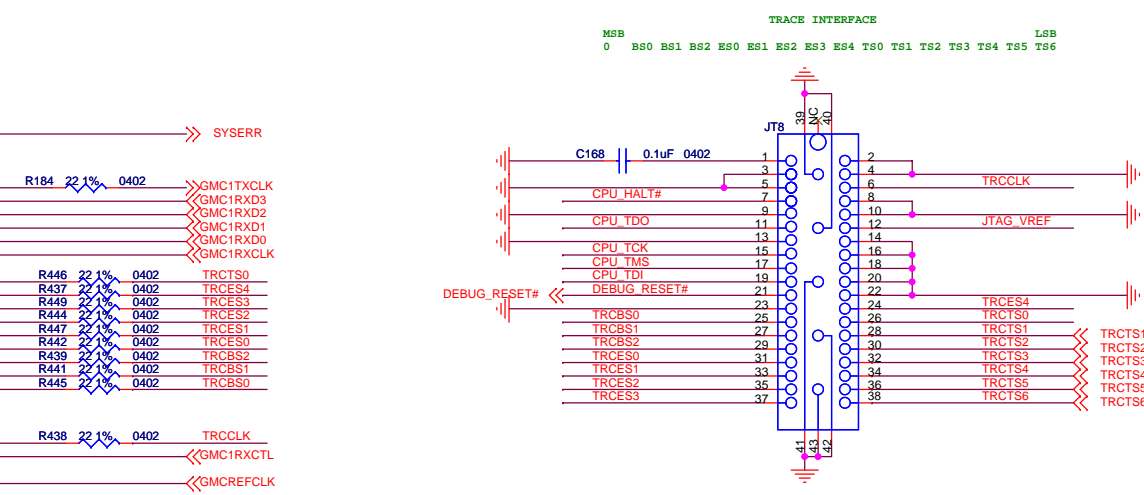
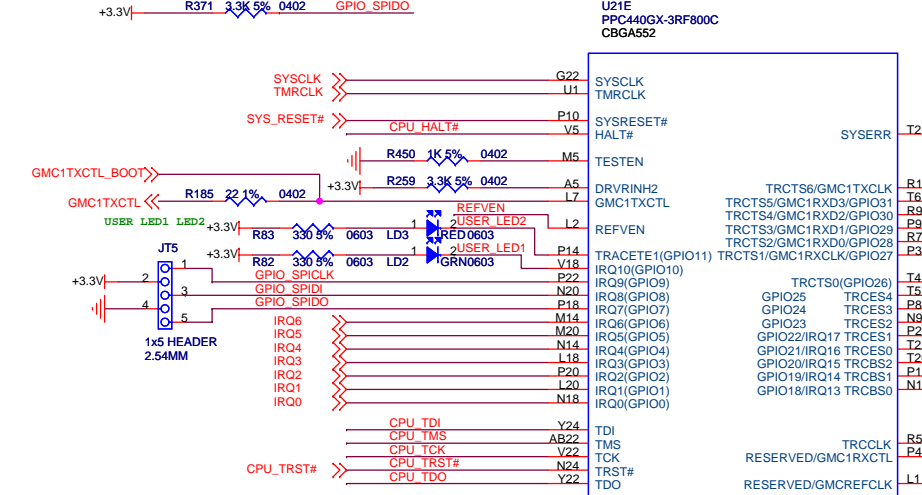
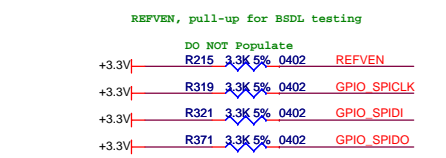
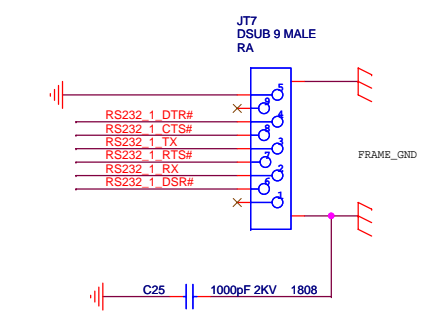
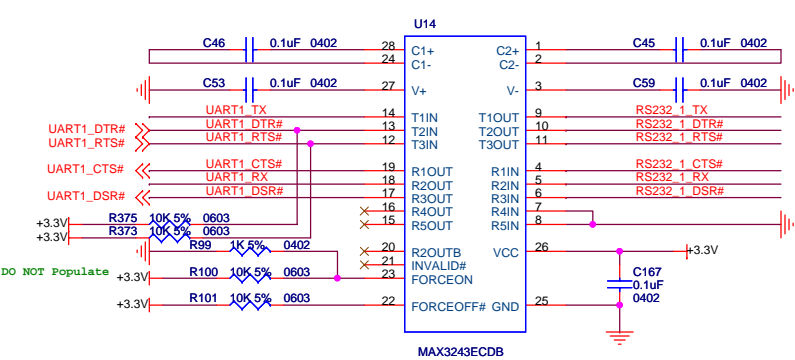
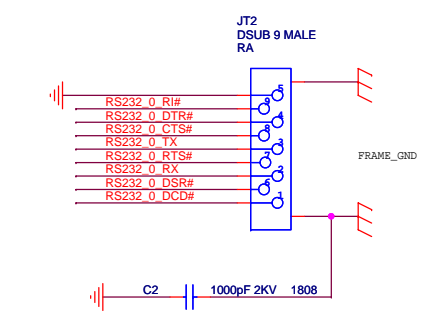
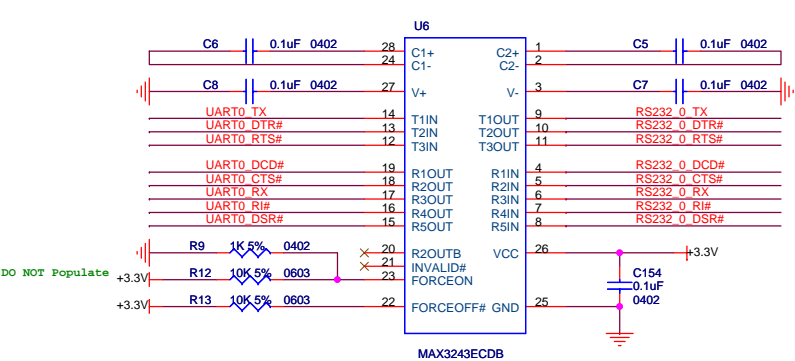
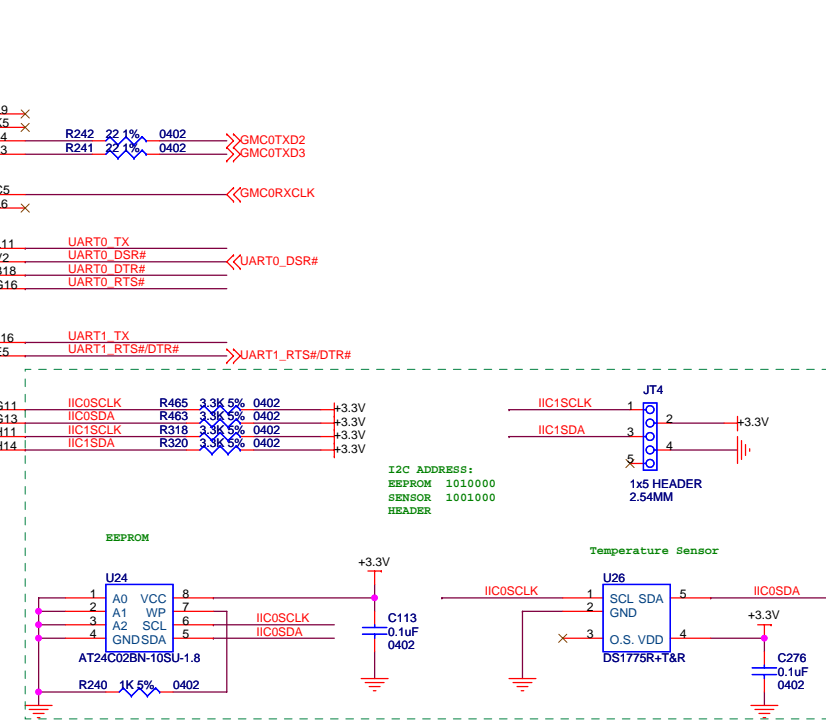
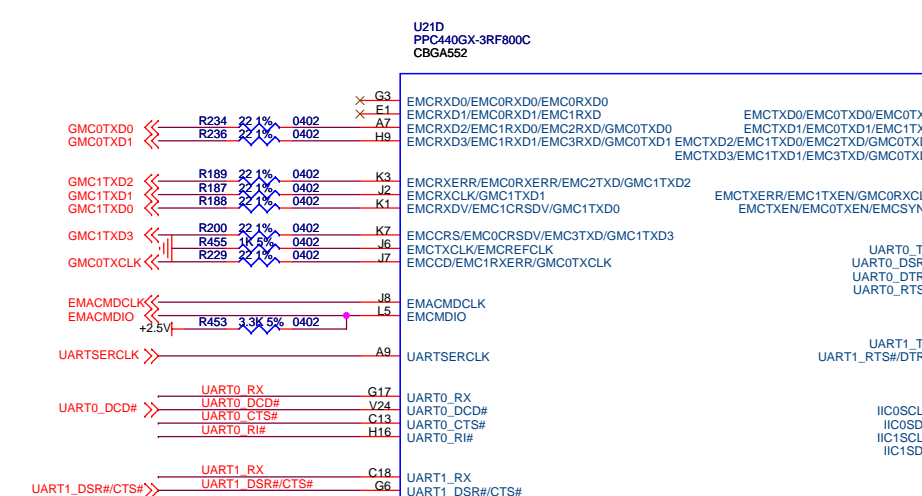
OE, S8CG#, S0, S1: internal pullup

INPUT PINS			OUTPUT PINS		
OE	S1	S0	REF	CLK	CLK
HIGH	LOW	LOW	XIN	XIN	33.33MHz
HIGH	LOW	HIGH	XIN	2*XIN	66.66MHz
HIGH	HIGH	LOW	XIN	3*XIN	100MHz
HIGH	HIGH	HIGH	XIN	4*XIN	133.33MHz
LOW	X	X	TRI-STATE	TRI-STATE	X

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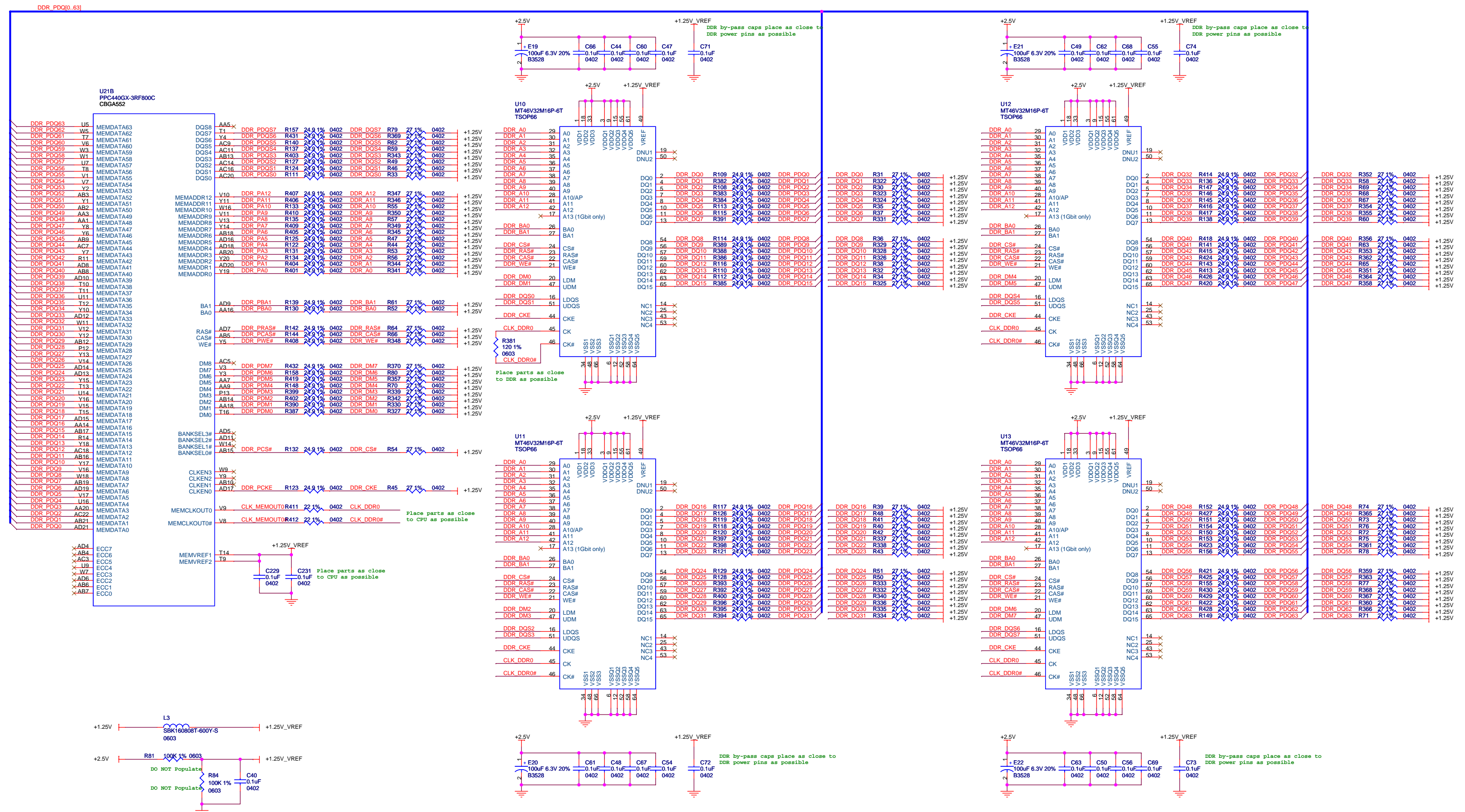
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Size: Custom	Document Number: Taishan440GX	Rev: 1.0
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Title: RGMIL, UART, GPIO, IRQ, Debug		
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Date: Friday, September 15, 2006	Sheet: 5 of 10	

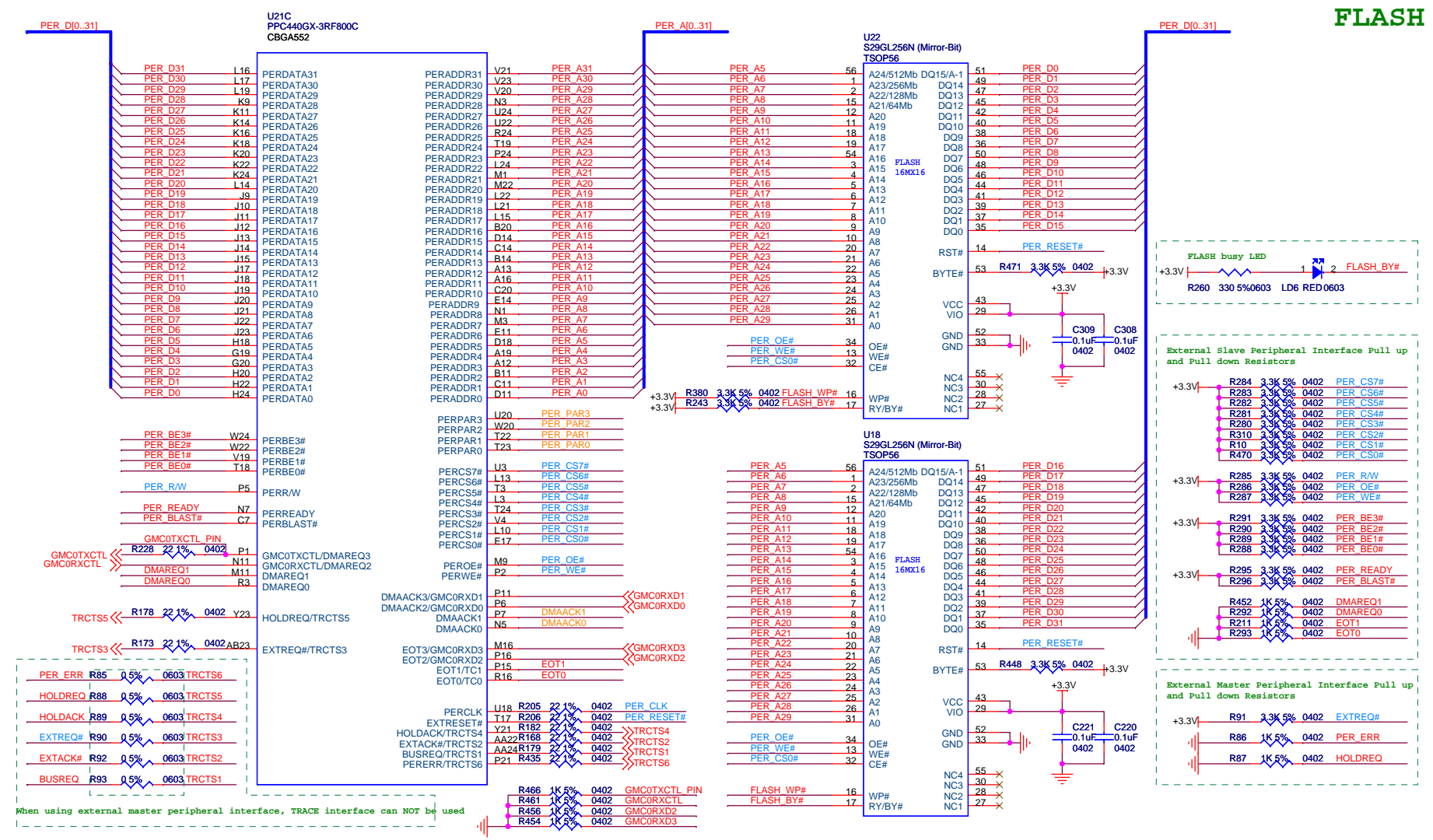




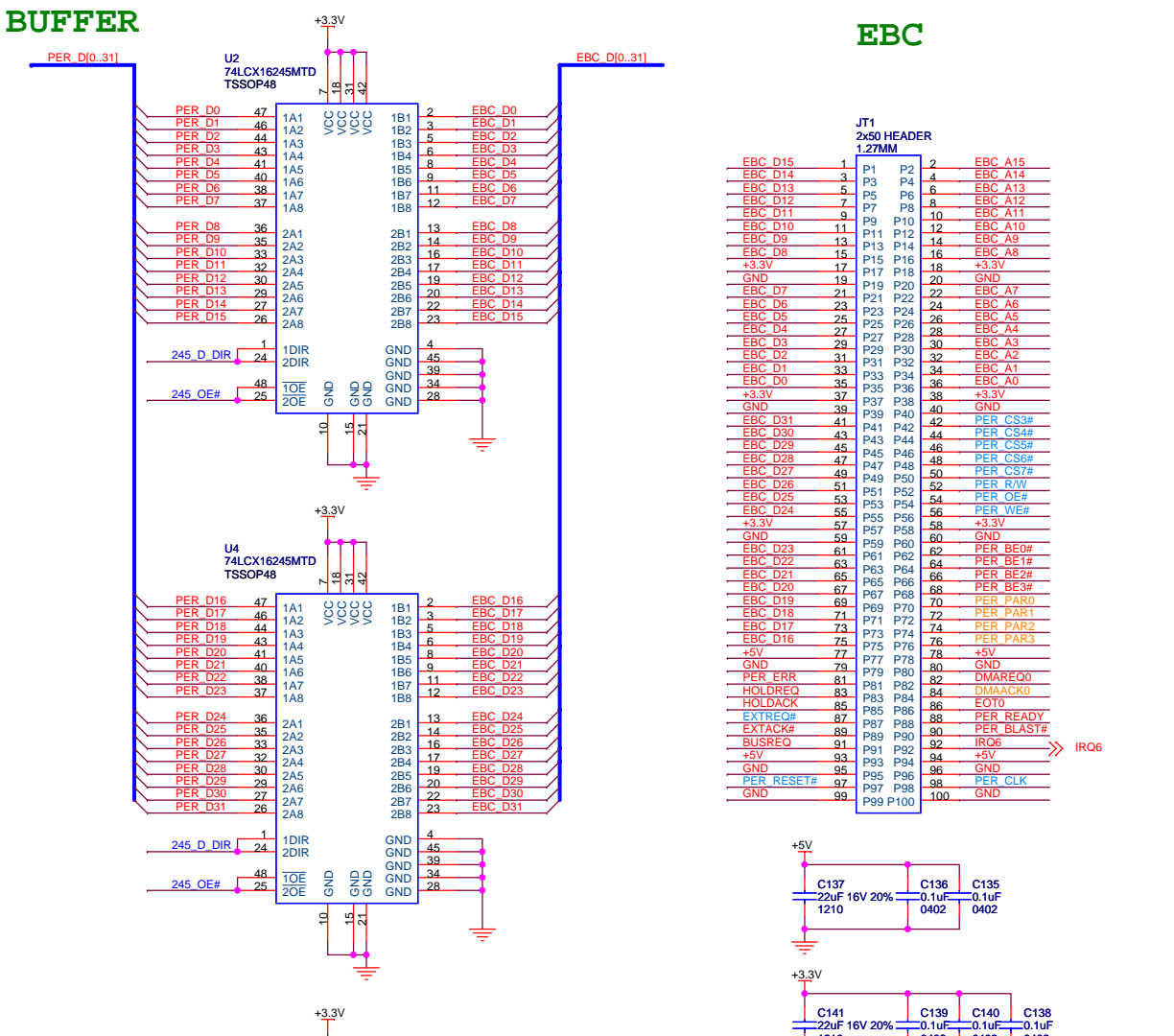
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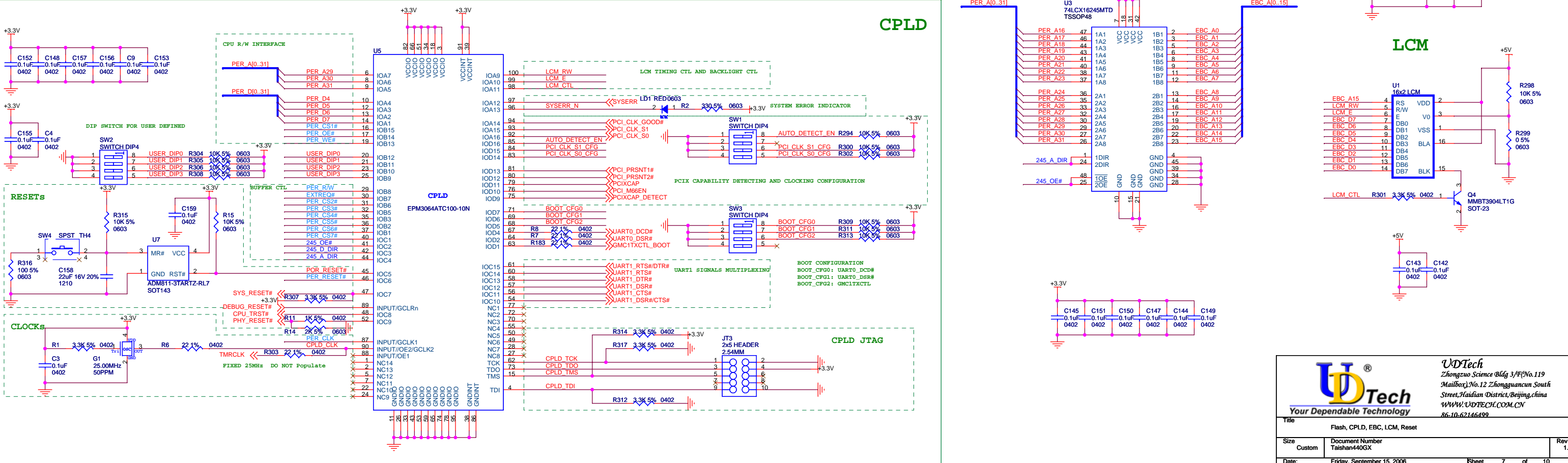
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Size Custom	Document Number Taishan4400X		Rev 1.0
Date: Friday, September 15, 2006	Sheet 6	of 10	



FLASH BUFFER



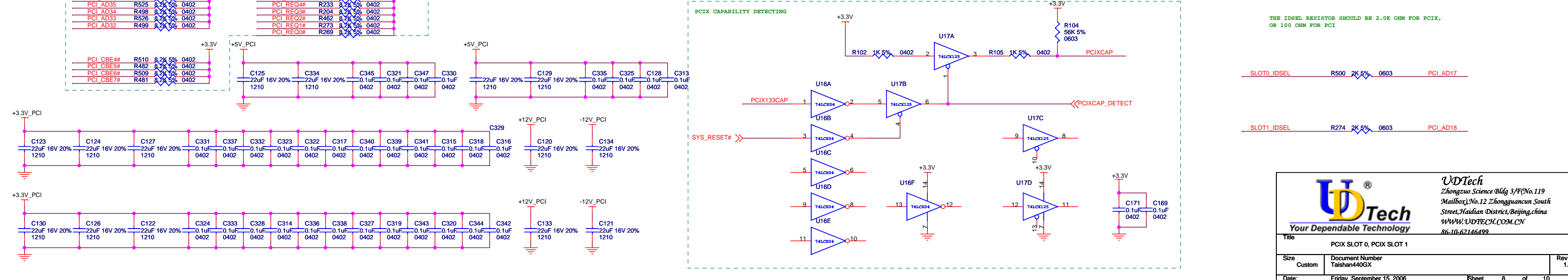
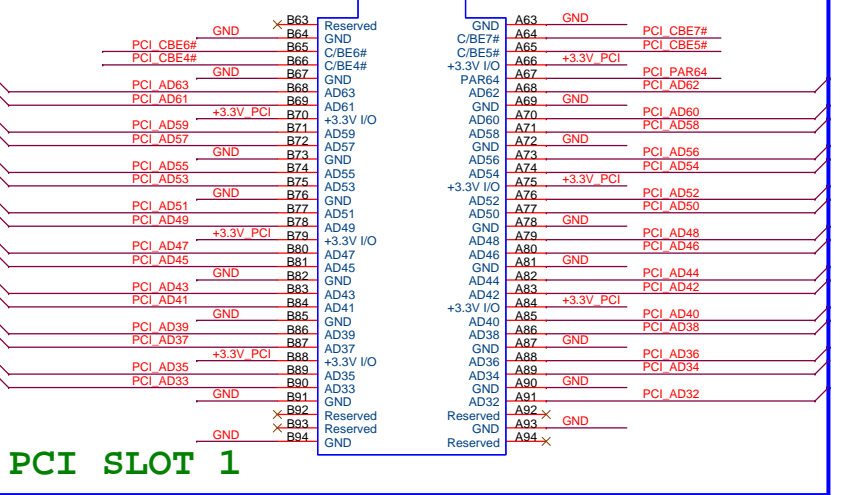
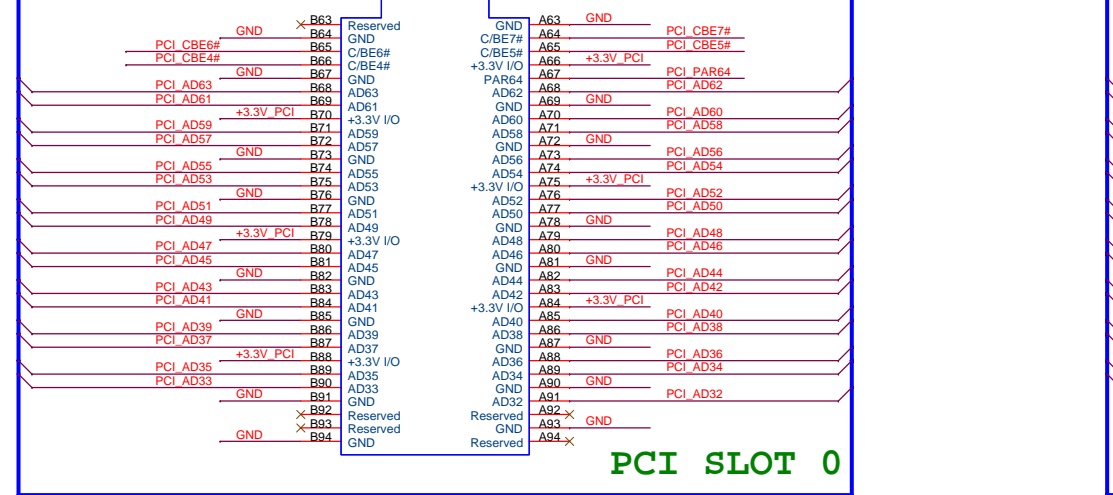
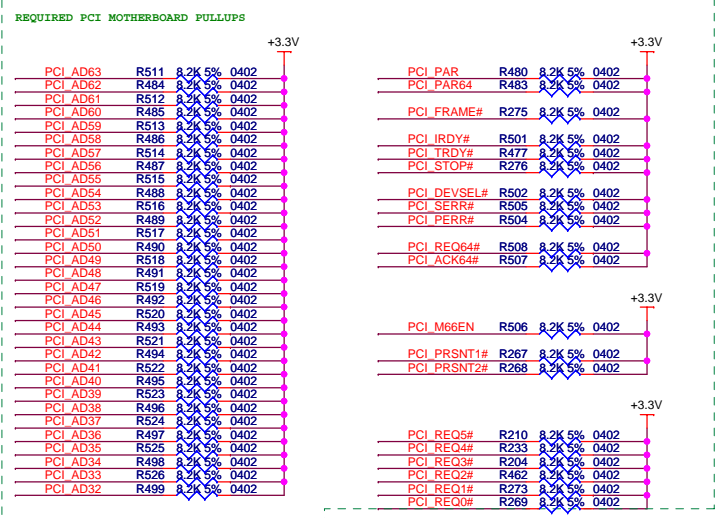
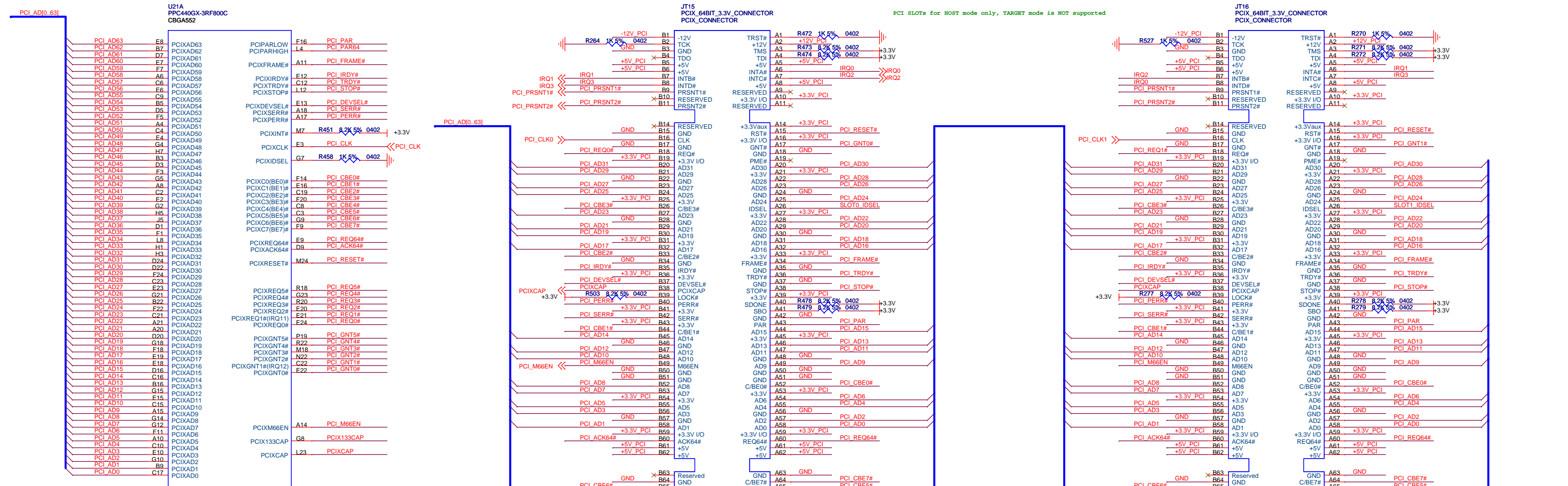
CPLD



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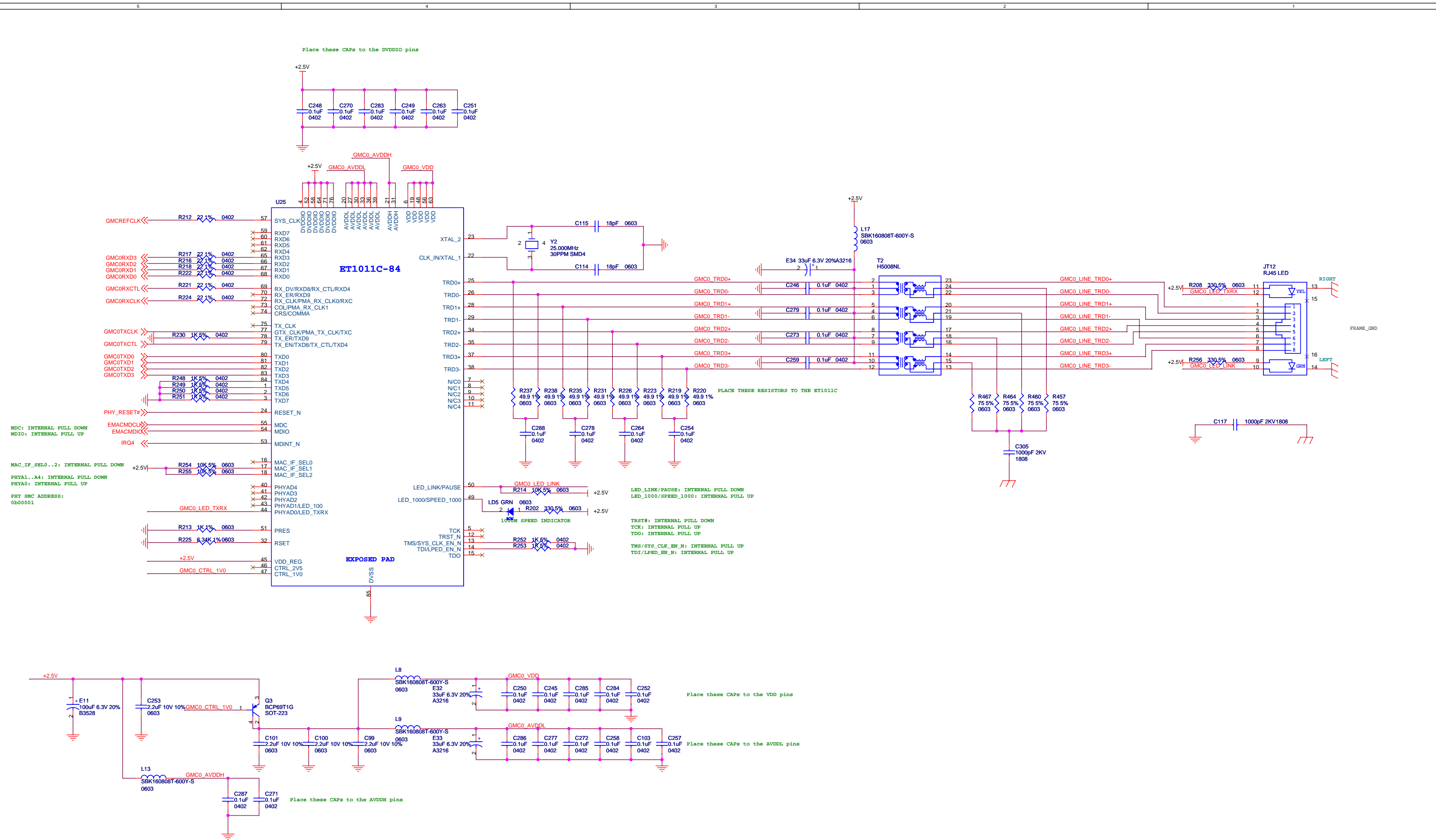
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Size	Custom	Document Number	Taishan440GX		
Date:	Friday, September 15, 2006	Sheet	7	of	10
Rev	1.0				



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Title		PCIX SLOT 0, PCIX SLOT 1		Rev	1.0
Size	Custom	Document Number	Taishan440X	Date	Friday, September 15, 2006
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Place these CAPs to the DVDDIO pins

PLACE THESE RESISTORS TO THE ET1011C

Place these CAPs to the VDD pins

Place these CAPs to the AVDDL pins

Place these CAPs to the AVDDH pins

MDC: INTERNAL PULL DOWN
MDIO: INTERNAL PULL UP

MAC_IF_SEL0..2: INTERNAL PULL DOWN
PHYA1..A4: INTERNAL PULL DOWN
PHYAD: INTERNAL PULL UP

PHY SMC ADDRESS:
0b00001

LED_LINK/PAUSE: INTERNAL PULL DOWN
LED_1000/SPEED_1000: INTERNAL PULL UP

TRST#: INTERNAL PULL DOWN
TCK: INTERNAL PULL UP
TDO: INTERNAL PULL UP

TMS/SYS_CLK_EN_N: INTERNAL PULL UP
TDI/LPED_EN_N: INTERNAL PULL UP

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		Title Gigabit Ethernet I	
Size Custom	Document Number Taishan440GX	Rev 1.0	
Date: Friday, September 15, 2006	Sheet 9	of 10	

