MACH™ Family Data Book

High Density EE CMOS Programmable Logic

Summer 1992

Advanced
Micro
Devices

INCLUDES THE NEW MACH215 DATA SHEET

MACH™ 1 and MACH 2 Families

High Density EE CMOS Programmable Logic

Q3 1992 Data Book

Final:

MACH110-12/15/20 Com'l, Mil
MASC110-15/20 Com'l
MACH120 Com'l
MACH130-15/20 Com'l, Mil
MACH210-12/15/20 Com'l, Mil
MASC210-15/20 Com'l
MACH220 Com'l
MACH230-15/20 Com'l

Preliminary:

MACH215-12/15/20
MACH230 Mil

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If you have always wanted higher-density EE CMOS PAL® devices, with no penalty in speed or cost per function, this booklet will help you a lot!

We have taken our high-volume 0.8 micron EE CMOS PAL device process and applied it to a new family of 44-, 68-, and 84-pin 12- and 15-ns PLDs aimed at letting you meet your designs' speed and real estate targets.

In just a few short years, AMD has become a force in CMOS PLDs, building on our #1 spot in bipolar. With the new benefits that our breakthrough architecture CMOS family brings you, we continue moving towards the #1 spot in CMOS too.

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Chris Henry
Director of Marketing
Programmable Logic

INTRODUCTION

This book introduces you to the new MACH 1 and MACH 2 families of programmable logic from Advanced Micro Devices. These devices provide programmable logic capabilities from around 900 gates to 3600 gates. Included in this book are a general discussion; final data sheets for the six original MACH family members; and preliminary data sheets for the military MACH230 and the new asynchronous MACH215.

The general discussion deals with those issues that affect the entire device family, including a brief discussion of design software used in configuring the devices. Because of the common architecture, most of the understanding of the device can come from a look at the family as a whole. Individual devices differ only in number of resources.

The data sheets discuss items that are specific to each device. They contain the basic DC and switching specifications. Other general specifications, such as switching waveforms and endurance, follow the data sheets, since they are the same for all devices.

Rounding out this book is the MACH Device Design Planning Guide. This section introduces you to the methodology of designing with MACH devices. It will help you select the right device and will show you how to structure your designs for successful fitting within a MACH device.

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MACH Device Family

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High-performance, high-density, electrically-erasable CMOS PLD families**
- **900 to 3600 gate equivalents**
- **44 to 84 pins in cost-effective PLCC and CQFP packages**
- **32 to 128 macrocells**
- **0.8 µm CMOS provides predictable design-independent high speeds**
  - Commercial 12/15/20-ns t_{PD}, 67/50/40-MHz f_{MAX}
  - Military 20-ns t_{PD}, 40-MHz f_{MAX}
- **Synchronous and asynchronous devices**
- **PAL blocks connected by switch matrix**
  - Provides optimized global connectivity
  - Switch matrix integrates blocks into uniform device
- **Configurable macrocells**
  - Programmable polarity
  - Registered or combinatorial
  - Internal and I/O feedback
  - D-type or T-type flip-flops
  - Choice of clocks for each flip-flop
  - Input registers for MACH 2 family
- **Extensive third-party software and programmer support through FusionPLD℠ partners**
  - Schematic capture and text entry
  - Compilation and JEDEC file generation
  - Design simulation
  - Logic and timing models
  - Standard PLD programmers
- **Each MACH product has a metal-masked MASC™ product counterpart with exactly equivalent specifications for high-volume applications**

PRODUCT SELECTOR GUIDE

Device	Pins	Macrocells	Gate Equivalents	Max Inputs	Max Outputs	Max Flip-Flops	Speed (ns)
MACH 1 Family							
MACH110	44	32	900	38	32	32	12,15, 20
MACH120	68	48	1200	56	48	48	15, 20
MACH130	84	64	1800	70	64	64	15, 20
MACH 2 Family							
MACH210	44	64	1800	38	32	64	12,15, 20
MACH220	68	96	2400	56	48	96	15, 20
MACH230	84	128	3600	70	64	128	15, 20
Asynchronous MACH Device							
MACH215	44	64	1500	38	32	64	12, 15, 20

GENERAL DESCRIPTION

The MACH (Macro Array CMOS High-density) family provides a new way to implement large logic designs in a programmable logic device. AMD has combined an innovative architecture with advanced CMOS technology to offer a device with several times the logic capability of the industry's most popular existing PAL device solutions at comparable speed and cost.

Their unique architecture makes these devices ideal for replacing large amounts of TTL logic. They are the first devices to provide such increased functionality without forcing the designer to sacrifice speed and cost.

The MACH devices consist of PAL blocks interconnected by a programmable switch matrix (Figure 1). Designs that consist of several interconnected functional modules can be efficiently implemented by placing the modules into the PAL blocks. Designs that are not as modular can still be implemented since the switch matrix provides a high level of connectivity between the PAL

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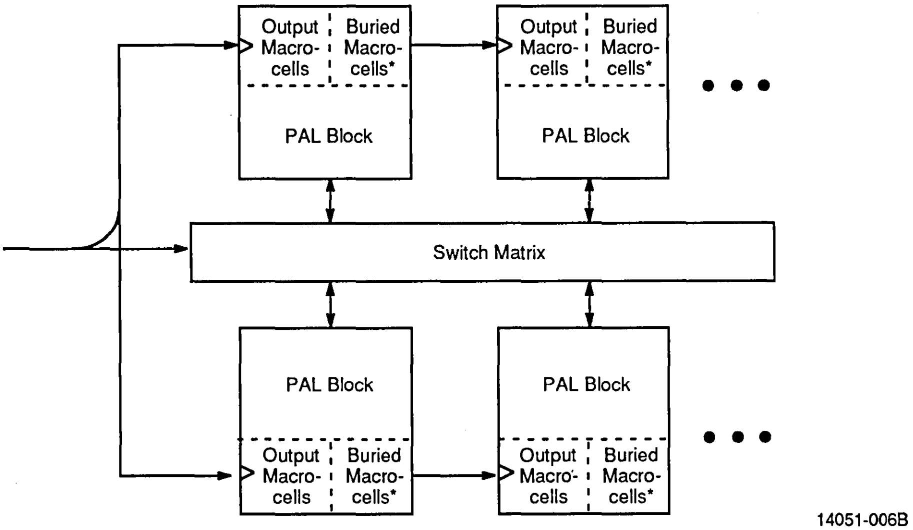
blocks. This internal arrangement of resources is managed automatically by the design software, so that the designer does not have to be concerned with the logic implementation details.

The MACH family consists of the MACH 1 and MACH 2 series of synchronous devices and the MACH215, an asynchronous device. The MACH 1 and 2 series are ideal for synchronous subsystems like memory controllers and peripheral controllers. The MACH215 is appropriate for applications having asynchronous inputs and for collecting random glue logic.

AMD's FusionPLD program allows MACH device designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. This ensures that a designer does not have to buy a complete new set of tools for each new device, but rather can count on the tools with which he or she is already familiar. The MACH devices can be programmed on conventional PAL device programmers with appropriate personality and socket adapter modules.

The MACH devices are manufactured using AMD's state-of-the-art advanced CMOS electrically-erasable process for high performance and logic density. The CMOS EE technology provides 100% testability, thus reducing the designer's prototype development costs.



* Buried macrocell available on MACH 2 devices only.

Figure 1. General MACH Device Block Diagram

Design Methodology

An important aspect of the MACH family is the fact that design tools are widely available both from AMD and from third-party software vendors. AMD provides PALASM® software as a low-cost baseline tool set and works with tools vendors to ensure broad MACH device support. This allows designers to do MACH device designs using the same tools that they would use to do PAL device designs, whether PALASM software or any of the other popular PAL device design packages.

Design entry is the same as that used for PAL devices, including the capability of using schematic capture. The basic logic processing steps are the same steps that are needed to process and minimize logic for any PAL device. Simulation is available for verifying the correct behavior of the device. Functional (unit-delay) simulation of MACH devices is supported in all approved software packages, and other options for simulating the timing and board-level behavior of the MACH devices are available. The end result is a JEDEC file that can be downloaded to a programmer for device configuration.

The MACH design methodology differs from that of a PAL device somewhat due to the automatic design fitting procedure that the software performs. Designs written by logic designers—whether by schematic capture, state machine equations, or Boolean equations—are partitioned and placed into the PAL blocks of the MACH device. While this procedure is handled automatically by the software, the software can also accept manual direction based upon the user's working knowledge of the design. The overall device utilization provided by the Fitter will vary from design to design, but a utilization target of no greater than 70% is recommended. Since a design must be entered and fit in order to calculate actual utilization, it is best to be conservative when estimating utilization before starting a design.

AMD recommends letting the software decide the best fit and pin placement automatically for the first iteration of the design. This will provide the best chance of fitting. With this approach, large designs can be implemented incrementally, starting with low device utilization and building up by adding logic until the device is full. This generally means that designs are done without any specific pinout assignments, with the final pinout decided by the software. While it is possible to pre-place signals, it is not recommended in most cases. If done carefully, pre-placement can help the software fit difficult designs; if not done carefully, it may make it harder for the design to fit. Guidelines on specifying the initial pinout are provided in the MACH Technical Briefs book.

Once an initial design fits, there may be subsequent changes to the design. This is important if board layout has already started based on the original pinout. Design changes make it necessary to refit the design, which may result in a different pinout. Some design changes may make it impossible to refit the design, regardless of the pinout. The stability of the design and the expected extent of any changes should therefore be considered before committing the design to layout. Careful designs that target about 70% utilization will make future changes much easier. Higher utilization will make design changes much more difficult to implement. Hints on designing for change can be found in the *MACH Device Design Planning Guide* near the end of this book, and in the article *Designing for Change with MACH Devices* in the Technical Briefs book.

In all cases, the way the design is partitioned and placed into the MACH device by the software does not affect the performance of the design. With designs that do not fit, it is possible to make some performance tradeoffs to aid in fitting (for example, by optimizing the flip-flop type or using multi-level logic), but those tradeoffs must be specifically requested, and any additional delays are entirely predictable.

Synchronous MACH Devices

Advanced Micro Devices

SYNCHRONOUS MACH DEVICES

The MACH 1 and MACH 2 families of synchronous devices each consist of several members. The items that differentiate the members of the family are the number of pins, the number of macrocells, the amount of interconnect, and the number of clocks. The MACH 1 family has output macrocells; the MACH 2 family has output and buried macrocells. In all other respects, the two families are the same.

This provides a convenient way of migrating designs up or down with little difficulty. Because there is a choice of I/O-pin-to-macrocell ratio, the designer can choose a device that suits both his internal logic needs and his I/O needs.

The devices range in pin count from 44 to 84, and in number of macrocells from 32 to 128. All devices are provided in cost-effective PLCC packages; military versions are available in CQFP packages.

Functional Description

The fundamental architecture of the MACH devices consists of several PAL blocks interconnected by a switch matrix. The switch matrix allows communication between PAL blocks, and routes inputs to the PAL blocks. Together the PAL blocks and switch matrix allow the logic designer to create large designs in a single device instead of multiple devices.

Most pins are I/O pins that can be used as inputs, outputs, or bidirectional pins. There are some dedicated input pins, but all macrocells have internal feedback, allowing the pin to be used as an input if the macrocell signal is not needed externally.

The key to being able to make effective use of these devices lies in the interconnect schemes used. Because of the use of programmable interconnections, the product-term arrays have been decoupled from the switch matrix, the macrocells, and the I/O pins. This provides much greater flexibility, and allows designs to be placed and routed efficiently and quickly.

The internal architecture is such that all signals incur the same delays, regardless of routing. This means that the performance of a design is design-independent, and is known before the design is even begun.

The PAL Blocks

The PAL blocks can be viewed as independent PAL devices on the chip. This provides for logic functions that need the complete interconnect that a PAL device provides. The PAL blocks communicate with each other only through the switch matrix.

Each PAL block contains a product-term array, a logic allocator, macrocells, and I/O cells. The product-term array generates the basic logic, although the number of product terms per macrocell is variable. The logic allocator distributes the product terms to the macrocells. This allows the distribution of product terms as required by the design. The macrocell configures the signal, and the I/O cell delivers the final signal to the output pin.

Each PAL block additionally contains an asynchronous reset product term and an asynchronous preset product term. This allows the flip-flops within a single PAL block to be initialized as a bank. There are also several three-state product terms that provide three-state control to the I/O cells.

The Switch Matrix

The switch matrix takes all dedicated inputs, I/O feedback signals, and buried feedback signals and routes them as needed to the various PAL blocks. Feedback signals that only return to the same PAL block still go through the switch matrix. This provides a way for the PAL blocks to communicate with each other with consistent, predictable delays. It is the switch matrix which makes the MACH devices more than just multiple PAL devices on a single chip.

For designs that consist of smaller functional units that are connected together, the PAL blocks provide the routing software with local full connectivity for each unit, connected by the switch matrix. For designs that are larger in scope, the switch matrix allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into the PAL blocks through the switch matrix so that the designer does not have to be concerned with the internal organization.

The Product-Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the switch matrix (Table 1), and are provided in both true and complement forms for efficient logic implementation.

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Table 1. PAL Block Inputs

Device	Number of Inputs to PAL Block
MACH110	22
MACH120	26
MACH130	26
MACH210	22
MACH220	26
MACH230	26

Because the number of product terms allocated to each macrocell is not fixed, the full sum of products is not realized in the array. The product terms drive the logic allocator, which allocates the product terms to the appropriate macrocells.

The Logic Allocator

The logic allocator (Figure 2) is a block within which different product terms are allocated to the appropriate macrocells in groups of four product terms called "product term clusters". The availability and distribution of product term clusters is automatically considered by the software as it places and routes functions within the PAL block. The size of the product term clusters has been designed to provide high utilization of product terms. Complex functions using many product terms are possible. Yet when functions use few product terms, there will be a minimal number of unused–or wasted–product terms left over.

The product term clusters do not "wrap" around the logic block. This means that the macrocells at the ends of the block have fewer product terms available. Please refer to the individual product data sheets for details.

The Macrocell

There are two fundamental types of macrocell: the output macrocell and the buried macrocell. The buried macrocell is only found in MACH 2 devices. The use of buried macrocells effectively doubles the number of macrocells available without increasing the pin count.

Both macrocell types can generate registered or combinatorial outputs. For the MACH 2 series, a transparent-low latched configuration is provided. If used, the register can be configured as a T-type or a D-type flip-flop. Register and latch functionality is defined in Table 2. Programmable polarity (for output macrocells) and the T-type flip-flop both give the software a way to minimize the number of product terms needed. These choices can be made automatically by the software when it fits the design into the device.

Table 2. Register/Latch Operation

Configuration	D/T	CLK/LE	Q+
D-Register	X	0, 1, ↓	Q
	0	↑	0
	1	↑	1
T-Register	X	0,1, ↓	Q
	0	↑	Q
	1	↑	$\overline{Q}$
Latch	0	0	0
	1	0	1
	0	1	Q
	1	1	Q

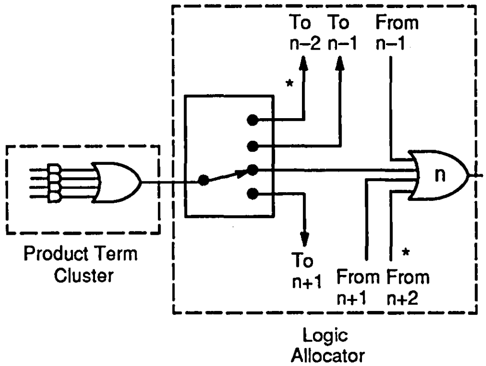
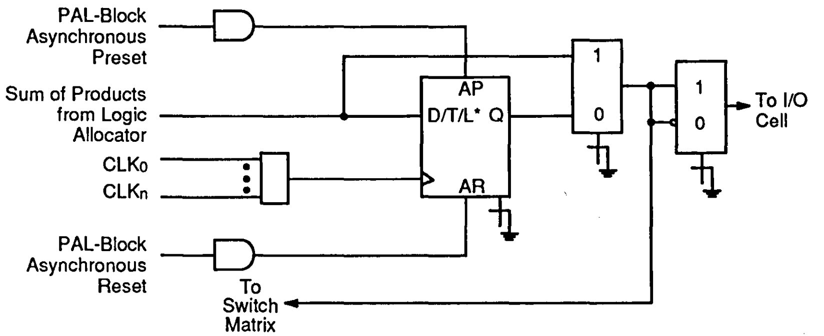


Figure 2. Product Term Clusters and the Logic Allocator



* Latch option available on MACH 2 devices only.

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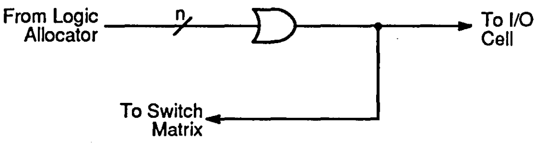
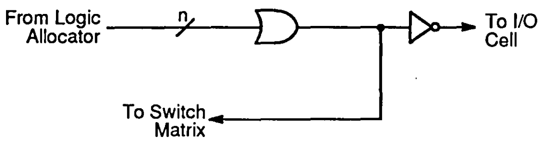
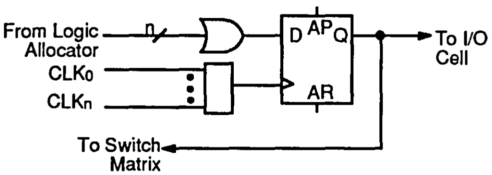
Figure 3. Output Macrocell



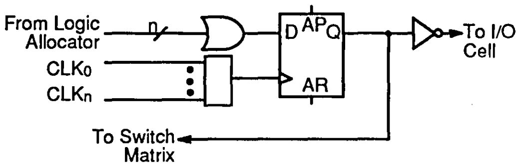
a. Combinatorial, Active High



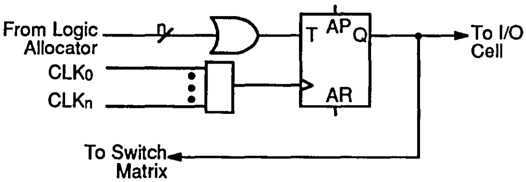
b. Combinatorial, Active Low



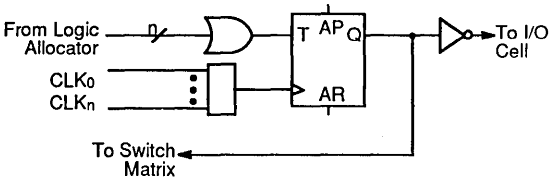
c. D-type Register, Active High



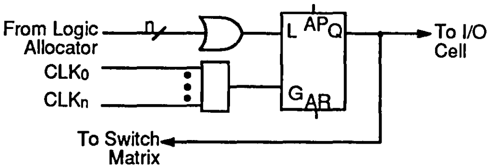
d. D-type Register, Active Low



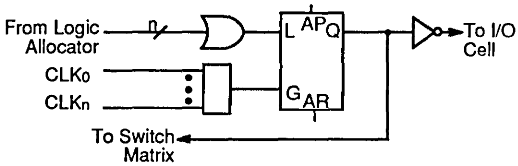
e. T-type Register, Active High



f. T-type Register, Active Low



g. Latch, Active High (MACH 2 only)



h. Latch, Active Low (MACH 2 only)

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Figure 4. Output Macrocell Configurations

The output macrocell (Figure 3) sends its output back to the switch matrix, via internal feedback, and to the I/O cell. The feedback is always available regardless of the configuration of the I/O cell. This allows for buried combinatorial or registered functions, freeing up the I/O pins for use as inputs if not needed as outputs. The basic output macrocell configurations are shown in Figure 4.

The buried macrocell (Figure 5) does not send its output to an I/O cell. The output of a buried macrocell is provided only as an internal feedback signal which feeds the switch matrix. This allows the designer to generate additional logic without requiring additional pins.

In addition to the capabilities of the output macrocell, the buried macrocell allows the use of registered or latched inputs. The input register is a D-type flip-flop; the input latch is a transparent-low D-type latch. Once configured as a registered or latched input, the buried macrocell cannot generate logic from the product-term array. The basic buried macrocell configurations are shown in Figure 6.

The flip-flops in either macrocell type can be clocked by one of several clock pins (Table 3). Registers are clocked on the rising edge of the clock input. Latches hold their data when the gate input is HIGH. Clock pins are also available as inputs, although care must be taken when a signal acts as both clock and input to the same device.

Table 3. Macrocell Clocks

Device	Number of Clocks Available
MACH110	2
MACH120	4
MACH130	4
MACH210	2
MACH220	4
MACH230	4

All flip-flops have asynchronous reset and preset. This is controlled by the common product terms that control all flip-flops within a PAL block. For a single PAL block, all flip-flops, whether in an output or a buried macrocell, are initialized together. The functionality of the flip-flops with respect to initialization is illustrated in Table 4.

Table 4. Asynchronous Reset/Preset Operation

Configuration	AR	AP	CLK/LE	Q+
Register	0	0	X	See Table 2
	0	1	X	1
	1	0	X	0
	1	1	X	0
Latch	0	0	X	See Table 2
	0	1	0	Illegal
	0	1	1	1
	1	0	0	Illegal
	1	0	1	0
	1	1	0	Illegal
	1	1	1	0

The I/O Cell

The I/O cell (Figure 7) provides a three-state output buffer. The three-state buffer can be left permanently enabled, for use only as an output; permanently disabled, for use as an input; or it can be controlled by one of two product terms, for bidirectional signals and bus connections. The two product terms provided are common to a bank of I/O cells.

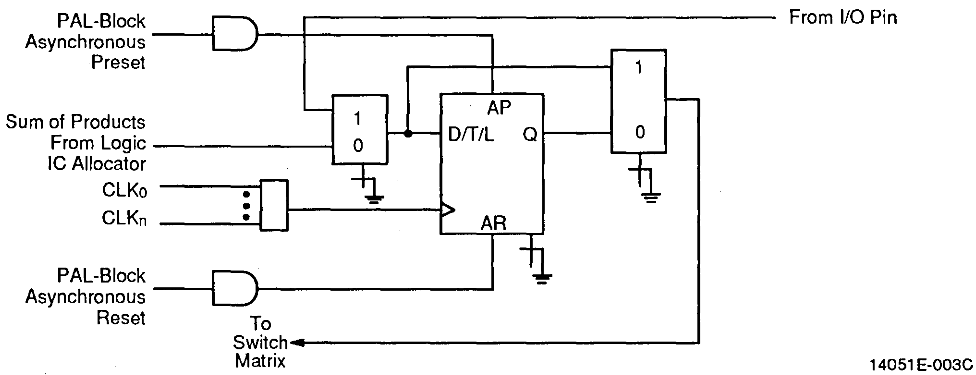

Figure 5. Buried Macrocell (MACH 2 only)

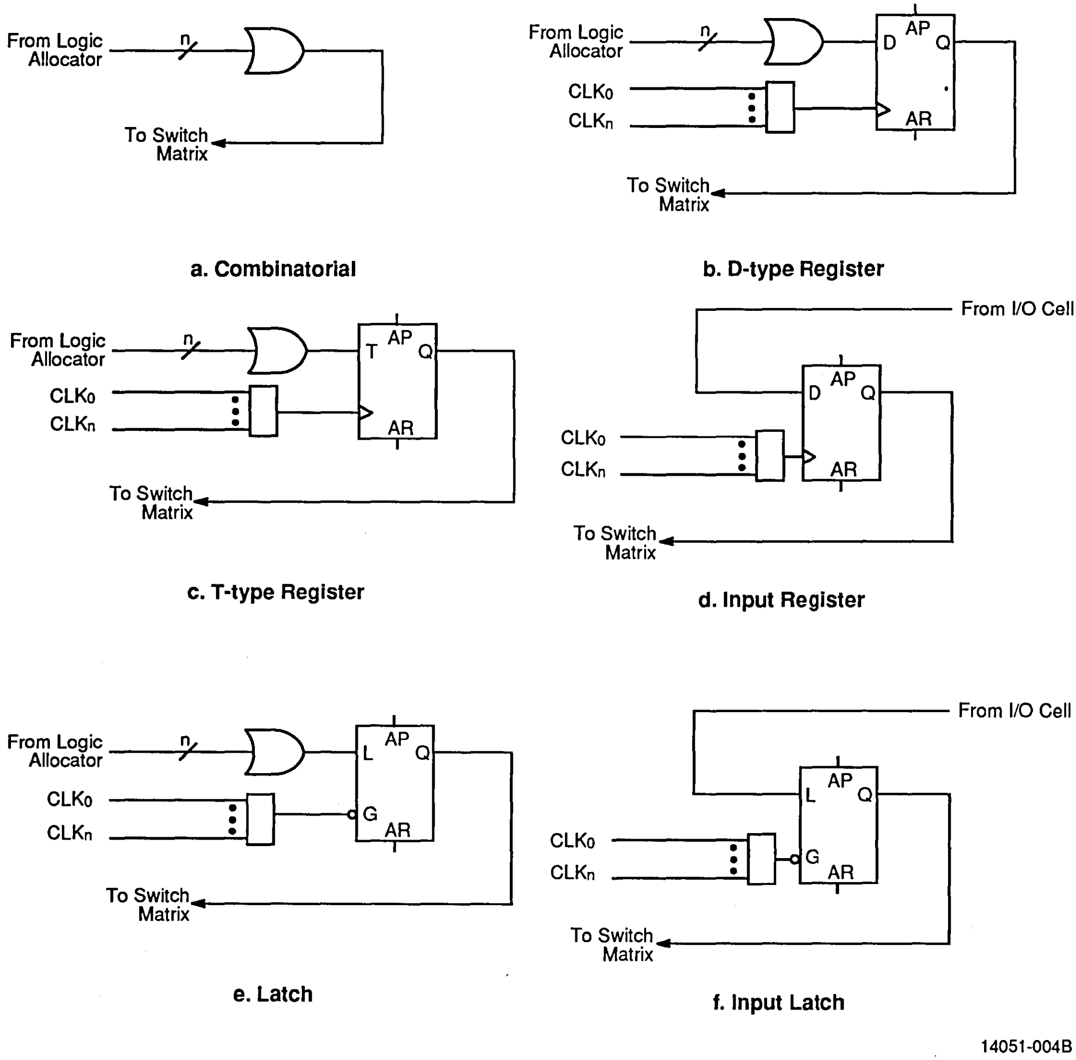

Figure 6. Buried Macrocell Configurations (MACH 2 only)

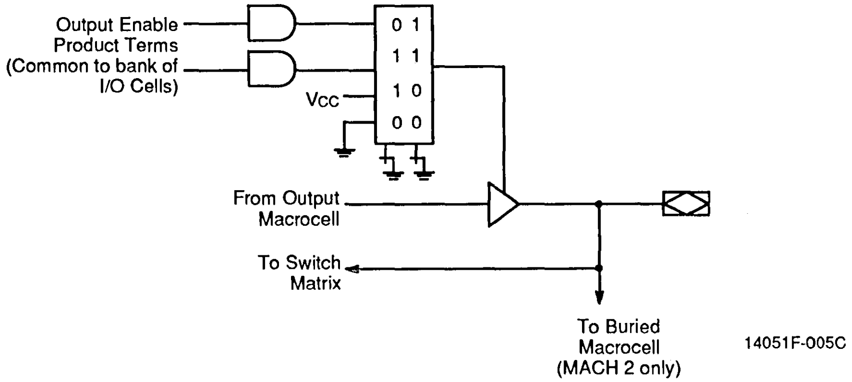

Figure 7. I/O Cell

Register Preload

All registers on the MACH devices can be preloaded from the I/O pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Observability

In addition to the control offered by preload, testing requires observability of the internal state of the device following a sequence of vectors. The MACH devices offer an observability feature that allows the user to send hidden buried register values to observable output pins.

For macrocells that are configured as combinatorial, the observability function suppresses the selection of the combinatorial output by forcing the macrocell output multiplexer into registered output mode. The observability function allows observation of the associated registers by overriding the output enable control and enabling the output buffer.

Power-up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. The actual values of the outputs of the MACH devices will depend on the configuration of the macrocell. The V_{CC} rise must be monotonic and the reset delay time is 10 µs maximum.

Security Bit

A security bit is provided on the MACH devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit, but test vectors containing preload can be used independently of the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Programming and Erasing

The MACH devices can be programmed on standard logic programmers. They may also be erased to reprogram a previously configured device with a new program. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

The MACH devices offer a very high level of built-in quality. The fact that the device is erasable allows direct verification of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The MACH devices are fabricated with AMD's advanced electrically-erasable floating-gate 0.8-µm CMOS technology. This provides the devices with performance and power consumption that are unmatched in the industry. The floating gate cells rely on Fowler-Nordheim tunneling to charge the gate, and have long proven their endurance and reliability. 20-year data retention is provided over operating conditions when devices are programmed on approved programmers.

The substrate of these devices is grounded, providing for a more efficient circuit. In addition, this provides substrate clamp diodes at all inputs, making them more immune to noisy input signals.

MACH110-12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 44 Pins
- 32 Macrocells
- 12 ns t_{PD} Commercial
  20 ns t_{PD} Military
- 66.7 MHz f_{MAX} Commercial
  40 MHz f_{MAX} Military
- 38 Inputs
- 32 Outputs
- 32 Flip-Flops; 2 clock choices
- 2 "PAL22V16" Blocks
- Pin-compatible with MACH210
- MASC110 for high-volume applications

GENERAL DESCRIPTION

The MACH110 is a member of AMD's high-performance EE CMOS MACH 1 family. This device has approximately three times the logic macrocell capability of the popular PAL22V10 at an equal speed with a lower cost per macrocell.

The MACH110 consists of two PAL blocks interconnected by a programmable switch matrix. The two PAL blocks are essentially "PAL22V16" structures complete with product-term arrays and programmable macrocells. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH110 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

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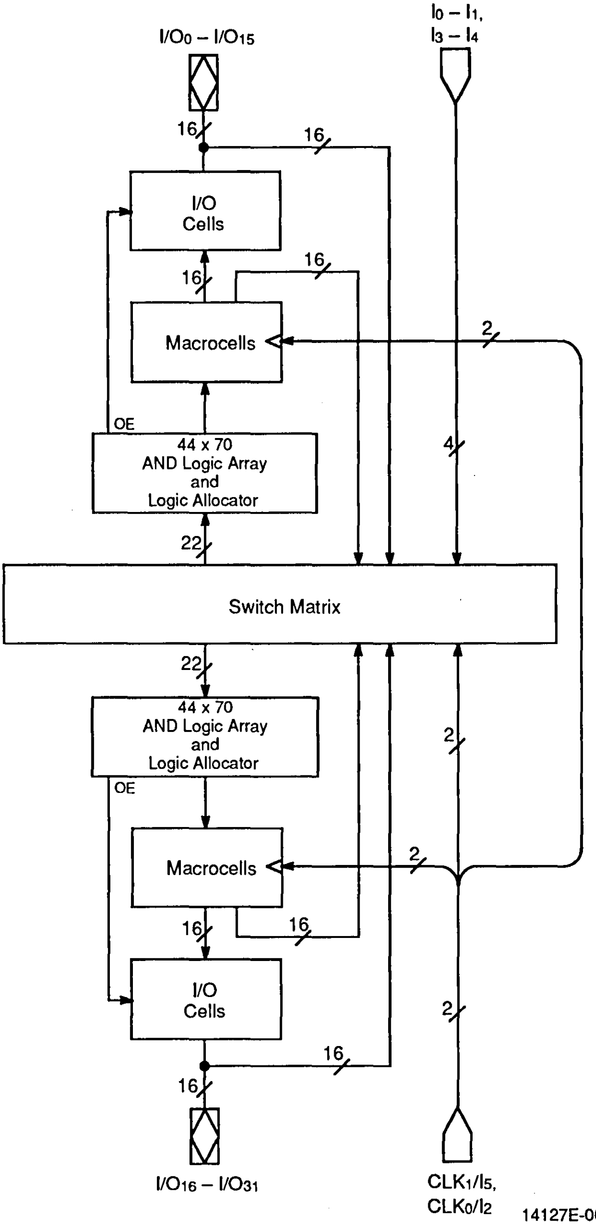
BLOCK DIAGRAM



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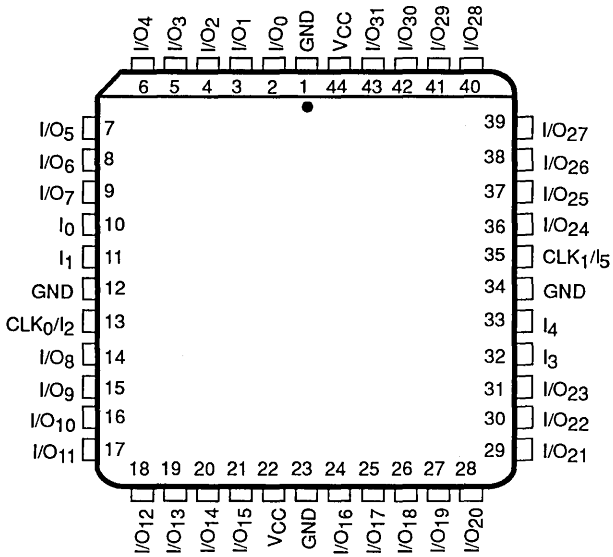
CONNECTION DIAGRAM
Top View

PLCC/CQFP



Pin Designations

CLK/I	Clock or Input
GND	Ground
I	Input
I/O	Input/Output
V_{CC}	Supply Voltage

14127-002A

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

MACH 110 -12 J C

FAMILY TYPE
MACH = Macro Array CMOS High-Speed
MASC = MACH Architecture Superior Cost

DEVICE NUMBER
110 = 32 Macrocells, 44 Pins

SPEED
-12 = 12 ns t_{PD}
-15 = 15 ns t_{PD}
-20 = 20 ns t_{PD}

OPTIONAL PROCESSING
Blank = Standard Processing

OPERATING CONDITIONS
C = Commercial (0°C to +75°C)

PACKAGE TYPE
J = 44-Pin Plastic Leaded Chip Carrier (PL 044)

Valid Combinations	
MACH110-12	JC
MACH110-15	JC
MACH110-20	JC
MASC110-15	JC
MASC110-20	JC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION
APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Product List) products are fully compliant with MIL–STD–883 requirements. The order number (Valid Combination) is formed by a combination of:

MACH 110 -20 /B X A

OPTIONAL PROCESSING
MACH = Macro Array CMOS High-Speed

DEVICE NUMBER
110 = 32 Macrocells, 44 Pins

SPEED
-20 = 20 ns t_{PD}

LEAD FINISH
A = Hot Solder Dip

PACKAGE TYPE
X = 44-Pin Metal-Lid Ceramic Quad Flatpack (CFT044)

DEVICE CLASS
/B = Class B

Valid Combinations
MACH110-20/BXA

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

FUNCTIONAL DESCRIPTION

The MACH110 consists of two PAL blocks connected by a switch matrix. There are 32 I/O pins and 6 dedicated input pins feeding the switch matrix. These signals are distributed to the two PAL blocks for efficient design implementation. There are two clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH110 (Figure 8) contains a 64-product-term logic array, a logic allocator, 16 macrocells and 16 I/O cells. The switch matrix feeds each PAL block with 22 inputs. This makes the PAL block look effectively like an independent "PAL22V16".

There are four additional output enable product terms in each PAL block. For purposes of output enable, the 16 I/O cells are divided into 2 banks of 8 macrocells. Each bank is allocated two of the output enable product terms.

An asynchronous reset product term and an asynchronous preset product term are provided for flip-flop initialization. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH110 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 16 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH110 product-term array consists of 64 product terms for logic use, and 6 special-purpose product terms. Four of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset. Two of the output enable product terms are used for the first eight I/O cells; the other two control the last eight macrocells.

The Logic Allocator

The logic allocator in the MACH110 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 12 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 5 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 8 for cluster and macrocell numbers.

Table 5. Logic Allocation

Output Macrocell	Available Clusters
M_0	C_0, C_1
M_1	C_0, C_1, C_2
M_2	C_1, C_2, C_3
M_3	C_2, C_3, C_4
M_4	C_3, C_4, C_5
M_5	C_4, C_5, C_6
M_6	C_5, C_6, C_7
M_7	C_6, C_7
M_8	C_8, C_9
M_9	C_8, C_9, C_{10}
M_{10}	C_9, C_{10}, C_{11}
M_{11}	C_{10}, C_{11}, C_{12}
M_{12}	C_{11}, C_{12}, C_{13}
M_{13}	C_{12}, C_{13}, C_{14}
M_{14}	C_{13}, C_{14}, C_{15}
M_{15}	C_{14}, C_{15}

The Macrocell

The MACH110 macrocells can be configured as either registered or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured as registered or combinatorial. The flip-flops can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of two clock pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The I/O Cell

The I/O cell in the MACH110 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to eight I/O cells. Within each PAL block, two product terms are available for selection by the first eight three-state outputs; two other product terms are available for selection by the last eight three-state outputs.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

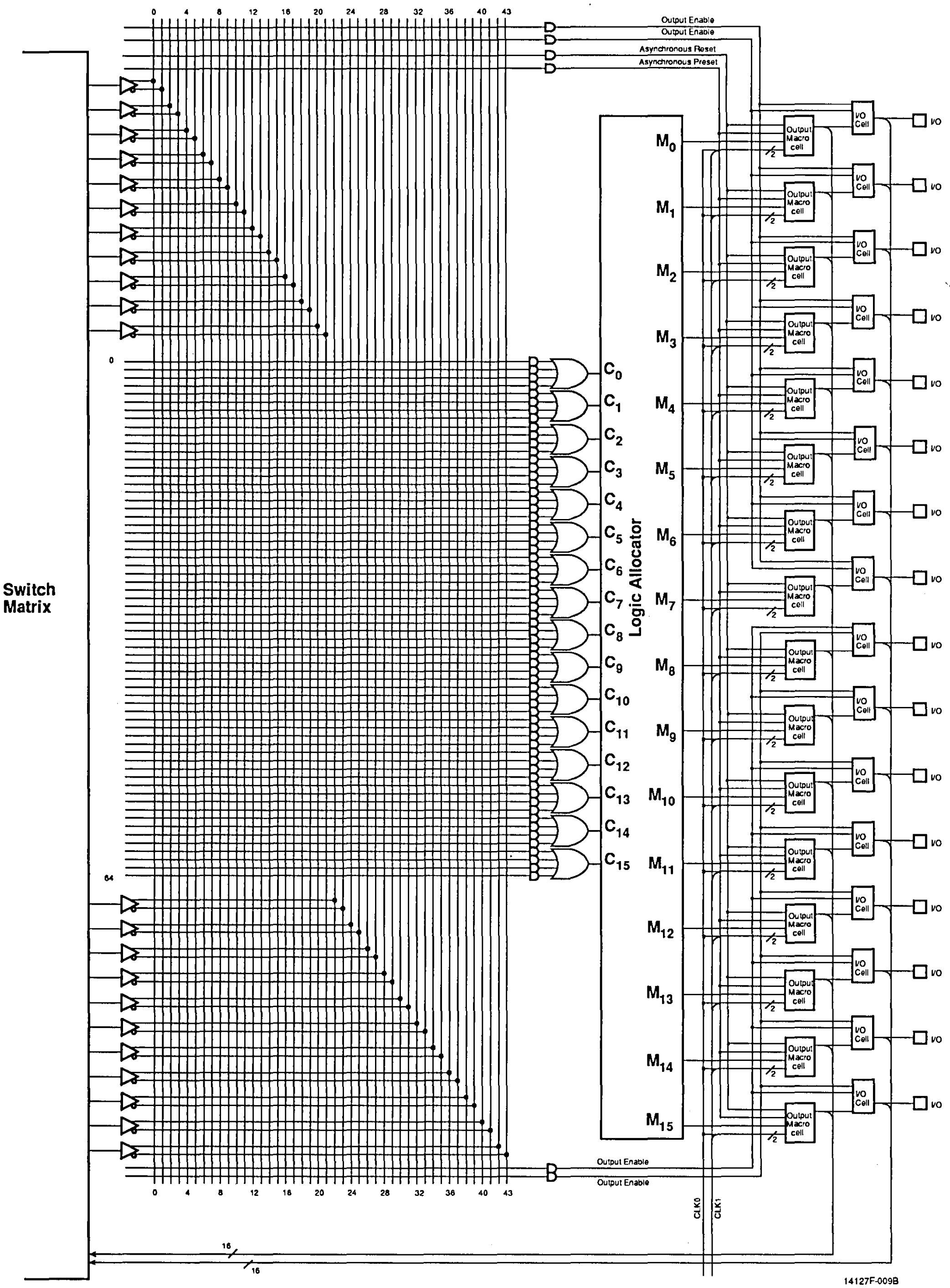


Figure 8. MACH110 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to 75°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		−10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 0 MHz		150	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-12		-15		-20		
					Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					12		15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	7		10		13		ns
				T-type	8		11		14		ns
t_H	Hold Time				0		0		0		ns
t_{CO}	Clock to Output (Note 3)					8		10		12	ns
t_{WL}	Clock Width			LOW	6		6		8		ns
t_{WH}				HIGH	6		6		8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	D-type	66.7		50		40		MHz
				T-type	62.5		47.6		38.5		MHz
		Internal Feedback (f_{CNT})		D-type	76.9		66.6		47.6		MHz
				T-type	71.4		55.5		43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		83.3		83.3		62.5		MHz
t_{AR}	Asynchronous Reset to Registered Output					16		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)				12		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)				8		10		15		ns
t_{AP}	Asynchronous Preset to Registered Output					16		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 4)				12		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 4)				8		10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)					12		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)					12		15		20	ns

Notes:

2. See Switching Test Circuit, page 112, for test conditions.
3. Parameters measured with 16 outputs switching.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_C = –55°C to +125°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	–55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C and –55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		40	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		–40	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	–30	–200	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 0 MHz		170	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	9	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

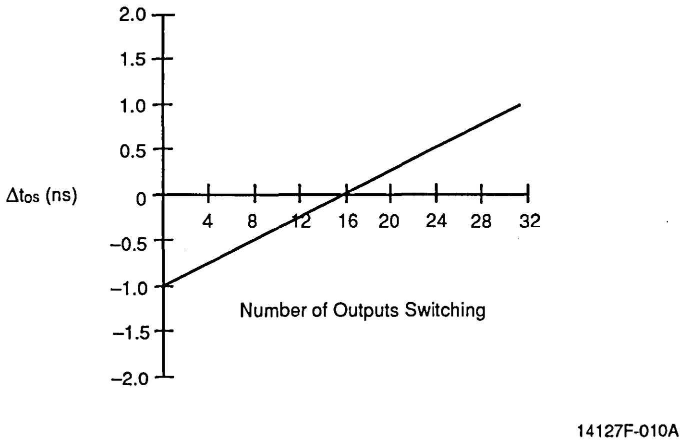
Parameter Symbol	Parameter Description				-20 Min.	-20 Max.	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	13		ns
				T-type	15		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output (Note 3)					12	ns
t_{WL}	Clock Width			LOW	8		ns
t_{WH}				HIGH	8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	D-type	40		MHz
				T-type	37		MHz
		Internal Feedback (f_{CNT})		D-type	47.6		MHz
				T-type	43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		62.5		MHz
t_{AR}	Asynchronous Reset to Registered Output					25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)				20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)				15		ns
t_{AP}	Asynchronous Preset to Registered Output					25	ns
t_{APW}	Asynchronous Preset Width (Note 4)				20		ns
t_{APR}	Asynchronous Reset Recovery Time (Note 4)				15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Notes 3, 4)					20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Notes 3, 4)					20	ns

Notes:

2. See Switching Test Circuit, page 112, for test conditions. For APL products, Group A, Subgroups 9, 10 and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Parameters measured with 16 outputs switching.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

TYPICAL SWITCHING CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C. These parameters are not tested.



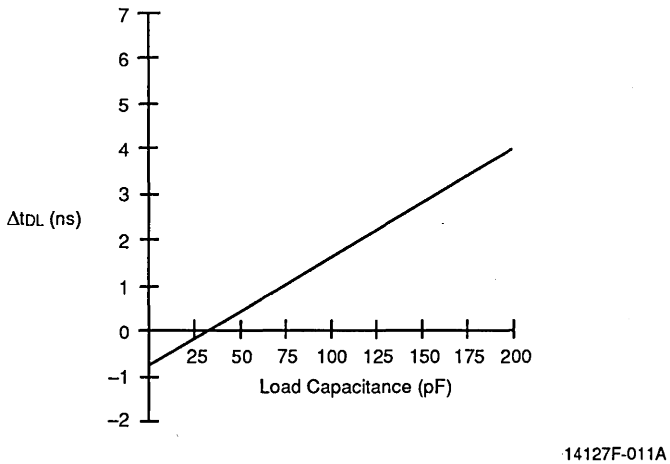
Derating for Number of Outputs Switching

Note:

Applies to t_{PD}, t_{CO}. Calculate as:

$t_{derated} = t_{16\ O/P} + \Delta t_{OS}$

Datasheet numbers ($t_{16\ O/P}$) are specified at 16 outputs switching



Capacitive Load Derating

Note:

Applies to all AC specifications and rise and fall times. Calculate as:

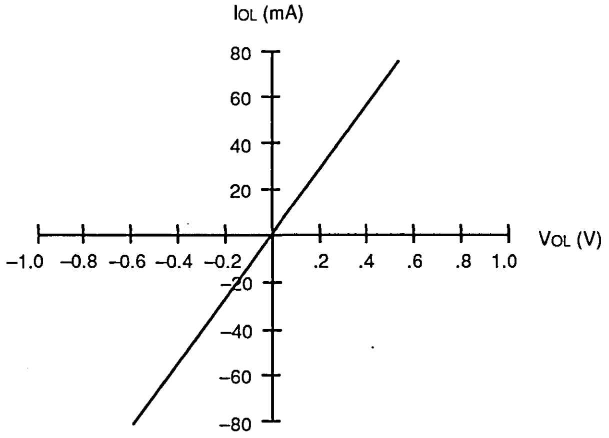
$t_{derated} = t_{35\ pF} + \Delta t_{DL}$

Datasheet numbers ($t_{35\ pF}$) are specified with 35 pF.

For typical rise and fall rates, use 1V/ns at 35 pF.

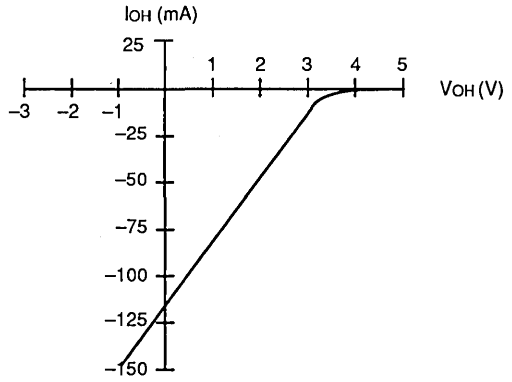
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

$V_{CC} = 5.0$ V, $T_A = 25°C$



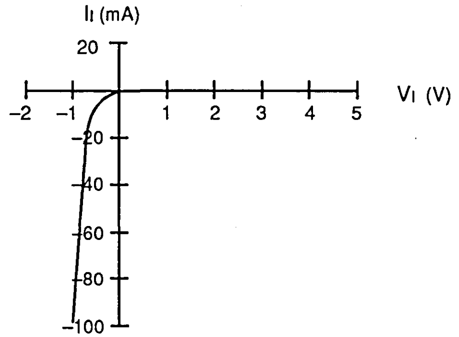
Output, LOW

14127-007A



Output, HIGH

14127-008A



14127-009A

Input

TYPICAL DYNAMIC I_{CC} CHARACTERISTICS

These parameters are not tested. Please refer to page 114 for a discussion on the usage of these parameters.

Parameter Symbol	Parameter Description	Typ.	Unit
I_{CC0}	Base static I_{CC}	90	mA
i_I	Incremental input current	15	µA/MHz
i_B	Incremental current per PAL block	13	µA/MHz
i_O	Incremental output current	90	µA/MHz
i_V	Voltage dependence	40	%/V
i_T	Temperature dependence	–0.17	%/°C

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ. PLCC	Typ. CQFP	Unit
θ_{jc}	Thermal impedance, junction to case		14	13	°C/W
θ_{ja}	Thermal impedance, junction to ambient		39	44	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	33	38	°C/W
		400 lfpm air	30	35	°C/W
		600 lfpm air	27	33	°C/W
		800 lfpm air	25	31	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

COM'L: -15/20

MACH120-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 68 Pins
- 48 Macrocells
- 15 ns t_{PD} Commercial
  20 ns t_{PD} Military
- 50 MHz f_{MAX} Commercial
  40 MHz f_{MAX} Military
- 56 Inputs
- 48 Outputs
- 48 Flip-flops; 4 clock choices
- 4 PAL blocks
- Pin-compatible with MACH220

GENERAL DESCRIPTION

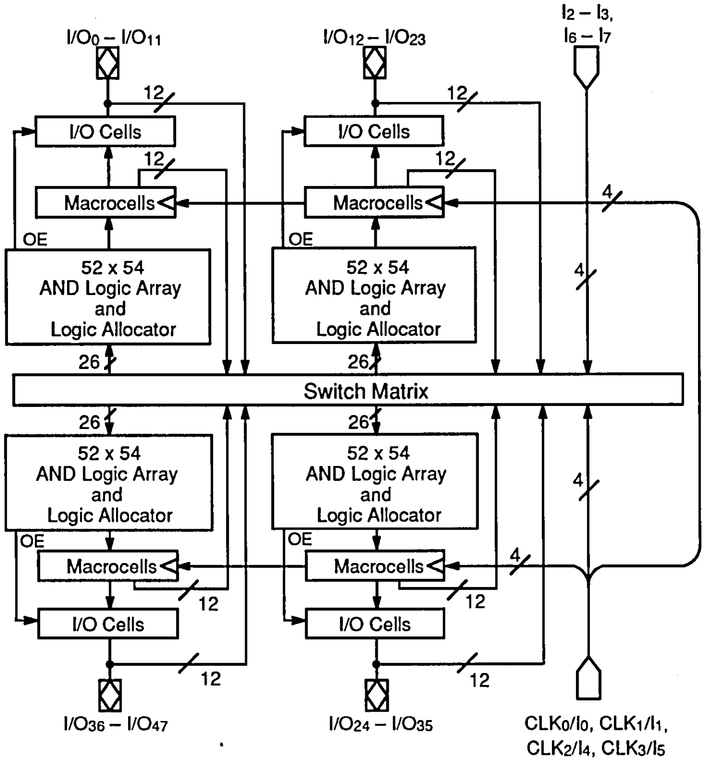
The MACH120 is a member of AMD's high-performance EE CMOS MACH 1 family. This device has approximately five times the logic macrocell capability of the popular PAL22V10 at an equal speed with a lower cost per macrocell.

The MACH120 consists of four PAL blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH120 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

Publication# 14129 Rev. F Amendment/0
Issue Date: July 1992

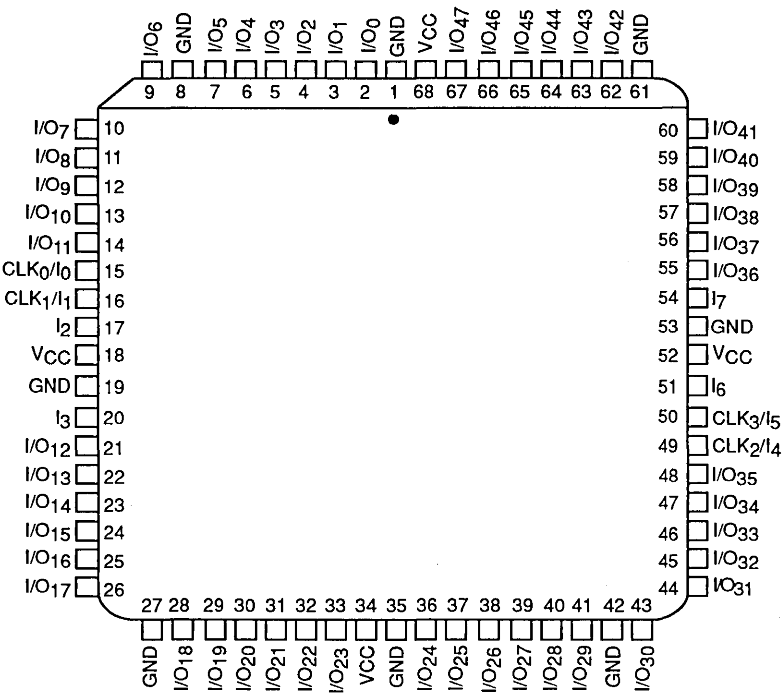
BLOCK DIAGRAM



14129D-001C

CONNECTION DIAGRAMS
Top View

PLCC



Pin Designations

CLK/I	Clock or Input
GND	Ground
I	Input
I/O	Input/Output
V_{CC}	Supply Voltage

14129D-002A

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

MACH 120 –15 J C

FAMILY TYPE
MACH = Macro Array CMOS High-Speed

DEVICE NUMBER
120 = 48 Macrocells, 68 Pins

SPEED
–15 = 15 ns t_{PD}
–20 = 20 ns t_{PD}

OPTIONAL PROCESSING
Blank = Standard Processing

OPERATING CONDITIONS
C = Commercial (0°C to +75°C)

PACKAGE TYPE
J = 68-Pin Plastic Leaded Chip Carrier (PL 068)

Valid Combinations	
MACH120-15 MACH120-20	JC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH120 consists of four PAL blocks connected by a switch matrix. There are 48 I/O pins and 4 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are 4 clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH120 (Figure 9) contains a 48-product-term logic array, a logic allocator, 12 macrocells and 12 I/O cells. The switch matrix feeds each PAL block with 26 inputs. This makes the PAL block look effectively like an independent "PAL26V12".

There are four additional output enable product terms in each PAL block. For purposes of output enable, the 12 I/O cells are divided into 2 banks of 6 macrocells. Each bank is allocated two of the output enable product terms.

An asynchronous reset product term and an asynchronous preset product term are provided for flip-flop initialization. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH120 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 12 internal feedback signals and 12 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH120 product-term array consists of 48 product terms for logic use, and 6 special-purpose product terms. Four of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset. Two of the output enable product terms are used for the first six I/O cells; the other two control the last six macrocells.

The Logic Allocator

The logic allocator in the MACH120 takes the 48 logic product terms and allocates them to the 12 macrocells as needed. Each macrocell can be driven by up to 12 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 6 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 9 for cluster and macrocell numbers.

Table 6. Logic Allocation

Output Macrocell	Available Clusters
M_0	C_0, C_1
M_1	C_0, C_1, C_2
M_2	C_1, C_2, C_3
M_3	C_2, C_3, C_4
M_4	C_3, C_4, C_5
M_5	C_4, C_5, C_6
M_6	C_5, C_6, C_7
M_7	C_6, C_7, C_8
M_8	C_7, C_8, C_9
M_9	C_8, C_9, C_{10}
M_{10}	C_9, C_{10}, C_{11}
M_{11}	C_{10}, C_{11}

The Macrocell

The MACH120 macrocells can be configured as either registered or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured as registered or combinatorial. The flip-flops can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of four global clock pins, which are also available as logic inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The I/O Cell

The I/O cell in the MACH120 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to six I/O cells. Within each PAL block, two product terms are available for selection by the first six three-state outputs; two other product terms are available for selection by the last six three-state outputs.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

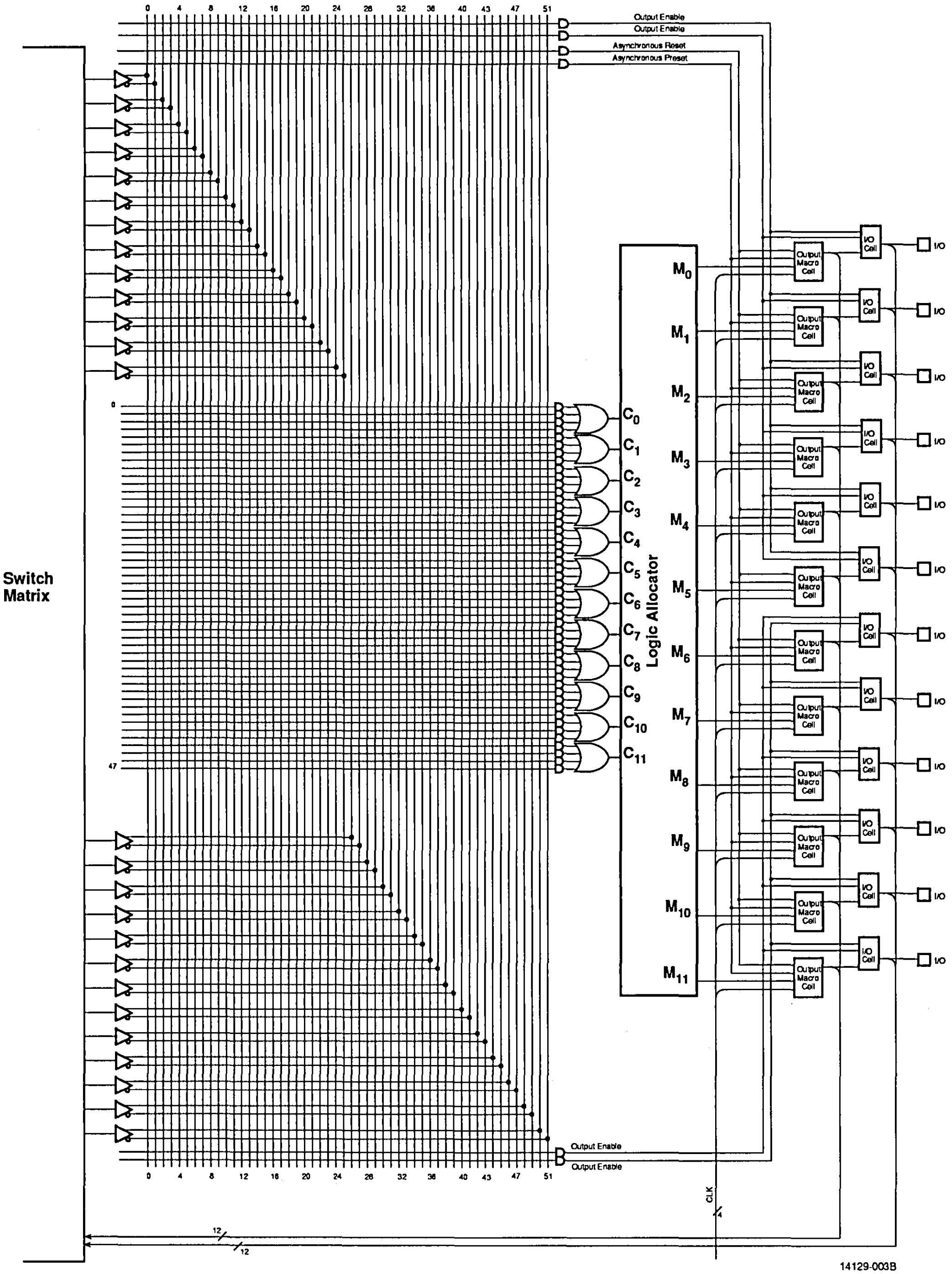


Figure 9. MACH120 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to 75°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	μA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		−10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	μA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−10	μA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 0 MHz		180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

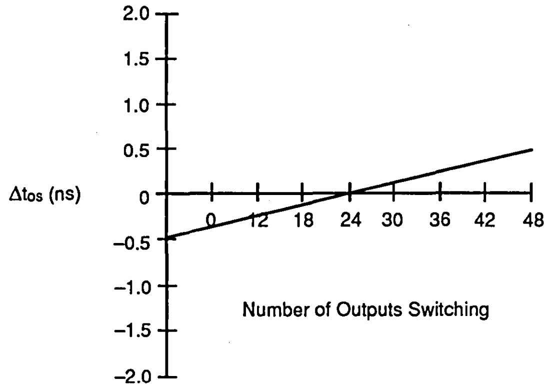
Parameter Symbol	Parameter Description		-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)			15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock	D-type	10		13		ns
		T-type	11		14		ns
t_H	Hold Time		0		0		ns
t_{CO}	Clock to Output (Note 3)			10		12	ns
t_{WL}	Clock Width	LOW	6		8		ns
t_{WH}		HIGH	6		8		ns
f_{MAX}	Maximum Frequency (Note 4): External Feedback, $1/(t_S + t_{CO})$	D-type	50		40		MHz
		T-type	47.6		38.5		MHz
	Internal Feedback (f_{CNT})	D-type	66.6		47.6		MHz
		T-type	55.5		43.5		MHz
	No Feedback, $1/(t_{WL} + t_{WH})$		83.3		62.5		MHz
t_{AR}	Asynchronous Reset to Registered Output			20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)		10		15		ns
t_{AP}	Asynchronous Preset to Registered Output			20		25	ns
t_{APW}	Asynchronous Preset Width (Note 4)		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 4)		10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)			15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)			15		20	ns

Notes:

2. See Switching Test Circuit, page 112, for test conditions.
3. Parameters measured with 24 outputs switching.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

TYPICAL SWITCHING CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C. These parameters are not tested.



14129F-004A

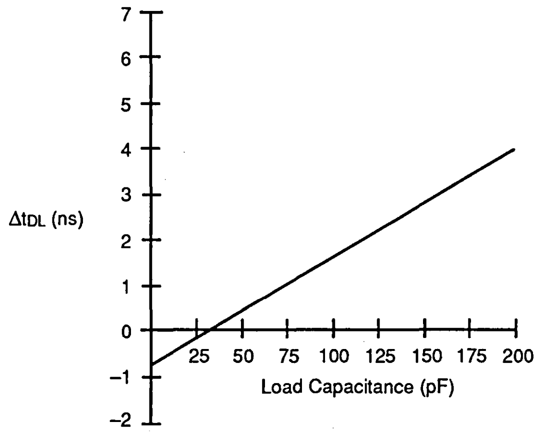
Derating for Number of Outputs Switching

Note:

Applies to t_{PD}, t_{CO}. Calculate as:

$t_{derated} = t_{24\ O/P} + \Delta t_{os}$

Datasheet numbers ($t_{16\ O/P}$) are specified at 24 outputs switching



14129F-005A

Capacitive Load Derating

Note:

Applies to all AC specifications and rise and fall times. Calculate as:

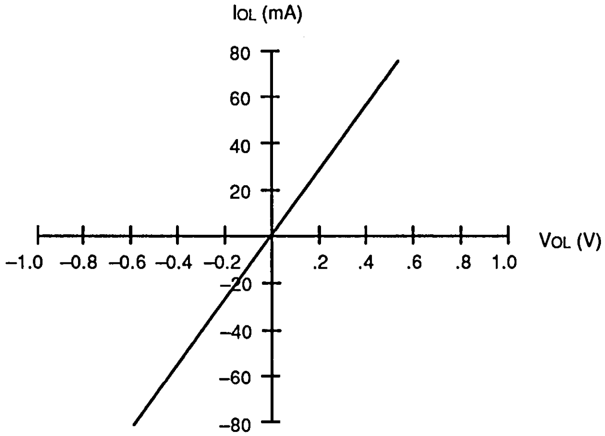
$t_{derated} = t_{35\,pF} + \Delta t_{DL}$

Datasheet numbers ($t_{35\,pF}$) are specified with 35 pF.

For typical rise and fall rates, use 1V/ns at 35 pF.

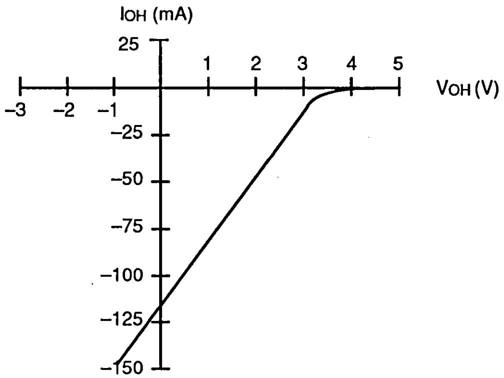
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



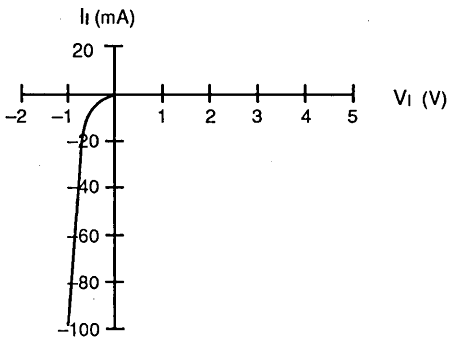
Output, LOW

14129F-006A



Output, HIGH

14129F-007A



14129F-008A

Input

TYPICAL DYNAMIC I_{CC} CHARACTERISTICS

These parameters are not tested. Please refer to page 114 for a discussion on the usage of these parameters.

Parameter Symbol	Parameter Description	Typ.	Unit
I_{CC0}	Base static I_{CC}	90	mA
i_I	Incremental input current	21	µA/MHz
i_B	Incremental current per PAL block	19	µA/MHz
i_O	Incremental output current	93	µA/MHz
i_V	Voltage dependence	41	%/V
i_T	Temperature dependence	–0.18	%/°C

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ. PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		13	°C/W
θ_{ja}	Thermal impedance, junction to ambient		37	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	33	°C/W
		400 lfpm air	30	°C/W
		600 lfpm air	28	°C/W
		800 lfpm air	25	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

COM'L: -15/20 MIL: -20

MACH130-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 84 Pins
- 64 Macrocells
- 15 ns t_{PD} Commercial
  20 ns t_{PD} Military
- 50 MHz f_{MAX} Commercial
  40 MHz f_{MAX} Military
- 70 Inputs
- 64 Outputs
- 64 Flip-flops; 4 clock choices
- 4 "PAL26V16" Blocks with buried Macrocells
- Pin-compatible with MACH230

GENERAL DESCRIPTION

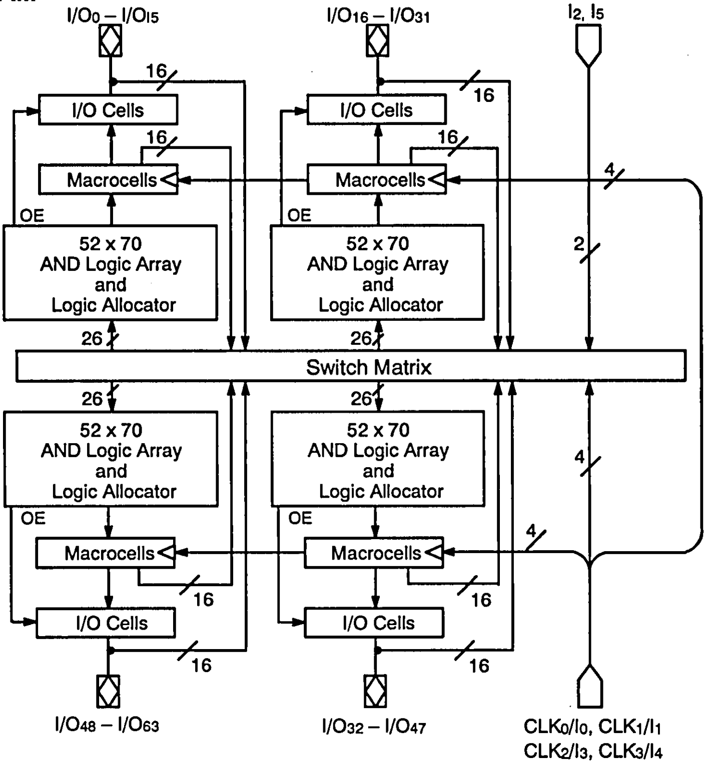
The MACH130 is a member of AMD's high-performance EE CMOS MACH 1 family. This device has approximately six times the logic macrocell capability of the popular PAL22V10 at an equal speed with a lower cost per macrocell.

The MACH130 consists of four PAL blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH130 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

Publication # 14131 Rev. E Amendment/0
Issue Date: July 1992

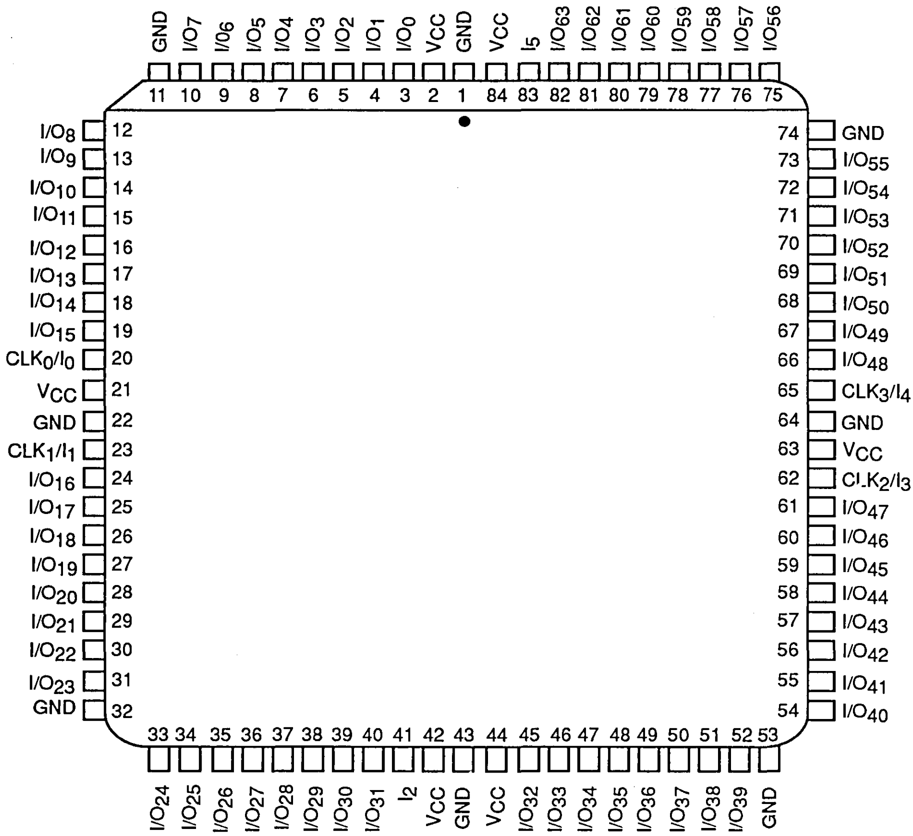
BLOCK DIAGRAM



14131D-001D

CONNECTION DIAGRAM
Top View

PLCC/CQFP



Pin Designations

CLK/I	Clock or Input
GND	Ground
I	Input
I/O	Input/Output
V_{CC}	Supply Voltage

14131D-003C

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

MACH 130 -15 J C

FAMILY TYPE
MACH = Macro Array CMOS High-Speed

DEVICE NUMBER
130 = 64 Macrocells, 84 Pins

SPEED
-15 = 15 ns t_{PD}
-20 = 20 ns t_{PD}

OPTIONAL PROCESSING
Blank = Standard Processing

OPERATING CONDITIONS
C = Commercial (0°C to +75°C)

PACKAGE TYPE
J = 84-Pin Plastic Leaded Chip Carrier (PL 084)

Valid Combinations	
MACH130-15 MACH130-20	JC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION
APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Product List) products are fully compliant with MIL–STD–883 requirements. The order number (Valid Combination) is formed by a combination of:

MACH 130 -20 /B X A

OPTIONAL PROCESSING
MACH = Macro Array CMOS High-Speed

DEVICE NUMBER
130 = 64 Macrocells, 84 Pins

SPEED
-20 = 20 ns t_{PD}

LEAD FINISH
A = Hot Solder Dip

PACKAGE TYPE
X = 84-Pin Metal-Lid Ceramic Quad Flatpack (CFT084)

DEVICE CLASS
/B = Class B

Valid Combinations
MACH130-20/BXA

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

FUNCTIONAL DESCRIPTION

The MACH130 consists of four PAL blocks connected by a switch matrix. There are 64 I/O pins and 2 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are 4 clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH130 (figure 10) contains a 64-product-term logic array, a logic allocator, 16 macrocells and 16 I/O cells. The switch matrix feeds each PAL block with 26 inputs. This makes the PAL block look effectively like an independent "PAL26V16".

There are four additional output enable product terms in each PAL block. For purposes of output enable, the 16 I/O cells are divided into 2 banks of 8 macrocells. Each bank is allocated two of the output enable product terms.

An asynchronous reset product term and an asynchronous preset product term are provided for flip-flop initialization. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH130 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 16 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH130 product-term array consists of 64 product terms for logic use, and 6 special-purpose product terms. Four of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset. Two of the output enable product terms are used for the first eight I/O cells; the other two control the last eight macrocells.

The Logic Allocator

The logic allocator in the MACH130 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 12 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 7 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 10 for cluster and macrocell numbers.

Table 7. Logic Allocation

Output Macrocell	Available Clusters
M_0	C_0, C_1
M_1	C_0, C_1, C_2
M_2	C_1, C_2, C_3
M_3	C_2, C_3, C_4
M_4	C_3, C_4, C_5
M_5	C_4, C_5, C_6
M_6	C_5, C_6, C_7
M_7	C_6, C_7, C_8
M_8	C_7, C_8, C_9
M_9	C_8, C_9, C_{10}
M_{10}	C_9, C_{10}, C_{11}
M_{11}	C_{10}, C_{11}, C_{12}
M_{12}	C_{11}, C_{12}, C_{13}
M_{13}	C_{12}, C_{13}, C_{14}
M_{14}	C_{13}, C_{14}, C_{15}
M_{15}	C_{14}, C_{15}

The Macrocell

The MACH130 macrocells can be configured as either registered or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured as registered or combinatorial. The flip-flops can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of four global clock pins, which are also available as logic inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The I/O Cell

The I/O cell in the MACH130 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to eight I/O cells. Within each PAL block, two product terms are available for selection by the first eight three-state outputs; two other product terms are available for selection by the last eight three-state outputs.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

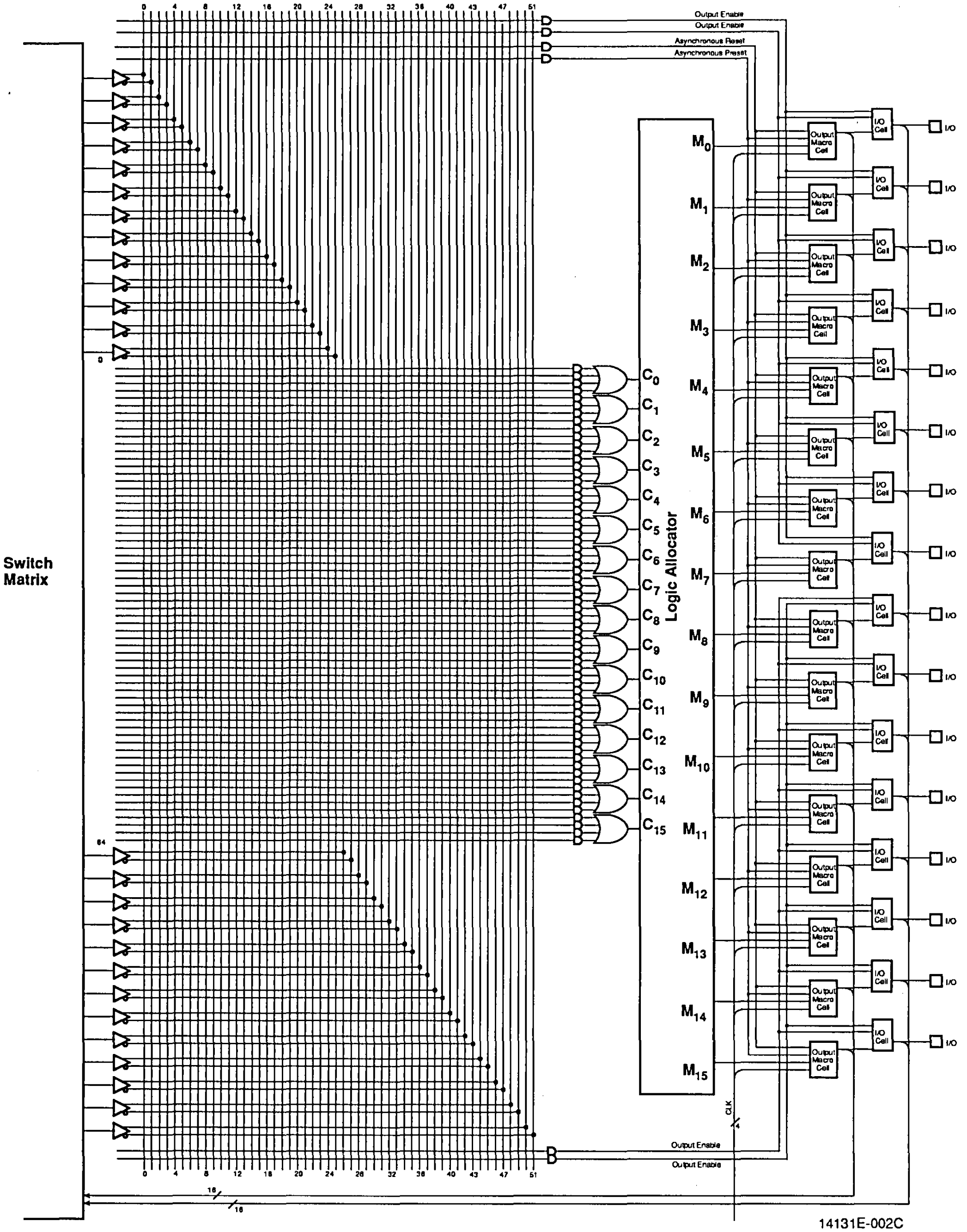


Figure 10. MACH130 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} +0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} +0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to 75°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		−10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 0 MHz		180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	10		13		ns
				T-type	11		14		ns
t_H	Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					10		12	ns
t_{WL}	Clock Width			LOW	6		8		ns
t_{WH}				HIGH	6		8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	D-type	50		40		MHz
				T-type	47.6		38.5		MHz
		Internal Feedback (f_{CNT})		D-type	66.6		47.6		MHz
				T-type	55.5		43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		83.3		62.5		MHz
t_{AR}	Asynchronous Reset to Registered Output					20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)				15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)				10		15		ns
t_{AP}	Asynchronous Preset to Registered Output					20		25	ns
t_{APW}	Asynchronous Preset Width (Note 4)				15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 4)				10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)					15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)					15		20	ns

Notes:

2. See Switching Test Circuit, page 112, for test conditions.
3. Parameters measured with 32 outputs switching.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} +0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} +0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_C = −55°C to +125°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	−55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C and −55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)		−10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		40	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		−40	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	−30	−200	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 0 MHz		220	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	9	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

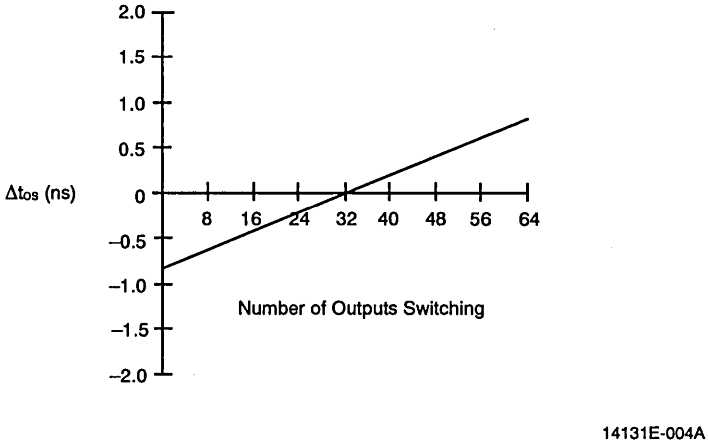
Parameter Symbol	Parameter Description				-20 Min.	-20 Max.	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	13		ns
				T-type	14		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output (Note 3)					12	ns
t_{WL}	Clock Width			LOW	8		ns
t_{WH}				HIGH	8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	D-type	40		MHz
				T-type	38.5		MHz
		Internal Feedback (f_{CNT})		D-type	47.6		MHz
				T-type	43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		62.5		MHz
t_{AR}	Asynchronous Reset to Registered Output					25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)				20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)				15		ns
t_{AP}	Asynchronous Preset to Registered Output					25	ns
t_{APW}	Asynchronous Preset Width (Note 4)				20		ns
t_{APR}	Asynchronous Reset Recovery Time (Note 4)				15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Notes 3, 4)					20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Notes 3, 4)					20	ns

Notes:

2. See Switching Test Circuit, page 112, for test conditions. For APL products, Group A, Subgroups 9, 10 and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Parameters measured with 32 outputs switching.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

TYPICAL SWITCHING CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C. These parameters are not tested.



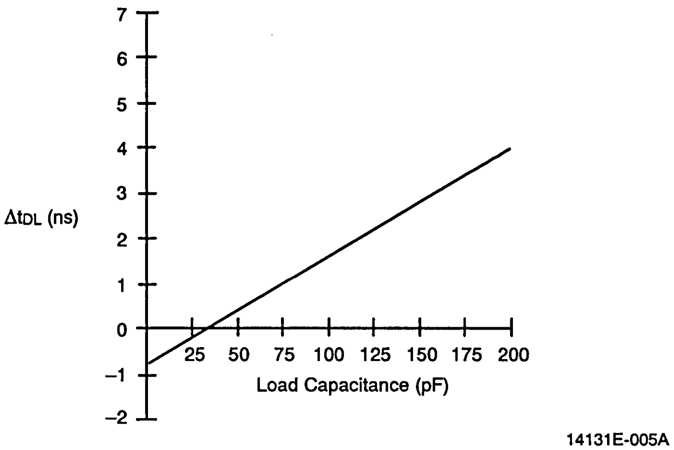
Derating for Number of Outputs Switching

Note:

Applies to t_{PD}, t_{CO}. Calculate as:

$t_{derated} = t_{32\ O/P} + \Delta t_{OS}$

Datasheet numbers ($t_{32\ O/P}$) are specified at 32 outputs switching



Capacitive Load Derating

Note:

Applies to all AC specifications and rise and fall times. Calculate as:

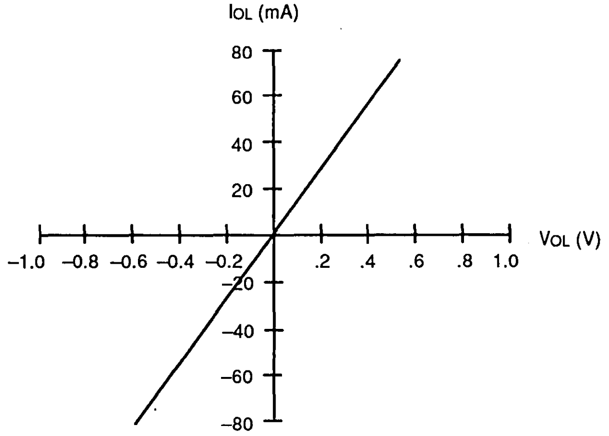
$t_{derated} = t_{35\ pF} + \Delta t_{DL}$

Datasheet numbers ($t_{35\ pF}$) are specified with 35 pF.

For typical rise and fall rates, use 1V/ns at 35 pF.

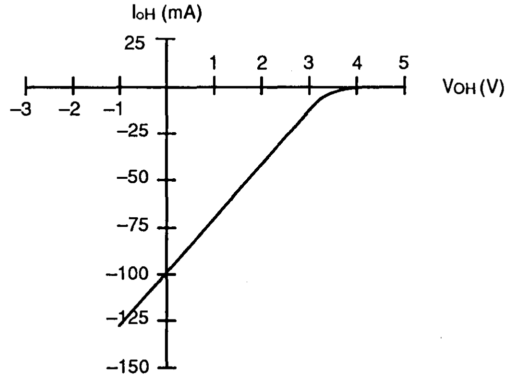
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

$V_{CC} = 5.0\ V$, $T_A = 25°C$



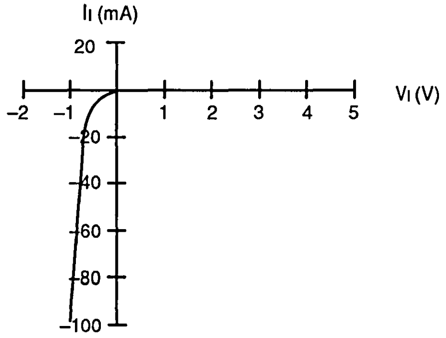
14131E-006A

Output, LOW



14131E-007A

Output, HIGH



14131E-008A

Input

TYPICAL DYNAMIC I_{CC} CHARACTERISTICS

These parameters are not tested. Please refer to page 114 for a discussion on the usage of these parameters.

Parameter Symbol	Parameter Description	Typ.	Unit
I_{CC0}	Base static I_{CC}	125	mA
i_I	Incremental input current	21	µA/MHz
i_B	Incremental current per PAL block	18	µA/MHz
i_O	Incremental output current	96	µA/MHz
i_V	Voltage dependence	40	%/V
i_T	Temperature dependence	–0.18	%/°C

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ. PLCC	Typ. CQFP	Unit
θ_{jc}	Thermal impedance, junction to case		13	x	°C/W
θ_{ja}	Thermal impedance, junction to ambient		34	x	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	30	x	°C/W
		400 lfpm air	28	x	°C/W
		600 lfpm air	26	x	°C/W
		800 lfpm air	25	x	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

MACH210-12/15/20

Advanced
Micro
Devices

High-Density EE CMOS Programmable Logic

DISTINCTIVE CHARACTERISTICS

- 44 Pins
- 64 Macrocells
- 12 ns t_{PD} Commercial
  20 ns t_{PD} Military
- 66.7 MHz f_{MAX} Commercial
  40 MHz f_{MAX} Military
- 38 Inputs
- 32 Outputs
- 64 Flip-flops; 2 clock choices
- 4 "PAL22V16" blocks with buried macrocells
- Pin-compatible with MACH110
- MASC210 for high-volume applications

GENERAL DESCRIPTION

The MACH210 is a member of AMD's high-performance EE CMOS MACH 2 device family. This device has approximately six times the logic macrocell capability of the popular PAL22V10 at an equal speed with a lower cost per macrocell.

The MACH210 consists of four PAL blocks interconnected by a programmable switch matrix. The four PAL blocks are essentially "PAL22V16" structures complete with product-term arrays and programmable macrocells, including additional buried macrocells. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH210 has two kinds of macrocell: output and buried. The MACH210 output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACH210 has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers or latches for use in synchronizing signals and reducing setup time requirements.

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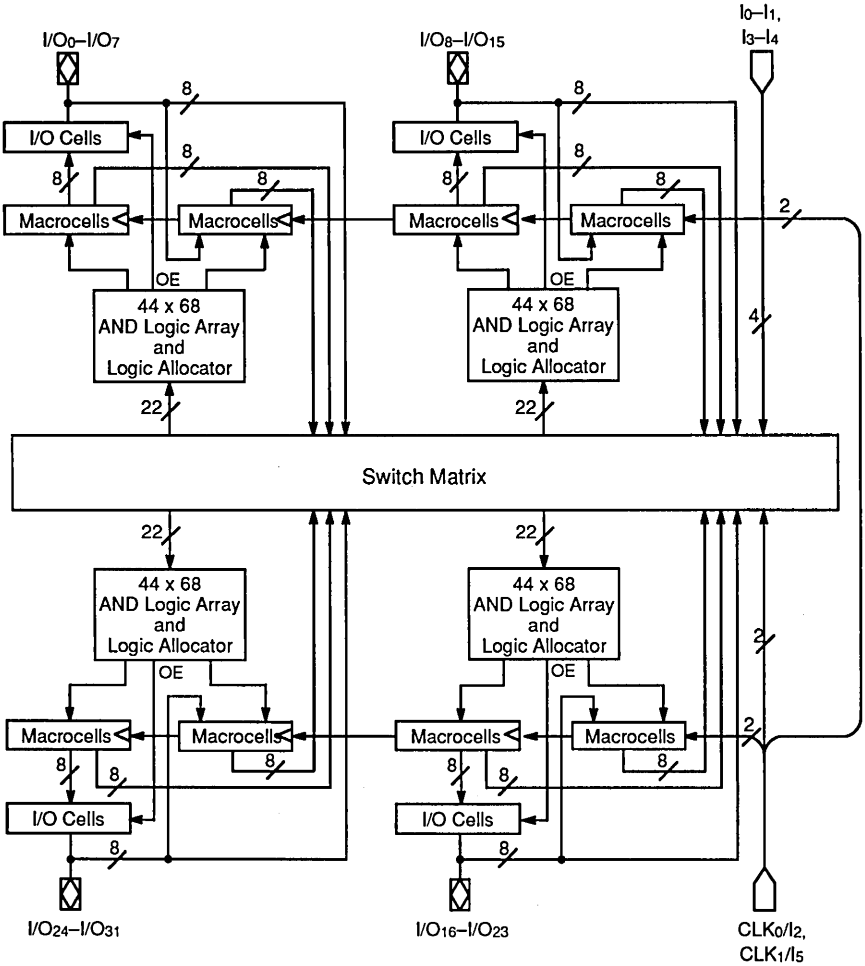
Issue Date: July 1992

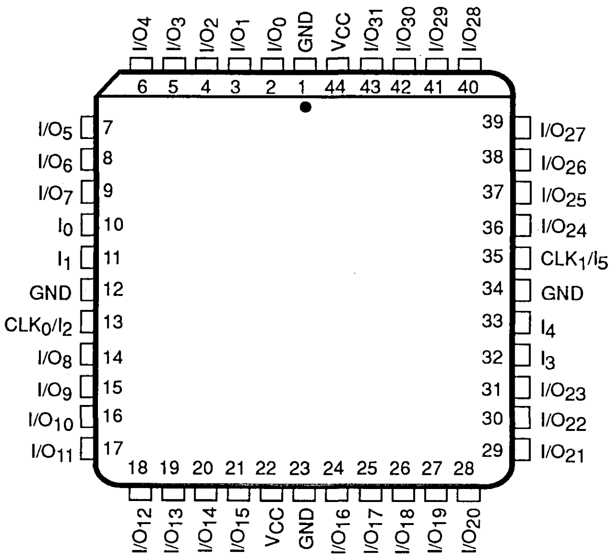
BLOCK DIAGRAM



14128E-001C

CONNECTION DIAGRAM
Top View

PLCC/CQFP



14127-002A

Pin Designations

CLK/I	Clock or Input
GND	Ground
I	Input
I/O	Input/Output
Vcc	Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

MACH 210 -12 J C

FAMILY TYPE
MACH = Macro Array CMOS High-Speed
MASC = MACH Architecture Superior Cost

DEVICE NUMBER
210 = 64 Macrocells, 44 Pins

SPEED
-12 = 12 ns t_{PD}
-15 = 15 ns t_{PD}
-20 = 20 ns t_{PD}

OPTIONAL PROCESSING
Blank = Standard Processing

OPERATING CONDITIONS
C = Commercial (0°C to +75°C)

PACKAGE TYPE
J = 44-Pin Plastic Leaded Chip Carrier (PL 044)

Valid Combinations	
MACH210-12 MACH210-15 MACH210-20	JC
MASC210-15 MASC210-20	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION
APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Product List) products are fully compliant with MIL–STD–883 requirements. The order number (Valid Combination) is formed by a combination of:

MACH 210 –20 /B X A

FAMILY TYPE
MACH = Macro Array CMOS High-Speed

DEVICE NUMBER
210 = 64 Macrocells, 44 Pins

SPEED
-20 = 20 ns t_{PD}

LEAD FINISH
A = Hot Solder Dip

PACKAGE TYPE
X = 44-Pin Metal-Lid Ceramic Quad Flatpack

DEVICE CLASS
/B = Class B

Valid Combinations
MACH210-20/BXA

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

FUNCTIONAL DESCRIPTION

The MACH210 consists of four PAL blocks connected by a switch matrix. There are 32 I/O pins and 4 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are two clock pins that can also be used as dedicated inputs. This device provides two kinds of macrocell: output macrocells and buried macrocells. This adds greater logic density without affecting the number of pins.

The PAL Blocks

Each PAL block in the MACH210 (figure 11) contains a 64-product-term logic array, a logic allocator, 8 output macrocells, 8 buried macrocells, and 8 I/O cells. The switch matrix feeds each PAL block with 22 inputs. This makes the PAL block look effectively like an independent "PAL22V16" with 8 buried macrocells.

In addition to the logic product terms, two output enable product terms, an asynchronous reset product term, and an asynchronous preset product term are provided. One of the two output enable product terms can be chosen within each I/O cell in the PAL block. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH210 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 8 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-term Array

The MACH210 product-term array consists of 64 product terms for logic use, and 4 special-purpose product terms. Two of the special-purpose product terms provide programmable output enable; one provides asynchronous reset, and one provides asynchronous preset.

The Logic Allocator

The logic allocator in the MACH210 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 16 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 8 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 11 for cluster and macrocell numbers.

Table 8. Logic Allocation

Macrocell		Available Clusters
Output	Buried	
M_0		C_0, C_1, C_2
	M_1	C_0, C_1, C_2, C_3
M_2		C_1, C_2, C_3, C_4
	M_3	C_2, C_3, C_4, C_5
M_4		C_3, C_4, C_5, C_6
	M_5	C_4, C_5, C_6, C_7
M_6		C_5, C_6, C_7, C_8
	M_7	C_6, C_7, C_8, C_9
M_8		C_7, C_8, C_9, C_{10}
	M_9	C_8, C_9, C_{10}, C_{11}
M_{10}		$C_9, C_{10}, C_{11}, C_{12}$
	M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_{12}		$C_{11}, C_{12}, C_{13}, C_{14}$
	M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_{14}		C_{13}, C_{14}, C_{15}
	M_{15}	C_{14}, C_{15}

The Macrocell

The MACH210 has two types of macrocell: output and buried. The output macrocells can be configured as either registered, latched, or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured with or without the flip-flop. The registers can be configured as D-type or T-type, allowing for product-term optimization.

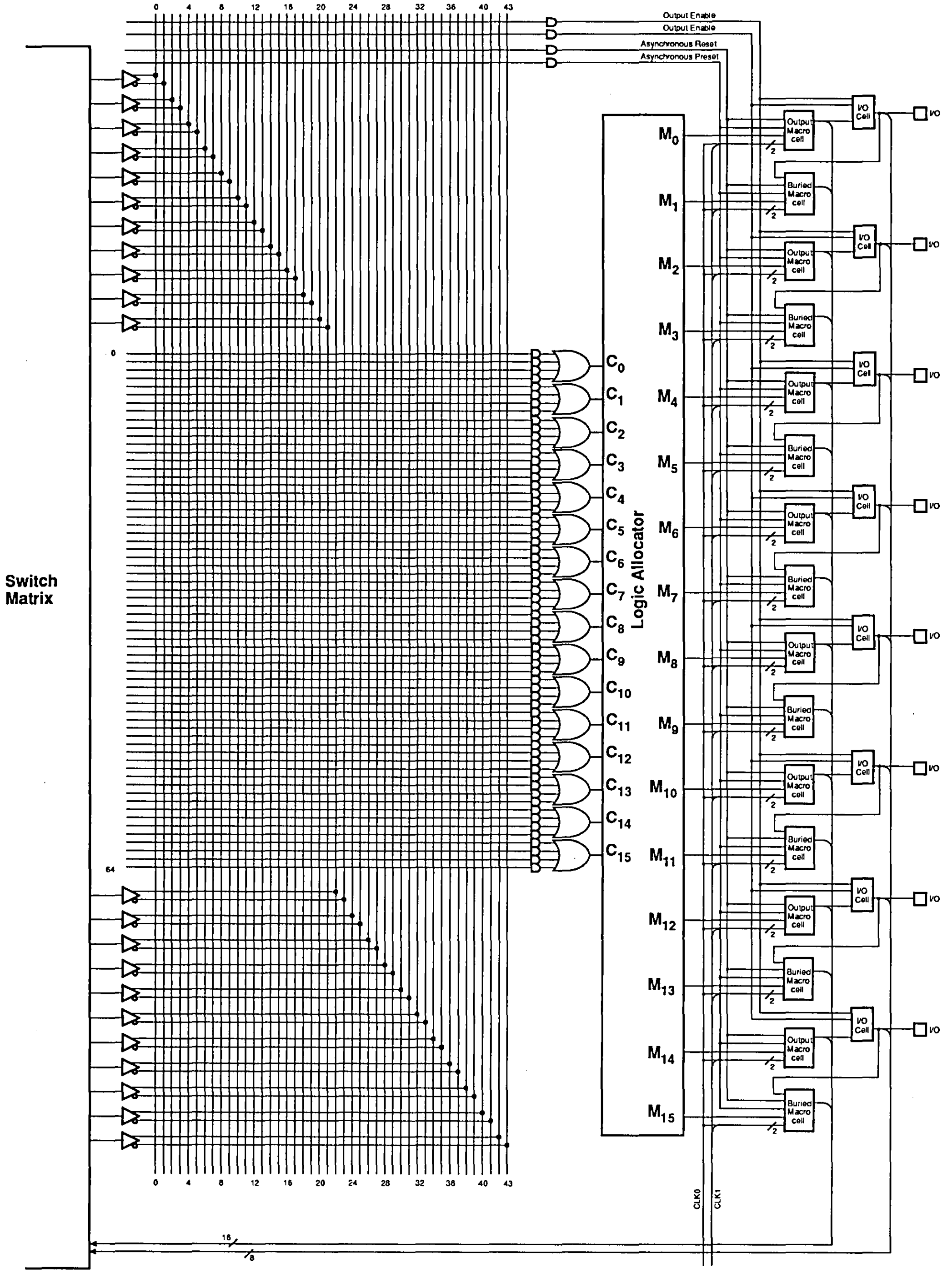
The flip-flops can individually select one of two clock/gate pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The latch holds its data when the gate input is HIGH, and is transparent when the gate input is LOW. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The buried macrocells are the same as the output macrocells if they are used for generating logic. In that case, the only thing that distinguishes them from the output macrocells is the fact that there is no I/O cell connection, and the signal is only used internally. The buried macrocell can also be configured as an input register or latch.

The I/O Cell

The I/O cell in the MACH210 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to all I/O cells in a PAL block.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.



14128F-002B

Figure 11. MACH210 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} + 0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} + 0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	μA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		−10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	μA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−10	μA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f =0 MHz		180	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-12 Min.	-12 Max.	-15 Min.	-15 Max.	-20 Min.	-20 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					12		15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	7		10		13		ns
				T-type	8		11		14		ns
t_H	Register Data Hold Time				0		0		0		ns
t_{CO}	Clock to Output (Note 3)					8		10		12	ns
t_{WL}	Clock Width			LOW	6		6		8		ns
t_{WH}				HIGH	6		6		8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	D-type	66.7		50		40		MHz
				T-type	62.5		47.6		38.5		MHz
		Internal Feedback (f_{CNT})		D-type	76.9		66.6		47.6		MHz
				T-type	71.4		55.5		43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		83.3		83.3		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				7		10		13		ns
t_{HL}	Latch Data Hold Time				0		0		0		ns
t_{GO}	Gate to Output (Note 3)					10		11		12	ns
t_{GWL}	Gate Width LOW				6		6		8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					14		17		22	ns
t_{SIR}	Input Register Setup Time				2		2		2		ns
t_{HIR}	Input Register Hold Time				2		2		2		ns
t_{ICO}	Input Register Clock to Combinatorial Output					14		17		22	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	9		12		15		ns
				T-Type	10		14		17		ns
t_{WICL}	Input Register Clock Width			LOW	6		6		8		ns
t_{WICH}				HIGH	6		6		8		ns
f_{MAXIR}	Maximum Input Register Frequency		$1/(t_{WICL} + t_{WICH})$		83.3		83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time				2		2		2		ns
t_{HIL}	Input Latch Hold Time				2		2		2		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					14		17		22	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					16		19		24	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				9		12		15		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				9		12		15		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (Continued)

Parameter Symbol	Parameter Description	-12		-15		-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WIGZ}	Input Latch Gate Width LOW	6		6		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		16		19		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		16		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)	12		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)	8		10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		16		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 4)	12		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 4)	8		10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		12		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		12		15		20	ns

Notes:

2. See Switching Test Circuit, page 112, for test conditions.
3. Parameters measured with 16 outputs switching.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} +0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} +0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_C = −55°C to +125°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	−55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C and −55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)		−10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		40	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		−40	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	−30	−200	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 0 MHz		195	mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	9	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description				-20 Min.	-20 Max.	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	13		ns
				T-type	14		ns
t_H	Register Data Hold Time				0		ns
t_{CO}	Clock to Output (Note 3)					12	ns
t_{WL}	Clock Width			LOW	8		ns
t_{WH}				HIGH	8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	D-type	40		MHz
				T-type	38.5		MHz
		Internal Feedback (f_{CNT})		D-type	47.6		MHz
				T-type	43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				13		ns
t_{HL}	Latch Data Hold Time				0		ns
t_{GO}	Gate to Output (Note 3)					12	ns
t_{GWL}	Gate Width LOW				8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					22	ns
t_{SIR}	Input Register Setup Time				2		ns
t_{HIR}	Input Register Hold Time				2		ns
t_{ICO}	Input Register Clock to Combinatorial Output					22	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	15		ns
				T-Type	17		ns
t_{WICL}	Input Register Clock Width			LOW	8		ns
t_{WICH}				HIGH	8		ns
f_{MAXIR}	Maximum Input Register Frequency (Note 4)			$1/(t_{WICL} + t_{WICH})$	62.5		MHz
t_{SIL}	Input Latch Setup Time				2		ns
t_{HIL}	Input Latch Hold Time				2		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					22	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					24	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				15		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				15		ns

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2) (Continued)

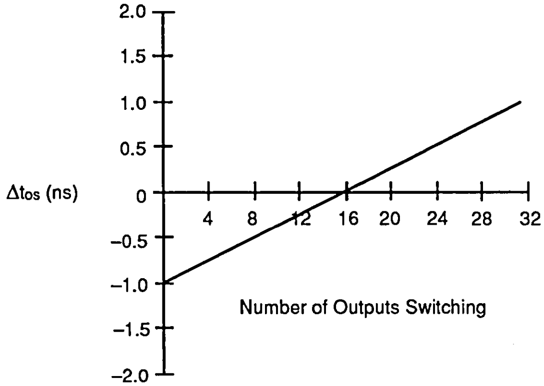
Parameter Symbol	Parameter Description	-20 Min.	-20 Max.	Unit
t_{WIGZ}	Input, Latch Gate Width LOW	8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)	20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)	15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		25	ns
t_{APW}	Asynchronous Preset Width (Note 4)	20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 4)	15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Notes 3, 4)		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Notes 3, 4)		20	ns

Notes:

2. See Switching Test Circuit, page 112, for test conditions. For APL products, Group A, Subgroups 9, 10 and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Parameters measured with 16 outputs switching.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

TYPICAL SWITCHING CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C. These parameters are not tested.



14128F-003A

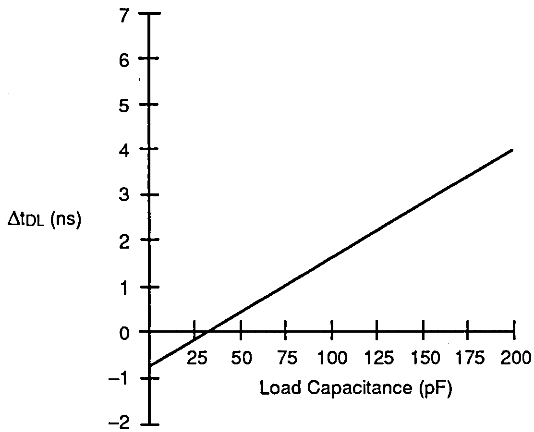
Derating for Number of Outputs Switching

Note:

Applies to t_{PD}, t_{CO} . Calculate as:

$t_{derated} = t_{16\ O/P} + \Delta t_{os}$

Datasheet numbers ($t_{16\ O/P}$) are specified at 16 outputs switching



14128F-004A

Capacitive Load Derating

Note:

Applies to all AC specifications and rise and fall times. Calculate as:

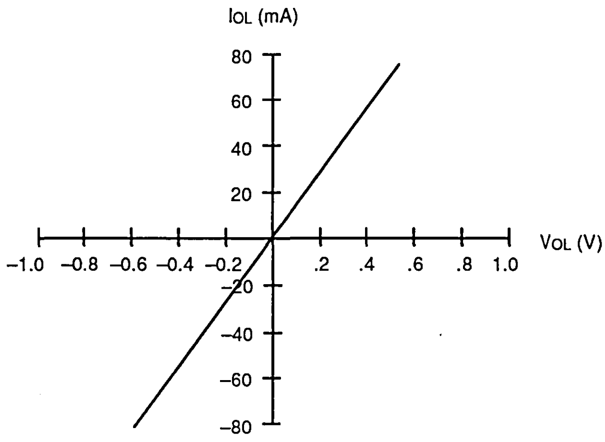
$t_{derated} = t_{35\ pF} + \Delta t_{DL}$

Datasheet numbers ($t_{35\ pF}$) are specified with 35 pF.

For typical rise and fall rates, use 1V/ns at 35 pF.

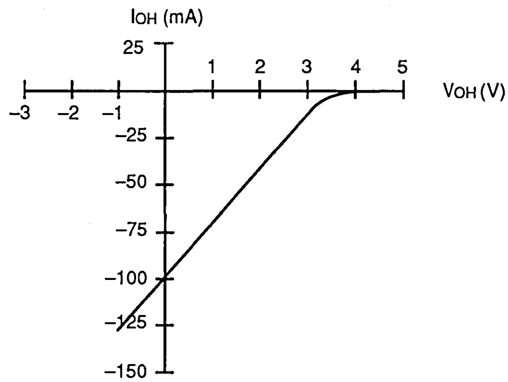
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

$V_{CC} = 5.0$ V, $T_A = 25°C$



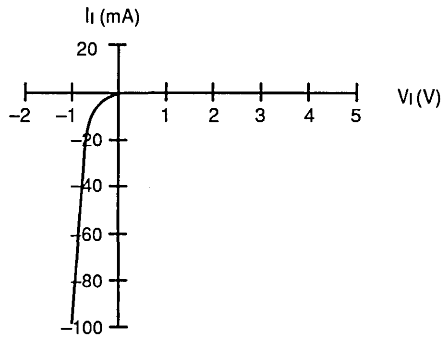
Output, LOW

14128F-005A



Output, HIGH

1412F8-006A



14128F-007A

Input

TYPICAL DYNAMIC I_{CC} CHARACTERISTICS

These parameters are not tested. Please refer to page 114 for a discussion on the usage of these parameters.

Parameter Symbol	Parameter Description	Typ.	Unit
I_{CC0}	Base static I_{CC}	125	mA
i_I	Incremental input current	21	µA/MHz
i_B	Incremental current per PAL block	18	µA/MHz
i_O	Incremental output current	96	µA/MHz
i_V	Voltage dependence	40	%/V
i_T	Temperature dependence	–0.18	%/°C

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ. PLCC	Typ. CQFP	Unit
θ_{jc}	Thermal impedance, junction to case		15	11	°C/W
θ_{ja}	Thermal impedance, junction to ambient		40	44	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	36	39	°C/W
		400 lfpm air	33	35	°C/W
		600 lfpm air	31	31	°C/W
		800 lfpm air	29	29	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

MACH220-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 68 Pins
- 96 Macrocells
- 15 ns t_{PD} Commercial
  20 ns t_{PD} Military
- 50 MHz f_{MAX} Commercial
  40 MHz f_{MAX} Military
- 56 Inputs with pull-up resistors
- 48 Outputs
- 96 Flip-flops; 4 clock choices
- 8 PAL blocks with buried macrocells
- Pin-compatible with MACH120

GENERAL DESCRIPTION

The MACH220 is a member of AMD's high-performance EE CMOS MACH 2 device family. This device has approximately nine times the logic macrocell capability of the popular PAL22V10 at an equal speed with a lower cost per macrocell.

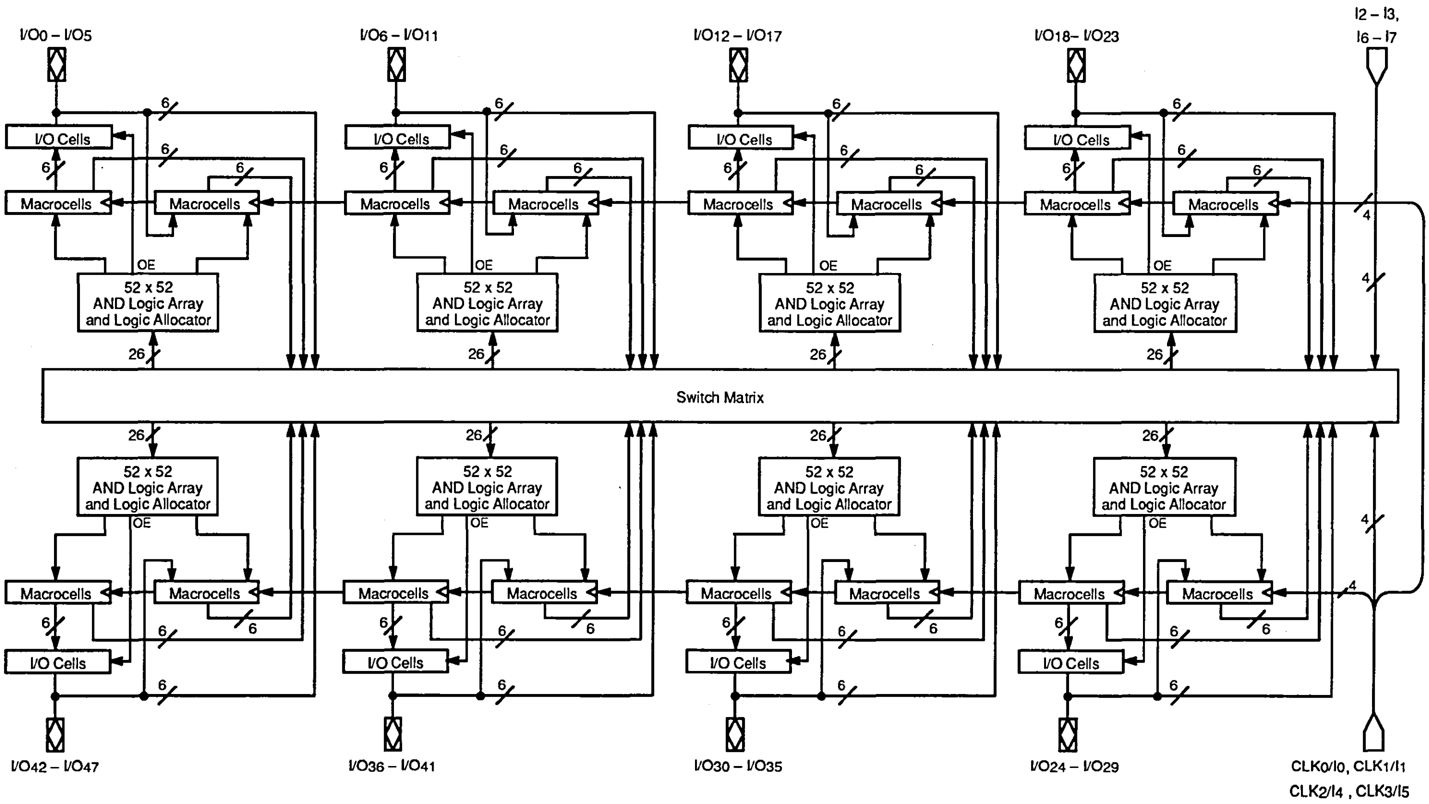
The MACH220 consists of eight PAL blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH220 has two kinds of macrocell: output and buried. The output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACH220 has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers for use in synchronizing signals and reducing setup time requirements.

Publication # 14130 Rev. F Amendment/0
Issue Date: July 1992

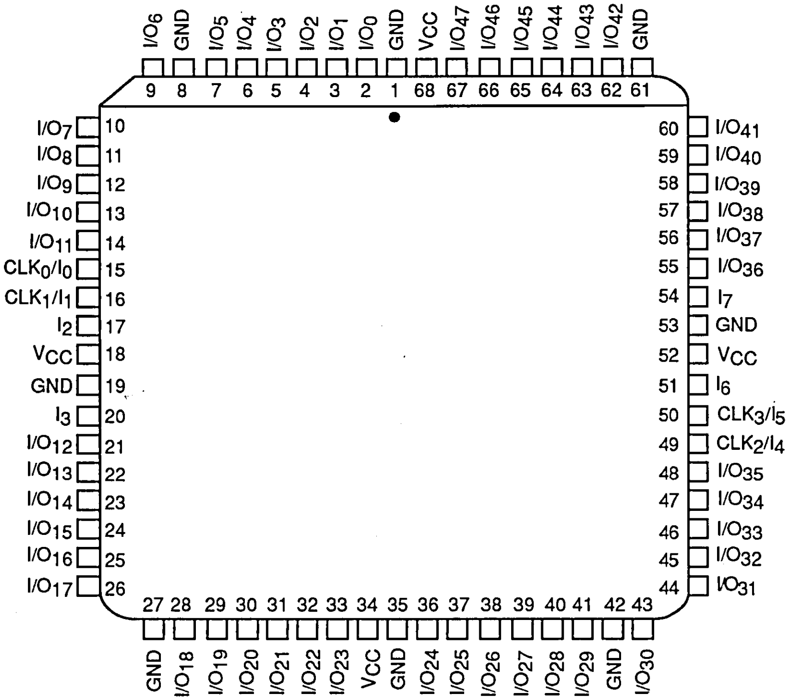
BLOCK DIAGRAM



14130F-001C

CONNECTION DIAGRAMS
Top View

PLCC



14130F-002A

Pin Designations

CLK/I	Clock or Input
GND	Ground
I	Input
I/O	Input/Output
V_{CC}	Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

MACH 220 -15 J C

FAMILY TYPE
MACH = Macro Array CMOS High-Speed

DEVICE NUMBER
220 = 96 Macrocells, 68 Pins

SPEED
-15 = 15 ns t_{PD}
-20 = 20 ns t_{PD}

OPTIONAL PROCESSING
Blank = Standard Processing

OPERATING CONDITIONS
C = Commercial (0°C to +75°C)

PACKAGE TYPE
J = 68-Pin Plastic Leaded Chip Carrier (PL 068)

Valid Combinations	
MACH220-15 MACH220-20	JC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH220 consists of eight PAL blocks connected by a switch matrix. There are 48 I/O pins and 4 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are 4 clock pins that can also be used as dedicated inputs.

All inputs and I/O pins have built-in pull-up resistors. While it is always good design practice to tie unused pins high or low, the pull-up resistors provide design security and stability in the event that unused pins are left disconnected.

The PAL Blocks

Each PAL block in the MACH220 (Figure 12) contains a 48-product-term logic array, a logic allocator, 6 output macrocells, 6 buried macrocells, and 6 I/O cells. The switch matrix feeds each PAL block with 26 inputs. This makes the PAL block look effectively like an independent "PAL26V12" with 6 buried macrocells.

In addition to the logic product terms, two output enable product terms, an asynchronous reset product term, and an asynchronous preset product term are provided. One of the two output enable product terms can be chosen within each I/O cell in the PAL block. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH220 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 12 internal feedback signals and 6 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH220 product-term array consists of 48 product terms for logic use, and 4 special-purpose product terms. Two of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset.

The Logic Allocator

The logic allocator in the MACH220 takes the 48 logic product terms and allocates them to the 12 macrocells as needed. Each macrocell can be driven by up to 16 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 9 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 12 for cluster and macrocell numbers.

Table 9. Logic Allocation

Macrocell		Available Clusters
Output	Buried	
M_0		C_0, C_1, C_2
	M_1	C_0, C_1, C_2, C_3
M_2		C_1, C_2, C_3, C_4
	M_3	C_2, C_3, C_4, C_5
M_4		C_3, C_4, C_5, C_6
	M_5	C_4, C_5, C_6, C_7
M_6		C_5, C_6, C_7, C_8
	M_7	C_6, C_7, C_8, C_9
M_8		C_7, C_8, C_9, C_{10}
	M_9	C_8, C_9, C_{10}, C_{11}
M_{10}		C_9, C_{10}, C_{11}
	M_{11}	C_{10}, C_{11}

The Macrocell

The MACH220 has two types of macrocell: output and buried. The output macrocells can be configured as either registered, latched, or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured with or without the flip-flop. The registers can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of four clock/gate pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The latch holds its data when the gate input is HIGH, and is transparent when the gate input is LOW. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The buried macrocells are the same as the output macrocells if they are used for generating logic. In that case, the only thing that distinguishes them from the output macrocells is the fact that there is no I/O cell connection, and the signal is only used internally. The buried macrocell can also be configured as an input register or latch.

The I/O Cell

The I/O cell in the MACH220 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to all I/O cells in a PAL block.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

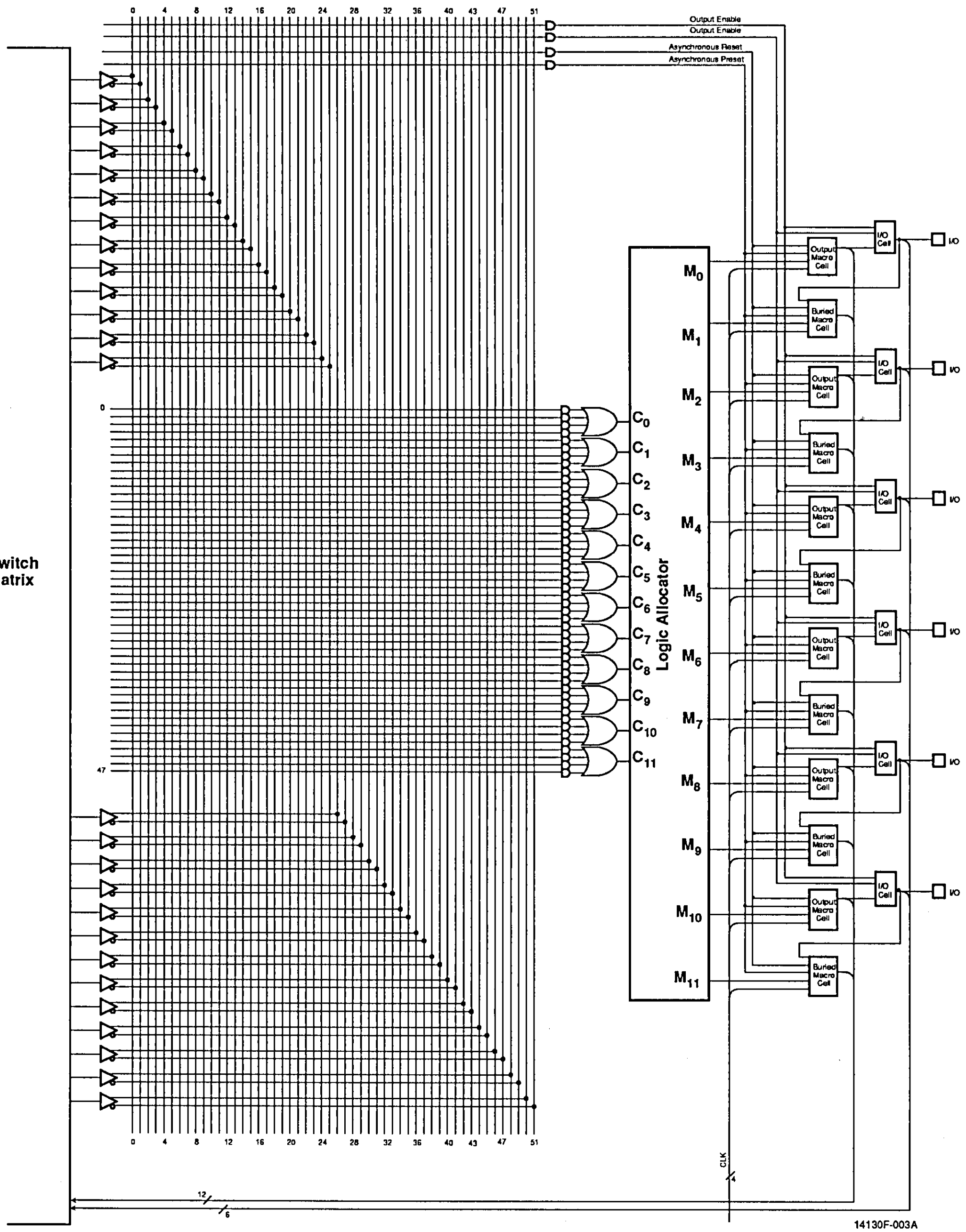


Figure 12. MACH220 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} +0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} +0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		−100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f =0 MHz		300	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	10		13		ns
				T-type	11		14		ns
t_H	Register Data Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					10		12	ns
t_{WL}	Clock Width			LOW	6		8		ns
t_{WH}				HIGH	6		8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	D-type	50		40		MHz
				T-type	47.6		38.5		MHz
		Internal Feedback (f_{CNT})		D-type	66.6		47.6		MHz
				T-type	55.5		43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		83.3		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				10		13		ns
t_{HL}	Latch Data Hold Time				0		0		ns
t_{GO}	Gate to Output (Note 3)					11		12	ns
t_{GWL}	Gate Width LOW				6		8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					17		22	ns
t_{SIR}	Input Register Setup Time				2		2		ns
t_{HIR}	Input Register Hold Time				2		2		ns
t_{ICO}	Input Register Clock to Combinatorial Output					17		22	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-Type	12		15		ns
				T-Type	14		17		ns
t_{WICL}	Input Register Clock Width			LOW	6		8		ns
t_{WICH}				HIGH	6		8		ns
f_{MAXIR}	Maximum Input Register Frequency		$1/(t_{WICL} + t_{WICH})$		83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time				2		2		ns
t_{HIL}	Input Latch Hold Time				2		2		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					17		22	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					19		24	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				12		15		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				12		15		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (Continued)

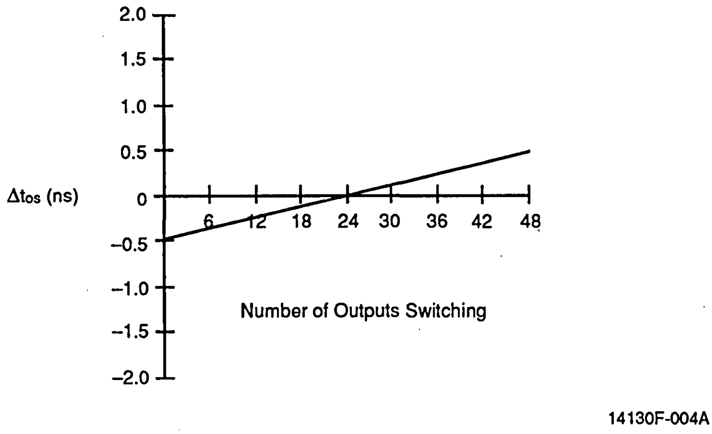
Parameter Symbol	Parameter Description	-15		-20		Unit
		Min.	Max.	Min.	Max.	
t_{WIGZ}	Input Latch Gate Width LOW	6		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		19		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)	15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)	10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 4)	15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 4)	10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		15		20	ns

Notes:

2. See Switching Test Circuit, page 112, for test conditions.
3. Parameters measured with 32 outputs switching.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

TYPICAL SWITCHING CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C. These parameters are not tested.



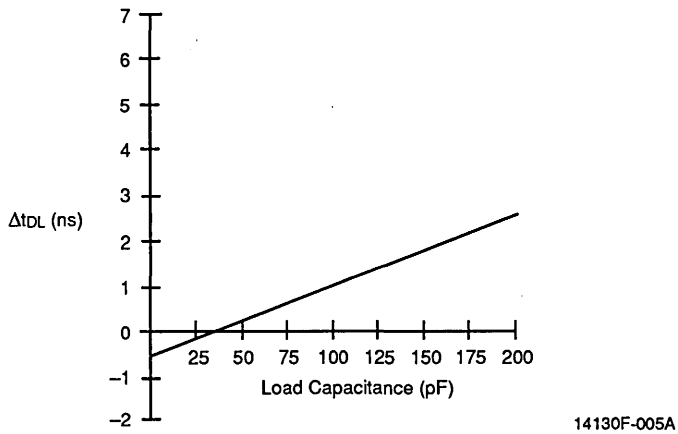
Derating for Number of Outputs Switching

Note:

Applies to t_{PD}, t_{CO}. Calculate as:

$t_{derated} = t_{24\ O/P} + \Delta t_{OS}$

Datasheet numbers ($t_{24\ O/P}$) are specified at 24 outputs switching



Capacitive Load Derating

Note:

Applies to all AC specifications and rise and fall times. Calculate as:

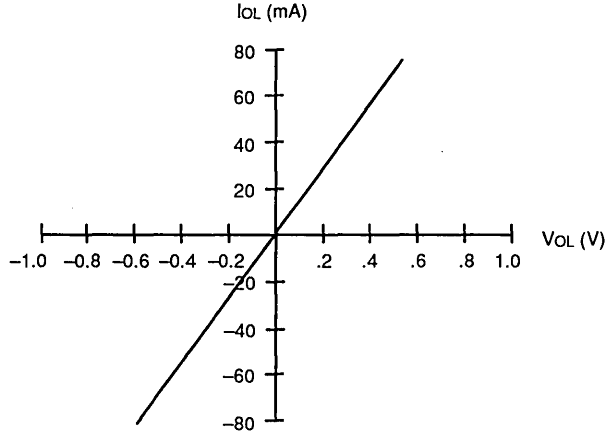
$t_{derated} = t_{35\ pF} + \Delta t_{DL}$

Datasheet numbers ($t_{35\ pF}$) are specified with 35 pF.

For typical rise and fall rates, use 1V/ns at 35 pF.

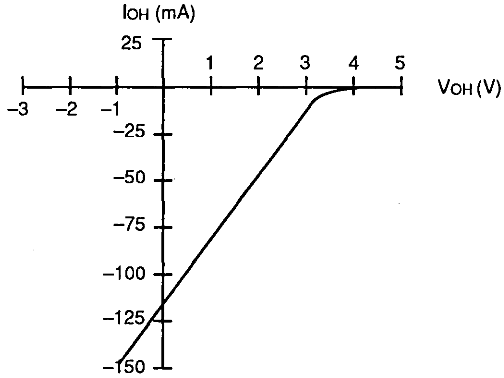
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



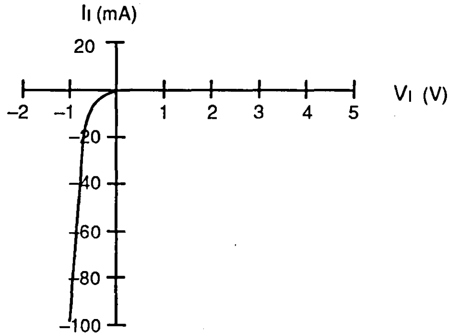
14130F-006A

Output, LOW



14130F-007A

Output, HIGH



14130F-008A

Input

TYPICAL DYNAMIC I_{CC} CHARACTERISTICS

These parameters are not tested. Please refer to page 114 for a discussion on the usage of these parameters.

Parameter Symbol	Parameter Description	Typ.	Unit
I_{CC0}	Base static I_{CC}	175	mA
i_I	Incremental input current	29	µA/MHz
i_B	Incremental current per PAL block	26	µA/MHz
i_O	Incremental output current	102	µA/MHz
i_V	Voltage dependence	38	%/V
i_T	Temperature dependence	–0.14	%/°C

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ. PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		10	°C/W
θ_{ja}	Thermal impedance, junction to ambient		33	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	29	°C/W
		400 lfpm air	27	°C/W
		600 lfpm air	24	°C/W
		800 lfpm air	23	°C/W

Plastic θ_{jc} Considerations

The data listed for plastic θ_{jc} are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θ_{jc} measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θ_{jc} tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

MACH230-15/20

Advanced Micro Devices

High-Density EE CMOS Programmable Logic

DISTINCTIVE CHARACTERISTICS

- 84 Pins
- 128 Macrocells
- 15 ns t_{PD} Commercial
  20 ns t_{PD} Military
- 50 MHz f_{MAX} Commercial
  40 MHz f_{MAX} Military
- 70 Inputs
- 64 Outputs
- 128 Flip-flops; 4 clock choices
- 8 "PAL26V16" blocks with buried macrocells
- Pin-compatible with MACH130

GENERAL DESCRIPTION

The MACH230 is a member of AMD's high-performance EE CMOS MACH 2 device family. This device has approximately twelve times the logic macrocell capability of the popular PAL22V10 at an equal speed with a lower cost per macrocell.

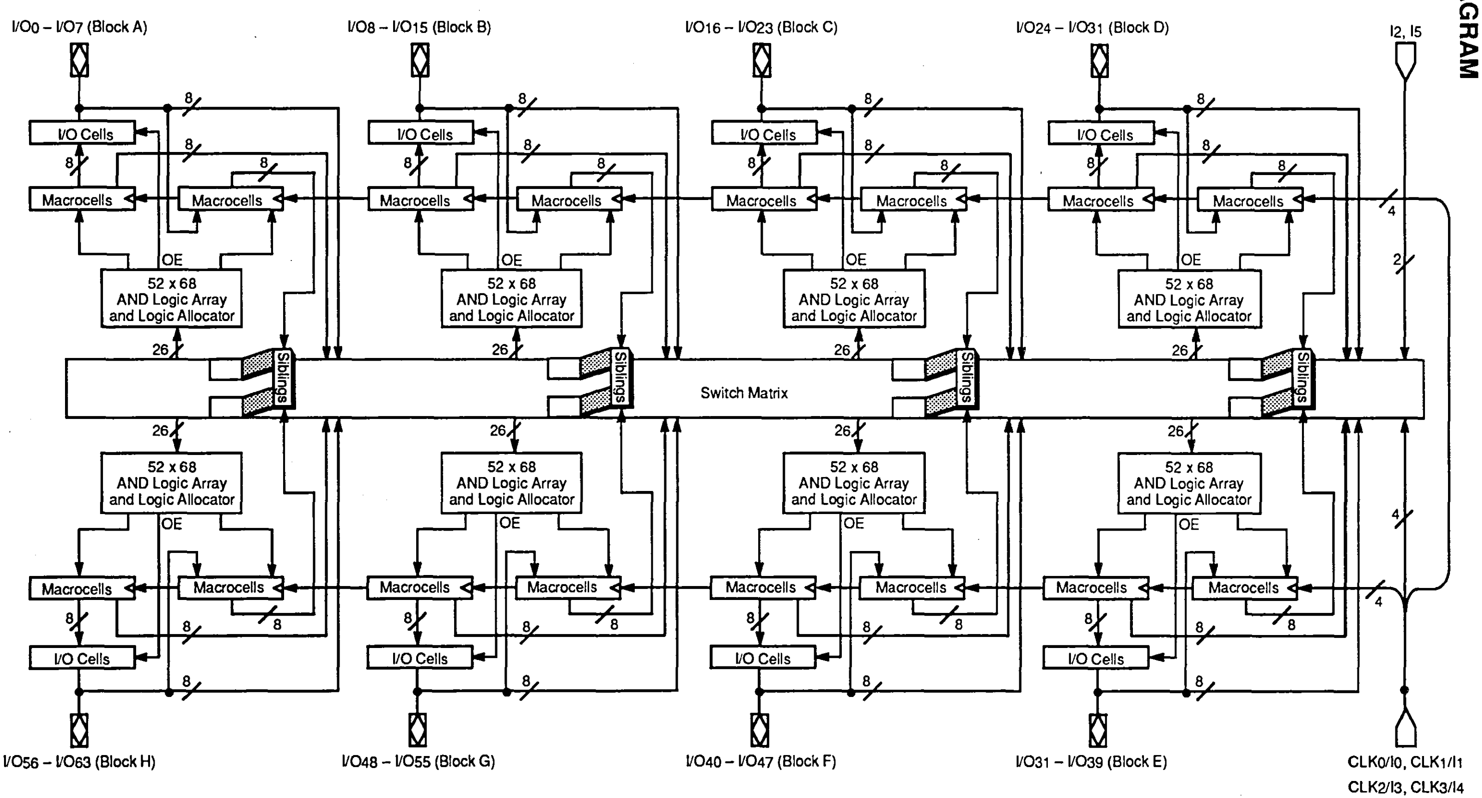
The MACH230 consists of eight PAL blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH230 has two kinds of macrocell: output and buried. The output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACH230 has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers for use in synchronizing signals and reducing setup time requirements.

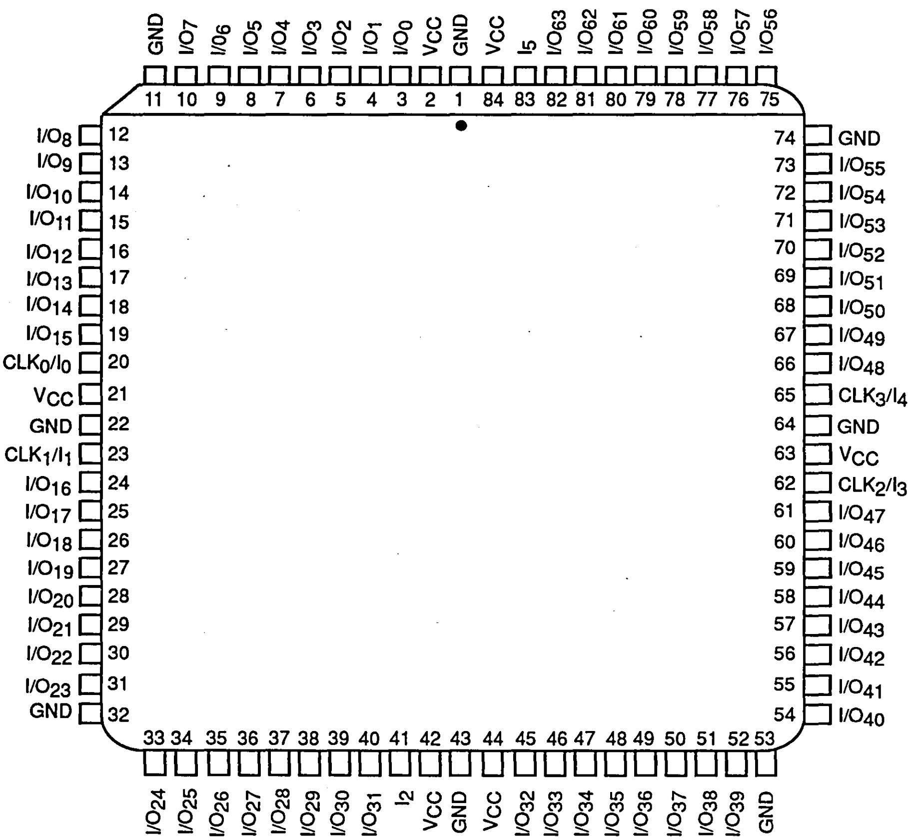
Publication # 14132 Rev. F Amendment/0
Issue Date: July 1992

BLOCK DIAGRAM



14132F-001B

CONNECTION DIAGRAM
Top View



14132D-002A

Pin Designations

CLK/I	Clock or Input
GND	Ground
I	Input
I/O	Input/Output
V_{CC}	Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

MACH 230 -15 J C

FAMILY TYPE
MACH = Macro Array CMOS High-Speed

DEVICE NUMBER
230 = 128 Macrocells, 84 Pins

SPEED
-15 = 15 ns t_{PD}
-20 = 20 ns t_{PD}

OPTIONAL PROCESSING
Blank = Standard Processing

OPERATING CONDITIONS
C = Commercial (0°C to +75°C)

PACKAGE TYPE
J = 84-Pin Plastic Leaded Chip Carrier (PL 084)

Valid Combinations	
MACH230-15 MACH230-20	JC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations.

ORDERING INFORMATION (Preliminary)
APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Product List) products are fully compliant with MIL–STD–883 requirements. The order number (Valid Combination) is formed by a combination of:

MACH 230 -20 /B X A

OPTIONAL PROCESSING
MACH = Macro Array CMOS High-Speed

DEVICE NUMBER
230 = 128 Macrocells, 84 Pins

SPEED
-20 = 20 ns t_{PD}

LEAD FINISH
A = Hot Solder Dip

PACKAGE TYPE
X = 84-Pin Metal-Lid Ceramic Quad Flatpack (CFT084)

DEVICE CLASS
/B = Class B

Valid Combinations
MACH230-20/BXA

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

FUNCTIONAL DESCRIPTION

The MACH230 consists of eight PAL blocks connected by a switch matrix. There are 64 I/O pins and 2 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are 4 clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH230 (Figure 13) contains a 64-product-term logic array, a logic allocator, 8 output macrocells, 8 buried macrocells, and 8 I/O cells. The switch matrix feeds each PAL block with 26 inputs. This makes the PAL block look effectively like an independent "PAL26V16" with 8 buried macrocells.

In addition to the logic product terms, two output enable product terms, an asynchronous reset product term, and an asynchronous preset product term are provided. One of the two output enable product terms can be chosen within each I/O cell in the PAL block. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH230 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 8 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The MACH230 places a restriction on buried macrocell feedback only. Buried macrocell feedback from one block can be used as an input only to that block or its "sibling" block. Sibling blocks are illustrated in the block diagram on page 80 and in Table 10. Output macrocell feedback is not restricted.

Table 10. Sibling Blocks

PAL Block	Sibling Block
A	H
B	G
C	F
D	E
E	D
F	C
G	B
H	A

The Product-Term Array

The MACH230 product-term array consists of 64 product terms for logic use, and 4 special-purpose product terms. Two of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset.

The Logic Allocator

The logic allocator in the MACH230 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 16 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 11 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 13 for cluster and macrocell numbers.

Table 11. Logic Allocation

Macrocell		Available Clusters
Output	Buried	
M_0		C_0, C_1, C_2
	M_1	C_0, C_1, C_2, C_3
M_2		C_1, C_2, C_3, C_4
	M_3	C_2, C_3, C_4, C_5
M_4		C_3, C_4, C_5, C_6
	M_5	C_4, C_5, C_6, C_7
M_6		C_5, C_6, C_7, C_8
	M_7	C_6, C_7, C_8, C_9
M_8		C_7, C_8, C_9, C_{10}
	M_9	C_8, C_9, C_{10}, C_{11}
M_{10}		$C_9, C_{10}, C_{11}, C_{12}$
	M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_{12}		$C_{11}, C_{12}, C_{13}, C_{14}$
	M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_{14}		C_{13}, C_{14}, C_{15}
	M_{15}	C_{14}, C_{15}

The Macrocell

The MACH230 has two types of macrocell: output and buried. The output macrocells can be configured as either registered, latched, or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured with or without the flip-flop. The registers can be configured as D-type or T-type, allowing for product-term optimization.

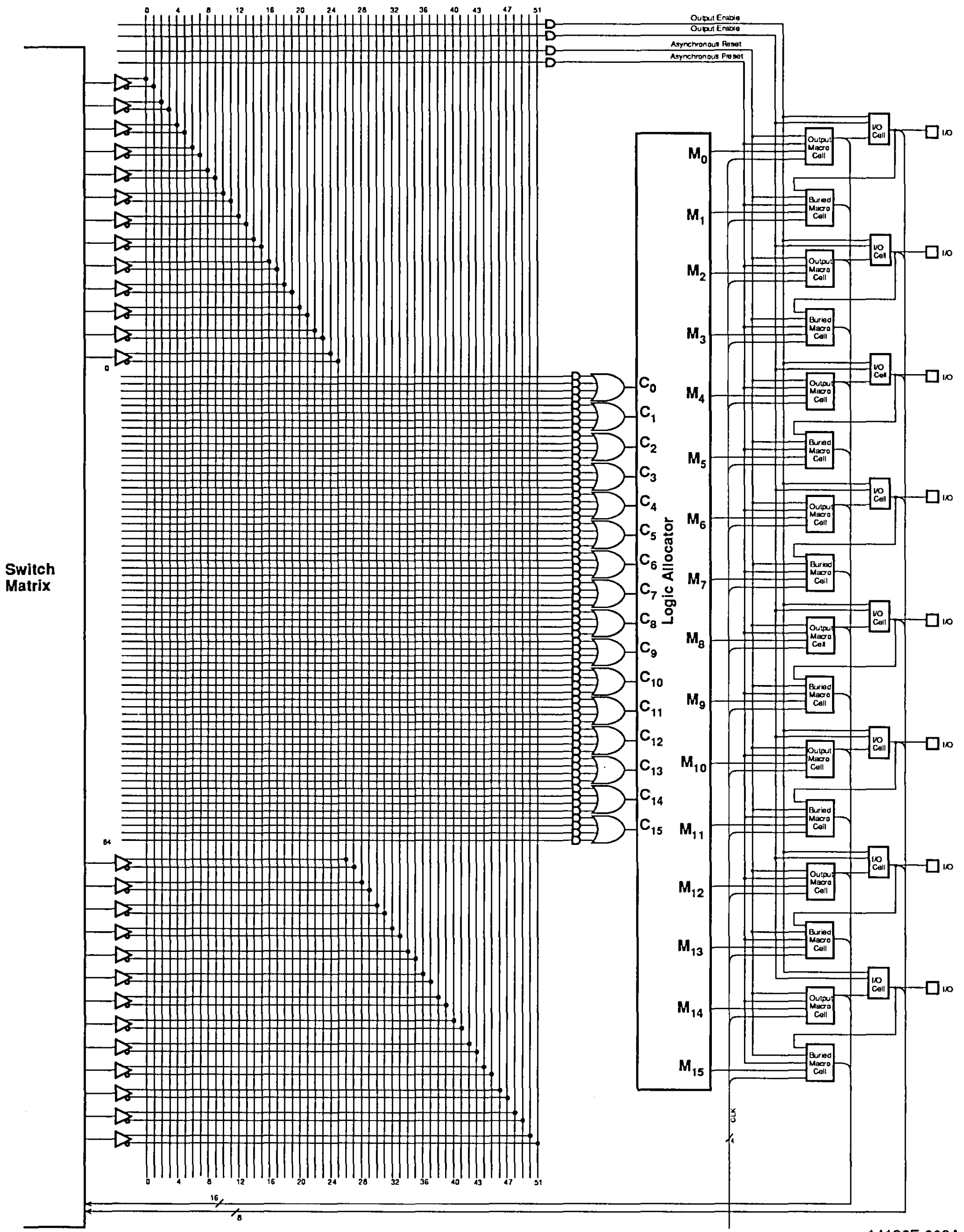
The flip-flops can individually select one of four clock/gate pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The latch holds its data when the gate input is HIGH, and is transparent when the gate input is LOW. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The buried macrocells are the same as the output macrocells if they are used for generating logic. In that case, the only thing that distinguishes them from the output macrocells is the fact that there is no I/O cell connection, and the signal is only used internally. The buried macrocell can also be configured as an input register or latch.

The I/O Cell

The I/O cell in the MACH230 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to all I/O cells in a PAL block.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.



14132F-003A

Figure 13. MACH230 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to V_{CC} +0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V_{CC} +0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f =0 MHz		360	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-15		-20		
					Min.	Max.	Min.	Max.	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	10		13		ns
				T-type	11		14		ns
t_H	Register Data Hold Time				0		0		ns
t_{CO}	Clock to Output (Note 3)					10		12	ns
t_{WL}	Clock Width			LOW	6		8		ns
t_{WH}				HIGH	6		8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	D-type	50		40		MHz
				T-type	47.6		38.5		MHz
		Internal Feedback (f_{CNT})		D-type	66.6		47.6		MHz
				T-type	55.5		43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		83.3		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				10		13		ns
t_{HL}	Latch Data Hold Time				0		0		ns
t_{GO}	Gate to Output (Note 3)					11		12	ns
t_{GWL}	Gate Width LOW				6		8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					17		22	ns
t_{SIR}	Input Register Setup Time				2		2		ns
t_{HIR}	Input Register Hold Time				2		2		ns
t_{ICO}	Input Register Clock to Combinatorial Output					17		22	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-Type	12		15		ns
				T-Type	14		17		ns
t_{WICL}	Input Register Clock Width			LOW	6		8		ns
t_{WICH}				HIGH	6		8		ns
f_{MAXIR}	Maximum Input Register Frequency		$1/(t_{WICL} + t_{WICH})$		83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time				2		2		ns
t_{HIL}	Input Latch Hold Time				2		2		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					17		22	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					19		24	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				12		15		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				12		15		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (Continued)

Parameter Symbol	Parameter Description	-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
t_{WIGZ}	Input Latch Gate Width LOW	6		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		19		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)	15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)	10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 4)	15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 4)	10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		15		20	ns

Notes:

2. See Switching Test Circuit, page 112, for test conditions.
3. Parameters measured with 32 outputs switching.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} +0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} +0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_C = −55°C to +125°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES

Military (M) Devices (Note 1)

Operating Case Temperature (T_C)	−55°C to +125°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at T_C = +25°C, +125°C and −55°C, per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

PRELIMINARY

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.5 V, V_{CC} = Max. (Note 4)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 4)		−10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.5 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		40	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 4)		−40	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 5)	−30	−200	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f = 0 MHz			mA

Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at any time the design is modified where I_{SC} may be affected.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz		pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

PRELIMINARY

Parameter Symbol	Parameter Description				-20 Min.	-20 Max.	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	13		ns
				T-type	14		ns
t_H	Register Data Hold Time				0		ns
t_{CO}	Clock to Output (Note 3)					12	ns
t_{WL}	Clock Width			LOW	8		ns
t_{WH}				HIGH	8		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	D-type	40		MHz
				T-type	38.5		MHz
		Internal Feedback (f_{CNT})		D-type	47.6		MHz
				T-type	43.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				13		ns
t_{HL}	Latch Data Hold Time				0		ns
t_{GO}	Gate to Output (Note 3)					12	ns
t_{GWL}	Gate Width LOW				8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					22	ns
t_{SIR}	Input Register Setup Time				2		ns
t_{HIR}	Input Register Hold Time				2		ns
t_{ICO}	Input Register Clock to Combinatorial Output					22	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	15		ns
				T-type	17		ns
t_{WICL}	Input Register Clock Width			LOW	8		ns
t_{WICH}				HIGH	8		ns
f_{MAXIR}	Maximum Input Register Frequency (Note 4)			$1/(t_{WICL} + t_{WICH})$	62.5		MHz
t_{SIL}	Input Latch Setup Time				2		ns
t_{HIL}	Input Latch Hold Time				2		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					22	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					24	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				15		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				15		ns

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2) (Continued)

PRELIMINARY

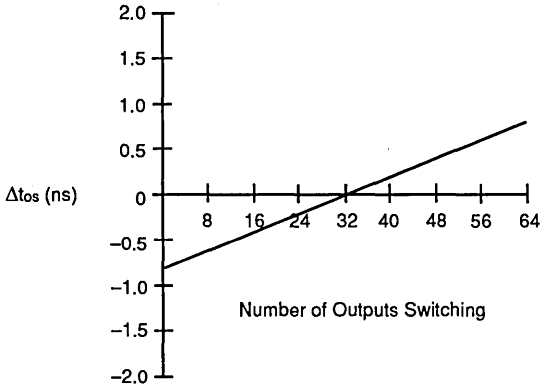
Parameter Symbol	Parameter Description	-20 Min.	-20 Max.	Unit
t_{WIGZ}	Input, Latch Gate Width LOW	8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		25	ns
t_{ARW}	Asynchronous Reset Width (Note 4)	20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 4)	15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		25	ns
t_{APW}	Asynchronous Preset Width (Note 4)	20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 4)	15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Notes 3, 4)		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Notes 3, 4)		20	ns

Notes:

2. See Switching Test Circuit, page 112, for test conditions. For APL products, Group A, Subgroups 9, 10 and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3. Parameters measured with 32 outputs switching.
4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

TYPICAL SWITCHING CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C. These parameters are not tested.



14132F-004A

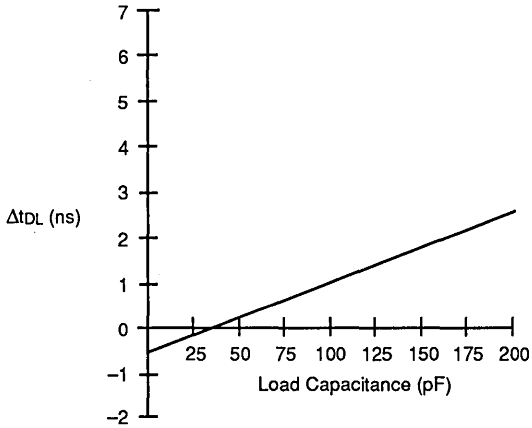
Derating for Number of Outputs Switching

Note:

Applies to t_{PD}, t_{CO}. Calculate as:

$t_{derated} = t_{32\ O/P} + \Delta t_{OS}$

Datasheet numbers ($t_{32\ O/P}$) are specified at 32 outputs switching



14132F-005A

Capacitive Load Derating

Note:

Applies to all AC specifications and rise and fall times. Calculate as:

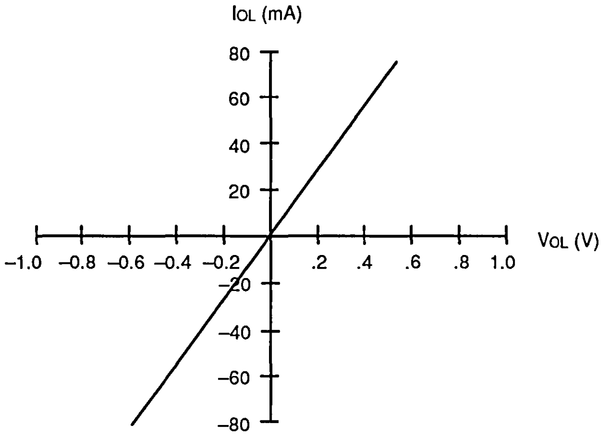
$t_{derated} = t_{35\ pF} + \Delta t_{DL}$

Datasheet numbers ($t_{35\ pF}$) are specified with 35 pF.

For typical rise and fall rates, use 1V/ns at 35 pF.

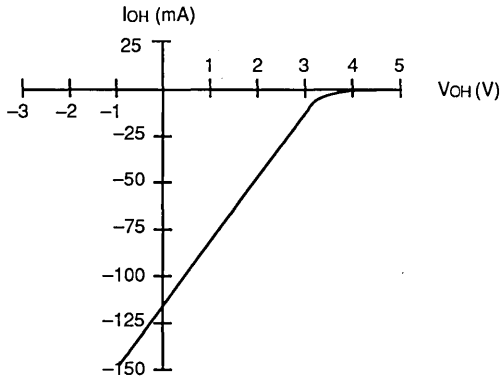
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



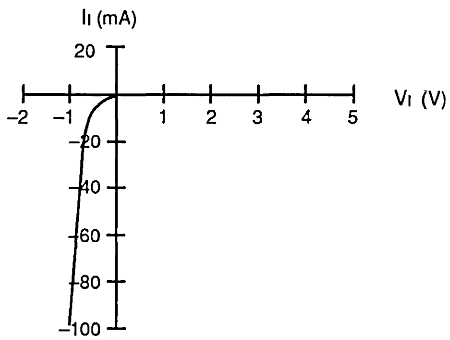
Output, LOW

14132-006A



Output, HIGH

14132-007A



14132-008A

Input

TYPICAL DYNAMIC I_{CC} CHARACTERISTICS

These parameters are not tested. Please refer to page 114 for a discussion on the usage of these parameters.

Parameter Symbol	Parameter Description	Typ.	Unit
I_{CC0}	Base static I_{CC}	225	mA
i_I	Incremental input current	29	µA/MHz
i_B	Incremental current per PAL block	26	µA/MHz
i_O	Incremental output current	102	µA/MHz
i_V	Voltage dependence	38	%/V
i_T	Temperature dependence	–0.13	%/°C

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ. PLCC	Typ. CQFP	Unit
θ_{jc}	Thermal impedance, junction to case		5	4	°C/W
θ_{ja}	Thermal impedance, junction to ambient		20	28	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	17	24	°C/W
		400 lfpm air	14	20	°C/W
		600 lfpm air	12	19	°C/W
		800 lfpm air	10	17	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

Asynchronous MACH Devices

Advanced Micro Devices

ASYNCHRONOUS MACH DEVICES

The MACH215 is a MACH device designed for use in asynchronous applications as well as in synchronous ones. In addition to having the two global clocks present in the MACH210, each output macrocell can also be clocked by its own individual product term. The polarity of all clock signals, including the global clocks, is programmable for each macrocell. Individual asynchronous reset, asynchronous preset, and three-state product-term controls are also provided for each macrocell.

Each I/O pin is also capable of being registered or latched as an input, with the register or latch being driven by one of the two global clock signals. The polarity of the clock signals is also programmable for each input macrocell.

The MACH215 is a 44-pin device with 32 output macrocells and 32 input macrocells. It is provided in a PLCC package.

Functional Description

The MACH215 has a structure fundamentally very similar to that of the other MACH devices.

The fundamental architecture of the MACH devices consists of several PAL blocks interconnected by a switch matrix. The switch matrix allows communication between PAL blocks, and routes inputs to the PAL blocks. Together the PAL blocks and switch matrix allow the logic designer to create large designs in a single device instead of multiple devices.

Most pins are I/O pins that can be used as inputs, outputs, or bidirectional pins. There are some dedicated input pins, but all macrocells have internal feedback, allowing the pin to be used as an input if the macrocell signal is not needed externally.

The key to being able to make effective use of these devices lies in the interconnect schemes used. Because of the use of programmable interconnections, the product-term arrays have been decoupled from the switch matrix, the macrocells, and the I/O pins. This provides much greater flexibility, and allows designs to be placed and routed efficiently and quickly.

The internal architecture is such that all signals incur the same delays, regardless of routing. This means that the performance of a design is design-independent, and is known before the design is even begun.

The PAL Blocks

The PAL blocks can be viewed as independent PAL devices on the chip. This provides for logic functions that need the complete interconnect that a PAL device provides. The PAL blocks communicate with each other only through the switch matrix.

Each PAL block contains a product-term array, a logic allocator, macrocells, and I/O cells. The product-term array generates the basic logic, although the number of product terms per macrocell is variable. The logic allocator distributes the product terms to the macrocells. This allows the distribution of product terms as required by the design. The macrocell configures the signal, and the I/O cell delivers the final signal to the output pin.

The Switch Matrix

The switch matrix takes all dedicated inputs, I/O feedback signals, and buried feedback signals and routes them as needed to the various PAL blocks. Feedback signals that only return to the same PAL block still go through the switch matrix. This provides a way for the PAL blocks to communicate with each other with consistent, predictable delays. It is the switch matrix which makes the MACH devices more than just multiple PAL devices on a single chip.

For designs that consist of smaller functional units that are connected together, the PAL blocks provide the routing software with local full connectivity for each unit, connected by the switch matrix. For designs that are larger in scope, the switch matrix allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into the PAL blocks through the switch matrix so that the designer does not have to be concerned with the internal organization.

The Product-Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the switch matrix, and are provided in both true and complement forms for efficient logic implementation.

Because the number of product terms allocated to each macrocell is not fixed, the full sum of products is not realized in the array. The product terms drive the logic allocator, which allocates the product terms to the appropriate macrocells.

In addition to product terms for use in generating logic, product terms are also provided for clock, asynchronous reset, asynchronous preset, and output enable controls for each output macrocell.

The Logic Allocator

The logic allocator (Figure 14) is a block within which different product terms are allocated to the appropriate macrocells in groups of four product terms called "product term clusters". The availability and distribution of product term clusters is automatically considered by the software as it places and routes functions within the PAL block. The size of the product term clusters has been designed to provide high utilization of product terms. Complex functions using many product terms are possible. Yet when functions use few product terms, there will be a minimal number of unused–or wasted–product terms left over.

The product term clusters do not "wrap" around the logic block. This means that the macrocells at the ends of the block have fewer product terms available. Please refer to the individual product data sheets for details.

The Macrocell

There are two types of macrocell in the MACH215: output macrocells and input macrocells. The output macrocell takes the logic of the device and provides it to I/O pins and/or provides feedback for additional logic generation. The input macrocell allows I/O pins to be configured as registered or latched inputs.

The output macrocell (Figure 15) can generate registered or combinatorial outputs. In addition, a transparent-low latched configuration is provided. If used, the register can be configured as a T-type or a D-type flip-flop. Register and latch functionality is defined in Table 12. Programmable polarity and the T-type flip-flop both give the software a way to minimize the number of product terms needed. These choices can be made automatically by the software when it fits the design into the device.

Table 12. Register/Latch Operation

Configuration	D/T	CLK/LE*	Q+
D-Register	X	0, 1, ↓ (↑)	Q
	0	↑ (↓)	0
	1	↑ (↓)	1
T-Register	X	0,1, ↓ (↑)	Q
	0	↑ (↓)	Q
	1	↑ (↓)	$\overline{Q}$
Latch	0	0 (1)	0
	1	0 (1)	1
	0	1 (0)	Q
	1	1 (0)	Q

*Polarity of CLK/LE can be programmed.

The output macrocell sends its output back to the switch matrix, via internal feedback, and to the I/O cell. The feedback is always available regardless of the configuration of the I/O cell. This allows for buried combinatorial or registered functions, freeing up the I/O pins for use as inputs if not needed as outputs. The basic output macrocell configurations are shown in Figure 16.

The clock/latch-enable for each individual output macrocell can be driven by one of four signals. Two of the signals are provided by the global clock pin CLK_0/LE_0; either polarity may be chosen. The other two signals come from a product term provided for each output macrocell. Either polarity of the logic generated by the product term can be chosen. The global clock pin is also available as an input, although care must be taken when a signal acts as both clock and input to the same device.

Each individual output macrocell also has a product term for asynchronous reset and a product term for asynchronous preset. This means that any register or latch may be reset or preset without affecting any other register or latch in the device. The functionality of the flip-flops with respect to initialization is illustrated in Table 13.

Table 13. Asynchronous Reset/Preset Operation

AR	AP	CLK/LE	Q+
0	0	X	See Table 12
0	1	X	1
1	0	X	0
1	1	X	0

The input macrocell (Figure 17) consists of a flip-flop that can be used to provide registered or latched inputs. The flip-flop can be clocked by either polarity of one of the two global clock/latch-enable pins.

No reset or preset is provided for these flip-flops. If combinatorial inputs are desired, this macrocell is not used, and the feedback from the I/O pin is used directly. Both the I/O pin feedback and the output of the input register or latch are always available to the switch matrix.

Possible input macrocell configurations are shown in Figure 18.

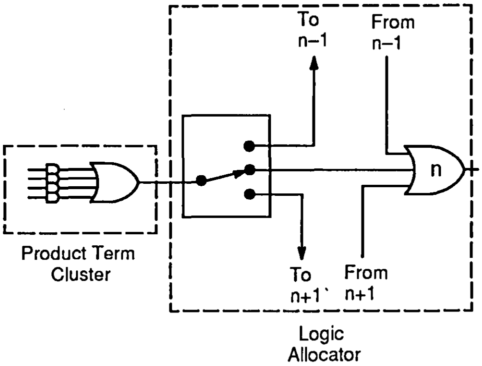


Figure 14. Product Term Clusters and the Logic Allocator

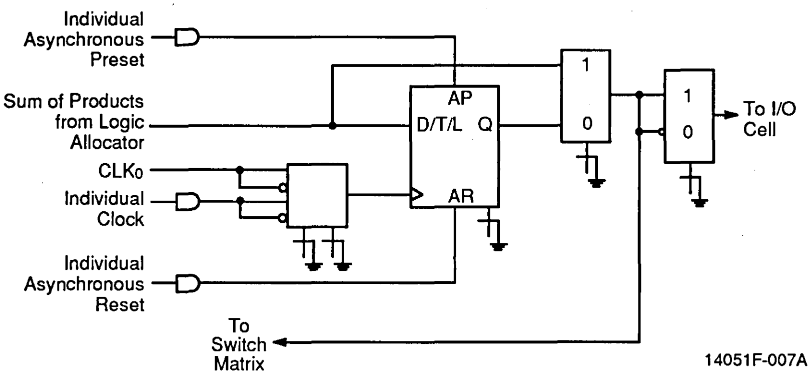


Figure 15. Output Macrocell

The I/O cell (Figure 19) provides a three-state output buffer. The three-state control is provided by an individual product term for each I/O cell. Depending on the logic programmed onto this product term, the I/O pin can be configured as an output, an input, or a bidirectional pin. The feedback from the I/O pin is always available to the switch matrix, regardless of the state of the output buffer or the output macrocell.

Register Preload

All registers on the MACH devices can be preloaded from the I/O pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Observability

In addition to the control offered by preload, testing requires observability of the internal state of the device following a sequence of vectors. The MACH devices offer an observability feature that allows the user to send hidden buried register values to observable output pins.

For macrocells that are configured as combinatorial, the observability function suppresses the selection of the combinatorial output by forcing the macrocell output multiplexer into registered output mode. The observability function allows observation of the associated registers by overriding the output enable control and enabling the output buffer.

Power-up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. The actual values of the outputs of the MACH devices will depend on the configuration of the macrocell. The Vcc rise must be monotonic and the reset delay time is 10 µs maximum.

Security Bit

A security bit is provided on the MACH devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit, but test vectors containing preload can be used independently of the security bit. The bit can only be erased in conjunction with the array during an erase cycle.

Programming and Erasing

The MACH devices can be programmed on standard logic programmers. They may also be erased to reprogram a previously configured device with a new program. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

The MACH devices offer a very high level of built-in quality. The fact that the device is erasable allows direct verification of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The MACH devices are fabricated with AMD's advanced electrically-erasable floating-gate 0.8-µm CMOS technology. This provides the devices with performance and power consumption that are unmatched in the industry. The floating gate cells rely on Fowler-Nordheim tunneling to charge the gate, and have long proven their endurance and reliability. 20-year data retention is provided over operating conditions when devices are programmed on approved programmers.

The substrate of these devices is grounded, providing for a more efficient circuit. In addition, this provides substrate clamp diodes at all inputs, making them more immune to noisy input signals.

Input and I/O pins all have built-in pull-up resistors that provide a default input value when a pin is disconnected, although it is recommended that unused pins be tied HIGH or LOW.

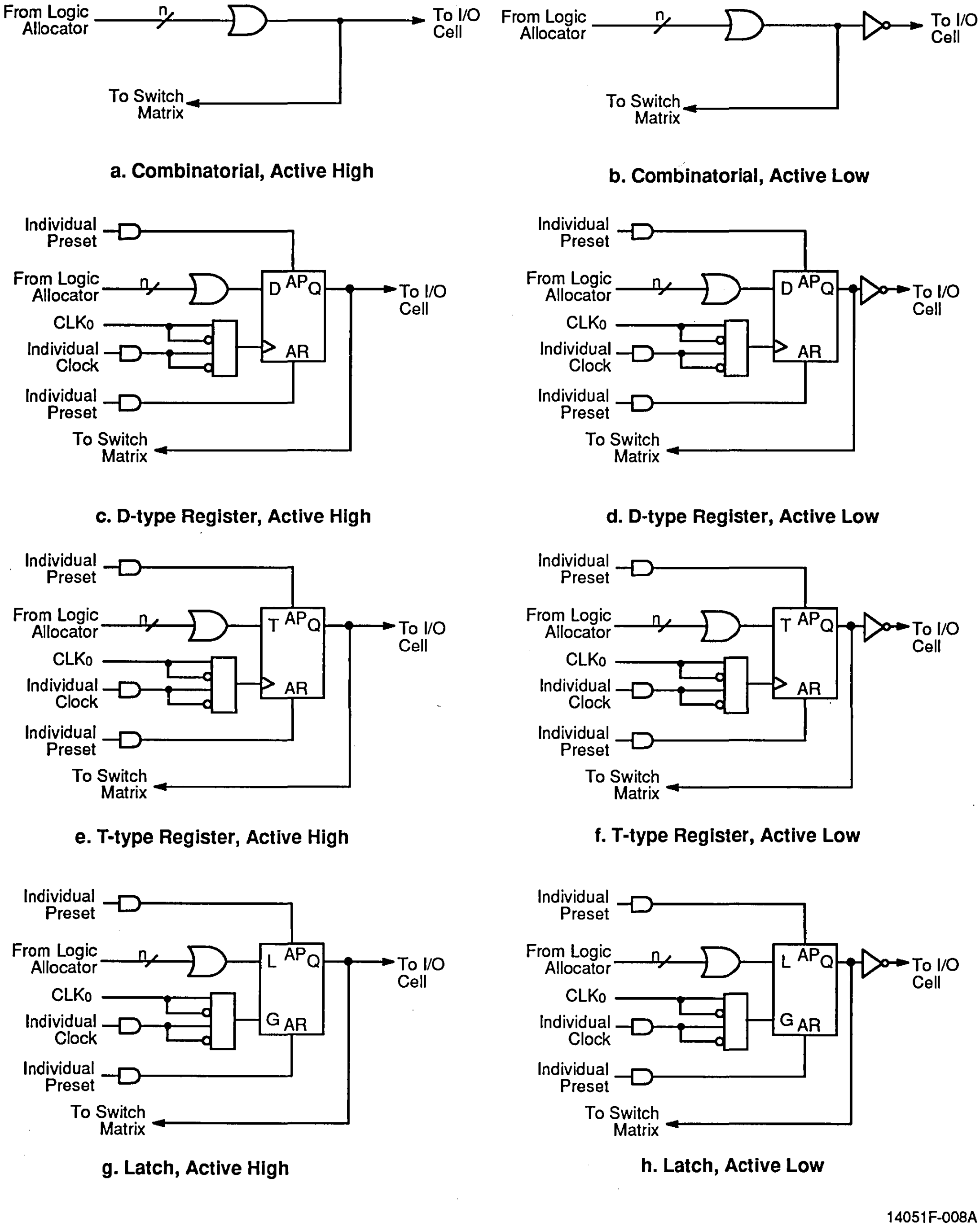


Figure 16. Output Macrocell Configurations

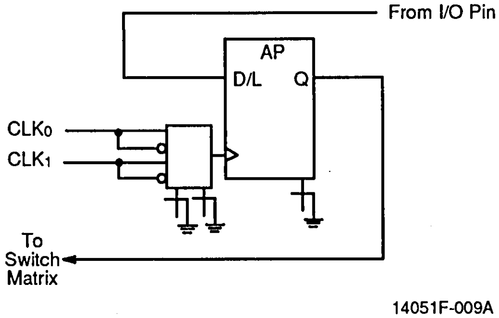


Figure 17. Input Macrocell

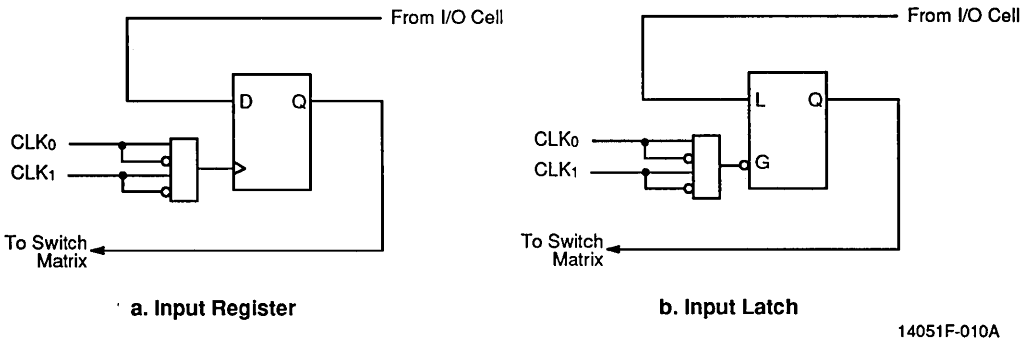


Figure 18. Input Macrocell Configurations

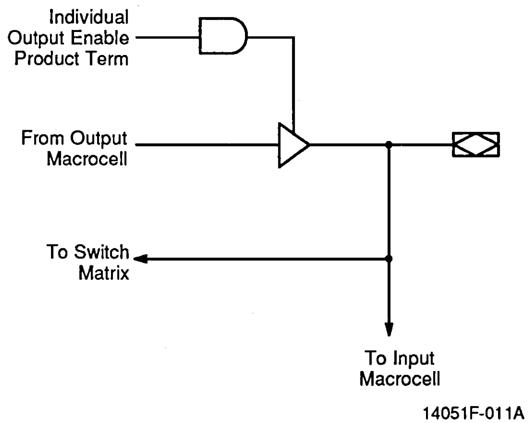


Figure 19. I/O Cell

Advanced Micro Devices

MACH215-12/15/20

High-Density EE CMOS Programmable Logic

DISTINCTIVE CHARACTERISTICS

- **44 Pins**
- **32 Output Macrocells**
- **32 Input Macrocells**
- **Product terms for:**
  - individual flip-flop clock
  - individual asynchronous reset, preset
  - individual output enable
- **12 ns t_{PD}**
- **67 MHz f_{MAX} Commercial**
- **38 Inputs with pull-up resistors**
- **32 Outputs**
- **64 Flip-flops**
- **4 "PAL22RA8" blocks with buried macrocells**
- **Pin-compatible with MACH110, MACH210**

GENERAL DESCRIPTION

The MACH215 is a member of AMD's high-performance EE CMOS MACH device family. This device has approximately three times the capability of the popular PAL20RA10 at an equal or better speed with a lower cost per macrocell.

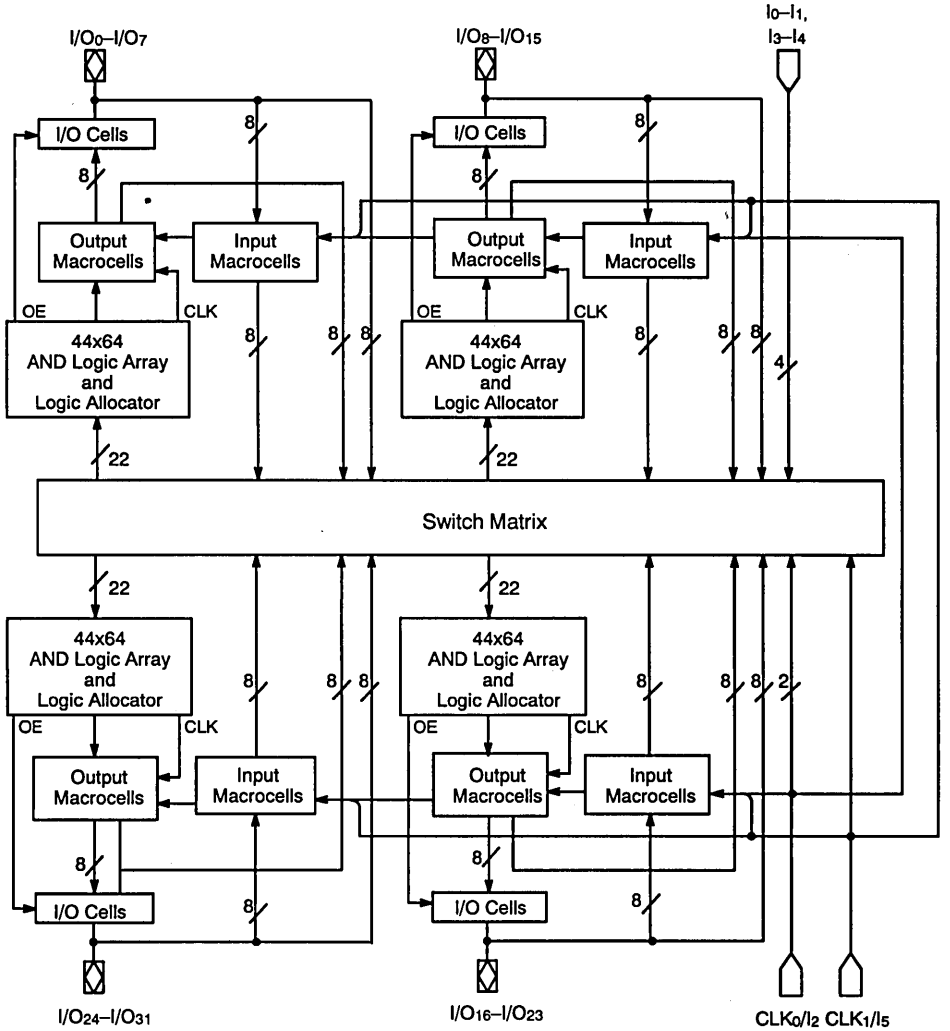
The MACH215 consists of four PAL blocks interconnected by a programmable switch matrix. The four PAL blocks are essentially "PAL22RA8" structures complete with product-term arrays and programmable macrocells, individual register control product terms, and input registers. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH215 has two kinds of macrocell: output and input. The MACH215 output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. Each macrocell has its own dedicated clock, asynchronous reset, and asynchronous preset control. The polarity of the clock signal is programmable. All output macrocells can be connected to an I/O cell.

The MACH215 has dedicated input macrocells which provide input registers or latches for synchronizing input signals and reducing setup time requirements.

Publication# 16751 Rev. A Amendment/0
Issue Date: June 1992

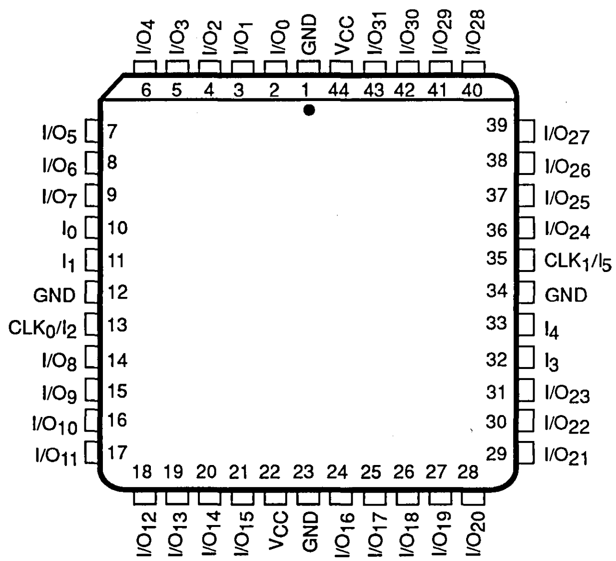
BLOCK DIAGRAM



16751A-001B

CONNECTION DIAGRAM
Top View

PLCC/CQFP



16751A-002A

Pin Designations

CLK/I	Clock or Input
GND	Ground
I	Input
I/O	Input/Output
V_{CC}	Supply Voltage

FUNCTIONAL DESCRIPTION

The MACH215 consists of four asynchronous PAL blocks connected by a switch matrix. There are 32 I/O pins and 4 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are also two additional global clock pins that can be used as dedicated inputs. This device provides two kinds of macrocell: output macrocells and input macrocells. This adds greater logic density without affecting the number of pins.

The PAL Blocks

Each PAL block in the MACH215 (Figure 20) contains a 64-product-term array, a logic allocator, 8 output macrocells, 8 input macrocells, and 8 I/O cells. The switch matrix feeds each PAL block with 22 inputs. This makes the PAL block look effectively like an independent "PAL22RA8" with 8 input macrocells. All flip-flops within the device can operate independently.

The Switch Matrix

The MACH215 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 8 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-term Array

The MACH215 product-term array consists of 32 product terms for logic use and 32 product terms for generating macrocell control signals.

The Logic Allocator

The logic allocator in the MACH215 takes the 32 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 12 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 14 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 20 for cluster and macrocell numbers.

Table 14. Logic Allocation

Output Macrocell	Available Clusters
M_0	C_0, C_1
M_1	C_0, C_1, C_2
M_2	C_1, C_2, C_3
M_3	C_2, C_3, C_4
M_4	C_3, C_4, C_5
M_5	C_4, C_5, C_6
M_6	C_5, C_6, C_7
M_7	C_6, C_7

The Macrocell

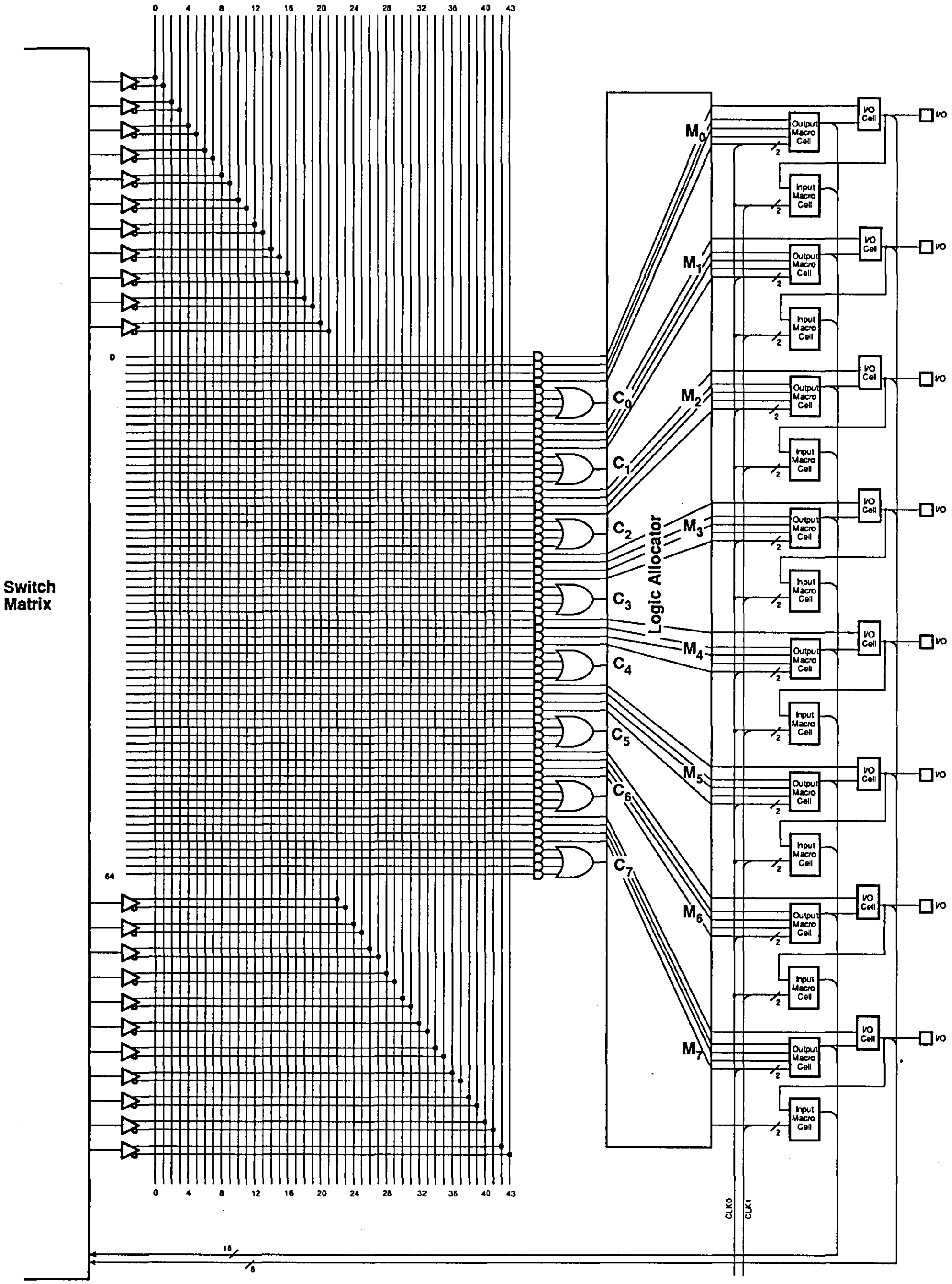
The MACH215 has two types of macrocell: output and input. The output macrocells can be configured as either registered, latched, or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured with or without the flip-flop. The registers can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select either polarity of one of two clock/gate sources: a dedicated product term and a global clock pin. The registers can therefore be clocked on either edge of the clock signal. The latch can hold its data when the gate input is LOW, and be transparent when the gate input is HIGH; or the opposite relationship can be used. The flip-flops can also be asynchronously initialized with the individual asynchronous reset and preset product terms.

The input macrocells can be used to register or latch the input signal. The clock or latch enable can be driven by either polarity of either of the two global clock/latch-enable pins.

The I/O Cell

The I/O cell in the MACH215 consists of a three-state output buffer. The three-state buffer is controlled by a separate product term. This choice makes it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus. The choice can be made independently for each pin.



16751A-003B

Figure 20. MACH215 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to V_{CC} +0.5 V
DC Output or I/O Pin Voltage	−0.5 V to V_{CC} +0.5 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min. V_{IN} = V_{IH} or V_{IL} (Note 1)		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 3)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 3)		−100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 3)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IH} or V_{IL} (Note 3)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 4)	−30	−160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max., f =0 MHz		180	mA

CAPACITANCE (Note 5)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Notes:

1. Total I_{OL} for one PAL block should not exceed 128 mA.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.
5. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description		-12 Min.	-12 Max.	-15 Min.	-15 Max.	-20 Min.	-20 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 2)		3	12	3	15	4	20	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock	D-type	5		6		8		ns
		T-type	6		7		9		ns
t_{HA}	Register Data Hold Time Using Product Term Clock		5		6		8		ns
t_{COA}	Product Term Clock to Output (Note 3)		4	14	4	18	5	22	ns
t_{WLA}	Product Term, Clock Width	LOW	8		9		12		ns
t_{WHA}		HIGH	8		9		12		ns
f_{MAXA}	Maximum Frequency Using Global Clock (Note 3): External Feedback, $1/(t_{SA} + t_{COA})$	D-type	52.6		41.7		33.3		MHz
		T-type	50		40		32.2		MHz
	Internal Feedback (f_{CNTA})	D-type							MHz
		T-type							MHz
	No Feedback, $1/(t_{WLA} + t_{WHA})$		62.5		55.6		41.7		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock	D-type	7		10		13		ns
		T-type	8		11		14		ns
t_{HS}	Register Data Hold Time Using Global Clock		0		0		0		ns
t_{COS}	Global Clock to Output (Note 3)		2	8	2	10	3	12	ns
t_{WLS}	Global Clock Width	LOW	6		6		8		ns
t_{WHS}		HIGH	6		6		8		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 3): External Feedback, $1/(t_{SS} + t_{COS})$	D-type	66.7		50		40		MHz
		T-type	62.5		47.6		38.5		MHz
	Internal Feedback (f_{CNTS})	D-type	76.9		66.6		47.6		MHz
		T-type	71.4		55.5		43.5		MHz
	No Feedback, $1/(t_{WLS} + t_{WHS})$		83.3		83.3		62.5		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Gate		5		6		8		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock		5		6		8		ns
t_{GOA}	Product Term Gate to Output (Note 2)			16		19		22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		8		9		12		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate		7		10		13		ns
t_{HLS}	Latch Data Hold Time Using Global Gate		0		0		0		ns
t_{GOS}	Gate to Output (Note 3)			10		11		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		6		6		8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch			14		17		22	ns
t_{SIR}	Input Register Setup Time		2		2		2		ns
t_{HIR}	Input Register Hold Time		2		2		2		ns
t_{ICO}	Input Register Clock to Combinatorial Output			14		17		22	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (Continued)

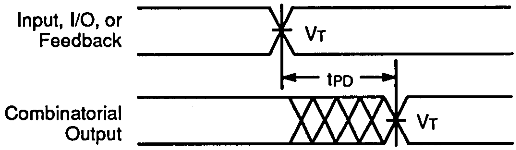
Parameter Symbol	Parameter Description		-12 Min.	-12 Max.	-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
t_{ICS}	Input Register Clock to Output Register Setup	D-type	9		12		15		ns
		T-type	10		14		17		ns
t_{WICL}	Input Register Clock Width	LOW	6		6		8		ns
t_{WICH}		HIGH	6		6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	83.3		83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time		2		2		2		ns
t_{HIL}	Input Latch Hold Time		2		2		2		ns
t_{IGO}	Input Latch Gate to Combinatorial Output			14		17		22	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			16		19		24	ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Latch Gate		7		8		10		ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		7		8		10		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Global Output Latch Gate		9		12		15		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		9		12		15		ns
t_{WIGZ}	Input Latch Gate Width LOW		6		6		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			16		19		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			16		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 3)		12		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)		8		10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			16		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 3)		12		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 3)		8		10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 2)		2	12	2	15	3	20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 2)		2	12	2	15	3	20	ns

Notes:

1. See Switching Test Circuit, page 112, for test conditions.
2. Parameters measured with 16 outputs switching.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

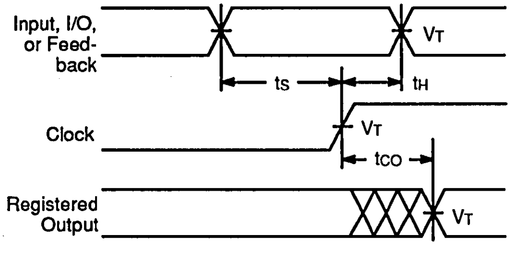
GENERAL INFORMATION

SWITCHING WAVEFORMS



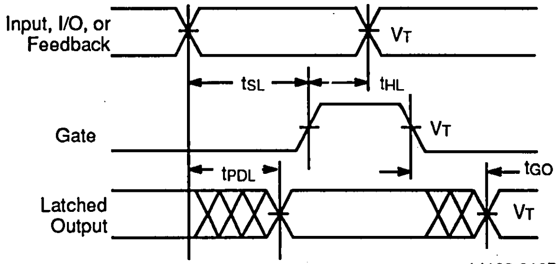
14128-010B

Combinatorial Output



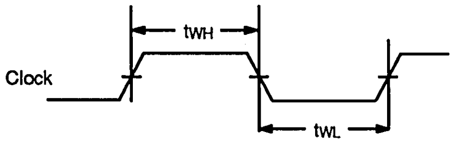
14128-011B

Registered Output



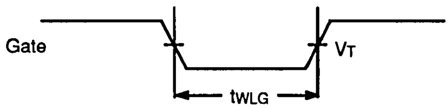
14128-012B

Latched Output (MACH 2 only)



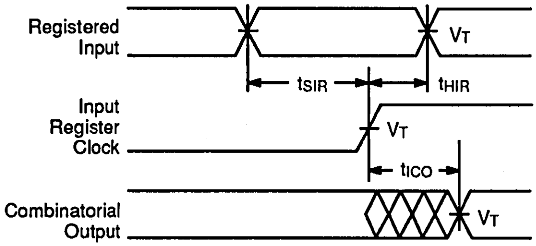
12015-011A

Clock Width



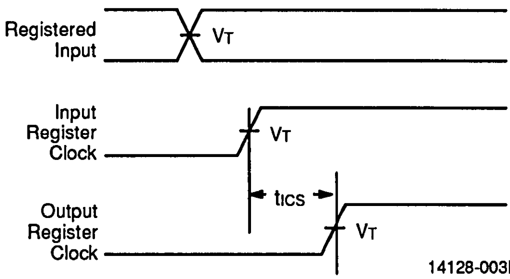
14128-014A

Gate Width (MACH 2 only)



14128-002B

Registered Input (MACH 2 only)



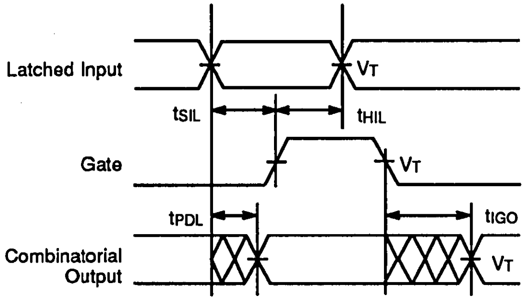
14128-003B

Input Register to Output Register Setup (MACH 2 only)

Notes:

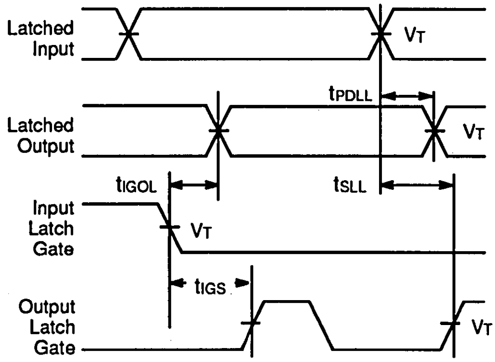
1. $V_T = 1.5$ V.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–4 ns typical.

SWITCHING WAVEFORMS



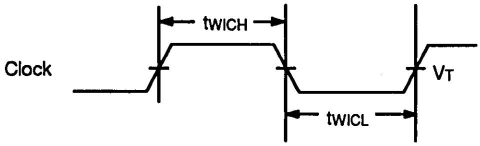
14128-016A

Latched Input (MACH 2 only)



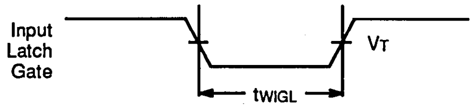
14128-017B

Latched Input and Output (MACH 2 only)



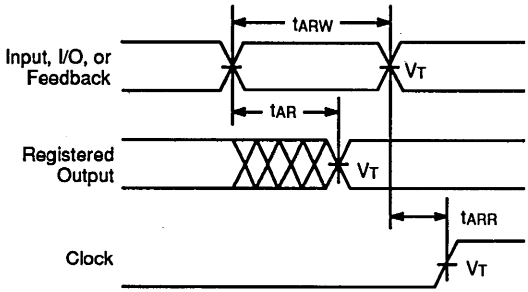
14128-003B

Input Register Clock Width (MACH 2 only)



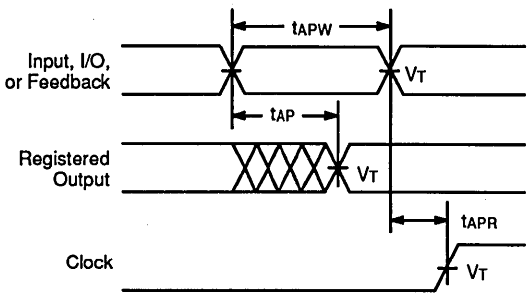
14128-018A

Input Latch Gate Width (MACH 2 only)



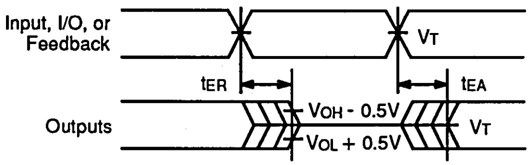
14128-005B

Asynchronous Reset



14128-006B

Asynchronous Preset



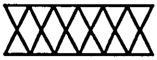
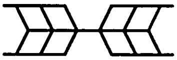
14128-019A

Output Disable/Enable

Notes:

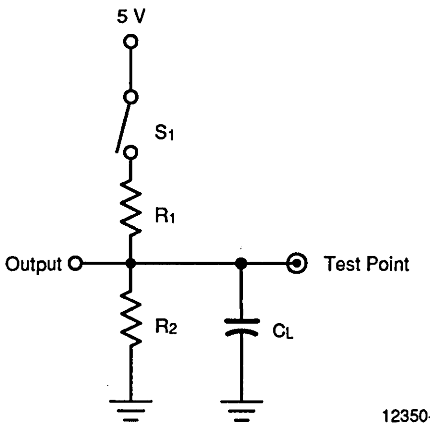
1. V_T = 1.5 V.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–4 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



12350-019A

<table>
<tr><th rowspan="2">Specification</th><th rowspan="2">S_1</th><th rowspan="2">C_L</th><th colspan="2">Commercial</th><th colspan="2">Military</th><th rowspan="2">Measured Output Value</th></tr>
<tr><th>R_1</th><th>R_2</th><th>R_1</th><th>R_2</th></tr>
<tr><td>t_{PD}, t_{CO}</td><td>Closed</td><td rowspan="2">35 pF</td><td rowspan="3">300 Ω</td><td rowspan="3">390 Ω</td><td rowspan="3">390 Ω</td><td rowspan="3">750 Ω</td><td>1.5 V</td></tr>
<tr><td>t_{EA}</td><td>Z → H: Open
Z → L: Closed</td><td>1.5 V</td></tr>
<tr><td>t_{ER}</td><td>H → Z: Open
L → Z: Closed</td><td>5 pF</td><td>H → Z: V_{OH} − 0.5 V
L → Z: V_{OL} + 0.5 V</td></tr>
</table>

f_{MAX} PARAMETERS

The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

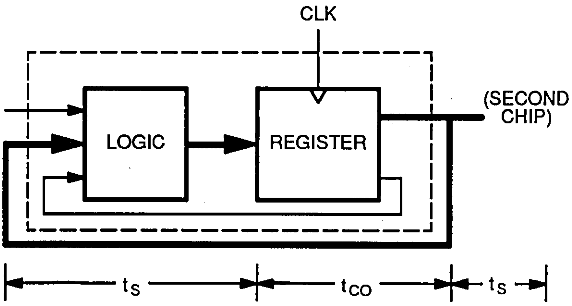
The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external".

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal". A simple internal counter is a good example of this type of design; therefore, this parameter is sometimes called "f_{CNT}".

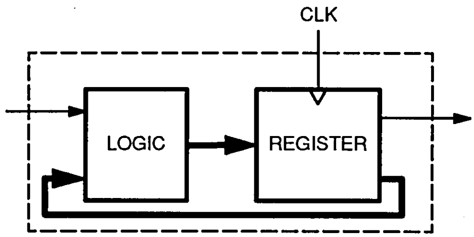
The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback".

For devices with input registers, one additional f_{MAX} parameter is specified: f_{MAXIR}. Because this involves no feedback, it is calculated the same way as f_{MAX} no feedback. The minimum period will be limited either by the sum of the setup and hold times ($t_{SIR} + t_{HIR}$) or the sum of the clock widths ($t_{WICL} + t_{WICH}$). The clock widths are normally the limiting parameters, so that f_{MAXIR} is specified as $1/(t_{WICL} + t_{WICH})$. Note that if both input and output registers are use in the same path, the overall frequency will be limited by t_{ICS}.

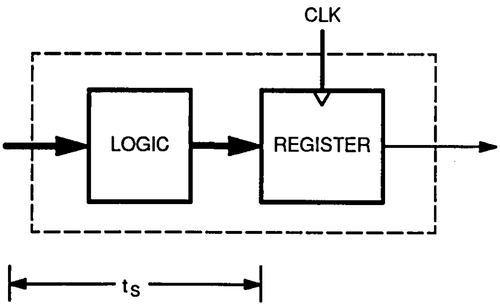
All frequencies except f_{MAX} internal are calculated from other measured AC parameters. f_{MAX} internal is measured directly.



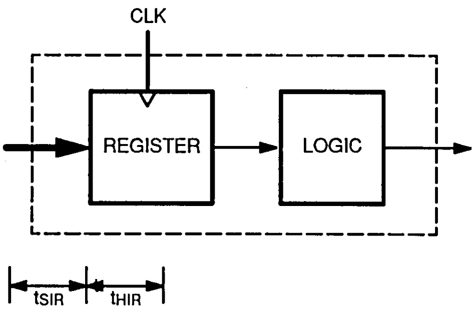
f_{MAX} External; $1/(t_S + t_{CO})$



f_{MAX} Internal (f_{CNT})



f_{MAX} No Feedback; $1/(t_S + t_H)$ or $1/(t_{WH} + t_{WL})$



f_{MAXIR} ; $1/(t_{SIR} + t_{HIR})$ or $1/(t_{WICL} + t_{WICH})$

12350-023B

APPROXIMATING ACTUAL APPLICATION SUPPLY CURRENT

The specifications for a MACH device give the worst-case supply current while the device is static. Dynamic operation is also important, especially on large devices like this that have many signals. However, using simple I_{CC} vs Frequency curves is difficult, since there is great variation in behavior between a few outputs switching and all outputs switching. In addition, real-life devices have outputs that switch at different frequencies, making it difficult to assess an actual frequency for the device as a whole. Breaking the current down into its components gives a much more accurate result than trying to define a "typical" pattern.

The following formula gives you a way to approximate the actual supply current that your application will require. It is not necessary to go through all of the calculations if you do not desire to. Each component is independent, and only those components you are concerned with need be calculated.

Note that the concept of frequency used below is a little different from that normally discussed with PLDs: it generally does not refer to the clock frequency. The frequency of each individual signal must be considered, since in most designs, the different signals operate at widely differing frequencies. In many cases, a signal is not even periodic. In that case, an approximation as to the "average" frequency should be made.

There are six new parameters that are used in this formula. Values for the parameters for each product are given at the end of each individual data sheet. Note that they are typical numbers, and are not tested. The new parameters are:

I_{CC0} The base static I_{CC} at 25°C and 5.0 V V_{CC}, in mA.

i_I The incremental current for a single input switching, but not driving logic, in µA/MHz.

i_B The incremental current for each PAL block that an input or feedback signal drives, in µA/MHz.

i_O The incremental current for a single output switching an unloaded output, but not driving feedback logic, in µA/MHz.

i_V The current change due to changes in V_{CC}, in %/V.

i_T The change in current due to changes in temperature, in %/°C.

The following components of the total current are considered:

- the basic DC current, I_{CC0}
- the AC components for the inputs
- the AC components for the outputs
- V_{CC} derating
- temperature derating
- the output load

Calculating the AC Components

The AC components are a result of inputs and outputs switching.

Contribution of Inputs

The incremental current due to a switching input or buried feedback signal x can be calculated as:

$$i_{Ix} = (i_I + N_{BX}\, i_B)\, f_{Ix}$$

where

i_{Ix} is the total incremental current for input x

N_{BX} is the number of PAL blocks that input x drives

f_{Ix} is the average frequency of input x (not the clock frequency)

The number of blocks driven by an input, also known as the block fanout, can be determined from the MACH Report generated by the MACH Fitter after the design has been successfully fit. The fanout for each individual input is in the "Blocks" column on the far right of the "Signals—Tabular Information" table. Each block that the input drives is listed here. Note that with some devices you may see blocks in this list that you would not expect from the logic equations and signal placement. This is a normal part of the fitting process, and does not affect the logic in any way, but should be accounted for in the current calculation.

The current is calculated for each switching input and buried feedback signal; the results for each input should be summed to give the total incremental current due to switching inputs:

$$i_{IT} = \sum_{x}^{\text{inputs \& buried}} i_{Ix}$$

A short-cut calculation is also possible if you can determine an "average" frequency that you can apply to all inputs, and if you can tolerate less accuracy than that given by the calculation above. Given such a single average frequency f_A, you can estimate the input contribution to current with the calculation

$$i_{IT} = (N_I i_I + N_{TBF} i_B)\, f_A$$

where

N_I is the number of inputs used

N_{TBF} is the total block fanout

The total block fanout is listed in the MACH Report that the AMD Fitter generates, just before the "Signals—Tabular Information" table. It is simply the sum of all the fanouts of the individual inputs.

An example of the part of the report that gives fanout information follows.

```
•
•
•
Wiring Completion:   100% -> (   0 nc)

|>  INFORMATION F058 - Total Block Fanout (All Signals) *: 40          <--

***Signals - Tabular Information

    Signal      #      P/N #     (Loc)        Type       Logic    # PT    Blocks
     CLK1       1       35       I  5      clock pin       .        .       ...
     COUNT      2       13       I  2        input         .        .       .AB     <--
     LOAD       3       10       I  0        input         .        .       .AB     <--
•
•
•
```

In this example, N_{TFB} is 40 for the short-cut calculation. If input contributions are to be considered individually, then N_B for inputs COUNT and LOAD is 2, since both inputs drive blocks A and B. So out of the total fanout of 40, COUNT and LOAD account for 4.

Contribution of outputs

The incremental current for an output *y* is calculated as

$$i_{Oy} = i_O f_{Oy}$$

where

i_{Oy} is the incremental current for output *y*

f_{Oy} is the average frequency at which output *y* is switching (not the clock frequency)

This is calculated for each switching output; the results for each output should be summed to give the total incremental current due to switching outputs:

$$i_{OT} = \sum_{y}^{outputs} i_{Oy}$$

The total AC current under nominal conditions (5.0 V Vcc, 25°C, 35-pF load) is then

$$I_{CCN} = I_{CC0} + i_{IT} + i_{OT}$$

Derating for Vcc

The current will change with applied Vcc. To estimate the current at a given applied Vcc (V_a), calculate the following:

$$I_{CCV} = I_{CCN}\,[1 + i_V\,(V_a - 5.0\text{ V})]$$

where

I_{CCV} is the total dynamic current derated only for Vcc

Derating for Temperature

To estimate the current at an applied temperature T_a, calculate the following:

$$I_{CCT} = I_{CCN}\,[1 + i_T\,(T_a - 25°C)]$$

or

$$I_{CCVT} = I_{CCV}\,[1 + i_T\,(T_a - 25°C)]$$

where

I_{CCT} is the total current derated only for temperature

I_{CCVT} is the total current derated for both Vcc and temperature

Note that i_T will be a negative number, since current increases as temperature decreases.

Calculating the Load Current

A load may have both capacitive and resistive portions, both of which draw current.

Capacitive load contribution

The dynamic current of a purely capacitive output load on an output *w* can be calculated as:

$$i_{CLw} = C_{Lw} V_{Sw} f_{Ow}$$

where

i_{CLw} is the incremental current due to the capacitive load on output *w*

C_{Lw} is the amount of capacitance on output *w*

V_{Sw} is the voltage swing of output *w*

f_{Ow} is the average frequency at which output *w* is switching (not the clock frequency)

Resistive load contribution

If there is a resistive component to the load, then there will be a current component that can be calculated as follows for an output w with a single resistor:

$$i_{RLw} = K_{DCw}\frac{V_O}{R_w}$$

where

i_{RLw} is the current due to the resistive load on output w

K_{DCw} is the average duty cycle for output w being HIGH in the case of a resistor to ground, or LOW in the case of a resistor to V_{CC}

V_O is V_{OH} in the case of a resistor to ground, or V_{OL} in the case of a resistor to V_{CC}

R_w is the value of the terminating resistor on output w

If there is a resistor network with Thévenin equivalent resistance R_{eq} and voltage V_{eq}, then the current can be calculated as:

$$i_{RLw} = \frac{K_{DCH}\,(V_{OH} - V_{eq}) + (1 - K_{DCH})\,(V_{eq} - V_{OL})}{R_{eq}}$$

where

K_{DCH} is the average duty cycle for output w being HIGH

The total current due to the load is then

$$i_{LT} = \sum_{w}^{outputs} i_{CLw} + i_{RLw}$$

Load currents can be derated for temperature, but the behavior of the load with temperature may not be available.

Summary

To get the best approximation of supply current, two fundamental components must be added: current drawn by the chip, and current drawn by the load. The former is a combination of static current and dynamic current from inputs and outputs switching. The latter is a function of the voltage swing and the kind of load. The sum of the two should give a reasonable idea of the actual supply current requirements for your application.

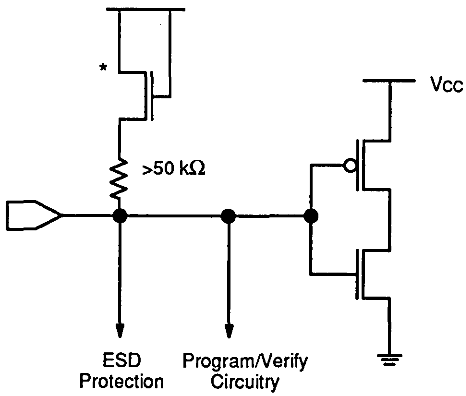
ENDURANCE CHARACTERISTICS

The MACH 1 and MACH 2 families are manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed, a feature which allows 100% testing at the factory.

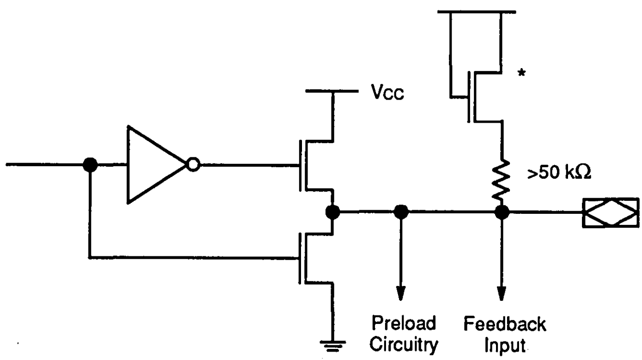
Endurance Characteristics

Parameter Symbol	Parameter Description	Min.	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature (Military)
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Input



Output

*Pull-up resistor circuit on MACH220 and MACH215 only

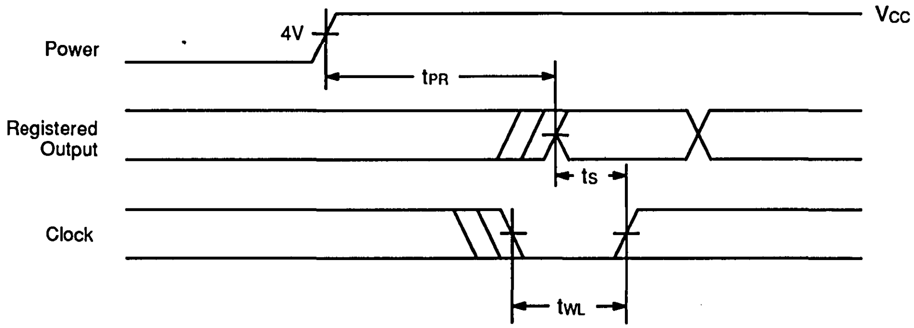
12197-013A

POWER-UP RESET

The MACH devices have been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways Vcc can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The Vcc rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max.	Unit
t_{PR}	Power-Up Reset Time	10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

USING PRELOAD AND OBSERVABILITY

In order to be testable, a circuit must be both controllable and observable. To achieve this, the MACH devices incorporate register preload and observability.

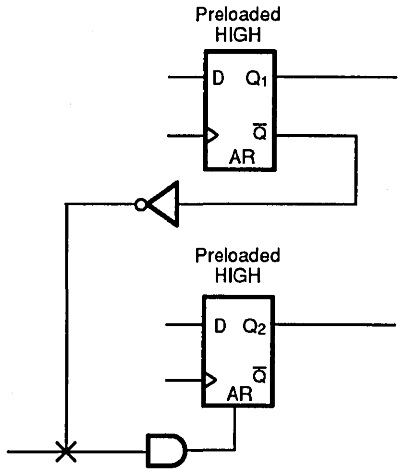
In preload mode, each flip-flop in the MACH device can be loaded from the I/O pins, in order to perform functional testing of complex state machines. Register preload makes it possible to run a series of tests from a known starting state, or to load illegal states and test for proper recovery. This ability to control the MACH device's internal state can shorten test sequences, since it is easier to reach the state of interest.

The observability function makes it possible to see the internal state of the buried registers during test by overriding each register's output enable and activating the output buffer. The values stored in output and buried registers can then be observed on the I/O pins. Without this feature, a thorough functional test would be impossible for any designs with buried registers.

While the implementation of the testability features is fairly straightforward, care must be taken in certain instances to insure valid testing.

One case involves asynchronous reset and preset. If the MACH registers drive asynchronous reset or preset lines and are preloaded in such a way that reset or preset are asserted, the reset or preset may remove the preloaded data. This is illustrated in Figure 21. Care should be taken when planning functional tests, so that states that will cause unexpected resets and presets are not preloaded.

Another case to be aware of arises in testing combinatorial logic. When an output is configured as combinatorial, the observability feature forces the output into registered mode. When this happens, all product terms are forced to zero, which eliminates all combinatorial data. For a straight combinatorial output, the correct value will be restored after the preload or observe function, and there will be no problem. If the function implements a combinatorial latch, however, it relies on feedback to hold the correct value, as shown in Figure 22. As this value may change during the preload or observe operation, you cannot count on the data being correct after the operation. To insure valid testing in these cases, outputs that are combinatorial latches should not be tested immediately following a preload or observe sequence, but should first be restored to a known state.



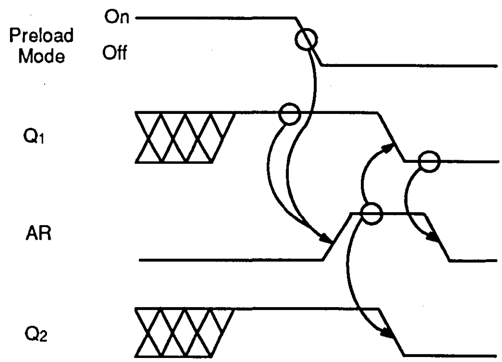


Figure 21. Preload/Reset Conflict

14051F-021A

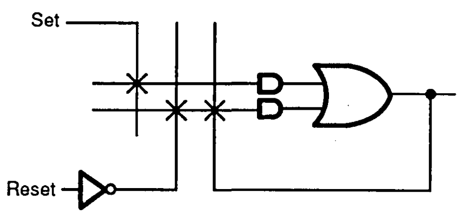


Figure 22. Combinatorial Latch

14051F-022A

DEVELOPMENT SYSTEMS (subject to change)

For more information on the products listed below, please consult the AMD FusionPLD catalog.

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEM (Note 1)	
Advanced Micro Devices, Inc. 901 Thompson Place MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	PALASM 4 Software MACH Libraries and Interface to OrCAD/SDT™ III Software (Optional) (Note 2)	MACH110: Rev. 1.0 MACH120: Rev. 1.4 MACH130: Rev. 1.2 MACH210: Rev. 1.1 MACH215: Rev. 1.5 MACH220: Rev. 1.5 MACH230: Rev. 1.4
Cadence Design Systems 555 River Oaks Pkwy San Jose, CA 95134 (408) 943-1234	ComposerPLD™ Option (Requires SmartPart™ MACH Fitter) SystemPGA™	MACH110: Future MACH120: Future MACH130: Future MACH210: Future MACH215: Future MACH220: Future MACH230: Future
Capilano Computing 960 Quayside Dr., Suite 406 New Westminster, B.C. Canada V3M 6G2 (800) 444-9064 or (604) 552-6200	MacABEL™ Software (Requires SmartPart MACH Fitter)	MACH110: Rev. 4.11 MACH120: Rev. 4.11 MACH130: Rev. 4.11 MACH210: Rev. 4.11 MACH215: Future MACH220: Rev. 4.12 MACH230: Rev. 4.11
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	ABEL™ Software (Requires SmartPart MACH Fitter)	MACH110: Rev. 4.12 MACH120: Rev. 4.12 MACH130: Rev. 4.12 MACH210: Rev. 4.12 MACH215: Rev. 4.12 MACH220: Rev. 4.12 MACH230: Rev. 4.12
ISDATA GmbH Daimlerstr. 51 W7500 Karlsruhe 21 Germany 0721/75 10 87 (206) 863-8447 (SMS North America)	LOG/iC™ Software (Requires MACH Fitter)	MACH110: Rev. 3.4 MACH120: Future MACH130: Rev. 3.4 MACH210: Rev. 3.4 MACH215: Future MACH220: Future MACH230: Future
Logical Devices Inc. 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	CUPL™ Software	MACH110: Rev. 4.2A MACH120: Rev. 4.3 MACH130: Rev. 4.2A MACH210: Rev. 4.2A MACH215: Future MACH220: Future MACH230: Rev. 4.3
Mentor Graphics Corp. 8005 S.W. Beckman Rd. Wilsonville, OR 97070-777 (800) 345-2308	PLDSynthesis™	MACH110: Future MACH120: Future MACH130: Future MACH210: Future MACH215: Future MACH220: Future MACH230: Future
MINC Incorporated 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (719) 590-1155	PGADesigner™ Software	MACH110: Rev. 2.1A MACH120: Rev. 3.0 MACH130: Rev. 2.1A MACH210: Rev. 2.1A MACH215: Future MACH220: Rev. 3.0 MACH230: Rev. 3.0
OrCAD 3175 N.W. Aloclek Dr. Hillsboro, OR 97124 (503) 690-9881	Programmable Logic Design Tools Schematic Design Tool	MACH110: Rev. IV MACH120: Future MACH130: Future MACH210: Rev. IV MACH215: Future MACH220: Future MACH230: Future
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 442-4660 or (504) 480-0881	ViewPLD Synthesis (Requires SmartPart MACH Fitter)	MACH110: Available MACH120: Available MACH130: Available MACH210: Available MACH215: Future MACH220: Available MACH230: Available

DEVELOPMENT SYSTEMS (subject to change) (Continued)

MANUFACTURER	BOARD-LEVEL SIMULATION PACKAGE	
Aldec Company, Inc. 3525 Old Conejo Rd., Suite 111 Newbury Park, CA 91320 (805) 499-6867	SUSIE™	MACH110: Rev. 6.1 MACH120: Future MACH130: Rev. 6.1 MACH210: Rev. 6.1 MACH215: Future MACH220: Future MACH230: Rev. 6.1
Cadence Design Systems 555 River Oaks Pkwy San Jose, CA 95134 (408) 943-1234	Models available through Logic Modeling	
Logic Modeling 19500 NW Gibbs Dr. P.O. Box 310 Beaverton, OR 97075 (503) 690–6900	SmartModel® Library	MACH110: Available MACH120: Available MACH130: Available MACH210: Available MACH215: Future MACH220: Available MACH230: Available
OrCAD 3175 N.W. Aloclek Dr. Hillsboro, OR 97124 (503) 690-9881	Digital Simulation Tools (Requires OrCAD/MOD)	MACH110: Rev. 4.03 MACH120: Future MACH130: Future MACH210: Rev. 4.03 MACH215: Future MACH220: Future MACH230: Future
Productivity Through Automation Corp. 175 Southfield Rd. Concord, MA 01742 (508) 371-9881	VERMOD (JEDEC-to-Verilog translator)	MACH110: Available MACH120: Available MACH130: Available MACH210: Available MACH215: Future MACH220: Available MACH230: Available
Teradyne EDA 321 Harrison Ave. Boston, MA 02118 (800) 777-2432 or (617) 422-2793	MultiSIM Interactive Simulator LASAR	MACH110: Future MACH120: Future MACH130: Future MACH210: Future MACH215: Future MACH220: Future MACH230: Future
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 442-4660 or (504) 480-0881	ViewSim Models available through Logic Modeling	
MANUFACTURER	**TEST GENERATION SYSTEM**	
Acugen Software, Inc. 427-3 Amherst St., Suite 391 Nashua, NH 03063 (603) 891-1995	ATGEN™ Test Generation Software	MACH110: Available MACH120: Available
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	Contact Data I/O	

Advanced Micro Devices is not responsible for any information relating to the products of third parties. The inclusion of such information is not a representation nor an endorsement by AMD of these products.

Notes:

1. Contact manufacturer for support of devices not listed for that manufacturer.
2. Supports only rev. 3.22 of OrCAD/SDT III.

APPROVED PROGRAMMERS (subject to change)

For more information on the products listed below, please consult the AMD FusionPLD catalog.

MANUFACTURER	PROGRAMMER CONFIGURATION	
Advanced Micro Devices 901 Thompson Pl. Sunnyvale, CA 94088 (800) 222-9323 or (408) 732-2400	LabPro™ (Note 1) MACH110: Rev. 1.2 MACH120: Rev. 1.3 MACH210: Rev. 1.3	
Advin Systems, Inc. 1050-L East Duane Ave. Sunnyvale, CA 94086 (408) 243-7000	U40 MACH110: Rev. 10.10 MACH120: Rev. 10.21 MACH130: Rev. 10.10 MACH210: Rev. 10.10 MACH230: Rev. 10.22	U84 MACH110: Rev. 10.10 MACH120: Rev. 10.21 MACH130: Rev. 10.21 MACH210: Rev. 10.21 MACH230: Rev. 10.39
BP Microsystems 10681 Haddington, Suite #190 Houston, TX 77043 (800) 225-2102 or (713) 461-9430	CP-1128/PLD-1128 (Note 1) MACH110: Rev. 1.55 MACH120: Rev. 1.86 MACH130: Rev. 1.86 MACH210: Rev. 1.86 MACH220: Rev. 1.94 MACH230: Rev. 1.94	
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	UniSite™ (Note 2) MACH110: Rev. 3.2 MACH120: Rev. 3.6 MACH130: Rev. 3.4 MACH210: Rev. 3.3 MACH215: Rev. 3.8x MACH220: Rev. 3.8x MACH230: Rev. 3.6 Model 2900 MACH110: Rev. 1.2 MACH130: Rev. 1.9 MACH210: Rev. 1.4 Model 29 (Note 1) LogicPak™ 303A–011A MACH110: V14 MACH210: V15	Family-Pinout Codes: MACH110: 17F-0BD MACH120: 1F1-1F1 MACH130: 194-0F6 MACH210: 194-0C1 MACH230: 194-0F2 MACH110: 7F-BD MACH130: 194-0F6 MACH210: 94-C1
Logical Devices Inc. 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	ALLPRO™ (Note 1) MACH110: Rev. 2.1 MACH210: Rev. 2.1	ALLPRO88 MACH110: Rev. 2.1 MACH210: Rev. 2.1 MACH130: Rev. 2.1B MACH230: Rev. 2.1B
Micropross Parc d'Activite des Pres 5, rue Denis-Papin 59650 Villeneuve-d'Ascq, France (20) 47.90.40	Contact Manufacturer	
SMS North America, Inc. 16522 NE 135th Place Redmond, WA 98052 (800) 688-3122 or (214) 233-3122 or SMS Im Morgental 13 D-8994 Hergatz, Germany 07522-5018	Expert MACH110: Rev. 1/92 MACH130: Rev. 1/92 MACH210: Rev. 1/92 MACH230: Rev. 1/92	

Notes:

1. Requires socket adapter.
2. Requires 12 pin driver boards.

APPROVED PROGRAMMERS (subject to change) (Continued)

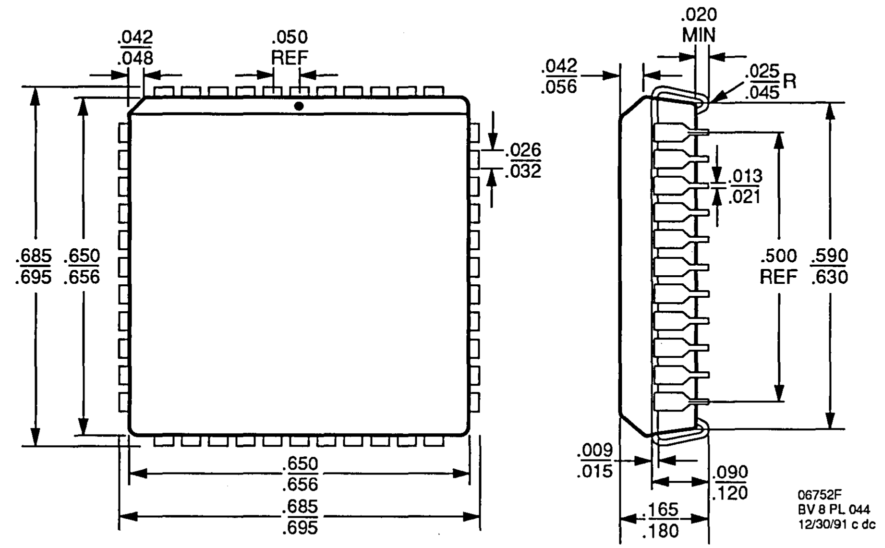
MANUFACTURER	PROGRAMMER CONFIGURATION	
Stag Microsystems Inc. 1600 Wyatt Dr. Suite 3 Santa Clara, CA 95054 (408) 988-1118 or Stag House Martinfield, Welwyn Garden City Herfordshire UK AL7 1JT 707-332148	ZL30A (Note 1) MACH110: Rev. 30A45	Family-Pinout Codes: MACH110: 25253
System General 244 S. Hillview Dr. Milpitas, CA 95035 (408) 263-6667 or 3F, No. 1, Alley 8, Lane 45 Bao Shing Rd., Shin Diau Taipei, Taiwan 2-917-3005	MACH110: Rev. 1.50 MACH210: Rev. 1.50	

PROGRAMMER SOCKET ADAPTERS (subject to change)

MANUFACTURER	PART NUMBER
CTI 14425 N. Scottsdale Rd. Suite 300 Scottsdale, AZ 85260 (602) 998–1484	MACH110/210: (44-Pin to 28-Pin) PLCC: PD1065-0
Emulation Technology 2344 Walsh Ave., Bldg. F Santa Clara, CA 95051 (408) 982–0660	MACH110/210: (44-Pin to 28-Pin) PLCC: AS-44-28-01P-3 CQFP: AS-44-28-01F2-3 MACH130/230: (84-Pin to 28-Pin) PLCC: AS-84-28-01P-6
Logical Systems 1201 East Fayette St. Syracuse, NY 13210 (315) 478-0722	MACH110/210: (44-Pin to 28-Pin) PLCC: PA-MACH210
Procon Technologies, Inc. 1333 Lawrence Expwy, Suite 207 Santa Clara, CA 95051 (408) 246-4456	MACH110/210: (44-Pin to 28-Pin) PLCC: 325-044-1221-028A CQFP: 327-044-1121-028A MACH120/220: (68-Pin to 28-Pin) PLCC: 325-068-1221-028A MACH130/230: (84-Pin to 28-Pin) PLCC: 325-084-1221-028A CQFP: 327-084-1121-028A

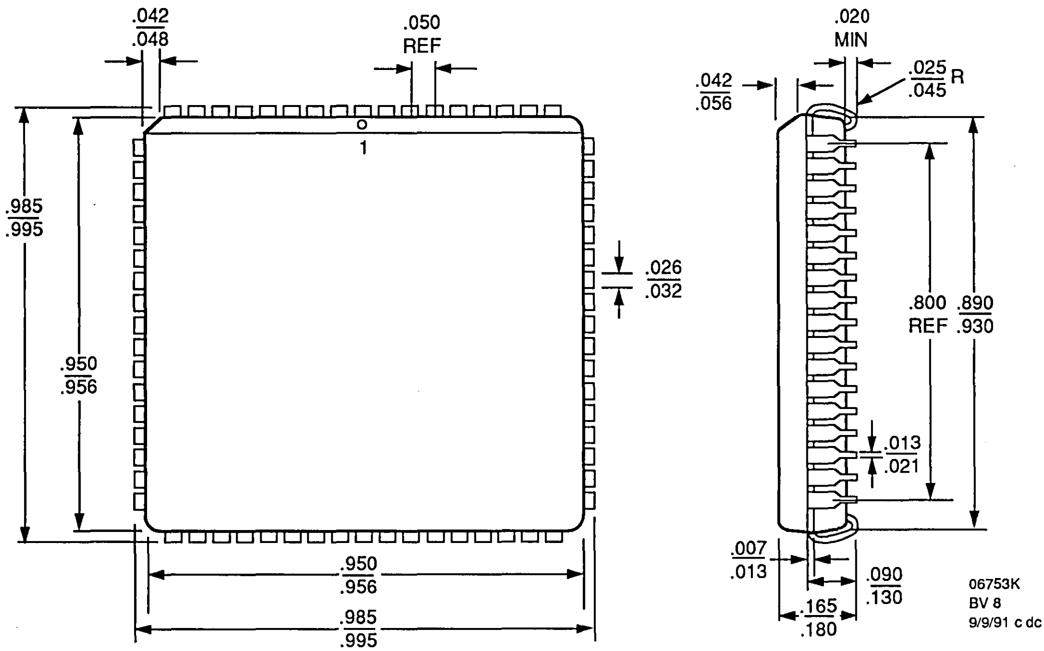
PHYSICAL DIMENSIONS*

PL 044
44-Pin Plastic Leaded Chip Carrier

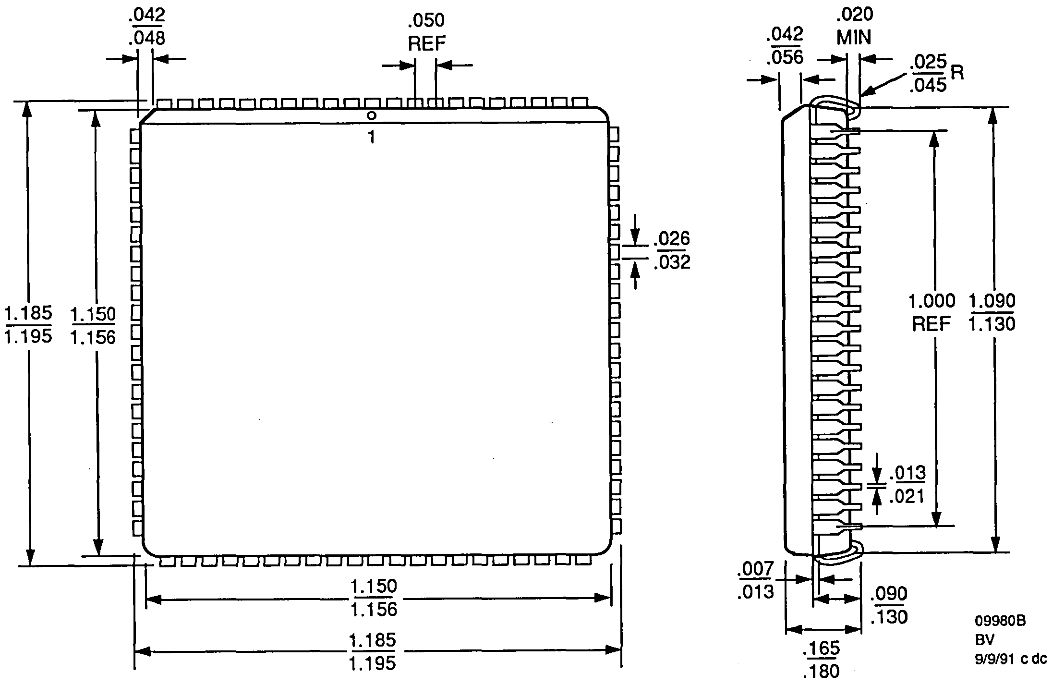


TOP VIEW   SIDE VIEW

PL 068
68-Pin Plastic Leaded Chip Carrier

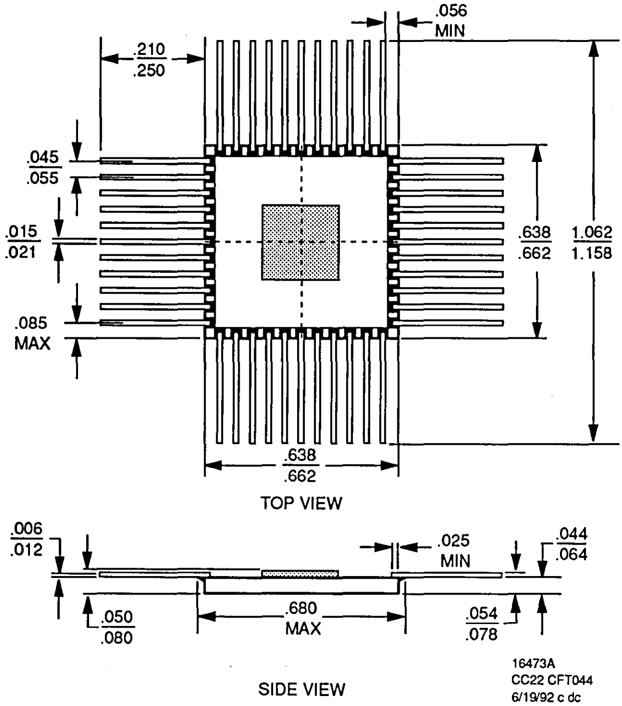


PHYSICAL DIMENSIONS*
PL 084
84-Pin Plastic Leaded Chip Carrier



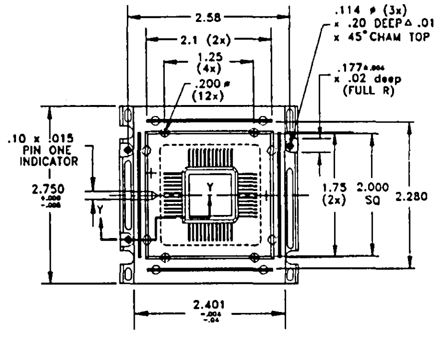
* For reference only. All dimensions are measured in inches. BSC is an ANSI standard for Basic Spacing Centering.

PHYSICAL DIMENSIONS*
CFT044
44-Pin Ceramic Top-Brazed Flatpack

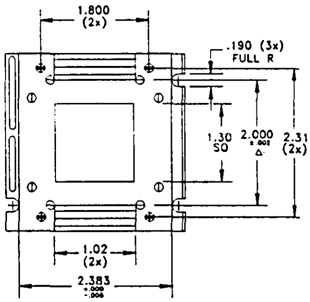


* For reference only. All dimensions are measured in inches. BSC is an ANSI standard for Basic Spacing Centering.

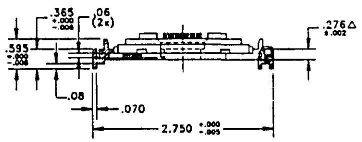
PHYSICAL DIMENSIONS*
Carrier for 44-Pin Top-Brazed Flatpack (CFT044)



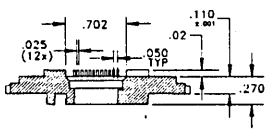
CARRIER TOP VIEW



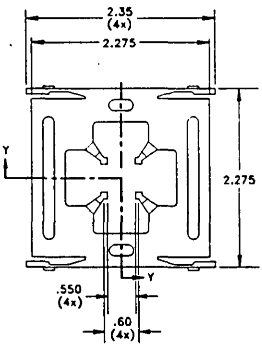
CARRIER BOTTOM VIEW



SECTION Y–Y
DETAILED CROSS SECTION



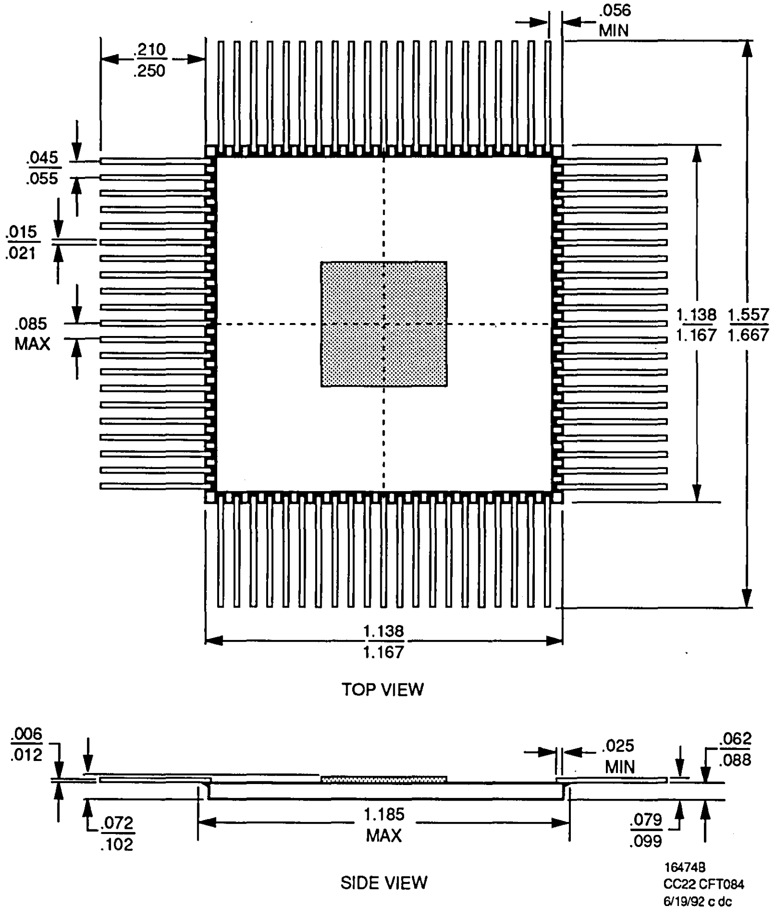
SECTION Y–Y
DETAILED CROSS SECTION
(BOTTOM VIEW)



CLIP TOP VIEW

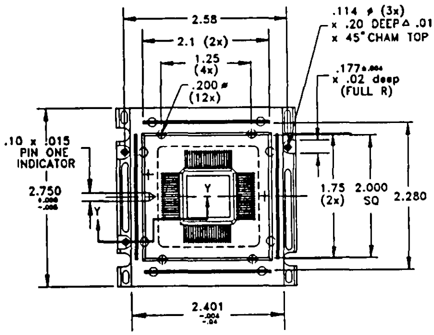
* For reference only. All dimensions are measured in inches. BSC is an ANSI standard for Basic Spacing Centering.

PHYSICAL DIMENSIONS*
CFT084
84-Pin Ceramic Top-Brazed Flatpack

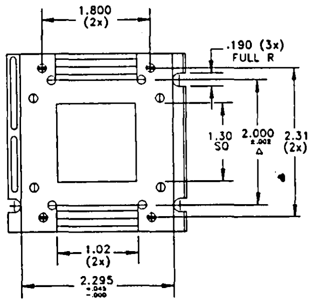


* For reference only. All dimensions are measured in inches. BSC is an ANSI standard for Basic Spacing Centering.

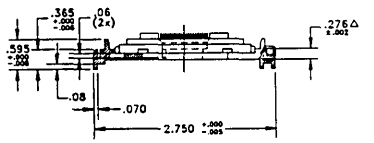
PHYSICAL DIMENSIONS*
Carrier for 84-Pin Top-Brazed Flatpack (CFT084)



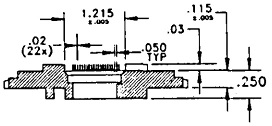
CARRIER TOP VIEW



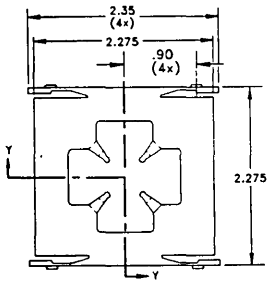
CARRIER BOTTOM VIEW



SECTION Y–Y
DETAILED CROSS SECTION



SECTION Y–Y
DETAILED CROSS SECTION
(BOTTOM VIEW)



CLIP TOP VIEW

* For reference only. All dimensions are measured in inches. BSC is an ANSI standard for Basic Spacing Centering.

MACH™ Device Design Planning Guide

Jerry Vea, PLD Software Applications Engineer, Advanced Micro Devices, Inc.

1.0 INTRODUCTION

This technical brief provides planning guidelines for a MACH device design that will lead to its successful implementation. The method presented estimates whether logic will fit in a MACH device before the design has been entered.

The tutorial in this brief is an exhaustive device resource analysis. For many designs, an analysis like this is not practical, and instead, a rough estimation of pins, product term clusters (see definition in section 3.2), reset, preset, and tristate resources is used to predict fitting.

- The planning-process overview in discussion 2 introduces you to the differences between planning PAL® device designs and MACH-device designs.
- A counter design is used in discussion 3 to illustrate the MACH design planning process.
- Discussion 4 is a summary.
- The appendices provide the complete PALASM® 4 software .PDS design file and MACH Fitter report.

As a reader, you should be familiar with the MACH devices and architectures described in the MACH Family Data Book. You should also know how to count/estimate the number of product terms (PTs) in a design.

2.0 DESIGN PLANNING PROCESS OVERVIEW

The MACH design planning process applied in it's full detail differs from a standard PAL device design process as shown in Figure 20.

PAL devices have a universal internal interconnect while MACH devices provide a reduced interconnect through the switch matrix. The block partitioning steps used when you're estimating with a high degree of detail (as in the following tutorial) are not required when estimating a single PAL device design. Note, however, that if multiple PAL devices are used in a design, similar partitioning steps between PAL devices are necessary.

Both the PAL and MACH device planning processes begin with a well-defined high-level design. You analyze and count the resources required for the design and select an appropriate device.

Block Partitioning Steps *(optional, for detailed planning):*

- Once a MACH device is selected, you begin design partitioning by determining which of the partitioning constraints apply to the design.
- Then you place logic into blocks in a way that maximizes common inputs of equations within the blocks without exceeding the limits of block partitioning constraints.
- Lastly, the resources used in each block are counted.

Manual partitioning is discussed in more detail in the MACH Manual Partitioning Technical Brief.

If the block partitioning steps are performed, you can calculate device and block resources precisely, from which an informed decision may be made as to whether the design will fit. If the block partitioning steps aren't performed, a less reliable decision is made using the information gathered in step 3.2.

3.0 PLANNING A MACH-DEVICE COUNTER DESIGN

The following example illustrates the MACH device planning process in detail. The level of detail in your planning process may vary due to individual design styles and time constraints. Since the design must be entered and the software run to guarantee that the design will fit even if the block partitioning steps have been completed, many users skip the block partitioning steps.

3.1 High-Level Design

Planning begins with a high-level definition of the design. Figure 21 illustrates an 8-bit counter that can be parallel-loaded from I/O pins which also output the count value. The counter counts up or down, based on the control bits, and may be reset or preset. The counter output is decoded to generate several pulse and clock-divide outputs (decoded equations are described and shown in the BUSCNTR.PDS design file in Appendix A).

Publication #	Rev.	Amendment	Issue Date
15967	B	/0	7/92

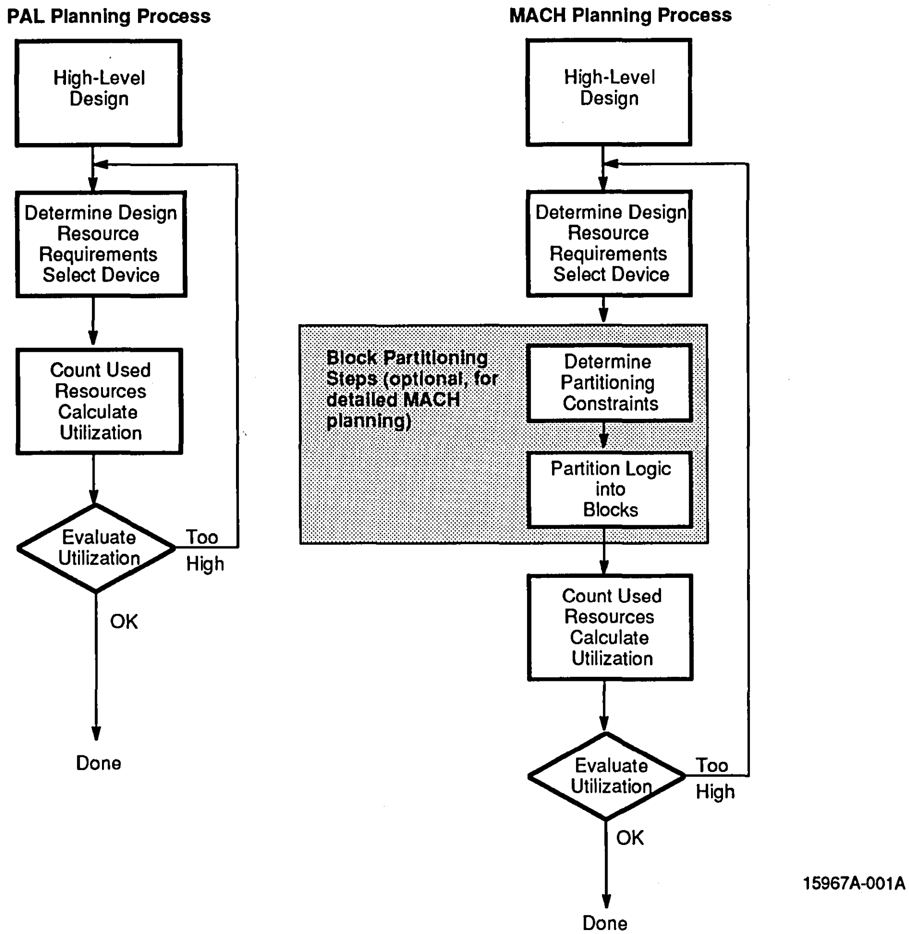


Figure 20. MACH, PAL Device Planning Processes

The counter in this design is implemented using T-type flip-flops rather than D-type because T-type flip-flops require fewer PTs for the hold and count states of each counter bit. Since PTs are required for a T flip-flop only when it changes state, and the most significant bits of a counter do not change during most count states, few PTs are used.

Figure 22 identifies the implementation of each bit in the counter. A T-type flip-flop requires only four PTs: one PT each for counting up and counting down, and two PTs for parallel loading; no PTs are required to hold the macrocell in the same state. In this case, a T-type flip-flop uses less PTs; however, it also reduces the maximum clock frequency of the counter from 76.9 MHz to 71.4 MHz[1].

The count bits are fed back from the counter macrocells via internal feedback and parallel-loaded count values are input via the I/O pins. Each counter macrocell therefore feeds two array inputs simultaneously.

[1] See the MACH Family Data Book for all timing specifications.

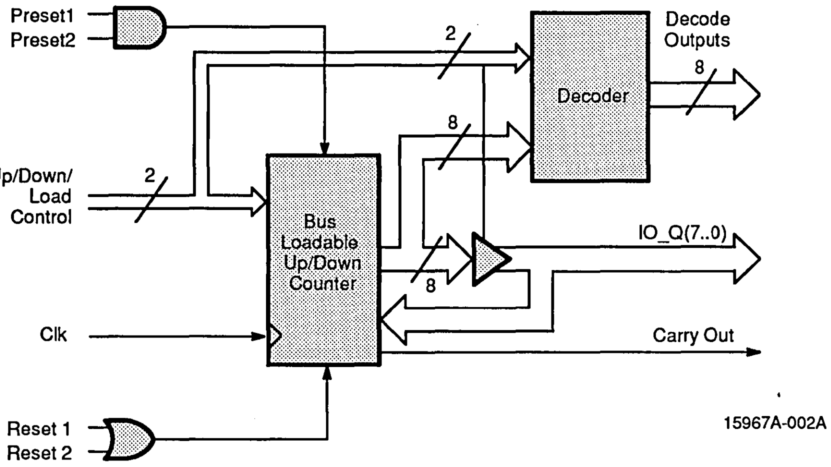


Figure 21. Bus Loadable Up/Down Counter with Decoded Outputs

3.2 Determine Resource Requirements/ Select Device

You must count design resource requirements and match these to an appropriate MACH device. Counting the number of pins, clocks, asynchronous resets and presets, and output enables is a straightforward process. Array input utilization cannot be calculated at this point because the design hasn't been partitioned into blocks.

The group of four PTs associated with each macrocell in a MACH device is called a product-term cluster. One cluster is allocated when from one to four PTs are required by an equation. Each counter bit requires four PTs, or one PT cluster.

Two of the decoded outputs, XORXNOR and Pulse 16, each require more than four PTs. Additional clusters of four product terms each are allocated as needed when the 5th, 9th, etc. PTs are used in an equation. At this point, you must decide whether to estimate the number of PTs used by these equations or reduce the equations to the fewest number of PTs and count them[2]. If you can estimate with a high degree of confidence, the detailed calculation of product terms can be eliminated.

One asynchronous reset PT is available per MACH110 block. In this design, the reset input uses more than one product term and requires an additional product-term cluster, which adds an extra feedback delay to it. The output enable and preset inputs use only one product term; additional product-term clusters are not required.

Resource	Used
Pins	24
PT Clusters	?
Clock	1
Reset	1
Preset	1
Output Enable	1
Array Inputs	?

3.2.1 Product-Term Calculations

When planning your own design, an estimation of product-term requirements may be sufficient. As you use these estimations to analyze device utilization, you should account for the minimization of PTs which will be performed during compilation and may result in fewer PTs than you expected.

Note:

This discussion explains PT estimation in detail. However, counting PT resources in your own designs, for example, in a complicated state-machine design written in high-level syntax, may not prove as straightforward. If counting PTs is difficult, or estimation can be done with a high degree of confidence, you should estimate the number of PT clusters used in your design rather than count them.

Optional steps to calculate the number of PTs required by the sample XORXNOR and Pulse 16 equations are shown below. The sample XORXNOR equation is discussed first.

```
XORXNOR = (((Q0*Q1*Q2*Q3*Q4*Q5) :+: Q6)
          :*:Q7);
```

[2] Because this is a non-trivial task, it is explained in detail under discussion 3.2.1.

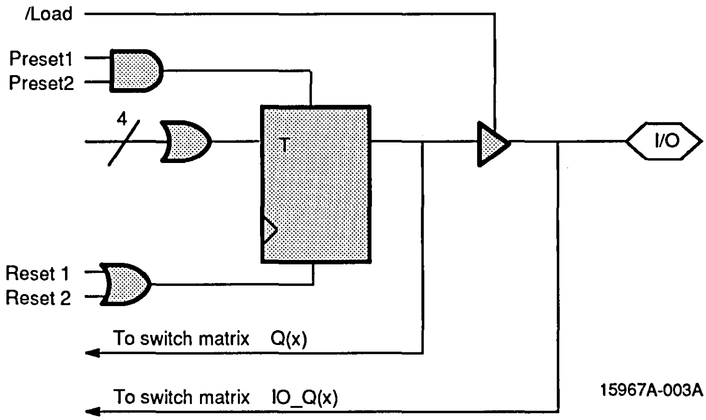


Figure 22. Counter Macrocell

To simplify the equation you set the following, then expand XORXNOR into a sum-of-products form as shown below.

Set

$$A = (Q_0*Q_1*Q_2*Q_3*Q_4*Q_5)$$

XOR Expansion

$$XORXNOR = (A*/Q_6 + /A*Q_6) :*: Q_7$$

XORXNOR Expansion

$$XORXNOR = (A*/Q_6 + /A*Q_6)*Q_7 + (/A + Q_6)*(A + /Q_6)*/Q_7$$

Sum-of-products form

$$XORXNOR = A*/Q_6*Q_7 + A*Q_6*/Q_7 + /A*Q_6*Q_7 + /A*/Q_6*/Q_7$$

/A requires 6 PTs. Therefore, the two latter equations expand into six product terms each.

Since

$$/A = /Q_0 + /Q_1 + /Q_2 + /Q_3 + /Q_4 + /Q_5$$

6 PTs are required for each of the following

$$/A*Q_6*Q_7$$
$$/A*/Q_6*/Q_7$$

The sample XORXNOR equation requires a total of 14 product terms, or four PT clusters. Clearly, terms using XOR and XNOR operators may require many product terms.

Note:

The XORXNOR equation uses more than 12 product terms. Gate splitting and an extra feedback path are required to implement it in a MACH110 device. The maximum clock speed of the counter is reduced if timing-critical signals route through this feedback path.

The Pulse 16 equation is shown next. This equation requires five product terms, or two product-term clusters.

$$Pulse16 = Q_0*Q_1*Q_2*Q_3*/Q_4*Q_5*Q_6 + Q_0*Q_1*Q_2*Q_3*Q_4*/Q_6 + Q_0*Q_1*Q_2*Q_3*/Q_5*/Q_6 + Q_0*Q_1*Q_2*Q_3*/Q_7 + Q_0*Q_1*Q_2*Q_3*Q_4*/Q_5$$

3.2.2 Product-Term Cluster Summary

Following are the product-term cluster requirements for this counter design.

Bus counter Decoded outputs Reset	9 PT clusters 8 + 3 + 1 = 12 PT clusters 1 PT cluster
Total	22 PT clusters used, 69% of the 32 available

3.2.3 Select a Device

A summary of device-resource requirements for this design is shown below. Based on the 70% recommended utilization guideline, it appears this design will fit in a MACH110 device. The only unknown is the number of array inputs, which will be determined using the block partitioning steps.

Resource	Used	MACH110	Utilization
Pins	24	38	63%
PT Clusters	22	32	69%
Clock	1	2	OK
Reset	1	2	OK
Preset	1	2	OK
Output Enable	1	8	OK
Array Inputs	?	22 per block	?

3.3 Determine Partitioning Constraints (*optional*)

Once the device has been selected, you can determine block partitioning constraints. Reset, preset, and output enable signals constrain block partitioning if you use more of the resource than will fit in 1 block. In this design, however, the single reset, preset, and output enable do not constrain logic to a certain block.

The total number of product terms and array inputs used in this design won't fit into one block. Therefore, these resource requirements constrain the partitioning of logic into blocks. A summary of possible partitioning constraints, and those that impact this design, appear next. Note that MACH2XX devices have 7 possible constraints. Pins are a constraint since the user must differentiate between buried and I/O macrocell resources. Macrocells are also a constraint if input registers are used.

In this design, since array inputs and product term clusters are constraints, they will be considered when partitioning the design. The reset, preset, and output enable resources can be ignored.

3.4 Partition Logic into Blocks (*optional*)

Once partitioning constraints have been determined, the logic can be partitioned into blocks within those constraints so array inputs will be minimized.

To minimize array inputs, equations with similar inputs are placed in the same block. If all equations driven by a signal are in one block, the input signal uses only one array input. An additional array input is needed for each additional block a signal drives.

The block diagram in Figure 21 shows a distinct division of logic between the counter and the output decoder. This helps direct the partitioning process. This design can be partitioned in two ways.

A. Place the counter in one block and the decoder in the other.

B. Divide the counter and decoder into bit slices and place half of each into a single block.

Note that the two presets and the ORed reset are not inputs to the output decoder, so grouping the counter logic in one block uses three fewer array inputs than splitting it into two blocks. Therefore, the first partition will be used.

3.5 Count Resources Used, Calculate Utilization (*optional*)

The constraining resources used in each block (product term clusters and array inputs) are now counted.

3.5.1 Count Resources

Counter-block resources are determined before decoder-block resources because the counter block uses more array inputs than the decoder block (8 extra inputs from counter pins), so the logic is more difficult to place. The following analysis applies to the counter block.

Product-term clusters in counter block

8	$Q_{(7...0)}$
+1	carry out
9	

Array inputs in counter block

8 * 2	$IO\_Q_{(7...0)}$, $Q_{(7...0)}$
3	reset, preset1, preset2
+ 2	control signals
21	

Possible Constraints	Used	# Provided in 1 block	Constraint in Counter? (more than will fit in 1 block)
Product-Term Clusters	24	16	Yes
Asynchronous Resets	1	2	No
Asynchronous Presets	1	2	No
Output Enables	1	at least 2	No
Array Inputs	?	22	Yes
Pins (MACH2XX only)	N/A	N/A	N/A
Macrocells (MACH2XX only)	N/A	N/A	N/A

Note:

If the fitting process cannot place all 21 array inputs into this block, they may be reduced in one of the following ways.

- Moving Q[7] to the decoder block reduces array inputs to this block by two. Since it is the counter MSB, it's not used in any other equations within the block. When it's moved to the decoder block, IO_Q[7] and Q[7] drive the decoder block instead of the counter block.
- "ANDing" preset1 and preset2 in the decoder block reduces array inputs to this block by one. This will cause the counter block to have only 1 preset input instead of 2.

Refer to Figure 21 and section 3.2 as you count the product-term clusters and array inputs in the decoder block.

Product-term clusters in decoder block

8	output equations
1	carry out
1	reset
3	extra for XORXNOR
+ 1	extra for pulse 16
14	

Array inputs in decoder block

8	$Q_{(7...0)}$
2	control
2	reset1, reset2
+ 1	XORXNOR gate splitting
13	

Though 14 of the 16 product-term clusters in this block are used, only 13 of the 22 array inputs are used. Placing this logic should pose no problem.

3.5.2 Calculate Total Utilization

At this point, you can calculate total utilization (as listed in the MACH Fitter report file) for the design. This is not a necessary planning step but is shown for clarification and to provide you with an additional planning tool. Total utilization is the average of the following itemized utilizations.

- Pin utilization: defined as the number of pins used divided by the number available.
- Product-term utilization: defined as the number of allocated product-term clusters divided by the number available.
- Array input utilization: defined as the number of array inputs used divided by the total available.

The following utilizations apply to this counter design.

Pin Utilization	24 used, or 63% of the 38 available
Product-term Utilization	(8 + 14) = 22 PT Clusters or 69% of the 32 available
Array Input Utilization	(21 + 13) = 34 or 77% of the 44 available
Total Utilization	(63% + 69% + 77%) / 3 = 70%

3.6 Determine if Utilization is Too High

70% utilization is within MACH device general recommendations (70% is the recommended maximum). Although this design should fit, it is possible that additional logic won't. Designs with higher utilizations are less likely to accommodate changes, particularly after their pinout has been fixed. If no changes are expected to this design, 70% is an appropriate utilization. If changes are expected, modify the design to lower utilization if possible.

4.0 SUMMARY

Overall utilization is only one measure of the likelihood of achieving a successful fit during implementation. Individual resource utilization within blocks must also be taken into account. Partitioning minimizes the total number of array inputs. However, at 21 array inputs, the counter block's switch-matrix utilization in this design is high even after partitioning. This design meets overall device-utilization guidelines and should fit in a MACH110 device.

Note:

In this brief, a detailed pre-entry analysis of the device resources used in a MACH device design was performed. When estimating whether your own design will fit, you may execute a detailed analysis using the block partitioning steps detailed in this document, or simply estimate the resources used as was done in sections 3.1 and 3.2.

APPENDIX A
.PDS Design File from PALASM 4 Software: BUSCNTR. PDS

```
TITLE           cntr_reg
REVISION       1
PATTERN         cntr_register
AUTHOR          Arthur Khu, Jerry Vea
COMPANY         AMD
DATE            01/07/1991
CHIP cntr_reg MACH110
; This design is a bus-loadable, up/down counter, with outputs generated from
; the decoded count value and control inputs. The following MACH constructs are
; illustrated in the design: grouping, output pairing, gate splitting,
; registered logic, combinatorial logic, xor operator, xnor operator, tristate
; input, reset input, and preset input. Also, PALASAM 4 software-specific string
; statements and vector notation are used.
;
; The counter counts up, down or is loaded based on the value of the mode bits.
; The outputs CNT7, CNT7REG, PULSE16, DIV16, and XORXNOR are decoded from the
; count bits Q[7..0]. CNT15UP, CNT15DN, and LD0 are decoded from Q[7..0] and
; mode[1..0]. The count bits are fed back at their node to the switch matrix,
; and also output to pins as IO_Q[7..0].

; This design falls within suggested macrocell, product term and switch matrix
; specifications for successful MACH110 fitting. It has been implemented
; and fitted using PALASM 4 and at least one other 3rd party software tool.
;
; Note: suggested fitting options are: expand small - on, max packing -on,
; and expand all - off.

PIN ? CLK                ; Inputs: Counter clock
PIN ? mode[1..0]         ; Inputs: Count up, count down, load control
PIN ? IO_Q[7..0]         ; Outputs: Count value
PIN ? CARRY0             ; Output: Carry look-ahead
PIN ? CNT7               ; Output: Pulses high on count of 7
PIN ? CNT7REG            ; Output: Set high on count of 7
PIN ? CNT15UP            ; Output: Pulses high when counting up to 15
PIN ? CNT15DN            ; Output: Pulses high when counting down to 15
PIN ? PULSE16            ; Output: Pulses high on certain multiples of 16
PIN ? DIV16              ; Output: Divides clock rate by 16
PIN ? LD0                ; Output: Pulses high on load of 0
PIN ? XORXNOR            ; Output: Uses xor, xnor operators
PIN ? RESET1             ; Input: If both resets are high, resets counter
PIN ? RESET2             ; Input: If both resets are high, resets counter
PIN ? PRESET1            ; Input: If both presets are high, presets counter
PIN ? PRESET2            ; Input: If both presets are high, presets counter
NODE ? Q[7..0] PAIR IO_Q[7..0]  ; Nodes: count value feedback
NODE ? RESET             ; Node: asynchronous reset signal

;***************************************************************************
; Group statements partitioned so design will fit: notice count values in one
; block.
group mach_seg_a IO_Q[7..0]
group mach_seg_b CNT7 CNT7REG CNT15UP CNT15DN LD0 PULSE16 DIV16 XORXNOR
                 RESET

;***************************************************************************
; String statements improve readability of equations
string CNT_UP '(/mode[1] * /mode[0])'
string CNT_DN '(/mode[1] *  mode[0])'
string LOAD   '( mode[1] * /mode[0])'
string Q3_Q0  '(Q[0] * Q[1] * Q[2] * Q[3])'
;***************************************************************************
; Counter equations
```

```
EQUATIONS

Q[ 0].T    := CNT_UP +
              CNT_DN +
              LOAD*(Q[ 0] :+: IO_Q[ 0]);

Q[ 1].T    := CNT_UP* Q[0] +
              CNT_DN*/Q[0] +
              LOAD*(Q[ 1] :+: IO_Q[ 1]);

Q[ 2].T    := CNT_UP* Q[0]* Q[1] +
              CNT_DN*/Q[0]*/Q[1] +
              LOAD*(Q[ 2] :+: IO_Q[ 2]);

Q[ 3].T    := CNT_UP* Q[0]* Q[1]* Q[2] +
              CNT_DN*/Q[0]*/Q[1]*/Q[2] +
              LOAD*(Q[ 3] :+: IO_Q[ 3]);

Q[ 4].T    := CNT_UP* Q[0]* Q[1]* Q[2]* Q[3] +
              CNT_DN*/Q[0]*/Q[1]*/Q[2]*/Q[3] +
              LOAD*(Q[ 4] :+: IO_Q[ 4]);

Q[ 5].T    := CNT_UP* Q[0]* Q[1]* Q[2]* Q[3]* Q[4] +
              CNT_DN*/Q[0]*/Q[1]*/Q[2]*/Q[3]*/Q[4] +
              LOAD*(Q[ 5] :+: IO_Q[ 5]);

Q[ 6].T    := CNT_UP* Q[0]* Q[1]* Q[2]* Q[3]* Q[4]* Q[5] +
              CNT_DN*/Q[0]*/Q[1]*/Q[2]*/Q[3]*/Q[4]*/Q[5] +
              LOAD*(Q[ 6] :+: IO_Q[ 6]);

Q[ 7].T    := CNT_UP* Q[0]* Q[1]* Q[2]* Q[3]* Q[4]* Q[5]* Q[6] +
              CNT_DN*/Q[0]*/Q[1]*/Q[2]*/Q[3]*/Q[4]*/Q[5]*/Q[6] +
              LOAD*(Q[ 7] :+: IO_Q[ 7]);

CARRY0  := CNT_UP*
             /Q[ 0]* Q[ 1]* Q[ 2]* Q[ 3]* Q[ 4]* Q[ 5]* Q[ 6]* Q[ 7] +
              CNT_DN*
              Q[ 0]*/Q[ 1]*/Q[ 2]*/Q[ 3]*/Q[ 4]*/Q[ 5]*/Q[ 6]*/Q[ 7];
;***************************************************************************
; DECODED OUTPUTS
CNT7 =        Q[ 0]* Q[ 1]* Q[ 2]* /Q[ 3]* /Q[ 4]* /Q[ 5]* /Q[ 6]* /Q[ 7];

CNT7REG :=  Q[ 0]* Q[ 1]* Q[ 2]* /Q[ 3]* /Q[ 4]* /Q[ 5]* /Q[ 6]* /Q[ 7];

CNT15UP =   Q[ 0]* Q[ 1]* Q[ 2]* Q[ 3]* /Q[ 4]* /Q[ 5]* /Q[ 6]* /Q[ 7] *
              CNT_UP;

CNT15DN =   Q[ 0]* Q[ 1]* Q[ 2]* Q[ 3]* /Q[ 4]* /Q[ 5]* /Q[ 6]* /Q[ 7] *
              CNT_DN;

PULSE16 =     Q3_Q0 * /Q[ 4]* Q[ 5]* Q[ 6] +
              Q3_Q0 * Q[ 4]* /Q[ 6] +
              Q3_Q0 * /Q[ 5]* /Q[ 6] +
              Q3_Q0 *  /Q[ 7] +
              Q3_Q0 * Q[ 4]* /Q[ 5];

DIV16 =       Q[3];

XORXNOR =         (((Q[0] * Q[ 1] *  Q[ 2] *  Q[ 3] * Q[ 4] *
              Q[ 5]):+: Q[ 6]):*: Q[ 7]);

LD0 =         /Q[ 0]* /Q[ 1]* /Q[ 2]* /Q[ 3]* /Q[ 4]* /Q[ 5]* /Q[ 6]* /Q[ 7] *
              LOAD;

RESET = RESET1 + RESET2;
;***************************************************************************
; Count output assignments
IO_Q[ 0].T := {Q[ 0].T};
IO_Q[ 1].T := {Q[ 1].T};
IO_Q[ 2].T := {Q[ 2].T};
IO_Q[ 3].T := {Q[ 3].T};
IO_Q[ 4].T := {Q[ 4].T};
IO_Q[ 5].T := {Q[ 5].T};
```

```
IO_Q[ 6].T := {Q[ 6].T};

IO_Q[ 7].T := {Q[ 7].T};
;*****************************************************************************
; Reset, preset, and tristate equations

IO_Q[7..0].trst = CNT_UP + CNT_DN;
Q[7..0].RSTF = RESET;
CNT7REG.RSTF = GND;
CARRY0.RSTF  = GND;
Q[7..0].SETF = PRESET1 * PRESET2;
CNT7REG.SETF = GND;
CARRY0.SETF  = GND;
Q[7..0].CLKF = CLK;
CARRY0.CLKF  = CLK;
CNT7REG.CLKF = CLK;
```

APPENDIX B
PALASM 4 MACH Fitter Report
BUSCNTR.RPT

```
PALASM 4.1 MACH FITR - MARKET RELEASE (1-24-91)
 (C) - COPYRIGHT ADVANCED MICRO DEVICES INC., 1990
Reading User Design (TRE File)...
Flags Used:            Unplace=False        Max Packing=True
Flags Used:        Expand Small=True         Expand All=False
Reading Device Database ...
***************************************************
     MACH PLD Fitter - v 1.46         cntr_reg
***************************************************
PAIR Analysis...
Pre-Placement & Equation Usage Checks...

*** Timing Analysis for Signals
 Parameter   Min   Max          Signal List (Those having Max delay.)
      Tpd     1     1           CNT15UP         CNT15DN           LD0
      Tsu     1     2           IO_Q[7]         IO_Q[6]         IO_Q[5]
                                IO_Q[4]         IO_Q[3]         IO_Q[2]
                                IO_Q[1]         IO_Q[0]
      Tco     0     0           IO_Q[7]         IO_Q[6]         IO_Q[5]
                                IO_Q[4]         IO_Q[3]         IO_Q[2]
                                IO_Q[1]         CNT7REG


 Key:
 Tpd - Combinatorial propagation delay, input to output
 Tsu - Combinatorial setup delay before clock
 Tco - Register clock to combinatorial output
 Tcr - Register thru combinatorial logic to setup
 All delay values are expressed in terms of array passes

*** Device Resource Checks
               Available        Used        Remaining
        Clocks:    2              1             1
          Pins:   38             24            14     ->    63%
     I/O Macro:   32             17            15
   Total Macro:   32             19            13
 Product Terms:  128             61            40     ->    68%

MACH-PLD Resource Checks OK!


Partitioning Design into Blocks...

*** Last Equations Placed in Blocks

Weakly -

*** Block Partitioning Results
              Array    Macros     # I/O    Buried   Product    Signal
             Inputs    Remain     Macro    Logic     Terms     Fanout
   Block-> A   21        8          8        0        32         24
   Block-> B   13        5          9        2        56          2

*** Block Signal List
Block-> A          Q[0]         IO_Q[0]            Q[1]          IO_Q[1]
                   Q[2]         IO_Q[2]            Q[3]          IO_Q[3]
                   Q[4]         IO_Q[4]            Q[5]          IO_Q[5]
                   Q[6]         IO_Q[6]            Q[7]          IO_Q[7]
Block-> B        _NODE0          CARRY0           RESET          XORXNOR
                    LD0           DIV16         PULSE16          CNT15DN
                CNT15UP         CNT7REG            CNT7

|> INFORMATION F050 - Device Utilization....... *: 68 %
```

```
Assigning Resources...

*** Macro Block A

   I/O Macros>          IO_Q[1]          IO_Q[2]          IO_Q[3]          IO_Q[4]
      Targets>   0( 2)    6( 8)    9(15)   12(18)
        IO_Q[1] (A  0) -> (A  3) (A  0) (B  0)
        IO_Q[2] (A  6) -> (A  5) (A  6) (B  6)
        IO_Q[3] (A  9) -> (A 10) (A  9) (B  9)
        IO_Q[4] (A 12) -> (A 15) (A 12) (B 12)

 I/O Macros>          IO_Q[5]          IO_Q[6]          IO_Q[7]
      Targets>   1( 3)    7( 9)   13(19)
        IO_Q[5] (A  1) -> (A  2) (A  1) (B  1)
        IO_Q[6] (A  7) -> (A  4) (A  7) (B  7)
        IO_Q[7] (A 13) -> (A 14) (A 13) (B 13)

I/O Macros>          IO_Q[0]
      Targets>   2( 4)   10(16)   14(20)
        IO_Q[0] (A  2) -> (A 18) (A 21) (B  2)

*** Macro Block Inputs

       Inputs>          MODE[0]          MODE[1]          PRESET1          PRESET2
     RESET1
      Targets>   0(10)    1(11)    2(13)    3(32)    4(33)
        MODE[0] (I  0) -> (A 16) (B 16)
        MODE[1] (I  1) -> (A 17) (B 17)
        PRESET1 (I  2) -> (A 19)
        PRESET2 (I  3) -> (A 20)
         RESET1 (I  4) -> (B 21)

*** Macro Block B

   I/O Macros>          PULSE16
      Targets>   0(24)    2(26)    4(28)    6(30)    8(36)   10(38)   12(40)   14(42)

        PULSE16 (B  0)

  I/O Macros>            CNT7              LD0          CNT15DN          XORXNOR
     DIV16          CNT15UP
      Targets>   1(25)    4(28)    6(30)    8(36)   10(38)   12(40)   14(42)
           CNT7 (B  1)              LD0 (B  4)          CNT15DN (B  6)
        XORXNOR (B  8)            DIV16 (B 10)          CNT15UP (B 12)

 Buried Logic>          _NODE0
      Targets>  14(42)
         _NODE0 (B 14) -> (B 14)

  I/O Macros>          CNT7REG          CARRY0
      Targets>   2(26)    5(29)    7(31)    9(37)   11(39)

 CNT7REG (B  2)          CARRY0 (B  5)

 Buried Logic>           RESET
      Targets>   7(31)    9(37)   11(39)

 * Retry Mapping
          RESET (B 11) -> (A 11)

       Inputs>          RESET2
      Targets>   3( 5)    4( 6)    5( 7)    8(14)   10(16)   11(17)   14(20)   15(21)

     * Retry Mapping
     * Retry Mapping
     * Retry Mapping

 RESET2 (A 11) -> (B  8)

*** Signals - Tabular Information
```

Signal	#	P/N #	(Loc)	Type	Logic	# PT	Blocks
CLK	1	35	I 5	clock pin	.		
MODE[1]	2	11	I 1	input	.		AB
MODE[0]	3	10	I 0	input	.		AB
IO_Q[7]	4	19	A 13	i/o pin	t-ff	4	A
IO_Q[6]	5	9	A 7	i/o pin	t-ff	4	A
IO_Q[5]	6	3	A 1	i/o pin	t-ff	4	A
IO_Q[4]	7	18	A 12	i/o pin	t-ff	4	A
IO_Q[3]	8	15	A 9	i/o pin	t-ff	4	A
IO_Q[2]	9	8	A 6	i/o pin	t-ff	4	A
IO_Q[1]	10	2	A 0	i/o pin	t-ff	4	A
IO_Q[0]	11	4	A 2	i/o pin	t-ff	3	A
CARRY0	12	29	B 5	i/o pin	d-ff	2	
CNT7	13	25	B 1	i/o pin	comb	1	
CNT7REG	14	26	B 2	i/o pin	d-ff	1	
CNT15UP	15	40	B 12	i/o pin	comb	1	
CNT15DN	16	30	B 6	i/o pin	comb	1	
PULSE16	17	24	B 0	i/o pin	comb	5	
DIV16	18	38	B 10	i/o pin	comb	1	
LD0	19	28	B 4	i/o pin	comb	1	
XORXNOR	20	36	B 8	i/o pin	comb	3	
RESET1	21	33	I 4	input	.		B
RESET2	22	17	A 11	input	.		B
PRESET1	23	13	I 2	input	.		A
PRESET2	24	32	I 3	input	.		A
Q[7]	25	15	A 13	out pair	t-ff	4	AB
Q[6]	26	9	A 7	out pair	t-ff	4	AB
Q[5]	27	3	A 1	out pair	t-ff	4	AB
Q[4]	28	14	A 12	out pair	t-ff	4	AB
Q[3]	29	11	A 9	out pair	t-ff	4	AB
Q[2]	30	8	A 6	out pair	t-ff	4	AB
Q[1]	31	2	A 0	out pair	t-ff	4	AB
Q[0]	32	4	A 2	out pair	t-ff	3	AB
RESET	33	29	B 11	buried	comb	2	A
_NODE0	34	32	B 14	buried	comb	12	B

```
Key:
P/N # - Pin/Node Number
.?. - Signal Unplaced
(Loc) - Macrocell Location (Block & Cell)
# PT - Number of used product terms in logic
Blocks- Device blocks driven by signal
comb - Combinatorial logic function
d-ff - D-Type Flip-flop
t-ff - T-Type Flip-flop


*** Signals - Equations Where Used

  Signal Source                Fanout List
          CLK
      MODE[1]:        IO_Q[7]         IO_Q[6]         IO_Q[5]         IO_Q[4]
             :        IO_Q[3]         IO_Q[2]         IO_Q[1]         IO_Q[0]
             :         CARRY0         CNT15UP         CNT15DN             LD0
             :           Q[7]            Q[6]            Q[5]            Q[4]
             :           Q[3]            Q[2]            Q[1]            Q[0]
             {AAAA AAAA BBBB AAAA AAAA}
      MODE[0]:        IO_Q[7]         IO_Q[6]         IO_Q[5]         IO_Q[4]
             :        IO_Q[3]         IO_Q[2]         IO_Q[1]         IO_Q[0]
             :         CARRY0         CNT15UP         CNT15DN             LD0
             :           Q[7]            Q[6]            Q[5]            Q[4]
             :           Q[3]            Q[2]            Q[1]            Q[0]
             {AAAA AAAA BBBB AAAA AAAA}

      IO_Q[7]:        IO_Q[7]            Q[7]
             {AA}
      IO_Q[6]:        IO_Q[6]            Q[6]
             {AA}
      IO_Q[5]:        IO_Q[5]            Q[5]
             {AA}
      IO_Q[4]:        IO_Q[4]            Q[4]
             {AA}
      IO_Q[3]:        IO_Q[3]            Q[3]
```

```
         {AA}
IO_Q[2]:        IO_Q[2]         Q[2]
         {AA}
IO_Q[1]:        IO_Q[1]         Q[1]
         {AA}
IO_Q[0]:        IO_Q[0]         Q[0]
         {AA}
 RESET1:         RESET
         {B}
 RESET2:         RESET
         {B}
PRESET1:        IO_Q[7]         IO_Q[6]         IO_Q[5]         IO_Q[4]
       :        IO_Q[3]         IO_Q[2]         IO_Q[1]         IO_Q[0]
       :           Q[7]            Q[6]            Q[5]            Q[4]
       :           Q[3]            Q[2]            Q[1]            Q[0]
         {AAAA AAAA AAAA AAAA}
PRESET2:        IO_Q[7]         IO_Q[6]         IO_Q[5]         IO_Q[4]
       :        IO_Q[3]         IO_Q[2]         IO_Q[1]         IO_Q[0]
       :           Q[7]            Q[6]            Q[5]            Q[4]
       :           Q[3]            Q[2]            Q[1]            Q[0]
         {AAAA AAAA AAAA AAAA}
   Q[7]:        IO_Q[7]          CARRY0            CNT7         CNT7REG
       :        CNT15UP         CNT15DN         PULSE16             LD0
       :        XORXNOR            Q[7]          _NODE0
         {ABBB BBBB BAB}
   Q[6]:        IO_Q[7]         IO_Q[6]          CARRY0            CNT7
       :        CNT7REG         CNT15UP         CNT15DN         PULSE16
       :            LD0         XORXNOR            Q[7]            Q[6]
       :         _NODE0
         {AABB BBBB BBAA B}
   Q[5]:        IO_Q[7]         IO_Q[6]         IO_Q[5]          CARRY0
       :           CNT7         CNT7REG         CNT15UP         CNT15DN
       :        PULSE16             LD0         XORXNOR            Q[7]
       :           Q[6]            Q[5]          _NODE0
         {AAAB BBBB BBBA AAB}
   Q[4]:        IO_Q[7]         IO_Q[6]         IO_Q[5]         IO_Q[4]
       :         CARRY0            CNT7         CNT7REG         CNT15UP
       :        CNT15DN         PULSE16             LD0         XORXNOR
       :           Q[7]            Q[6]            Q[5]            Q[4]
       :         _NODE0
         {AAAA BBBB BBBB AAAA B}
   Q[3]:        IO_Q[7]         IO_Q[6]         IO_Q[5]         IO_Q[4]
       :        IO_Q[3]          CARRY0            CNT7         CNT7REG
       :        CNT15UP         CNT15DN         PULSE16           DIV16
       :            LD0         XORXNOR            Q[7]            Q[6]
       :           Q[5]            Q[4]            Q[3]          _NODE0
         {AAAA ABBB BBBB BBAA AAAB}
   Q[2]:        IO_Q[7]         IO_Q[6]         IO_Q[5]         IO_Q[4]
       :        IO_Q[3]         IO_Q[2]          CARRY0            CNT7
       :        CNT7REG         CNT15UP         CNT15DN         PULSE16
       :            LD0         XORXNOR            Q[7]            Q[6]
       :           Q[5]            Q[4]            Q[3]            Q[2]
       :         _NODE0
         {AAAA AABB BBBB BBAA AAAA B}
   Q[1]:        IO_Q[7]         IO_Q[6]         IO_Q[5]         IO_Q[4]
       :        IO_Q[3]         IO_Q[2]         IO_Q[1]          CARRY0
       :           CNT7         CNT7REG         CNT15UP         CNT15DN
       :        PULSE16             LD0         XORXNOR            Q[7]
       :           Q[6]            Q[5]            Q[4]            Q[3]
       :           Q[2]            Q[1]          _NODE0
         {AAAA AAAB BBBB BBBA AAAA AAB}
   Q[0]:        IO_Q[7]         IO_Q[6]         IO_Q[5]         IO_Q[4]
       :        IO_Q[3]         IO_Q[2]         IO_Q[1]         IO_Q[0]
       :         CARRY0            CNT7         CNT7REG         CNT15UP
       :        CNT15DN         PULSE16             LD0         XORXNOR
       :           Q[7]            Q[6]            Q[5]            Q[4]
       :           Q[3]            Q[2]            Q[1]            Q[0]
       :         _NODE0
         {AAAA AAAA BBBB BBBB AAAA AAAA B}
  RESET:        IO_Q[7]         IO_Q[6]         IO_Q[5]         IO_Q[4]
       :        IO_Q[3]         IO_Q[2]         IO_Q[1]         IO_Q[0]
       :           Q[7]            Q[6]            Q[5]            Q[4]
       :           Q[3]            Q[2]            Q[1]            Q[0]
```

```
              {AAAA AAAA AAAA AAAA}
         _NODE0:          XORXNOR
              {B}

*** Outputs with no feedback

           CARRY0            CNT7          CNT7REG          CNT15UP          CNT15DN
          PULSE16           DIV16              LD0          XORXNOR

*** Feedback Map - cntr_reg
 Gbl Inp .--.       I/O  .--+--A--+--.  I/O             I/O  .--+--B--+--.  I/O
         | 0|      Q[1] : 0|      |21| Q[0]            Q[1] : 0|      |21| RESET1
         | 1|      Q[5] : 1|      |20| PRESET2         Q[5] : 1|      |20|
         | 2|   IO_Q[5] : 2|      |19| PRESET1         Q[0] : 2|      |19|
         | 3|   IO_Q[1] : 3|      |18| IO_Q[0]              | 3|      |18|
         | 4|   IO_Q[6] : 4|      |17| MODE[1]              | 4|      |17| MODE[1]
         | 5|   IO_Q[2] : 5|      |16| MODE[0]              | 5|      |16| MODE[0]
         '--'      Q[2] : 6|      |15: IO_Q[4]         Q[2] : 6|      |15|
                   Q[6] : 7|      |14: IO_Q[7]         Q[6] : 7|      |14: _NODE0
                        | 8|      |13: Q[7]          RESET2 : 8|      |13: Q[7]
                   Q[3] : 9|      |12: Q[4]            Q[3] : 9|      |12: Q[4]
                IO_Q[3] :10|      |11: RESET                |10|      |11|
                         '--+-u--u+--'                       '--+-u--u+--'
*** Logic Map - cntr_reg
 Gbl Inp .--.      I/O   .--+--A--+--.  I/O             I/O  .--+--B--+--.  I/O
  MODE[0]| 0|   IO_Q[1] | 0| 4    |21|              PULSE16 | 0| 5    |21|
  MODE[1]| 1|   IO_Q[5] | 1| 4    |20|                 CNT7 | 1| 1    |20|
  PRESET1| 2|   IO_Q[0] | 2| 3    |19|              CNT7REG | 2| 1    |19|
  PRESET2| 3|           | 3| .    |18|                      | 3| *    |18|
   RESET1| 4|           | 4| .    |17|                  LD0 | 4| 1    |17|
      CLK| 5|           | 5| .    |16|               CARRY0 | 5| 2    |16|
         '--'   IO_Q[2] | 6| 4   .|15|              CNT15DN | 6| 1   *|15|
                IO_Q[6] | 7| 4   .|14|                      | 7| .  12|14| _NODE0
                        | 8| .   4|13| Q[7][7]      XORXNOR | 8| 3   *|13|
                IO_Q[3] | 9| 4   4|12| Q[4][4]              | 9| .   1|12| CNT15UP
                        |10| .   .|11|                 DIV16 |10| 1   2|11| RESET
                         '--+-u--u+--'                        '--+-u--u+--'
*** Pin Map - cntr_reg



                              IO_Q[1]
                           IO_Q[5]  |          .
                        IO_Q[0]  |  |          |  .
                              .  |  |  |          |  |  .
                        .  |  |  |  |          |  |  |  CNT15UP
                        |  |  |  |  |          |  |  |  |
                  .-----'--'--'--'--'--o-----'--'--'--'---.
                  |                       4  4  4  4  4     |
                  |     6  5  4  3  2  1  4  3  2  1  0     |
                  | 7                                    39|
          IO_Q[2] | 8                   G  V             38|DIV16
          IO_Q[6] | 9                   n  c             37|
          MODE[0] |10                   d  c             36|XORXNOR
          MODE[1] |11                                    35|CLK
              Gnd |12             MACH-110               34| Gnd
          PRESET1 |13                                    33|RESET1
                  |14             V  G                   32|PRESET2
          IO_Q[3] |15             c  n                   31|
                  |16             c  d                   30|CNT15DN
           RESET2 |17                                    29|CARRY0
                  |   1  1  2  2  2  2  2  2  2  2  2      |
                  |   8  9  0  1  2  3  4  5  6  7  8      |
                  '---.--.--.--.--------.--.--.--.--.-----'
                      |  |  |  |           |  |  |  |  |
                IO_Q[4]  |  |  |           |  |  |  |  LD0
                   IO_Q[7]  |  |           |  |  |  '
                            '  |           |  |  CNT7REG
                               '           |  CNT7
                                        PULSE16
The Design Doc is  stored in ===> Buscntr.Rpt
The Jedec Data is  stored in ===> Buscntr.Jed
```

```
The Placements are stored in ===> Buscntr.Plc

%% FITR %% Error Count: 0, Warning Count: 0
%% FITR %% File Processed Successfully. - File: Buscntr
```

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