CIRRUS LOGIC

# CL-SH360

*Product Bulletin*

## FEATURES

- Fully hardware- and software-compatible with PC XT/AT computers
- Reed-Solomon error correction code (ECC) with automatic, 'on-the-fly' hardware correction
- Low-power or 'sleep' mode
- Proprietary split-data-field support for zoned recording formats
- Multisector data transfer reduces real-time processing demand
- Programmable buffer segments for user-defined caching, read look-ahead, microcode storage, etc.
- Provides direct bus interface logic with on-chip 24-mA drivers
- Contains the logic for daisy chaining two embedded disk controller drives on a PC XT, as well as PC AT
- Support for multiplexed and non-multiplexed address and data bus microcontroller interface
- Provides logic to speed up PC AT command response
- Provides on-chip registers to emulate the IBM® Task File for PC AT, IBM Command Descriptor Block for PC XT
- 100-pin QFP and VQFP packages
- Low-power CMOS technology

**Supports:**

— Host data transfer under DMA or programmed I/O for both PC XT and PC AT modes
— Direct buffer memory addressing up to 64K bytes of static RAM
— 8- and 16-bit data transfer on the host bus
— Any XT/AT interface speed with programmable and auto-inserted wait states

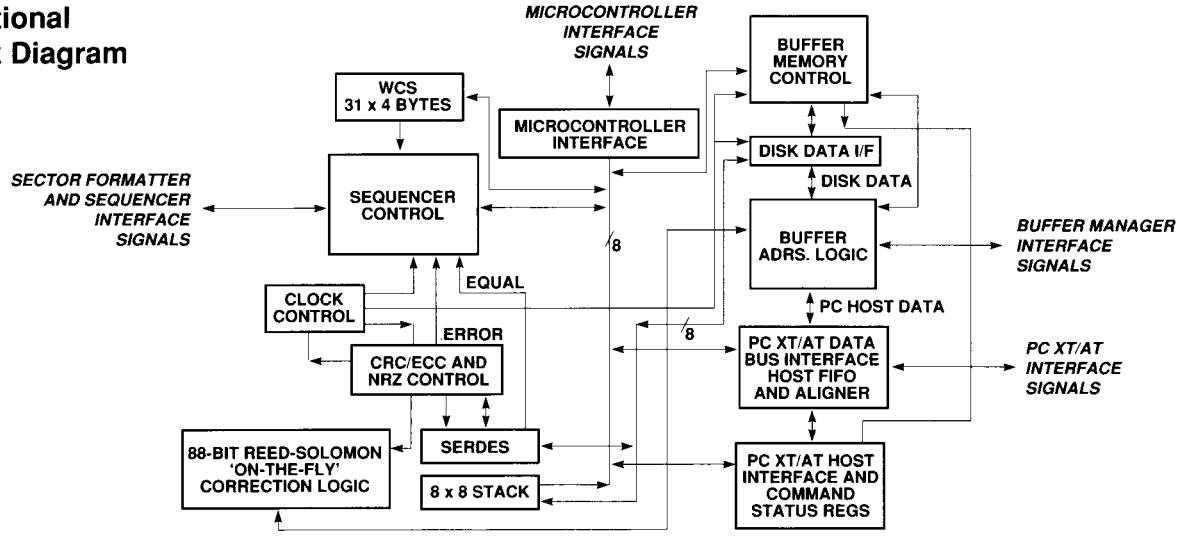
## High-performance PC XT/AT™ Disk Controller

## OVERVIEW

The highly integrated CL-SH360 provides a large portion of the hardware necessary to build a Winchester disk controller for the PC XT/AT or other compatible interface. The CL-SH360 includes an advanced Winchester Disk Formatter, a dual-port Buffer Manager, and a host bus interface. The CL-SH360 provides the enabling feature set and technology for smaller, faster, higher-capacity and lower-cost drives.

To ensure data integrity, the CL-SH360 performs 'on-the-fly' Reed-Solomon error correction, while transferring data at a continuous 32-Mbit/second rate. It automatically performs correction of data errors during disk-read operations (without local microprocessor intervention), making it ideal for high-performance applications. The CL-SH360 is the first intelligent PC AT-compatible disk drive controller to implement this error-tolerance capability. *(cont. next page)*

### Functional Block Diagram



## OVERVIEW (cont.)

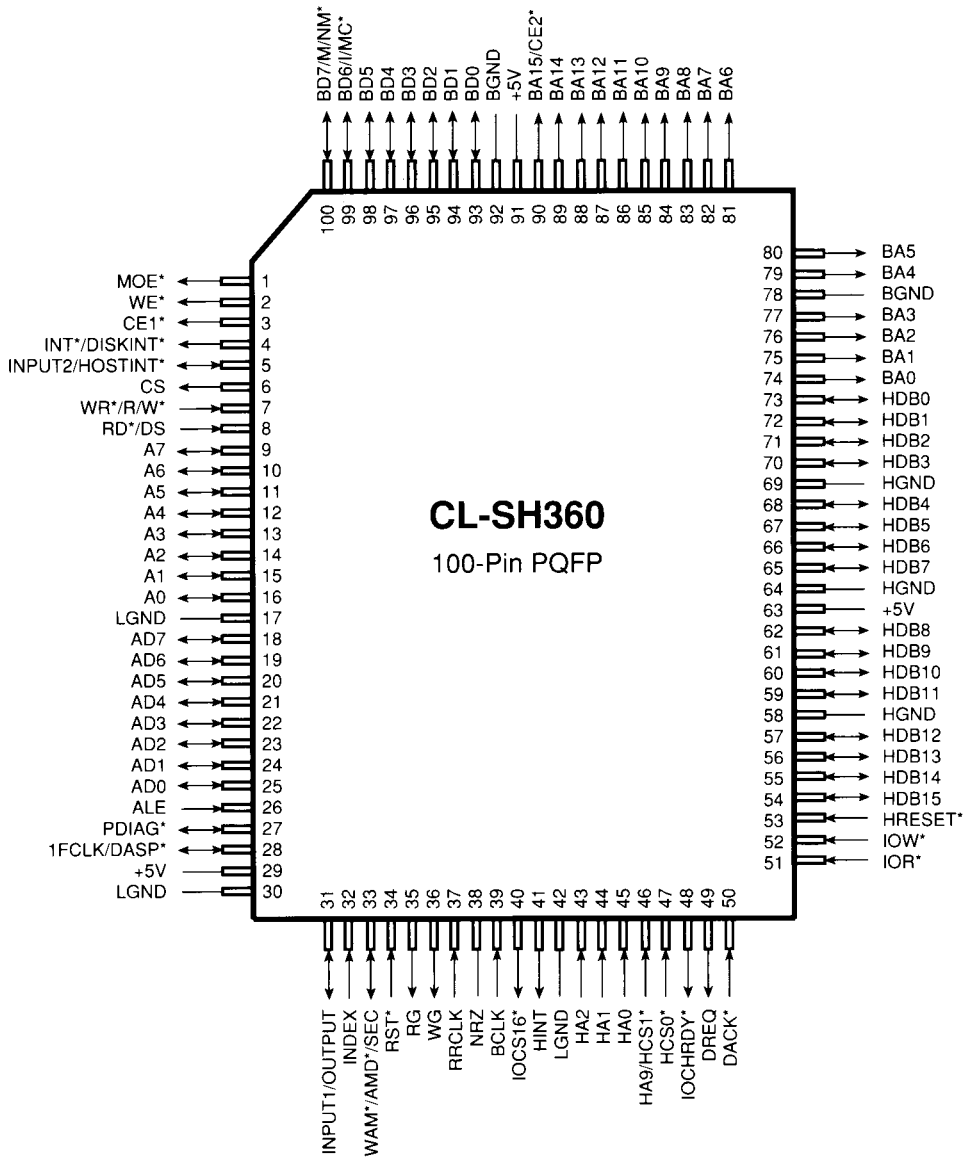
The enhanced CL-SH360 supports disk data rates up to 32 Mbits/second. A proprietary split-data-field technique optimizes disk capacity, enables faster access times, and increases data rates. A power-down mode reduces power consumption by up to 75 percent, making the CL-SH360 ideal for laptop and power-sensitive applications. Because the controller is architecturally compatible, it provides an easy upgrade for both existing designs and higher-performance systems.

The CL-SH360 Disk Formatter consists of a serializer/deserializer, a flexible RAM-based Sequencer, and CRC/ECC generation circuitry. The industry-standard 16-bit CCITT-CRC and proprietary 88-bit Reed-Solomon ECC polynomial are supported in hardware. The CL-SH360 Buffer Manager will control up to 64K bytes of SRAM buffer memory as a dual-port circular buffer. The CL-SH360 supports multisector data transfer, thus reducing real-time processing demand on local microcontrollers, allowing creation of lower-cost, single-processor disk drive designs. It also segments a programmable buffer, for user-defined caching algorithims or protected-memory area in buffer memory.

The CL-SH360 works with a local microcontroller and supports both multiplexed address and data bus architecture, similar to Intel® 8051 family and Motorola® 68HC11 microcontrollers, as well as the newer non-multiplexed bus processor architectures. Also provided is a READY Signal interface for high-speed microcontrollers. It supports both interrupt- and polled-processor interfaces. The maskable interrupts include many disk and host interface events. The CL-SH360 also has hardware to speed microcontroller access of the buffer memory.

## ADVANTAGES

| Unique Features | Benefits |
|---|---|
| • *Reed-Solomon error correction* | Supports true 'on-the-fly' error correction during full-speed data reads. Probability of miscorrection is as low as $10^{-20}$ per bit corrected. |
| • *Multisector data transfer* | Reduces real-time processing demand on the local disk drive microcontroller, allowing creation of lower-cost, single-processor disk drive designs. |
| • *Proprietary split-data-field support* | Optimizes disk capacity, enables faster access times and data rates. |
| • *Low-power or sleep mode* | Reduces power consumption by up to 75 percent. |
| • *Provides automatic wait states or pre-programmed wait states for extended cycle transfers* | Can be compatible with any host CPU speeds. Prevents host overrun or underrun conditions. |
| • *Provides logic for daisy chaining two embedded controller drives on the PC Bus in a Master/Slave Configuration* | Allows the use of two embedded disk controllers in a system. |
| • *Supports 10 Mbytes/second buffer memory throughput* | Compatible with high-performance applications. |
| • *Data rate up to 32 Mbits/second* | Compatible with high-performance applications. |
| • *Maskable microcontroller interrupt capability* | Relieves the microcontroller from polling to perform other tasks. Provides status information to the microprocessor when interrupts are disabled. |

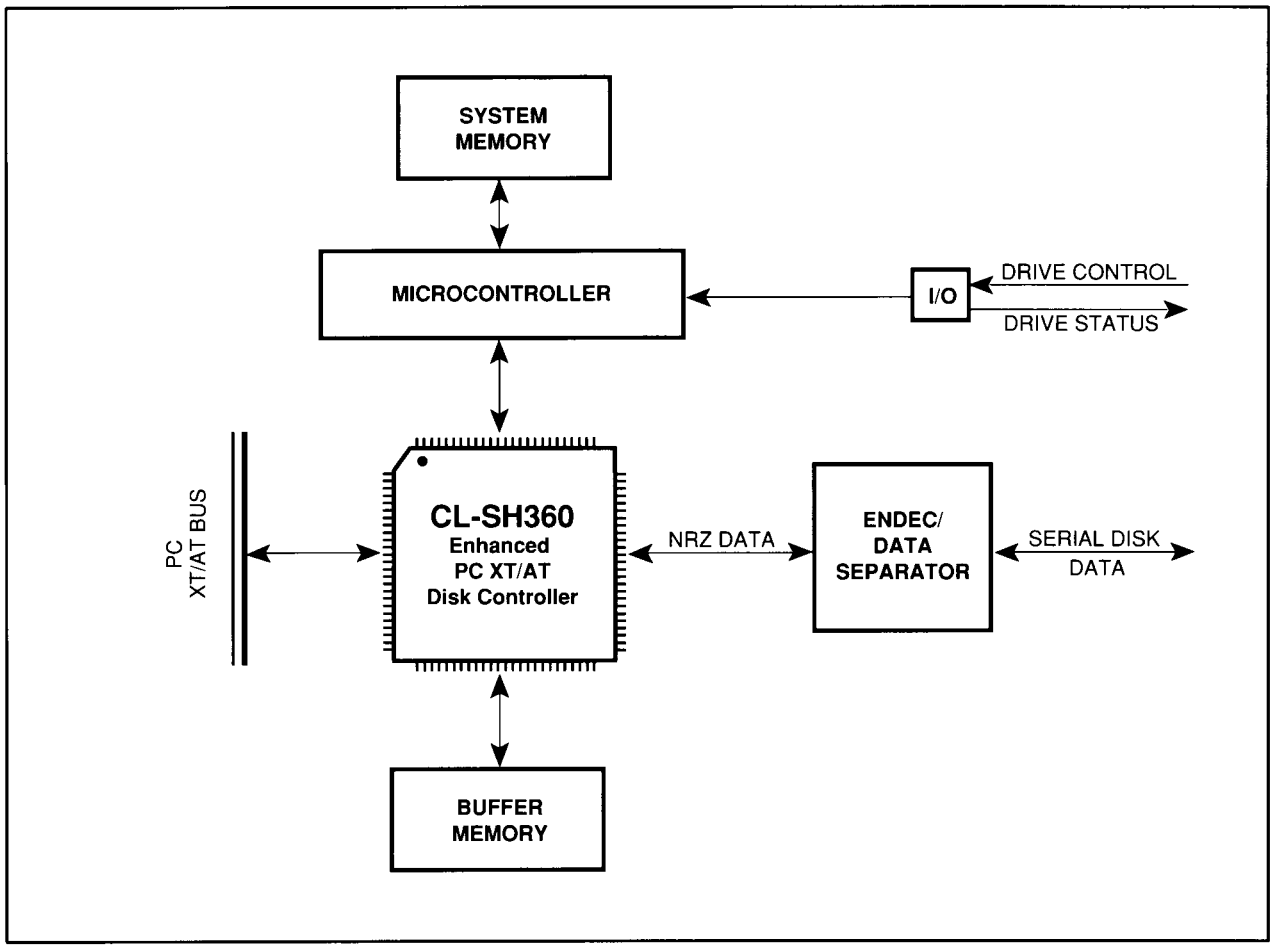



**100-Pin Quad Flat Pack (QFP) Diagram**

## PIN DESCRIPTION

| *Symbol* | *Pin Number (QFP)* | *Type* | *Description* |
|---|---|---|---|
| **Buffer Memory Interface Pins** | | | |
| BA[0:15] | 74-77, 79-90 | O | Buffer Address Lines |
| BD[0:7] | 93-100 | I/O, Z | Buffer Data Bus |
| MOE* | 1 | O | Memory Output Enable |
| WE* | 2 | O | Write Enable |
| CE* | 3 | O | Buffer Chip Enable |
| **Microcontroller Interface Pins** | | | |
| INT* | 4 | O | Interrupt |
| I/MC* | 5 | I | Intel/Motorola |
| CS | 6 | I | Chip Select |
| WR*/R/W* | 7 | I | Write Strobe/Read/Write |
| RD*/DS | 8 | I | Read Strobe/Data Strobe |
| A[7:0] | 9-16 | I/O, Z | Local Microcontroller Address/Data Bus |
| AD[7:0] | 18-25 | I/O, Z | Microcontroller Address/Data |
| ALE/M/NM* | 26 | I | Address Latch Enable/Multiplexed/Non-multiplexed Address Configuration |
| LRDY* | 27 | O | Local Microcontroller Ready |
| 1FCLK | 28 | I | ECC Corrector Circuit Clock |
| **Disk Interface Pins** | | | |
| INPUT/OUTPUT | 31 | I/O, Z | Input/Output |
| INDEX | 32 | I | Index |
| WAM*/AMD*/SECTOR | 33 | I/O, Z | Write Address Mark/Address Mark Detect/Sector |
| RST* | 34 | I | Reset |
| RG | 35 | O | Read Gate |
| WG | 36 | O | Write Gate |
| RRCLK | 37 | I | Read Reference Clock |
| NRZ | 38 | I/O, Z | Non Return to Zero |
| **Host Bus Interface Pins** | | | |
| BCLK | 39 | I | Buffer Clock |
| IOCS16* | 40 | OD | 16-bit Data Transter |
| HINT | 41 | O, Z | Host Interrupt |
| A[2:0] | 43-45 | I | PC Bus Address Lines |
| A9/HCS1* | 46 | I | PC Address Line 9 or Chip Select 1 |
| HCS0* | 47 | I | Chip Select 0 |
| IOCHRDY* | 48 | O, Z | Input/Out Channel Ready |
| DREQ | 49 | O, Z | DMA Request |
| DACK* | 50 | I | DMA Acknowledge |
| IOR* | 51 | I | Input Read Select |
| IOW* | 52 | I | Input Write Select |
| HRESET | 53 | I | Host Reset |
| HDB[15:0] | 54-57, 59-62, 65-68, 70-73 | I/O, Z | Host Data Bus |
| **Power and Ground Pins** | | | |
| HGND | 58, 64, 69 | N/A | Host Ground |
| BGND | 78, 92 | N/A | Buffer Bus Ground |
| LGND | 17, 30, 42 | N/A | Logic Ground |
| +5V | 29, 63, 91 | N/A | Power Supply (+5) |

**NOTE:** (*) denotes negative true signal. I indicates input pin; O indicates output pin; I/O indicates input/output pin; OD indicates open drain output pin; Z indicates tri-state output or input/output pin.




***TYPICAL CL-SH360 APPLICATION***

## Direct Sales Offices

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## The Company

Cirrus Logic, Inc., produces high-integration peripheral controller circuits for mass storage, graphics, and data communications. Our products are used in leading-edge personal computers, engineering workstations, and office automation equipment.

The Cirrus Logic formula combines proprietary S/LA™† IC design automation with system design expertise. The S/LA design system is a proven tool for developing high-performance logic circuits in half the time of most semiconductor companies. The results are better VLSI products, on-time, that help you win in the marketplace.

Cirrus Logic's fabless manufacturing strategy, unique in the semiconductor industry, employs a full manufacturing infrastructure to ensure maximum product quality, availability and value for our customers.

Talk to our systems and applications specialists; see how you can benefit from a new kind of semiconductor company.

† U.S. Patent No. 4,293,783





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