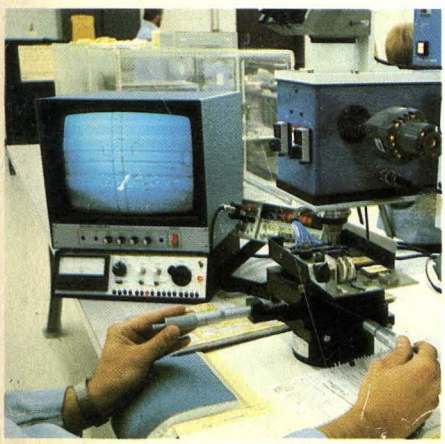
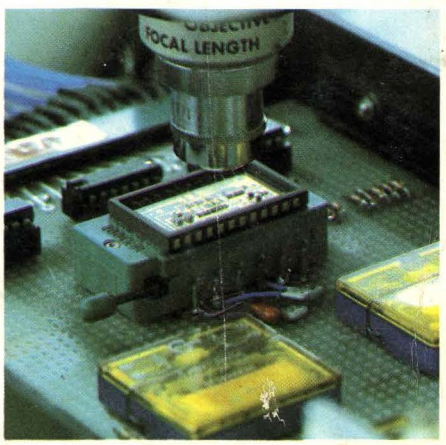
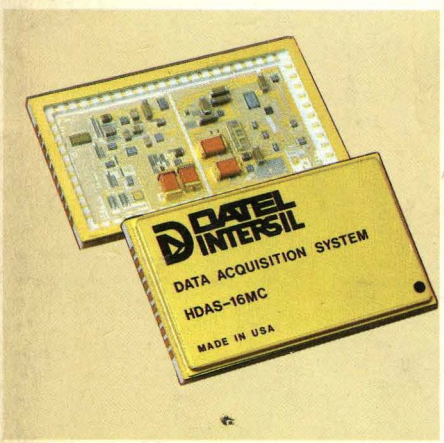
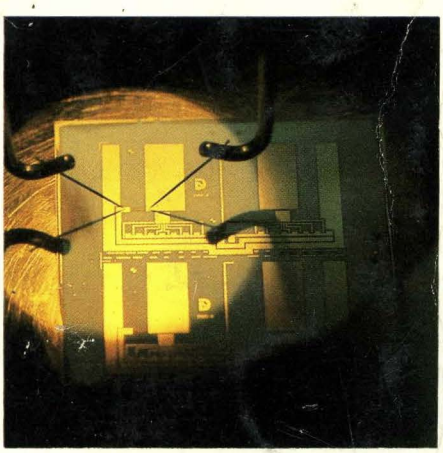
DATEL INTERSIL

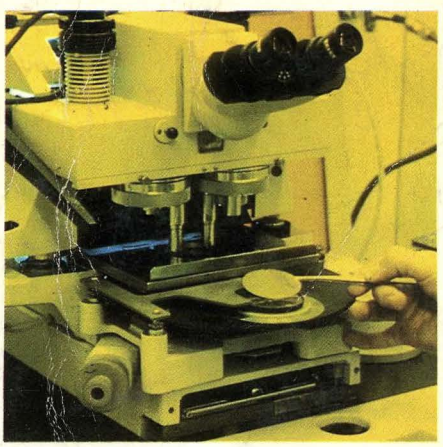
DATA ACQUISITION COMPONENT HANDBOOK

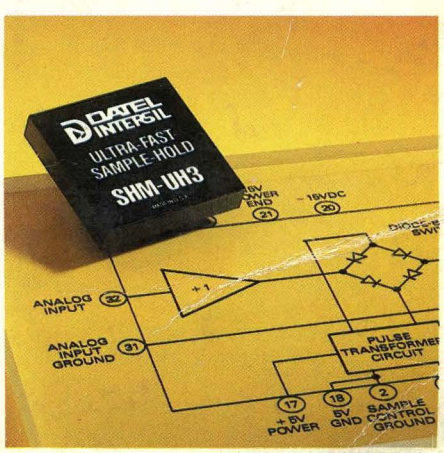












DATA ACQUISITION COMPONENT HANDBOOK

INSTRUMENTS AND SYSTEMS HANDBOOK

ORDERING GUIDE

THIS ORDERING GUIDE IS PRESENTED AS A PROCEDURAL GUIDE. FOR A FORMAL STATEMENT OF POLICIES REFER TO THE TERMS AND CONDITIONS OF SALE FOUND ON THE QUOTATION FORM OR ON THE CUSTOMER ACKNOWLEDGEMENT COPY OF THE SALES ORDER.

PLACING AN ORDER

When ordering a Datel-Intersil product, the complete model number, product description, and option description should be given. Orders may be placed with a Datel-Intersil field sales representative or with the factory by letter, telephone, TWX, or TELEX. **MINIMUM ORDER IS** $50.00, except for cash or C.O.D. orders where minimum is **$30.00.**

OUTSIDE THE U.S.A. AND CANADA: Orders should be placed with a Datel-Intersil Sales Subsidiary (in West Germany, France, the United Kingdom, and Japan) or with a Datel-Intersil overseas sales representative. Orders received directly will be treated the same as if placed through our overseas sales representative. In countries without a Datel-Intersil representative, orders should be placed by TELEX and confirmed by air mail.

FIELD SALES REPRESENTATIVES

Datel-Intersil employs field sales representatives throughout the United States, Canada, Europe, and the Far East. In addition, it has direct Sales Offices in Santa Ana, California; Sunnyvale, California; Gaithersburg, Maryland; and Dallas and Houston, Texas. Datel-Intersil also has Sales Subsidiaries in Munich, West Germany; Paris, France; London, England; and Tokyo and Osaka, Japan. These sales representatives are the only ones authorized by Datel-Intersil to solicit sales, and any information or data received by sources other than these authorized representatives or the Datel-Intersil factory cannot be considered binding.

PRICES

All prices are F.O.B., Mansfield, Massachusetts, U.S.A. in U.S. dollars. Applicable federal, state, and local taxes are extra and paid by buyer. Prices are subject to change without notice.

TERMS: Net 30 Days.

DISCOUNTS

Quantity discounts are available when placed in a single order. OEM discounts are available on an order or contract basis; consult the factory for details.

QUOTATIONS

Price and delivery quotations made by Datel-Intersil or its authorized field sales representatives are valid for 30 days unless otherwise stated.

DELIVERY

Datel-Intersil uses an IBM System 3, Model 12, for efficient processing of orders. All orders placed with Datel-Intersil are acknowledged within a few days by an acknowledgement copy of our sales order form. This copy will indicate pertinent information including a formal statement of terms and conditions of sale and estimated delivery date. This date has preference over all other agreed upon dates unless otherwise specified.

All products are shipped in rugged commercial containers suitable for insuring safe delivery under normal shipping conditions. Unless shipping method is specified, the best available method will be used. UPS, UPS Blue Label, Parcel Post, and Air Parcel Post are among the methods normally used. Datel-Intersil recommends insurance on Parcel Post and Air Parcel Post shipments for tracing purposes. Shipping charges are normally prepaid and billed to the customer except for Air Freight charges which are sent collect. The appropriate data sheet and/or instruction is packed with each product shipped.

ORDER CANCELLATION

All orders entered with Datel-Intersil are binding and are subject to a cancellation charge if cancelled before or after the scheduled shipping date on the acknowledgement copy of the sales order form. The normal cancellation charge is 20% but may be higher depending on expenses already incurred and commitments made by Datel-Intersil.

WARRANTY

Datel-Intersil warrants that its products are free from defects in material and workmanship under normal use and service for a period of one year from the date of shipment for monolithic products. Datel-Intersil's obligations under this warranty are limited to replacement only. In no case shall Datel-Intersil's liability exceed the original purchase price.

RETURNS

When returning products for any reason, contact the factory first for **return authorization number** and shipping instructions. Items should not be returned air freight collect as they cannot be accepted. It is absolutely necessary to return products in the manner stated here otherwise considerable delay will result in processing the return.

RETURNS OUTSIDE THE U.S.A. AND CANADA: Contact the local sales representative or factory for authorization and shipping instructions first.

CERTIFICATE OF COMPLIANCE

Datel-Intersil will provide a standard Certificate of Compliance with all shipments when requested by the customer. This request must be specified on the purchase order.

ABOUT DATEL-INTERSIL

Datel-Intersil is an established international leader in all phases of data conversion technology. In order to meet the rapidly growing need for data acquisition components and systems to interface with computers in industrial, commercial, scientific and military applications, Datel-Intersil offers one of the broadest lines of products in the industry. This product line includes A/D and D/A converters, sample-holds, analog multiplexers, operational and instrumentation amplifiers, V/F and F/V converters, voltage references, temperature sensors, active filters, data-loggers and readers, data acquisition systems, computer analog I/O boards, digital panel meters, digital panel printers, digital voltage calibrators, linear and switching power supplies, and DC-DC converters.

Datel-Intersil's modern 120,000 square foot manufacturing facility in Mansfield, Massachusetts, just 40 minutes from Boston's Logan Airport, houses all Datel-Intersil operations. This new headquarters is dedicated to continuing our leadership position by supplying a steady stream of significant new products to meet the demand for high performance data acquisition devices in the 1980's.

ABOUT THIS PRODUCT HANDBOOK

You are holding two Datel-Intersil catalogs. This section is the Data Acquisition Components Handbook; simply turn this whole volume over to the opposite cover for access to the Instruments and Systems Handbook. This dual catalog reflects Datel-Intersil's dual expertise: leadership in data conversion components technology and leadership in data conversion systems and instrumentation technology.

DATA ACQUISITION COMPONENTS HANDBOOK

This handbook is written for the design engineer who requires detailed technical information about products in order to select and apply a product appropriate to a particular application.

In this handbook, comprised of pages 1C through 566C, products are categorized by function. Products in each category are organized into quick selection tables followed by detailed data sheets for our most popular products. Data Sheets not included in this catalog may be obtained by contacting Datel-Intersil's nearest sales office.

Datel-Intersil also maintains an Application Engineering Department to answer any additional questions that may arise concerning the application of our products.

Our highly qualified team of Field Sales Engineers is available to service your needs throughout the United States, Canada, Western Europe, the Mid East, and Far East.

DATA ACQUISITION COMPONENTS TABLE OF CONTENTS

INSTRUMENTS AND SYSTEMS

Product Index

DC-DC CONVERTER MODULES

INSTRUMENTS AND SYSTEMS SECTION

Digital Panel Meters

Digital Voltage Calibrator

SineTrac A/D-D/A Computer Analog Boards

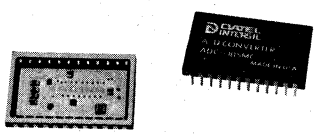
Panel-Mount Thermal Printers

A/D-D/A Computer Data Systems

Low-Power Digital Cassette Data Loggers

New Data Acquisition Components From Datel-Intersil

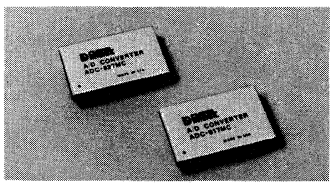
Ultra-fast 8 bit A/D converters Models ADC-815 and ADC-825



- 8 bits resolution
- 600 nsec or 1 μsec conversion times
- 6 analog input ranges
- Parallel or serial outputs
- Logic-controlled bipolar offset
- No calibration required

For full information see page 78C

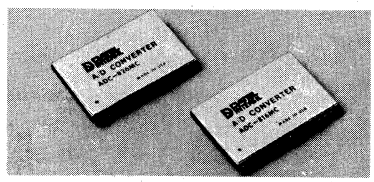
Ultra-fast 12 bit A/D converters Models ADC-817 and ADC-827



- 12 bits resolution
- 2 μsec or 3 μsec conversion times
- 5 programmable analog input ranges
- Parallel or serial data output
- Short cycle capability
- Output coding selection

For full information see page 86C

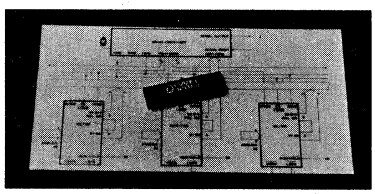
Ultra-fast 10 bit A/D converters Models ADC-816 and ADC-826



- 10 bits resolution
- 800 nsec or 1.4 μsec conversion time
- 6 analog input ranges
- Parallel or serial output
- Selectable output coding
- Fastest 10 bit A/D currently available

For full information see page 82C

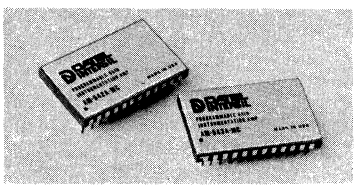
Microprocessor compatible 12 bit integrating A/D converter—Model ADC-7109



- 12 bit resolution
- Polarity and overrange outputs
- Byte-organized three-state TTL outputs
- Uart handshake mode for microprocessor interfacing
- 30 conversions per second
- Fully protected CMOS

For full information see page 46C

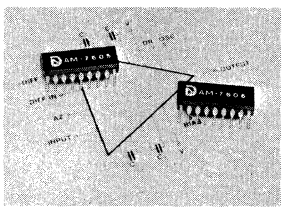
Digitally programmable gain instrumentation amplifiers Models AM-542 and AM-543



- 11 binary weighted gains from 1 to 1024
- 4 bit gain code
- 10^{12} Ω input impedance
- 0.01% nonlinearity
- Gain tempcos to 10 ppm/°C
- Settling times to 10 μsec

For full information see page 378C

CAZ instrumentation amplifiers Models AM-7605 and AM-7606



- 0.05 μV/°C input offset drift
- 2 μV input offset voltage
- 1 to 1000 gain range
- 0.5 μV/year long term drift
- 1.5 nA input bias current
- 100 dB common mode rejection

For full information see page 368C

Ultra-fast 16 bit A/D converter
Model ADC-876

- 16 bit resolution
- 2 μsec conversion time
- ±½ LSB linearity
- ±5V analog input range
- True 500 KHz throughput rate
- Compact 5" x 3" x 0.375" module

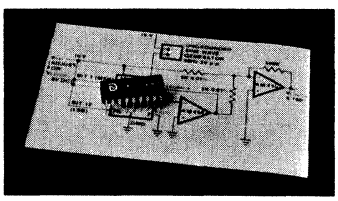
For full information see page 112C

Ultra-linear 8 bit A/D converter
Model ADC-881

- 8 bit resolution
- Statistically linearized conversion
- ±0.0087% nonlinearity
- ±5V analog input range
- 1.5 μsec conversion time
- Out of range indicator

For full information see page 116C

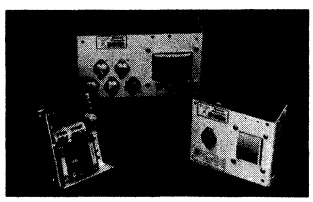
CMOS 12 bit multiplying D/A converter
Model DAC-7541



- 12 bit resolution
- 4 quadrant multiplying
- 0.01% linearity error
- 1 μsec current settling time
- +5V to +15V power supply range
- DTL/TTL/CMOS compatible

For full information see page 168C

Low cost open-frame power supplies
Power chassis series



- Open frame construction
- 4 single output models
- 6 dual output models
- 6 triple output models
- 115 VAC or 230 VAC operated
- 0.05% line regulation

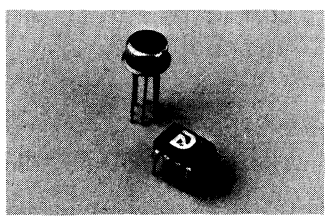
For full information see page 546C

High efficiency 25 watt switching power supplies
Model USM-5/5

- 5VDC ± 1% at 5 AMPS
- 80% efficiency, minimum
- No overshoot on turn-on or turn-off
- Short circuit and overvoltage protection
- Compact 3.5" x 2.5" x 1.25"

For full information see page 543C

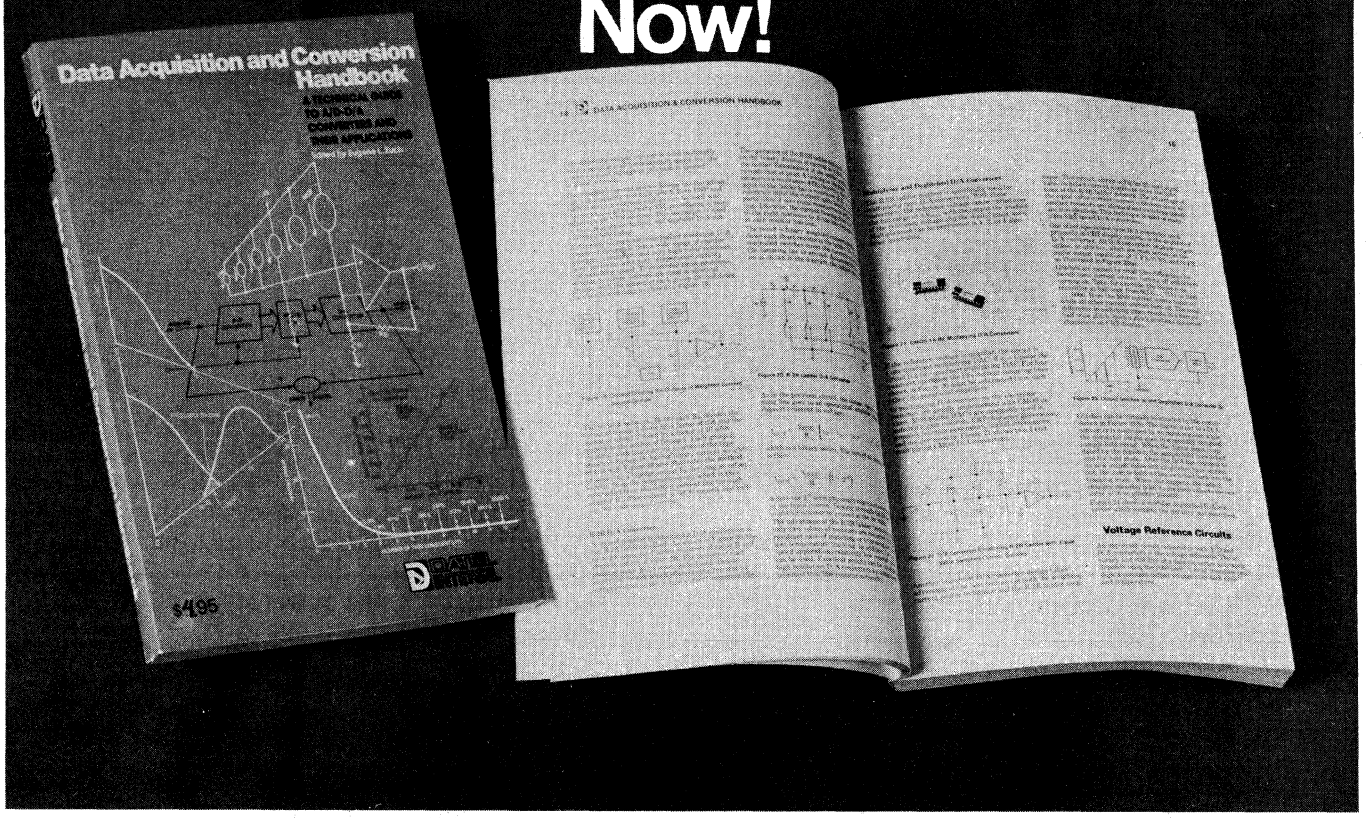
Monolithic CMOS voltage inverter
Model VI-7660



- Converts +5V logic supply to ±5VDC supplies
- Simple voltage multiplication
- 99.9% voltage conversion efficiency
- 98% power efficiency
- Operates from 1.5V to 10.0V supplies
- Two package configurations

For full information see page 422C

Be an Expert on Data Acquisition and Conversion Now!



Datel-Intersil's new 242 page Data Acquisition and Conversion Handbook

This handbook contains a wealth of useful information on the theory and application of data conversion circuits and systems. Written in clear concise language, this book contains 35 technical articles with 312 illustrations and 40 tables. It concludes with a handy glossary of the 200 most commonly used data acquisition terms.

Major topics covered:

- Principles of Data Acquisition and Conversion
- A/D and D/A Converters
- Data Conversion Systems
- Sample-Holds
- High Speed Op Amps
- V/F Converters

You will want to add this useful reference work to your engineering library. Just mail the coupon with your payment. Please, No Purchase Orders.

PRICE: U.S. & Canada $4.95
Elsewhere add $2.75 for air shipment and handling.

Massachusetts Residents add 5% Sales Tax.

TO: Datel-Intersil, Inc.
Attn: Marketing Department
11 Cabot Boulevard, Mansfield, MA 02048

Please send _____ copies of "Data Acquisition and Conversion Handbook." $_____ enclosed.

NAME _____

COMPANY _____

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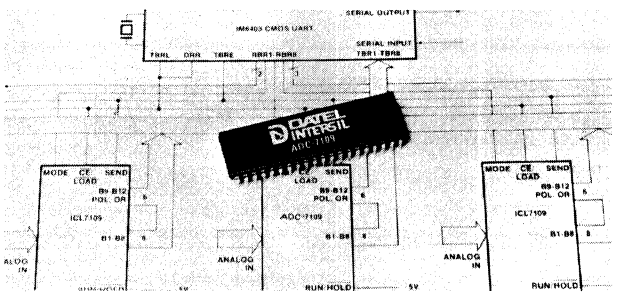
STREET _____

CITY _____ STATE _____ ZIP _____

COUNTRY _____

Analog-To-Digital Converters



Quick Selection: General Purpose A/D Converters

	MODEL	DESCRIPTION	RESOLUTION	CONVERSION TIME, MAX.	LINEARITY ERROR, MAX.	ANALOG INPUT RANGE
MONOLITHIC	**ADC-EK8B**	Low Cost Integrating A/D	8 Bits	1.8 msec	±½ LSB	0 to +10V, ±5V
	ADC-EK10B		10 Bits	6 msec		
	ADC-EK12B		12 Bits	24 msec		
	ADC-EK12DC		3½ Digits	12 msec		0 to +10V
	ADC-EK12DR					
	ADC-EK12DM					
	ADC-ET8BC	Low Cost Integrating A/D with Three-State Outputs	8 Bits	1.8 msec	±½ LSB	0 to +10V, ±5V
	ADC-ET8BM					
	ADC-ET10BC		10 Bits	6 msec		
	ADC-ET10BM					
	ADC-ET12BC		12 Bits	24 msec	±1½ LSB	
	ADC-ET12BR				±½ LSB	
	ADC-ET12BM					
	ADC-MC8BC	Multifunction A/D-D/A	8 Bits	500 μsec	±½ LSB	0 to +2.5V, 0 to +5V 0 to +10V
	ADC-MC8BM					
	ADC-856C	Tracking A/D Latched Outputs	10 Bits	1 μsec/LSB[1]	±½ LSB	0 to +5V, 0 to +10V ±2.5V, ±5V, ±10V
	ADC-856M					
	ADC-7109C	Integrating A/D Byte-Organized Three State Outputs	13 Bits	33.3 msec	±1 LSB	±4V
	ADC-7109R					
	ADC-7109M					
HYBRID	**ADC-HX12BGC**	Successive Approximation A/D with Input Buffer Amp	12 bits	20 μsec	±½ LSB	0 to +5V, 0 to +10V ±2.5V, ±5V, ±10V
	ADC-HX12BMC					
	ADC-HX12BMR					
	ADC-HX12BMM					

NOTES: 1. For tracking operation only, non-tracking Full Scale conversion time is 1.024 msec. max.

2. Coding: Bin = Straight Binary or Offset Binary
   BCD = Binary Coded Decimal
   C Bin = Complementary Binary
   C2C = Complementary Two's Complement
   Sign Mag Bin = Sign Magnitude Binary

OUTPUT CODING[2]	GAIN TEMPCO	POWER REQUIREMENT	PACKAGE	PACKAGE MATERIAL	OPER. TEMP. RANGE (°C)	PRICE (1-24)	SEE PAGE
Bin	25 ppm/°C	±5VDC	24 pin DIP	Plastic	0 to +70	**$ 11.50**	16C
				Ceramic	0 to +70	**$ 29.00**	
					0 to +70	**$ 38.00**	
BCD				Plastic	0 to +70	**$ 13.95**	
				Ceramic	−25 to +85	**$ 23.00**	
					−55 to +125	**$ 43.00**	
Bin	25 ppm/°C	±5VDC	24 pin DIP	Plastic	0 to +70	**$ 14.00**	20C
				Ceramic	−55 to +125	**$ 42.00**	
				Plastic	0 to +70	**$ 18.50**	
				Ceramic	−55 to +125	**$ 52.50**	
				Plastic	0 to +70	**$ 19.50**	
				Ceramic	−25 to +85	**$ 41.50**	
					−55 to +125	**$ 71.50**	
Bin	10 ppm/°C	+5V	16 pin DIP	Plastic	0 to +70	**$ 9.95**	26C
				Ceramic	−55 to +125	**$ 22.00**	
Bin	40 ppm/°C	±5VDC	28 pin DIP	Ceramic	0 to +70	**$ 52.00**	62C
					−55 to +125	**$ 83.00**	
Sign Mag. Bin. with Overrange	5 ppm/°C	±5VDC	40 pin DIP	Plastic	0 to +70	**$ 18.22**	46C
				Cerdip	−25 to +85	**$ 29.83**	
				Ceramic	−55 to +125	**$ 61.76**	
CBin C2C	20 ppm/°C	±15VDC, +5V	32 pin Ceramic DIP	Epoxy Seal	0 to 70	**$ 87.00**	74C
				Hermetic Seal	0 to 70	**$110.00**	
					−25 to +85	**$125.00**	
					−55 to +125	***$165.00**	

*Available with MIL-STD-883 class B screening.

THESE PRODUCTS ARE COVERED BY GSA CONTRACT

Quick Selection: General Purpose A/D Converters

	MODEL	DESCRIPTION	RESOLUTION	CONVERSION TIME, MAX.	LINEARITY ERROR, MAX.	ANALOG INPUT RANGE
MODULES	**ADC-Econoverter**	Counter Type	6 Bits	50 μsec	±½ LSB	0 to +5, 0 to +10, ±2.5V, ±5V
	ADC-89A8B	Counter Type	8 Bits	200 μsec	±½ LSB	0 to +10V, ±5V
	ADC-89A8D		2 Digits	100 μsec		0 to +10V
	ADC-E8B	Fast Dual Slope	8 Bits	312 μsec	±½ LSB	±1V, ±5V, ±10V
	ADC-E10B		10 Bits	1.25 msec		
	ADC-E12B		12 Bits	5.0 msec		
	ADC-E8D		2½ Digits	500 μsec		±2V, ±5V, ±10V
	ADC-E12D		3½ Digits	5.0 msec		
	ADC-L8B2	Successive Approximation Type	8 Bits	12 μsec	±½ LSB	0 to +5V, 0 to +10V, ±5V, ±10V
	ADC-L10B2		10 Bits	16 μsec		
	ADC-L12B2		12 Bits	20 μsec		
	ADC-L8D2		2 Digits	12 μsec		0 to +5V, 0 to +10V
	ADC-L12D2		3 Digits	20 μsec		
	ADC-MA10B2A	Successive Approximation Parallel or Serial Output	10 Bits	40 μsec	±½ LSB	0 to +5V, 0 to +10V ±2.5V, ±5V, ±10V
	ADC-MA10B2B			20 μsec		
	ADC-MA12B2A		12 Bits	40 μsec		
	ADC-MA12B2B			20 μsec		
	ADC-M8B2	Fast Successive Approximation Type	8 Bits	4.0 μsec	±½ LSB	0 to +5V, 0 to +10V ±5V, ±10V
	ADC-M10B2		10 Bits	11.5 μsec		
	ADC-M12B2		12 Bits	13.0 μsec		
	ADC-M8D2		2 Digits	4.0 μsec		0 to +5V, 0 to +10V
	ADC-M12D2		3 Digits	13.0 μsec		

OUTPUT CODING	GAIN TEMPCO	POWER REQUIREMENT	PACKAGE SIZE INCHES (MM)	OPER. TEMP. RANGE (°C)	PRICE (1-9)	SEE PAGE
Bin	100ppm/° C	±15V, +5V	2x2x0.375 (51x51x10)	0 to +70	**$ 46.00**	*
Bin	50ppm/° C	±15VDC, +5V	3x2x0.375 (76x51x10)	0 to +70	**$ 84.00**	*
BCD					**$ 84.00**	
Sign Mag. Bin	50ppm/° C	±15VDC, +5V	4x2x0.4 (102×51×10)	0 to +70	**$ 94.50**	90C
					$105.00	
					$121.00	
Sign Mag. BCD					**$ 94.50**	
					$121.00	
Bin, 2C	10ppm/° C	±15VDC +5V	3x2x0.375 (76x51x10)	0 to +70	**$157.50**	*
					$180.50	
			4x2x0.4 (102x51x10)		**$203.50**	
BCD					**$157.50**	
					$203.50	
Bin, 2C	30ppm/° C	±15VDC, +5V	4x2x0.4 (102x51x10)	0 to +70	**$132.00**	*
					$146.00	
					$140.50	
					$194.00	
Bin, 2C	10ppm/° C	±15VDC +5V	4x2x0.4 (102x51x10)	0 to +70	**$266.50**	*
					$343.50	
					$405.00	
BCD					**$266.50**	
					$405.00	

*For Data Sheet Contact Nearest Datel Sales Office

Datel offers modular products in operating temperature ranges of −25 to +85°C (suffix-EX) and −55 to +85°C (suffix-EXX-HS). For information on these high reliability modules contact nearest Datel sales office.

THESE PRODUCTS ARE COVERED BY GSA CONTRACT

Quick Selection: High Performance A/D Converters

	MODEL	DESCRIPTION	RESOLUTION	CONVERSION TIME, MAX.	LINEARITY ERROR, MAX.	ANALOG INPUT RANGE
MON.	**ADC-7104-14C**	Integrating A/D;	15 Bits	81 msec	±1 LSB	±150mV to ±10V
	ADC-8068AC	Byte Organized	Analog Sec. for Two Chip A/D			
	ADC-7104-16C	Three State Outputs	17 Bits	328 msec		
HYBRID	**ADC-HC12BMC** **ADC-HC12BMR** **ADC-HC12BMM**	Low Power CMOS A/D	12 Bits	300 μsec	±½ LSB	0 to +5V, 0 to +10V ±2.5V, ±5V, ±10V
	ADC-HS12BMC **ADC-HS12BMR** **ADC-HS12BMM**	Fast A/D with Sample-Hold	12 Bits	9 μsec	±½ LSB	0 to +5V, 0 to +10V ±2.5V, ±5V, ±10V
	ADC-HZ12BGC **ADC-HZ12BMC** **ADC-HZ12BMR** **ADC-HZ12BMM**	Fast A/D with Input Buffer Amplifier	12 Bits	8 μsec	±½ LSB	0 to +5V, 0 to +10V ±2.5V, ±5V, ±10V
	ADC-825MC **ADC-825MR** **ADC-825MM**	Very Fast A/D Logic Controlled Bipolar Offset	8 Bits	1 μsec	±½ LSB	0 to +5V, 0 to +10V 0 to +20V, ±2.5V, ±5V, ±10V
	ADC-826MC **ADC-826MR** **ADC-826MM**	Very Fast Successive Approximation A/D	10 Bits	1.4 μsec	±½ LSB	0 to -5V, 0 to -10V, 0 to -20V, ±2.5V, ±5V, ±10V
	ADC-827MC **ADC-827MR** **ADC-827MM**	Very Fast A/D with Internal Buffer	12 Bits	3 μsec	±½ LSB	0 to -5V, 0 to -10V ±2.5V, ±5V, ±10V
MOD	**ADC-881**	Ultra-Linear	8 Bits	1.5 μsec	±0.04 LSB	±5V
	ADC-149-14B	Fast High Res.	14 Bits	50 μsec	±½ LSB	0 to -10, -20, ±5, ±10V

NOTES:
1. Two chip A/D converter, requires ADC-8068AC and either ADC-7104-14C or ADC-7104-16C for complete function.
2. Output Coding: Bin = Straight Binary or Offset Binary
   2C = Two's Complement
   C Bin = Complementary Binary
   C2C = Complementary Two's Complement
   Sign Mag Bin = Sign Magnitude Binary

OUTPUT CODING[2]	GAIN TEMPCO	POWER REQUIREMENT	PACKAGE	PACKAGE TYPE	OPER. TEMP. RANGE (°C)	PRICE (1-24)	SEE PAGE
Sign Mag Bin. with Over Range	5ppm/°C	±15VDC, +5V	40 pin DIP	Plastic	0 to +70	$ 34.12	30C
			14 pin DIP	Cerdip		$ 12.10	
			40 pin DIP	Plastic		$ 38.32	
Bin, 2C	30ppm/°C	+9 to +15V, ±9 to ±15V	32 pin Ceramic DIP	Hermetic Seal	0 to +70	$129.00	66C
					-25 to +85	$169.00	
					-55 to +125	*$209.00	
C Bin C2C	20ppm/°C	±15VDC, +5V	32 pin Ceramic DIP	Hermetic Seal	0 to +70	$139.00	70C
					-25 to +85	$189.00	
					-55 to +100	*$239.00	
C Bin, C2C	20ppm/°C	±15VDC, +5V	32 pin Ceramic DIP	Epoxy Seal	0 to +70	$119.00	74C
				Hermetic Seal		$130.00	
					-25 to +85	$165.00	
					-55 to +125	*$205.00	
Bin 2C	20ppm/°C	±15VDC, +5V	24 pin Ceramic DIP	Hermetic Seal	0 to +70	$165.00	78C
					-25 to +85	$195.00	
					-55 to +125	*$235.00	
Bin 2C	37ppm/°C	±15VDC, +5V	32 pin Ceramic DIP	Hermetic Seal	0 to +70	$180.00	82C
					-25 to +85	$210.00	
					-55 to +125	*$255.00	
Bin, 2C	25ppm/°C	±15VDC, +5V	32 pin Ceramic DIP	Hermetic Seal	0 to +70	$195.00	86C
					-25 to +85	$225.00	
					-55 to +125	*$275.00	
Bin	30ppm/°C	±15V, +5V	5"x3"x.375" (127x76x9,5mm)		0 to +70	Consult Factory	116C
Bin, 2C	15ppm/°C	±15V, +5V	4"x2"x.8" (102x51x20mm)		0 to +70	(1-9) $264.50	110C

*Available with MIL-STD-883 class B screening.

Datel offers modular products in operating temperature ranges of −25 to +85°C (suffix-EX) and −55 to +85°C (suffix-EXX-HS). For information on these high reliability modules contact nearest Datel sales office.

THESE PRODUCTS ARE COVERED BY GSA CONTRACT

Quick Selection: High Speed A/D Converters

	MODEL	DESCRIPTION	RESOLUTION	CONVERSION TIME, MAX.	LINEARITY ERROR, MAX.	ANALOG INPUT RANGE
HYBRIDS	ADC-HU3BMC ADC-HU3BMR ADC-HU3BMM	Ultra-Fast Flash Type	3 Bits	20 nsec	0.1%	± 2.1V
	ADC-815MC ADC-815MR ADC-815MM	Ultra-Fast, No Calibration, Logic Controlled Bip. Offs.	8 Bits	600 nsec	± ½ LSB	0 to + 5v, 0 to + 10V 0 to + 20V, ± 2.5V ± 5V, ± 10V
	ADC-816MC ADC-816MR ADC-816MM	Fastest Hybrid 10 Bit A/D Available	10 Bits	800 nsec	± ½ LSB	0 to − 5V, 0 to − 10V, 0 to − 20V, ± 2.5V, ± 5V, ± 10V
	ADC-817MC ADC-817MR ADC-817MM	Ultra-Fast with Input Buffer Amplifier	12 Bits	2 μsec	± ½ LSB	0 to − 5V, 0 to − 10V ± 2.5V, ± 5V ± 5V
MODULES	ADC-SH4B	Int. Sample-Hold	4 Bits	500 nsec	± ⅓ LSB	0 to + 1V
	ADC-UH4B ADC-UH4B2	Ultra-Fast Flash Type	4 Bits	40 nsec	± ½ LSB	0 to − 2.56V ± 1.28V
	ADC-EH8B1 ADC-EH8B2	Fast with Par. and Ser. Outputs	8 Bits	4 μsec 2 μsec	± ½ LSB	0 to + 10V, ± 5V
	ADC-G8B	Ultra-fast	8 Bits	800 nsec	± ½ LSB	0 to − 5, − 10V, ± 5, ± 10V
	ADC-UH8B ADC-UH8B2	Two-Stage Flash Type	8 Bits	100 nsec	± 1LSB	0 to − 2.56V ± 1.28V
	ADC-TV8B1 ADC-TV8B2	Video Speed, 20 MHz	8 Bits	50 nsec	± ½ LSB	0 to + 1, + 2, + 5V ± 1, ± 2, ± 5V
	ADC-EH10B1 ADC-EH10B2	Serial and Parallel Outputs	10 Bits	4 μsec 2 μsec	± ½ LSB	0 to 10V, ± 5V
	ADC-G10B	Ultra-fast	10 Bits	1 μsec	± ½ LSB	0 to − 5, 10V, ± 5, ± 10V
	ADC-EH12B1 ADC-EH12B2 ADC-EH12B3	Fast Very Fast Ultra-Fast	12 Bits	8 μsec 4 μsec 2 μsec	± ½ LSB	0 to + 10V, ± 5V
	ADC-876	Fastest Available	16 Bits	2 μsec	± ½ LSB	± 5V

NOTES: 1. Coding: Bin = Straight Binary or Offset Binary
2C = Two's Complement

OUTPUT CODING[1]	GAIN TEMPCO	POWER REQUIREMENT	PACKAGE	OPER. TEMP RANGE (°C)	PRICE (SINGLES)	SEE PAGE
Bin	25 ppm/°C	±5VDC	32 Pin Hermetically Sealed Triple Spaced Ceramic DIP	0 to +70	$169.00	**
				−25 to +85	$199.00	
				−55 to +125	$249.00	
Bin, 2C	20 ppm/°C	±15VDC, +5V	24 Pin Hermetically Sealed Triple Spaced Ceramic DIP	0 to +70	$205.00	78C
				−25 to +85	$235.00	
				−55 to +125	*$275.00	
Bin, 2C	38 ppm/°C	±15VDC, +5V	32 Pin Hermetically Sealed Triple Spaced Ceramic DIP	0 to +70	$245.00	82C
				−25 to +85	$275.00	
				−55 to +125	*$315.00	
Bin, 2C	25 ppm/°C	±15VDC, +5V	32 Pin Hermetically Sealed Triple Spaced Ceramic DIP	0 to +70	$295.00	86C
				−25 to +85	$325.00	
				−55 to +125	*$365.00	
Bin.	200 ppm/°C	±15V, +5V	2 × 2 × .375 IN.(51 × 51 × 10mm)	0 to +70	$110.00	**
Bin.	50 ppm/°C	±15VDC, +5V	5 × 3 × 1.15 IN.(127 × 76 × 29mm)	0 to +70	$379.00	102C
					$379.00	
Bin, 2C	50 ppm/°C	±15VDC, +5V	2 × 2 × .375 IN(51 × 51 × 10mm)	0 to +70	$ 99.50	94C
					$151.00	
Bin, 2C	25 ppm/°C	±15V, +5V	4 × 2 × .4 IN(102 × 51 × 10mm)	0 to +70	$264.50	**
Bin.	50 ppm/°C	±15VDC, +5V	5 × 3 × 1.15 IN(127 × 76 × 29mm)	0 to +70	$626.00	102C
					$626.00	
Bin (ECL)	60 ppm/°C	±15VDC, +5V	7.5 × 4.25 × .875 IN (191 × 108 × 22mm)	0 to +70	$941.00	106C
Bin (TTL)					$998.50	
Bin, 2C	30 ppm/°C	±15VDC, +5V	3 × 2 × .375 IN(76 × 51 × 10mm)	0 to +70	$174.00	96C
					$210.00	
Bin, 2C	25 ppm/°C	±15V, +5V	4 × 2 × .8 IN(102 × 51 × 20mm)	0 to +70	$308.50	**
Bin, 2C	30 ppm/°C	±15VDC, +5V	4 × 2 × .375 IN(102 × 51 × 10mm)	0 to +70	$199.50	98C
					$241.50	
					$286.50	100C
Bin, 2C	25 ppm/°C	±15V, +5V	5 × 3 × .375 IN(127 × 76 × 10mm)	0 to +70	Contact Fact.	112C

*Available with MIL-STD-883 class B screening.
**For data sheet contact nearest DATEL-INTERSIL sales office.

Datel offers modular products in operating temperature ranges of −25 to +85°C (suffix-EX) and −55 to +85°C (suffix-EXX-HS). For information on these high reliability modules contact nearest Datel sales office.

THESE PRODUCTS ARE COVERED BY GSA CONTRACT

Monolithic Integrating Analog-to-Digital Converters ADC-EK Series

FEATURES

- **Monolithic CMOS**
- **Binary or BCD Models**
- **20mW Power Consumption**
- **To 12 Bit Accuracy**
- **No Missing Codes**
- **Low Cost**

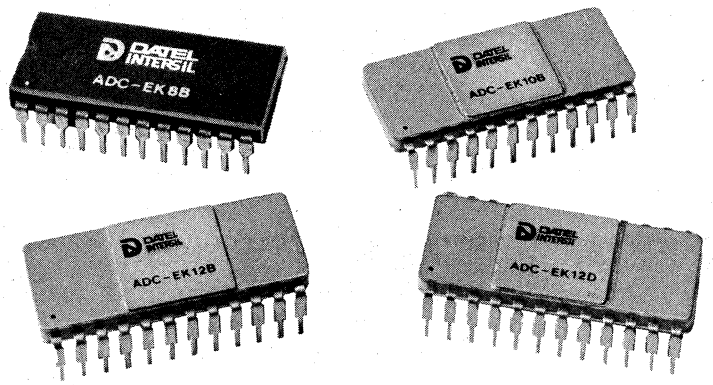
GENERAL DESCRIPTION

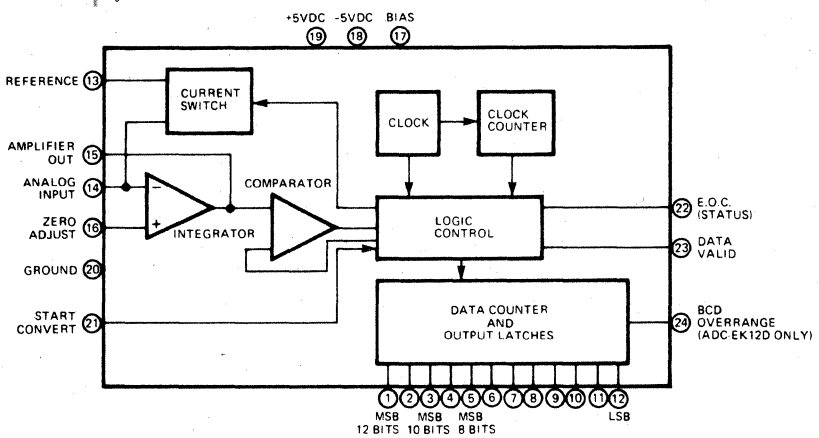
The ADC-EK series are low power, integrating A/D converters fabricated on a single monolithic chip using CMOS technology. The circuit employs a charge balancing integrator, current switch, comparator, clock counter, data counter, and control logic circuitry to implement conversion. The charge balancing integration technique gives high linearity and noise immunity along with inherent monotonicity resulting in no missing codes. Output data appears in parallel form on latched outputs which are CMOS, low power TTL, or low power Schottky TTL compatible. The ADC-EK series consists of 5 different models with 8, 10, and 12 bit binary coding and 3½ digit BCD coding.

Conversion time is 1.8 to 24 milliseconds maximum depending on model. Nonlinearity is ±½ LBS max. while differential nonlinearity is ±¼ LSB typical. Other specifications include gain tempco of ±25ppm/°C typ. and zero drift of ±50μ V/°C max. An external reference, integrating capacitor, and several other components are required for operation. The analog input voltage range is programmable by means of an external resistor which sets the current into the integrator at 10μA full scale. Standard operating mode is unipolar but bipolar operation is accomplished using an external op amp to provide an offset current from the reference.

Power requirement is ±5VDC at 2mA, giving a power consumption of only 20 milliwatts. The units are packaged in 24 pin ceramic or plastic DIP's.

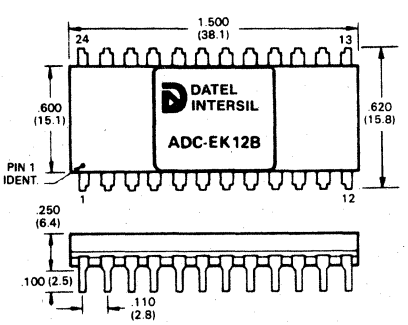
CAUTION: The ADC-EK Series are CMOS devices and should be handled carefully to prevent static charge pick-up which might damage the devices. The devices should be kept in the shipping containers until ready for installation.



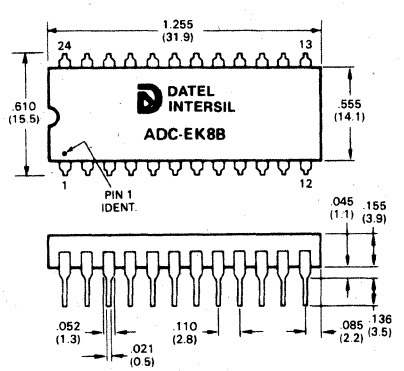


MECHANICAL DIMENSIONS
INCHES (MM)

CERAMIC
ACD-EK10B, 12B, 12DR, 12DM



PLASTIC
ADC-EK8B
ADC-EK12DC



DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, ADC-EK SERIES
(Typical at 25°C, ±5V Supplies, R_{BIAS} = 100K, unless otherwise noted)

	ADC-EK8B/10B/12B	ADC-EK12DC/DR/DM
MAXIMUM RATINGS		
I_{IN}	±10 mA	
I_{REF}	±10 mA	
Digital Input Voltage	−0.3V to V_{DD} + 0.3V	
$V_{DD} - V_{SS}$	18V	
Package Dissipation	500 mW	
ANALOG INPUTS		
Type Analog Input	Single Ended	
Full Scale Input Current	+10 μA	
Reference Current	−20 μA	
DIGITAL INPUTS		
Logical "1" V_{IN}	3.5V min	
Logical "0" V_{IN}	1.5V max.	
Start Convert Pulse	>3.5V for 500 nsec min.	
OUTPUTS		
Parallel Output Data	8, 10, 12 Lines	12 Lines and Overrange
Logic "1" Output Voltage	+4.5V min. at −10 μA, +2.4V min. at −360 μA[2]	
Logic "0" Output Voltage	+0.4 max. at −360 μA[2]	
E.O.C. (Status)	HI During Conversion, LO When Completed	
DATA VALID	HI When Data Valid, LO When Data Changing	
PERFORMANCE		
Resolution	8, 10, 12 Bits	3½ Digits
Coding	Straight Binary	BCD
Nonlinearity	½ LSB, max.	0.025% max
Differential Nonlinearity	¼ LSB, typ. ½ LSB max.	0.025% max.
Diff. Nonlinearity Tempco	±2.5 ppm/°C typ., ±5 ppm/°C max.	
No Missing Codes	Over Operating Temperature Range	
Initial Gain Error, Adj. to Zero	+5, −3% max[1]	
Gain Temperature Coefficient	±25 ppm/°C typ., ±75 ppm/°C max.[1]	
Initial Zero Error, Adj. to Zero	±50 mV max	
Zero Drift Tempco	±50 μV/°C max.[1]	
Conversion Time, max.	1.8 msec. (8 Bits) 6 msec. (10 Bits) 24 msec. (12 Bits)	12 msec. (3½ Digits)
Power Supply Sensitivity	±0.05% of Full Scale Gain[3]	
POWER REQUIREMENT		
Voltage, Rated Performance	±5 VDC	
Voltage Range, Operating	±3.5 VDC to ±7 VDC	
Supply Quiescent Current		
ADC-EK8B, EK12DC	5.0 mA	
ADC-EK10B, EK12B, EK12DR	2.5 mA max.	
ADC-EK12DM	3.5 mA max.	
PHYSICAL-ENVIRONMENTAL		
Operating Temp. Range	See Ordering Information	
Storage Temp. Range	−65°C to +150°C	
Package	24 Pin DIP	

NOTES: 1. For the ADC-EK12DM Only. Initial Gain Error is ±5%. Gain Tempco is ±40 ppm/°C typ., ±80 ppm/°C max. and Zero Drift Tempco is 80 μV/°C.
2. ADC-EK12DM outputs can sink and source 500 μA.
3. Supply Sensitivity given for $V_{DD} = V_{SS} = 5V \pm 1V$.

TECHNICAL NOTES

1. The ADC-EK series are CMOS devices and must be properly handled to prevent damage from static pick-up. Proper anti-static handling procedures should be observed including storage in conductive form or shorting all pins together with aluminum foil. Do not connect in circuits under "power on" conditions. The input voltage should be applied after power is on. Do not open circuit the zero adjust, reference, or start convert pins while power is on. It should also be noted that the top and bottom of the ceramic package are connected to the positive supply.
2. Nominal values of input, reference, and offset resistors are given in the resistor table. Due to the possible ±5% tolerance of the external reference and +5% −3% tolerance on the converter scale factor, the actual resistor value can vary by almost ±10%. R_G and R_T in the diagrams are for trimming gain and bipolar offset during calibration. It is recommended that R_G be 1% of R_{IN} (nominal) and R_T be 1% of R_{OFF} (nominal). They should both be 100ppm/°C cermet trimming pots. The recommended procedure for selecting R_{IN} and R_{OFF} is to set the R_G and R_T to center of range and then choose 1% metal film resistor which gives the nearest fit at the full scale point 1111...111 for R_{IN} and one that gives the nearest fit to zero scale point 1000...000 for R_T.
3. To choose any intermediate scale values for R_{IN} and R_T or values of R_{REF} for other reference voltages, use the following formulas:

$$R_{IN}\,(\text{nom.}) = \frac{FSR}{10\mu A}$$

FSR is full scale range or total input voltage span for the converter.

$$R_{OFF}\,(\text{nom.}) = \frac{V_{REF}}{5\mu A}$$

$$R_{REF}\,(\text{nom.}) = \frac{V_{REF}}{20\mu A}$$

It is recommended that large full-scale voltage ranges be chosen such

ORDERING INFORMATION

MODEL NO.	OPER. TEMP RANGE	PACKAGE
BINARY		
ADC-EK8B	0°C to +70°C	Plastic
ADC-EK10B	−25°C to +85°C	Ceramic
ADC-EK12B	−25°C to +85°C	Ceramic
BCD		
ADC-EK12DC	0°C to +70°C	Plastic
ADC-EK12DR	−25°C to +85°C	Ceramic
ADC-EK12DM	−55°C to +125°C	Ceramic

THESE CONVERTERS ARE COVERED UNDER GSA CONTRACT

TECHNICAL NOTES (Cont'd.)

as 0 to +10V, 0 to +5V etc. in order to keep the error due to input offset voltage drift to a minimum.

4. The temperature stability of the ADC-EK converters depends directly on the converter itself, R_{IN}, R_{REF}, R_{OFF}, and V_{REF}. Since the converter is typically ±20ppm/°C it is recommended that a **10ppm/°C reference be used along with 10ppm/°C metal film resistors for** R_{IN}, R_{REF}, and R_{OFF} for best performance over temperature. On a statistical basis this would give about 28ppm/°C stability for the complete converter.
5. Other passive components used with the converter may have tolerances as indicated here: R_C is a ±10% carbon comp. resistor; C_C is a ±20% ceramic capacitor; C_{INT} is a ±10% glass or ceramic capacitor; R_{BIAS} is a ±10% carbon comp. resistor; and the two zero adjust resistors are ±10% carbon composition type. It is recommended that two 0.1μF bypass capacitors be used right at the power supply pins. C_{INT} should be connected as close as possible to pins 14 and 15 away from any noisy lines.
6. The start convert pulse initiates conversion on the LO to HI transition after which the conversion cycle cannot be interrupted and must run to completion.
7. Logic signals should not be routed under these devices or near the input reference, or zero adjust pins.
8. The unused data output pins on the 8 and 10 bit models should not be used for external connection points since they have internal connections to the converter.
9. All digital outputs will drive 2 low power TTL loads or 1 low power Schottky TTL load. They should not be overloaded as this will affect the performance of the converter.
10. Conversion accuracy is directly dependent on V_{REF}. In order to avoid degrading accuracy, V_{REF} voltage regulation must be ±.04% for 8 bit models, ±.01% for 10 bit models and ±.0025% for 12 bit models.

INPUT/OUTPUT CONNECTIONS

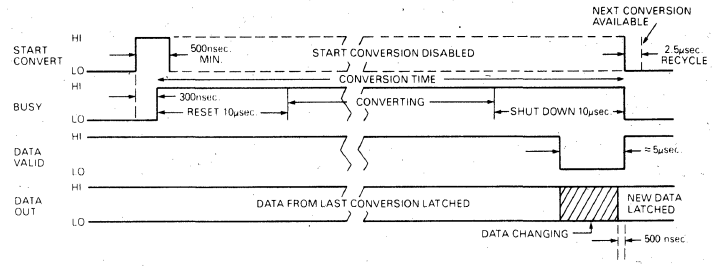
PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 OUT (MSB-12 BITS)	13	REFERENCE
2	BIT 2 OUT	14	ANALOG INPUT
3	BIT 3 OUT (MSB-10 BITS)	15	AMPLIFIER OUT
4	BIT 4 OUT	16	ZERO ADJUST
5	BIT 5 OUT (MSB-8 BITS)	17	BIAS
6	BIT 6 OUT	18	5V POWER
7	BIT 7 OUT	19	-5V POWER
8	BIT 8 OUT	20	GROUND
9	BIT 9 OUT	21	START CONVERT
10	BIT 10 OUT	22	E O C (STATUS)
11	BIT 11 OUT	23	DATA VALID
12	BIT 12 OUT (LSB-ALL)	24	BCD OVERRANGE*

*NO CONNECTION FOR OTHER MODELS

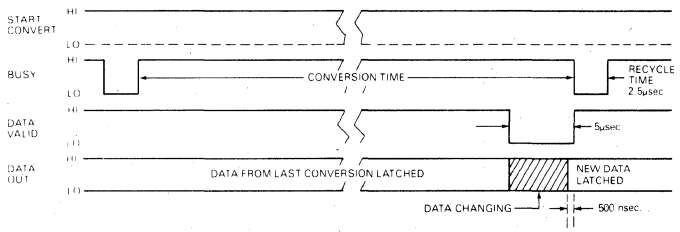
NOTE:
FOR 8 AND 10 BIT MODELS DO NOT CONNECT TO UNUSED DATA OUTPUT TERMINALS SINCE THEY HAVE INTERNAL CONNECTIONS

TIMING DIAGRAMS

CLOCKED OPERATION



FREE RUNNING OPERATION



CODING TABLES

STRAIGHT BINARY

SCALE	8 BIT		10 BIT		12 BIT	
	0 TO +10V	CODE	0 TO +10V	CODE	0 TO +10V	CODE
FS-1 LSB	+9.96V	1111 1111	+9.990V	11 1111 1111	+9.9976V	1111 1111 1111
½ FS	+5.00	1000 0000	+5.000	10 0000 0000	+5.0000	1000 0000 0000
1LSB	+0.04	0000 0001	+0.010	00 0000 0001	+0.0024	0000 0000 0001
0	0.00	0000 0000	0.000	00 0000 0000	0.0000	0000 0000 0000

OFFSET BINARY

SCALE	8 BIT		10 BIT		12 BIT	
	±5V	CODE	±5V	CODE	±5V	CODE
+FS-1 LSB	+4.96V	1111 1111	+4.990V	11 1111 1111	+4.9976V	1111 1111 1111
0	0.00	1000 0000	0.000	10 0000 0000	0.0000	1000 0000 0000
-FS + 1LSB	-4.96	0000 0001	-4.990	00 0000 0001	-4.9976	0000 0000 0001
-FS	-5.00	0000 0000	-5.000	00 0000 0000	-5.0000	0000 0000 0000

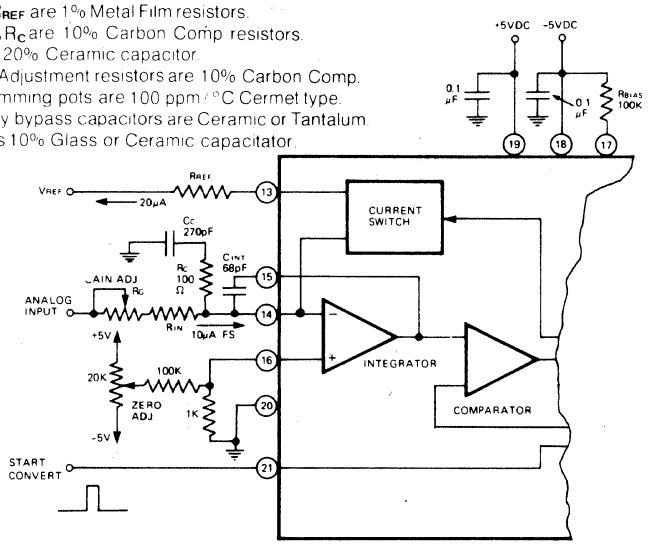
BCD

SCALE	FULL SCALE RANGE			CODE
	0 TO +2V	0 TO +10V	0 TO +20V	
FS-1 LSB	+1.999V	+9.995V	+19.990V	1 1001 1001 1001
½ FS	+1.000	+5.000	+10.000	1 0000 0000 0000
1 LSB	+0.001	+0.005	+ 0.010	0 0000 0000 0001
0	0.000	0.000	0.000	0 0000 0000 0000

CONNECTIONS AND CALIBRATION

CONNECTION FOR UNIPOLAR OPERATION

R_{IN}, R_{REF} are 1% Metal Film resistors.
R_{BIAS}, R_C are 10% Carbon Comp resistors.
C_C is 20% Ceramic capacitor.
Zero Adjustment resistors are 10% Carbon Comp.
All trimming pots are 100 ppm/°C Cermet type.
Supply bypass capacitors are Ceramic or Tantalum.
C_{INT} is 10% Glass or Ceramic capacitator.

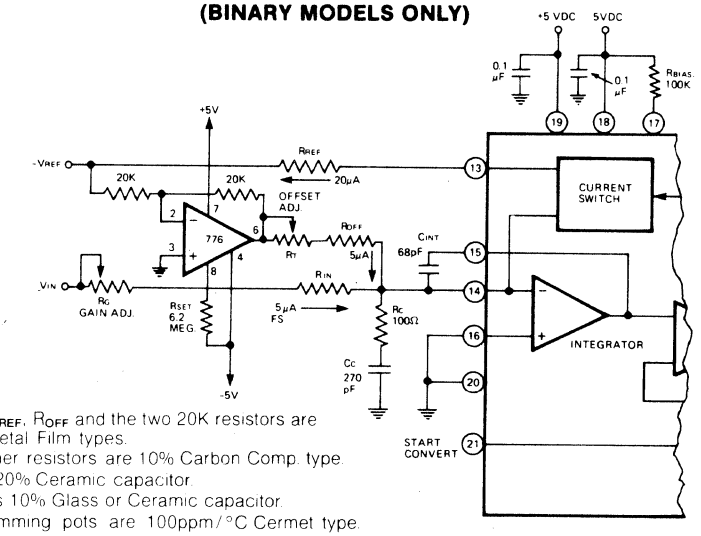


RESISTOR TABLES

UNIPOLAR RANGE	BIPOLAR RANGE	R_{IN} (NOM.)
0 TO +2V	±1V	200K
0 TO +5V	±2.5V	500K
0 TO +10V	±5V	1 MEG
0 TO +20V	±10V	2 MEG

V_{REF}	R_{REF} (NOM.)	R_{OFF} (NOM.)
-1.22V	61K	244K
-2.5V	125K	500K
-6.4V	320K	1.28 MEG.

CONNECTION FOR BIPOLAR OPERATION (BINARY MODELS ONLY)



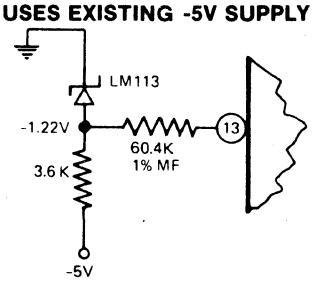
R_{IN}, R_{REF}, R_{OFF} and the two 20K resistors are 1% Metal Film types.
All other resistors are 10% Carbon Comp. type.
C_C is 20% Ceramic capacitor.
C_{INT} is 10% Glass or Ceramic capacitor.
All trimming pots are 100ppm/°C Cermet type.
Supply bypass capacitors are Ceramic or Tantalum.

CALIBRATION PROCEDURE

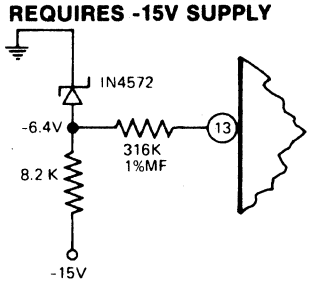
1. Connect the converter as shown in the connection diagrams for either unipolar or bipolar operation. Determine the input voltage range and select the required input resistors. Apply a logic HI to the start convert input (pin 21) to give free-running operation.
2. **Zero and Offset Adjustments.** Apply a precision voltage reference source from the analog input resistor to ground. Adjust the reference source to zero + ½ LSB for unipolar operation or -FS + ½ LSB for bipolar operation. Adjust the zero or offset potentiometer so that the output code flickers between 000....000 and 000....001.
3. **Gain Adjustment.** Set the output of the reference source to +FS −1½ LSB and adjust the gain trimming potentiometer so that the output code just flickers between 111....110 and 111....111.
   For BCD coding the output code should flicker between 1001 1001 1000 and 1001 1001 1001.

REFERENCE CIRCUITS

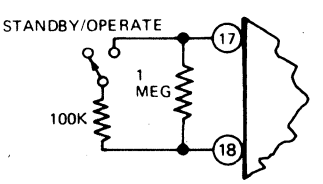
1.22V BAND GAP REFERENCE USES EXISTING -5V SUPPLY



6.4V ZENER REFERENCE REQUIRES -15V SUPPLY



REDUCTION OF STAND-BY POWER



This reduces power consumption to about 200µA during Standby

DATEL INTERSIL
11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617)339-9341 / TWX 710-346-1953 / TLX 951340
Santa Ana, (714)835-2751, (L.A.) (213)933-7256 • Sunnyvale, CA (408)733-2424 • Gaithersburg, MD (301)840-9490
• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Monolithic A/D Converters with Three-State Outputs ADC-ET Series

FEATURES

- **Monolithic CMOS**
- **Three State Outputs**
- **To 12 Bit Accuracy**
- **No Missing Codes**
- **Low Cost**
- **Microprocessor Compatible**

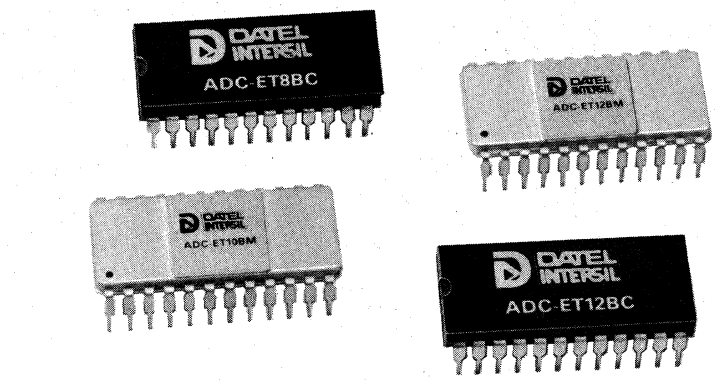
GENERAL DESCRIPTION

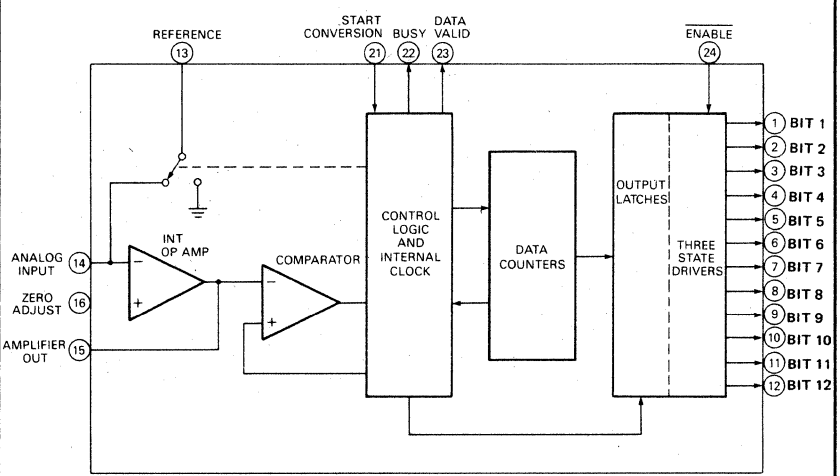
The ADC-ET series devices are low cost integrating A/D converters optimized for high accuracy, linearity and noise immunity. They operate at low power consumption, with sufficient speed to handle most industrial and instrumentation requirements. Discretely controllable three state outputs allow bus organized output connections making these units ideal for microprocessor interfacing.

Fabricated with monolithic CMOS techniques, each device is housed in a single 24 pin dual in-line package. The converter consists of an integrating operational amplifier, comparator, current switch, internal clock, two counters, latching output buffers and control logic circuitry. Operation of the circuit requires only a few external passive components and connection to external reference and power supplies. Conversion is accomplished by an incremental charge balancing technique which assures high linearity and noise immunity, along with inherent monotonicity resulting in no missing codes. At the completion of a conversion, the binary coded result appears in parallel form on discretely controlled latched outputs which are CMOS, low power TTL, or low power Schottky TTL compatible. The controllable outputs may be switched to a high impedance or off state by holding the $\overline{\text{ENABLE}}$ high.

Conversion times are 1.8, 6 and 24 msec. for the 8, 10 and 12 bit units respectively. Other typical specifications include linearity to ¼ LSB and a gain tempco of 25 ppm/°C. The analog input voltage range is programmable by means of an external resistor which sets the current into the integrator at 10 μA full scale. Standard operating mode is unipolar but bipolar operation can be implemented by using an external op amp to provide an offset current from the reference. Power requirement is ±5 VDC at 2 mA which, for intermittent duty applications, may be reduced to only 200 μA during standby periods without affecting data in the output latches.

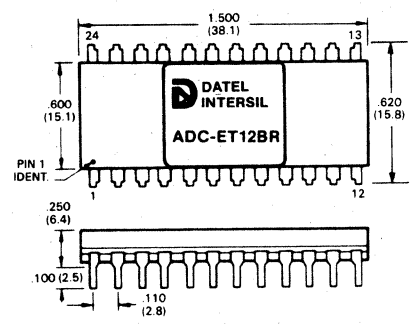
CAUTION: These are CMOS devices and may be damaged by static discharge.



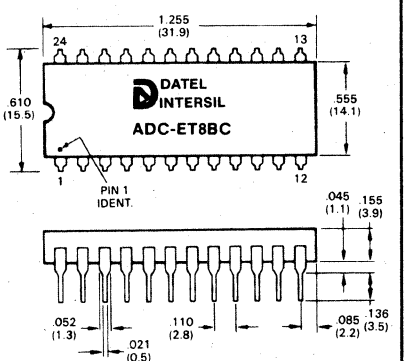


MECHANICAL DIMENSIONS INCHES (MM)

CERAMIC PACKAGE



PLASTIC PACKAGE



DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, ADC-ET SERIES
(Typical at 25 C, 5V Supplies, R_{BIAS} 100K Ω, unless otherwise noted)

MAXIMUM RATINGS

I_{IN}	±10 mA
I_{REF}	±10 mA
Digital Input Voltage	-0.3V to V_{DD} +0.3V
V_{DD}-V_{SS}	18V
Package Dissipation	500 mW

ANALOG INPUTS

Type Analog Input	Single Ended
Input Current Range	0 to +10 μA
Reference Current	-20 μA

DIGITAL INPUTS

Logical "1" V_{IN}	3.5V min.
Logical "0" V_{IN}	1.5V max.
Start Convert Pulse Width	500 nsec. min.
$\overline{\text{ENABLE}}$ Propagation Delay	500 nsec.

OUTPUTS

Output Off State Current	0.1 μA typ, ±10 μA max.
Logic "1" Output Voltage	+4.5V min at -10 μA +2.4V min at -360 μA[4]
Logic "0" Output Voltage	+0.4V max at 360 μA[4]
Data Valid Output	Hi for Data Valid, Lo When Loading
Busy Output	Hi During Conversion

PERFORMANCE

Resolution	8, 10, 12 Bits
Coding, Unipolar	Straight Binary
Bipolar	Offset Binary
Conversion Times	
8 Bits	1.8 msec. max
10 Bits	6 msec. max.
12 Bits	24 msec. max.
Nonlinearity	±1/4 LSB typ., ±1/2 LSB Max.[1]
Differential Nonlinearity	±1/4 LSB typ., ±1/2 LSB max.
Diff. Nonlinearity Tempco	±2.5 ppm/°C
No Missing Codes	Over Operating Temp. Range
Initial Gain Error, (Adj. to Zero)	±5% max.
Gain Temperature Coefficient	±25 ppm/°C typ, ±75 ppm/°C max.[2]
Initial Zero Error (Adj. to Zero)	±50 mV max.
Zero Drift Tempco	±50 μV/°C max.[2]
Power Supply Sensitivity	±0.05%/% max.[3]

POWER REQUIREMENT

Voltage, Rated Performance	±5 VDC
Voltage Range, Operating	±3.5 VDC to ±7 VDC
Supply Quiescent Current	
C Suffix	±5.0 mA max.
R Suffix	±2.5 mA max.
M Suffix	±3.5 mA max.

PHYSICAL-ENVIRONMENTAL

Operating Temperature Range	
C Suffix	0°C to +70°C
R Suffix	-25°C to +85°C
M Suffix	-55°C to +125°C
Package	
C Suffix	24 Pin Plastic DIP
R & M Suffix	24 Pin Ceramic DIP

NOTES:
1. Nonlinearity for model ADC-ET12BC only is typically ±1/4 LSB, ±1-1/2 LSB max.
2. For M suffix units only gain tempco is typically 40 ppm/°C, 80 ppm/°C max. and zero drift tempco is ±80 μV/°C.
3. V_{DD} ±1V, V_{SS} ±1V
4. M suffix logic outputs can sink and source 500 μA.

TECHNICAL NOTES

1. The ADC-ET series are CMOS devices and must be properly handled to prevent damage due to static discharge. Proper anti-static precautions should be taken, including storage and transport in anti-static containers or conductive foam, and grounding of work stations, handling equipment and personnel. Do not connect in circuits under "power on" conditions. The input voltage should be applied after power is on. Do not open circuit the zero adjust, reference or start convert pins while the power is on. It should be noted that the top and bottom of the ceramic package are connected to the positive supply.
2. Nominal values of input, reference and offset resistors are given in the resistor table. Due to the possible ±5% tolerance of the external reference and the +5%, -3% tolerance of the converter scale factor, the actual resistor value can vary by almost ±10%. R_G and R_T in the diagrams are for trimming gain and bipolar offset during calibration. It is recommended that R_G be 1% of R_{IN} (nominal) and that R_T be 1% of R_{OFF} (nominal). They should both be 100 PPM/°C cermet trimming pots. The recommended procedure for selecting R_{IN} and R_{OFF} is to set R_G and R_T to the center of their ranges and choose a 1% metal film resistor which gives the closest fit at the full scale point 1111....111 for R_{IN} and one that gives the closest fit to the zero scale point 0000...000 for R_T.
3. To choose any intermediate scale values for R_{IN} and R_T or values of R_{REF} for other reference voltages, use the following formulas:

$$R_{IN}\ (NOM.) = \frac{FSR}{10\mu A}$$

FSR is full scale range or total input voltage span for the converter.

$$R_{OFF}\ (NOM.) = \frac{V_{REF}}{5\mu A} \qquad R_{REF}\ (NOM.) = \frac{V_{REF}}{20\mu A}$$

It is recommended that large full scale voltage ranges be chosen, such as 0 to +10V, 0 to +5V etc., in order to keep the error due to input offset voltage drift to a minimum.
4. The temperature stability of the ADC-ET converters depends directly on the converter itself, R_{IN}, R_{REF}, R_{OFF} and V_{REF}. Since the converter is typically ±25ppm/°C it is recommended that a 10ppm/°C reference be used along with 10ppm/°C metal film resistors for R_{IN}, R_{REF} and R_{OFF} for best performance over temperature.
5. Passive components used with the converter may have tolerances as indicated here: C_c is a ±20% ceramic capacitor; C_{INT} is a ±10% glass or ceramic capacitor; R_{c1}, R_{BIAS} and the two zero adjust resistors are ±10% carbon composition type.
6. It is recommended that two 0.1 μF bypass capacitors be used at the power supply pins as shown in the connection diagram. C_{INT} should be connected as close as possible to pins 14 and 15 and as far as possible from any noisy lines.
7. Logic signals should not be routed under these devices or near the input, reference or zero adjust pins.
8. All digital outputs will drive two low power TTL loads or one low power Schottky TTL load. The outputs should not be overloaded as this will affect the performance of the converter.
9. It should be noted that there is a propagation delay of approximately 500 nsec. between the time $\overline{\text{ENABLE}}$ changes state and the time that the outputs change state.
10. For intermittent conversion applications the ADC-ET can be configured to use only 200μA during standby. In this mode the op amp and internal clock are shut down but data at the output latches remains available. See application diagram.
11. Two's complement coding can be implemented by inverting the MSB signal.
12. I_{IN} and I_{REF}, pins 14 and 13 respectively, connect to the summing junction of an operational amplifier which requires a current input. Voltage sources cannot be attached directly to them, but must be buffered by external resistors. Refer to Test Circuit Diagrams. Analog input can be any positive voltage when applied through the proper scaling resistor.
13. Conversion accuracy is directly dependent on V_{REF}. In order to avoid degrading accuracy, V_{REF} voltage regulation must be ±.04% for 8 bit models, ±.01% for 10 bit models and ±.0025% for 12 bit models.

DESCRIPTION OF OPERATION

When the START CONVERT input is strobed with a positive pulse of at least 500 nsec. duration, the busy line latches high and a start up cycle of approximately 10 μsec. begins, during which the integrating capacitor is discharged and both counters are reset. Conversion begins at the end of an internal reset pulse.

During conversion, the sum of a continuous current, I_{IN} and pulses of an inversely signed reference current I_{REF}, is integrated. I_{IN} is proportional to the analog input voltage and I_{REF} is proportional to the reference voltage. A pulse of I_{REF} is applied as required to maintain the summing input of the integrating op amp near zero. The total number of pulses of I_{REF} required to maintain the summing input near zero is counted and the binary coded result is latched into the outputs at the end of conversion.

The end of conversion is signaled by a pulse generated by the clock counter or by the data counter when an overflow condition occurs; this pulse disables further inputs into both counters and begins a 10 μsec. shutdown cycle. During the shutdown cycle, Data Valid goes low for 5 μsec., while the result of the latest conversion is being transferred to the outputs. Until transfer is complete, the data at the outputs is not valid. At the end of the shutdown cycle, Data Valid goes high indicating that the outputs are latched with the result of the last conversion, and the Busy Output goes low indicating the completion of the conversion cycle and the availability of the converter for the next conversion.

When the converter is employed in a free-running mode, the START CONVERT input is held high (simply connect pin 21 to pin 19), the Busy Output will go low for approximately 2.5 μsec. to mark the completion and initiation of consecutive conversion cycles. It should be noted that once conversion is initiated, the cycle cannot be interrupted; the START CONVERT pin is disabled when the Busy Output is high, and thus its logic state has no effect until completion of the conversion cycle. After the completion of a conversion, the output data remains valid for as long as power is applied to the circuit, or until Data Valid goes low at the end of a conversion.

RESISTOR TABLES

UNIPOLAR RANGE	BIPOLAR RANGE	R_{IN} (NOM.)
0 TO +2V	±1V	200K
0 TO +5V	±2.5V	500K
0 TO +10V	±5V	1 MEG
0 TO +20V	±10V	2 MEG

V_{REF}	R_{REF} (NOM.)	R_{OFF} (NOM.)
-1.22V	61K	244K
-2.5V	125K	500K
-6.4V	320K	1.28 MEG.

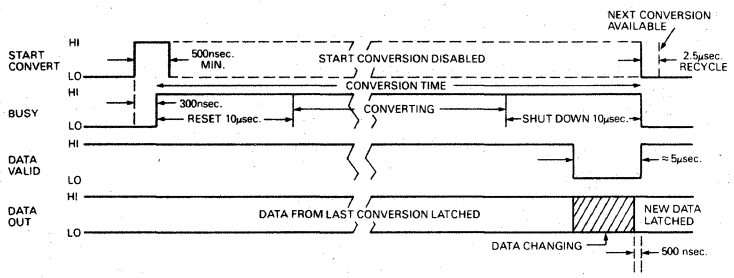
INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB-12 BITS)	13	REFERENCE
2	BIT 2	14	ANALOG INPUT
3	BIT 3 (MSB-10 BITS)	14	AMPLIFIER OUT
4	BIT 4	16	ZERO ADJUST
5	BIT 5 (MSB-8 BITS)	17	BIAS
6	BIT 6	18	-5V POWER
7	BIT 7	19	+5V POWER
8	BIT 8	20	GROUND
9	BIT 9	21	START CONVERT
10	BIT 10	22	BUSY OUTPUT
11	BIT 11	23	DATA VALID
12	BIT 12 (LSB-ALL)	24	ENABLE

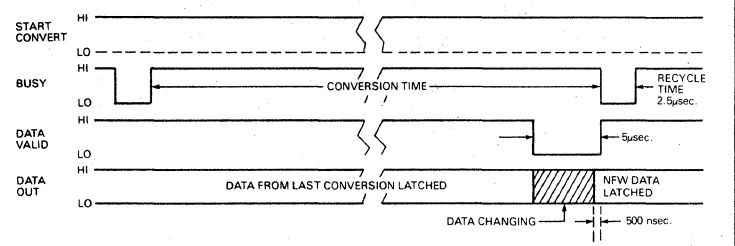
NOTE:
Do not connect unused data output pins on 8 and 10 bit models, they are internally connected to the converter.

TIMING DIAGRAMS

CLOCKED OPERATION



FREE RUNNING OPERATION



CODING TABLES

STRAIGHT BINARY

	8 BIT		10 BIT		12 BIT	
SCALE	0 TO +10V	CODE	0 TO +10V	CODE	0 TO +10V	CODE
FS-1 LSB	+9.96V	1111 1111	+9.990V	11 1111 1111	+9.9976V	1111 1111 1111
½ FS	+5.00	1000 0000	+5.000	10 0000 0000	+5.0000	1000 0000 0000
1LSB	+0.04	0000 0001	+0.010	00 0000 0001	+0.0024	0000 0000 0001
0	0.00	0000 0000	0.000	00 0000 0000	0.0000	0000 0000 0000

OFFSET BINARY

	8 BIT		10 BIT		12 BIT	
SCALE	±5V	CODE	±5V	CODE	±5V	CODE
+FS-1 LSB	+4.96V	1111 1111	+4.990V	11 1111 1111	+4.9976V	1111 1111 1111
0	0.00	1000 0000	0.000	10 0000 0000	0.0000	1000 0000 0000
-FS + 1LSB	-4.96	0000 0001	-4.990	00 0000 0001	-4.9976	0000 0000 0001
-FS	-5.00	0000 0000	-5.000	00 0000 0000	-5.0000	0000 0000 0000

ORDERING INFORMATION

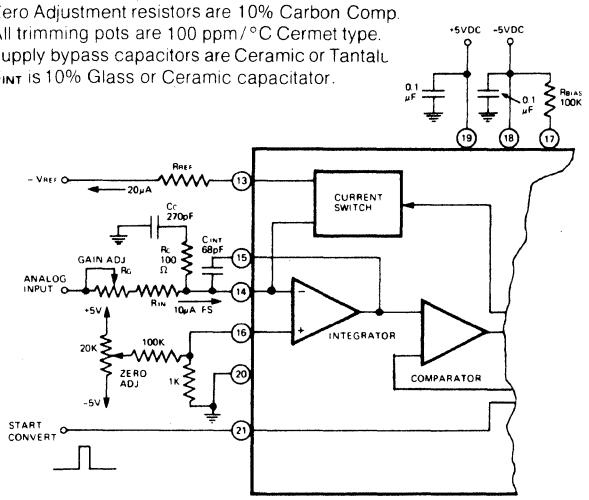
MODEL	OPERATING TEMP. RANGE	PACKAGE
ADC-ET8BC	0°C to +70°C	Plastic
ADC-ET8BM	-55°C to +125°C	Ceramic
ADC-ET10BC	0°C to +70°C	Plastic
ADC-ET10BM	-55°C to +125°C	Ceramic
ADC-ET12BC	0°C to +70°C	Plastic
ADC-ET12BR	-25°C to +85°C	Ceramic
ADC-ET12BM	-55°C to +125°C	Ceramic

THESE CONVERTERS ARE COVERED UNDER GSA CONTRACT

CONNECTIONS AND CALIBRATION

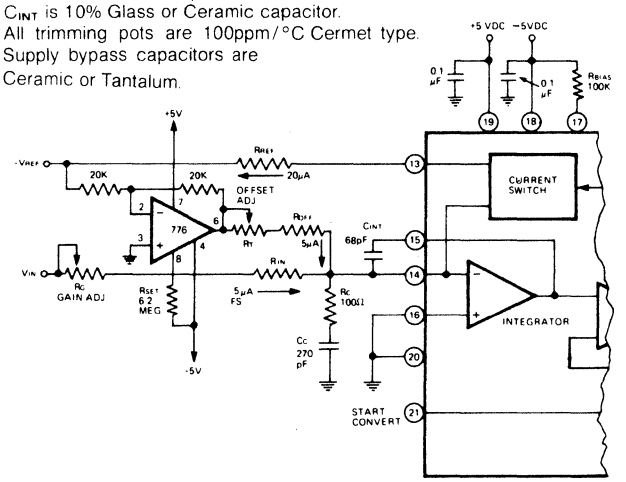
CONNECTION FOR UNIPOLAR OPERATION

R_{IN}, R_{REF} are 1% Metal Film resistors.
R_{BIAS}, R_C are 10% Carbon Comp resistors.
C_C is 20% Ceramic capacitor.
Zero Adjustment resistors are 10% Carbon Comp.
All trimming pots are 100 ppm/°C Cermet type.
Supply bypass capacitors are Ceramic or Tantalum.
C_{INT} is 10% Glass or Ceramic capacitator.

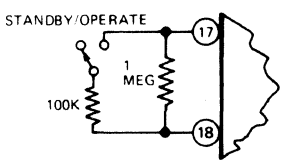


CONNECTION FOR BIPOLAR OPERATION

R_{IN}, R_{REF}, R_{OFF} and the two 20K resistors are 1% Metal Film types.
All other resistors are 10% Carbon Comp. type.
C_C is 20% Ceramic capacitor.
C_{INT} is 10% Glass or Ceramic capacitor.
All trimming pots are 100ppm/°C Cermet type.
Supply bypass capacitors are Ceramic or Tantalum.



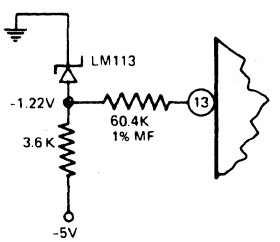
REDUCTION OF STAND-BY POWER



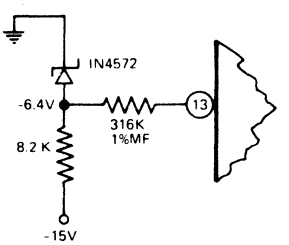
This reduces power consumption to about 200µA during Standby

REFERENCE CIRCUITS

1.22V BAND GAP REFERENCE USES EXISTING -5V SUPPLY



6.4V ZENER REFERENCE REQUIRES -15V SUPPLY



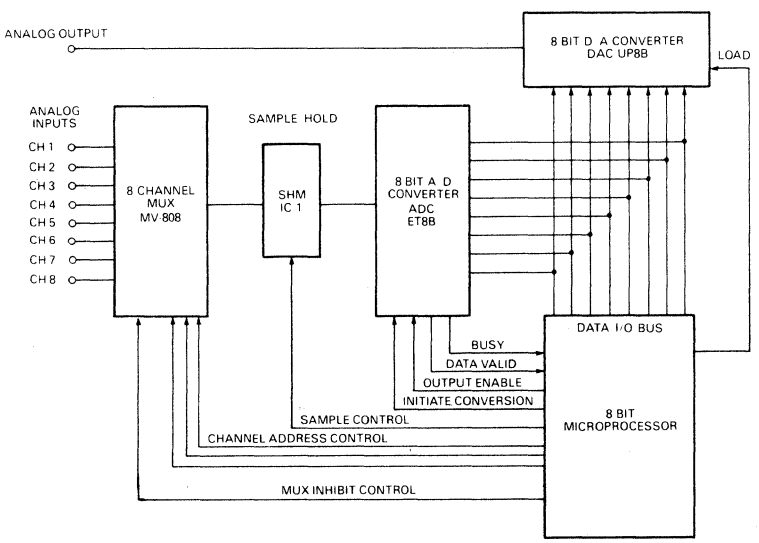
CALIBRATION PROCEDURE

1. Connect the converter as shown in the connection diagrams for either unipolar or bipolar operation. Determine the input voltage range and select the required input resistors. Apply a logic HI to the start convert input (pin 21) to give free-running operation.

2. **Zero and Offset Adjustments.** Apply a precision voltage reference source from the analog input resistor to ground. Adjust the reference source to zero + ½ LSB for unipolar operation or -FS + ½ LSB for bipolar operation. Adjust the zero or offset potentiometer so that the output code flickers between 000 .... 000 and 000 .... 001.

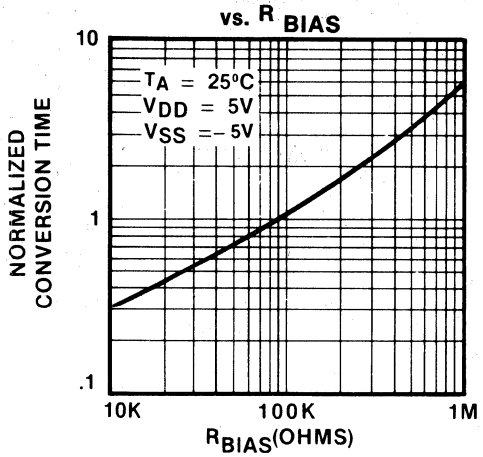
3. **Gain Adjustment.** Set the output of the reference source to +FS-1½ LSB and adjust the gain trimming potentiometer so that the output code just flickers between 111 .... 110 and 111 .... 111.

LOW COST MICROPROCESSOR A/D, D/A INTERFACE

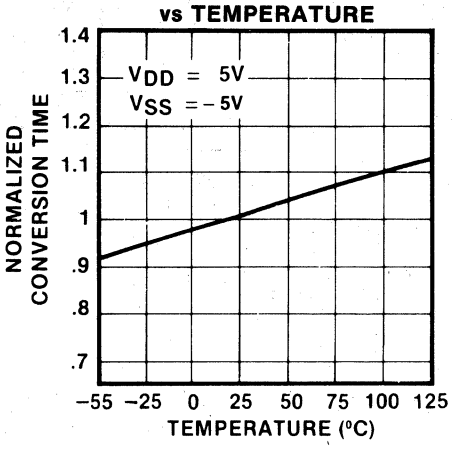


TYPICAL PERFORMANCE CURVES

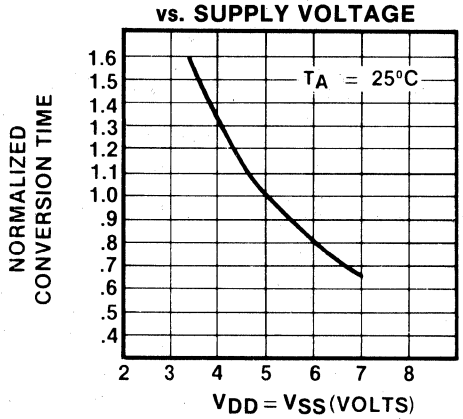
CONVERSION TIME vs. R_{BIAS}



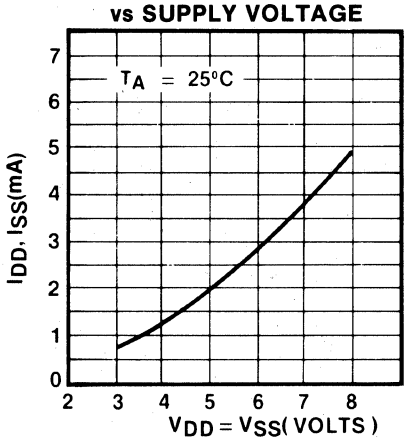
CONVERSION TIME vs TEMPERATURE



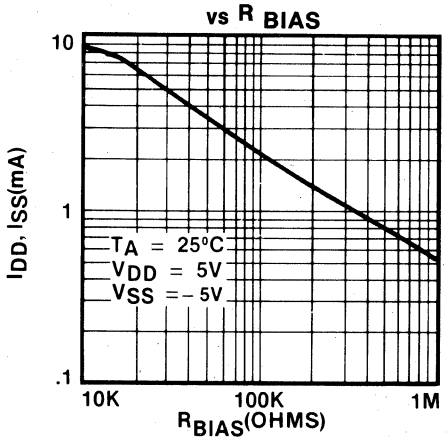
CONVERSION TIME vs. SUPPLY VOLTAGE



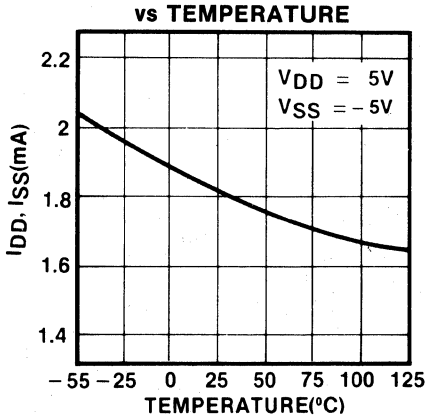
SUPPLY CURRENT vs SUPPLY VOLTAGE



SUPPLY CURRENT vs R_{BIAS}

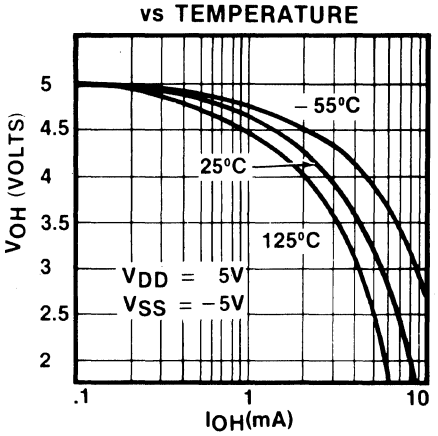


SUPPLY CURRENT vs TEMPERATURE

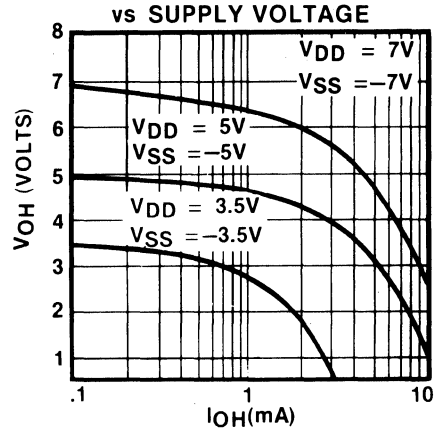


TYPICAL PERFORMANCE CURVES

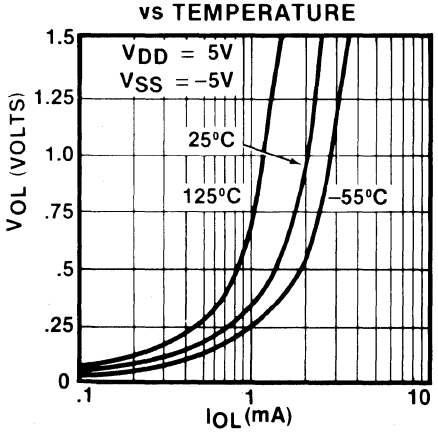
OUTPUT SOURCE CURRENT vs TEMPERATURE



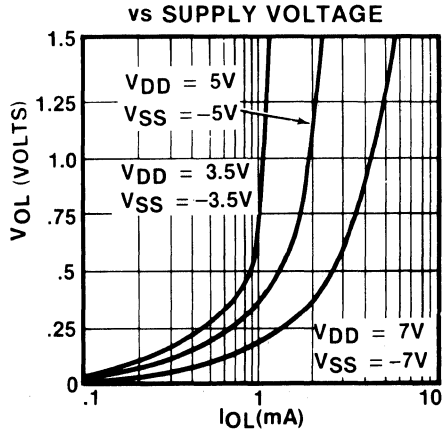
OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE



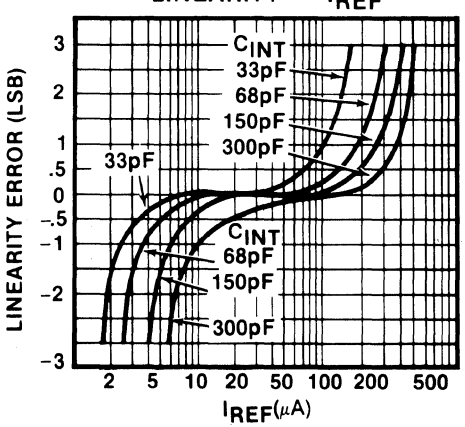
OUTPUT SINK CURRENT vs TEMPERATURE



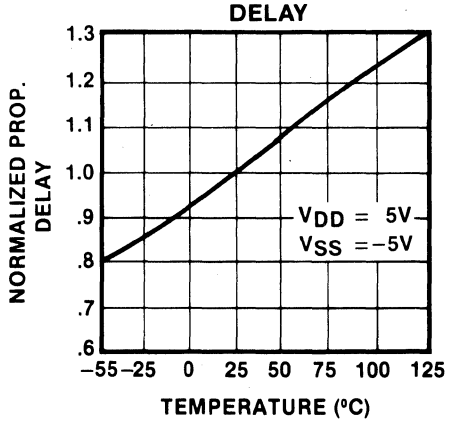
OUTPUT SINK CURRENT vs SUPPLY VOLTAGE



LINEARITY vs I_{REF}



THREE-STATE PROPAGATION DELAY



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PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Low Cost, 8 Bit Monolithic A/D and D/A Converters Models ADC-MC8BC, ADC-MC8BM

FEATURES

- **Low Cost**
- **8 Bit Resolution**
- **Internal Reference**
- **Single Supply Operation**
- **Multifunction-A/D-D/A**
- **Full Mil Temp. Range Available**

GENERAL DESCRIPTION

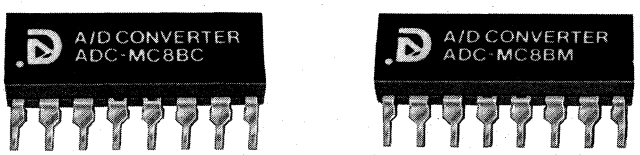
The ADC-MC8B is an 8-bit monolithic multifunction A/D-D/A converter with single +5 Volts supply operation. This device is a complete D/A converter which can be configured as an A/D converter by using the internal binary counter and two external IC's (311 comparator and a 74132 quad 2-input Schmitt trigger NAND gate).

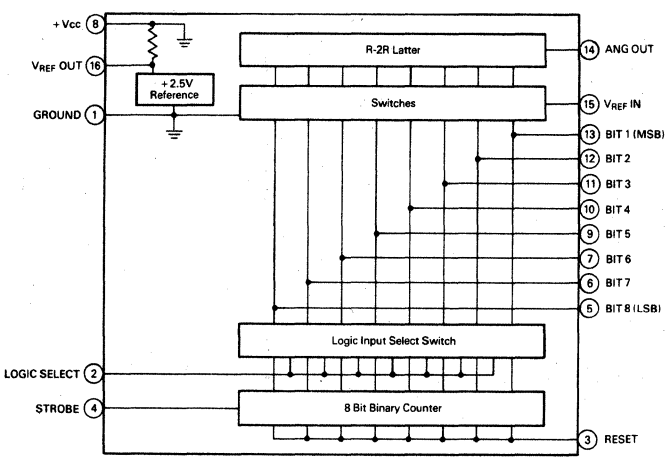
The ADC-MC8B consists of eight current switches, a specially designed ladder network using diffused resistors, a precision +2.5V reference, an eight bit binary counter and a logic input select switch. This feature allows a single control signal to determine whether the switches accept the output from the binary counter (A/D MODE) or external digital inputs (D/A MODE).

The converter can be used with the internal reference to give an output voltage range of 0 to +2.5V or connected to an external reference for a 0 to +3.0V range. Full scale settling time is 2.0μS MAX for the voltage output mode. Using the device as a counter-comparator A/D, a full scale conversion time of 500 μS can be achieved.

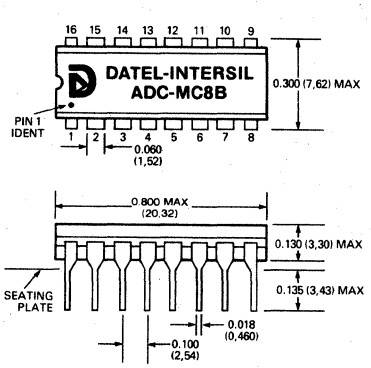
The ADC-MC8B is ideal for such applications as complete low cost D/A's, multiplying D/A's, low cost A/D's and precision ramp generators.

This converter is available in two operating temperature ranges. The ADC-MC8BC (0°C to 70°C) is packaged in a plastic 16 pin DIP and the ADC-MC8BM (-55°C to +125°C) is packaged in a ceramic DIP.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	9	BIT 5
2	LOGIC SELECT	10	BIT 4
3	RESET	11	BIT 3
4	STROBE	12	BIT 2
5	BIT 8 (LSB)	13	BIT 1 (MSB)
6	BIT 7	14	ANG OUT
7	BIT 6	15	V_{REF} IN
8	+Vcc	16	V_{REF} OUT

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, MODEL ADC-MC8B (Typical at 25°C, +5V supply unless otherwise noted)

MAXIMUM RATINGS

	ADC-MC8BC ADC-MC8BM
Supply Voltage, Vcc	+7.0V
Digital Input Voltage	+5.5V
Reference Input Voltage	+5.5V

INPUT/OUTPUTS

Coding, unipolar	Straight Binary
Coding, bipolar	Offset Binary
V_{REF} IN	0 to +3V
V_{REF} OUT	+2.55V[1]
Input Logic Level, Bit ON ("1")	+2.0V min.
Input Logic Level, Bit OFF ("0")	+0.7V max.
Output Logic Level, "1"	+2.4V min.
Output Logic Level, "0"	+0.4V max.
Logic Loading	1 TTL load
Parallel Output Data	12 Parallel lines of data held until next convert command.

REFERENCE

V_{REF} OUT	+2.55V
V_{REF} Tempco	±40 ppm/°C

D/A PERFORMANCE

Resolution	8 Bits (1 part in 256)	
Output Voltage Range	0 to +3.0V[2]	
Output Resistance	10K Ohms	
Nonlinearity	±1/2 LSB max.	±1 LSB max.[3]
Differential Linearity Error	±1/2 LSB max.	±1/2 LSB[4]
Zero Error	3 mV	8 mV
Gain Error	0.1%	
Zero Tempco	5μV/°C	
Gain Tempco	3 ppm/°C	
Nonlinearity Tempco	7.5 ppm/°C	
Monoticity	Guaranteed 0°C to +70°C	
Settling Time, full scale change to 1/2 LSB	2μS	
Settling Time, 1 LSB change to 1/2 LSB	1μS	

A/D PERFORMANCE

	ADC-MC8BC ADC-MC8BM
Analog Input Range	Dependent on values of R_1 & R_2 (See Range Select Chart)
Resolution	8 Bits (1 part in 256)
Nonlinearity	±1/2 LSB
Differential Nonlinearity	±1/2 LSB
Conversion Time	500μS max.[5]

POWER REQUIREMENT

Supply Voltage	+5.0V ±10%
Supply Current	30 mA typ., 40 mA max.

PHYSICAL-ENVIRONMENTAL

Operating Temperature Range	0°C to 70°C	-55°C to +125°C
Storage Temperature Range	-55°C to +125°C	
Package Type	16 Pin Plastic	16 Pin Ceramic

NOTES:

1. Internal Reference requires .22 μf stabilization capacitor between Pin 1 and 16.
2. 0 to +2.55V when using internal reference
3. ±1/2 LSB max. nonlinearity from 0°C to +70°C
4. ±1/2 LSB max. differential nonlinearity from 0°C to +70°C
5. See Graph CONV. TIME vs VIN

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	CASE
ADC-MC8BC	0 to 70°C	Plastic
ADC-MC8BM	-55°C to +125°C	Ceramic

Trimming Potentiometers: TP2K and TP10K are available from Datel-Intersil

THE ADC-MC8BC and ADC-MC8BM ARE COVERED BY GSA CONTRACT

THEORY OF OPERATION

A negative going pulse on the START line will reset counter to all zeros and enable the clock. If the DAC's output is less than ANG IN, the counter is incremented and DAC's output increases by one LSB. These comparisons continue until DAC's output is equal to the analog signal, at which time the EOC goes low (Logic "0") indicating that the digital output data is valid. Maximum clock frequency is 512 kHz. This may be varied by using different values for R and C.

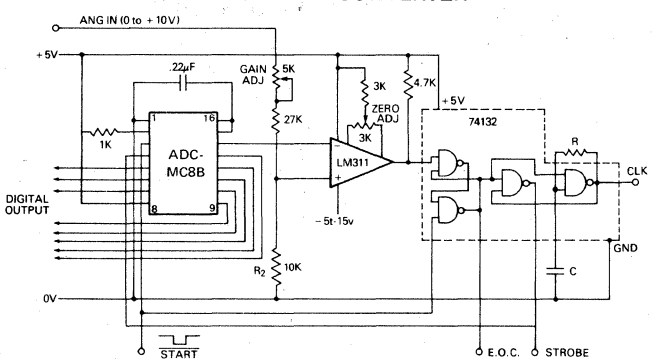
Full Scale voltage may also be changed by setting R_1 and R_2 to desired gain function.

1% Metal Film resistors and 100 ppm/°C trim pots are recommended for best performance over temperature.

CALIBRATION PROCEDURES

1. Connect converter as shown in connection diagram. Apply continuous start commands to the START input.
2. ZERO ADJUSTMENT—Ground analog input. Vary ZERO ADJ. potentiometer until LSB flickers between logic "1" and "0" with all other bits at logic "0".
3. GAIN ADJUSTMENT—Apply FS-1/2 LSB to ANG IN. Vary GAIN ADJ. potentiometer until LSB flickers between logic "1" and "0" with all other bits at logic"1".

8 BIT A/D CONVERTER



RANGE SELECT

FSR	R_2
10V	10K
5V	15K
2.5V	30K

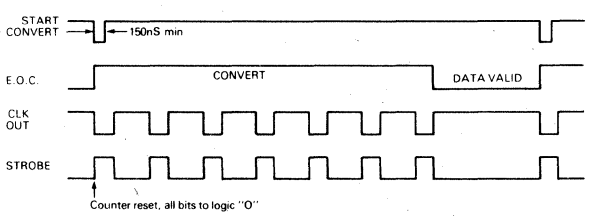
Conversion time – 500μS MAX

F_{CLK} = 512 KHZ

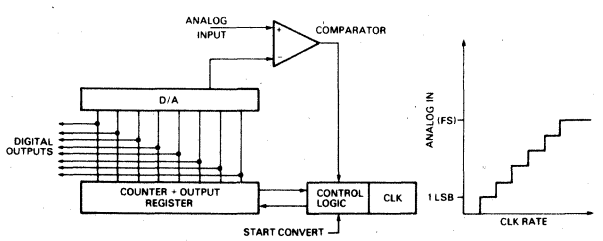
R = 560Ω

C = 2200pF

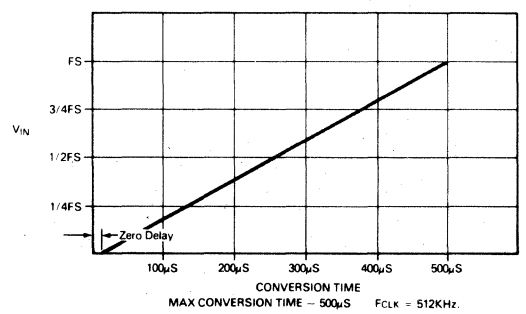
A/D TIMING DIAGRAM



COUNTER-COMPARATOR A/D



CONVERSION TIME VS. VIN



MAX CONVERSION TIME – 500μS F_{CLK} = 512KHz.

THEORY OF OPERATION

Vout is directly proportional to digital input. R_L should be kept ≥650K Ohms to assure good T.C. To remove offset voltage and calibration of converter, a buffer amplifier is necessary. The sources impedance of the inverting input should be approximately 6K Ohms to minimize temperature drift.

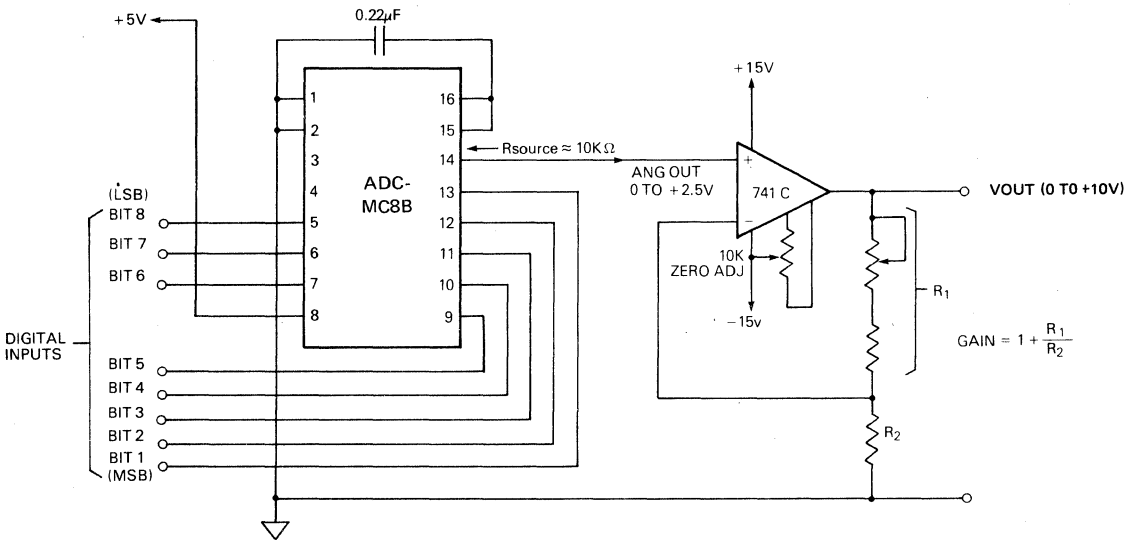
1% Metal Film resistors and 100 ppm/°C trim pots are recommended for best performance over temperature. For best settling time, a fast buffer amplifier is required (DATEL -INTERSIL'S AM-452).

CALIBRATION PROCEDURE

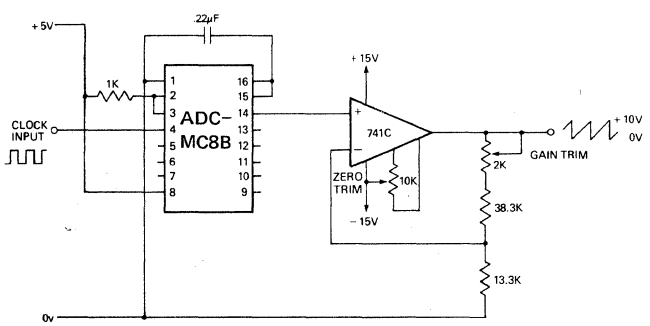
1. Connect converter as shown in connections diagram. Apply continuous start commands to the START input.
2. Set all bits to logic "0" and vary ZERO ADJ. potentiometer until Vout is equal to zero volts.
3. Set all bits to logic "1" and vary GAIN ADJ. potentiometer until Vout = Nominal F.S.– 1 LSB

$$LSB = \frac{FSR}{256}$$

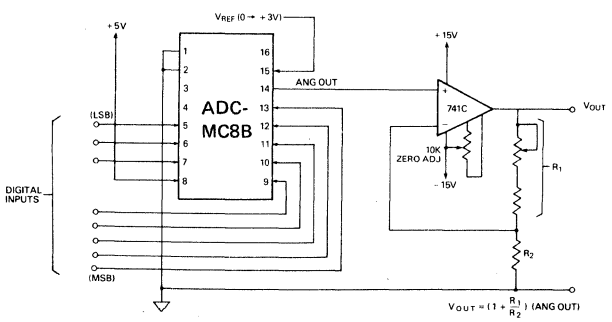
BASIC D/A WITH OUTPUT BUFFER



PRECISION RAMP GENERATOR



MULTIPLYING D/A



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• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

ADC-8068A/ADC-7104 Pair
16/14 Bit Binary A/D Converters for μProcessors

FEATURES

- **16 bit binary three-state latched outputs plus polarity and overrange. Also 14 bit version.**
- **Ideally suited for interface to UARTs, microprocessors, or other complex circuitry.**
- **Conversion on demand or continuously.**
- **Handshake byte-serial transmission synchronously or on demand.**
- **Guaranteed zero reading for zero volts input.**
- **True polarity at zero count for precise null detection.**
- **Single reference voltage for true ratiometric operation.**
- **Onboard clock and reference.**
- **Auto-Zero; Auto-Polarity**
- **Accuracy guaranteed to 1 count.**
- **All outputs TTL compatible.**
- **±10V analog input range**
- **Status signal available for external sync, A/Z in preamp, etc.**

GENERAL DESCRIPTION

The ADC-7104, combined with our model ADC-8068, forms a member of DATEL-INTERSIL's high performance A/D converter family. The 16-bit version, ADC-7104-16 performs the analog switching and digital function for a 16-bit binary A/D converter, with full three-state output, UART handshake capability, and other outputs for a wide range of output interfacing. The ADC-7104-14 is a 14 bit binary member of this series. The analog section, as with all DATEL-INTERSIL's integrating converters, provides fully precise Auto-Zero, Auto-Polarity (including ±0 null indication), single reference operation, very high input impedance, true input integration over a constant period for maximum EMI rejection, fully ratiometric operation, overrange indication, and a medium quality built-in reference. The chip pair also offers optional input buffer gain for high sensitivity applications, a built-in clock oscillator, and output signals for providing an external Auto-Zero capability in preconditioning circuitry, synchronizing external multiplexers, etc. The basic schematic connections are shown in Figure 1.

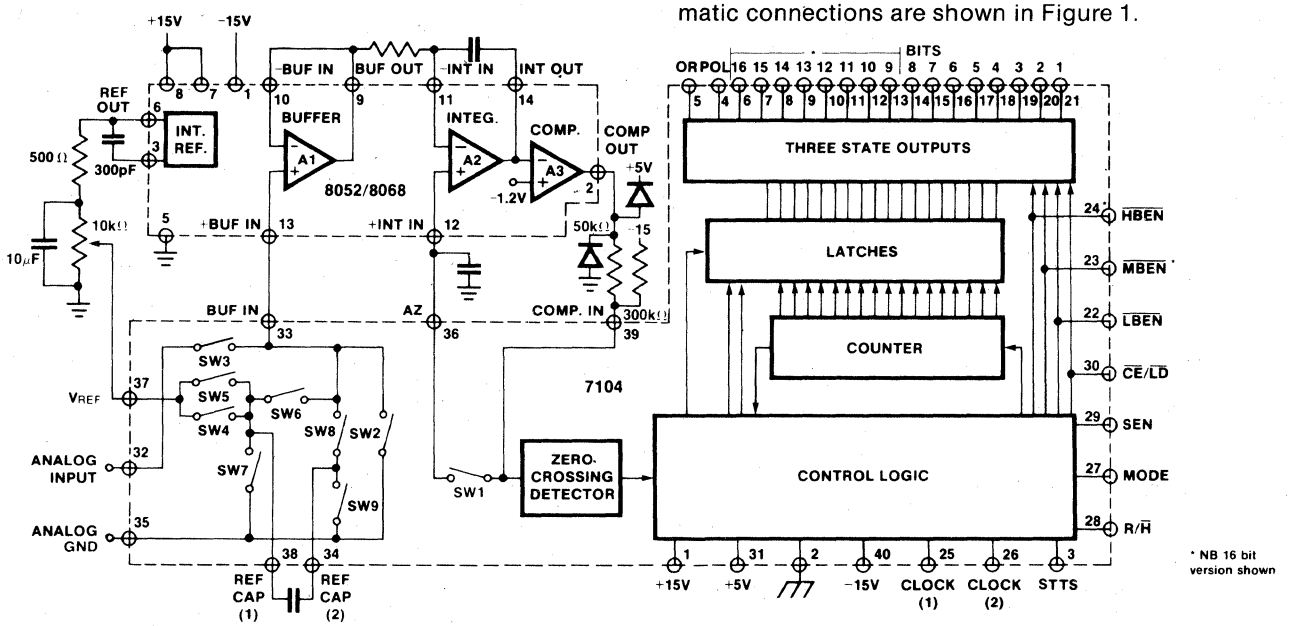

Figure 1: 8068A /7104 16/14 Bit A/D Converter Functional Block Diagram

ORDERING INFORMATION

MODEL*	DESCRIPTION	PACKAGE
ADC-7104-14C	14 Bit Digital Section	40 pin Epoxy DIP
ADC-7104-16C	16 Bit Digital Section	40 pin Epoxy DIP
ADC-8068AC	Analog Input Section	14 pin CerDIP

*Two chip A/D converter, requires ADC-8068AC and either ADC-7104-14C or ADC-7104-16C for complete function.

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ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 500 mW
Storage Temperature ..... −65°C to +150°C

8068

Supply Voltage ..... ±18V
Differential Input Voltage(8068) ..... ±30V

Input Voltage (Note 2) ..... ±15V
Output Short Circuit Duration,
All Outputs (Note 3) ..... Indefinite
Operating Temperature ..... 0°C to +70°C
Lead Temperature (Soldering, 60 Sec.)

7104

V+ Supply (GND to V+) 12
V++ to V− 32
Positive Supply Voltage (GND to V++) 17
Negative Supply Voltage (GND to V−) 17
Analog Input Voltage (Pin 32-39) (Note 4) ..... V+ to V−
Digital Input Voltage ..... V+ +0.3V
(Pins 2-30) (Note 5) ..... GND −0.3V

Note 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.
Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
Note 3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.
Note 4: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.
Note 5: Connecting any digital inputs or outputs to voltages greater than V+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources not on the same power supply be applied to the ADC-7104 before its power supply is established.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7104 ELECTRICAL CHARACTERISTICS (V+ = +5V, V++ = +15V, V- = -15V, Ta = 25°C)

CHARACTERISTICS		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Input	CLOCK 1	I_{IN}	Vin = +5V to 0V	±2	±7	±30	μA
Comparator I/P	COMP IN (Note 1)	I_{IN}	Vin = 0V to +5V	-10	±0.001	+10	μA
Inputs with Pulldown	MODE	I_{IH}	Vin = +5V	+1	+5	+30	μA
		I_{IL}	Vin = 0V	-10	±0.01	+10	μA
Inputs with Pullups	SEN, R/$\overline{H}$	I_{IH}	Vin = +5V	-10	±0.01	+10	μA
	$\overline{LBEN}$, $\overline{MBEN}$, $\overline{HBEN}$, $\overline{CE/LD}$ (Note 2)	I_{IL}	Vin = 0V	-30	-5	-1	μA
Input High Voltage	All Digital Inputs	V_{IH}		2.5	2.0	—	V
Input Low Voltage	All Digital Inputs	V_{IL}			1.5	1.0	V
Digital Outputs Three-Stated On	$\overline{LB\ EN}$	V_{OL}	I_{OL} = 1.6 mA	—	.27	.4	V
	$\overline{MB\ EN}$ (16 only) (Note 3)	V_{OH}	I_{OH} = −10μA		4.5	—	V
	$\overline{HB\ EN}$	V_{OH}	I_{OH} = −240μA	2.4	3.5	—	V
	$\overline{CE/LD}$						
	BIT n, POL, OR						
Digital Outputs Three-Stated Off	BIT n, POL, OR	I_{LO}	0 ≤ Vout ≤ V+	-10	±.001	+10	μA
Non-Three-State Digital Output	STTS	V_{OL}	I_{OL} = 3.2 mA	—	.3	.4	V
		V_{OH}	I_{OH} = −400μA	2.4	3.3	—	V
	CLOCK 2	V_{OL}	I_{OL} = 320μA		0.5		V
		V_{OH}	I_{OH} = −320μA		4.5		V
	CLOCK 3 -14 ONLY	V_{OL}	I_{OL} = 1.6 mA		.27	.4	V
		V_{OH}	I_{OH} = −320μA	2.4	3.5		V
Switch	Switch 1	$R_{DS}ON$		—	25k		Ω
	Switches 2,3	$R_{DS}ON$		—	4k	20k	Ω
	Switches 4,5,6,7,8,9	$R_{DS}ON$		—	2k	10k	Ω
	Switch Leakage	I_DOFF		—	15		pA
Clock	Clock Freq. (Note 4)			DC	200	400	kHz
Supply Currents	+5V Supply Current All outputs high impedance	I+	Freq. = 200 kHz		200	600	μA
	+15V Supply Current	I++	Freq. = 200 kHz		.3	1.0	mA
	-15V Supply Current	I-	Freq. = 200 kHz		25	100	μA
Supply Voltage Range	Logic Supply	V+	Note 5	4.0		+11.0	V
	Positive Supply	V++		+10.0		+16.0	V
	Negative Supply	V-		-16.0		-10.0	V

Note 1: This spec applies when not in Auto-Zero phase.
Note 2: These specs apply when these pins are inputs i.e. the mode pin is low, and the 7104 is not in handshake mode.
Note 3: These specs apply when these pins are outputs, i.e. the mode pin is high or the 7104 is in handshake mode.
Note 4: Clock circuit shown in Fig. 12 or 13.
Note 5: V+ must not be more positive than V++.

8068 ELECTRICAL CHARACTERISTICS (V_S = ±15V unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8068A MIN	8068A TYP	8068A MAX	UNITS
EACH OPERATIONAL AMPLIFIER					
Input Offset Voltage	V_{CM} = 0V		20	65	mV
Input Current (either input) (Note 1)	V_{CM} = 0V		80	150	pA
Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		dB
Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V_{CM} = ±2V		110		
Large Signal Voltage Gain	R_L = 50kΩ	20,000			V/V
Slew Rate			6		V/μs
Unity Gain Bandwidth			2		MHz
Output Short-Circuit Current			5	10	mA
COMPARATOR AMPLIFIER					
Small-signal Voltage Gain	R_L = 30kΩ				V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		-2.0	-2.6		V
VOLTAGE REFERENCE					
Output Voltage		1.60	1.75	1.90	V
Output Resistance			5		ohms
Temperature Coefficient			40		ppm/°C
Supply Voltage Range		±10		±16	V
Supply Current Total			8	14	mA

Note 1: The input bias currents are junction leakage currents which approximately double for every 10° C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta jA\ Pd$ where θjA is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

Note 2: This is the only component that causes error in dual-slope converter.

SYSTEM ELECTRICAL CHARACTERISTICS: 8068/7104

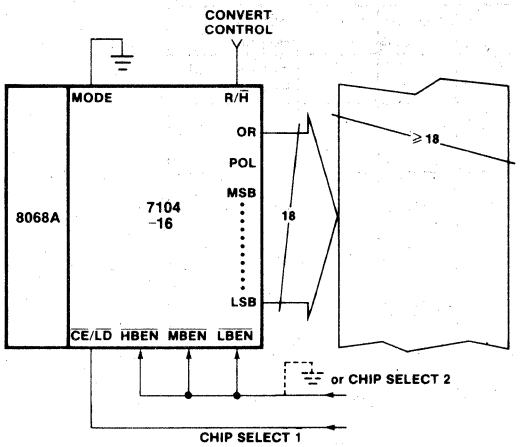
(V_{++} = +15V, V_+ = +5V, V_- = −15V Clock Frequency = 200KHz

CHARACTERISTICS	CONDITIONS	8068A/7104-14			8068A/7104-16			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	V_{in} = 0.0V Full Scale = 4.000V	-0.0000	±0.0000	+0.0000	-0.0000	±0.0000	+0.0000	Hexadecimal Reading
Ratiometric Reading (1)	$V_{in} = V_{Ref}$ Full Scale = 4.000V	1FFF	2000	2001	7FFF	8000	8001	Hexadecimal Reading
Linearity over ± Full Scale (error of reading from best straight line)	$-4V \leq V_{in} \leq +4V$		0.5	1		0.5	1	LSB
Differential Linearity (difference between worse case step of adjacent counts and ideal step	$-4V \leq V_{in} \leq +4V$		.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \approx +V_{in} \approx 4V$		0.5	1		0.5	1	LSB
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 4.000V		2			2		μV
Leakage Current at Input (2)	V_{in} = 0V		100	165		100	165	pA
Zero Reading Drift	V_{in} = 0V $0°C \leq T_A \leq 70°C$		0.5	2		0.5	2	μV/°C
Scale Factor Temperature Coefficient (3)	V_{in} = +4V $0 \leq T_A \leq 50°C$ (ext. ref. 0 ppm/°C)		2	5		2	5	ppm/°C

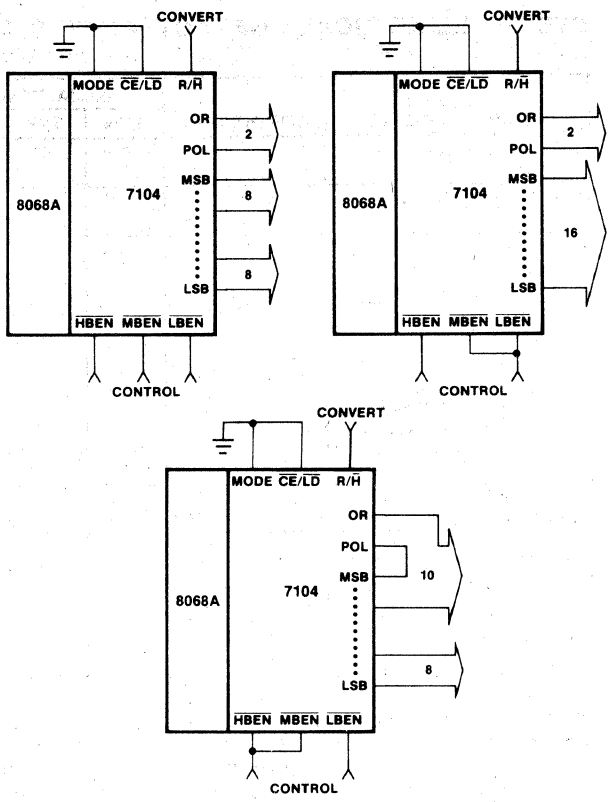
Note 1: Tested with low dielectric absorption integrating capacitor.

Note 2: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta jA\,Pd$ where θjA is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

Note 3: The temperature range can be extended to 70°C and beyond if the Auto-Zero and Reference capacitors are increased to absorb the high temperature leakage of the 8068. See note 2 above.



Full 18 Bit Three State Output



Various Combinations of Byte Disables

AC CHARACTERISTICS (V++ = +15V, V+ = +5V, V− = −15V)

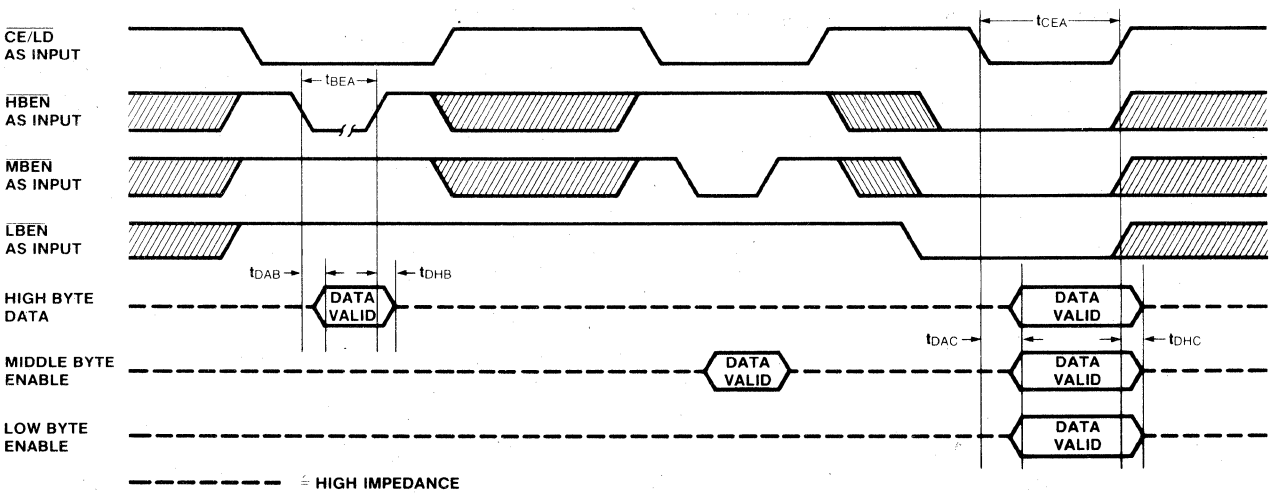


Figure 2: Direct Mode Output Timing

TABLE 1: Direct Mode Timing Requirements

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{BEA}	$\overline{XBEN}$ Min. Pulse Width		500		ns
t_{DAB}	Data Access Time from $\overline{XBEN}$		200		
t_{DHB}	Data Hold Time from $\overline{XBEN}$		200		
t_{CEA}	$\overline{CE/LD}$ Min. Pulse Width		500		
t_{DAC}	Data Access Time from $\overline{CE/LD}$		200		
t_{DHC}	Data Hold Time from $\overline{CE/LD}$		200		

TABLE 2: Handshake Timing Requirements

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{MW}	MODE Pulse (minimum)		20		ns
t_{SM}	MODE pin set-up time		−150		
t_{ME}	MODE pin high to low Z $\overline{CE/LD}$ high delay		200		
t_{MB}	MODE pin high to $\overline{XBEN}$ low Z (high) delay		200		
t_{CEL}	CLOCK 1 high to $\overline{CE/LD}$ low delay		700		
t_{CEH}	CLOCK 1 high to $\overline{CE/LD}$ high delay		600		
t_{CBL}	CLOCK 1 high to $\overline{XBEN}$ low delay		900		
t_{CBH}	CLOCK 1 high to $\overline{XBEN}$ high delay		700		
t_{CDH}	CLOCK 1 high to data enabled delay		1100		
t_{CDL}	CLOCK 1 low to data disabled delay		1100		
t_{SS}	Send ENable set-up time		−350		
t_{CBZ}	CLOCK 1 high to $\overline{XBEN}$ disabled delay		2000		
t_{CEZ}	CLOCK 1 high to $\overline{CE/LD}$ disabled delay		2000		

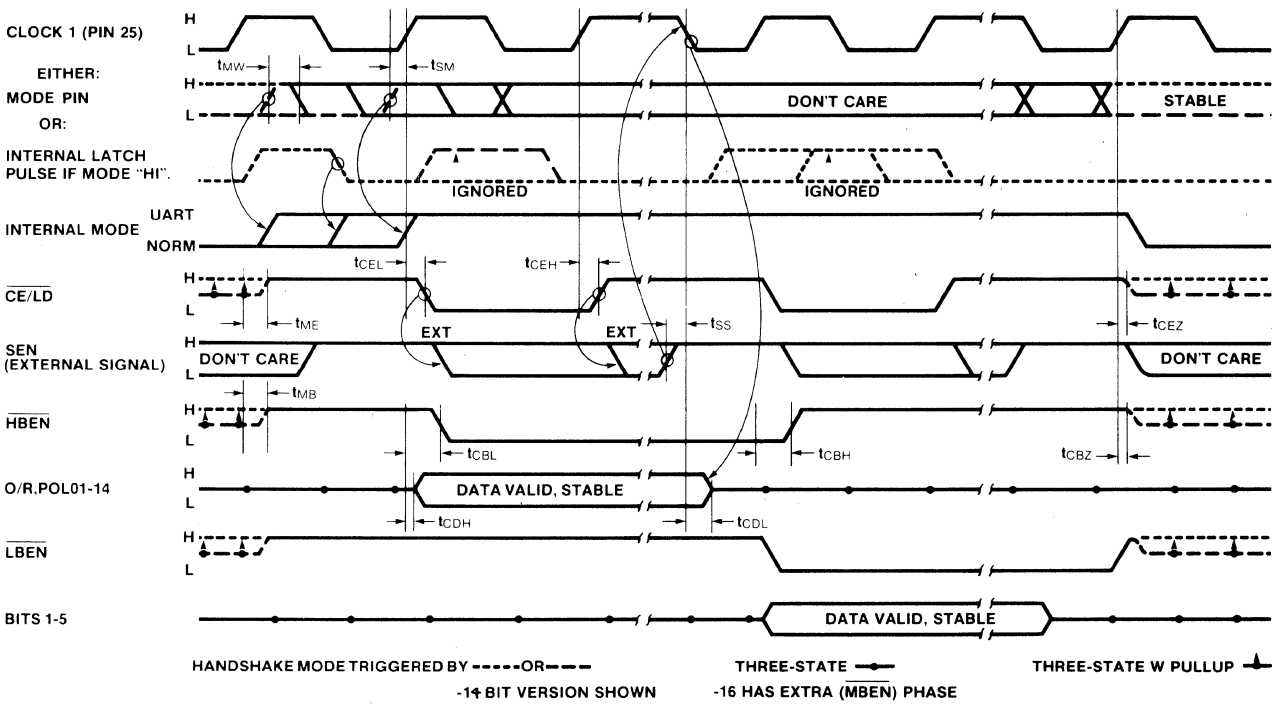
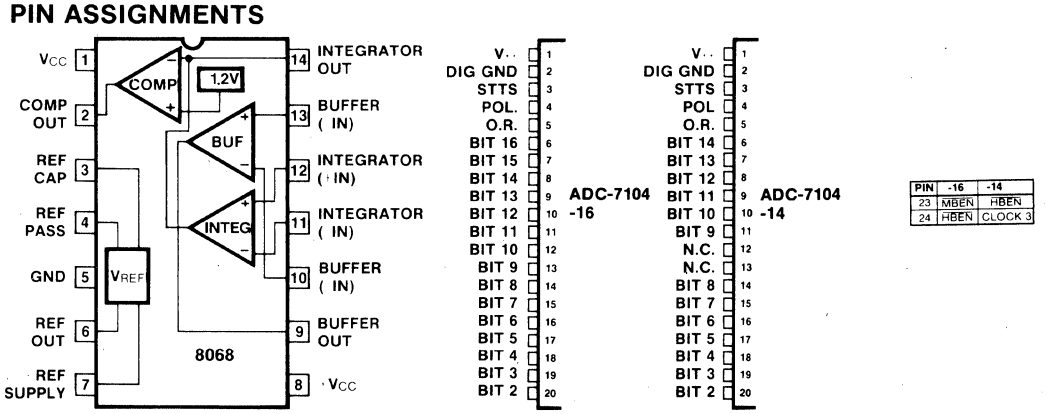


FIGURE 3: Timing Relationships In Handshake Mode

PIN ASSIGNMENTS



PIN	-16	-14
23	MBEN	HBEN
24	HBEN	CLOCK 3

TABLE 3: Pin Assignment and Function Description

PIN	SYMBOL	OPTION	DESCRIPTION
1	V(++)		Positive Supply Voltage Nominally +15V
2	GND		Digital Ground .0V, ground return
3	STTS		STaTuS output .HI during Integrate and Deintegrate until data is latched .LO when analog section is in Auto-Zero configuration.
4	POL		POLarity. Three-state output. HI for positive input.
5	OR		OverRange. Three-state output.
6	BIT 16 BIT 14	-16 -14	(Most significant bit)
7	BIT 15 BIT 13	-16 -14	Data Bits, Three-state outputs. See Table 4 for format of $\overline{\text{EN}}$ables and bytes.
8	BIT 14 BIT 12	-16 -14	
9	BIT 13 BIT 11	-16 -14	
10	BIT 12 BIT 10	-16 -14	
11	BIT 11 BIT 9	-16 -14	
12	BIT 10 nc	-16 -14	
13	BIT 9 nc	-16 -14	
14	BIT 8		
15	BIT 7		
16	BIT 6		
17	BIT 5		
18	BIT 4		
19	BIT 3		
20	BIT 2		
21	BIT 1		Least significant bit
22	$\overline{\text{LBEN}}$		Low Byte $\overline{\text{EN}}$able. If not in handshake mode (see pin 27) when LO (with $\overline{\text{CE}}/\overline{\text{LD}}$, pin 30) activates low-order byte outputs, BITS 1-8 When in handshake mode (see pin 27), serves as a low-byte flag output. See Figures 8, 9 and 10.
23	$\overline{\text{MBEN}}$ $\overline{\text{HBEN}}$	-16 -14	Mid Byte $\overline{\text{EN}}$able. Activates BITS 9-16, see $\overline{\text{LBEN}}$ (pin 22) High Byte $\overline{\text{EN}}$able. Activates BITS 9-14, POL, OR, see $\overline{\text{LBEN}}$ (pin 22)
24	$\overline{\text{HBEN}}$ CLOCK3	-16 -14	High Byte $\overline{\text{EN}}$able. Activates POL, OR, see $\overline{\text{LBEN}}$ (pin 22). RC oscillator pin. Can be used as clock output.

PIN	SYMBOL	DESCRIPTION
25	CLOCK1	Clock input. External clock or oscillator.
26	CLOCK2	Clock output. Crystal or RC oscillator.
27	MODE	Input LO;Direct output mode where $\overline{\text{CE}}/\overline{\text{LD}}$, $\overline{\text{HBEN}}$, $\overline{\text{MBEN}}$, and $\overline{\text{LBEN}}$ act as inputs directly controlling byte outputs. If pulsed HI causes immediate entry into handshake mode (see Figure 9). If HI, enables $\overline{\text{CE}}/\overline{\text{LD}}$, $\overline{\text{HBEN}}$, $\overline{\text{MBEN}}$, and $\overline{\text{LBEN}}$ as outputs. Handshake mode will be entered and data output as in Figures 7 & 8 at conversion completion.
28	R/$\overline{\text{H}}$	Run/$\overline{\text{Hold}}$; Input HI-conversions continuously performed every 2^{17} (-16) 2^{15} (-14) clock pulses. Input LO-conversion in progress completed, converter will stop in Auto-Zero 7 counts before input integrate.
29	SEN	Send-ENable: Input controls timing of byte transmission in handshake mode. HI indicates 'send'.
30	$\overline{\text{CE}}/\overline{\text{LD}}$	Chip-Enable/$\overline{\text{LoaD}}$. With MODE (pin 27) LO, $\overline{\text{CE}}/\overline{\text{LD}}$ serves as a master output enable; when HI, the bit outputs and POL, OR are disabled. With MODE HI, pin serves as a $\overline{\text{LoaD}}$ strobe (-ve going) used in handshake mode. See Figures 7 & 8.
31	V(+)	Positive Logic Supply Voltage. Nominally +5V.
32	AN.IN	ANalog INput. High side.
33	BUF IN	BUFfer INput to analog chip
34	REFCAP2	REFerence CAPacitor (negative side)
35	AN.GND.	ANalog GrouND. Input low side and reference low side.
36	A-Z	Auto-Zero node.
37	VREF	Voltage REFerence input (positive side)
38	REFCAP1	REFerence CAPacitor (positive side)
39	COMP-IN	COMParator INput from 8068
40	V(-)	Negative Supply Voltage. Nominally -15V.

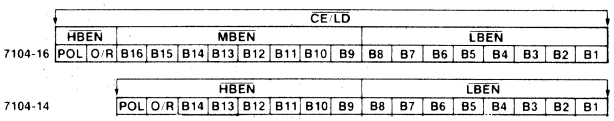


TABLE 4: Three-State Byte Formats and $\overline{\text{EN}}$able Pins.

DETAILED DESCRIPTION

Analog Section

Figure 4 shows the equivalent Circuit of the Analog Section of the 7104/8068 in the 3 different phases of operation. If the Run/Hold pin is left open or tied to V+, the system will perform conversions at a rate determined by the clock frequency: 131,072 for -16; 32,368 for -14 clock periods per cycle (see Figure 5 conversion timing).

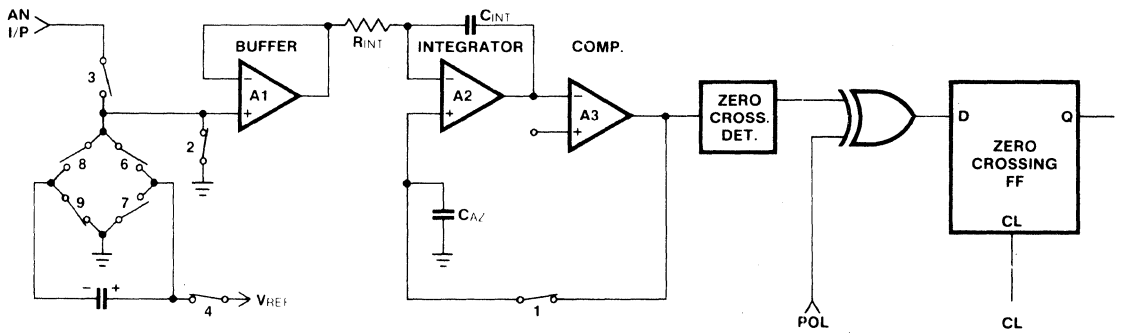


Figure 4A: Phase I Auto-Zero

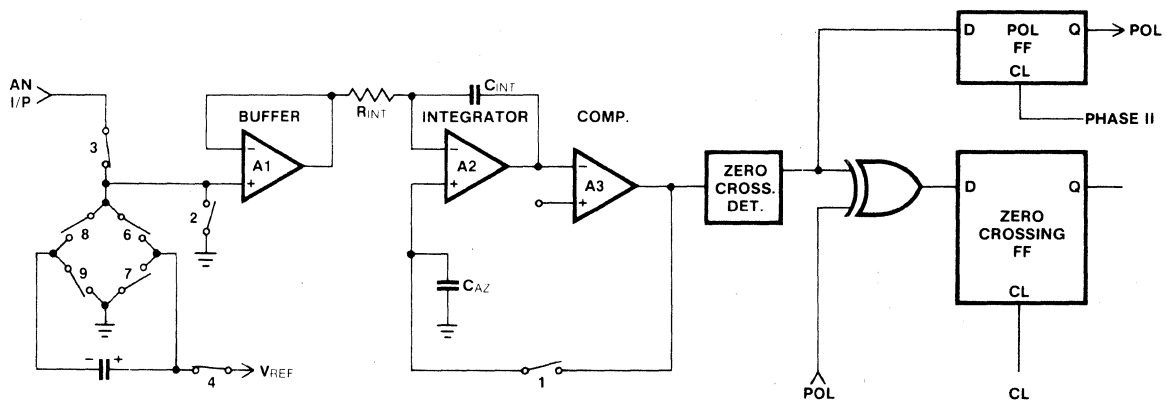


Figure 4B: Phase II Integrate Input

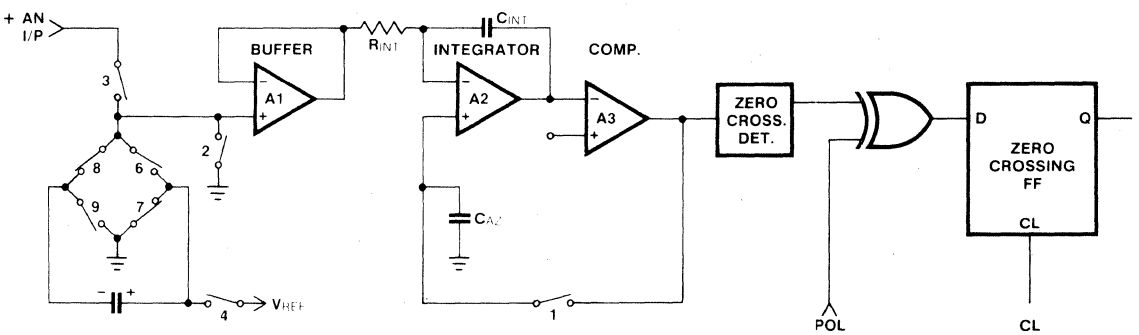


Figure 4C: Phase III + Deintegrate

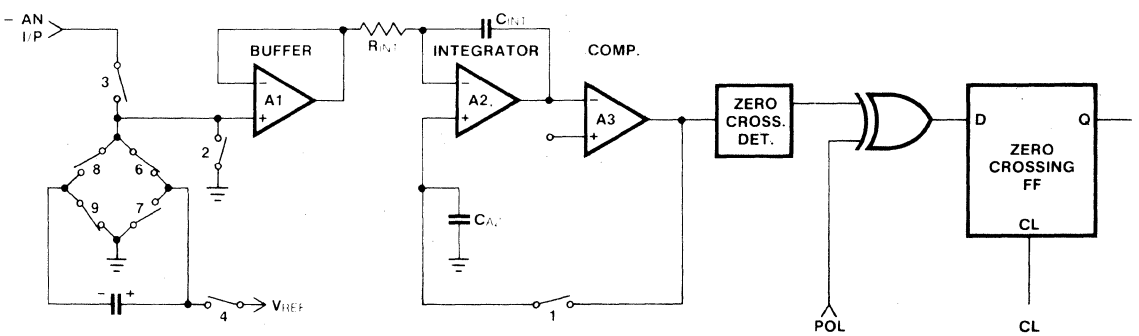


Figure 4D: Phase III - Deintegrate

Figure 4: Analog Section of 8068 with 7104

1. **Auto-Zero Phase I** Fig. 4A.

   During Auto-Zero, the input of the buffer is shorted to analog ground thru switch 2, and switch 1 closes a loop around the integrator and comparator. The purpose of the loop is to charge the Auto-Zero capacitor until the integrator output does not change with time. Also switches 4 and 9 recharge the reference capacitor to Vref.

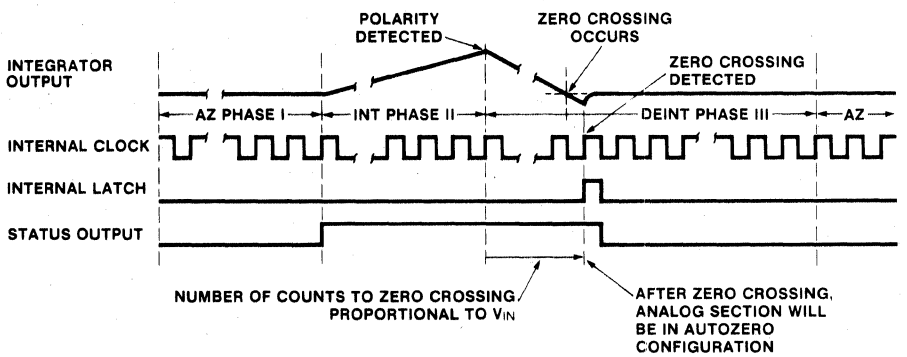
2. **Input Integrate Phase II** Fig. 4B.

   During input integrate the Auto-Zero loop is opened and the analog input is connected to the buffer input thru switch 3. (The reference capacitor is still being charged to V_{ref} during this time.) If the input signal is zero, the buffer, integrator and comparator will see the same voltage that existed in the previous state (Auto-Zero). Thus the integrator output will not change but will remain stationary during the entire Input Integrate cycle. If V_{in} is not equal to zero, an unbalanced condition exists compared to the Auto-Zero phase, and the integrator will generate a ramp whose slope is proportional to V_{in}. At the end of this phase, the sign of the ramp is latched into the polarity F/F.

Deintegrate Phase III Fig. 4 C&D

During the Deintegrate phase, the switch drive logic uses the output of the polarity F/F in determining whether to close switches 6 and 9 or 7 and 8. If the input signal was positive, switches 7 and 8 are closed and a voltage which is V_{ref} more negative than during Auto-Zero is impressed on the buffer input. Negative inputs will cause $+V_{ref}$ to be applied to the buffer input via switches 6 and 9. Thus, the reference capacitor generates the equivalent of a (+) reference or a (−) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to the zero-crossing point established in Phase I. The time, or number of counts, required to do this is proportional to the input voltage. Since the Deintegrate phase can be twice as long as the Input integrate phase, the input voltage required to give a full scale reading = $2V_{ref}$.

Note: Once a zero crossing is detected, the system automatically reverts to Auto-Zero phase for the leftover Deintegrate time (unless Run/$\overline{\text{Hold}}$ is manipulated, see Run/$\overline{\text{Hold}}$ Input in detailed description, digital section).



	COUNTS		
	Phase I	Phase II	Phase III
-16	32768	32768	65536
-14	8192	8192	16384

Figure 5: Conversion Timing

Table 5: Some Typical Component Values

V++ = +15V, V+ = 5V, V− = −15V, Clock Freq = 200 kHz

8068 with	7104-16			7104-14		UNITS
Full scale V_{IN}	200	800	4000	100	4000	mV
Buffer Gain	10	1	1	10	1	
R_{INT}	100	43	200	47	180	kΩ
C_{INT}	.33	.33	.33	0.1	0.1	μF
C_{AZ}	1.0	1.0	1.0	1.0	1.0	μF
C_{ref}	10	1.0	1.0	10	1.0	μF
V_{ref}	100	400	2000	50	2000	mV
Resolution	3.1	12	61	6.1	244	μV

Component Value Selection

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. This current should be small compared to the output short circuit current such that thermal effects are kept to a minimum and linearity is not affected. Values of 5 to 40 μA give good results with a nominal of 20 μA. The exact value may be chosen by

$$R_{INT} = \frac{\text{full scale voltage}^*}{20\mu A}$$

*Note: If gain is used in the buffer amplifier then -

$$R_{INT} = \frac{\text{(Buffer gain) (full scale voltage)}}{20\mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor is selected to give 9 volt swing for full scale inputs. This is a compromise between possibly saturating the integrator (at +14 volts) due to tolerance build-up between the resistor, capacitor and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. In general, the value of C_{INT} is give by

$$C_{INT} = \frac{\left[\begin{matrix}\text{(32768 for -16}\\ \text{(8192 for -14 X clock period)}\end{matrix}\right] \text{X } (20\mu A)}{\text{Integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it have low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale 100 . . . 000 and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

Note: When gain is used in the buffer amplifier the reference capacitor should be substantially larger than the auto-zero capacitor. As a rule of thumb, the reference capacitor should be approximately the gain times the value of the auto-zero capacitor. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the 7104 at 16 bits is one part in 65536, or 15.26ppm. Thus, if the reference has a temperature coefficient of 50ppm/°C (on board reference) a temperature change of 1/3°C will introduce a one-bit absolute error. For this reason, it is recommended that an external high quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

Buffer Gain

At the end of the auto-zero interval, the instantaneous noise voltage on the auto-zero capacitor is stored, and subtracts from the input voltage while adding to the reference voltage during the next cycle. The result is that this noise voltage effectively is somewhat greater than the input noise voltage of the buffer itself during integration. By introducing some voltage gain into the buffer, the effect of the auto-zero noise (referred to the input) can be reduced to the level of the inherent buffer noise. This generally occurs with a buffer gain of between 3 and 10. Further increase in buffer gain merely increases the total offset to be handled by the auto-zero loop, and reduces the available buffer and integrator swings, without improving the noise performance of the system. The circuit recommended for doing this with the 8068/ 7104 is shown in Figure 6. With careful layout, the circuit shown can achieve effective input noise voltages on the order of 1-2μV, allowing full 16-bit use with full scale inputs of as low as 150mV. Note that at this level, thermo-electric EMFs between PC boards, IC pins, etc., due to local temperature changes can be very troublesome.

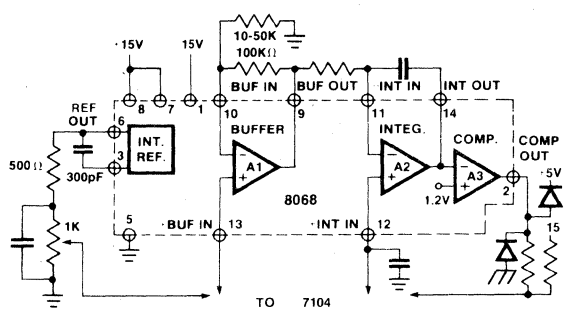


Figure 6: Adding Buffer Gain to 8068

DETAILED DESCRIPTION

Digital Section

The digital section includes the clock oscillator circuit, a 16 bit or 14 bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic and UART handshake logic, as shown in the Block Diagram Figure 7 (16 bit verison shown).

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined under "ADC-7104 Electrical Characteristics". For minimum power consumption, all inputs should swing from GND (low) to V+ (high). Inputs driven from TTL gates should have 3-5kΩ pull-up resistors added for maximum noise immunity.

Mode Input

The MODE input is used to control the output mode of the converter. When the MODE pin is connected to GND or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in three bytes for the 7104-16 or two bytes for the 7104-14, then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

STaTuS Output

During a conversion cycle, the STaTuS output goes high at the beginning of Input Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 5 for details of this timing. This signal may be used as a "data valid" flag (data never changes while STaTuS is low) to drive interrupts, or for monitoring the status of the converter.

Run/$\overline{\text{Hold}}$ Input

When the Run/$\overline{\text{Hold}}$ input is connected to V+ or left open (this input has a pullup resistor to ensure a high level when the pin is left open), the circuit will continuously perform conversion cycles, updating the output latches at the end of every Deintegrate (Phase III) portion of the conversion cycle (See Figure 5). (See under "Handshake Mode" for exception.) In this mode of operation, the conversion cycle will be performed in 131,072 for 7104-16, or 32768 for 7104-14 clock periods, regardless of the resulting value.

If Run/$\overline{\text{Hold}}$ goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to eliminate the time spent in Deintegrate after the zero-crossing. If Run/$\overline{\text{Hold}}$ stays or goes low, the converter will ensure a minimum Auto-Zero time, and then wait in Auto-Zero until the Run/$\overline{\text{Hold}}$ input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STaTuS output will go high) seven clock periods after the high level is detected at Run/$\overline{\text{Hold}}$. See Figure 8 for details.

Using the Run/$\overline{\text{Hold}}$ input in this manner allows an easy "convert on demand" interface to be used. The converter may be held at idle in Auto-Zero with Run/$\overline{\text{Hold}}$ low. When Run/$\overline{\text{Hold}}$ goes high the conversion is started, and when the STaTuS output goes low the new data is valid (or transferred to the UART - see Handshake Mode). Run/$\overline{\text{Hold}}$ may now go low terminating Deintegrate and ensuring a minimum Auto-Zero time before stopping to wait for the next conversion. Alternately, Run/$\overline{\text{Hold}}$ can be used to minimize conversion time by ensuring that it goes low during Deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the Run/$\overline{\text{Hold}}$ input can be provided by connecting it to the CLOCK3 (-14), CLOCK2 (-16) Output. In this mode the conversion time is dependent on the input value measured.

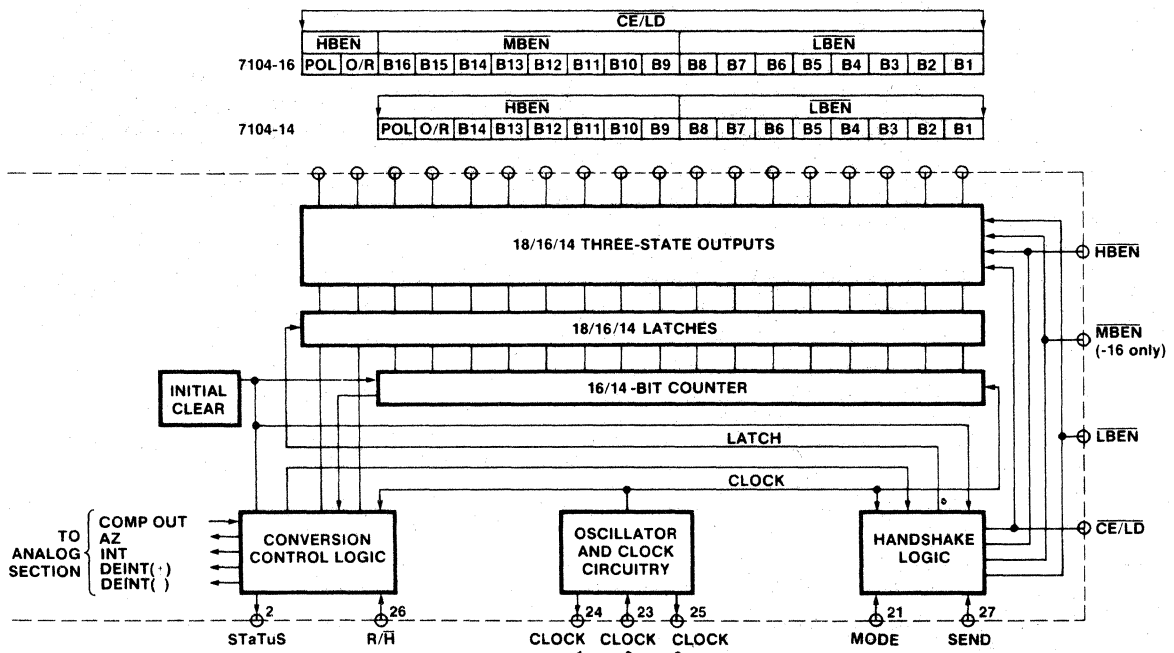


Figure 7: Digital Section

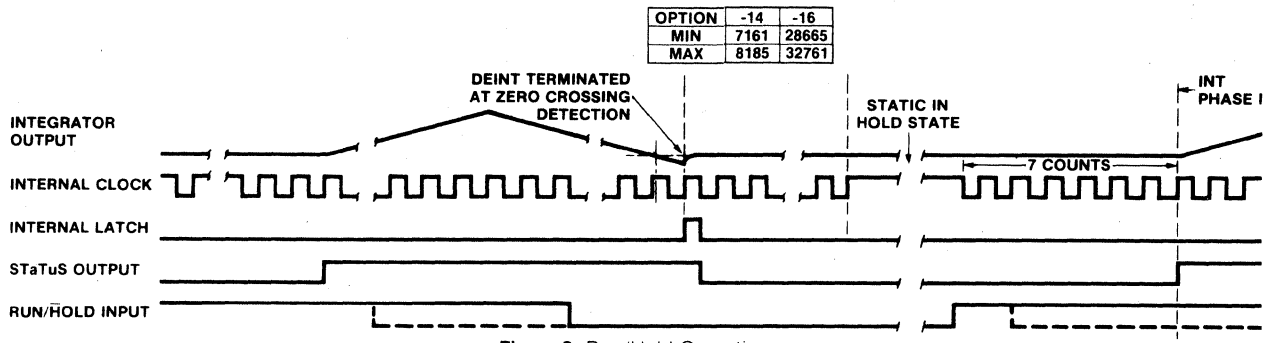


Figure 8: Run/Hold Operation

If the Run/Hold input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for Run/Hold to go high. As above, Integrate (Phase II) begins seven clock periods after the high level is detected.

Direct Mode

When the MODE pin is left at a low level, the data outputs (bits 1 through 8 low order byte, see Table 4 for format of middle (-16) and high order bytes) are accessible under control of the byte and chip ENable terminals as inputs. These ENable inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip ENable input is low, taking a byte ENable input low will allow the outputs of that byte to become active (three-stated on). This allows a variety of parallel data accessing techniques to be used, as shown in Figure 2. The timing requirements for these outputs are shown in Figure 2 and Table 1.

It should be noted that these control inputs are asynchronous with respect to the converter clock - the data may be accessed at any time. Thus it is possible to access the data while it is being updated, which could lead to scrambled data. Synchronizing the access of data with the conversion cycle by monitoring the STaTuS output will prevent this. Data is never updated while STaTuS is low. Also note the potential bus conflict described under "Initial Clear Circuitry".

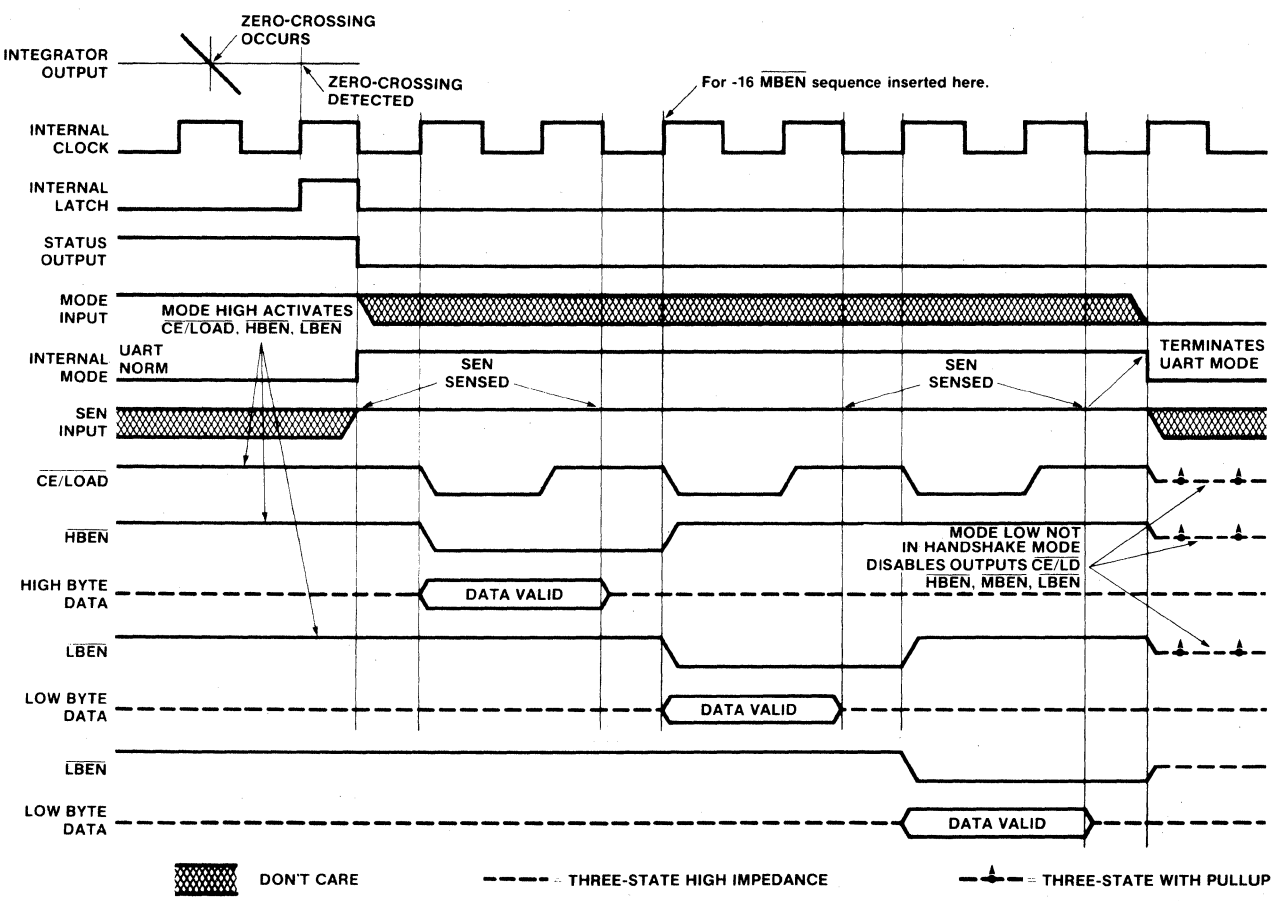


Figure 9: Handshake With SEN Held Positive

Handshake Mode

The handshake output mode is provided as an alternative means of interfacing the 7104 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte ENable inputs. This mode is specifically designed to allow a direct interface between the 7104 and industry-standard UARTs (such as the Intersil CMOS UART's, IM6402/3) with no external logic required. When triggered into the handshake mode, the 7104 provides all the control and flag signals necessary to sequence the three (7106-16) or two (7104-14) bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission to minimize the number of lines to the central controlling processor.

Entry into the handshake mode will occur if either of two conditions are fulfilled; first, if new data is latched (i.e. a conversion is completed) while MODE pin (pin 27) is high, in which case entry occurs at the end of the latch cycle; or secondly, if the MODE pin goes from low to high, when entry will occur immediately (if new data is being latched, entry is delayed to the end of the latch cycle). While in the handshake mode, data latching is inhibited, and the MODE pin is ignored. (Note that conversion cycles will continue in the normal manner). This allows versatile initiation of handshake operation without danger of false data generation; if the MODE pin is held high, every conversion (other than those completed during handshake operations) will start a new handshake operation, while if the MODE pin is pulsed high, handshake operations can be obtained "on demand."

When the converter enters the handshake mode, or when the MODE input is high, the chip and byte $\overline{\text{E}}$Nable terminals become TTL-compatible outputs which provide the control signals for the output cycle. The Send $\overline{\text{E}}$Nable pin (SEN) (pin 29) is used as an indication of the ability of the external device to receive data. The condition of the line is sensed once every clock pulse, and if it is high, the next (or first) byte is enabled on the next rising CLOCK 1 (pin 25) clock edge, the corresponding byte $\overline{\text{E}}$Nable line goes low, and the Chip $\overline{\text{E}}$Nable/LoaD line (pin 30) (CE/LD) goes low for one full clock pulse only, returning high.

On the next falling CLOCK 1 clock pulse edge, if SEN remains high, or after it goes high again, the byte output lines will be put in the high impedance state (or three-stated off). One half pulse later, the byte $\overline{\text{E}}$Nable pin will be cleared high, and (unless finished) the CE/LD and the next byte ENable pin will go low. This will continue until all three (2 in the case of 14 bit devices) bytes have been sent. The bytes are individually put into the low impedance state i.e.: three-stated on during most of the time that their byte ENable pin is (active) low. When receipt of the last byte has been acknowledged by a high SEN, the handshake mode will be cleared, re-enabling data latching from conversions, and recognizing the condition of the MODE pin again. The byte and chip ENable will be three-stated off, if MODE is low, but held high by their (weak) pull-ups. These timing relationships are illustrated in Figure 9, 10, and 11, and Table 2.

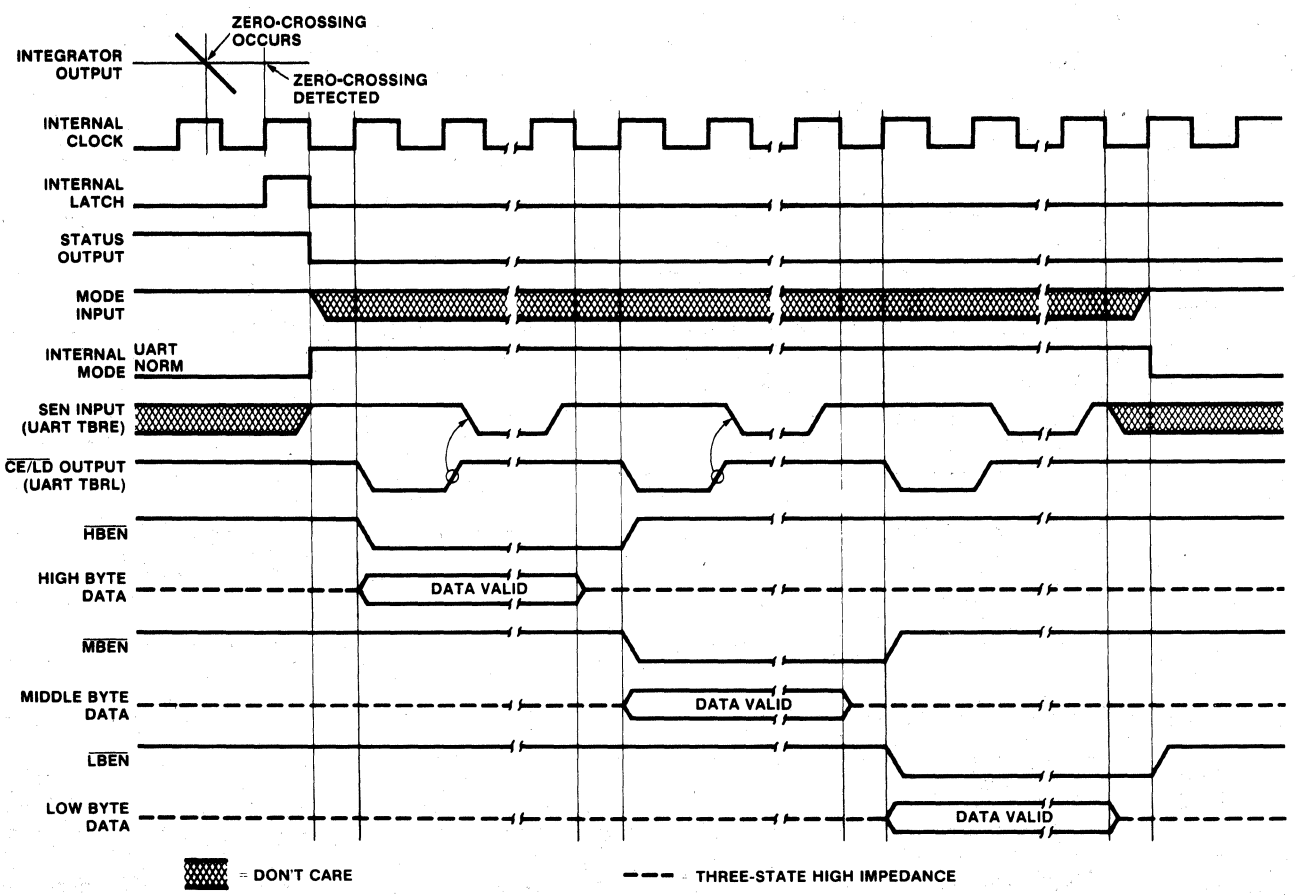


Figure 10: Handshake - Typical UART Interface Timing

Figure 9 shows the sequence of the output cycle with SEN held high. The handshake mode (Internal MODE high) is entered after the data latch pulse (since MODE remains high the $\overline{CE}/\overline{LD}$, $\overline{LBEN}$, $\overline{MBEN}$ and $\overline{HBEN}$ terminals are active as outputs). The high level at the SEN input is sensed on the same high to low internal clock edge. On the next low to high internal clock edge, the $\overline{CE}/\overline{LD}$ and the $\overline{HBEN}$ outputs assume a low level and the high-order byte (POL and OR, and except for -16, Bis 9-14) outputs are enabled. The $\overline{CE}/\overline{LD}$ output remains low for one full internal clock period only, the data outputs remain active for 1-1/2 internal clock periods, and the high byte $\overline{EN}$able remains low for two clock periods. Thus the $\overline{CE}/\overline{LD}$ output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte $\overline{EN}$able as an output may be used as a byte identification flag. With SEN remaining high the converter completes the output cycle using $\overline{CE}/\overline{LD}$, $\overline{MBEN}$ and $\overline{LBEN}$ while the remaining byte outputs (see Table 4) are activated. The handshake mode is terminated when all bytes are sent (3 for -16, 2 for -14, -12).

Figure10 shows an output sequence where the SEN input is used to delay portions of the sequence, or handshake, to ensure correct data transfer. This timing diagram shows the relationships that occur using an industry-standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEN input to the ICL7104 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{CE}/\overline{LD}$ terminal of the ICL7104 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

Assuming the UART Transmitter Buffer Register is empty, the SEN input will be high when the handshake mode is entered after new data is stored. The $\overline{CE}/\overline{LD}$ and $\overline{HBEN}$ terminals will go low after SEN is sensed, and the high order byte outputs become active. When $\overline{CE}/\overline{LD}$ goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the $\overline{HBEN}$ output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next 7104 internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the $\overline{HBEN}$ output returns high. At the same time, the $\overline{CE}/\overline{LD}$ and $\overline{MBEN}$ (-16) or $\overline{LBEN}$ outputs go low, and the corresponding byte outputs become active. Similarly, when the $\overline{CE}/\overline{LD}$ returns high at the end of one clock period, the enabled data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7104 internal clock high to low edge, disabling the data outputs. For the 16 bit device, the sequence is repeated for $\overline{LBEN}$. One-half internal clock later, the handshake mode will be cleared, and the chip and byte $\overline{EN}$able terminals return high and stay active (as long as MODE stays high).

With the MODE input remaining high as in these examples, the converter will output the results of every conversion

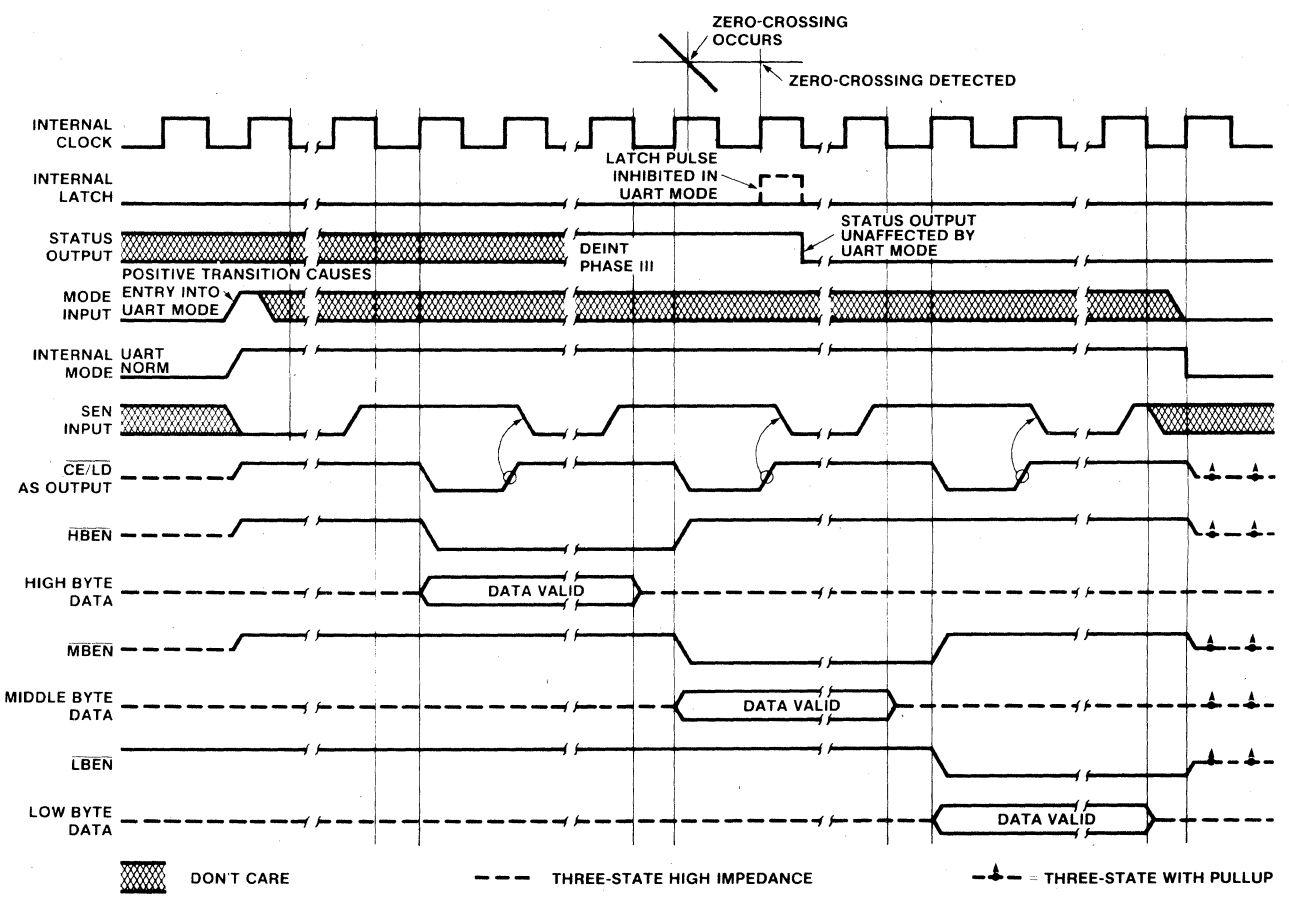


Figure 11: Handshake Triggered By Mode

except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 11 shows a handshake output sequence triggered by such an edge. In addition, the SEN input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEN input, and the sequence for the first (high order) byte is similar to the sequence for the other bytes. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STaTuS output and Run/$\overline{\text{Hold}}$ input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

Initial Clear Circuitry

The internal logic of the 7104 is supplied by an internal regulator between V++ and Digital Ground. The regulator includes a low-voltage detector that will clear various registers. This is intended to ensure that on initial power-up, the control logic comes up in Auto-Zero, with the 2nd, 3rd, and 4th MSB bits cleared, and the "mode" FF cleared (i.e. in "direct" mode). This, however, will also clear these registers if the supply voltage "glitches" to a low enough value. Additionally, if the supply voltage comes up too fast, this clear pulse may be too narrow for reliable clearing. In general, this is not a problem, but if the UART internal "MODE" FF should come up set, the byte and chip ENable lines will become active outputs. In many systems this could lead to buss conflicts, especially in non-handshake systems. In any case, SEN should be high (held high for non-handshake systems) to ensure that the MODE FF will be cleared as fast as possible (see Fig. 9 for timing). For these and other reasons, adequate supply bypass is recommended.

Oscillator

The 7104 is provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be over-driven, or may be operated as an RC or crystal oscillator.

Figure 12 shows the oscillator configured for RC operation. The internal clock will be of the same frequency and phase as the voltage on the CLOCK 3 pin. The resistor and capacitor should be connected as shown. The circuit will oscillate at a frequency given by f = .45/RC. An 100kΩ resistor is recommended for useful ranges of frequency. For optimum 60Hz line rejection, the capacitor value should be chosen such that 32768 (-16) or 8192 (-14) clock periods is close to an integral multiple of the 60Hz period.

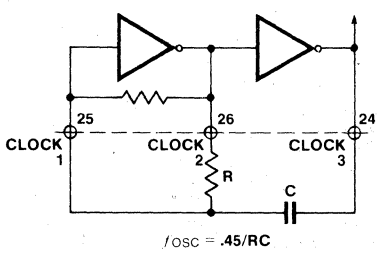


Figure 12: RC Oscillator

Note that CLOCK 3 has the same output drive as the bit outputs.

As a result of pin count limitations, the ICL7104-16 has only CLOCK 1 and CLOCK 2 available, and cannot be used as an RC oscillator. The internal clock will correspond to the inverse of the signal on CLOCK 2. Figure 13 shows a crystal oscillator circuit, which can be used with all 7104 versions. If an external clock is to be used, it should be applied to CLOCK 1. The internal clock will correspond to the signal applied to this pin.

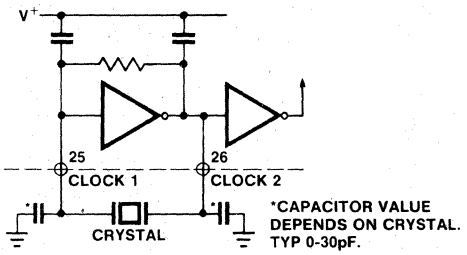


Figure 13: Crystal Oscillator

POWER SUPPLY SEQUENCING

Because of the nature of the CMOS process used to fabricate the 7104, and the multiple power supplies used, there are certain conditions of these supplies under which a disabling and potentially damaging SCR action can occur. All of these conditions involve the V+ supply (nom. +5V) being more positive than the V++ supply. If there is any possibility of this occuring during start-up, shut down, under transient conditions during operation, or when inserting a PC board into a "hot" socket, etc., a diode should be placed between V− and V++ to prevent it. A germanium or Schottky rectifier diode would be best, but in most cases a silicon rectifier diode is adequate.

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of 8068/7104 circuits, especially in 16-bit and high sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line. A recommended connection sequence for the ground lines is shown in Figure 14.

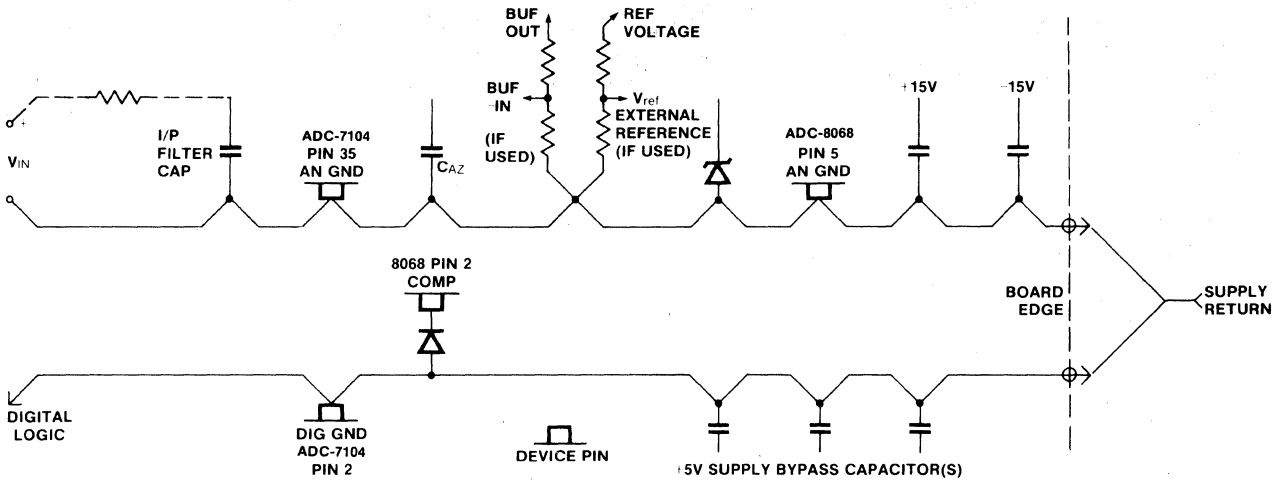
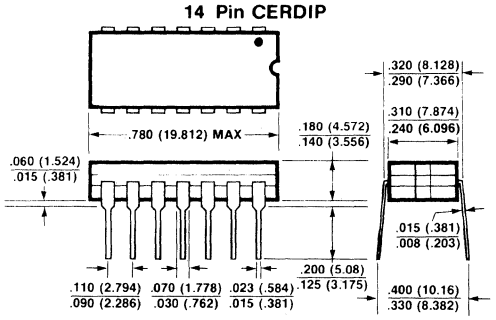


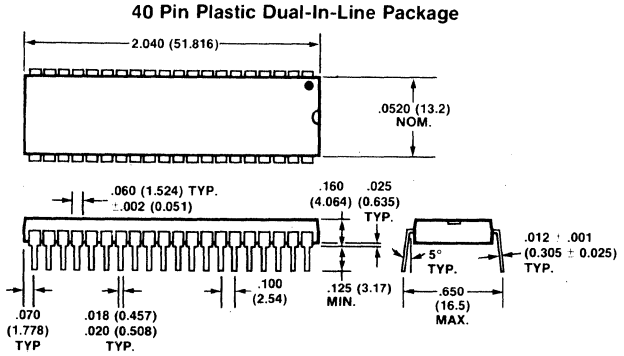
Figure 14: Grounding Sequence

PACKAGE DIMENSIONS

14 Pin CERDIP



40 Pin Plastic Dual-In-Line Package



DATEL INTERSIL
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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089,77-60-95 • DATEL KK Tokyo 793-1031

1/80

ADC-7109
12 Bit Binary A/D Converter for Microprocessor Interfaces

FEATURES

- **12 bit binary (plus polarity and overrange) dual slope integrating analog-to-digital converter.**
- **Byte-organized TTL-compatible three-state outputs and UART handshake mode for simple parallel or serial interfacing to microprocessor systems.**
- **RUN/$\overline{\text{HOLD}}$ input and STATUS output can be used to monitor and control conversion timing.**
- **True differential input and differential reference.**
- **Low noise-typically 15μV peak-to-peak.**
- **1pA typical input current.**
- **Operates at up to 30 conversions per second.**
- **On-chip oscillator operates with inexpensive 3.58MHz TV crystal giving 7.5 conversions per second for 60Hz rejection, or may be operated as an RC oscillator for other clock frequencies.**
- **Combines analog and digital functions on a single low power LSI CMOS chip.**
- **All inputs fully protected against static discharge; no special handling precautions necessary.**

GENERAL DESCRIPTION

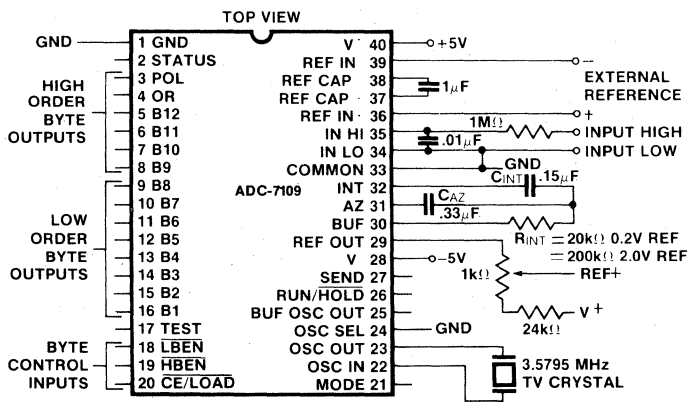
The ADC-7109 is a high performance, low power integrating A/D converter designed to easily interface to microprocessors.

The output data (12 bits, polarity and overrange) may be directly accessed under control of two byte enable inputs and a chip select input for a simple parallel bus interface. A UART handshake mode is provided which allows the ADC-7109 to work with industry-standard UARTs to provide serial data transmission, ideal for remote data logging applications. The RUN/HOLD input and STATUS output allow monitoring and control of conversion timing.

The ADC-7109 provides the user the high accuracy, low noise, low drift, versatility, and economy of the dual-slope integrating A/D converter. Features like true differential input and reference, zero drift of less than 1μV/° C max., input bias current of 10pA max., and typical power consumption of 20mW make the ADC-7109 an attractive per-channel alternative to analog multiplexing for many data acquisition applications.

PIN CONFIGURATION AND TEST CIRCUIT:

(See Figure 1 for typical connection to a UART or Microcomputer)

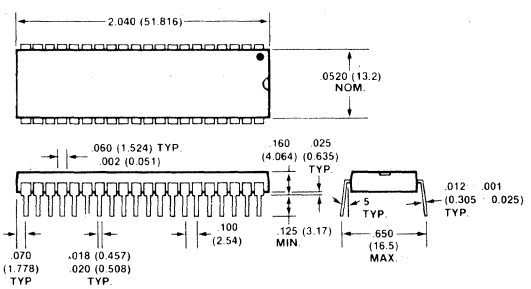


ORDERING INFORMATION

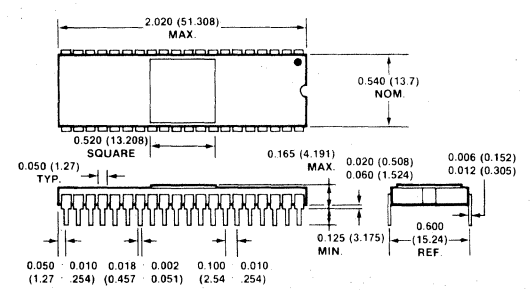
MODEL	OPER. TEMP. RANGE	PACKAGE
ADC-7109C	0 to +70° C	40 pin Epoxy DIP
ADC-7109R	−25 to +85° C	40 pin CerDIP
ADC-7109M	−55 to +125° C	40 pin Ceramic DIP

PACKAGE DIMENSIONS

40 Pin Plastic Dual-in-Line Package



40 Pin Ceramic Dual-in-Line Package



DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (GND to V^+)	+6.2V
Negative Supply Voltage (GND to V^-)	−9V
Analog Input Voltage (Lo or Hi) (Note 1)	V^+ to V^-
Reference Input Voltage (Lo or Hi) (Note 1)	V^+ to V^-
Digital Input Voltage (Pins 2-27) (Note 2)	$V^+ + 0.3V$ / GND − 0.3V
Power Dissipation (Note 3)	
Ceramic or Cerdip Package	1W @ 85° C
Plastic Package	500mW @ 70° C
Operating Temperature	
Ceramic or Cerdip Package	−25° C ≤ T_A ≤ 85° C
Plastic Package	0° C ≤ T_A ≤ 70° C
Storage Temperature	−55° C ≤ T_A ≤ 125° C
Lead Temperature (soldering, 60 sec)	300° C

Absolute maximum ratings define stress limitations which if exceeded may permanently damage the device. These ratings are not continuous duty ratings. For continuous operation these devices must be operated under the conditions defined under "Operating Characteristics."

TABLE I OPERATING CHARACTERISTICS

All parameters with $V^+ = +5V$, $V^- = -5V$, GND = 0V, $T_A = 25°C$, unless otherwise indicated.
Test circuit as shown on page 1.

ANALOG SECTION

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading		V_{IN} = 0.0V Full scale = 409.6mV	0000_8	$\pm 0000_8$	$+0000_8$	Octal Reading
Ratiometric Reading		$V_{IN} = V_{REF}$ V_{REF} = 204.8mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
Non-Linearity (Max deviation from best straight line fit)		Full scale = 409.6mV or 4.096V	−1	±.2	+1	Counts
Roll-over Error (difference in reading for equal pos. and neg. inputs near full scale.			−1	±.2	+1	Counts
Common Mode Rejection Ratio		V_{CM} ± 1V V_{IN} = 0V Full Scale = 409.6mV		50		μV/V
Noise (p-p value not exceeded 95% of time)		V_{IN} = 0V Full Scale = 409.6mV		15		μV
Leakage Current at Input		V_{IN} = 0V		1	10	pA
Zero Reading Drift		V_{IN} = 0V		0.2	1	μV/° C
Scale Factor Temperature Coefficient		V_{IN} = 408.9mV => 7770_8 reading Ext. Ref. 0 ppm/° C		1	5	ppm/° C
Supply Current V^+ to GND	I_{DL}	V_{IN} = 0, Crystal Osc. 3.58MHz test circuit Pins 2-21, 25, 26, 27, 29, open		700	1500	μA
Supply Current V^+ to V^-	I_{DA}			700	1500	μA
Ref Out Voltage		Referred to V^+, 25kΩ between V^+ and REF OUT	−2.4	−2.8	−3.2	V
Ref Out Temp. Coefficient		25kΩ between V^+ and REF OUT		80		ppm/° C

DIGITAL SECTION

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage		V_{OH}	I_{OUT} = 100μA Pins 2-16, 18, 19, 20	3.5	4.3		V
Output Low Voltage		V_{OL}	I_{OUT} = 1.6mA		0.2	0.4	V
Output Leakage Current			Pins 3-16 high impedance		±.01	±1	μA
Control I/O Pullup Current			Pins 18, 19, 20 V_{OUT} = V+ −3V MODE input at GND		5		μA
Control I/O Loading			$\overline{HBEN}$ Pin 19 $\overline{LBEN}$ Pin 18			50	pF
Input High Voltage		V_{IH}	Pins 18-21, 26, 27 referred to GND	2.5			V
Input Low Voltage		V_{IL}	Pins 18-21, 26, 27 referred to GND			1	V
Input Pull-up Current			Pins 26, 27 V_{OUT} = V+ −3V		5		μA
Input Pull-up Current			Pins 17, 24 V_{OUT} = V+ −3V		25		μA
Input Pull-down Current			Pin 21 V_{OUT} GND +3V		5		μA
Oscillator Output Current	High	O_{OH}	V_{OUT} = 2.5V		1		mA
	Low	O_{OL}	V_{OUT} = 2.5V		1.5		mA
Buffered Oscillator Output Current	High	BO_{OH}	V_{OUT} = 2.5V		2		mA
	Low	BO_{OL}	V_{OUT} = 2.5V		5		mA
MODE Input Pulse Width				50			ns

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

Note 2: Due to the SCR structure inherent in the process used to fabricate these devices, connecting any digital inputs or outputs to voltages greater than V+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources not on the same power supply be applied to the ADC-7109 before its power supply is established, and that in multiple supply systems the supply to the ADC-7109 be activated first.

Note 3: This limit refers to that of the package and will not be obtained during normal operation.

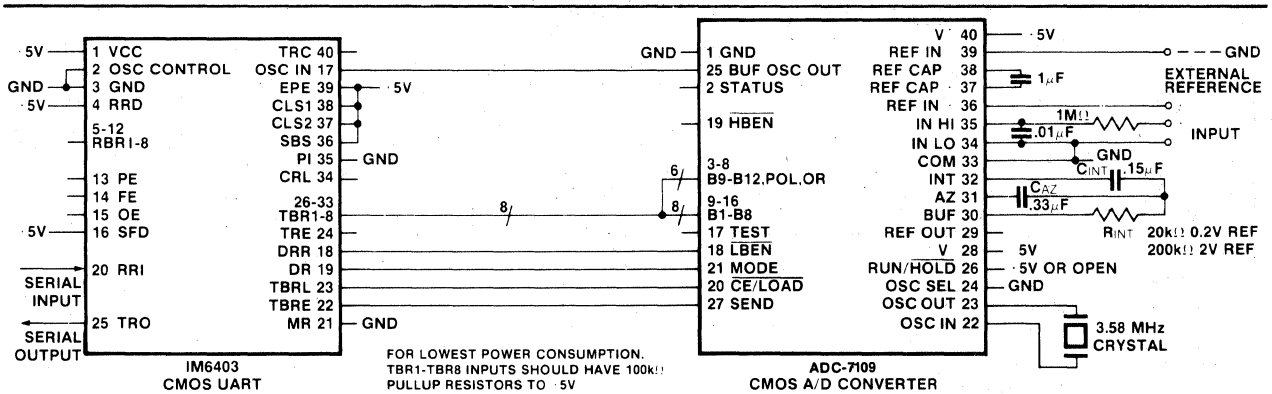


Figure 1A. To transmit latest result, send any word to UART.

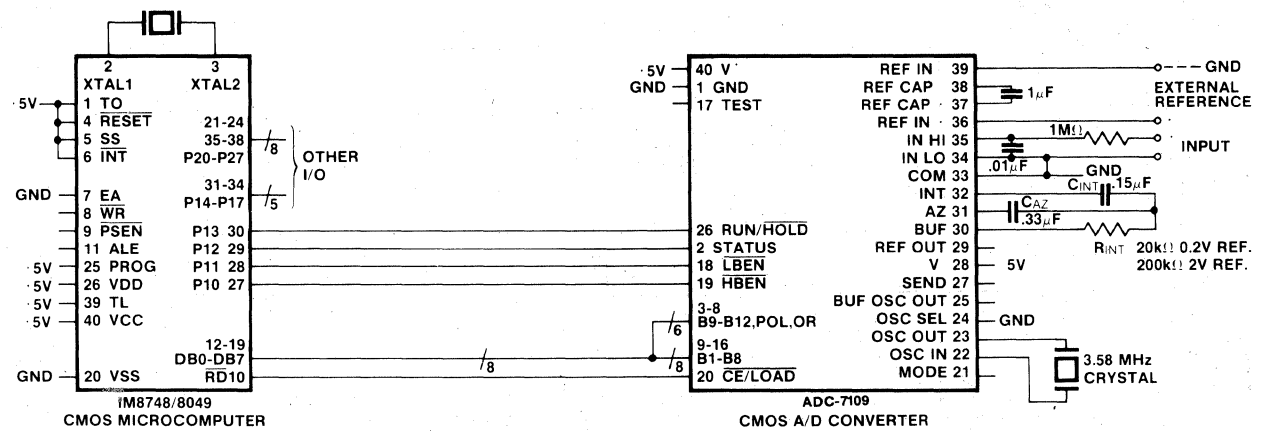


Figure 1B. Typical Connection Diagram Parallel Interface With 8748/8048 Microcomputer

TABLE 2 - Pin Assignment and Function Description

PIN	SYMBOL	DESCRIPTION
1	GND	Digital Ground. 0V. Ground return for all digital logic
2	STATUS	Output - High during integrate and deintegrate until data is latched. - Low when analog section is in Auto-Zero configuration.
3	POL	Polarity. Three-State Output
4	OR	Over-range. Three-State Output
5	B12	Bit 12 (Most Significant Bit)
6	B11	Bit 11
7	B10	Bit 10
8	B9	Bit 9
9	B8	Bit 8
10	B7	Bit 7
11	B6	Bit 6
12	B5	Bit 5
13	B4	Bit 4
14	B3	Bit 3
15	B2	Bit 2
16	B1	Bit 1 (Least Significant Bit)
17	TEST	Input High - Normal Operation. Input Low - Forces all bit outputs high. Note: This input is used for test purposes only.
18	$\overline{\text{LBEN}}$	Low Byte Enable - With Mode (Pin 21) low, and $\overline{\text{CE LOAD}}$ (Pin 20) low, taking this pin low activates low order byte outputs B1-B8. - With Mode (Pin 21) high, this pin serves as a low byte flag output used in handshake mode. See Figures 7, 8, 9.
19	$\overline{\text{HBEN}}$	High Byte Enable - With Mode (Pin 21) low, and $\overline{\text{CE LOAD}}$ (Pin 20) low, taking this pin low activates high order byte outputs B9-B12, POL, OR. - With Mode (Pin 21) high, this pin serves as a high byte flag output used in handshake mode. See Figures 7, 8, 9.
20	$\overline{\text{CE LOAD}}$	Chip Enable Load - With Mode (Pin 21) low, $\overline{\text{CE LOAD}}$ serves as a master output enable. When high, B1-B12, POL, OR outputs are disabled. - With Mode (Pin 21) high, this pin serves as a load strobe used in handshake mode. See Figures 7, 8, 9.

PIN	SYMBOL	DESCRIPTION
21	MODE	Input Low - Direct output mode where $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19) and $\overline{\text{LBEN}}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed High - Causes immediate entry into handshake mode and output of data as in Figure 9. Input High - Enables $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19), and $\overline{\text{LBEN}}$ (Pin 18) as outputs, handshake mode will be entered and data output as in Figures 7 and 8 at conversion completion.
22	OSC IN	Oscillator Input
23	OSC OUT	Oscillator Output
24	OSC SEL	Oscillator Select - Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator - clock will be same phase and duty cycle as BUF OSC OUT. - Input low configures OSC IN, OSC OUT for crystal oscillator - clock frequency will be 1.58 of frequency at BUF OSC OUT.
25	BUF OSC OUT	Buffered Oscillator Output
26	RUN $\overline{\text{HOLD}}$	Input High - Conversions continuously performed every 8192 clock pulses. Input Low - Conversion in progress completed, converter will stop in Auto-Zero 7 counts before integrate.
27	SEND	Input - Used in handshake mode to indicate ability of an external device to accept data.
28	V⁻	Analog Negative Supply - Nominally -5V with respect to GND (Pin 1).
29	REF OUT	Reference Voltage Output - Nominally 2.8V down from V⁺ (Pin 40).
30	BUFFER	Buffer Amplifier Output
31	AUTO-ZERO	Auto-Zero Node - Inside foil of C_{AZ}
32	INTEGRATOR	Integrator Output - Outside foil of C_{INT}
33	COMMON	Analog Common - System is Auto-Zeroed to COMMON
34	INPUT LO	Differential Input Low Side
35	INPUT HI	Differential Input High Side
36	REF IN⁺	Differential Reference Input Positive
37	REF CAP⁺	Reference Capacitor Positive
38	REF CAP⁻	Reference Capacitor Negative
39	REF IN⁻	Differential Reference Input Negative
40	V⁺	Positive Supply Voltage - Nominally +5V with respect to GND (Pin 1).

DETAILED DESCRIPTION

Analog Section

Figure 2 shows the equivalent circuit of the Analog Section of the ADC-7109. When the RUN/$\overline{\text{HOLD}}$ input is left open or connected to V⁺, the circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle). Each measurement cycle is divided into three phases as shown in Figure 3. They are (1) Auto-Zero (AZ), (2) Signal Integrate (INT) and (3) Deintegrate (DE).

1. **Auto-Zero Phase**

During auto-zero three things happen. First, input high and low are disconnected from their pins and internally shorted to analog common. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the AZ accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. **Signal Integrate Phase**

During signal integrate the auto-zero loop is opened, the internal short is removed and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between input high and input low for a fixed time of 2048 clock periods. At the end of this phase, the polarity of the integrated signal is determined.

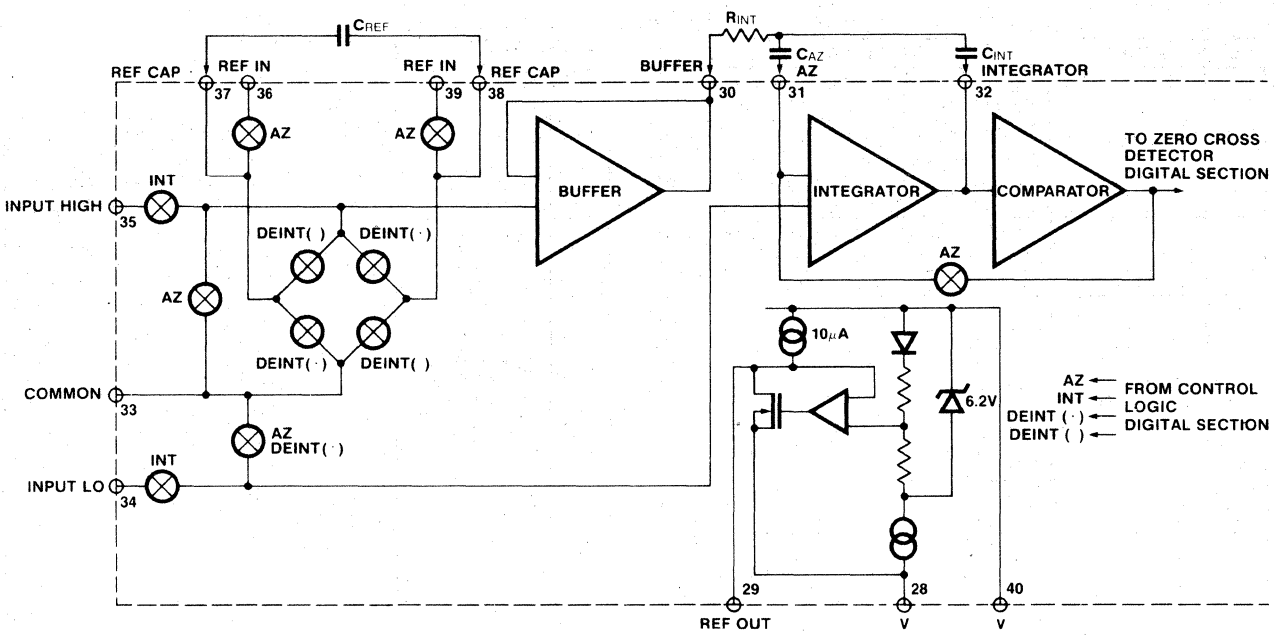


Figure 2: Analog Section

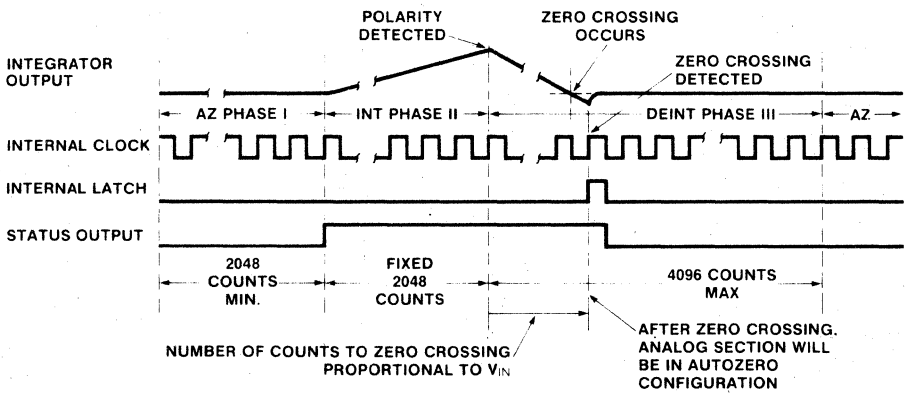


Figure 3: Conversion Timing

3. **Deintegrate Phase**

   The final phase is deintegrate, or reference integrate. Input low is internally connected to analog common and input high is connected across the previously charged (during auto-zero) reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to the zero crossing (established in Auto Zero) with a fixed slope. Thus the time for the output to returr. to zero (represented by the number of clock periods counted) is proportional to the input signal.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full scale with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

The ADC-7109 has, however, been optimized for operation with analog common near digital ground. With power supplies of +5V and -5V, this allows a 4V full scale integrator swing positive or negative maximizing the performance of the analog section.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to deintegrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (-) input voltage will give a roll-over error. However, by

selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Values Selection below).

The roll-over error from these sources is minimized by having the reference common mode voltage near or at analog common.

Component Value Selection

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

The most important consideration is that the integrator output swing (for full-scale input) be as large as possible. For example, with ±5V supplies and COMMON connected to GND, the nominal integrator output swing at full scale is ±4V. Since the integrator output can go to 0.3V from either supply without significantly affecting linearity, a 4V integrator output swing allows 0.7V for variations in output swing due to component value and oscillator tolerances. With ±5V supplies and a common mode range of ±1V required, the component values should be selected to provide ±3V integrator output swing. Noise and rollover errors will be slightly worse than in the ±4V case. For larger common mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and rollover errors. To improve the performance, supplies of ±6V may be used.

1. **Integrating Resistor**

   Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 4.096 volt full scale, 200kΩ is near optimum and similarly a 20kΩ for a 409.6mV scale. For other values of full scale voltage, R_{INT} should be chosen by the relation $R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$

2. **Integrating Capacitor**

   The integrating capacitor C_{INT} should be selected to give the maximum integrator output voltage swing without saturating the integrator (approximately 0.3 volt from either supply). For the ADC-7109 with ±5 volt supplies and analog common connected to GND, a ±3.5 to ±4 volt integrator output swing is nominal. For 7-1/2 conversions per second (61.72KHz clock frequency) as provided by the crystal oscillator, nominal values for C_{INT} and C_{AZ} are 0.15μF and 0.33μF, respectively. If different clock frequencies are used, these values should be changed to maintain the integrator output voltage swing. In general, the value of C_{INT} is given by

   $$C_{INT} = \frac{(2048 \times \text{clock period})\ (20\mu A)}{\text{integrator output voltage swing}}$$

   An additional requirement of the integrating capacitor is that it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

3. **Auto-Zero Capacitor**

   The size of the auto-zero capacitor has some influence on the noise of the system; a big capacitor, giving less noise. However, it cannot be increased without limits since it, in parallel with the integrating capacitor forms an R-C time constant that determines the speed of recovery from overloads and more important the error that exists at the end of an auto-zero cycle. For 409.6mv full scale where noise is very important and the integrating resistor small, a value of C_{AZ} twice C_{INT} is optimum. Similarly for 4.096V full scale where recovery is more important than noise, a value of C_{AZ} equal to half of C_{INT} is recommended.

   For optimal rejection of stray pickup, the outer foil of C_{AZ} should be connected to the R-C summing junction and the inner foil to pin 31. Similarly the outer foil of C_{INT} should be connected to pin 32 and the inner foil to the R-C summing junction.

4. **Reference Capacitor**

   A 1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the reference low is not at analog common) and a 409.6mV scale is used, a larger value is required to prevent roll-over error. Generally 10μF will hold the roll-over error to 0.5 count in this instance.

5. **Reference Voltage**

   The analog input required to generate a full scale output of 4096 counts is $V_{IN} = 2V_{REF}$. Thus for a normalized scale, a reference of 2.048V should be usd for a 4.096V full scale, and 204.8mV should be used for a 0.4096V full scale. However, in many applications where the A/D is sensing the output of a transducer, there will exist a scale factor other than unity between the absolute output voltage to be measured and a desired digital output. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 409.6mV, the input voltage should be measured directly and a reference voltage of 0.341V should be used. Suitable values for integrating resistor and capacitor are 34k and 0.15μF. This avoids a divider on the input. Another advantage of this system occurs when a zero reading is desired for non-zero input. Temperature and weight measurements with an offset or tare are examples. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing poiarities carefully. However, in processor-based systems using the ADC-7109, it may be more efficient to perform this type of scaling or tare subtraction digitally using software.

6. **Reference Sources**

   The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ADC-7109 at 12 bits is one part in 4096, or 244ppm. Thus if the reference has a temperature coefficient of 80ppm/°C (onboard reference) a temperature difference of 3°C will introduce a one-bit absolute error. For this reason, it is recommended that an external high-quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

The ADC-7109 provides a Reference Output (pin 29) which may be used with a resistive divider to generate a suitable reference voltage. This output will sink up to about 20mA without significant variation in output voltage, and is provided with a pullup bias device which sources about 10μA. The output voltage is nominally 2.8V below V⁺, and has a temperature coefficient of ±80ppm/°C typ. When using the onboard reference, Ref Out (Pin 29) should be connected to Ref – (pin 39), and Ref+ should be connected to the wiper of a precision potentiometer between Ref Out and V⁺. The circuit for a 204.8mV reference is shown in the test circuit. For a 2.048V reference, the fixed resistor should be removed, and a 25kΩ precision potentiometer between Ref Out and V⁺ should be used.

DETAILED DESCRIPTION

Digital Section

The digital section includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic, and UART handshake logic, as shown in the Block Diagram Figure 4.

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined in Table 1 "Operating Characteristics". For minimum power consumption, all inputs should swing from GND (low) to V⁺ (high). Inputs driven from TTL gates should have 3-5kΩ pullup resistors added for maximum noise immunity.

MODE Input

The MODE input is used to control the output mode of the converter. When the MODE pin is connected to GND or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

STATUS Output

During a conversion cycle, the STATUS output goes high at the beginning of Signal Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 3 for details of this timing. This signal may be used as a "data valid" flag (data never changes while STATUS is low) to drive interrupts, or for monitoring the status of the converter.

RUN/$\overline{\text{HOLD}}$ Input

When the RUN/$\overline{\text{HOLD}}$ input is connected to V⁺ or left open (this input has a pullup resistor to ensure a high level when the pin is left open), the circuit will continuously perform conversion cycles, updating the output latches at the end of every Deintegrate (Phase III) portion of the conversion cycle (See Figure 3). In this mode of operation, the conversion cycle will be performed in 8192 clock periods, regardless of the resulting value.

If the RUN/$\overline{\text{HOLD}}$ input goes low (and stays there) during Integrate (Phase II) or Deintegrate (Phase III) before the zero crossing is detected, the converter will complete the conversion in progress, update the output latches, and then terminate Phase III, jumping to Auto-Zero (Phase I). If RUN/$\overline{\text{HOLD}}$ stays low, the converter will ensure a minimum Auto-Zero time, and wait in Auto-Zero until the RUN/$\overline{\text{HOLD}}$ input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STATUS output will go high) seven clock periods after the high level is detected at RUN/$\overline{\text{HOLD}}$. See Figure 5 for details.

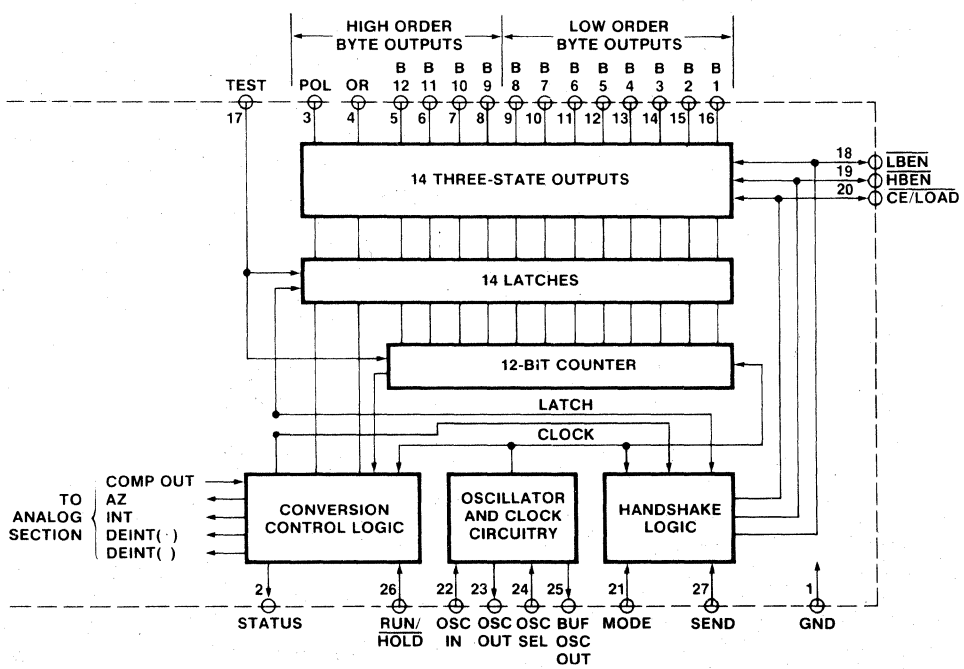


Figure 4: Digital Section

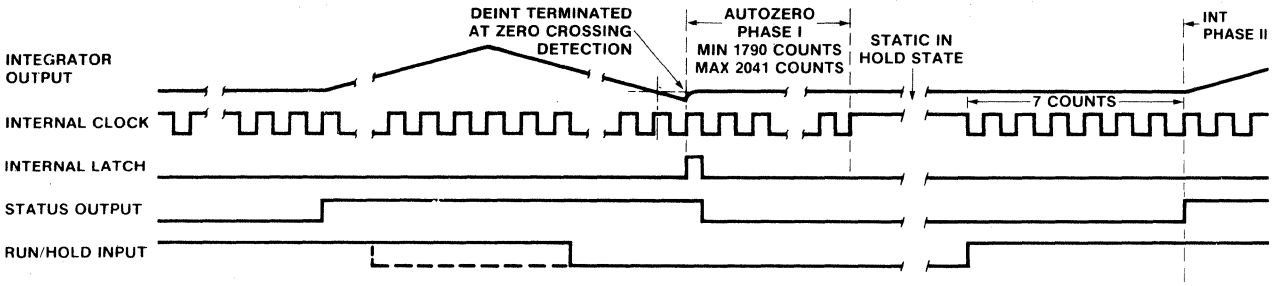


Figure 5: Run/$\overline{\text{Hold}}$ Operation

Using the RUN/$\overline{\text{HOLD}}$ input in this manner allows an easy "convert on demand" interface to be used. The converter may be held at idle in auto-zero with RUN/$\overline{\text{HOLD}}$ low. When RUN/$\overline{\text{HOLD}}$ goes high the conversion is started, and when the STATUS output goes low the new data is valid (or transferred to the UART - see Handshake Mode). RUN/$\overline{\text{HOLD}}$ may now go low terminating Deintegrate and ensuring a minimum Auto-Zero time before stopping to wait for the next conversion.

If RUN/$\overline{\text{HOLD}}$ goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to "short-cycle" the converter by eliminating the time spent in Deintegrate after the zero crossing. The required activity on the RUN/$\overline{\text{HOLD}}$ input can be provided by connecting it to the Buffered Oscillator Output. In this mode the conversion time is dependent on the input value measured. Also refer to Intersil Application Bulletin A030 for a discussion of the effects this will have on Auto-Zero performance.

If the RUN/$\overline{\text{HOLD}}$ input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for RUN/$\overline{\text{HOLD}}$ to go high. As above, Integrate (Phase II) begins seven clock periods after the high level is detected.

Direct Mode

When the MODE pin is left at a low level, the data outputs (bits 1 through 8 low order byte, bits 9 through 12, polarity and over-range high order byte) are accessible under control of the byte and chip enable terminals as inputs. These three inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip enable input is low, taking a byte enable input low will allow the outputs of that byte to become active (three-stated on). This allows a variety of parallel data accessing techniques to be used, as shown in the section entitled "Interfacing." The timing requirements for these outputs are shown in Figure 6 and Table 3.

Table 3 - Direct Mode Timing Requirements

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{BEA}	Byte Enable Width	200	500		ns
t_{DAB}	Data Access Time from Byte Enable		150	300	ns
t_{DHB}	Data Hold Time from Byte Enable		150	300	ns
t_{CEA}	Chip Enable Width	300	500		ns
t_{DAC}	Data Access Time from Chip Enable		200	400	ns
t_{DHC}	Data Hold Time from Chip Enable		200	400	ns

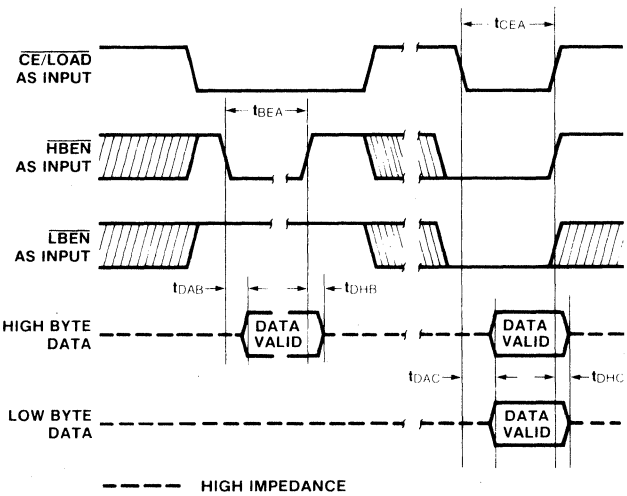


Figure 6: Direct Mode Output Timing

It should be noted that these control inputs are asynchronous with respect to the converter clock - the data may be accessed at any time. Thus it is possible to access the data while it is begin updated, which could lead to scrambled data. Synchronizing the access of data with the conversion cycle by monitoring the STATUS output will prevent this. Data is never updated while STATUS is low.

Handshake Mode

The handshake output mode is provided as an alternative means of interfacing the ADC-7109 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte enable inputs. This mode is specifically designed to allow a direct interface between the ADC-7109 and industry-standard UARTs (such as the Intersil CMOS UARTs, IM6402/3) with no external logic required. When triggered into the handshake mode, the ADC-7109 provides all the control and flag signals necessary to sequence the two bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission to minimize the number of lines to the central controlling processor.

Entry into the handshake mode is controlled by the MODE pin. When the MODE terminal is held high, the ADC-7109 will enter the handshake mode after new data has been stored in the output latches at the end of every conversion performed (See Figures 7 and 8). The MODE terminal may also be used to trigger entry into the handshake mode on demand. At any time during the conversion cycle, the low to high transition of a short pulse at the MODE input will cause immediate entry

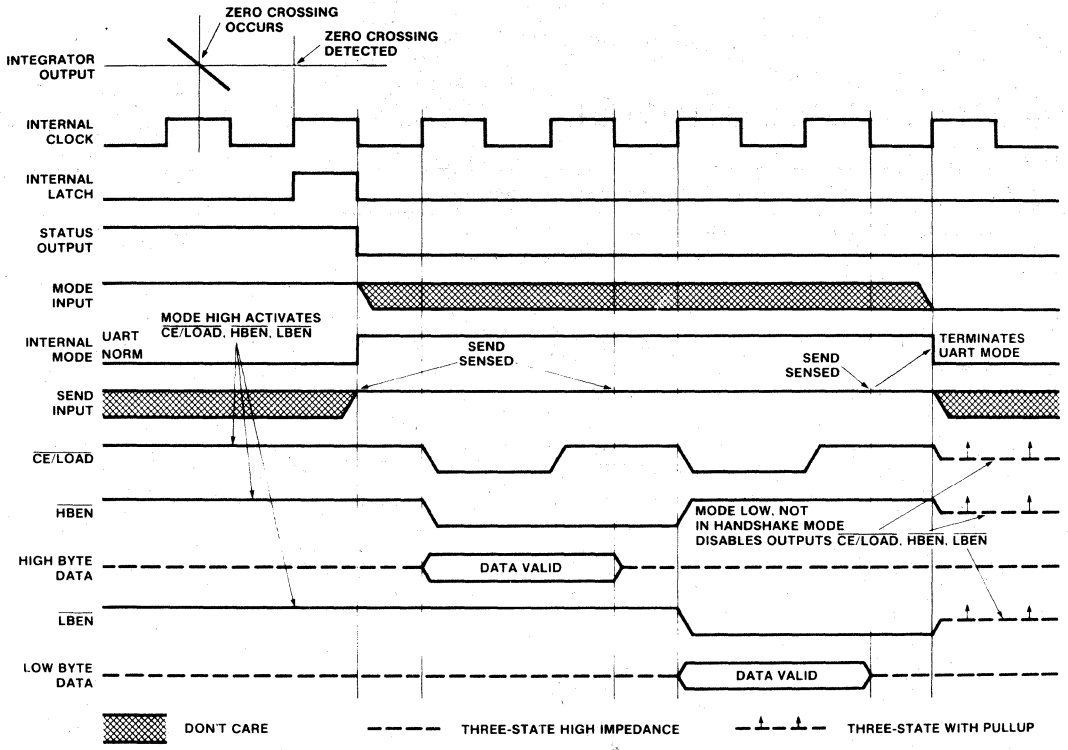


Figure 7: Handshake With Send Held Positive

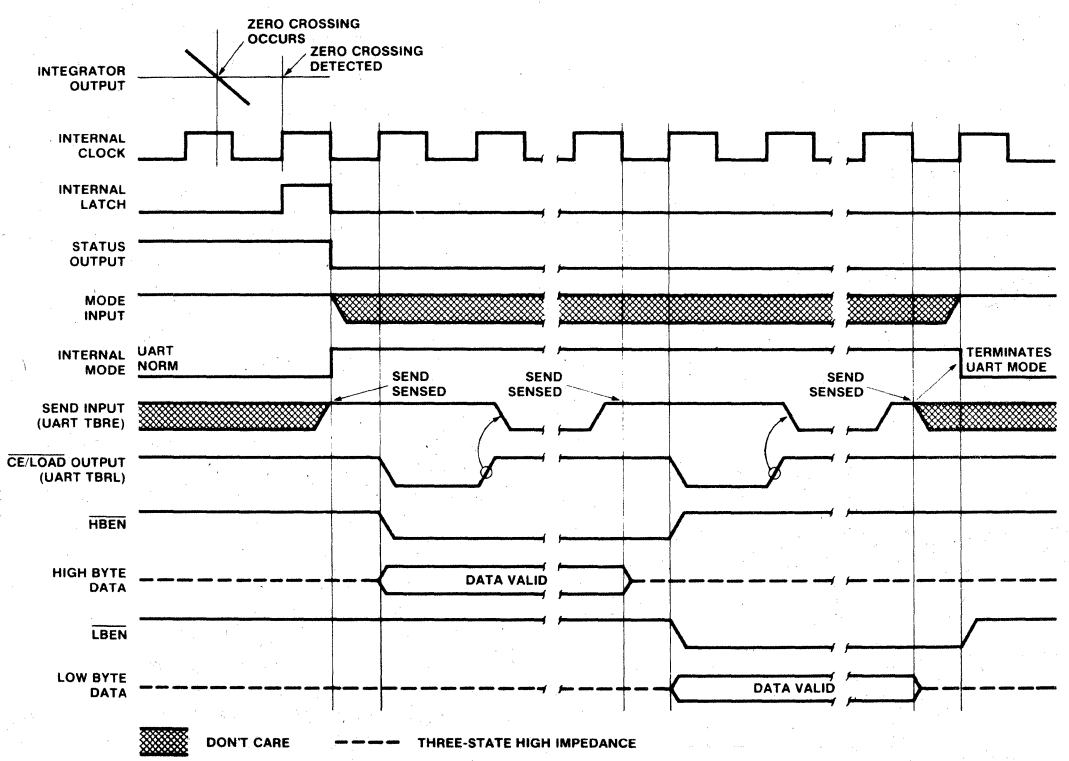


Figure 8: Handshake - Typical UART Interface Timing

into the handshake mode. If this pulse occurs while new data is being stored, the entry into handshake mode is delayed until the data is stable. While the converter is in the handshake mode, the MODE input is ignored, and although conversions will still be performed, data updating will be inhibited (See Figure 9) until the converter completes the output cycle and clears the handshake mode.

When the converter enters the handshake mode, or when the MODE input is high, the chip and byte enable terminals become TTL-compatible outputs which provide the control signals for the output cycle (See Figures 7, 8, and 9).

In handshake mode, the SEND input is used by the converter as an indication of the ability of the receiving device (such as a UART) to accept data.

Figure 7 shows the sequence of the output cycle with SEND held high. The handshake mode (Internal MODE high) is entered after the data latch pulse (since MODE remains high the $\overline{\text{CE/LOAD}}$, $\overline{\text{LBEN}}$ and $\overline{\text{HBEN}}$ terminals are active as outputs). The high level at the SEND input is sensed on the same high to low internal clock edge. On the next low to high internal clock edge, the $\overline{\text{CE/LOAD}}$ and the $\overline{\text{HBEN}}$ outputs assume a low level, and the high-order byte (bits 9 through 12, POL, and OR) outputs are enabled. The $\overline{\text{CE/LOAD}}$ output remains low for one full internal clock period only, the data outputs remain active for 1-1/2 internal clock periods, and the high byte enable remains low for two clock periods. Thus the $\overline{\text{CE/LOAD}}$ output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte enable as an output may be used as a byte identification flag. With SEND remaining high the converter completes the output cycle using $\overline{\text{CE/LOAD}}$ and $\overline{\text{LBEN}}$ while the low order byte outputs (bits 1 through 8) are activated. The handshake mode is terminated when both bytes are sent.

Figure 8 shows an output sequence where the SEND input is used to delay portions of the sequence, or handshake, to ensure correct data transfer. This timing diagram shows the relationships that occur using an industry-standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEND input to the ADC-7109 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{\text{CE/LOAD}}$ terminal of the ADC-7109 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

Assuming the UART Transmitter Buffer Register is empty, the SEND input will be high when the handshake mode is entered after new data is stored. The $\overline{\text{CE/LOAD}}$ and $\overline{\text{HBEN}}$ terminals will go low after SEND is sensed, and the high order byte outputs become active. When $\overline{\text{CE/LOAD}}$ goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the $\overline{\text{HBEN}}$ output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next ADC-7109

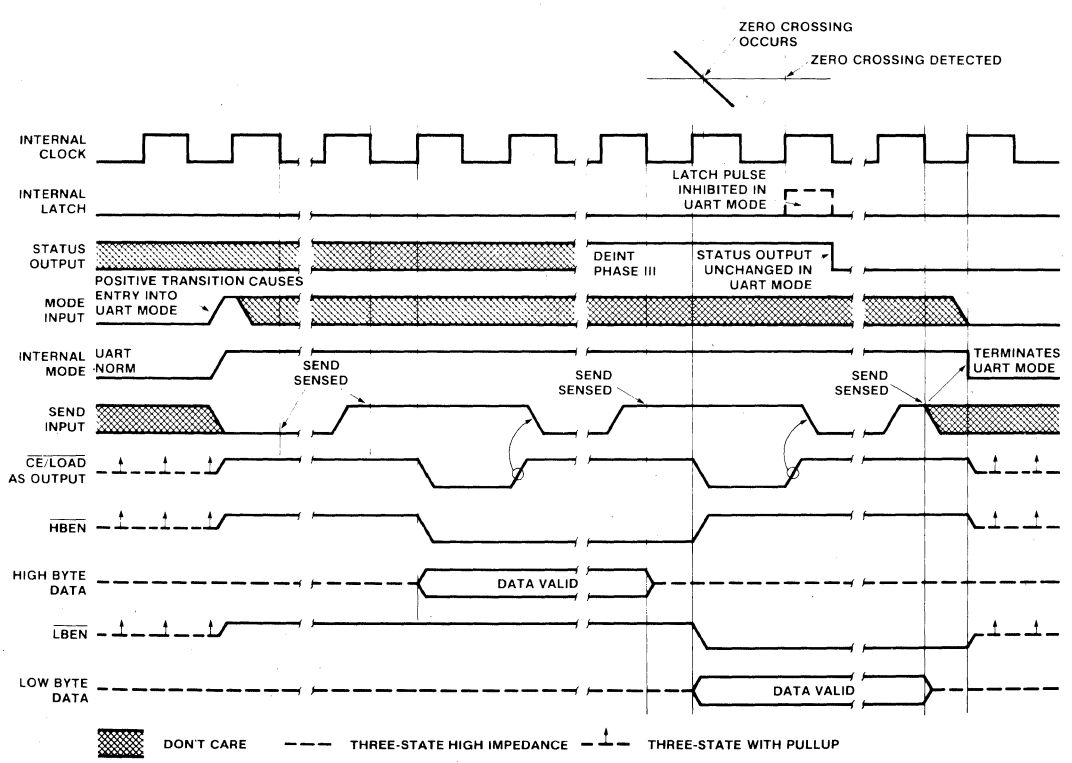


Figure 9: Handshake Triggered By Mode

internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the $\overline{HBEN}$ output returns high. At the same time, the $\overline{CE/LOAD}$ and $\overline{LBEN}$ outputs go low, and the low order byte outputs become active. Similarly, when the $\overline{CE/LOAD}$ returns high at the end of one clock period, the low order data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ADC-7109 internal clock high to low edge, disabling the data outputs. One-half internal clock later, the handshake mode will be cleared, and the $\overline{CE/LOAD}$, $\overline{HBEN}$, and $\overline{LBEN}$ terminals return high and stay active (as long as MODE stays high).

With the MODE input remaining high as in these examples, the converter will output the results of every conversion except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 9 shows a handshake output sequence triggered by such an edge. In addition, the SEND input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEND input, and the sequence for the first (high order) byte is similar to the sequence for the second byte. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STATUS output and RUN/$\overline{HOLD}$ input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

Oscillator

The ADC-7109 is provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated as an RC or crystal oscillator. The OSCILLATOR SELECT input changes the internal configuration of the oscillator to optimize it for RC or crystal operation.

When the OSCILLATOR SELECT input is high or left open (the input is provided with a pullup resistor), the oscillator is configured for RC operation, and the internal clock will be of the same frequency and phase as the signal at the BUFFERED OSCILLATOR OUTPUT. The resistor and capacitor should be connected as in Figure 10. The circuit will oscillate at a frequency given by f = .45/RC. A 100kΩ resistor is recommended for useful ranges of frequency. For optimum 60Hz line rejection, the capacitor value should be chosen such that 2048 clock periods is close to an integral multiple of the 60Hz period.

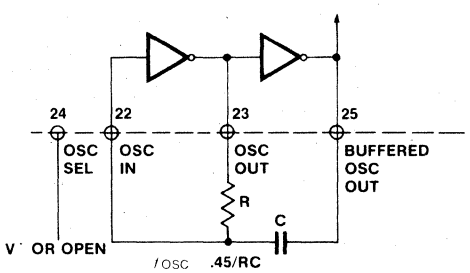


Figure 10: RC Oscillator

When the OSCILLATOR SELECT input is low a feedback device and output and input capacitors are added to the oscillator. In this configuration, as shown in Figure 11, the

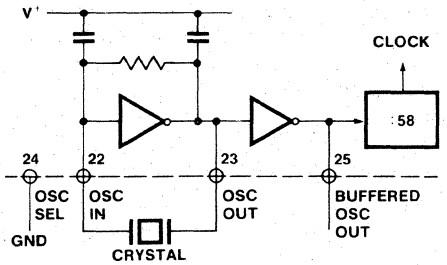


Figure 11: Crystal Oscillator

oscillator will operate with most crystals in the 1 to 5MHz range with no external components. Taking the OSCILLATOR SELECT input low also inserts a fixed ÷58 divider circuit between the BUFFERED OSCILLATOR OUTPUT and the internal clock. Using an inexpensive 3.58MHz TV crystal, this division ratio provides an integration time given by:

$$T = (2048 \text{ clock periods}) \times \left(\frac{58}{3.58\text{MHz}}\right) = 33.18\text{ms}$$

This time is very close to two 60Hz periods or 33.33ms. The error is less than one percent, which will give better than 40dB 60Hz rejection. The converter will operate reliably at conversion rates of up to 30 per second, which corresponds to a clock frequency of 245.8kHz.

If at any time the oscillator is to be overdriven, the overdriving signal should be applied at the OSCILLATOR INPUT, and the OSCILLATOR OUTPUT should be left open. The internal clock will be of the same frequency, duty cycle, and phase as the input signal when OSCILLATOR SELECT is left open. When OSCILLATOR SELECT is at GND, the clock will be a factor of 58 below the input frequency.

When using the ADC-7109 with the IM6403 UART, it is possible to use one 3.58MHz crystal for both devices. The BUFFERED OSCILLATOR OUTPUT of the ADC-7109 may be used to drive the OSCILLATOR INPUT of the UART, saving the need for a second crystal. However, the BUFFERED OSCILLATOR OUTPUT does not have a great deal of drive, and when driving more than one slave device, external buffering should be used.

Test Input

When the TEST input is taken to a level halfway between V⁺ and GND, the counter output latches are enabled, allowing the counter contents to be examed anytime.

When the TEST input is connected to GND, the counter outputs are all forced into the high state, and the internal clock is disabled. When the input returns to the 1/2 (V⁺ - GND) voltage or to V⁺ and one clock is input, the counter outputs will all be clocked to the negative state. This allows easy testing of the counter and its outputs.

INTERFACING

Direct Mode

Figure 12 shows some of the combinations of chip enable and byte enable control signals which may be used when interfacing the ADC-7109 to parallel data lines. The $\overline{CE/LOAD}$ input may be tied low, allowing either byte to be controlled by its own enable as in Figure 12A. Figure 12B shows a configuration where the two byte enables are connected together. In this configuration, the $\overline{CE/LOAD}$ serves as a chip enable, and the $\overline{HBEN}$ and $\overline{LBEN}$ may be connected to GND or serve as a second chip enable. The 14 data outputs will all be enabled simultaneously. Figure 12C shows the $\overline{HBEN}$ and $\overline{LBEN}$ as flag inputs, and $\overline{CE/LOAD}$ as a master enable, which could be the READ strobe available from most microprocessors.

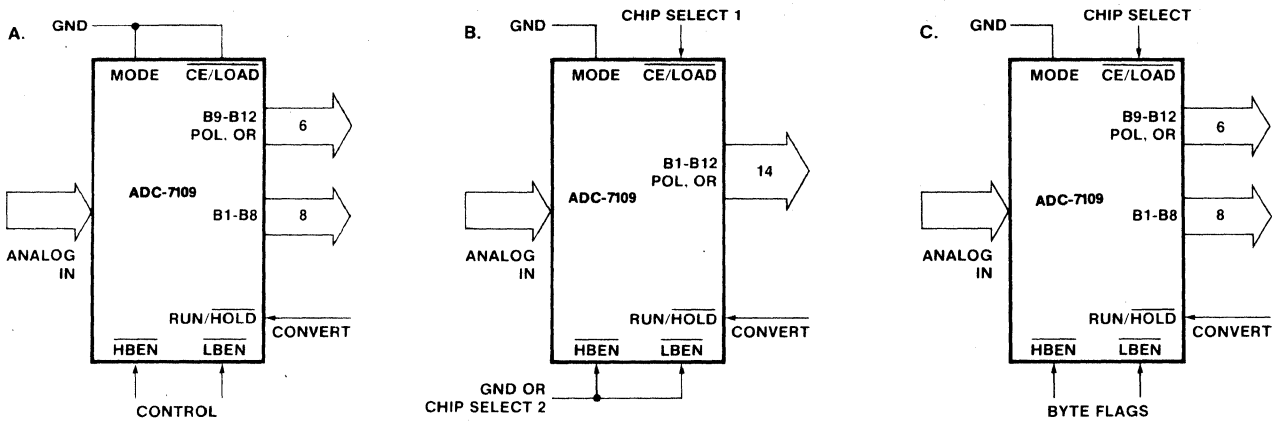


Figure 12: Direct Mode Chip and Byte Enable Combinations

Figure 13 shows an approach to interfacing several ADC-7109s to a bus, ganging the $\overline{HBEN}$ and $\overline{LBEN}$ signals to several converters together, and using the $\overline{CE/LOAD}$ inputs (perhaps decoded from an address) to select the desired converter.

Some practical circuits utilizing the parallel three-state output capabilities of the ADC-7109 are shown in Figures 14 through 19. Figure 14 shows a straightforward application to the Intel MCS-48, -80 and -85 systems via an 8255PPI, where the ADC-7109 data outputs are active at all times. The I/O ports of an 8155 may be used in the same way. This interface can be used in a read-anytime mode, although a read performed while the data latches are being updated will lead to scrambled data. This will occur very rarely, in the proportion of setup-skew times to conversion time. One way to overcome this is to read the STATUS output as well, and if it is high, read the data again after a delay of more than 1/2 converter clock period. If STATUS is now low, the second reading is correct, and if it is still high, the first reading is correct. Alternatively, this timing problem is completely avoided by using a read-after-update sequence, as shown in Figure 15. Here the high to low transition of the STATUS output drives an interrupt to the microprocessor causing it to access the data. This application also shows the RUN/$\overline{HOLD}$ input being used to initiate conversions under software control.

A similar interface to Motorola MC6800 or MOS Technology MCS650X systems is shown in Figure 16. The high to low transition of the STATUS output generates an interrupt via the Control Register B CB1 line. Note that CB2 controls the RUN/$\overline{HOLD}$ pin through Control Register B, allowing software-controlled initiation of conversions in this system also.

Figure 17 shows an interface to the Intersil IM6100 CMOS microprocessor family using the IM6101 PIE to control the data transfers. Here the data is read by the microprocessor in an 8-bit and a 6-bit word, directly from the ADC-7109 to the microprocessor data bus. Again, the high to low transition of the STATUS output generates an interrupt leading to a software routine controlling the two read operations. As before, the RUN/$\overline{HOLD}$ input to the ADC-7109 is shown as being under software control.

The three-state output capability of the ADC-7109 allows direct interfacing to most microprocessor busses. Examples of this are shown in the Typical Connection Diagram on

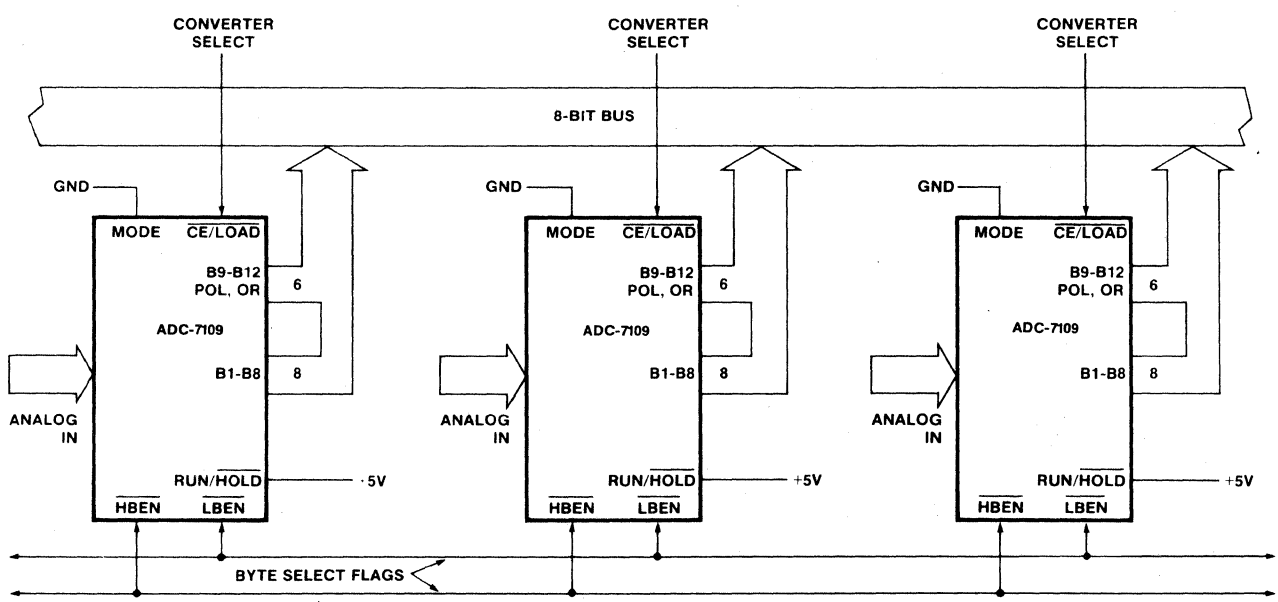


Figure 13: Three-stating Several 7109's to a Small Bus

Page 3 and in Figures 18 and 19. It is necessary to carefully consider the system timing in this type of interface, to be sure that requirements for setup and hold times, and minimum pulse widths are met. Note also the drive limitations on long busses. Generally this type of interface is only favored if the memory peripheral address density is low so that simple address decoding can be used. Interrupt handling can also require many additional components, and using an interface device will usually simplify the system in this case.

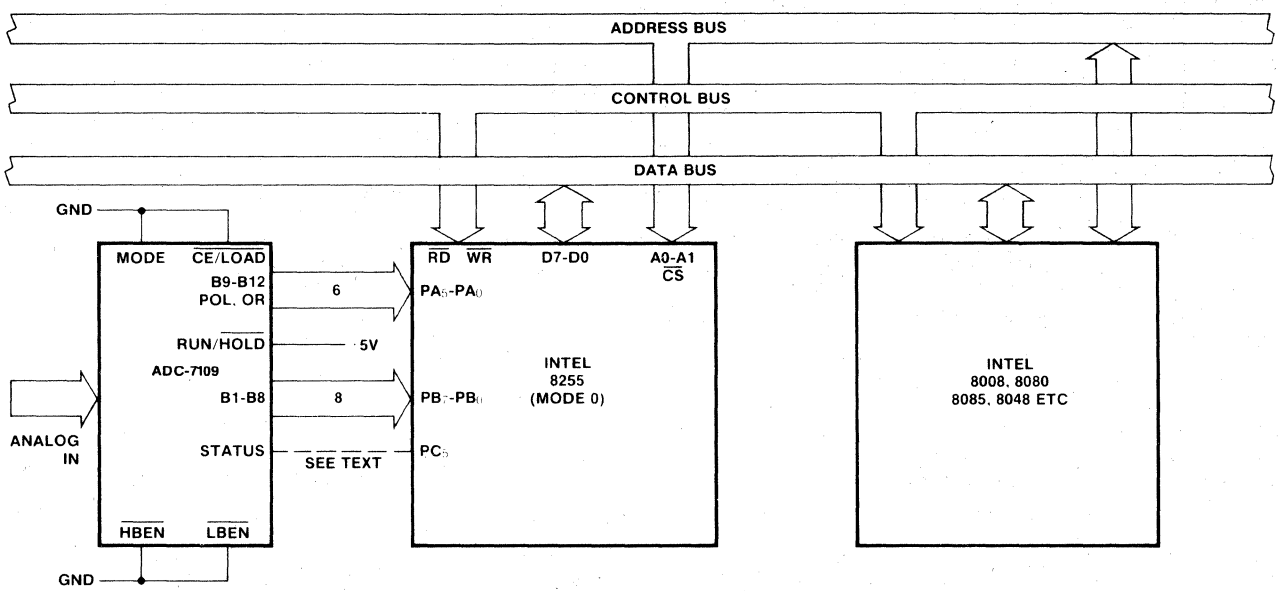


Figure 14: Full-time Parallel Interface to INTEL Microcomputer Systems

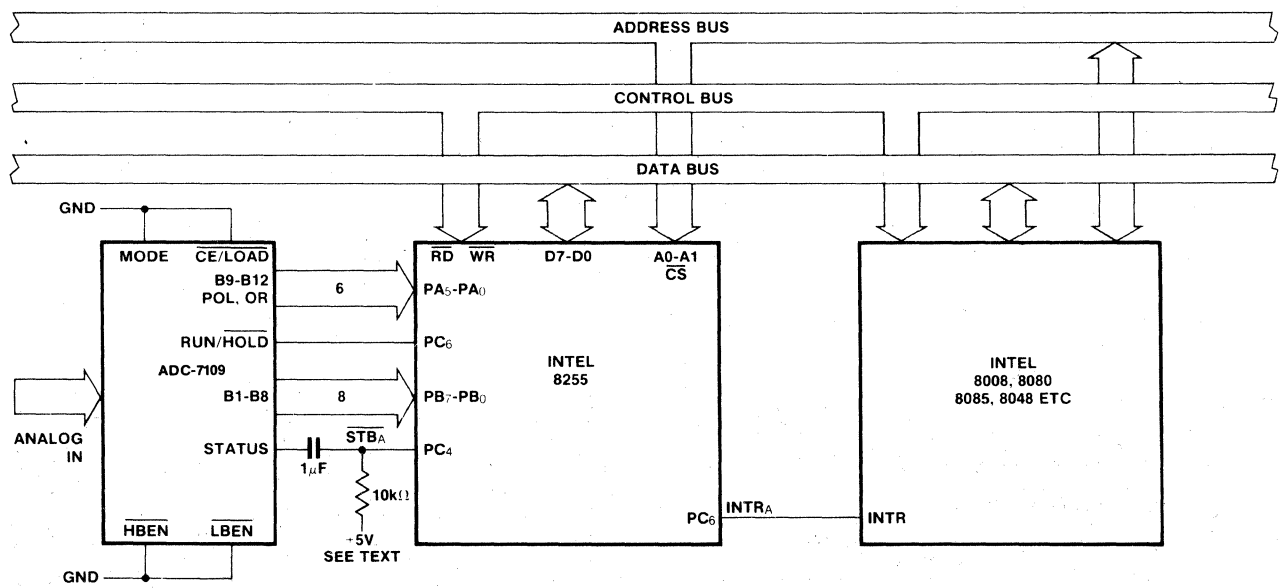


Figure 15: Full-time Parallel Interface to INTEL Microcomputers With Interrupt

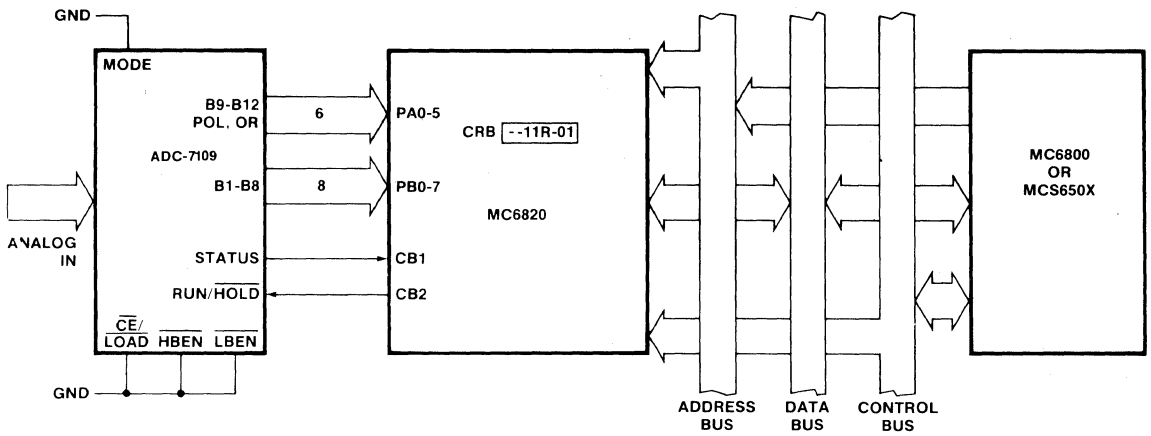


Figure 16: Full-time Parallel Interface to MC6800 or MCS650X Microprocessors

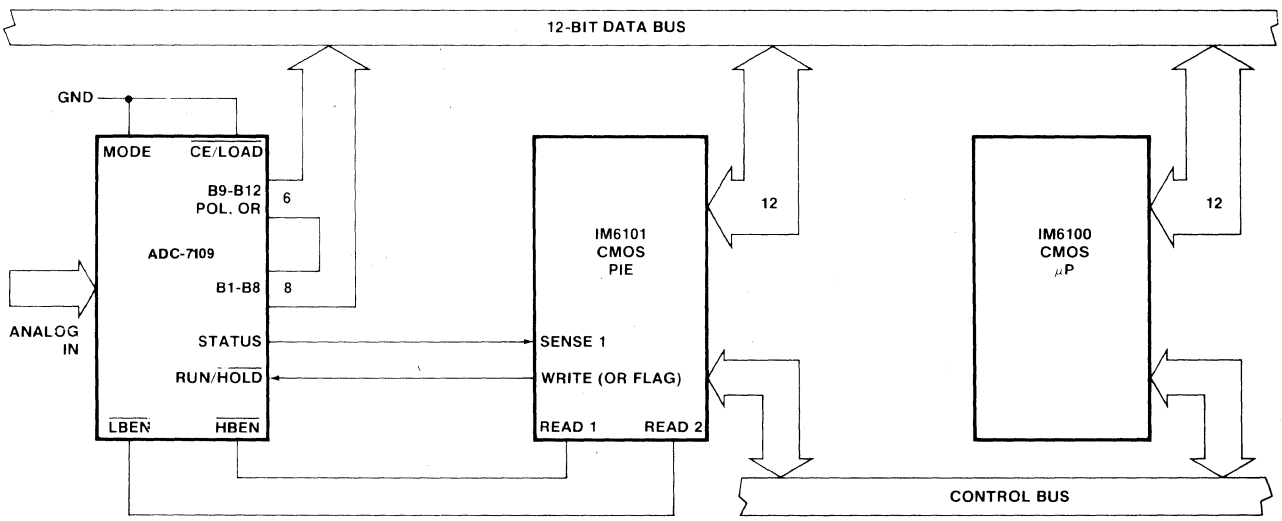


Figure 17: ADC-7109-IM6100 Interface Using IM6101 PE

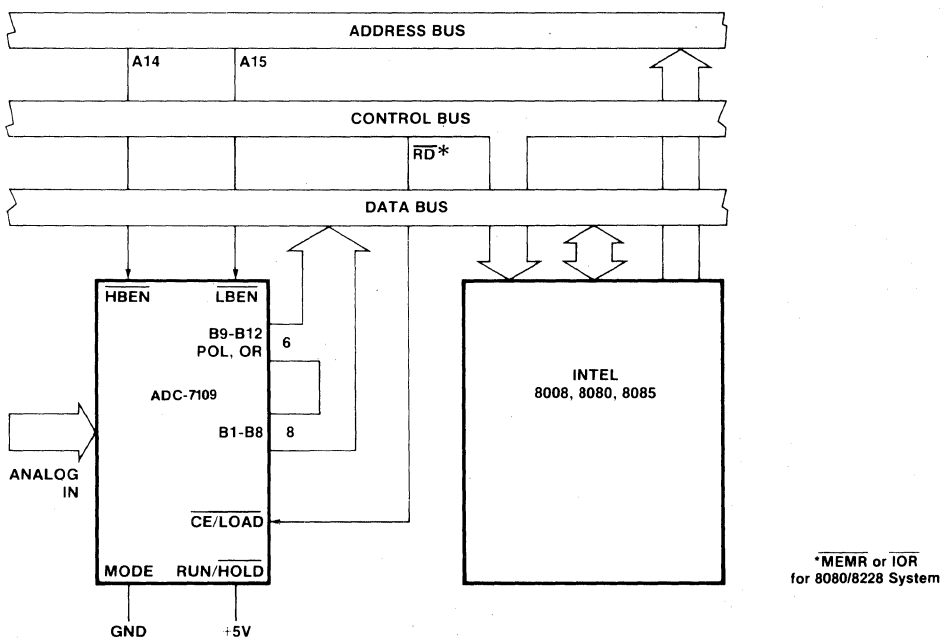


Figure 18: Direct ADC-7109-INTEL 8080/8085 Interface

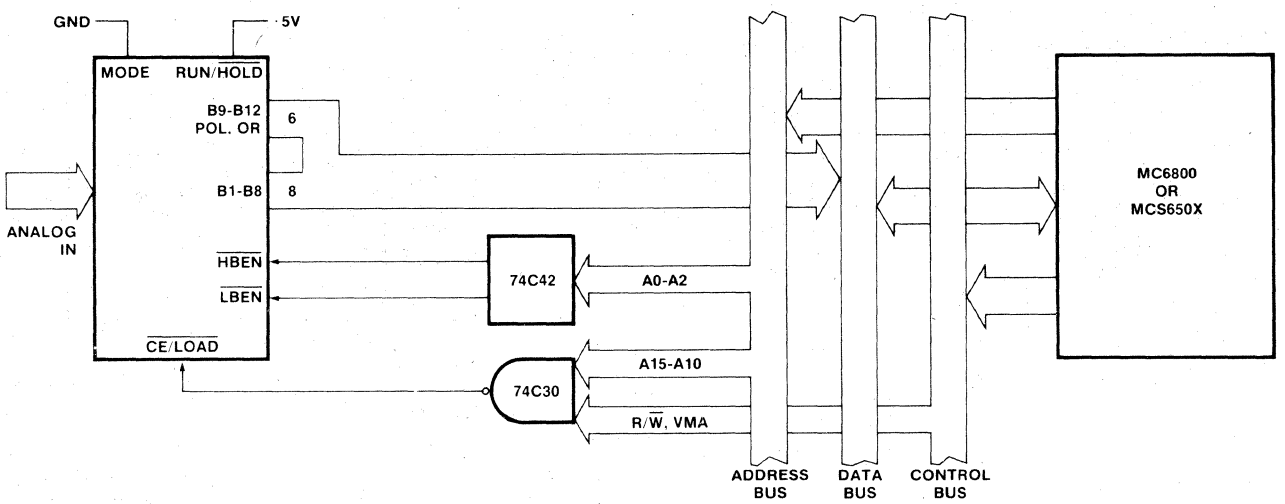


Figure 19: Direct ADC-7109 — MC6800 Bus Interface

Handshake Mode

The handshake mode allows ready interface with a wide variety of external devices. For instance, external latches may be clocked by the rising edge of $\overline{CE/LOAD}$, and the byte enables may be used as byte identification flags or as load enables.

Figure 20 shows a handshake interface to Intel microprocessors again using an 8255PPI. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the ADC-7109, and using the $\overline{CE/LOAD}$ to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1 for the port used. If the 7109 is in handshake mode and the 8255 IBF flag is low, the next word will be strobed into the port. The strobe will cause IBF to go high (SEND goes low), which will keep the enabled byte outputs active. The PPI will generate an interrupt which when executed will result in the data being read. When the byte is read, the IBF will be reset low, which causes the ADC-7109 to sequence into the next byte. This figure shows the MODE input to the ADC-7109 connected to a control line on the PPI. If this output is left high, or tied high separately, the data from every conversion (provided the data access takes less time than a conversion) will be sequenced in two bytes into the system.

If this output is made to go from low to high, the output sequence can be obtained on demand, and the interrupt may be used to reset the MODE bit. Note that the RUN/$\overline{HOLD}$ input to the ADC-7109 may also be driven by a bit of the 8255 so that conversions may be obtained on command under software control. Note that one port of the 8255 is not used, and can service another peripheral device. The same arrangement can also be used with the 8155.

Figure 21 shows a similar arrangement with the MC6800 or MCS650X microprocessors, except that both MODE and RUN/$\overline{HOLD}$ are tied high to save port outputs.

The handshake mode is particularly convenient for directly interfacing to industry standard UARTs (such as the Intersil IM6402/6403 or Western Digital TR1602) providing a minimum component count means of serially transmitting converted data. A typical UART connection is shown on page 3. In this circuit, any word received by the UART causes

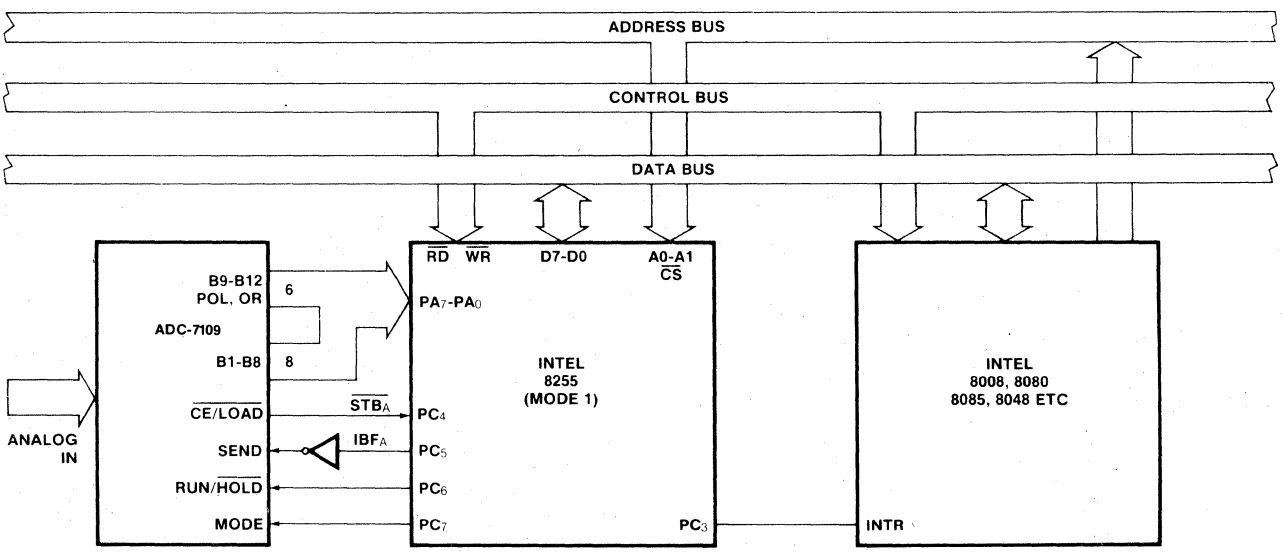


Figure 20: Handshake Interface — ADC-7109 to INTEL MCS-48, -80, 85

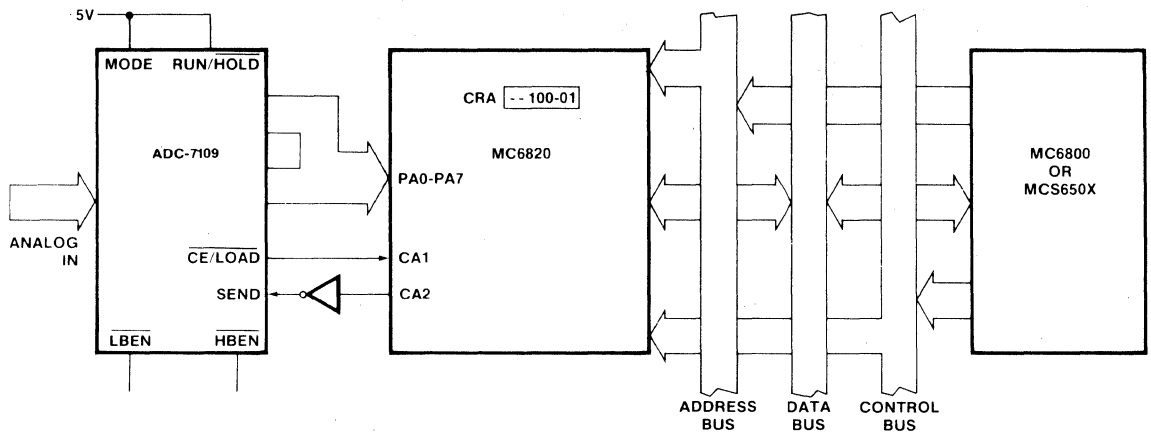


Figure 21: Handshake Interface — ADC-7109 to MC6800, MCS650X

the UART DR (Data Ready) output to go high. This drives the MODE input to the ADC-7109 high, triggering the ADC-7109 into handshake mode. The high order byte is output to the UART first, and when the UART has transferred the data to the Transmitter Register, TBRE (SEND) goes high and the second byte is output. When TBRE (SEND) goes high again, $\overline{\text{LBEN}}$ will go high, driving the UART DRR (Data Ready Reset) which will signal the end of the transfer of data from the ADC-7109 to the UART.

Figure 22 shows an extension of the one converter - one UART scheme of the Typical Connection to several ICL7109s with one UART. In this circuit, the word received by the UART (available at the RBR outputs when DR is high) is used to select which converter will handshake with the UART. With no external components, this scheme will allow up to eight ADC-7109s to interface with one UART. Using a few more components to decode the received word will allow up to 256 converters to be accessed on one serial line.

The applications of the ADC-7109 are not limited to those shown here. The purpose of these examples is to provide a starting point for users to develop useful systems, and to show some of the variety of interfaces and uses of the ADC-7109 . Many of the ideas suggested here may be used in combination; in particular the uses of the STATUS, RUN/$\overline{\text{HOLD}}$, and MODE signals may be mixed.

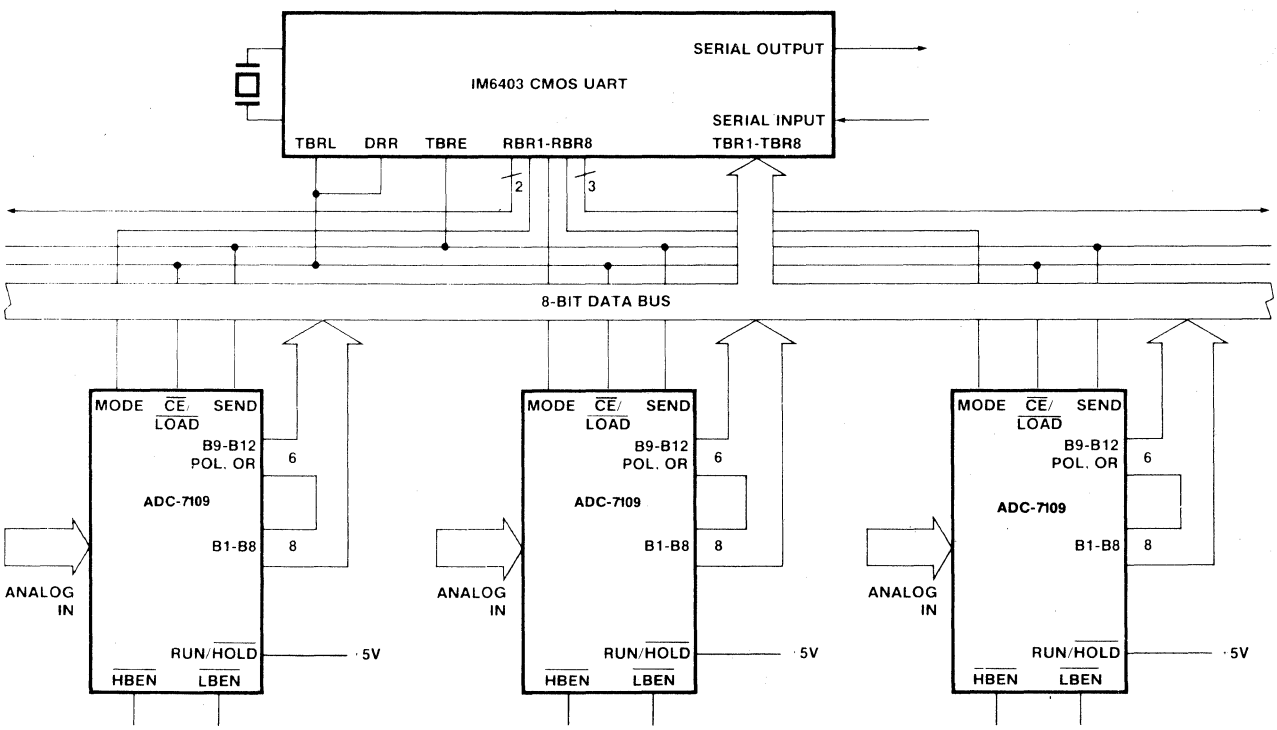


Figure 22: Multiplexing Converters with Mode Input

DATEL INTERSIL
11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL (617)339-9341 / TWX 710-346-1953 / TLX 951340
Santa Ana, (714)835-2751, (L.A.) (213)933-7256 • Sunnyvale, CA (408)733-2424 • Gaithersburg, MD (301)840-9490
• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

Monolithic 10 Bit Tracking A/D Converter ADC-856

FEATURES

- **Continuous Tracking Operation**
- **10^6 Conversions/sec**
- **10 Bit Resolution**
- **Monotonic Over Temperature**
- **Controllable Outputs**
- **TTL/CMOS Compatible**

GENERAL DESCRIPTION

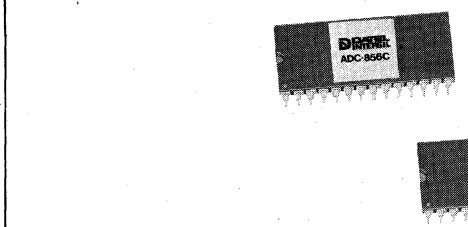
The ADC-856 is a 10 bit tracking A/D converter, capable of supplying continuously updated conversion data on full scale sinusoidal signals up to 300 Hz without the need for a sample and hold. This converter is linear to ±½ LSB min. and is monotonic over its operating temperature range. A number of innovative features give this device the flexibility for a wide range of applications.

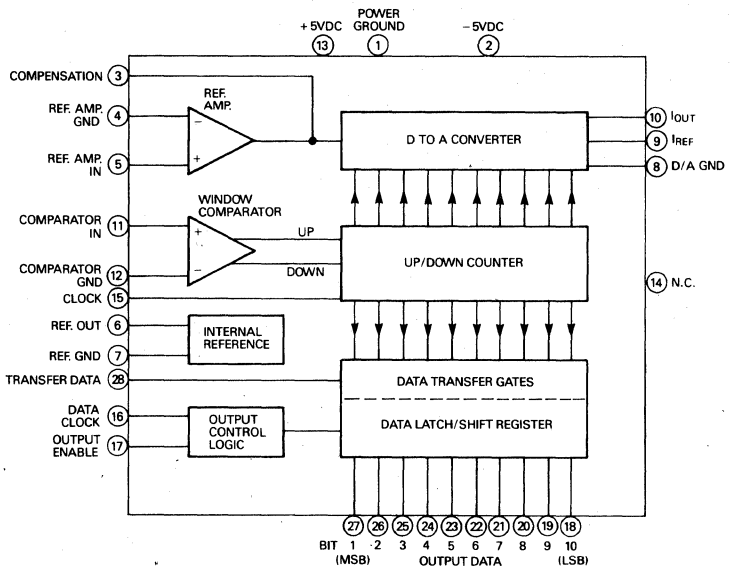
The circuit is implemented in bipolar, monolithic form. The chip contains a fast window comparator, tracking logic, an up/down counter, a D/A converter, a precision voltage reference with amplifier, data transfer gates, and a data latch/shift register. The external parts required for operation have been held to a few passive components, and allow external programming of the analog input voltage range. Gain temperature coefficient of the circuit is ±10 ppm/°C, exclusive of reference.

The ADC-856 is optimized for operation in a continuous tracking mode. In this conversion technique each conversion of an analog signal is based on the last converted value of that signal. For signals that do not vary faster than the converter can track, or 1 LSB/μsec, continuous tracking will provide a valid, updated conversion result every microsecond.

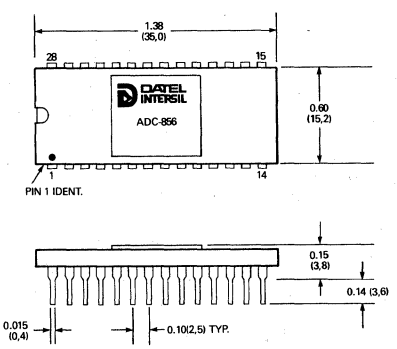
Logic control inputs contribute to this device's usefulness in many different applications. The data transfer gates allow selection of the rate at which the output latch/shift register is updated. The rate may vary from once every microsecond to updating only upon receipt of a command from an external controller. External control also allows selection of output data form, which may be parallel or serial (by supplying an optional clock input). The outputs may be disabled completely in either mode by holding the output enable input low.

The ADC-856 operates on ±5 VDC power at 50 mA with a power supply rejection of 0.1%/V. The device is packaged in a 28 ceramic DIP and is available in two operating temperature ranges: 0°C to +70°C and −55°C to +125°C.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	POWER GROUND	15	CLOCK
2	−5VDC	16	DATA CLOCK
3	COMPENSATION	17	OUTPUT ENABLE
4	REF. AMP. GND.	18	BIT 10 OUT (LSB)
5	REF. AMP. IN	19	BIT 9 OUT
6	REF. OUT	20	BIT 8 OUT
7	REF. GND.	21	BIT 7 OUT
8	D/A GND.	22	BIT 6 OUT
9	I_{REF}	23	BIT 5 OUT
10	I_{OUT}	24	BIT 4 OUT
11	COMPARATOR IN	25	BIT 3 OUT
12	COMPARATOR GND.	26	BIT 2 OUT
13	+5VDC	27	BIT 1 OUT* (MSB)
14	N.C.	28	TRANSFER DATA

*Serial data output when in serial data mode

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS ADC-856
Typical at 25° C, ±5V Supply and Internal Reference, unless otherwise noted

MAXIMUM RATINGS	
Supply Voltage	±7 Volts
Logic Input Voltage	0V to $+V_{CC}$
PERFORMANCE	
Resolution	10 Bits
Linearity Error	±½ LSB max.
Differential Linearity Error	±½ LSB
No Missing Codes	Over Oper. Temp. Range
Conversion Time, 1 LSB change	1 μsec.
Conversion Time, Full Scale Change	1.024 msec[1]
Tracking Speed	1 LSB/μsec max.
Tracking Bandwidth, Full Scale	300 Hz[2]
Gain Tempco	10 ppm/° C[4]
Zero Tempco	7 ppm/° C of FSR[6]
Power Supply Rejection	0.1%/V
INPUTS	
Analog Input Range[7], Unipolar	0 to +5V, 0 to +10V
Bipolar	±2.5V, ±5V, ±10V
Reference Current	1 mA ±0.2 mA
Input Logic Level, HI ("1")	+2.0V min @ 50 μA[3]
Input Logic Level, LO ("0")	+0.8V max. @ 1 μA[3]
Clock Pulse Width	100 nsec. min.
Clock Rate	1 MHz max.
Data Transfer Input	Hold HI for 50 nsec. min. to load output latches
Output Enable Input	When LO, disables data clock and turns outputs off (HI)
Data Clock Input	When driven by clock at ≤ 1MHz with min. pulse width of 100 nsec., provides serial data ouput at Pin 27.
OUTPUTS	
Reference Voltage	2.48V ±1.5%
Reference Tempco	40 ppm/° C
Reference Load Current, max.	4 mA
D/A Output Current, Full Scale	4 mA[5]
Data Output	Parallel or Serial
Output Logic Level, HI ("1")	+2.4V min. @ −40 μA
Output Logic Level, LO ("0")	+0.4V max. @ 1.6 mA
Coding, Unipolar	Straight Binary
Coding, Bipolar	Offset Binary
POWER REQUIREMENT	
Supply Voltage Range	±4.5V to ±5.5V
Supply Current	50 mA
Power Consumption	500 mW
Operating Temperature Range	
ADC-856C	0° C to +70° C
ADC-856M	−55° C to +125° C
Storage Temperature Range	−55° C to +125° C
Package	28 Pin Ceramic DIP

NOTES:

1. Conversion time is directly dependent on the magnitude of input signal change.
2. Tracking bandwidth is inversely proportional to input signal amplitude, e.g. at half scale bandwidth is 600 Hz.
3. $V_S = \pm 5.5V$
4. Exclusive of Reference.
5. The Full Scale D/A Output Current is 4 Times I_{REF}.
6. FSR is Full Scale Range, the difference between maximum and minimum inputs.
7. Analog input range is programmed by an external resistor.

TECHNICAL NOTES

1. The transfer of conversion data to the outputs is controlled by the transfer gates. When TRANSFER DATA is held high the outputs update with each conversion. To update the outputs upon command, TRANSFER DATA is taken high for a maximum of 50 nsec., no sooner than 150 nsec. after the active (negative going) edge of the main clock. TRANSFER DATA must go low before the next main clock edge. When TRANSFER DATA is low, the data is held in the output register.

2. Conversion data appears at the outputs in parallel form. Data may be obtained in serial form by clocking DATA CLOCK at up to 1 MHz, with a minimum pulse width of 100 nsec and TRANSFER DATA low. Serial output data (MSB first) is then available at pin 27.

3. When OUTPUT ENABLE is taken low DATA CLOCK is disabled and all output transistors are turned off (all bit outputs go high).

4. The converter tracks the input signal level at a speed of 1 LSB/μsec; thus the conversion time for any input signal change is given by

$$\frac{\Delta V_{IN}}{1\ LSB} = \text{conversion time in } \mu\text{sec}$$

5. Full Scale D/A output current is four times the reference current; for optimum performance the reference current should be 1 mA. An external reference can be used which can range from .8 mA to 1.2 mA.

6. The tracking bandwidth is inversely proportional to the amplitude of the input signal, e.g., at half scale the bandwidth is 600 Hz.

7. The window comparator and tracking logic determine whether the up/down counter will count up/count down or retain the same value on the negative going edge of the clock pulse.

8. Since the gain tempco of the converter is typically 10 ppm/° C, it is recommended that 10 ppm/° C metal film resistors be used for R_3, R_4 and R_5 for best performance over temperature. The internal reference will typically add 40 ppm/° C to the gain tempco. For improved performance a high quality external reference should be used.

9. R_1 and R_2 compensate for the input bias currents of the reference amplifier and comparator whose inputs are at virtual ground. Thus $R_1 = R_3$ and R_2 = the parallel combination of R_4, R_5 and R_6. The parallel combination of R_4, R_5 and R_6 should be as close to 625Ω as possible as this determines the D/A settling tim e and therefore conversion time. Refer to the resistor tables for a list of typical values for these resistors.

ORDERING INFORMATION

MODEL	OPER. TEMP. RANGE
ADC-856C	0° C to +70° C
ADC-856M	−55° C to +125° C

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

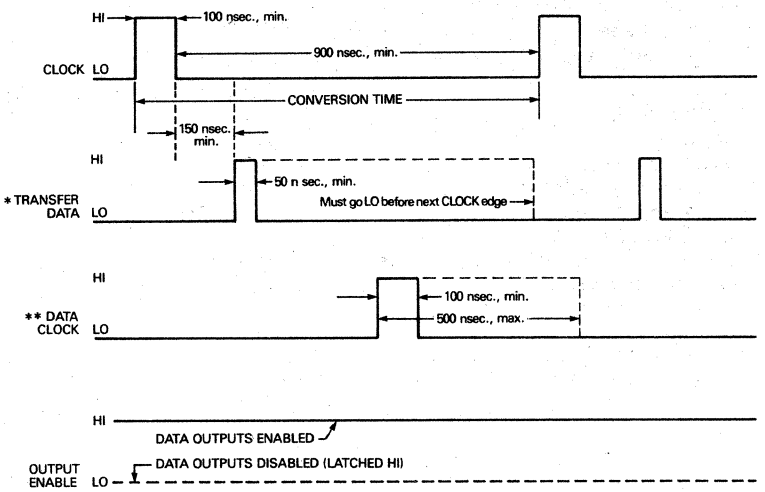
THEORY OF OPERATION

The ADC-856 converters employ a tracking conversion technique. Tracking converters are most effectively used in single channel operations on a continuous signal. In this technique each conversion is based on the previous conversion value. A fast window comparator determines whether an up/down counter increments by 1 LSB, decrements by 1 LSB or remains at its last value. The digital word in the counter controls a D/A converter with a precision reference; the analog output goes to the comparator and is compared with the analog input signal.

For signals with a rate of change less than the converter's maximum rate of change (tracking speed), each comparison represents a valid conversion and the converter is therefore tracking the signal. Tracking is not possible when the input signal varies at a rate greater than the converter's maximum or is discontinuous, as in multiplexed applications. In these cases the converter will change at its maximum rate (1 LSB/μsec) until it attains the new signal level. While this acquisition is in progress, each converter step is available to the output as data, even though it does not yet represent the input signal level. The time required to acquire a new signal level is directly proportional to its difference from the previous level; for a full scale change this period is over 1 msec. Allowance should be made for the acquisition time when a rapid signal change is introduced.

APPLICATIONS

TIMING DIAGRAM



*IF TRANSFER DATA IS HELD HI, THEN THE COUNTER OUTPUTS APPEAR DIRECTLY AT THE BIT OUTPUTS.

**DRIVEN FOR SERIAL DATA OUTPUT ONLY

CODING TABLES

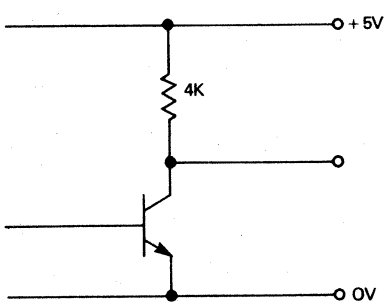
UNIPOLAR OPERATION STRAIGHT BINARY

SCALE	CODE
+FS −1 LSB	1111111111
+¾ FS	1100000000
+½ FS	1000000000
+¼ FS	0100000000
+1 LSB	0000000001
0	0000000000

BIPOLAR OPERATION OFFSET BINARY

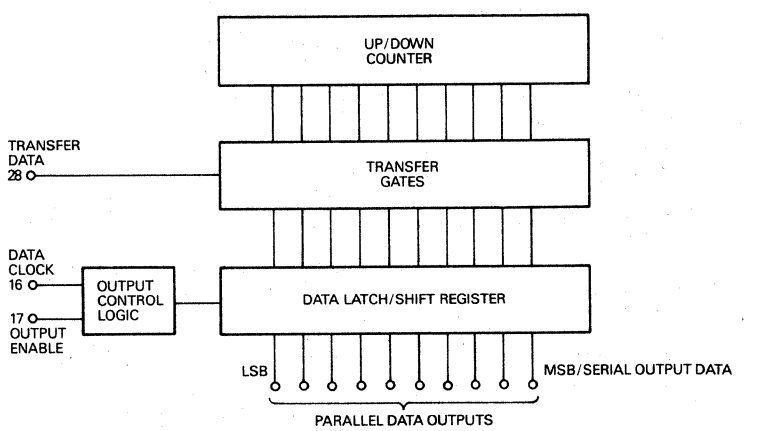
SCALE	CODE
+FS −1 LSB	1111111111
+½ FS	1100000000
+1 LSB	1000000001
0	1000000000
−1 LSB	0111111111
−½ FS	0100000000
−FS + 1 LSB	0000000001
−FS	0000000000

BIT OUTPUT DIAGRAM



IF OUTPUT ENABLE IS LO ALL OUTPUTS TRANSISTORS ARE TURNED OFF AND ALL BIT OUTPUTS ARE HI.

OUTPUT LOGIC CONTROL



TRANSFER DATA (PIN 28)

HI: Min. 50 nsec pulse transfers parallel data from the up/down counter to the data latch/shift register. May be held high for continuous data transfer

LO: Data in latches held, new data from counter not transferred to data latches

DATA CLOCK (PIN 16)

HI: Clocked at up to 1 MHz for serial data output at Pin 27, MSB first

LO: Output data in parallel format at pins 18-27

OUTPUT ENABLE (PIN 17)

HI: Data available at outputs (parallel or serial)

LO: Output transistors turned OFF, all data outputs latched HI

CONNECTION AND CALIBRATION

CALIBRATION PROCEDURE

1. Connect the converter as shown in the connection diagram. Note that Pin 6 is connected to R_3 and R_4 only when the internal reference is used (dotted line on diagram).
2. Select R_1 through R_6 from values given in the resistor table or calculate from the equations that accompany it.
3. Drive the MAIN CLOCK input (Pin 15) with a compatible clock signal at up to 1 MHz and apply a logic HI to TRANSFER DATA (Pin 28).

UNIPOLAR OPERATION

Zero and Gain Adjustments

1. Apply an analog input voltage of zero +½ LSB.
2. Adjust the zero adjustment so that the output code flickers between 000...000 and 000...001.
3. Apply an analog input voltage of +F.S. −1½ LSB.
4. Adjust the gain adjustment (R_3) so that the output code flickers between 111...110 and 111...111.

BIPOLAR OPERATION

Offset and Gain Adjustments

1. Apply an analog input voltage of −F.S. +½ LSB.
2. Adjust the offset adjustment (R_4) so that the output code flickers between 000...000 and 000...001.
3. Apply an analog input voltage of +F.S. −1½ LSB.
4. Adjust the gain adjustment (R_3) so that the output code flickers between 111...110 and 111...111.

CALIBRATION RESISTOR VALUES

R_4 adjusts the offset for bipolar operations; in unipolar operations R_4 is replaced with a zero adjustment circuit shown in applications. In either mode R_3 adjusts the gain. If the predicted values of these resistors do not supply the transition points expected, their values should be recalculated. Each may be trimmed with a 100 ppm/°C trimming pot used in series with the resistor. The trim pots should be constrained to approximately 1% of the nominal value calculated.

The values of R_1 through R_6 are calculated from the following:

*$R_1 = R_3$ *R_2 = the parallel combination of R_4, R_5 and R_6.

$$R_3 = \frac{V_{REF}}{1.0\ mA} \qquad R_4 = \frac{-V_{REF} R_5}{V_{IN}min}$$

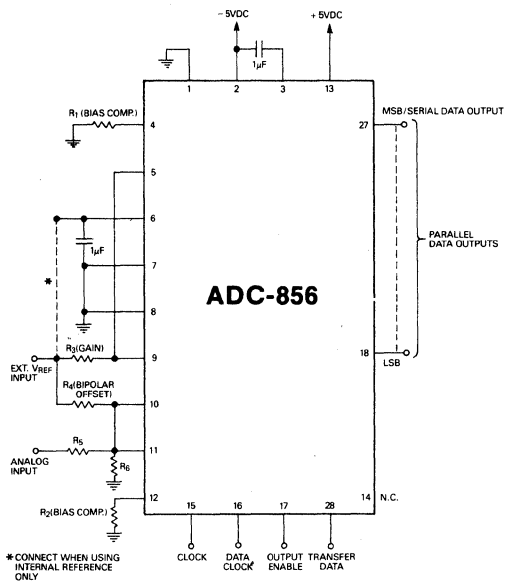
$$R_5 = \frac{FSR^{**}}{I_{OUT}(max)}$$

*R_6 is chosen so that the parallel combination of R_4, R_5 and R_6 is approximately 625Ω, this determines the D/A time constant and hence conversion time.

*The nearest preferred value may be used for these resistors.

**F.S.R. is Full Scale Range, the difference between maximum input voltage and minimum input voltage.

CONNECTION & CALIBRATION DIAGRAM

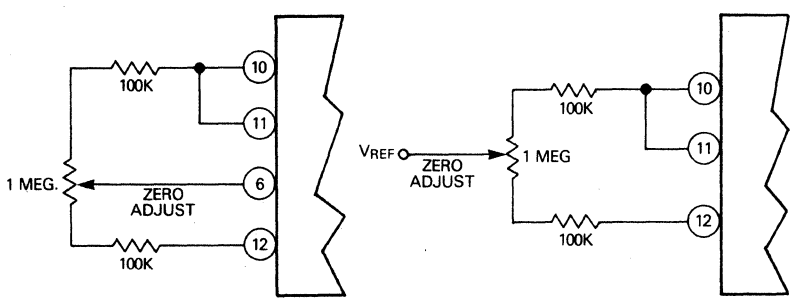


RESISTOR TABLES

ANALOG INPUT RANGE	V_{REF}[2]	R_1[1]	R_2[1]	R_3	R_4	R_5	R_6[1]
0 to +2.5V	2.5V	2.5K	625Ω	2.5K	∞	625Ω	∞
0 to +5.0V	2.5V	2.5K	625Ω	2.5K	∞	1.25K	1.25K
±2.5V	2.5V	2.5K	625Ω	2.5K	1.25K	1.25K	∞
0 to +10V	2.5V	2.5K	625Ω	2.5K	∞	2.5K	835Ω
±5V	2.5V	2.5K	625Ω	2.5K	1.25K	2.5K	2.5K
±10V	2.5V	2.5K	625Ω	2.5K	1.25K	5K	1.67K

NOTES: 1. The nearest preferred value may be used for R_1, R_2 and R_6.
2. For external reference set $R_1 = V_{REF}$ (Kohms)

UNIPOLAR ZERO



FOR UNIPOLAR OPERATION WHERE R_4 APPROACHES ∞ AND A ZERO ADJUSTMENT IS REQUIRED, THIS CIRCUIT MAY BE USED TO REPLACE R_4

DATEL INTERSIL
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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

12 Bit, Low Power A/D Converter Model ADC-HC12B

FEATURES

- **Single Supply Operation**
- **Automatic Standby Mode Control**
- **Low Power Consumption**
- **Six Input Ranges**
- **MIL Temp Range Available**

GENERAL DESCRIPTION

The ADC-HC is a complete, 12 bit, low power analog to digital converter utilizing CMOS technology. This hybrid IC incorporates active laser trimming of highly stable thin-film resistors to provide module performance (ADC-CM) with IC price, size and reliability.

The device is ideal for portable and remote applications such as seismology, oceanography, meteorology, pollution monitoring and battery operation system. Other key applications include military and aerospace, requiring wide operating temperature range and high reliability.

The ADC-HC converter has the capability of operating from either a single +9V DC to +15V DC power source (interrupt power mode) or from a ±9VDC to ±15VDC power source (continuous power mode) at a maximum conversion rate of 3.3 kHz.

A key feature of this unit when operating in the interrupt power mode is the extremely low quiescent power consumption (less than 10μA @ 12V, 25°C).

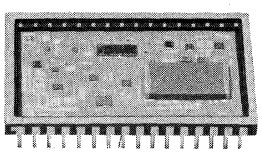
Upon receipt of a convert command, the analog circuitry of the converter is energized and stabilizes in 50 μsec. A complete conversion is performed at which time the EOC goes low, turning off the analog circuitry, and returns to its quiescent state. The digital data remains valid until it is updated by the next conversion.

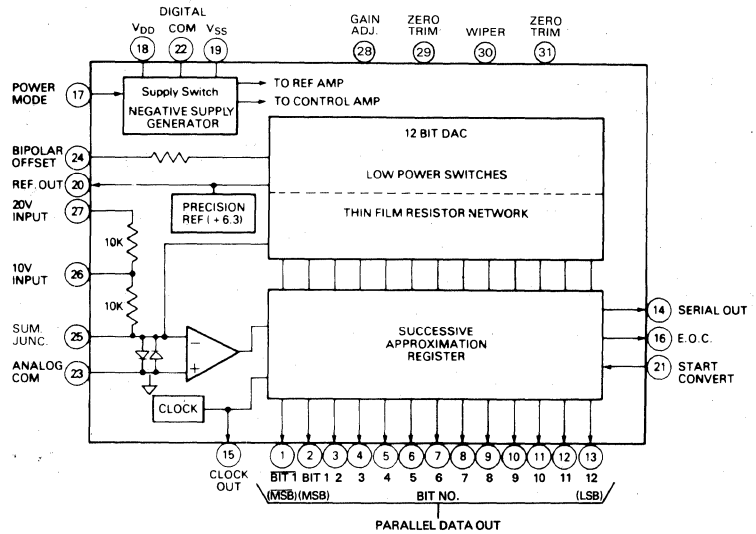
Power consumption is a function of conversion rate. For 100, 1K and 2K conversions per second, the average power drain is approximately 3.5, 26 and 50 milliwatts respectively.

Six input voltage ranges are provided by external pin connection: 0 to +5V, 0 to +10V, 0 to +20V, ±2.5V, ±5V, and ±10V. Nonlinearity is specified at ±½ LSB max. with a gain tempco of ±30 ppm/°C. Output coding is straight binary, offset binary or 2's complement. Serial data is also brought out.

The converters are cased in 32 pin DIP packages. Models are available for three different operating temperature ranges: 0 to +70, −25 to +85 and −55 to +125 degrees centigrade. High reliability versions of each temperature range are also available under Datel-Intersil's "S" program and MIL-STD-883 level B screening.

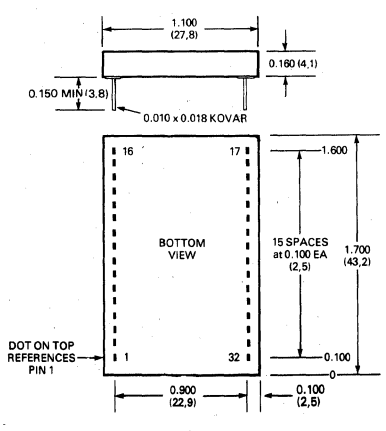
CAUTION: The ADC-HC Series are CMOS devices and should be handled carefully to prevent static charge pickup which might damage the devices. The devices should be kept in the shipping containers until ready for installation.





MECHANICAL DIMENSIONS

INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	17	POWER MODE
2	BIT 1 (MSB)	18	V_{DD}
3	BIT 2	19	V_{SS}
4	BIT 3	20	REF OUT
5	BIT 4	21	START CONVERT
6	BIT 5	22	DIGITAL COM.
7	BIT 6	23	ANALOG COM.
8	BIT 7	24	BIPOLAR OFFSET
9	BIT 8	25	SUM. JUNC.
10	BIT 9	26	10V INPUT
11	BIT 10	27	20V INPUT
12	BIT 11	28	GAIN ADJ.
13	BIT 12 (LSB)	29	ZERO TRIM
14	SERIAL OUT	30	ZERO ADJ (WIPER)
15	CLOCK OUT	31	ZERO TRIM
16	E.O.C. (STATUS)	32	N.C.

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, ADC-HC12B
(Typical at 25°C, ±12V, unless otherwise noted)

MAXIMUM RATINGS

Positive Supply (V_{DD})	+18V
Negative Supply (V_{SS})	−18V
Analog Inputs	±25V
Digital Inputs	0 to V_{DD}

INPUTS

Analog Input Ranges, unipolar	0 to +5V, 0 to +10V, 0 to +20V
Analog Input Ranges, bipolar	±2.5V, ±5V, ±10V
Input Impedance	5K (0 to +5V, ±2.5V) 10K (0 to +10V, ±5V) 20K (0 to +20V, ±10V)
Start Convert, Interrupt Mode	Positive Pulse with duration of 50μS min.
Start Convert, Continuous Mode	Positive Pulse with duration of 5μS min.
V_{IL} (Logic "0")	0.05 V_{DD} max.
V_{IH} (Logic "1")	0.95 V_{DD} min.
Input Current	30 pA
Input Capacitance	15 pF

OUTPUTS

Parallel Output Data	12 parallel lines of data, held until next conversion command
V_{OL} (Logic "0")	0V, −2.0mA
V_{OH} (Logic "1")	V_{DD}, +4.0mA
All Digital Outputs	CMOS Compatible
Coding, unipolar	Straight Binary
Coding, bipolar	Offset Binary, 2's Complement
Serial Output	NRZ successive decision pulses out MSB first, Straight Binary or Offset Binary
Clock Output	Train of positive going (V_{DD}) 25 μS pulses, 40 kHz
E.O.C. (Status)	Conversion Status Signal, Logic "1" during reset and conversion, Logic "0" when conversion complete (data valid)

PERFORMANCE

Resolution	12 Bits
Nonlinearity	±½ LSB max.
Differential Nonlinearity	±½ LSB max.
Gain Error	Adjust to zero
Offset or Zero Error	Adjust to zero
Gain Tempco	±30 ppm/°C max.
Offset Tempco	±20 ppm/°C of FSR max.
Zero Tempco	±10 ppm/°C of FSR
Diff. Nonlinearity Tempco	±2 ppm/°C of FSR
No Missing Codes	Guaranteed over operating temperature range
Conversion Time	300 μS max.
Throughput Time	305 μS max. continuous power mode 350 μS max. interrupt power mode
Power Supply Rejection	.003%/% Supply

POWER REQUIREMENT

Continuous Power Mode V_{DD}	+9.0V to +15.0V
V_{SS}	−9.0V to −15.0V
Interrupt Power Mode V_{DD}	+9V to +15.0V
Power Consumption, Continuous Mode	112 mW
Quiescent Mode	120μW max., 12μW typ.

PHYSICAL-ENVIRONMENTAL

Operating Temperature Range	0°C to +70°C (BGC, BMC) −25°C to +85°C (BMR) −55°C to +125°C (BMM)
Storage Temperature Range	−65°C to +150°C
Package Type	Ceramic
Pins	0.010 x 0.018 inch Kovar
Weight	0.5 oz. (14 g.)

TECHNICAL NOTES

1. The ADC-HC contains CMOS components and must be properly handled to prevent damage from static pick-up. Proper anti-static handling procedures should be observed including storage in conductive foam or shorting all pins together with aluminum foil. Do not connect in circuit under "power on" conditions. Digital signals should be applied after the converters power has been turned on.
2. It is recommended for single supply (+12V nominal) or dual supply (±12V nominal) operation, the power input pins should be bypassed to ground with a .1μF ceramic capacitor. It is not critical that the supplies be balanced.
3. Analog and digital grounds should be kept separate whenever possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Common (Pin 23) and Digital Ground (Pin 22) are not connected internally and must be tied together externally.
4. The ADC-HC can operate from either a single or dual supply. When using dual supplies, tie POWER MODE (Pin 17) to V_{DD} (Pin 18). In this continuous power mode, an A/D conversion will take place when a 5μsec. or greater positive going pulse is applied to START CONVERT (Pin 21). For single supply operation (interrupt power mode), tie Power Mode (Pin 17) to E.O.C. (Pin 16). When EOC goes low the converter is switched to standby mode (power is disconnected to analog circuitry) and digital output data becomes valid and remains valid until next start pulse is applied. Upon receipt of a 50 μsec. min., 500 usec. max. pulse on START CONVERT (Pin 21), the converter will stabilize, make a complete conversion and return to standby mode.
5. Digital output codes are listed in coding tables. Parallel data is valid when EOC is in low state. This data can be transferred into latches during logic "1" to logic "0" transition of EOC line. Serial data out (Pin 14) is in NRZ (non-return to zero) format. This data is guaranteed valid in a 50 nsec. to 300 nsec. time frame after positive edge of clock. All digital inputs and outputs are CMOS compatible. See application notes for CMOS-TTL interface.
6. REF OUT (Pin 20) is a 6.3V ±5% internal reference pin connection.
7. For zero or offset and gain adjustment refer to connections and calibration notes. The trim pots should be located as close as possible to the converter to avoid noise pickup. Zero point is always adjusted first followed by gain the adjustment with analog input at the most positive end of analog range. The range of the OFFSET (ZERO)ADJ. is ±15 mV. The range of GAIN ADJ. is .1% of full scale range can also be increased by decreasing the value of the series resistor (3.9 MΩ nominal). Potentiometer values are 10K and should be 100 ppm/°C ceramic type (such as Datel TP series).

ORDERING INFORMATION

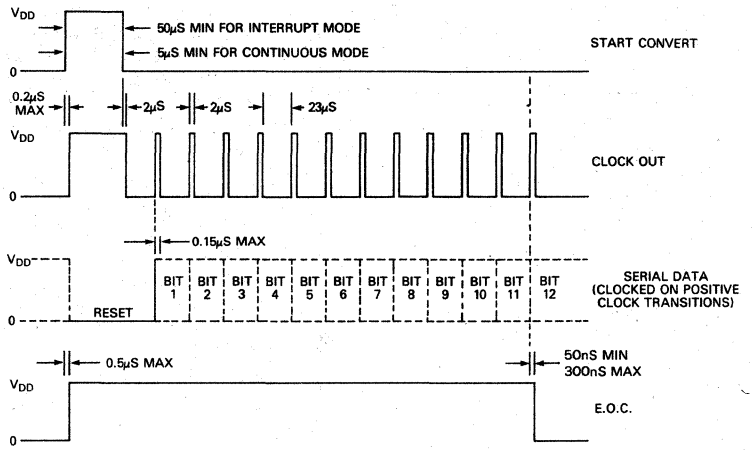
MODEL	TEMP. RANGE	SEAL
ADC-HC12BMC	0 to +70°C	Hermetic
ADC-HC12BMR	−25°C to +85°C	Hermetic
ADC-HC12BMM	−55°C to +125°C	Hermetic

Trimming Potentiometers: TPK 10K (10K ohms)

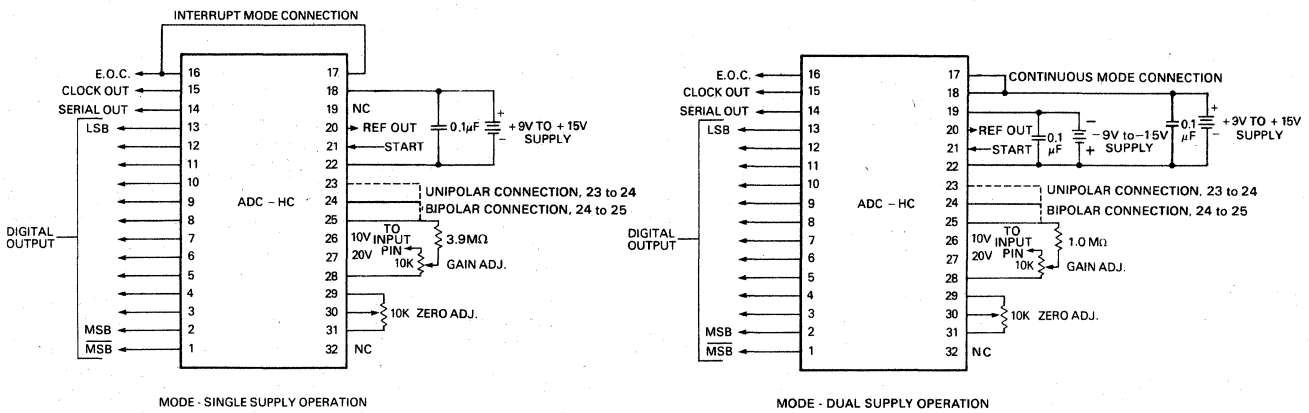
For high reliability versions of the ADC-HC series, including units screened to MIL-STD-883 Level B, contact factory.

THE CONVERTERS ARE COVERED BY GSA CONTRACT

ADC-HC TIMING DIAGRAM



CONNECTIONS DIAGRAM



OUTPUT CODING

INPUT VOLTAGE RANGE				CODING		
	UNIPOLAR			STRAIGHT BINARY		
	0 to +20V	0 to +10V	0 to +5V	MSB		LSB
+FS-1 LSB	+19.9951	+9.9976	+4.9988	1111	1111	1111
+½ FS	+10.0000	+5.0000	+2.5000	1000	0000	0000
+1 LSB	+0.0049	+0.0024	+0.0012	0000	0000	0001
ZERO	0.0000	0.0000	0.0000	0000	0000	0000

	BIPOLAR			OFFSET BINARY*		
	±10V	±5V	±2.5V	MSB		LSB
+FS-1 LSB	+9.9951	+4.9976	+2.4988	1111	1111	1111
+½ FS	+5.0000	+2.5000	+1.2500	1100	0000	0000
+1 LSB	+0.0049	+0.0024	+0.0012	1000	0000	0001
ZERO	0.0000	0.0000	0.0000	1000	0000	0000
−FS-1 LSB	−9.9951	−4.9976	−2.4988	0000	0000	0001
−FS	−10.0000	−5.0000	−2.5000	0000	0000	0000

* For 2's COMPLEMENT, MSB is inverted, use $\overline{\text{MSB}}$ (pin 1)

INPUT PIN CONNECTIONS

INPUT VOLTAGE RANGE	INPUT PIN	CONNECT THESE PINS TOGETHER
0 to +5V	26	23 to 24, 25 to 27
0 to +10V	26	23 to 24
0 to +20V	27	23 to 24
±2.5V	26	24 to 25, 25 to 27
±5V	26	24 to 25
±10V	27	24 to 25

CALIBRATION PROCEDURE

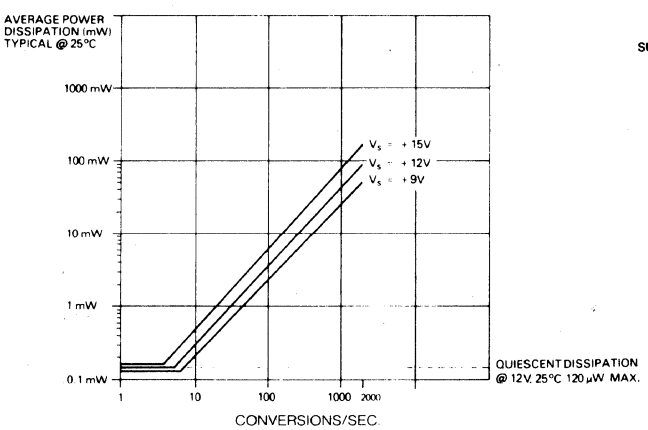
1. Connect converter as shown in the Connection Diagram. Use the Input Pin Connections table for the desired input voltage range. Apply start conversion pulses to start pin.

2. **Zero and Offset Adjustment.**
   Apply a precision voltage reference source between the selected analog input range and ground. Adjust the output of the reference source to + ½ LSB. Adjust zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 for unipolar and 1000 0000 0000 and 1000 0000 0001 for bipolar mode.

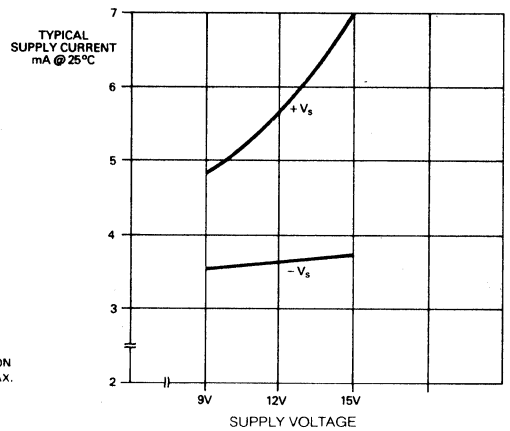
3. **Full Scale Adjustment**
   Change the output of the precision reference source for +FS-1½ LSB. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111.

APPLICATIONS

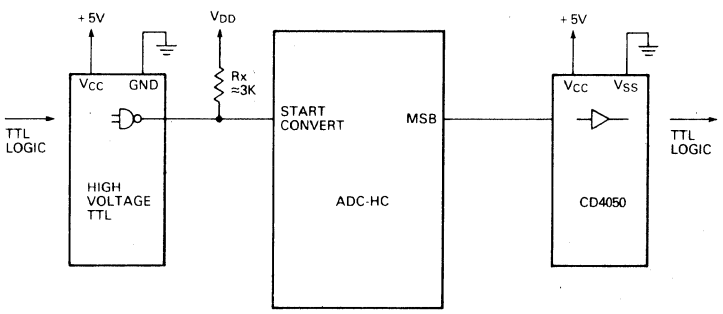
ADC-HC INTERRUPT POWER MODE



ADC-HC CONTINUOUS POWER MODE



TTL-CMOS INTERFACE

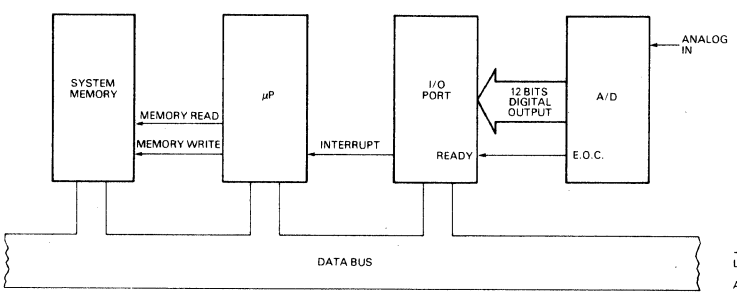


CMOS and TTL logic are not compatible due to different threshold levels. They can, however, be interfaced by simple techniques.

The START CONVERT (Pin 21) can be driven directly from an open collector, high voltage TTL gate. Resistor Rx is used to source current and bring the TTL output up to the CMOS threshold level. Typical values of Rx are 3.3K to 10K ohms.

CMOS to TTL interface requires sufficient sink current in the low state. The CD4049 (inverting) and CD4050 (noninverting) buffers, powered from +5V logic supply can accept input voltage swings of +5 to +15V from the CMOS system. Each buffer gate can drive at least one input from any TTL family.

LOW POWER MICRO-PROCESSOR INTERFACE



SYSTEMS COMPONENTS	MANUFACTURE	MODEL	DATA BITS	TYPE
LOW POWER MICROPROCESSOR	RCA	CDP1802	8	CMOS
	INTERSIL	IM6100	12	CMOS
A/D CONVERTER	DATEL SYSTEMS	ADC-HC	12	CMOS

DATEL INTERSIL
11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617)339-9341 / TWX 710-346-1953 / TLX 951340
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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

12 Bit Microelectronic A/D Converter With Sample-Hold Model ADC-HS12B

FEATURES

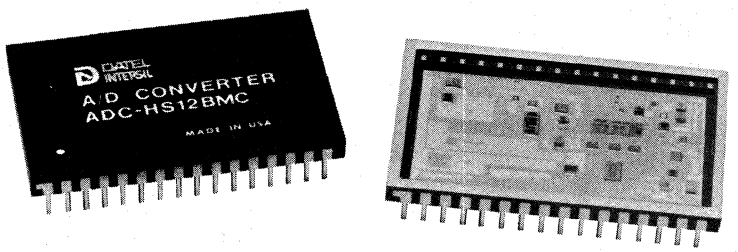
- **12 Bit Resolution**
- **Internal Sample Hold**
- **6μsec. Acquisition Time**
- **9μsec. Conversion Time**
- **Programmable Input Ranges**
- **Parallel & Serial Outputs**

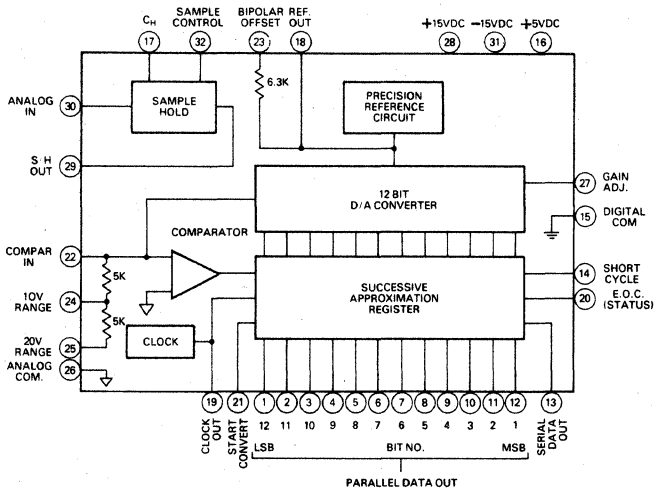
GENERAL DESCRIPTION

The ADC-HS12B is a high performance 12 bit hybrid A/D converter with a self-contained sample-hold. It is specifically designed for systems applications where the sample-hold is an integral part of the conversion process. The internal sample-hold has a 6μsec. acquisition time for a full 10V input change; the A/D converter has a fast 9μsec. conversion time. Five input voltage ranges are programmable by external pin connection: 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V. Input impedance to the sample-hold is 100 megohms. Output coding is complementary binary for unipolar operation and complementary offset binary for bipolar operation, with both parallel and serial outputs brought out.

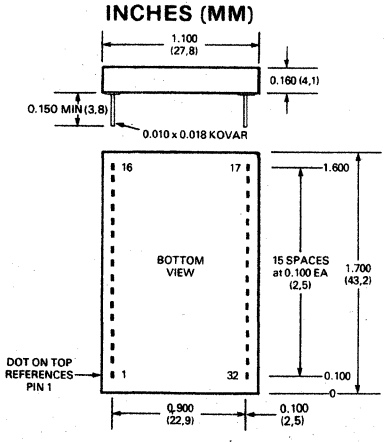
This converter incorporates proven thin film hybrid technology used in high volume production. Quad current switches are combined with a nichrome thin film resistor network to implement the internal 12 bit DAC. To achieve 9μsec. conversion time, the thin film resistors are fabricated on glass, giving lower stray capacitance. Other internal circuits include a precision zener reference, fast comparator, successive approximation register, clock, and sample hold. The thin film resistor network is functionally laser trimmed for optimum converter linearity.

Other features include a gain tempco of 20ppm/°C maximum and differential nonlinearity tempco of ±2ppm/°C; there are no missing codes over the operating temperature range. The package is a miniature 32 pin triple spaced DIP and different models are offered for each of the operating temperature ranges: 0 to 70C, −25 to +85C, and −55 to +100C. Power supply requirement is ±15VDC and +5VDC. High reliability versions are also available under Datel-Intersil's "S" program and MIL-STD-883 level B screening.





MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	17	CH
2	BIT 11 OUT	18	REF. OUT
3	BIT 10 OUT	19	CLOCK OUT
4	BIT 9 OUT	20	E.O.C. (STATUS)
5	BIT 8 OUT	21	START CONVERT
6	BIT 7 OUT	22	COMPAR. INPUT
7	BIT 6 OUT	23	BIPOLAR OFFSET
8	BIT 5 OUT	24	10V RANGE
9	BIT 4 OUT	25	20V RANGE
10	BIT 3 OUT	26	ANALOG COM
11	BIT 2 OUT	27	GAIN ADJ.
12	BIT 1 OUT (MSB)	28	+15V POWER
13	SERIAL DATA OUT	29	S/H OUTPUT
14	SHORT CYCLE	30	ANALOG IN
15	DIGITAL COM.	31	−15V POWER
16	+5V POWER	32	SAMPLE CONTROL

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, ADC-HS12B

(Typical at 25°C. ±15V and +5V supplies unless otherwise noted)

MAXIMUM RATINGS

Positive Supply, pin 28	+18V
Negative Supply, pin 31	−18V
Logic Supply Voltage, pin 16	+5.5V
Digital Input Voltage, pins 14, 21, 32	+5.5V
Analog Input Voltage, pin 30	±15V

INPUTS

Analog Input Ranges, unipolar	0 to +5V, 0 to +10V
Analog Input Ranges, bipolar	±2.5V, ±5V, ±10V
Input Impedance[1]	100 megohms
Input Bias Current[1]	50nA typ., 200nA max.
Start Conversion	2V min. to +5.5V max. positive pulse with 100 nsec. duration min. Rise and fall times <30 nsec. Logic HI to LO transition resets converter and initiates next conversion. Loading: 1 TTL load
Sample Control Input	Logic HI = hold Logic LO = sample Loading: 1 TTL load

OUTPUTS[2]

Parallel Output Data	12 parallel lines of data held until next conversion command. V_{OUT} ("0") ≤ +0.4V V_{OUT} ("1") ≥ +2.4V
Coding, unipolar	Complementary Binary
Coding, bipolar	Complementary Offset Binary
Serial Output Data	Successive decision pulses out, NRZ format, MSB first
End of Conversion (status)	Conversion status signal. Output is logic HI during reset and conversion and LO when conversion is complete.
Clock Output	Train of positive going +5V, 100 nsec. pulses at 1.5 MHz rate.

SAMPLE-HOLD PERFORMANCE[3]

Input Offset Drift	25μV/°C
Acquisition Time, 10V to 0.01%	6μsec.
Bandwidth	1 MHz
Aperture Delay Time	100 nsec.
Aperture Uncertainty Time	10 nsec.
Sample to Hold Error	25mV max.
Hold Mode Droop	200nV/μsec. max.
Hold Mode Feedthrough	0.01% max.

CONVERTER PERFORMANCE

Resolution	12 bits (1 part in 4096)
Nonlinearity	±½ LSB max.
Differential Nonlinearity	±½ LSB max.
Temp. Coefficient of Gain	±20ppm/°C max.
Temp. Coefficient of Zero, unipolar	±5ppm/°C of FSR max.
Temp. Coefficient of Offset, bipolar	±10ppm/°C of FSR max.
Differential Nonlinearity Tempco	±2ppm/°C of FSR
Missing Codes	None over oper. temp. range
Conversion Time	9μsec. max.
Power Supply Rejection	0.002%/% max.

POWER REQUIREMENT

+15VDC ±0.5V @ 60mA
−15VDC ±0.5V @ 50mA
+5VDC ±0.25V @ 100mA

PHYSICAL-ENVIRONMENTAL

Operating Temperature Range	0°C to 70°C (BMC) −25°C to +85°C (BMR) −55°C to +100°C (BMM)
Storage Temperature Range	−65°C to +150°C
Package Type	32 pin ceramic
Pins	0.010 x 0.018 inch Kovar
Weight	0.5 oz. (14 g.)

NOTES:
1. For sample-hold input
2. All digital outputs can drive 2 TTL loads
3. For 1000pF external hold capacitor

TECHNICAL NOTES

1. It is recommended that the −15V power input pins both be bypassed to ground with a .01μF ceramic capacitor in parallel with a 1μF electrolytic capacitor and the +5V power input pin be bypassed to ground with a 1μF electrolytic capacitor as shown in the connection diagrams. In addition, pin 27 should be bypassed to ground with a 0.01μF ceramic capacitor. These precautions will assure noise free operation of the converter.
2. Digital Common (pin 15) and Analog Common (pin 26) are not connected together internally, and therefore must be connected as directly as possible externally. It is recommended that a ground plane be run underneath the case between the two commons. Analog ground and ±15V power ground should be run to pin 26 whereas digital ground and +5V ground should be run to pin 15.
3. External adjustment of zero or offset and gain are provided for by trimming potentiometers connected as shown in the connection diagrams. The potentiometer values can be between 10K and 100K ohms and should be 100ppm/°C cermet types (such as Datel Systems TP series). The adjustment range is ±0.5% of FSR for zero or offset and ±0.3% for gain. The trimming pots should be located as close as possible to the converter to avoid noise pickup. Calibration of the ADC-HS12B is performed with the sample-hold connected and operating dynamically. This results in adjusting out the sample-hold errors along with the A/D converter. For slow throughput applications it is recommended that a 0.01μF hold capacitor be used for best accuracy. With this value the acquisition time becomes 25μsec. and the external timing must be adjusted accordingly.
4. The recommended timing shown in the Timing Diagram allows 6 microseconds for the sample-hold acquisition and then 1 microsecond after the sample-hold goes into the hold mode to allow for output settling before the A/D begins its conversion cycle.
5. Short cycled operation results in shorter conversion times where the conversion can be truncated to less than 12 bits. This is done by connecting pin 14 to the output bit following the last bit desired. For example for an 8 bit conversion, pin 14 is connected to bit 9 output. Maximum conversion times are given for short-cycled conversions in the Table.
6. Note that output coding is complementary coding. For unipolar operation it is complementary binary and for bipolar operation it is complementary offset binary. In cases where bipolar coding of offset binary is required, this can be achieved by inverting the analog input to the converter (using an op amp connected for gain of −1.0000). The converter is then calibrated so that −FS analog input gives an output code of 0000 0000 0000, and +FS−1LSB gives 1111 1111 1111.
7. These converters dissipate approximately 2 watts of power. The case to ambient thermal resistance is approximately 25°C per watt. For ambient temperatures above 50°C, care should be taken not to restrict air circulation in the vicinity of the converter.
8. These converters can be operated with an external clock. To accomplish this, a negative pulse train is applied to START CONVERT (Pin 21). The rate of the external clock must be lower than the rate of the internal clock. The pulse width of the external clock should be between 100 nsec. and 300 nsec. Each N bit converison cycle requires a pulse train of N + 1 clock pulses for completion, e.g., an 8 bit conversion requires 9 clock pulses for completion. A continuous pulse train may be used for consecutive conversions, resulting in an N bit conversion every N + 1 pulses, or the E.O.C. output may be used to gate a continuous pulse train for single conversions.

ORDERING INFORMATION

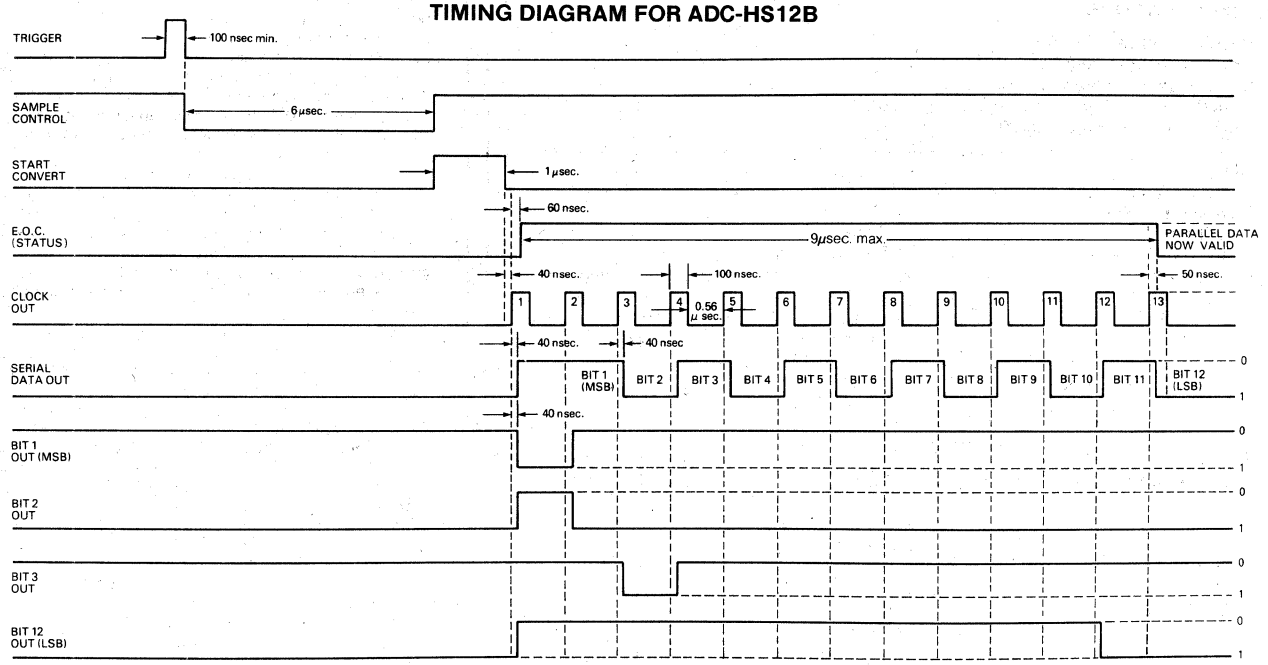
MODEL	TEMP. RANGE	SEAL
ADC-HS12BMC	0 to 70C	Hermetic
ADC-HS12BMR	−25 to +85C	Hermetic
ADC-HS12BMM	−55 to +100 C	Hermetic

Mating Socket: DILS-2 (2 required per converter)
Trimming Potentiometers: TP50K

For high reliability versions of the ADC-HS12B including units screened to MIL-STD-883 level B, contact factory.

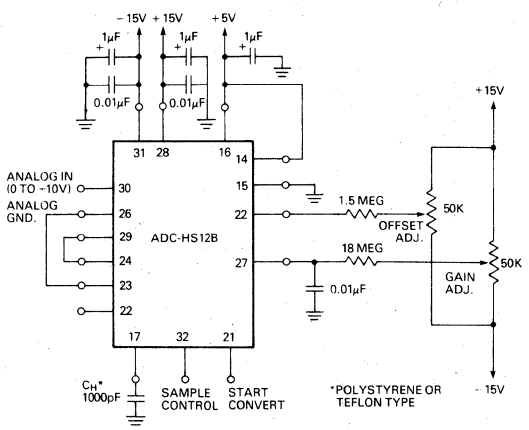
THESE CONVERTERS ARE COVERED BY GSA CONTRACT

TIMING DIAGRAM FOR ADC-HS12B

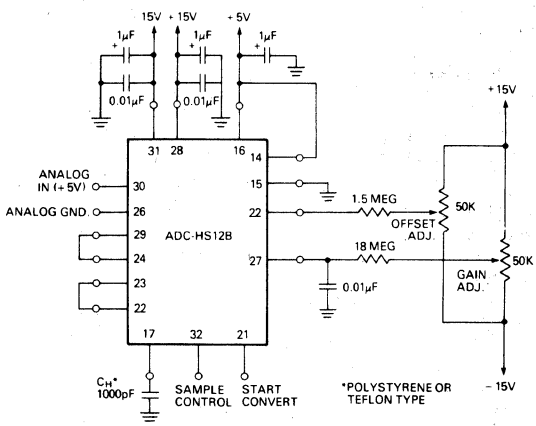


NOTE: TRIGGER, SAMPLE CONTROL, AND START CONVERT PULSES MUST BE EXTERNALLY GENERATED

UNIPOLAR OPERATION, 0 TO +10V



BIPOLAR OPERATION, ±5V



CODING TABLES

UNIPOLAR OPERATION

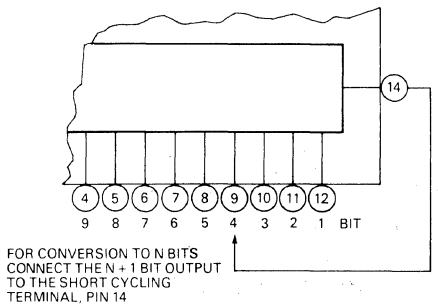
INPUT RANGE		COMP. BINARY CODING		
0 TO +10V	0 TO +5V	MSB		LSB
+9.9976V	+4.9988V	0000	0000	0000
+8.7500	+4.3750	0001	1111	1111
+7.5000	+3.7500	0011	1111	1111
+5.0000	+2.5000	0111	1111	1111
+2.5000	+1.2500	1011	1111	1111
+1.2500	+0.6250	1101	1111	1111
+0.0024	+0.0012	1111	1111	1110
0.0000	0.0000	1111	1111	1111

BIPOLAR OPERATION

INPUT VOLTAGE RANGE			COMP. OFFSET BINARY		
±10V	±5V	±2.5V	MSB		LSB
+9.9951V	+4.9976V	+2.4988V	0000	0000	0000
+7.5000	+3.7500	+1.8750	0001	1111	1111
+5.0000	+2.5000	+1.2500	0011	1111	1111
0.0000	0.0000	0.0000	0111	1111	1111
−5.0000	−2.5000	−1.2500	1011	1111	1111
−7.5000	−3.7500	−1.8750	1101	1111	1111
−9.9951	−4.9976	−2.4988	1111	1111	1110
−10.0000	−5.0000	−2.5000	1111	1111	1111

CONNECTIONS AND CALIBRATION

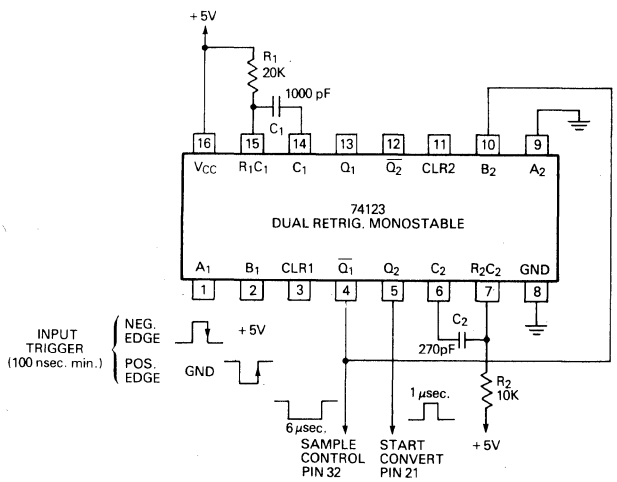
SHORT CYCLE OPERATION



PIN 14 CONNECTION

RES. (BITS)	PIN 14 TO	CONV. TIME
1	PIN 11	0.7 μsec.
2	PIN 10	1.3
3	PIN 9	2.0
4	PIN 8	2.6
5	PIN 7	3.3
6	PIN 6	4.0
7	PIN 5	4.6
8	PIN 4	5.3
9	PIN 3	6.0
10	PIN 2	6.6
11	PIN 1	7.3
12	PIN 16	9.0

RECOMMENDED CIRCUIT FOR GENERATING SAMPLE CONTROL AND START CONVERT PULSES



INPUT CONNECTIONS

INPUT VOLTAGE RANGE	CONNECT THESE PINS TOGETHER		
0 to +5V	29 & 24	22 & 25	23 & 26
0 to +10V	29 & 24	—	23 & 26
±2.5V	29 & 24	22 & 25	23 & 22
±5V	29 & 24	—	23 & 22
±10V	29 & 25	—	23 & 22

CALIBRATION PROCEDURE

1. Connect the ADC-HS12B as shown in one of the connection diagrams. The sample-hold and A/D converter should be timed as shown in the timing diagram. The trigger pulse should be applied at a rate of 70 kHz or less and should be 100 nsec. minimum width.
2. **Zero and Offset Adjustments**
   Apply a precision voltage reference source between the selected analog input and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (zero +½ LSB) or the bipolar offset adjustment (−FS+½ LSB). Adjust the trimming potentiometer so that the output code flickers equally betwen 1111 1111 1111 and 1111 1111 1110.
3. **Full Scale Adjustment**
   Change the output of the precision voltage reference source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+FS−1½ LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 0000 0000 0001 and 0000 0000 0000.

CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 TO +5V	ZERO GAIN	+0.6 mV +4.9982V
0 TO +10V	ZERO GAIN	+1.2 mV +9.9963V
BIPOLAR RANGE		
±2.5V	OFFSET GAIN	−2.4994V +2.4982V
±5V	OFFSET GAIN	−4.9988V +4.9963V
±10V	OFFSET GAIN	−9.9976V +9.9927V

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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

12-Bit Microelectronic Analog-to-Digital Converters ADC-HX, ADC-HZ Series

FEATURES

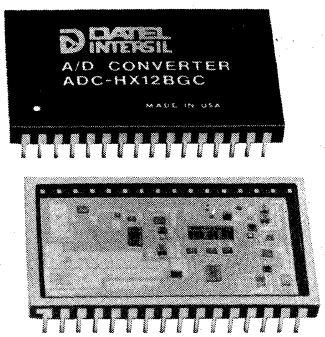
- 12 Bits Resolution
- 8 or 20 μSec. Conversions
- 5 Input Ranges
- Internal Hi Z Buffer
- Short Cycle Operation

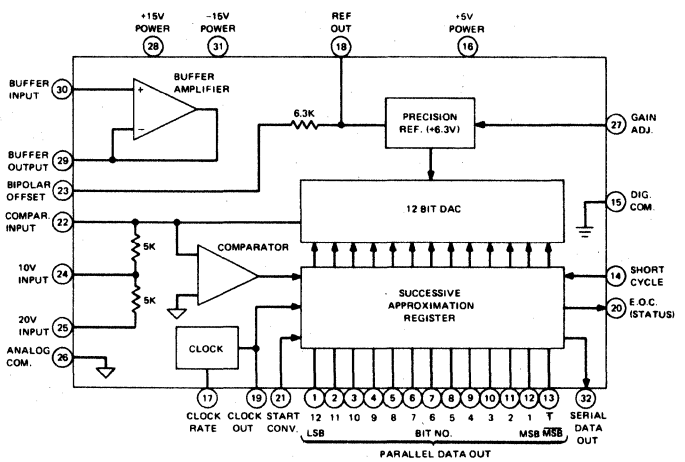
GENERAL DESCRIPTION

The ADC-HX12B and ADC-HZ12B are self-contained, high performance, 12 bit A/D converters manufactured with thin-film hybrid technology. They use the successive approximation conversion technique to achieve a 12 bit conversion in 20 and 8 microseconds respectively. Five input voltage ranges are programmable by external pin connection: 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V. An internal buffer amplifier is also provided for applications where 100 megohm input impedance is required.

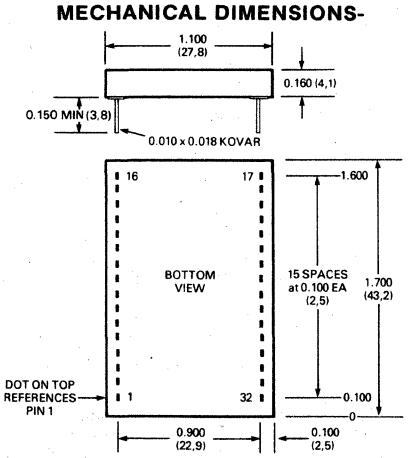
These converters utilize a fast 12 bit DAC consisting of tightly matched monolithic quad current switches, a stable nichrome thin-film resistor network, and a precision zener reference source. The circuit also contains a fast monolithic comparator, a monolithic 12 bit successive approximation register, a clock, and a monolithic buffer amplifier. The thin-film resistor network is functionally trimmed by a laser to precisely set the 8-4-2-1 current weighting in the quad current switches. The close tracking of the thin-film resistor and quad current switches result in a differential nonlinearity tempco of only ±2ppm/°C. Gain tempco is ±20ppm/°C maximum.

Both models have identical operation except for conversion speed. They can be short-cycled to give faster conversion in lower resolution applications. Use of the internal buffer amplifier increases conversion time by 3μsec., the settling time of the amplifier. Output coding is complementary binary, complementary offset binary, or complementary 2's complement. Serial data is also brought out. The package is a 32 pin ceramic case. Eight different models are offered covering the operating temperature ranges of 0 to 70°C, –25 to +85°C, and –55 to +100°C.





MECHANICAL DIMENSIONS-



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	17	CLOCK RATE
2	BIT 11 OUT	18	REF. OUT
3	BIT 10 OUT	19	CLOCK OUT
4	BIT 9 OUT	20	E.O.C. (STATUS)
5	BIT 8 OUT	21	START CONVERT
6	BIT 7 OUT	22	COMPAR. INPUT
7	BIT 6 OUT	23	BIPOLAR OFFSET
8	BIT 5 OUT	24	10V INPUT
9	BIT 4 OUT	25	20V INPUT
10	BIT 3 OUT	26	ANALOG COM.
11	BIT 2 OUT	27	GAIN ADJUST
12	BIT 1 OUT (MSB)	28	+15V POWER
13	BIT 1 OUT ($\overline{\text{MSB}}$)	29	BUFFER OUTPUT
14	SHORT CYCLE	30	BUFFER INPUT
15	DIGITAL COM.	31	-15V POWER
16	+5V POWER	32	SERIAL OUTPUT

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SPECIFICATIONS, ADC-HX12B, ADC-HZ12B
(Typical at 25°C, ±15V and +5V supplies unless otherwise noted)

	ADC-HX12B	ADC-HZ12B
INPUTS		
Analog Input Ranges, unipolar	0 to +5V, 0 to +10V FS	
Analog Input Ranges, bipolar	±2.5V, ±5V, ±10V FS	
Input Impedance	2.5K (0 to +5V, ±2.5V) 5K (0 to +10V, ±5V) 10K (±10V)	
Input Impedance with Buffer	100 Megohms	
Input Bias Current of Buffer	125nA typ., 250nA max.	
Input Overvoltage	±15V	
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 100nsec. min. Rise and fall times <30nsec. Logic "1" to "0" transition resets converter and initiates next conversion. Loading: 1 TTL load	
OUTPUTS[1]		
Parallel Output Data	12 parallel lines of data held until next conversion command. V_{OUT} ("0") ≤ +0.4V V_{OUT} ("1") ≥ +2.4V	
Coding, unipolar	Complementary Binary	
Coding, bipolar	Complementary Offset Binary Complementary Two's Complement	
Serial Output Data	NRZ successive decision pulses out, MSB first. Compl. Binary or Compl. Offset Binary Coding	
End of Conversion (Status)	Conversion status signal. Output is logic "1" during reset and conversion and logic "0" when conversion complete.	
Clock Output	Train of positive going +5V 100nsec. pulses. 600 kHz for ADC-HX12B and 1.5MHz for ADC-HZ12B (pin 17 grounded).	
PERFORMANCE		
Resolution	12 bits (1 part in 4096)	
Nonlinearity	±1/2 LSB max.	
Differential Nonlinearity	±1/2 LSB max.	
Gain Error, before adjustment	±0.1%	
Zero Error, unipolar, before adj.	±.05% of FSR[3]	
Offset Error, bipolar, before adj.	±0.1% of FSR[3]	
Temp. Coeff. of Gain	±20ppm/°C max.	
Temp. Coeff. of Zero, unipolar	±5ppm/°C of FSR max.[3]	
Temp. Coeff. of Offset, bipolar	±10ppm/°C of FSR max.[3]	
Diff. Nonlinearity Tempco	±2ppm/°C of FSR[3]	
No Missing Codes	Over oper. temp. range	
Conversion Time[2], 12 bits	20 µsec. max.	8.0 µsec. max.
10 bits[4]	15 µsec. max.	6.0 µsec. max.
8 bits[4]	10 µsec. max.	4.0 µsec. max.
Buffer Settling Time, 10V step	3.0 µsec. to .01%	
Power Supply Rejection	.002% / % Supply max.	
POWER REQUIREMENT		
	+15VDC ±0.5V @ 55mA −15VDC ±0.5V @ 45mA + 5VDC ±0.25 @ 100mA	
PHYSICAL-ENVIRONMENTAL		
Operating Temperature Range	0 to 70°C, -25 to +85°C, or -55 to +100°C	
Storage Temperature Range	-65°C to +150°C	
Package Size	1.700 x 1.100 x 0.160 inches	
Package Type	32 pin ceramic	
Pins	0.010 x 0.018 inch Kovar	
Weight	0.5 oz. (14g.)	

NOTES:

1. All digital outputs can drive 2 TTL loads.
2. Without buffer amplifier used. ADC-HZ12B may require external adjustment of clock rate.
3. FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input.
4. Short cycled operation.

TECHNICAL NOTES

1. It is recommended that the ±15V power input pins both be bypassed to ground with a .01µF ceramic capacitor in parallel with a 1µF electrolytic capacitor and the +5V power input pin be bypassed to ground with a 10µF electrolytic capacitor as shown in the connection diagrams. In addition, pin 27 should be bypassed to ground with a .01µF ceramic capacitor. These precautions will assure noise free operation of the converter.
2. Digital Common (pin 15) and Analog Common (pin 26) are not connected together internally, and therefore must be connected as directly as possible externally. It is recommended that a ground plane be run underneath the case between the two commons. Analog ground and ±15V power ground should be run to pin 26 whereas digital ground and +5V ground should be run to pin 15.
3. External adjustment of zero or offset and gain are provided for by trimming potentiometers connected as shown in the connection diagrams. The potentiometer values can be between 10K and 100K ohms and should be 100ppm/°C cermet types (such as Datel-Intersil's TP series). The adjustment range is ±0.2% of FSR for zero or offset and ±0.3% for gain. The trimming pots should be located as close as possible to the converter to avoid noise pickup. In some cases, for example 8 bit short-cycled operation, external adjustment may not be necessary.
4. Short cycled operation results in shorter conversion times where the conversion can be truncated to less than 12 bits. This is done by connecting pin 14 to the output bit following the last bit desired. For example for an 8 bit conversion, pin 14 is connected to bit 9 output. Maximum conversion times are given for short-cycled conversions of 8 or 10 bits. In these two cases the clock rate is also speeded up by connecting the clock rate adjust (pin 17) to +5V (10 bits) or +15V (8 bits). The clock rate should not be arbitrarily speeded up to exceed the maximum conversion rate at a given resolution, however, or missing codes will result.
5. Note that output coding is complementary coding. For unipolar operation it is complementary binary and for bipolar operation it is complementary offset binary or complementary 2's complement. In cases where bipolar coding of offset binary or 2's complement is required, this can be achieved by inverting the analog input to the converter (using an op amp connected for gain of −1.0000). The converter is then calibrated so that −FS analog input gives an output code of 0000 0000 0000, and +FS−1LSB gives 1111 1111 1111.
6. These converters dissipate approximately 2 watts of power. The case to ambient thermal resistance is approximately 25°C per watt. For ambient temperatures above 50°C, care should be taken not to restrict air circulation in the vicinity of the converter.

ORDERING INFORMATION

MODEL	TEMP. RANGE	SEAL
ADC-HX12BGC	0 to 70C	EPOXY
ADC-HX12BMC	0 to 70C	HERM.
ADC-HX12BMR	-25 to +85C	HERM.
ADC-HX12BMM	-55 to +100C	HERM.
ADC-HZ12BGC	0 to 70C	EPOXY
ADC-HZ12BMC	0 to 70C	HERM.
ADC-HZ12BMR	-25 to +85C	HERM.
ADC-HZ12BMM	-55 to +100C	HERM.

Mating Socket: DILS-2 (2/converter)

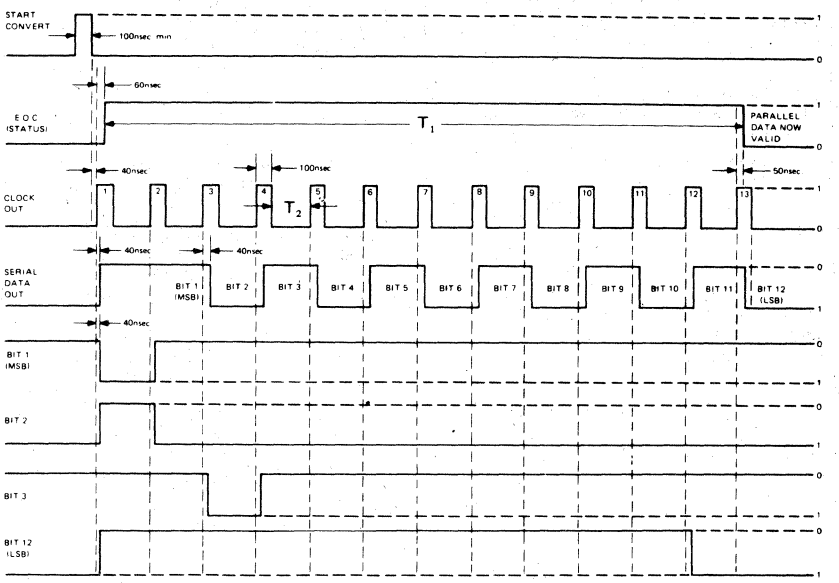
Trimming Potentiometers: TP2K, TP5K, TP10K, TP20K, TP50K or TP100K

THESE CONVERTERS ARE COVERED UNDER GSA CONTRACT

TIMING AND CONNECTION DIAGRAMS

7. These converters can be operated with an external clock. To accomplish this, a negative pulse train is applied to START CONVERT (Pin 21). The rate of the external clock must be lower than the rate of the internal clock as adjusted (see clock rate adjustment diagram) for the converter resolution selected. The pulse width of the external clock should be between 100 nsec. and 300 nsec. Each N bit conversion cycle requires a pulse train of N + 1 clock pulses for completion, e.g., an 8 bit conversion requires 9 clock pulses for completion. A continuous pulse train may be used for consecutive conversions, resulting in an N bit conversion every N + 1 pulses, or the E.O.C. output may be used to gate a continuous pulse train for single conversions.

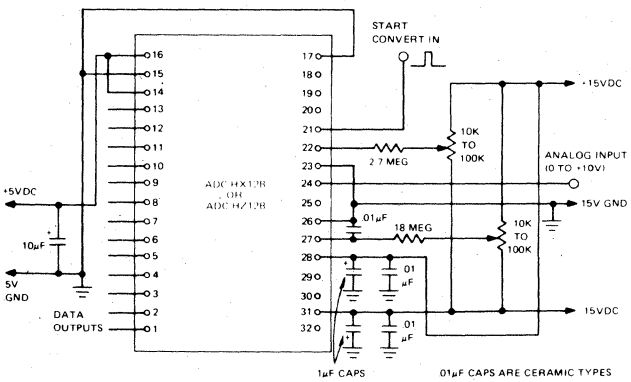
TIMING DIAGRAM FOR ADC-HX12B, ADC-HZ12B OUTPUT: 010101010101



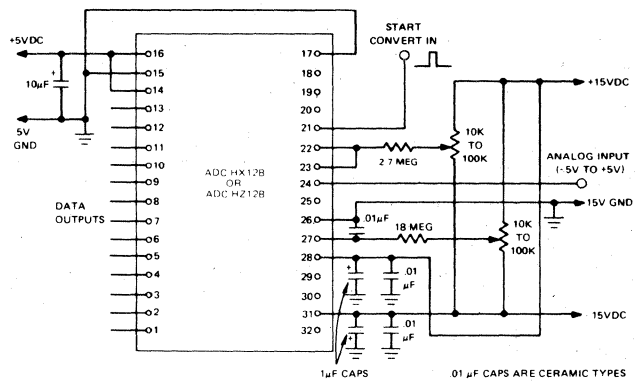
TIMING DIAGRAM OPERATING PERIODS

	ADC-HX12B	ADC-HZ12B
T_1	20 μsec.	8.0 μsec.
T_2	1.56 μsec.	0.56 μsec.

UNIPOLAR OPERATION, 0 TO +10V



BIPOLAR OPERATION, -5V TO +5V



CODING TABLES

UNIPOLAR OPERATION

INPUT RANGE		COMP. BINARY CODING
0 TO +10V	0 TO +5V	MSB LSB
+9.9976V	+4.9988V	0000 0000 0000
+8.7500	+4.3750	0001 1111 1111
+7.5000	+3.7500	0011 1111 1111
+5.0000	+2.5000	0111 1111 1111
+2.5000	+1.2500	1011 1111 1111
+1.2500	+0.6250	1101 1111 1111
+0.0024	+0.0012	1111 1111 1110
0.0000	0.0000	1111 1111 1111

BIPOLAR OPERATION

INPUT VOLTAGE RANGE			COMP. OFFSET BINARY		COMP. TWO'S COMPLEMENT	
±10V	±5V	±2.5V	MSB LSB		MSB LSB	
+9.9951V	+4.9976V	+2.4988V	0000 0000 0000		1000 0000 0000	
+7.5000	+3.7500	+1.8750	0001 1111 1111		1001 1111 1111	
+5.0000	+2.5000	+1.2500	0011 1111 1111		1011 1111 1111	
0.0000	0.0000	0.0000	0111 1111 1111		1111 1111 1111	
−5.0000	−2.5000	−1.2500	1011 1111 1111		0011 1111 1111	
−7.5000	−3.7500	−1.8750	1101 1111 1111		0101 1111 1111	
−9.9951	−4.9976	−2.4988	1111 1111 1110		0111 1111 1110	
−10.0000	−5.0000	−2.5000	1111 1111 1111		0111 1111 1111	

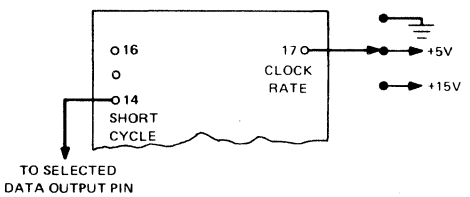
CONNECTIONS AND CALIBRATION

INPUT CONNECTIONS

INPUT VOLT. RANGE	WITHOUT BUFFER			WITH BUFFER			
	INPUT PIN	CONNECT THESE PINS TOGETHER		INPUT PIN	CONNECT THESE PINS TOGETHER		
0 TO +5V	24	22 & 25	23 & 26	30	22 & 25	23 & 26	29 & 24
0 TO +10V	24	–	23 & 26	30	–	23 & 26	29 & 24
±2.5V	24	22 & 25	23 & 22	30	22 & 25	23 & 22	29 & 24
±5V	24	–	23 & 22	30	–	23 & 22	29 & 24
±10V	25	–	23 & 22	30	–	23 & 22	29 & 25

SHORT CYCLE OPERATION

CONNECTIONS



8, 10, & 12 BIT CONVERSION

RESOLUTION	12 BITS	10 BITS	8 BITS
ADC-HX12B CONV. TIME	20 µsec.	15 µsec.	10 µsec.
ADC-HZ12B CONV. TIME	8 µsec.	6 µsec.	4 µsec.
CONNECT THESE	17 & 15	17 & 16	17 & 28
PINS TOGETHER	14 & 16	14 & 2	14 & 4

CLOCK RATE VS. VOLTAGE

PIN 17 VOLTAGE	CLOCK RATE	
	ADC-HX12B	ADC-HZ12B
0V	600 kHz	1.5MHz
+5V	720 kHz	1.8MHz
+15V	880 kHz	2.2MHz

PIN 14 CONNECTION

RES. (BITS)	PIN 14 TO
1	PIN 11
2	PIN 10
3	PIN 9
4	PIN 8
5	PIN 7
6	PIN 6

RES. (BITS)	PIN 14 TO
7	PIN 5
8	PIN 4
9	PIN 3
10	PIN 2
11	PIN 1
12	PIN 16

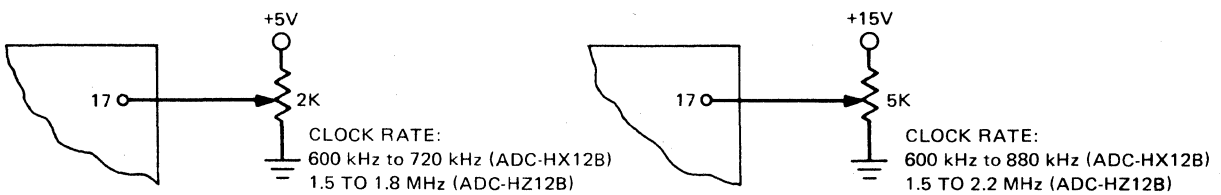
CALIBRATION PROCEDURE

1. Connect converter as shown in the Standard Connection diagrams. Use the Input Connection Table for the desired input voltage range and input impedance. Apply Start Convert pulses of 100 nsec. minimum duration to pin 21. The spacing of the pulses should be no less than the maximum conversion time.
2. **Zero and Offset Adjustments**
   Apply a precision voltage reference source between the selected analog input and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (zero +½ LSB) or the bipolar offset adjustment (–FS+½ LSB). Adjust the trimming potentiometer so that the output code flickers equally between 1111 1111 1111 and 1111 1111 1110.
3. **Full Scale Adjustment**
   Change the output of the precision voltage reference source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+FS–1½ LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 0000 0000 0001 and 0000 0000 0000.

CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 TO +5V	ZERO	+0.6 mV
	GAIN	+4.9982V
0 TO +10V	ZERO	+1.2 mV
	GAIN	+9.9963V
BIPOLAR RANGE		
±2.5V	OFFSET	–2.4994V
	GAIN	+2.4982V
±5V	OFFSET	–4.9988V
	GAIN	+4.9963V
±10V	OFFSET	–9.9976V
	GAIN	+9.9927V

CLOCK RATE ADJUSTMENT



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Ultra-Fast 8 Bit A/D Converters
Models ADC-815, ADC-825

FEATURES

- **8 Bits Resolution**
- **600 nsec. or 1 μsec. Conversion Time**
- **6 Input Ranges**
- **Parallel or Serial Outputs**
- **Logic-Controlled Bipolar Offset**
- **No Calibration Required**

GENERAL DESCRIPTION

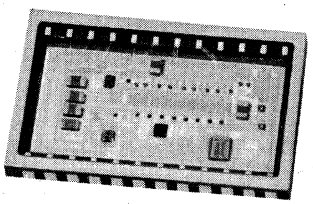
Datel-Intersil's ADC-815 and ADC-825 are very high speed 8 bit successive approximation A/D converters in miniature hybrid form. Both models have identical specifications except for conversion time. The ADC-825 has a maximum conversion time of 1 μsec., while the ultra-fast ADC-815 accomplishes an 8 bit conversion in only 600 nsec., maximum.

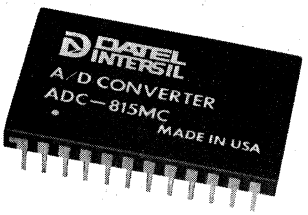
These converters feature six analog input voltage ranges: 0 to +5V, 0 to +10V, 0 to +20V, ±2.5V, ±5V and ±10V. Selection of input ranges is accomplished by simple external pin connection. Unipolar or bipolar operating mode is selected by a digital control applied to the bipolar offset input. Operation of these devices is further simplified by complete functional laser trimming, resulting in a factory-trimmed converter that requires no external adjustments.

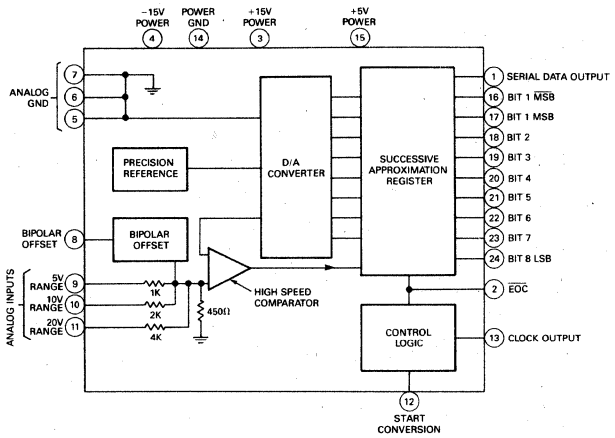
Each converter is a functionally complete unit requiring a minimum of passive external components for operation, and is packaged in a miniature, hermetically sealed 24-pin ceramic DIP.

Output data is available in parallel or serial form by external pin connection. Parallel output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. Output coding in the parallel mode is accomplished by connection to either the MSB output or the $\overline{\text{MSB}}$ output. Serial output data is coded as straight binary for unipolar operation or offset binary for bipolar operation.

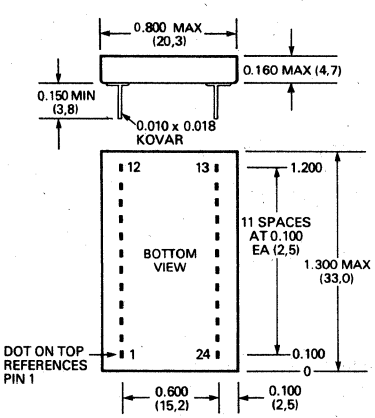
Additional specifications shared by both models include maximum nonlinearity of ±½ LSB, differential nonlinearity of ±½ LSB maximum, gain tempco of 20 ppm/°C maximum, power supply rejection of ±0.02%/% supply maximum, and long term stability of ±0.05%/year. Both models require ±15V and 5V supplies, and are available in different versions for operating temperature ranges of 0 to +70°C, −25 to +85°C, or −55 to +125°C.







MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	SERIAL DATA OUTPUT	13	CLOCK OUTPUT
2	$\overline{\text{EOC}}$	14	POWER GROUND
3	+15V POWER IN	15	+5V POWER IN
4	−15V POWER IN	16	BIT 1 OUT ($\overline{\text{MSB}}$)
5	ANALOG GROUND	17	BIT 1 OUT (MSB)
6	ANALOG GROUND	18	BIT 2 OUT
7	ANALOG GROUND	19	BIT 3 OUT
8	BIPOLAR OFFSET	20	BIT 4 OUT
9	ANALOG INPUT, 5V RANGE	21	BIT 5 OUT
10	ANALOG INPUT, 10V RANGE	22	BIT 6 OUT
11	ANALOG INPUT, 20V RANGE	23	BIT 7 OUT
12	START CONVERSION	24	BIT 8 OUT (LSB)

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, ADC-815, ADC-825

Typical at 25°C, ±15 VDC and +5 VDC supplies, unless otherwise noted.

	ADC-815	ADC-825
MAXIMUM RATINGS		
Positive Supply	+18V	
Negative Supply	−18V	
Logic Supply	+7V	
Digital Inputs	+5.5V	
Analog Inputs	±25V	
INPUTS		
Analog Input Ranges,[1] Unipolar	0 to +5V, 0 to +10V, 0 to +20V,	
Bipolar	±2.5V, ±5V, ±10V	
Input Impedance, 5V Range	1.34K	
10V Range	2.3K	
20V Range	4.27K	
Start Conversion	+2V min. to +5.5V max. Positive Pulse 50 nsec min. duration, 10 nsec. typ. rise and fall times. Positive Going Edge resets outputs to 011 . . . 1 and sets $\overline{EOC}$ HI. Negative going edge initiates conversion. Loading: 2 TTL loads.	
Bipolar Offset	Hold HI (+2.0V to +5V) for bipolar operation, hold LO ≤ +0.8V) for unipolar operation.	
OUTPUTS		
Parallel Output Data	9 parallel lines (8 binary bits plus $\overline{MSB}$) V_{OUT} ("0") ≤ +0.4V V_{OUT} ("1") ≥ +2.4V Loading: 4 TTL loads	
Serial Output Data	NRZ format successive Decision pulse output at internal clock rate generated during conversion. MSB first. Loading: 4 TTL loads	
Coding, Unipolar	Straight Binary	
Bipolar	Offset Binary, Two's Complement	
$\overline{EOC}$	Conversion Status Signal. HI ≥ +2.4V during conversion and reset periods. LO≤ +0.4V when conv. complete. Loading: 4 TTL loads	
Clock Output	Internal clock pulse train of negative going pulses[2] from +5V to 0V. Loading: 6 TTL loads	
PERFORMANCE		
Conversion Time[3], max.	600 nsec.	1 μsec.
Resolution	8 bits	
Nonlinearity	±½ LSB max.	
Differential Nonlinearity	±½ LSB max.	
Gain Error	±½ LSB max.	
Zero Error	±½ LSB max.	
Gain Tempco, 0°C to +70°C[4]	±20 ppm of FSR/°C max.[5]	
Zero Drift	±100 μV/°C max.	
Offset Tempco	±10 ppm of FSR/°C max.[5]	
Long Term Stability	±0.02%/year	
No Missing Codes	Over Operating Temp. Range	
POWER REQUIREMENT		
Analog Supply	+15V ±0.5V @ 35 mA max. −15V ±0.05V @ 15 mA max.	
Logic Supply	+5V ±0.25V @ 100 mA max.	
Power Dissipation	1.25W max.	
PHYSICAL ENVIRONMENTAL		
Operating Temp. Range, BMC	0°C to +70°C	
BMR	−25°C to +85°C	
BMM	−55°C to +125°C	
Storage Temp. Range	−65°C to +150°C	
Package Type	24 pin Ceramic DIP	
Pins	0.010 × 0.018 inch Kovar	
Weight	0.2 oz. (6 g)	

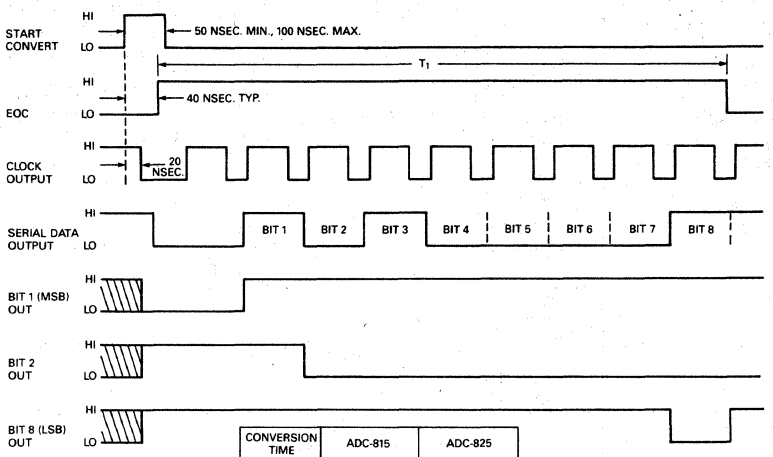
NOTES: 1. Unused analog inputs must be grounded.
2. At 15.9 MHz for the ADC-815, 9.52 MHz for the ADC-825.
3. The conversion time temperature coefficient for these converters is 0.15%/°C. This tempco is positive from 0°C to +125°C and from 0°C to −55°C Maximum conversion time is specified at 25° C. Max. Conversion Time for "M M" version is 700 nsec. at 25° C.
4. Doubles outside this temperature range. 5. FSR is Full Scale Range.

TECHNICAL NOTES

1. The high operating speed of these converters requires that good high frequency board layout techniques be used. Leads from data outputs should be kept as short as possible, output leads longer than 1 inch (2.5 cm) require the use of an output register. Use of a ground plane is particularly important with high speed data converters as it reduces high frequency noise and aids in decoupling analog signals from digital signals. Ground loop problems are avoided by connecting all grounds on the board to the ground plane. The basic configuration of the ground plane directly below the ADC-815 or ADC-825 is shown in the ground plane layout diagram. This layout should be modified after selection of analog input range to include unused analog inputs.
2. Analog input leads should be as short and direct as possible. The use of shielded cable as an analog input lead will ensure isolation of analog signals from environmental interference. Unused analog inputs should be grounded.
3. For applications of the ADC-815 or ADC-825 that require an input buffer amplifier, an amplifier should be selected with particular attention to its high speed performance and low output impedance.
4. Analog and digital supplies are internally bypassed to ground with .01 μF capacitors; however, it is recommended that the +15V, −15V and +5V supplies be additionally bypassed externally with 1 μF electrolytic capacitors as shown in the connection diagrams.
5. For bipolar operation the bipolar offset input (pin 8) is held at logic HI (+2.0V to +5V); for unipolar operation pin 8 is held at logic LO (0V to +0.8V).
6. In the bipolar mode, two's complement output coding is available by using the MSB output (pin 16); offset binary coding is obtained by using the MSB output (pin 17). Unipolar operation requires use of the MSB output (pin 17) to achieve straight binary output coding.
7. Serial output data is available at pin 1 in standard NRZ format with the MSB appearing first. Coding is straight binary for unipolar operation or offset binary for bipolar operation. Synchronization of serial output data is achieved by use of the clock output (pin 13). Each data bit is valid when the clock output is HIGH and appears in succession from the MSB at the second clock LOW to HIGH transition to the LSB at the ninth clock LOW to HIGH transition.
8. Applications of these converters that require the use of a sample-hold may be satisfied by Datel-Intersil's model SHM-HU, an ultra-fast hybrid unit featuring 25 nsec acquisition time and a ±2.5V input range.
9. These converters have a maximum power dissipation of 1.25W. The case-to-ambient thermal resistance for this package is approximately 33°C per watt. For operation in ambient temperatures exceeding 83°C, airflow of at least 400 linear feet per minute is recommended.

APPLICATIONS

TIMING DIAGRAM FOR ADC-815, ADC-825
OUTPUT: 10100001



CONVERSION TIME	ADC-815	ADC-825
T_1 =	600 NSEC. MAX.	1.0 μSEC. MAX.

CODING TABLES

UNIPOLAR OPERATION

UNIPOLAR SCALE	OUTPUT CODING* STRAIGHT BINARY	ANALOG INPUT 0 to +5V	0 to +10V	0 to +20V
F.S. - 1 LSB	1111 1111	+4.980V	+9.961V	+19.922V
¾ F.S.	1100 0000	+3.750V	+7.500V	+15.000V
½ F.S.	1000 0000	+2.500V	+5.000V	+10.000V
¼ F.S.	0100 0000	+1.250V	+2.500V	+5.000V
1 LSB	0000 0001	+0.020V	+0.039V	+0.078V
0	0000 0000	0.000V	0.000V	0.000V

*FOR PARALLEL OR SERIAL OUTPUT DATA

BIPOLAR OPERATION

BIPOLAR SCALE	OUTPUT CODING OFFSET BINARY[1]	OUTPUT CODING TWO'S COMPLEMENT[2]	INPUT VOLTAGE RANGE ±2.5V	±5V	±10V
+F.S.−1 LSB	1111 1111	0111 1111	+2.480V	+4.961V	+9.922V
+½ F.S.	1100 0000	0100 0000	+1.250V	+2.500V	+5.000V
+1 LSB	1000 0001	0000 0001	+0.020V	+0.039V	+0.078V
0	1000 0000	0000 0000	0.000V	0.000V	0.000V
−½ F.S.	0100 0000	1100 0000	−1.250V	−2.500V	−5.000V
−F.S.+1 LSB	0000 0001	1000 0001	−2.480V	−4.961V	+9.922V
−F.S.	0000 0000	1000 0000	−2.500V	−5.000V	+10.000V

NOTES: 1. FOR PARALLEL OR SERIAL OUTPUT DATA
2. FOR PARALLEL OUTPUT DATA ONLY

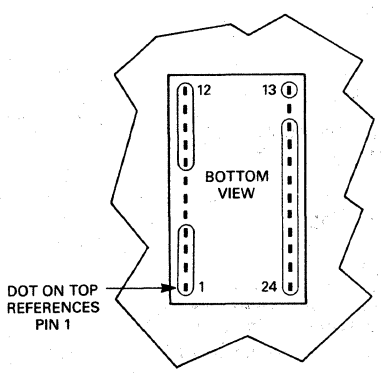
ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	SEAL
ADC-815MC	0°C to +70°C	Hermetic
ADC-815MR	−25°C to +85°C	Hermetic
ADC-815MM	−55°C to +125°C	Hermetic
ADC-825MC	0°C to +70°C	Hermetic
ADC-825MR	−25°C to +85°C	Hermetic
ADC-825MM	−55°C to +125°C	Hermetic

Mating Socket: DILS-3 (24-pin socket)
Trimming Potentiometers: TP-100

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

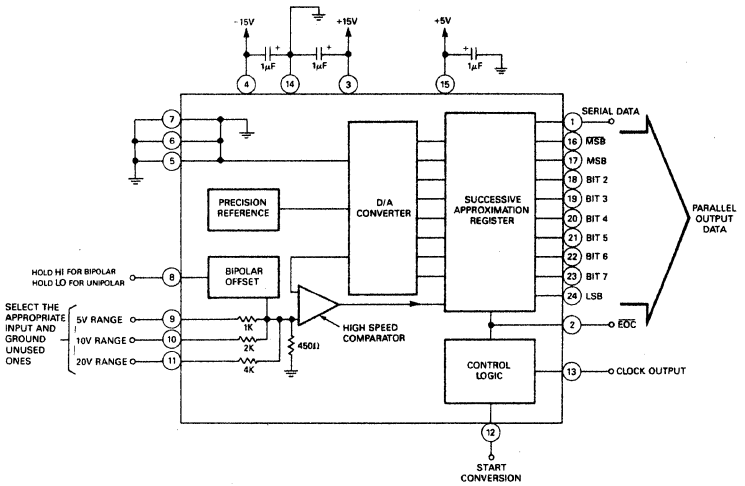
BASIC GROUND PLANE LAYOUT



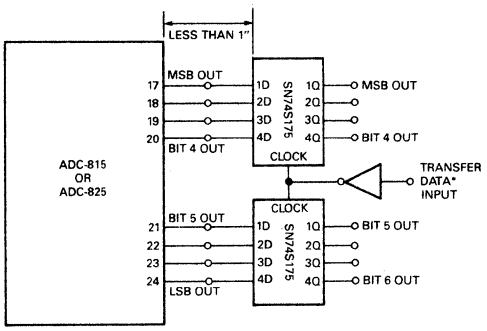
THIS BASIC GROUND PLANE LAYOUT SHOULD BE MODIFIED BEFORE IMPLEMENTATION TO INCLUDE UNUSED ANALOG INPUTS.

CONNECTIONS

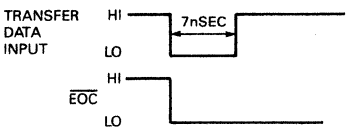
UNIPOLAR/BIPOLAR OPERATIONS



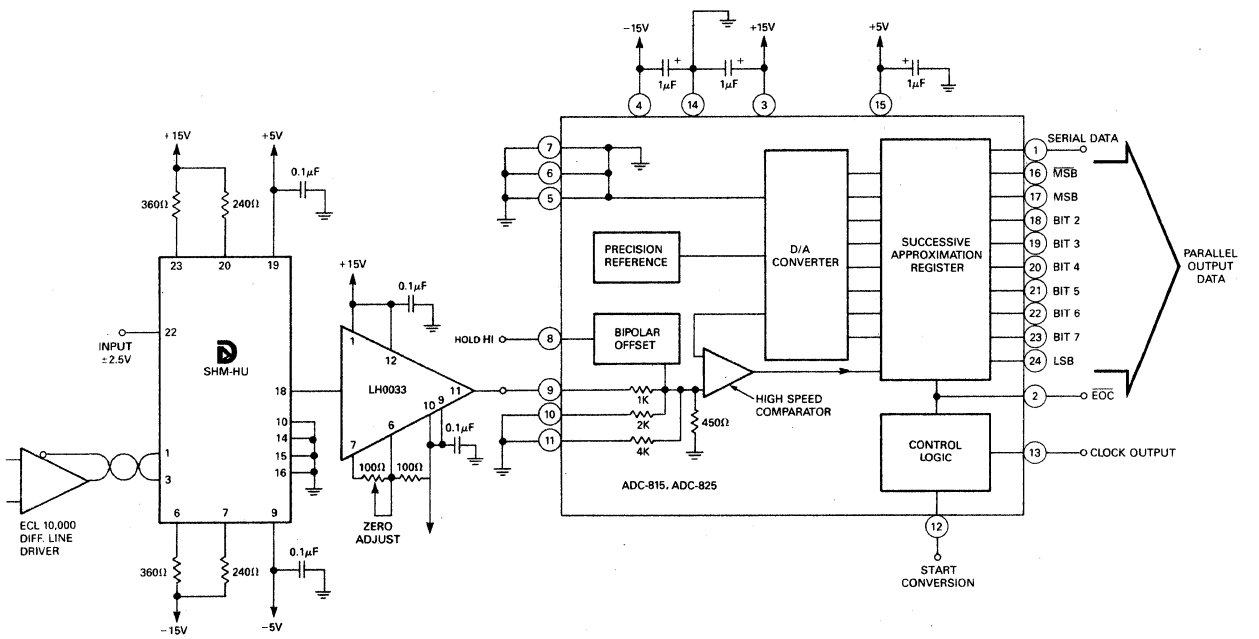
OUTPUT REGISTER



*TRANSFER DATA INPUT MAY BE TIED TO $\overline{EOC}$ OUTPUT (PIN 2) OR EXTERNALLY DRIVEN. WHEN TRANSFER DATA IS EXTERNALLY CONTROLLED TIMING OF CONTROL PULSE SHOULD BE AS SHOWN



ADC-815/SHM-HU CONNECTION



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PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Ultra-Fast 10-Bit A/D Converters ADC-816, ADC-826

FEATURES

- **10 Bits Resolution**
- **800 nsec or 1.4 μsec Conversion Time**
- **6 Input Ranges**
- **Unipolar and Bipolar Operation**
- **Programmable Output Coding**

GENERAL DESCRIPTION

Datel-Intersil's ADC-816 and ADC-826 are very high speed 10 bit successive approximation A/D converters, realized as miniature thin-film hybrids. Both models have identical specifications except for conversion time. The ADC-826 has a maximum conversion time of 1.4 μsec. The ultra-fast ADC-816 offers a maximum conversion time of only 800 nsec, making this the fastest 10 bit A/D converter of any hybrid, monolithic, or modular unit currently available. Please note that these conversion times are specified as maximum at *full rated operating temperature!*

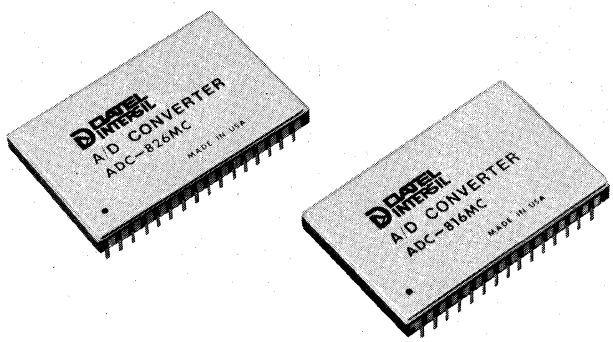
These converters feature six analog input voltage ranges: 0 to −5V, 0 to −10V, 0 to −20V, ±2.5V, ±5V and ±10V. Selection of input range is accomplished by simple external pin connection.

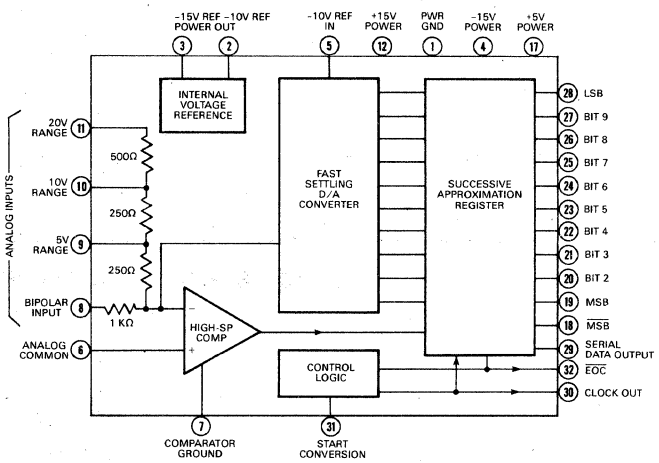
Output data is available in parallel or serial form by external connection. Data is coded as straight binary for unipolar operation and as either offset binary or Two's complement for bipolar operation. Two's complement is available in the parallel output mode only and is selected by pin connection.

Specifications shared by both models include maximum nonlinearity of ±½ LSB and differential nonlinearity of ±½ LSB maximum.

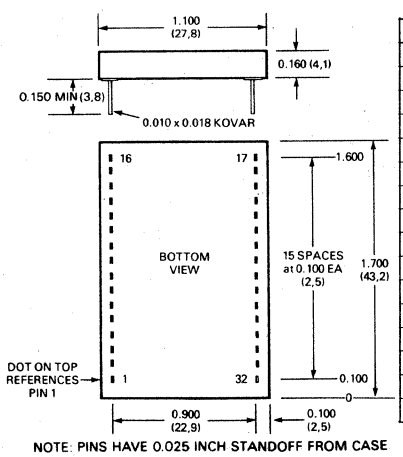
These converters are functionally complete units requiring a minimum of passive external components for operation. Each unit is composed of a high speed comparator, an ultra-fast settling D/A converter, a precision voltage reference, successive approximation register, clock generator and control logic circuits. The combination of unique design and the latest hybrid fabrication technology allows this level of performance to be achieved in a miniature hermetically sealed 32 pin ceramic DIP package.

Both models require ±15 VDC and +5V supplies, and are available in versions for the 0 to 70°C, −25 to +85°C or −55 to +125°C operating temperature ranges. For information on versions certified to MIL-STD-883 Class B, contact the factory.





MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	POWER COM	17	+5V POWER
2	REF OUT	18	$\overline{\text{MSB}}$ 1
3	REF POWER	19	MSB 1
4	−15V POWER	20	BIT 2
5	REF IN	21	BIT 3
6	SIG COM	22	BIT 4
7	COMPARATOR COM.	23	BIT 5
8	BIP IN	24	BIT 6
9	+5V IN	25	BIT 7
10	+10V IN	26	BIT 8
11	+20V IN	27	BIT 9
12	+15V POWER	28	LSB 10
13	NC	29	SERIAL DATA OUT
14	NC	30	CLOCK OUT
15	NC	31	START
16	NC	32	$\overline{\text{EOC}}$

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SPECIFICATIONS ADC-816, ADC-826
(Typical at +25°C, ±15 VDC and +5 VDC supplies, unless otherwise noted)

MAXIMUM RATINGS

Positive Supply, pin 12	+16VDC
Negative Supply, pin 4	−16 VDC
Logic Supply, pin 17	+7 VDC
Logic Inputs	+7 VDC
Analog Inputs	± Twice selected analog input range

INPUTS

Analog Input Ranges	**, unipolar**[1]	0 to −5V, 0 to −10V, 0 to −20V
	, bipolar	±2.5V, ±5V, ±10V
	, reference	−9.5V to −10.5V
Input Impedance[2]	**, 5V range**	250Ω
	, 10V range	500Ω
	, 20 V range	1 KΩ
	, bipolar input	1 KΩ
	, reference (pin 5)	2 KΩ
Start conversion		2V min to 5.5V max. positive pulse with duration of 50 nsec min. Rise and fall times typ. 10 nsec. Logic "1" resets converter, Logic "0" initiates conversion. Loading: 1 TTL Load.

OUTPUTS

Parallel Output Data	11 Parallel lines of data (10 binary bits + $\overline{\text{MSB}}$) held until next conversion command. Vout ("0") ≤ +0.4V, Vout ("1") ≥ +2.4V. Loading: 2 TTL loads
Coding[3] **, unipolar**	Straight Binary
, bipolar[4]	Offset Binary, Two's Complement
Serial Output Data	NRZ successive decision pulses out, MSB first, at internal clock frequency Loading: 4 TTL Loads.
End of Conversion ($\overline{\text{EOC}}$)	Conversion Status Signal. Output is logic HI during reset and conversion, LO when conversion is complete. Loading: 4 TTL Loads.
Clock Output	Train of positive going, 0 to +5V, 30 nsec pulses.
Clock Frequency, ADC-816MC/MR[5]	12.5 MHz
, ADC-826MC/MR/MM	6.6 MHz
Reference Output, Voltage	−10.00V ± 0.02V
, Current	0 to +20 mA (sink only)
, Impedance	10 Ω max. fo ≤ 10 MHz

PERFORMANCE

Resolution	10 Bits
Conversion Time[6] **, ADC-816MC/MR**[7]	800 nsec max.
, ADC-826MC/MR/MM	1.4 μsec max.
Nonlinearity	±½ LSB max.
Differential Nonlinearity[8]	±½ LSB max.
Gain Error[9]**, before adjustment, unipolar**	±0.3% of FSR[10], max.
, bipolar	±0.2% of FSR max.
Zero Error, before adjustment, unipolar	±0.2% of FSR max.
Offset Error, before adjustment, bipolar	±0.1% of FSR max.
Gain Tempco[11] **, unipolar**	±37 ppm/°C max.
, bipolar	±28 ppm/°C max.
Zero Tempco , unipolar	±12 ppm/°C max.
, bipolar	±23 ppm/°C max.
Conversion Time Tempco	±0.1%/°C
Reference Output Tempco	±20 ppm/°C max.
Power Supply Rejection	Effectively infinite for rated supplies
No missing codes	Over operating Temp. Range

POWER REQUIREMENTS

Analog Supply , pin 12	+15V ±0.1V @ 106mA max.
, pin 4	−15V ±0.5V @ 20mA max.
Reference Supply, pin 3	−15V ±0.5V @ 34mA max.
Logic Supply, pin 17	+5V ±0.25V @ 194mA max.
Power Dissipation	3.6W max.

PHYSICAL-ENVIRONMENTAL

Operating Temp. Range	**Suffix C**	0°C to +70°C
	Suffix R	−25°C to +85°C
	Suffix M	−55°C to +125°C
Storage Temperature Range		−65°C to +150°C
Package Type		32 pin hermetically sealed Ceramic DIP
Pins		0.010 × 0.018 inch gold plated Kovar
Weight		0.8 oz (23g)

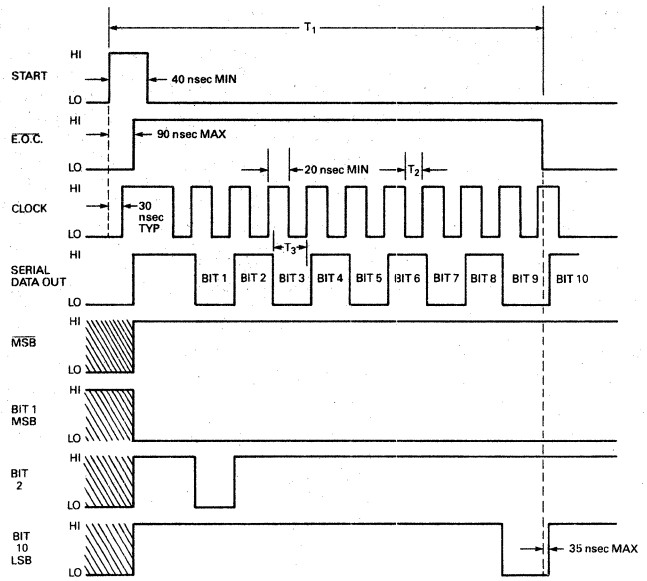
NOTES: 1. Bipolar input must be tied to ground.
2. Resistance tolerance is −30%, +50%, ±50 ppm/°C.
3. All coding is inverted analog.
4. Two's Complement Binary available for parallel output only.
5. Clock frequency for ADC-816MM is 10.5 MHz.
6. Max. conversion time is specified at full rated operating temp.
7. The ADC-816MM has a maximum conversion time of 975 nsec at full rated operating temperature.
8. Tested over full rated operating temperature range.
9. Includes Zero Error.
10. FSR is Full Scale Range.
11. Includes internal reference Tempco. Given as a maximum for 5V FSR, these values improve by 10% for 10V FSR, and by 20% for 20V FSR.

TECHNICAL NOTES

1. Use of good high frequency circuit board layout techniques is required for rated performance. The power common (pin 1) and comparator common (pin 7) are not connected internally, and therefore must be connected externally as directly as possible, through a low resistance, low inductance path. The signal common (pin 6) is connected to power common (pin 1) internally and so may be used as a signal sense line to reference the signal input. The extensive use of a ground plane for all common connections is highly recommended. Also, it is recommended that the analog and digital supplies, although they are internally bypassed with 0.033 μF capacitors, be additionally bypassed externally at the supply pins with 1 μF electrolytic capacitors.
2. The digital outputs are not buffered from their internal application and so are sensitive to unusual loading or long lines. Terminate these outputs with normal TTL inputs not more than 3 inches from the data output pin. Analog inputs must be non-reactive such that leads should be short and purely resistive. The reactive component of any analog input source, as seen at the analog input pin, should be less than 0.3% of the analog input resistance at that pin, for frequencies below 20 MHz.
3. Conversion time is measured from the rising edge of a 50 nsec start input pulse to the falling edge of the $\overline{\text{EOC}}$ output. The conversion time is factory set at +25°C for the ADC-816 MC/MR at 750 nsec, 875 nsec for the ADC-816MM, and 1.25 μsec for the ADC-826MC/MR/MM. The worst case conversion time at the maximum rated operating temperature is given as a maximum specification.
4. To use the internal reference the reference supply pin (pin 3) must be connected to the −15V supply. If the reference supply pin (pin 3) is disconnected or grounded, the internal reference will be disabled at a power saving of approximately 200 mW.
5. Serial output data is available in NRZ format successive decision pulses, MSB first, in straight binary or offset binary coding. Synchronization of the serial output data is achieved through the use of the clock output (pin 30). This same clock output also controls the output register such that at the rising edge of the output clock the previous data bit may be clocked out, however, there will be no clock edge to clock out the LSB. A Serial DATA Recovery circuit is diagrammed on the applications page that will correct this.
6. These converters have a case to ambient thermal resistance of 22°C per watt. At temperatures above +70°C an air flow of at least 400 linear feet per minute is recommended. To operate at elevated temperatures it is recommended that the converter be mounted directly to the circuit board (without the use of a mounting socket) and that good thermal contact be established between the case bottom and the circuit board ground plane by use of a silicone thermal joint compound such as Wakefield Type 120 or equivalent.
7. Applications of these converters that require the use of a sample-hold may be satisfied by Datel-Intersil's model SHM-HU, an ultra-fast hybrid unit featuring 25 nsec acquisition time and a ±2.5V input range.

APPLICATIONS

TIMING DIAGRAM FOR ADC-816, ADC-826



MODEL	T_1	T_2	T_3
ADC-816 MC/MR	800 n sec	60 n sec	65 n sec MAX
ADC-816 MM	975 n sec	75 n sec	85 n sec MAX
ADC-826 MC/MR/MM	1.4 n sec	130 n sec	135 n sec MAX

CODING TABLES

UNIPOLAR OPERATION

INPUT RANGE			STRAIGHT BINARY		
0 to -20V	0 to -10V	0 to -5V	MSB		LSB
-19.9805	-9.9902	-4.9951	1111	11	1111
-17.5000	-8.7500	-4.3750	1110	00	0000
-15.0000	-7.5000	-3.7500	1100	00	0000
-10.0000	-5.0000	-2.5000	1000	00	0000
-5.0000	-2.5000	-1.2500	0100	00	0000
-2.5000	-1.2500	-0.6250	0010	00	0000
-0.0198	-0.0098	-0.0049	0000	00	0001
0.0000	0.0000	0.0000	0000	00	0000

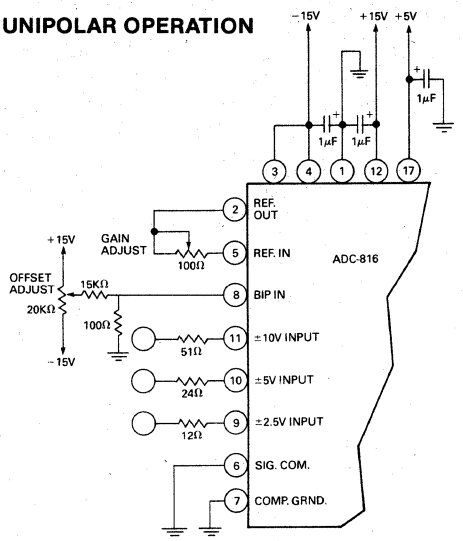
BINARY OPERATION

INPUT RANGE			OFFSET BINARY			TWO'S COMPLEMENT		
±10V	±5V	±2.5V	MSB		LSB	MSB		LSB
-9.9805	-4.9902	-2.4951	1111	11	1111	0111	11	1111
-7.5000	-3.7500	-1.8750	1110	00	0000	0110	00	0000
-5.0000	-2.5000	-1.2500	1100	00	0000	0100	00	0000
0.0000	0.0000	0.0000	1000	00	0000	1100	00	0000
+5.0000	+2.5000	+1.2500	0100	00	0000	1100	00	0000
+7.5000	+3.7500	+1.8750	0010	00	0000	1010	00	0000
+9.9805	+4.9902	+2.4951	0000	00	0001	1000	00	0001
+10.0000	+5.0000	+2.5000	0000	00	0000	1000	00	0000

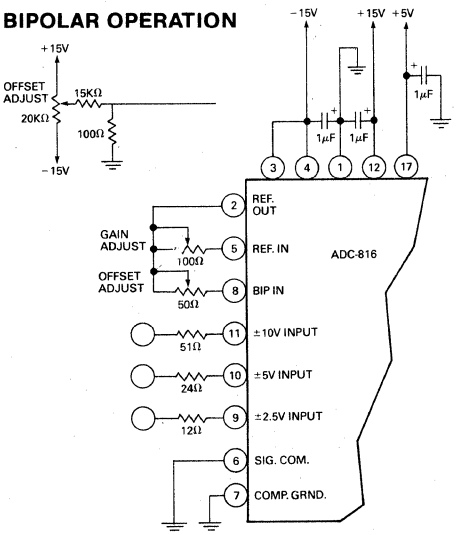
ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
ADC-816MC	0°C To +70°C
ADC-816MR	-25°C To +85°C
ADC-816MM	-55°C To +125°C
ADC-826MC	0°C To +70°C
ADC-826MR	-25°C To +85°C
ADC-826MM	-55°C To +125°C
Mating Socket	DILS-2 (2/converter)
Trimming Potentiometers	TP20K, TP100, TP50

UNIPOLAR OPERATION



BIPOLAR OPERATION



CALIBRATION PROCEDURE

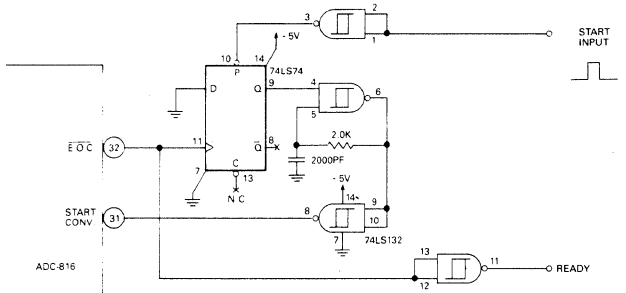
1. Connect the converter as shown in the applicable connections diagram. A trigger pulse of between 50 nsec and 100 nsec is applied to the start conversion input (pin 31) at the rate of 200KHz.
2. **Zero and Offset Adjustments**
   Apply a precision voltage reference source between the appropriate input for the selected full scale range and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (0-1/2 LSB) or the bipolar offset adjustment (+FS-1/2 LSB). Adjust the appropriate trimming potentiometer so that the output code flickers equally between X0000 00000 and X0000 00001. The MSB, indicated by X will be 0 for straight binary and offset binary coding or 1 for two's complement output coding.
3. **Full Scale Adjustment**
   Set the output of the voltage reference source used in step 2 to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (-FS + 1 1/2 LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between X1111 11111 and X1111 11110. The MSB, indicated by X, will be 1 for straight binary and offset binary coding or coding or 0 for two's complement output coding.

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 To -5V	Zero	-2.4mV
	Gain	-4.9927V
0 To -10V	Zero	-4.9mV
	Gain	-9.9854V
0 to -20V	Zero	-9.8mV
	Gain	-19.9707.V

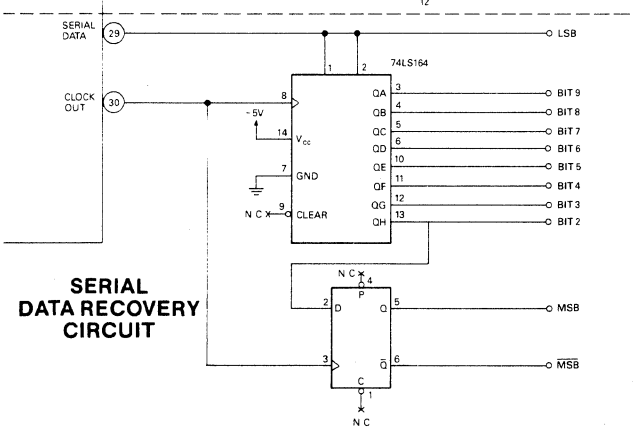
BIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
±2.5V	Offset	±2.4975V
	Gain	-2.4927V
±5V	Offset	±4.9951V
	Gain	-4.9854V
±10V	Offset	±9.9902V
	Gain	-9.9707V

PERFORMANCE DATA

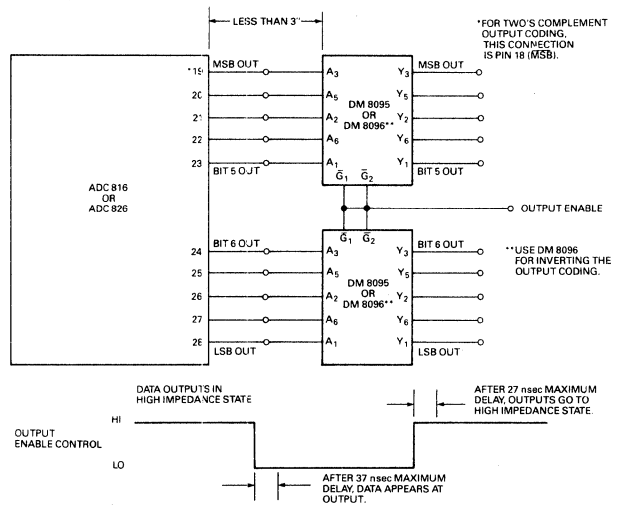
UNCONDITIONAL/START CIRCUIT



SERIAL DATA RECOVERY CIRCUIT



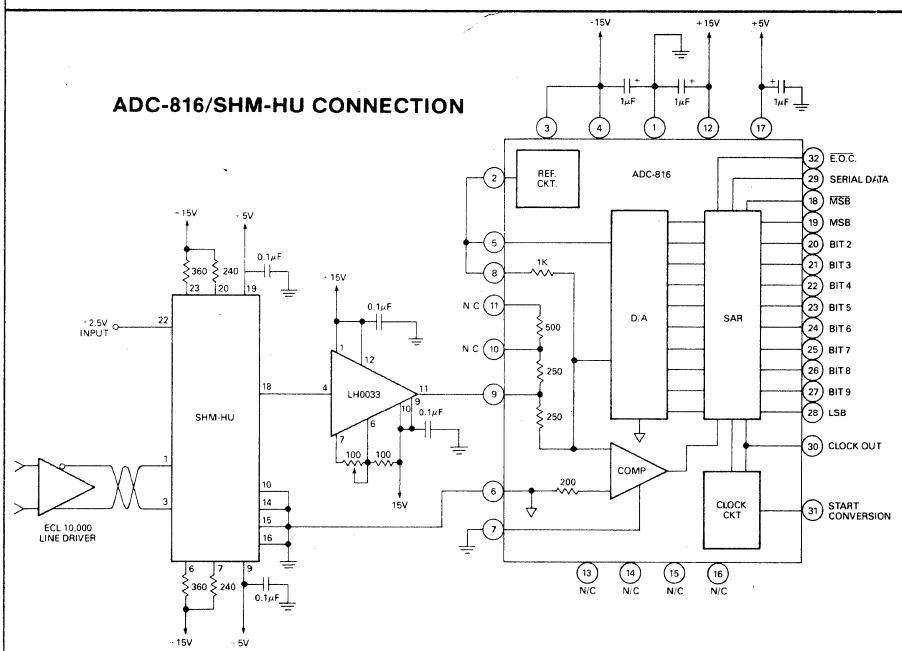
HIGH SPEED THREE-STATE OUTPUT BUFFER GROUND PLANE LAYOUT



The Unconditional Start Circuit, shown for the ADC-816/826 insures the initiation of a conversion cycle upon the application of one start pulse of 40 nsec minimum pulse width regardless of converter status.

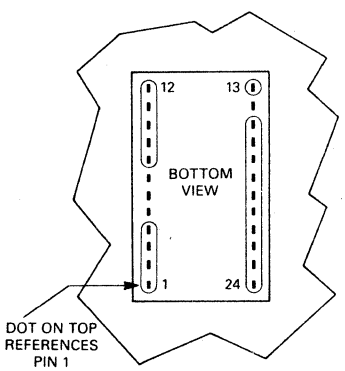
The serial data output of the ADC-816/826 is converted into parallel form, with the addition of an $\overline{MSB}$ output, by the Serial Data Recovery circuit. Users should refer to technical note No. 2 on the loading of the ADC-816/826 digital outputs when using these circuits.

ADC-816/SHM-HU CONNECTION



When the ADC-816 or ADC-826 is configured as shown here with Datel-Intersil's SHM-HU hybrid sample-hold, a ±2.5V input step can be acquired to 0.1% accuracy in 30 nsec and held to within 40 μV while the A/D conversion takes place. Use of the SHM-HU reduces the time over which the input signal is averaged to a few nanoseconds (an A/D converter without a sample-hold averages the analog input signal over the total conversion time of the A/D).

GROUND PLANE LAYOUT



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PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Ultra-Fast 12 Bit A/D Converters Models ADC-817, ADC-827

FEATURES

- **12 Bit Resolution**
- **2 μsec or 3 μsec Conversion Times**
- **Unipolar & Bipolar Operation**
- **Short Cycle Operating Capability**
- **5 Programmable Input Ranges**
- **Parallel or Serial Data Output**

GENERAL DESCRIPTION

The ADC-817 and ADC-827 are high-speed successive approximation A/D converters in miniature hybrid form. Both Models have identical specifications except for conversion times. The ADC-827 has a maximum conversion time of 3 μsec while the ultra-fast ADC-817 accomplishes a 12 bit conversion in only 2.0 μsec., maximum.

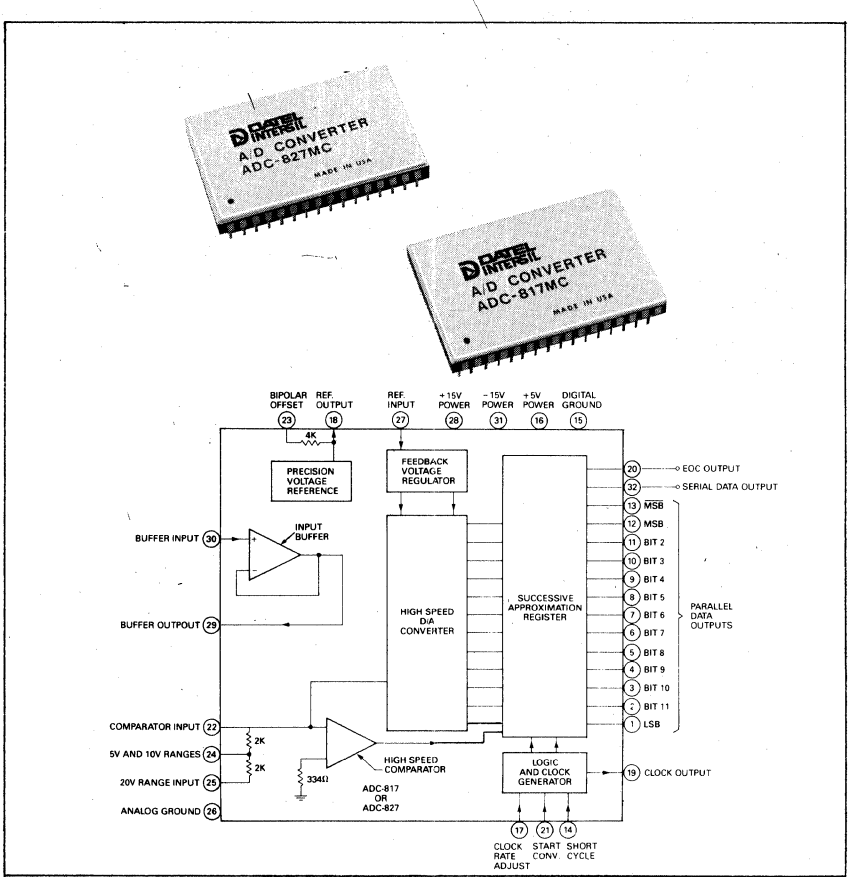
These converters feature five analog input voltage ranges: 0 to −5V, 0 to −10V, ±2.5V, ±5V, and ±10V. Selection of input range is accomplished by simple external pin connection. Both devices provide a user-selectable, fast settling precision input buffer with an input impedance of 100 MΩ, allowing them to be driven directly from a high impedance source. The input buffer may be bypassed for maximum speed applications with low impedance sources such as a sample and hold.

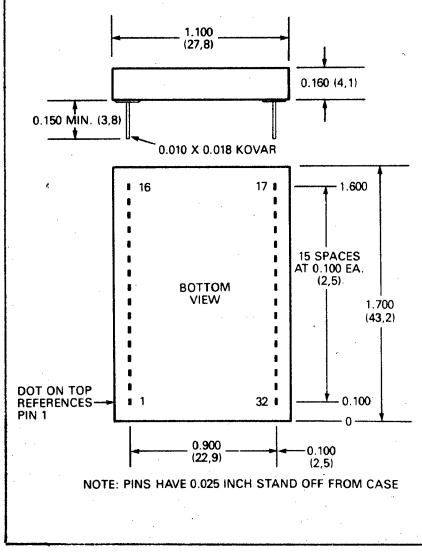
Output data is available in parallel or serial form by external connection. Data is coded as straight binary for unipolar operation and as either offset binary or two's complement for bipolar operation. Two's complement coding is available in the parallel output mode only, and is selected by pin connection.

Specifications shared by both models include maximum nonlinearity of ±1/2 LSB, differential nonlinearity of ±1/2 LSB maximum, gain tempco of 25 ppm/°C maximum, and a power supply rejection of ±0.01%/% supply maximum.

These converters are functionally complete units requiring a minimum of passive external components for operation. Each unit is composed of a fast settling precision input buffer, a high speed comparator, an ultra-fast settling D/A converter, a precision voltage reference, successive approximation register, clock generator and control logic circuits. The combination of unique design and the latest hybrid fabrication technology allows this level of performance to be achieved in a miniature, hermetically sealed 32 pin ceramic DIP package.

Both models require ±15 VDC and +5V supplies, and are available in versions for the 0 to +70° C, −25 to +85° C or −25 to +125° C operating temperature ranges. For information on versions certified to MIL-STD-883 Class B, contact the factory.





NOTE: PINS HAVE 0.025 INCH STAND OFF FROM CASE

ADC-817, 827 INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	BIT 12 OUT (LSB)
2	BIT 11 OUT
3	BIT 10 OUT
4	BIT 9 OUT
5	BIT 8 OUT
6	BIT 7 OUT
7	BIT 6 OUT
8	BIT 5 OUT
9	BIT 4 OUT
10	BIT 3 OUT
11	BIT 2 OUT
12	BIT 1 OUT (MSB)
13	$\overline{\text{BIT 1 OUT (MSB)}}$
14	SHORT CYCLE
15	DIGITAL GROUND
16	+5V POWER

PIN	FUNCTION
17	CLOCK RATE
18	REFERENCE OUT
19	CLOCK OUT
20	EOC OUT
21	START CONVERSION
22	COMPARATOR IN
23	BIPOLAR OFFSET
24	10V INPUT RANGE
25	20V INPUT RANGE
26	ANALOG GROUND
27	REFERENCE OUT
28	+15V POWER
29	BUFFER OUT
30	BUFFER IN
31	−15V POWER
32	SERIAL OUT

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SPECIFICATIONS, ADC-817, ADC-827

Typical at 25°C, ±15V supplies, unless otherwise noted.

	ADC-817	ADC-827
MAXIMUM RATINGS		
Positive Supply	+18V	
Negative Supply	−18V	
Logic Supply	+7V	
Digital Inputs	+5.5V	
Analog Inputs	±20V	
Buffer Amplifier Input	±15V	
INPUTS		
Analog Input Ranges Unipolar	0 to −5V, 0 to −10V	
Bipolar	±2.5V, ±5V, ±10V	
Input Impedance 5V Ranges	1 KΩ	
10V Ranges	2 KΩ	
20V Ranges	4 KΩ	
Start Conversion	+2V min. to +5.5V max. Positive Pulse with duration of 50 nsec min. Logic "1" resets converter Logic "0" initiates conversion Loading: 2 TTL loads	
Buffer Amplifier Gain	+1	
Buffer Amplifier Input Voltage	±10.0V	
Buffer Amplifier Input Impedance	100 MΩ	
Buffer Amplifier Settling Time[1]	300 nsec	
OUTPUTS		
Parallel Output Data	13 parallel lines (12 binary bits plus $\overline{\text{MSB}}$) valid from negative going edge of EOC pulse to positive going edge of START CONVERSION pulse. V_{OUT} "0" ≤+0.4V V_{OUT} "1" ≥+2.4V Loading: 4 TTL loads	
Serial Output Data	NRZ format, successive decision pulse output at internal clock rate generated during conversion. MSB appears first. Loading: 4 TTL loads	
Coding, Unipolar[2]	Straight Binary	
Bipolar[3]	Offset Binary, Two's Complement[3]	
End of Conversion (EOC)	Conversion Status Signal V_{OUT} "0" ≤+0.4V for conversion complete V_{OUT} "1" ≥+2.4V for conversion in progress	
Clock Output	Negative going pulses from +5V to 0V, gated on during conversion Loading: 6 TTL loads	
PERFORMANCE		
Resolution	12 binary bits[4]	
Nonlinearity	±1/2 LSB max.	
Differential Nonlinearity	±1/2 LSB max.	
Diff. Nonlinearity Tempco	±5 ppm/° C max.	
Gain Tempco	±25 ppm/° C max.	
Zero Tempco, Unipolar	±150 μV/° C max.	
Offset Tempco, Bipolar	±15 ppm of FSR/° C max.[5]	
Power Supply Rejection	±0.01%/% Supply, max.	
Conversion Time Over Full Temp.	2.0 μsec max.	3.0 μsec max.
POWER REQUIREMENT		
Supply Voltage	+15V ±0.5V @ 50 mA max. −15V ±0.5V @ 25mA max. + 5V ±0.25V @ 150 mA max.	
Power Dissipation	1.9 W max.	
PHYSICAL-ENVIRONMENTAL		
Operating Temp. Range, BMC	0° C to +70° C	
BMR	−25° C to +85° C	
BMM	−55° C to +125° C	
Storage Temp. Range	−65° C to +125° C	
Package Type	32 pin hermetically sealed ceramic DIP	
Pins	0.010 × 0.018 inch Kovar	
Weight	0.42 oz. (12g)	

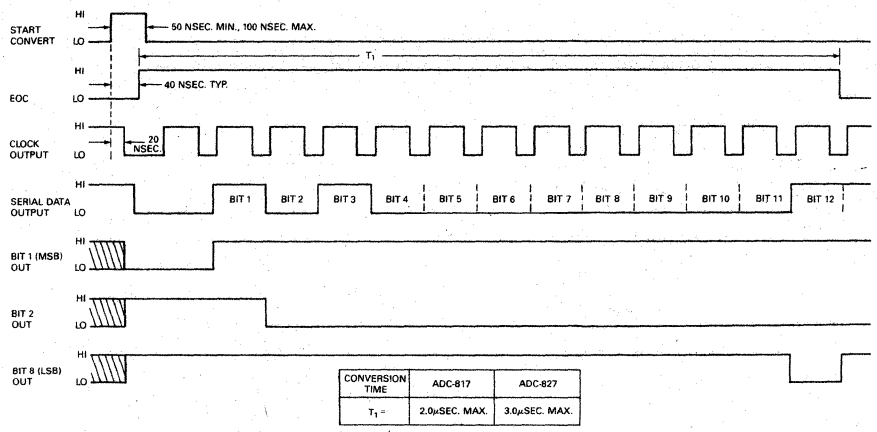
NOTES:
1. 10V step to 0.01%, 5V and 20V steps settle to 0.01% in 150 nsec and 800 nsec, respectively.
2. These converters operate with inverted analog, that is− F.S. +1 LSB is encoded as 1111 1111 1111 and +F.S. is encoded as 0000 0000 0000 (examples given are for offset binary coding).
3. Parallel output data only is available in offset binary (uses MSB out) or two's complement coding (uses $\overline{\text{MSB}}$ out).
4. May be reduced by connection of short cycle input as shown in the Short Cycle Operation table.
5. FSR is Full Scale Range

TECHNICAL NOTES

1. The high operating speed of these converters requires that good high frequency board layout techniques be used. Leads from data outputs should be kept as short as possible, output leads longer than 1 inch (2.5 cm) require the use of an output register. Ground loop problems are avoided by connecting all grounds on the board to the ground plane.
2. Analog input leads should be as short and direct as possible. The use of shielded cable as an analog input lead will ensure isolation of analog signals from environmental interference.
3. When the input buffer amplifier is used, a delay equal to its settling time must be allowed between input level change, such as multiplexer channel change, and the negative going edge of the START CONVERSION pulse. If the buffer is not required its input (pin 30) should be tied to analog ground (pin 26). This will prevent the unused amplifier from introducing noise into the converter. For applications in which the internal buffer is not used, the converter must be driven from a source with an extremely low input impedance.
4. Both analog and digital supplies should be bypassed to ground with 1 μF electrolytic capacitors in parallel with 0.1 μF ceramic capacitors as shown in the connections diagrams. Bypass capacitors should be located directly adjacent to, or on, each supply pin. The −10V reference output (pin 18) should be bypassed to ground with a 2.2 μF electrolytic capacitor mounted as previously indicated.
5. In the bipolar mode, two's complement output coding is available by using the $\overline{\text{MSB}}$ output (pin 13); offset binary coding is obtained by using the MSB output (pin 12). Unipolar operation requires use of the MSB output (pin 12) to achieve straight binary output coding.
6. Serial output data is available at pin 32 in standard NRZ format with the MSB appearing first. Coding is straight binary for unipolar operation or offset binary for bipolar operation. Synchronization of serial output data is achieved by use of the clock output (pin 19). Each data bit is valid when the clock output is HIGH and appears in succession from the MSB at the second clock LOW to HIGH transition to the LSB at the thirteenth clock LOW to HIGH transition.
7. Applications of these converters that require the use of a sample-hold may be satisfied by Datel-Intersil's model SHM-6, a high-speed hybrid unit featuring 1.0 μsec acquisition time, 0.01% accuracy, programmable gains from ±1 to ±10 and a ±10V output range.
8. These converters have a maximum power dissipation of 2.4W. The case-to-ambient thermal resistance for this package is approximately 28° C per watt. For operation in ambient temperatures exceeding 70° C, care must be taken to ensure free air circulation in the vicinity of the converter.
9. Clock rate control (pin 17) is left unconnected for operation at rated conversion speed. Connect to +5V to decrease conversion time by 50-75 nsec, or to ground to increase conversion time by 50-75 nsec.

APPLICATIONS

TIMING DIAGRAM FOR ADC-817, ADC-827
OUTPUT: 1010000000001



CONVERSION TIME	ADC-817	ADC-827
T_1 =	2.0μSEC. MAX.	3.0μSEC. MAX.

OUTPUT CODING

UNIPOLAR SCALE	ANALOG INPUT 0 to −10V RANGE	ANALOG INPUT 0 to −5V RANGE	STRAIGHT BINARY OUTPUT CODE
−FS + 1 LSB	−9.9976V	−4.9988V	1111 1111 1111
− 7/8 FS	−8.7500V	−4.3750V	1110 0000 0000
− 3/4 FS	−7.5000V	−3.7500V	1100 0000 0000
− 1/2 FS	−5.0000V	−2.5000V	1000 0000 0000
− 1/4 FS	−2.5000V	−1.2500V	0100 0000 0000
−1 LSB	−0.0024V	−0.0012V	0000 0000 0001
0	0.0000V	0.0000V	0000 0000 0000

BIPOLAR SCALE	ANALOG INPUT ±10V RANGE	±5V RANGE	±2.5V RANGE	DATA OUTPUT CODING OFFSET BINARY	TWO's COMPLEMENT
−FS + 1 LSB	−9.9951V	−4.9976V	−2.4988V	1111 1111 1111	0111 1111 1111
− 1/2 FS	−4.5000V	−2.5000V	−1.2500V	1100 0000 0000	0100 0000 0000
−1 LSB	−0.0049V	−0.0024V	−0.0012V	1000 0000 0001	0000 0000 0001
0	0.0000V	0.0000V	0.0000V	1000 0000 0000	0000 0000 0000
+ 1 LSB	+0.0049V	+0.0024V	+0.0012V	0000 0000 0001	1000 0000 0001
+ 1/2 FS	+4.5000V	+2.5000V	+1.2500V	0100 0000 0000	1100 0000 0000
+ FS − 1 LSB	+9.9951V	+4.9976V	+2.4988V	0000 0000 0001	1000 0000 0001
+FS	+10.0000V	+5.0000V	+2.5000V	0000 0000 0000	1000 0000 0000

SHORT CYCLE OPERATION

CONNECTION RES. (BITS)	CONNECTION PIN 14 TO	CONVERSION TIME ADC-817	CONVERSION TIME ADC-827
1	PIN 11	300 nsec	462 nsec
2	PIN 10	462 nsec	693 nsec
3	PIN 9	615 nsec	923 nsec
4	PIN 8	770 nsec	1.15 μsec
5	PIN 7	923 nsec	1.38 μsec
6	PIN 6	1.07 μsec	1.62 μsec
7	PIN 5	1.23 μsec	1.85 μsec
8	PIN 4	1.38 μsec	2.08 μsec
9	PIN 3	1.54 μsec	2.31 μsec
10	PIN 2	1.69 μsec	2.54 μsec
11	PIN 1	1.85 μsec	2.77 μsec
12	NC	2.0 μsec	3.0 μsec

ORDERING INFORMATION

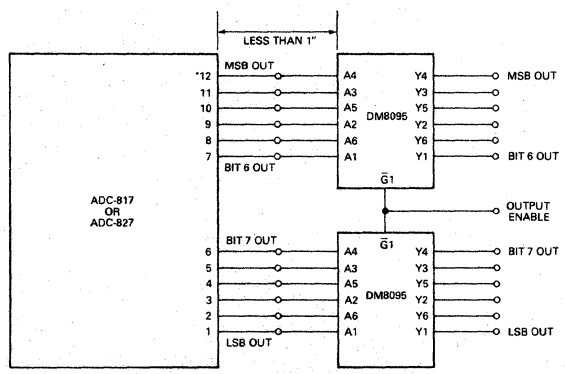
MODEL	OPERATING TEMP. RANGE	PRICE (1-24)
ADC-817MC	0 to +70° C	**$295.00**
ADC-817MR	−25 to +85° C	**$325.00**
ADC-817MM	−55 to +125° C	**$365.00**
ADC-827MC	0 to +70° C	**$195.00**
ADC-827MR	−25 to +85° C	**$225.00**
ADC-827MM	−55 to +125° C	**$275.00**

Mating Socket: DILS-2 (2 Required Per Converter) **$ 6.00 /Pr**

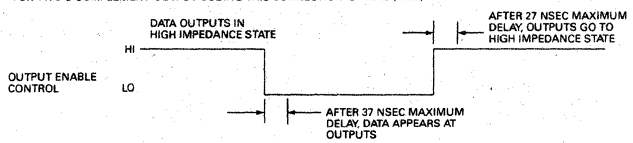
Trimming Potentiometer: TP-100 **$ 3.50**

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

HIGH SPEED THREE-STATE OUTPUT BUFFER

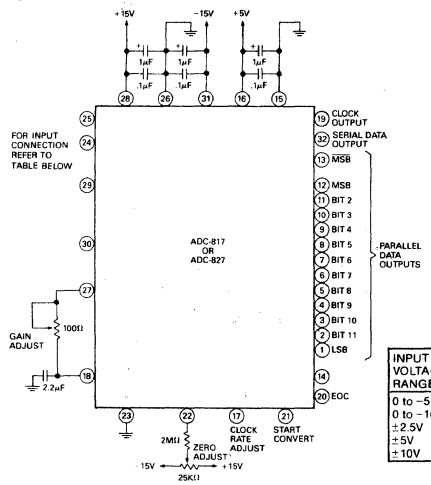


*FOR TWO'S COMPLEMENT OUTPUT CODING THIS CONNECTION IS PIN 13 ($\overline{MSB}$)

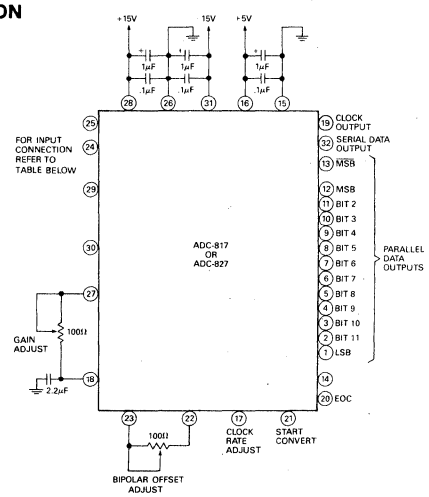


CONNECTIONS AND CALIBRATION

UNIPOLAR OPERATION



BIPOLAR OPERATION



INPUT CONNECTIONS

INPUT VOLTAGE RANGE	WITH INPUT BUFFER			WITHOUT INPUT BUFFER		
	INPUT PIN	CONNECT THESE PINS TOGETHER		INPUT PIN	CONNECT THESE PINS TOGETHER	
0 to −5V	30	29 to 24	22 to 25	24	22 to 25	30 to 26
0 to −10V	30	29 to 24	—	24	—	30 to 26
±2.5V	30	29 to 24	22 to 25	24	22 to 25	30 to 26
±5V	30	29 to 24	—	24	—	30 to 26
±10V	30	29 to 25	—	25	—	30 to 26

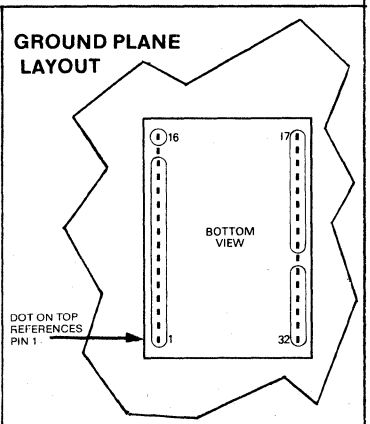
CALIBRATION PROCEDURE

1. Connect the converter as shown in the applicable connections diagram. A trigger pulse of between 50 nsec and 100 nsec is applied to the start conversion input (pin 21) at a rate of 200 kHz.
2. Zero and Offset Adjustments
   Apply a precision voltage reference source between the appropriate input for the selected full scale range and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (0 −1/2 LSB) or the bipolar offset adjustment (+FS − LSB). Adjust the appropriate trimming potentiometer so that the output code flickers equally between X000 0000 0000 and X000 0000 0001. The MSB, indicated by X, will be 0 for straight binary and offset binary output coding, or 1 for two's complement output coding.
3. Full Scale Adjustment
   Set the output of the voltage reference source used in step 2 to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (−F.S. +1½ LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between X111 1111 1111 and X111 1111 1110. The MSB, indicated by X, will be 1 for straight binary and offset binary output coding, or 0 for two's complement output coding.

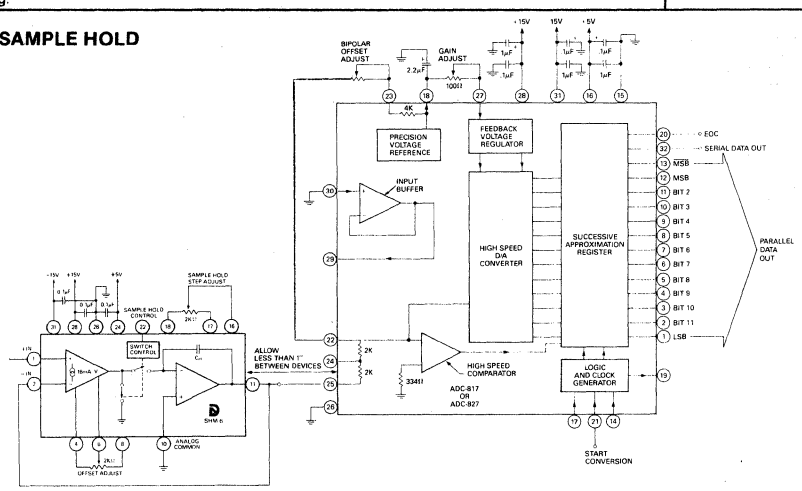
CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 TO −5V	ZERO	−0.6 mV
	GAIN	−4.9982V
0 TO −10V	ZERO	−1.2 mV
	GAIN	−9.9963V
BIPOLAR RANGE		
±2.5V	OFFSET	+2.4994V
	GAIN	−2.4982V
±5V	OFFSET	+4.9988V
	GAIN	−4.9963V
±10V	OFFSET	+9.9976V
	GAIN	−9.9927V

GROUND PLANE LAYOUT



ULTRA-FAST A/D WITH SAMPLE HOLD



When the ADC-817 or ADC-827 is configured as shown here with Datel-Intersil's SHM-6 hybrid sample-hold, a 10V input step can be acquired to 0.01% accuracy in 1 μsec and held to within 20 μV while the A/D conversion takes place. The SHM-6 can also be configured for inverting operation for applications with positive unipolar analog signals. Use of the SHM-6 reduces the time over which the input signal is averaged to a few nanoseconds (an A/D converter used without a samplehold averages the analog input signal over the total conversion time of the A/D).

DATEL INTERSIL
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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL. ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

Fast, Dual-Slope Analog-to-Digital Converters ADC-E Series

FEATURES

- **Differential or Single Ended Inputs**
- **Binary or BCD Coding**
- **Resolutions to 12 Bits or 3½ Digits**
- **6 Input Ranges Available**
- **100 Megohms Input Impedance**
- **80 dB Common Mode Rejection**

GENERAL DESCRIPTION

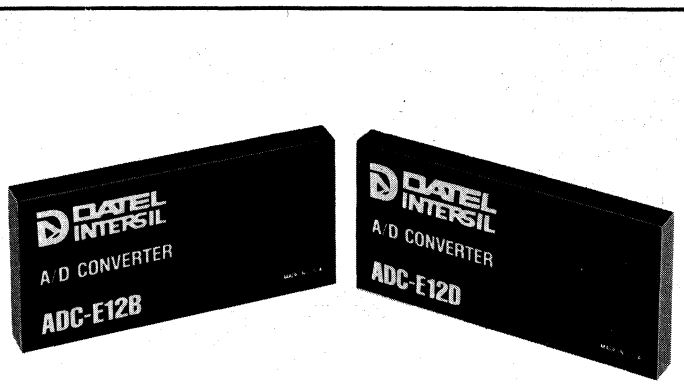
The ADC-E series devices are low cost, high accuracy analog-to-digital converters featuring differential inputs, high linearity and excellent noise immunity. These converters utilize a modified dual-slope conversion technique ideally suited for converting analog voltage levels such as transducer outputs at moderate speed. Models are available in 8, 10 and 12 binary bit resolutions with sign magnitude binary output coding, or in 2½ or 3½ BCD digit resolution with sign-magnitude BCD output coding.

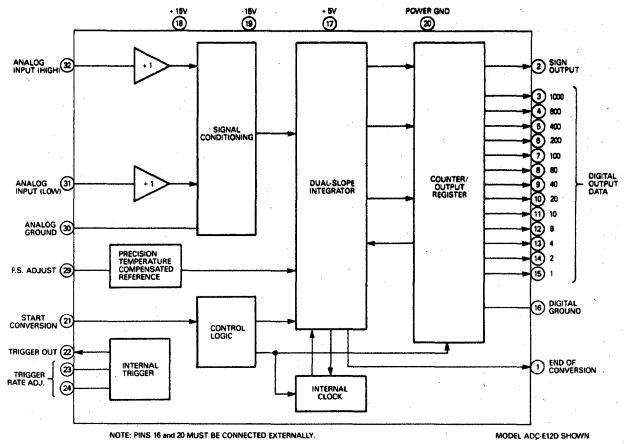
These converters employ a differential input amplifier, resulting in high input impedance and excellent common mode input characteristics for the measurement of floating differential signals. The dual-slope integrator yields high accuracy and linearity, integrating out spikes and noise that may degrade the accuracy of measurement. Performance is further enhanced through the use of a precision, temperature compensated reference source. Each converter also contains a clock generator, counter/output register and the necessary control logic circuitry to interface with DTL/TTL logic levels.

Data output format is either sign-magnitude binary or sign-magnitude BCD output code. Conversion data appears at the outputs in parallel form and is valid from the time that the end of conversion output goes low until the next start conversion command is received.

Analog input ranges available in this series are, ±1V, ±5V and ±10V for the binary version, and ±2V, ±10V and ±20V for the BCD version.

These converters are compact, fully encapsulated modules suitable for P.C. board mounting. Each is a functionally complete unit, requiring only external D.C. power for operation over a temperature range of 0°C to +70°C. Extended operating temperature range versions are also available.

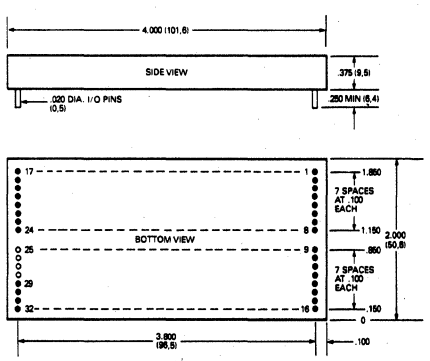




NOTE: PINS 16 and 20 MUST BE CONNECTED EXTERNALLY.

MODEL ADC-E12D SHOWN

MECHANICAL DIMENSIONS INCHES (MM)



NOTES:
1. OPEN DOTS DESIGNATE PINS OMITTED FROM ALL ADC-E MODELS.
2. 0.100 INCH = 2.5mm

INPUT/OUTPUT CONNECTIONS

	FUNCTION				
PIN	8B	10B	12B	8D	12D
1	END OF CONVERSION				
2	SIGN OUTPUT				
3	BIT 1 OUT	BIT 1 OUT	BIT 1 OUT	100	1000
4	—	BIT 2 OUT	—	—	800
5	—	BIT 3 OUT	—	—	400
6	BIT 2 OUT	BIT 4 OUT	BIT 2 OUT		200
7	BIT 3 OUT	BIT 5 OUT	BIT 3 OUT	—	100
8	—	—	BIT 4 OUT	80	80
9	—	—	BIT 5 OUT	40	40
10	—	—	BIT 6 OUT	20	20
11	—	—	BIT 7 OUT	10	10
12	BIT 4 OUT	BIT 6 OUT	BIT 8 OUT	8	8
13	BIT 5 OUT	BIT 7 OUT	BIT 9 OUT	4	4
14	BIT 6 OUT	BIT 8 OUT	BIT 10 OUT	2	2
15	BIT 7 OUT	BIT 9 OUT	BIT 11 OUT	1	1
16	DIGITAL GROUND				
17	+5V POWER IN				
18	+15V POWER IN				
19	−15V POWER IN				
20	POWER GROUND				
22	START CONVERSION INPUT				
23	TRIGGER OUTPUT				
24	TRIGGER RATE ADJUST				
29	TRIGGER RATE ADJUST				
30	FULL SCALE ADJUST				
31	ANALOG GROUND				
32	ANALOG INPUT (LOW)				
	ANALOG INPUT (HIGH)				

NOTE: Pins with no function designated are not present on that model.

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, ADC-E SERIES
(Typical at 25° C, ±15 VDC and +5 VDC supplies, unless otherwise noted)

	ADC-E8B/ 10B/12B (Binary)	ADC-E8D/ E12D. (BCD)
MAXIMUM RATINGS		
Analog Supply Voltage	±16VDC	
Logic Supply Voltage	+7 VDC	
Analog Input Voltage	±15 VDC	
INPUTS		
Analog Input Range,		
Differential Type, Suffix 2 Models[1]	±1V	±2V[2]
Single Ended, Suffix 3 Models	±5V	±10V[2]
Suffix 4 Models	±10V	±20V[2]
Input Impedance, Suffix 2 Models	100 Meg Typ	
Suffix 3, 4 Models	10K typ.	
Input Bias Current	250 nA typ, 500 nA max.	
Common Mode Voltage	±5V[7]	
Common Mode Rejection, DC to 60 Hz	80 dB	
External Start Conversion	+2.4V min to +5V max. Positive Pulse, 100 nsec to 1 μsec wide, with maximum rise and fall times of 500 nsec. Positive going edge resets converter register and initiates conversion. Loading: 1 TTL LOAD	
OUTPUTS		
Output Data	8/10/12 Parallel Lines	10/14 Parallel Lines
Output Data Logic Levels	V_{OUT} ("0")≤+0.4V V_{OUT} ("1")≥+2.4V Loading: 6 TTL LOADS	
Sign	Logic "1" for Positive Inputs	
Overrrange	Logic "1" for ± Input > Full Scale	
Output Coding	Sign-Mag. Binary	Sign-Mag. BCD
End of Conversion (E.O.C.)	V_{OUT} ("0")≤+0.4V, Conversion Complete V_{OUT} ("1")≥+2.4V, Conversion in Progress Loading: 8 TTL LOADS	
PERFORMANCE		
Resolution[3]	8, 10, 12 Bin. Bits	2½, 3½ BCD Digits
Linearity Error	±½ LSB max.	
No Missing Codes	Over Operating Temp. Range	
Gain Tempco	±50 ppm/° C max.	
Long Term Stability	±0.1%/Year, min.	
Input Integration Time[6]	8 bits, 103 μsec	2½ digits, 160 μsec
	10 bits, 410 μsec	3½ digits, 1.60 μsec
	12 bits, 1.64 msec	
Conversion Time, max.[5]	8 bits, 314 μsec	2½ digits, 478 μsec
	10 bits, 1.24 msec	3½ digits, 4.79 msec
	12 bits, 4.9 msec	
Conversion Rate, max.[6]	8 bits, 3.2 KHz	2½ digits, 2 KHz
	10 bits, 800 Hz	3½ digits, 200 Hz
	12 bits, 200 Hz	
POWER REQUIREMENT		
Analog Supply	+15V ±0.5 VDC @ 50 mA max. −15V ±0.5 VDC @ 50 mA max.	
Digital Supply	+5V ±0.25 VDC @ 150 mA max.	
PHYSICAL-ENVIRONMENTAL		
Operating Temperature Range	0° C to +70° C	
Storage Temperature Range	−55° C to +85° C	
Relative Humidity	Up to 100% Non-condensing	
Case Material	Black Diallyl Phthalate per MIL-M-14	
Case Size	4 X 2 X 0.4 inches (101,6 X 50,8 X 10,2 mm)	
Pins	.020" Round, Gold Plated, 0.250" Long min.	
Weight	4 oz. (114g)	

TECHNICAL NOTES

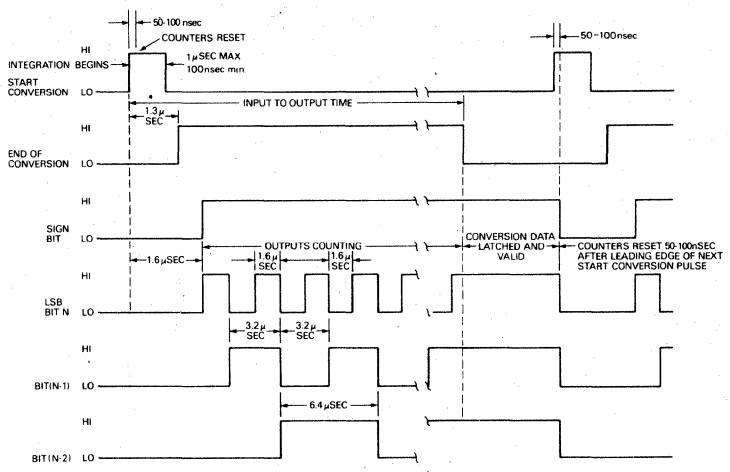
1. Conversion time is comprised of integration time and encoding time. It is measured fom the positive edge of the start conversion pulse to the negative going edge of the end of conversion pulse. This includes start conversion pulse width, analog input integration time and encoding time. Since encoding time varies with analog input level, this time period varies as a result. A maximum value is given to allow reliable timing of full scale conversions.
2. The analog input signal is integrated over a known time period for the beginning of the start conversion pulse until the end of the counter ramp-up time. The counter ramp-up is used to provide a fixed time period for integration.
3. Encoding time is the time required for the counters to sequence to the value of the input signal that has been acquired during the integration period. Since the counters sequence from zero to full scale, encoding time varies directly with the absolute value of the converter scale of the input, i.e., encoding time is ½ of maximum value for ±½ full scale inputs.
4. External start conversion pulse width should not be less than 100 nsec in order to insure resetting of the counters. Pulse widths over 1 μsec. will introduce an error due to their effect on integration time.
5. For applications of these converters under external control, the end of conversion pulse may be used to trigger output data transfer and system initiation of the next start conversion pulse.
6. Output data is valid from the negative going edge of the end of conversion pulse until the positive going edge of the next start conversion pulse.
7. All power supply inputs are internally bypassed.
8. Due to the integration period used in the dual-slope conversion technique, input noise is attenuated. Attenuation of input noise with a period equal to an integer multiple of the integration period is effectively infinite.

NOTES:

1. Bias current ground return required for differential input.
2. Includes 100% overange.
3. For bipolar inputs.
4. Conversion data valid when E.O.C. is low, remains valid until positive going edge of next conversion command.
5. Full scale input signal and 1 μsec start conversion pulsewidth. Refer to Technical Note 1.
6. For 1 μsec start conversion pulse width. See Technical Note 2.
7. The algebraic sum of both input voltage and common mode voltage must not exceed ±5V max.

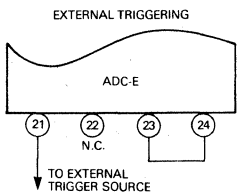
APPLICATIONS INFORMATION

ADC-E TIMING DIAGRAM

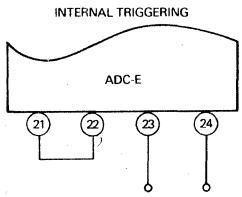


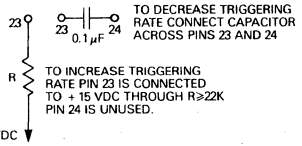
NOTE: OUTPUT COUNTING SEQUENCE SHOWN FOR BINARY VERSION.

INTERNAL/EXTERNAL TRIGGERING



NOTE: USE PIN 16 FOR DIGITAL GROUND





INTERNAL/EXTERNAL TRIGGERING

All ADC-E models include an internal clock for self triggering of the unit at approximately its maximum allowed rate, depending on the output register word length. The internal trigger circuit output when externally connected to the start conversion input, generates a main reset pulse which initiates a conversion, gates the clocked pulse train and sets up the sign polarity. The rate of the internal trigger can be reduced, if desired, with an external capacitor connected across pins 23-24, identified "Internal trigger rate adjust". When connected as directed, the external capacitor is in parallel with a 0.1 μF internal timing capacitor. Addition of a 0.1 μF external capacitor halves the rate of the internal trigger.

The rate of the internal trigger can be increased by connecting a resistor of greater than 22KΩ from pin 23 to + 15 VDC.

When an external start conversion pulse is provided for system synchronization, the internal trigger output (Pin 22) is not connected and the internal clock should be disabled by connecting a shorting lead between pins 23 and 24. External start conversion pulses can be applied at up to the maximum conversion rate as defined in the specifications, or may be applied discretely when the end of conversion output goes low. Start conversion pulses should be of as short a duration as possible while still yielding reliable operation, i.e., approximately 150 nsec. This will insure maximum converter accuracy during the analog input integration period.

ORDERING INFORMATION

MODEL	DESCRIPTION
ADC-E8B*_	8 Binary Bits
ADC-E10B*_	10 Binary Bits
ADC-E12B*_	12 Binary Bits
ADC-E8D*_	2½ Digit BDC
ADC-E12D*_	3½ Digit BDC

*FULL SCALE ANALOG INPUT RANGE AND TYPE	
B MODELS SUFFIX	**2** = ±1V Differential Inputs **3** = ±5V Single Ended Inputs **4** = ±10V Single Ended Inputs
D MODELS SUFFIX	**2** = ±2V Differential Inputs **3** = ±10V Single Ended Inputs **4** = ±20V Single Ended Inputs

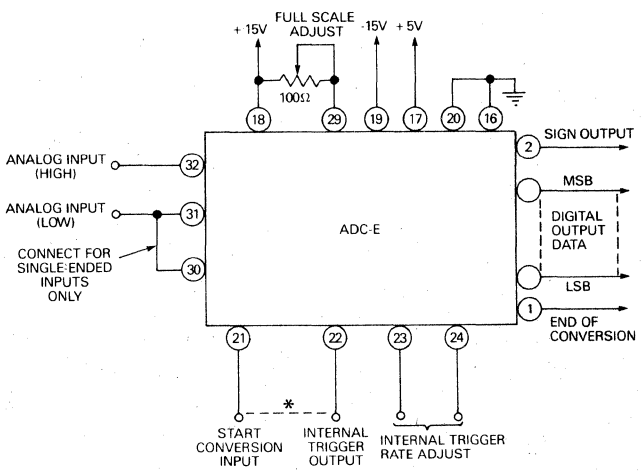
DILS-2 Mating Socket, 2 Req'd Per Module
TP100 Trimming Potentiometer, 100Ω

For extended temperature range operation, the following suffix is added to the model number. Consult factory for price and delivery.

—EX −25°C to +85°C operation

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

CONNECTIONS DIAGRAM



*NOTE: SEE "INTERNAL/EXTERNAL TRIGGERING"

CODING AND CALIBRATION

CODING TABLES

ADC-E12D

SCALE	ANALOG INPUT		3½ DIGIT SIGN MAGNITUDE BCD OUTPUT CODE	
	±20V RANGE	±10V RANGE	±2V RANGE	SIGN
+F.S.-1LSD	+19.990V	+9.995V	+1.999V	1 1 1001 1001 1001
+½F.S.	+10.000V	+5.000V	+1.000V	1 1 0000 0000 0000
+1 LSD	+0.010V	+0.005V	+0.001V	1 0 0000 0000 0001
+0	+0.000V	+0.000V	+0.000V	1 0 0000 0000 0000
−0	−0.000V	−0.000V	−0.000V	0 0 0000 0000 0000
−1 LSD	−0.010V	−0.005V	−0.001V	0 0 0000 0000 0001
−½F.S.	−10.000V	−5.000V	−1.000V	0 1 0000 0000 0000
−F.S.+1 LSD	−19.990V	−9.995V	−1.999V	0 1 1001 1001 1001

ADC-E8D

SCALE	ANALOG INPUT		2½ DIGIT SIGN MAGNITUDE BDC OUTPUT CODE	
	±20V RANGE	±10V RANGE	±2V RANGE	SIGN
+F.S.-1LSD	+19.9	+9.95V	+1.99V	1 1 1001 1001
+½F.S.	+10.0V	+5.00V	+1.00V	1 1 0000 0000
+1 LSD	+0.1V	+0.05V	+0.01V	1 0 0000 0001
+0	+0.0V	+0.00V	+0.00V	1 0 0000 0000
−0	−0.0V	−0.00V	−0.00V	0 0 0000 0000
−1 LSD	−0.1V	−0.05V	−0.01V	0 0 0000 0001
−½F.S.	−10.0V	−5.00V	−1.00V	0 1 0000 0000
−F.S.+1 LSD	−19.9V	−9.95V	−1.99V	0 1 1001 1001

ADC-E12B

SCALE	ANALOG INPUT			SIGN MAGNITUDE BINARY OUTPUT CODE	
	±1V RANGE	±5V RANGE	±10V RANGE	SIGN BIT	MSB LSB
+F.S.-1 LSB	+9.9951V	+4.9976V	+9.9952V	1	11111111111
+½F.S.	+0.5000V	+2.5000V	+5.000V	1	10000000000
+1 LSB	+0.49mV	+2.44mV	+4.880V	1	00000000001
+0	0.0000V	0.0000V	0.0000V	1	00000000000
−0	0.0000V	0.0000V	0.0000V	0	00000000000
−1 LSB	−0.49mV	−2.44mV	−4.88mV	0	00000000001
−½ F.S.	−0.5000V	−2.5000V	−5.0000V	0	10000000000
−F.S.+1 LSB	−9.9951V	−4.9976V	−9.9952V	0	11111111111

ADC-E10B

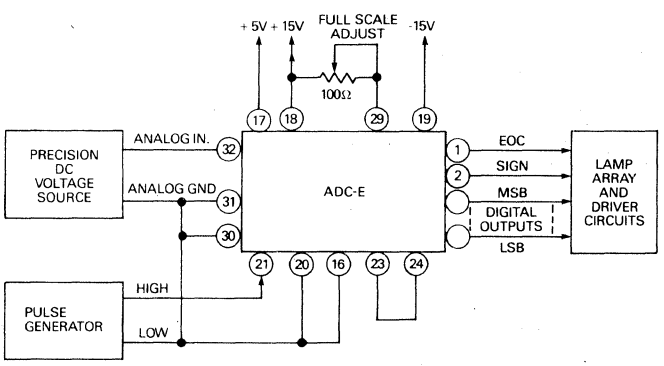
SCALE	ANALOG INPUT			SIGN MAGNITUDE BINARY OUTPUT CODE	
	±1V RANGE	±5V RANGE	±10V RANGE	SIGN BIT	MSB LSB
+F.S.-1 LSB	+0.9980V	+4.9902V	+9.9805V	1	111111111
+½F.S.	+0.5000V	+2.5000V	+5.0000V	1	100000000
+1 LSB	+2.0mV	+9.7mV	+19.5mV	1	000000001
+0	0.0000	0.0000	0.0000	1	000000000
−0	0.0000	0.0000	0.0000	0	000000000
−1 LSB	−2.0mV	−9.7mV	−19.5mV	0	000000001
−½ F.S.	−0.5000V	−2.5000V	−2.5000V	0	100000000
−F.S.+1 LSB	−0.9980V	−4.9902V	−9.9805V	0	111111111

ADC-E8B

SCALE	ANALOG INPUT			SIGN MAGNITUDE BINARY OUTPUT CODE	
	±1V RANGE	±5V RANGE	±10V RANGE	SIGN BIT	MSB LSB
+F.S.−1 LSB	+0.9922V	+4.9609V	+9.9219V	1	1111111
+½F.S.	+0.5000V	+2.5000V	+5.0000V	1	1000000
+1 LSB	+7.8mV	+39.1mV	+78.1mV	1	0000001
+0	0.0000V	0.0000V	0.0000V	1	0000000
−0	0.0000V	0.0000V	0.0000V	0	0000000
−1 LSB	−7.8mV	−39.1mV	−78.1mV	0	0000001
−½ F.S.	−0.5000V	−2.5000V	−5.0000V	0	1000000
−F.S.+1 LSB	−0.9922V	−4.9609V	−9.9219V	0	1111111

CALIBRATION PROCEDURE

ADJUSTMENT CONNECTIONS



CALIBRATION PROCEDURE

1. Connect the converter as shown in the adjustment connection diagram.
2. Allow 15 minutes after applying power for temperature stabilization.
3. Set pulse generator to supply a positive pulse of 150 nsec duration at a repetition rate of 1/2 of maximum conversion rate.
4. Set the precision DC voltage source to + F.S. -1 LSB value shown in the coding table for the ADC-E model and range under adjustment.
5. The lamp array displays the conversion result when the EOC indicator lamp is out. Adjust the Full Scale Adjustment potentiometer so that the output code for + F.S. -1 LSB shown in the applicable coding table is observed.

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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
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PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Fast, 8 Bit Analog-to-Digital Converters Model ADC-EH8B

FEATURES

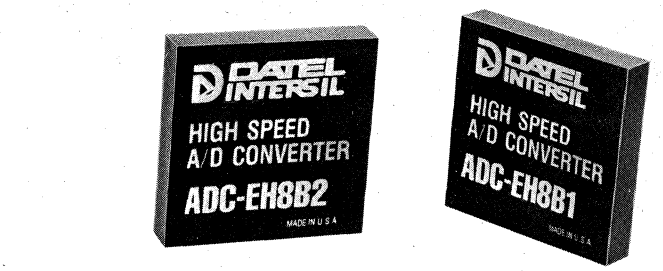
- 8 Bit Resolution
- 4.0 & 2.0 μsec. Conversion Time
- Unipolar or Bipolar Operation
- Parallel & Serial Outputs
- Low Cost

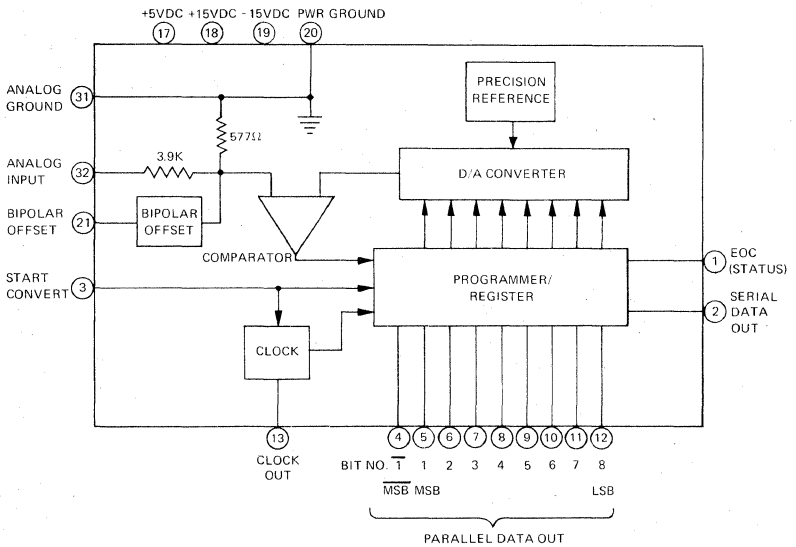
GENERAL DESCRIPTION

The model ADC-EH8B is a fast, 8 bit successive approximation type analog to digital converter in a compact 2 x 2 x .375 inch module. These converters are low cost devices with application in pulse code modulation systems and instrumentation and control systems requiring fast data conversion rates up to 500,000 per second. There are two models to choose from based on conversion speed: ADC-EH8B1 with a conversion time of 4.0 μsec. (250 kHz rate), and ADC-EH8B2 with a conversion time of 2.0 μsec. (500 kHz rate).

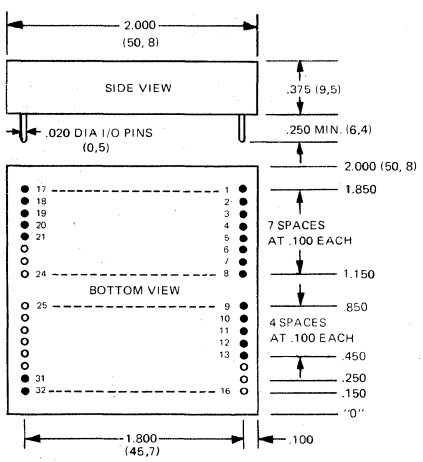
The high speed in a small size is made possible by the use of an MSI integrated circuit which provides all the necessary successive approximation logic, along with other new integrated circuit components. The analog input range is either unipolar 0 to +10V or bipolar -5V to +5V, determined by external pin connection. For unipolar operation no external adjustments are necessary; for bipolar operation only a bipolar offset adjustment must be made externally. Parallel output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. A serial output gives successive decision pulses in NRZ format with straight or offset binary coding. Other outputs are clock output for synchronization with serial data, and $\overline{\text{MSB}}$ output for two's complement coding.

Other specifications include full scale temperature coefficient of 50 ppm/°C max., long term stability of .05%/year, and linearity of ±1/2 LSB. Power requirement is ±15VDC and +5VDC.





MECHANICAL DIMENSIONS INCHES (MM)



NOTES
1. Open dots designate omitted pins.
2. 0.100 inch = 2.5 mm, 0.150 inch = 3.8 mm.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	E.O.C. (STATUS)
2	SERIAL DATA OUTPUT
3	START CONVERT
4	$\overline{\text{BIT 1 OUT (MSB)}}$
5	BIT 1 OUT (MSB)
6	BIT 2 OUT
7	BIT 3 OUT
8	BIT 4 OUT
9	BIT 5 OUT
10	BIT 6 OUT
11	BIT 7 OUT
12	BIT 8 OUT (LSB)
13	CLOCK OUT
17	+5V POWER IN
18	+15V POWER IN
19	-15V POWER IN
20	POWER GROUND
21	BIPOLAR OFFSET
31	ANALOG GROUND
32	ANALOG INPUT

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SPECIFICATIONS, ADC-EH8B

(Typical at 25°C, ±15V & +5V Supplies, unless otherwise indicated)

INPUTS

Analog Input Range	0V to +10V FS or ±5V FS
Input Impedance	4.45K ohms ±50 ohms
Input Overvoltage	±20V (no damage)
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 100 nsec. min. Rise and fall times <50 ns. Logic "1" resets converter Logic "0" initiates conversion Loading: 1 TTL load

OUTPUTS

Parallel Output Data	8 parallel lines of data held until next conversion command. V out ("0") ⩽ +0.4V V out ("1") ⩾ +2.4V Each output capable of driving up to 4 TTL loads.
Coding, Unipolar Operation	Straight Binary, positive true
Bipolar Operation	Offset Binary, positive true. Two's Complement, positive true.
Serial Output Data	NRZ successive decision pulse output generated during conversion, with MSB first. Straight binary or offset binary coding. Loading: 4 TTL loads
End of Conversion (EOC)	Conversion Status Signal. V out ("O") ⩽ 0.4V indicates conversion time completed. V out ("1") ⩾ +2.4V during reset and conversion periods. Loading: 4 TTL loads.
Clock Output	Internal clock pulse train of negative going pulses from +5V to 0V gated on during conversion time. Loading: 6 TTL loads

PERFORMANCE

Resolution	8 Bits (1 part in 256)
Linearity Error	± 1/2 LSB max.
Differential Nonlinearity	± 1/2 LSB max.
Temp. Coeff. of Gain	± 50ppm/°C max.
Temp. Coeff. of Zero, Unipolar	± 100μV/°C max.
Temp. Coeff. of Offset, Bipolar	± 35 ppm of FS/°C max.
Long Term Stability	± .05%/year
Power Supply Rejection	± .02% of FS/% supply, max.
Conversion Time	4.0 μsec. max., ADC-EH8B1 2.0 μsec. max., ADC-EH8B2

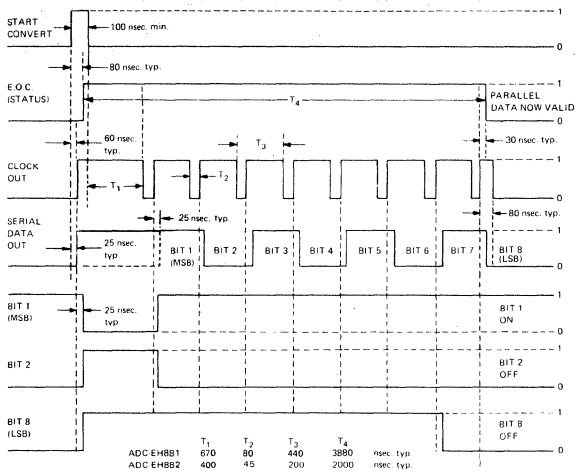
POWER REQUIREMENT

± 15VDC ±0.5V @ 25mA max.
+5VDC ± 0.25V @ 125mA max.

PHYSICAL-ENVIRONMENTAL

Operating Temp. Range	0°C to 70°C
Storage Temp. Range	−55°C to +85°C
Relative Humidity	Up to 100% non-condensing
Case Size	2 x 2 x 0.375 inches (50,8 x 50,8 x 9,5 mm)
Case Material	Black diallyl phthalate per MIL-M-14
Pins	.020" round, gold plated, .250" lg. min.
Weight	2 oz. max. (57g.)

TIMING DIAGRAM FOR ADC-EH8B Output: 10101010



OUTPUT CODING

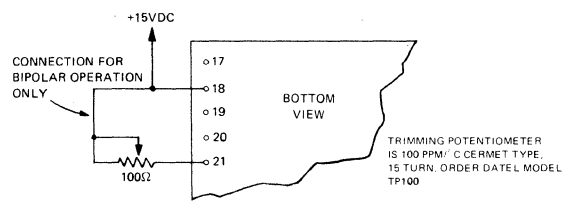
UNIPOLAR (0 TO +10V)

SCALE	INPUT VOLTAGE	STRAIGHT BINARY
+FS−1 LSB	+9.96V	1111 1111
+7/8 FS	+8.75V	1110 0000
+3/4 FS	+7.50V	1100 0000
+1/2 FS	+5.00V	1000 0000
+1/4 FS	+2.50V	0100 0000
+1 LSB	+0.04V	0000 0001
0	0.00V	0000 0000

BIPOLAR (−5V TO +5V)

SCALE	INPUT VOLTAGE	OFFSET BIN	2'S COMPLEMENT
+FS−1 LSB	+4.96V	1111 1111	0111 1111
+3/4 FS	+3.75V	1110 0000	0110 0000
+1/2 FS	+2.50V	1100 0000	0100 0000
0	0.00V	1000 0000	0000 0000
−1/2 FS	−2.50V	0100 0000	1100 0000
−3/4 FS	−3.75V	0010 0000	1010 0000
−FS+1 LSB	−4.96V	0000 0001	1000 0001
−FS	−5.00V	0000 0000	1000 0000

ADC-EH8B CALIBRATION



1. UNIPOLAR – No adjustments are necessary and 100Ω trimming pot is not used. Full scale and zero are internally set to better than 1/2 LSB. Pin 21 is left open.
2. BIPOLAR – Connect pin 18 (+15VDC) to pin 21 through a 100Ω trimming potentiometer as shown. Connect a precision voltage source to pin 32 and set the input voltage to + 1/2 LSB or +0.020V. Adjust the trimming potentiometer so that the output code flickers equally between 1000 0000 and 1000 0001.

ORDERING INFORMATION

ADC-EH8B —

CONVERSION TIME
1 = 4.0 μSEC.
2 = 2.0 μSEC.

MATING SOCKETS:
DILS-2 (2/MODULE)
TP100 TRIMMING POT.

For extended temperature range operation, the following suffixes are added to the model number. Consult factory for pricing.

−EX	−25°C to +85°C operation
−EXX−HS	−55°C to +85°C operation with hermetically sealed semiconductor components.

NOTE: ADC-EH8B1 & 2 replace former models ADC-EH1 & 2 and are improved models of these units respectively. The only difference from the previous models is the 3 additional output pins for serial output, clock output, and $\overline{\text{MSB}}$ output, and a change in input impedance from 5K ohms to 4.45K ohms. If the newly used pins (nos. 2, 4, and 13) cause a problem in an existing application, they should be clipped off.

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PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

10 Bit, 2.0 and 4.0 μSec. Analog-to-Digital Converters Model ADC-EH10B

FEATURES

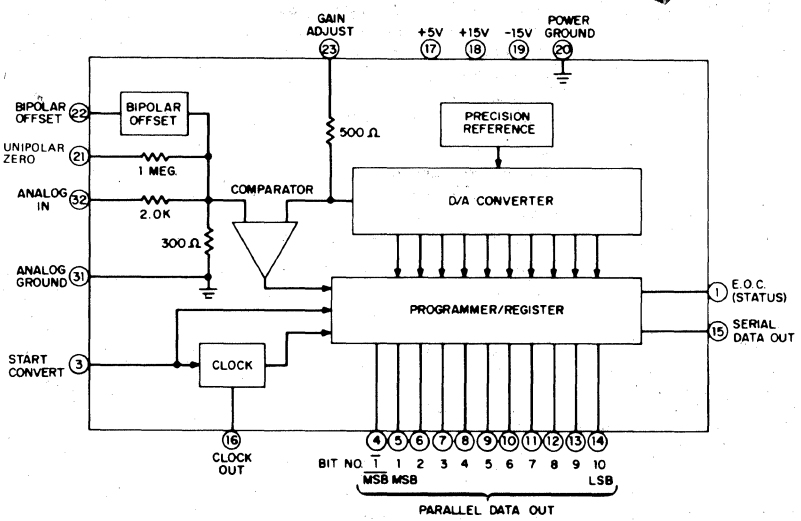
- 2.0 μsec. Conversion — ADC-EH10B2
- 4.0 μsec. Conversion — ADC-EH10B1
- 10 Bit Resolution
- Compact 3" x 2" x .375" Module
- ±30ppm/°C max. Tempco

GENERAL DESCRIPTION

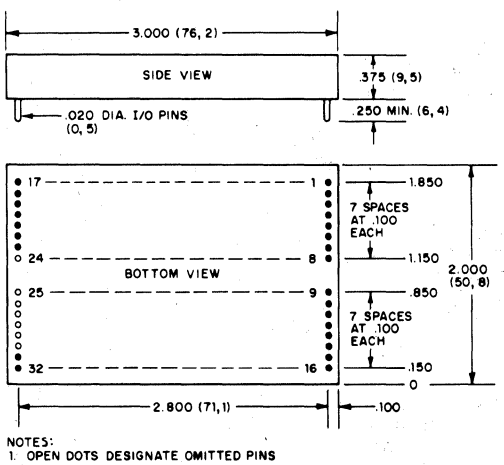
Model ADC-EH10B is a very fast 10 bit successive approximation type A/D converter in a compact low profile package. Low pricing makes this converter an ideal choice for many applications including fast scanning data acquisition systems, PCM systems, and fast pulse analysis. This converter is available in two versions based on conversion speed: ADC-EH10B1 with 4.0 μsec. (250kHz rate) and ADC-EH10B2 with 2.0 μsec. (500kHz rate).

High speed and moderate power consumption (1.7 watts) in a compact size (3" x 2" x .375") are made possible by use of an MSI integrated circuit successive approximation programmer/register used with 10 fast switching current sources driving a low impedance R-2R ladder network. A fast precision comparator and precision voltage reference circuit are also used.

Operating features include unipolar (0 to +10V) or bipolar (±5V) operation by external pin connection. The converter has a maximum full scale temperature coefficient of ±30ppm/°C and is monotonic over the full operating temperature range of 0°C to 70°C. External offset and gain adjustments are provided for precise calibration of zero and full scale. Parallel output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. A serial output gives successive decision pulses in NRZ format with straight binary or offset binary coding. Other outputs include clock output for synchronizing serial data, MSB output for two's complement coding, and end of conversion (status) signal. All outputs are DTL/TTL compatible. Power requirement is ±15VDC and +5VDC. The ADC-EH10B is also available in extended temperature range versions.



MECHANICAL DIMENSIONS INCHES (MM)



NOTES:
1. OPEN DOTS DESIGNATE OMITTED PINS
2. 0.100 INCH = 2.5mm

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	E.O.C. (STATUS)
2	NO CONNECTION
3	START CONVERT
4	BIT 1 OUT (MSB)
5	BIT 1 OUT (MSB)
6	BIT 2 OUT
7	BIT 3 OUT
8	BIT 4 OUT
9	BIT 5 OUT
10	BIT 6 OUT
11	BIT 7 OUT
12	BIT 8 OUT
13	BIT 9 OUT
14	BIT 10 OUT (LSB)
15	SERIAL DATA OUT
16	CLOCK OUT
17	+5VDC POWER IN
18	+15VDC POWER IN
19	-15VDC POWER IN
20	POWER GROUND
21	UNIPOLAR ZERO
22	BIPOLAR OFFSET.
23	GAIN ADJUST.
31	ANALOG GROUND
32	ANALOG IN

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SPECIFICATIONS, ADC-EH10B
(Typical at 25°C, ±15V & +5V Supplies, unless otherwise indicated)

INPUTS

Analog Input Range	0V to +10V FS or ±5V FS
Input Impedance	2.3K ±0.1%
Input Overvoltage	±20V, no damage
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 50 nsec. min. Rise and fall times <500 nsec. Logic "1" resets converter Logic "0" initiates conversion Loading: 1 TTL load

OUTPUTS

Parallel Output Data	10 parallel lines of data held until next conversion command. V out ("0") ⩽ +0.4V V out ("1") ⩾ +2.4V Each output capable of driving up to 4 TTL loads.
Coding, Unipolar operation	Straight Binary, positive true
Bipolar operation	Offset Binary, positive true Two's complement, positive true
Serial Output Data	NRZ successive decision pulse output generated during conversion with MSB first. Straight binary or offset binary, positive true coding. Loading: 4 TTL loads
End of Conversion (EOC)	Conversion Status Signal. V out ("0") ⩽ +0.4V indicates conversion completed. V out ("1") ⩾ +2.4V during reset and conversion. Loading: 4 TTL loads
Clock Output	Internal clock pulse train of negative going pulses from +5V to 0V gated on during conversion time. Loading: 6 TTL loads

PERFORMANCE

Resolution	10 Bits (1 part in 1024)
Nonlinearity	±1/2 LSB max.
Differential Nonlinearity	±1/2 LSB max.
Differential Nonlinearity T.C.	±10ppm/°C max.
Temp. Coeff. of Gain	±30ppm/°C max.
Temp. Coeff. of Zero, unipolar	±150 μV/°C max.
Temp. Coeff. of Offset, bipolar	±20ppm/°C max.
Power Supply Rejection	.01% FS/% supply, max.
Conversion Time	4.0 μsec. max., ADC-EH10B1 2.0 μsec. max., ADC-EH10B2

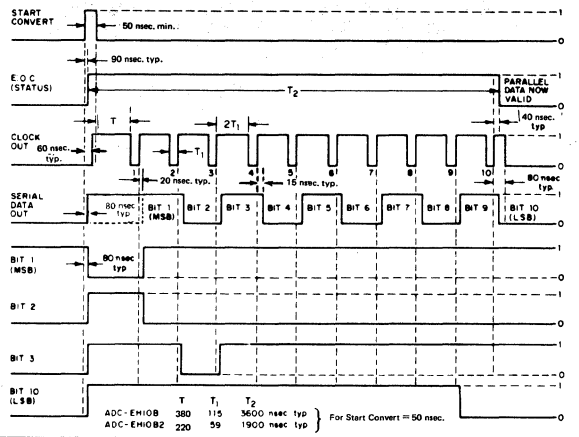
POWER REQUIREMENT

+15VDC ±0.5VDC @ 75mA max.
-15VDC ±0.5VDC @ 20mA max.
+5VDC ±0.25VDC @ 150mA max.

PHYSICAL-ENVIRONMENTAL

Operating Temp. Range	0°C to 70°C
Storage Temp. Range	-25°C to +85°C
Relative Humidity	Up to 100% non-condensing
Case Size	3 x 2 x .375 inches (76,2 x 30,8 x 9,5mm)
Case Material	Black Diallyl Phthalate per MIL-M-14
Pins	.020" round, gold plated, .250" long min.
Weight	3 oz. max. (85g.)

TIMING DIAGRAM FOR ADC-EH10B Output: 1010101010



OUTPUT CODING

UNIPOLAR (0V TO +10V)

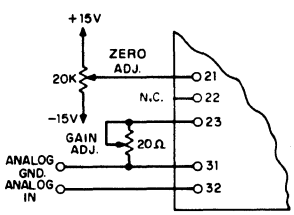
SCALE	INPUT VOLTAGE	STRAIGHT BINARY
+FS - 1 LSB	+9.9902V	1111 1111 11
+7/8 FS	+8.7500V	1110 0000 00
+3/4 FS	+7.5000V	1100 0000 00
+1/2 FS	+5.0000V	1000 0000 00
+1/4 FS	+2.5000V	0100 0000 00
+ 1 LSB	+0.0098V	0000 0000 01
0	0.0000V	0000 0000 00

BIPOLAR (–5V TO +5V)

SCALE	INPUT VOLTAGE	OFFSET BINARY	TWO'S COMPLEMENT*
+FS -1 LSB	+4.9902V	1111 1111 11	0111 1111 11
+3/4 FS	+3.7500V	1110 0000 00	0110 0000 00
+1/2 FS	+2.5000V	1100 0000 00	0100 0000 00
0	0.0000V	1000 0000 00	0000 0000 00
-1/2 FS	-2.5000V	0100 0000 00	1100 0000 00
-3/4 FS	-3.7500V	0010 0000 00	1010 0000 00
-FS + 1 LSB	-4.9902V	0000 0000 01	1000 0000 01
-FS	-5.0000V	0000 0000 00	1000 0000 00

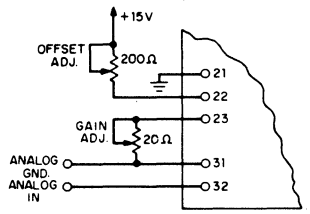
*Using $\overline{\text{MSB}}$ output for Bit 1

GAIN & OFFSET ADJUSTMENTS



UNIPOLAR OPERATION

1. Apply START CONVERT pulses to pin 3 (see specifications and timing diagram).
2. Apply a precision reference voltage source to ANALOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to Zero +1/2 LSB (+4.9mV). Adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 00 and 0000 0000 01.
3. Adjust the output of the voltage reference to +FS – 1 1/2 LSB (+9.9854V). Adjust the GAIN trimming potentiometer so that the output code flickers equally between 1111 1111 10 and 1111 1111 11.



BIPOLAR OPERATION

1. Apply START CONVERT pulses to pin 3 (see specifications and timing diagram).
2. Apply a precision reference voltage source to ANALOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to –FS +1/2 LSB (–4.9951V). Adjust the offset trimming potentiometer so that the output code flickers equally between 0000 0000 00 and 0000 0000 01.
3. Adjust the output of the voltage reference to +FS – 1 1/2 LSB (+4.9854V). Adjust the GAIN trimming potentiometer so that the output code flickers equally between 1111 1111 10 and 1111 1111 11.

ORDERING INFORMATION

ADC-EH10B ____

CONVERSION TIME
1 = 4.0 μsec.
2 = 2.0 μsec.

MATING SOCKETS:
DILS-2 (2/MODULE)
TRIMMING POTENTIOMETERS:
TP20, TP200, TP20K

For extended temperature range operation, the following suffixes are added to the model number. Consult factory for pricing.

–EX	-25°C to +85°C operation
–EXX–HS	-55°C to +85°C operation with hermetically sealed semiconductor components

NOTE: ADC-EH10B1 replaces former Datel model ADC-EH10B and is an improved version of the model. The only differences from the previous model is the change in input impedance from 10K ohms to 2.3K ohms, and the reduction in 5V supply current from 280mA to 150mA.

THE ADC-EH10B CONVERTERS ARE COVERED BY GSA CONTRACT

DATEL INTERSIL
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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

12 Bit, 4.0 and 8.0 μSec. Analog-to-Digital Converters Model ADC-EH12B1, B2

FEATURES

- 4.0 μsec. Conversion—ADC-EH12B2
- 8.0 μsec. Conversion—ADC-EH12B1
- 12 Bit Resolution
- 30PPM/°C Tempco
- Low Profile—0.4" High

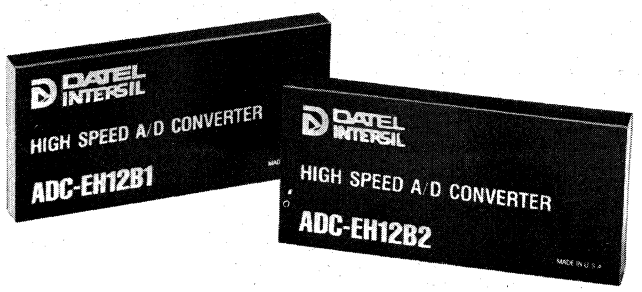
GENERAL DESCRIPTION

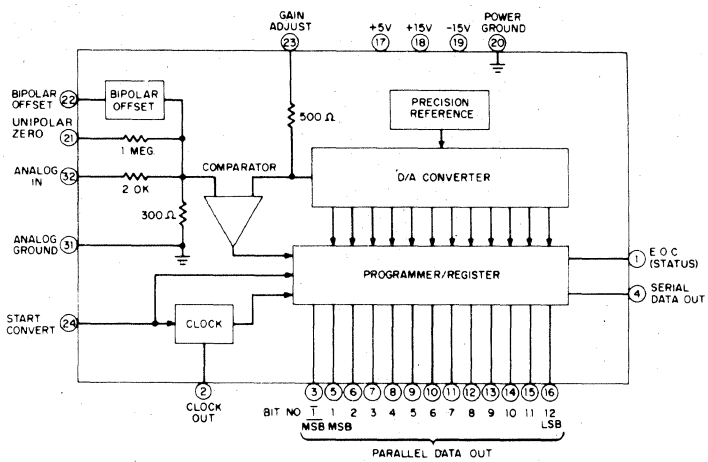
Model ADC-EH12B is a 4 microsecond, 12 bit successive approximation type A/D converter in a low profile 4 x 2 x 0.4 inch module. This high performance converter is priced at about half that of other competing models; in addition, it consumes only 2.0 watts of power, much less than competing devices. It is ideal for application in PCM systems, data acquisition systems, and other instrumentation and control systems requiring very fast data conversion rates up to 250,000 per second. The ADC-EH12B is also available in an even lower cost 8.0 μsec. version.

The ADC-EH12B design utilizes an MSI integrated circuit successive approximation programmer/register, 12 fast switching current sources, a low impedance R-2R resistor network, a precision voltage reference circuit, and a fast precision comparator to achieve its very fast conversion rate.

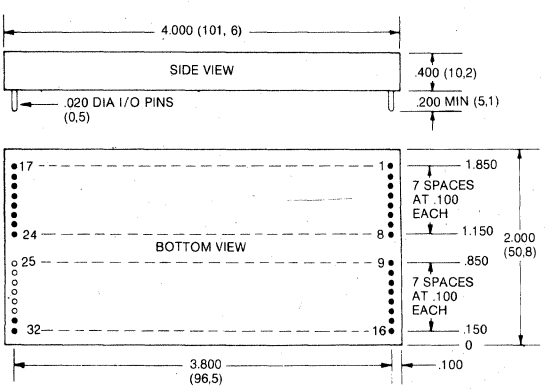
Operating features include unipolar (0 to +10V) or bipolar (±5V) operation by external pin connection. Full scale temperature coefficient is 30ppm/°C maximum and the converter is monotonic over its full operating temperature range of 0°C to 70°C. External offset and gain adjustments are provided for precise calibration of zero and full scale. Parallel output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. A serial output gives successive decision pulses in NRZ format with straight binary or offset binary coding. Other outputs include clock output for synchronization with serial data, $\overline{\text{MSB}}$ output for use in two's complement coding, and end of conversion (status) signal. All outputs are DTL/TTL compatible.

Power requirement is ±15VDC and +5VDC. Extended temperature range versions are also available.





MECHANICAL DIMENSIONS INCHES (MM)



NOTES:
1. OPEN DOTS DESIGNATE OMITTED PINS
2. 0.100 INCH = 2.5mm

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	E.O.C. (STATUS)
2	CLOCK OUT
3	BIT 1 OUT (MSB)
4	SERIAL DATA OUT
5	BIT 1 OUT (MSB)
6	BIT 2 OUT
7	BIT 3 OUT
8	BIT 4 OUT
9	BIT 5 OUT
10	BIT 6 OUT
11	BIT 7 OUT
12	BIT 8 OUT
13	BIT 9 OUT
14	BIT 10 OUT
15	BIT 11 OUT
16	BIT 12 OUT (LSB)
17	+5V POWER IN
18	+15V POWER IN
19	-15V POWER IN
20	POWER GROUND
21	UNIPOLAR ZERO
22	BIPOLAR OFFSET
23	GAIN ADJUST
24	START CONVERT IN
31	ANALOG GROUND
32	ANALOG IN

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, ADC-EH12B
(Typical at 25°C, ±15V & +5V Supplies, unless otherwise indicated)

INPUTS

Analog Input Range	0V to +10V FS or ±5V FS
Input Impedance	2.3K ohms ±0.1%
Input Overvoltage	±20V, no damage
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 100 nsec. min. Rise and fall times <500 nsec. Logic "1" resets converter Logic "0" initiates conversion Loading: 1 TTL load

OUTPUTS

Parallel Output Data	12 parallel lines of data held until next conversion command. V out ("0") ≤ +0.4V V out ("1") ≥ +2.4V Each output capable of driving up to 4 TTL loads.
Coding, Unipolar operation	Straight Binary, positive true
Bipolar operation	Offset Binary, positive true Two's complement, positive true
Serial Output Data	NRZ successive decision pulse output generated during conversion with MSB first. Straight binary or offset binary, positive true coding. Loading: 4 TTL loads
End of Conversion (EOC)	Conversion Status Signal. V out ("0") ≤ +0.4V indicates conversion completed. V out ("1") ≥ +2.4V during reset and conversion. Loading: 4 TTL loads
Clock Output	Internal clock pulse train of negative going pulses from +5V to 0V gated on during conversion time. Loading: 6 TTL loads

PERFORMANCE

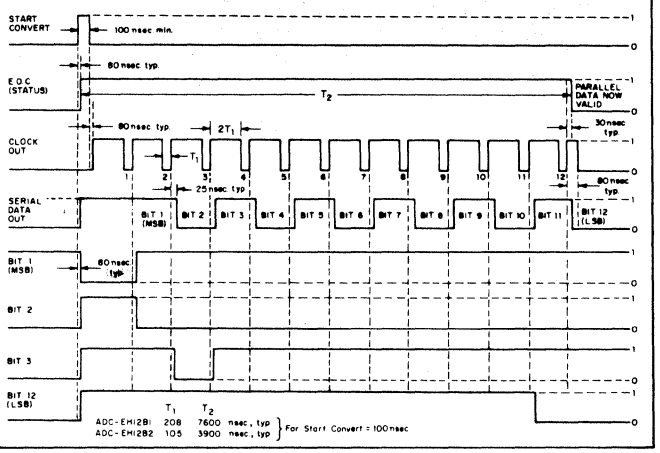
Resolution	12 Bits (1 part in 4096)
Nonlinearity	±1/2 LSB max.
Differential Nonlinearity	±1/2 LSB max.
Differential Nonlinearity T.C.	±3ppm/°C max.
Temp. Coeff. of Gain	±30ppm/°C max.
Temp. Coeff. of Zero, unipolar	±150 μV/°C max.
Temp. Coeff. of Offset, bipolar	±15ppm of F.S./°C max.
Power Supply Rejection	.01% FS/% supply, max.
Conversion Time	8.0 μsec. max., ADC-EH12B1 4.0 μsec. max., ADC-EH12B2

POWER REQUIREMENT	±15VDC ±0.5VDC @ 40mA max. +5VDC ±0.25VDC @ 150mA max.

PHYSICAL-ENVIRONMENTAL

Operating Temp. Range	0°C to 70°C
Storage Temp. Range	-25°C to +85°C
Relative Humidity	Up to 100% non-condensing
Case Size	4 x 2 x 0.4 inches (101,6 x 50,8 x 10,2mm)
Case Material	Black Diallyl Phthalate per MIL-M-14
Pins	.020" round, gold plated, .200" long min.
Weight	4 oz. max. (114 g.)

TIMING DIAGRAM FOR ADC-EH12B Output: 101010101010



OUTPUT CODING

UNIPOLAR (0V TO +10V)

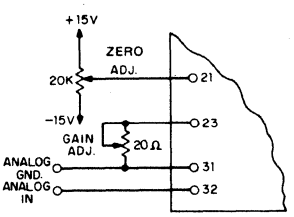
SCALE	INPUT VOLTAGE	STRAIGHT BINARY
+FS - 1 LSB	+9.9976V	1111 1111 1111
+7/8 FS	+8.7500V	1110 0000 0000
+3/4 FS	+7.5000V	1100 0000 0000
+1/2 FS	+5.0000V	1000 0000 0000
+1/4	+2.5000V	0100 0000 0000
+1 LSB	+0.0024V	0000 0000 0001
0	0.0000V	0000 0000 0000

BIPOLAR (-5V TO +5V)

SCALE	INPUT VOLTAGE	OFFSET BINARY	TWO'S COMPLEMENT*
+FS - 1 LSB	+4.9976V	1111 1111 1111	0111 1111 1111
+3/4 FS	+3.7500V	1110 0000 0000	0110 0000 0000
+1/2 FS	+2.5000V	1100 0000 0000	0100 0000 0000
0	0.0000V	1000 0000 0000	0000 0000 0000
-1/2 FS	-2.5000V	0100 0000 0000	1100 0000 0000
-3/4 FS	-3.7500V	0010 0000 0000	1010 0000 0000
-FS + 1 LSB	-4.9976V	0000 0000 0001	1000 0000 0001
-FS	-5.0000V	0000 0000 0000	1000 0000 0000

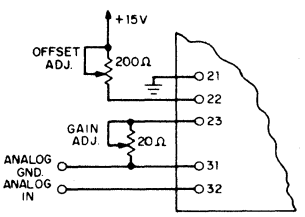
*Using $\overline{\text{MSB}}$ output for Bit 1

GAIN & OFFSET ADJUSTMENTS



UNIPOLAR OPERATION

1. Apply START CONVERT pulses to pin 24 (see specifications and timing diagram).
2. Apply a precision reference voltage source to ANALOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to Zero +1/2 LSB (+1.2mV). Adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.
3. Adjust the output of the voltage reference to +FS - 1 1/2 LSB (+9.9963V). Adjust the GAIN trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111.



BIPOLAR OPERATION

1. Apply START CONVERT pulses to pin 24 (see specifications and timing diagram).
2. Apply a precision reference voltage source to ANALOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to -FS +1/2 LSB (-4.9988V). Adjust the offset trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.
3. Adjust the output of the voltage reference to +FS - 1 1/2 LSB (+4.9854V). Adjust the GAIN trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111.

ORDERING INFORMATION

ADC-EH12B—

CONVERSION TIME
1= 8.0 μsec.
2= 4.0 μsec.

MATING SOCKETS:
DILS-2 (2/MODULE)
TRIMMING POTENTIOMETERS:
TP20, TP200, TP20K

For extended temperature range operation, the following suffixes are added to the model number. Consult factory for pricing.

—EX	-25°C to +85°C operation
—EXX—HS	-55°C to +85°C operation with hermetically sealed semiconductor components

THE ADC-EH12B CONVERTERS ARE COVERED BY GSA CONTRACT.

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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Ultra-Fast, 12 Bit Analog-to-Digital Converter Model ADC-EH12B3

FEATURES

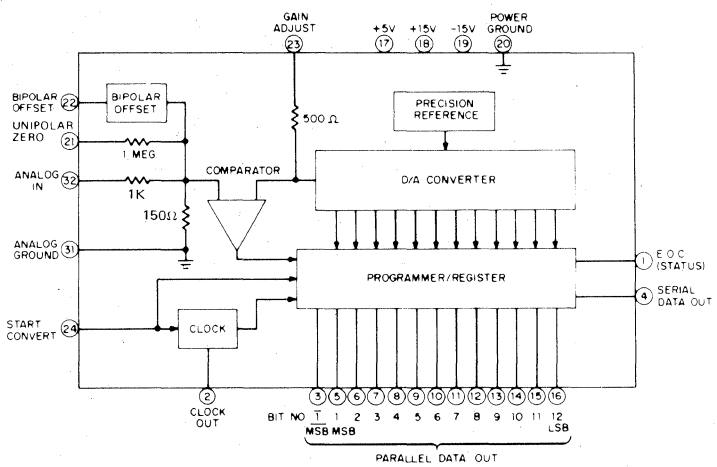
- 2.0 μsec. Conversion Time
- 12 Bit Resolution
- Low Power Consumption – 2.25W
- Low Profile Case – 0.4" High
- Economy Price

GENERAL DESCRIPTION

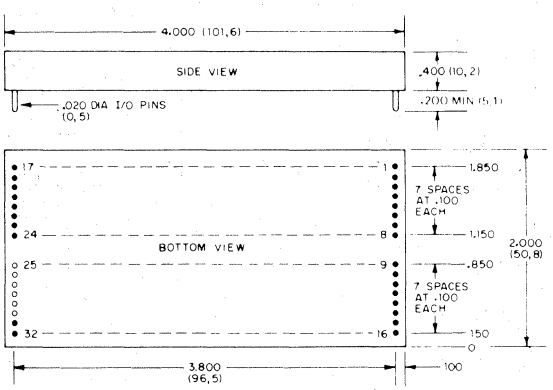
Model ADC-EH12B3 is a new, ultra fast, 12 bit successive approximation A/D converter with a 2.0 microsecond maximum conversion time. This converter utilizes 12 very fast switched current sources with a low impedance R-2R ladder network, a fast precision comparator, a precision zener reference source, and an MSI integrated circuit successive approximation register to achieve its state of the art performance. It is encapsulated in a low profile 2 x 4 x 0.4 inch module and consumes only 2.25 watts of power. The ADC-EH12B3 opens up a broad range of fast data conversion applications where conversion rates up to 500,000 per second are required.

Input voltage ranges are 0 to +10V unipolar or ±5V bipolar by external pin connection; input impedance is 1.15K ohms. The parallel output is in straight binary, offset binary, or two's complement coding. Serial output data is also brought out in the form of an NRZ format MSB first pulse train. Full scale temperature coefficient is ±30ppm/°C maximum and zero temperature coefficient is ±150μV/°C maximum. Due to its low differential linearity temperature coefficient there are no missing codes over the 0°C to 70°C operating temperature range. Provision is made for precise alignment in a given application.

Other DTL/TTL compatible outputs include clock, $\overline{\text{MSB}}$ output (for two's complement coding), and end of conversion (status) output. Power supply requirement is ±15VDC and +5VDC.



MECHANICAL DIMENSIONS INCHES (MM)



NOTES:
1. OPEN DOTS DESIGNATE OMITTED PINS
2. 0.100 INCH = 2.5mm

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	E.O.C. (STATUS)
2	CLOCK OUT
3	BIT 1 OUT (MSB)
4	SERIAL DATA OUT
5	BIT 1 OUT (MSB)
6	BIT 2 OUT
7	BIT 3 OUT
8	BIT 4 OUT
9	BIT 5 OUT
10	BIT 6 OUT
11	BIT 7 OUT
12	BIT 8 OUT
13	BIT 9 OUT
14	BIT 10 OUT
15	BIT 11 OUT
16	BIT 12 OUT (LSB)
17	+5V POWER IN
18	+15V POWER IN
19	-15V POWER IN
20	POWER GROUND
21	UNIPOLAR ZERO
22	BIPOLAR OFFSET
23	GAIN ADJUST
24	START CONVERT IN
31	ANALOG GROUND
32	ANALOG IN

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SPECIFICATIONS, ADC-EH12B3
(Typical at 25°C, ±15V & +5V Supplies, unless otherwise indicated)

INPUTS

Analog Input Range	0V to +10V FS or ±5V FS
Input Impedance	1.15K ohms ±0.1%
Input Overvoltage	±20V, no damage
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 100 nsec. min. Rise and fall times <500 nsec. Logic "1" resets converter Logic "0" initiates conversion Loading: 3 TTL loads

OUTPUTS

Parallel Output Data	12 parallel lines of data held until next conversion command. V out ("0") ≤ +0.4V V out ("1") ≥ +2.4V Each output capable of driving up to 4 TTL loads.
Coding, Unipolar operation	Straight Binary, positive true
Bipolar operation	Offset Binary, positive true Two's complement, positive true
Serial Output Data	NRZ successive decision pulse output generated during conversion with MSB first. Straight binary or offset binary, positive true coding. Loading: 4 TTL loads
End of Conversion (EOC)	Conversion Status Signal. V out ("0") ≤ +0.4V indicates conversion completed. V out ("1") ≥ +2.4V during reset and conversion. Loading: 4 TTL loads
Clock Output	Internal clock pulse train of negative going pulses from +5V to 0V gated on during conversion time. Loading: 6 TTL loads

PERFORMANCE

Resolution	12 Bits (1 part in 4096)
Nonlinearity	±1/2 LSB max.
Differential Nonlinearity	±1/2 LSB max.
Differential Nonlinearity T.C.	±3ppm/°C max.
Temp. Coeff. of Gain	±30ppm/°C max.
Temp. Coeff. of Zero, unipolar	±150μV/°C max.
Temp. Coeff. of Offset, bipolar	±15ppm of F.S./°C max.
Power Supply Rejection	.01% FS/% supply, max.
Conversion Time	2.0 μsec. maximum

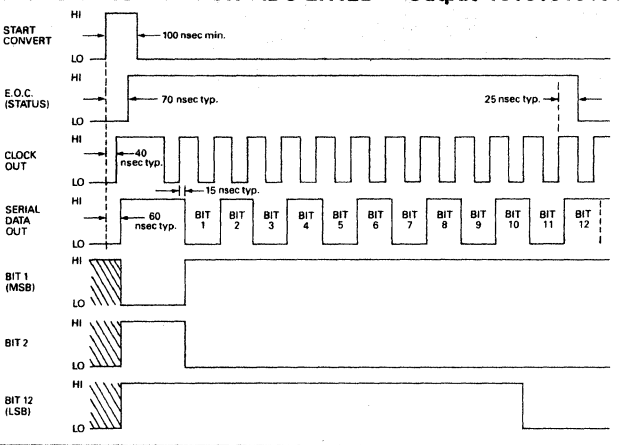
POWER REQUIREMENT

+15VDC ±0.5V @ 80mA max.
−15VDC ±0.5V @ 20mA max.
+5VDC ±0.25V @ 150mA max.

PHYSICAL-ENVIRONMENTAL

Operating Temp. Range	0°C to 70°C
Storage Temp. Range	-25°C to +85°C
Relative Humidity	Up to 100% non-condensing
Case Size	4 x 2 x 0.4 inches (101,6 x 50,8 x 10,2mm)
Case Material	Black Diallyl Phthalate per MIL-M-14
Pins	.020" round, gold plated, .200" long min.
Weight	4 oz. max. (114 g.)

TIMING DIAGRAM FOR ADC-EH12B Output 101010101010



OUTPUT CODING

UNIPOLAR (0V TO +10V)

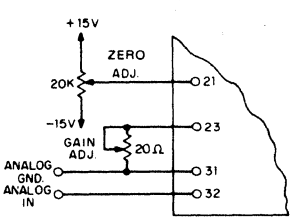
SCALE	INPUT VOLTAGE	STRAIGHT BINARY
+FS - 1 LSB	+9.9976V	1111 1111 1111
+7/8 FS	+8.7500V	1110 0000 0000
+3/4 FS	+7.5000V	1100 0000 0000
+1/2 FS	+5.0000V	1000 0000 0000
+1/4	+2.5000V	0100 0000 0000
+1 LSB	+0.0024V	0000 0000 0001
0	0.0000V	0000 0000 0000

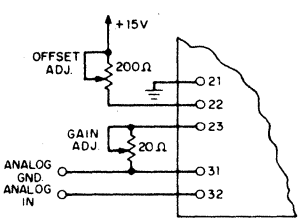
BIPOLAR (−5V TO +5V)

SCALE	INPUT VOLTAGE	OFFSET BINARY	TWO'S COMPLEMENT*
+FS - 1 LSB	+4.9976V	1111 1111 1111	0111 1111 1111
+3/4 FS	+3.7500V	1110 0000 0000	0110 0000 0000
+1/2 FS	+2.5000V	1100 0000 0000	0100 0000 0000
0	0.0000V	1000 0000 0000	0000 0000 0000
-1/2 FS	-2.5000V	0100 0000 0000	1100 0000 0000
-3/4 FS	-3.7500V	0010 0000 0000	1010 0000 0000
-FS + 1 LSB	-4.9976V	0000 0000 0001	1000 0000 0001
-FS	-5.0000V	0000 0000 0000	1000 0000 0000

*Using $\overline{MSB}$ output for Bit 1

GAIN & OFFSET ADJUSTMENTS





UNIPOLAR OPERATION

1. Apply START CONVERT pulses to pin 24 (see specifications and timing diagram).
2. Apply a precision reference voltage source to ANALOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to Zero +1/2 LSB (+1.2mV). Adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.
3. Adjust the output of the voltage reference to +FS − 1 1/2 LSB (+9.9963V). Adjust the GAIN trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111.

BIPOLAR OPERATION

1. Apply START CONVERT pulses to pin 24 (see specifications and timing diagram).
2. Apply a precision reference voltage source to ANALOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to −FS +1/2 LSB (−4.9988V). Adjust the offset trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.
3. Adjust the output of the voltage reference to +FS − 1 1/2 LSB (+4.9854V). Adjust the GAIN trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111.

ORDERING INFORMATION

For extended temperature range operation, the following suffixes are added to the model number. Consult factory for pricing.

−EX	-25°C to +85°C operation
−EXX−HS	-55°C to +85°C operation with hermetically sealed semiconductor components

MATING SOCKETS:
DILS-2 (2/MODULE)
TRIMMING POTENTIOMETERS:
TP20, TP200, TP20K

THE ADC-EH12B3 CONVERTER IS COVERED UNDER GSA CONTRACT.

DATEL
11 CABOT BOULEVARD, MANSFIELD, MA 02048
TEL. (617)828-8000 / (617)339-9341 / TWX 710-346-1953 / TLX 951340

Low Cost, 4 and 8 Bit Flash A/D Converters ADC-UH Series

FEATURES

- **4 bits at 25 MHz**
- **8 bits at 8.33 MHz**
- **Unipolar and Bipolar Models 50 ppm/°C Tempco**
- **Rugged modular construction**
- **Low Cost**

GENERAL DESCRIPTION

The ADC-UH series is made up of two ultra high speed analog to digital converters: an eight binary bit model operating at conversion rates up to 8.33 MHz and a four bit version operating at rates up to 25 MHz.

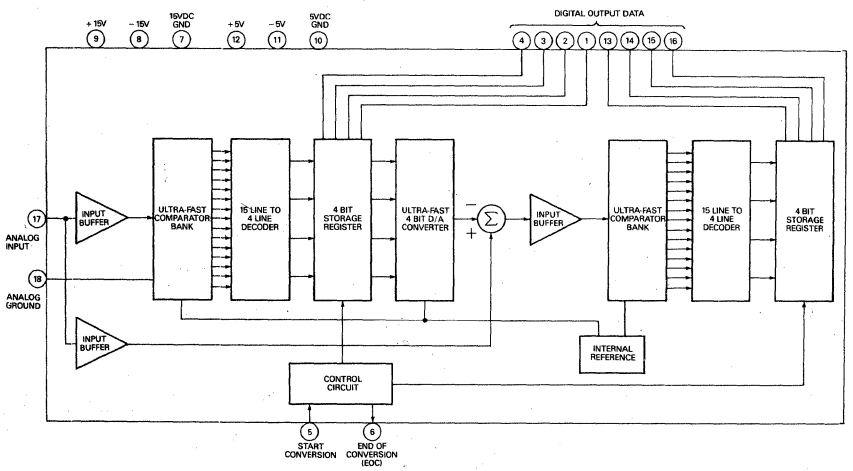
Converters in this series employ the ultra-fast parallel, or flash, conversion technique and are of modular construction. These high-speed designs have been tested and proven in many different applications. Close attention to circuit and layout detail has resulted in highly reliable converters having relatively low power consumption.

The ADC-UH4B uses a single stage parallel conversion technique to achieve a conversion in forty nanoseconds. This model is composed of a bank of 15 ultra-fast comparators, a 15 line to 4 bit decoder, a 4 bit storage register, and control logic circuitry.

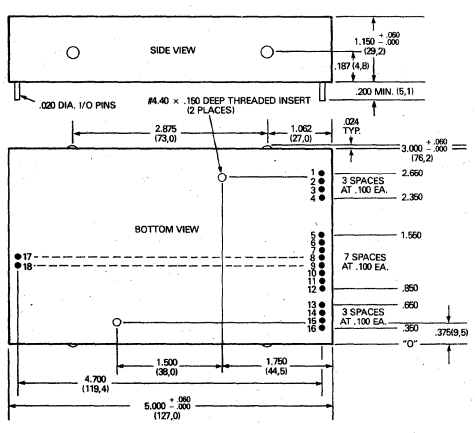
The ADC-UH8B employs a two-stage parallel conversion technique to accomplish an 8 bit conversion every 120 nanoseconds. The two stage modification of the parallel conversion technique is employed to keep the number of comparators to 30 instead of 255 which would be required with the single stage technique. In addition to 30 ultra-fast comparators, the eight bit model contains two 15 line to 4 bit decoders, two 4 bit storage registers, a high speed 4 bit D/A converter, and control logic circuitry.

Output coding for both models is straight binary for unipolar operation and offset binary for bipolar operation. Converters for bipolar analog inputs are designated by the suffix "2" after the model number. All control inputs, outputs, and data outputs are compatible with standard TTL logic levels.

Each model is fully encapsulated in a 3" x 5" x 1.15" black anodized aluminum module suitable for direct mounting to pc boards. Input power requirements are ±15 VDC and ±5 VDC. Operating temperature range is 0°C to +70°C.



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: CASE IS BLACK ANODIZED ALUMINUM

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	BIT 4 (LSB, ADC-UH4B)
2	BIT 3
3	BIT 2
4	BIT 1 (MSB)
5	START CONVERT
6	E.O.C. (STATUS)
7	15VDC GROUND
8	-15VDC
9	+15VDC
10	5VDC GROUND
11	-5VDC
12	+5VDC
13	BIT 5
14	BIT 6
15	BIT 7
16	BIT 8 (LSB, ADC-UH8B)
17	ANALOG INPUT
18	ANALOG GROUND

NOTE: PINS 7, 10 AND 18 ARE INTERNALLY CONNECTED.

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, ADC-UH SERIES
Typical @ 25° C, ±15 VDC and +5 VDC Supplies, unless otherwise noted

	ADC-UH4B	ADC-UH8B
ADC-UH8B		
MAXIMUM RATINGS		
Analog Supply Voltage	±18 VDC	±18 VDC
Logic Supply Voltage	±5.25 VDC	±5.25 VDC
Analog Input Voltage	±5 VDC	±5 VDC
INPUTS		
Analog Input Range, Unipolar	0V to -2.56V	0V to -2.56V
Analog Input Range, Bipolar[1]	±1.28V	±1.28V
Input Impedance[2]	100K	100K
Input Capacitance	250 pF	20 pF
Input Current	+150 μA	±30 μA
Start Conversion	2V min. to 5V max. Positive Pulse, 40 nsec min. width. Positive Going Edge Initiates Conversion. Loading: 1 HTTL Load	
OUTPUTS		
Output Data	4 Parallel Lines	8 Parallel Lines
Output Logic Levels	VOUT ("0") ≤ +0.4V; VOUT ("1") ≥ +2.4V; Loading: 4 TTL Loads	
Output Coding, Unipolar	Straight Binary	Straight Binary
Output Coding, Bipolar[1]	Offset Binary	Offset Binary
End of Conversion	2V min. to 5V max. Positive Pulse 45 nsec Width. Negative Going Edge Indicates Conversion Complete. Loading: 1 HTTL Load	
PERFORMANCE		
Resolution	4 Bits (1 part in 16)	8 Bits (1 part in 256)
Differential Linearity Error, max.	±¼ LSB	±1 LSB
Missing Codes	None over oper. temp. range	None at 25°C
Gain Tempco	±50 ppm/°C	±50 ppm/°C
Long Term Stability	±0.25%/Year	±0.25%/Year
Conversion Time	40 nsec.	120 nsec.
Conversion Rate, max.	25 MHz	8.33 MHz
POWER REQUIREMENT		
Analog Supply Voltage	±15 VDC ±0.2 VDC	±15 VDC ±0.2 VDC
Positive Analog Current	80 mA	80 mA
Negative Analog Current	9 mA	9 mA
Logic Supply Voltage	±5 VDC ±0.1 VDC	±5 VDC ±0.1 VDC
Positive Logic Current	650 mA	1300 mA
Negative Logic Current	150 mA	250 mA
PHYSICAL-ENVIRONMENTAL		
Operating Temp. Range	0°C to +70°C	
Storage Temp. Range	-55°C to +85°C	
Relative Humidity	Up to 100% Non-Condensing	
Package Type	Black Anodized Aluminum Module	
Package Size	3 × 5 × 1.150 inches (76,2 × 127,0 × 29,2 mm)	
Pins	0.020" Dia. × 0.250" Long, Gold Plated	
Weight	15 oz. (425g)	

NOTES:

1. For bipolar operation order suffix "2" model.
2. 10K min.

TECHNICAL NOTES

1. Model ADC-UH8B has a throughput delay of 140 nsec. due to the two stage conversion technique used. However, a new conversion can be started every 120 nsec. for a conversion rate of 8.33 MHz.
2. The eight bit conversion result of the ADC-UH8B is made up of two 4 bit partial results that appear 95 nsec. apart. Since each 4 bit result is present at the outputs for 110 nsec., the 15 nsec. overlap between the two partial results is the period in which the complete 8 bit conversion result is available at the outputs. This overlap period occurs immediately prior to the falling edge of the end of conversion output pulse. While the 8 bit word is available at the outputs, it may be loaded into an external register for transfer. Transfer may be accomplished by using a zero hold-time register such as an SN74H106 or a fast quad D-type flip-flop such as the SN74S175. One configuration of the ADC-UH8B is shown in the diagram titled "Two State Data Transfer Register". This register allows access to the full 8 bit word for 150 nsec. after the negative going edge of the end of conversion pulse and acts as a deskewing register.
3. For applications of the ADC-UH8B requiring a sample-hold, Datel-Intersil's SHM-UH3 is recommended. The SHM-UH3 is an ultra-fast sample-hold designed specifically for use with the ADC-UH8B. The ADC-UH4B generally does not require a sample-hold due to its high speed.
4. The ADC-UH series has inverted analog input. Therefore, for the bipolar ±1.280V analog input range, a -1.280V input results in an output code of 11111111. Conversely, an analog input of +1.280V is coded as 00000000. Coding for bipolar models is offset binary.
5. The ADC-UH is completely calibrated at the factory and does not require any customer adjustment. Due to the high speed and sophisticated design of these units, calibration is a complex procedure involving specialized equipment. No attempt at adjustment should be made without contacting the factory for assistance.
6. The ADC-UH series modules are supplied with two threaded mounting holes on the bottom of the case to allow securing the module to a circuit board. Screws used for mounting should be tightened to between 4 and 8 inch pounds.
7. During operation, airflow over the case must be unrestricted to provide proper cooling. For operations in ambient temperatures above 50°C airflow of at least 100 linear feet per minute is recommended.

ORDERING INFORMATION

MODEL	DESCRIPTION
ADC-UH4B	4 Bits, 25 MHz, Unipolar
ADC-UH4B2	4 Bits, 25 MHz, Bipolar
ADC-UH8B	8 Bits, 8.33 MHz, Unipolar
ADC-UH8B2	8 Bits, 8.33 MHz, Bipolar

For extended temperature range operation the following suffixes should be added to the model number. Consult factory for price and delivery.

-EX	-25°C to +85°C operation
-EXX-HS	-55°C to +85°C operation with all hermetically sealed semiconductors

THESE CONVERTERS ARE COVERED BY GSA CONTRACT.

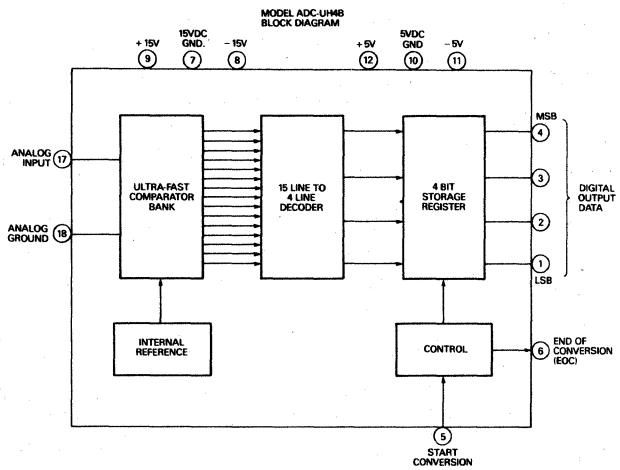
THEORY OF OPERATION

The ADC-UH4B employs the well-known parallel, or flash, high speed conversion technique. With this technique an analog input is digitized to a resolution of N bits by a bank of 2^N-1 comparators operating in parallel. These comparators are biased 1 LSB apart by a precision resistor network connected to a voltage reference. With an analog input applied, all comparators biased below the level of the input signal turn on (output "1") while those biased above the input level turn off (output "0"). Since the comparators operate simultaneously, the quantization takes place in the switching time of a single comparator. For a four bit converter, which requires a bank of 15 comparators, the results of this quantization appear in the form of a 15 line code which increments sequentially from all zeros to all ones. This result is fed to a special 15 line to 4 bit decoder, whose output is a 4 bit binary code.

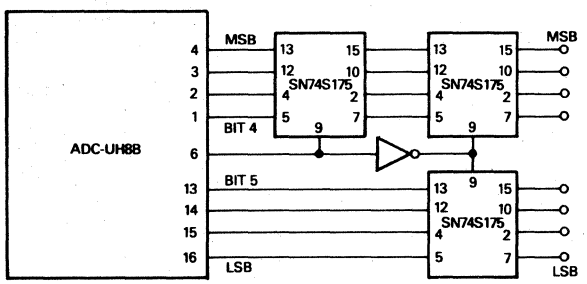
To achieve high speed 8 bit conversions, the above technique is used in a two stage operation. The first quantization stage determines the four most significant bits. This four bit word is then stored in an output register that also controls a 4 bit digital-to-analog converter. The output of the D/A coverter is the analog value of the four most significant bits, which is then subtracted from the analog input. The resulting voltage difference is fed to a second comparator bank where the four least significant bits are determined and stored in a second output register. The contents of the two output registers is the 8 bit binary word representing the analog input signal level.

A useful result of this two stage method is that once the four most significant bits have been determined and stored in the output register, the first stage comparator bank is free to perform the next conversion. The second conversion will begin while the remaining four bits of the original conversion are being determined in the second stage (refer to the timing diagram for the dynamics of interleaved two-stage conversion). This mode of operation makes possible an 8.33 MHz word rate.

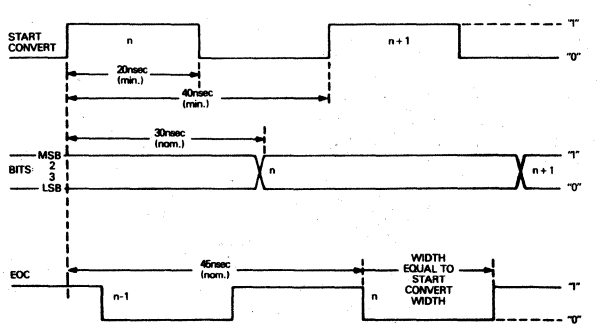
MODEL ADC-UH4B BLOCK DIAGRAM



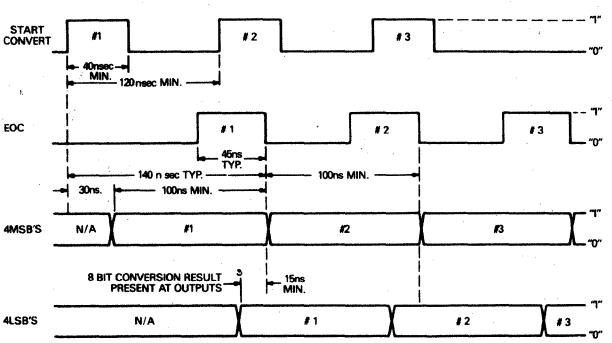
TWO-STAGE DATA TRANSFER REGISTER FOR ADC-UH8B



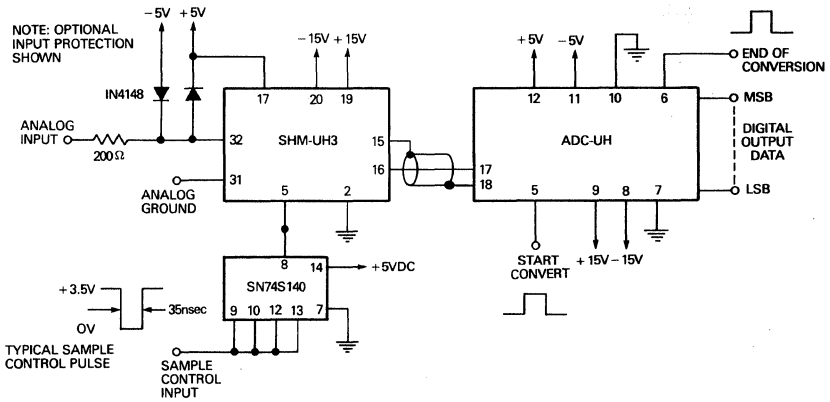
ADC-UH4B TIMING DIAGRAM



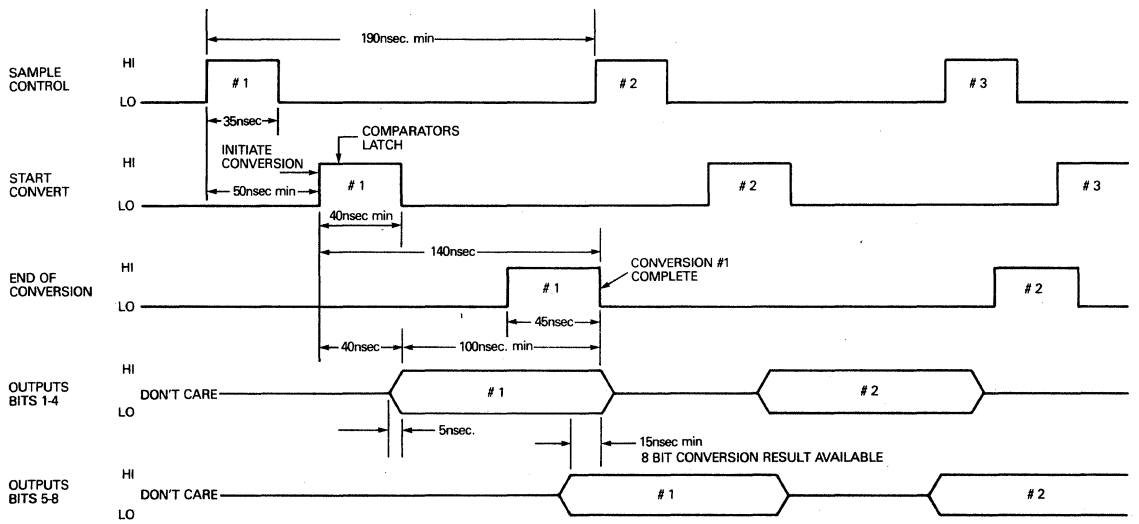
ADC-UH8B TIMING DIAGRAM



SHM-UH3 AND ADC-UH8B CONNECTION



ADC-UH8B/SHM-UH3 TIMING DIAGRAM



CODING TABLES

ADC-UH8B CODING TABLE

CONVERTER SCALE	ANALOG INPUT VOLTAGE	STRAIGHT BINARY OUTPUT CODE
-F.S. + 1LSB	-2.550V	11111111
-¾F.S.	-1.920V	11000000
-½ F.S.	-1.280V	10000000
-¼ F.S.	-0.640V	01000000
1 LSB	-0.010V	00000001
0	0.00V	00000000

ADC-UH8B2 CODING TABLE

CONVERTER SCALE	ANALOG INPUT VOLTAGE	OFFSET BINARY OUTPUT CODE
-F.S. + 1 LSB	-1.270V	11111111
-½ F.S.	-0.640V	11000000
-1 LSB	-0.010V	10000001
0	0.000V	10000000
+½ F.S.	+0.640V	01000000
+F.S.	+1.280V	00000000

ADC-UH4B2 CODING TABLE

CONVERTER SCALE	ANALOG INPUT VOLTAGE	OFFSET BINARY OUTPUT CODE
-F.S. + 1 LSB	-1.120V	1111
-½ F.S.	-0.640V	1100
-1 LSB	-0.160V	1001
0	0.000V	1000
+½ F.S.	+0.640V	0100
+ F.S.	+1.280V	0000

ADC-UH4B CODING TABLE

CONVERTER SCALE	ANALOG INPUT VOLTAGE	STRAIGHT BINARY OUTPUT CODE
-F.S. + 1 LSB	-2.400V	1111
-¾ F.S.	-1.920V	1100
-½ F.S.	-1.280V	1000
-¼ F.S.	-0.640V	0100
-1 LSB	-0.010V	0001
0	0.000V	0000

DATEL INTERSIL
11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617)339-9341 / TWX 710-346-1953 / TLX 951340
Santa Ana, (714)835-2751, (L.A.) (213)933-7256 • Sunnyvale, CA (408)733-2424 • Gaithersburg, MD (301)840-9490
• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

8 Bit, 20MHz Video Analog-to-Digital Converter Model ADC-TV8B

FEATURES

- **8 Bit Resolution**
- **20 MHz Encoding Rate**
- **Internal Sample Hold**
- **ECL or TTL Interfacing**
- **Hybrid Building Block Design**

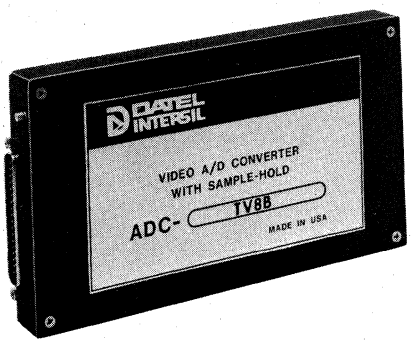
GENERAL DESCRIPTION

The ADC-TV8B is an 8 bit video analog to digital converter employing a unique new design concept. The circuit realization is based on a hybrid building block principle using four specially developed circuits: a 3-bit parallel decoded A/D, a 15 line (4 bit) D/A, an ultra-fast sample-hold, and an ultra-fast inverting op amp. These devices, manufactured with thin-film hybrid technology, are combined with other digital and analog IC's, in addition to passive components to construct the ADC-TV8B. This building block principle results in single circuit board construction in a compact, anodized aluminum module only 7.5 x 4.25 x 0.875 inches (191 x 108 x 22mm).

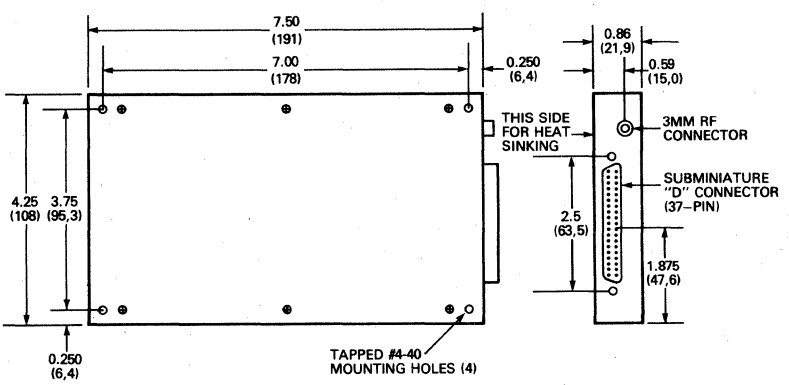
Digital and power connections are made through a 37-pin subminiature "D" connector and the analog input is a 3mm terminated coax connector. Ultra-fast 10,000 series ECL logic is used throughout the design, but there is a choice of two external logic interfaces: ECL or TTL. There is a further choice in analog input termination impedances of 50, 75, or 93 ohms and analog input ranges of 0 to +1V, 0 to +2V, 0 to +5V, ±1V, ±2V, or ±5V. These choices are made by selecting the appropriate converter model number.

The time between conversions is 50 nsec. maximum, giving a conversion rate of 20 MHz. The conversion delay, or time from the start convert pulse to the time data is valid, is 65 nsec. for the ECL version and 75 nsec. for the TTL version. Linearity error is ±½ LSB maximum, and there are no missing codes over the operating temperature range. Temperature coefficient is ±60 ppm/°C of full scale range.

Power requirement is ±15VDC and ±5VDC at 16 watts consumption. Operating temperature range is 0°C to 70°C.



MECHANICAL DIMENSIONS-INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	E.O.C. (ECL)*	14	$\overline{\text{BIT 3}}$ OUT **	26	POWER COMMON
2	START CONV. (ECL)	15	$\overline{\text{BIT 4}}$ OUT	27	−5V POWER
3	START CONV. (TTL)	16	$\overline{\text{BIT 5}}$ OUT **	28	−15V POWER
4	N.C.	17	$\overline{\text{BIT 6}}$ OUT **	29	N.C.
5	+15V POWER	18	$\overline{\text{BIT 7}}$ OUT **	30	BIT 1 OUT*
6	+5V POWER	19	$\overline{\text{BIT 8}}$ OUT **	31	BIT 2 OUT*
7	POWER COMMON	20	$\overline{\text{E.O.C.}}$ (ECL)*	32	BIT 3 OUT*
8	POWER COMMON	21	$\overline{\text{START CONV.}}$ (ECL)	33	BIT 4 OUT*
9	−5V POWER	22	TTL COMMON	34	BIT 5 OUT*
10	−15V POWER	23	+15V POWER	35	BIT 6 OUT*
11	N.C.	24	+5V POWER	36	BIT 7 OUT*
12	$\overline{\text{BIT 1}}$ OUT **	25	POWER COMMON	37	BIT 8 OUT*
13	$\overline{\text{BIT 2}}$ OUT **	COAX CONNECTOR: ANALOG INPUT			

*Output for ECL or TTL models.
**ECL outputs present on all models.

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, ADC-TV8B (Typical at 25°C, ±15V and ±5V supplies, after 5 minutes warmup, unless otherwise noted.)

MAXIMUM RATINGS

Analog Supply Voltage, pins 5&23, 10&28	±18V
Logic Supply Voltage, pins 6&24, 9&27	±5.5V
ECL Logic Inputs, pins 2&21	0V, −5V
TTL Logic Input, pin 3	+5.5V
Analog Input Voltage	±15V

INPUTS[1]

Analog Input Range[2], unipolar	0 to +1V, 0 to +2V, 0 to +5V
Analog Input Range[2], bipolar	±1V, ±2V, ±5V
Input Impedance[2]	50, 75, or 93 ohms.
Start Conversion, ECL[7]	Complementary ECL 10,000 input pulses, 15 nsec. min. Conversion initiated on leading edge. Negative going pulse to pin 2.
Start Conversion, TTL	Positive going pulse, 15 nsec. min +0.8V max. to +2.0V min. levels. 50 ohms input impedance. Conversion initiated on leading edge.

OUTPUTS[1]

Parallel Output Data, ECL	8 pins of parallel lines, complementary ECL 10,000. Valid after E.O.C. pulse.
Loading	20 ECL loads
Skew[3]	< 2 nsec.
Parallel Output Data, TTL	8 parallel lines of data, valid after E.O.C. pulse. Vout ("0") ≤ +0.4 Vout ("I") ≥ +2.4V
Loading	10 TTL loads
Skew[3]	<5 nsec.
Coding, unipolar[4]	Straight binary
Coding, bipolar[4]	Offset binary
End of Conversion, ECL	Complementary ECL 10,000. 20 nsec. pulse after which data is valid.
Loading	20 ECL loads
End of Conversion, TTL	20 nsec. positive pulse after which data is valid.
Loading	10 TTL loads.

PERFORMANCE

Resolution	8 bits (1 part in 256)
Linearity Error	± ½ LSB max.
Conversion Delay, ECL	65 nsec.
Conversion Delay, TTL	75 nsec.
Time Between Conversions	50 nsec. min.
Max. Conversion Rate	20 MHz
Sample Hold Bandwidth	10 MHz
Sample Hold Acquisition Time	25 nsec.
Aperture Uncertainty	<30 psec.
Temperature Coefficient	±60 ppm/°C of FSR[5]
Missing Codes	None over oper. temp. range.
Signal to Noise Ratio, DC to 5 MHz	50 dB
Long Term Stability	±0.15% per year

POWER REQUIREMENTS

±15VDC ±0.75V at 200 mA
+5VDC ±0.25V at 0.5A[6]
-5VDC ±0.25V at 1.5A

PHYSICAL-ENVIRONMENTAL

Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−55°C to +85°C
Relative Humidity	Up to 100% non-condensing
Size	7.5 x 4.25 x 0.875 inches 191 x 108 x 21,9 mm.
Type Case	Black Anodized Aluminum.
Weight	16 oz. (454 g.)

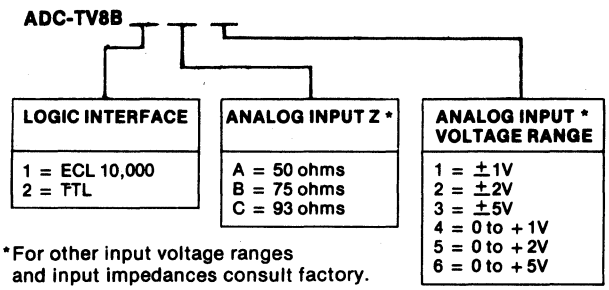
NOTES:

1. ECL or TTL interface is determined by model number.
2. Input ranges and impedances are determined by model number.
3. Skew is defined as the maximum difference between times that any two bits change.
4. Determined by number.
5. Full scale range, or the difference between high ahd low ends of the input range.
6. For TTL model this current is 0.7 A.
7. Use of pin 21 for complementary drive is optional.

TECHNICAL NOTES

1. Note that there are two basic models of the ADC-TV8B: one for ECL interfacing (ADC-TV8B1) and one for TTL interfacing (ADC-TV8B2). The former is designed for complementary series 10,000 ECL interfacing and can be conveniently used with ECL differential line drivers and receivers. The latter model uses standard TTL interface levels.
2. The ADC-TV8B1 dissipates 16 watts while the ADC-TV8B2, which draws slightly higher +5V supply current, dissipates 17 watts. It is recommended in general that one side of the package (see Mechanical Dimensions) be mounted against a metal heat sink such as chassis. Internal components are heat sinked to this side of the package and there are tapped #4-40 mounting holes for this purpose.
3. The analog input coax connector is a standard 3mm RF connector (mating part, Sealectro Corp. part no. 51-024-0000). The mating part to the subminiature "D" connector is Cinch type DC37S.
4. Each power supply connection has two pins connected in parallel. It is recommended that both of these pins be used in all cases. There is no requirement to bypass the power supply leads in most cases since this is done internally.
5. The ADC-TV8B does not require any external adjustments. All adjustments have been made at the factory and after an initial 5 minute warm-up period, the unit will perform to specification.
6. The ECL model can be operated with a single start convert pulse applied to pin 2. The complementary input may be used in addition to improve noise immunity. If the start convert pulse, for either ECL or TTL versions remains HI longer than 35 nsec., the samplehold will remain in the hold mode for the duration of the start convert pulse.

ORDERING INFORMATION



*For other input voltage ranges and input impedances consult factory.

PRICING

Model	Logic Interface
ADC-TV8B1	ECL
ADC-TV8B2	TTL

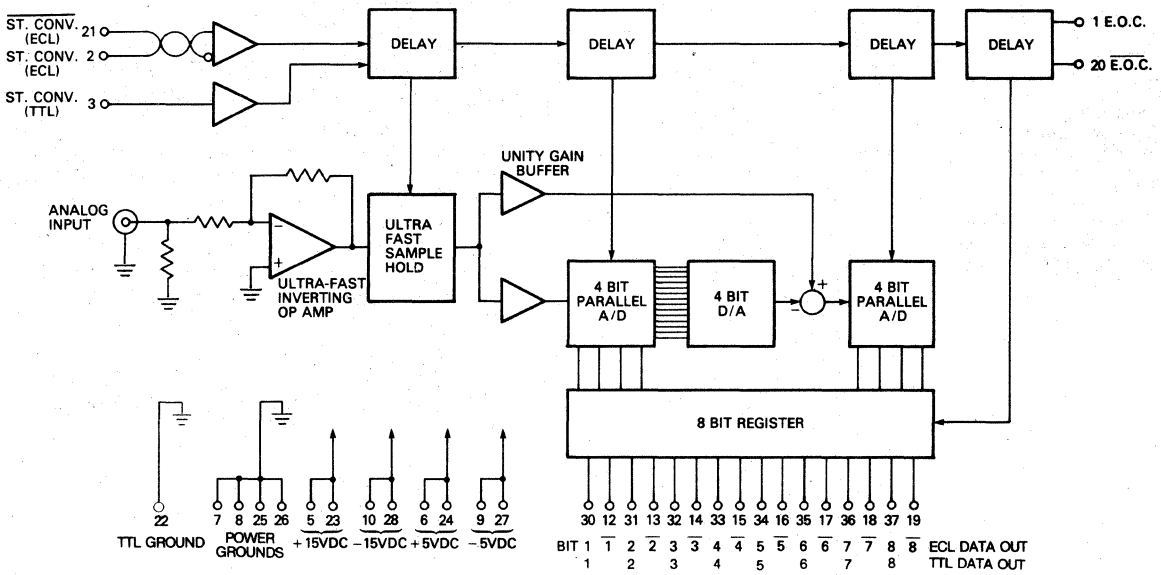
The following mating connectors are supplied with ADC-TV8B: TRW Cinch DC37S
Sealectro 51-024-0000

For extended temperature range operation the following suffixes are added to the model number. Consult factory for price and delivery.

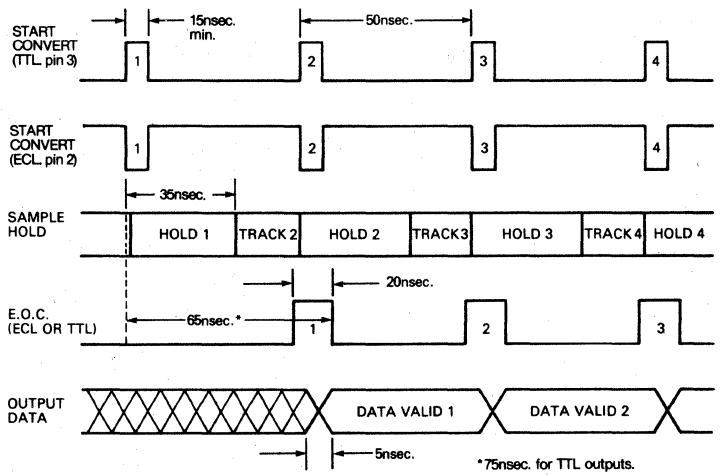
-EX	−25°C to +85°C operation
-EXX-HS	−55°C to +85°C operation with hermetically sealed semiconductor components.

THE ADC-TV8B IS COVERED BY GSA CONTRACT

BLOCK DIAGRAM



TIMING DIAGRAM



DESCRIPTION OF OPERATION

The ADC-TV8B A/D converter employs a two step parallel conversion technique illustrated by the block diagram and timing diagram. Each of the 4 bit parallel A/D converters shown is made up of two 3 bit hybrid expandable A/D's.

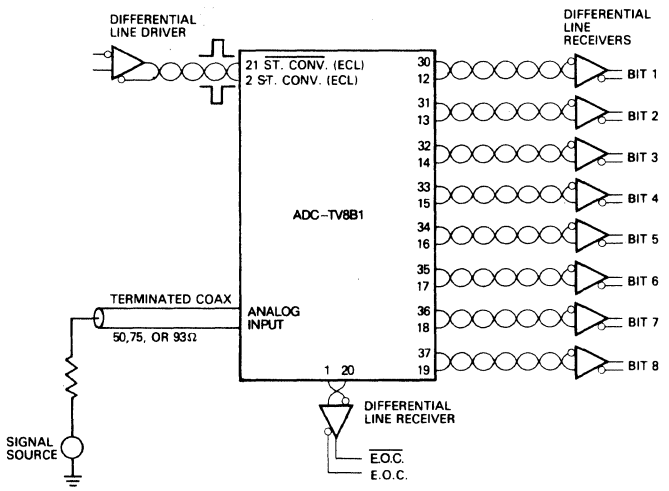
The analog input comes from a terminated RF connector to an ultra-fast inverting op amp which scales the input to the desired level for the sample-hold and A/D converter. A conversion is initiated by an input start convert pulse which begins a timing sequence determined by 4 ECL digital delay circuits. The first delay causes the sample-hold to go from the tracking mode to the hold mode for about 35 nanoseconds. The output of the sample-hold is buffered and goes to the first 4 bit A/D where the 4 most significant bits are converted and decoded into binary form. This A/D simultaneously drives a 4 bit D/A by means of a 15 line output.

The D/A output is subtracted from the buffered sample-hold output and the analog remainder goes to the second 4 bit A/D which converts the 4 least significant bits into decoded binary form. The last delay circuit puts out a 20 nsec. pulse indicating that data is ready at the output of the 8 bit register.

The delay for a conversion is 65 nanoseconds for ECL outputs and 75 nanoseconds for TTL outputs. This is the time measured from the leading edge of the start convert pulse to the trailing edge of E.O.C. (or status) pulse. The time between successive conversions, however, is only 50 nanoseconds max. giving a conversion rate of 20 MHz.

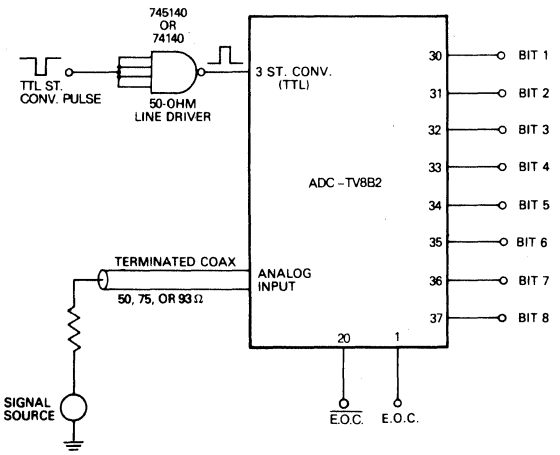
APPLICATIONS

ECL SERIES 10,000 INTERFACING



NOTE: $\overline{\text{START CONVERT}}$ CONNECTION TO PIN 21 IS OPTIONAL FOR IMPROVED NOISE IMMUNITY.

TTL INTERFACING



CODING TABLES

UNIPOLAR MODELS

INPUT VOLTAGE RANGE				
Scale	**0 to +1V**	**0 to +2V**	**0 to +5V**	**Output Code**
+FS −1LSB	+0.996V	+1.992V	+4.998V	1111 1111
+¾FS	+0.750	+1.500	+3.750	1100 0000
+½FS	+0.500	+1.000	+2.500	1000 0000
+¼FS	+0.250	+0.500	+1.250	0100 0000
+1LSB	+0.004	+0.008	+0.020	0000 0001
ZERO	0.000	0.000	0.000	0000 0000

BIPOLAR MODELS

INPUT VOLTAGE RANGE				
Scale	**±1V**	**±2V**	**±5V**	**Output Code**
+FS −1LSB	+0.992V	+1.984	+4.961V	1111 1111
+½FS	+0.500	+1.000	+2.500	1100 0000
ZERO	0.000	0.000	0.000	1000 0000
−½FS	−0.500	−1.000	−2.500	0100 0000
−FS+1LSB	−0.992	−1.984	−4.961	0000 0001
−FS	−1.000	−2.000	−5.000	0000 0000

DIGITIZING VIDEO SIGNALS

The most widely used digital standard found in digital video circuits involves an encoding rate based on 8 bits/sample at a sample rate of 3X or 4X the subcarrier. The ADC-TV can meet or exceed these conversion rates.

STANDARD	COLOR SUBCARRIER FREQUENCY (MHZ)	3X (MHZ)	4X (MHZ)
NTSC	3.58	10.74	14.32
PAL	4.43	13.29	17.72

For a NTSC or PAL signal, the subcarrier can extend from −33 to +133 IRE units, reference blanking level. Keep in mind that 1 IRE = 7.14 mV. To calculate the *least significant bit* (LSB) size, the following formula applies:

$$1\ \text{LSB} = \frac{166}{256} = .648\ \text{IRE units on 4.63 mV.}$$

where 166 IRE is the full scale range* and 256 is the number of steps in an 8 bit A/D.

Differential linearity is the maximum deviation of an actual bit size from its theoretical value for any bit over the full range of the converter. If the differential linearity is 1 LSB or greater, missing codes will appear on the A/D output. The ADC-TV is guaranteed not to miss codes over the entire operating temperature range.

*The ADC-TV can be supplied to this input range.

THERMAL MANAGEMENT

Circuit performance and long-term circuit reliability are affected by the junction temperature of the internal IC's. Normally, both are improved by keeping these junctions at a low temperature.

The ADC-TV has been designed to operate at case temperatures of 0 to 70°C. It is recommended that the converter not be operated outside this range.

The average junction temperature is dependent on the amount of power dissipation and the net thermal resistance between the heat source and a reference point. In this case, we have already determined that the case temperature is the reference point.

Controlled air flow over the case or a heat sink are effective means of reducing the ADC-TV's temperature. An air flow of 500 linear feet per minute is recommended especially when operating the unit with cooling air temperatures up to 50°C. A heat sink should be mounted on the side noted in the mechanical dimensions.

Care must be taken when mounting the device on a heat sink. To assure efficient heat transfer from case to heat sink when mounting the ADC-TV, the following special precautions should be observed:

1. Mounting torque should be between 4 and 8 inch-pounds.
2. The mounting holes should be kept small and free of burrs and ridges.
3. The mounting surface should be flat.
4. Thermal Joint Compound (Wakefield Engineering Type 120 or equivalent) should be used.
5. A lock washer or torque washer, made of material having sufficient creep strength should be used to prevent degradation of heat sink efficiency during life.

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14 Bit, 50 Microsecond Analog-to-Digital Converter Model ADC-149

FEATURES

- **14 Bit Resolution**
- **50 μsec. Conversion Time**
- **Low Price**
- **Unipolar or Bipolar Inputs**
- **15ppm/°C Gain Temp. Coeff.**

GENERAL DESCRIPTION

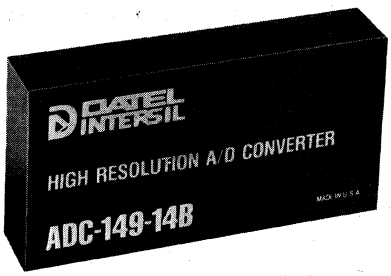
The ADC-149 is a 14 bit successive approximation type analog to digital converter for OEM use. It was specifically designed to give high resolution and accuracy at moderate cost for incorporation into precision instruments for process control systems and test and measurement systems.

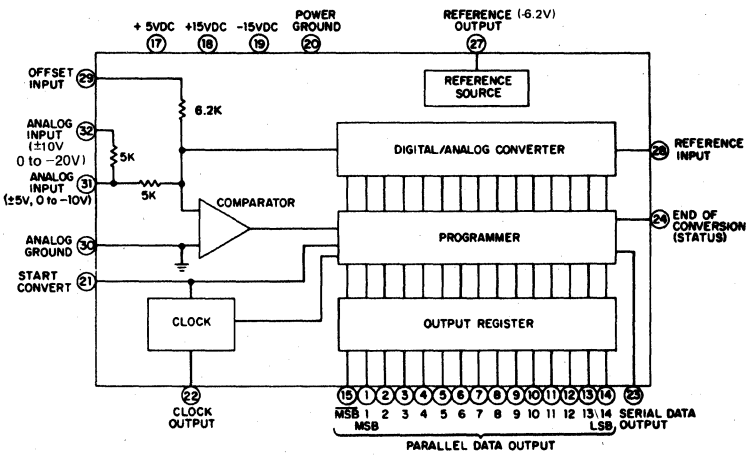
This converter accepts either unipolar or bipolar input voltages of 0 to −10V, 0 to −20V, ±5V, or ±10V full scale by external pin connection and performs a 14 bit conversion in 50 μsec. Several output codes are available including straight binary for unipolar inputs and either offset binary or two's complement for bipolar inputs. Two's complement is obtained by using the $\overline{\text{MSB}}$ output pin. Reverse coding sense is used with the most negative analog input corresponding to full scale digital output. A serial data output is also provided and has a nonreturn-to-zero (NRZ) format. Logic outputs ate DTL/TTL compatible and will drive 6 standard TTL loads.

The ADC-149 can resolve 1 part in 16,384 giving an operating dynamic range of 84.3dB. On the 10 volt full scale range it can detect an input change of less than 1 millivolt. Accuracy is adjustable to ±.005% of full scale ±½LSB. The temperature coefficient is held to a low ±15ppm/°C over the 0° to 70°C operating temperature range.

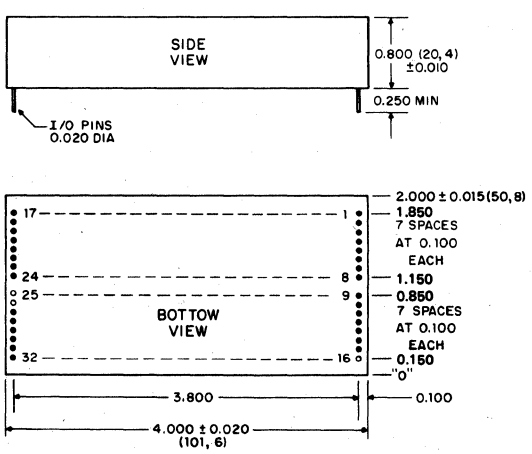
This converter is encapsulated in a compact 2X4X0.8 inch module with DIP compatible pin spacing for PC board mounting. It can be stored from −55°C to +85°C. Power supplies required are standard ±15VDC and +5VDC. (Available from Datel's line of modular power supplies.)

The high resolution and accuracy of the ADC-149 make it particularly valuable in applications such as moderate speed data reduction, and computer arithmetic processing of analog inputs. Digitizing inputs from sensors and transducers allows data transmission or storage with drastically reduced degradation of accuracy compared to analog methods. This is also vital for automatic process and alarm limit computer control, and digital linearization of logarithmic or special function analog inputs.





MECHANICAL DIMENSIONS INCHES (MM)



NOTES:
1. OPEN HOLES DESIGNATE WHERE PINS ARE OMITTED

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	BIT 1 (MSB)
2	BIT 2
3	BIT 3
4	BIT 4
5	BIT 5
6	BIT 6
7	BIT 7
8	BIT 8
9	BIT 9
10	BIT 10
11	BIT 11
12	BIT 12
13	BIT 13
14	BIT 14 (LSB)
15	BIT 1 (MSB)
16	NOT USED
17	+5V POWER
18	+15V POWER
19	−15V POWER
20	POWER GROUND
21	START CONVERT
22	CLOCK OUTPUT
23	SERIAL OUTPUT
24	END OF CONVERT (STATUS)
25	NOT USED
26	NOT USED
27	REFERENCE OUTPUT
28	REFERENCE INPUT
29	OFFSET INPUT
30	ANALOG GROUND
31	ANALOG IN (0 to +10, ±5V)
32	ANALOG IN (±10V)

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SPECIFICATIONS (Typical @ +25°C unless noted)

INPUTS

Analog Input Range (single-ended input referenced to ground) ..... ±5V FS, ±10V FS
0 to -10V FS, 0 to -20V FS

Input Overvoltage ..... ±15VDC without damage to unit.

Input Impedance ..... 5K Ohms (±5V and 0 to -10V FS range)
10K Ohms (±10V and 0 to −20V FS range)

Start of Conversion ..... +2.5V min. to +5.5V max. positive pulse with 150 nsec. min. duration.
Loading: 1mA
Logic "1" resets converter
Logic "0" initiates conversion

OUTPUTS

Parallel Output Data ..... 14 parallel lines of data held until the next conversion command.
Vout (Logic "0") ⩽ +0.4V
Vout (Logic "1") ⩾ +2.4V
Each output capable of driving up to 6 TTL loads.

Coding ..... Straight Binary (Unipolar Input)
Offset Binary (Bipolar Input)
Two's Complement (Bipolar Input)
Pin 15 provides MSB output for this coding. (Reverse coding sense used).

Serial Output ..... NRZ successive decision pulse output generated during conversion with MSB first. LO = "1", HI = "0"
Straight binary or offset binary coding

End of Conversion ..... Conversion Status Signal
Vout (Logic "0") ⩽ +0.4V conversion complete
Vout (Logic "1") ⩾ +2.4V during reset and conversion period.

Clock ..... Internal clock output, positive going 3 microsecond pulse. Loading up to 6 TTL loads.

PERFORMANCE

Resolution ..... 14 Bits (one part in 16,384)
Linearity Error ..... ±½ LSB max.
Temperature Coefficient of Gain ..... ±15ppm/°C
Temperature Coefficient of Zero Unipolar ..... ±10ppm/°C
Bipolar ..... ±10ppm/°C
Conversion Time ..... 50μsec. max.
Throughput Rate 20kHz
Power Requirements ..... ±15VDC ±0.5VDC @ 80mA max.
+5VDC ±0.25 VDC @ 200mA max.

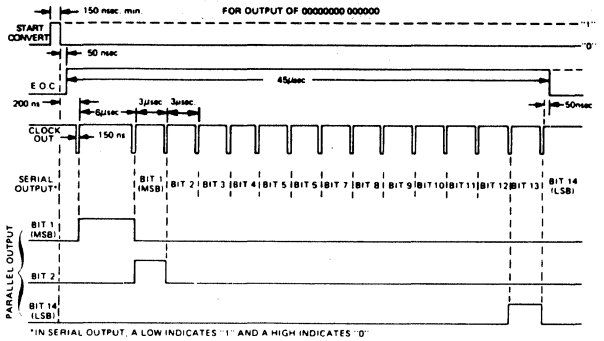
PHYSICAL-ENVIRONMENTAL

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range −55°C to +85°C
Relative Humidity ..... Up to 100% non-condensing
Size ..... 2"W×4"L×0.8" H
Pins ..... .020" round, gold plated, 0.250" long min.
Case Material ..... Black Diallyl Phthalate per MIL-M-14
Weight ..... 8 oz.
Mating Sockets ..... DILS-2, 2 required @ $6/pair

ORDERING INFORMATION

Model ADC-149-14B
Mating Socket DILS 2

TIMING FOR ADC-149-14B



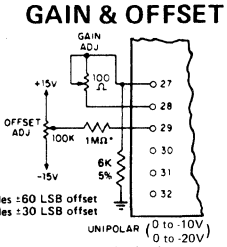
*IN SERIAL OUTPUT, A LOW INDICATES "1" AND A HIGH INDICATES "0"

OUTPUT DIGITAL CODING

BIPOLAR						UNIPOLAR		
Analog Input Range		Offset Binary		2's Complement (MSB Output)		Analog Input Range 0 to	Straight Binary	
±5V FS	±10V FS	MSB	LSB	MSB	LSB	10V FS	MSB	LSB
+5.0000	+10.0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0		1 0 0 0 0 0 0 0 0 0 0 0 0 0		0 0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0	
+2.5000	+ 5.0000	0 1 0 0 0 0 0 0 0 0 0 0 0 0		1 1 0 0 0 0 0 0 0 0 0 0 0 0		0 0006	0 0 0 0 0 0 0 0 0 0 0 0 0 1	
+0.0006	+ 0.0012	0 1 1 1 1 1 1 1 1 1 1 1 1 1		1 1 1 1 1 1 1 1 1 1 1 1 1 1		2.5000	0 1 0 0 0 0 0 0 0 0 0 0 0 0	
0.0000	0.0000	1 0 0 0 0 0 0 0 0 0 0 0 0 0		0 0 0 0 0 0 0 0 0 0 0 0 0 0		5.0000	1 0 0 0 0 0 0 0 0 0 0 0 0 0	
−2.5000	− 5.0000	1 1 0 0 0 0 0 0 0 0 0 0 0 0		0 1 0 0 0 0 0 0 0 0 0 0 0 0		7.5000	1 1 0 0 0 0 0 0 0 0 0 0 0 0	
−4.9994	− 9.9988	1 1 1 1 1 1 1 1 1 1 1 1 1 1		0 1 1 1 1 1 1 1 1 1 1 1 1 1		9.9994	1 1 1 1 1 1 1 1 1 1 1 1 1 1	

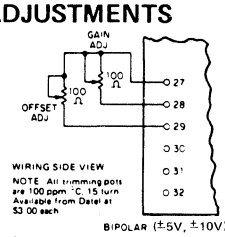
NOTE: *Reverse coding sense is used with the most negative analog input corresponding to full scale digital output. Normal coding sense can be obtained by using an external inverting amplifier. Or complementary binary can be used by adjusting for a 1 LSB offset.

GAIN & OFFSET ADJUSTMENTS



*1MΩ provides ±60 LSB offset
2MΩ provides ±30 LSB offset

UNIPOLAR (0 to -10V / 0 to -20V)



BIPOLAR (±5V, ±10V)

Adjustment Procedure – Unipolar Input

A. Connect a precision pulse generator to the "Start Convert" input terminal. See specifications for pulse width and amplitude.
B. Connect a precision voltage reference source to the appropriate analog input terminals. See I/O Connections.

Zero Offset Control

Adjust the voltage output from the reference to minus ½ LSB. Rotate the zero offset control until the LSB output (Least Significant Bit) flickers between logic "zero" and logic "one".

Full Scale Gain Control

Adjust the output from the reference source to full scale minus 1½ LSB. Rotate the gain control until the LSB output (Least Significant Bit) flickers between logic "zero" and logic "one".

Adjustment Procedure – Bipolar Input

A. Connect a precision pulse generator to the "Start Convert" input terminals. See specifications for pulse width and amplitude.
B. Connect a precision voltage reference source to the appropriate analog input terminals. See I/O connections.

Zero Offset Control

Adjust the voltage output from the reference source to plus full scale minus ½ LSB.
Rotate the offset control until the LSB output (Least Significant Bit) flickers between logic "zero" and logic "one".

Gain Control

Adjust the output from the reference source to minus full scale minus 1½ LSB.
Rotate the gain control until LSB output (Least Significant Bit) flickers between logic "zero" and logic "one".

TRIMMING OF 3 MOST SIGNIFICANT BITS (INTERNAL)

The three trimming potentiometers on the side of the module are for periodic adjustment of the three most significant bits. Normally no adjustment of these trims is necessary since they are calibrated at the factory at 25°C. Should readjustment be required for optimum accuracy at a different temperature or to compensate periodically for long term drift, the following procedure should be carefully followed:

1. Adjust external offset and gain as above.
2. Readjust external gain trim and then bits 3, 2, and 1 in accordance with the table below. Adjust so that the output flickers equally between the two codes shown.
3. Readjust external zero or offset and gain.
4. Repeat steps 2 and 3 as necessary.

Input Voltage		Output Code	Adjustment
Unipolar (0 to -10V)	**Bipolar (±5V)**		
-0.625V -1/2 LSB (-0.62531V)	+4.375V -1/2 LSB (+4.37469V)	00010 . . . 01 00010 . . . 00	Gain Trim
-1.25V -1/2 LSB (-1.25031V)	+3.75V -1/2 LSB (+3.74969V)	00100 . . . 01 00100 . . . 00	Trim #3 (Bit 3)
-2.5V -1/2 LSB (-2.50031V)	+2.50V -1/2 LSB (+2.49969V)	01000 . . . 01 01000 . . . 00	Trim #2 (Bit 2)
-5.0V -1/2 LSB (-5.00031V)	0V -1/2 LSB (-0.00031V)	10000 . . . 01 10000 . . . 00	Trim #1 (Bit 1)

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PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Ultra-Fast 16 Bit A/D Converter Model ADC-876

FEATURES

- **16 Bit Resolution**
- **2 μsec Conversion Time**
- **±½ LSB Linearity**
- **±5V Analog Input Range**
- **500 kHz Throughput**
- **Compact 5" × 3" × 0.375" Module**

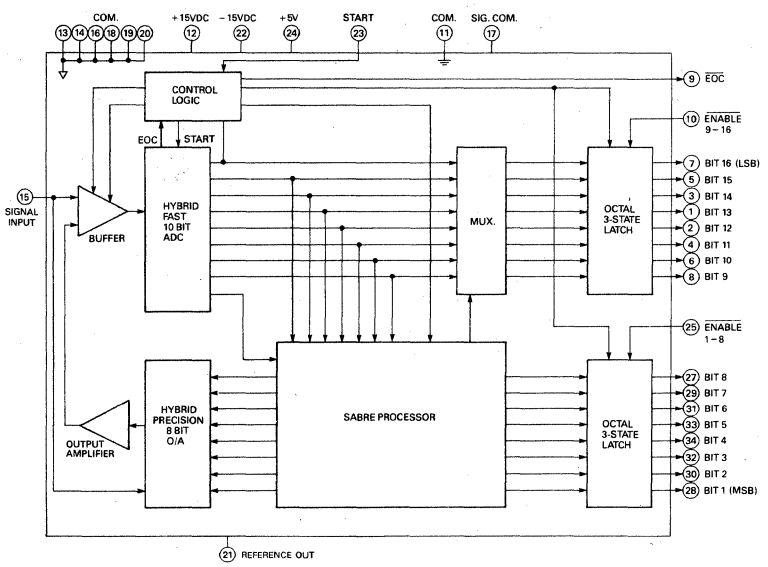
GENERAL DESCRIPTION

The ADC-876 is a 16 bit A/D converter with a maximum conversion time of 2 μsec. This ultra-fast high resolution converter utilizes the SABRE conversion technique, developed by Datel-Insersil (Successive Approximation By Residual Expansion). Although the potential for a unique combination of high speed and high resolution is inherent in this technique, realization of its potential requires real design leadership. As a result, this compact modular A/D has a number of key functions implemented as ultra-high performance thin-film hybrid components. It is these hybrid components that allow the ADC-876 to achieve levels of performance that would be impractical with discrete components.

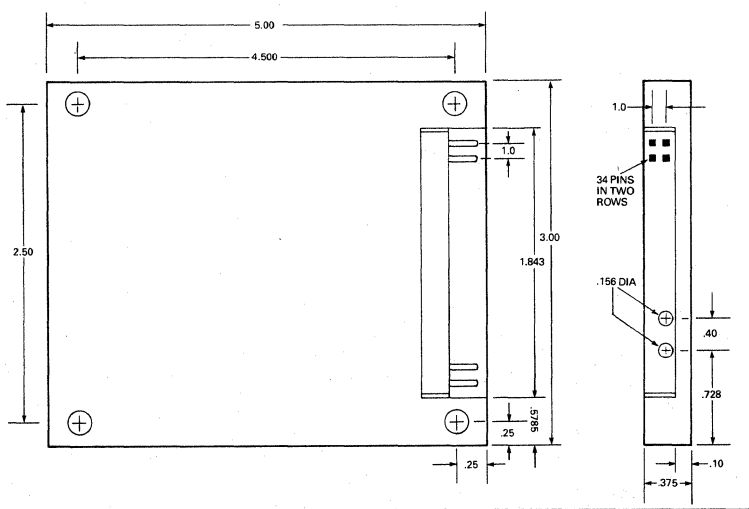
This converter accepts analog inputs over a ±5V range and completes a full 16 bit conversion in 2 μsec maximum, including all set-up, settling and delay times, thus providing a true throughput rate of 500 kHz. The conversion result is coded as complementary two's complement and is latched into the TTL compatible outputs until the next start conversion command.

The ADC-876 features ±½ LSB maximum nonlinearity, ±½ LSB maximum differential nonlinearity, offset drift of only ±1 LSB over the rated operating temperature range and a reference output tempco of ±5 ppm/°C.The 16 bit resolution and ±5V input range yield a LSB size of 152.5 μV.

The converter is housed in a compact 5" × 3" × 0.375" black enameled steel module. A 34 pin AMP connector mounted at one end supplies all interconnect points without extending case size. Each module is functionally complete, requiring only ±15 VDC and +5V supplies for operation, and has an operating temperature range of 0 to +70° C. For information on extended temperature range and high reliability versions, contact the factory.



MECHANICAL DIMENSIONS INCHES



DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

PRELIMINARY SPECIFICATIONS, ADC-876
(Typical at +25°C, ±15 VDC, +5 VDC supplies, unless otherwise noted.)

INPUTS

Analog Input Range	±5V
Input Impedance	1.25KΩ ±20%
Analog Input Step Loading	±0.4mA[1]
Analog Input Source Step Load Recovery Required	≤30 nsec to 0.1% ≤200 nsec to 0.005%, Fo ±0.4mA Step Load
Common Mode Range	±10mV
Common Mode Rejection Ratio	40 dB, Fo ≤ 10MHz
Start Conversion	+2.0V min. to +5.5V max. positive pulse. 25 nsec minimum duration if $\overline{EOC}$ is low when pulse is applied. 125 nsec minimum duration if $\overline{EOC}$ is high when pulse is applied. Loading: 2 LSTTL loads
Enable Inputs[2]	Two inputs, one for bits 1 through 8 and one for bits 9 through 16 control the state of the three state data output registers to allow for 8 bit or 16 bit data bussing. Data is available within 17 nsec of a low state input to the enable controls. Loading: ¼ LSTTL load for each input.

OUTPUTS

Parallel Output Data	16 parallel lines of data. Loading: 20 LSTTL loads in enabled state, and ±50μA max. in disabled state.
Coding	Complementary 2's complement
$\overline{EOC}$ Output	Conversion Status Signal. Normally low, the $\overline{EOC}$ rises 50 nsec max. after the rising edge of the start input and stays high during conversion. The $\overline{EOC}$ falls 15 nsec max. after the new data has been strobed into the data output storage registers, Typ. 3 nsec before data is available at outputs. Loading: 9 LSTTL loads.
Reference Output, Voltage[3]	+10.000V, ±0.010V
, Impedance	≤ 2.0Ω, Fo ≤ 1 MHz
, Noise[4]	≤ 20μV RMS

PERFORMANCE

Conversion Time	2 μsec
Resolution	16 Bits
Nonlinearity	±½ LSB
, Tempco	±1 LSB over Full Rated Operating Temperature Range.
Differential Nonlinearity	±½ LSB
, Tempco	±1 LSB over Full Rated Operating Temperature Range.
Relative Accuracy	±½ LSB
, Tempco	±1 LSB over Full Rated Operating Temperature Range.
Offset Error, Initial	Adjustable to ≤ ½ LSB over a range of 50 LSB.
, Tempco, max.	±1 LSB over Full Rated Operating Temperature.
, Stability	±10 ppm/1000 hrs.
, PSRR, max.	±5 LSB/V.
Gain Error, Initial	Adjustable to ½ LSB over a range of 50 LSB.
, Tempco, max.	±1 LSB, −25°C to +70°C ±25 ppm/°C, +70°C to +85°
, Stability	±25 ppm/1000 hrs
, PSRR, max.	±10 LSB/V
Reference Output Tempco	±5 ppm/°C, −25°C to +70°C ±20 ppm/°C, +70°C to +85°C

PHYSICAL ENVIRONMENTAL

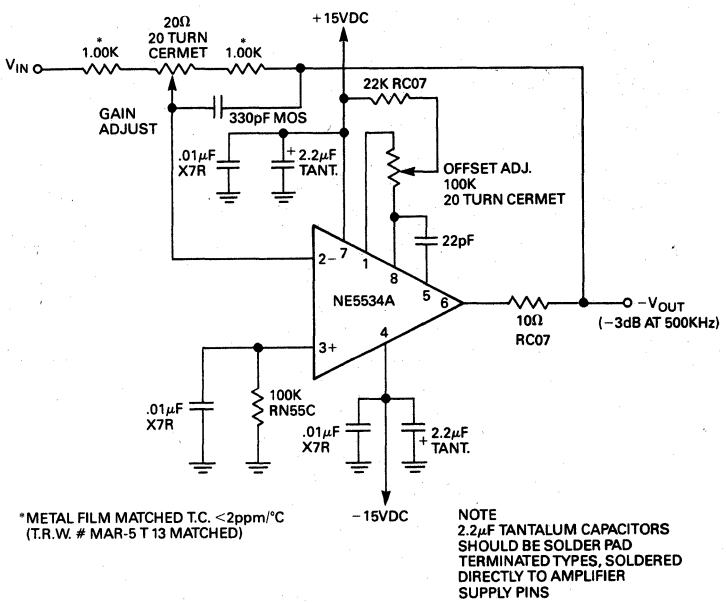
Operating Temperature Range	
ADC-876	0°C to +70°C
ADC-876-EX	−25°C to +85°C
ADC-876-EXX-HS	−25>C to +85°C Hermetic Sealed Semiconductors
Storage Temperature Range	−55°C to +125°C
Package Type[6]	Black enameled 25 gauge CR steel. 5 × 3 × 0.375 in. (127 × 76 × 10 mm).
Weight	6.5 oz (184G).
Connector	34 Pin AMP # 1-86063-3 at one end of case (mating connector supplied) supplies all interconnect points without extending case size.

POWER REQUIREMENTS

Supply Voltage[5]	+15V ±0.5V @ 187mA max. −15V ±0.5V @ 187mA max. +5V ±0.5V @ 472mA max. −5V ±0.5V @ 19mA max.
Power Dissipation, max	8.4 Watts

APPLICATIONS

INPUT BUFFER AMPLIFIER



*METAL FILM MATCHED T.C. <2ppm/°C (T.R.W. # MAR-5 T 13 MATCHED)

NOTE
2.2μF TANTALUM CAPACITORS SHOULD BE SOLDER PAD TERMINATED TYPES, SOLDERED DIRECTLY TO AMPLIFIER SUPPLY PINS

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	Bit 13	18	Power Common
2	Bit 12	19	Power Common
3	Bit 14	20	Power Common
4	Bit 11	21	REFERENCE OUTPUT
5	Bit 15	22	-15V
6	Bit 10	23	START
7	Bit 16 (LSB)	24	+5V
8	Bit 9	25	ENABLE 1-8
9	EOC	26	N.C.
10	ENABLE 9-16	27	Bit 8
11	Common	28	Bit 1
12	+15V	29	Bit 7
13	Power Common	30	Bit 2
14	Power Common	31	Bit 6
15	Signal Input	32	Bit 3
16	Power Common	33	Bit 5
17	Signal Common	34	Bit 4

CODING TABLE

SCALE	INPUT VOLTAGE	OUTPUT CODING COMPLEMENTARY TWO'S COMPLEMENT			
+F.S. -1LSB	+4.99985V	1000	0000	0000	0000
+¾ FS	+3.75000V	1001	1111	1111	1111
+½ FS	+2.5000V	1011	1111	1111	1111
+1 LSB	+0.152mV	1111	1111	1111	1110
0	0.00000V	1111	1111	1111	1111
-½ F.S.	-2.5000V	0011	1111	1111	1111
-¾ F.S.	-3.75000V	0101	1111	1111	1111
-F.S. +1LSB	-4.99985V	0111	1111	1111	1110
-F.S.	-5.00000V	0111	1111	1111	1111

ORDERING INFORMATION

MODEL	DESCRIPTION
ADC-876	2μsec, 16 Bit A/D Converter

For information on extended temperature range versions consult factory

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

SPECIFICATIONS NOTES:

1. At 14.7 MHz during first 1000 nsec of the conversion cycle.
2. For two state operation, tie both enable inputs to digital common.
3. For 0 mA ≤ Tref ≤ 5mA.
4. BW = 10MHz
5. The internal reference heater draws 14mA from the ±15V at +25°C decreasing at 2.5mA/°C and dropping to zero above +70°C. At turn-on, an inrush of 130mA to the heater decays to 15mA in less than 10 seconds.
6. Four 4-40 threaded holes are available on the bottom of the case. It is recommended that the user secure the case to a .032 glass epoxy board or equivalent to help reduce the case temperature resulting from internal power dissipation. Good thermal contact between the case bottom and the circuit board may be established by the use of a silicone thermal joint compound such as Wakefield Type 120 or equivalent.

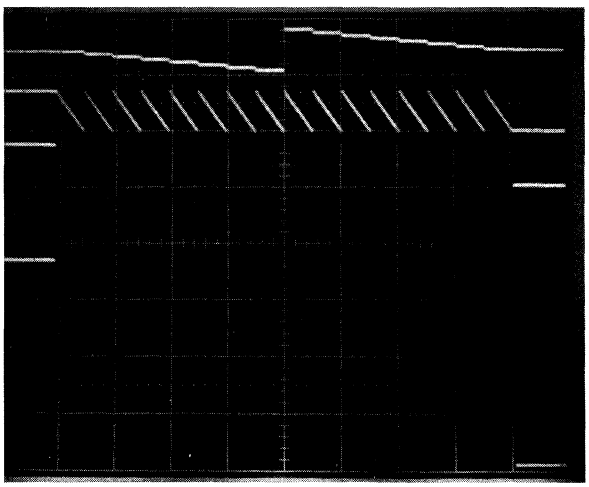


Fig. 1

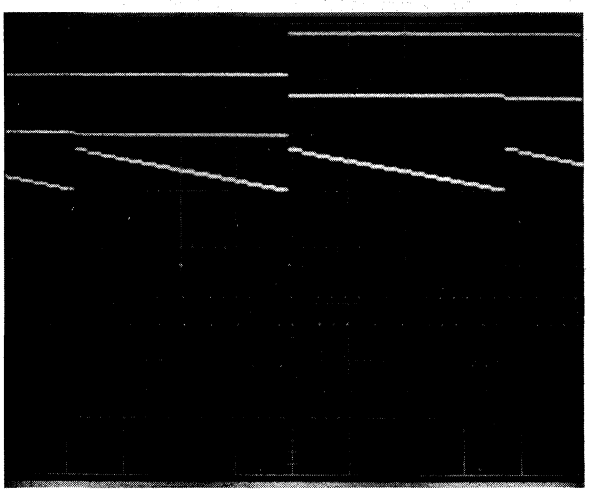


Fig. 2

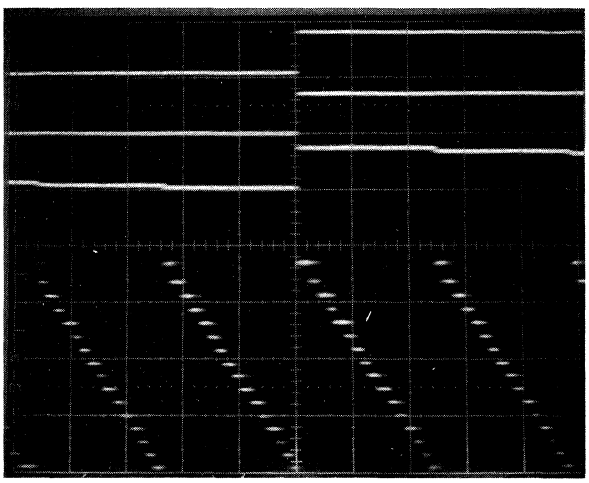
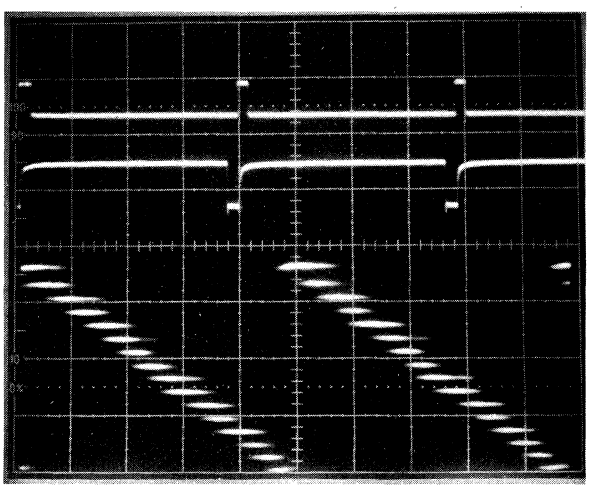


Fig. 3

HIGH SPEED OPERATIONS DISPLAY

This sequence of photos shows the conversion sequence of the ADC-876 SABRE technique. Figure 1 shows the converter operating over it's full scale range at full conversion speed (2 μsec/conversion, max.). Figure 2 shows this expanded to allow viewing bits 13-16, notice that the 4 least significant bits begin to appear. Figure 3 is expanded further to allow viewing the 4 least significant bits. Please note for all these photos the major carry is centered on the centeral vertical grid line.



5V/cm

Fig. 4 500nsec/DIV

CONVERSION, MAXIMUM THROUGHPUT RATE

Fig. 4 shows the start conversion input trace at the top with the EOC shown just below. The bottom trace shows the 4 least significant bits of the ADC-876 at full conversion speed.

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Ultra-Linear 8 Bit A/D Converter Model ADC-881

FEATURES

- **8 Bit Resolution**
- **Statistically Linearized Conversion**
- **12½ Bit Linearity**
- **±15V Input Range**
- **1.5 μsec Conversion Time**
- **Out of Range Indication**

GENERAL DESCRIPTION

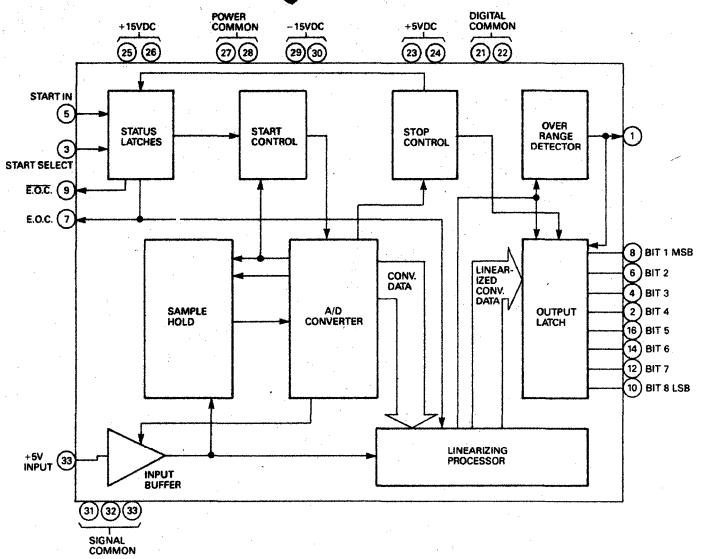
The ADC-881 is an 8 bit analog to digital converter with an internal sample-hold. This converter employs a stochastic distributional technique to enhance the statistical (average) linearity by a factor of 11.2, thus achieving a linearity error of only .0087%. Systematic nonlinearities are scattered in a pseudorandom fashion over the range of the converter, thus appearing as noise rather than nonlinearities. This result is particularly desirable in applications that use the digital output of an A/D converter to compile a histogram. The fundamental properties of any non-distributive A/D converter cause class widths within the histogram to vary from the ideal, thereby artificially increasing or decreasing the frequency within discrete class widths.

This ultra-linear A/D has a wide range of applications in spectrum analysis, nuclear research, vibration analysis, geological research, sonar digitizing, medical imaging systems, industrial testing and other signal analysis applications.

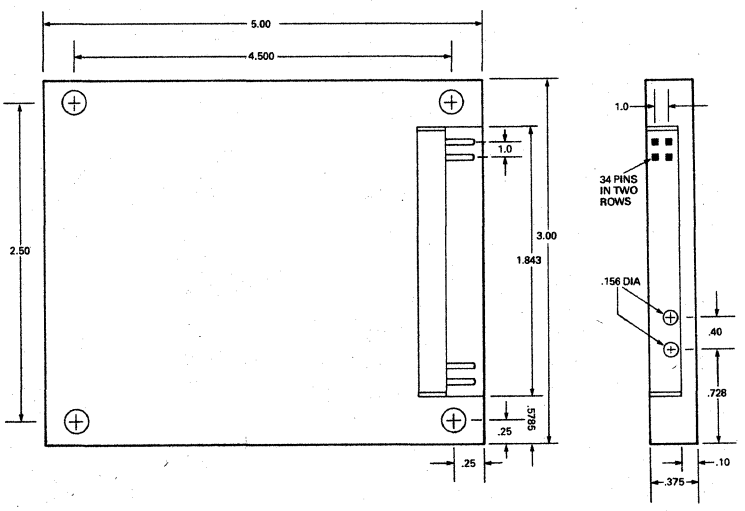
The ADC-881 has an analog input range of ±5V and will accomplish an eight bit sample and conversion in 1.5 μsec maximum. Output data is coded as offset binary with an over range output to indicate analog values out of the converter's range.

Additional specifications include a gain tempco of 30 ppm/°C maximum, offset tempco of 25 ppm/°C maximum, zero crossing tempco of 10 ppm/°C maximum and long term stability of ±0.02%/year.

Each converter is a functionally complete unit requiring only ±15 Vdc and +5V power supplies for operation. The device is packaged in a compact 5" x 3" x 0.375" black enameled steel module. For information on extended temperature range versions contact the factory.



MECHANICAL DIMENSIONS INCHES



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PRELIMINARY SPECIFICATIONS, ADC-881

(Typical at +25°C, ±15 VDC and +5 VDC supplies, unless otherwise noted)

MAXIMUM RATINGS

Positive Supply	+18V
Negative Supply	-18V
Logic Supply	+7V
Digital Supply	+5.5V

INPUTS

Analog Input Range	±5V
Analog Input Impedance	14 KΩ
Start Conversion	A pulse[1] 20 nsec to 80 nsec duration with rise and fall times less than 10 nsec. Logic "0" = 0V to +0.8V. Logic "1" +2.0 to +5.5V. Conversion commences on the leading edge of the pulse. Loading: 1 LSTTL load.
Start Select	For positive start input pulses, set Start Select to a Logic "1" or leave open. For negative start input pulses, set Start Select to a Logic "0" or ground.

OUTPUTS

Parallel Output Data	8 parallel latched data lines - 8 bits binary. V out "0"≤+0.4V, V out "1"≥+2.4V. Loading: 5TTL loads
Coding	Offset Binary
EOC	Conversion Status Signal. High (V out "1" ≥+2.4V) from 32 nsec typical after leading edge of Start Convert to 14 nsec typical after all data outputs are valid. V out "0"≤+0.4V. Loading: 5 TTL loads.
$\overline{\text{EOC}}$	Conversion Status Signal. Complement of $\overline{\text{EOC}}$. Loading: 5 TTL loads
$\overline{\text{Over Range}}$[2]	Out of Range Signal. High (Vout "1"≥+2.4V) for all Signal Input values within ±5V, Low (V out "0"≤+0.4V for all Signal Input values beyond ±5V.

PERFORMANCE

Conversion Time[3], max.	1.5 μsec
Resolution	8 Bits
Integral Linearity Error[4]	0.0087% of FSR
Differential Linearity Error[4]	0.0087% of FSR
Noise (RMS)[5]	0.2% of FSR
Gain Error	Adjustable to zero
Offset Error	Adjustable to zero
Gain Tempco, max.	±30 ppm of FSR/°C
Offset Tempco, max.	±25 ppm of FSR/°C
Zero Crossing Tempco, max.	±10 ppm of FSR/<C
Long Term Stability	±0.02% / year

POWER REQUIREMENTS

Analog Supply	+15V ± 0.5V @ 130mA max. -15V ± 0.5V @ 148mA max.
Logic Supply	+5V ±0.25V @ 481mA max.
Power Dissipation, max.	6.58 Watts.

PHYSICAL ENVIRONMENTAL

Operating Temperature Range	
ADC-881	0°C to +70°C
ADC-881-EX	-25°C to +85°C
ADC-881-EXX-HS	-25°C to +85°C Hermetic Sealed Semiconductors
Storage Temperature Range	-55°C to +125°C
Package Type	Black enameled 25 gauge CR steel. 5 × 3 × 0.375 in. (127 × 76 × 10mm).
Weight	6.5 oz. (184g).
Connector	.025" square pins, gold plated phosphor bronze. Mating connector — supplied — is similar to AMP # 1-85930-1.

NOTES:

1. An alternate method for generating Start Input pulses is to drive the Start Input with a rising edge and the Start Select with a falling edge delayed 20 nsec to 80 nsec.
2. When the Signal Input is less than -5V, the Data Output lines are all "0". When the Signal Input is greater than +5V, the Data Output lines are all "1".
3. Conversion Time is measured from the leading edge of the Start Conversion input to the trailing edge of the $\overline{\text{EOC}}$ output.
4. The Linearity Error is the systematic error which remains after a sufficient number of samples have been averaged to suppress the noise.
5. The RMS noise value is reduced by the second root of the number of samples that have been averaged.

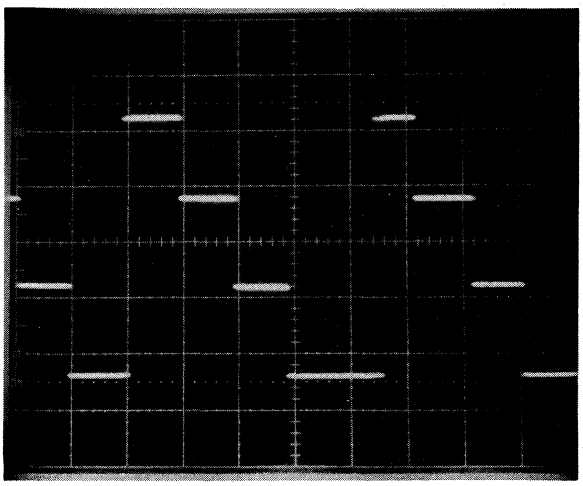


Fig.1 The output of a non-linearized 8 bit A/D converter is shown above. The display shows the 4 least significant bits at the major carry transition, demonstrating differential nonlinearity. This is a property of all non-linearized A/D converters. (The unit used for this example is a typical non-linearized A/D with ±½ LSB of integral linearity and ±½ LSB of differential nonlinearity).

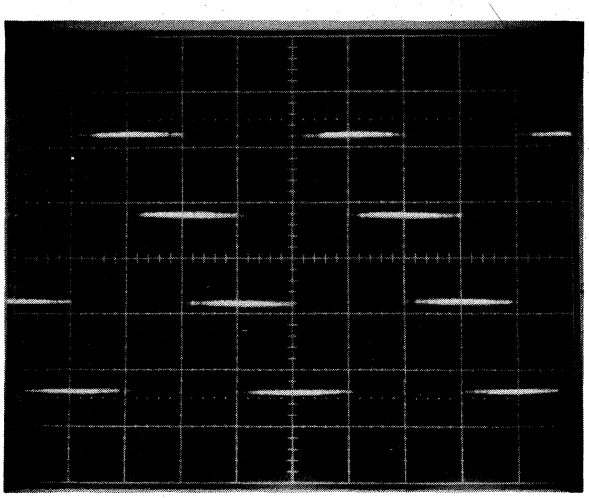


Fig. 2 The output of a linearized 8 bit A/D shown for the 4 least significant bits at the major carry. Notice the improvement in differential nonlinearity. This photo shows the effect of averaging multiple conversions performed with the linearizing technique employed in the ADC-881.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	$\overline{\text{OVER RANGE}}$	18	NC
2	BIT 4	19	NC
3	START SELECT	20	NC
4	BIT 3	21	Digital Common
5	START in	22	Digital Common
6	BIT 2	23	+5VDC
7	EOC	24	+5VDC
8	BIT 1 (MSB)	25	+15VDC
9	$\overline{\text{EOC}}$	26	+15VDC
10	BIT 8 (MSB)	27	Power Common
11	NC	28	Power Common
12	BIT 7	29	−15VDC
13	NC	30	−15VDC
14	BIT 6	31	Signal Common
15	NC	32	Signal Common
16	BIT 5	33	Analog Input
17	NC	34	Signal Common

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
ADC-881	0 to +70°C

For information on extended temperature range and high reliability versions of this product, contact factory.

THIS PRODUCT IS COVERED BY GSA CONTRACT.

The ADC-881 employs a statistically linearized conversion technique that yields unique advantages in many applications. This technique uses a fundamental property of all A/D converters, differential nonlinearity, in a pseudo-random distributional technique to yield a converter with an "ideal" transfer function. This technique scatters the effects of systematic nonlinearities over the full range of the A/D in pseudo-random (a random sequency of finite length) fashion. The average transfer function, taken over the full range of the pseudo-random sequence, has extremely good integral linearity and minimal differential non-linearity. The trade-off appears here as "noisy" codes, this is the result of distributing systemic non-linearities over a wide range. Noise may be suppressed by repeated sampling of the data since the average value of true random noise is zero. The RMS noise value of the data is reduced by the second root of the number of samples less one that have been averaged.

Since this converter's extreme linearity is realized in an average transfer function, it follows that averaging a larger number of conversions will improve linearity. This is true, with maximal linearity resulting as an average of all values within the pseudo-random sequence (127 random values). Since the ADC-881 has conversion times of 1.3 μsec typical and 1.5 μsec maximum, this averaging procedure will require between 165 and 191 μsec (127 conversions x conversion time). In applications where repeated sampling is employed to reduce noise, this converter yields optimal linearity when the number of samples averaged is an integral multiple of 127 (this is inherent in the stochastic distributional technique used).

The largest group of applications for this class of converters is in areas in which recurring systematic nonlinearities have an adverse effect on the distribution of acquired data values. This is particularly of interest in situations where data is required to compile a histogram (a frequency distribution of sample data into discrete categories). The effects of converter nonlinearities cause some categories to be artificially "widened" while others are "narrowed", thus increasing and decreasing, respectively, the frequence of occurrence of data values within these categories. This effect causes a non-linearized converter to yield a "converter distorted" histogram. Until now many users had to resort to extensive computational processing of digitized data simply to minimize the effects of "converter distortion". The architecture of the ADC-881 obviates the need for this, allowing statistically valid processing of analog data in real-time. Thus we see that the ADC-881 is ideally suited for applications in spectrum analysis, particle event monitors, fast signal processing, vibration analysis, sonar digitizing, and a whole spectrum of imaging applications, from medical imaging to industrial non-destructive testing.

CONNECTION AND CALIBRATION

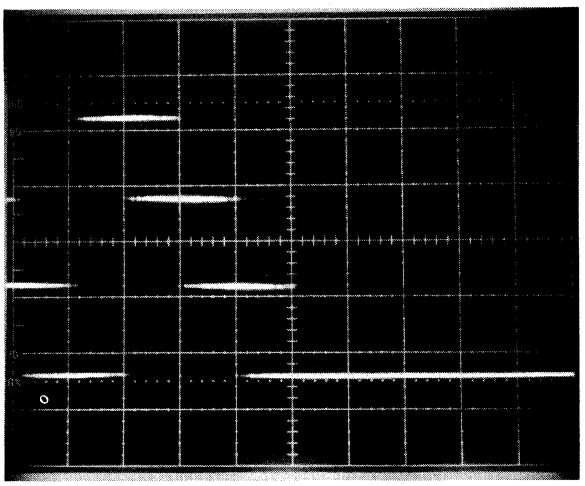


Fig. 3

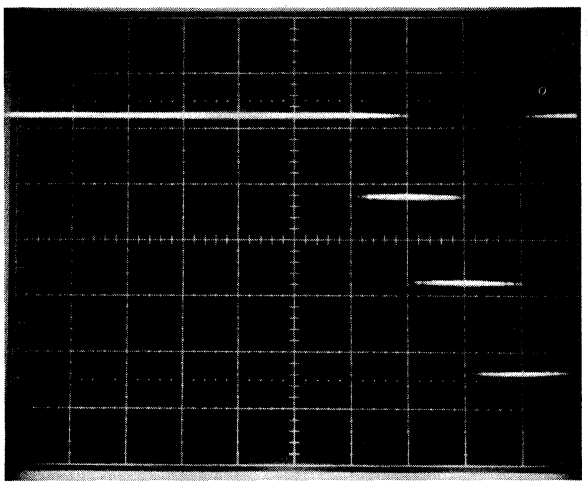
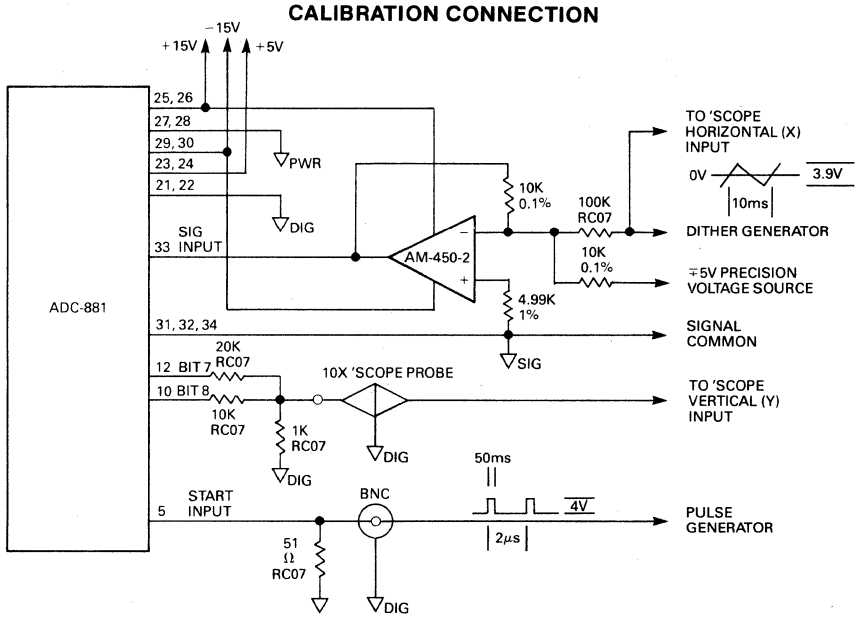


Fig. 4

OFFSET AND GAIN CALIBRATION PROCEDURE

1. Connect A/D to external test circuitry shown in "Calibration Connection" diagram with no power applied.
2. Apply power to the A/D converter and test circuitry and allow them to reach operating temperature.
3. Observe A/D output as a crossplot on the oscilloscope. Calibrate the axis gain for one cm per step and adjust crossplot dither amplitude for 10 cm. Calibrate Y axis for an easily read cross plot.
4. Apply a precision voltage reference set to −5V to the analog input (pin 33). Observe cross plot as shown in figure 3. The last step should be centered on the vertical grid line one cm to the left of center. Adjust offset potentiometer as necessary to achieve this positioning.
5. Set the precision voltage reference to +5V. Observe the cross plot as shown in figure 4. The last step should be centered on the vertical grid line two cm to the right of center. Adjust gain potentiometer as necessary to achieve this position.
6. Repeat steps 4 and 5 until no further adjustment is required. Repetition is necessary, as the offset and gain adjustments interact. The following technique will minimize the number of adjustments. After the initial adjustment outlined in steps 4 and 5, repeat step 4. At this point repeat step 5 but over adjust the gain potentiometer so that the error displayed maintains its initial magnitude but occurs in a direction opposite from its original one, i.e., if the crossplot is 1.5 cm to the left of its desired position, adjust the gain potentiometer so that the crossplot is 1.5 cm to the right of its desired position. Repeat steps 4 and 5, the crossplot should now show perfect position.

CALIBRATION CONNECTION



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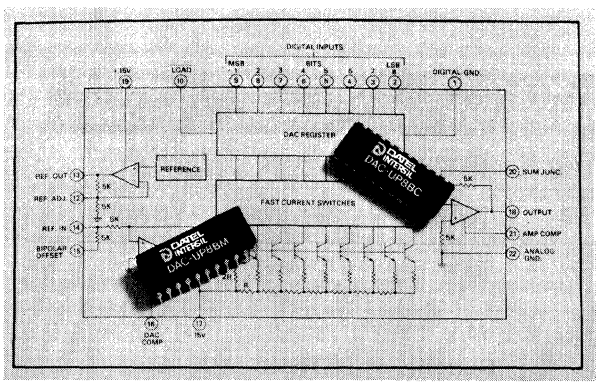
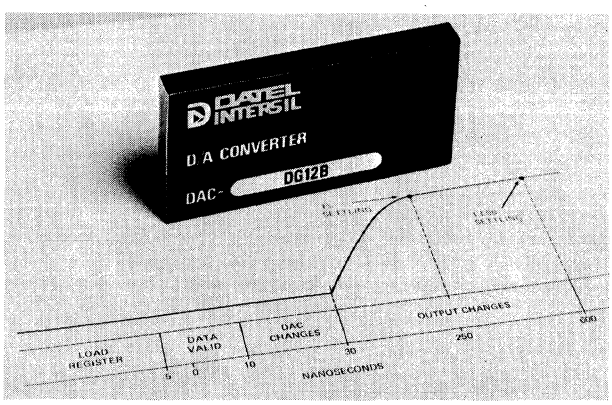
Digital-To-Analog Converters





Quick Selection: General Purpose D/A Converters

	MODEL	DESCRIPTION	RESOLUTION	LINEARITY	OUTPUT	SETTLING TIME, MAX[1]	INPUT CODING[2]
MONOLITHIC	**DAC-IC8BC**	Low Cost 8 bit Monolithic D/A	8 Bits	±½ LSB	Current	300 nsec	Bin
	DAC-IC8BM						
	DAC-08BC	Fast 8 bit Monolithic D/A	8 Bits	±½ LSB	Current	150 nsec	Bin
	DAC-08BM						
	DAC-UP8BC	8 Bit Monolithic with Input Register	8 Bits	±½ LSB	Voltage	2 μsec	Bin
	DAC-UP8BM						
	DAC-IC10BC	Low Cost Fast 10 Bit Monolithic D/A	10 Bits	±1 LSB	Current	250 nsec	Bin
	DAC-IC10B			±½ LSB			
	DAC-IC10BM						
	DAC-681C	12 Bit Monolithic	12 Bits	±½ LSB	Current	400 nsec	Bin
	DAC-681M			±¼ LSB			
HYBRID	**DAC-HZ12BGC**	Low cost with 5 Pin selected Output Voltage Ranges	12 Bits	±½ LSB	Voltage	3 μsec	C Bin
	DAC-HZ12BMC						
	DAC-HZ12BMR						
	DAC-HZ12BMM						
	DAC-HZ12DGC	Low cost with 3 Pin selected Output Voltage Ranges	3 Digits	±¼ LSB	Voltage	3 μsec	BCD
	DAC-HZ12DMC						
	DAC-HZ12DMR						
	DAC-HZ12DMM						

NOTES:

1. For full scale output change to rated accuracy.

2. CODING: Bin = Straight binary or offset binary.
   BCD = Binary coded decimal.
   CBIW = Complementary binary.

OUTPUT RANGES	GAIN TEMPCO	POWER REQUIREMENT	PACKAGE	TYPE	OPERATING TEMP (°C)	PRICE (1-24)	SEE PAGE
0 to −2mA	20 ppm/°C	+5V, −15V	16 pin DIP	Cerdip	0 to +70	$ 3.50	134C
					−55 to +125	$ 9.50	
0 to −2mA	10 ppm/°C	±15VDC	16 pin DIP	Plastic	0 to +70	$ 4.50	146C
				Ceramic	−55 to +125	$ 10.50	
±5V, 0 to 10V	80 ppm/°C	±15VDC	22 pin DIP	Plastic	0 to +70	$ 13.00	142C
				Cerdip	−55 to +125	$ 26.50	
0 to −4mA	20 ppm/°C	±15VDC	16 pin DIP	Ceramic		$ 9.95	138C
					0 to +70	$ 16.95	
					−55 to +125	$ 32.50	
0 to −5mA, ±2.5mA	10 ppm/°C	+5 to +15V, −15V	24 pin DIP	Ceramic	0 to +70	$ 24.50	150C
					−55 to +125	$152.00	
0 to +5V 0 to +10V ±2.5V, ±5V ±10V	20 ppm/°C	±15VDC	24 pin Ceramic DIP	Epoxy Seal	0 to +70	$ 42.00	192C
				Hermetic Seal	0 to +70	$ 59.00	
					−25 to +85	$ 79.00	
					−55 to +125	$125.00 *	
0 to +2.5V 0 to +5V 0 to +10V	20 ppm/°C	±15VDC	24 pin Ceramic DIP	Epoxy Seal	0 to +70	$ 42.00	192C
				Hermetic Seal	0 to +70	$ 59.00	
					−25 to +85	$ 79.00	
					−55 to +125	$125.00 *	

*Available with MIL-STD-833 class B screening.

THESE PRODUCTS ARE COVERED BY GSA CONTRACT

Quick Selection: General Purpose D/A Converters

	MODEL	DESCRIPTION	RESOLUTION	LINEARITY	OUTPUT	SETTLING TIME	INPUT CODING[1]
MODULAR	**DAC-98BI[2]**	Low Cost	8 Bits	½ LSB	Current	500nsec	Bin
	DAC-98DI[2]		2 Digits				BCD
	DAC-98BIR	Low Cost with Int. Ref.	8 Bits				Bin
	DAC-98DIR		2 Digits				BCD
	DAC-198B	Voltage Output	8 Bits	½ LSB	Voltage	20 μsec	Bin, 2C
	DAC-198D		2 Digits				BCD
	DAC-198BI	Current Output	8 Bits		Current	300 nsec	Bin
	DAC-198DI		2 Digits				BCD
	DAC-298B	5 μsec Voltage Output	8 Bits	½ LSB	Voltage	5 μsec	Bin, 2C
	DAC-298D		2 Digits				BCD
	DAC-4910B	Voltage or Current Output	10 Bits	½ LSB	Voltage	5 μsec	Bin, 2C
	DAC-4910BI		10 Bits		Current	300 nsec	Bin
	DAC-4912D		3 Digits		Voltage	5 μsec	BCD
	DAC-4912DI		3 Digits		Current	300 nsec	
	DAC-6912B	Voltage or Current Output	12 Bits	½ LSB	Voltage	20 μsec	Bin, 2C
	DAC-6912BI				Current	300 nsec	Bin
	DAC-I8B	Fast Settling	8 Bits	½ LSB	Current	150 nsec	Bin
	DAC-I10B		10 Bits				
	DAC-I12B		12 Bits				
	DAC-I8D		2 Digits				BCD
	DAC-I12D		3 Digits				

NOTES: 1. Coding: Bin = Straight Binary or Offset Binary
BCD = Binary Coded Decimal
2C = Two's Complement
2. These models derive their reference from the +15V supply.

OUTPUT RANGES	GAIN TEMPCO	POWER REQUIREMENT	PACKAGE	OPERATING TEMP. (°C)	PRICE (SINGLES)	SEE PAGE
0 to +2.6mA	100 ppm/°C	+15V	2x1x0.375 IN (51x25x10 mm)	0 to +70	$ 30.00	*
0 to +1.6mA					$ 30.00	
0 to +2.6mA					$ 32.00	
0 to +1.6mA					$ 32.00	
0 to +10V, ±5V	50 ppm/°C	±15V	2x2x0.375 IN (51x51x10 mm)	0 to +70	$ 46.00	*
0 to +10V					$ 46.00	
0 to +2.5mA					$ 46.00	
0 to +1.54mA					$ 46.00	
0 to +10V, ±5V	50 ppm/°C	±15V	2x2x0.375 IN (51x51x10mm)	0 to +70	$ 52.50	*
0 to +10V					$ 52.50	
0 to +10V, ±5V	50 ppm/°C	±15V	2x2x0.375 IN (51x51x10mm)	0 to +70	$ 66.00	*
0 to +2.5mA					$ 66.00	
0 to +10V					$ 66.00	
0 to +1.54mA					$ 66.00	
0 to +10V, ±5V	50 ppm/°C	±15V	2x2x0.375 IN (51x51x10mm)	0 to +70	$ 77.50	*
0 to +2.5mA					$ 77.50	
0 to +2mA, ±1mA	15 ppm/°C	±15V	2x1x0.375 IN (51x25x10 mm)	0 to +70	$ 82.50	*
					$ 92.50	
					$105.00	
0 to +1.25mA					$ 82.00	
					$105.00	

*For Data Sheet contact nearest Datel Sales Office.

Datel offers modular products in operating temperature ranges of −25 to +85°C (suffix-EX) and −55 to +85°C (suffix-EXX-HS). For information on these high reliability modules contact nearest Datel sales office.

THESE PRODUCTS ARE COVERED BY GSA CONTRACT

Quick Selection: Multiplying D/A Converters

	MODEL	DESCRIPTION	RESOLUTION	LINEARITY	OUTPUT	SETTLING, TIME, MAX[1]
MONOLITHIC	**DAC-7523C** **DAC-7523R** **DAC-7523M**	4 Quadrant Multiplying D/A	8 Bits	±½ LSB	Current	150 nsec
	DAC-7533C **DAC-7533R** **DAC-7533M**	4 Quadrant Multiplying D/A	10 Bits	±½ LSB	Current	600 nsec
	DAC-7520C **DAC-7520R** **DAC-7520M**	4 Quadrant Multiplying D/A	10 Bits	±½ LSB	Current	500 nsec
	DAC-7521C **DAC-7521R** **DAC-7521M**	4 Quadrant Multiplying D/A	12 Bits	±2 LSB	Current	500 nsec
	DAC-7541C **DAC-7541R** **DAC-7541M**	Low cost 4 Quadrant Multiplying D/A	12 Bits	±½ LSB	Current	1.0 μsec
HYBRID	**DAC-HA10BC** **DAC-HA10BR** **DAC-HA10BM**	Precision 4 Quadrant Multiplying D/A	10 Bits	±½ LSB	Current	1.3 μsec
	DAC-HA12BC **DAC-HA12BR** **DAC-HA12BM**	Precision 4 Quadrant Multiplying D/A	12 Bits	±½ LSB	Current	5.0 μsec
	DAC-HA12DC **DAC-HA12DR** **DAC-HA12DM**	Precision Multiplying D/A	3 Digits	±½ LSB	Current	5.0 μsec
	DAC-HA14BC **DAC-HA14BR** **DAC-HA14BM**	High Resolution 4 Quadrant Multiplying D/A	14 Bits	±1 LSB	Current	7.0 μsec

NOTES: 1. Given for a fullscale output transition
2. Coding: Bin = Straight Binary or Offset Binary
3. For +15V supply option, add suffix −1 to model number.

INPUT CODING[2]	REFERENCE INPUT RANGE	GAIN TEMPCO	POWER REQUIREMENT	PACKAGE	OPERATING TEMP (°C)	PRICE (1-24)	PAGE
Bin	±10V	10ppm/° C	+15VDC	Plastic	0 to +70	$ 3.82	
				Cerdip	−25 to +85	$ 5.72	
					−55 to +125	$ 12.62	
Bin	±10V	10ppm/° C	+15VDC	Plastic	0 to +70	$ 13.57	164C
				Cerdip	−25 to +85	$ 18.07	
					−55 to +125	$ 45.07	
Bin	±10V	10ppm/° C	+15VDC	Plastic	0 to +70	$ 18.22	154C
				Cerdip	−25 to +85	$ 29.83	
					−55 to +125	$ 61.76	
Bin	±10V	10ppm/° C	+15VDC	Plastic	0 to +70	$ 18.87	154C
				Cerdip	−25 to +85	$ 26.32	
					−55 to +125	$ 76.83	
Bin	±10V	10ppm/° C	+15VDC	Plastic	0 to +70	$ 27.12	168C
				Cerdip	−25 to +85	$ 36.08	
					−55 to +125	$103.58	
Bin	±12V	20ppm/° C	+5V or +15V[3]	Ceramic	0 to +70	$ 30.00	174C
					−25 to +85	$ 36.00	
					−55 to +125	* $ 69.00	
Bin	±12V	5ppm/° C	+5V or +15V[3]	Ceramic	0 to +70	$ 49.00	174C
					−25 to +85	$ 69.00	
					−55 to +125	* $ 95.00	
BCD	±12V	5ppm/° C	+5V or +15V[3]	Ceramic	0 to +70	$ 49.00	174C
					−25 to +85	$ 69.00	
					−55 to +125	* $ 95.00	
Bin	±12V	5ppm/° C	+5V or +15V[3]	Ceramic	0 to +70	$ 65.00	174C
					−25 to +85	$ 95.00	
					−55 to +125	* $125.00	

*Available with MIL-STD-883 class B screening.

Datel offers modular products in operating temperature ranges of −25 to +85°C (suffix-EX) and −55 to +85°C (suffix-EXX-HS). For information on these high reliability modules contact nearest Datel sales office.

Quick Selection: High Performance D/A Converters

	MODEL	DESCRIPTION	RESOLUTION	LINEARITY	OUTPUT	SETTLING TIME	INPUT CODING[1]
HYBRID	DAC-HK12BGC	Fast Settling Time with Input Register	12 Bits	½ LSB	Voltage	3 μsec	Bin
	DAC-HK12BMC						
	DAC-HK12BMR						
	DAC-HK12BMM						
	DAC-HK12DGC		3 Digits	¼ LSB			BCD
	DAC-HK12DMC						
	DAC-HK12DMR						
	DAC-HK12DMM						
	DAC-HK12BGC-2		12 Bits	½ LSB			2C
	DAC-HK12BMC-2						
	DAC-HK12BMR-2						
	DAC-HK12BMM-2						
MODULAR	DAC-V8B	Fast Voltage Output	8 Bits	½ LSB	Voltage	2 μsec	Bin
	DAC-V10B		10 Bits				
	DAC-V12B		12 Bits				
	DAC-V8D		2 Digits				BCD
	DAC-V12D		3 Digits				
	DAC-VR8B	Fast Voltage Output With Input Register	8 Bits	½ LSB	Voltage	2 μsec	Bin
	DAC-VR10B		10 Bits				
	DAC-VR12B		12 Bits				
	DAC-VR8D		2 Digits				BCD
	DAC-VR12D		3 Digits				

NOTES: 1. Coding: Bin = Straight Binary or Offset Binary
BCD = Binary Coded Decimal
2C = Two's Complement

OUTPUT RANGES	GAIN TEMPCO	POWER REQUIREMENT	PACKAGE	SEAL	OPERATING TEMP (°C)	PRICE (SINGLES)	SEE PAGE
0 to +5V, 0 to +10V, ±2.5V, ±5V, ±10V	20ppm/°C	+5V ±15V	24 Pin Ceramic DIP	Epoxy	0 to +70	**$ 59.00**	184C
				Hermetic	0 to +70	**$ 75.00**	
					-25 to +85	**$ 89.00**	
					* -55 to +125	**$145.00**	
0 to +2.5V, 0 to +5V, 0 to +10V				Epoxy	0 to +70	**$ 59.00**	
				Hermetic	0 to +70	**$ 75.00**	
					-25 to +85	**$ 89.00**	
					* -55 to +125	**$145.00**	
0 to +5V, 0 to +10V, ±2.5V, ±5V, ±10V				Epoxy	0 to +70	**$ 59.00**	
				Hermetic	0 to +70	**$ 75.00**	
					-25 to +85	**$ 89.00**	
					* -55 to +125	**$145.00**	
0 to +5V, 0 to +10V, ±5V, ±10V	20ppm/°C	±15V	2x2x0.375IN (51x51x10 mm)		0 to +70	**$ 92.50**	* *
						$115.50	
						$138.50	
0 to +5V, 0 to +10V						**$ 92.50**	
						$138.50	
0 to +5V, 0 to +10V, ±5V, ±10V	20ppm/°C	±15V	2x2x0.375IN (51x51x10 mm)		0 to +70	**$105.00**	* *
						$128.00	
						$151.00	
0 to +5V, 0 to +10V						**$105.00**	
						$151.00	

** For Data Sheet contact nearest Datel sales office.

* Available with MIL-STD-883 class B screening.

Datel offers modular products in operating temperature ranges of −25 to +85°C (suffix-EX) and −55 to +85°C (suffix-EXX-HS). For information on these high reliability modules contact nearest Datel sales office.

THESE PRODUCTS ARE COVERED BY GSA CONTRACT

Quick Selection: High Speed D/A Converters

	MODEL	DESCRIPTION	RESOLUTION	LINEARITY	OUTPUT	SETTLING TIME, MAX[1]	INPUT CODING[2]
HYBRID	DAC-HF8BMC	Ultra-Fast 8 bit D/A	8 Bits	±½ LSB	Current	25 nsec	Bin
	DAC-HF8BMR						
	DAC-HF8BMM						
	DAC-HF10BMC	Ultra-Fast 10 bit D/A	10 Bits	±½ LSB	Current	25 nsec	Bin
	DAC-HF10BMR						
	DAC-HF10BMM						
	DAC-HF12BMC	Ultra-Fast 12 bit D/A	12 Bits	±½ LSB	Current	50 nsec	Bin
	DAC-HF12BMR						
	DAC-HF12BMM						
MODULE	DAC-HI8B	Ultra-Fast D/A	8 Bits	±½ LSB	Current	25 nsec	Bin
	DAC-HI10B		10 Bits				
	DAC-HI12B		12 Bits			50 nsec	
	DAC-DG12B1	Fast Deglitched D/A	12 Bits	±½ LSB	Voltage	600 nsec	Bin, 2C
	DAC-DG12B2						

NOTES:

1. For full scale output change to rated accuracy.

2. CODING: Bin = Straight binary or offset binary.
   2C = Two's complement.

OUTPUT RANGES	GAIN TEMPCO	POWER REQUIREMENT	PACKAGE	OPERATING TEMP (° C)	PRICE SINGLES	SEE PAGE
0 to +10mA, ±5mA	20 ppm/° C	±15 VDC	24 pin Ceramic DIP Hermetic Seal	0 to +70	**$ 99.00**	180C
				−25 to +85	**$119.00**	
				55 to +125	***$189.00**	
0 to +10mA, ±5mA	20 ppm/° C	±15 VDC	24 pin Ceramic DIP Hermetic Seal	0 to +70	**$109.00**	180C
				−25 to +85	**$129.00**	
				55 to +125	***$209.00**	
0 to +10mA, ±5mA	20 ppm/° C	±15 VDC	24 pin Ceramic DIP Hermetic Seal	0 to +70	**$129.00**	180C
				−25 to +85	**$149.00**	
				55 to +125	***$219.00**	
±2.5mA, +5mA	15 ppm/° C	±15 VDC	2 x 2 x 0.375IN (51 x 51 x 10mm)	0 to +70	**$115.00**	200C
	20 ppm/° C				**$138.50**	
					$151.00	
−10V, ±5V, ±10V ±5V, ±10V	35 ppm/° C	±15 VDC +5V	4 x 2 x 0.4 IN (102 x 51 x 10mm)	0 to +70	**$290.00**	196C
					$290.00	

*Available with MIL-STD-883 Class B screening.

Datel offers modular products in operating temperature ranges of −25 to +85°C (suffix-EX) and −55 to +85°C (suffix-EXX-HS). For information on these high reliability modules contact nearest Datel sales office.

Quick Selection: High Resolution D/A Converters

	MODEL	DESCRIPTION	RESOLUTION	LINEARITY	OUTPUT	SETTLING TIME
HYBRID	DAC-HA14BC	Multiplying CMOS	14 Bits	1 LSB	Current	7 μsec
	DAC-HA14BR					
	DAC-HA14BM					
	DAC-HP16BGC	Internal Reference and Output OP-Amp.	16 Bits	4 LSB	Voltage	15 μsec
	DAC-HP16BMC					
	DAC-HP16BMR					
	DAC-HP16BMM					
	DAC-HP16DGC		4 Digits	½ LSB		
	DAC-HP16DMC					
	DAC-HP16DMR					
	DAC-HP16DMM					
MODULES	DAC-169-16B	Low Cost	16 Bits	4 LSB	Voltage[3]	30 μsec
	DAC-169-16D		4 Digits	½ LSB		
	DAC-HR13B	Ultra-Low Drift	13 Bits	½ LSB	Current	1 μsec
	DAC-HR14B		14 Bits			
	DAC-HR15B		15 Bits			
	DAC-HR16B		16 Bits	1 LSB		

NOTES:

1. Coding: Bin = Straight binary or offset binary
   BCD = Binary Coded Decimal
   CBin = Complementary binary
   CBCD = Complementary BCD
2. For + 15V supply option add suffix " – 1" to model number
3. Can also be connected for current output. Current output is 0 to + 2mA or ± 1mA for binary version and 0 to – 1.25mA for BCD version.

INPUT CODING[1]	OUTPUT RANGES	GAIN TEMPCO	POWER REQUIREMENT	PACKAGE	OPERATING TEMP(°C)	PRICE (SINGLES)	SEE PAGE
Bin	±1mA	5 ppm/°C	+5V or +15V[2]	20 Pin Ceramic DIP	0 to +70	$ 65.00	174C
					−25 to +85	$ 95.00	
					−55 to +125	$125.00	
CBin	0 to +10V ±5V	20 ppm/°C	±15V	24 Pin Ceramic DIP	0 to +70	$ 65.00	188C
		15 ppm/°C			0 to +70	$ 82.00	
					−25 to +85	$ 92.00	
					−55 to +125	$145.00	
CBCD	0 to +10V	20 ppm/°C			0 to +70	$ 65.00	
		15 ppm/°C			0 to +70	$ 89.00	
					−25 to +85	$ 92.00	
					−55 to +125	$145.00	
Bin	0 to +10V 0 to −10V, ±5V	10 ppm/°C	±15V	2 × 2 × 0.375 in (51×51×10mm)	0 to +70	$126.00	*
BCD	0 to +10V 0 to −10V					$126.00	
CBin	0 to −2mA ±1mA	1.5ppm/°C	±15V	4 × 2 × 0.375 in (102×51×10mm)	0 to +70	$290.00	204C
						$306.00	
						$321.00	
						$347.50	

*For data sheet contact nearest Datel Sales Office.

These products are covered by GSA contract.

Datel offers modular products in operating temperature ranges of −25 to +85°C (suffix-EX) and −55 to +85°C (suffix-EXX-HS). For information on these high reliability modules contact nearest Datel sales office.

Low Cost, 8 Bit Monolithic Digital-to-Analog Converters Model DAC-IC8B

FEATURES

- **Low Cost**
- **8 Bit Resolution**
- **Fast Settling—300 nsec.**
- **1 or 2 Quadrant Multiplication**
- **±½LSB Linearity**
- **DTL/TTL Compatible Inputs**

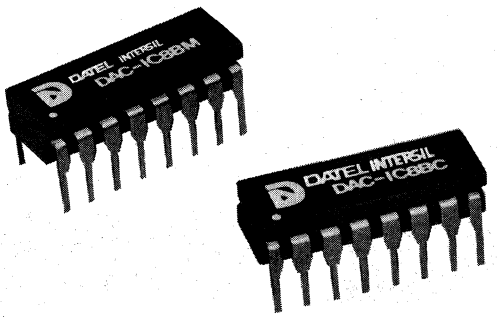
GENERAL DESCRIPTION

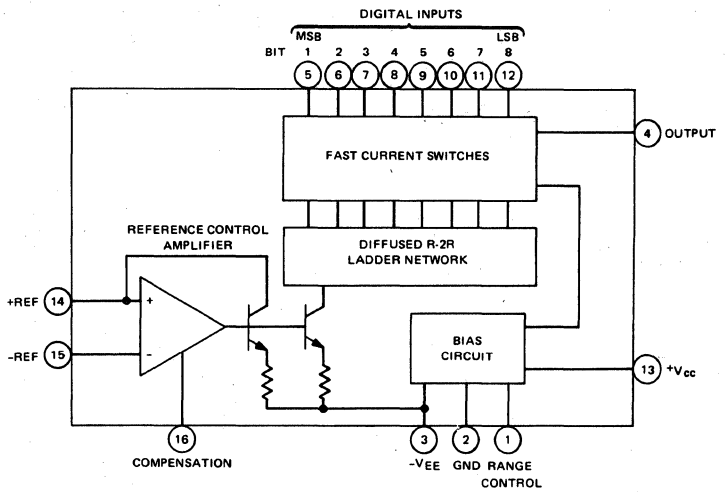
The DAC-IC8BC and DAC-IC8BM are 8 bit monolithic DAC's with fast setting current outputs. The units are housed in a 16 pin ceramic DIP and require only an external reference and output amplifier for fast voltage output operation. A full scale output change settles in only 300 nanoseconds for current output operation and 600 nanoseconds for voltage output operation using a fast monolithic output amplifier (Datel-Intersil's AM-452). Digital input coding is straight binary for unipolar operation and offset binary for bipolar operation and is compatible with standard DTL/TTL logic.

The DAC-IC8B converters consist of 8 fast-switching current sources, a diffused R-2R resistor ladder network, a bias circuit, and a reference control amplifier. The diffused resistor ladder gives excellent temperature tracking resulting in a gain temperature coefficient of −20ppm/°C. The monolithic fabrication results in excellent linearity and tempco, fast output settling, and low cost. Linearity is ±½LSB.

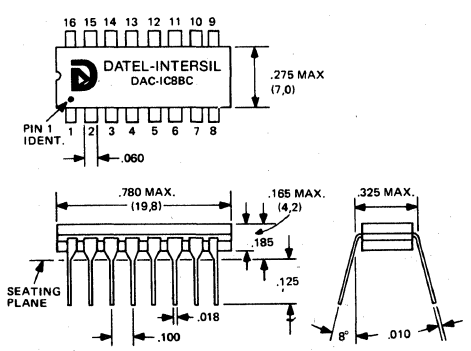
An external reference current of 2mA nominal programs the scale factor for the DAC; this is done by means of an external voltage reference source (such as Zener diode) and a resistor. This reference current can also be varied, resulting in one or two quadrant multiplying operation. The output voltage can be unipolar or bipolar depending on whether an external offsetting current (derived from the reference) is used. Output voltage compliance of the DAC is −0.6V to +0.5V; this can be made as large as −5V to +0.5V by external pin connection for cases where direct voltage output from a load resistor is desired.

Power supply requirement is +5VDC and −5V to −15VDC. Model DAC-IC8BC has an operating temperature range of 0°C to 70°C while DAC-IC8BM operates over −55°C to +125°C. The two models are pin compatible with industry standard devices 1408L-8 and 1508L-8 respectively.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	RANGE CONTROL
2	GROUND
3	V_{EE}
4	OUTPUT
5	BIT 1 IN (MSB)
6	BIT 2 IN
7	BIT 3 IN
8	BIT 4 IN
9	BIT 5 IN
10	BIT 6 IN
11	BIT 7 IN
12	BIT 8 IN (LSB)
13	V_{CC}
14	+REFERENCE
15	−REFERENCE
16	COMPENSATION

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, DAC-IC8BC & DAC-IC8BM (Typical at 25°C, V_{CC} = +5V, V_{EE} = −15V, and I_{REF} = 2mA unless otherwise specified)

ABSOLUTE MAXIMUM RATINGS	
Power Supply Voltage, V_{CC}	+5.5V
V_{EE}	−16.5V
Digital Input Voltage	+5.5V
Reference Current	5.0mA
Reference Amp. Inputs	$+V_{CC}$, $-V_{EE}$
Power Dissipation	1.0 watt
INPUTS	
Resolution	8 bits
Coding, unipolar output	Straight Binary
Coding, bipolar output	Offset Binary
Input Logic Level, bit ON ("1")	+2.0V to +5.5V @ 40μA
Input Logic Level, bit OFF ("0")	0V to +0.8V @ −0.8mA
Logic Loading	1 TTL load
Nominal Reference Current (+ Ref.)	2.0mA
Reference Current Range (+ Ref.)	0 to 4.2mA
Reference Bias Current (− Ref.)	−3μA max.
OUTPUTS	
Output Current, I_{REF} = 2.0mA	2.0mA ±0.1mA
Output Current Range, V_{EE} = −5V	0 to 2.1mA
Output Current Range, V_{EE} = −6 to −15V	0 to 4.2mA
Output Current, all bits OFF	4μA maximum
Output Voltage Compliance, pin 1 gnded	−0.6 to +0.5V
Output Voltage Comp., pin 1 open, $V_{EE} < -10V$	5.0V to +0.5V
PERFORMANCE	
Relative Accuracy[1]	±½LSB (±0.19%) maximum
Nonlinearity	±½LSB (±0.19%) maximum
Differential Nonlinearity	±½LSB (±0.19%)
Temp. Coefficient of Gain	−20ppm/°C
Power Supply Rejection (V_{EE})	2.7μA/V max.
Settling Time, 2mA to ½LSB	300 nsec.
Update Rate	3.3MHz
Reference Current Slew Rate	4.0mA/μsec
POWER REQUIREMENT	
V_{CC} Voltage	+5VDC ±0.5V
V_{CC} Current	22mA maximum
V_{EE} Voltage	−4.5V to −16.5VDC
V_{EE} Current	13mA maximum
PHYSICAL-ENVIRONMENTAL	
Operating Temp. Range, DAC-IC8BC	0°C to 70°C
Operating Temp. Range, DAC-IC8BM	−55°C to +125°C
Storage Temp. Range, either model	−65°C to +150°C
Package	16 pin ceramic DIP

[1] With zero and full scale adjustments made.

ORDERING INFORMATION

DAC-IC8B —

OPER. TEMP. RANGE
C = 0°C TO 70°C
M = −55°C TO +125°C

PRICES
DAC-IC8BC
DAC-IC8BM

Trimming Potentiometers: TP500, TP1K, and TP20K are available from Datel-Intersil

The DAC-IC8BC and DAC-IC8BM converters are covered under GSA contract.

TECHNICAL NOTES

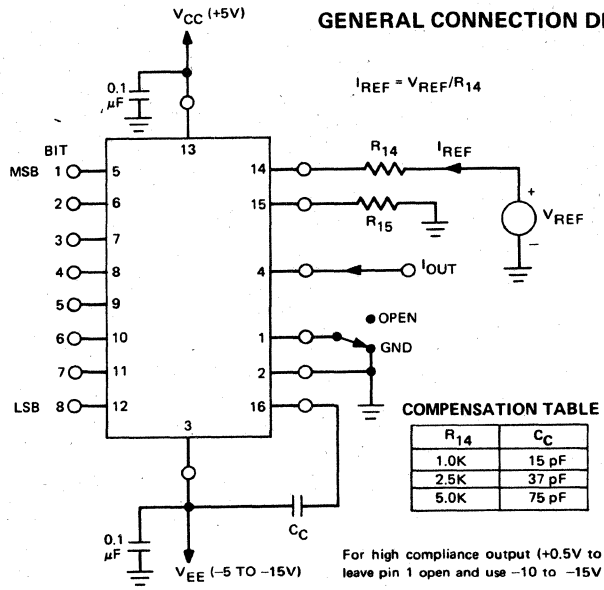
1. The *General Connection Diagram* shows the basic connections for the DAC-IC8B converter. The scale factor is set by a reference current injected into pin 14. Pins 14 and 15 are the input terminals to the reference control amplifier. When connected as shown, pin 15 is grounded through R_{15} and pin 14 is at virtual ground. Therefore, the reference current is determined by the external voltage reference and R_{14}: $I_{REF} = V_{REF}/R_{14}$. R_{14} should be a stable metal film resistor. R_{15} is used only to compensate for the input bias current into pin 15 (1 μA typical) and can be shorted out with negligible effect. R_{15}, if used, should be equal to R_{14} and may be a carbon composition type. An I_{REF} of 2.0mA is recommended for most applications.
2. There is a second method of connecting the reference shown in *Two Ways to Connect Reference.* A negative reference can be applied to pin 15. In this case only the bias current must be supplied from the reference since pin 15 is a high impedance input. Pin 14 is at the negative voltage and I_{REF} still flows into pin 14. Again, R_{15} is used only to compensate for bias current and may be omitted. There is an important requirement for this connection: *the negative reference voltage must always be 3 volts above V_{EE}.*
3. The reference amplifier must be externally compensated, and this is done by capacitor C_C, connected from pin 16 to pin 3 (V_{EE}). C_C may also be connected from pin 16 to ground, but connection to pin 3 improves the negative supply rejection. The value of C_C depends on R_{14}, and typical values are given in the compensation table. Compensation is particularly important when the DAC-IC8B is used as a multiplying D/A converter. Proper compensation assures that output peaking does not occur when the reference voltage steps to a new value. If pin 14 is driven from a high impedance current source such as a transistor collector, then much larger values of C_C must be used and the bandwidth of the reference amplifier is significantly reduced.
4. The *Alternative Compensation Diagram* shows another way of achieving the desired compensation. Here a 1.0K resistor is always used at pin 14, but it is in series with another R to the reference voltage. The junction of the two resistors is bypassed to ground by a 0.1μF capacitor. For high frequencies pin 14 always "sees" a 1K resistance, thus allowing a 15pF capacitor for C_C. R_{15}, if used, should be the sum of 1.0K and R. This compensation scheme is useful with voltage references such as 6.2 or 6.4 volt Zener diodes.
5. It is recommended that pin 13 (V_{CC}) and pin 3 (V_{EE}) always be bypassed to ground with at least 0.1μF capacitors located close to the pins.
6. As shown in the *General Connection Diagram,* pin 1 may be either connected to ground or left open. This connection determines the voltage compliance at pin 4 (I_{OUT}). For pin 1 grounded, the output compliance is −0.6 to +0.5 volt. This is satisfactory when pin 4 is used to drive a current to voltage converter and pin 4 is held at virtual ground. It is also satisfactory for low values of R_L connected to pin 4 to directly convert the output current to a voltage. The voltage compliance may be extended to −5.0 volts by leaving pin 1 open and using a V_{EE} more negative than −10 volts. In this way a 2.5K load resistor may be used at pin 14 to give an output voltage range of 0 to −5 volts (with reference current of 2mA). As shown in the table of *Settling Time vs R_L*, the output settling time is constant (300 nsec.) for R_L values from 0 to 500 ohms; thereafter it increases to 1.2μsec for R_L = 2.5K.
7. The accuracy of the DAC-IC8B is specified for a reference current of 2.0mA; the accuracy, however, is essentially constant for reference currents from 1.5mA to 2.5mA. Typically, this device is monotonic for all values of reference current above 0.5mA. Reference currents up to 4.2mA may be used. *When using a 4mA reference current, V_{EE} must be more negative than −6 volts.*

TECHNICAL NOTES (Cont'd)

8. For fastest voltage output settling times in either unipolar or bipolar modes, two circuits using Datel Systems AM-452 monolithic operational amplifiers are recommended. These circuits, with the compensation shown, result in output settling times of typically 600 nsec. for a 10 volt change to 1 LSB. This is the worst case settling time which occurs when all bits are turned on. For current output and R_L less than 500 ohms, this time is 300 nsec.; when all bits are turned off the time is shorter, typically 100 nsec. The two circuits shown also illustrate a simple method of deriving both reference current and offset current from a precision 6.4 volt Zener reference diode.
9. Both one and two quadrant multiplication are also possible with the DAC-IC8B as shown in the two diagrams. V_{IN} is shown operating into pin 14; this results in an input impedance of 2.5K. Alternatively, V_{IN} can be applied to pin 15 for a high impedance input as explained previously. The range of V_{IN} is then 0 to −10V. For two quadrant multiplication V_{IN} is unipolar and the digital input is bipolar with offset binary coding. V_{OUT} then varies over the bipolar range of ±5 volts. In multiplication applications, it is recommended that full scale I_{REF} be set to 4.0mA; the output is then monotonic as the reference current varies over 0.5mA to 4.0mA.

CONNECTION DIAGRAMS

GENERAL CONNECTION DIAGRAM

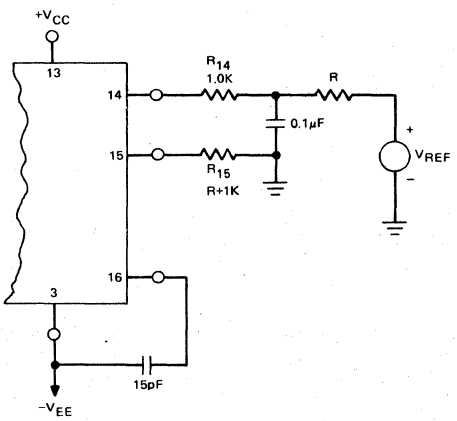


COMPENSATION TABLE

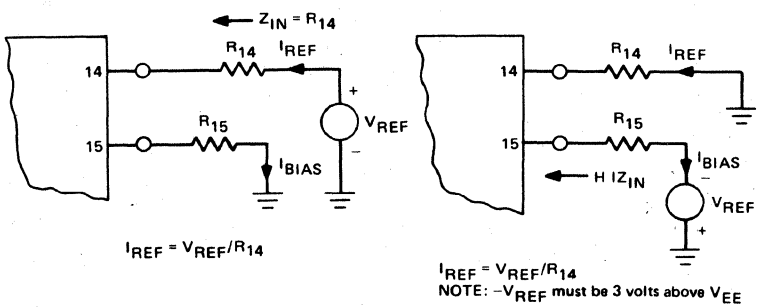
R_{14}	C_C
1.0K	15 pF
2.5K	37 pF
5.0K	75 pF

For high compliance output (+0.5V to −5.0V) leave pin 1 open and use −10 to −15V for V_{EE}.

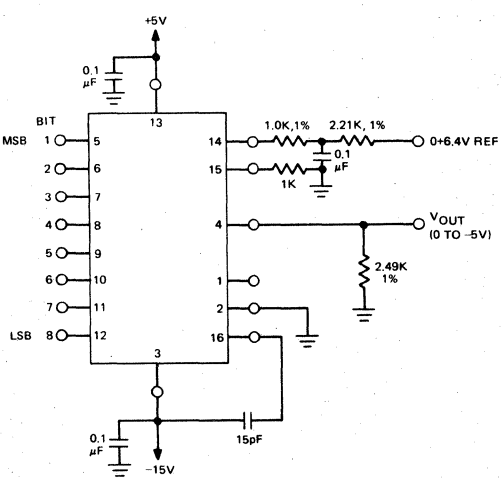
ALTERNATIVE COMPENSATION



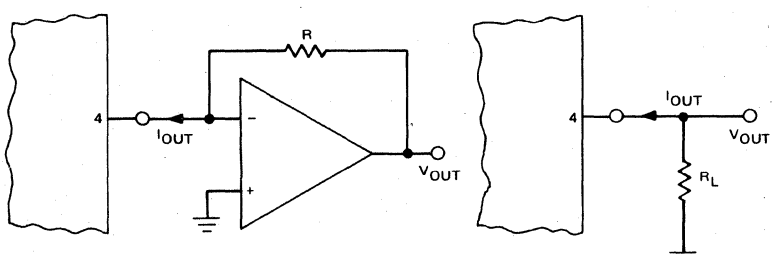
TWO WAYS TO CONNECT REFERENCE



HIGH COMPLIANCE OUTPUT



OUTPUT CONNECTIONS

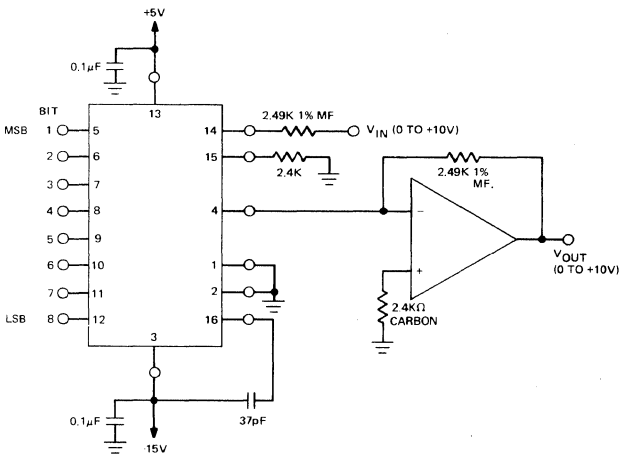


SETTLING TIME VS. R_L

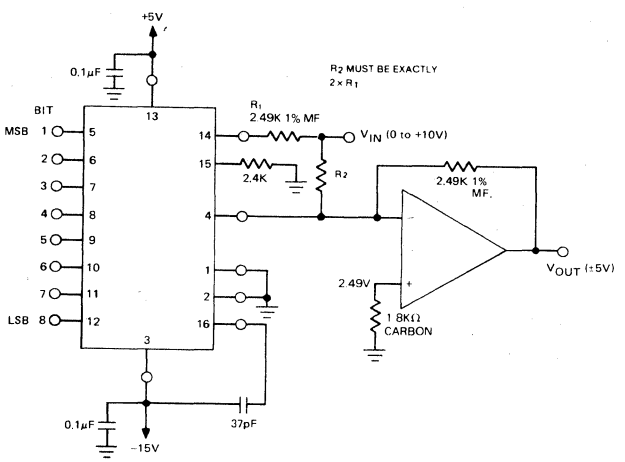
R_L	S.T.
0	300 nsec.
500	300 nsec.
1 K	400 nsec.
2.5 K	1.2 μsec.

APPLICATION DIAGRAMS

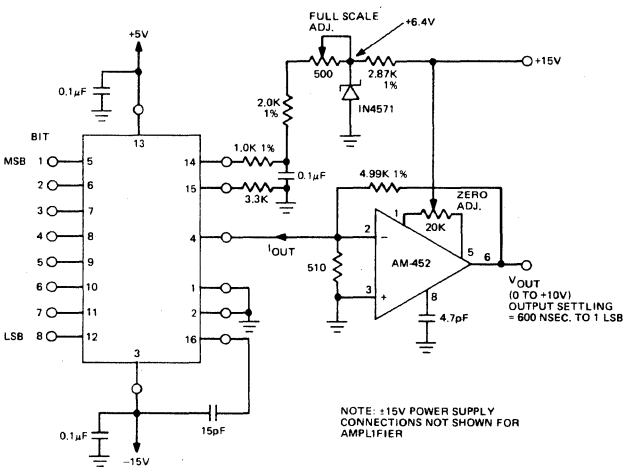
ONE QUADRANT MULTIPLICATION



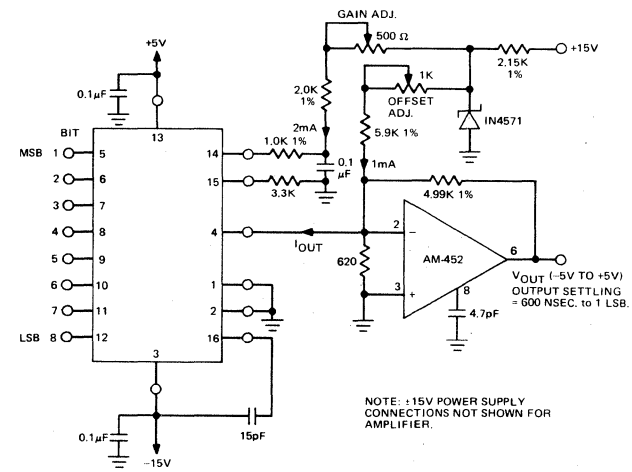
TWO QUADRANT MULTIPLICATION



FAST, UNIPOLAR VOLTAGE OUTPUT



FAST, BIPOLAR VOLTAGE OUTPUT



CALIBRATION AND CODING TABLES

1. Select the desired output range by means of the feedback resistor of the external operational amplifier and the externally programmed reference current.
2. *Zero and Offset Adjustments*
   For unipolar operation, set all digital inputs to "0" (0V to +0.8V) and adjust the output amplifier ZERO ADJUSTMENT for zero output voltage. For bipolar operation, set all digital inputs to "0" (0 to +0.8V) and adjust the OFFSET ADJUSTMENT for the negative full scale voltage shown in the Coding Table.
3. *Gain Adjustment*
   For either unipolar or bipolar operation, set all digital inputs to "1" (+2.0 to +5.5V) and adjust the GAIN ADJUSTMENT for the positive full scale voltage shown in the Coding Table.

UNIPOLAR OPERATION–STRAIGHT BINARY CODING

INPUT CODE	UNIPOLAR OUTPUT RANGES			
MSB LSB	0 TO +5V	0 TO +10V	0 TO −2MA	0 TO −4MA
1111 1111	+4.980	+9.961V	−1.992MA	−3.984MA
1110 0000	+4.375	+8.750	−1.750	−3.500
1100 0000	+3.750	+7.500	−1.500	−3.000
1000 0000	+2.500	+5.000	−1.000	−2.000
0100 0000	+1.250	+2.500	−0.500	−1.000
0000 0001	+0.020	+0.039	−0.008	−0.016
0000 0000	0.000	0.000	0.000	0.000

BIPOLAR OPERATION–OFFSET BINARY CODING

INPUT CODE	BIPOLAR OUTPUT RANGES			
MSB LSB	±5V	±10V	±1MA	±2MA
1111 1111	+4.961V	+9.922V	−0.992MA	−1.984MA
1110 0000	+3.750	+7.500	−0.750	−1.500
1100 0000	+2.500	+5.000	−0.500	−1.000
1000 0000	0.000	0.000	0.000	0.000
0100 0000	−2.500	−5.000	+0.500	+1.000
0000 0001	−4.961	−9.922	+0.992	+1.984
0000 0000	−5.000	−10.000	+1.000	+2.000

DATEL INTERSIL
11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617)339-9341 / TWX 710-346-1953 / TLX 951340
Santa Ana, (714)835-2751, (L.A.) (213)933-7256 • Sunnyvale, CA (408)733-2424 • Gaithersburg, MD (301)840-9490
• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Low Cost, 10 Bit Monolithic Digital-to-Analog Converter DAC-IC10B Series

FEATURES

- **10 Bit Resolution**
- **Straight Binary Coding**
- **Current Output**
- **250 nsec. Settling Time**
- **TTL/CMOS Compatible**
- **Low Cost**

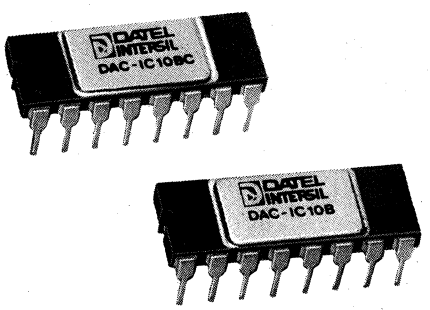
GENERAL DESCRIPTION

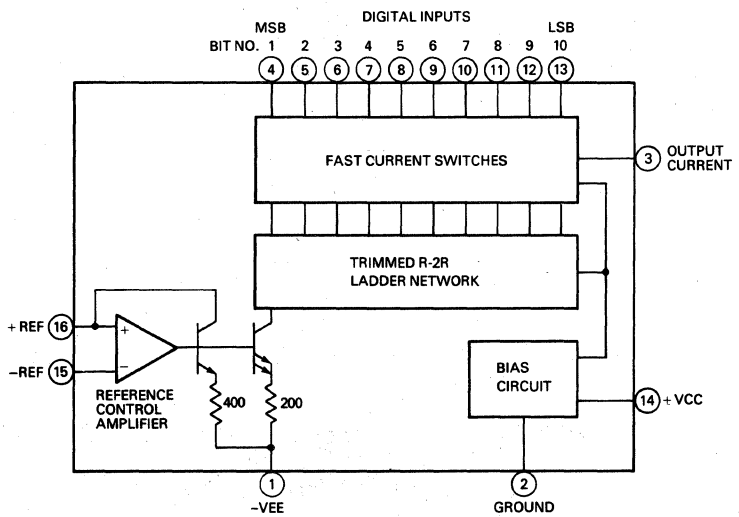
The DAC-IC10B is a low cost, 10 bit monolithic DAC with fast output current settling time. It is packaged in a 16 pin ceramic DIP and requires only an external reference and operational amplifier for voltage output operation. A full scale change in output current settles in 250 nanoseconds, and with a fast I.C. op amp (such as Datel-Intersil's AM-452) a 10V output change can settle within 1 microsecond. Digital input coding is straight binary for unipolar operation, and offset binary for bipolar operation; the logic inputs are compatible with TTL or CMOS.

This converter is manufactured with monolithic bipolar technology. The circuit incorporates 10 fast switching current sources which drive a diffused resistor R-2R network. The ladder network is laser trimmed by cutting aluminum links. The circuit also contains a reference control amplifier and a bias circuit. An external reference current of 2 mA is required at the + Reference input terminal; this is accomplished by an external voltage reference and a metal film resistor.

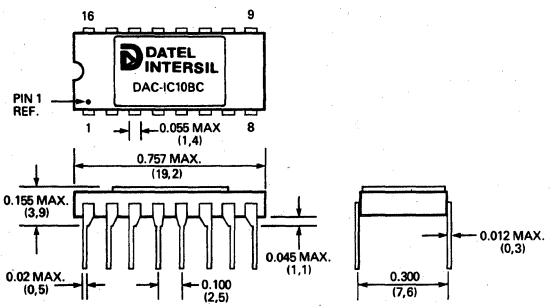
Other characteristics of the DAC-IC10B include linearity to ±½ LSB and guaranteed monotonic performance. The gain temperature coefficient of this unit is typically −20ppm/°C. Output voltage compliance is −2.5V to +0.2V, permitting direct driving of a 625 ohm resistor for a voltage output. The reference input current can be varied from 0.5 mA to 2.5mA to give monotonic operation as a one or two quadrant multiplier.

Power supply requirement is +5VDC and −15VDC. The DAC-IC10B is available in three models covering two temperature ranges, 0°C to +70°C and −55°C to +125°C.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	−VEE
2	GROUND
3	OUTPUT CURRENT
4	BIT 1 IN (MSB)
5	BIT 2 IN
6	BIT 3 IN
7	BIT 4 IN
8	BIT 5 IN
9	BIT 6 IN
10	BIT 7 IN
11	BIT 8 IN
12	BIT 9 IN
13	BIT 10 IN
14	+VCC
15	−REFERENCE
16	+REFERENCE

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, DAC-IC10B
(Typical at 25°C, V_{CC} = +5V, V_{EE} = −15V, I_{REF} = 2.0 mA)

MAXIMUM RATINGS

V_{CC}	+7.0 Volts
V_{EE}	+18.0 Volts
Digital Input Voltage	+15 Volts
Output Voltage, Pin 3	+0.5, −5.0 Volts
Ref. Current	2.5 mA
Diff. Ref. Voltage	0.7V

INPUTS

Resolution	10 Bits
Coding, Unipolar Output	Straight Binary
Coding, Bipolar Output	Offset Binary
Input Level, Logic "1"	+2.0 to +15V @ +40μA
Input Level, Logic "0"	0 to +0.8V @ −0.4 mA
Nom. Ref. Current, Pin 16	2.0 mA
Reference Current Range	0.5 mA to 2.5 mA
Ref. Bias Current, Pin 15	−5 μA max.

OUTPUTS

Output Current	4.0 mA ±0.2 mA
Output Current Range	0 to 5.0 mA
Output Current, All Bits "0"	2.0 μA max.[1]
Output Voltage Compliance	−2.5 to +0.2V
Output Capacitance	25 pF

PERFORMANCE

Linearity Error, B, BM	±½ LSB, max.
BC	±1 LSB, max.
Diff. Linearity Error	±½ LSB
Monotonicity, B, BM	Full Temp. Range[2]
BC	At 25°C
Gain Tempco	−20 ppm/°C, 60 ppm/°C max.[3]
Ref. Current, Slew Rate	20 mA/μsec.
Ref. Current Settling	2.0 μsec.[4]
Output Current Settling	250 nsec.[5]
Update Rate	4 MHz
Power Supply Sensitivity	.02%/% max.

POWER REQUIREMENT

V_{CC} Voltage	+5 VDC ±0.25V
V_{CC} Current	18 mA max.
V_{EE} Voltage	−15 VDC ±0.75V
V_{EE} Current	−20 mA max.

PHYSICAL-ENVIRONMENTAL

Operating Temp. Range	
DAC-IC10B, BC	0°C to +70°C
DAC-IC10BM	−55°C to +125°C
Storage Temp. Range	−65°C to +125°C
Package	16 Pin Ceramic DIP

NOTES:
1. 4.0 μA max. for DAC-IC10BC only.
2. All converters in this series typically retain rated monotonicity for values of input reference current from 0.5 mA to 2.5 mA.
3. 70 ppm/°C max. for DAC-IC10BM only.
4. Zero to 4 mA output change to rated accuracy.
5. Full scale change to ½ LSB.

ORDERING INFORMATION

MODEL	OPER. TEMP RANGE
DAC-IC10BC	0°C to +70°C
DAC-IC10B	0°C to +70°C
DAC-IC10BM	−55°C to +125°C

THESE CONVERTERS ARE COVERED BY GSA CONTRACT.

TECHNICAL NOTES

1. The *General Connection Diagram* shows the basic connections for the converter. The scale factor is set by a reference current injected into pin 16. Pins 15 and 16 are the input terminals to the reference control amplifier. When connected as shown, pin 15 is grounded through R_{15} and pin 16 is at virtual ground. Therefore, the reference current is determined by the external voltage reference and R_{16}: $I_{REF} = V_{REF}/R_{16}$. R_{16} should be a stable metal film resistor. R_{15} is used only to compensate for the input bias current into pin 15 (1 μA typical). R_{15}, if used, should be equal to R_{16} and may be a carbon composition type. An I_{REF} of 2.0 mA is recommended for most applications.

2. There is a second method of connecting the reference shown in *Two Ways to Connect Reference.* A negative reference can be applied to pin 15. In this case only the bias current must be supplied from the reference since pin 15 is a high impedance input. Pin 16 is at the negative voltage and I_{REF} still flows into pin 16. Again, R_{15} is used only to compensate for bias current. There is an important requirement for this connection: **the negative reference voltage must always be 3 volts above V_{EE}.**

3. I_{OUT} is inversely proportional to the reference input current (I_{REF}) times the digital word. Scaling of the applied reference can be represented as follows:

$$I_{OUT} = -2\left(\frac{V_{REF}}{R_{REF}}\right)\left(\frac{A_n}{2^n}\right)$$

where n = 10 (10 bit DAC)
A_n = digital code

Note: 1) The largest digital code for a 10 bit DAC is 1023.
2) The reference current is scaled by a factor of 2 within the DAC.

Example:

$$I_{OUT}(FS) = -2\left(\frac{2.5V}{1.25K}\right)\left(\frac{1023}{1024}\right)$$
$$= -3.996 \text{ mA (nominal)}$$

$$I_{OUT}(ZERO) = -2\left(\frac{2.5V}{1.25K}\right)\left(\frac{0}{1024}\right)$$
$$= 0 \text{ mA (nominal)}$$

4. The reference amplifier is internally compensated. The minimum reference current supplied from a current source is 0.5 mA for stability.

5. The voltage on pin 3 is restricted to a range of −2.5V to +0.2V. This compliance voltage is guaranteed at 25°C and nearly constant over temperature.

6. Full scale output current of 3.996 mA is guaranteed for input reference currents to pin 16 between 1.9 and 2.1 mA.

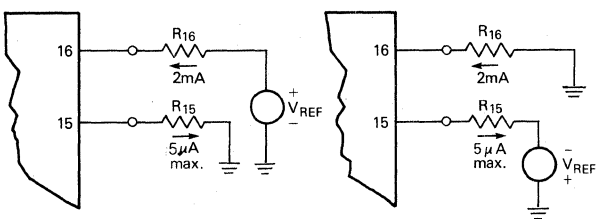
7. It is recommended that pin 14 (V_{CC}) and pin 1 (V_{EE}) always be bypassed to ground with at least 0.1 μF capacitors located close to the pins.

8. The accuracy of the converter is specified for a reference current of 2.0 mA; the accuracy, however, is essentially constant for reference currents from 1.5 mA to 2.5 mA. Typically, this device is monotonic for all values of reference current above 0.5 mA.

TECHNICAL NOTES (cont'd.)

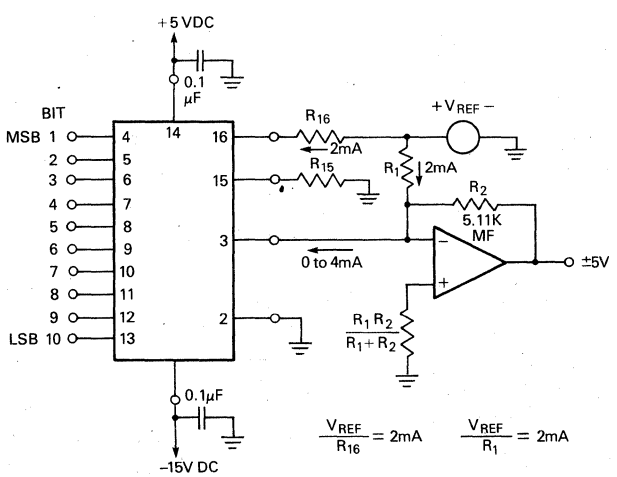
9. For fastest voltage output settling times in either unipolar or bipolar modes, two circuits using Datel-Intersil AM-452 monolithic operational amplifiers are recommended. These circuits, with the compensation shown, result in output settling times of typically 550 nsec. for a 10 volt change to 1 LSB. This is the worst case settling time which occurs when all bits are turned on. For current output and R_L less than 500 ohms, this time is 250 nsec.; when all bits are turned off the time is shorter, typically 100 nsec. The two circuits shown also illustrate a simple method of deriving both reference current and offset current from a precision 6.4 volt Zener reference diode.
10. Both one and two quadrant multiplication are also possible with the converter as shown in the two diagrams. V_{IN} is shown operating into pin 16; this results in an input impedance of 2.5K. Alternatively, V_{IN} can be applied to pin 15 for a high impedance input as explained previously. The range of V_{IN} is then 0 to −10V. For two quadrant multiplication V_{IN} is unipolar and the digital input is bipolar with offset binary coding. V_{OUT} then varies over the bipolar range of ±5 volts. In multiplication applications, it is recommended that full scale I_{REF} be set to 2.0 mA; the output is then monotonic as the reference current varies over 0.5 mA to 2.0 mA.

TWO WAYS TO CONNECT REFERENCE



$R_{15} = R_{16}$ $\quad \frac{V_{REF}}{R_{16}} = 2mA$

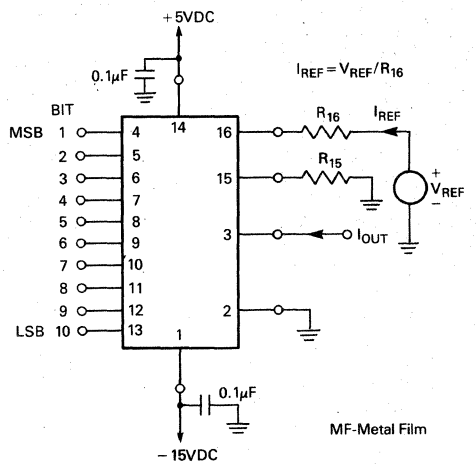
CONNECTION FOR BIPOLAR VOLTAGE OUT



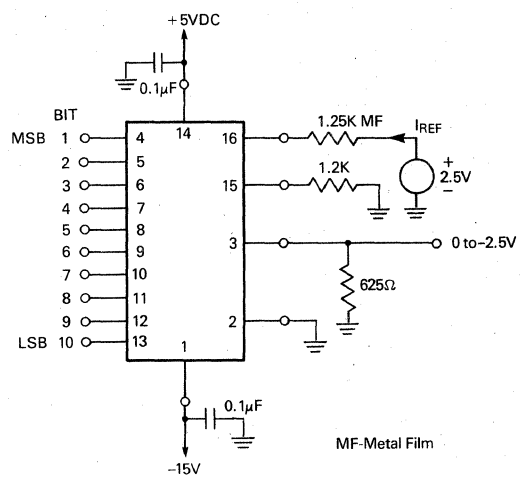
$\frac{V_{REF}}{R_{16}} = 2mA$ $\quad \frac{V_{REF}}{R_1} = 2mA$

CONNECTION DIAGRAMS

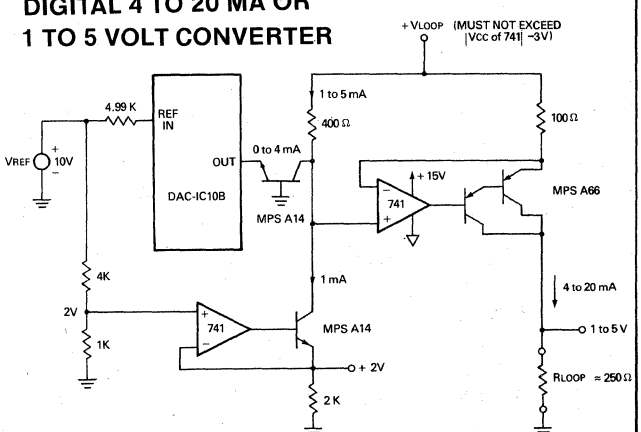
GENERAL CONNECTION DIAGRAM



CONNECTION FOR DIRECT VOLTAGE OUTPUT

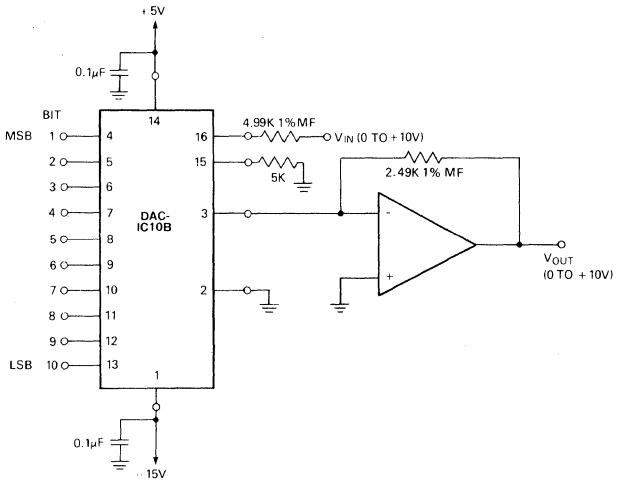


DIGITAL 4 TO 20 MA OR 1 TO 5 VOLT CONVERTER

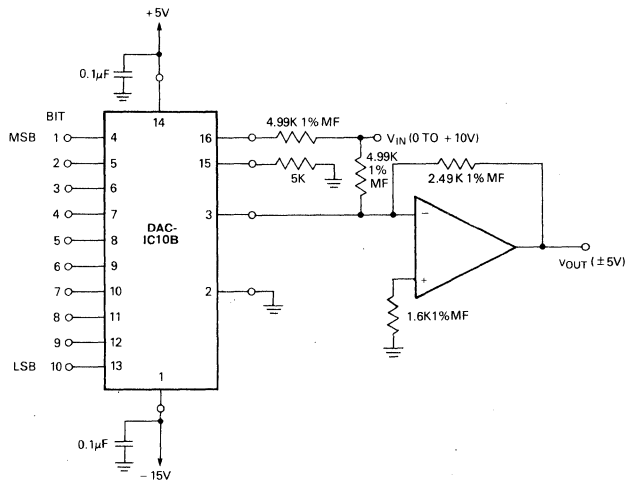


APPLICATION DIAGRAMS

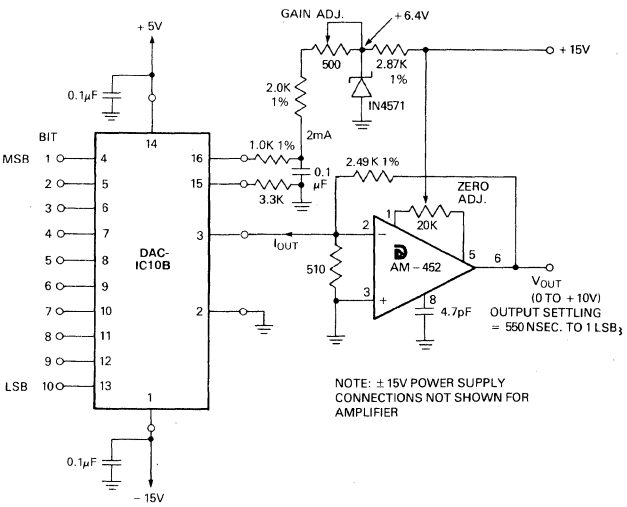
ONE QUADRANT MULTIPLICATION



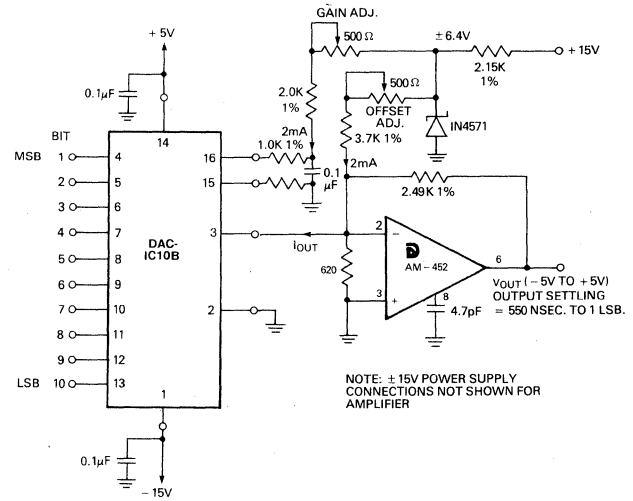
TWO QUADRANT MULTIPLICATION



FAST, UNIPOLAR VOLTAGE OUTPUT



FAST, BIPOLAR VOLTAGE OUTPUT



CALIBRATION AND CODING TABLE

1. Select the desired output range by means of the feedback resistor of the external operational amplifier and the externally programmed reference current.
2. *Zero and Offset Adjustments*/ For unipolar operation, set all digital inputs to "0" (0V to +0.8V) and adjust the output amplifier ZERO ADJUSTMENT for zero output voltage. For bipolar operation, set all digital inputs to "0" (0 to +0.8V) and adjust the OFFSET ADJUSTMENT for the negative full scale voltage shown in the Coding Table.
3. *Gain Adjustment*/ For either unipolar or bipolar operation, set all digital inputs to "1" (+2.0 to +5.5V) and adjust the GAIN ADJUSTMENT for the positive full scale voltage shown in the Coding Table.

INPUT CODE	UNIPOLAR OPERATION—STRAIGHT BINARY			
MSB LSB	0 TO +5V	0 TO +10V	0 TO −2MA	0 TO −4MA
1 1 1111 1111	+4.995V	+9.990	−1.998 MA	−3.996
1 1 1000 0000	+4.375	+8.750	−1.750	−3.500
1 1 0000 0000	+3.750	+7.500	−1.500	−3.000
1 0 0000 0000	+2.500	+5.000	−1.000	−2.000
0 1 0000 0000	+1.250	+2.500	−0.500	−0.100
0 0 0000 0001	+0.005	+0.010	−0.002	−0.004
0 0 0000 0000	0.000	0.000	0.000	0.000

INPUT CODE	BIPOLAR OPERATION—OFFSET BINARY CODING			
MSB LSB	±5V	±10V	±1MA	±2MA
1 1 1111 1111	+4.990V	+ 9.980V	−0.998MA	−1.996MA
1 1 1000 0000	+3.750	+ 7.500	−0.750	−1.500
1 1 0000 0000	+2.500	+ 5.000	−0.500	−1.000
1 0 0000 0000	0.000	0.000	0.000	0.000
0 1 0000 0000	−2.500	− 5.000	+0.500	+1.000
0 0 0000 0001	−4.990	− 9.980	+0.998	+1.996
0 0 0000 0000	−5.000	−10.000	+1.000	+2.000

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PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

8-Bit Monolithic D/A Converter with Input Register Model DAC-UP8B

FEATURES

- **Input Register**
- **Internal Reference**
- **Voltage Output**
- **Low Cost**
- **8-Bit Resolution**

GENERAL DESCRIPTION

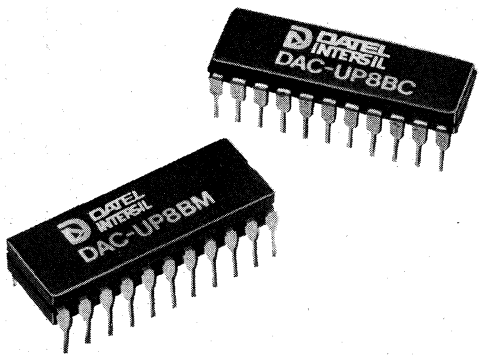
The DAC-UP8BC and DAC-UP8BM are 8-bit monolithic DAC's with internal registers. Contained in the 22 pin DIP is a 8-bit DAC, stable reference, a high-speed output amplifier and an 8-bit input latch. These microprocessor compatible converters are ideal for low cost applications.

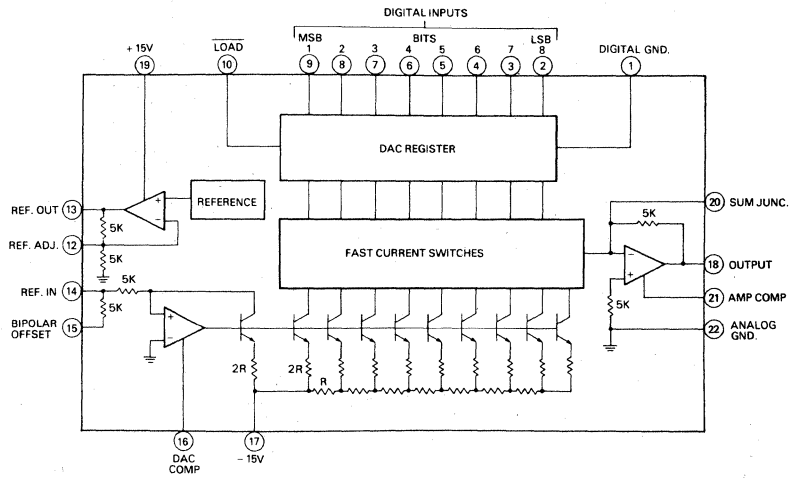
The output voltage range is 0 to + 10V for unipolar mode and ± 5V for bipolar. Typical settling time is 2 μsec for a full scale change. Either the internal reference or an external reference can be used to bias the current switching network. The converter can function as a multiplying DAC by varying the reference input voltage. The reference and output amplifier are short circuit protected.

The input register is controlled by an enable line (LOAD). When low, the registers are transparent and any change on the digital input pins will be reflected on the analog output. A high state level will latch this digital information, and the data is retained until this enable line goes low. The data and latch enable input lines have low input load currents.

The DAC design consists of 8 fast-switching current sources, a diffused R-2R resistor ladder network and a control amplifier. The diffused resistor network gives excellent temperature tracking resulting in a gain temperature coefficient of 30 ppm/°C. This bipolar monolithic fabrication results in excellent linearity and temperature coefficient.

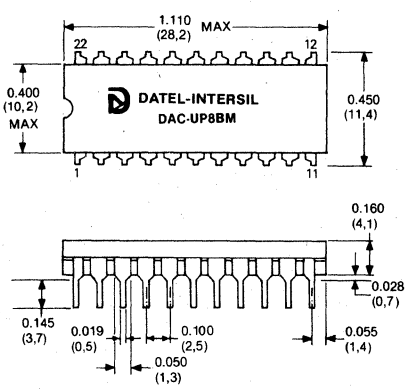
With an accuracy of .19% the device is monotonic (no missing codes) over the entire operating temperature range. Power supply requirements are ± 12V to ± 18V. The operating temperature range of the DAC-UP8BC is 0 to + 70 °C while the DAC-UP8BM operates from − 55 °C to + 125 °C.



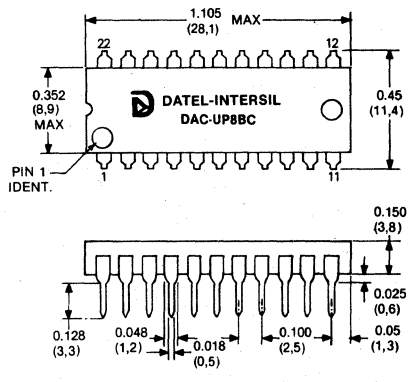


MECHANICAL DIMENSIONS INCHES (MM)

CERAMIC PACKAGE DAC-UP8BM



PLASTIC PACKAGE DAC-UP8BC



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SPECIFICATIONS, DAC-UP8BC & DAC-UP8BM

(Typical at 25°C, ±15V Supply, Ref. In = +5V unless otherwise noted)

MAXIMUM RATINGS

Positive Supply, pin 19	+ 18V
Negative Supply, pin 17	− 18V
Digital Input Voltage, pins 2-10	+ 18V
Reference Input, pin 14	+ 12V
Summing Junction, pin 20	+ 12V

INPUTS

Resolution	8 bits
Coding, unipolar output	Straight Binary
Coding, bipolar output	Offset Binary
Input Logic Level, bit ON ("1")	+ 2.0V to + 5.5V @ 10 μA
Input Logic Level, bit OFF ("0")	0V to + 0.8V @ − 50 μA
Load Input	HI ("1") = Hold Data LO ("0") = Transfer Data
Load Pulse Width[1]	200 nsec min.
Reference Input Voltage	+ 5V ± 10%
Reference Input Resistance	5K
Reference Input Slew Rate	25V/μsec.

OUTPUT

Output Voltage Range, unipolar	0 to +10V
Output Voltage Range, bipolar	± 5V
Output Current	5mA
Output Resistance	5 ohms
Reference Output Voltage	+ 5V ± 10%
Reference Output Current	5mA

PERFORMANCE

Linearity Error	± ½ LSB max.
Differential Linearity Error	± ½ LSB
Monotonicity	8 Bits over oper. temp. range
Gain Error	Adjustable to zero
Zero Error	Adjustable to zero
Gain Tempco	20 ppm/°C
Zero Tempco, Unipolar	5 ppm/°C of FS.
Offset Tempco, Bipolar	10 ppm/°C of FS.
Reference Tempco	60 ppm/°C
Settling Time to ½ LSB[2]	2 μsec
Power Supply Rejection	± 1mV/V

POWER REQUIREMENT

Rated Power Supply Voltage	± 15V DC
Power Supply Voltage Range	± 12 to ± 18V DC
Supply Current, quiescent	+ 7mA, − 10mA

PHYSICAL-ENVIRONMENTAL

Operating Temperature Range	0°C to + 70°C (BC) 55°C to +125°C (BM)
Storage Temperature Range	− 65°C to +150°C
Package Type	22 pin plastic (BC) 22 pin ceramic (BM)

NOTES:

1. See Timing Diagram
2. For 10V change

TECHNICAL NOTES

1. It is recommended that the ± 15V power input pins both be bypassed to ground with 0.1 μf ceramic capacitors. This precaution will assure noise free operation of the converter.

2. Both the Output (pin 18) and Reference Output (pin 13) are short circuit protected. Output short circuit current is typically 40 mA for the Output and 15 mA for the Reference Output.

3. The "LOAD" control pin is a level triggered input which causes the register to hold data with a logic "1" input state and transfer data to the DAC with a logic "0" input.

4. A Setup Time of 200 nsec. minimum must be allowed for the input data before the LOAD input goes from LO to HI. In addition, a 50 nsec. minimum Hold Time must be allowed for the input data after the LOAD input goes from LO to HI. The minimum pulse width for the LOAD input is 200 nsec. The maximum update rate is determined by the output settling time. See Timing Diagram.

5. The output settling time may be decreased somewhat by decreasing the value of the 50 pF feedback capacitor from the amplifier Output (pin 18) to the Summing Junction (pin 20). The minimum capacitance value is 10 pF.

6. The gain temperature coefficient of the DAC-UP8B without the internal reference is 20 ppm/°C. By using the internal reference, which has a tempco of 60 ppm/°C, a total tempco of 80 ppm typical results for the converter. If greater temperature stability is required, a more stable external reference should be used.

7. The data inputs (Bits 1 through 8) are high impedance inputs which give minimal logic loading. For an input LO, the current that must be sinked is only 50 μA maximum, or about 1/32 of a standard TTL load. This minimizes the loading of the DAC-UP8B on a data bus.

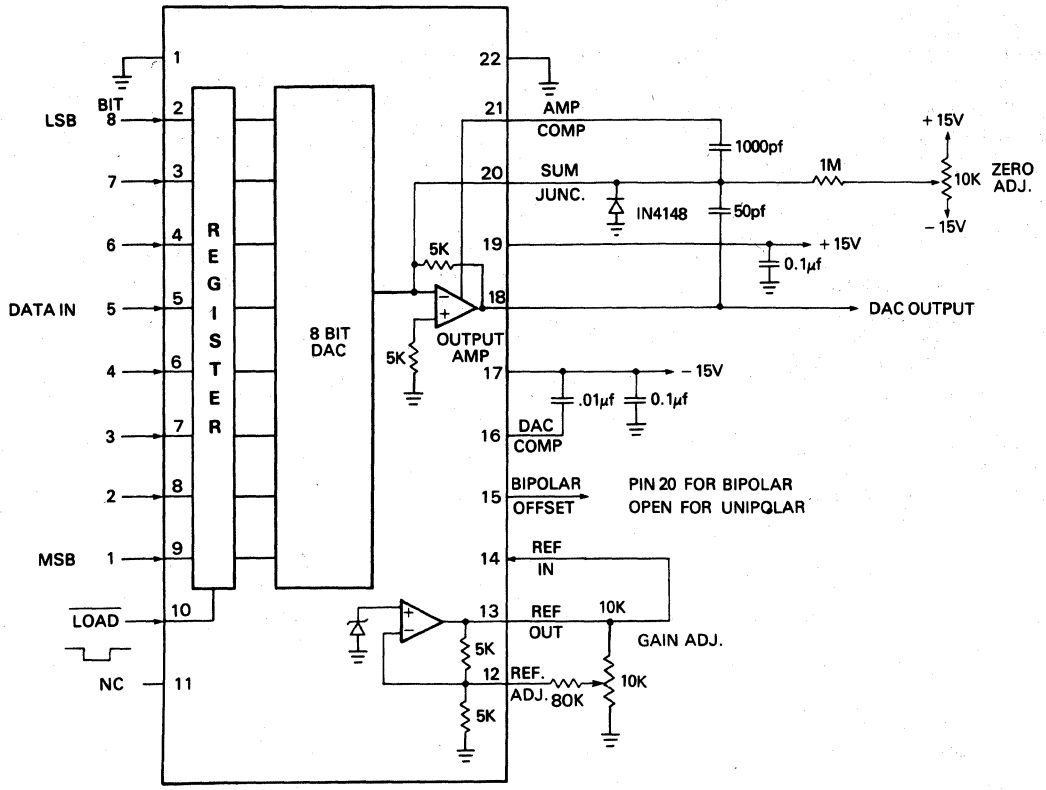
ORDERING INFORMATION

MODEL	OPERATING TEMP RANGE	CASE
DAC-UP8BC	0 to 70°C	Plastic
DAC-UP8BM	− 55 to 125°C	Ceramic

Trimming Potentiometers: TP10K

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

CONNECTION AND CALIBRATION



CALIBRATION PROCEDURE

1. Select the desired output range and connect as shown in OUTPUT RANGE SELECTION table.
2. Apply a logic "0" to $\overline{\text{LOAD}}$ (pin 10).
3. **Zero and Offset Adjustments**
   For unipolar operation, set all digital inputs to "0" and adjust ZERO ADJ for zero output voltage. For bipolar operation, set all digital inputs to "0" and adjust ZERO ADJ for negative full scale voltage. of – 5.000V.
4. **Gain Adjustment**
   For either unipolar or bipolar operation, set all digital inputs to "1" and adjust FULL SCALE ADJ for the positive full scale voltage of + 9.961V (unipolar) or + 4.961V (bipolar).

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	DIGITAL GND	12	REF ADJ
2	BIT 8 IN (LSB)	13	REF OUT
3	BIT 7 IN	14	REF IN
4	BIT 6 IN	15	BIPOLAR OFFSET
5	BIT 5 IN	16	DAC COMP
6	BIT 4 IN	17	– 15V
7	BIT 3 IN	18	OUTPUT
8	BIT 2 IN	19	+ 15V
9	BIT 1 IN (MSB)	20	SUM JUNCTION
10	$\overline{\text{LOAD}}$	21	AMP COMP
11	NC	22	ANALOG GND

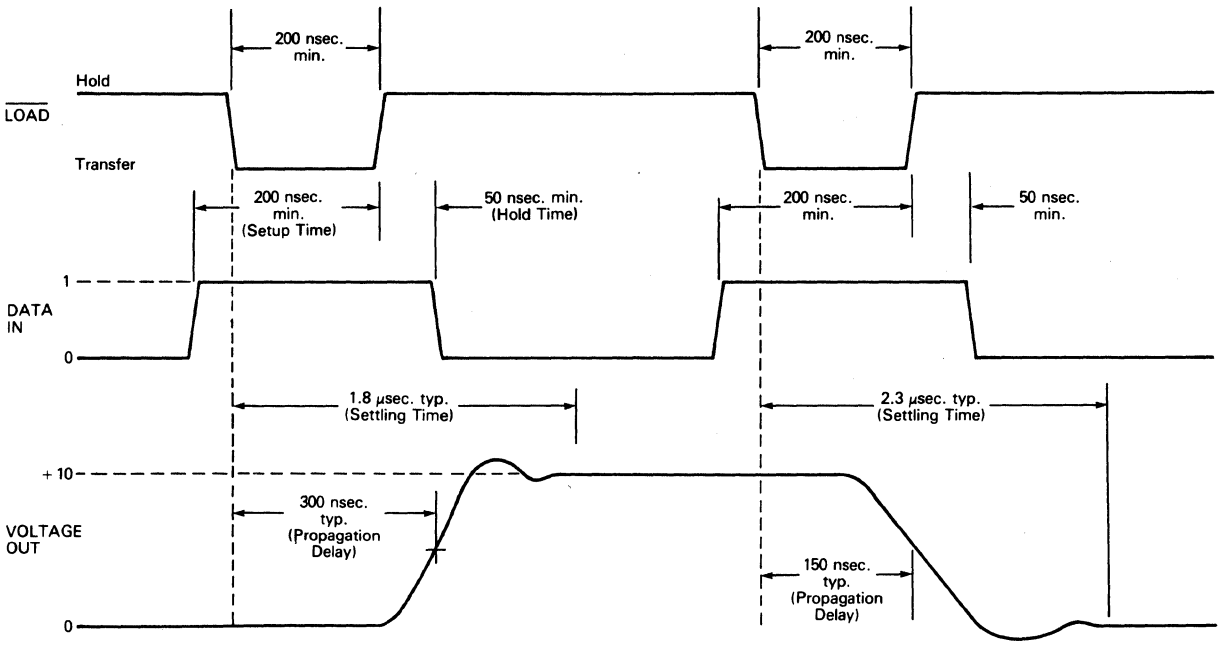
CODING TABLE

INPUT CODE MSB				LSB				OUTPUT RANGES 0 to + 10V	± 5V
1	1	1	1	1	1	1	1	+ 9.961V	+ 4.961V
1	1	1	0	0	0	0	0	+ 8.750	+ 3.750
1	1	0	0	0	0	0	0	+ 7.500	+ 2.500
1	0	0	0	0	0	0	0	+ 5.000	0.000
0	1	0	0	0	0	0	0	+ 2.500	– 2.500
0	0	0	0	0	0	0	1	+ 0.039	– 4.961
0	0	0	0	0	0	0	0	0.000	– 5.000

OUTPUT RANGE SELECTION

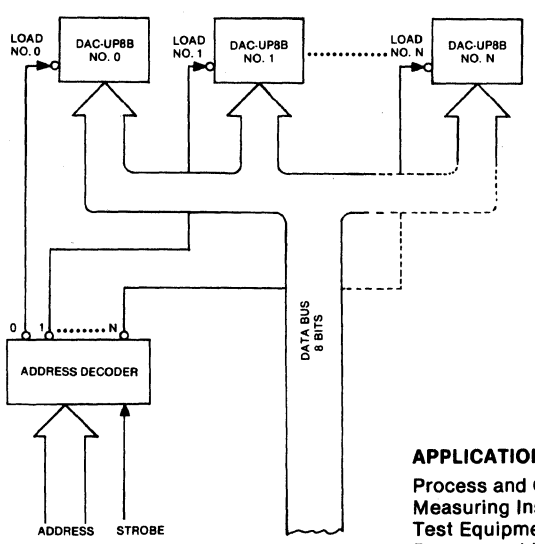
MODE	RANGE	CONNECTION
Unipolar	0 to +10V	Pin 15 open
Bipolar	± 5V	Pin 15 to 20

TIMING DIAGRAM



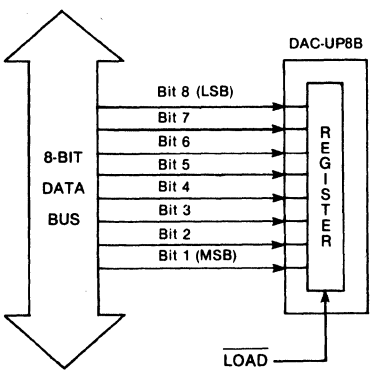
APPLICATIONS

INTERFACING TO 8 BIT DATA BUS



APPLICATIONS

Process and Control
Measuring Instruments
Test Equipment
Programmable Power Supplies
Computer I/O Equipment



This illustrates the connection for loading parallel data into the input register. The register circuit is a static latch and is controlled by the $\overline{\text{LOAD}}$, active low. When the data is stable on the data inputs (bits 1-8), it can be transferred on the positive edge of the $\overline{\text{LOAD}}$ pulse. The voltage levels on the data bus should be stable for at least 200 nsec before $\overline{\text{LOAD}}$ goes HI. The minimum pulse width of the $\overline{\text{LOAD}}$ command is 200 nsec.

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High Speed, 8 Bit Monolithic Digital-to-Analog Converter Model DAC-08B

FEATURES

- 85 nsec Settling Time
- −10 to +18 Volt Compliance
- ±4.5 to ±18 Volt Supply
- 8 Bit Resolution
- 1 or 2 Quadrant Multiplication
- Low Cost

GENERAL DESCRIPTION

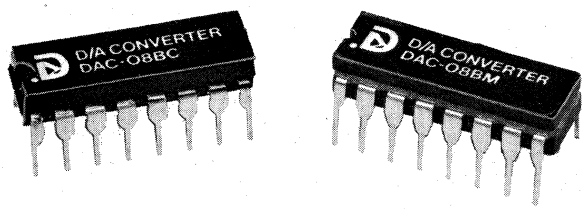
The DAC-08BC and DAC-08BM provide very high speed performance coupled with low cost and application flexibility. These units have guaranteed full 8-bit monotonicity with nonlinearity of 0.19% over the full operating temperature range. High speed current steering switches achieve 85 nanosecond settling time with a very low glitch for full scale changes. A large output voltage compliance range (−10 to +18 Volts) allows direct current to voltage conversion with just an output resistor, omitting the need for an op amp in many cases.

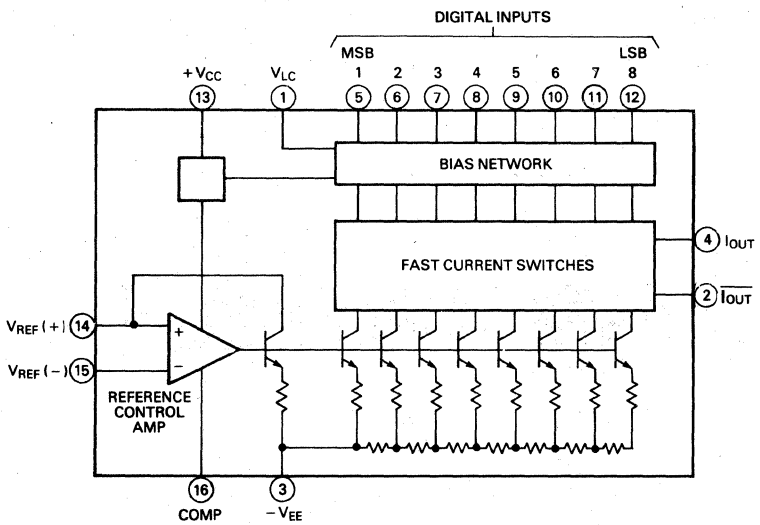
The DAC-08 consists of 8 fast-switching current sources, a diffused R-2R resistor ladder, a bias circuit, and a reference control amplifier. The diffused resistor ladder gives excellent temperature tracking resulting in a gain temperature coefficient of 10 ppm/°C. The monolithic fabrication results in excellent linearity and tempco, fast output settling and low cost. Linearity is ±½ LSB.

An external reference current of 2 mA nominal programs the scale factor of the DAC. This reference current can also be varied, resulting in one or two quadrant multiplying operation. The output voltage can be unipolar or bipolar dependent upon the connection of the two complementary output sink currents.

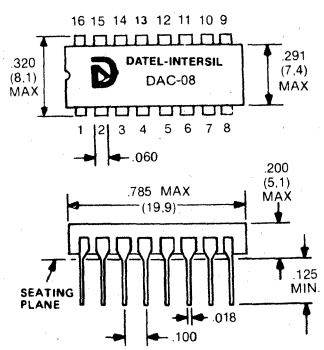
DAC-08 applications include fast A/D converters, waveform generators, audio encoder and attentuators, CRT display drivers, and high speed modems.

Power supply requirements are ±4.5V to ±18V. Operating temperature range is 0°C to 70°C for the DAC-08BC and −55°C to +125°C for the DAC-08BM. These models have equivalent specs and pinouts to industry standard DAC-08's.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	THRESHOLD CONTROL (VLC)
2	$\overline{IOUT}$
3	VEE
4	IOUT
5	BIT 1 IN (MSB)
6	BIT 2 IN
7	BIT 3 IN
8	BIT 4 IN
9	BIT 5 IN
10	BIT 6 IN
11	BIT 7 IN
12	BIT 8 IN (LSB)
13	VCC
14	VREF+
15	VREF−
16	COMPENSATION

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SPECIFICATIONS. DAC-08BC & DAC-08BM

(Typical at 25°C, Vs = ±15V, I_{REF} = 2.0 mA unless otherwise noted)

MAXIMUM RATINGS

V_{CC} Supply to V_{EE} Supply	36V
Digital Input Voltage	$-V_{EE}$ to $-V_{EE}$ plus 36V
V_{LC}	$-V_{EE}$ to $+V_{CC}$
Reference Input Voltage	$-V_{EE}$ to $+V_{CC}$
Reference Input Current	5.0 mA

INPUTS

Resolution	8 Bits
Coding, Unipolar Output	Straight Binary
Coding, Bipolar Output	Offset Binary
Input Logic Level, Bit ON ("1")	+2.0V min. @ +10.0μA
Input Logic Level, Bit OFF ("0")	+0.8V max. @ −10.0μA[1]
Nominal Reference Current	2.0 mA
Reference Bias Current	−1.0 μA
Reference Input Slew Rate	8 mA/μsec

OUTPUTS

Output Current, I_{REF} = 2.0 mA	1.99 mA ±.05 mA[2]
Output Current Range, V_{EE} = −5V	0 to 2.1 mA
Output Current Range, V_{EE} = −7 to −18V	0 to 4.2 mA
Output Current, all bits OFF	±0.2μA typ. ±2.0μA max.
Full Scale Symmetry	±1.0 μA typ. ±8.0 μA max.
Output Voltage Compliance	−10 to +18V

PERFORMANCE

Relative Accuracy	±½ LSB (±0.19%) max.
Nonlinearity	±½ LSB (±0.19%) max.
Differential Nonlinearity	±½ LSB (±0.19%)
Full Scale Tempco	±10 ppm/°C typ. ±50 ppm/°C max.
Settling Time, 2 mA to ½LSB	85 nsec. typ., 150 nsec. max.
Propagation Delay	60 nsec. max.
Power Supply Sensitivity, I_{REF} = 1 mA	±0.002%/%

POWER REQUIREMENTS

V_{CC}	+4.5V to +18V
V_{EE}	−4.5V to −18V
Power Supply Current, I_{REF} = 1.0mA	
V = ±5V	+3.8, −5.8 mA max.
Power Supply Current, I_{REF} = 2.0mA	
V = +5V, −15V	+3.8, −7.8 mA max.
V = ±15V	+3.8, −7.8 mA max.

PHYSICAL-ENVIRONMENTAL

Operating Temp Range	
DAC-08BC	0°C to 70°C
DAC-08BM	−55°C to 125°C
Storage Temp Range	−65°C to −150°C
Package	16 Pin Dip

NOTES

1. For TTL, DTL Interface, V_{LC} = 0V. For other digital interfaces see TECHNICAL NOTE 3.
2. I_{OUT} (Pin 4) + I_{OUT} (Pin 2) = Output Current.

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	PACKAGE
DAC-08BC	0°C to 70°C	Plastic
DAC-08BM	−55°C to +125°C	Ceramic

THESE D/A CONVERTERS ARE COVERED BY GSA CONTRACT.

TECHNICAL NOTES

1. The DAC-08 series is a multiplying D/A converter in which the output current is a product of the digital word and the input reference current. Excellent performance is obtained for I_{REF} from 4.0 mA to 4.0 μA. Monotonic operation is maintained from 4.0 mA to 100 μA. The full scale output current is a linear function of the reference current and is given by:

$$I_{FS} = \frac{255}{256} \times I_{REF} \quad (I_{REF} \text{ is current at Pin 14})$$

2. **Reference Amplifier Set-up.** If a regulated power supply is used as the reference, a resistor divider should be used with the junction by-passed to gnd with a 0.1 μf capacitor. TTL logic supplies are not recommended to be used as the reference. AC and DC reference applications will require the reference amplifier to be compensated using a capacitor (C_C)from pin 16 to V_{EE}. For fixed reference application (DC). a 0.01 μF capacitor is recommended. For AC reference applications, the value of C_C depends on the impedance present at pin 14. For R_{REF} values of 1.0, 2.5 and 5.0 KΩ, minimum values of C_C are 15, 37 and 75 pf respectively. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin. See Graph on Reference Input Frequency Response. Low R_{REF} values enable small C_C achieving highest throughput on V_{REF}. If pin 14 is driven by a high impedance such as a transistor current source, the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{REF} = 1.0 KΩ and C_C = 15 pf, the reference amplifier slews at 4.0 mA/μsec. enabling a transition from I_{REF} = 0 to I_{REF} = 2.0 mA in 500 nsec.

3. **Interfacing Various Logic Families.** The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. A large input swing capability allows adjustable logic threshold voltage and 200 μA max source current on pin 1. Minimum input logic swing and minimum logic threshold voltage is given by V_{EE} +(I_{REF} x 1.0 kΩ) +2.5V. Logic threshold is adjusted by appropriate voltage at V_{LC}. Interfacing Various Logic Families Diagram shows appropriate connections. Fastest settling times are obtained when V_{LC} sees a low impedance. Use .01 μF by-pass capacitors whenever possible.

4. **Analog Output Currents.** Both true and complemented output sink currents are provided, $I_O + \overline{I_O} = I_{FS}$. Both outputs can be used simultaneously. If one of the outputs is not required, it must be connected to ground or a point capable of sourcing I_{FS}. **Do not leave unused output pin** (I_O or $\overline{I_O}$) **open.** The compliance voltage is the voltage swing on output pin without affecting DAC accuracy. Positive compliance is 36V above V_{EE} and is independent of V +. Negative compliance is V_{EE} + (I_{REF} x 1kΩ) +2.5V.

5. **Settling Time.** The DAC-08 is capable of extremely fast settling times, typically 85 nsec. at I_{REF} = 2.0 mA. Judicious circuit design and careful board layout must be employed to obtain full performance. The output capacitance of the DAC including the package is approximately 15 pf; therefore the output RC time constant dominates at $R_L > 500\Omega$.

   Settling time remains essentially constant for I_{REF} values down to 1.0 mA, with gradual increases for lower I_{REF} values. The switching transients (glitches) are very low and may be further reduced by small capacitive loads at the output. Settling time will be increased slightly.

6. **Power Supplies.** The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq 1$ mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range. For example,

TECHNICAL NOTES (Cont'd)

operation at −4.5V with I_{REF} = 2 mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network. It is recommended that V_{CC} and V_{EE} always be bypassed to ground with at least 0.1 μf capacitors.

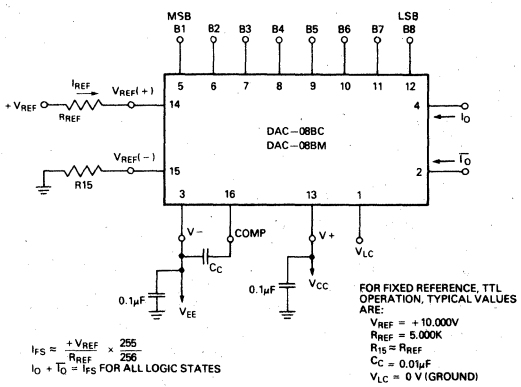
Symmetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible, as no ground connection is required; however, an artificial ground may be useful to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows:
$P_d = (I+)(V+) + (I-)(V-) + (2\ I_{REF})(V-)$. A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

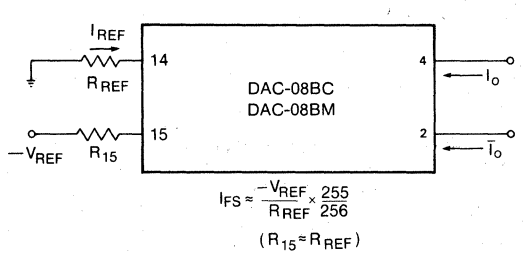
7. **Temperature Performance.** For most applications, a +10.0 Volt reference is recommended for optimum full scale temperature coefficient performance. Full scale trimming may by accomplished by adjusting I_{REF} (changing value of R_{REF}). R_{REF} and R_L should be selected for similar temperature coefficient to minimize accuracy error. Settling time of the DAC decreases approximately 10% at −55°C and increases 15% at 125°C.

APPLICATION DIAGRAMS

BASIC POSITIVE REFERENCE OPERATION

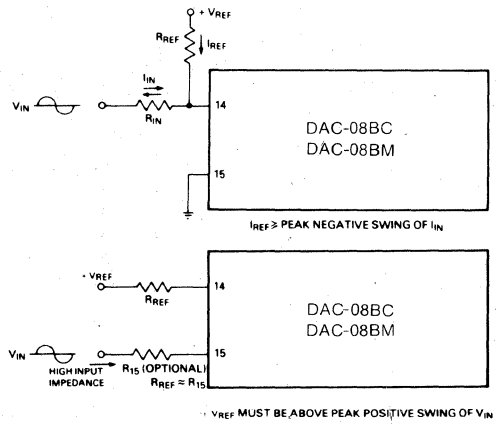


BASIC NEGATIVE REFERENCE OPERATION

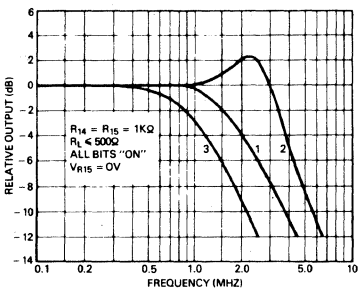


APPLICATION DIAGRAMS (Cont'd)

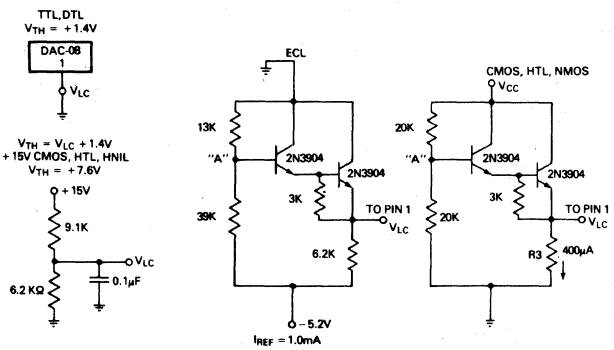
ACCOMMODATING BIPOLAR REFERENCES



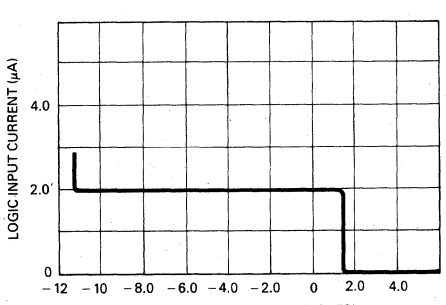
REFERENCE INPUT FREQUENCY RESPONSE



INTERFACING VARIOUS LOGIC FAMILIES

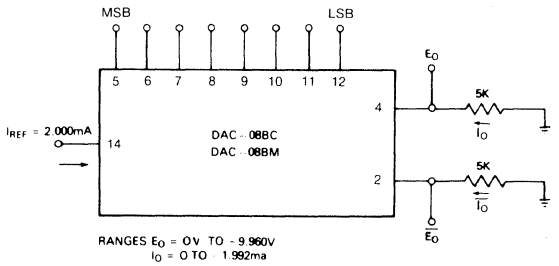


LOGIC INPUT CURRENT VS. INPUT VOLTAGE



APPLICATION DIAGRAMS (Cont'd)

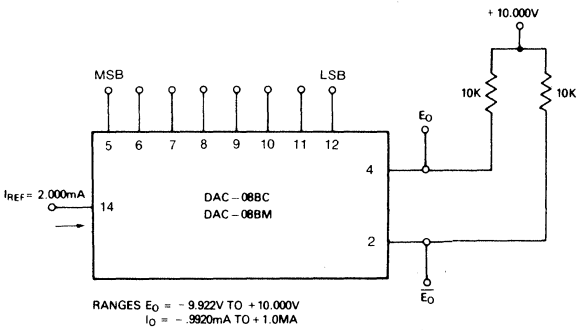
BASIC UNIPOLAR NEGATIVE OPERATION



RANGES E_O = 0V TO -9.960V
I_O = 0 TO -1.992ma

SEE CODING TABLE

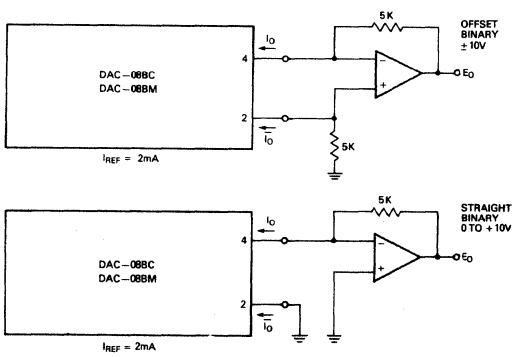
BASIC BIPOLAR OUTPUT OPERATION



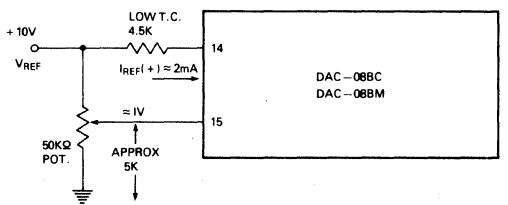
RANGES E_O = -9.922V TO +10.000V
I_O = -.9920mA TO +1.0MA

SEE CODING TABLE

VOLTAGE OUTPUT OPERATION



RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT



CALIBRATION AND CODING TABLES

CALIBRATION PROCEDURE

1. Select the desired output range by means of the feedback resistor of the external operational amplifier and the externally programmed reference current.

2. **Zero and Offset Adjustments**
   For unipolar operation, set all digital inputs to "0" and adjust the output amplifier ZERO ADJUSTMENT for zero output voltage. For bipolar operation, set all digital inputs to "0" and adjust the OFFSET ADJUSTMENT for the negative full scale voltage shown in the Coding Table.

3. **Gain Adjustment**
   For either unipolar or bipolar operation, set all digital inputs to "1" and adjust the GAIN ADJUSTMENT for the positive full scale voltage shown in the DAC-08B Coding Table.

UNIPOLAR OPERATION—STRAIGHT BINARY CODING

For 5k load resistors at pins 2 and 4

INPUT CODE	E_O	$\overline{E_O}$	I_O	$\overline{I_O}$
1111 1111	−9.961	0.000	1.992	0.000
1110 0000	−8.750	−1.211	1.750	0.242
1100 0000	−7.500	−2.461	1.500	0.492
1000 0000	−5.000	−4.961	1.000	0.992
0100 0000	−2.500	−7.461	0.500	1.492
0000 0001	−0.039	−9.922	0.008	1.984
0000 0000	0.000	−9.961	0.000	1.992

BIPOLAR OPERATION—OFFSET BINARY CODING

For 10k load resistors from pins 2 and 4 to +10V.

INPUT CODE	E_O	$\overline{E_O}$
1111 1111	− 9.922	+10.000
1110 0000	− 7.500	+ 7.578
1100 0000	− 5.000	+ 5.078
1000 0000	0.000	+ 0.078
0100 0000	+ 5.000	− 4.922
0000 0001	+ 9.922	− 9.844
0000 0000	+10.000	− 9.922

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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Monolithic, High Performance 12 Bit D/A Converter Model DAC-681

FEATURES

- **12 Bit Resolution**
- **300 nsec. Settling Time**
- **±10ppm/°C Max. Tempco**
- **5 Output Ranges**
- **±¼ LSB Linearity**
- **562 Pin Compatibility**

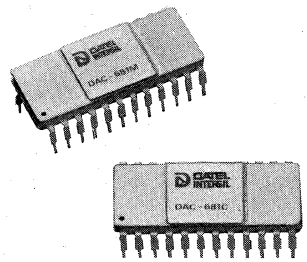
GENERAL DESCRIPTION

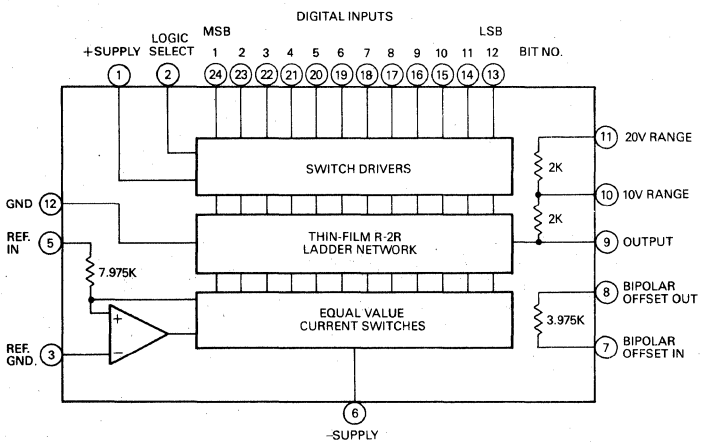
The DAC-681 is a new high performance monolithic 12 bit D/A converter fabricated with advanced bipolar technology. The circuit uses a precision, laser-trimmed thin film R-2R ladder network driven by equal-value switched current sources to achieve ¼ LSB typical linearity, 300 nsec. settling time and ±10 ppm/°C max. gain tempco.

The DAC-681 operates from TTL or CMOS input logic and provides a 0 to 5 mA or ±2.5 mA output current. The converter contains tracking feedback and bipolar offsetting resistors to provide five output voltage ranges when used with an external operational amplifier: 0 to +5V, 0 to +10V, ±2.5, ±5V, and ±10V. Since these resistors closely track the R-2R ladder with temperature, gain stability of better than 10 ppm/°C is achieved. Differential linearity error is ¼ LSB typical and ½ LSB maximum, with output monotonicity guaranteed over the operating temperature range.

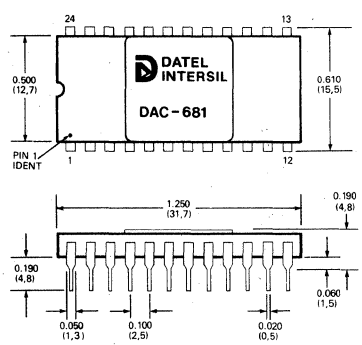
Output settling time for a full scale change to ½ LSB is 300 nsec. typical and 400 nsec. maximum.

The DAC-681 features pin compatibility with 562 type DAC's while offering superior performance to these earlier devices. The package is a 24 pin hermetically sealed ceramic DIP; power requirement is +5V to +15V and −15 VDC. There are two basic models: DAC-681C operates over 0°C to 70°C while DAC-681M operates over −55°C to +125°C.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+ SUPPLY	13	BIT 12 IN (LSB)
2	LOGIC SELECT	14	BIT 11 IN
3	REF. GROUND	15	BIT 10 IN
4	N.C.	16	BIT 9 IN
5	REFERENCE IN	17	BIT 8 IN
6	− SUPPLY	18	BIT 7 IN
7	BIP. OFF IN	19	BIT 6 IN
8	BIP. OFF OUT	20	BIT 5 IN
9	OUTPUT	21	BIT 4 IN
10	10V RANGE	22	BIT 3 IN
11	20V RANGE	23	BIT 2 IN
12	GROUND	24	BIT 1 IN (MSB)

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SPECIFICATIONS, DAC-681

Typical at 25°C, +5V & −15V Supplies, +10V Reference unless otherwise noted.

	DAC-681C	DAC-681M
MAXIMUM RATINGS		
Positive Supply, pin 1	+20V	*
Negative Supply, pin 6	−20V	*
Reference Input, pin 5	±Supply	*
Reference Ground, pin 3	0V	*
Digital Inputs, pins 13-24	−1V to +12V	*
Logic Select Input, pin 2	−1V to +12V	*
Output, pin 9	+Supply, −5V	*
Resistors, pins 7, 8, 10, 11	±Supply	*
INPUTS		
Resolution	12 Bits	*
Coding, unipolar output	Straight Binary	*
Coding, bipolar output	Offset Binary	*
Input Logic Level, bit ON ("1")[1]	+2.0 min. @ 100nA max.	
Input Logic Level, bit OFF ("1")[1]	+0.8V max. @ −100μA max.	
Reference Input Voltage	+10V	*
Reference Input Resistance	8K	*
OUTPUTS		
Output Current, unipolar	0 to −5 mA	*
Output Current, bipolar	±2.5 mA	*
Output Voltage Ranges, unipolar	0 to +5V	*
	0 to +10V	*
Output Voltage Ranges, bipolar	±2.5V	*
	±5V	*
	±10V	*
Output Voltage Compliance	±1V	*
Output Resistance	1K	*
Output Capacitance	20 pF	*
PERFORMANCE		
Linearity Error, max.	±½ LSB	±¼ LSB
Linearity Error Over Temp.,	±1 LSB	±½ LSB
Differential Linearity Error, typ.	±½ LSB	±¼ LSB
Monotonicity	Over Oper. Temp. Range	
Gain Error, max.[2]	±0.25%	*
Unipolar Zero Error, max.[2]	±0.05%	*
Bipolar Offset Error, max.[2]	±0.25%	*
Gain Tempco, max.[3]	±10 ppm/°C	±5 ppm/°C
Zero Tempco, max.[3]	±2 ppm/°C	±2 ppm/°C
Bipolar Offset Tempco, max.[3]	±5 ppm/°C	±5 ppm/°C
Settling Time to ½ LSB[4]	300 nsec. typ., 400 nsec. max.	
Power Supply Sensitivity	±7.5 ppm of FSR/% Supply	
Reference Slew Rate	6 mA/μsec.	*
Reference Bandwidth	10 MHz	*
POWER REQUIREMENT		
Rated Power Supply Voltage	+5 VDC, −15 VDC	
Positive Supply Range[6]	+4.75 VDC to +15 VDC	
Negative Supply Range	−15 VDC ±10%	
Power Supply Quiescent Current, max.	+9 mA, −28 mA	
PHYSICAL-ENVIRONMENTAL		
Operating Temp. Range	0°C to +70°C	−55°C to +125°C
Storage Temp. Range	−65° C to +150°C	*
Package, Hermetically Sealed	24 pin ceramic	*

*Specifications same as first column

NOTES:

1. + Supply must be +5V ±5% for DAC-681C and +5V ±10% for DAC-681M. For operation with CMOS logic see Technical Note 1.
2. Adjustable to zero using external potentiometers. Specified error is for 24.9 ohm trim resistors and external op amp using internal feedback resistor.
3. Using external op amp and internal feedback and offset resistor. Zero Tempco and Bipolar Offset Tempco are in ppm/°C of FSR (Full Scale Range)
4. For full scale change: all bits ON-to-OFF, or all bits OFF-to-ON.
5. See Technical Note 1.

TECHNICAL NOTES

1. For TTL input logic, pin 2 should be connected to pin 12 and the + supply must be +5 VDC (±5% for DAC-681C and ±10% for DAC-681M). For CMOS input logic, connect pin 2 to pin 1 and use any + supply voltage from +4.75V to +12 VDC. CMOS threshold levels are then + Vs × 0.7 for bit ON and +Vs × 0.3 for bit OFF. Logic input current is the same as that specified for TTL.
2. Gain and bipolar offset errors are adjustable to zero by means of two 50 ohm trimming pots. The adjustment range is ±0.3% of FSR for gain and ±0.6% of FSR for bipolar offset. The unipolar zero error is adjustable to zero by means of the offset adjustment of the external output amplifier.
3. The output voltage compliance range of ±1V should not be exceeded or else accuracy will be affected. If a resistor load is driven instead of an op amp summing junction then the maximum resistor value is 200 ohms for unipolar operation and 400 ohms for bipolar operation.
4. Output settling time is specified for current output and is measured with a small current sampling resistor to ground (100 ohms). Voltage output settling time depends on the output operational amplifer used. Datel's AM-500 is recommended for about 500 nsec. settling and AM-452-2 is recommended for about 1.5 μsec. settling. Both should be used with a 3-20 pF variable compensating capacitor across the feedback resistor which should be adjusted for optimum settling time.
5. For best high speed performance, both power supplies should be bypassed with 1 μF electrolytics in parallel with 0.01 μF ceramic capacitors as close as possible to the ± supply pins.
6. The gain and bipolar offset temperature coefficients are specified with the internal feedback and offset resistors used in conjunction with an external operational amplifier. This is because these resistors track the R-2R ladder with temperature and therefore the tempco's do not depend on absolute resistor tempco. The tempco of the external +10V reference must also be included in the total converter tempco, however.
7. Because of the DAC-681 circuit which incorporates equally weighted current sources driving an R-2R ladder network, the turn ON and turn OFF times are virtually symmetrical, resulting in low output glitches compared with other DAC's. The major carry glitch typically has an amplitude of 14% of FSR. The time duration to 90% complete is typically 35 nsec.
8. The DAC-681 wideband output noise with all bits ON is typically 100 μV P-P over 0.1 Hz to 5 MHz.

ORDERING INFORMATION

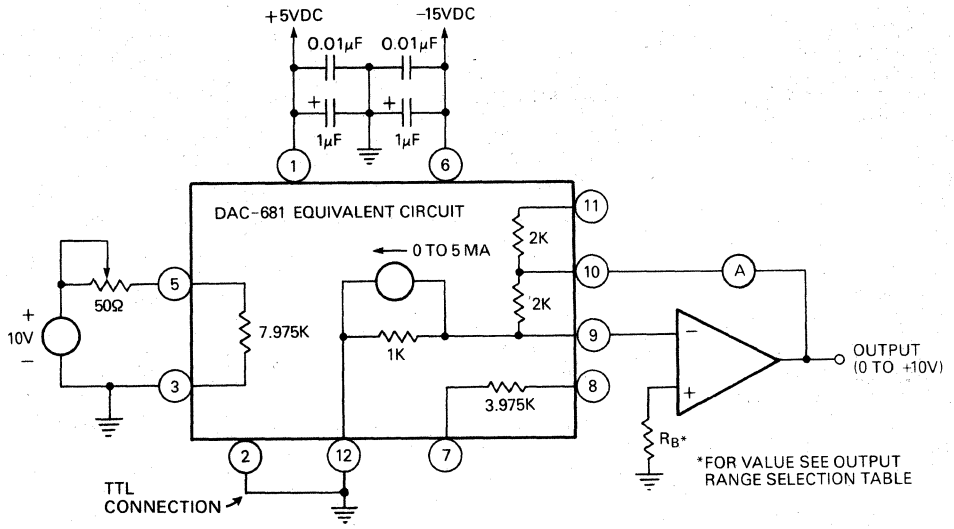
Model	Temp. Range
DAC-681C	0 to 70°C
DAC-681M	−55 to +125°C

Trimming Potentiometer: TP50

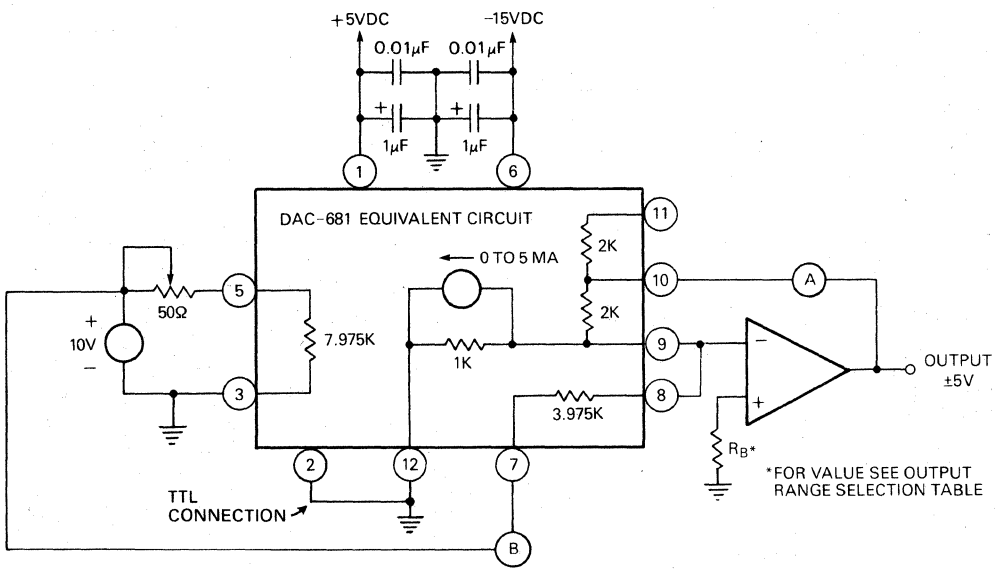
THESE CONVERTERS ARE COVERED BY GSA CONTRACT.

STANDARD CONNECTIONS

UNIPOLAR OPERATION—See Output Range Selection Table



BIPOLAR OPERATION—See Output Range Selection Table



OUTPUT VOLTAGE RANGE SELECTION (See Connection Diagrams Above)

OUTPUT VOLTAGE RANGE	CONNECT THESE PINS TOGETHER				R_B, BIAS COMP. RESISTOR*
0 to +5V	A & 10	9 & 11			510
0 to +10V	A & 10				680
±2.5V	A & 10	9 & 11	8 & 9	7 & B	430
±5V	A & 10	8 & 9	7 & B		560
±10V	A & 11	8 & 9	7 & B		680

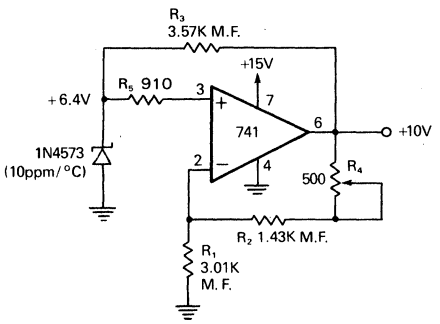
*Carbon composition resistor value used from amplifier + input terminal to ground to compensate for offset due to bias current.

CALIBRATION AND APPLICATION

CODING TABLE—See Calibration Procedure

INPUT CODE	OUTPUT VOLTAGE RANGE				
	0 TO +5V	0 TO +10V	±2.5V	±5V	±10V
1111 1111 1111	+4.9988V	+9.9976V	+2.4988V	+4.9976V	+9.9951V
1100 0000 0000	+3.7500	+7.5000	+1.2500	+2.5000	+5.0000
1000 0000 0000	+2.5000	+5.0000	0.0000	0.0000	0.0000
0100 0000 0000	+1.2500	+2.5000	−1.2500	−2.5000	−5.0000
0000 0000 0001	+0.0012	+0.0024	−2.4988	−4.9976	−9.9951
0000 0000 0000	0.0000	0.0000	−2.5000	−5.0000	−10.0000

+10V REFERENCE CIRCUIT



Adjust R_4 for +10.000V output. For best stability R_1 & R_2 should track each other closely with temperature. R_4 should be a low tempco trimming pot or else a selected metal film trim resistor.

CALIBRATION PROCEDURE

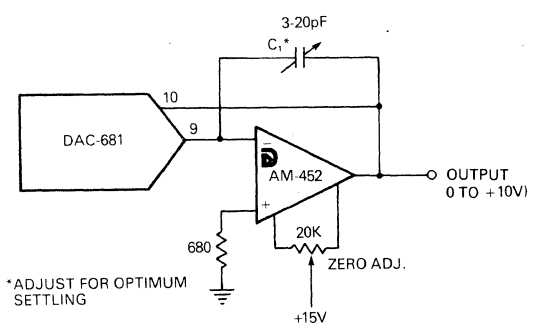
UNIPOLAR OPERATION

1. Set all digital inputs LO. Adjust the output amplifier offset for 0 volts output.
2. Set all digital inputs HI. Adjust Gain trimming pot for an output of +FS-1LSB.
   FS-1LSB = +9.9976V for 0 to +10V range.
   = +4.9988V for 0 to +5V range.

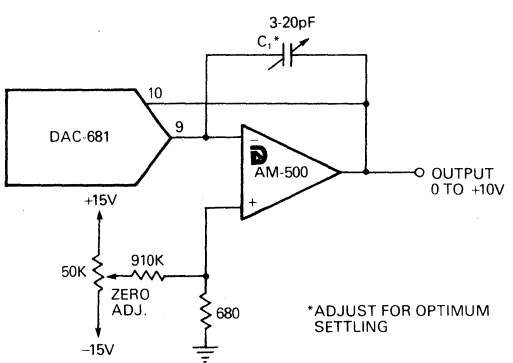
BIPOLAR OPERATION

1. Set all digital inputs LO. Adjust Bipolar Offset trimming pot for one of the following output voltages:
   −2.5V for ±2.5V range
   −5.0V for ±5V range
   −10.0V for ±10V range
2. Set bit 1 (MSB) input HI and all other digital inputs LO. Adjust Gain trimming pot for 0 volts output.

CIRCUIT FOR FAST VOLTAGE OUTPUT (≈1.5 μSEC. SETTLING)



CIRCUIT FOR FAST VOLTAGE OUTPUT (≈0.5 μSEC. SETTLING)



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10 & 12 Bit Monolithic Multiplying D/A Converters DAC-7520, DAC-7521 Series

FEATURES

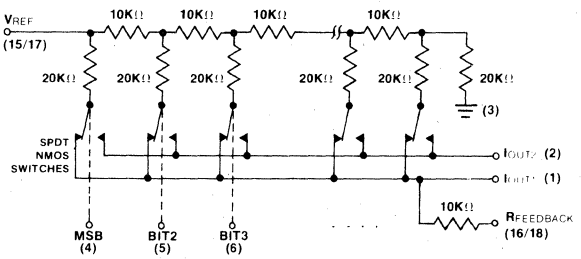
- **DAC-7520: 10 Bit Resolution; 10 Bit Linearity**
- **DAC-7521: 12 Bit Resolution; 10 Bit Linearity**
- **Low Power Dissipation: 20 mW (Max)**
- **Low Nonlinearity Tempco: 2 PPM of FSR/° C (Max)**
- **Current Settling Time: 500 nS to 0.05% of FSR**
- **Supply Voltage Range: +5V to +15V**
- **DTL/TTL/CMOS Compatible**
- **Full Input Static Protection**

GENERAL DESCRIPTION

The DAC-7520 and DAC-7521 are monolithic, high accuracy, low cost 10-bit and 12-bit resolution, multiplying digital-to-analog converters. DATEL-INTERSIL's thin-film on CMOS process enables 10-bit accuracy with DTL/TTL/CMOS compatible operation. Digital inputs are fully protected against static discharge by compensating diodes to ground and positive supply.

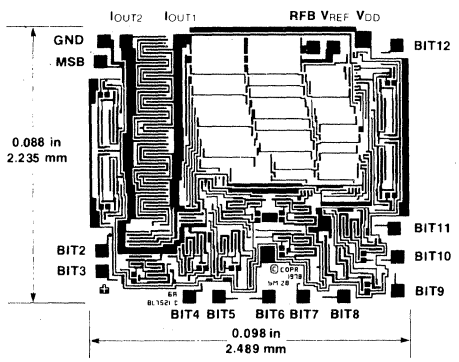
Typical applications for the DAC-7520 and DAC-7521 include: digital/analog interfacing, multiplication and division; programmable power supplies; CRT character generation; digitally controlled gain circuits, integrators and attenuators, etc.

FUNCTIONAL DIAGRAM



(Switches shown for Digital Inputs "High")

CHIP TOPOGRAPHY



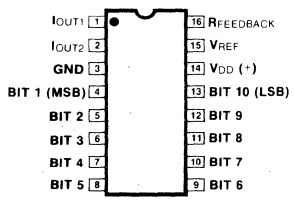
ORDERING INFORMATION

MODEL	RESOLUTION	OPER. TEMP. RANGE	PACKAGE
DAC-7520C	10 Bits	0 to +70° C	EPOXY
DAC-7520R		−25 to +85° C	CERDIP
DAC-7520M		−55 to +125° C	CERDIP
DAC-7521C	12 Bits	0 to +70° C	EPOXY
DAC-7521R		−25 to +85° C	CERDIP
DAC-7521M		−55 to +125° C	CERDIP

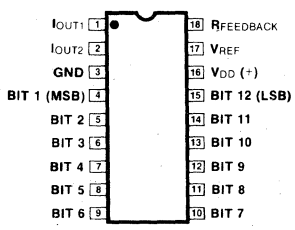
PIN CONFIGURATION

TOP VIEW

DAC-7520



DAC-7521



DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

DAC-7520, DAC-7521

ABSOLUTE MAXIMUM RATINGS (T_A = 25° C unless otherwise noted)

VDD (to GND) ..... +17V
VREF (to GND) ..... ±25V
Digital Input Voltage Range ..... VDD to GND
Output Voltage Compliance ..... −100mV to VDD
Power Dissipation (package)
up to +75° C ..... 450 mW
derates above +75° C by ..... 6 mW/° C

Operating Temperatures
C Versions ..... 0° C to +70° C
R Versions ..... −25° C to 85° C
M Versions ..... −55° C to +125° C
Storage Temperature ..... −65° C to +150° C

CAUTION: **1)** The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2) Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.

SPECIFICATIONS (VDD=+15V, VREF=+10V, TA=25° C unless otherwise specified)

PARAMETER	DAC-7520	DAC-7521	UNITS	LIMIT	TEST CONDITIONS	FIG.
DC ACCURACY (Note 1) Resolution	10	12	Bits			
Nonlinearity	0.05 (10-Bit)		% of FSR	Max	M: over −55° C to +125° C −10V≤VREF≤+10V	1
Nonlinearity Tempco	2		PPM of FSR/° C	Max		
Gain Error (Note 2)	0.3		% of FSR	Typ	−10V≤VREF≤+10V	
Gain Error Tempco (Note 2)	10		PPM of FSR/° C	Max		
Output Leakage Current (either output)	200		nA	Max	Over the specified temperature range	
Power Supply Rejection	±0.005		% of FSR/%	Typ		2
AC ACCURACY Output Current Settling Time	500		nS	Typ	To 0.05% of FSR (All digital inputs low to high and high to low)	6
Feedthrough Error	10		mV pp	Max	VREF=20Vpp, 100 KHz All digital inputs low	5
REFERENCE INPUT Input Resistance (Note 3)	5K		Ω	Min	All digital inputs high. I_{OUT1} at ground.	
	10K			Typ		
	20K			Max		
ANALOG OUTPUT Voltage Compliance (both outputs)	See absolute max. ratings					
Output Capacitance	I_{OUT1} 120 I_{OUT2} 37		pF pF	Typ Typ	All digital inputs high	4
	I_{OUT1} 37 I_{OUT2} 120		pF pF	Typ Typ	All digital inputs low	4
Output Noise (both outputs)	Equivalent to 10KΩ Johnson noise			Typ		3
DIGITAL INPUTS Low State Threshold	0.8		V	Max	Over the specified temp range	
High State Threshold	2.4		V	Min		
Input Current (low to high state)	1		μA	Typ		
Input Coding	Binary/Offset Binary				See Tables 1 & 2 on pages 4 and 5	
POWER REQUIREMENTS Power Supply Voltage Range	+5 to +15		V			
IDD	5		nA	Typ	All digital inputs at GND	
	2		mA	Max	All digital inputs high or low	
Total Power Dissipation (Including the ladder)	20		mW	Typ		

NOTES: **1.** Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Ladder and feedback resistor Tempco is approximately −150ppm/° C.

Specifications subject to change without notice.

TEST CIRCUITS

NOTE: The following test circuits apply for the DAC-7520. Similar circuits can be used for the DAC-7521.

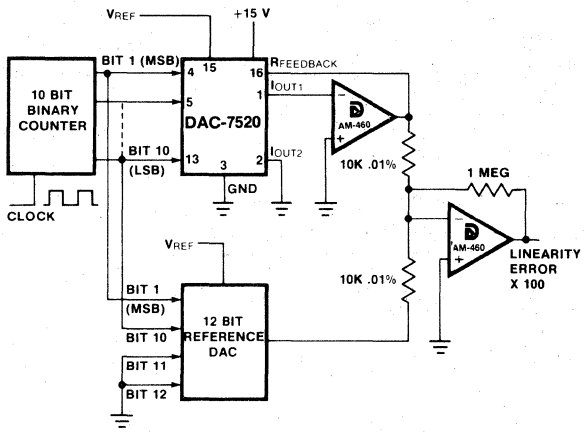


Figure 1. Nonlinearity

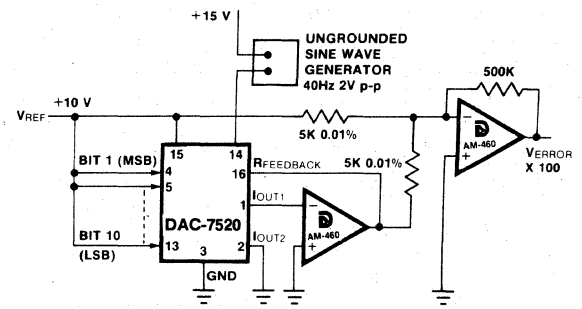


Figure 2. Power Supply Rejection

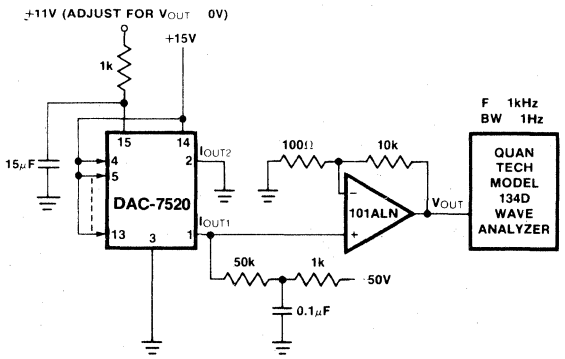


Figure 3. Noise

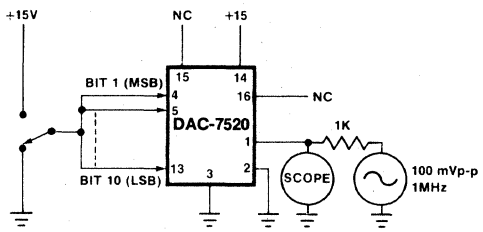


Figure 4. Output Capacitance

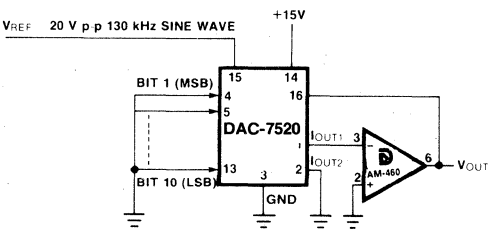


Figure 5. Feedthrough Error

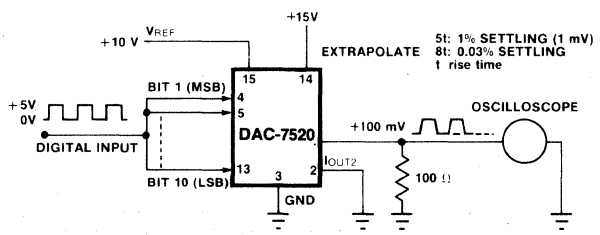


Figure 6. Output Current Settling Time

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

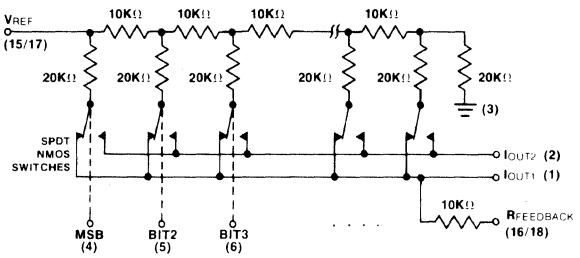
OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

DAC-7520, DAC-7521

GENERAL CIRCUIT INFORMATION

The DAC-7520 and DAC-7521 are monolithic, multiplying D/A converters. Highly stable thin film R-2R resistor ladder network and NMOS DPDT switches form the basis of the converter circuit. CMOS level shifters also enable low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 7. The NMOS DPDT switches steer the ladder leg currents between IOUT1 and IOUT2 busses which must be held at ground potential or virtual ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.



(Switches shown for Digital Inputs "High")

Figure 7. 7520 (7521) Functional Diagram

Converter errors are further eliminated by using separate metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 8). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder DPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors, resulting in accurate leg currents.

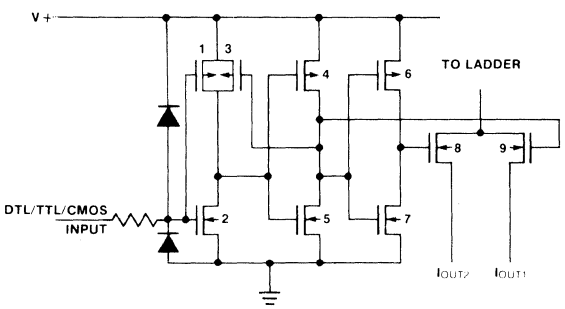


Figure 8. CMOS Switch

APPLICATIONS

UNIPOLAR BINARY OPERATION

The circuit configuration for operating the 7520 and 7521 in unipolar mode is shown in Figure 9. With positive and negative VREF values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1.

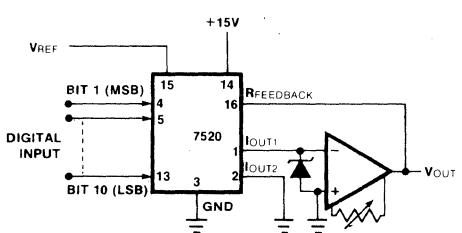


Figure 9. Unipolar Binary Operation (2-Quadrant Multiplication)

Zero Offset Adjustment

1. Connect all 7520 or 7521 digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0 V ± 1 mV at VOUT.

Gain Adjustment

1. Connect all 7520 or 7521 digital inputs to VDD.
2. Monitor VOUT for a $-VREF(1-2^{-n})$ reading. (n=10 for 7520 and n=12 for 7521.)
3. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

TABLE 1
CODE TABLE — UNIPOLAR BINARY OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}(1-2^{-n})$
1000000001	$-V_{REF}(1/2+2^{-n})$
1000000000	$-V_{REF} / 2$
0111111111	$-V_{REF}(1/2-2^{-n})$
0000000001	$-V_{REF}(2^{-n})$
0000000000	0

NOTE: 1. LSB = 2^{-n} VREF 2. n=10 (12) for 7520 (7521)

(APPLICATIONS, Cont'd.)

BIPOLAR (OFFSET BINARY) OPERATION

The circuit configuration for operating the DAC-7520 or DAC-7521 in the bipolar mode is given in Figure 10. Using offset binary digital input codes and positive and negative reference voltage values 4-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

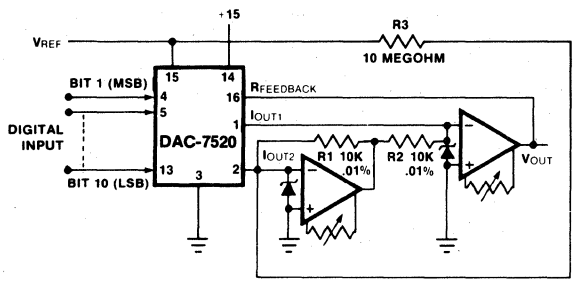


Figure 10. Bipolar Operation (4-Quadant Multiplication)

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to IOUT1 bus. A "Logic 0" input forces the bit current to IOUT2 bus. For any code the IOUT1 and IOUT2 bus currents are complements of one another. The current amplifier at IOUT2 changes the polarity of IOUT2 current and the transconductance amplifier at IOUT1 output sums the two currents. This configuration doubles the output range but halves the resolution of the DAC. The difference current resulting at zero offset binary code, (MSB="Logic 1", All other bits="Logic 0), is corrected by using an external resistor, (10 Megohm), from VREF to IOUT2.

Offset Adjustment

1. Adjust VREF to approximately +10 V.
2. Connect all digital inputs to "Logic 1"
3. Adjust IOUT2 amplifier offset zero adjust trimpot for 0V±1 mV at IOUT2 amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust IOUT1 amplifier offset zero adjust trimpot for 0V±1 mV at VOUT.

Gain Adjustment

1. Connect all DAC-7520 or DAC-7521 digital inputs to VDD.
2. Monitor VOUT for a $-VREF\ (1\text{-}2^{-(n-1)})$ volts reading. (n=10 for DAC-7520 and n=12 for DAC-7521).
3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

TABLE 2
CODE TABLE — BIPOLAR (OFFSET BINARY) OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}\ (1 - 2^{-(n-1)})$
1000000001	$-V_{REF}\ (2^{-(n-1)})$
1000000000	0
0111111111	$V_{REF}\ (2^{-(n-1)})$
0000000001	$V_{REF}\ (1 - 2^{-(n-1)})$
0000000000	V_{REF}

NOTE: 1. LSB = $2^{-(n-1)}\ V_{REF}$ 2. n = 10(12) for 7520 (7521)

POWER PAC DESIGN USING DAC-7520

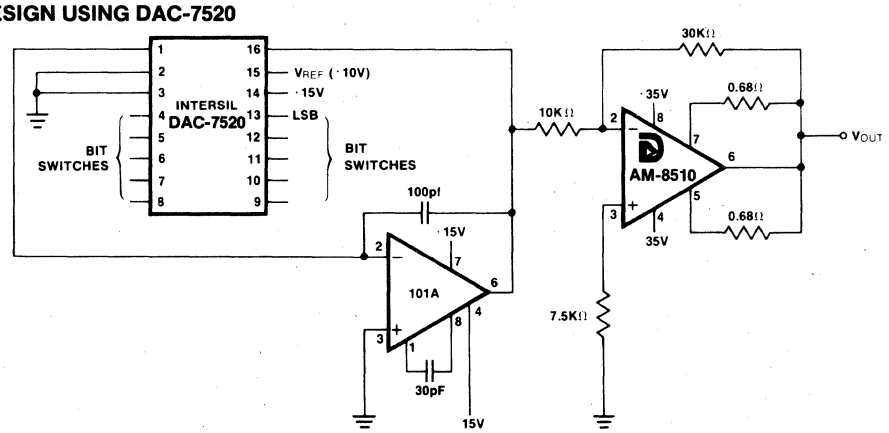


Figure 11. The Basic Power DAC

A typical power DAC designed for 8 bit accuracy and 10 bit resolution is shown in Figure 11. Datel's AM-8510 power amplifier (1 Amp continuous output with up to +25 V) is driven by the 7520.

A summing amplifier between the 7520 and the 8510 is used to separate the gain block containing the 7520 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise 7520 can be directly connected to the 8510, by using a 25 volts reference for the DAC.

An important note on the 7520/101A interface concerns the connection of pin 1 of the DAC and pin 2 of the 101A. Since this point is the summing junction of an amplifier with an AC gain of 50,000 or better, stray capacitance should be minimized; otherwise instabilities and poor noise performance will result. Notice that the output of the 101A is fed into an inverting amplifier with a gain of −3, which can be easily changed to a non-inverting configuration.

DAC-7520, DAC-7521

(APPLICATIONS, Cont'd.)

ANALOG/DIGITAL DIVISION

With the 7520 connected in its normal multiplying configuration as shown in figure 15, the transfer function is

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}\right)$$

where the coefficients A_x assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 12, the transfer function becomes

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero isn't defined. With the LSB (Bit-10) ON, the gain is 1023. With all bits ON, the gain is 1 (±1 LSB).

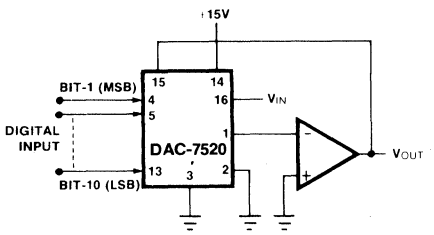
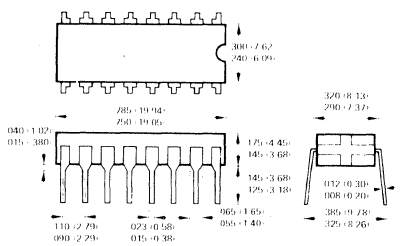


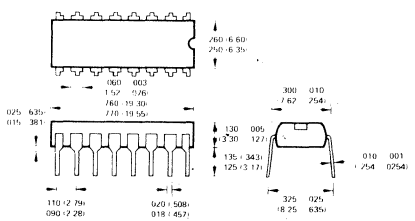
Figure 12. Analog/Digital Divider

PACKAGE DIMENSIONS

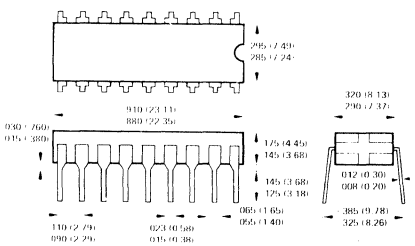
DAC-7520R, M
16 PIN CERDIP



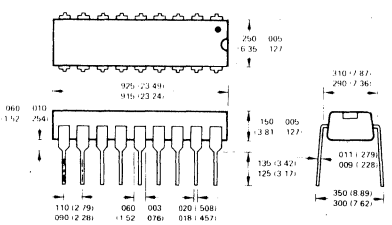
DAC-7520C
16 PIN PLASTIC DIP



DAC-7521R, M
18 PIN CERDIP



DAC-7521C
18 PIN PLASTIC DIP



1. Lead no. 1 identified by dot or notch.
2. Dimensions in inches (millimeters).

DATEL INTERSIL
11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL (617)339-9341 / TWX 710-346-1953 / TLX 951340
Santa Ana, (714)835-2751, (L.A.) (213)933-7256 • Sunnyvale, CA (408)733-2424 • Gaithersburg, MD (301)840-9490
• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

8 Bit Monolithic Multiplying D/A Converters Model DAC-7523

FEATURES

- **8 bit linearity**
- **Low gain and linearity Tempcos**
- **Full temperature range operation**
- **Full input static protection**
- **DTL/TTL/CMOS compatible**
- **+5 to +15 volts supply range**
- **Fast settling time: 100 nS**
- **Four quadrant multiplication**

GENERAL DESCRIPTION

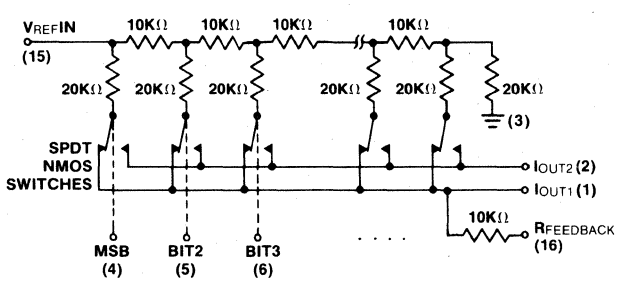
The DAC-7523 is a monolithic, low cost, high performance, 10 bit accurate, multiplying digital-to-analog converter (DAC), in a 16-pin DIP.

Datel-Intersil's thin-film resistors on CMOS circuitry provide 8-bit resolution and linearity, with DTL/TTL/CMOS compatible operation.

The DAC-7523's accurate four quadrant multiplication, full military temperature range operation, full input protection from damage due to static discharge by clamps to V+ and GND and very low power dissipation make it a very versatile converter.

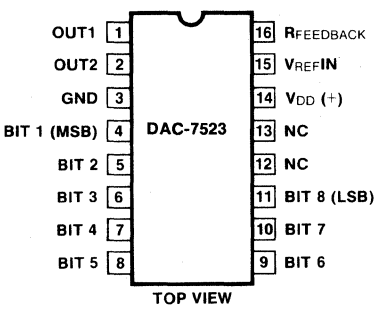
Low noise audio gain control, motor speed control, digitally controlled gain and attenuators are a few of the wide number of applications of the 7523.

FUNCTIONAL DIAGRAM



(Switches shown for Digital Inputs "High")

PIN CONFIGURATION



TOP VIEW

ORDERING INFORMATION

MODEL	OPER. TEMP. RANGE	PACKAGE
DAC-7523C	0 to +70°C	EPOXY
DAC-7523R	−25 to +85°C	CERDIP
DAC-7523M	−55 to +125°C	CERDIP

DAC-7523

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

VDD (to GND) ..... +17V
VREF (to GND) ..... ±25V
Digital Input Voltage Range ..... −0.3 to VDD
Output Voltage Compliance ..... −0.3 to VDD
Power Dissipation (package)
Plastic
up to +70°C 670mW
derates above +70°C by ..... 8.3mW/°C
Ceramic
up to 75°C 450mW
derates above 75°C by ..... 6mW/°C
Operating Temperatures
C Versions ..... 0°C to +70°C
R Versions ..... −25°C to +85°C
M Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

CAUTION: 1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2. Do not apply voltages higher than VDD and lower than GND to any terminal except VREF.

SPECIFICATIONS (VDD = +15V, VREF = +10V unless otherwise specified)

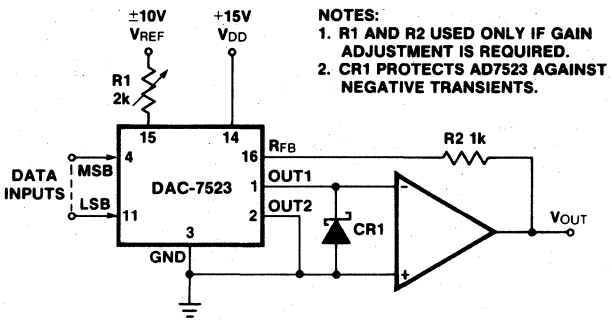
PARAMETER	TA +25°C	TA MIN-MAX	UNITS	LIMIT	TEST CONDITIONS
DC ACCURACY (Note 1)					
Resolution	8	8	Bits	Min	
Nonlinearity (Note 2) (±1/2 LSB)	±0.2	±0.2	% of FSR	Max	−10V ≤ VREF ≤ +10V $V_{OUT1} = V_{OUT2} = 0V$
Monotonicity	Guaranteed				
Gain Error (Note 2)	±1.5	±1.8	% of FSR	Max	Digital inputs high.
Nonlinearity Tempco (Note 2 and 3)	2		PPM of FSR/°C	Max	−10V VREF +10V
Gain Error Tempco (Note 2 and 3)	10		PPM of FSR/°C	Max	
Output Leakage Current (either output)	±50	±200	nA	Max	$V_{OUT1} = V_{OUT2} = 0$
AC ACCURACY (Note 3)					
Power Supply Rejection (Note 2)	0.02	0.03	% of FSR/%	Max	V_{DD} = 14.0 to 15.0V
Output Current Settling Time	150	200	nS	Max	To 0.2% of FSR, R_L = 100Ω
Feedthrough Error	±1/2	±1	LSB	Max	VREF = 20V pp, 200KHz sine wave. All digital inputs low.
REFERENCE INPUT	5K		Ω	Min	All digital inputs high. I_{OUT1} at ground.
Input Resistance (Pin 15)	20K		Ω	Max	
Temperature Coefficient (Note 3)	−500		ppm/°C	Max	
ANALOG OUTPUT (Note 3)					Both outputs.
Voltage Compliance (Note 4)	−100mV to V_{DD}				See maximum ratings.
Output Capacitance C_{OUT1}	100		pF	Max	All digital inputs high (VINH)
Output Capacitance C_{OUT2}	30		pF	Max	
Output Capacitance C_{OUT1}	30		pF	Max	All digital inputs low (VINL)
Output Capacitance C_{OUT2}	100		pF	Max	
DIGITAL INPUTS					
Low State Threshold (VINL)	0.8		V	Max	Guarantees DTL/TTL and CMOS (0.5 max, 14.5 min) levels
High State Threshold (VINH)	2.4		V	Min	
Input Current (per input)	±1		μA	Max	V_{IN} = 0V or +15V
Input Coding	Binary/Offset Binary				See Tables 1 & 2
Input Capacitance (Note 3)	4		pF	Max	
POWER REQUIREMENTS					Accuracy is tested and guaranteed at
Power Supply Voltage Range	+5 to +16		V		V_{DD} = +15V, only.
IDD	100		μA	Max	All digital inputs low or high.

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

Specifications subject to change without notice.

DAC-7523

APPLICATIONS
UNIPOLAR OPERATION



NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. CR1 PROTECTS AD7523 AGAINST NEGATIVE TRANSIENTS.

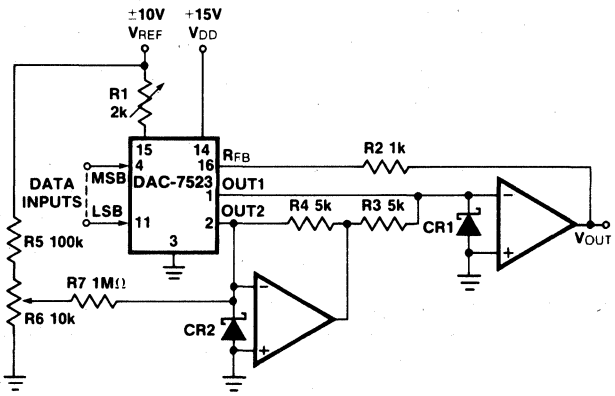
Figure 1. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	ANALOG OUTPUT	
11111111	$-V_{REF}$	$\left(\frac{255}{256}\right)$
10000001	$-V_{REF}$	$\left(\frac{129}{256}\right)$
10000000	$-V_{REF}$	$\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
01111111	$-V_{REF}$	$\left(\frac{127}{256}\right)$
00000001	$-V_{REF}$	$\left(\frac{1}{256}\right)$
00000000	$-V_{REF}$	$\left(\frac{0}{256}\right) = 0$

Note: 1 LSB = (2^{-8}) $(V_{REF}) = \left(\frac{1}{256}\right)$ (V_{REF})

Table 1. Unipolar Binary Code Table

BIPOLAR OPERATION



NOTES:
1. R3/R4 MATCH 0.1% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. R5-R7 USED TO ADJUST V_{OUT} = 0V AT INPUT CODE 10000000.
4. CR1 & CR2 PROTECT AD7523 AGAINST NEGATIVE TRANSIENTS.

Figure 2. Bipolar (4-Quadrant) Operation

DIGITAL INPUT MSB LSB	ANALOG OUTPUT	
11111111	$-V_{REF}$	$\left(\frac{127}{128}\right)$
10000001	$-V_{REF}$	$\left(\frac{1}{128}\right)$
10000000	0	
01111111	$+V_{REF}$	$\left(\frac{1}{128}\right)$
00000001	$+V_{REF}$	$\left(\frac{127}{128}\right)$
00000000	$+V_{REF}$	$\left(\frac{128}{128}\right)$

Note: 1LSB = (2^{-7}) $(V_{REF}) = \left(\frac{1}{128}\right)$ (V_{REF})

Table 2. Bipolar (Offset Binary) Code Table

POWER DAC DESIGN USING 7523

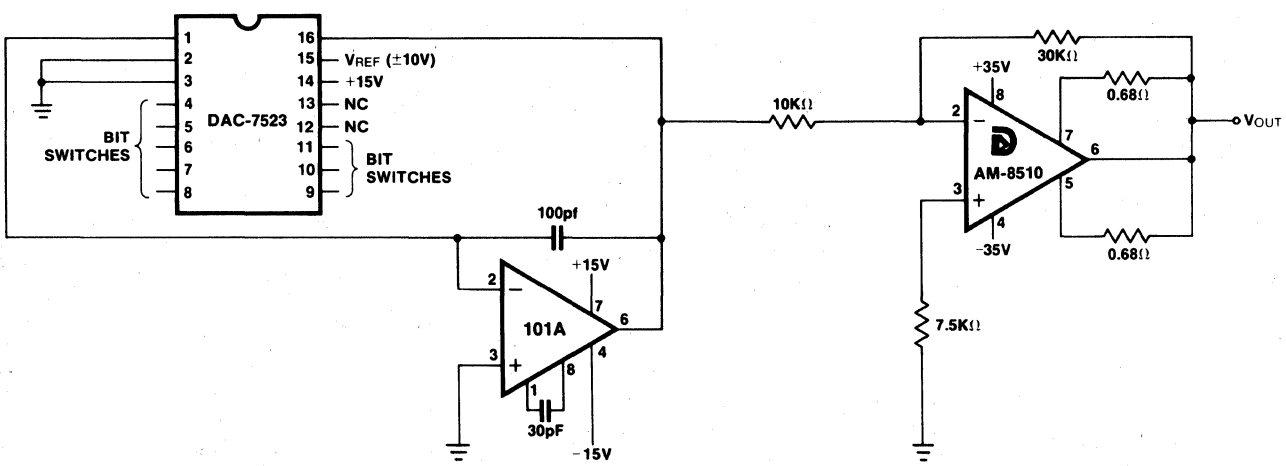


Figure 3. The Basic Power DAC

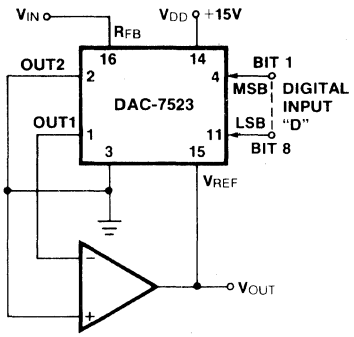
A typical power DAC designed for 10 bit accuracy and 8 bit resolution is shown in Figure 3. Datel's AM-8510 power amplifier (1 Amp continuous output with up to +25V) is driven by the 7523.

A summing amplifier between the 7523 and the 8510 is used to separate the gain block containing the 7520 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise 7523 can be directly connected to the 8510, by using a 25 volts reference for the DAC.

DAC-7523

APPLICATIONS (continued)

DIVIDER (DIGITALLY CONTROLLED GAIN)



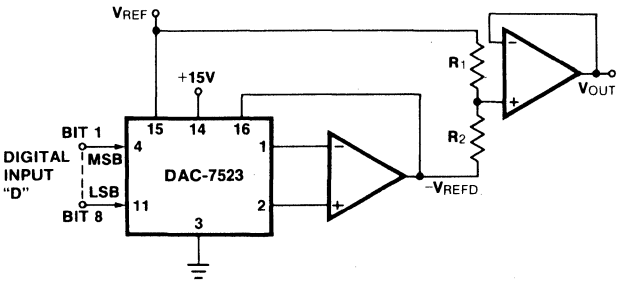
$V_{OUT} = -V_{IN}/D$

WHERE:

$$D = \frac{BIT1}{2^1} + \frac{BIT2}{2^2} + \cdots \frac{BIT8}{2^8}$$

$$\left(0 \leq D \leq \frac{255}{256}\right)$$

MODIFIED SCALE FACTOR AND OFFSET



$$V_{OUT} = V_{REF}\left[\left(\frac{R_2}{R_1 + R_2}\right) - \left(\frac{R_1 D}{R_1 + R_2}\right)\right] \quad \text{WHERE:} \quad D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \cdots \frac{BIT\ 8}{2^8}$$

$$\left(0 \leq D \leq \frac{255}{256}\right)$$

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

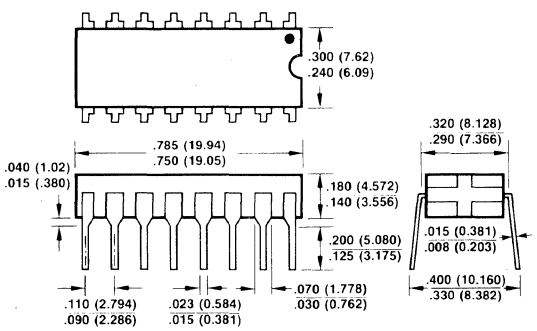
FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

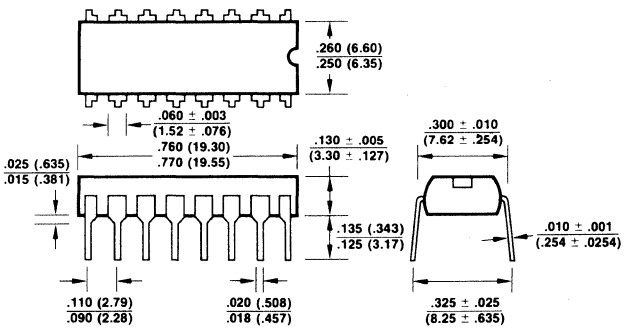
OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

PACKAGE DIMENSIONS

DAC-7523R, M
16 PIN CERDIP



DAC-7523C
16 PIN PLASTIC DIP



1. Lead no. 1 identified by dot or notch.
2. Dimensions in inches (millimeters).

Low Cost, 10 Bit Monolithic Multiplying D/A Converters Model DAC-7533

FEATURES

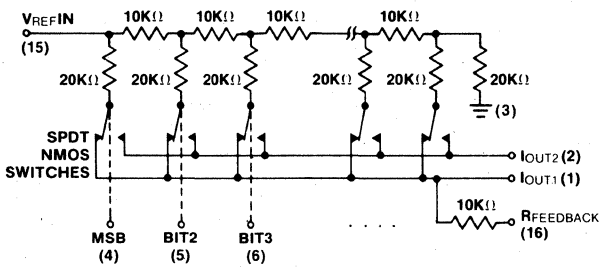
- **Lowest cost 10-bit DAC**
- **True 10 bit linearity**
- **Low gain and linearity Tempcos**
- **Full temperature range operation**
- **Full input static protection**
- **DTL/TTL/CMOS direct interface**
- **+5 to +15 volts supply range**
- **Low power dissipation**
- **Fast settling time**
- **Four quadrant multiplication**
- **Direct AD7520 equivalent**

GENERAL DESCRIPTION

The DAC-7533 is a low cost, monolithic 10-bit, four-quadrant multiplying digital-to-analog converter (DAC). Datel's thin-film resistors on CMOS circuitry provide TRUE 10 bit accuracy, full temperature range operation, +5V to +15V power range, full input protection from damage due to static discharge by clamps to V+ and ground and very low power dissipation. Pin and function equivalent to Industry Standard AD7520, the DAC-7533 is recommended as a lower cost alternative for old or new 10-bit DAC designs.

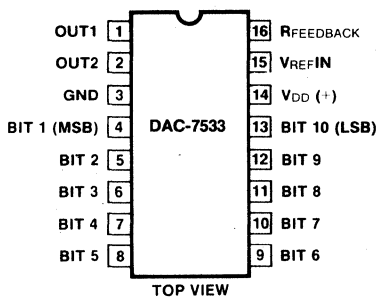
Application of DAC-7533 includes programmable gain amplifiers, digitally controlled attenuators, function generators and control systems.

FUNCTIONAL DIAGRAM



(Switches shown for Digital Inputs "High")

PIN CONFIGURATION



TOP VIEW

ORDERING INFORMATION

Model	Oper. Temp. Range	Package
DAC-7533C	0 to +70° C	Epoxy
DAC-7533R	-25 to +85° C	Cerdip
DAC-7533M	-55 to +125° C	Cerdip

DAC-7533

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

VDD (to GND) ..... −0.3V, +17V
VREF (to GND) ..... ±25V
Digital Input Voltage Range ..... −0.3V to V_{DD}
Output Voltage Compliance ..... −0.3 to VDD
Power Dissipation (package)
Ceramic
up to +75°C 450mW
derates above +75°C by ..... 6mW/°C
Plastic
up to 70°C 670mW
derates above 70°C by ..... 8.3mW/°C
Operating Temperatures
C Versions ..... 0°C to +70°C
R Versions ..... −25°C to +85°C
M Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

CAUTION: 1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2. Do not apply voltages lower than ground or higher than V_{DD} to any pin except V_{REF} and R_{FB}.

SPECIFICATIONS (VDD = +15V, VREF = +10V, V_{OUT1} = V_{OUT2} = 0 unless otherwise specified)

PARAMETER		TA +25°C	TA MIN-MAX	UNITS	LIMIT	TEST CONDITIONS
DC ACCURACY (Note 1)						
Resolution		10	10	Bits	Min	
Nonlinearity (Note 2)						−10V ≤ VREF ≤ +10V
		±0.05	±0.05	% of FSR	Max	V_{OUT1} = V_{OUT2} = 0V
Gain Error (Note 2 and 5)		±1.4	±1.5	% of FS	Max	Digital Inputs = VINH
Output Leakage Current (either output)		±50	±200	nA	Max	V_{REF} = ±10V
AC ACCURACY						
Power Supply Rejection (Note 2 and 3)		0.005	0.008	% of FSR/%	Max	V_{DD} = 14.0 to 17.0V
Output Current Settling Time		600 (Note 6)	800 (Note 3)	nS	Max	To 0.05% of FSR, R_L = 100Ω
Feedthrough Error (Note 3)		±0.05	±0.1	% FSR	Max	VREF = ±10V, 100KHz sine wave. Digital inputs low.
REFERENCE INPUT		5K			Min	
Input Resistance (Pin 15)		20K		Ω	Max	All digital inputs high.
Temperature Coefficient		−300		ppm/°C	Typ	
ANALOG OUTPUT						Both outputs.
Voltage Compliance (Note 4)		−100mV to V_{DD}				See maximum ratings.
Output Capacitance (Note 3)	C_{OUT1}	100		pF	Max	All digital inputs high (VINH)
	C_{OUT2}	35		pF	Max	
	C_{OUT1}	35		pF	Max	All digital inputs low (VINL)
	C_{OUT2}	100		pF	Max	
DIGITAL INPUTS						
Low State Threshold (VINL)		0.8		V	Max	
High State Threshold (VINH)		2.4		V	Min	
Input Current (I_{IN})		±1		μA	Max	V_{IN} = 0V and V_{DD}
Input Coding		Binary/Offset Binary				See Tables 1 & 2
Input Capacitance (Note 3)		5		pF	Max	
POWER REQUIREMENTS						
V_{DD}		+15 ±10%		+15 ±10%		Rated Accuracy
Power Supply Voltage Range		+5 to +16		V		
IDD		2		mA	Max	Digital Inputs = V_{INL} to V_{INH}
I_{DD}		100μA		150μA	Max	Digital Inputs = 0V or V_{DD}

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.
5. Full scale (FS) = − (V_{REF}) • (1023/1024)
6. Sample tested to ensure specification compliance.

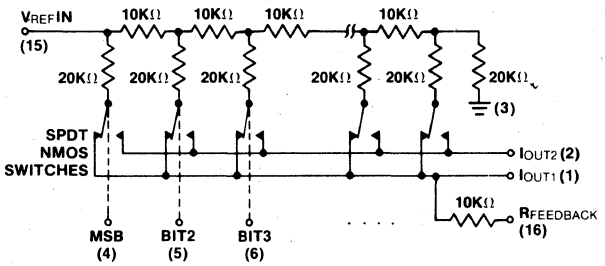
Specifications subject to change without notice.

DAC-7533

GENERAL CIRCUIT INFORMATION

The DAC-7533 is a 10 bit, monolithic, multiplying D/A converter. Highly stable thin film R-2R resistor ladder network and NMOS DPDT switches form the basis of the converter circuit. CMOS level shifters provide low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 1. The NMOS DPDT switches steer the ladder leg currents between IOUT1 and IOUT2 busses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.



(Switches shown for Digital Inputs "High")

Figure 1

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 2). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder DPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors resulting in accurate leg currents.

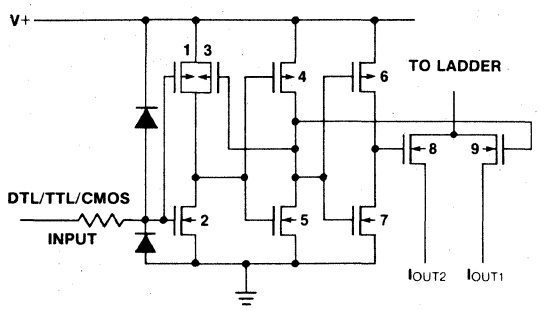
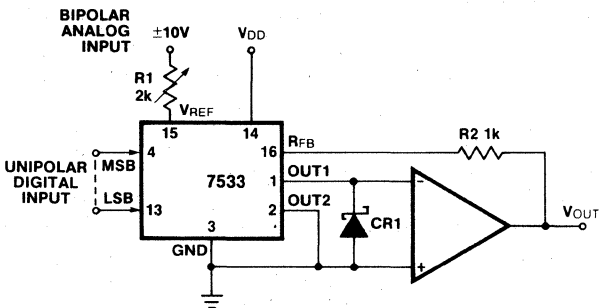


Figure 2

APPLICATIONS

UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)



NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. SCHOTTKY DIODE CR1 (HP5082-2811 OR EQUIV) PROTECTS OUT1 TERMINAL AGAINST NEGATIVE TRANSIENTS.

Figure 3. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (VOUT as shown in Figure 3)	
1111111111	$-V_{REF}\left(\frac{1023}{1024}\right)$	
1000000001	$-V_{REF}\left(\frac{513}{1024}\right)$	
1000000000	$-V_{REF}\left(\frac{512}{1024}\right)$	$\frac{V_{REF}}{2}$
0111111111	$-V_{REF}\left(\frac{511}{1024}\right)$	
0000000001	$-V_{REF}\left(\frac{1}{1024}\right)$	
0000000000	$-V_{REF}\left(\frac{0}{1024}\right) = 0$	

NOTES:

1. Nominal Full Scale for the circuit of Figure 3 is given by

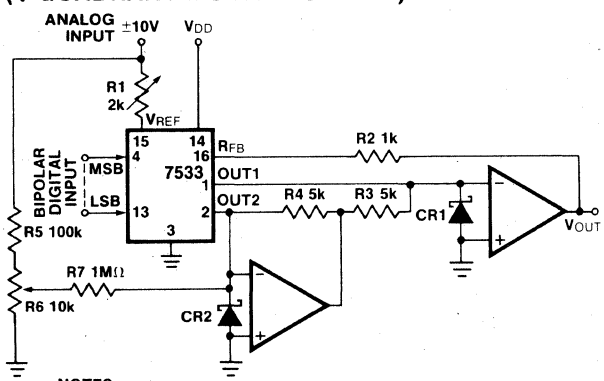
$$FS = -V_{REF}\left(\frac{1023}{1024}\right)$$

2. Nominal LSB magnitude for the circuit of Figure 3 is given by

$$LSB = V_{REF}\left(\frac{1}{1024}\right)$$

Table 1. Unipolar Binary Code

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)



NOTES:
1. R3/R4 MATCH 0.05% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. SCHOTTKY DIODES CR1 AND CR2 (HP5082-2811 OR EQUIV) PROTECT OUT1 AND OUT2 TERMINALS FROM NEGATIVE TRANSIENTS

Figure 4. Bipolar Operation (4-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (VOUT as shown in Figure 4)	
1111111111	$-V_{REF}\left(\frac{511}{512}\right)$	
1000000001	$-V_{REF}\left(\frac{1}{512}\right)$	
1000000000	0	
0111111111	$+V_{REF}\left(\frac{1}{512}\right)$	
0000000001	$+V_{REF}\left(\frac{511}{512}\right)$	
0000000000	$+V_{REF}\left(\frac{512}{512}\right)$	

NOTES:

1. Nominal Full Scale Range for the circuit of Figure 4 is given by

$$FSR = V_{REF}\left(\frac{1023}{512}\right)$$

2. Nominal LSB magnitude for the circuit of Figure 4 is given by

$$LSB = V_{REF}\left(\frac{1}{512}\right)$$

Table 2. Bipolar (Offset Binary) Code Table

DAC-7533

POWER DAC DESIGN USING DAC-7533

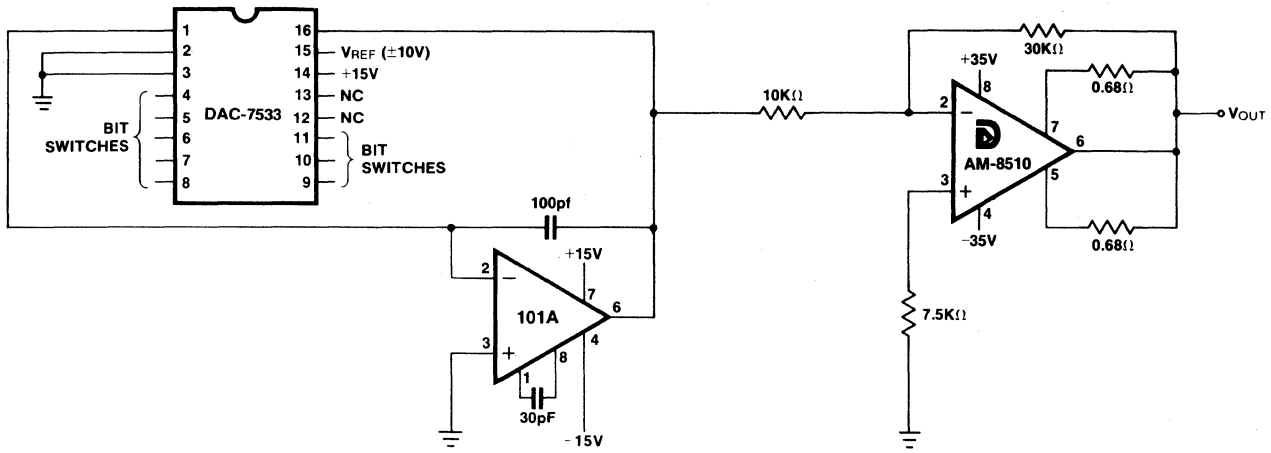
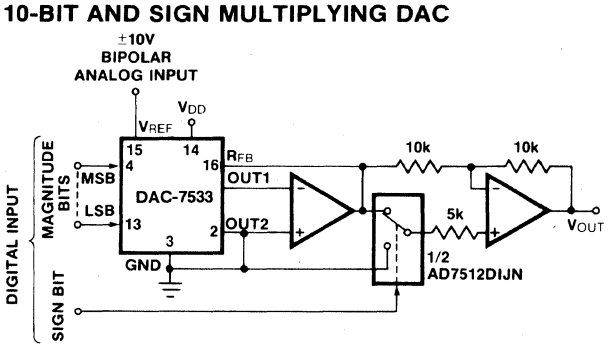


Figure 5. The Basic Power DAC

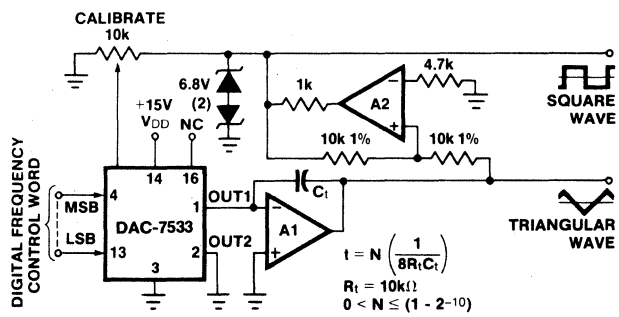
A typical power DAC designed for 8 bit accuracy and 10 bit resolution is shown in Figure 5. Datel Intersil's AM-8510 power amplifier (1 Amp continuous output with up to +25V) is driven by the DAC-7533.

A summing amplifer between the 7533 and the 8510 is used to separate the gain block containing the 7533 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise 7533 can be directly connected to the 8510, by using a 25 volts reference for the DAC. Notice that the output of the 101A is fed into an inverting amplifier with a gain of -3, which can be easily changed to a non-inverting configuration.

10-BIT AND SIGN MULTIPLYING DAC

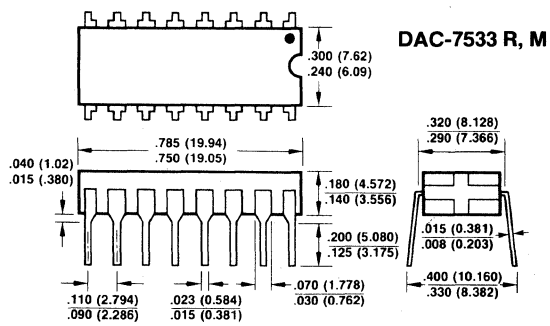


PROGRAMMABLE FUNCTION GENERATOR

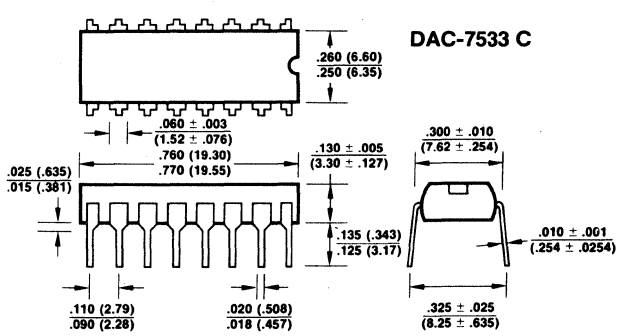


PACKAGE DIMENSIONS

16 PIN CERDIP



16 PIN PLASTIC DIP



1. Lead no. 1 identified by dot or notch.
2. Dimensions in inches (millimeters).

12 Bit Monolithic Multiplying D/A Converters Model DAC-7541

FEATURES

- 12 bit linearity (0.01%)
- Pretrimmed gain
- Low gain and linearity Tempcos
- Full temperature range operation
- Full input static protection
- DTL/TTL/CMOS compatible
- +5 to +15 volts supply range
- Low power dissipation (20mW)
- Current settling time: 1μs to 0.01% of FSR
- Four quadrant multiplication

GENERAL DESCRIPTION

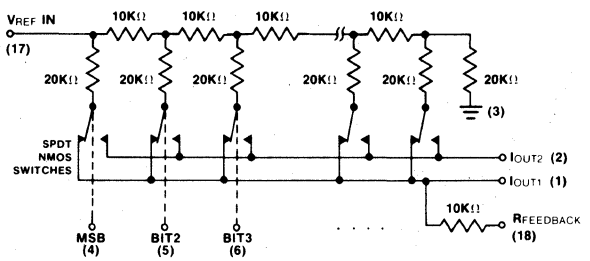
Datel-Intersil's DAC-7541 is a monolithic, low cost, high performance, 12-bit accurate, multiplying digital-to-analog converter.

Datel-Intersil's wafer level laser-trimmed thin-film resistors on CMOS circuitry provide true 12-bit linearity with DTL/TTL/CMOS compatible operation.

Special tabbed-resistor geometries (improving time stability), full input protection from damage due to static discharge by diode clamps to V+ and ground, large IOUT1 and IOUT2 bus lines (improving superposition errors) are some of the features offered by Datel-Intersil's DAC-7541.

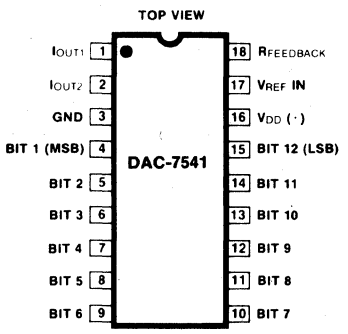
Pin compatible with DAC-7521, this new DAC provides accurate four quadrant multiplication over the full military temperature range.

FUNCTIONAL DIAGRAM



(Switches shown for Digital Inputs "High')

PIN CONFIGURATION



ORDERING INFORMATION

MODEL	OPER. TEMP. RANGE	PACKAGE
DAC-7541C	0 to +70° C	CERDIP
DAC-7541R	−25 to +85° C	CERDIP
DAC-7541M	−55 to +12° C	CERDIP

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

DAC-7541

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

VDD (to GND) ..... +17V
VREF (to GND) ..... ±25V
Digital Input Voltage Range ..... VDD to GND
Output Voltage Compliance ..... −100mV to VDD
Power Dissipation (package)
up to +75°C 450mW
derates above +75°C by ..... 6mW/°C

Operating Temperatures
C Versions ..... 0°C to +70°C
R Versions ..... −25°C to +85°C
M Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C

CAUTION 1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.

SPECIFICATIONS (VDD = +15V, VREF = +10V, TA = 25°C unless otherwise specified)

PARAMETER		TA +25°C	TA MIN-MAX	UNITS	LIMIT	TEST CONDITIONS	FIG.
DC ACCURACY (Note 1)							
Resolution		12	12	Bits	Min		
Nonlinearity (Note 2)		±0.010	±0.012	% of FSR	Max	−10V ≤ VREF ≤ +10V $V_{OUT1} = V_{OUT2} = 0V$	1
Gain Error (Note 2)		±0.3	±0.4	% of FSR	Max	−10V ≤ VREF ≤ +10V	
Output Leakage Current (either output)		±50	±200	nA	Max	$V_{OUT1} = V_{OUT2} = 0$	
AC ACCURACY (Note 3)							
Power Supply Rejection (Note 2)		±0.01	±0.02	% of FSR %	Max	V_{DD} = 14.5 to 15.5V	2
Output Current Settling Time		1		µS	Max	To 0.01% of FSR	6
Feedthrough Error		1		mV pp	Max	VREF = 20V pp, 10 KHz. All digital inputs low.	5
REFERENCE INPUT		5K		Ω	Min	All digital inputs high. I_{OUT1} at ground.	
Input Resistance		10K			Typ		
		20K			Max		
ANALOG OUTPUT						Both outputs.	
Voltage Compliance (Note 4)		−100mV to V_{DD}				See maximum ratings.	
Output Capacitance (Note 3)	C_{OUT1}	200		pF	Max	All digital inputs high (VINH)	4
	C_{OUT2}	60		pF	Max		
	C_{OUT1}	60		pF	Max	All digital inputs low (VINL)	4
	C_{OUT2}	200		pF	Max		
Output Noise (both outputs)		Equivalent to 10KΩ Johnson noise			Typ		3
DIGITAL INPUTS							
Low State Threshold (VINL)		0.8		V	Max		
High State Threshold (VINH)		2.4		V	Min		
Input Current		±1		µA	Max	V_{IN} = 0 or V_{DD}	
Input Coding		Binary/Offset Binary				See Tables 1 & 2 on pages 4 and 5.	
Input Capacitance (Note 3)		8		pF	Max		
POWER REQUIREMENTS						Accuracy is not guaranteed	
Power Supply Voltage Range		+5 to +16		V		over this range	
IDD		2		mA	Max	All digital inputs high or low	
Total Power Dissipation (including the ladder)		20		mW	Typ		

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

Specifications subject to change without notice.

TEST CIRCUITS

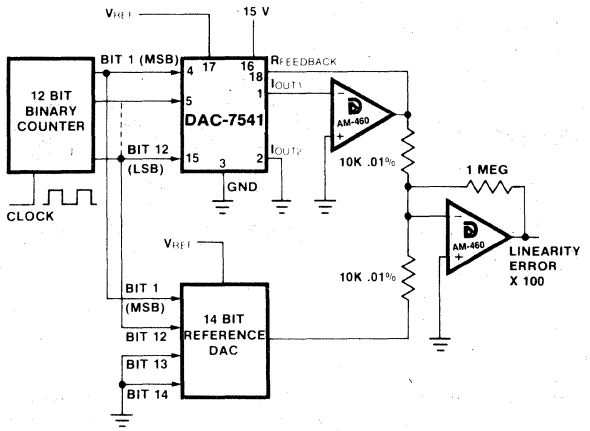


Figure 1. Nonlinearity

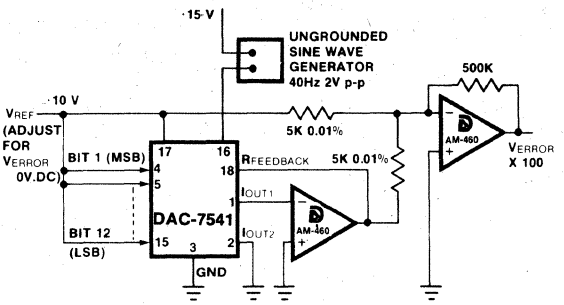


Figure 2. Power Supply Rejection

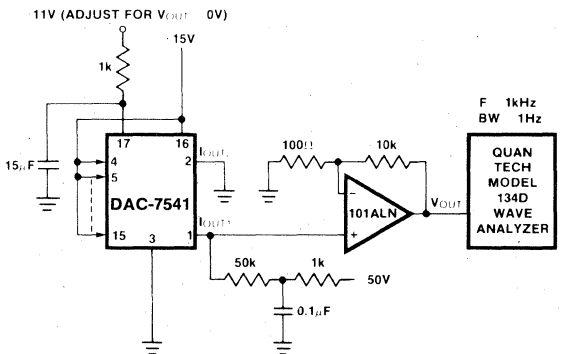


Figure 3. Noise

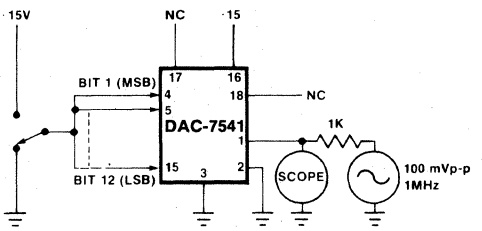


Figure 4. Output Capacitance

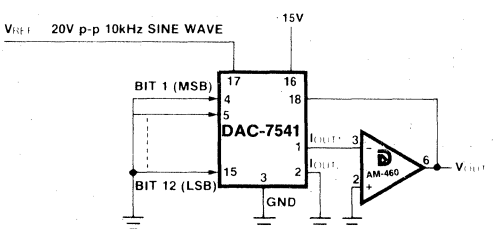


Figure 5. Feedthrough Error

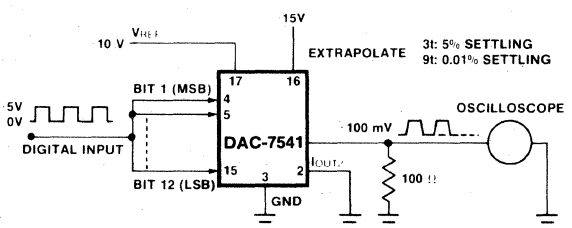


Figure 6. Output Current Settling Time

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

DAC-7541

GENERAL CIRCUIT INFORMATION

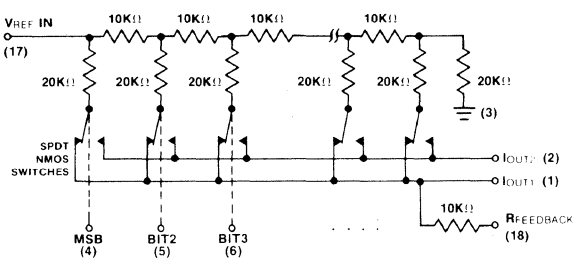
The DAC-7541 is a 12 bit, monolithic, multiplying D/A converter. Highly stable thin film R-2R resistor ladder network and NMOS DPDT switches form the basis of the converter circuit. CMOS level shifters provide low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 7. The NMOS DPDT switches steer the ladder leg currents between IOUT1 and IOUT2 busses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.

Converter errors are further eliminated by using wider metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

Each circuit is laser-trimmed, at the wafer level, to better than 12 bits linearity. For the first four bits of the ladder, special trim-tabbed geometries are used to keep the body of the resistors, carrying the majority of the output current, undisturbed. The resultant time stability of the trimmed circuits is comparable to that of untrimmed units.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first (Figure 8). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder DPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors, resulting in accurate leg currents.



(Switches shown for Digital Inputs "High")

Figure 7. DAC-7541 Functional Diagram

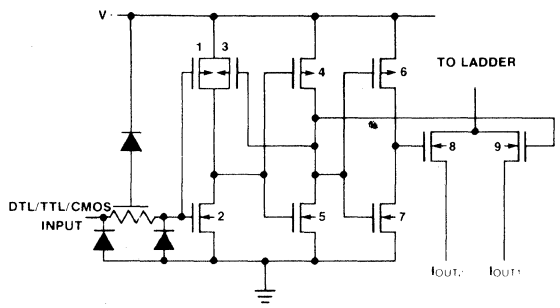


Figure 8. CMOS Switch

APPLICATIONS

General Recommendations

Static performance of the 7541 depends on I_{OUT1} and I_{OUT2} (pin 1 and pin 2) potentials being exactly equal to GND (pin 3).

The output amplifier should be selected to have a low input bias current (typically less than 75nA), and a low drift (depending on the temperature range). The voltage offset of the amplifier should be nulled (typically less than $\pm 200\mu V$).

The bias current compensation resistor in the amplifier's non-inverting input can cause a variable offset. Non-inverting input should be connected to GND with a low resistance wire.

Ground-loops must be avoided by taking all pins going to GND to a common point, using separate connections.

The V_{DD} (pin 18) power supply should have a low noise level and should not have any transients exceeding +17 volts.

Unused digital inputs must be connected to GND or V_{DD} for proper operation.

A high value resistor (~1MΩ) can be used to prevent static charge accumulation, when the inputs are open-circuited for any reason.

When gain adjustment is required, low tempco (approximately 50ppm/°C) resistors or trim-pots should be selected.

APPLICATIONS, Continued

UNIPOLAR BINARY OPERATION

The circuit configuration for operating the 7541 in unipolar mode is shown in Figure 9. With positive and negative VREF values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1. Schottky diode (HP 5082-2811 or equivalent) prevents I_{OUT1} from negative excursions which could damage the device. This precaution is only necessary with certain high speed amplifiers.

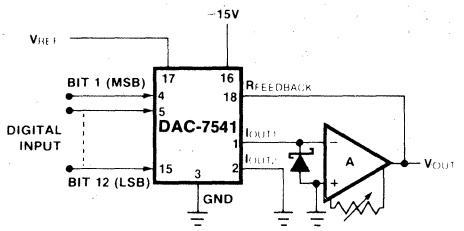


Figure 9. Unipolar Binary Operation (2-Quadrant Multiplication)

Zero Offset Adjustment

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±0.5mV (max) at VOUT.

Gain Adjustment

1. Connect all digital inputs to VDD.
2. Monitor VOUT for a $-V_{REF}(1 - 1/2^{12})$ reading.
3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

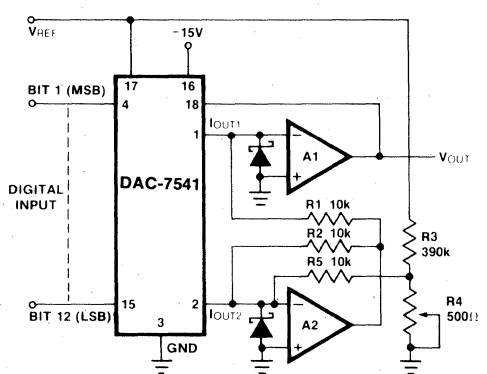
TABLE 1

Code Table — Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}(1 - 1/2^{12})$
100000000001	$-V_{REF}(1/2 + 1/2^{12})$
100000000000	$-V_{REF}/2$
011111111111	$-V_{REF}(1/2 - 1/2^{12})$
000000000001	$-V_{REF}(1/2^{12})$
000000000000	0

BIPOLAR (OFFSET BINARY) OPERATION

The circuit configuration for operating the 7541 in the bipolar mode is given in Figure 10. Using offset binary digital input codes and positive and negative reference voltage values Four-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.



Note: R1 and R2 should be 0.01%, low-TCR resistors.

Figure 10. Bipolar Operation (4-Quadrant Multiplication)

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to IOUT1 bus. A "Logic 0" input forces the bit current to IOUT2 bus. For any code the IOUT1 and IOUT2 bus currents are complements of one another. The current amplifier at IOUT2 changes the polarity of IOUT2 current and the transconductance amplifier at IOUT1 output sums the two currents. This configuration doubles the output range but halves the resolution of the DAC. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistive divider, from VREF to IOUT2.

Offset Adjustment

1. Adjust VREF to approximately +10V.
2. Connect all digital inputs to "Logic 1".
3. Adjust IOUT2 amplifier offset zero adjust trimpot for 0V ± 0.1mV at IOUT2 amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust IOUT1 amplifier offset zero adjust trimpot for 0V ± 0.1mV at IOUT1 amplifier output.
6. Adjust R4 for 0V ± 0.2mV at VOUT.

Gain Adjustment

1. Connect all digital inputs to VDD.
2. Monitor VOUT for a $-V_{REF}(1 - 1/2^{11})$ volts reading.
3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

TABLE 2

Code Table — Bipolar (Offset Binary) Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}(1 - 1/2^{11})$
100000000001	$-V_{REF}(1/2^{11})$
100000000000	0
011111111111	$V_{REF}(1/2^{11})$
000000000001	$V_{REF}(1 - 1/2^{11})$
000000000000	V_{REF}

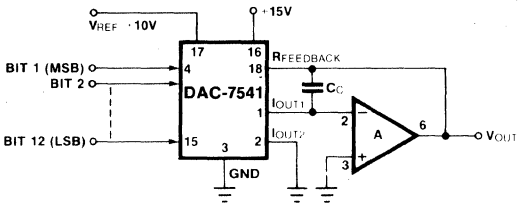


Figure 11. General DAC Circuit with Compensation Capacitor, C_C.

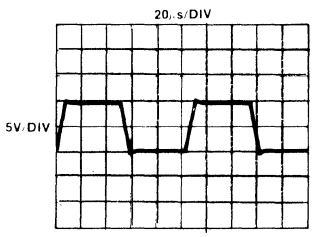


Figure 12. DAC-7541 Response with: A = Intersil 741HS

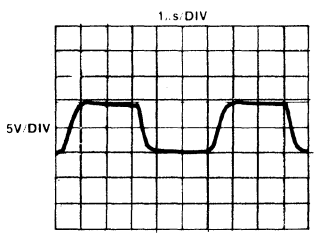


Figure 13. DAC-7541 Response with: A = Intersil 2515
C_C = 15pF

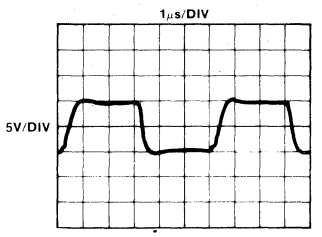


Figure 14. DAC-7541 Response with: A=Datel AM-452

DYNAMIC PERFORMANCE

The dynamic performance of the DAC, also depends on the output amplifier selection. For low speed or static applications, AC specifications of the amplifier are not very critical. For high-speed applications slew-rate, settling-time, open-loop gain and gain/phase-margin specifications of the amplifier should be selected for the desired performance.

The output impedance of the 7541 looking into I_{OUT1} varies between 10kΩ ($R_{Feedback}$ alone) and 5kΩ ($R_{Feedback}$ in parallel with the ladder resistance).

Similarly the output capacitance varies between the minimum and the maximum values depending on the input code. These variations necessitate the use of compensation capacitors, when high speed amplifiers are used.

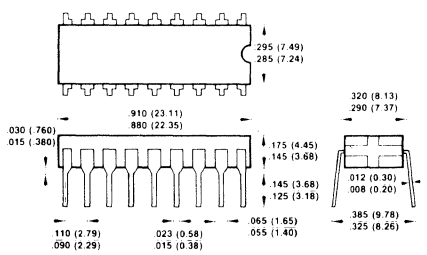
A capacitor in parallel with the feedback resistor provides the necessary phase compensation to critically damp the output.

A small capacitor connected to the compensation pin of the amplifier may be required for unstable situations causing oscillations. Careful PC board layout, minimizing parasitic capacitances, is also vital.

Three typical circuits and the resultant waveforms are shown in Figures 11 to 14. A low-cost general purpose (Intersil 741HS), a low-cost high-speed (Intersil 2515) and a high-speed fast-settling Datel AM-452 amplifier cover the principal application areas.

PACKAGE DIMENSIONS

18 PIN CERDIP



1. Lead no. 1 identified by dot or notch.
2. Dimensions in inches (millimeters).

Precision, Multiplying CMOS D/A Converters DAC-HA Series

FEATURES

- **10, 12 & 14 Bit Binary Models**
- **3 Digit BCD Model**
- **20 MHz Reference Bandwidth**
- **2 ppm/°C Gain Tempco**
- **+5V and +15V Supply Versions**
- **Input Protected**

GENERAL DESCRIPTION

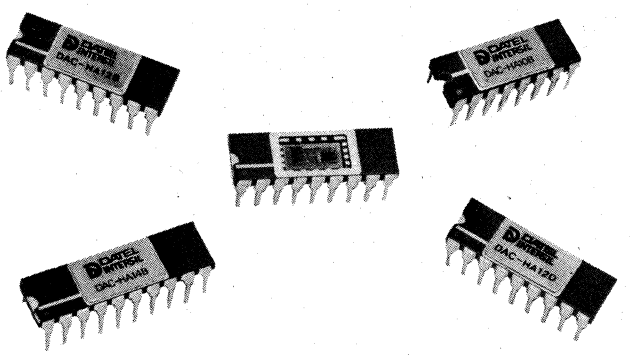
The DAC-HA Series are new, high performance multiplying digital to analog converters specifically designed for critical applications. The series features 10, 12, and 14 bit models and a 3 digit BCD model with a choice of either +5V or +15V power supply options. They are fabricated with advanced thin-film hybrid technology combining low ON-resistance CMOS switches with a precision laser trimmed R-2R ladder network. The ladder network is deposited on glass to realize low distributed capacitance resulting in a 20 MHz minimum reference bandwidth. Digital and power supply inputs are protected against overvoltage and latchup.

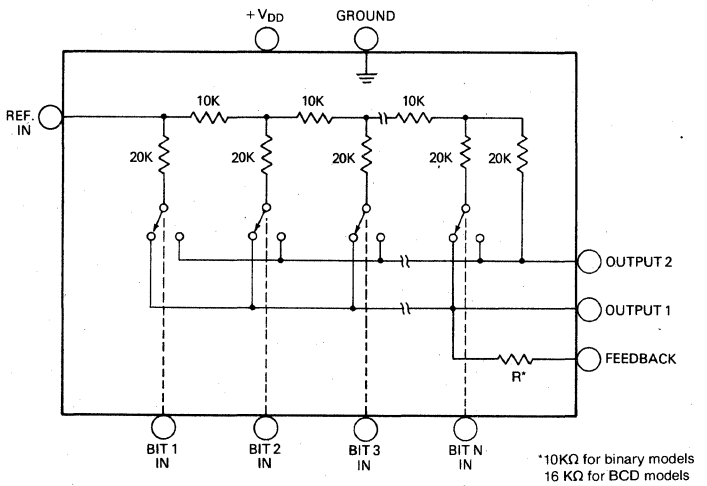
The DAC-HA series offer significant performance advantages over similar monolithic multiplying DAC's while retaining the industry 7500 series pin compatibility. Tightly controlled process parameters hold the ladder resistance to 10K ohms ±30% rather than the −50%, +100% tolerance common to monolithic versions. Close temperature tracking between the R-2R ladder and the feedback resistor results in a typical gain tempco of 2 ppm/°C. Linearity error is ±½ LSB max. for the 10 and 12 bit models and ±1 LSB max. for the 14 bit model.

The +5V supply versions draw only 1 μA of supply current while the +15V supply versions draw 1.4 mA; both have optimized accuracy at the specified supply voltages. Different models are also available for three standard operating temperature ranges along with MIL-STD-883 level B versions. The units are packaged in hermetically sealed 16, 18, or 20 pin ceramic packages for the 10, 12, and 14 bit verisons respectively.

Applications include digitally controlled attenuators, automatic gain control circuits, CRT character generation, one, two or four quadrant multiplier circuits, one or two quadrant divider circuits, complex function circuits and automatic bridge circuits.

CAUTION: These devices contain CMOS circuits and should be handled with standard anti-static procedures.





INPUT/OUTPUT CONNECTIONS

DAC-HA10B

PIN	FUNCTION
1	OUTPUT 1
2	OUTPUT 2
3	GROUND
4	BIT 1 IN (MSB)
5	BIT 2 IN
6	BIT 3 IN
7	BIT 4 IN
8	BIT 5 IN
9	BIT 6 IN
10	BIT 7 IN
11	BIT 8 IN
12	BIT 9 IN
13	BIT 10 IN (LSB)
14	+VDD
15	REFERENCE IN
16	FEEDBACK

DAC-HA12B, 12D

PIN	FUNCTION
1	OUTPUT 1
2	OUTPUT 2
3	GROUND
4	BIT 1 IN (MSB)
5	BIT 2 IN
6	BIT 3 IN
7	BIT 4 IN
8	BIT 5 IN
9	BIT 6 IN
10	BIT 7 IN
11	BIT 8 IN
12	BIT 9 IN
13	BIT 10 IN
14	BIT 11 IN
15	BIT 12 IN (LSB)
16	+VDD
17	REFERENCE IN
18	FEEDBACK

DAC-HA14B

PIN	FUNCTION
1	OUTPUT 1
2	OUTPUT 2
3	GROUND
4	BIT 1 IN (MSB)
5	BIT 2 IN
6	BIT 3 IN
7	BIT 4 IN
8	BIT 5 IN
9	BIT 6 IN
10	BIT 7 IN
11	BIT 8 IN
12	BIT 9 IN
13	BIT 10 IN
14	BIT 11 IN
15	BIT 12 IN
16	BIT 13 IN
17	BIT 14 IN (LSB)
18	+VDD
19	REFERENCE IN
20	FEEDBACK

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, DAC-HA SERIES Typical at 25°C. V_{REF} = +10V, +5V standard or +15V optional[1] power supply

	DAC-HA14B	DAC-HA12B	DAC-HA12D	DAC-HA10B
MAXIMUM RATINGS				
V_{DD}, +5V Supply Option	+15V, −10V	*	*	*
V_{DD}, +15V Supply Option	+40V, −30V	*	*	*
Logic Input Voltage	+10V, −5V	*	*	*
Reference Input Voltage	±25V	*	*	*
Output 1 or Output 2 Voltage	+5V, −0.5V	*	*	*
Feedback Resistor to Gnd	±25V	*	*	*
INPUTS				
Resolution	14 Bits	12 Bits	12 Bits	10 Bits
Coding, Unipolar Operation	Straight Binary	*	BCD	*
Coding, Bipolar Operation	Offset Binary	*	—	*
Logic Threshold, Bit ON ("1")[2]	≥+4.0V	*	*	*
Logic Threshold, Bit OFF ("0")[2]	≤+1.0V	*	*	*
Logic Input Current[3]	±1 μA	*	*	*
Reference Input Voltage Range	±12V	*	*	*
Reference Input Resistance	10K ±30%	*	*	*
Reference Input Resistance vs Temp.	0 to +50 ppm/°C	*	*	*
OUTPUTS				
Output Current Range, Either Output	$\pm V_{REF}/R_{IN}$	*	*	*
Output Capacitance, Output 1[4]	260 pF	260 pF	260 pF	55 pF
Output Capacitance, Output 2[4]	160 pF	160 pF	160 pF	18 pF
Output Capacitance, Output 1[5]	160 pF	160 pF	160 pF	18 pF
Output Capacitance, Output 2[5]	260 pF	260 pF	260 pF	55 pF
PERFORMANCE				
Integral Linearity Error[6], max.	±1 LSB	±½ LSB	±½ LSB	±½ LSB
Differential Linearity Error[6]	±½ LSB typ. ±1 LSB max.	±¼ LSB typ. ±½ LSB max.	±¼ LSB typ. ±½ LSB max.	±¼ LSB typ. ±½ LSB max.
Differential Linearity Error Over Temp[6]	±2 LSB max.	±1 LSB max.	±1 LSB max.	±1 LSB max.
Gain Linearity Error, max.	±1 LSB	±½ LSB	±½ LSB	±½ LSB
Gain Error, Before Trimming[7]	+0, −0.2%	*	*	*
Output Leakage Current, max.[8]	100 pA	100 pA	100 pA	50 pA
Gain Temp. Coefficient, ppm/°C[9]	2 typ, 5 max.	2 typ, 5 max.	2 typ, 5 max.	7 typ, 20 max.
Monotonicity	At 25°C	Over Temp Range	Over Temp Range	Over Temp Range
Output Current Settling Time, max.[10]	7 μsec.	5 μsec.	5 μsec.	1.3 μsec.
Reference Input Bandwidth, −3 dB	20 MHz	*	*	*
Feedthrough at 20 KHz	0.025%	0.025%	0.025%	0.01%
Power Supply Rejection	5 ppm of FSR/%	5 ppm of FSR/%	5 ppm of FSR/%	0.01% of FSR/%
POWER REQUIREMENT				
Standard Version Supply Voltage	+5 VDC	*	*	*
Standard Version Supply Range	+3V to +7.5V	*	*	*
Standard Version Supply Current, max.	1 μA	*	*	*
Optional Version Supply Voltage[1]	+15 VDC	*	*	*
Optional Version Supply Range	+7.5V to +20V	*	*	*
Optional Version Supply Current, max.	1.4 mA	*	*	*
PHYSICAL-ENVIRONMENTAL				
Operating Temp. Range, C Suffix	0°C to 70°C	*	*	*
R Suffix	−25°C to +85°C	*	*	*
M Suffix	−55°C to +125°C	*	*	*
Storage Temp. Range	−65°C to +150°C	*	*	*
Package Type, Ceramic	20 Pin DIP	18 Pin DIP	18 Pin DIP	16 Pin DIP

*Specification same as first column.

NOTES:

1. The optional +15V version is designated by the Suffix −1.
2. Interfaces with TTL logic. See Technical Notes
3. Over Operating Temperature Range
4. All Digital Inputs HI
5. All Digital Inputs LO
6. $V_{OUT}1 = V_{OUT}2 = \pm 200$ mV
7. Adjustable to Zero
8. At +125°C Leakages are 100 nA and 50 nA max. respectively.
9. Using feedback resistor.
10. To ½ LSB for full scale digital input change.

THEORY OF OPERATION

The circuit of the DAC-HA series uses a precision, thin-film R-2R ladder network with R = 10K ohms ±30%, as shown in Figure 1. An external reference source is applied at the input of the network, and, depending on the digital input code, the resulting current is split between the Output 1 and Output 2 terminals. The switches at the bottom of the 20K network resistors are low on-resistance, single pole double throw CMOS devices of the type shown in Figure 2. The equivalent input impedance seen by the reference source is shown in Figure 3.

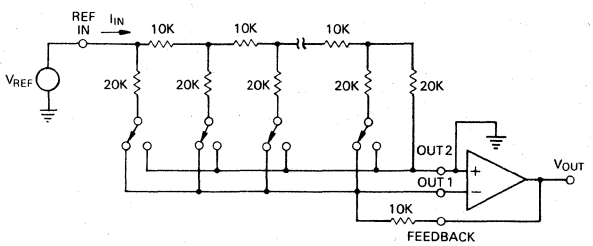


Figure 1. PRECISION DAC-HA CIRCUIT

From the reference end of the network, the input current divides in two at each successive junction as it flows down the ladder. It should be noted that the 20K terminating resistor at the right end of the network goes to Output 2 in the DAC-HA series rather than to ground as in monolithic devices of the 7500 type. The output currents at Output 1 and Output 2 represent the digital complements of one another except for a 1 LSB analog difference. The result is that when Output 1 and Output 2 are added together they always sum to the reference input current.

Furthermore, with a digital input code of 1000....0000, the two output currents are precisely equal. Therefore, in 4 quadrant multiplying applications where the two outputs are subtracted, the result is zero. With 7500 series monolithic units these currents do not cancel each other and an additional 1 LSB offset current must be externally provided to give exact cancellation.

The DAC-HA series are designed to be used with an external operational amplifier which converts the current output into a voltage. Since the feedback resistor tracks the ladder network with temperature, the resulting gain tempco is ±2 ppm/°C typical except for the 10 bit model. If the output current is used without the internal feedback resistor, the output current tempco is then 0 to −50 ppm/°C.

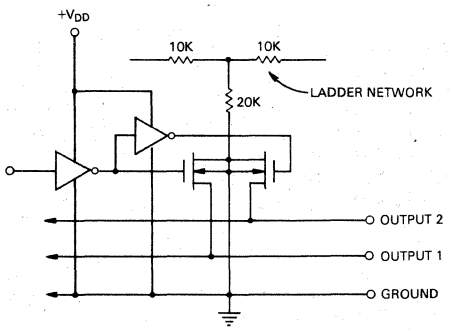


Figure 2. SINGLE POLE DOUBLE THROW CMOS SWITCH

With an external amplifier at Output 1 the output voltage ranges from zero to $-V_{REF}$ $(1-2^{-n})$, depending on the input code. If an external amplifier is used at Output 2 with the same value of feedback resistor, the output voltage ranges from zero to $-V_{REF}$ depending on input code.

The DAC-HA series have optimized linearity for the two power supply options +5V and +15V. It should be noted that while 7500 series devices operate over a +5V to +15V supply range, nonlinearity increases as the supply voltage is decreased from +15V.

To realize the specified linearity, it is necessary to carefully zero the input offset voltage of the amplifier or amplifiers used at the outputs. The input offset voltage should be zeroed to less than ±0.1 mV in order to have negligible effect on accuracy. Actually the two offset voltages can be as large as ±200 mV if they are within ±0.1 mV of each other.

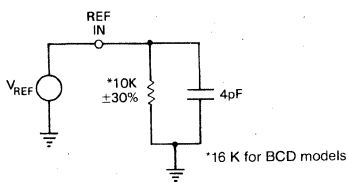


Figure 3. EQUIVALENT INPUT IMPEDANCE OF DAC-HA REFERENCE INPUT

CODING TABLE

CODE	SCALE	OUTPUT 1	OUTPUT 2
1111...11	FS-1 LSB	$I_{IN}(1-2^{-n})$	$I_{IN}(2^{-n})$
1100...00	+3/4 FS	$I_{IN}(2^{-1}+2^{-2})$	$I_{IN}(2^{-2})$
1000...01	+1/2 FS + 1 LSB	$I_{IN}(2^{-1}+2^{-n})$	$I_{IN}(2^{-1}-2^{-n})$
1000...00	+1/2 FS	$I_{IN}(2^{-1})$	$I_{IN}(2^{-1})$
0100...00	+1/4 FS	$I_{IN}(2^{-2})$	$I_{IN}(2^{-1}+2^{-2})$
0000...01	+1 LSB	$I_{IN}(2^{-n})$	$I_{IN}(1-2^{-n})$
0000...00	0	$I_{IN}(0)$	$I_{IN}(1)$

NOTE: $I_{IN} = \frac{V_{REF}}{R_{IN}}$

where R_{IN} is ladder network impedance, or 10k ±30%

OUTPUT EQUATIONS

$$\text{OUTPUT 1} = I_{IN}(a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + ... + a_n 2^{-n})$$

$$\text{OUTPUT 2} = I_{IN}(\bar{a}_1 2^{-1} + \bar{a}_2 2^{-2} + \bar{a}_3 2^{-3} + ... + \bar{a}_n 2^{-n} + 2^{-n})$$

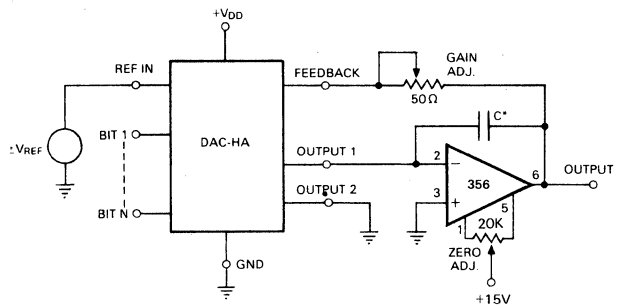
"a's" are digital coefficients, 0 or 1.
n = converter resolution in bits

TECHNICAL NOTES

1. CAUTION. The DAC-HA series contains MOS devices and should be handled carefully to prevent static charge pickup that might damage the units. The converters should be kept in conductive foam until ready for installation. During installation the user should be grounded by means of a conductive wrist strap. Do not insert or remove these devices from their sockets unless power is turned off.
2. Unused digital inputs should be connected to ground or to +5V, never left open.
3. In general, pull-up resistors are not required for TTL logic interfacing. The DAC-HA series will interface directly with all standard TTL circuits and operate within specifications.
4. The logic input voltages are stated as $\leq +1.0V$ for a logic "0" and $\geq +4.0V$ for a logic "1" at the recommended power supply voltages of +5V or +15V. For other supply voltages in the specified range, the logic "1" level becomes $V_{DD}-1$ for the 5V version and $\frac{V_{DD}}{3}-1$ for the +15V version.
5. For interfacing with HNIL or CMOS logic where logic HI is greater than +5V, CD4050 interface circuits should be used and connected as shown in the applications diagram.
6. The DAC-HA series devices are protected against both power supply and logic input overvoltages by means of series thin-film resistors. The result is that these devices are free from latch-up problems which have been associated with some CMOS multiplying DAC circuits in the past.
7. While the DAC-HA series gives optimum accuracy at recommended supply voltage and at room temperature, the maximum linearity error is ±1 LSB over both specified supply range and temperature range for the 10 and 12 bit models and is ±2 LSB for the 14 bit model.
8. The supply current is given as the quiescent value. The current increases to 200 μA max. for the +5V version and 1.6 mA max. for the +15V version with all bits switched at a 10 KHz rate at 50% duty cycle. Supply current increases at the rate of 1 μA per KHz of switching frequency.
9. The noise output of the DAC-HA devices can be computed from the Johnson noise of the resistance between either output terminal and ground. This resistance varies with input code from 6.67K (based on nominal ladder resistance of 10K) to 30K for Output 2 and from 6.67K to infinity for Output 1. When using an output amplifier at either output the feedback resistor is then in parallel with the ladder resistance, and the noise gain of the amplifier must also be used in the computation.
10. Feedthrough, which is specified at 20 KHz, is due to capacitive coupling from the reference input to the output, and increases directly with frequency. The frequency of the reference input is only limited by the amount of feedthrough error.
11. With most output amplifiers a small feedback capacitor across the feedback resistor is necessary to compensate for the output capacitance of the DAC-HA. By using a small trim capacitor, the compensation can be adjusted for optimum response.
12. It is recommended that output amplifiers with less than 25 nA input bias current be used with the DAC-HA series. This permits precise adjustment of the output voltage to zero with all digital inputs OFF and at the same time assures that the input offset voltage is minimized. For most applications the 356 type op amp is an excellent choice. For faster response, however, Datel's AM-462 is recommended.

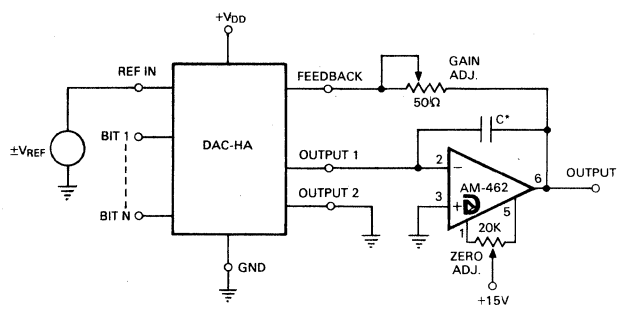
CONNECTIONS

DAC-HA CONNECTION WITH 356 OUTPUT AMPLIFIER



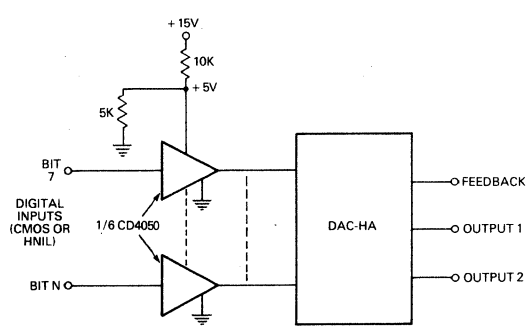
*Use 3 to 30pF trim capacitor and adjust for optimum step response.

DAC-HA CONNECTION FOR FAST VOLTAGE OUTPUT USING DATEL AM-462 MONOLITHIC OPERATIONAL AMPLIFIER



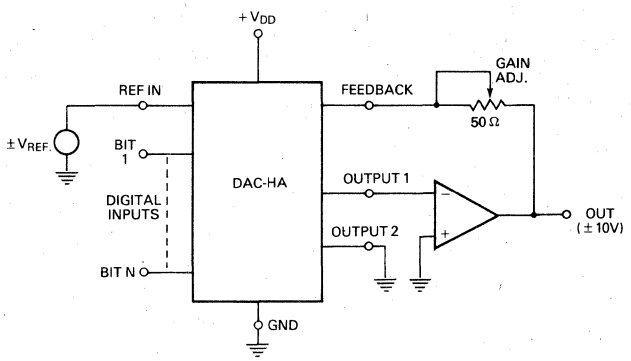
*Use 3 to 30pF trim capacitor and adjust for optimum step response.

CMOS OR HNIL LOGIC INTERFACE

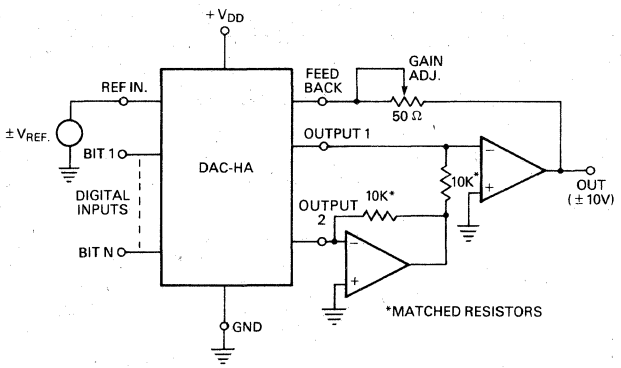


APPLICATIONS

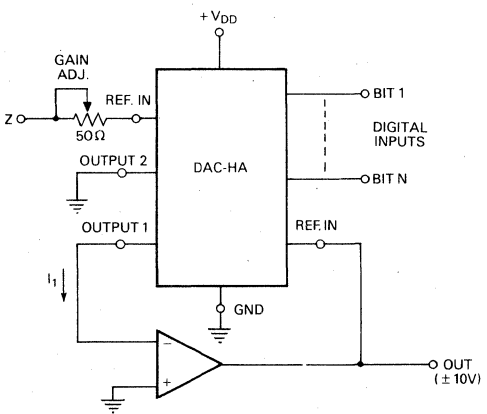
2 QUADRANT MULTIPLICATION (DIGITAL ATTENUATOR)



4 QUADRANT MULTIPLICATION



DIVISION CIRCUIT USING DAC-HA



(D) = Digital Input = $(a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + \ldots a_n 2^{-n})$

$$I_1 = \frac{\text{OUT (D)}}{R}$$ where R is internal ladder resistance = 10K

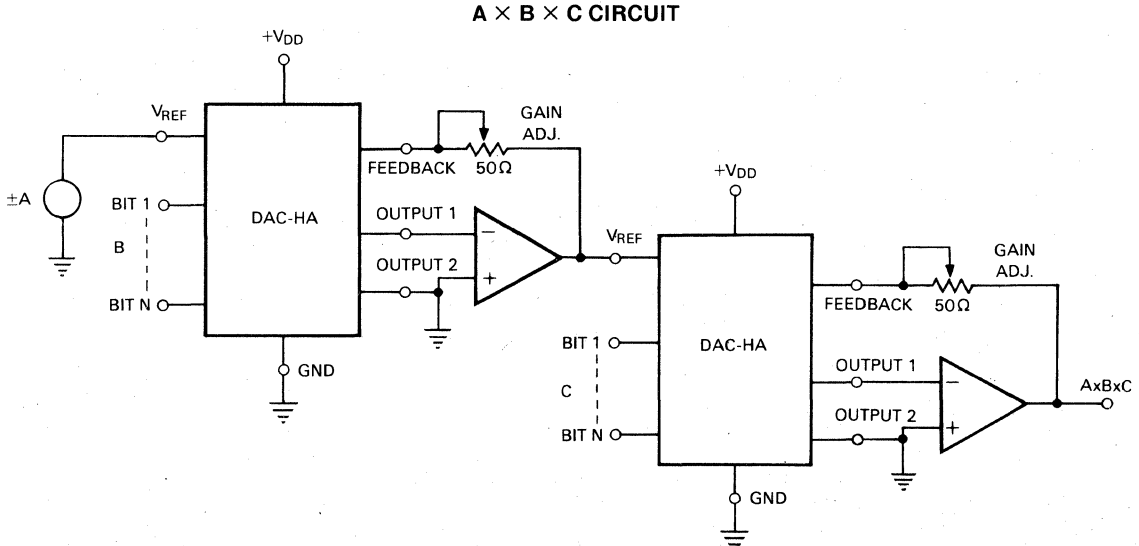
$$I_1 = \frac{-Z}{R}$$ R is feedback resistor which is matched to internal ladder resistance.

$$\frac{\text{OUT (D)}}{R} = \frac{-Z}{R}$$

$$\boxed{\text{OUT} = \frac{-Z}{(D)}}$$

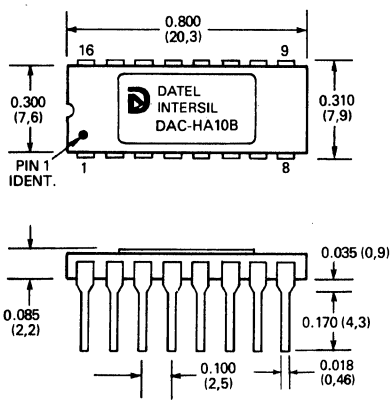
The circuit is stable for ±Z.

A × B × C CIRCUIT

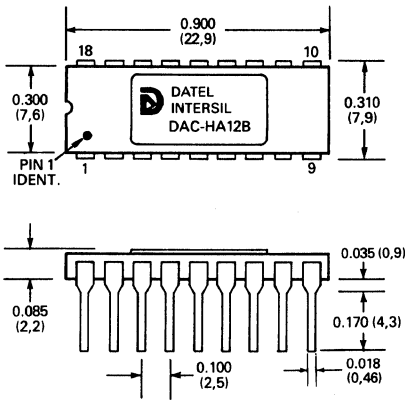


MECHANICAL DIMENSIONS—INCHES (MM)

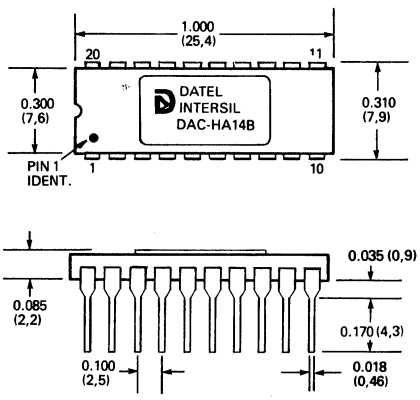
16-PIN DIP CERAMIC PACKAGE



18-PIN DIP CERAMIC PACKAGE



20-PIN DIP CERAMIC PACKAGE



ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	POWER SUPPLY	MODEL	OPERATING TEMP. RANGE	POWER SUPPLY
DAC-HA10BC	0 to 70°C	+5 VDC	**DAC-HA10BC-1**	0 to 70°C	+15 VDC
DAC-HA10BR	−25 to +85°C	+5 VDC	**DAC-HA10BR-1**	−25 to +85°C	+15 VDC
DAC-HA10BM	−55 to +125°C	+5 VDC	**DAC-HA10BM-1**	−55 to +125°C	+15 VDC
DAC-HA12BC	0 to 70°C	+5 VDC	**DAC-HA12BC-1**	0 to 70°C	+15 VDC
DAC-HA12BR	−25 to +85°C	+5 VDC	**DAC-HA12BR-1**	−25 to +85°C	+15 VDC
DAC-HA12BM	−55 to +125°C	+5 VDC	**DAC-HA12BM-1**	−55 to +125°C	+15 VDC
DAC-HA12DC	0 to 70°C	+5 VDC	**DAC-HA12DC-1**	0 to 70°C	+15 VDC
DAC-HA12DR	−25 to +85°C	+5 VDC	**DAC-HA12DR-1**	−25 to +85°C	+15 VDC
DAC-HA12DM	−55 to +125°C	+5 VDC	**DAC-HA12DM-1**	−55 to +125°C	+15 VDC
DAC-HA14BC	0 to 70°C	+5 VDC	**DAC-HA14BC-1**	0 to 70°C	+15 VDC
DAC-HA14BR	−25 to +85°C	+5 VDC	**DAC-HA14BR-1**	−25 to +85°C	+15 VDC
DAC-HA14BM	−55 to +125°C	+5 VDC	**DAC-HA14BM-1**	−55 to +125°C	+15 VDC

Trimming Potentiometer: TP50 (50 ohms)
For high reliability versions of the DAC-HA series including units screened to MIL-STD-883 level B, contact factory.

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

DATEL INTERSIL
11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617)339-9341 / TWX 710-346-1953 / TLX 951340
Santa Ana, (714)835-2751, (L.A.) (213)933-7256 • Sunnyvale, CA (408)733-2424 • Gaithersburg, MD (301)840-9490
• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Ultra-Fast Microelectronic D/A Converters DAC-HF Series

FEATURES

- **8, 10, 12 Bit Resolution**
- **Settling Times to 25 nsec.**
- **20 ppm/°C Tempco**
- **Unipolar or Bipolar Operation**
- **Current Output**
- **Internal Feedback Resistor**

GENERAL DESCRIPTION

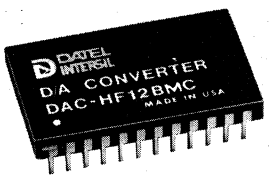
The DAC-HF series of hybrid DAC's are ultra high speed, current output devices. They incorporate state-of-the art performance in a miniature package, achieving maximum output settling times of 25 nanoseconds for the 8 and 10 bit models and 50 nanoseconds for the 12 bit model. They can be used to drive a resistor load directly for up to ±1V output or a fast operational amplifier (such as Datel-Intersil's AM-500) for higher voltage outputs with sub-microsecond settling times. A tapped feedback resistor and a bipolar offset resistor are included internally to give five programmable output voltage ranges with an external op amp.

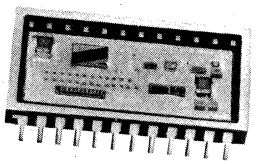
The DAC-HF design combines proven hybrid production techniques with advanced circuit design to realize high speed current switching. The design incorporates fast PNP current switches driving a low impedance R-2R thin film ladder network. The nichrome thin film resistor network is deposited by electron beam evaporation on a low capacitance substrate to assure high speed performance. The resistors are then functionally trimmed by laser for optimum linearity.

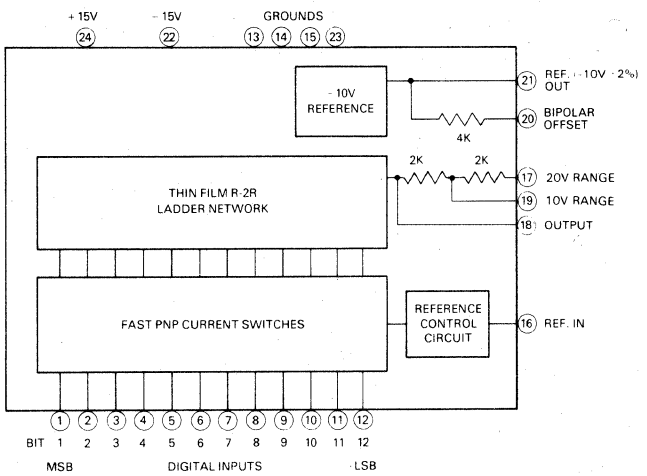
The digital inputs are TTL compatible and use straight binary coding for unipolar operation and offset binary coding for bipolar operation. Output current is 0 to +5 mA for unipolar operation and ±2.5 mA for bipolar operation into an output amplifier summing junction. Linearity is ±½ LSB, and the converters are monotonic over the operating temperature range specified for each. Gain temperature coefficient is ±20 ppm/°C maximum.

Applications for the DAC-HF series include high speed function generators, fast computer control systems, graphic display systems, and CRT displays.

Power supply requirement is ±15 VDC with less than 780 milliwatts consumption. The DAC-HF is available in models covering three operating temperature ranges.

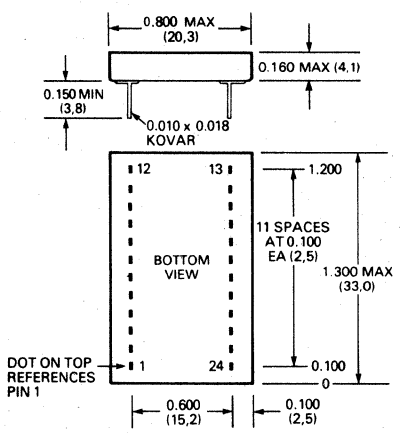






NOTE: FOR DAC-HF10B PINS 11 & 12 ARE NO CONNECTION
FOR DAC-HF8B PINS 9, 10, 11 & 12 ARE NO CONNECTION

MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN (MSB)	13	GROUND
2	BIT 2 IN	14	GROUND
3	BIT 3 IN	15	GROUND
4	BIT 4 IN	16	REF. IN
5	BIT 5 IN	17	20 V RANGE
6	BIT 6 IN	18	OUTPUT
7	BIT 7 IN	19	10 V RANGE
8	BIT 8 IN	20	BIPOLAR OFFSET
9	BIT 9 IN	21	REF. OUT
10	BIT 10 IN	22	-15 VDC
11	BIT 11 IN	23	GROUND
12	BIT 12 IN (LSB)	24	+15 VDC

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, DAC-HF SERIES
(Typical at 25°C, ±15V supplies unless otherwise specified)

	8B	10B	12B
MAXIMUM RATINGS			
Positive Supply, Pin 24	+18V		
Negative Supply, Pin 22	−18V		
Digital Input Voltage, Pins 1 to 12	+15V		
INPUTS			
Resolution, Bits	8	10	12
Coding, Unipolar Output	Straight Binary		
Coding, Bipolar Output	Offset Binary		
Input Logic Level, Bit ON ("1")	+2.2 to +5.5V @ +40μA		
Input Logic Level, Bit OFF ("0")	0V to +0.8V @ 2.6mA		
OUTPUT			
Output Current Range, Unipolar	0 to +5 mA		
Output Current Range, Bipolar	±2.5mA		
Output Voltage Compliance	±1.2V		
Output Voltage Ranges[2]	0 to −5V 0 to −10V ±2.5V ±5V ±10V		
Output Resistance	400 ohms		
Output Capacitance	15 pF		
Output Leakage Current, All Bits OFF	15 nA		
PERFORMANCE			
Linearity Error, max	±1/2 LSB		
Differential Linearity Error, max	±1/2 LSB		
Diff. Linearity Tempco	±2 ppm/°C		
Monotonicity	Guaranteed over oper. temp. range		
Gain Tempco, max	±20 ppm/°C		
Offset Tempco, Bipolar, max	±10 ppm/°C of F.S.R.[3]		
Zero Tempco, max	±1.5 ppm/°C of F.S.R.[3]		
Settling Time, nsec. max.[1]	25	25	50
Power Supply Sensitivity	0.01%/% Supply		
POWER REQUIREMENT			
Supply Voltage	±15VDC ±0.5V		
Positive Quiescent Current, max	30mA	35mA	40mA
Negative Quiescent Current, max	12mA	12mA	12mA
PHYSICAL-ENVIRONMENTAL			
Operating Temperature Range	0°C to +70°C (BMC) −25°C to +85°C (BMR) −55°C to +125°C (BMM)		
Storage Temperature Range	−65°C to +150°C		
Package Type	24 Pin Ceramic DIP		
Pins	.010 x .018 inch Kovar		
Weight	0.2 oz. (6g.)		

NOTES:
1. Full scale current change to 1 LSB with 400Ω load.
2. With External Operational Amplifier.
3. F.S.R. is Full Scale Range, or the difference between minimum and maximum output values.

TECHNICAL NOTES

1. Proper operation of the DAC-HF series converters is dependent on good board layout and connection practices. Supplies should be bypassed as shown in the connection diagrams. Bypass capacitors should be mounted close to the converter, directly to the supply pins where possible.
2. Use of a ground plane is particularly important in high speed D to A converters as it reduces high frequency noise and aids in decoupling the digital inputs from the analog output. Ground loop problems are avoided by connecting all grounds on the board to the ground plane. The configuration of the ground plane directly below the DAC-HF is shown in the ground plane layout diagram. The remainder of the ground plane should include as much of the circuit board as possible.
3. When the converter is configured for voltage output with an external op-amp, the leads from the converter to the output amplifier should be kept as short as possible.
4. The high speed current switching technique used in the DAC-HF series inherently reduces the amplitude and duration of large transient spikes at the output ("glitches"). The most severe glitches occur at half-scale, the major carry transition from 011...1 to 100...0 or vice versa. At this time a skewing of the input codes can create a transition state code of 111...1. The duration of the "transition state code" is dependent on the degree of skewing but its effect is dependent on the speed of the DAC (an ultra-fast DAC will respond to these brief spurious inputs to a greater degree than a slow DAC). The effects of input skewing can be easily minimized through the use of a high-speed input register to match input switching times. The input register recommended for use with the DAC-HF is easily implemented with two Texas Instruments SN74S174 hex D-type flip-flops. This register will reduce glitches to a very low level and ensure fast output settling times.
5. Testing of the DAC-HF should be performed with a low capacitance test probe (such as a 10X probe). Care should be taken to assure the shortest possible connection between probe ground and circuit ground. Long probe ground leads may pick up environmental E.M.I. causing artifacts on the scope display, i.e. signals that do not originate at the unit under test.
6. Passive components used with the DAC-HF may be as indicated here: 0.1 μF and 1 μF bypass capacitors should be ceramic type and tantalum type respectively; the 400Ω output load is a 0.1% 10 ppm/°C metal film type; adjustment potentiometers are cermet types; other resistors may be ±10% carbon composition types.
7. Output voltage compliance is ±1.2V to preserve the linearity of the converter. In the bipolar mode the DAC-HF can be operated with no load to give an output voltage of ±1.0V. In the unipolar mode the load resistance must be less than 600Ω to give less than +1.2V output. The specified output currents of 0 to +5 mA and ±2.5 mA are measured into a short circuit or an operational amplifier summing junction.

ORDERING INFORMATION

MODEL	TEMP. RANGE	SEAL
DAC-HF8BMC	0° to +70°C	Hermetic
DAC-HF8BMR	−25° to +85°C	Hermetic
DAC-HF8BMM	−55° to +125°C	Hermetic
DAC-HF10BMC	0° to +70°C	Hermetic
DAC-HF10BMR	−25° to +85°C	Hermetic
DAC-HF10BMM	−55° to +125°C	Hermetic
DAC-HF12BMC	0° to +70°C	Hermetic
DAC-HF12BMR	−25° to +85°C	Hermetic
DAC-HF12BMM	−55° to +125°C	Hermetic

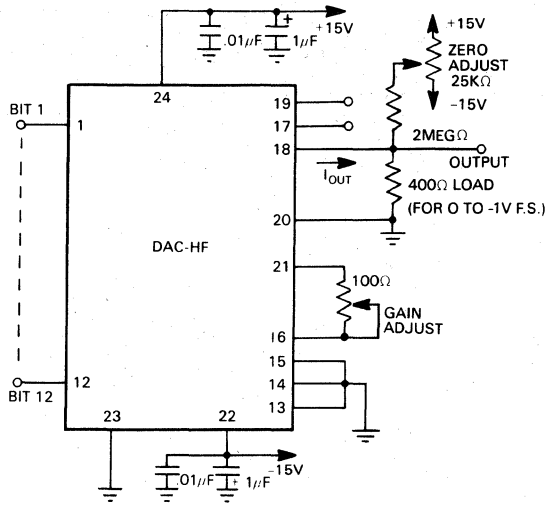
Mating Socket: DILS-3 (24-pin socket)
Trimming Potentiometers: TP-100 or TP25K

For high reliability versions of the DAC-HF series including units screened to MIL-STD-883 Level B, contact factory.

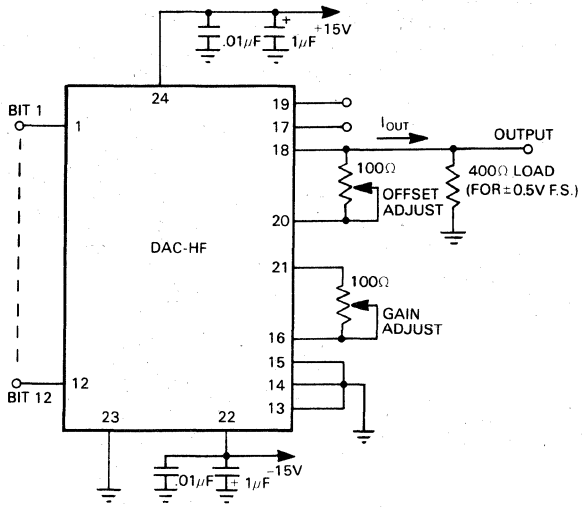
THESE CONVERTERS ARE COVERED BY GSA CONTRACT

CONNECTION AND CALIBRATION

UNIPOLAR CURRENT OUTPUT CONNECTIONS



BIPOLAR CURRENT OUTPUT CONNECTIONS



UNIPOLAR CURRENT OUTPUT CALIBRATION PROCEDURE

1. Connect the converter as shown in the connection diagram.
2. Set all inputs LO and adjust the ZERO ADJUST potentiometer for a reading of 0V at the output.
3. Set all inputs HI and adjust the GAIN ADJUST potentiometer for a reading of −F.S. +ILSB (given in the coding table for 12 bit units).

BIPOLAR CURRENT OUTPUT CALIBRATION PROCEDURE

1. Connect the converter as shown in the connection diagram.
2. Set all inputs LO and adjust the OFFSET ADJUST potentiometer for an output reading of +F.S., (given in the coding table for 12 bit units).
3. Set all inputs HI and adjust the GAIN ADJUST potentiometer for an output reading of −F.S. +1 LSB, (given in the coding table for 12 bit units).

CODING TABLES
UNIPOLAR OUTPUT

UNIPOLAR SCALE	INPUT CODING STRAIGHT BINARY	ANALOG OUTPUT 0 to +1V F.S.	0 to −5V F.S.	0 to −10V F.S.
F.S. −1 LSB	1111 1111 1111	+0.9998V	−4.9988V	−9.9976V
−¾ F.S.	1100 0000 0000	+0.7500V	−3.7500V	−7.5000V
−½ F.S.	1000 0000 0000	+0.5000V	−2.5000V	−5.0000V
−¼ F.S.	0100 0000 0000	+0.2500V	−1.2500V	−2.5000V
−1 LSB	0000 0000 0001	+0.0002V	−0.0012V	−0.0024V
0	0000 0000 0000	0.0000V	0.0000V	0.0000V

BIPOLAR OUTPUT

BIPOLAR SCALE	INPUT CODING OFFSET BINARY	ANALOG OUTPUT ±0.5V F.S.	±2.5V F.S.	±5V F.S.	±10V F.S.
−F.S.+1LSB	1111 1111 1111	+0.4998V	−2.4988V	−4.9976V	−9.9951V
−½ F.S.	1100 0000 0000	+0.1250V	−1.2500V	−2.5000V	−5.0000V
−1 LSB	1000 0000 0001	+0.0002V	−0.0012V	−0.0024V	−0.0049V
0	1000 0000 0000	0.0000V	0.0000V	0.0000V	0.0000V
+½ F.S.	0100 0000 0000	−0.1250V	+1.2500V	+2.500V	+5.0000V
+F.S.−1LSB	0000 0000 0001	−0.4998V	+2.4988V	+4.9976V	+9.9951V
+F.S.	0000 0000 0000	−0.5000V	+2.5000V	+5.0000V	+10.0000V

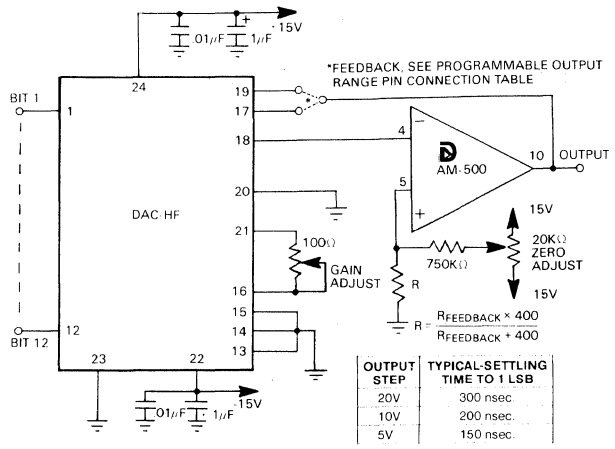
PROGRAMMABLE OUTPUT RANGE PIN CONNECTIONS

OUTPUT VOLTAGE RANGE	FEEDBACK CONNECTION	CONNECT THESE PINS TOGETHER
0 to −5V	PIN 19	PIN 17 to PIN 18 PIN 20 to PIN 23
0 to −10V	PIN 19	PIN 20 to PIN 23
±2.5V	PIN 19	PIN 17 to PIN 18 PIN 20 to PIN 23
±5V	PIN 19	PIN 20 to PIN 23
±10V	PIN 17	PIN 20 to PIN 23

In all Programmable Output Ranges PIN 18 connects to external OP-AMP inverting input

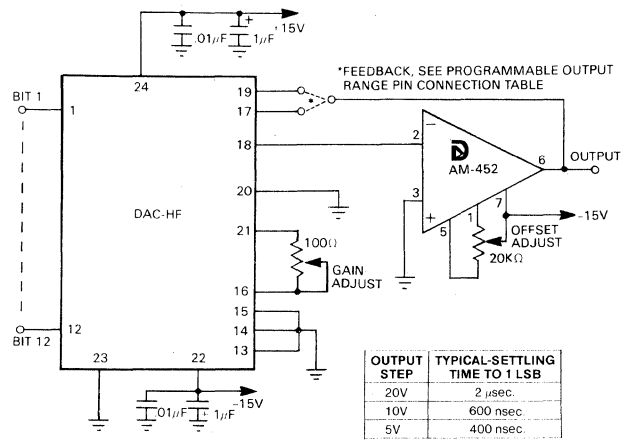
APPLICATIONS

ULTRA-FAST VOLTAGE OUTPUT



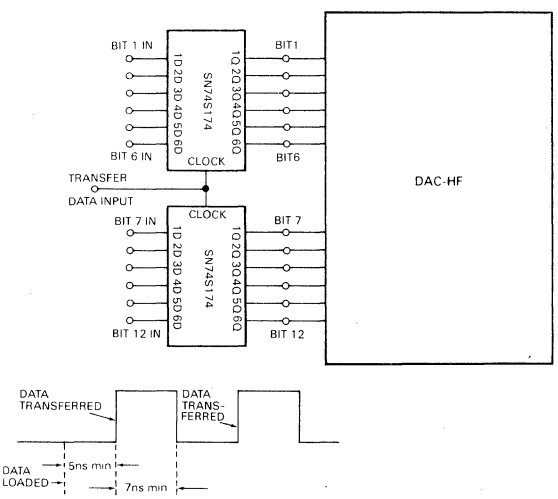
OUTPUT STEP	TYPICAL-SETTLING TIME TO 1 LSB
20V	300 nsec.
10V	200 nsec.
5V	150 nsec.

FAST VOLTAGE OUTPUT CIRCUIT

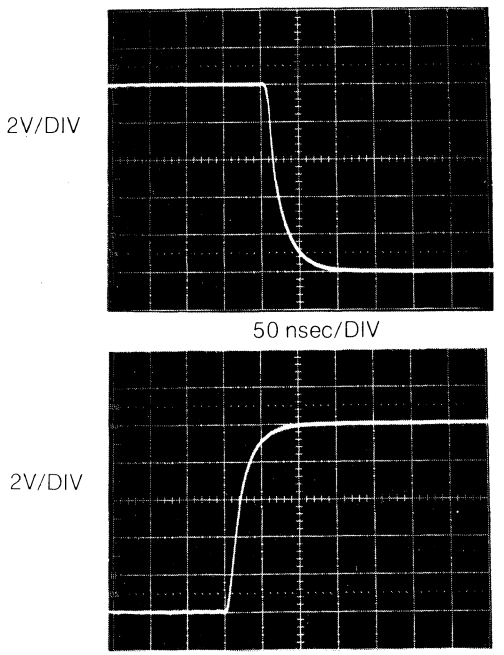


OUTPUT STEP	TYPICAL-SETTLING TIME TO 1 LSB
20V	2 μsec.
10V	600 nsec.
5V	400 nsec.

HIGH SPEED INPUT REGISTER

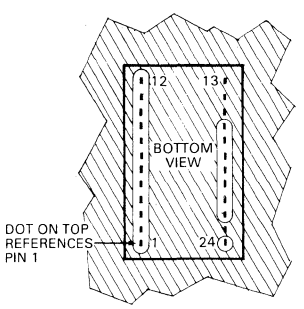


VOLTAGE OUTPUT WAVEFORMS

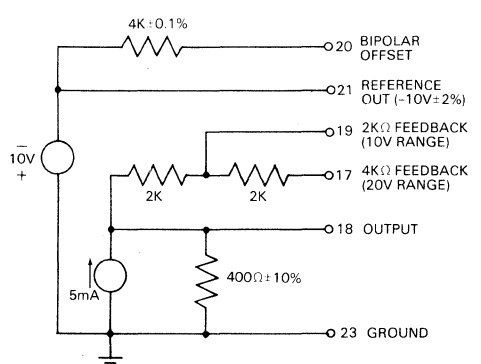


DAC-HF with AM-500, ±5V output full scale (10V) step

GROUND PLANE LAYOUT



EQUIVALENT OUTPUT CIRCUIT



DATEL INTERSIL
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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

12-Bit Hybrid DAC's with Input Register DAC-HK Series

FEATURES

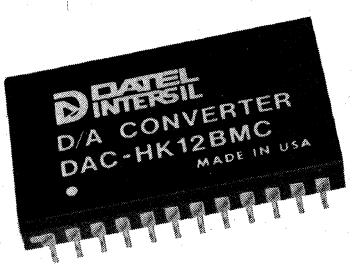
- 12-Bit Resolution
- 20 ppm/°C Tempco
- Input Register
- 3 Coding Options
- Fast Settling Time

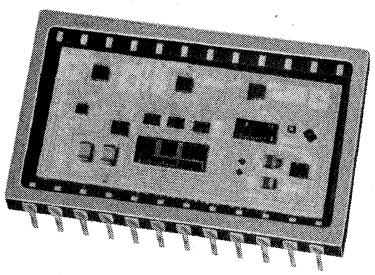
GENERAL DESCRIPTION

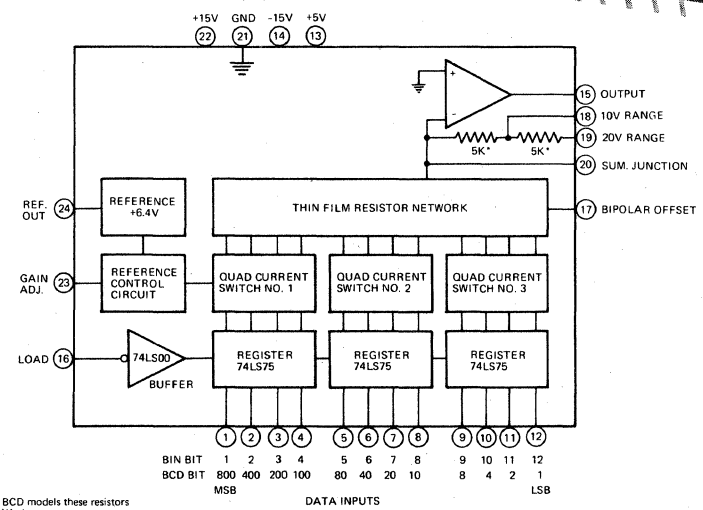
The DAC-HK series hybrid D/A converters are high performance 12-bit devices with a fast settling voltage output. They incorporate a level controlled input storage register and are specifically designed for systems applications such as data bus interfacing with computers. When the "load" input is high data in the storage register is held, and when the load input is low data is transferred through to the DAC. There are three basic models available by coding option: binary, BCD, and two's complement. The output voltage ranges are externally pin-programmable and include: 0 to +2.5 V, 0 to +5 V, 0 to +10 V, ±2.5 V, ±5 V, and ±10 V.

The DAC-HK design is based on proven, reliable thin film hybrid technology. Quad current switches are combined with a low T.C. thin film resistor network and a low T.C. Zener reference to achieve better than 20 ppm/°C gain tempco. Optimum linearity is attained by functional laser trimming of the thin film nichrome resistors. The tight temperature tracking of these resistors and the quad current switch transistors result in a differential linearity error tempco of only 2 ppm/°C. Each model of the DAC-HK series is monotonic over its operating temperature range.

The converters are cased in 24-pin ceramic packages. Models are available for three different operating temperature ranges: 0 to 70, −25 to +85, and −55 to +125 degrees Centigrade. High reliability versions of each model are also available under Datel-Intersil's "S" program and MIL-STD-883 level B screening. Power requirement is ±15 VDC and +5 VDC. Total power dissipation is 900 milliwatts.

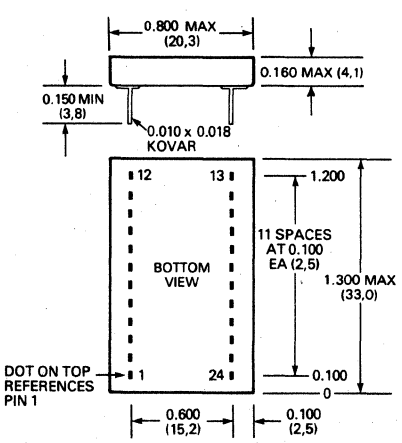






*For BCD models these resistors are 4K ohms.

MECHANICAL DIMENSIONS - INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN (MSB)	13	+5 VDC
2	BIT 2 IN	14	−15 VDC
3	BIT 3 IN	15	OUTPUT
4	BIT 4 IN	16	LOAD
5	BIT 5 IN	17	BIPOLAR OFF.
6	BIT 6 IN	18	10 V RANGE
7	BIT 7 IN	19	20 V RANGE
8	BIT 8 IN	20	SUM. JUNCTION
9	BIT 9 IN	21	GROUND
10	BIT 10 IN	22	+15 VDC
11	BIT 11 IN	23	GAIN ADJ.
12	BIT 12 IN (LSB)	24	REF OUT

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, DAC-HK SERIES
(Typical at 25°C, ±15 V and +5 V supplies unless otherwise noted)

	DAC-HK12B	DAC-HK12D
MAXIMUM RATINGS		
Positive Supply, pin 22	+18 V	*
Negative Supply, pin 14	−18 V	*
Logic Supply, pin 13	+5.25 V	*
Digital Input Voltage, pins 1-12 & 16	+5.5 V	*
Output Current, pin 15	±20 mA	*
INPUTS		
Resolution	12 bits	3 digits
Coding, unipolar output	Straight Binary	BCD
Coding, bipolar output	Offset Binary	-
	Two's Complement [1]	-
Input Logic Level, bit ON ("1")	+2.0 V to +5.5 V	
Input Logic Level, bit OFF ("0")	0 V to +0.8 V	
Logic Loading	1 LSTTL load	
Load Input[2]	HI ("1") = hold data	
	LO ("0") = transfer data	
Load Input Loading	3 LSTTL loads	
OUTPUT		
Output Voltage Ranges[3], unipolar	0 to +5 V	0 to +2.5 V
	0 to +10 V	0 to +5 V
	-	0 to +10 V
Output Voltage Ranges[3], bipolar	±2.5 V	-
	±5 V	-
	±10 V	-
Output Current	±5 mA min.	*
Output Impedance	0.05 ohm	*
PERFORMANCE		
Linearity Error, max.	±½ LSB	±¼ LSB
Differential Linearity Error, max.	±½ LSB	±¼ LSB
Gain Error, before trimming	±0.1%	*
Zero Error, before trimming	±0.1%	*
Gain Tempco, max.	±20 ppm/°C	*
Zero Tempco, unipolar, max.	±5 ppm/°C of FSR	*
Offset Tempco, bipolar, max.	±10 ppm/°C of FSR	*
Diff. Linearity Error Tempco	±2 ppm/°C of FSR	*
Monotonicity	Guaranteed over oper. temp. range	
Settling Time, 5 V change	3 μsec.	3 μsec.
Settling Time, 10 V change	3 μsec.	4 μsec.
Settling Time, 20 V change	4 μsec.	-
Settling Time, 1 LSB change	800 nsec.	*
Slew Rate	20 V/μsec.	*
Power Supply Rejection	±0.002% FSR/%	*
POWER REQUIREMENT	+15 VDC ±0.5 V at 15 mA	
	−15 VDC ±0.5 V at 30 mA	
	+5 VDC ±0.25V at 65mA	
PHYSICAL-ENVIRONMENTAL		
Operating Temperature Range	0°C to 70°C (BGC, BMC)	
	−25°C to +85°C (BMR)	
	−55°C to +125°C (BMM)	
Storage Temperature Range	−55°C to +125°C	
Package Type	24-pin Ceramic DIP	
Pins	0.010 × 0.018 inch Kovar	
Weight	0.2 oz. (6g.)	

*Same specification as first column.

NOTES:

1. For two's complement coding order the model described under ordering information.
2. Logic levels are the same as for data inputs.
3. By external pin connection.

TECHNICAL NOTES

1. It is recommended that these converters be operated with local supply bypass capacitors of 1 μF (tantalum type) at the +15, −15, and +5 V supply pins. The capacitors should be connected as close to the pins as possible. In high RFI noise environments these capacitors should be shunted with .01 μF ceramic capacitors.
2. The analog, digital, and power grounds should be separated from each other as close as possible to pin 21 where they all must come together.
3. The "load" control pin is a level triggered input which causes the register to hold data with a HI input and transfer data to the DAC with a LO input.
4. A setup time of 50 nsec. minimum must be allowed for the input data. The DAC output voltage begins to change when the register output changes.
5. The external gain adjustment shown in the Connection Diagrams has a range of ±0.2% of full scale. If a wider range is desired the 18-Megohm resistor can be decreased slightly in value. The full scale output is typically accurate within ±0.1% with no adjustment. The zero, or offset, adjustment has a range of ±0.35% of FS.
6. If the reference output terminal (pin 24) is used an operational amplifier in non-inverting mode should be used as a buffer. Current drawn from pin 24 should be limited to ±10μA in order not to affect the T.C. of the reference.

ORDERING INFORMATION

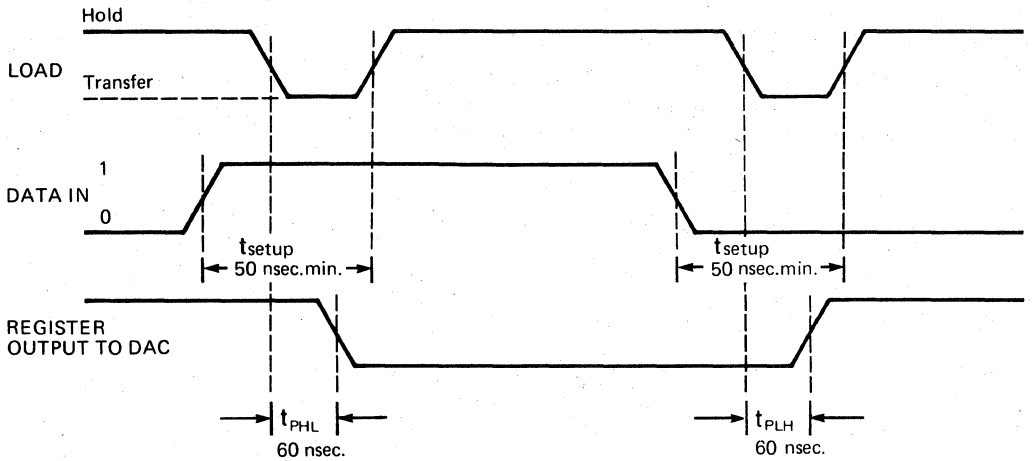
MODEL	TEMP. RANGE	SEAL
Binary Coding		
DAC-HK12BGC	0 to 70°C	Epoxy
DAC-HK12BMC	0 to 70°C	Herm.
DAC-HK12BMR	-25 to +85°C	Herm.
DAC-HK12BMM	-55 to +125°C	Herm.
BCD Coding		
DAC-HK12DGC	0 to 70°C	Epoxy
DAC-HK12DMC	0 to 70°C	Herm.
DAC-HK12DMR	-25 to +125°C	Herm.
DAC-HK12DMM	-55 to +125°C	Herm.
2's Complement Coding		
DAC-HK12BGC-2	0 to 70°C	Epoxy
DAC-HK12BMC-2	0 to 70°C	Herm.
DAC-HK12BMR-2	-25 to +85°C	Herm.
DAC-HK12BMM-2	-55 to +125°C	Herm.

Mating Socket: DILS-3(24-pin socket)
Trimming Potentiometers: TP100K (100K ohms)

For high reliability versions of the DAC-HK series, including units screened to MIL-STD-883 level B, contact factory.

THESE CONVERTERS ARE COVERED BY GSA CONTRACT.

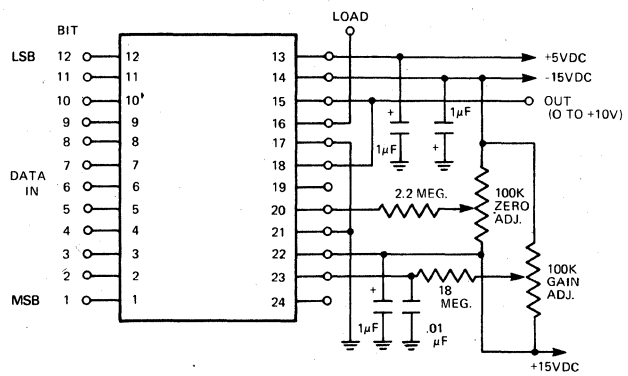
TIMING DIAGRAM



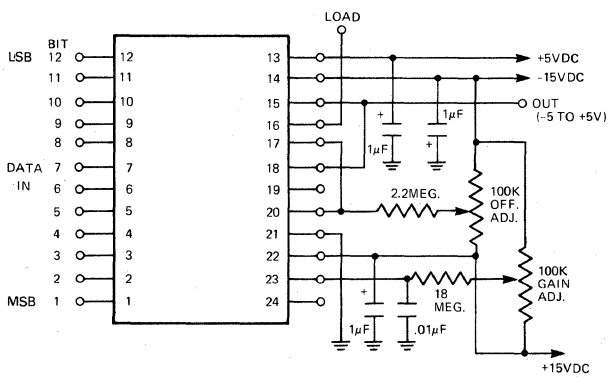
All rise and fall times ≤ 10 nsec.

CONNECTION DIAGRAMS

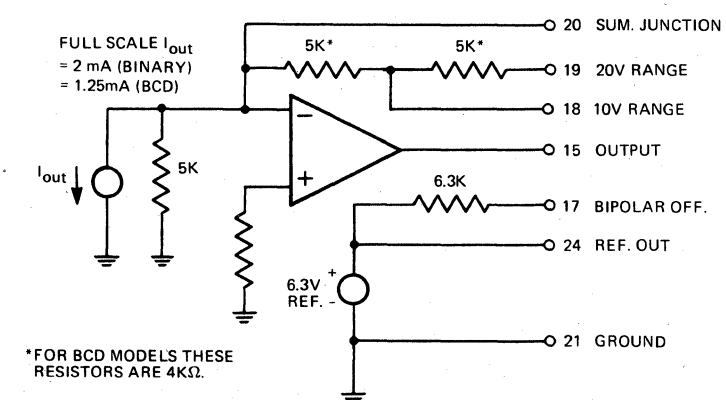
UNIPOLAR OPERATION (0 to +10V)



BIPOLAR OPERATION (±5 V)



OUTPUT CIRCUIT



*FOR BCD MODELS THESE RESISTORS ARE 4KΩ.

OUTPUT RANGE SELECTION

BINARY, 2's COMP.	CONNECT THESE PINS TOGETHER		
±10 V	15 & 19	17 & 20	
±5 V	15 & 18	17 & 20	
±2.5 V	15 & 18	17 & 20	19 & 20
+10 V	15 & 18	17 & 21	
+5 V	15 & 18	17 & 21	19 & 20
BCD	**CONNECT THESE PINS TOGETHER**		
+10 V	15 & 19		17 & 21
+ 5 V	15 & 18		17 & 21
+2.5 V	15 & 18	19 & 20	17 & 21

CODING TABLES

UNIPOLAR OPERATION

STRAIGHT BINARY	OUTPUT RANGES	
MSB LSB	0 to +10 V	0 to +5 V
1111 1111 1111	+9.9976	+4.9988
1100 0000 0000	+7.5000	+3.7500
1000 0000 0000	+5.0000	+2.5000
0100 0000 0000	+2.5000	+1.2500
0000 0000 0001	+0.0024	+0.0012
0000 0000 0000	0.0000	0.0000

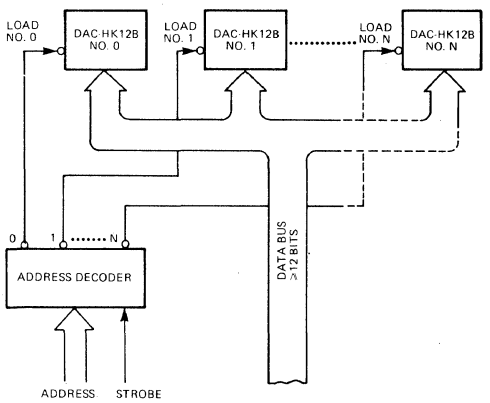
BCD	OUTPUT RANGES		
MSB LSB	0 to +10 V	0 to +5 V	0 to +2.5 V
1001 1001 1001	+9.990	+4.995	+2.498
1000 0101 0000	+7.500	+3.750	+1.875
0101 0000 0000	+5.000	+2.500	+1.250
0010 0101 0000	+2.500	+1.250	+0.625
0000 0000 0001	+0.010	+0.005	+0.003
0000 0000 0000	0.000	0.000	0.000

BIPOLAR OPERATION

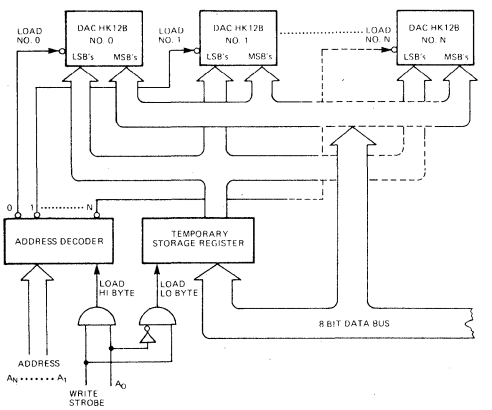
OFFSET BINARY	TWO's COMPLEMENT	OUTPUT RANGES		
MSB LSB	MSB LSB	±10 V	±5 V	±2.5 V
1111 1111 1111	0111 1111 1111	+9.9951	+4.9976	+2.4988
1100 0000 0000	0100 0000 0000	+5.0000	+2.5000	+1.2500
1000 0000 0000	0000 0000 0000	0.0000	0.0000	0.0000
0100 0000 0000	1100 0000 0000	−5.000	−2.5000	−1.2500
0000 0000 0001	1000 0000 0001	−9.9951	−4.9976	−2.4988
0000 0000 0000	1000 0000 0000	−10.0000	−5.0000	−2.5000

APPLICATION

INTERFACING TO ≥ 12 BIT DATA BUS



INTERFACING TO 8 BIT DATA BUS



CALIBRATION PROCEDURE

Select the desired output voltage range and connect the converter up as shown in the Output Range Selection Table and the Connection Diagrams. Refer to the Coding Tables.

UNIPOLAR OPERATION

1. **Zero Adjustment.** Set the input digital code to 0000 0000 0000 and adjust the ZERO ADJ. potentiometer to give 0.0000 V output.
2. **Gain Adjustment.** Set the input digital code to 1111 1111 1111 (straight binary) or 1001 1001 1001 (BCD) and adjust the GAIN ADJ. potentiometer to give the full scale output voltage shown in the Coding Table.

BIPOLAR OPERATION

1. **Offset Adjustment.** Set the digital input code to 0000 0000 0000 (offset binary) or 1000 0000 0000 (two's complement) and adjust the OFFSET ADJ. potentiometer to give the negative full scale output voltage shown in the Coding Table.
2. **Gain Adjustment.** Set the digital input code to 1111 1111 1111 (offset binary) or a 0111 1111 1111 (two's complement) and adjust the GAIN ADJ. potentiometer to give the positive full scale output voltage shown in the Coding Table.

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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

16-Bit, Microelectronic Digital-to-Analog Converters DAC-HP16B And DAC-HP16D

FEATURES

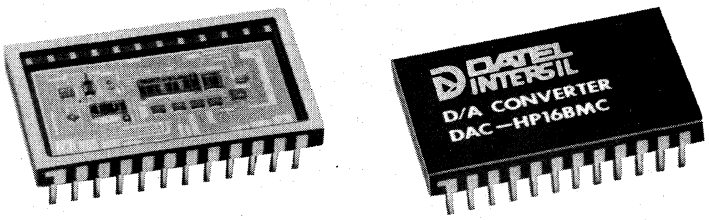
- 16 Bit Binary Model
- 4 Digit BCD Model
- Voltage Output
- 15ppm/°C max. Gain Tempco
- Linearity to ±0.003%

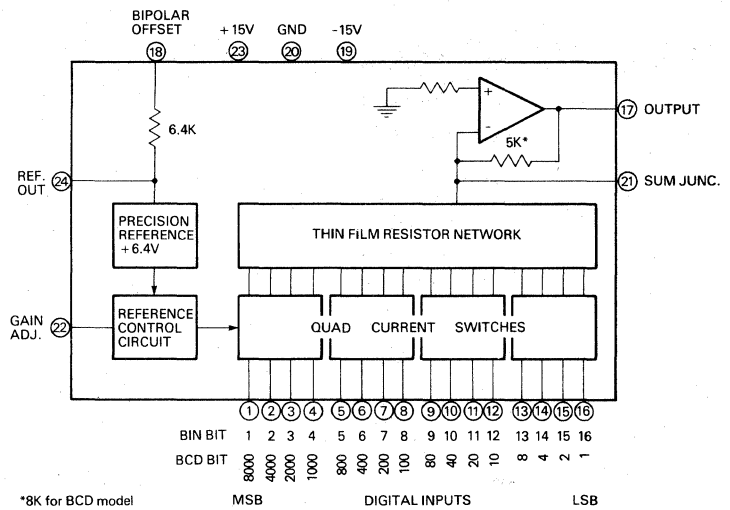
GENERAL DESCRIPTION

The DAC-HP series are high resolution hybrid D/A converters with voltage output. They are self-contained, including a low tempco zener reference circuit and output operational amplifier, all in a miniature 24 pin double spaced ceramic DIP package. There are two basic models in the series. The DAC-HP16B has 16 bit binary resolution with ±0.003% linearity while the DAC-HP16D has 4 digit BCD resolution with ±0.005% linearity. Input coding is complementary binary and complementary offset binary for the DAC-HP16B and complementary BCD for the DAC-HP16D. The binary version operates in both unipolar and bipolar modes with output voltages of 0 to +10V and ±5V respectively. Binary versions with a bipolar output voltage range of ±10V are available, denoted by the suffix "−1" after the model designation. The BCD version operates in the unipolar mode only with 0 to +10V output.

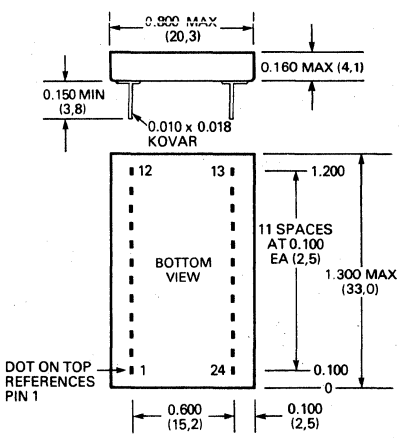
The DAC-HP design incorporates thin film hybrid technology which has been in volume production. Selected low tempco nichrome-on-silicon thin film resistor networks are combined with tightly matched quad current switches to achieve 16 bit resolution. The thin film resistors together with the low tempco zener reference circuit result in a maximum gain tempco of ± 15ppm/°C for the DAC. The thin film resistors are functionally laser trimmed for optimum converter linearity.

The resolution, stability, and voltage output of these converters make them ideal for precision applications such as speech and waveform reconstruction, precision ramp generators, and computer controlled testing. They are available in three operating temperature ranges: 0 to 70°C, −25 to +85°C, and −55 to +125°C. High reliability versions are also available under Datel Intersil's "S" program and MIL-STD-883 level B screening. Power requirement is ±15VDC.





MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN (MSB)	13	BIT 13 IN
2	BIT 2 IN	14	BIT 14 IN
3	BIT 3 IN	15	BIT 15 IN
4	BIT 4 IN	16	BIT 16 IN (LSB)
5	BIT 5 IN	17	OUTPUT
6	BIT 6 IN	18	BIPOLAR OFF.
7	BIT 7 IN	19	−15VDC
8	BIT 8 IN	20	GROUND
9	BIT 9 IN	21	SUM. JUNCTION
10	BIT 10 IN	22	GAIN ADJ.
11	BIT 11 IN	23	+15VDC
12	BIT 12 IN	24	REF. OUT

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SPECIFICATIONS, DAC-HP SERIES
(Typical at 25°C, and ±15 V supplies unless otherwise noted)

	DAC-HP16B (Binary)	DAC-HP16D (BCD)
MAXIMUM RATINGS		
Positive Supply, pin 23	+18V	*
Negative Supply, pin 19	−18V	*
Digital Input Voltage, pins 1-16	+5.5V	*
Output Current, pin 17	±20mA	*
INPUTS		
Resolution	16 bits	4 digits
Coding, unipolar output	Comp. Binary	Comp. BCD
Coding, bipolar output	Comp. Off. Binary	—
Input Logic Level, bit ON ("0")[1]	0V to +0.8V @ −1mA	
Input Logic Level, bit OFF ("1")[1]	+2.4V to +5.5V @ +40μA	
Logic Loading	1 TTL load	*
OUTPUT		
Output Voltage Range, Unipolar[2]	0 to +10V	*
Output Voltage Range, Bipolar	±5V	-
Output Voltage Range, "−1" Suffix	±10V	-
Output Current, min.[6]	±5 mA	0 to −5mA
Output Impedance	0.05 ohm	*
PERFORMANCE		
Linearity Error, max.	±0.003%	±0.005%
Monotonicity, 10°C to 40°C	14 bits	16 bits
Gain Error, before trimming	±0.1%	*
Zero Error, before trimming	±0.1%	*
Gain Tempco, max.[3]	±15ppm/°C	*
Gain Tempco, max. BGC, DGC	±20ppm/°C	*
Zero Tempco, unipolar, max.	±5ppm/°C of FSR[4]	*
Offset Tempco, bipolar, max.	±8ppm/°C of FSR[4]	—
Differential Linearity Tempco	±2ppm/°C of FSR[4]	*
Settling Time, 10V change[5]	15μsec.	15μsec.
Slew Rate	20V/μsec.	*
Power Supply Rejection	±0.002% FSR/%	*
POWER REQUIREMENT (Quiescent, all bits HI)	+15VDC at 38mA −15VDC at 38mA	
PHYSICAL-ENVIRONMENTAL		
Operating Temperature Range	0°C to 70°C (BMC, DMC, BGC, DGC) -25°C to +85°C (BMR, DMR) -55°C to +125°C (BMM, DMM)	
Storage Temperature Range	-65°C to +150°C	
Package Type	24 pin ceramic	
Pins	0.010 x 0.018 inch diameter Kovar	
Weight	0.2 oz. (6g.)	

*Specifications same as first column.

NOTES:
1. Drive from TTL output with only the DAC-HP as load.
2. Unipolar output range for suffix "—1" models, 0 to +10V, is reached at ½ scale input.
3. For all models except DAC-HP16BGC & DAC-16DGC.
4. FSR is 0 to +FS or -FS to +FS voltage.
5. To 0.005% FSR. 6 Pin 17

TECHNICAL NOTES

1. It is recommended that these converters be operated with local supply bypass capacitors of 1μF (tantalum type) at the +15V and −15V supply pins. The capacitors should be connected as close to the pins as possible. In high frequency noise environments an additional .01μF ceramic capacitor should be used in parallel with each tantalum bypass.
2. The analog, digital, and power grounds should be separated from each other as close as possible to pin 20 where they all must connect together.
3. The external gain adjustment shown in the diagrams gives an adjustment of ±0.2% of full scale range. The converters are internally trimmed to ±0.1% at full scale. A wider range of adjustment may be achieved by decreasing the value of the 510K ohm resistor.
4. The zero adjustment, or offset adjustment, has an adjustment range of ±0.35% of full scale range. The unipolar zero is internally set to zero within ±0.1% of full scale range.
5. If the reference output (pin 24) is used, it must be buffered by an operational amplifier in the noninverting mode. Current drawn from pin 24 should be limited to ±10μA in order that the temperature coefficient of the reference circuit not be affected. This is sufficient current for the bias current of most of the popular operational amplifier types.

ORDERING INFORMATION

MODEL	OPER. TEMP. RANGE	SEAL
DAC-HP16BGC	0 to 70C	EPOXY
DAC-HP16BMC	0 to 70C	HERM.
DAC-HP-16BMR	-25 to +85C	HERM.
DAC-HP16BMM	-55 to +125C	HERM.
DAC-HP16BMC-1	0 to 70C	HERM.
DAC-HP16BMR-1	-25 to +85C	HERM.
DAC-HP16BMM-1	-55 to +125C	HERM.
DAC-HP16DGC	0 to 70C	EPOXY
DAC-HP16DMC	0 to 70C	HERM.
DAC-HP16DMR	-25 to +85C	HERM.
DAC-HP16DMM	-55 to +125C	HERM.

Mating Socket: DILS-3 (24 pin socket)

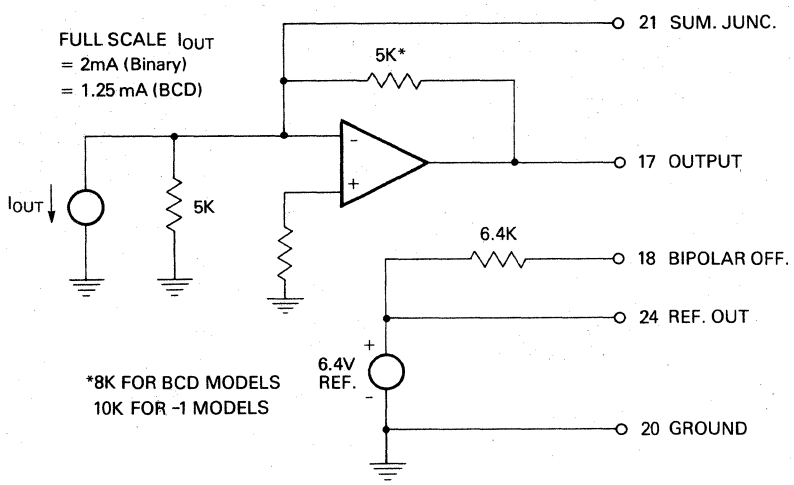
Trimming Potentiometer: TP50K

For high reliability versions of the DAC-HP series, including units screened to MIL-STD-883, Level B, contact factory.

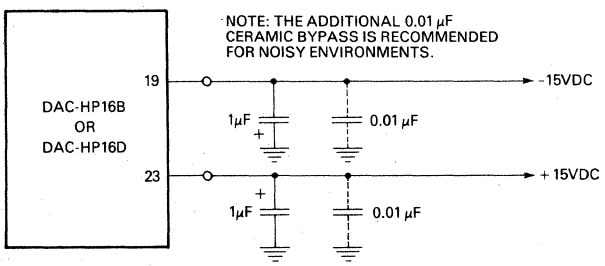
THESE CONVERTERS ARE COVERED BY GSA CONTRACT

APPLICATION

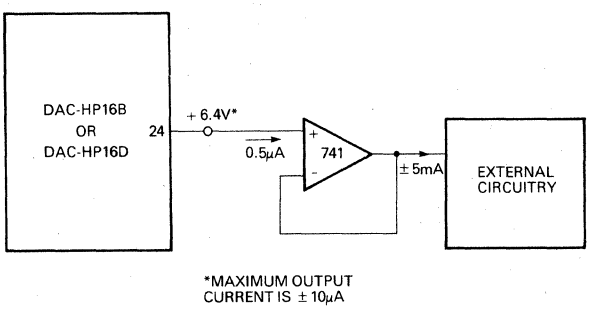
OUTPUT CIRCUIT



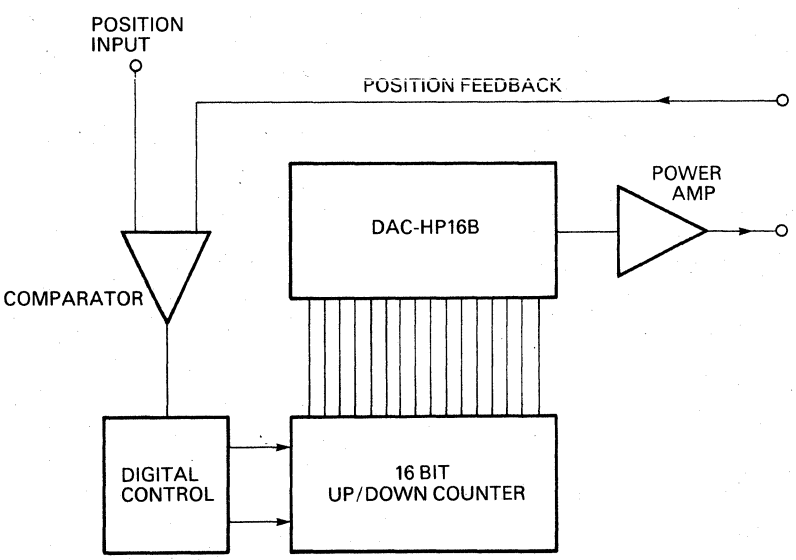
POWER SUPPLY BYPASSING



USE OF REFERENCE OUTPUT



PRECISION INDUSTRIAL POSITION CONTROLLER



CONNECTION AND CALIBRATION

CODING TABLES

BIPOLAR OUTPUT— Complementary Offset Binary

INPUT CODE MSB LSB	SCALE	OUTPUT VOLTAGE	OUTPUT VOLTAGE SUFFIX "−1" MODELS
0000 0000 0000 0000	+FS−1LSB	+4.99985V	+9.99969V
0011 1111 1111 1111	+½FS	+2.50000	+5.00000
0111 1111 1111 1111	0	0.00000	0.00000
1011 1111 1111 1111	−½FS	−2.50000	−5.00000
1111 1111 1111 1110	−FS+1LSB	−4.99985	−9.99969
1111 1111 1111 1111	−FS	−5.00000V	−10.00000V

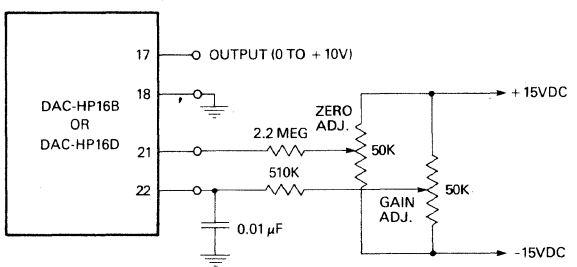
UNIPOLAR OUTPUT—Complementary BCD

INPUT CODE MSB LSB	SCALE	OUTPUT VOLTAGE
0110 0110 0110 0110	+FS−1LSB	+9.999V
1000 1010 1111 1111	+¾FS	+7.500
1010 1111 1111 1111	+½FS	+5.000
1101 1010 1111 1111	+¼FS	+2.500
1111 1111 1111 1110	+1LSB	+1.00mV
1111 1111 1111 1111	0	0

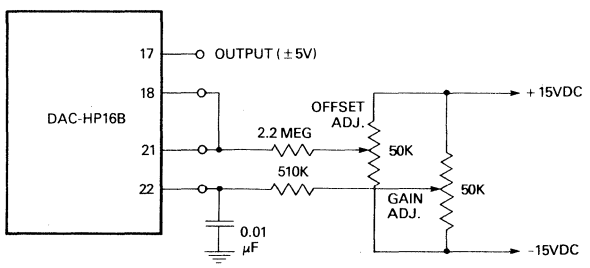
UNIPOLAR OUTPUT—Complementary Binary

INPUT CODE MSB LSB	SCALE	OUTPUT VOLTAGE
0000 0000 0000 0000	+FS−1LSB	+9.99985V
0011 1111 1111 1111	+¾FS	+7.50000
0111 1111 1111 1111	+½FS	+5.00000
1011 1111 1111 1111	+¼FS	+2.50000
1111 1111 1111 1110	+1LSB	+153μV
1111 1111 1111 1111	0	0

UNIPOLAR OPERATION



BIPOLAR OPERATION



CALIBRATION PROCEDURE

Connect the converter as shown in the application diagrams. For bipolar operation connect Bipolar Offset (pin 18) to Summing Junction (pin 21). For unipolar operation connect Bipolar Offset (pin 18) to Ground (pin 20). In making the following adjustments, refer to the coding tables.

UNIPOLAR OPERATION

1. **Zero Adjustment.** Set the input digital code to 1111 1111 1111 1111 and adjust the ZERO ADJ. potentiometer to give 0.00000V output.
2. **Gain Adjustment.** Set the input digital code to 0000 0000 0000 0000 (complementary binary) or 0110 0110 0110 0110 (complementary BCD) and adjust the GAIN ADJ. potentiometer to give +9.99985V output (complementary binary) or +9.999V output (complementary BCD).

BIPOLAR OPERATION

1. **Offset Adjustment.** Set the Digital Input Code to 1111 1111 1111 1111 and adjust the OFFSET ADJ. potentiometer to give the −F.S. output shown in the coding table above for the model being calibrated.
2. **Gain Adjustment.** Set the Digital Input Code to 0000 0000 0000 0000 and adjust the GAIN ADJ. potentiometer to give the +FS-1 LSB output shown in the coding table above for the model being calibrated.

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12 Bit Hybrid Digital-to-Analog Converters DAC-HZ Series

FEATURES

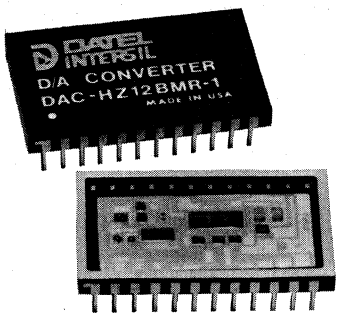
- 12 Bit Binary or 3 Digit BCD
- 5 Output Ranges
- 3 μSec. Settling Time
- Internal Ref. & Output Amp.
- High Performance

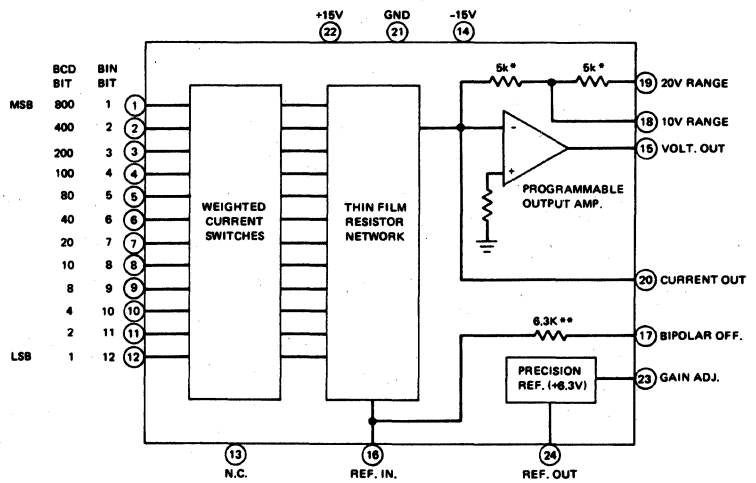
GENERAL DESCRIPTION

The DAC-HZ series are high performance, hybrid 12 bit binary and 3 digit BCD digital-to-analog converters. These converters are manufactured in volume in Datel Intersil's modern in-house thin film hybrid facility. They are complete and self-contained with a precision internal reference and fast output operational amplifier. Pin programmable output voltage ranges are provided for a high degree of application flexibility; the output voltage ranges are 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V with only unipolar ranges available on the BCD models. Current output is also provided.

The internal design utilizes three quad current switches, two thin film resistor networks, a precision zener reference circuit, reference control circuit and output amplifier. The thin film resistor networks are functionally trimmed with a laser to precisely set the binary weights of the current switches. The excellent tracking of the thin film resistors in conjunction with the tightly matched current switches results in a differential nonlinearity tempco of only 2ppm/°C. Temperature coefficient of gain is ±20ppm/°C max. and tempco of zero is ±5ppm/°C of FS max.

The DAC-Hz series consists of 8 different models covering the operating temperature ranges of 0°C to 70°C, −25°C to +85°C, and −55°C to +125°C. The models come in a 24-pin ceramic package. Power requirement is ±15 VDC at 35mA with no 5V logic supply required. Input coding is complementary binary or complementary BCD. Voltage output settling time is 3 μsec. to ½ LSB.

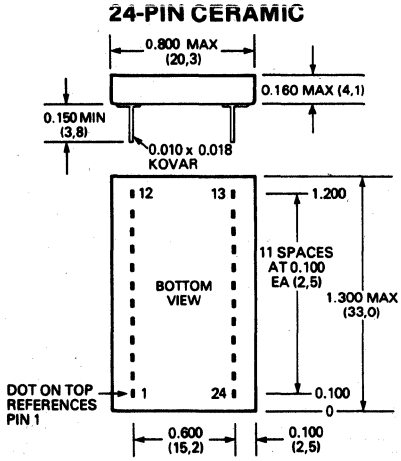




* For BCD model these resistors are 4KΩ.
** For BCD model this resistor is open circuit.

MECHANICAL DIMENSIONS INCHES (MM)

24-PIN CERAMIC



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN	13	NO CONN.
2	BIT 2 IN	14	-15VDC
3	BIT 3 IN	15	VOLT. OUT
4	BIT 4 IN	16	REF. IN
5	BIT 5 IN	17	BIPOLAR OFF.
6	BIT 6 IN	18	10V RANGE
7	BIT 7 IN	19	20V RANGE
8	BIT 8 IN	20	CURRENT OUT
9	BIT 9 IN	21	GROUND
10	BIT 10 IN	22	+15VDC
11	BIT 11 IN	23	GAIN ADJ.
12	BIT 12 IN	24	REF. OUT

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SPECIFICATIONS, DAC-HZ SERIES
(Typical at 25°C and ±15V supplies unless otherwise noted)

	DAC-HZ12B (Binary)	DAC-HZ12D (BCD)
INPUTS		
Resolution	12 Binary bits	3 BCD digits
Coding, unipolar output	Complementary Binary	Complementary BCD
Coding, bipolar output	Comp. Offset Bin.	–
Input Logic Level, bit ON ("0")	0V to +0.8V @ -1mA	
Input Logic Level, bit OFF ("1")	+2.4V to +5.5V @ +40μA	
Logic Loading	1 TTL load	
OUTPUTS		
Output Current, unipolar	0 to −2mA, ±10%	0 to −1.25mA, ±10%
Output Current, bipolar	±1mA, ±10%	–
Voltage Compliance, Iout	±2.5V	*
Output Impedance, Iout, unipolar	5K ohms	*
Output Impedance, Iout, bipolar	2.8K ohms	–
Output Voltage Ranges, unipolar	0V to +5V	0 to +2.5V
	0V to +10V	0 to +5V
		0 to +10V
Output Voltage Ranges, bipolar	±2.5V	–
	±5V	–
	±10V	–
Output Current, Vout	±5mA min.	*
Output Impedance, Vout	.05 ohm	*
PERFORMANCE, Voltage Output		
Nonlinearity	±1/2 LSB max.	±1/4 LSB max.
Differential Nonlinearity	±1/2 LSB max.	±1/4 LSB max.
Gain Error, before trimming	±0.1% of FSR[1]	*
Zero Error, before trimming	±0.1% of FSR[1]	*
Gain Tempco, max.	±20ppm/°C	*
Zero Tempco, unipolar, max.	±5ppm/°C of FSR[1]	*
Offset Tempco, biopolar, max.	±10ppm/°C of FSR[1]	*
Diff. Nonlinearity Tempco	±2ppm/°C of FSR[1]	*
Monotonicity	Over oper. temp. range	*
Settling Time, Iout to 1/2 LSB[2]	300nsec.	*
Settling Time, Vout to 1/2 LSB	3 μsec.[3]	*
Slew Rate	20V/μsec.	*
Power Supply Rejection	±.002% FSR/% Supply[1]	*
POWER REQUIREMENT		
Power Supply Voltage	±15VDC ±0.5V	
Quiescent Current	35mA	
PHYSICAL-ENVIRONMENTAL		
Operating Temperature Ranges	0°C to 70°C, −25°C to +85°C, and −55°C to +125°C	
Storage Temperature Range	-65°C to +150°C	
Package Size	1.300 x 0.800 x 0.160 inches	
Package Type	24 Pin Ceramic DIP	
Pins	Kovar 0.010 x 0.018 inches	
Weight	0.22 oz. (63 g.)	

*Specifications same as first column

1. FSR is full scale range and is 10V for 0 to +10V or −5V to +5V output; 20V for ±10V output, etc.
2. Current output mode.
3. For 2.5K or 5K feedback (2K or 4K, BCD). For 10K feedback (8K, BCD) the settling time is 4 μsec.

TECHNICAL NOTES

1. The DAC-HZ12 series converters are designed and factory calibrated to give ±½LSB linearity (binary version) and ±¼LSB linearity (BCD version) with respect to a straight line between end points. This means that if zero and full scale are exactly adjusted externally, the relative accuracy will be ±1/2 LSB (±1/4 LSB, BCD) everywhere over the full output range without any additional adjustments to achieve a best straight line fit. The linearity specification is therefore a conservative one since the user does not have to make more complicated adjustments for a best straight line fit.
2. The external zero or offset adjustment for the converters has a range of ±0.2% of full scale and the external gain adjustment has a range of ±0.3% of full scale.
3. These converters must be operated with local supply by-pass capacitors from +15V to ground and −15V to ground. Tantalum type capacitors of 1μF are recommended and should be mounted as close as possible to the converter. If the converters are used in a high frequency noise environment a .01μF ceramic capacitor should be used across each tantalum capacitor.
4. When operating in the current output mode the equivalent internal current source of 2mA (1.25mA, BCD) must drive both the internal source resistances and the external load resistor. A 300 nsec. output settling time is achieved for the voltage across a 100 ohm load resistor; for higher value resistors the settling time becomes longer due to the output capacitance of the converter. For fastest possible voltage output for a large transition, an external fast settling amplifier such as Datel-Intersil's AM-500 should be used in the inverting mode. Settling time of less than 1 μsec. can be achieved. See application diagram.

ORDERING INFORMATION

Model	Operating Temp. Range	Seal
DAC-HZ12BGC	0°C to +70°C	Epoxy
DAC-HZ12BMC	0°C to +70°C	Hermetic
DAC-HZ12BMR	-25°C to +85°C	Hermetic
DAC-HZ12BMM	-55°C to +125°C	Hermetic
DAC-HZ12DGC	0°C to +70°C	Epoxy
DAC-HZ12DMC	0°C to +70°C	Hermetic
DAC-HZ12DMR	-25°C to +85°C	Hermetic
DAC-HZ12DMM	-55°C to +125°C	Hermetic

Mating Socket: DILS-3 (24 pin socket)

Trimming Potentiometers: TP10K OR TP100K

For high reliability versions of the DAC-HZ series, including units screened to MIL-STD-883 level B, contact factory.

The DAC-HZ12 SERIES CONVERTERS ARE COVERED BY GSA CONTRACT.

INTERCONNECTIONS AND CALIBRATION

CALIBRATION PROCEDURE

1. Select the desired output range and connect the converter up as shown in the Output Range Selection table and the Standard Connection diagrams below.
2. To calibrate refer to the Coding Tables below. Note that complementary coding is used.
3. **Zero and Offset Adjustments**
   For unipolar operation set all digital inputs to "1" (+2.0 to +5.5V) and adjust the ZERO ADJ. potentiometer for zero output voltage or current. For bipolar operation (binary model only) set all digital inputs to "1" and adjust the OFFSET ADJ. potentiometer for the negative full scale (for voltage out) or positive full scale (for current out) output value shown in the Coding Table.
4. **Gain Adjustment**
   For the binary model set all digital inputs to "0" (0V to +0.8V) and adjust the GAIN ADJ. potentiometer for the positive full scale (for voltage out) or negative full scale (for current out) output value shown in the Coding Table.
   For the BCD model (unipolar only) set each BCD digit to 0110 and adjust the GAIN ADJ. potentiometer for the positive full scale (for voltage out) or negative full scale (for current out) output value shown in the Coding Table.

OUTPUT RANGE SELECTION

BIN RANGE	CONNECT THESE PINS TOGETHER			
±10V	15 & 19	17 & 20		16 & 24
±5V	15 & 18	17 & 20		16 & 24
±2.5V	15 & 18	17 & 20	19 & 20	16 & 24
+10V	15 & 18	17 & 21		16 & 24
+5V	15 & 18	17 & 21	19 & 20	16 & 24
±1mA		17 & 20		16 & 24
−2mA		17 & 21		16 & 24
BCD RANGE	**CONNECT THESE PINS TOGETHER**			
+10V	15 & 19	17 & 21		16 & 24
+5V	15 & 18	17 & 21		16 & 24
+2.5V	15 & 18	17 & 21	19 & 20	16 & 24
−1.25MA		17 & 21		16 & 24

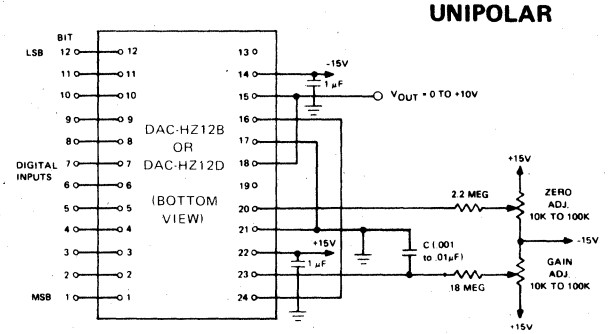
VOLTAGE OUTPUT IS AT PIN 15.
CURRENT OUTPUT IS AT PIN 20.

STANDARD CONNECTIONS

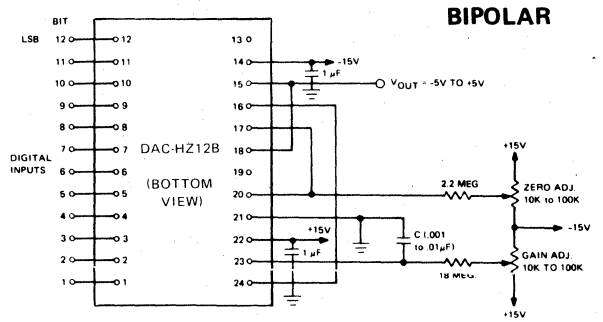
VOLTAGE OUTPUT CONNECTIONS

(FOR DIFFERENT OUTPUT SCALING REFER TO OUTPUT RANGE SELECTION TABLE)

UNIPOLAR

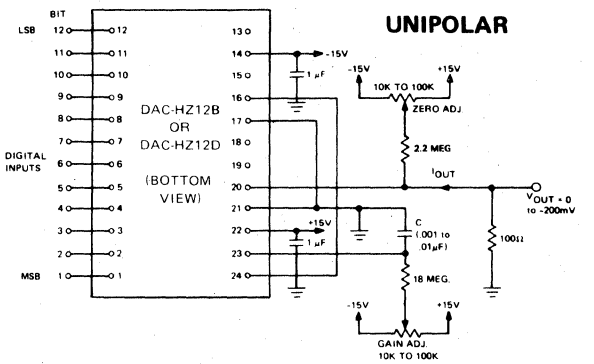


BIPOLAR

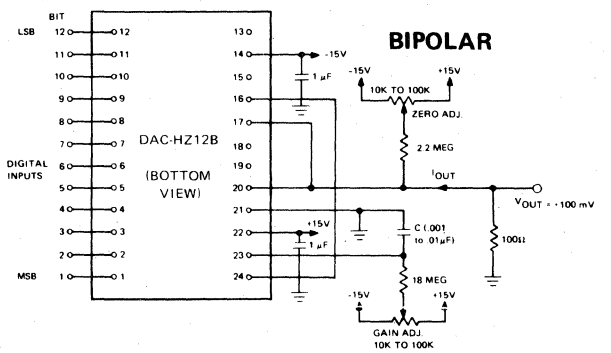


CURRENT OUTPUT CONNECTIONS

UNIPOLAR



BIPOLAR



CODING TABLES

UNIPOLAR OUTPUT – COMPLEMENTARY BINARY

BINARY INPUT CODE		UNIPOLAR OUTPUT RANGES		
MSB	LSB	0 TO +10V	0 TO +5V	0 TO -2MA
0000	0000 0000	+9.9976V	+4.9988V	-1.9995MA
0011	1111 1111	+7.5000	+3.7500	-1.5000
0111	1111 1111	+5.0000	+2.5000	-1.0000
1011	1111 1111	+2.5000	+1.2500	-0.5000
1111	1111 1110	+0.0024	+0.0012	-0.0005
1111	1111 1111	0.0000	0.0000	0.0000

UNIPOLAR OUTPUT – COMPLEMENTARY BCD

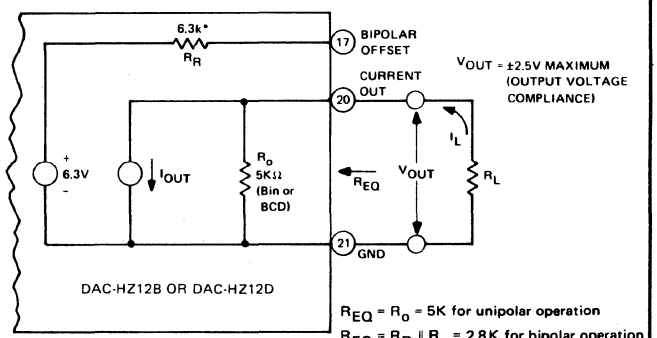
BCD INPUT CODE		UNIPOLAR OUTPUT RANGES			
MSD	LSD	0 TO +10V	0 TO +5V	0 TO +2.5V	0 TO -1.25MA
0110	0110 0110	+9.990V	+4.995V	+2.498V	-1.2488MA
1000	1010 1111	+7.500	+3.750	+1.875	-0.9375
1010	1111 1111	+5.000	+2.500	+1.250	-0.6250
1101	1010 1111	+2.5000	+1.250	+0.625	-0.3125
1111	1111 1110	+0.0100	+0.005	+0.003	-0.0013
1111	1111 1111	0.0000	0.000	0.000	0.0000

BIPOLAR OUTPUT – COMPLEMENTARY OFFSET BINARY

INPUT CODE		BIPOLAR OUTPUT RANGES			
MSB	LSB	±10V	±5V	±2.5V	±1MA
0000	0000 0000	+9.9951V	+4.9976V	+2.4988V	-0.9995MA
0011	1111 1111	+5.0000	+2.5000	+1.2500	-0.5000
0111	1111 1111	0.0000	0.0000	0.0000	0.0000
1011	1111 1111	-5.0000	-2.5000	-1.2500	+0.5000
1111	1111 1110	-9.9951	-4.9976	-2.4988	+0.9995
1111	1111 1111	-10.0000	-5.0000	-2.5000	+1.0000

EQUIVALENT CIRCUITS & APPLICATIONS

EQUIVALENT CURRENT MODE OUTPUT CIRCUIT



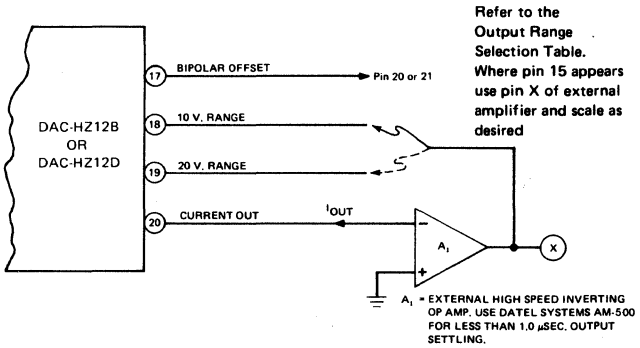
*Open circuit in DAC-HZ12D

$R_{EQ} = R_o = 5K$ for unipolar operation

$R_{EQ} = R_R \parallel R_o = 2.8K$ for bipolar operation

I_{OUT} = 2mA binary
= 1.25mA BCD

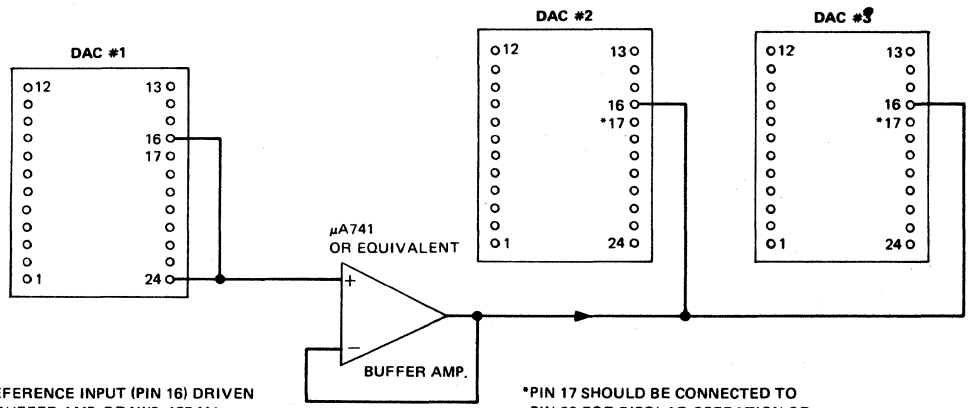
USE OF HIGH SPEED EXTERNAL OP AMP FOR FASTER SETTLING



Refer to the Output Range Selection Table. Where pin 15 appears use pin X of external amplifier and scale as desired

A_1 = EXTERNAL HIGH SPEED INVERTING OP AMP. USE DATEL SYSTEMS AM-500 FOR LESS THAN 1.0 μSEC. OUTPUT SETTLING.

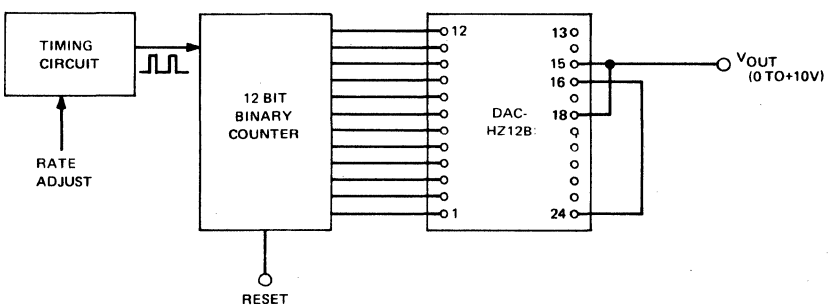
USE OF A SINGLE BUFFERED REFERENCE IN A MULTI-DAC SYSTEM FOR IMPROVED TEMPERATURE TRACKING

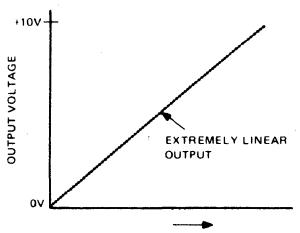


EACH REFERENCE INPUT (PIN 16) DRIVEN BY THE BUFFER AMP. DRAWS .125 MA IN UNIPOLAR OPERATION AND 1.125 MA IN BIPOLAR OPERATION.

*PIN 17 SHOULD BE CONNECTED TO PIN 20 FOR BIPOLAR OPERATION OR LEFT OPEN FOR UNIPOLAR OPERATION OF DAC'S #2 AND #3.

PRECISION, LOW COST BASE LINE RAMP GENERATOR





THIS CIRCUIT DEVELOPS A HIGHLY LINEAR (.01%) OUTPUT VOLTAGE RAMP FROM 0 TO +10V. THE RAMP CAN BE MADE AS SLOW AS DESIRED WITHOUT AFFECTING LINEARITY BY SETTING THE PULSE RATE OF THE TIMING CIRCUIT TO THE PROPER VALUE. THE OUTPUT RAMP IS GENERATED IN DISCRETE STEPS OF .024% FS (4096 STEPS FOR FS CHANGE).

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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
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Fast, 12-Bit Deglitched Digital-to-Analog Converter Model DAC-DG12B

FEATURES

- **±2 LSB Max. Glitch**
- **600 nsec. Settling Time**
- **Up to 2.5 MHz Update Rate**
- **12 Bit Resolution**
- **Self-Contained Module**

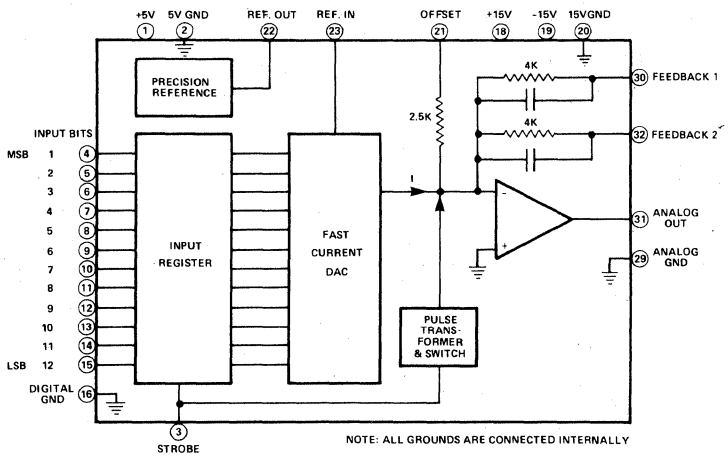
GENERAL DESCRIPTION

Model DAC-DG12B is a deglitched 12-bit D/A converter with a fast voltage output. The maximum output glitch amplitude is ±2 LSB's while settling time for a 10 volt output change is 600 nsec. to 1 LSB. For a 10 volt change to 1% the settling time is 250 nsec., and for small output changes it is only 400 nsec., permitting update rates as fast as 2.5 MHz.

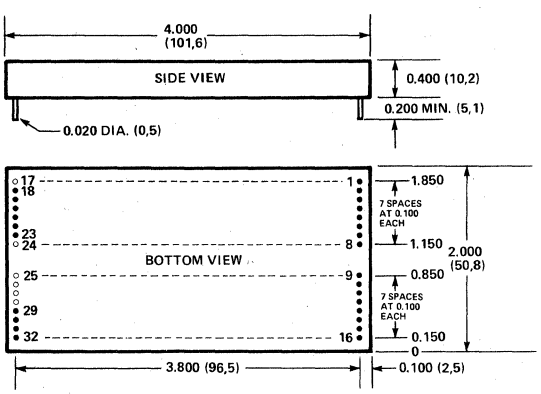
The unique circuit design of the DAC-DG12B realizes both small size and low price at the same time. Unlike other deglitched DAC's which are comprised of several inter-connected modules mounted on a circuit card, the DAC-DG12B is completely self-contained in a compact 4 x 2 x 0.4 inch (102 x 51 x 10 mm) module. It consists of several optimized circuit functions: digital input register, ultra-fast 12-bit current DAC, stable Zener voltage reference, fast deglitching switch, and a fast output operational amplifier.

The DAC-DG12B has three voltage output ranges determined by external pin connection: 0 to −10 V, ±5V and ±10 V. Output current is ±10 mA with output short circuit protection; for higher output current requirements an external current booster amplifier may be connected inside the feedback loop of the output amplifier. There are two input coding options: complementary binary complementary offset binary or complementary two's complement.

The DAC-DG12B is an ideal device for fast CRT display applications and for other test and measurement applications where monotonic output changes are required.



MECHANICAL DIMENSIONS—INCHES (MM)



NOTE: OPEN HOLES DESIGNATE OMITTED PINS

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	+5 V POWER
2	5 V GND
3	STROBE
4	BIT 1 IN (MSB)
5	BIT 2 IN
6	BIT 3 IN
7	BIT 4 IN
8	BIT 5 IN
9	BIT 6 IN
10	BIT 7 IN
11	BIT 8 IN
12	BIT 9 IN
13	BIT 10 IN
14	BIT 11 IN
15	BIT 12 IN (LSB)
16	DIGITAL GND
18	+15 V POWER
19	−15 V POWER
20	15 V GND
21	OFFSET
22	REF. OUT
23	REF. IN
29	ANALOG GND
30	FEEDBACK 1
31	ANALOG OUT
32	FEEDBACK 2

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, DAC-DG12B
(Typical at 25° C, ±15 V and +5 V supplies unless otherwise noted)

INPUTS

Resolution	12 bits
Coding, unipolar	Complementary Binary
Coding, bipolar	Complementary Offset Binary [1] Complementary Two's Comp.[1]
Input Logic Level, bit ON ("0")	0V to +0.8 V
Input Logic Level, bit OFF ("1")	+2.0 V to +5.5 V
Logic Loading	1 TTL load
Input Strobe Pulse[2]	HI to LO transition causes transfer of data from register to DAC.
Input Strobe Loading	2 TTL loads

OUTPUTS

Output Voltage, unipolar[3]	0 to −10 V
Output Voltage, bipolar[3]	±5 V, ±10 V
Output Current, S.C. protected	±20 mA typ., ±10 mA min.
Output Impedance, DC	0.05 ohm

PERFORMANCE

Linearity Error	±½ LSB max.
Differential Nonlinearity	±½ LSB max.
Zero Error, before trimming	±½ LSB max.
Gain Tempco	±35 ppm/° C max.
Offset Tempco, bipolar	±15 ppm/° C max.
Zero Tempco, unipolar	±5 ppm/° C of FS max.
Diff. Nonlinearity Tempco	±2 ppm/° C of FS
Monotonicity	0° C to 70° C
Settling Time, 10 V change to 1 LSB	600 nsec. typ., 700 nsec. max.
Settling Time, 20 V change to 1 LSB	1.0 μsec. typ., 1.2 μsec. max.
Settling Time, 10 V change to 1%	250 nsec. max.
Settling Time, 20 V change to 1%	550 nsec. max.
Settling Time, ±4 LSB change[5]	400 nsec.
Slew Rate	50 V/μsec.
Glitch Amplitude[4]	±1 LSB typ., ±2 LSB max.
Glitch Area	250 mV-nsec.
Power Supply Rejection	0.01%/% supply

POWER REQUIREMENT	+15 VDC ±0.5 V @ 50 mA −15 VDC ±0.5 V @ 35 mA + 5 VDC ±0.25 V @ 230 mA

PHYSICAL-ENVIRONMENTAL

Operating Temperature Range	0° C to 70° C
Storage Temperature Range	−55° C to +125° C
Case Size	4 x 2 x 0.4 inches (101,6 x 50,8 x 10,2 mm)
Case Material	Black Diallyl Phthalate per MIL-M-14
Pins	0.020" round, gold plated, 0.200 lg. min.
Weight	4 oz. max. (114 g)

NOTES

1. Because the analog output is inverted, in the bipolar mode the complementary offset binary code is equivalent to offset binary and the complementary two's complement code is equivalent to two's complement. See Technical Note 4.
2. Has same logic levels as data inputs.
3. Determined by external pin connection.
4. Measured with 20 MHz bandwidth oscilloscope at major carry (half scale) and at 7 transitions either side of major carry.
5. See Technical Note 7.

TECHNICAL NOTES

1. The sequence of operations inside the DAC-DG12B after the input strobe changes from HI to LO are:
   a. the pulse transformer and switch are activated and turn ON
   b. within 11 nanoseconds (typically) the data in the input register is transferred to the current DAC
   c. during the next 19 nanoseconds (typically) the DAC output current changes
   d. after 30 nanoseconds (typically) from the strobe change the pulse transformer and switch are deactivated, turning OFF
   e. the output amplifier begins to change to its new output value
2. A 5 nanosecond minimum setup time is required for the input data to be valid before the input strobe goes from HI to LO. The input strobe then should not go HI again for at least 40 nanoseconds.
3. The maximum update rate for the DAC-DG12B is 2.5 MHz, based on the 400 nanosecond settling time for small output changes (±4 LSB's max.). For 10 V changes to 1% of final value the maximum update rate is 4 MHz and for 10 V changes to within 1 LSB of final value the maximum update rate is 1.6 MHz.
4. From the coding tables it should be noted that each model of the DAC-DG12B has its coding defined in two ways when operating in bipolar mode. For the DAC-DG12B1 the complementary offset binary coding with inverted (negative) analog output is the same as offset binary coding with noninverted (positive) analog output except for an analog shift of 1 LSB. The converter therefore can be externally calibrated for either code. For the DAC-DG12B2 the complementary two's complement coding with inverted (negative) analog output is the same as two's complement coding with noninverted (positive) analog output except for an analog shift of 1 LSB.
5. The DAC-DG12B is internally calibrated at zero for unipolar operation, with a zero error of ±½ LSB maximum. In many applications, therefore, no external zero adjustment is required. For exact calibration the external zero adjustment should be used. The DAC-DG12B2 operates in unipolar mode except that its input code is complementary binary with the MSB inverted.
6. For higher output current drive capability a wideband current booster amplifier with unity voltage gain may be enclosed inside the feedback loop of the output amplifier.
7. The DAC-DG12B can be updated at up to 10 MHz with partial settling. This mode can be useful in some applications such as fast CRT displays. The DAC's output is integrated by the CRT deflection amplifier, resulting in a continuous, monotonic deflection signal that is offset by a small amount from its theoretical value. This small offset is the sole effect of the D/A's partial settling.

ORDERING INFORMATION

MODEL	CODING
DAC-DG12B1	Comp. Binary/Comp. Offset Binary
DAC-DG12B2	Comp. Two's Complement

Mating Socket: DILS-2, 2 Req'd Per Unit
Trimming Potentiometers: TP100 (100Ω), TP10K (10KΩ)

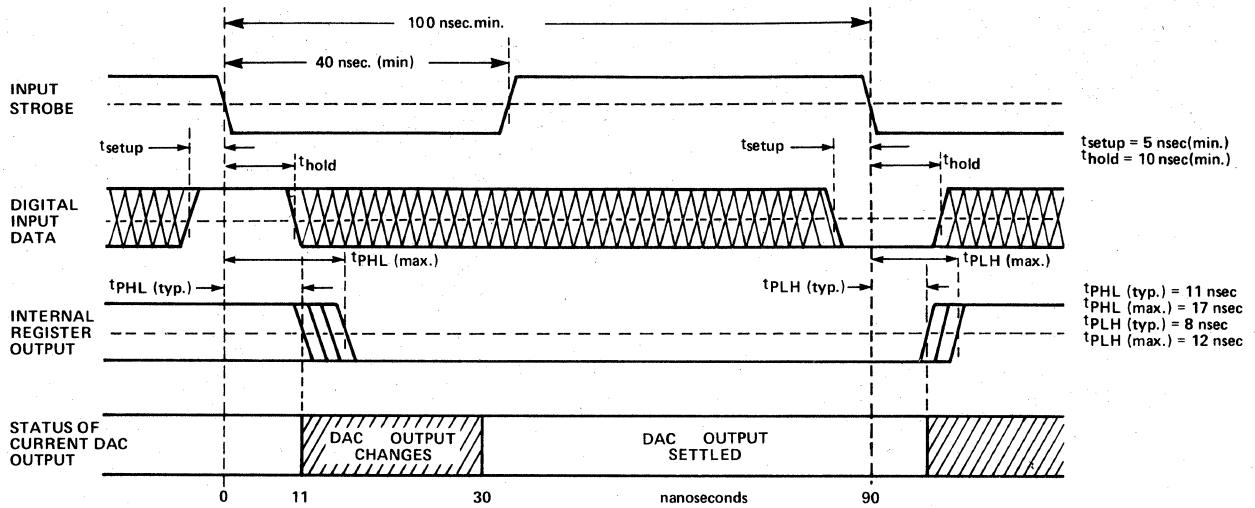
For extended temperature range operation, the following suffixes are added to the model number. Consult factory for pricing.

−EX	−25°C to +85°C Operation
−EXX-HS	−55°C to +85°C Operation with Hermetically sealed semiconductor components

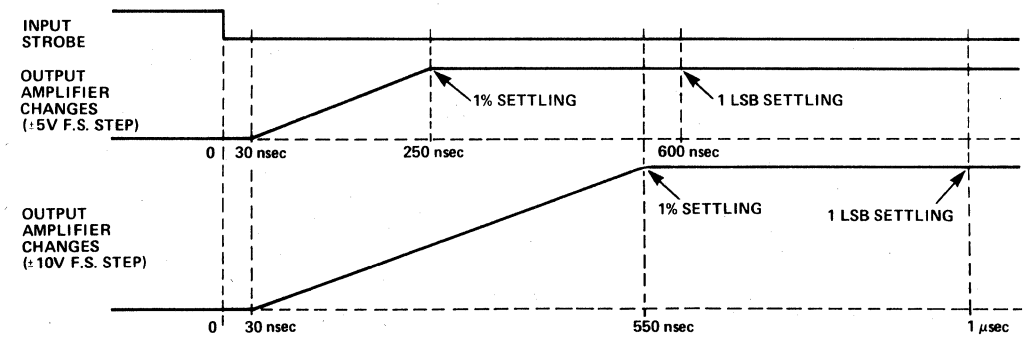
THE DAC-DG12B IS COVERED BY GSA CONTRACT

TIMING DIAGRAMS

INTERNAL TIMING



EXTERNAL TIMING



CODING TABLES

UNIPOLAR OPERATION

SCALE	VOLTAGE RANGE	DAC-DG12B1
	0 TO −10 V	COMP. BINARY
0	0.0000	1111 1111 1111
0-1 LSB	−0.0024	1111 1111 1110
−¼FS	−2.5000	1011 1111 1111
−½FS	−5.0000	0111 1111 1111
−¾FS	−7.5000	0011 1111 1111
−FS + 1 LSB	−9.9976	0000 0000 0000

BIPOLAR OPERATION

SCALE	VOLTAGE RANGE		DAC-DAC-DG12B1		DAC-DG12B2	
	±5 V	±10 V	COMP. OFFS. BIN	OFFSET BINARY	COMP. 2's COMP.	2'S COMPLEMENT
+FS	+5.0000 V	+10.0000 V	1111 1111 1111		0111 1111 1111	
+FS-1 LSB	+4.9976	+9.9951	1111 1111 1110	1111 1111 1111	0111 1111 1110	0111 1111 1111
0 + 1 LSB	+0.0024	+0.0049	1000 0000 0000	1000 0000 0001	0000 0000 0000	0000 0000 0001
0	0.0000	0.0000	0111 1111 1111	1000 0000 0000	1111 1111 1111	0000 0000 0000
−FS + 1 LSB	−4.9976	9.9951	0000 0000 0000	0000 0000 0001	1000 0000 0000	1000 0000 0001
−FS	−5.0000	−10.000		0000 0000 0000		1000 0000 0000

CONNECTIONS AND CALIBRATION

CALIBRATION PROCEDURE

Select the desired output voltage range (0 to −10 V, ±5 V, or ±10 V) and make the connections shown in the diagrams below. To calibrate refer to the coding tables on the previous page.

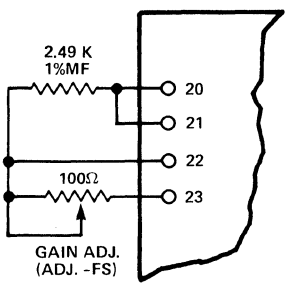
UNIPOLAR OPERATION (0 TO −10 V OUTPUT)

1. **Zero Adjustment:** Set the digital input code to 1111 1111 1111 and adjust the ZERO ADJ. potentiometer to give 0.0000 V output.
2. **Gain Adjustment:** Set the digital input code to 0000 0000 0000 and adjust the GAIN ADJ. potentiometer to give −9.9976 V output.

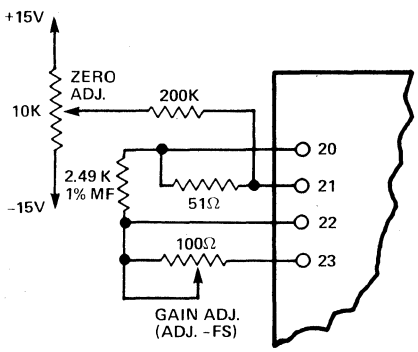
BIPOLAR OPERATION (±5 V OR ±10 V OUTPUT)

1. **Offset Adjustment:** Set the digital input code to 0111 1111 1111 (comp. offset binary), 1000 0000 0000 (offset binary), 1111 1111 1111 (comp. two's complement), or 0000 0000 0000 (two's complement) and adjust the BIPOLAR OFFSET ADJ. potentiometer to give 0.0000 V output.
2. **Gain Adjustment:** Set the digital input code to 0000 0000 0000 (comp. offset binary), 0000 0000 0001 (offset binary), 1000 0000 0000 (comp. two's complement), or 1000 0000 0001 (two's complement) and adjust the GAIN ADJ. potentiometer to give −4.9976 V output (for ±5 V range) or −9.9951 V output (for ±10 V range).
3. Repeat steps 1 and 2 to recheck adjustments.

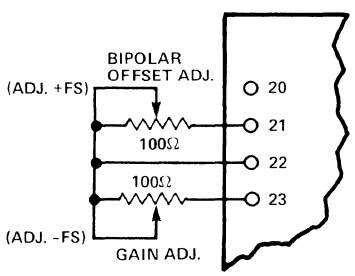
UNIPOLAR OPERATION—NO ZERO ADJ.



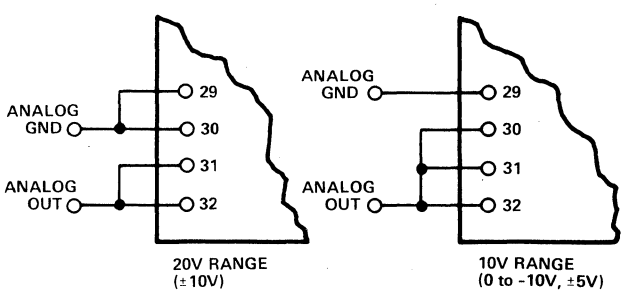
UNIPOLAR OPERATION—WITH ZERO ADJ.



BIPOLAR OPERATION



OUTPUT CONNECTIONS



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Ultra-Fast Settling Digital-to-Analog Converters DAC-HI Series

FEATURES

- **Settling to 25 nsec**
- **8, 10 or 12 Bit Resolution**
- **Unipolar or Bipolar Operation**
- **5 mA Current Output**
- **20 ppm/°C Gain Tempco**

GENERAL DESCRIPTION

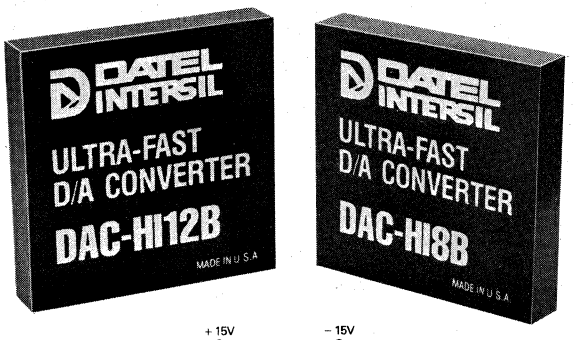
The DAC-HI series devices are ultra high speed, current output, modular D/A converters offering state of the art performance in a compact plug-in module. Full scale output transitions settle in only 25 nsec. max. with the 8 and 10 bit units and in 50 nsec. max. with the 12 bit model. Speed is attained without sacrificing accuracy or stability; linearity is guaranteed to ±½LSB and the gain temperature coefficient is only ±20 ppm/°C max.

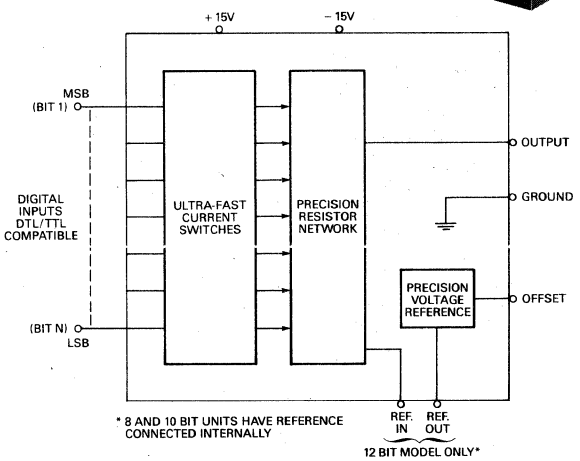
Input coding is straight binary for unipolar output and offset binary for bipolar output. These units may be used in the bipolar mode with two's complement coding by externally inverting the MSB.

One of the prime features of the DAC-HI series is output flexibility. The 5 mA current output can be fed directly into an external resistor to develop a +1.2V maximum output or, by external pin strapping, a bipolar output of ±1.2V maximum can be generated across the resistor. For applications requiring greater voltage ranges or sign inversion, the output current drives an external operational amplifier. When the amplifier is Datel's AM-500, a 20V output step will typically settle in 300 nsec.

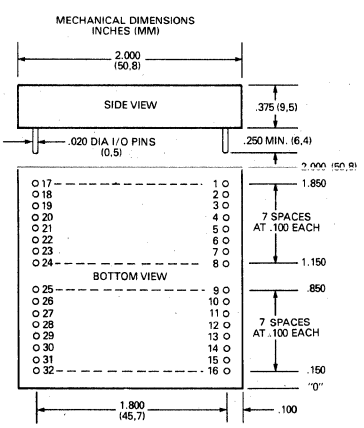
These DAC's are completely self-contained, requiring only ±15 VDC supplies. Each unit is packaged in a 2″ × 2″ × 0.375″, low profile module; internal circuitry consists of digital interface logic, a precision resistor network, high speed electronic switches and a temperature compensated precision voltage reference source.

The combination of speed, accuracy, stability, and a choice of resolutions allow the DAC-HI series converters to meet a broad range of requirements. Applications for these devices include high speed graphic generators, CRT displays, high speed function generators and high speed computer control systems.





MECHANICAL DIMENSIONS



NOTES
NUMBERS DESIGNATE ALLOWABLE PIN POSITIONS. ONLY PINS SPECIFIED IN INPUT/OUTPUT CONNECTIONS TABLE ARE ACTUALLY PRESENT

INPUT/OUTPUT CONNECTIONS 8 AND 10 BIT MODELS

PIN	FUNCTION	PIN	FUNCTION
6	BIT 1 IN	14*	BIT 9 IN
7	BIT 2 IN	15*	BIT 10 IN
8	BIT 3 IN	18	+15 V POWER
9	BIT 4 IN	19	−15 V POWER
10	BIT 5 IN	20	GROUND
11	BIT 6 IN	21	OFFSET
12	BIT 7 IN	22	OUTPUT
13	BIT 8 IN	31	N.C.

*These Pins Omitted on 8 Bit Model

12 BIT MODEL

PIN	FUNCTION	PIN	FUNCTION
4	BIT 1 IN	14	BIT 11 IN
5	BIT 2 IN	15	BIT 12 IN
6	BIT 3 IN	18	+15 V POWER
7	BIT 4 IN	19	−15 V POWER
8	BIT 5 IN	20	GROUND
9	BIT 6 IN	21	OFFSET
10	BIT 7 IN	22	OUTPUT
11	BIT 8 IN	30	REFERENCE OUT
12	BIT 9 IN	31	REFERENCE IN
13	BIT 10 IN		

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, DAC-HI SERIES
(Typical at 25°C, ±15V supplies unless otherwise noted)

	8B	10B	12B
INPUTS			
Resolution, Bits	8	10	12
Coding, Unipolar Output	Straight Binary		
Coding, Bipolar Output	Offset Binary or Two's Complement		
Input Logic Level, Bit ON ("1")	+2.0V to +5.5V		
Input Logic Level, Bit OFF ("0")	0V to +0.8V		
Logic Loading	2 TTL Loads		
OUTPUTS			
Output Current Range, Unipolar	0 to +5 mA		
Output Current Range, Bipolar	±2.5 mA		
Output Voltage Compliance	±1.2V max.		
Output Impedance	600 ohms ±1%		
Output Zero Offset	15 nA		
PERFORMANCE			
Linearity Error, max.	±½ LSB		
Differential Linearity Error, max.	±½ LSB		
Differential Linearity Tempco	±2.7 ppm/°C of FSR[3], max.		
Monotonicity	Over Oper. Temp. Range		
Gain Tempco, ppm/°C of FSR[3] max.	±20		
Bipolar Offset Tempco ppm/°C of FSR[3] max.	±10		
Zero Tempco, ppm/°C of FSR[3] max.	±1.5		
Settling Time, nsec. max.[2]	25	25	50
Long Term Stability	±0.5%/yr.		
Power Supply Sens., % of FSR[3]/V	0.05	0.05	0.0085
POWER REQUIREMENT			
Positive Supply	+15V ±0.5V		
Positive Supply Current, mA max.	75	75	40
Negative Supply	−15V ±0.5V @ 20 mA max.		
Negative Supply Current, mA max.	20		
PHYSICAL-ENVIRONMENTAL			
Operating Temperature Range	0°C to +70°C		
Storage Temperature Range	−55°C to +85°C		
Relative Humidity	Up to 100% Non-Condensing		
Package Size	2 + 2 + 0.375 inches 50,8 + 50,8 + 9,5 mm		
Pins	0.020" Round, Gold Plated 0.250" Long, min.		
Weight	2 oz. max (57g)		

NOTES:
1. For two's complement coding, the MSB of the input code must be externally inverted.
2. Full scale output change to 1 LSB.
3. FSR is Full Scale Range, the difference between minimum maximum output.

TECHNICAL NOTES

1. Proper operation of the DAC-HI series converters is dependent on good board layout and connection practices.

2. Use of a ground plane is particularly important in high speed D/A converters as it reduces high frequency noise and aids in decoupling the digital inputs from the analog output. Ground loop problems are avoided by connecting all grounds on the board to the ground plane. The ground plane should pass beneath the converter and include as much of the circuit board as possible.

3. The high speed current switching technique used in the DAC-HI series inherently reduces the amplitude and duration of large transient spikes at the output ("glitches"). The most severe glitches occur at half-scale, the major carry transition from 011...1 to 100...0 or vice versa. At this time a skewing of the input codes can create a transition state code of 111...1. The duration of the "transition state code" is dependent on the degree of skewing, but its effect is dependent on the speed of the DAC (an ultra-fast DAC will respond to these brief spurious inputs to a greater degree than a slow DAC). The effects of input skewing can be easily minimized through the use of a high-speed input register to match input switching times. The input register recommended for use with the DAC-HI is easily implemented with two Texas Instruments SN74S174 hex D-type flip-flops. This register will minimize skewing-induced glitches to a very low level and ensure fast output settling times.

4. When the converter is configured for voltage output with an external op amp the leads from the converter to the output amplifier should be kept as short as possible.

5. Testing of the DAC-HI should be performed with a low capacitance test probe (such as a 10X probe). Care should be taken to assure the shortest possible connection between the probe ground and circuit ground. Long probe leads may pick up environmental E.M.I. causing artifacts on the scope display, i.e., signals that do not originate at the unit under test.

6. Power supply inputs on the DAC-HI series are bypassed internally with 1 μF capacitors. For use in particularly noisy environments a 0.1 μF ceramic capacitor should be added between each supply input and ground.

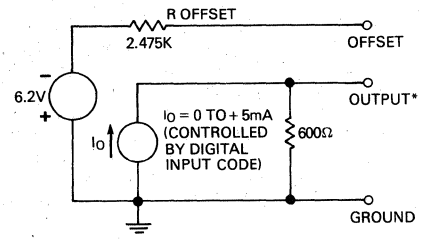
7. Values given for R_{LOAD}, R_F and R are nominal values only. These values should be approximated as closely as possible with 0.1% 10 ppm/°C metal film resistors and trimmed, if necessary, with a small value series carbon composition resistor.

8. These converters may be operated with two's complement input coding by externally inverting the MSB.

9. The DAC-HI series modules are fully repairable.

APPLICATIONS INFORMATION

EQUIVALENT OUTPUT CIRCUIT



*OUTPUT VOLTAGE LIMITED TO ±1.2V max.

OUTPUT AMPLIFIER RESISTOR TABLE

OUTPUT RANGE	R_F*	R*
0 to −5V ±2.5V	1KΩ	375Ω
0 to −10V ±5V	2KΩ	462Ω
±10V	4KΩ	522Ω

*Nominal values, see Tech. Note 7.

ORDERING INFORMATION

MODEL	DESCRIPTION
DAC-HI8B	8 Bits, 25 nsec.
DAC-HI10B	10 Bits, 25 nsec.
DAC-HI12B	12 Bits, 50 nsec.

Mating Socket DILS-2, 2 Per Unit
Trimming Potentiometers: TP100 or TP500

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

CODING TABLES

8 BIT MODEL

OUTPUT MODE	DIGITAL INPUT CODING	OUTPUT VOLTAGE RANGE			
UNIPOLAR	STRAIGHT BINARY	0 TO +1V	0 TO −5V*	0 TO −10V*	
F.S. - 1 LSB	1111 1111	+0.9961V	−4.9805V	−9.9609V	
½ F.S.	1000 0000	+0.5000V	−2.5000V	−5.0000V	
1 LSB	0000 0001	+0.00391V	−0.01953V	−0.03906V	
0	0000 0000	0.0000V	0.0000V	0.0000V	
BIPOLAR	OFFSET BINARY	±1V	±2.5V*	±5V*	±10V*
+F.S. − 1 LSB	1111 1111	+0.9922V	−2.4805V	−4.9609V	−9.9219V
+1 LSB	1000 0001	+0.00781V	−0.01953V	−0.03906V	−0.07813V
0	1000 0000	0.0000V	0.0000V	0.0000V	0.0000V
−F.S. +1 LSB	0000 0001	−0.9922V	+2.4805V	+4.9609V	+9.9219V
−F.S.	0000 0000	−1.0000V	+2.5000V	+5.0000V	+10.0000V

*With External Output Amplifier

10 BIT MODEL

OUTPUT MODE	DIGITAL INPUT CODING	OUTPUT VOLTAGE RANGE			
UNIPOLAR	STRAIGHT BINARY	0 TO +1V	0 TO −5V*	0 TO −10V*	
F.S. - 1 LSB	11111 11111	+0.9990V	−4.9951V	−9.9902V	
½ F.S.	10000 00000	+0.5000V	−2.5000V	−5.0000V	
1 LSB	00000 00001	+0.00097V	−0.00488V	−0.00977V	
0	00000 00000	0.0000V	0.0000V	0.0000V	
BIPOLAR	OFFSET BINARY	±1V	±2.5V*	±5V	±10V*
+FS - 1 LSB	11111 11111	+0.9980V	−2.4951V	−4.9902V	−9.9805V
+1 LSB	10000 00001	+0.00195V	−0.00488V	−0.00977V	−0.01953V
0	10000 00000	0.0000V	0.0000V	0.0000V	0.0000V
−FS + 1 LSB	00000 00001	−0.9980V	+2.4951V	+4.9902V	+9.9805V
−F.S.	00000 00000	−1.0000V	+2.5000V	+5.0000V	+10.0000V

*With External Output Amplifier

12 BIT MODEL

OUTPUT MODE	DIGITAL INPUT CODING	OUTPUT VOLTAGE RANGE			
UNIPOLAR	STRAIGHT BINARY	0 TO +1V	0 TO −5V*	0 TO −10V*	
F.S. - 1 LSB	1111 1111 1111	+0.9998V	−4.9988V	−9.9976V	
½F.S.	1000 0000 0000	+0.5000V	−2.5000V	−5.0000V	
1 LSB	0000 0000 0001	+0.00024V	−0.00122V	−0.00244V	
0	0000 0000 0000	0.0000V	0.0000V	0.0000V	
BIPOLAR	OFFSET BINARY	3±1V	±2.5V*	±5V*	±10V*
+FS - 1 LSB	1111 1111 1111	+0.9995V	−2.4988V	−4.9976V	−9.9951V
+1 LSB	1000 0000 0001	+0.00049V	−0.00122V	−0.00244V	−0.00488V
0	1000 0000 0000	0.0000V	0.0000V	0.0000V	0.0000V
−F.S. +1 LSB	0000 0000 0001	−0.9995V	+2.4988V	+4.9976V	+9.9951V
−F.S.	0000 0000 0000	−1.0000V	+2.5000V	+5.0000V	+10.0000V

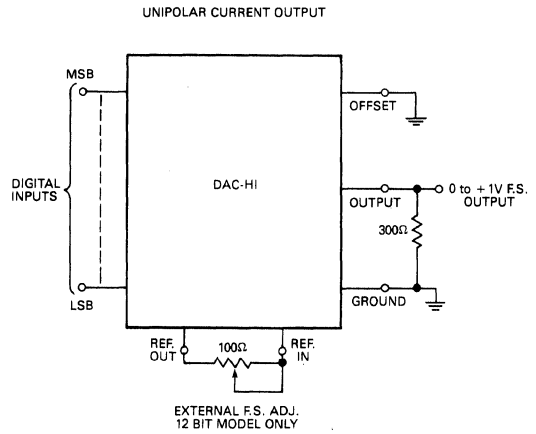
*With External Output Amplifier

CONNECTIONS TABLE

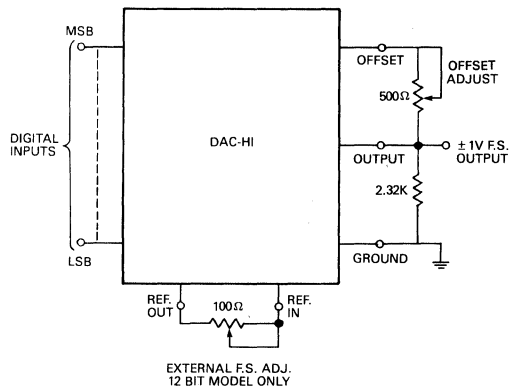
OUTPUT VOLTAGE RANGE	8 AND 10 BIT MODELS	12 BIT MODEL
0 TO +1V	Connect 300Ω load resistor between pin 13 and pin 15 Ground pin 14	Connect 300Ω load resistor between pin 17 and pin 15, connect 100Ω trim pot between pin 18 and pin 19. Ground pin 16
±1V	Connect 2.32 KΩ load resistor between pin 13 and pin 15. Connect 500Ω trim pot between pin 14 and pin 15	Connect 2.32 KΩ between pin 17 and pin 15, connect 500Ω trim pot. between pin 16 and pin 17. Connect 100Ω trim pot between pin 18 and pin 19.
0 TO −5V 0 TO − 10V	Connect pin 13 to pin 14 Connect external op amp as shown in diagram.	Connect pin 15 to pin 16. Connect 100Ω trim pot between pin 18 and pin 19. Connect external op amp as shown in diagram.
±2.5V ±5V ±10V	Connect 500Ω trim pot between pin 14 and pin 15. Connect external op. amp as shown in diagram.	Connect 500Ω trim pot between pin 16 and pin 17. Connect 100Ω trim pot between pin 18 and pin 19. Connect external op amp as shown in diagram.

APPLICATIONS

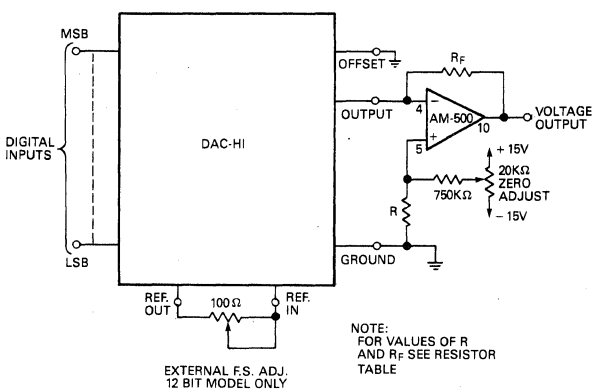
UNIPOLAR CURRENT OUTPUT



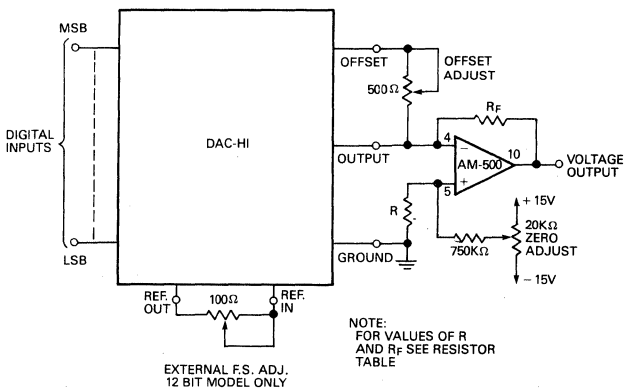
BIPOLAR CURRENT OUTPUT



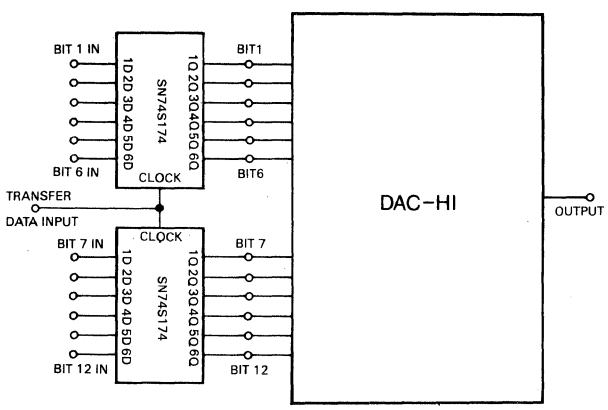
ULTRA-FAST UNIPOLAR VOLTAGE OUTPUT

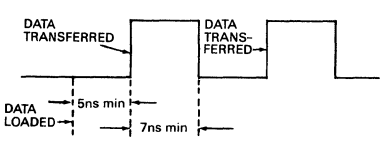


ULTRA-FAST BIPOLAR VOLTAGE OUTPUT



HIGH SPEED INPUT REGISTER





High Resolution, Ultra-Low Drift D/A Converters DAC-HR Series

FEATURES

- **13 to 16 Bits Resolution**
- **1.5 ppm/°C max. Tempco**
- **2 μsec max. settling time**
- **Unipolar or Bipolar Output**
- **2 mA Current Output**
- **Internal Feedback Resistors**

GENERAL DESCRIPTION

Datel-Intersil's DAC-HR series converters are precision digital-to-analog converters that offer high linearity, extreme stability and high resolution. Models with 13 to 16 bits allow resolving up to one part in 65,536, with a linearity error of only ±0.00075% and one of the lowest temperature coefficients of any commercially available converter, 1.5ppm/°C max.

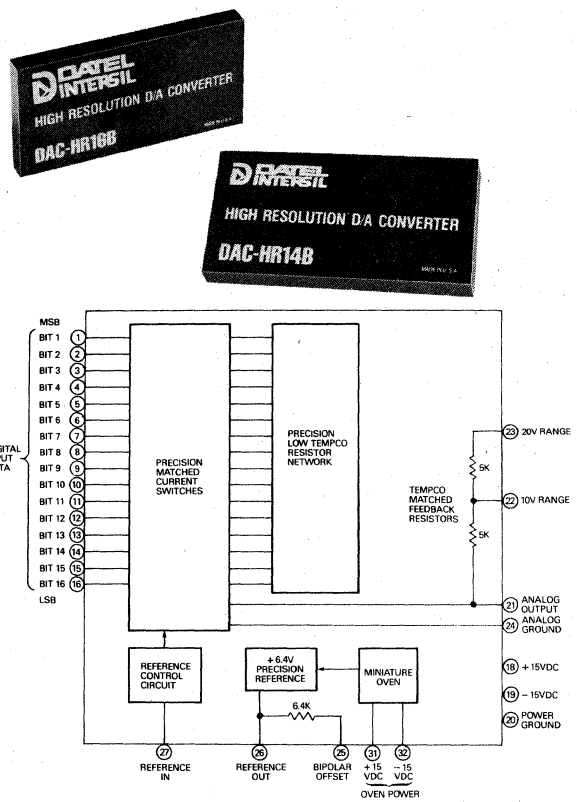
The DAC-HR's excellence in linearity and stability is due to a precision metal film resistor network that tracks to within 1 ppm/°C; an oven controlled zener reference which has a temperature coefficient of 0.25 ppm/°C and is current controlled within a high gain servo loop; plus the use of four individual monolithic quad current switches. The superior uniformity of these switches leads to inherently high accuracy of matching, requiring only minor trimming. The DAC-HR's are specifically designed for applications demanding a wide dynamic range, up to 96.3 dB for the 16 bit version. This allows a unit with a one volt full scale output to resolve down to 15 μV.

A full scale output current step settles to within 0.025% of full scale in only 200 nsec and to within 0.0015% of full scale in 2 μsec maximum.

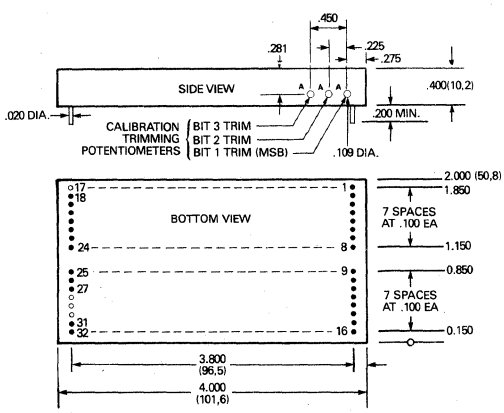
These converters can be used for either unipolar or bipolar applications. Full scale output is 0 to -2 mA for unipolar operation and ±1 mA for bipolar operation. Maximum voltage compliance is ±1V. For applications where an external operational amplifier is used, the necessary feedback and offset resistors are provided internally. These resistors have temperature coefficients matched to the ladder network. When used with an appropriate operational amplifier, the feedback resistance may be externally connected to produce outputs of 0 to +5V, 0 to +10V, ±2.5V, ±5V or ±10V.

Input coding is complementary binary for unipolar operation and complementary offset binary for bipolar operation. Inputs are compatible with standard DTL/TTL logic levels.

The DAC-HR series are completely self-contained in a 4 × 2 × 0.4 inch encapsulated module with dual in-line pinning compatibility.



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: OPEN DOTS INDICATE OMITTED PINS.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	BIT 1 IN (MSB)
2	BIT 2 IN
3	BIT 3 IN
4	BIT 4 IN
5	BIT 5 IN
6	BIT 6 IN
7	BIT 7 IN
8	BIT 8 IN
9	BIT 9 IN
10	BIT 10 IN
11	BIT 11 IN
12	BIT 12 IN
13	BIT 13 IN
14	BIT 14 IN*
15	BIT 15 IN*
16	BIT 16 IN*
18	+15V SUPPLY
19	-15V SUPPLY
20	POWER GROUND
21	ANALOG OUTPUT
22	10V RANGE
23	20V RANGE
24	ANALOG OUTPUT
25	OFFSET OUT
26	REFERENCE OUT
27	REFERENCE IN
31	+15V OVEN POWER
32	-15V OVEN POWER

*OPTIONAL PINS DEPENDING ON CONVERTER RESOLUTION

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, DAC-HR SERIES
(Typical at 25° C, ±15 VDC supplies unless otherwise noted)

	13B	14B	15B	16B
INPUT CHARACTERISTICS				
Coding, Unipolar Output	Complementary Binary			
Coding, Bipolar Output	Complementary Offset Binary			
Input Logic	DTL/TTL Compatible			
Input Logic Level, bit OFF ("1")	+2.0V min to +5.5V max.			
Input Logic Level, bit ON ("0")	0V min to +0.8V max.			
Loading	1 TTL load			
OUTPUT				
Output Current Range, unipolar	0 to -2 mA			
Output Current Range, bipolar	±1 mA			
Output Resistance	5K			
Output Voltage Compliance	±1V			
Output Voltage Ranges[1]	0 to +5V 0 to +10V ±2.5V ±5V ±10V			
PERFORMANCE				
Resolution, bits	13	14	15	16
Linearity Error, ±LSB max[2]	½	½	½	1
Monotonicity	Over Oper. Temp. Range			
Temperature Coefficient	1.5 ppm/° C max. with ref. oven ON 5 ppm/° C max. with ref. oven OFF			
Output Current Settling Time	200 nsec. to 0.025% of FS 2 μsec. to 0.0015% of FS			
Zero Current, all bits off	5 nA			
Power Supply Rejection	±10 ppm of FS/% Supply (−15V) ±1 ppm of FS/% Supply (+15V)			
POWER REQUIREMENT				
Supply Voltage	+15 VDC ±0.5 VDC @ 30 mA -15 VDC ±0.5 VDC @ 35 mA			
Oven Supply[4]	±15 VDC ±0.5 VDC @ 45 mA[4]			
PHYSICAL-ENVIRONMENTAL				
Operating Temp. Range	0° C to +70° C			
Storage Temp. Range	-55° C to +85° C			
Relative Humidity	Up to 100% Non-Condensing			
Package Size	2 × 2 × 0.4 inches 50,8 × 50,8 × 10, 1 mm			
Pins	0,020" Dia × 0.200" Long, min. Gold Plated			
Case Material	Black Diallyl Phthalate, Per MIL-M-14[3]			
Weight	4 Oz. (113 g.)			

NOTES:

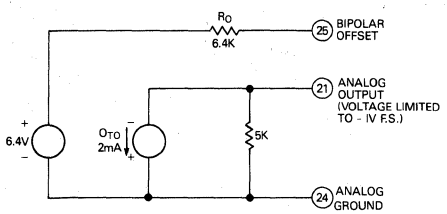
1. With external operational amplifier.
2. Differential Linearity is ±1 LSB max. for 16 Bit Units, performance remains monotonic.
3. Modules are fully repairable.
4. After 10 minute warm-up. See graph of Oven Current vs. Time.

TECHNICAL NOTES

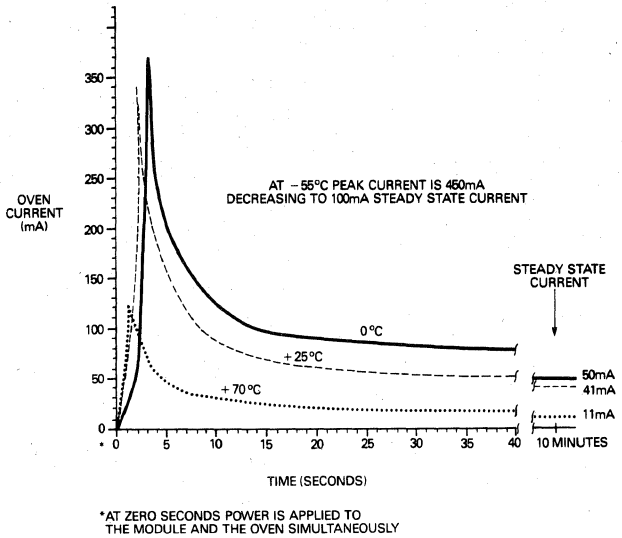
1. Linearity and output current specifications are measured into a short circuit or an operational amplifier summing junction. Operation of the device must be into the virtual ground of an operational amplifier summing junction. Any other output configuration can degrade linearity.
2. Calibration and adjustment should be carried out only after the D/A and all peripheral components have reached thermal equilibrium at their projected operating temperature. This is a necessary condition for realization of the high linearity and accuracy of these devices.
3. Although the DAC-HR series shares one of the lowest temperature coefficients of any commercially available D/A converters, high resolutions limit the allowable ambient temperature change from the calibration temperature to the values shown in the table provided. Performance is ensured by operation within these limits (as long as the operating temperature range of the unit is not exceeded).
4. The external operational amplifier selected for use must be matched for high accuracy low drift, low input bias current and low noise to the DAC-HR model selected. Datel-Intersil's AM-490-2 series chopper stabilized op amps feature three models with performance compatible to converters of the DAC-HR series.
5. Skewing of input codes can be a major contributor to the appearance of large transient spikes at the output ("glitches"). The most severe glitches occur at half-scale, the major carry transition from 011...1 to 100...0 or vice versa. At this time a skewing of the input codes can create a transition state code of 111...1 or 000...0. The duration of the "transition state code" is dependent on the degree of skewing, but its effect is dependent on the speed of the DAC (a fast DAC will respond to these brief spurious inputs to a greater degree than a slow DAC). The effects of input skewing can be easily minimized through the use of a high-speed input register to match input switching times. The input register shown is easily implemented with four Texas Instruments SN74S175 quad D-type flip-flops. Use of this register will minimize skewing induced glitching and ensure specified output settling times.
6. For bipolar output operation, the DAC-HR may be operated with complementary two's complement coding by externally complementing the MSB. Use of the input register shown makes this particularly easy as the flip-flops specified have complementary outputs, a feature that also allows the DAC-HR to be interfaced with straight binary coding as well as complementary binary.
7. Good board layout and connection practices are recommended to ensure proper operation of the converter. Leads to the external operational amplifier should be as short as possible.
8. The temperature controlled oven's ±15 VDC supply is separate from that of the module. The oven current requirements depend on temperature and vary during the warm-up period. Typical behavior is shown on the graph provided.
9. The DAC-HR series has externally accessible trimming potentiometers for the first three bits of each model. Calibration of these three bits at operating temperature insures linearity at operating temperature.

APPLICATIONS INFORMATION

EQUIVALENT OUTPUT CIRCUIT



REFERENCE OVEN CURRENT VS. TIME



*AT ZERO SECONDS POWER IS APPLIED TO THE MODULE AND THE OVEN SIMULTANEOUSLY

MAXIMUM AMBIENT TEMPERATURE CHANGE FOR MONOTONICITY

DAC-HR MODEL	13B	14B	15B	16B[2]
MAXIMUM CHANGE FROM CAL. TEMP[1]	±40°C	±20°C	±10°C	±5°C

1. All units must remain within specified operating temperature range.
2. For ±1-1/2 LSB linearity.

LSB OUTPUT VOLTAGES

OUTPUT VOLTAGE RANGE	OUTPUT VOLTAGE FOR LSB			
	HR-13B	HR-14B	HR-15B	HR-16B
0 to +5V ±2.5V	+0.610mV	+0.305mV	+0.153mV	+0.076mV
0 to +10V ±5V	+1.221mV	+0.610mV	+0.305mV	+0.153mV
±10V	+2.441mV	+1.221mV	+0.610mV	+0.305mV

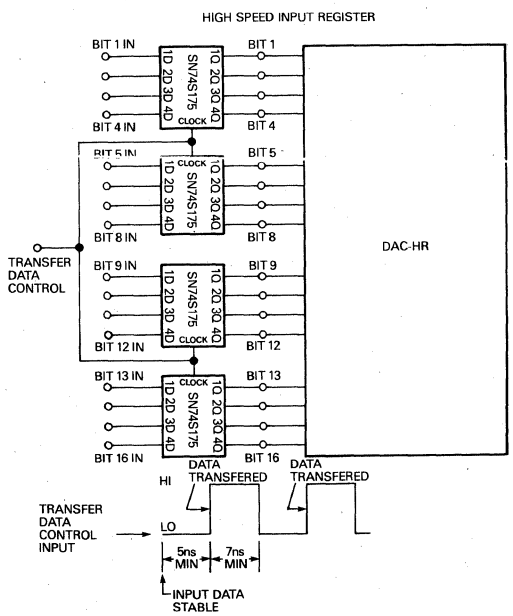
ORDERING INFORMATION

MODEL	RESOLUTION
DAC-HR13B	13 Binary Bits
DAC-HR14B	14 Binary Bits
DAC-HR15B	15 Binary Bits
DAC-HR16B	16 Binary Bits

Mating Socket DILS-2; 2 Required Per Module
Trimming Pot TP50 50Ω Cermet
100 ppm/°C

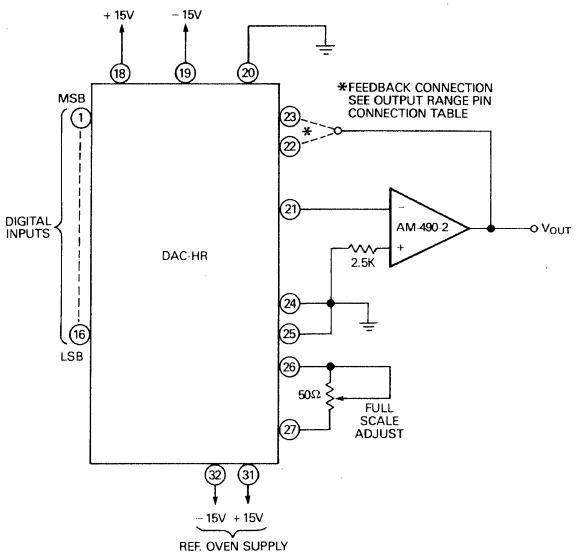
THESE CONVERTERS ARE COVERED BY GSA CONTRACT

HIGH SPEED INPUT REGISTER

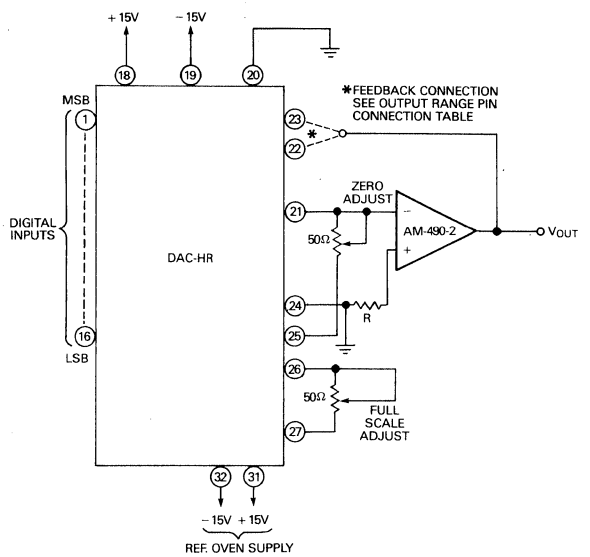


CONNECTIONS AND CALIBRATION

UNIPOLAR VOLTAGE OUTPUT



BIPOLAR VOLTAGE OUTPUT



UNIPOLAR CALIBRATION AND ADJUSTMENT OF BITS 1, 2 AND 3

1. Allow the converter and peripheral components to reach thermal equilibrium at operating temperature.
2. Find the voltage value of 1 LSB for the applicable converter resolution and Full Scale Voltage Range in the table of values provided.
3. With all bits OFF ("1"), set the Zero Adjust potentiometer to give a zero voltage output.
4. Set inputs as shown below and perform the indicated procedures.

INPUT CODE	INSTRUCTION
11100...0000	Record output voltage (V_1)
11011...1111	Adjust bit 3 trim for an output of V_1 +1 LSB
11000...0000	Record output voltage (V_2)
10111...1111	Adjust bit 2 trim for an output of V_2 +1 LSB
10000...0000	Record output voltage (V_3)
01111...1111	Adjust bit 1 trim for an output of V_3 +1 LSB

5. With all bits ON ("0") adjust the Full Scale Adjust potentiometer to give an output voltage of F.S. −1 LSB.

BIPOLAR CALIBRATION AND ADJUSTMENT OF BITS 1, 2 AND 3

1. Allow the converter and peripheral components to reach thermal equilibrium at operating temperature (approx. 10 minutes).
2. Find the voltage value of 1 LSB for the applicable converter resolution and Full Scale Voltage Range in the table of values provided.
3. With all bits OFF ("1") adjust the Zero Adjust potentiometer to give an output voltage of −F.S.
4. Set inputs as shown below and perform the indicated procedures

INPUT CODE	INSTRUCTION
11100...0000	Record output voltage (V_1)
11011...1111	Adjust bit 3 trim for an output of V_1 +1 LSB
11000...0000	Record output voltage (V_2)
10111...1111	Adjust bit 2 trim for an output of V_2 +1 LSB
10000...0000	Record output voltage (V_3)
01111...1111	Adjust bit 1 trim for an output of V_3 +1 LSB

5. With all bits ON ("0") adjust the Full Scale Adjust potentiometer to give an output reading of +F.S. −1 LSB.
6. With the MSB ON ("0") and all other bits OFF ("1") the output should read exactly zero ±1/2 LSB.

INPUT CODING TABLES

UNIPOLAR OUTPUT

UNIPOLAR OUTPUT SCALE	COMPLEMENTARY BINARY INPUT CODING	OUTPUT VOLTAGE FOR SELECTED RANGES	
		0 to +5V	0 to +10V
FS-1LSB	00000...00	+5V-1LSB*	+10V-1LSB*
⅞ FS	00011...11	+4.3750V	+8.7500V
¾ FS	00111...11	+3.7500V	+7.5000V
½ FS	01111...11	+2.5000V	+5.0000V
¼ FS	10111...11	+1.2500V	+2.5000V
⅛ FS	11011...11	+0.6250V	+1.2500V
1 LSB	11111...10	*	*
0	11111...11	0V	0V

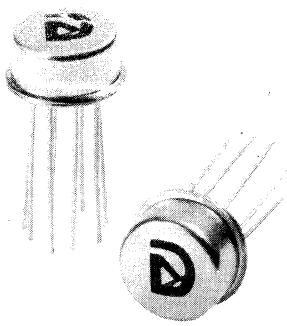
*SEE TABLE OF LSB VOLTAGES

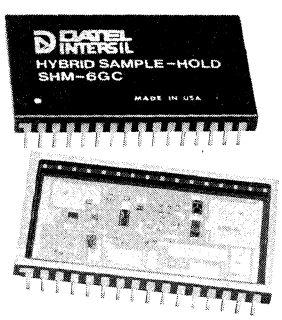
BIPOLAR OUTPUT

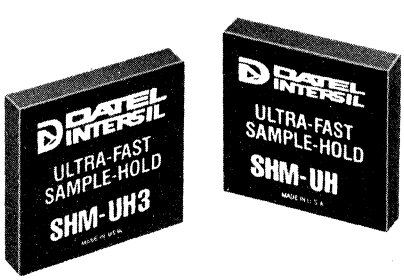
BIPOLAR OUTPUT SCALE	COMPLEMENTARY OFFSET BINARY INPUT CODING	OUTPUT VOLTAGE FOR SELECTED RANGES		
		±2.5V	±5V	±10V
+FS-1LSB	00000...00	+2.5V-1LSB*	+5V-1LSB*	+10V-1LSB*
+¾ FS	00011...11	+1.8750V	+3.7500V	+7.5000V
+½ FS	00111...11	+1.2500V	+2.5000V	+5.0000V
+1 LSB	01111...10	*	*	*
0	01111...11	0V	0V	0V
−½ FS	10111...11	−1.2500V	−2.5000V	−5.0000V
−¾ FS	11011...11	−1.8750V	−3.7500V	−7.5000V
−FS	11111...11	−2.5000V	−5.0000V	−10.0000V

*SEE TABLE OF LSB VOLTAGES

Sample-Holds







Quick Selection: Sample-Holds

	MODEL	DESCRIPTION	ACCURACY	ACQUISITION TIME[1]	APERTURE DELAY	INPUT RANGE	GAIN	BANDWITH
MON	**SHM-IC-1** **SHM-IC-1M**	Low Cost Sample-Hold	0.01%	5 μsec	50 nsec	±10V	±1.00[2]	2 MHz
MON	**SHM-LM-2** **SHM-LM-2M**	Low Cost Sample-Hold	0.01%	6 μsec	100 nsec	±10V	+1.00	1 MHz
HYBRID	**SHM-6MC** **SHM-6MR** **SHM-6MM**	Fast Sample-Hold	0.01%	1 μsec	20 nsec	±10V	±1 to ±10	5 MHz
HYBRID	**SHM-HUMC** **SHM-HUMR** **SHM-HUMM**	Ultra-Fast Sample-Hold	0.1%	25 nsec	6 nsec	±2.5V	+0.975	50 MHz
MODULAR	**SHM-1**	General Purpose	0.025%	5 μsec	50 nsec	±10V	+1.00	650 kHz
MODULAR	**SHM-2** **SHM-2E**	Ultra-Fast Sample-Hold	0.1%	100 nsec	10 nsec	±10V	+1.00	10 MHz
MODULAR	**SHM-5**	Ultra-Fast Sample-Hold	0.01%	350 nsec	20 nsec	±10V	-1.00	5 MHz
MODULAR	**SHM-UH** **SHM-UH3**	Ultra-Fast Sample-Hold	0.25% 0.05%	50 nsec 30 nsec	10 nsec 5 nsec	±5V	+0.95 +0.98	45 MHz

NOTES:
1. For 10V Change.
2. Can be configured for gains greater than ±1.
3. Maximum offset voltage over operating temperature range.

HOLD-MODE DROOP	TEMPCO	POWER REQUIREMENT	PACKAGING	OPERATING TEMP. (°C)	PRICE (1-24)	SEE PAGE
50μV/msec	20μV/°C	±15 VDC	14 Pin Ceramic DIP Hermetically Sealed	0 to +70	$ 12.50	212C
				-55 to +125	$ 56.00	
200μV/msec	10mV[3]	±15 VDC	8 Pin TO-99 Hermetically Sealed	0 to +70	$ 5.95	216C
100μV/msec	5mV[3]			-55 to +125	$ 52.50	
10μV/μsec	100μV/°C	±15 VDC +5V	32 Pin Ceramic DIP Hermetically Sealed	0 to +70	$119.00	220C
				-25 to +85	$149.00	
				-55 to +100	$209.00	
50μV/μsec	50μV/°C	±15 VDC +5V	24 Pin Ceramic DIP Hermetically Sealed	0 to +70	$ 99.00	218C
				-25 to +85	$149.00	
				-55 to +100	$199.00	
1μV/μsec	20ppm/°C	±15 VDC -20V	2 x 1 x 0.375 in. (51 x 25 x 10 mm)	0 to +70	$ 82.00	*
50μV/μsec	30ppm/°C	±15 VDC	2 x 1 x 0.375 in. (51 x 25 x 10 mm)	0 to +70	$105.00	*
330μV/μsec					$110.00	
20μV/μsec	15ppm/°C	±15 VDC	2 x 2 x 0.375 in. (51 x 51 x 10 mm)	0 to +70	$219.00	230C
50μV/μsec	50μV/°C	±15 VDC +5V	2 x 2 x 0.375 in. (51 x 51 x 10 mm)	0 to +70	$210.00	224C
					$231.00	

*For Data Sheet Contact Nearest Datel Sales Office

Datel offers modular products in operating temperature ranges of −25 to +85°C (suffix-EX) and −55 to +85°C (suffix-EXX-HS). For information on these high reliability modules contact nearest Datel sales office.

THESE PRODUCTS ARE COVERED BY GSA CONTRACT

Monolithic Sample-Hold
Model SHM-IC-1

FEATURES

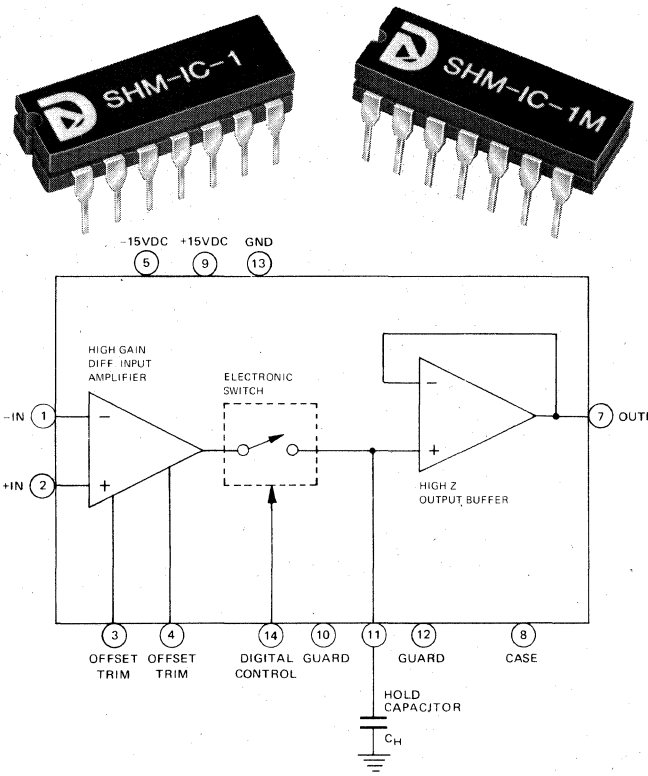
- 5 μsec. Acquisition to .01%
- 50 nsec. Aperture
- Inverting or Noninverting
- 2MHz Bandwidth
- .01% Feedthrough
- 14 Pin DIP Package

GENERAL DESCRIPTION

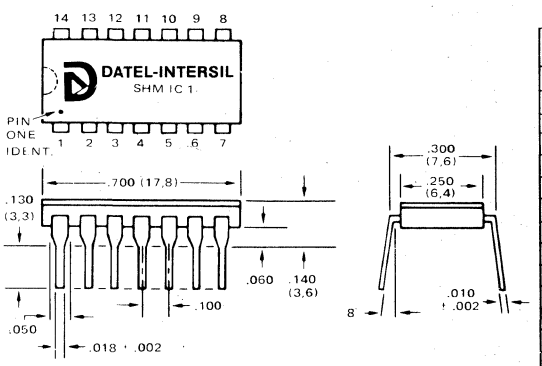
The SHM-IC-1 is a new monolithic integrated circuit sample and hold with excellent performance features. It is a self-contained device requiring only an external holding capacitor, the value of which can be chosen by the user to achieve his desired speed and accuracy requirement. The unit consists of a high gain differential input amplifier, a digitally controlled electronic switch, and a high input impedance buffer amplifier. The SHM-IC-1 operates in a closed loop configuration, either inverting or noninverting, with accuracy and speed determined by the input amplifier characteristics and the value of the holding capacitor. The electronic switch is controlled by a DTL/TTL compatible logic input.

The most common configuration for the SHM-IC-1 is a unity gain, noninverting sample and hold. In this configuration the device has a ±10V input and output range with 10 ohms input impedance. Specifications are given for this unit with two different values of holding capacitor, .001μF and .01μF. The .001μF capacitor gives a 4 μsec. acquisition time to 0.1% for a 10V change, a 2MHz tracking bandwidth and 50mV/sec. maximum hold mode droop. The .01μF capacitor gives a 10 μsec. acquisition time, 1MHz tracking bandwidth, and 5mV/sec. maximum droop. Characteristics for other values of holding capacitor can be determined from graphs which are shown. The SHM-IC-1 can also be configured as either an inverting or noninverting sample and hold with gain by the use of two external resistors.

This device is housed in a 14-pin hermetically sealed dual-in-line package. Operating temperature range is 0°C to +70°C for the SHM-IC-1 and −55°C to +125°C for the SHM-IC-1M.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	−IN
2	+IN
3	OFFSET TRIM
4	OFFSET TRIM
5	−15VDC POWER
6	NO CONNECTION
7	OUTPUT
8	CASE
9	+15VDC POWER
10	GUARD
11	HOLD CAPACITOR (C_H)
12	GUARD
13	GROUND
14	DIGITAL CONTROL

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, SHM-IC-1

(Typical at 25°C, ±15V Supplies, unless otherwise noted)

INPUT AMPLIFIER SPECIFICATIONS	
DC Gain, volts/volt[1]	50K, 25K min.
Bias Current	50nA, 200nA max.
Offset Current	10nA, 50nA max.
Offset Voltage (adjust. to zero)	3mV, 6mV max.
Offset Voltage Drift	20 μV/°C
Common Mode Voltage Range	±10V min.
Common Mode Rejection Ratio	74dB min.
Power Supply Rejection	±30μV/% max.
Gain Bandwidth Product	2MHz
GENERAL SPECIFICATIONS, SAMPLE & HOLD, G = +1	
Input Voltage Range	±10V min.
Input Impedance	10^8 ohms
Output Voltage Range	±10V min.
Output Current, S.C. protected	±10mA min.
Output Impedance	0.2 ohm
Aperture Delay	50 nsec.
Aperture Uncertainty	5 nsec.
Gain Error, sampling mode	.01% max.
Hold Mode Noise	350μV RMS
Digital Input, Sample Mode, DTL/TTL	0 to +0.8V @ −0.8mA
Hold Mode, DTL/TTL[2]	+2.0 to +5.5V @ +20μA
SAMPLE & HOLD, G = +1, C_H = .001μF	
Acquisition Time, 10V to 0.1%	4 μsec.
Acquisition Time, 10V to .01%	5 μsec.
Bandwidth, small signal, sampling	2.0MHz
Slew Rate	5V/μsec.
Hold Mode Voltage Droop	50mV/sec. max.
Hold Mode Feedthrough	.01% max.
Sample-to-Hold Offset Error, V_{IN} = 0	20mV max.
Sample-to-Hold Gain Error, V_{IN} = ±10V	.05% max. of output
Sample-to-Hold Nonlinearity Error	.01% max. of output
SAMPLE & HOLD, G = +1, C_H = .01μF	
Acquisition Time, 10V to 0.1%	10 μsec.
Acquisition Time, 10V to .01%	12 μsec.
Bandwidth, small signal, sampling	1.0MHz
Slew Rate	3V/μsec.
Hold Mode Voltage Droop	5mV/sec. max.
Hold Mode Feedthrough	.002% max.
Sample-to-Hold Offset Error, V_{IN} = 0	2mV max.
Sample-to-Hold Gain Error, V_{IN} = ±10V	.005% max.
Sample-to-Hold Nonlinearity Error	.001% max.
POWER REQUIREMENT	±15VDC @ 5mA max.
PHYSICAL-ENVIRONMENTAL	
Operating Temperature Range, SHM-IC-1	0°C to 70°C
Operating Temperature Range, SHM-IC-1M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Package, hermetically sealed ceramic DIP	TO-116

NOTES: 1. 40K and 20K respectively at +125°C for SHM-IC-1M.
2. +3.0 to +5.5V at −55°C for SHM-IC-1M.

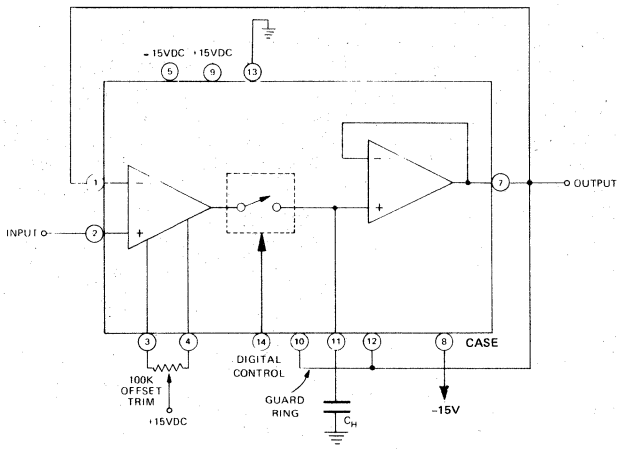
TECHNICAL NOTES

The most commonly used sample and hold configuration for the SHM-IC is the noninverting unity gain circuit. This gives a high input impedance of 10^8 ohms, and the output voltage in the sample mode follows the input. Specifications are given for this configuration for two values of C_H, .001μF and .01μF. The .001μF capacitor gives excellent speed (4 μsec. acquisition) with good hold mode voltage droop (only 50mV/sec. max). For even better speed, a 100 pF capacitor may be used to give an acquisition time of only 2 μsec. The hold mode droop, however, increases by an order of magnitude to 500mV/sec., and the sample-to-hold errors also increase. For excellent accuracy a .01 μF capacitor should be used, giving an acquisition time of 10 μsec., and a hold mode droop of only 5mV/sec. max. Even larger values of holding capacitor can be used with proportionate increases in accuracy but slower speed. The application graphs show the results for the different values.

For best results, C_H should be a good quality capacitor with very high insulation resistance and low dielectric absorption. For temperatures up to +85°C polystyrene type capacitors are recommended. It is also recommended for lowest hold mode droop that a guard ring be used around the C_H terminal (pin 11) in the circuit board layout as shown on the last page. This is done to present leakage to other conductors on the circuit board due to board leakage and contamination. If a large value polystyrene capacitor is used, such as 1μF, hold mode droop as low as 20μV/sec. (typical) can be achieved with an acquisition time of about 3 milliseconds.

Three error contributions are specified for sample-to-hold errors: offset error, gain error, and nonlinearity error. These sampling errors are caused by a small amount of charge being dumped to or from the holding capacitor by the sampling switch and are reduced by a larger value of C_H. It is possible to compensate for these errors by changing the gain and offset elsewhere in the external circuitry for the noninverting unity gain case. For the inverting case, the gain can be accomplished by adjusting the external resistor values and an offset can be applied to pin 2 of the input amplifier. When this external compensation is used, the output will be in error during sampling, but will be accurate in the hold mode. Only the nonlinearity error will remain of the sample-to-hold errors. The offset adjustment of the input amplifiers should be used only to zero the device in the sample mode.

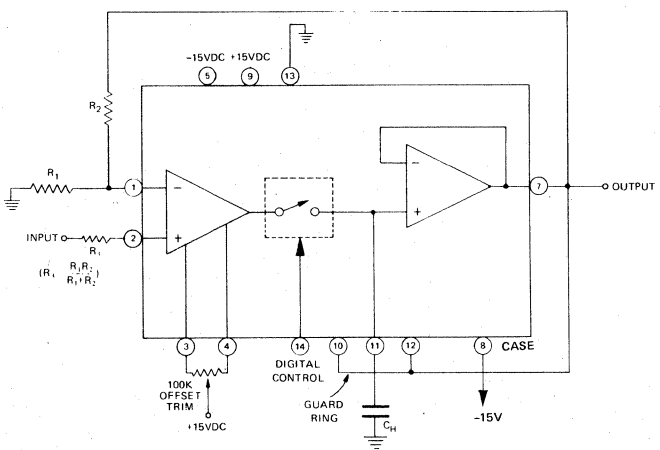
In the inverting gain of one operating mode, the feedback and input resistors should be carefully matched or trimmed to give the desired gain of one. In general, the operating parameters are the same as in the noninverting unity gain configuration except that the sampling bandwidth is reduced by a factor of two. Likewise, for higher gain configurations the sampling bandwidth is proportionately reduced.



SAMPLE & HOLD, UNITY GAIN, NONINVERTING

GAIN = +1

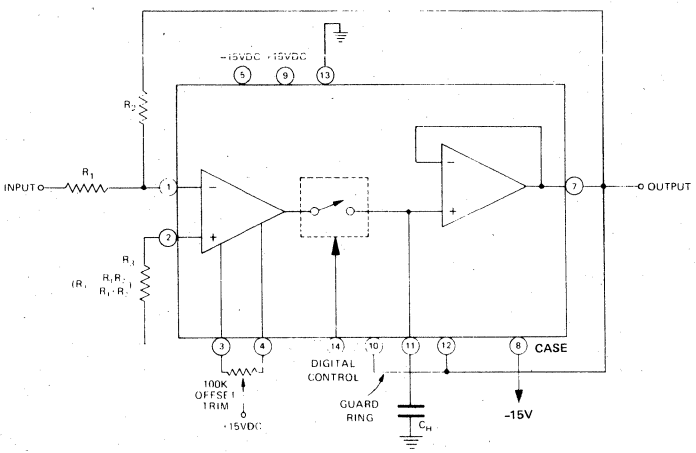
The 100K ohm offset trimming potentiometer should be a 100 ppm/°C cermet 15 turn type. These are available from Datel-Intersil at each. To zero, ground input (pin 2) and digital control (pin 14) and adjust 100K offset trim for zero output (pin 7).



SAMPLE & HOLD, NONINVERTING WITH GAIN

$$\text{GAIN} = 1 + \frac{R_2}{R_1}$$

Bandwidth decreases proportionately with gain. R_3 is equal to the parallel combination of R_1 and R_2 and is used to compensate for voltage offset caused by input bias current. R_1 and R_2 should be 100 ppm/°C metal film type resistors.



SAMPLE & HOLD, INVERTING

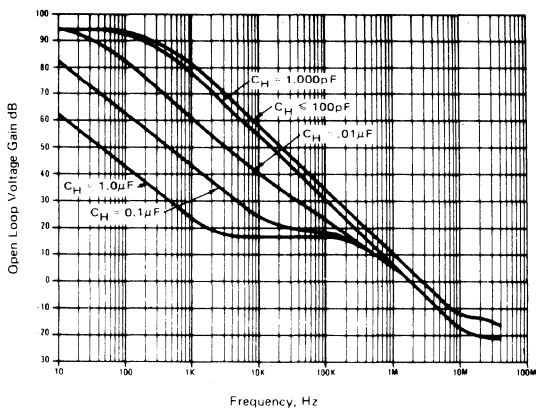
$$\text{GAIN} = -\frac{R_2}{R_1}$$

For a gain of −1 the bandwidth is one half of that given for the noninverting mode. R_3 is equal to the parallel combination of R_1 and R_2 and is used to compensate for voltage offset caused by input bias current. R_1 and R_2 should be matched 100 ppm/°C metal film type resistors for a gain of −1. For higher gains the ratio should be matched closely or trimmed with a small value carbon composition type resistor.

PERFORMANCE PARAMETERS

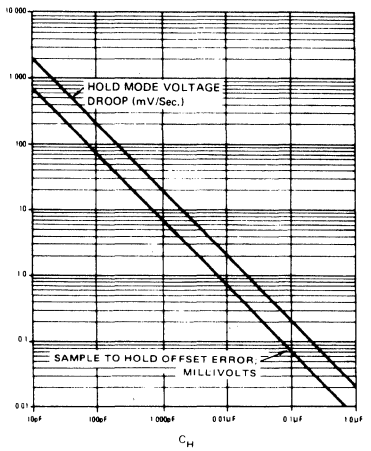
OPEN LOOP FREQUENCY RESPONSE

Typical at 25°C, ±15V Supplies



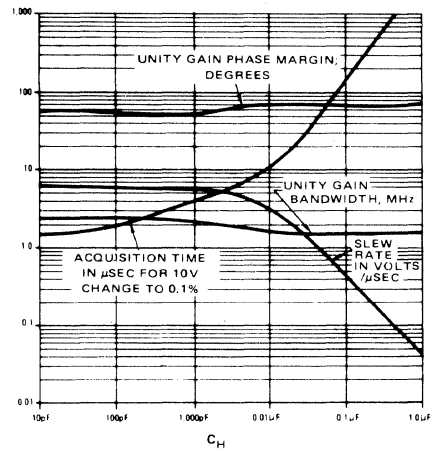
ACCURACY CHARACTERISTICS VS. C_H

Typical at 25°C, ±15V Supplies



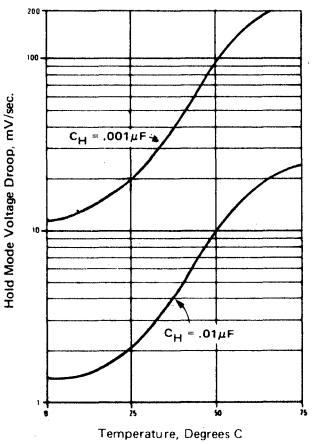
SPEED CHARACTERISTICS VS. C_H

Typical at 25°C, ±15V Supplies

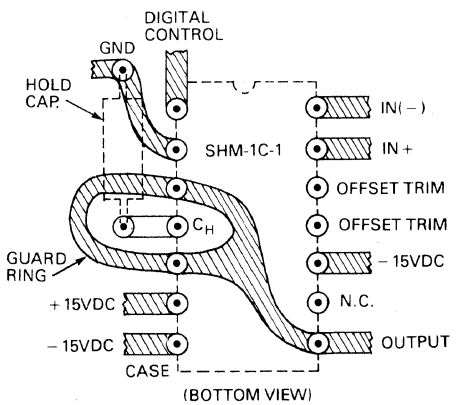


HOLD MODE VOLTAGE DROOP VS. TEMPERATURE

Typical, ±15V Supplies



RECOMMENDED CIRCUIT BOARD LAYOUT USING GUARD RING



ORDERING INFORMATION

Model SHM-IC-1
Model SHM-IC-1M
Trimming Potentiometer
TP100K (100KΩ)

Contact Factory for Quantity Pricing

The SHM-IC-1 is covered under GSA Contract

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PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Low Cost Monolithic Sample-Hold Model SHM-LM-2

FEATURES

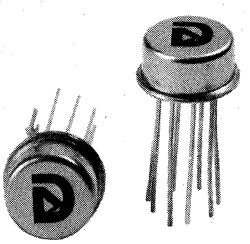
- **5 μsec. Acquisition Time**
- **.01% Gain Accuracy**
- **TTL/CMOS Logic Compatible**
- **±5V to ±18V Supplies**
- **TO-99 Package**
- **Low Cost**

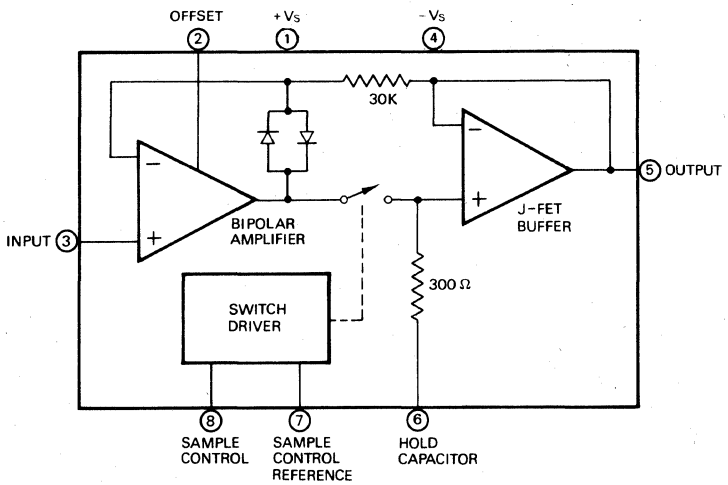
GENERAL DESCRIPTION

The SHM-LM-2 is a low cost monolithic sample-hold circuit with excellent performance features. It is self-contained requiring only an external hold capacitor with the value selected by the user for desired speed and accuracy characteristics. Acquisition time is 6 μsec. for a 10V change to .01% using a 1000pF capacitor and 25 μsec. using a .01 μF capacitor. It is 5 μsec. and 20 μsec. respectively for a 10V change to 0.1%. This device is internally configured as a unity gain follower with a gain error of less than .01% in the sample mode.

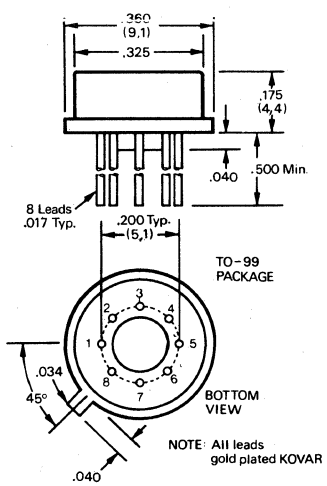
The circuit consists of a bipolar input amplifier, a low leakage electronic switch, and an FET output amplifier. The monolithic fabrication process combines P channel junction FET's with bipolar transistors to achieve a low noise, high input impedance output amplifier. Other important specifications include 10^{10} ohms input impedance and 1 MHz bandwidth. Aperture time is less than 100 nsec. and hold mode feedthrough is less than .005%. Hold mode droop is 200 μV/msec. max. with a 1000pF hold capacitor and 20 μV/msec. max. with a .01 μF capacitor. The SHM-LM-2 can operate over a power supply range of ±5V to ±18V.

Applications include sampling for A/D conversion, deglitching circuits, automatic zeroing circuits, and analog demultiplexing circuits. It is recommended that the holding capacitor (C_H) be a teflon, polystyrene, or polypropylene type for best results. Operating temperature range is 0°C to 70°C for SHM-LM-2 and -55°C to +125°C for SHM-LM-2M.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	+ POWER SUPPLY
2	OFFSET ADJUST
3	INPUT
4	− POWER SUPPLY
5	OUTPUT
6	HOLD CAPACITOR (C_H)
7	SAMPLE CONTROL REF.
8	SAMPLE CONTROL

DATEL-INTERSIL, INC. 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 95134

SPECIFICATIONS

(Typical at 25°C, ±15V supplies and C_H = .01 μF unless otherwise stated)

MAXIMUM RATINGS	
Power Supply Voltage, pins 1 & 4	±18V
Input Voltage, pin 3	±Supply
Sample Control to Sample Reference, pin 8 to pin 7	+7, -30V
Hold Capacitor Short Circuit	10 sec.
INPUTS	
Input Voltage Range	±11.5V min.
Input Overvoltage, no damage	± Supply
Input Impedance	10^{10} ohms
Input Bias Current	10 nA typ., 50 nA max.
Sample Control	TTL or CMOS
Sample Control Input Current[1]	10 μA max.
OUTPUT	
Output Voltage Range	±11.5V min.
Output Current, S.C. protected	±5 mA
Output Impedance	0.5 ohm
PERFORMANCE	
Gain	+1.000, +0, −.01%
Output Offset Voltage, adj. to zero	±7 mV max.
Offset Voltage Drift, SHM-LM-2	20 μV/°C
Offset Voltage Drift, SHM-LM-2M	10 μV/°C[2]
Sample to Hold Offset	2.5 mV max.
Hold Mode Feedthrough	.01% max.
Power Supply Rejection Ratio	80 dB min.
Output Noise, hold mode (10Hz-100kHz)	8.5 μV RMS
Hold Mode Droop, C_H = 1000 pF	200 μV/msec. max.
C_H = .01 μF	20 μV/msec. max.
DYNAMIC RESPONSE	
Acquisition Time	
10V Change, C_H = 1000 pF	5 μsec. to 0.1%
10V Change, C_H = 1000 pF	6 μsec. to .01%
20V Change, C_H = 1000 pF	7 μsec. to 0.1%
20V Change, C_H = 1000 pF	8 μsec. to .01%
10V Change, C_H = .01 μF	20 μsec. to 0.1%
10V Change, C_H = .01 μF	25 μsec. to .01%
Aperture Delay Time	100 nsec.
Hold Mode Settling Time[3]	800 nsec.
Bandwidth, Sample Mode, −3 dB	1 MHz
POWER REQUIREMENT	
Voltage, rated performance	±15VDC
Voltage Range, operating	±5V to ±18VDC
Quiescent Current	6 mA
PHYSICAL-ENVIRONMENTAL	
Operating Temp. Range, SHM-LM-2	0°C to +70°C
SMM-LM-2M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Case	8 pin TO-99

NOTES:
1. For either Sample Control or Sample Control Reference inputs
2. 28 μV/°C max.
3. The time for the output to settle within 1 mV of final value after the logic command to switch into hold mode.

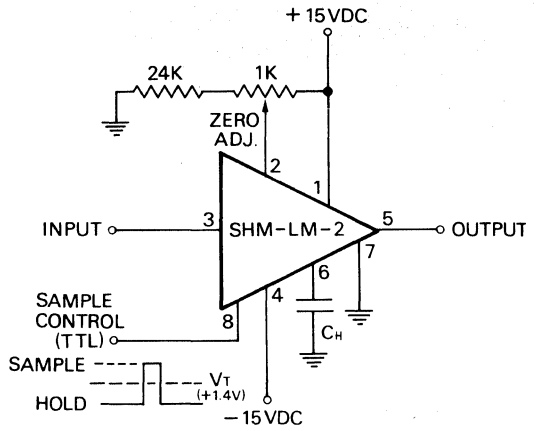
ORDERING INFORMATION

Model	Operating Temp. Range
SHM-LM-2	0°C to 70°C
SHM-LM-2M	-55°C to +125°C

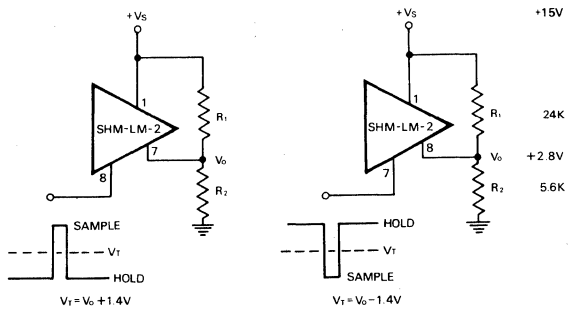
Trimming Potentiometer, TP1K

THE SHM-LM-2 IS COVERED BY GSA CONTRACT

CONNECTION DIAGRAM



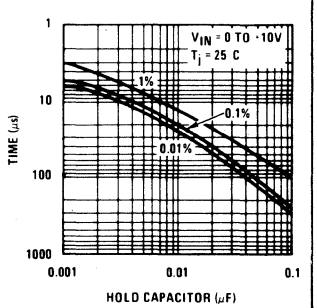
SAMPLE-CONTROL CONNECTIONS



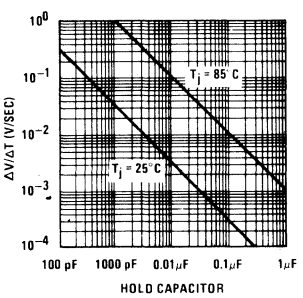
For TTL connect pin 7 to ground.

For TTL use values shown on right.

ACQUISITION TIME



HOLD MODE DROOP



TECHNICAL NOTES

1. The sample to hold offset can be adversely affected by stray capacitive coupling from input sample control signals to the hold capacitor. It is recommended that a guard ring connected to the output be put around pin 6 in a circuit board layout in order to minimize this effect.
2. For various types of logic inputs the logic threshold (V_T) is set by two biasing resistors as shown in the diagram. Inverted or non-inverted pulses may be used by using either pin 7 or pin 8 as the sample control input.

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PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Ultra-Fast, 0.1% Microelectronic Sample-Hold Model SHM-HU

FEATURES

- **25 nsec Acquisition Time**
- **50 MHz Bandwidth**
- **10 psec Aperture Uncertainty**
- **Up to 8 Bit Accuracy**
- **± 2.5V Input Range**

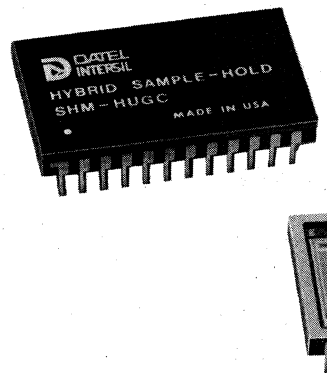
GENERAL DESCRIPTION

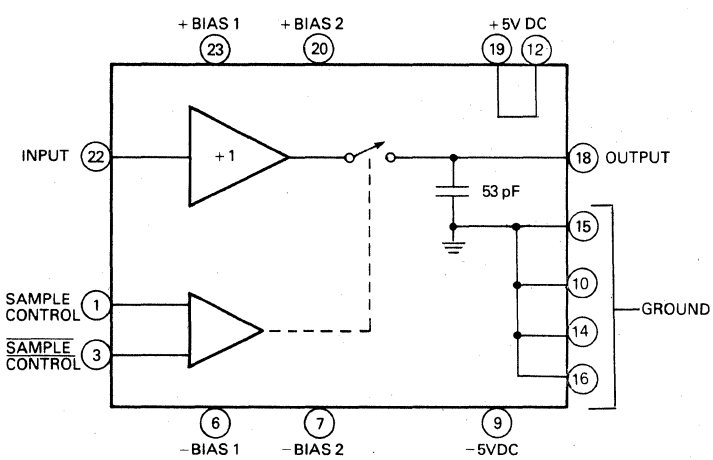
The SHM-HU is an ultra high speed sample-hold capable of video speed signal processing. While specifically designed for use with Datel-Intersil's ADC-HU3B A/D converter, it is compatible with other ultrafast A/D's with resolutions up to 8 bits. The SHM-HU acquires a full scale 5V input change in just 25 nsec. and features a 10 psec aperture uncertainty time. Bandwidth is 50 MHz and the slew rate is 200V/μsec.

Through the use of thin film hybrid construction, this ultra high speed circuit is contained in a miniature 24-pin ceramic package. A 53 picofarad MOS hold capacitor is incorporated inside the package and provision is made for externally added capacitance when necessary. The sample-hold requires four external resistors and an LH0033 fast buffer amplifier for completion. The circuit is zeroed by adjustment of the LH0033 amplifier.

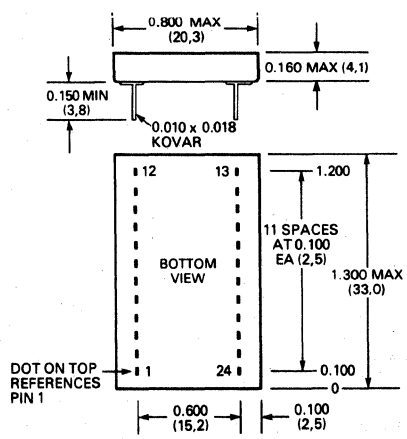
Other features of this unit include a ± 2.5V input/output voltage range and a fixed gain of 0.955. The sampling switch is controlled by a complementary series 10,000 ECL input. An ECL differential line driver can be conveniently used for the sample control inputs.

Power requirements are ± 15 VDC at 60 mA and ± 5 VDC at 70 mA. There are three basic models covering three operating temperature ranges, 0 to +70°C, −25 to +85°C and −55 to +100°C. For high reliability versions of the SHM-HU, including Datel's "S" program and MIL-STD-883 level B, contact the factory.





MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	SAMPLE CONTROL
3	$\overline{\text{SAMPLE CONTROL}}$
6	−BIAS 1
7	−BIAS 2
9	−5V POWER
15	GROUND
18	OUTPUT
19	+5V POWER
20	+BIAS 2
22	INPUT
23	+BIAS 1

NOTE: ALL OTHER PINS ARE NO CONNECTION

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, SHM-HU
(Typical at 25°C, ±15V and ±5V supplies with external LH0033 Buffer Amp. unless otherwise noted)

MAXIMUM RATINGS

Power Supplies, Pins 9-19	±6V
Analog Input Volatage, Pin 22	±5V
Sample Inputs, Pins 1 & 3	±5V Differential
Current, Pins 6, 7, 20, 23,	50 mA

INPUTS

Input Voltage Range, Min	±2.5V
Input Bias Current	25μA
Maximum Source Impedance	51 Ohms
Input Impedance	10^6 Ohms
Sample Control Inputs[4]	Differential ECL 10,000 Positive Pulse on Pin 1 and Negative Pulse on Pin 2 gives Sample Mode

OUTPUT[1]

Output Voltage Range, Min.	±2.5V
Output Current	±10 mA
Output Impedance	6 Ohms

PERFORMANCE

Accuracy	0.1%
Gain	+0.955
Output Offset Voltage[2], Sample Mode	±100 mV max.
Output Offset Voltage Drift	±100 μV/°C max.
Sample to Hold Offset Error	±100 mV max.
Hold Mode Droop	50 μV/μ sec.
Hold Mode Feedthrough	0.02%

DYNAMIC RESPONSE

Acquisition Time, 5V Step to 0.2%	25 nsec.
Bandwidth, -3 dB, Sample Mode	50 MHz
Slew Rate	200V/μsec.
Aperture Delay Time	6 nsec.
Aperture Uncertainty Time	10 psec.

POWER REQUIREMENTS[3]

±15 VDC ±0.75V @ 60 mA
±5 VDC ±0.25V @ 70 mA

PHYSICAL ENVIRONMENTAL

Operating Temperature Ranges

SHM-HUMC	0 to +70°C
SHM-HUMR	-25 to +85°C
SHM-HUMM	-55 to +100°C
Storage Temperature Range	-65 to +150°C
Package Type	24 Pin Ceramic
Pins	.010 x .018 Inch Kovar
Weight	0.2 Oz (6 g)

NOTES

1. Output is from LH0033 amplifier and is not short circuit proof.
2. Output offset voltage adjustable to zero by LH0033 offset adjustment.
3. ±12V supplies can be used if the 360 ohm resistors at the Bias 1 pins are changed to 240 ohms and the 240 ohm resistors at the Bias 2 pins are changed to 160 ohms.
4. The SHM-HU can be driven by TTL logic input by biasing $\overline{\text{SAMPLE}}$ CONTROL input to +1.2V and driving the SAMPLE CONTROL with a positive pulse for sample mode.

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	TYPE SEAL
SHM-HUMC	0 to +70°C	Hermetic
SHM-HMUR	-25 to +85°C	Hermetic
SHM-HUMM	-55 to +100°C	Hermetic

Mating Socket: DILS-3 (24-Pin Socket)
Trimming Potentiometer: TP100 (100 ohms)

For high reliability versions of the SHM-HU, including Datel's "S" program and MIL-STD-883 level B, contact factory.

THE SHM-HU IS COVERED BY GSA CONTRACT.

TECHNICAL NOTES

1. It is recommended that the ±5V supplies of the SHM-HU be bypassed with 0.1 μF ceramic capacitors as close as possible to pins 9 and 19. The ±15V supplies to the LH0033 should be bypassed with the same value capacitors.

2. It is essential that the output lead from pin 18 to pin 5 of the LH0033 be kept as short and direct as possible. Also, the complementary ECL driver should be as close as possible to pins 1 and 3 to minimize lead lengths to these pins.

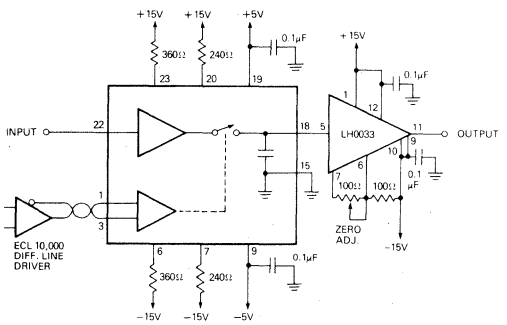
3. With models SHM-HUGC, SHM-HUMC and SHM-HUMR, the LH0033C should be used, and with model SHM-HUMM, model LH0033 should be used.

4. An external hold capacitor may be added from pin 18 to pin 15. This capacitor should be an MOS or polystyrene type. Hold mode droop and sample-to-hold offset error will decrease proportionately with the size of this capacitor and acquisition time will increase proportionately.

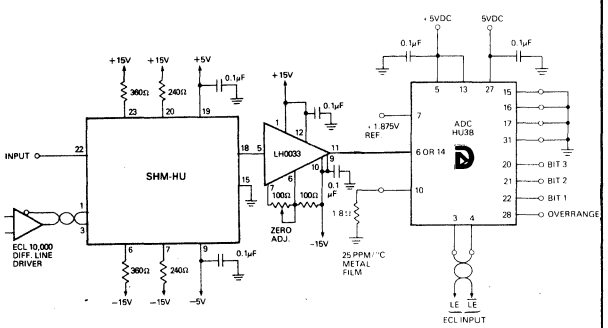
5. The SHM-HU can be used with model ADC-HZ12B to realize a fast 4 μsec A/D converter with sample-hold. The ultra high speed of the SHM-HU will add negligibly to the conversion time. The ADC-HZ12B in this configuration is connected for ±2.5V input and has its output coding short cycled to 8 bits instead of 12.

6. Although the SHM-HU has been specifically designed for use with Datel-Intersil's ADC-HU3B A/D converter, it is compatible with other ultra-fast A/D s of up to 8 bits resolution.

CONNECTION DIAGRAM



CONNECTION TO DATEL SYSTEMS ADC-HU3B



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PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

0.01%, 1.0 μ Sec. Microelectronic Sample-Hold Model SHM-6

FEATURES

- **0.01% Accuracy**
- **1.0 μs Acquisition Time**
- **2 nsec Aperture Uncertainty**
- **5 MHz Bandwidth**
- **50mA Output Current**
- **Gain Programmable From ±1 to ±10**

GENERAL DESCRIPTION

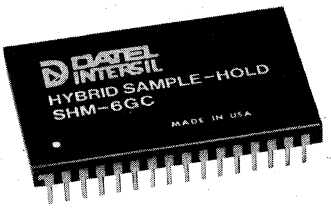
The SHM-6 is a high speed, high accuracy sample-hold circuit manufactured with thin film hybrid technology. This design offers the speed and performance of modular sample-holds with the compactness and integrity of advanced hybrid techniques. The unit's excellent high-speed characteristics include a guaranteed acquisition time of 800 nsec to 0.1% accuracy and 1.0 μsec to 0.01% for a 10 volt change.

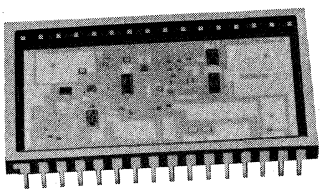
The SHM-6 is a complete sample-hold containing a precision MOS holding capacitor. The input amplifier is an open loop transductance amplifier which can be externally connected for closed loop gains from ±1 to ±10. In addition to its speed, accuracy and selectable gain, the SHM-6 has an output capability of 50 mA. These features allow this unit to offer an unusual degree of adaptability.

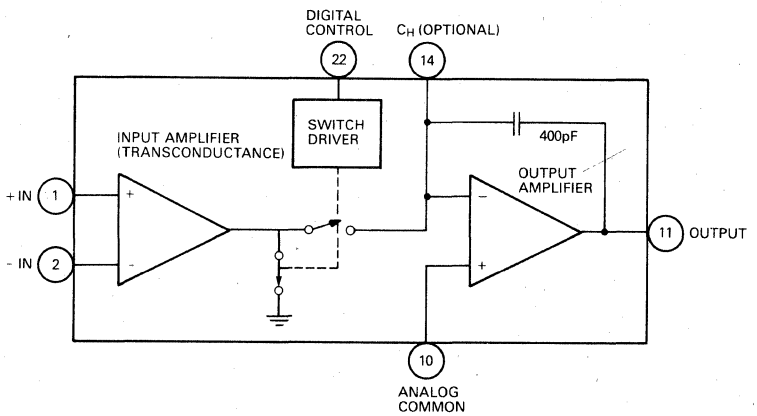
The most frequently utilized configuration of the SHM-6 is a unity gain, noninverting sample-hold. In this mode, the device has a ±10V input and output range with $10^8\Omega$ input resistance. Full power bandwidth is 500 KHz, and small signal tracking capability is 5 MHz. The input offset voltage and sample to hold error can be adjusted to zero with the use of two external trim pots.

The SHM-6 is a key component in fast data acquisition systems. A 110 KHz throughput rate can be accomplished using the SHM-6 in conjunction with Datel-Intersil's ADC-HZ 12 bit A/D converter (which offers 8 μsec maximum conversion time).

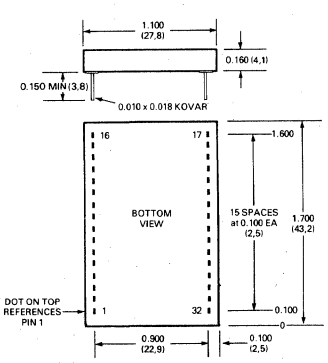
The sample-hold is cased in a 32-pin ceramic package. Models are available in three operating temperature ranges: 0 to +70, -25 to +85, and -55 to +100 degrees centigrade. High reliability versions of each model are available under Datel-Intersil's "S" program and MIL-STD-883 level B. For further information on these, contact the factory.







MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STAND OFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+IN	17	S/H STEP ADJUST.
2	-IN	18	S/H STEP ADJUST.
3	NC	19	NC
4	OFFSET ADJUST.	20	NC
5	NC	21	NC
6	OFFSET ADJ. (WIPER)	22	DIGITAL CONTROL
7	NC	23	NC
8	OFFSET ADJUST.	24	+5 VDC
9	NC	25	NC
10	ANALOG COMMON	26	POWER GROUND
11	OUTPUT	27	NC
12	NC	28	+15 VDC
13	NC	29	NC
14	C.H. (OPTIONAL)	30	NC
15	NC	31	-15 VDC
16	S/H ADJ. (WIPER)	32	NC

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SPECIFICATIONS, SHM-6

Typical at 25°C, ±15V and +5V supplies unless otherwise noted

MAXIMUM RATINGS

Positive Supply	+18V
Negative Supply	-18V
Logic Supply	+7.0V
Digital Input Voltage	+5.5V
Analog Input Voltage	±Vs
Differential Input Voltage	±30V

INPUT AMPLIFIER SPECIFICATIONS

Offset Voltage	±2 mV
Offset Voltage Tempco	±100 μV/°C
Offset Current	1 nA max.
Offset Current vs. Temp.	Doubles every 10°C
Bias Current	10 nA max.
Input Resistance	$10^8\Omega$
Common Mode Voltage Range	±10V min.
Common Mode Rejection Ratio	74 dB min.
Open Loop Gain	10^6V/V
Gain Bandwidth Product	5MHz
Power Supply Rejection Ratio	0.004%/% Supply

DIGITAL INPUT CHARACTERISTICS

Digital Control Logic	DTL, TTL
Input Logic Level, Sample Mode	0V to +0.8V @ -3.2 mA
Input Logic Level, Hold Mode	+2.0V to +5.0V @ +80μA

ANALOG OUTPUT CHARACTERISTICS

Output Voltage Range	±10V min.
Output Current	±50 mA max.
Output Resistance	0.1Ω max.

SAMPLE HOLD CHARACTERISTICS (Noninverting unity gain)

Acquisition Time, 10V Step to 0.1%	800 nsec. max.
Acquisition Time, 10V Step to 0.01%	1 μsec. max.
Aperture Delay Time	20 nsec.
Aperture Uncertainty Time	2 nsec.
Sample to Hold Error	Adjustable to Zero
Hold Mode Voltage Droop	10 μV/μsec. max.
Hold Mode Feedthrough	0.01% max.
Offset	Adjustable to Zero
Gain	±1 to ±10
Gain Error	0.01% max.
Nonlinearity, V_{OUT} = ±10V	0.01% max.
Full Power Bandwidth, V_{OUT} = ±10V	500 KHz
Slew Rate	40V/μsec.

POWER REQUIREMENTS

Positive Supply	+15 VDC ±0.5V @ 55 mA
Negative Supply	-15 VDC ±0.5V @ 60 mA
Logic Supply	+5 VDC ±0.5V @ 30 mA

PHYSICAL-ENVIRONMENTAL

Operating Temperature Ranges	
SHM-6MC	0°C to +70°C
SHM-6MR	-25°C to +85°C
SHM-6MM	-55°C to +100°C
Storage Temperature Range	-65°C to +150°C
Package Type	32 Pin Ceramic
Pins	Kovar (.010 x .018)
Weight	0.5 Oz (14g)

TECHNICAL NOTES

1. It is essential that the +15V, -15V and +5V supplies, pins 28, 31 and 24 respectively, each be bypassed to ground with a 0.1 μF ceramic capacitor connected as close to the pins as possible.
2. Digital Common, pin 26, and Analog Common, pin 10, are not connected together internally, therefore they must be connected externally as directly as possible. It is strongly recommended that a ground plane be run underneath the case between the two commons. Analog ground and ±15V power ground should be run to pin 10, digital ground and +5V power ground should be run to pin 26.
3. An external holding capacitor can be added to decrease hold mode voltage droop but with consequently longer acquisition time. For temperatures up to +85°C, polystyrene capacitors are recommended; for higher temperatures, polypropylene or teflon capacitors should be used.
4. In the inverting unity gain operating mode, the feedback and input resistors should be carefully matched or trimmed to yield the desired gain of one. In general, the operating parameters are the same as in the noninverting unity gain configuration, except that the sampling bandwidth is reduced by a factor of two. For applications of the SHM-6 with gain greater than one, sampling bandwidth is inversely proportional to gain.
5. Capacitive loads on the output should be limited to 100 pF to maximize acquisition time. The SHM-6 has a ±50 mA current drive capability.
6. This device dissipates approximately 2 watts of power due to the transconductance amplifier. The case to ambient thermal resistance is approximately 25°C per watt. For ambient temperatures above +50°C, care should be taken to maintain air circulation in the vicinity of the case.
7. The adjustment procedures for the SHM-6 are as follows. Ground the input pin and connect the output to a D.V.M., operate the offset adjustment potentiometer to yield an output of zero as read on the D.V.M. The sample-hold step adjustment is performed with the input pin grounded and the output connected to an oscilloscope set to 1 mV/cm sensitivity. The digital input pin is driven with a compatible square wave at approximately 250 KHz and the sample-hold step adjustment potentiometer is operated to produce a flat-line output on the oscilloscope.

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	SEAL
SHM-6MC	0°C to +70°C	Hermetic
SHM-6MR	-25°C to +85°C	Hermetic
SHM-6MM	-55°C to +100°C	Hermetic

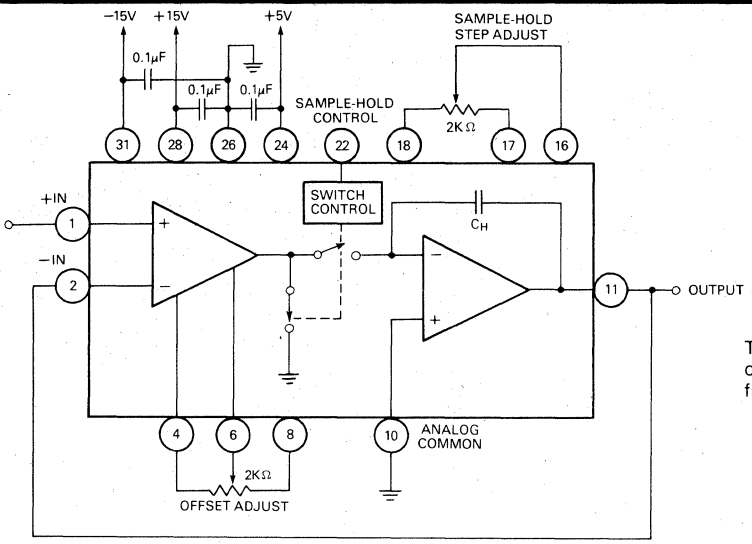
Trimming Potentiometers TP2K
(2 Required Per SHM-6)

DILS-2 Mating Socket
(2 Required Per Sample-Hold)

For High Reliability versions of the SHM-6, including units screened to MIL-STD-883, Level B, contact the factory.

THESE SAMPLE-HOLDS ARE COVERED BY GSA CONTRACT.

OPERATING MODES

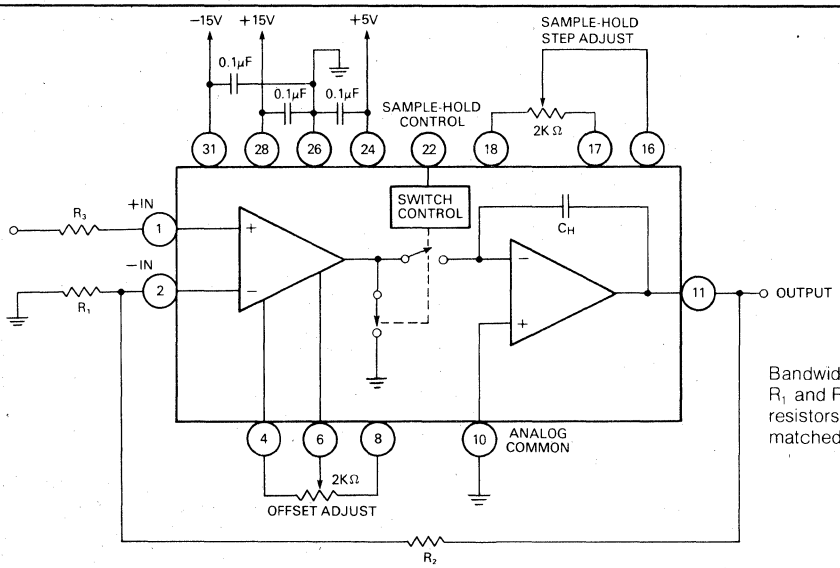


SAMPLE-HOLD

NONINVERTING

GAIN = +1

The zKΩ offset trimming potentiometers should be of the 100PM/° C cermet type. These are available from Datel-Intersil as model TP2K

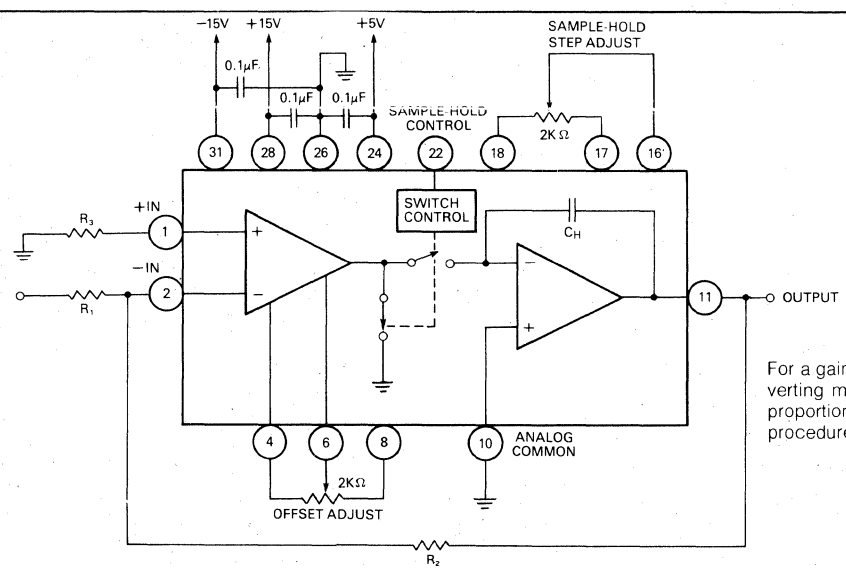


SAMPLE-HOLD

NONINVERTING

$$\textbf{GAIN} = 1 + \frac{R_2}{R_1}$$

Bandwidth decreases proportionately with gain. Resistors R_1 and R_2 should be 100PPM/°C or better, metal film type resistors. The indicated ratio between R_1 and R_2 should be matched as closely as possible and trimmed if necessary.



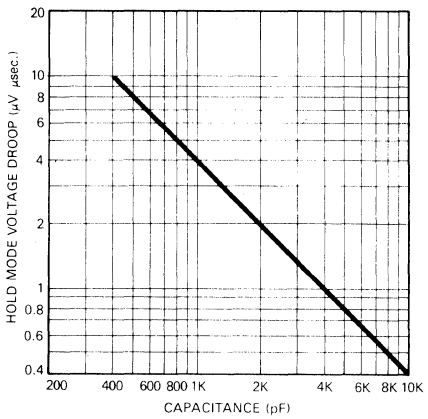
SAMPLE-HOLD

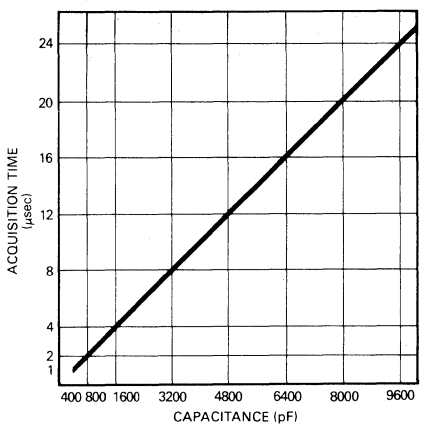
INVERTING

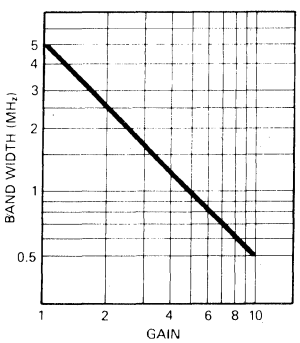
$$\textbf{GAIN} = -\frac{R_2}{R_1}$$

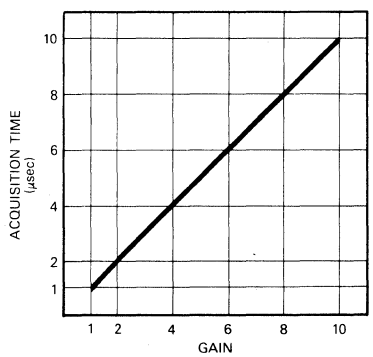
For a gain of -1 the bandwidth is one half that of the noninverting mode, for higher gains the sampling bandwidth is proportionately reduced. The above-mentioned matching procedures should be followed.

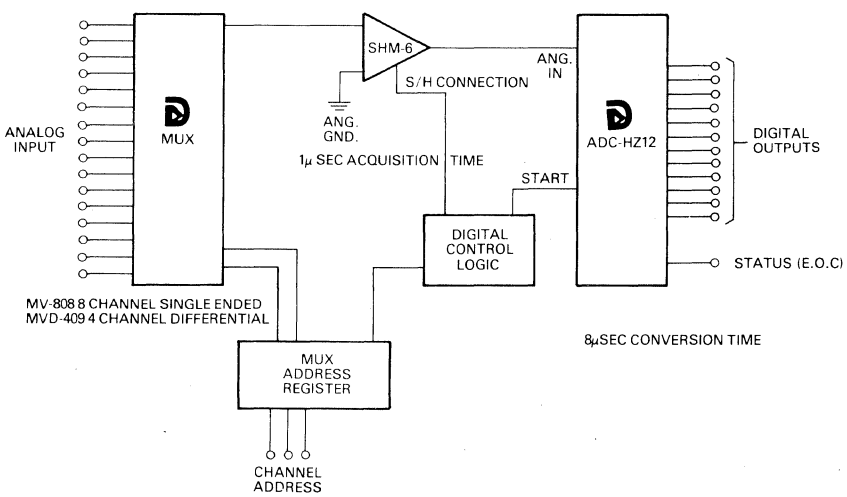
TYPICAL PERFORMANCE
(Noninverting unity gain at 25°C, ±15V and +5V supplies unless otherwise noted)











A high speed data acquisition system employing the SHM-6. This system is capable of a 110 KHz throughput rate with 12 bit resolution. In this system the SHM-6 is used with Datel-Intersil's ADC-HZ12, a high-speed hybrid 12 bit A/D converter, and Datel's MV-808, a low cost monolithic analog multiplexer. Use of a low on-resistance MUX is recommended, so that the time constant formed by MUX on-resistance and bus capacitance does not limit the acquisition performance of the SHM-6.

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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Ultra-High Speed Sample-Holds SHM-UH Series

FEATURES

- **10 MHz Sampling Rate**
- **30 nsec Acquisition Time**
- **30 psec Aperture Uncertainty**
- **Diode Bridge Switch**
- **45 MHz Bandwidth**

GENERAL DESCRIPTION

The SHM-UH series is comprised of two ultra-fast sample-holds specifically designed for use with Datel-Intersil ACD-UH series, or other ultra-fast 6, 8 and 10 bit A/D converters. Both models in this series use an open loop design optimized for ultra-high speed operation. This design consists of an ultra-fast input buffer amplifier, a transformer driven diode bridge switch, and a high impedance output buffer amplifier.

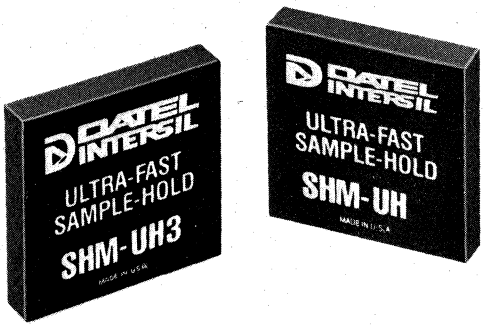
The unique pulse transformer driven diode bridge switch is a key design feature in attaining a 30 nsec. acquisition time for a 10V signal change. This switch also holds aperture uncertainty time to less than 30 picoseconds for the SHM-UH3 and less than 200 picoseconds for the SHM-UH.

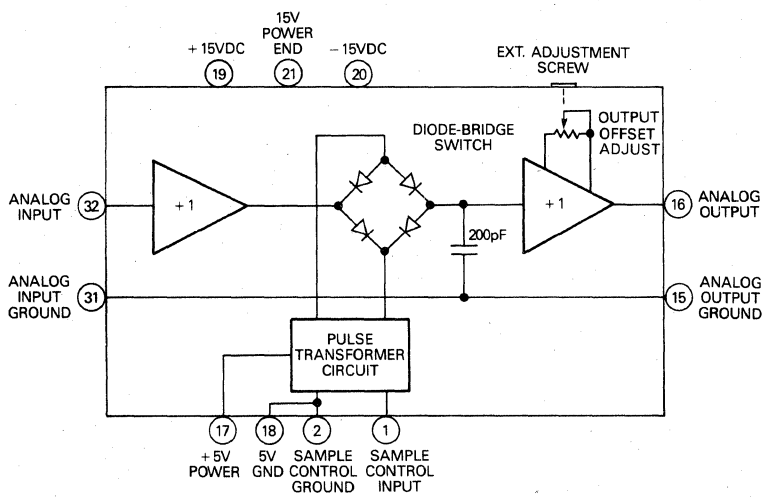
The SHM-UH3 is the newest member of this series and embodies substantial performance improvements on an already high performance design. This model is recommended for inclusion in new design applications. In addition to a 30 nsec acquisition time with only 30 picoseconds of aperture uncertainty, linearity is 0.05% of full scale and hold-mode feedthrough is -66 dB for inputs from DC to 10 MHz. The SHM-UH3 utilizes all hermetically sealed semiconductors in its design.

The SHM-UH is the lower cost version of the series. An acquisition time of 50 nsec, aperture uncertainty of less than 200 picoseconds, and linearity of 0.25% make this model well suited to use with ultra-high speed A/D converters with up to 8 bits resolution.

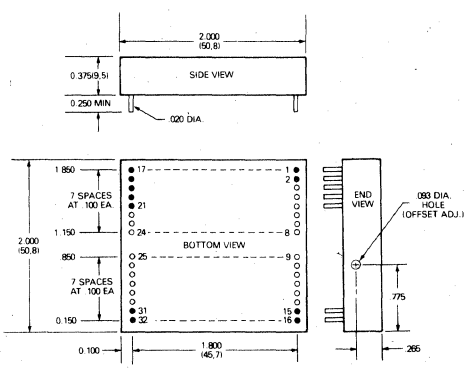
Both models have sample-mode bandwidths of 45 MHz, output slew rates of 500V/μsec and output current drive capabilities of ±30 mA. Each has an output offset adjustment accessible from the side of the module.

These sample-holds are encapsulated in 2 × 2 × 0.375 inch (51 × 51 × 5 mm) cases with dual-in-line pinning compatibility. Power requirements are ±15 VDC and +5 VDC. Standard versions operate over a temperature range of 0 to +70°C with extended temperature range versions also available.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	SAMPLE CONTROL IN
2	SAMPLE CONTROL GND
15	ANALOG OUTPUT GND
16	ANALOG OUTPUT
17	+5V POWER
18	5V POWER GND
19	+15V POWER
20	−15V POWER
21	15V POWER GND
31	ANALOG INPUT GND
32	ANALOG INPUT

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SPECIFICATIONS, SHM-UH SERIES
(Typical at 25°C and ±15 VDC and +5 VDC Supplies, unless otherwise noted)

	SHM-UH	SHM-UH3
MAXIMUM RATINGS[1]		
Analog Input Voltage	±15V	±5.5V
Sample Control Input Voltage	+5.5V	+5.5V
Sample Pulse Width[7]	70 nsec	100 nsec
Analog Supply Voltage	±18V	±18V
Digital Supply Voltage	+5.5V	+5.5V
INPUTS		
Input Voltage Range	±5V	±5V
Input Impedance	100 Meg	100k
Input Bias Current	50 pA[2]	±20 μA
Sample Control Pulse	+5V @ 130 mA	+3.5 @ 60 mA
Sample Control Pulse Width	40 ±10 nsec.	35 ±10 nsec.
Sample Control Input Impedance	50Ω	50Ω
Sample Pulse Rise or Fall Time	3 nsec, max.	3 nsec, max.
OUTPUTS		
Output Voltage Range, min.	±5V	±5V
Output Current, max.	±30 mA	±30 mA
Output Impedance, DC	3Ω	3Ω
Output Load[3]	500Ω	500Ω
Maximum Capacitive Load	100 pF	100 pF
PERFORMANCE		
Gain	+0.92 to +0.95	+0.95 to +0.98
Linearity Error, % of Full Scale	±0.25%, max.[9]	±0.05%, max.
Output Offset Voltage, Hold Mode	Adj. to Zero	Adj. to Zero
Output Offset Voltage Drift	±50 μV/°C	±50 μV/°C
Hold Mode Droop	50 μV/μsec	50 μV/μsec
Hold Mode Feedthrough[4]	-50 dB @ 10 MHz	-66 dB, DC to 10 MHz
Analog Supply Rejection	6 mV/V	25 mV/V
DYNAMIC RESPONSE		
Acquisition Time	50 nsec[5]	30 nsec
Acquisition to Output Time[11]	70 nsec	50 nsec
Hold Mode Settling Time	20 nsec	20 nsec
Bandwidth, Sample Mode	45 MHz	45 MHz
Output Slew Rate	500V/μsec	500V/μsec
Aperture Delay Time	12 nsec[6]	12 nsec[8]
Aperture Uncertainty Time	200 psec	30 psec
Sampling Rate, max.	10 MHz[10]	10 MHz[10]

POWER REQUIREMENT	
Analog Power Supply	±15 VDC ±0.2 VDC @ 50 mA
Digital Power Supply	+5 VDC ±0.25 VDC @ 100 mA
PHYSICAL-ENVIRONMENTAL	
Operating Temp. Range	0°C to +70°C
Storage Temp. Range	-55°C to +85°C
Relative Humidity	Up to 100% Non-condensing
Case Size	2 × 2 × 0.375 inches (50,8 × 50,8 × 9,5 mm)
Case Material	Black Diallyl Phthalate, per MIL-M-14
Pins	0.020" Dia, Gold Plated 0.25" Long, min.
Weight	3 oz. (85g)

NOTES:
1. Maximum ratings represent the limits of device operation without damage. The devices should not be operated at these limits.
2. 150 pA max @ 25° C. Doubles every 10° C (SHM-UH Only).
3. For full scale signal outputs. For small signal outputs (±1V), output load resistance must be decreased to 100Ω.
4. See Feedthrough Attenuation Graph.
5. Model SHM-UH requires three sampling pulses to acquire a full scale signal change.
6. For the SHM-UH this will vary by ±2 nsec max. with temperature.
7. See Technical Note 10.
8. This may vary between units by 3 nsec.
9. For input signal changes of ±1.25V max., larger input signal changes require additional sample pulses and settling time. See Technical Note 9.
10. 30 nsec sampling pulses with 70 nsec between pulses.
11. See Technical Note 4.

TECHNICAL NOTES

1. These devices are true sample-holds, rather than track and holds, in that they take an "instantaneous" sample of the input signal rather than continuously track it and hold on command. The extremely high speed available with this series allows a close approximation to sampling period of the ideal zero-order hold. Design considerations necessary to attain this level of performance place a limit on long-term holding ability. A/D converters used with these sample-holds should be selected for compatible speed and accuracy.

2. Aperture uncertainty time is a measurement of the time uncertainty or jitter of the actual point in time of the switch change to the off state. It is an indication of the repeatability of the switch characteristics. This time should not be confused with the aperture delay time which is a fixed delay and can be compensated for.

3. Acquisition time is the time required, after the sampling switch is closed, for the hold capacitor to charge to a full scale voltage change and remain within a specified error band around the final value.

4. Acquisition to output time is defined as the period from the receipt of the sample command until the output of the sample-hold has settled to within a specified error band of its final value. This is the operating period of the sample-hold, including all internal delays and settling time, and consequently defines the total time required for a single sample-hold operation.

5. Digital and analog grounds are not connected internally. When using these sample-holds with A/D converters, good design practice dictates the connection of analog and digital grounds from both devices at one point, preferably at the A/D converter to avoid ground loops. Use of a ground plane is recommended for best performance.

6. For Model SHM-UH only, hold mode droop is from the held value of the analog input signal toward the signal level at the input. The droop experienced is also dependent on input signal characteristics and is related to the feedthrough attenuation characteristics. The combination of these factors may cause the observed hold mode voltage droop to be significantly less than 50 μV/μsec for some applications, e.g., droop is zero for a constant input signal. In the case of Model SHM-UH3, droop is independent of feedthrough.

7. For both the SHM-UH and the SHM-UH3 input sources should be purely resistive.

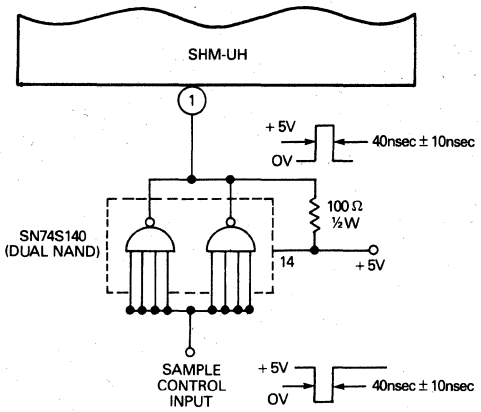
8. Input overvoltage protection may be added to the SHM-UH3 by connecting diodes from the analog input and the analog input ground to the +5V and -5V supplies, see "Input Protection" diagram.

9. To acquire full scale input signal changes, the SHM-UH requires three sampling pulses with a 100 nsec. settling time allowed between each to acquire full scale input changes to rated linearity.

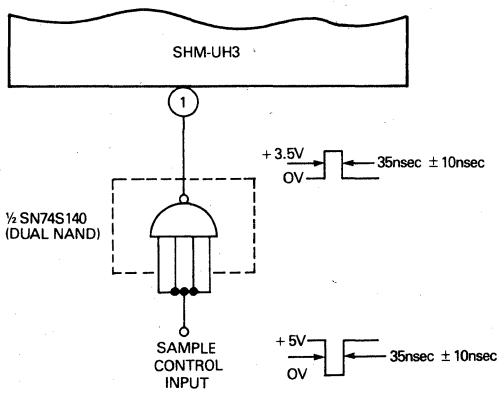
10. Sample pulse widths greater than those specified under MAXIMUM RATINGS will give unsatisfactory performance due to drive transformer saturation. For Model SHM-UH3, excessive pulse widths will result in the sample-hold returning to the hold mode before the sample control input is taken low. Model SHM-UH may be damaged by exceeding sample pulse width limits.

APPLICATION

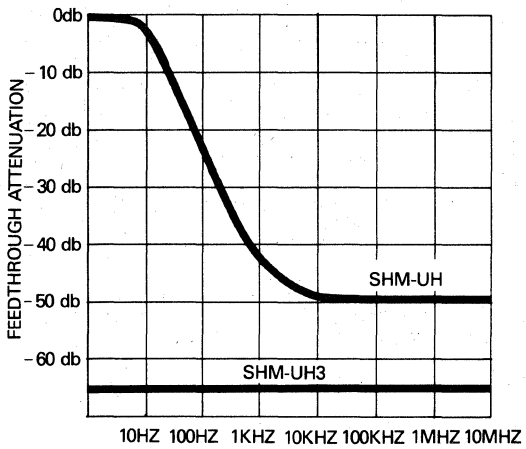
SAMPLE CONTROL INTERFACE SHM-UH



SAMPLE CONTROL INTERFACE SHM-UH3



HOLD MODE FEEDTHROUGH ATTENUATION



HOLD-MODE FEEDTHROUGH IS A PHENOMENA THAT OCCURS AFTER THE SWITCH HAS BEEN OPENED AND THE SIGNAL IS BEING HELD. A SMALL PART OF THE SIGNAL ON THE INPUT WILL BE COUPLED TO THE OUTPUT.

ORDERING INFORMATION

MODEL	DESCRIPTION
SHM-UH	50 nsec, 0.25%
SHM-UH3	30 nsec, 0.05%

Mating Socket DILS-2, 2 req'd/Module

For extended temperature range operation the following suffixes should be added to the model number. Consult Factory for Price and Delivery.

-EX	-25°C to +85°C Operation
-EXX-HS	-55°C to +85°C Operation, with all hermetically sealed semiconductor components.

THESE SAMPLE-HOLDS ARE COVERED BY GSA CONTRACT

ADJUSTMENT PROCEDURE

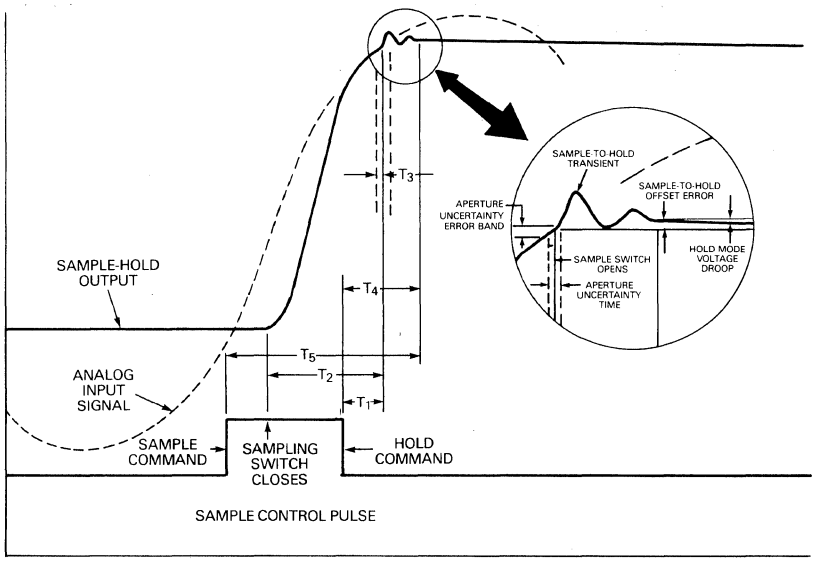
1. Connect the Analog Input (pin 32) to the Analog Input Ground (Pin 31).
2. Connect a precision pulse generator with negative going output pulses via a terminated coaxial cable to the Sample Control Input (pin 1) and the Sample Control Ground (pin 2). Use the sample control interface shown in the applicable diagram.
3.

Pulse Repetition Rate	50 KHz
Pulse Width	40 nsec
Pulse Amplitude	+5V

   Note: Sample Control Input Impedance is 50 Ohms
4. Connect a precision digital voltmeter to the Analog Output (pin 16) and the Analog Output Ground (pin 15).
5. Adjust the Offset Adjust Potentiometer (accessible through side of case) until the digital voltmeter reads 0.0000V.

APPLICATION

SAMPLE-HOLD DEFINITIONS



T_1, **APERTURE DELAY TIME**
The period between the receipt of the hold command and opening of the sampling switch. Due to sampling switch characteristics, the measurement of this period contains a small amount of uncertainty, i.e., the actual point in time of the opening of the sampling switch will vary by a small amount with each operation. This variance falls within a narrow time range which is specified as the aperture uncertainty time (see definition below).

T_2, **ACQUISITION TIME**
The time required, after the closing of the sampling switch, for the hold capacitor to charge to a full scale voltage change and then remain within a specified error band around the final value.

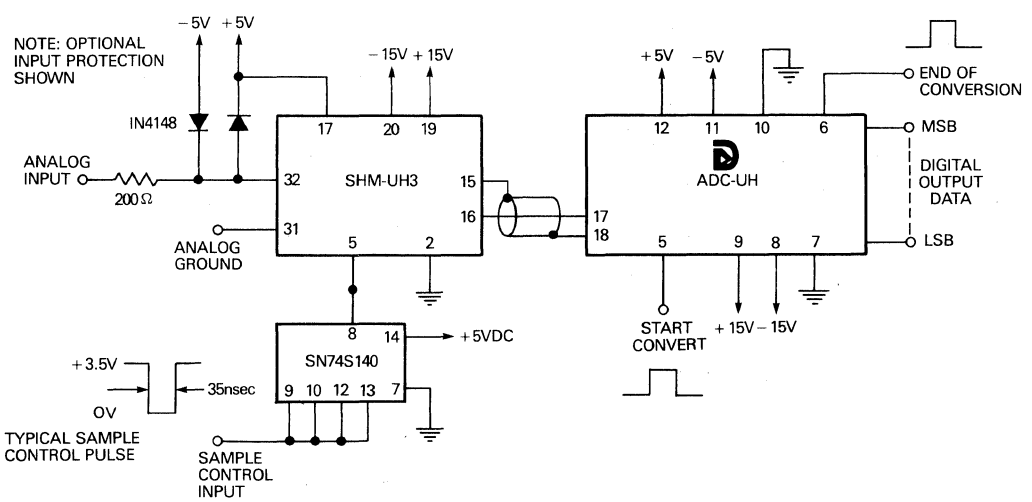
T_3, **APERTURE UNCERTAINTY TIME**
The time variation, or jitter, in the opening of the sample switch.

APERTURE UNCERTAINTY ERROR
An amplitude uncertainty in the held value due to the change in the analog input signal during the aperture uncertainty time. This error is the product of the rate of change of the input signal and the aperture uncertainty time. Therefore, small values of aperture uncertainty time yield small values of aperture uncertainty error.

T_4, **HOLD MODE SETTLING TIME**
The time from the hold command transition until the output has settled within a specified error band around the final value.

T_5, **ACQUISITION TO OUTPUT TIME**
The time from the receipt of the sample command until the output of the sample-hold has settled within a specified error band around the final value.

SHM-UH3 AND ADC-UH8B CONNECTION



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Ultra Fast Accurate Analog Storage Sample & Hold Models SHM-2,SHM-2E

FEATURES

- Ultra Fast Acquisition Time
- Short Aperture Time
- Wide Frequency Response
- Fast Output Settling
- Low Temperature Coefficient

DESCRIPTION

Model SHM-2 Sample and Hold is the ultimate in speed. Designed to operate in conjunction with Datel Intersil's analog to digital converters, SHM-2 can track a full scale analog input in less than 100 nsec's to within ±0.1% of full scale accuracy. Additional features include wide frequency response (D.C. to 500 KHz), an aperture uncertainty of less than 10 nsec's and an output settling time of one μsec to within ±0.1%.

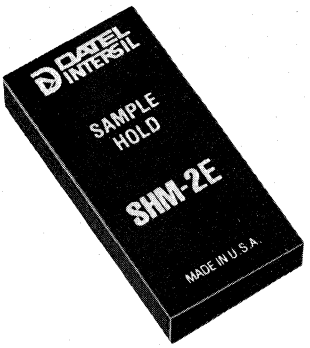
SHM-2 is usually connected between a signal source to be quantized and analog to digital converter, providing an excellent throughput rate for an overall data system.

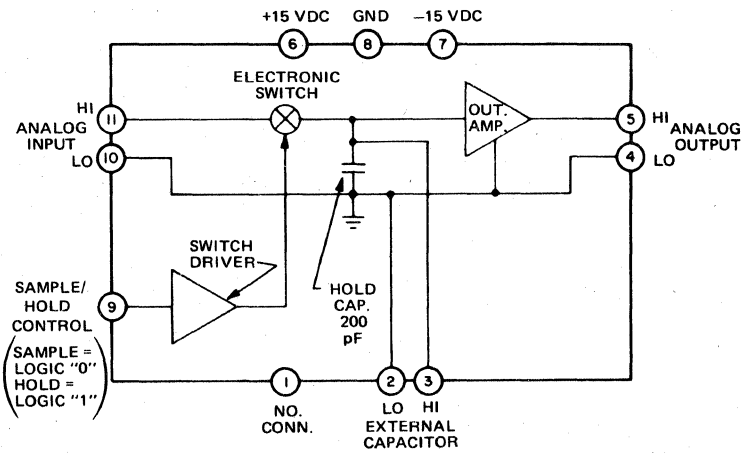
APPLICATION

When digitizing an analog signal which varies with time and having a frequency spectrum, it is difficult to determine what point of this signal is exactly represented by the resultant digital output. Since the maximum time "uncertainty" of the conversion is the total conversion time of the converter which may be called "aperture time or ambiguity time"; therefore, the maximum error due to this uncertainty is the difference of two points of the analog signal under measurement from T_0 to time, T_1 representing the time required to convert the changing analog signal.

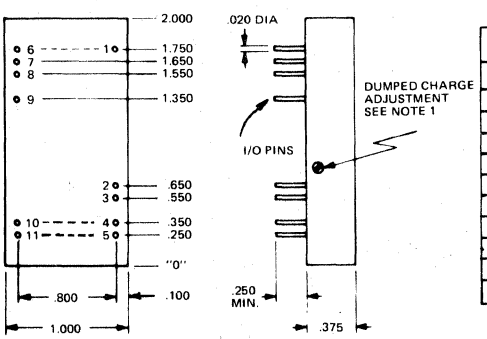
A faster converter will obviously shorten the aperture and the error will be reduced proportionately, but a device such as the SHM-2 with very narrow aperture characteristics, controlled by command, is far more useful in trying to determine the exact point of the changing analog signal when converting. The purpose of SHM-2 is to "hold" upon command at the beginning of the conversion (T_0 time) the analog voltage applied at its input. The "held" value will remain constant during the conversion process.

Relationships of error due to time uncertainty versus input frequency is plotted on the reverse side of this sheet.





MECHANICAL DIMENSIONS (INCHES)



NOTE
1. ADJUST FOR HOLD OFFSET AT V_{IN} = 0 VOLTS OR GROUNDED ANALOG INPUT.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	NO CONNECTION
2	LO EXTERNAL CAPACITOR
3	HI EXTERNAL CAPACITOR
4	LO ANALOG OUTPUT
5	HI ANALOG OUTPUT
6	+ 15 V POWER IN
7	− 15 V POWER IN
8	GROUND
9	SAMPLE/HOLD CONTROL
10	LO ANALOG INPUT
11	HI ANALOG INPUT

USE POLYSTYRENE TYPE CAPACITOR

SPECIFICATIONS (Typical @ 25°C unless noted)

ELECTRICAL

Analog Input:

Analog input voltage range . . . Up to ±10 VFS

Input overvoltage . . . . . ± 15V (max.) with a recovery time of 500 nsec

Input source current . . . . . ±12mA max drive during transition ±2mA bias during steady state. (Switching circuit is a diode bridge driven by 2 current sources.)

Mode control input . . . . . DTL or TTL compatible, positive logic

Status	Input Code	Vinput Min.	Vinput Max.
Sample	"0"	0V	+0.8V
Hold	"1"	+2.0V	+5.5V

Rise and Fall time ⩽ 10 nsec to maintain aperture time spec s.

Analog Output

Output voltage range . . . . . Up to ±10 VFS

Output current . . . . . ±5 mA, SHM-2
±10 mA, SHM-2E

Dynamic Characteristics:

Bandwidth . . . . . DC to 500 KHz (max.) full power @ 3 db point

Acquisition time . . . . . 100 nsec (max.) to ± 0.1% of FS of input signal (5V step)

Aperture time . . . . . 10 nsec max. (8 nsec delay, 2 nsec jitter)

Feedthrough @ any input frequency 0.5%

Settling time . . . . . 1 μsec (max.) to ±0.1%, SHM-2 (10V step)
400nsec (max.) to ±0.1% SHM-2E (10V step)

Hold decay rate . . . . . 50 μV/μsec, SHM-2

Output slewing rate 250V/μsec, SHM-2E

Performance:

Gain . . . . . + 1.00 Max. to +0.999 Min

Accuracy (@ 25°C) . . . . . **± 0.1% of FS**

Linearity . . . . . ±0.1% of FS

Temperature coefficient . . . . . ±30 ppm/°C of FS

Long term stability . . . . . ±0.025%/6 months (gain & offset)

Input power requirements . . . . +15±.5VDC @ 35 ma
−15±.5VDC @ 35 ma

PHYSICAL-ENVIRONMENTAL

Operating temperature range . . 0°C to +75°C

Storage temperature range . . . . −55°C to +85°C

Relative humidity . . . . . Up to 100% non-condensing

Size . . . . . 2"L x 1"W x 0.375"H plug-in module

Pins . . . . . 0.020" round gold plated 0.250" long minimum

Case material . . . . . Black diallyl phthalate, per MIL-M-14. Fully repairable

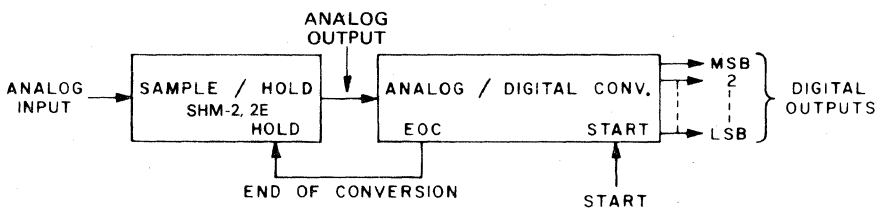
Weight . . . . . 2 oz.

Model SHM-2. . . . . .
Model SHM-2E. . . . . .

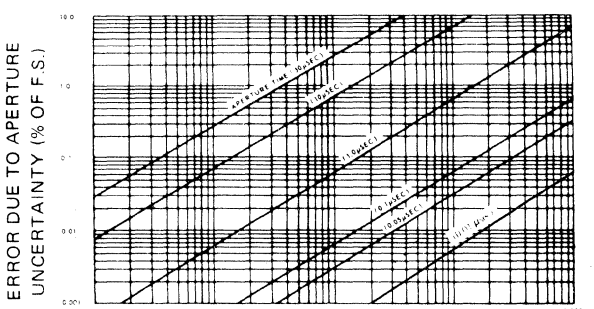
Mating Socket . . . . . DILS-2, 2 Req'd. . . . . .

Model SHM-2 and SHM-2E sample and hold modules are fully encapsulated and feature dual in-line pinning compatibility (i.e., 0.100" grid pin spacing and 0.800" between rows of pins).

TYPICAL SYSTEM CONFIGURATION



ERROR DUE TO TIME UNCERTAINTY (APERTURE TIME)
AS A FUNCTION OF INPUT SIGNAL FREQUENCY



TYPICAL EXAMPLE

ANALOG DIGITAL CONV. W WO SAMPLE & HOLD

FULL SCALE ACCURACY	WITH S & H (10 NANOSEC APERTURE)	WITHOUT S & H (20 μsec CONVERSION TIME)
.06%	10 KHz (MAX. INPUT FREQUENCY)	400 Hz (MAX. INPUT FREQUENCY)
.01%	2000 Hz (MAX. INPUT FREQUENCY)	1 Hz (MAX. INPUT FREQUENCY)

THESE SAMPLE HOLDS ARE COVERED BY GSA CONTRACT

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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Ultra-Fast, .01% Sample-Hold
Model SHM-5

FEATURES

- **200nSec. Acquisition to 0.1%**
- **350nSec. Acquisition to .01%**
- **5MHz Bandwidth**
- **.005% Linearity**
- **250 pSec. Aperture Uncertainty**

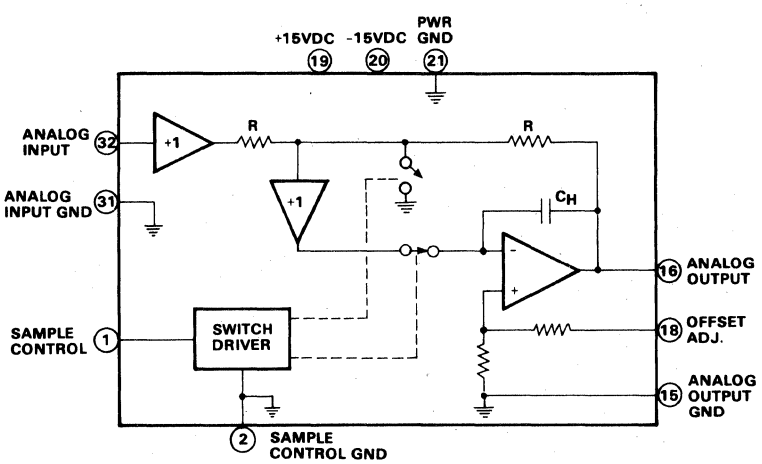
GENERAL DESCRIPTION

Model SHM-5 is a new, ultra-fast acquisition sample-hold module for use with high speed 10 and 12-bit A/D converters. When used with Datel-Intersil's model ADC-EH12B3, a 12-bit 2 μsec, A/D, the SHM-5 permits sampling and conversion at rates up to 425 kHz. The key circuit element in the SHM-5 is an ultra-fast settling hybrid operational amplifier manufactured in Datel's thin-film hybrid facility. This amplifier operates in the inverting mode as a hold amplifier. A fast FET sampling switch operates between two virtual ground points in order to keep switching errors small and independent of signal level. A second FET switch operates out-of-phase with the first one to minimize signal feedthrough errors.

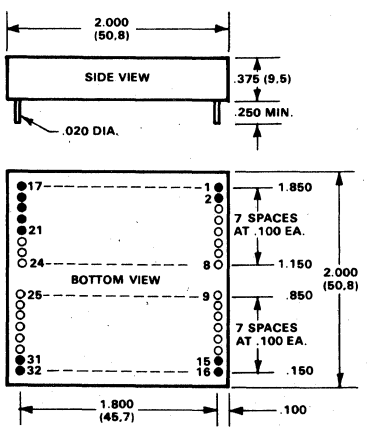
The SHM-5 is designed primarily for fast track & hold and simultaneous sampling applications with A/D converters. From the tracking mode it realizes acquisition times of 200 nsec. to 0.1% or 350 μsec. to 0.01% for a 10V change. When the input buffer amplifier must also make a 10V change, as in multiplexer applications, the total acquisition time is 1 μsec. to 0.01%.

The SHM-5 operates in the inverting mode with a gain of -1 and an input impedance of 10^8 ohms. Dynamic characteristics include a 5 MHz small signal bandwidth, and 25V/μsec. slew rate in the sampling (tracking) mode. When acquiring a new sample, however, the internal slew rate across the holding capacitor is 200V/μsec. Aperture delay time is 20 nanoseconds and aperture uncertainty time is 250 picoseconds.

This device is packaged in a 2 x 2 x 0.375 inch epoxy encapsulated module. Operating temperature range is 0°C to 70°C and power requirement is ±15VDC at 75 mA maximum. Model SHM-5 is pin compatible with Datel-Intersil's model SHM-UH3.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	SAMPLE CONTROL
2	SAMPLE CONTROL GND
15	ANALOG OUTPUT GND
16	ANALOG OUTPUT
17	NO CONNECTION
18	OFFSET ADJ.
19	+15V POWER
20	-15V POWER
21	POWER GND
31	ANALOG INPUT GND
32	ANALOG INPUT

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, SHM-5

(Typical at 25°C, ±15V supply unless otherwise noted)

INPUTS	
Input Voltage Range	±10V min.
Input Overvoltage, no damage	±15V
Input Impedance	10^8 ohms
Input Bias Current	250nA max.
Sample Control, sample mode	+2.0 to +5.5V
hold mode	0V to +0.8V
Sample Control Loading	+1mA
Offset Adjustment Range	±300mV
OUTPUT	
Output Voltage Range, min.	±10V
Output Current, S.C. protected	±40mA
Output Impedance	0.1 Ωmax.
PERFORMANCE	
Gain	−1.000±0.1%
Gain Temp. Coefficient	±15ppm/°C max.
Output Offset Voltage, sample mode	±50mV max.
Output Offset Voltage Drift	±30μV/°C max.
Sample to Hold Offset Error	±5mV max.
Tracking Nonlinearity	±.005% max.
Hold Mode Droop	20μV/μsec max.
Hold Mode Feedthrough, DC-500kHz	0.02%
Output Offset vs Supply	1mV/V
DYNAMIC RESPONSE	
Acquisition Time[1], 10V to 0.1%	200 nsec. max.
Acquisition Time[1], 10V to .01%	350 nsec. max.
Acquisition Time[2], 10V to 0.01%	1.0 μsec typ., 1.5 μsec. max.
Bandwidth, tracking, −3dB	5MHz
Slew Rate, tracking	25V/μsec.
Aperture Delay Time	20nsec.
Aperture Uncertainty Time	250 psec.
POWER REQUIREMENT	
Power Supply Voltage	±15VDC ±0.5V
Quiescent Current	75mA max.
PHYSICAL-ENVIRONMENTAL	
Operating Temp. Range	0°C to 70°C
Storage Temp. Range	−55°C to +85°C.
Relative Humidity	Up to 100% non-condensing
Case Size	2.0 X 2.0 X 0.375 in, 50,8 X 50,8 X 9,5 mm
Case Material	Black diallyl phthalate per MIL-M-14
Pins	.020" round, gold plated; .25" long min.
Weight	2 oz. (57g.)

NOTES:

1. From tracking mode.
2. From input buffer.

ORDERING INFORMATION

SHM-5

Mating Socket: DILS-2 (2/module)

Trimming Potentiometer, TP20K

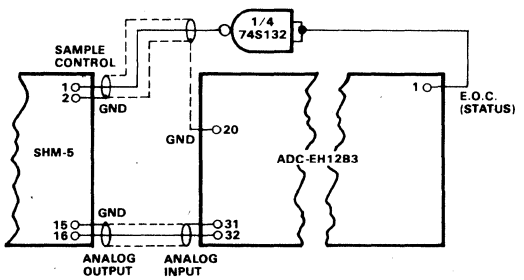
For extended temperature range operation, the following suffix is added to the model number. Consult factory for price and delivery.

−EX −25°C to +85°C operation.
−EXX-HS −55°C to +85°C with hermetically sealed semiconductor components.

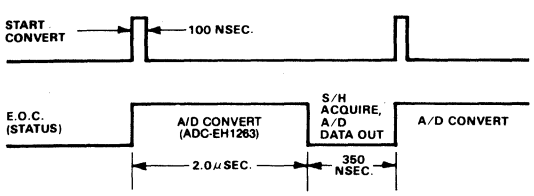
TECHNICAL NOTES

1. The SHM-5 initial gain error of ±0.1% must be adjusted out separately from the sample hold. This is most easily done by using the gain adjust of the A/D converter used with the SHM-5.
2. The maximum sample-to-hold offset error of 5mV is constant with signal level. This error can be adjusted out in the hold mode by means of the external offset adjustment shown in the diagram. It should be noted that the SHM-5 can be adjusted for zero output offset in either the sample (tracking) mode or the hold mode, but not in both at the same time.
3. The sample control input is compatible with standard TTL levels. It is recommended that this input be driven from its own active pull-up Schottky TTL circuit, such as the 74S132. This will readily supply the +1mA drive current required by the SHM-5.
4. The analog signal delay from the input of the SHM-5 to the sampling switch is approximately 32 nsec. Aperture delay is 20 nsec.
5. When the SHM-5 is switched into the hold mode, about 50 nsec. is required for the switch transient to settle. This time should be allowed for before the first A/D conversion is made.

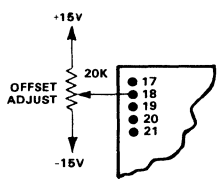
CONNECTION TO ADC-EH12B3



TIMING DIAGRAM



OFFSET ADJUSTMENT



THE SHM-5 IS COVERED BY GSA CONTRACT.

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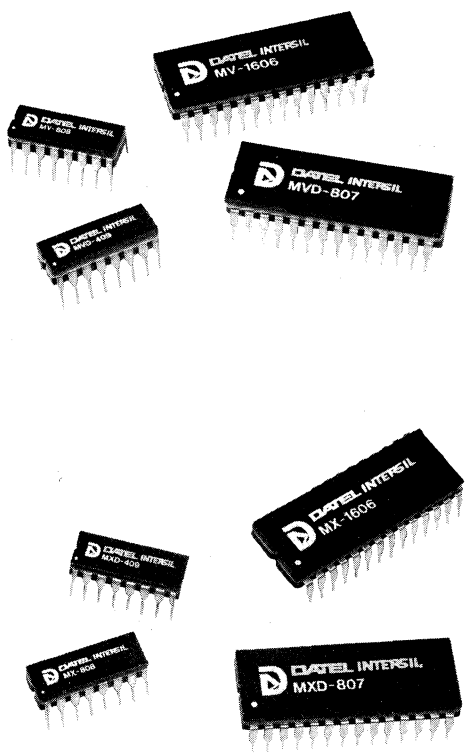
PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Analog Multiplexers



Quick Selection: Analog Multiplexers

	MODEL	FEATURES	CHANNELS NO.	CHANNELS TYPE	INPUT VOLTAGE RANGE OPER.	INPUT VOLTAGE RANGE ABS. MAX.	CHANNEL RESISTANCE ON (Ω)	TRANSFER ACCURACY	CROSSTALK
MONOLITHIC	**MX-808** **MX-808M**	Overvoltage Protection	8	Sing. End.	±15V	±35V	1.5K 1.2K	0.01%	-86 dB
	MV-808 **MV-808M**	Low ON Resistance	8	Sing. End.	±15V	±17V	250	0.01%	-86 dB
	MU-6108C **MU-6108M**	Low ON Resistance Low Leakage	8	Sing. End.	±14V	±17V	180	0.01%	—
	MX-1606 **MX-1606M**	Overvoltage Protection	16	Sing. End.	±15V	±35V	1.5K 1.2K	0.01%	-86 dB
	MV-1606 **MV-1606M**	Low ON Resistance	16	Sing. End.	±15V	±17V	270 170	0.01%	-86 dB
	MU-6116C **MU-6116M**	Low ON Resistance Low Leakage	16	Sing. End.	±11V	±16V	480	0.01%	—
	MXD-409 **MXD-409M**	Overvoltage Protection	4	Diff.	±15V	±35V	1.5K 1.2K	0.01%	-86 dB
	MVD-409 **MVD-409M**	Low ON Resistance	4	Diff.	±15V	±17V	250	0.01%	-86 dB
	MU-6208C **MU-6208M**	Low ON Resistance Low Leakage	4	Diff.	±14V	±16V	180	0.01%	—
	MXD-807 **MXD-807M**	Overvoltage Protection	8	Diff.	±15V	±35V	1.5K 1.2K	0.01%	-86 dB
	MVD-807 **MVD-807M**	Low ON Resistance	8	Diff.	±15V	±17V	270 170	0.01%	-86 dB
	MU-6216C **MU-6216M**	Low ON Resistance Low Leakage	8	Diff.	±11V	±16V	480	0.01%	—

COMMON MODE REJECTION	CHANNEL ACCESS TIME TURN ON (nSEC)	POWER REQUIREMENT	PACKAGE SIZE	PACKAGE MATERIAL	OPERATING TEMP (°C)	SINGLE PRICE	SEE PAGE
—	500	±15 VDC	16 Pin DIP	Ceramic	0 to +70 -55 to +125	**$17.50** **$57.00**	264C
—	350	±15 VDC +5V	16 Pin DIP	Ceramic	0 to +70 -55 to +125	**$16.50** **$43.00**	260C
—	300	±15 VDC	16 Pin DIP	Plastic Cerdip	0 to +70 -55 to +125	**$ 9.92** **$20.65**	236C
—	500	±15 VDC	28 Pin DIP	Ceramic	0 to +70 -55 to +125	**$29.50** **$78.50**	264C
—	300	±15 VDC	28 Pin DIP	Ceramic	0 to +70 -55 to +125	**$19.50** **$60.00**	260C
—	600	±15 VDC	28 Pin DIP	Plastic Cerdip	0 to +70 -55 to +125	**$17.80** **$56.20**	242C
120 dB	500	±15 VDC	16 Pin DIP	Ceramic	0 to +70 -55 to +125	**$17.50** **$57.00**	264C
120 dB	350	±15 VDC +5V	16 Pin DIP	Ceramic	0 to +70 -55 to +125	**$16.50** **$43.00**	260C
—	300	±15 VDC	16 Pin DIP	Plastic Cerdip	0 to +70 -55 to +125	**$ 9.92** **$20.65**	248C
120 dB	500	±15 VDC	28 Pin DIP	Ceramic	0 to +70 -55 to +125	**$29.50** **$78.50**	264C
120 dB	300	±15 VDC	28 Pin DIP	Ceramic	0 to +70 -55 to +125	**$19.50** **$60.00**	260C
—	600	±15 VDC	28 Pin DIP	Plastic Cerdip	0 to +70 -55 to +125	**$17.80** **$56.20**	254C

THESE PRODUCTS ARE COVERED BY GSA CONTRACT

Model MU-6108
CMOS 8 Channel Analog Multiplexer

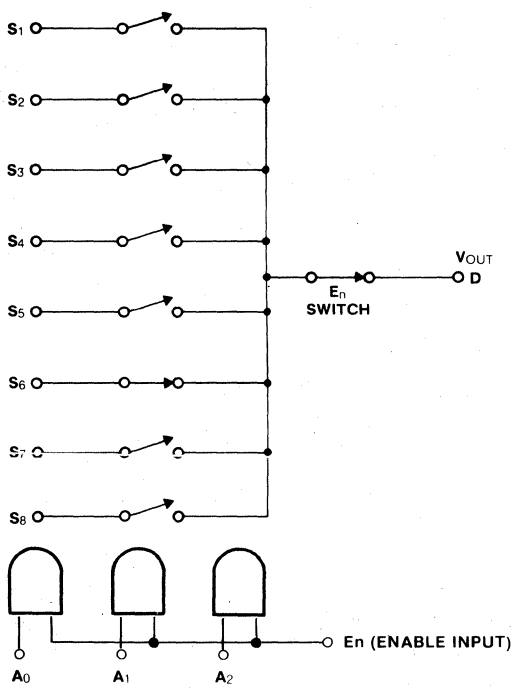
FEATURES

- **Ultra Low Leakage ≤ 100pA (Total I_{Doff})**
- **r_{on} <400 ohms over full signal and temperature range**
- **Power supply quiescent current less than 100μA**
- **±14V analog signal range**
- **No Latch up or "S.C.R." action**
- **Break before make switching**
- **Binary strobe control (3 strobe inputs control 8 channels)**
- **TTL and CMOS compatible strobe control**
- **Pin — Pin with DG508 HI-508 & AD7508**

GENERAL DESCRIPTION

The 6108 is a CMOS monolithic, one-out-of-8 multiplexer. The part is a plug-in replacement for the DG508. Three line binary decoding is used so that the 8 channels can be controlled by 3 strobe inputs; additionally a fourth input is provided to use as a system enable; if the enable input is 0V, none of the channels can be turned on. When the enable input is high (5V) the channels are sequenced by the 3 line strobe inputs. The 3 strobe inputs are controlled by TTL logic or CMOS logic elements; a "0" corresponds to any voltage less than 0.8V and a "1" corresponds to any voltage greater than 2.4V; however the enable input (En) *must* be taken to 5V to enable the system and less than 0.8V to disable the system.

FUNCTIONAL DIAGRAM



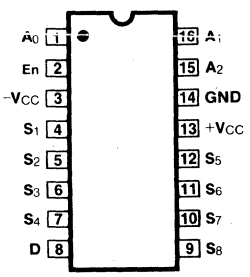
3 LINE BINARY STROBE INPUTS
(1 0 1) AND En @ 5V
ABOVE EXAMPLE SHOWS CHANNEL 6 TURNED ON.

DECODE TRUTH TABLE

A_2	A_1	A_0	En	ON SWITCH
x	x	x	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2
Logic "1" = $V_{AH} \geq 2.4V$
Logic "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION



ORDERING INFORMATION

Model	Oper. Temp. Range	Package
MU-6108C	0 to +70° C	16 pin Epoxy DIP
MU-6108M	−55 to +125° C	16 pin Cerdip

MU-6108

ABSOLUTE MAXIMUM RATINGS

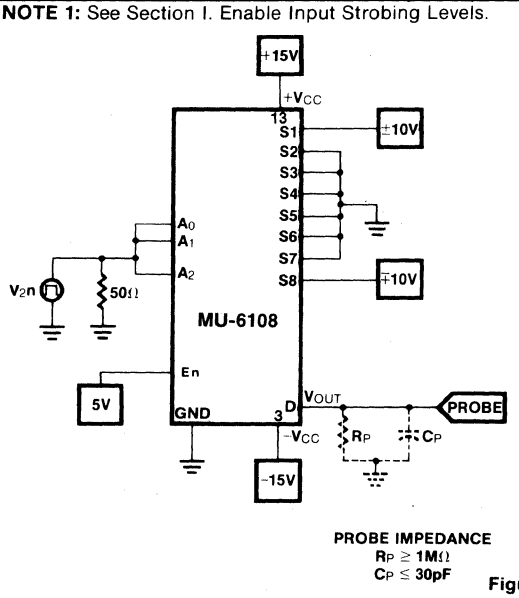
V_{IN} (A, En) to Ground ..... −15V to 15V
V_S or V_D to V_{CC} ..... 0, −32V
V_S or V_D −V_{CC} 0, 32V
+V_{CC} to Ground 16V
−V_{CC} to Ground ..... −16V
Current (Any Terminal) ..... 30 mA
Current (Analog Drain) ..... 20 mA
Current (Analog Source) ..... 20 mA
Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Power Dissipation (Package)* ..... 1200 mW

*All leads soldered or welded to PC board. Derate 10 mW/°C above 70°C.

ELECTRICAL CHARACTERISTICS

	CHARACTERISTIC	MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT	TEST CONDITIONS (UNLESS OTHERWISE NOTED) +V_{CC} = 15V, −V_{CC} = −15V, Ground = 0V V_{En} = +5V (Note 1)	
SWITCH	$r_{DS(ON)}$	S to D	8	180	300	300	400	350	350	450	Ω	V_D = 10V, I_S = −1.0mA	Sequence each switch on
			8	150	300	300	400	350	350	450		V_D = −10V. I_S = −1.0mA	$V_{A(L)}$ = 0.8V, $V_{A(H)}$ = 2.4V
	$\Delta r_{DS(ON)}$			20							%	$\Delta r_{DS(ON)} = \frac{r_{DS(ON)MAX} - r_{DS(ON)MIN}}{r_{DS(ON)AVG.}}$ −10V ≤ V_S 10V	
	$I_{S(OFF)}$	S	8	0.002		0.05	50		0.1	50	NA	V_S = 10V, V_D = −10V	V_{En} = 0
			8	0.002		0.05	50		0.1	50		V_S = −10V, V_D = 10V	
	$I_{D(OFF)}$	D	1	0.03		0.1	100		0.2	100		V_D = 10V, V_S = −10V	
			1	0.03		0.1	100		0.2	100		V_D = −10V, V_S = 10V	
	$I_{D(ON)}$	D	8	0.1		0.2	100		0.4	100		$V_{S(All)}$ = V_D = 10V	Sequence each switch on
			8	0.1		0.2	100		0.4	100		$V_{S(All)}$ = V_D = −10V	$V_{A(L)}$ = 0.8V, $V_{A(H)}$ = 2.4V
INPUT	$I_{AN(ON)}$ or	A_0, A_1 or A_2	3	.01		−10	−30		−10	−30	µA	V_A = 2.4V or 0V	
	$I_{AN(OFF)}$	Inputs	3	.01		10	30		10	30		V_A = 15V or 0V	
	I_{2n}	A_0 A_1 A_2	3			−10	−30		−10	−30		V_{En} = 5V	All V_A = 0 (Strobe pins)
		En	1			−10	−30		−10	−30		V_{En} = 0	
DYNAMIC	$t_{transition}$	D		0.3		1					µs	See Fig. 1	
	t_{open}	D		0.2								See Fig. 2	
	$t_{on(En)}$	D		0.6		1.5						See Fig. 3	
	$t_{off(En)}$	D		0.4		1							
	"OFF" Isolation	D		60							dB	V_{En} = 0, R_L = 200Ω, C_L = 3pF, V_S = 3 VRMS, f = 500 kHz	
	$C_{S(OFF)}$			5							pF	V_S = 0	
	$C_{D(OFF)}$			25								V_D = 0	V_{En} = 0V. f = 140 kHz to 1 MHz
	$C_{DS(OFF)}$			1								V_S = 0, V_D = 0	
SUPPLY	$I_{13(+V_{CC})}$	+V_{CC}	1	40		200			1000		µA	V_{En} = 5V	All V_A = 0 OR 5V
	$I_{3(-V_{CC})}$	−V_{CC}	1	2		100			1000				
	I_{13} Standby	+V_{CC}	1	1		100			1000			V_{En} = 0	
	I_3 Standby	−V_{CC}	1	1		100			1000				

NOTE 1: See Section I. Enable Input Strobing Levels.



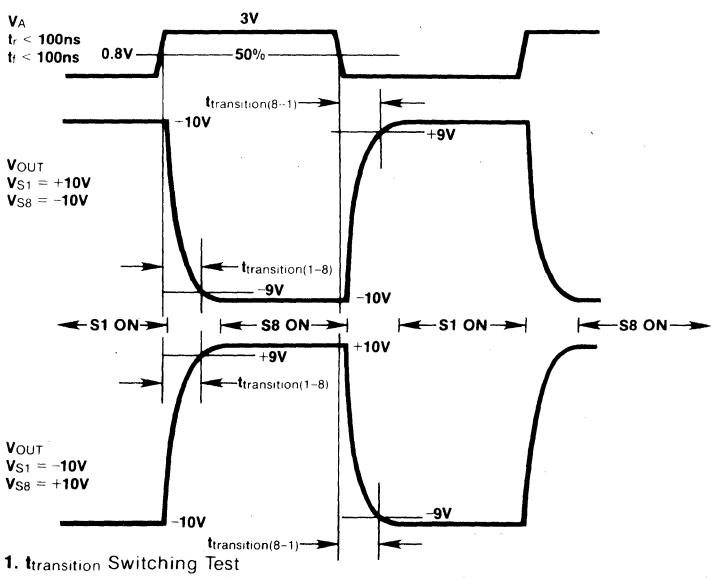


Figure 1. $t_{transition}$ Switching Test

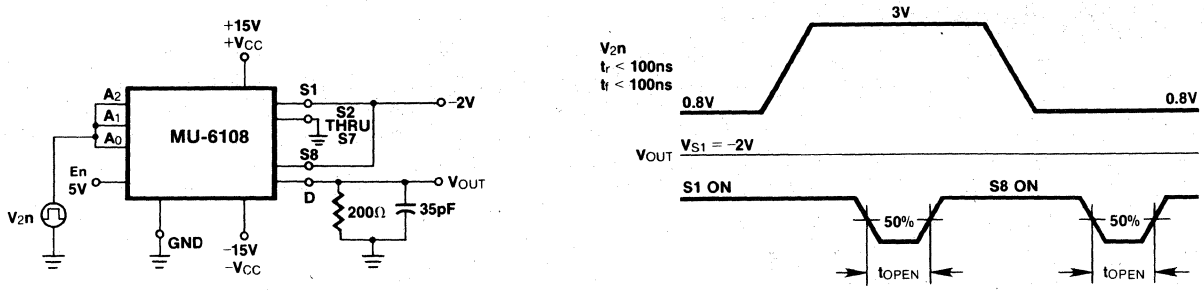


Figure 2. t_{open} (Break-Before-Make) Switching Test

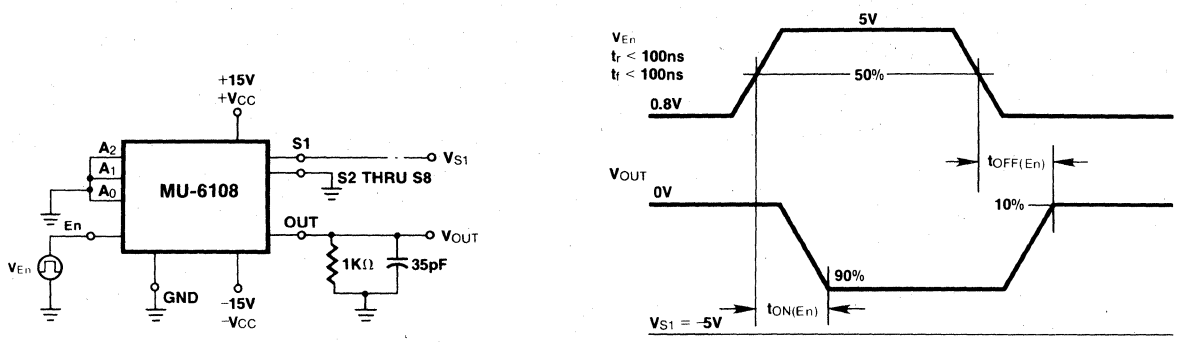


Figure 3. t_{on} and t_{off} Switching Test

MU-6108 APPLICATION INFORMATION

I. Enable Input Strobing Levels

The chip enable input on the 6108 requires a minimum of +4.5V to trigger it into the "1" state and a maximum of +0.8V to trigger it into the "0" state. If the chip enable input is being driven from TTL logic, a pull-up resistor is required from the gate output to +5V supply. The value of this resistor is not critical and can be in the 1K to 3KΩ range (See Figure 4).

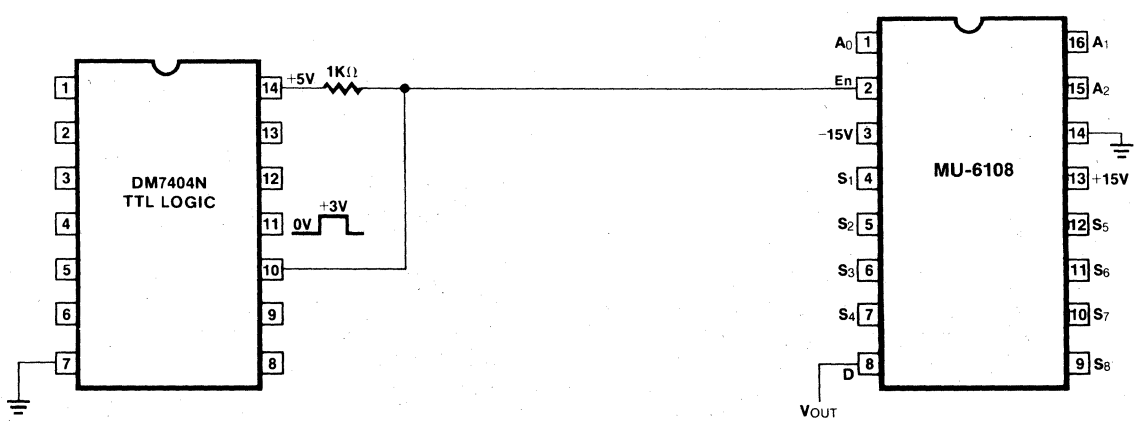


Figure 4. Enable Input Strobing from TTL Logic

MU-6108 APPLICATION INFORMATION (CONT.)

When the En input is driven from CMOS logic, no pullup is necessary. Fig. 5 shows the CD4009 driving the En input.

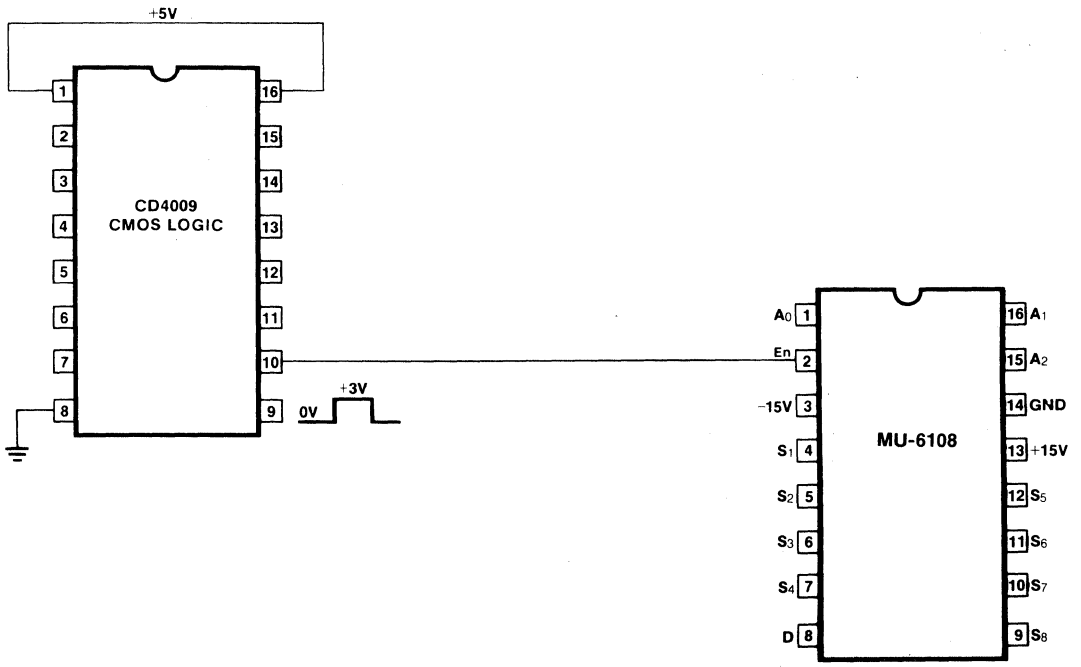


Figure 5. Enable Input Strobing from CMOS Logic

The Supply Voltage of the CD4009 does affect the switching speed of the 6108. The same is true for TTL Supply Voltage Levels The chart below shows the effect, on $t_{transition}$ times, of supply varying from +4.5V to +5.5V.

CMOS OR TTL SUPPLY VOLTAGE	TYPICAL $t_{transition}$ @ 25°C
+4.5V	400ns
+4.75V	300ns
+5.00V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the Enable Strobe Logic.

The cases shown in Figures 4 and 5 deal with enable strobing when expandability to more than eight channels is required. In these cases the En terminal acts as a fourth binary input. If eight channels or less are being multiplexed, the En terminal can be directly connected to +5V logic supply which would "enable" the 6108 at all times.

MU-6108 APPLICATION INFORMATION (CONT.)

APPLICATIONS

II. Using the MU-6108 with supplies other than ±15V

The 6108 can be used with power supplies ranging from ±6V to ±16V. The switch $r_{DS(on)}$ will increase as the supply voltages decrease. However, the multiplexer error term the product of leakage times $r_{DS(on)}$ will remain approximately constant since leakage decreases as the supply voltages are reduced.

Caution must be taken to ensure that the chip enable (En) voltage is at least 0.7V below V_{CC} at all times. If this is not done the binary input strobing levels will not function properly. This may be achieved quite simply by connecting En (pin 2) to $+V_{CC}$ (pin 13) via a silicon diode as shown in Figure 6. If the 6108 is hooked up in this type of a configuration a further requirement must be met — the strobe levels at A_0 and A_1 must be within 2.5V of the En voltage to define a binary "1" state.

For the case shown in Figure 6 the En voltage is 11.3V which means that logic high at A_0 and A_1 is = +8.8V (logic low continues to be = 0.8V). In this configuration the 6108 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the 6108 have common supplies the En pin should again be connected to the supply through a silicon diode. In this case tying En to the logic supply directly will not work since it will violate the 0.7V differential voltage required between $+V_{CC}$ and En on the 6108 (See Figure 7). A 1μf capacitor can be placed across the diode to minimize switching glitches.

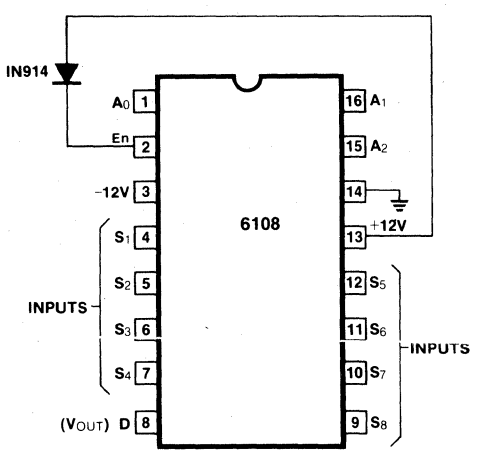


Figure 6. MU-6108 Connection Diagram for less than ±15V Supply Operation.

MU-6108 APPLICATION INFORMATION (CONT.)

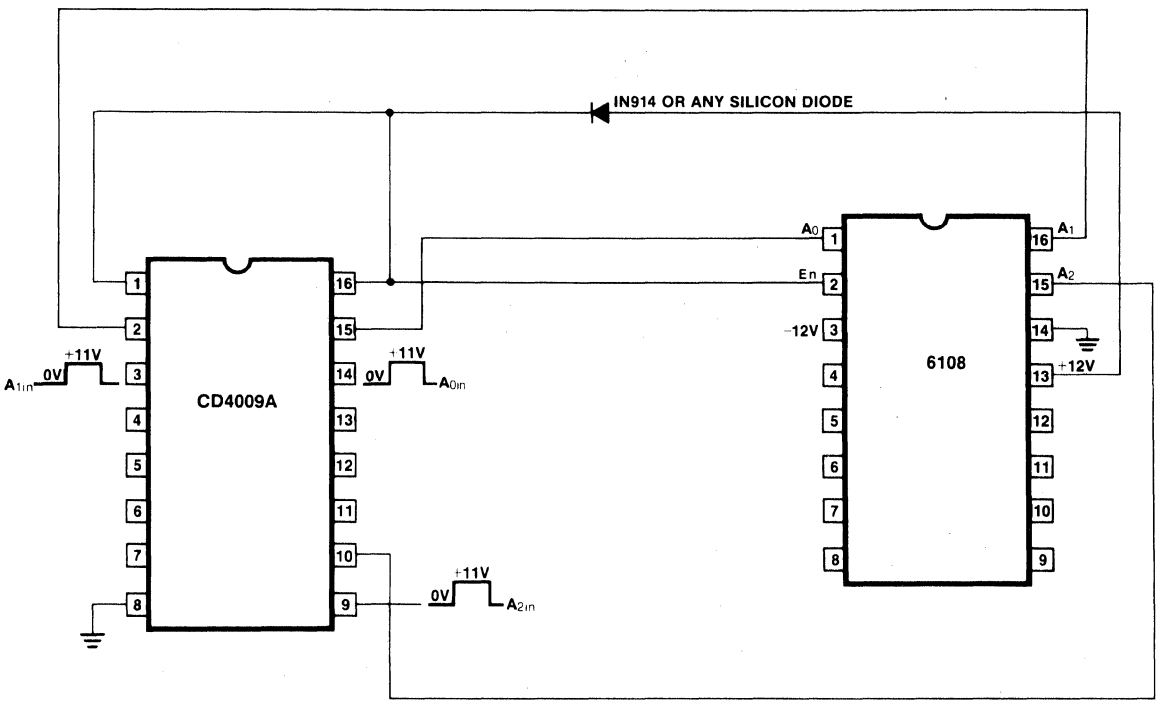
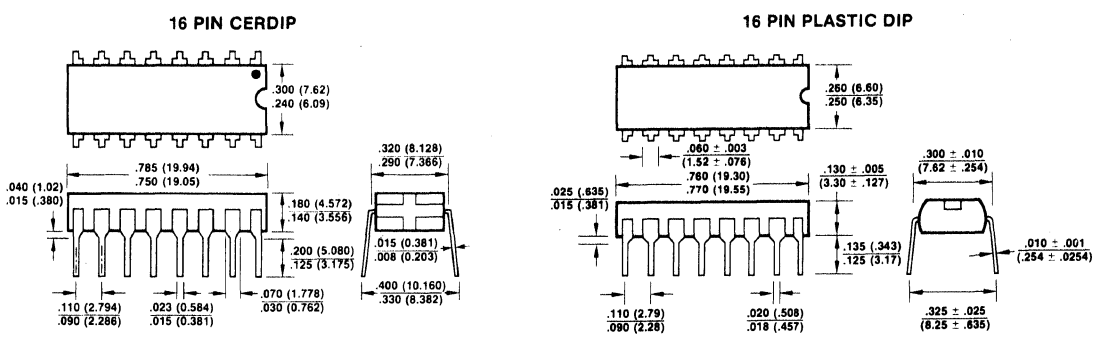


Figure 7. MU-6108 Connection Diagram with Enable Input Strobing for less than ±15V Supply Operation.

III. Peak-to-Peak Signal Handling Capability

The MU-6108 can handle input signals up to ±14V, actually −15V to +14.3V, when it has ±15V supplies. The input protection diode prevents the handling of signals up to +15V. The electrical specifications of the MU-16108 are guaranteed for ±10V signals but the specifications have very minor changes for ±14V signals. The notable changes would be slightly lower $r_{DS(on)}$ and slightly higher leakages.

PACKAGE DIMENSIONS



1. Lead no. 1 identified by dot or notch.
2. Dimensions in inches (millimeters).

CMOS 16-Channel Analog Multiplexer Model MU-6116

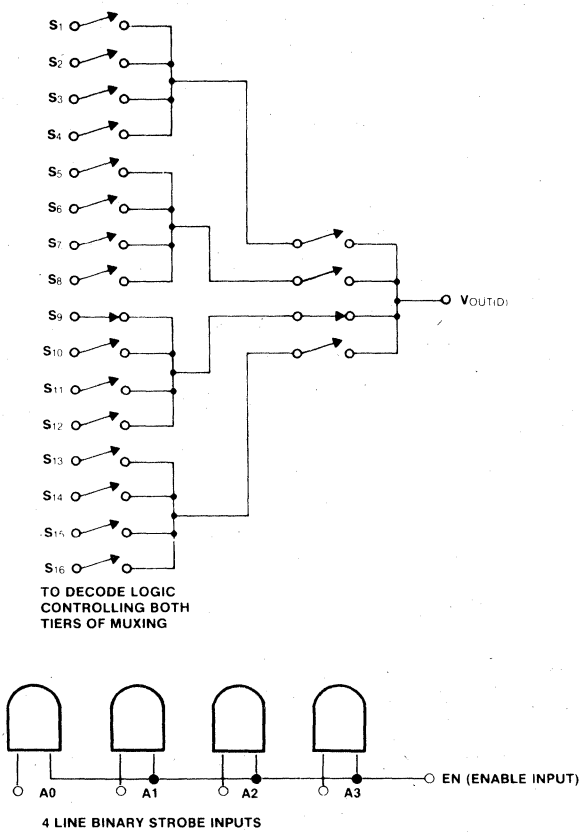
FEATURES

- **Pin Compatible with DG506, HI-506 & AD7506**
- **Ultra Low Leakage ≤100pA**
- **±11V analog signal range**
- **r_{on} <750 ohms over full signal and temperature range**
- **Break before make switching**
- **TTL and CMOS compatible strobe control**
- **Binary strobe control (4 strobe inputs control 16 channels)**
- **Two tier submultiplexing to facilitate expandability**
- **Power supply quiescent current less than 100μA**
- **No Latch up or "S.C.R." action**

GENERAL DESCRIPTION

The MU-6116 is a CMOS monolithic, one-out-of 16 multiplexer, and is a plug-in replacement for the DG506. Four line binary decoding is used so that the 16 channels can be controlled by 4 strobe inputs; additionally a fifth input is provided to use as a system enable; if the enable input is 0V, none of the channels can be turned on. When the enable input is high (5V) the channels are sequenced by the 4 line strobe inputs. The 4 strobe inputs are controlled by TTL logic or CMOS logic elements; a "0" corresponds to any voltage less than 0.8V and a "1" corresponds to any voltage greater than 3V; however the enable input (EN) *must* be taken to 5V to enable the system and less than 0.8V to disable the system.

FUNCTIONAL DIAGRAM

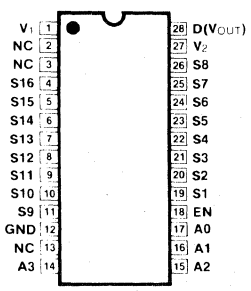


DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	EN	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Logic "1" = $V_{AH} \geq 3.0V$
Logic "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION



TOP VIEW
V_1 COMMON TO SUBSTRATE

ORDERING INFORMATION

MODEL	OPER. TEMP RANGE	PACKAGE
MU-6116C	0 to +70°C	28 Pin Epoxy DIP
MU-6116M	−55 to +125°C	28 Pin CerDIP

MU-6116

ABSOLUTE MAXIMUM RATINGS

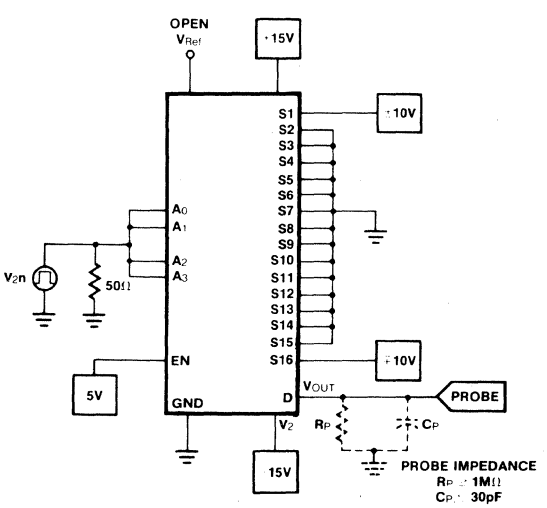
V_{IN} (A, EN) to Ground ..... −15V to 15V
V_S or V_D to V_1 ..... 0, −32V
V_S or V_D to V_2 ..... 0, 32V
V_1 to Ground 16V
V_2 to Ground ..... −16V
Current (Any Terminal) ..... 30 mA
Current (Analog Drain) ..... 20 mA
Current (Analog Source) ..... 20 mA
Operating Temperature ..... −55 to 125° C
Storage Temperature ..... −65 to 150° C
Power Dissipation (Package)* ..... 1200 mW

*All leads soldered or welded to PC board. Derate 10 mW/° C above 70° C.

ELECTRICAL CHARACTERISTICS

	CHARACTERISTIC	MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT	TEST CONDITIONS (UNLESS OTHERWISE NOTED) V_1 = 15V, V_2 = −15V, Ground = 0 V_{EN} = +5V (Note 1)	
SWITCH	$r_{DS(ON)}$	S to D	16	480	600	600	700	650	650	750	Ω	V_D = 10V, I_S = −1.0mA	Sequence each switch on
			16	300	600	600	700	650	650	750		V_D = −10V, I_S = −1.0mA	$V_{A(L)}$ = 0.8V, $V_{A(H)}$ = 3V
	$\Delta r_{DS(ON)}$			20							%	$\Delta r_{DS(ON)} = \frac{r_{DS(ON)MAX} - r_{DS(ON)MIN}}{r_{DS(ON)AVG.}}$ −10V ≤ V_S 10V	
	$I_{S(OFF)}$	S	16	0.01		0.1	50		0.2	50	NA	V_S = 10V, V_D = −10V	V_{EN} = 0
			16	0.01		0.1	50		0.2	50		V_S = −10V, V_D = 10V	
	$I_{D(OFF)}$	D	1	0.1		0.2	100		0.4	100		V_D = 10V, V_S = −10V	
			1	0.1		0.2	100		0.4	100		V_D = −10V, V_S = 10V	
			16	0.1		0.2	100		0.4	100		$V_{S(All)}$ = V_D = 10V	Sequence each switch on
	$I_{D(ON)}$	D	16	0.1		0.2	100		0.4	100		$V_{S(All)}$ = V_D = −10V	$V_{A(L)}$ = 0.8V, $V_{A(H)}$ = 3V
INPUT	$I_{AN(ON)}$ or		4	.01		−10	−30		−10	−30	μA	V_A = 3.0V	
	$I_{AN(OFF)}$		4	.01		10	30		10	30		V_A = 15V	
	I_A	A_0 A_1 A_2 A_3	4			−10	−30		−10	−30		V_{EN} = 5V	All V_A = 0
		EN	1			−10	−30		−10	−30		V_{EN} = 0	
DYNAMIC	$t_{transition}$	D		0.6		1					μs	See Fig. 1	
	t_{open}	D		0.2								See Fig. 2	
	$t_{on(En)}$	D		0.8		1.5						See Fig. 3	
	$t_{off(En)}$	D		0.3		1							
	"OFF" Isolation	D		60							dB	V_{EN} = 0, R_L = 200Ω, C_L = 3pF, V_S = 3 VRMS, f = 500 kHz	
	$C_{S(OFF)}$			5							pF	V_S = 0	
	$C_{D(OFF)}$			40								V_D = 0	V_{EN} = 0, f = 140 kHz to 1 MHz
	$C_{DS(OFF)}$			1								V_S = 0, V_D = 0	
SUPPLY	I_1	V_1	1	55		200			1000		μA	V_{EN} = 5V	All V_A = 0 OR 3V
	I_2	V_2	1	2		100			1000				
	I_1 Standby	V_1	1	1		100			1000			V_{EN} = 0	
	I_2 Standby	V_2	1	1		100			1000				

NOTE 1: See Section V. Enable Input Strobing Levels.



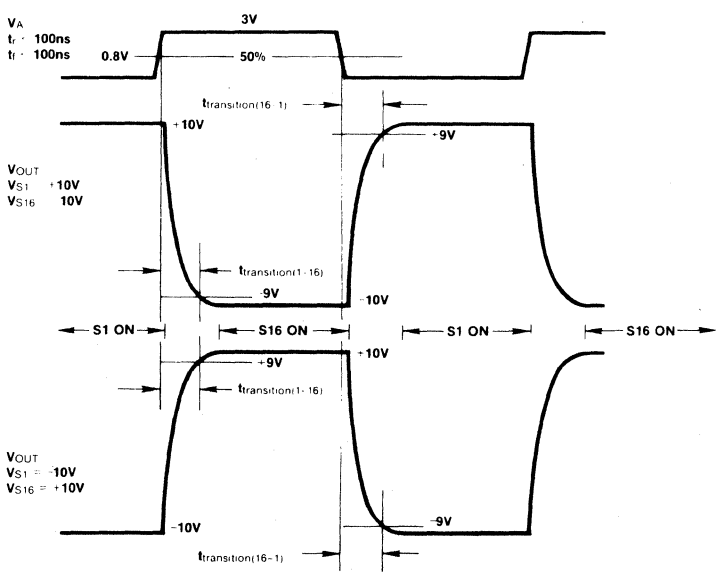


Figure 1

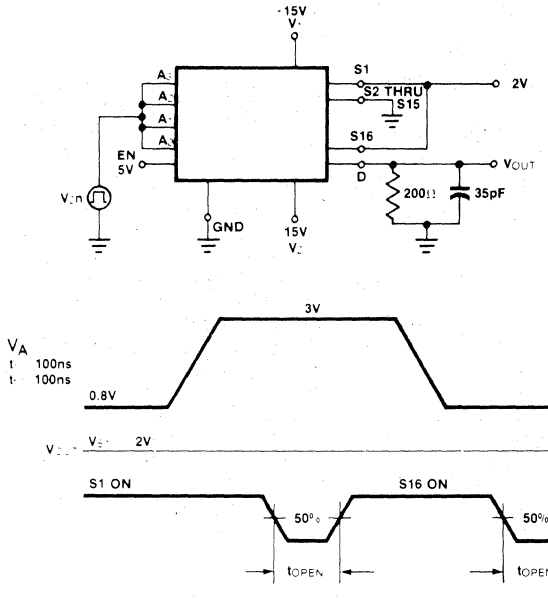


Figure 2

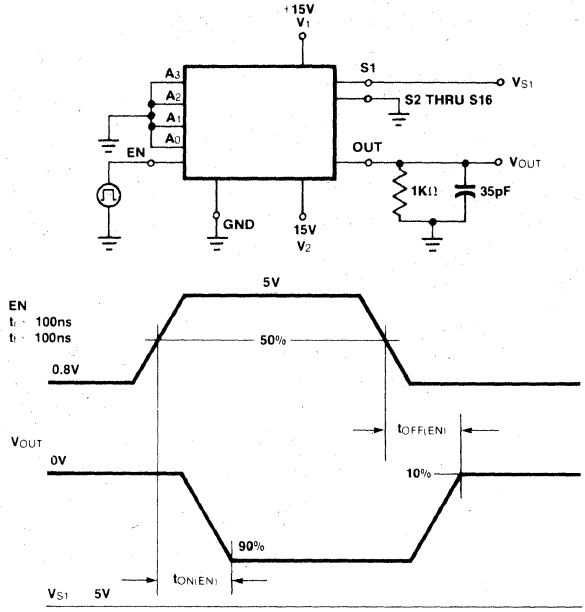


Figure 3

MU-6116 APPLICATIONS

1. 1 out of 32 channel multiplexer using 2 MU-6116s.

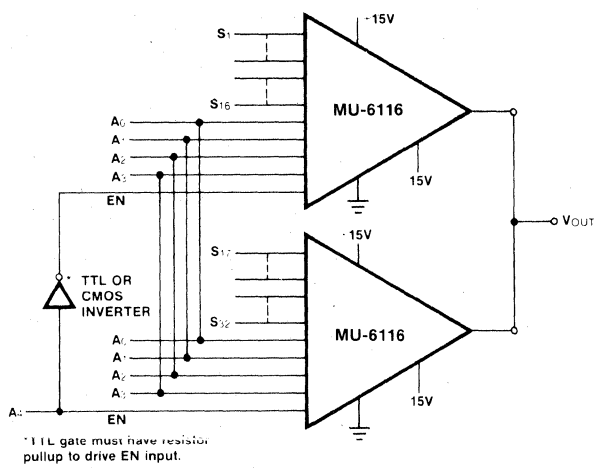


Figure 4

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

MU-6116

MU-6116 APPLICATIONS

II. 1 out of 32 channel multiplexer using 2 MU-6116s; using an AS-5041 for submultiplexing.

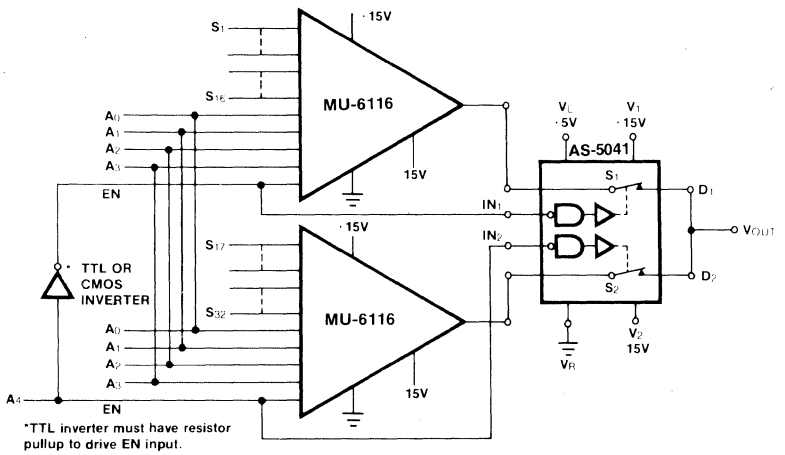


Figure 5

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

MU-6116 APPLICATIONS

III. 1 out of 64 multiplexer using 4 1/16s and IH5053 as submultiplexer.

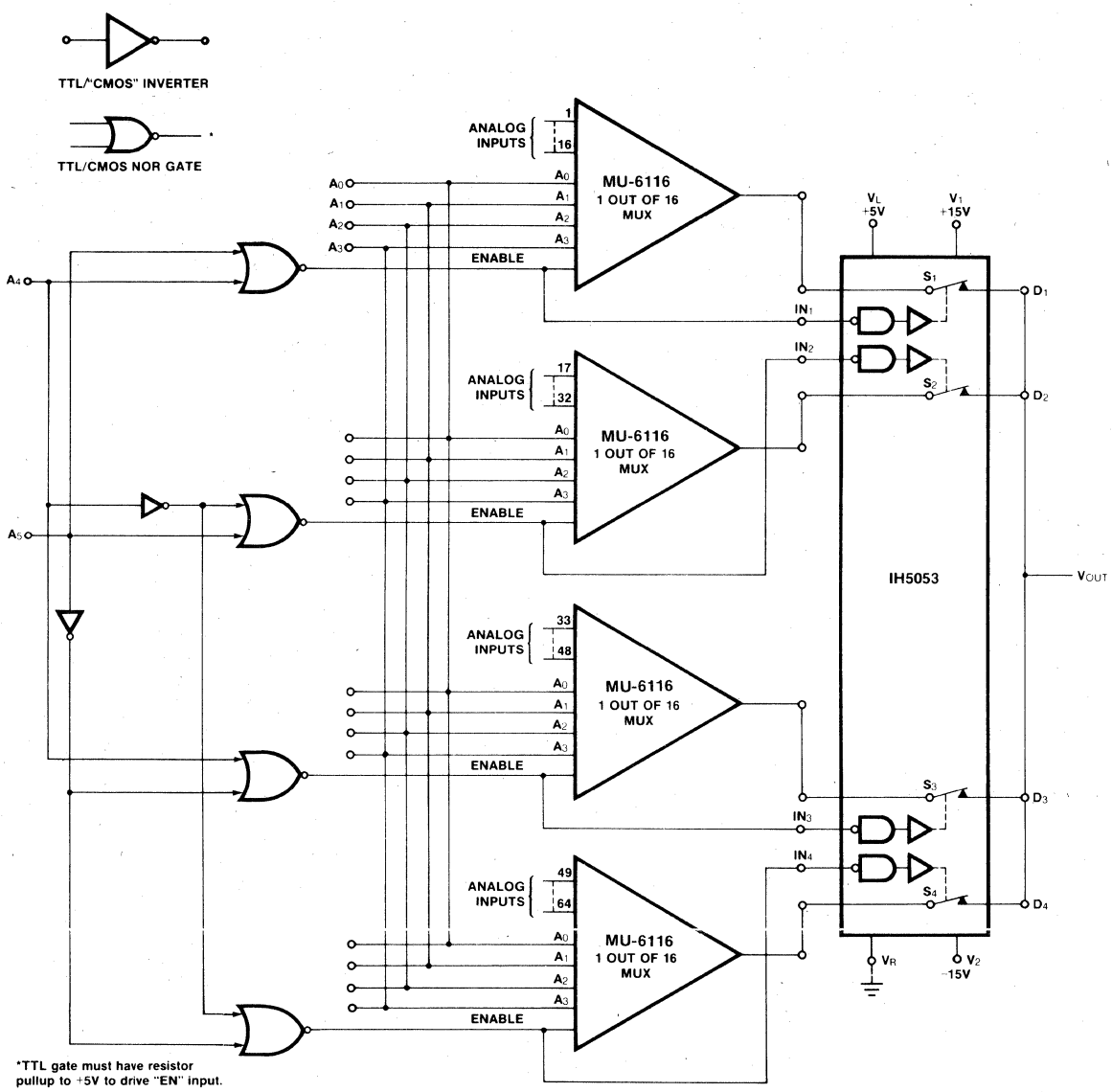


Figure 6

IV. GENERAL NOTE ON EXPANDABILITY OF MU-6116

The MU-6116 is a two tier multiplexer wherein sixteen input channels are routed to a common output in blocks of 4 channels at a time. Each block of 4 input channels is routed to one common output channel; thus the submultiplexed system looks like 4 blocks of 4 inputs routed to 4 different outputs, and the 4 outputs are all tied together. Thus 20 switches are needed to handle the 16 channels of information. The advantage of this scheme is lower output capacity and lower leakage than a system with all 16 channels tied to one common output. Also the expandability into 32, 64, 128, etc. is facilitated. Figures 4, 5, and 6 show how the MU-6116 is expanded.

Figure 4 shows a 1 out of 32 multiplexer using 2 of the MU-6116s. Since the 6116 is itself a 2 tier mux the system as shown is basically a 2 tier system. Now the four output channels of each 6116 are tied together so that 8 channels are tied for the V_{out} common point. Since only one channel of information is on at a time, the common output will consist of 7 off channels and 1 on channel. Thus the output leakage will correspond to 7 $I_{D(offs)}$ and 1 $I_{D(on)}$; this should result in about 1.0 nA of typical leakage at room temperature. Thruput speed will be typically 0.8μs for t_{on} and 0.3μs for t_{off}. Thruput channel resistance will be in the 500 ohm area.

Figure 5 shows the same 1 out of 32 mux as Figure 4, except that a third tier of submultiplexing is added to further reduce leakage and output capacity. The AS-5041 has typical on resistances of 50 ohms (max. is 75 ohms) so it only increases thruput channel resistance from the 500 ohms of Figure 4 to about 550 ohms for Figure 5. Thruput channel speed is a little slower by about 0.5μs for both on and off time. Output leakage is about 0.2 nA typical.

Figure 6 shows a 1 out of 64 mux using 3 tier muxing (similar to Figure 5 application). The Intersil IH5053 is used to get the third tier of muxing. The V_{out} point will see 3 off channels and 1 on channel at any time so that the typical leakages will be about 0.4 nA. Thruput channels resistance will be in the 550 ohm area and thruput switching speeds will be about 1.3μs for on time and 0.8μs for off time.

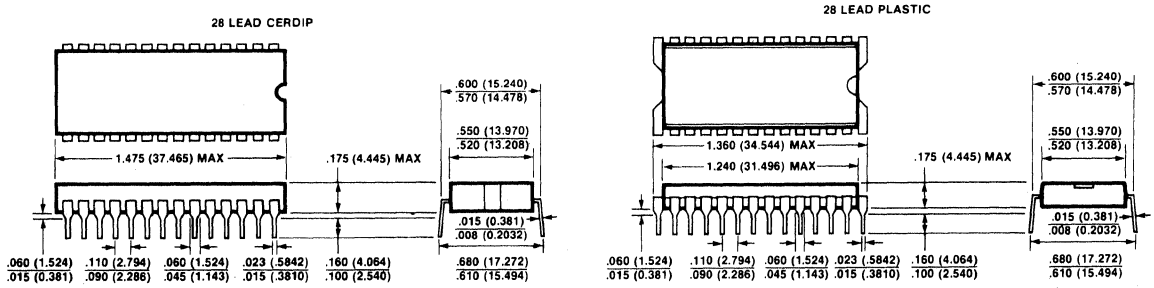
The IH5053 was chosen as the third tier of the mux because it will switch the same AC signals as the MU-6116 (typically plus and minus 11V) and break before make switching is guaranteed so that the muxing system remains a break-before-make. Also power supply quiescent currents are typically 1μA from any supply, so that no excessive system power is generated. Also the logic of the 5053 is such that it can be tied directly to the enable input (as shown in the figures) with no extra logic being required.

V. ENABLE INPUT STROBING LEVELS

The enable input (EN) acts as an enabling or disabling pin for the MU-6116, when used as a 16 channel mux; however, when expanding the mux to more than 16 channels, the EN pin acts as another address input. As an example, we see in Figures 4 and 5 that the EN pin acts as the A_4 input.

For the system to function properly the EN input (pin 18) must go to 5V ±5% for the high state and less than 0.8V for the low state. When using TTL logic, a pull-up resistor should be used to pull the output voltage up to 5V; this resistor should be 1k ohm or less. When using CMOS logic, the high state goes up to the power supply so no pull-up is required.

PACKAGE DIMENSIONS



NOTE: This multiplexer does not require external resistors and/or diodes to eliminate what is commonly known as a latch up or SCR action. Because of the elimination of external resistors in each channel the $r_{DS(ON)}$ of the switch is maintained at specified values.

CMOS 4-Channel Differential Analog Multiplexer Model MU-6208

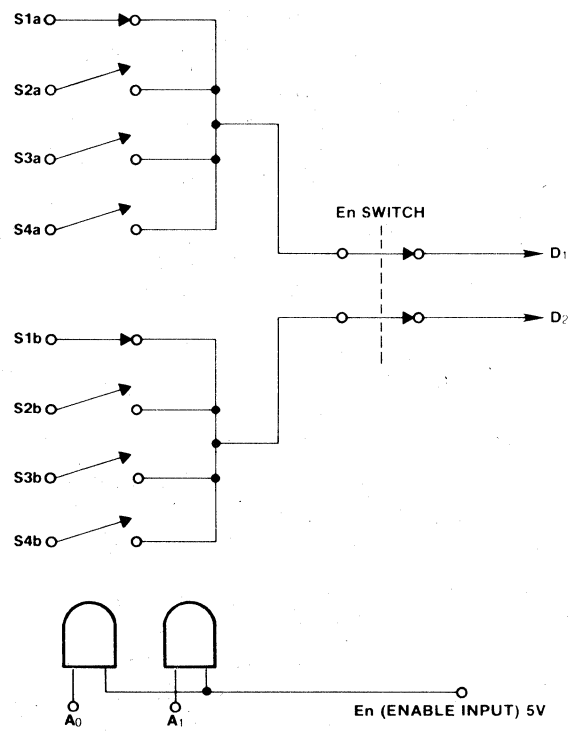
FEATURES

- **Ultra low leakage ≤ 100pA (Total I_{Doff})**
- **r_{on} < 400 ohms over full signal and temperature range**
- **Power supply quiescent current less than 100μA**
- **±14V analog signal range**
- **No latch up or "S.C.R." action**
- **Break before make switching**
- **Binary strobe control (2 strobe inputs controls 2 out of 8 channels).**
- **TTL and CMOS compatible strobe control**
- **Pin — Pin with HI509, DG509 & AD7509**

GENERAL DESCRIPTION

The MU-6208 is a 2 out of 8 CMOS monolithic multiplexer.The part is a plug-in replacement for the DG509. Two line binary decoding is used so that the 8 channels can be controlled in pairs by the binary inputs; additionally a third input is provided to use as a system enable; if the enable input is 0V, none of the channels can be turned on. When the enable input is high (5V) the channels are sequenced by the 2 line binary inputs. The 2 strobe inputs are controlled by TTL logic or CMOS logic elements; a "0" corresponds to any voltage less than 0.8V and a "1" corresponds to any voltage greater than 2.4V; however the enable input (En) *must* be taken to 5V to enable the system and less than 0.8V to disable the system.

FUNCTIONAL DIAGRAM



2 LINE BINARY STROBE INPUTS
(0 0) AND En 5V (En "1" FOR +5V, "0" FOR 0V)
ABOVE EXAMPLE SHOWS CHANNELS 1a & 1b ON.

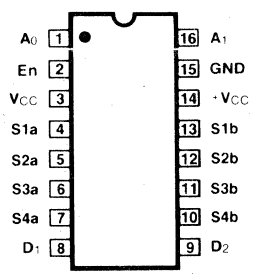
DECODE TRUTH TABLE

A_1	A_0	En	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1a, 1b
0	1	1	2a, 2b
1	0	1	3a, 3b
1	1	1	4a, 4b

A_0, A_1

LOGIC "1" = V_{AH} > 2.4V
LOGIC "0" = V_{AL} < 0.8V

PIN CONFIGURATION



ORDERING INFORMATION

MODEL	OPER. TEMP. RANGE	PACKAGE
MU-6208C	0 to +70° C	16 PIN EPOXY DIP
MU-6208M	−55 to +125° C	16 PIN CERDIP

MU-6208

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, En) to Ground ..... −15V, V_1
V_S or V_D to V_{CC} ..... 0, −32V
V_S or V_D to V_{CC} 0, 32V
+V_{CC} to Ground 16V
−V_{CC} to Ground ..... −16V
Current (Any Terminal) ..... 30 mA
Current (Analog Drain) ..... 20 mA
Current (Analog Source) ..... 20 mA
Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Power Dissipation (Package)* ..... 1200 mW

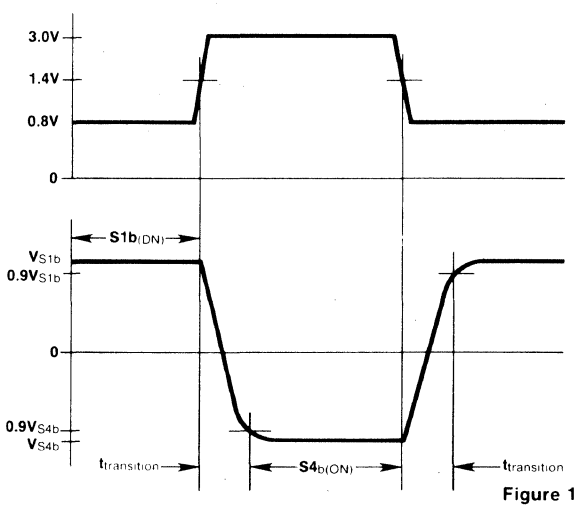
*All leads soldered or welded to PC board. Derate 10 mW/° C above 70° C.

ELECTRICAL CHARACTERISTICS

	CHARACTERISTIC	MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25° C	MAX LIMITS M SUFFIX −55° C	M SUFFIX 25° C	M SUFFIX 125° C	C SUFFIX 0° C	C SUFFIX 25° C	C SUFFIX 70° C	UNIT	TEST CONDITIONS (UNLESS OTHERWISE NOTED) +V_{CC} = 15V, −V_{CC} = −15V, Ground = 0V V_{En} = +5V (Note 1)	
SWITCH	$r_{DS(ON)}$	S to D	8	180	300	300	400	350	350	450	Ω	V_D = 10V, I_S = −1.0 mA	Sequence each switch on
			8	150	300	300	400	350	350	450		V_D = −10V, I_S = −1.0 mA	$V_{A(L)}$=0.8V, $V_{A(H)}$=2.4V
	$\Delta r_{DS(ON)}$			20							%	$\Delta r_{DS(ON)} = \frac{r_{DS(ON)MAX} - r_{DS(ON)MIN}}{r_{DS(ON)\ AVG.}}$ −10V ≤ V_S 10V	
	$I_{S(OFF)}$	S	8	0.002		0.05	50		0.1	50	NA	V_S = 10V, V_D = −10V	V_{En} 0
			8	0.002		0.05	50		0.1	50		V_S = −10V, V_D = 10V	
	$I_{D(OFF)}$	D	2	0.03		0.1	50		0.2	100		V_D = 10V, V_S = −10V	
			2	0.03		0.1	50		0.2	100		V_D = −10V, V_S = 10V	
	$I_{D(ON)}$	D	8	0.1		0.2	50		0.4	100		$V_{S(All)}$ = V_D = 10V	Sequence each switch on
			8	0.1		0.2	50		0.4	100		$V_{S(All)}$ = V_D = −10V	$V_{A(L)}$=0.8V, $V_{A(H)}$=2.4V
INPUT	$I_{AN(ON)}$ or		2	.01		−10	−30		−10	−30	μA	V_A = 2.4V or 0V	
	$I_{AN(OFF)}$		2	.01		10	30		10	30		V_A = 15V or 0V	
	I_{2n}	A_0 A_1	2			−10	−30		−10	−30		V_{En} 5V	All V_A = 0
		En	1			−10	−30		−10	−30		V_{En} 0	(Strobe Pins)
DYNAMIC	$t_{transition}$	D		0.3		1					μs	See Fig. 1	
	t_{open}	D		0.2								See Fig. 2	
	$t_{on(En)}$	D		0.6		1.5						See Fig. 3	
	$t_{off(En)}$	D		0.4		1							
	"OFF" Isolation	D		60							dB	V_{En} = 0, R_L = 200Ω, C_L = 3 pF, V_S = 3 VRMS, f = 500 kHz	
	$C_{S(OFF)}$			5							pF	V_S = 0	
	$C_{D(OFF)}$			12								V_D = 0	V_{En} = 0, f = 140 kHz to 1 MHz
	$C_{DS(OFF)}$			1								V_S = 0, V_D = 0	
SUPPLY	I_{14} (+V_{CC})	+V_{CC}	1	40		200			1000		μA	V_{En} 5V	All V_A 0 OR 5V
	I_3 (−V_{CC})	−V_{CC}	1	2		100			1000				
	I_{14} Standby	+V_{CC}	1	1		100			1000			V_{En} 0	
	I_3 Standby	−V_{CC}	1	1		100			1000				

NOTE 1: See Section I Enable Input Strobing Levels.

SWITCHING INFORMATION



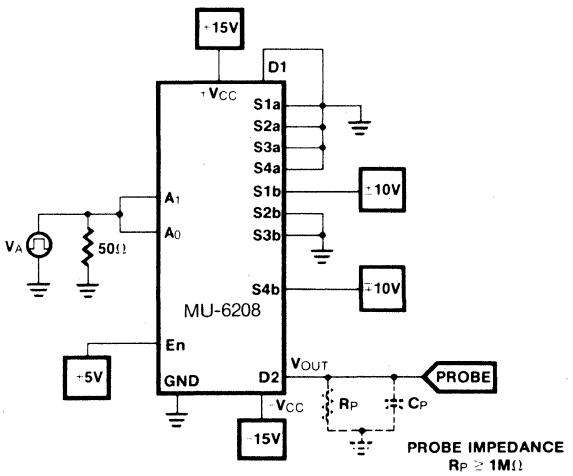


Figure 1. $t_{transition}$ Switching Test

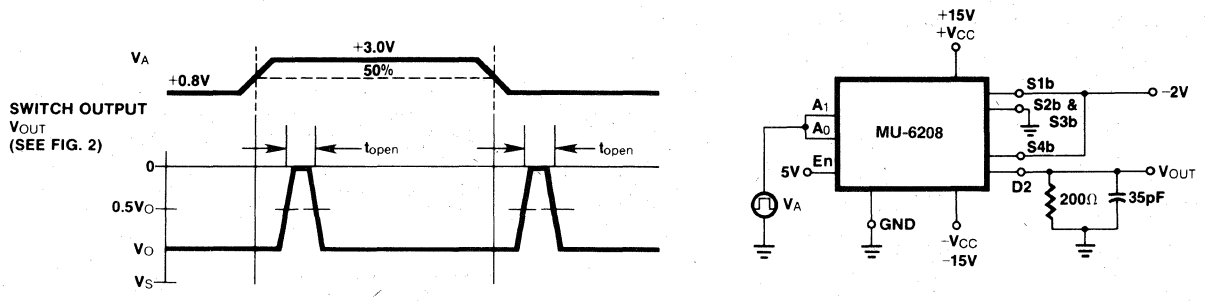
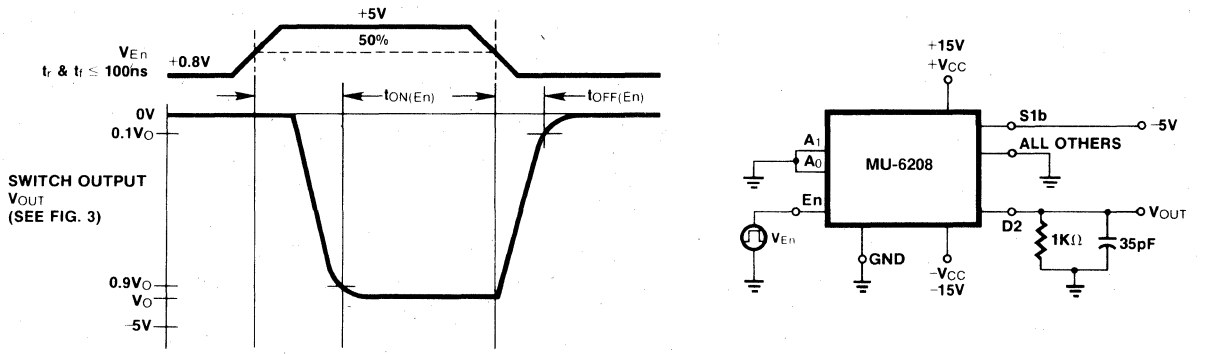


Figure 2. t_{open} (Break-Before-Make) Switching Test



MU-6208
MU-6208
MU-6208

Figure 3. t_{on} and t_{off} Switching Test

IH6208 APPLICATION INFORMATION

I. Enable Input Strobing Levels

The chip enable input on the MU-6208 requires a minimum of +4.5V to trigger it into the "1" state and a maximum of +0.8V to trigger it into the "0" state. If the chip enable input is being driven from TTL logic, a pull-up resistor is required from the gate output to +5V supply. The value of this resistor is not critical and can be in the 1K to 3KΩ range (See Figure 4).

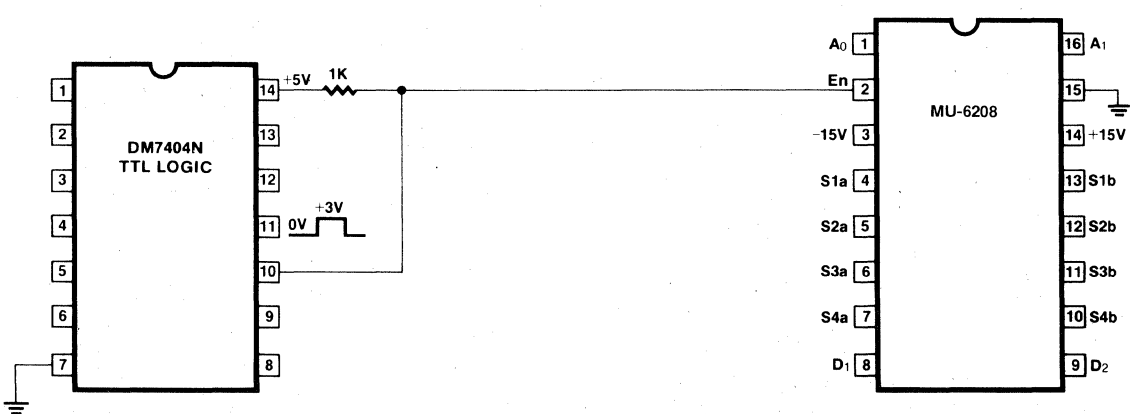


Figure 4. Enable Input Strobing from TTL Logic

6208 APPLICATION INFORMATION (CONT.)

When the En input is driven from CMOS logic, no pullup is necessary. Fig. 5 shows the CD4009 driving the En input.

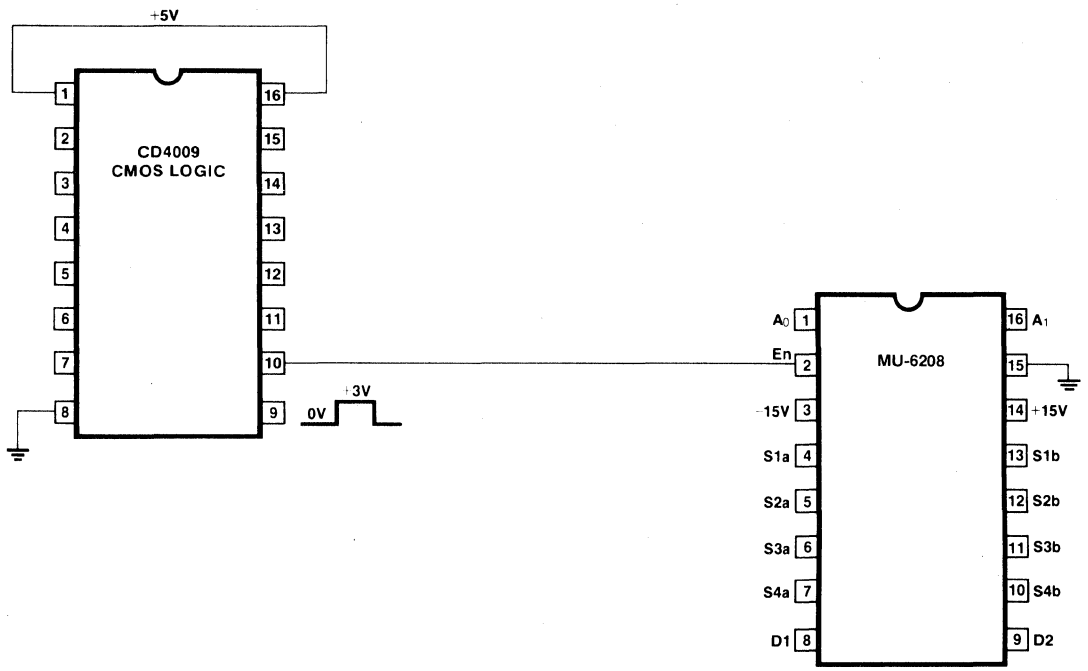


Figure 5

The Supply Voltage of the CD4009 does affect the switching speed of the MU-6208 with the same being true for Supply Voltage Levels. The chart below shows the effect, on $t_{transition}$ times, of supply varying from +4.5V to +5.5V.

CMOS OR TTL SUPPLY	TYPICAL $t_{transition}$ @ 25°C
+4.5V	400ns
+4.75V	300ns
+5.0V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the Enable Strobe Logic.

The cases shown in Figures 4 and 5 deal with enable strobing when expandability to more than four differential channels is required. In these cases the En terminal acts as a third binary input. If four channel pairs or less are being multiplexed, the En terminal can be directly connected to +5V logic supply which would "enable" the MU-6208 at all times.

APPLICATIONS

II. Using the MU-6208 with supplies other than ±15V

The MU-6208 can be used with power supplies ranging from ±6V to ±16V. The switch $r_{DS(ON)}$ will increase as the supply voltages decrease. However, the multiplexer error term (the product of leakage times $r_{DS(ON)}$ will remain approximately constant since leakage decreases as the supply voltages are reduced.

Caution must be taken to ensure that the chip enable (En) voltage is at least 0.7V below V_{CC} at all times. If this is not done the binary input strobing levels will not function properly. This may be achieved quite simply by connecting En (pin 2) to $+V_{CC}$ (pin 14) via a silicon diode as shown in Figure 6. If the MU-6208 is hooked up in this type of a configuration a further requirement must be met — the strobe levels at A_0 and A_1 must be within 2.5V of the En voltage to define a binary "1" state. For the case shown in Figure 6 the En voltage is 11.3V which means that logic high at A_0 and A_1 is = +8.8V (logic low continues to be = 0.8V). In this configuration the MU-6208 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the MU-6208 have common supplies the En pin should again be connected to the supply through a silicon diode. In this case tying En to the logic supply directly will not work since it will violate the 0.7V differential voltage required between $+V_{CC}$ and En on the MU-6208 (See Figure 7). A 1μf capacitor can be placed across the diode to minimize switching glitches.

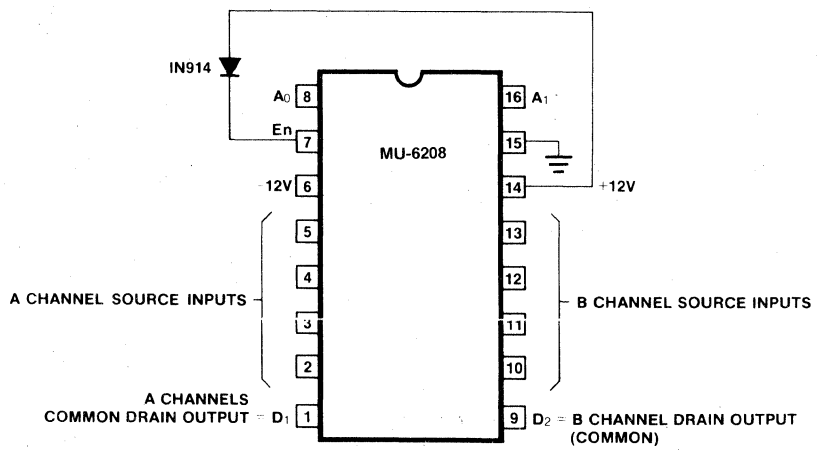


Figure 6. MU-6208 Connection Diagram for less than ±15V Supply Operation.

MU-6208 APPLICATION INFORMATION

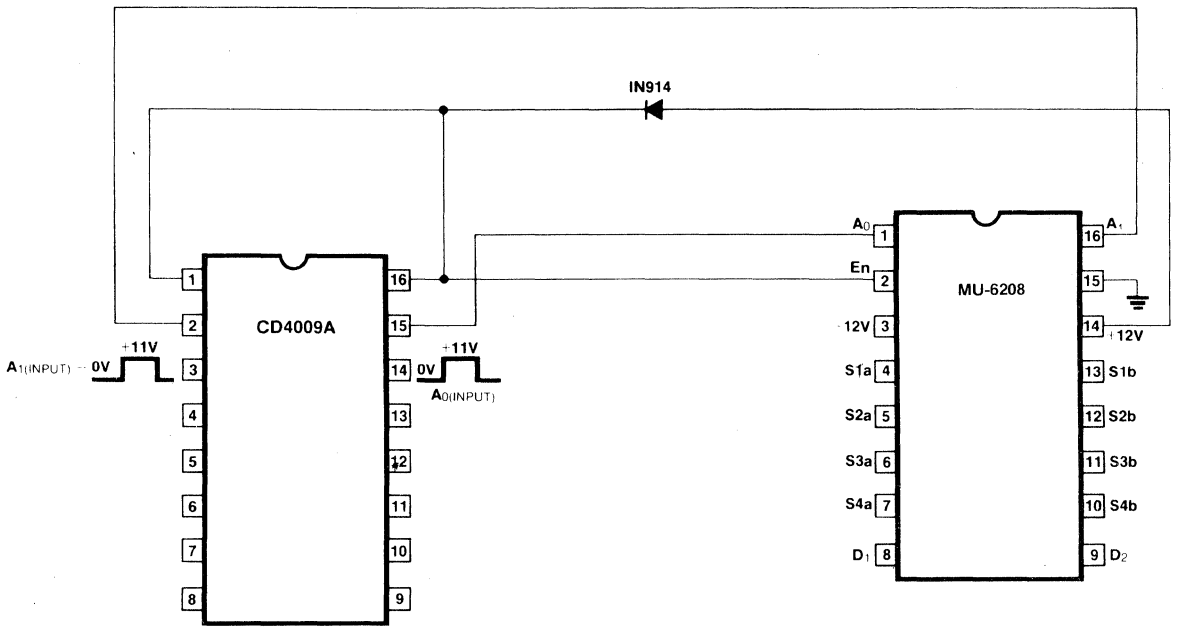


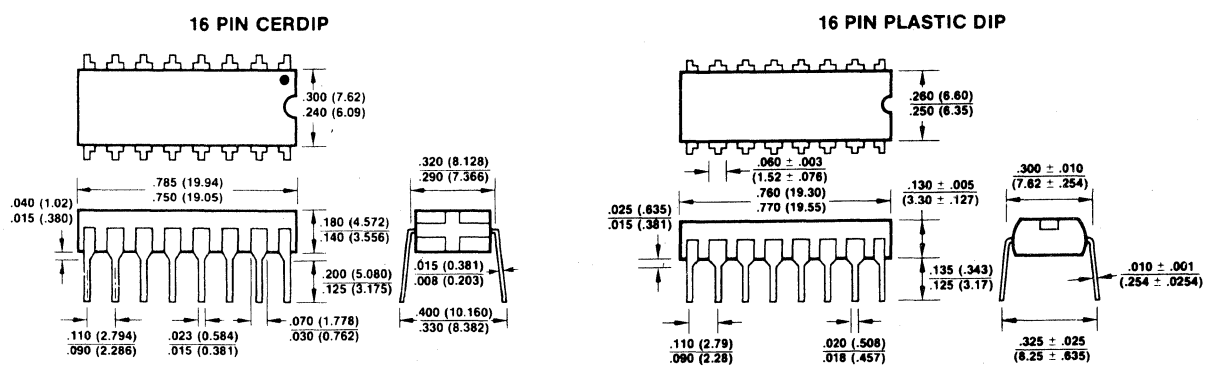
Figure 7. MU-6208 Connection Diagram with Enable Input Strobing for less than ±15V Supply Operation.

III. Peak-to-Peak Signal Handling Capability

The MU-6208 can handle input signals up to ±14V (actually -15V to +14.3V) when it has ±15V supplies. The input protection diode prevents the handling of signals up to +15V.

The electrical specifications of the MU-6208 are guaranteed for ±10V signals but the specifications have very minor changes for ±14V signals. The notable changes would be slightly lower $r_{DS(on)}$ and slightly higher leakages.

PACKAGE DIMENSIONS



1. Lead no. 1 identified by dot or notch. 2. Dimensions in inches (millimeters).

CMOS 8-Channel Differential Analog Multiplexer Model MU-6216

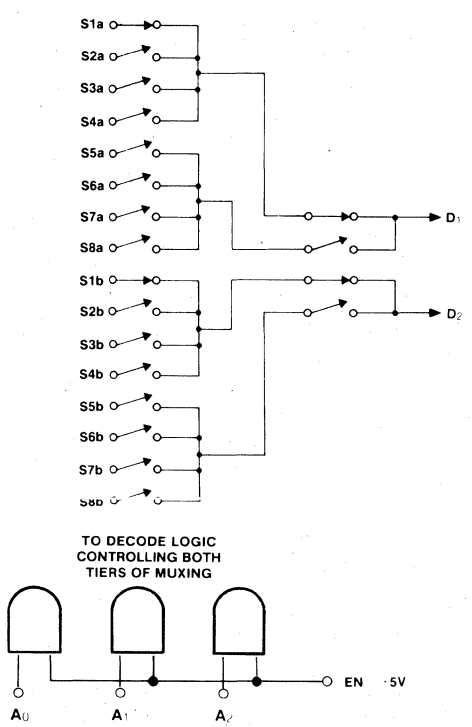
FEATURES

- **Pin Compatible with HI507, DG507 & AD7507**
- **±11V analog signal range**
- **r_{on} < 750 ohms over full signal and temperature range**
- **Break before make switching**
- **TTL and CMOS compatible strobe control**
- **Binary strobe control (3 strobe inputs controls 2 out of 16 channels).**
- **Two tier submultiplexing to facilitate expandability**
- **Power supply quiescent current less than 100μA**
- **No latch up or "S.C.R." action**
- **Very low leakage ≤ 100pA**

GENERAL DESCRIPTION

The MU-6216 is a 2 out of 16 CMOS monolithic multiplexer. The part is a plug-in replacement for the DG507. Three line binary decoding is used so that the 16 channels can be controlled in pairs by the binary inputs; additionally a fourth input is provided to use as a system enable; if the enable input is 0V, none of the channels can be turned on. When the enable input is high (5V) the channels are sequenced by the 3 line binary inputs. The 3 strobe inputs are controlled by TTL logic or CMOS logic elements; a "0" corresponds to any voltage less than 0.8V and a "1" corresponds to any voltage greater than 3.0V; however the enable input (EN) *must* be taken to 5V to enable the system and less than 0.8V to disable the system.

FUNCTIONAL DIAGRAM

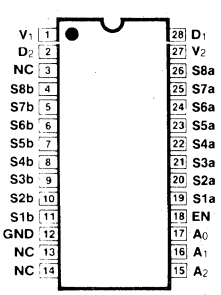


DECODE TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

LOGIC "1" = V_{AH} > 3V
LOGIC "0" = V_{AL} < 0.8V

PIN CONFIGURATION



TOP VIEW
V_1 COMMON TO SUBSTRATE

ORDERING INFORMATION

MODEL	OPER. TEMP. RANGE	PACKAGE
MU-6216C	0 to +70°C	28 PIN EPOXY DIP
MU-6216M	−55 to +125°C	28 PIN CERDIP

MU-6216

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V, V_1
V_S or V_D to V_1 ..... 0, −32V
V_S or V_D to V_2 ..... 0, 32V
V_1 to Ground 16V
V_2 to Ground ..... −16V
Current (Any Terminal) ..... 30 mA
Current (Analog Drain) ..... 20 mA
Current (Analog Source) ..... 20 mA
Operating Temperature ..... −55 to 125° C
Storage Temperature ..... −65 to 150° C
Power Dissipation (Package)* 1200mW
Lead Temperature (Soldering 10 sec) ..... 300 °C

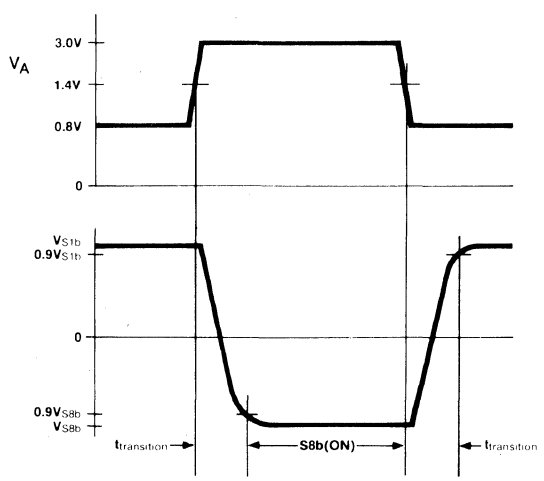
*All leads soldered or welded to PC board. Derate 10 mW/° C above 70° C

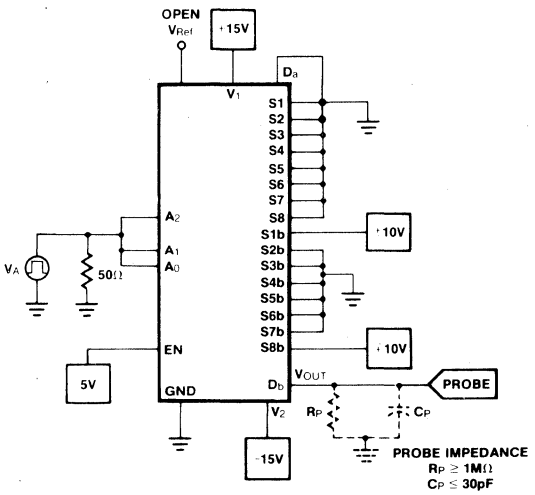
ELECTRICAL CHARACTERISTICS

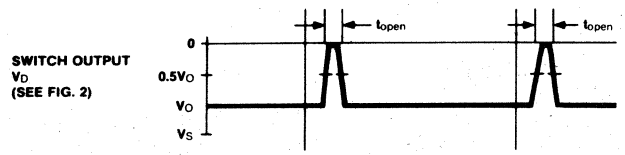
	CHARACTERISTIC	MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25° C	MAX LIMITS M SUFFIX −55° C	M SUFFIX 25° C	M SUFFIX 125° C	C SUFFIX 0° C	C SUFFIX 25° C	C SUFFIX 70° C	UNIT	TEST CONDITIONS (UNLESS OTHERWISE NOTED) V_1 = 15V, V_2 = −15V, Ground = 0 V_{EN} = +5V (Note 1)	
SWITCH	$r_{DS(ON)}$	S to D	16	480	600	600	700	650	650	750	Ω	V_D = 10V, I_S = −1.0mA	Sequence each switch on
			16	300	600	600	700	650	650	750		V_D = −10V, I_S = −1.0mA	$V_{A(L)}$=0.8V, $V_{A(H)}$=3V
	$\Delta r_{DS(ON)}$			20							%	$\Delta r_{DS(ON)} = \frac{r_{DS(ON)MAX} - r_{DS(ON)MIN}}{r_{DS(ON)\ AVG.}}$ −10V ≤ V_S 10V	
	$I_{S(OFF)}$	S	16	0.01		0.1	50		0.2	50	nA	V_S = 10V, V_D = −10V	V_{EN} = 0
			16	0.01		0.1	50		0.2	50		V_S = −10V, V_D = 10V	
	$I_{D(OFF)}$	D	2	0.1		0.2	100		0.4	100		V_D = 10V, V_S = −10V	
			2	0.1		0.2	100		0.4	100		V_D = −10V, V_S = 10V	
	$I_{D(ON)}$	D	16	0.1		0.2	100		0.4	100		$V_{S(All)}$ = V_D = 10V	Sequence each switch on
			16	0.1		0.2	100		0.4	100		$V_{S(All)}$ = V_D = −10V	$V_{A(L)}$=0.8V, $V_{A(H)}$=3V
INPUT	$I_{AN(ON)}$ or $I_{AN(OFF)}$		3	.01		−10	−30		−10	−30	μA	V_A = 3.0V	
			3	.01		10	30		10	30		V_A = 15V	
	I_A	A_0 A_1 A_2 A_3	3			−10	−30		−10	−30		V_{EN} = 5V	All V_A = 0
		EN	1			−10	−30		−10	−30		V_{EN} = 0	
DYNAMIC	$t_{transition}$	D		0.6		1					μs	See Fig. 1	
	t_{open}	D		0.2								See Fig. 2	
	$t_{on(En)}$	D		0.8		1.5						See Fig. 3	
	$t_{off(En)}$	D		0.3		1							
	"OFF" Isolation	D		60							dB	V_{EN} = 0, R_L = 200Ω, C_L = 3 pF, V_S = 3 VRMS, f = 500 kHz	
	$C_{S(OFF)}$			5							pF	V_S = 0	
	$C_{D(OFF)}$			20								V_D = 0	V_{EN} = 0, f = 140 kHz to 1 MHz
	$C_{DS(OFF)}$			1								V_S = 0, V_D = 0	
SUPPLY	I_1	V_1	1	55		200			1000		μA	V_{EN} = 5V	All V_A = 0 OR 3V
	I_2	V_2	1	2		100			1000				
	I_1 Standby	V_1	1	1		100			1000			V_{EN} = 0	
	I_2 Standby	V_2	1	1		100			1000				

NOTE 1: See Section V. Enable Input Strobing Levels.

SWITCHING INFORMATION







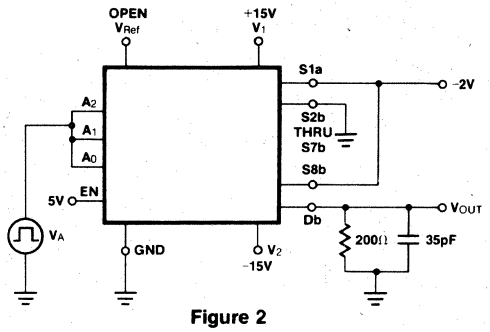
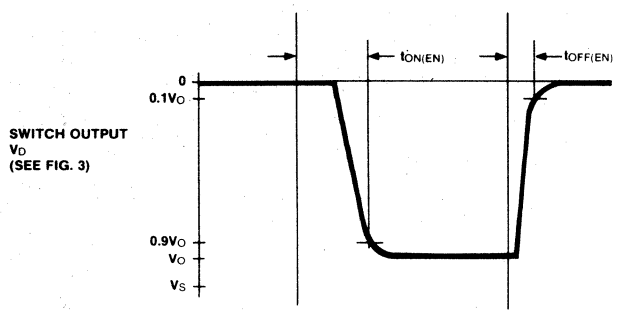


Figure 2



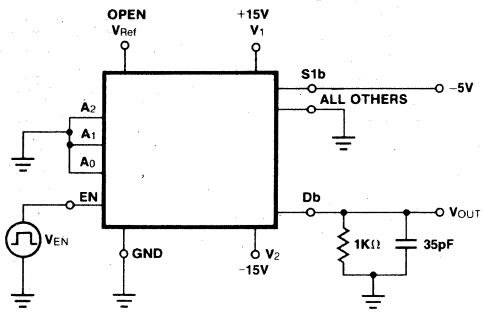
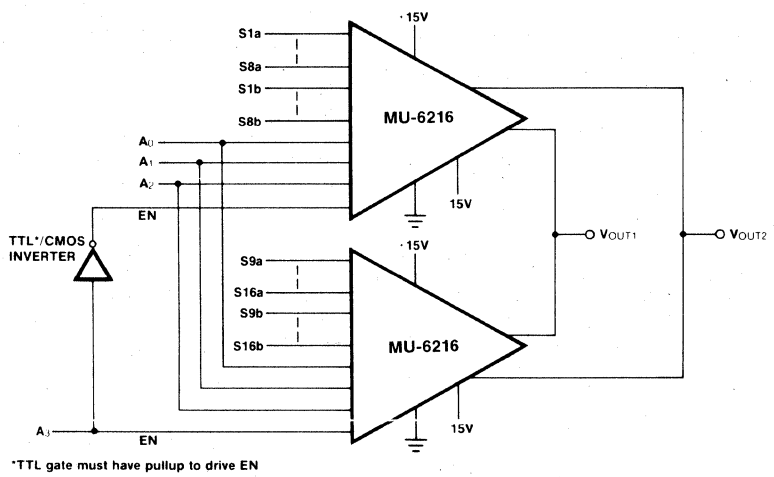


Figure 3

MU-6216 APPLICATIONS

I. 2 out of 32 channel multiplexer



*TTL gate must have pullup to drive EN

Figure 4

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1a	
0	0	0	1	S2a	
0	0	1	0	S3a	
0	0	1	1	S4a	
0	1	0	0	S5a	
0	1	0	1	S6a	
0	1	1	0	S7a	
0	1	1	1	S8a	V_{OUT1}
1	0	0	0	S9a	
1	0	0	1	S10a	
1	0	1	0	S11a	
1	0	1	1	S12a	
1	1	0	0	S13a	
1	1	0	1	S14a	
1	1	1	0	S15a	
1	1	1	1	S16a	

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1b	
0	0	0	1	S2b	
0	0	1	0	S3b	
0	0	1	1	S4b	
0	1	0	0	S5b	
0	1	0	1	S6b	
0	1	1	0	S7b	
0	1	1	1	S8b	V_{OUT2}
1	0	0	0	S9b	
1	0	0	1	S10b	
1	0	1	0	S11b	
1	0	1	1	S12b	
1	1	0	0	S13b	
1	1	0	1	S14b	
1	1	1	0	S15b	
1	1	1	1	S16b	

MU-6216 APPLICATIONS

II. 2 out of 32 channel multiplexer using 2 MU-6216s; using an AS-5043 for submultiplexing.

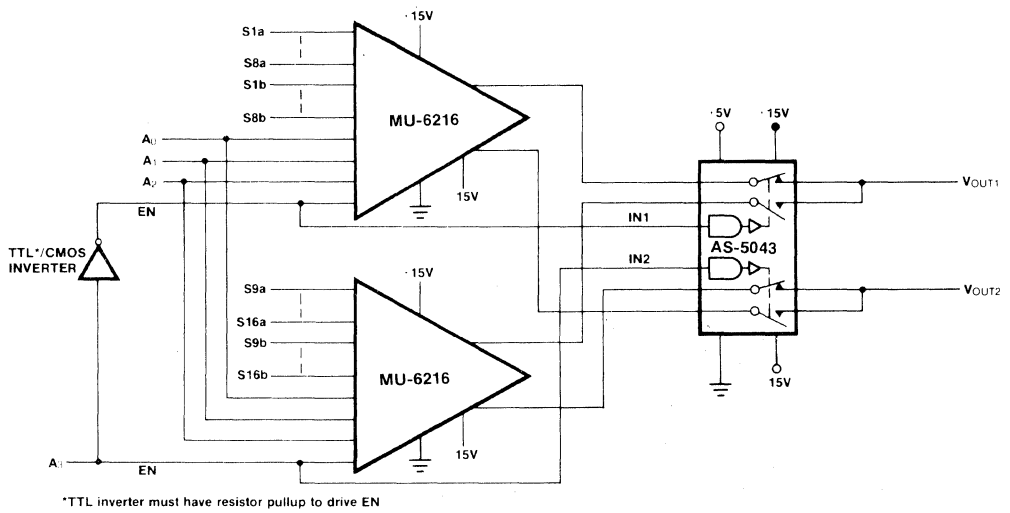


Figure 5

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1a	
0	0	0	1	S2a	
0	0	1	0	S3a	
0	0	1	1	S4a	
0	1	0	0	S5a	
0	1	0	1	S6a	
0	1	1	0	S7a	
0	1	1	1	S8a	V_{OUT1}
1	0	0	0	S9a	
1	0	0	1	S10a	
1	0	1	0	S11a	
1	0	1	1	S12a	
1	1	0	0	S13a	
1	1	0	1	S14a	
1	1	1	0	S15a	
1	1	1	1	S16a	

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1b	
0	0	0	1	S2b	
0	0	1	0	S3b	
0	0	1	1	S4b	
0	1	0	0	S5b	
0	1	0	1	S6b	
0	1	1	0	S7b	
0	1	1	1	S8b	V_{OUT2}
1	0	0	0	S9b	
1	0	0	1	S10b	
1	0	1	0	S11b	
1	0	1	1	S12b	
1	1	0	0	S13b	
1	1	0	1	S14b	
1	1	1	0	S15b	
1	1	1	1	S16b	

MU-6216 APPLICATIONS

III. 2 out of 64, using 4 MU-6216s and 2 AS-5043s.

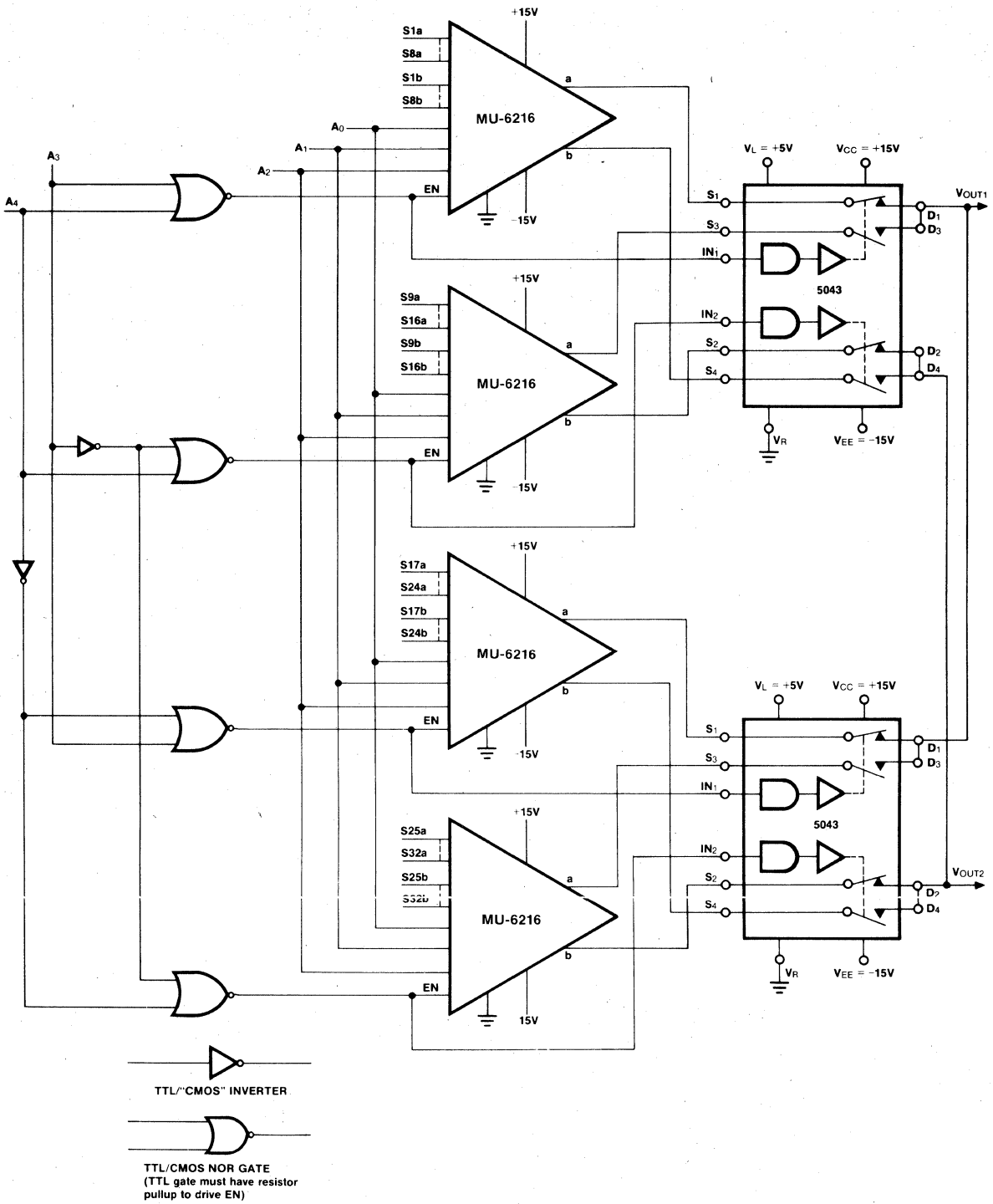


Figure 6

IV. GENERAL NOTE ON EXPANDABILITY

The MU-6216 is a two tier multiplexer wherein 8 pairs of input channels are routed to a pair of outputs in blocks of 4 channels at a time. Each block of 4 input channels is routed to one common output channel; thus the submultiplexed system looks like 4 bloks of 4 inputs routed to 4 different outputs, and the 4 outputs are tied in pairs. Thus 20 switches are needed to handle the 16 channels of information. The advantage of this scheme is lower output capacity and lower leakage than a system with all 8 channels tied to one common output. Also the expandability into 2 out of 32, 64, 128, etc. is facilitated. Figures 4, 5, and 6 show how the MU-6216 is expanded.

Figure 4 shows a 2 out of 32 multiplexer using 2 of the MU-6216s. Since the 6216 is itself a 2 tier mux, the system as shown is basically a 2 tier system. Corresponding output points of each of the 6216 are connected together, and the enable input strobe is used as the A_3 input. Since each output (pins 2 and 28) corresponds to an "on" fet and an "off" fet, the overall system looks like 1 "on" fet and 3 "off" fets for each of the V_{out1} and V_{out2} outputs. Thus the output leakage will be 1 $I_{D(on)}$ plus 3 $I_{D(off)}$s or about 0.4 nA typical, at room temperature. Thruput speed will be typically 0.8μs for t_{on} and 0.3μs for t_{off}. Thruput channel resistance will be in the 500 ohm area.

Figure 5 shows the same 2 out of 32 mux as Figure 4, except that a third tier of submultiplexing is added to further reduce leakage and output capacity. The MU-6216 has typical on resistance of 50 ohms (max. is 75 ohms) so it only increases thruput channel resistance from the 500 ohms of Figure 4 to about 550 ohms for Figure 5. Thruput channel speed is a little slower by about 0.5μs for both on and off time. Output leakage is about 0.2 nA typical.

Figure 6 shows a 2 out of 64 mux using 3 tier muxing (similar to Figure 5 application). Again the Model AS-5043 is used to get the third tier of muxing. Each V_{out} point will see 3 off channels and 1 on channel at any time so that the typical leakages will be about 0.4 nA. Thruput channel resistance will be in the 550 ohm area and thruput switching speeds will be about 1.3μs for on time and 0.8μs for off time.

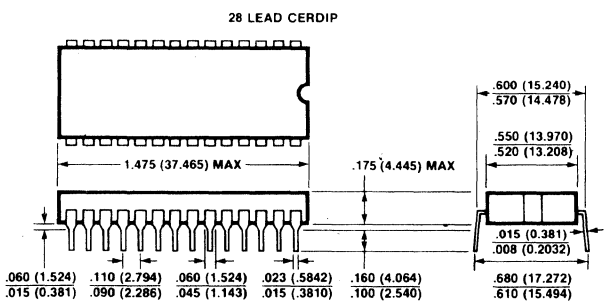
The MU-6216 was chosen as the third tier of the mux because it will switch the same AC signals as the MU-6216 (typically plus and minus 15V) and break before make switching is guaranteed so that the muxing system remains a break-before-make. Also power supply quiescent currents are typically 1μA from any supply, so that no excessive system power is generated. Also the logic of the 5043 is such that it can be tied directly to the enable input (as shown in the figures) with no extra logic being required.

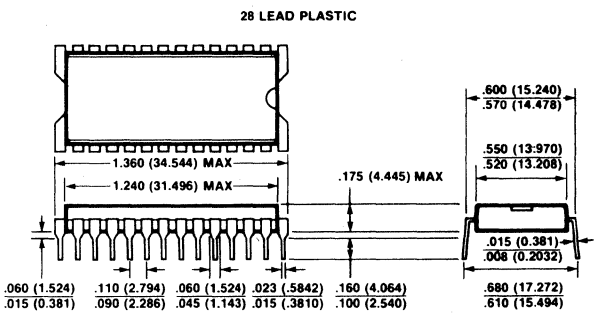
V. ENABLE INPUT STROBING LEVELS

The enable input (EN) acts as an enabling or disabling pin for the MU-6216 when used as a 2 out of 16 channel mux; however, when expanding the mux to more than 16 channels, the EN pin acts as another address input. As an example, we see in Figures 4 and 5 that the EN pin acts as the A_3 input.

For the system to function properly the EN input (pin 18) must go to 5V ±5% for the high state and less than 0.8V for the low state. When using TTL logic, a pull-up resistor should be used to pull the output voltage up to 5V; this resistor should be 1k ohm or less. When using CMOS logic, the high state goes up to the power supply so no pull-up is required.

PACKAGE DIMENSIONS





NOTE: This multiplexer does not require external resistors and/or diodes to eliminate what is commonly known as a latch up or SCR action. Because of the elimination of external resistors in each channel the $r_{DS(ON)}$ of the switch is maintained at specified values.

Low ON-Resistance CMOS Analog Multiplexers MV Series

FEATURES

- **Low ON Resistance**
- **Break-Before-Make Switching**
- **Dielectrically Isolated CMOS**
- **Single Ended or Differential**
- **Fast Settling Time**
- **DTL/TTL/CMOS Compatible**

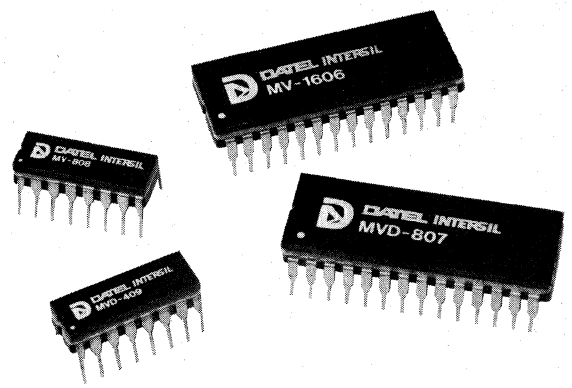
GENERAL DESCRIPTION

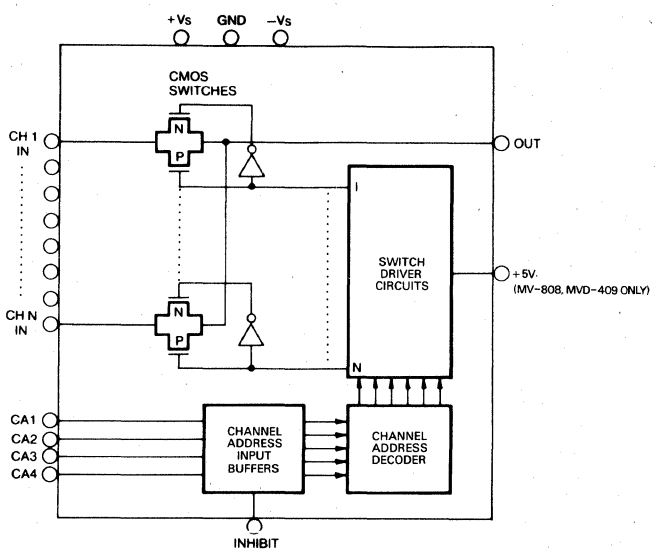
The MV series analog multiplexers are 4, 8, and 16 channel monolithic devices featuring a low ON resistance of 270 ohms. These units are manufactured with CMOS technology using a dielectric isolation process. There are 8 and 16 channel single-ended models and 4 and 8 channel differential models in this series. Channel addressing is done by a 2, 3, or 4 bit binary code; an inhibit input enables or disables the entire device to permit expansion of the number of channels by using several devices together. Another important feature is break-before-make switching, which insures that no two channels are ever momentarily shorted together.

With a high impedance load, transfer accuracies of 0.01% can be achieved at channel sampling rates up to 350 KHz. These multiplexers are ideal for multi-channel data acquisition systems where the multiplexer operates into a high impedance load such as a sample-hold, buffer amplifier, or instrumentation amplifier. The channel ON resistance is less than 500 ohms over full operating temperature range.

These multiplexers are packaged in 16 pin and 28 pin ceramic DIP's. Standard versions operate over 0 to 70°C while military versions operate from -55°C to +125°C. The MV series is similar in specification to Datel's MX series multiplexers. The MX series is recommended where input overvoltage protection to 20 volts above supply voltage is required and where higher channel ON resistance can be tolerated.

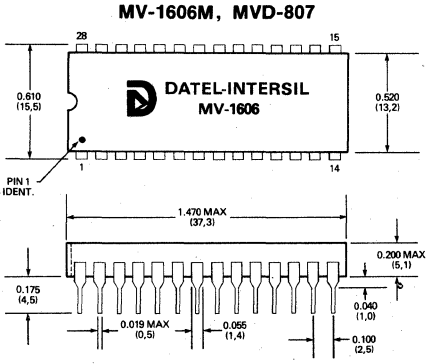
CAUTION:
These multiplexers are CMOS devices and should be handled with anti-static precautions until installed in a circuit with leakage return paths.



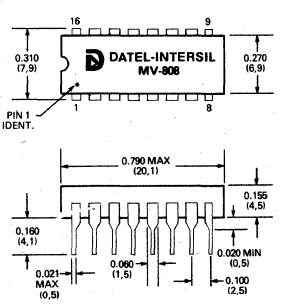


MECHANICAL DIMENSIONS - INCHES (MM)

MV-1606M, MVD-807



MV-808, MVD-409



DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS
Typical at ±15V supplies (and +5V supply for MV-808 & MVD-409), unless otherwise noted.

	MV-808 MV-808M	MV-1606 MV-1606M	MVD-409 MVD-409M	MVD-807 MVD-807M
MAXIMUM RATINGS				
Power Supply, analog	±20V	±20V	±20V	±20V
Power Supply, digital	+30V	—	+30V	—
Analog Input Voltage	±|Vs+2V|	±|Vs+2V|	±|Vs+2V|	±|Vs+2V|
Digital Input Voltage	±Vs	±|Vs+4V|	±Vs	±|Vs+4V|
Package Dissipation, max.	780mW	1200mW	780mW	1200mW
ANALOG INPUTS				
Number of Channels	8	16	4	8
Type	Single Ended	Single Ended	Differential	Differential
Input Voltage Range	±15V	±15V	±15V	±15V
Channel ON Resistance[1]	250Ω	270Ω	250Ω	270Ω
Channel ON Resistance[2], max. over temp.	500Ω	500Ω	500Ω	500Ω
Channel OFF Input Leakage	20pA	30pA	20pA	30pA
Channel OFF Output Leakage	100pA	1.0nA	50pA	1.0nA
Channel ON Leakage	100pA	1.0nA	50pA	1.0nA
Channel OFF Input Capacitance	4pF	4pF	4pF	4pF
Channel OFF Output Capacitance	20pF	44pF	10pF	22pF
DIGITAL INPUTS[3]				
Logic "0" Threshold, max.	+0.4V	+0.8V	+0.4V	+0.8V
Logic "1" Threshold,[4] min.	+4.0V	+2.4V	+4.0V	+2.4V
Input Current, max., HI or LO	1μA	5μA	1μA	5μA
Channel Address Coding	3 Bits	4 Bits	2 Bits	3 Bits
Channel Inhibit, all channels OFF	Logic "1"	Logic "0"	Logic "1"	Logic "0"
PERFORMANCE				
Transfer Error, max.	0.01%	0.01%	0.01%	0.01%
Crosstalk, 10KHz	-86dB	-86dB	-86dB	-86dB
Common Mode Rejection	—	—	120dB	120dB
Settling Time, 20V to 0.1%	1.1 μsec.	1.2 μsec.	1.1 μsec.	1.2 μsec.
Settling Time, 20V to 0.01%	2.8 μsec.	2.4 μsec.	2.8 μsec.	2.4 μsec.
Turn ON Time	350 nsec.	300 nsec.	350 nsec.	300 nsec.
Turn OFF Time	250 nsec.	220 nsec.	250 nsec.	220 nsec.
Inhibit/Enable Delay	300 nsec.	300 nsec.	300 nsec.	300 nsec.
Break-Before-Make Delay	100 nsec.	80 nsec.	100 nsec.	80 nsec.
POWER REQUIREMENT				
Power Supply Voltage	±15VDC	±15VDC	±15VDC	±15VDC
Power Supply Current,[5] max.	+1, -2mA	+5, -2mA	+1, -2mA	+5, -2mA
Digital Supply Voltage	+5VDC	—	+5VDC	—
Digital Supply Current, max.	2mA	—	2mA	—
PHYSICAL-ENVIRONMENTAL				
Operating Temp. Range, standard version	0 to 70°C	0 to 70°C	0 to 70°C	0 to 70°C
Operating Temp. Range, military, version	-55° to +125°C	-55° to +125°C	-55° to +125°C	-55° to +125°C
Storage Temperature Range	-65° to +150°C	-65° to +150°C	-65° to +150°C	-65° to +150°C
Package	16 Pin DIP	28 Pin DIP	16 Pin DIP	28 Pin DIP

NOTES:
1. For MV-1606M & MVD-807M typical value is 170 ohms.
2. For MV-1606M & MVD-807M max. value is 400 ohms.
3. Channel address and inhibit inputs.
4. For MV-808 and MVD-409, to drive from DTL/TTL logic 1K pull-up resistors to +5V should be used.
5. For MV-1606M & MVD-807M max. current is +3, -1 mA. For MV-808M & MVD-409M max. current is +0.5, -1 mA for analog supply, 1mA for digital supply.

CONNECTION AND APPLICATION

CHANNEL ADDRESSING

MV-1606

8	4	2	1	INHIB.	ON CHANNEL
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

MV-808, MVD-807

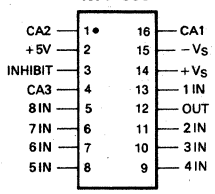
4	2	1	MVD-807 INHIB.	MV-808 INHIB.	ON CHANNEL
X	X	X	0	1	NONE
0	0	0	1	0	1
0	0	1	1	0	2
0	1	0	1	0	3
0	1	1	1	0	4
1	0	0	1	0	5
1	0	1	1	0	6
1	1	0	1	0	7
1	1	1	1	0	8

MVD-409

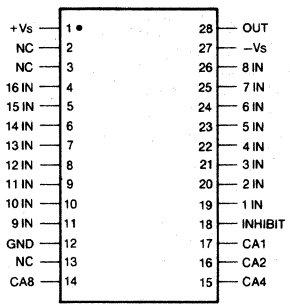
2	1	INHIB.	ON CHANNEL
X	X	1	NONE
0	0	0	1
0	1	0	2
1	0	0	3
1	1	0	4

PIN CONNECTIONS

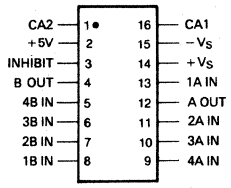
MV-808



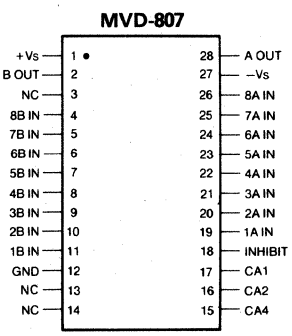
MV-1606



MVD-409



MVD-807



NOTES:

CA = CHANNEL ADDRESS
VS = SUPPLY VOLTAGE
NC = NO CONNECTIONS

TOP VIEW SHOWN

TECHNICAL NOTES

1. The transfer accuracy of the MV series multiplexers depends on both the source resistance and load resistance. For example, with zero source resistance and assuming 500 ohms max. channel ON resistance, the load impedance must be at least 5 megohms to achieve 0.01% accuracy. In practice it is recommended that a load impedance of 10^8 ohms or more be used. This is a typical input impedance value for most IC operational amplifiers connected in the follower mode (see Datel's AM-400 series) or for IC sample-holds (see Datel's SHM-IC-1 or SHM-LM-2). Source resistance should be kept as low as possible so that accuracy or settling time are not degraded. Less than 250 ohms is recommended.

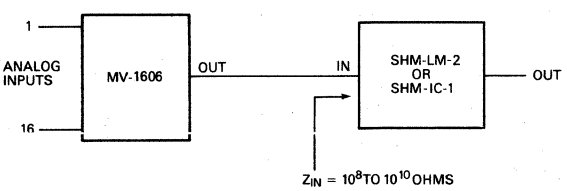
2. For differential operation either two unity gain buffers or an instrumentation amplifier (such as Datel's AM-435) is recommended as the output load. To maintain high CMR, source impedance unbalance must be kept to a minimum, and amplifiers with high CMR should be used.

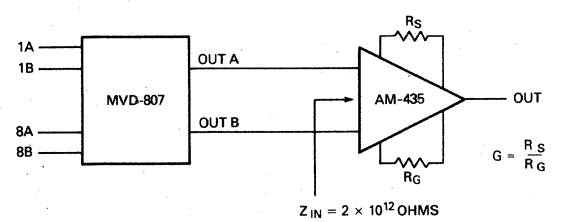
3. The maximum analog input overvoltage for the MV series is ±|Vs+2V|. The maximum digital input voltage is ±Vs. It should be noted that the logic (channel address) inputs are protected with resistors and clamp diodes but the analog inputs are not. Because the analog inputs are not protected, the low ON resistance is achieved.

4. Channel expansion is accomplished by use of the inhibit input of the multiplexers. To expand the number of channels, use multiple multiplexers with the inhibit inputs connected to a decoder.

5. For the MV-808 and MVD-409 it is recommended that 1K pull-up resistors to the +5V logic supply be used when the logic inputs are driven from DTL or TTL circuits. Only these two models require a +5V logic supply.

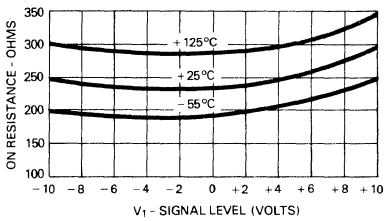
CIRCUIT CONNECTIONS



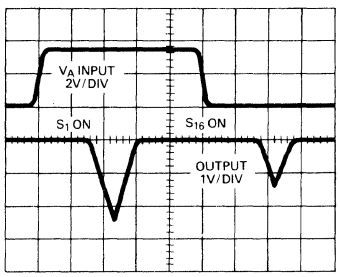


PERFORMANCE GRAPHS

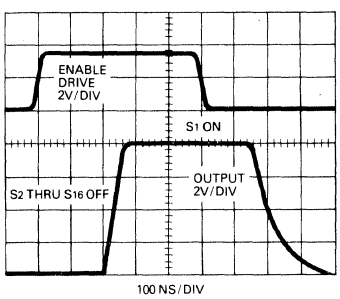
ON RESISTANCE VS. TEMPERATURE



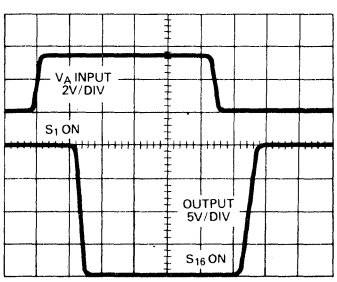
BREAK-BEFORE-MAKE DELAY
(t_{OPEN})



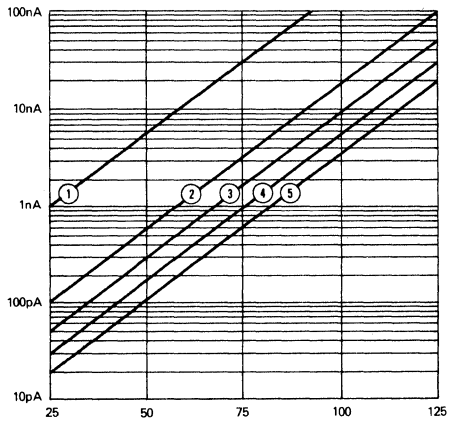
ENABLE DELAY
($t_{ON(EN)}$, $t_{OFF(EN)}$)



ACCESS TIME

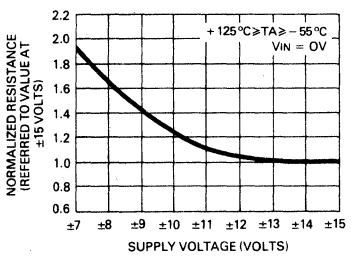


LEAKAGE CURRENT VS. TEMPERATURE



1. MV-1606, MVD-807 CHANNEL OFF OUTPUT LEAKAGE
2. MV-808 CHANNEL OFF OUTPUT LEAKAGE
3. MVD-409 CHANNEL OFF INPUT LEAKAGE
4. MV-1606, MVD-807 CHANNEL OFF INPUT LEAKAGE
5. MV-808, MVD-409 CHANNEL OFF INPUT LEAKAGE

NORMALIZED ON RESISTANCE VS. SUPPLY VOLTAGE



ORDERING INFORMATION

MODEL	CHANNELS	OPERATING TEMP. RANGE
MV-808	8 S.E.	0 to 70C
MV-808M	8 S.E.	-55 to +125C
MV-1606	16 S.E.	0 to 70C
MV-1606M	16 S.E.	-55 to +125C
MVD-409	4 Diff.	0 to 70C
MVD-409M	4 Diff.	-55 to +125C
MVD-807	8 Diff.	0 to 70C
MVD-807M	8 Diff.	-55 to +125C

THESE MULTIPLEXERS ARE COVERED BY GSA CONTRACT

DATEL INTERSIL
11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617)339-9341 / TWX 710-346-1953 / TLX 951340
Santa Ana, (714)835-2751, (L.A.) (213)933-7256 • Sunnyvale, CA (408)733-2424 • Gaithersburg, MD (301)840-9490
• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

4, 8, and 16 Channel CMOS Multiplexers MX Series

FEATURES

- **Dielectrically Isolated CMOS**
- **Break-Before-Make Switching**
- **Single-Ended and Differential**
- **Overvoltage Protection**
- **DTL/TTL/CMOS Compatible**
- **7.5 mW Standby Power**

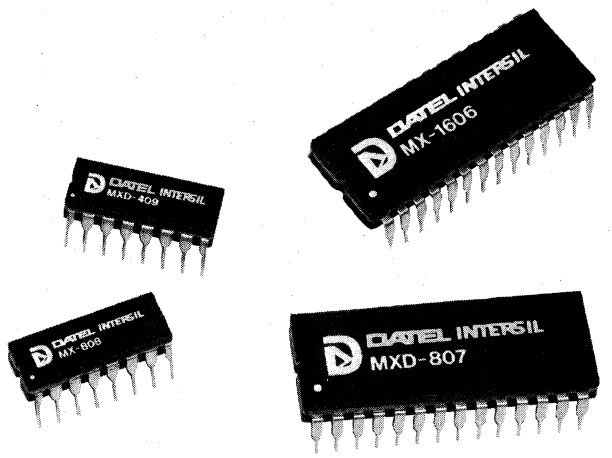
GENERAL DESCRIPTION

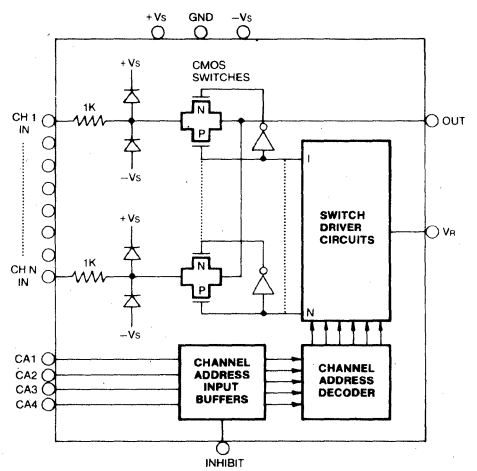
The MX series analog multiplexers are 4, 8, and 16 channel monolithic devices manufactured with a dielectrically isolated complementary MOS process. The circuits incorporate analog and digital input protection which protects the units from both overvoltage and loss of power. The digital inputs are DTL/TTL/CMOS compatible and address the proper channel by means of a 2, 3, or 4 bit binary code. An inhibit input enables or disables the entire device and thus permits expansion of the number of channels by using several devices together. Another important feature of these multiplexers is the use of break-before-make switching to insure that no two channels are ever momentarily shorted together.

Transfer accuracies of .01% can be achieved at channel sampling rates up to 200 kHz and over ±10V signal ranges. These multiplexers are ideal for multi-channel data acquisition systems where the multiplexer operates into a high impedance load such as a sample-hold, buffer amplifier, or instrumentation amplifier. Channel ON resistance is typically 1.5K at 25°C and is less than 2K over the operating temperature range.

Power consumption is only 7.5 mW at standby and 15 mW at 100 kHz switching rate. Power supply range is ±5V to ±20V. The devices are packaged in 16 pin or 28 pin DIP's and operate over the 0°C to 70°C temperature range.

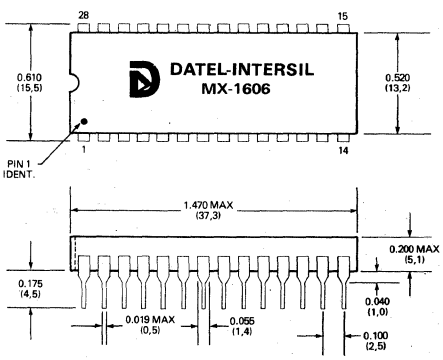
CAUTION: These are CMOS devices and may be damaged by static discharge. Standard anti-static precautions should be taken to prevent possible damage.



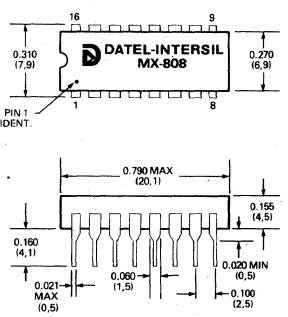


MECHANICAL DIMENSIONS — INCHES (MM)

MX-1606M, MXD-807



MX-808, MXD-409



DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS MX-808 & MXD-409
Typical at 25°C, ±15V supplies, R source <1K, unless otherwise noted

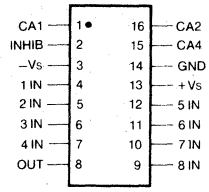
	MX-808 MX-808M	MX-1606 MX-1606M	MXD-409 MXD-409M	MXD-807 MXD-807M
MAXIMUM RATINGS				
Voltage Between Supply Pins	40V	40V	40V	40V
V_{REF} to Ground, V+ to Ground	+20V	+20V	+20V	+20V
Digital Input Overvoltage	±|Vs +4V|	±|Vs +4V|	±|Vs +4V|	±|Vs +4V|
Analog Input Overvoltage	±|Vs +20V|	±|Vs +20V|	±|Vs +20V|	±|Vs +20V|
Package Dissipation, max.	725 mW	1200 mW	725 mW	1200 mW
ANALOG INPUTS				
Number/Type of Channels	8 Single-end	16 Single-end	4 Differential	8 Differential
Input Voltage Range	±15V	±15V	±15V	±15V
Channel ON Resistance	1.5 KΩ	1.5 KΩ	1.5 KΩ	1.5 KΩ
Channel ON Resistance, Over Temp	2.0 KΩ, max.	2.0 KΩ, max.	2.0 KΩ, max.	2.0 KΩ, max.
Channel OFF Input Leakage	30 pA	30 pA	30 pA	30 pA
Channel OFF Output Leakage	1.0 nA	1.0 nA	1.0 nA	1.0 nA
Channel ON Leakage	100 pA	100 pA	100 pA	100 pA
Channel OFF Input Capacitance	5 pF	5 pF	5 pF	5 pF
Channel OFF Output Capacitance	25 pF	50 pF	12 pF	25 pF
DIGITAL INPUTS[1]				
Logic "0" Threshold	+0.8V, max.	+0.8V, max.	+0.8V, max.	+0.8V, max.
Logic "1" Threshold, (TTL)[2]	+4.0V, min.	+4.0V, min.	+4.0V, min.	+4.0V, min.
Logic "1" Threshold, (CMOS)[3]	+6.0V, min.	+6.0V, min.	—	—
Input Current, High or Low	5 μA, max.	5 μA, max.	5 μA, max.	5 μA, max.
Channel Address Coding	3 Bits	4 Bits	2 Bits	3 Bits
Channel Inhibit, All Channels OFF	Logic "0"	Logic "0"	Logic "0"	Logic "0"
PERFORMANCE				
Transfer Error, max.	.01%	.01%	.01%	.01%
Crosstalk, 1 KHz	.005%	.005%	.005%	.005%
Common Mode Rejection	—	—	120 dB	120 dB
Settling Time[4], 20V step to 0.1%	2 μsec	2 μsec	2 μsec	2 μsec
Settling Time[4], 20V Step to 0.01%	3 μsec	3 μsec	3 μsec	3 μsec
Turn ON Time	500 nsec.	500 nsec.	500 nsec.	500 nsec.
Turn OFF Time	300 nsec.	300 nsec.	300 nsec.	300 nsec.
Break Before Make Delay	80 nsec.	80 nsec.	80 nsec.	80 nsec.
Inhibit/Enable Delay	300 nsec.	300 nsec.	300 nsec.	300 nsec.
POWER REQUIREMENT				
Rated Power Supply Voltage	±15 VDC	±15 VDC	±15 VDC	±15 VDC
Power Supply Voltage Range	±5V to ±20V	±5V to ±20V	±5V to ±20V	±5V to ±20V
Quiescent Current, max.	+5, −2 mA	+5, −2 mA	+5, −2 mA	+5, −2 mA
Power Consumption, 10 KHz Sampling	7.5 mW	7.5 mW	7.5 mW	7.5 mW
PHYSICAL-ENVIRONMENTAL				
Operating Temp. Range, Standard Models	0°C to +70°C	0°C to +70°C	0°C to +70°C	0°C to +70°C
Operating Temp. Range, M Suffix Models	−55°C to +125°C	−55°C to +125°C	−55°C to +125°C	−55°C to +125°C
Storage Temp. Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Package	16 Pin DIP	28 Pin DIP	16 Pin DIP	28 Pin DIP

NOTES: 1. The digital inputs are the channel address inputs and the inhibit input.
2. To drive from DTL/TTL circuits, 1K pull-up resistors to +5V are recommended. With models MX-1606 and MXD-807, pin 13 should be left open.
3. For a +6.0V threshold with models MX-1606 and MXD-807, pin 13 is connected to +10V.
4. With a load impedance of >100 megohms in parallel with 2 pF.

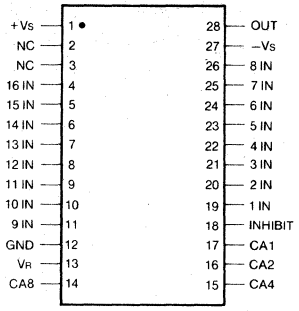
CONNECTION & APPLICATION

PIN CONNECTIONS

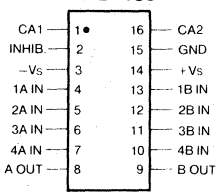
MX-808



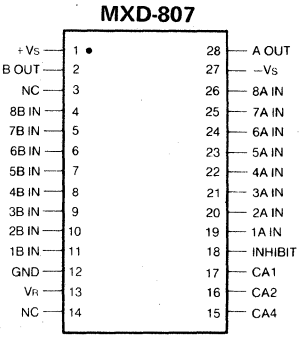
MX-1606



MXD-409



MXD-807



NOTES:

CA - CHANNEL ADDRESS
Vs - SUPPLY VOLTAGE
VR - REFERENCE VOLTAGE
NC - NO CONNECTIONS

CHANNEL ADDRESSING

MX-1606

8	4	2	1	INHIB.	ON CHANNEL
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

MX-808, MXD-807

4	2	1	INHIB.	ON CHANNEL
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

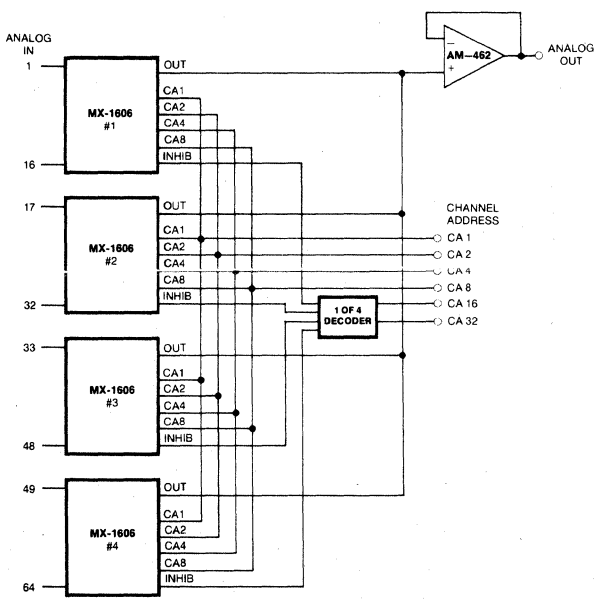
MXD-409

2	1	INHIB.	ON CHANNEL
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

TECHNICAL NOTES

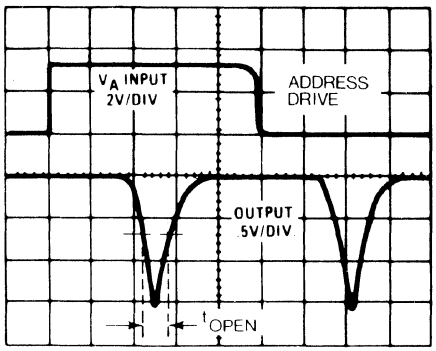
1. The transfer accuracy of these multiplexers depends on both the source resistance and the load resistance. With zero source resistance, and assuming 2K ohms max. channel ON resistance, the load impedance should be at least 20 megohms to achieve .01% accuracy. In practice it is recommended that a load impedance of at least 100 megohms be used to minimize errors. This can be done by using a good high gain, high CMR operational amplifier as a buffer (such as Datel's AM-462). Source resistance should be kept as low as possible so that accuracy is not affected; less than 1K ohms is recommended. Higher source resistance, in addition to affecting accuracy, will degrade the settling time of the multiplexer.
2. For differential operation two buffer amplifiers or a good quality instrumentation amplifier (such as Datel's AM-201) should be used. To maintain high CMR, source impedance unbalance should be kept to a minimum, the highest possible load impedance should be used, and an amplifier with high CMR should be chosen.
3. The maximum analog input overvoltage for these models is ± | Vs +20V | . Maximum logic input overvoltage is ± | Vs +4V | .
4. Channel expansion is accomplished by use of the inhibit input of the multiplexer. A logic "0" on this input disables the multiplexer. The expansion technique shown in the diagram to the right applies to all of the multiplexer models.
5. The reference terminal (V_R) sets the noise immunity level of the input logic for models MX-1606 and MXD-807. In most cases this terminal is left open (TTL inputs). For higher level inputs (+6V min.) this terminal should be connected to +10V. When addressing from DTL/TTL logic it is recommended that 1K ohm pull-up resistors to the +5V supply be used.

EXPANSION TO 64 CHANNELS



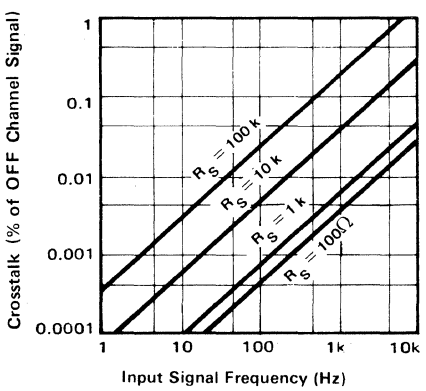
PERFORMANCE GRAPHS

BREAK-BEFORE-MAKE DELAY (t OPEN)

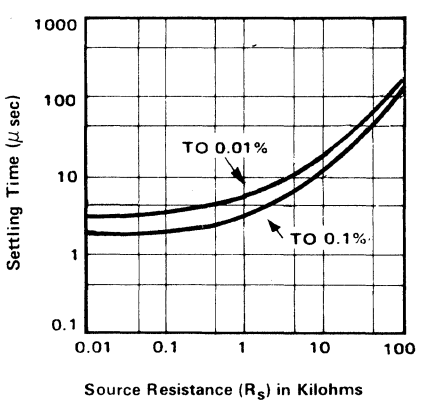


100ns/Div.

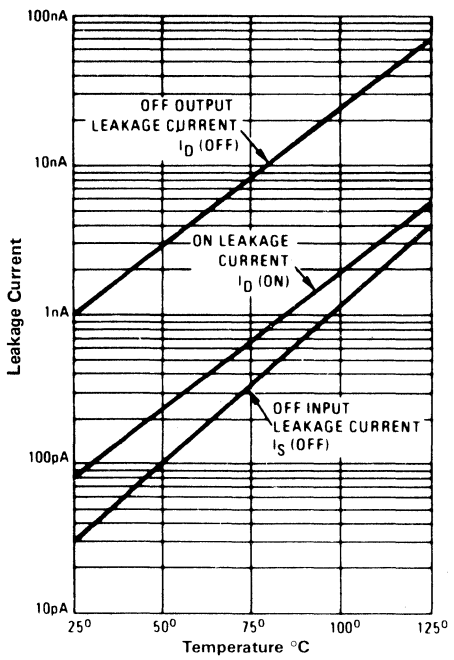
CROSSTALK VS. FREQUENCY OF INPUT SIGNAL



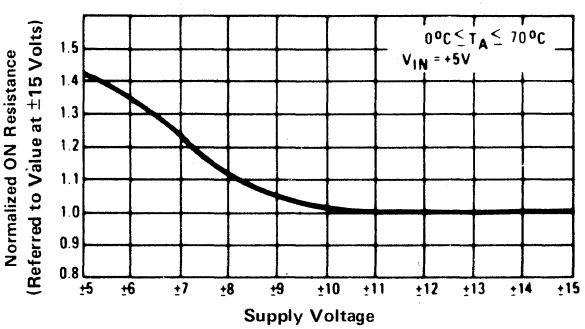
SETTLING TIME VS. SOURCE RESISTANCE (20V STEP)



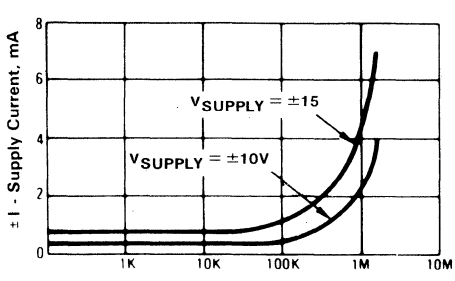
LEAKAGE CURRENT VS. TEMP.



NORMALIZED ON RESISTANCE VS. SUPPLY VOLTAGE



SUPPLY CURRENT VS. SAMPLING FREQUENCY



DATEL INTERSIL
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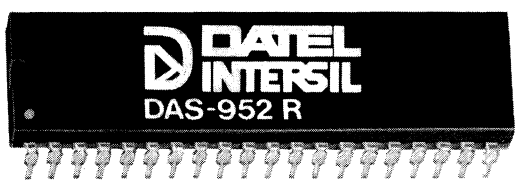
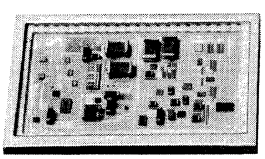
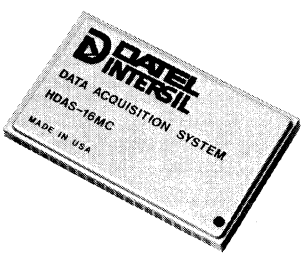
• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

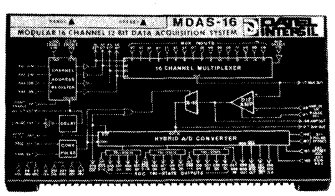
PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Data Acquisition Systems









Quick Selection: Data Acquisition Systems

Specifications at 25° C	DAS-952R Monolithic	HDAS-16MC[1] Hybrid	HDAS-8MC[1] Hybrid
No. Channels	16	16	8
Input Type	Single Ended	Single Ended	Differential
Input Voltage Ranges, Unipolar	0 to +5V	0 to +10mV, 0 to +10V	0 to +10mV, 0 to +10V
Input Voltage Ranges, Bipolar	———	±10mV to ±10V	±10mV to ±10V
Input Impedance	±1μA[5]	100 Meg.	100 Meg.
Channel Addressing	4 Bit Code	4 Bit Code	3 Bit Code
Address Logic Compatibility	CMOS	DTL/TTL	DTL/TTL
Resolution	8 Bits	12 Bits	12 Bits
Nonlinearity, max.	½ LSB	½ LSB	½ LSB
Differential Nonlinearity, max.	½ LSB	½ LSB	½ LSB
Max. Error at maximum throughput	0.2%	.025%	.025%
Temp. Coefficient, max.	50 ppm/° C	30 ppm/° C	30 ppm/° C
No Missing Codes	-25 to +85° C	0 to 70° C	0 to 70° C
Throughput Rate, max.	17 kHz	50 kHz	50 kHz
Acquisition Time	2.5 μsec.	10 μsec.	10 μsec.
Conversion Time	54 μsec.	10 μsec.	10 μsec.
Aperture Time	———	50 nsec.	50 nsec.
Output Coding[3]	Bin	Bin	Bin
Output Logic	3-State TTL	3-State TTL	3-State TTL
Power Requirement	+5V	±15V, +5V	±15V, +5V
Package Size, Inches	40-Pin DIP	2.3 × 1.4 × 0.24	2.3 × 1.4 × 0.24
Package Size, mm		58 × 36 × 6	58 × 36 × 6
Operating Temp. Range	-25 to +85° C	0 to 70° C[2]	0 to 70° C[2]
Price, singles	**$37.50**	**$350.00**	**$350.00**
See Page	272C	278C	278C

NOTES: 1. Includes programmable gain instrumentation amplifier
2. Models for other temperature ranges:
HDAS-16MR, HDAS-8MR, -25° C to +85° C, **$467.00**
HDAS-16MM, HDAS-8MM, -55° C to +125° C, **$787.00**
3. Coding: Bin = Straight Binary or Offset Binary
2C = Two's complement
4. Double Buffered
5. Input Current

MDAS-16 Modular	MDAS-8D Modular	DAS-250A Modular	DAS-250B Modular
16	8	16	16
Single Ended	Differential	Single Ended	Single Ended
0 to +5, +10V	0 to +5, +10V	0 to -10V	———
±2.5, ±5, ±10V	±2.5, ±5, ±10V	———	±5V
100 Meg.	100 Meg.	100 Meg.	100 Meg.
4 Bit Code	3 Bit Code	4 Bit Code	4 Bit Code
DTL/TTL	DTL/TTL	DTL/TTL	DTL/TTL
12 Bits	12 Bits	12 Bits	12 Bits
½ LSB	½ LSB	½ LSB	½ LSB
½ LSB	½ LSB	½ LSB	½ LSB
.025%	.025%	.025%	.025%
30 ppm/° C	30 ppm/° C	45 ppm/° C	45 ppm/° C
0 to 70° C	0 to 70° C	0 to 70° C	0 to 70/° C
50 kHz	50 kHz	250 kHz	250 kHz
6 μsec.	6 μsec.	2 μsec.	2 μsec.
14 μsec.	14 μsec.	2 μsec.	2 μsec.
50 nsec.	50 nsec.	20 nsec.	20 nsec.
Bin, 2C	Bin, 2C	Bin, 2C	Bin, 2C
3-State TTL	3-State TTL	3-State TTL[4]	3-State TTL[4]
±15V, +5V	±15V, +5V	±15V, +5V	±15V, +5V
4.6 × 2.5 × 0.375	4.6 × 2.5 ×0.375	5.0 × 4.5 × 1.5	5.0 × 4.5 × 1.5
117 × 64 × 10	117 × 64 × 10	127 × 114 × 38	127 × 114 × 38
0 to 70° C	0 to 70° C	0 to 70° C	0 to 70° C
$310.00	**$310.00**	**$730.00**	**$730.00**
286C	286C	298C	298C

THESE PRODUCTS ARE COVERED BY GSA CONTRACT

Datel offers modular products in operating temperature ranges of −25 to +85°C (suffix-EX) and −55 to +85°C (suffix-EXX-HS). For information on these high reliability modules contact nearest Datel sales office.

16 Channel, 8 Bit Monolithic Data Acquisition System DAS-952R

FEATURES

- **16 Single Ended Channels**
- **8 Bits Resolution**
- **Monolithic CMOS Construction**
- **Three-State Outputs**
- **Ratiometric Operation**
- **Low Cost**

GENERAL DESCRIPTION

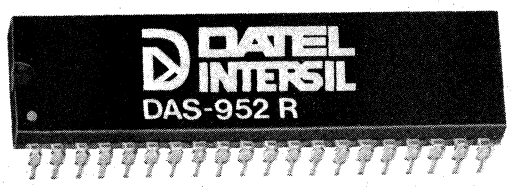
The DAS-952R is a single-chip, 16 channel, 8 bit data acquisition system. Monolithic CMOS technology allows a 16 channel multiplexer, 8 bit successive approximation A/D converter, and microprocessor-compatible control logic to be fabricated on a single chip and contained in a compact Dual-In-Line package.

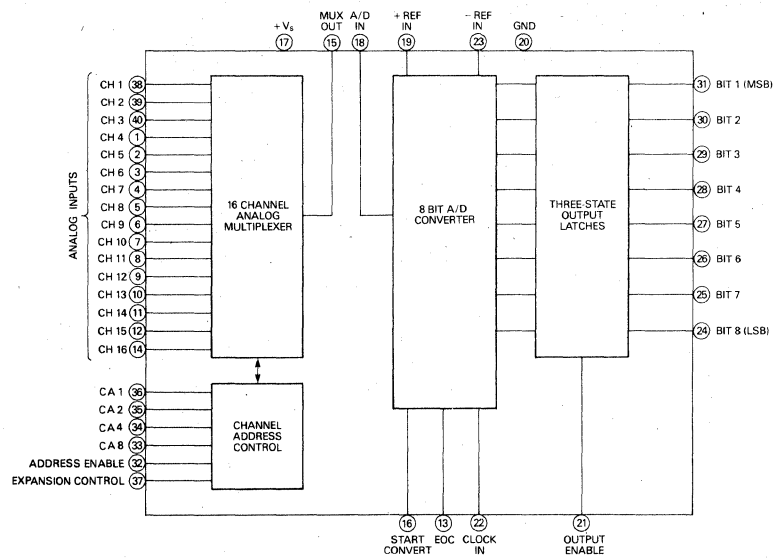
The design of this system emphasizes high accuracy, excellent repeatability, low power consumption, and a minimum of adjustments (no full scale or zero adjustment required). Latched and decoded address inputs and latched TTL three-state outputs allow easy interfacing to microprocessors.

The input multiplexer allows random access to any one of 16 single ended analog input channels and provides necessary logic for additional channel expansion. Connection of the multiplexer output to the converter input is by external pin connection, thus permitting easy signal conditioning such as amplification, linearization, or the use of a sample and hold.

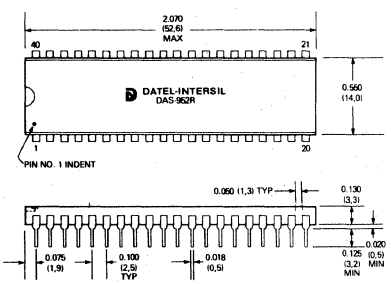
The 8 bit A/D converter uses a 256R ladder network, successive approximation register, and a chopper-stabilized comparator to implement the successive approximation conversion technique with a switching tree. Use of 256R ladder network ensures monotonicity while the chopper-stabilizer comparator makes the converter highly resistant to thermal effects and long term drift. In ratiometric conversion, the converter expresses the analog value being measured as a percentage of reference input. Full scale range may be selected within limits, to adjust the sensitivity of the converter to the desired application or to refer the output to a secondary standard.

Accuracy, speed, flexibility, excellent performance over a wide temperature range (−25°C to +85°C) and low cost make the DAS-952R an easy and practical answer to many data acquisition needs.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	CH. 4 IN	21	OUTPUT ENABLE
2	CH. 5 IN	22	CLOCK INPUT
3	CH. 6 IN	23	−REF. IN
4	CH. 7 IN	24	BIT 8 OUT (LSB)
5	CH. 8 IN	25	BIT 7 OUT
6	CH. 9 IN	26	BIT 6 OUT
7	CH. 10 IN	27	BIT 5 OUT
8	CH. 11 IN	28	BIT 4 OUT
9	CH. 12 IN	29	BIT 3 OUT
10	CH. 13 IN	30	BIT 2 OUT
11	CH. 14 IN	31	BIT 1 OUT (MSB)
12	CH. 15 IN	32	ADDRESS ENABLE
13	E.O.C.	33	CA 8 INPUT
14	CH. 16 IN	34	CA 4 INPUT
15	MULTIPLEXER OUTPUT	35	CA 2 INPUT
16	START CONVERT	36	CA 1 INPUT
17	+Vs	37	EXPANSION CONTROL
18	A/D IN	38	CH. 1 INPUT
19	+REF. IN	39	CH. 2 INPUT
20	GROUND	40	CH. 3 INPUT

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, DAS-952R

(Typical at 25° C, $+V_{SUPPLY} = +V_{REF}$, $-V_{REF} = G_{ND}$, clock = 640 KHz unless otherwise noted)

MAXIMUM RATINGS	
Voltage at Any Pin (Except Digital and REF inputs)	−0.3V to V_s +0.3V
Voltage at Digital Inputs	−0.3V to +15V
$+V_s$	+6.5V
+REF	V_s +0.1V
ANALOG INPUTS	
Number of Channels	16 Single Ended[1]
Input Voltage Range	0 to +5.25V max.
Channel ON-Resistance	1.5KΩ typ, 3KΩ max.[2]
Channel ON-Resistance, 85°C	6KΩ max.
Channel OFF Leakage Current, V_{IN} = +5V	10 nA typ., 200 nA max.
Channel OFF Leakage Current, V_{IN} = 0V	−10 nA typ., −200 nA min.
Channel Input Capacitance	5pF type., 7.5 pF max.
REF Input Resistance	1 KΩ min, 4.5 KΩ typ.[3]
REF Input Voltage	+0.512V to +5.25V[3]
A/D Converter Input Current[4]	±0.5 μA
DIGITAL INPUTS	
Logic HI ("1") Threshold, min.	V_s −1.5V
Logic LO ("0") Threshold, max	+1.5V
Input Current, Max. HI or LO	1.0 μA
Input Capacitance	7.5 pF max.
Clock Frequency	10KHz min., 1.2MHz max.
DIGITAL OUTPUTS	
Logic HI ("1") OUT, I_{OUT} = +360 μA	V_s −0.4V min.
Logic LO ("0") OUT, I_{OUT} = −1.6 mA	+0.45V max.
EOC Logic LO OUT, I_{OUT} = −1.2 mA	+0.45V max.
3-State Output Current, V_{OUT} = +5V	+3 μA max.
3-State Output Current V_{OUT} = 0V	−3 μA max.
3-State Output Capacitance	7.5 pF
Output Coding	Straight Binary, Positive True
CONVERTER PERFORMANCE	
Resoltuion	8 Bits
Linearity Error	±½ LSB, max.
Zero Error	±½ LSB, max.
Full Scale Error	±½ LSB, max.
Total Unadjusted Error	±½ LSB, max.[5]
Power Supply Rejection	±0.15%/V max.[6]
DYNAMIC PERFORMANCE	
Conversion Time	100 μsec typ., 114 μsec max.[7]
MUX Delay, from ADDRESS ENABLE	1 μsec typ., 2.5 μsec max.
3-State Turn-ON Delay	250 nsec max.
POWER REQUIREMENT	
Supply Voltage, rated performance	+5V ±.25V
Supply Voltage, operating range	+4.5V to +6V
Supply Current	300 μA typ., 1000 μA max.
PHYSICAL-ENVIRONMENTAL	
Operating Temperature Range	−25° C to +85° C
Storage Temperature Range	−65° C to +150° C
Package	40 Pin Plastic DIP

NOTES:

1. Logic is provided for expanding the number of channels externally.
2. Channel ON-resistances matched to within 75Ω maximum difference between any two channels.
3. Measured from +REF input to −REF input.
4. This is the comparator input current, a bias current into or out of the chopper stabilized comparator. It varies directly with clock frequency and is relatively independent of temperature.
5. Total unadjusted error is the sum of linearity, zero, and full-scale errors at any point on the transfer function.
6. V_s = +REF = +5V ±.25V
7. For clock frequency of 640 KHz. See technical note 4.

TECHNICAL NOTES

1. The DAS-952R is a ratiometric data acquisition system. The analog input voltage is expressed as a percentage of full scale voltage range. Full scale voltage range may be varied from +0.512V to +5.25V. The system uses an 8 bit converter with the full scale range divided into 256 steps (one step = 1 LSB). The ability to select the full scale range by means of the reference voltage allows selection of the size of the LSB, thereby allowing selection of the converter's sensitivity. The center of the full scale voltage range must be held within ±0.1V of the center of the supply range because the analog switch tree changes from N-channel switches to P-channel switches at this point. Failure to maintain the symmetry of these ranges may result in erratic switch operation. This condition is automatically satisfied in configurations where +REF = $+V_s$ and −REF = GND. For configurations where +REF $< +V_s$, −REF must be greater than GND by an equal amount. +REF can never exceed $+V_s$ and −REF can never be less than GND.
2. The system requires less than 1 mA of supply current. For applications where full scale range is selected between +4.75V and +5.25V, the reference can be used to generate the supply.
3. To preserve the accuracy of the system over its full operating temperature range, the reference source should have a temperature coefficient of 20 ppm/°C or less. For ambient temperature changes less than 75° C, a reference temperature coefficient of 30 ppm/° C is sufficient to maintain accuracy.
4. Conversion time and throughput rate for the DAS-1952R is dependent on external clock frequency. The clock may be varied from 10 KHz to 12 KHz (see comparator input current graph).

ORDERING INFORMATION

MODEL

DAS-952R

All external devices designated with ◘ in the Applications Diagrams are available from Datel/Intersil.

THIS DATA ACQUISITION SYSTEM IS COVERED BY GSA CONTRACT

DESCRIPTION OF OPERATION

Any one of 16 single-ended analog inputs may be selected by using the address decoder. The multiplexer input selection table shows the channel address input states required to select each channel. Channel address input states are latched into the address decoder on the low-to-high transition of the ADDRESS ENABLE input. Channel address inputs are required to be stable for 50 nsec. before and after the ADDRESS ENABLE low-to-high transition. Additional channel expansion is accomplished by disabling the internal multiplexer (all channels are off when EXPANSION CONTROL input is low) and connecting the additional signals directly to the converter input.

The converter input may also be used to introduce various signal conditioning devices into the analog signal path. The analog signal at the multiplexer input selected is available to the comparator after a maximum delay time of 2.5 usec. The converter's successive approximation register is reset on the positive going edge of 200 nsec. start conversion pulse, and conversion is initiated on the falling edge of the pulse.

A conversion in progress may be interrupted by a new start conversion pulse. The EOC output goes LO in 1 to 8 clock periods after the rising edge of the start conversion pulse. For continuous conversions the EOC output can be tied to the start conversion input and an initial external start conversion pulse applied after power up.

The 8 bit A/D converter requires 64 clock periods to resolve the analog signal voltage level. The converter employs a chopper stabilized comparator for extreme resistance to input offset drift errors. The 256R ladder network ensures monotonicity and does not cause load variations on the reference voltage. The values of the top and bottom resistors are different from the rest of the ladder so that the first output transition occurs when the analog voltage level reaches +½ LSB and each succeeding output transition occurs at intervals of 1 LSB up to full scale.

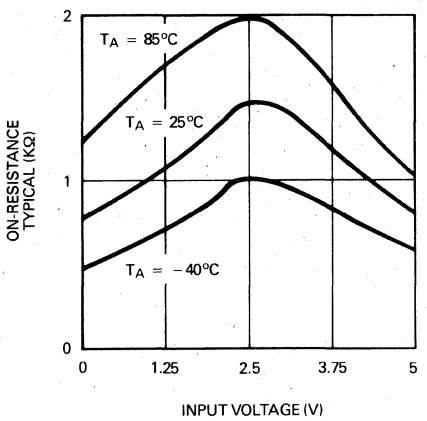
The 8 bit, straight binary, positive true result appears at the three-state output latches, which are enabled when the OUTPUT ENABLE control is HI.

CHANNEL ADDRESS TABLE

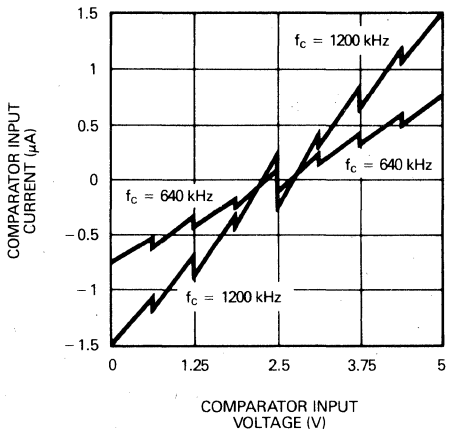
CHANNEL ADDRESS INPUT 8	4	2	1	INHIBIT CONTROL	ON CHANNEL
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

TYPICAL PERFORMANCE

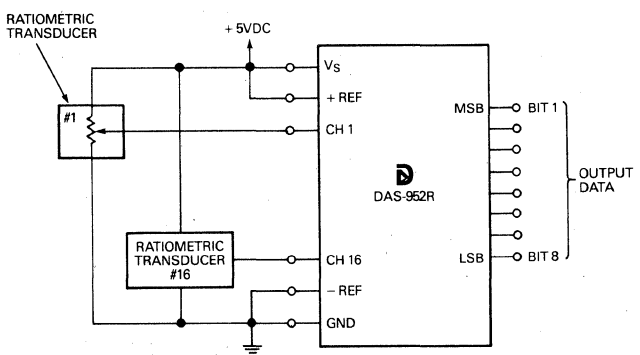
MULTIPLEXER ON RESISTANCE



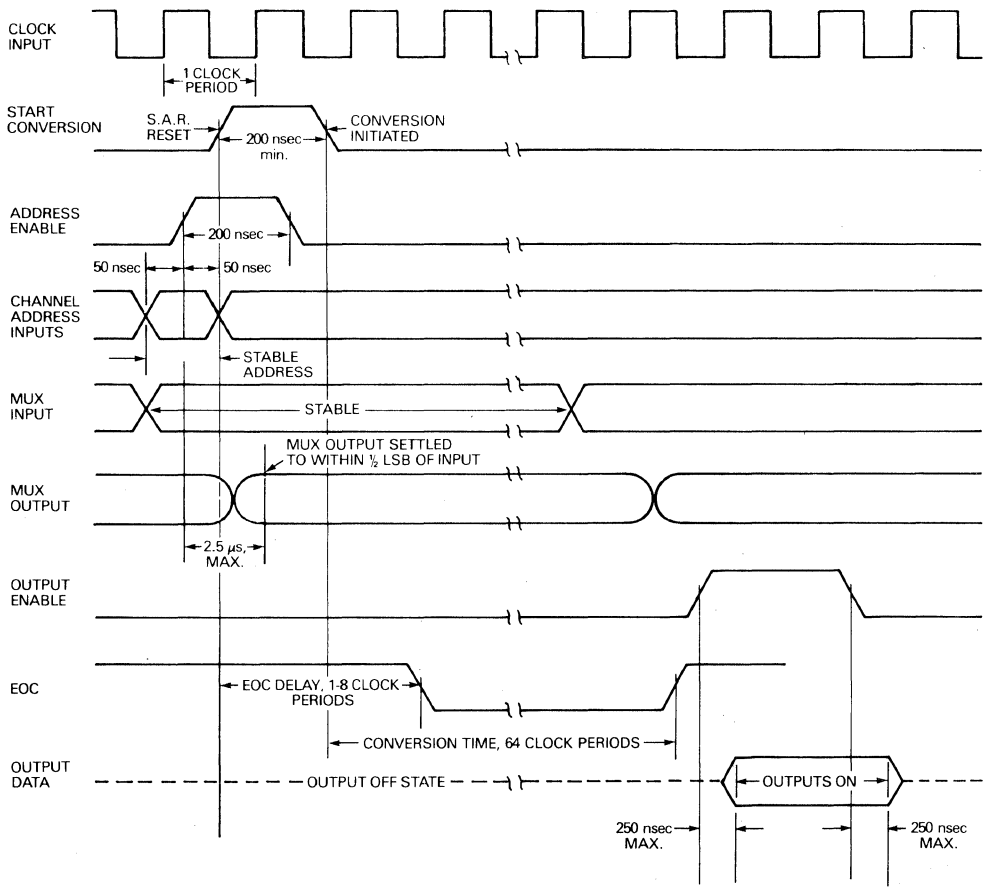
COMPARATOR INPUT CURRENT



RATIOMETRIC CONVERSION SYSTEM

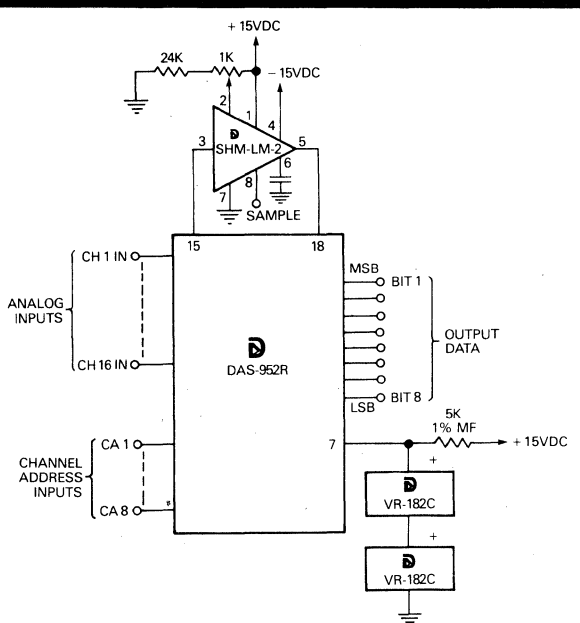


TIMING DIAGRAM



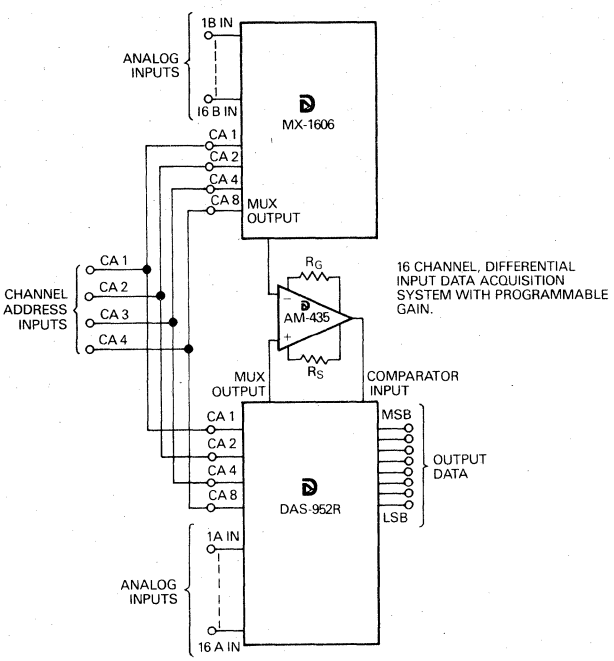
DATA ACQUISITION SYSTEM WITH SAMPLE-HOLD

For applications where a sample-hold is required, connections are made as shown in the accompanying diagram. The sample-hold may be put in the sample mode after the multiplexer output settles (see timing diagram). The start conversion input can be taken high as shown in the timing diagram but should not be taken low until the sample-hold has acquired the input voltage. The acquisition time of the sample-hold is dependent on the value of the hold capacitance. This value must be selected for the acquisition time and hold-mode voltage droop required by the converter speed and accuracy, respectively. Optimal values of hold capacitance may be selected after throughput rate is determined. See SHM-LM-2 data sheet.

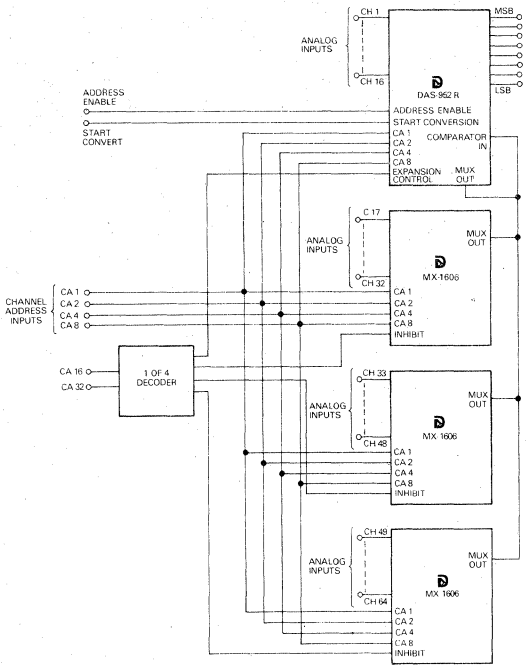


APPLICATIONS

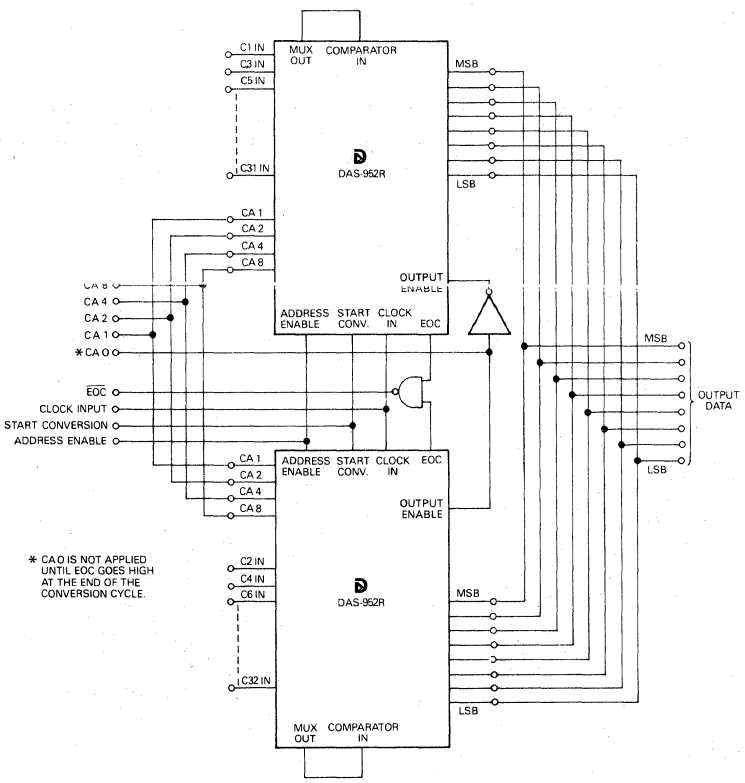
DIFFERENTIAL INPUT CONNECTION



EXPANSION TO 64 CHANNELS

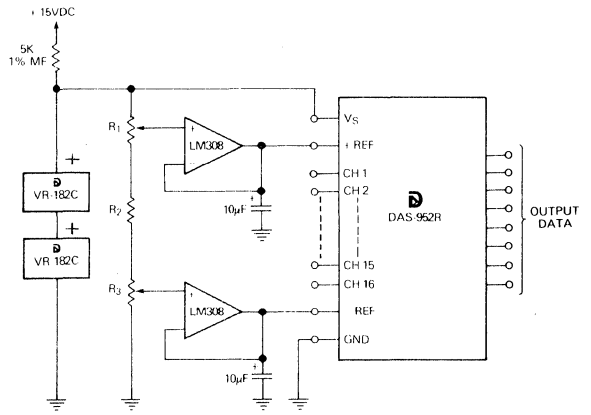


32 CHANNEL, 35KHz DATA ACQUISITION SYSTEM



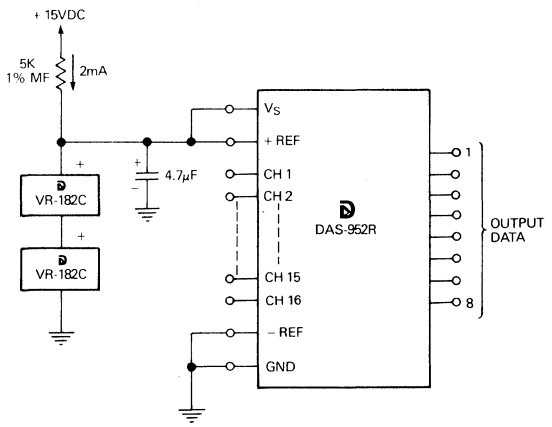
REFERENCE AND SUPPLY CIRCUITS

DUAL ADJUSTABLE REFERENCE

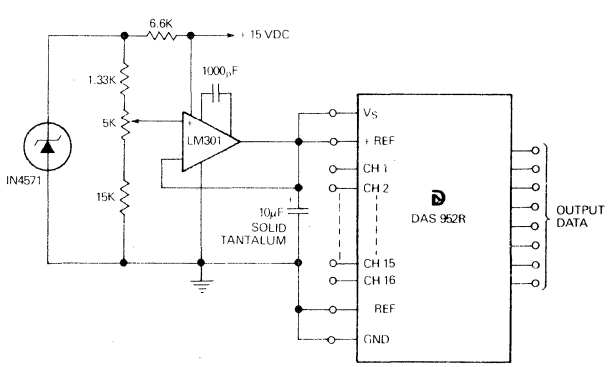


NOTE: VALUES OF R_1, R_2 and R_3 ARE SELECTED TO YIELD THE DESIRED FULL SCALE CONVERSION RANGE. SEE TECHNICAL NOTE 1.

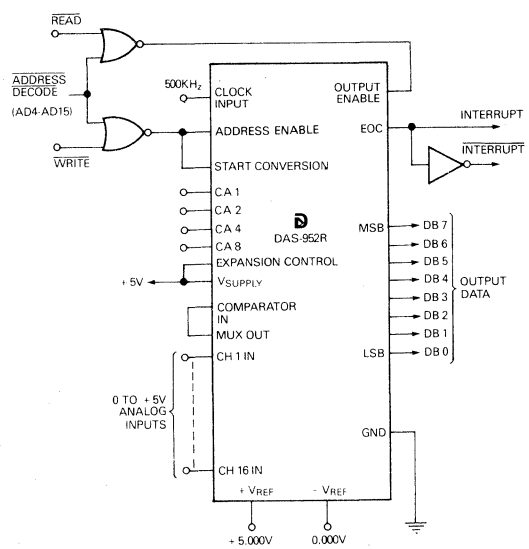
30 PPM/°C REFERENCE AND SUPPLY



ADJUSTABLE REFERENCE AND SUPPLY



TYPICAL MICROPROCESSOR INTERFACE



12 Bit Microelectronic Data Acquisition System Models HDAS-16, HDAS-8

FEATURES

- **Miniature 62 Pin Package**
- **12 Bit Resolution**
- **10mV to 10V Full Scale Range**
- **Three-State Outputs**
- **16 Channels Single Ended or 8 Channels Differential**

GENERAL DESCRIPTION

Utilizing hybrid technology, Datel-Intersil offers a data acquisition system with superior performance and reliability, combined with low cost.

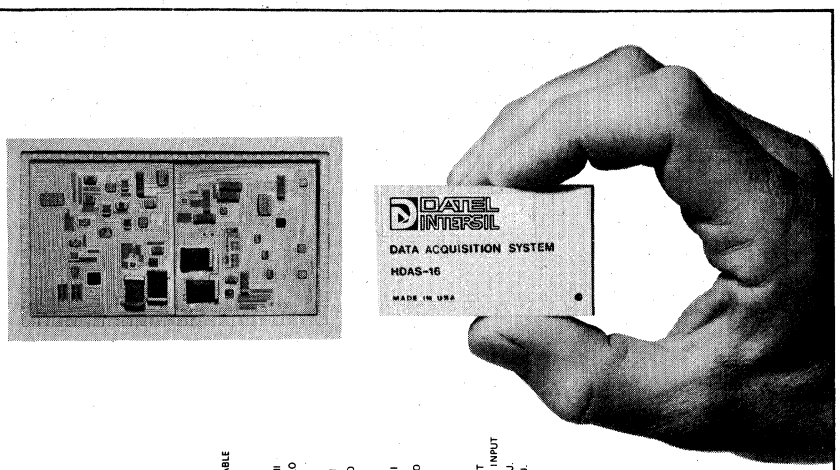
The HDAS-8 with 8 differential input channels and HDAS-16 with 16 single ended input channels are complete high performance 12 bit data acquisition systems in a 62 pin package. Acquisition and conversion time combined is 20μsec. max., giving a minimum throughput rate of 50 kHz. The twelve bit binary data can be transferred out in three four bit bytes, by means of the three-state data bus drivers. Output coding is straight binary in unipolar operation and offset binary in bipolar operation.

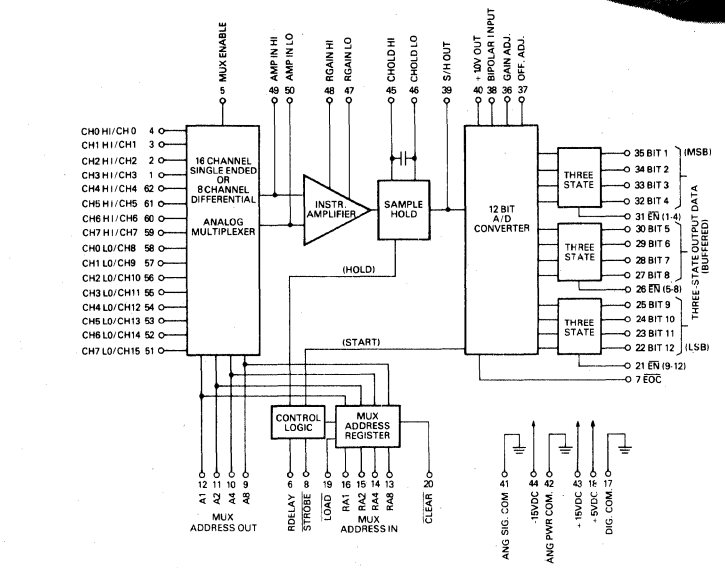
The HDAS circuit includes a multiplexer, programmable gain instrumentation amplifier, sample and hold circuit complete with MOS hold capacitor, 10 volt buffered reference, a twelve bit A/D converter with three-state outputs and digital logic.

The internal instrumentation amplifier is programmed with a single resistor for gains of 1 to 1000. This key feature is useful in low level signal applications involving bridge amplifiers, transducers, strain gauge and thermocouple interface.

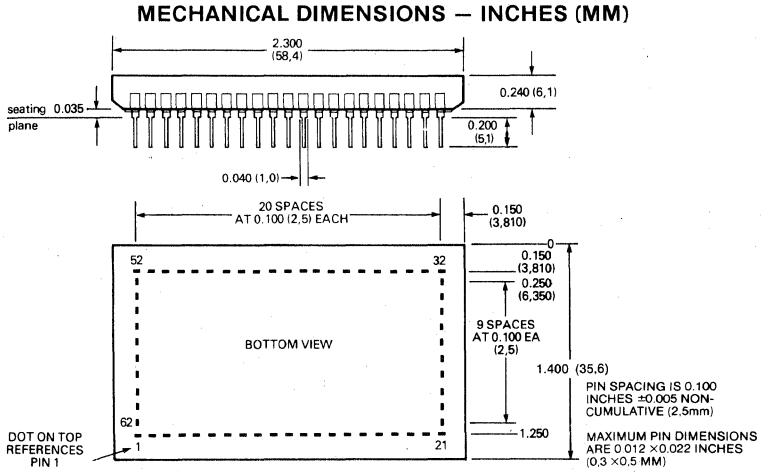
The HDAS is cased in a small hermetic 62 pin package. Models are available in three different temperature ranges: 0 to +70, −25 to +85, and −55 to +125 degrees centigrade.

High reliability versions of each model are also available. Power requirements are ±15VDC and +5VDC.





MECHANICAL DIMENSIONS — INCHES (MM)



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SPECIFICATIONS, HDAS-16 & HDAS-8 (Typical at 25°C, ±15V and +5V supplies unless otherwise indicated)

MAXIMUM RATINGS

+5V Supply	−0.5V to +7.0V
+15V Supply	−0.5V to +18.0V
−15V Supply	+0.5 to −18.0V
Analog Input Channels[1]	±35V
Digital Input Pins	−0.5V to +7.0V

ANALOG INPUTS

Number of Channels	16 Single Ended (HDAS-16) 8 Differential (HDAS-8)
Voltage Ranges[2], **unipolar**	0 to +10mV to 0 to +10V
bipolar	±10mV to ±10V
Input Gain Equation	$G=1+\frac{20K}{RG}$
Common Mode Range	±11V min.
Input Resistance	100 megohms
Gain Equation Error	0.1% max.
Input Bias Current	200pA max.
Bias Current Tempco	Doubles every 10°C
Input Offset Current	50pA max.
Offset Current Tempco	Doubles every 10°C
Input Offset Voltage	8mV typ., 27 mV max.
Offset Voltage Tempco	20μV/°C + (10μV/°C×G)
Voltage Noise (RMS)	
G=1	150μV RTI[3]
G=1000	1.62μV RTI[3]
Input Capacitance, OFF channel	10pF
ON channel	100pF (HDAS-16) 50pF (HDAS-8)

ACCURACY

Resolution	12 Bits
System Error	±0.025% of FSR[4] max. (±1 LSB)
Nonlinearity	±½LSB max.
Differential Nonlinearity	±½LSB max.
Gain Error	Adj. to zero
Offset Error	Adj. to zero
Temp. Coeff. of Gain	±10ppm/°C typ., ±30ppm/°C max.
Temp. Coeff. of Offset	±7ppm/°C of FSR max.
Diff. Linearity Tempco	±3ppm/°C of FSR max.
CMRR(Gain=1)	82 db @ 10 KHz
CMRR(Gain=1000)	110 db @ 60 Hz
Monotonicity	Guaranteed over operating temp range
Power Supply Rejection	.01%/%

DYNAMIC CHARACTERISTICS

Throughput Rate	50 kHz min.
Acquisition Time	9μsec. typ. 10μsec. max.
Conversion Time	9μsec. typ. 10μsec. max.
Aperture Delay Time	100nsec.
Sample-Hold Droop	1 μV/μsec.
Feedthrough (1 KHz)	.01% max.
Channel Crosstalk (MUX)	−80 dB at 1 kHz

DIGITAL OUTPUTS[5]

Parallel Data Out	12 parallel lines of buffered three-state output data. Drives 5 TTL loads.
Coding	Straight binary, Offset binary
Mux Address Out	Buffered output of address register. Drives 5 TTL loads.
$\overline{\text{EOC}}$ (Status)	Drives 5 TTL loads.

DIGITAL INPUTS[6]

$\overline{\text{Enable}}$	Three separate inputs which enable three-state outputs in 4 bit bytes. 1 LS TTL load.
Mux Address In	3 Bit (HDAS-8) or 4 bit (HDAS-16) binary address 1 LS TTL load.
$\overline{\text{Strobe}}$	1 LS TTL load Pulse Width: 40 nsec. $\leq t_W \leq$ EOC
MuxEnable	1 LS TTL load
$\overline{\text{Load}}$	1 LS TTL load
$\overline{\text{Clear}}$	1 LS TTL load
POWER REQUIREMENT	+15VDC ±0.5V @ 67 mA max. −15VDC ±0.5V @ 71 mA max. +5VDC ±0.25V @ 155 mA max.

PHYSICAL ENVIRONMENTAL

Operating Temperature Range	0°C to +70°C (MC) −25°C to +85°C (MR) −55°C to +125°C (MM)
Storage Temperature Range	−65°C to +150°C
Package Size, max.	2.33 × 1.42 × .3 inches (36,07 × 59,18 × 8,89 mm)
Package Type	62 pin, hermetically sealed
Pins	Kovar
Weight	1.4 oz. (40 g)

NOTES:

1. ±20V in power off condition
2. Selectable with proper gain range.
3. RTI - Referred to Input
4. FSR - Full Scale Range 10V for 0 to +10V input, 5V for ±2.5V input.
5. All outputs are LSTTL (low power Schottky)
   Vout ("O") ≤ 0.4V Vout ("1") ≥ 2.7V
6. All inputs are LSTTL
   Vin ("O") < 0.8V Vin ("1") ≥ 2.0V

ORDERING INFORMATION

MODEL	OP. TEMP. RANGE
HDAS-16MC	0°C to 70°C
HDAS-16MR	−25°C to +85°C
HDAS-16MM	−55°C to +125°C
HDAS-8MC	0°C to 70°C
HDAS-8MR	−25°C to +85°C
HDAS-8MM	−55°C to +125°C

Receptacle for PC board mounting can be ordered through AMP Incorporated, #3-331272-4 (component lead spring socket) 62 required.

Evaluation socket, Datel P/N 58-6322-1 Includes PC board with offset and gain potentiometers, bifurcated terminals for electrical connections.

Trimming Potentiometer: TP20K (20 K ohms)

For high reliability versions of the HDAS, contact factory.

THESE MODELS ARE COVERED BY GSA CONTRACT

PIN CONNECTIONS

PIN NO.	HDAS-16	HDAS-8
1	CH3 IN	CH3 HI IN
2	CH2 IN	CH2 HI IN
3	CH1 IN	CH1 HI IN
4	CH0 IN	CH0 HI IN
5	MUX ENABLE	*
6	R DELAY	*
7	E.O.C.	*
8	STROBE	*
9	A8 ┐ MUX	*
10	A4 ├ ADDRESS	*
11	A2 ├ OUT	*
12	A1 ┘	*
13	RA8 ┐ MUX	*
14	RA4 ├ ADDRESS	*
15	RA2 ├ IN	*
16	RA1 ┘	*
17	DIGITAL COM.	*
18	+5VDC	*
19	LOAD ENABLE	*
20	CLEAR ENABLE	*
21	ENABLE (Bits 9-12)	*
22	BIT 12 OUT (LSB)	*
23	BIT 11 OUT	*
24	BIT 10 OUT	*
25	BIT 9 OUT	*
26	ENABLE (Bits 5-8)	*
27	BIT 8 OUT	*
28	BIT 7 OUT	*
29	BIT 6 OUT	*
30	BIT 5 OUT	*
31	ENABLE (Bits 1-4)	*
32	BIT 4 OUT	*
33	BIT 3 OUT	*
34	BIT 2 OUT	*
35	BIT 1 OUT (MSB)	*
36	GAIN ADJ.	*
37	OFFSET ADJ.	*
38	BIPOLAR INPUT	*
39	SAMPLE/HOLD OUT	*
40	+10V OUT	*
41	ANALOG SIGNAL COM	*
42	ANALOG POWER COM.	*
43	+15 VDC	*
44	−15 VDC	*
45	C HOLD HI	*
46	C HOLD LO	*
47	R GAIN LO	*
48	R GAIN HI	*
49	AMP. IN HI	*
50	AMP. IN LO	*
51	CH15 IN	CH7 LO IN
52	CH14 IN	CH6 LO IN
53	CH13 IN	CH5 LO IN
54	CH12 IN	CH4 LO IN
55	CH11 IN	CH3 LO IN
56	CH10 IN	CH2 LO IN
57	CH9 IN	CH1 LO IN
58	CH8 IN	CH0 LO IN
59	CH7 IN	CH7 HI IN
60	CH6 IN	CH6 HI IN
61	CH5 IN	CH5 HI IN
62	CH4 IN	CH4 HI IN

*Same as HDAS-16

TABLE 1 DESCRIPTION OF PIN FUNCTIONS

FUNCTION	LOGIC STATE	DESCRIPTION
DIGITAL INPUTS		
STROBE	"1" to "0"	Initiates acquisition and conversion of analog signal
LOAD	"0"	Random Address Mode Initiated on falling edge of STROBE
	"1"	Sequential Address Mode
CLEAR	"0"	Allows next STROBE pulse to reset MUX ADDRESS to CH0 overriding LOAD command.
MUX ENABLE	"0"	Disables internal MUX
	"1"	Enables internal MUX
MUX ADDRESS IN		Selects channel for Random Address Mode 8,4,2,1 natural binary coding
DIGITAL OUTPUTS		
E.O.C.		End of Conversion (STATUS)
	"0"	Conversion complete
	"1"	Conversion in process
ENABLE (1-4)	"0"	Enables three-state outputs Bits 1-4
	"1"	Disables three-state outputs Bits 1-4
ENABLE (5-8)	"0"	Enables three-state outputs Bits 5-8
	"1"	Disables three-state outputs Bits 5-8
ENABLE (9-12)	"0"	Enables three-state outputs Bits 9-12
	"1"	Disables three-state outputs Bits 9-12
MUX ADDRESS OUT		Output of MUX Address Register 8,4,2,1 natural binary coding
ANALOG INPUTS		
Channel Inputs		Limit voltage to ±20 V beyond power supplies. Ex.-if power supplies ON (±15V), maximum input voltage is ±35 V. If power supplies OFF (0 V), maximum input voltage is ±20 V.
Bipolar Input		For unipolar operation, connect to PIN 39 (S/H OUT) For bipolar operation, connect to PIN 40 (+10 V OUT)
ANALOG OUTPUTS		
S/H OUT		Sample/Hold Output
+10V OUT		Buffered +10 V reference output
ADJUSTMENT PINS		
ANG SIG COM		Low level analog signal return.
GAIN ADJ		External gain adjustment, see calibration instructions.
OFFSET ADJ		External offset adjustment, see calibration instructions.
R GAIN		Optional gain selection point. Factory adjusted for G = 1 when left open.
C HOLD		Optional hold capacitor connection.
R DELAY		Optional acquisition time adjustment when connected to +5V factory adjusted for 9 μS.

TECHNICAL NOTES

1. Input channels are protected to 20 V beyond power supplies. All digital output pins have one second short circuit protection and CHOLD has a ten second short circuit protection.
2. To increase acquisition time allotment, (time for the multiplexer, instrumentation amplifier and sample-hold to settle out) connect a resistor from RDELAY (Pin 6) to +5 V (Pin 18). Refer to Table 2 for delay times and resistor values.
3. An external hold capacitor can be connected between CHOLD HI and CHOLD LO. The addition of this capacitor will improve the sample-hold droop rate especially at high operating temperature ranges. It is recommended that polypropylene or teflon capacitors be used for best results.
4. The HDAS has a self starting circuit for free running sequential operation. If, however, in a power up condition the supply voltage slew rate is less than .3V/usec., the free running state may not be initialized. By applying a negative pulse to the STROBE, this condition will be eliminated.
5. All digital inputs must be stable 50nsec before and 50nsec after high to low transition of STROBE.
6. For UNIPOLAR operation connect BIPOLAR IN (Pin 38) to S/H out (Pin 39). For BIPOLAR operation connect BIPOLAR IN (Pin 38) to +10V OUT (Pin 40).
7. If HDAS reference (+10V OUT) is used for external circuitry, source current should be limited to 1mA.

TABLE 2 INPUT RANGE PARAMETERS (Typical)

INPUT RANGE	GAIN	RGAIN (Ω)	AMPLIFIER SETTLING TIME	RDELAY (Ω)	THROUGHPUT	SYSTEM ACCURACY
±10V	1	NONE	9μsec.	NONE	55.5 KHz	0.009%
±5V	2	20.0K	9μsec.	NONE	55.5 KHz	0.009%
±2.5V	4	6.667K	9μsec.	NONE	55.5 KHz	0.009%
±1V	10	2.222K	9μsec.	NONE	55.5 KHz	0.009%
±200mV	50	408.2	16μsec.	7K	40.0 KHz	0.010%
±100mV	100	202.0	30μsec.	21K	25.6 KHz	0.011%
±50mV	200	100.5	60μsec.	51K	14.5 KHz	0.016%
±20mV	500	40.08	144μsec.	135K	6.5 KHz	0.035%
±10mV	1000	20.02	288μsec.	279K*	3.3 KHz	0.069%

*This value exceeds the maximum recommended for use over military temperature ranges.

NOTES:

$$RGAIN\ (\Omega) = \frac{20{,}000}{(GAIN-1)} \qquad RDELAY\ (\Omega) = \frac{\text{Amp Setting time}}{10^{-9}} - 9K$$

1. Throughput time = Amplifier Setting time and A/D Conversion Time
   A/D Conversion time = 9 μsec
2. Full Scale can be accommodated for analog signal ranges of ±10mV to ±10V.
3. The analog input range to the A/D Converter is 0 to +10.0V for unipolar and −10.0V to +10.0V for bipolar operation.

TABLE 3 CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST	INPUT VOLTAGE
0 TO +5V	ZERO	+0.6 mV
	GAIN	+4.9982V
0 TO +10V	ZERO	+1.2 mV
	GAIN	+9.9963V
BIPOLAR RANGE		
±2.5V	OFFSET	−2.4994V
	GAIN	+2.4982V
±5V	OFFSET	−4.9988V
	GAIN	+4.9963V
±10V	OFFSET	−9.9976V
	GAIN	+9.9927V

CALIBRATION PROCEDURES

A) Offset and gain adjustments may be made by connecting two 20K trim potentiometers as shown in Figure 1.

B) Connect a precision voltage source to pin 4 (CH0). If the HDAS-8 is used, connect pin 58 (CH.0 LO) to analog ground. Ground pin 20 ($\overline{CLEAR}$) and momentarily short pin 8 ($\overline{STROBE}$). Trigger the A/D by connecting pin 7 ($\overline{EOC}$) to pin 8 ($\overline{STROBE}$). Select proper value for RGAIN and RDELAY by referring to Table 2.

C) Adjust the precision voltage source to the value shown in the Calibration Table for the unipolar zero adjustment (ZERO + ½ LSB) or the bipolar offset adjustment (−FS + ½ LSB). Adjust the offset trim potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.

D) Change the output of the precision voltage source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+FS−1½LSB). Adjust the gain trim potentiometer so that the output flickers equally between 1111 1111 1110 and 1111 1111 1111.

FIG 1 EXTERNAL ADJ.

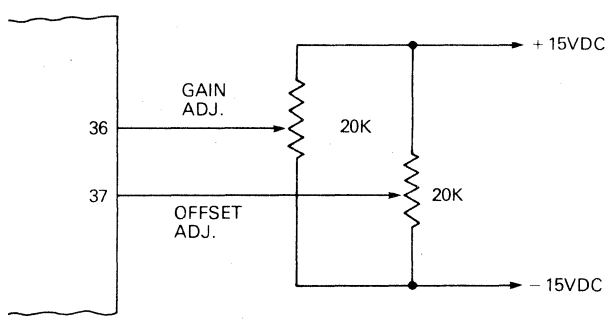


TABLE 4 OUTPUT CODING

	UNIPOLAR		STRAIGHT BINARY
	0 to +10 V	0 to +5V	
+FS-1 LSB	+9.9976	+4.9988	1111 1111 1111
+½FS	+5.0000	+2.5000	1000 0000 0000
+1 LSB	+0.0024	+0.0012	0000 0000 0001
ZERO	0.0000	0.0000	0000 0000 0000

	BIPOLAR		OFFSET BINARY*
	±10 V	±5V	
+FS-1 LSB	+9.9951	+4.9976	1111 1111 1111
+½FS	+5.0000	+2.5000	1100 0000 0000
+1 LSB	+0.0049	+0.0024	1000 0000 0001
ZERO	0.0000	0.0000	1000 0000 0000
−FS+1 LSB	−9.9951	−4.9976	0000 0000 0001
−FS	−10.000	−5.0000	0000 0000 0000

*For 2's complement - add inverter to MSB line.

TABLE 5 MUX CHANNEL ADDRESSING

← MUX ADDRESS →						
PIN						
9	10	11	12	5		
RA8	RA4	RA2	RA1	MUX ENAB.	ON CHANNEL	
X	X	X	X	0	NONE	
0	0	0	0	1	0	
0	0	0	1	1	1	
0	0	1	0	1	2	
0	0	1	1	1	3	
0	1	0	0	1	4	
0	1	0	1	1	5	
0	1	1	0	1	6	HDAS-8 (3 BIT ADDRESS)
0	1	1	1	1	7	
1	0	0	0	1	8	
1	0	0	1	1	9	
1	0	1	0	1	10	
1	0	1	1	1	11	
1	1	0	0	1	12	
1	1	0	1	1	13	
1	1	1	0	1	14	HDAS-16 (4 BIT ADDRESS)
1	1	1	1	1	15	

MULTIPLEXER ADDRESSING

Channel Selection

The HDAS is capable of two modes of addressing the multiplexer.

RANDOM ADDRESS

Set Pin 19 ($\overline{LOAD}$) to logic "0". The next falling edge of $\overline{STROBE}$ will load the MUX CHANNEL ADDRESS present on Pin 13 to Pin 16. Address inputs must be stable 50 nsec before and after falling edge of $\overline{STROBE}$ pulse.

FREE RUNNING SEQUENTIAL ADDRESS

Set Pin 19 ($\overline{LOAD}$) and Pin 20 ($\overline{CLEAR}$) to logic "1" or leave open. Connect Pin 7 ($\overline{EOC}$) to Pin 8 ($\overline{STROBE}$). The falling edge of $\overline{EOC}$ will increment channel address. This means that when the $\overline{EOC}$ is low, the digital output data is valid for the previous channel (CHn - 1) than that channel indicated on MUX ADDRESS OUTPUT. The HDAS will continually scan all 16 channels.

example

CH 4 has been addressed and a conversion takes place. The $\overline{EOC}$ goes low and that Channels data becomes valid but MUX ADDRESS CODE is now CH5.

TRIGGERED SEQUENTIAL ADDRESS

Set Pin 19 ($\overline{LOAD}$) and Pin 20 ($\overline{CLEAR}$) to logic "1" or leave open. Apply a falling edge trigger pulse to Pin 8 ($\overline{STROBE}$). This negative transition causes the contents of the address counter to be incremented by one followed by an A/D conversion in 9 μsec.

FIG. 2 HDAS TIMING DIAGRAM

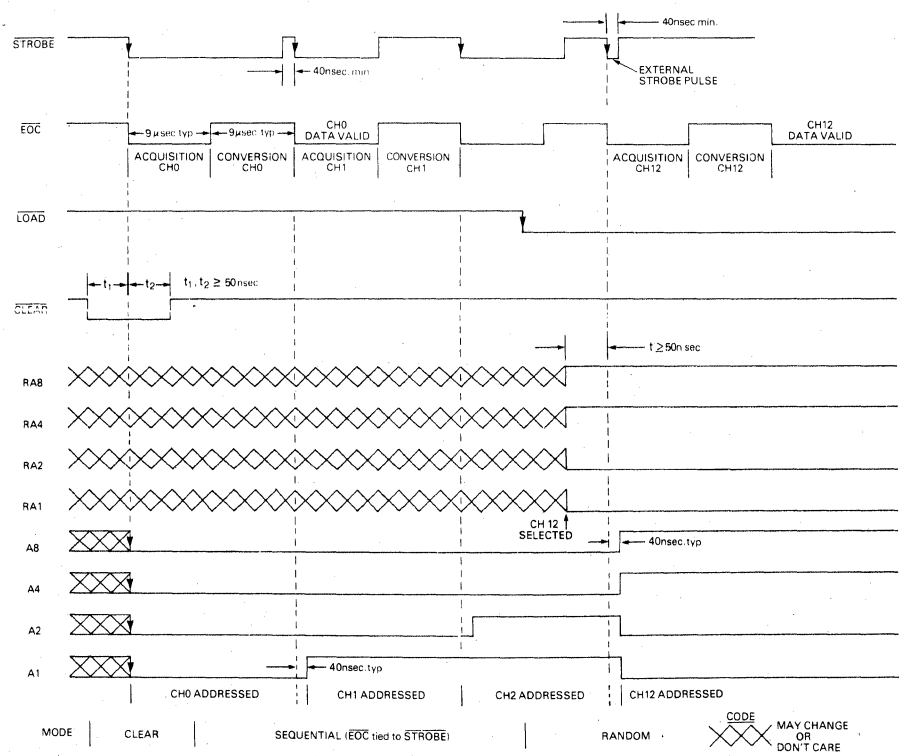
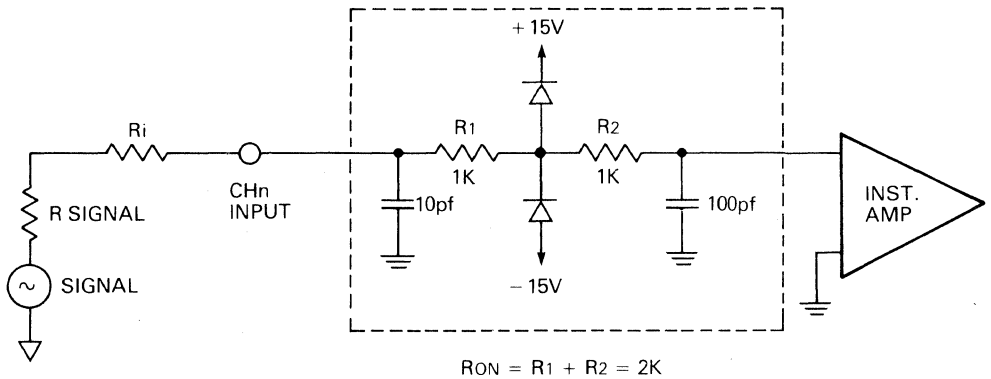


FIG. 3 MULTIPLEXER EQUIVALENT CIRCUIT



INPUT VOLTAGE PROTECTION

As shown in Fig. 3, the multiplexer has reversed biased diodes which protect the input channels from being damaged by overvoltage signals. The HDAS input channels are protected up to 20 V beyond the supplies and can be increased by adding series resistors (Ri) to each channel. This input resistor must limit the current flowing through the protection diodes to 10 mA.

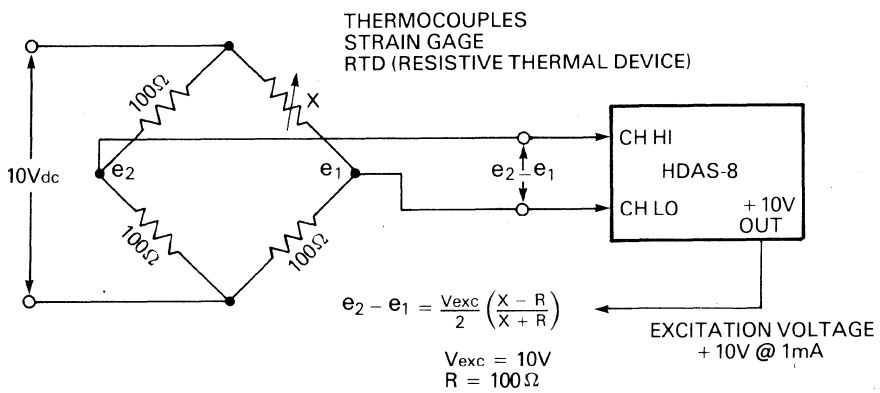
The value of Ri for a specific voltage protection range (Vp) can be calculated by the following formula:

$$Vp = (R\ signal + Ri + Ron)(10\ mA)$$

where Ron = 2K

NOTE: Increased input series resistance will increase multiplexer settling time.

FIG. 4 LOW LEVEL INPUTS



Remote monitoring of low level signals can be difficult, especially when analog signals pass through an environment with high levels of electrical noise. One solution is to use an instrumentation amplifier to extract the common mode voltage and amplify the voltage difference. The HDAS-8, an eight channel differential input system, can reject common-mode noise and allow amplification up to a gain of 1000. Direct connections to thermocouples, transducers, strain gages and RTD can be made through shielded twisted pairs. A differential RC filter may be used to attenuate normal mode noise.

FIG. 5 32 CHANNEL SINGLE ENDED DATA ACQUISITION SYSTEM

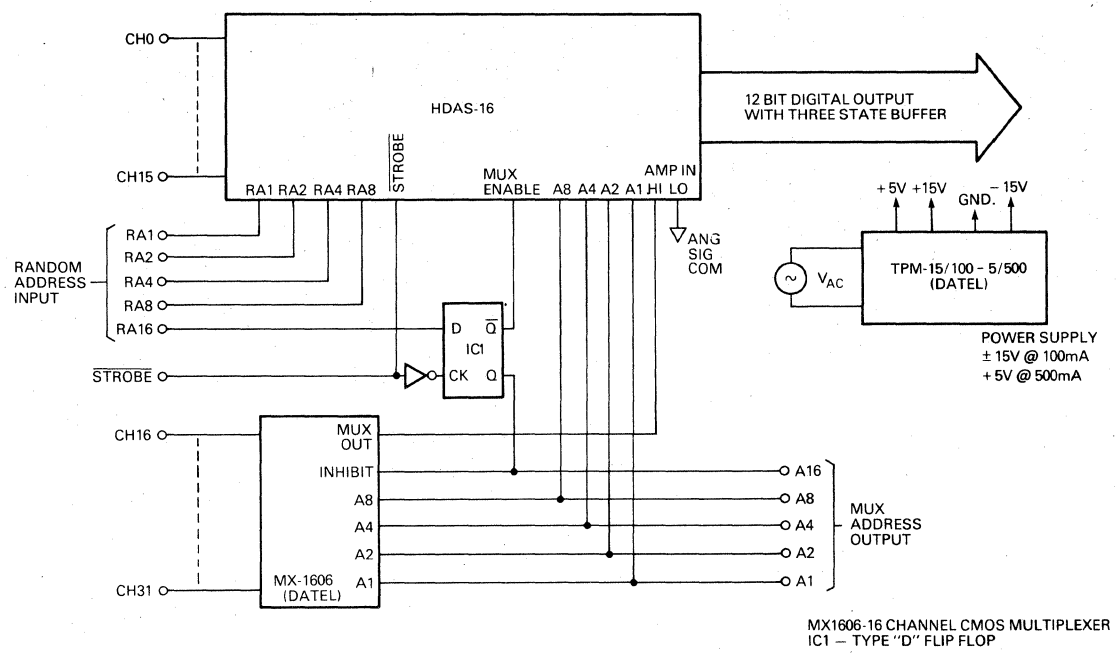
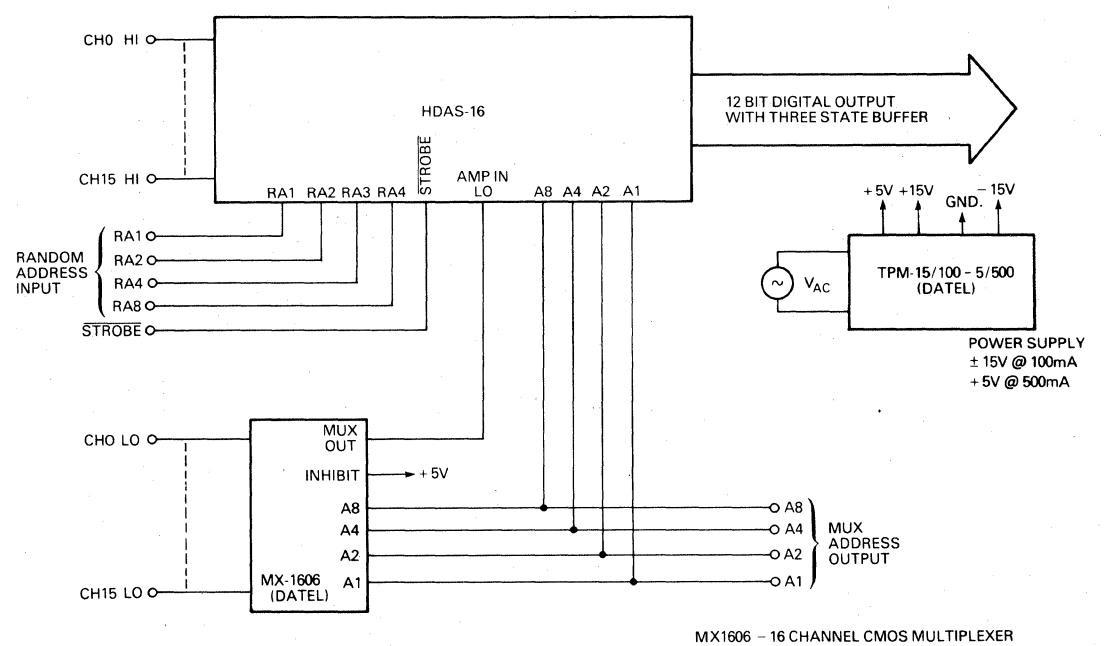


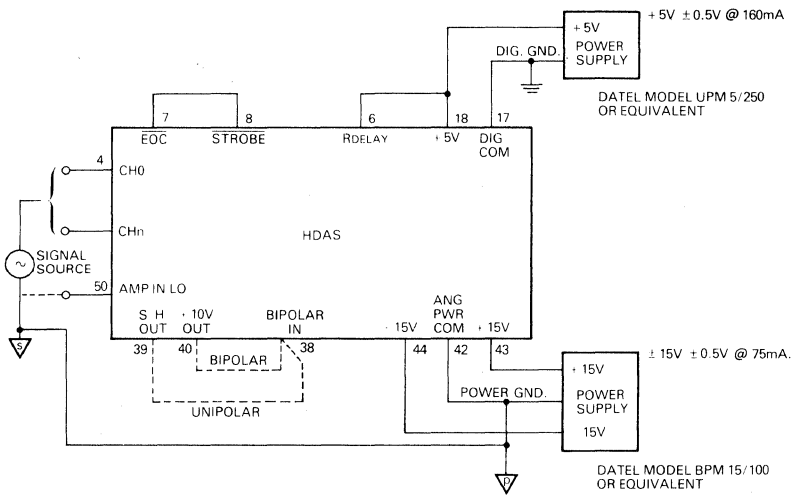
FIG. 6 16 CHANNEL DIFFERENTIAL DATA ACQUISITION SYSTEM



MULTIPLEXER EXPANSION

Fig. 5 shows the interconnection scheme for expanding the multiplexer channel capacity of the HDAS-16 from 16 channels single ended to 32 channels. Fig. 6 shows a similar scheme to expand the HDAS-16 to 16 differential channels.

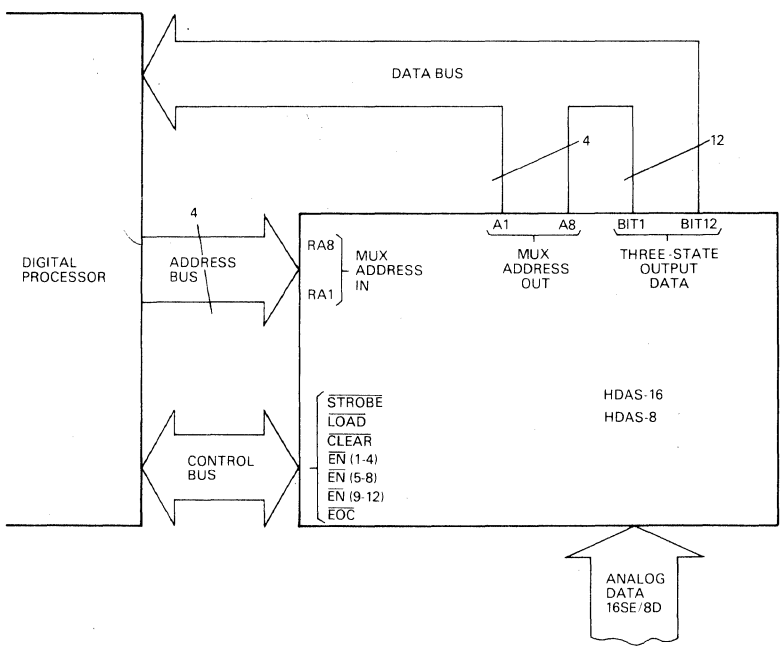
FIG. 7 SIMPLE CONNECTION DIAGRAM



NOTES:

1. For HDAS-16, tie PIN 50 to "signal source common" if possible. Otherwise tie PIN 50 to PIN 41 (ANG SIG COM)
2. BIPOLAR connection yields +10V range. UNIPOLAR connection yields 0 to ±10 V range. Other ranges are created by selecting appropriate value of Rg.
3. DIG COM, ANG PWR COM and ANG SIG COM are internally connected.

FIG. 8 PROCESSOR INTERFACE



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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Miniature Modular Data Acquisition System Models MDAS-16, MDAS-8D

FEATURES

- 16 Channels Single Ended or 8 Channels Differential
- 12 Bits Resolution
- 50 kHz Throughput Rate
- Three-State Outputs
- Low Cost
- Miniature Size

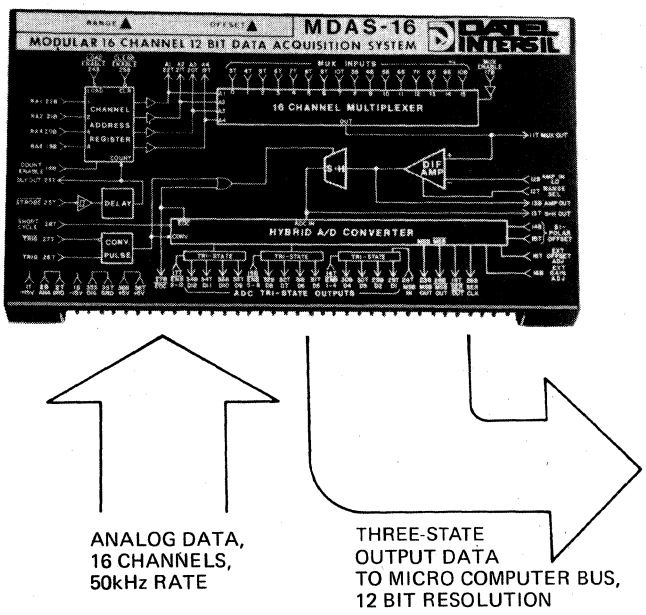
DESCRIPTION

The MDAS-16 and MDAS-8D data acquisition modules are complete, self-contained systems featuring 16 channel single ended or 8 channel differential operation respectively. Resolution is 12 bits and throughput rate is 50kHz. Output data is buffered three-state for interfacing to mini or micro-computer data buses. Output data can be transferred in three 4 bit bytes. Output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation.

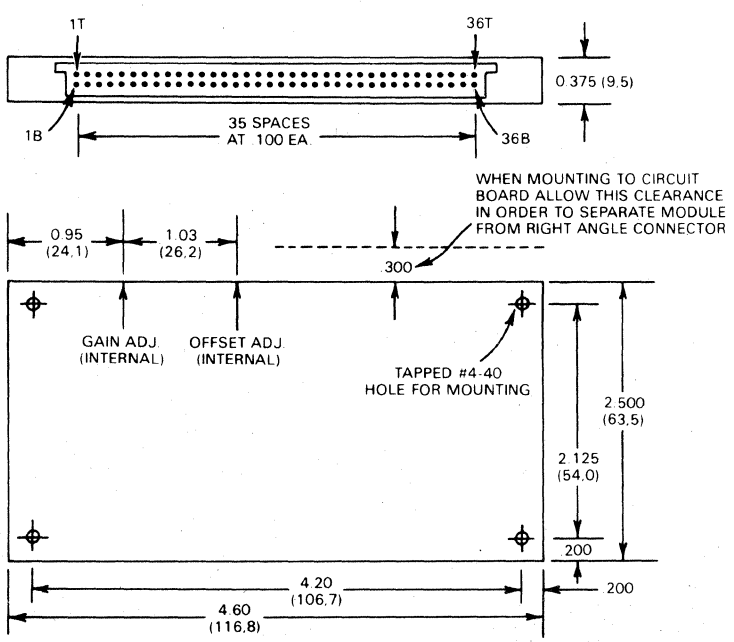
The 4.6 x 2.5 x 0.375 inch size of these modules is ½ inch narrower than other competitive models. The small size and low cost are made possible by extensive use of hybrid and monolithic circuits to reduce parts count and increase reliability. Both models use Datel-Intersil's new ADC-HZ12BGC 12 bit hybrid A/D converter along with a monolithic sample-hold and analog multiplexer.

The MDAS-16 and MDAS-8D feature a high degree of user flexibility with pin-programmable input ranges of 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V. The systems may be operated in either random or sequential channel addressing modes. For applications where lower than 12 bit resolution can be used, the A/D converter can be short-cycled to achieve a faster conversion rate. Output data is also available in serial form with a gated clock output.

The modules are housed in a shielded steel case. Input-output connections are made by means of a 72-pin connector. The number of channels may be expanded by 32 for the MDAS-16 or by 16 for the MDAS-8D by use of the multiplexer expander modules MDXP-32, and MDXP-32-1.



MECHANICAL DIMENSIONS - INCHES (MM)



DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, MDAS-16 & MDAS-8D
(Typical at 25°C, ±15V and +5V supplies unless otherwise indicated)

ANALOG INPUTS

Number of Channels	16 Single Ended (MDAS-16) 8 Differential (MDAS-8D)
Input Voltage Ranges	
unipolar	0 to +5V 0 to +10V
bipolar	±2.5V, ±5V, ±10V
Common Mode Range, min.	±10V
Max. Input Voltage, no damage	±15V
Input Impedance	100 megohms
Input Bias Current	3nA, 10nA max. 0 to 70°C
Input Capacitance	
OFF channel	10 pF
ON channel	100pF

ACCURACY

Resolution	12 Bits
Error, max. 50kHz sampling	±.025% of FSR
Nonlinearity, max.	±½ LSB
Diff. Nonlinearity, max.	±½ LSB
Gain Error	Adj. to zero
Offset Error	Adj. to zero
Temp. Coeff. of Gain, max.	±30ppm/°C
Temp. Coeff. of Offset, max.	±7ppm/°C of FS
Diff. Linearity Tempco, max.	±3ppm/°C of FS
Common Mode Rejec., min.	70 dB at 1 kHz
Monotonicity	0°C to 70°C
Power Supply Rejection	.01%/% Supply

DYNAMIC CHARACTERISTICS

Throughput Rate, max.	50 kHz
Acquisition Time	6 µsec.
Conversion Time	14 µsec.
Aperture Time, max.	100 nsec.
Sample-Hold Droop, max.	200 µV/msec.
Feedthrough, max.	.01%
Channel Crosstalk (Mux.)	-80 dB at 1 kHz

DIGITAL OUTPUTS

Parallel Data Out	12 parallel lines of buffered three-state output data. Drives 12 TTL loads.
Coding	Straight binary, offset binary, and two's complement
Serial Out	Output data in MSB first, NRZ format. Straight binary and offset binary coding. Drives 5 TTL loads
Mux Address Out	Buffered output of address register Drives 20 TTL loads
Delay Out	Drives 5 TTL loads
Clock Out	Drives 5 TTL loads
$\overline{\text{EOC}}$ (Status)	Drives 4 TTL loads
MSB Out	Drives 5 TTL loads
$\overline{\text{MSB}}$ Out	Drives 5 TTL loads

DIGITAL INPUTS

$\overline{\text{Enable}}$	Three separate inputs which enable three-state outputs in 4 bit bytes. 1 TTL load
Mux Address In	3 bit (MDAS-8D) or 4 bit (MDAS-16) binary address 1 LS TTL load
$\overline{\text{Strobe}}$	1 LS TTL load with 10K pull-up resistor
A/D Trigger	1 LS TTL load with 10K pull-up resistor
A/D $\overline{\text{Trigger}}$	1 LS TTL Load
Mux Enable	1 TTL load with 10K pull-up resistor
Count Enable	1 LS TTL load with 10K pull-up resistor
$\overline{\text{Load Enable}}$	1 LS TTL load with 10K pull-up resistor
$\overline{\text{Clear Enable}}$	1 LS TTL load with 10K pull-up resistor
MSB In	1 TTL load
Short Cycle	1 TTL load with 10K pull-up resistor

POWER REQUIREMENT

+15VDC ±0.5V @ 65mA
-15VDC ±0.5V @ 60 mA
+5VDC ±0.25V @ 200mA

PHYSICAL ENVIRONMENTAL

Operating Temp. Range	0°C to 70°C
Storage Temperature Range	-25°C to +85°C
Package Size	4.6 x 2.5 x 0.375 inches (116.8 x 63.5 x 9.5 mm)
Package Type	Steel, shielded on 5 sides
Weight	6 oz. (170 g)

NOTES: 1. All outputs are Vout ("0") ≤+0.4V, Vout ("1") ≥+2.4V
2. All inputs are Vin ("0") ≤+0.8V, Vin ("1") ≥+2.0V

ORDERING INFORMATION

MDAS-16 .....
MDAS-8D .....

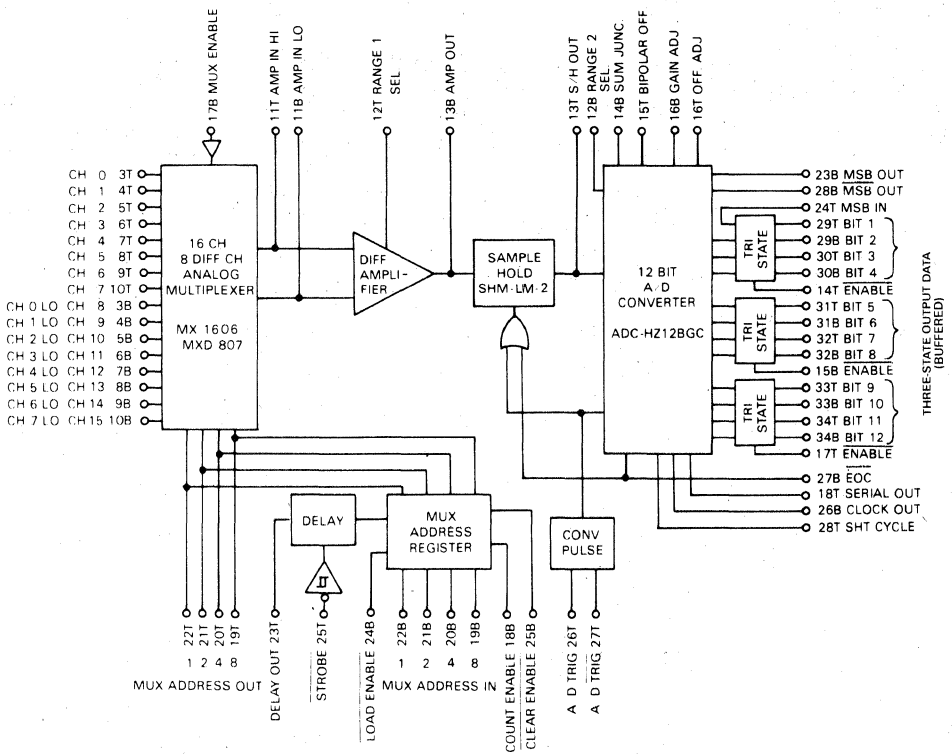
These modules are also available in extended temperature range versions designated with the suffix EX (-25°C to +85°C) or EXX-HS (-55°C to 85°C) with hermetically sealed semiconductor components. Contact factory for price and delivery.

Included with each module is a mating right-angle 72 pin connector. (AMP 3-86063-2). Additional connectors may also be ordered by the following number: 58-2083010 Connector

Trimming Potentiometers:

Multiplexer expander modules are also available.
The MDXP-32 adds 32 single ended or 16 differential channels with control logic.
The MDXP-32-1 is identical but without control logic.

BLOCK DIAGRAM MDAS-16, MDAS-8D



PIN CONNECTIONS for MDAS-16

	Top	Bottom	
+15VDC	1T	1B	-15VDC
Analog Gnd.	2T	2B	Analog Gnd.
Ch. 0 In	3T	3B	Ch. 8 In
Ch. 1 In	4T	4B	Ch. 9 In
Ch. 2 In	5T	5B	Ch. 10 In
Ch. 3 In	6T	6B	Ch. 11 In
Ch. 4 In	7T	7B	Ch. 12 In
Ch. 5 In	8T	8B	Ch. 13 In
Ch. 6 In	9T	9B	Ch. 14 In
Ch. 7 In	10T	10B	Ch. 15 In
Amplifier In Hi	11T	11B	Amplifier In Lo
Range 1 Select	12T	12B	Range 2 Select
Sample Hold Out	13T	13B	Amplifier Out
Enable (Bits 1-4 Out)	14T	14B	Sum Junc.(Bipolar Off.)
Bipolar Offset	15T	15B	Enable (Bits 5-8 Out)
Ext. Offset Adjust	16T	16B	Ext. Gain Adjust
Enable (Bits 9-12)	17T	17B	Mux Enable
Serial Out	18T	18B	Count Enable
8 Out (Mux Address Lines)	19T	19B	8 In (Mux Address Lines)
4 Out (Mux Address Lines)	20T	20B	4 In (Mux Address Lines)
2 Out (Mux Address Lines)	21T	21B	2 In (Mux Address Lines)
1 Out (Mux Address Lines)	22T	22B	1 In (Mux Address Lines)
Delay Out	23T	23B	MSB Out (TTL)
MSB In (TTL)	24T	24B	Load Enable
Strobe	25T	25B	Clear Enable
A/D Trigger	26T	26B	Clock Out
A/D Trigger	27T	27B	EOC (status)
Short Cycle	28T	28B	MSB Out (TTL)
Bit 1 Out* (MSB)	29T	29B	Bit 2 Out*
Bit 3 Out*	30T	30B	Bit 4 Out*
Bit 5 Out*	31T	31B	Bit 6 Out*
Bit 7 Out*	32T	32B	Bit 8 Out*
Bit 9 Out*	33T	33B	Bit 10 Out*
Bit 11 Out*	34T	34B	Bit 12 Out* (LSB)
Digital Gnd.	35T	35B	Digital Gnd.
+5VDC	36T	36B	+5VDC

*Three-State Outputs

PIN CONNECTIONS for MDAS-8D

	Top	Bottom	
+15VDC	1T	1B	-15VDC
Analog Gnd.	2T	2B	Analog Gnd.
Ch. 0 Hi In	3T	3B	Ch. 0 Lo In
Ch. 1 Hi In	4T	4B	Ch. 1 Lo In
Ch. 2 Hi In	5T	5B	Ch. 2 Lo In
Ch. 3 Hi In	6T	6B	Ch. 3 Lo In
Ch. 4 Hi In	7T	7B	Ch. 4 Lo In
Ch. 5 Hi In	8T	8B	Ch. 5 Lo In
Ch. 6 Hi In	9T	9B	Ch. 6 Lo In
Ch. 7 Hi In	10T	10B	Ch. 7 Lo In
Amplifier In Hi	11T	11B	Amplifier In Lo
Range 1 Select	12T	12B	Range 2 Select
Sample Hold Out	13T	13B	Amplifier Out
Enable (Bits 1-4 Out)	14T	14B	Sum Junc.(Bipolar Off!)
Bipolar Offset	15T	15B	Enable (Bits 5-8 Out)
Ext. Offset Adjust	16T	16B	Ext. Gain Adjust
Enable (Bits 9-12 Out)	17T	17B	Mux Enable
Serial Out	18T	18B	Count Enable
8 Out (Mux Address Lines)	19T	19B	8 In (Mux Address Lines)
4 Out (Mux Address Lines)	20T	20B	4 In (Mux Address Lines)
2 Out (Mux Address Lines)	21T	21B	2 In (Mux Address Lines)
1 Out (Mux Address Lines)	22T	22B	1In (Mux Address Lines)
Delay Out	23T	23B	MSB Out (TTL)
MSB In (TTL)	24T	24B	Load Enable
Strobe	25T	25B	Clear Enable
A/D Trigger	26T	26B	Clock Out
A/D Trigger	27T	27B	EOC (status)
Short Cycle	28T	28B	MSB Out (TTL)
Bit 1 Out* (MSB)	29T	29B	Bit 2 Out*
Bit 3 Out*	30T	30B	Bit 4 Out*
Bit 5 Out*	31T	31B	Bit 6 Out*
Bit 7 Out*	32T	32B	Bit 8 Out*
Bit 9 Out*	33T	33B	Bit 10 Out*
Bit 11 Out*	34T	34B	Bit 12 Out* (LSB)
Digital Gnd.	35T	35B	Digital Gnd.
+5VDC	36T	36B	+5VDC

*Three-State Outputs

TABLE I DESCRIPTION OF CONTROL PIN FUNCTIONS

FUNCTION	PIN	DESCRIPTION
Amplifier In Lo	11B	Analog monitoring point for MDAS-8D. For the MDAS-16 this pin must be grounded.
Amplifier In Hi	11T	Analog monitoring point.
Range 2 Select Range 1 Select	12B 12T	These pins program analog input voltage range. See Table II
Amplifier Out	13B	Analog monitoring point.
Sample Hold Out	13T	Analog monitoring point.
Summing Junction	14B	Used to program analog input voltage range and bipolar offset. See Table II
$\overline{\text{Enable}}$	14T	Input LO enables tri-state outputs for bits 1-4. Input HI inhibits outputs.
$\overline{\text{Enable}}$	15B	Input LO enables tri-state outputs for bits 5-8. Input HI inhibits outputs.
Bipolar Offset	15T	Connects to 14B for bipolar operation and to analog ground for unipolar operation. See Table II
Ext. Gain Adjust	16B	Used to adjust out gain error. Operates independently of the internal adjustment. See External Adjustments diagram.
Ext. Offset Adjust	16T	Used to adjust out offset error. Operates independently of the internal adjustment. See External Adjustments diagram.
Mux Enable	17B	Input HI enables analog multiplexer. Input LO inhibits analog multiplexer.
$\overline{\text{Enable}}$	17T	Input LO enables three-state outputs for bits 9-12. Input HI inhibits outputs.
Count Enable	18B	Input HI enables Mux Address Register. Input LO inhibits Mux address Register.
Mux Address In	19B, 20B, 21B, 22B	Digital inputs for channel address selection in random addressing mode. Straight binary coding. See Table III
Mux Address Out	19T, 20T, 21T, 22T	Straight binary coded output of Mux Address Register.
MSB Out	23B	Bit 1 TTL output of A/D converter. Connect to pin 24T for straight binary or offset binary output coding.
Delay Output	23T	An output delay pulse for 6μsec. to allow for multiplexer and amplifier settling time and sample hold acquisition time. This pin is normally connected to A/D $\overline{\text{Trigger}}$ (pin 27T) to initiate A/D conversion.
$\overline{\text{Load Enable}}$	24B	Input HI for sequential addressing. Input LO for random addressing.
MSB In	24T	Bit 1 input to three-state output buffers. Connect to either pin 23B (MSB Out) or pin 28B ($\overline{\text{MSB}}$ Out).
$\overline{\text{Clear Enable}}$	25B	Input LO and a negative transition on pin 25T resets Mux address counter to zero.
$\overline{\text{Strobe}}$	25T	Negative input transition initiates channel scanning sequence in sequential mode or a conversion in the random mode. A Schmidt trigger input adds hysteresis for good noise rejection.
Clock Output	26B	A/D converter clock pulses for synchronization of serial data. Negative going pulses of approximately 100 nsec. duration.
A/D Trigger	26T	A positive logic transition on this input initiates A/D conversion.
$\overline{\text{EOC}}$ (status)	27B	End of conversion (status) output. Output HI during conversion and LO when conversion is complete.
A/D $\overline{\text{Trigger}}$	27T	A negative logic transition on this input initiates A/D conversion. This pin is normally connected to pin 23T (Delay Output).
$\overline{\text{MSB}}$ Out	28B	Complemented bit 1 TTL output of A/D converter. Connect to pin 24T for two's complement output coding.
Short Cycle	28T	For 12 bit resolution connect this pin to ground. To short cycle A/D converter for lower resolution, connect this pin to output bit n + 1 for a resolution of n bits. Short cycling of the A/D converter can only be done with the $\overline{\text{Enable}}$ inputs (pins 14T, 15B and 17T) LO.

TABLE II INPUT RANGE SELECTION

INPUT RANGE	CONNECT THESE PINS TOGETHER		
	RANGE 1 PIN 12T	RANGE 2 PIN 12B	BIPOLAR OFF. PIN 15T
0 TO +5V	13B	13T	2B OR 2T
0 TO +10V	2B OR 2T	13T	2B OR 2T
±2.5V	13B	13T	14B
± 5V	2B OR 2T	13T	14B
±10V	2B OR 2T	OPEN	14B

TABLE IV
THROUGHPUT RATES VS. NO. BITS FOR SHORT-CYCLED A/D CONVERTER

NO. BITS	THROUGHPUT RATE
12	50 kHz
10	53 kHz
8	57 kHz
4	67 kHz

TABLE III MUX CHANNEL ADDRESSING

← MUX ADDRESS → PIN					ON CHANNEL	
19B	20B	21B	22B	17B		
8	4	2	1	MUX ENAB.		
X	X	X	X	0	NONE	
0	0	0	0	1	0	
0	0	0	1	1	1	
0	0	1	0	1	2	
0	0	1	1	1	3	
0	1	0	0	1	4	
0	1	0	1	1	5	
0	1	1	0	1	6	MDAS-8D (3 BIT ADDRESS)
0	1	1	1	1	7	
1	0	0	0	1	8	
1	0	0	1	1	9	
1	0	1	0	1	10	
1	0	1	1	1	11	
1	1	0	0	1	12	
1	1	0	1	1	13	
1	1	1	0	1	14	MDAS-16 (4 BIT ADDRESS)
1	1	1	1	1	15	

TABLE V

CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 TO +5V	ZERO GAIN	+0.6 mV +4.9982V
0 TO +10V	ZERO GAIN	+1.2 mV +9.9963V
BIPOLAR RANGE		
±2.5V	OFFSET GAIN	-2.4994V +2.4982V
±5V	OFFSET GAIN	-4.9988V +4.9963V
±10V	OFFSET GAIN	-9.9976V +9.9927V

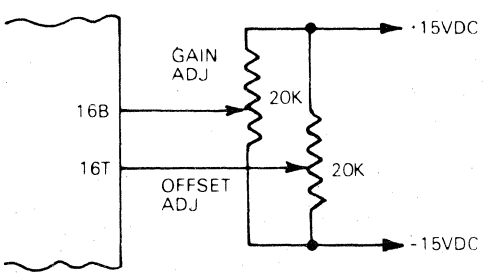


FIG. 1 EXTERNAL ADJUSTMENTS

SET-UP AND CALIBRATION INSTRUCTIONS

1. Select input voltage range desired and connect pins 12B, 12T, and 15T in accordance with Table II. If the MDAS-16 is used, ground pin 11B. Ground all analog channel inputs which are not to be used. Leave pin 17B open.
2. Determine resolution to be used. For full 12 bits, ground pin 28T. For lower resolution requirements, connect pin 28T to bit output n + 1 for n bit resolution. For example: for 8 bit resolution connect pin 28T to pin 33T (Bit 9 Out). To operate the A/D converter in this short cycled mode, the $\overline{\text{Enable}}$ inputs (pins 14T, 15B, and 17T) must be connected to ground thereby enabling the three-state outputs. For 12 bit resolution the three-state outputs can be either enabled or disabled.
3. Select the output coding desired. For straight binary (unipolar) or offset binary (bipolar) connect pin 23B (MSB Out) to pin 24T (MSB In). For two's complement (bipolar) connect pin 28B ($\overline{\text{MSB}}$ Out) to pin 24T.
4. Select desired multiplexer mode. Connect pin 23T (Delay Out) to pin 27T (A/D $\overline{\text{Trigger}}$).

   A. **Free Running Sequential Addressing**

   Connect pin 27B ($\overline{\text{EOC}}$) to pin 25T ($\overline{\text{Strobe}}$). Leave pins 24B ($\overline{\text{Load Enable}}$) and 25B ($\overline{\text{Clear Enable}}$) open. Sequencing is initiated by a positive logic transition applied to pin 26T (A/D Trigger). Pin 26T must remain HI during free running sequential addressing. Sequencing is stopped by a LO applied to pin 26T.

   B. **Triggered Sequential Addressing**

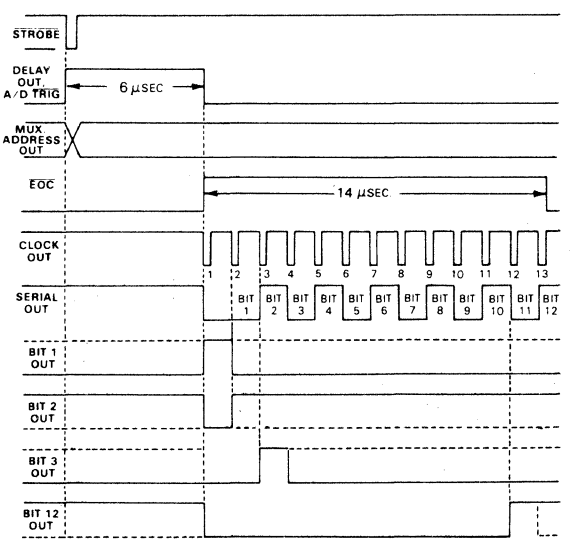
   Leave pins 24B ($\overline{\text{Load Enable}}$) and 25B ($\overline{\text{Clear Enable}}$) open. Apply a falling edge trigger to pin 25T ($\overline{\text{Strobe}}$). The negative transition of the strobe will cause the contents of the address counter to be incremented by one.

   C. **Random Addressing**

   Ground pin 24B ($\overline{\text{Load Enable}}$). Leave pin 25B ($\overline{\text{Clear Enable}}$) open. Each negative transition applied to pin 25T ($\overline{\text{Strobe}}$) will cause the data at pins 19B, 20B, 21B and 22B (Mux Address In) to be loaded into the Address Register. Address inputs must be stable for at least 300 nsec. after negative transition of $\overline{\text{Strobe}}$.

5. Calibration Procedure
   A. Offset and gain adjustments may be made either internally or externally. Self-contained trimming potentiometers are provided for the internal adjustments. For external adjustment, 20K trimming potentiometers must be used with pins 16B and 16T. Connect as shown in Figure 1.
   B. Connect power supplies to the module and a precision voltage source to pin 3T (Chan 0 In). If the MDAS-8D is used, connect pin 3B (Chan 0 LO) to analog ground. Ground pin 25B ($\overline{\text{Clear Enable}}$) and momentarily short pin 25T ($\overline{\text{Strobe}}$) to ground. Use an oscilloscope to monitor the serial output code at pin 18T. Trigger the A/D converter with 50kHz positive going pulses applied to pin 26T (A/D Trigger).
   C. Adjust the precision voltage source to the value shown in the Calibration Table for the unipolar zero adjustment (zero + ½ LSB) or the bipolar offset adjustment (-FS + ½ LSB). Adjust the offset trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.
   D. Change the output of the precision voltage source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+FS - 1½ LSB). Adjust the gain trimming potentiometer so that the output flickers equally between 1111 1111 1110 and 1111 1111 1111.

MDAS-16, MDAS-8D TIMING DIAGRAM Output Code: 010101010101



DATEL INTERSIL
11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617)339-9341 / TWX 710-346-1953 / TLX 951340
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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

Data Acquisition Expander Modules
Models MDXP-32, MDXP-32-1

FEATURES

- **Compatible with MDAS-16 or MDAS-8D**
- **32 Single Ended Channels**
- **16 Differential Channels**
- **Expansion to 256 Channels**
- **Miniature Module**
- **Low Cost**

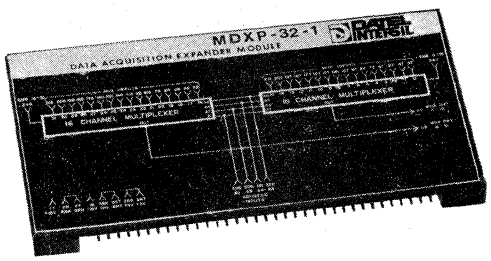
GENERAL DESCRIPTION

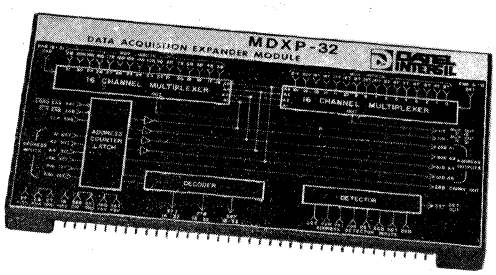
The MDXP-32 and MDXP-32-1 are companion devices to Datel Systems' MDAS-16 and MDAS-8D Miniature Modular Data Acquisition Systems. They can also be used with data acquisition systems from other manufacturers. Both models contain 32 analog multiplex channels which permit expanding the MDAS-16 up to 48 single ended channels and the MDAS-8D up to 24 differential channels using single level multiplexing. With double level multiplexing up to 256 single ended channels or 128 differential channels can be realized using 1 MDXP-32 and 7 MDXP-32-1's with an MDAS-16 or MDAS-8D.

The MDXP-32 contains an address counter, address decoder, address detector logic, and two 16 channel analog multiplexers. The MDXP-32-1 contains two 16 channel analog multiplexers and an address decoder. The expanded systems can be operated in three modes: free running sequential addressing, triggered sequential addressing, or random addressing. In sequential operation the system can be short cycled to any number of desired channels less than the maximum by use of the address detector in the MDXP-32. The MDXP-32-1 can be used to expand the MDAS-16 or MDAS-8D for random addressing operation only.

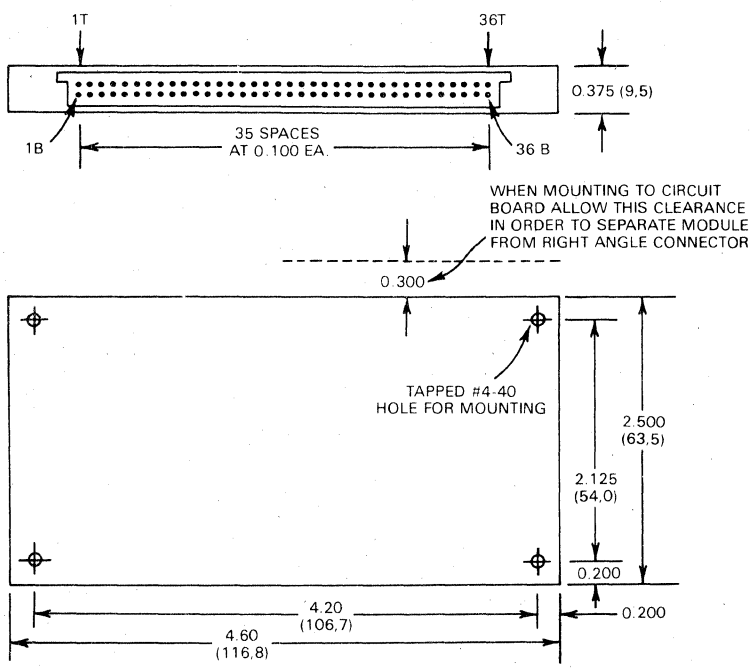
The analog multiplexers in these units are dielectrically isolated CMOS with fully protected inputs. The ON resistance of each channel is typically 1.5K ohms. Transfer accuracies better than 0.01% are achieved if a very high impedance load such as a unity gain buffer amplifier input is used. The channels switch with a break-before-make delay of 80 nsec.

Both the MDXP-32 and MDXP-32-1 are contained in a 4.6 x 2.5 x 0.375 inch (116,8 x 63,5 x 9,5 mm) shielded steel case. Operating temperature range is 0°C to 70°C.





MECHANICAL DIMENSIONS - INCHES (MM)



DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, MDXP-32 & MDXP-32-1
(Typical at 25°C, ±15V and +5V supplies unless otherwise noted)

MAXIMUM RATINGS

Positive Supply Voltage, pin 1T ... +20V
Negative Supply Voltage, pin 1B .. −20V
Logic Supply Voltage, pins 36T & 36B ..... +5.5V
Digital Input Voltages ..... +5.5V
Analog Input Voltages ..... +Supply +20V
−Supply −20V

ANALOG INPUTS

Number of Channels, single ended 32
Number of Channels, differential . 16
Input Voltage Range ..... ±15V
Channel ON Resistance 1.5K
Channel ON Resistance, max. 0°C to 70°C 2.0K
Channel OFF Input Leakage 30pA
Channel ON Input Leakage 100pA

DIGITAL INPUTS

Input Logic Level[1], HI ("1") ..... +2.0V to +5.5V
Input Logic Level[1], LO ("0") ..... 0V to +0.8V
Logic Loading[1] ..... 1 LS TTL load
Address Coding ..... 4 bits (MDXP-32-1)
6 bits (MDXP-32)
Mux Enable Inputs[2], enable ..... HI (+4.0V to +Supply)
disable ..... LO (0 to +0.8V)

DIGITAL OUTPUTS

Output Logic Level, HI ("1") ..... +2.4V Min.
Output Logic Level, LO ("0") ..... +0.4V Max.
Output Drive Capability ..... 10 LS TTL loads

PERFORMANCE

Transfer Error, max.[3] 0.01%
Channel Crosstalk, 1 kHz ..... −80 dB
Turn ON Time ..... 500 nsec.
Turn OFF Time ..... 300 nsec.
Break-Before-Make Delay ..... 80 nsec.
Inhibit/Enable Delay ..... 300 nsec.

POWER REQUIREMENT ..... +15VDC ±0.5V @ 10mA
−15VDC ±0.5V @ 4mA
+5VDC ±0.25V @ 100mA[4]

PHYSICAL-ENVIRONMENTAL

Operating Temperature Range ... 0°C to 70°C
Storage Temperature Range ..... −25°C to +85°C
Package Size ..... 4.6 x 2.5 x 0.375 inches
116,8 x 63,5 x 9,5 mm
Package Type ..... Steel, shielded on 5 sides
Weight ..... 6 oz. (170 g.)

NOTES:

1. All digital inputs except for Mux Enable Inputs on both models and Address Inputs on MDXP-32-1.
2. The logic levels are also the same for the Address Inputs on MDXP-32-1.
3. For zero source impedance and ⩾ 20 megohm load impedance.
4. MDXP-32 only. The MDXP-32-1 does not use +5V power.

ORDERING INFORMATION

MDXP-32 .....
MDXP-32-1 .....

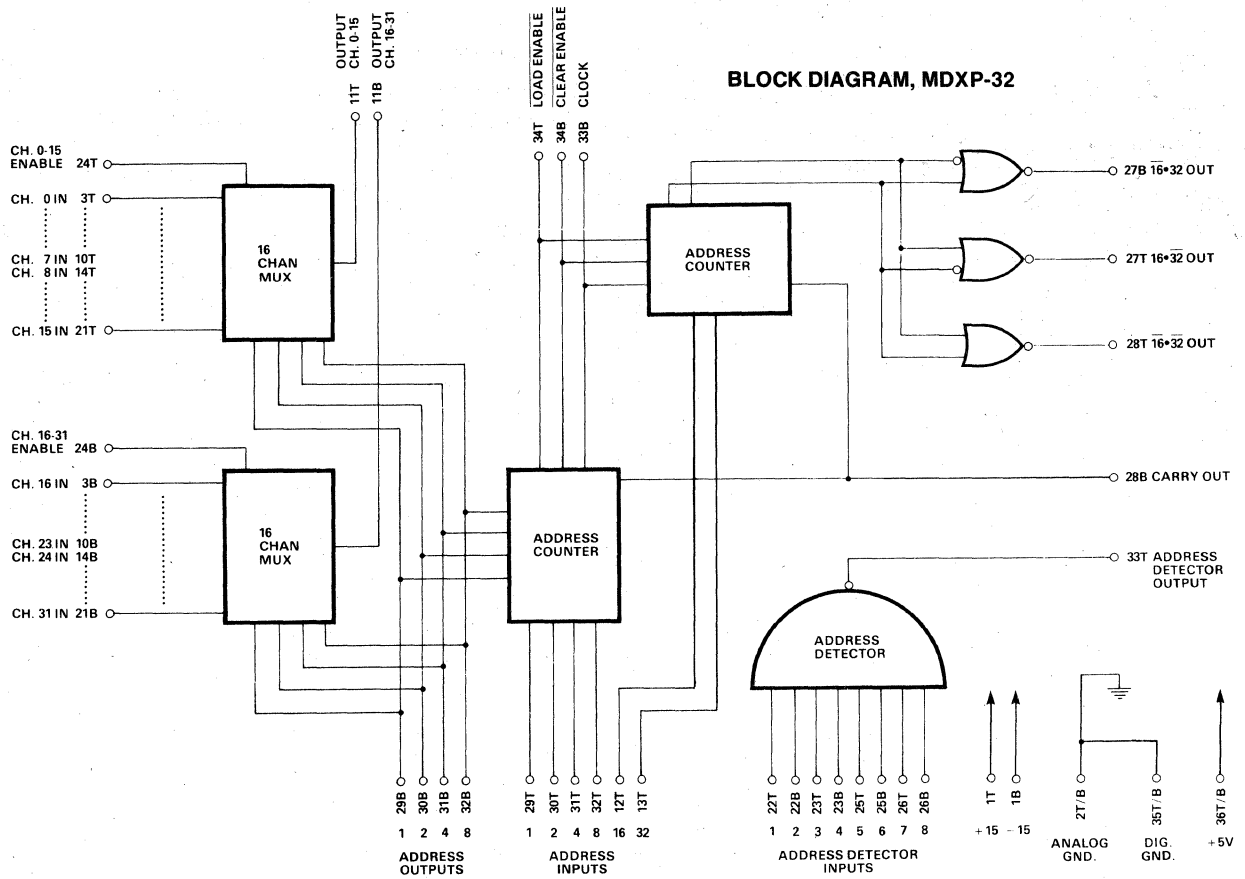
Included with each module is a mating right-angle 72-pin connector. Additional connectors may also be ordered by the following number.

58-2083010 Connector

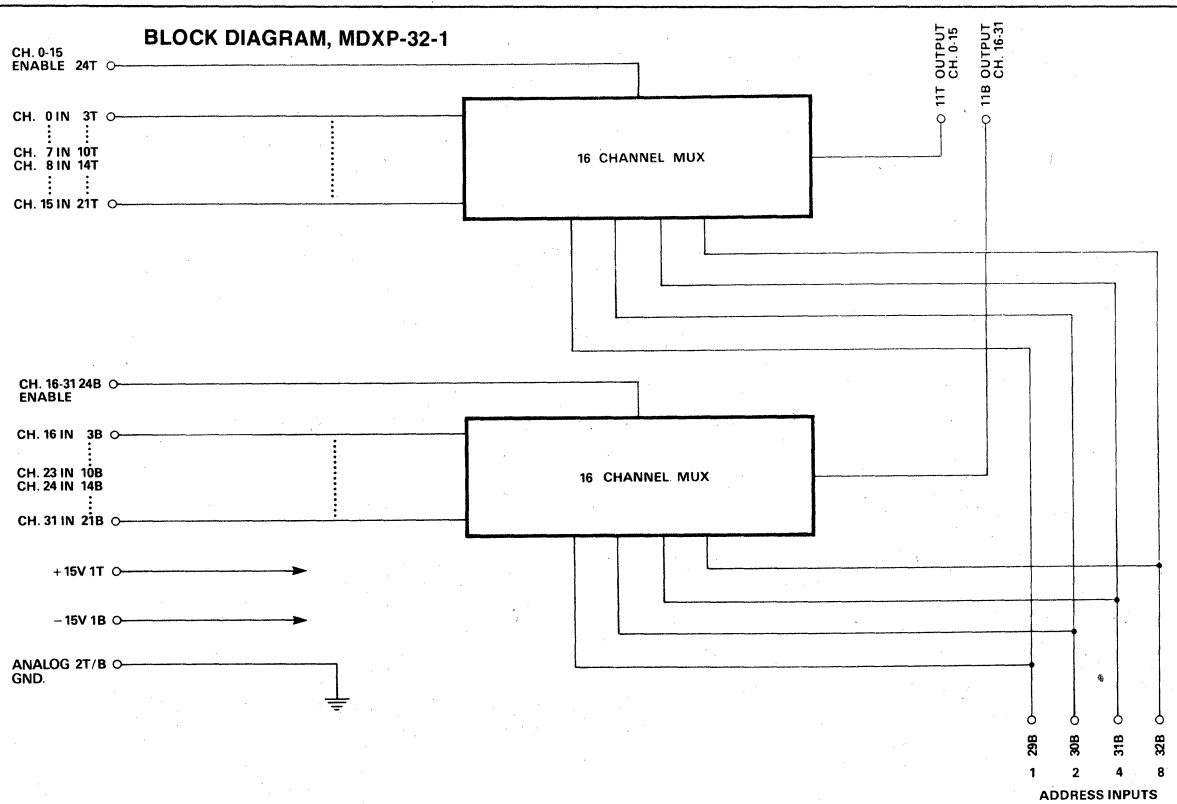
THE MDXP-32 AND MDXP-32-1 ARE COVERED BY GSA CONTRACT

BLOCK DIAGRAMS

BLOCK DIAGRAM, MDXP-32



BLOCK DIAGRAM, MDXP-32-1



INPUT/OUTPUT CONNECTIONS

PIN CONNECTIONS for MDXP-32

	Top	Bottom	
+15VDC	1T	1B	−15VDC
Analog Gnd.	2T	2B	Analog Gnd.
Ch. 0 In	3T	3B	Ch. 16 In
Ch. 1 In	4T	4B	Ch. 17 In
Ch. 2 In	5T	5B	Ch. 18 In
Ch. 3 In	6T	6B	Ch. 19 In
Ch. 4 In	7T	7B	Ch. 20 In
Ch. 5 In	8T	8B	Ch. 21 In
Ch. 6 In	9T	9B	Ch. 22 In
Ch. 7 In	10T	10B	Ch. 23 In
Output, Ch. 0-15	11T	11B	Output, Ch. 16-31
16 In } Address	12T	12B	NC
32 In } Inputs	13T	13B	NC
Ch. 8 In	14T	14B	Ch. 24 In
Ch. 9 In	15T	15B	Ch. 25 In
Ch. 10 In	16T	16B	Ch. 26 In
Ch. 11 In	17T	17B	Ch. 27 In
Ch. 12 In	18T	18B	Ch. 28 In
Ch. 13 In	19T	19B	Ch. 29 In
Ch. 14 In	20T	20B	Ch. 30 In
Ch. 15 In	21T	21B	Ch. 31 In
Addr. Det. In 1	22T	22B	Addr. Det. In 2
Addr. Det. In 3	23T	23B	Addr. Det. In 4
Enable Ch. 0-15	24T	24B	Enable Ch. 16-31
Addr. Det. In 5	25T	25B	Addr. Det. In 6
Addr. Det. In 7	26T	26B	Addr. Det. In 8
$\overline{16}\cdot\overline{32}$ Out	27T	27B	$\overline{16}\cdot 32$ Out
$\overline{16}\cdot\overline{32}$ Out	28T	28B	Carry Out
1 In } Address	29T	29B	1 Out } Address
2 In } Inputs	30T	30B	2 Out } Outputs
4 In } Inputs	31T	31B	4 Out } Outputs
8 In } Address	32T	32B	8 Out } Address
Address Det. Out	33T	33B	Clock
Load Enable	34T	34B	Clear Enable
Digital Gnd.	35T	35B	Digital Gnd.
+5VDC	36T	36B	+5VDC

PIN CONNECTIONS for MDXP-32-1

	Top	Bottom	
+15VDC	1T	1B	−15VDC
Analog Gnd.	2T	2B	Analog Gnd.
Ch. 0 In	3T	3B	Ch. 16 In
Ch. 1 In	4T	4B	Ch. 17 In
Ch. 2 In	5T	5B	Ch. 18 In
Ch. 3 In	6T	6B	Ch. 19 In
Ch. 4 In	7T	7B	Ch. 20 In
Ch. 5 In	8T	8B	Ch. 21 In
Ch. 6 In	9T	9B	Ch. 22 In
Ch. 7 In	10T	10B	Ch. 23 In
Output, Ch. 0-15	11T	11B	Output, Ch. 16-31
NC	12T	12B	NC
NC	13T	13B	NC
Ch. 8 In	14T	14B	Ch. 24 In
Ch. 9 In	15T	15B	Ch. 25 In
Ch. 10 In	16T	16B	Ch. 26 In
Ch. 11 In	17T	17B	Ch. 27 In
Ch. 12 In	18T	18B	Ch. 28 In
Ch. 13 In	19T	19B	Ch. 29 In
Ch. 14 In	20T	20B	Ch. 30 In
Ch. 15 In	21T	21B	Ch. 31 In
NC	22T	22B	NC
NC	23T	23B	NC
Enable Ch. 0-15	24T	24B	Enable Ch. 16-31
NC	25T	25B	NC
NC	26T	26B	NC
NC	27T	27B	NC
NC	28T	28B	NC
NC	29T	29B	1 In } Address
NC	30T	30B	2 In } Inputs
NC	31T	31B	4 In } Inputs
NC	32T	32B	8 In } Address
NC	33T	33B	NC
NC	34T	34B	NC
NC	35T	35B	NC
NC	36T	36B	NC

DESCRIPTION OF CONTROL PIN FUNCTIONS

FUNCTION	PIN	DESCRIPTION
Load Enable	34T	Input HI for sequential addressing and LO for random addressing. Connect to MDAS Load Enable (pin 24B).
Clear Enable	34B	When input is LO a negative transition on the MDAS Strobe resets Address counter to zero. Connect to MDAS Clear Enable (pin 25B).
Clock	33B	Each LO to HI transition at this input increments the address counter. Connect to MDAS Delay Out (pin 23T).
Carry Out	28B	Output carry of the address counter which is used in double level multiplexing. Connect to MDAS Count Enable (pin 18B).
Address Detector Inputs	22T thru 26T 22B thru 26B	NAND gate inputs used to short cycle the number of channels in sequential mode. When all inputs are HI the Address Counter can be reset. Connect to Address Outputs and leave unused inputs open.
Address Detector Output	33T	For short cycled sequential operation connect to Clear Enable on MDXP-32 (pin 34B) and MDAS (pin 25B). When output goes LO the Address Counter stops and is reset to zero when a negative transition is applied to the MDAS Strobe (pin 25T).
16·32 Out	28T	Decoder output enables channels 0 to 15 of the multiplexer for single level multiplexing. Connect to MDAS (pin 17B) for single-ended operation and MDXP-32 (pins 24B and 24T) for differential operation.
16·32 Out	27T	Decoder output enables channels 16 to 31 of the multiplexer for single-level multiplexing. Connect to pin 24T for single-ended operation and MDAS (pin 17B) for differential operation.
16·32 Out	27B	Decoder output enables channels 32 to 47 of the multiplexer for single-level multiplexing. Connect to pin 24B for single-ended operation and leave unconnected for differential operation.
Address Inputs	29T thru 32T	Input channel address. Connect to MDAS Address Inputs for single-level multiplexing.
Mux Enable	24B, 24T	Input HI enables multiplexer.

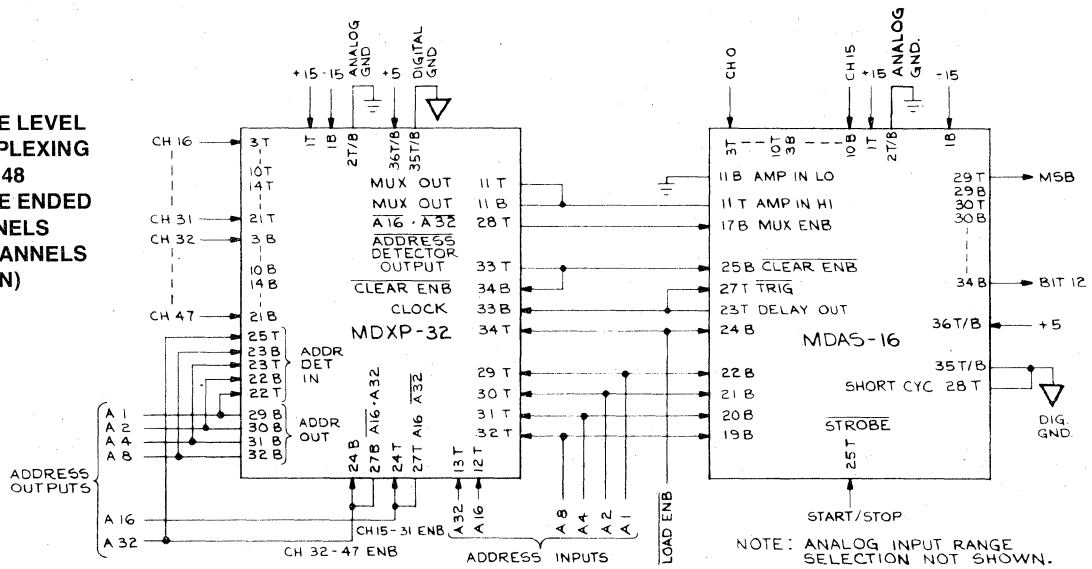
APPLICATION NOTES

SINGLE LEVEL MULTIPLEXING

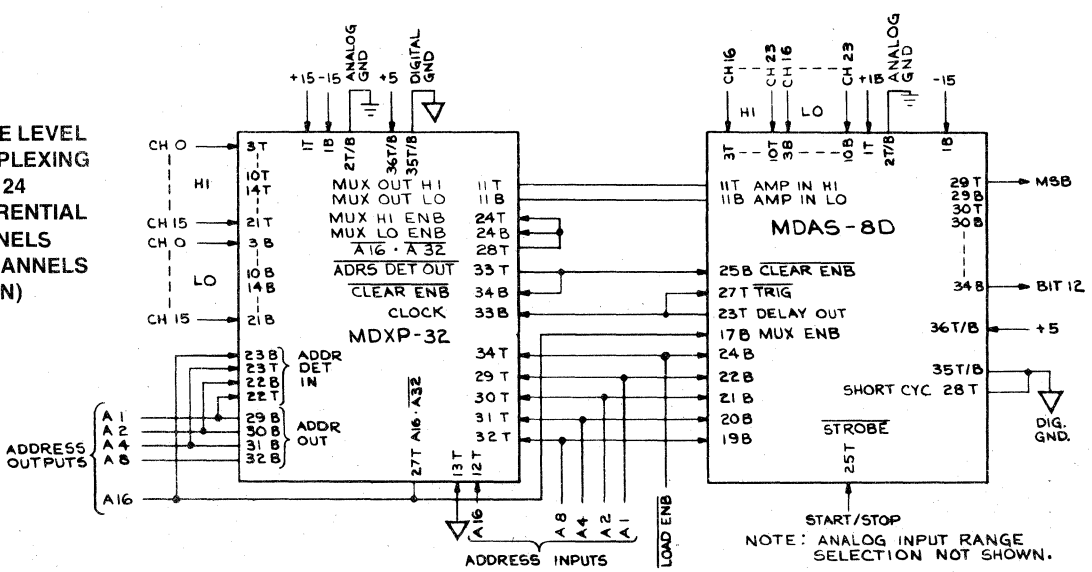
1. For up to 48 single-ended channels or up to 24 differential channels, single level multiplexing is used. This requires one MDAS-16 and one MDXP-32 or one MDAS-8D and one MDXP-32.
2. The three Address Decoder outputs are used in single level multiplexing only, to control the Mux Enable inputs as follows:

   $\overline{16} \cdot \overline{32}$ Output selects Channels 0 to 15 (MDAS pin 17B)
   $16 \cdot \overline{32}$ Output selects Channels 16 to 31 (MDXP-32 pin 24T)
   $\overline{16} \cdot 32$ Output selects Channels 32 to 47 (MDXP-32 pin 24B)
3. Address inputs 1, 2, 4, 8 are common to both MDAS and MDXP-32. Address inputs 16 and 32 are applied to the MDXP-32 only.
4. For short cycling, which is required for sequential operation for any number of channels less than 256, the Address Outputs of the MDXP-32 are connected to the Address Detector Inputs. The rule is to connect Address Outputs whose binary value equals the number of the last channel in sequence. Note that channels are counted from 0 to 47. For example, for 37 channels the Address Outputs 4 and 32 would be used (adding up to 36).

SINGLE LEVEL MULTIPLEXING UP TO 48 SINGLE ENDED CHANNELS (48 CHANNELS SHOWN)



SINGLE LEVEL MULTIPLEXING UP TO 24 DIFFERENTIAL CHANNELS (24 CHANNELS SHOWN)



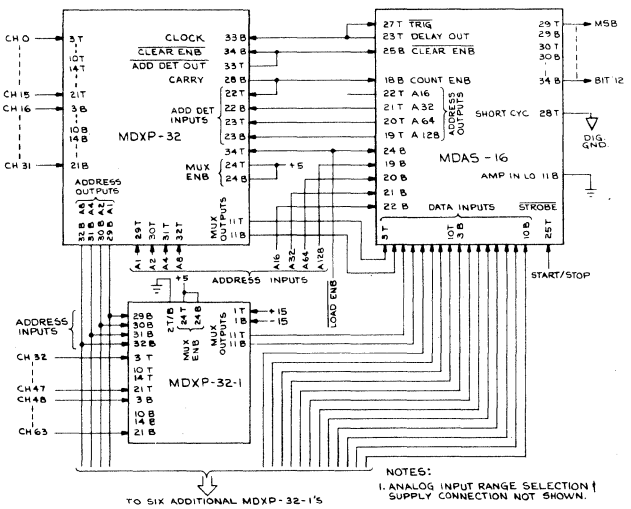
APPLICATION NOTES

DOUBLE LEVEL MULTIPLEXING

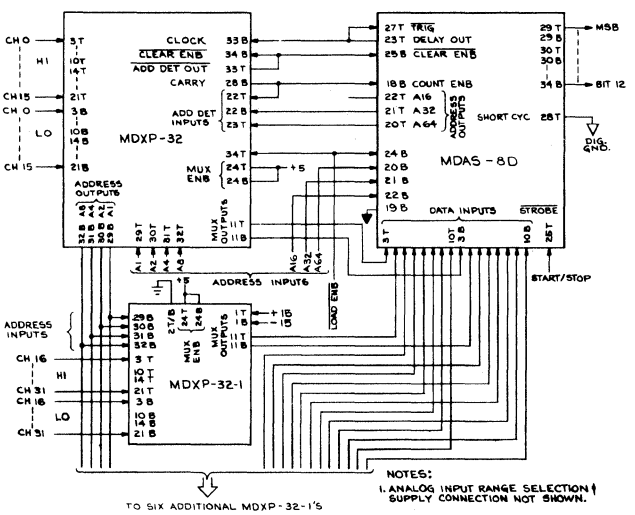
1. For more than 48 single ended channels or more than 24 differential channels, double level multiplexing is required. Up to 256 single ended and up to 128 differential channels may be achieved by double level multiplexing. This technique uses all the channels of the MDAS for the second level of multiplexing so that these channels cannot be used as input channels.
2. One MDXP-32 and one MDAS-16 give 32 single ended channels, and each added MDXP-32-1 gives another 32 channels. Likewise, one MDXP-32 and one MDAS-8D give 16 differential channels and each added MDXP-32-1 gives another 16 channels.
3. With double level multiplexing the Mux Enable inputs of the MDXP-32 and MDXP-32-1's are connected to +5V to permanently enable them.
4. One input to the Address Detector Inputs is the Carry Out (pin 28B). As a result of this connection the other Address Detector Inputs are determined from the desired number of channels as follows:

   Channel No. − 15 = Binary value of Address Outputs
   Remembering that the channel count is from 0 to 255 the address output required for 157 channels would be
   156 − 15 = 140
   This requires binary Address Outputs of 128, 8, and 4.
5. In the case of using the maximum 256 channels, the connection from the Address Detector Output (pin 33T) to Clear Enable (pin 34B) is left open and no Address Detector Inputs are required.

DOUBLE LEVEL MULTIPLEXING FOR UP TO 256 SINGLE ENDED CHANNELS (240 CHANNELS SHOWN)



DOUBLE LEVEL MULTIPLEXING FOR UP TO 128 DIFFERENTIAL CHANNELS (112 CHANNELS SHOWN)



DATEL INTERSIL
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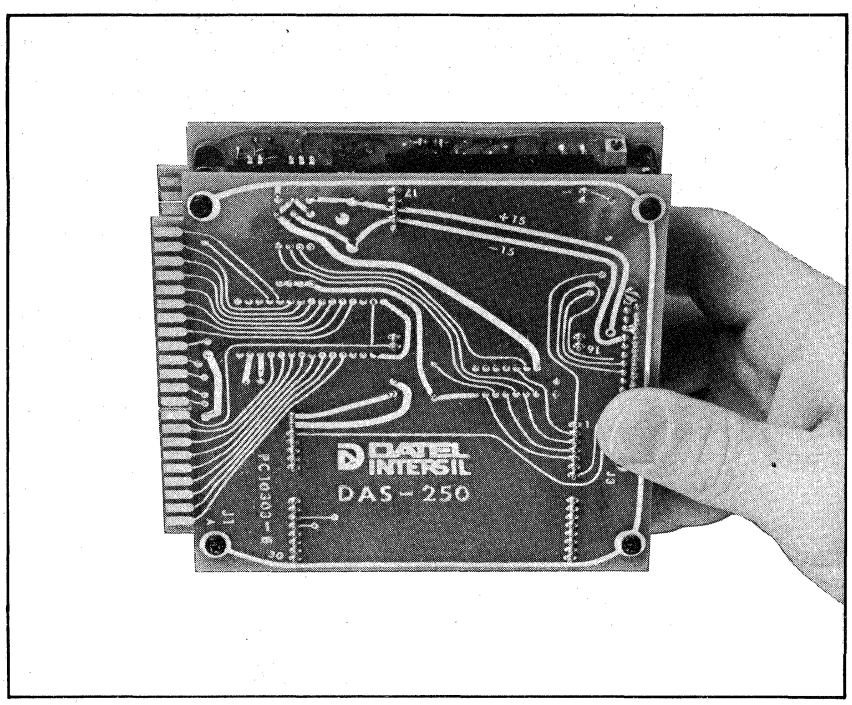
• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

250 KHZ, 12-Bit, 16-Channel Data Acquisition Module Model DAS-250

FEATURES

- **250,000 A/D Samples Per Second**
- **12 Bits, 16 Channels**
- **Double-buffered, Tri-State Gatable Outputs for 4, 8, 12 or 16-bit computer busses**
- **Stored, Open-Collector Bus-Compatible Input Commands**
- **Automatic Channel Sequencing**



DESCRIPTION

Datel's DAS-250 is a very fast, 16-channel data acquisition (A/ D) system with a throughput period of 4 microseconds. The DAS-250 is a modular A/D front end for mini- and microcomputers. When operated with a very fast I/O cycle in the computer (one microsecond or less), data rates in excess of 200,000 analog samples per second may be achieved.

The DAS-250 features a 12-bit binary A/D output and a 4-bit channel address output both of which are latched and gated. This output data may be gated out in 4-bit groups so that 4, 8, 12 or 16 bit computer busses may be used. Most input commands are negative true and may be internally stored using device select and strobe commands. Again, this is ideal for open-collector computer control busses.

The DAS-250 includes an internal 16-channel address counter and analog multiplexer which increments with each A/D conversion for automatic sequential multi-channel scanning. Alternatively, this counter may be used as a jammed register which is loaded with a 4-bit address from an external processor. This latter mode offers random channel addressing whereby some high-activity channels may be sampled more often than others under program control.

The DAS-250 uses Datel's very high speed, fast-settling SHM-5 Sample/Hold amplifier with a 20 nanosecond aperture time and 350 nanosecond settling time. Using this fast S/H amplifier plus latched data outputs and an ADC-EH12B3 A/D converter with 2 microsecond 12-bit conversion performance, the DAS-250 achieves its high speed using overlapped conversion and storage techniques.

The analog multiplexer is switched to a new channel at the start of A/D conversion while the S/H amplifier holds the present analog value stable during conversion. The multiplexer and S/H input stage may then settle and track the next channel while the A/D is converting.

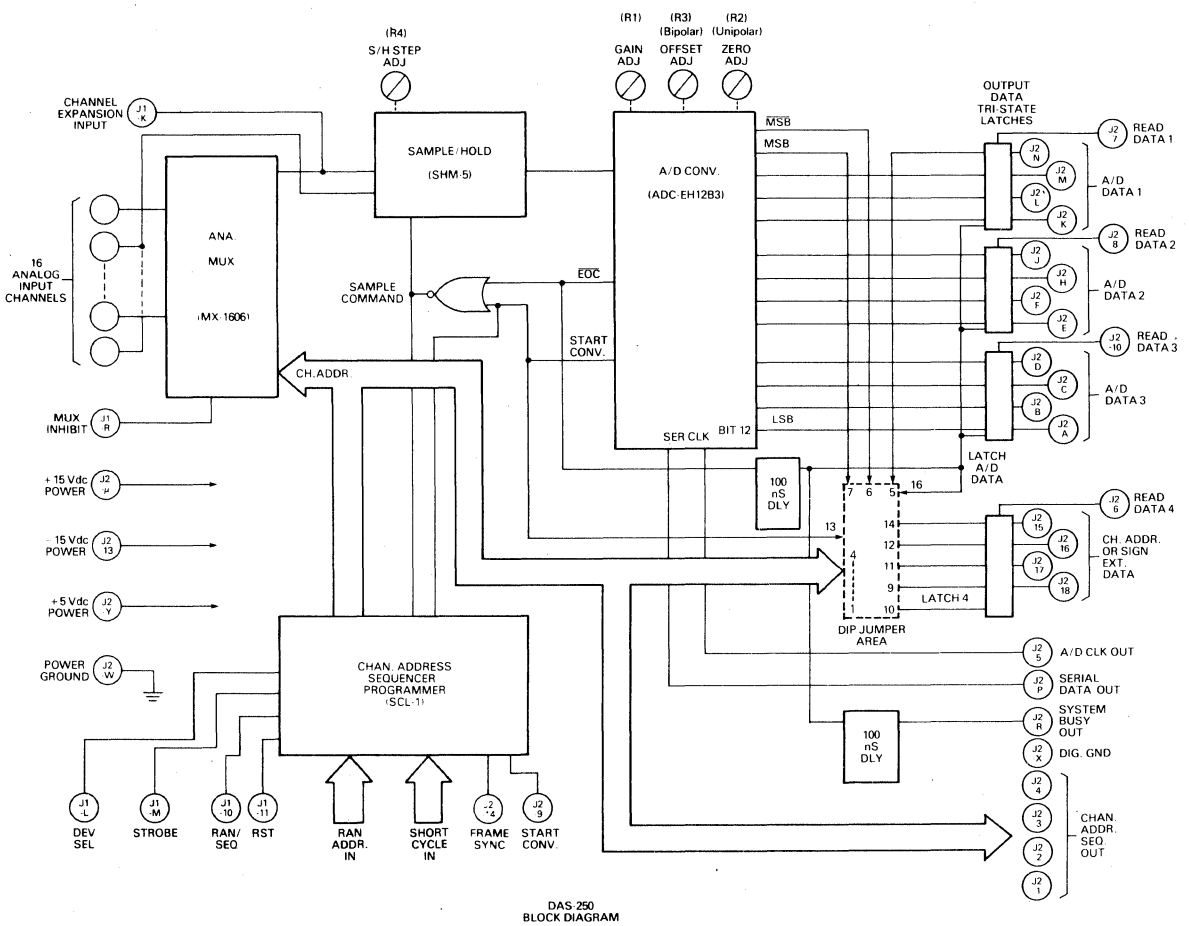
A/D data is valid in the output latches at the end of conversion and channel address data appears at either the beginning or end of conversion (a jumper-selected mode).

The DAS-250 features an overall accuracy of ±0.025% ±1 LSB. It is packaged on 2 small PC boards which are joined by standoffs. Overall dimensions are 4.25"W x 5.00"D with spacing between parallel dual-22-pin PC fingers of 1". Power requirements are +5VDC @ 450 mA (500 mA max.), +15VDC @ 165 mA (180 mA max.) and -15VDC @ 85 mA (100 mA max.), for 6 watts total. The operating temperature range is 0 to +70°.

FOR FULL 250 KHz, 256-CHANNEL SYSTEMS, SEE DATEL'S PDAS-250 SERIES

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

BLOCK DIAGRAM



DAS-250
BLOCK DIAGRAM

Overlapped Conversion and Storage Description

A/D Conversion begins with a start convert command after the input has been previously settled for 2 microseconds minimum. (This is usually achieved by having system reset to channel 1 while idle.) As the A/D conversion is started, the sample/hold (S/H) amplifier switches to temporarily hold the analog voltage stable during conversion. Simultaneously with the convert start, the channel address is stored in the output latches. Another jumper-selected mode delays this address storage until the end of conversion, but will store the next incremented address. This latter mode holds stable data all the way to the next end of conversion for processors which do not want the address data to change at start of conversion. Regardless of the mode chosen, the channel address sequencer is then incremented at start of conversion (or the sequencer is updated with a jamming external address in random mode). To summarize: channel address storage may occur at start or end of conversion, but channel address multiplexer sequencing always occurs at start of conversion (after storage, if done).

The analog multiplexer and sample/hold input stage settle and track the next channel during A/D conversion. At the end of conversion, A/D binary data are stored in the output latches. A slightly delayed BUSY output flags the external processor to collect the data by using Read Data commands to gate data onto the bus from the latches. Address and MSB data should be taken first if the address latch will be updated with the next start convert command. Most fast minicomputers will take the next 2 microseconds to decode the BUSY falling edge and retrieve all data. Since the S/H returns to the sample mode at the end of conversion, one microsecond minimum must be allowed until the next start convert command to let the S/H output stage follow the new channel. The processor will have until the end of the next conversion to read the previous A/D data.

This timing is ideal for 8-bit bus systems which must take data in two bytes yet with high throughput speed. Single-channel operations (such as Fast Fourier Transform vibration analysis), which run in random mode without updating the multiplexer, may achieve speeds up to 300 KHz and beyond, assuming data is taken quickly.

Of the two timing modes (channel address storage occurring at the beginning or end of conversion), storing at the beginning produces an address which coincides with the A/D data, but this address will be lost at the next convert start which occurs in 2 microseconds at 250 KHz. With the address stored at the end of conversion, both the address and A/D data latches are updated simultaneously (at end of conversion). However, the address leads data by one channel.

SPECIFICATIONS MODEL DAS-250 (Typical at +25° C unless noted)

GENERAL

System Type . 16 channel, very high speed Data Acquisition System with automatic sequential or external random channel addressing.

Channel Addressing Modes ..... Random (externally supplied address) or Sequential (internal address counter)

Multiplexer Type ..... Break-before-make CMOS monolithic integrated circuit with internal voltage clamps

ANALOG INPUTS

Number of Channels ... 16 single-ended channels

Channel Expansion . Available using expander input and MUX inhibit at some sacrifice in speed depending on configuration.

Full Scale Input Ranges ..... 0 to -10 Volts (unipolar) or +5V to -5 Volts (bipolar)

Input Overvoltage ±20 Volts maximum sustained (no damage)

Input Impedance 100 Megohms minimum

Input Bias Current ..... 250 nA max.

Input Capacitance 10 pF, OFF channel to ground
100 pF, ON channel to ground

MUX Switches .... 1.5K Ohms, ON resistance, 30 pA, OFF input leakage

PERFORMANCE

Accuracy @ +25° C ..... ±.025% of full scale range ± 1 LSB

Non Linearity ±½ LSB max.

Differential Nonlinearity ±½ LSB max.

Resolution .... 12 Binary Bits (1 part in 4096)

Gain Error ..... Adjustable to zero

Offset or Zero Error ..... Adjustable to zero

Gain Temperature Drift .... ±45ppm of FSR/°C, max.

Zero Temperature Drift .... ±130 μ V/°C, max.

Power Supply Rejection ... 1 mV per Volt

DYNAMIC CHARACTERISITICS

Throughput Period ..... 4 microseconds (See timing diagrams.)

Throughput Rate ..... 250,000 samples per second

Acquisition Time ..... 1.35 microseconds

A/D Conversion Time .. 2 microseconds

Sample/Hold Aperture Time ..... 20 nanoseconds

Sample/Hold Switch Feedthrough ±.005% of input

MUX Crosstalk from OFF channels .... ±.01% of input max.

DIGITAL OUTPUTS

Logic Levels and Loading All digital outputs are TTL levels.
0 = LO = +0.4V Max
1 = HI = +2.4V Min
A/D data outputs can drive 10 TTL loads. The A/D Channel Address outputs can drive 8 TTL loads. Busy and Clock outputs are 74LS and 74S logic, respectively.

Data Output Format ..... (Pins J2-A to J2-N: A/D Data)
(Pins J2-15 to J2-18: Chan. Addr.)
Data is arranged as four 4-bit latchable, gatable, tri-state outputs corresponding to 12 binary bits of A/D data and 4 bits of A/D binary channel address. The 4 channel bits may also be hard-wired as A/D MSB sign extension or hard-wired all zero's or all one's. Coding may be jumper-selected as straight or offset binary or 2's complement.

Output Coding ..... Straight Binary (unipolar) or 2's complement (jumper-selected) or Offset Binary (bipolar) with inverted analog coding.

Channel Address Outputs ..... (Pins J2-1 through J2-4) 4 lines positive true, provides a binary output count of internal channel sequencer. (CH. 1 = 0000, Ch. 16 = 1111)
May be used to short cycle channel scan up to a preselected channel.

Frame Sync Out ..... (Pin J2 - 14) Goes to logic LO during channel one and is HI during channels 2 through 16.

System Busy Out ..... (Pin J2 - R) Delayed End-of-Conversion (Status) output from the A/D converter. A falling edge indicates when data is stabilized in the output buffer. The System Busy should be used to initiate a sequence of Read Data inputs to gate 4-bit output groups to the user's bus from the output buffers.

Serial Data Out ..... (Pin J2 - P) This is a NRZ successive decision pulse generated during the 4 microsecond A/D conversion period. The most significant bit is presented first. This output is very useful for oscilloscope calibration of the A/D converter offset and gain adjust by triggering on the End of Conversion (A/D pin 1).

Serial Data Clock Out .. (Pin J2 - 5) Use the falling edges of this clock to load or shift Serial Data from the A/D converter into external registers.

DIGITAL INPUTS

(NOTE: Most inputs are negative true coding, compatible with most computers and open-collector TTL buses)

$\overline{\text{Device Select}}$ In ..... (Pin J1 - L) A logic LO on this line enables all other inputs (except short cycle inputs and mux inhibit) to be strobed into the DAS-250. This allows the controls to be multiplexed on a common bus with other external devices such as computer parallel I/O ports.

$\overline{\text{Strobe In}}$ ..... (Pin J1 - M) A logic LO on this line loads all other digital inputs into the DAS-250 on the Strobe falling edge. This does not apply to the short cycle address inputs or mux inhibit. The strobe provides for storage of control status and therefore noise immunity when the DAS-250 is operated on a multiplexed bus. The Strobe function occurs only when Device Select is LO. (Strobe and Device Select are NANDed).

$\overline{\text{Mux Inhibit}}$ ... (Pin J1 - R) This line includes an internal 1K ohm +5V pullup resistor so that analog multiplexer inputs are enabled when this line is normally left unconnected. Logic LO inhibits the multiplexer so that additional external channels may be switched through the Expander Input. (Pin J1 - K)

Random/$\overline{\text{Sequential}}$ In ..... (Pin J1 - 10) Logic HI selects the random channel addressing mode. Logic LO allows automatic channel sequencing by the internal channel address counter. Random/$\overline{\text{Sequential}}$ is enabled by ($\overline{\text{Device Select}}$ • $\overline{\text{Strobe}}$)

$\overline{\text{Reset In}}$ ..... (Pin J1 - 11) Logic LO resets the internal channel sequencer to channel 1. Reset is enabled by ($\overline{\text{Device Select}}$ • $\overline{\text{Strobe}}$)

Random Address In .. (4 Pins, J1-P, N, 12, 13) This four-bit binary input is a complementary jam input (when in Random mode) that selects one of 16 channels for data conversion. (Note negative true coding 0 = LO, 1 = HI).
111 = Ch. 1, 1110 = Ch. 2,
0000 = Ch. 16. The Random Address is enabled by ($\overline{\text{Device Select}}$ • $\overline{\text{Strobe}}$)

Short Cycle Channel Address Inputs ..... (Pins J2 - 19 through J2 - 22) These four inputs can be externally tied back to the channel address outputs to terminate the channel scan at any address. These lines are a 4-input NAND gate. To operate an untermi- nated full 16-channel scan, one of the short cycle inputs must be LO. With all inputs HI, the address will be reset to channel 1. Reset to channel one will occur after the addressed channel has been converted.

$\overline{\text{Start Convert}}$ In ..... (Pin J2 - 9) A falling edge triggers the next A/D conversion. Pulse width 50 nSec. min., 2μSec max. This input is enabled by (Device Select • Strobe) and normally, start convert is held low all during scanning with starts initiated by the strobe (see timing).

$\overline{\text{Read Data 1}}$ .... (Pin J2 - 7) A logic LO will gate out A/D bits 1 (MSB) thru 4.

$\overline{\text{Read Data 2}}$ .... (Pin J2 - 8) A logic LO will gate out A/D bits 5 thru 8.

$\overline{\text{Read Data 3}}$ .... (Pin J2 - 10) A logic LO will gate out A/D bits 9 thru 12 (LSB).

$\overline{\text{Read Data 4}}$ .... (Pin J2 - 6) A logic LO will gate out the 4 address bits or MSB sign extension.

Power Requirements (6 Watts total) . +5VDC ±.25V @ 450mA, typ. 500mA, max. Regulated, bypassed power supplies must be used
+15VDC ±.5V @ 165mA, typ. 180mA, max.
-15VDC ±.5V @ 85mA, typ. 100mA, max.
Logic spikes 50 mV max.

PHYSICAL-ENVIRONMENTAL

Size ..... 4.25"W x 5.00"D x 1" spacing between PC card edges

Operating Temperature Range ..... 0 to +70°C (non-condensing)

Storage Temperature Range ..... -55°C to +85°C

Weight ..... 1 pound (0.45 Kg)

Altitude ..... 0 to 15,000 feet (4900 m)

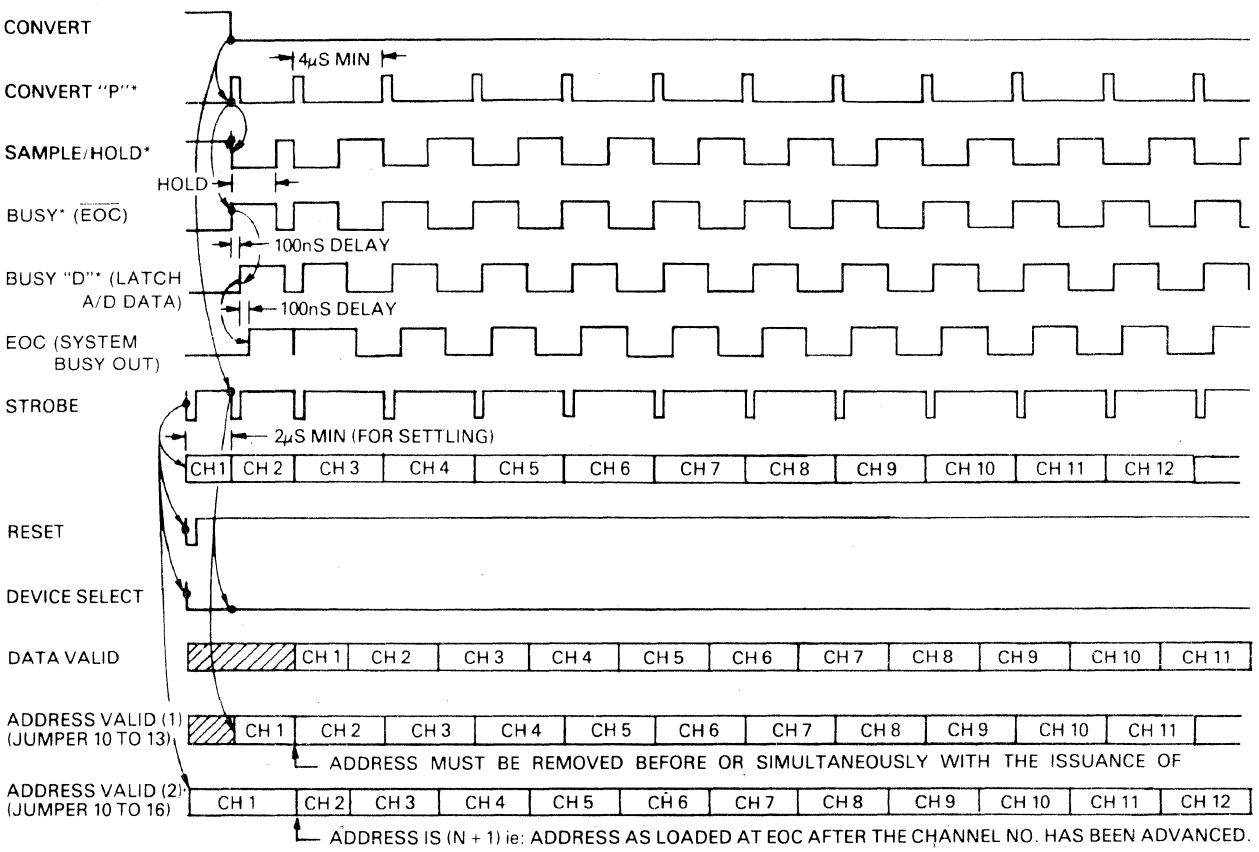
Mounting Method ..... By PC edgeboard connectors. Users may attach standoffs at the 4 module card corners using 4-40 threaded hardware for firmer mounting.

Fabrication ... Modules are soft-potted in black diallyl-phthlate cases with a hard-pot surface.

Ordering Guide

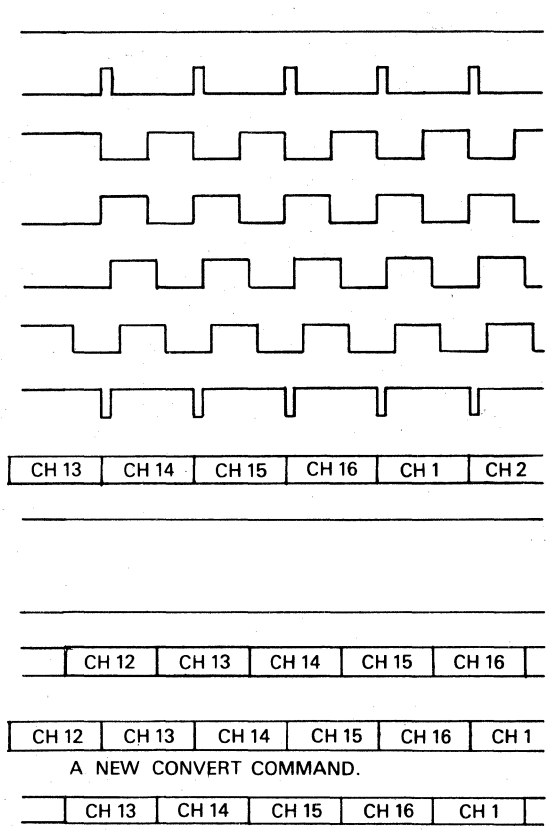
Model Number	Full Scale Analog Input Range	
DAS-250A	0 to -10 Volts	
DAS-250B	+5V to -5V	
36-2075060	Dual 44-pin PC edge connectors, solder tabs, .156"	**2 (included)**
58-12140-27	Instruction Manual	**(included)**

SEQUENTIAL MODE SYSTEM TIMING

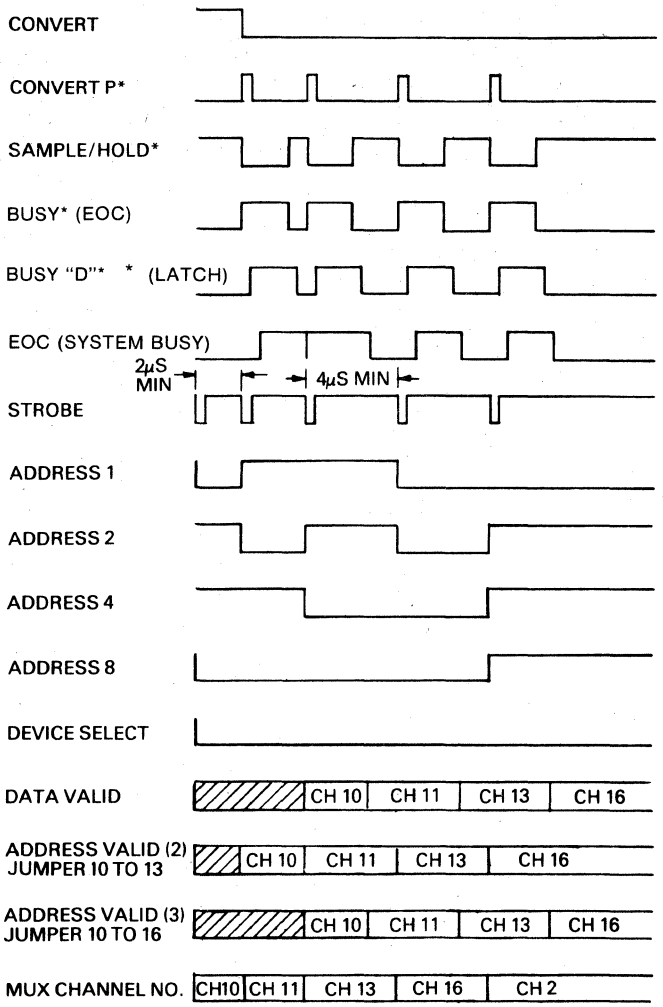


NOTES:

1. * DENOTES INTERNAL SIGNALS.
2. EXAMPLE SHOWN IS FOR 16 SEQUENTIAL CHANNELS AFTER BEEN RESET TO CHANNEL ONE.
3. NOTE THAT AT LEAST 2μ SEC IS REQUIRED TO SELECT THE FIRST CHANNEL. TO AVOID THIS SETTLING TIME IT WOULD BE NECESSARY TO ALWAYS INITIALIZE TO CHANNEL ONE UPON POWER UP & TO RETURN TO CHANNEL ONE AT THE END OF A GIVEN SEQUENCE. (THE LATTER IS AUTOMATICALLY DONE IN THE SEQUENTIAL MODE, WHEN THE LAST CHANNEL IS CONVERTED THE SEQUENCER ADVANCES TO CHANNEL ONE).
4. NOTE THERE ARE TWO JUMPER SELECTABLE OPTIONS FOR ADDRESS VALID. ONE REPRESENTS THE ACTUAL CHANNEL ADDRESS BUT ALLOWS MINIMAL TIME TO READ THE ADDRESS. THE OTHER ALLOWS MAXIMUM TIME TO READ THE ADDRESS BUT THE CHANNEL NUMBER IS (N + 1).
5. SIGNAL NAMES IN (PARENTHESES) ARE THE SAME AS THOSE SHOWN ON THE BLOCK DIAGRAM ON PAGE 2.



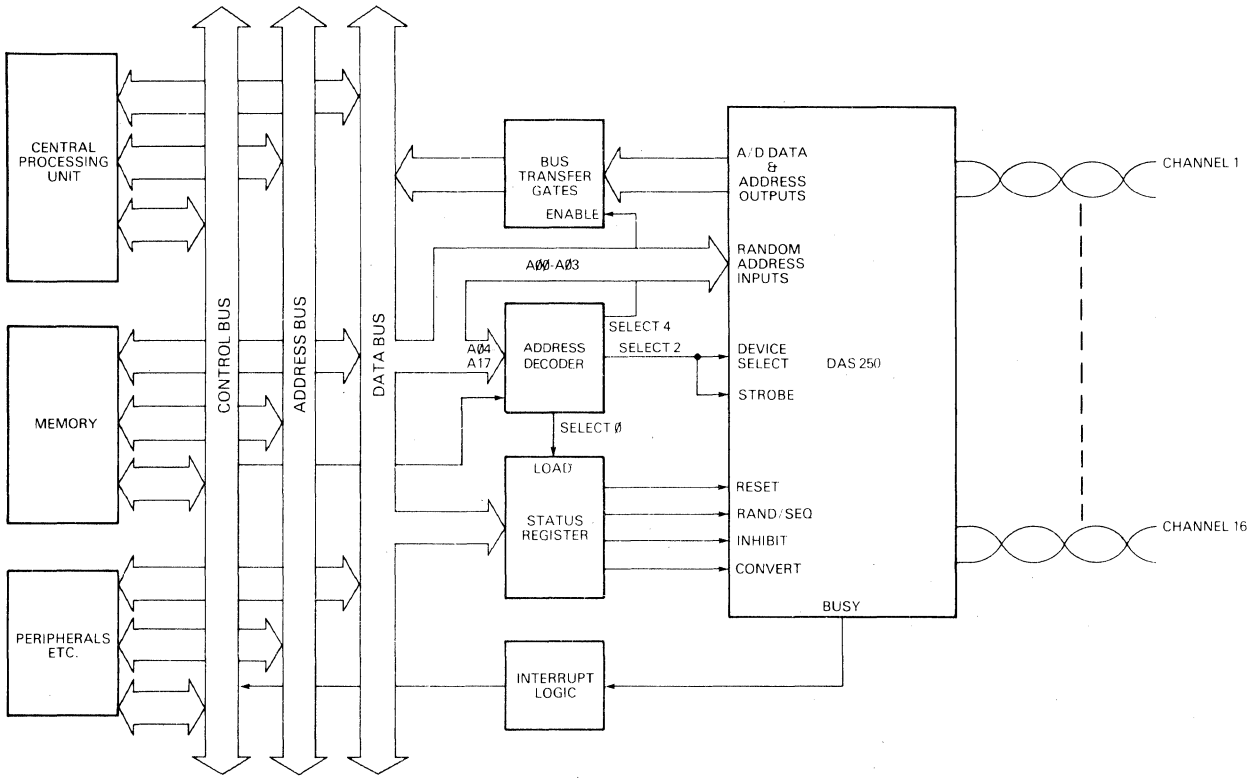
RANDOM MODE SYSTEM TIMING



NOTES:

1. * DENOTES INTERNAL SIGNALS.
2. NOTE THAT IF THE CHANNEL ADDRESS IS GIVEN SIMULTANEOUSLY WITH THE CONVERT COMMAND THE PREVIOUS SELECTED CHANNEL WILL BE HELD BY THE SAMPLE & HOLD AND CONVERTED WHILE THE MULTIPLEXER IS SET TO THE NEW CHANNEL. (THIS ALLOWS THE INPUT TO SETTLE WHILE THE CONVERSION IS BEING MADE.)
3. CHANNEL TWO WAS SELECTED BUT NOT CONVERTED, IF THIS IS TO BE THE FIRST CHANNEL OF THE NEXT SEQUENCE, THE 2μ SEC SETTLING TIME DELAY REQUIRED BETWEEN SELECTING A NEW CHANNEL & CONVERTING DOES NOT APPLY.
4. NOTE THAT ADDRESS VALUE (2) IS MORE DESIRABLE FOR RANDOM OPERATION AS IT IS SYNCHRONOUS WITH THE OUTPUT DATA & REPRESENTS THE ACTUAL CHANNEL CONVERTED.
5. SIGNAL NAMES IN (PARENTHESES) ARE THE SAME AS THOSE SHOWN ON THE BLOCK DIAGRAM ON PAGE 2.

COMPUTER INTERFACE BLOCK DIAGRAM



MINICOMPUTER FRONT END

This block diagram indicates how the DAS-250 may be interfaced to a Digital Equipment Corporation PDP-11 Series minicomputer. The modules labeled "Address Decoder" and "Interrupt Logic" are standard DEC cards, types M105 and M7821 respectively which slide into the computer's connector block. Many interface circuit details have been omitted for clarity and are beyond the scope of this brochure.

To realize the full speed advantage of the DAS-250, a fast minicomputer is desirable. A slower 8-bit microcomputer may also be used and the DAS-250 offers the advantage of quick data conversion 4 microseconds after an external event triggers the start of conversion. By contrast, slower conversion systems require 20 microseconds or greater before data is acquired, sampled and converted.

MOUNTING INSTRUCTIONS

For normal laboratory conditions, the dual card assembly will be adequately supported when mounted vertically in both PC board connectors.

For more rigid mounting in rough service applications, remove the four corner screws on the A/D PC board, labeled PC 10306. The four corner standoffs will remain captive and boards will remain attached by means of the interboard connector. Drill four 0.129" holes (#30 drill) on the desired mounting surface using the side view dimensions. Assemble four 4-40 bolts with 0.205" min spacers through the mounting surface and A/D board to thread into the captive standoffs.

MODEL DAS-250, INPUT/OUTPUT CONNECTIONS

CONNECTOR J1

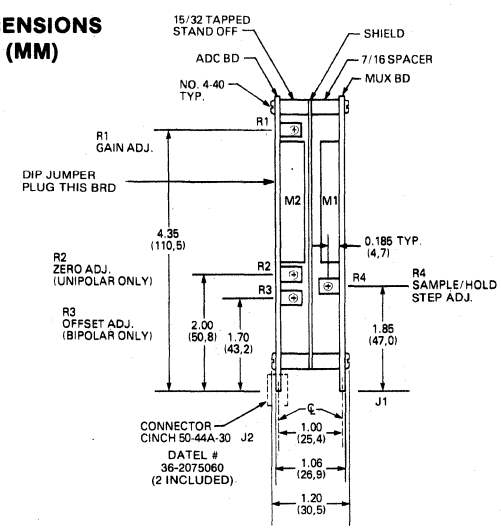
PIN	FUNCTION	PIN	FUNCTION
A	CH. 16 HI ANALOG INPUT	1	CH. 16 LO ANALOG INPUT
B	CH. 15 HI ANALOG INPUT	2	CH. 15 LO ANALOG INPUT
C	CH. 14 HI ANALOG INPUT	3	CH. 14 LO ANALOG INPUT
D	CH. 13 HI ANALOG INPUT	4	CH. 13 LO ANALOG INPUT
E	CH. 12 HI ANALOG INPUT	5	CH. 12 LO ANALOG INPUT
F	CH. 11 HI ANALOG INPUT	6	CH. 11 LO ANALOG INPUT
H	CH. 10 HI ANALOG INPUT	7	CH. 10 LO ANALOG INPUT
J	CH. 9 HI ANALOG INPUT	8	CH. 9 LO ANALOG INPUT
K	MUX. EXPDR. INPUT	9	AUX. LO ANALOG INPUT
L	DEVICE SELECT IN	10	RANDOM/SEQUENTIAL IN
M	STROBE INPUT	11	RESET IN
N	2 RANDOM ADDR. INPUT	12	4 RANDOM ADDR. INPUT
P	1 RANDOM ADDR. INPUT	13	8 RANDOM ADDR. INPUT
R	INHIBUT MUX.	14	AUX. LO ANALOG INPUT
S	CH. 8 HI ANALOG INPUT	15	CH. 8 LO ANALOG INPUT
T	CH. 7 HI ANALOG INPUT	16	CH. 7 LO ANALOG INPUT
U	CH. 6 HI ANALOG INPUT	17	CH. 6 LO ANALOG INPUT
V	CH. 5 HI ANALOG INPUT	18	CH. 5 LO ANALOG INPUT
W	CH. 4 HI ANALOG INPUT	19	CH. 4 LO ANALOG INPUT
X	CH. 3 HI ANALOG INPUT	20	CH. 3 LO ANALOG INPUT
Y	CH. 2 HI ANALOG INPUT	21	CH. 2 LO ANALOG INPUT
Z	CH. 1 HI ANALOG INPUT	22	CH. 1 LO ANALOG INPUT

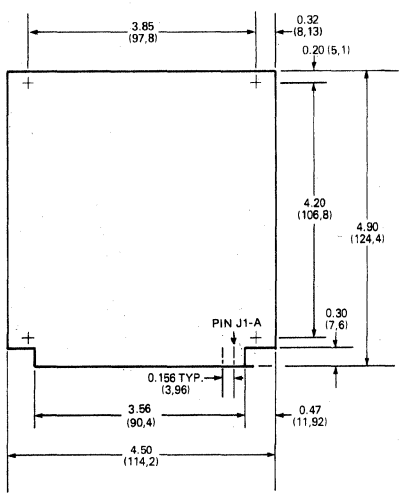
CONNECTOR J2

PIN	FUNCTION	PIN	FUNCTION
A	BIT 12 ADC OUTPUT (LSB)	1	BIT 1 CH. ADDR. OUTPUT
B	BIT 11 ADC OUTPUT	2	BIT 2 CH. ADDR. OUTPUT
C	BIT 10 ADC OUTPUT	3	BIT 4 CH. ADDR. OUTPUT
D	BIT 9 ADC OUTPUT	4	BIT 8 CH. ADDR. OUTPUT
E	BIT 8 ADC OUTPUT	5	ADC SER. CLK. OUTPUT
F	BIT 7 ADC OUTPUT	6	READ DATA 4
H	BIT 6 ADC OUTPUT	7	READ DATA 1
J	BIT 5 ADC OUTPUT	8	READ DATA 2
K	BIT 4 ADC OUTPUT	9	START A/D CONVERT IN
L	BIT 3 ADC OUTPUT	10	READ DATA 3
M	BIT 2 ADC OUTPUT	11	NO CONNECTION
N	BIT 1 ADC OUTPUT (MSB)	12	NO CONNECTION
P	ADC SERIAL OUTPUT	13	-15 VDC POWER INPUT
R	SYSTEM BUSY OUTPUT	14	FRAME SYNC. OUTPUT
S	NO CONNECTION	15	BIT 1 LATCHED ADDR. OUT
T	NO CONNECTION	16	BIT 2 LATCHED ADDR. OUT
U	+15 VDC POWER INPUT	17	BIT 4 LATCHED ADDR. OUT
U	NO CONNECTION	18	BIT 8 LATCHED ADDR. OUT
W	GROUND	19	BIT 1 SHORT CYCLE IN.
X	GROUND	20	BIT 2 SHORT CYCLE IN.
Y	+5 VDC POWER INPUT	21	BIT 4 SHORT CYCLE IN.
Z	+5 VDC POWER INPUT	22	BIT 8 SHORT CYCLE IN.

Connector functions are arranged in vertical edgeboard view

OUTLINE DIMENSIONS INCHES - (MM)





A/D OUTPUT DATA CODING (Input voltages are system inputs)

UNIPOLAR (0V TO -10V)

SCALE	INPUT VOLTAGE	STRAIGHT BINARY
-FS + 1 LSB	-9.9976V	1111 1111 1111
-7/8 FS	-8.7500V	1110 0000 0000
-3/4 FS	-7.5000V	1100 0000 0000
-1/2 FS	-5.0000V	1000 0000 0000
-1/4	-2.5000V	0100 0000 0000
-1 LSB	-0.0024V	0000 0000 0001
0	0.0000V	0000 0000 0000

BIPOLAR (+5V TO -5V)

SCALE	INPUT VOLTAGE	OFFSET BINARY
-FS + 1 LSB	-4.9976V	1111 1111 1111
-3/4 FS	-3.7500V	1110 0000 0000
-1/2 FS	-2.5000V	1100 0000 0000
0	0.0000V	1000 0000 0000
+1/2 FS	+2.5000V	0100 0000 0000
+3/4 FS	+3.7500V	0010 0000 0000
+FS - 1 LSB	+4.9976V	0000 0000 0001
+FS	+5.0000V	0000 0000 0000

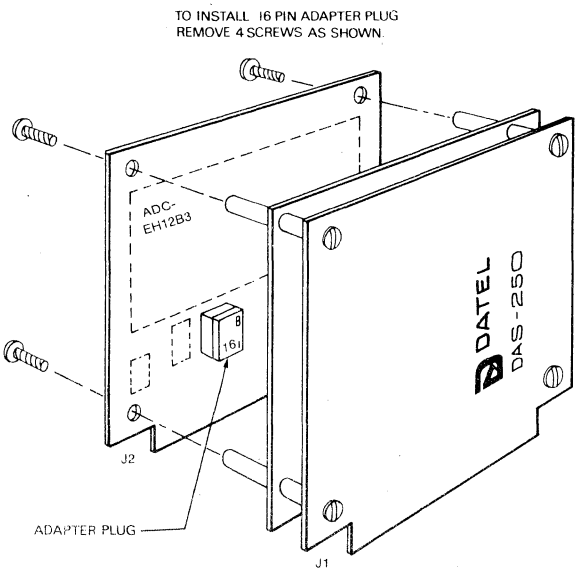
NOTE: ANALOG INPUT IS INVERTING
OTHER INPUT RANGES ARE AVAILABLE
FOR QUANTITY ORDERS CONTACT FACTORY

DIP JUMPER PLUG WIRING

Output Type	Install Jumpers
1. Next Channel Address (Stores address of *next* channel at falling edge of Busy out)	4 to 9, 3 to 11, 2 to 12, 1 to 14, 10 to 16
2. Present Channel Address (Stores address of *present* channel at rising edge of Busy out)	4 to 9, 3 to 11, 2 to 12 1 to 14, 10 to 13
3. Sign Extension of ADC Bit 1 (MSB), Straight Binary or Offset Binary	5 to 9, 5 to 7, 9 to 11, 11 to 12, 12 to 14
4. Sign Extension of ADC Bit 1 (MSB), 2's Complement	5 to 9, 5 to 6, 9 to 11, 11 to 12, 12 to 14
5. Leading Zero's	8 to 9, 9 to 11, 11 to 12, 12 to 14, 10 to 16

Bipolar Output Coding:

Offset Binary (Bit 1 = MSB)	Jumper 5 to 7
2's Complement (Bit 1 = MSB)	Jumper 5 to 6



DIP JUMPER PLUG WIRING AND INSTALLATION

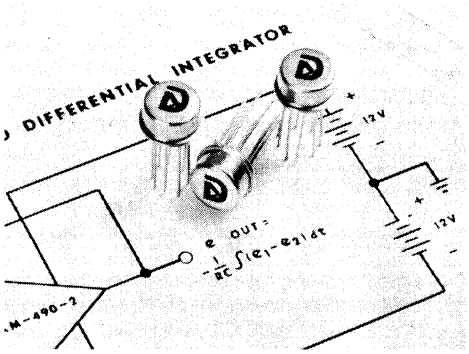
The DAS-250 has a 16-bit full parallel data output. Twelve bits of this data are for A/D converter output. The additional four bits are unassigned and may be set by the user to indicate one of five data output types (see listing). These include the analog channel address (either the present address or next address), sign extension (either binary or two's complement coding) or all zeros. The channel address outputs are useful to the computer if the DAS-250 is controlling its own channel sequencing. Or they may be used to confirm a random channel address commanded by the computer. Sign extension mirrors the ADC most significant bit over to the highest order bit in the computer's accumulator. With bipolar inputs, this simplifies polarity detection of the data since the computer can test the displaced MSB by using a shift left (rotate) instruction. This enhances accumulator binary arithmetic (for example, simple averages). Also, data arithmetic carries into the accumulator's flag bit, which can be easily tested.

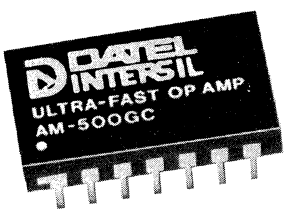
The five modes for the DAS-250's unassigned address bits are selected by soldering appropriate jumpers onto a 16-pin DIP plug (supplied) which inserts into a socket on the A/D board inside the DAS-250. This board is identified as having only one large module (the ADC-EH12B3 A/D Converter.)

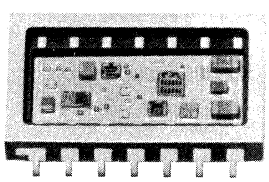
The two PC boards of the DAS-250 must be separated to gain access to the DIP plug socket. Remove the four corner screws on the PC board labeled PC 10306 *(opposite* the PC board with "Datel DAS-250" etch). With the screws removed, only the interboard connector will remain holding the boards together. Separate the connector halves. The corner standoffs are threaded and will remain captive. After wiring the DIP jumper plug, insert it into its socket with the notch (pins 1 and 16) facing toward the PC edge connector, J2 (facing away from the ADC module). Reassemble the interboard connector and tighten the four corner screws.

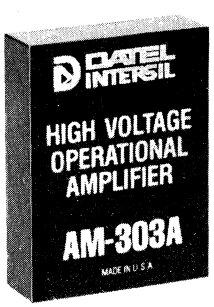
DATEL INTERSIL
11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617)339-9341 / TWX 710-346-1953 / TLX 951340
Santa Ana, (714)835-2751, (L.A.) (213)933-7256 • Sunnyvale, CA (408)733-2424 • Gaithersburg, MD (301)840-9490
• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

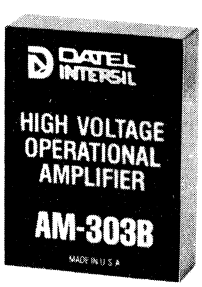
Operational Amplifiers











Quick Selection: High Performance Op Amps

	MODEL	DESCRIPTION	DC OPEN LOOP GAIN	GAIN BAND-WIDTH	SLEW RATE (V/ sec)	SETTLING TIME TO 0.1%[1]	OUTPUT, MIN.	COM. MODE RANGE, MIN.
MONOLITHIC	AM-410-2C	Wideband, JFET	100K	18 MHz	8	2 μsec	± 11V	± 10V
	AM-410-2M	Input, Compensated	150K			1.7 μsec	± 12V	
	AM-411-2C	Wideband, JFET	100K	50 MHz	40	1 μsec	± 11V	± 10V
	AM-411-2M	Input, Uncomp.	150K	60 MHz	50	.85 μsec	± 12V	
	AM-414-2A	Ultra-Low Drift	400K	600 kHz	0.17	—	± 11.5V	± 13V
	AM-414-2B	Chopperless Op	500K				± 12V	
	AM-414-2M	Amp						
	AM-453-2C	Low Noise Wide-	100K	10 MHz	13	—	± 12V	± 12V
	AM-453-2M	band Op Amp						
	AM-460-2C	Wideband, Fast	150K	12 MHz	7	1.5 μsec	± 10V	± 11V
	AM-460-2M	Settling Op Amp						
	AM-490-2A	Chopper Stabilized	5×10^8	3 MHz	2.5	—	± 10V	± 10V
	AM-490-2B							
	AM-490-2C							
	AM-490-2M							
	AM-7600C	Ultra-Low Off-	105 dB	1.2 MHz	1.8	—	± 4.9V	± 4.2V
	AM-7600R	set CAZ Op Amp						
	AM-7600M	Compensated						
	AM-7601C	Ultra-Low Off-	105 dB	1.8 MHz	1.8	—	± 4.9V	± 4.2V
	AM-7601R	set CAZ Op Amp						
	AM-7601M	Uncompensated						

NOTES: 1. 10V output step unless otherwise noted.
2. Adjustable to Zero.

COMMON MODE REJECTION	INPUT IMPEDANCE	INPUT BIAS CURRENT, MAX.	INPUT OFFSET CURRENT, MAX.	INPUT OFFSET VOLTAGE, MAX.[2]	INPUT OFFSET VOLTAGE DRIFT	POWER SUPPLY RANGE	OPERATING TEMP(°C)	PRICE (1-24)	SEE PAGE
86 dB	10^{12}	100 pA	50 pA	1.5 mV	15 V/°C	±5VDC to	0 to +70	**$ 6.95**	314C
		50 pA	10 pA	1.0 mV	5 V/°C	±20VDC	−55 to +125	**$29.50**	
86 dB	10^{12}	100 pA	50 pA	1.5 mV	15 V/°C	±5VDC to	0 to +70	**$ 9.95**	314C
		50 pA	10 pA	1.0 mV	5 V/°C	±20 VDC	−55 to +125	**$32.50**	
100 dB	33 G	±7 nA	±6 nA	150 V	2.0 V/°C	±3VDC to	0 to +70	**$ 7.00**	318C
106 dB	50 G	±4 nA	±3.8nA	75 V	1.3 V/°C	±18VDC	0 to +70	**$12.95**	
110 dB	60 G	±3 nA	±2.8nA				−55 to +125	**$22.50**	
100 dB	100 K	1.5 A	300 nA	4 mV	30 V/°C	±3VDC to	0 to +70	**$ 6.50**	324C
						±20VDC	−55 to +125	**$19.50**	
100 dB	300 M	25 nA	25 nA	5 mV	10 V/°C	±5VDC to	0 to +70	**$ 3.50**	320C
						±22.5VDC	−55 to +125	**$14.50**	
120 dB	100 M	150 pA	50 pA	20 V	1.0 V/°C	±12VDC to	0 to +70	**$30.50**	330C
					0.3 V/°C	±20VDC	0 to +70	**$36.00**	
					0.1 V/°C		0 to +70	**$41.00**	
					0.6 V/°C		−55 to +125	**$99.50**	
88 dB	—	3 nA	1.5 nA	5 V	.01 V/°C	±4VDC to	0 to +70	**$ 9.81**	334C
						±16VDC	−25 to +85	**$15.07**	
							−55 to +125	**$30.07**	
88 dB	—	3 nA	1.5 nA	5 V	.01 V/°C	±4VDC to	0 to +70	**$ 9.81**	334C
						±16VDC	−25 to +85	**$15.07**	
							−55 to +125	**$30.07**	

1. 10V output step unless otherwise noted.
2. Adjustable to Zero.

THESE PRODUCTS ARE COVERED BY GSA CONTRACT

Quick Selection:
High Performance Op Amps

	MODEL	DESCRIPTION	DC OPEN LOOP GAIN	GAIN BAND-WIDTH	SLEW RATE (V/μsec)	SETTLING TIME TO 0.1%[1]	OUTPUT, MIN.	COM. MODE RANGE, MIN.	COM. MODE REJECTION
	AM-470-2C **AM-470-2M**	Low Power, High Performance Op Amp	300K V/V	1 MHz	20	—	±12V	±11V	106 dB
MONOLITHIC	**AM-7611C** **AM-7611M**	Low Power, Selectable Quiescent Current	104 dB	1.4 MHz	1.6	—	±4.9V	±4.4	96 dB
MONOLITHIC	**AM-7612C** **AM-7612M**	Low Power, Extended Com. Mode Volt. Range	104 dB	1.4 MHz	1.6	—	±4.9V	±5.3	96 dB
MONOLITHIC	**AM-7613C** **AM-7613M**	Low Power, Input Protected to ±200V	104 dB	1.4 MHz	1.6	—	±4.9V	±4.4	96 dB
MONOLITHIC	**AM-7614C** **AM-7614M**	Low Power, External Compensation	104 dB	1.4 MHz	1.6	—	±4.9V	±4.4	96 dB
MONOLITHIC	**AM-7615C** **AM-7615M**	External Compensation, Input Protected ±200V	104 dB	1.4 MHz	1.6	—	±4.9V	±4.4	96 dB
MONOLITHIC	**AM-464-2C** **AM-464-2M**	High Voltage Op Amp	100K V/V	4 MHz	5	—	±35V	±35V	74 dB
HYBRID	**AM-8510R** **AM-8510M**	Hybrid Power Op Amp	100 dB	30 kHz	0.5	—	±24V @ 1A	±10V	70 dB
HYBRID	**AM-8520R** **AM-8520M**	Hybrid Power Op Amp	100 dB	30 kHz	0.5	—	±24V @ 2A	±10V	70 dB
HYBRID	**AM-8530R** **AM-8530M**	Hybrid Power Op Amp	100 dB	30 kHz	0.5	—	±24V @ 2.7A	±10V	70 dB
MOD	**AM-303A** **AM-303B**	Modular High Voltage Op Amp	10^6 V/V	10 MHz	100	2.5 μsec	±140V @ 20mA	±140V	100 dB

NOTES: 1. 10V output step unless otherwise noted.
2. Adjustable to zero.

INPUT IMPEDANCE	INPUT BIAS CURRENT, MAX.	INPUT OFFSET CURRENT, MAX.	INPUT OFFSET VOLTAGE, MAX.[2]	INPUT OFFSET VOLTAGE DRIFT	POWER SUPPLY RANGE	OPERATING TEMP (°C)	PRICE SINGLES	SEE PAGE
500 MΩ	40 nA	15 nA	5 mV	5μV/°C	±5.5VDC to ±20VDC	0 to +70	$ 9.50	328C
						-55 to +125	$ 31.00	
$10^{12}\Omega$	50 pA	30 pA	5 mV	15μV/°C	±0.5VDC to ±8VDC	0 to +70	$ 2.85	344C
						-55 to +125	$ 5.25	
$10^{12}\Omega$	50 pA	30 pA	5 mV	15μV/°C	±0.5VDC to ±8VDC	0 to +70	$ 3.15	344C
						-55 to +125	$ 7.05	
$10^{12}\Omega$	50 pA	30 pA	5 mV	15μV/°C	±0.5VDC to ±8VDC	0 to +70	$ 2.95	344C
						-55 to +125	$ 6.35	
$10^{12}\Omega$	50 pA	30 pA	5 mV	15μV/°C	±0.5VDC to ±8VDC	0 to +70	$ 2.50	344C
						-55 to +125	$ 5.25	
$10^{12}\Omega$	50 pA	30 pA	5 mV	15μV/°C	±0.5VDC to ±8VDC	0 to +70	$ 2.95	344C
						-55 to +125	$ 6.35	
200 MΩ	30 nA	30 nA	6 mV	15μV/°C	±10VDC to ±40VDC	0 to +70	$ 8.00	326C
						-55 to +125	$ 36.00	
30 MΩ	500 nA	200 nA	6 mV	67μV/°C	±18VDC to ±30VDC	-25 to +85	$ 30.99	352C
				60μV/°C		-55 to +125	$ 46.19	
30 MΩ	500 nA	200 nA	6 mV	67μV/°C	±18VDC to ±30VDC	-25 to +85	$ 34.74	352C
				60μV/°C		-55 to +125	$ 51.99	
30 MΩ	500 nA	200 nA	6 mV	67μV/°C	±18VDC to ±30VDC	-25 to +85	$ 51.99	352C
				60μV/°C		-55 to +125	$ 65.04	
$10^{12}\Omega$	100 pA	30 pA	1 mV	50μV/°C	±15VDC to ±150VDC	0 to +70	$105.00	360C
				20μV/°C		0 to +70	$140.00	

Datel offers modular products in operating temperature ranges of −25 to +85°C (suffix-EX) and −55 to +85°C (suffix-EXX-HS). For information on these high reliability modules contact nearest Datel sales office.

THESE PRODUCTS ARE COVERED BY GSA CONTRACT

Quick Selection: High Speed Op Amps

	MODEL	DESCRIPTION	DC OPEN LOOP GAIN	GAIN BAND-WIDTH	SLEW RATE (V/μsec)	SETTLING TIME TO 0.1%[1]	OUTPUT, MIN.	COM. MODE RANGE, MIN.	COM. MODE REJECTION
MONOLITHIC	**AM-450-2** **AM-450-2M**	Wideband Fast Settling Op Amp	25K	12 MHz	30	330nsec	±10V	±10V	90 dB
	AM-452-2 **AM-452-2M**	Wideband Fast Settling	15K	20 MHz	120	200nsec	±10V	±10V	90 dB
	AM-462-1, -2 **AM-462-1M, 2M**	Wideband Fast Settling	150K	100 MHz	35	1μsec	±10V	±11V	100 dB
HYBRID	**AM-500GC** **AM-500MC** **AM-500MR** **AM-500MM**	Ultra-Fast Hybrid Inverting Op Amp	10^6	130 MHz	1000	200nsec	±10V @50mA	—	—
MODULES	**AM-100A** **AM-100B** **AM-100C**	Fast Settling Modular Op Amp	300K	13.5 MHz	45	550nsec	±10V @20mA	±10V	70 dB
	AM-101A **AM-101B**	Optimized for Capac. Loads	300K	5.5 MHz	45	1μsec	±10V @20mA	±10V	93 dB
	AM-102A **AM-102B**	Fast Settling Follower	130K	32 MHz	140	550nsec	±10V @20mA	±10V	93 dB
	AM-103A **AM-103B**	Fast Slewing Modular Op Amp	130K	32 MHz	400	350nsec	±10V @20mA	±10V	70 dB

NOTES: 1. 10V output step unless otherwise noted.
2. Adjustable to zero.

INPUT IMPEDANCE	INPUT BIAS CURRENT, MAX.	INPUT OFFSET CURRENT, MAX.	INPUT OFFSET VOLTAGE, MAX.[2]	INPUT OFFSET VOLTAGE DRIFT	POWER SUPPLY RANGE	OPERATING TEMP (°C)	PRICE SINGLES	SEE PAGE
50 MΩ	250 nA	50 nA	8 mV	20μV/°C	±10VDC to ±20VDC	0 to +70	**$ 3.95**	320C
						-55 to +125	**$ 14.50**	
100 MΩ	250 nA	50 nA	5 mV	30μV/°C	±10VDC to ±20VDC	0 to +70	**$ 10.50**	320C
						-55 to +125	**$ 26.50**	
300 MΩ	25 nA	25 nA	3 mV	15μV/°C	±5VDC to ±22.5VDC	0 to +70	**$ 9.50**	320C
						-55 to +125	**$ 18.00**	
30 MΩ	4 nA	0.5 nA	3 mV	5μV/°C	±10VDC to ±18VDC	0 to +70	**$ 69.00**	350C
						0 to +70	**$ 89.00**	
						-25 to +85	**$104.00**	
						-55 to +125	***$149.00**	
$10^{12}\Omega$	100 pA	10 pA	—	50μV/°C	±15VDC	0 to +70	**$ 59.00**	**
	50 pA			25μV/°C		0 to +70	**$ 63.00**	
	20 pA			10μV/°C		0 to +70	**$ 69.00**	
$10^{12}\Omega$	50 pA	10 pA	—	40μV/°C	±15VDC	0 to +70	**$ 61.00**	**
	20 pA			20μV/°C		0 to +70	**$ 66.00**	
$10^{12}\Omega$	50 pA	10 pA	—	40μV/°C	±15VDC	0 to +70	**$ 63.00**	**
				20μV/°C		0 to +70	**$ 72.00**	
$10^{12}\Omega$	50 pA	10 pA	—	40μV/°C	±15VDC	0 to +70	**$ 63.00**	**
				20μV/°C		0 to +70	**$ 72.00**	

*Available with MIL-STD-833 Class B Screening
**For Data Sheet contact nearest Datel sales office.

THESE PRODUCTS ARE COVERED BY GSA CONTRACT

Datel offers modular products in operating temperature ranges of −25 to +85°C (suffix-EX) and −55 to +85°C (suffix-EXX-HS). For information on these high reliability modules contact nearest Datel sales office.

Wide Bandwidth, FET Input Monolithic Operational Amplifier AM-410 & AM-411 SERIES

FEATURES

- **60 MHz — Gain Bandwidth**
- **50 V/μsec — Slew Rate**
- **850 nsec — Settling to 0.1%**
- **150,000 — Open Loop Gain**
- **5 μV/°C — Input Offset Voltage Drift**
- **$10^{12}\Omega$ — Input Impedance**

GENERAL DESCRIPTION

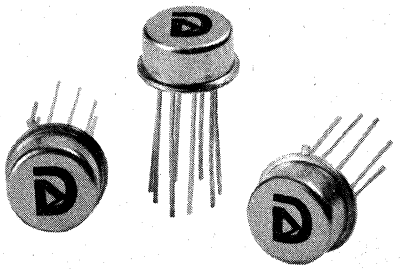
The AM-410 and AM-411 series are monolithic wideband operational amplifiers manufactured with FET/bipolar technology. Active laser trimming of the input stage complements the high frequency capabilities of these amplifiers with excellent input characteristics. Features available on both devices include an input offset voltage of 1 mV maximum with a temperature drift of typically 5 μV/°C, input bias current of 50 pA maximum, and an input impedance of $10^{12}\Omega$. All devices provide a ±11V output at 8 mA, and open loop voltage gain of up to 150,000.

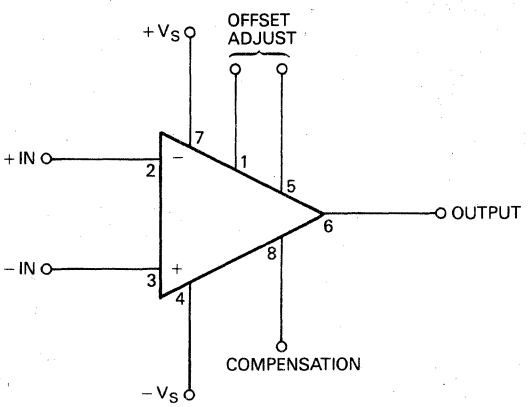
The AM-410 devices are compensated for unity gain operation. The dynamic characteristics of these devices include 10 MHz unity gain bandwidth, 8V/μsec slew rate, and a settling time of 1.7 μsec.

The AM-411 series units are uncompensated devices that are stable at closed loop gains of greater than 10 without external compensation. These units feature dynamic characteristics that include 60 MHz gain bandwidth, 50V/μ slew rate, and a settling time of 850 nsec.

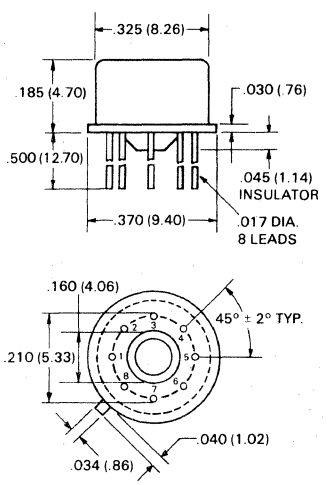
These devices are ideal for use in sample and hold circuits, active filters, A/D input buffering, D/A output amplification and a wide variety of signal conditioning applications.

All models are available in both 0°C to +70°C operating temperature range or −55°C to +125°C for suffix M models. All devices are packaged in a hermetically sealed, 8 pin, TO-99 case.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	OFFSET ADJUST
2	−INPUT
3	+INPUT
4	−Vs
5	OFFSET ADJUST
6	OUTPUT
7	+Vs
8	BANDWIDTH CONTROL
CASE IS CONNECTED TO -SUPPLY	

DATEL-INTERSIL, INC. 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, AM-410, AM-411

Typical at 25°C, ±15 VDC supplies, unless otherwise noted.

	AM-410-2C	AM-410-2M	AM-411-2C	AM-411-2M
MAXIMUM RATINGS				
Power Supply Voltage	±20VDC			
Differential Input Voltage	40V			
Peak Output Current	Full Short Circuit Protection			
Internal Power Dissipation[1]	300mW			
INPUT CHARACTERISTICS				
Input Offset Voltage, max.[2]	1.5mV	1.0mV	1.5mV	1.0mV
Input Offset Current, max.	50pA	10pA	50pA	10pA
Input Bias Current, max.	100pA	50pA	100pA	50pA
Input Resistance	$10^{12}\Omega$	$10^{12}\Omega$	$10^{12}\Omega$	$10^{12}\Omega$
Common Mode Voltage Range, min.	±10V	±10V	±10V	±10V
OUTPUT CHARACTERISTICS				
Output Voltage Swing, min.[3]	±11V	±12V	±11V	±12V
Short Circuit Output Current, min.	±8mA	±10mA	±8mA	±10mA
Output Impedance	40Ω	30Ω	40Ω	30Ω
PERFORMANCE				
D.C. Open Loop Gain[4]	100K V/V	150K V/V	100K V/V	150K V/V
Full Power Bandwidth[5]	125KHz	150KHz	625KHz	625KHz
Gain Bandwidth Product, G=10	18MHz	18MHz	50MHz	60MHz
Slew Rate[6]	8 V/μsec	8 V/μsec	40 V/μsec	50 V/μsec
Rise Time[6]	20 nsec	15 nsec	20 nsec	20 nsec
Settling Time,[7] **10V to 0.1%**	2.0 μsec	1.7 μsec	1.0 μsec	.85 μsec
Input Offset Voltage Drift	15 μV/c°	5 μV/c°	15 μV/c°	5 μV/c°
Power Supply Rejection Ratio[8]	86 dB	86 dB	94 dB	94 dB
POWER REQUIREMENTS				
Voltage, Rated Performance	±15VDC			
Operating Voltage Range	±5VDC to ±20VDC			
Supply Current, max.				
Suffix — 2C	8mA			
Suffix — 2M	7mA			
PHYSICAL ENVIRONMENT				
Operating Temperature Range				
Suffix — 2C	0°C to +70°C			
Suffix — 2M	−55°C to +125°C			
Storage Temperature Range	−65°C to +150°C			
Package, Hermetically Sealed	TO -99			

NOTES:

1. Derate by 6.8 mW/°C for operation at ambient temperatures above +75°C.
2. 2mV max. at full operating temperature for devices with a −2M suffix. 3.5 mV max. for devices with a −2C suffix.
3. R_L = 10KΩ.
4. Vout = ±10V, R_L =2KΩ.
5. R_L = 2KΩ.
6. G = 10 for AM-411, G = 1 for AM-410.
7. G = −10 for AM-411, G = −1 for AM-410.
8. At full operating temperature, Vsupp. = ±10VDC to ±20VDC.

TECHNICAL NOTES

1. It is recommended that these amplifiers be operated with power supply lines decoupled to ground with .01μF ceramic capacitors. Decoupling capacitors should be located as close to the amplifier power pins as possible.
2. Input offset voltage may be adjusted to zero, if required, by connecting the amplifier as shown in the external offset and bandwidth compensation diagram. The trimming potentiometer used should be 100K cermet type with a temperature coefficient less than 100 ppm/°C (available from Datel-Intersil as part no. TP-100K). It should be noted that adjustment of initial offset voltage may affect the input offset voltage drift tempco.
3. When the AM-410 or AM-411 are used to drive heavy capacitive loads (≥ 100 pF)a small value resistor should be connected in series with the output and inside the feedback loop. Resistance values of approximately 100Ω are suggested.
4. When large values of feedback resistance are used, a small capacitor in parallel with the feedback resistor will neutralize the pole introduced by the input capacitance. Capacitor values of approximately 3 pF should be sufficient to stabilize high feedback resistance configurations.
5. The AM-411 is an uncompensated operational amplifier that is stable at closed loop gains of greater than 10 without external compensation. For stable operation in a unity gain configuration a suggested compensation circuit is given.

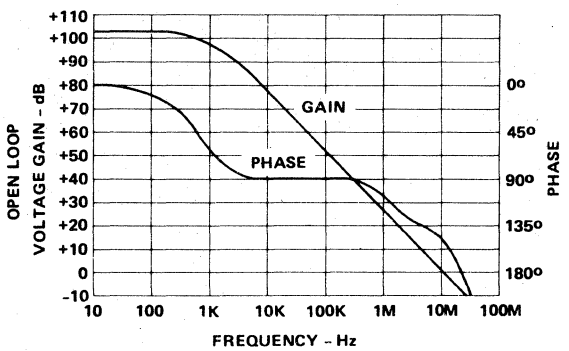
ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
AM-410-2C	0°C To +70°C
AM-410-2M	−55°C To +125°C
AM-411-2C	0°C To +70°C
AM-411-2M	−55°C To +125°C

Trimming Potentiometer: TP100K

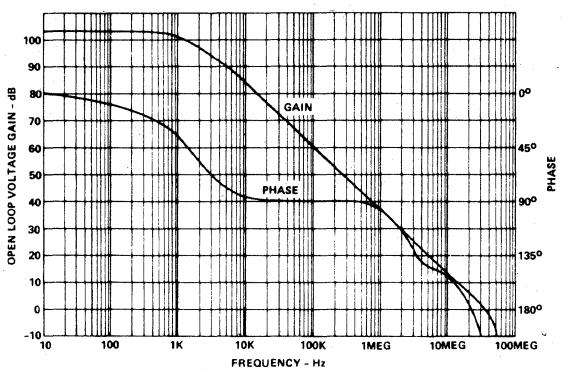
TYPICAL PERFORMANCE CURVES

OPEN LOOP FREQUENCY RESPONSE



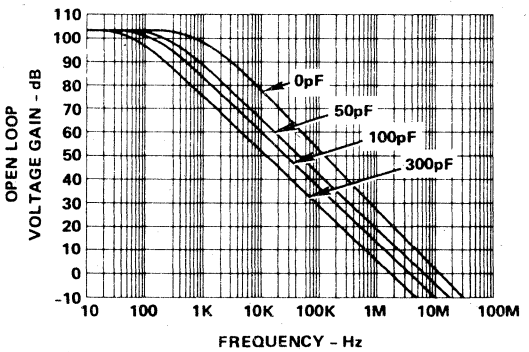
AM-410

OPEN LOOP FREQUENCY RESPONSE



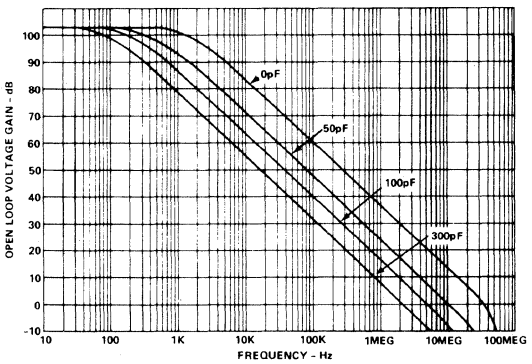
AM-411

OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS BANDWIDTH CAPACITANCES



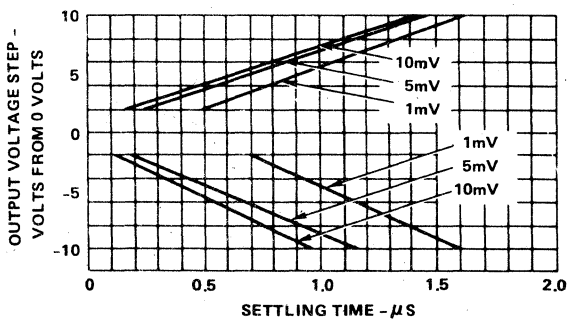
AM-410

OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS BANDWIDTH CONTROL CAPACITANCES



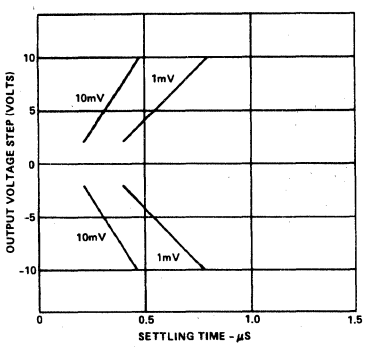
AM-411

SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



AM-410

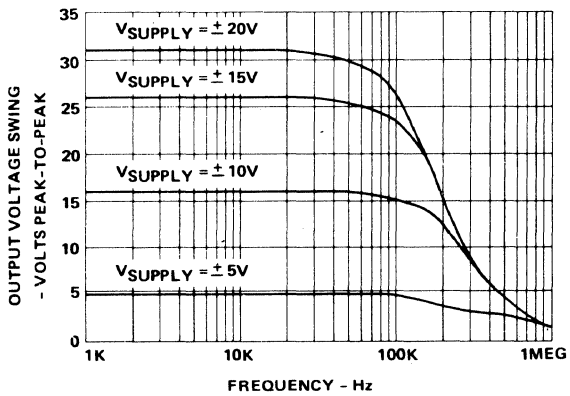
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



AM-411

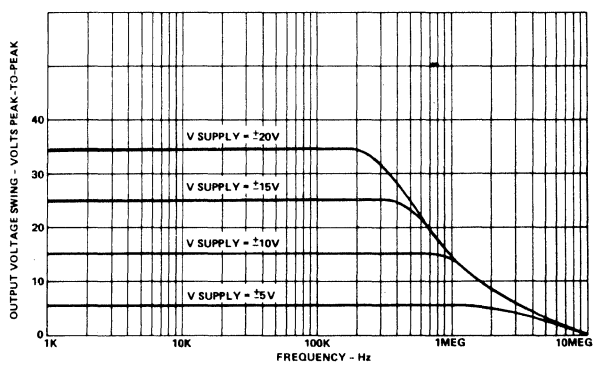
TYPICAL PERFORMANCE CURVES

OUTPUT VOLTAGE SWING VS FREQUENCY



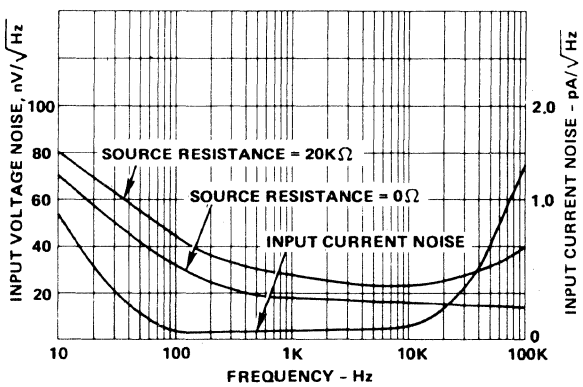
AM-410

OUTPUT VOLTAGE SWING VS FREQUENCY



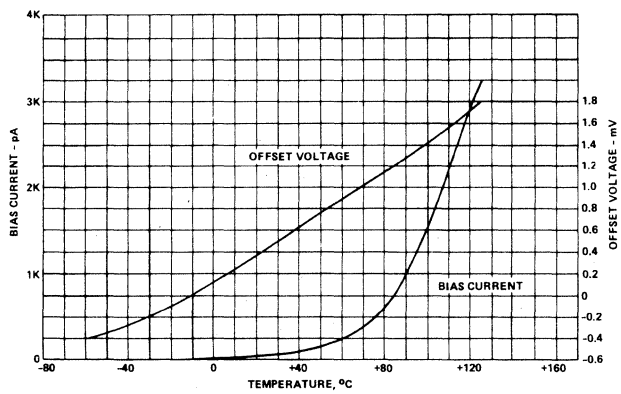
AM-411

INPUT VOLTAGE AND CURRENT NOISE VS FREQUENCY



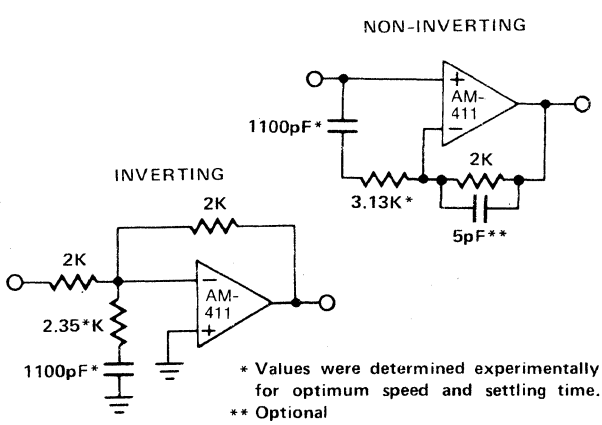
AM-410 AND AM-411

INPUT OFFSET VOLTAGE AND BIAS CURRENT VS TEMPERATURE



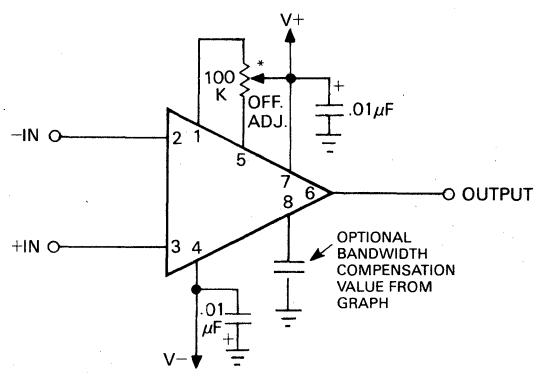
AM-410 AND AM-411

SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY ON AM-411



* Values were determined experimentally for optimum speed and settling time.
** Optional

EXTERNAL OFFSET ADJUST AND BANDWIDTH COMPENSATION FOR AM-410 AND AM-411



*AVAILABLE FROM DATEL-INTERSIL PART NO. TP100K

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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
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PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Ultra-Low Drift, Monolithic Operational Amplifier AM-414

FEATURES

- **1.3 μV/°C Max. Drift**
- **30 μV Input Offset**
- **500,000 Open Loop Gain**
- **±4 nA Max. Bias**
- **10 nV/√Hz Voltage Noise**
- **123 dB CMRR**

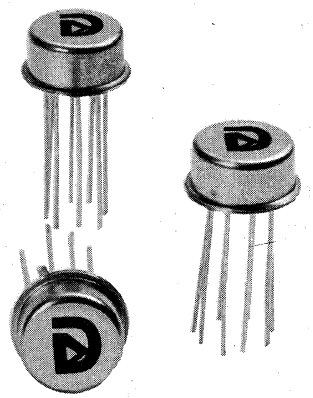
GENERAL DESCRIPTION

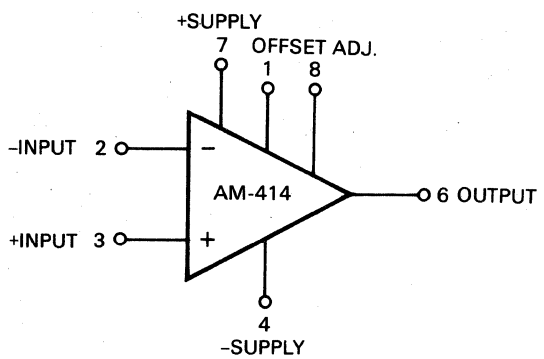
Model AM-414 is a chopperless, ultra-low drift operational amplifier fabricated with bipolar monolithic technology. It is specifically designed for accurate, low level signal amplification applications where low noise, low drift, and precise closed loop gain are required. This amplifier features 0.3 μV/°C typical input offset voltage drift with 1.3 μV/°C maximum; the drift rivals that of many chopper stabilized amplifiers costing much more.

Other significant features include 500,000 open loop voltage gain, ±4 nA maximum bias current, and 123 typical common mode rejection ratio. The input offset voltage is only ±75 μV maximum, making it unnecessary to zero the amplifiers in most applications; there is, however, provision for external zeroing for critical applications. The AM-414 also has 1.5 μV per month maximum long term drift.

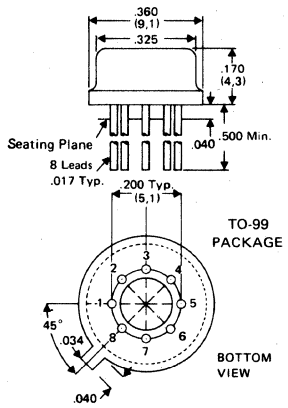
Output voltage range is ±12V minimum at ±5 mA load current with a short circuit protected output. In addition to low drift, the AM-414 also has low input noise characteristics of 10 nV/√Hz voltage noise density and 0.14 pA/√Hz current noise density. Dynamic characteristics include 600 KHz unity gain bandwidth and 0.17 V/μsec. slew rate.

There are three versions of the AM-414 of which one is a military temperature range model. The amplifiers are packaged in a hermetically sealed 8 pin TO-99 case. The AM-414 is ideal for transducer amplification, stable analog integrators, low drift active filters, and precision D/A converter output amplifiers.





MECHANICAL DIMENSIONS INCHES (MM)



NOTE: All leads gold plated KOVAR

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	OFFSET TRIM
2	− INPUT
3	+ INPUT
4	− SUPPLY VOLTAGE
5	NO CONNECTION
6	OUTPUT
7	+ SUPPLY VOLTAGE
8	OFFSET TRIM

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, AM-414

Typical at 25°C, ±15V supply, unless otherwise noted

	A	B	M
MAXIMUM RATINGS			
Power Supply Voltage		±22V	
Differential Input Voltage		±30V	
Common Mode Input Voltage		±Vs	
INPUT CHARACTERISTICS			
Common Mode Voltage Range		±13V min	
Input Resistance, comm. mode, MΩ	33	50	60
Input Resistance, diff. mode, GΩ	120	160	200
Input Offset Voltage, μV typ.	60	30	30
Input Offset Voltage, μV max.	150	75	75
Input Bias Current, nA max.	±7	±4	±3
Input Offset Current, nA max.	±6	±3.8	±2.8
OUTPUT CHARACTERISTICS			
Output Voltage, 2K load, min.	±11.5V	±12V	±12V
Output Current., S.C. protected, max.		±10 mA	
Output Resistance, open loop		60 ohms	
PERFORMANCE			
DC Open Loop Gain[1], V/V, 2K load	400K	500K	500K
Input Offset Voltage Drift[2], μV/°C typ.	0.5	0.3	0.3
Input Offset Voltage Drift[2], μV/°C max.	2.0	1.3	1.3
Input Bias Current Drift, pA/°C max.	50	35	50
Input Offset Current Drift, pA/°C max.	50	35	50
Long Term Stability, μV/mo. max	2.0	1.5	1.0
Common Mode Rej. Ratio, dB min.	100	106	110
Input Noise Voltage, 0.1 to 10 Hz		0.4 μV P-P	
Input Noise Voltage Density, 1 KHz		10 nV/√Hz	
Input Noise Current, 0.1 to 10 Hz		15 pA P-P	
Input Noise Current Density, 1KHz		0.13 pA/√Hz	
Power Supply Rejection Ratio, dB min.	90	94	100
DYNAMIC CHARACTERISTICS			
Unity Gain Bandwidth		600 KHz	
Slew Rate		0.17 V/μsec.	
POWER REQUIREMENT			
Voltage, rated performance		±15 VDC	
Voltage, operating		±3 VDC to ±18 VDC	
Quiescent Current, ±15V supply		5 mA max.	
PHYSICAL-ENVIRONMENTAL			
Operating Temp. Range, AM-414A, B		0°C to 70°C	
Operating Temp. Range, AM-414M		−55°C to +125°C	
Storage Temp. Range		−65°C to +150°C	
Package, hermetically sealed		TO-99	

NOTES: 1. Minimum gains are 120K, 200K, and 200K respectively
2. With or without external zeroing of offset

ORDERING INFORMATION

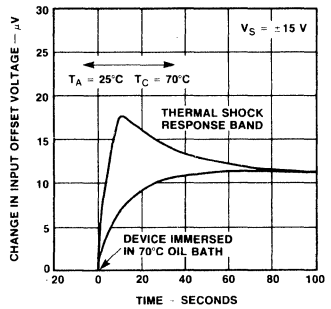
MODEL	INPUT OFFSET VOLTAGE DRIFT
AM-414A	2.0 μV/°C max.
AM-414B	1.3 μV/°C max.
AM-414M	1.3 μV/°C max.

Trimming Potentiometer, TP20K

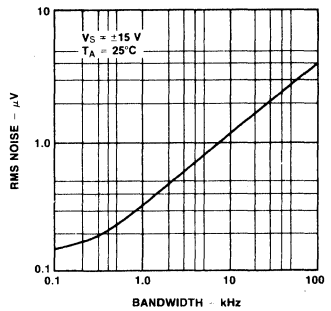
THESE AMPLIFIERS ARE COVERED BY GSA CONTRACT

PERFORMANCE

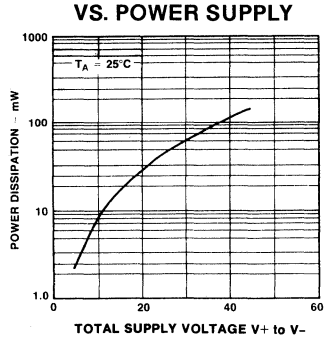
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



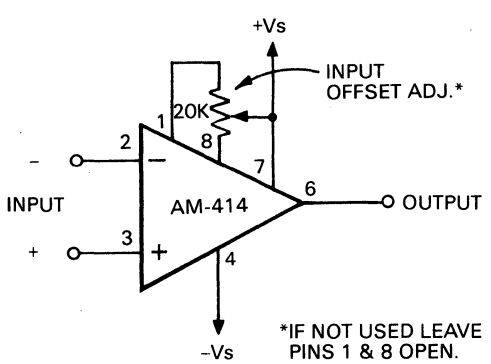
INPUT WIDEBAND NOISE VS. BANDWIDTH (0.1 Hz TO FREQUENCY INDICATED)



POWER CONSUMPTION VS. POWER SUPPLY



CONNECTION DIAGRAM



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PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Wide Bandwidth, Fast Settling Monolithic Operational Amplifiers AM-450 & AM-460 Series

FEATURES

- **120V/μsec. Slew Rate**
- **100 MHz Gain Bandwidth**
- **200 nsec. Settling to 0.1%**
- **300 Meg. Input Impedance**
- **Bipolar Differential Inputs**
- **5 nA Input Offset Current**

GENERAL DESCRIPTION

Datel-Intersil's AM-450 and AM-460 series bipolar input op amps provide a wide spectrum of capabilities required for high-speed, wide bandwidth signal processing applications. Features available within these two high-performance families include a 100 MHz gain-bandwidth product (AM-462), a 120V/μsec slew rate (AM-452), 300 Meg input impedance (AM-460 and AM-462) and 200 nsec settling time to 0.1% of full scale (AM-452).

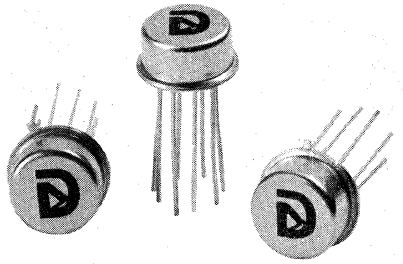
All models provide a full ±10V output at 10 mA and may be operated in non-inverting as well as inverting modes. Other features common to these units are low input offset currents and low input offset voltages as well as common mode rejection ratios typically greater than 90 dB.

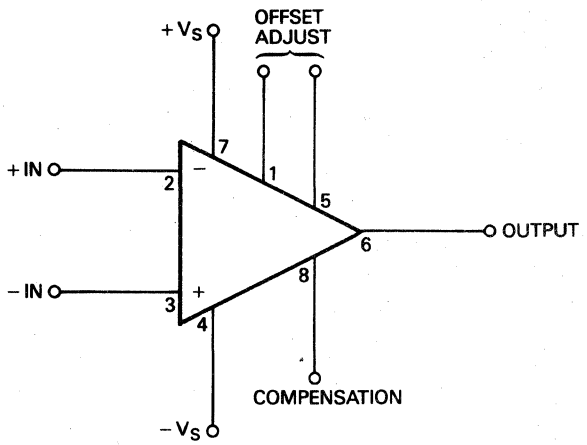
The AM-460 devices are bipolar operational amplifiers with very high impedance differential inputs, making them particularly well suited to applications as high speed comparators, wideband active filters and low distortion oscillators.

Both AM-450 and the AM-460 series units find many applications as fast acquisition sample and hold amplifiers, D/A output amplifiers, A/D input buffer amplifiers, pulse amplifiers, and fast integrators.

The AM-462-1 and AM-462-1M are packaged in a 14 pin ceramic DIP. All other models are packaged in an 8 lead, hermetically sealed TO-99 package with standard pin out, allowing them to be used easily as pin for pin replacements for general purpose IC operational amplifiers.

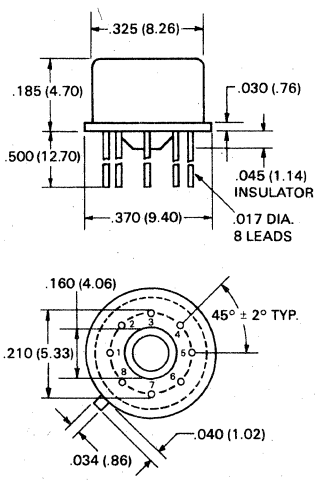
All models are available in 0°C to +70C operating temperature range or in -55°C to +125°C for suffix M models.



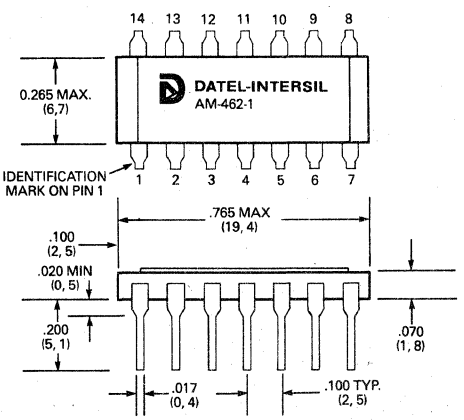


MECHANICAL DIMENSIONS INCHES (MM)

TO-99



14-PIN DUAL INLINE CERAMIC PACKAGE MODEL AM-462-1 AND AM-462-1M



DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, AM-450 AND AM-460 SERIES
(Typical @ +25°C, ±15 VDC Supplies, R_L + 2K, Unless Otherwise Noted)

	AM-450	AM-452	AM-460	AM-462
MAXIMUM RATINGS				
Power Supply Voltage	±20V	±20V	±22.5V	±22.5V
Differential Input Voltage	±15V	±15V	±12V	±12V
Peak Output Current	50 mA	50 mA	S.C. Prot.	S.C. Prot.
INPUT CHARACTERISTICS				
Common Mode Voltage Range[1], min.	±10V	±10V	±11V	±11V
Input Resistance	50 Meg	100 Meg	300 Meg	300 Meg
Input Resistance, min.	20 Meg	20 Meg	40 Meg	40 Meg
Input Offset Voltage	±4 mV	±5 mV	±3 mV	±3 mV
Input Offset Current, typ.	20 nA	20 nA	5 nA	5 nA
max.	50 nA	50 nA	25 nA	25 nA
Input Bias Current, typ.	125 nA	125 nA	5 nA[6]	5 nA
max.	250 nA	250 nA	25 nA	25 nA
OUTPUT CHARACTERISTICS				
Output Voltage, min.	±10V	±10V	±10V	±10V
Output Current, min.[7]	±10 mA	±10 mA	±10 mA	±10 mA
PERFORMANCE				
DC Open Loop Gain[2]	25K V/V	15K V/V	150K V/V	150K V/V
Full Power Bandwidth[2]	500 KHz	1600 KHz	75 KHz	600 KHz
Gain Bandwidth Product	12 MHz	20 MHz	12 MHz	100 MHz
Slew Rate	30V/μsec	120V/μsec	7V/μsec	35V/μsec
Settling Time, 10V to 0.1%	330 nsec[3]	200 nsec[3]	1.5μsec[4]	1.0 μsec
Common Mode Rejection Ratio[5], typ.	90 dB	90 dB	100 dB	100 dB
max.	74 dB	74dB	74 dB	74 dB
Input Offset Voltage Drift	20 μV/°C	30 μV/°C	10 μV/°C	15 μV/°C
External Compensation Required	None	Gains <3	Gains <3	Gains <5
Power Supply Rejection Ratio	90 dB	90 dB	90 dB	90 dB
POWER REQUIREMENTS				
Voltage, Rated Performance	±15 VDC	±15 VDC	±15 VDC	±15 VDC
Operating Voltage Range, min.	±10V	±10V	±5V	±5V
max.	±20V	±20V	±22.5V	±22.5V
Supply Current, max.	6 mA	6 mA	4 mA	4 mA

PHYSICAL-ENVIRONMENTAL	
Oper. Temp. Range, -1 & -2 Models	0°C to +70°C
-1M & -2M Models	-55°C to +125°C
Storage Temp. Range	-65°C to +150°C
Package Type, -2 & -2M Models	TO-99
-1 & -1M Models	14 Pin Ceramic DIP

NOTES:
1. At Full Temperature
2. V_{OUT} = ±10V
3. C_L 50 pF
4. C_L = 100 pF
5. For ±5V Common Mode Range
6. 15nA typ. for AM-460-2M only
7. AM-460 and AM-462 outputs are short circuit protected

ORDERING INFORMATION

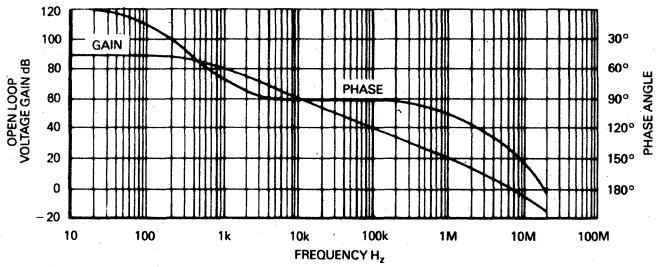
MODEL	OPERATING TEMP. RANGE
AM-450-2	0°C to +70°C
AM-450-2M	-55°C to +125°C
AM-452-2	0°C to +70°C
AM-452-2M	-55° to +125°C
AM-460-2	0°C to +70°C
AM-460-2M	-55° to +125°C
AM-462-1, 2	0°C to +70°C
AM-462-1M, 2M	-55° to +125°C

Trimming Potentiometers: TP100K, TP20K

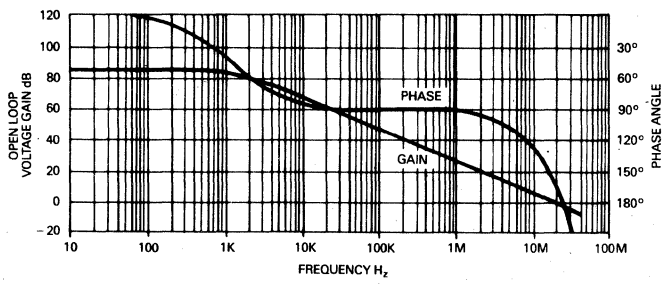
THESE AMPLIFIERS ARE COVERED BY GSA CONTRACT

TYPICAL OPEN LOOP FREQUENCY AND PHASE RESPONSE

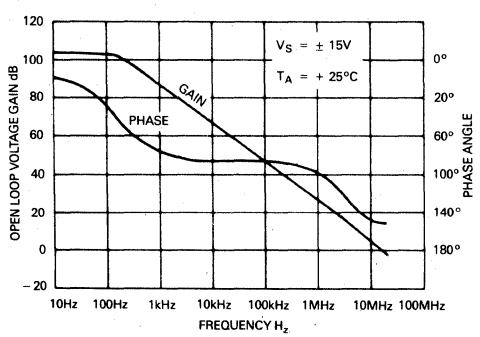
AM-450



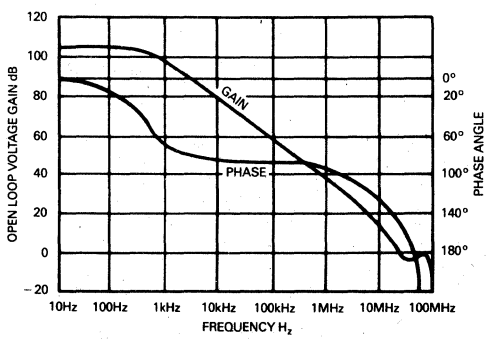
AM-452



AM-460



AM-462



CONNECTIONS

INPUT/OUTPUT CONNECTIONS

ALL -2 AND -2M MODELS

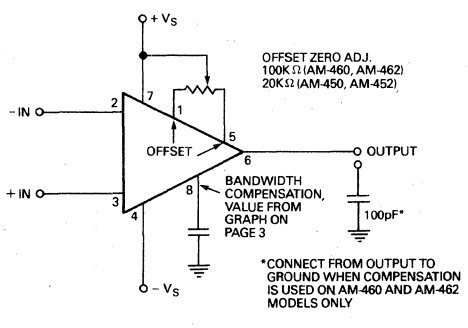
PIN	FUNCTION
1	OFFSET ADJUST
2	-INPUT
3	+INPUT
4	-Vs
5	OFFSET ADJUST
6	OUTPUT
7	+Vs
8	BANDWIDTH CONTROL
CASE IS CONNECTED TO -SUPPLY	

AM-462-1 AND AM-462-1M ONLY

PIN	FUNCTION
3	OFFSET ADJUST
4	-INPUT
5	+INPUT
6	-Vs
9	OFFSET ADJUST
10	OUTPUT
11	+Vs
14	BANDWIDTH CONTROL
ALL OTHER PINS ARE NO CONNECTION. CASE IS CONNECTED TO -SUPPLY	

EXTERNAL OFFSET ADJUSTMENT AND BANDWIDTH COMPENSATION (ALL MODELS)

EXTERNAL OFFSET ADJUSTMENT AND BANDWIDTH COMPENSATION (ALL MODELS)



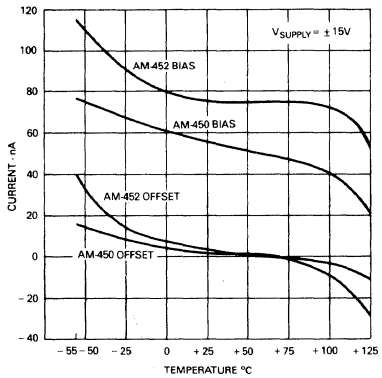
*CONNECT FROM OUTPUT TO GROUND WHEN COMPENSATION IS USED ON AM-460 AND AM-462 MODELS ONLY

NOTE: PINS SHOWN FOR TO-99 CASE

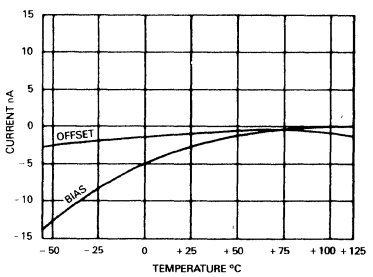
TYPICAL PERFORMANCE CURVES

INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE

AM-450 AND AM-452

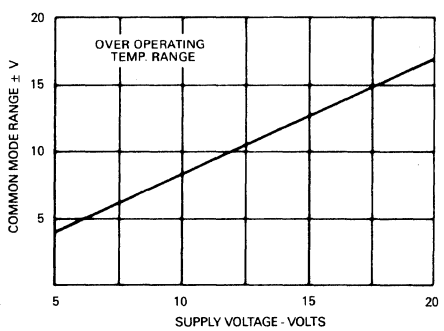


AM-460 AND AM-462



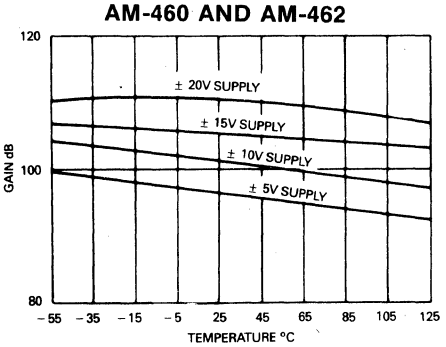
COMMON MODE VOLTAGE RANGE Vs SUPPLY VOLTAGE

AM-460 AND AM-462



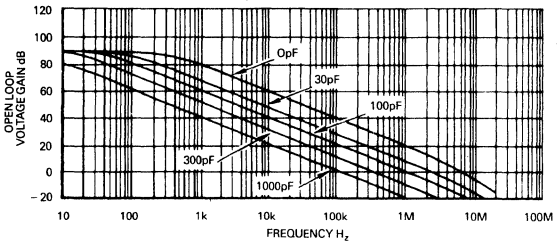
OPEN LOOP VOLTAGE GAIN Vs TEMPERATURE

AM-460 AND AM-462



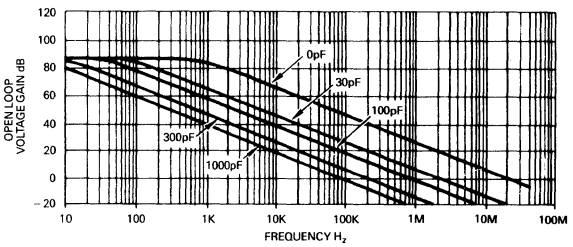
OPEN LOOP FREQUENCY RESPONSE AND EXTERNAL BANDWIDTH COMPENSATION

AM-450



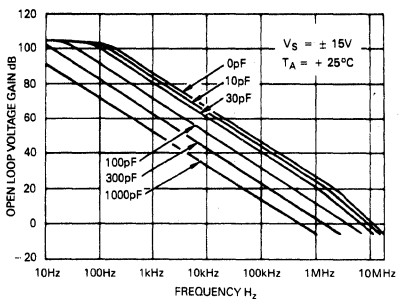
NOTE: EXTERNAL COMPENSATION COMPONENTS ARE NOT REQUIRED FOR STABILITY, BUT MAY BE ADDED TO REDUCE BANDWIDTH IF DESIRED.

AM-452



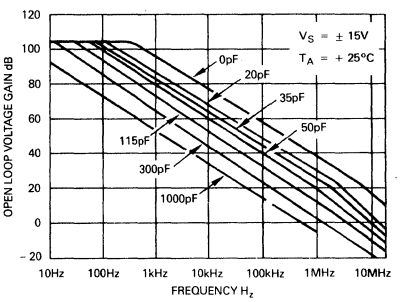
NOTE: EXTERNAL COMPENSATION IS REQUIRED FOR CLOSED LOOP GAIN <3.

AM-460



NOTE: EXTERNAL COMPENSATION COMPONENTS ARE NOT REQUIRED FOR STABILITY, BUT MAY BE ADDED TO REDUCE BANDWIDTH IF DESIRED. IF EXTERNAL COMPENSATION IS USED, ALSO CONNECT 100pF CAPACITOR FROM OUTPUT TO GROUND.

AM-462



NOTE: EXTERNAL COMPENSATION IS REQUIRED FOR CLOSED LOOP GAIN <5. IF EXTERNAL COMPENSATION IS USED, ALSO CONNECT 100pF CAPACITOR FROM OUTPUT TO GROUND.

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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Low Noise, Wideband Monolithic OP AMP Model AM-453-2

FEATURES

- **4 nV/√Hz Wideband Noise Voltage**
- **0.6 pA/√Hz Wideband Noise Current**
- **13V/μsec. Slew Rate**
- **20 mA Output Current**
- **±3V to ±20V Supply Range**

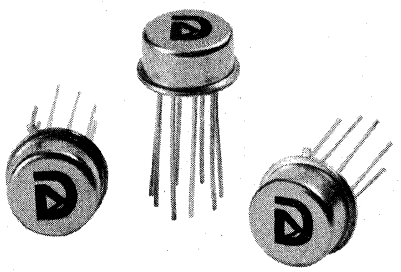
GENERAL DESCRIPTION

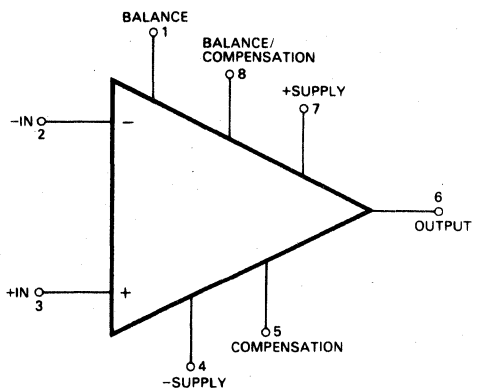
The AM-453-2 is a high performance, low noise monolithic operational amplifier. It offers better noise characteristics, improved output drive capability and extended small signal and power bandwidths when compared with standard operational amplifiers.

Typical input noise voltage is less than 7nV/ √Hz at 30Hz and drops to 4 nV/ √Hz for frequencies greater than 200 Hz. Input noise current is typically 2.5 pA/ √Hz at 30 Hz falling to only 0.6 pA/ √Hz for frequencies above 1 KHz. Along with low noise performance, the AM-453-2 has a gain bandwidth product of 10 MHz and a full power frequency response that typically extends to 200 KHz for an output swing of ±10V. In addition, the amplifier has the capability to drive 600Ω at 10V (RMS) when supplied by ±18V. The AM-453-2 is internally compensated for a gain of three or greater while frequency response may be optimized for various applications by the addition of an external compensation capacitor. Other features include a minimum common mode rejection ratio of 80 dB, 13V/μsec. slew rate, input overvoltage protection by diodes and a large supply voltage range extending from ±3V to ±20V.

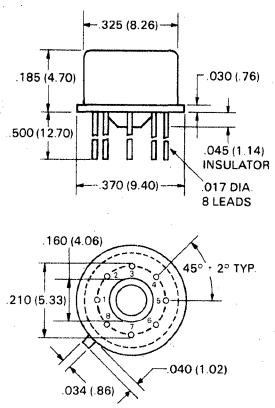
Its low noise, wideband, extended output characteristics make the AM-453-2 exceptionally well-suited to applications in instrumentation and control circuits, data acquisition circuits, wideband transducer amplification and audio frequency analog signal processing including active filters.

Packaged in an 8 lead hermetically sealed TO-99 case, the AM-453-2 is available in two operating temperature ranges, 0°C to 70°C or -55°C to +125°C.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	BALANCE
2	-INPUT
3	+INPUT
4	-SUPPLY
5	COMPENSATION
6	OUTPUT
7	+SUPPLY
8	BAL./COMP.

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS — AM-453-2
Typical at 25°C, ±15V Supply unless otherwise noted

MAXIMUM RATINGS

Maximum Supply Voltage	±22V
Max. Common Mode Voltage Range	±V Supply
Maximum Differential Input Voltage[1]	±0.5V
Maximum Power Dissipation	680 mW

INPUT CHARACTERISTICS

Input Offset Voltage	0.5 mV typ., 4 mV max.
Input Offset Current	20 nA typ., 300 nA max.
Input Bias Current	500 nA typ., 1.5 μA max.
Input Resistance	100 KΩ
Common Mode Voltage Range	±12V min.

OUTPUT CHARACTERISTICS

Output Voltage	±12V min.
Output Current, S.C. Protected	±20 mA
Output Resistance	0.3Ω

PERFORMANCE

Input Offset Voltage Drift[2]	30μV/°C
Input Noise Voltage, 30 Hz	7 nV/$\sqrt{Hz}$
Input Noise Voltage, 200 Hz – 100 KHz	4 nV/$\sqrt{Hz}$
Input Noise Current, 30 Hz	2.5 pA/$\sqrt{Hz}$
Input Noise Current, 1 KHz – 100 KHz	0.6 pA/$\sqrt{Hz}$
Common Mode Rejection Ratio	100 dB typ. 80 dB min.
Power Supply Sensitivity	10 μV/V
D.C. Open Loop Gain	100,000 V/V
Full Power Frequency, ±10V Output	200 KHz
Unity Gain Bandwidth	10 MHz
Slew Rate	13V/μs

POWER REQUIREMENTS

Supply Voltage Rated Performance	±15V
Supply Voltage Range	±3V to ±20V
Supply Current	4 mA typ., 8 mA max.

PHYSICAL ENVIRONMENTAL

Operating Temperature Range	
AM-453-C	0°C to +70°C
AM-453-M	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Package, Hermetically Sealed	TO-99

NOTES:

1. Since the inputs are protected against overvoltage by diodes differential input exceeding 0.6V will cause large current flows unless current limiting resistors are used. Maximum current should be limited to ±10 mA.
2. 30μV/°C typical for C models only, 30μV/°C maximum for M models.

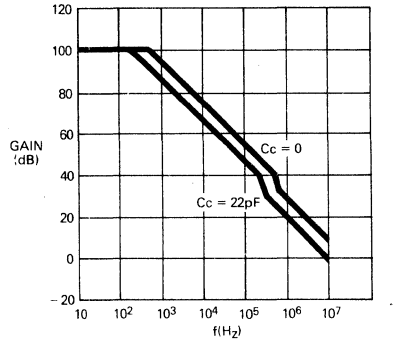
ORDERING INFORMATION

	OPERATING TEMP. RANGE
AM-453-2C	0°C to +70°C
AM-453-2M	-55°C to +125°C
Trimming Pot TP 100K	Cermet, 100 ppm/°C

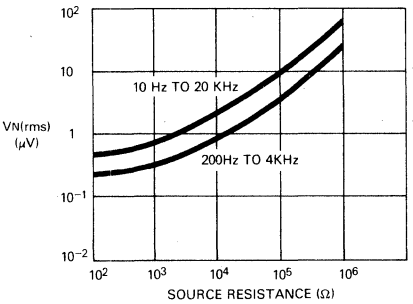
THE AM-453 AMPLIFIERS ARE COVERED BY GSA CONTRACT

TYPICAL PERFORMANCE

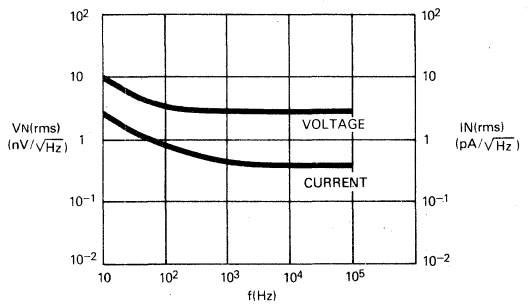
OPEN LOOP FREQUENCY RESPONSE



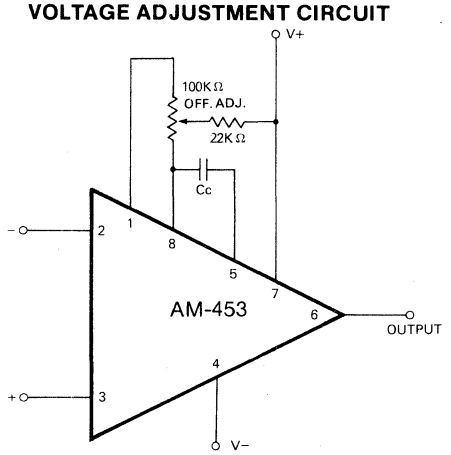
BROADBAND INPUT NOISE VOLTAGE



INPUT NOISE VOLTAGE AND CURRENT VS. FREQUENCY



FREQUENCY COMPENSATION AND OFFSET VOLTAGE ADJUSTMENT CIRCUIT



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• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

High Voltage, Monolithic Operational Amplifier Model AM-464-2

FEATURES

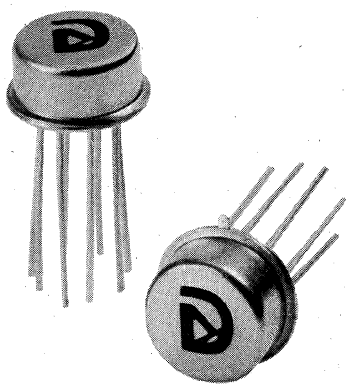
- ±35V Output Swing
- ±10V to ±40V Supply
- 4 MHz Gain Bandwidth
- 5V/μsec. Slew Rate
- 74 dB min. CMRR

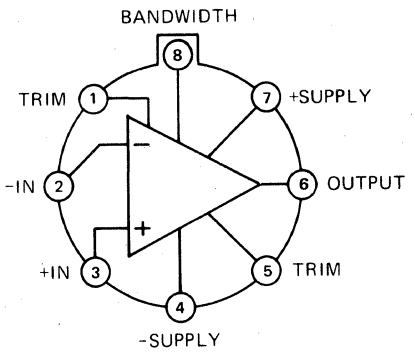
GENERAL DESCRIPTION

The AM-464-2 is a monolithic IC operational amplifier with an input common mode voltage range of ±35V and an output voltage swing of ±35V when operated from a ±40 supply. Along with high voltage performance this amplifier has a 4 MHz gain bandwidth product and a 5V/μsec. output slew rate. It is particularly useful in data conversion circuits and other signal processing applications where higher than normal common mode voltage and output voltage swings are required. The AM-464-2 is internally compensated for all gains and has an on-chip temperature sensing, output current-limiting circuit for absolute output short-circuit protection.

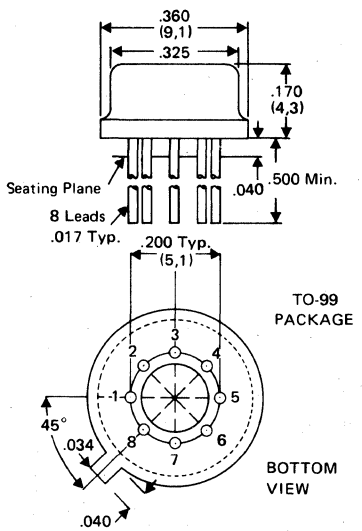
Other features of this amplifier include: common mode rejection of 74 dB minimum, input bias current of 30nA maximum, and open loop voltage gain of 100,000 minimum. The output slew rate of 5 volts per microsecond gives a 70 volt peak to peak sinusoidal output voltage at up to 23 kHz. The power supply voltage can range from ±10V to ±40 VDC to give output swings from ±5V to ±35V. Power supply quiescent current is only 3.2mA typical.

The AM-464-2 is packaged in an 8 lead, hermetically sealed TO-99 case and may be used as a pin for pin replacement for general purpose IC operational amplifiers such as 741, 101, and 108 for higher voltage applications. Operating temperature range is 0°C to 70°C for the AM-464-2 and −55°C to +125°C for the AM-464-2M.





MECHANICAL DIMENSIONS
INCHES (MM)



NOTE: All leads gold plated KOVAR

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	TRIM
2	−IN
3	+IN
4	−SUPPLY
5	TRIM
6	OUTPUT
7	+SUPPLY
8	BANDWIDTH (C_B)

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, AM-464-2
(Typical at 25°C, ±40V Supply, unless otherwise noted)

MAXIMUM RATINGS
- **Input Overvoltage** ..... ±37V max.
- **Supply Voltage** ..... ±50V max.
- **Internal Power Dissipation** ..... 680 mW

INPUT CHARACTERISTICS
- **Common Mode Voltage Range** ..... ±35V min.
- **Input Impedance, AM-464-2** ..... 200 Meg.Ω
- **AM-464-2M** ..... 250 Meg.Ω
- **Input Offset Voltage, AM-464-2** ..... ±6 mV max.
- **AM-464-2M** ..... ±4 mV max.
- **Input Bias Current, AM-464-2** ..... 30 nA max.
- **AM-464-2M** ..... 25 nA max.
- **Input Offset Current, AM-464-2** ..... 30 nA max.
- **AM-464-2M** ..... 12 nA max.

OUTPUT CHARACTERISTICS
- **Output Voltage** ..... ±35V min.
- **Output Current[1], AM-464-2** ..... ±10 mA min.
- **AM-464-2M** ..... ±12 mA min.
- **Output Resistance** ..... 500 Ohms
- **Stable Capacitive Load** ..... 100 pF

PERFORMANCE
- **DC Gain, 5 KΩ Load** ..... 100K V/V min.
- **Common Mode Rejection[2], AM-464-2** ..... 74 dB min.
- **AM-464-2M** ..... 80 dB min.
- **Input Offset Voltage Drift** ..... 15μV/°C
- **Input Offset Current[3], AM-464-2** ..... 50 nA max.
- **AM-464-2M** ..... 35 nA max.
- **Input Noise Voltage, 10 Hz-10 KHz** ..... 3 μV RMS

DYNAMIC CHARACTERISTICS
- **Unity Gain Bandwidth** ..... 4 MHz
- **Slew Rate** ..... 5V/μsec.
- **Full Power Frequency, 70V p-p** ..... 23 KHz

POWER REQUIREMENT
- **Voltage, Rated Performance** ..... ±40 VDC
- **Power Supply Voltage Range** ..... ±10 to ±40 VDC
- **Quiescent Current, AM-464-2** ..... 4.5 mA max.
- **AM-464-2M** ..... 3.8 mA max.

PHYSICAL ENVIRONMENTAL
- **Operating Temperature Range, AM-464-2** ..... 0°C to +70°C
- **AM-464-2M** ..... −55°C to +125°C
- **Storage Temperature Range** ..... −65°C to +150°C
- **Package, Hermetically Sealed** TO-99

NOTES:
1. Overload protected by current limiting and temperature sensing.
2. For common mode voltage = ±30V.
3. At maximum operating temperature.

ORDERING INFORMATION

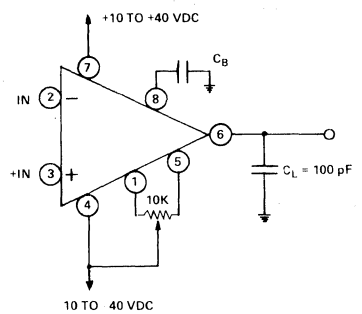
MODEL	OPER. TEMP RANGE
AM-464-2	0°C to +70°C
AM-464-2M	−55°C to +125°C

Trimming Potentiometer: **TP 10K**

THESE AMPLIFIERS ARE COVERED BY GSA CONTRACT

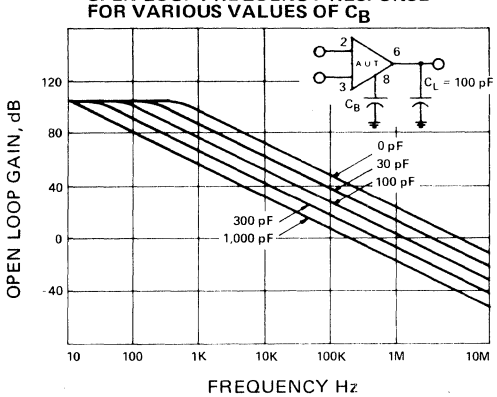
PERFORMANCE PARAMETERS

OFFSET TRIMMING AND BANDWIDTH REDUCTION

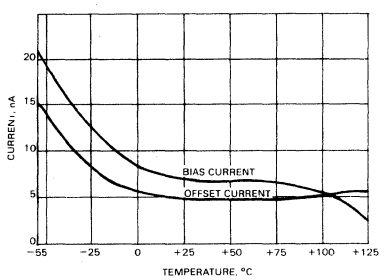


NOTES:
C_B is not required for stability since amplifier is internally compensated. It may be used to reduce bandwidth, however. C_L = 100 pF may be required for stability if external C_B is used.

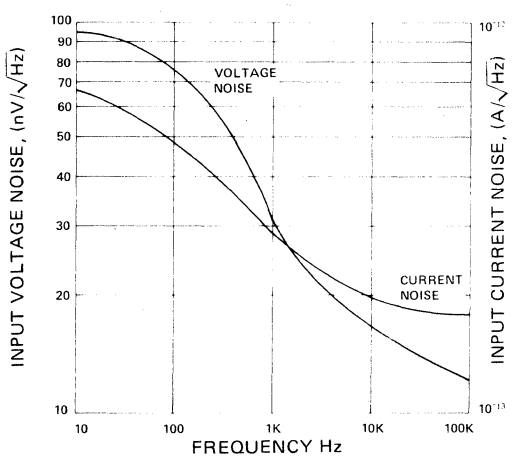
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF C_B



INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



INPUT NOISE CHARACTERISTICS



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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
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PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Fast, Low Power Monolithic Operational Amplifier Model AM-470-2

FEATURES

- **150 μA max. Quiescent Current**
- **20V/μsec. Slew Rate**
- **106 dB CMRR**
- **Internally Compensated**
- **±12V Output at ±10 mA**
- **±5.5V to ±20V Supply**

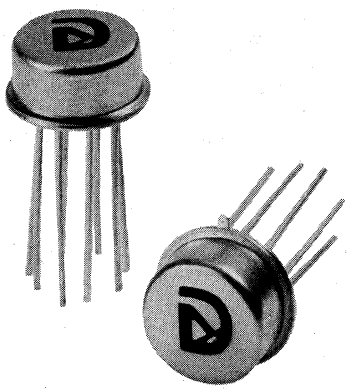
GENERAL DESCRIPTION

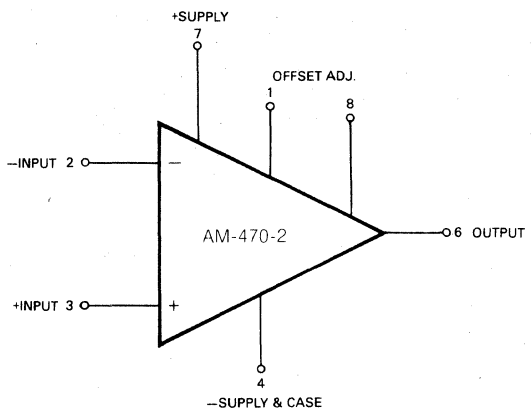
Model AM-470-2 is a high performance monolithic operational amplifier which features fast response and excellent DC characteristics while drawing only 75 μA quiescent operating current. This internally compensated amplifier, employing dielectric isolation, has a gain-bandwidth product of 1 MHz and an output slew rate of 20V/μsec., making it an ideal choice for low power data acquisition systems. While its quiescent operating current is very low, it nevertheless has a ±12 volt output drive capability at ±10 milliamperes; the output stage is also short circuit protected.

The AM-470-2 exhibits superior DC input characteristics. Input bias current is typically 5 nA and input offset voltage is typically ±1 mV; input offset voltage drift is ±5 μV/°C typical. The common mode input voltage range is ±11V minimum and common mode rejection ratio is 106 dB. DC open loop gain is 300,000, resulting in low summing junction error voltages. Power supply rejection ratio is 100 dB.

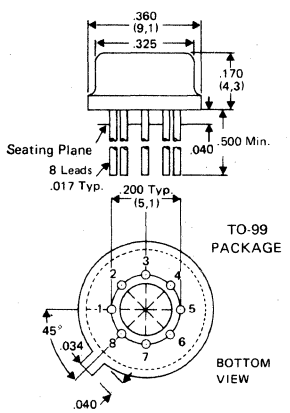
This amplifier can be operated over a wide power supply range: ±5.5V to ±20V. Two basic versions are available, the AM-470-2C for 0 to 70C operation, and the AM-470-2M for -55 to +125C operation.

Typical applications include transducer amplifiers, portable and remote instrumentation systems, battery operated data logging systems, data acquisition systems, instrumentation amplifiers, and active filters.





MECHANICAL DIMENSIONS INCHES (MM)



NOTE: All leads gold plated KOVAR

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	OFFSET ADJ.
2	–INPUT
3	+INPUT
4	–SUPPLY & CASE
5	N.C.
6	OUTPUT
7	+SUPPLY
8	OFFSET ADJ.

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, AM-470-2
Typical at 25°C, ±15V supply unless otherwise noted

MAXIMUM RATINGS

Power Supply Voltage	±22V
Differential Input Voltage	±18V
Package Dissipation	300 mW

INPUT CHARACTERISTICS

Common Mode Voltage Range	±11V min.
Input Offset Voltage[1]	±1 mV typ., ±5 mV max.
Input Bias Current[2]	5 nA typ., 40 nA max.
Input Offset Current[3]	2.5 nA typ., 15 nA max.

OUTPUT CHARACTERISTICS

Output Voltage	±12V min.
Output Current, S.C. Protected	±10 mA min.

PERFORMANCE

DC Open Loop Gain[4]	300,000 V/V
Common Mode Rejection Ratio[5]	106 dB typ., 80 dB min.
Input Offset Voltage Drift	±5 μV/°C
Gain Bandwidth Product[4]	1.0 MHz
Slew Rate	20V/μsec.
Input Offset Current over Temp.	40 nA max.
Power Supply Rejection Ratio	100 dB

POWER REQUIREMENT

Voltage, Rated Performance	±15V
Voltage Range, Operating	±5.5 to ±20V
Quiescent Current	75 μA typ., 150 μA max.

PHYSICAL-ENVIRONMENTAL

Operating Temperature Range	0 to 70C (AM-470-2C)
Mil-Version Temp. Range	-55 to +125C (AM-470-2M)
Storage Temperature Range	-65 to +150C
Package, Hermetically Sealed	TO-99

NOTES

1. ±3 mV max. for AM-470-2M
2. 20 nA max. for AM-470-2M
3. 10 nA max. for AM-470-2M
4. With 2K load in parallel with 100 pF
5. For ±5V common mode voltage

ORDERING INFORMATION

Model

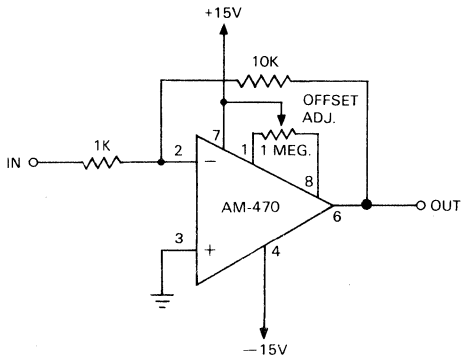
AM-470-2C

AM-470-2M

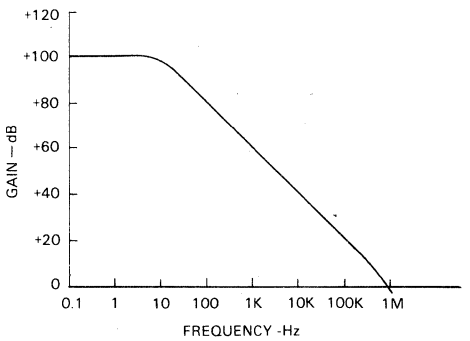
THESE AMPLIFIERS ARE COVERED BY GSA CONTRACT

PERFORMANCE GRAPHS

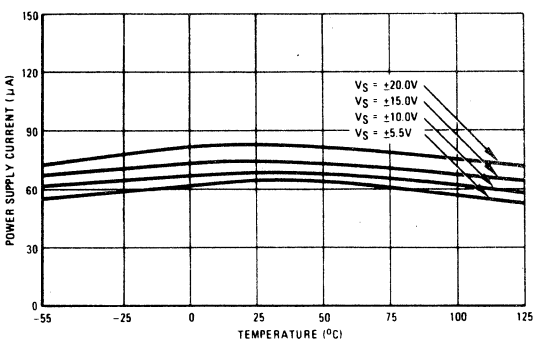
CONNECTION FOR INVERTING GAIN OF 10



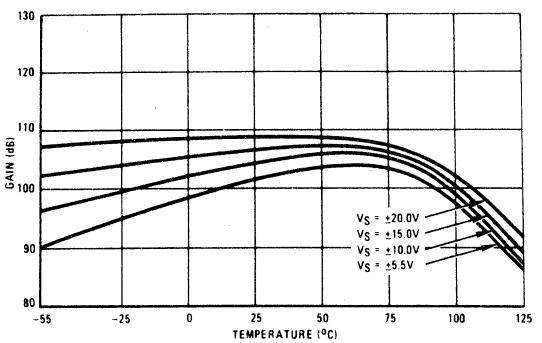
OPEN LOOP GAIN VS. FREQUENCY



POWER SUPPLY VS. TEMP. & SUPPLY VOLTAGE



OPEN LOOP GAIN VS. TEMP. & SUPPLY VOLTAGE



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PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Chopper Stabilized Operational Amplifier Model AM-490-2

FEATURES

- **Differential Inputs**
- **120 dB CMR**
- **Drift to 0.1μV/°C max.**
- **5 x 10^8 Open Loop Gain**
- **20μV Input Offset Voltage**
- **200 msec. Warm-Up**

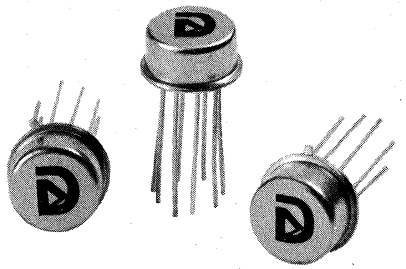
GENERAL DESCRIPTION

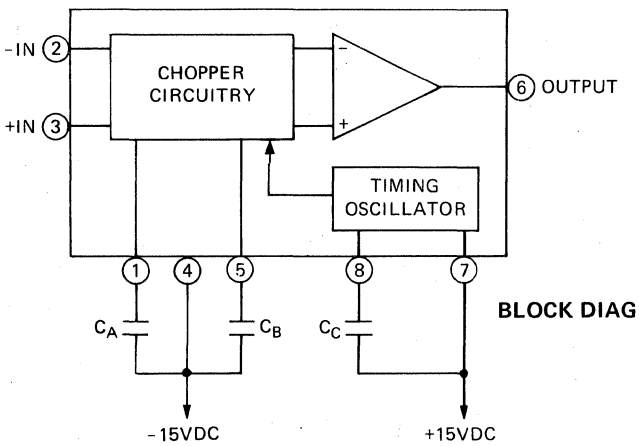
Model AM-490-2 is a monolithic, chopper stabilized operational amplifier with differential inputs; it is specifically designed for applications requiring ultra-stable DC characteristics together with good bandwidth. This device is available in three different grades of maximum input offset voltage drift: 1.0, 0.3, and 0.1μV/°C. The extremely low input offset voltage drift and initial input offset voltage of only 20μV eliminate the requirement for zero adjustment in most applications. Other important input characteristics include an input impedance of 100 megohms, input bias current of 150pA, and input offset current drift of 1pA/°C. This permits the AM-490-2 to operate accurately with source impedances over 100 kilohms. A common mode rejection of 120 dB minimum and open loop gain of 5 x 10^8 result in extremely low output errors. Long term stability is typically 5μV per year.

The circuit of the AM-490-2 utilizes a complex monolithic chip 93 x 123 mils with 256 active devices. Both bipolar and N channel MOS FET's are used to implement the linear and switching portions of the circuitry. The chopper circuitry utilizes two DC coupled sample-hold circuits driven by a multivibrator circuit. The DC coupling, contrasted with AC coupling commonly used in chopper amplifiers, results in fast overload recovery. Three external capacitors are required for the sample-hold circuits and the multivibrator which generates a 750 Hz chopping square wave.

Other specifications of the AM-490-2 include ±10V input common mode range and ±10V output at 7mA which is short circuit protected. The operating power supply range is ±12V to ±20VDC with a constant quiescent current drain of 3.5mA typical over this range. Power supply rejection is 120 dB. The low power drain and fast warm-up time of 200 msec. make this device ideal for use in battery operated, interrupted service circuits. Other applications include inverting, noninverting, and balanced gain amplifier configurations in addition to very accurate integrators and sample-holds. The AM-490-2 is packaged in a hermetically sealed, 8 pin TO-99 case.

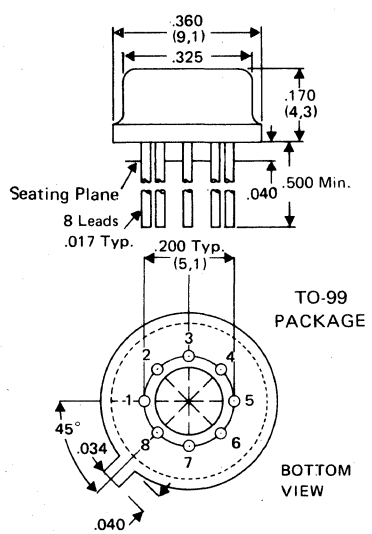
CAUTION: The AM-490-2 has MOS FET input devices and should be handled carefully to prevent static charge pick-up which might damage the devices.





BLOCK DIAGRAM

MECHANICAL DIMENSIONS INCHES (MM)



NOTE: All leads gold plated KOVAR

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	HOLD CAPACITOR (C_A)
2	-IN
3	+IN
4	-15VDC POWER
5	HOLD CAPACITOR (C_B)
6	OUTPUT
7	+15VDC POWER
8	TIMING CAPACITOR (C_C)

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, AM-490-2

(Typical at 25°C, ±15V supplies and $C_A = C_B = 0.1\mu F$, $C_C = .0015\mu F$ unless otherwise noted)

	A	B	C	M
INPUT CHARACTERISTICS				
Common Mode Voltage Range	±10V min.			
Maximum Diff. Input Voltage, no damage	±Vs			
Input Impedance, diff. or com. mode	100 megohms			
Input Capacitance	10pF			
Input Bias Current	150pA			
Input Offset Current	50pA			
Input Offset Voltage	±20μV			
OUTPUT CHARACTERISTICS				
Output Voltage	±10V min.			
Output Current, S.C. protected	±7mA min.			
Output Resistance	200 ohms			
Stable Capacitive Load	1000pF			
PERFORMANCE				
DC Open Loop Gain, 2K load	5×10^8			
Common Mode Rejection, DC, ±5V	120 dB min.			
Warm-Up Time	200 msec.			
DRIFT AND NOISE				
Input Offset Voltage Drift, μV/°C max.	1.0	0.3	0.1	0.6
Input Offset Current Drift	±1pA/°C			
Input Voltage Noise, .01 to 10 Hz	13μV P-P			
Input Voltage Noise, 10 Hz to 10 kHz	33μV RMS			
Input Current Noise, .01 to 10 Hz	8pA RMS			
Input Current Noise, 10 Hz to 10 kHz	700pA RMS			
Chopper Voltage Noise, RTI, 100K unbal.	200μV P-P			
Power Supply Rejection	120 dB min.			
Long Term Stability	±5μV/year			
DYNAMIC CHARACTERISTICS				
Gain Bandwidth Product	3 MHz			
Rise Time, small signal, 10%–90%[1]	200 nsec.			
Slew Rate	2.5V/μsec.			
Full Power Frequency	40 kHz			
Overload Recovery Time	200 msec.			
POWER REQUIREMENT				
Voltage, rated performance	±15VDC, ±0.5V			
Voltage, operating	±12V to ±20VDC[2]			
Current, quiescent	3.5mA typ., 5mA max.			
PHYSICAL-ENVIRONMENTAL				
Operating Temperature Range –2A, B, C	0°C to 70°C			
Operating Temperature Range –2M	–55°C to +125°C			
Storage Temperature Range	–65°C to +150°C			
Package, hermetically sealed	TO-99			

1. Connected as voltage follower.
2. Input common mode range and output range are ±7V to ±15V.

ORDERING INFORMATION

PRICES (1-24)

AM-490-2A	1.0μV/°C max.	0 to 70°C
AM-490-2B	0.3μV/°C max.	0 to 70°C
AM-490-2C	0.1μV/°C max.	0 to 70°C
AM-490-2M	0.6μV/°C max.	–55 to +125°C

AM-490-CK1 CAPACITOR KIT

Consists of 3 miniature metallized polycarbonate capacitors for C_A, C_B, and C_C:

2 ea. 0.1μF ±10% (.203"D x .438"L)
1 ea. .0015μF ±10% (.156"D x .438"L)

THESE AMPLIFIERS ARE COVERED BY GSA CONTRACT

TECHNICAL NOTES

1. Three external capacitors are required for operation of the AM-490-2. One of these, C_c (.0015 μF) is used to set the timing oscillator to give a chopper frequency of 750 Hz; the other two, C_A and C_B (both 0.1μF), are used as holding capacitors for the direct coupled internal sample-holds. All three of these capacitors should have good temperature stability, low leakage, and low dielectric absorption. Polystyrene, teflon or polycarbonate types are recommended. As a convenience, the capacitors are available as a kit of three miniature metallized polycarbonate types.

2. In most requirements the AM-490-2 eliminates the need for a zeroing adjustment. Typical input offset voltage is only ±20μV while the maximum is only ±80μV over the operating temperature range. In cases where zeroing is still necessary, however, there are two methods shown in the application diagrams. In the inverting mode where the negative summing junction is at virtual ground, the zeroing can be accomplished by injecting an offset current into the summing junction by means of a high value resistor connected to a potentiometer. (See "Precision Integrator" diagram). In all other cases, zeroing is accomplished by means of a voltage divider connection to the positive input terminal. (See "Differential Amplifier Connection").

3. The superior input offset voltage drift (1.0, 0.3 or 0.1μV/°C max.) and input offset current drift (1pA/°C) of this amplifier permit it, when properly applied, to resolve microvolt and picoampere level signals. To successfully amplify these very low level signals, it is necessary to use great care in circuit layout and assembly with particular attention given to proper grounding and shielding. Other potential error sources include leakage, thermal environment, and thermocouple effects.

4. The highest practical input impedance which can be used with the AM-490-2 is determined by the point where input offset current drift and input offset voltage drift produce equal errors. Thus:

$$R_{MAX} = \frac{\Delta Eos/\Delta T}{\Delta Ios/\Delta T}$$

Where R_{MAX} is the maximum practicable input resistance seen by either input terminal of the amplifier. This comes out to 1 megohm for the A version, 300 kilohms for the B version, and 100 kilohms for the C version.

5. The amplifier input terminals are differential and symmetrical; for best results the

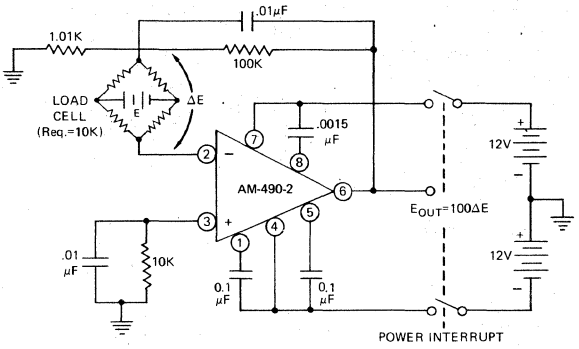
impedance to ground seen by each input terminal should be equal. Matched impedance (resistance and capacitance) as shown in the application diagrams result in minimum output offset drift due to bias currents and also minimum output chopper noise. Chopper noise appears as a common mode input current signal, and under balanced conditions of both resistance and capacitance this noise can be minimized to less than random noise at the output.

6. The AM-490-2 is dynamically stable with 100% feedback (unity gain follower) and 1000pF capacitive load. In very high closed loop gain configurations (>70 dB), it may become desirable to put a capacitor in parallel with the feedback resistor for better stability. This should be done to yield a gain-bandwidth product of 2MHz (RC=80 μsec.) to insure absolute stability. In general, the closed loop bandwidth should be limited to that necessary to pass the required signal frequency components only; this results in minimum output noise. Minimum bandwidth should also be used to eliminate small modulation effects of input signal frequencies near the chopper frequency (750 Hz).

7. Other features of these amplifiers include an exceptionally high open loop gain of 5 x 10^8. For an output voltage swing of ±10V, this reduces the input error due to gain to only ± 20 nanovolts. Common mode rejection is very high (120 dB minimum) at DC, but falls off rapidly with frequency as shown in the graph under Performance Parameters. CMR is typically greater than 100 dB at 10 Hz. For best common mode rejection, therefore, the signal frequency should be limited to about 10 Hz. The noise performance of the amplifier can be readily computed from the two noise graphs shown under Performance Parameters.

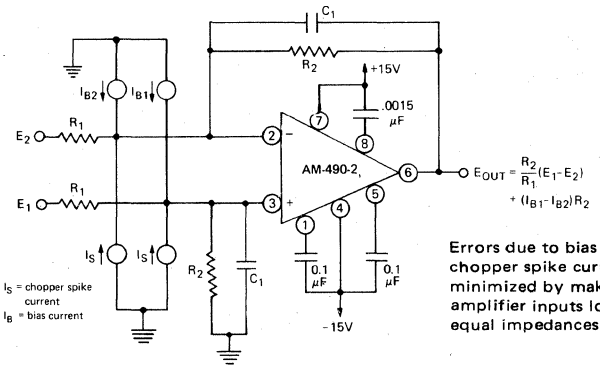
8. The AM-490-2 amplifiers draw a quiescent current of only 3.5mA typical and 5mA maximum; the current is virtually constant over the operating power supply range of ±12V to ±20V. Bandwidth and slew rate change only slightly over this range as shown in the graph "Normalized AC Parameters vs. Power Supply". For the ±12V to ±20V supply range input common mode voltage range and output voltage range become ±7V to ±15V. The wide supply range together with the fast warm-up time of only 200 msec. make the AM-490-2 an excellent amplifier for precision, low power, interrupted supply operation in portable and remote instrumentation systems.

BATTERY POWERED LOAD CELL AMPLIFIER FOR DISCONTINUOUS SERVICE



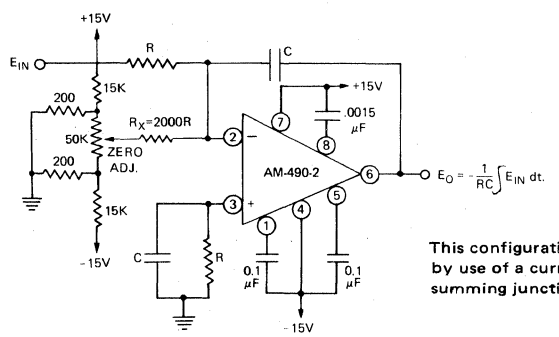
For power interrupt applications the amplifier has a warm-up time of only 200 msec.

INPUT OFFSET CURRENT AND CHOPPER NOISE CONSIDERATIONS



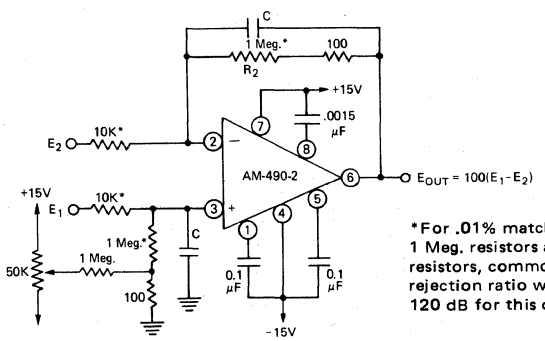
Errors due to bias current and chopper spike current are minimized by making both amplifier inputs look back into equal impedances to ground.

PRECISION INTEGRATOR



This configuration shows zeroing by use of a current into the summing junction.

DIFFERENTIAL AMPLIFIER CONNECTION

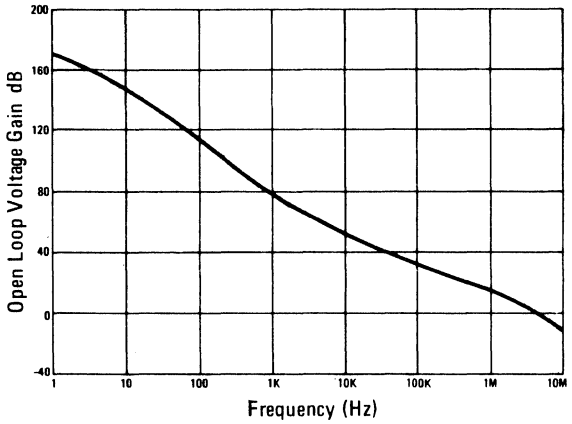


*For .01% match between 1 Meg. resistors and 10K resistors, common mode rejection ratio will be approx. 120 dB for this circuit.

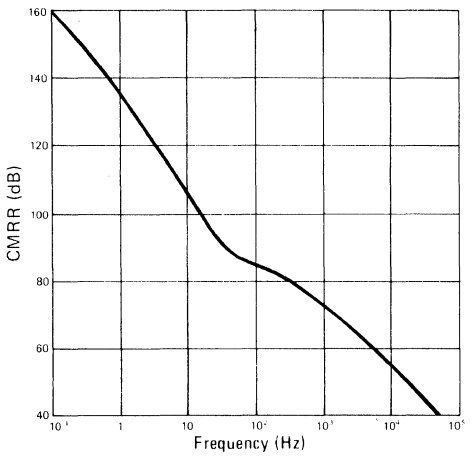
Capacitors C are used only to reduce bandwidth and hence output noise.

PERFORMANCE PARAMETERS (Typical at 25°C, ±15VDC unless otherwise noted)

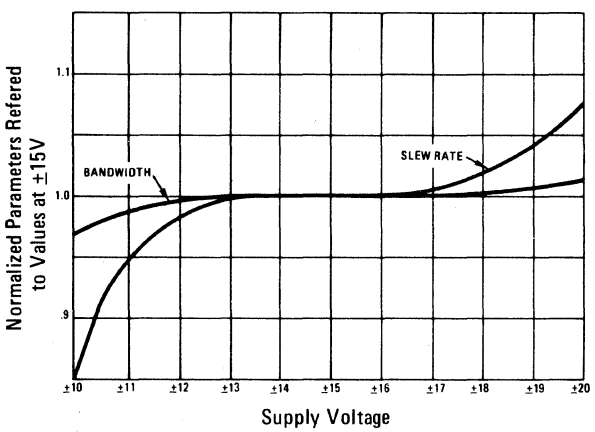
OPEN LOOP FREQUENCY RESPONSE



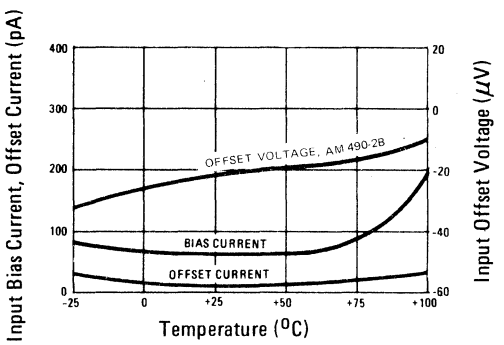
COMMON MODE REJECTION VS. FREQUENCY (TYPICAL)



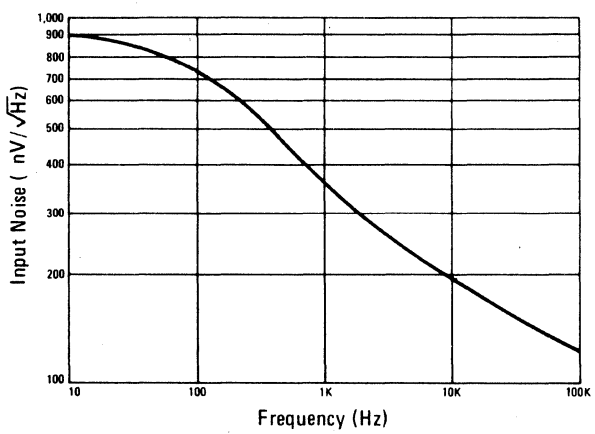
NORMALIZED AC PARAMETERS VS. POWER SUPPLY



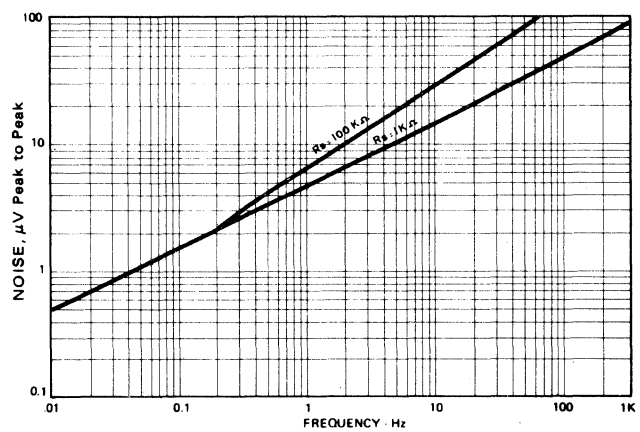
TYPICAL INPUT DRIFT CHARACTERISTICS VS. TEMPERATURE



INPUT VOLTAGE NOISE



EQUIVALENT INPUT NOISE VS. CLOSED LOOP BANDWIDTH



DATEL INTERSIL
11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617)339-9341 / TWX 710-346-1953 / TLX 951340
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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
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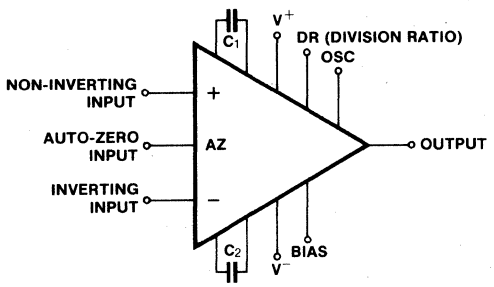
PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Models AM-7600, AM-7601
Commutating Auto-Zero (CAZ) Operational Amplifier

FEATURES

- **Exceptionally low input offset voltage -- 2 μV**
- **Low long-term input offset voltage drift -- 0.2 μV/year**
- **Low input offset voltage temperature drift -- 0.005 μV/°C**
- **Low DC input bias current -- 300 pA**
- **Low DC input offset bias current -- 150 pA**
- **Wide common mode and differential input voltage ranges**
- **Excellent low supply voltage operation -- Down to ±2V**
- **Static-protected inputs -- no special handling required**



GENERAL DESCRIPTION

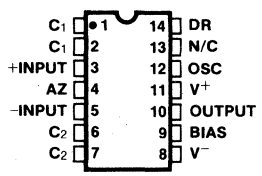
The AM-7600/AM-7601 commutating auto-zero (CAZ) operational amplifiers are designed to replace almost any of today's expensive hybrid or monolithic ultra-low offset op amps, and will provide almost three orders of magnitude (1000×) reduction in input offset voltage compared with conventional device designs. This is achieved through an innovative CAZ amp principle, which uses an entirely new approach to low-frequency operational amplifier design.

The key feature of the CAZ principle is automatic compensation for long-term drift phenomena and temperature effects. Two internal op amps are connected so that when one amplifier is processing an input signal the other is maintained in an "auto-zero" mode. The CAZ amplifiers contain all of the circuitry required for system operation, including an oscillator, a counter, level translators, analog switches and operational amplifiers. Only two external gainsetting resistors and two auto-zero capacitors are needed for complete amplifier function. Control of the oscillator and counter section is provided through the OSC and DR (division ratio) terminals. Internal biasing of the two on-chip op amps is programmable through a three-voltage-level terminal designated BIAS.

The AM-7600 is internally-compensated and is intended for applications which require voltage gains from unity through 100. The uncompensated AM-7601 is intended for those situations which require voltage gains of greater than 20. The major advantage of the AM-7601 over the AM-7600 at high gain settings is the reduction in communication noise and subsequent greater accuracy.

Minimum periodic adjustments and extremely low offset voltage and temperature coefficients make the CAZ operational amplifiers very desirable for operation in adverse environments (temperature, humidity, toxic or radioactive) where equipment service is difficult. Since the device will auto-zero its internal offset errors, no adjustment is required other than that of gain, which is established by the external resistors.

PIN CONFIGURATION



ORDERING INFORMATION

Compensation	Model	Oper.-Temp. Range	Package
COMP.	AM-7600C	0 to + 70° C	14 Pin Epoxy DIP
	AM-7600R	–25 to + 85° C	14 Pin CERDIP
	AM-7600M	–55 to +125° C	14 Pin CERDIP
UNCOMP.	AM-7601C	0 to + 70° C	14 Pin Epoxy DIP
	AM-7601R	–25 to + 85° C	14 Pin CERDIP
	AM-7601M	–55 to +125° C	14 Pin CERDIP

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (sum of both positive and negative supply voltages, V^+ and V^-) ..... 18 Volts
Positive Supply Voltage (GND to V^+) ..... 18 Volts
Negative Supply Voltage (GND to V^-) ..... 18 Volts
DR Input Voltage ..... (V^+ +0.3) to (V^+ −8) Volts
Input Voltage (C_1, C_2, +INPUT, −INPUT, BIAS, OSC (Note 2)) ..... (V^+ +0.3) to (V^- −0.3) Volts
Differential Input Voltage (Note 3) . ±(V^+ +0.3) to (V^- −0.3) Volts
Duration of Output Short Circuit (Note 4) ..... Unlimited
Continuous Total Power Dissipation at or below +25° C free air temperature (Note 5)
CERDIP Package ..... 500 mW
Plastic Package ..... 375 mW

Operating Temperature Range
Suffix M ..... −55° C to +125° C
Operating Temperature Range
Suffix R ..... −25° C to +85° C
Operating Temperature Range
Suffix C ..... 0 to +70° C
Storage Temperature Range ..... −55 to +150° C
Lead Temperature (soldering, 60 seconds) ..... +300° C

Note 1: Stresses above those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent device failures. These are stress ratings only and functional operation of devices under conditions other than those indicated in the Table of Electrical Characteristics is not recommended. Exposure to absolute maximum rating conditions for extended periods of time can cause device failures.

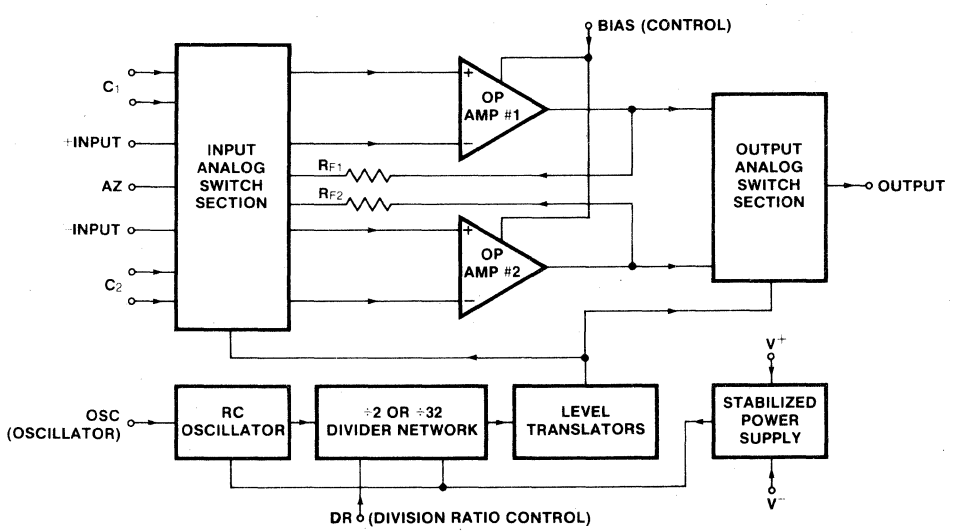
Note 2: An SCR structure is inherent in the CMOS process used in the fabrication of these devices. If voltages in excess of (V^+ +0.3) to (V^- −0.3) volts are connected to either inputs or outputs, destructive latchup can occur. For this reason it is recommended that no inputs from sources not on the same power supply or supplies be applied before the AM-7600/AM-7601 supplies are established, and that if multiple supplies are used the AM-7600/AM-7601 supplies be activated first.

Note 3: No restrictions are placed on the differential input voltages on either the inverting or non-inverting inputs, so long as these voltages do not exceed the power supply voltages by more than 0.3V.

Note 4: Outputs may be shorted to ground (GND) or to either supply (V^+, V^-). Temperature and/or supply voltages must be limited to insure that the dissipation rating is not exceeded.

Note 5: For operation above 25° C free-air temperature, derate 4mW/° C from 500mW for CERDIP and 3mW/° C from 375mW for plastic above 25° C.

BLOCK DIAGRAM



AM-7600/AM-7601

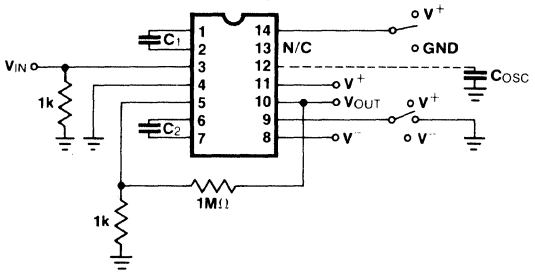
OPERATING CHARACTERISTICS:

Test Conditions: $V^+ = +5$ volts, $V^- = -5$ volts, $T_A = +25°C$, DR pin connected to V^+ ($f_{COM} \cong 160Hz$), $C_1 = C_2 = 1\mu F$, Test Circuit 1, unless otherwise specified.

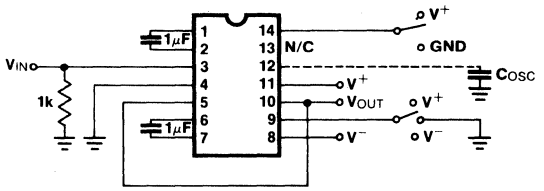
PARAMETER	SYMBOL	CONDITIONS		MIN	VALUE TYP	MAX	UNIT
Input Offset Voltage	V_{OS}	$R_S \leq 1k\Omega$	Low Bias Setting		±2		μV
		$C_1 = C_2 = 1\mu F$	Med Bias Setting		±2	±5	μV
			High Bias Setting		±7		μV
		MIL version over temp.	Med Bias Setting			±20	μV
Long Term Input Offset Voltage Stability	$V_{OS/Time}$	Low or Med Bias Settings			0.2		μV/year
Average Input Offset Voltage Temperature Coefficient	TCV_{OS}	Low or Med Bias Settings	$-55°C > T_A > +25°C$		0.005	0.1	μV/°C
			$+25°C > T_A > +85°C$		0.01	0.1	μV/°C
			$+25°C > T_A > +125°C$		0.05	0.15	μV/°C
Noise Voltage (RMS)	e_n	Band Width 0.1 to 10Hz $R_S \leq 1k\Omega$	Low Bias		0.8		μV
			Med Bias		0.8		μV
			High Bias		1.0		μV
Equivalent Input Noise Voltage Peak-to-peak	e_{np-p}	Band Width 0.1 to 10Hz $R_S \leq 1k\Omega$	Low Bias		4.0		μV
			Med Bias		4.0		μV
			High Bias		5.0		μV
Spot equivalent Noise voltage	e_{n10}	f = 10Hz Band Width 1Hz				700	nV/√Hz
Spot equivalent Noise Current	i_{n10}	f = 10Hz Band Width 1Hz				0.1	pA/√Hz
Differential Input Voltage Range	DIF V_{IN}			$V^--0.3$	to	$V^++0.3$	V
Common Mode Input Range	CMVR	Low Bias		-4.2		+4.2	V
		Med Bias		-4.0		+4.0	V
		High Bias		-3.5		+3.5	V
Common Mode Rejection Ratio	CMRR	Any Bias Setting			88		dB
Power Supply Rejection Ratio	PSRR	Any Bias Setting			110		dB
Non Inverting Input Bias Current	I_{NIB}	Any Bias Setting, (Includes charge injection currents)			0.300	3	nA
Inverting Input Bias Current	I_{IB}	Any Bias Setting, (Includes charge injection currents)			0.150	1.5	nA
Voltage Gain	A_V	$R_L = 100k\Omega$	Low Bias	90	105		dB
			Med Bias	90	105		dB
			High Bias	80	100		dB
Maximum Output Voltage Swing	V_{OUT}	$R_L = 1M\Omega$			±4.9		V
							V
		$R_L = 100k\Omega$			±4.8		V
							V
		$R_L = 10k\Omega$	Positive Swing	+4.4			V
			Negative Swing			-4.5	V
Large Signal Slew Rate	SR	Unity	High Bias Setting		1.8		V/μs
		Gain	Med Bias Setting		0.5		V/μs
		AM-7600	Low Bias Setting		0.2		V/μs
Unity Gain Band Width	GBW		High Bias Setting		1.2		MHz
		AM-7600	Med Bias Setting		0.3		MHz
		Test Circuit 2	Low Bias Setting		0.12		MHz
Extrapolated Unity Gain Band Width	GBW		High Bias Setting		1.8		MHz
		AM-7601	Med Bias Setting		0.4		MHz
			Low Bias Setting		0.2		MHz
BIAS Terminal Input Current	I_{BIAS}	$V^--0.3 \leq V_{BIAS} \leq V^++0.3$ volt			±30		pA
BIAS Voltage to Define Current Modes	V_{BH}	Low Bias Setting		$V^--0.3$		$V^++0.3$	V
	V_{BM}	Med Bias Setting		$V^-+1.4$		$V^+-1.4$	V
	V_{BL}	High Bias Setting		$V^--0.3$		$V^-+0.3$	V
DR (Division Ratio) Input Current	I_{DR}	$V^+ -8.0V \leq V_{DR} \leq V^++0.3V$			±30		pA
DR Voltage to define oscillator division ratio	V_{DRH}	Internal oscillator division ratio 32		$V^--0.3$		$V^++0.3$	V
	V_{DRL}	Internal oscillator division ratio 2		V^--8		$V^+-1.4$	V
Nominal Commutation Frequency	f_{COM}	C_{OSC} = 0 pF	DR Connected to V^+		160		Hz
			DR Connected to GND		2560		Hz
Supply Current	I_S	High Bias Setting		4	7	15	mA
		Medium Bias Setting		0.6	1.7	5	mA
		Low Bias Setting		0.25	0.6	1.5	mA
Operating Supply Voltage Range	V^+-V^-	High Bias Setting		5		16	V
		Medium or Low Bias Setting		4		16	V

AM-7600/AM-7601

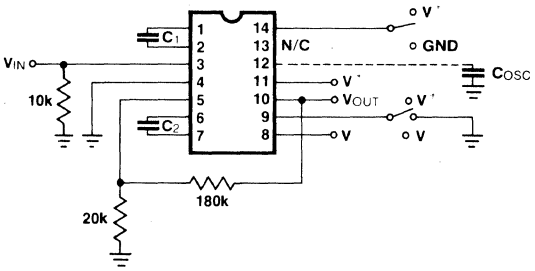
TEST CIRCUITS



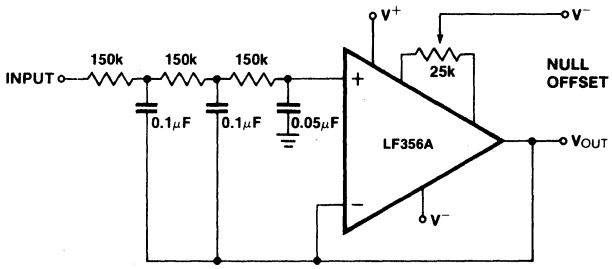
Test Circuit 1: Voltage Gain = 1000



Test Circuit 2: Unity Voltage Gain



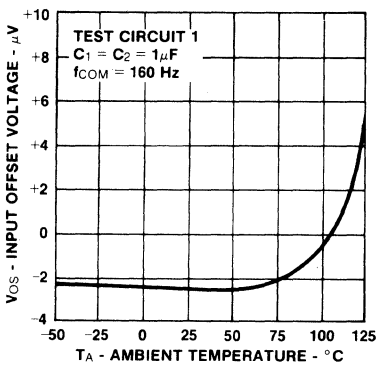
Test Circuit 3: Voltage Gain = 10



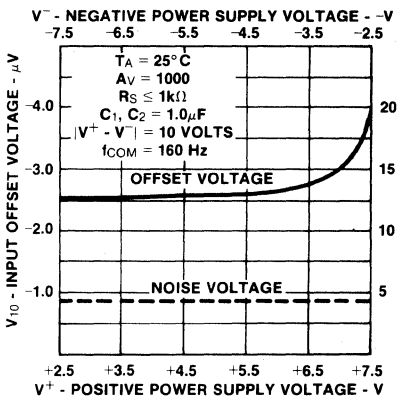
Test Circuit 4: DC to 10Hz Unity Gain Low Pass Filter

TYPICAL CHARACTERISTICS

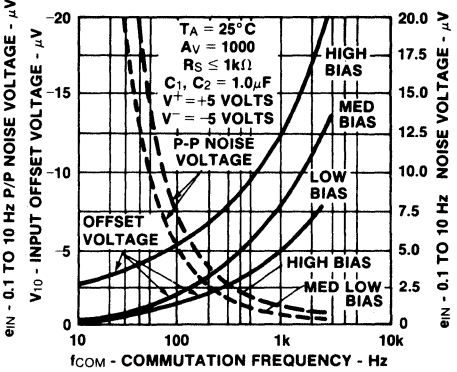
INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



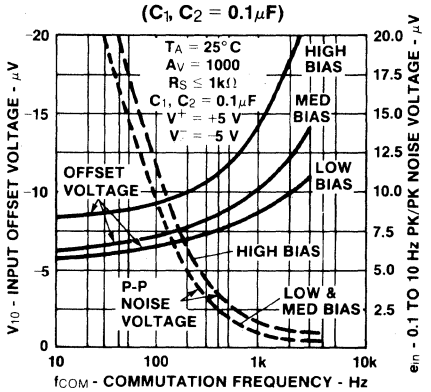
INPUT OFFSET VOLTAGE AND PK TO PK NOISE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGES



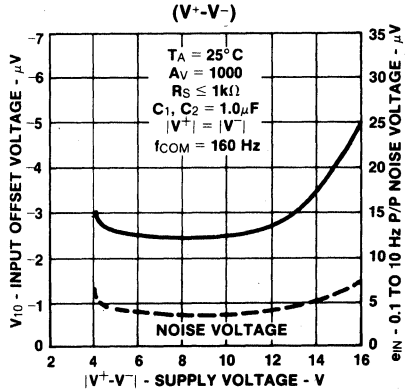
INPUT OFFSET VOLTAGE AND PK TO PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C_1, C_2 = 1μF)



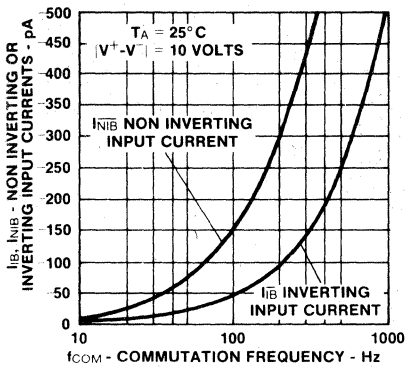
INPUT OFFSET VOLTAGE AND PK TO PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C_1, C_2 = 0.1μF)



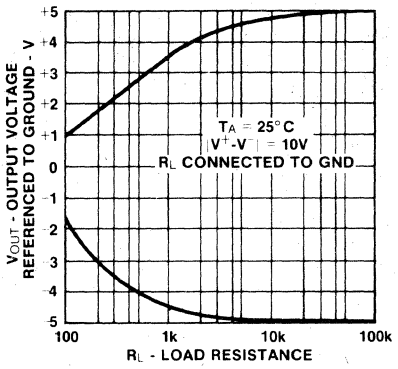
INPUT OFFSET VOLTAGE AND PK TO PK NOISE AS A FUNCTION OF SUPPLY VOLTAGE (V+-V−)



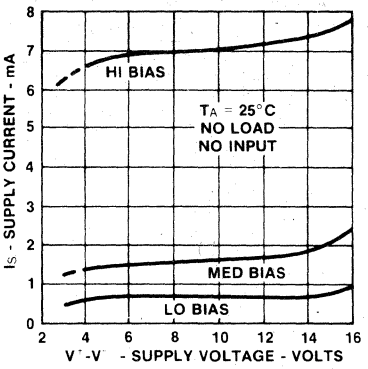
INPUT CURRENT AS A FUNCTION OF COMMUTATION FREQUENCY



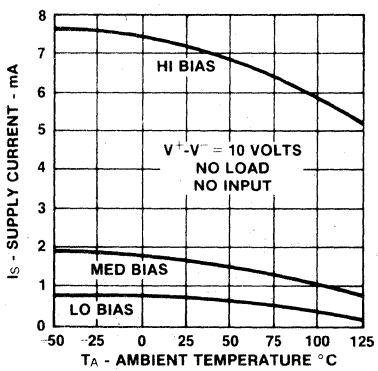
MAXIMUM OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT LOAD RESISTANCE



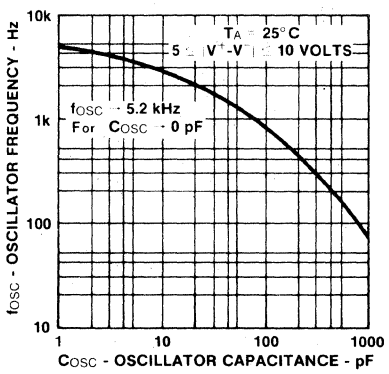
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



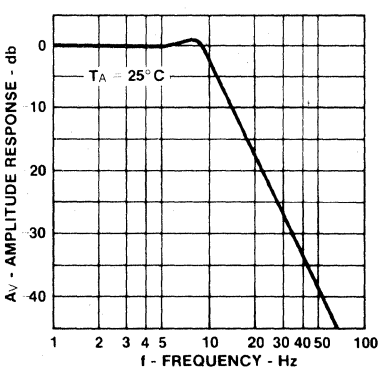
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



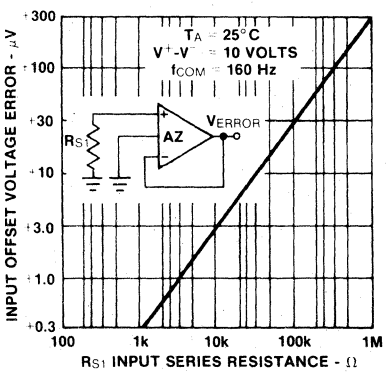
OSCILLATOR FREQUENCY AS A FUNCTION OF EXTERNAL CAPACITIVE LOADING



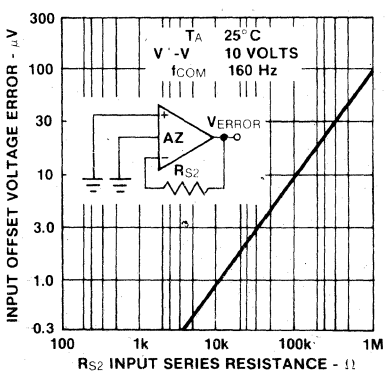
FREQUENCY RESPONSE OF THE 10 Hz LOW PASS FILTER USED TO MEASURE NOISE (TEST CIRCUIT 4).



TOTAL EQUIVALENT INPUT OFFSET VOLTAGE AS A FUNCTION OF SOURCE IMPEDANCE — +INPUT



TOTAL EQUIVALENT INPUT OFFSET VOLTAGE AS A FUNCTION OF SOURCE IMPEDANCE — -INPUT



DETAILED DESCRIPTION

CAZ Operational Amplifier Operation

The CAZ operational amplifier functions on principles which are very different from those encountered in conventional op amp types. An important advantage of the AM-7600/AM-7601 devices is the ability to self-compensate for internal error voltages, whether they are steady-state, related to temperature or supply voltage, or variable in nature over a long term.

Operation of the AM-7600/AM-7601 CAZ operational amplifier is demonstrated in Figure 1. The basic amplifier configuration represented by the large triangles has one more input than does a regular op amp--the AZ, or auto-zero input. The voltage at the AZ input is that voltage to which each of the internal op amps must be auto-zeroed. In Mode A, op amp #2 is connected into a unity gain mode through on-chip analog switches, and charges the external capacitor C_2 to a voltage equal to the DC offset voltage of that amplifier, in addition to the instantaneous low frequency noise voltage. A short time later, the analog switches reconnect to the on-chip op amps in the configuration shown in Mode B. In this mode, op amp #2 has capacitor C_2 (which was charged to a voltage equal to its offset and noise voltage) connected in series to its non-inverting (+) input and nulls out the input offset and noise voltage of the amplifier. While one of the op amps is processing the input signal, the other is placed in an auto-zero mode and charges a capacitor to a voltage equal to its equivalent DC and low-frequency error voltage. The internal op amps are connected (at a rate designated as the commutation frequency, f_{COM}) so that at all times one or the other of the op amps is processing the input signal, while the voltages on capacitors C_1 and C_2 are being updated regularly to compensate for variables such as low-frequency noise voltage and input offset voltages due to drift with temperature, time, or supply voltage.

The CAZ amp concept offers a number of other advantages to the designer, as compared to standard bipolar or FET-input op amps:

- Effective input offset voltages can be made between 1000x and 10,000x less without trimming.
- Long-term drift phenomena are compensated for and dramatically reduced.
- Temperature effects are compensated for over a wide range. Reductions can be as high as 100 times or higher.
- Supply voltage sensitivity is reduced.

CMOS processing is ideally suited to implement the CAZ op amp structure. Not only is the digital section simple to design in CMOS, but the transmission gates (analog switches), which connect the internal op amps, are efficiently implemented for minimum charge injection and widest operating voltage range. The analog section, which includes the two on-chip op amps, provides performance which in most cases is similar to bipolar or FET input designs. Open loop gains of greater than 100 dB, typical offset voltages of ±5mV, and ultra-low input leakage currents (typically 1 pA) make the CMOS process quite suitable for the CAZ amp concept.

The on-chip op amps are connected internally to the external input and output terminals via CMOS analog switches, as shown in Figure 2. The analog switch structure shown in Figure 2 is arranged so that at any time three switches are open and three switches are conducting. Each analog switch includes a P-channel transistor in parallel with an N-channel transistor.

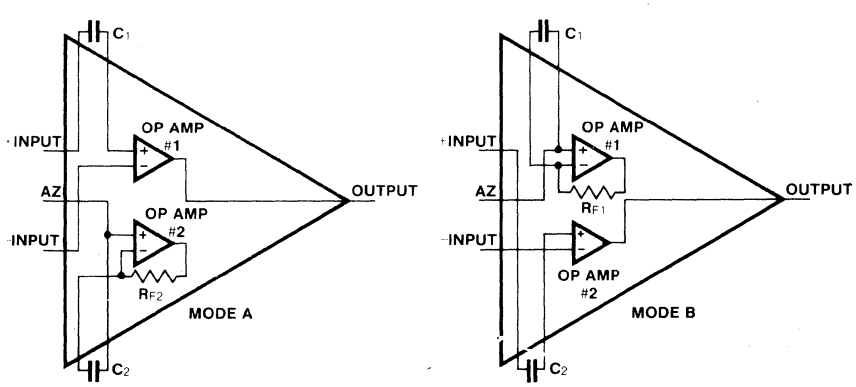


Figure 1: Diagramatic representation of the 2 half cycles of operation of the CAZ OP AMP.

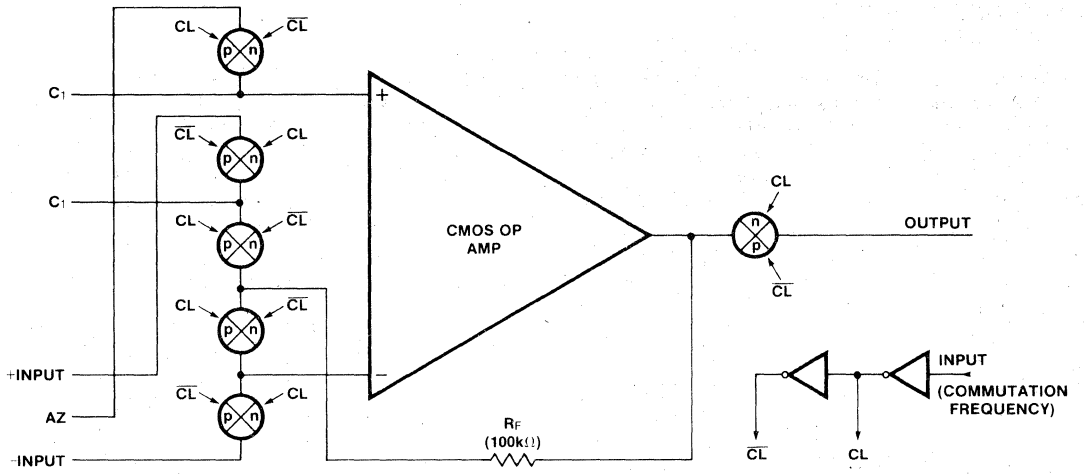


Figure 2: Schematic of analog switches connecting each internal OP AMP to the external inputs at the output.

APPLICATIONS

The AM-7600/AM-7601 CAZ op amp is ideal for use as a front-end preamplifier for dual-slope A/D converters which require high sensitivity for single-ended input sources such as thermocouples.

A typical high-sensitivity A/D converter system is shown in Figure 3. The system uses a model ADC-7109 12-bit monolithic A/D binary converter, and is intended for direct interface with microprocessors Both the AM-7600/AM-7601 and the ADC-7109 use power supply voltages of ±5V, and the entire system consumes typically 2.5 mA of current.

The input signal is applied through a low-pass filter (150 Hz) to the CAZ op amp, which is connected in a non-inverting gain configuration of either 10 or 100. The internal oscillator of the CAZ amp is allowed to run free at about 5,200 Hz, resulting in a commutation frequency of 160 Hz, with the DR terminal connected to V⁻. The error-storage capacitors C_1 and C_2 are each 1 μF value, and provide a good compromise between the minimum equivalent input offset voltage and the lowest value of low-frequency noise.

The output signal is then passed through a low-pass filter (1 MΩ and 0.1 μF), with a bandwidth of 1.5 Hz. This results in an equivalent DC offset voltage of 1 to 2 μV, and a peak-to-peak noise voltage of 1.7 μV, referred to the input of the CAZ amp. The output from the low-pass filter feeds directly into the input of the ADC-7109.

In a system such as that shown in Figure 3 there is a degree of flexibility possible in assigning various gains to the AM-7600/AM-7601 pre-amplifier, and to various sensitivities for the ADC-7109. For optimum performance, the CAZ op amp must amplify the input signal so that the equivalent 15μV input noise voltage of the A/D converter is masked. This implies a gain of at least 10 for the CAZ op amp preamplifier.

On the other hand, if the gain of the CAZ op amp is increased too much, its output swing will be limited by the ±5V supplies. This condition imposes a maximum gain of 200 to produce an output of ±0.000005 times 4,096 times 200, or ±4.096V, for a 5μV per count sensitivity. Use of an AM-7600 is recommended for low gains (<20) and the AM-7601 for gains of more than 20.

The values of the integrating resistor and the reference voltage must be chosen to suit the overall sensitivity of the system. For example, in a system requiring a sensitivity of 5μV per count, it is suggested to use a CAZ amp in a gain configuration of 100 (use AM-7601). Thus for a full scale count of 4096 (12 bits), the input voltage to the ADC-7109 would be 5μV times 100 times 4096 or 2.048 volts. Since the ratio of input to reference is 2:1, the value of the reference voltage becomes 1.024V, and a 100kΩ integrating resistor is recommended. A system such as that shown in Figure 3 will allow a resolution of 1°C for low sensitivity platinum/rhodium junctions. For 0.1°C resolution, use high sensitivity thermocouples having copper/constantan junctions.

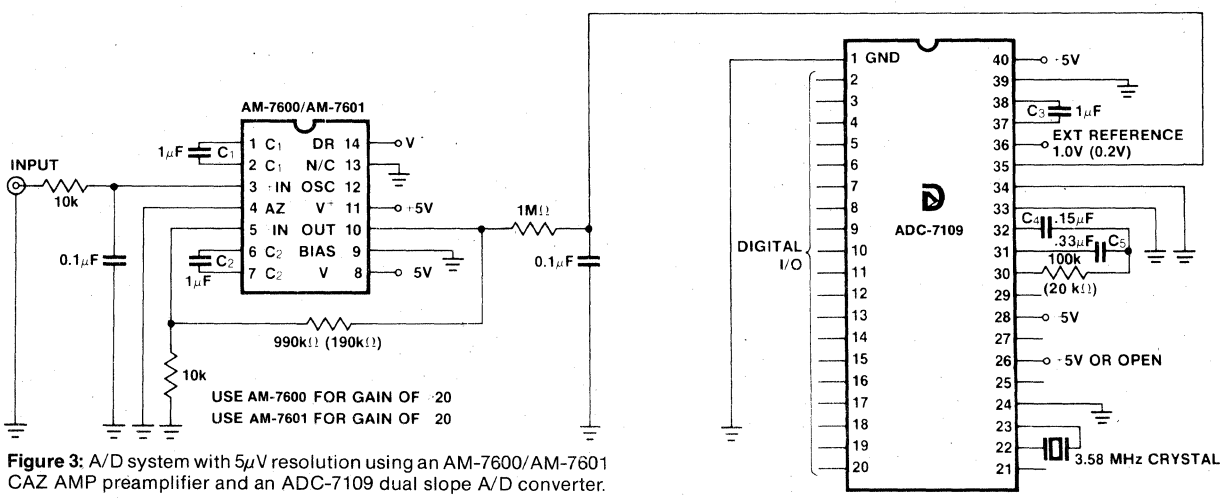


Figure 3: A/D system with 5μV resolution using an AM-7600/AM-7601 CAZ AMP preamplifier and an ADC-7109 dual slope A/D converter.

The low-pass filter between the output of the CAZ op amp and the input of the ADC-7109 A/D converter can be used to improve the signal-to-noise ratio of the system by reducing bandwidth. A 10 Hz filter will result in an equivalent peak-to-peak noise voltage figure of 4μV. If the bandwidth is reduced to 1.5 Hz, the peak-to-peak noise voltage will be reduced to about 1.7 μV, a reduction by a factor of three. The penalty for this reduction will be a lower system response time; however in most cases this will not be a major consideration, because of the large thermal inertia of many thermocouple probes.

SOME HELPFUL HINTS

Testing the AM-7600/AM-7601 CAZ Operational Amplifier

A simple and relatively accurate means of testing the CAZ op amp is to use a Tektronix Type 577 curve tracer, with the CAZ op amp inserted in a special 14-lead socket which plugs into a Tektronix 178, and which contains two soldered-in auto-zero capacitors of 1 μF each. This simple and convenient tester will provide most of the information needed for low-frequency parameters. The test setup will allow resolution of input offset voltages to about 10 μV.

For greater accuracy, it is suggested that a breadboard be built which minimizes thermoelectric effects and which includes an output low-pass filter of the type shown in Test Circuit #4. The output from the CAZ amp can be connected to a dual-slope A/D converter as shown in Figure 3. The low-frequency noise can then be displayed on a storage scope or on a strip chart recorder.

Bias Control

The on-chip op amps consume over 90% of the power required for the AM-7600/AM-7601. Three externally-programmable bias levels are provided. These levels are set by connecting the BIAS terminal to V^+, GND or V^-. The difference between each bias setting is approximately a factor of three, which allows a 9:1 ratio between supply current and the bias setting. The reason for this current programmability is to provide the user with a choice of device power dissipation levels, slew rate values (the higher the slew rate the better the recovery from commutation spikes), and offset errors due to chip "voltage drop" and thermoelectric effects (the higher the power dissipation the higher the input offset error). In most cases, the medium (MED BIAS) setting will be the best choice.

Output Loading (Resistive)

With a 10 kΩ load the output swing can cover nearly the entire supply voltage range, and the device can be used with loads as low as 2 kΩ. However, with loads of less than 50 kΩ, the on-chip op amps become transconductance amplifiers, since their output impedances are about 50 kΩ each. Thus the open-loop gain is 20 dB less with a 2 kΩ load than it would be with a 20 kΩ load. For high gain configurations requiring high accuracy, output loads of 100 kΩ or more are suggested.

Another consideration which must not be overlooked is the additional power dissipation of the chip which results from a large output swing into a low value load. This added variable can affect the initial input offset voltages under certain conditions.

Output Loading (Capacitive)

In many applications, it is desirable to include a low-pass filter at the output to reduce high-frequency noise outside the signal passband of interest. With conventional op amps, the obvious solution would be to place a capacitor across the external feedback resistor to provide the low pass filter.

However, with the CAZ op amp, this is not feasible because of the nature of commutation voltage spikes. The voltage spikes show a low impedance characteristic in the direction of the auto-zero voltage, and a high impedance on the recovery edge, as shown in Figure 4. It can be seen that the effect of a large load capacitor is to produce an area error in the output waveform, and hence an effective gain error. The output low pass filter must be a high impedance type to avoid output voltage area errors. For example, a 1.5 Hz filter should use a 100 kΩ resistor and a 1.0 μF capacitor, or a 1.0 MΩ resistor and an 0.1 μF capacitor.

Oscillator and Digital Considerations

The oscillator has been designed to run free at about 5.2 kHz when the OSC terminal is open-circuited. If the full divider network is used, this will result in a commutation frequency of about 160 Hz nominal. The commutation frequency is the frequency at which the on-chip op amps are switched between the signal processing and the auto-zero modes. A 160 Hz commutation frequency represents approximately the optimum frequency at which the input offset voltage is close to minimum, where the low-frequency noise is acceptable, and where errors derived from noise spikes will be low. Other commutation frequencies may provide optimization of other parameters, but always to the detriment of major characteristics.

The oscillator is of a high impedance type, so that a load of only a few picofarads on the OSC terminal will cause a significant shift in frequency. It is therefore recommended that if the desired frequency of the oscillation is 5.2kHz, the terminal should be left unattached and open. In other instances, it may be desirable to lock the oscillator to a clock

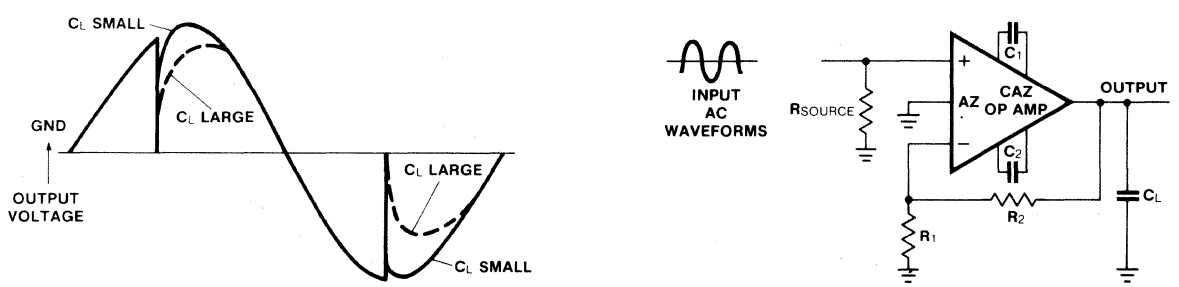


Figure 4: Effect of a load capacitor on output voltage waveforms.

or to run it at another frequency. The AM-7600/AM7601 provides two degrees of flexibility. First, the DR (division ratio) terminal permits the user to choose between dividing the oscillator by 32 (DR terminal to V^+) or by 2 (DR terminal to GND), to obtain the commutation frequency. Second, the oscillator may have its frequency lowered by the addition of an external capacitor connected between the OSC terminal and V^+, or system ground terminals. For situations which required the commutation frequency to be locked onto a master clock, the OSC terminal can be driven from TTL logic (with resistive pull-up) or from CMOS logic, provided that the V^+ supply (with respect to ground) is +5V (±10%) and the logic driver also operates from a similar supply voltage. This is because the logic section -- including the oscillator -- operates from an internal -5V supply referenced to V^+ generated on-chip, and is not accessible externally.

Thermoelectric Effects

The ultimate limitations to ultra-high-precision DC amplifiers are due to thermoelectric, Peltier or thermocouple effects whereby junctions consist of various metals, alloys, silicon, etc. Unless all junctions are at precisely the same temperature, small thermoelectric voltages will be produced, generally about 0.1 μV/°C. However, these voltages can be several tens of microvolts per °C for certain thermocouple materials.

In order to realize the extremely low offset voltages which the CAZ op amp can provide, it is essential to take precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement across device surfaces. Special low-temperature solder (70% cadmium. 30% tin) should be used. In addition, the supply voltages and power dissipation should be kept to a minimum. Use the medium bias mode as well as a high impedance load, and keep well away from heat dissipated by surrounding equipment.

Component Selection

The two required auto-zero capacitors, C_1 and C_2, should each be of 1.0 μF value. These are large values for non-electrolytic capacitors, but since the voltages impressed on them do not change significantly, problems of dielectric absorption and the like are not as important as they would be in applications involving integrating dual-slope A/D converters.

Excellent results have been obtained in operation at commercial temperature ranges when using several of the smaller-size and more economical capacitors, since the absolute values of the capacitors need not be critical. Although not guaranteed, polarized electrolytic capacitors rated at 1.0μF/50V have been used with success.

Commutating Voltage Transient Effects

While in most respects the CAZ op amp behaves like a conventional op amp, its principal applications will be in very low level, low-frequency preamplifiers limited to DC through 100 Hz. This is because of the finite switching transients which occur in the input and output terminals due to commutation effects. These transients have a frequency spectrum beginning at the commutation frequency, and include all of the higher harmonics. If the commutation frequency is higher than the highest in-band frequency, these transients can be effectively blanked with a low-pass filter.

The input commutation transients arise when each of the on-chip op amps experiences a shift in voltage equal to the input offset voltage about (5 - 10 mV), which usually occurs during the transition from the signal processing mode to the auto-zero mode. Since the input capacitances of the on-chip op amps are typically in the 10 pF range, and since it is desirable to reduce the effective input offset voltage about 10,000 times, the offset voltage auto-zero capacitors C_1 and C_2 must be at least 10,000 x 10 pF, or 0.1μF each.

Figure 5: Output waveform from Test Circuit 1.

The charge which is injected into the op amp when it is switched into the signal-processing mode produces a rapidly-decaying voltage spike at the input, in addition to an equivalent DC bias current averaged over a full cycle. This bias current is directly proportional to the commutation frequency, and in most instances will greatly exceed the inherent leakage currents of the input analog switches, which are typically about 1.0 pA at ambient temperature of 25°C.

The output waveform shown in Test Circuit #1 (with no input) is treated in Figure 5. Note that the equivalent noise voltage shown is amplified 1000 times, and that because of the finite slew rate of the on-chip op amps the 7 mV input transients are not amplified by 1000.

The output transient voltage effects (as distinct from the input effects which are propagated through the on-chip op amps) will occur if there is a difference in the output voltage of the internal op amps between the auto-zero modes and the signal-processing modes. The output stage of the on-chip op amp must slew from its auto-zero output voltage to the desired signal-processing output voltage. This is shown in Figure 6, where the system is auto-zeroed to ground.

The duration of the output transients is greatly affected by the gain configuration and the bias setting, since these two parameters have an effect on system slew rate. At low gains and high bias settings, the output transient durations are very short. For this reason there are two versions of the CAZ op amp, the AM-7600 which is compensated for unity gain and which can be used for gain configurations up to 100, and the AM-7601, which is uncompensated and recommended for operation in gain configurations greater than 20. Thus, when a signal is being processed in a high gain configuration, the effective output signal error is greater for the AM-7600 than it is for the AM-7601.

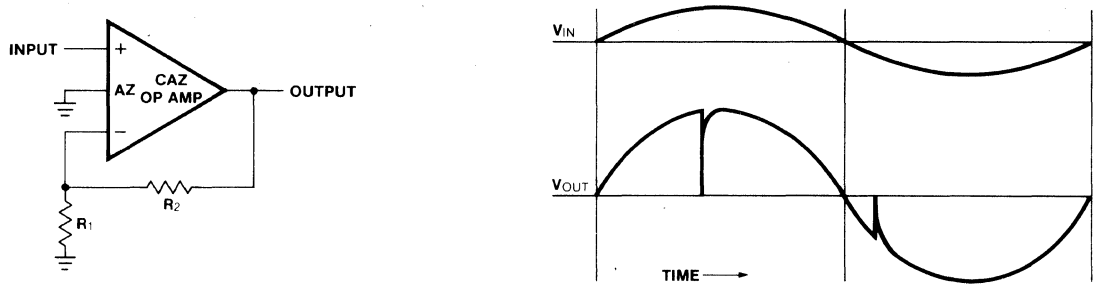
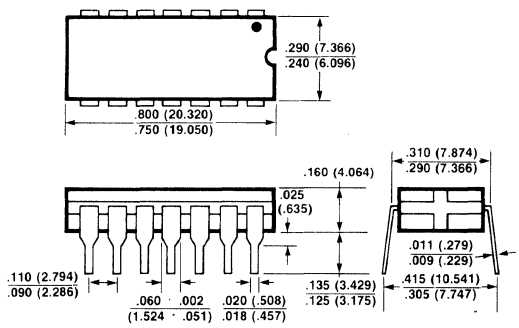


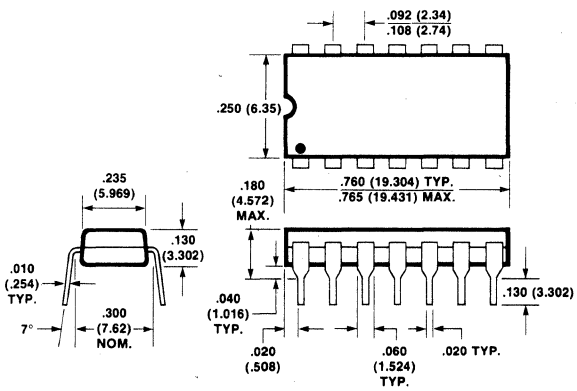
Figure 6: Simple CAZ OP AMP circuit and the output voltage waveform.

PACKAGE DIMENSIONS

14 LEAD CERDIP PACKAGE



14 LEAD PLASTIC PACKAGE



AM-761X Series Low Power CMOS Operational Amplifiers

FEATURES

- **Wide Operating Voltage Range — ±0.5V to ±8V**
- **Programmable Power Consumption — as low as 10μW**
- **High Input Impedance — $10^{12}\Omega$**
- **Low Input Bias — 50 pA max.**
- **Internally Compensated and Uncompensated Models**

GENERAL DESCRIPTION

The AM-761X series is a family of monolithic CMOS op amps. These amplifiers provide high performance operation at low supply voltages and selectable quiescent currents. Their features make them ideal for applications that require ultra low input current and low power drain.

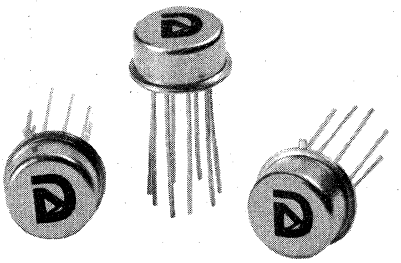
The AM-7611, 12, and 13 have a unique quiescent current programming pin that allows the setting of standby current to 1 mA, 100 μA or 10 μA with no external components. This results in power drain as low as 10 μW. These models are internally compensated and are stable for closed loop gains as low as 1.

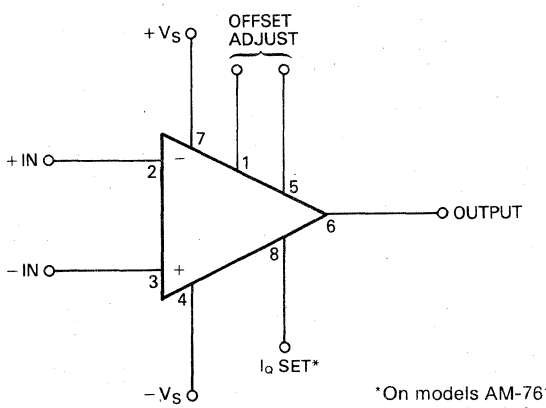
The basic amplifier will operate at supply voltages ranging from ± 0.5V to ± 8V, and may be operated from a single Ni-Cad battery. Output voltage swings range to within a few millivolts of the supply voltage.

Other significant features include 50 pA maximum input bias current, $10^{12}\Omega$ input impedance, and low noise current density, typically .01 pA/√Hz. Dynamic characteristics include 1 MHz unity gain bandwidth and 1.6V/μsec slew rate at I_Q = 1 mA.

All devices are internally protected by the use of input diodes, models AM-7613 and AM-7615 are protected for inputs of up to ±200V. Outputs are fully short circuit protected.

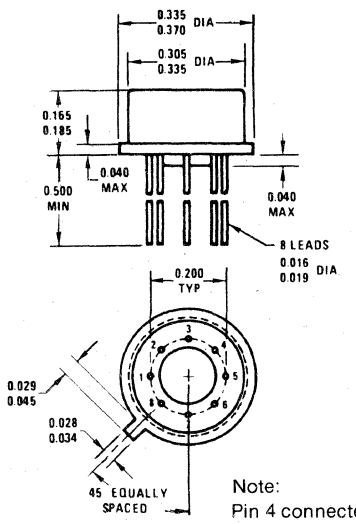
Packaged in an 8 pin hermetically sealed TO-99 case, these devices are available in 0° C to +70° C and in −55° C to +125° C operating temperature ranges.





*On models AM-7614 and 15, Pin 8 is for external compensation

MECHANICAL DIMENSIONS



Note:
Pin 4 connected to case.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	Trim
2	−in
3	+in
4	−Supply
5	Trim
6	Output
7	+Supply
8	I_Q Set*

*On models AM-7614 and 15, pin 8 is for external compensation

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, AM-761X SERIES

Typical @ +25°C, RL = 100 KΩ, unless otherwise noted

	Vsupp = ±5V	Vsupp = ±0.5V[1]
MAXIMUM RATINGS[2]		
Power Supply Voltage	±9V	±9V
Power Dissipation[3]	250 mW	250 mW
Differential Input Voltage	± [(V+ +0.3) − (V− −0.3)] V	± [(V+ +0.3) − (V− −0.3)] V
Differential Input Voltage (AM-7613, AM-7615)	± [(V+ +200) − (V− −200)] V	± [(V+ +0.3) − (V− −0.3)] V[4]
INPUT CHACTERISTICS		
Input Offset Voltage, max.	5 mV	5 mV
Input Bias Current, max.	50 pA	50 pA
Input Offset Current, max.	30 pA	30 pA
Common Mode Voltage Range, min.,		
I_Q = 10 μA[5]	±4.4V	±0.1V
I_Q = 100 μA	±4.2V	---
I_Q = 1 mA[5]	±3.7V	---
Extended Common Mode Voltage Range, min.		
I_Q = 10 μA[5]	±5.3V	±0.1V to −0.6V
(AM-7612 Only) I_Q = 100 μA	+5.3V −5.1V	---
I_Q = 1 mA[5]	+5.3V −4.5V	---
Input Resistance	$10^{12}\Omega$	$10^{12}\Omega$
OUTPUT CHARACTERISTICS		
Output Voltage	±4.9V min	±0.49V
PERFORMANCE		
Large Signal Voltage Gain	80 dB min[6]	80 db[7]
Unity Gain Bandwidth, I_Q = 10 μA[5]	44 kHz	44 kHz
I_Q = 1 mA[5]	1.4 MHz	---
Common Mode Rejection Ratio,		
I_Q = 10 μA[5]	70 dB min	80 dB
I_Q = 100 μA	70 dB min	---
I_Q = 1 mA[5]	60 dB min	---
Power Supply Rejection Ratio,		
I_Q = 10 μA[5]	80 dB min	80 dB
I_Q = 100 μA	80 dB min	---
I_Q = 1 mA[5]	70 dB min	---
Input Offset Voltage Drift	15 μV/°C	15 μV/°C
Input Noise Voltage[8]	100 nV/√Hz	100 nV/√Hz
Input Noise Current[8]	.01 pA/√Hz	.01 pA/√Hz
Slew Rate[9] R_L = 1 MΩ, I_Q = 10 μA[5]	.016V/μsec	.016V/μsec
R_L = 100 KΩ, I_Q = 100 μA	.16V/μsec	---
R_L = 10 KΩ, I_Q = 1 mA[5]	1.6V/μsec	---
POWER REQUIREMENTS		
Voltage, Rated Performance	±5 VDC	±0.5 VDC
Supply Voltage Range	±0.5V to ±8 VDC	±0.5V to ±8 VDC
Supply Current, max, I_Q = 10 μA[5]	20 μA	15 μA
I_Q = 100 μA	250 μA	---
I_Q = 1 mA[5]	2.5 mA	---
PHYSICAL ENVIRONMENTAL		
Operating Temperature Range		
Suffix — C		0°C to +70°C
Suffix — M		−55°C to +125°C
Storage Temperature Range		−55°C to +150°C
Package, Hermetically Sealed		TO-99

NOTES:

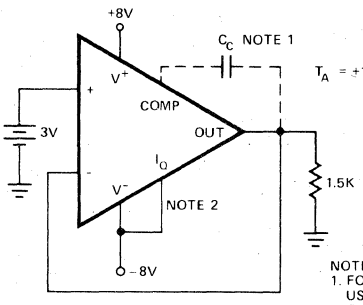
1. Operation at Vsupp = ±0.5V is guaranteed at I_Q = 10 μA only. Those devices with a selectable I_Q of 10 μA are the AM-7611, 7612, and 7613.
2. Stresses above those listed under "MAXIMUM RATINGS" may cause permanent device failure. These are stress ratings only, functional operation of the device at these, or at conditions above those indicated in the operating section of this specification is not implied. Exposure to maximum rating conditions for extended periods may cause device failures.
3. At +25°C, for operation in ambient temperatures in excess of +25°C derate by 2 mW/°C.
4. AM-7613 only.
5. I_Q is selectable on AM-7611, 12, and 13 only. On AM-7614, and 15, I_Q = 100 μA.
6. Vout = 4V, R_L = 10 KΩ, I_Q = 100 μA
7. Vout = ±0.1V, R_L = 100 KΩ, I_Q = 10 μA
8. Rs = 100Ω, f = 1 kHz
9. CL = 100 pF, Vin = 8V

TECHNICAL NOTES

1. The AM-7611, 12, and 13 have an external I_Q control pin (pin 8), permitting the amplifiers quiescent current to be set at 1 mA, 100 μA, or 10 μA. These current settings change only very slightly over the entire supply voltage range. To set the I_Q of these programmable models, connect the I_Q pin (pin 8) as follows:
   I_Q = 10 μA - I_Q pin (pin 8) to V+ (pin 7)
   I_Q = 100 μA - I_Q pin (pin 8) to grnd. — (If this is impossible, any voltage from V+ −0.8V to V− +0.8V may be used)
   I_Q = 1 mA - I_Q pin (pin 8) to V− (pin 4)
   Since the amount of negative current available is a function of quiescent current, for maximum p-p output voltage swings into low impedance loads, I_Q of 1 mA should be selected.
2. All models are provided with external offset null capability. Zeroing is accomplished by connecting a 25 KΩ pot between the offset pins (pins 1 and 5) with the wiper connected to V+ (pin 7).
3. Operation at Vsupp = ±0.5V is guaranteed at I_Q = 100 μA only. This applies to those models, the AM-7611, 12, and 13, with a selectable I_Q.
4. The AM-7611, 12, and 13 are internally compensated through the use of a 33 pF capacitor. This compensation gives stable operation for closed loop gains as low as 1 for capacative loads up to 100 pF. The AM-7614, and 15 are externally compensated by connecting a capacitor between the compensation (pin 8) and output (pin 6) pins. For unity gain compensation, a 33 pF capacitor is required; for greater than unity gain applications, increased bandwidth and slew rate can be obtained by reducing the value of the compensating capacitor. Since the gm of the first stage is proportional to $\sqrt{I_Q}$, greatest compensation is required when I_Q = 1 mA.
5. The AM-7613 and 15 include on-chip thin film resistors and clamping diodes which allow voltages of up to ±200V to be applied to either input for an indefinite time without device failure. These devices will be useful where high common mode voltages, differential mode voltages or high transients may be experienced.
6. The AM-7612 allows the common mode voltage range to exceed the magnitude of Vsupp. For those applications where Vsupp ≥ ±1.5V, the input common mode voltage range is allowed to exceed Vsupp by 0.1V. Where Vsupp ≤ ±1.5V, the input common mode voltage range is limited to the magnitude of Vsupp in the positive direction, but may exceed Vsupp in the negative direction by 0.1V.
7. To prevent latchup the amplifier supplies must be established simultaneously with, or before any input signals are applied. If this is not possible, the drive circuits must limit input current to 2 mA to prevent latchup. Also, no voltage greater than 0.3V beyond Vsupp may be applied to any pin, with the exception of the AM-7613 and AM-7615 inputs, which are protected to ±200V.
8. Due to the high input impedances, care should be taken in layout construction, board cleanliness, and supply filtering in order to avoid hum and noise pickup.

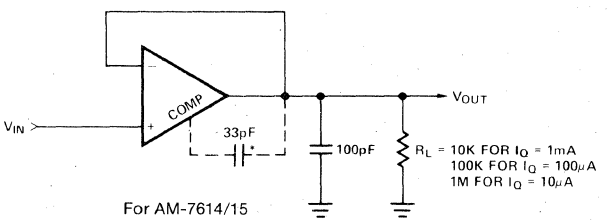
APPLICATIONS

BURN—IN AND LIFE TEST CIRCUIT



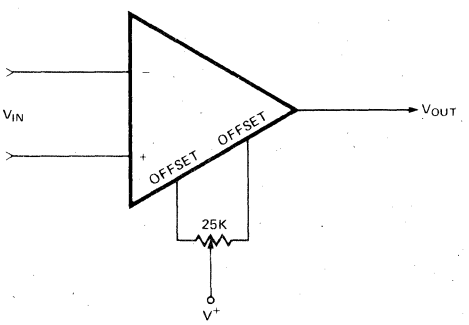
NOTES:
1. FOR DEVICES WITH EXTERNAL COMPENSATION, USE 33pF.
2. FOR DEVICES WITH PROGRAMMABLE STANDBY CURRENT, CONNECT I_Q PIN TO V^- (I_Q = 1mA MODE).

UNITY GAIN FREQUENCY COMPENSATION



For AM-7614/15

V_{OS} NULL CIRCUIT



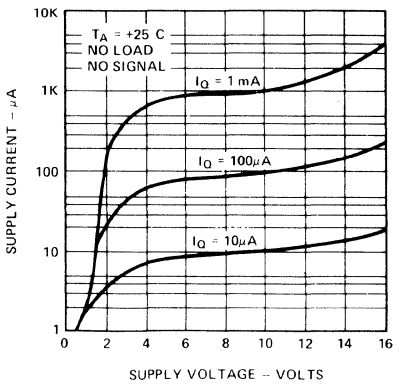
ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
AM-7611C	0°C to +70°C
AM-7611M	−55°C to +125°C
AM-7612C	0°C to +70°C
AM-7612M	−55°C to +125°C
AM-7613C	0°C to +70°C
AM-7613M	−55°C to +125°C
AM-7614C	0°C to +70°C
AM-7614M	−55°C to +125°C
AM-7615C	0°C to +70°C
AM-7615M	−55°C to +125°C

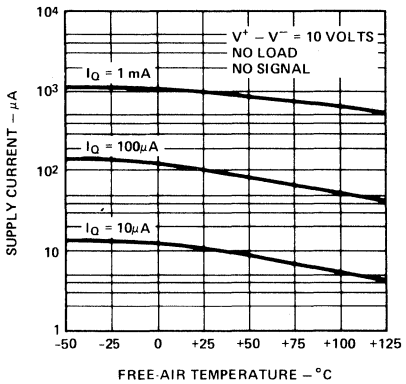
Trimming Potentiometer: TP25K

TYPICAL PERFORMANCE CURVES

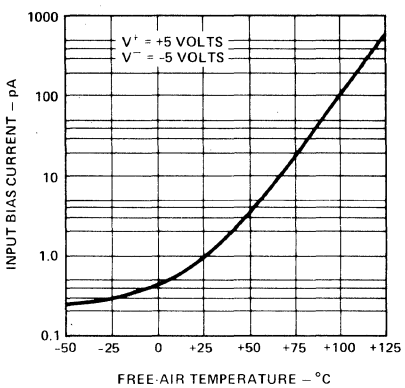
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



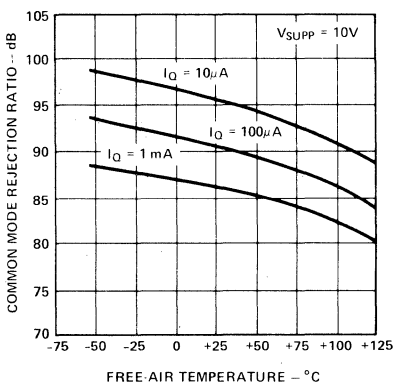
SUPPLY CURRENT AS A FUNCTION OF FREE-AIR TEMPERATURE



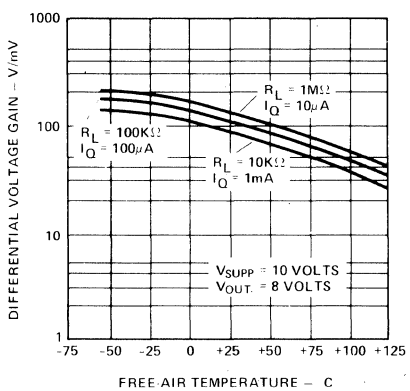
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



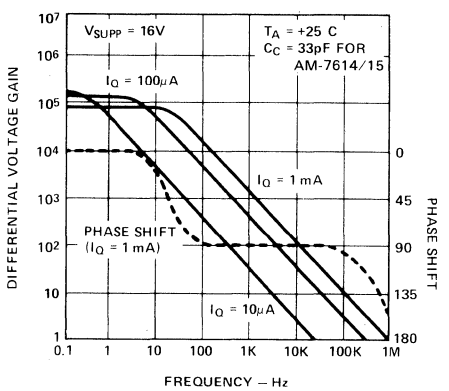
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE



LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF FREE-AIR TEMPERATURE

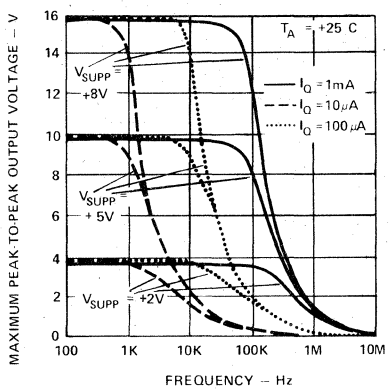


LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AND PHASE SHIFT AS A FUNCTION OF FREQUENCY

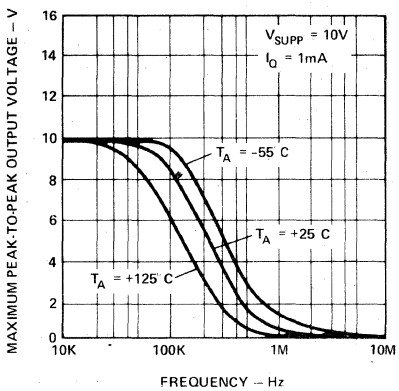


TYPICAL PERFORMANCE CURVES

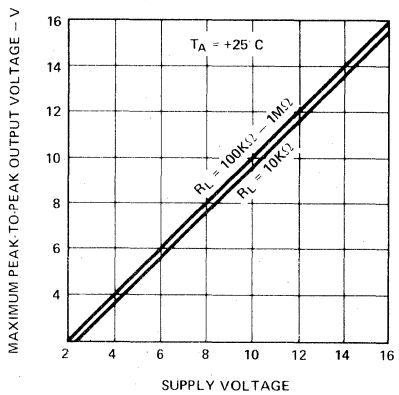
PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY



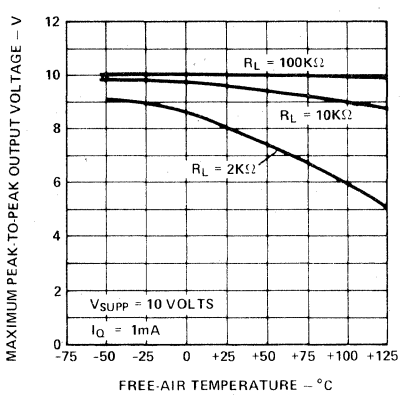
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY



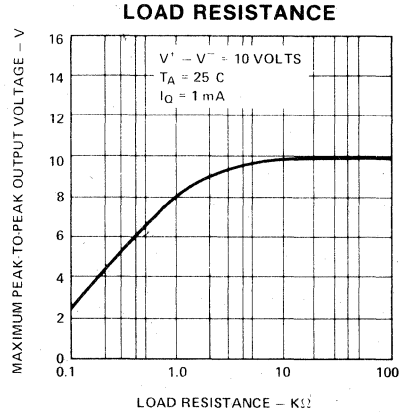
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



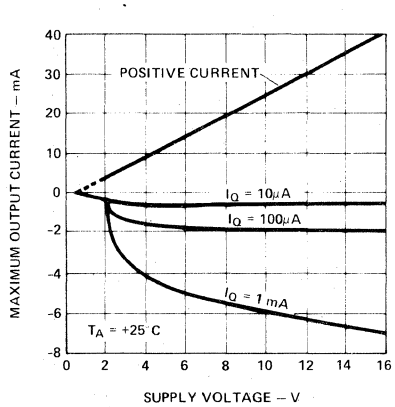
MAXIMUM PEAK-TO-PEAK VOLTAGE AS A FUNCTION OF FREE-AIR TEMPERATURE



MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF LOAD RESISTANCE



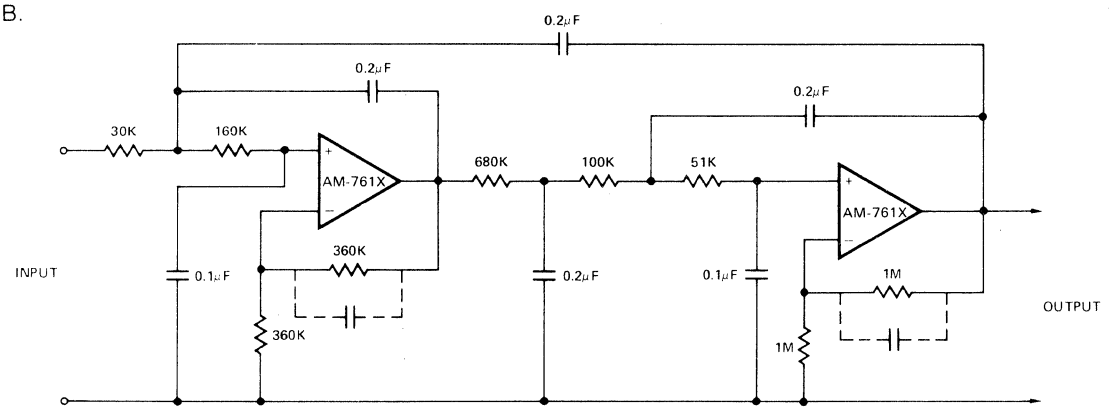
MAXIMUM OUTPUT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



APPLICATIONS

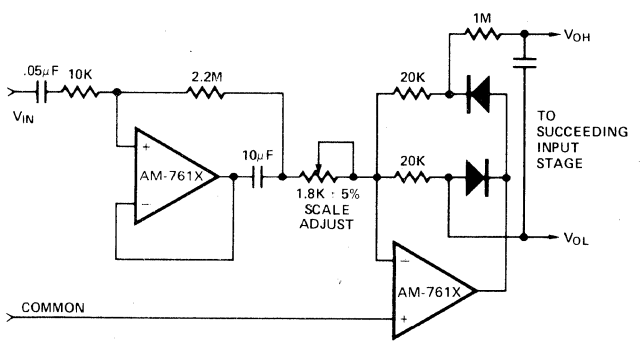
FIFTH ORDER CHEBYSHEV MULTIPLE FEEDBACK LOW PASS FILTER

The low bias currents permit high resistance and low capacitance values to be used to achieve low frequency cutoff. $f_C = 10Hz$, $A_{VOL} = 4$, Passband ripple = 0.1 dB.



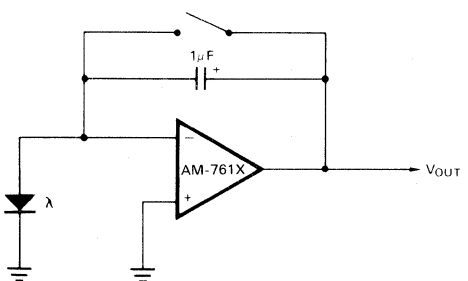
Note that small capacitors (25-50pF) may be needed for stability in some cases.

AVERAGING AC TO DC CONVERTER FOR A/D CONVERTERS SUCH AS THE ADC-7109

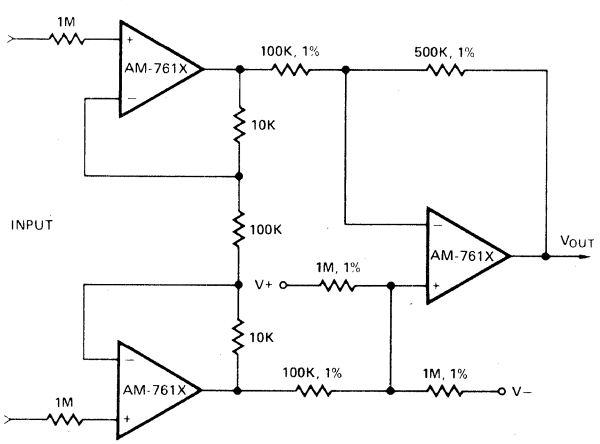


PHOTOCURRENT INTEGRATOR

Low leakage currents allow integration times up to several hours.



MEDICAL INSTRUMENT PREAMP



NOTE: Av = 25;
SINGLE NI-CAD BATTERY OPERATION.
INPUT CURRENT (FROM SENSORS CONNECTED TO PATIENT) LIMITED TO <5μA UNDER FAULT CONDITIONS.

DATEL INTERSIL
11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617)339-9341 / TWX 710-346-1953 / TLX 951340
Santa Ana, (714)835-2751, (L.A.) (213)933-7256 • Sunnyvale, CA (408)733-2424 • Gaithersburg, MD (301)840-9490
• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Ultra-Fast Microelectronic Operational Amplifiers AM-500 Series

FEATURES

- **200 nsec. Settling to .01%**
- **1000V/μsec. Slew Rate**
- **100 MHz min. Gain-Bandwidth**
- **10^6 Open Loop Gain**
- **1μV/°C Drift**
- **±50 mA Output Current**

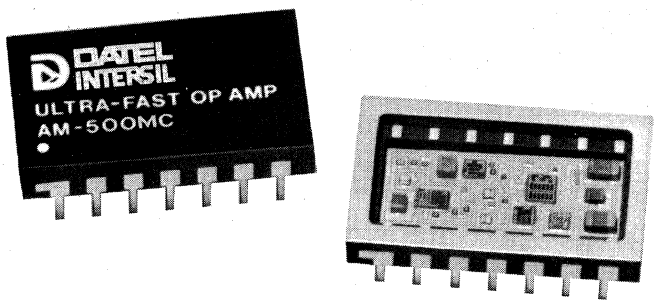
GENERAL DESCRIPTION

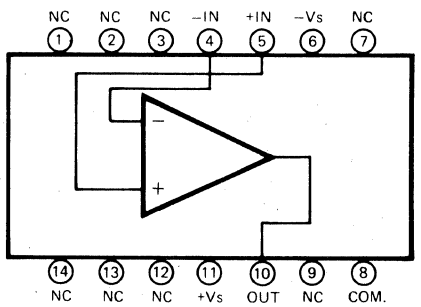
The AM-500 series amplifiers are ultra-fast settling operational amplifiers for use in inverting applications. A unique feedforward amplifier design combines the characteristics of a low drift DC amplifier with those of a very fast AC amplifier. For optimum fast settling performance, this amplifier has an open loop gain roll-off of 6 dB per octave to beyond 100 MHz. Miniature thin-film hybrid construction permits an optimum combination of semiconductor devices and minimum lead lengths to realize the amplifier circuitry. Applications for the AM-500 series include fast integrators, sample-holds, fast waveform drivers, and fast D/A converter output amplifiers.

Output settling time is 200 nanoseconds max. to .01% for a 10 volt step change. Slew rate is 1000V/μsec. for positive output transitions and 1800V/μsec. for negative transitions. This high slew rate permits undistorted reproduction of a full load, 20V peak to peak sine-wave out to 16 MHz. Gain bandwidth product is 100 MHz minimum.

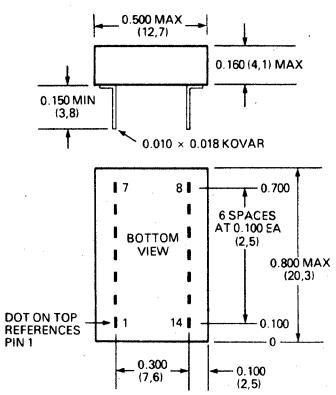
DC characteristics of the AM-500 series include a DC open loop gain of 10^6, 30 megohm input impedance, and 1 nanoampere bias current. Input offset voltage is ±0.5 mV and input offset voltage drift is 1μV/°C. Although these amplifiers do not operate differentially, a DC offset voltage in the range ±5V can be applied to the positive input terminal.

Power supply requirement is ±15VDC at 22 mA quiescent current. The amplifiers will operate over a supply range of ±10V to ±18V. Output current capability is ±50 mA with output short circuit protection. Four basic versions are available: AM-500GC and AM-500MC for 0° C to 70° C, AM-500MR for −25° C to +85° C, and AM-500MM for −55° C to +125° C. The device package is a 14 pin ceramic.





MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	N.C.
2	N.C.
3	N.C.
4	-INPUT
5	+INPUT
6	-SUPPLY
7	N.C.
8	COMMON
9	N.C.
10	OUTPUT
11	+SUPPLY
12	N.C.
13	N.C.
14	N.C.

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, AM-500 SERIES

Typical at 25° C, ±15VDC supplies, inverting operation, unless otherwise noted.

INPUT CHARACTERISTICS

Input Common Mode Voltage Range[1]	±5V
Max. Input Voltage, no damage	+18V
Differential Input Impedance	30 Meg.
Input Bias Current	1nA typ., 4nA max.
Input Offset Current	0.5nA
Input Offset Voltage	0.5mV typ., 3mV max.

OUTPUT CHARACTERISTICS

Output Voltage	+10V min.
Output Current, S.C. protected	±50mA
Stable Capacitive Load	100 pF

PERFORMANCE

DC Open Loop Gain	10^6 volts/volt
Input Offset Volt. Drift, 0° C to 70° C	1μV/° C typ., 5μV/° C max.
-25° C to +85° C	2μV/° C typ., 7μV/° C max.
-55° C to +125° C	5μV/° C typ., 10μV/° C max.
Input Bias Current Drift, -55° C to +70° C	-20pA/° C
+70° C to +125° C	doubles every 10° C
Input Voltage Noise, .01 Hz to 1Hz[2]	5μV P-P
100Hz to 10kHz[2]	1μV RMS
1Hz to 10MHz[2]	20μV RMS
Power Supply Rejection Ratio	80 dB min.

DYNAMIC CHARACTERISTICS

Gain Bandwidth Product	130MHz typ., 100 MHz min.
Slew Rate, positive going	1000V/μsec.
Slew Rate, negative going	1800V/μsec.
Full Power Frequency (20V P-P)	16MHz
Settling Time, 10V step to 1%[3]	70 nsec.
10V step to 0.1%[3]	100 nsec.
10V step to .01%[3]	200 nsec. max.
Overload Recovery Time	10μsec.

POWER REQUIREMENT

Voltage, rated performance	+15VDC
Voltage, operating	+10V to ±18VDC
Quiescent Current	22 mA

PHYSICAL-ENVIRONMENTAL

Operating Temperature Range	
AM-500GC	0° C to 70° C
AM-500MC	0° C to 70° C
AM-500MR	-25° C to +85° C
AM-500MM	-55° C to +125° C
Storage Temperature Range	-55° C to +125° C
Package Type	14 pin ceramic
Pins	0.010X0.018" Kovar
Weight	0.09 oz. (2.5g)

NOTES:
1. DC only
2. -3dB single pole bandwidth
3. 1K input and feedback resistors, 2.4pF feedback capacitor

ORDERING INFORMATION

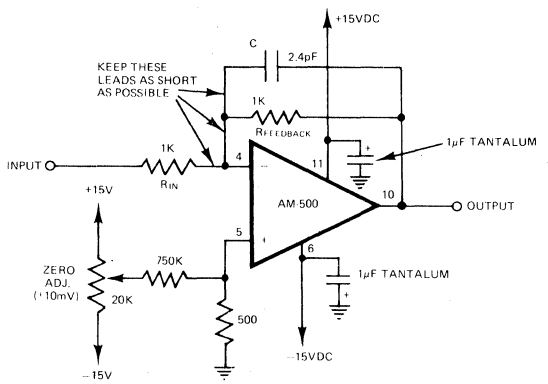
MODEL	OP. TEMP. RANGE	SEAL
AM-500GC	**0° C to 70° C**	**Epoxy**
AM-500MC	**0° C to 70° C**	**Herm.**
AM-500MR	**-25° C to +85° C**	**Herm.**
AM-500MM	**-55° C to +125° C**	**Herm.**

Socket: Standard 14 pin DIP socket. Not available from Datel-Intersil

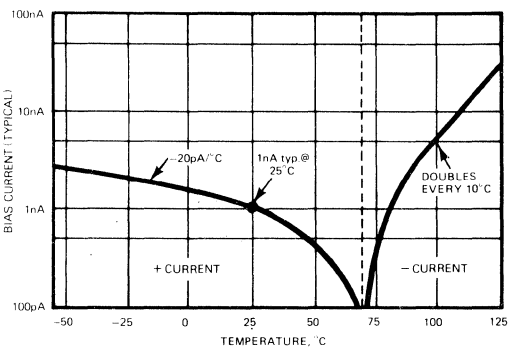
Trimming Potentiometer: TP-20K

THE AM-500 AMPLIFIERS ARE COVERED BY GSA CONTRACT

CONNECTION FOR FAST SETTLING WITH GAIN OF –1



INPUT BIAS CURRENT VS. TEMPERATURE



TECHNICAL NOTES

1. The circuit design shows the connection of the AM-500 series for fast settling operation with a closed loop gain of -1. It can be used for fast settling at closed loop gains up to -10. The equivalent resistance seen by the summing junction should be 500 ohms or less. For gains larger than -1 use an input resistor of 500 ohms and pick a feedback resistor for the required closed loop gain (1K for -2, 1.5K for -3, etc.).
2. A small feedback capacitor should be used across the feedback resistor. Determine C in picofarads from the following formula: $C = \frac{1 + |G|}{.816R}$ where G is closed loop gain and R is in kilohms.
3. Summing point leads must be kept as short as possible. Input and feedback resistors should be soldered close to the body of the resistor directly to the summing point (pin 4). Summing point capacitance to ground must be kept very low.
4. Low output impedance power supplies should be used with 1 μF tantalum bypassing capacitors at the amplifier supply terminals. There are internal .03 μF ceramic capacitors in the amplifier.
5. Although these amplifiers are inverting mode only, a DC voltage in the range of ±5V may be applied to the positive input terminal for offsetting the amplifier.

DATEL INTERSIL
11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617)339-9341 / TWX 710-346-1953 / TLX 951340
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• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Models 8510, 20, 30 Power Amplifier Motor and Actuator Driver

KEY FEATURES:

- **Capable of delivering 2.7 amps @ 24–28V d.c. operation (30V supplies)**
- **Protected against inductive kick back with internal power limiting**
- **Programmable current limiting (short circuit protection)**
- **Package is electrically isolated (allowing easy heat sinking)**
- **d.c. gain >100dB**
- **20mA typical standy quiescent current**
- **Popular 8 pin TO-3 package**
- **Internal frequency compensation**
- **Can drive up to 0.1 horsepower motors.**

DESCRIPTION:

The AM-8510/8520/8530 is a family of hybrid power amplifiers that have been specifically designed to drive linear and rotary actuators, electronic valves, push-pull solenoids, and d.c. & a.c. motors.

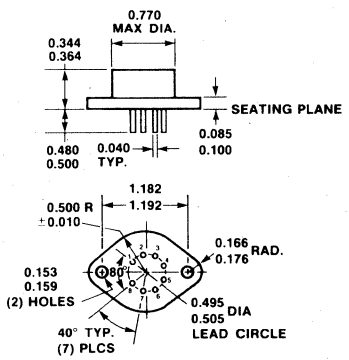
There are three models available for up to ±30V power supply operation. One model will deliver up to 2.7 amps @ 24 volt output levels, while the remaining models deliver 2 amps & 1 amp @ 24V outputs. All amplifiers are protected against shorts to ground by the addition of 2 external protection resistors.

The design uses a conventional 741 operational amplifier, a special monolithic driver chip (BL8063), NPN & PNP power transistors, and internal frequency compensating capacitors. The chips are mounted on a beryllium oxide substrate, for optimum heat transfer to the metal package; this substrate provides electrical isolation between amplifiers and metal package.

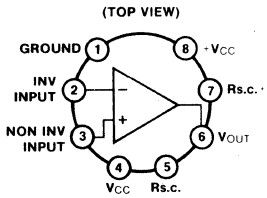
The I.C. power driver chip has built-in regulators to drive the 741 @ typically ±13v supply voltages.

PACKAGE CONFIGURATION:

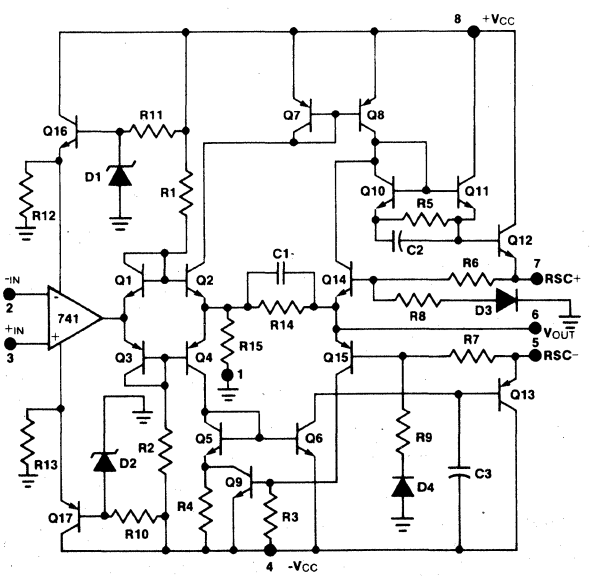
8 Lead TO-3 Metal Can



CONNECTION DIAGRAM



SCHEMATIC DIAGRAM



ORDERING INFORMATION

MODEL	OUTPUT CURRENT	OPER. TEMP. RANGE
AM-8510R	1 AMP	−25° C to +85° C
AM-8510M		−55° C to +125° C
AM-8520R	2 AMP	−25° C to +85° C
AM-8520M		−55° C to +125° C
AM-8530R	2.7 AMP	−25° C to +85° C
AM-8530M		−55° C to +125° C

AM-8510/8520/8530

ABSOLUTE MAXIMUM RATINGS @ T_A = 25°C

Supply Voltage	±35V
Power Dissipation, Safe Operating Area	See Curves
Differential Input Voltage	±30V
Input Voltage	±13V (Note 1)
Peak Output Current	See Figs. 9 & 13 (Note 2)
Output Short Circuit Duration (to ground)	Continuous (Note 2)
Operating Temperature Range	M -55°C → +125°C
	R -25°C → +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Max Case Temperature	150°C

Note 1: Rating applies to supply voltage > ± 18.

Note 2: Rating applies as long as maximum junction temperature is not exceeded (200 °C). See important note on power dissipation, page 3.

ELECTRICAL SPECIFICATIONS @ T_A = +25°C (unless stated otherwise)

		V_{CC} = ±30V		V_{CC} = ±30V		V_{CC} = ±30V	
Description	**Conditions**	**AM-8530R**	**AM-8530M**	**AM-8520R**	**AM-8520M**	**AM-8510R**	**AM-8510M**
Max. Input Offset Change/Watt of Pdiss.	Part Mtd. on Wakefield 403 Heat Sink	4mv/watt	2mv/watt	4mv/watt	2mv/watt	4mv/watt	2mv/watt
Maximum Input Offset Voltage	$R_S \leq 10K\Omega$, Pdiss. < 1 watt	±6mv	±3mv	±6mv	±3mv	±6mv	±3mv
Maximum Input Offset Current	$R_S \leq 10K\Omega$, Pdiss. < 1 watt	200na	100na	200na	100na	200na	100na
Maximum Input Bias Current	$R_S \leq 10K\Omega$, Pdiss. < 1 watt	500na	250na	500na	250na	500na	250na
Minimum Large Signal Voltage Gain	R_L=20Ω, f=10HZ $V_{OUT} \geq 67\%$ V_{CC}	100dB	100dB	100dB	100dB	100dB	100dB
Minimum Input Voltage Range		±10v	±10v	±10v	±10v	±10v	±10v
Minimum CMRR	R_S=10KΩ, f=10HZ	70dB	70dB	70dB	70dB	70dB	70dB
Minimum PSRR	R_S=10KΩ, f=10HZ	77dB	77dB	77dB	77dB	77dB	77dB
Minimum Slew Rate	C_L=30Pf, A_V=1 R_L=20Ω, $V_{OUT} \geq 67\%$ V_{CC}	0.5v/μs	0.5v/μs	0.5v/μs	0.5v/μs	0.5v/μs	0.5v/μs
Minimum Output Voltage Swing (V_{SW})	R_L=20Ω, A_V=+10 f=1KC	±25v	±25v	±26v	±26v	(R_L = 30Ω) ±26v	(R_L = 30Ω) ±26v
Minimum Output Current Capability(I_{MAX})	$V_{OUT} \geq 24v$ Note 3	2.7 amps	2.7 amps	2 amps	2 amps	1 amp	1 amp
Max. ±V_{CC} Power Supply Quiescent Current	R_L=∞, V_{IN}=0v	50ma	40ma	50ma	40ma	50ma	40ma

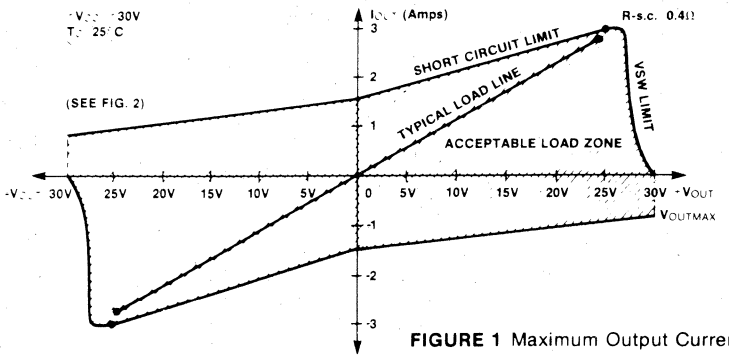
Note 3: Output current and V_{SWING} are reduced as power supplies are lowered. See Figures 1, 2, &9.

ELECTRICAL SPECIFICATIONS @ T_A = -55°C→+125°C(M) or T_A = -25°C→+85°C(R)

Maximum Input Offset Voltage	Pdiss < 1 watt	±10mv	±9mv	±10mv	±9mv	±10mv	±9mv
Maximum Input Bias Current	Pdiss < 1 watt	1.5μa	750na	1.5μa	750na	1.5μa	750na
Maximum Input Offset Current		500na	200na	500na	200na	500na	200na
Minimum Large Signal Voltage Gain	R_L=20Ω, V_{OUT}=67% V_{CC} f=10HZ; with heat sink	90dB	90dB	90dB	90dB	90dB	90dB
Minimum Output Voltage Swing	R_L = 20Ω, Pkg. Mtd. on Wakefield 403 Heat Sink	±24v	±24v	±24v	±24v	±24v	±24v
Maximum Thermal Resistance Junction to Ambient	Without Heat Sink	40° C/watt	40° C/watt	40° C/watt	40° C/watt	40° C/watt	40° C/watt
Maximum Thermal Resistance Junction to Case		2.5° C/watt	2.5° C/watt	2.5° C/watt	2.5° C/watt	3.0° C/watt	3.0° C/watt
Typical Thermal Resistance Junction to Ambient	Pkg. Mtd. on Wakefield 403 Heat Sink	4.0° C/watt	4.0° C/watt	4.0° C/watt	4.0° C/watt	4.5° C/watt	4.5° C/watt
±V_{CC} Range (typical)		±18V to ±30V	±18Vto ±30V	±18Vto ±30V	±18Vto ±30V	±18Vto ±30V	±18Vto ±30V

How To Set The Externally Programmable, Current Limiting Resistors:

The maximum output current is set by the addition of two external resistors—R+s.c. and R-s.c. Because of the INTERNAL POWER LIMITING CIRCUITRY, the maximum output current is only available when Vout is close to either power supply. As Vout moves away from ±Vcc, the maximum output current decreases in proportion to output voltage. The curve below shows maximum output current versus output voltage.



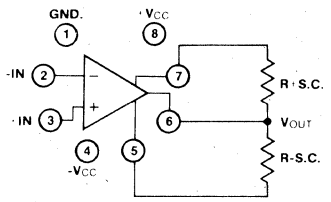


FIGURE 1 Maximum Output Current for Given Rs.c.

In general, for a given V_{OUT}, Isc limit, and case temperature T_C, Rs.c. can be calculated from the equation below (V_{OUT} in Volts):

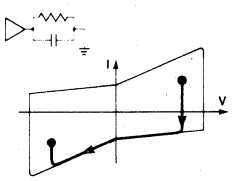
$$\text{Rs.c.} = \frac{[600 + (24 \times V_{OUT}) - 2.2\ (T_C - 25°\ C)]\ \text{mV}}{\text{Isc limit}}$$

i.e., If Iout (maximum) = 1.5 amps @ Vout = 25V, T_C = 25° C

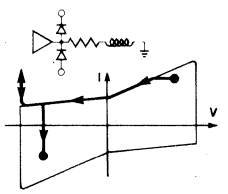
$$\text{Rs.c.} = \frac{1200\ \text{mV}}{1.5\ \text{amps}} = 0.8\Omega$$

When an Rs.c. = 0.8Ω is used, Iout @ Vout = OV will be reduced to 750 mA. Except for small changes in the "Vsw Limit" area, the effects of changing Rs.c. on the I_{OUT} vs V_{OUT} characteristics can be determined by merely changing the I_{OUT} scale on Fig. 1 to correspond to the new value. Changes in T_C move the limit curve bodily up and down.

This INTERNAL POWER LIMITING CIRCUITRY however does not at all restrict the normal use of the driver. For any normal load, the static load line will be similar to that shown in Figure 1. Clearly, as V_{OUT} decreases, the I_{OUT} requirement falls also, more steeply than the I_{OUT} available. For reactive loads, the dynamic load lines are more complex. Two typical operating point loci are sketched here:



Capacitive Load



Inductive Load
(Note catch diode)

Thus the limiting circuitry protects the load and avoids needless damage to the driver during abnormal conditions. For any 24Vdc-28Vdc motor/actuator, the Rs.c. resistors must be calculated to get proper power delivered to the motor (up to a maximum of 2.7 amps) and ±Vcc set at ±30V. For lower supply and/or output voltages, the maximum output current will follow graphs of Figures 1 and 10.

IMPORTANT NOTE ON POWER DISSIPATION OF POWER AMPLIFIER

The steady state power dissipation equation is:

$$P_{diss\ max} = \frac{T_{JMAX} - T_{AMB}}{\Theta_{JC} + \Theta_{CH} + \Theta_{HA}}$$

Where:

T_{JMAX} = Maximum junction temperature
T_{AMB} = Ambient temperature
Θ_{JC} = Thermal resistance from transistor junction to case of package
Θ_{CH} = Thermal resistance from case to heat sink
Θ_{HA} = Thermal resistance from heat sink to ambient air

Now:

T_{JMAX} = 200° C for silicon transistors
$\Theta_{JC} \cong$ 2.0 C/WATT for a steel bottom TO-3 package with die attachment to beryllia substrate to header
Θ_{CH} = .045° C/W for 1mil thickness of Wakefield type 120 thermal joint compound.
.09° C/W for 2mil thickness of type 120
.13° C/W for 3mil thickness of type 120
.17° C/W for 4mil thickness of type 120
.21° C/W for 5mil thickness of type 120
.24° C/W for 6mil thickness of type 120

Θ_{HA} The choice of heat sink that a user selects depends upon the amount of room available to mount the heat sink. A sample calculation follows: by choosing a Wakefield 403 heat sink, with free air, natural convection (no fan). $\Theta_{HA} \cong$ 2.0° C/W. Using 4 mil joint compound,

$$\therefore P_{diss\ MAX} = \frac{200°\ C - T_{AMB}}{2.0°\ C/W + .17°\ C/W + 2.0°\ C/W}$$

$$= \frac{200°\ C - T_{AMB}}{4.17°\ C/W}$$

$$\therefore P_{diss\ MAX}\ \text{at}\ T_{AMB} = 25°\ C = \frac{200°\ C - 25°\ C}{4.17°\ C/W} = 42\ \text{watts}$$

$$P_{diss\ MAX}\ \text{at}\ T_{AMB} = 125°\ C\ \text{is}\ \frac{200°\ C - 125°\ C}{4.17°\ C/W} = 18\ \text{watts}$$

From Fig. 2 the worst case steady state power dissipation for an AM-8520 (R_{SC} = 0.6Ω) are about 30 W and 18 W respectively. Thus this heat sink is adequate. The AM-8530 (R_{SC} = 0.4Ω) would need a bigger heat sink (or a blower) giving about 1° C/W for Θ_{CA} to maintain satisfactory junction and case temperatures with 25 W dissipation and T_{AMB} = 125° C.

TYPICAL PERFORMANCE CURVES

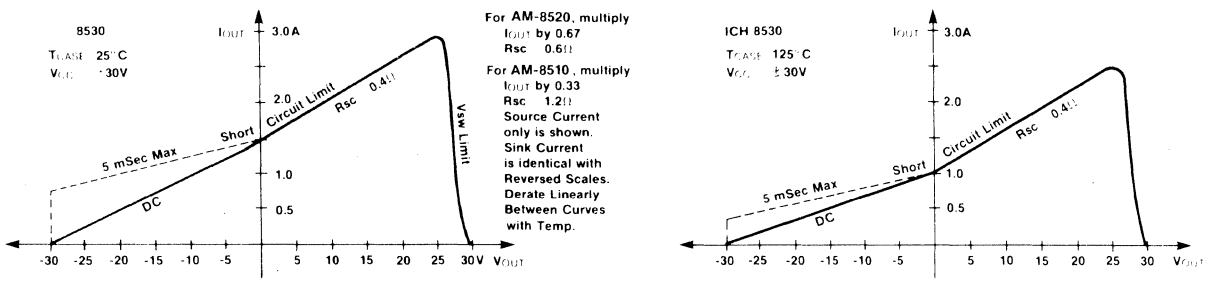


Figure 2: Safe Operating Area; I_{OUT} vs V_{OUT} vs T_C

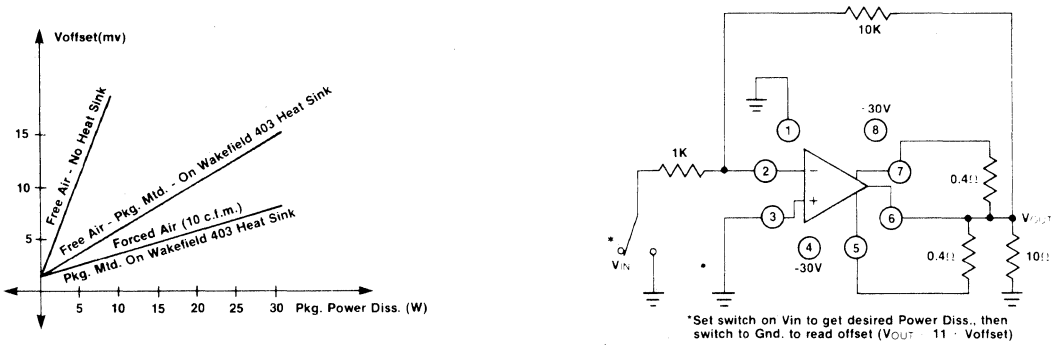


Figure 3: Input Offset Voltage vs Power Dissipation

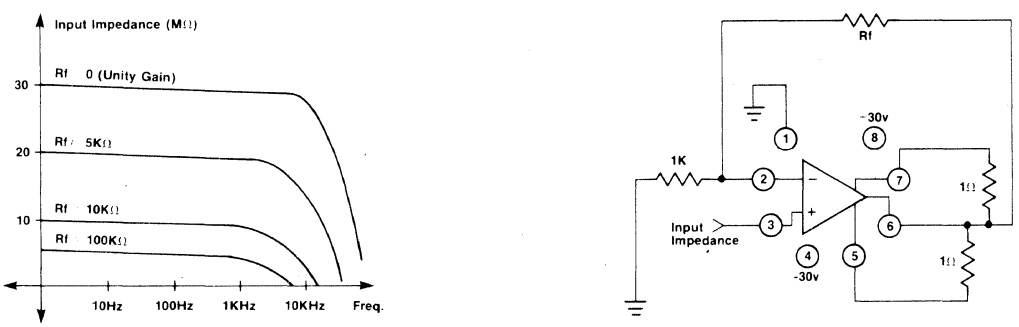


Figure 4: Input Impedance vs Gain vs Frequency

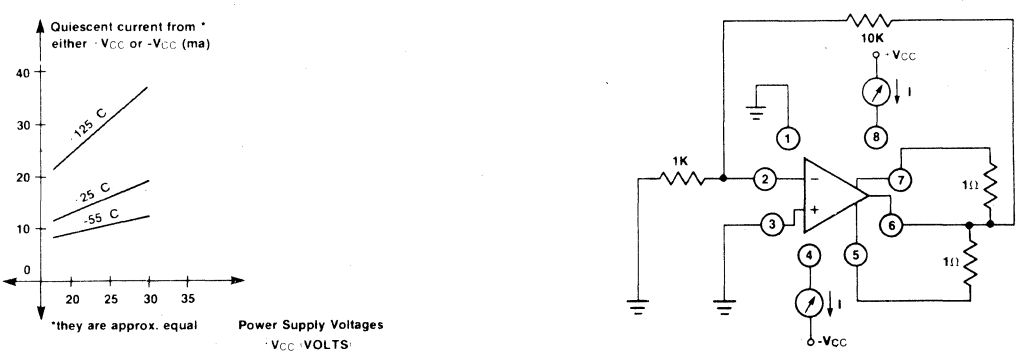


Figure 5: Quiescent Current vs Power Supply Voltage

TYPICAL PERFORMANCE CURVES, CONTINUED.

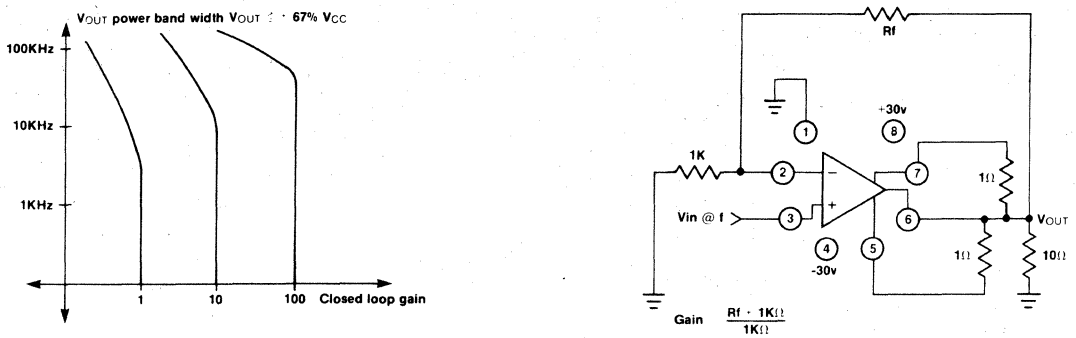


Figure 6: Large Signal Power Band Width

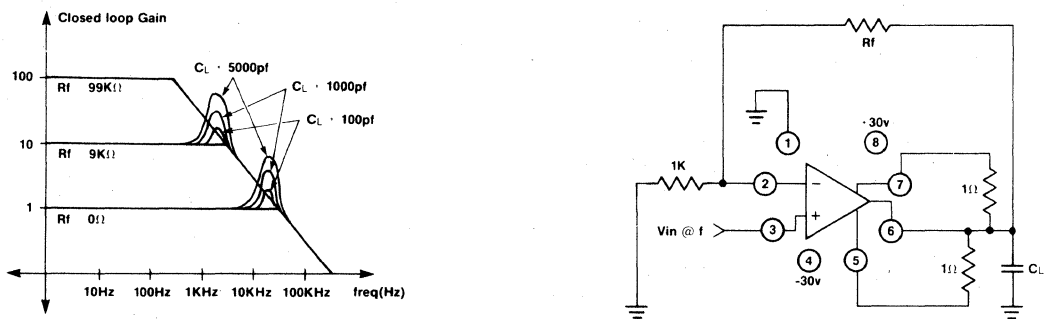


Figure 7: Small Signal Frequency Response

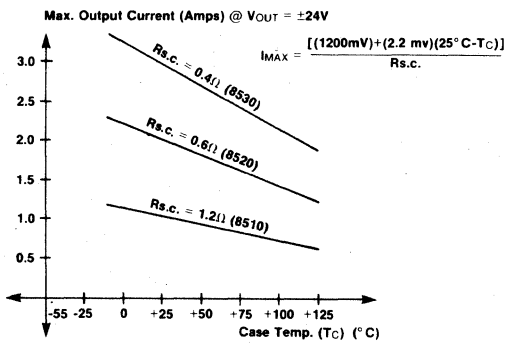


Figure 8: Maximum Output Current vs. Case Temperature

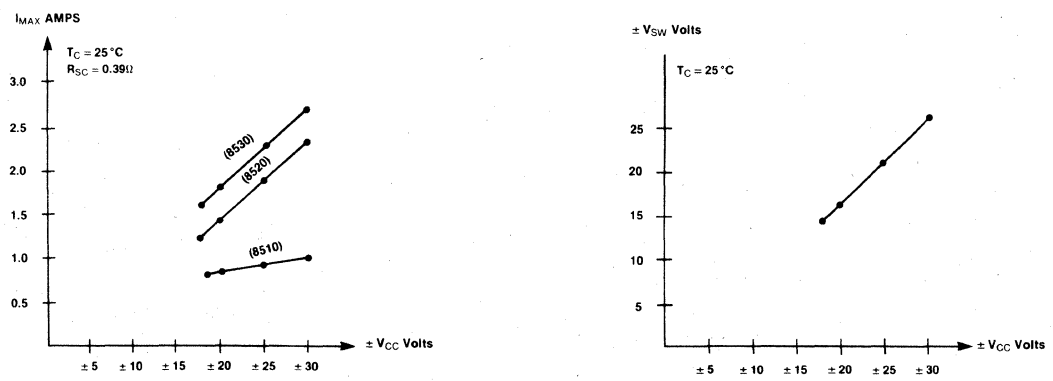


Figure 9: Maximum Output Current and Voltage vs. V_{CC}

BRIEF APPLICATION NOTES

The maximum input voltage range, for $\pm V_{CC} > \pm 18V$, is substantially less than the available output voltage swing. Thus non-inverting amplifiers, as in Figure 11, should always be set up with a gain greater than about 2.5, (with $\pm 30V$ V_{CC}), so that the full output swing is available without hazard to the input. At first sight, it would seem that no restrictions would apply to inverting amplifiers, since the inputs are virtual ground and ground. However, under fault (output short-circuited) or high slew conditions, the input can be substantially removed from ground. Thus for inverting amplifiers with gains less than about 5, some protection should be provided at this input. A suitable resistor from the input to ground will provide protection, but also increases the effect of input offset voltage at the output. A pair of diodes, as shown in Figure 12, has no effect on normal operation, but gives excellent protection.

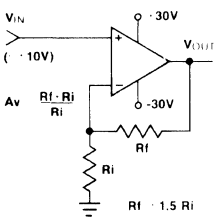


Figure 10:
Non-Inverting Amplifier

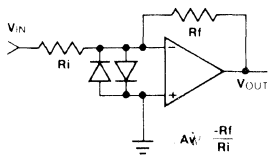


Figure 11:
Inverting Amplifier

Power dissipation is another important parameter to consider. The current protection circuit protects the device against short circuits to ground, (but only for transients to the opposite supply) provided the device has adequate heat sink. A curve of power dissipation vs V_{OUT} under short circuit conditions is given in Figure 13. The limiting circuit is more closely dependent on case temperature than (output transistor) junction temperatures. Although these operating conditions are unlikely to be attained in actual use, they do represent the limiting case a heat sink must cope with. For fully safe design, the anticipated range of V_{OUT} values that could occur, (steady state, including faults) should be examined for the highest power dissipation, and the device provided with a heat sink that will keep the junction temperature below 200° C and the case temperature below 150° C with the worst case ambient temperature expected.

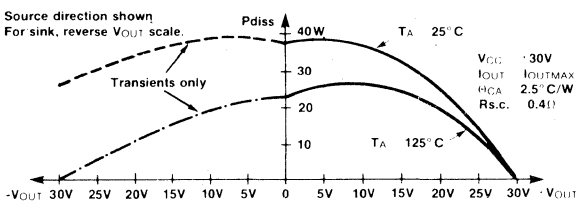


Figure 12: Power Dissipation under Short Circuit Conditions

TYPICAL APPLICATIONS

I. Actuator Driving Circuit (24→28Vd.c. rated)

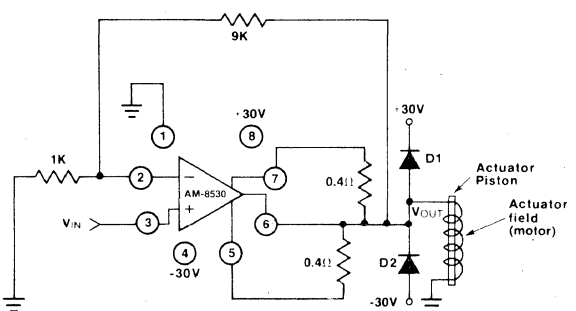


Figure 13: Power Amp Driving Actuator

The gain of the circuit is set to +10, so a +2.4V input Vin will produce a +24V output (and will deliver up to 2.7 amps output current). To reverse the piston travel, invert Vin to −2.4V and Vout will go to −24V. Diodes D1 and D2 absorb the inductive kick of the motor during transients (turn-on or turn-off); their breakdown should exceed 60V.

II. Obtaining Up To 5 Amps Output Current Capability By Paralleling Amplifiers

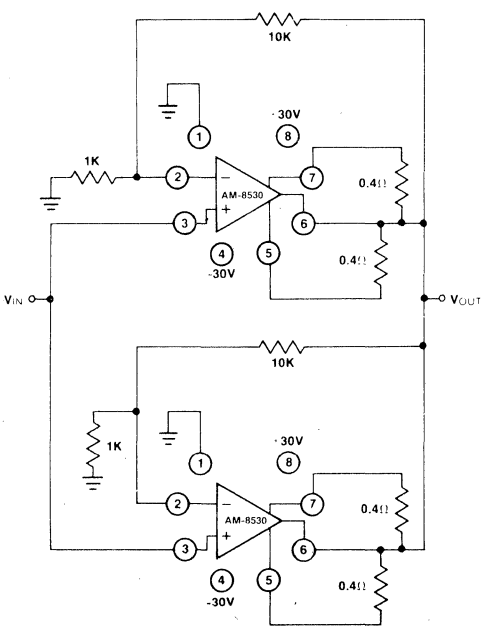


Figure 14: Paralleling Power Amps for Increased Current Capability

This paralleling procedure can be repeated to get any desired output current. However, care must be taken to ensure that enough load is provided to avoid the amplifiers pulling against each other.

III. Driving A 48VDC Motor

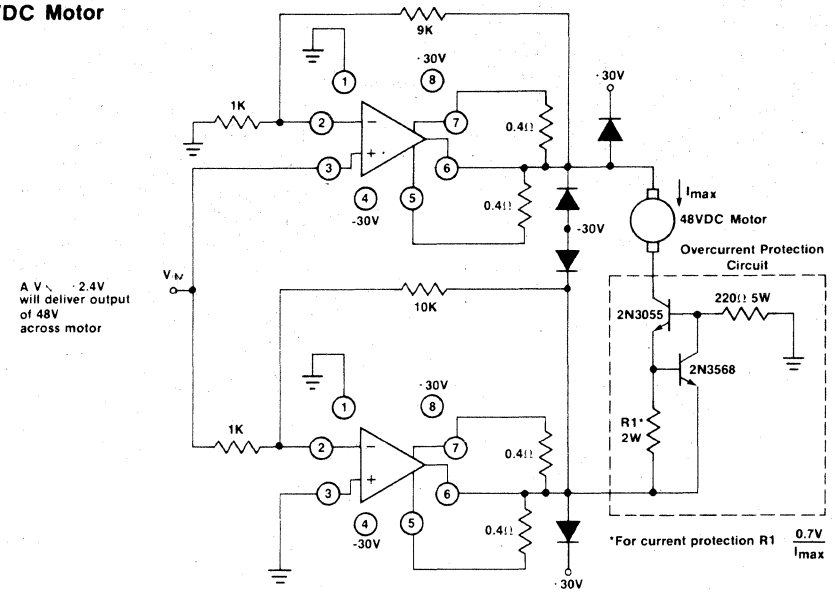


Figure 15: Power Amp Driving 48 VDC Motor

IV. Precise Rate Control of an Electronic Valve

To get very fine control of the opening of an orifice, driven by an electronic valve, there are two ways to go.

1. Keep the voltage constant, i.e., 24Vdc or 12Vdc, and vary the time the voltage is applied, i.e., if it takes five seconds to completely open an orifice at 24Vdc, then applying 24V for only 2-1/2 seconds opens it only 50%.
2. Simply vary the d.c. driving voltage to valve. Most valves obtain full opening as an inverse of applied voltage., i.e., valves opens 100% in five seconds at 24Vdc and in 10 seconds at 12Vdc.

A circuit to perform the second method is shown below; the advantage of this is that digit switches can precisely set driving voltage to 0.2% accuracy (8-bit DAC), thereby controlling the rate at which the valve opens.

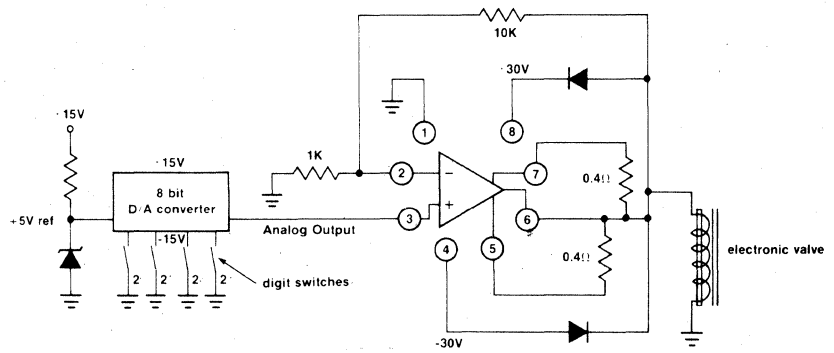


Figure 16: Digitally Controlled Electronic Value

V. The circuit presented in IV is also an excellent way to get a precise power supply voltage; in fact, a precision, variable power supply can be made. Using a BCD coded DAC with BCD Thumbwheel switches.

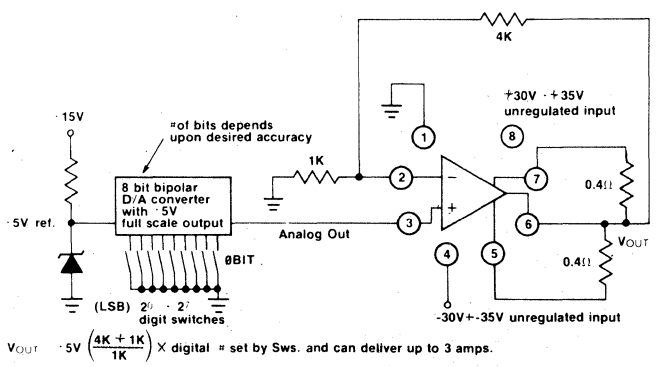


Figure 17: Digitally Programmable Power Supply

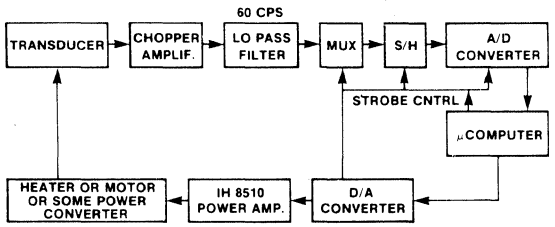
2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	Ø BIT	Vout
1	1	1	1	1	1	1	1	1	+25Vd.c.
1	1	1	1	1	1	1	1	0	-25Vd.c.
0	1	0	1	1	0	0	1	1	+15Vd.c.
0	1	0	1	1	0	0	1	0	-15Vd.c.
1	0	0	0	0	0	0	0	1	+0.098Vd.c.
1	0	0	0	0	0	0	0	0	-0.098Vd.c.

Etc.

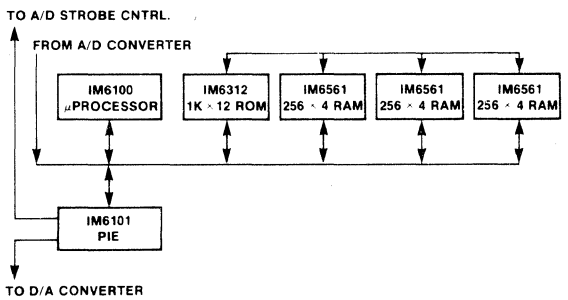
The power supply can be set to ±0.1Vd.c.

VI. There is great power available (no pun intended) in the sub-systems shown in IV and V; there the D/A converter is shown being set manually (via digit switches) to get a precise analog output (binary # × full scale voltage), then the driver amplifier multiplies this voltage to produce the final output voltage. It seems obvious that the next logical step is to let a microprocessor (local) or C.P.U. program the D/A converter. Then total, pre-programmable, electronic control of an actuator, electronic valve, motor, etc., is obtained. This would be used in conjunction with a transducer/multiplex system for electronic monitoring and control of any electro-mechanical function.

ELECTRONIC CONTROL SYSTEM:



MUX = MX SERIES
S/H (SAMPLE & HOLD) = SHM-LM2
D/A CONVERTER = DAC-7520
POWER AMP = AM-8510/8520/8530
A/D CONVERTER = ADC-6108A/7104
μ COMPUTER = IM6100 family:



NOTE. This product contains Beryllia. If used in an application where the package integrity may be breached and the internal parts crushed or machined, avoid inhalation of the dust.

Fast, High Voltage FET Operational Amplifiers AM-303 Series

FEATURES

- ±140V Output Swing
- 10 MHz Gain Bandwidth
- 2.5 μsec. Settling Time
- 100V/μsec. Slew Rate
- 100 dB CMRR
- Output Current Limiting

GENERAL DESCRIPTION

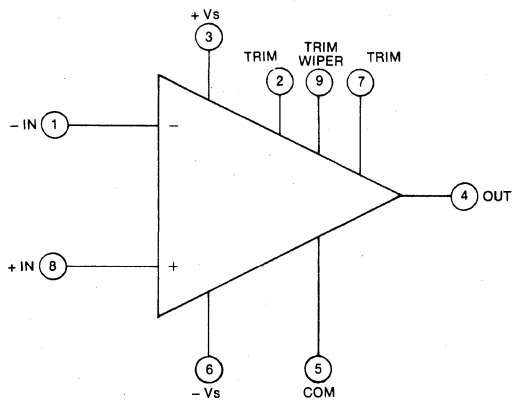
Datel-Intersil's AM-303 series are FET input operational amplifiers which feature a combination of high voltage operation and very fast response. With a power supply of ±150V the output voltage swings ±140V at ±25mA output current. The supply voltage can range from ±15V to ±150V with the output voltage capability 10V less than the supply voltage. A unique output current limiting circuit protects the output of the amplifier by means of voltage and temperature dependent limiting.

Common mode input voltage range is ±140V with a common mode rejection ratio of 100 dB minimum. The input offset voltage drift is ±50 μV/°C max. for the AM-303A and ±20 μV/°C max. for the AM-303B. Input impedance is 10^{12} ohms with bias current of 300 pA max. and open loop gain is 10^6 volts per volt minimum.

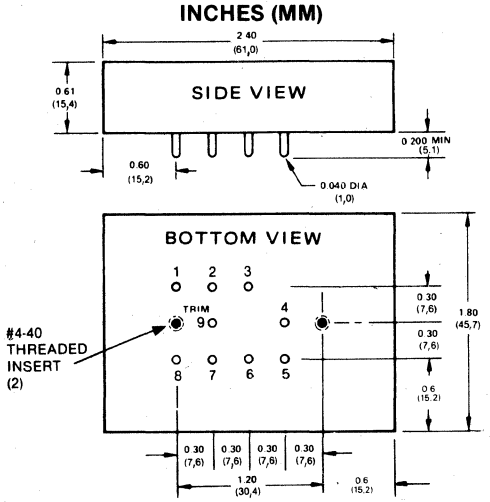
Dynamic characteristics include a typical gain bandwidth product of 10 MHz and a slew rate exceeding 100V/μsec. Settling time to 0.01% for a 10V step is 2.5 μsec.

The AM-303 amplifiers are completely encapsulated and have an aluminum bottom plate to permit external heat sinking for efficient heat removal. Although convection cooling is sufficient for most applications, heat sinking should be employed when operating near maximum output capability or when driving capacitive loads at high speed. Two 4-40 screw inserts in the bottom plate permit easy mounting.

The AM-303 devices are ideal for electron beam deflectors, beam intensity modulators and other high voltage applications. The AM-303 replaces both of Datel-Intersil's earlier AM-301 and AM-302 amplifiers.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	- IN
2	TRIM
3	+ Vs
4	OUT
5	COM
6	- Vs
7	TRIM
8	+ IN
9	TRIM (WIPER)

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, AM-303 SERIES

Typical at 25°C, ±150V Supplies unless otherwise noted.

MAXIMUM RATINGS	
Power Supply Voltage	±150V
Output Voltage	±140V
Common Mode Input Voltage	$\pm V_S$
Differential Input Voltage	$\pm V_S$
INPUT CHARACTERISTICS	
Common Mode Voltage Range	$\pm(V_S\text{-}10)$
Common Mode Input Impedance	10^{12} Ohms // 5 pF
Differential Input Impedance	10^{12} Ohms // 7 pF
Input Bias Current	300 pA max.
Input Offset Voltage[1]	±1 mV max.
OUTPUT CHARACTERISTICS	
Output Voltage	$\pm(V_S\text{-}10)$, ±140V max.
Output Current, S.C. Protected[2]	±25 mA min.
Capacitive Load	100 pF max.
PERFORMANCE	
DC Open Loop Gain	10^6 V/V min.
Input Offset Voltage Drift	
AM-303A	±50 μV/°C max.
AM-303B	±20 μV/°C max.
Input Bias Current Drift	Doubles every 10°C
Common Mode Rejection Ratio[3]	100 dB min.
Input Voltage Noise[4]	
.01 Hz to 10 Hz	5 μV P-P
10 Hz to 10 KHz	3 μV RMS
Power Supply Rejection Ratio	5 μV/V
DYNAMIC CHARACTERISTICS	
Gain Bandwidth Product	10 MHz typ., 5 MHz min.
Settling Time to 0.01%[5]	2.5 μsec.
Slew Rate	100V/μsec. min.
Full Power Output Frequency	150 KHz min.
POWER REQUIREMENT	
Power Supply Voltage Range	±15V to ±150V
Quiescent Current	±12 mA max.
PHYSICAL-ENVIRONMENTAL	
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−55°C to +125°C
Package Size	1.8 x 2.4 x 0.61 inches (45.7 x 61.0 x 15.4 mm)
Case Material	Black Diallyl Phthalate Per MIL-M-14
Pins	0.040" Round, Gold Plated 0.250" Long min.
Bottom Cover	Black Anodized Aluminum for Heat Conduction
Weight	2.5 oz. (71g.)

NOTES:

1. Adjustable to zero
2. For current limiting characteristics see Technical Note 1 and graph.
3. Measured at DC
4. −3 dB single pole bandwidth
5. For 10V output change at gain of −1.

ORDERING INFORMATION

MODEL	INPUT OFFSET DRIFT, MAX.
AM-303A	50 μV/°C
AM-303B	20 μV/°C

Mating Socket: MS-11
Trimming Potentiometer: TP100

THESE AMPLIFIERS ARE COVERED BY GSA CONTRACT

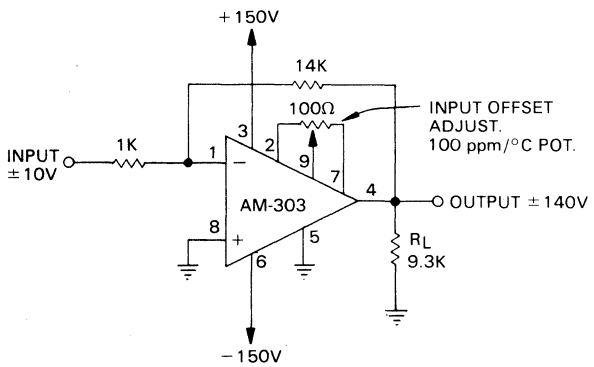
APPLICATION

1. The output circuit of the AM-303 employs both voltage dependent and temperature dependent output current limiting to protect the output stage from excessive dissipation or second breakdown. The limiting depends on the + supply voltage minus the output voltage for sourcing and the − supply voltage plus the output voltage for sinking. See the figure below. The useful output current is approximately 40% less than the limiting current shown in the graph.

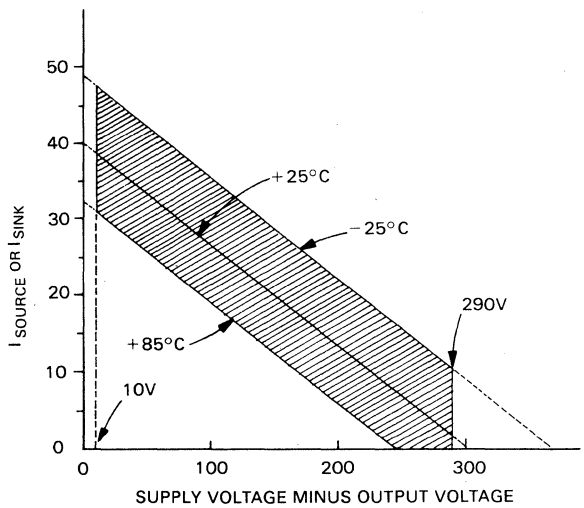
2. In low closed loop gain configurations, use a small adjustable compensating capacitor across the feedback resistor. A 3 to 30 pF value will permit adjustment of the step response for optimum settling time.

3. When operating near maximum output current, the amplifier should be mounted on a metal heat sink using conductive silicone grease. The bottom of the AM-303 case is an anodized aluminum plate to give efficient heat conduction.

CONNECTION FOR GAIN OF −14 and ±140V OUTPUT



AM-303 OUTPUT CURRENT LIMITING CHARACTERISTIC



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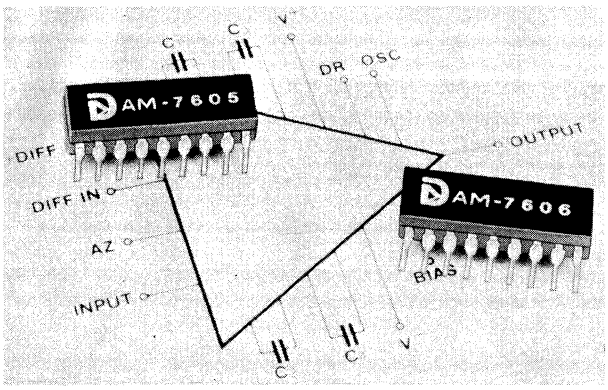
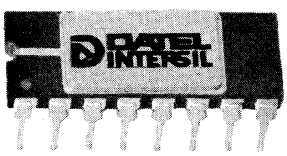
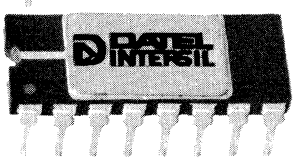
• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Instrumentation Amplifiers







Quick Selection:
Instrumentation Amplifiers

MODEL	DESCRIPTION	GAIN RANGE	GAIN NON-LINEARITY	GAIN TEMPCO	INPUT IMPEDANCE	INPUT BIAS CURRENT	INPUT OFFSET CURRENT	INPUT OFFSET VOLTAGE
AM-435-1C	Low	1 to 1000	0.1%	±3 ppm/°C	$2 \times 10^{12}\Omega$	40 pA	20 pA	±30mV
AM-435-1M	Cost		0.05%			20 pA	10 pA	±15mV
AM-7605C	CAZ							
AM-7605R	Amplifier	1 to 1000	—	—	—	1.5 nA	150 pA	±5mV
AM-7605M	Compensated							
AM-7606C	CAZ							
AM-7606R	Amplifier	1 to 1000	—	—	—	1.5 nA	150 pA	±5mV
AM-7605M	Uncompensated							
AM-542AC								
AM-542AR		1 to 1024	0.01%	±10 ppm/°C	$1.2 \times 10^{9}\Omega$	±14 nA	12 nA	±200 μV
AM-542AM	Digitally							
AM-542BC	Programmable							
AM-542BR	Gain,	1 to 1024	0.01%	±10 ppm/°C	$1.2 \times 10^{9}\Omega$	±14 nA	12 nA	±200 μV
AM-542BM	Low							
AM-542CC	Drift							
AM-542CR		1 to 1024	0.01%	±10 ppm/°C	$1.2 \times 10^{9}\Omega$	±14 nA	12 nA	±200 μV
AM-542CM								
AM-543AC	Digitally							
AM-543AR	Programmable	1 to 1024	0.01%	±15 ppm/°C	$10^{12}\Omega$	±100 pA	20 pA	±1mV
AM-543AM	Gain							
AM-201A						±50 nA	2.5 nA	Adj.
AM-201B	High Performance	1 to 1000	0.01%	±20 ppm/°C	$10^{9}\Omega$	±25 nA	1 nA	to
AM-201C						±25 nA	1 nA	Zero

NOTES:
1. G = 1000
2. 10V to 0.1%, G = 1
3. 20V to 0.01%, G = 1
4. 10V to 0.01%, G = 1000

These products are covered by GSA contract.

INPUT OFFSET VOLTAGE DRIFT	SLEW RATE	SETTLING TIME	BANDWIDTH	COMMON MODE REJECTION[1]	POWER REQUIREMENT	PACKAGE	OPERATING TEMP. (°C)	PRICE (SINGLES)	SEE PAGE
± 10μV/°C	1V/μsec	15μsec[2]	7 KHz[1]	105dB	± 15V	16 Pin Ceramic DIP	0 to +70	$ 12.00	366C
				115dB			−55 to +125	$ 28.50	
0.1μV/°C	—	—	20 Hz	104dB	± 5V	18 Pin Cerdip	0 to +70	$ 22.58	368C
							−25 to +85	$ 33.83	
							−55 to +125	$ 67.58	
0.1μV/°C	—	—	20 Hz	104dB	± 5V	18 Pin Cerdip	0 to +70	$ 22.58	368C
							−25 to +85	$ 33.83	
							−55 to +125	$ 67.58	
10μV/°C	.14V/μsec	160μsec[3]	—	120dB	± 15V + 5V	24 Pin Ceramic DIP	0 to +70	Contact Factory	378C
							−22 to +85		
							−55 to +125		
5μV/°C	.14V/μsec	160μsec[3]	—	120dB	± 15V + 5V	24 Pin Ceramic DIP	0 to +70	Contact Factory	378C
							−25 to +85		
							−55 to +125		
2μV/°C	.14V/μsec	160μsec[3]	—	120dB	± 15V + 5V	24 Pin Ceramic DIP	0 to +70	Contact Factory	378C
							−25 to +85		
							−55 to +125		
15μV/°C	3.3/Vμsec	10μsec[3]	—	100dB	± 15V + 5V	24 Pin Ceramic DIP	0 to +70	Contact Factory	378C
							−25 to +85		
							−55 to +125		
± 1μV/°C	1V/μsec	20μsec[4]	45 KHz	100dB	± 15V	1.5 x 1.5 x 0.375 (38 x 38 x 10)	0 to +70	$ 84.00	382C
± 0.5μV/°C				106dB				$ 94.00	
± 0.25μV/°C				114dB				$105.00	

THESE PRODUCTS ARE COVERED BY GSA CONTRACT

Monolithic Precision Instrumentation Amplifier Model AM-435

FEATURES

- **1 to 1000 Gain Range**
- **3 pA typ. Bias Current**
- **2 × 10^{12} Input Z**
- **110 dB min. CMRR**
- **Low Power**
- **Low Cost**

GENERAL DESCRIPTION

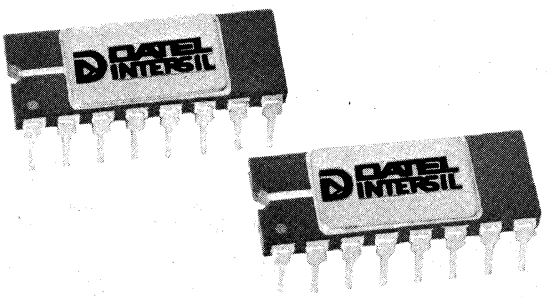
The AM-435 is a monolithic JFET input instrumentation amplifier. Designed as a high impedance, differential gain block, the unit accurately amplifies the voltage difference between the inputs. Common mode noise on the input line is rejected by the unit's high CMRR. The resultant signal is then transferred into a single-ended output, thus eliminating ground loops.

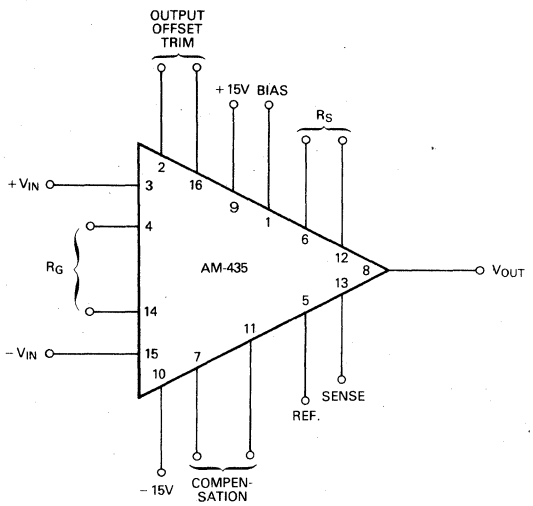
The amplifier's transfer function is set by two external resistors. The AM-435 utilizes internal differential current feedback eliminating the need for precision feedback resistors. The amplifier's gain can be easily adjusted for gains of 1 to 1000 by changing the value of one of the resistors. The AM-435 has a typical gain nonlinearity of 0.02%. The initial input offset voltage is 8mV for the "M" version and 15mV for the "C", with extremely low bias currents of 20pA and 40pA respectively.

The unique two stage amplifier design makes it possible to trim out any input offset errors which would otherwise be amplified by the closed loop gain. Output offset nulling can be achieved with a single optional trimming potentiometer.

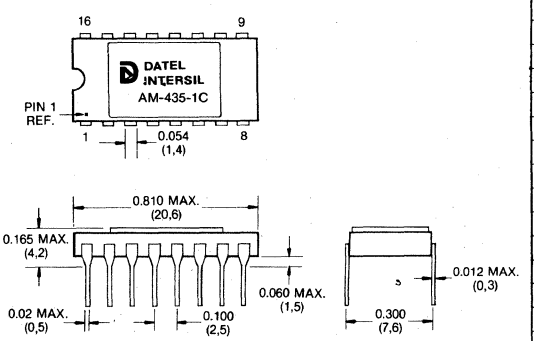
The AM-435 offers a low cost solution for data acquisition applications. These easy to use components offer design engineers an alternative to both modular and inhouse designs. The device is commonly used as a transducer amplifier for thermocouples, strain gauge bridges, RTD's, current shunts, biological amplifiers, or simply as preamplifiers for processing small differential signals superimposed on common mode voltages.

The instrumentation amplifiers are packaged in 16-pin DIP packages. The operating temperature range of the AM-435-1C is 0 to + 70°C while the AM-435-1M operates from – 55°C to + 125°C. Power supply requirement is ± 5V to ± 20V. The maximum power dissipation for the "C" version is 54mW and for the "M", 45 mW.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	BIAS
2	OUTPUT TRIM
3	+ V_{IN}
4	R_G
5	REFERENCE
6	R_S
7	COMPENSATION
8	OUTPUT
9	+ 15V DC
10	– 15V DC
11	COMPENSATION
12	R_S
13	SENSE
14	R_G
15	– V_{IN}
16	OUTPUT TRIM

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, AM-435-1C and AM-435-1M
(Typical at 25°C, ± 15V supplies, R_L = 10K unless otherwise noted)

	AM-435-1C	AM-435-1M
MAXIMUM RATINGS		
Positive Supply, pin 9	+ 18V	+ 22V
Negative Supply, pin 10	− 18V	− 22V
Differential Input Voltage	± 36V	± 44V
Input Voltage Range	± 18V	± 22V
GAIN		
Gain Range	1 to 1000	1 to 1000
Gain Equation	R_S / R_G	R_S / R_G
Gain Equation Error, max[1]	0.2%	0.1%
Gain Nonlinearity	0.1% max.	0.5% max.
INPUT CHARACTERISTICS		
Common Mode Voltage Range	± 12V	± 12V
Input Impedance	2×10^{12} ohms	2×10^{12} ohms
Input Capacitance	2.5pF	2.5pF
Input Bias Current, max.	40pA	20pA
Input Offset Current, max.	20pA	10pA
Input Offset Voltage	± 15mV	± 8mV
CMRR, DC to 60 Hz[2]		
G = 1, dB min.	65 (80 typ.)	75 (85 typ.)
G = 10, dB min.	85 (100 typ.)	95 (105 typ.)
G = 100, dB min.	100 (120 typ.)	110 (125 typ.)
G = 1000, dB min.	105 (120 typ.)	115 (125 typ.)
OUTPUT CHARACTERISTICS		
Output Voltage Range	± 10V min.	± 10V min.
Output Current S.C. prot.	± 5mA	± 5mA
Output Resistance, G = 1	1.5 ohms	1.2 ohms
Output Offset Voltage[3]	± 400mV max.	± 200mV max.
DRIFT ERRORS AND NOISE		
Gain Tempco	± 3ppm/°C	± 3ppm/°C
Input Bias Current Drift	× 2 / 10°C	× 2 / 10°C
Input Offset Current Drift	1.5pA/°C	3pA/°C
Input Offset Voltage Drift	10μV/°C	10μV/°C
Output Offset Volt. Drift	600μV/°C	600μV/°C
Power Supply Rej., G = 1000	100 dB	100 dB
Input Voltage Noise,		
0.1 Hz to 10 Hz, μV p-p	1.3 + 670 / G	1.3 + 670 / G
10 Hz to 10 kHz, μV RMS	8 + 450 / G	8 + 450 / G
DYNAMIC RESPONSE		
Small Sig. Bandwidth, ± 3dB		
G = 1	140 kHz	140 kHz
G = 10	50 kHz	50 kHz
G = 100	30 kHz	30 kHz
G = 1000	7 kHz	7kHz
Slew Rate	1V/μsec.	1V/μsec.
Full Power Bandwidth	25 kHz	25 kHz
Settling Time to 0.1%,		
G = 1 to 10	15 μsec.	15 μsec.
G = 100	40 μsec.	40 μsec.
G = 1000	200 μsec.	200 μsec.
POWER REQUIREMENT		
Voltage, Rated Performance	± 15V	± 15V
Voltage Range, Operating	± 5V to ± 18V	± 5V to ± 20V
Supply Current	1.8mA max.	1.5mA max.
PHYSICAL ENVIRONMENTAL		
Operating Temp. Range	0 to + 70°C	− 55°C to + 125°C
Storage Temp. Range	− 65°C to + 150°C	− 65°C to + 150°C
Package Type	16 Pin DIP	16 Pin DIP

NOTES: 1. For gain range of 1 to 100, typical error is 0.05%.
2. 1K source unbalance. 3. Can be adjusted to zero.

ORDERING INFORMATION

MODEL	TEMP RANGE	CASE
AM-435-1C	0 to + 70°C	Ceramic
AM-435-1M	− 55°C to + 125°C	Ceramic

Trimming Potentiometer: TP50K, TP10K

THE AM-435 is COVERED BY GSA CONTRACT.

TECHNICAL NOTES

1. Maximum differential input voltage is independent of the supply voltage, but neither input should exceed the negative supply. (+ 36 to − Vs). Slew rate of the input should be limited to 5V/μsec to insure low input bias currents.
2. The gain of the AM-435 is set by the ratio of R_S and R_G. For optimum gain stability, a low tempco gain setting resistor is recommended. A 5 or 10 ppm/°C metal film resistor is recommended. For more critical applications, we recommend a Vishay type S102 (± 1 ppm/°C). The resistors should be located as close to the terminals as possible. R_G should be used to select gain range keeping R_S constant.

GAIN	R_S (OHMS)	R_G (OHMS)
1	1M	1M
10	1M	100K
100	1M	10K
1000	1M	1K

3. The gain equation is as follows:

$$V_{OUT} = \triangle V_{IN} \frac{R_S}{R_G} + V_{REF}$$

4. For nulling out small gain errors, a 50K trimming potentiometer in series with a 953K resistor should be used to replace R_S.
5. The maximum linear output swing is determined by the magnitude of resistor R_S:

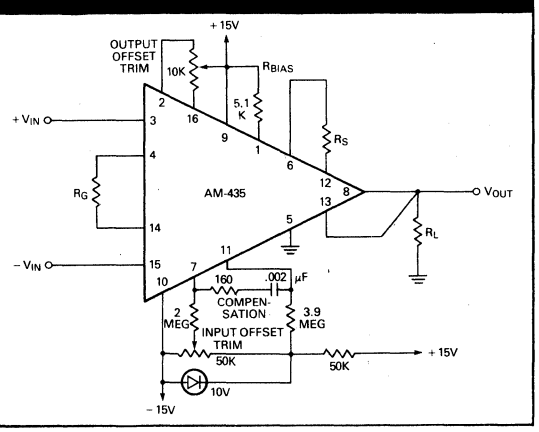
$$(V_{OUT})_{MAX} = 10\mu A \times R_S$$

6. The sense input is, in effect, the feedback "summing point" of the output section. This terminal is usually connected to the output. For remote loads or for load current sensing, the sense terminal is run separately to the load or to the current sensing resistors. The reference terminal is normally connected to ground but may be connected to a voltage source in a range of ± 10V in order to directly offset the amplifier output. The Reference Input is useful for zeroing offsets whether they occur in the source, the amplifiers, or the system that follows. To minimize errors due to input current (typically 20μA), the effective resistances in series with the Sense and Reference terminals should be equal.
7. The AM-435 is a two stage instrumentation amplifier and each stage contributes independently to the offset referred to the output (R.T.O.)

   Total Offset (R.T.O.) = (Input Offset × G) + Output Offset

   For gains under 10, the output trim should be sufficient to zero out errors. If the output trim is not used, pins 2 and 16 must be connected together to the positive supply. If the input trim is not used, pin 1 must be connected to the positive supply. For gains greater than 10, the input offset zeroing circuit should be used to optimize accuracy.
8. A 160 ohm resistor in series with a 0.0022μF capacitor between the COMP pins will compensate the unit for all gain ranges. External components should be located as close to the package as possible for maximum accuracy.

CONNECTIONS



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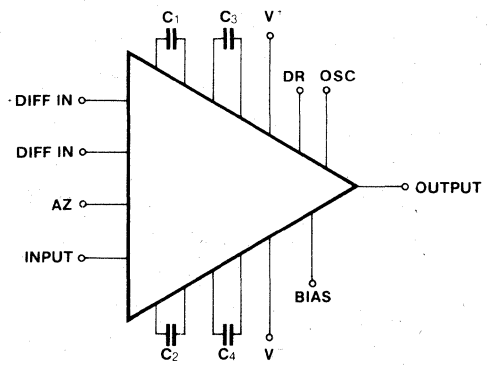
PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

AM-7605/AM-7606

Commutating Auto-Zero (CAZ) Instrumentation Amplifier

FEATURES

- **Exceptionally low input offset voltage — 2μV**
- **Low long term input offset voltage drift — 0.2μV/year**
- **Low input offset voltage temperature drift — 0.05μV/°C**
- **Wide common mode input voltage range — 0.3V above supply rail**
- **High common mode rejection ratio — 100 dB**
- **Excellent low supply voltage — Down to ±2V**
- **Short circuit protection on outputs for ±5V operation**
- **Static-protected inputs — no special handling required**



GENERAL DESCRIPTION

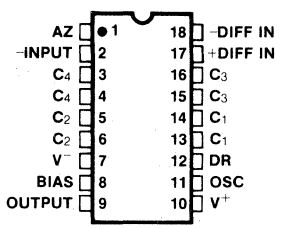
The AM-7605/AM-7606 commutating auto-zero (CAZ) instrumentation amplifiers are designed to replace almost any of today's expensive hybrid or monolithic instrumentation amplifiers for low frequency applications from DC to 10 Hz. This is made possible by the unique construction of this new device, which takes an entirely new design approach to low frequency amplifiers.

Unlike conventional amplifier designs which employ three op amps and require ultra-high accuracy in resistor tracking and matching, the CAZ instrumentation amplifier requires no trimming except for gain. The key feature of the CAZ principle involves automatic compensation for long term drift phenomena and temperature effects.

The AM-7605/AM-7606 is a monolithic CMOS chip which consists of two analog sections — a unity gain differential to single-ended voltage converter and a CAZ op amp. The first section serves to insure that at all times the differential input source is being sensed and applied to the CAZ amp section. The CAZ instrumentation amp section consists of an operational amplifier circuit which continuously corrects itself for input voltage errors, such as input offset voltage, temperature effects, and long term drift.

The AM-7605/AM-7606 is intended for low-frequency operation in applications such as strain gauges, which require voltage gains from 1 to 1000 and bandwidths from DC to 10 Hz. Since the CAZ amp automatically corrects itself for internal errors, the only periodic adjustment required is that of gain, which is established by two external resistors. The no-adjustment feature, combined with extremely low offset and temperature coefficient figures, makes the CAZ instrumentation amplifier very desirable for operation in severe environments (temperature, humidity, toxicity, radiation, etc.) where equipment service is difficult.

PIN CONFIGURATION



ORDERING INFORMATION

COMPENSATION	MODEL	OPER. TEMP. RANGE	PACKAGE
COMP.	AM-7605C	0 to + 70°C	18 pin Cerdip
	AM-7605R	−25 to + 85°C	
	AM-7605M	−55 to + 125°C	
UNCOMP.	AM-7606C	0 to + 70°C	18 pin Cerdip
	AM-7606R	−25 to + 85°C	
	AM-7606M	−55 to + 125°C	

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (sum of both positive and negative supply voltages V^+ to V^-) ..... 18 Volts
Positive Supply Voltage (GND to V^+) ..... 18 Volts
Negative Supply Voltage (GND to V^-) ..... 18 Volts
DR Input Voltage ..... (V^+ +0.3) to (V^+ −8) Volts
Input Voltage (C_1, C_2, C_3, C_4, +DIFF IN, −DIFF IN, −INPUT, BIAS, OSC) (Note 2) ..... (V^++0.3) to (V^-−0.3) Volts
Differential Input Voltage (+DIFF IN to −DIFF IN) (Note 3) ..... +(V^++0.3) to (V^-−0.3) Volts
Duration of Output Short Circuit (Note 4) ..... Unlimited
Continuous Total Power Dissipation (at or below 25°C free-air temperature) (Note 5) ..... 500 mW
Operating Temperature Range:
C ..... 0 to +70°C
R ..... −25°C to +85°C
M .....−55°C to +125°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering 60 seconds) ..... 300°C

Note 1 — Stresses above those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent device failure. These are stress ratings only, and functional operation of devices under conditions other than those indicated in the Table of Electrical Characteristics is not recommended. Exposure to absolute maximum rating conditions for extended periods of time can cause device failures.

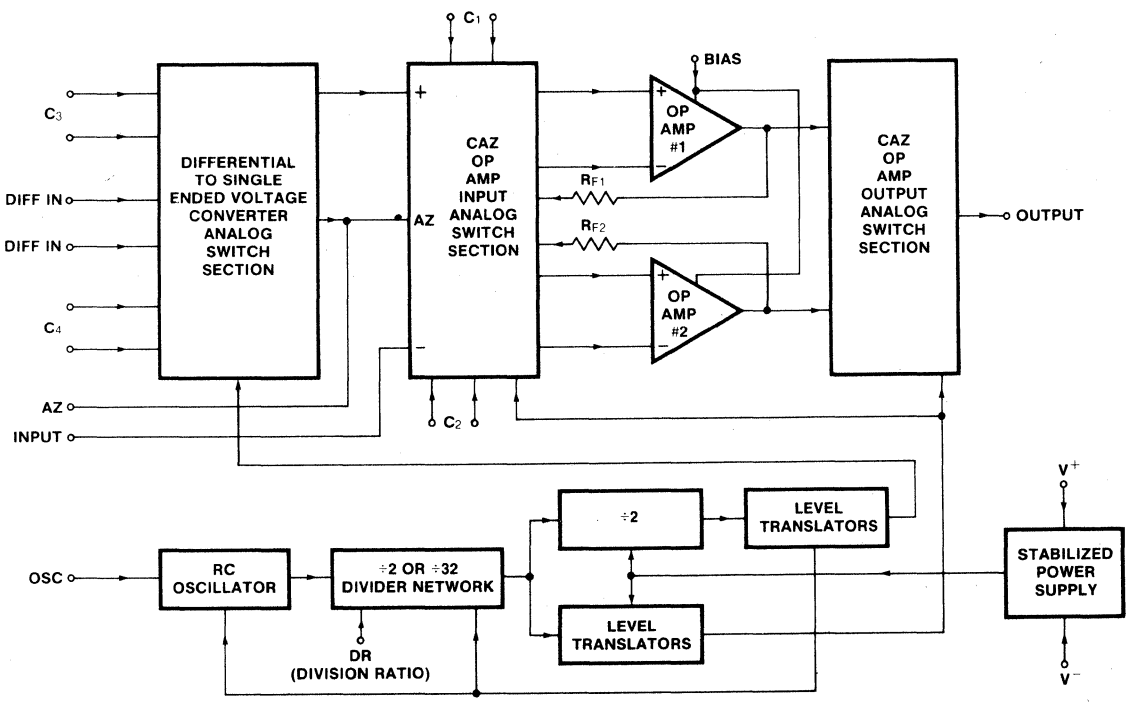
Note 2 — An SCR structure is inherent in the CMOS process used in the fabrication of these devices. If voltages in excess of V^++0.3 volts to V^- −0.3 volts are connected to either inputs or outputs, destructive latchup can occur. For this reason it is recommended that no inputs from sources not on the same power supply or supplies be applied before the AM-7605/AM-7606 supplies are established, and that if multiple supplies are used the AM-7605/AM-7606 supplies be activated first.

Note 3 — No restrictions are placed on the differential input voltages on either the +DIFF IN or −DIFF IN inputs so long as these voltages do not exceed the power supply voltages by more than 0.3V.

Note 4 — The outputs may be shorted to ground (GND) or to either supply (V^+ or V^-). Temperatures and/or supply voltages must be limited to insure that the dissipation ratings are not exceeded.

Note 5 — For operation above 25°C free-air temperature, derate 4mW/°C from 500 mW above 25°C.

BLOCK DIAGRAM



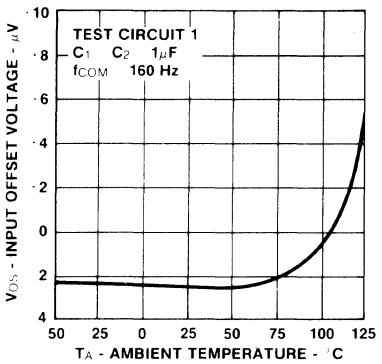
AM-7605/AM-7606

OPERATING CHARACTERISTICS

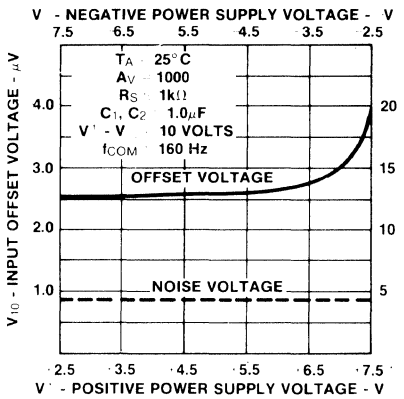
Test Conditions: $V^+ = +5$ volts, $V^- = -5$ volts, $T_A = +25°C$, DR pin connected to V^+ ($f_{COM} \cong 160Hz$, $f_{COM1} \cong 80Hz$), $C_1 = C_2 = C_3 = C_4 = 1\mu F$, Test Circuit 1 unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS		VALUE MIN	VALUE TYP	VALUE MAX	UNIT
Input Offset Voltage	V_{OS}	$R_S \leq 1k\Omega$	Low Bias Setting		±2		μV
			Med Bias Setting		±2	±5	μV
			High Bias Setting		±7		μV
		MIL version over temp.	Med Bias Setting			±20	μV
Average Input Offset Voltage Temperature Coefficient	TCV_{OS}	Low or Med Bias Settings	$-55°C > T_A > +25°C$		0.01	0.1	μV/°C
			$+25°C > T_A > +85°C$		0.01	0.1	μV/°C
			$+25°C > T_A > +125°C$		0.05	0.15	μV/°C
Long Term Input Offset Voltage Stability	$V_{OS/Time}$	Low or Med Bias Settings			0.5		μV/Year
Common Mode Input Range	CMVR			-5.3		+5.3	V
Common Mode Rejection Ratio	CMRR	C_{OSC} = 0, DR connected to V^+, $C_3 = C_4 = 1\mu F$			94		dB
		$C_{OSC} = 1\mu F$, DR connected to GND, $C_3 = C_4 = 1\mu F$			100		dB
		$C_{OSC} = 1\mu F$, DR connected to GND, $C_3 = C_4 = 10\mu F$			104		dB
Power Supply Rejection Ratio	PSRR				110		dB
-INPUT Bias Current	I_{NTB}	Any bias setting, f_C = 160Hz (Includes charge injection currents)			0.15	1.5	nA
Equivalent Input Noise Voltage peak-to-peak	e_{np-p}		Low Bias Mode		4.0		μV
		Band Width	Med Bias Mode		4.0		μV
		0.1 to 10Hz	High Bias Mode		5.0		μV
Equivalent Input Noise Voltage	e_{np-p}	Band Width 0.1 to 1.0Hz	All Bias Modes		1.7		μV
Voltage Gain	A_V	R_L = 100kΩ	Low Bias Setting	90	105		dB
			Med Bias Setting	90	105		dB
			High Bias Setting	80	100		dB
Maximum Output Voltage Swing	V_{OUT}	R_L 1MΩ			±4.9		V
		R_L 100kΩ			±4.8		V
		R_L 10kΩ	Positive Swing	+4.4			V
			Negative Swing			-4.5	V
Band Width of Input Voltage Translator	GBW	$C_3 = C_4 = 1\mu F$	All Bias Modes		10		Hz
Nominal Commutation Frequency	f_{COM}	C_{OSC} = 0pF	DR Connected to V^+		160		Hz
			DR Connected to GND		2560		Hz
Nominal Input Converter Commutation Frequency	f_{COM1}	C_{OSC} = 0pF	DR Connected to V^+		80		Hz
			DR Connected to GND		1280		Hz
Bias Voltage to define Current Modes	V_{BA}	Low Bias Setting		V^+ -0.3		V^+ +0.3	V
	V_{BM}	Med Bias Setting		V^+ +1.4		V^+ 1.4	V
	V_{BL}	High Bias Setting		V^+ -0.3		V^+ +0.3	V
Bias (Pin 8) Input Current	I_{BIAS}				±30		pA
Division Ratio Input Current	I_{DR}	$V^+ - 8.0 \leq V_{DR} \leq V^+ + 0.3$ volt			±30		pA
DR Voltage to define Oscillator division ratio	V_{DRH}	Internal oscillator division ratio 32		V^+ 0.3		V^+ +0.3	V
	V_{DRL}	Internal oscillator division ratio 2		V^+ 8		V^+ 1.4	V
Effective Impedance of Voltage Translator Analog Switches	R_{AS}				30		kΩ
Supply Current	I_S	High Bias Setting		4	7	15	mA
		Med Bias Setting		0.6	1.7	5	mA
		Low Bias Setting		0.25	0.6	1.5	mA
Operating Supply Voltage Range	V^+-V^-	High Bias Setting		5		10	V
		Med or Low Bias Setting		4		10	V

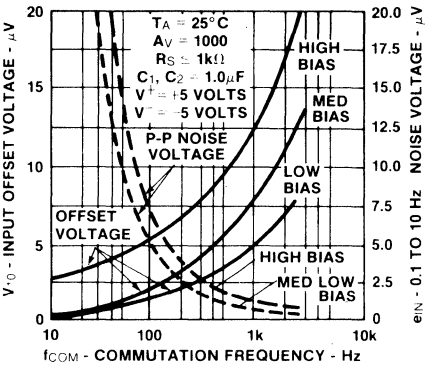
INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



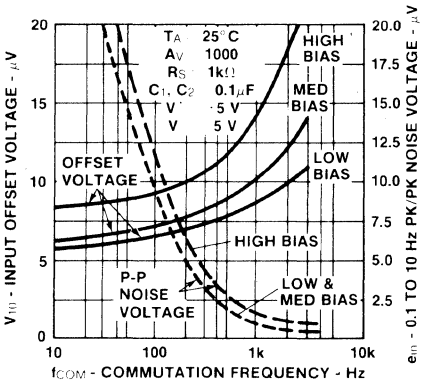
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGES



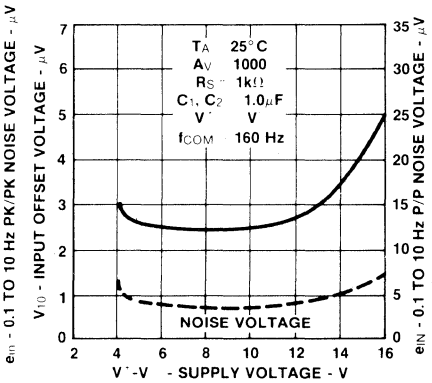
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C_1, C_2 = 1μF)



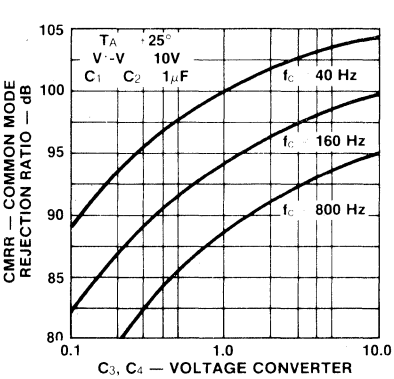
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C_1, C_2 = 0.1 μF)



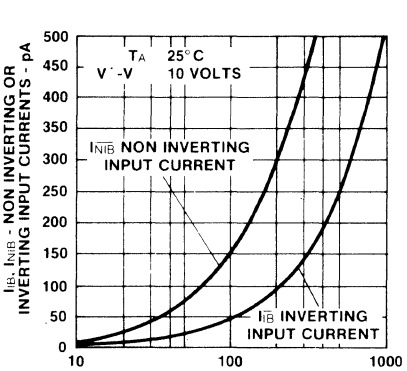
INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE AS A FUNCTION OF SUPPLY VOLTAGE (V+-V-)



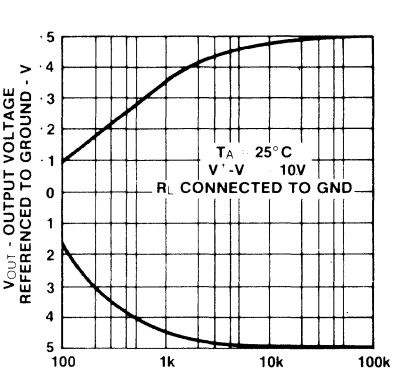
COMMON MODE REJECTION RATIO AS A FUNCTION OF THE INPUT DIFFERENTIAL TO SINGLE ENDED VOLTAGE CONVERTER CAPACITORS



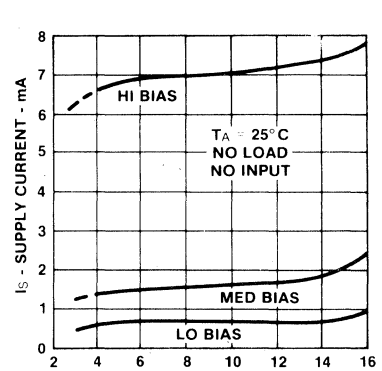
INPUT CURRENT AS A FUNCTION OF COMMUTATION FREQUENCY



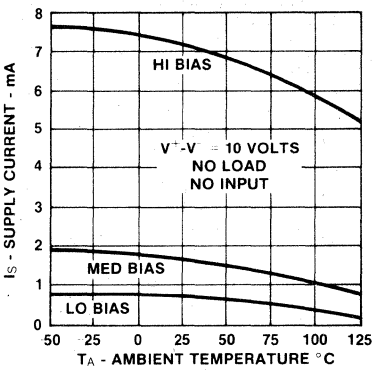
MAXIMUM OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT LOAD RESISTANCE



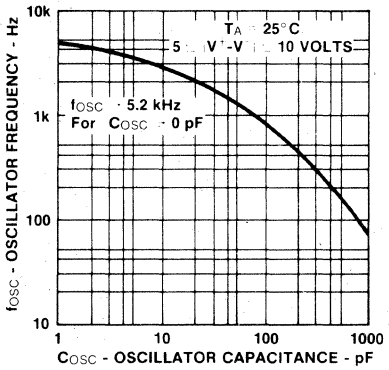
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



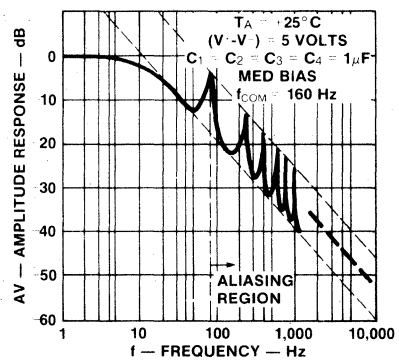
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



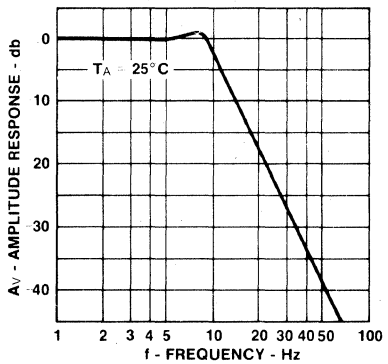
OSCILLATOR FREQUENCY AS A FUNCTION OF EXTERNAL CAPACITIVE LOADING

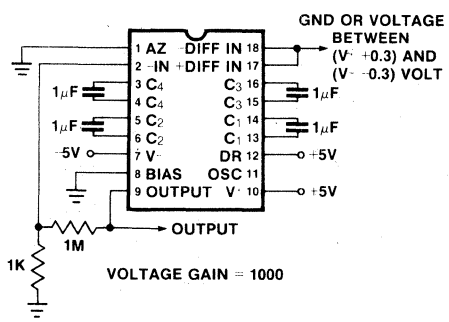


AMPLITUDE RESPONSE OF THE INPUT DIFFERENTIAL TO SINGLE ENDED VOLTAGE CONVERTER



FREQUENCY RESPONSE OF THE 10 Hz LOW PASS FILTER USED TO MEASURE NOISE (TEST CIRCUIT 2).





TEST CIRCUIT 1: USE TO MEASURE:

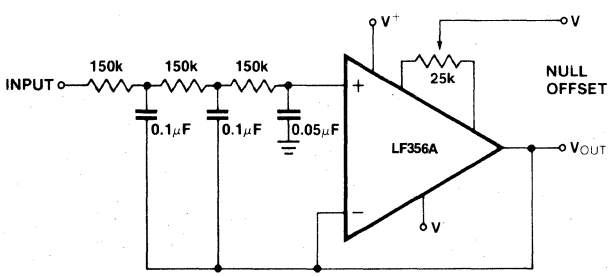
a) INPUT OFFSET VOLTAGE $\left(\frac{V_{OUT}}{1000}\right)$

b) INPUT EQUIV NOISE VOLTAGE

c) SUPPLY CURRENT

d) CMRR

e) PSRR



TEST CIRCUIT 2: DC to 10Hz (1Hz) Unity Gain Low Pass Filter

DETAILED DESCRIPTION

CAZ Instrumentation Amp Overview

The CAZ instrumentation amplifier operates on principles which are very different from those of the conventional three op amp designs, which must use ultra-precise trimmed resistor networks in order to achieve acceptable accuracy. An important advantage of the AM-7605/AM-7606 CAZ instrumentation amp is the provision for self-compensation for internal error voltages, whether they are derived from steady-state conditions, temperature, supply voltage fluctuations, or are variable over a long term.

The CAZ instrumentation amplifier is constructed with monolithic CMOS technology, and consists of three distinct sections, two analog and one digital. The two analog sections — a differential to single-ended voltage converter, and a CAZ op amp — have on-chip analog switches to steer the input signal. The analog switches are driven from a self-contained digital section which consists of an RC oscillator, a programmable divider, and associated voltage translators. A functional layout of the AM-7605/AM-7606 is shown in Figure 1.

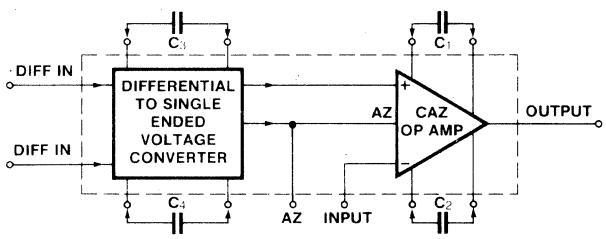


Figure 1: Simplified Block Diagram

The AM-7605/AM-7606 have approximately constant input equivalent noise voltage, CMRR, PSRR, input offset voltage and drift values independent of the gain configuration. By comparison, hybrid-type modules which use the traditional three op amp configuration have relatively poor performance at low gain (1 to 100) with improved performance above a gain of 100.

The only major limitation of the AM-7605/AM-7606 is its low-frequency operation (10 to 20 Hz maximum). However in many applications speed is not the most important parameter.

CAZ Op Amp Section

Operation of the CAZ amp section of the AM-7605/AM-7606 instrumentation amplifier is best illustrated by referring to Figure 2. The basic amplifier configuration, represented by the large triangles, has one more input than does a regular op amp — the AZ, or auto-zero terminal. The voltage on the AZ input is that level to which each of the internal op amps are to be auto-zeroed. In Mode A, op amp #2 is connected into a unity gain mode through on-chip analog switches, and charges external capacitor C_2 to a voltage equal to the DC input offset voltage of the amplifier, in addition to the instantaneous low-frequency noise voltage. A short time later, the analog switches reconnect the on-chip op amps to the configuration shown in Mode B. In this mode, op amp #2 has capacitor C_2 (which is charged to a voltage equal to the offset and noise voltage of op amp #2) connected in series to its non-inverting (+) input in such a manner as to null out the input offset and noise voltages of the amplifier. While one of the on-chip op amps is processing the input signal, the second op amp is in an auto-zero mode, and charges a capacitor to a voltage equal to its equivalent DC and low frequency error voltage. The on-chip amplifiers are connected and reconnected at a rate designated as the commutation frequency (f_{COM}) so that at all times one or the other of the on-chip op amps is processing the input signal while the voltages on capacitors C_1 and C_2 are being updated regularly to compensate for variables such as low frequency noise voltage and input offset voltage changes due to temperature, drift or supply voltages effects.

Compared to the standard bipolar or FET input op amps, the CAZ amp scheme demonstrates a number of important advantages:

* Effective input offset voltages can be reduced from 1000 to 10,000 times without trimming.
* Long-term offset voltage drift phenomena can be compensated and dramatically reduced.
* Thermal effects can be compensated for over a wide operating temperature range. Reductions can be as much as 100 times or better.
* Supply voltage sensitivity is reduced.

CMOS processing is ideally suited to implement the CAZ amp structure. The digital section is easily fabricated, and

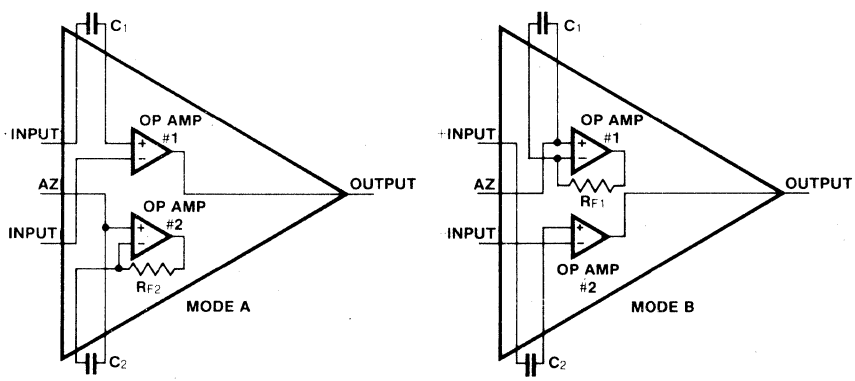


Figure 2: Diagrammatic representation of the 2 half cycles of operation of the CAZ OP AMP.

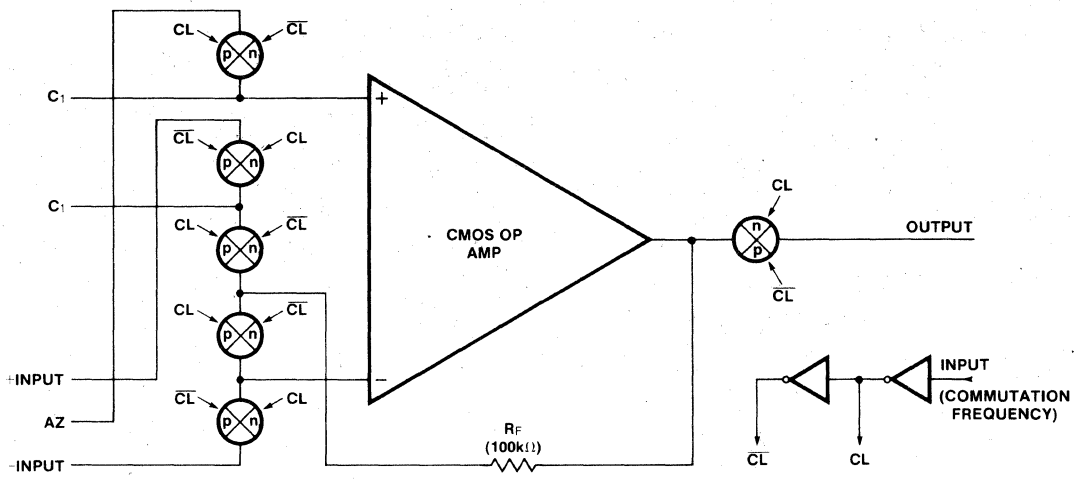


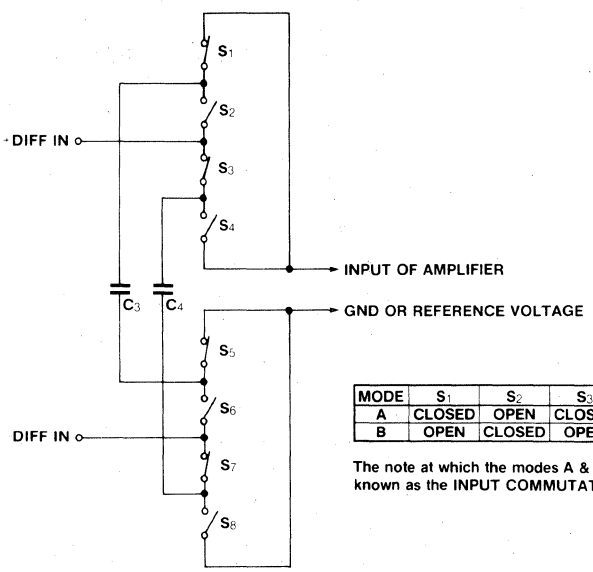
Figure 3: Schematic of analog switches connecting each internal OP AMP to the external inputs at the output.

the transmission gates (analog switches) which connect the on-chip op amps can be constructed for minimum charge injection and the widest operating voltage range. The analog section, which includes the on-chip op amps, contributes performance figures which are similar to bipolar or FET input designs. CMOS structure provides the CAZ amp concept with open-loop gains of greater than 100 dB, typical input offset voltages of ±5 mV, and ultra-low output leakage currents, typically 1 pA.

The CMOS transmission gates connect the on-chip op amps to external input and output terminals, as shown in Figure 3. Here, one op amp and its associated analog switches are required to connect each on-chip op amp so that at any time three switches are open and three switches are closed. Each analog switch consists of a P-channel transistor in parallel with an N-channel transistor.

DIFFERENTIAL-TO-SINGLE-ENDED UNITY GAIN VOLTAGE CONVERTER

An idealized schematic of a voltage converter block is shown in Figure 4. The mode of operation is quite simple, involving two capacitors and eight switches. The switches are arranged so that four are open and four are closed. The four conducting switches connect one of the capacitors across the differential input and the other from a ground or reference voltage to the input of the CAZ instrumentation amp. The output signal of this configuration is shown in Figure 5, where the voltage steps equal the differential voltage (V_A-V_B) at commutation times a, b, c, etc. The output waveform thus represents all information contained in the input signal from DC up to the commutation frequency, commutation and noise voltages are added. Sampling theory states that to preserve the integrity of the information to be processed, at least two samples must be taken within a period (1/f) of the highest frequency of the signal being



MODE	S1	S2	S3	S4	S5	S6	S7	S8
A	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN
B	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED

The note at which the modes A & B are cycled through is known as the INPUT COMMUTATION FREQUENCY

Figure 4: Schematic of the differential to single ended voltage converter

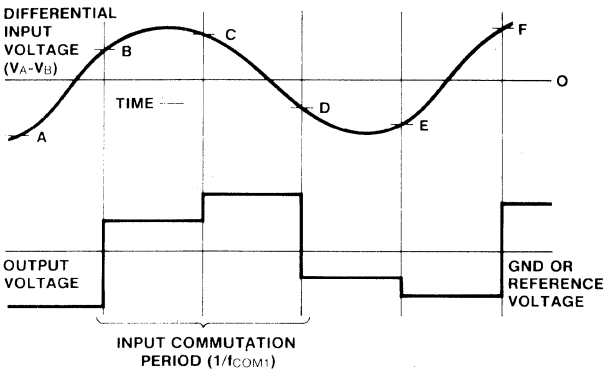


Figure 5: Input to Output Voltage waveforms from the differential to single ended voltage converter. For additional information, see frequency characteristics in Amplitude Response of the Input Differential to single ended voltage converter graph on page 5.

sampled. Consequently this scheme preserves information up to the commutation frequency. Above the commutation frequency, the input signal is transferred to a lower frequency. This phenomenon is known as aliasing. Although the output responds above the commutation frequency, the frequencies of the output responses have been aliased down to frequencies below the commutation frequency.

The example shown in Figure 4 for the voltage converter is fabricated with CMOS analog switches, which contain a parallel combination of P-channel and N-channel transistors. The switches have finite ON impedances of 30kΩ, plus parasitic capacitances to the substrate. Because of the charge injection effects which appear at both the switches and the output of the voltage converter, the values of capacitors C_0 and C_O must be about 1μF to preserve signal translation accuracies to 0.01%. The 1μF capacitors, coupled with the 30kΩ equivalent impedance of the switches, produce a low-pass filter response from the voltage converter which is approximately 3 dB at 10 Hz.

APPLICATIONS

USING THE AM-7605/AM-7606 TO BUILD A DIGITAL READOUT TORQUE WRENCH

A typical application for the AM-7605/AM-7606 is in a strain gauge system, such as the digital readout torque wrench circuit shown in Figure 6. In this application, the CAZ intrumentation amplifier is used as a preamplifier, taking the differential voltage of the bridge and converting this voltage to a single-ended voltage reference to ground. The signal is then amplifier by the CAZ instrumentation amplifier and applied to the input of a 3-1/2 digit dual-slope A/D converter chip for LCD panel meter display. The A/D converter device used in this instance is the Intersil ICL7106.

In the digital readout torque wrench circuit, the internal reference voltage of the ICL7106 is used instead of the conventional external reference source. In order to set the full-scale reading, it is required that, given a certain strain gauge bridge with a defined pressure voltage sensitivity, a value of gain for the AM-7605/AM-7606 instrumentation CAZ amp be selected along with an appropriate value for the reference voltage. The gain should be set so that at full scale the output will swing about 0.5V. The reference voltage required is about one-half the maximum output swing, or approximately 0.25V.

In this type of system, only one adjustment is required. Either the amplifier gain or the reference voltage must be varied for full-scale adjustment. Note that the common to V^+ voltage of the CAZ amp is about 2.8V. This voltage must therefore be divided by about 10 to provide the 0.25V reference voltage. Total current consumption of all circuitry, less the current through the strain gauge bridge, is typically 2 mA.

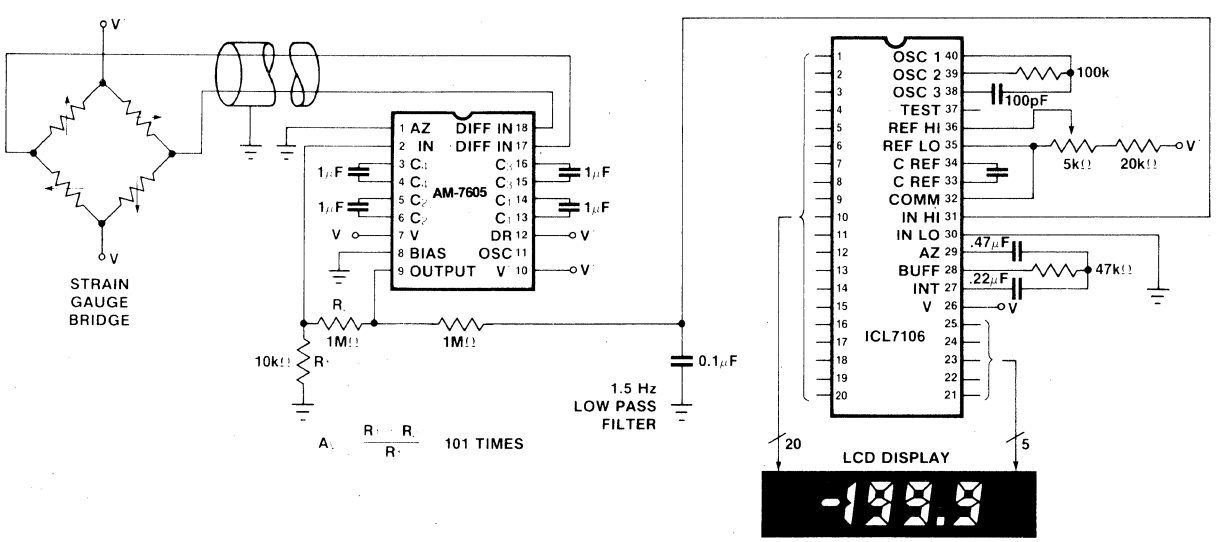


Figure 6: 3-1/2 Digit Digital Readout Torque Wrench

SOME HELPFUL HINTS

Testing the AM-7605/AM-7606 CAZ Instrumentation Amplifier

Test Circuits #1 and #2 provide convenient means of measuring most of the important electrical parameters of the CAZ instrumentation amp. The output signal can be viewed on an oscilloscope after being fed through a low-pass filter. It is recommended that for most applications, a low-pass filter of about 1.0 to 1.5 Hz be used to reduce the peak-to-peak noise to about the same level as the input offset voltage.

The output low-pass filter must be of a high-input impedance type — not a capacitor across the feedback resistor R_2 nor a low-impedance type of around 1kΩ — but rather must be rated at about 100kΩ and 1.0μF so that the output dynamic loading on the CAZ instrumentation amp is about 100kΩ.

Bias Control

The on-chip op amps consume over 90% of the power required by the AM-7605/AM-7606 instrumentation op amp. For this reason, the internal op amps have externally-programmable bias levels. These levels are set by connecting the BIAS terminal to either V^+, GND, or V^-. The difference between each bias setting is about a factor of 3, allowing a 9:1 ratio of power supply versus bias setting. This current programmability provides the user with a choice of device power dissipation levels, slew rates (the higher the slew rate, the lower the amplitude of commutation spikes) and offset errors due to "IR" voltage drops and thermoelectric temperature gradients across the chip and the higher the temperature gradients across the chip and the highe the input offset error). In most cases, the medium bias (MED BIAS) setting will be found to be the best choice.

Output Loading (Resistive)

With a 10kΩ load, the output voltage swing can vary across nearly the entire supply voltage range, and the device can be used with loads as low as 2kΩ.

However, with loads of less than 50kΩ, the on-chip op amps will begin to exhibit the characteristics of transconductance amplifiers, since their respective output impedances are nearly 50kΩ each. Thus the open-loop gain is 20 dB less with a 2kΩ load than it would be with a 20kΩ load. Therefore, for high gain configurations requiring high accuracy, an output loading of 100kΩ or less is suggested.

There is another consideration in applying the CAZ instrumentation op amps which must not be overlooked, and that is the additional power dissipation of the chip which will result from a large output voltage swing into a low resistance load. This added power dissipation can affect the initial input offset voltages under certain conditions.

Output Loading (Capacitive)

In many applications, it is desirable to include a low-pass filter at the output of the CAZ instrumentation op amp to reduce high-frequency noise outside the desired signal passband. An obvious solution when using a conventional op amp would be to place a capacitor across the external feedback resistor and thus produce a low-pass filter.

However, with the CAZ op amp concept this is not possible because of the nature of the commutation spikes. These voltage spikes exhibit a low-impedance characteristic in the direction of the auto-zero voltage and a high-impedance characteristic on the recovery edge, as shown in Figure 7. It can be seen that the effect of a large load capacitor produces an area error in the output waveform, and hence an effective gain error. The output low-pass filter must be of a high-impedance type to avoid these area errors. For example, a 1.5 Hz filter will require a 100kΩ resistor and a 1.0μF capacitor, or a 1 MΩ resistor and an 0.1μF capacitor.

Oscillator and Digital Circuitry Considerations

The oscillator has been designed to run free at about 5.2 kHz when the OSC terminal is open circuit. If the full divider network is used, this will result in a nominal commutation frequency of approximately 160 Hz. The commutation frequency is that frequency at which the on-chip op amps are switched between the signal processing and the auto-zero modes. A 160 Hz commutation frequency represents the best compromise between input offset voltage and low frequency noise. Other commutation frequencies may provide optimization of some parameters, but always at the expense of others.

The oscillator has a very high output impedance, so that a load of only a few picofarads on the OSC terminal will cause a significant shift in frequency. It is therefore recommended that if the natural oscillator frequency is desired (5.2 kHz) the terminal remains open circuit. In other instances, it may be desirable to synchronize the oscillator with an external clock source, or to run it at another frequency. The AM-7605/AM-7606 CAZ amp provides two degrees of flexibility in this respect. First, the DR (division ratio) terminal allows a choice of either dividing the oscillator by 32 (DR terminal to V^+) or by 2 (DR terminal to GND) to obtain the commutation frequency. Second, the oscillator may have its frequency lowered by the addition of an external capacitor connected between the OSC terminal and the V^+ or system GND terminals. For situations which require that the commutation frequency be synchronized with a master clock, (Figure 8) the OSC terminal may be driven from TTL logic (with resistive pull-up) or by CMOS logic, provided that the V^+ supply (with respect to ground) is +5V (±10%) and the logic driver also operates from a similar voltage supply. The

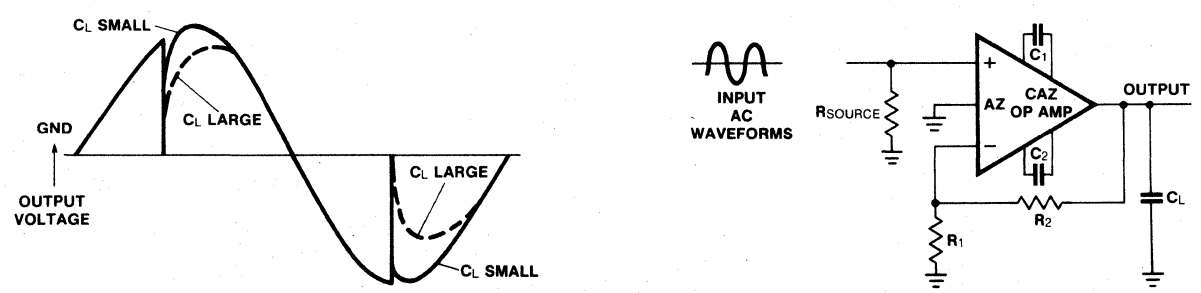


Figure 7: Effect of a load capacitor on output voltage waveforms.

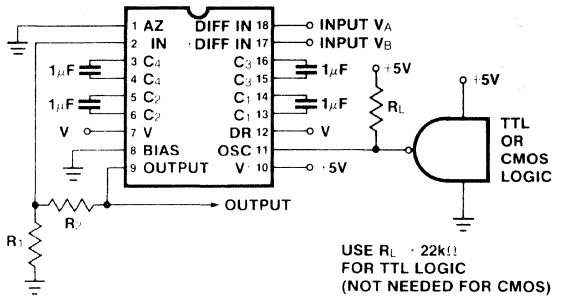


Figure 8: AM-7605 being clocked from external logic into the oscillator terminal.

reason for this requirement is that the logic section (including the oscillator) operates from an internal -5V supply, referenced to V⁻ support which is generated on-chip, and which is not accessible externally.

Thermoelectric Effects

The ultimate limitations to ultra-high-sensitivity DC amplifiers are due to thermoelectric, Peltier, or thermocouple effects whereby electrical junctions consist of various metals (alloys, silicon, etc.) Unless all junctions are at precisely the same temperature, small thermoelectric voltages will be produced, generally about 0.1μV/°C. However, these voltages can be several tens of microvolts per °C for certain thermocouple materials.

In order to realize the extremely low offset voltages which the CAZ op amp can produce, it is necessary to take precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement across device surfaces. Special thermoelectric solder (70% cadmium, 30% tin) should be used. In addition, the supply voltages and power dissipation should be kept to a minimum by use of the MED BIAS setting. Employ a high impedance load and keep well away from equipment which dissipates heat.

Component Selection

The two auto-zero capacitors (C_1 and C_2) should each be about 1.0μF value. These are relatively large values for non-electrolytic capacitors, but since the voltages stored on them do not change significantly, problems of dielectric absorption, charge bleed-off and the like are not as significant as they would be for integrating dual-slope A/D converter applications. Polypropylene and Mylar are the best.

Excellent results have been obtained for commercial temperature ranges using several of the less-expensive, smaller-size capacitors, since the absolute values of the capacitors is not critical. Even polarized electrolytic capacitors rated at 1.0μF and 50V have been used successfully at room temperature, although no recommendations are made concerning the use of such capacitors.

Commutation Voltage Transient Effects

Although in most respects the CAZ instrumentation amplifier resembles a conventional op amp, its principal applications will be in very low level, low-frequency preamplifiers limited to DC through 10 Hz. The is due to the finite switching transients which occur at both the input and output terminals because of commutation effects. These transients have a frequency spectrum beginning at the commutation frequency, and including all of the higher harmonics of the commutation frequency. Assuming that the commutation frequency is higher than the highest in-band frequency, then the commutation transients can be filtered out with a low-pass filter.

The input commutation transients arise when each of the on-chip op amps experiences a shift in voltage which is equal to the input offset voltages (about 5-10mV), usually occurring during the transition between the signal processing mode and the auto-zero mode. Since the input capacitances of the on-chip op amps are typically in the 10 pF range, and since it is desirable to reduce the effective input offset voltage about 10,000 times, the offset voltage auto-zero capacitors C_1 and C_2 must have values of at least 10,000 x 10 pF, or 0.1μF each.

The charge that is injected into the input of each op amp when being switched into the signal processing mode produces a rapidly-decaying voltage spike at the input, plus an equivalent DC input bias current averaged over a full cycle. This bias current is directly proportional to the commutation frequency, and in most instances will greatly exceed the inherent leakage currents of the input analog switches, which are typically 1.0 pA at an ambient temperature of 25°C.

The output waveform in Test Circuit #1 (with no input signal) is shown in Figure 9. Note that the equivalent noise voltage is amplified 1000 times, and that due to the slew rate of the on-chip op amps, the input transients of approximately 7 mV are not amplified by 1000.

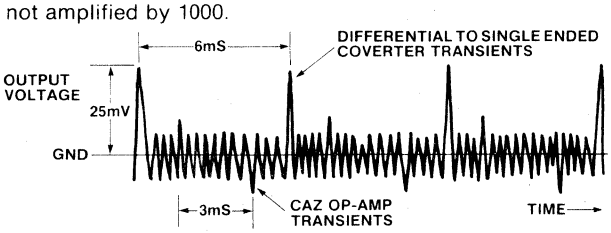
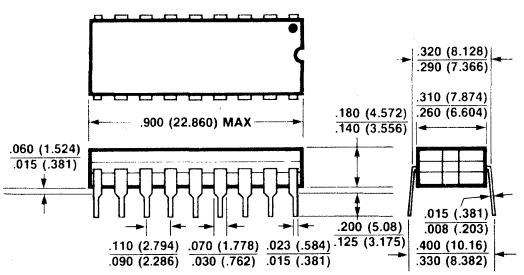


Figure 9: Output waveform from Test Circuit 1.

Layout Considerations

Care should be exercised in positioning components on the PC board, particularly the capacitors C_1, C_2, C_3 and C_4, all of which must be shielded from the OSC terminal. Also, parasitic PC board leakage capacitances associated with these four capacitors should be kept as low as possible to minimize charge injection effects.

PACKAGE DIMENSIONS



DATEL INTERSIL

PRELIMINARY DATA

Programmable Gain Instrumentation Amplifiers Models AM-542, AM-543

FEATURES

- **1 to 1024 Gains**
- **4 Bit Gain Programming**
- **$10^{12}\Omega$ Input Impedance**
- **.01% Gain Nonlinearity**
- **Gain Drift to 10ppm/°C max.**
- **Fast Settling to 10 μsec**
- **CMRR to 120 dB**

GENERAL DESCRIPTION

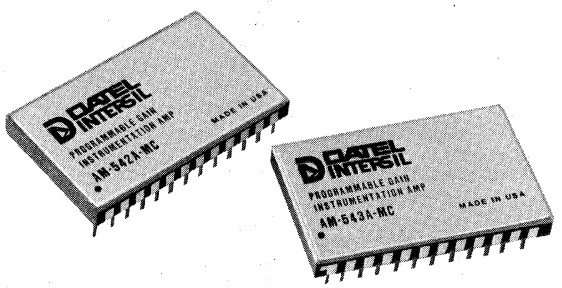
The AM-542 and AM-543 are high performance, digitally controlled Programmable Gain Instrumentation Amplifiers. These amplifiers permit selection of gains from 1 to 1024 in 11 binary weighted steps, through the input of a 4 bit TTL compatible word. One version is optimized for low drift and the other is optimized for fast settling. Use of these devices in data acquisition applications yields a system with wide dynamic range and high resolution. These amplifiers have special damping circuits which result in fast settling times with both gain range and signal amplitudes changing simultaneously. Most other PGIA's do not have this capability.

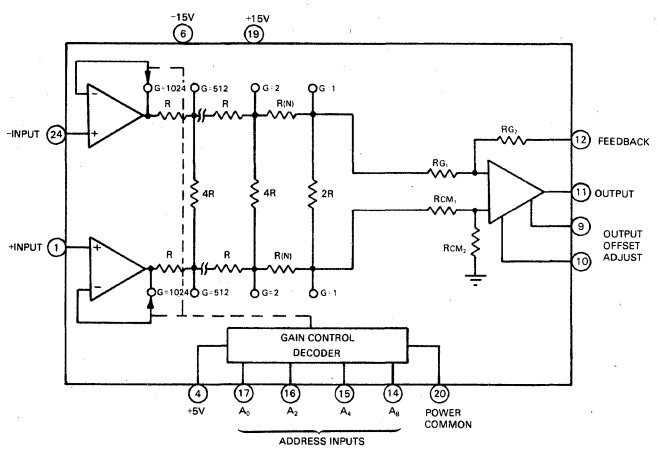
These amplifiers feature high input impedances, common mode rejection ratios to 120dB, gain nonlinearity of 0.01%, maximum output impedance of 0.1Ω at 1 KHz, input overvoltage protection, and settling times that are not degraded by gain switching.

The AM-542 is optimized for the lowest drift performance currently attainable in a Programmable Gain Instrumentation Amplifier, with models available offering input offset voltage drift of only 2 μV/°C max. All AM-542's provide an input impedance of 1.2 x $10^9\Omega$, common mode range of ±11V min., gain temperature coefficient of 10 ppm/°C max., common mode rejection up to 120 dB and a unity gain settling time to 0.01% of 160 μsec.

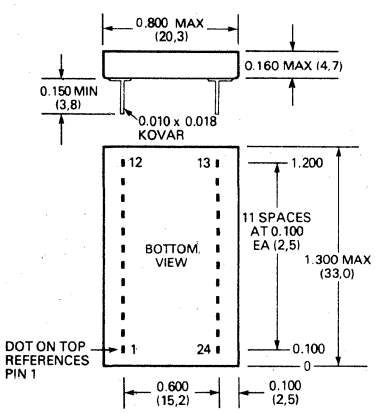
The AM-543 is tailored to provide the fastest settling time for any hybrid PGIA; a 20V output step settles to 0.01% in only 10 μsec at unity gain. These high-speed units feature a slew rate of 3.3V/μsec, an input impedance of $10^{12}\Omega$, output voltage range of ±10V min. at 5 mA, common mode rejection up to 100 dB and a gain temperature coefficient of ±15 ppm,/°C.

State-of-the-art design and thin-film hybrid technology combine to permit these amplifiers to be packaged in a compact, hermetically sealed, 24 pin ceramic DIP. The AM-542 and AM-543 are available in versions for operation over the 0 to +70°C, −25°C to +85°C or −55 to +125°C temperature ranges.





MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	+ INPUT
2	NC
3	NC
4	+5 VDC
5	NC
6	−15 VDC
7	NC
8	ANALOG COMMON
9	OUTPUT OFFSET ADJUST
10	OUTPUT OFFSET ADJUST
11	OUTPUT
12	FEEDBACK
13	NC
14	A_8
15	A_4
16	A_2
17	A_0
18	NC
19	+15 VDC
20	POWER COMMON
21	NC
22	INPUT OFFSET ADJUST
23	INPUT OFFSET ADJUST
24	− INPUT

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617)339-9341/TWX710-346-1453/TLX951340

SPECIFICATIONS, AM-542 and AM-543
(Typical at +25°C, ±15 VDC and +5 VDC supplies, unless otherwise noted).

	AM-542	AM-543
MAXIMUM RATINGS		
Positive Supply, Pin 19	+22V	+22V
Negative Supply, Pin 6	−22V	−22V
Input Voltage Range	±20V	±20V
INPUT CHARACTERISTICS		
Input Offset Voltage	±200 μV × Gain	±1 mV × Gain
Input Bias Current, max.	±14 nA	±100 pA
Input Offset Current, max.	12 nA	20 pA
Input Impedence, Diff. or Com. mode.	1.2 × 10Ω	$10^{12}\Omega$
Common Mode Voltage Range, min.	±11V	±11V
Digital Inputs, Logic "1".	Vin = ≥ +2.4V	Vin = ≥ +2.4V
Digital Inputs, Logic "0"	Vin = ≤ +0.4V	Vin = ≤ +0.4V
OUTPUT CHARACTERISTICS		
Output Voltage Range, min.	±11V	±10V
Output Current	5 mA	5 mA
Output Impedance[1]	.1Ω	.1Ω
PERFORMANCE		
Gain Range	1 to 1024	1 to 1024
Gain Accuracy, G=1 to 1024, max.	.02%	.02%
Gain NonLinearity, G=1 to 1024 max.	.01%	.01%
Gain Temperature Coefficient.	±10 ppm/°C	±15 ppm/°C
Power Supply Rejection Ratio, min.	86 dB	85 dB
Input Offset Temperature Drift,		
AM-54XA, max.	10 μV/°C	15 μV/°C
AM-54XB, max.	5 μV/°C	----
AM-54XC, max.	2 μV/°C	----
Input Voltage Noise, DC to 100Hz, G=1	100 uV p-p	1 mV p-p, max.
G=1024		
Common Mode Rejection Ratio[2],		
G=1, DC	120 dB	100 dB
G=1, 100 Hz	100 dB	98 dB
G=1, 1KHz	96 dB	96 dB
G=1024, DC	120 dB	100 dB
G=1024, 100Hz	100 dB	98 dB
G=1024, 1KHz	96 dB	96 dB
Slew Rate	0.14 V/μsec	3.3 V/μsec
Settling Time to 0.01%[3], G=1	160 μsec	10 μsec
, G=1024	3 msec	550 μsec
POWER REQUIREMENTS		
Analog Supply, Rated Value	+15V @ 50 mA	+15V @ 50 mA
	−15V @ 25 mA	−15V @ 25 mA
Analog Supply Range	±15V to ±22 VDC	±15V to ±18 VDC
Logic Supply	+5V @ 5 mA	+5V @ 5 mA
PHYSICAL ENVIRONMENTAL		
Operating Temperature Range.		
Suffix - C	0 to +70°C	
Suffix - R	−25 to +85°C	
Suffix - M	−55 to +125°C	
Storage Temperature Range.	−65 to +150°C	
Package Type.	24 Pin Ceramic DIP	
Weight	0.2 oz (6g)	

TECHNICAL NOTES

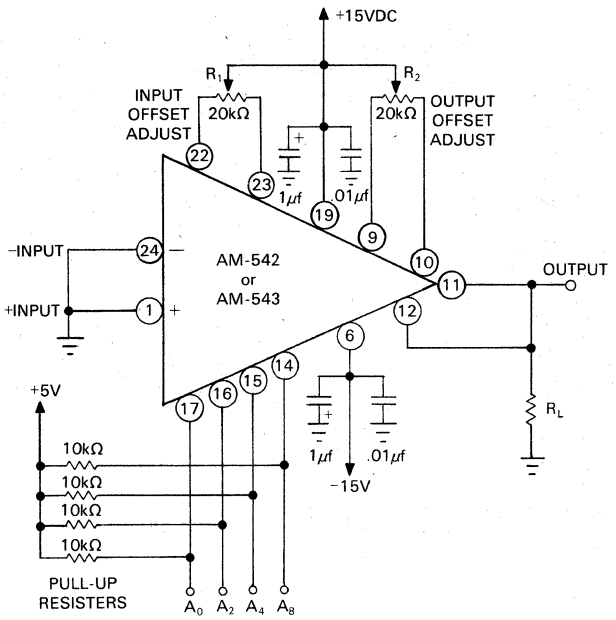
1. The AM-542 and AM-543 have an offset adjustment capability for each stage, input and output. The output trim should be sufficient to zero out offset errors on the lower gain ranges, and adjustment should be made with a gain of 1 selected. For the higher gain ranges the input offset zeroing circuit should be used to optimize accuracy. Adjustment of the input offset should be made with a gain of 1024 selected.
2. Power supply inputs to the AM-542 and AM-543 are bypassed internally. However, for best performance both power supplies should be bypassed with 1μF ceramic capacitors as close as possible to the ± supply pins.
3. Pull-up resistors are required for interfacing with the logic inputs on the AM-542/543. Recommended values are 10 KΩ.

NOTES:

1. At 1 KHz, all gain ranges.
2. 1 KΩ source imbalance.
3. For 20V output change, with or without a range change.

PERFORMANCE DATA

OFFSET ADJUSTMENT



The AM-542/543 are functionally laser trimmed to reduce initial offset voltage and offset voltage change due to gain change to a minimum level. However, for critical applications where zero offset is required, the following procedure can be followed to externally zero the offset.

1. Allow the Amplifier to reach operating temperature.
2. Set R_1 and R_2 to mid-range.
3. Set gain to 1 V/V.
4. Adjust R_2 for zero output.
5. Set gain to 1024 V/V.
6. Adjust R_1 for zero output.

This technique minimizes the offset voltage change over the maximum change in gain. Trimming may cause input offset temperature drift to increase slightly.

ORDERING INFORMATION

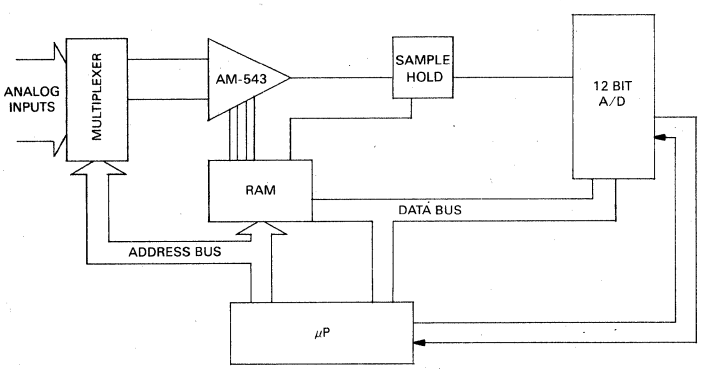
MODEL	INPUT OFFSET VOLTAGE DRIFT	SETTLING TIME TO 0.01% G-1	OPERATING TEMP. RANGE
AM-542AMC	10μV/°C	160 μsec	0°C to +70°C
AM-542AMR			-25°C to +85°C
AM-542AMM			-55°C to +125°C
AM-542BMC	5 μV/°C		0°C to +70°C
AM-542BMR			-25°C to +85°C
AM-542BMM			-55°C to +125°C
AM-542CMC	2 μV/°C		0°C to +70°C
AM-542CMR			-25°C to +85°C
AM-542CMM			-55°C to +125°C
AM-543AMC	15 μV/°C	10 μsec	0°C to +70°C
AM-542AMR			-25°C to +85°C
AM-543AMM			-55°C to +125°C

TRIMMING POTENTIOMETERS TP20K

GAIN STATE TRUTH TABLE

DIGITAL INPUTS				
A_8(PIN 14)	**A_4(PIN 15)**	**A_2(PIN 16)**	**A_0(PIN 17)**	**GAIN**
0	0	0	0	1
0	0	0	1	2
0	0	1	0	4
0	0	1	1	8
0	1	0	0	16
0	1	0	1	32
0	1	1	0	64
0	1	1	1	128
1	0	0	0	256
1	0	0	1	512
1	0	1	0	1024

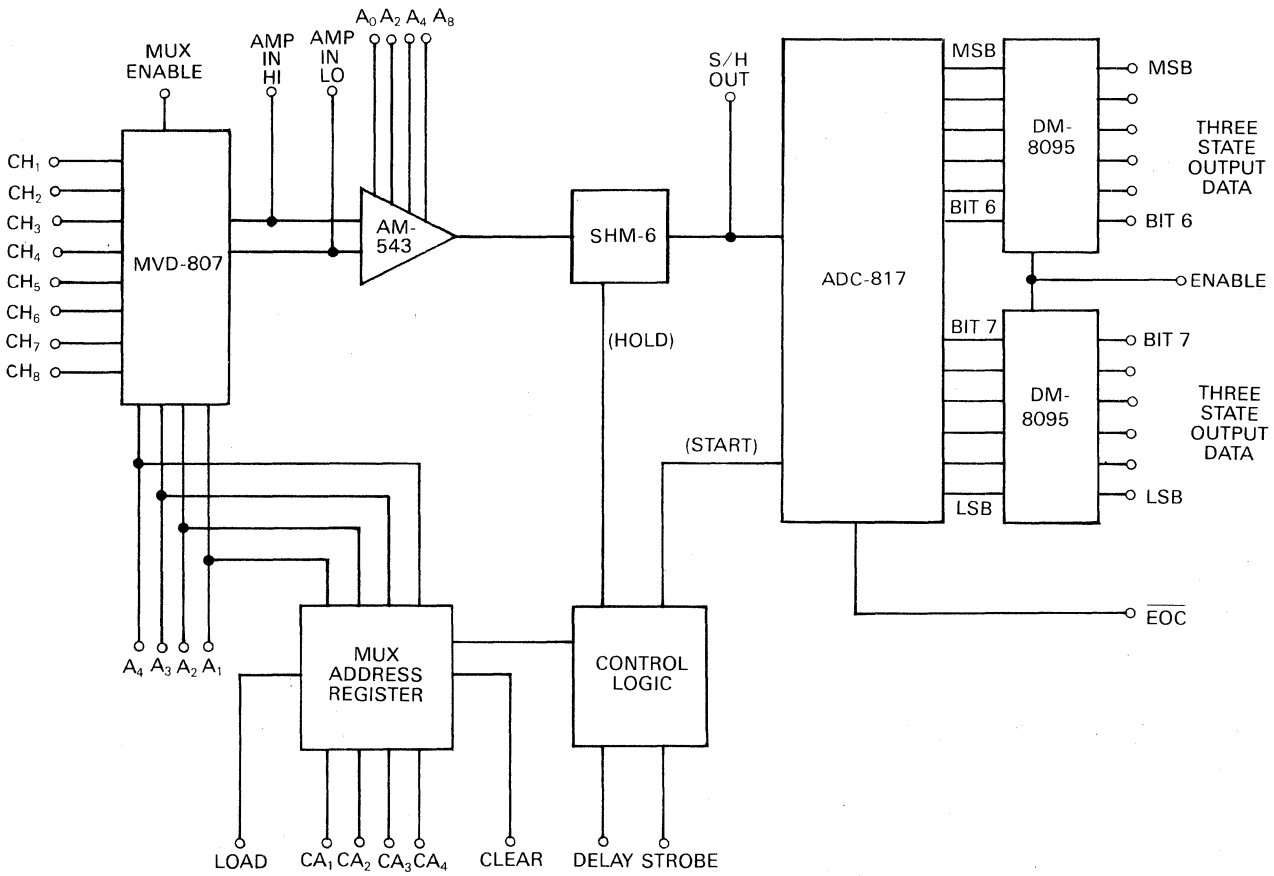
MICROPROCESSOR BASED DATA ACQUISITION SYSTEM



A typical application of the AM-542/543 is in a microprocessor controlled data acquisition system. The microprocessor loads the RAM with the desired gain coding. This coding relates the selected gain ranges to a specific address. When the processor instructs the multiplexer to multiplex a particular analog input channel, this instruction is also received by the RAM, which puts out the appropriate gain code to the AM-542/543. This system allows acquisition of signals over a wide dynamic range at high resolution.

TYPICAL APPLICATION

HIGH SPEED 12 BIT DATA ACQUISITION SYSTEM



APPLICATION NOTE

A high speed data acquisition system with 8 differential inputs and 12 bit resolution that utilizes the AM-543. If the control logic is timed so that the Sample-Hold-ADC section is converting one analog value while the mux-amplifier section is allowed to settle to the next input value, throughput rates greater than 90 KH_z can be achieved. The AM-543 is used with Datel-Intersil's ADC-817, a 12 bit hybrid A/D with a 2 μsec conversion rate, the SMH-6, a .01%, 1μsec hybrid Sample-Hold, and the MVD-807, a low cost monolithic analog multiplexer.

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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
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High Performance Instrumentation Amplifiers AM-201 Series

FEATURES

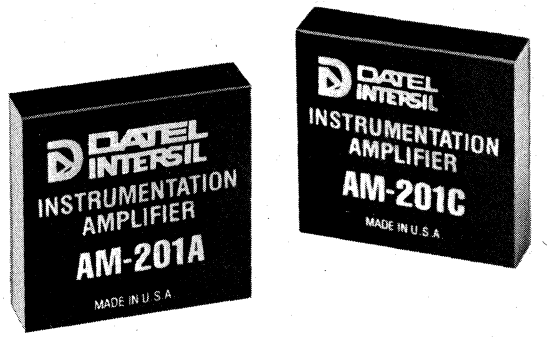
- Gain Range 1 to 1000
- Input Drift to .25 $\mu V/^{\circ}C$
- CMRR to 114 dB
- Gain Nonlinearity .01% Max.
- 180kHz Bandwidth at G=100

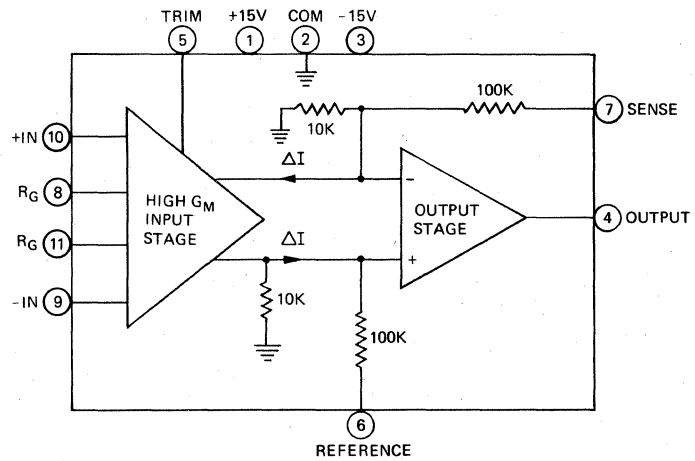
GENERAL DESCRIPTION

The AM-201 series instrumentation amplifiers offer the highest available performance in a compact, low cost module. These amplifiers are specifically designed for critical applications where the lowest input drifts and noise are required together with the highest possible common mode rejection; at the same time wide bandwidth and excellent settling time are achieved. This series rivals the performance of expensive rack-mounted instrumentation amplifiers and yet is packaged in a small 1.5 x 1.5 x .375 inch module.

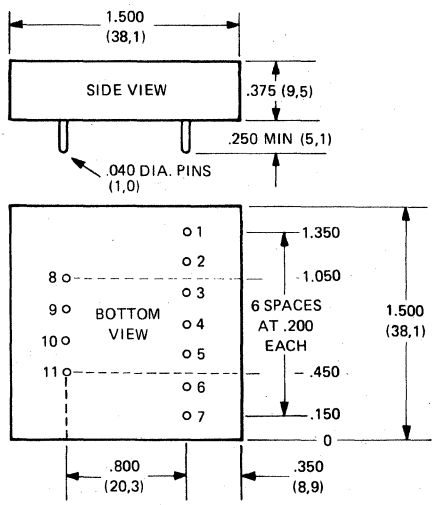
The key to the performance of the AM-201 series is a unique very high transconductance (gm = 50 mhos) input stage which gives optimum results for high gains of 100 to 1000. The amplifiers are programmed by a single external resistor for gains of 1 to 1000 and give guaranteed total voltage offset drifts referred to the input of 1.0, 0.5, and $0.25\mu V/^{\circ}C$ at a gain of 1000 for the three models AM-201A, AM-201B, and AM-201C respectively. At a gain of 1000 the common mode rejection ratio is 100, 106, and 114 dB minimum for the three models, with a source unbalance of 1 kilohm. The input stage gives very low bias currents and an input offset current drift of only $20pA/^{\circ}C$, allowing use of up to 50 kilohm balanced input source impedances. These performance characteristics are achieved without sacrificing good bandwidth: 3 dB bandwidth is 45 kHz at G=1000 and 180 kHz at G=100. Output settling time is 20 μsec. for a 10V step to .01%.

The gain equation for these models is: $G=200K/R_G$. Gain equation accuracy is ±0.5% with a gain nonlinearity of .01% maximum and gain temperature coefficient of $20ppm/^{\circ}C$ maximum. Other input specifications include input voltage noise of 1μV peak to peak from 0.1 to 10 Hz and 1μV RMS from 10 Hz to 10 kHz. The input offset voltage is adjustable to zero by means of an external trimming potentiometer. These amplifiers also have sense and reference terminals for load sensing and externally offsetting the output voltage. Output capability is ±10V at 5mA, with output short circuit protection.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	+15V POWER IN
2	COMMON
3	-15V POWER IN
4	OUTPUT
5	TRIM
6	REFERENCE
7	SENSE
8	R_G
9	-INPUT
10	+INPUT
11	R_G

DATEL-INTERSIL INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617) 339-9341 / TWX 710-346-1953 / TLX 951340

SPECIFICATIONS, AM-201 SERIES

Typical at 25°C and ±15V supplies unless otherwise noted.

	A	B	C
INPUT CHARACTERISTICS			
Differential Input Voltage Range		±10V min.	
Common Mode Input Voltage Range		±10V min.	
Input Overvoltage, no damage		±V supply	
Input Impedance, Diff. or Com. Mode		10^9 ohms	
Input Bias Current, nA max.	50	25	25
Input Offset Current, nA	2.5	1	1
Input Impedance, Ref. & Sense Inputs		110K	
Input Offset Voltage		Adj. to zero	
OUTPUT CHARACTERISTICS			
Output Voltage		±10V min.	
Output Current, S.C. protected		±5mA min.	
Output Impedance		0.1 ohm	
Capacitive Load		.01μF max.	
Output Offset Range		±10V min.	
PERFORMANCE			
Gain Range		1 to 1000	
Gain Equation		$200K/R_G$	
Gain Equation Accuracy		±0.5%	
Gain Nonlinearity		.01% max.	
Gain Temperature Coefficient		±20ppm/°C max.	
CMR, ±10V, 1K unbal., DC-120 Hz			
G=1000, dB min.	100	106	114
G=100 dB min.	80	86	94
G=10 dB min.	60	66	74
G=1 dB min.	40	46	54
DRIFT AND NOISE			
Input Offset Voltage Drift[1], μV/°C max. at G=1000	±1.0	±0.5	±0.25
Output Offset Voltage Drift, G=1		±100μV/°C	
Input Bias Current Drift		100pA/°C	
Input Offset Current Drift		20pA/°C	
Power Supply Rej., μV/V at G=1000	10	5	2
Input Voltage Noise, 0.1 to 10 Hz		1μV P-P	
Input Voltage Noise, 10 Hz to 10 kHz		1μV RMS	
Input Current Noise, 10 Hz to 10 kHz		20pA RMS	
DYNAMIC RESPONSE			
Small Sig. Bandwidth, –3 dB, G=1000		45 kHz	
G=100		180 kHz	
G=10		300 kHz	
Slew Rate		1 V/μsec.	
Full Power Response, 20V P-P		15 kHz	
Settling Time, 10V to .01% at G=1000		20 μsec.	
Overload Recovery		10 μsec.	
POWER REQUIREMENT			
Voltage, rated performance		±15VDC ±0.5V	
Voltage Range, operating[2]		±12V to ±18VDC	
Current, quiescent		5 mA	
PHYSICAL-ENVIRONMENTAL			
Operating Temperature Range		0°C to 70°C	
Storage Temperature Range		–55°C to +85°C	
Relative Humidity		Up to 100% non-condensing	
Case Size		1.5 x 1.5 x .375 inches (38,1 x 38,1 x 9,5 mm)	
Case Material		Black Diallyl Phthalate per MIL-M-14	
Pins		.040 round, gold plated, .250" long min.	
Weight		2.5 oz. max. (71 g.)	

1. With input offset voltage initially zeroed.
2. Signal input and output range is ±7V to ±13V.

TECHNICAL NOTES

1. The guaranteed input offset voltage drift specification requires that the input offset voltage be zeroed. This is done by means of an external 50K trimming potentiometer connected from the TRIM pin to +15V. For minimum effect upon input offset drift, a low tempco trimming pot is recommended such as Vishay type 1203 (20ppm/°C). If the operating temperature range is relatively constant, then a 100ppm/°C cermet type trimming pot may be used (Datel Systems TP50K at $3.00 each). A 100ppm/°C drift in the trimming pot causes a 0.3μV/°C input offset voltage drift in the amplifier.

2. For optimum gain stability a low tempco gain setting resistor is recommended. The temperature coefficient of this resistor adds directly to the 20ppm/°C maximum gain tempco of the amplifier. For negligible effect on tempco Vishay type S102 (±1ppm/°C) is recommended. For less critical applications a 5 or 10ppm/°C metal film resistor is recommended. The resistor should be located as close as possible to the R_G terminals of the amplifier, and shunt capacitance across the resistor should be kept to a minimum in order to prevent noise pick-up or instability at low gains. For gain-switched applications it is recommended that reed relays located close to the amplifier be used rather than running leads from a panel switch to the R_G terminals.

3. The differential input terminals require a bias current path to ground and therefore cannot be used with floating inputs. Due to the very low input offset current drift of 20pA/°C, balanced source resistances up to 50K ohms can be used with these amplifiers. For example, 50K ohms x 20pA/°C gives an equivalent input offset voltage drift of 1μV/°C.

4. The guaranteed input offset voltage drifts of 1.0, 0.5, or 0.25 μV/°C include both input and output drifts referred to the input at a gain of 1000. Drifts at other gains are approximately (referred to input):

$$\Delta \text{ Eos } (\mu V/^\circ C) = (\Delta \text{ Eos})_{1000} + \frac{100}{G}$$

ORDERING INFORMATION

AM-201A
AM-201B
AM-201C

Mating Socket: MS-9
Trimming Pot: 100ppm/°C Cermet Type TP50K

THE AM-201 SERIES AMPLIFIERS ARE COVERED BY GSA CONTRACT.

TECHNICAL NOTES (Cont'd)

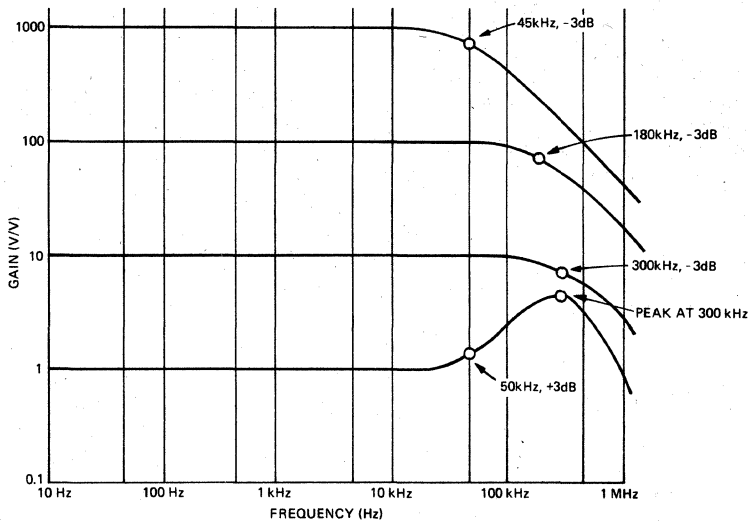
where $[\Delta \text{ Eos}]_{1000}$ is the drift spec. at G=1000 and G is the programmed gain.

5. The sense terminal is normally connected to the output terminals, and the reference terminal is normally connected to ground. For remote loads or for load current sensing, the sense terminal is run separately to the load or to the current sensing resistor. The reference terminal may be connected to a voltage source in the range ±10V in order to directly offset the output of the amplifier by the same amount. Both sense and reference terminals should be connected only to low impedance sources (less than 10 ohms), as any impedance seen by these terminals will degrade the power supply rejection of the amplifier in proportion to the source impedance. A unity gain buffer amplifier can be used to isolate the reference terminal from high impedance sources. See application diagram.

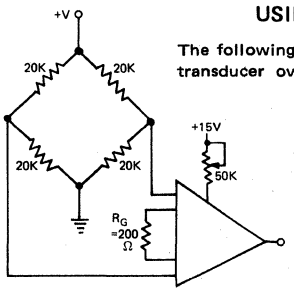
6. The AM-201 series amplifiers have a distinct advantage over many other instrumentation amplifiers in gain-switched applications. Because the gain formula is $200K/R_G$ the switched gain varies precisely inversely with R_G. If R_G is halved, for example, the gain is exactly doubled. Therefore, unlike instrumentation amplifiers with a constant term of 1 in the gain formula, the selection of gain setting resistors is greatly simplified. In switched gain applications the AM-201 amplifiers should be zeroed at the highest gain. The input offset voltage then will not change with gain.

PERFORMANCE DATA

SMALL SIGNAL BANDWIDTH AT SELECTED GAINS



ANALYSIS OF SIGNIFICANT ERROR SOURCES USING BRIDGE TRANSDUCER

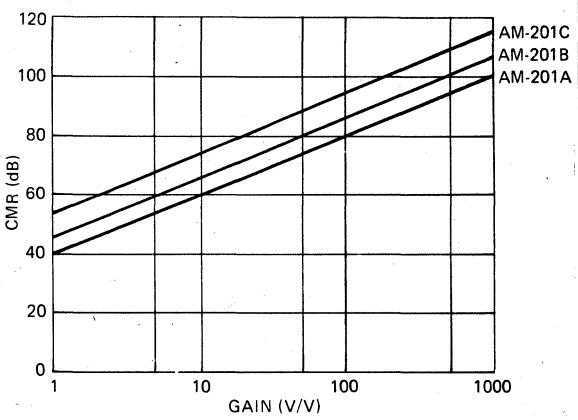


The following errors are computed for an AM-201C operated from a bridge transducer over a ±10°C ambient temperature range at a gain of 1000.

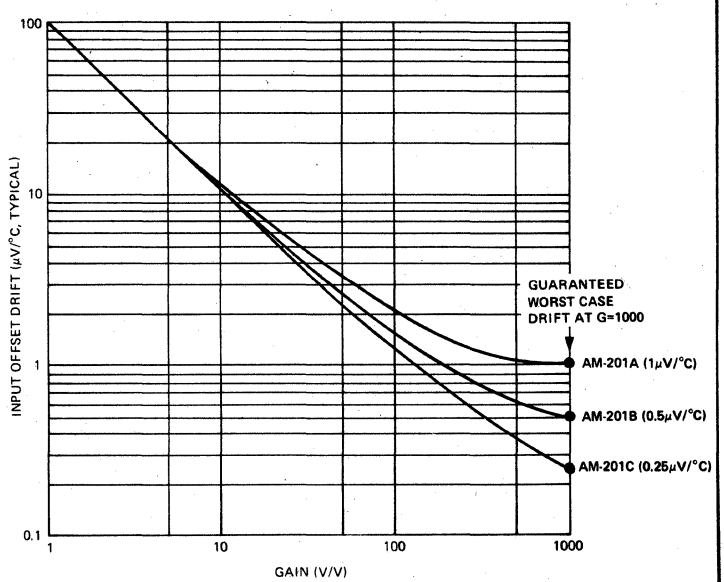
Error Source	Calculation	Error (% 10V FS)
Volt. Offset Drift	.25 μV/°C x 10°C x 1000	.025%
Cur. Offset Drift	20 pA/°C x 10°C x 10K x 1000	.020%
Gain Change	.002%/°C x 10°C	.020%
Noise (.1 to 10 Hz)	1 μV P-P x 1000	.010%
Gain Nonlinearity	.01%	.010%
Power Supply Drift	Negligible	—
	TOTAL OUTPUT ERROR	.085%

Power supply drift (assuming .02%/°C) contributes a negligible amount to the error and therefore the computation is omitted. The total output errors for a 10°C temperature change are less than 0.1%.

COMMON MODE REJECTION RATIO VS. GAIN

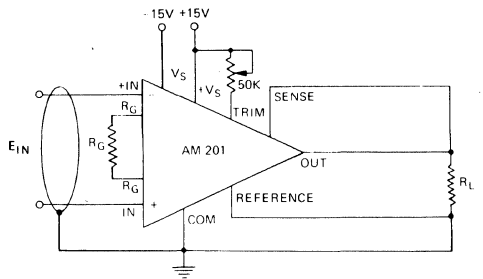


TOTAL VOLTAGE OFFSET DRIFT (REFERRED TO INPUT) VS. GAIN



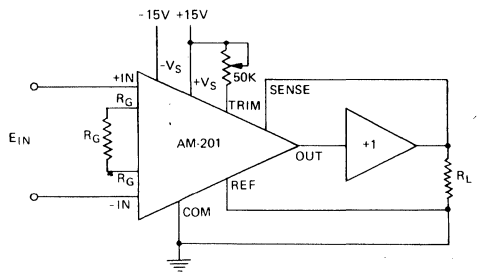
APPLICATION DIAGRAMS

STANDARD CONNECTION

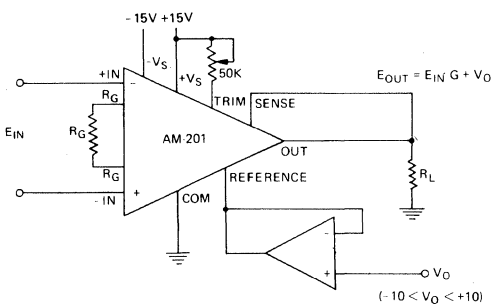


INPUT OFFSET TRIMMING: Short input terminals together and connect to ground or to common mode voltage at which input will be used. Adjust 50K trimming pot for zero output voltage. For critical applications R_G should be a Vishay type S102 and the trimming pot should be a Vishay type 1203. See technical notes.

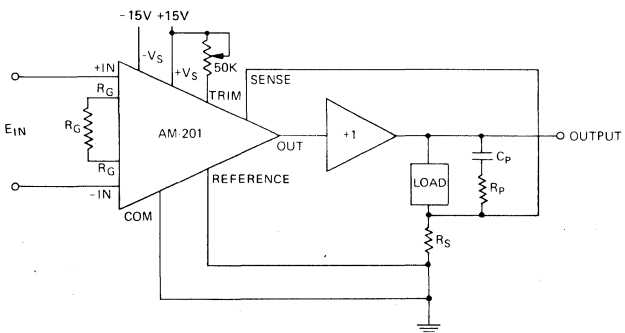
USING AN OUTPUT CURRENT BOOSTER



OFFSETTING THE OUTPUT BY USE OF THE REFERENCE TERMINAL

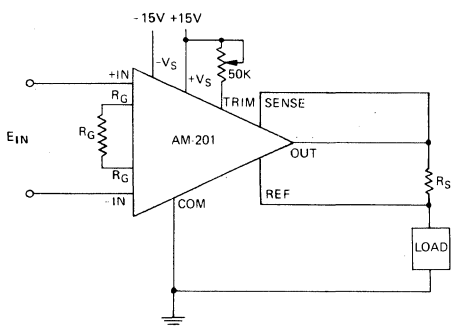


CONNECTION FOR DRIVING LOAD WITH CURRENT BOOSTER USING LOAD CURRENT SENSING

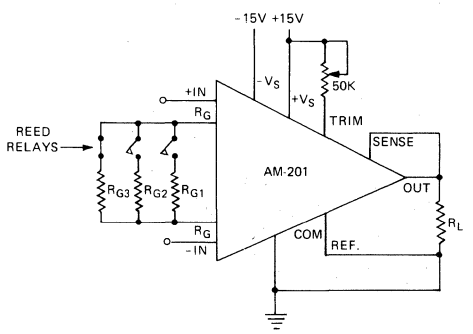


NOTE: The output voltage using the gain equation will appear across R_S. The load impedance and output of the current booster must be compatible with this. Highly inductive loads may cause ringing or oscillation. In this case add R_P and C_P as shown.

DRIVING A GROUNDED LOAD USING CURRENT SENSING



GAIN SWITCHING WITH THE AM-201



Gain is inversely proportional to R_G. Thus if R_G is halved the gain is exactly doubled. Input offset voltage does not change with R_G.

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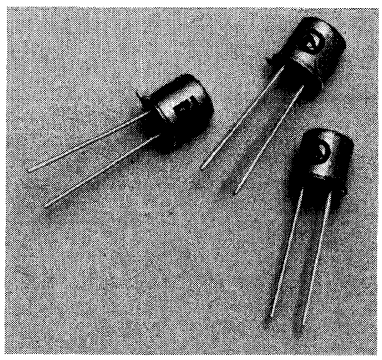
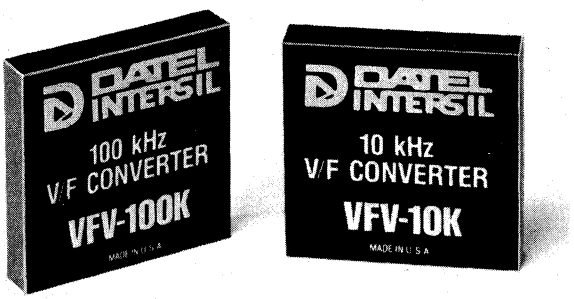
PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Special Functions





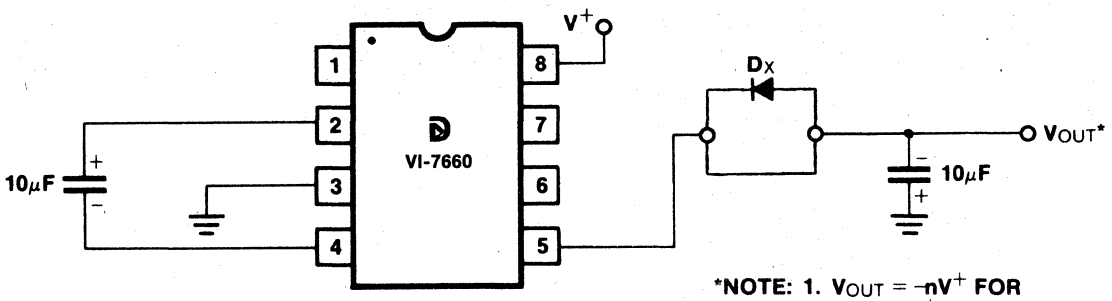
Special Functions

MODEL	DESCRIPTION	NON-LINEARITY % of F.S.	DRIFT/°C	POWER REQUIRE-MENTS	OPER. TEMP. RANGE (°C)	PRICE (1-24)	SEE PAGE
AMC-8013-CC	Four Quadrant Analog	± 0.8	0.06%	± 15VDC	0 to + 70	**$ 5.89**	392C
AMC-8013-CM	Multipliers with Accuracies				− 55 to + 125	**$36.69**	
AMC-8013-BC	To 0.5%. Feature + 10V	+ 0.5			0 to + 70	**$10.84**	
AMC-8013-BM	Input Range, 1MHz Band-				− 55 to + 125	**$56.19**	
AMC-8013-AC	Width, Division or Square				0 to + 70	**$24.84**	
AMC-8013-AM	Root Functions				− 55 to + 125	**$62.79**	
FLT-U2	Universal Active Filter	± 5%	0.01%	± 5 to ± 18V	0 to + 70	**$21.00**	404C
LA-8048-CC	Log Amp. with 6 Decades Input	± 1%	0.8mV	± 15VDC	0 to + 70	**$21.67**	396C
LA-8048-BC	1 Volt/Decade Output	± 0.5%			0 to + 70	**$43.22**	
LA-8049-CC	Anti-Log Amp. with 3	25mV	0.55mV	± 15VDC	0 to + 70	**$21.67**	396C
LA-8049-BC	Decades Voltage Output	10mV	0.38mV		0 to + 70	**$43.22**	
TT-590-I	Two Terminal I.C. Temperature	± 3.0	—	+ 4 to + 30V	− 55 to + 150	**$ 2.70**	410C
TT-590-J	Transducer, 1μ A/°C Output	± 1.5			− 55 to + 150	**$ 3.15**	
TT-590-K	for Temps. from − 55°C to	± 0.8			− 55 to + 150	**$ 6.15**	
TT-590-L	+ 150°C and Supplied from	± 0.4			− 55 to + 150	**$12.15**	
TT-590-M	+ 4V to + 30V	± 0.3			− 55 to + 150	**$27.15**	
VFQ-IC	V/F-F/V Converter	0.25%	40 ppm	± 4 to ± 7.5V	0 to + 70	**$ 6.95**	412C
VFQ-IR	Operates to 100KHz				− 25 to + 85	**$14.25**	
VFV-10K	Modular V/F-F/V Converter	0.005%	20 ppm	± 15VDC	0 to + 70	**$66.00**	416C
VFV-100K	10KHz or 100KHz Versions	0.05%	100 ppm		0 to + 70	**$84.00**	

MODEL	DESCRIPTION	NON-LINEARITY % of F.S.	DRIFT/°C	POWER REQUIREMENTS	OPER. TEMP. RANGE (°C)	PRICE (1-24)	SEE PAGE
VI-7660PC	Monolithic Voltage	—	—	+1.5 to +10V	−20 to +70	**$ 2.99**	422C
VI-7660C	Inverter Provides −1.5 to −10V				−20 to +70	**$ 3.45**	
VI-7660M	From +1.5 to +10V Supplies				−55 to +125	**$ 8.85**	
VR-182A	2.455V Precision	+35mV	100 ppm	2mA	0 to +70	**$ 1.95**	428C
VR-182B	Bandgap Voltage Reference		50 ppm		0 to +70	**$ 2.50**	
VR-182C	with 0.1Ω Dynamic Impedance		30 ppm		0 to +70	**$ 2.95**	
VR-8069-DC	1.2V Precision Bandgap	−20mV, +30mV	100 ppm	.05 to 5mA	0 to +70	**$ 1.90**	430C
VR-8069-DM	Voltage Reference				−55 to +125	**$ 3.70**	
VR-8069-CC	with 1Ω Dynamic		50 ppm		0 to +70	**$ 2.60**	
VR-8069-CM	Impedance				−55 to +125	**$ 5.35**	
VR-8069-BC			25 ppm		0 to +70	**$ 6.85**	
VR-8069-AC			10 ppm		0 to +70	**$15.10**	
WG-8038-CC	Precision Waveform Gen.	+0.5	50 ppm	+10 to +30V or ±5 to ±15V	0 to +70	**$ 4.12**	432C
WG-8038-BC	and Voltage Controlled Osc.	±0.2	100 ppm Max.		0 to +70	**$10.97**	
WG-8038-BM	with Sine, Square Triangle				−55 to +125	**$12.17**	
WG-8038-AC	Sawtooth and Pulse Waveforms		50 ppm, Max.		0 to +70	**$28.57**	
WG-8038-AM	at .001Hz to 1MHz				−55 to +125	**$31.12**	

Special Functions—Problem Solvers

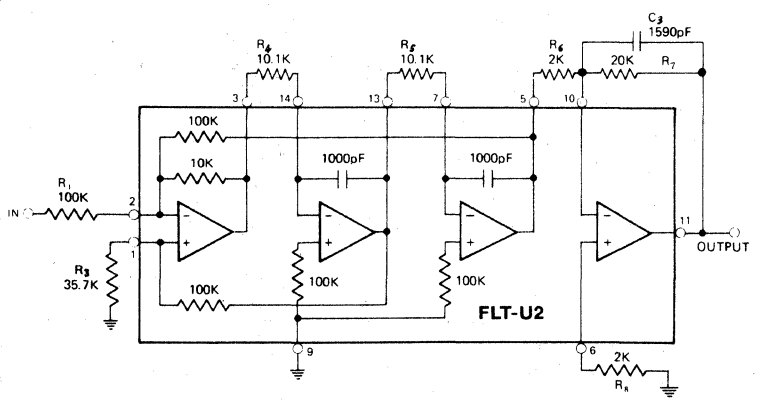
SIMPLE NEGATIVE CONVERTER



DATEL-INTERSIL'S VI-7660 ALLOWS EASY GENERATION OF NEGATIVE SUPPLIES FROM POSITIVE SUPPLIES.

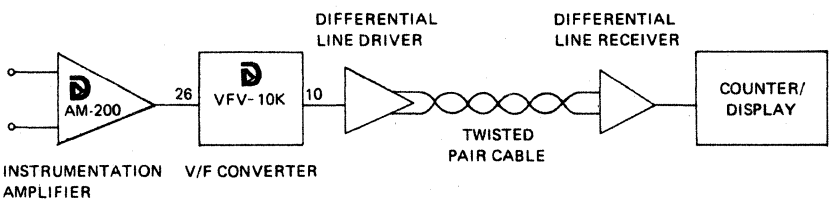
***NOTE: 1. $V_{OUT} = -nV^+$ FOR $1.5V \leq V^+ \leq 6.5V$**
2. $V_{OUT} = -n(V^+ - V_{FDX})$ FOR $6.5 \leq V^+ \leq 10.0V$

STATE VARIABLE ACTIVE FILTER



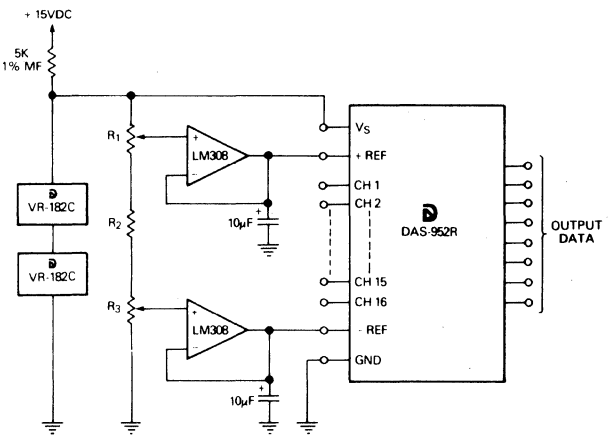
DATEL-INTERSIL'S FLT-U2 ALLOWS A VARIETY OF FILTER FUNCTIONS WITH A MINIMUM OF EXTERNAL COMPONENTS; FOR EXAMPLE, THIS THREE POLE BUTTERWORTH LOW PASS FILTER.

HIGH NOISE IMMUNITY DATA TRANSMISSION



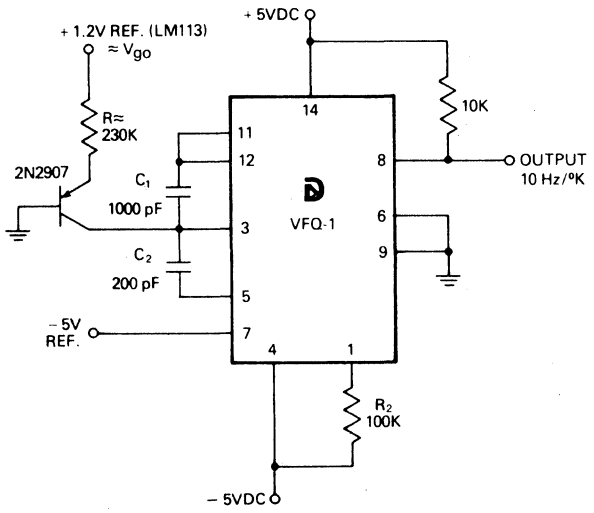
HIGH NOISE IMMUNITY DATA TRANSMISSION SYSTEM USES DATEL-INTERSIL'S VFV-10K.

DUAL ADJUSTABLE REFERENCE



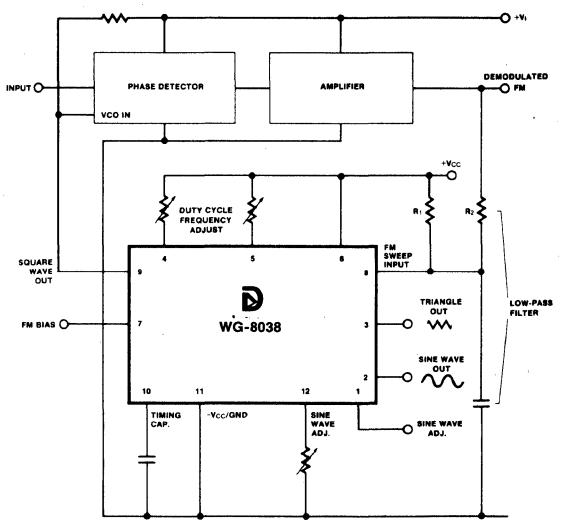
DUAL ADJUSTABLE REFERENCE ACHIEVES VERY GOOD THERMAL PERFORMANCE USING TWO VR-182's

TEMPERATURE TO FREQUENCY CONVERTER



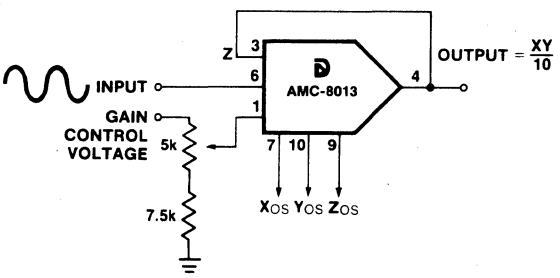
THE VFQ-1 ALLOWS THIS CIRCUIT TO ACHIEVE ACCURACY TO 1°K.

WAVEFORM GENERATOR USED AS STABLE VCO IN A PHASE-LOCKED LOOP.



THE WG-8038 PRODUCES A VARIETY OF WAVEFORM OR PULSE OUTPUTS WITH HIGH ACCURACY, USING A MINIMUM OF EXTERNAL COMPONENTS.

VARIABLE GAIN AMPLIFIER



DATEL-INTERSIL'S AMC-8013 ALLOWS ANALOG MULTIPLICATION, DIVISION AND EXPONENTIATION, OR MAY BE CONFIGURED AS A VARIABLE GAIN AMPLIFIER.

AMC-8013
Four Quadrant Analog Multiplier

FEATURES

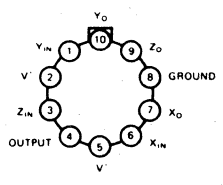
- ±0.5% Accuracy
- Internal Op-Amp for Level Shift, Division and Square Root Functions
- Uses Film Resistors for Minimum External Components
- Full ±10 Volt Input/Output Voltage Range
- Wide Bandwidth – 1 MHz
- Operates with Standard ±15 Volt Supplies

GENERAL DESCRIPTION

The 8013 is a four quadrant analog multiplier whose output is proportional to the algebraic product of two input signals. Feedback around an internal op-amp provides level shifting and can be used to generate division and square root functions. A simple arrangement of potentiometers may be used to trim gain accuracy, offset voltage and feedthrough performance. The high accuracy, wide bandwidth, and increased versatility of the 8013 makes it ideal for all multiplier applications in control and instrumentation systems.

CONNECTION DIAGRAM

TO-100 PACKAGE

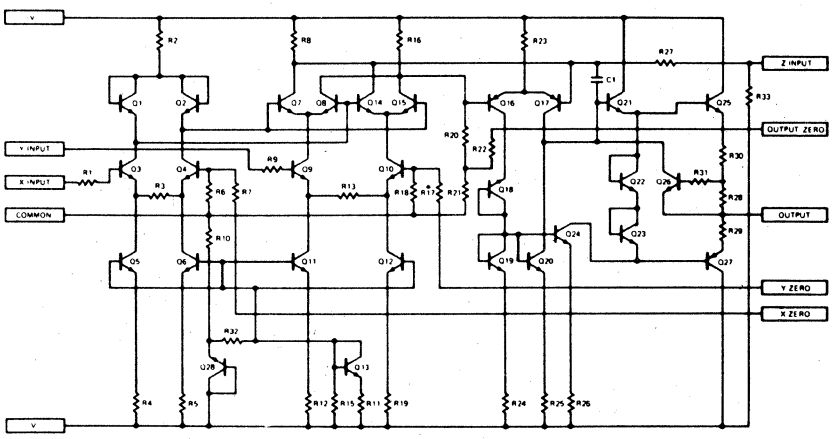


TOP VIEW

APPLICATIONS

- Multiplication, Division, Squaring, Square Roots
- RMS Measurements
- Frequency Doubler
- Balanced Modulator and Demodulator
- Electronic Gain Control
- Function Generator and Linearizing Circuits
- Process Control Systems

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Input Voltages (X, Y, Z, X_o, Y_o, Z_o)	±V Supply
Lead Temperature (60 sec)	300°C
Storage Temperature Range	-65°C to +150°C

NOTE 1: Derate at 6.8 mW/°C for operation at ambient temperature above 75°C.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified $T_A = 25°C$, $V_S = \pm 15V$, Gain and Offset Potentiometers Externally Trimmed)

PARAMETER	CONDITIONS	8013-A			8013-B			8013-C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Multiplier Function			$\frac{XY}{10}$			$\frac{XY}{10}$			$\frac{XY}{10}$		
Multiplication Error	$-10 < X < 10$ $-10 < Y < 10$			.5			1.0			2.0	% Full Scale
Divider Function			$\frac{10Z}{X}$			$\frac{10Z}{X}$			$\frac{10Z}{X}$		
Division Error	$X = -10$		0.3			0.3			0.3		% Full Scale
	$X = -1$		1.5			1.5			1.5		% Full Scale
Feedthrough	$X = 0$ $Y = 20V_{pp}$ $f = 50$ Hz			50			100			200	mV_{pp}
	$Y = 0$ $X = 20V_{pp}$ $f = 50$ Hz			50			100			150	mV_{pp}
Nonlinearity											
X Input	$X = 20V_{pp}$ $Y = \pm 10$ Vdc		±0.5			±0.5			±0.8		%
Y Input	$Y = 20\ V_{pp}$ $X = \pm 10$ Vdc		±0.2			±0.2			±0.3		%
Frequency Response											
Small Signal Bandwidth (-3 dB)			1.0			1.0			1.0		MHz
Full Power Bandwidth			750			750			750		kHz
Slew Rate			45			45			45		V/μs
1% Amplitude Error			75			75			75		kHz
1% Vector Error (0.5° Phase Shift)			5			5			5		kHz
Settling Time (to ±2% of Final Value)	$E_{IN} = \pm 10V$		1			1			1		μs
Overload Recovery (to ±2% of Final Value)			1			1			1		μs
Output Noise	5 Hz to 10 kHz		0.6			0.6			0.6		mVrms
	5 Hz to 5 MHz		3			3			3		mVrms
Input Resistance											
X Input			10			10			10		MΩ
Y Input			6			6			6		MΩ
Z Input			36			36			36		kΩ
Input Bias Current											
X or Y Input			2	5			7.5			10	μA
Z Input			25			25			25		μA
Power Supply Variation											
Multiplication Error			0.2			0.2			0.2		%/%
Output Offset				50			75			100	mV/V
Scale Factor			0.1			0.1			0.1		%/%
Quiescent Current			3.5	6.0		3.5	6.0		3.5	6.0	mA
THE FOLLOWING SPECIFICATIONS APPLY OVER THE OPERATING TEMPERATURE RANGES											
Multiplication Error	$-10 < X < 10$, $-10 < Y < 10$		1.5			2			3		% Full Scale
Average Temperature Coefficient of											
Accuracy			0.06			0.06			0.06		%/°C
Output Offset			0.2			0.2			0.2		mV/°C
Scale Factor			0.04			0.04			0.04		%/°C
Input Bias Current											
X or Y Input				10			10			20	μA
Z Input				70			70			100	μA
Input Voltage (X, Y, or Z)				±10			±10			±10	V
Output Voltage Swing	$R_L \geq 2k$ $C_L \leq 1000$ pF	±10			±10			±10			V

APPLICATIONS INFORMATION

MULTIPLIER Trimming Procedure

1. Set X_{IN} = Y_{IN} = 0V and adjust Z_o for zero Output.
2. Apply a low frequency sweep ($f_o \leq 100$ Hz sine or triangle) of = ±10V to Y_{IN} with X_{IN} = 0V and adjust X_o for minimum Output.
3. Apply the sweep signal of Step 2 to X_{IN} with Y_{IN} = 0V and adjust Y_o for minimum Output.
4. Readjust Z_o as in Step 1, if necessary.
5. With X_{IN} = 10.0V dc and the sweep signal of Step 2 applied to Y_{IN}, adjust the Gain potentiometer for Output = Y_{IN}. This is easily accomplished with a differential scope plug-in (A + B) by inverting one signal and adjusting Gain control for (Output − Y_{IN}) = Zero.

DIVIDER Trimming Procedure

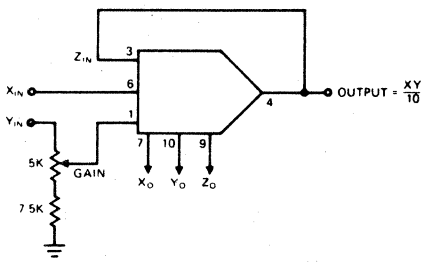
1. Set trimming potentiometers at mid-scale by adjusting voltage on pins 7, 9 and 10 (X_o, Y_o, Z_o) for zero volts.
2. With Z_{IN} = 0V, trim Z_o to hold the Output constant, as X_{IN} is varied from −10V through −1V.
3. With Z_{IN} = 0V and X_{IN} = −10.0V adjust Y_o for zero Output voltage.
4. With Z_{IN} = X_{IN} (and/or Z_{IN} = $-X_{IN}$) adjust X_o for minimum worst-case variation of Output as X_{IN} is varied from −10V to −1V.
5. Repeat Steps 2 and 3 if Step 4 required a large initial adjustment.
6. With Z_{IN} = X_{IN} (and/or Z_{IN} = $-X_{IN}$) adjust the gain control until the output is the closest average around +10.0V (−10V for Z_{IN} = $-X_{IN}$) as X_{IN} is varied from −10V to −3V.

SQUARE ROOT Trimming Procedure

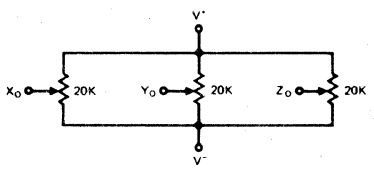
1. Connect the 8013 in the *Divider* configuration.
2. Adjust Z_o, Y_o, X_o and Gain using Steps 1 through 6 of Divider Trimming Procedure.
3. Convert to the Square Root configuration by connecting X_{IN} to the Output and inserting a diode between Pin 4 and the Output node.
4. With Z_{IN} = 0V adjust Z_o for zero Output voltage.

TYPICAL APPLICATIONS

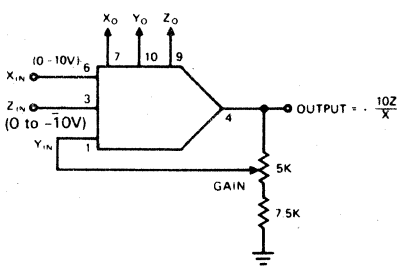
MULTIPLICATION



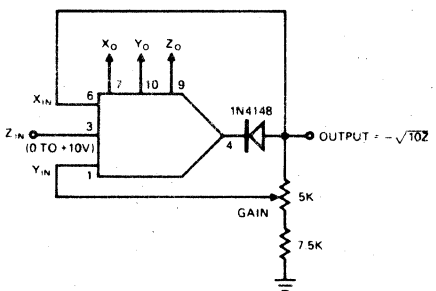
POTENTIOMETERS FOR
TRIMMING OFFSET AND FEEDTHROUGH



DIVISION



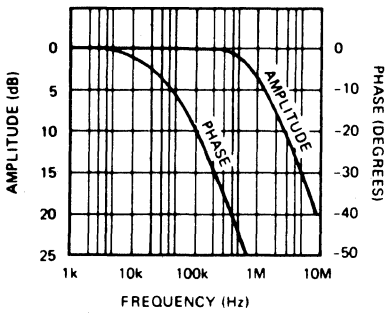
SQUARE ROOT



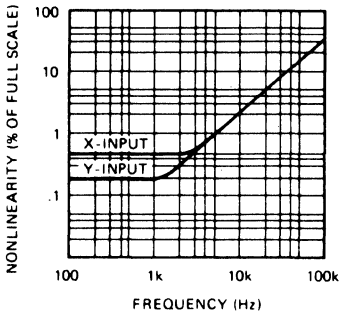
AMC-8013

TYPICAL PERFORMANCE CURVES

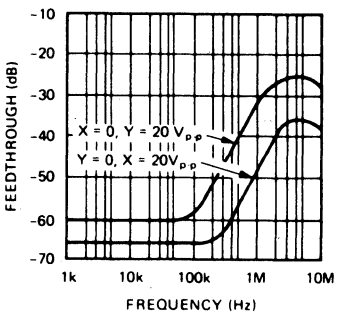
AMPLITUDE AND PHASE AS A FUNCTION OF FREQUENCY



NONLINEARITY AS A FUNCTION OF FREQUENCY



FEEDTHROUGH AS A FUNCTION OF FREQUENCY



DEFINITION OF TERMS

Multiplication/Division Error: This is the basic accuracy specification. It includes terms due to linearity, gain, and offset errors, and is expressed as a percentage of the full scale output.

Feedthrough: With either input at zero the output of an ideal multiplier should be zero regardless of the signal applied to the other input. The output seen in a non-ideal multiplier is known as the feedthrough.

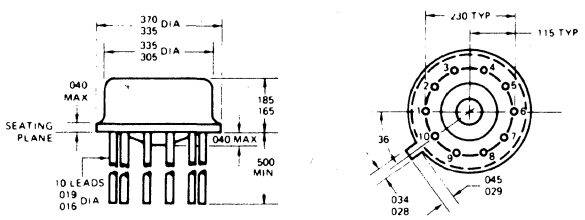
Nonlinearity: The maximum deviation from the best straight line constructed through the output data, expressed as a percentage of full scale. One input is held constant and the other swept through its nominal range. The nonlinearity is the component of the total multiplication/division error which cannot be trimmed out.

ORDERING INFORMATION

Model	Multiplication Error, max.	Oper. Temp. Range (°C)	Package
AMC-8013-CC	±2.0%	0 to +70	TO-100
AMC-8013-CM	±2.0%	−55 to +125	TO-100
AMC-8013-BC	±1.0%	0 to +70	TO-100
AMC-8013-BM	±1.0%	−55 to +125	TO-100
AMC-8013-AC	±0.5%	0 to +70	TO-100
AMC-8013-AM	±0.5%	−55 to +125	TO-100

PACKAGE DIMENSIONS

TO-100



NOTE: Pin 5 connected to case.

LA-8048, LA-8049
Monolithic Log Amplifier
Monolithic Antilog Amplifier

FEATURES

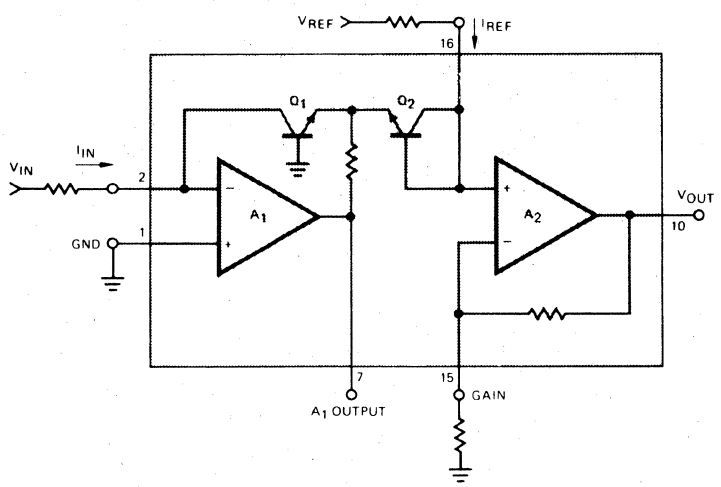
- 1/2% Full Scale Accuracy
- Temperature Compensated 0°C to 70°C
- Scale Factor 1V/Decade, Adjustable
- 120dB Dynamic Current Range (8048)
- 60dB Dynamic Voltage Range (8048 & 8049)
- Dual FET-Input Op-Amps

GENERAL DESCRIPTION

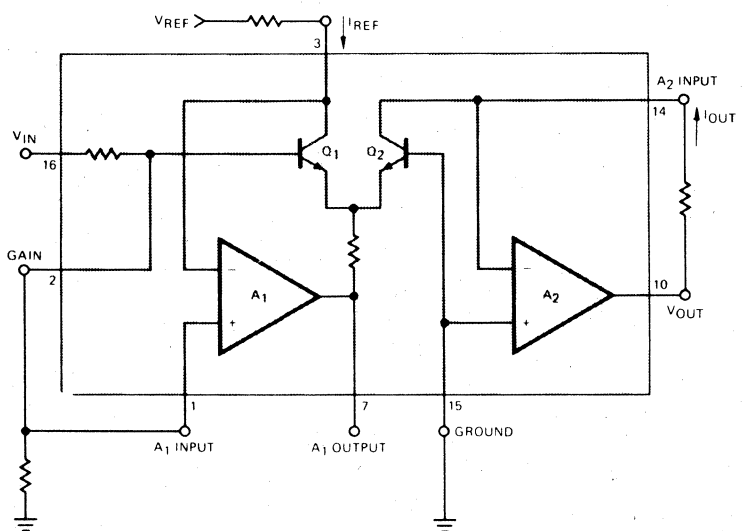
The 8048 is a monolithic logarithmic amplifier capable of handling six decades of current input, or three decades of voltage input. It is fully temperature compensated and is nominally designed to provide 1 volt of output for each decade change of input. For increased flexibility, the scale factor, reference current and offset voltage are externally adjustable.

The 8049 is the antilogarithmic counterpart of the 8048; it nominally generates one decade of output voltage for each 1 volt change at the input.

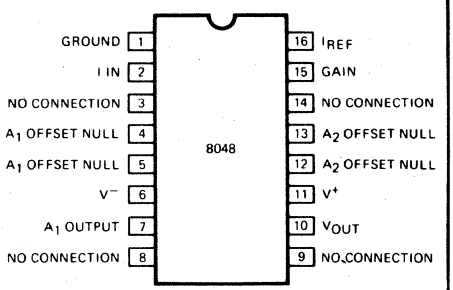
8048 SCHEMATIC DIAGRAM



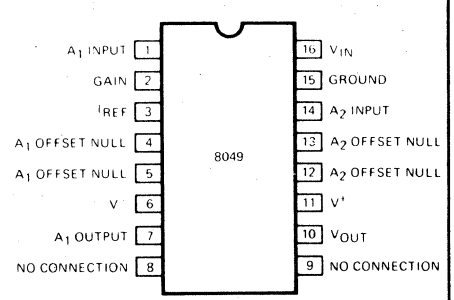
8049 SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



CONNECTION DIAGRAM



LA-8048, LA-8049

MAXIMUM RATINGS

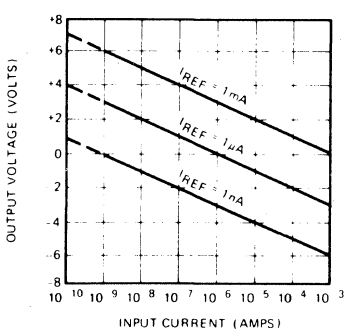
Supply Voltage	±18 V	Operating Temperature Range	0°C to +70°C
I_{in} (Input Current)	2 mA	Output Short Circuit Duration	Indefinite
I_{ref} (Reference Current)	2 mA	Storage Temperature Range	−65°C to +125°C
Voltage between Offset Null and V^+	±0.5 V	Lead Temperature (Soldering, 60 sec.)	300°C
Power Dissipation	750 mW		

ELECTRICAL CHARACTERISTIC (Note 1)

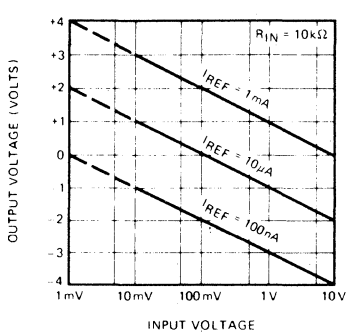
PARAMETER	CONDITION	LA-8048-B MIN.	LA-8048-B TYP.	LA-8048-B MAX.	LA-8048-C MIN.	LA-8048-C TYP.	LA-8048-C MAX.	UNITS
Dynamic Range								
I_{in} (1 nA–1 mA)		120			120			dB
V_{in} (10 mV–10 V)	R_{IN} = 10 kΩ	60			60			dB
Error, % of Full Scale	T_A = 25°C, I_{IN} = 1 nA to 1 mA		.20	0.5		.25	1.0	%
Error, % of Full Scale	T_A = 0°C to +70°C, I_{IN} = 1 nA to 1 mA		.60	1.25		.80	2.5	%
Error, Absolute Value	T_A = 25°C, I_{IN} = 1 nA to 1 mA		12	30		14	60	mV
Error, Absolute Value	T_A = 0°C to +70°C, I_{IN} = 1 nA to 1 mA		36	75		50	150	mV
Temperature Coefficient of V_{OUT}	I_{IN} = 1 nA to 1 mA		0.8			0.8		mV/°C
Power Supply Rejection Ratio	Referred to Output		2.5			2.5		mV/V
Offset Voltage (A_1 & A_2)	Before Nulling		15	25		15	50	mV
Wideband Noise	At Output, for I_{IN} = 100 μA		250			250		μV (RMS)
Output Voltage Swing	R_L = 10 kΩ	±12	±14		±12	±14		V
	R_L = 2 kΩ	±10	±13		±10	±13		V
Power Consumption			150	200		150	200	mW
Supply Current			5	6.7		5	6.7	mA

NOTE 1: Unless otherwise noted, specifications apply for V_S = ±15V, T_A = 25°C, I_{REF} = 1mA, scale factor adjusted for 1V/decade. Accuracy specifications assume that offset voltages and scale factor have been adjusted using the procedure outlined on page 3.

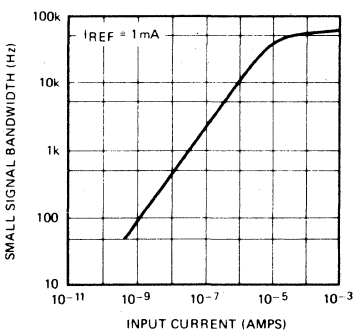
TRANSFER FUNCTION FOR CURRENT INPUTS



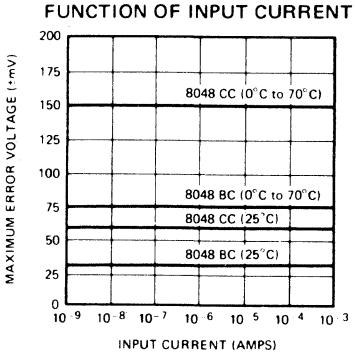
TRANSFER FUNCTION FOR VOLTAGE INPUTS



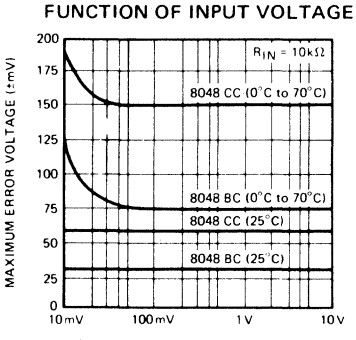
SMALL SIGNAL BANDWIDTH AS A FUNCTION OF INPUT CURRENT



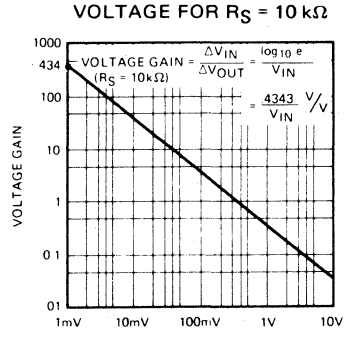
MAXIMUM ERROR VOLTAGE AT THE OUTPUT AS A FUNCTION OF INPUT CURRENT



MAXIMUM ERROR VOLTAGE AT THE OUTPUT AS A FUNCTION OF INPUT VOLTAGE



SMALL SIGNAL VOLTAGE GAIN AS A FUNCTION OF INPUT VOLTAGE FOR R_S = 10 kΩ



THEORY OF OPERATION

The 8049 relies on the same logarithmic properties of the transistor as the 8048. The input voltage forces a specific ΔV_{BE} between Q_1 and Q_2 (Fig. 2). This V_{BE} difference is converted into a difference of collector currents by the transistor pair. The equation governing the behavior of the transistor pair is derived from (2) on Page 3 and is as follows:

$$I_{C_1}/I_{C_2} = \exp\left[q\Delta V_{BE}/kT\right] \quad (5)$$

When numerical values for q/kT are put into this equation, it is found that a ΔV_{BE} of 59mV (at 25°C) is required to change the collector current ratio by a factor of ten. But for ease of application, it is desirable that a 1 volt change at the input generate a tenfold change at the output. The required input attenuation is achieved by the network comprising R_1 and R_2. In order that scale factors other than one decade per volt may be selected, R_2 is external to the chip. It should have a value of 1kΩ, adjustable ±20%, for one decade per volt. R_1 is a thin film resistor deposited on the monolithic chip; its temperature characteristics are chosen to compensate the temperature dependence of equation 5, as explained on Page 3.

The overall transfer function is as follows:

$$I_{OUT}/I_{REF} = \exp\left[\frac{-R_2}{(R_1+R_2)} \times \frac{q\,V_{IN}}{kT}\right] \quad (6)$$

Substituting $V_{OUT} = I_{OUT} \times R_{OUT}$ gives:

$$V_{OUT} = R_{OUT}\, I_{REF} \exp\left[\frac{-R_2}{(R_1+R_2)} \times \frac{q\,V_{IN}}{kT}\right] \quad (7)$$

For voltage references equation 7 becomes

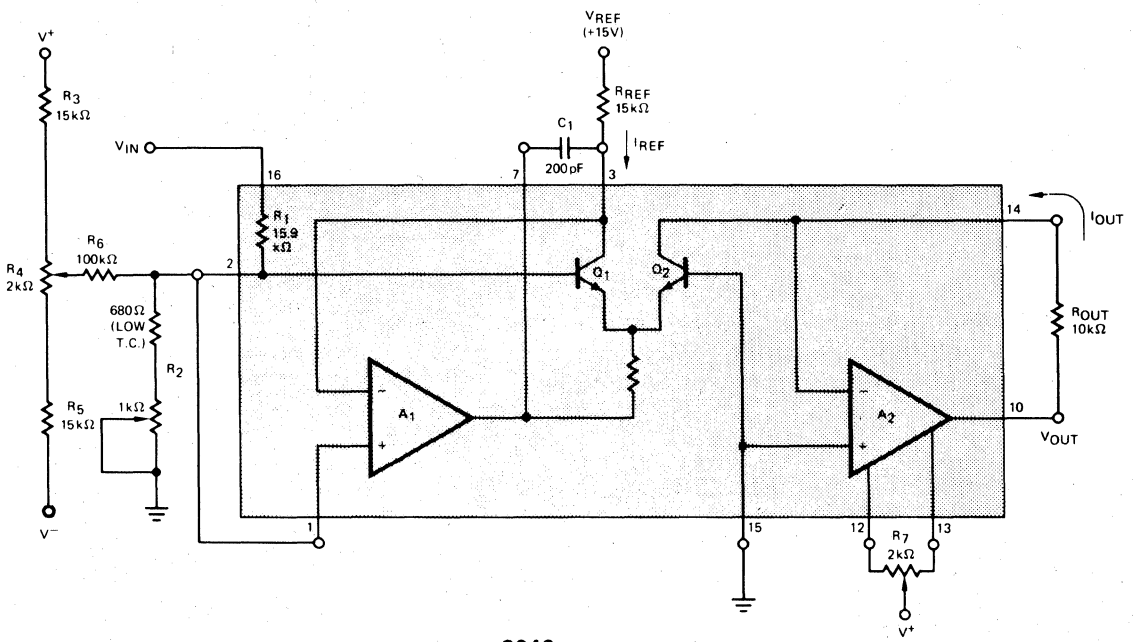
$$V_{OUT} = V_{REF} \times \frac{R_{OUT}}{R_{REF}} \exp\left[\frac{-R_2}{(R_1+R_2} \times \frac{q\,V_{IN}}{kT}\right] \quad (8)$$

OFFSET AND SCALE FACTOR ADJUSTMENT

As with the log amplifier, the antilog amplifier requires three adjustments. The first step is to null out the offset voltage of A_2. This is accomplished by reverse biasing the base-emitter of Q_2. A_2 then operates as a unity gain buffer with a grounded input. The second step forces $V_{IN} = 0$; the output is adjusted for $V_{OUT} = 10V$. This step essentially "anchors" one point on the transfer function. The third step applies a specific input and adjusts the output to the correct voltage. This sets the scale factor. Referring to Fig. 2, the exact procedure for 1 decade/volt is as follows:

1) Connect the input (pin #16) to +15V. This reverse biases the base-emitter of Q_2. Adjust R_7 for $V_{OUT} = 0V$. Disconnect the input from +15V.
2) Connect the input to Ground. Adjust R_4 for $V_{OUT} = 10V$. Disconnect the input from Ground.
3) Connect the input to a precise 2V supply and adjust R_2 for $V_{OUT} = 100mV$.

The procedure outlined above optimizes the performance over a 3 decade range at the output (i. e., V_{OUT} from 10mV to 10V). For a more limited range of output voltages, for example 1V to 10V, it would be better to use a precise 1 volt supply and adjust for $V_{OUT} = 1V$. For other scale factors and/or starting points, different values for R_2 and R_{REF} will be needed, but the same basic procedure applies.



8049
FIGURE 2

LA-8048, LA-8049

MAXIMUM RATINGS

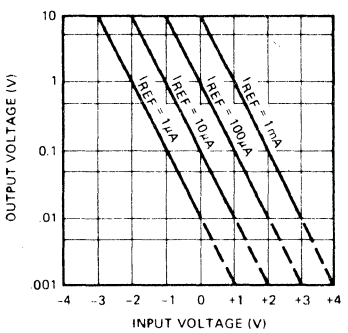
Supply Voltage	±18 V
V_{in} (Input Voltage)	±15 V
I_{ref} (Reference Current)	2 mA
Voltage between Offset Null and V^+	±0.5 V
Power Dissipation	750 mW
Operating Temperature Range	0°C to +70°C
Output Short Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTIC (Note 1)

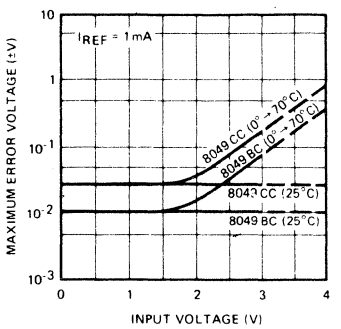
PARAMETER	CONDITION	LA-8049-B MIN.	LA-8049-B TYP.	LA-8049-B MAX.	LA-8049-C MIN.	LA-8049-C TYP.	LA-8049-C MAX.	UNITS
Dynamic Range (V_{OUT})	V_{OUT} = 10mV to 10V	60			60			dB
Error, Absolute Value	T_A = 25°C, 0V≤V_{IN}≤3V		3	10		5	25	mV
Error, Absolute Value	T_A = 0°C to +70°C, 0V≤V_{IN}≤3V		20	75		30	150	mV
Temperature Coefficient, Referred to V_{IN}	V_{IN} = 3V		0.38			0.55		mV/°C
Power Supply Rejection Ratio	Referred to Input, for V_{IN} = 0V		2.0			2.0		μV/V
Offset Voltage (A_1 & A_2)	Before Nulling		15	25		15	50	mV
Wideband Noise	Referred to Input, for V_{IN} = 0V		26			26		μV(RMS)
Output Voltage Swing	R_L = 10kΩ	±12	±14		±12	±14		V
	R_L = 2kΩ	±10	±13		±10	±13		V
Power Consumption			150	200		150	200	mW
Supply Current			5	6.7		5	6.7	mA

NOTE 1: Unless otherwise noted, specifications apply for V_S = ±15V, T_A = 25°C, I_{REF} = 1mA, scale factor adjusted for 1 decade (out) per volt (in). Accuracy specifications assume that offset voltages and scale factor have been adjusted using the procedure on page 5.

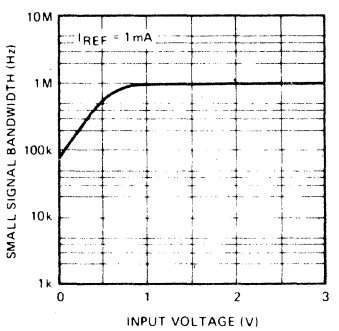
TRANSFER FUNCTION
(V_{OUT} AS A FUNCTION OF V_{IN})



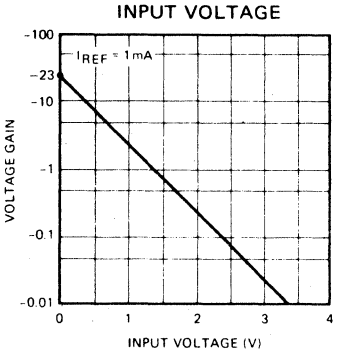
MAXIMUM ERROR VOLTAGE
REFERRED TO THE INPUT AS A
FUNCTION OF V_{IN}



SMALL SIGNAL BANDWIDTH
AS A FUNCTION OF
INPUT VOLTAGE



SMALL SIGNAL VOLTAGE GAIN
AS A FUNCTION OF
INPUT VOLTAGE



THEORY OF OPERATION

The 8048 relies for its operation on the well-known exponential relationship between the collector current and the base-emitter voltage of a transistor:

$$I_C = I_S\left[e^{q\,V_{BE}/kT} - 1\right] \quad (1)$$

For base-emitter voltages greater than 100mV, Eq. (1) becomes

$$I_C = I_S\, e^{q\,V_{BE}/kT} \quad (2)$$

From Eq. (2), it can be shown that for two identical transistors operating at different collector currents, the V_{BE} difference (ΔV_{BE}) is given by:

$$\Delta V_{BE} = -2.303 \times \frac{kT}{q} \log 10 \left[I_{C1}/I_{C2}\right] \quad (3)$$

Referring to Fig. 1, it is clear that the potential at the collector of Q_2 is equal to the ΔV_{BE} between Q_1 and Q_2. The output voltage is ΔV_{BE} multiplied by the gain of A_2:

$$V_{OUT} = -2.303\left(\frac{R_1\,R_2}{R_2}\right)\left(\frac{kT}{q}\right) \log 10 \left[I_{IN}/I_{REF}\right] \quad (4)$$

The expression $2.303 \times \frac{kT}{q}$ has a numerical value of 59mV at 25°C; thus in order to generate 1 volt/decade at the output, the ratio $(R_1 + R_2)/R_2$ is chosen to be 16.9. For this scale factor to hold constant as a function of temperature, the $(R_1 + R_2)/R_2$ term must have a 1/T characteristic to compensate for kT/q.

In the 8048 this is achieved by making R_1 a thin film resistor, deposited on the monolithic chip. It has a nominal value of 15.9kΩ at 25°C, and its temperature coefficient is carefully designed to provide the necessary compensation. Resistor R_2 is external and should be a low T.C. type; it should have a nominal value of 1kΩ to provide 1 volt/decade, and must have an adjustment range of ±20% to allow for production variations in the absolute value of R_1.

OFFSET AND SCALE FACTOR ADJUSTMENT

A log amp, unlike an op-amp, cannot be offset adjusted by simply grounding the input. This is because the log of zero approaches minus infinity; reducing the input current to zero starves Q_1 of collector current and open the feedback loop around A_1. Instead, it is necessary to zero the offset voltage of A_1 and A_2 separately, and then to adjust the scale factor. Referring to Fig. 1, this is done as follows:

1) Temporarily connect a 10kΩ resistor (R_0) between pins 2 and 7. With no input voltage, adjust R_4 until the output of A_1 (pin 7) is zero. Remove R_0.

   Note that for a current input, this adjustment is not necessary since the offset voltage of A_1 does not cause any error for current-source inputs.

2) Set $I_{IN} = I_{REF} = 1mA$. Adjust R_5 such that the output of A_2 (pin 10) is zero.

3) Set $I_{IN} = 1\mu A$, $I_{REF} = 1mA$. Adjust R_2 for V_{OUT} = 3 volts (for a 1 volt/decade scale factor) or 6 volts (for a 2 volt/decade scale factor).

Step #3 determines the scale factor. Setting $I_{IN} = 1\mu A$ optimizes the scale factor adjustment over a fairly wide dynamic range, from 1mA to 1nA. Clearly, if the 8048 is to be used for inputs which only span the range 100μA to 1mA, it would be better to set $I_{IN} = 100\mu A$ in Step #3. Similarly, adjustment for other scale factors would require different I_{IN} and V_{OUT} values.

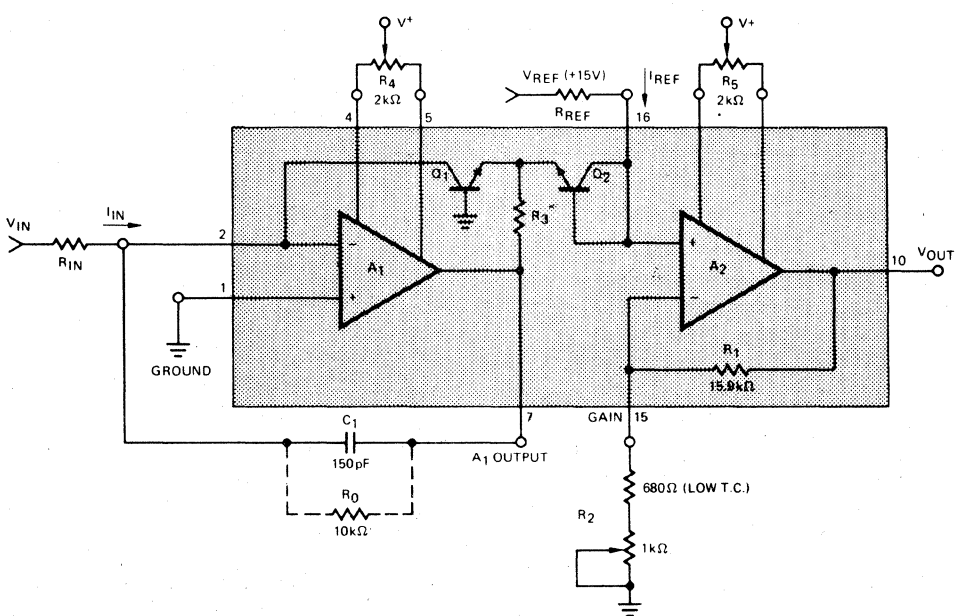


FIGURE 1. 8048 OFFSET AND SCALE FACTOR ADJUSTMENT

APPLICATIONS INFORMATION

Scale Factor Adjustment

The scale factor adjustment procedures outlined on Page 3 (8048) and Page 5 (8049) are primarily directed towards setting up 1 volt (ΔV_{OUT}) per decade (ΔI_{IN} or ΔV_{IN}) for the log amp, or one decade (ΔV_{OUT}) per volt (ΔV_{IN}) for the antilog amp.

This corresponds to K = 1 in the respective transfer functions:

$$\text{Log Amp: } V_{OUT} = -K \log_{10}\left[I_{IN}/I_{REF}\right] \quad (9)$$

$$\text{Antilog Amp: } V_{OUT} = R_{OUT} I_{REF}\ 10^{-V_{IN}/K} \quad (10)$$

By adjusting R_2 (Fig. 1 and Fig. 2) the scale factor "K" in equation 9 and 10 can be varied. The effect of changing K is shown graphically in Fig. 3 for the log amp, and Fig. 4 for the antilog amp. The nominal value of R_2 required to give a specific value of K can be determined from equation 11. It should be remembered that R_1 has a ±20% tolerance in absolute value, so that allowance shall be made for adjusting the nominal value of R_2 by ±20%.

$$R_2 = \frac{941}{(K - .059)}\ \Omega \quad (11)$$

EFFECT OF VARYING "K" ON THE LOG AMPLIFIER

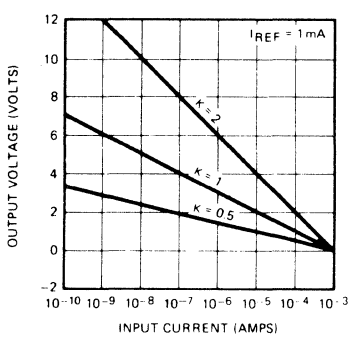


FIGURE 3

EFFECT OF VARYING "K" ON THE ANTILOG AMPLIFIER

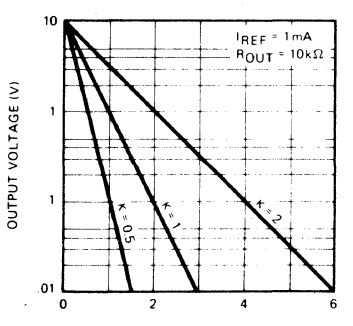


FIGURE 4

Frequency Compensation

Although the op-amps in both the 8048 and the 8049 are compensated for unity gain, some additional frequency compensation is required. This is because the log transistors in the feedback loop add to the loop gain. In the 8048, 150 pF should be connected between Pins 2 and 7 (Fig. 1). In the 8049, 200 pF between Pins 3 and 7 is recommended (Fig. 2).

Error Analysis

Performing a meaningful error analysis of a circuit containing log and antilog amplifiers is more complex than dealing with a similar circuit involving only op-amps. In this data sheet every effort has been made to simplify the analysis task, without in any way compromising the validity of the resultant numbers.

The key difference in making error calculations in log/antilog amps, compared with op-amps, is that the gain of the former is a function of the input signal level. Thus, it is necessary, when referring errors from output to input, or vice versa, to check the input voltage level, then determine the gain of the circuit by referring to the graphs given on Pages 2 and 4.

The various error terms in the log amplifier, the 8048, are referred to the output (RTO) of the device. The error terms in the antilog amplifier, the 8049, are referred to the input (RTI) of the device. The errors are expressed in this way because in the majority of systems a number of log amps interface with an antilog amp, as shown in Fig. 5.

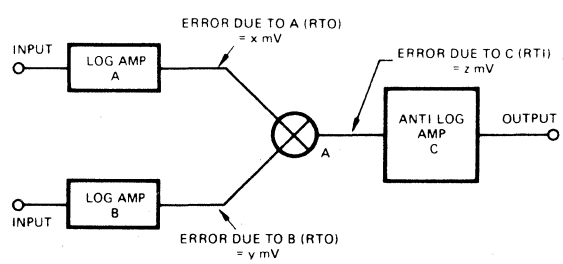


FIGURE 5

It is very straightforward to estimate the system error at node (A) by taking the square root of the sum-of-the squares of the errors of each contributing block.

$$\text{Total Error} = \sqrt{x^2 + y^2 + z^2} \quad \text{at (A)}$$

If required, this error can be referred to the system output through the voltage gain of the antilog circuit, using the voltage gain plot on Page 4.

The numerical values of x, y, and z in the above equation are obtained from the maximum error voltage plots given on Pages 2 and 4. For example, with the 8048BC, the maximum error at the output is 30mV at 25°C. This means that the measured output will be within 30mV of the theoretical transfer function, provided the unit has been adjusted per the procedures on Page 3. Fig. 6 illustrates this point.

To determine the maximum error over the operating temperature range, the 0 to 70°C absolute error values given in the table of electrical characteristics should be used. For intermediate temperatures, assume a linear increase in the error between the 25°C value and the 70°C value.

For the antilog amplifier, the only difference is that the error refers to the input, i. e., the horizontal axis. It will be noticed that the maximum error voltage of the 8049, over the temperature range, is strongly dependent on the input voltage. This is because the output amplifier, A_2, has an offset voltage drift which is directly transmitted to the output. When this error is referred to the input, it must be divided by the voltage gain, which is input voltage dependent. At V_{IN} = 3V, for example, errors at the output are multiplied by 1/.023 (= 43.5) when referred to the input.

It is important to note that both the 8048 and the 8049 require positive values of I_{REF}, and the input and output currents (or voltages) respectively must also be positive. Application of negative I_{IN} to the 8048 or negative I_{REF} to either circuit will cause malfunction, and if maintained for long periods, would lead to device degradation. Some protection can be provided by placing a diode between pin 7 and ground.

SETTING UP THE REFERENCE CURRENT

In both the 8048 and the 8049 the input current reference pin (I_{REF}) is not a true virtual ground. For the 8048, a fraction of the output voltage is seen on Pin 16 (Fig. 1). This does not constitute an appreciable error provided V_{REF} is much greater than this voltage. A 10V or 15V reference satisfies this condition. For the 8049, a fraction of the input voltage appears on Pin 3 (Fig. 2), placing a similar restraint on the value of V_{REF}.

Alternatively, I_{REF} can be provided from a true current source. One method of implementing such a current source is shown in Fig. 7.

LOG OF RATIO CIRCUIT, DIVISION

The 8048 may be used to generate the log of a ratio by modulating the I_{REF} input. The transfer function remains the same, as defined by equation 9:

$$V_{OUT} = -K \log_{10}\left[\frac{I_{IN}}{I_{REF}}\right] \qquad (9)$$

Clearly it is possible to perform division using just one 8048, followed by an 8049. For multiplication, it is generally necessary to use two log amps, summing their outputs into an antilog amp.

To avoid the problems caused by the I_{REF} input not being a true virtual ground (discussed in the previous section), the circuit of Fig. 7 is again recommended if the I_{REF} input is to be modulated.

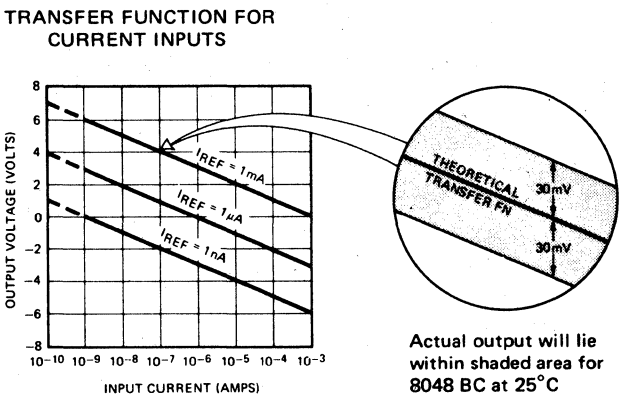


FIGURE 6

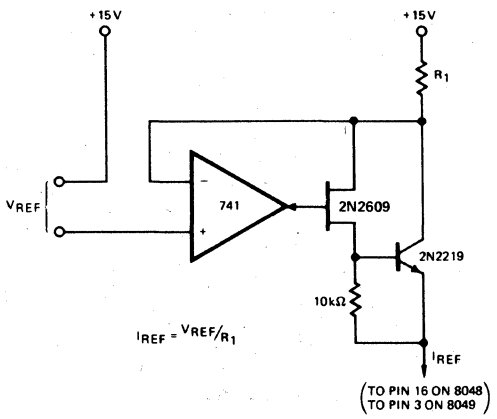


FIGURE 7

DEFINITION OF TERMS

In the definitions which follow, it will be noted that the various error terms are referred to the output of the log amp, and to the input of the antilog amp. The reason for this is explained on Page 6.

DYNAMIC RANGE The dynamic range of the 8048 refers to the range of input voltages or currents over which the device is guaranteed to operate. For the 8049 the dynamic range refers to the range of output voltages over which the device is guaranteed to operate.

ERROR, ABSOLUTE VALUE The absolute error is a measure of the deviation from the theoretical transfer function, after performing the offset and scale factor adjustments as outlined on Pages 3 (8048) or 5 (8049). It is expressed in mV and referred to the linear axis of the transfer function plot. Thus, in the case of the 8048, it is a measure of the deviation from the theoretical output voltage for a given input current or voltage. For the 8049 it is a measure of the deviation from the theoretical input voltage required to generate a specific output voltage.

The absolute error specification is guaranteed over the dynamic range.

ERROR, % OF FULL SCALE The error as a percentage of full scale can be obtained from the following relationship:

$$\text{Error, \% of Full Scale} = \frac{100 \times \text{Error, absolute value}}{\text{Full Scale Output Voltage}}$$

TEMPERATURE COEFFICIENT OF V_{OUT} OR V_{IN} For the 8048 the temperature coefficient refers to the drift with temperature of V_{OUT} for a constant input current.

For the 8049 it is the temperature drift of the input voltage required to hold a constant value of V_{OUT}.

POWER SUPPLY REJECTION RATIO The ratio of the voltage change in the linear axis of the transfer function (V_{OUT} for the 8048, V_{IN} for the 8049) to the change in the supply voltage, assuming that the log axis is held constant.

WIDEBAND NOISE For the 8048, this is the noise occurring at the output under the specified conditions. In the case of the 8049, the noise is referred to the input.

SCALE FACTOR For the log amp, the scale factor (K) is the voltage change at the output for a decade (i. e. 10:1) change at the input. For the antilog amp, the scale factor is the voltage change required at the input to cause a one decade change at the output. See equations 9 and 10.

ORDERING INFORMATION

LOGARITHMIC AMPLIFIER

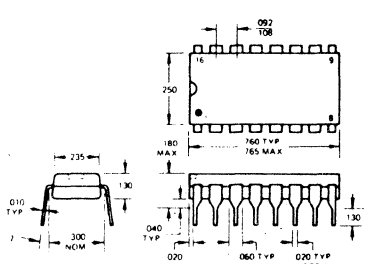
MODEL	MAX. ERROR	OPER. TEMP RANGE	PACKAGE
LA-8048-BC	30mV	0 to +70° C	16 pin Plastic DIP
LA-8048-CC	60mV		

ANTI-LOGARITHMIC AMPLIFIER

MODEL	MAX. ERROR	OPER. TEMP RANGE	PACKAGE
LA-8049-BC	10mV	0 to +70° C	16 pin Plastic DIP
LA-8049-CC	25mV		

PACKAGE DIMENSIONS

16 PIN PLASTIC DIP



Microelectronic Universal Active Filter Model FLT-U2

FEATURES

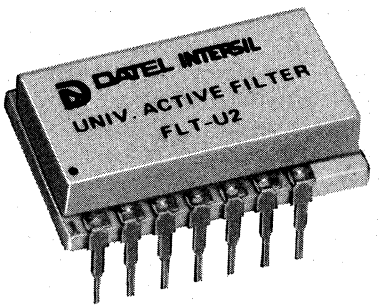
- State Variable Filter
- LP, BP, or HP Functions
- 2 Pole Response
- Low Noise Op Amps
- 16-Pin DIP
- Low Cost

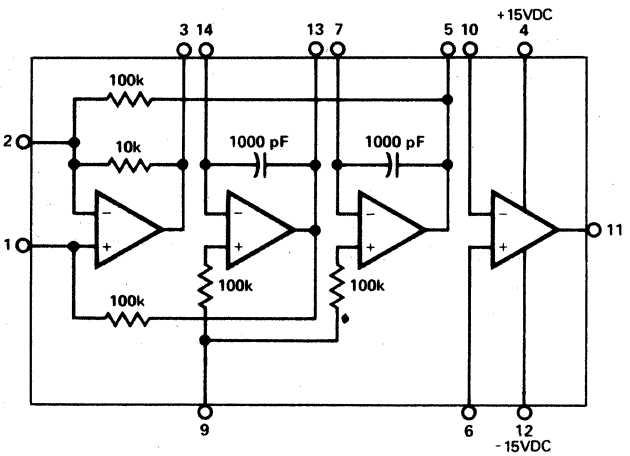
GENERAL DESCRIPTION

The FLT-U2 is a universal active filter manufactured with thick-film hybrid technology. It uses the state variable active filter principle to implement a second order transfer function. Three committed operational amplifiers are used for the second order function while a fourth uncommitted op amp can be used as a gain stage, summing amplifier, buffer amplifier, or to add another independent real pole.

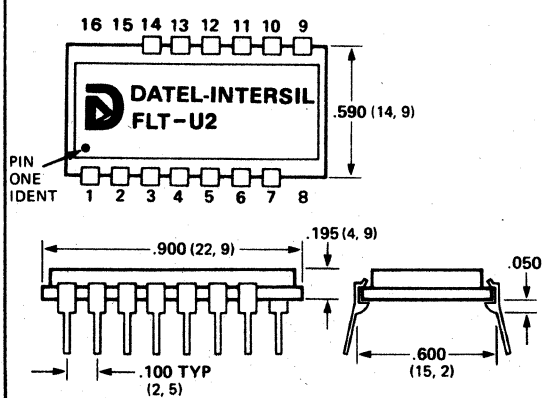
Two-pole lowpass, bandpass, and highpass output functions are available simultaneously from three different outputs, and notch and allpass functions are available by combining these outputs in the uncommitted op amp. To realize higher order filters, several FLT-U2's can be cascaded. Q range is from 0.1 to 1,000 and resonant frequency range is 0.001 Hz to 200 kHz. Frequency stability is .01%/°C and resonant frequency accuracy is within ±5% of calculated values. Frequency tuning is done by two external resistors and Q tuning by a third external resistor. For resonant frequencies below 50 Hz two external tuning capacitors must be added. Exact tuning of the resonant frequency is done by varying one of the resistors around its calculated value.

The internal op amps in the FLT-U2 have 3 MHz gain bandwidth products and a wideband input noise specification of only 10nV/√Hz. This results in considerably improved operation over most other competitive active filters which employ lower performance amplifiers. By proper selection of external components any of the popular filter types such as Butterworth, Bessel, Chebyshev, or Elliptic may be designed. Applications include audio, tone signalling, sonar, data acquisition, and feedback control systems.

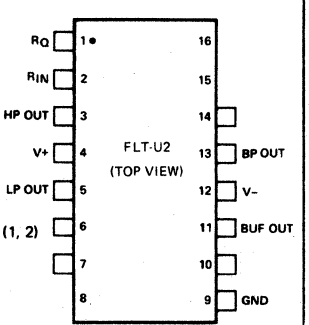




MECHANICAL DIMENSIONS INCHES (MM)



CONNECTIONS DIAGRAM



DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, FLT-U2

Typical at 25°C, ±15V supplies, unless otherwise stated

FILTER CHARACTERISTICS

Frequency Range[1]	0.001 Hz to 200 kHz
Q Range[1]	0.1 to 1,000
f_0 Accuracy	±5%
f_0 Temperature Coefficient	0.01%/°C
Voltage Gain[1]	0.1 to 1,000

AMPLIFIER CHARACTERISTICS

Input Offset Voltage	0.5 mV typ., 6 mV max.
Input Bias Current	40 nA typ., 500 nA max.
Input Offset Current	5 nA typ., 200 nA max.
Input Impedance	5 Megohms
Input Com. Mode Voltage Range	±12V min.
Input Voltage Noise, wideband	$10nV/\sqrt{Hz}$
Output Voltage Range	±10V min.
Output Current	±5mA min.
Open Loop Voltage Gain	300,000
Common Mode Rejection Ratio	100 dB
Power Supply Rejection	10 μV/V
Unity Gain Bandwidth	3 MHz
Slew Rate	1 V/μsec.

POWER SUPPLY REQUIREMENT

Voltage, rated performance	±15 VDC
Voltage Range, operating	±5V to ±18V
Quiescent Current	10 mA max.

PHYSICAL-ENVIRONMENTAL

Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−25°C to +85°C
Case	Ceramic 16-pin DIP (double-spaced)

NOTE: 1. $f_0Q \leq 2 \times 10^6$

ORDERING INFORMATION

THE FLT-U2 IS COVERED BY GSA CONTRACT.

TECHNICAL NOTES

1. The FLT-U2 has simultaneous lowpass, bandpass, and highpass output functions. The chosen output for a particular function will be at unity gain based on Tables II and III. This means that the other two unused outputs will be at other gain levels. The gain of the lowpass output is always 10 dB higher than the gain of the bandpass output and 20 dB higher than the gain of the highpass output.

2. When tuning the filter and checking it over its frequency range, the outputs should be checked with a scope to make sure there is no waveform clipping present, as this will affect the operation of the filter. In particular the lowpass output should be checked since its gain is the highest.

3. f_1, the center frequency for bandpass and the cutoff frequency for lowpass or highpass, should be checked at the bandpass output. Here the peaking frequency can easily be determined for high Q filters and the 0° or 180° phase frequency can easily be determined for low Q filters (depending on whether inverting or noninverting).

4. Tuning resistors should be 1% metal film resistors with 100 ppm/°C temperature stability or better for best performance. Likewise external tuning capacitors should be NPO ceramic or other stable capacitor types.

THEORY OF OPERATION

The FLT-U2 block diagram is shown in Figure 1. This is a second order state-variable filter using three operational amplifiers. Lowpass, bandpass, and highpass transfer functions are simultaneously produced at its three output terminals. These three transfer functions are characterized by the following second order equations:

$$H(s) = \frac{K_1}{S^2 + \frac{\omega_0}{Q} S + \omega_0^2} \quad \text{LOWPASS}$$

$$H(s) = \frac{K_2 S}{S^2 + \frac{\omega_0}{Q} S + \omega_0^2} \quad \text{BANDPASS}$$

$$H(s) = \frac{K_3 S^2}{S^2 + \frac{\omega_0}{Q} S + \omega_0^2} \quad \text{HIGHPASS}$$

where K_1, K_2, and K_3 are arbitrary gain constants.

A second order system is characterized by the location of its poles in the s-plane as shown in Figure 2. The natural radian frequency of this system is ω_0. In Hertz this is $f_0 = \frac{\omega_0}{2\pi}$.

THEORY OF OPERATION, (Cont'd)

The resonant radian frequency of the circuit is different from the natural radian frequency and is:

$$\omega_1 = \omega_0 \sin \phi = \sqrt{\omega_0^2 - \sigma_1^2}$$

The damping factor d determines the amount of peaking in the filter frequency response and is defined as:

$$d = \cos \phi$$

The point at which the peaking becomes zero is called "critical damping" and is $d = \sqrt{2}/2$.

Q is found from d and is a measure of the sharpness of the resonance of the peaking:

$$Q = \frac{1}{2d}$$

$$\text{Also, } Q = \frac{f_0}{-3 \text{ dB Bandwidth}} = \frac{\omega_0}{2\sigma_1}$$

For high Q filters the natural frequency and resonant frequency are approximately equal:

$$\omega_1 \simeq \omega_0 \text{ or } f_1 \simeq f_0$$

This is true since $\omega_1 = \omega_0 \sin \phi$ and $\sin \phi \simeq 1$ as the poles move close to the $j\omega$ axis in the s-plane.

For high Q's ($Q > 1$) we therefore have for the second order filter:

$f_0 \simeq$ Bandpass center frequency
$\simeq$ Lowpass corner frequency
$\simeq$ Highpass corner frequency

In the simplified tuning procedure which follows, the tuning is accomplished by independently setting the natural frequency and Q of the filter. This is done most simply by assuming unity gain for the output of the desired filter function. Unity gain means a gain of one (±) at DC for lowpass, at center frequency for bandpass, and at high frequency ($f >> f_0$) for highpass. Unity gain does not apply to all outputs simultaneously but only to the chosen output based on the component values given in the tables. Figure 3 shows the relative gains of the three simultaneous outputs assuming the bandpass gain is set to unity. Note that lowpass gain is always 10 dB higher than bandpass gain and highpass gain is always 10 dB lower than bandpass gain.

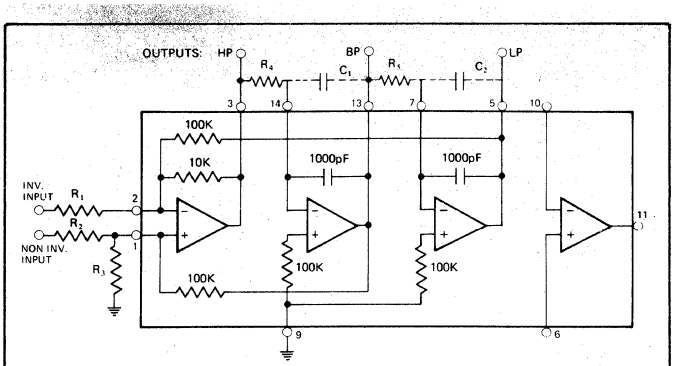


Figure 1.
FLT-U2 Block Diagram

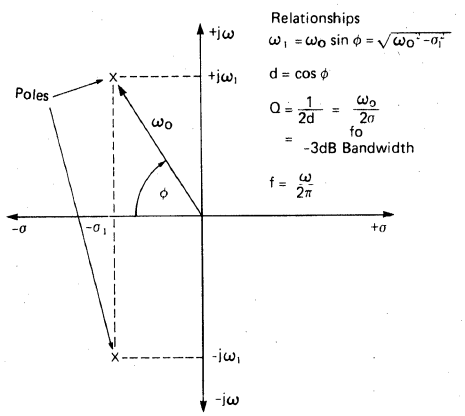


Figure 2.
S-Plane Diagram

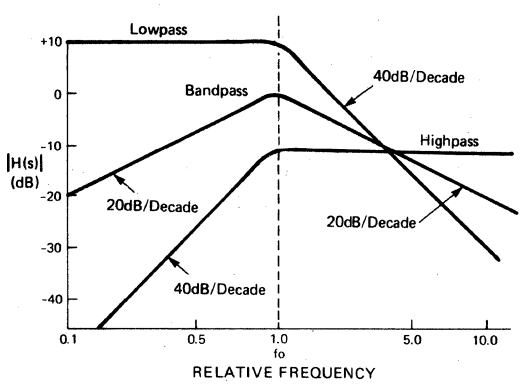


Figure 3.
Relative Gains of Simultaneous Outputs, Q=1

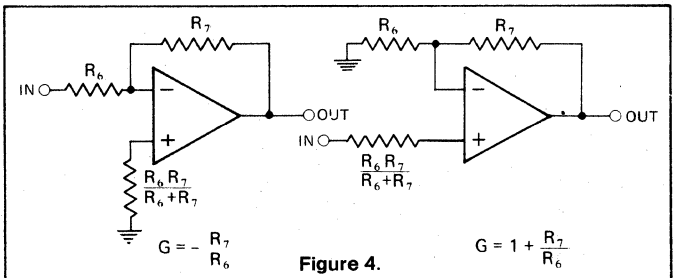


Figure 4.
Uncommitted Op Amp Gain Configurations

SIMPLIFIED TUNING PROCEDURE

1. Select the desired transfer function (lowpass, bandpass, or highpass) and inverted or noninverted output. From this determine the filter configuration (inverting or noninverting) using Table I.

TABLE I FILTER CONFIGURATION

	LP	BP	HP
INVERTING INPUT	INV.	NON-INV	INV
NONINVERTING INPUT	NON-INV.	INV	NON-INV

2. Starting with the desired natural frequency and Q (determined from the filter transfer function or s-plane diagram), compute f_0Q. For $f_0Q > 10^4$ the actual realized Q will exceed the calculated value. At $f_0Q = 10^4$ the increase is about 1% and at $f_0Q = 10^5$ it is about 20%

3. **Inverting Configuration.** Using the value of Q from Step 2 find R_1 and R_3 from Table II. R_2 is open, or infinite.

TABLE II INVERTING CONFIGURATION

	R_1	R_2	R_3
LOWPASS	100K	OPEN	$\frac{100K}{3.80\ Q-1}$
BANDPASS	$Q \times 31.6K$	OPEN	$\frac{100K}{3.48Q}$
HIGHPASS	10K	OPEN	$\frac{100K}{6.64Q-1}$

4. **Noninverting Configuration.** Using the value of Q from Step 2 find R_2 and R_3 from Table III. R_1 is open, or infinite.

TABLE III NONINVERTING CONFIGURATION

	R_1	R_2	R_3
LOWPASS	OPEN	$\frac{316K}{Q}$	$\frac{100K}{3.16Q-1}$
BANDPASS	OPEN	100K	$\frac{100K}{3.48Q-1}$
HIGHPASS	OPEN	$\frac{31.6K}{Q}$	$\frac{100K}{0.316Q-1}$

5. Using the value of f_0 from Step 2, set the natural frequency of the filter by finding R_4 and R_5 from the equation:

$$R_4 = R_5 = \frac{5.03 \times 10^7}{f_0}$$

where R_4 and R_5 are in ohms and f_0 is in Hertz. The natural frequency varies as $\sqrt{R_4R_5}$ and therefore one value may be increased and the other decreased and the natural frequency will be constant if the geometric mean is constant. To maintain constant bandwidth at the bandpass output while varying center frequency, fix R_4 and vary R_5.

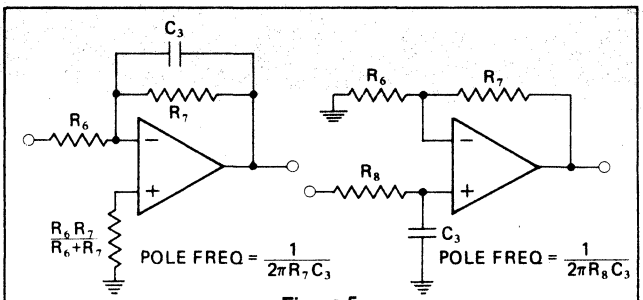


Figure 5.
Using the Uncommitted Op Amp to Add a Real Axis Pole

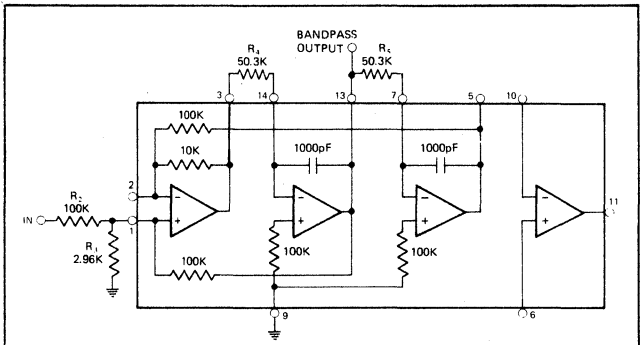


Figure 6.
Bandpass Filter Example

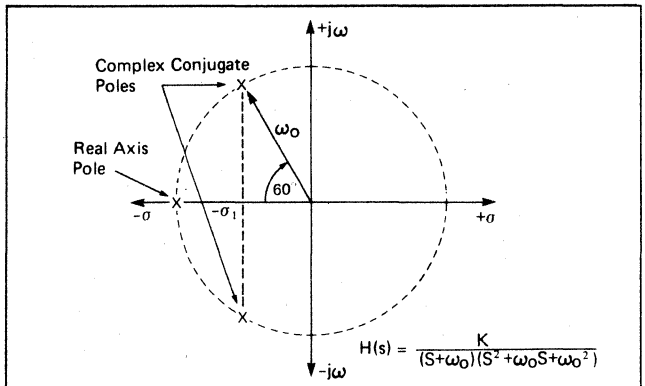


Figure 7.
S-Plane Diagram of 3-Pole Butterworth Lowpass Filter

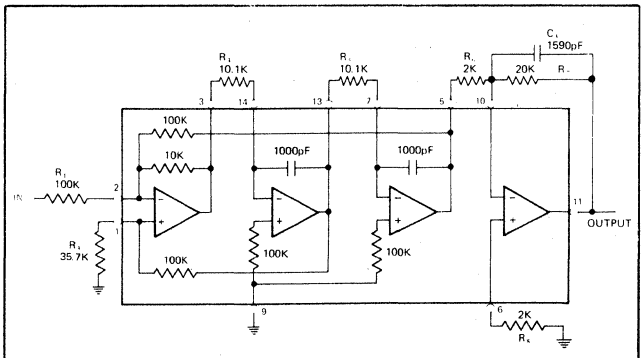


Figure 8.
Three Pole Butterworth Low Pass Filter Example

SIMPLIFIED TUNING PROCEDURE,(Cont'd)

6. For $f_0 < 50$ Hz the internal 1000pF capacitors should be shunted with external capacitors across pins 5 & 7 and 13 & 14. If equal value capacitors are used, R_4 and R_5 are then computed from:

$$R_4 = R_5 = \frac{5.03 \times 10^{10}}{f_0 C} \text{ (C in pF)}$$

For unequal value capacitors this becomes:

$$R_4 = R_5 = \frac{5.03 \times 10^{10}}{f_0\sqrt{C_1 C_2}} \text{ } (C_1C_2 \text{ in pF})$$

In both cases the capacitance is the sum of the external values and the internal 1000 pF values.

7. This procedure is based on unity gain output for the desired function. For additional gain, the fourth uncommitted operational amplifier should be used as an inverting or noninverting gain stage following the selected output. See Figure 4. A third pole on the real axis of the s-plane may also be added to the transfer function by adding a capacitor to the gain stage as shown in Figure 5.

FILTER DESIGN EXAMPLES

Bandpass Filter With 1kHz Center Frequency, Q = 10, and Inverted Output

1. From Table I the noninverting configuration is chosen to realize an inverted bandpass output. $f_0Q = 10^4$ which means the realized Q will be about 1% higher than calculated.

2. From Table III, using Q = 10, we find:

R_1 = open
R_2 = 100K ohms
$R_3 = \frac{100K}{3.48Q-1} = \frac{100K}{33.8} = 2.96K$ ohms

3. Using f_0 of 1 kHz, R_4 and R_5 are found from the equation.

$$R_4 = R_5 = \frac{5.03 \times 10^7}{1000} = 50.3K \text{ ohms}$$

4. This completes the filter design which is shown in Figure 6. To choose the nearest 1% standard value resistors either 49.9K or 51.1K ohms could be used; likewise one value of 49.9K and one of 51.1K could be used giving the geometric mean of $\sqrt{R_4R_5} = \sqrt{49.9K \times 51.1K} = 50.5K$ which is even closer. But due to the filter ±5% frequency tolerance it may be better to hold R_4 constant while varying R_5 to tune it exactly.

Three-Pole Noninverting Butterworth Low Pass Filter With DC Gain Of 10 And Cutoff Frequency Of 5 kHz.

The s-plane diagram of the 3-pole Butterworth filter is shown in Figure 7. We will use a second order filter to realize the two complex conjugate poles and the uncommitted op amp to provide the third real axis pole and a DC gain of 10.

1. From Table I, the noninverting filter configuration would normally be used to give a noninverting low pass output.

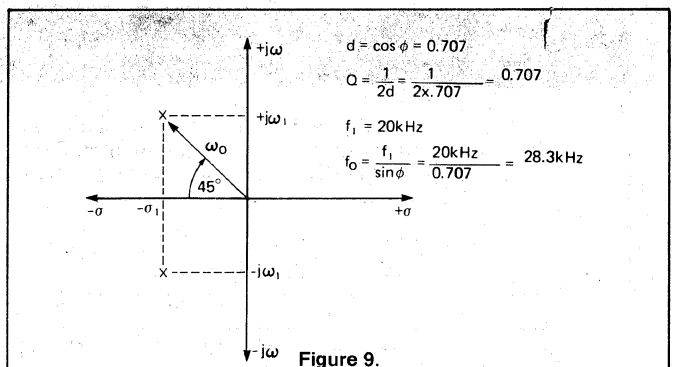


Figure 9.
S-Plane Diagram of Highpass Filter with Critical Damping

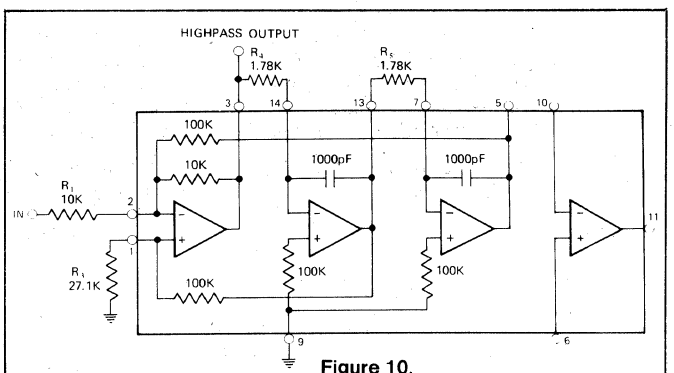


Figure 10.
Highpass Filter Example

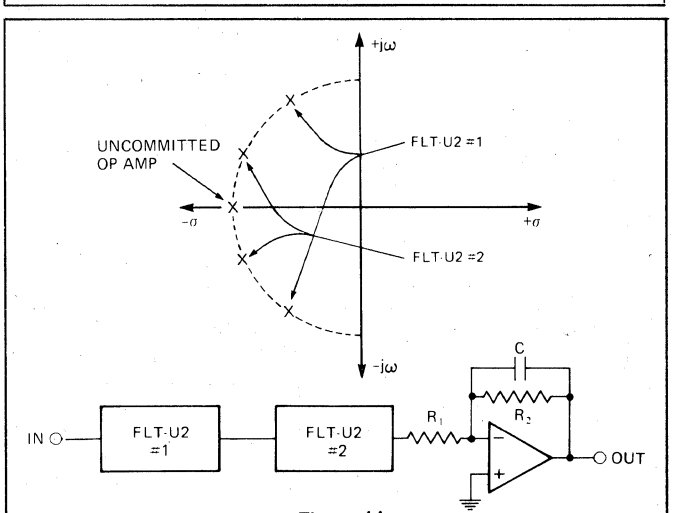


Figure 11.
Realization of a Complex Multipole Filter

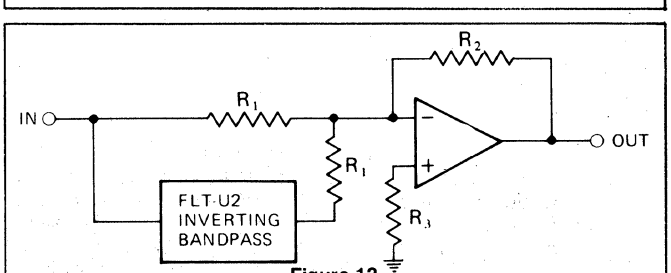


Figure 12.
Realization of Notch Filter

FILTER DESIGN EXAMPLES, (Cont'd)

In this case, however, we choose an inverting uncommitted op amp with a gain of 10 and therefore we use the inverting configuration for the filter. By comparing the second order portion of the Butterworth function $S^2 + \omega_0 S + \omega_0^2$ to the standard second order function $S^2 + \frac{\omega_0}{Q} S + \omega_0^2$ we find $Q = 1$. $f_0 Q$ is then 5×10^3 so that Q will not exceed its specified value.

2. From Table II, using Q = 1, we find:

$$R_1 = 100K \text{ ohms}$$
$$R_2 = \text{open}$$
$$R_3 = \frac{100K}{3.80Q-1} = 35.7K \text{ ohms}$$

3. Using f_0 of 5 kHz, R_4 and R_5 are found from the equation:

$$R_4 = R_5 = \frac{5.03 \times 10^7}{5000} = 10.1K \text{ ohms}$$

4. For the uncommitted output amplifier, a gain of −10 is required. This defines $R_7/R_6 = 10$ and we arbitrarily choose $R_6 = 2K$, $R_7 = 20$ K ohms.

5. The final step is to realize the real axis pole of the Butterworth filter. This pole is at 5 kHz and is set by using capacitor C_3 across the feedback resistor R_7:

$$C_3 = \frac{1}{2\pi f R_7} = \frac{1}{6.28 \times 5 \times 10^3 \times 20 \times 10^3} = 1590 \text{ pF}$$

6. This completes the 3-pole Butterworth filter which is shown in Figure 8.

Highpass Filter with Gain of −1, 20 kHz Cutoff Frequency, and Critical Damping

1. From Table I the inverting configuration must be used to realize a highpass gain of −1. An s-plane diagram of this function is shown in Figure 9. Critical damping requires the pole positions to be on a line 45° with respect to the real axis and this results in no frequency peaking. The damping factor d is:

$$d = \cos\phi = \cos 45^\circ = 0.707$$

and

$$Q = \frac{1}{2d} = \frac{1}{2(.707)} = 0.707$$

Because this is a low Q system the natural frequency will not be the same as the highpass cutoff frequency f_1. From Figure 9:

$$f_0 = \frac{f_1}{\cos\phi} = \frac{20 \text{ kHz}}{0.707} = 28.3 \text{ kHz}$$

Then $f_0 Q = 0.707 \times 28.3 \times 10^3 = 2 \times 10^4$ and the Q will exceed its desired value by slightly over 1%.

2. From Table II, using Q = 0.707 we find:

$$R_1 = 10K \text{ ohms}$$
$$R_2 = \text{open}$$
$$R_3 = \frac{100K}{6.64Q-1} = \frac{100K}{3.69} = 27.1K \text{ ohms}$$

3. Using $f_0 = 28.3$ kHz, R_4 and R_5 are found from the equation:

$$R_4 = R_5 = \frac{5.03 \times 10^7}{28.3 \times 10^3} = 1.78K \text{ ohms}$$

4. This completes the highpass filter design which is shown in Figure 10. When using this filter, care should be exercised so that clipping does not occur in the filter due to excessive input levels. If clipping occurs, the filter will not operate properly. Clipping will first occur at the lowpass output around f_0 since its gain is 20 dB higher than the highpass output. The signal level should be reduced so that clipping does not occur anywhere in the frequency range used. If higher signal level is required, the highpass output should be amplified by a gain stage using the uncommitted op amp.

ADVANCED FILTERS

All of the common filter types can be realized by using cascaded FLT-U2 stages. This includes multi-pole Butterworth, Bessel, Chebyshev, and Elliptic types. The basic procedure is to implement each pole pair with a single FLT-U2 and cascade enough units to realize all poles. A real axis pole is implemented by an uncommitted op amp. stage. Each stage should be separately tuned with an oscillator and scope and then the stages connected together and checked. See Figure 11.

A notch filter can be constructed in several ways. The first way is to use the FLT-U2 as an inverting bandpass filter and sum the output of the filter with the input signal by means of the uncommitted op amp. This produces a net subtraction at the center frequency of the bandpass which produces a null at the output of the amplifier. (See Figure 12.) Likewise lowpass and highpass outputs (which are always in phase) can be subtracted from each other with an external op amp. The highpass output must have some gain added to it, however, so that its gain is equal to that of the lowpass output. A third method is to use two separate FLT-U2's, one as a two-pole lowpass filter and the other as a two-pole highpass filter. Again the outputs are subtracted in an op amp. This method permits independent tuning of the two sections to get the best null response.

Further discussion of filter designs is beyond the scope of this data sheet and the user is referred to the various texts on filter design, some of which are listed below.

Estep, G.J., *The State Variable Active Filter Configuration Handbook*, 2nd Edition, Agoura, Ca., 1974.

Reference Data for Radio Engineers, Howard W. Sams & Co. Inc., 5th Edition.

Christian, E., and Eisenmann, E., *Filter Design Tables and Graphs*. McGraw-Hill Book Co., 1974.

DATEL INTERSIL

11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617)339-9341 / TWX 710-346-1953 / TLX 951340
Santa Ana, (714)835-2751, (L.A.) (213)933-7256 • Sunnyvale, CA (408)733-2424 • Gaithersburg, MD (301)840-9490
• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

TT-590
Two-Terminal IC Temperature Transducer

FEATURES

- **Linear current output: 1μA/°K**
- **Wide range: −55°C to +150°C**
- **Two-terminal device: Voltage in/current out**
- **Laser trimmed to ±1°C calibration accuracy (TT-590-L)**
- **Excellent linearity: ±0.5°C over full range (TT-590-L,K)**
- **Wide power supply range: +4V to +30V**
- **Sensor isolation from case**
- **Low cost**

GENERAL DESCRIPTION

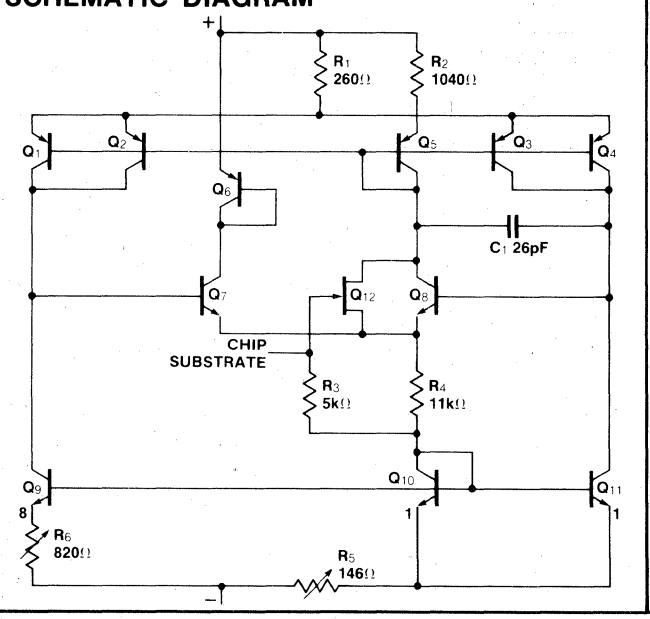
The TT-590 is a two-terminal integrated circuit temperature transducer which produces an output current proportional to absolute temperature. The device acts as a high impedance, constant current regulator passing 1μA/°K for supply voltages between +4V and +30V. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2μA output at 298.2°K (+25°C).

The TT-590 should be used in any temperature sensing application between −55°C and +150°C in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the TT-590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance-measuring circuitry and cold junction compensation are not needed in applying the TT-590. In the simplest application a resistor, a power source and any voltmeter can be used to measure temperature.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, and biasing proportional to absolute temperature.

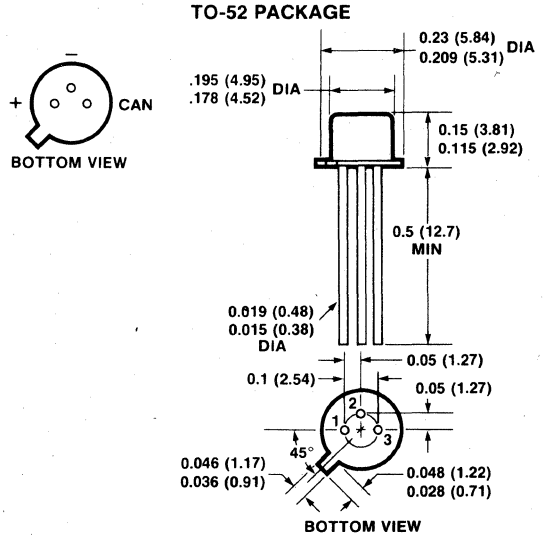
The TT-590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the TT-590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

SCHEMATIC DIAGRAM



OUTLINE DIMENSIONS AND PIN DESIGNATIONS

TO-52 PACKAGE



Dimensions shown in inches and (mm).

ORDERING INFORMATION

ABS. ERROR OVER TEMP.	NON—LINEARITY MAX.	MODEL		ABS. ERROR OVER TEMP.	NON-LINEARITY MAX.	MODEL	
±5.8°C max.	±3.0°C	TT-590-I		±1.6°C max.	±0.4°C	TT-590-L	
±3.0°C max.	±1.5°C	TT-590-J		±1.0°C max.	±0.3°C	TT-590-M	
±2.0°C max.	±0.8°C	TT-590-K					

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

TT-590

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

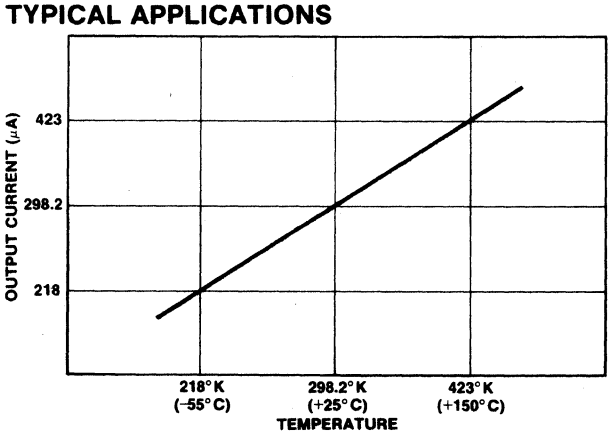
Forward Voltage (V^+ to V^-)	+44V
Reverse Voltage (V^+ to V^-)	−20V
Breakdown Voltage (Case to V^+ or V^-)	±200V
Rated Performance Temperature Range	−55°C to +150°C
Storage Temperature Range	−65°C to +275°C
Lead Temperature (Soldering, 10 sec)	+300°C

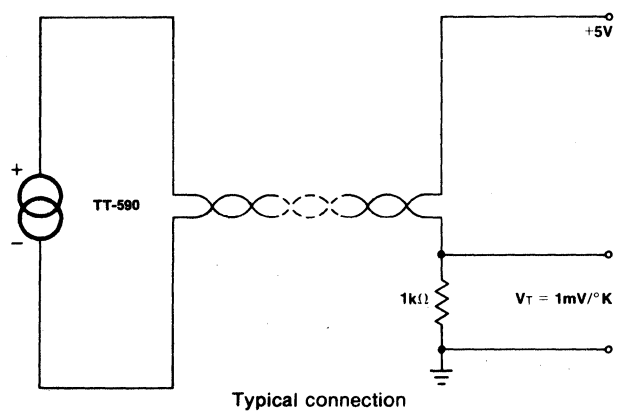
SPECIFICATIONS (Typical values at T_A = +25°C, V_S = 5V unless otherwise noted)

CHARACTERISTICS	TT-590-I	TT-590-J	TT-590-K	TT-590-L	TT-590-M	UNITS
Output Nominal Output Current @ +25°C (298.2°K)	298.2	298.2	298.2	298.2	298.2	μA
Nominal Temperature Coefficient	1.0	1.0	1.0	1.0	1.0	μA/°C
Calibration Error @ +25°C (notes)	±10.0max	± 5.0max	± 2.5max	± 1.0max	± 0.5max	°C
Absolute Error (−55 to +150°C) (Note 1) Without external calibration adjustment	±20.0max	±10.0max	± 5.5max	± 3.0max	± 1.7max	°C
With external calibration adjustment	± 5.8max	± 3.0max	± 2.0max	± 1.6max	± 1.0max	°C
Non-Linearity	± 3.0max	± 1.5max	± 0.8max	± 0.4max	± 0.3max	°C
Repeatability (Note 2)	± 0.1max	± 0.1max	± 0.1max	± 0.1max	± 0.1max	°C
Long Term Drift (Note 3)	± 0.1max	± 0.1max	± 0.1max	± 0.1max	± 0.1max	°C
Current Noise	40	40	40	40	40	pA/√Hz
Power Supply Rejection +4 < V_S < +5V	0.5	0.5	0.5	0.5	0.5	μA/V
+5 < V_S < +15V	0.2	0.2	0.2	0.2	0.2	μA/V
+15V < V_S < +30V	0.1	0.1	0.1	0.1	0.1	μA/V
Case Isolation to Either Lead	10^{10}	10^{10}	10^{10}	10^{10}	10^{10}	Ω
Effective Shunt Capacitance	100	100	100	100	100	pF
Electrical Turn-on Time (Note 1)	20	20	20	20	20	μS
Reverse Bias Leakage Current (Note 4)	10	10	10	10	10	pA
Power Supply Range	+4 to +30	+4 to +30	+4 to +30	+4 to +30	+4 to +30	Volts

Notes 1. Does not include self heating effects.
2. Maximum deviation between +25°C reading after temperature cycling between −55°C and +150°C; guaranteed, not tested.
3. Conditions: Constant +5V, constant +125°C; Guaranteed, not tested.
4. Leakage current doubles every +10°C.

TYPICAL APPLICATIONS





Typical connection

DATEL INTERSIL
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Santa Ana, (714)835-2751, (L.A.) (213)933-7256 • Sunnyvale, CA (408)733-2424 • Gaithersburg, MD (301)840-9490
• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

Low Cost Monolithic Voltage to Frequency Converters Models VFQ-1C, VFQ-1R

FEATURES

- **10 kHz to 100 kHz FS**
- **0.01% Typ. Linearity at 10 kHz**
- **25 ppm/°C Gain Tempco**
- **Open Collector Output**
- **Pulse and Square Wave Outputs**
- **Operates as V/F or F/V**

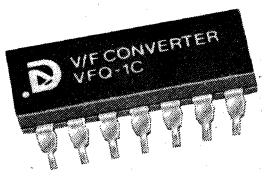
GENERAL DESCRIPTION

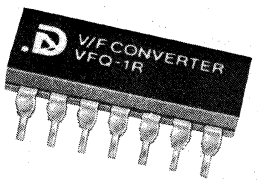
Model VFQ-1 is a new monolithic voltage to frequency converter using combined bipolar and CMOS technologies. This device accepts a positive analog input current and produces an output pulse train with a frequency linearly proportional to an input current. In addition to the pulse output, there is also a square wave output at half the pulse frequency. The full scale output pulse rate can be set from 10 kHz to 100 kHz by means of two external capacitors. Linearities are typically 0.01% for 10 kHz full scale and 0.1% for 100 kHz full scale; linearity holds all the way down to zero.

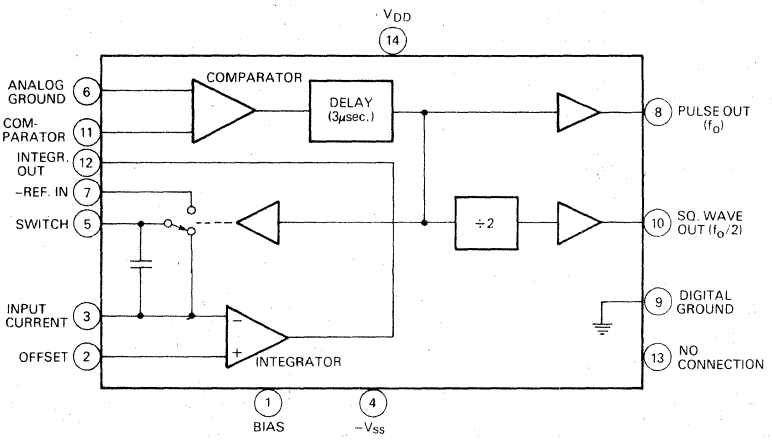
The VFQ-1 internal circuitry includes an operational integrator, a comparator, digital delay circuit, single-pole double-throw electronic switch, a start circuit, a divide by two circuit, and two output driver circuits. It operates on the well-known charge balancing integrator principle. The two outputs are open collector NPN which can sink up to 10 mA and give a logic HI output up to +18 volts.

In normal operation this converter requires only five external components and a reference. If the zeroing adjustment is used, a trimming potentiometer and two more resistors are required. The VFQ-1 can be operated from dual ±4 to ±7.5V supplies or from a single +10V to +15V supply. Current drain is 4 mA max. The device can also be operated as a frequency to voltage converter.

There are two basic packages offered: a 14 pin plastic DIP for 0°C to 70°C operation (VFQ-1C), and a 14 pin ceramic DIP for −25°C to +85°C operation (VFQ-1R).

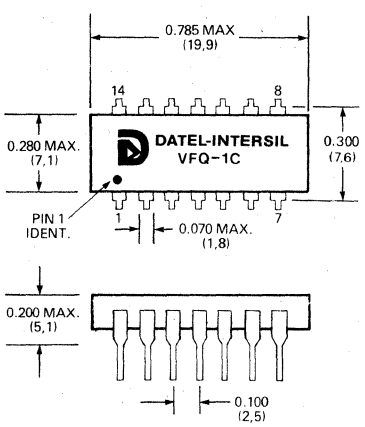




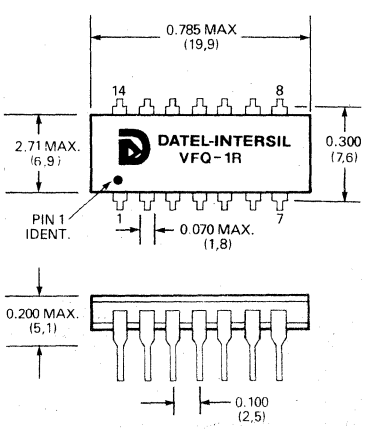


MECHANICAL DIMENSIONS
INCHES (MM)

PLASTIC PACKAGE



CERAMIC PACKAGE



DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, VFQ-1
(Typical at 25°C, ±5V supplies, −5V ref., unless otherwise noted)

	VFQ-1C	VFQ-1R
MAXIMUM RATINGS		
Supply Voltage, pin 4 to pin 14	18 Volts	*
Input Current, pin 3	±10 mA	*
Reference Current, pin 7	±10 mA	*
Output Voltage, pins 8 and 10	+18 Volts	*
Reference (pin 7) to −Vss	±1.5 Volts	*
INPUTS		
Input Current Range	0 to +10 μA	*
Input Current Overrange	+50 μA	*
Input Offset Voltage	±50 mV max.	*
Reference Input	Negative Voltage within ±1.5V of negative supply	
OUTPUTS		
Type Outputs	Open Collector, NPN	
Pulse Output, pin 8	Negative going, 3 μsec pulses at f_0.	
Square Wave Output, pin 10	Square Wave at $f_0/2$	
Output Logic Levels	V_{OUT} ("0") ≤ +0.4V @ −10 mA V_{OUT} ("1") = $+V_{DD}$	
PERFORMANCE		
Linearity, 10 kHz Full Scale	0.01% typ., 0.05% max.	
Linearity, 100 kHz Full Scale	0.1% typ., 0.25% max.	
Gain Tempco, ppm/°C	±25 typ., ±40 max.	
Full Scale Accuracy, before trim	±10%	*
Output Settling Time	2 Pulses of New Frequency	
Power Supply Rejection	0.025%/V	*
SPECIFICATION AS F/V		
Input Frequency Range	0 to 100 kHz	*
Input Voltage, Minimum	±0.4V	*
Input Voltage, Maximum	−2V to $+V_{DD}$	*
Input Impedance	10 Meg., min.	*
Input Pulse Width	0.5 μsec. min. (Negative Pulse) 5.0 μsec. min. (Positive Pulse)	
Output Voltage Range	0 V to ($+V_{DD}$-1)	*
Linearity	±0.1%	*
Output Load, Min.	2K	*
POWER REQUIREMENT	+4.0 to +7.5V @ 4 mA max. −4.0 to −7.5V @ 4 mA max.	
PHYSICAL ENVIRONMENTAL		
Operating Temp. Range	0°C to 70°C	−25°C to +85°C
Storage Temp. Range	−65°C to +150°C	−65°C to +150°C
Package, 14 pin	Plastic DIP	Ceramic DIP

*Same Specification as First Column

TECHNICAL NOTES

1. To calibrate the VFQ-1 as a V/F converter, connect as shown in the diagrams. Connect a precision voltage source (such as Datel-Intersil's DVC-8500) to the input resistor. Connect a 5 digit counter, with time base set to one second, to the output (pin 8).
   Zero. Set the voltage reference to +0.01V and adjust the zero adjust potentiometer for an output frequency of 10 Hz (for 10 kHz FS) or 100 Hz (for 100 kHz FS).
   Gain. Assuming 10V FS input, set the voltage reference to +10.000V and trim the value of R1 to give an output frequency of 10,000 Hz (for 10 kHz FS) or 100,000 Hz (for 100 kHz FS).
2. The two outputs (pins 8 and 10) are open collector NPN transistor for easy interfacing to a variety of standard logic circuits. A pull-up resistor must be used as shown in the diagrams. The resistor may be tied to any voltage up to +18V, which can be separate from $+V_{DD}$.
3. Note that the negative reference voltage must be within ±1.5V of the negative supply ($-V_{SS}$). For a given full scale output frequency the value of C_2 is dependent on the negative reference voltage. See "VFQ-1 Formulas" for the relationship.
4. Note the min-max waveform requirements for the input when using the VFQ-1 as a frequency to voltage converter. See "Input Waveform Limits" diagram. The minimum ±0.4V must be observed as well as the minimum widths for both positive and negative going portions of the waveform. If the input waveform exceeds the maximum amplitude limits, an input resistor and back-to-back clamping diodes should be used as shown in the connection diagram.
5. The temperature to frequency converter shown in the application diagram is a simple but useful method of sensing temperature accurately and transmitting the result in digital form over some distance. Once calibrated at a known temperature the circuit has a resolution of 0.1°C (10 Hz per °K).

ORDERING INFORMATION

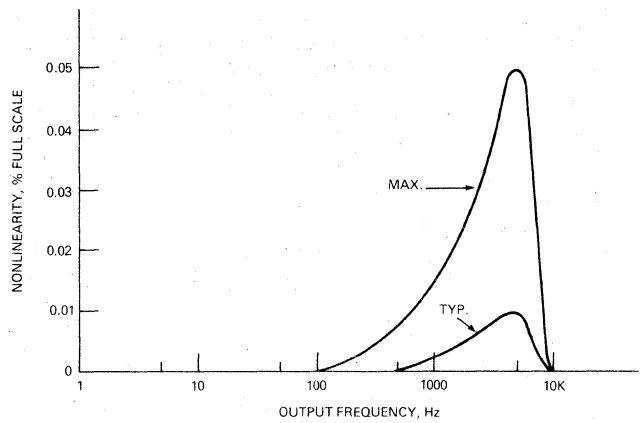
MODEL	TEMP. RANGE	PACKAGE
VFQ-1C	0°C to 70°C	Plastic DIP
VFQ-1R	25°C to +85°C	Ceramic DIP

TRIMMING POTENTIOMETER: TP50K

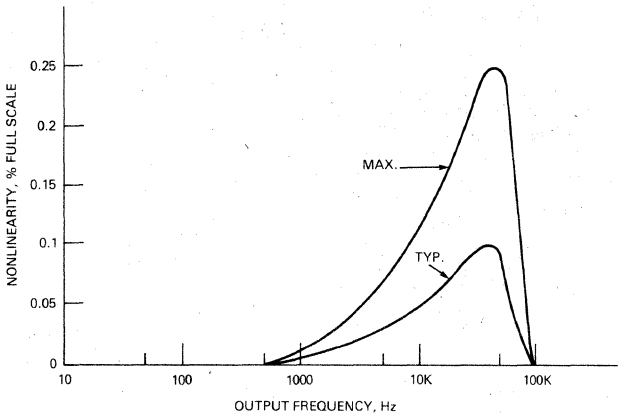
THESE CONVERTERS ARE COVERED BY GSA CONTRACT.

PERFORMANCE CHARACTERISTICS

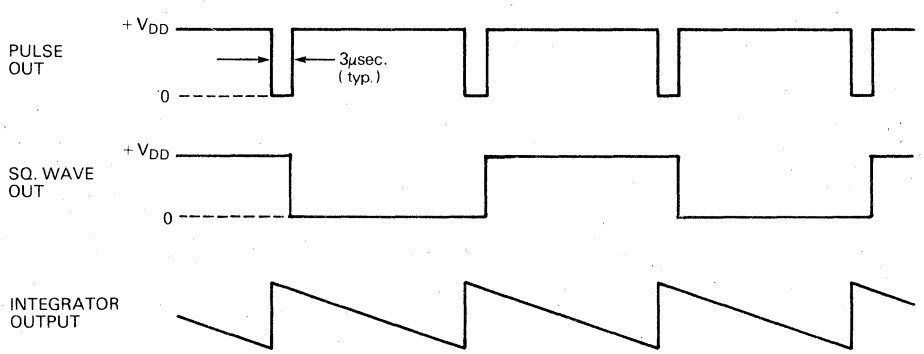
NONLINEARITY—10 kHz FULL SCALE



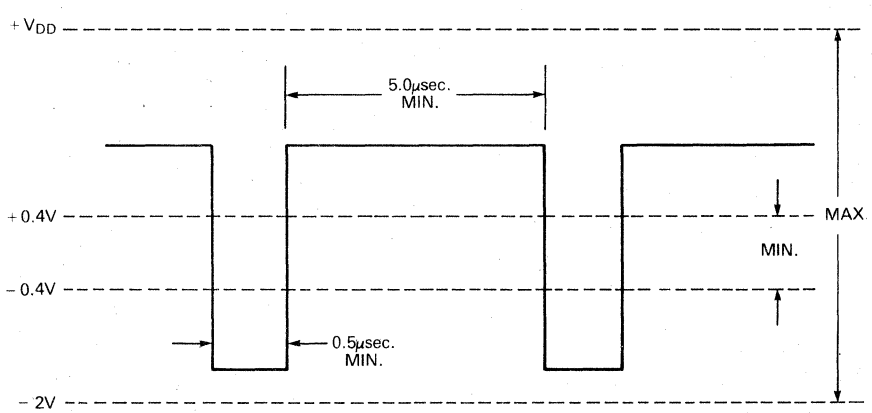
NONLINEARITY—100 kHz FULL SCALE



OUTPUT WAVEFORMS



INPUT WAVEFORM LIMITS (F/V CONVERTER)



VFQ-1 FORMULAS

$$f_{OUT} = \frac{V_{IN}}{R_1} \times \frac{1}{V_{REF}\ C_2}$$

$$R_1 = \frac{V_{IN}\ (max.)}{10\mu A}$$

$82K \leq R_2 \leq 120K$

$3C_2 \leq C_1 \leq 10\ C_2$

C_1 (optimum) $= 4\ C_2$

F/V CONVERTER

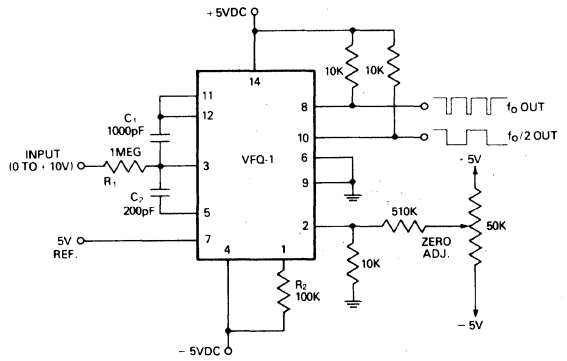
$V_{OUT} = f_{IN} \times V_{REF} \times C_2 \times R_1$

OUTPUT TIME CONSTANT:

$T = R_1\ C_1$

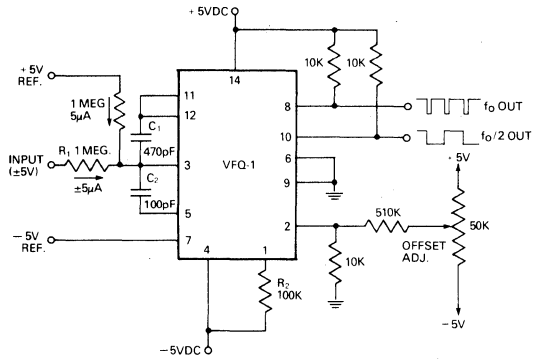
APPLICATIONS DIAGRAMS

NORMAL CONNECTION—10 kHz FULL SCALE

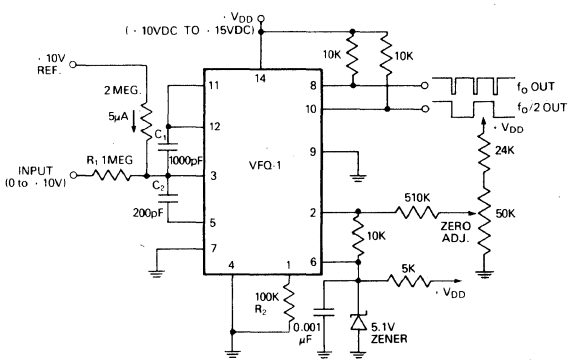


NOTE: FOR 100kHz FULL SCALE, C_1 = 100pF AND C_2 = 20 pF

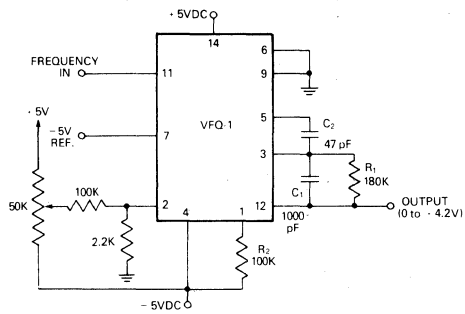
BIPOLAR OPERATION (0 to 20 kHz)



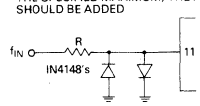
SINGLE SUPPLY OPERATION



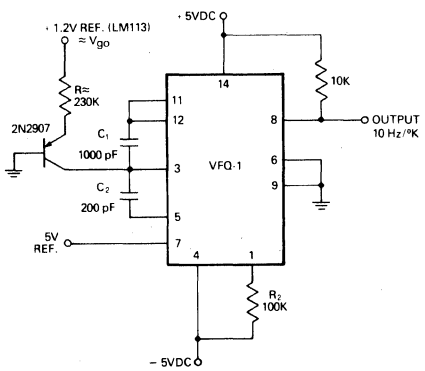
FREQUENCY TO VOLTAGE CONVERTER (0 to 100 kHz INPUT)



NOTE: IF THE AMPLITUDE OF THE INPUT WAVEFORM EXCEEDS THE SPECIFIED MAXIMUM, THE FOLLOWING INPUT CIRCUIT SHOULD BE ADDED



TEMPERATURE TO FREQUENCY CONVERTER



NOTES:

1. V_{go} IS THE EXTRAPOLATED ENERGY-BAND-GAP VOLTAGE FOR SILICON AT 0°K.
2. R IS A STABLE METAL FILM RESISTOR (50 PPM/°C OR BETTER) ITS EXACT VALUE SHOULD BE FOUND BY ADJUSTING IT TO GIVE AN OUTPUT FREQUENCY OF 10 X °K IN HZ FOR A KNOWN TEMPERATURE SUCH AS 300°K. IT WILL THEN BE CORRECTLY CALIBRATED FOR ALL OTHER TEMPERATURES.
3. WHEN PROPERLY IMPLEMENTED THIS CONVERTER IS ACCURATE TO 1°K.

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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
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Universal V-to-F and F-to-V Converter VFV Series

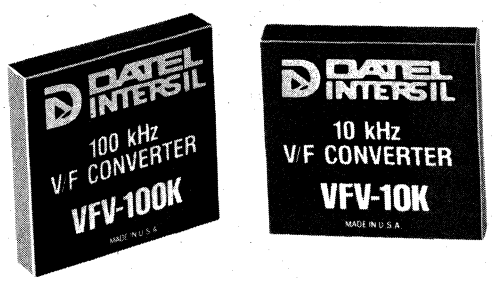
FEATURES

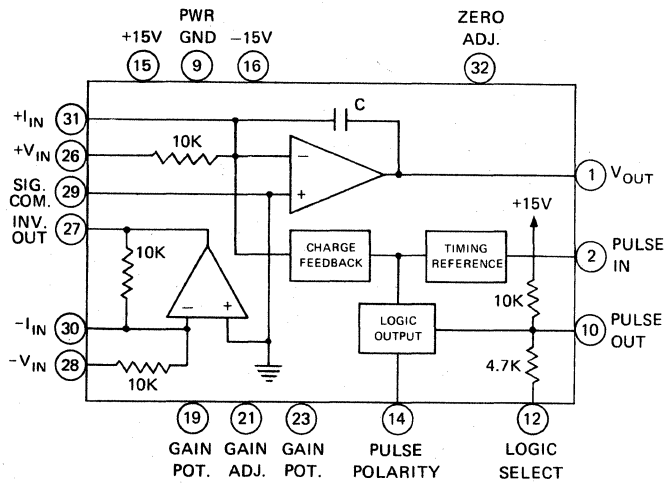
- **Linearity to .005%**
- **V or I Input**
- **V/F or F/V Conversion**
- **10kHz or 100kHz FS**
- **DTL/TTL or CMOS Output**

GENERAL DESCRIPTION

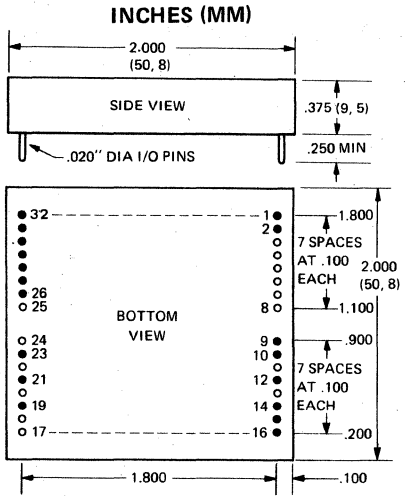
The VFV series voltage to frequency converters, with universal operating characteristics offers significant advantages over other available units. These converters can be operated as either voltage to frequency or frequency to voltage converters by external pin connection. In addition, voltage inputs of 0 to +10V or 0 to -10V and current inputs of 0 to +1mA or 0 to -1mA can be chosen by pin connection. As an F/V converter either 0 to +10V or 0 to -10V outputs can be chosen by pin connection. Output pulses can be selected to be positive or negative going, with DTL/TTL, CMOS, or high level logic interfacing. The output is short circuit proof to common or either supply voltage. The result of these universal pin connectable operating characteristics is wide flexibility in applications.

There are two basic models in this series, the VFV-10K and VFV-100K, with 10kHz and 100kHz full scale output frequencies respectively. Both models have a linear minimum overrange capability of 10%. The linearity holds down to zero input, resulting in an extremely wide dynamic range of operation. The output pulses are constant width pulses of 70 μsec. for the VFV-10K and 7 μsec. for the VFV-100K. Both models are internally trimmed to 1% accuracy with external offset and gain adjustments for precise calibration in a specific application. When used as an F/V converter, an external capacitor can be used to reduce output ripple to a specified level.





MECHANICAL DIMENSIONS INCHES (MM)



NOTE: OPEN DOTS INDICATE OMITTED PINS. PIN POSITION TOLERANCE IS ±0.005" FROM DATUM, NON-ACCUMULATIVE.
WEIGHT: 1.8 OZ. (51 G)

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	VOLTAGE OUT
2	PULSE IN
3	OMITTED
4	"
5	"
6	"
7	"
8	"
9	POWER & LOGIC GND
10	PULSE OUT
11	OMITTED
12	LOGIC SELECT
13	OMITTED
14	PULSE POLARITY
15	+15 VDC POWER
16	-15 VDC POWER
17	OMITTED
18	"
19	GAIN POTENTIOMETER
20	OMITTED
21	GAIN ADJUST
22	OMITTED
23	GAIN POTENTIOMETER
24	OMITTED
25	"
26	+VOLTAGE IN
27	INVERTED OUT
28	-VOLTAGE IN
29	SIGNAL COMMON
30	-CURRENT IN
31	+CURRENT IN
32	ZERO ADJUST

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS

Typical at 25°C, ±15V Supplies unless otherwise noted	VFV-10K	VFV-100K
V/F CONVERTER INPUT		
Input Voltage Range	0 to +10V	*
	0 to −10V	*
Input Current Range	0 to +1mA	*
	0 to −1mA	*
Input Overrange, min.	10%	*
Input Impedance, voltage in	10K ohms	*
V/F CONVERTER OUTPUT		
Frequency Range	0 to 10kHz	0 to 100kHz
Frequency Overrange, min.	10%	*
Pulse Width	70 μsec	7 μsec
Rise and Fall Time, max.	200 nsec.	*
Pulse Polarity	Pos. or Neg.	*
Settling Time to .01%	1 pulse of new freq.	*
Overload Recovery	1 pulse of new freq.	*
Capacitive Loading, max.	1000pF	100pF
Output Logic (Output Code: 1 = Min. +2.4V, Max. +15V; 0 = Min. 0V, Max. +0.4V)	DTL/TTL or CMOS	*
Output Loading, S.C. protected	12 TTL loads	*
ACCURACY		
Full Scale Error, pretrimmed, max. (adj. to zero)	±1%	*
Nonlinearity, max.	±.005%	±.05%
Offset Voltage, max. (adj. to zero)	±10mV	*
Temp. Coefficient of Gain max.	±20ppm/°C	±100ppm/°C
Gain vs. time	±100ppm/day	*
Temp. Coefficient of Zero, max.	±30μV/°C	*
Zero Drift vs. Time	±10μV/day	*
Power Supply Sensitivity, max.	.002%/%	.02%/%
Warm Up Time to Rated Accuracy	1 minute	5 minutes
F/V CONVERTER SPECIFICATIONS		
Input Pulses (Input Code: 1 = Min. 0V, Max. +0.8V; 0 = Min. +2.0V, Max. +15V)	Negative Going	*
	<1TTL Load	*
Input Impedance, min.	30K ohms	4K ohms
Input Pulse Width	10 − 60 μsec.	1 − 6 μsec.
Filter Time Constant	0.5 msec.	.025 msec.
Output Voltage	0 to +10V	*
	0 to −10V	*
Output Impedance	0.1 ohm	*
Output Current, S.C. protected	±5mA	*
POWER REQUIREMENT	±15VDC@25mA quiescent	*
PHYSICAL-ENVIRONMENTAL		
Operating Temperature Range	0°C to 70°C	*
Storage Temperature Range	−55°C to +85°C	*
Relative Humidity	Up to 100% non. cond.	*
Case Size	2" x 2" x .375"	*
Case Material	Black Diallyl Phthalate, Epoxy Encapsulated	*
Pins	0.020" dia. round, gold plated, .250" min.	*
Weight	1.8 oz. (51 g.)	*
Mating Sockets	DILS-2, 2 ea.	*

*Specifications same as VFV-10K

TECHNICAL NOTES

V/F CONVERTER OPERATION

The V/F converter can be thought of as an A/D converter with serial output pulses which must be counted. The first applications diagram shows the V/F converter used as A/D converter by connecting the output to a digital counter and register. The digital counter is shown with a one second counting time base and an output register to store the output data while the V/F converter is making a conversion. The VFV-10K has a resolution of 1 part in 10,000 using a 1 second time base. This is equivalent to better than 13 bits binary resolution (1 part in 8,192). The nonlinearity of this model is 50 ppm maximum which is equivalent (50 ppm = 1/2 LSB) to a better than 13 bit binary converter. With a gain temperature stability of 20 ppm/°C worst case, the VFV-10K is equivalent to a very high quality A/D converter in its performance.

The VFV-100K has a resolution of 1 part in 100,000 using a 1 second time base. This is equivalent to better than 16 bits binary resolution (1 part in 65,536). The VFV-100K can be used to give equivalent resolution to the VFV-10K with only one tenth the time base, or 0.1 second for a resolution of 1 part in 10,000.

An important characteristic of both the VFV-10K and VFV-100K is that their linearity does not fall off near zero as with some other converters. They are both linear right to zero, and this results in a wide dynamic operating range. In practice the lower limit of operation is about 1 millivolt input due to adjustment accuracy, long term stability, temperature drift, etc. This results in a dynamic range of 10,000 to 1 or 80dB for both models.

As a V/F converter positive inputs are achieved using inputs directly into the integrator (pins 26 or 31). For negative inputs the internal inverting amplifier is connected ahead of the integrator and the input is applied to pin 28 or 30. Using both the inverting amplifier inputs and the integrator inputs it is possible to algebraically add and subtract inputs for V/F converter operation.

The output logic level can be set from 0 to +15V by use of an external resistor connected to pin 10 while pin 12 is left open. The output voltage is determined by the resistor ratio with the internal 10K ohm resistor as shown in the Output Logic Connections diagram.

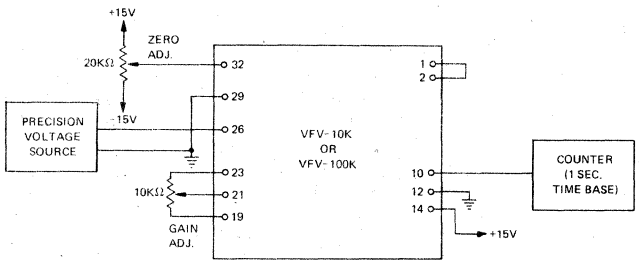
F/V CONVERTER OPERATION

For operation as an F/V converter negative going input pulses must be used. The pulses must go from a HI logic level of +2.0V to +15V to a LO logic level of 0 to +0.8V. The pulse widths must be between 10 and 60 μsec for the VFV-10K and 1 and 6 μsec for the VFV-100K. If these pulse widths are not available, then input conditioning circuits must be used as shown in the diagrams of Input Conditioning for F/V Converter.

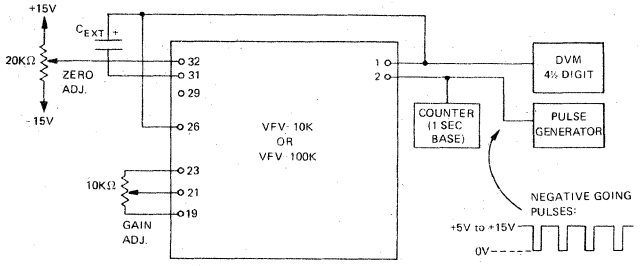
Output ripple of the F/V converter can be made arbitrarily low by using an external filtering capacitor. This also slows down the output response time. As an F/V converter, a positive output is taken directly from the integrator output (pin1). For a negative output voltage the internal inverting amplifier is used after the integrator and the output is taken at pin 27.

CALIBRATION PROCEDURE

AS V/F CONVERTER



AS F/V CONVERTER



Trimming potentiometers are 100ppm/°C, 15 turn type, available from Datel-Intersil

V/F CONVERTER

1. Connect the unit as a V/F converter as shown above with zero and gain trimming potentiometers.
2. Connect a precision dial-up voltage source to +Vin (pin 26) and a digital counter and display set to a 1 second time base to PULSE OUT (pin 10) as shown.
3. Set the precision voltage source to +.010 volt and adjust the zero trimming potentiometer to give an output count of 10 for the VFV-10K or 100 for the VFV-100K.
4. Set the precision voltage source to +10.000 volts and adjust the gain trimming potentiometer to give an output count of 10,000 for the VFV-10K or 100,000 for the VFV-100K.

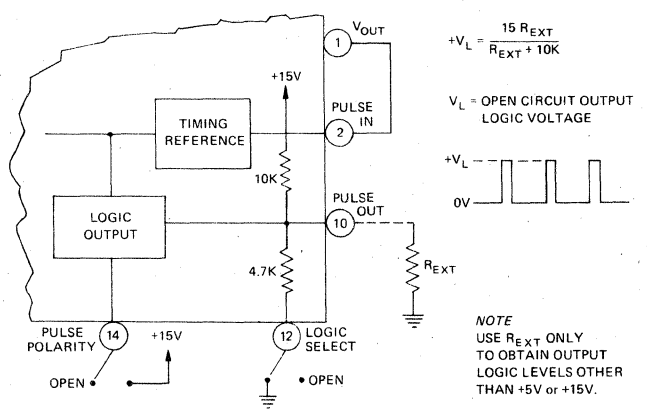
   The above procedure applies for a positive input voltage V/F converter. For a negative input voltage, connect pin 27 to pin 26 and use pin 28 as the input.

F/V CONVERTER

1. Connect the unit as an F/V converter as shown with desired external filter capacitor and zero and gain trimming potentiometers.
2. Connect a 4-1/2 digit DVM to the Vout terminal (pin 1). Connect the PULSE IN terminal (pin 2) to +15 volt supply, and adjust the zero trimming potentiometer for 0.000 volts output.
3. Connect a pulse generator to PULSE IN (pin 2) and set the generator to give +5 volt negative going pulses 50 μsec wide for the VFV-10K or 5 μsec wide for the VFV-100K. Connect a digital counter to the pulse generator output and set the pulse rate to exactly 10kHz for the VFV-10K or 100kHz for the VFV-100K.
4. Adjust the gain trimming potentiometer to give +10.000 volts output.

   The above procedure applies for a positive output voltage F/V converter. If negative output voltage is desired, connect pin 1 to pin 28 and measure the output at pin 27.

OUTPUT LOGIC CONNECTIONS

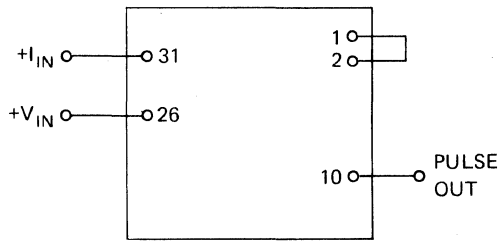


OUTPUT PULSE PROGRAMMING

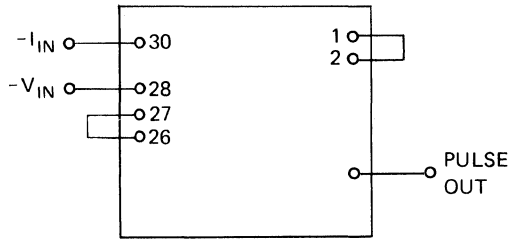
PULSE TYPE	PULSE OUTPUT	LOGIC SELECT (PIN 12)	PULSE POLARITY (PIN 14)
POSITIVE GOING 5V PULSES	+5 / 0	GND	+15V
NEGATIVE GOING 5V PULSES	+5 / 0	GND	OPEN
POSITIVE GOING 15V PULSES	+15 / 0	OPEN	+15V
NEGATIVE GOING 15V PULSES	+15 / 0	OPEN	OPEN

VFV OPERATING MODES

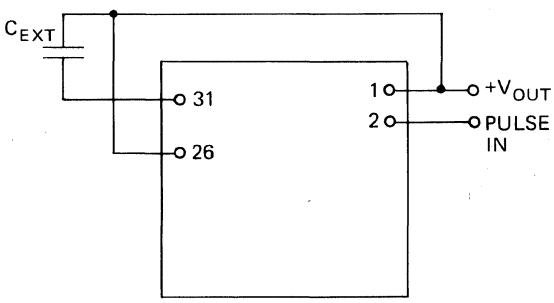
V/F CONVERTER, +V or +I INPUT



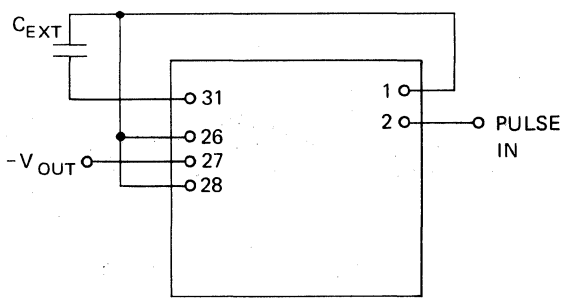
V/F CONVERTER, -V OR -I INPUT



F/V CONVERTER, +V OUT

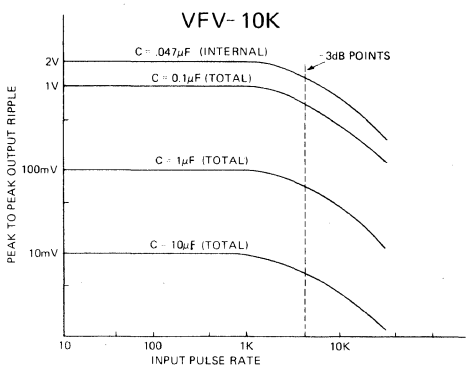


F/V CONVERTER, -V OUT

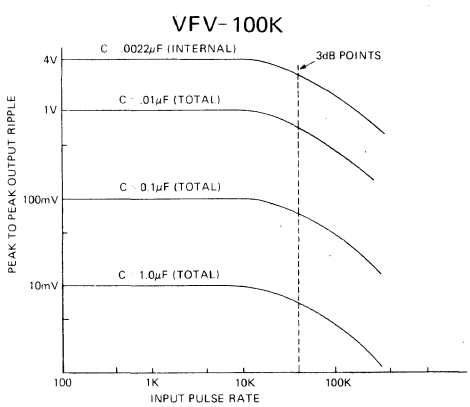


OUTPUT RIPPLE FOR F/V CONVERTER

VFV-10K

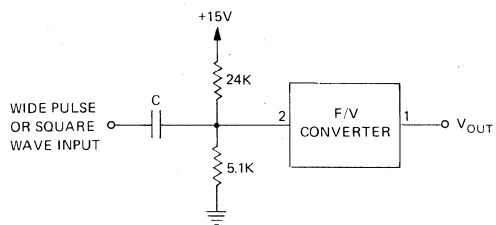


VFV-100K



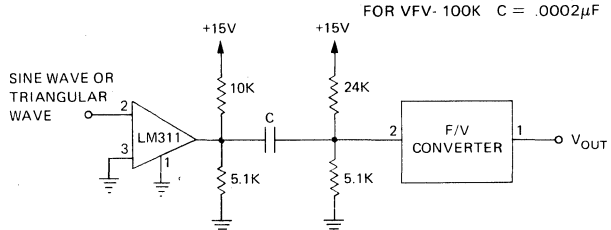
INPUT CONDITIONING FOR F/V CONVERTER

NOTE: FOR VFV-10K C = .002μF
FOR VFV-100K C = .0002μF
ALL RESISTORS SHOWN ARE FOR VFV-10K.
FOR VFV-100K DIVIDE ALL VALUES BY 10.



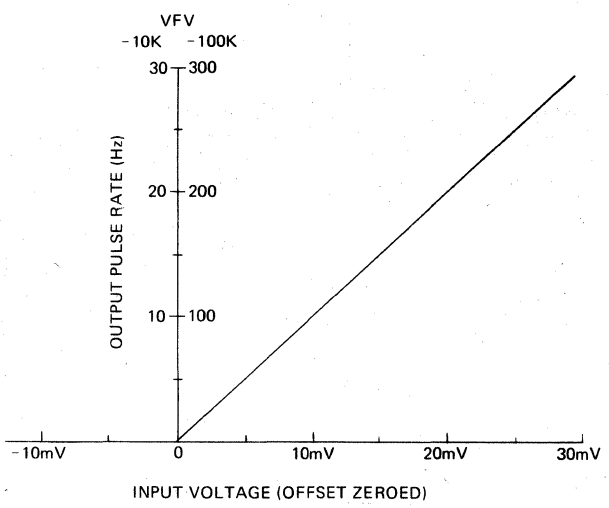
INPUT CONDITIONING CIRCUIT FOR WIDE PULSE OR SQUARE WAVE

NOTE: FOR VFV-10K C = .002μF
FOR VFV-100K C = .0002μF

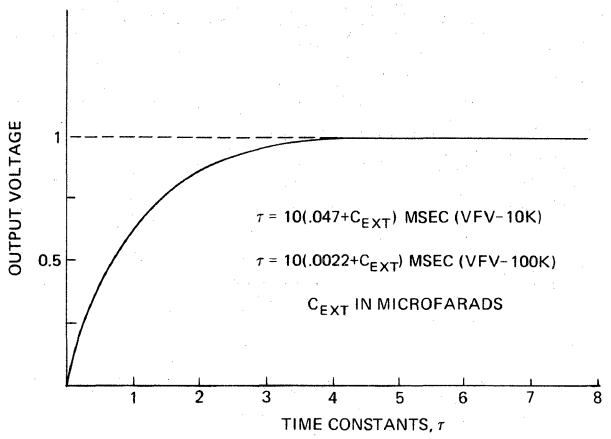


INPUT CONDITIONING CIRCUIT FOR SINE WAVE, TRIANGULAR WAVE, AND OTHER ZERO CROSSING WAVEFORMS

LINEARITY NEAR ZERO INPUT, VFV-10K and VFV-100K

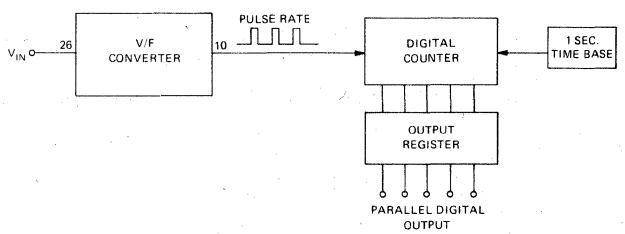


NORMALIZED STEP RESPONSE, F/V CONVERTER

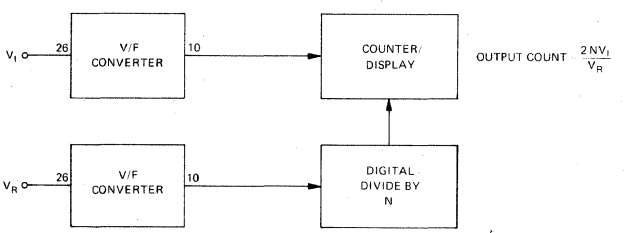


APPLICATIONS

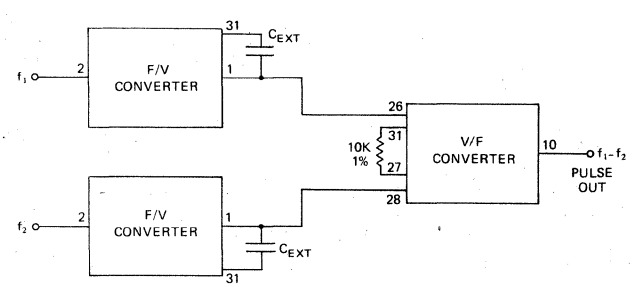
A/D CONVERTER USING V/F CONVERTER



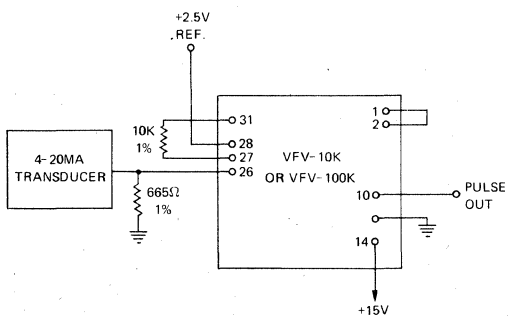
RATIOMETRIC MEASUREMENT



FREQUENCY DIFFERENCE MEASUREMENT

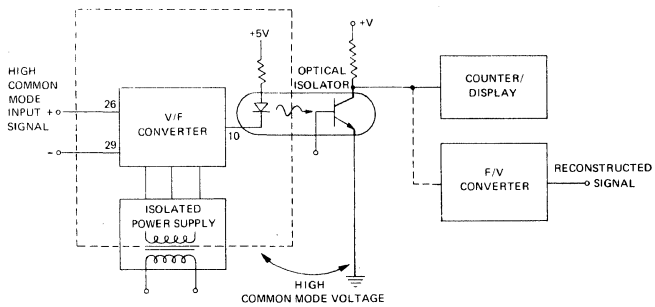


INTERFACING WITH 4 TO 20 MA INDUSTRIAL TRANSDUCER

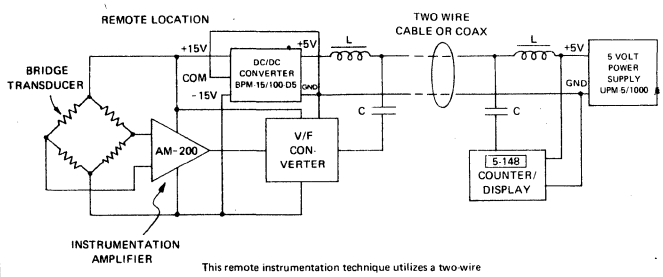


APPLICATIONS (cont'd)

SIGNAL ISOLATION FOR HIGH COMMON MODE VOLTAGE SIGNAL

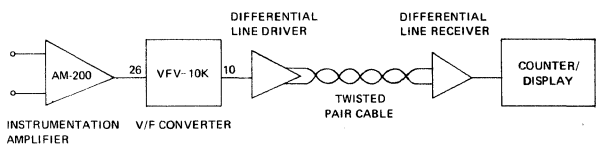


REMOTE INSTRUMENTATION

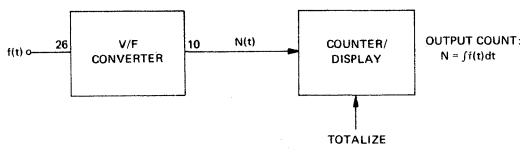


This remote instrumentation technique utilizes a two-wire DC power line for transmitting data back to the counter and display.

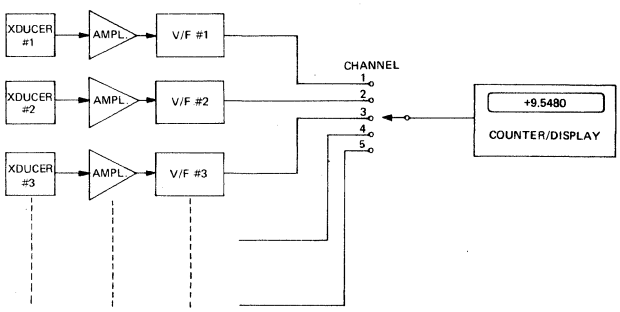
HIGH NOISE IMMUNITY DATA TRANSMISSION



ANALOG SIGNAL INTEGRATION



MULTI-CHANNEL DATA TRANSMISSION AND READOUT



ORDERING INFORMATION

VFV-10K (0 to 10 kHz)

VFV-100K (0 to 100 kHz)

Mating Socket: DILS-2, 2 required

Trimming Potentiometers: TP10K, TP20K,

DATEL INTERSIL
11 CABOT BOULEVARD, MANSFIELD, MA 02048 / TEL. (617)339-9341 / TWX 710-346-1953 / TLX 951340
Santa Ana, (714)835-2751, (L.A.) (213)933-7256 • Sunnyvale, CA (408)733-2424 • Gaithersburg, MD (301)840-9490
• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Monolithic Voltage Converter Model VI-7660

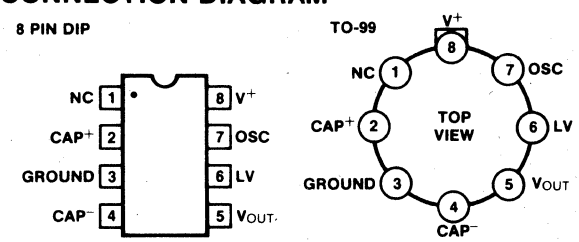
FEATURES

- **Simple Conversion of +5V Logic Supply to ±5V Supplies**
- **Simple Voltage Multiplication (V_{OUT} = (−) nV_{IN})**
- **99.9% Typical Open Circuit Voltage Conversion Efficiency**
- **98% Typical Power Efficiency**
- **Wide Operating Voltage Range 1.5V to 10.0V**
- **Easy to use - Requires only 2 External Non-Critical Passive Components**

APPLICATIONS

- On Board Negative Supply for up to 64 Dynamic RAMs.
- Localized μ-Processor (8080 type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems

CONNECTION DIAGRAM



Note: 1. Pin 1 is designated by dot or notch for DIP.

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
VI-7660C	−20° to +70° C	TO-99
VI-7600PC	−20° to +70° C	8 PIN MINI DIP
VI-7660M	−55° to +125° C	TO-99

GENERAL DESCRIPTION

The VI-7660 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The VI-7660 performs the complete supply voltage conversion from positive to negative for an input range of +1.5V to +10.0V, resulting in complementary output voltages of −1.5 to −10.0V with the addition of only 2 non-critical external capacitors needed for the charge pump and charge reservoir functions. Note that an additional diode is required for V_{SUPPLY} >6.5V.

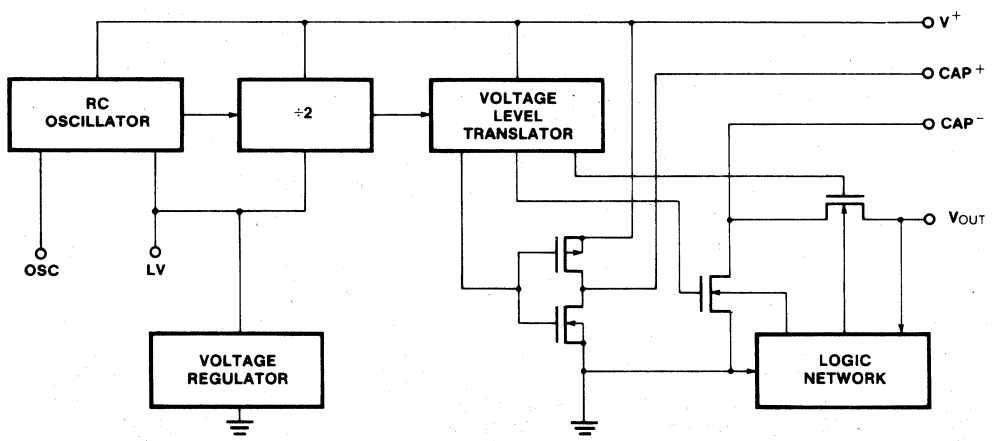
Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, four output power MOS switches, and a unique logic element which senses the most negative voltage in the device and ensures that the output N-channel switches are not forward biased. This assures latch-up free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be over-driven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5 to +10.0 volts), the LV pin is left floating to prevent device latchup.

Typical applications for the VI-7660 will be data acquisition and microprocessor based systems where there is a +5 volt supply available for the digital functions and an additional −5 volt supply is required for the analog functions. The VI-7660 is also ideally suited for providing low current, −5V body bias supply for dynamic RAMs.

BLOCK DIAGRAM



DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

VI-7660

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 10.5V
Oscillator Input Voltage (Note 1) ..... −0.3V to (V^+ +0.3V) for V^+ < 5.5V
(V^+ −5.5V) to (V^+ +0.3V) for V^+ > 5.5V
−0.3V to (V^+ +0.3V) for V^+ < 3.5V
LV (Note 1) ..... No connection for V^+ > 3.5V
Output Short Duration (V_{SUPPLY} ≤5.5V) ..... Continuous
Power Dissipation (Note 2)
VI-7660C 500mW
VI-7660PC 300mW
VI-7660M 500mW

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

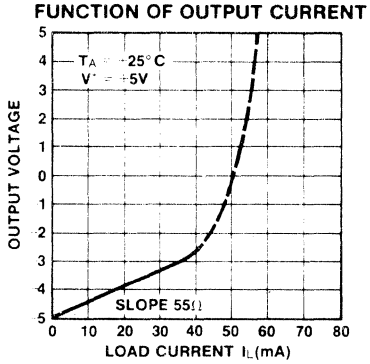
OPERATING CHARACTERISTICS V^+ = 5V, T_A = 25°C, C_{OSC} = 0, Test Circuit Figure 1 (unless otherwise specified)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
I^+	Supply Current		170	500	μA	R_L = ∞
V^+_{H1}	Supply Voltage Range - Hi (Dx out of circuit)	3.0		6.5	V	0°C ≤ T_A ≤ 70°C, R_L = 10kΩ, LV = No Connection
		3.0		5.0	V	−55°C ≤ T_A ≤ 125°C, R_L = 10kΩ, LV = Ground
V^+_{L1}	Supply Voltage Range - Lo (Dx out of circuit)	1.5		3.5	V	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV = Ground
V^+_{H2}	Supply Voltage Range - Hi (Dx in circuit)	3.0		10.0	V	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV = No Connection
V^+_{L2}	Supply Voltage Range - Lo (Dx in circuit)	1.5		3.5	V	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV = Ground
R_{OUT}	Output Source Resistance		55	100	Ω	I_{OUT} = 20mA, T_A = 25°C
				120	Ω	I_{OUT} = 20mA, −20°C ≤ T_A ≤ +70°C
				150	Ω	I_{OUT} = 20mA, −55°C ≤ T_A ≤ +125°C
				300	Ω	V^+ = 2V, I_{OUT} = 3mA, LV = Ground, −20°C ≤ T_A ≤ +70°C
				400	Ω	V^+ = 2V, I_{OUT} = 3mA, LV = Ground, −55°C ≤ T_A ≤ +125°C, Dx in circuit
f_{OSC}	Oscillator Frequency		10		kHz	
P_{Ef}	Power Efficiency	95	98		%	R_L = 5kΩ
$V_{OUT\ Ef}$	Voltage Conversion Efficiency	97	99.9		%	R_L = ∞
Z_{OSC}	Oscillator Impedance		1.0		MΩ	V^+ = 2 Volts
			100		kΩ	V^+ = 5 Volts

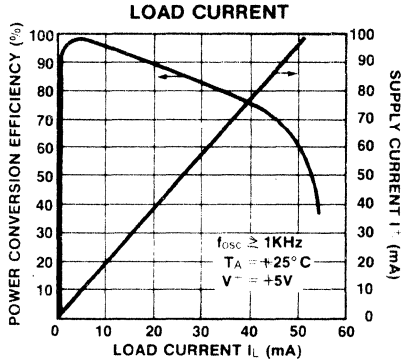
Notes: **1.** Connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the VI-7660.
2. Derate linearly above 50°C by 5.5mW/°C.

TYPICAL PERFORMANCE CHARACTERISTICS

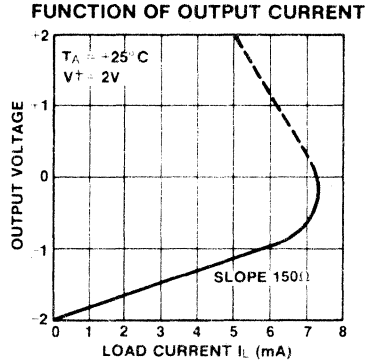
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



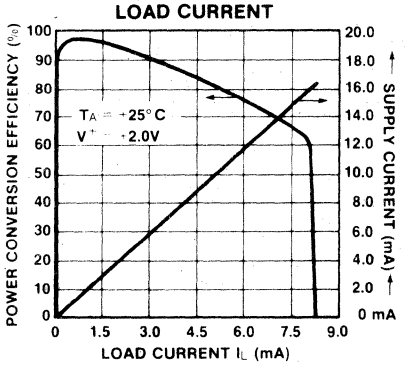
SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



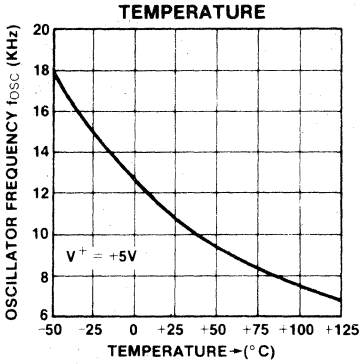
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



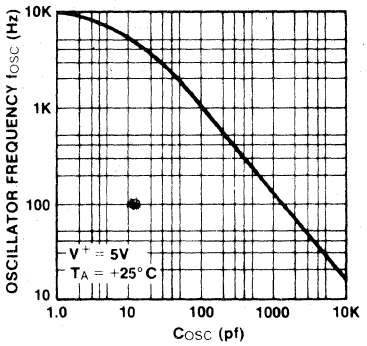
SUPPLY CURRENT POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



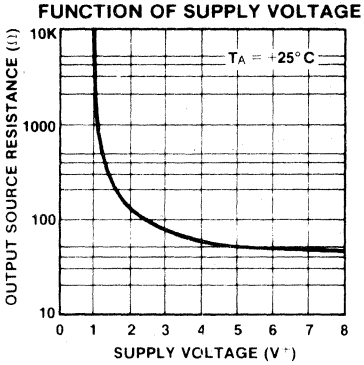
UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE



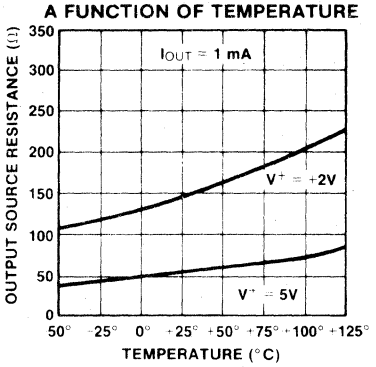
FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE



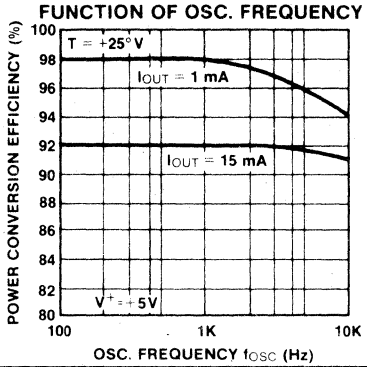
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



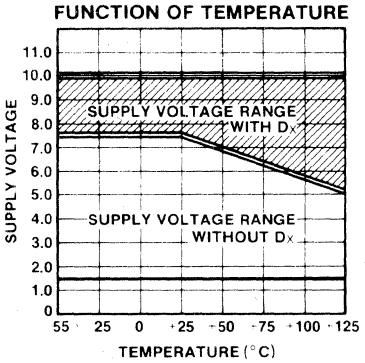
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE

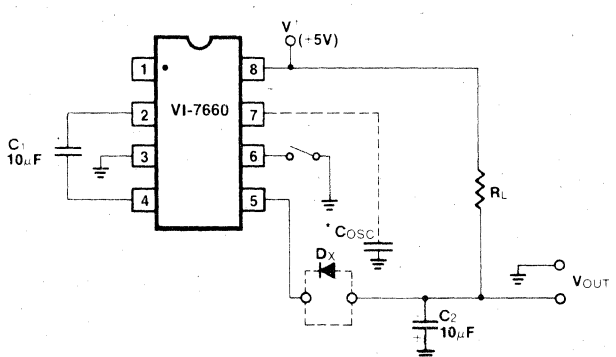


POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY



OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE





NOTES: 1. For large value of C_{OSC} (>1000pF) the values of C_1 and C_2 should be increased to 100μF.

2. D_X is required for supply voltages greater than 6.5V @ −55° ≤ T_A ≤ +70°C; refer to performance curves for additional information.

Figure 1: VI-7660 Test Circuit

CIRCUIT DESCRIPTION

The VI-7660 contains all the necessary circuitry to complete a voltage doubler, with the exception of 2 external capacitors which may be inexpensive 10μF polarized electrolytic capacitors. The mode of operation of the device may be best understood by considering Figure 3, which shows an idealized voltage doubler. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2. The VI-7660 approaches this ideal situation more closely than existing non-mechanical circuits.

In the VI-7660, the 4 switches in Figure 3 are MOS power switches; S_1 is a P-channel device and S_2, S_3 & S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 & S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the VI-7660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators and switches the substrates or S_3 & S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the VI-7660 is an integral part of the anti-latchup circuitry, however it's inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

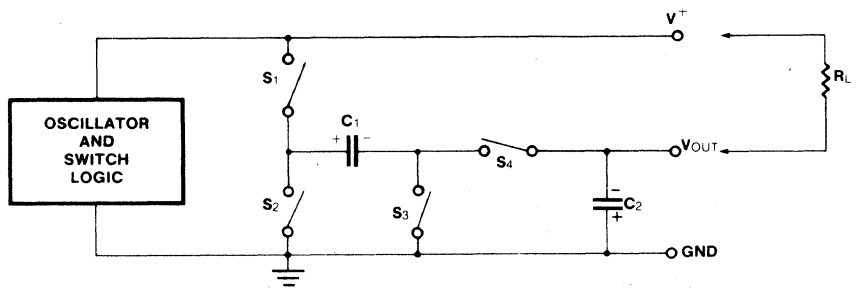


Figure 3: Idealized Voltage Doubler

THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory a voltage multiplier can approach 100% efficiency if certain conditions are met:

A The drive circuitry consumes minimal power
B The output switches have extremely low ON resistance and virtually no offset.
C The impedances of the pump and reservoir capacitors must be negligible at the pump frequency.

The VI-7660 approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$E = 1/2\ C_1\ (V_1^2 - V_2^2)$$

Where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Fig. 3) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

DO'S AND DON'TS

1 Do not exceed maximum supply voltages.
2 Do not connect LV terminal to GROUND for supply voltages greater than 3.5 volts.
3 Do not short circuit the output to V^+ supply for supply voltages above 5.5 volts for extended periods, however, transient conditions including startup are okay.
4 When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the VI-7660 and the + terminal of C_2 must be connected to GROUND.
5 Add diode D_X as shown in Fig. 1 for hi-voltage, elevated temperature applications.

CONSIDERATIONS FOR HI VOLTAGE & ELEVATED TEMPERATURE

The VI-7660 will operate efficiently over its specified temperature range with only 2 external passive components (charge & pump capacitors), provided the operating supply voltage does not exceed 6.5 volts at +70°C and 5.0 volts at +125°C. Exceeding these maximums at the temperatures indicated may result in destructive latch-up of the VI-7660. (Ref: Graph "Operating Voltage Vs. Temperature")

Operation at supply voltages of up to 10.0 volts over the full temperature range without danger of latch-up can be achieved by adding a general purpose diode in series with the VI-7660 output, as shown by "D_X" in the circuit diagrams. The effect of this diode on overall circuit performance is the reduction of output voltage by one diode drop (approximately 0.6 volts).

TYPICAL APPLICATIONS

1. Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the VI-7660 for generation of negative supply voltages. Figure 4 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of +1.5V to +10.0 volts, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5 volts, and that diode D_X must be included for proper operation at higher voltages and/or elevated temperatures.

The output characteristics of the circuit in Figure 4 are those of a nearly ideal voltage source in series with 70 ohms. Thus for a load current of −10mA and a supply voltage of +5 volts, the output voltage will be −4.3 volts. The dynamic output impedance due to the capacitor impedances is $1/\omega C$ where

$$C = C_1 = C_2$$

$$\text{giving} \quad \frac{1}{\omega C} = \frac{1}{2\pi f_{OSC} \times 10^{-5}} = 3 \text{ ohms}$$

for C = 10μF and f_{OSC} = 5kHz (1/2 of oscillator frequency)

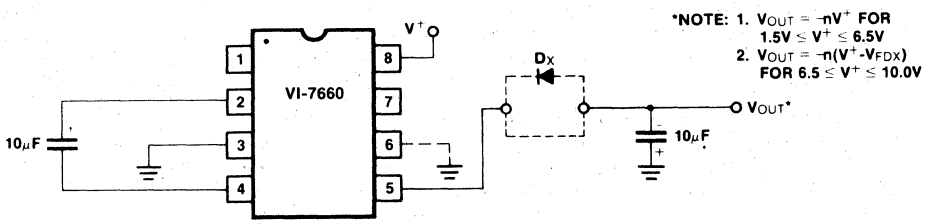


Figure 4: Simple Negative Converter

2. Paralleling Devices

Any number of VI-7660 voltage convertors may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately

$$R_{OUT} = \frac{R_{OUT} \text{ (of VI-7660)}}{\text{n (number of devices)}}$$

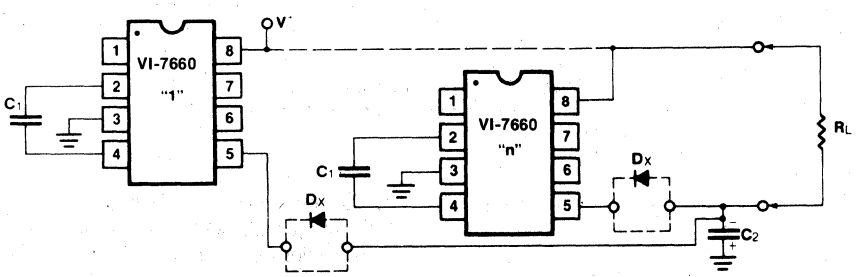


Figure 5: Paralleling Devices

3. Cascading Devices

The VI-7660 may be cascaded as shown to produce larger negative multiplication of the initial supply voltage, however, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\,(V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the sum of the individual VI-7660 R_{OUT}s.

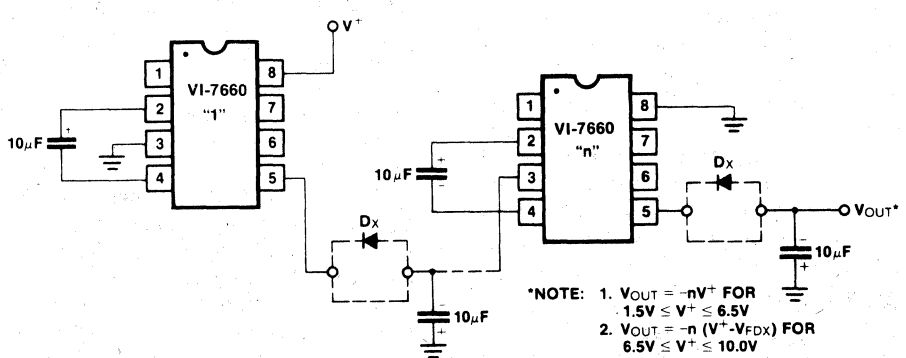


Figure 6: Cascading Devices for Increased Output Voltage

4. Changing the VI-7660 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 7. In order to prevent possible device latchup, a 1kΩ resistor must be used in series with the clock output. In the situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency.

It is also possible to maximize the conversion efficiency of the VI-7660 by lowering the oscillator frequency. This is achieved by connecting an additional capacitor C_{OSC} as shown in Figure 8, however.

Lowering the oscillator frequency will necessitate an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and V^+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from 10μF to 100μF).

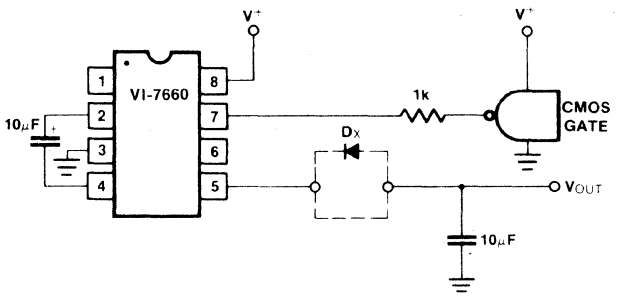


Figure 7: External Clocking

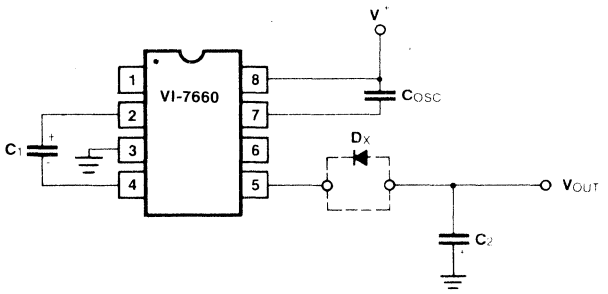


Figure 8: Lowering Oscillator Frequency

5. Positive Voltage Multiplication

The VI-7660 may be employed to achieve positive voltage multiplication using the circuit shown in Figure 9. In this application, the pump inverter switches of the VI-7660 are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2V^+) - (2V_F)$ or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5$ volts and an output current of 10mA it will be approximately 60 ohms.

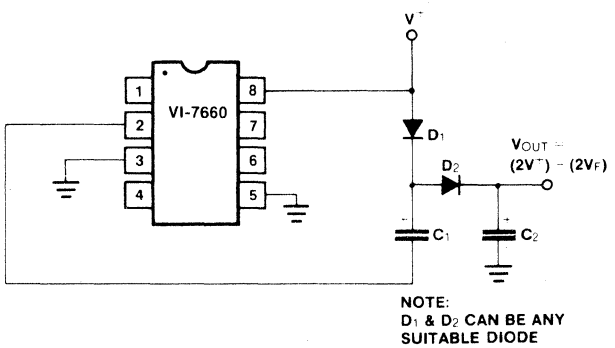


Figure 9: Positive Voltage Multiplier

6. Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 10 combines the functions shown in Figures 4 and 9 to provide negative voltage conversion and positive voltage multiplication simultaneously. This approach would be, for example, suitable for generating +9 volts and −5 volts from an existing +5 volt supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the multiplied positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

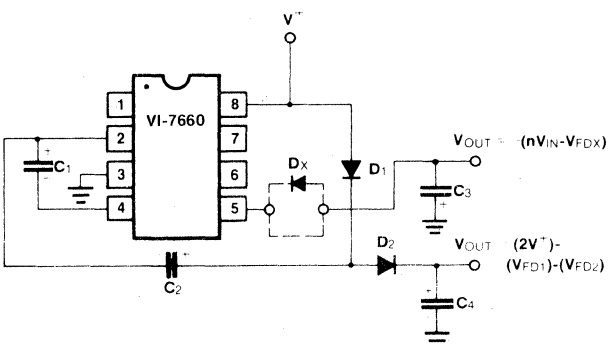


Figure 10: Combined Negative Converter and Positive Multiplier

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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL: ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

Precision Bandgap Voltage References VR-182 Series

FEATURES

- 2.455V Output
- Tempcos to 30 ppm/°C
- 2 to 120 mA Ref. Current
- ±1.4% Tolerance
- 2-Terminal
- Low Cost

GENERAL DESCRIPTION

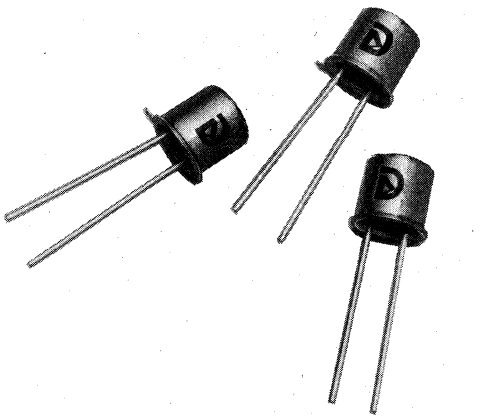
The VR-182 series precision references are two-terminal monolithic bandgap devices which feature 2.455 volts output with tight tolerance and low tempcos. Temperature coefficients are 100, 50, and 30 ppm/°C respectively for Models VR-182A, VR-182B, and VR-182C.

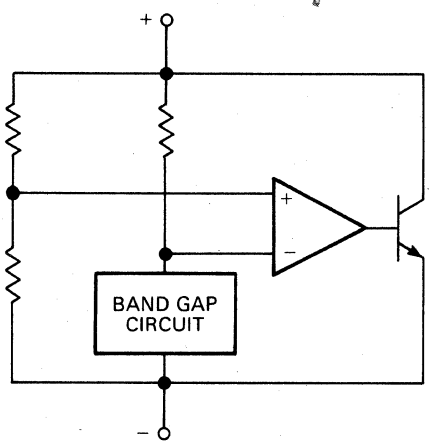
An active regulator around the bandgap circuit results in 0.1 ohm typical dynamic impedance with a wide 2 to 120 mA reference current range. Furthermore, the dynamic impedance is flat to 4 KHz rising to only 1.2 ohms at 50 KHz. Other specifications include ±1.43% voltage tolerance, 10 μV RMS output voltage noise, and 10 ppm per 1000 hours long term stability.

These low cost references are easy to use and are ideal for use with monolithic A/D and D/A converters which do not have internal references. They are also useful in voltage regulator circuits, switching power supplies, comparator circuits, and other analog signal processing applications.

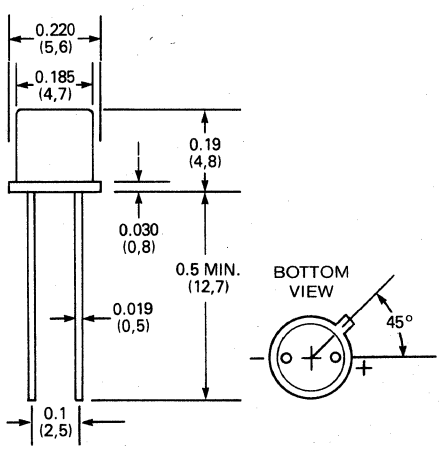
The low 2.455 reference voltage allows these references to be used with 5V logic supplies and other power supply voltages as low as 3.5V. In many cases they give improved performance over higher priced Zener diode references which require higher supply voltages and have much higher dynamic impedances.

The VR-182 devices are supplied in a two-lead hermetically sealed TO-18 package and operate over the 0°C to 70°C temperature range.

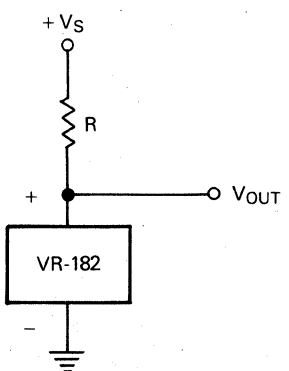




MECHANICAL DIMENSIONS
INCHES (MM)



CONNECTION



DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SPECIFICATIONS, VR-182 SERIES
Typical at 25°C, I_{REF} = 2 mA unless otherwise noted.

MAXIMUM RATINGS
- **Reference Current** . . . . . 120 mA*
- **Dissipation** . . . . . 300 mW

OUTPUT
- **Output Voltage** 2.455V
- **Output Voltage Tolerance, %** . . . . ±1.43%
- **Output Voltage Tolerance, mV** . . . ±35 mV

PERFORMANCE
- **Reference Current Range** . . . . . 2 to 120 mA*
- **Temperature Coefficient, ppm/°C**
  - **VR-182A** . . . . . 60 typ., 100 max.
  - **VR-182B** . . . . . 35 typ., 50 max.
  - **VR-182C** . . . . . 23 typ., 30 max.
- **Dynamic Impedance, DC** . . . . . 0.1 typ., 0.2 ohm max.
- **Dynamic Impedance, 50 KHz** . . . 1.2 ohms
- **Noise Voltage, 1 Hz to 10 Hz** . . . . 10 μV RMS
- **Long Term Stability** . . . . . ±10 ppm/1000 hours

PHYSICAL-ENVIRONMENTAL
- **Operating Temperature Range** . . 0°C to 70°C
- **Storage Temperature Range** . . . . −55°C to +150°C
- **Package Type** 2-lead TO-18

*Derate the 120 mA by 1 mA/°C above 25°C

APPLICATION

VR-182 series voltage references are recommended for use with the following Datel products:

A/D Converters	D/A Converters
ADC-EK Series	DAC-08B
ADC-ET Series	DAC-IC8B
	DAC-IC10B

Application Equation: $R = \frac{V_S - 2.455}{I_L + I_R}$

V_S = Supply Voltage
I_R = Reference Current
I_L = Load Current

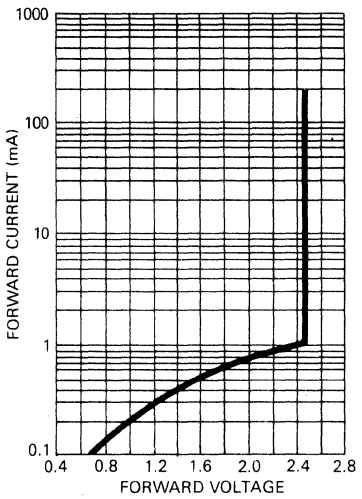
ORDERING INFORMATION

MODEL	TEMPCO/MAX
VR-182A	100 ppm/°C
VR-182B	50 ppm/°C
VR-182C	30 ppm/°C

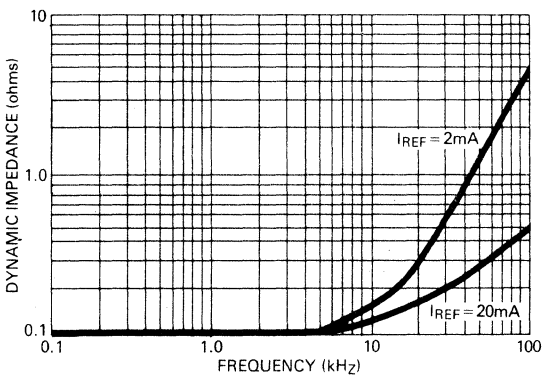
THESE REFERENCES ARE COVERED BY GSA CONTRACT

PERFORMANCE

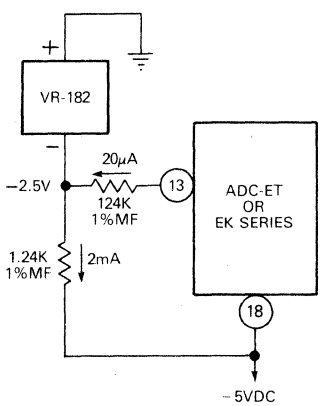
FORWARD CHARACTERISTIC



DYNAMIC IMPEDANCE



CONNECTION TO DATEL ADC-EK OR ADC-ET SERIES AID CONVERTERS



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PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

VR-8069 Series
Low Voltage Reference

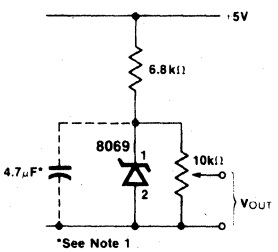
FEATURES

- **Temperature Coefficient guaranteed to 10 ppm/° C max.**
- **Low Bias Current . . . 50μA min**
- **Low Dynamic Impedance**
- **Low Reverse Voltage**
- **Low Cost**

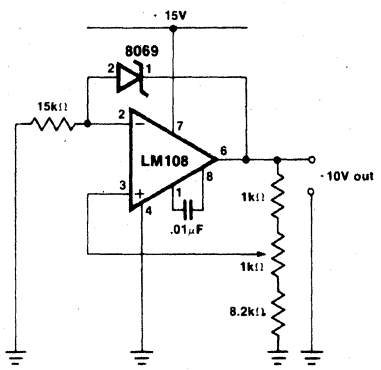
GENERAL DESCRIPTION

The VR-8069 is a 1.2V temperature compensated voltage reference. It uses the band-gap principle to achieve excellent stability and low noise at reverse currents down to 50μA. Applications include analog-to-digital converters, digital-to-analog converters, threshold detectors, and voltage regulators. Its low power consumption makes it especially suitable for battery operated equipment.

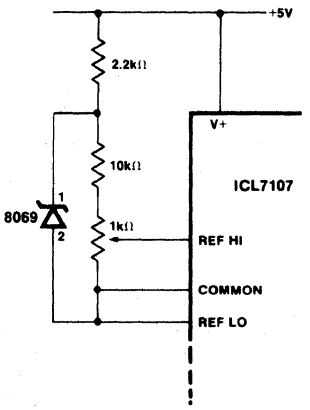
TYPICAL CONNECTION DIAGRAMS



(a) Simple Reference (1.2 volts or less)



(b) Buffered 10V Reference using a single supply.



(c) Double regulated 100mV reference for ICL7107 one-chip DPM circuit.

ORDERING INFORMATION

Model	Tempco. of V_{REF}, Max.	Oper. Temp. Range	Package
VR-8069-DC	1.0%/° C	0 to +70° C	TO-52
VR-8069-DM		−55 to +125° C	
VR-8069-CC	.005%/° C	0 to +70° C	
VR-8069-CM		−55 to +125° C	
VR-8069-BC	.0025%/° C	0 to +70° C	
VR-8069-AC	.001%/° C	0 to +70° C	

VR-8069 SERIES

ABSOLUTE MAXIMUM RATINGS

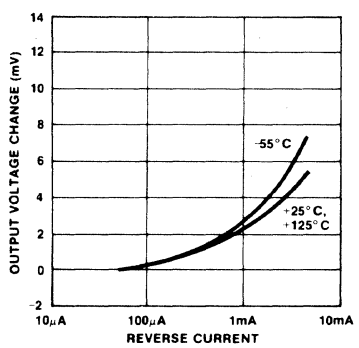
Reverse Voltage ..... See Note 2
Forward Current 10mA
Reverse Current 10mA
Power Dissipation . Limited by max forward/reverse current
Storage Temperature ..... −65° C to +200° C
Operating Temperature
Suffix "C" ..... 0° C to +70° C
Suffix "M" ..... −55° C to +125° C
Lead Temperature (Soldering, 10 Sec) ..... 300° C

ELECTRICAL CHARACTERISTICS (@ 25° C unless otherwise noted)

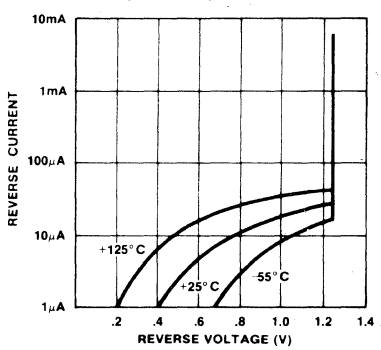
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse breakdown Voltage	I_R = 500μA	1.20	1.23	1.25	V
Reverse breakdown Voltage change	50μA ≤ I_R ≤ 5mA		15	20	mV
Reverse dynamic Impedance	I_R = 50μA I_R = 500μA		1 1	2 2	Ω
Forward Voltage Drop	I_F = 500μA		.7	1	V
RMS Noise Voltage	10Hz ≤ f ≤ 10kHz I_R = 500μA		5		μV
Breakdown voltage Temperature coefficient: 8069A 8069B 8069C 8069D	I_R = 500μA T_A = operating temperature range (Note 3)			 .001 .0025 .005 .01	%/° C
Reverse Current		.050		5	mA

TYPICAL PERFORMANCE CHARACTERISTICS

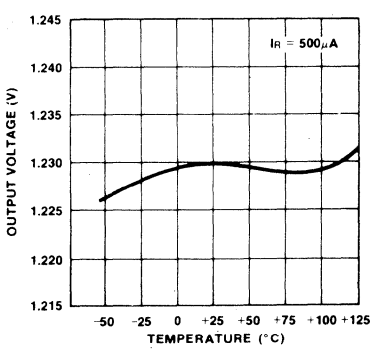
VOLTAGE CHANGE AS A FUNCTION OF REVERSE CURRENT



REVERSE VOLTAGE AS A FUNCTION OF CURRENT



REVERSE VOLTAGE AS A FUNCTION OF TEMPERATURE



Notes:

1) The diode should not be operated with shunt capacitances between 200pF and 0.22μF, as it may oscillate at some currents. If circuit strays in excess of 200pF are anticipated, a 4.7μF shunt capacitor will ensure stability under all operating conditions.
2) In normal use, the reverse voltage cannot exceed the reference voltage. However when plugging units into a powered-up test fixture, an instantaneous voltage equal to the compliance of the test circuit will be seen. This should not exceed 20V.
3) For the military part, measurements are made at 25° C, −55° C, and +125° C. The unit is then classified as a function of the worst case T.C. from 25° C to −55° C, or 25° C to +125° C.

WG-8038 Precision Waveform Generator Voltage Controlled Oscillator

FEATURES

- Low Frequency Drift With Temperature – 50ppm/°C Max.
- Simultaneous Outputs – Sine-Wave, Square-Wave and Triangle.
- High Level Outputs – T^2L to 28V
- Low Distortion – 1%
- High Linearity – 0.1%
- Easy to Use – 50% Reduction in External Components.
- Wide Frequency Range of Operation 0.001Hz to 1.0MHz
- Variable Duty Cycle – 2% to 98%

GENERAL DESCRIPTION

The 8038 Waveform Generator is a monolithic integrated circuit, capable of producing sine, square, triangular, sawtooth and pulse waveform of high accuracy with a minimum of external components (refer to Figures 8 and 9) The frequency (or repetition rate) can be selected externally over a range from less than 1/1000 Hz to more than 1MHz and is highly stable over a wide temperature and supply voltage range. Frequency modulation and sweeping can be accomplished with an external voltage and the frequency can be programmed digitally through the use of either resistors or capacitors. The Waveform Generator utilizes advanced monolithic technology, such as thin film resistors and Schottky-barrier diodes. The 8038 Voltage Controlled Oscillator can be interfaced with phase lock loop circuitry to reduce temperature drift to below 50ppm/°C.

FUNCTIONAL DIAGRAM

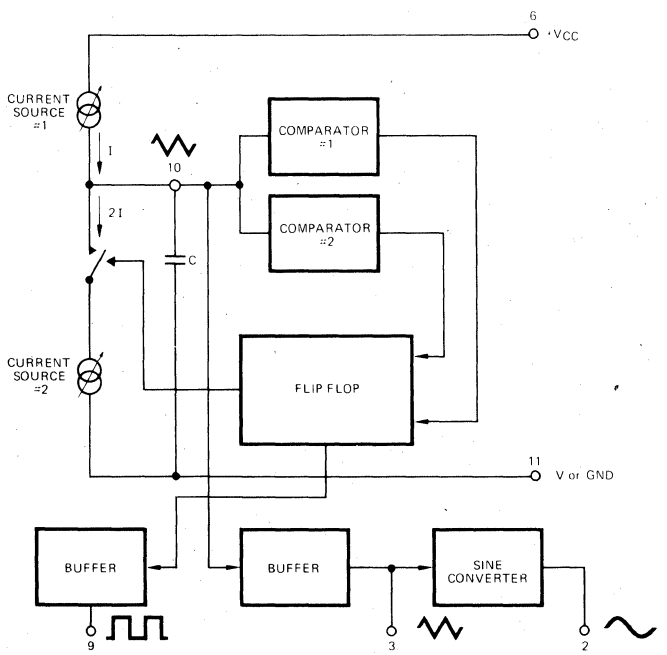
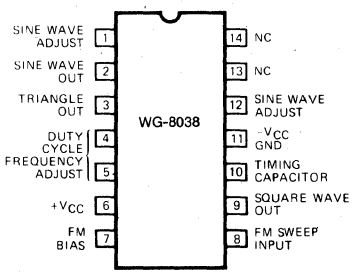


FIGURE 1. BLOCK-DIAGRAM OF WAVEFORM GENERATOR.

CONNECTION DIAGRAM



ORDERING INFORMATION

Model	Stability	Oper. Temp. Range	Package
WG-8038-CC	100 ppm/° C	0 to +70° C	14 pin Cer DIP
WG-8038-BC	50 ppm/° C	0 to +70° C	14 pin Cer DIP
WG-8038-BM	50 ppm/° C	−55 to +125° C	14 pin Cer DIP
WG-8038-AC	20 ppm/° C	0 to +70° C	14 pin Cer DIP
WG-8038-AM	20 ppm/° C	−55 to +125° C	14 pin Cer DIP

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

WG-8038

MAXIMUM RATINGS

Supply Voltage ..... ±18V or 36V Total
Power Dissipation ..... 750mW (Note 5)
Input Voltage (any pin) ..... Not To Exceed Supply Voltages
Input Current (Pins 4 and 5) 25mA
Output Sink Current (Pins 3 and 9) 25mA
Storage Temperature Range ..... −65°C to +125°C
Operating Temperature Range:
  Suffix "M" ..... −55°C to +125°C
  Suffix "C" ..... 0°C to +70°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

ELECTRICAL CHARACTERISTICS

(V_S = ±10V or +20V, T_A = 25°C, R_L = 10 KΩ, Unless Otherwise Specified) Note 3.

GENERAL CHARACTERISTICS	WG-8038-C MIN	WG-8038-C TYP	WG-8038-C MAX	WG-8038-B MIN	WG-8038-B TYP	WG-8038-B MAX	WG-8038-A MIN	WG-8038-A TYP	WG-8038-A MAX	UNITS
Supply Voltage Operating Range										
Single Supply	+10		+30	+10		30	+10		30	V
Dual Supplies	±5		±15	±5		±15	±5		±15	V
Supply Current (V_S = ±10V) Note 1.										
Suffix "M"					12	15		12	15	mA
Suffix "C"		12	20		12	20		12	20	mA
FREQUENCY CHARACTERISTICS (all waveforms)										
Maximum Frequency of Oscillation	100,000			100,000			100,000			Hz
Sweep Frequency of FM		10			10			10		kHz
Sweep FM Range (Note 2)		40:1			40:1			40:1		
FM Linearity 10:1 Ratio		0.5			0.2			0.2		%
Frequency Drift With Temperature Note 6		50			50	100		20	50	ppm/°C
Frequency Drift With Supply Voltage (Over Supply Voltage Range)		0.05			0.05			0.05		%/V_S
Recommended Programming Resistors (R_A and R_B)	1000		1M	1000		1M	1000		1M	Ω
OUTPUT CHARACTERISTICS										
Square-Wave										
Leakage Current (V9 = 30v)			1			1			1	μA
Saturation Voltage (I_{SINK} = 2mA)		0.2	0.5		0.2	0.4		0.2	0.4	V
Rise Time (R_L = 4.7kΩ)		100			100			100		ns
Fall Time (R_L = 4.7kΩ)		40			40			40		ns
Duty Cycle Adjust	2		98	2		98	2		98	%
Triangle/Sawtooth/Ramp										
Amplitude (R_T = 100kΩ)	0.30	0.33		0.30	0.33		0.30	0.33		xV_S
Linearity		0.1			0.05			0.05		%
Output Impedance (I_{OUT} = 5mA)		200			200			200		Ω
Sine-Wave										
Amplitude (R_S = 100kΩ)	0.2	0.22		0.2	0.22		0.2	0.22		xV_S
THD (R_S = 1MΩ) Note 4.		0.8	5		0.7	3		0.7	1.5	%
THD Adjusted (Use Fig. 8b)		0.5			0.5			0.5		%

NOTE 1: R_A and R_B collection currents not included.
NOTE 2: V_S = 20V; R_A and R_B = 10kΩ, f ≅ 9kHz; Can be extended to 1000.1 See Figures 13 and 14
NOTE 3: All parameters measured in test circuit given in Fig. 2
NOTE 4: 82kΩ connected between pins 11 and 12, Triangle Duty Cycle set at 50%. (Use R_A and R_B)
NOTE 5: Derate ceramic package at 12.5mW/°C for ambient temperatures above 100°C
NOTE 6: Over operating temperature range, Fig. 2, pins 7 and 8 connected, V_S = ±10V. See Fig. 6c for T.C. vs V_S

WG-8038

TEST CONDITIONS (See Fig. 2)

PARAMETER	R_A	R_B	R_L	C_1	SW_1	MEASURE
Supply Current	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Current into Pin 6
Maximum Frequency of Oscillation	1kΩ	1kΩ	4.7kΩ	100pf	Closed	Frequency at Pin 9
Sweep FM Range (Note 1)	10kΩ	10kΩ	10kΩ	3.3nF	Open	Frequency at Pin 9
Frequency Drift with Temperature	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 9
Frequency Drift with Supply Voltage (Note 2)	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 9
Output Amplitude: Sine	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk output at Pin 2
Triangle	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk output at Pin 3
Leakage Current (off) Note 3	10kΩ	10kΩ		3.3nF	Closed	Current into Pin 9
Saturation Voltage (on) Note 3	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Output (low) at Pin 9
Rise and Fall Times	10kΩ	10kΩ	4.7kΩ	3.3nF	Closed	Waveform at Pin 9
Duty Cycle Adjust: MAX	50kΩ	~1.6kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
MIN	~25kΩ	50kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
Triangle Waveform Linearity	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 3
Total Harmonic Distortion	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 2

NOTE 1: The hi and lo frequencies can be obtained by connecting pin 8 to pin 7 (f_{hi}) and then connecting pin 8 to pin 6 (f_{lo}). Otherwise apply Sweep Voltage at pin 8 $(2/3\ V_{CC} + 2V) \leq V_{SWEEP} \leq V_{CC}$ where V_{CC} is the total supply voltage. In Fig. 2, Pin 8 should vary between 5.3V and 10V with respect to ground.

NOTE 2: $10V \leq V_{CC} \leq 30V$, or $\pm 5V \leq V_S \leq \pm 15V$.

NOTE 3: Oscillation can be halted by forcing pin 10 to +5 volts or −5 volts.

DEFINITION OF TERMS:

Supply Current — The current required from the power supply to operate the device, excluding load currents and the currents through R_A and R_B.

Frequency Range — The frequency range at the square wave output through which circuit operation is guaranteed.

Sweep FM Range — The ratio of maximum frequency to minimum frequency which can be obtained by applying a sweep voltage to Pin 8. For correct operation, the sweep voltage should be within the range $(2/3\ V_{CC} + 2V) < V_{sweep} < V_{CC}$.

FM linearity — The percentage deviation from the best-fit straight line on the control voltage versus output frequency curve.

Frequency Drift with Temperature — The change in output frequency as a function of temperature.

Frequency Drift with Supply Voltage — The change in output frequency as a function of supply voltage.

Output Amplitude — The peak-to-peak signal amplitude appearing at the outputs.

Saturation Voltage — The output voltage at the collector of Q_{23} when this transistor is turned on. It is measured for a sink current of 2mA.

Rise Time and Fall Time — The time required for the square wave output to change from 10% to 90%, or 90% to 10%, of its final value.

Triangle Waveform Linearity — The percentage deviation from the best-fit straight line on the rising and falling triangle waveform.

Total Harmonic Distortion — The total harmonic distortion at the sine-wave output.

TEST CIRCUIT

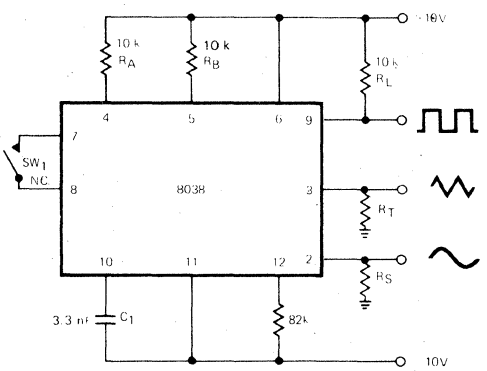


FIGURE 2

WG-8038

CHARACTERISTIC CURVES

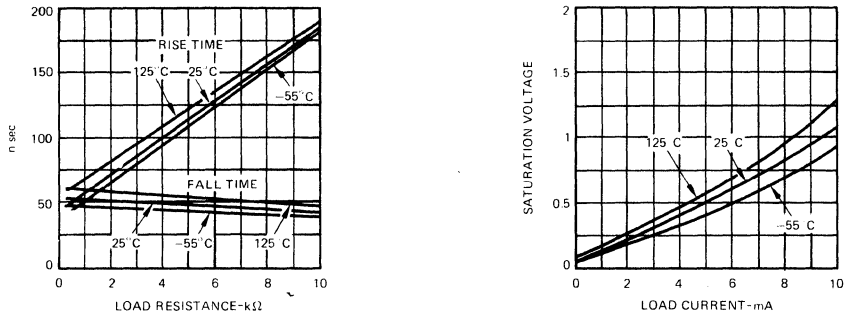


FIGURE 3. PERFORMANCE OF THE SQUARE-WAVE OUTPUT (PIN 9).

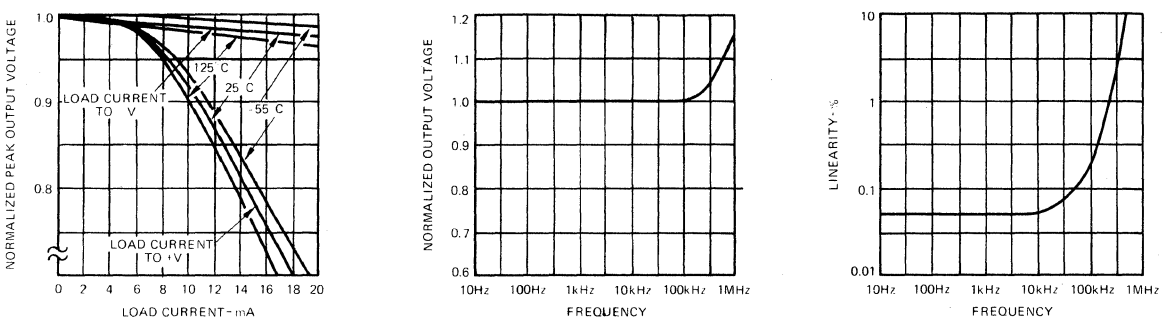


FIGURE 4. PERFORMANCE OF TRIANGLE-WAVE OUTPUT.

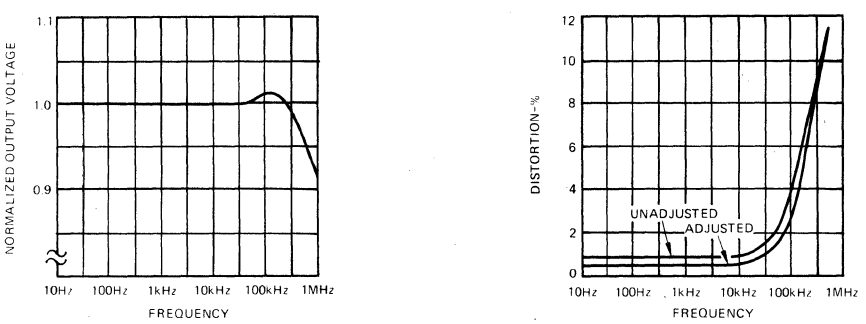


FIGURE 5. PERFORMANCE OF SINE-WAVE OUTPUT.

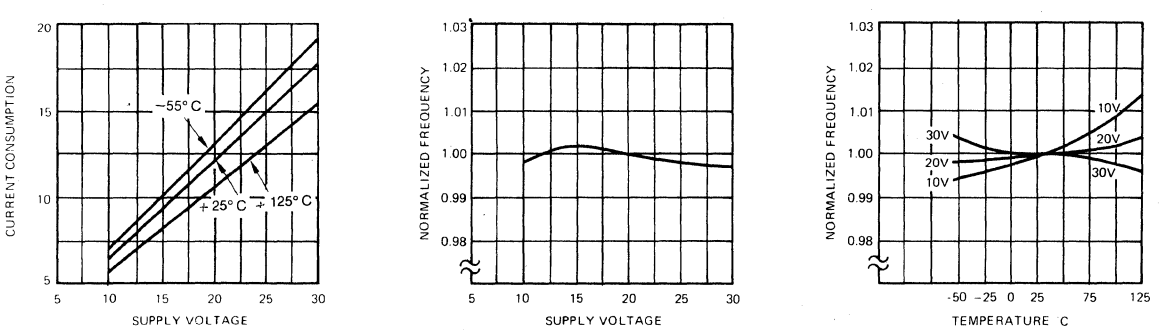


FIGURE 6. CURRENT CONSUMPTION AND FREQUENCY STABILITY.

THEORY OF OPERATION

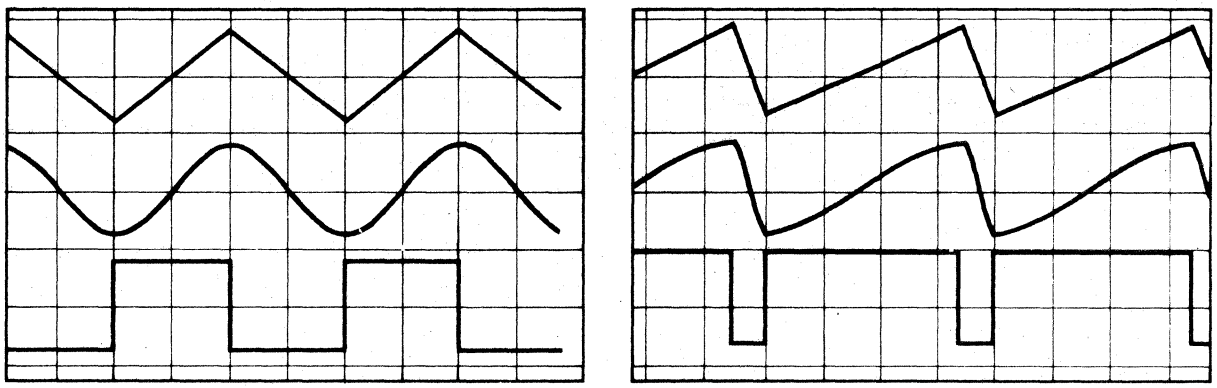


FIGURE 7. PHASE RELATIONSHIP OF WAVEFORMS.

The performance of the sine-wave output is shown in Figure 5. Figure 6 shows additional general information concerning current consumption and frequency stability and Figure 7 shows the phase relationship between the three waveforms.

WAVEFORM TIMING

The *symmetry* of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figure 8. Best results are obtained by keeping the timing resistors R_A and R_B separate (a). R_A controls the rising portion of the triangle and sine-wave and the 1 state of the square-wave.

The magnitude of the triangle-waveform is set at 1/3 V_{CC}; therefore the rising portion of the triangle is,

$$t_1 = \frac{C \times V}{I} = \frac{C \times 1/3 \times V_{CC} \times R_A}{1/5 \times V_{CC}} = \frac{5}{3} R_A \times C$$

The falling portion of the triangle and sine-wave and the 0 state of the square-wave is:

$$t_2 = \frac{C \times V}{I} = \frac{C \times 1/3\, V_{CC}}{\frac{2}{5} \times \frac{V_{CC}}{R_B} - \frac{1}{5} \times \frac{V_{CC}}{R_A}} = \frac{5}{3} \times \frac{R_A R_B C}{2R_A - R_B}$$

Thus a 50% duty cycle is achieved when $R_A = R_B$.

If the duty-cycle is to be varied over a small range about 50% only, the connection shown in Figure 8b is slightly more convenient. If no adjustment of the duty cycle is desired, terminals 4 and 5 can be shorter together, as shown in Figure 8c. This connection, however, carries an inherently larger variation of the duty-cycle.

With two separate timing resistors, the *frequency* is given by

$$f = \frac{1}{t_1 + t_2} = \frac{1}{\frac{5}{3} R_A C \left(1 + \frac{R_B}{2R_A - R_B}\right)}$$

or, if $R_A = R_B = R$

$$f = \frac{0.3}{R C} \qquad \text{(for Figure 8a)}$$

If a single timing resistor is used (Figures 8c only), the frequency is

$$f = \frac{0.15}{R C}$$

Neither time nor frequency are dependent on supply voltage, even though none of the voltages are regulated inside the integrated circuit. This is due to the

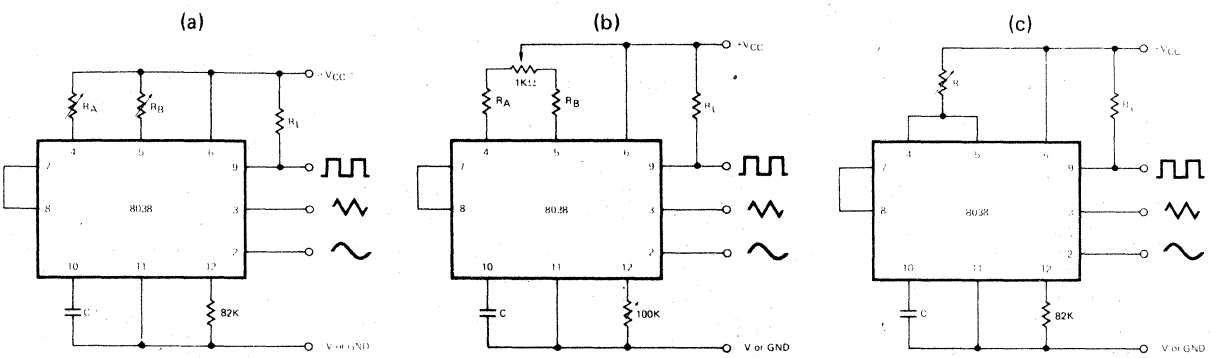


FIGURE 8. POSSIBLE CONNECTIONS FOR THE EXTERNAL TIMING RESISTORS.

fact that both currents *and* thresholds are direct, linear function of the supply voltage and thus their effects cancel.

To minimize *sine-wave* distortion the 82kΩ resistor between pins 11 and 12 is best made a variable one. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 9. This configuration allows a reduction of sine-wave distortion close to 0.5%.

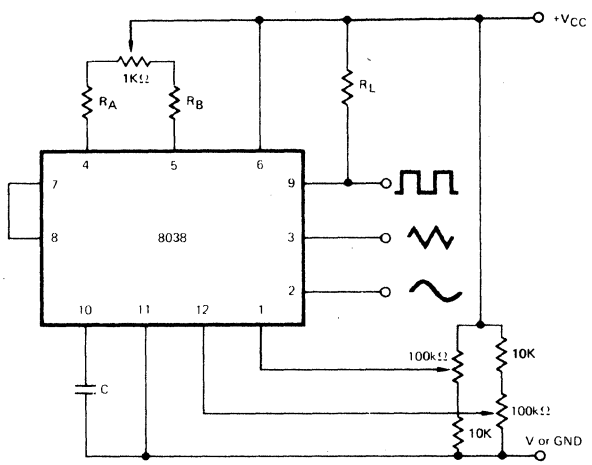


FIGURE 9. CONNECTION TO ACHIEVE MINIMUM SINE-WAVE DISTORTION.

SELECTING R_A, R_B and C

For any given output frequency, there is a wide range of RC combinations that will work. However certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 1μA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents ($I > 5$ mA), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will be obtained for charging currents of 10μA to 1 mA. If pins 7 and 8 are shorted together, the magnitude of the charging current due to R_A can be calculated from:

$$I = \frac{R_1 \times V_{CC}}{(R_1 + R_2)} \times \frac{1}{R_A} = \frac{V_{CC}}{5R_A}$$

A similar calculation holds for R_B.

The capacitor value should be as large as possible.

WAVEFORM OUT LEVEL CONTROL AND POWER SUPPLIES

The waveform generator can be operated either from a single power-supply (10 to 30 Volts) or a dual power-supply (±5 to ±15 Volts). With a single power-supply the average levels of the triangle and sine-wave are at exactly one-half of the supply voltage, while the square-wave alternates between +V and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square-wave output is not committed. A load resistor can be connected to a different power-supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30V). In this way, the square-wave output be made TTL compatible (load resistor connected to +5 Volts) while the waveform generator itself is powered from a much higher voltage.

FREQUENCY MODULATION AND SWEEPING

The frequency of the waveform generator is a direct function of the DC voltage at terminal 8 (measured from $+V_{CC}$). By altering this voltage, frequency modulation is performed.

For small deviations (e. g. ±10%) the modulating signal can be applied directly to pin 8, merely providing dc decoupling with a capacitor, as shown in Figure 10a. An external resistor between pins 7 and 8 is not necessary, but it can be used to increase input impedance. Without it (i.e. terminals 7 and 8 connected together), the input impedance is 8kΩ; with it, this impedance increases to (R+8kΩ).

For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 10b). In this way the entire bias for the current sources is created by the modulating signal and a very large (e.g. 1000:1) sweep range is created (f = 0 at $V_{sweep} = 0$). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger thresholds still are) and thus the frequency becomes dependent on the supply voltage. The potential on Pin 8 may be swept from V_{CC} to (2/3 V_{CC} + 2V).

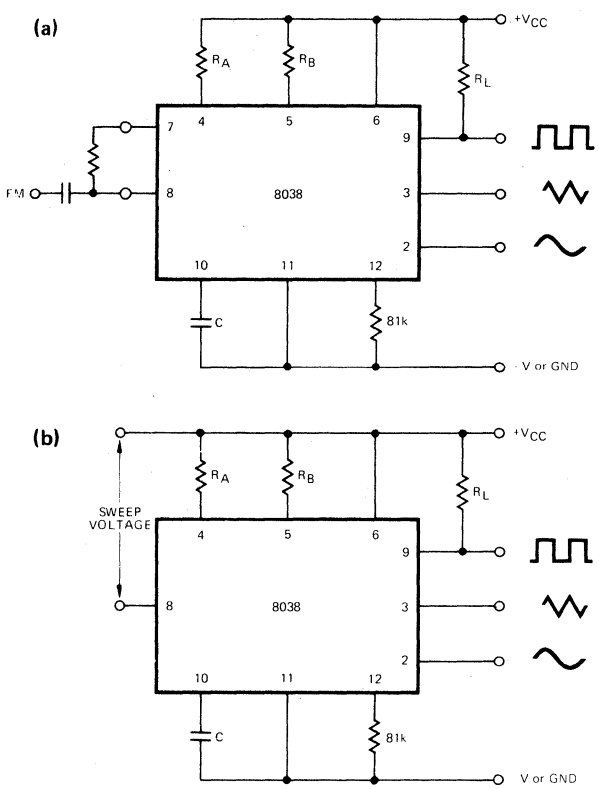


FIGURE 10. CONNECTIONS FOR FREQUENCY MODULATION (a) AND SWEEP (b).

WG-8038

APPLICATIONS

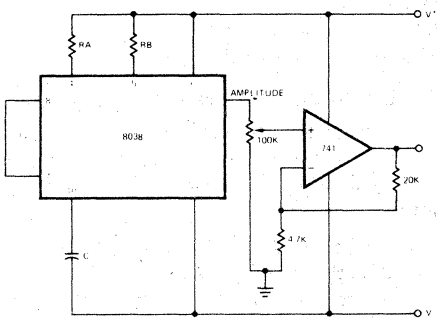


FIGURE 11. SINE WAVE OUTPUT BUFFER AMPLIFIERS

The sine wave output has a relatively high output impedance (1KΩ Typ). The circuit of Figure 11 provides buffering, gain and amplitude adjustment. A simple op amp follower could also be used.

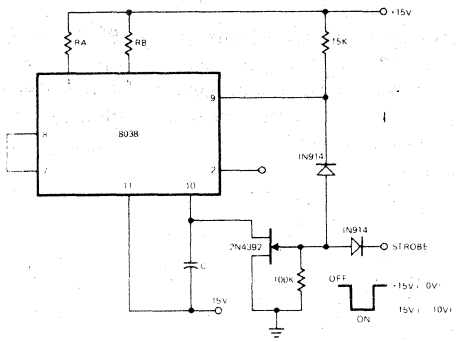


FIGURE 12. STROBE – TONE BURST GENERATOR

With a dual supply voltage the external capacitor on Pin 10 can be shorted to ground to halt the 8038 oscillation. Figure 12 shows a FET switch, diode ANDed with an input strobe signal to allow the output to always start on the same slope.

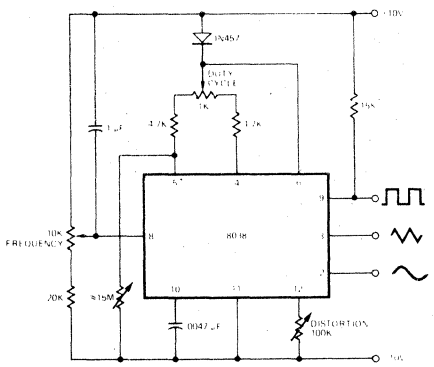


FIGURE 13. VARIABLE AUDIO OSCILLATOR, 20Hz to 20 KHz

To obtain a 1000:1 Sweep Range on the 8038 the voltage across external resistors RA and RB must decrease to nearly zero. This requires that the highest voltage on control Pin 8 exceed the voltage at the top of RA and RB by a few hundred millivolts.

The Circuit of Figure 13 achieves this by using a diode to lower the effective supply voltage on the 8038. The large resistor on pin 5 helps reduce duty cycle variations with sweep.

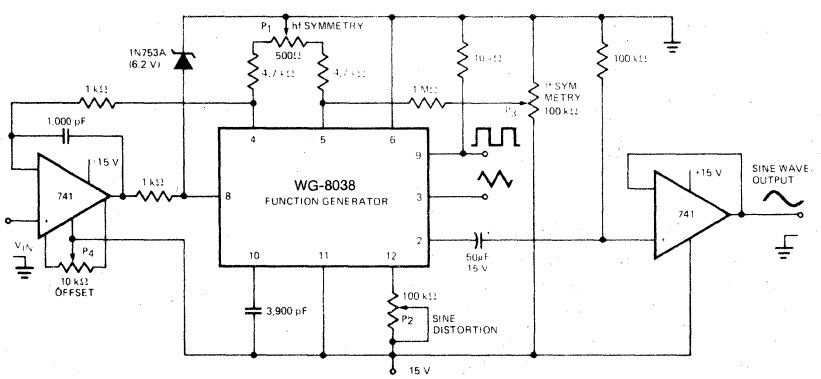
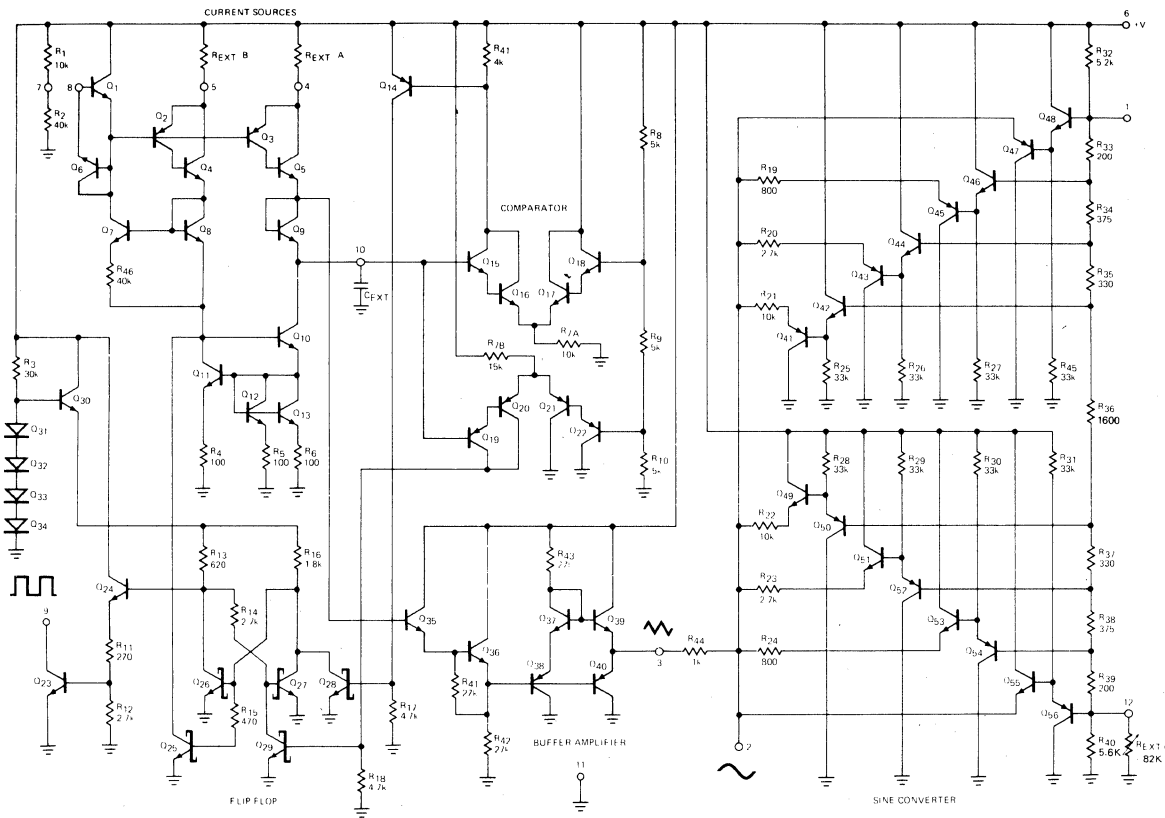


FIGURE 14. LINEAR VOLTAGE CONTROLLED OSCILLATOR

The linearity of input sweep voltage verses output frequency can be significantly improved by using an op amp as shown in Figure 14.

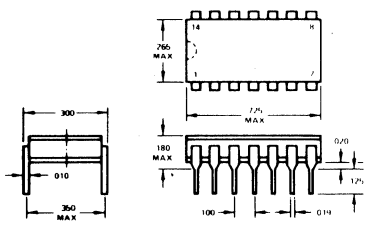
WG-8038

DETAILED SCHEMATIC



PACKAGE DIMENSIONS

14 PIN CERDIP



DATEL INTERSIL

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PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Analog Switches

Quick Selection: Analog Switches

MODEL	SWITCH TYPE	ON RESISTANCE	OFF LEAKAGE CURRENT, MAX.	TURN ON TIME, MAX.	PACKAGE	OPER. TEMP. RANGE(°C)	PRICE (1-24)	SEE PAGE
AS-5040C	SPST	80Ω	5nA	500nsec	16 PIN PLAS. DIP	0 to +70	**$ 4.27**	444C
AS-5040M					16 PIN CERDIP	−55 to +125	**$12.00**	
AS-5041C	DUAL SPST	80Ω	5nA	500nsec	16 PIN PLAS. DIP	0 to +70	**$ 4.87**	444C
AS-5041M					16 PIN CERDIP	−55 to +125	**$12.07**	
AS-5042C	SPDT	80Ω	5nA	500nsec	16 PIN PLAS. DIP	0 to +70	**$ 4.87**	444C
AS-5042M					16 PIN CERDIP	−55 to +125	**$12.07**	
AS-5043C	DUAL SPDT	80Ω	5nA	500nsec	16 PIN PLAS. DIP	0 to +70	**$ 6.82**	444C
AS-5043M					16 PIN CERDIP	−55 to +125	**$22.50**	
AS-5044C	DPST	80Ω	5nA	500nsec	16 PIN PLAS. DIP	0 to +70	**$ 5.87**	444C
AS-5044M					16 PIN CERDIP	−55 to +125	**$12.00**	
AS-5045C	DUAL DPST	80Ω	5nA	500nsec	16 PIN PLAS. DIP	0 to +70	**$ 6.82**	444C
AS-5045M					16 PIN CERDIP	−55 to +125	**$22.57**	
AS-5046C	DPDT	80Ω	5nA	500nsec	16 PIN PLAS. DIP	0 to +70	**$ 6.82**	444C
AS-5046M					16 PIN CERDIP	−55 to +125	**$22.57**	
AS-5047C	4PST	80Ω	5nA	500nsec	16 PIN PLAS. DIP	0 to +70	**$ 6.82**	444C
AS-5047M					16 PIN CERDIP	−55 to +125	**$24.07**	
AS-5048C	DUAL SPST	45Ω	5nA	300nsec	16 PIN PLAS. DIP	0 to +70	**$ 7.95**	444C
AS-5048M					16 PIN CERDIP	−55 to +125	**$14.45**	

MODEL	SWITCH TYPE	ON RESISTANCE	OFF LEAKAGE CURRENT, MAX.	TURN ON TIME, MAX.	PACKAGE	OPER. TEMP. RANGE(°C)	PRICE (1-24)	SEE PAGE
AS-5049C	DPST	45Ω	5nA	300nsec	16 PIN PLAS. DIP	0 to +70	**$10.50**	444C
AS-5049M					16 PIN CERDIP	−55 to +125	**$27.75**	
AS-5050C	SPDT	45Ω	5nA	300nsec	16 PIN PLAS. DIP	0 to +70	**$ 7.95**	444C
AS-5050M					16 PIN CERDIP	−55 to +125	**$14.45**	
AS-5051C	SPDT	45Ω	5nA	300nsec	16 PIN PLAS. DIP	0 to +70	**$10.50**	444C
AS-5051M					16 PIN CERDIP	−55 to +125	**$27.75**	
AS-5140C	SPST	75Ω	0.5nA	175nsec	16 PIN PLAS. DIP	0 to +70	**$ 6.17**	454C
AS-5140M					16 PIN CERDIP	−55 to +125	**$26.35**	
AS-5141C	DUAL SPST	75Ω	0.5nA	175nsec	16 PIN PLAS. DIP	0 to +70	**$ 6.82**	454C
AS-5141M					16 PIN CERDIP	−55 to +125	**$29.25**	
AS-5142C	SPDT	75Ω	0.5nA	300nsec	16 PIN PLAS. DIP	0 to +70	**$ 6.82**	454C
AS-5142M					16 PIN CERDIP	−55 to +125	**$29.25**	
AS-5143C	DUAL SPDT	75Ω	0.5nA	300nsec	16 PIN PLAS. DIP	0 to +70	**$ 8.17**	454C
AS-5143M					16 PIN CERDIP	−55 to +125	**$37.50**	
AS-5144C	DPST	75Ω	0.5nA	300nsec	16 PIN PLAS. DIP	0 to +70	**$ 6.82**	454C
AS-5144M					16 PIN CERDIP	−55 to +125	**$29.25**	
AS-5145C	DUAL DPST	75Ω	0.5nA	300nsec	16 PIN PLAS. DIP	0 to +70	**$ 8.17**	454C
AS-5145M					16 PIN CERDIP	−55 to +125	**$37.50**	

THESE PRODUCTS ARE COVERED BY GAS CONTRACT

AS-5040/AS-5051 Family High Level CMOS Analog Gates

FEATURES

- Switches Greater Than 20Vpp Signals With ±15V Supplies
- Quiescent Current Less Than 1μA
- Overvoltage Protection to ±25V
- Break-Before-Make Switching t_{OFF} 200nsec, t_{ON} 300nsec Typical
- T²L, DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- Low r_{DS} (ON) – 35Ω
- New DPDT & 4PST Configurations
- Complete Monolithic Construction AS-5040 through AS-5047

CMOS ANALOG GATE PRODUCT CONDITIONING

The following processes are performed 100% in accordance with MIL-STD-883.

Precap Visual – Method 2010, Cond. B.
Stabilization Bake – Method 1008
Temperature Cycle – Method 1010
Centrifuge – Method 2001, Cond. E
Hermeticity – Method 1014, Cond. A, C.
(Leak Rate $< 5 \times 10^{-7}$ atm cc/s)

GENERAL DESCRIPTION

The AS-5040 family of solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. These devices provide ease-of-use and performance advantages not previously available from solid state switches. This improved CMOS technology provides input overvoltage capability to ±25 volts without damage to the device, and destructive latch-up of solid state analog gates has been eliminated. Early CMOS gates were destroyed when power supplies were removed with an input signal present. The AS-5040 CMOS technology has eliminated this serious systems problem.

Key performance advantages of the 5040 series are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 1μA. Also designed into the 5040 is guaranteed Break-Before-Make switching, which is accomplished by extending the t_{ON} time (300 nsec TYP.) so that it exceeds t_{OFF} time (200 nsec TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. This eliminates the need for external logic required to avoid channel to channel shorting during switching.

Many of the 5040 series improve upon and are pin-for-pin and electrical replacements for other solid state switches.

FUNCTIONAL DIAGRAM

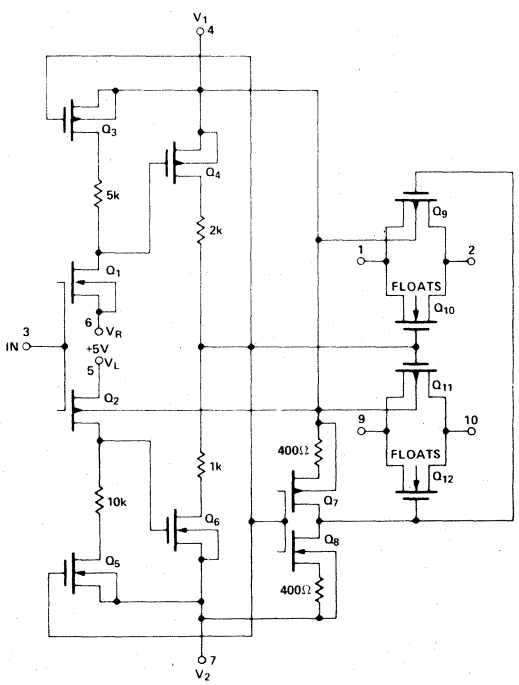


FIGURE 1. TYPICAL DRIVER, GATE — AS-5042

FUNCTIONAL DESCRIPTION

PART NO.	TYPE	R_{ON}	FUNCTIONAL EQUIVALENT
AS-5040	SPST	75Ω	
AS-5041	Dual SPST	75Ω	
AS-5042	SPDT	75Ω	DG 188AA/BA
AS-5043	Dual SPDT	75Ω	DG 191AP/BP
AS-5044	DPST	75Ω	
AS-5045	Dual DPST	75Ω	DG 185AP/BP
AS-5046	DPDT	75Ω	
AS-5047	4PST	75Ω	
AS-5048 (hybrid)	Dual SPST	35Ω	
AS-5049 (hybrid)	Dual DPST	35Ω	DG 184AP/BP
AS-5050 (hybrid)	SPDT	35Ω	DG 187AA/BA
AS-5051 (hybrid)	Dual SPDT	35Ω	DG 190AP/BP

MAXIMUM RATINGS

Current (Any Terminal)	< 30mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Power Dissipation	450mW
(All Leads Soldered to a P. C. Board) Derate 6mW/°C Above 70°C	
Lead Temperature (Soldering, 10 sec)	300°C

$V_I - V_2$	< 33V
$V_I - V_D$	< 30V
$V_D - V_2$	< 30V
$V_D - V_S$	< ±22V
$V_L - V_2$	< 33V
$V_L - V_{IN}$	< 30V
$V_L - V_R$	< 20V
$V_{IN} - V_R$	< 20V

ELECTRICAL CHARACTERISTICS (@ 25°C, V_1 = +15 V, V_2 = −15 V, V_L = +5 V, V_R = 0 V)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	-55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	TEST CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	µA	V_{IH} 2.4 V Note 1
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	µA	V_{IH} 0.8 V Note 1
$r_{DS(ON)}$	Drain Source On Resistance	75(35)	75(35)	150(60)	80 (45)	80 (45)	130 (45)	Ω	(5048 Thru 5051) I_S 1mA. V_{ANALOG} 10 V to −10 V
$\Delta r_{DS(ON)}$	Channel to Channel $R_{DS(ON)}$ Match	25(15)	25 (15)	25(15)	30(15)	30(15)	30(15)	Ω	(5048 thru 5051) I_S (Each Channel) 1 mA.
V_{ANALOG}	Min. Analog Signal Handling Capability	+11(+10)	+11(+10)	+11(+10)	+10(+10)	+10(+10)	+10(+10)	V	I_S 10 mA (5048 thru 5051)
$I_{D(OFF)}$	Switch OFF Leakage Current	1(1)	1(1)	100(100)	5(5)	5(5)	100(100)	nA	V_{ANALOG} 10 V to −10 V (5048 thru 5051)
$I_{D(ON)}$ + $I_{S(ON)}$	Switch On Leakage Current	2(2)	2(2)	200(200)	10 (10)	10 (10)	100(200)	nA	V_D V_S 10 V to −10 V (5048 thru 5051)
t_{ON}	Switch "ON" Time		500(250)			500(300)		ns	R_L 1 kΩ, V_{ANALOG} 10V to −10 V See Fig. A
t_{OFF}	Switch "OFF" Time		250(150)			250(150)		ns	R_L 1 kΩ, V_{ANALOG} 10 V to −10 V See Fig. A (5048 thru 5051)
$Q_{(INJ.)}$	Charge Injection		15 (10)			20 (10)		mV	See Fig. B (5048 thru 5051)
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f 1 MHz, R_L 100Ω, C_L 5 pF See Fig. C
I_{V1}	+ Power Supply Quiescent Current	1	1	10	10	10	100	µA	
I_{V2}	− Power Supply Quiescent Current	1	1	10	10	10	100	µA	V_1 +15 V, V_2 −15 V, V_L +5 V V_L +5 V, V_R 0 Switch Duty Cycle 10%
I_{VL}	+5 V Supply Quiescent Current	1	1	10	10	10	100	µA	
I_{VR}	Gnd Supply Quiescent Current	1	1	10	10	10	100	µA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off. Any Other Channel Switches as per Fig. E

TEST CIRCUITS

FIG. A

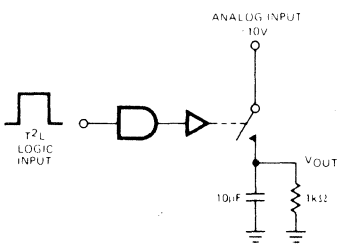


FIG. B

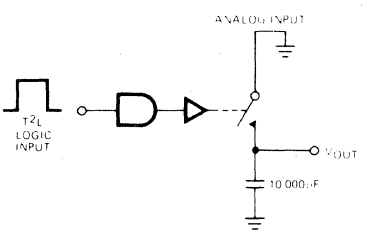
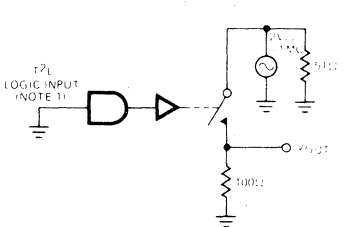


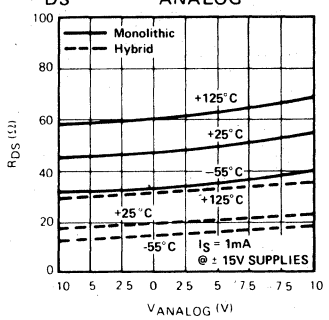
FIG. C



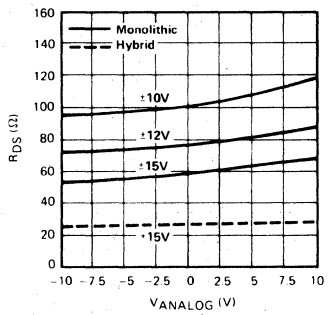
NOTE 1: Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

TYPICAL ELECTRICAL CHARACTERISTICS (Per Channel)

R_{DS} (ON) vs V_{ANALOG} SIGNAL



R_{DS} (ON) vs POWER SUPPLY VOLTAGE



CHARGE INJECTION vs V_{ANALOG} (SEE FIG. B) C_L = 10,000pF

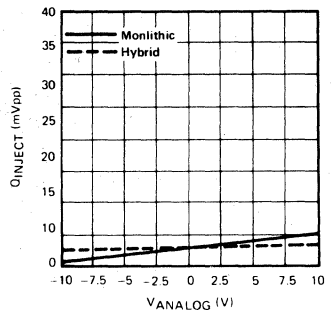
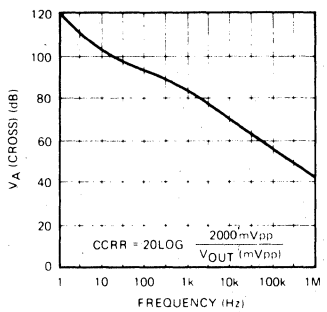


FIGURE D

CROSS COUPLING REJECTION vs FREQUENCY



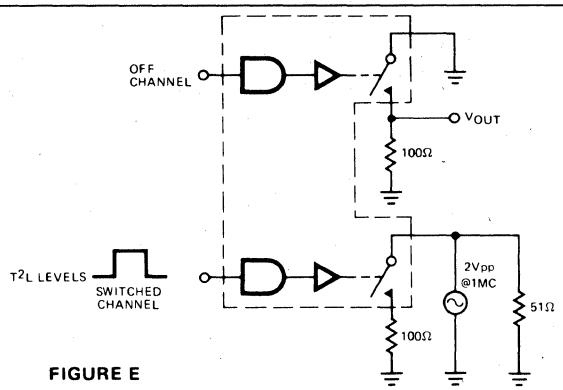
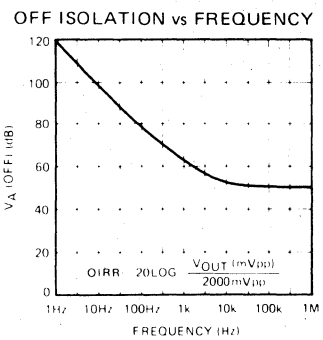


FIGURE E

OFF ISOLATION vs FREQUENCY



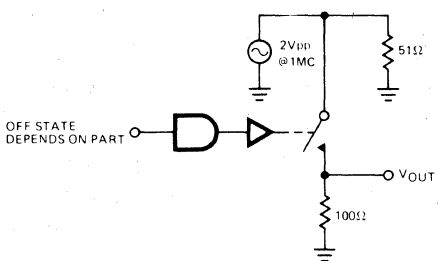
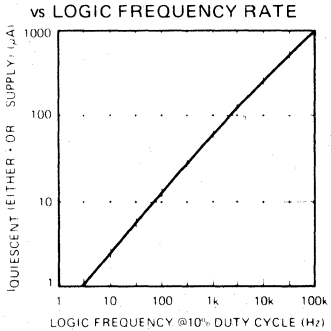


FIGURE F

POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE



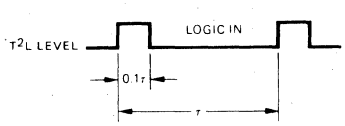


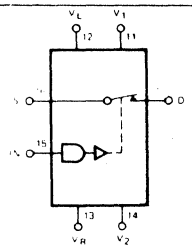
FIGURE G

SWITCHING STATE DIAGRAMS

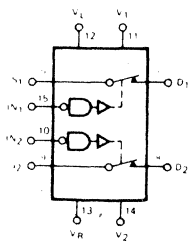
SWITCH STATES
ARE FOR LOGIC "1" INPUT

DIP PACKAGE

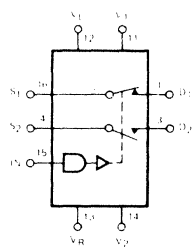
SPST
5040 (r_{DS} (ON) <75Ω)



DUAL SPST
5041 (r_{DS} (ON) <75Ω)

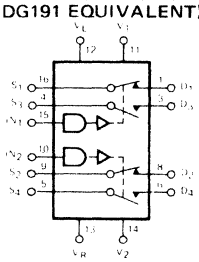


SPDT
5042 (r_{DS} (ON) <75Ω)

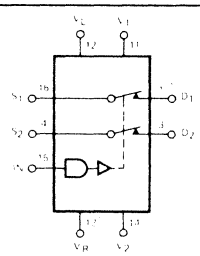


(DG191 EQUIVALENT)

DUAL SPDT
5043 (r_{DS}(ON) <75Ω)

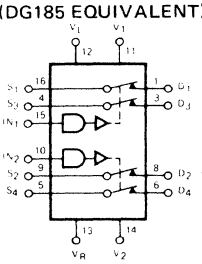


DPST
5044 (r_{DS} (ON) <75Ω)



(DG185 EQUIVALENT)

DUAL DPST
5045 (r_{DS} (ON) <75Ω)

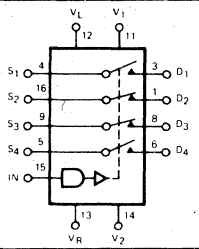


SWITCHING STATE DIAGRAMS (Cont.)

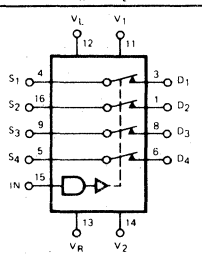
SWITCH STATES
ARE FOR LOGIC "1" INPUT

DIP PACKAGE

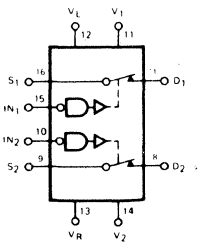
DPDT
5046 (r_{DS} (ON) <75Ω)



4PST
5047 (r_{DS} (ON) <75Ω)

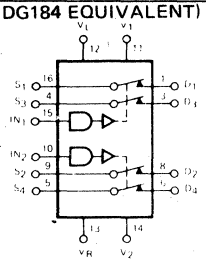


DUAL SPST
5048 (r_{DS} (ON) <35Ω)

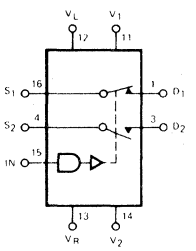


(DG184 EQUIVALENT)

DUAL DPST
5049 (r_{DS} (ON) <35Ω)

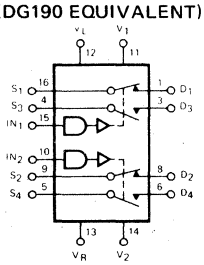


SPDT
5050 (r_{DS} (ON) <35Ω)



(DG190 EQUIVALENT)

DUAL SPDT
5051 (r_{DS} (ON) <35Ω)



APPLICATIONS

IMPROVED SAMPLE & HOLD
USING AS-5043

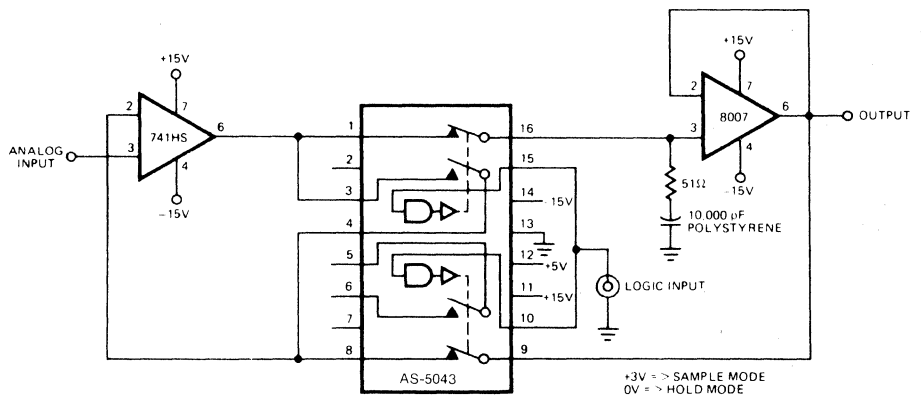


FIGURE H

USING THE CMOS SWITCH TO DRIVE
AN R/2R LADDER NETWORK (2 LEGS)

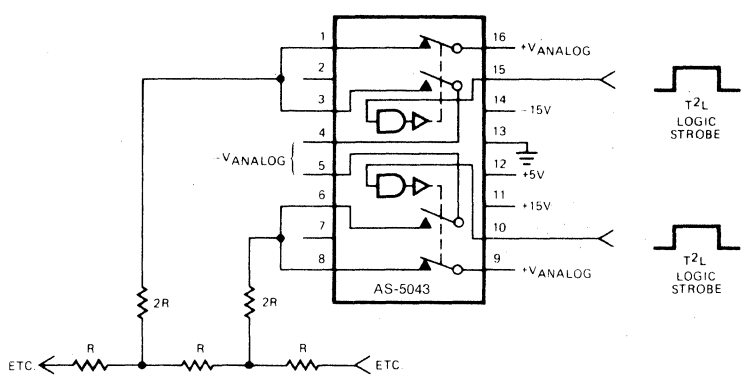


FIGURE I

EXAMPLE: If $-V_{ANALOG} = -10VDC$ and $+V_{ANALOG} = +10VDC$ then Ladder Legs are switched between ±10VDC, depending upon state of Logic Strobe.

THEORY OF OPERATION

A. FLOATING BODY CMOS STRUCTURE

In a conventional C-MOS structure, the body of the "n" channel device is tied to the negative supply, thus forming a reverse biased diode between the drain/source and the body (Fig. J). Under certain conditions this diode can become forward biased; for example, if the supplies are off (at ground) and a negative input is applied to the drain. This can have serious consequences for two reasons. Firstly, the diode has no current limiting and if excessive current flows, the circuit may be permanently damaged. Secondly, this diode forms part of a parasitic SCR in the conventional C-MOS structure. Forward biasing the diode causes the SCR to turn on, giving rise to a "latch-up" condition.

The new improved C-MOS process incorporates an additional diode in series with the body (Fig. K). The cathode of this diode is then tied to V+, thus effectively floating the body. The inclusion of this diode not only blocks the excessive current path, but also prevents the SCR from turning on.

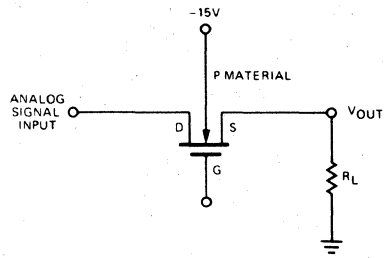


FIGURE J

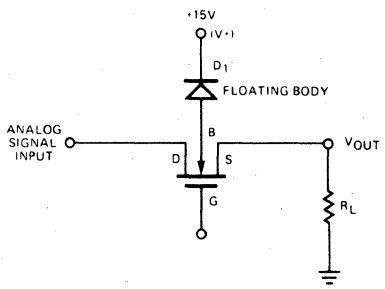


FIGURE K

B. OVERVOLTAGE PROTECTION

The floating body construction inherently provides overvoltage protection. In the conventional C-MOS process, the body of all N-channel FETs is tied to the most negative power supply and the body of all P-channel devices to the most positive supply (i. e., ±15V). Thus, for an overvoltage spike of $>$ ±15V, a forward bias condition exists between drain and body of the MOSFET. For example, in Fig. J if the analog signal input is more negative than −15V, the drain to body of the N-channel FET is forward biased and destruction of the device can result. Now by floating the body, using diode D1, the drain to body of the MOSFET is still forward biased, but D1 is reversed biased so no current flows (up to the breakdown of D1 which is $\geq$ 40V). Thus, negative excursions of the analog signal can go up to a maximum of -25V. When the signal goes positive ($\geq$ +15V, D1 is forward biased, but now the drain to body junction is reversed for the N-channel FET; this allows the signal to go to a maximum of +25V with no appreciable current flow. While the explanation above has been restricted to N-channel devices, the same applies to P-channel FETs and the construction is as shown in Fig. L. Fig. L describes an output stage showing the paralleling of an N and P channel to linearize the $r_{DS(ON)}$ with signal input. The presence of diodes D1 and D2 effectively floats the bodies and provides over voltage protection to a maximum of ±25V.

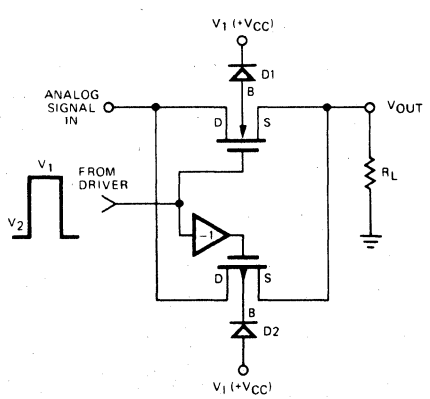
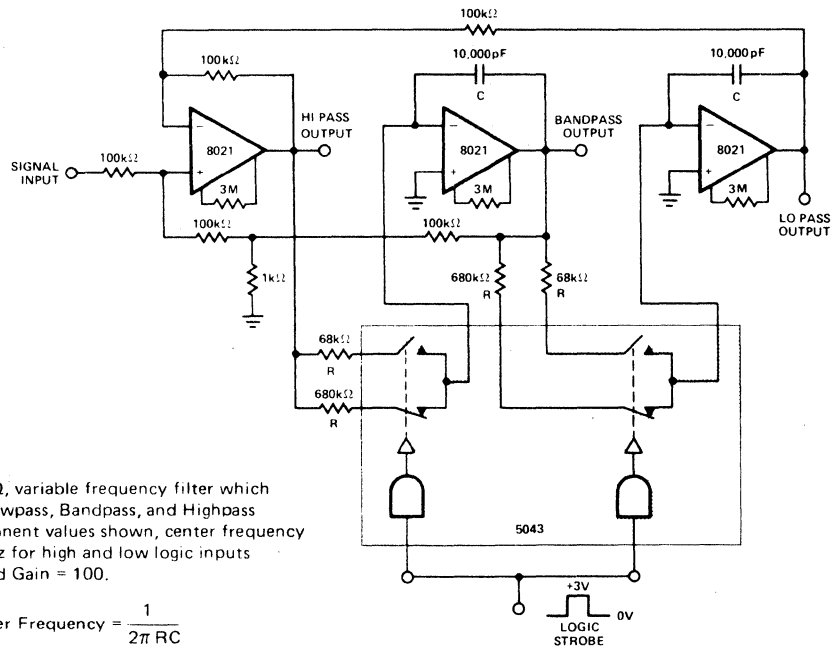


FIGURE L

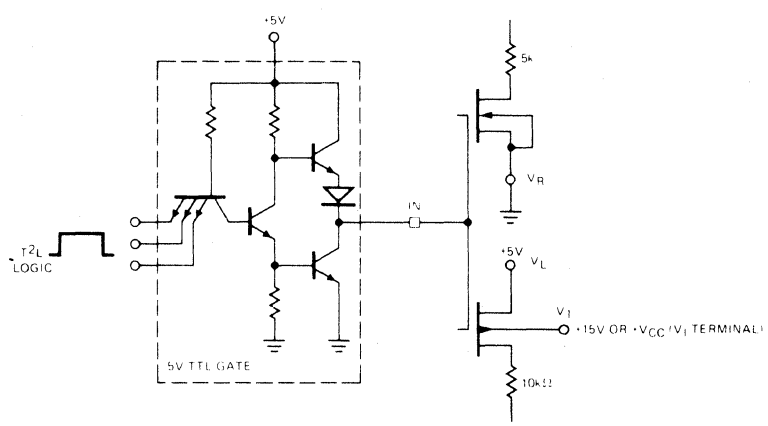
DIGITALLY TUNED
LOW POWER ACTIVE FILTER



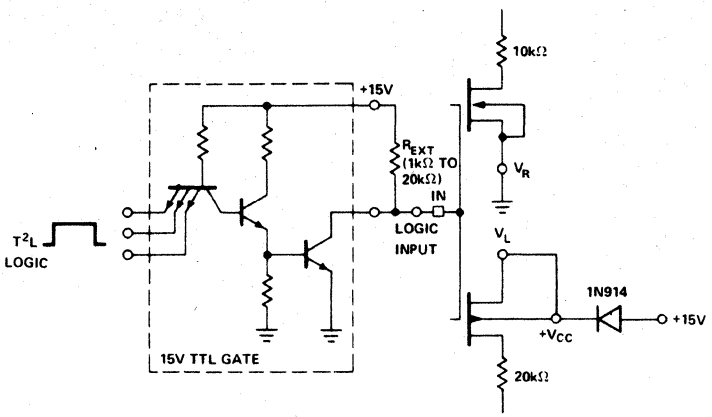
Constant gain, constant Q, variable frequency filter which provides simultaneous Lowpass, Bandpass, and Highpass outputs. With the component values shown, center frequency will be 235Hz and 23.5Hz for high and low logic inputs respectively, Q = 100, and Gain = 100.

$$f_n = \text{Center Frequency} = \frac{1}{2\pi RC}$$

LOGIC INTERFACING

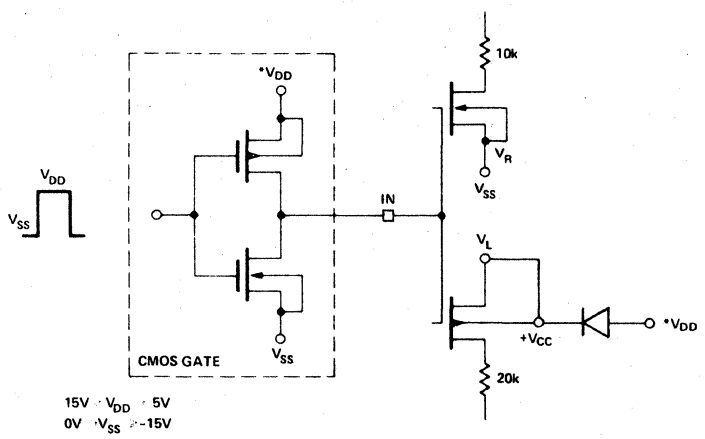


FOR INTERFACING WITH T^2L OPEN COLLECTOR LOGIC.



TYP. EXAMPLE FOR +15V CASE SHOWN

FOR USE WITH CMOS LOGIC.



15V ≤ V_{DD} ≤ 5V
0V ≤ V_{SS} ≤ -15V

ORDERING INFORMATION

MODEL	SWITCH CONFIGURATION	OPER. TEMP RANGE	PACKAGE
AS-5040C	SPST	0 to +70° C	16 pin Epoxy
AS-5040M		−55 to +125° C	16 pin Cerdip
AS-5041C	Dual SPST	0 to +70° C	16 pin Epoxy
AS-5041M		−55 to +125° C	16 pin Cerdip
AS-5042C	SPDT	0 to +70° C	16 pin Epoxy
AS-5042M		−55 to + 125 ° C	16 pin Cerdip
AS-5043C	Dual SPDT	0 to +70° C	16 pin Epoxy
AS-5043M		−55 to +125° C	16 pin Cerdip
AS-5044C	DPST	0 to +70° C	16 pin Epoxy
AS-5044M		−55 to +125° C	16 pin Cerdip
AS-5045C	Dual DPST	0 to +70° C	16 pin Epoxy
AS-5045M		−55 to +125° C	16 pin Cerdip
AS-5046C	DPDT	0 to +70° C	16 pin Epoxy
AS-5046M		−55 to +125° C	16 pin Cerdip
AS-5047C	4PST	0 to +70° C	16 pin Epoxy
AS-5047M		−55 to +125° C	16 pin Cerdip
AS-5048C	Dual SPST	0 to +70° C	16 pin Epoxy
AS-5048M		−55 to +125° C	16 pin Cerdip
AS-5049C	Dual DPST	0 to +70° C	16 pin Epoxy
AS-5049M		−55 to +125° C	16 pin Cerdip
AS-5050C	SPDT	0 to +70° C	16 pin Epoxy
AS-5050M		−55 to +125° C	16 pin Cerdip
AS-5051C	Dual SPDT	0 to +70° C	16 pin Epoxy
AS-5051M		−55 to +125° C	16 pin Cerdip

AS-5140/AS-5145 Family High Level CMOS Analog Gates

FEATURES

- **Super fast break before make switching t_{on} 80ns typ, t_{off} 50ns typ (SPST switches)**
- **Power supply currents less than 1μA**
- **"OFF" leakages less than 100pA @ 25°C guaranteed**
- **Non-latching with supply turn-off**
- **Single monolithic CMOS chip**
- **Plug-in replacements for 5040 family and part of the DG180 family to upgrade speed and leakage**
- **Greater than 1MHz toggle rate**
- **Switches greater than 20Vp-p signals with ±15V supplies**
- **T^2L, CMOS direct compatibility**

CMOS ANALOG GATE PRODUCT CONDITIONING

The following processes are performed 100% in accordance with MIL-STD-883.
Precap Visual — Method 2010, Cond. B
Stabilization Bake — Method 1008
Temperature Cycle — Method 1010
Centrifuge — Method 2001, Cond. E
Hermeticity — Method 1014, Cond. A, C
(Leak Rate < 5 x 10^{-7} atm cc/s)

GENERAL DESCRIPTION

The AS-5140 Family of CMOS monolithic switches utilizes latch-free junction isolated processing to build the fastest switches now available. "OFF" leakages are guaranteed to be less than 100pA at 25°C. These switches can be toggled at a rate of greater than 1MHz with super fast t_{on} times (80ns typical) and faster t_{off} times (50ns typical) guaranteeing break before make switching. This family of switches therefore combines the speed of the hybrid FET DG180 Family with the reliability and low power consumption of a monolithic CMOS construction.

No quiescent power is dissipated in either the "ON" or the "OFF" state of the switch. Maximum power supply current is 1μA from any supply and typical quiescent currents are in the 10nA range which makes these devices ideal for portable equipment and military applications.

The AS-5140 Family is completely compatible with TTL (5V) logic, TTL open collector logic and CMOS logic gates. It is pin compatible with Datel's AS-5040 Family and part of the DG180/190 Family.

ORDERING INFORMATION

MODEL	SWITCH CONFIGURATION	OPER. TEMP RANGE	PACKAGE
AS-5140C	SPST	0 to +70°C	16 pin Epoxy
AS-5140M		−55 to +125°C	16 pin Cerdip
AS-5141C	Dual SPST	0 to +70°C	16 pin Epoxy
AS-5141M		−55 to +125°C	16 pin Cerdip
AS-5142C	SPDT	0 to +70°C	16 pin Epoxy
AS-5142M		−55 to +125°C	16 pin Cerdip
AS-5143C	Dual SPDT	0 to +70°C	16 pin Epoxy
AS-5143M		−55 to +125°C	16 pin Cerdip
AS-5144C	DPST	0 to +70°C	16 pin Epoxy
AS-5144M		−55 to +125°C	16 pin Cerdip
AS-5145C	Dual DPST	0 to +70°C	16 pin Epoxy
AS-5145M		−55 to +125°C	16 pin Cerdip

AS-5140-AS-5145 Family

MAXIMUM RATINGS

Current (Any Terminal) ..... < 30 mA
Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Power Dissipation ..... 450 mW
(All Leads Soldered to a P.C. Board)
Derate 6 mW/°C Above 70°C
Soldering Temperature

V_I—V_2 <33V
V_I—V_D <30V
V_D—V_2 <30V
V_D—V_S <±22V
V_L—V_2 <33V
V_L—V_{IN} <30V
V_L—V_R <20V
V_{IN}—V_R <20V

ELECTRICAL CHARACTERISTICS (@ 25°C, V_1 = +15V, V_2 = -15V, V_L = +5V, V_R = 0 V)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	-55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	TEST CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 2.4 V Note 1
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 0.8 V Note 1
$R_{DS(ON)}$	Drain—Source On Resistance	50	50	75	75	75	100	Ω	I_S = -10 mA V_{ANALOG} = -10 V to +10 V
$\Delta R_{DS(ON)}$	Channel to Channel $R_{DS(ON)}$ Match	25	25	25	30	30	30	Ω	I_S (Each Channel) = -10 mA
V_{ANALOG}	Min. Analog Signal Handling Capability	±11	±11	±11	±10	±10	±10	V	I_S = 10 mA
$I_{D(OFF)}$	Switch OFF Leakage	0.1	0.1	20	0.5	0.5	20	nA	V_D = +10 V, V_S = -10 V
$I_{S(OFF)}$	Current	0.1	0.1	20	0.5	0.5	20		V_D = -10V, V_S = +10 V
$I_{D(ON)}$	Switch On Leakage	0.2	0.2	40	1	1	40	nA	V_D = V_S = -10 V to +10 V
$+I_{S(ON)}$	Current								
t_{ON}	Switch "ON" Time	See pages 4 & 5 for switching time specifications and timing diagrams.							
t_{OFF}	Switch "OFF" Time								
$Q_{(INJ)}$	Charge Injection		10			15		mVPP	See Fig. 4, Note 2
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R_L = 100Ω, C_L ≤ 5 pF See Fig. 5, Note 2
I_{V1}	+ Power Supply Quiescent Current	1.0	1.0	10.0	10	10	100	μA	V_1 = +15 V, V_2 = -15 V, V_L = +5 V, V_R = 0 Switch Duty Cycle < 10% See Fig. 6
I_{V2}	- Power Supply Quiescent Current	1.0	1.0	10.0	10	10		μA	
I_{VL}	+5 V Supply Quiescent Current	1.0	1.0	10.0	10	10	100	μA	
I_{VR}	Gnd Supply Quiescent Current	1.0	1.0	10.0	10	10	100	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off; Any Other Channel Switches See Fig. 7, Note 2

Note: 1. Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.
2. Charge injection, OFF isolation, and Channel to Channel isolation are only sample tested in production.

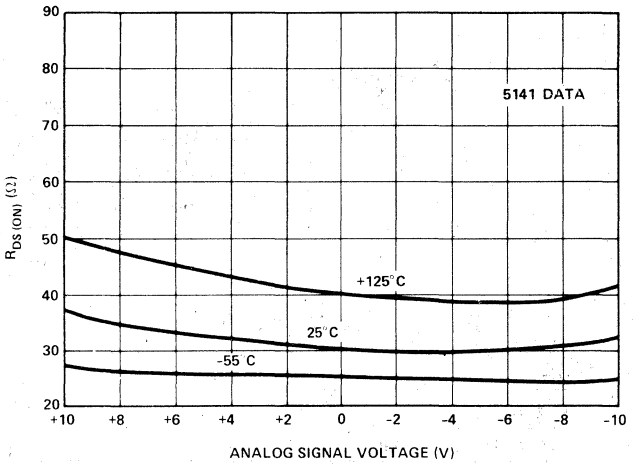


FIGURE 2. $R_{DS(ON)}$ vs. Temp., @ ±15V, +5V Supplies.

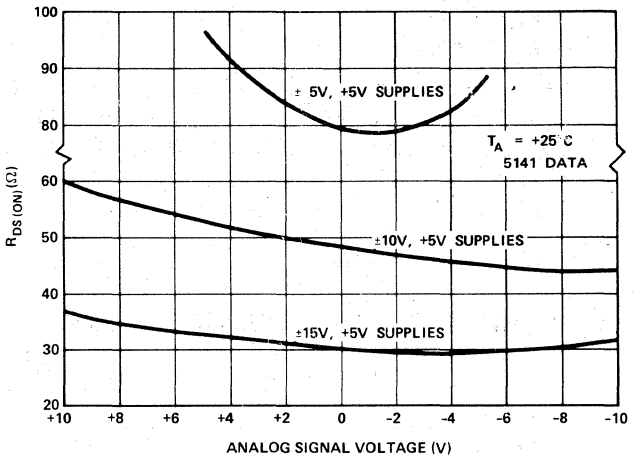


FIGURE 3. $R_{DS(ON)}$ vs. Power Supplies.

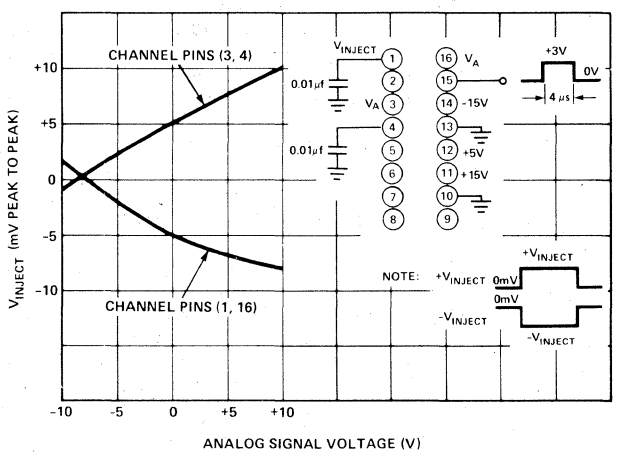


FIGURE 4. Charge Injection vs. Analog Signal.

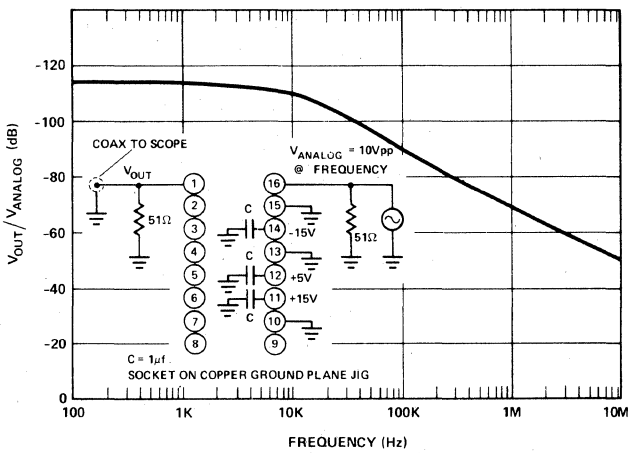


FIGURE 5. "OFF" Isolation vs. Frequency.

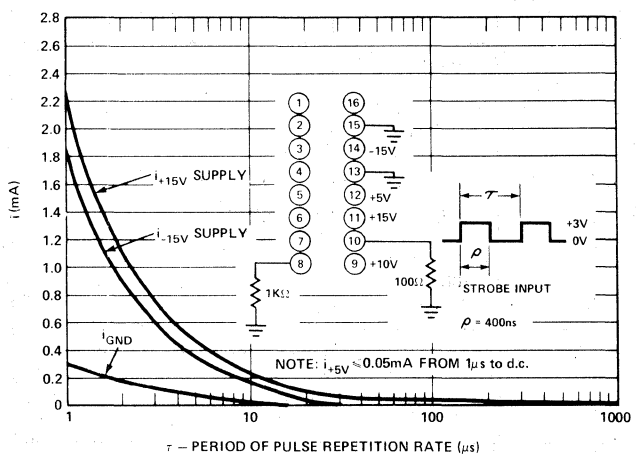


FIGURE 6. Power Supply Current Draws vs. Logic Strobe Rate.

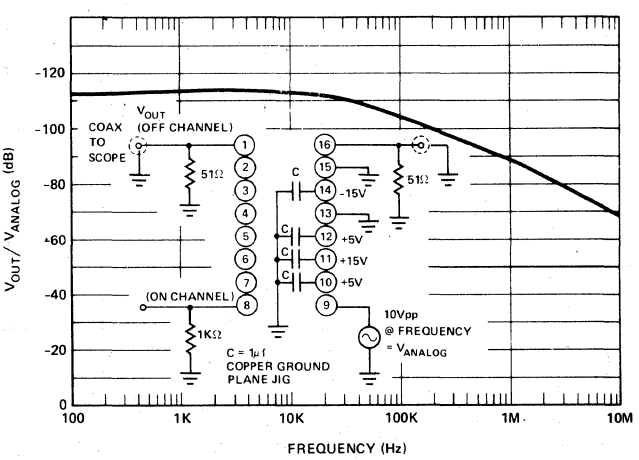


FIGURE 7. Channel to Channel Cross Coupling Rejection vs. Frequency.

AS-5140-AS-5145 Family

SWITCHING TIME SPECIFICATIONS

(t_{on}, t_{off} are maximum specifications and t_{on}-t_{off} is minimum specifications)

Part Number	Symbol	Characteristics	MILITARY -55°C	MILITARY +25°C	MILITARY +125°C	COMMERCIAL 0°C	COMMERCIAL +25°C	COMMERCIAL +70°C	Units	Test Conditions
5140-5141	t_{ON}	Switch "ON" time		100			150		ns	Figure 8
	t_{OFF}	Switch "OFF" time		75			125			
	t_{ON}-t_{OFF}	Break-before-make		10			5			
	t_{ON}	Switch "ON" time		150			175		ns	Figure 9
	t_{OFF}	Switch "OFF" time		125			150			
	t_{ON}-t_{OFF}	Break-before-make		10			5			
5142-5143	t_{ON}	Switch "ON" time		175			250		ns	Figure 8
	t_{OFF}	Switch "OFF" time		125			150			
	t_{ON}-t_{OFF}	Break-before-make		10			5			
	t_{ON}	Switch "ON" time		200			300		ns	Figure 9
	t_{OFF}	Switch "OFF" time		125			150			
	t_{ON}-t_{OFF}	Break-before-make		10			5			
	t_{ON}	Switch "ON" time		175			250		ns	Figure 10
	t_{OFF}	Switch "OFF" time		125			150			
	t_{ON}-t_{OFF}	Break-before-make		10			5			
	t_{ON}	Switch "ON" time		200			300		ns	Figure 11
	t_{OFF}	Switch "OFF" time		125			150			
	t_{ON}-t_{OFF}	Break-before-make		10			5			
5144-5145	t_{ON}	Switch "ON" time		175			250		ns	Figure 8
	t_{OFF}	Switch "OFF" time		125			150			
	t_{ON}-t_{OFF}	Break-before-make		10			5			
	t_{ON}	Switch "ON" time		200			300		ns	Figure 9
	t_{OFF}	Switch "OFF" time		125			150			
	t_{ON}-t_{OFF}	Break-before-make		10			5			

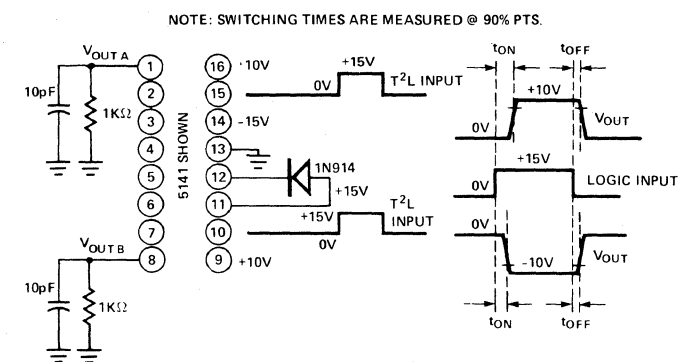


FIGURE 8.

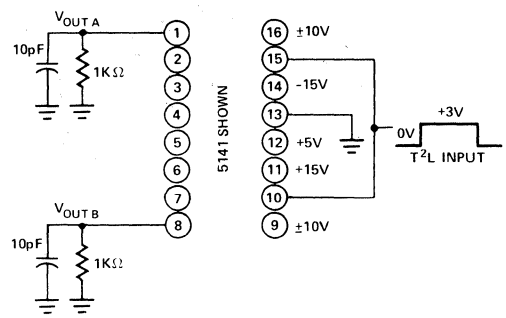


FIGURE 9.

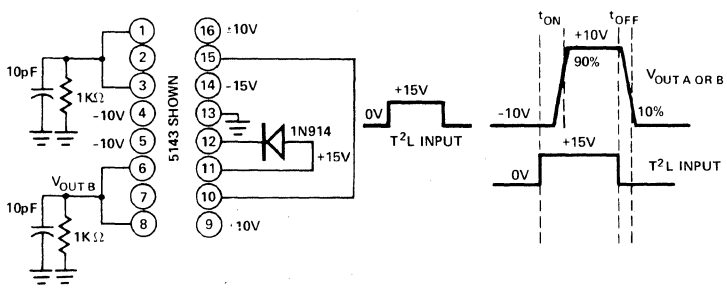


FIGURE 10.

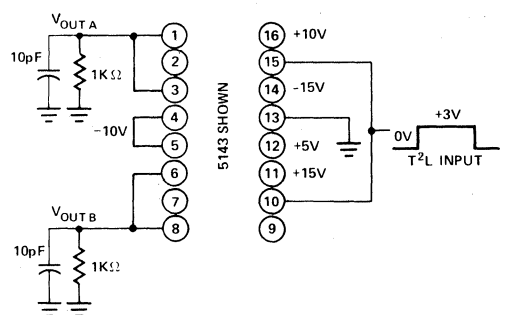


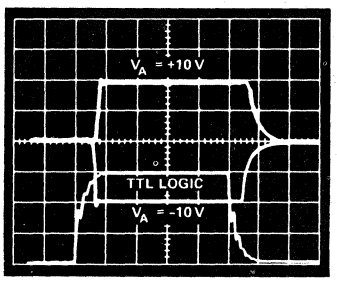
FIGURE 11.

AS-5140-AS-5145 Family

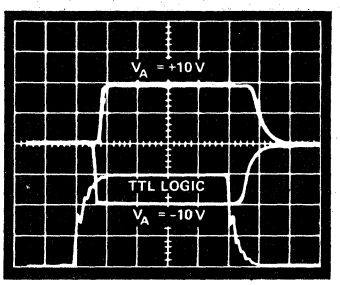
TYPICAL SWITCHING APPLICATIONS

SCALE: VERT. = 5V/DIV.
HORIZ. = 100ns/DIV.

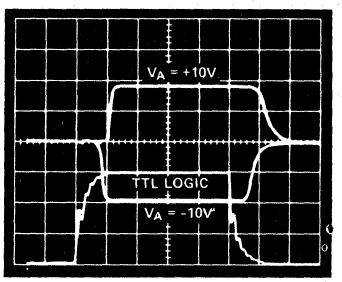
TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 8)



-55°C

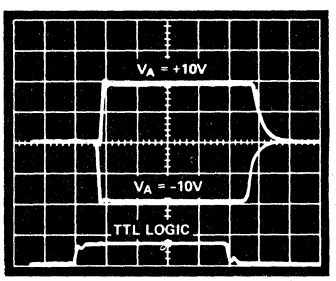


+25°C

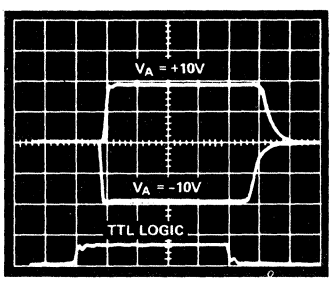


+125°C

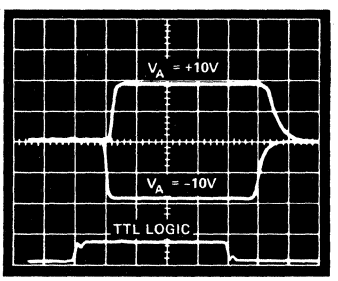
TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 9)



-55°C

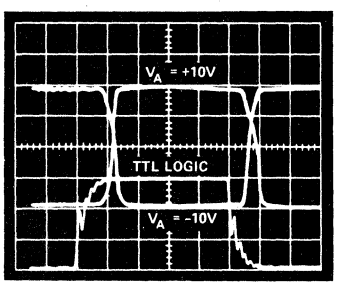


+25°C



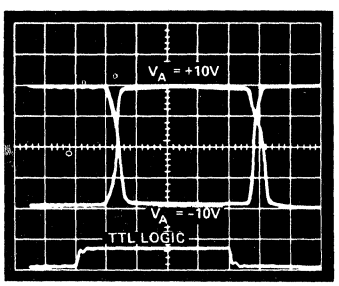
+125°C

TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 10)



+25°C

TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 11)



+25°C

APPLICATIONS

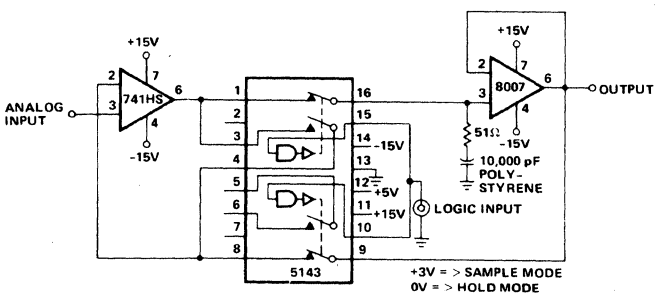
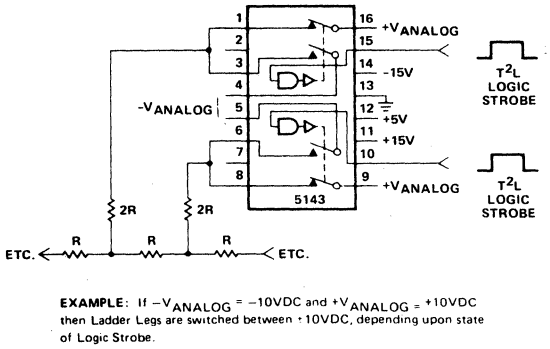
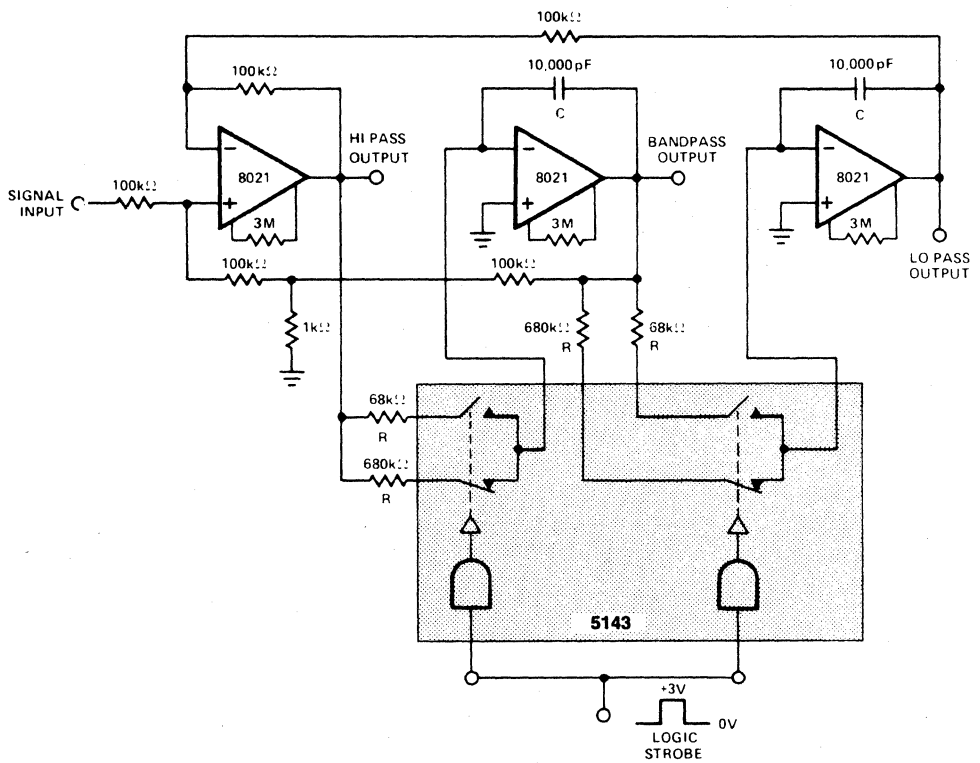


FIGURE 12. Improved Sample and Hold Using 5143



EXAMPLE: If $-V_{ANALOG} = -10VDC$ and $+V_{ANALOG} = +10VDC$ then Ladder Legs are switched between +10VDC, depending upon state of Logic Strobe.

FIGURE 13. Using the CMOS Switch to Drive an R/2R Ladder Network (2 Legs)



CONSTANT GAIN, CONSTANT Q, VARIABLE FREQUENCY FILTER WHICH PROVIDES SIMULTANEOUS LOWPASS, BANDPASS, AND HIGHPASS OUTPUTS. WITH THE COMPONENT VALUES SHOWN, CENTER FREQUENCY WILL BE 235Hz AND 23.5Hz FOR HIGH AND LOW LOGIC INPUTS RESPECTIVELY, Q = 100, AND GAIN = 100.

$$f_n = \text{CENTER FREQUENCY} = \frac{1}{2\pi RC}$$

FIGURE 14. Digitally Tuned Low Power Active Filter.

AS-5140-AS-5145 Family

APPLICATION NOTE

To maximize switching speed on the 5140 family use TTL open collector logic (15V with a 1K or less collector resistor). For SPST switches, typical $t_{on} \approx 80ns$ and typical $t_{off} \approx 50ns$ for signals in range of -10V to +10V with this high level drive configuration. The SPDT and DPST switches are approximately 30ns slower in both t_{on} and t_{off} with the same drive configuration. 15V CMOS logic levels can be used (0V to +15V), but propagation delays in the CMOS logic will slow down the switching (typical 50ns → 100ns delays).

When driving the 5140 Family from either +5V TTL or CMOS logic, switching times run 20ns slower than if they were driven from +15V logic levels. Thus $t_{on} \approx$ 105ns typical, and $t_{off} \approx$ 75ns typical for SPST switches and 135ns typical and 105ns typical (t_{on}, t_{off}) for SPDT or DPST switches. The low level drive can be made as fast as the high level drive if ±5V strobe levels are used instead of the usual 0V→+3.0V drive. Pin 13 is taken to -5V instead of the usual GND and strobe input is taken from +5V to -5V levels as shown in Figure 15.

The typical channel of the 5140 family consists of an N-channel MOS-FET. The N-channel MOS-FET uses a "Body Puller" FET to drive the body to -15V (±15V supplies) to get good breakdown voltages when the switch is in the off state (See Fig. 16). This "Body Puller" FET also allows the N-channel body to electrically float when the switch is in the on state producing a fairly constant $R_{DS(ON)}$ with different signal voltages. While this "Body Puller" FET improves switch performance, it can cause a problem when analog input signals are present (negative signals only) and power supplies are off. This fault condition is shown in Figure 17.

Current will flow from -10V analog voltage through the drain to body junction of Q1, then through the drain to body junction of Q3 to GND. This means that there is 10V across two forward-biased silicon diodes and current will go to whatever value the input signal source is capable of supplying. If the analog input signal is derived from the same supplies as the switch this fault condition cannot occur. Turning off the supplies would turn off the analog signal at the same time.

This fault situation can also be eliminated by placing a diode in series with the negative supply line (pin 14) as shown in Figure 18. Now when the power supplies are off and a negative input signal is present this diode is reverse biased and no current can flow.

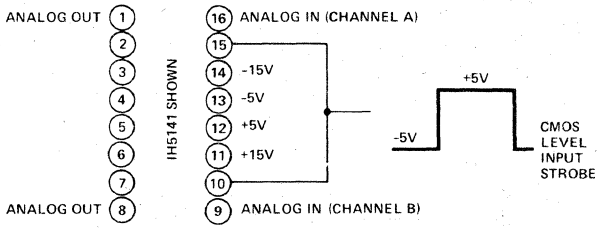


FIGURE 15.

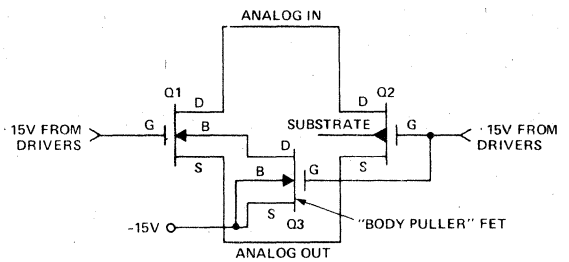


FIGURE 16.

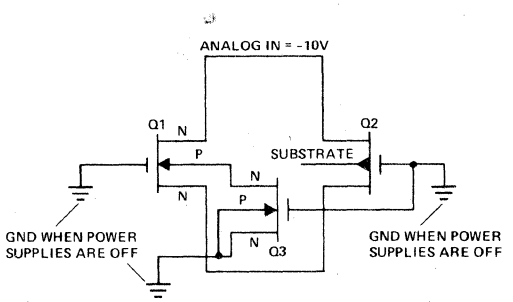


FIGURE 17.

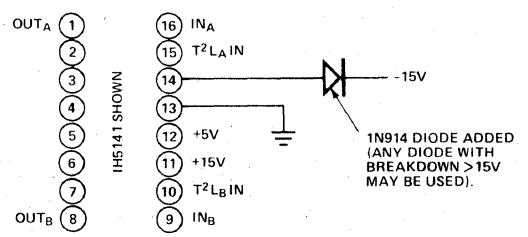
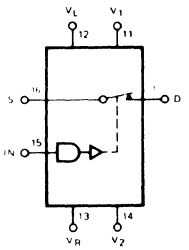


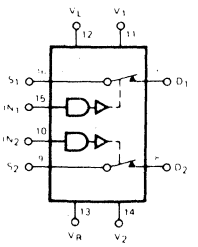
FIGURE 18.

AS-5140-AS-5145 Family

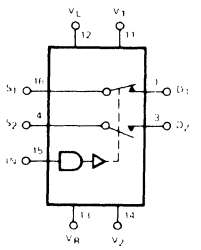
SWITCHING STATE DIAGRAMS SWITCH STATES ARE FOR LOGIC "1" INPUT



SPST
5140 (R_{DS} (ON) <75Ω)

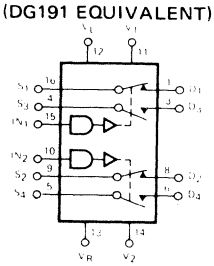


DUAL SPST
5141 (R_{DS} (ON) <75Ω)

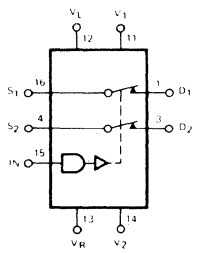


SPDT
5142 (R_{DS}(ON) < 75Ω)

(DG191 EQUIVALENT)

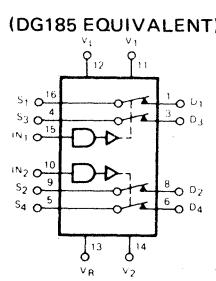


DUAL SPDT
5143 (R_{DS} (ON) <75Ω)



DPST
5144 (R_{DS} (ON) <75Ω)

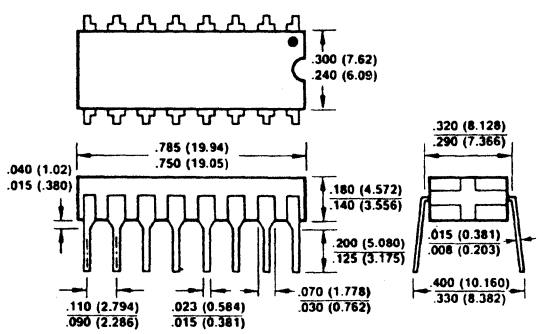
(DG185 EQUIVALENT)



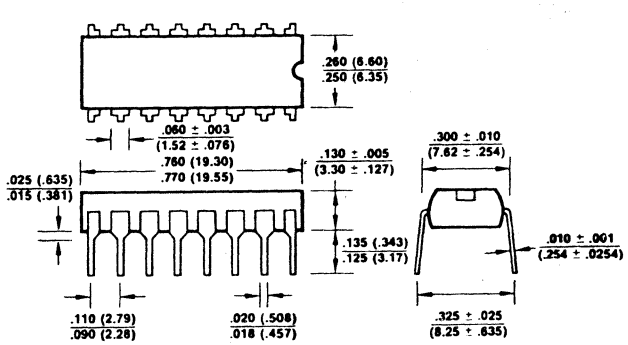
DUAL DPST
5145 (R_{DS} (ON) <75Ω)

PACKAGE DIMENSIONS

16 PIN CERDIP



16 PIN PLASTIC DIP



1. Lead no. 1 identified by dot or notch. 2. Dimensions in inches (millimeters).

Counters, Display Drivers

Quick Selection: Counters And Display Drivers

MODEL	DESCRIPTION	PACKAGE	OPER. TEMP. RANGE (°C)	PRICE (1-24)	SEE PAGE
CD-7216AC	Eight Digit Universal Counter Drives Seven Segment LED Display, Measures Frequency, Period, Freq. Ratio, Time Interval or Units	28 Pin Cerdip	-20 to +70	**$32.13**	466C
CD-7216BC		28 Pin Plastic DIP	-20 to +70	**$26.80**	
CD-7216CC		28 Pin Cerdip	-20 to +70	**$26.78**	
CD-7216DC		28 Pin Plastic DIP	-20 to +70	**$21.55**	
CD-7217C	Four Digit CMOS Up/Down Counter Drives Seven Segment LED Display. Pre-settable Start/ Count and Compare Register. Thumb-wheel Switch Controlled.	28 Pin Cerdip	-20 to +70	**$12.53**	481C
CD-7217AC		28 Pin Plastic DIP	-20 to +70	**$11.40**	
CD-7217BC		28 Pin Cerdip	-20 to +70	**$12.53**	
CD-7217CC		28 Pin Plastic DIP	-20 to +70	**$10.50**	
CD-7224C	4½ Digit High Speed Counter/ Decoder/Driver, 25 MHz Typ., for LCD Application	40 Pin Plastic DIP	-20 to +70	**$11.47**	493C
CD-7224AC			-20 to +70	**$11.47**	
CD-7225C	4½ Digit High Speed Counter/ Decoder/Driver, 25 MHz Typ., for LED Displays	40 Pin Plastic DIP	-20 to +70	**$ 8.77**	493C
CD-7225AC			-20 to +70	**$ 8.77**	
CD-7226AC	8 Digit Universal Counter Drives 7 Seg. LED Displays. Counts Freq., Period, Units.	40 Pin Cerdip	-20 to +70	**$32.00**	501C
CD-7226BC		40 Pin Plastic DIP	-20 to +70	**$26.87**	

MODEL	DESCRIPTION	PACKAGE	OPER. TEMP. RANGE (°C)	PRICE (1-24)	SEE PAGE
CD-7227C	Four Digit CMOS Up/Down Counter Drives Seven Segment LED Display. Pre-settable Start/Count and Compare Register. μP Controlled. Applications.	28 Pin Cerdip	-20 to +70	**$14.58**	481C
CD-7227AC		28 Pin Plastic DIP	-20 to +70	**$12.55**	
CD-7227BC		28 Pin Cerdip	-20 to +70	**$14.58**	
CD-7227CC		28 Pin Plastic DIP	-20 to +70	**$12.55**	
DD-7211C	Four Digit Display Decoder Drivers for LCD Applications. BCD Input, Hexadecimal Code B Output. Simplifies Alphanumeric Displays for μPs.	40 Pin Plastic DIP	-20 to +70	**$ 8.62**	513C
DD-7211AC			-20 to +70	**$ 6.22**	
DD-7211AMC			-20 to +70	**$ 6.22**	
DD-7211MC			-20 to +70	**$ 8.62**	
DD-7212C	Four Digit Display Decoder Drivers for LED Displays. BCD Input, Hexadecimal Code B Output. Simplifies Alpha-numeric Displays for μPs.	40 Pin Plastic DIP	-20 to +70	**$ 6.22**	513C
DD-7212AC			-20 to +70	**$ 6.22**	
DD-7212AMC			-20 to +70	**$ 6.22**	
DD-7212MC			-20 to +70	**4 6.22**	
DD-7218AC	LED Driver System for μPs. Features Digit and Segment Drivers, Multiplex Scan Circuitry, 8x8 Static Memory, Hexadecimal Code B Decoders, Hardwire Controllable Versions.	28 Pin Cerdip	-20 to +70	**$10.88**	523C
DD-7218BC		28 Pin Plastic DIP	-20 to +70	**$10.35**	
DD-7218CC		28 Pin Cerdip	-20 to +70	**$10.88**	
DD-7218DC		28 Pin Plastic DIP	-20 to +70	**$10.35**	
DD-7218EC		40 Pin Ceramic DIP	-20 to +70	**$14.45**	

DATEL INTERSIL

CD-7216A/B/C/D

CD-7216A 10 MHz Universal Counter, Drives Common Anode LED's
CD-7216B 10 MHz Universal Counter, Drives Common Cathode LED's
CD-7216C 10 MHz Frequency Counter, Drives Common Anode LED's
CD-7216D 10 MHz Frequency Counter, Drives Common Cathode LED's

FEATURES

CD-7216A AND B

- **Functions as a Frequency Counter, Period Counter, Unit Counter, Frequency Ratio Counter or Time Interval Counter**
- **Four Internal Gate Times: 0.01 sec, 0.1 sec, 1 sec, 10 sec in Frequency Counter Mode**
- **1 Cycle, 10 Cycles, 100 Cycles, 1000 Cycles in Period, Frequency Ratio and Time Interval Modes**
- **Measures Frequencies from DC to 10 MHz**
- **Measures Period from 0.5μ sec to 10 sec**

CD-7216C AND D

- **Functions as a Frequency Counter. Measures Frequencies from DC to 10 MHz**
- **Decimal Point and Leading Zero Blanking May be Externally Selected**

ALL VERSIONS:

- **Eight Digit Multiplexed LED Outputs**
- **Output Drivers will Directly Drive Both Digits and Segments of Large LED Displays. Both Common Anode and Common Cathode Versions are Available**
- **Single Nominal 5V Supply Required**
- **Stable High Frequency Oscillator, Uses Either 1 MHz or 10 MHz Crystal**
- **Internally Generated Multiplex Timing with Interdigit Blanking, Leading Zero Blanking and Overflow Indication**
- **Decimal Point and Leading Zero Blanking Controlled Directly by the Chip**
- **Display Off Mode Turns Off Display and Puts Chip into Low Power Mode**
- **Hold and $\overline{\text{Reset}}$ Inputs for Additional Flexibility**
- **Test Speedup Function Included**
- **All Terminals Protected Against Static Discharge**

GENERAL DESCRIPTION

The CD- 7216A and B are fully integrated Universal Counters with LED display drivers. They combine a high frequency oscillator, a decade timebase counter, an 8 decade data counter and latches, a 7 segment decoder, digit multiplexers and 8 segment and 8 digit drivers which can directly drive large LED displays. The counter inputs have a maximum frequency of 10 MHz in frequency and unit counter modes and 2 MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The CD- 7216A and B can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or as a totalizing counter. The counter uses either a 10 MHz or 1 MHz quartz crystal timebase. For period and time interval, the 10MHz timebase gives a 0.1 μsec resolution. In period average and time interval average, the resolution can be in the nanosecond range. In the frequency mode, the user can select accumulation times of 0.01 sec, 0.1 sec, 1 sec and 10 sec. With a 10 sec accumulation time, the frequency can be displayed to a resolution of 0.1 Hz in the least significant digit. There is 0.2 seconds between measurements in all ranges.

The CD-7216C and D function as frequency counters only, as described above.

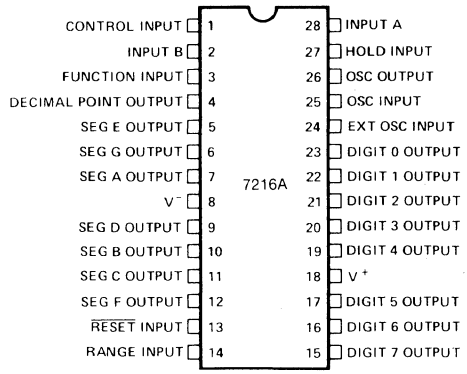
All versions of the CD-7216 incorporate leading zero blanking. Frequency is displayed in KHz. In the CD- 7216A and B, time is displayed in μsec. The display is multiplexed at 500Hz with a 12.5% duty cycle for each digit. The CD-7216A and C are designed for common anode display with typical peak segment currents of 25mA. The CD-7216B and D are designed for common cathode displays with typical peak segment currents of 12mA. In the display off mode, both digit drivers and segment drivers are turned off enabling the display to be used for other functions.

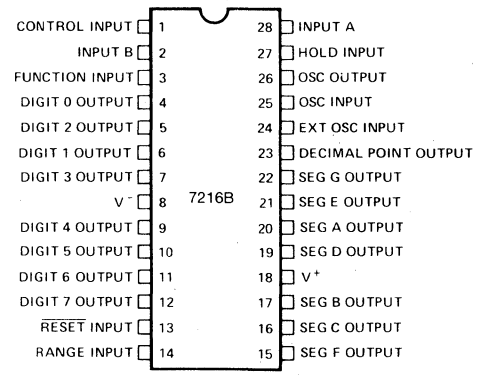
ORDERING INFORMATION

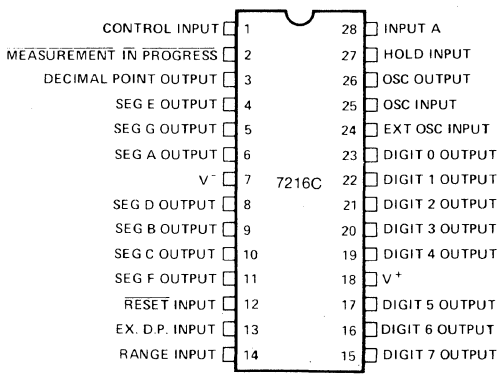
	MODEL	OPERATING TEMP. RANGE
Universal Counter for use with Common Anode LED Display:	**CD-7216 AC**	**−20° C to +70° C**
Universal Counter for use with Common Cathode LED Display:	**CD-7216 BC**	**−20° C to +70° C**
Frequency Counter for use with Common Anode LED Display:	**CD-7216 CC**	**−20° C to +70° C**
Frequency Counter for use with Common Cathode LED Display:	**CD-7216 DC**	**−20° C to +70° C**

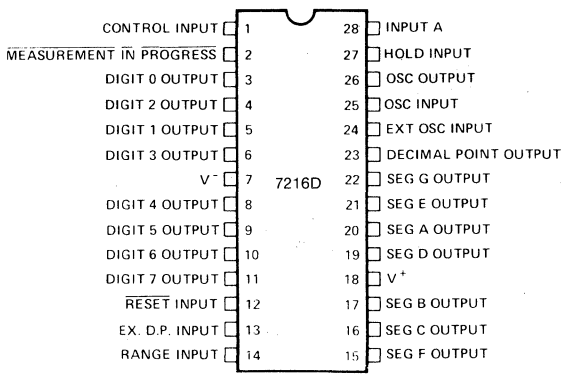
CD-7216

PIN CONFIGURATIONS









ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage ($V^+ - V^-$) ..... 6.5 Volts
Maximum Digit Output Current 400mA
Maximum Segment Output Current 60mA
Voltage On Any Input or
Output Terminal[1] ..... $V^+ + .3V$ to $V^- - .3V$
Maximum Power Dissipation at
70°C ..... 1.0 Watts (7216A & C)
0.5 Watts (7216B & D)
Maximum Operating Temperature
Range ..... −20°C to +70°C
Maximum Storage Temperature
Range ..... −55°C to +125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

Notes:

1. The 7216 may be triggered into a destructive latchup mode if either input signals are applied before the power supply is applied or if input or output are forced to voltages exceeding V^+ to V^- by more than 0.3 volts.

CD-7216

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: $V^+ - V^- = 5.0V$, Test Circuit, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
7216A/B						
Operating Supply Current	I_{DD}	Display Off, Unused Inputs to V^-		2	5	mA
Supply Voltage Range		-20°C < T_A < +70°C, Input A, Input B Frequency at F_{MAX}	4.75		6.0	Volts
Maximum Frequency Input A, Pin 28	$F_{A\ MAX}$	-20°C < T_A < +70°C 4.75 < $V^+ - V^-$ < 6.0V, Figure 1, Function = Frequency, Ratio, Unit Counter Function = Period, Time Interval	 10 2.5			 MHz MHz
Maximum Frequency Input B, Pin 2	F_{BMAX}	-20°C < T_A < +70°C 4.75V < $V^+ - V^-$ < 6.0V Figure 2	 2.5			 MHz
Minimum Separation Input A to Input B Time Interval Function		-20°C < T_A < 70°C 4.75V < $V^+ - V^-$ < 6.0V Figure 3	 250			 nsec
Maximum Osc. Freq. and Ext. Osc. Frequency		-20°C < T_A < +70°C 4.75 < $V^+ - V^-$ < 6.0V	 10			 MHz
Minimum Ext. Osc. Freq.					100	KHz
Oscillator Transconductance	g_m	$V^+ - V^-$ = 4.75V, T_A = +70°C	2000			μmhos
Multiplex Frequency	f_{mux}	f_{osc} = 10MHz		500		Hz
Time Between Measurements		f_{osc} = 10MHz		200		msec
Input Voltages: Pins 2,13,25,27,28 Input Low Voltage Input High Voltage	 V_{IL} V_{IH}	-20°C < T_A < +70°C	 3.5		 1.0	 Volts Volts
Input Resistance to V^+ Pins 13,24	R	$V_{IN} = V^+ - 1.0V$	100K	400K		ohms
Input Leakage Pin 27,28,2	I_L				20	μA
7216A						
Digit Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Low Output Current	 I_{OH} I_{OL}	 $V_{OUT} = V^+ - 2.0V$ $V_{OUT} = V^- + 1.0V$	 -150	 -180 +0.3		 mA mA
Segment Driver: Pins 4,5,6,7,9,10,11,12 Low Output Current High Output Current	 I_{OL} I_{OH}	 $V_{OUT} = V^- + 1.5V$ $V_{OUT} = V^+ - 2.5V$	 25	 35 -100		 mA μA
Multiplex Inputs: Pins 1,3,14 Input Low Voltage Input High Voltage Input Resistance to V^-	 V_{IL} V_{IH} R	 $V_{IN} = V^- + 1.0V$	 $V^- + 2.0$ 50	 100	 0.8	 Volts Volts KΩ
7216B						
Digit Driver: Pins 4,5,6,7,9,10,11,12 Low Output Current High Output Current	 I_{OL} I_{OH}	 $V_{OUT} = V^- + 1.0V$ $V_{OUT} = V^+ - 2.5V$	 50	 75 -100		 mA μA
Segment Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Leakage Current	 I_{OH} I_L	 $V_{OUT} = V^+ - 2.0V$ $V_{OUT} = V^+ - 2.5V$	 -10	 	 10	 mA μA
Multiplex Inputs: Pins 1,3,14 Input Low Voltage Input High Voltage Input Resistance to V^+	 V_{IL} V_{IH} R	 $V_{IN} = V^+ - 1.0V$	 $V^+ - 0.8$ 200	 360	 $V^+ - 2.0$	 Volts Volts KΩ

CD-7216

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: $V^+ - V^- = 5.0V$, Test Circuit, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
7216C/D						
Operating Supply Current	I_{DD}	Display Off, Unused Inputs to V^-		2	5	mA
Supply Voltage Range		$-20°C \leq T_A \leq +70°C$, Input A Frequency at F_{MAX}	4.75		6.0	Volts
Maximum Frequency Input A, Pin 28	F_{MAX}	$-20°C \leq T_A \leq +70°C$ $4.75 \leq V^+ - V^- \leq 6.0V$, Figure 1	10			MHz
Maximum Osc. Freq and Ext. Osc. Frequency		$-20°C \leq T_A \leq +70°C$ $4.75 \leq V^+ - V^- \leq 6.0V$	10			MHz
Minimum Ext. Osc. Freq.					100	KHz
Oscillator Transconductance	g_m	$V^+ - V^- = 4.75V$, $T_A = +70°C$	2000			μmhos
Multiplex Frequency	f_{mux}	$f_{osc} = 10MHz$		500		Hz
Time Between Measurements		$f_{osc} = 10MHz$		200		msec
Input Voltages: Pins 12,27,28 Input Low Voltage Input High Voltage	V_{IL} V_{IH}	$-20°C \leq T_A \leq +70°C$	3.5		1.0	Volts Volts
Input Resistance to V^+ Pins 12,24	R	$V_{IN} = V^+ - 1.0V$	100	400		KΩ
Input Leakage Pin 27, Pin 28	I_L				20	μA
Output Current Pin 2	I_{OL}	$V_{OL} = V^- + .4V$	0.36			mA
	I_{OH}	$V_{OH} = V^+ - .8V$	265			μA
7216C						
Digit Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Low Output Current	I_{OH} I_{OL}	$V_{OUT} = V^+ - 2.0V$ $V_{OUT} = 1.0V$	-150	-180 +0.3		mA mA
Segment Driver: Pins 3,4,5,6,8,9,10,11 Low Output Current High Output Current	I_{OL} I_{OH}	$V_{OUT} = V^- + 1.5V$ $V_{OUT} = V^+ - 2.5V$	25	30 -100		mA μA
Multiplex Inputs: Pins 1,13,14 Input Low Voltage Input High Voltage Input Resistance to V^-	V_{IL} V_{IH} R	$V_{IN} = V^- + 1.0V$	$V^- + 2.0$ 50	100	$V^- + 0.8$	Volts Volts KΩ
7216D						
Digit Driver: Pins 3,4,5,6,8,9,10,11 Low Output Current High Output Current	I_{OL} I_{OH}	$V_{OUT} = V^- + 2.0V$ $V_{OUT} = V^+ - 2.5V$	50	75 100		mA μA
Segment Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Leakage Current	I_{OH} I_L	$V_{OUT} = V^+ - 2.0V$ $V_{OUT} = V^+ - 2.5V$	10	15	10	mA μA
Multiplex Inputs: Pins 1,13,14 Input Low Voltage Input High Voltage Input Resistance to V^+	V_{IL} V_{IH}	$V_{IN} = V^+ - 1.0V$	$V^+ - 0.8$ 200	360	$V^+ - 2.0$	Volts Volts kΩ

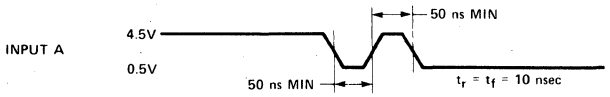


FIGURE 1. Waveform for Guaranteed Minimum FAMAX Function = Frequency, Frequency Ratio, Unit Counter.

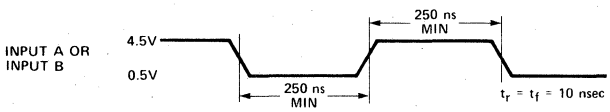


FIGURE 2. Waveform for Guaranteed Minimum FBMAX and FAMAX for Function = Period and Time Interval.

TIME INTERVAL MEASUREMENT

The CD-7216/7226 can be used to accurately measure the time interval between two events. With a 10 MHz timebase crystal, the time between the two events can be as long as ten seconds. Accurate resolution in time interval measurement is 100ns.

The feature operates with Channel A going low at the start of the event to be measured, followed by Channel B going low at the end of the event.

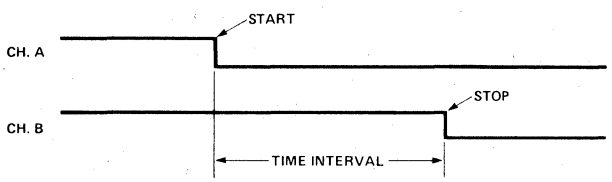


FIGURE 3a.

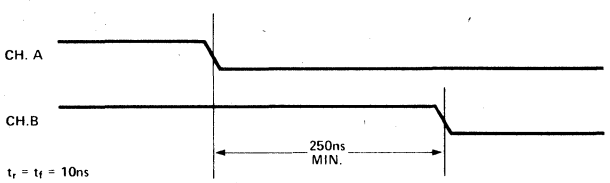


FIGURE 3b. Waveform for Minimum Time Between Transitions of Input A and Input B.

When in the time interval mode and measuring a single event, the CD-7216/7226 must first be "primed" prior to measuring the event of interest. This is done by placing both Channel A and Channel B at V^+, then causing A to toggle to V^- and back to V^+ followed by B toggling to V^- and back to V^+ The input is then ready for measurement.

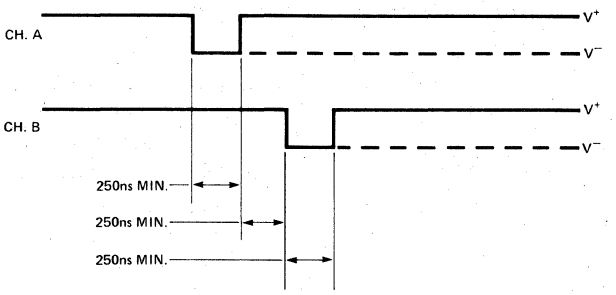
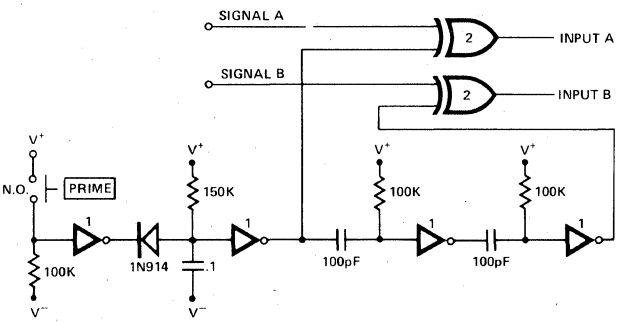


FIGURE 3c.

This can be easily accomplished with the following circuit: (Figure 3d)



Device	Type
1	CD4049B Inverting Buffer
2	CD4070B Exclusive-OR

FIGURE 3d. Priming Circuit, Signal A&B High or Low.

Following the priming procedure (when in single event or 1 cycle range input) the device is ready to measure one (only) event.

When timing repetitive signals, it is not necessary to "prime" the CD-7216/7226 as the first alternating signal states automatically prime the device.

During any time interval measurement cycle, the CD-7216/7226 requires 200ms following B going low to update all internal logic. A new measurement cycle will not take place until completion of this internal update time.

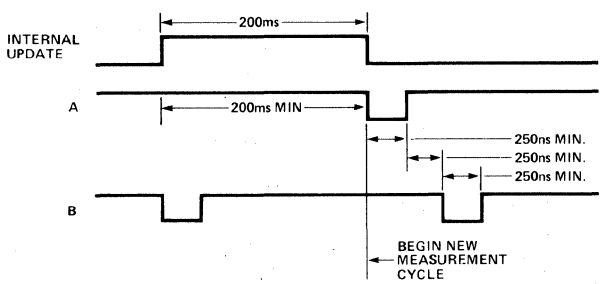
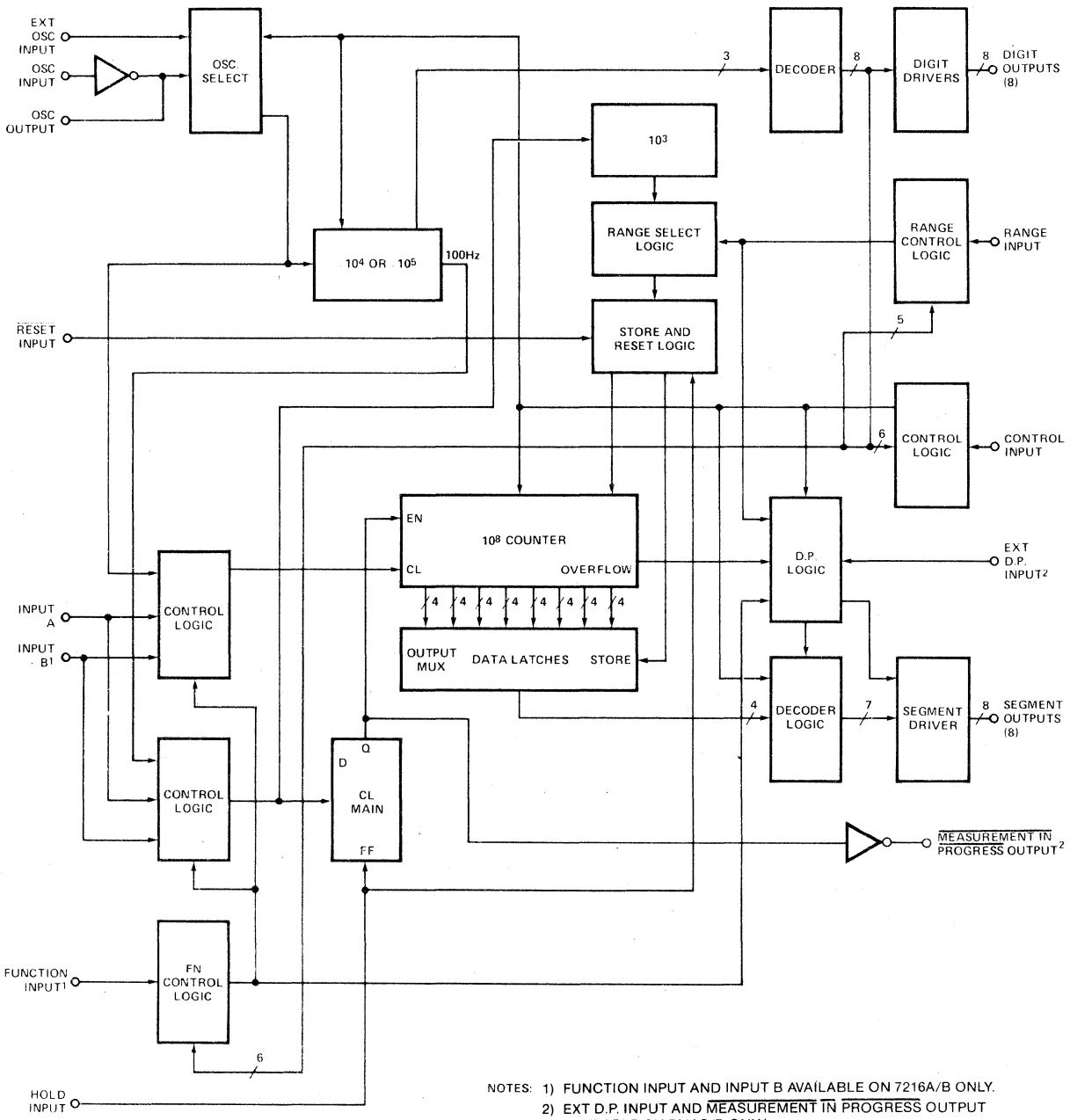
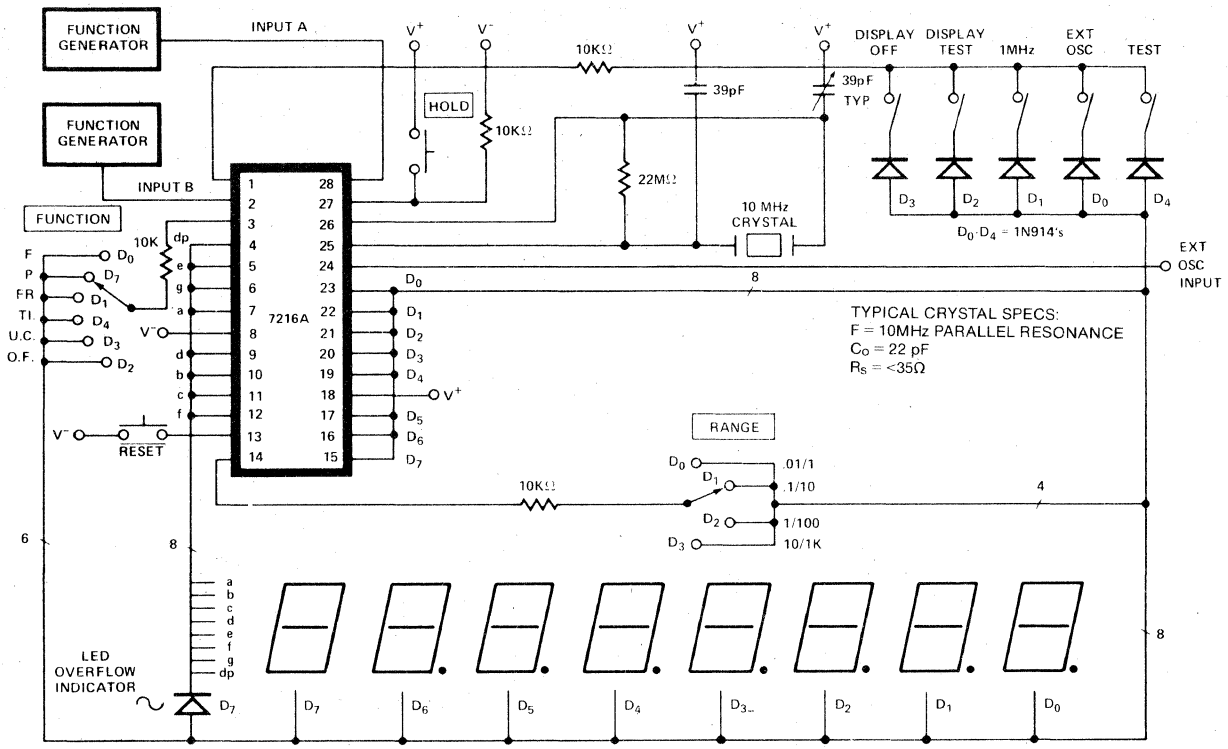


FIGURE 3e.



NOTES: 1) FUNCTION INPUT AND INPUT B AVAILABLE ON 7216A/B ONLY.
2) EXT D.P. INPUT AND MEASUREMENT IN PROGRESS OUTPUT AVAILABLE ON 7216C/D ONLY.

BLOCK DIAGRAM



TEST CIRCUIT

OVERFLOW WILL BE INDICATED ON THE DECIMAL POINT OUTPUT OF DIGIT 7.

LED OVERFLOW INDICATOR CONNECTIONS

	CATHODE	ANODE
CD-7216AC	DEC. PT.	D_7
CD-7216BC	D_7	DEC. PT.
CD-7216CC	DEC. PT.	D_7
CD-7216DC	D_7	DEC. PT.

APPLICATIONS NOTES

GENERAL

Inputs A and B

Inputs A and B are digital inputs with a typical switching threshold of 2.0V at $V^+ = 5.0V$. For optimum performance the peak-to-peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from T^2L logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs.

Note: The amplitude of the input should not exceed the supply, otherwise, the circuit may be damaged.

Multiplexed Inputs

The function, range, control and external decimal point inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate digit driver output to the inputs. The input function, range and control inputs must be stable during the last half of each digit output, (typically 125μsec). The multiplex inputs are active high for the common anode CD-7216A and C and active low for the common cathode CD-7216B and D.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the unit counter mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10K resistor should be placed in series with the multiplex inputs as shown in the application notes.

Table 1 shows the functions selected by each digit for these inputs.

Control Input Functions

Display Test — All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be blanked if Display Off is selected at the same time.

Display Off — To enable the Display Off mode it is necessary to input D_3 to the control input and have the HOLD input at V^+. The chip will remain in the Display Off mode until HOLD is switched back to V^-. While in the Display Off mode, the segment and digit driver outputs are open. During Display Off the oscillator continues to run with a typical supply current of 1.5mA with a 10 MHz crystal and no measurements are made. In addition, inputs to the multiplexed inputs will have no effect. A new measurement is initiated when the HOLD input is switched to V^-.

1 MHz Select — The 1 MHz select mode allows use of a 1 MHz crystal with the same digit multiplex rate and time between measurements as with a 10 MHz crystal. The decimal point is also shifted one digit to the right in Period and Time Interval, since the least significant digit will be in μsecond increments rather than 0.1 μsec increments.

External Oscillator Enable — In this mode the external oscillator input is used instead of the on-chip oscillator for Timebase input and Main Counter input in Period and Time interval modes. The on-chip oscillator will continue to function when the external oscillator is selected. The external oscillator input frequency must be greater than 100 KHz or the chip will reset itself to enable the on-chip oscillator.

TABLE 1

	FUNCTION	DIGIT
Function Input Pin 3 (CD-7216A & B Only)	Frequency	D_0
	Period	D_7
	Frequency Ratio	D_1
	Time Interval	D_4
	Unit Counter	D_3
	Oscillator Frequency	D_2
Range Input Pin 14	.01 sec/1 Cycle	D_0
	.1 sec/10 Cycles	D_1
	1 sec/100 Cycles	D_2
	10 sec/1K Cycles	D_3
Control Input Pin 1	Blank Display	D_3 and Hold
	Display Test	D_7
	1 MHz Select	D_1
	External Oscillator Enable	D_0
	External Decimal Point Enable	D_2
	Test	D_4
External Decimal Point Input Pin 13, CD-7216C & D Only	Decimal point is output for same digit that is connected to this input	

External Decimal Point Enable — When external decimal point is enabled a decimal point will be displayed whenever the digit driver connected to the external decimal point is active. Leading Zero Blanking will be disabled for all digits following the decimal point.

Test Mode — In the test mode the main counter is split into groups of two digits each and the groups are clocked in parallel. The reference counter is split such that the clock into the reference count goes directly to the clock of the second decade counter (.1 sec/10 cycle range). The count in the main counter is continuously output.

Range Input — The range input selects whether the measurement is made for 1, 10 , 100, 1000 counts of the reference counter. In all functional modes except Unit Counter a change in the range input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the Range Input is changed.

Function Input — The six functions that can be selected are: Frequency, Period, Time Interval, Unit Counter, Frequency Ratio and Oscillator Frequency. This Input is available on the CD-7216A and B only.

These functions select which signal is counted into the Main Counter and which signal is counted by the reference counter, as shown in Table 2. In Time Interval, a flip flop is toggled first by a 1-0 transition of Input A and then by a 1-0 transition of Input B. The oscillator is gated into the Main Counter from the time Input A toggles the flip flop until Input B gates the flip flop. A change in the function input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the Function Input is changed.

TABLE 2

DESCRIPTION	MAIN COUNTER	REFERENCE COUNTER
Frequency (F_A)	Input A	100 Hz (Oscillator ÷ 10^5 or 10^4)
Period (T_A)	Oscillator	Input A
Ratio (F_A/F_B)	Input A	Input B
Time Interval (A → B)	Oscillator (Time Interval FF)	Time Interval FF
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq. (F_{osc})	Oscillator	100 Hz (Oscillator ÷ 10^5 or 10^4)

External Decimal Point Input — When the external decimal point is selected this input is active. Any of the digits, except D_7, can be connected to this point. D_7 should not be used since it will override the overflow output and leading zeros will remain unblanked after the decimal point. This input is available on the CD-7216C and D only.

Hold Input — When the Hold Input is at V^+, any measurement in progress is stopped, the main counter is reset and the chip is held ready to initiate a new measurement. The latches which hold the main counter data are not updated so the last complete measurement is displayed. When Hold is changed to V^-, a new measurement is initiated.

$\overline{\text{Reset}}$ Input — The $\overline{\text{Reset}}$ Input is the same as a Hold Input, except the latches for the Main Counter are enabled, resulting in an output of all zeros.

DISPLAY CONSIDERATIONS

The display is multiplexed at a 500 Hz rate with a digit time of 244 μsec. An interdigit blanking time of 6 μsec is used to prevent ghosting between digits. The decimal point and leading zero blanking have been implemented for right hand decimal point displays, zeros following the decimal point will not be blanked. Also, the leading zero blanking will be disabled when the Main Counter overflows.

The CD-7216A and C are designed to drive common anode LED displays at peak current of 25mA/segment, using displays with $V_F = 1.8$ V at 25mA. The average DC current will be over 3mA under these conditions. The CD-7216B and D are designed to drive common cathode displays at peak current of 15mA/segment using displays with $V_F = 1.8$V at 15mA. Resistors can be added in series with the segment drivers to limit the display current in very efficient displays, if required. Figures 4,5,6 and 7 show the digit and segment currents as a function of output voltage.

To get additional brightness out of the displays, V^+ may be increased up to 6.0V. However, care should be taken to see that maximum power and current ratings are not exceeded.

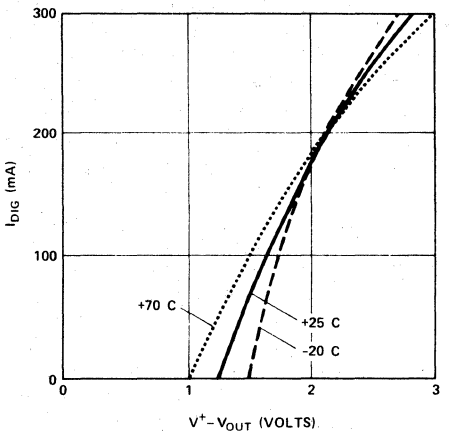
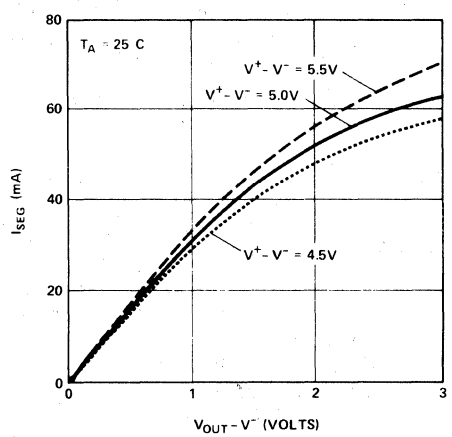


FIGURE 4. CD-7216A & C Typical I_{DIG} vs. $V^+ - V_{OUT}$, $4.5V \leq V^+ - V^- \leq 6.0V$



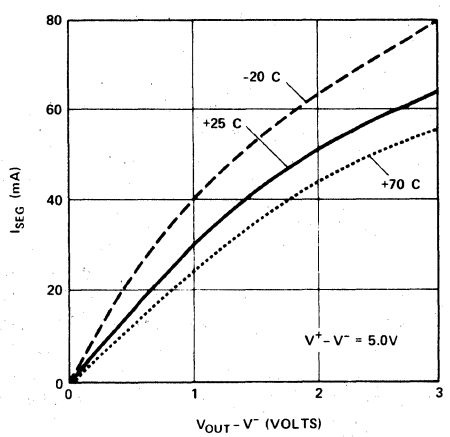


FIGURE 5. CD-7216A & C Typical I_{SEG} vs. $V_{OUT} - V^-$

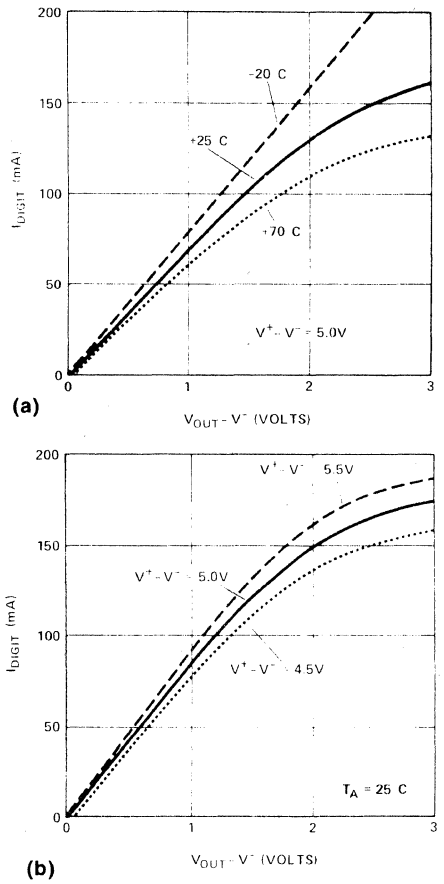


FIGURE 6. CD-7216B & D Typical I_{DIGIT} vs. $V_{OUT} - V^-$

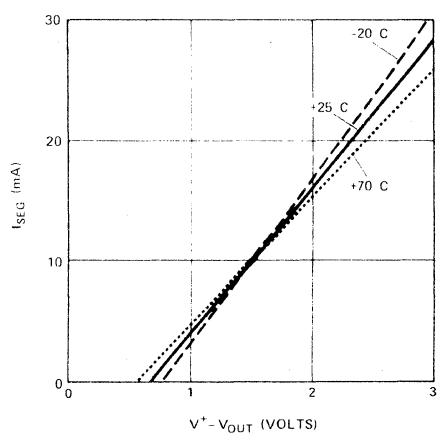
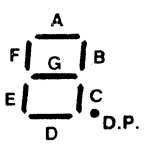


FIGURE 7. CD-7216B & D Typical I_{SEG} vs. $V^+ - V_{OUT}$, $4.5V \leq V^+ - V^- \leq 6.0V$

The segment and digit outputs in CD-7216's are not directly compatible with either TTL or CMOS logic. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals.

Segment Identification:



ACCURACY

In a Universal Counter crystal drift and quantization errors cause errors. In Frequency, Period and Time Interval modes, a signal derived from the oscillator is used in either the Reference Counter or Main Counter. Therefore, in these modes an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppM/°C will cause a measurement error of 20ppM/°C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the Frequency mode the maximum accuracy is obtained with high frequency inputs and in Period mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 8, the least accuracy will be obtained at 10 KHz. In Time Interval measurements there can be an error of 1 count per interval. As a result there is the same inherent accuracy in all ranges as shown in Figure 9. In Frequency Ratio measurement can be more accurately obtained by averaging over more cycles of Input B as shown in Figure 10.

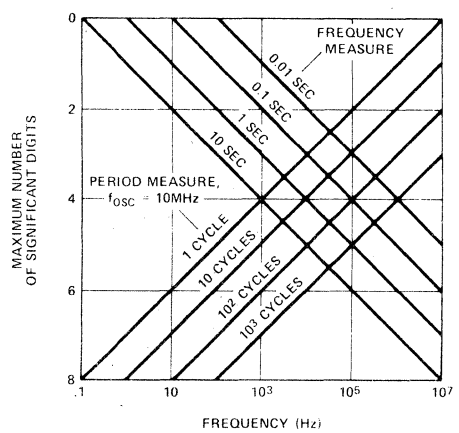


FIGURE 8. Maximum Accuracy of Frequency and Period Measurements Due to Limitations of Quantization Errors

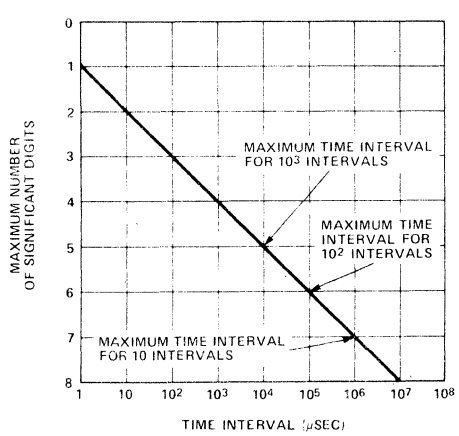


FIGURE 9. Maximum Accuracy of Time Interval Measurement Due to Limitations of Quantization Errors

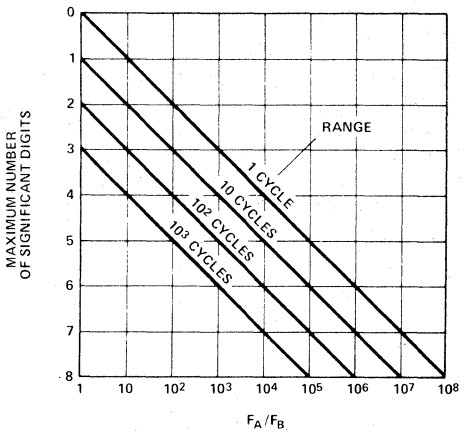


FIGURE 10. Maximum Accuracy for Frequency Ratio Measurement Due to Limitation of Quantization Errors

CIRCUIT APPLICATIONS

The CD-7216 has been designed for use in a wide range of Universal and Frequency counters. In many cases, prescalers will be required to reduce the input frequencies to under 10 MHz. Because Input A and Input B are digital inputs, additional circuitry is often required for input buffering, amplification, hysterisis, and level shifting to obtain a good digital signal.

The CD-7216A or B can be used as a minimum component complete Universal Counter as shown in Figure 11. This circuit can use input frequencies up to 10 MHz at Input A and 2 MHz at Input B.

For input frequencies up to 40 MHz the circuit shown in Figure 12 can be used to implement a frequency counter. To obtain the correct measured value, it is necessary to divide the oscillator frequency by four as well as the input frequency. In doing this the time between measurements is also lengthened to 800 msec and the display multiplex rate is decreased to 125 Hz.

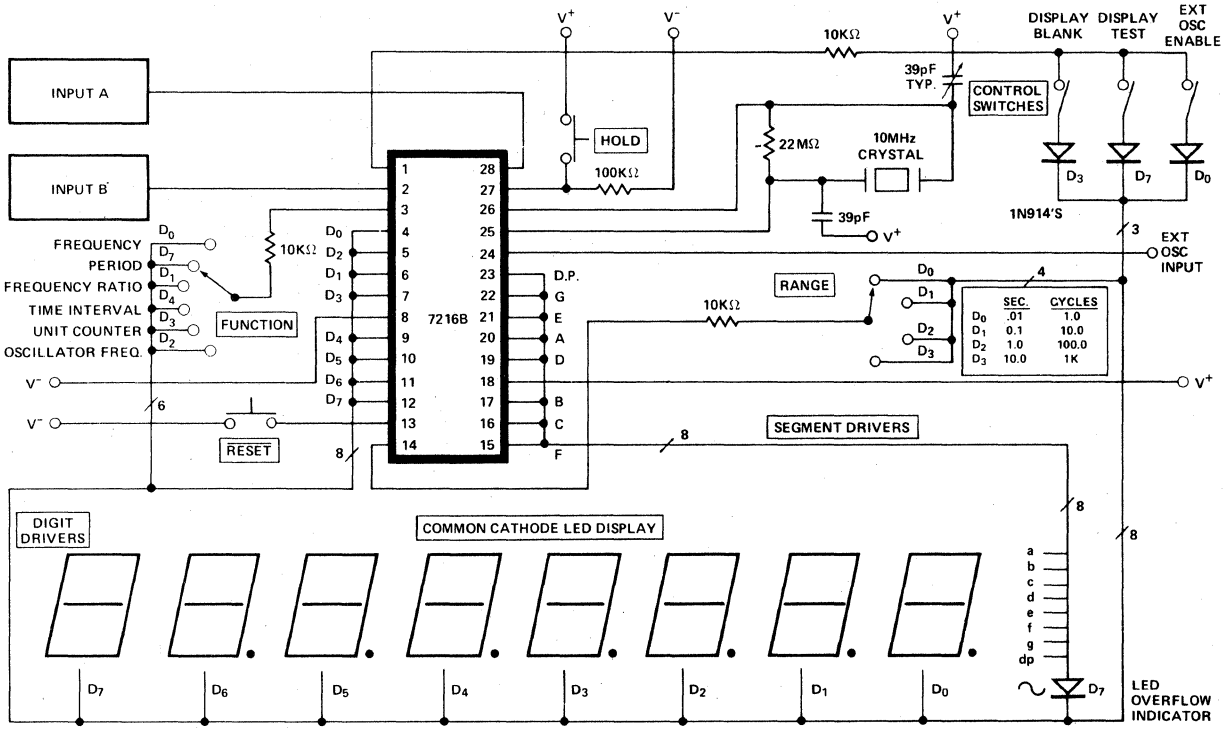


FIGURE 11. 10MHz Universal Counter

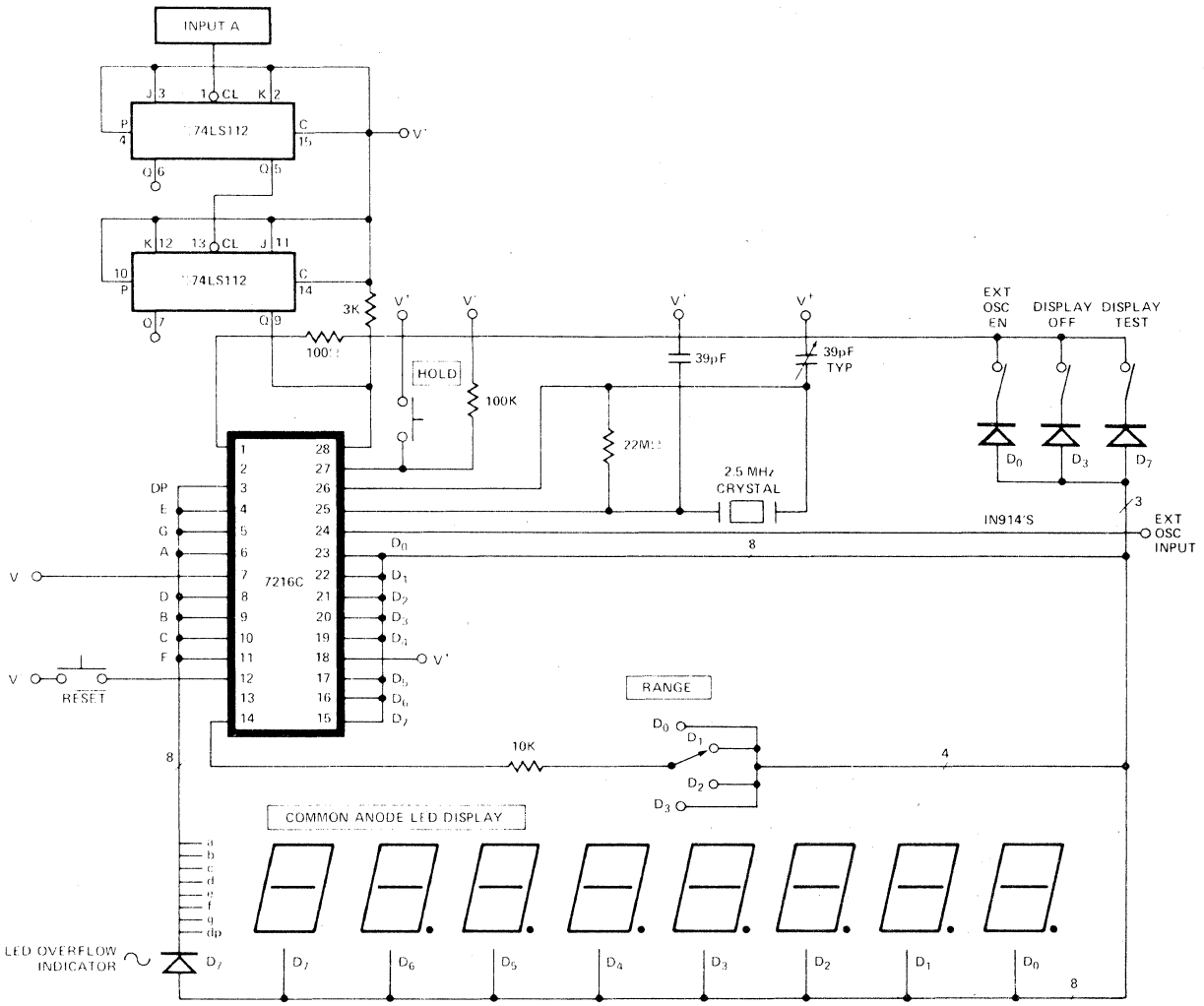


FIGURE 12. 40MHz Frequency Counter

If the input frequency is prescaled by ten, then the oscillator can remain at 10 or 1 MHz, but the decimal point must be moved one digit to the right. Figure 13 shows a frequency counter implemented with a ÷10 prescaler and an CD-7216C. Since there is no external decimal point with the CD-7216A or B, the decimal point must be implemented with additional drivers as shown in Figure 14. Note that there can be one zero to the left of the decimal point since the internal leading zero blanking cannot be changed. In Figure 15 additional logic has been added to count the input directly in period mode for maximum accuracy. In both Figures 13 and 14, Input A comes from Q_C of the prescaler rather than Q_A to obtain an input duty cycle of 40%. If the signal at Input A has a very low duty cycle then it may be necessary to use a 74121 monostable multivibrator or similar circuit to stretch the input pulse width to guarantee 50 nsec minimum pulse width.

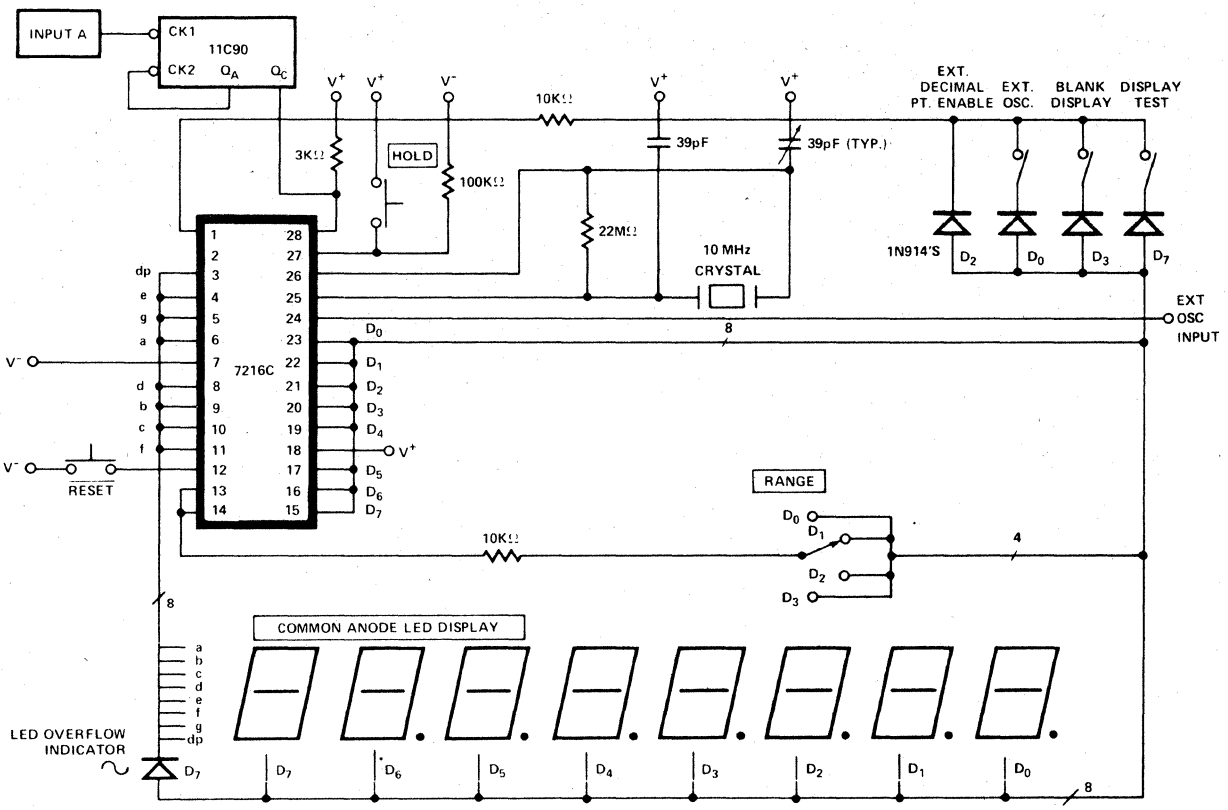


FIGURE 13. 100MHz Frequency Counter

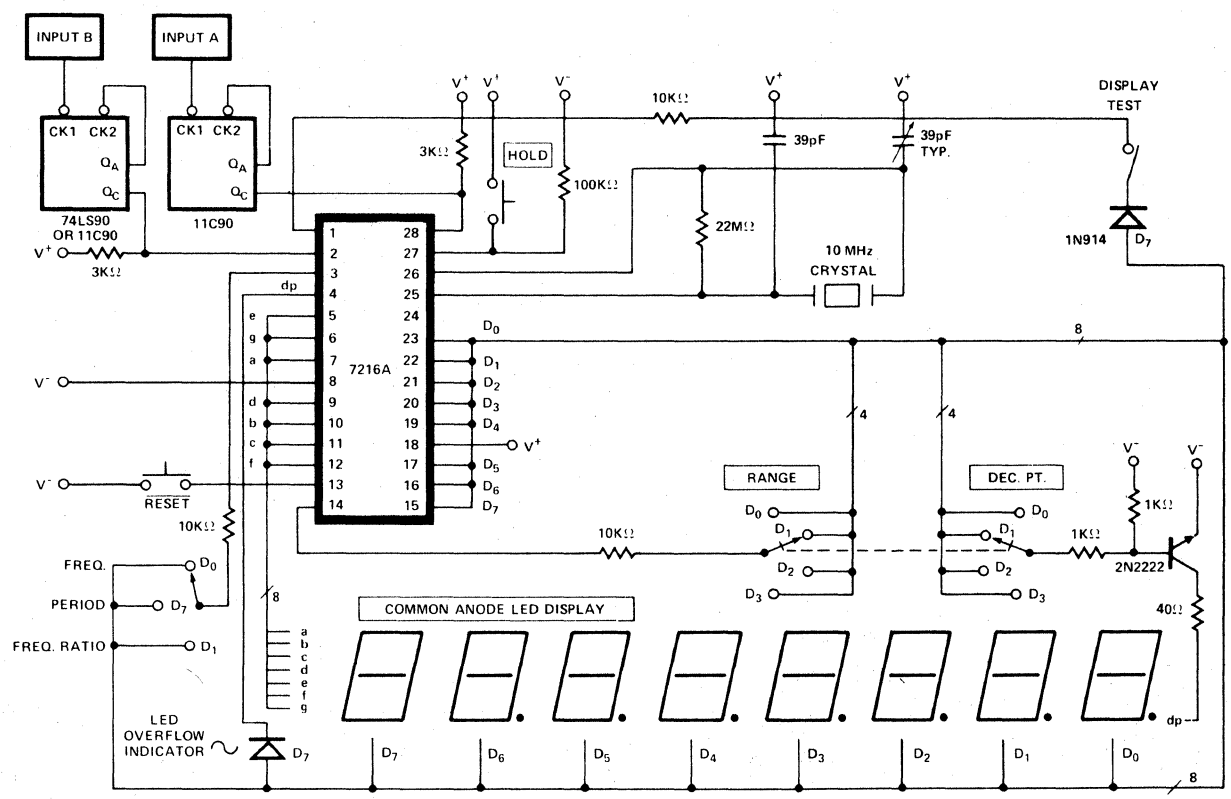


FIGURE 14. 100MHz Multifunction Counter

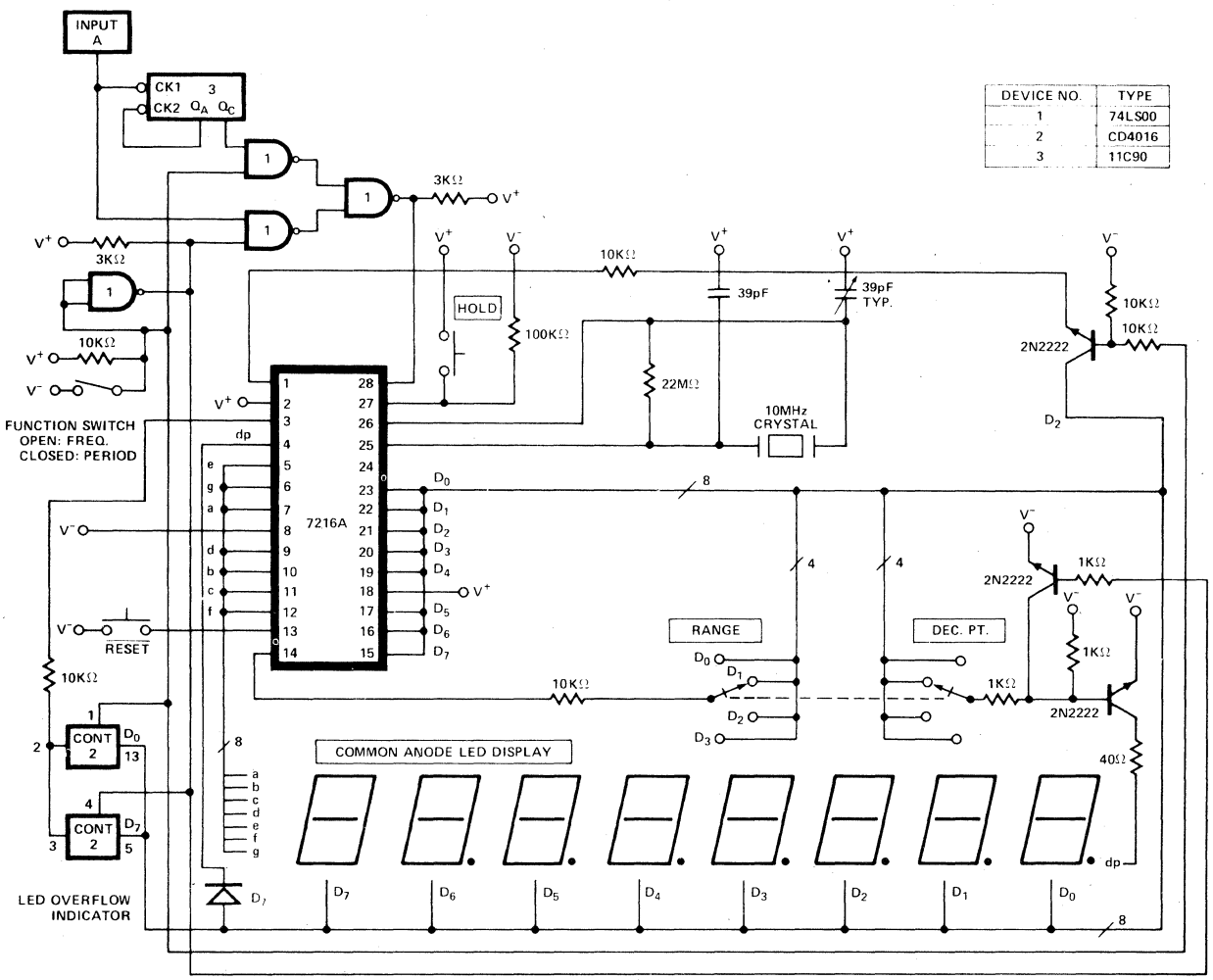


FIGURE 15. 100MHz Frequency, 2MHz Period Counter

OSCILLATOR CONSIDERATIONS

The oscillator has been implemented as a high gain complementary FET inverter. An external resistor of 10MΩ or 22MΩ should be connected between the oscillator input and output to provide biasing. The oscillator is designed to work with a parallel resonant 10 MHz quartz crystal with a static capacitance of 22pF and a series resistance of less than 35 ohms.

For a specific crystal and load capacitance, the required g_m can be calculated as follows:

$$g_m = \omega^2 C_{in} C_{out} R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

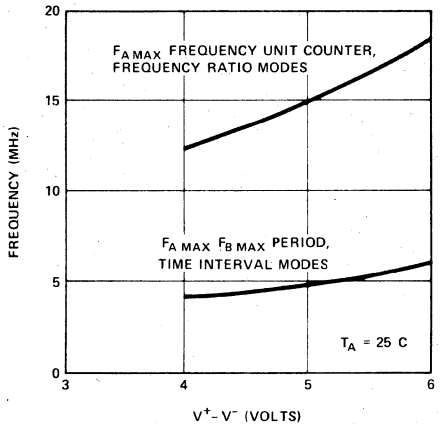
where $C_L = \left(\frac{C_{in}C_{out}}{C_{in}+C_{out}}\right)$

C_O = Crystal Static Capacitance
R_S = Crystal Series Resistance
C_{in} = Input Capacitance
C_{out} = Output Capacitance
$\omega = 2\pi f$

The required g_m should exceed the g_m specified for the CD-7216 by at least 50% to insure reliable startup. The oscillator input and output pins each contribute about 5pf to C_{in} and C_{out}. For maximum stability of frequency, C_{in} and C_{out} should be approximately twice the specified crystal static capacitance.

In cases where non decade prescalers are used it may be desirable to use a crystal which is neither 10 MHz or 1 MHz. In that case both the multiplex rate and time between measurements will be different. The multiplex rate is $f_{max} = \frac{f_{osc}}{2x10^4}$ for 10 MHz mode and $f_{max} = \frac{f_{osc}}{2x10^3}$ for the 1 MHz mode. The time between measurements is $\frac{2x10^6}{f_{osc}}$ in the 10 MHz mode and $\frac{2x10^5}{f_{osc}}$ in the 1 MHz mode.

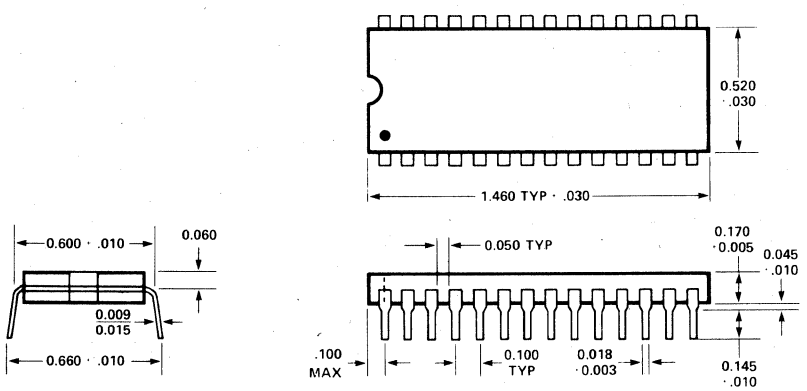
The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. Coupling from the External oscillator input to the oscillator output or input can cause undesirable shifts in oscillator frequency.



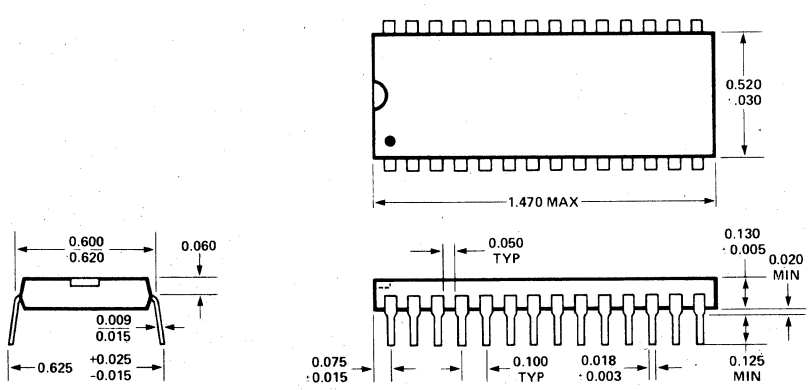
$F_{A\,MAX}$, $F_{B\,MAX}$ as a Function of $V^+ - V^-$

FIGURE 16. Typical Operating Characteristics

PACKAGE DIMENSIONS



28 PIN CERDIP DUAL IN LINE PACKAGE



28 PIN PLASTIC DUAL IN LINE PACKAGE

CD-7217 Series
CD-7227 Series
4 Digit CMOS Up/Down Counter/ Display Driver

FEATURES

- **Four decade, presettable up-down counter with parallel zero detect**
- **Settable register with contents continuously compared to counter**
- **Directly drives multiplexed 7 segment common anode or common cathode LED displays**
- **On-board multiplex scan oscillator**
- **Schmitt trigger on count input**
- **TTL compatible BCD I/O port, carry/borrow, equal, and zero outputs**
- **Display blank control for lower power operation; quiescent power dissipation < 5mW**
- **All terminals fully protected against static discharge**
- **Single 5V supply operation**

DESCRIPTION

The CD-7217 and CD-7227 are four digit, presettable up/down counters, each with an onboard presettable register continuously compared to the counter. The CD-7217 versions are intended for use in hardwired applications where thumbwheel switches are used for loading data, and simple SPDT switches are used for chip control. The CD-7227 versions are for use in processor-based systems, where presetting and control functions are performed under processor control.

These circuits provide multiplexed 7 segment LED display outputs, with common anode or common cathode configurations available. Digit and segment drivers are provided to directly drive displays of up to 1" character height at a 25% duty cycle. The frequency of the onboard multiplex oscillator may be controlled with a single capacitor, or the oscillator may be allowed to free run. Leading zeroes can be blanked. The data appearing at the 7 segment and BCD outputs is latched; the content of the counter is transferred into the latches under external control by means of the Store pin.

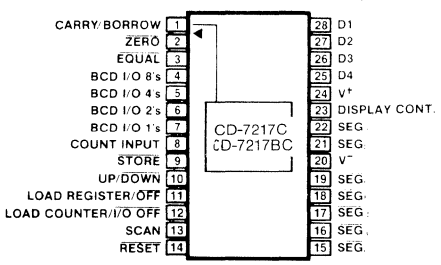
The CD-7217C/7227C (common anode) and CD-7217AC/7227AC (common cathode) versions are decade counters, providing a maximum count of 9999, while the CD-7217BC/7227BC (common anode) and CD-7217CC/7227CC (common cathode) are intended for timing purposes, providing a maximum count of 5959.

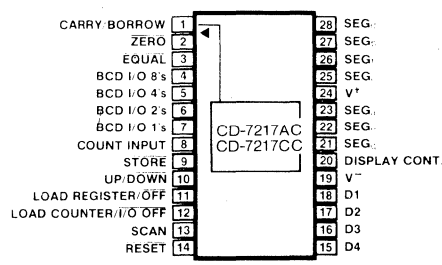
These circuits provide 3 main outputs; a carry/borrow output, which allows for direct cascading of counters, a zero output, which indicates when the count is zero, and an equal output, which indicates when the count is equal to the value contained in the register. Data is multiplexed to and from the device by means of a tri-state BCD I/O port. The carry/borrow, equal, zero outputs, and the BCD port will each drive one standard TTL load.

To permit operation in noisy environments and to prevent multiple triggering with slowly changing inputs, the count input is provided with a Schmitt trigger.

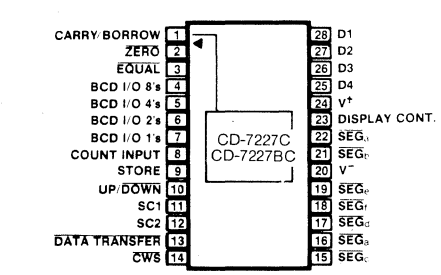
Input frequency is guaranteed to 2MHz, although the device will typically run with f_{in} as high as 5MHz.

CONNECTION DIAGRAMS

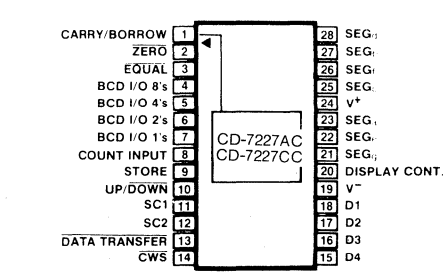




COMMON ANODE



COMMON CATHODE



CD-7217/7227

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (common anode/Cerdip) ..... 1 Watt } Note 1
Power Dissipation (common cathode/Plastic) ..... 0.5 Watt }
Supply Voltage V^+-V^- 6V
Input voltage (any terminal) ..... V^++0.3V V^- −0.3V − Note 2
Operating temperature range ..... −20°C to +70°C
Storage temperature range ..... −55°C to +125°C

Absolute maximum ratings define stress limitations which if exceeded may permanently damage the device. For continuous operation these devices must be operated under the conditions defined under "Operating Characteristics."

OPERATING CHARACTERISTICS

V^+-V^- = 5V, T_A = 25°C, Test Circuit, Display Diode Drop 1.7V, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply current (Lowest power mode)	I_{MIN}, (7217)	Display Off, LC, DC, UP/DN, ST, RS, BCD I/O Floating or at V^+ (Note 3)		350	500	μA
Supply current (Lowest power mode)	I_{MIN}, (7227)	Display off (Note 3)		300	500	μA
Supply current OPERATING	I_{OP}	Common Anode, Display On, all "8's"	175	200		mA
		Common Cathode, Display On, all "8's"	85	100		mA
Supply Voltage	V^+-V^-		4.5	5	5.5	V
Digit Driver output current	I_{DIG}	Common anode, V_{OUT} = V^+ −2.2V	175	200		mA peak
Segment driver output current	I_{SEG}	Common anode, V_{OUT} = V^- +1.3V	−25	−40		mA peak
Digit Driver output current	I_{DIG}	Common cathode, V_{OUT} = V^- +1.3V	−75	−100		mA peak
Segment Driver output current	I_{SEG}	Common cathode V_{OUT} = V^+ −2V	10	12.5		mA peak
$\overline{ST}$, $\overline{RS}$, UP/DN input pullup current	I_P	V_{OUT} = V^+ −2V (See Note 3)	5	25		μA
3 level input impedance				100		kΩ
BCD I/O input high voltage	V_{BIH}	7217 common anode (Note 4)	1.3			V
		7217 common cathode (Note 4)	4.1			V
		7227 with 50pF effective load	3			V
BCD I/O input low voltage	V_{BIL}	7217 common anode (Note 4)			0.8	V
		7217 common cathode (Note 4)			3.7	V
		7227 with 50pF effective load			1.5	V
BCD I/O input pullup current	I_{BPU}	7217 common anode V_{IN} = V^+ −2V (Note 3)	5	25		μA
BCD I/O input pulldown current	I_{BPD}	7217 common cathode V_{IN} = V^- +1.3V (Note 3)	5	25		μA
BCD I/O, Carry/borrow zero, equal outputs output high current	I_{BOH}	V_{OH} = V^+ −1.5V	100			μA
BCD I/O, Carry/borrow zero, equal outputs output low current	I_{BOL}	V_{OL} = V_{OL} V^- +0.4V	−2			mA
Count input frequency (Guaranteed)	f_{in}	V^+ - V^- = 5V ± 10%, −20°C < T_A < +70°C	0	5	2	MHz
Count input threshold	V_{TC}	V^+ - V^- = 5V		2		V
Count input hysteresis	V_{HC}	V^+-V^- = 5V		0.5		V
Display scan oscillator frequency	f_{ds}	Free-running (SCAN terminal open circuit)		10		KHz
Operating Temperature Range	T_A		−20		70	°C

NOTE 1 These limited refer to the package and will not be obtained during normal operation.

NOTE 2 Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ or less than V^- may cause destructive device latchup. For this reason it is recommended that the power supply to the device be established before any inputs are applied and that in multiple systems the supply to the 7217/7227 be turned on first.

NOTE 3 In the 7217 the Up/Down, Store, Reset and the BCD I/O as inputs have pullup devices which consume power when connected to the negative supply. When all these terminals are connected to the negative supply, with the display off, the device will consume typically 750 μA. The 7227 devices do not have these pullups and thus are not subject to this condition.

NOTE 4 These voltages are adjusted to allow the use of thumbwheel switches for the 7217 versions. Note that a positive level is taken as a logic zero for 7217 common-cathode versions only.

TEST CIRCUITS

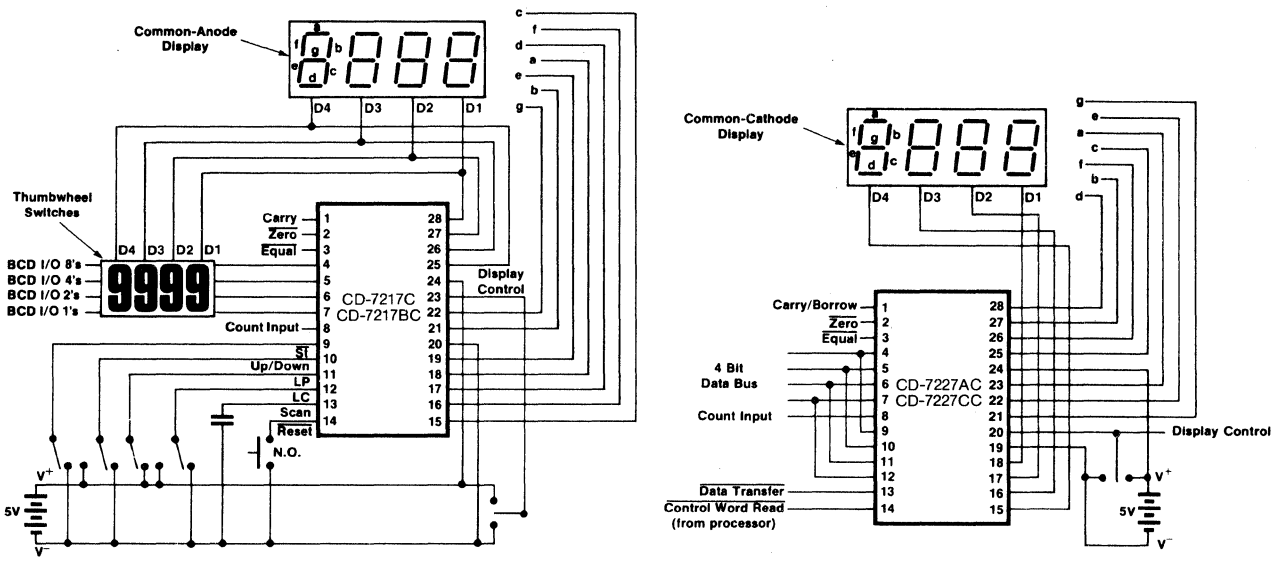


Figure 1

Figure 1 shows the CD-7217 in the common-anode version and the CD-7227 in the common-cathode version.

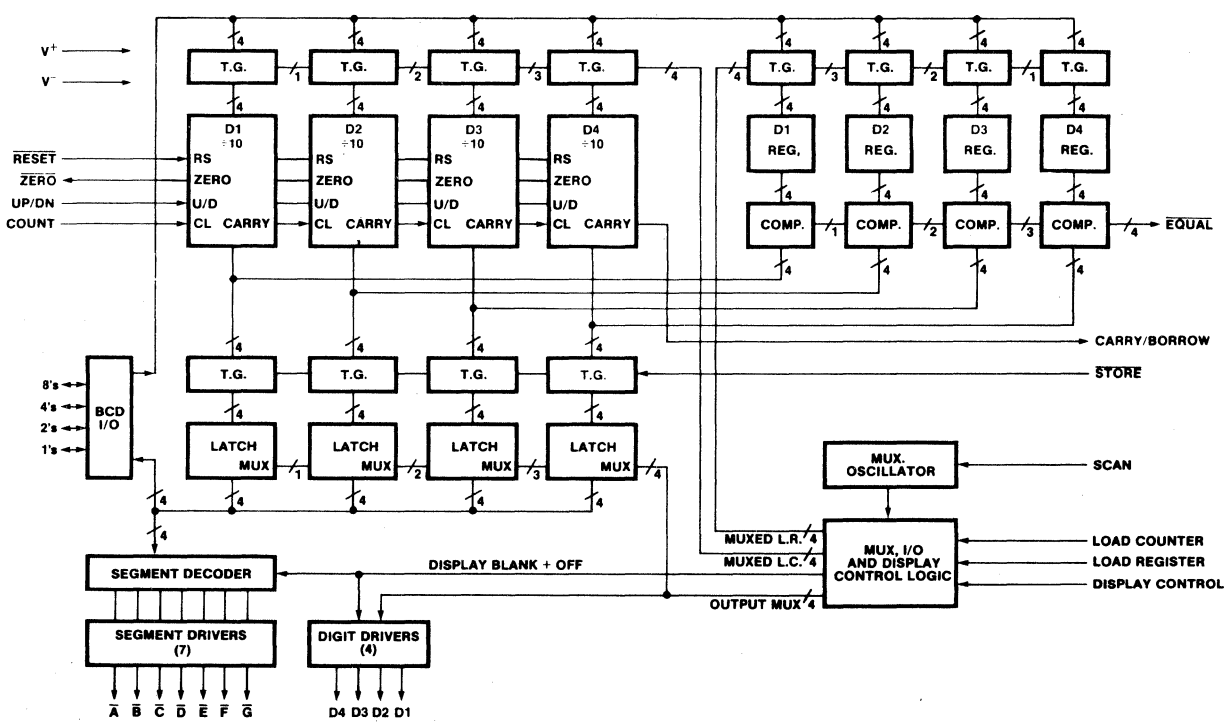


Figure 2: Block Diagram CD-7217

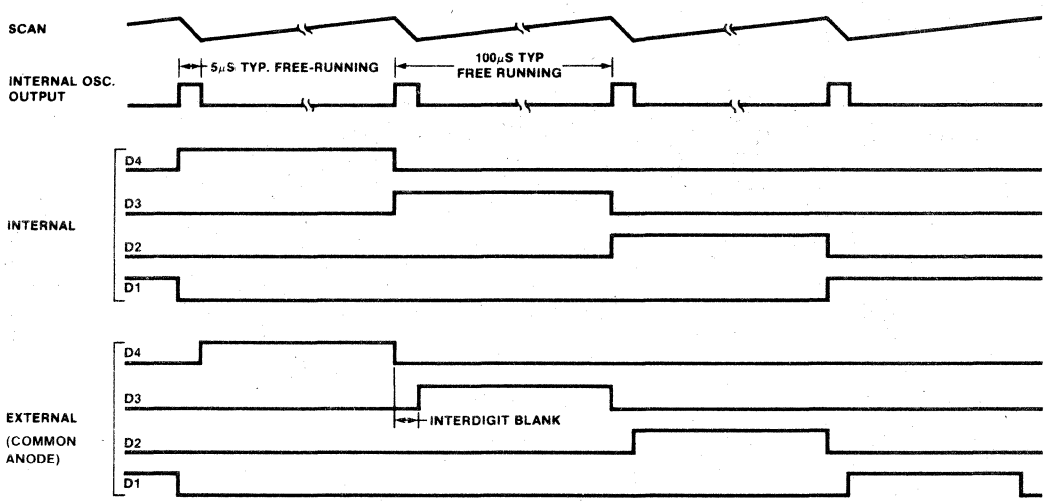


Figure 3: Multiplex Timing

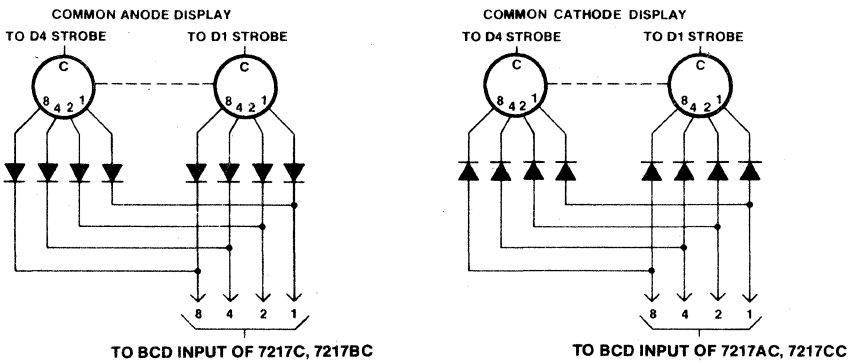


Figure 4: Thumbwheel switch/diode connections

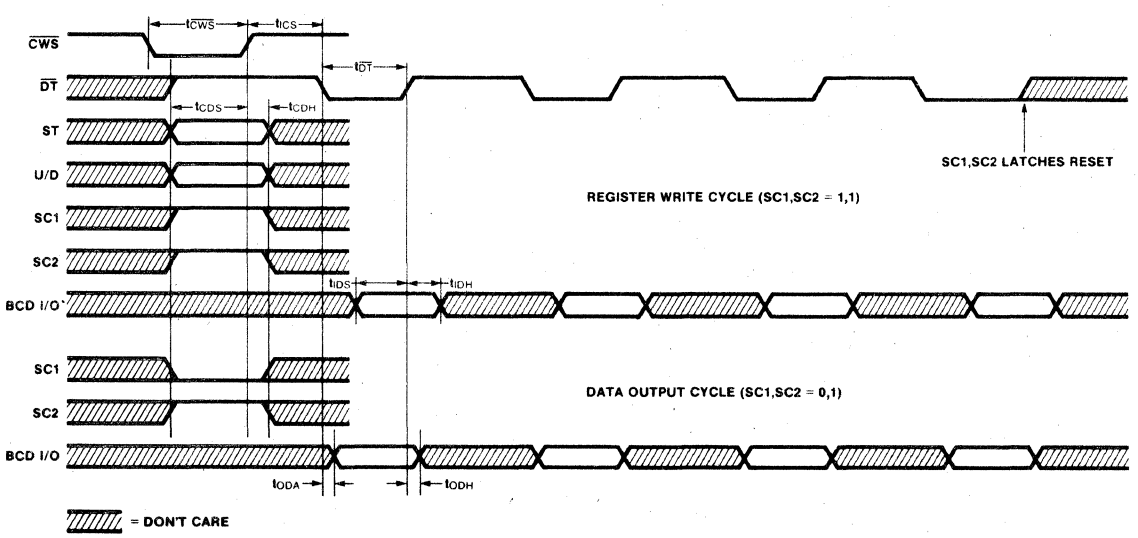


Figure 5: CD-7227 I/O Timing (See Table 2)

CONTROL INPUT DEFINITIONS ICM7217

INPUT	TERMINAL	VOLTAGE	FUNCTION
Store ($\overline{ST}$)	9	V^+ (or floating) V^-	Output latches not updated Output latches updated
Up/Down (U/$\overline{D}$)	10	V^+ (or floating) V^-	Counter counts up Counter counts down
Reset ($\overline{RST}$)	14	V^+ (or floating) V^-	Normal Operation Counter Reset
Load Counter LC/$\overline{I/O\ OFF}$	12	Unconnected V^+ V^-	Normal operation Counter loaded with BCD data BCD port forced to Hi Z condition
Load Register LR/$\overline{OFF}$	11	Unconnected V^+ V^-	Normal operation Register loaded with BCD data Display drivers disabled; BCD port forced to Hi Z condition, mpx counter reset to D3; mpx oscillator inhibited
Display Control (DC)	23 Common Anode 20 Common Cathode	Unconnected V^+ V^-	Normal operation Segment drivers disabled Leading zero blanking inhibited

CONTROL INPUT DEFINITIONS CD-7227

INPUT		TERMINAL	VOLTAGE	FUNCTION
	Data Transfer ($\overline{DT}$)	13	V^+ V^-	Normal Operation Causes transfer of data as directed by select code
Control Word Port	Store (ST)	9	V^+ (During $\overline{CWS}$ Pulse) V^-	Output latches updated Output latches not updated
,,	Up/Down (U/$\overline{D}$)	10	V^+ (During $\overline{CWS}$ Pulse) V^-	Counter counts up Counter counts down
,, ,,	Select Code Bit 1 (SC1) Select Code Bit 2 (SC2)	11 12	$V^+ = 1$ $V^- = 0$	SC1, SC2 00 Change store and up/down latches. No data transfer. 01 Output latch data active 10 Counter to be preset 11 Register to be preset
	Control Word Strobe ($\overline{CWS}$)	14	V^+ V^-	Normal operation Causes control word to be written into control latches
	Display Control (DC)	23 Common Anode 20 Common Cathode	Unconnected V^+ V^-	Normal operation Display drivers disabled Leading zero blanking inhibited

DESCRIPTION OF OPERATION

OUTPUTS

The carry/borrow output is a positive going signal occurring typically 500nS after the positive going edge of the count input. It advances the counter from 9999 to 0000 when counting up and from 0000 to 9999 when counting down. This output allows direct cascading of counters.

The $\overline{equal}$ output assumes a negative level when the contents of the counter and register are equal.

The $\overline{zero}$ output assumes a negative level when the content of the counter is 0000.

The carry/borrow, $\overline{equal}$, and $\overline{zero}$ outputs will drive a single TTL load over the full range of supply voltage and ambient temperature; for a logic zero, these outputs will sink 2mA @ 0.4V (on resistance 200 ohms), and for a logic one, the outputs source >60μA.

The digit and segment drivers provide a decoded 7 segment display system, capable of directly driving common anode LED displays at typical peak currents of 40mA/seg. This corresponds to average currents of 10mA/seg at a 25% multiplex duty cycle. For the common cathode versions, peak segment currents are 12.5mA, corresponding to average segment currents of 3.1mA. The display pin controls the display output using three level logic. The pin is self-biased to a voltage approximately 1/2 (V^+-V^-); this corresponds to normal operation. When this pin is connected to V^+, the segments are inhibited, and when connected to V^-, the leading zero blanking feature is inhibited. For normal operation (display on with leading zero blanking) the pin may be left open. The display may be controlled with a 3 position SPDT switch; see fig. 1.

The BCD I/O port provides a means of transferring data to and from the device. The CD-7217 versions multiplex data into the counter or register via thumbwheel switches, depending on inputs to the load counter or load register pins; in the CD-7227 versions, input/output control and timing must be provided externally. When functioning as outputs, the BCD I/O pins will drive one standard TTL load.

The onboard multiplex scan oscillator has a nominal free-running frequency of 10kHz. This may be reduced by the addition of a single capacitor between the Scan pin and the positive supply, or the oscillator may be directly overdriven to about 20kHz. Capacitor values and corresponding nominal oscillator frequencies, digit repetition rates, and loading times (for CD-7217 versions) are shown in Table 1 below.

The internal oscillator output has a duty cycle of approximately 25:1, providing a short pulse occurring at the oscillator frequency. This pulse clocks the four-state counter which provides the four multiplex phases. The short pulse width is used to delay the digit driver outputs, thereby providing inter-digit blanking which prevents ghosting. The digits are scanned from MSD (D4) to LSD (D1). See Fig. 3 for the display digit multiplex timing.

Table 1

Scan Capacitor	Nominal Oscillator Frequency	Digit Repetition Date	Scan Cycle Time
None	10kHz	2.5kHz	400μs
20pF	5kHz	1.2kHz	800μs
90pF	1kHz	250Hz	4ms

CONTROL OF CD-7217

The counter is incremented by the rising edge of the count input signal when U/D is high. It is decremented when U/D is low. A Schmitt trigger on the count input provides hysteresis to prevent double triggering on slow rising edges and permits operation in noisy environments.

The $\overline{ST}$ pin controls the internal latches and consequently the signals appearing at the 7 segment and BCD outputs. Bringing the store pin to V^- transfers the contents of the counter into the latches.

The counter is asynchronously reset to 0000 by bringing the $\overline{RST}$ pin to V^-. The count input is inhibited during reset and load counter operations. The $\overline{ST}$, $\overline{RST}$ and Up/$\overline{Down}$ pins are provided with pullup resistors of approximately 75 kΩ.

The BCD I/O pins, the load counter (LC), and load register (LR) pins combine to provide presetting and compare functions. LC and LR are three-level inputs, being self-biased at approximately 1/2 (V^+-V^-) for normal operation. With both LC and LR open, the BCD I/O pins provide a multiplexed BCD output of the latch contents, scanned from MSD to LSD by the display multiplex. In this mode of operation, the BCD pins will drive one TTL load. When either or both of the LC or LR pins is connected to V^+, the TTL driver devices are turned off and the BCD pins become high-impedance inputs. When LC is connected to V^+, the count input is inhibited and the levels at the BCD pins are multiplexed into the counter. When LR is connected to V^+, the levels at the BCD pins are multiplexed into the register without disturbing the counter. When both are connected to V^+, the count is inhibited and both register and counter are presettable. When LR is connected to V^-, the oscillator is inhibited, the BCD I/O pins go to the high impedance state, and the segment and digit drivers are turned off. This allows the display to be used for other purposes and minimizes power consumption. In this display off condition, the circuit will continue to count, and the carry/borrow, equal, zero, up/down, reset and store functions operate as normal. When LC is connected to V^-, the BCD I/O pins are forced to the high impedance state without disturbing the counter or register. See "Control Input Definitions" for a cataloging of the pins that function as three-state self-biased inputs and their respective operations.

Note that the 7217C and 7217BC have been designed to drive common anode displays. The BCD inputs are active high, as are the BCD outputs.

The 7217AC and 7217CC are used to drive common cathode displays, and the BCD inputs are active low. BCD outputs are active high.

The 7227 series has been designed to permit microprocessor control of the inputs. BCD inputs and outputs are active high.

NOTES ON THUMBWHEEL SWITCHES & MULTIPLEXING

The thumbwheel switches used with these circuits (both common anode and common cathode) are TRUE BCD coded; i.e. all switches open corresponds to 0000.

Since the thumbwheel switches are connected in parallel, diodes must be provided to prevent crosstalk between digits. See fig. 4.

In order to maintain reasonable noise margins, these diodes should be specified with low forward voltage drops.

During load counter and load register operations, the multiplex oscillator is disconnected from the scan input and is allowed to free-run. In all other conditions, the oscillator may be directly overdriven; however the internal oscillator output will be of the same duty cycle and phase as the overdriving signal, and the digits are blanked during the time the internal oscillator output is at a positive level. To insure proper leading zero blanking, the blanking time should not be less than about 2μs, and by varying the duty cycle, the display brightness may be altered. Overdriving the oscillator at less than 200Hz may cause display flickering. See fig. 6 for brightness control circuits.

These circuits are variable-duty-cycle oscillators suitable for overdriving the multiplex oscillator at the Scan input of a CD-7217. The inverters should be CMOS CD4000 series, and the diodes may be any inexpensive device such as IN914.

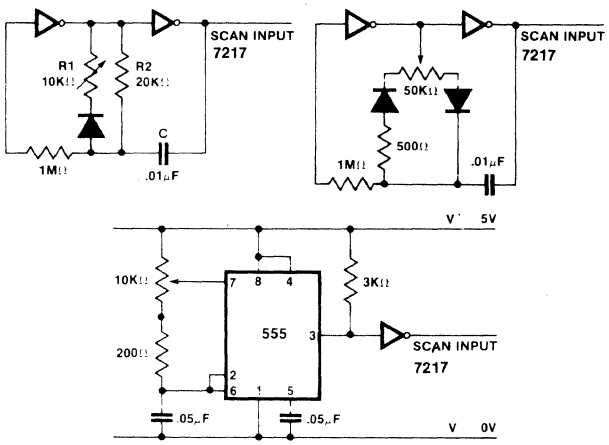


Figure 6: Brightness Circuits

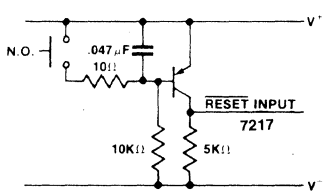
OUTPUT AND INPUT RESTRICTIONS

The carry/borrow output is not valid during load counter and reset operations.

The $\overline{\text{equal}}$ output is not valid during load counter or load register operations.

The $\overline{\text{zero}}$ output is not valid during a load counter operation.

The reset input may be susceptible to noise if its input rise time (coming out of reset) is less than about 500μs. This will present no problems when this input is driven by active devices (i.e., TTL or CMOS logic) but in hardwired systems adding virtually any capacitance to the $\overline{\text{reset}}$ input can cause trouble. A simple circuit which provides a reliable power-up reset and a fast rise time on the $\overline{\text{reset}}$ input is shown below.



CONTROL OF 7227 VERSIONS

In the 7227 versions, the Store, Up/$\overline{\text{Down}}$, SC1 and SC2 (select code bits 1 and 2) pins form a four-bit control word input. A negative-going pulse on the $\overline{\text{CWS}}$ (control word strobe) pin writes the data on these pins into four internal control latches, and resets the multiplex counter in preparation for sequencing a data transfer operation. The select code 00 is reserved for changing the state of the Store and/or Up/$\overline{\text{Down}}$ latches without initiating a data transfer. Writing a one into the Store latch sets the latch and causes the data in the counter to be transferred into the output latches, while writing a zero resets the latches causing them to retain data and not be updated. Similarly, writing a one into the Up/$\overline{\text{Down}}$ latch causes the counter to count up and writing a zero causes the counter to count down. The state of the Store and Up/$\overline{\text{Down}}$ latches may also be changed with a nonzero select code.

Writing a nonzero select code initiates a data transfer operation. Writing select code of 01 (SC1, SC2) indicates that the data in the output latches will be active and enables the BCD I/O port to output the data. Writing a select code of 11 indicates that the register will be preset, and a 10 indicates that the counter will be preset.

When a nonzero select code is read, the clock of the four-state multiplex counter is switched to the $\overline{\text{DT}}$ (data transfer) pin. Negative-going pulses at this pin then sequence a digit-by-digit data transfer, either outputting data or presetting the counter or register as determined by the select code. The output drivers of the BCD I/O port will be enabled only while $\overline{\text{DT}}$ is low during a data transfer initiated with a 01 select code.

The sequence of digits will be D4-D3-D2-D1, i.e. when outputting, the data from D4 will be valid during the first $\overline{\text{DT}}$ pulse, then D3 will be valid during the second pulse, etc. When presetting, the data for D4 must be valid at the positive-going transition (trailing edge) of the first $\overline{\text{DT}}$ pulse, the data for D3 must be valid during the second $\overline{\text{DT}}$ pulse, etc.

At the end of a data transfer operation, on the positive going transition of the fourth $\overline{\text{DT}}$ pulse, the SC1 and SC2 control latches will automatically reset, terminating the data transfer and reconnecting the multiplex counter clock to the oscillator. In the 7227 versions, the multiplex oscillator is always free-running, except during a data transfer operation when it is disabled.

Fig. 5 shows the timing of data transfers initiated with a 11 select code (writing into the register) and a 01 select code (reading out of the output latches). Typical times during which data must be valid at the control word and BCD I/O ports are indicated in Table 2.

Table 2

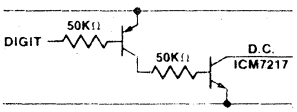
SYMBOL	DEFINITION	TIME, NS	SYMBOL	DEFINITION	TIME, NS
$t_{\overline{cws}}$	CONTROL WORD STROBE WIDTH	200	t_{cdh}	CONTROL DATA HOLD	100
t_{ics}	INTERNAL CONTROL SETUP	500	t_{ids}	INPUT DATA SETUP	100
			t_{idh}	INPUT DATA HOLD	100
$t_{\overline{dt}}$	DATA TRANSFER PULSE WIDTH	200	t_{oda}	OUTPUT DATA ACCESS	100
t_{cds}	CONTROL DATA SETUP	100	t_{odh}	OUTPUT DATA HOLD	100

APPLICATIONS

1. FIXED DECIMAL POINT

In the common anode versions, a fixed decimal point may be implemented by connecting the D.P. segment lead from the appropriate digit (with separate digit displays) through a 39Ω series resistor to V⁻. With common cathode devices, the D.P. segment lead should be connected through a 75Ω series resistor to V⁺.

To force the device to display leading zeroes after a fixed decimal point, use a bipolar transistor and base resistor in a configuration like that of Fig. 8 with the resistor connected to the digit output driving the D.P. for left hand D.P. displays, and to the next least significant digit output for right hand D.P. display. For common cathode devices use a PNP and NPN transistor as shown below:



2. UNIT COUNTER WITH BCD OUTPUT (Figure 7)

The simplest application of the CD-7217 is a 4 digit unit counter. All that is required is a CD-7217, a power supply and a 4 digit display. Add a momentary switch for reset, an SPDT center-off switch to blank the display or view leading zeroes, and one more SPDT switch for up/down control. Using a CD-7217AC and a common-cathode calculator-type display, results in the least expensive digital counter/display system available.

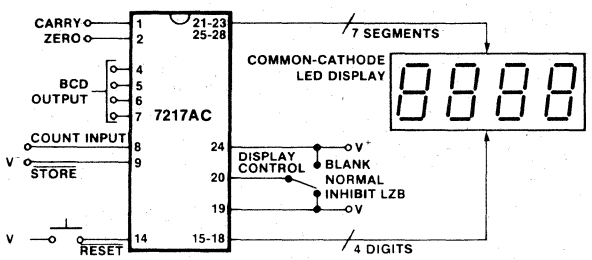


Figure 7: Unit Counter

3. PRECISION ELAPSED TIME/COUNTDOWN TIMER (Figure 8)

This circuit uses an ICM7213 precision one minute/one second timebase generator and a 4.1943 MHz crystal oscillator and divider for generating pulses counted by an CD-7217BC. The thumbwheel switches allow a starting time to be entered into the counter for a preset-countdown type timer, and allow the register to be set for compare functions. For instance, to make a 24-hour clock with BCD output the register can be preset with 2400 and the $\overline{\text{Equal}}$ output used to reset the counter. Note the 10k resistor connected between the LC terminal and V⁻. This resistor pulls the LC input low when not loading, thereby inhibiting the BCD output drivers. This resistor should be eliminated and SW4 replaced with an SPDT center-off switch if the BCD outputs are to be used. This technique may be used on any 3-level input. The 100k pullup resistor on the count input is used to ensure proper logic voltage swing from the ICM7213. For a less expensive (and less accurate) timebase, a 555 timer may be used in a configuration like that shown in Fig. 12 to generate a 1Hz reference.

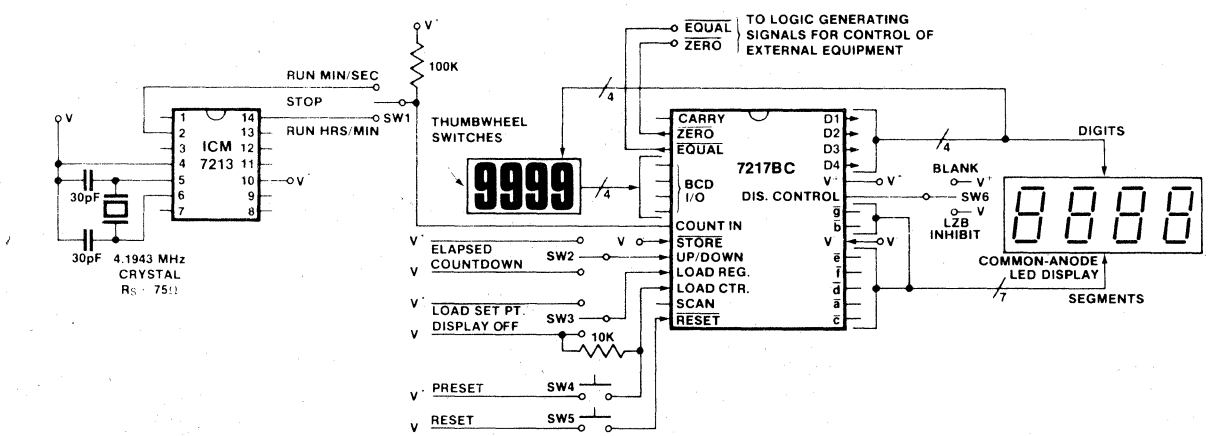


Figure 8: Precision Timer

4. 8-DIGIT UP/DOWN COUNTER (Figure 9)

This circuit shows how to cascade counters and retain correct leading zero blanking. The NAND gate detects whether a digit is active since one of the two segments $\overline{a}$ or $\overline{b}$ is active on any unblanked number. The flip flop is clocked by the least significant digit of the high order counter, and if this digit is not blanked, the Q output of the flip flop goes high and turns on the NPN transistor, thereby inhibiting leading zero blanking on the low order counter.

It is possible to use separate thumbwheel switches for presetting, but as the devices load data with the oscillator free-running, the multiplexing of the two devices is difficult to synchronize. This presents no problems with the CD-7227 devices, since the two devices are operated as peripherals to a processor.

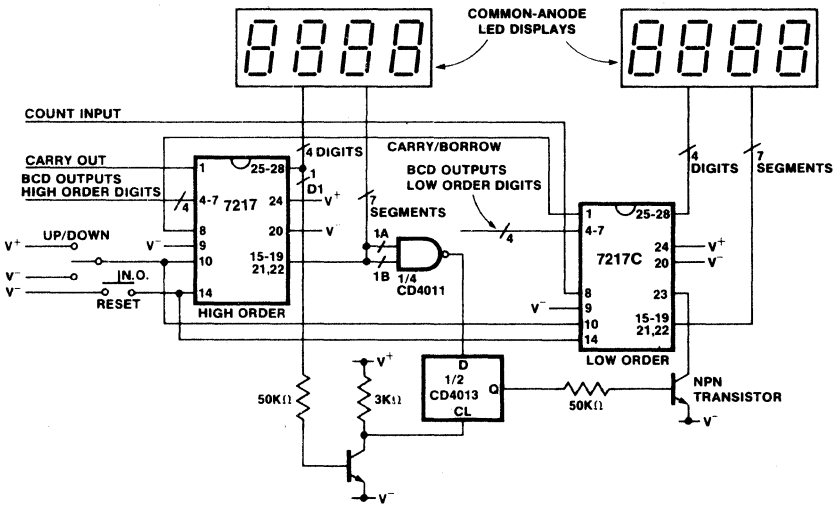


Figure 9: 8 Digit Up/Down Counter

5. TAPE RECORDER POSITION INDICATOR/ CONTROLLER (Figure 10)

This circuit shows an application which uses the up/down counting feature of the CD-7217 to keep track of tape position. This circuit is representative of the many applications of up/down counting in monitoring dimensional position. For example, an CD-7227 as a peripheral to a processor can monitor the position of a lathe bed or digitizing head, transfer the data to the processor, drive interrupts to the processor using the $\overline{\text{equal}}$ or $\overline{\text{zero}}$ outputs, and serve as a numerical display for the processor.

In the tape recorder application, the preset register, $\overline{\text{equal}}$ and $\overline{\text{zero}}$ outputs are used to control the recorder. To make the recorder stop at a particular point on the tape, the register can be set with the stop point and the $\overline{\text{equal}}$ output used to stop the recorder either on fast forward, play or rewind.

To make the recorder stop before the tape comes free of the reel on rewind, a leader should be used. Resetting the counter at the starting point of the tape, a few feet from the end of the leader, allows the zero output to be used to stop the recorder on rewind, leaving the leader on the reel.

The 1MΩ resistor and .0047μF capacitor on the count input provide a time constant of about 5ms to debounce the reel switch. The Schmitt trigger on the count input of the CD-7217 squares up the signal before applying it to the counter. This technique may be used to debounce switch-closure inputs in other applications.

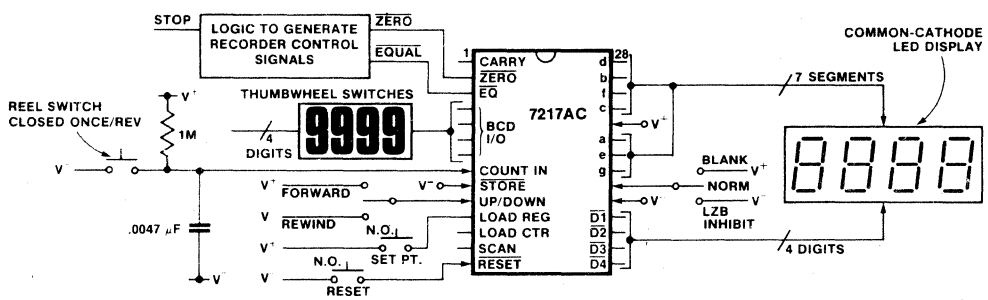


Figure 10: Recorder Indicator

6. PRECISION FREQUENCY COUNTER/ TACHOMETER (Figure 11)

This circuit is a simple implementation of a four digit frequency counter, using an ICM7207A to provide the one second gating window and the $\overline{\text{store}}$ and $\overline{\text{reset}}$ signals. In this configuration, the display reads hertz directly. With Pin 11 of the ICM7027A connected to V^+, the gating time will be 0.1 second; this will display tens of hertz as the least significant digit. For shorter gating times, an ICM7207 may be used (with a 6.5536 MHz crystal), giving a 0.01 second gating with Pin 11 connected to V^+, and a 0.1 second gating with Pin 11 open.

To implement a four digit tachometer, the ICM7207A with one second gating should be used. To get the display to read directly in RPM, the rotational frequency of the object to be measured must be multiplied by 60. This can be done electronically using a phase-locked loop, or mechanically by using a disc rotating with the object with the appropriate number of holes drilled around its edge to interrupt the light from an LED to a photo-dector. For faster updating, use 0.1 second gating, and multiply the rotational frequency by 600.

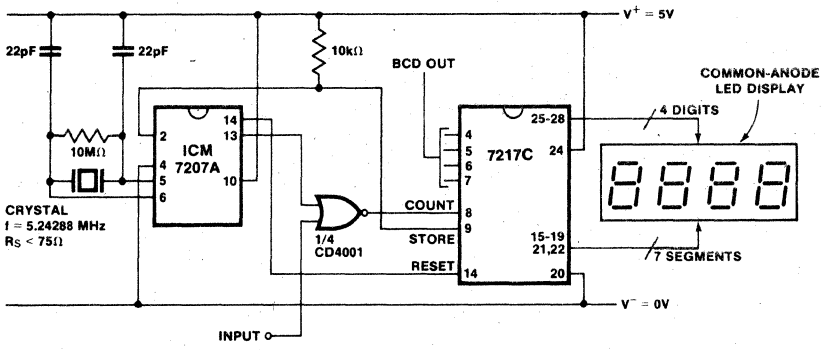


Figure 11: Precision Frequency Counter

7. INEXPENSIVE FREQUENCY COUNTER/ TACHOMETER (Figure 12)

This circuit uses an inexpensive 556 dual timer rather than an ICM7027A to generate the gating, $\overline{\text{store}}$ and $\overline{\text{reset}}$ signals. To provide the gating signal, one timer is configured as an astable multivibrator, using R_A, R_B and C to provide an output that is positive for approximately 1 second and negative for approximately 300-500μS. The gating positive time is given by $G_L = 0.693\ (R_A + R_B)\ C$ while the gating low time is $G_L = 0.693 R_B C$. The system is calibrated by using a 5MΩ potentiometer for R_A as a "coarse" control and a 1k potentiometer for R_B as a "fine" control. The other timer in the 556 is configured as a one-shot triggered by the negative-going edge of the gating signal. This one-shot output is inverted to serve as the $\overline{\text{store}}$ pulse and to hold $\overline{\text{reset}}$ high. When the one-shot times out and $\overline{\text{store}}$ goes high, $\overline{\text{reset}}$ goes low, resetting the counter for the next measurement. The one-shot pulse width will be approximately 50μs with the component values shown. When "fine" trimming the gating signal with R_B, care should be taken to keep the gating low time (= $0.693 R_B C$) at least twice as long as the one-shot pulse width.

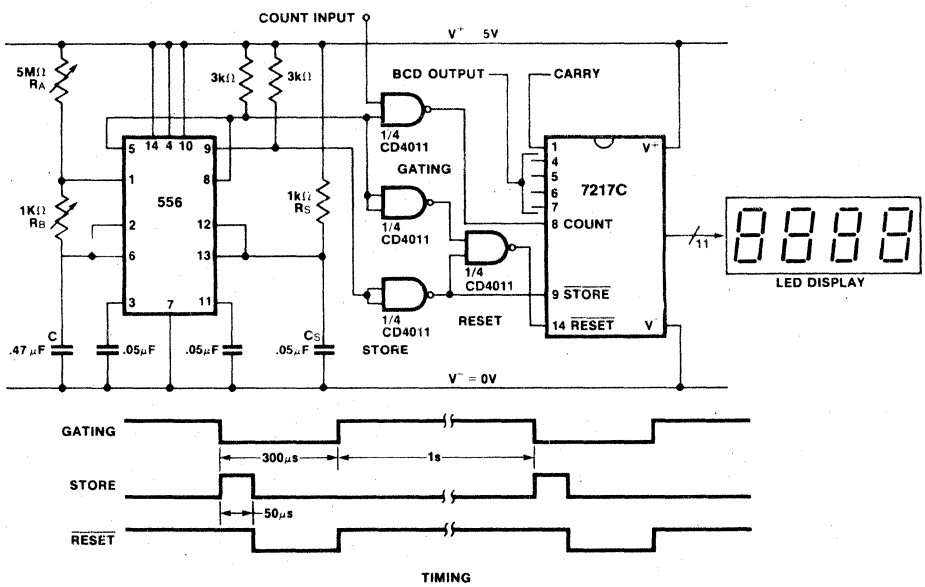


Figure 12: Inexpensive Frequency Counter

8. INEXPENSIVE CAPACITANCE METER (Figure 13)

This circuit uses two 555 timers (or one 556) to generate a gated count to the CD-7217 dependent on the value of an arbitrary capacitor. The clock timer operates as a fixed oscillator whose output period is determined by R_1, R_2 and C (which is switched with the range). The relation is $T_{CL} = 0.693\ (R_1 + 2R_2)\ C$. The gating timer also operates as an oscillator, but its output high time (and period) is determined by the value of the measured capacitor in combination with R_3 and R_4 (also switched with range). The output high time of this timer is given by $G_H = 0.693\ (R_3 + R_4)\ Cm$. The number of clock pulses during one gating time is thus given by

$$N = \frac{(R_3 + R_4)\ Cm}{(R_1 + 2R_2)\ C}$$

With the values shown, this number is ten times the number to be displayed when the circuit is calibrated. This allows the use of a dummy divide by 10 (the CD4017) to eliminate jitter in the least significant digit of the display. The R_3 resistors should be precision potentiometers for greatest accuracy, and the circuit must be calibrated in each range. Range A reads 1-9999pF, Range B reads 1-9999nF, and Range C reads 1-9999μF.

Note that in comparison to Fig. 12, the $\overline{\text{store}}$ and $\overline{\text{reset}}$ signals are generated by CD4000 series one-shots. The operation of the two circuits is similar.

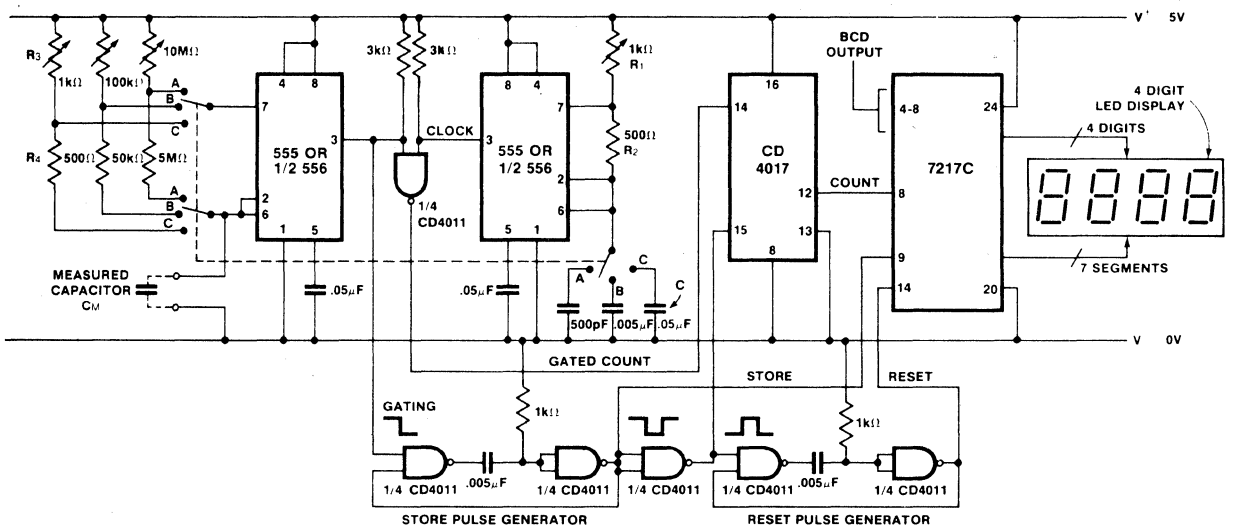


Figure 13: Capacitance Meter

9. LCD DISPLAY INTERFACE (Figure 14)

The low-power operation of the CD-7217 makes an LCD interface desirable. The Siliconix CF411 4 digit BCD to LCD display driver easily interfaces to the CD-7217AC with one CD4000-series package to provide a total system power consumption of less than 5mW. The common-cathode devices should be used, since the digit drivers are CMOS, while the common-anode digit drivers are NPN devices and will not provide full logic swing.

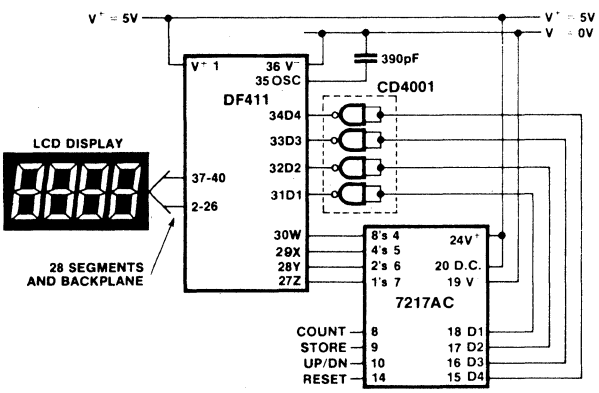


Figure 14: LCD Display Interface

10. MICROPROCESSOR INTERFACE- 7227 (Figure 15)

This circuit shows the hardware necessary to interface the CD-7227 to an Intersil IM6100 CMOS microprocessor. Using an IM6101 Parallel Interface Element (PIE) allows the addition of one or more CD-7227 devices as generalized peripherals to any IM6100 system, using a minimum of external components.

A similar configuration may be used with the MC6800 using the corresponding PIE, while an 8223 can be used to interface 8080 based systems.

The CD-7227 can perform many "accessory" functions that are inefficient or impossible for the processor to perform. For simple systems, the CD-7227 can provide a cost-effective display latch/decoder/driver. By adding a timebase such as an ICM7213, and using a 7227CC or DC, an inexpensive real-time clock/display, directly accessible by the procesor, can be implemented.

In the area of "intelligent" instrumentation, the CD-7227 can serve as a high speed (up to 2MHz) counter/comparator. This is the element often used for converting time, frequency, and positional and occurence data into digital form. For example, an CD-7207A can be used with two CD-7227's to provide an 8 digit, 2MHz frequency counter.

Since the CD-7207A gating output has a 50% duty cycle, there is 1 second for the processor to respond to an interrupt, generated by the negative going edge of this signal while it inhibits the count. The processor can respond to the interrupt using ROM based subroutines, to store the data, reset the counter, and read the data into main memory. To add simultaneous period display, the processor inverts the data and a DD-7218 Universal Display Driver stores and displays it. Capacitance can be measured by counting the frequency of an oscillator, as in the Capacitance Meter circuit, allowing the measurement of fluid levels, proximity detectors, etc.

Future Application Notes and Bulletins will address the CD-7227 more fully, and users are welcome to submit any circuits or unique uses for review and possible publication in application information.

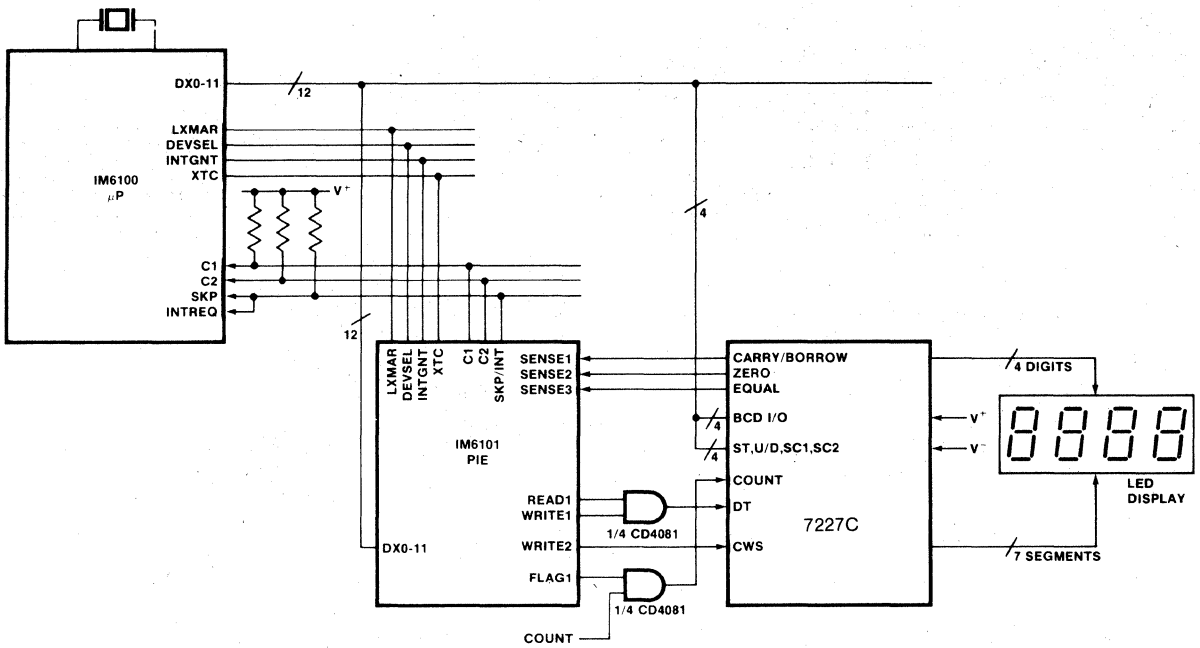
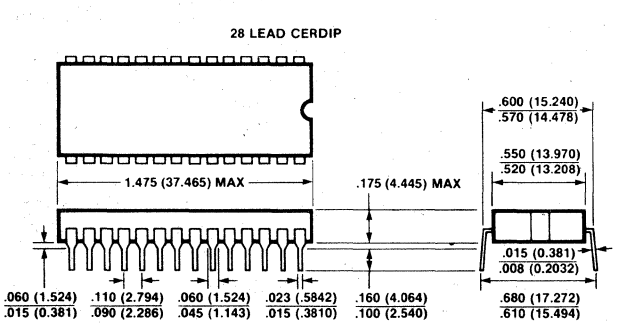


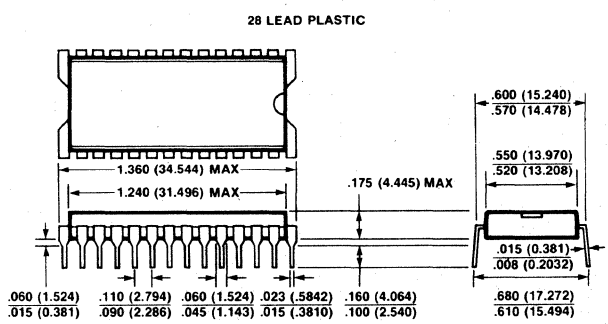
Figure 15: IM6100 Interface

OPTION MATRIX & ORDERING INFORMATION

	Order Part Number	Display Option	Count Option Max Count	28-LEAD Package
Hardwired Control Versions	CD-7217C	Common Anode	Decade/9999	CERDIP
	CD-7217AC	Common Cathode	Decade/9999	PLASTIC
	CD-7217BC	Common Anode	Timer/5959	CERDIP
	CD-7217CC	Common Cathode	Timer/5959	PLASTIC
Processor Control Versions	CD-7227C	Common Anode	Decade/9999	CERDIP
	CD-7227AC	Common Cathode	Decade/9999	PLASTIC
	CD-7227BC	Common Anode	Timer/5959	CERDIP
	CD-7227CC	Common Cathode	Timer/5959	PLASTIC

PACKAGE DIMENSIONS





DATEL INTERSIL

CD-7224 (LCD)
CD-7225 (LED)
4½ Digit Counter/Decoder/Drivers

FEATURES

- **High frequency counting - guaranteed 15MHz, typically 25MHz at 5V**
- **Low power operation - less than 100μW quiescent**
- **Direct 4 1/2 digit seven-segment display drive - CD-7224 for LCD displays, CD-7225 for LED displays**
- **Store and Reset inputs permit operation as frequency or period counter**
- **True count inhibit disables first counter stage**
- **Carry output for cascading four-digit blocks**
- **Schmitt-trigger on the count input allows operation in noisy environments or with slowly changing inputs**
- **Leading zero blanking input and output for correct leading zero blanking with cascaded devices**
- **LCD devices provide complete onboard oscillator and divider chain to generate backplane frequency, or backplane driver may be disabled allowing segments to be slaved to a master backplane signal**
- **LED devices provide Brightness input which can function digitally as a display enable or with a single potentiometer as a continuous display brightness control**
- **All inputs fully protected against static discharge - no special handling precautions necessary**

DESCRIPTION

The CD-7224 and CD-7225 devices constitute a family of high-performance CMOS 4 1/2-digit counters, including decoders, output latches, display drivers, count inhibit, leading zero blanking, and reset circuitry.

The CD-7224 (19999 maximum count) and CD-7224A (15959 maximum count) provide 29 segment outputs and a backplane driver output, generating the zero dc component signals necessary to darive a conventional 4 1/2-digit liquid crystal display. These devices also include a complete RC oscillator and divider chain to generate the backplane frequency, and a backplane driver disable control which allows the segments to be slaved to a master backplane signal.

The CD-7225 (19999 maximum count) and CD-7225A (15959 maximum count) provide 28 segment and 1 half-digit open-drain n-channel transistor outputs, suitable for directly driving common-anode LED displays at greater than 5mA per segment. These devices provide a brightness input which may be used digitally as a display enable, or with a potentiometer as a continuous display brightness control.

The counter section of all the devices in the CD-7224/CD-7225 family provides direct static counting from DC to 15 MHz, guaranteed, with a 5V ±10% supply over the operating temperature range. At normal ambient temperatures, the devices will typically count up to 25 MHz. The count input is provided with a Schmitt trigger to allow operation in noisy environments and correct counting with slowly changing inputs. These devices also provide count inhibit, store and reset circuitry which allows a direct interface with the ICM7207/A devices to implement a low cost, low power frequency counter with a minimum component count.

These devices also incorporate several features intended to simplify cascading four-digit blocks. The carry output allows the counter to be cascaded, while the leading zero blanking input and output allows correct leading zero blanking between four-decade blocks. The backplane driver of the LCD devices may be disabled, allowing the segments to be slaved to another backplane signal, which is necessary when using an eight or twelve digit, single backplane display. In LED systems, the brightness input to several CD-7225 devices may be ganged to one potentiometer.

All the devices in the CD-7224/ CD-7225 family are packaged in a standard 40-pin dual-in-line plastic package.

Table 1, the option matrix and ordering information, shows the four standard devices in the CD-7224/CD-7225 family and their markings, which serve as part numbers for ordering purposes.

ORDERING INFORMATION

Model	Display Compatibility	Count Option	Oper. Temp. Range	Package
CD-7224C	4½ Digit LCD	19999	−20°C to +70°C	40 pin Plastic DIP
CD-7224AC	4½ Digit LCD	15959	−20°C to +70°C	40 pin Plastic DIP
CD-7225C	4½ Digit LED	19999	−20°C to +70°C	40 pin Plastic DIP
CD-7225AC	4½ Digit LED	15959	−20°C to +70°C	40 pin Plastic DIP

CD-7224/CD-7225

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5 Watt @ 70° C
Supply Voltage (V^+-V^-) ..... 6.5 Volts
Input Voltage (Any Terminal) (Note 2) ..... V^+ +0.3V, V^- −0.3V
Operating Temperature Range ..... −20° C to +70° C
Storage Temperature Range ..... −55° C to +125° C

Absolute maximum ratings define stress limitations which, if exceeded, may permanently damage the device. These are not continuous duty ratings. For continuous operation these devices must be operated under the conditions defined under "Operating Characteristics."

OPERATING CHARACTERISTICS TABLE 2

(All Parameters measured with V^+-V^- = 5V unless otherwise indicated)

CD-7224 CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current	I_{op}	Test circuit, Display blank		10	50	μA
Operating supply voltage range	V_s	V^+-V^-	3	5	6	V
Oscillator input current	I_{OSL}	Pin 36		±2	±10	μA
Segment rise/fall time	t_{rfs}	C_{load} = 200pf		0.5		μs
Backplane rise/fall time	t_{rfb}	C_{load} = 5000pf		1.5		μs
Oscillator frequency	f_{osc}	Pin 36 Floating		16		KHz
Backplane frequency	f_{bp}	Pin 36 Floating		125		Hz

CD-7225 CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current display off	I_{OPQ}	Pin 5 (Brightness) at V^- Pins 29, 31-34 at V^+		10	50	μA
Operating supply voltage range	V_s	V^+-V^-	4	5	6	V
Operating current	I_{OP}	Pin 5 at V^+, Display 18888		200		mA
Segment leakage current	I_{SL}	Segment Off		±0.01	±1	μA
Segment on current	I_S	Segment On, Vout = V^- + 3V	5	8		mA
Half digit on current	I_H	Half digit on, Vout = V^- + 3V	10	16		mA

FAMILY CHARACTERISTICS

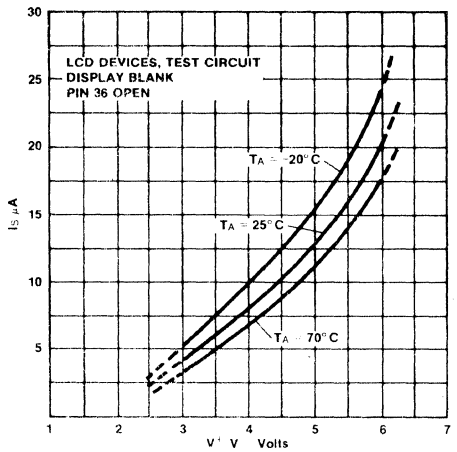
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pullup Currents	I_{PU}	Pins 29, 31, 33, 34 Vout = V^+- 3V		10		μA
Input High Voltage	V_{IH}	Pins 29, 31, 33, 34	3			V
Input Low Voltage	V_{IL}	Pins 29, 31, 33, 34			2	V
Count Input Threshold	V_{CT}			2		V
Count Input Hysteresis	V_{CH}			0.5		V
Output High Current	I_{OH}	Carry Pin 28 Leading Zero Out Pin 30 Vout = V^+ −3V	350	500		μA
Output Low Current	I_{DL}	Carry Pin 28 Leading Zero Out Pin 30 Vout = V^- +3V	350	500		μA
Count Frequency	f_{count}	4.5V > (V^+-V^-) > 6V	0		15	MHz
Store, Reset Minimum Pulse Width	t_S,t_R		3			μs

NOTE 1: This limit refers to that of the package and will not be obtained during normal operation.

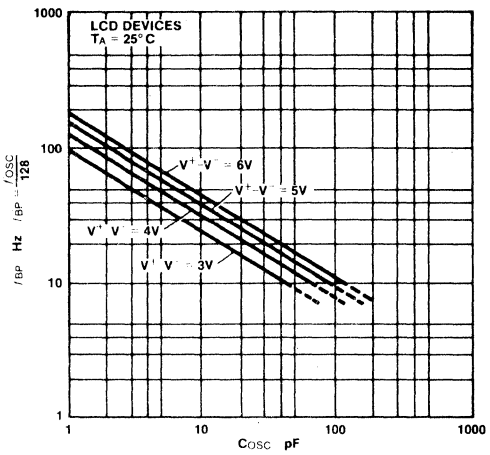
NOTE 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than V^+ or less than V^- may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the 7224/7225 be turned on first.

TYPICAL CHARACTERISTICS

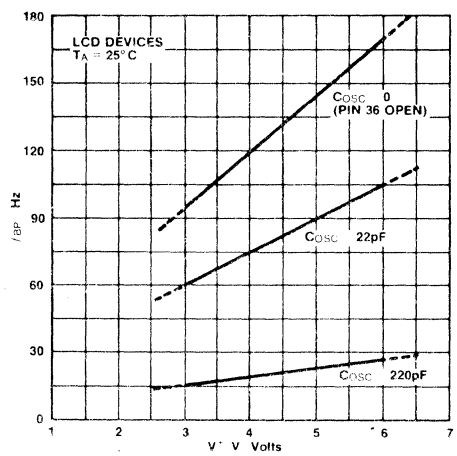
OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



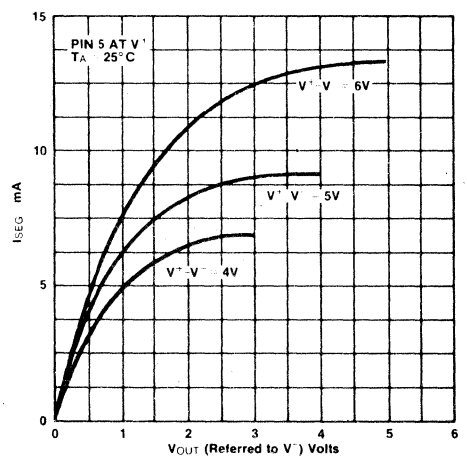
BACKPLANE FREQUENCY AS A FUNCTION OF OSCILLATOR CAPACITOR COSC



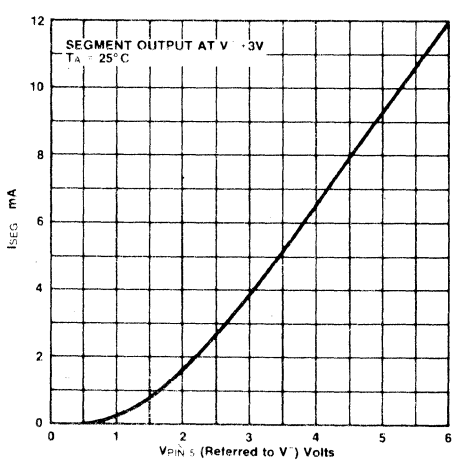
BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



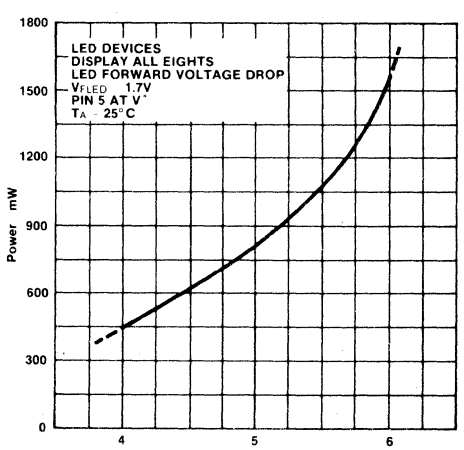
LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE



OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE



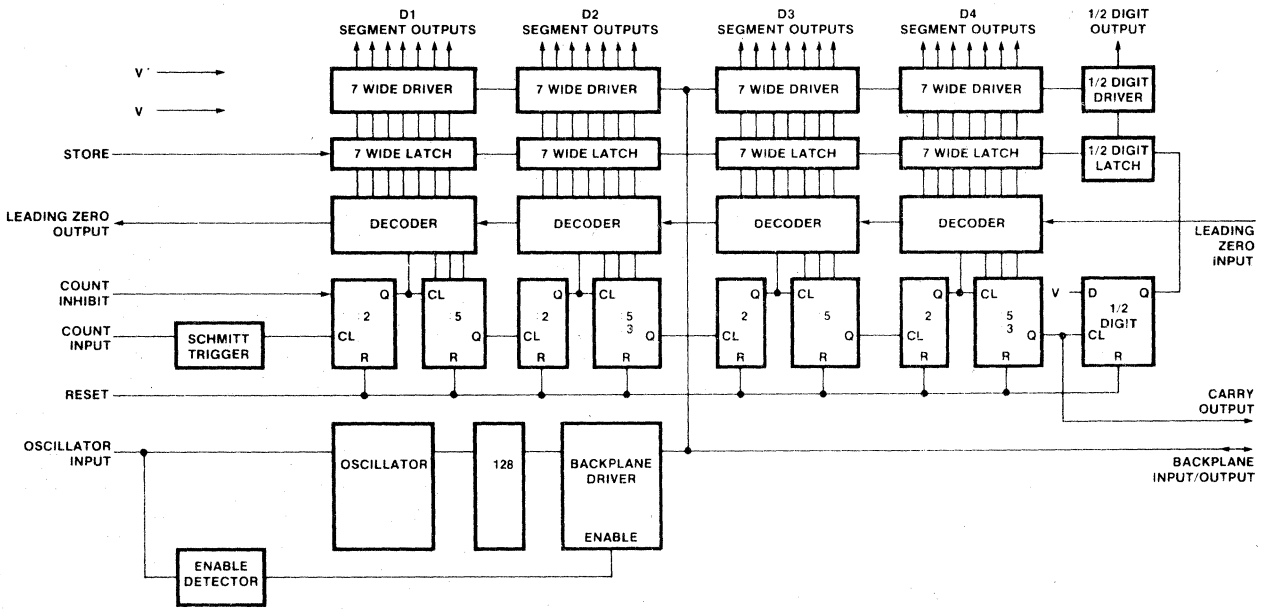
CONTROL INPUT DEFINITIONS

In this table, V^+ and V^- are considered to be normal operating input logic levels. Actual input low and high levels are specified in Table 2. For lowest power consumption, input signals should swing over the full supply.

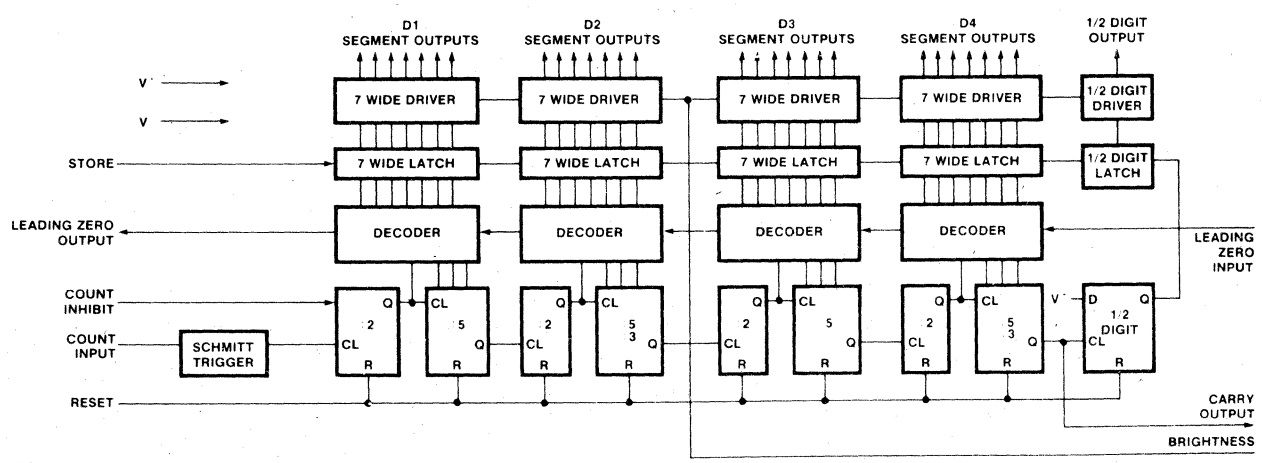
INPUT	TERMINAL	VOLTAGE	FUNCTION
Leading Zero Input	29	V^+ or Floating V^-	Leading Zero Blanking Enabled Leading Zeroes Displayed
Count Inhibit	31	V^+ or Floating V^-	Counter Enabled Counter Disabled
Reset	33	V^+ or Floating V^-	Inactive Counter Reset to 0000
Store	34	V^+ or Floating V^-	Output Latches not Updated Output Latches Updated

BLOCK DIAGRAMS

CD-7224 (A)

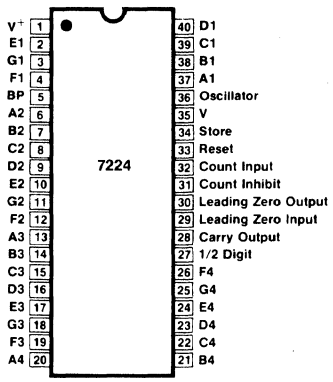


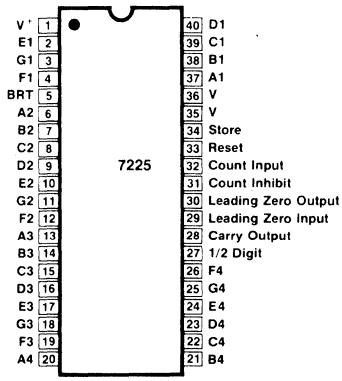
CD-7225 (A)



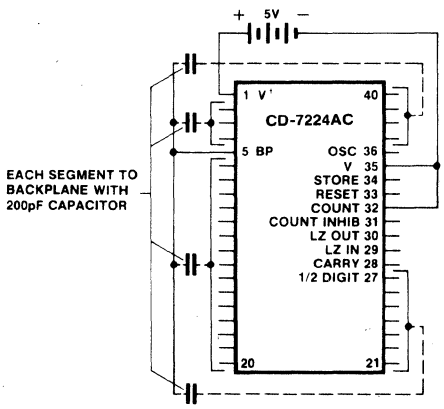
CD-7224/CD-7225

CONNECTION DIAGRAMS

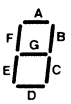




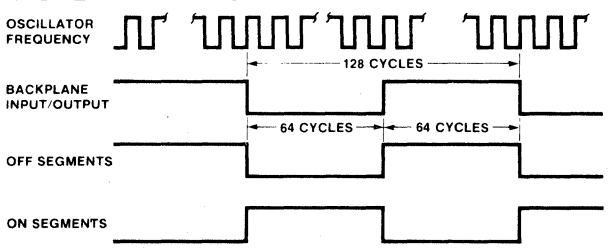
TEST CIRCUIT



SEGMENT ASSIGNMENT



DISPLAY WAVEFORMS



DESCRIPTION OF OPERATION

LCD Devices

The LCD devices in the family (7224C and 7224AC) provide outputs suitable for driving conventional four digit by seven segment LCD displays, including 29 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any dc component which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the oscillator input (pin 36) to the negative supply. This allows the 29 segment outputs to be synchronized directly to a signal input at the BP terminal (pin 5). In this manner, several slave devices may be cascaded to the backplane output of one master device or the backplane may be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device will represent a load of approximately 200 pF (comparable to one additional segment). The limitation on how many devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits, and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimize power consumption is to keep the rise and fall times less than about 5 microseconds. The backplane driver devices of one device should handle the backplane to a display of 16 one-half-inch characters without the rise and fall times exceeding 5μs (ie, 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the CD-7224 devices be slaved to it.

This external signal should be capable of driving very large capacitive loads with short (1-2 μs) rise and fall times. The maximum frequency for a backplane signal should be about 125Hz, although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 16KHz at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 125Hz with the oscillator free-running. The oscillator frequency may be reduced by connecting an external capacitor to the oscillator terminal (pin 36); see the plot of oscillator/backplane frequency vs. external capacitance for detailed information.

The oscillator may also be overdriven if desired, although care must be taken to insure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a d.c. component to the display). This

can be done by driving the oscillator input between the positive supply and a level out of the range where the backplane disable is sensed, about one fifth of the supply voltage above the negative supply. Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

LED Devices

The LED devices in the family (7225C and 7225AC) outputs suitable for directly driving four digit by seven segment common-anode LED displays, including 28 individual segment drivers and one half-digit driver, each consisting of a low-leakage current-controlled open-drain n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the Brightness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Fig (3). The potentiometer should be a high value (100kΩ to 1MΩ) to minimize I^2R power consumption, which can be significant when the display is off.

The brightness input may also be operated digitally as a display enable; when at V^+, the display is fully on, and at V^- fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two supplies at the Brightness input.

Note that the LED devices have two connections for V^-; both of these pins should be connected to the negative supply. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating the LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (−15mW/°C above 35°C). Power dissipation for the device is given by:

$$P = [(V^+ - V^-) - V_{FLED}]^* \times I_S \times N_S$$

where V_{FLED} is the LED forward voltage drop, I_S is segment current, and N_S is the number of "on" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the Brightness input to keep power dissipation within the limits described above.

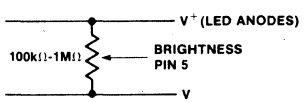


Figure 3: Brightness Control

COUNTER SECTION

The devices in the CD-7224/CD-7225 family implement a four digit ripple carry resetable counter, including a Schmitt trigger on the count input and a carry output. Also included is an extra D-type flip-flop, clocked by the carry signal and outputting to the half-digit segment driver, which can be used as either a true half-digit or as an overflow indicator. The counter will index on the negative-going edge of the signal at the count input, and the carry output will provide a negative-going edge following the count which indexes the counter from 9999 (or 5959) to 10000. Once the half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the Reset terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half digit is set, and subsequent carry outputs will not be affected.

A negative level at the Count Inhibit input disables the first divide-by-two in the counter chain without affecting its clock. This provides a true count inhibit which is not sensitive to the state of the count input, preventing false counts which can result from using a normal logic gate forcing the state of the clock to prevent counting.

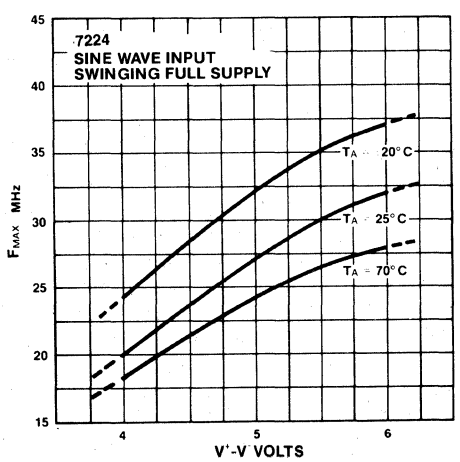
Each decade of counter drives directly into a four-to-seven decoder which derives the seven segment output code. Each decoder output corresponds to one segment terminal of the device. The output data is latched at the driver; when the Store pin is at a negative level, these latches are updated, and when the Store pin is left open or at a positive level, the latches hold their contents.

The decoders also include zero detect and blanking logic to provide leading zero blanking. When the leading zero input is floating or at a positive level, this circuitry is enabled and the device will blank leading zeroes. When the leading zero input is at a negative level, or the half digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The leading zero output is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked, which can only occur when the leading zero input is at a positive level and the half digit is not set.

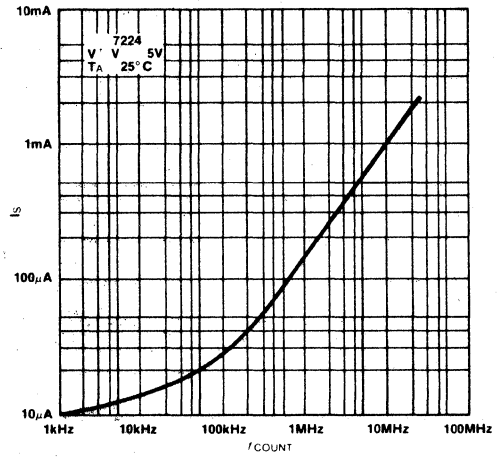
For example in an eight-decade counter with overflow using two CD-7224/CD-7225 devices, the leading zero output of the high order digit device would be connected to the leading zero input of the low order digit device. This will assure correct leading zero blanking for all eight digits.

The Store, Reset, Count Inhibit, and Leading Zero inputs are provided with pullup devices, so that they may be left open when a positive level is desired. The Carry and Leading Zero outputs are suitable for interfacing to CMOS logic in general, and are specifically designed to allow cascading of CD-7224 or CD-7225 devices in four digit blocks.

MAXIMUM COUNT FREQUENCY (TYPICAL) AS A FUNCTION OF SUPPLY VOLTAGE

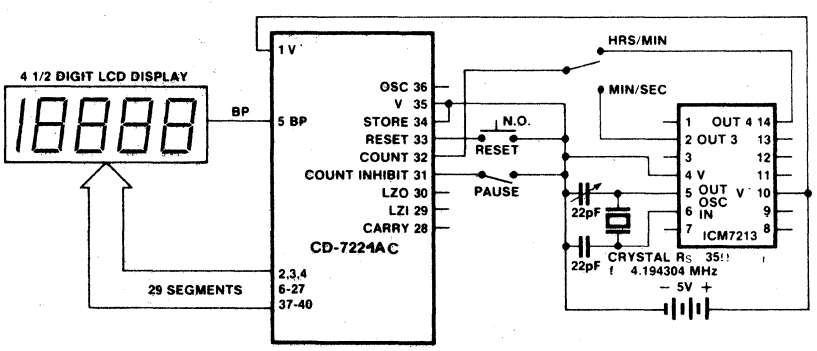


SUPPLY CURRENT AS A FUNCTION OF COUNT FREQUENCY

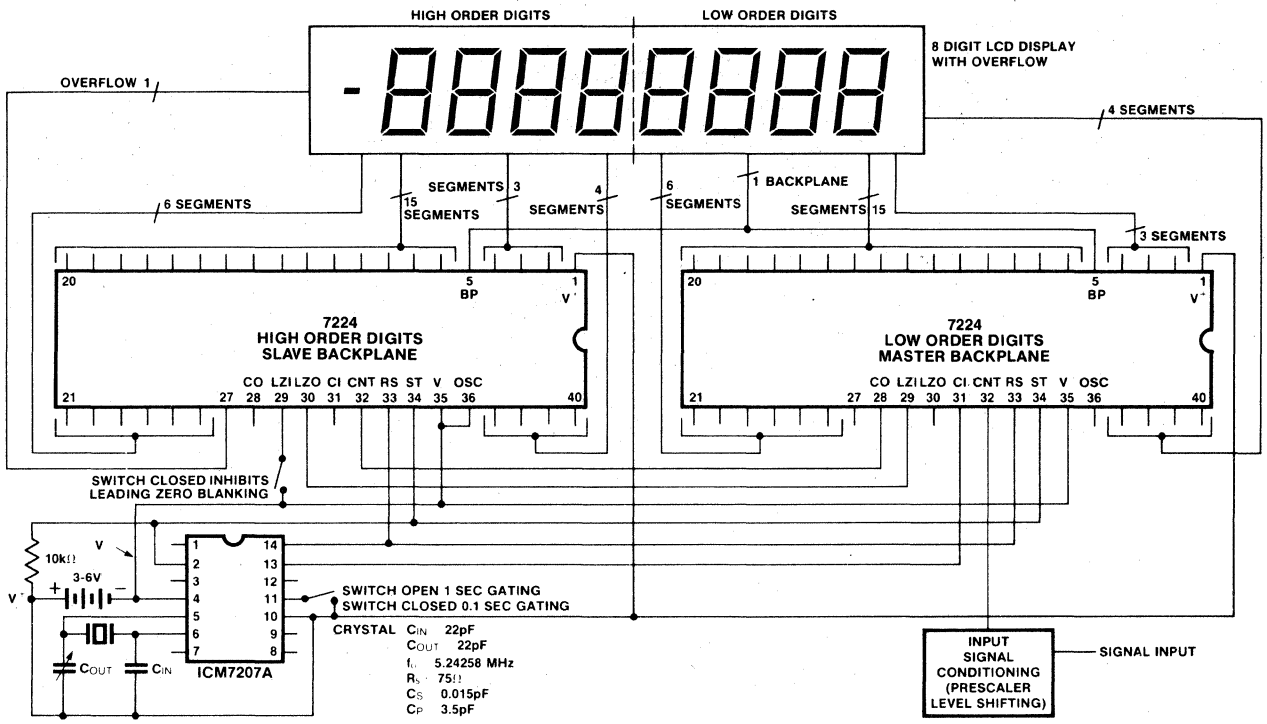


APPLICATIONS

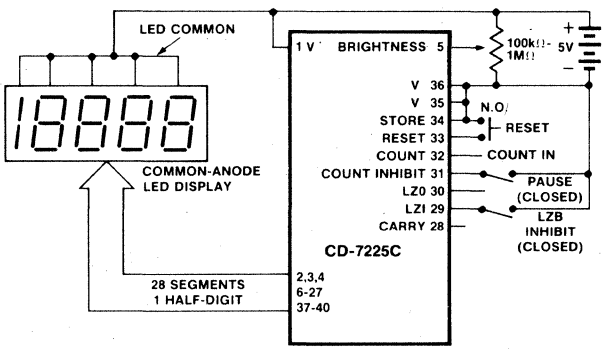
1. Two-Hour Precision Timer



2. Eight-Digit Precision Frequency Counter

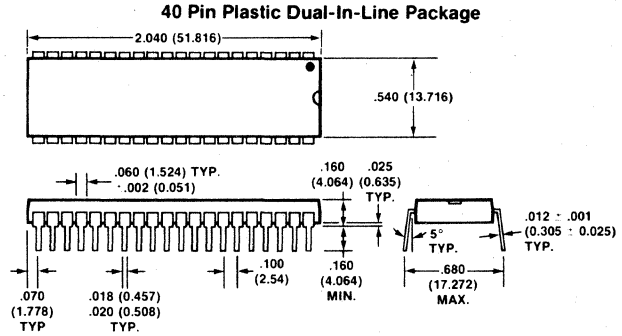


3. Unit Counter



PACKAGE DIMENSIONS

40 Pin Plastic Dual-In-Line Package



CD-7226A/B
10 MHz Universal Counter System

CD-7226A Drives Common Anode LED's
CD-7226B Drives Common Cathode LED's

FEATURES

- **Functions as a frequency counter, period counter, unit counter, frequency ratio counter or time interval counter**
- **Output drivers directly drive both digits and segments of large 8 digit LED displays. Both common anode and common cathode versions are available**
- **Measures frequencies from DC to 10 MHz**
- **Measures period from 0.5μ sec to 10 sec**
- **Stable high frequency oscillator, uses either 1MHz or 10MHz crystal**
- **Control signals available for gating of prescalers and prescaler display logic**
- **Multiplexed BCD outputs**
- **All terminals protected against static discharge; no special handling precautions required**

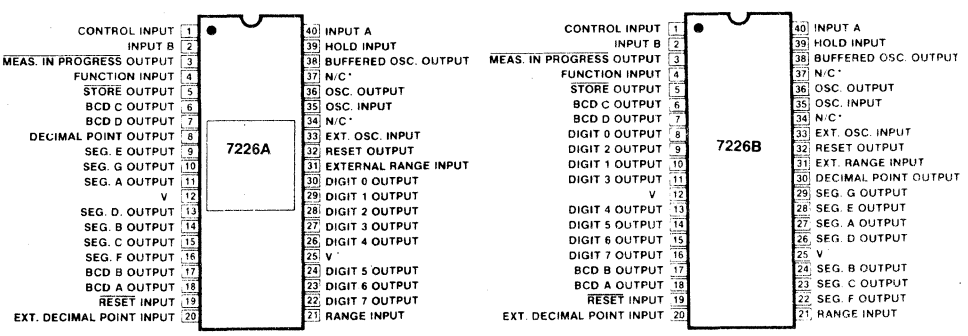
GENERAL DESCRIPTION

The CD-7226 is a fully integrated Universal Counter and LED display driver. It combines a high frequency oscillator, a decade timebase counter, an 8 decade data counter and latches, a 7 segment decoder, digit multiplexer and 8 segment and 8 digit drivers which can directly drive large LED displays. The counter inputs accept a maximum frequency of 10MHz in frequency and unit counter modes and 2MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The CD-7226 can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or as a totalizing counter. The counter uses either a 10MHz or 1MHz crystal timebase. An external timebase input is also provided. For period and time interval, the 10MHz timebase gives a 0.1μsec resolution. In period average and time interval average, the resolution can be in the nanosecond range. In the frequency mode, the user can select accumulation time of .01 sec, .1 sec, 1 sec and 10 sec. With a 10 sec accumulation time, the frequency can be displayed to a resolution of .1 Hz in the least significant digit. There is 0.2 second interval between measurements in all ranges. Control signals are provided to enable gating and storing of prescaler data.

Leading zero blanking has been incorporated with frequency displayed in KHz and time in usec. The display is multiplexed at a 500Hz rate with a 12.5% duty cycle for each digit. The CD-7226A is designed for common anode display with typical peak segment currents of 25mA. The CD-7226B is designed for common cathode displays with typical segment currents of 12mA. In the display off mode both digit drivers & segment drivers are turned off allowing the display to be used for other functions.

PIN CONFIGURATION



*FOR MAXIMUM FREQUENCY STABILITY, CONNECT TO V^+ OR V^-

CD-7226A/B

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage (V^+-V^-) ..... 6.5 volts
Maximum Digit Output Current 400mA
Maximum Segment Output Current 60mA
Voltage on any Input or Output Terminal (Note 2) ..... Not to exceed V^+-V^- by more than ±0.3 volts
Maximum Power Dissipation at ..... 1.0 watts (7226A)
70° C (Note 1) ..... 0.5 watts (7226B)
Maximum Operating Temperature Range ..... −20° C to +70° C
Maximum Storage Temperature Range ..... −55° C to +125° C

Absolute maximum ratings refer to values that if exceeded may destroy or permanently change the device. The device is guaranteed for continous operation only under the conditions defined under the section TYPICAL OPERATING CHARACTERISTICS.

Note 1: The 7226 may be triggered into a destructive latchup mode if either input signals are applied before the power supply is applied or if input or outputs are forced to voltages exceeding V^+-V^- by more than 0.3 volts.

ELECTRICAL CHARACTERISTICS V^+-V^- = 5.0V, Test Circuit, T_A = 25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Operating Supply Current	I_{DD}	Display Off Unused inputs to V^-		2	5	mA
Supply Voltage Range		−20° C < T_A < 70° C Input A, Input B Frequency at F_{MAX}	4.75		6.0	volts
Maximum Guaranteed Frequency Input A, Pin 40	F_{AMAX}	−20° C < T_A < 70° C 4.75V < V^+-V^- < 6.0V Figure 1 Function = Frequency, Ratio, Unit Counter Function = Period, Time Interval	 10 2.5	 14	 	 MHz MHz
Maximum Frequency Input B, Pin 2	F_{BMAX}	−20° C < T_A < 70° C 4.75V < V^+ −V^- < 6.0V Figure 2	2.5			MHz
Minimum Separation Input A to Input B Time Interval Function		−20° C < T_A < 70° C 4.75V < V^+ −V^- < 6.0V Figure 3	250			nsec
Maximum osc. freq. and ext. osc. freq. Minimum ext. osc. freq.		−20° C < T_A < 70° C 4.75V < V^+ −V^- < 6.0V	10		 100	MHz kHz
Oscillator Transconductance	gm	V^+ −V^- = 4.75V T_A = +70° C	2000			μS
Multiplex Frequency Time Between Measurements	F_{MAX}	f_{osc} = 10 MHz f_{osc} = 10 MHz		500 200		Hz msec

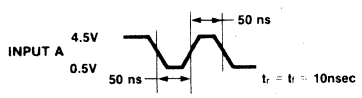


Figure 1: Waveform for Guaranteed Minimum F_{AMAX} Function = Frequency, Frequency Ratio, Unit Counter.

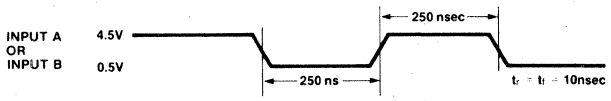


Figure 2: Waveform for Guaranteed Minimum F_{BMAX} and F_{AMAX} for Function = Period and Time Interval.

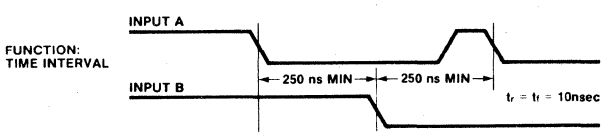


Figure 3: Waveform for Minimum Time Between Transitions of Input A and Input B.

For single or "one-shot" time interval measurements, Input A then Input B must have a high to low transition prior to the interval which is to be measured. Provisions for "priming" the circuit as described above must be made using external circuitry. For repetitive signals this occurs automatically.

CD-7226A/B

ELECTRICAL CHARACTERISTICS = $V^+ - V^-$ = 5.0V, test circuit, T_A = 25°C, unless otherwise specified.

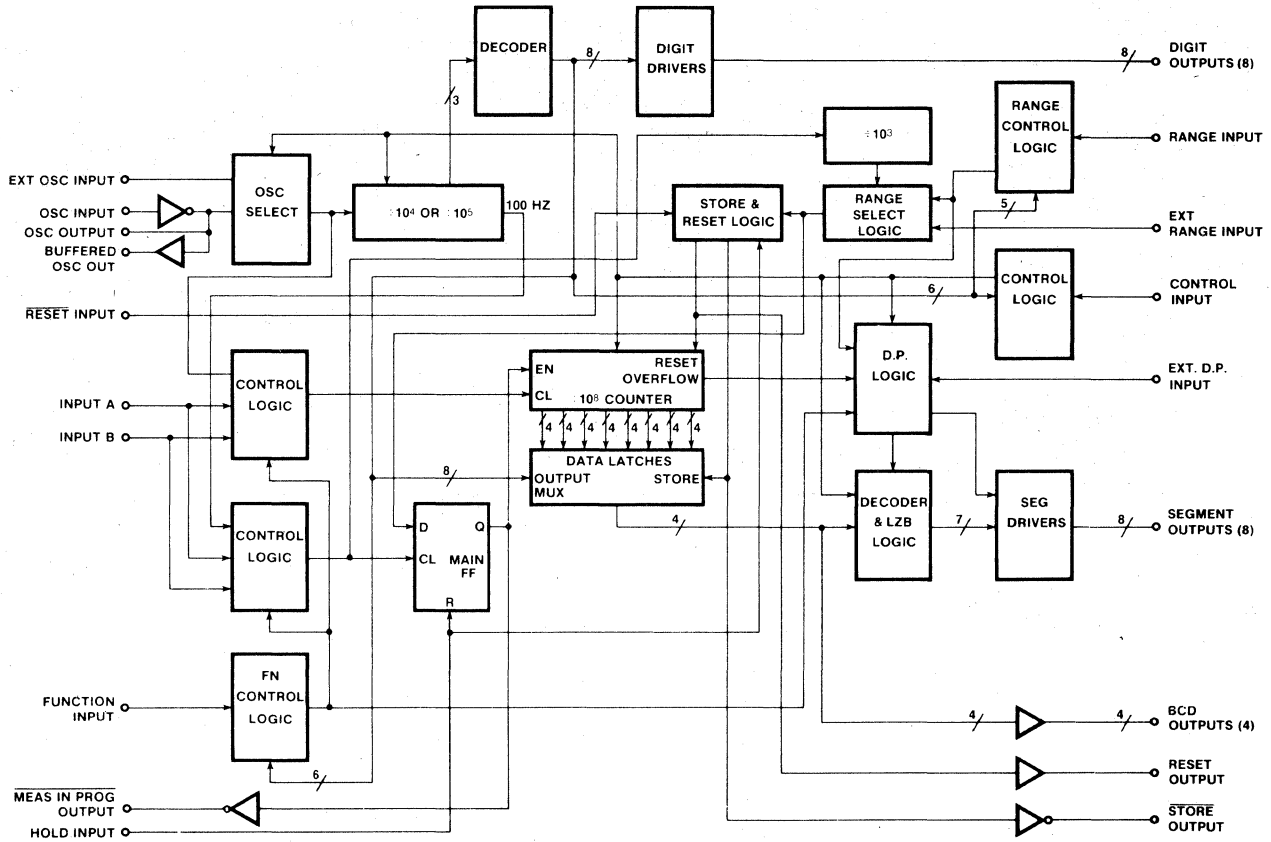
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
INPUT VOLTAGES PINS 2,19,33,39,40 input low voltage input high voltage	 V_{IL} V_{IH}	 −20°C < T_A < +70°C Referred to V^-	 1.0	 	 3.5	 V V
PIN 2, 39, 40 INPUT LEAKAGE, A,B	I_L				20	μA
PIN 33 input low voltage input high voltage	 V_{IL} V_{IH}	 −20°C < T_A < 70°C Referred to V^-	 .8	 	 2.0	 V V
Input resistance to V^+ PINS 19,33	 R	 V_{IN} = V^+ −1.0V.	 100	 400	 	 kΩ
Input resistance to V^- PIN 31	 R	 V_{IN} = V^- +1.0V	 50	 100	 	 kΩ
Output Current PINS 3,5,6,7,17,18,32,38	 I_{OL}	 V_{OL} = V^- +0.4V	 .40	 	 	 mA
PINS 5,6,7,17,18,32	I_{OH}	V_{OH} = V^- +0.4V	100			μA
PINS 3,38	I_{OH}	V_{OH} = V^+ −.8V	265			μA
7226A DIGIT DRIVER PINS 22,23,24,26,27,28,29,30 high output current low output current	 I_{OH} I_{OL}	 V_{out} = V^+ −2.0V V_{out} = V^- +1.0V	 150	 180 −.3	 	 mA mA
SEGMENT DRIVER PINS 8,9,10,11,13,14,15,16 low output current high output current	 I_{OL} I_{OH}	 V_{out} = V^- +1.5 V_{out} = V^+ −1.0V	 25	 35 100	 	 mA μA
MULTIPLEX INPUTS PINS 1,4,20,21 input low voltage input high voltage	 V_{IL} V_{IH}	 Referred to V^-	 2.0	 	 .8 	 V V
Input Resistance to V−	R	V_{IN} = V^- +1.0V	50	100		kΩ
7226B DIGIT DRIVER PINS 8,9,10,11,13,14,15,16 low output current high output current	 I_{OL} I_{OH}	 V_{out} = V^- +1.0V V_{out} = V^+ −2.5V	 50	 75 100	 	 mA μA
SEGMENT DRIVER PINS 22,23,24,26,27,28,29,30 high output current leakage current	 I_{OH} I_L	 V_{out} = V^+ −2.0V V_{out} = V^-	 10	 15	 10	 mA μA
MULTIPLEX INPUTS PINS 1,4,20,21 input low voltage input high voltage	 V_{IL} V_{IH}	 	 V^+ −.8	 	 V^+ −2.0	 V V
input resistance to V^+	R	V_{IN} = V^+ −1.0V	200	360		kΩ

ORDERING INFORMATION

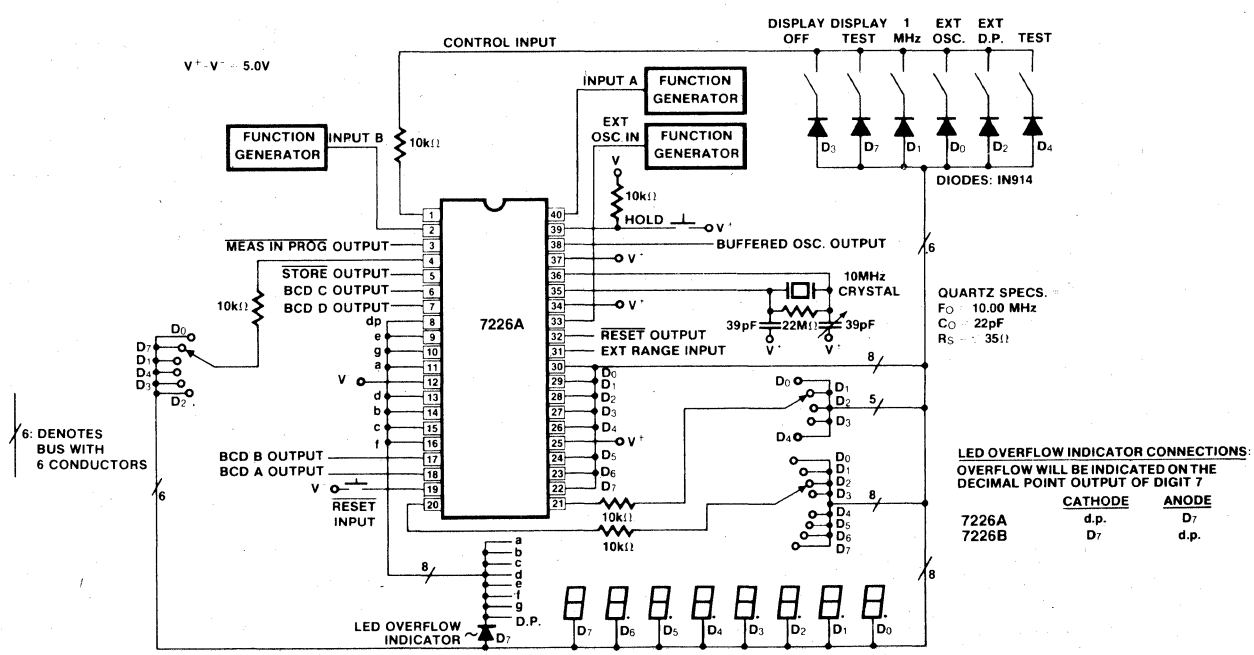
Model	Display Option	Oper. Temp. Range	Package
CD-7226AC	Common Anode	−20°C to +70°C	40 pin Cerdip
CD-7226BC	Common Cathode	−20°C to +70°C	40 pin Plastic DIP

CD-7226A/B

BLOCK DIAGRAM



TEST CIRCUIT



APPLICATION NOTES

GENERAL

Inputs A & B

The signal to be measured is input at Input A in Frequency, Period, Unit Counter, Frequency Ratio and Time Interval modes. The other input signal to be measured is input at Input B in Frequency Ratio and Time Interval. In Frequency Ratio F_A should be larger than F_B.

Both inputs are digital inputs with a typical switching threshold of 2.0V at $V^+ = 5.0V$. For optimum performance the peak to peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from TTL logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs.

Note: The amplitude of the input should not exceed the supply by more than .3 volt otherwise, the circuit may be damaged.

Multiplexed Inputs

The function, range, control and external decimal point inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate digit driver output to the inputs. The input function, range and control inputs must be stable during the last half of each digit output, (typically 125 μsec). The multiplex inputs are active high for the common anode CD-7226A and active low for the common cathode CD-7226B.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the unit counter mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10K resistor should be placed in series with the multiplex inputs as shown in the application notes.

Table 1 shows the functions selected by each digit for these inputs.

TABLE 1

	FUNCTION	DIGIT
FUNCTION INPUT PIN 4	Frequency	D_0
	Period	D_7
	Frequency Ratio	D_1
	Time Interval	D_4
	Unit Counter	D_3
	Oscillator Frequency	D_2
RANGE INPUT PIN 21	.01 Sec/1 Cycle	D_0
	.1 Sec/10 Cycles	D_1
	1 Sec/100 Cycles	D_2
	10 Sec/1k Cycles	D_3
External Range Input PIN 31	Enabled	D_4
CONTROL INPUT PIN 1	Blank Display	D_3&Hold
	Display Test	D_7
	1MHz Select	D_1
	External Oscillator Enable	D_0
	External Decimal Point Enable	D_2
	Test	D_4
EXTERNAL DECIMAL POINT INPUT, PIN 20	Decimal Point is Output for Same Digit That is Connected to This Input	

Control Input Functions

Display Test - All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be blanked if Display Off is selected at the same time.

Display Off - To enable the Display Off mode it is necessary to input D_3 to the control input and have the HOLD input at V^+. The chip will remain in the Display Off mode until HOLD is switched back to V^-. While in the Display Off mode, the segment and digit driver outputs are open. During Display Off the oscillator continues to run with a typical supply current of 1.5mA with a 10MHz crystal and no measurements are made. In addition, inputs to the multiplexed inputs will have no effect. A new measurement is initiated when the HOLD input is switched to V^-.

1MHz Select - The 1MHz select mode allows use of a 1MHz crystal with the same digit multiplex rate and time between measurements as with a 10MHz crystal. The decimal point is also shifted one digit to the right in Period and Time Interval, since the least significant digit will be in μsecond increments rather than 0.1 μsec increments.

External Oscillator Enable - In this mode the external oscillator input is used instead of the on chip oscillator for the Timebase input and Main Counter input in Period and Time interval modes. The on chip oscillator will continue to function when the external oscillator is selected, but will have no effect on circuit operation. The external oscillator input frequency must be greater than 100KHz or the chip will reset itself to enable the on chip oscillator.

External Decimal Point Enable - When external decimal point is enabled a decimal point will be displayed whenever the digit driver connected to the external decimal point is active. Leading Zero Blanking will be disabled for all digits following the decimal point.

Test Mode - In the test mode the main counter is split into groups of two digits each and the groups are clocked in parallel. The reference counter is split such that the clock into the reference count goes directly to the clock of the third decade counter (10 sec/1k cycle range). Store is also enabled so the count in the main counter is continuously output.

Range Input - The range input selects whether the measurement is made for 1, 10, 100, 1000 counts of the reference counter or if the external range input determines the measurement time. In all functional modes except Unit Counter a change in the range input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the Range Input is changed.

Function Input - The six functions that can be selected are: Frequency, Period, Time Interval, Unit Counter, Frequency Ratio and Oscillator Frequency.

These functions select which signal is counted into the main counter and which signal is counted by the reference counter as shown in Table 2. In Time Interval a flip flop is toggled first by a $1 \rightarrow 0$ transition at Input A and then by a $1 \rightarrow 0$ transition at Input B. The oscillator is gated into the Main Counter from the time Input A toggles the flip flop until Input B gates the flip flop. A change in the function input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the Function Input is changed. If main counter overflows, an overflow indication is output on the decimal point output during D7.

TABLE 2

DESCRIPTION	MAIN COUNTER	REFERENCE COUNTER
Frequency (F_A)	Input A	100Hz (Oscillator ÷ 10^5 or 10^4)
Period (T_A)	Oscillator	Input A
Ratio (F_A/F_B)	Input A	Input B
Time Interval (A→B)	Osc•Time Interval FF	Time Interval FF
Unit Counter(Count A)	Input A	Not Applicable
Osc. Freq. (Fosc)	Oscillator	100Hz (Osc ÷ 10^5 or 10^4)

External Decimal Point Input - when the external decimal point is selected this input is active. Any of the digits, except D_7, can be connected to this point. D_7 should not be used since it will overide the overflow output and leading zeros will remain unblanked after the decimal point.

Hold Input - Except in the Unit counter mode when the Hold Input is at V^+, any measurement in progress is stopped, the main counter is reset and the chip is held ready to initiate a new measurement. The latches which hold the main counter data are not updated so the last complete measurement is displayed. In Unit counter mode when Hold Input is at V^+ the counter is stopped but not reset. When Hold is changed to V^- the count continues from where the counter stopped.

$\overline{\text{Reset}}$ Input - The $\overline{\text{Reset}}$ Input is the same as a Hold Input, except the latches for the main counter are enabled, resulting in an output of all zeros.

External Range Input - The External Range Input is used to select different ranges than those provided on the chip. Figure 4 shows the relationship between Measurement In Progress and External Range Input.

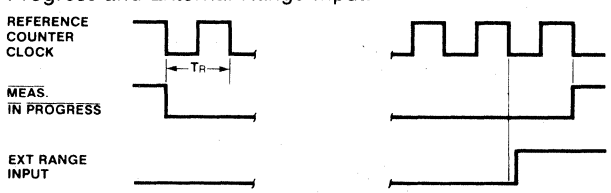


Figure 4: External Range Input to End of Measurement in Progress.

$\overline{\text{Measurement In Progress}}$, $\overline{\text{Store}}$ and $\overline{\text{Reset}}$ Outputs - These outputs are provided to enable display of prescaler digits. Figure 5 shows the relationship between these signals during the time between measurements. All three outputs can drive a low power Schottky TTL load. The $\overline{\text{Measurement In Progress}}$ Output can directly drive an ECL load, if the ECL device is powered from the same power supply as the 7226.

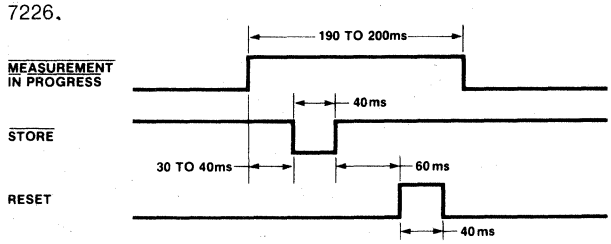


Figure 5: Reset, $\overline{\text{Store}}$, and $\overline{\text{Measurement in Progress}}$ Outputs Between Measurements.

BCD Outputs - The BCD representation of each digit output is output on the BCD outputs. Leading zero blanking of the display has no effect on the BCD output. Each BCD output will drive one low power Schottky TTL load. Table 3 shows the truth table for the BCD outputs.

TABLE 3 Truth Table BCD Outputs

NUMBER	D PIN 7	C PIN 6	B PIN 17	A PIN 18
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Buffered Oscillator Output - The Buffered Oscillator Output has been provided to enable use of the on chip oscillator signal without loading the oscillator itself. This output will drive one low power Schottky TTL load. Care should be taken to minimize capacitive loading on this pin.

DISPLAY CONSIDERATIONS

The display is multiplexed at a 500Hz rate with a digit time of 244 μsec. An interdigit blanking time of 6 μsec is used to prevent ghosting between digits. The decimal point and leading zero blanking have been implemented for right hand decimal point displays. Any zeros following the decimal point will not be blanked. Also, the leading zero blanking will be disabled if the Main Counter overflows. The decimal point has been implemented to display frequency in KHz and time in μsec.

The 7226A is designed to drive common anode LED displays at peak current of 25mA/segment, using displays with V_F = 1.8V at 25mA. The average DC current will be over 3mA under these conditions. The 7226B is designed to drive common cathode displays at peak current of 15mA/ segment using displays with V_F = 1.8V at 15mA. Resistors can be added in series with the segment drivers to limit the display current in very efficient displays, if required. Figures 6, 7, 8 and 9 show the digit and segment currents as a function of output voltage for common anode and common cathode drivers.

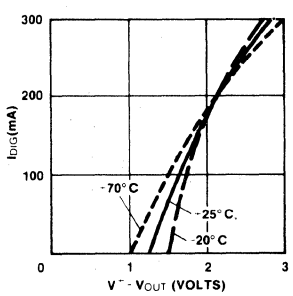


Figure 6: 7226B Typical I_{SEG} Vs. $V^+ - V_{out}$
$4.5 \leq V^+ - V^- \leq 6.0V$

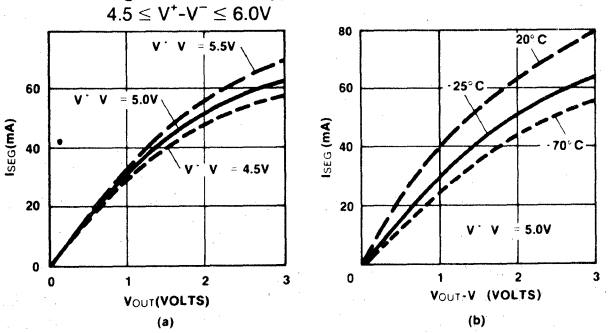


Figure 7: 7226B Typical I_{SEG} Vs. $V^+ - V_{out}$

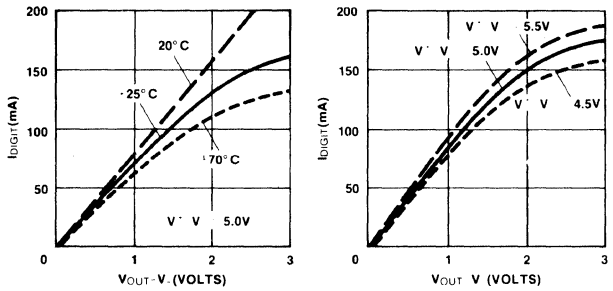


Figure 8: 7226B Typical I_{DIGIT} Vs. $V_{OUT}-V^-$

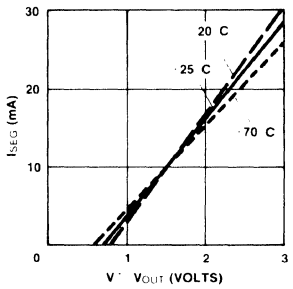
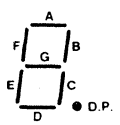


Figure 9: 7226B Typical I_{SEG} Vs. V^+-V_{out}
$4.5V \leq V^+-V^- \leq 6.0V$

To increase the light output from the displays, V^+ may be increased up to 6.0V, however, care should be taken to see that maximum power and current ratings are not exceeded.

The segment and digit outputs in both the 7226A and B are not directly compatible with either TTL or CMOS logic. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals.

Segment Identification



ACCURACY

In a Universal Counter crystal drift and quantization errors cause errors. In Frequency, Period and Time Interval Modes, a signal derived from the oscillator is used in either the Reference Counter or Main Counter. Therefore, in these modes an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/° C will cause a measurement error of 20ppm/° C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the Frequency Mode the maximum accuracy is obtained with high frequency inputs and in Period Mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 10, the least accuracy will be obtained at 10 KHz. In Time Interval measurements there is a maximum error of 1 count per interval. As a result there is the same inherent accuracy in all ranges as shown in Figure 11. In Frequency Ratio measurement more accuracy can be obtained by averaging over more cycles of Input B as shown in Figure 12.

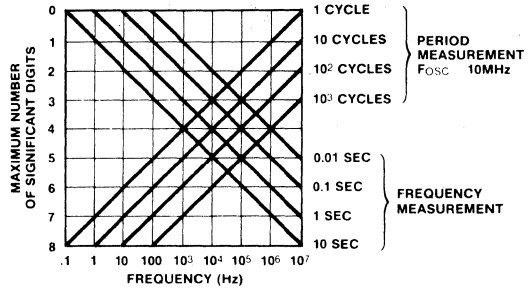


Figure 10: Maximum Accuracy of Frequency and Period Measurements Due to Limitations of Quantization Errors.

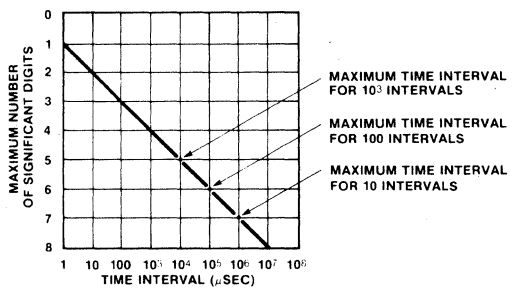


Figure 11: Maximum Accuracy of Time Interval Measurement Due to Limitations of Quantization Errors.

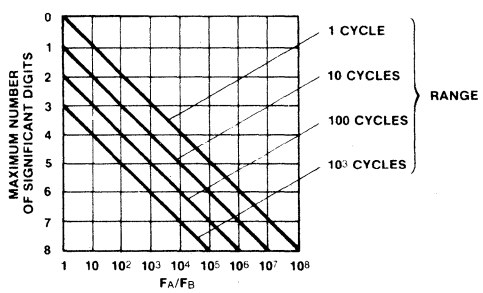


Figure 12: Maximum Accuracy for Frequency Ratio Measurement Due to Limitations of Quantization Errors.

CIRCUIT APPLICATIONS

The 7226 has been designed to be used as a complete Universal Counter or with prescalers and other circuitry in a variety of applications. Since Input A and Input B are digital inputs additional circuitry will be required in many applications for input buffering, amplification, hysteresis, and level shifting to obtain the required digital voltages. For many applications an FET source follower can be used for input buffering and an ECL 10116 line receiver can be used for amplification and hysteresis to obtain a high impedance input, sensitivity and bandwidth. However, cost and complexity of this circuitry can vary widely depending upon the sensitivity and bandwidth required. When TTL prescalers or input buffers are used, pull up resistors to V^+ should be used to obtain optimal voltage swing at Inputs A and B.

If prescalers aren't required the 7226 can be used to implement a minimum component Universal counter as shown in figure 13. This circuit can be for input frequencies up to 10MHz at Input A and 2MHz at Input B.

For input frequencies up to 40 MHz the circuit shown in figure 14 can be used to implement a Frequency and Period Counter. To obtain the correct value when measuring

frequency and period it is necessary to divide the 10MHz oscillator frequency down to 2.5MHz. In doing this the time between measurements is also lengthened to 800 msec. and the display multiplex rate is decreased to 125 Hz.

If the input frequency is prescaled by ten then the oscillator frequency can remain at 10 or 1MHz, but the decimal point must be moved. Figure 15 shows use of a ÷10 prescaler in frequency counter mode. Additional logic has been added to have the 7226 count the input directly in Period mode for maximum accuracy. Note that Input A comes from Q_C rather than Q_D to obtain an input duty cycle of 40%. If an output without a duty cycle near 50% must be used then it may be necessary to use a 74121 monostable multivibrator or similar circuit to stretch the input pulse to guarantee a 50 nsec minimum pulse width.

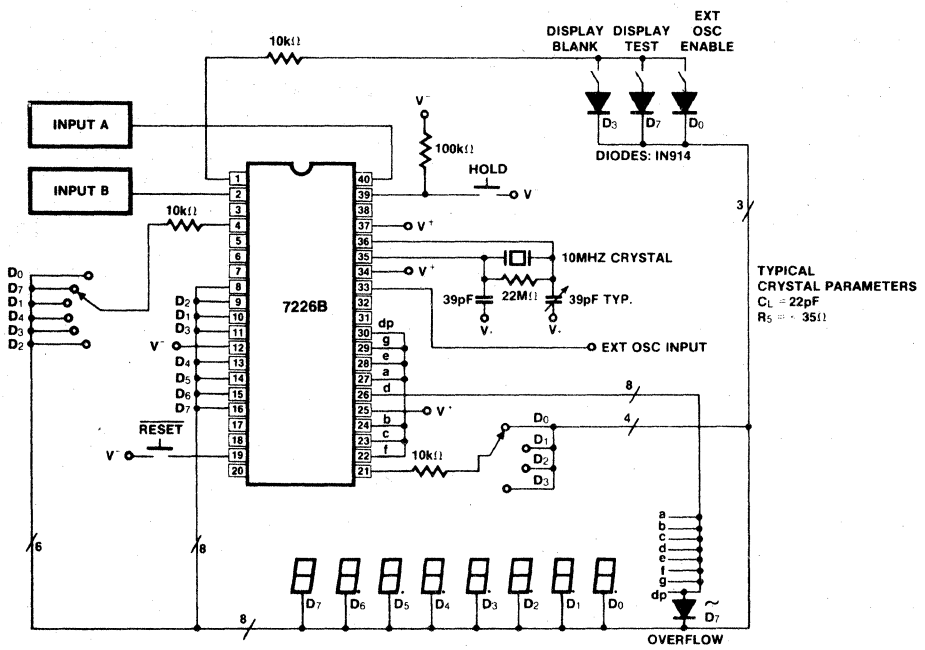
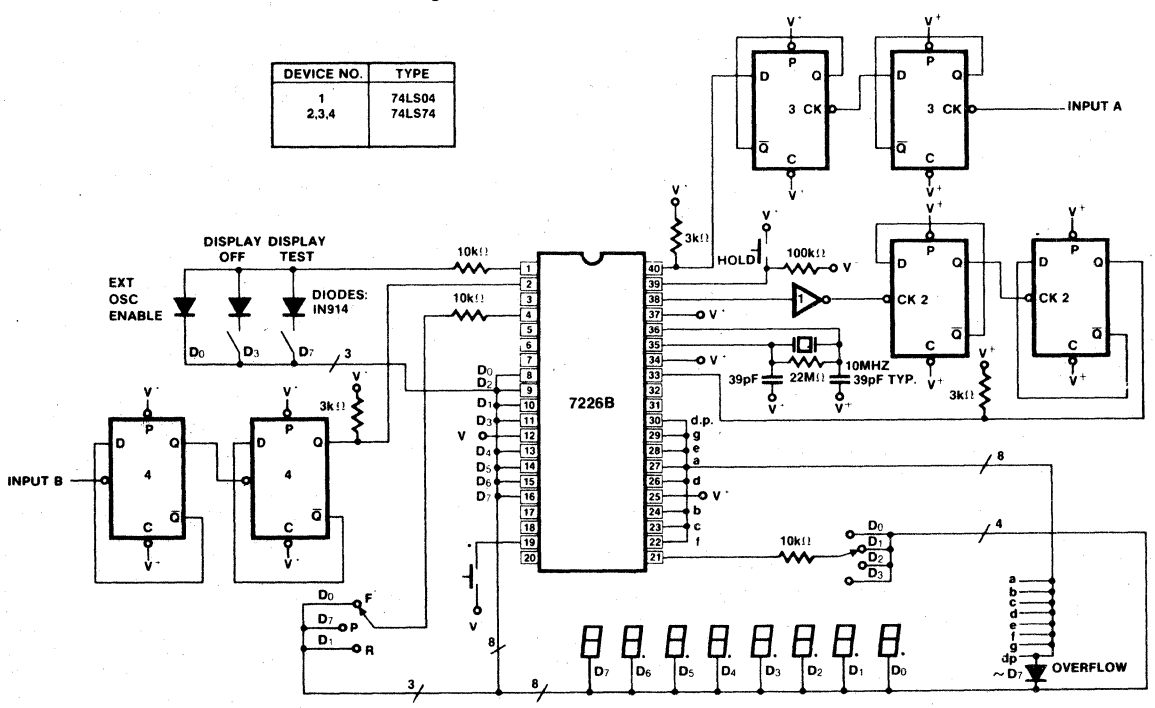


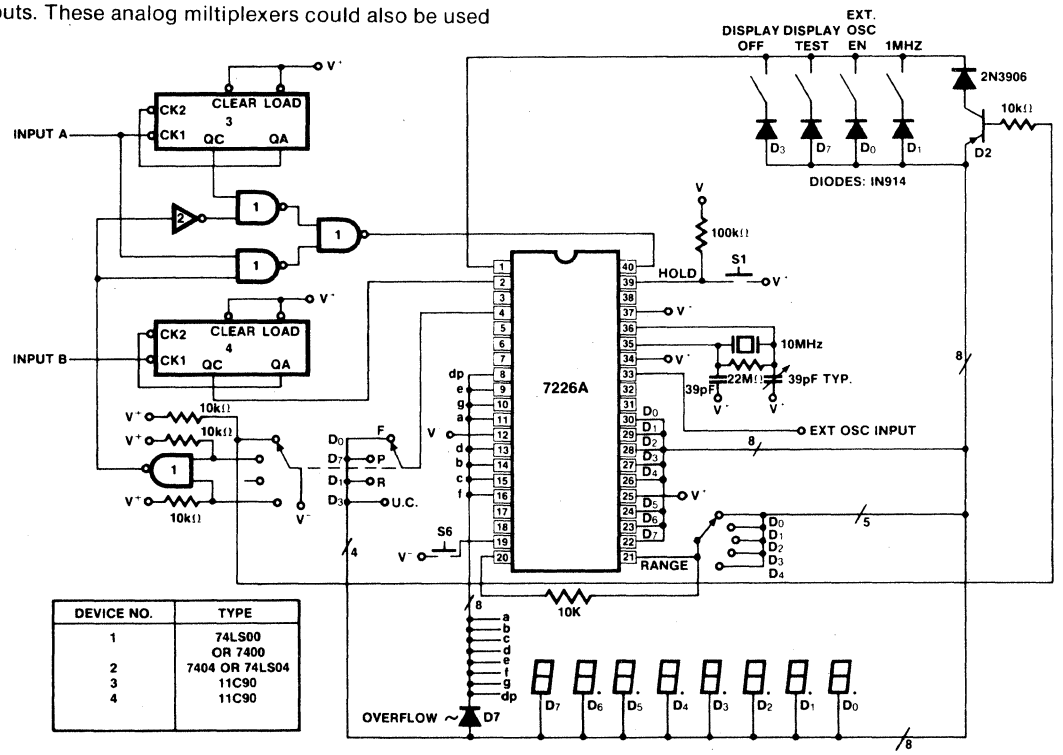
Figure 13: 10MHz Universal Counter



Notes: 1) If a 2.5MHz crystal is used then diode D1 and I.C's 1 and 2 can be eliminated.

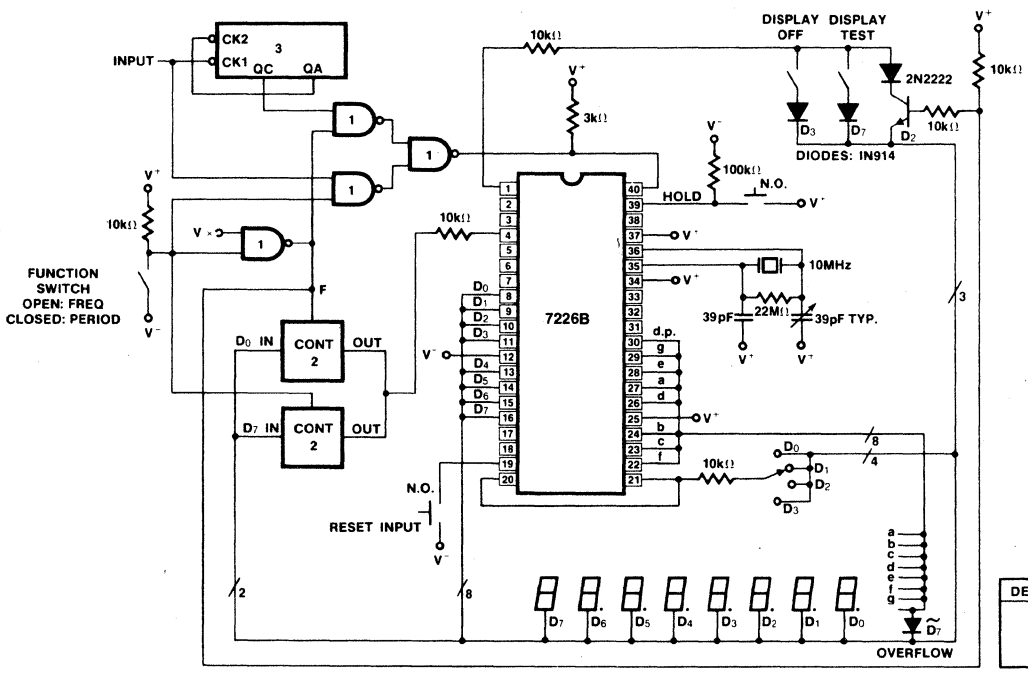
Figure 14: 40MHz Frequency, Period Counter

Figure 16 shows the use of a CD4016 analog multiplexer to multiplex the digital outputs back to the Function Input. Since the CD4016 is a digitally controlled analog transmission gate no level shifting of the digit output is required. CD4051's or CD4052's could also be used to select the proper inputs for the multiplexed input on the 7226 from 2 or 3 bit digital inputs. These analog miltiplexers could also be used in systems in which the mode of operation is controlled by a microprocessor rather than directly from front panel switches. TTL multiplexers such as the 74153 or 74251 could also be used, but some additional circuitry will be required to convert the digit output to TTL compatible logic levels.



DEVICE NO.	TYPE
1	74LS00 OR 7400
2	7404 OR 74LS04
3	11C90
4	11C90

Figure 15: 100MHz Multi Function Counter



DEVICE NO.	TYPE
1	7400 OR 74LS00
2	CD4016
3	11C90

Figure 16: 100MHz Frequency Period Counter

If the prescaler information needs to be displayed, then the Measurement in Progress, Store and Reset outputs from the CD-7226 can be used to control the prescaler and data latch as shown in figure 17. Note that the output of IC 7 has been decoded with a NAND to obtain a 40% duty cycle for the signal into input A.

To obtain a full Universal Counter with prescalers with the count displayed, it is necessary to add significantly more circuitry to implement the Time External Mode as shown in figure 18.

All of the circuits shown directly drive a multiplexed LED display, however, the BCD outputs can be used with external BCD to 7 segment decoders and appropriate level shifting to drive other types of displays.

FIGURE 17
9 DIGIT MULTIFUNCTION COUNTER

DEVICE	TYPE
1,5	74LS04
2	7404
3	74S00
4	74LS00
6	11C90
7,8	75S112
9	7477
10	7446

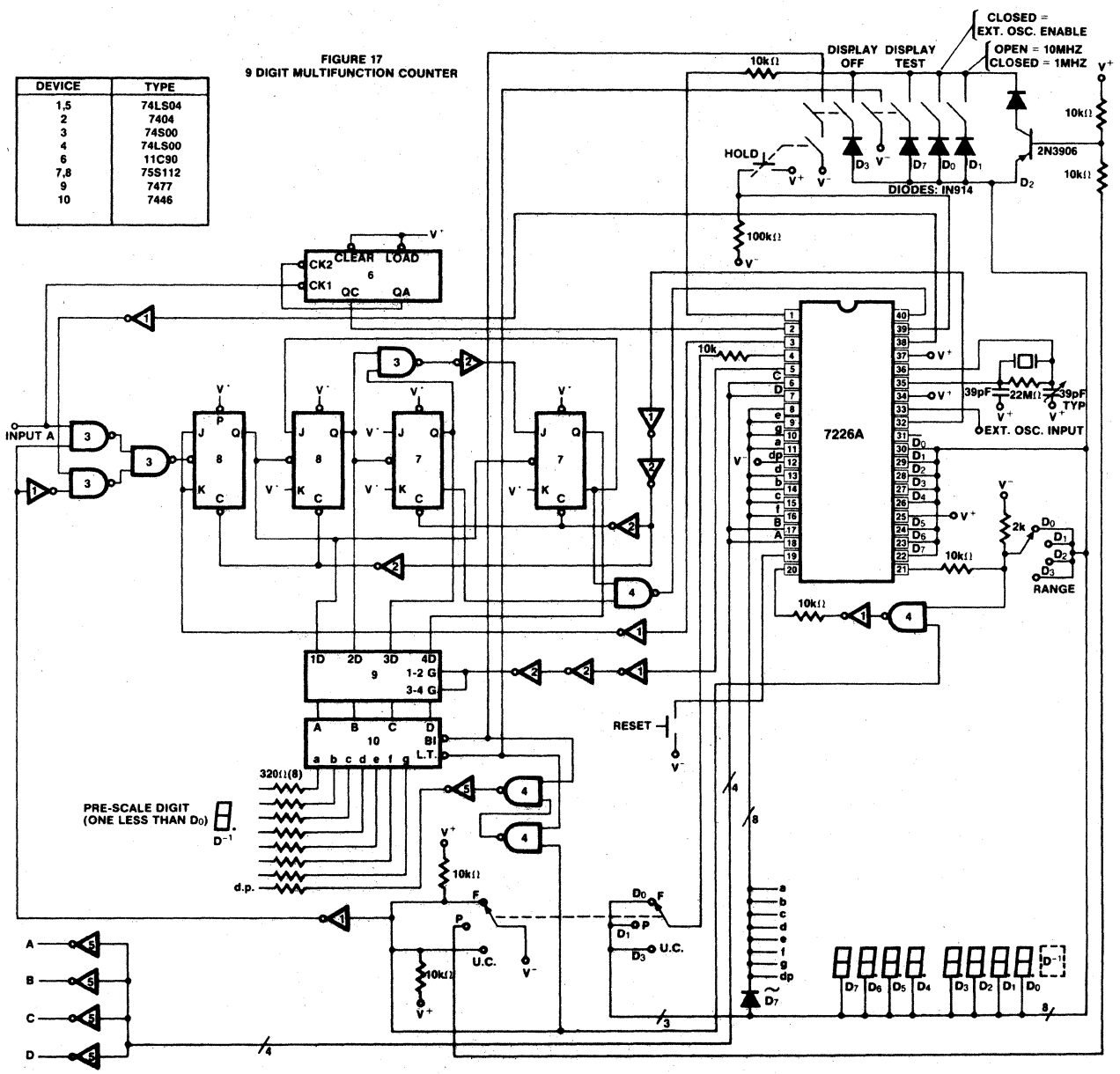


Figure 17: 9 Digit Multi Function Counter

DEV. #	TYPE
1,2,5	74LS04 OR CD4049
3,9	74S04
4	74LS10
6,7,10	74S00
8	74S10
11	74LS80
12,13,14	74S112 OR 74S114
15	7477
16	7446

FIGURE 18
9 DIGIT UNIVERSAL COUNTER

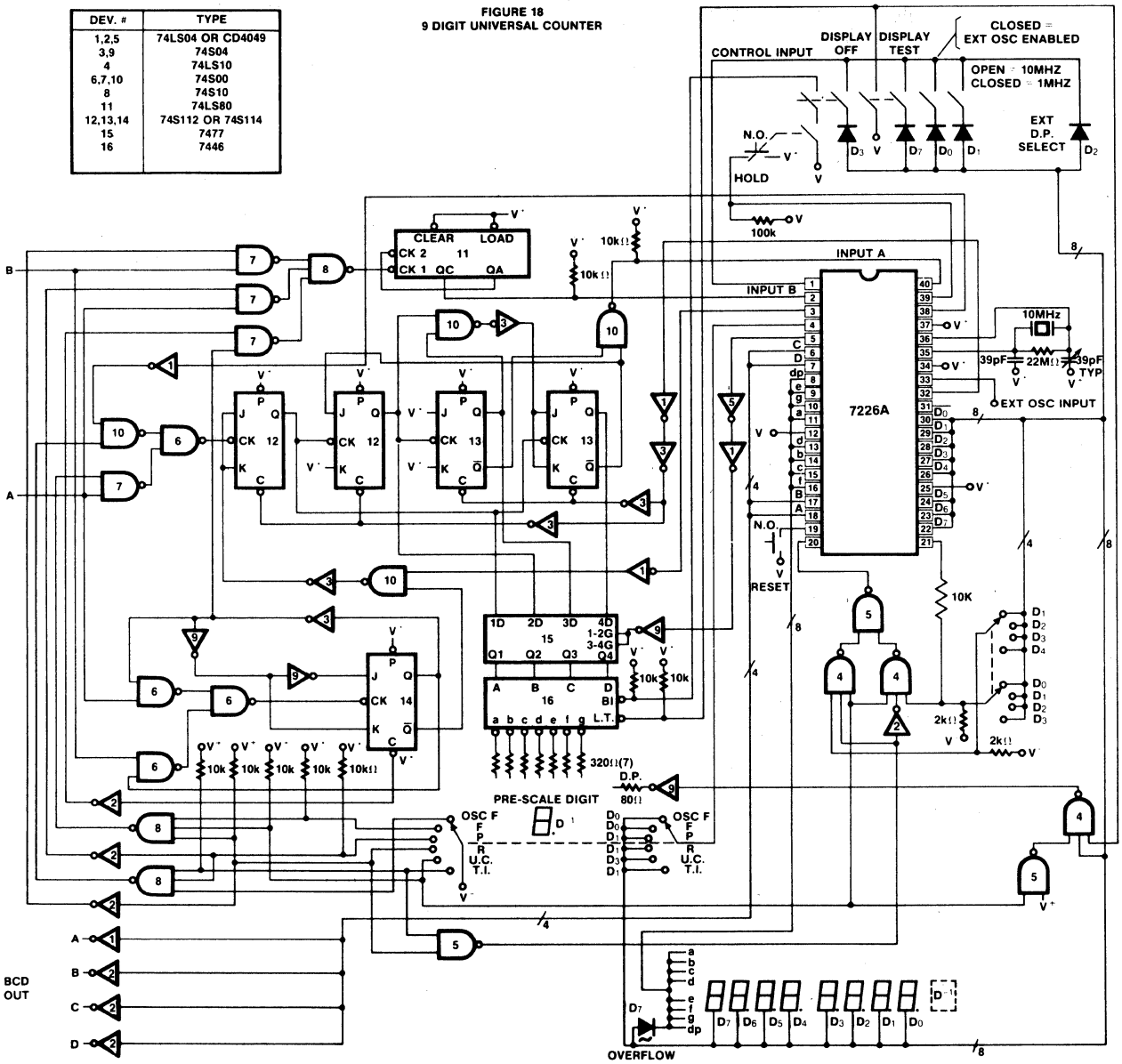
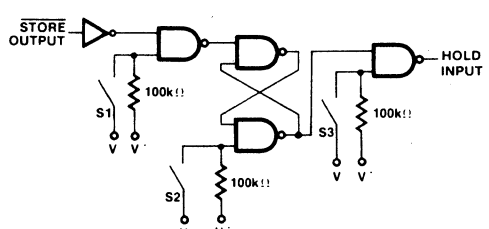


Figure 18: 9 Digit Universal Counter

The circuit shown in figure 19 can be used in any of the circuit applications shown to implement a single measurement mode of operation. This circuit uses the Store output to put the 7226 into a hold mode. The Hold input can also be used to reduce the time between measurements. The circuit shown in Figure 20 puts a short pulse into the Hold input a short time after Store goes low. A new measurement wil be initiated at the end of the pulse on the Hold Input. This circuit reduces the time between measurements to less than 40 msec from 200 msec. Use of the circuit shown in Figure 20 on the circuit shown in Figure 14 will reduce the time between measurements from 800 msec. to 1600 msec.



SWITCH	FUNCTION
S1	OPEN SINGLE MEAS MODE ENABLED
S2	CLOSED INITIATE NEW MEASUREMENT
S3	CLOSED HOLD INPUT

Figure 19: Single Measurement Circuit for Use With 7226

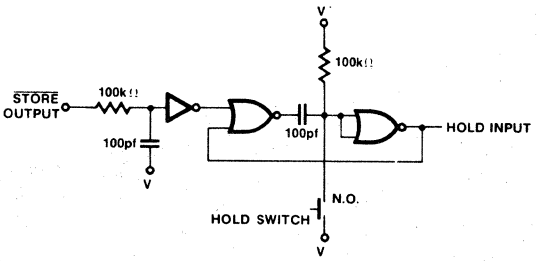


Figure 20: Circuit for Reducing Time Between Measurements

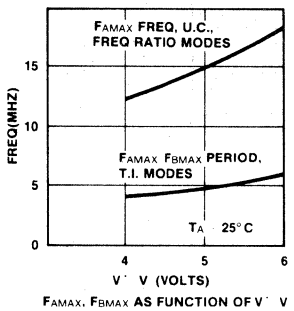


Figure 21: Typical Operating Characteristics

OSCILLATOR CONSIDERATIONS

The oscillator has been implemented as a high gain complementary FET inverter. An external resistor of 10MΩ or 22MΩ should be connected between the oscillator input and output to provide biasing. The oscillator is designed to work with a parallel resonance of 10 MHz quartz crystal with a static capacitance of 22pF and a series resistance of less than 35 ohms.

For a specific crystal and load capacitance, the required g_m can be calculated as follows:

$$g_m = \omega^2 \, Cin \, Cout \, Rs \left(1+\frac{Co}{C_L}\right)^2$$

where $C_L = \left(\frac{CinCout}{Cin+Cout}\right)$

Co = Crystal static capacitance
Rs = Crystal Series Resistance
Cin = Input Capacitance
$Cout$ = Output Capacitance
$\omega = 2\pi f$

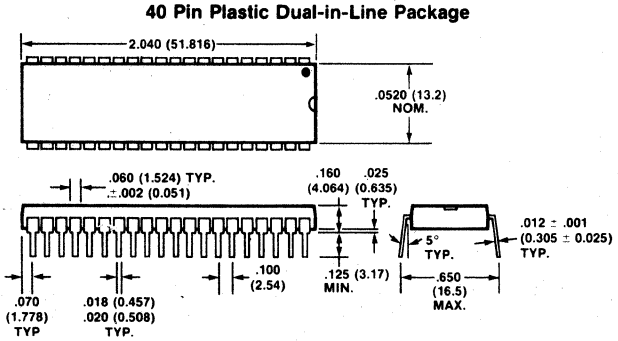
The required g_m should exceed the g_m specified for the 7226 by at least 50% to insure reliable startup. The oscillator input and output pins each contribute about 5pf to Cin and Cout. For maximum frequency stability, Cin and Cout should be approximately twice the specified crystal static capacitance.

In cases where non decade prescalers are used it may be desirable to use a crystal which is neither 10MHz. In that case, both the multiplex rate and time between measurements will be different. The multiplex rate is $f_{max} = \frac{f_{osc}}{2x10^4}$ for 10MHz mode and $f_{max} = \frac{f_{osc}}{2x10^3}$ for the 1MHz mode. The time between measurements is $\frac{2x10^6}{f_{osc}}$ in the 10MHz mode and $2x10^5$ in the 1MHz mode. The buffered oscillator output should be used for an oscillator test point or to drive additional logic. This output will drive one low power Schottky TTL load. When the buffered oscillator output is used to drive CMOS or to drive the external oscillator input, a 10kΩ resistor should be added from buffered oscillator output to V^+.

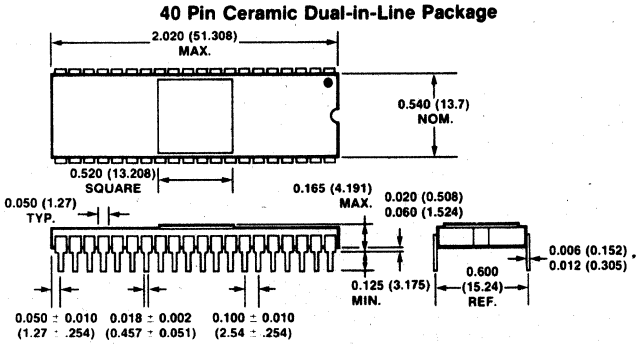
The crystal and oscillator components should be located as close to to the chip as practical to minimize pickup from other signals. In particular, coupling from the Buffered Oscillator Output and External Oscillator Input to the oscillator output or input can cause undesirable shifts in oscillator frequency. To minimize this coupling, pins 34 and 37 should be connected to V^+ or V^- and these two signals should be kept away from the oscillator circuit.

PACKAGE DIMENSIONS

40 Pin Plastic Dual-in-Line Package



40 Pin Ceramic Dual-in-Line Package



DD-7211 (LCD)
DD-7212 (LED)
Four Digit Display Decoder-Drivers

DD-7211 (LCD) FEATURES

- **Four digit non-multiplexed 7 segment LCD display outputs with backplane driver.**
- **Complete onboard RC oscillator to generate backplane frequency.**
- **Backplane input/output allows simple synchronization of slave-device segment outputs with a master backplane signal.**
- **DD-7211 devices provide separate digit select inputs to accept multiplexed BCD input (Pinout and functionally compatible with Siliconix DF411).**
- **D-7211M devices provide data and digit select code input latches controlled by chip select inputs to provide a direct high speed processor interface.**
- **DD-7211 device for binary-to-hexadecimal decoding; DD-7211A device for binary-to-EHLP-dash-blank decoding.**

DD-7212 (LED) FEATURES

- **28 current-limited segment outputs provide 4 digit non-multiplexed direct LED drive at > 5mA per segment.**
- **Brightness input allows direct control of LED segment current with a single potentiometer, or can function digitally as a display enable.**

FAMILY FEATURES

- **All devices fabricated using high density CMOS LSI technology for very low-power, high-performance operation.**
- **All inputs fully protected against static discharge; no special handling precautions necessary.**

DESCRIPTION

THE DD-7211(LCD) and DD-7212(LED) devices constitute a family of non-multiplexed four digit seven segment display decoder-drivers.

The DD-7211 devices are configured to drive conventional LCD displays, by providing a complete (no external components necessary) RC oscillator, divider chain, backplane driver devices, and 28 segment outputs. These outputs provide the zero d.c. component signals necessary for long display life.

The DD-7212 devices are configured to drive common-anode LED displays, providing 28 current-controlled low leakage open-drain n-channel outputs. These devices provide a Brightness input which may be used at normal logic levels as a display enable, or with a potentiometer as a continuous display brightness control.

Both the LCD and LED devices are available with two input configurations. The basic devices provide four data-bit inputs and four digit select inputs. This configuration is suitable for interfacing with multiplexed BCD or binary output devices, such as the CD-7217 or CD-7226. The microprocessor interface devices provide data input latches and digit select code latches under control of high-speed chip select inputs. These devices simplify the task of implementing a cost-effective alphanumeric 7 segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

The standard devices available will provide two different decoder configurations. The basic device will decode the four bit binary input into a seven-segment alphanumeric hexa-decimal output. The "A" versions will provide the same output code as the DD-7218 "Code B", i.e., 0-9, E, H, L, P, dash, blank. Either device will correctly decode true BCD to seven segment decimal outputs.

All devices in the DD-7211/7212 family are packaged in a standard 40 pin plastic dual-in-line package.

Table 1, the option matrix and ordering information, shows the 8 standard devices of the DD-7211/7212 family and their markings, which serve as part numbers for ordering purposes.

ORDERING INFORMATION

ORDER PART NUMBER		OUTPUT CODE	INPUT CONFIGURATIONS
LCD DISPLAY	DD-7211C	HEXADECIMAL	MULTIPLEXED 4-BIT
	DD-7211AC	CODE B	
	DD-7211MC	HEXADECIMAL	MICROPROCESSOR INTERFACE
	DD-7211AMC	CODE B	
LED DISPLAY	DD-7212C	HEXADECIMAL	MULTIPLEXED 4-BIT
	DD-7212AC	CODE B	
	DD-7212MC	HEXADECIMAL	MICROPROCESSOR INTERFACE
	DD-7212AMC	CODE B	

DD-7211/DD-7212

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5 Watt @ 70° C
Supply Voltage (V^+-V^-) ..... 6.5 Volts
Input Voltage (Any Terminal) (Note 2) ..... V^+ +0.3V, V^- −0.3V
Operating Temperature Range ..... −20° C to +70° C
Storage Temperature Range ..... −55° C to +125° C

Absolute maximum ratings define stress limitations which, if exceeded, may permanently damage the device. These are not continuous duty ratings. For continuous operation these devices must be operated under the conditions defined under "Operating Characteristics."

TABLE 2: OPERATING CHARACTERISTICS

All parameters measured with V^+-V^- = 5V

DD-7211 CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_S	V^+-V^-	3	5	6	V
Operating Current	I_{op}	Test circuit, Display blank		10	50	μA
Oscillator Input Current	I_{OSL}	Pin 36		±2	±10	μA
Segment Rise/Fall Time	t_{rfs}	C_{load} = 200pf		0.5		μs
Backplane Rise/Fall Time	t_{rfb}	C_{load} = 5000pf		1.5		μs
Oscillator Frequency	f_{osc}	Pin 36 Floating		16		kHz
Backplane Frequency	f_{bp}	Pin 36 Floating		125		Hz

DD-7212 CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_S	V^+-V^-	4	5	6	V
Operating Current Display Off	I_{OPQ}	Pin 5 (Brightness) at V^- Pins 27-34		10	50	μA
Operating Current	I_{OP}	Pin 5 at V^+, Display all 8's		200		mA
Segment Leakage Current	I_{SL}	Segment Off		±0.01	±1	μA
Segment On Current	I_S	Segment On, Vout = V- +3V	5	8		mA

INPUT CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Logical "1" input voltage	V_{IH}	Referred to V^-	3			V
Logical "0" input voltage	V_{IL}	Referred to V^-			2	V
Input leakage current	I_{DL}	Pins 27-34		±.01	±1	μA
Input capacitance	C_{In}	Pins 27-34		5		pF
BP/Brightness input leakage	I_{LBPI}	Measured at pin 5 with Pin 36 at V^-		±.01	±1	μA
BP/Brightness input capacitance	C_{BPI}	All Devices		200		pF
AC CHARACTERISTICS - MULTIPLEXED INPUT CONFIGURATION						
Digit Select Active Pulse Width	t_{sa}	Refer to Timing Diagrams	1			μs
Data Setup Time	t_{ds}		500			ns
Data Hold Time	t_{dh}		200			ns
Inter-Digit Select Time	t_{ids}		2			μs
AC CHARACTERISTICS - MICROPROCESSOR INTERFACE						
Chip Select Active Pulse Width	t_{csa}	other chip select either held active, or both driven together	200			ns
Data Setup Time	t_{dsm}		100			ns
Data Hold Time	t_{dhm}		10	0		ns
Inter-Chip Select Time	t_{ics}		2			μs

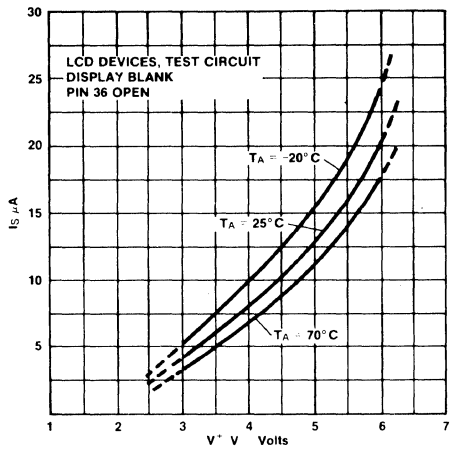
NOTE 1: This limit refers to that of the package and will not be obtained during normal operation.

NOTE 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than V^+ or less than V^- may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the 7211/7212 be turned on first.

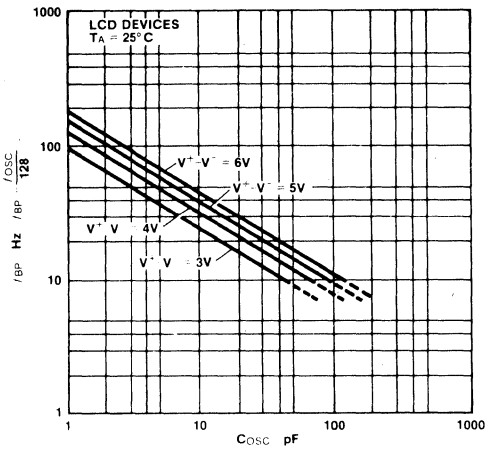
DD-7211/DD-7212

TYPICAL CHARACTERISTICS

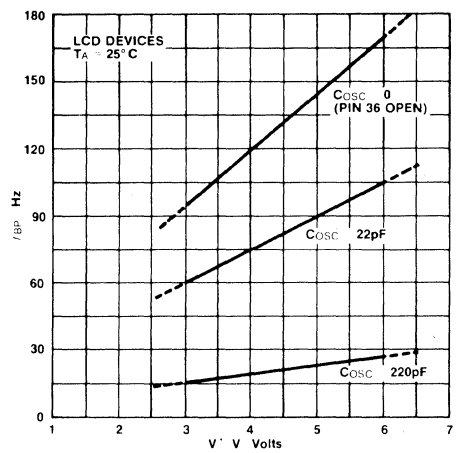
OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



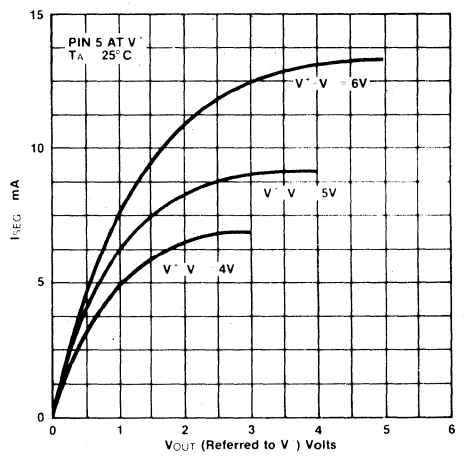
BACKPLANE FREQUENCY AS A FUNCTION OF OSCILLATOR CAPACITOR COSC



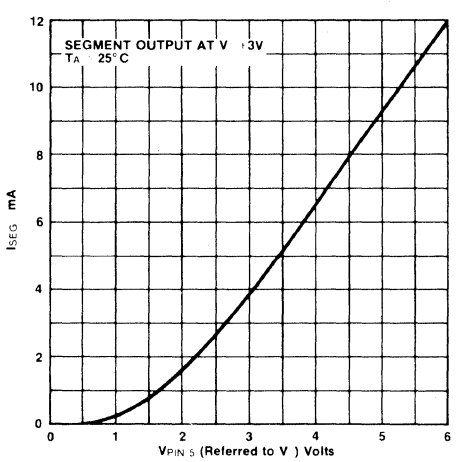
BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



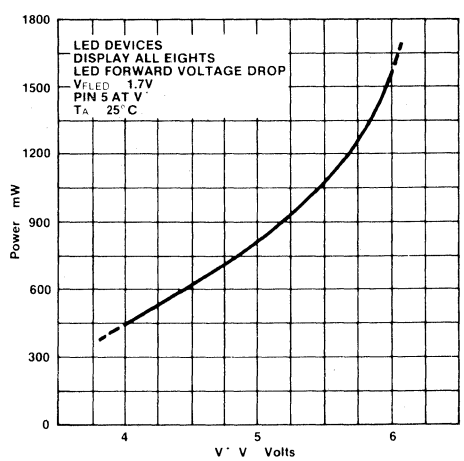
LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE

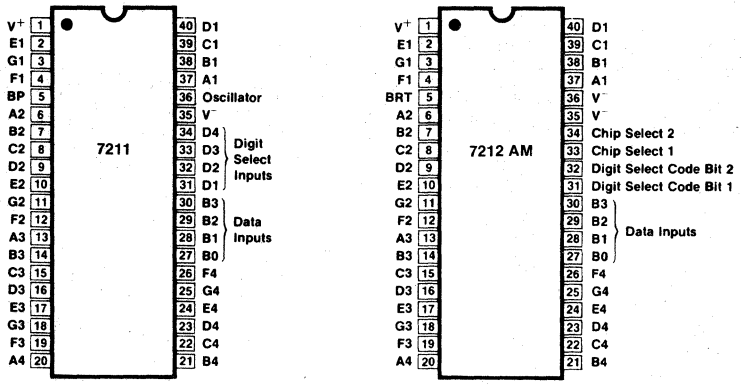


OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE



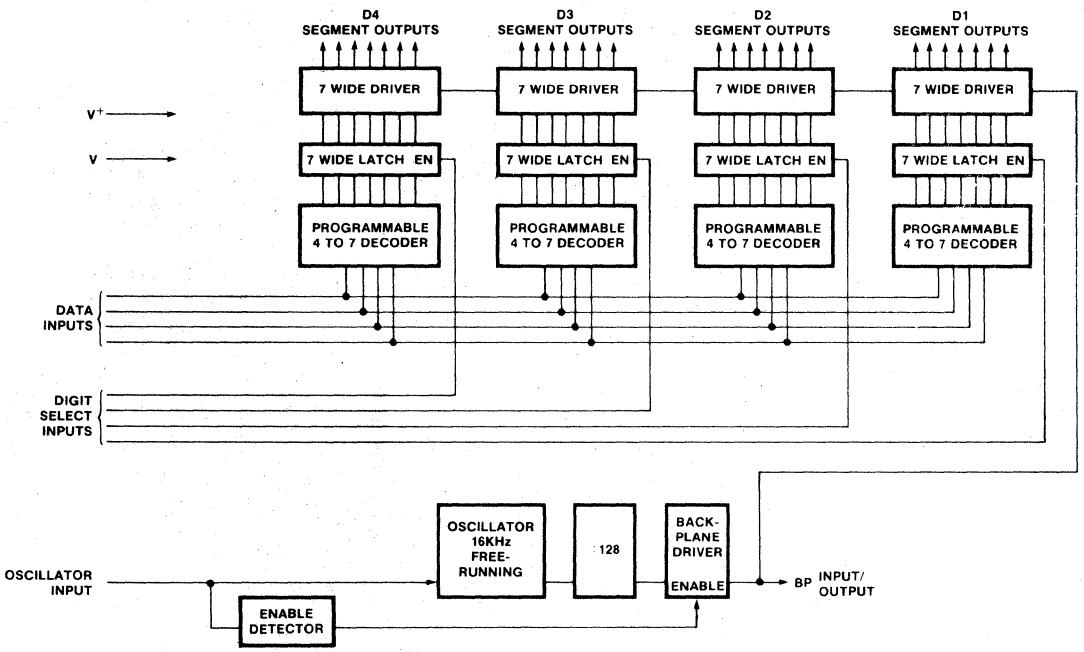
DD-7211/DD-7212

CONNECTION DIAGRAMS

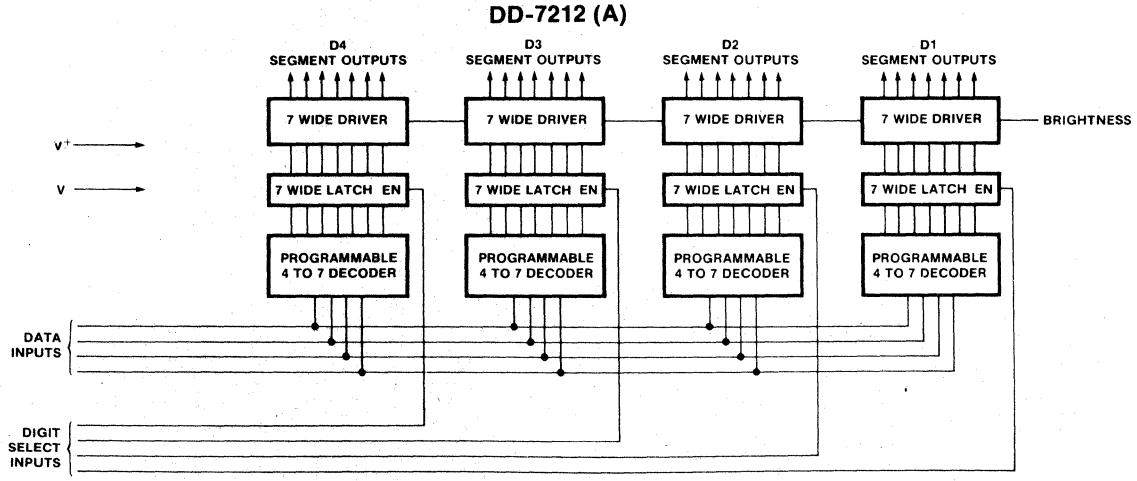


BLOCK DIAGRAMS

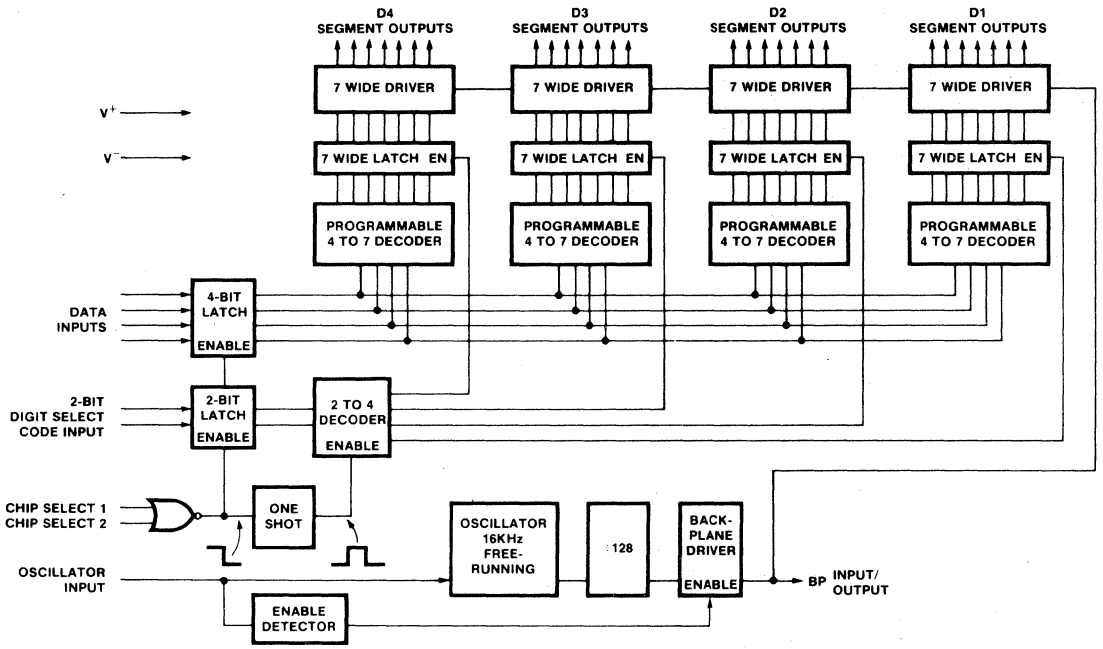
DD-7211 (A)



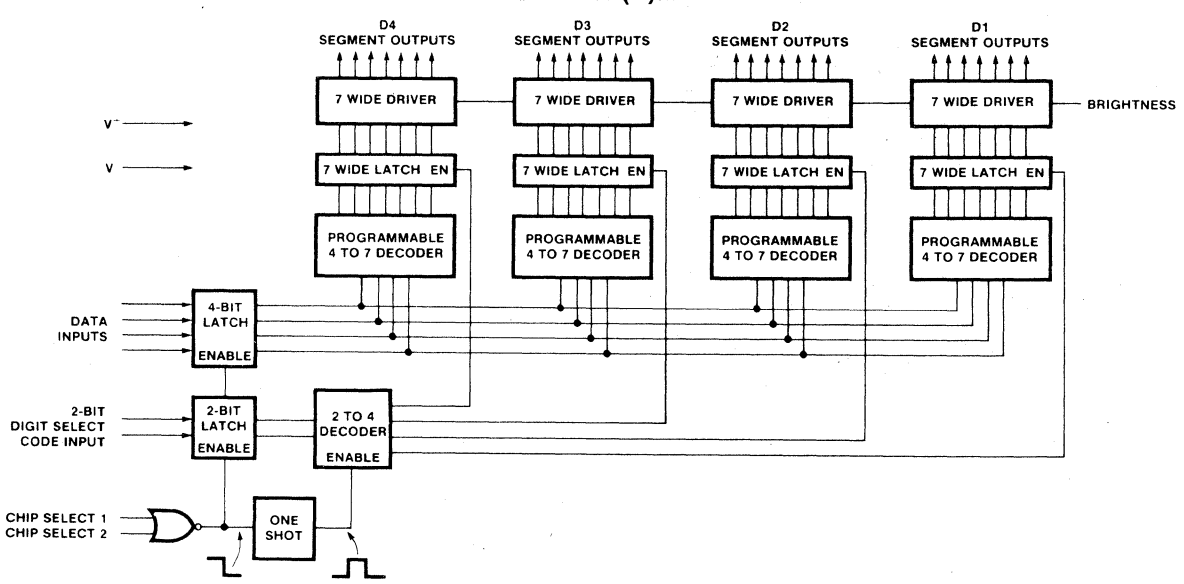
DD-7212 (A)



DD-7212 (A)M



DD-7211 (A)M



DD-7211/DD-7212

INPUT DEFINITIONS

In this table, V^+ and V^- are considered to be normal operating input logic levels. Actual input low and high levels are specified in Table 2. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	CONDITION	FUNCTION	
B0	27	V^+ = Logical One V^- = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V^+ = Logical One V^- = Logical Zero	Twos	
B2	29	V^+ = Logical One V^- = Logical Zero	Fours	
B3	30	V^+ = Logical One V^- = Logical Zero	Eights (Most significant)	
OSC (LCD Devices Only)	36	Floating or with external capacitor V^-	Oscillator input Disables BP output devices, allowing segments to be synced to an external signal input at the BP terminal (Pin 5)	

DD-7211/DD-7212

MULTIPLEXED-BINARY INPUT CONFIGURATION

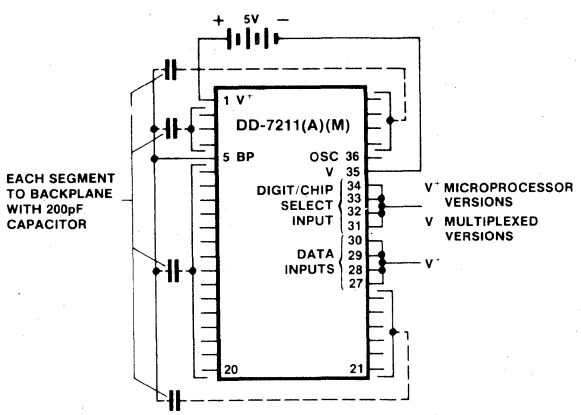
INPUT	TERMINAL	CONDITION	FUNCTION
D1	31	V^+ = Active V^- = Inactive	D1 (Least significant) Digit Select
D2	32		D2 Digit Select
D3	33		D3 Digit Select
D4	34		D4 (Most significant) Digit Select

DD-7211M/DD-7212M

MICROPROCESSOR INTERFACE INPUT CONFIGURATION

INPUT	DESCRIPTION	TERMINAL	CONDITION	FUNCTION
DS1	Digit Select Code Bit 1	31	V^+ = Logical One V^- = Logical Zero	DS1 & DS2 serve as a two bit Digit Select Code Input DS1, DS2 = 00 selects D4 DS1, DS2 = 01 selects D3 DS1, DS2 = 10 selects D2 DS1, DS2 = 11 selects D1
DS2	Digit Select Code bit 2	32		
CS1	Chip Select 1	33	V^+ = Inactive V^- = Active	When both CS1 and CS2 are taken to V^-, the data at the Data and Digit Select code inputs are written into the input latches. On the rising edge of either Chip Select, the data is decoded and written into the output latches.
CS2	Chip Select 2	34		

TEST CIRCUIT



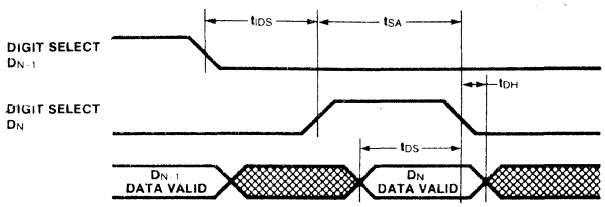


Figure 1: Multiplexed Input Timing Diagram

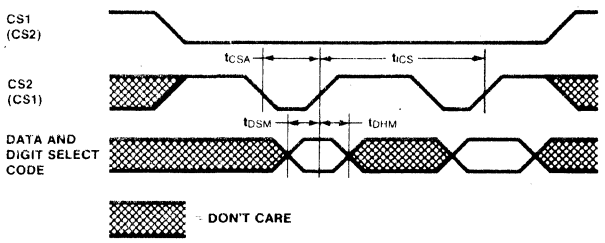
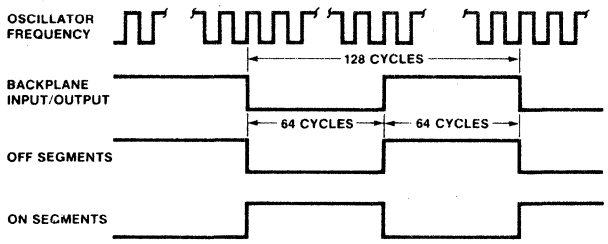


Figure 2: Microprocessor Interface Input Timing Diagram



Display Waveforms

DESCRIPTION OF OPERATION

LCD Devices

The LCD devices in the family 7211, 7211A, 7211M, 7211AM) provide outputs suitable for driving conventional four digit by seven segment LCD displays, including 28 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p- channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any dc component which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the oscillator input (pin 36) to the negative supply. This allows the 28 segment outputs to be synchronized directly to a signal input at the BP terminal (pin 5). In this manner, several slave devices may be cascaded to the backplane output of one master device or the backplane may be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device will represent a load of approximately 200pF (comparable to one additional segment). The limitation on how many devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits, and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimize power consumption is to keep the rise and fall times less than about 5 microseconds. The backplane driver devices of one device should handle the backplane to a display of 16 one-half-inch characters without the rise and fall times exceeding 5μs. (ie, 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the 7211 devices slaved to it. This external signal should be capabale of driving very large capacitive loads with short (1-2μ^s) rise and fall times. The maximum frequency for a backplane signal should be about 125Hz although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 16KHz at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 125Hz with the oscillator free-running. The oscillator frequency may be reduced by connecting an external capacitor to the oscillator terminal (pin 36); see the plot of oscillator/backplane frequency vs. external capacitance for detailed information.

The oscillator may also be overdriven if desired, although care must be taken to insure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a d.c. component to the display). This can be done by driving the oscillator input between the positive supply and a level out of the range where the backplane disable is sensed, about one fifth of the supply voltage above the negative supply. Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

LED Devices

The LED devices in the 7212, 7212A, 7212M, 7212AM) provide outputs suitable for directly driving four digit by seven segment common-anode LED displays, including 28 individual segment drivers, each consisting of a low-leakage current- controlled open-drain n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the Brightness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Fig (3). The potentiometer should be a high value (100KΩ to 1MΩ) to minimize I^2R power consumption, which can be significant when the display is off.

The brightness input may also be operated digitally as a display enable; when at V^+, the display is fully on, and at V^- fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two supplies at the Brightness input.

Note that the LED devices have two connections for V^-; both of these pins should be connected to the negative supply. The double connection is necessary to minimize effects of

bond wire resistance with the large total display currents possible.

When operating the LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (−15mW/°C above 35°C). Power dissipation for the device is given by:

$$P = [(V^+ - V^-) - V_{FLED}] \times I_S \times N_S$$

where V_{FLED} is the LED forward voltage drop, I_S is segment current, and N_S is the number of "on" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the Brightness input to keep power dissipation within the limits described above.

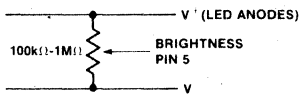


Figure 3: Brightness control

Input Configurations And Output Codes

The standard devices in the DD-7211/12 family accept a four-bit true binary (ie, positive level = logical one) input at pins 27 thru 30, least significant bit at pin 27 ascending to the most significant bit at pin 30. The DD-7211, DD-7211M, DD-7212, and DD-7212M devices decode this binary input into a seven-segment alphanumeric hexadecimal output. The DD-7211A, DD-7211AM, DD-7212A, and DD-7212AM decode the binary input into the same seven-segment output as in the ICM 7218 "Code B", ie 0-9, E, H, L, P, dash, blank. These codes are shown explicitly in Table 3. Either decoder option will correctly decode true BCD to a seven-segment decimal output.

The DD-7211, DD-7211A, DD-7212, and DD-7212A devices are intended to accept multiplexed binary or BCD output. These devices provide four separate digit lines (least significant digit at pin 31 ascending to most significant digit at pin 34), each of which when taken to a positive level decodes and stores in the output latches of its respective digit the character corresponding to the data at the input port, pins 27 through 30. More than one digit select may be activated simultaneously (which will write the same character into all selected digits), although the timing requirements shown in Fig (1) and Table 2 for data setup, hold, and inter-digit select times must be met to ensure correct output.

The DD-7211M, DD-7211AM, DD-7212M, and DD-7212AM devices are intended to accept data from a data bus under processor control.

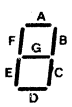
In these devices, the four data input bits and the two-bit digit select code (DS1 pin 31, DS2 pin 32) are written into input buffer latches when both chip select inputs (CS1 pin 33, CS2 pin 34) are taken to a negative level. On the rising edge of either chip select input, the content of the data input latches is decoded and stored in the output latches of the digit selected by the contents of the select code latches.

A select code of 00 writes into D4, SC2 = 0, SC1 = 1 writes into D3, SC2 = 1, SC1 = 0 writes into D2, and 11 writes into D1. The timing relationships for inputting data are shown in Fig (2), and the chip select pulse widths and data setup and hold times are specified in Table 2.

Table 3 Output Codes

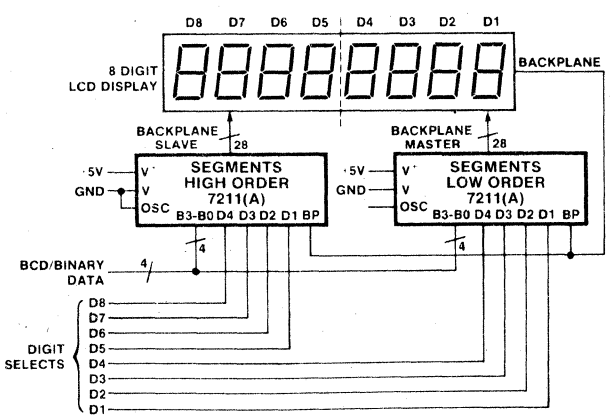
BINARY B3	B2	B1	B0	HEXADECIMAL ICM7211(M) ICM7212(M)	CODE B ICM7211A(M) ICM7212A(M)
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(BLANK)

SEGMENT ASSIGNMENT



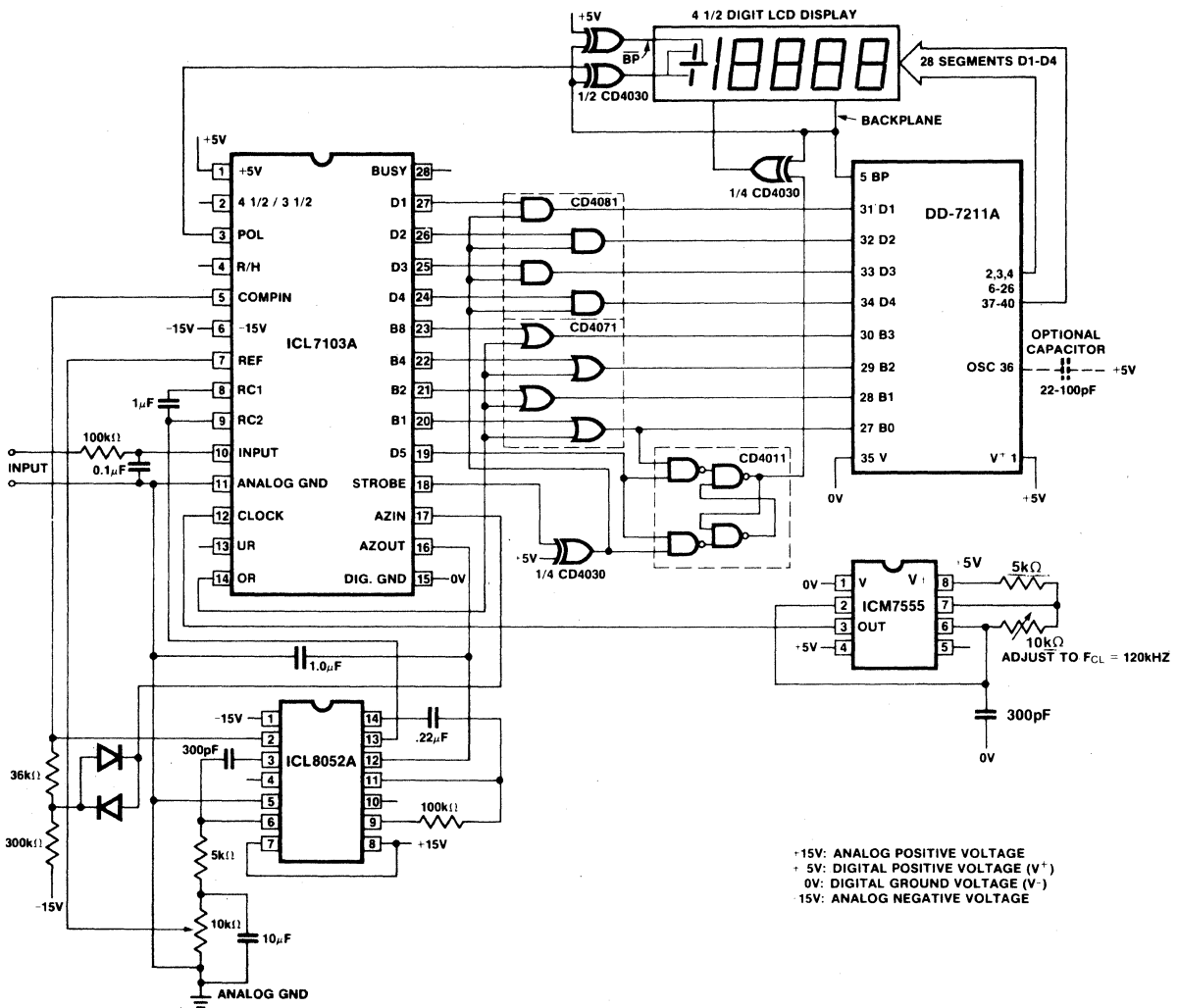
APPLICATIONS

1. Ganged 7211's Driving 8-Digit LCD Display.



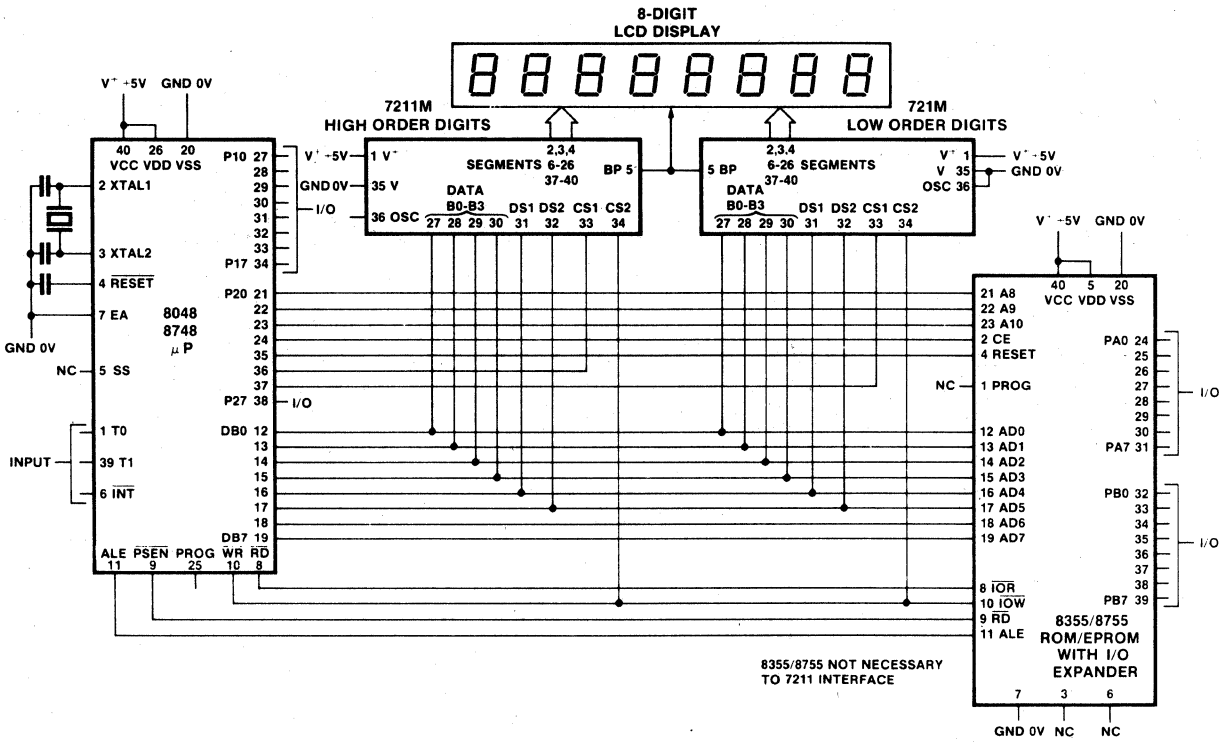
DD-7211/DD-7212

2. 4 1/2 Digit LCD DPM with Digit Blanking on Overrange.



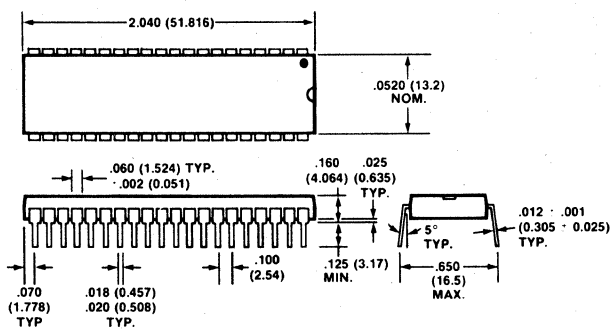
DD-7211/DD-7212

3. 8048/8748 Microprocessor Interface.



PACKAGE DIMENSIONS

40 Pin Plastic Dual-In-Line Package



DD-7218 Series CMOS Universal 8 Digit LED Driver System

FEATURES

- **Total circuit integration on chip includes:**
  - **a) Digit and segment drivers**
  - **b) All multiplex scan circuitry**
  - **c) 8X8 static memory**
  - **d) 7 segment Hexadecimal and Code B decoders**
- **Output drive suitable for large LED displays**
- **Both common anode and common cathode LED drive versions**
- **Single 5 volt supply required**
- **Data retention to 2 volts supply**
- **Shutdown feature - turns off display and puts chip into very low power dissipation mode**
- **Pin selectable choice of 2 seven segment decoders - Hexa or Code B**
- **Pin selectable choice of seven segment decode or no decoder**
- **Microprocessor compatible and hardwire versions**
- **All terminals protected against static discharge**

GENERAL DESCRIPTION

The DD-7218 series of universal LED driver systems provide, in a single package, all the circuitry necessary to interface most common microprocessors or digital systems and an LED display. Included on chip is an 8x8 static memory array providing storage for the displayed information, 2 types of 7 segment decoders, all the multiplex scan circuitry and the high power digit and segment drivers.

The DD-7218A and DD-7218B are intended to be used primarily in microprocessor systems. Data is read directly from the I/O bus line from the microprocessor. 2 Control lines (Write, and Mode) define chip select, which reads either 4 bits of control information (Data Coming, Shutdown, Decode, Hexa or Code B Decoding) or 8 bits of Display Input Data. Display Input Data (8 words, 8 bits each) is automatically sequenced into the memory on successive negative going Write pulses. Data may be displayed either directly or decoded in Hexadecimal or Code B formats. The DD-7218A drives a common anode display while the DD-7218B drives a common cathode display. (See Block Diagram 1)

The DD-7218C and DD-7218D feature 2 lines for control information (Write, Three Level Input; Hexa, Code B, Shutdown), 4 lines for Input Data and 3 lines for BCD Data Addressing of each of eight data memory locations.

Data is written into memory by setting up a BCD Data Address memory location, defining 4 lines of Input Data and then strobe the Write line low. The Three Level Control Input is independent of the Write instruction. Only Hexadecimal and Code B decoding are available for the Display Outputs. The DD-7218C drives a common anode display, the DD-7218D a common cathode display. (See Block Diagram 2)

The DD-7218E provides 4 separate lines for control information (Write, Hexa-Code B, Decode, Shutdown), 8 lines for input data, and 3 lines for BCD digit address. Data is written into the memory by setting up a BCD Data Address memory location, defining 8 lines of Input Data, and then strobe the Write line low. Control information is on separate lines and is independent of the Write instruction. Data may be displayed either directly or decoded in Hexadecimal or Code B formats. The DD-7218E drives a common anode display. (See Block Diagram 3)

ORDERING INFORMATION

Microprocessor Control Applications

Model	Display Option	Package
DD-7218AC	Common Anode	28 Pin CERDIP
DD-7218BC	Common Cathode	28 Pin PLASTIC

Hardwire Control Applications

Model	Display Option	Package
DD-7218CC	Common Anode	28 Pin CERDIP
DD-7218DC	Common Cathode	28 Pin PLASTIC
DD-7218EC	Common Anode	40 Pin CERAMIC

DD-7218 SERIES

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6V
Digit Output Current	300mA
Segment Output Current	50mA
Input Voltage (any terminal)	V^+ +0.3V to V^- −0.3V NOTE 1
Power Dissipation (28 Pin CERDIP)	1 watt NOTE 2
Power Dissipation (28 Pin Plastic)	0.5 watt NOTE 2
Power Dissipation (40 Pin Ceramic)	1 watt NOTE 2
Operating Temperature Range	−20° C to +70° C
Storage Temperature Range	−55° C to +125° C

NOTE 1 Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ or less than V^- may cause destructive device latchup. For this reason it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established. When using multiple supply systems the supply to the DD-7218 should be turned on first.

NOTE 2 These limits refer to the package and will not be obtained during normal operation. Derate above 50° C by 25mW per °C.

SYSTEM ELECTRICAL CHARACTERISTICS V^+-V^- = 5V, T_A = 25° C, Test Circuit, Display Diode Drop 1.7V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage	V^+-V^-		4		6	V
	V^+-V^-	Power Down Mode	2		6	V
Quiescent Supply Current	I_Q	Shutdown (Note 3)	6	10	300	μA
Operating Supply Current	I_{DP}	Decoder On, Outputs Open Ckt	250		950	μA
		No Decode, Outputs Open Ckt	200		450	μA
Digit Drive Current	I_D	Common Anode Vout = V^+ −2.0	−170			mA
		Common Cathode Vout = V^- +1V	50			mA
Digit Leakage Current	I_{DL}				100	μA
Peak Segment Drive Current	I_S	Common Anode Vout = V +1.5V	20	25		mA
		Common Cathode Vout = V^+ −2.0V	−10			mA
Segment Leakage Current	I_{SL}				50	μA
Display Scan Rate	F_{MUX}			250		Hz
Three Level Input						
Logical "1" Input Voltage	V_{TH}	Hexidecimal 7218C, D (Pin 9)	4.0			V
Floating Input	V_{TD}	Code B 7218C, D (Pin 9)	2.0		3.0	V
Logical "0" Input Voltage	V_{TL}	Shutdown 7218C, D (Pin 9)			1.75	V
Three Level Input Impedance				100		kΩ
Logical "1" Input Voltage	V_{IH}		2.4			V
Logical "0" Input Voltage	V_{IL}				.8	V
Write Pulse Width (Negative)	tw		550			nS
Write Pulse Width (Positive)	$t\overline{w}$		550			nS
Mode Pulse Width	tm		400			nS
Data Set Up Time	t_{ds}		400			nS
Data Hold Time	t_{dh}		25			nS
Digit Address Set Up Time	t_{das}	7218	400			nS
Digit Address Hold Time	t_{dah}	7218	100			nS
Operating Temperature Range	T_A	Industrial Temperature Range	−20		70	°C

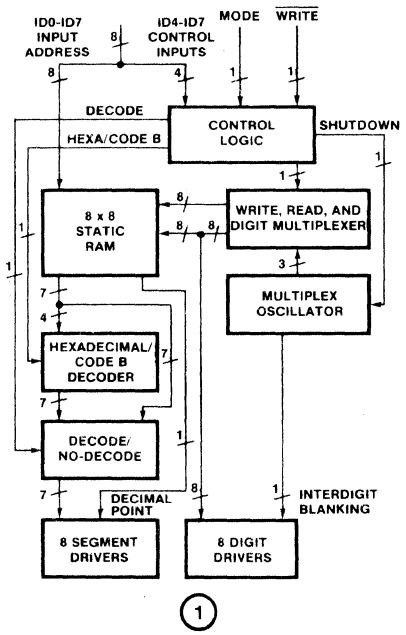
NOTE 3 In the 7218C and D (hardwire control versions) the Hexa/Code B/Shutdown Input (Pin 9) has internal biasing resistors to hold it at $V^+/2$ when Pin 9 is open circuited. These resistors consume power and result in a Quiescent Supply Current (I_Q) of typically 50μA. The 218A, B, and E devices do not have these biasing resistors and thus are not subject to this condition.

NOTE 4 For Ac and BC suffixes only, 250nsec min. for CC, DC and EC suffixes.

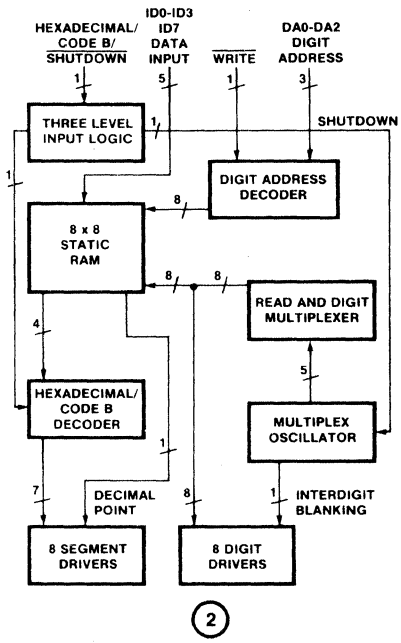
DD-7218 SERIES

BLOCK DIAGRAMS

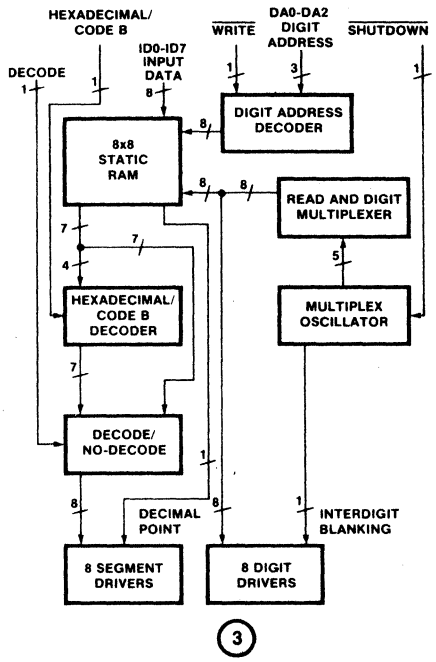
7218A, 7218B



7218C, 7218D



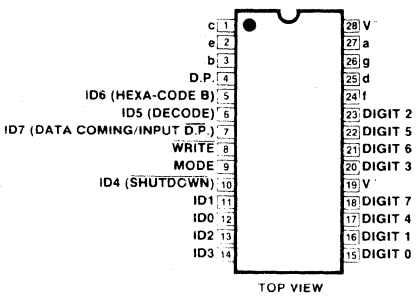
7218E



PIN CONFIGURATION

7218A

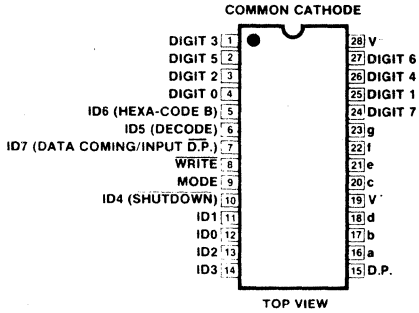
COMMON ANODE



TOP VIEW

7218B

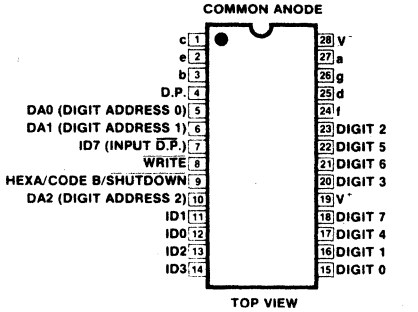
COMMON CATHODE



TOP VIEW

7218C

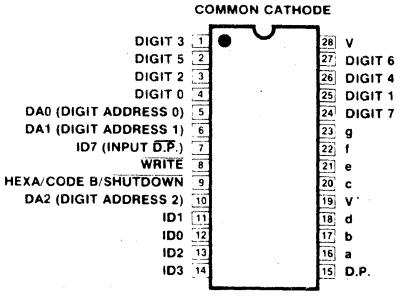
COMMON ANODE



TOP VIEW

7218D

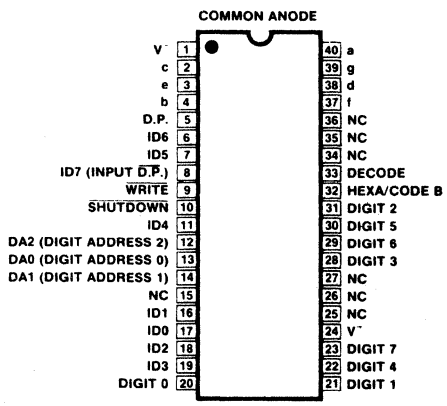
COMMON CATHODE



TOP VIEW

7218E

COMMON ANODE



TOP VIEW

DD-7218 SERIES

CONTROL INPUT DEFINITIONS DD-7218A and B

INPUT	TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{Write}}$	8	High Low	Input Not Loaded Into Memory Input Loaded Into Memory
Mode	9	High Low	Load Control Word on Write Pulse Load Input Data on Write Pulse
ID6 (Hexadecimal/Code B)	5	High Low	Hexadecimal Decoding Code B Decoding
ID5 (Decode/No Decode)	6	High Low	No Decode Decode
ID7 (Data Coming/Input $\overline{\text{D.P.}}$)	7	High Low	Data Coming No Data Coming
ID4 $\overline{\text{Shutdown}}$	10	High Low	Normal Operation Shutdown (Oscillator, Decoder, and Displays Disabled)
Input Data ID0-ID7	11,12,13, 14,5,6 10,7	High Low	Loads "One" (Note 2) Loads "Zero"

CONTROL INPUT DEFINITIONS DD-7218C and D

INPUT	TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{Write}}$	8	High Low	Inputs Not Loaded Into Memory Inputs Loaded Into Memory
Three Level Input (Note 1)	9	High Floating Low	Hexadecimal Decode Code B Decode Shutdown (Oscillator, Decoder and Displays Disabled)
Digit Address DA0-DA2	5,6,10	High Low	Loads "Ones" Loads "Zeros"
Input Data ID0-ID7	11,12,13, 14,5, 6,10,7	High Low	Loads "Ones" (Note 2) Loads "Zeros"

CONTROL INPUT DEFINITIONS DD-7218E

INPUT	TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{Write}}$	9	High Low	Input Latches Not Updated Input Latches Updated
$\overline{\text{Shutdown}}$	10	High Low	Normal Operation Shutdown (Oscillator, Decoder and Displays Disabled)
Digit Address (0,1,2) DA0-DA2	13,14,12	High Low	Loads "Ones" Loads "Zeros"
Decode/No Decode	33	High Low	No Decode Decode
Hexadecimal/Code B	32	High Low	Code B Decoding Hexadecimal Decoding
Input Data ID0-ID7	16,17,18,19 6 7,11,8	High Low	Loads "Ones" (Note 2) Loads "Zeros"

NOTE 1 In the 7218C and 7218D versions, Hexadecimal, Code B and Shutdown are controlled with a three level input on Pin 9. Pulling Pin 9 high decodes Hexadecimal. Floating Pin 9 decodes Code B and pulling Pin 9 low puts the 7218 in a Shutdown mode.

NOTE 2 In the No Decode Mode, "Ones" represents "on" segments for all inputs except for the Decimal Point, where "Zero" represents "on" segments, (i.e. segments are positive true, decimal point is negative true).

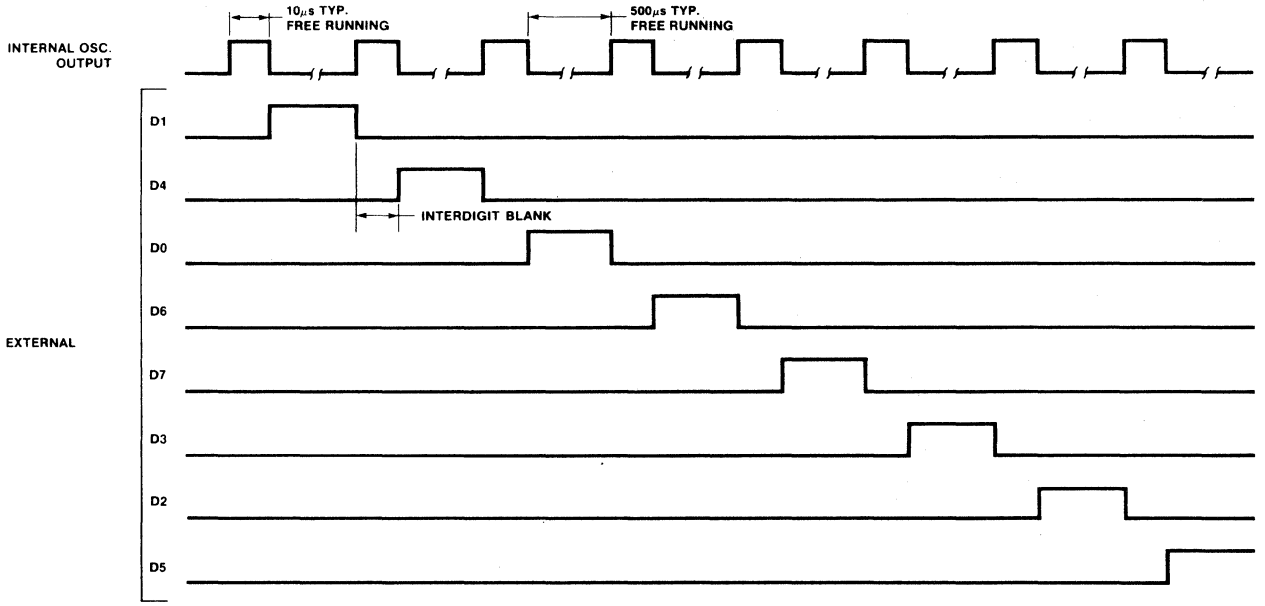


Figure 1: Multiplex Timing

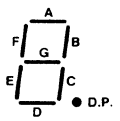


Figure 2: Segment Assignments

APPLICATIONS

Decode/No Decode

For the DD-7218A/B/E products, there are 3 input data formats possible; either direct segment and decimal point information-8 bits per digit or 2 BCD codes plus decimal point-5 bits per digit. The 7 segment decoder on chip may be disabled if direct segment information is inputted.

In the No Decode format, the inputs directly control the outputs as follows:

Input Data: ID7 ID6 ID5 ID4 ID3 ID2 ID1 ID0

Output Segments: $\overline{\text{D.P.}}$ a b c e g f d

The No Decode Mode, "Ones" represents on segments for all inputs except for the Decimal Point, where "zero" represents on segments.

Hexadecimal or Code B Decoding:
For all products, a choice of either Hexa or Code B decoding may be made. Hexa decoding provides 7 segment plus six alpha characters while Code B provides a negative sign (–), a blank (for leading zero blanking) and certain useful alpha characters for most numeric formats.

The four bit binary code is set up on inputs ID3-ID0.

Binary Code	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Hexa Code	0	1	2	3	4	5	6	7	8	9	A	b	C	d	E	F
Code B	0	1	2	3	4	5	6	7	8	9	-	E	H	L	P	(Blank)

$\overline{\text{Shutdown}}$

$\overline{\text{Shutdown}}$ performs several functions: it puts the device into a very low dissipation mode (typically 10μA at V^+-V^- = 5), turns off both the digit and segment drivers, stops the multiplex scan oscillator (this is the only way the scan oscillator can be disabled). However, it is still possible to input the memory during shutdown - only the output and read sections of the device are disabled.

Powerdown

In a Shutdown Mode, the supply voltage may be reduced to 2 volts without data being lost in memory. However, data should not be written into memory if the supply voltage is less than 4 volts.

Output Drive

The common anode output drive is approximately 200 mA per digit at a 12% duty cycle. With 5 segments being driven, this is equal to about 40mA per segment peak drive or 5mA average drive. The common cathode drive is approximately one half that of the common anode drive. If high impedance LED displays are used, the drive will be correspondingly less.

Inter Digit Blanking

A blanking time of approximately 10μs occurs between digit strobes to ensure that segment information is correct before the next digit drive thereby avoiding ghosting.

Leading Zero Blanking

This may be programmed into chip memory in the no-decode operation (each segment programmed for a zero for the blanked digits) or by using the 16th state (binary 15) with the Code B decoder.

Driving Larger Displays

If a higher average drive current per digit is required, it is possible to parallel connect digit drives together. For example, by paralleling pairs of digit drives together to drive a 4 digit display 10 mA average segment drive can be obtained.

APPLICATIONS, continued

Power Dissipation Considerations

Assuming common anode drive at V^+-V^- = 5 volts and all digits on with an average of 5 segments driven per digit, the average current would be approximately 200mA. Assuming further a 1.8 volt drop across the LED display would result in a 3.2 volt drop across the DD-7218. The device power dissipation will, therefore, be 640mW rising to about 900mW for all '8"s displayed. Caution: Position device in system such that air can flow freely to provide maximum cooling. The common cathode dissipation is approximately one half that of the common anode dissipation.

Processor Input Drive Considerations (DD-7218A/B)

The control instructions are read from the input bus lines if Mode is high and $\overline{\text{Write}}$ low. The instructions occur on 4 lines and are - Decode/no Decode, type of Decode (if desired), Shutdown/no Shutdown and Data Coming/not Coming. After the control instructions have been read (with Data Coming instruction) display data can be written into memory with each following negative going pulse of $\overline{\text{Write}}$, Mode being low. After all 8 words or digit memory locations have been re-written, additional transitions of the state of $\overline{\text{Write}}$ are ignored. It is not possible to change for example digit #7 only without refreshing the data for all the other digits. (This can, however, be achieved with the DD-7218C/D/E where the digits are individually addressed.)

Hardwire Input Drive Considerations (DD-7218C/D/E)

Control instructions are provided to the DD-7218C/D by a single three level input terminal (Pin 9), which operates independently of the $\overline{\text{Write}}$ pulse. The DD-7218E control instructions are also independent but are on three separate pins (10, 32, 33).

Data can be written into memory on the DD-7218C/D/E by setting up a 3 bit binary code (one of eight) on the digit address inputs, which define the digit where the data is to be written into the memory, and apply a negative going $\overline{\text{Write}}$ pulse. For example, it is possible to change only digit 7 without refreshing the data for all the other digits. (However, this cannot be achieved with the DD-7218A/B.

Supply Capacitor

A .1μF capacitor is recommended between V^+ and V^- to inhibit multiplex noise.

SWITCHING WAVEFORMS DD-7218

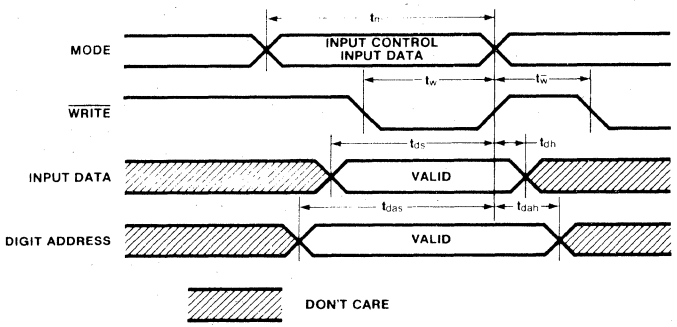


Figure 3

CHIP ADDRESS SEQUENCE DD-7218A and B

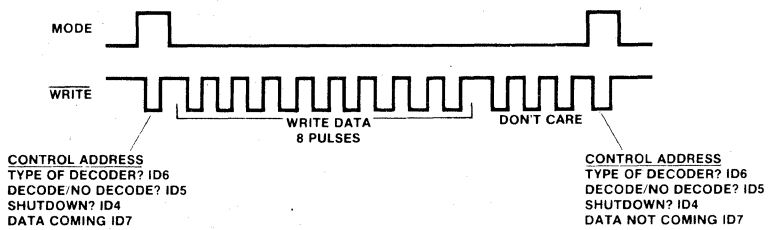


Figure 4

CHIP ADDRESS SEQUENCE EXAMPLE DD-7218C/D/E

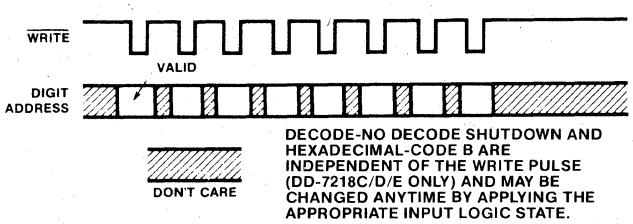
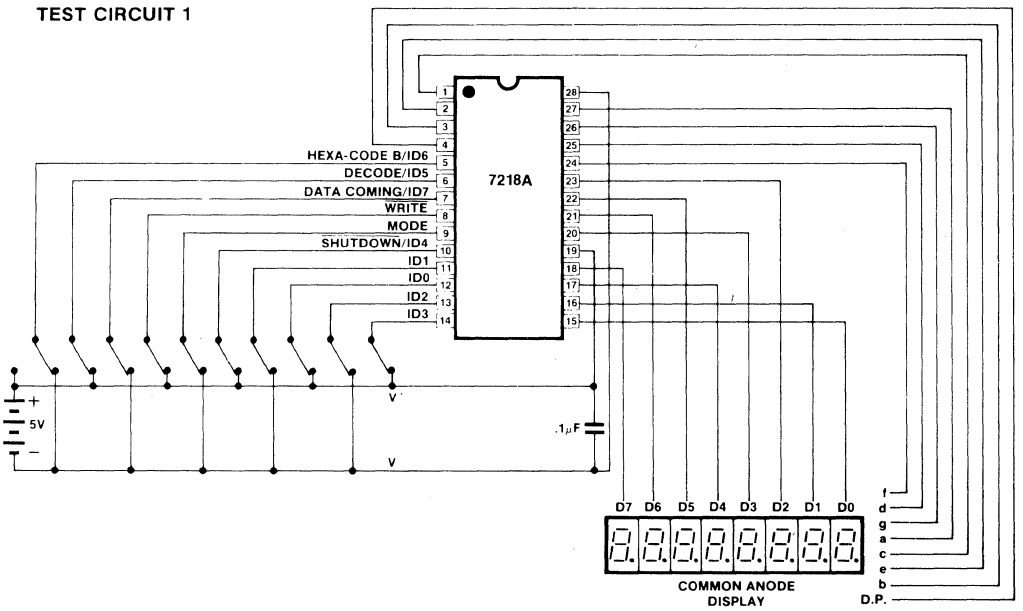


Figure 5

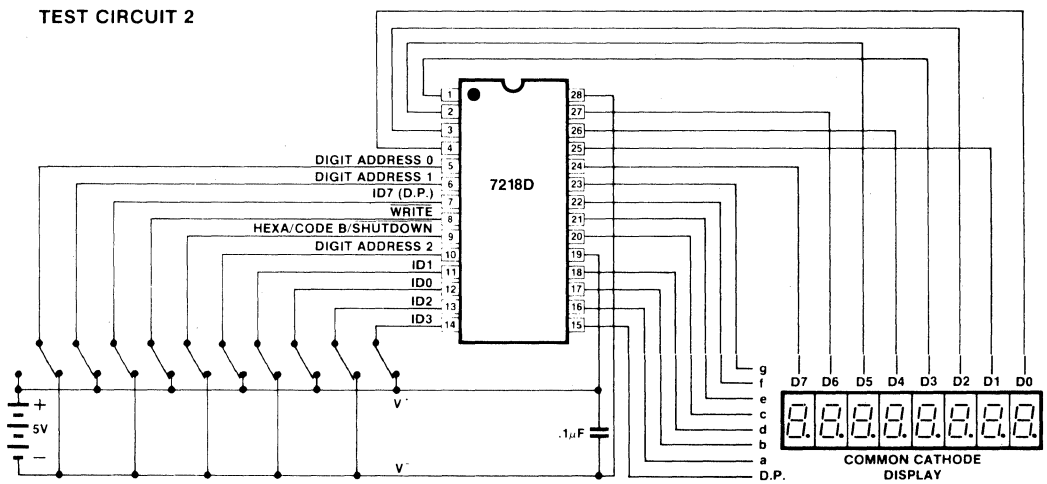
DD-7218 SERIES

TEST CIRCUITS

TEST CIRCUIT 1

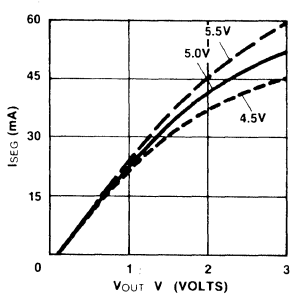


TEST CIRCUIT 2

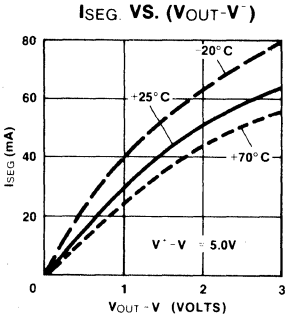


TYPICAL CHARACTERISTICS

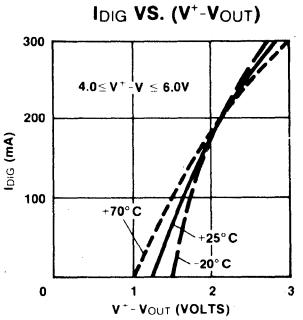
COMMON ANODE SEG. DRIVER
I_{SEG} VS. (V_{OUT}-V^-) AT 25°C



COMMON ANODE SEG. DRIVER
I_{SEG} VS. (V_{OUT}-V^-)

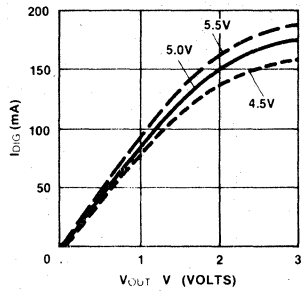


COMMON ANODE DIGIT DRIVER
I_{DIG} VS. (V^+-V_{OUT})

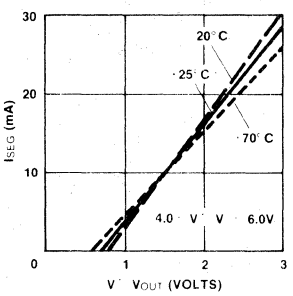


TYPICAL CHARACTERISTICS, continued

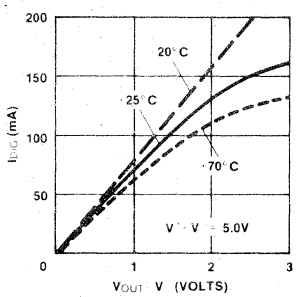
COMMON CATHODE DIGIT DRIVER I_{DIG} VS. (V_{OUT}-V^-) AT 25°C



COMMON CATHODE SEG. DRIVER I_{SEG} VS. (V^+-V_{OUT})



COMMON CATHODE DIGIT DRIVER I_{DIG} VS. (V_{OUT}-V^-)



APPLICATION EXAMPLES

8 DIGIT MICROPROCESSOR DISPLAY APPLICATION

The display interface (7218) is shown with an Intel 8048 microprocessor. The 8 bit data bus DB0/DB7 - ID0/ID7 transfers control and data information to the 7218 display interface on successive Write pulses. When Mode is high a control word is transferred. Mode low allows data transfer on a Write pulse. Eight memory address locations in the 8 ×8 static memory are automatically sequenced on each successive Write pulse. After eight Write pulses have occurred, further pulses are ignored and the display interface returns to normal display operations until a new control word is transferred. See Figure 4.

Decoding of the stored data in memory is defined by the control word and may be decoded in Hexadecimal, Code B, or No-Decode formats.

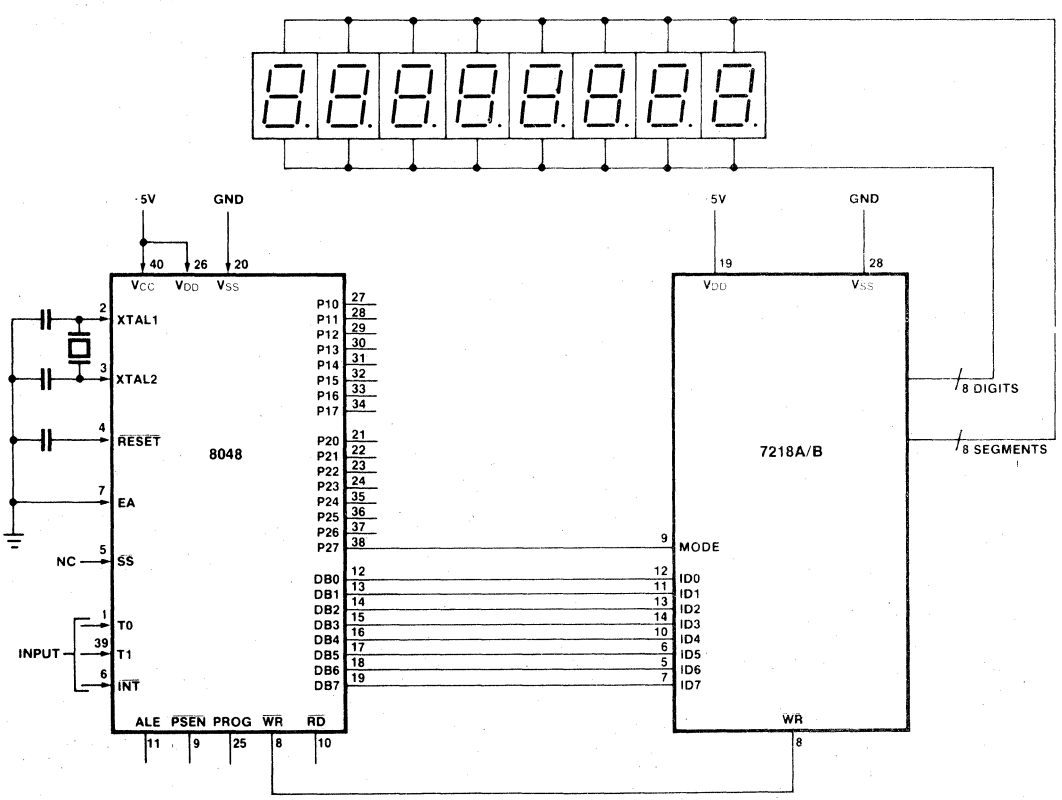


Figure 6: 8 Digit Microprocessor Display

DD-7218 SERIES

16 DIGIT MICROPROCESSOR DISPLAY APPLICATION

Both 7218's are addressed simultaneously with a 3 bit word, DA2-DA0.

Display data from the 8048 I/O bus (DB7-DB0) is transferred to both 7218 (ID3-ID0) simultaneously, 4 bits + 4 bits on Write enable.

Display digits from both 7218's are interleaved to allow adjacent pairs of digits to be loaded sequentially on a single 8 bit data bus, ie D0 D1, D2 D3, D4 D5, etc.

Decimal point information (from 8048, P26 - P27) is supplied to the 7218 on bus lines ID7 to both devices.

Choice of decoding is available in either Hexadecimal or Code-B format by hardwiring or decoding to a Three Level format on Pin 9 of the 7218.

Multiplexing is asynchronous with respect to the microprocessor and is completely performed by the 7218.

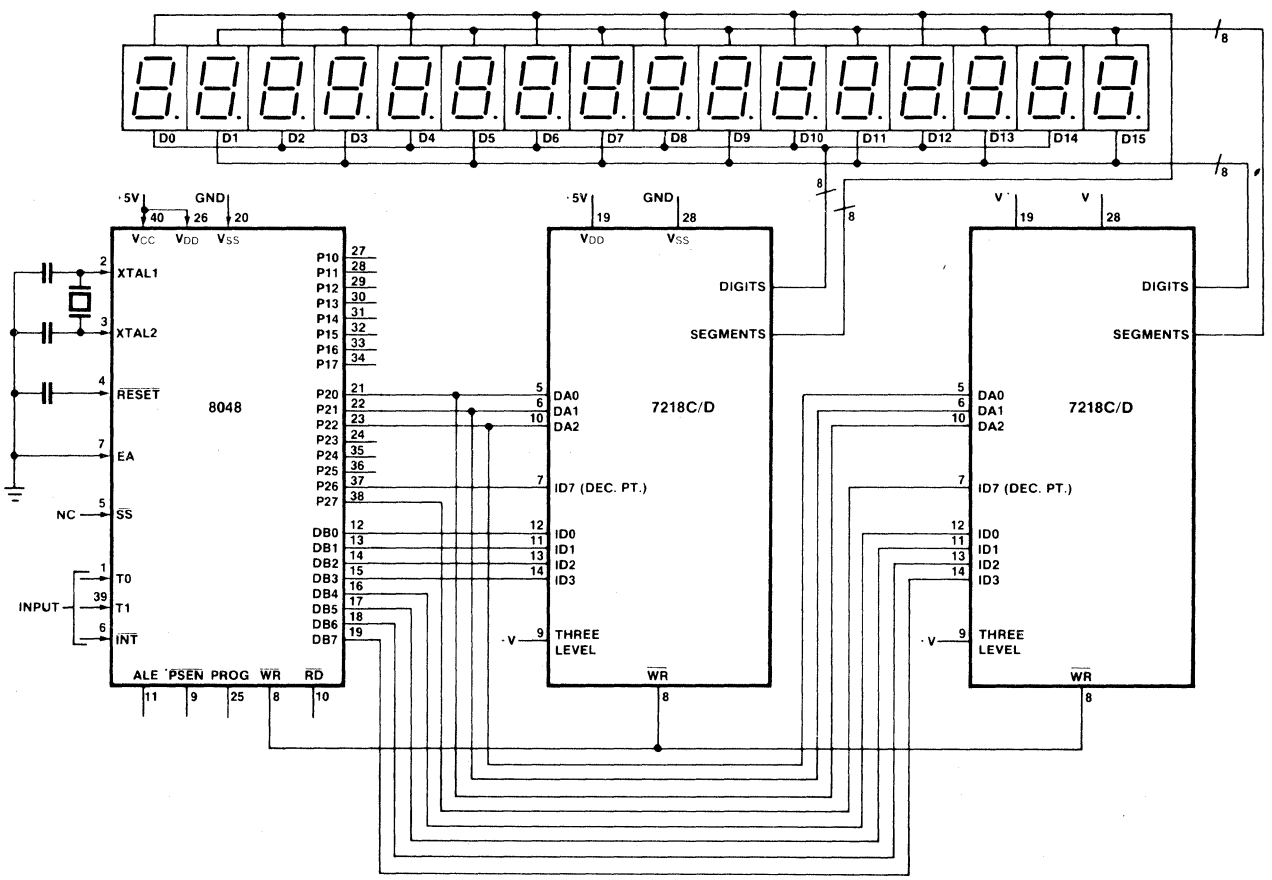


Figure 7: 16 Digit Display

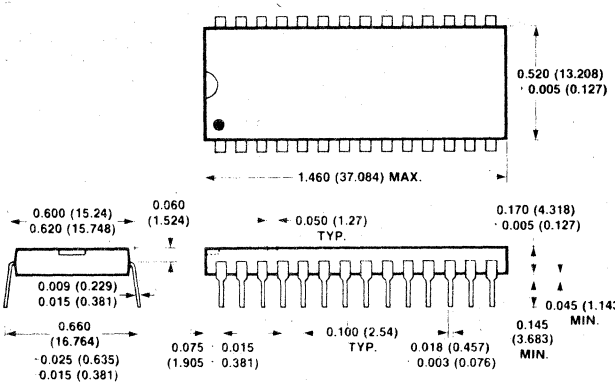
The 7218 can be used as a microprocessor based LED status panel driver. The microprocessor selected control word would include "No Decode" and "Data Coming". The computer then outputs word oriented "Ones" and Zeroes" to indicate on-off states. This data is read into the 7218 which in turn directly drives appropriate descrete LEDs. LED indicators can be red or green (8 "segments" × 8 digits = 64 dots ÷ 2 per red or green = 32 channels) on red, yellow or green (21 channels).

Additional 7218's may be bussed and addressed (see Figure 7) to expand the status panel capacity. Note per figure 4 that after the 7218 has read in its data (8 write pulses), it ignores additional information on the data lines. A new control word must be received before the next write sequence can be accommodated. Consequently, by address decoding and write pulse enabling, numerous 7218's can be bussed together to allow a large number of indicator channels.

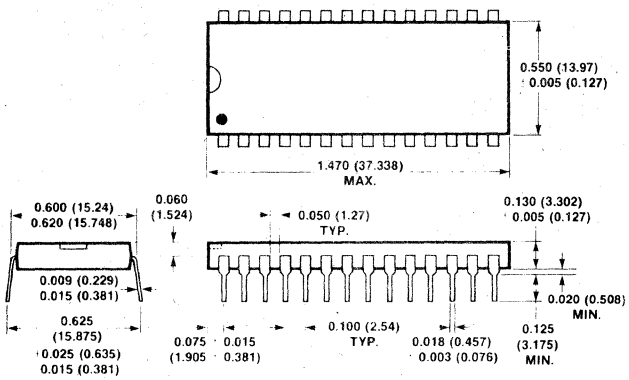
DD-7218 SERIES

PACKAGE DIMENSIONS

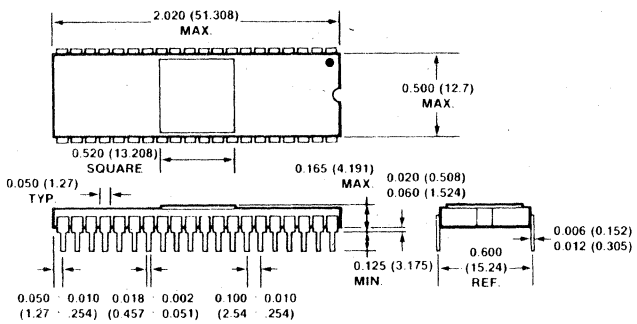
28 Pin CERDIP Dual-In-Line Package



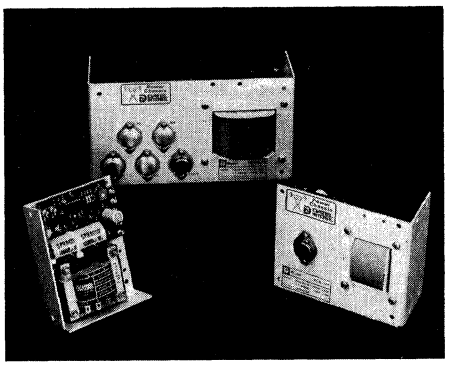
28 Pin Plastic Dual-In-Line Package



40 Pin Ceramic Dual-In-Line Package



Power Supplies and DC-DC Converters



Glossary of Power Supply Terms

AMBIENT TEMPERATURE: The temperature of still air surrounding a power supply. For power supplies a good practical definition is: **the temperature measured at a point ½" from the body of a power supply which is protected from direct air movement by a suitable enclosure.** It should be noted that the temperature of circulating air, such as in a temperature chamber with a fan, is not a correct ambient temperature measurement since the power supply is being cooled by the circulating air.

BACK RIPPLE CURRENT: For DC to DC converters, the input peak to peak AC current, as a percentage of input current, with an ideal voltage source input. This ripple current is caused by switching transients in the converter and is less than 1% in well-designed converters. See Figure 1.

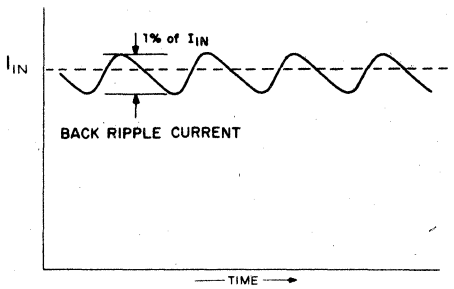


Figure 1. Back Ripple Current of a DC-DC Converter.

BREAKDOWN VOLTAGE: The maximum AC or DC voltage which may be applied between input and output terminals of a supply. See Figure 2.

EFFICIENCY: The ratio of output power to input power expressed as a percentage. This is generally measured under full load at nominal line voltage.

FARADAY SHIELD: An electrostatic shield between input and output windings of a transformer. This is done to reduce capacitive coupling between the input and output of the power supply.

FOLDBACK CURRENT LIMITING: An overload protection method whereby the output current is decreased as the load approaches short circuit. Under output short circuit, the output current is therefore less than rated output current. This technique minimizes internal power dissipation under overload conditions. See Figure 3 (b).

ISOLATION: The resistive and capacitive coupling between the input and output of an isolated supply. This is generally given in megohms and picofarads and is normally determined by the transformer characteristics. See Figure 2.

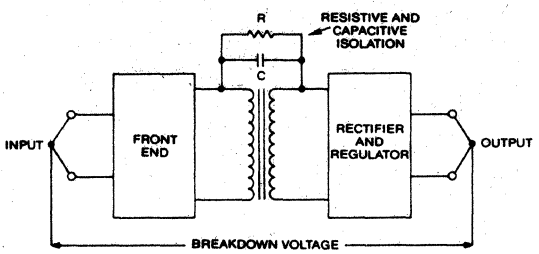


Figure 2. Breakdown Voltage and Isolation.

LEAKAGE CURRENT: The AC or DC current flowing between input and output of an isolated supply with a specified voltage applied between input and output.

LINE REGULATION: The maximum deviation of the output voltage in percent as the input voltage is varied from nominal to high line and nominal to low line. Output load and ambient temperature are held constant.

LOAD REGULATION: The maximum deviation of the output voltage in percent as the load is changed from minimum to maximum rated load. Input voltage is nominal value and ambient temperature is constant.

OUTPUT CURRENT LIMITING: An overload protection method whereby the maximum output current is automatically limited in value under overload conditions so that the power supply is not damaged. See Figure 3 (a).

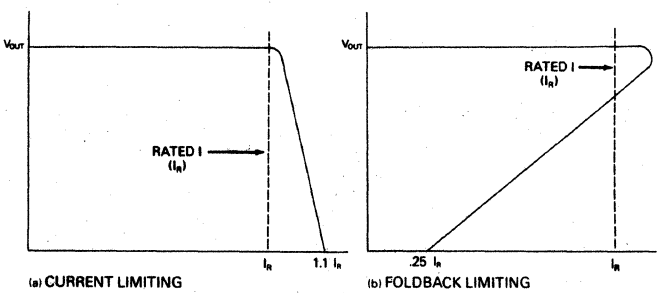


Figure 3. Output Overload Characteristics.

OUTPUT IMPEDANCE : Defined as dV_{OUT}/dI_{OUT}. This can be measured at DC or at a specified AC frequency. A typical output impedance vs. frequency graph is shown in Figure 4. Output impedance is sometimes called "dynamic load regulation".

OUTPUT VOLTAGE : The nominal DC value of the voltage **at the output terminals** of the supply. It is assumed that any ripple or noise is averaged in the measurement.

OUTPUT VOLTAGE ACCURACY: The maximum deviation of the output voltage from its rated DC value. Input voltage is nominal value and temperature is room temperature (+25°C).

OVERSHOOT: A transient voltage change in excess of the normal regulation limits which can occur when a power supply is turned on or off, or when there is a step change in line voltage or load.

OVER VOLTAGE PROTECTION: A mechanism whereby the output is shut down if the output voltage for any reason exceeds a specified value. This feature is specially important for 5 Volt logic supplies.

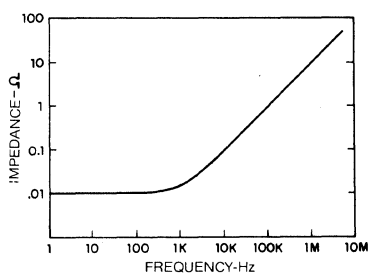


Figure 4. Output Impedance vs. Frequency.

RATED OUTPUT CURRENT: The maximum current which can be drawn from the output of the supply for specified regulation or temperature change. The output current is derated with temperature for some supplies.

REMOTE SENSING: A method whereby the regulator circuit senses the voltage directly at the load. This is done by running separate wires from the regulator to the load in order to circumvent the voltage drop in the lines carrying the load current. See Figure 14.

RIPPLE AND NOISE: The magnitude of AC voltage appearing superimposed on the DC output. It is usually stated in either peak to peak or RMS volts. For line operated supplies the ripple is normally a 120 Hz waveform. For DC to DC converters the ripple is twice the switching frequency.

SERIES REGULATION: A popular regulation method whereby a control device (transistor) is placed in series with the power source in order to regulate the voltage across the load. See Figure 13.

STABILITY: The percent change in output voltage as a function of time at constant input voltage, load, and temperature.

TEMPERATURE COEFFICIENT: The average change in output voltage per degree Centigrade change in temperature with load and input voltage held constant. The coefficient is generally derived from output voltage measurements at room temperature and the two extremes of the operating temperature range.

TEMPERATURE RANGE, OPERATING: The range of environmental temperatures (usually in °C) over which a power supply can be safely operated.

TEMPERATURE RANGE, STORAGE: The range of environmental temperatures (usually in °C) over which a power supply can be safely stored, nonoperating.

TRANSIENT RECOVERY TIME: The time required for the output voltage to settle within specified regulation limits after an instantaneous change in output load current. This is generally measured with a defined load change. See Figure 5.

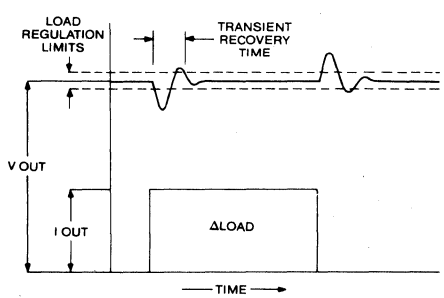


Figure 5. Transient Recovery Time.

WARM-UP TIME: The time (after power turn on) required for the output voltage to reach its equilibrium value within the output accuracy specification.

Single Output Line Operated Power Modules

SPECIFICATIONS, 25° C	UPM-5/250	UPM-5/500	UPM-5/1000	UPM-5/1000B	UPM-5/2000
Output Voltage	5VDC	5VDC	5VDC	5VDC	5VDC
Output Voltage Accuracy	±1%	±1%	±1%	±2%	±1%
Rated Output Current	250mA	500mA	1.0A	1.0A	2.0A
Line Regulation, max.	.05%	.05%	.05%	0.25%	.05%
Load Regulation, max.	0.1%	0.1%	0.1%	0.25%	0.1%
Temp. Coefficient, max.	.02%/° C	.02%/° C	.02%/° C	.02%/° C	.02%/° C
Output Ripple, RMS max.	1mV	1mV	1mV	1mV	1mV
Output Impedance, max.	.05Ω	.05Ω	.01Ω	.01Ω	.005Ω
Trans. Recovery Time, max.	50 μsec.	50 μsec.	50 μsec.	50 μsec.	50 μsec.
Isolation Resistance, min.	100 Meg.	100 Meg.	100 Meg.	100 Meg.	100 Meg.
Isolation Capacitance, max.	250pF	250pF	250pF	250pF	250pF
Breakdown Voltage, min.	1500VAC	1500VAC	1500VAC	1500VAC	1500VAC
Operating Temp. Range		-25° C to +71° C (No Derating)			(2)
Storage Temp. Range		-25° C to +85° C			
Case Material	Phenolic	Phenolic	Phenolic	Phenolic	Phenolic
Module Size, inches	3.5 × 2.5 × .875	3.5 × 2.5 × .875	3.5 × 2.5 × 1.25	3.5 × 2.5 × 1.25	3.5 × 2.5 × 1.56
Module Size, millimeters	88,9×63,5×22,2	88,9×63,5×22,2	88,9×63,5×31,8	88,9×63,5×31,8	88,9×63,5×39,6
Module Weight	14 oz. (397g)	14 oz. (397g)	18 oz. (510g)	18 oz. (510g)	24 oz. (680g)
Case/Pin Configuration	C1	C1	C2	C2	C3
Other Versions	E,J (1)	E,J (1)	E,J	E,J	E,J
Mating Socket	MS-7	MS-7	MS-7	MS-7	MS-7
Price (1-9)	**$45.00**	**$53.50**	**$72.50**	**$57.00**	**$83.00**

NOTES: 1. For "E" version module size is C2 (3.5 × 2.5 × 1.25 inches, 18 oz.)
2. For UPM-5/2000 operating temp. range should be restricted for a max. case temperature of 80° C in use.

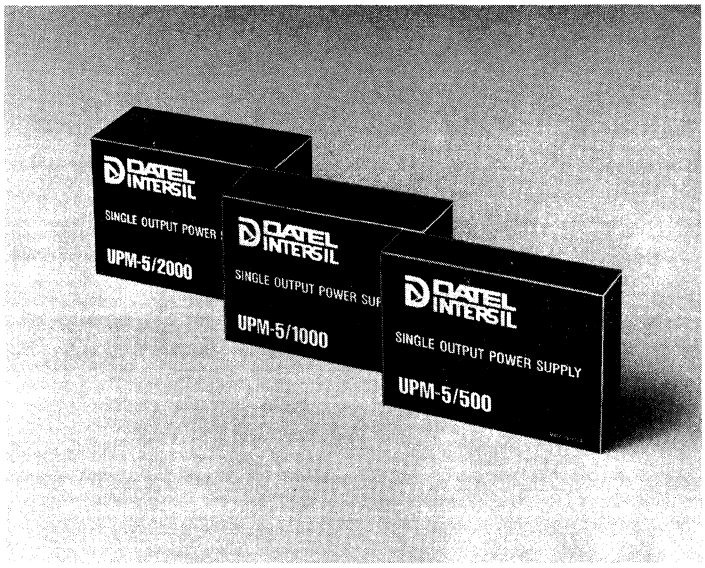
DESCRIPTION

This line of single output, voltage regulated DC power supplies features six 5 volt output models with output currents from 250mA to 4 amperes. In addition, there are 4 other models with 6V to 15V outputs. All outputs have current limiting short circuit protection. Temperature coefficients are .02%/°C and output ripple voltage is 1 to 2 millivolts RMS.

INPUT VOLTAGE SPECIFICATIONS

Standard input specification: 115VAC ±10%
@ 60-440 Hz
E version: 220VAC ±10% @ 48-440 Hz
J version: 100VAC ±10% @ 48-440 Hz

There is no extra charge for E and J versions. When ordering, add E or J suffix after model number. Note that in some instances the module size is larger for the E version. MS-7 sockets are $4.00 each.



UPM-6/150A	UPM-9/100A	UPM-12/100A	UPM-15/100A
6VDC	9VDC	12VDC	15VDC
±1%	±1%	±1%	±1%
150mA	100mA	100mA	100mA
.05%	.05%	.02%	.02%
0.1%	0.1%	.05%	.05%
.02%/°C	.02%/°C	.02%/°C	.02%/°C
1mV	2mV	2mV	2mV
.05Ω	.01Ω	.01Ω	.01Ω
50 μsec.	50 μsec.	50 μsec.	50 μsec.
100 Meg.	100 Meg.	100 Meg.	100 Meg.
250pF	250pF	250pF	250pF
1500VAC	1500VAC	1500VAC	1500VAC
	-25°C to +71°C (No Derating)		
	-25°C to +85°C		
Phenolic	Phenolic	Phenolic	Phenolic
3.5 × 2.5 × .875	3.5 × 2.5 × .875	3.5 × 2.5 × .875	3.5 × 2.5 × .875
88,9 × 63,5 × 22,2	88,9 × 63,5 × 22,2	88,9 × 63,5 × 22,2	88,9 × 63,5 × 22,2
14 oz. (397g)	14 oz. (397g)	14 oz. (397g)	14 oz. (397g)
C1	C1	C1	C1
E,J (1)	E,J (1)	E,J (1)	E,J (1)
MS-7	MS-7	MS-7	MS-7
$44.00	**$44.00**	**$51.50**	**$51.50**

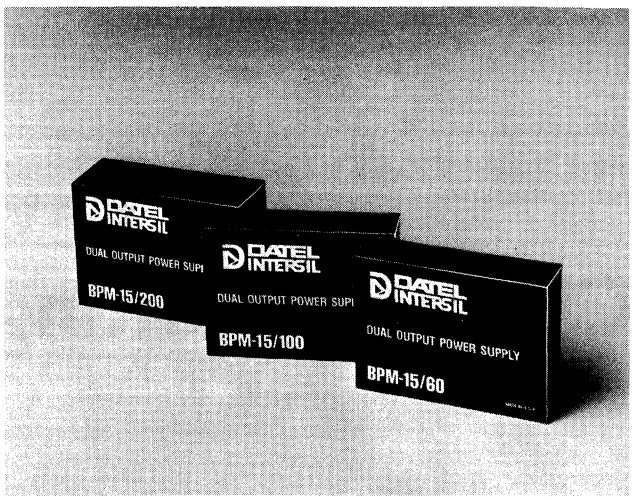
THESE POWER SUPPLIES ARE COVERED BY GSA CONTRACT

Dual Output Line Operated Power Modules

SPECIFICATIONS, 25° C	BPM-5/250	BPM-5/500	BPM-12/60	BPM-12/100	BPM-12/200	BPM-12/300
Output Voltage	±5VDC	±5VDC	±12VDC	±12VDC	±12VDC	±12VDC
Output Voltage Accuracy	±1%	±1%	±1%	±1%	±1%	±1%
Rated Output Current	±250mA	±500mA	±60mA	±100mA	±200mA	±300mA
Line Regulation, max.	.05%	.05%	.02%	.02%	.02%	.02%
Load Regulation, max.	0.1%	0.1%	.05%	.05%	.05%	.05%
Temp. Coefficient, max.	.02%/° C	.02%/° C	.02%/° C	.02%/° C	.02%/° C	.02%/° C
Output Ripple, RMS max.	1mV	1mV	2mV	2mV	2mV	2mV
Output Impedance, max.	.05Ω	.03Ω	0.2Ω	0.1Ω	.05Ω	.05Ω
Trans. Recovery Time, max.	50 μsec.	50 μsec.	50 μsec.	50 μsec.	50 μsec.	50 μsec.
Isolation Resistance, min.	100 Meg.	100 Meg.	100 Meg.	100 Meg.	100 Meg.	100 Meg.
Isolation Capacitance, max.	250pF	250pF	250pF	250pF	250pF	250pF
Breakdown Voltage, min.	1500VAC	1500VAC	1500VAC	1500VAC	1500VAC	1500VAC
Operating Temp. Range	-25° C to +71° C (No Derating)					(3)
Storage Temp. Range	-25° C to +85° C					
Case Material	Phenolic	Phenolic	Phenolic	Phenolic	Phenolic	Phenolic
Module Size, inches	3.5 × 2.5 × .875	3.5 × 2.5 × 1.25	3.5 × 2.5 × .875	3.5 × 2.5 × .875	3.5 × 2.5 × 1.25	3.5 × 2.5 × 1.56
Module Size, millimeters	88,9×63,5×22,2	88,9×63,5×31,8	88,9×63,5×22,2	88,9×63,5×22,2	88,9×63,5×318	88,9×63,5×396
Module Weight	14 oz. (397g)	18 oz. (510g)	14 oz. (397g)	14 oz. (397g)	18 oz. (510g)	24 oz. (680g)
Case/Pin Configuration	C1	C2	C1	C1	C2	C3
Other Versions	E,J(1)	E,J(2)	E,J(1)	E,J(1)	E,J	E,J
Mating Socket	MS-7	MS-7	MS-7	MS-7	MS-7	MS-7
Price (1-9)	**$72.50**	**$83.00**	**$43.00**	**$51.50**	**$67.00**	**$86.00**

NOTES: 1. For "E" version module size is C2 (3.5 × 2.5 × 1.25 inches, 18 oz.)
2. For "E" version module size is C3 (3.5 × 2.5 × 1.56 inches, 24 oz.)
3. For BPM-12/300 and BPM-15/300, operating temp. range should be restricted for max. case temperature of 80° C in use.

Temperature coefficient is .02% per degree Centigrade and output ripple voltage is 1 to 2 millivolts RMS. These rugged, encapsulated modules are useful for powering a wide variety of devices including linear IC's, op amps, data converters, and other analog circuits.



INPUT VOLTAGE SPECIFICATIONS

Standard input specification:
115VAC ±10% @ 60-440 Hz.
E version: 220VAC ±10% @ 48-440 Hz.
J version: 100VAC ±10% @ 48-440 Hz.

There is no extra charge for E and J versions. When ordering, add E or J suffix after model number. Note that in some instances the module size is larger for the E version.
MS-7 sockets are $4.00 each.

BPM-15/60	BPM-15/100	BPM-15/200	BPM-15/300
±15VDC	±15VDC	±15VDC	±15VDC
±1%	±1%	±1%	±1%
±60mA	±100mA	±200mA	±300mA
.02%	.02%	.02%	.02%
.05%	.05%	.05%	.05%
.02%/° C	.02%/° C	.02%/° C	.02%/° C
2mV	2mV	2mV	2mV
0.2Ω	0.1Ω	.05Ω	.03Ω
50 μsec.	50 μsec.	50 μsec.	50 μsec.
100 Meg.	100 Meg.	100 Meg.	100 Meg.
250pF	250pF	250pF	250pF
1500VAC	1500VAC	1500VAC	1500VAC
	-25° C to +71° C (No Derating)		(3)
	-25° C to +85° C		
Phenolic	Phenolic	Phenolic	Phenolic
3.5 × 2.5 × .875	3.5 × 2.5 ×.875	3.5 × 2.5 × 1.25	3.5 × 2.5 × 1.56
88,9 × 63,5 × 22,2	88,9 × 63,5 × 22,2	88,9 × 63,5 × 31,8	8,9 × 63,5 × 39,6
14 oz. (397g)	14 oz. (397g)	18 oz. (510g)	24 oz. (680g)
C1	C1	C2	C3
E,J(1)	E,J(1)	E,J	E,J
MS-7	MS-7	MS-7	MS-7
$43.00	**$51.50**	**$67.00**	**$86.00**

THESE POWER SUPPLIES ARE COVERED BY GSA CONTRACT

Chassis Mounting Modules

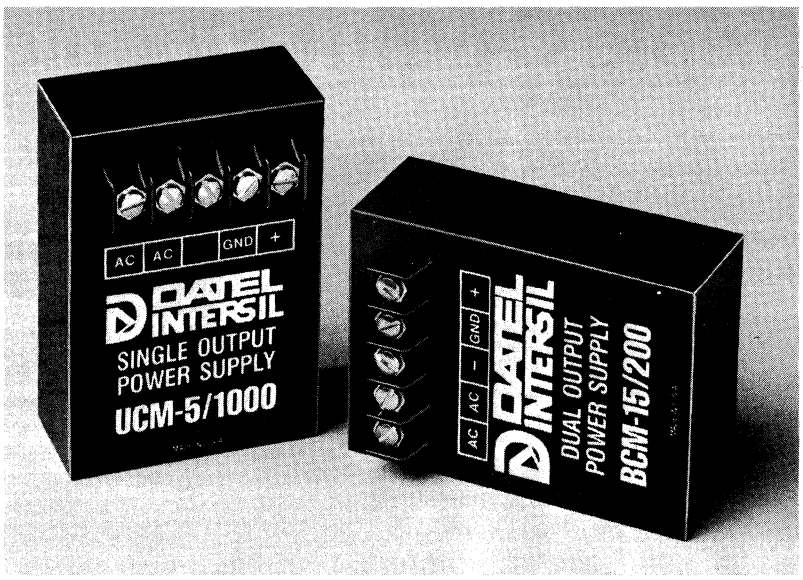
SPECIFICATIONS, 25° C	UCM-5/250	UCM-5/500	UCM-5/1000	UCM-5/1000B
Output Voltage	5VDC	5VDC	5VDC	5VDC
Output Voltage Accuracy	±1%	±1%	±1%	±2%
Rated Output Current	250mA	500mA	1.0A	1.0A
Line Regulation, max.	.05%	.05%	.05%	0.25%
Load Regulation, max.	0.1%	0.1%	0.1%	.025%
Temperature Coefficient, max.	.02%/° C	.02%/° C	.02%/° C	.02%/° C
Output Ripple, RMS max.	1mV	1mV	1mV	1mV
Output Impedance, max.	.05Ω	.05Ω	.01Ω	.01Ω
Transient Recovery Time, max.	50μsec.	50μsec.	50μsec.	50μsec.
Isolation Resistance, min.	100 Meg.	100 Meg.	100 Meg.	100 Meg.
Isolation Capacitance, max.	250pF	250pF	250pF	250pF
Breakdown Voltage, min.	1500VAC	1500VAC	1500VAC	1500VAC
Operating Temp. Range		-25° C to +71° C (No Derating)		
Storage Temp. Range		-25° C to +85° C		
Case Material	Phenolic	Phenolic	Phenolic	Phenolic
Module Size, inches	3.5 × 2.5 × .875	3.5 × 2.5 × .875	3.5 × 2.5 × 1.25	3.5 × 2.5 × 1.25
Module Size, millimeters	88,9 × 63,5 × 22,2	88,9 × 63,5 × 22,2	88,9 × 63,5 × 31,8	88,9 × 63,5 × 31,8
Module Weight	14 oz.(397g)	14 oz.(397g)	18 oz.(510g)	18 oz.(510g)
Case/Pin Configuration	D1	D1	D2	D2
Other Versions	E,J(1)	E,J(1)	E,J	E,J
Price (1-9)	**$45.00**	**$55.50**	**$75.50**	**$60.00**

NOTES: 1. For "E" version module size is D2 (3.5 × 2.5 × 1.25 inches, 18 oz.)
2. For UCM-5/2000 and BCM-15/300 operating temp. range should be restricted for a max. case temperature of 80° C in use.
3. All outputs are short circuit protected — current limited

This line of popular power supplies has input-output connections made to a terminal strip on top of the modules. These supplies are useful in applications where it is impractical or undesirable to use printed circuit cards or sockets. For simple mounting to a metal chassis, screw inserts are provided on the bottom of the modules.

INPUT VOLTAGE SPECIFICATIONS

Standard Input Specification:
115VAC ±10% @ 60-440 Hz.
E version: 220VAC ±10% @ 48-440 Hz.
J version: 100VAC ±10% @ 48-440 Hz.



UCM-5/2000	BCM-15/60	BCM-15/100	BCM-15/200	BCM-15/300
5VDC	±15VDC	±15VDC	±15VDC	±15VDC
±1%	±1%	±1%	±1%	±1%
2.0A	±60mA	100mA	200mA	300mA
.05%	.02%	.02%	.02%	.02%
.01%	.05%	.05%	.05%	.05%
.02%/° C	.02%/° C	.02%/° C	.02%/° C	.02%/° C
1mV	2mV	2mV	2mV	2mV
.005Ω	0.2Ω	0.1Ω	.05Ω	.05Ω
50μsec.	50μsec.	50μsec.	50μsec.	50μsec.
100 Meg.	100 Meg.	100 Meg.	100 Meg.	100 Meg.
250pF	250pF	250pF	250pF	250pF
1500VAC	1500VAC	1500VAC	1500VAC	1500VAC
(2)	-25° C to +71° C (No Derating)			(2)
	-25° C to +85° C			
Phenolic	Phenolic	Phenolic	Phenolic	Phenolic
3.5 × 2.5 × 1.56	3.5 × 2.5 × .875	3.5 × 2.5 × .875	3.5 × 2.5 × 1.25	3.5 × 2.5 × 1.56
88,9 × 63,5 × 39,6	88,9 × 63,5 × 22,2	88,9 × 63,5 × 22,2	88,9 × 63,5 × 31,8	88,9 × 63,5 × 39,6
24 oz.(680g)	14 oz.(397g)	14 oz.(397g)	18 oz.(510g)	24 oz.(680g)
D3	D1	D1	D2	D3
E,J	E,J(1)	E,J(1)	E,J	E,J
$86.00	**$45.00**	**$61.00**	**$71.50**	**$86.00**

THESE POWER SUPPLIES ARE COVERED BY GSA CONTRACT

Triple Output Modules

These power modules are specially designed for operation with data conversion and other circuits where both a dual analog supply and a 5V logic supply are required. Using a triple output supply to power these circuits can be more economical than using two separate equivalent supplies.

INPUT VOLTAGE SPECIFICATIONS

Standard input specifications: 115VAC ±10% @ 60-440 Hz
E version: 220VAC ±10% @ 48-440 Hz.
J version: 100VAC ±10% @ 48-440 Hz.

Mating MS-13 sockets are $4.00 each

SPECIFICATIONS	TPM-15/100-5/500 TPM-12/100-5/500	TPM-15/200-5/500 TPM-12/200-5/500	TPM-15/150-5/1000 TPM-12/150-5/1000
Output Voltages, dual 15V	±15VDC/5VDC	±15VDC/5VDC	±15VDC/5VDC
Output Voltages, dual 12V	±12VDC/5VDC	±12VDC/5VDC	±12VDC/5VDC
Output Voltage Accuracy	±1%	±1%	±1%
Rated Output Current	±100mA/500mA	±200mA/500mA	±150mA/1000mA
Line Regulation, max.	.02%/.05%	.02%/.05%	.02%/.05%
Load Regulation, max.	.05%/0.1%	.05%/0.1%	.05%/0.1%
Temperature Coefficient, max.	.02%/° C	.02%/° C	.02%/° C
Output Ripple, RMS max.	2mV/1mV	2mV/1mV	2mV/1mV
Output Impedance, max.	0.1/.05 ohm	0.1/.05 ohm	0.1/.05 ohm
Transient Recovery Time, max.	50μsec.	50μsec.	50μsec.
Isolation Resistance, min.	100 Meg.	100 Meg.	100 Meg.
Isolation Capacitance, max.	250pF	250pF	250pF
Breakdown Voltage, min.	1500VAC	1500VAC	1500VAC
Operating Temp. Range	-25° C to +71° C		
Storage Temp. Range	-25° C to +85° C		
Case Material	Phenolic	Phenolic	Phenolic
Module Size, inches	3.5 × 2.5 × 1.56	3.5 × 2.5 × 1.56	3.5 × 2.5 × 1.56
Module Size, millimeters	88,9 × 63,5 × 39,6	88,9 × 63,5 × 39,6	88,9 × 63,5 × 39,6
Module Weight	24 oz. (681g)	24 oz. (681g)	24 oz. (681g)
Case/Pin Configuration	E3	E3	E3
Other Versions	E, J	E, J	E, J
Mating Socket	MS-13	MS-13	MS-13
Price (1-9)	**$72.50**	**$83.00**	**$93.50**

THESE NAMED MODELS ARE COVERED BY GSA CONTRACT

Modular Switching Supplies

GENERAL DESCRIPTION

These supplies are compact, line operated switching modules producing 5 VDC at 3 or 5 amperes with 80% efficiency. The design employs a monolithic switching regulator and Schottky rectifiers, operating at 20 KHz minimum to give silent operation. The output has an overvoltage protection circuit with SCR crowbar fixed at 6.5V and also short circuit protection. The USM-5/3 and USM-5/5 produce no output overshoot on turn-on or turn-off.

Input voltage specification 90 to 130 VAC, 47 to 450 Hz. Mating MS-7 sockets are $3.50 each.

INPUT VOLTAGE SPECIFICATION

90 to 130 VAC, 47 to 450 Hz
Mating MS-7 sockets are $4.00 each.

SPECIFICATIONS 25° C	USM-5/3	USM-5/5
Output Voltage	5VDC	5VDC
Output Voltage Accuracy	±1%	±1%
Rated Output Current	3 Amps	5 Amps
Efficiency, min.	80%	80%
Line Regulation, max.	.05%	.05%
Load Regulation, max.	0.1%	0.1%
Temp. Coefficient, max.	.02%/° C	.02%/° C
Output Ripple, P-P, max.	50 mV	50mV
Output Impedance, max.	.001Ω	.002Ω
Trans. Recovery Time, typ.	300μsec.	300μsec.
Isolation Resistance, min.	50 Meg.	50 Meg.
Isolation Capacitance, typ.	100pF	100pF
Breakdown Voltage, min.	1800VAC	1800VAC
Operating Temp. Range	-25° C to +71° C	
Storage Temp. Range	-25° C to +85° C	
Case Material	Phenolic	Phenolic
Module Size, inches	3.5×2.5×1.25	3.5×2.5×1.25
Module Size, millimeters	88,9×63,5×31,8	88,9×63,5×31,8
Module Weight	14 oz. (397g)	14 oz. (397g)
Case/Pin Configuration	C2	C2
Mating Socket	MS-7	MS-7
Price (1-9)	**$98.50**	**$114.50**

NOTE: For the USM-5/5 only-derate 60mA/° C from 35° C to 71° C

THESE POWER SUPPLIES ARE COVERED BY GSA CONTRACT

High Voltage Dual Output Modules

DESCRIPTION

This series of dual high voltage supplies is specially designed for use with high voltage operational amplifiers such as Datel Systems AM-300 series. The 3 supplies in this series offer output voltages of ±120, ±150, and ±180 volts with excellent regulation, stability, and low output ripple.

INPUT VOLTAGE SPECIFICATIONS

Standard input specification: 115VAC ±10% @ 60-550 Hz.
E version: 220VAC ±10% @ 48-440 Hz.
J version: 100VAC ±10% @ 48-440 Hz.

Mating MS-13 sockets are $4.00 each

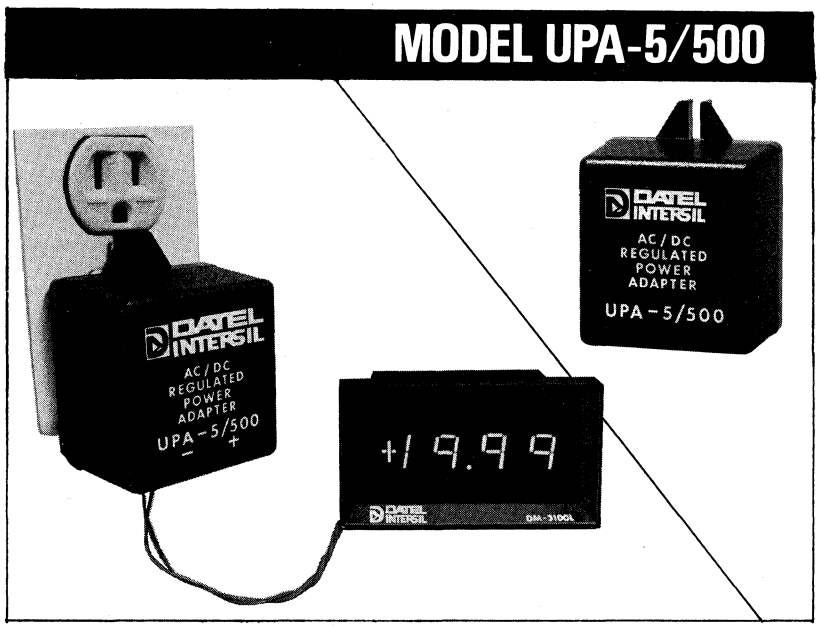
SPECIFICATIONS, 25° C	BPM-120/25	BPM-150/20	BPM-180/16
Output Voltage	±120VDC	±150VDC	±180VDC
Output Voltage Accuracy	±1%	±1%	±1%
Rated Output Current	25mA	20mA	16mA
Line Regulation, max.	.05%	.05%	.05%
Load Regulation, max.	0.2%	0.2%	0.2%
Temperature Coefficient, max.	.02%/° C	.02%/° C	.02%/° C
Output Ripple, RMS max.	10mV	10mV	10mV
Output Impedance, max.	5 ohms	5 ohms	5 ohms
Transient Recovery Time, max.	50μsec.	50μsec.	50μsec.
Isolation Resistance, min.	100 Meg.	100 Meg.	100 Meg.
Isolation Capacitance, max.	250pF	250pF	250pF
Breakdown Voltage, min.	1500VAC	1500VAC	1500VAC
Operating Temp. Range	-25° C to +71° C (No Derating)		
Storage Temp. Range	-25° C to +85° C		
Case Material	Phenolic	Phenolic	Phenolic
Module Size, inches	3.5 × 2.5 × 1.56	3.5 × 2.5 × 1.56	3.5 × 2.5 × 1.56
Module Size, millimeters	88,9 × 63,5 × 39,6	88,9 × 63,5 × 39,6	88,9 × 63,5 × 39,6
Module Weight	24 oz. (681g.)	24 oz. (681g.)	24 oz. (681 g.)
Case/Pin Configuration	C3	C3	C3
Other Versions	E,J	E,J	E,J
Mating Socket	MS-7	MS-7	MS-7
Price (1-9)	**$86.00**	**$86.00**	**$86.00**

THESE POWER SUPPLIES ARE COVERED BY GSA CONTRACT

Plug-In Regulated Power Adapter AC to DC

Only
$15.75

The 5 Volt Source For Digital Panel Meters



FEATURES

- Low Cost
- Isolated - Low Voltage Operation of Product
- Flame Retardant Molded Case
- Designated for U.L. and C.S.A. Listing
- Portable Power Supply
- Direct Plug-in to U.S. AC Outlets

ADVANTAGES

- No Heat Dissipation
- Easier Maintenance of Power Source
- Reduction or Elimination of the Costly Need to Submit Equipment for U.L. or C.S.A. Investigation
- Ease of Replacement

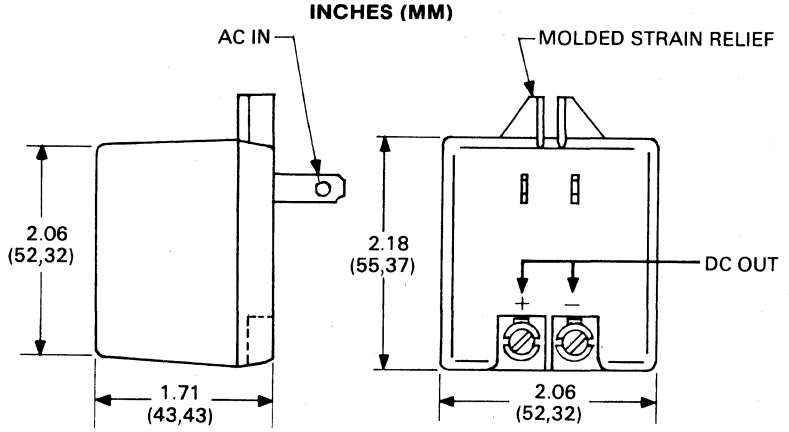
DC OUTPUT
▸ 5VDC @ 500mA

SPECIFICATIONS

Input Voltage.....115VAC ± 10%
Input Frequency.....60 Hz
Output Voltage.....+4.8 to +5.3Vdc
Output Current.....0-500 mA
Regulation (0 to 500mA)
Line and Load.....0.3% typ.
Ripple/Noise.....8mV RMS max.
Breakdown Voltage.....1500VAC min.

DIMENSIONS AND CONNECTIONS

MECHANICAL DIMENSIONS
INCHES (MM)



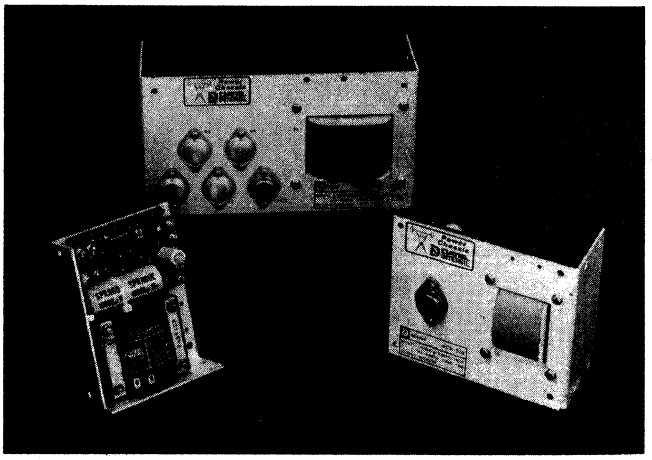
Power Chassis Series: Open Frame Power Supplies

MODEL	OUTPUT VOLTAGE & CURRENT (0 to 50° C)	LINE REG. (MAX.)	LOAD REG. (MAX.)	TEMPCO (MAX.)	OUTPUT IMPED. (MAX.)
SINGLE OUTPUT					
PCS-5/3	5V @ 3.0A	.05%	0.1%	.02%/° C	1.6mΩ
PCS-5/6	5V @ 6.0A	.05%	0.1%	.02%/° C	0.9mΩ
PCS-5/12	5V @ 12.0A	.05%	0.1%	.02%/° C	0.5mΩ
PCS-5/18	5V @ 18.0A	.05%	0.1%	.02%/° C	0.3mΩ
DUAL OUTPUT					
PCD-12/1	±12V @ 1.0A	.05%	0.1%	.02%/° C	15mΩ
PCD-15/1	±15V @ 1.0A	.05%	0.1%	.02%/° C	15mΩ
PCD-12/2	±12V @ 2A	.05%	0.1%	.02%/° C	7.5mΩ
PCD-15/2	±15V @ 2A	.05%	0.1%	.02%/° C	7.5mΩ
PCD-12/3	±12V @ 3.0A	.05%	0.1%	.02%/° C	5mΩ
PCD-15/3	±15V @ 3.0A	.05%	0.1%	.02%/° C	5mΩ
TRIPLE OUTPUT					
PCT-12/1-5/3	±12V @ 1A/5V @ 3A	.05/0.1%	.05/0.1%	.02%/° C	15mΩ
PCT-15/1-5/3	±15V @ 1A/5V @ 3A	.05/0.1%	.05/0.1%	.02%/° C	15mΩ
PCT-12/2-5/6	±12V @ 2A/5V @ 6A	.05/0.1%	.05/0.1%	.02%/° C	7.5mΩ
PCT-15/2-5/6	±15V @ 2A/5V @ 6A	.05/0.1%	.05/0.1%	.02%/° C	7.5mΩ
PCT-12/3-5/12	±12V @ 3A/5V @ 12A	.05/0.1%	.05/0.1%	.02%/° C	5mΩ
PCT-15/3-5/12	±15V @ 3A/5V @ 12A	.05/0.1%	.05/0.1%	.02%/° C	5mΩ

NOTES: 1. Input voltage is selected by transformer connection.
2. Derated to 40% of output current at 71° C.

GENERAL SPECIFICATIONS
COMMON TO ALL MODELS

Input Voltage[1] ..... 115/230VAC ±10%
Line Frequency ..... 48-440 Hz
Output Voltage Adjustment ..... ±10%
Output Ripple ..... 2mV RMS, max.
Transient Response ..... 50μsec. max.
Output Protection ..... Current Limiting or Foldback Limiting
Isolation Resistance ..... 100 Meg. min.
Voltage Stability, after warmup .... ±0.25%, 24 hours
Isolation Capacitance ..... 250pF max.
Breakdown Voltage ..... 1500VAC min.
Operating Temperature Range .... 0° C to 50° C (No Derating)
Storage Temperature Range[2] ..... -25° C to +85° C

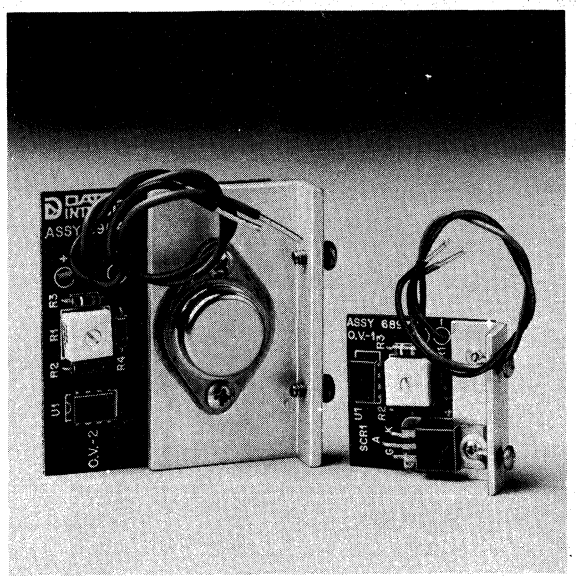


CHASSIS SIZE INCHES (LxHxW)	CHASSIS SIZE (CM)	WEIGHT (LBS.)	WEIGHT (KG.)	PRICES (1-9)
4.9 X 4.0 X 1.6	12 X 10 X 4	2	.91	**$ 35.00**
5.6 X 4.9 X 2.5	14 X 12 X 6	3	1.4	**$ 55.00**
9.0 X 5.1 X 2.8	23 X 13 X 7	7.2	3.3	**$ 85.00**
14 X 5.1 X 2.8	36 X 13 X 7	9.8	4.5	**$115.00**
6.5 X 4 X 1.62	26 X 16 X 6.48	1.6	3.52	**$ 59.00**
6.5 X 4 X 1.62	26 X 16 X 6.48	1.6	3.52	**$ 59.00**
7 X 4.87 X 2.5	28 X 19.48 X 10	3.6	7.92	**$ 75.00**
7 X 4.87 X 2.5	28 X 19.48 X 10	3.6	7.92	**$ 75.00**
9.38 X 4.87 X 2.75	37.52 X 19.48 X 11	55	12.1	**$ 89.00**
9.38 X 4.87 X 2.75	37.52 X 19.48 X 11	55	12.1	**$ 89.00**
10.25 X 4 X 2.5	41 X 16 X 10	4.2	9.24	**$ 89.00**
10.25 X 4 X 2.5	41 X 16 X 10	4.2	9.24	**$ 89.00**
11.25 X 4.87 X 2.75	45 X 19.48 X 11	5.8	12.76	**$105.00**
11.25 X 4.87 X 2.75	45 X 19.48 X 11	5.8	12.76	**$105.00**
14.25 X 5.1 X 2.75	57 X 20.4 X 11	9.8	21.56	**$159.00**
14.25 X 5.1 X 2.75	57 X 20.4 X 11	9.8	21.56	**$159.00**

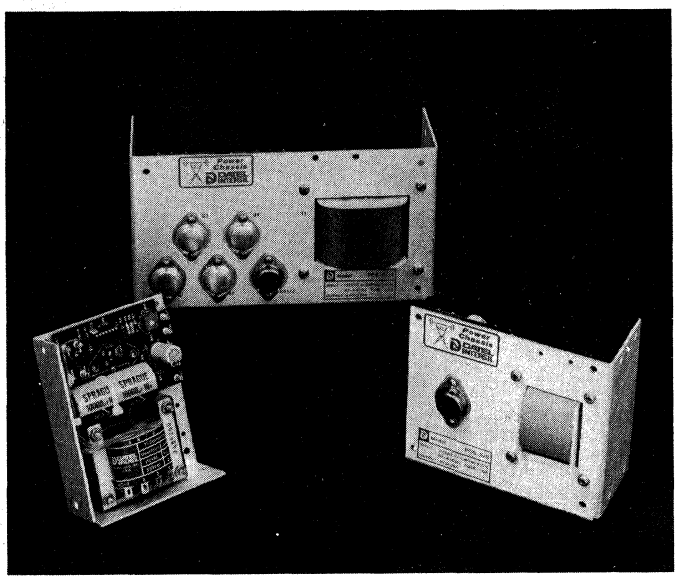
THESE POWER SUPPLIES ARE COVERED BY GSA CONTRACT

Overvoltage Protection Modules

OV-1 AND OV-2 MODULES



OV MODULES ARE USED WITH THE PC SERIES OPEN FRAME SUPPLIES



OVERVOLTAGE PROTECTION

OV-1 and OV-2 are available for use with the Power Chassis (PC) series of open frame power supplies.

The OV models are only designed for use with the 5 volt outputs on the PC series. Each model has a screwdriver pot adjustment — adjustable from 6.0V to 8.0V.

MODELS

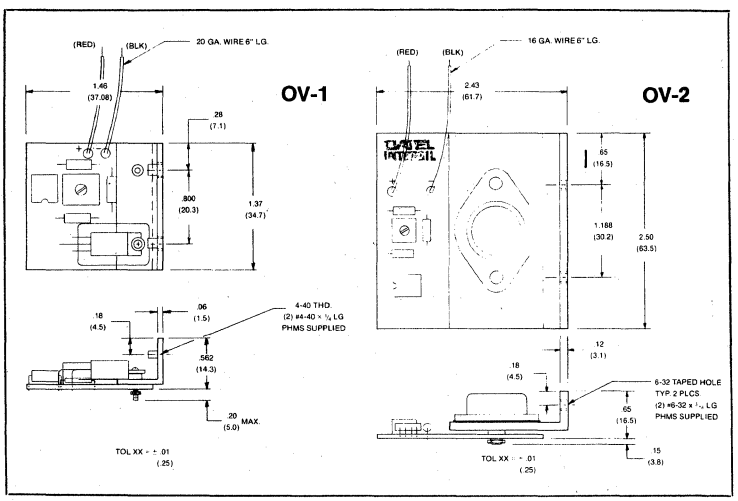
OV-1 — for 3 and 6 Amp PC models
Used with PCS-5/3
PCS-5/6
PCT-5/3-12/1
PCT-5/3-15/1
PCT-5/6-12/1
PCT-5/6-15/1

OV-2 for 12 and 18 Amp PC models
Used with: PCS-5/12
PCS-5/18
PCT-5/12-12/2
PCT-5/12-15/2

CUSTOM

Overvoltage protection modules are available for other open frame power supply outputs, but on special request only. Contact the factory for voltage ranges that can be custom designed.

MECHANICAL DIMENSIONS



Mounting holes are provided in the PC series open frames for the OV modules

PRICE: (1-9)

OV-1	**$ 8.00**
OV-2	**$10.00**

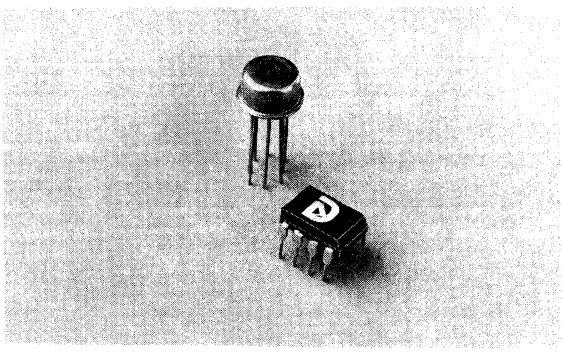
Monolithic Voltage Converter

FEATURES

- **Simple Conversion of +5V Logic Supply to ±5V Supplies**
- **Simple Voltage Multiplication (V_{OUT} = (−) nV_{IN})**
- **99.9% Typical Open Circuit Voltage Conversion Efficiency**
- **98% Typical Power Efficiency**
- **Wide Operating Voltage Range 1.5V to 10.0V**
- **Easy to use - Requires only 2 External Non-Critical Passive Components**

APPLICATIONS

- On Board Negative Supply for up to 64 Dynamic RAMs.
- Localized μ-Processor (8080 type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems



GENERAL DESCRIPTION

The VI-7660 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The VI-7660 performs the complete supply voltage conversion from positive to negative for an input range of +1.5V to +10.0V, resulting in complementary output voltages of −1.5 to −10.0V with the addition of only 2 non-critical external capacitors needed for the charge pump and charge reservoir functions. Note that an additional diode is required for V_{SUPPLY} >6.5V.

Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, four output power MOS switches, and a unique logic element which senses the most negative voltage in the device and ensures that the output N-channel switches are not forward biased. This assures latch-up free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be over-driven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5 to +10.0 volts), the LV pin is left floating to prevent device latchup.

Typical applications for the VI-7660 will be data acquisition and microprocessor based systems where there is a +5 volt supply available for the digital functions and an additional −5 volt supply is required for the analog functions. The VI-7660 is also ideally suited for providing low current, −5V body bias supply for dynamic RAMs.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 10.5V
Oscillator Input Voltage (Note 1) ..... −0.3V to (V^+ +0.3V) for V^+ < 5.5V
(V^+ −5.5V) to (V^+ +0.3V) for V^+ > 5.5V
−0.3V to (V^+ +0.3V) for V^+ < 3.5V
LV (Note 1) ..... No connection for V^+ > 3.5V
Output Short Duration (V_{SUPPLY} ≤5.5V) ..... Continuous
Power Dissipation (Note 2)
VI-7660C 500mW
VI-7660PC 300mW
VI-7660M 500mW

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS

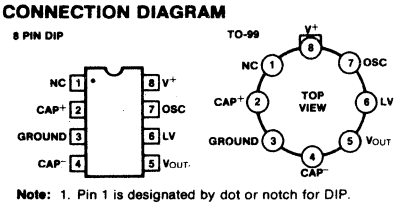
V^+ = 5V, T_A = 25°C, C_{OSC} = 0, Test Circuit Figure 1 (unless otherwise specified)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
I^+	Supply Current		170	500	μA	R_L = ∞
V^+_{H1}	Supply Voltage Range - Hi	3.0		6.5	V	0°C ≤ T_A ≤ 70°C, R_L = 10kΩ, LV = No Connection
	(Dx out of circuit)	3.0		5.0	V	−55°C ≤ T_A ≤ 125°C, R_L = 10kΩ, LV = Ground
V^+_{L1}	Supply Voltage Range - Lo (Dx out of circuit)	1.5		3.5	V	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV = Ground
V^+_{H2}	Supply Voltage Range - Hi (Dx in circuit)	3.0		10.0	V	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV = No Connection
V^+_{L2}	Supply Voltage Range - Lo (Dx in circuit)	1.5		3.5	V	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV = Ground
R_{OUT}	Output Source Resistance		55	100	Ω	I_{OUT} = 20mA, T_A = 25°C
				120	Ω	I_{OUT} = 20mA, −20°C ≤ T_A ≤ +70°C
				150	Ω	I_{OUT} = 20mA, −55°C ≤ T_A ≤ +125°C
				300	Ω	V^+ = 2V, I_{OUT} = 3mA, LV = Ground, −20°C ≤ T_A ≤ +70°C
				400	Ω	V^+ = 2V, I_{OUT} = 3mA, LV = Ground, −55°C ≤ T_A ≤ +125°C, Dx in circuit
f_{OSC}	Oscillator Frequency		10		kHz	
P_{Ef}	Power Efficiency	95	98		%	R_L = 5kΩ
$V_{OUT\ Ef}$	Voltage Conversion Efficiency	97	99.9		%	R_L = ∞
Z_{OSC}	Oscillator Impedance		1.0		MΩ	V^+ = 2 Volts
			100		kΩ	V^+ = 5 Volts

Notes: 1. Connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the VI-7660.
2. Derate linearly above 50°C by 5.5mW/°C.

VI-7660

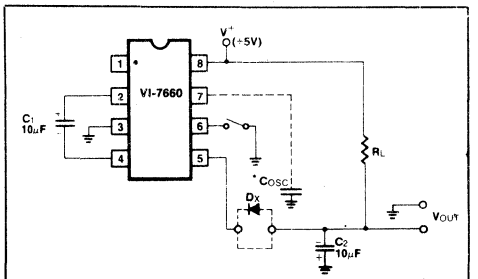
CONNECTION DIAGRAM



Note: 1. Pin 1 is designated by dot or notch for DIP.

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE	1-24
VI-7660C	−20° C to + 70° C	TO-99	$3.45
VI-7600PC	−20° C to + 70° C	8 PIN MINI DIP	$2.99
VI-7660M	55° C to +125° C	TO-99	$8.85



NOTES: 1. For large value of C_{OSC} (>1000pF) the values of C_1 and C_2 should be increased to 100μF.
2. D_X is required for supply voltages greater than 6.5V @ −55° ≤ T_A ≤ +70°C; refer to performance curves for additional information.

Figure 1: VI-7660 Test Circuit

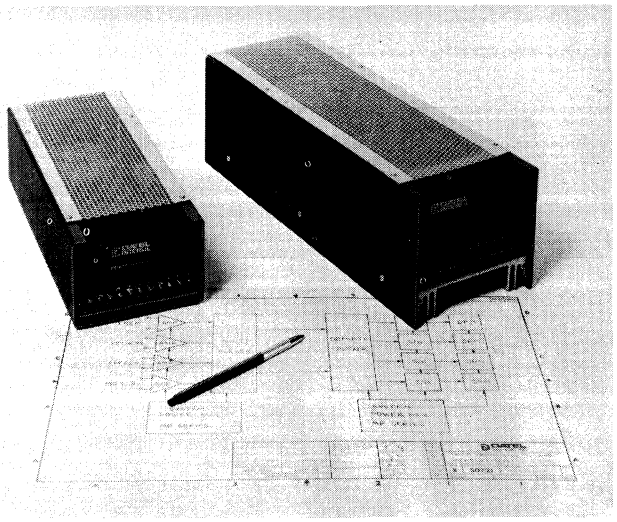
MP Series: High Power Enclosed Modular Supplies

MODEL	OUTPUT VOLTAGE & CURRENT (0 to 65° C)	OUTPUT 1 AT 71° C[1]	LINE REG. (MAX.)[2]	LOAD REG. (MAX.)[3]	TEMPCO (TYPICAL)	RIPPLE (RMS MAX.)[4]
SINGLE OUTPUT						
MPS-5/3	5V @ 3.0A	2.5A	0.1%	0.1%	.01%/° C	1mV
MPS-5/6	5V @ 6.0A	5.0A	0.1%	0.1%	.01%/° C	1mV
MPS-5/12	5V @ 12.0A	10.0A	0.1%	0.1%	.01%/° C	1mV
MPS-5/18	5V @ 18.0A	15.0A	0.1%	0.1%	.01%/° C	1mV
DUAL OUTPUT						
MPD-12/1	±12V @ 1.0A	0.85A	.05%	.05%	.01%/° C	1mV
MPD-15/1	±15V @ 1.0A	0.85A	.05%	.05%	.01%/° C	1mV
MPD-12/1.5	±12V @ 1.5A	1.25A	.05%	.05%	.01%/° C	1mV
MPD-15/1.5	±15V @ 1.5A	1.25A	.05%	.05%	.01%/° C	1mV
MPD-12/3	±12V @ 3.0A	2.5A	.05%	.05%	.01%/° C	1mV
MPD-15/3	±15V @ 3.0A	2.5A	.05%	.05%	.01%/° C	1mV
TRIPLE OUTPUT						
MPT-12/1-5/3	±12V @ 1A/5V @ 3A	0.85/2.5A	.05/0.1%	.05/0.1%	.01%/° C	1mV
MPT-15/1-5/3	±15V @ 1A/5V @ 3A	0.85/2.5A	.05/0.1%	.05/0.1%	.01%/° C	1mV
MPT-12/1.5-5/6	±12V @ 1.5A/5V @ 6A	1.25/5.0A	.05/0.1%	.05/0.1%	.01%/° C	1mV
MPT-15/1.5-5/6	±15V @ 1.5A/5V @ 6A	1.25/5.0A	.05/0.1%	.05/0.1%	.01%/° C	1mV
MPT-12/1.5-5/12	±12V @ 1.5A/5V @ 12A	1.25/10.0A	.05/0.1%	.05/0.1%	.01%/° C	1mV
MPT-15/1.5-5/12	±15V @ 1.5A/5V @ 12A	1.25/10.0A	.05/0.1%	.05/0.1%	.01%/° C	1mV

NOTES: 1. 15% derating from 65° C output.
2. For ±10% line change.
3. No load to full load.
4. Typically 3mV peak to peak.
5. 0.1% tracking over operating temp. range.

GENERAL SPECIFICATIONS
COMMON TO ALL MODELS

Input Voltage ..... 115/230VAC ±10%
Line Frequency ..... 48-440 Hz
Output Voltage Adjustment ..... ±5%
Output Ripple ..... 1mV RMS, max.
3mV P-P typ.
Transient Response ..... 50 μsec. max.
Output Protection ..... Current Limiting or
Foldback Limiting
Overvoltage Protection, 5V outputs ... 6.2V ±5%
Voltage Stability, after warmup ..... ±0.25%, 24 hours
Dual Output Tracking ..... .05%, 0.1% over
temp. range
Operating Temperature Range ..... 0° C to 71° C
Storage Temperature Range ..... -25° C to +85° C



EFFICIENCY (NOM. LINE)	TRACKING (DUALS)[5]	REMOTE SENSING	OVER-VOLT. PROTECTION	CASE SIZE (H × W × L, INCHES/CM)	WEIGHT (LBS./KG)	PRICE (1-9)
40%	—	YES	YES	2.0 × 4.6 × 7.6 /50,8 × 116,8 × 193,0	3.6/1,6	**$ 62.00**
40%	—	YES	YES	4.9 × 5.3 × 10.3/12,4 × 13,5 × 26,2	6.5/2,9	**$ 93.50**
40%	—	YES	YES	4.9 × 5.3 × 11.9/12,4 × 13,5 × 30,2	10.4/4,7	**$146.00**
40%	—	YES	YES	4.9 × 5.3 × 11.9/12,4 × 13,5 × 30,2	14.0/6,3	**$167.00**
50%	.05%	YES	NO	2.5 × 4.9 × 10.0/6,4 × 12,4 × 25,4	5.0/2,3	**$ 93.50**
50%	.05%	YES	NO	2.5 × 4.9 × 10.0/6,4 × 12,4 × 25,4	5.0/2,3	**$ 93.50**
50%	.05%	YES	NO	3.7 × 5.3 × 10.3/9,4 × 13,5 × 26,2	6.5/2,9	**$110.00**
50%	.05%	YES	NO	3.7 × 5.3 × 10.3/9,4 × 13,5 × 26,2	6.5/2,9	**$110.00**
50%	.05%	YES	NO	4.9 × 5.3 × 10.3/12,4 × 13,5 × 26,2	10.5/4,8	**$150.00**
50%	.05%	YES	NO	4.9 × 5.3 × 10.3/12,4 × 13,5 × 26,2	10.5/4,8	**$150.00**
45%	.05%	5V ONLY	5V ONLY	3.4 × 4.9 × 11.0/8,6 × 12,4 × 27,9	11.0/5,0	**$146.00**
45%	.05%	5V ONLY	5V ONLY	3.4 × 4.9 × 11.0/8,6 × 12,4 × 27,9	11.0/5,0	**$146.00**
45%	.05%	5V ONLY	5V ONLY	4.9 × 5.3 × 14.0/12,4 × 13,5 × 35,6	14.0/6,3	**$183.00**
45%	.05%	5V ONLY	5V ONLY	4.9 × 5.3 × 14.0/12,4 × 13,5 × 35,6	14.0/6,3	**$183.00**
45%	.05%	5V ONLY	5V ONLY	4.9 × 5.3 × 15.6/12,4 × 13,5 × 39,6	17.0/7,7	**$235.00**
45%	.05%	5V ONLY	5V ONLY	4.9 × 5.3 × 15.6/12,4 × 13,5 × 39,6	17.0/7,7	**$235.00**

THESE POWER SUPPLIES ARE COVERED BY GSA CONTRACT

1 and 3 Watt DC-DC Converters

1 WATT SERIES

MODEL	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	INPUT VOLT. TOLERANCE	NO LOAD INPUT CURRENT	FULL LOAD INPUT CURRENT	EFFICIENCY (FULL LOAD)	LINE REGULATION
UPM-5/200-D12	+ 5V	200mA	12VDC	±10%	40mA	170mA	50%	.05%
UPM-5/200-D28	+ 5V	200mA	28VDC	±10%	20mA	72mA	50%	.05%
UPM-12/80-D5	+12V	80mA	5VDC	±10%	95mA	370mA	50%	.05%
UPM-12/80-D28	+12V	80mA	28VDC	±10%	20mA	65mA	55%	.05%
UPM-24/40-D5	+24V	40mA	5VDC	±10%	95mA	370mA	50%	.05%
UPM-24/40-D12	+24V	40mA	12VDC	±10%	40mA	150mA	55%	.05%
UPM-28/25-D5	+28V	25mA	5VDC	±10%	70mA	280mA	50%	.05%
UPM-28/25-D12	+28V	25mA	12VDC	±10%	40mA	105mA	55%	.05%
BPM-12/25-D5	±12V	25mA	5VDC	±10%	90mA	220mA	55%	.05%
BPM-12/25-D12	±12V	25mA	12VDC	±10%	25mA	90mA	55%	.05%
BPM-12/25-D28	±12V	25mA	28VDC	±10%	15mA	38mA	55%	.05%
BPM-15/25-D5	±15V	25mA	5VDC	±10%	80mA	300mA	50%	.05%
BPM-15/25-D12	±15V	25mA	12VDC	±10%	40mA	115mA	55%	.05%
BPM-15/25-D28	±15V	25mA	28VDC	±10%	15mA	48mA	55%	.05%
BPM-18/25-D5	±18V	25mA	5VDC	±10%	95mA	370mA	50%	.05%
BPM-18/25-D12	±18V	25mA	12VDC	±10%	40mA	136mA	55%	.05%
BPM-18/25-D28	±18V	25mA	28VDC	±10%	15mA	58mA	55%	.05%

3 WATT SERIES

MODEL	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	INPUT VOLT. TOLERANCE	NO LOAD INPUT CURRENT	FULL LOAD INPUT CURRENT	EFFICIENCY (FULL LOAD)	LINE REGULATION
UPM-5/500-D12	+ 5V	500mA	12VDC	±10%	100mA	470mA	45%	.05%
UPM-5/500-D28	+ 5V	500mA	28VDC	±10%	50mA	200mA	45%	.05%
UPM-12/250-D5	+12V	250mA	5VDC	±10%	300mA	1250mA	50%	.05%
UPM-12/250-D28	+12V	250mA	28VDC	±10%	50mA	195mA	55%	.05%
UPM-24/125-D5	+24V	125mA	5VDC	±10%	300mA	1250mA	50%	.05%
UPM-24/125-D12	+24V	125mA	12VDC	±10%	90mA	450mA	55%	.05%
UPM-28/100-D5	+28V	100mA	5VDC	±10%	270mA	1120mA	50%	.05%
UPM-28/100-D12	+28V	100mA	12VDC	±10%	90mA	420mA	55%	.05%
BPM-12/100-D5	±12V	100mA	5VDC	±10%	210mA	960mA	50%	.05%
BPM-12/100-D12	±12V	100mA	12VDC	±10%	90mA	400mA	50%	.05%
BPM-12/100-D28	±12V	100mA	28VDC	±10%	40mA	156mA	55%	.05%
BPM-15/100-D5	±15V	100mA	5VDC	±10%	350mA	1300mA	45%	.05%
BPM-15/100-D12	±15V	100mA	12VDC	±10%	80mA	460mA	55%	.05%
BPM-15/100-D28	±15V	100mA	28VDC	±10%	50mA	195mA	55%	.05%
BPM-18/100-D5	±18V	100mA	5VDC	±10%	350mA	1500mA	50%	.05%
BPM-18/100-D12	±18V	100mA	12VDC	±10%	120mA	545mA	55%	.05%
BPM-18/100-D28	±18V	100mA	28VDC	±10%	60mA	240mA	55%	.05%

LOAD REGULATION	TEMP. COEFFICIENT	OUTPUT IMPEDANCE	CASE CONFIG.	PRICE (1-9)
0.1%	.02%/° C	.07Ω	F	**$44.00**
0.1%	.02%/° C	.07Ω	F	**$44.00**
.05%	.02%/° C	.02Ω	F	**$44.00**
.05%	.02%/° C	.02Ω	F	**$44.00**
.05%	.02%/° C	.02Ω	F	**$44.00**
.05%	.02%/° C	.02Ω	F	**$44.00**
.05%	.02%/° C	.02Ω	F	**$44.00**
.05%	.02%/° C	.02Ω	F	**$44.00**
.05%	.02%/° C	.02Ω	F	**$51.50**
.05%	.02%/° C	.02Ω	F	**$51.50**
.05%	.02%/° C	.02Ω	F	**$51.50**
.05%	.02%/° C	.02Ω	F	**$51.50**
.05%	.02%/° C	.02Ω	F	**$51.50**
.05%	.02%/° C	.02Ω	F	**$51.50**
.05%	.02%/° C	.02Ω	F	**$51.50**
.05%	.02%/° C	.02Ω	F	**$51.50**
.05%	.02%/° C	.02Ω	F	**$51.50**

LOAD REGULATION	TEMP. COEFFICIENT	OUTPUT IMPEDANCE	CASE CONFIG.	PRICE (1-9)
0.1%	.02%/° C	.07Ω	G1	**$67.00**
0.1%	.02%/° C	.07Ω	G1	**$67.00**
.05%	.02%/° C	0.2Ω	G1	**$67.00**
.05%	.02%/° C	0.2Ω	G1	**$67.00**
.05%	.02%/° C	0.2Ω	G1	**$67.00**
.05%	.02%/° C	0.2Ω	G1	**$67.00**
.05%	.02%/° C	0.2Ω	G1	**$67.00**
.05%	.02%/° C.	0.2Ω	G1	**$67.00**
.05%	.02%/° C	0.2Ω	G1	**$72.50**
.05%	.02%/° C	0.2Ω	G1	**$72.50**
.05%	.02%/° C	0.2Ω	G1	**$72.50**
.05%	.02%/° C	0.2Ω	G1	**$72.50**
.05%	.02%/° C	0.2Ω	G1	**$72.50**
.05%	.02%/° C	0.2Ω	G1	**$72.50**
.05%	.02%/° C	0.2Ω	G1	**$72.50**
.05%	.02%/° C	0.2Ω	G1	**$72.50**
.05%	.02%/° C	0.2Ω	G1	**$72.50**

DESCRIPTION

This broad line of DC-DC converters features 17 one watt models and 18 three watt models with single and dual output voltages. Input voltages are 5, 12, and 28V with single outputs of 5, 12, 24, and 28V, and dual outputs of ±12, ±15, and ±18V. Output voltage accuracies are ±1% with .02%/°C temperature coefficient. Other features include low output ripple, 100 megohm isolation, and output current limiting.

GENERAL SPECIFICATIONS—ALL MODELS

Output Voltage Accuracy	±1%
Output Noise and Ripple, max.	20mV P-P (2mV RMS)
Back Ripple Current, max.	1% of I_{IN}
Capacitive Coupling, max.	250 pF
Breakdown Voltage, min.	300VDC
Transient Recovery Time, max.	50μsec.
Operating Temp. Range	-25°C to +71°C
Storage Temp. Range	-55°C to +85°C
Case Material	Diallyl Phthalate (G2)

MODULE SIZES

F Case:	1.5 × 2.0 × 0.375 inches 38,1 × 50,8 × 9,5 mm
Weight:	1.5 oz. (43g.)
G1 Case:	20 × 2.0 × 0.432 inches 50,8 × 50,8 × 11,0 mm
Weight:	2.5 oz. (71g.)

Both 1 and 3 watt series use 2 DILS-1 or DILS-2 terminal strips (at $6.00/pair) for sockets.

THESE DC-DC CONVERTERS ARE COVERED BY GSA CONTRACT

5 and 10 Watt DC-DC Converters

5 WATT SERIES

MODEL	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	INPUT VOLT. TOLERANCE	NO LOAD INPUT CURRENT	FULL LOAD INPUT CURRENT	EFFICIENCY (FULL LOAD)	LINE REGULATION
UPM-5/1000-D12	+ 5V	1000mA	12VDC	±10%	200mA	830mA	50%	.05%
UPM-5/1000-D28	+ 5V	1000mA	28VDC	±10%	100mA	360mA	50%	.05%
UPM-12/420-D5	+12V	420mA	5VDC	±10%	500mA	2000mA	50%	.05%
UPM-12/420-D28	+12V	420mA	28VDC	±10%	75mA	325mA	55%	.05%
UPM-24/210-D5	+24V	210mA	5VDC	±10%	400mA	1830mA	55%	.05%
UPM-24/210-D12	+24V	210mA	12VDC	±10%	170mA	760mA	55%	.05%
UPM-28/180-D5	+28V	180mA	5VDC	±10%	400mA	1830mA	55%	.05%
UPM-28/180-D12	+28V	180mA	12VDC	±10%	170mA	760mA	55%	.05%
BPM-12/210-D5	±12V	210mA	5VDC	±10%	500mA	2000mA	50%	.05%
BPM-12/210-D12	±12V	210mA	12VDC	±10%	170mA	760mA	55%	.05%
BPM-12/210-D28	±12V	210mA	28VDC	±10%	75mA	325mA	55%	.05%
BPM-15/165-D5	±15V	165mA	5VDC	±10%	500mA	2000mA	50%	.05%
BPM-15/165-D12	±15V	165mA	12VDC	±10%	170mA	760mA	55%	.05%
BPM-15/165-D28	±15V	165mA	28VDC	±10%	75mA	325mA	55%	.05%
BPM-18/140-D5	±18V	140mA	5VDC	±10%	500mA	2000mA	55%	.05%
BPM-18/140-D12	±18V	140mA	12VDC	±10%	170mA	760mA	55%	.05%
BPM-18/140-D28	±18V	140mA	28VDC	±10%	75mA	325mA	55%	.05%

10 WATT SERIES

MODEL	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	INPUT VOLT. TOLERANCE	NO LOAD INPUT CURRENT	FULL LOAD INPUT CURRENT	EFFICIENCY (FULL LOAD)	LINE REGULATION
UPM-5/2000-D12	+ 5V	2000mA	12VDC	±10%	300mA	1660mA	50%	.05%
UPM-5/2000-D28	+ 5V	2000mA	28VDC	±10%	150mA	720mA	50%	.05%
UPM-12/840-D5	+12V	840mA	5VDC	±10%	1000mA	4000mA	50%	.05%
UPM-12/840-D28	+12V	840mA	28VDC	±10%	150mA	650mA	55%	.05%
UPM-24/420-D5	+24V	420mA	5VDC	±10%	900mA	3600mA	55%	.05%
UPM-24/420-D12	+24V	420mA	12VDC	±10%	360mA	1530mA	55%	.05%
UPM-28/360-D5	+28V	360mA	5VDC	±10%	900mA	3600mA	55%	.05%
UPM-28/360-D12	+28V	360mA	12VDC	±10%	360mA	1530mA	55%	.05%
BPM-12/420-D5	±12V	420mA	5VDC	±10%	1000mA	4000mA	50%	.05%
BPM-12/420-D12	±12V	420mA	12VDC	±10%	360mA	1530mA	55%	.05%
BPM-12/420-D28	±12V	420mA	28VDC	±10%	150mA	650mA	55%	.05%
BPM-15/330-D5	±15V	330mA	5VDC	±10%	1000mA	4000mA	50%	.05%
BPM-15/330-D12	±15V	330mA	12VDC	±10%	360mA	1530mA	55%	.05%
BPM-15/330-D28	±15V	330mA	28VDC	±10%	150mA	650mA	55%	.05%
BPM-18/280-D5	±18V	280mA	5VDC	±10%	900mA	3600mA	55%	.05%
BPM-18/280-D12	±18V	280mA	12VDC	±10%	360mA	1530mA	55%	.05%
BPM-18/280-D28	±18V	280mA	28VDC	±10%	150mA	650mA	55%	.05%

LOAD REGULATION	TEMP. COEFFICIENT	OUTPUT IMPEDANCE	CASE CONFIG.	PRICE (1-9)
0.1%	.02%/°C	.005Ω	G2	**$72.50**
0.1%	.02%/°C	.005Ω	G2	**$72.50**
.05%	.02%/°C	.015Ω	G2	**$72.50**
.05%	.02%/°C	.15Ω	G2	**$72.50**
.05%	.02%/°C	.03Ω	G2	**$72.50**
.05%	.03%/°C	.03Ω	G2	**$72.50**
.05%	.02%/°C	.035Ω	G2	**$72.50**
.05%	.02%/°C	.035Ω	G2	**$72.50**
.05%	.02%/°C	.03Ω	G2	**$78.00**
.05%	.02%/°C	.03Ω	G2	**$78.00**
.05%	.02%/°C	.03Ω	G2	**$78.00**
.05%	.02%/°C	.03Ω	G2	**$78.00**
.05%	.02%/°C	.03Ω	G2	**$78.00**
.05%	.02%/°C	.03Ω	G2	**$78.00**
.05%	.02%/°C	.03Ω	G2	**$78.00**
.05%	.02%/°C	.03Ω	G2	**$78.00**
.05%	.02%/°C	.03Ω	G2	**$78.00**

LOAD REGULATION	TEMP. COEFFICIENT	OUTPUT IMPEDANCE	CASE CONFIG.	PRICE (1-9)
0.1%	.02%/°C	.005Ω	CB	**$93.50**
0.1%	.02%/°C	.005Ω	CB	**$93.50**
.05%	.02%/°C	.02Ω	CB	**$93.50**
.05%	.02%/°C	.02Ω	CB	**$93.50**
.05%	.02%/°C	.02Ω	CB	**$93.50**
.05%	.02%/°C	.02Ω	CB	**$93.50**
.05%	.02%/°C	.02Ω	CB	**$93.50**
.05%	.02%/°C	.02Ω	CB	**$93.50**
.05%	.02%/°C	.02Ω	CB	**$98.50**
.05%	.02%/°C	.02Ω	CB	**$98.50**
.05%	.02%/°C	.02Ω	CB	**$98.50**
.05%	.02%/°C	.02Ω	CB	**$98.50**
.05%	.02%/°C	.02Ω	CB	**$98.50**
.05%	.02%/°C	.02Ω	CB	**$98.50**
.05%	.02%/°C	.02Ω	CB	**$98.50**
.05%	.02%/°C	.02Ω	CB	**$98.50**

DESCRIPTION

This comprehensive line of higher power DC-DC converters features 34 different models with both single and dual outputs. Input voltages are 5, 12, and 28V with single output voltages of 5, 12, 24, and 28 volts, and dual outputs of ±12, ±15, and ±18 volts. Output voltage accuracies are ±1% with .02%/°C temperature coefficients. Other features include low output ripple, 100 megohm isolation, and output current limiting protection.

GENERAL SPECIFICATIONS— ALL MODELS

Output Voltage Accuracy	±1%
Output Noise and Ripple, max.	20mV P-P (2mV RMS)
Back Ripple Current, max.	1% of I_{IN}
Capacitive Coupling, max.	250 pF
Breakdown Voltage, min.	300VDC
Transient Recovery Time, max.	50μsec.
Operating Temp. Range	-25°C to +71°C
Storage Temp. Range	-55°C to +85°C
Case Material	Diallyl Phthalate (G2) Phenolic (CB)

MODULE SIZES

G2 Size:	2.0 × 2.0 × .750 inches 50,8 × 50,8 × 19,1 mm
Weight	4.5 oz. (128g.)
CB Size:	3.5 × 2.5 × .875 inches 88,9 × 63,5 × 22,2 mm
Weight	14 oz. (397g.)

The 5 watt series use 2 DILS-1 or DILS-2 terminal strips
The 10 watt series use the MS-7 socket

THESE DC-DC CONVERTERS ARE COVERED BY GSA CONTRACT

48 Volt Input DC-DC Converters

1 WATT SERIES

MODEL	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	INPUT VOLT. TOLERANCE	NO LOAD INPUT CURRENT	FULL LOAD INPUT CURRENT	EFFICIENCY (FULL LOAD)	LINE REGULATION
UPM-5/200-D48	+ 5V	200mA	48VDC	±12.5%	10mA	42mA	50%	.05%
UPM-12/80-D48	+12V	80mA	48VDC	±12.5%	10mA	42mA	50%	.05%
UPM-15/60-D48	+15V	60mA	48VDC	±12.5%	10mA	42mA	50%	.05%
BPM-12/40-D48	±12V	40mA	48VDC	±12.5%	10mA	42mA	50%	.05%
BPM-15/30-D48	±15V	30mA	48VDC	±12.5%	10mA	42mA	50%	.05%

3 WATT SERIES

MODEL	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	INPUT VOLT. TOLERANCE	NO LOAD INPUT CURRENT	FULL LOAD INPUT CURRENT	EFFICIENCY (FULL LOAD)	LINE REGULATION
UPM-5/600-D48	+ 5V	600mA	48VDC	±12.5%	45mA	125mA	50%	.05%
UPM-12/250-D48	+12V	250mA	48VDC	±12.5%	45mA	125mA	50%	.05%
UPM-15/200-D48	+15V	200mA	48VDC	±12.5%	45mA	125mA	50%	.05%
BPM-12/125-D48	±12V	125mA	48VDC	±12.5%	45mA	125mA	50%	.05%
BPM-15/100-D48	±15V	100mA	48VDC	±12.5%	45mA	125mA	50%	.05%

5 WATT SERIES

MODEL	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	INPUT VOLT. TOLERANCE	NO LOAD INPUT CURRENT	FULL LOAD INPUT CURRENT	EFFICIENCY (FULL LOAD)	LINE REGULATION
UPM-5/1000-D48	+ 5V	1000mA	48VDC	±12.5%	60mA	208mA	50%	.05%
UPM-12/420-D48	+12V	420mA	48VDC	±12.5%	60mA	208mA	50%	.05%
UPM-15/330-D48	+15V	330mA	48VDC	±12.5%	60mA	208mA	50%	.05%
BPM-12/210-D48	±12V	210mA	48VDC	±12.5%	60mA	208mA	50%	.05%
BPM-15/165-D48	±15V	165mA	48VDC	±12.5%	60mA	208mA	50%	.05%

10 WATT SERIES

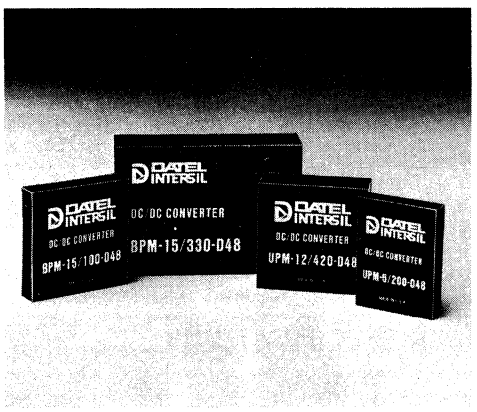
MODEL	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	INPUT VOLT. TOLERANCE	NO LOAD INPUT CURRENT	FULL LOAD INPUT CURRENT	EFFICIENCY (FULL LOAD)	LINE REGULATION
UPM-5/2000-D48	+ 5V	2000mA	48VDC	±12.5%	120mA	415mA	50%	.05%
UPM-12/840-D48	+12V	840mA	48VDC	±12.5%	120mA	415mA	50%	.05%
UPM-15/660-D48	+15V	660mA	48VDC	±12.5%	120mA	415mA	50%	.05%
BPM-12/420-D48	±12V	420mA	48VDC	±12.5%	120mA	415mA	50%	.05%
BPM-15/330-D48	±15V	330mA	48VDC	±12.5%	120mA	415mA	50%	.05%

LOAD REGULATION	TEMP. COEFFICIENT	OUTPUT IMPEDANCE	CASE CONFIG.	PRICE (1-9)
0.1%	.02%/° C	.07Ω	F	**$44.00**
0.1%	.02%/° C	.2 Ω	F	**$44.00**
0.1%	.02%/° C	.2 Ω	F	**$44.00**
0.1%	.02%/° C	.2 Ω	F	**$51.50**
0.1%	.02%/° C	.2 Ω	F	**$51.50**

LOAD REGULATION	TEMP. COEFFICIENT	OUTPUT IMPEDANCE	CASE CONFIG.	PRICE (1-9)
.01%	.02%/° C	.07Ω	G1	**$67.00**
.05%	.02%/° C	0.2Ω	G1	**$67.00**
.05%	.02%/° C	0.2Ω	G1	**$67.00**
.05%	.02%/° C	0.2Ω	G1	**$72.50**
.05%	.02%/° C	0.2Ω	G1	**$72.50**

LOAD REGULATION	TEMP. COEFFICIENT	OUTPUT IMPEDANCE	CASE CONFIG.	PRICE (1-9)
0.1%	.02%/° C	.005Ω	G2	**$72.50**
.05%	.02%/° C	.03 Ω	G2	**$72.50**
.05%	.02%/° C	.03 Ω	G2	**$72.50**
.05%	.02%/° C	.03 Ω	G2	**$78.00**
.05%	.02%/° C	.03 Ω	G2	**$78.00**

LOAD REGULATION	TEMP. COEFFICIENT	OUTPUT IMPEDANCE	CASE CONFIG.	PRICE (1-9)
.1%	.02%/° C	.005Ω	CB	**$93.50**
.05%	.02%/° C	.02 Ω	CB	**$93.50**
.05%	.02%/° C	.02 Ω	CB	**$93.50**
.05%	.02%/° C	.02 Ω	CB	**$98.50**
.05%	.02%/° C	.02 Ω	CB	**$98.50**



DESCRIPTION

This new series of 48 volt input DC-DC converters features 20 different models with both single and dual outputs. There are 12 single output models offering 5, 12 and 15 volts. There are 8 dual output models offering ±12 or ±15 volts. Output voltage accuracies are ±1% with .02%/° C temperature coefficients. Other features include low output ripple, 100 megohm isolation and output current limiting protection.

GENERAL SPECIFICATIONS
ALL MODELS

Output Voltage Accuracy	±1%
Output Noise and Ripple, max.	20mV P-P (2mV RMS)
Back Ripple Current, max.	1% of Iin
Capacitive Coupling, max.	250 pF
Breakdown Voltage, min.	300VDC
Transient Recovery Time, max.	50μsec.
Operating Temp. Range	−25° C to +71° C
Storage Temp. Range	−55° C to +85° C

MODULE SIZES

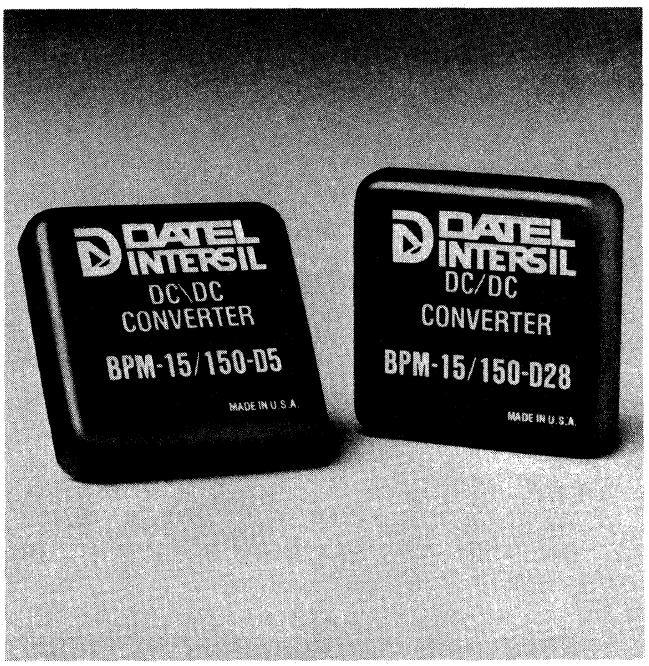
F Case:	1.5× 2.0× 0.375 inches 38,1× 50,8× 9,5 mm
Weight:	1.5 oz. (43g.)
G1 Case:	2.0× 2.0× 0.432 inches 50,8× 50,8× 11,0 mm
Weight:	2.5 oz. (71g.)
G2 Size:	2.0× 2.0× .750 inches 50,8× 50,8× 19,1 mm
Weight:	4.5 oz. (128g.)
CB Size:	3.5× 2.5× .875 inches 88,9× 63,5× 22,2 mm
Weight:	14 oz. (397 g.)
Case Material	Diallyl Phthalate (F), (G1), (G2) Phenolic (CB)

Both 1 and 3 watt series use 2 DILS-1 or DILS-2 terminal strips (at $6.00/pair) for sockets. The 5 watt series use 2 DILS-1 or DILS-2 terminal strips at $6.00/pair for sockets. The 10 watt series use the MS-7 socket at $4.00 each.

THESE DC-DC CONVERTERS ARE COVERED BY GSA CONTRACT

4.5 Watt DC-DC Converters

These miniature, aluminum cased DC-DC converters are ideal for applications where mounting space is tight, yet highly regulated ±15VDC is required at up to 150mA output current. Specifications include voltage accuracy of ±1%, line regulation of .05% max., load regulation of .05% max., and tempco of .005%/°C. For convenient heat sinking, two 2-56 studs are provided on the bottom of the case. All models have output current limiting protection.



OTHER SPECIFICATIONS

Isolation Resistance, min.	100 Meg.
Isolation Capacitance, max.	100 pF
Breakdown Voltage, min.	300VDC
Operating Temp. Range	-25°C to +71°C
Storage Temp. Range	-55°C to +85°C

MS-6 sockets are $4.00 each

SPECIFICATIONS, 25 °C	BPM-15/150-D5	BPM-15/150-D24	BPM-15/150-D28
Output Voltage	±15VDC	±15VDC	±15VDC
Output Voltage Accuracy	±1%	±1%	±1%
Rated Output Current[1]	±150mA	±150mA	±150mA
Input Voltage	5VDC	24VDC	28VDC
Input Voltage Tolerance	±.25V	±3.5V	±4V
Maximum Input Current	1.75A	0.35A	0.3A
Efficiency, full load	51%	54%	54%
Line Regulation, max.	.05%	.05%	.05%
Load Regulation, max.	.05%	.05%	.05%
Temperature Coefficient, max.	.005%/°C	.005%/°C	.005%/°C
Output Ripple RMS max.	1mV	1mV	1mV
Output Impedance, max.	.05Ω	.05Ω	.05Ω
Transient Recovery Time, max.	50μsec.	50μsec.	50μsec.
Case Material	Aluminum	Aluminum	Aluminum
Module Size, inches	2.0 × 2.0 × 0.4	2.0 × 2.0 × 0.4	2.0 × 2.0 × 0.4
Module Size, millimeters	50,8 × 50,8 × 10,2	50,8 × 50,8 × 10,2	50,8 × 50,8 × 10,2
Module Weight	3.0 oz. (85g.)	3.0 oz. (85g.)	3.0 oz. (85g.)
Case/Pin Configuration	B	B	B
Mating Socket	MS-6	MS-6	MS-6
Price (1-9)	**$83.00**	**$83.00**	**$83.00**

NOTE: 1. Above 35°C (95°F) mounting surface temperature, derate 1.3mA/°C.

THESE POWER SUPPLIES ARE COVERED BY GSA CONTRACT

5 Volt Input DC-DC Isolator Regulators

DESCRIPTION

Datel-Intersil offers a line of 5 Volt DC isolator regulators in 1, 3, 5, and 10 Watt capacities. These isolator-regulators provide a stable, accurate, low-ripple +5 Vdc source from supplies of +4.5 to +5.5 VDC, including 5V sources with poor regulation, ripple or noise characteristics.

Output voltage accuracy is ±1% with 0.02%/°C temperature coefficient. Other features include low output ripple, 100 megohm isolation, and output current limiting.

All models in this series are compact encapsulated modules designed to occupy a minimum of space on a printed circuit board.

GENERAL SPECIFICATIONS — ALL MODELS

Input Voltage Tolerance	±10%
Output Voltage Accuracy	±1%
Regulation	
Line	.05%
Load	0.1%
Temperature Coefficient, max.	.02%/°C
Output Noise and Ripple, max.	20mV P-P (2mV RMS)
Back Ripple Current, max.	1% of I_{IN}
Capacitive Coupling, max.	250 pF
Breakdown Voltage, min.	300VDC
Transient Recovery Time, max.	50μsec.
Operating Temp. Range	−25°C to +71°C
Storage Temp. Range	−55°C to +85°C

MODULE SIZES

F Case:	1.5 × 2.0 × 0.375 inches 38,1 × 50,8 × 9,5 mm
Weight:	1.5 oz. (43g.)
G1 Case:	2.0 × 2.0 × 0.432 inches 50,8 × 50,8 × 11,0 mm
Weight:	2.5 oz. (71g.)
G2 Size:	2.0 × 2.0 × .750 inches 50,8 × 50,8 × 19,1 mm
Weight:	4.5 oz. (128g.)
CB Size:	3.5 × 2.5 × .875 inches 88,9 × 63,5 × 22,2 mm
Weight:	14 oz. (397g.)
Case Material:	Diallyl Phthalate (F) (G1), (G2) Phenolic (CB)

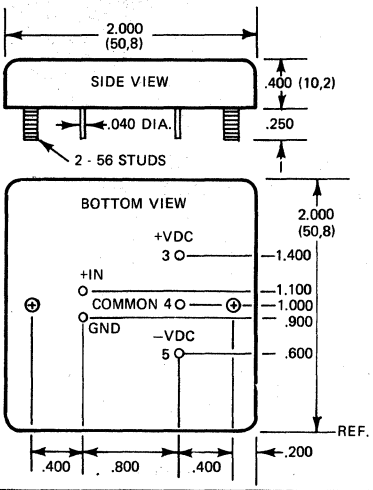
Both 1 and 3 watt series uses 2 DILS-1 or DILS-2 terminal strips (at $6.00/pair) for sockets. The 5 watt series uses 2 DILS-1 or DILS-2 terminal strips at $6.00/pair for sockets. The 10 watt series uses the MS-7 socket at $4.00 each.

MODEL	OUTPUT VOLTAGE	OUTPUT CURRENT	NO LOAD INPUT CURRENT	FULL LOAD INPUT CURRENT	EFFICIENCY (FULL LOAD)	OUTPUT IMPEDANCE	CASE CONFIG.	PRICE (1-9)
1 WATT SERIES								
UPM-5-200-D5	+5V	200mA	95mA	370mA	50%	.07Ω	F	**$44.00**
3 WATT SERIES								
UPM-5/500-D5	+5V	500mA	300mA	125mA	40%	.07Ω	G1	**$67.00**
5 WATT SERIES								
UPM-5/1000-D5	+5V	1000mA	500mA	2000mA	50%	.015Ω	G2	**$72.50**
10 WATT SERIES								
UPM-5/2000-D5	+5V	2000mA	1000mA	4000mA	50%	.005Ω	CB	**$93.50**

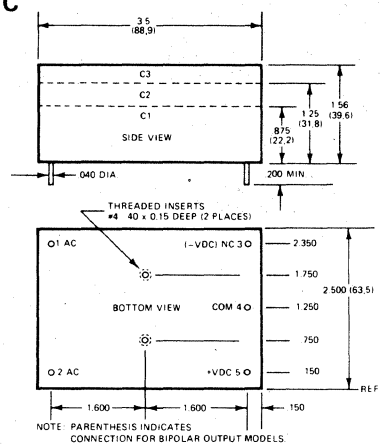
THESE DC-DC CONVERTERS ARE COVERED BY GSA CONTRACT

Case/Pin Configurations and Sockets

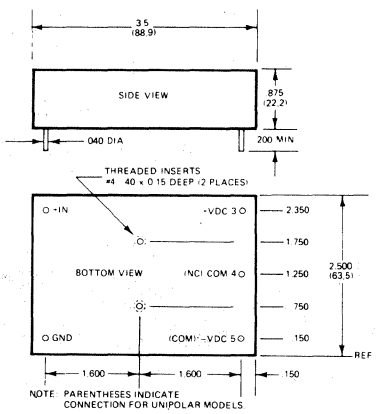
CASE B



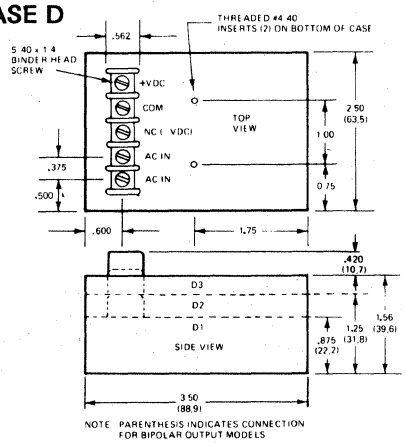
CASE C



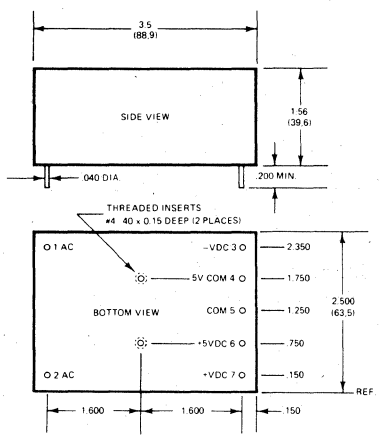
CASE CB



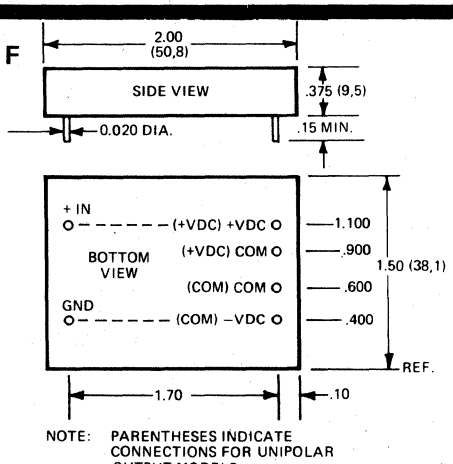
CASE D



CASE E3

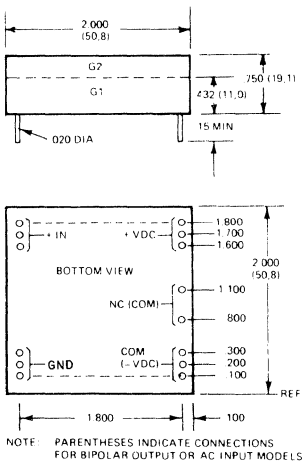


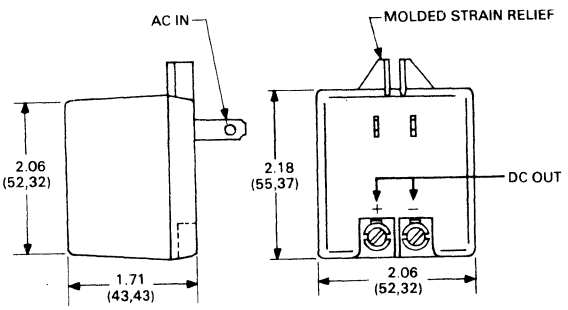
CASE F



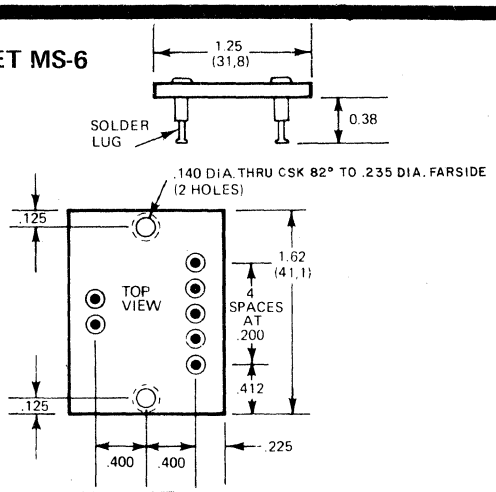
NOTE: PARENTHESES INDICATE CONNECTIONS FOR UNIPOLAR OUTPUT MODELS.

CASE G

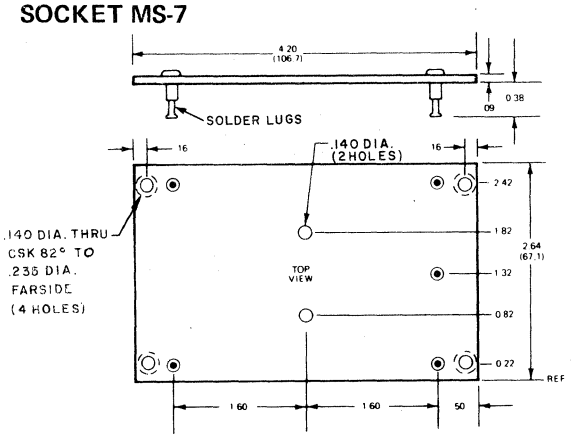




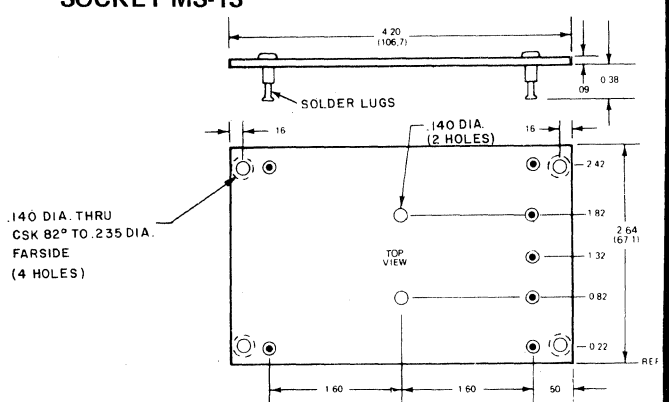
SOCKET MS-6



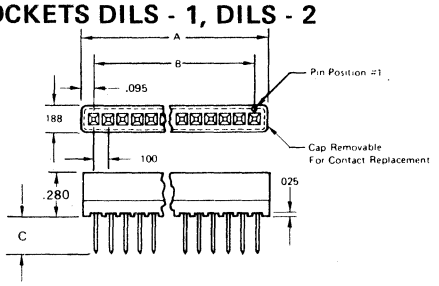
SOCKET MS-7



SOCKET MS-13

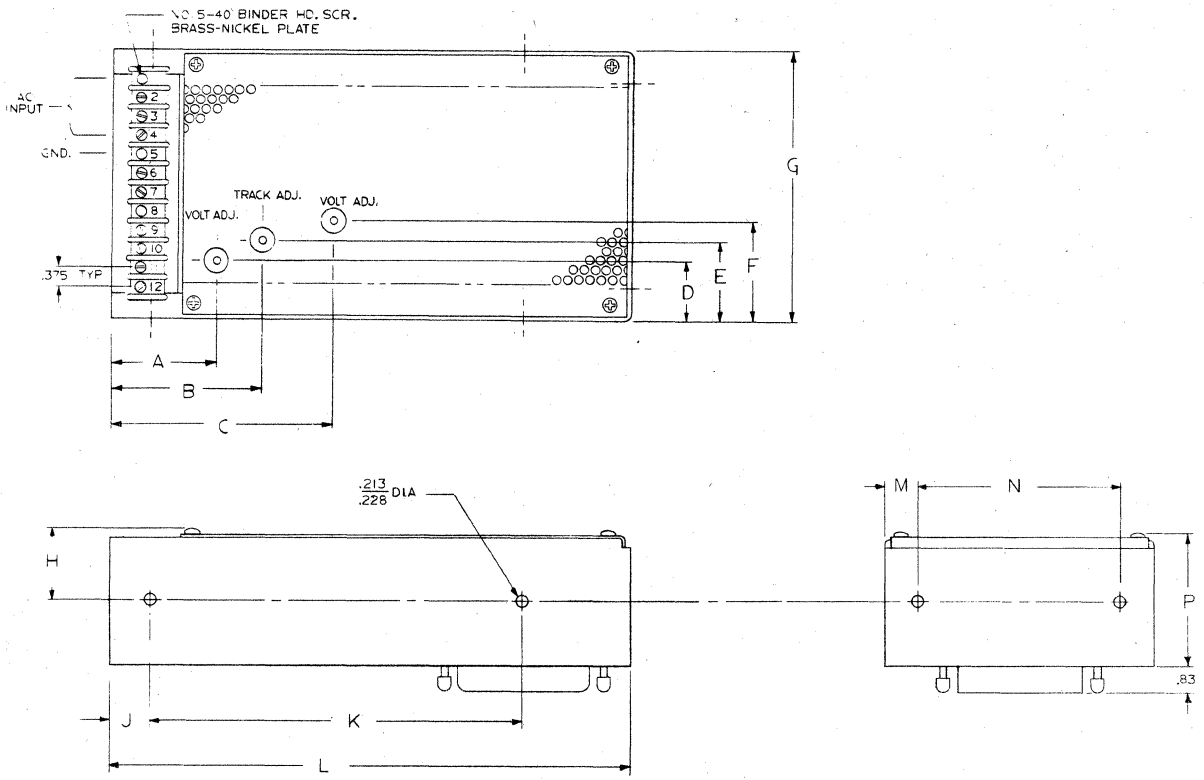


SOCKETS DILS - 1, DILS - 2



Model	No. of Contacts	A	B	C
DILS-1	20	2.090	1.900	.645
DILS-2	20	2.090	1.900	.145

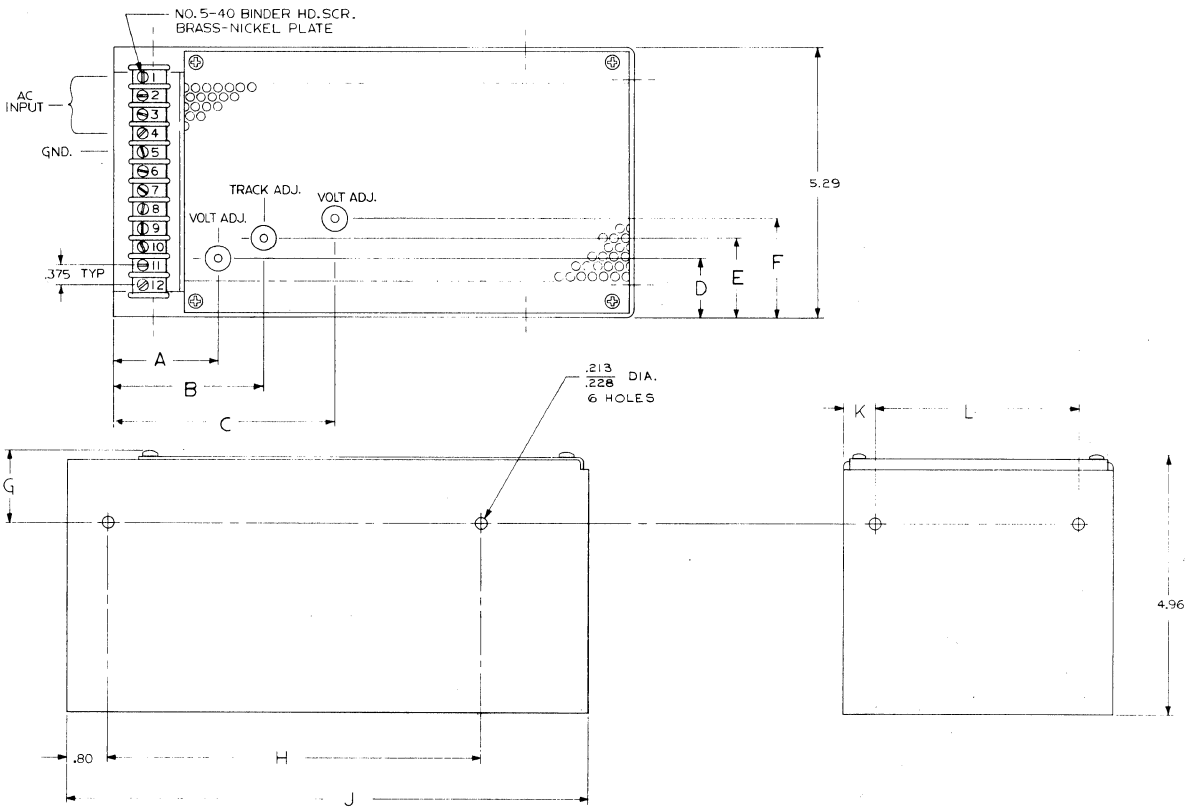
MP Series Supplies



MODEL	MECHANICAL DIMENSIONS													
	A	B	C	D	E	F	G	H	J	K	L	M	N	P
MPS-5/3	1.72	——	——	.57	——	——	4.60	.80	.55	5.80	7.62	.59	3.40	2.20
MPD-12/1	2.03	2.68	——	2.16	2.16	——	4.84	1.34	.80	7.00	10.00	.66	3.50	2.67
MPD-15/1	2.03	2.68	——	2.16	2.16	——	4.84	↑	↑	7.00	10.00	.66	3.50	2.67
MPD-12/1.5	2.00	2.50	——	2.60	2.60	——	5.29	↕	↕	7.30	10.28	.63	4.00	3.84
MPD-15/1.5	2.00	2.50	——	2.60	2.60	——	5.29	↕	↕	7.30	10.28	.63	4.00	3.84
MPT-12/1-5/3	2.36	3.18	2.53	.66	2.50	2.50	4.84	↓	↓	7.95	10.97	.78	3.25	3.56
MPT-15/1-5/3	2.36	3.18	2.53	.66	2.50	2.50	4.84	1.34	.80	7.95	10.97	.78	3.25	3.56

FOR 115 VAC INPUT, JUMPER PINS 1 & 2 AND 3 & 4. INPUT IS TO PINS 1 AND 4.
FOR 230 VAC INPUT, JUMPER PINS 2 & 3. INPUT IS TO PINS 1 AND 4.

MODEL	NO. OF TERM.	TERMINAL DESIGNATIONS						
		6	7	8	9	10	11	12
MPS-5/6	9	+OUT	+SENS	-SENS	-OUT	-	-	-
MPS-5/12	11	+OUT	+OUT	+SENS	-SENS	-OUT	-OUT	-
MPS-5/18	11	+OUT	+OUT	+SENS	-SENS	-OUT	-OUT	-
MPD-12/3	12	+12V	SENS HI	SENS LO	COM	SENS LO	SENS HI	-12V
MPD-15/3	12	+15V	SENS HI	SENS LO	COM	SENS LO	SENS HI	-15V
MPT-12/1.5-5/6	12	+5V OUT	+SENS	-SENS	+5V RET	+12V	COM	-12V
MPT-15/1.5-5/6	12	↑	↑	↑	↑	+15V	↑	-15
MPT-12/1.5-5/12	12	↓	↓	↓	↓	+12V	↓	-12
MPT-15/1.5-5/12	12	+5V OUT	+SENS	-SENS	+5V RET	+15V	COM	-15

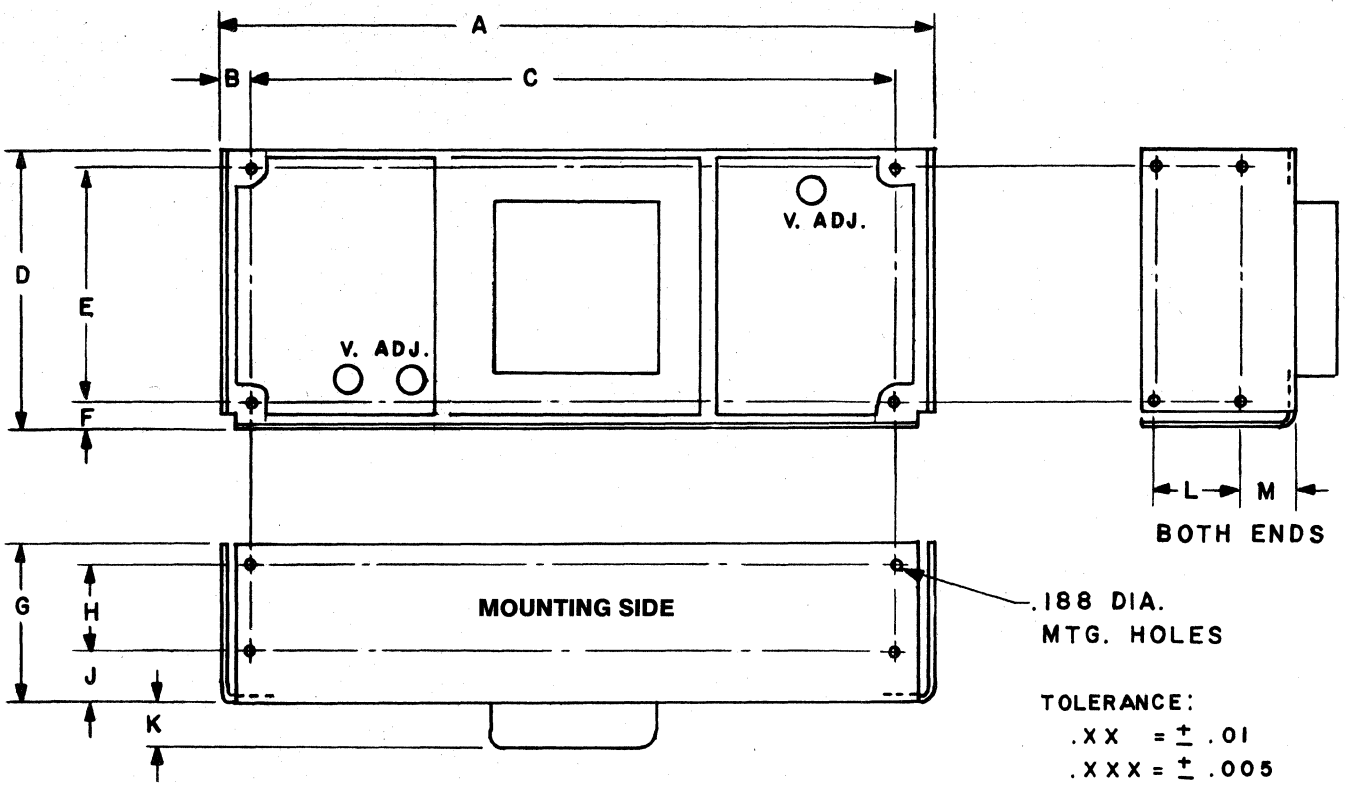


MODEL	MECHANICAL DIMENSIONS										
	A	B	C	D	E	F	G	H	J	K	L
MPS-5/6	3.10	——	——	1.08	——	——	1.59	6.00	10.28	.63	4.00
MPS-5/12	2.70	——	——	1.33	——	——	↑	7.50	11.91	↑	↑
MPS-5/18	2.70	——	——	1.33	——	——	↓	7.50	11.91	↓	↓
MPD-12/3	2.00	2.50	——	2.60	2.60	——		6.00	10.28		
MPD-15/3	2.00	2.50	——	2.60	2.60	——	1.59	6.00	10.28	.63	4.00
MPT-12/1.5-5/6	3.17	3.21	11.73	1.10	1.13	4.50	1.85	10.92	13.98	.29	4.50
MPT-15/1.5-5/6	3.17	3.21	11.73	1.10	↑	↑	↑	10.92	13.98	↑	↑
MPT-12/1.5-5/12	2.70	3.06	13.36	1.33	↓	↓	↓	12.59	15.55	↓	↓
MPT-15/1.5-5/12	2.70	3.06	13.36	1.33	1.13	4.50	1.85	12.59	15.55	.29	4.50

MODEL	NO. OF TERM.	TERMINAL DESIGNATIONS						
		6	7	8	9	10	11	12
MPS-5/3	9	+OUT	+SENS	-SENS	-OUT	-	-	-
MPD-12/1	12	+12V	SENS HI	SENS LO	COM	SENS LO	SENS HI	-12V
MPD-15/1	12	+15V	↑	↑	↑	↑	↑	-15V
MPD-12/1.5	12	+12V	↓	↓	↓	↓	↓	-12V
MPD-15/1.5	12	+15V	SENS HI	SENS LO	COM	SENS LO	SENS HI	-15V
MPT-12/1-5/3	12	+5V OUT	+SENS	-SENS	+5V RET	+12V	COM	-12V
MPT-15/1-5/3	12	+5V OUT	+SENS	-SENS	+5V RET	+15V	COM	-15V

FOR 115 VAC INPUT, JUMPER PINS 1 & 2 AND 3 & 4. INPUT IS TO PINS 1 AND 4.
FOR 230 VAC INPUT, JUMPER PINS 2 & 3. INPUT IS TO PINS 1 AND 4.

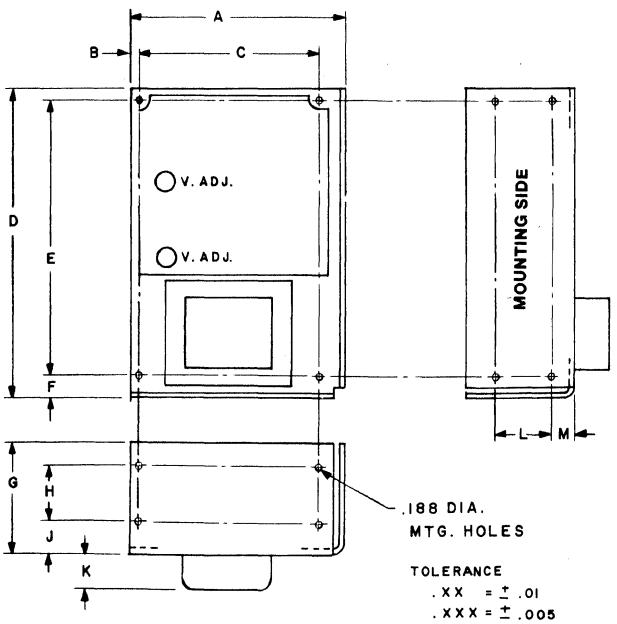
Power Chassis Series:



MODEL	A	B	C	D	E	F
PCS-5/12	9.00	.50	8.00	5.10	4.125	.50
PCS-5/18	14.00	.50	13.00	5.10	4.125	.50
PCD-12/3 PCD-15/3	9.38	.50	8.375	4.87	4.125	.50
PCT-5/3-12/1 PCT-5/3-15/1	10.25	.50	9.250	4.00	3.375	.37
PCT-5/6-12/2 PCT-5/6-15/2	11.25	3.25	7.500	4.87	4.125	.50
PCT-5/12-12/2 PCT-5/12-15/2	14.25	5.00	8.750	5.10	4.125	.50

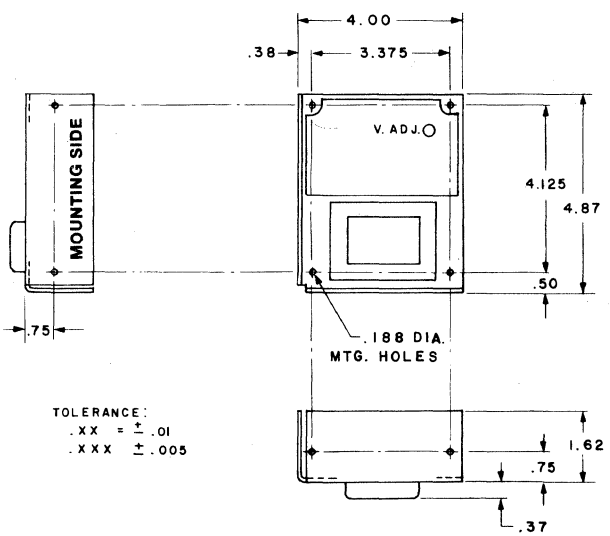
MODEL	G	H	J	K	L	M
PCS-5/12	2.75	1.250	.75	.60	1.250	.75
PCS-5/18	2.75	1.250	.75	.67	1.250	.75
PCD-12/3 PCD-15/3	2.75	1.250	.75	.67	1.250	.75
PCT-5/3-12/1 PCT-5/3-15/1	2.50	1.250	.75	.42	1.250	.75
PCT-5/6-12/2 PCT-5/6-15/2	2.75	1.250	.75	.54	1.250	.75
PCT-5/12-12/2 PCT-5/12-15/2	2.75	1.250	.75	.67	1.250	.75

Power Chassis Series:



MODEL	A	B	C	D	E	F
PCS-5/6	4.87	.25	4.125	5.62	4.875	.50
PCD-12/1 PCD-15/1	4.00	.25	3.375	6.50	5.750	.50
PCD-12/2 PCD-15/2	4.87	.25	4.125	7.00	6.250	.50

MODEL	G	H	J	K	L	M
PCS-5/6	2.50	1.250	.75	.37	1.25	.75
PCD-12/1 PCD-15/1	1.62	—	.75	.80	—	.75
PCD-12/2 PCD-15/2	2.50	1.250	.75	.93	1.25	.75



PCS-5/3

END OF
DATA ACQUISITION
COMPONENTS SECTION

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END OF
INSTRUMENTS AND SYSTEMS
SECTION

FOR OUR COMPLETE CATALOG OF
DATA ACQUISITION COMPONENTS
INVERT THIS VOLUME AND
TURN TO PAGE 1C.