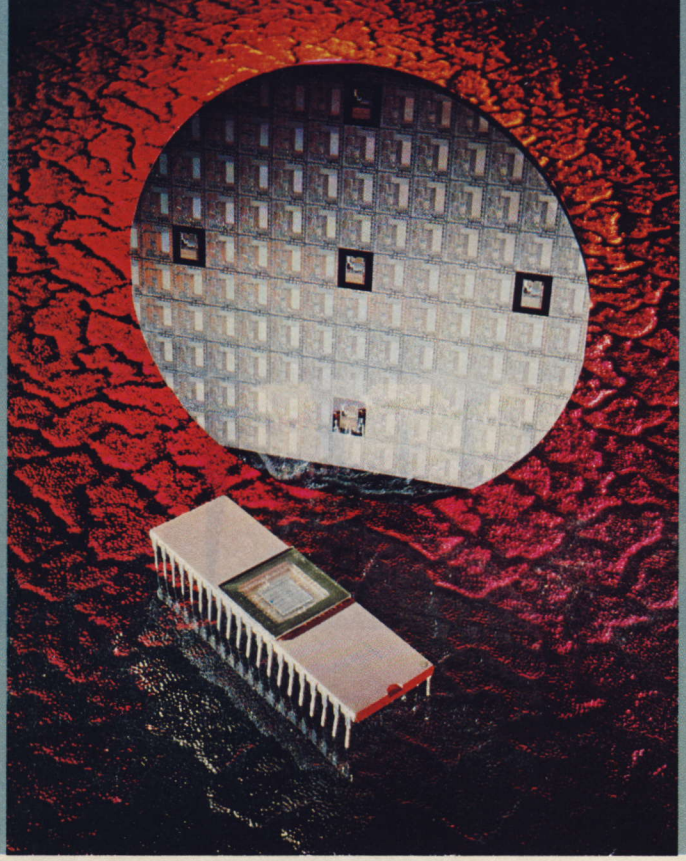
EDN μC DESIGN SERIES

EDN's Fourth Annual Microprocessor Directory



Robert H. Cushman, Special Features Editor

In preparing material for this Microcomputer Systems Reference Issue, EDN has spotted seven significant trends in the semiconductor industry. Since many if not all of these developments could have a significant impact on the way you can successfully perform your design functions, let's examine each in detail.

- **Suppliers of midrange μP's are compressing whole multichip systems into 1- or 2-chip systems for minimum cost low-end applications.** Examples illustrating this trend include the 3870 version of the F8, the 6801 variant of the 6800, the 6600 outgrowth of the 6500, the 9940 version of the 9900, the Z8 version of the Z80, etc. To this list we might also add the 8048, because although it isn't a software-compatible version of the 8080/85 family, it shares much of the same hardware support.
- **Widespread activity is evident from many sources in developing support chips for use with the established μC families.** This trend is particularly true for such midrange families as the 8080 and 6800. EDN predicts the CRT controllers, A/D converters and other peripheral chips will be the most numerous new IC's introduced in 1978.
- **Growing interest exists in serial I/O buses.** The leader in this innovative effort is Texas Instruments. For many years the firm has used its CRU serial bus for its 990 minicomputer family. Finding the serial bus ideally suited to LSI devices with their limited package pinouts, TI has designed a whole series of serial-bus support chips. National Semiconductor has also favored serial buses (notice that the company brings out flags and jump conditions on Pace and provides a serial shift-register port for SC/MP).

EDN notes that most of the one-chip μC's scheduled for introduction in '78 will have similar serial ports. The list includes the 6801, 6600 and

INDEX TO μP'S IN THIS DIRECTORY

The 4/10 has 64K-word addressing and a MAXI-BUS that allows interfacing with the wide variety of interchangeable memories and I/O controllers in the NAKED MINI 4 family.

What about software? It's one of the 4/10's real strengths. Not only a wide range of software, but also software optimized individually for both development and execution needs.

Available software ranges from the simplest—a memory-based system that runs in as few as 4K words—through the most sophisticated, a full-blown, disk operating system that supports FORTRAN IV, BASIC, PASCAL, and MACRO 4 assembler.

In terms of hardware and software, the 4/10 is fully compatible with its higher performance brothers, the 4/30 and 4/90.

Okay, we've served up our new 4/10 mini with lots of standard and optional hors d'oeuvres. Still hungry for information? Contact Department 1161, NAKED MINI Division, 18651 Von Karman, Irvine, CA 92713, (714) 833-8830, for our new brochure. It's quite a bit of food for thought.

SBOARD.

ComputerAutomation®
Naked Mini® Division

For more information, Circle No. 29

NAKED MINI products are sold only under volume purchase agreements.

Low-cost systems for all—that's one key effect of the continuing development of tried-and-true μP families and the explosion of support chips for them. Typifying these trends is Intel's 8748 μC. *(Photo courtesy Intel Corp.)*

Z8. Even some of the support "combo" chips for 2-chip systems will have serial ports. For emphasis, we observe that higher end μC's such as the microNova also use high-performance versions of these serial buses.

• **There seems to be a general industry reluctance to risk bringing out a new μC family.** Most of the innovations found in this year's μC directories are actually embellishments on such established μC families as the 8080, 6800 or F8, or on such established minicomputer families as the PDP-11 or Nova 1200. Perhaps just too many good μC's are available for any semiconductor supplier to hope at this late date to launch any totally new μC family. And it would cost perhaps $50 million to generate a barrage of product and support sufficient to convince designers that they should learn a totally new machine. (This financial fact of life was one of the reasons that Electronic Arrays abandoned its fine 9002 μP, despite having produced working chips.)

• **Several ambitious high-end projects are underway, but they will mostly use existing software.** Fairchild's impressive 9940 μP uses I^2L technology to squeeze a full bipolar-speed Nova 1200 CPU on a 182×189-mil chip. The company is also working on an ECL microprogrammable chip set that will feature such extreme performance features as 20 MHz clock and 20-nsec instruction cycle time. This "super-speed" chip set will be made up of slices of eight bits plus parity and

Coming soon: a low-end 8048

As EDN went to press with this issue, we received word that Intel plans to introduce a low-end addition to its 8048 single-chip μC family. Designated the 8021, the new chip will serve automotive, appliance and instrumentation applications.

Slated for sampling by the end of the year and volume production by April of 1978, the 8021 will come in a 28-pin DIP and incorporate 21 I/O lines. Software compatible with the 8048, it will house 1k bytes of ROM and 64 bytes of RAM just like that chip.

The 8021 will have a 10-μsec instruction time. For noncritical applications, a single resistor can replace the crystal for frequency generation. Power requirements can span the 4.5-6.5V range.

Additional features will include zero crossing detection for ac control and time generation, plus two high-current output pins capable of driving 7 mA in audio alarm applications.

Intel sees the device competing with such 4-bit controllers as the Texas Instruments TMS1000 Series and plans to sell it for about $3 in large OEM quantities.

Among the missing...

Five microprocessors that appeared in last year's EDN μP Directory do not appear in this year's listing. Moreover, two other units have been intentionally omitted.

SX200—Essex International admits that this μP was not a success on the open market, so the company is not actively pushing it.

7150—Developed by ITT in the United Kingdom, this μP has been supported by only one marketing person in the USA. EDN was advised not to list the 7150 because the firm is going to do "something better." (The "something better" could include second-sourcing popular devices from Silicon Valley.)

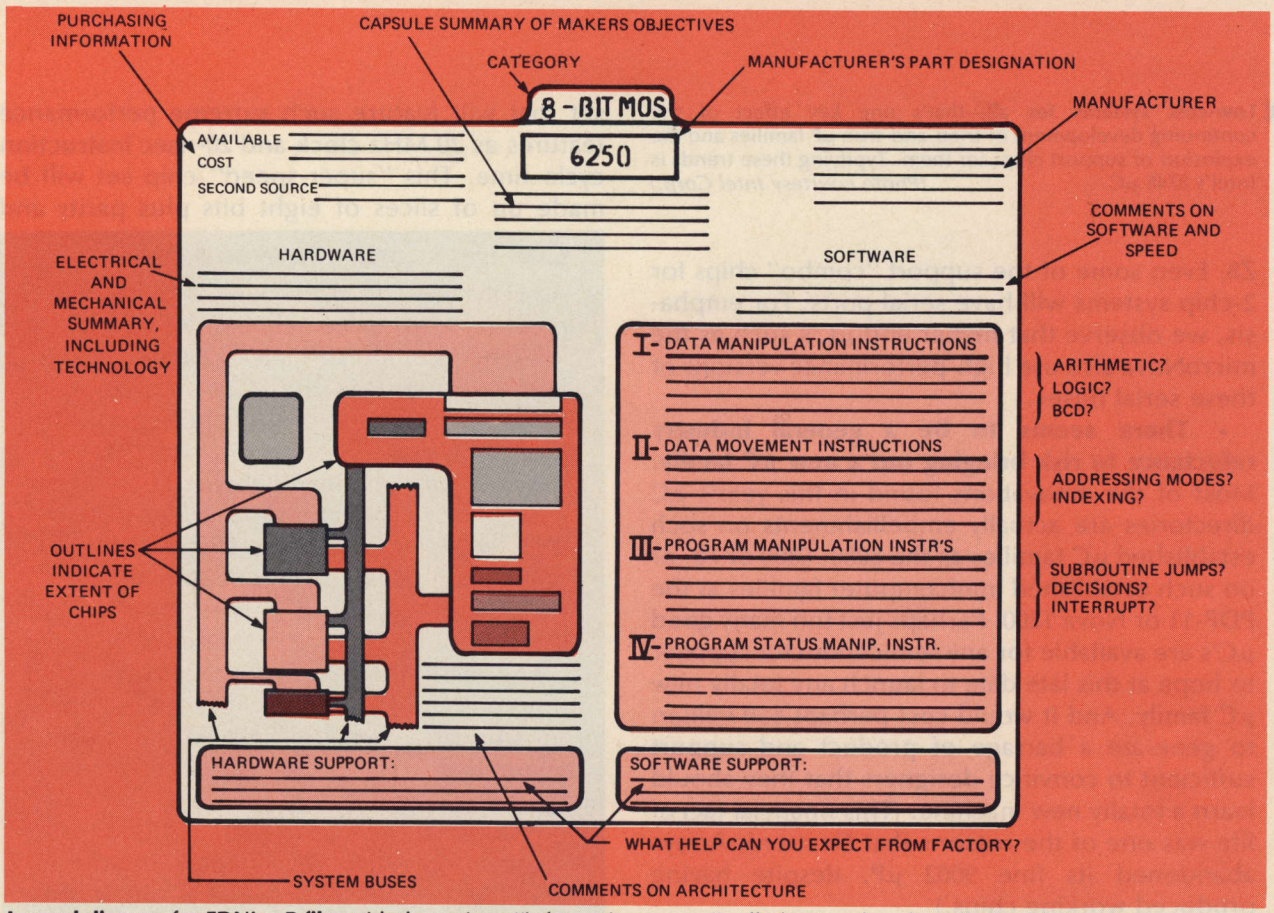
EA9002—The project staff at Electronic Arrays associated with this μP has been disbanded and the marketing effort closed down. The firm entered the market too late and was too small to mount a competitive sales effort.

3859—Fairchild rushed this μP to the market, only to realize that F8 second-source Mostek had upstaged it and done a better design job (in particular, the 3870 has a larger on-chip memory). Our sources confirm that the 3859 has been withdrawn.

8000—Developed in Europe, this μP has been quite successful there. However, it's essentially the predecessor of the F8, and, as such, it couldn't be competitive in the USA market once the more advanced Fairchild machine was introduced. Therefore, General Instrument is no longer actively pushing the 8000, although it's listed in the firm's catalog.

SBA—Termed the "Sequential Boolean Analyzer," this 1-bit device from General Instrument is no more a μP than is a PLA. Rather, it's a device designed to implement Boolean equations. Marketing management at GI agreed with EDN's assessment.

825100—This family of bipolar field-programmable gate arrays and logic arrays actually is more related to μP's than the SBA because it performs many μP-like functions and often is used with μP's. However, although the devices handle part of the μP function, they are not classical digital computers, as are all true μP's.



Legend diagram for EDN's μP files with the various "information spaces" called out and explained. The information is purposely equally divided into a hardware half and a software half to emphasize the "two-sided" nature of these SP/GP/DC-type products. (SP/GP/DC stands for stored program, general-purpose digital computer.)

1-BIT CMOS

AVAILABILITY: Now.
COST: $7.58 in 100 qty.
SECOND SOURCE: None.

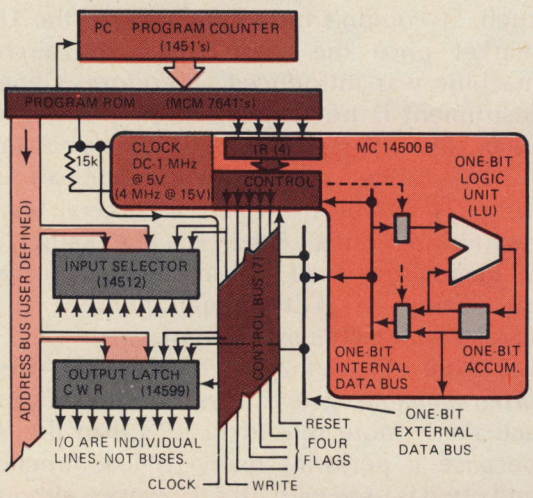
MC 14500

One-bit serial controller is suitable for scanning input lines, making decisions and generating control signals. Unit needs external program counter.

Motorola Semiconductor Products
3501 Ed Bluestein Blvd.
Austin, TX 78721
Phone (512) 928-2600.

HARDWARE

Device specs matched to JEDEC B series CMOS, with full 3-18V power supply range. 16-pin DIP. Quiescent current is 5 μA at 5V. Outputs will drive low-power TTL.



SOFTWARE

Primitive set of 16 instructions; most execute in one clock cycle (1 μsec).

I — DATA MANIPULATION INSTRUCTIONS
Logicals.
Complement.
No arithmetic as such (if desired must be generated from logicals).

II — DATA MOVEMENT INSTRUCTIONS
Load and store.

III — PROGRAM MANIPULATION INSTRUCTIONS
Skip decision (if results = ZERO) is used with jump instructions to perform conditional branches. Can perform subroutines if external LIFO such as 34706 is used.

IV — PROGRAM STATUS MANIPULATION INSTRUCTIONS
Four flags can be set by software.

NOTES: Program is counted out by external counter and will repeat endlessly as pc wraps around. PC addresses program ROM (or RAM) which contains both op code for 14500 and addresses for I/O bit selection. Notice "Harvard" architecture with program separate from data and absence of data memory.

HARDWARE SUPPORT: Only sales demonstration units being contemplated.

SOFTWARE SUPPORT: None claimed to be needed, since simple instructions permit hand assembly of programs.

housed in a new JEDEC standard, 68-pin leadless package (a requirement because the packages dissipate 5W). Needless to say, Fairchild is not developing this super μC on its own; rather, it's working jointly with a sponsor identified only as a major computer manufacturer. Because the set will be microprogrammable, it will be able to emulate existing software.

EDN observes that Intel and Zilog have been widely rumored to be developing advanced machines that will execute higher level languages like PL/M and PASCAL directly. The word is that they will do so by using stack architectures like that of the Hewlett-Packard HP 3000. Again, the goal is not to launch a new instruction set.

• **Most of the innovation in μP's these days is found at the very, very low end.** Only down at the extreme low end does EDN's directory reveal any significant willingness on the part of IC makers to innovate with new architectures. Motorola's little CMOS 14500 "controller," Rockwell's MPC (listed in our Support Chip Directory) and GI's continued development of its PIC 1650 are examples of such innovation. Other very low-end innovative μP's include TI's TMS1000, National's MM 5799 Cop family and WD's 1872.

EDN sees three reasons why the semiconductor houses are willing to risk innovation in these devices. First, the software for such μP's is simpler (for example, the Motorola 14500 has only

For more information

Our "file card" format dictates that the information on each μP be considerably condensed. To obtain additional details on specific processors (or on support chips covered in our μC Support Directory), or to obtain data on μP's manufactured overseas, contact these manufacturers directly. We thank them for providing information vital to the preparation of our μP Directory and μC Support Chip Directory.

Advanced Micro Devices
901 Thompson Pl.
Sunnyvale, CA 94086
(408) 732-2400
AM2900 μP
Support Chips
8048/8748, 8041/8741, 8035 μC
8080A μP
8085 μP*

AEG Telefunken
6 Frankfurt 70
AEG Hochhaus
Federal Republic of Germany
PPS-4 μP Family
Series 8000 μP
PPS-8 μP Family
Support Chips

Analog Devices
Box 280
Norwood, MA 02062
(617) 329-4700
Support Chips

American Microsystems, Inc.
3800 Homestead Rd.
Santa Clara, CA 95051
(408) 246-0300
S2000 μC
6800 μP*
TMS9900/9980/9940 μP*
SBP9900 μP*
Support Chips

Burr-Brown
Box 11400
Tucson, AZ 85734
(602) 294-1431
Support Chips

Data General Corp.
Microcomputer Div.
Westboro, MA 01581
(617) 366-8911
microNova μP
Support Chips

EMM Semi
3883 N. 28th Ave.
Phoenix, AZ 85017
(602) 263-0202
CP-1600/1610 μP*
PIC 1650/1655/1670 μC
Support Chips

Fairchild Semiconductor
464 Ellis St.
Mt. View, CA 94040
(415) 962-3541
6800 μP*
Macrologic μP
9440 μP
AM2900 μP
Support Chips

Fairchild Micro Systems
1725 Technology Dr.
San Jose, CA 95110
(408) 998-0123
F8 μP
3870 μC*
Support Chips

Ferranti Electric
E. Bethpage Rd.
Plainview, NY 11803
(516) 293-8383
F100-L μP
Support Chips

Fujitsu Ltd.
6-1 Marunochi 2 Chome
Chiyoda-ku
Tokyo, Japan
MB8861 μP
Support Chips

General Instrument Corp.
Microelectronics Div.
600 W. John St.
Hicksville, NY 11802
(516) 733-3000
PIC 1650/1655/1670 μC
CP-1600/1610 μP
Support Chips

Harris Semiconductor
Box 883
Melbourne, FL 32901
(305) 727-5407
IM6100 μP*
Support Chips

Hitachi, Ltd.
6-2, 2-Chome
Ohtemachi, Chiyoda-ku
Tokyo 100, Japan
6800 μP*
8080A μP
Support Chips

Hughes Microelectronics
500 Superior Ave.
Newport Beach, CA 92663
(714) 548-0671
CDP1802 μP*
Support Chips

Intel Corp.
3065 Bowers Ave.
Santa Clara, CA 95051
(408) 987-8080
4040/4004 μP
8048/8748, 8041/8741, 8035,8021 μC
8080A/8085 μP
3000 μP
Support Chips

Intersil, Inc.
10900 N. Tantau Ave.
Cupertino, CA 95014
(408) 996-5000
IM6100 μP
Support Chips

ITT Semiconductors
74 Commerce Way
Woburn, MA 01801
(617) 935-7910
5701/6701 μP*
Support Chips

Micro Networks Corp.
324 Clark St.
Worcester, MA 01606
(617) 852-5400
Support Chips

Monolithic Memories, Inc.
1165 E. Arques Ave.
Sunnyvale, CA 94086
(408) 739-3535
5701/6701 μP
AM2900 μP
Support Chips

MOS Technology, Inc.
950 Rittenhouse Rd.
Norristown, PA 19401
(215) 666-7950
650X, 651X μP
MCS-660X μC
Support Chips

Mostek
1215 W. Crosby Rd.
Carrollton, TX 75006
(214) 242-0444
F8 (3850) μP*
3870,3870/2 μC
Z80/Z8/Z8000 μP*
Support Chips

Motorola Semiconductor
5005 E. McDowell Rd.
Phoenix, AZ 85008
(602) 244-6900
F8 μP*
6800 μP
10800 μP
3870 μC*
AM2900 μP*
Support Chips

Motorola Integrated Ckts. Div.
3510 Ed Bluestein Blvd.
Austin, TX 78721
(512) 928-2600
6801 μC
MC14500 μP

*Licensed

Listing continues on pg. 49

4-BIT MOS

AVAILABILITY: Now

COST: $5.50 for 4040, $5.00 for 4004 (100 qty in plastic).

SECOND SOURCE: National Semiconductor for 4001, 4002, 4004, 4008 and 4009

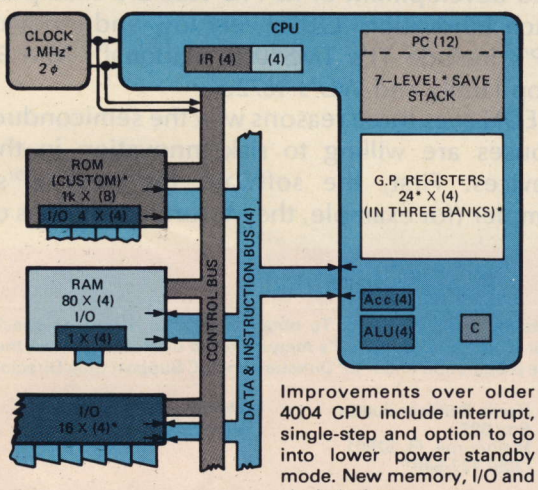
4040/4004

4040 is upwards compatible version of widely used 4004, which will still be available. 4040 includes features lacking in 4004 (marked with asterisk).

Intel Corp.
3065 Bowers Ave.
Santa Clara, CA 95051
Phone (408) 987-8080

HARDWARE

PMOS LSI family of custom parts powered from single −15V supply with CPU in 24-pin pkg.*



Improvements over older 4004 CPU include interrupt, single-step and option to go into lower power standby mode. New memory, I/O and clock devices.

SOFTWARE

59 instructions* include all the older 4004 set and are executed in 8 μsec vs. 10.8 μsec cycle time.

I—DATA MANIPULATION INSTRUCTIONS
Arithmetic and shift.
BCD arithmetic via BCD correction.
Logicals.*
Compare.*

II—DATA MOVEMENT INSTRUCTIONS
Uses GP registers on CPU as pointers to reach memory, taking several steps.
Can reach GP registers directly.
Also has immediate and indirect mode.
I/O on memory chips & shares addresses.

III—PROGRAM MANIPULATION INSTR'S
Two decision instructions, conditional branch and skip-on-zero.
Seven levels of subroutine nesting.*
Software interrupt disable.*
Interrupt with automatic saving and vectoring.*

IV—PROGRAM STATUS MANIP. INSTR.
Can test status via the conditional branch instruction.

HARDWARE SUPPORT: Designer's kit and Intellect 4/Mod 4 development system that has resident monitor and peripheral interfaces.

SOFTWARE SUPPORT: "MAC40" cross-assembler and "Interp/40" 4004/4040 cross-simulator are available on timeshare and for minis. Program library has over 50 programs. No higher-level language planned.

4-BIT MOS

AVAILABILITY: Now.

COST: Under $5 in 25k qty, under $3 at 100k.

SECOND SOURCE: Under negotiation.

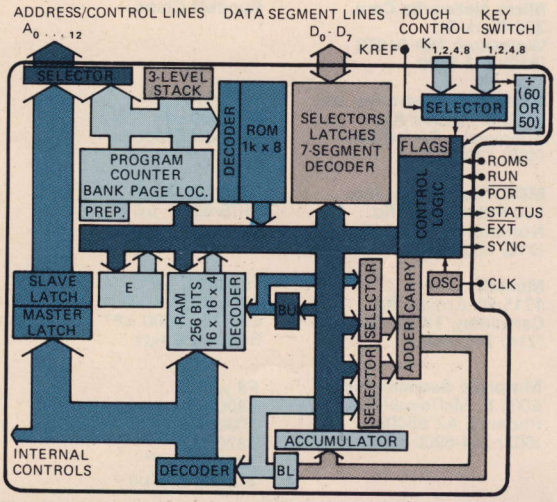
S2000

Aimed primarily at appliance, game and timing/control applications, this 1-chip μC interfaces directly to standard or capacitive keyboards, drives displays directly and provides motor control (phase control or triac drive).

American Microsystems, Inc.
3800 Homestead Rd.
Santa Clara, CA 95051
Phone (408) 246-0300.

HARDWARE

NMOS, 40-pin DIP, 9V, 234 mW. Has on-chip 7-segment decoder, LED or vacuum-fluorescent drivers, timer that accepts 50/60 Hz for sync to line-frequency controls, and power-on reset circuit. MIL-temp version being developed.



SOFTWARE

51 single-byte instructions; 4 μsec cycle time. On-chip 1k x 8 mask-programmable ROM, with external expansion capability to 8k. Escapes and dual-use options give designer feel of using more general architecture than calculator.

I — DATA MANIPULATION INSTRUCTIONS
Arithmetic and logicals. BCD and complement. Many instructions have combined SKIP-IF options.

II — DATA MOVEMENT INSTRUCTIONS
Implied, immediate and direct addressing. Page-oriented indexing. Architecture uses many small pointers for internal memory and I/O port addressing and provides software access to these pointers. Instructions that reconfigure I/O offer unusual versatility in chip applications.

III — PROGRAM MANIPULATION INSTRUCTIONS
Three-level subroutine nesting. Conditional branches and skips.

IV — PROGRAM STATUS MANIPULATION INSTRUCTIONS
Test flags (2) and timer flip-flop status.

HARDWARE SUPPORT: MDC (disk-based CRT terminal with editing, macro and trace capability); software simulator; hardware emulator with PROM sockets; logic analyzer; tester.

SOFTWARE SUPPORT: Assembler; text editor; real-time debugger; software simulator; floppy disc operating system; self-diagnostics; macroprogram library; applications programs; logic analyzer.

National Semiconductor Corp. 2900 Semiconductor Dr. Santa Clara, CA 95051 (408) 737-5000	AM2900 μP 8060 (SC/MP-II) μP 8900 (Pace) μP IMP-16 μP 4040/4004 μP MM5799 μP 8080A μP 2650/A/A-1 μP* Support Chips
NEC Microcomputers, Inc. 5 Militia Dr. Lexington, MA 02173 (617) 862-6413	8080A μP 8085 μP AM2900 μP Support Chips
Panasonic 50 Meadowland Pkwy. Secaucus, NJ 07094 (201) 348-7276	MN 1400 μC Support Chips
Panfacom Ltd. 2-10-16 Jiyuzaoka Mezuro-ku Toyko, Japan	MN 1610 μP Support Chips
Raytheon Semiconductor Div. 350 Ellis St. Mt. View, CA 94042 (415) 968-9211	AM2900 μP* Support Chips
RCA Solid State Div. Route 202 Somerville, NJ 08876 (201) 685-6462	CDP1802 μP Support Chips
Rockwell International 3310 Miraloma Ave. Anaheim, CA 92803 (714) 632-3729	PPS-4/1 μP Family PPS-4, PPS-4/2 μC PPS-8, PPS-8/2 μP 650X, 651X μP* 6500/1 μC Support Chips
Scientific Micro Systems 520 Clyde Ave. Mt. View, CA 94043 (415) 964-5700	Microcontroller Support Chips
Sescosem/Thomson CSF 101 Blvd. Murat 75781 Paris Cedex 16, France	6800 μP* AM2900 μP* Support Chips
SGS-ATES Via C Olivetti 1/20041 Agrate Brianza, Italy	Senes 8000 μP 3850 μP Support Chips
Sharp 22-22 Nagaike-Cho Abeno-ku Osaka 545, Japan	Z80 μP Support Chips
Siemens AG Oskar Von Miller Ring 18 D-8000 Munchen 2 Federal Republic of Germany	8080A μP* 8085 μP* Support Chips
Signetics 811 E. Arques Ave. Sunnyvale, CA 94086 (408) 739-7700	Support Chips AM2900 μP 2650/A/A-1 μP 8X300 μP 8048/8748, 8041/8741, 8035 μC 8080A μP 8060 (SC/MP-II) μP* Macrologic μP 3000 μP
Solid State Scientific, Inc. Montgomeryville, PA 18936 (215) 855-8400	CDP1802 μP* Support Chips
Standard Microsystems Corp. 35 Marcus Blvd. Hauppauge, NY 11787 (516) 273-3100	Support Chips
Synertek Corp. 3050 Coronado Dr. Santa Clara, CA 95051 (408) 984-8900	650X, 651X μP* Support Chips
Texas Instruments, Inc. Microcomputer Products Houston, TX 77001 (713) 494-5115	TMS1000/1200 μP TMS9900/9980/9940 μP SBP9900 μP SBP0400A μP 74S481 μP 8080A μP Support Chips
Toshiba 1 Komukai Toshiba-cho Kawasaki-shi Kanaganaken, Japan	T3472 μC T3190 μP Support Chips
Western Digital Corp. 3128 Red Hill Ave. Newport Beach, CA 92663 (714) 557-3550	1872 μP MCP-1600 μP Support Chips
Zilog 10460 Bubb Rd. Cupertino, CA 95014 (408) 446-4666	Z80/Z8/Z8000 μP Support Chips

*Licensed

16 instructions), and therefore an innovative new part doesn't demand that the user be willing to invest in many months of self-education.

Second, low-end μP's typically need only short (1k bytes or less) application programs. Designers can hand code such short programs if necessary, further cutting down on the support needed.

Which μC's are the safest bets?

You can obtain criteria for assessing the "safeness" of a μC family as follows:

- From our μP Directory, determine the number of second sources for a given μP.
- From our μC Systems Directory, gauge the relative popularity of different μP's with board-level systems suppliers.
- From our μC Support Chip Directory, determine the scope of support chips for the various μC families.

Each of these criteria has its strong and weak points and must be used with common sense.

Third, low-end μP's are typically used in high-volume end applications (because they can sell for just a few dollars in volume). Therefore designers can afford to spend extra time on their hardware and software application. (Actually, in many instances the IC maker's own team performs the application design for the customer, under contract.)

- **Steady progress in CMOS technology could see CMOS μC's finally coming into their own in 1978.** Both Intersil and RCA and their respective second sources say that CMOS EROM's will become available in 1978, not to mention a wider selection of RAM's. EDN's Support Chip Directory points out the growing selection of CMOS auxiliary chips, including A/D converters. Fairchild should share in this CMOS growth with its Macrologic, as should Texas Instruments with its CMOS version of the TMS1000, Motorola with its "nano-P" 14500 and Hewlett-Packard with its advanced MC² (many inside H-P would like to offer MC² as a general product.) □

4-BIT MOS

AVAILABILITY: Now.
COST: $3 to $12 in volume (for COPS family).
SECOND SOURCE: None announced.

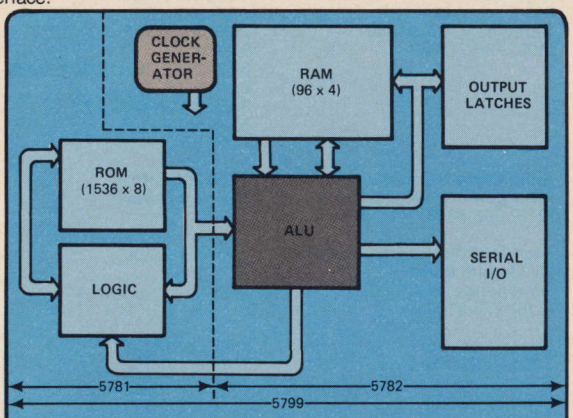
MM5799

MM5799 is middle of line of calculator-oriented processor system (COPS) family of dedicated controllers. Others are 5782 and 57140.

National Semiconductor Corp.
2900 Semiconductor Dr., M/S 470
Santa Clara, CA 95051
Phone(408)737-5000

HARDWARE

PMOS; 9V; 28-pin DIP; 108 mW, typ. Members of family differ mainly in memory size and I/O capability; most provide BCD or 7-segment outputs, have on-chip clocks; all handle direct keyboard interface.



NOTE: The 1-chip 5799 is not expandable. However, a 2-chip version (5781 and 5782) provides double the ROM and more RAM and also allows for further memory expansion. Available support chips interface to printers and displays, etc.

SOFTWARE

41 instructions execute in 10 μsec. Processor works in strings of BCD-coded digits. Programmable, calculator-oriented input/output.

I – DATA MANIPULATION INSTRUCTIONS
Basic binary BCD-coded instructions.
Individual memory bit manipulation.
Performs right and left shifts and floating point via software.
Includes general-purpose I/O instructions in addition to specialized calculator instructions.

II – DATA MOVEMENT INSTRUCTIONS
Versatile output with printer and display interface, including LED and fluorescent. Compatible with 8-bit μP bus for number crunching.

III – PROGRAM MANIPULATION INSTR'S
Two-level nesting.
No hardware interrupt.

IV – PROGRAM STATUS MANIP. INSTR.
Status flag flip-flops set and reset by switch.

HARDWARE SUPPORT: Chips without ROM available for hardware emulation of systems with PROM's or RAM's. IMP-16 development system has ROM-simulation capability.

SOFTWARE SUPPORT: Simulation and assembly programming available on time-sharing networks. Cross-assembler runs on IMP-16P.

4-BIT MOS

AVAILABILITY: Now for most versions.
COST: Approx. $9 in min 1k qty, with $5k mask charge. Total cost/unit is under $3 in high (100k) volume.
SECOND SOURCE: None announced.

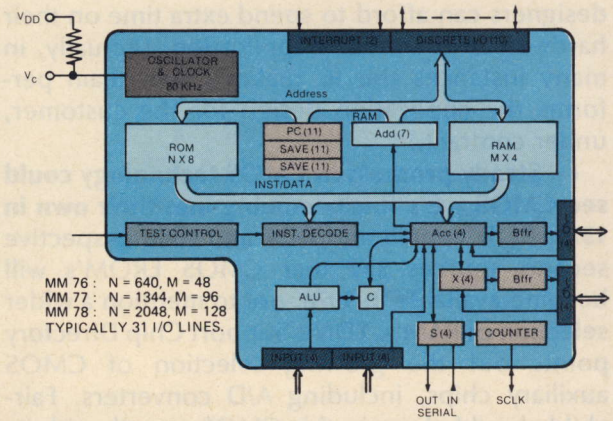
PPS-4/1 FAMILY

One-chip microprocessor family offers wide range of I/O and several sizes of ROM/RAM. Seven standard models aim at low speed, high volume applications.

Rockwell International
3310 Miraloma Ave.
Anaheim, CA 92803
Phone(714)632-3729

HARDWARE

PMOS powered from single – 15V supply (or + 5 and – 10V for TTL compatibility), with 70 mW dissipation. On-chip test for ROM. Low voltage version, MM76L, operates from 6 to 11V.*



SOFTWARE

50 unique instructions, most of which execute in one 12.5-μsec cycle.

I – DATA MANIPULATION INSTRUCTIONS
Arithmetic and logicals.
BCD with decimal correction instr.
Complement.

II – DATA MOVEMENT INSTRUCTIONS
Instructions for moving strings of 4-bit words, so can handle as multiple precision.
Can achieve function of indexing if memory carefully allocated, as several instructions incorporate automatic address modification and tests for loop termination.

III – PROGRAM MANIPULATION INSTR'S
Two-level subroutine nesting.
Table look-up function.
Two conditional interrupt test instructions.

IV – PROGRAM STATUS MANIP. INSTR.
Bit setting and testing directly in RAM memory.

***NOTE:**
Most packages are 42-pin QIL, but MM75 available in 28-pin DIP and MM76C/D in 52-Pin QIL. (76C has counters; 76D incorporates 12-bit A/D.)

HARDWARE SUPPORT: Stand-alone development system, XPO-1, costs $495, contains PPS-4/1's with either utility/debug/monitors or assembler/line editors. Socket brings out ROM address lines Personality board for universal development system.

SOFTWARE SUPPORT: Cross-assembler on time-sharing network. Text editor, assembler and debug utility on universal assemulator. Tutorial manuals. Regular seminars.

4-BIT MOS

AVAILABILITY: Now.
COST: $18.15 for PPS-4 in 100 qty; $5-$10 for PPS-4/2 set in 100 qty.
SECOND SOURCE: None.
(National Semiconductor not active.)

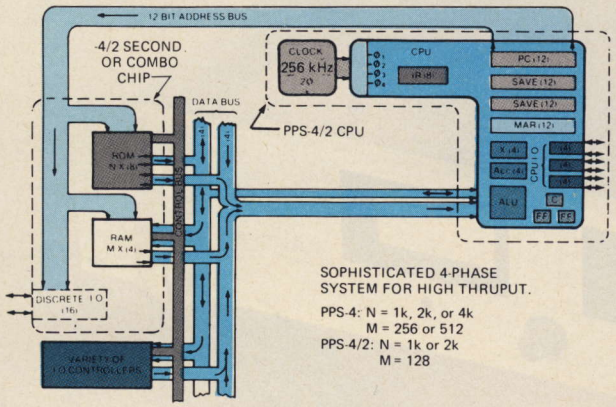
PPS-4, PPS-4/2

Self-sufficient system with expansion capability intended to implement full SP/GP/DC at lowest cost in high volume. Substantial use history. (See PPS-4/1 for single-chip version.)

Rockwell International
3310 Miraloma Ave.
Anaheim, CA 92803
Phone(714)632-3729

HARDWARE

PMOS LSI powered from −17V supply; 42-pin pkg. PPS-4/2 has clock on CPU. PPS-4 has interrupt.



SOFTWARE:

50 unique instructions, most of which execute in one 5-μsec cycle.

I—DATA MANIPULATION INSTRUCTIONS
Arithmetic and logicals.
BCD with decimal correction instr.
Complement.

II—DATA MOVEMENT INSTRUCTIONS
Instructions for moving strings of 4-bit words,so can handle as "calculator-length" BCD-coded decimal numbers.

III—PROGRAM MANIPULATION INSTR'S
Can achieve function of indexing if memory carefully allocated, as several instructions incorporate automatic address modification and tests for loop termination.
Can implement subroutine return address stack in RAM for unlimited nesting. PPS-4 has interrupt.

IV—PROGRAM STATUS MANIP. INSTR.
Carry and two FF's that are software accessible for setting and testing.

HARDWARE SUPPORT: Prototype board. Personality boards for universal assemulator with System Analysis Module (SAM).

SOFTWARE SUPPORT: Cross-assembler on time-sharing network. Text editor, assembler, and debug utility on universal assemulator. Tutorial manuals. Regular seminars.

4-BIT MOS

AVAILABILITY: Now.
COST: As low as $2 in 100k volume.
SECOND SOURCE: None for PMOS chip; Motorola possible for CMOS version.

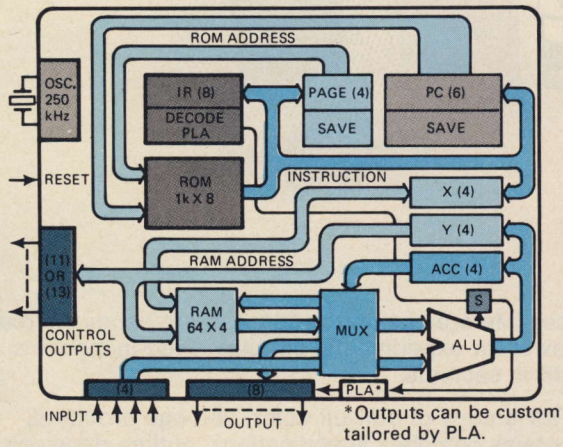
TMS—1000/1200 (1100/1300)

Very successful calculator based-family of μC's comes in versions with up to 2k x 8 ROM, or 128 x 4 RAM or 16 output lines. Trades reduced speed for lowest cost.

Texas Instruments, Inc.
Houston, TX 77001
Phone (713) 494-5115

HARDWARE

PMOS, 15V. 28- and 40-pin DIP's. Both T.I. and Motorola are developing CMOS versions.



Note: TMS-1100/1300 has twice ROM and RAM capacity at 50% more cost.

SOFTWARE:

43 fixed instruction set can be augmented by microcoding the decode PLA. This allows compacting oversized programs into limited on-chip ROM. 24-μsec instruction cycle.

I—DATA MANIPULATION INSTRUCTIONS
Binary two's-complement arithmetic with decimal operations done by test and correction instructions.
Logical and comparison and bit tests.

II—DATA MOVEMENT INSTRUCTIONS
Has implied, immediate and direct addressing modes, with separate for program ROM, data RAM and I/O input and I/O output. Can switch output format by status bit (therefore could have both 7-segment and BCD output formats).

III—PROGRAM MANIPULATION INSTR'S
One-level subroutine calls. Branches on test of status bit. Status bit serves both for carry and for indicating result of comparisons.

IV—PROGRAM STATUS MANIP. INSTR.
None.

HARDWARE SUPPORT: SE-1/TMS-1099 ($26.20) and SE-2/TMS-1098 ($35.63) provides access to ROM connections for development. Prototype boards. "AMPL" development system permits assembly, simulation and (soon) in-circuit emulation.

SOFTWARE SUPPORT: Assembler and simulator on 3 timeshare networks. High-level-language compiler (TIML) and variety of utility programs. Four-day training course at Houston costs $500.

MULTIPLE OUTPUT POWER SUPPLIES

Single, dual, and triple output supplies having output ratings from 1 to 28 volts; from 30 ma to 60 amps. A choice of performance levels, with regulation ranging from ±0.005% to ±0.5%. Many provide dual and triple isolated outputs, matched or dissimilar, in both standard and user-selectable combinations. Others have balanced, tracking outputs.

The variety of shape factors and the mounting versatility of these supplies provide easy answers to mechanical layout problems. Miniaturized models are available for either PCB mounting or, with screw terminals, for chassis mounting. Narrow profile units fit into thin spaces. Metered benchtop supplies are handy sources of power for experimental circuitry. Plug-in modules mount in seconds.

Ask for a copy of our full color, 28-page brochure. It contains complete specifications, outline drawings, prices, and — just as important — it also details our guarantee to ship within 3 days after receiving your order.

Acopian Corp., Easton, Pa. 18042 • Tel: (215) 258-5441

For more information, Circle No. 30

4-BIT MOS

AVAILABILITY: Now (mask in 6 weeks).
COST: $8.55 in 1000 qty with $1500 mask charge. (Total cost will be well under $5 in 100k qty in 1978.)
SECOND SOURCE: Under negotiation.

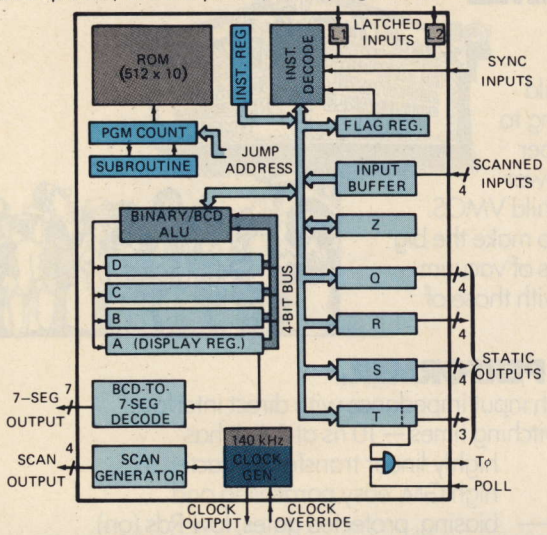
1872

Self-contained one-chip processing system designed to replace small logic systems used in simple control applications.

Western Digital Corp.
3128 Redhill Ave.
Newport Beach, CA 92663
Phone(714)557-3550

HARDWARE

PMOS LSI powered from single 12V supply. 40-pin package, on-chip clock, TTL compatible, mask programmable.



SOFTWARE

37 instructions, with most excuted in 6.25 μsec. Instructions are designed for control applications and do not require computer-programming techniques to use.

I—DATA MANIPULATION INSTRUCTIONS

Binary or BCD arithmetic under program control.
Multi-digit arithmetic operations are programmed in two words instead of a subroutine.

II—DATA MOVEMENT INSTRUCTIONS

Data movement, AND & OR instructions provide for easy movement of data to register files and direct setting and resetting of bits in output registers.

III—PROGRAM MANIPULATION INSTR'S

One-level subroutine call. 16-way conditional jumps and unconditional jump. Special unconditional jump provides vectored addressing.

IV—PROGRAM STATUS MANIP. INSTR.

Binary-BCD set/reset, reset latched inputs.

HARDWARE SUPPORT: Special 64-pin device (CR2872, $40) allows use of external PROM's or RAM's during development of application program.

SOFTWARE SUPPORT: Cross-assembler and simulator available for PDP-11 disc-based systems. Alternatively, W.D. will contract to do in-house programming and deliver board-level solution.

8-BIT MOS

AVAILABILITY: Now.
COST: $9.95 for CPU in 100 qty.
SECOND SOURCE: Mostek, Motorola and SGS/ATES, licensed.

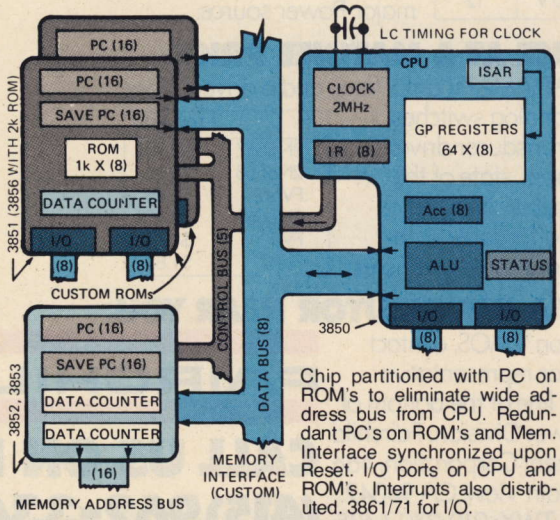
F8 (3850)

Intended to cover both the 8-bit data communication and 4-bit controller markets, F8 has reached high volume use in minimal 2- and 3-chip configurations. (See 3870 for 1-chip version.)

Fairchild Micro Systems
1725 Technology Dr.
San Jose, CA 95110
Phone(408)998-0123

HARDWARE

NMOS, Isoplanar, 40-pin DIP, 5V at 80 mA plus 12V at 25 mA. Minimum system contains 3850 CPU plus one or more program storage units (3851/56/57 PSU's) that can hold up to 2k bytes.



Chip partitioned with PC on ROM's to eliminate wide address bus from CPU. Redundant PC's on ROM's and Mem. Interface synchronized upon Reset. I/O ports on CPU and ROM's. Interrupts also distributed. 3861/71 for I/O.

SOFTWARE

Unique instruction set to go with unusual architecture. Most of 76 basic instructions execute in 2 μsec.

I—DATA MANIPULATION INSTRUCTIONS

Arithmetic and logicals.
Decrement any scratch pad register.
BCD arithmetic
Built-in timer functions distributed in all chips and tied to interrupt.

II—DATA MOVEMENT INSTRUCTIONS

Most instructions operate on GP registers in CPU scratchpad with 1-byte codes. But 1-byte code can reach only first 12 of 64 CPU GP registers, and indirect addressing via "ISAR" register needed to reach the rest.

III—PROGRAM MANIPULATION INSTR'S

"Data Counter" registers can perform pseudo indexing. Subroutines save by hardware for first level and by software-directed movements for deeper levels. Novel interrupt scheme whereby each of system chips is in daisy chain.

IV—PROGRAM STATUS MANIP. INSTR.

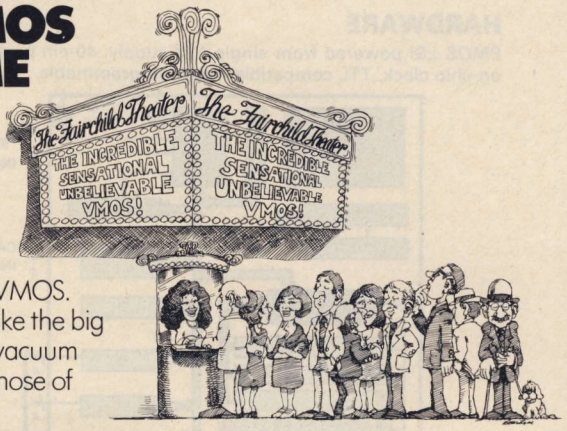
5-bit status registers (sign, carry, overflow, zero and interrupt enable) have instructions to store.

HARDWARE SUPPORT: Complete software and hardware development system (Formulator family). Prototyping and development microcomputer (F8 Kit 1A) available at $185. MOSTEK also offers extensive support.

SOFTWARE SUPPORT: Fortran-IV cross assembler runs on 16-bit minis. Assembler, editor and debugger in resident development system. ROM-based FAIRBUG has load, dump, display and store features.

POWER TRANSISTOR

PRESENTING VMOS FROM A BIG TIME PRODUCER.

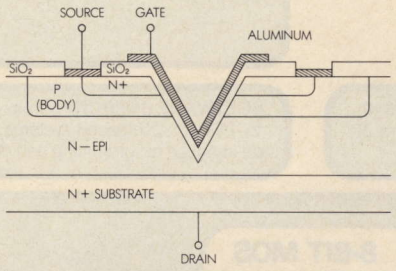


With a major producer like Fairchild behind it, you know VMOS is going to be a big star someday. So remember the name: Enhancement Mode Power Vertical Mosfet. Stagename: Fairchild VMOS.

VMOS transistors are going to make the big time by combining the advantages of vacuum tubes — or lower power FETS — with those of conventional power transistors.

AN AWARD WINNING PERFORMER.

Fairchild VMOS gives you high input impedance with direct interface to CMOS. It's capable of super switching times — 10 ns at 1 A. It has highly linear transfer characteristics, high GM, easy paralleling and biasing, protected gates, low Rds (on) and no second breakdown or thermal runaway. And here's the initial cast of characters:



Cross-section of Fairchild's VMOS power transistor.

	Package	PD	ID	BVDSS
2N6657	TO-3	25 W	2.0 A	60 V
2N6658	TO-3	25 W	2.0 A	90 V
FVN2	TO-39	6.26 W	2.0 A	60 V
2N6661	TO-39	6.25 V	2.0 A	90 V

INTRODUCING A SUPERSTAR SUPPORTING CAST.

In addition to N-Channel VMOS, Fairchild is also producing the world's first P-Channel Power Mosfets with all the features of N-Channel. This means you can now get a complementary product line in VMOS technology from a major Power source.

Device Type	Package	PD	ID (max)	BVDSS	Rds (on)
FVP1	TO-3	25 W	2.0 A	60 V	6
FVP2	TO-39	6.25 W	1.5 A	60 V	12

FEATURE PERFORMANCE AT A MATINEE PRICE.

Whether you're designing CATV, MATV amplifiers, audio drivers, core memories, switching regulators, analog switches, pin diode drivers, lasers, transducer drivers, or microprocessor interfaces, state of the art designs are now possible. And just as importantly, they're now affordable with Fairchild Power VMOS. Here are some examples:

	100-999
2N6657	$4.20
2N6658	$5.05
FVN2	$1.85
2N6661	$2.95
FVP1	$4.25
FVP2	$1.85

NOW PLAYING AT A DISTRIBUTOR NEAR YOU.

For more information on VMOS, contact your Fairchild sales office or representative today. Or use the direct line at the bottom of this ad to reach our Power Division. Fairchild Camera and Instrument Corporation, 464 Ellis Street, Mountain View, CA 94042. Tel: (415) 962-3343. TWX: 910-379-6435.

FAIRCHILD

CALL US ON IT.

(415) 962-3343

For more information, Circle No. 31

8-BIT MOS

AVAILABILITY: Now.
COST: Masked-ROM versions (8048/8041) will sell at $5 in high volumes. EPROM versions are $245 for the 8748, $250 for the 8741.
SECOND SOURCE: AMD, Signetics and NEC, licensed, mask exchange.

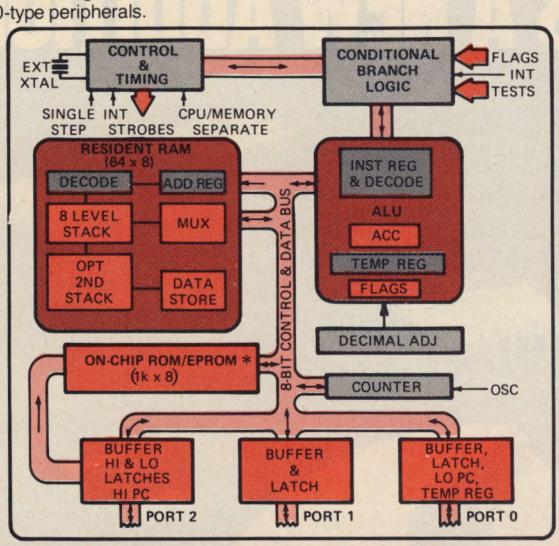
8048/8748, 8041/8741, 8035

Intel Corp.
3065 Bowers Ave.
Santa Clara, CA 95051
Phone (408) 987-8080

These devices have 1k-byte on-chip program memories, small 64 byte RAM's, timers, interrupts and 27 I/O lines. The 8048/8748 is a stand-alone μC; the 8041/8741, a slave computer for peripheral control in the 8035, a fall-out unit (ROM not used).

HARDWARE

NMOS, silicon gate, +5V operation, 40-pin pkg. Compatible with all 8080-type peripherals.



* Note: +5V EPROM's in 8748 and 8741 are more susceptable to erasure by sunlight than high voltage EPROM's.

SOFTWARE

Over 90 instructions. Most single cycle. Cycle time=2.5 μsec. Takes best instructions of 4004 and 8080, but not 8080 compatible.

I—DATA MANIPULATION INSTRUCTIONS
Arithmetic and logic.
Bit set and reset.
Two working banks of 8-bit registers.

II—DATA MOVEMENT INSTRUCTIONS
Both internal and external RAM are fully accessible by instruction set. Indirect and direct data fetches.

III—PROGRAM MANIPULATION INSTR'S
Decrement and skip if zero.
Over 20 conditional branches.
An 8-level stack with expansion capability.
Two vectored interrupts.
Two programmable flag bits under software control.

IV—PROGRAM STATUS MANIP. INSTR.
Status word is fully accessible and is stored in the stack.

Note: At press time Intel announced the 8021, a low end, lower cost version of the 8048. Available details are summarized in a **box** in the introductory text of this article.

HARDWARE SUPPORT: PROMPT-48 stand-alone development aid ($1750 lets user enter programs in RAM during development, then burn them into 8748 for trial via the built-in EPROM programmer. Unit contains resident monitor.

SOFTWARE SUPPORT: Macroassembler on floppy disc or paper tape, resident text editor in MDS development system, debug software in ICE-48 in-circuit emulator. "Insite" program library contains over 350 programs.

8-BIT MOS

AVAILABILITY: Now for both.
COST: $13.10 for 8080A in 100 qty; $19 for 8085.
SECOND SOURCE: 8080A: Siemens, licensed; AMD, TI, NEC, National, Signetics Hitachi; 8085: AMD and Siemens, licensed; NEC.

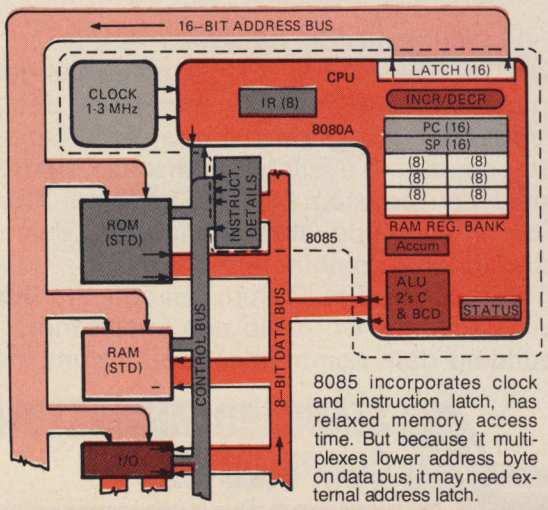
8080A/8085

8080A is most popular μP by wide margin. Software compatible 8085 reduces parts count and runs faster. Upcoming 16-bit 8086 may or may not be part of family.

Intel Corp.
3065 Bowers Ave.
Santa Clara, CA 95051
Phone (408) 987-8080

HARDWARE

8080A: NMOS, 2-phase clock, uses ±5 and +12V. 8085 needs only +5V. High speed versions (4 MHz 8080A, 5 MHz 8085) expected in 1978.



8085 incorporates clock and instruction latch, has relaxed memory access time. But because it multiplexes lower address byte on data bus, it may need external address latch.

SOFTWARE

Three 16-bit pointer registers allow efficient addressing of 65k memory space. 78 basic instructions, with 2 μsec typ add-register-to-accumulator execute time.

I—DATA MANIPULATION INSTRUCTIONS
Arithmetic and Logic.
BCD arithmetic.
Double-precision operations (instructions string two data bytes together as 16-bit word).

II—DATA MOVEMENT INSTRUCTIONS
Uses three pairs of so-called GP registers as pointers in CPU RAM bank to address low- and high-order bits of 16-bit memory address. Can do multiple indexing with these, but takes additional steps compared to classical index register concept.

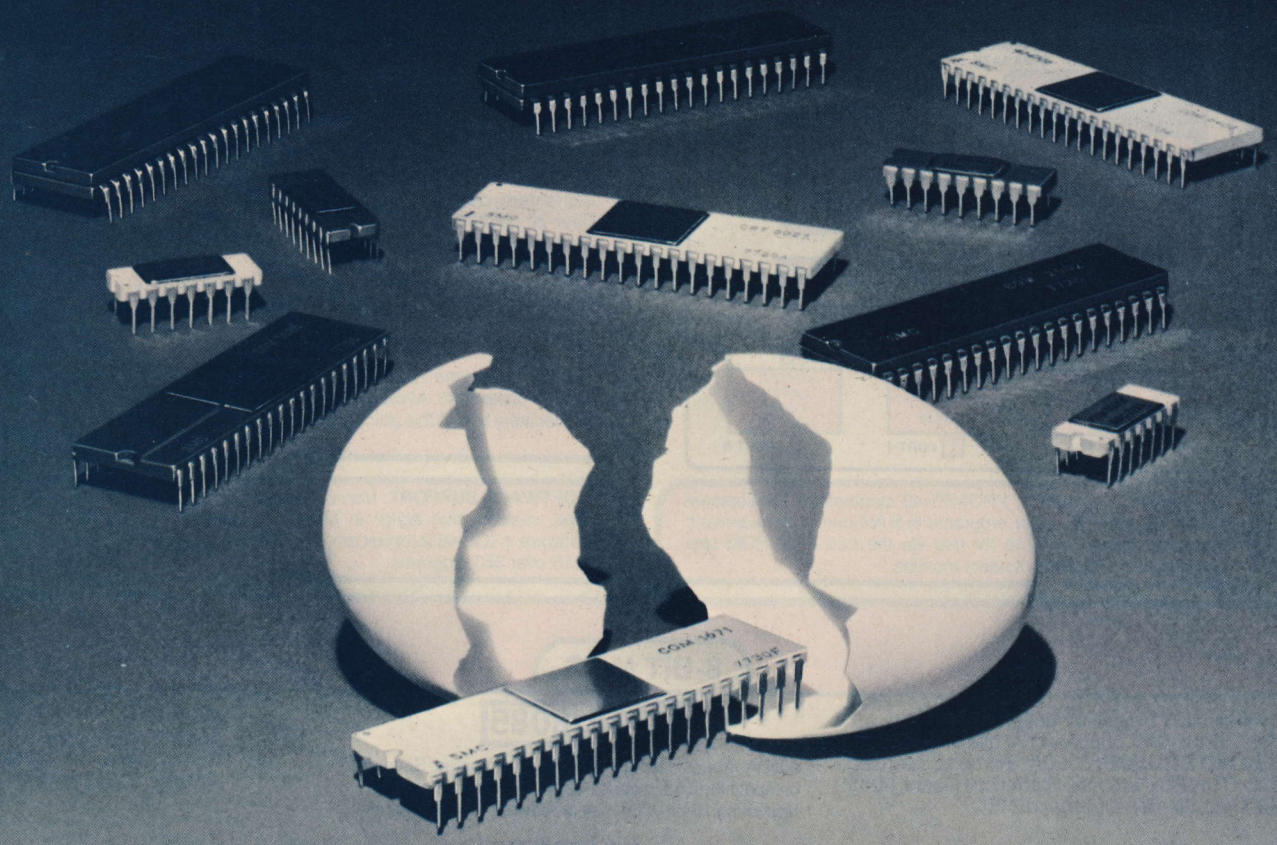
III—PROGRAM MANIPULATION INSTR'S
Uses stack pointer (SP) to create LIFO stacks in external RAM for unlimited subroutine nesting.
All GP registers can be incremented and decremented.
Multiple interrupt capability.
Bus controls allow adding DMA.

IV—PROGRAM STATUS MANIP. INSTR.
Software access to status register.

HARDWARE SUPPORT: Wide range — from board assembler to full development systems — from many manufacturers, including support on Tektronix 8001/8002. Intel offers ICE-85, SDK-85 and UPP-855 for 8085.

SOFTWARE SUPPORT: PL/M high-level language, relocating macro-assembler and text editor resident in MDS development system. "Insite" library contains over 200 programs.

THE LARGEST FAMILY OF MOS/LSI DATA COMMUNICATIONS CIRCUITS PROUDLY ANNOUNCES A NEW ADDITION:



THE COM 1671 ASTRO

We've lead the way in MOS/LSI data communications circuits with proprietary products like our COM 5025 Multi-Protocol Synchronous Receiver/Transmitter and our COM 2017 and COM 2502 Universal Asynchronous Receiver/Transmitter plus others. Now we're second sourcing Western Digital's UC 1671 ASTRO with our new COM 1671.

It's a software responsive device capable of handling complex communications formats in a variety of systems applications.

Like our COM 5025, and our recently announced CRT 5027, the new COM 1671 ASTRO has high speed, and high density n-channel Coplamos® technology in a 40 lead ceramic DIP.

And it carries the Standard Microsystems Corp. name so you know you can count on it for maximum performance and reliability.

We make custom LSIs too.

SMC's custom circuit department has helped many medium-volume users with the design and production of custom devices. Applications personnel are available to discuss the tradeoffs involved in custom MOS/LSI design. The solution may include either standard or custom circuits or a combination of both.

For standard or custom LSI come to Standard Microsystems Corp. No one knows more about building data communications circuits than us.

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(516) 273-3100 TWX-510-227-8898

PICTURED ABOVE: VIDEO TIMER/CONTROLLER CRT5027 ■ UNIVERSAL SYNCHRONOUS RECEIVER/TRANSMITTER COM5025 & COM2601 ■ BAUD RATE GENERATOR COM5026 & COM5046 ■ DUAL BAUD RATE GENERATOR COM5036 & COM5016 ■ UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER COM6402, COM2017 & COM2502 ■ ASYNCHRONOUS/SYNCHRONOUS RECEIVER/TRANSMITTER COM1671

For more information, Circle No. 32

8-BIT MOS

650X, 651X

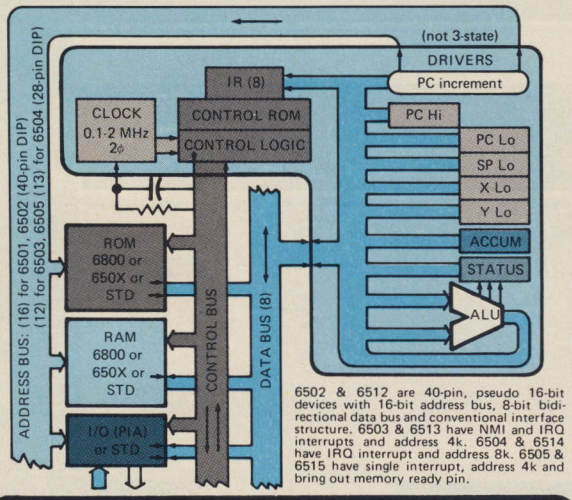
AVAILABILITY: Now.
COST: $10.90 for basic 1-MHz 6502 and 6512 in 100 qty; $8.50 for others. Add 20% for each MHz increase in speed up to 4 MHz.
SECOND SOURCE: Synertek and Rockwell, both licensed.

Somewhat similar to 6800, but not software compatible. 650X μP's have on-chip oscillator & clock driver, while 651X machines (aimed primarily at multiple-processor systems) require 2-phase, high-level clock.

MOS Technology, Inc.
950 Rittenhouse Rd.
Norristown, PA 19401
Phone (215) 666-7950

HARDWARE

NMOS, silicon gate, +5V, 250 mW. Versions are available that can run at up to 4 MHz clock rates (250 nsec cycle time).



6502 & 6512 are 40-pin, pseudo 16-bit devices with 16-bit address bus, 8-bit bidirectional data bus and conventional interface structure. 6503 & 6513 have NMI and IRQ interrupts and address 4k. 6504 & 6514 have IRQ interrupt and address 8k. 6505 & 6515 have single interrupt, address 4k and bring out memory ready pin.

HARDWARE SUPPORT: KIM-1 pc assembly has keyboard and display ($245). Rockwell offers System-65 development system with dual floppies ($4800). Coordinated effort by MOS Technology, Synertek and Rockwell to develop support chips.

SOFTWARE

Fifty-seven instructions execute in 2.5 μsec, typ; 13 powerful addressing modes.

I—DATA MANIPULATION INSTRUCTIONS
Arithmetic and logical. Decimal mode via control bit in status register. Can operate on locations in memory space (which can be either RAM or I/O ports).

II—DATA MOVEMENT INSTRUCTIONS
True indexed addressing, though index offset limited to 8 bits in two CPU registers, X and Y. Short-form addressing to zero page. Has two sophisticated indirect indexed and indexed indirect instructions for handling tables.

III—PROGRAM MANIPULATION INSTR'S
Conditional branches with signed relative addresses. Non-maskable and/or maskable interrupt, depending on model. Stack pointer for implementing 256-byte LIFO in external RAM.

IV—PROGRAM STATUS MANIP. INSTR.
Push and pull status register from memory stack. Set and clear carry, decimal mode and interrupt bits. (6502 & 6512 have external input to one status bit, useful for handshaking with peripherals.)

SOFTWARE SUPPORT: Cross-assembler that runs on DEC minis, debugger, text editor, math package, resident assembler in ROM form, Fortran compiler, cross-emulator and BASIC.

8-BIT MOS

MCS-660X (6500/1)

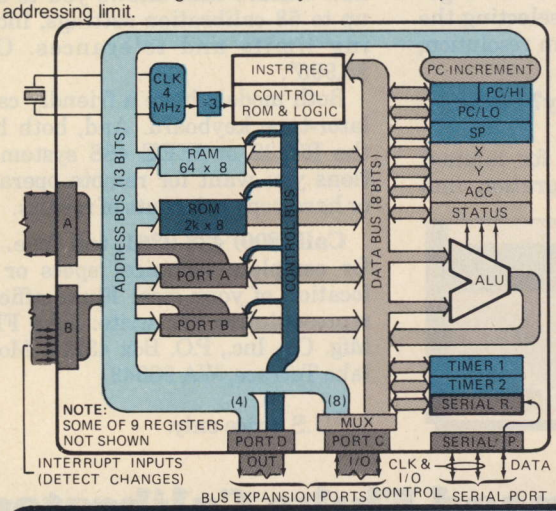
AVAILABILITY: First qtr '78 for both MOS technology and Rockwell versions.
COST: Under $10 in volume; approx $6 in high volume.
SECOND SOURCE: Possibly Synertek and Rockwell for 660X; possibly Synertek and MOS Technology for 6500/1.

Single-chip 650X-type μC's. Rockwell's 6500/1 will be essentially same as 650X, while MOS Technology's 660X will be more powerful machine.

MOS Technology, Inc.
950 Rittenhouse Rd.
Norristown, PA 19401
Phone(215)666-7950

HARDWARE

660X: NMOS, depletion mode, silicon gate, +5V, 40-pin DIP. Initially 1MHz, 2k bytes ROM, 64 bytes RAM. Later, higher speeds and versions accommodating other memory combinations up to 12-13 bit addressing limit.



HARDWARE SUPPORT: Special 64-pin device for prototyping. 660X's ROM can carry "KIM" or "TIM" monitors, so users can develop stand-alone prototyping stations. Besides 650X parallel-bus support chips, 660X will have serial-bus peripheral devices.

SOFTWARE

660X is upward compatible with 650X, with 61 new instructions giving user access to architectural additions. Cycle time, 1 μsec; execution time, 2 μsec avg.

I — DATA MANIPULATION INSTRUCTIONS
Decimal add now sets ZERO flag.

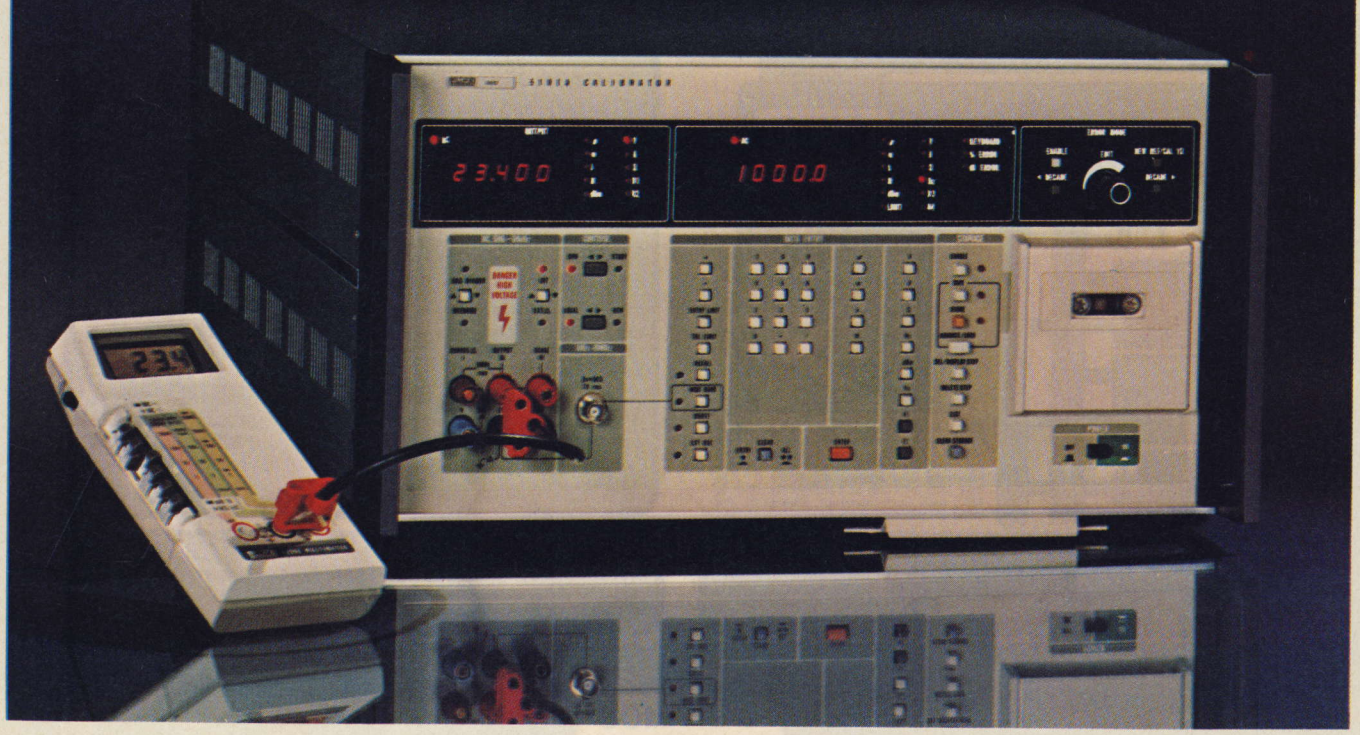
II — DATA MOVEMENT INSTRUCTIONS
New instructions take advantage of on-chip memory and allow software-direct data movements in and out of 9 new on-chip registers, including those for I/O ports and timers. Stack pointer is "aimed" at page zero to allow use with small RAM's.

III — PROGRAM MANIPULATION INSTRUCTIONS
Optional use of 16-bit time as full-range indexer with software choice of auto decrement. Auto-decrement and test-for-zero for refreshing displays from RAM. Branch-always and compare-timer instructions.

IV — PROGRAM STATUS MANIPULATION INSTRUCTIONS
Unused 650X flag-bit 5 brings address and internal buses out to ports for expansion.

SOFTWARE SUPPORT: All software packages for 650X family.

Recalibrate.
(Your thinking and your budget)



Our new 5100/5101A calibrators can calibrate VTVMs, VOMs, 3½-, 4½- and most 5½-digit DMMs around, in a fraction of the time it takes you now! (It's a cal lab in a box! All at an average price under $9,000.)

For $10,000 to $15,000, you *could* invest in an intricate maze of instruments that takes a wizard to operate. Or, you could fill a room with computer-based hardware and expensive talent. About $100,000 worth.

The Fluke μP-controlled alternative.

We've designed the new 5100A and 5101A for production test, QA and cal lab applications that need large system flexibility at a fraction of large system cost.

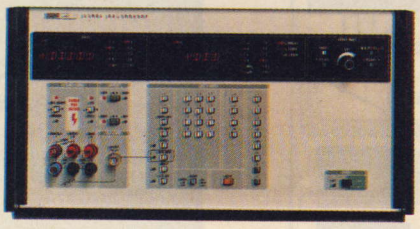
The heart of our new meter calibrators is a microprocessor that eliminates mechanical switches—the largest contributor to failure in conventional calibrators.

And, you can enter your tolerances in dB, volts or percent. The μP converts for you! For safety, store current or voltage limits and protect both your operator and the meter being calibrated.

Microprocessor control also facilitates scaling (for linearity checking), and makes your calibrator a *rangeless* instrument, always selecting the proper range for maximum resolution, *automatically!*

Automation or economy? Fluke has both.

The 5100A is perfect for manual bench operation or integration into your existing cal system to upgrade it to Fluke standards of calibration excellence. Priced at $6,995*, you save dollars but don't sacrifice accuracy or overall performance.



For perfection in automated calibration, you'll want the 5101A with its *mini-tape cassette reader,* a unique new feature that allows you to store up to 58 calibration settings, including limits and tolerances. Only $8,995*.

Both models have a friendly calculator-type keyboard. And, both have the RS232 or IEEE 488 system options you want for remote operation or hard-copy printouts of results.

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2010-8001

For Literature, Circle No. 33
For Demonstration, Circle No. 34

8 BIT MOS

AVAILABILITY: Now.
COST: $9.95 in 1000 qty, with much lower prices in large volumes.
SECOND SOURCE: Fairchild and Motorola, licensed.

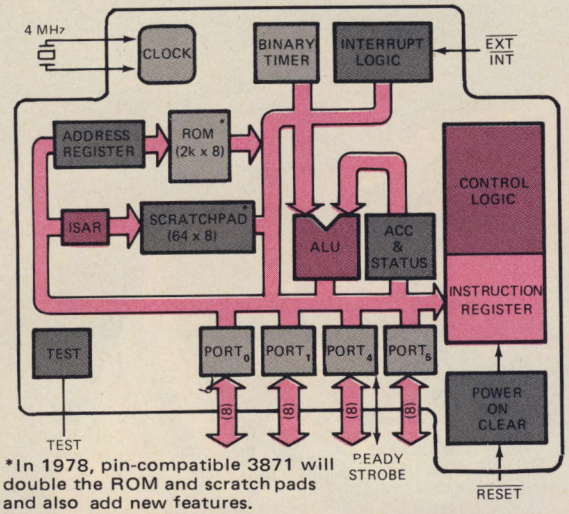
3870

Mostek
1215 W. Crosby Rd.
Carrollton, TX 75006
Phone(214)242-0444

A complete F8 μC on one chip, the 3870 features 2k x 8 program ROM, 64 x 8 RAM, 32 bits of bidirectional I/O ports and a timer/event counter. Device has gained wide popularity in short time.

HARDWARE

NMOS, silicon gate, +5V (± 10%), 40-pin DIP, 300 mW. F8 hardware compatibility for system expansion. Planned are +5V EROM and 4k ROM versions.



*In 1978, pin-compatible 3871 will double the ROM and scratch pads and also add new features.

SOFTWARE

Executes F8's complete set of 70 instructions, except STORE. Most execute in 2 μsec. Software compatible with F8 systems.

I—DATA MANIPULATION INSTRUCTIONS
Arithmetic and logicals.
Decrement any scratch-pad register.
BCD arithmetic.
Built-in binary timer (with start/stop and pulse-width interval capabilities, plus 2/5/20 programmable prescaler).
Timer is tied to interrupt.

II—DATA MOVEMENT INSTRUCTIONS
Most instructions operate on GP registers in CPU scratch pad with 1-byte code. Because 1-byte code can reach only first 12 registers of 64, you need indirect addressing via "ISAR" register to reach the rest.

III—PROGRAM MANIPULATION INSTR'S
Full vectored-interrupt capability.
DC registers can perform pseudo-indexing.
Subroutines save by hardware for first level; by software for deeper levels.

IV—PROGRAM STATUS MANIP. INSTR.
5-bit status registers (sign, carry, overflow, zero and interrupt) have instructions to store.

HARDWARE SUPPORT: EMU-70 emulation and prototyping board — ROM- or PROM-based — has in-circuit emulation capability. Prototyping kit, AIM-70 (real-time emulator that gives snapshot software in ROM) and SDB 50/70 software development board.

SOFTWARE SUPPORT: Fortran IV cross assembler for ≥ 16-bit minis; resident edit, assembly and debug programs; and many ROM-based software packages. 3870 uses all F8 application programs.

8 BIT MOS

AVAILABILITY: Now.
COST: In 25-99 qty: $17.95 for 1-MHz 6800, $25 for 1.5-MHz 6800A, $30 for 2-MHz 6800B, $22 for 6802.
SECOND SOURCE: AMI, Fairchild, Hitachi and Sescosem, licensed. Fujitsu MB8861 is a slightly enhanced 6800 with 5 more instructions.

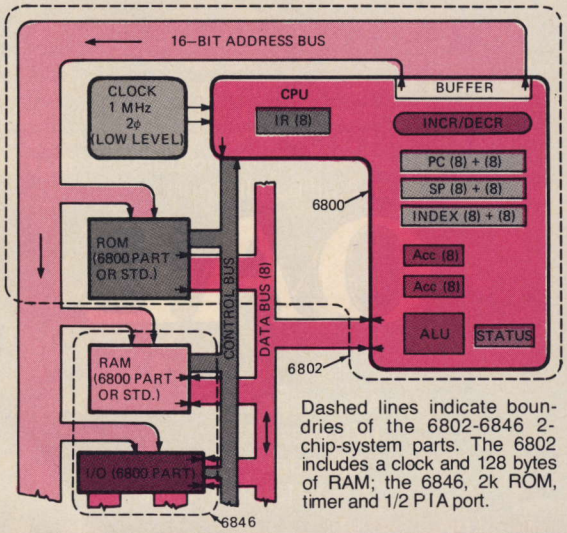
6800

Motorola Inc., Semiconductor Div.,
5005 E. McDowell Rd.,
Phoenix, AZ 85008.
Phone (602)244-6900

Popular μP family is being expanded to include faster 6800 CPU's, a 6802/6846 2 chip μC, a 6801 1-chip μC (see separate listing) and a 6809 16 bit "super" CPU.

HARDWARE

NMOS, silicon gate, 40-pin DIP, +5V, 500 mW. Versions with −55 to +125°C operation available.



Dashed lines indicate boundries of the 6802-6846 2-chip-system parts. The 6802 includes a clock and 128 bytes of RAM; the 6846, 2k ROM, timer and 1/2 PIA port.

SOFTWARE:

Copied from the PDP-11 set as closely as is possible with a shorter word-length machine. Execution times from 2-5 μsec.

I—DATA MANIPULATION INSTRUCTIONS
Arithmetic and logic.
Instructions to take advantage of two accumulators.

II—DATA MOVEMENT INSTRUCTIONS
Can reach the first 256 locations of memory with short instructions.
Can list-process efficiently with the Index Register.
Relative addressing allows data relocation.

III—PROGRAM MANIPULATION INSTR'S
Has the PDP-11 Branches and Conditional Branches. Unlimited subroutine nesting via stack pointer addressing LIFO stacks in RAM.
Does not have vectored interrupt, but can achieve function with software.

IV—PROGRAM STATUS MANIP. INSTR.
Instructions for storing status register.

HARDWARE SUPPORT: Various levels of pc-board and console aids, including the EXORciser and Evaluation MOD/2. Tektronix 8001/8002 supports the 6800. Many new peripheral chips being added to family.

SOFTWARE SUPPORT: Cross-assembler, interactive simulator, editor, macroassembler, disc-based operating system, debug, PL/M, BASIC and FORTRAN. Over 65 programs in user library.

There's a New Force in PROM Programming

OAE introduces a powerful new concept in PROM programming-low cost programmers that interface in less than a minute! Read, program, verify, duplicate. Plug an **OAE** programmer into a read only PROM socket and you instantly have all the features of even the most expensive programmers.

OAE'S PP-2708/16 PROM programmer plugs directly into any 2708 or TMS 2716 memory socket. Simply drop a PROM into the zero insertion force socket and a short software routine sends the data over the eight lower address lines using **OAE'S** unique* interfacing technique. No additional power supplies are required and all timing and control sequences are handled by the programmer. In addition, multiple programmers may be connected in parallel for gang programming.

Each programmer comes *complete* with a DC to DC switching regulator, ten turn cermet trimmers for precise program voltage and pulse width alignment, and a zero insertion force socket. The unit is packaged in a handsome black anodized aluminum case for table top operation. A 5 foot ribbon cable terminated with a 24 pin plug connects the unit to the read only PROM socket. (The programmer may also be interfaced to an 8-bit parallel port.)

OAE Inc.

Oliver Advanced Engineering Division
676 West Wilson Avenue
Glendale • Ca. • 91203
(213) 240 • 0080

Model PP-2708/16
Programs 2708s & TMS 2716s $295.00

Model PP-2716
Programs the unique Intel 2716 EPROM $295.00

SALE! TMS 2708's. IK x 8 EPROM-450 NS . $ 15.00 ea.
(Quantities of 10)

*Pats. Pending

For more information, Circle No. 35

8-BIT MOS

AVAILABILITY: Now.
COST: $20 in 2500 (min) qty; $10 at 10k; $3-$4 at 100k.
SECOND SOURCE: Will be EM&M SEMI.

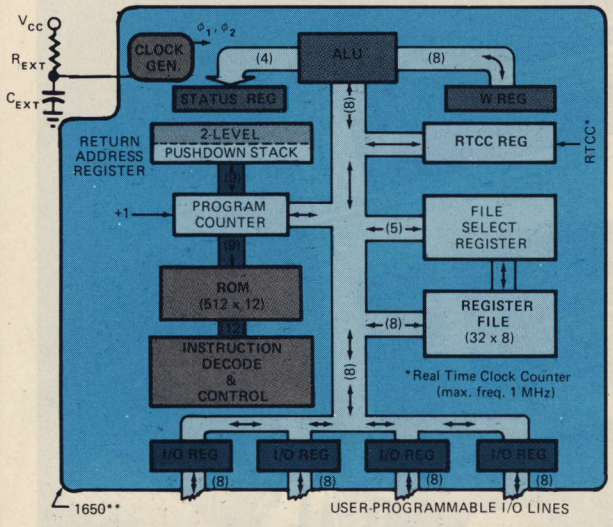
PIC1650/1655/1670

Containing ROM, RAM I/O and CPU, the PIC1650 is a complete, single chip, 8-bit μC. It's the only low-end machine to have mini-type access to its register stack.

General Instrument Corp.
600 W. John St.
Hicksville, NY 11802
Phone(516)733-3000

HARDWARE

NMOS device uses +5V. On-chip oscillator needs external R & C to provide 2-phase clock. 40-pin package.



SOFTWARE

User defines ROM program. Most of the 31 instructions execute in 1 μsec. Set is strong in bit manipulations and logical instructions. Word width of 12 bits shortens programs.

I DATA MANIPULATION INSTRUCTIONS
Add & subtract.
Logicals.
Rotate right and left.
Swap halves.
Bit set and clear.
Skip if zero.

II DATA MOVEMENT INSTRUCTIONS
Page addressing.
Move file.

III PROGRAM MANIPULATION INSTR'S
Move literal to W.
Call Subroutine.
Go to, return.

IV PROGRAM STATUS MANIP. INSTR.
Can bit test on status-register carry, decimal carry and zero.

** 1655 has 20 I/O lines; 1670, 1k words of ROM and 4 levels of stack.

HARDWARE SUPPORT: PIC emulator card contains 1650, resident "PICBUG" and 1664 (a special 1650 in 64-Pin DIP with ROM address and data lines brought out, so external RAM can be used for program development). TTL emulator board also offered.

SOFTWARE SUPPORT: "PICAL" assembler and "PICSIM" simulator in Fortran IV for use on minis, timeshare networks or G.I.'s "GIMINI" μC.

8-BIT MOS

AVAILABILITY: Second qtr '78 for masked-ROM version, 3rd qtr '78 for EPROM μC.
COST: Not yet available.
SECOND SOURCE: Possibly the same firms that now second-source the 6800.

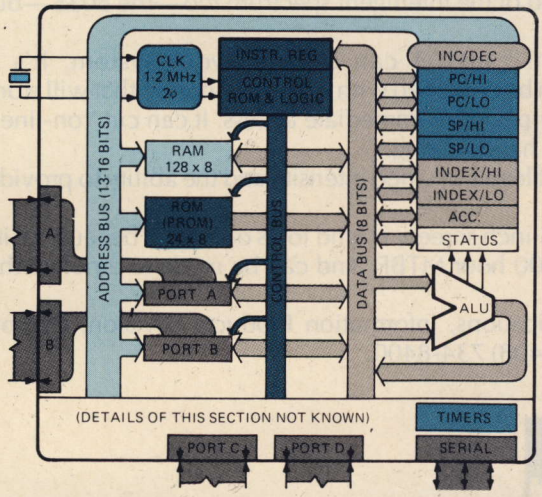
6801

Single-chip, but expandable, μC version of 6800. Features "PIA-type" parallel ports, a serial port and sophisticated timer. Machine will be suited to multiprocessing and master/slave modes.

Motorola Integrated Ckts Div.
3501 Ed Bluestein Blvd.
Austin, TX 78721
Phone (512) 928-2600

HARDWARE

NMOS, depletion mode, +5V, 40-pin DIP. CPU section is identical to 6800 (no truncating of address registers).



SOFTWARE

Upward compatible with 6800, but 12 new instructions.

I — DATA MANIPULATION INSTRUCTIONS
New: Hardware multiply and divide; 16-bit add, subtract shift and rotate; add B register to index register. From 6800: Arithmetic and logic; instructions to take advantage of dual accumulators.

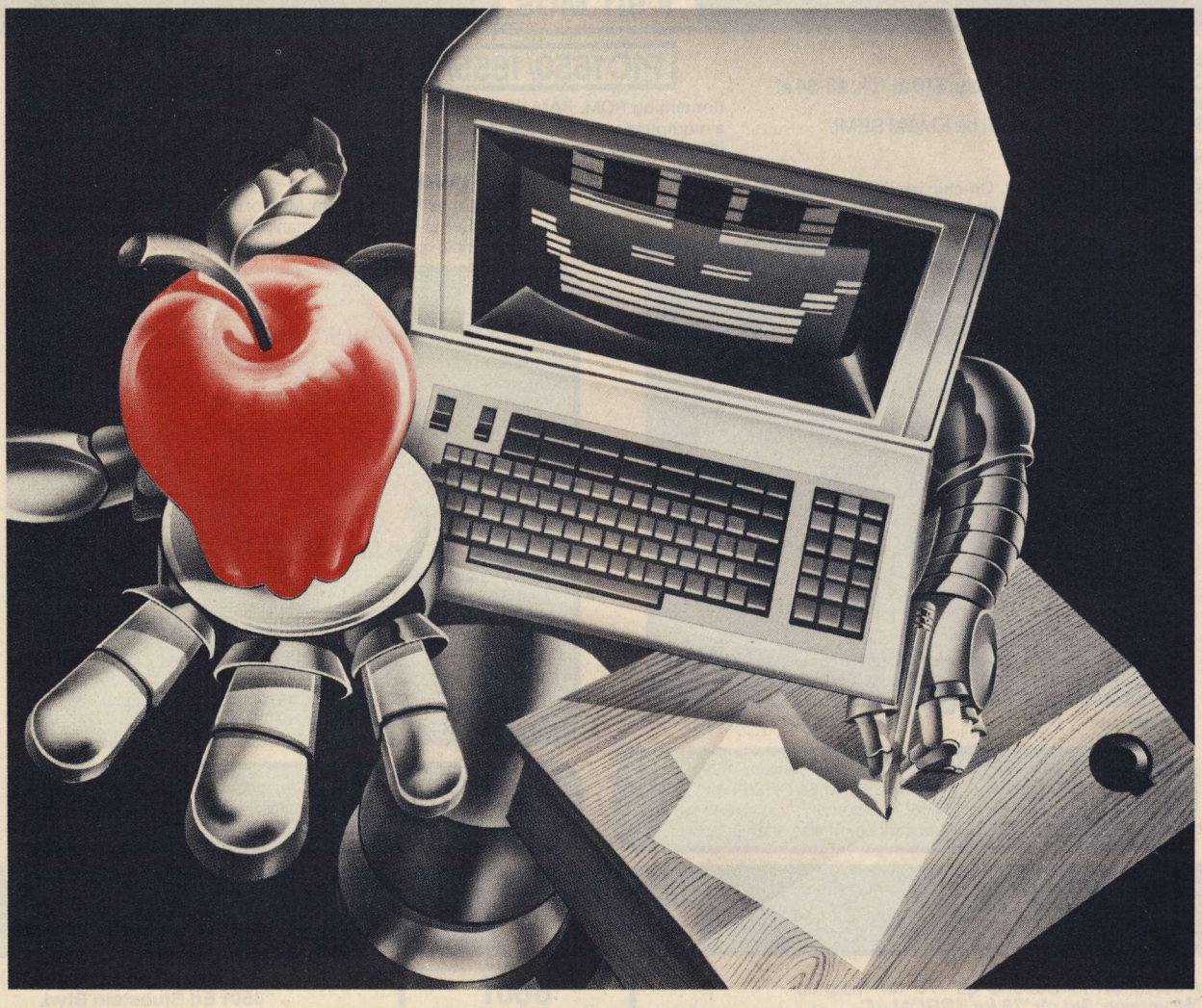
II — DATA MOVEMENT INSTRUCTIONS
New: Instructions to push and pull index register on and off stack (in RAM). From 6800: Can reach the first 256 memory locations with short instructions; can list-process efficiently with index register; relative addressing allows data relocation.

III — PROGRAM MANIPULATION INSTRUCTIONS
From 6800: Has PDP-11 branches and conditional branches; unlimited subroutine nesting via stack-pointer addressing LIFO stacks in RAM; achieves vectored interrupt via software.

IV — PROGRAM STATUS MANIPULATION INSTRUCTIONS
From 6800: Instructions for storing status register.

HARDWARE SUPPORT: Emulation board will be available early in 1978.

SOFTWARE SUPPORT: Will probably be able to use existing 6800 development system.



When you want more than a handshake but don't need a "Phi Bete."

Our 8030B is at the head of its class if you're looking for a smart CRT information terminal.

Of course, we can provide a Phi Beta Kappa at the top end of the intelligent spectrum too—the 8035—but you can always upgrade to that when you're ready.

In the meantime, here's a sampling of the "smarts" 8030B can bring to your system. It's a semi-programmable keyboard and display combination. It can be equipped with a memory option that will store and retrieve up to six pages of characters (1920 characters per page) for immediate access. It can cut "on-line" time as much as 50% and is, of course, available for the usual handshaking.

It's smart features also include full editing capability, eight levels of video intensity and the ability to provide 128 unique function codes.

It's 8080 based and delivers up to 9600 BAUD. It has a 15 inch screen, is kind to its operators because of its 14 x 9 dot matrix and its simplicity of operation. It has an 8000 hour MTBF. And can be made to emulate the protocol of most host computer systems.

Write or call Michael L. Squires for details and specifications, Information Products Division, Omron Electronics, Inc., 432 Toyama Drive, Sunnyvale, CA. 94086. (408) 734-8400.

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8-BIT MOS

8060 (SC/MP-II)

AVAILABILITY: Now for both versions.
COST: SC/MP-II is $9 in 100 qty in plastic. Price expected to drop under $5 in volume in 1978.
SECOND SOURCE: Signetics, licensed.

SC/MP-II is NMOS version of PMOS SC/MP. Though described as simple μP by National, this machine has sophisticated features that demand close study by user.

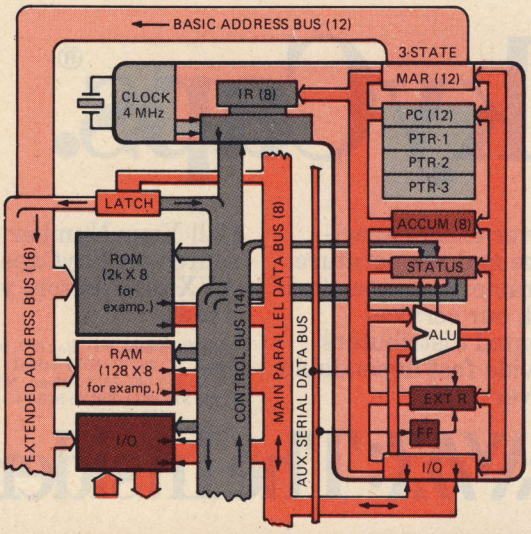
National Semiconductor Corp.
2900 Semiconductor Dr., M/S 470
Santa Clara, CA 95051
Phone(408)737-5000

HARDWARE

NMOS SC/MP-II uses +5V, dissipates 250mW. 40-pin DIP. Incorporates controls that permit 3 SC/MP's to operate in master/slave fashion on same bus for multiprocessing use.

SOFTWARE

Pointer-type addressing, auto indexing, plus special instructions to utilize unique I/O features. Executions take 5-25 μsec.



I—DATA MANIPULATION INSTRUCTIONS
Add, complement and add
Decimal add
Logicals
Delay via countdown in accumulator—22 μsec to 522 msec.

II—DATA MOVEMENT INSTRUCTIONS
Instruction codes carry bits that specify which pointer register (PTR) is to be used. This pointer must be preloaded by previous instruction. The second byte of 2-byte instructions carries either displacement for address (a form of indexing) or immediate data.

III—PROGRAM MANIPULATION INSTR'S
Serial I/O can be commanded via the Extension register (see diag.) Both subroutines and interrupts are handled by swapping a pointer register (PTR) with the PC. Unlimited nesting of subroutines is accomplished via a PTR that forms stack in main memory.

IV—PROGRAM STATUS MANIP. INSTR.
Instruction to handle status register as a whole and as individual bits.

HARDWARE SUPPORT: LCDS low-cost development system ($499) includes keyboard, display, TTY interface, RAM and ROM. Cards offered for prototyping and short-run production.

SOFTWARE SUPPORT: Cross-assemblers. "SUPAK" line assembler and development utility (8 ROM's, $300). "NIBL" language suited to control applications (2 ROM's, $85) requires 2k RAM.

8-BIT MOS

CDP1802

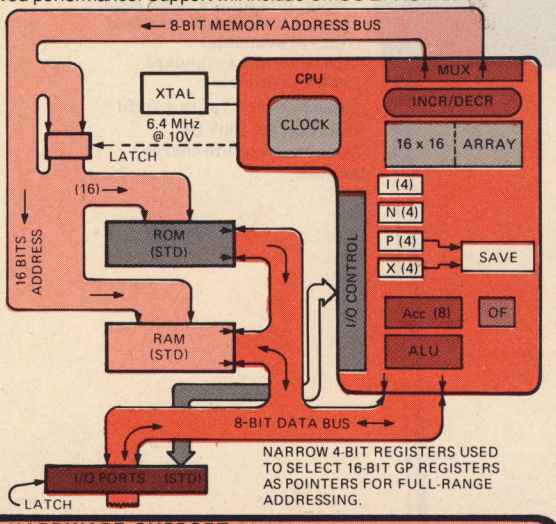
AVAILABILITY: Now.
COST: $15.90 in 100 qty.
SECOND SOURCE: Hughes and Solid State Scientific, licensed.

Second-generation CMOS machine makes extensive use of pointer-based addressing. Family device specs match standard 4000B CMOS, except for 11-15V voltage limits. Two- and one-chip μC's are planned.

RCA Solid State Div.
Route 202
Somerville, NJ 08876
Phone(201)685-6462

HARDWARE

Static CMOS chip consumes 10 mW at 3.2 MHz/5V; 40 mW at 6.4 MHz/10V. 40-pin pkg. 3-15V, −55 to +125°C operation. Noise immunity 30% of V_{DD}: Family being converted to CMOS/SOS for improved performance. Support will include CMOS EPROM in '78.



SOFTWARE

91-command instruction set uses pointer-based architecture. Most instructions require 2.5 μsec for fetch and execute.

I—DATA MANIPULATION INSTRUCTIONS
Add, subtract and logical.
Reverse subtract (M-Accum).
Right and left shift (with and without carry).
Register indexed and data immediate addressing formats.

II—DATA MOVEMENT INSTRUCTIONS
Addressing 2-stage using registers in 16×16 array as pointers. The 4-bit registers select pointers and define their function.
I/O, interrupt, and DMA control built into CPU.

III—PROGRAM MANIPULATION INSTR'S
Jump to subroutine by having 4-bit register "P" address different GP register in 16×16 array as PC. Return from subroutine by re-addressing original GP register as PC. Can use pointers to create multiple stacks in RAM.

IV—PROGRAM STATUS MANIP. INSTR.
Mark, save, and return instructions used to manipulate interrupt enable and "P" and "X" registers.
Software maskable interrupt via line into CPU.

HARDWARE SUPPORT: COSMAC development system (2900). Evaluation kit ($249) μC interfaces to TTY or microterminal ($140 hand-held TTY simulator). Microtutor stand-alone educator. Tektronix 8001/8002 will include 1802 support.

SOFTWARE SUPPORT: Cross assemblers, editors, and simulators for 16-bit minis and for ≧32-bit computers; also available on GE Timeshare and National CSS. Resident assembler and editor included with COSMAC.

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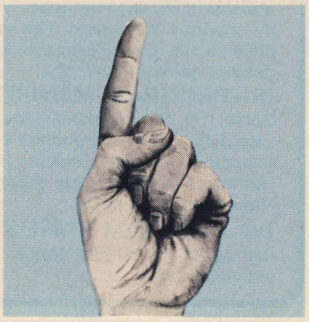

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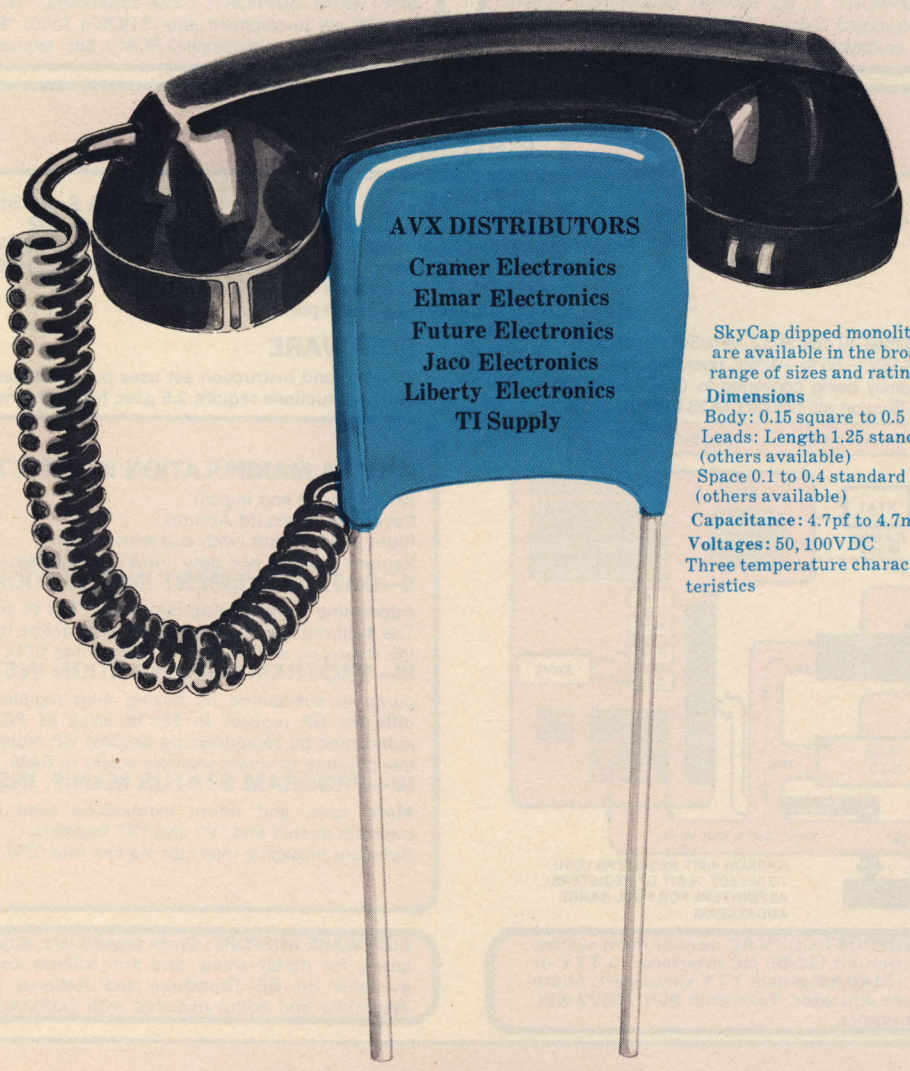
(716) 372-6611 TWX: 510-245-2815

AVX: The Insiders



SkyCap dipped monolithics are available in the broadest range of sizes and ratings.

Dimensions
Body: 0.15 square to 0.5 square
Leads: Length 1.25 standard (others available)
Space 0.1 to 0.4 standard (others available)

Capacitance: 4.7pf to 4.7mfd

Voltages: 50, 100VDC

Three temperature characteristics

For more information, Circle No. 37

8 BIT MOS

AVAILABILITY: Now.
COST: Under $24 for CPU in 100 qty; under $24 for PPS-8/2 in 1000 qty.
SECOND SOURCE: None (National Semiconductor not active).

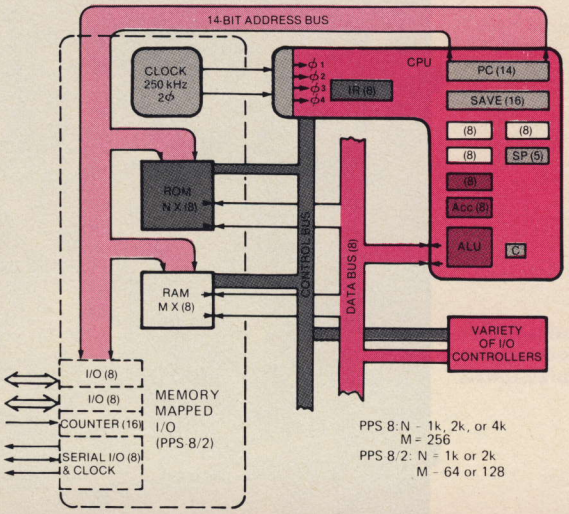
PPS-8, PPS-8/2

Aimed at low-cost controller and processor applications requiring high throughput.

Rockwell International
3310 Miraloma Ave.
Anaheim, CA 92803
Phone(714)632-3729

HARDWARE

PMOS at 17V supply in 42-pin pkg. Upward compatible with PPS-4, PPS-8/2 incorporates on-chip clock, I/O, ROM and RAM in 52-pin pkg.



SOFTWARE

Over 90 instructions, many unique, designed to take advantage of sophisticated architecture. Most executed in 1 cycle or 4 μsec.

I DATA MANIPULATION INSTRUCTIONS
Binary arithmetic and logicals. Shifting and compare.
Decimal arithmetic (packed).

II—DATA MOVEMENT INSTRUCTIONS
Many custom instructions designed to ease task of simultaneously processing multiple lists.
Indirect and auto-incrementing addressing.

III PROGRAM MANIPULATION INSTR'S
Custom instructions for generating efficient loops.
Subroutine starting-address pool allows code sharing to save ROM bytes. 16-level subroutine nesting.
Three levels of priority interrupt.
LSI DMA chip has 8 priority levels, and allows 250k-bytes/sec data transfers.

IV PROGRAM STATUS MANIP. INSTR.
Bit setting and testing directly in RAM memory.

*Note: Rockwell is now concentrating its development work on the NMOS 6500. However, the firm will continue to support the PPS-8.

***HARDWARE SUPPORT:** Standard evaluation modules available for prototyping. Universal PPS Assemulator with System Analysis Module (SAM). Many PPS-family support chips.

***SOFTWARE SUPPORT:** Cross-assembler available on time-sharing network. Resident text editor, assembler and debug utility on Universal PPS Assemulator. Tutorial manuals.

8 BIT MOS

AVAILABILITY: Now for the 2650; before end of 1978 for "A" and "A-1" chip redesigns.
COST: $21.50 for 2650 CPU (100). 2650A version will be lower priced. Pricing for 2650A-1 not yet determined.
SECOND SOURCE: National Semiconductor, licensed, mask interchange.

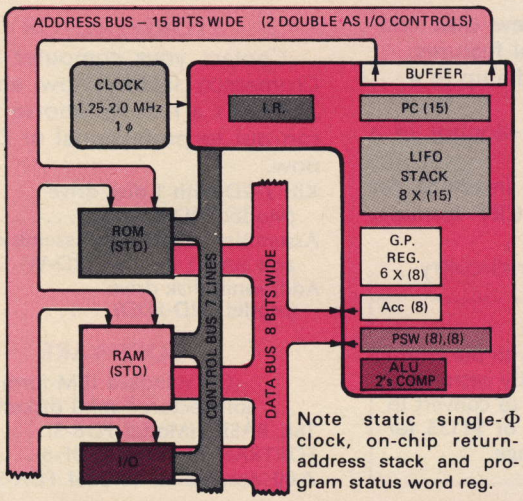
2650/A/A-1

When designed in 1973, this μP was ahead of its time. However, hardware implementation delays crippled sales. To gain market share Signetics is now investing heavily in the development of new support chips.

Signetics,
811 E. Arques Ave.,
Sunnyvale, CA 94086.
Phone (408)739-7700

HARDWARE

NMOS, depletion load, static, +5V, 500 mW, 40-pin DIP, single-phase external clock.



Note static single-Φ clock, on-chip return-address stack and program status word reg.

SOFTWARE

The 75 instructions are patterned after those found in minicomputers. Most take 2 or 3 machine cycles and are executed in 4.8 to 7.2 μsec for the 2650A (3 to 9 μsec for the 2650A-1).

I—DATA MANIPULATION INSTRUCTIONS
Add, Subtract and Logical with choice of 8 addressing modes: 1- Register, 2- Immediate, 3- Relative direct, 4- Relative indirect, 5- Absolute direct nonindexed, 6- Absolute indirect nonindexed, 7- Absolute direct indexed, 8- Absolute indirect indexed.

II—DATA MOVEMENT INSTRUCTIONS
Load and Store, with option of all 8 addressing modes. Any of the 7 GP registers can be assigned as index register by bits in the op code.
Buses can be 3-stated for DMA.

III — PROGRAM MANIPULATION INSTRUCTIONS
Branch on condition; branch to subroutine on conditions (with all relative and absolute addressing modes). All-in-one conditional branch instructions provide efficient loop housekeeping control. Single-level interrupts vectored by interrupt source to service routines.

IV PROGRAM STATUS MANIP. INSTR.
Sixteen-bit wide program status register has its own commands.

HARDWARE SUPPORT: Two Prototyping cards, two prototyping kits, 4k RAM card, "TWIN" development system. Support chips: 2651 USRT, 2652 multi-protocol, 2655 PIA, 2656 combo for 2-chip μC's.

SOFTWARE SUPPORT: "PIPBUG" ROM-based editor and loader, 16- and 32-bit Fortran IV assembler and simulator, plus 16- and 32-bit "PLμS" compiler.

You can now have the industry's finest microcomputer with that all-important disk drive

The professional-grade microcomputer for professionals

Shown with optional bench cabinet

YOU CAN GET THAT ALL-IMPORTANT SOFTWARE, TOO

Loading your programs and files will take you only a few seconds with the new Cromemco Z-2D computer.

You can load fast because the Z-2D comes equipped with a 5" floppy disk drive and controller. Each diskette will store up to 92 kilobytes.

Diskettes will also store your programs inexpensively—much more so than with ROMs. And ever so much more conveniently than with cassettes or paper tape.

The Z-2D itself is our fast, rugged, professional-grade Z-2 computer equipped with disk drive and controller. You can get the Z-2D with either single or dual drives (dual shown in photo).

CROMEMCO HAS THE SOFTWARE

You can rely on this: Cromemco is committed to supplying quality software support.

For example, here's what's now available for our Z-2D users:

CROMEMCO FORTRAN IV COMPILER: a well-developed and powerful FORTRAN that's ideal for scientific use. Produces optimized, relocatable Z-80 object code.

CROMEMCO 16K DISK BASIC: a powerful pre-compiling interpreter with 14-digit precision and powerful I/O handling capabilities. Particularly suited to business applications.

CROMEMCO Z-80 ASSEMBLER: a macro-assembler that produces relocatable object code. Uses standard Z-80 mnemonics.

ADVANCED CONTROLLER CARD

The new Z-2D is a professional system that gives you professional performance.

In the Z-2D you get our well-known 4-MHz CPU card, the proven Z-2 chassis with 21-slot motherboard and 30-amp power supply that can handle 21 cards and dual floppy drives with ease.

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- A disk bootstrap Monitor in a 1K 2708 PROM
- An RS-232 serial interface for interfacing your CRT terminal or teletype
- LSI disk controller circuitry

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Your Z-2 was designed with the future in mind. It can be easily retrofitted with everything needed to convert to a Z-2D. Only $935 kit; or $1135 for assembled retrofit package.

We're able to put all of this including a UART for the CRT interface on just one card because we've taken the forward step of using LSI controller circuitry.

STORE/FACTORY

Contact your computer store or Cromemco factory now about the Z-2D. It's a real workhorse that you can put to professional or OEM use now.

Kit: Z-2D with 1 disk drive (Model Z2D-K) . . . . . $1495.
Assembled: Z-2D fully assembled and tested (Model Z2D-W) . . . . $2095.
Additional disk drive (Model Z2D-FDD) . . . . . $495.

SOFTWARE

(On standard IBM-format soft-sectored mini diskettes)

16K BASIC (Model FDB-S) $95
FORTRAN IV (Model FDF-S) $95
Z-80 Assembler (Model FDA-S) $95

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For more information, Circle No. 38

8-BIT MOS | 16-BIT MOS

AVAILABILITY: Now.
COST: $134 for 3-chip CPU in 100 qty.
SECOND SOURCE: National Semiconductor possible. (W.D. has severed relations with DEC, and although the mini maker now manufactures the parts, it doesn't sell them at the device level.)

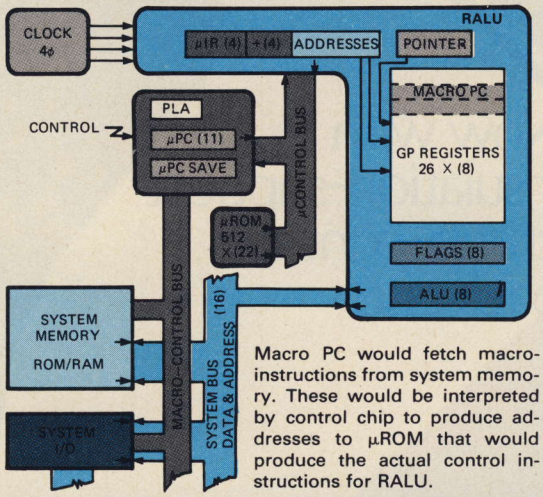
MCP-1600

Microprogrammable chip set builds 8- and 16-bit μP's with custom instructions (see NOTE, below).

Western Digital Corp.
3128 RedHill Ave.
Newport Beach, CA 92663
Phone(714)577-3550

HARDWARE

NMOS, 40-pin DIP, 3-chip CPU, needs ±5 and +12V. MCP-1600 is unprogrammed chip set; WD-16, preprogrammed set resembling LSI-11 from DEC in architecture and instructions.



Macro PC would fetch macro-instructions from system memory. These would be interpreted by control chip to produce addresses to μROM that would produce the actual control instructions for RALU.

HARDWARE SUPPORT: Development pc boards; 2-board CPU set is compatible with S-100 bus; microprogramming development system contains CPU, memory and writable control store. (Support effort has been cut back due to W.D.'s financial difficulties.)

SOFTWARE

Microinstructions operate in 500-nsec cycles. Four- and 8-bit op-codes allow machines of PDP-11/40 class to be attempted.

I—DATA MANIPULATION INSTRUCTIONS

The micro-instruction set includes decimal as well as binary arithmetic. It will operate with single bytes as well as double bytes so 8-bit machines can also be emulated.

II—DATA MOVEMENT INSTRUCTIONS

Developed by user, by selecting sequences of micro-instructions and encoding these in the μROM.

III—PROGRAM MANIPULATION INSTR'S

Developed by user.

IV—PROGRAM STATUS MANIP. INSTR.

Developed by user.

Note: MCP-1600 available from Western Digital in two macro versions: the MP-1600, which is similar to the Data General Eclipse; and the WD-1600, which has a unique instruction set aimed at the hobby market.

SOFTWARE SUPPORT: Assembler, simulator, editor and debugger run on disc-based DEC PDP-11/05 system. Single-user floppy-disc based software offered in source form without higher-level languages.

8-BIT MOS

AVAILABILITY: Now.
COST: $16.25 for 2.5 MHz version of Z80 , $25 for 4 MHz unit in 100 qty.
SECOND SOURCE: Mostek, NEC and Sharp.

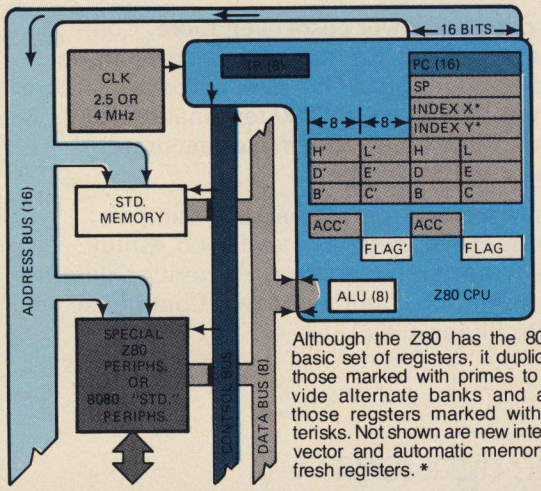
Z80/Z8/Z8000

Superset of 8080; adds hardware and software features. Not pin-for-pin compatible with 8080, but can use 8080 software and peripherals (though to do so would not take full advantage of Z80's capabilities).

Zilog
10460 Bubb Rd.
Cupertino, CA 95014
Phone(408)446-4666

HARDWARE

NMOS, Static, single-phase clock, +5V only. TTL-compatible I/O. Automatically refreshes dynamic RAM's. Military temp and plastic pkg units available. Z8 will be 1-chip version with 96 bytes RAM, 2k bytes ROM, four 8-bit I/O ports, 2 timer/counters and serial I/O port; Z8000, a 16 bit machine.



Although the Z80 has the 8080's basic set of registers, it duplicates those marked with primes to provide alternate banks and adds those regsters marked with asterisks. Not shown are new interrupt vector and automatic memory refresh registers. *

HARDWARE SUPPORT: Wide range, from evaluation pc boards to disc-based development system with real-time in-circuit emulation capability. Disc operating software includes the ability to edit files of any size.

SOFTWARE

Totally 8080A software compatible. Features 50 additional instructions plus many more registers. Two banks of GP registers allow fast response via bank switching.

I—DATA MANIPULATION INSTRUCTIONS

8-bit arithmetic and logicals.
16-bit arithmetic BCD add and subtract.
Nine types of rotate and shift directly on any register or memory location.
Can set, reset or test bit in any register or memory location.

II—DATA MOVEMENT INSTRUCTIONS

8- or 16-bit register or memory loads.
Two index registers allow indexed addressing.
Extensive memory-block move search commands.

III—PROGRAM MANIPULATION INSTR'S

Uses 16-bit stack pointer with LIFO stack with RAM memory. Relative jump capability. Interrupt capability with 3 types of selectable response.

IV—PROGRAM STATUS MANIP. INSTR.

Seven flag bits, including arithmetic and overflow, can be stored and tested.

* Support chips include peripheral interface (PIO), timer (CTC) and DMA which provide daisy chained vectored priority interrupt for CPU.

SOFTWARE SUPPORT: Macro-assembler with relocatable assembler, linking loader, file maintenance programs, and resident BASIC, COBOL, FORTRAN and PL/Z. (Latter can mix assembly and higher-level "system" language statements.)

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For more information, Circle No. 39

12-BIT CMOS

AVAILABILITY: Now.
COST: $15 in 100 qty for commercial CPU; $16.50 for industrial version; $52.80 for military-grade chip.
SECOND SOURCE: Harris licensed.

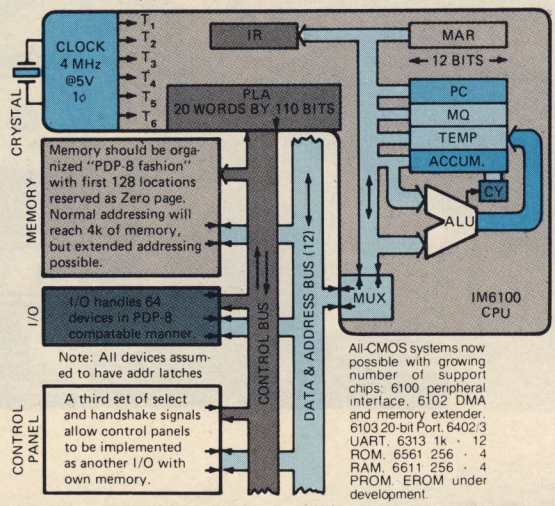
IM 6100

Very similar to popular DEC PDP-8/E, but differs in timing and doesn't use patented Unibus structure.

Intersil, Inc.
10900 N. Tantau Ave.
Cupertino, CA 95014
Phone(408)996-5000

HARDWARE:

Single-chip CPU in low-voltage CMOS (no guard rings). 4-11V PS. Operates dc to 8 MHz with upper limit proportional to supply voltage (speed increases 2½ times as voltage is doubled). Dissipation is less than 10 mW at 5V, 4 MHz.



SOFTWARE:

Executes PDP-8/E instructions with 5 μsec memory-to-accumulator add at 5V supply; 2.5 μsec add at 10V supply. PDP-8 family has been around so long, so many routines exist to circumvent its shortcomings.

I—DATA MANIPULATION INSTRUCTIONS

Basic, rather primitive selection of just a two's-complement binary add and a complementation for subtraction. Decimal arithmetic through software correction.

II—DATA MOVEMENT INSTRUCTIONS

Addresses 4k locations via paging method where pages are 128 locations long (instead of the 256 common now in μP's). No literal mode of "addressing," as that was not common when PDP-8 originally was developed some 15 years ago. Magnetic core memories rather than ROM's were used then for nonvolatility.

III—PROGRAM MANIPULATION INSTR'S

Subroutine returns accomplished via more primitive approach of using software step to save return address at top of subroutine, rather than modern use of hardware LIFO's or stack-pointer registers. Skip-type instructions used for conditional branching.

IV—PROGRAM STATUS MANIP. INSTR.

No status register, but link or carry flip-flop can be set, cleared or tested by software.

HARDWARE SUPPORT: Both Intersil and Harris offer board- and box-level prototyping system. Intersil uses the name "Intercept;" Harris, the name "SIMON."

SOFTWARE SUPPORT: Extended package contains loaders, assemblers, editors, debuggers and floating point arithmetic. Also: FOPAL cross assembler and FOCAL interpreter. Can use DECUS library and DEC service programs.

16-BIT MOS

AVAILABILITY: Now.
COST: mN601 CPU is $75 in 100 qty.
SECOND SOURCE: None announced.

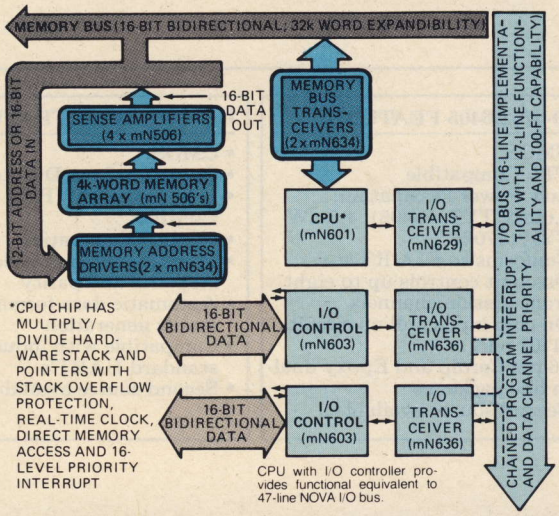
microNOVA

Designed around popular NOVA 16-bit, multiple-register minicomputer architecture, the microNOVA chip set consists of the mN601 CPU, mN606 4k RAM, mN603 I/O controller, plus buffer elements.

Data General Corp.
Southboro, MA 01772
Phone(617)485-9100

HARDWARE

NMOS, silicon-gate, dynamic CPU needs ±5 and +15V. On-chip 2-phase clock uses external 8.33 MHz xtal. Refresh control for dynamic RAM's.



SOFTWARE

Full compatibility with NOVA software. Accumulator load takes 2.9 μsec; add, 2.4 μsec.

I—DATA MANIPULATION INSTRUCTIONS

Hardware multiplication and division.
Single-word instructions can execute arithmetic or logical operations from any pair of registers, and can also shift, test and store the result.

II—DATA MOVEMENT INSTRUCTIONS

Single-word instructions move data between RAM locations and any register. Multiple addressing modes include absolute, relative, indexed, deferred and auto-increment/decrement. Two of the multiple accumulators can be used as index registers.

III—PROGRAM MANIPULATION INSTR's

Programmed priority interrupts to 16 levels.
Hardware stacks facilitate programming of reentrant and recursive subroutines.
SAVE instruction allocates new stack frame, while simultaneously storing all CPU registers.

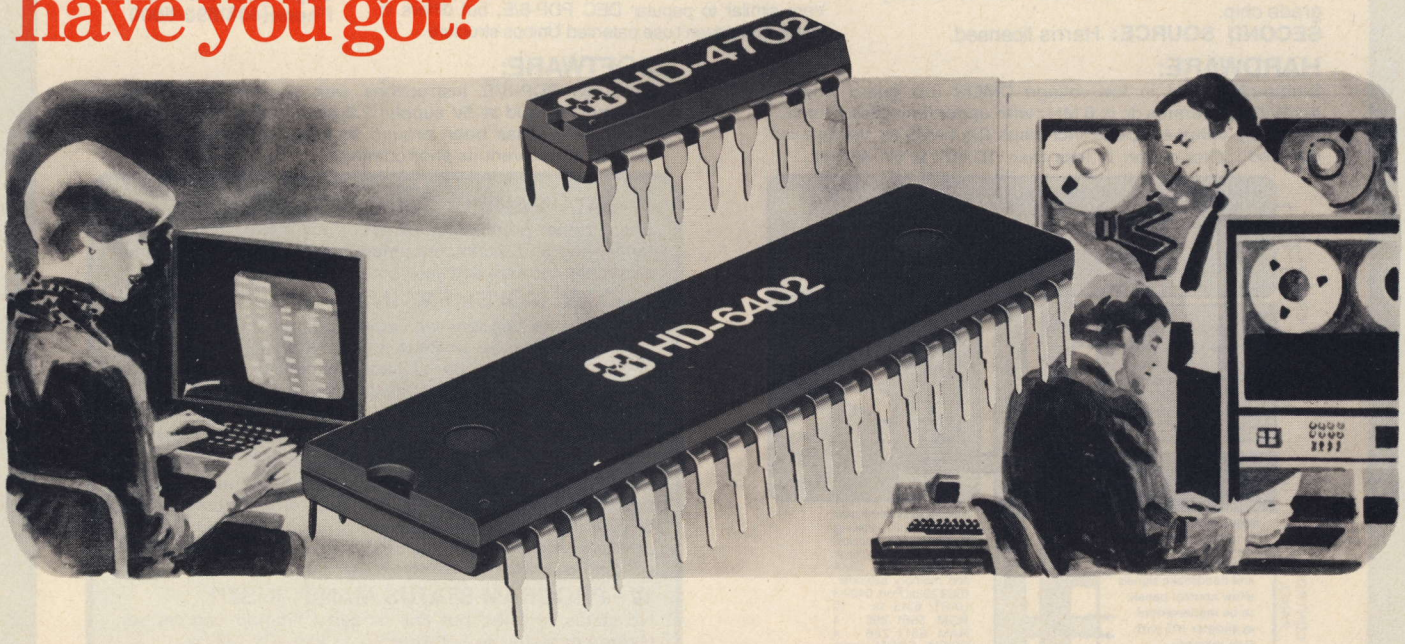
IV—PROGRAM STATUS MANIP. INSTR.

Carry bit, interrupt enable bit, real-time clock enable and request bits, stack-overflow request bit.

HARDWARE SUPPORT: Wide range, from single-board μC with up to 4k words RAM, to stand-alone mini, to development system with diskette-based Disc Operating System (DOS).

SOFTWARE SUPPORT: Wide range, including DOS with text editor, FORTRAN IV compiler, assembler, symbolic debugger and relocatable loader; real-time operating system and extensive application library.

Put our new UART and BIT RATE GENERATOR together and what have you got?



The first programmable CMOS Communications System.

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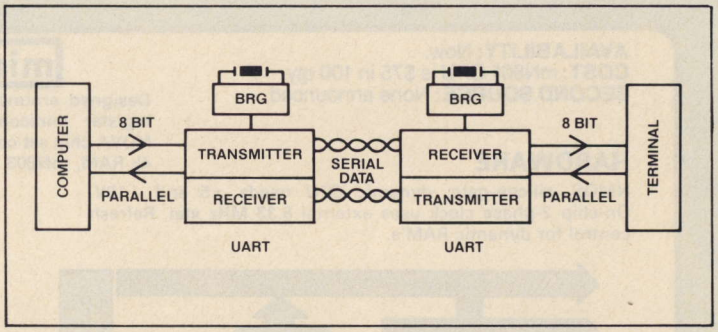
For full details, call the Harris Hot Line, or write: **Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901.**



HD-4702/6405 FEATURES

- CMOS
- TTL Compatible
- Low Power Dissipation: 4.0mW TYP. (6405); 4.5mW TYP. (4702)
- Conforms to EIA RS-404
- One unit controls up to eight transmission channels
- On-chip input pull-up circuit (4702 only)
- 16 pin Cerdip and Epoxy dual-in-line packages
- Second source available

HD-6402/6402A FEATURES

- CMOS
- Operation from D.C. to 4.0MHz
- Low power—TYP. 10 mW @ 2.0MHz
- 4V to 11V operation
- Programmable word length, stop bits and parity
- Automatic data formatting and status generation
- Compatible with industry standard UART's
- Second source available

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CMOS | BIPOLAR

AVAILABILITY: Now.
COST: $30 to $50 per 4-bit-slice system, 100 qty.
SECOND SOURCE: Signetics.

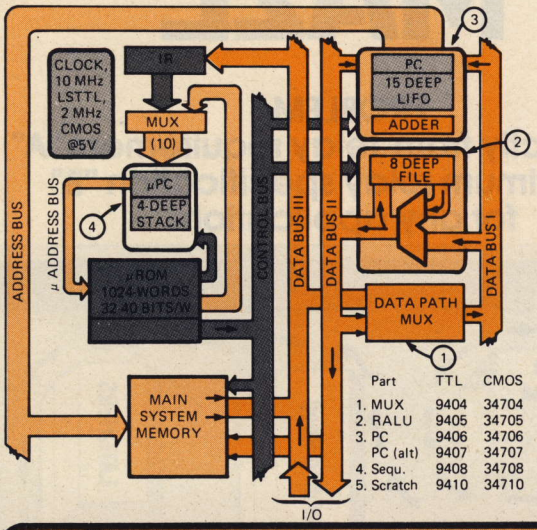
MACROLOGIC

Four-bit-slice building blocks for microprogrammable computers. Available in both Schottky-TTL and CMOS, with some parts using I^2L technology.

Fairchild Semiconductor
464 Ellis St.
Mt. View, CA 94040
Phone(415)962-3541

HARDWARE:

Low-power Schottky TTL has 4-nsec gate delays. CMOS version has "zero" standby power and 20-mW operating power/part at 2-MHz clock. Mil temp. range on both.



Part	TTL	CMOS
1. MUX	9404	34704
2. RALU	9405	34705
3. PC	9406	34706
PC (alt)	9407	34707
4. Sequ.	9408	34708
5. Scratch	9410	34710

HARDWARE SUPPORT: Development system based on emulation of NOVA-1200. Application notes show how to construct various types of programs. New parts being added to family.

SOFTWARE:

User defines his own instruction set by microprogramming the μROM. Parts will respond to the following type commands.

I—DATA MANIPULATION INSTRUCTIONS
Arithmetic and logic. Increment and decrement. Logic shift, left and right. Bit and byte masking. Sign extension.

II—DATA MOVEMENT INSTRUCTIONS
Uses register transfer module concept.
Any device can be designated as source or destination of data.
User can implement variety of addressing modes, including indexing.

III—PROGRAM MANIPULATION INSTR'S
Jump
Call Subroutine
Conditional and subroutine branch
4-deep stack for micro-subroutine nesting.
User can have stack with PC, or (via stack pointer register) he can put stack in main memory, depending on which of two PC parts he uses (9406 or 9407).

IV—PROGRAM STATUS MANIP. INSTR.
Carry, overflow, negative, zero and PC stack full and empty (on 9406).

SOFTWARE SUPPORT: Microprogram assembler available through purchase or timeshare.

16-BIT MOS

AVAILABILITY: Now.
COST: $30 in 100 qty for CP-1600; $8 for 1610.
SECOND SOURCE: EM&M SEMI and ITT Semiconductor.

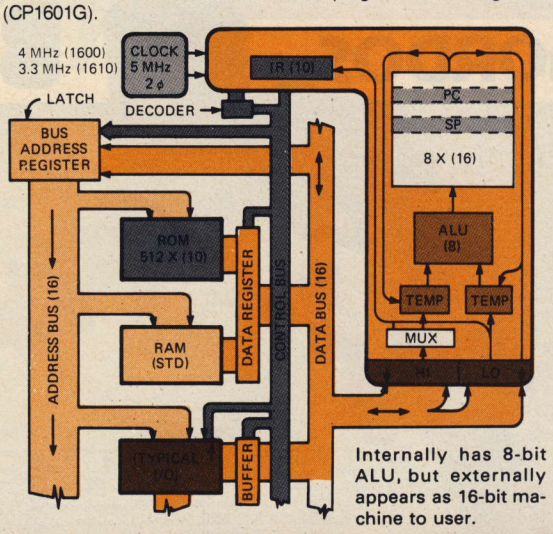
CP-1600/1610

Aimed at real-time control automation. Yield problems lowered 1600's clock spec from 5 MHz to 4 MHz. (The 1610 operates at 3.3 MHz.)

General Instrument Corp.,
600 W. John St.,
Hicksville, NY 11802.
Phone (516) 733-3000

HARDWARE

NMOS; metal gate; uses +12, +5 and −3V supplies; 40-pin DIP. Under development are an enhanced version that will more closely resemble PDP-11 mini and variant for programmable TV games (CP1601G).



Internally has 8-bit ALU, but externally appears as 16-bit machine to user.

HARDWARE SUPPORT: Prototyping pc board. Also, a complete mini with 8k-word memory and peripheral controllers ($3500). Growing number of support chips available.

SOFTWARE

68 instructions execute in 2-6 μsec (2.4-7.2 μsec for 1610). 16-bit add from memory takes 4 μsec (4.8 for 1610). Instructions patterned after PDP-11, but no indexing mode.

I—DATA MANIPULATION INSTRUCTIONS
Add, subtract and logicals.
Double-precision add, subtract and logicals.
Arithmetic and logical shift (one and two bits).

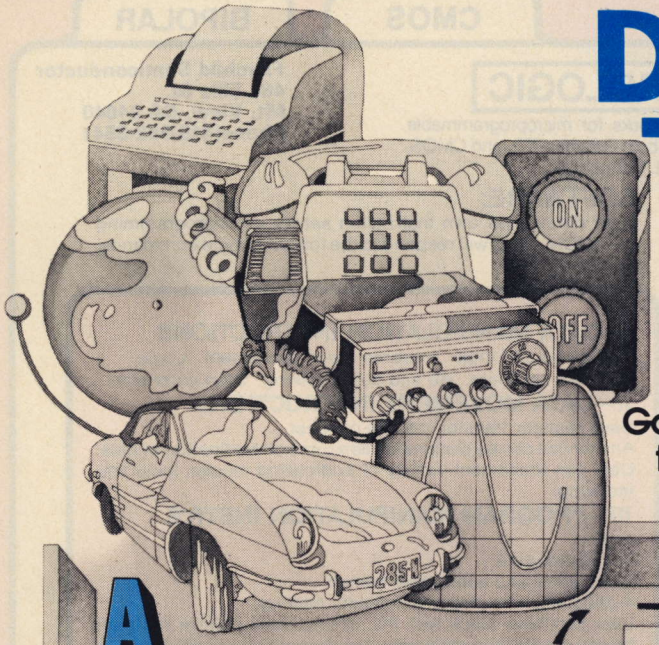
II—DATA MOVEMENT INSTRUCTIONS
After manner of PDP-11, uses 2-address instructions to treat 8 GP registers on CPU as accumulators.
Can directly address first 1024 external memory locations.
Treats I/O as memory (PDP-11 architecture).

III—PROGRAM MANIPULATION INSTR'S
Conditional Branches patterned after PDP-11, with address program-counter relative (PC± 1024).
Special external sense inputs.
Priority Interrupt with self-identifying vectors.
No Index register per se but can achieve function with GP registers.

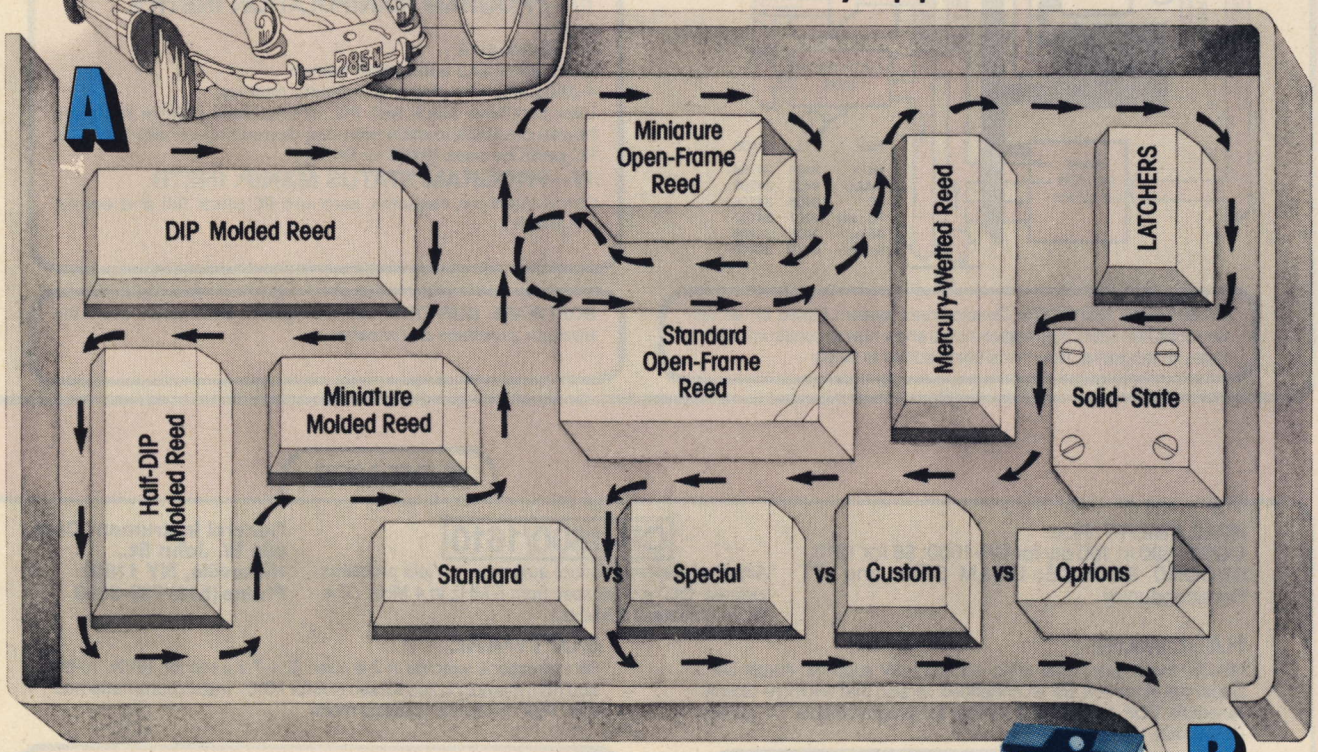
IV—PROGRAM STATUS MANIP. INSTR.
Can save and reload four status bits.

SOFTWARE SUPPORT: Cross-assembler. Debug, simulator, diagnostics and subroutine library. Also, relocatable linking loader, text editor and SUPER ASSEMBLY high-level language.

DON'T FIGHT THE RELAY MAZE



PROBLEM:
Go directly from relay requirement "A" to optimum relay specification "B" for any application.



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Open-Frame Reed Relays	RR406
Solid-State Relays	SS502
Dry and Mercury Reed Switches	RS125

GORDOS

Gordos Corporation, 250 Glenwood Ave., Bloomfield, N.J. 07003 • Telephone: (201) 743-6800 • TWX: 710-994-4787

For more information, Circle No. 41

16-BIT MOS

AVAILABILITY: Volume now for PACE; samples now for 8900.
COST: $26 in 100 qty for PACE; $16 for INS8900. Price expected to drop to $10 for 8900 in volume.
SECOND SOURCE: None.

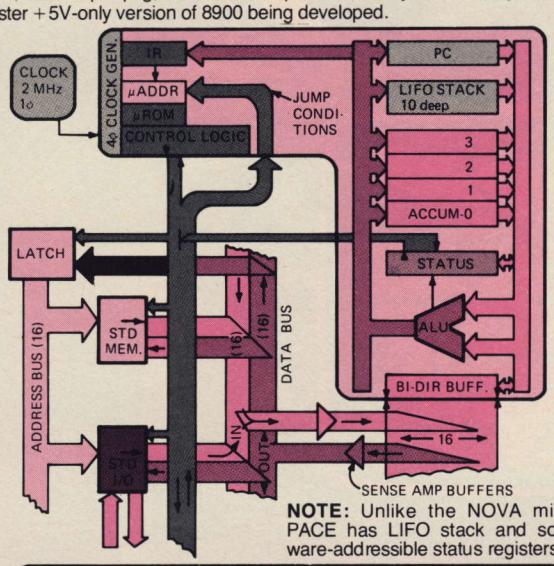
8900 (PACE)

National Semiconductor Corp.
2900 Semiconductor Dr., M/S 470
Santa Clara, CA 95051
Phone(408)737-5000

Similar to NOVA-1200 in architecture, but with instruction set suited to μC applications. Has many unassigned op codes, so much potential growth left.

HARDWARE

PACE is PMOS, silicon gate. New NMOS 8900 uses +5, +12, and −8V, has 40-pin pkg, can drive low-power Schottky TTL directly. Faster +5V-only version of 8900 being developed.



NOTE: Unlike the NOVA mini, PACE has LIFO stack and software-addressible status registers.

HARDWARE SUPPORT: Board assemblies for prototyping and short-run production. Development systems range from $585 LCDS to $5000 unit with 8k of memory.

SOFTWARE

All 45 instructions are single word length; most execute in 10 μsec. Rich option fields in each instruction provide over 300 combinations.

I — DATA MANIPULATION INSTRUCTIONS
Add, subtract and logicals (hardware multiply and divide are planned for future version). N-bit shifts and rotates. Efficient decimal-adjust instruction allows much better performance on decimal number than IMP-16.

II—DATA MOVEMENT INSTRUCTIONS
Indexing using any of four accumulators.
Can do serial I/O through jump condition inputs and flag outputs up to 4800 baud.

III — PROGRAM MANIPULATION INSTR'S
Skip and branch. Increment and skip if zero. Push and pull 10-level stack. Five levels of interrupts, with on-chip prioritized vectoring.

IV—PROGRAM STATUS MANIP. INSTR.
Full 16-bit status register has not only the usual indications of ALU results but space left over for user-definable flags.

SOFTWARE SUPPORT: FORTRAN-IV cross-assembler that runs on ≥16-bit computers ($495); BASIC interpreter that needs 8k memory system ($100); and resident 4k and 8k packages that include assemblers, loaders, debug and utilities ($200).

16-BIT MOS

AVAILABILITY: Now.
COST: $128 in 25 qty for 5-chip set.
SECOND SOURCE: None.

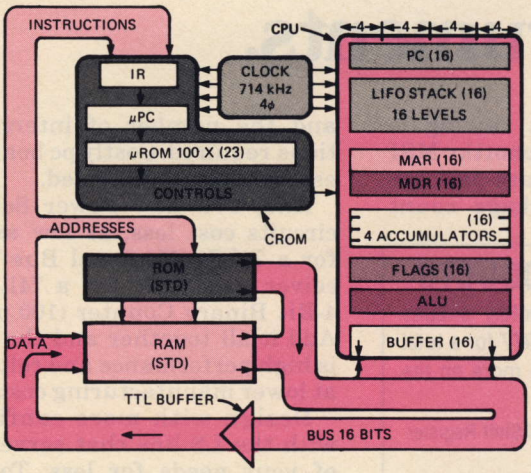
IMP-16

National Semiconductor Corp.
2900 Semiconductor Dr., M/S 470
Santa Clara, CA 95051
Phone(408)737-5000

Machine is based on 4-bit "RALU" slices plus microprogramming CROM. It will become obsolete when NMOS single-chip PACE is introduced.

HARDWARE:

PMOS slices for CPU and CROM, with rest of μP function filled in with TTL.



Slice approach plus microprogramming gives customers freedom to reconfigure hardware and software. (I/O not shown.)

HARDWARE SUPPORT: Functional computer on a pc board. Console-level "microcomputers."

SOFTWARE:

43 instructions for basic 16-bit full-sized version executed in 5-10 μsec. Similar to Data General Nova 1200 mini.

I—DATA MANIPULATION INSTRUCTIONS
Basic CROM provides conventional Add, Subtract and Logicals.
Additional CROM provides powerful instructions: multiply and divide and double-precision operations.

II—DATA MOVEMENT INSTRUCTIONS
Direct addressing in three modes: base page, PC relative and Indexed.
Indirect addressing to full 65k of memory.
Additional CROM will allow block transfer, I/O and memory search.

III—PROGRAM MANIPULATION INSTR'S
Skip and Branch.
Increment and skip-if-zero.
Push and pull 16-level stack.
Multi-level interrupt.

IV—PROGRAM STATUS MANIP. INSTR.
Can manipulate status flag bits and move 16-bit flag register as a whole.

SOFTWARE SUPPORT: Cross-assemblers and high-level language (SM/PL). Also, self-assembler, debug, timeshare, diagnostic, etc.

The new design standard. Low Power Schottky. From the leader. Texas Instruments.

Now there are 165 Low Power Schottky functions available from the leader, Texas Instruments. The broadest line in the industry... SSI, MSI and LSI circuits for every low-power, high-performance application... military systems, data processing, telecommunications, process control, with or without microprocessors. You'll find TI Low Power Schottky circuits provide greater reliability at a lower cost in less space with less power.

All of TI's innovative 54LS/74LS circuits feature typical speeds to 6 ns/gate with power dissipation of less than 2 mW. In fact, power requirements are 80% less than for standard TTL logic. Less heat is generated. Less heat sinking is required. Low Power Schottky MSI and LSI circuits increase package density reducing package count and the number of interconnections required. Costly pc board real estate is thus minimized.

And, TI's Low Power Schottky circuits cost less, as low as $1.40 for a 74LS245N Octal Bus Transceiver and $0.69 for a 74LS669N 4-Bit Binary Counter (100 pieces). Add it all together and the result is high performance and reliability at lower manufacturing costs.

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23 new Low Power Schottky circuits have been introduced in 1977 for a total of 165 since 1971... with more on the way.

- SN54LS/74LS673 16-Bit POSI Shift Register with Storage
- SN54LS/74LS674 16-Bit PISO Shift Register
- SN54LS/74LS322 8-Bit Shift Register w/Sign Extend
- SN54LS/74LS173 4-Bit D-type Register, 3-State

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For more information, Circle No. 42

BIPOLAR

AVAILABILITY: Now.
COST: $395 in 100 qty including software.
SECOND SOURCE: To be announced.

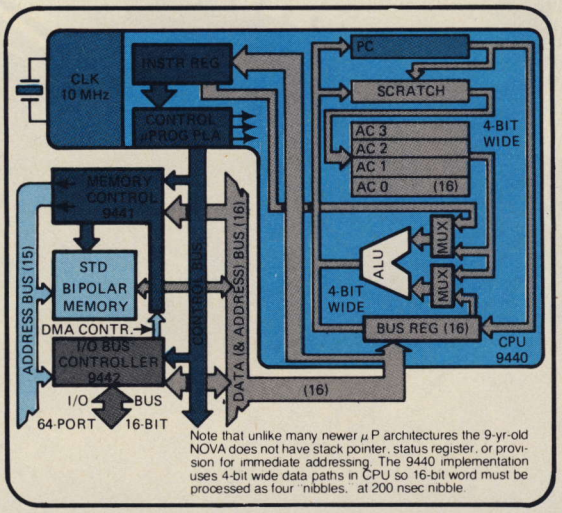
9440

Offers performance of NOVA-1200 mini in ambitious, state-of-art I²L/TTL CPU and support chips. (9440 is subject of suit against Fairchild by Data General.)

Fairchild Semiconductor
464 Ellis St.
Mt. View, CA 94040
Phone(415)962-5011

HARDWARE

I²L technology keeps CPU chip size to 182 × 189 mils. 930 mW (180 mA at 1 V for I²L, 150 mA at 5V for TTL). 40-pin DIP.



Note that unlike many newer μP architectures the 9-yr-old NOVA does not have stack pointer, status register, or provision for immediate addressing. The 9440 implementation uses 4-bit wide data paths in CPU so 16-bit word must be processed as four "nibbles," at 200 nsec nibble.

HARDWARE SUPPORT: Prototyping board and development system are expected.

SOFTWARE

Executes all NOVA-1200 instructions at full "bipolar" speed. Takes only 1.5 μsec for memory reads and writes.

I — DATA MANIPULATION INSTRUCTIONS
ALU instructions particularly powerful because code's multiple fields allows shifts, tests, etc. to also be performed in the same instruction that does arithmetic or logical. Hardware multiply/divide by external 9443 support chip (not shown).

II — DATA MOVEMENT INSTRUCTIONS
Eight addressing modes: zero page direct and indirect, PC-relative direct and indirect, indexing (via AC 2 and AC 3) direct and indirect. Many I/O instructions perform manipulations on I/O as well as basic data movement.

III — PROGRAM MANIPULATION INSTRUCTIONS
Decisions via conditional SKIP instructions. Subroutines must be software implemented using AC 3; stacks must be formed in memory using software and AC 2 and AC 3.

IV — PROGRAM STATUS MANIPULATION INSTRUCTIONS
No status register, per se, but equivalent functions built into ALU instruction fields.

SOFTWARE SUPPORT: Five items initially: system diagnostics, bootstrap loader, "FIREBUG" interactive program entry and debug monitor, stand-alone text editor and stand-alone business BASIC. In 1978 expect disc-based FORTRAN compiler with string operators and macro assembler.

BIPOLAR

AVAILABILITY: Now.
COST: $8.80 for 2-bit slice in 100 qty. (A 16-bit kit with 26 parts costs $210 in 100 qty.
SECOND SOURCE: Signetics.

3000

Flexible bit-slice structure suited for high-speed applications including computers and controllers with word widths ranging from 2 to 64 bits.

Intel Corp.
3065 Bowers Ave.
Santa Clara, CA 95051
Phone (408) 987-8080

HARDWARE

Schottky-TTL 2-bit wide slices and 9-bit microprogram sequencer. Use +5V power supply. Standard bipolar PROM's available.

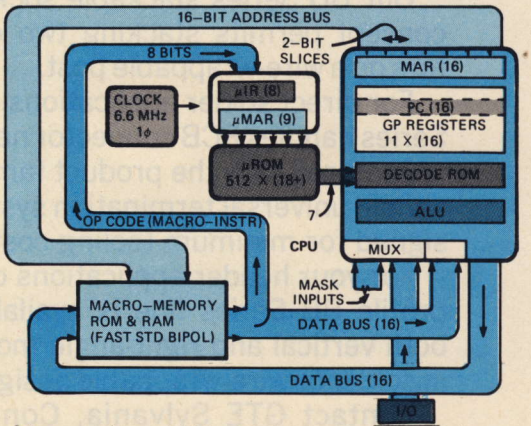


Diagram shows 16-bit minicomputer constructed from 3000-Series parts. Although slices are only two bits wide, they include a large number of parallel paths for high processing throughput.

HARDWARE SUPPORT: Available in 40-pin DIP's or with prototyping pc board. MDS-800 system ($3950); with ICE-30 ($850) and ROM simulator ($800).

SOFTWARE

CPU slices respond to 40 micro-instructions, taking 150 nsec/cycle on systems level. Hardware's 3 input and 2 output CPU buses allow fast 1-cycle processing of memory and I/O data. Good at bit testing for controller use.

I—DATA MANIPULATION INSTRUCTIONS
Arithmetic and logic.
Increment/decrement.
Shift left and right.
Swap bytes.
Bit testing.

II—DATA MOVEMENT INSTRUCTIONS
Developed by user using the micro-instructions to assemble desired macro-instructions.

III—PROGRAM MANIPULATION INSTR'S
Developed by user.

IV—PROGRAM STATUS MANIP. INSTR.
Developed by user.

NOTE: User codes μROM to define the regular or "macro" instruction set for each application. For example, Signetics emulates 8080 with 3000-Series parts.

SOFTWARE SUPPORT: CROMIS, cross-microassembler available in FORTRAN-IV tape form ($1250) or on several timesharing networks.

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8-BIT MOS | 16-BIT MOS | BIPOLAR

TMS9900/9980/9940, SBP9900

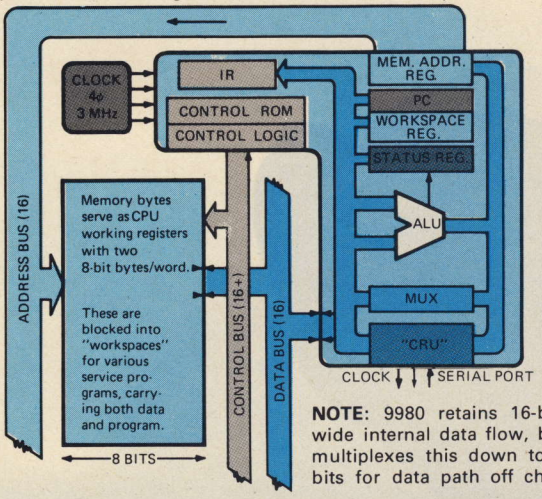
Memory-to-memory architecture (no accumulator or working registers in CPU) allows multiprocessing and rapid context switching upon interrupt or subroutining. All machines are 16 bits in CPU. One-chip 9940 μC makes extensive use of 1-bit serial port, includes ROM and RAM.

Texas Instruments, Inc.
MOS Products Div.
Houston, TX 77001
Phone (713) 494-5115

AVAILABILITY: First qrt '78 for 9940, now for others.
COST: In 100 qty: TMS9900, $70.58; 9980, $30.62; 9940 EPROM version, $90; SBP9900, $193. Masked-ROM 9940 is $6 in 10k qty.
SECOND SOURCE: AMI licensed TMS 9900/9980/9940. None for SBP-9900.

HARDWARE

TMS units: NMOS, silicon gate, ±5V and +12V, 64 pins for 9900, 40 pins for 9980 and 9940. SBP9900: I²L, single supply, 1000:1 speed × power selectable, single static clock, −55 to +125°C operation.



NOTE: 9980 retains 16-bit-wide internal data flow, but multiplexes this down to 8 bits for data path off chip.

SOFTWARE

Minicomputer set of 69 instructions (58 for 9940).

I—DATA MANIPULATION INSTRUCTIONS
Binary arithmetic including multiply and divide. Logicals and shifts. Can operate on words, bytes or bits.

II—DATA MOVEMENT INSTRUCTIONS
Addressing first chooses the "workspace" in memory that will contain the 16 GP registers used by instructions. This takes extra step, but allows rapid, easy context switching between a large number of alternate register groups. Information in workspaces can be left intact when computer switches tasks, allowing different tasks to be processed concurrently.

III—PROGRAM MANIPULATION INSTR'S
Some unique instructions due to memory-to-memory architecture. However, not difficult to understand. Can do indexing. Signed, relative type of precision jumps (branches). Sixteen levels of priority-vectored interrupt, speeded by the context switching. (Upon interrupt, machine switches to the service workspace.)

IV—PROGRAM STATUS MANIP. INSTR.
The 16-bit long status word contains usual ALU results indicator bits, plus extended mode set bit and four status code bits that set priority level allowed for interrupt.

HARDWARE SUPPORT: "AMPL" development system is floppy-disc based; PX990, cassette-based. Evaluation cards, modules and I/O peripherals. Tektronix 8001/8002 has TMS-9900 capability.

SOFTWARE SUPPORT: Assemblers and simulators in batch form or through timeshare networks; transportable ANSI Fortran assembler and simulator; PL/9900, Fortran and BASIC languages. Program library offered.

BIPOLAR

AM 2900

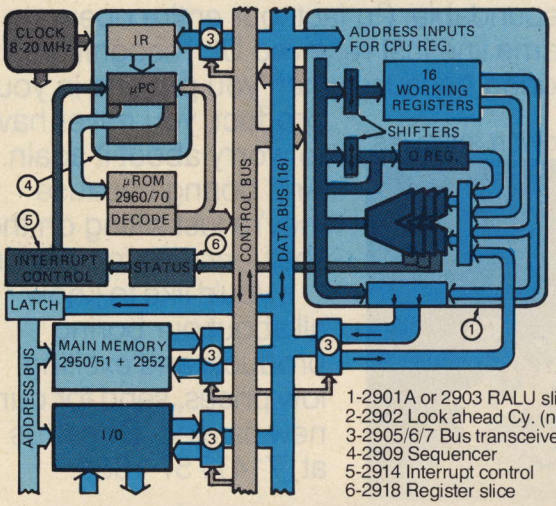
Popular family of low-power Schottky-TTL LSI devices aims at microprogrammable computers. New 2903 RALU slice is an enhanced 2901A, with features suited to arithmetic processing.

Advanced Micro Devices
901 Thompson Pl.
Sunnyvale, CA 94086
Phone (408) 732-2400

AVAILABILITY: Now for most parts.
COST: $14.70 for 2901A in 100 qty; pricing for 2903 not yet established.
SECOND SOURCE: Motorola, Raytheon and Sescosem, licensed. Also, Signetics, National, Fairchild, MMI and NEC.

HARDWARE

Classical computer architecture partitioned into MSI and LSI building blocks of the TTL type, but with fast (65 nsec) cycle.



1-2901A or 2903 RALU slices
2-2902 Look ahead Cy. (not shown)
3-2905/6/7 Bus transceivers
4-2909 Sequencer
5-2914 Interrupt control
6-2918 Register slice

SOFTWARE

User defines macroinstruction set by programming μROM. Parts respond to following instructions within 1 clock cycle (50-125 nsec); 16-bit RR add takes 145 nsec.

I — PROGRAM STATUS MANIPULATION INSTRUCTIONS
ALU performs three arithmetic operations on two operands and five logical functions.
Shifting networks can be used with add instruction for efficient multiplication and division.

II—DATA MOVEMENT INSTRUCTIONS
The 16 working registers in RALU RAM can be addressed two at a time for simultaneously supplying the two operands to the ALU.

III—PROGRAM MANIPULATION INSTR'S
Defined by user via microcode.
All modern modes of addressing should be possible.

IV—PROGRAM STATUS MANIP. INSTR.
Carry, overflow, zero and negative status outputs.

Note: In addition to the 2901A and 2903 RALU slices, the 2900 family includes the 2913 interrupt expander, 2919 1 × 2 port register; 29704/05 64-bit, 2-port RAM's; 29720/21 256-bit RAM's; 29750/51 256-bit PROM's; 29803 16-way branch controller for 2909; 29811 instruction controller for 2911; and N8X02 (Signetics) controlled-store sequencer.

HARDWARE SUPPORT: "System-29" development system with CRT and dual floppy discs ($24,950); microprogramming learning and evaluation kit ($289).

SOFTWARE SUPPORT: AMDASM microprogram assembler is available in 3 forms: timeshare, floppy disc for Intel MDS-80 and resident in AMD System-29.

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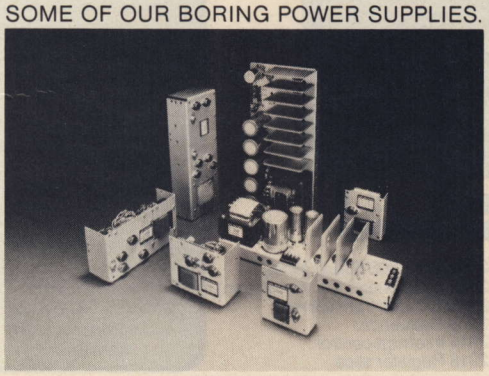

acdc electronics

401 Jones Road, Oceanside, California 92054

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AVAILABILITY: Now.
COST: 6701 is $26.15/slice in 100 qty; 5701, $53.30/slice.
SECOND SOURCE: ITT licensed.

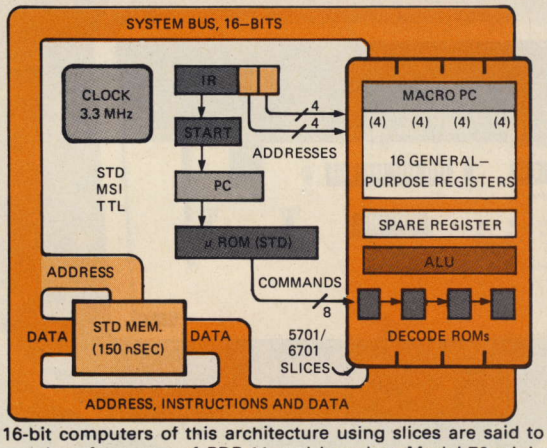
5701/6701

4-bit slice of ALU/Register portion of CPU that can be used to build computers 4 to 64 bits wide. Executes microinstructions.

Monolithic Memories Inc.,
1165 E. Arques Ave.,
Sunnyvale, CA 94086.
Phone (408)739-3535

HARDWARE

Schottky TTL. 5701 MIL version operates from −55 to +125°C at +5V ±10% power supply. 40-pin package.



16-bit computers of this architecture using slices are said to equal performance of PDP-11 and Interdata Model-70 minis with much reduced parts counts (50 vs. 200 or better).

HARDWARE SUPPORT: New 8 × 8 biopolar multiplier (67558/57588) costs $64/$110 in 100 qty. Under development is 16 × 16 multiplier (67516/57516). MMI now turning new-product efforts to second sourcing 2901 family, but will continue to support 6701/5701.

SOFTWARE:

Slices will respond to 32 microinstructions within 200 nsec (6701), doing complete on-chip register operations (longer with multiple slices).

I—DATA MANIPULATION INSTRUCTIONS

Arithmetic, logic and shifting

II—DATA MOVEMENT INSTRUCTIONS

Two-address capability due to double addressing of the 16 on-chip general-purpose registers (some of which may have to be dedicated to PC, etc.).

III—PROGRAM MANIPULATION INSTR'S

Jump, subroutine call and interrupt would be achieved by user via external microprogramming function.

IV—PROGRAM STATUS MANIP. INSTR.

ALU/Register slices have carry, overflow and zero outputs.

SOFTWARE SUPPORT: "Microaid" FORTRAN cross-assembler available for 16- and 32-bit machines and on NCSS timesharing system.

AVAILABILITY: Now for the 10800-10808.
COST: $30 per slice in 100 qty. for 10800.
SECOND SOURCE: Possibly Fairchild.

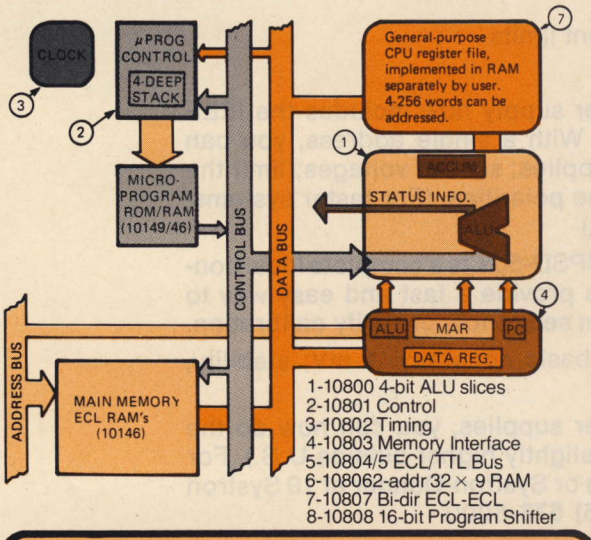
10800

Four-bit-slice building blocks for high-performance computers, controllers and communications processors. Compatible with ECL 10k family.

Motorola Semiconductor Products Div.
5005 E. McDowell Rd.
Phoenix, AZ 85008
Phone (602) 244-6900

HARDWARE

Bipolar ECL using −5.2 and −2.0V supplies. Package has 48 staggered pins that take up same area as 24-pin pkg. Can be pipelined for maximum speed.



HARDWARE SUPPORT: On-line demonstrator system in conjunction with 6800 EXORciser.

SOFTWARE

Microprogramming is used to meet requirements of any processor's instruction set. Cycle time is approx 100 nsec.

I—DATA MANIPULATION INSTRUCTIONS

Arithmetic including high-speed hardware BCD in ALU.
The 10803 includes an additional binary ALU.
Shifts, both left and right; both logical and arithmetic.

II—DATA MOVEMENT INSTRUCTIONS

The 10803 memory interface allows paged and associative addressing, which can prove useful for virtual-memory schemes.

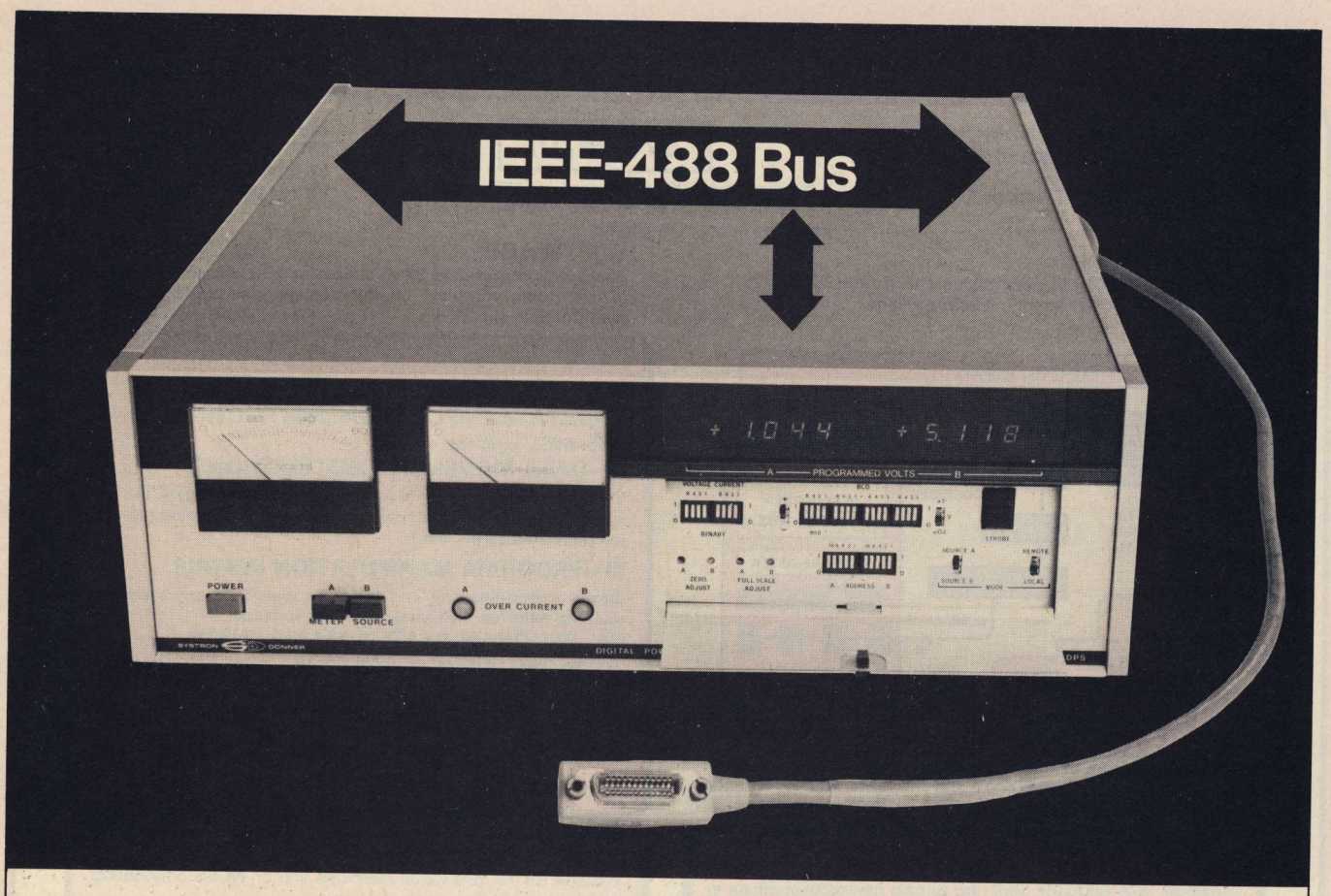
III—PROGRAM MANIPULATION INSTR'S

Sixteen microcode instructions: increment, direct and conditional jumps, N-Way branching, subroutine (expandable 4-deep nesting) and microinstruction repeats. Both the subroutines and microinstructions can be repeated—a unique capability.

IV—PROGRAM STATUS MANIP. INSTR.

Status indications brought out from ALU on 10800 and 10803; carry, overflow, sign, zero and parity.
Also, user's status can be stored in 10801.

SOFTWARE SUPPORT: MACE 29/800 system for developing microprogrammable μC's will handle both ECL and TTL slices. This system will be available in 1978.



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Key specifications: resolution, 1 mV; basic accuracy, 1 mV; stability, 300 μV.

Instead of buying **two** expensive power supplies, you can now do the job with **one** DPSD-50 ($3,000 in U.S., slightly higher outside U.S.). For more details, contact Scientific Devices or Systron-Donner at 10 Systron Drive, Concord, CA 94518. Phone (415) 676-5000.

SYSTRON DONNER

For more information, Circle No. 45

BIPOLAR

AVAILABILITY: Now.
COST: CPU is $32 (100) qty). The $175 starter kit includes CPU, 4 IV bytes and 1.5k words of PROM.
SECOND SOURCE: To be announced (a major U.S. company).

8X300 MicroController

Originally a custom chip processed for SMS by Signetics, 8X300 is now offered at device level. The first single-chip 8-bit processor, it is being applied to CRT and floppy disc control, real time digital communications, etc.

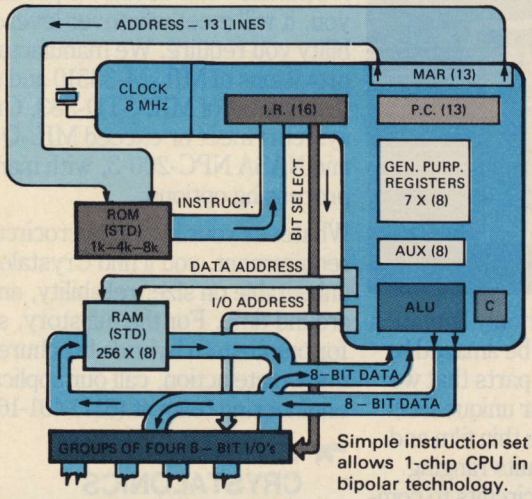
Signetics
811 E. Arques Ave.
Sunnyvale, CA 94086.
Phone (408) 739-7700

HARDWARE

Schottky-TTL LSI chips. CPU consumes 1.57 W, has 50-pin pkg.

SOFTWARE

Only 8 instruction types; all execute in 250 nsec, max. Each specifies source for data, operation to be performed, and destination for data. Data can be internal register or any group of 1 to 8 bits on interface.



Simple instruction set allows 1-chip CPU in bipolar technology.

I—DATA MANIPULATION INSTRUCTIONS

ADD is the sole arithmetic command. AND and XOR are two logical commands. However, the CPU can shift and bit test while executing instructions. Thus, it can examine I/O bits in 250 nsec.

II—DATA MOVEMENT INSTRUCTIONS

Move data between source and destination (MOVE).
Load literal value (part of instruction) into address (TRANSMIT).

III—PROGRAM MANIPULATION INSTR'S

Indexing by jamming offset into PC (EXECUTE).
Branch if data is not zero.
Although MicroController lacks hardware interrupt, software polling can be performed rapidly.

IV—PROGRAM STATUS MANIP. INSTR.

None.

HARDWARE SUPPORT: "McSim" development system from SMS has in-circuit emulation capability. Designers kit 8X300kT100SK available from Signetics.

SOFTWARE SUPPORT: $775 MicroController cross-assembler will run on any 16-bit machine that uses FORTRAN. Also available on NCSS timesharing.

BIPOLAR

AVAILABILITY: Now.
COST: $14.60 per 4-bit slice in 100 qty.
SECOND SOURCE: None announced.

SBP0400A

Four-bit I²L processor slice. (Because of continuous product improvements, designers should contact TI for latest specs.)

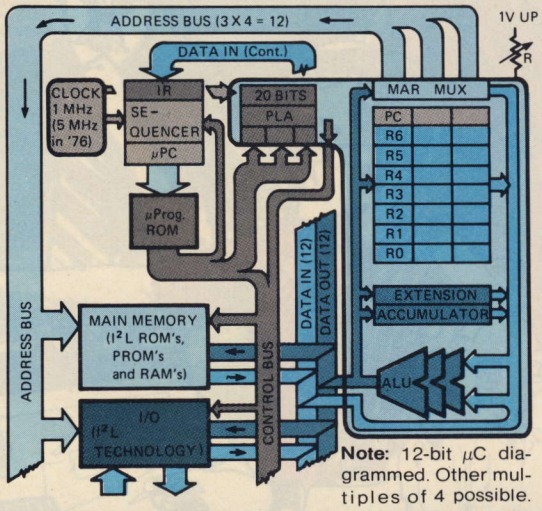
Texas Instruments, Inc.
Box 1443
Houston, TX 77001
Phone (713) 494-5115

HARDWARE

Circuits operate with very low voltage supplies over a 1000:1 range of injector current. Power consumption can be very low, but dropping resistors needed with 5V TTL raise total consumption. 40-pin DIP.

SOFTWARE

Slices respond to 512 microinstructions (9-bit control word) within one 200-nsec clock cycle, and operate at true micro or gate control level. User builds up his macroinstruction set from these.



Note: 12-bit μC diagrammed. Other multiples of 4 possible.

I—DATA MANIPULATION INSTRUCTIONS

Arithmetic and logical. Similar to TTL 74181 and 74182. The operations field of the microcontrol word is 4-bit wide, giving 16 basic ALU operations, plus full signed shifting capability.

II—DATA MOVEMENT INSTRUCTIONS

9-bit op-control word contains 3 fields: 4-bit ALU selection field; 3-bit source/destination field; and 2-bit shift-select field.

III—PROGRAM MANIPULATION INSTR'S

Must be created by user through sequences of microcode. Can be pipelined.

IV—PROGRAM STATUS MANIP. INSTR.

Must be created by user through microcode and register assignments.

HARDWARE SUPPORT: LCM-1000 series of microprogrammable prototyping modules (approximately $75 to $150).

SOFTWARE SUPPORT: Application-note examples detail micro- and macroinstruction codes for selection of instructions from variety of machine types.

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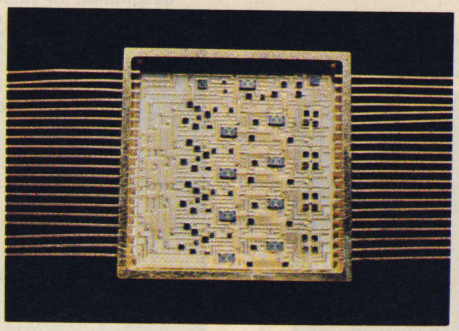

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Cambridge, MA 02140
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For more information, Circle No. 46

BIPOLAR

AVAILABILITY: Now.
COST: $29.25 in 100 qty.
SECOND SOURCE: None announced.

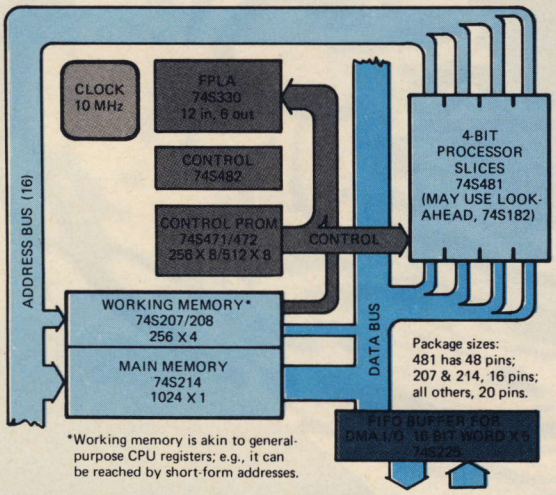
74S481, etc. Chip Set

Fast, microprogrammable Schottky TTL chip set suitable for constructing minicomputers with LSI parts.

Texas Instruments, Inc.
Bipolar Digital Circuit Div.
Houston, TX 77001
Phone (713) 494-5115

HARDWARE:

Schottky TTL will operate at 10-MHz clock, with usual 5V supply and over Mil. temp. range.



*Working memory is akin to general-purpose CPU registers; e.g., it can be reached by short-form addresses.

SOFTWARE:

Microprogrammable, so user defines instruction set. However, TI will offer version that emulates TI's own 990 mini.

Both hardwired algorithms (macro) and micro operations are available, totalling 24,780 unique instructions. The 14 classes of instructions include the following:

I—DATA MANIPULATION INSTRUCTIONS
Built-in multiples and divides.

II—DATA MOVEMENT INSTRUCTIONS

III—PROGRAM MANIPULATION INSTR'S

IV—PROGRAM STATUS MANIP. INSTR.

SOFTWARE SUPPORT: Minicomputer level.

HARDWARE SUPPORT: Minicomputer level.

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