

PLUG-AND-PLAY CONTROLLER (PPC)

ADVANCE INFORMATION

JULY 1994

KEY FEATURES

- Provides Plug-and-Play compatibility for ISA add-in cards
- Conforms to Intel/Microsoft Plug-and-Play specification v1.0a (May 5, 1994)
- Interface to serial resource EEPROM with read and write capability for storage of data structures required by Plug-and-Play and additional user defined data.
- Provides five chip select outputs:
 - Two I/O chip selects, /CS0 and /CS1, f{A0-A15}
 - Two memory chip selects, /CS2 and /CS3, f{A0-A23}
 - /CS4 is the OR of CS0 and CS3 and is used as described below
- Supports two DMA channels and two interrupts from the logical device
 - Interrupts directed to any of 11 interrupt channels on the ISA bus
 - DMA directed to any of 7 DMA channels on the ISA bus
- Provides four quasi-bidirectional general purpose I/O lines for use on the board
- 120-pin SQFP
- 5V operation

INTRODUCTION

The *Industry Standard Architecture* (ISA) bus is the most popular expansion standard in the PC industry. The bus architecture requires the allocation of memory and I/O address spaces, DMA channels and interrupt levels among multiple ISA cards. However, the ISA interface has no defined hardware or software mechanism for allocating these resources. As a result, configuration of ISA cards is typically done with jumpers that change the decode maps for memory and I/O space and direct the DMA and interrupt signals to different pins on the bus. Further, system configuration files may need to be updated to reflect these changes. For the average user, this configuration process can be frustrating and unreliable.

The Plug-and-Play ISA specification defines a hardware and software mechanism for incorporation in the next generation of ISA cards, referred to as Plug-and-Play ISA cards, that enables resolution of conflicts between Plug-and-Play ISA cards. It defines mechanisms that each Plug-and-Play ISA card must implement to support identification, resource usage determination, conflict detection, and conflict resolution.

The essential elements of the Plug-and-Play ISA process are:

- Isolate the ISA card

- Read the card's resource requirements data
- Identify the card and configure its resources
- Locate a driver for the card

This process is done automatically at every hard reset of the system. Plug-and-Play ISA cards will interoperate with standard ISA cards in a fully compatible manner. Information that identifies the card and describes the system resources which are requested by the card, such as memory and I/O space, DMA channel, and interrupt level supported is maintained in a standardized read-only format.

In a system that uses only Plug-and-Play ISA cards, it will be possible to achieve full auto-configuration. It is recognized that the current generation of standard ISA cards will coexist with Plug-and-Play ISA cards in the same system. In such systems, the configuration solution needs to be augmented in the BIOS and/or operating system to manage and arbitrate the allocation of ISA bus resources. User interaction may still be necessary in some cases.

GENERAL DESCRIPTION

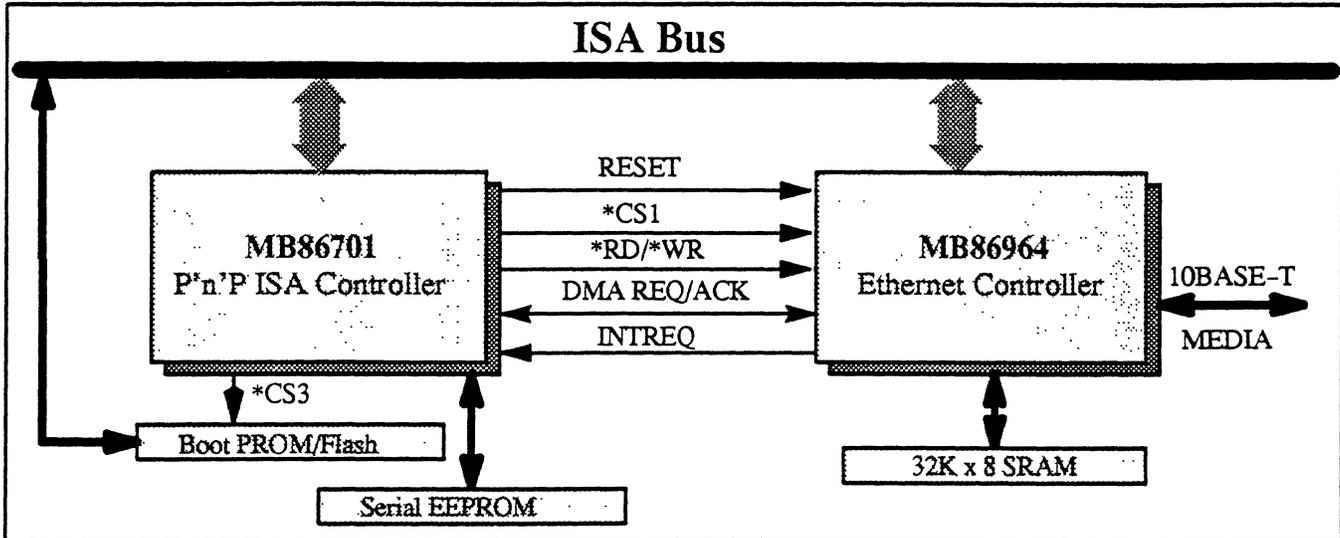
The MB86701 is a single chip device that provides the hardware resources required to build ISA cards compliant with the Plug-and-Play specification. It provides the interface to an external serial EEPROM which stores the card's resource requirements information and can also store additional user-defined data such as Ethernet ID or manufacturing traceability information. The chip stores the configuration information provided by the Plug-and-Play software in the registers defined by the specification. The chip then performs the functions of I/O and memory address decoding, interrupt request and DMA signal steering by appropriately decoding the stored configuration information, providing the basic capabilities described in KEY FEATURES above.

The MB86701 also provides several additional features, not required by the specification, which can enhance card performance and reduce the card's cost. For example, it provides a four-bit I/O port where each pin can be independently used as an input or an output. These lines allow control of functions such as media selection for a LAN card or monitoring of external events.

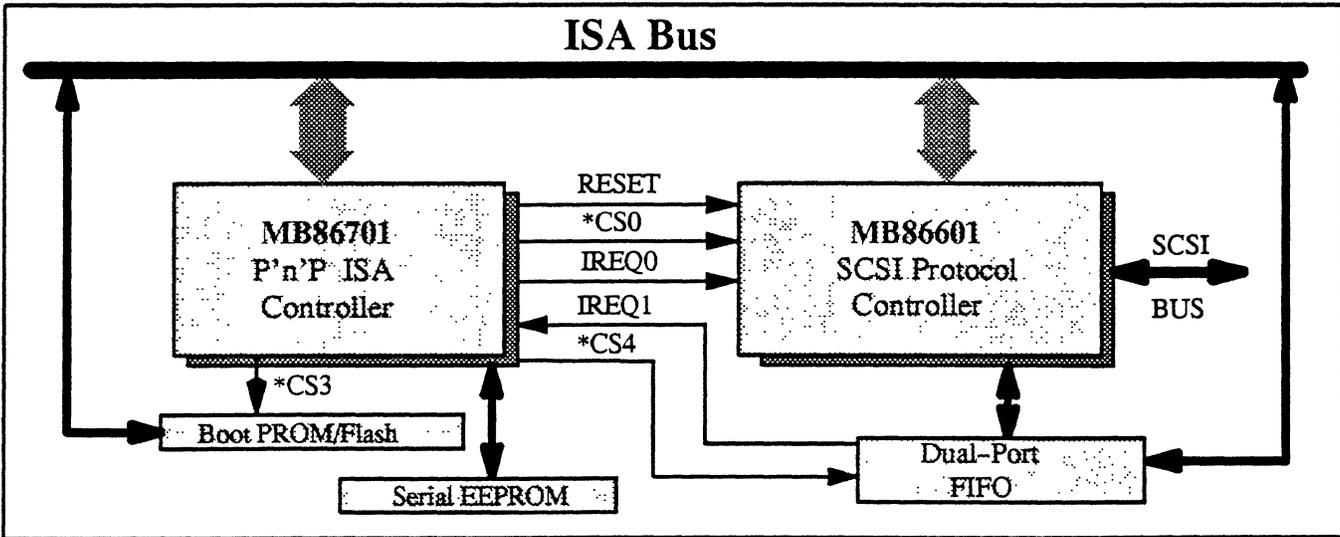
A unique feature maps any access to a user-defined memory window into a single user-defined address on the logical device side of the chip. This is done by providing a single output composed of two of the chip select signals, while simultaneously providing combined read and write strobes. This allows the driver software to use memory-reference instructions to access a fixed-address register

on the card and thus improve data-transfer performance. For example, this can be used to move a sector of data to or from a FIFO on a SCSI card using string or block move instructions instead of a loop of I/O instructions.

The MB86701 is fabricated using a low-power CMOS process and is furnished in a 120-pin shrink quad flat package.



MB86701 Application Example - Ethernet Card



MB86701 Application Example - SCSI Card

FUJITSU MICROELECTRONICS, INC.
 3545 North First Street
 San Jose, CA 95134
 Telephone: 408-922-9000 Fax: 408-526-9515

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