FUJITSU

May 1994

MB86680B
ATM SWITCH
ELEMENT
(SRE)

VER 2.0

FUJITSU MICROELECTRONICS, INC.

May 1994
Edition 2.0

FUJITSU

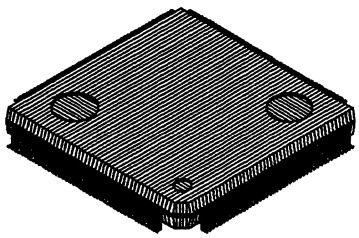
DATA SHEET

MB86680B
ATM SWITCH ELEMENT (SRE)

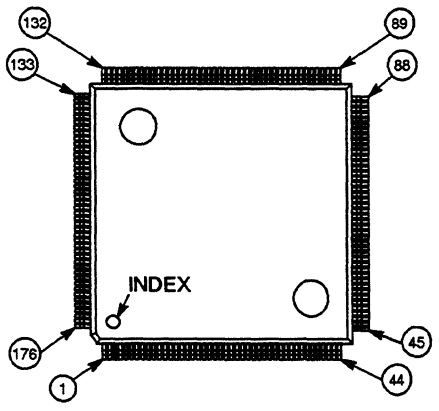
ATM Switch Element

The FUJITSU MB86680B is a self-routing switch element for use in ATM switch fabrics. It is ideally suited to applications in a variety of customer premises equipment such as ATM hubs and network access controllers. The device is organized as a 4 x 4 switch with separate input and output ports for matrix expansion. The main features of the device are listed below:-

PLASTIC PACKAGE
SQFP-176



PIN ASSIGNMENT



FEATURES

- Highly integrated 4x4 structure.
- Active matrix expansion ports for row and column interconnect.
- Selectable high and low priority output queues.
- Output port buffer capacity of 75 cells, which can be divided into a 50 cell low priority queue and a 25 cell high priority queue.
- Multicast support.
- Selective cell discard based on CLP bit and selectable queue level.
- Selectable Forward Explicit Congestion Notification (FECN) function.
- Statistics gathering and transmission to provide information on discarded cells and queue overflow events.
- Flexible tag processing to allow a variety of switch fabric architectures to be realized.
- All input / output ports operate at up to 25MHz using an 8-bit data format.
- Separate input clock signals for each interface.
- Separate cell synchronization signals for each port.
- Provides selectable UTOPIA compatibility.
- JTAG pins compatible with IEEE1149.1 are provided.
- Fabricated in sub-micron CMOS technology with CMOS/TTL compatible I/O and single +5V power supply.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Table of Contents

APPENDICES

TABLES

ILLUSTRATIONS

1. OVERVIEW

1.1. Outline

The Fujitsu MB86680B is a self-routing ATM cell switch element (SRE) which can be used as a basic building block for a variety of 155Mb/s ATM switch fabrics. The device provides 4 output data queues, one for each output port and each with an aggregate storage capacity of 75 cells per output port. A 24 bit routing tag is used to decide which output queue a particular cell will be loaded into.

Each output queue is divided into a high and low priority section. A control bit in the routing tag determines the cell priority. High priority cells will always be forwarded in preference to low priority cells. Hence cells using the high priority queues will suffer less queueing delay and will have a lower cell loss rate than cells using the low priority queues (assuming that high priority traffic only forms a small portion of total traffic).

The switch element includes four expansion inputs, which are provided to facilitate easy expansion in the form of a matrix. Cells received via the expansion inputs are directed into the attached output data queue.

1.2. Matrix Configuration

Various interconnection topologies can be applied to the SRE. However, the device is ideally suited to interconnection in the form of a matrix. In this case the SRE provides re-timed active outputs which allow direct connection to nearest neighbours. This eliminates the need for passive buses and reduces device interconnect problems at the board level. A matrix architecture is illustrated in Fig 1.

The number of switch elements required for an N x N switch is proportional to N^2 and hence is only appropriate for relatively small switch fabrics (eg. 32 X 32). For larger switches, individual matrices can be interconnected using a multi-path delta arrangement.

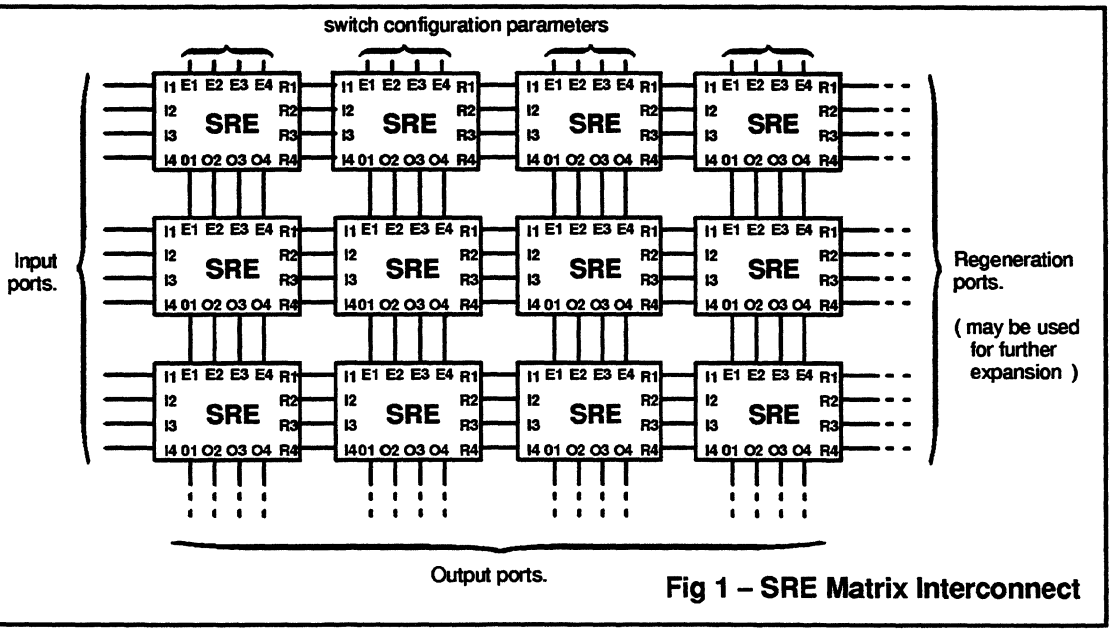


Fig 1 – SRE Matrix Interconnect

1.3. Delta Configuration

Larger switches may be realized by connecting SRE matrices into switch topologies similar to the two stage delta configuration as illustrated in Fig 2. Each switch element allows a selectable region of the tag field used for address filtering. Hence a multi-path delta switch can be constructed without the need for intermediate address translation/tag generation.

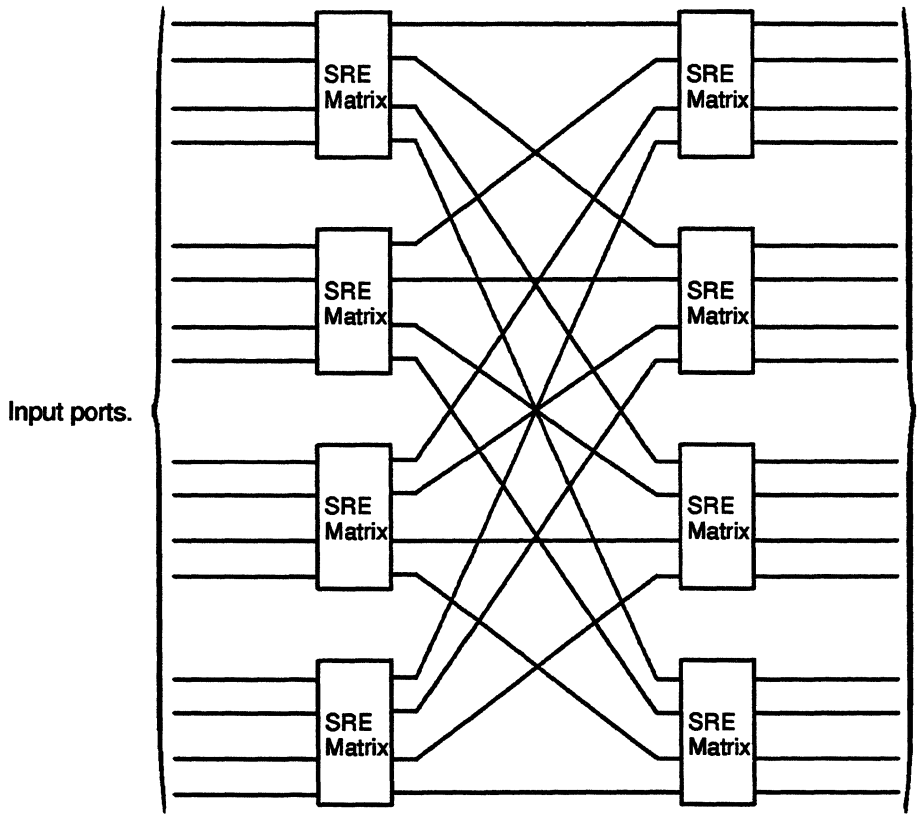


Fig 2 – Delta Switch Configuration

2. EXTERNAL INTERFACES

2.1. Logical Outline

A logical view of the SRE's external pins is illustrated in Fig 3 and a physical pin assignment is shown in Fig. 25.

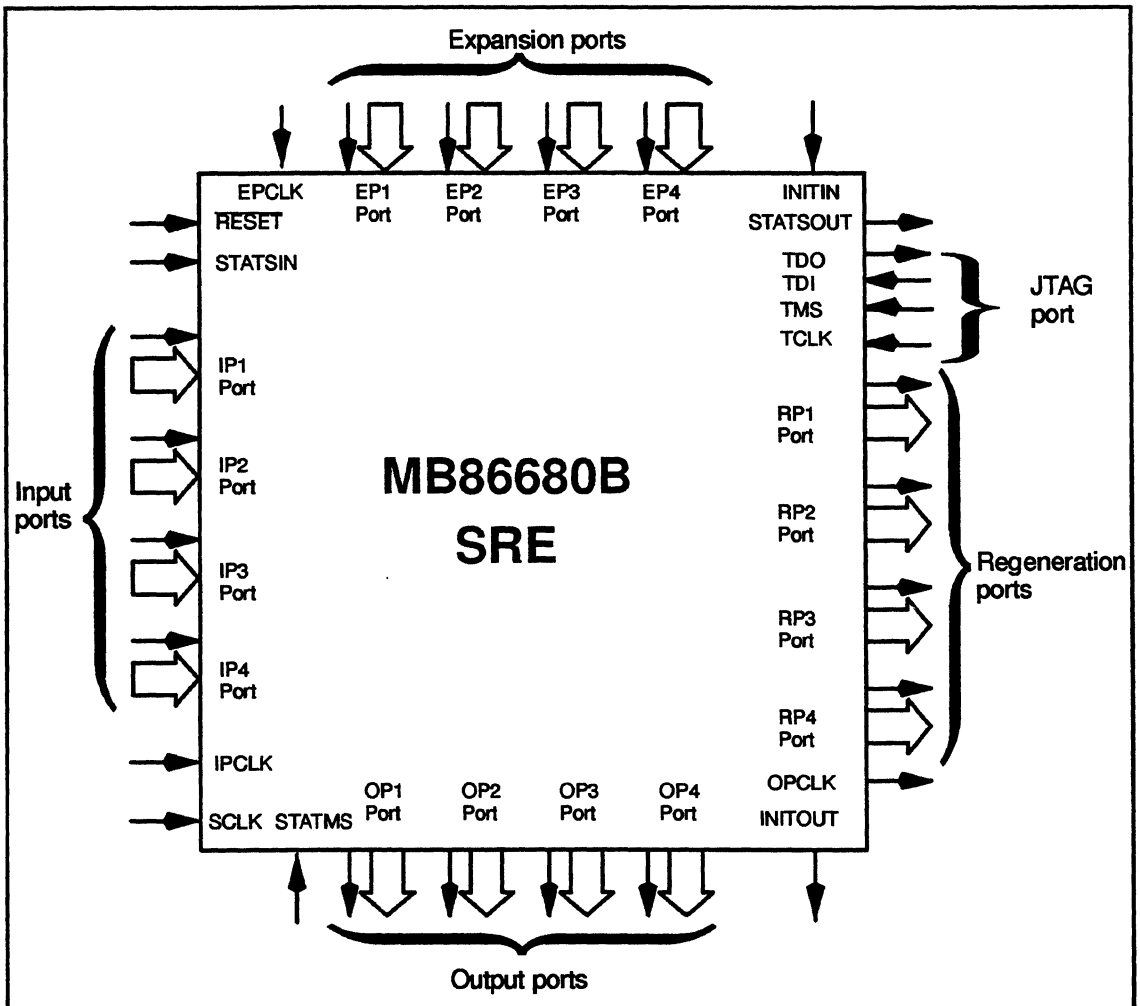


Fig 3 – SRE I/O Block Diagram

2.2. Detailed Description

A brief description of each of the SRE's input and output pins shall now be given.

$\overline{\text{RESET}}$
An active low pulse applied to the SRE's $\overline{\text{RESET}}$ pin will cause an SRE switch element to execute an internal Reset instruction cycle. The instruction will only be executed when a clock signal is applied to the IPCLK pin. A minimum of 2 IPCLK clocks will be required to complete the instruction cycle.

IPCLK
Data present on the input ports IP1DTx to IP4DTx, shall be sampled on the rising edge of this clock. This clock needs to be present if a complete Reset instruction cycle is to be executed following an active low transition on the $\overline{\text{RESET}}$ pin.

EPCLK
Data present on the input ports EP1DTx to EP4DTx, shall be sampled on the rising edge of this clock.

The EPCLK input pin shall also be used by an SRE switch element to determine whether the switch element should act as Master or as a Slave. If the EPCLK input pin is permanently tied to VSS then the switch element shall be deemed to be a Master.

If however a clock is present on the EPCLK input pin then the SRE shall be deemed to be a Slave.

SCLK
Data present on the STATSIN and STATSOUT serial highways shall be sampled/transmitted on the rising / falling edges of this clock respectively.

When operating in the Fujitsu Cell Stream mode, the Output port data transitions shall be synchronised to the falling edge of SCLK. When operating in the UTOPIA Cell Stream mode, the Output port data transitions shall be synchronised to the rising edge of SCLK.

The clock signal applied to this input pin may be of an arbitrary frequency up to and including the IPCLK clock frequency, and not necessarily phase aligned to it either.

IP1DTx – IP4DTx
The device comprises four primary input ports, IP1DTx to IP4DTx, each of which is organized as 8-bit parallel data together with a start of cell (IPxSOC) bit. All primary input data is sampled on the rising edge of an input clock signal (IPCLK). The nominal IPCLK frequency is 20MHz. Incoming data comprises a 3 byte routing tag followed by a 53 byte ATM cell.

EP1DTx – EP4DTx
Four expansion ports, EP1DTx to EP4DTx, are provided for column interconnect in a matrix architecture. The data format on the expansion ports is similar to the primary input port format, except that data is synchronized to an expansion port clock (EPCLK), which is provided by the previous switch element.

Master Switch elements at the top of each column do not need the expansion port, and in this case the input pins will take on different functions in order to allow the routing tag characteristics to be defined. Pin functions are described in Section 3.2.1..

The alternative functions are selected by connecting the EPCLK input signal to VSS. The functions of the tag control inputs are described in Section 3.3.1.

STATSMS

The STATSMS input pin allows the SRE switch element to be configured as either a Statistics master or as Statistics slave SRE.

If the STATSMS pin of an SRE switch element is tied to VDD then that switching element shall be deemed to be a Statistics master.

If the STATSMS pin of an SRE switch element is tied to VSS then that switching element shall be deemed to be a Statistics slave.

STATSIN

This STATSIN input pin is used to form a serial daisy-chain between multiple switch elements, thereby allowing a Statistics serial highway to be constructed between communicating SRE switch elements. This input receives data from the previous switch element. The data format for the daisy chain is based on variable length packets delimited by SYN characters as defined in CCITT international alphabet No. 5 and separated by flexible active high idle periods.

Data associated with the statistics daisy chain input is sampled on the rising edge of a serial data clock (SCLK), which can be of arbitrary frequency.

When the SRE switch element is configured as a Statistics master the STATSIN input is not used. In such a configuration the STATSIN input pin may be tied to either VSS or VDD.

STATSOUT

This output is used to format a serial daisy-chain between multiple switch elements. The output sends Stats data to the next switch element in the chain. The data format is logically equivalent to that received via the statistics input, except empty packets may be filled with local switch statistics.

The Output port data transitions shall be synchronised to the falling edge of SCLK.

Following an active low transition on the $\overline{\text{RESET}}$ pin the STATSOUT pin shall be driven to it's logic 1 state.

INITIN

The INITIN input pin shall be used by an SRE switch element when it is configured as a Slave i.e it's EPCLK input has a clock signal present. When configured as a Slave the switch element shall use the INITIN input pin to acquire configuration data from a Master SRE's INITOUT pin or from a device emulating the serial configuration capability of a Master SRE.

When the SRE switch element is deemed to be Master i.e it's EPCLK input is tied to VSS, the INITIN input pin is not used & therefore may be tied to either VSS or VDD.

INITOUT
The INITOUT pin shall be driven only by Master SRE switch elements ie. those switch elements whose EPCLK pin is permanently tied to VSS.

Master SRE switch elements shall use the INITOUT pin to convey configuration data loaded during it's initialisation phase, in a serial format to connected Slave SREs. On completion the INITOUT pin shall be driven to it's logic 1 state.

Following an active low transition on the $\overline{\text{RESET}}$ pin the INITOUT pin shall be driven to it's logic 1 state.

RP1DTx – RP4DTx
Four regeneration ports, RP1DTx to RP4DTx, are provided for matrix interconnection. The regeneration port data is logically identical to primary input port data, but is re-timed to an output clock (OPCLK), which can be directly connected to the IPCLK input of the next switch element.

When operating in the Fujitsu Cell Stream mode, the Output port data transitions shall be synchronised to the falling edge of IPCLK. When operating in the UTOPIA Cell Stream mode, the Output port data transitions shall be synchronised to the rising edge of IPCLK. Following a RESET instruction cycle these output pins shall be driven to their logic "0" state.

OP1DTx – OP4DTx
Four output ports, OP1DTx to OP4DTx, provide the primary switch output data. The data format is identical to all other ports.. When operating in the Fujitsu Cell Stream mode, the Output port data transitions shall be synchronised to the falling edge of OPCLK.

When operating in the UTOPIA Cell Stream mode, the Output port data transitions shall be synchronised to the rising edge of OPCLK. Following a RESET instruction cycle these output pins shall be driven to their logic "0" state.

When no data is being output the SRE shall drive these outputs to their logic 0 state.

TDO
The TDO output pin represents a tri-stateable serial output JTAG port through which test instructions and data from the internal test logic may be conveyed. Changes in the state of the signal driven through TDO shall only occur following the falling edge of TCK.When no signal is being driven through the TDO port the output pin should revert to it's tri-state condition.

Immediately following power-up the TDO output pin shall remain in it's undriven tri-state state.

TCK
The TCK input pin provides the clock signal for the JTAG internal test logic. Data received on the TDI input pin shall be sampled on the rising edge of TCK clock signal.

TMS

The TMS input pin shall be sampled on the rising edge of the TCK clock and decoded by the JTAG internal test logic to control test operations.

An External pull-up should be connected to this input to ensure that when this input is not driven a response identical to the application of a logical 1 results.

TDI

The TDI input pin shall provide a port through which JTAG serial test data and instructions may be received by the internal test logic.

An External pull-up should be connected to this input to ensure that when this input is not driven a response identical to the application of a logical 1 results.

3. FUNCTIONAL DESCRIPTION

3.1. Overview

A block diagram of the switch element is illustrated in Fig 4. From this it can be seen that each input port is connected in parallel to an address filter via a high speed multiplexer. The address filter processes the address bits contained in a 24 bit routing tag and if appropriate the associated cell will be allowed through to the desired FIFO buffer. Each FIFO is divided into a high and low priority section, and the address filter will determine the level of priority which should be associated with a particular cell.

Each output port is serviced by a High/ Low priority multiplexer, which removes cells from the high and low priority queues. The multiplexer will always give preference to high priority cells.

The above functions are described in more detail in the following paragraphs.

3.2. Initialisation.

The Configuration Manager block illustrated in Fig 4 is responsible for initialising an SRE switch element. An SRE switch element may be initialised/configured by one of two mechanisms depending on whether the element is a Master or a Slave element.

Fig 5 illustrates how the INITIN and INITOUT pins of SRE Master and Slave elements may be connected in order to allow initialisation of the respective elements.

Master SRE elements shall obtain their configuration data from the unused Expansion port pins as shown in Fig 5a, whilst Slave SRE elements may obtain their configuration data from either the INITOUT pin of a Master SRE as in Fig 5a or from a Programmable Logic Device (PLD), such as that shown in Fig 5b, capable of transferring a serial data stream identical to that shown in Fig 8.

Initialisation of an SRE switch element shall be carried out immediately following a Reset instruction cycle. A reset instruction cycle may be invoked by merely applying an active low reset pulse to the $\overline{\text{RESET}}$ pin and a clock signal to the IPCLK pin. The MB86680B switch element employs an internal reset strategy synchronous to the clock signal applied to the IPCLK pin and as a consequence the IPCLK clock must be present to complete the Reset instruction cycle.

All outputs shall be reset to their inactive states 1 IPCLK clock period after an active low pulse has been applied to the $\overline{\text{RESET}}$ pin.

The execution of the Reset instruction cycle shall be deemed to be complete 2 IPCLK clock periods after an active low pulse has been applied to the $\overline{\text{RESET}}$ pin. On completion of a Reset instruction cycle the an SRE switch element shall then enter it's Initialisation phase.

3.2.1. Initialisation of a Master SRE.

An SRE switch element shall be deemed to be a Master when it's EPCLK pin is permanently tied to VSS. In such a configuration the SRE switch element

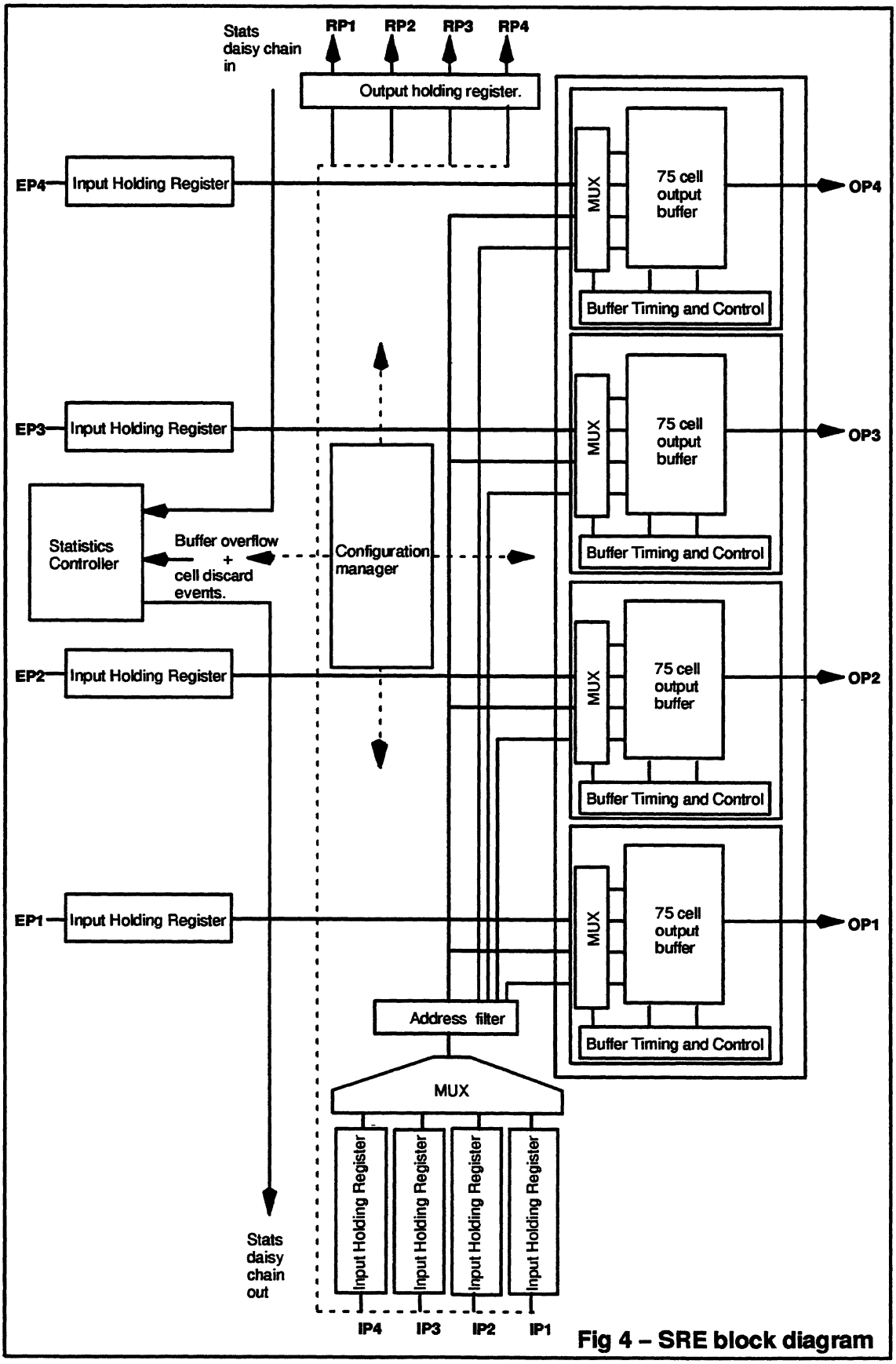
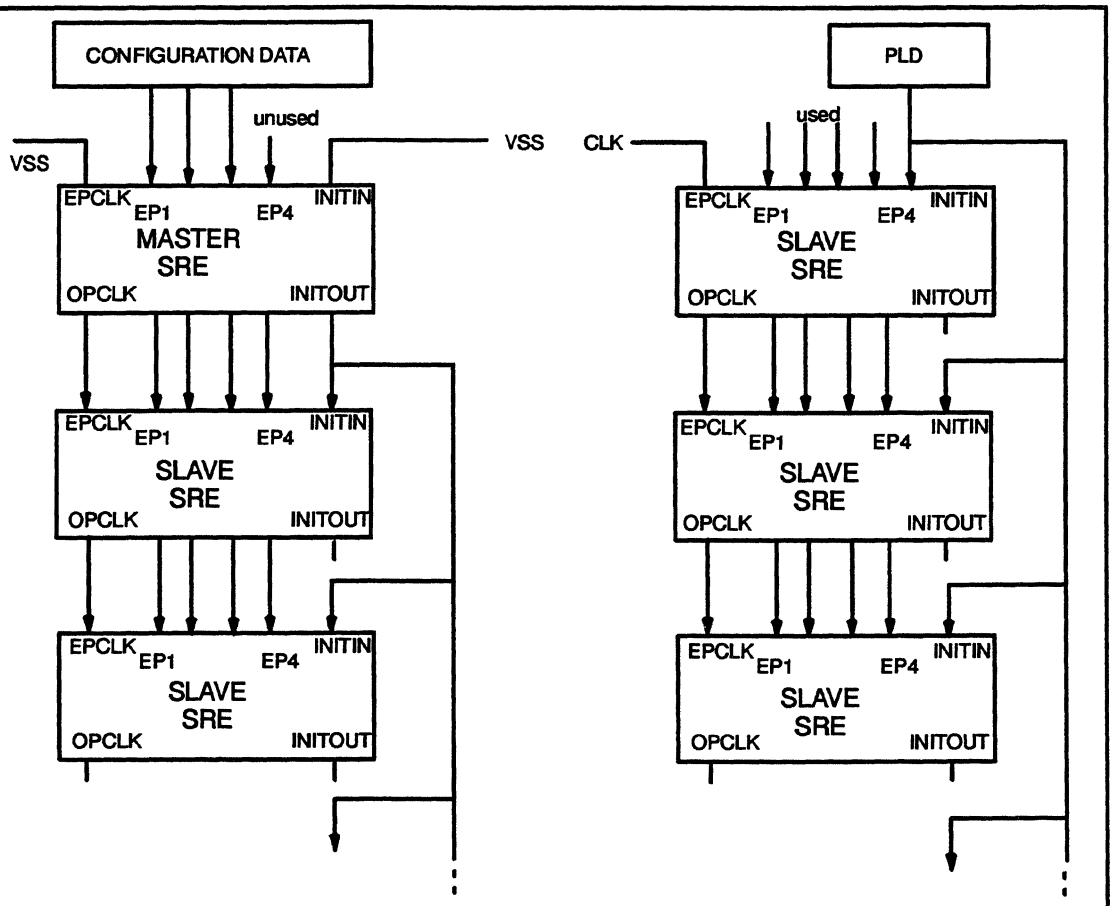


Fig 4 – SRE block diagram



a) Configuration Data from the unused Expansion Port

b) Configuration Data from INITIN/INITOUT pins

Fig 5 – Use of INITIN and INITOUT pins for Initialisation

may be internally configured via the data present on Expansion ports 1, 2 & 3.

The data present on the two expansion ports shall be immediately parallel loaded into the SRE switch element following a master reset instruction cycle operation.

A total of 14 input pins are used to configure the operating mode of the SRE. These inputs are shared with expansion port inputs and are selected by configuring the SRE switch element as a Master. The configuration information is transferred serially via the INITOUT line to other Slave SREs in the same column. The control pins are divided into seven groups:-

1. **Address Field Size**
   AFS1..AFS0 (EP1DT7..EP1DT6)
2. **Address Field Location**
   AFL3..AFL0 (EP1DT5..EP1DT2)
3. **Column Address**
   CA2..CA0 (EP2DT7..EP2DT5)
4. **High Priority Queue Enable**
   HPQE (EP2DT4)
5. **FECN Enable / Disable control**
   FECNE (EP2DT3)

6. **FECN Thresholds**
   FECNT1..FECNT0 (EP2DT2..EP2DT1)
7. **FCS_UTS**
   FCS (EP3DT7)

Note:
Test Pins
TST1 ..TST3 (EP3DT4..EPT3DT6)
These pins have been included for future board testability. These inputs should be tied low via a 2k7 resistor.
All other unused Expansion port input pins are reserved for internal use and should be connected to VSS.

Address Field Size and Location

The definition of these two groups of input pins are inter-dependent and are used to select a subset of tag bits which will be used by the SRE for address filtering. The address field size may vary from 2 bits (for Batcher/Banyan type topologies) to a maximum of 5 bits (for a 32 X 32 matrix). With a 5 bit address field, there are 4 possible locations within the 24 bits tag (note the upper 4 bits are used for control information). With a 2-bit address field there are 10 possible locations. The relationship between address field size and location within the routing tag is illustrated in Fig 6.

Fig 7 illustrates how the SRE shall interpret the Address size/location inter-relationship table, shown in Fig 6, to acquire the valid address field within the routing tag, when configured with an address size of four bits and a start address field location of PA8.

Column Address

This is a group of 3 input pins which is used to define the base address for the switch element when it is used in a matrix configuration. This code should be used to identify the group of columns that the SRE is connected to, as shown in Table 1.

Column Address CA2 (EP2DT7)	CA1 (EP2DT6)	CA0 (EP2DT5)	Column Group
0	0	0	1-4
0	0	1	5-8
0	1	0	9-12
0	1	1	13-16
1	0	0	17-20
1	0	1	21-24
1	1	0	25-28
1	1	1	29-32

Table 1 - Column Address Coding

High Priority Queue Enable

This input pin is used to enable or disable the high priority queue mechanism associated with each output buffer. When set to 0 the high priority queue is enabled, giving a 50 cell low priority queue and a 25 cell high priority queue. When set to 1 the high priority queue is disabled, giving a single 75 cell output queue.

FECN Enable / Disable control

The Expansion port pin EP2DT3, on a Master SRE, may be used to Enable / Disable the Forward Explicit Congestion Notification (FECN) function supported by the SRE. When this pin is tied low on a Master SRE, the FECN function shall be disabled on both the Master SRE and attached Slave SREs.

When the EP2DT3 pin is pulled high, the FECN function shall be enabled on both the Master SRE and attached Slave SREs.

Address Size Pins		
EP1DT7	EP1DT6	
AFS1	AFS0	Address size
0	0	2 bits
0	1	3 bits
1	0	4 bits
1	1	5 bits

Address Field Location Pins								
EP1DT5	EP1DT4	EP1DT3	EP1DT2	Start of Address field location within tag				
AFL3	AFL2	AFL1	AFL0					
0	0	0	0	PA0	PA0		PA0	PA0
0	0	0	1	PA5	PA4		PA3	PA2
0	0	1	0	PA10	PA8		PA6	PA4
0	0	1	1	PA15	PA12		PA9	PA6
0	1	0	0		PA16		PA12	PA8
0	1	0	1				PA15	PA10
0	1	1	0					PA12
0	1	1	1					PA14
1	0	0	0					PA16
1	0	0	1					PA18

Fig 6 – Address size/location inter–relationship

1st Octet	PC	MC	CLT1	CLT0	PA0	PA1	PA2	PA3
2nd Octet	PA4	PA5	PA6	PA7	PA8	PA9	PA10	PA11
3rd Octet	PA12	PA13	PA14	PA15	PA16	PA17	PA18	PA19

Fig 7 – Example of a Valid Address Field in a Normal Routing Tag

FECN Thresholds

The Expansion port pins EP2DT2 and EP2DT1, on a Master SRE, may be used to select the Output data queue fill level thresholds at which the FECN function may be implemented. Table 2 illustrates how the logic levels applied to these pins are interpreted by the Master SRE and attached Slave SREs.

EP2DT2 FECNT1	EP2DT1 FECNT0	FECN Threshold
0	0	Not used
0	1	20% full
1	0	50% full
1	1	80% full

Table 2 - FECN Threshold Coding

FCS_UTS

The Expansion port pin (EP3DT7) on a Master SRE may be used to select the Fujitsu Cell Stream (FCS) or the UTOPIA Cell Stream (UTS) mode of operation.

When the EP3DT7 pin is tied to VDD the UTS mode of operation is selected.

When the EP3DT7 pin is tied to VSS the FCS mode of operation is selected.

When operating in the FCS mode of operation, data present on the Inputs shall be sampled on the rising edge of their respective clocks whilst data transitions on the Outputs shall take place on the falling edge of their respective clocks.

When operating in the UTS mode of operation, data present on the Inputs shall be sampled on the rising edge of their respective clocks whilst data transitions on the Cell Stream Output Ports shall take place on the rising edge of their respective clocks.

Transmission of data on the serial INITOUT pin shall primarily be of an asynchronous format with data bit periods equal to the IPCLK/5. As already stated the transmitted data will not necessarily be phase aligned to the IPCLK. The INITOUT Port data transitions shall be synchronised to the falling edge of IPCLK/5 and shall be sampled by Slave SRE switch element's on the rising edge of their IPCLK.

Master SRE switch elements shall commence transmission on the INITOUT pin by driving the INITOUT pin low as shown in Fig 8. The configuration data shall then be transmitted as shown in Fig 8.

On completion of transmission, the Master SRE switch shall drive the line high until a further Reset instruction cycle is initiated.

3.2.2. Initialization of a Slave SRE

Slave SRE switch elements shall monitor their INITIN pins immediately following the execution of a Reset instruction cycle. On detecting the active low Start sync bit, as shown in Fig 8, the Slave SRE switch element shall commence using it's IPCLK to determine the nominal centre bit position whilst still checking that the line is still indicating the start polarity.

From then on, the Slave SRE shall sample each bit of the received initialization character by counting 5 clock periods from the preceding bit's nominal centre until all the necessary configuration data has been acquired.

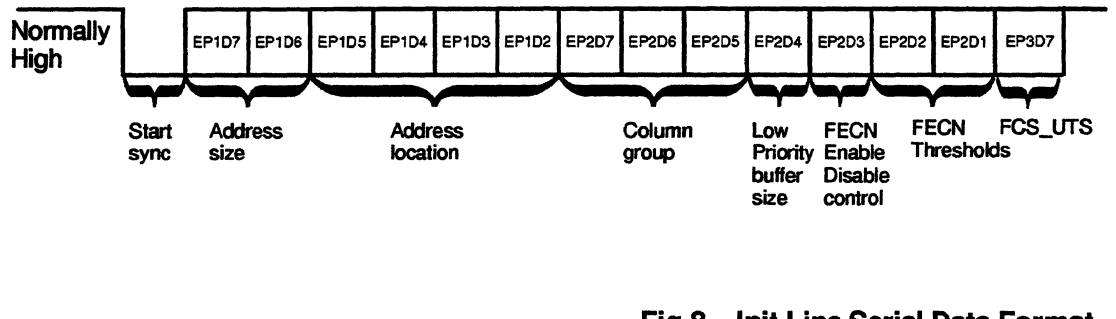


Fig 8 – Init Line Serial Data Format

On acquiring it's configuration data, the Slave SREs shall cease to monitor their INITIN pins until a further Reset instruction cycle has been initiated.

As a result of the initialization sequences described above the tag control settings for all SREs may be set by the INITOUT pin of a Master SRE being connected directly to the INITIN pin of the Slave SREs in the same column.

3.3. Address Filtering

Address filtering functions are controlled by the incoming 24 bit tag which is considered to be the first 3 bytes after a start of cell (IPxSOC) indication. The normal routing tag format is illustrated in Fig 9. A description of the function of the bits within this routing tag shall now be given. In all cases the MSB significance shall be left most justified.

3.3.1. Tag Control Field Format

PC Bit

The Priority Control (PC) bit determines whether the associated cell is loaded into the high priority queue or the low priority queue. This bit should be set on a per virtual circuit basis in order to guarantee that cell sequence is preserved. High priority channels should only be used for delay sensitive (or loss sensitive) data, and the total amount of traffic allocated to high priority channels should form a small percentage of the total available output bandwidth.

CLT0, CLT1

These bits are used to control the treatment of cells which have the CLP bit set. They determine the output queue fill level at which the cells will be discarded

CLT1	CLT0	Discard Threshold
0	0	no discard
0	1	20% full
1	0	50% full
1	1	80% full

Table 3 – Discard Threshold Coding

3.4. Multicast Operation

The Multicast Control (MC) bit may be used to invoke a special multicast routing mechanism within the switch. When this bit is set it changes the way in which the tag field is interpreted. In multicast mode the tag is divided into a 16 bit mask field, an output group select field, and a relay link address field. The PC and MC bit positions are unchanged. The multicast routing tag is illustrated in Fig 10.

The multicast routing mechanism is only applicable to matrix interconnection topologies, which may be either single stage or multi-stage. The following generic description assumes a two stage 64X64 switch comprising four 32X32 matrices, as shown in Fig 11.

For the purposes of this description, a multicast server is defined as a matrix which performs the multicast operation. A multicast server is identified by having its address location field configured to zero. It is assumed that these matrices provide primary outputs in a multi-stage configuration. Hence, in Fig 10 matrices B and D provide the primary outputs, have their address location bits set to zero, and hence are the multicast servers.

The multicast routing mechanism works as follows. Assuming that a cell with the MC bit set to 1 is received on input port 1, the SREs connected to input port 1 will examine the routing tag. All of these SREs will have their address location inputs set to something other than zero, and hence they are not multicast servers. These SREs will use the relay address field as the basis of their filtering operation. Hence all SREs except the one which matches the relay address will discard the cell. If we assume that the relay address is also set to 1, then the multicast cell will be relayed to matrix B on link 1.

Matrix B is a multicast server and it will perform the multicast operation. The output group select bit will determine which group of SREs will output the multicast cell. The bit mask will determine which outputs will be used. A logical one will cause the cell to be forwarded on the corresponding output port, and a logical zero will cause the cell to be discarded.

This mechanism allows a single primary input cell to be directed to up to 16

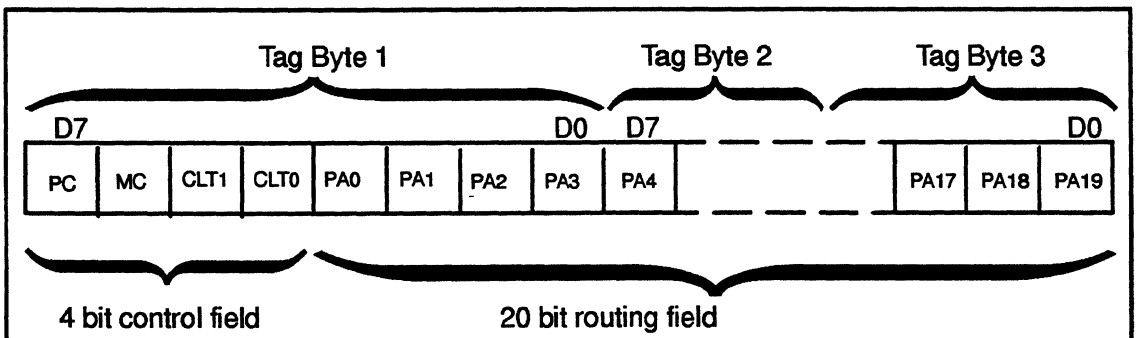


Fig 9 – Normal Routing Tag Format

primary outputs associated with a single output group. Hence, for the 64X64 switch illustrated in Fig 11, an input cell may need to be copied up to 4 times in order to achieve full coverage. The copying process may be performed by the Network Termination Controller (NTC), which will provide sufficient buffering to absorb the short 4-cell burst.

For multicast operation the user does not have control of cell loss threshold. A default cell loss threshold of 80% is assumed. If no discard is required then the CLP bit must be set to zero. The user does, however, have control over queue priority. If the PC bit is set to 1 then all relay and multicast operation will use the high priority queues.

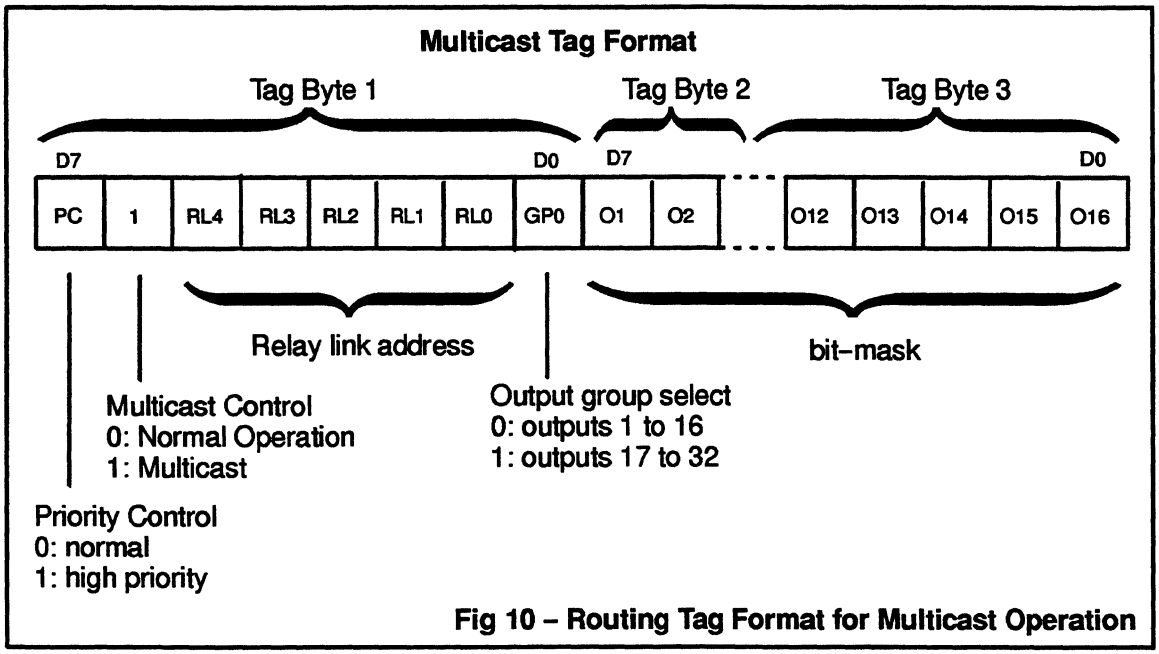


Fig 10 – Routing Tag Format for Multicast Operation

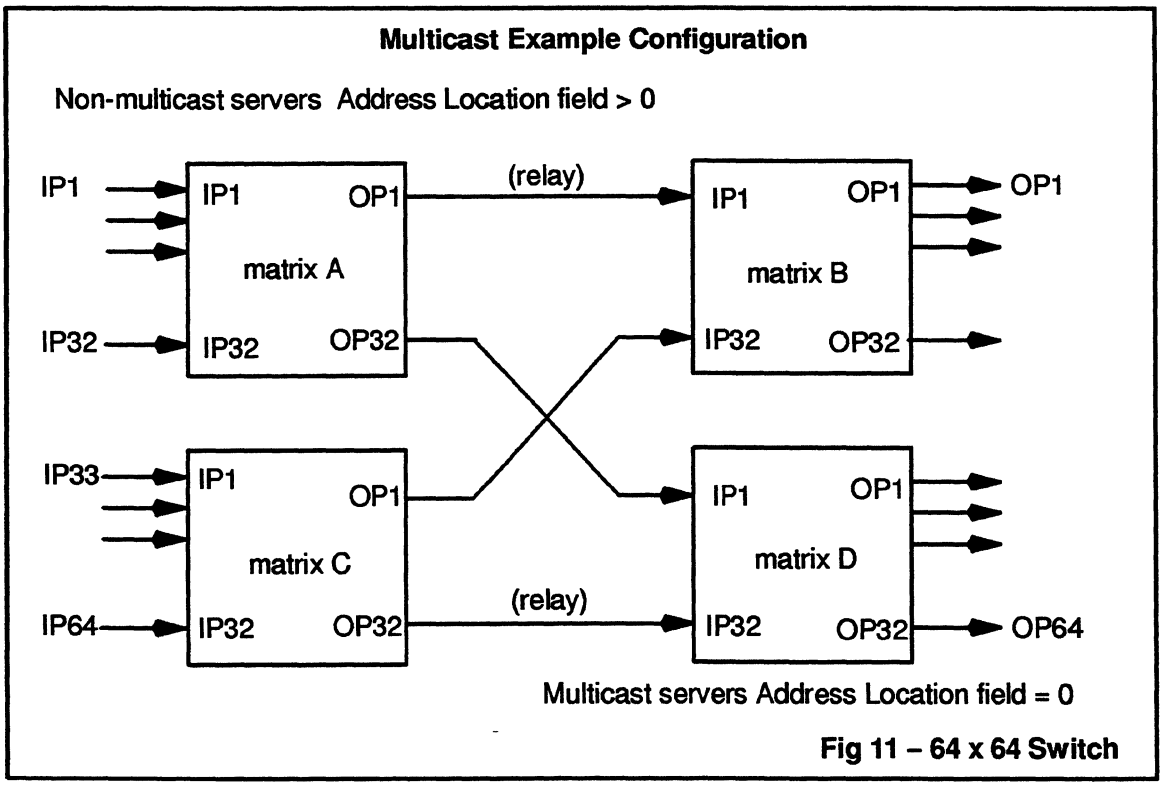


Fig 11 – 64 x 64 Switch

3.5. Forward Explicit Congestion Notification (FECN) function

An SRE's Forward Explicit Congestion Notification (FECN) function shall be enabled when the SRE has it's internal FECN Enable / Disable control bit set to a logical "1", as described in Section 3.2.1.

In such a circumstance, the SRE shall monitor the ATM cell header of incoming ATM cells in conjunction with the destined Output data queue threshold fill levels.

If an incoming cell is received with it's CLP bit set to a logic "0", at the same time the Output data queue to which it is being directed has a threshold fill level greater than or equal to the configured FECN Threshold (see Section 3.2.1. Table 2) , then the received cell shall have the PTI bits, see Fig 16, in it's ATM cell header altered to reflect congestion, prior to being loaded in to the Output data queue.

Bit 2 of the 3 bit PTI field shall be set to a logic "1" when the FECN function is activated.

The FECN function shall only be implemented on Low priority ATM cells whose CLP bit is set to a logic "0".

3.6. Statistics Generation

3.6.1. Introduction

The on chip Statistics Controller shown in Fig 4 is responsible for monitoring the SRE's STATSIN pin and for the processing of internally generated statistics.

When configured as a Statistics Master i.e the STATSMS pin is tied to VDD, the SRE switch element becomes responsible for driving the Stats highway. In such a configuration the switch element generates fixed length empty packets similar to those shown in Fig 12.

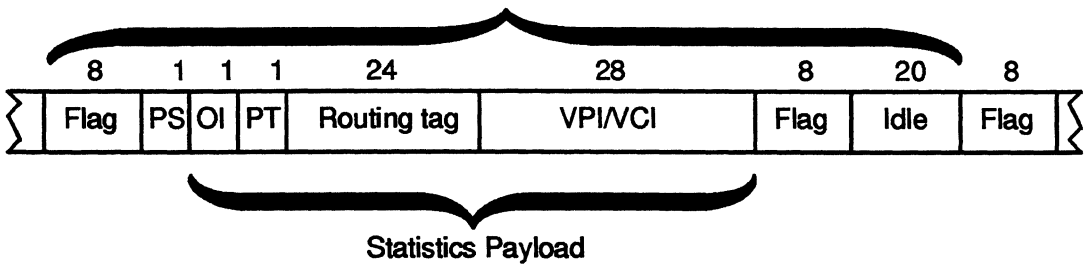
The fixed length empty packet in Fig 12 is delimited by SYN characters as defined in CCITT international alphabet No.5. An empty Statistics packet is denoted by the payload status bit of the packet being set to "0". In an empty Statistics packet the remaining bits in the Statistics payload are also set to "0".

The length of the Statistics packet shall vary depending on whether Automatic Zero Insertion (AZI) has been carried out on the Statistics payload and whether the Statistics payload data has been generated by an SRE switch element configured as a Statistics Master or as a Statistics Slave.

3.6.2. Statistics Generation by SRE Statistic Masters

As already mentioned the overall length of a Statistics packet will vary depending on whether AZI operations have been carried out on the (PS + Statistics Payload) bits and whether the Statistics data was generated within a Statistics Master or Statistics Slave.

If the Statistics data in a Stats packet was generated by a Statistics Master then the



Flag = 01111110

PS = statistics payload status : 0 = IDLE, 1 = BUSY

OI = statistics buffer overflow indication : 0 = Normal, 1 = Multiple Stats buffers overflowing

PT = statistics payload type : 0 = Normal CLP discard, 1 = SRE buffer overflow discard

Fig 12 – Normal Switch Statistics Packet Format

IDLE period as shown in Fig 12 will always be driven high for a period equal to 20 SCLK clock periods, no matter how many AZI operations have been carried out on the (PS + Statistics payload) bits.

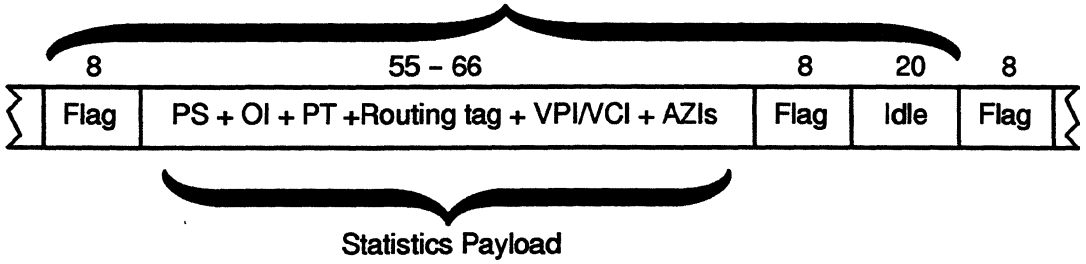
As a consequence of AZI operations, the bit length of the (PS + Statistics Payload) bits as shown in Fig 12 will vary from 55 bits, i.e no AZI operations carried out, to a maximum of 66 bits, i.e 11 AZI operations carried out.

As a result of this variation in the length of the (PS + Statistics payload), the overall Statistics packet generated by a Statistics Master may vary in length from 91 bits as shown in Fig 12, to a maximum packet length of 102 bits as shown in Fig 13.

3.6.3. Statistics Generation by SRE Statistic Slaves

Statistic Slave switch elements shall constantly monitor their STATSIN pin. When operating in the Fujitsu Cell Stream mode, the Output port data transitions shall be synchronised to the falling edge of SCLK. When operating in the UTOPIA Cell Stream mode, the Output port data transitions shall be synchronised to the rising edge of SCLK. The data received on this input port shall be latched on the rising edge of the SCLK clock

A Statistics slave switch element shall monitor the Stats serial highway in order to determine if the Statistics packet being received has an empty or full payload. If the PS bit is set to a "1", i.e BUSY, the Statistics payload shall be deemed to be full.



Flag = 01111110

PS = statistics payload status : 0 = IDLE, 1 = BUSY

OI = statistics buffer overflow indication : 0 = Normal, 1 = Multiple Stats buffers overflowing

PT = statistics payload type : 0 = Normal CLP discard, 1 = SRE buffer overflow discard

Fig 13 – Master Switch Statistics Packet Format

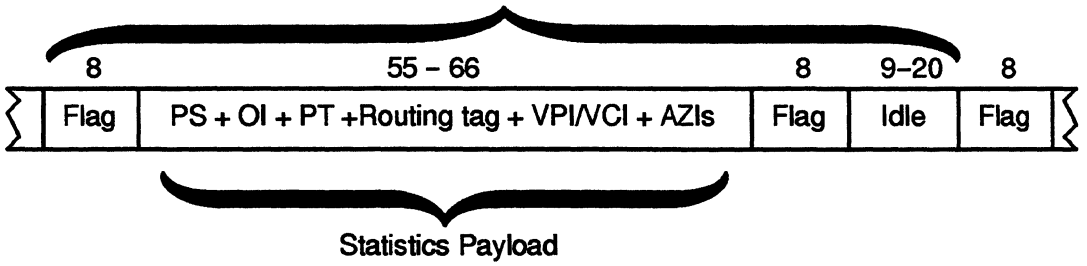
In such a circumstance, the Statistics packet shall proceed untouched through the Statistics Slave switch element. When operating in the Fujitsu Cell Stream mode, the Output port data transitions shall be synchronised to the falling edge of SCLK. When operating in the UTOPIA Cell Stream mode, the Output port data transitions shall be synchronised to the rising edge of SCLK. merely being latched on the rising and transmitted on the falling edge of the supplied SCLK.

If the PS bit is cleared, i.e PS = "0", the Statistics payload shall be deemed to be devoid/empty from Statistics data. In such a circumstance the packet is available for receiving any Statistics data that may have been generated within the Statistics Slave.

If the Statistics Slave switch element does not have any Statistics data to be processed, the Statistics packet shall be allowed to proceed untouched through the switch element, merely being latched on the rising and transmitted on the falling edge of the supplied SCLK.

If however the switch element does have Statistics data that does need processing the switch element shall commence transmitting it's Statistics data by setting the PS bit in the empty Statistics packet currently being received, to a "1".

The switch element shall then commence transmitting it's Statistics data onto the Stats highway. The transmitted data may or may not contain inserted zeros due to any AZI operations that may have been carried out the Statistics data. The net result of this operation is a Statistics payload that may vary from 55 bits to 66



Flag = 01111110

PS = statistics payload status : 0 = IDLE, 1 = BUSY

OI = statistics buffer overflow indication : 0 = Normal, 1 = Multiple Stats buffers overflowing

PT = statistics payload type : 0 = Normal CLP discard, 1 = SRE buffer overflow discard

Fig 14 - Slave Switch Statistics Packet Format

bits. The Statistics slave switch element shall then close the payload by generating a closing SYN character as shown in Fig 14.

On closing the switch statistics packet, the Statistics Slave switch element shall proceed by merely latching the data currently being received on it's STATSIN pin on the rising edge and transmitting it untouched on the falling edge of the supplied SCLK.

The net result of this action is a shortening of the IDLE period from it's normal 20 SCLK clock periods to a minimum of 9 SCLK clock periods depending on the number of AZI operations carried out on the (PS + Statistics payload) data. The variable parts of the Statistics packet generated by the Statistics Slave switch element are shown in Fig 14.

The net result of connecting the STATSOUT pin of a switch element to the STATSIN pin of a nearest neighbour as shown in Fig 15 is the construction of a synchronous Stats highway that may be terminated by a Fujitsu Network Termination Chip (NTC) such as the MB86683 or a HDLC controller type device utilizing a non-CRC checking mode.

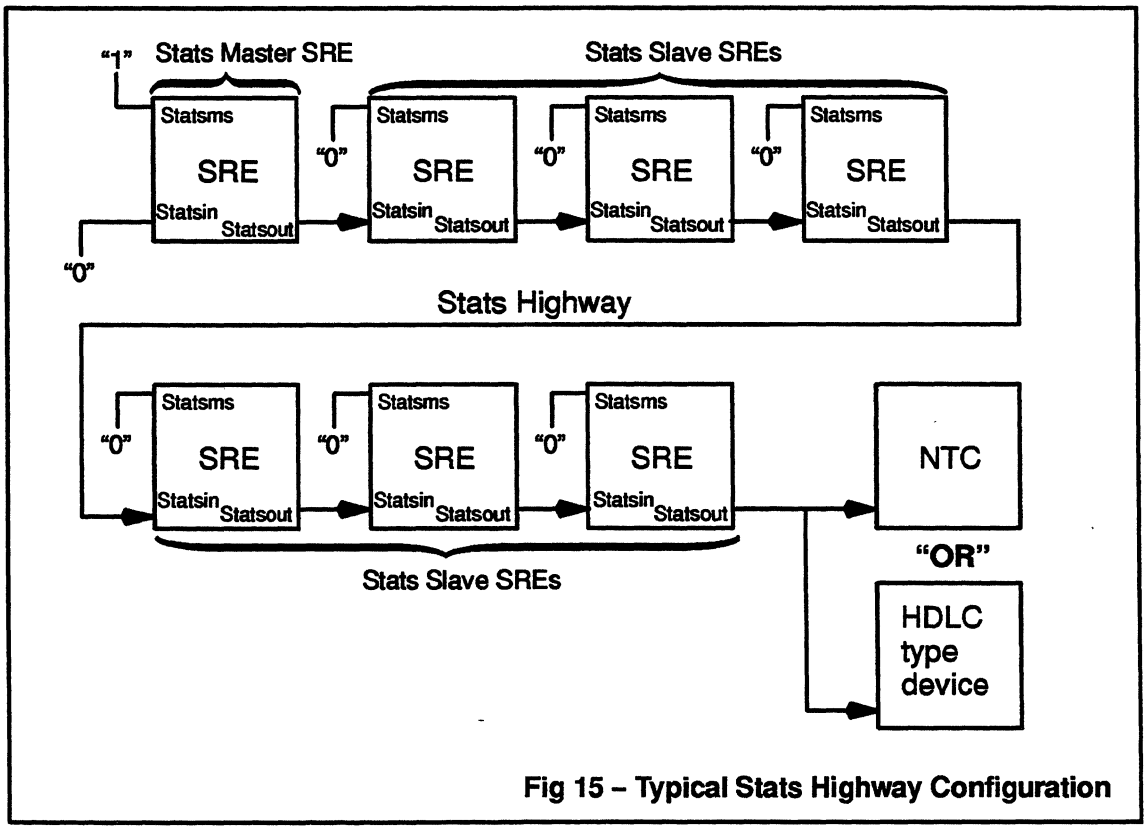


Fig 15 – Typical Stats Highway Configuration

3.7. JTAG

3.7.1. Introduction

This device now contains Boundary Scan Test Circuitry compliant with IEEE 1149.1 (JTAG). This requires the addition of the 4 pins identified below. The JTAG circuitry is internally reset at power on, and hence the optional JTAG reset pin (TRST) is not required.
The JTAG circuitry allows easier board level testing by allowing the signal pins on the device to form a serial scan chain around the device. The test modes are controlled by accessing an internal Test Access Port Controller (TAP), which is in turn controlled from the TAP.

3.7.2. Test Access Port (TAP)

Four pins are dedicated to JTAG:
TDO; TDI; TMS & TCK.
The functions of these signals are described in Section 2.3 (Pin Detailed Description) of this datasheet.

3.8. Test Instructions

The following JTAG instructions are implemented :-

BYPASS
SAMPLE/PRELOAD
EXTEST
INTEST

BYPASS

The BYPASS instruction is used to bypass a component that is connected in series with other components. This allows more rapid movement of test data through the components of the board, bypassing the ones that do not need to be tested. The BYPASS operation enables the bypass register, which is a single stage shift register, between TDI and TDO.

1. The binary code for the BYPASS instruction is 11.
2. The BYPASS instruction is forced into the instruction register output latches during the Test_Logic_Reset state. Note the distinction between the "01" content of the instruction shift register and the "11" of the instruction register output latch. Therefore, at the start of the instruction-shift cycle, a "01" pattern will be seen instead of "11".
3. The BYPASS operation does not interfere with the component operation at all. If the TDI input trace to the component is somehow disconnected, the test logic will see a "11" at TDI input during the instruction-shift state. Therefore, no unwarranted interference with the on-chip system logic occurs.

SAMPLE/PRELOAD

The SAMPLE/PRELOAD instruction is used to sample the state of the component pins. The sampled values can be examined by shifting out the data through TDO. This instruction selects the boundary scan-cell output latches with specific values. The preloaded values are then enabled to the output pins by the EXTEST.

1. The binary code for the instruction is 01.
2. The SAMPLE/PRELOAD instruction selects the boundary-scan cells to be connected between TDI and TDO in the Shift_DRTAP controller state.

3. The values of the component pins are sampled on the rising edge of TCK in the Capture_DR TAP controller state.

4. The preload values shifted in the boundary_scan cells are latched into the boundary-scan output latch at the falling edge of TCK in the Update_DR TAP controller state.

EXTEST

The EXTEST instruction allows testing of off-chip circuitry and board level interconnections. The PRELOAD /SAMPLE instruction is used to preload the data into the latched parallel outputs of the boundary-scan shift register stages. Then, the EXTEST instruction enables the preloaded values to the components output pins.

1. The binary code for the instruction is 00.

2. The device outputs the preloaded data to the pins at the falling edge of TCK in the Update_IR TAP controller state at which point the JTAG instruction register is updated with the EXTEST.

3. The EXTEST instruction selects the boundary-scan cells to be connected between TDI and TDO in the SHIFT-DR test logic controller state.

4. Once the EXTEST instruction is effective, the output pins can change at the falling edge of TCK in the Update_DR TAP controller state.

INTEST

This instruction allows testing of the on-chip system logic. Test stimuli are shifted in, one at a time, and applied to the on-chip logic. The test results are captured into the boundary scan register (BSR) and are examined by subsequent shifting. The PRELOAD/SAMPLE instruction is used to preload the data into the latched parallel outputs of the boundary-scan shift register stages prior to INTEST being selected.

The binary code for the instruction is 10.

4. DEVELOPERS NOTES

4.1. External Interfaces

External interfaces of the switch element are illustrated in Fig 3. and are described in the following paragraphs.

4.1.1 ATM Cell Structure

The structure of an ATM cell is illustrated in Fig 16. The only bit in the cell that is processed by the SRE is the CLP bit. This bit is used to determine whether a cell should be discarded when the output queue fill level exceeds a programmable threshold.

Note: When FECN is disabled, none of the bits in an ATM cell will be modified by the SRE. The SRE will not discard idle cells; it is assumed that idle cells will be discarded before data is applied to the switch (eg. by the Network Termination Controller).

4.1.2 External Data Structure

All input/output data for the SRE comprises 8 data bits together with a Start of Cell (SOC) bit and a clock signal. The data for one cell period comprises a 3 byte tag field followed by a 53 byte ATM cell. The cell stream may be continuous or discontinuous.

In both cases the SOC bit marks the first tag byte associated with a cell period. The clock rate should be selected to be as close as possible to 56/53 X ATM cell data rate. For SDH STM-1 applications a value of 155.52MHz / 8 provides a good match.

A diagram of the external data interface format for both Fujitsu Cell Steam and UTOPIA mode of operation is illustrated in Fig 17.

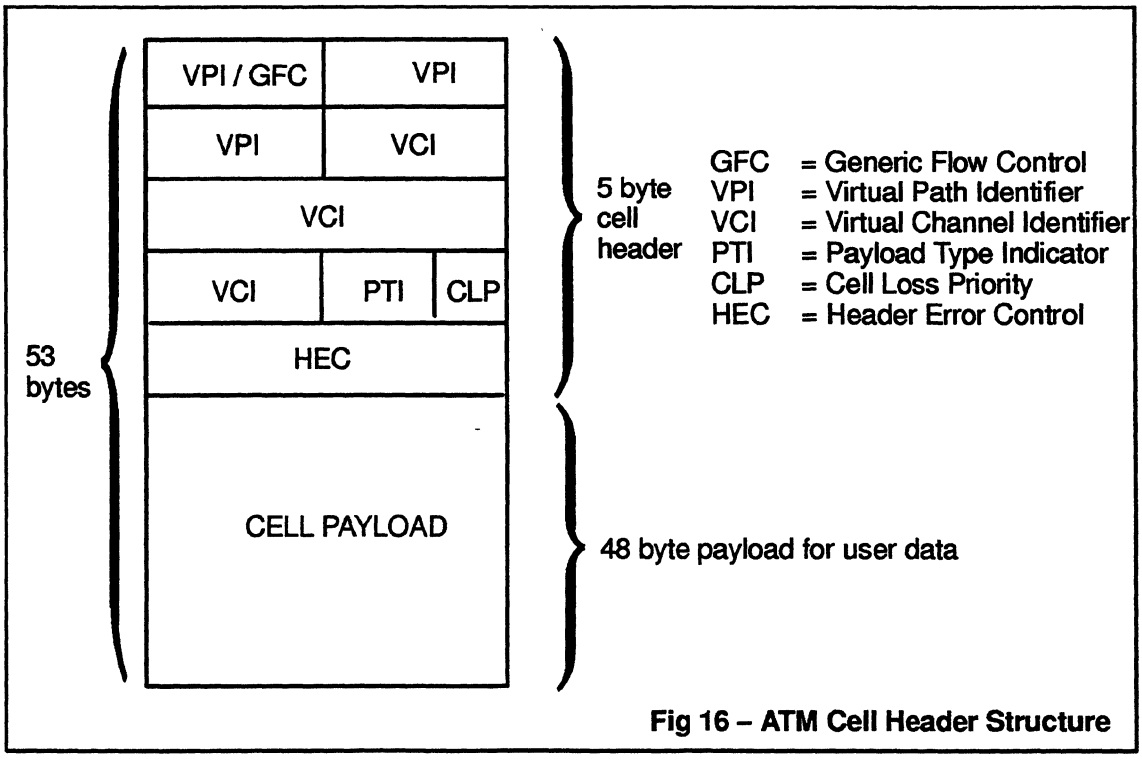
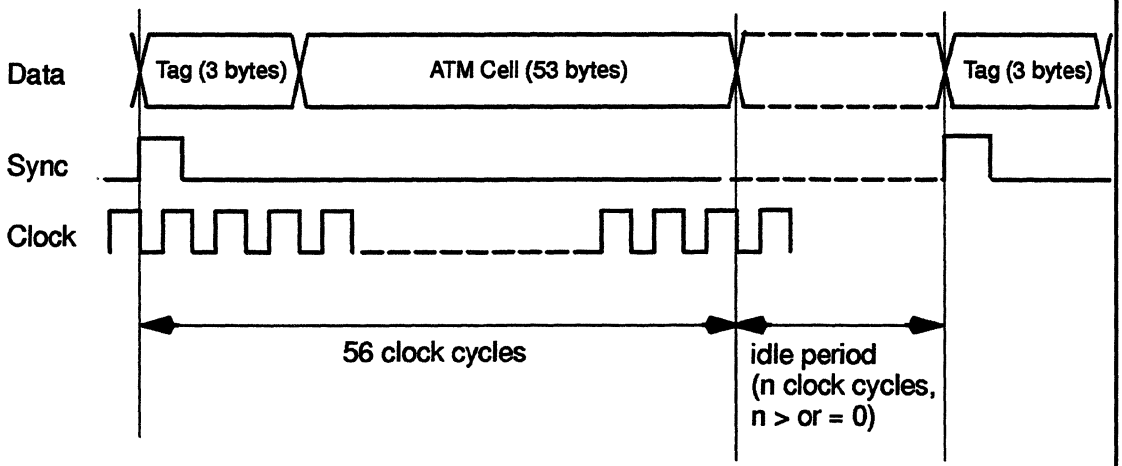
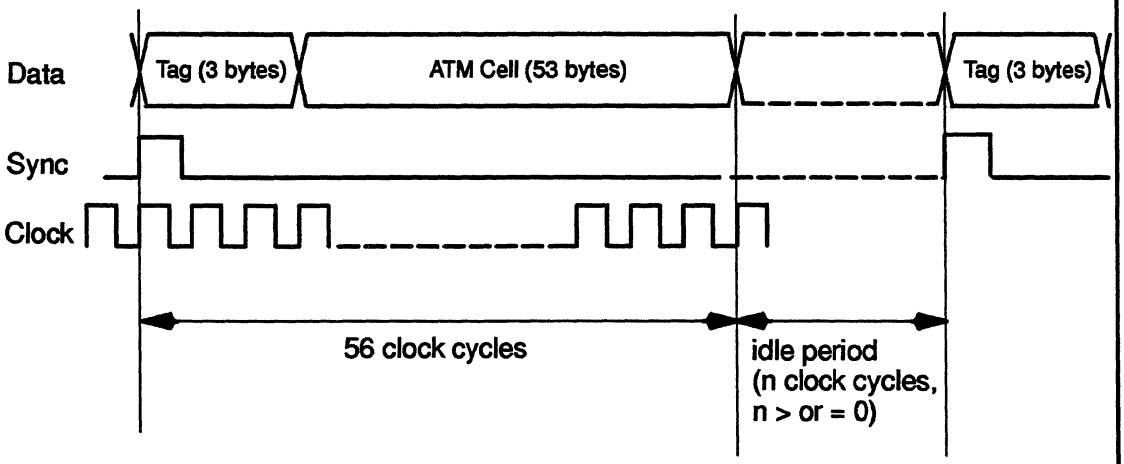


Fig 16 – ATM Cell Header Structure



a) Fujitsu Cell Stream Format



b) UTOPIA Cell Stream Format

Fig 17 – External Cell Stream Format

4.2. Switch Performance

4.2.1 Introduction

The overall performance of a switch fabric based on the SRE is dependent on a variety of factors, including interconnection topology and traffic characteristics. As a general guide, the switch performance of a typical matrix switch has been analysed and the cell loss rate calculated for various traffic loads. The performance is different for high and low priority channels.

A simulation software package is available from Fujitsu to allow users to analyse the performance of the switch for their own application. This allows any switch topology to be defined, and allows input traffic to be described in terms of a modified two state Markov model with programmable burst length, peak rate, and average rate.

4.2.2 Traffic Characteristics

For the purposes of switch performance analysis, various traffic types have been used with burst lengths in the range 1 to 24000 cells, peak rates in the range 16Kb/s to 140Mb/s, and average rates between 4Kb/s and 45Mb/s. Combinations of parameters have been selected to simulate the characteristics of various traffic types including LAN, Frame Relay, SMDS, image transfer, video, and voice.

4.2.3 High Priority Performance

The high priority channel performance has been analysed using an output load factor of approximately 0.9, but with high priority traffic accounting for around 30% of the total load. The traffic was based on a combination of voice and video data. Each input of a 32X32 switch was loaded with a variety of fixed and variable bit-rate voice and video data.

No cell loss was observed during the course of the simulations, which typically had a total cell transfer count of around 10^7. Moreover, since the high priority traffic had either a short burst length or low peak rate, it is predicted that the probability of cell loss in the high priority channel is very low, of the order of 10^{-12}. Also, the performance has been shown to be independent from the traffic applied to the low priority channel.

The peak delay associated with high priority traffic was observed to be less than one cell period. The corresponding peak delay for low priority traffic was observed to be in the range 20 - 30 cell periods.

4.2.4 Low Priority Performance

Analysis of the low priority channels assumes a total output load of 80% . The traffic load is assumed to be bursty. As expected, the switch was found to be sensitive to data having a long burst length and high peak rate. Clearly, such data will swamp the switch and cause a high cell loss rate.

A good cell loss rate (around $10^{-9)}$ was obtained by shaping either the burst length or peak rate. The longest burst length traffic was assumed to be image transfer data, with a burst length of 24000 cells. To avoid cell loss the peak rate for this type of data was set at 30Mb/s. For peak rates exceeding 100Mb/s the traffic was shaped with a burst length of 5 cells, and in this case a very low cell loss rate

was achieved, even with a high average data rate.

For general performance analysis a LAN hub model was constructed which comprised 15 multi-media workstations together with two server ports, each having an 80% output load. Each workstation was configured to transfer data to the server ports at an average rate of 10Mb/s and a peak rate of 100Mb/s, and the server was configured to send data to each workstation. In addition, bi-directional video and voice channels were set up between each workstation (assuming video at 10Mb/s), and image transfer operation were simulated between each workstation and the server. No cells were lost during the course of the simulation, which represented a transfer of around 10^7 cells. Extrapolating from this it seems reasonable to assume that a cell loss rate of around 1 in 10^9 would be achieved with this configuration.

It is also important to note that the matrix configuration is internally non-blocking. Therefore another possible scenario is to allocate server ports dynamically for maximum speed transfer between workstations and servers. In this case data could be transferred at 150Mb/s without causing any disruption to other traffic, due to the non-blocking nature of the matrix.

4.2.5 Conclusions

Simulation and analysis has shown that good performance can be obtained from the switch provided that certain characteristics of the input data are controlled. The most important factors are burst length and peak rate. It is recommended that data having a high peak rate and a long burst length is shaped prior to entry into the switch.

A. RATINGS

A.1 ABSOLUTE MAXIMUM RATINGS

Rating	symbol	Values		Units
		Min	Max	
Positive Supply Voltage	$+V_{DD}$	-0.5	6.0	V
Input Voltage	V_{DIN}	-0.5	$+V_{DD}$ + 0.5	V
Output Voltage	V_{O1}	-0.5	$+V_{DD}$ + 0.5	V
Input Current	I_{MAX}	-10.0	125	µA
Storage Temperature	T_{STG}	-40	125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this datasheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.2 DC CHARACTERISTICS

Parameter	Symbol	Pin	Test Condition	Value			Unit
				Min	Typ.	Max	
Positive Supply Voltage	V_{DD}		+4.75	+4.75	+5.0	+5.25	V
Positive Supply Current	$+I_{VS}$		Static no load	-	-	100	µA
Input High Voltage (TTL)	V_{IH}			2.2	-	$+V_{DD}$	V
Input Low Voltage (TTL)	V_{IL}			0	-	0.8	V
Input Leakage Current	I_L		$0<=V_I<=+V_{DD}$	-10	-	10	µA
Output Low Voltage	V_{OL}		I_{OL}=3.2mA	V_{SS}	-	0.4	V
Output High Voltage	V_{OH}		I_{OH}=-2mA	4.2	-	V_{DD}	V
Output Off Leakage Current	I_{LO}			-10	-	10	µA
Input Pin Capacitance	C_{in}			-	-	8	pF
Output Pin Capacitance	C_{out}			-	-	16	pF
I/O Pin Capacitance	$C_{i/o}$			-	-	21	pF
Operating Temperature	T_A			0	-	+70	°C
Power Dissipation (operating)	P_O				800		mW

B. AC CHARACTERISTICS

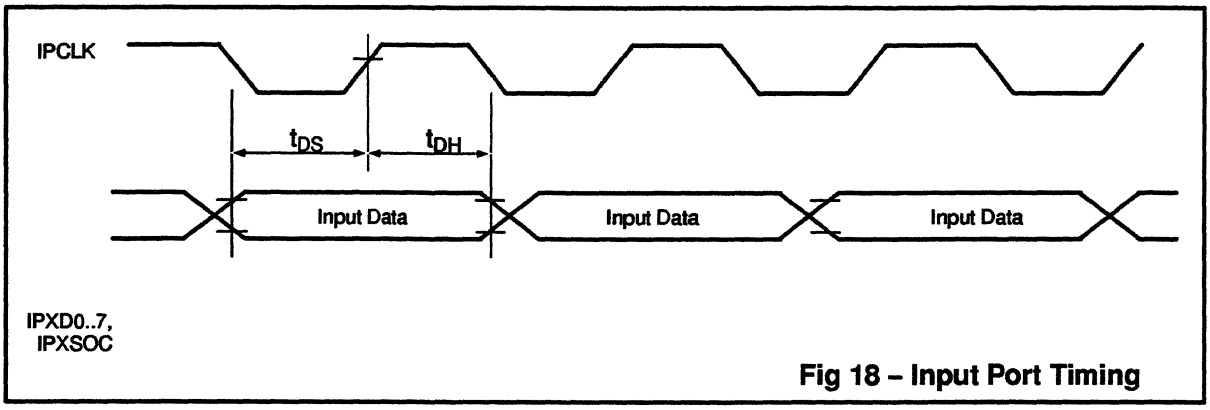


Fig 18 – Input Port Timing

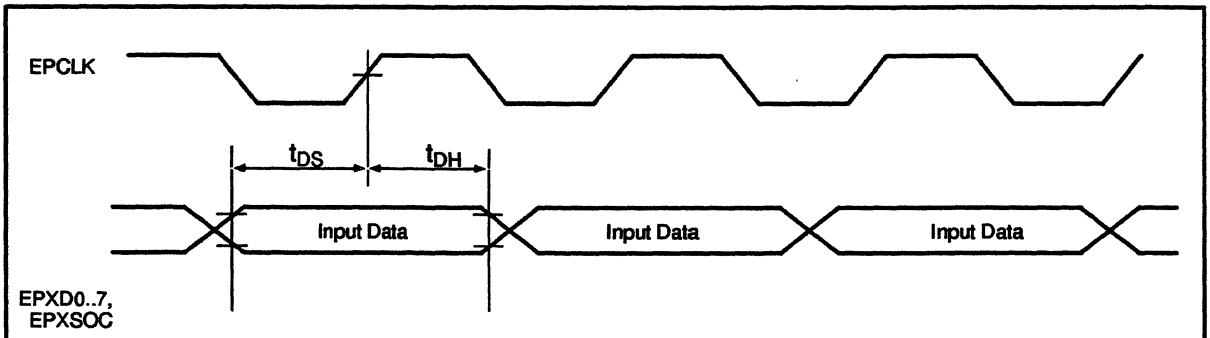


Fig 19 – Expansion Port Timing

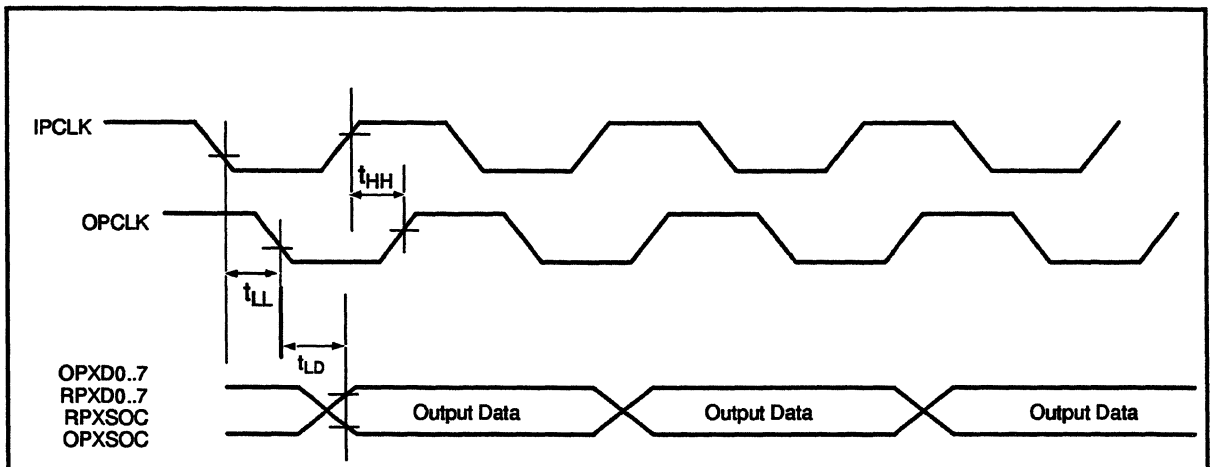


Fig 20 – Output Port Timing – Cell Stream Mode

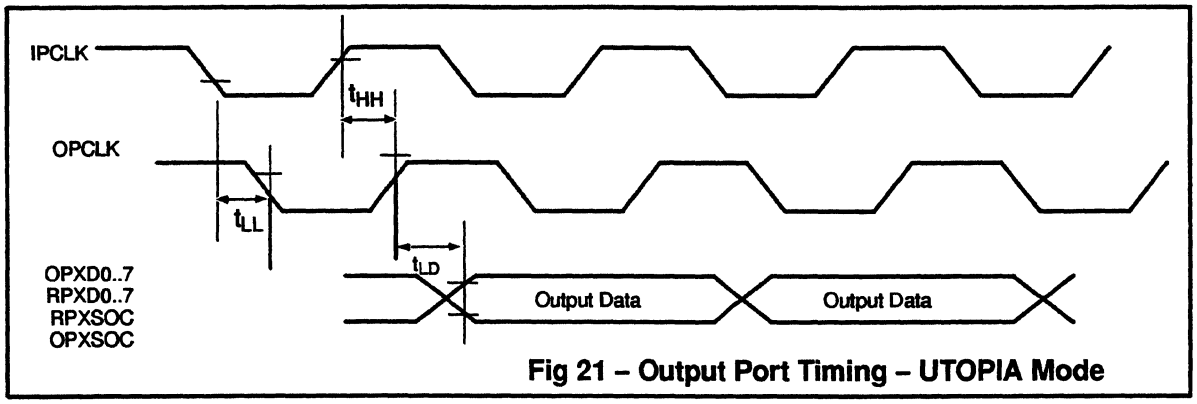


Fig 21 – Output Port Timing – UTOPIA Mode

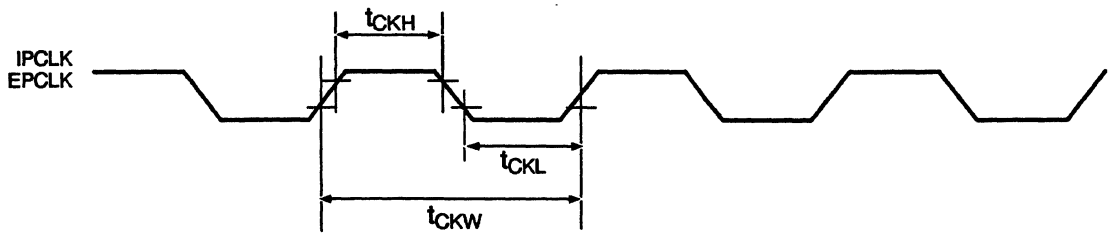
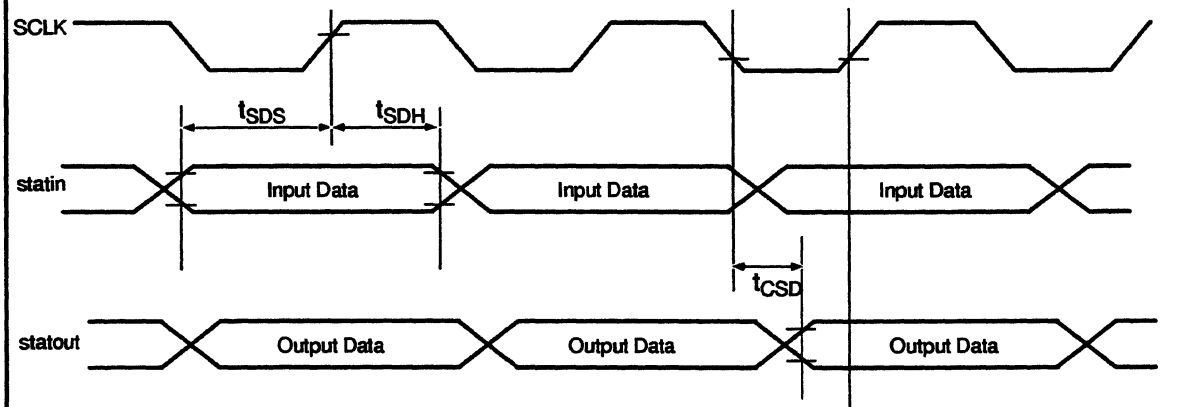
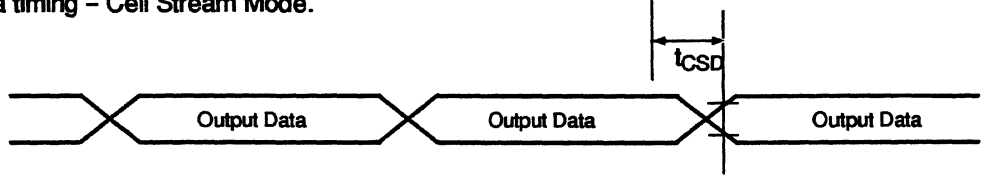


Fig 22 – Input Clock Timing



a) Output data timing – Cell Stream Mode.



b) Output data timing – UTOPIA Mode

Fig 23 – Statistics Timing

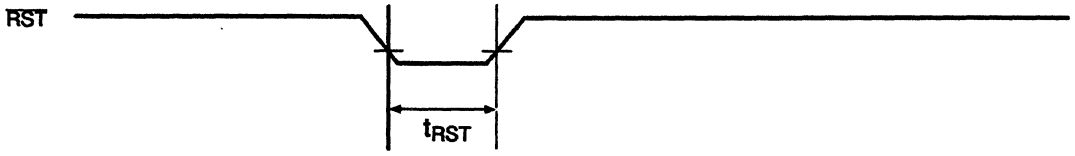


Fig 24 – Reset Timing

Parameter	Ref Signal	Abrev	Values			Units (ns)
			Min	Typ.	Max	
Input Data setup Time	IPCLK EPCLK	t_{DS}	5			ns
Input Data Hold Time	IPCLK EPCLK	t_{DH}	5			ns
Data Out Delay	OPCLK	t_{LD}			12	ns
IPCLK low to OPCLK low	IPCLK	t_{LL}			12	ns
IPCLK high to OPCLK high	IPCLK	t_{HH}			12	ns
Input Period Clock	IPCLK EPCLK	t_{CKW}	40			ns
Input Clock High Time	IPCLK EPCLK	t_{CKH}	20			ns
Input Clock Low Time	IPCLK EPCLK	t_{CKL}	20			ns
Statistics Data Setup Time	SCLK	t_{SDS}	5			ns
Statistics Data Hold Time	SCLK	t_{SDH}	5			ns
Statistics Out Delay	SCLK	t_{CSD}			15	ns
Reset Pulse Width	RESET	t_{RST}	30			ns

Note: These figures are not 100% tested. Guaranteed by design characterisation.

Table 4 – AC TIMING PARAMETERS

C. JTAG

C.1 JTAG Boundary Scan Cells

The Boundary Scan Register (BSR) consists of 154 registers, which form a serial shift register starting from pin 7 (OP1SOC), moving in a clockwise direction around the chip to finish at pin 48 (INITOUT).

It should be noted that none of the internal D-types which form the BSR are reset,and hence are initially undefined. A valid pattern needs to be shifted into the register prior to any testing. However, while the JTAG TAP controller is reset, the I/O pins are connected through to the system logic.

I / O Pin Type:

I = Input
C = Clock input
O = Output
B = Bidirectional,
T = Tristate
Iu = Input with pull-up resistor.

BSR Cell Type:

BSI1 allows capture of device input pin and control of logic input pin.
BSI3 allows capture of device input pin only.
BSO allows capture of logic output pin and control of device output pin (= BSI1).
BSOE allows control of tristate-able output pin (presettable).
BSDI allows control of bidirectional pin (= BSOE).
BSBI allows capture and control of bidirectional input and output pin (= BSI1 + BSO).

Control Group No.: Denotes a JTAG BSR cell which controls a (group of) tristate-able output(s) or bidirectional pin(s).

Controlled Group No.: Denotes a JTAG BSR cell which connects to a tristate-able output or bidirectional pin which is controlled by the JTAG BSR cell numbered in the previous column.

TABLE 5 – BOUNDARY SCAN

Pin No.	Pin Name	Pin Type	BSR Cell No.	BSR Cell Type	Control Group No.	Controlled Group No.
1	OP1DT0	O	9	BSO		
2	OP1DT1	O	8	BSO		
4	OP1DT2	O	7	BSO		
5	OP1DT3	O	6	BSO		
6	OP1DT4	O	5	BSO		
7	OP1SOC	O	1	BSO		
8	OP1DT5	O	4	BSO		
9	OP1DT6	O	3	BSO		
10	OP1DT7	O	2	BSO		
11	OP2DT0	O	18	BSO		
13	OP2DT1	O	17	BSO		
14	OP2DT2	O	16	BSO		
15	OP2DT3	O	15	BSO		
16	OP2DT4	O	14	BNSO		
17	OP2SOC	O	10	BSO		
18	OP2DT5	O	13	BSO		
19	OP2DT6	O	12	BSO		
20	OP2DT7	O	11	BSO		
21	OP3DT0	O	27	BSO		
23	OP3DT1	O	26	BSO		
24	OP3DT2	O	25	BSO		
25	OP3DT3	O	24	BSO		
26	OP3DT4	O	23	BSO		
27	OP3SOC	O	19	BSO		
28	OP3DT5	O	22	BSO		
29	OP3DT6	O	21	BSO		
30	OP3DT7	O	20	BSO		
31	OP4DT0	O	36	BSO		
33	OP4DT1	O	35	BSO		
34	OP4DT2	O	34	BSO		
35	OP4DT3	O	33	BSO		
36	OP4DT4	O	32	BSO		
37	OP4SOC	O	28	BSO		
38	OP4DT5	O	31	BSO		
39	OP4DT6	O	30	BSO		
40	OP4DT7	O	29	BSO		
41	TDO					
42	TDI					
43	TMS					
44	TCK					
45	STATSOUT	O	153	BSO		
46	OPCLK	O	152	BSO		
48	INITOUT	O	154	BSO		

Pin No.	Pin Name	Pin Type	BSR Cell No.	BSR Cell Type	Control Group No.	Controlled Group No.
49	RP4DT7	O	144	BSO		
50	RP4DT6	O	145	BSO		
51	RP4DT5	O	146	BSO		
52	RP4SOC	O	143	BSO		
53	RP4DT4	O	147	BSO		
54	RP4DT3	O	148	BSO		
55	RP4DT2	O	149	BSO		
57	RP4DT1	O	150	BSO		
58	RP4DT0	O	151	BSO		
59	RP3DT7	O	135	BSO		
60	RP3DT6	O	136	BSO		
61	RP3DT5	O	137	BSO		
62	RP3SOC	O	134	BSO		
63	RP3DT4	O	138	BSO		
64	RP3DT3	O	139	BSO		
65	RP3DT2	O	140	BSO		
67	RP3DT1	O	141	BSO		
68	RP3DT0	O	142	BSO		
69	RP2DT7	O	126	BSO		
70	RP2DT6	O	127	BSO		
71	RP2DT5	O	128	BSO		
72	RP2SOC	O	125	BSO		
73	RP2DT4	O	129	BSO		
74	RP2DT3	O	130	BSO		
75	RP2DT2	O	131	BSO		
77	RP2DT1	O	132	BSO		
78	RP2DT0	O	133	BSO		
79	RP1DT7	O	117	BSO		
80	RP1DT6	O	118	BSO		
81	RP1DT5	O	119	BSO		
82	RP1SOC	O	116	BSO		
83	RP1DT4	O	120	BSO		
84	RP1DT3	O	121	BSO		
85	RP1DT2	O	122	BSO		
87	RP1DT1	O	123	BSO		
88	RP1DT0	O	124	BSO		
89	INITIN	I	115	BSI1		
90	EP4DT7	I	104	BSI1		
92	EPCLK	C	112	BSI3		
93	EP4DT6	I	105	BSI1		
94	EP4DT5	I	106	BSI1		
95	EP4SOC	I	103	BSI1		
96	EP4DT4	I	107	BSI1		
97	EP4DT3	I	108	BSI1		
98	EP4DT2	I	109	BSI1		

Pin No.	Pin Name	Pin Type	BSR Cell No.	BSR Cell Type	Control Group No.	Controlled Group No.
99	EP4DT1	I	110	BSI1		
101	EP4DT0	I	111	BSI1		
102	EP3DT7/FCS	I	95	BSI1		
103	EP3DT6/TST3	I	96	BSI1		
104	EP3DT5/TST2	I	97	BSI1		
105	EP3SOC	I	94	BSI1		
106	EP3DT4/TST1	I	98	BSI1		
107	EP3DT3	I	99	BSI1		
108	EP3DT2	I	100	BSI1		
109	EP3DT1	I	101	BSI1		
111	$\overline{\text{RESET}}$	I	113	BSI1		
112	EP3DT0	I	102	BSI1		
113	EP2DT7/CA2	I	86	BSI1		
114	EP2DT6/CA1	I	87	BSI1		
115	EP2DT5/CA0	I	88	BSI1		
116	EP2SOC	I	85	BSI1		
117	EP2DT4/HPQE	I	89	BSI1		
118	EP2DT3/FECNE	I	90	BSI1		
119	EP2DT2/FECNT1	I	91	BSI1		
121	EP2DT1/FECNT0	I	92	BSI1		
122	EP2DT0	I	93	BSI1		
123	EP1DT7/AFS1	I	77	BSI1		
124	EP1DT6/AFS0	I	78	BSI1		
125	EP1DT5/AFL3	I	79	BSI1		
126	EP1SOC	I	76	BSI1		
127	EP1DT4/AFL2	I	80	BSI1		
128	EP1DT3/AFL1	I	81	BSI1		
129	EP1DT2/AFL0	I	82	BSI1		
130	EP1DT1	I	83	BSI1		
131	EP1DT0	I	84	BSI1		
132	STATSMS	I	114	BSI1		
133	IP1DT0	I	45	BSI1		
134	IP1DT1	I	44	BSI1		
136	IP1DT2	I	43	BSI1		
137	IP1DT3	I	42	BSI1		
138	IP1DT4	I	41	BSI1		
139	IP1SOC	I	37	BSI1		
140	IP1DT5	I	40	BSI1		
141	IP1DT6	I	39	BSI1		
142	IP1DT7	I	38	BSI1		
143	IP2DT0	I	54	BSI1		
145	IP2DT1	I	53	BSI1		
146	IP2DT2	I	52	BSI1		
147	IP2DT3	I	51	BSI1		
148	IP2DT4	I	50	BSI1		

Pin No.	Pin Name	Pin Type	BSR Cell No.	BSR Cell Type	Control Group No.	Controlled Group No.
149	IP2SOC	I	46	BSI1		
150	IP2DT5	I	49	BSI1		
151	IP2DT6	I	48	BSI1		
152	IP2DT7	I	47	BSI1		
153	IP3DT0	I	63	BSI1		
155	IP3DT1	I	62	BSI1		
156	IP3DT2	I	61	BSI1		
157	IP3DT3	I	60	BSI1		
158	IP3DT4	I	59	BSI1		
159	IP3SOC	I	55	BSI1		
160	IP3DT5	I	58	BSI1		
161	IP3DT6	I	57	BSI1		
162	IP3DT7	I	56	BSI1		
163	IP4DT0	I	72	BSI1		
165	IP4DT1	I	71	BSI1		
166	IP4DT2	I	70	BSI1		
167	IP4DT3	I	69	BSI1		
168	IP4DT4	I	68	BSI1		
169	IP4SOC	I	64	BSI1		
170	IP4DT5	I	67	BSI1		
171	IP4DT6	I	66	BSI1		
172	IP4DT7	I	65	BSI1		
173	SCLK	C	64	BSI3		
175	IPCLK	C	73	BSI3		
176	STATSIN	I	75	BSI1		
3	VSS					
12	VSS					
22	VDD					
32	VSS					
47	VSS					
56	VSS					
66	VDD					
76	VSS					
86	VDD					
91	VSS					
100	VSS					
110	VDD					
120	VSS					
135	VSS					
144	VSS					
154	VDD					
164	VSS					
174	VDD					

D. PIN ASSIGNMENTS

D.1. Pin Assignment

Fig. 25 below details the actual pin layout, whilst the table overleaf details the signals.

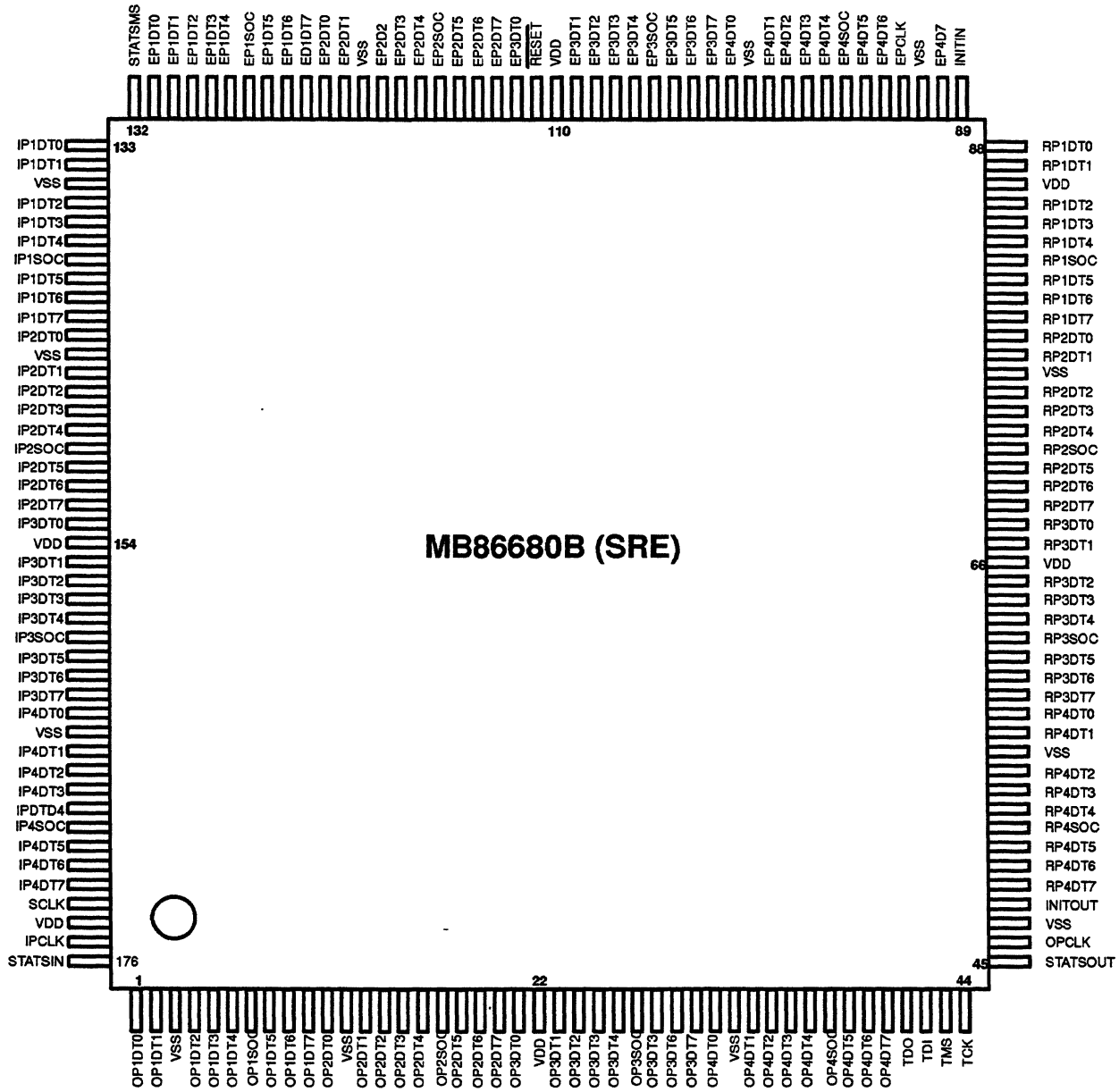


Fig. 25 Pin Assignment

Pin No	Name	Type	Function
1	OP1DT0	O	Output port 1, bit D0 (LSB)
2	OP1DT1	O	Output port 1, bit D1
3	VSS	-	
4	OP1DT2	O	Output port 1, bit D2
5	OP1DT3	O	Output port 1, bit D3
6	OP1DT4	O	Output port 1, bit D4
7	OP1SOC	O	Output port 1 Start Of Cell signal
8	OP1DT5	O	Output port 1, bit D5
9	OP1DT6	O	Output port 1, bit D6
10	OP1DT7	O	Output port 1, bit D7 (MSB)
11	OP2DT0	O	Output port 2, bit D0 (LSB)
12	VSS	-	
13	OP2DT1	O	Output port 2, bit D1
14	OP2DT2	O	Output port 2, bit D2
15	OP2DT3	O	Output port 2, bit D3
16	OP2DT4	O	Output port 2, bit D4
17	OP2SOC	O	Output port 2, Start Of Cell signal
18	OP2DT5	O	Output port 2, bit D5
19	OP2DT6	O	Output port 2, bit D6
20	OP3DT7	O	Output port 3, bit D7(MSB)
21	OP3DT0	O	Output port 3, bit D0
22	VDD	-	
23	OP3DT1	O	Output port 3, bit D1
24	OP3DT2	O	Output port 3, bit D2
25	OP3DT3	O	Output port 3, bit D3
26	OP3DT4	O	Output port 3, bit D4
27	OP3SOC	O	Output port 3 Start Of Cell signal
28	OP3DT5	O	Output port 3, bit D5
29	OP3DT6	O	Output port 3 bit D6
30	OP3DT7	O	Output port 3, bit D7 (MSB)
31	OP4DT0	O	Output port 4, bit D0 (LSB)
32	VSS	-	
33	OP4DT1	O	Output port 4, bit D1
34	OP4DT2	O	Output port 4, bit D2
35	OP4DT3	O	Output port 4, bit D3
36	OP4DT4	O	Output port 4, bit D4
37	OP4SOC	O	Output port 4 Start Of Cell signal
38	OP4DT5	O	Output port 4, bit D5
39	OP4DT6	O	Output port 4, bit D6
40	OP4DT7	O	Output port 4, bit D7 (MSB)
41	TDO	O	JTAG test data output
42	TDI	I	JTAG test data input
43	TMS	I	JTAG test mode select
44	TCK	I	JTAG test clock input

Pin No	Name	Type	Function
45	STATSOUT	O	Statistics output signal
46	OPCLK	O	Output clock signal
47	VSS	-	
48	INITOUT	O	Initialisation output signal
49	RP4DT7	O	Regeneration port 4, bit D7 (MSB)
50	RP4DT6	O	Regeneration port 4, bit D6
51	RP4DT5	O	Regeneration port 4, bit D5
52	RP4SOC	O	Regeneration port 4 Start Of Cell signal
53	RP4DT4	O	Regeneration port 4, bit D4
54	RP4DT3	O	Regeneration port 4, bit D3
55	RP4DT2	O	Regeneration port 4, bit D2
56	VSS	-	
57	RP4DT1	O	Regeneration port 4, bit D1
58	RP4DT0	O	Regeneration port 4, bit D0 (LSB)
59	RP3DT7	O	Regeneration port 3, bit D7 (MSB)
60	RP3DT6	O	Regeneration port 3, bit D6
61	RP3DT5	O	Regeneration port 3, bit D5
62	RP3SOC	O	Regeneration port 3 Start Of Cell signal
63	RP3DT4	O	Regeneration port 3, bit D4
64	RP3DT3	O	Regeneration port 3, bit D3
65	RP3DT2	O	Regeneration port 3, bit D2
66	VDD	-	
67	RP3DT1	O	Regeneration port 3, bit D1
68	RP3DT0	O	Regeneration port 3 , bit D0
69	RP2DT7	O	Regeneration port 2, bit D7 (MSB)
70	RP2DT6	O	Regeneration port 2, bit D6
71	RP2DT5	O	Regeneration port 2, bit D5
72	RP2SOC	O	Regeneration port 2 Start Of Cell signal
73	RP2DT4	O	Regeneration port 2, bit D4
74	RP2DT3	O	Regeneration port 2, bit D3
75	RP2DT2	O	Regeneration port 2, bit D2
76	VSS	-	
77	RP2DT1	O	Regeneration port 2, bit D1
78	RP2DT0	O	Regeneration port 2, bit D0 (LSB)
79	RP1DT7	O	Regeneration port 1, bit D7
80	RP1DT6	O	Regeneration port 1, bit D6
81	RP1DT5	O	Regeneration port 1, bit D5
82	RP1SOC	O	Regeneration port 1 Start Of Cell signal
83	RP1DT4	O	Regeneration port 1, bit D4
84	RP1DT3	O	Regeneration port 1, bit D3
85	RP1DT2	O	Regeneration port 1, bit D2
86	VDD	-	
87	RP1DT1	O	Regeneration port 1, bit D1
88	RP1DT0	O	Regeneration port 1, bit D0 (LSB)

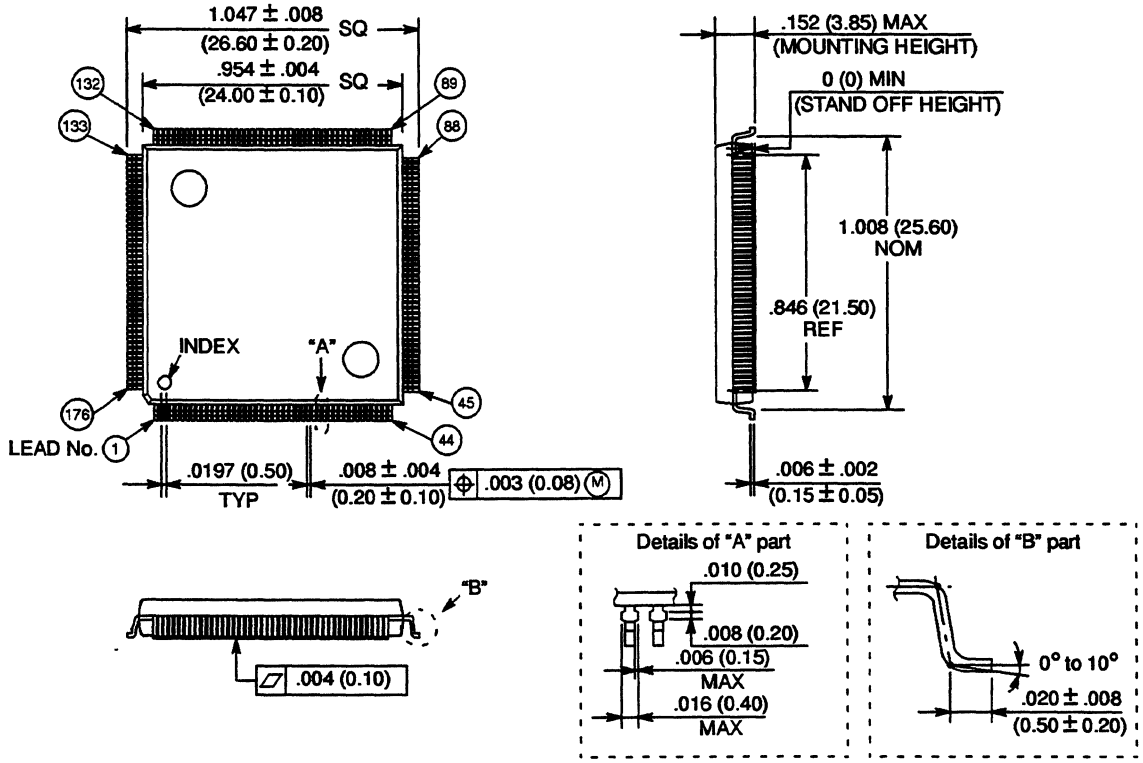
Pin No	Name	Type	Function
89	INITIN	I	Initialisation input signal
90	EP4DT7	I	Expansion port 4, bit D7 (MSB)
91	VSS	-	
92	EPCLK	I	Expansion port clock signal
93	EP4DT6	I	Expansion port 4, bit D6
94	EP4DT5	I	Expansion port 4, bit D5
95	EP4SOC	I	Expansion port 4 Start Of Cell signal
96	EP4DT4	I	Expansion port 4, bit D4
97	EP4DT3	I	Expansion port 4, bit D3
98	EP4DT2	I	Expansion port 4, bit D2
99	EP4DT1	I	Expansion port 4, bit D1
100	VSS	-	
101	EP4DT0	I	Expansion port 4, bit D0 (LSB)
102	EP3DT7/FCS	I	Expansion port 3, bit D7 (MSB)
103	EP3DT6/TST3	I	Expansion port 3, bit D6
104	EP3DT5/TST2	I	Expansion port 3, bit D5
105	EP3SOC	I	Expansion port 3 Start Of Cell signal
106	EP3DT4/TST1	I	Expansion port 3, bit D4
107	EP3DT3	I	Expansion port 3, bit D3
108	EP3DT2	I	Expansion port 3, bit D2
109	EP3DT1	I	Expansion port 3, bit D1
110	VDD	-	
111	$\overline{\text{RESET}}$	I	Switch reset signal
112	EP3DT0	I	Expansion port 3, bit D0 (LSB)
113	EP2DT7/CA2	I	Expansion port 2, bit D7 (MSB)
114	EP2DT6/CA1	I	Expansion port 2, bit D6
115	EP2DT5/CA0	I	Expansion port 2, bit D5
116	EP2SOC	I	Expansion port 2 Start Of Cell signal
117	EP2DT4/HPQE	I	Expansion port 2, bit D4
118	EP2DT3/FECNE	I	Expansion port 2, bit D3
119	EP2DT2/FECNT1	I	Expansion port 2, bit D2
120	VSS	-	
121	EP2DT1/FECNT0	I	Expansion port 2, bit D1
122	EP2DT0	I	Expansion port 2, bit D0 (LSB)
123	EP1DT7/AFS1	I	Expansion port 1, bit D7 (MSB)
124	EP1DT6/AFS0	I	Expansion port 1, bit D6
125	EP1DT5/AFL3	I	Expansion port 1, bit D5
126	EP1SOC	I	Expansion port 1 Start Of Cell signal
127	EP1DT4/AFL2	I	Expansion port 1, bit D4
128	EP1DT3/AFL1	I	Expansion port 1, bit D3
129	EP1DT2/AFL0	I	Expansion port 1, bit D2
130	EP1DT1	I	Expansion port 1, bit D1
131	EP1DT0	I	Expansion port 1, bit D0 (LSB)
132	STATSMS	I	Statistics master / slave select

Pin No	Name	Type	Function
133	IP1DT0	I	Input port 1, bit D0 (LSB)
134	IP1DT1	I	Input port 1, bit D1
135	VSS	-	
136	IP1DT2	I	Input port 1, bit D2
137	IP1DT3	I	Input port 1, bit D3
138	IP1DT4	I	Input port 1, bit D4
139	IP1SOC	I	Input port 1 Start Of Cell signal
140	IP1DT5	I	Input port 1, bit D5
141	IP1DT6	I	Input port 1, bit D6
142	IP1DT7	I	Input port 1, bit D7 (MSB)
143	IP2DT0	I	Input port 2, bit D0 (LSB)
144	VSS	-	
145	IP2DT1	I	Input port 2, bit D1
146	IP2DT2	I	Input port 2, bit D2
147	IP2DT3	I	Input port 2, bit D3
148	IP2DT4	I	Input port 2, bit D4
149	IP2SOC	I	Input port 2 Start Of Cell signal
150	IP2DT5	I	Input port 2, bit D5
151	IP2DT6	I	Input port 2, bit D6
152	IP2DT7	I	Input port 2, bit D7 (MSB)
153	IP3DT0	I	Input port 3, bit D0 (LSB)
154	VDD	-	
155	IP3DT1	I	Input port 3, data bit D1
156	IP3DT2	I	Input port 3, data bit D2
157	IP3DT3	I	Input port 3, data bit D3
158	IP3DT4	I	Input port 3, data bit D4
159	IP3SOC	I	Input port 3 Start Of Cell signal
160	IP3DT5	I	Input port 3, data bit D5
161	IP3DT6	I	Input port 3, data bit D6
162	IP3DT7	I	Input port 3, data bit D7 (MSB)
163	IP4DT0	I	Input port 4, data bit D0 (LSB)
164	VSS	-	
165	IP4DT1	I	Input port 4, data bit D1
166	IP4DT2	I	Input port 4, data bit D2
167	IP4DT3	I	Input port 4, data bit D3
168	IP4DT4	I	Input port 4, data bit D4
169	IP4SOC	I	Input port 4 Start Of Cell signal
170	IP4DT5	I	Input port 4, data bit D5
171	IP4DT6	I	Input port 4, data bit D6
172	IP4DT7	I	Input port 4, data bit D7 (MSB)
173	SCLK	I	Statistics clock signal
174	VDD	-	
175	IPCLK	I	Input clock signal
176	STATSIN	I	Statistics input signal

E – PACKAGE DIMENSIONS

FPT-176P-M01

176-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-176P-M01)



Dimensions in
inches (millimeters)