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ENHANCEMENT SUMMARY

Network Termination Controller (NTC)

MB86683/MB86683A

Edition 1.0, May 1994

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1. INTRODUCTION

1.1. Document Change History

Issue 0.1, first draft by Steve Dabecki, Jan 10th 1993.

Issue 0.2, added extra functionality and expanded some sections, Mar 1st 1994.

Edition 1.0, modified sections and redefined the UTOPIA interface, May 27th 1994.

1.2. Purpose of Document

This document details both the hardware and functional changes between the engineering sample version of the Network Termination Controller (NTC), and the production version of this device. These two parts have the chip numbers MB86683 and MB86683A respectively.

This document should be read in conjunction with the latest version of the NTC datasheet (Edition 1.0 October 1993).

1.3. Disclosure

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical applications. Complete information sufficient for construction purposes is not necessarily given.

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2. HARDWARE CHANGES

2.1. Summary

The main hardware changes between the two devices has been the addition of 9 signal pins. The purpose of these pins can be summarised in 4 ways :-

1. Addition of JTAG test pins :	TDO	(pin 132)
	TDI	(pin 131)
	TMS	(pin 130)
	TCK	(pin 129)
2. Additional system clock pin :	DCLK	(pin 61)
	CLKSEL	(pin 62)
3. Increased functionality of the Cell Stream :	CS/$\overline{UT}$	(pin 64)
4. Additional microprocessor pins :	$\overline{BCLR}$	(pin 173)
	$\overline{BERR}$	(pin 124)

Also, one pin name has been changed to improve clarity.
Pin DCOUT/$\overline{DCOUT}$ (pin 169), has been renamed to DCOUT/$\overline{BGOUT}$.
BGOUT is an abbreviation for Bus Grant Out, and is used in conjunction with the Bus Grant (BG) signal in MOTOROLA mode.

It should be noted that use of internal pull-up resistors on some of these pins ensures that the MB86683A is backwardly compatible.

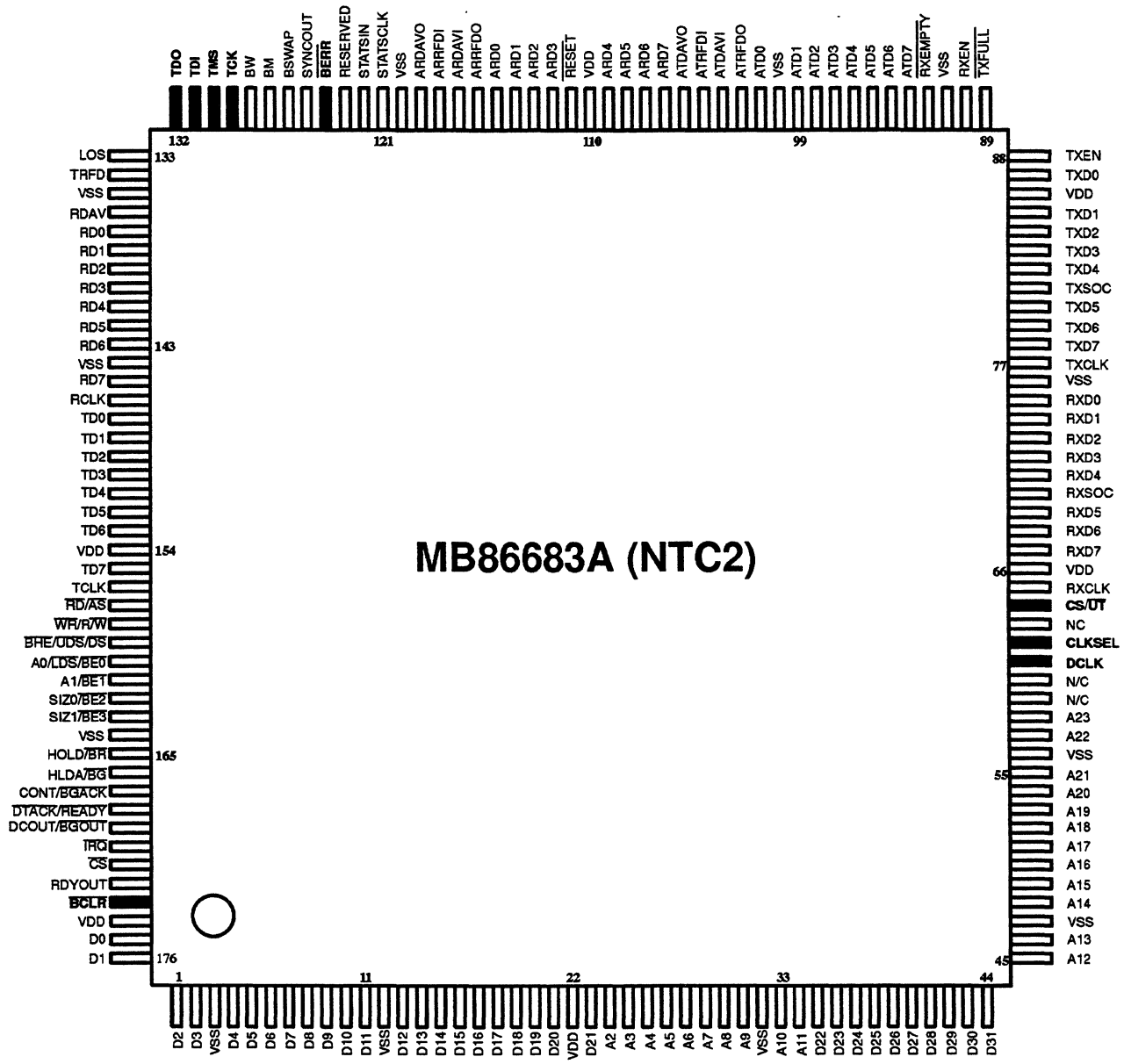
The following pins have internal pull-up resistors :-

CLKSEL, CS/$\overline{UT}$, $\overline{BCLR}$, $\overline{BERR}$.

The additional pins are highlighted in bold in the following pin assignment diagram. The pins are also shaded for clarity.

Further explanation of these signals follow the pin assignment diagram.

2.2. Pin Assignment



2.3. JTAG Test Port

MB86683A now contains Boundary Scan Test Circuitry compliant with IEEE 1149.1 (JTAG). This requires the addition of the 4 pins described earlier. The JTAG circuitry is internally reset at power on, and hence the optional JTAG reset pin (TRST) is not required.

The JTAG circuitry allows easier board level testing by allowing the signal pins on the device to form a serial scan chain around the device. The test modes are controlled by accessing an internal Test Access Port Controller (TAP), which is in turn controlled from the TAP.

The Boundary Scan Register (BSR) consists of 223 registers, which form a serial shift register starting from pin 133 (LOS), moving in a anti-clockwise direction around the chip to finish at pin 128 (BW).

It should be noted that none of the internal D-types which form the BSR are reset,and hence are initially undefined. A valid pattern needs to be shifted into the register prior to any testing. However, while the JTAG TAP controller is reset, the I/O pins are connected through to the system logic.

A detailed explanation of the scan chain is given in the following tables, and uses the following key :-

Pin Type : I = Input, C = Clock input, O = Output, B = Bidirectional, T = Tristate, Iu = Input with pull-up resistor.

BSR Cell Type : BSI1 allows capture of device input pin and control of logic input pin.
BSI3 allows capture of device input pin only.
BSO allows capture of logic output pin and control of device output pin (= BSI1).
BSOE allows control of tristate-able output pin.
BSDI allows control of bidirectional pin (= BSOE).
BSBI allows capture and control of bidirectional input and output pin (= BSI1 + BSO).

Control Group No. : Denotes a JTAG BSR cell which controls a (group of) tristate-able output(s) or bidirectional pin(s).

Controlled Group No. : Denotes a JTAG BSR cell which connects to a tristate-able output or bidirectional pin which is controlled by the JTAG BSR cell numbered in the previous column.

BSR Cell No.	BSR Cell Type	Control Group No.	Controlled Group No.	Pin Type	Pin No.	Pin Name
1	BSI1			I	133	LOS
2	BSI1			I	134	TRFD
3	BSI1			I	136	RDAV
4	BSI1			I	137	RD0
5	BSI1			I	138	RD1
6	BSI1			I	139	RD2
7	BSI1			I	140	RD3
8	BSI1			I	141	RD4
9	BSI1			I	142	RD5
10	BSI1			I	143	RD6
11	BSI1			I	145	RD7
12	BSI3			C	146	RCLK
13	BSO			O	147	TD0
14	BSO			O	148	TD1
15	BSO			O	149	TD2
16	BSO			O	150	TD3
17	BSO			O	151	TD4
18	BSO			O	152	TD5
19	BSO			O	153	TD6
20	BSO			O	155	TD7
21	BSI3			C	156	TCLK
22	BSDI	1				
23 & 24	BSBI		1	B	157	$\overline{RD}$ / $\overline{AS}$
25 & 26	BSBI		1	B	158	$\overline{WR}$ / R/$\overline{W}$
27	BSDI	2				
28 & 29	BSBI		2	B	159	$\overline{BHE}$ / $\overline{UDS}$ / $\overline{DS}$
30 & 31	BSBI		1	B	160	A0 / $\overline{LDS}$ / $\overline{BE0}$
32 & 33	BSBI		1	B	161	A1 / $\overline{BE1}$
34	BSDI	3				
35 & 36	BSBI		3	B	162	SIZ0 / $\overline{BE2}$
37 & 38	BSBI		3	B	163	SIZ1 / $\overline{BE3}$
39	BSDI	4				
40 & 41	BSBI		4	B	165	HOLD / $\overline{BR}$
42	BSI1			I	166	HLDA / $\overline{BG}$
43	BSDI	5				
44 & 45	BSBI		5	B	167	CONT / $\overline{BGACK}$
46	BSI1			I	168	$\overline{DTACK}$ / $\overline{READY}$
47	BSOE	6				
48	BSO		6	T	169	DCOUT / $\overline{BGOUT}$
49	BSOE	7				
50	BSO		7	T	170	$\overline{IRQ}$

BSR Cell No.	BSR Cell Type	Control Group No.	Controlled Group No.	Pin Type	Pin No.	Pin Name
51	BSI1			I	171	$\overline{CS}$
52	BSO			O	172	RDYOUT
53	BSI1			I	173	$\overline{BCLR}$
54	BSDI	8				
55 & 56	BSBI		8	B	175	D0
57 & 58	BSBI		8	B	176	D1
59 & 60	BSBI		8	B	1	D2
61 & 62	BSBI		8	B	2	D3
63 & 64	BSBI		8	B	4	D4
65 & 66	BSBI		8	B	5	D5
67 & 68	BSBI		8	B	6	D6
69 & 70	BSBI		8	B	7	D7
71 & 72	BSBI		8	B	8	D8
73 & 74	BSBI		8	B	9	D9
75 & 76	BSBI		8	B	10	D10
77 & 78	BSBI		8	B	11	D11
79 & 80	BSBI		8	B	13	D12
81 & 82	BSBI		8	B	14	D13
83 & 84	BSBI		8	B	15	D14
85 & 86	BSBI		8	B	16	D15
87	BSDI	9				
88 & 89	BSBI		9	B	17	D16
90 & 91	BSBI		9	B	18	D17
92 & 93	BSBI		9	B	19	D18
94 & 95	BSBI		9	B	20	D19
96 & 97	BSBI		9	B	21	D20
98 & 99	BSBI		9	B	23	D21
100 & 101	BSBI		1	B	24	A2
102 & 103	BSBI		1	B	25	A3
104 & 105	BSBI		1	B	26	A4
106 & 107	BSBI		1	B	27	A5
108 & 109	BSBI		1	B	28	A6
110	BSO		1	T	29	A7
111	BSO		1	T	30	A8
112	BSO		1	T	31	A9
113	BSO		1	T	33	A10
114	BSO		1	T	34	A11
115 & 116	BSBI		9	B	35	D22
117 & 118	BSBI		9	B	36	D23
119 & 120	BSBI		9	B	37	D24
121 & 122	BSBI		9	B	38	D25
123 & 124	BSBI		9	B	39	D26

BSR Cell No.	BSR Cell Type	Control Group No.	Controlled Group No.	Pin Type	Pin No.	Pin Name
125 & 126	BSBI		9	B	40	D27
127 & 128	BSBI		9	B	41	D28
129 & 130	BSBI		9	B	42	D29
131 & 132	BSBI		9	B	43	D30
133 & 134	BSBI		9	B	44	D31
135	BSO		1	T	45	A12
136	BSO		1	T	46	A13
137	BSO		1	T	48	A14
138	BSO		1	T	49	A15
139	BSO		1	T	50	A16
140	BSO		1	T	51	A17
141	BSO		1	T	52	A18
142	BSO		1	T	53	A19
143	BSO		1	T	54	A20
144	BSO		1	T	55	A21
145	BSO		1	T	57	A22
146	BSO		1	T	58	A23
147	BSI3			C	61	DCLK
148	BSI1			Iu	62	CLKSEL
149	BSI1			Iu	64	CS / $\overline{UT}$
150	BSI3			C	65	RXCLK
151	BSO			O	67	RXD7
152	BSO			O	68	RXD6
153	BSO			O	69	RXD5
154	BSO			O	70	RXSOC
155	BSO			O	71	RXD4
156	BSO			O	72	RXD3
157	BSO			O	73	RXD2
158	BSO			O	74	RXD1
159	BSO			O	75	RXD0
160	BSI3			C	77	TXCLK
161	BSI1			I	78	TXD7
162	BSI1			I	79	TXD6
163	BSI1			I	80	TXD5
164	BSI1			I	81	TXSOC
165	BSI1			I	82	TXD4
166	BSI1			I	83	TXD3
167	BSI1			I	84	TXD2
168	BSI1			I	85	TXD1
169	BSI1			I	87	TXD0
170	BSI1			I	88	TXEN

BSR Cell No.	BSR Cell Type	Control Group No.	Controlled Group No.	Pin Type	Pin No.	Pin Name
171	BSO			O	89	TXFULL
172	BSI1			I	90	RXEN
173	BSO			O	92	RXEMPTY
174	BSDI	10				
175 & 176	BSBI		10	B	93	ATD7
177 & 178	BSBI		10	B	94	ATD6
179 & 180	BSBI		10	B	95	ATD5
181 & 182	BSBI		10	B	96	ATD4
183 & 184	BSBI		10	B	97	ATD3
185 & 186	BSBI		10	B	98	ATD2
187 & 188	BSBI		10	B	99	ATD1
189 & 190	BSBI		10	B	101	ATD0
191	BSO			O	102	ATRFDO
192	BSI1			I	103	ATDAVI
193	BSI1			I	104	ATRFDI
194	BSO			O	105	ATDAVO
195	BSDI	11				
196 & 197	BSBI		11	B	106	ARD7
198 & 199	BSBI		11	B	107	ARD6
200 & 201	BSBI		11	B	108	ARD5
202 & 203	BSBI		11	B	109	ARD4
204	BSI1			I	111	RESET
205 & 206	BSBI		11	B	112	ARD3
207 & 208	BSBI		11	B	113	ARD2
209 & 210	BSBI		11	B	114	ARD1
211 & 212	BSBI		11	B	115	ARD0
213	BSO			O	116	ARRFDO
214	BSI1			I	117	ARDAVI
215	BSI1			I	118	ARRFDI
216	BSO			O	119	ARDAVO
217	BSI3			C	121	STATSCLK
218	BSI1			I	122	STATSIN
219	BSI1			I	124	BERR
220	BSO			O	125	SYNCOUT
221	BSI1			I	126	BSWAP
222	BSI1			I	127	BM
223	BSI1			I	128	BW
				C	129	TCK
				I	130	TMS
				I	131	TDI
				T	132	TDO

BSR Cell No.	BSR Cell Type	Control Group No.	Controlled Group No.	Pin Type	Pin No.	Pin Name
					3	V_{SS}
					12	V_{SS}
					32	V_{SS}
					47	V_{SS}
					56	V_{SS}
					76	V_{SS}
					91	V_{SS}
					100	V_{SS}
					120	V_{SS}
					135	V_{SS}
					144	V_{SS}
					164	V_{SS}
					22	V_{DD}
					66	V_{DD}
					86	V_{DD}
					110	V_{DD}
					154	V_{DD}
					174	V_{DD}
					59	N/C
					60	N/C
					63	N/C
					123	N/C

2.4. System Clock

In MB86683, the system clock pin is RXCLK. This pin is also used as the Cell Stream Interface (CSI) receive clock. The CSI should typically be clocked at 20MHz to support a maximum data rate of 160Mbps across this interface.
This rate would then support the 155.52Mbps (19.44 MHz byte clock) at the transceiver interface.
There may be cases where it is desirable to use a CSI clock of less than 20MHz, in a case where the transceiver interface data rate is considerably lower than 155Mbps, eg E3 framing mode at 34Mbps.

If the RXCLK frequency was lowered in this case, then this would reduce the internal operating speed of the device, and hence all DMA transfers will be proportionately slower.

In MB86683A, an extra pin has been added which may be used as the system clock instead of RXCLK. This clock is called DCLK, and may be derived directly from the processor clock.

Selection of the system clock is done by tying CLKSEL (clock select) pin either high or low. This pin has an internal pull-up resistor, which selects RXCLK by default, to ensure backward compatibility.

Hence,

- to select DCLK as the system clock : connect CLKSEL pin to VSS.
- to select RXCLK as the system clock : leave CLKSEL unconnected.

2.5. Cell Stream Interface

The Cell Stream Interface (CSI) provides access to higher layers in the ATM protocol stack. Data across this interface is byte based, but a cell synchronisation signal is provided to give information on the cell boundary. Furthermore, two extra signals are provided to support flow control between the NTC and any other external device supporting a similar scheme. This device may be a Fujitsu Adaptation Layer Controller (ALC), a FIFO used to increase the buffering at this layer, or any other similar device.

The additional signal CS/$\overline{UT}$ has been added (at pin 64) to give greater flexibility when connecting the NTC to such devices. This interface may be configured as either a standard Cell Stream interface, or as an interface compatible with that defined in the document :

"Utopia, an ATM-PHY Interface Specification"
Level 1, Version 2.01
Version 2.0
March 21, 1994.

The CS/$\overline{UT}$ pin has an internal pull-up resistor, and may be left unconnected for backward compatibility to the MB86683 (i.e. a logic "1" on this pin specifies the Cell Stream interface : a logic "0" specifies the Utopia interface).

The differences between the Cell Stream interface specification and the Utopia interface specification are as follows :-

1. Output signal changes occur on different clock edges (Cell Stream on falling edge, Utopia on rising edge).

2. Some flow control signals have different polarities (Cell Stream TXEN & RXEN are active high, Utopia $\overline{TXEN}$ & $\overline{RXEN}$ are active low).

3. Backward flow control applies to next transfer in Cell Stream and to next edge in Utopia. This is further modified in Utopia by provision of a four-transfer lookahead only on the transmit side (i.e. $\overline{TXFULL}$ is asserted when five (5) more transfers after the current cycle will cause buffer overrun and data loss) .

4. The Cell Stream interface includes the data format in the specification, because it has to define the routing tag applied to the front of cells going to the MB86680 SRE device. Utopia has no current specification of the data format.

The only aspect of Utopia which the NTC does not support is the tri-stating of the RXD & RXSOC outputs under the control of the $\overline{RXEN}$ input.

2.6. Microprocessor Interface

The microprocessor interface has two additional pins, namely $\overline{\text{BCLR}}$ and $\overline{\text{BERR}}$. Both signals are active low inputs, and have internal pull-up resistors to allow backward compatibility with MB86683.

$\overline{\text{BCLR}}$ (Bus Clear) :

This signal may be asserted by the control processor to gain control of the system bus by suspending any NTC DMA transfer.
The NTC will release the bus and any DMA transfer will be internally suspended. The NTC DMA controller will then re-request the bus, and once the bus has been granted, the DMA transfer will resume.

$\overline{\text{BERR}}$ (Bus Error) :

This signal may be asserted by the control processor to abort any DMA transfer. This would normally be done if the NTC should hold the bus greater than a set time. This may occur if the DMA descriptors have been incorrectly programmed and the NTC is trying to access invalid memory, and hence a $\overline{\text{DTACK/READY}}$ signal will never be generated. On detecting this active signal, the NTC will release the bus and any DMA transfer will be internally aborted.
An interrupt may also be generated by enabling the BERR interrupt in CR58.
On receiving this interrupt, the processor may then read SR63 which will indicate which DMA channel was active when the DMA aborted.

3. FUNCTIONAL CHANGES

There have been many functional improvements applied to the production version of the NTC (MB86683A). Some of these functionality improvements have been achieved by hardware changes described earlier.

These functionality improvements may be summarised as follows :-

3.1. Receive / Transmit Framer

1. STS-1 framing mode (in accordance with proposed addition to ATM Forum UNI specification).
2. Support for DS-3 using non PLCP framing.
3. Additional support for DS-3 OAM using C-bit parity.
4. Microprocessor full-duplex access to 5 C-bits. (Provides AIC, FEAC and DL support).
5. SYNCOUT output now provides frame sync indication when in framed modes. Still provides cell sync indication in unframed mode.
6. Option to invert any of the transmitted BIP values (B1,B2,B3) for test purposes.

3.2. Network Statistics Record

1. Improved statistics recording for ATM Forum UNI MIB support.
2. NSR now contains 32-bit counts for; total cells received and not dropped (R count), total cells received and dropped (D count), and total cells transmitted (T count).
3. NSR table selectable as either header only, header plus 16 user entries, or header plus 32 user entries.
4. Optional filtering of user statistics including "0,1 or X" bits over all 28 bits of the VP/VC fields. Allows a range of VP/VCs to monitored.
5. Filter may be set to either filter user cells defined by the mask, or not defined by the mask, or it may be disabled completely.
6. Optionally disable either of the automatic DMA transfer events, namely counter overflow, or programmable timer.
7. Optionally force DMA transfer, independent of automatic events.
8. Cell Insert counts in NSR header changed to ATE counts for both RX and TX paths.
9. User Cell counts recorded before address translation in RX path, and after address translation in TX path.
10. Unassigned Cell counts recorded after address translation in both RX and TX cases.
11. TXATE count on a per VP/VC basis has been deleted from the NSR.
12. Idle counts deleted (RX and TX), but indirectly available.

3.2.1. Network Statistics – further details

The addition of the three 32-bit counters will allow added support for the UNI MIB specification. The conditions for which these counters are incremented are described as follows :

R-count : Total number of assigned ATM layer cells received at the transceiver receive interface that have not been discarded.

These cells will emerge from the cell stream receive interface, unless they are discarded due to an address translation error, if the RXATE bit is set to discard. They will not emerge if overwritten due to inserted cells having priority.
The R-count will still be incremented, even if the cell is discarded due to an address translation error.
This count will not include cells that have been inserted via the insert buffer in the receive path.

D-count : Total number of cells received at the transceiver receive interface that have been discarded.

The cells may have been discarded due to the following reasons :-

- physical layer cells
- ATM layer cell with uncorrectable HEC error
- ATM layer cell which has been discarded via the discard mask

T-count : Total number of assigned ATM layer cells transmitted at the transceiver transmit interface.

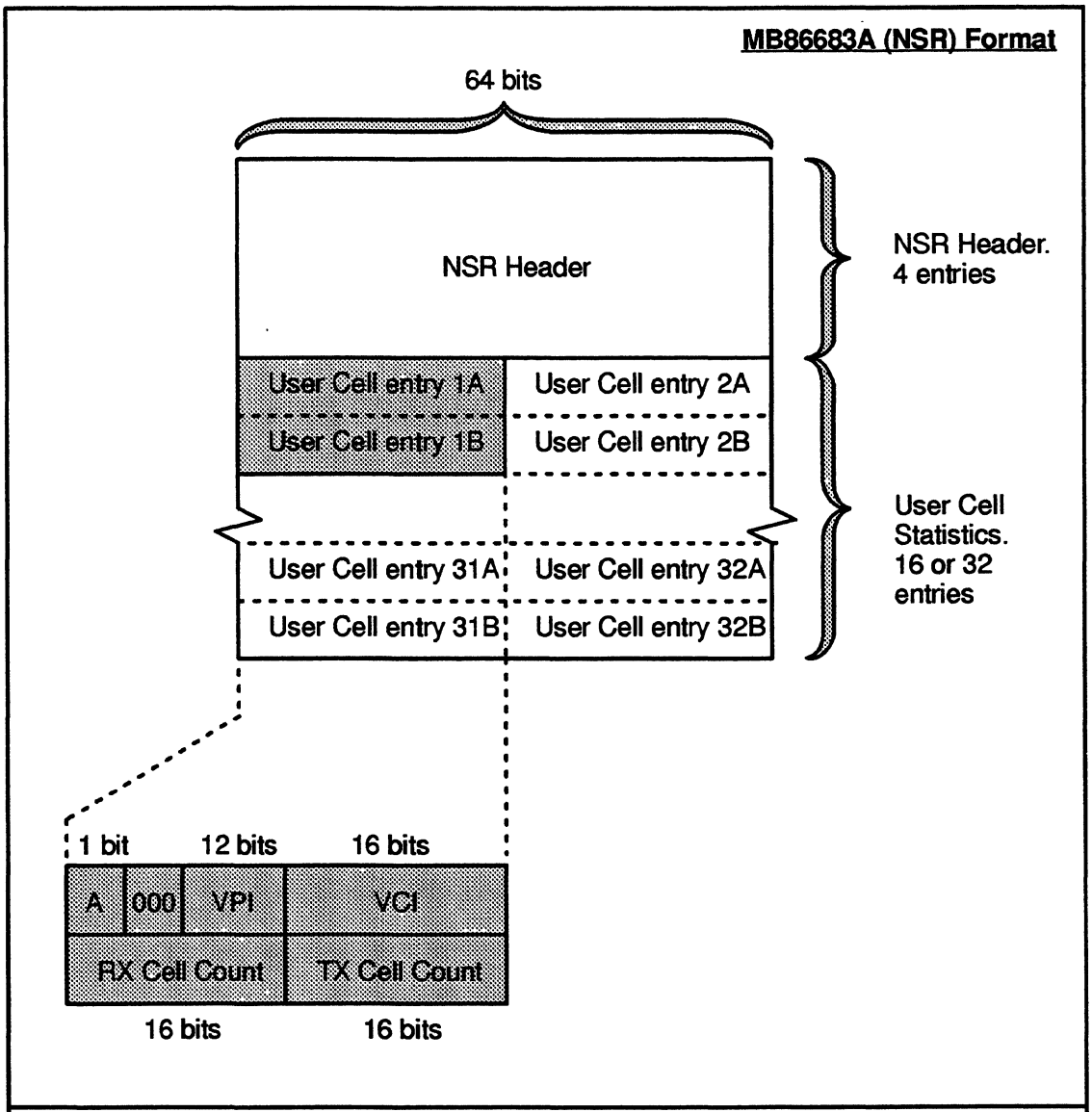
This will include assigned ATM layer cells that have been inserted via the cell transmitter insert buffer.

In order to accommodate the additional cell counts, the NSR table has been rearranged and increased in size. The table now consists of 36 x 64-bit entities. As the counts are now either 16 or 32-bit wide, they are aligned on 16-bit boundaries to allow greater flexibility for CPU masking. The VPI/VCI values are also aligned on 16-bit boundaries.

As the NSR table is now a different size, the DMA word transfer count (CC) in the descriptor should be set as follows for single burst transfers :-

Header only	: CC = 16
Header + 16 user entries	: CC = 80
Header + 32 user entries	: CC = 144

The format of the NSR is illustrated in the following diagram.



NSR Header Format (STM-1)

32-bit timestamp		D-count (total received and dropped)	
R-count (total received and not dropped)		T-count (total transmitted)	
HEC detected count	HEC corrected count	B2 FEBE count	B3 FEBE count
Unassigned cell (rx)	Unassigned cell (tx)	ATE count (rx)	ATE count (tx)
16 bits	16 bits	16 bits	16 bits

3.3. Cell Stream Interface

1. Addition of 1 input pin to configure the cell stream interface for either existing cell stream functionality or UTOPIA. (CS/$\overline{UT}$)
2. CSI now supports either 52 or 53 byte cells across the interface. In the 52 byte case, the HEC field is omitted. (OMITHEC bit in CR57).
3. Internal cell stream receive and transmit internal FIFOs have been reduced from 20 cells to 9.8 cells (512 bytes, excluding the HEC byte in each cell).

3.4. Cell Transmitter / Receiver

1. Option to generate either Idle cells or Unassigned cells for cell rate decoupling. (UNASGEN bit in CR26).
   Idle cells will always be discarded within the cell receiver.
   If unassigned cells are used for cell rate decoupling, then they may be discarded within the cell receiver by setting the UNASS bit in the Cell Receiver Discard register (CR25).
2. Option to ignore the GFC field for predefined cell type recognition (GFCIGN bit in CR18/CR26).
3. Distributed Sample Scrambler (DSS), which was used in cell-based mode ($1 + x^{28} + x^{31}$), has been deleted.

3.5. OAM controller

1. Deleted autonomous support for F1/F3 OAM cells.
2. Removed LOM interrupt and OAM interrupt indication register used for F1/F3 cell based PLOAM (SR60).
3. Rearranged the physical layer alarm status bits in SR59.

3.6. Microprocessor / DMA Interface.

1. Addition of 2 microprocessor input pins to suspend/abort the NTC control of the bus. ($\overline{BCLR}$ and $\overline{BERR}$).

2. Addition of 2 interrupts : BERR - set on receiving active $\overline{BERR}$ on pin.
   : ICD - set on gaining cell delineation.
   (moving from PRESYNC to SYNC state)

3. LOC interrupt now renamed to OCD (Out of Cell Delineation) in accordance with ATM Forum UNI.

4. LOM interrupt now deleted.

5. Microprocessor register read/write accesses now synchronous to the system clock. Internal read/writes require 7 clocks to complete.

6. Byte swapping of the Network Statistics Record and the Switch Statistics no longer performed. Data is always in big endian format to maintain data integrity.

7. SLT bit in Channel Control Register (CCR) of Descriptor Location Table no longer required. Direction of data transfer is implied by channel number.

3.7. Switch Statistics Handler.

1. Addition of separate register to enable this block independently from the Network Statistics. (CR50)

3.8. JTAG Test Circuitry

1. Addition of JTAG test circuitry in accordance with IEEE 1149.1.

The above changes have required additional control registers. Some existing registers have also had their control bits moved.

Any extra registers or modified register bits with existing registers have been high lighted in the following register table, followed by the additional/modified register map.

3.9. Control Registers

REG	ADDRESS AD0–6	FUNCTION	ACCESS
0	0	Not Used	
1	2	General Framer Control	Read/Write
2	4	Transmit Framer Overhead Access Bytes Block 1	Write
3	6	Transmit Framer Overhead Access Bytes Block 2	Write
4	8	Transmit Framer Overhead Access Bytes Block 3	Write
5	10	Transmit Framer Overhead Access Bytes Block 4	Write
6	12	Transmit Framer Overhead Access Bytes Block 5	Write
7	14	Transmit Framer Overhead Access Bytes Block 6	Write
8	16	Transmit Framer Overhead Access Bytes Block 7	Write
9	18	Transmit Framer Overhead Access Bytes Block 8	Write
10	20	Transmit Framer Overhead Access Bytes Block 9	Write
11	22	Transmit Framer Overhead Access Bytes Block 10	Write
12	24	Transmit Framer Overhead Access Bytes Block 11	Write
13	26	Transmit Framer Overhead Access Bytes Block 12	Write
14	28	Transmit Framer Overhead Access Bytes Block 13	Write
15	30	Transmit Framer Overhead Access Bytes Block 14	Write
16	32	Transmit Framer Overhead Access Bytes Block 15	Write
17	34	Transmit Framer Overhead Access Bytes Block 16	Write
18	36	Cell Receiver General Control	Read/Write
19	38	Cell Receiver HEC / Descrambler Control	Read/Write
20	40	Cell Receiver User Defined Extract/Discard XMASK #1	Read/Write
21	42	Cell Receiver User Defined Extract/Discard XMASK #2	Read/Write
22	44	Cell Receiver User Defined Extract/Discard SMASK #1	Read/Write
23	46	Cell Receiver User Defined Extract/Discard SMASK #2	Read/Write
24	48	Cell Receiver Extract Buffer Control	Read/Write
25	50	Cell Receiver Discard Control	Read/Write
26	52	Cell Transmitter General Control	Read/Write
27	54	Cell Transmitter HEC / Scrambler Control	Read/Write
28	56	Cell Transmitter User Defined Extract/Discard XMASK #1	Read/Write
29	58	Cell Transmitter User Defined Extract/Discard XMASK #2	Read/Write
30	60	Cell Transmitter User Defined Extract/Discard SMASK #1	Read/Write
31	62	Cell Transmitter User Defined Extract/Discard SMASK #2	Read/Write

Control Registers (continued)

REG	ADDRESS AD0–6	FUNCTION	ACCESS
32	64	Cell Transmitter Extract Buffer Control	Read/Write
33	66	Cell Transmitter Discard Control	Read/Write
34	68	OAM Framed Alarm Control	Read/Write
35	70	Not Used	
36	72	Not Used	
37	74	Not Used	
38	76	Not Used	
39	78	Not Used	
40	80	Not Used	
41	82	Not Used	
42	84	Not Used	
43	86	Not Used	
44	88	Not Used	
45	90	Not Used	
46	92	Not Used	
47	94	Not Used	
48	96	Not Used	
49	98	Not Used	
50	100	Switch Statistics Handler Control	Read/Write
51	102	Network Statistics General Control	Read/Write
52	104	Network Statistics User Cell Mask XMASK#1	Read/Write
53	106	Network Statistics User Cell Mask XMASK#2	Read/Write
54	108	Network Statistics User Cell Mask SMASK#1	Read/Write
55	110	Network Statistics User Cell Mask SMASK#2	Read/Write
56	112	Cell Stream Interface Control #1	Read/Write
57	114	Cell Stream Interface Control #2	Read/Write
58	116	Interrupt Enable	Write
59	118	Interrupt Under Service	Write
60	120	DMA Descriptor Pointer Table Low	Write
61	122	DMA Descriptor Pointer Table High	Write
62	124	DMA Channel Activity	Write
63	126	DMA Mode	Write

3.10. Status Registers

REG	ADDRESS AD0–6	FUNCTION	ACCESS
0	0		
1	2		
2	4	Receive Framer Overhead Access Bytes Block 1	Read
3	6	Receive Framer Overhead Access Bytes Block 2	Read
4	8	Receive Framer Overhead Access Bytes Block 3	Read
5	10	Receive Framer Overhead Access Bytes Block 4	Read
6	12	Receive Framer Overhead Access Bytes Block 5	Read
7	14	Receive Framer Overhead Access Bytes Block 6	Read
8	16	Receive Framer Overhead Access Bytes Block 7	Read
9	18	Receive Framer Overhead Access Bytes Block 8	Read
10	20	Receive Framer Overhead Access Bytes Block 9	Read
11	22	Receive Framer Overhead Access Bytes Block 10	Read
12	24	Receive Framer Overhead Access Bytes Block 11	Read
13	26	Receive Framer Overhead Access Bytes Block 12	Read
14	28	Receive Framer Overhead Access Bytes Block 13	Read
15	30	Receive Framer Overhead Access Bytes Block 14	Read
16	32	Receive Framer Overhead Access Bytes Block 15	Read
17	34	Receive Framer Overhead Access Bytes Block 16	Read
18	36		
19	38		
20	40		
21	42		
22	44		
23	46		
24	48		
25	50		
26	52		
27	54		
28	56		
29	58		
30	60		
31	62		

Status Registers (continued)

REG	ADDRESS AD0–6	FUNCTION	ACCESS
32	64		
33	66		
34	68		
35	70		
36	72		
37	74		
38	76		
39	78		
40	80		
41	82		
42	84		
43	86		
44	88		
45	90		
46	92		
47	94		
48	96		
49	98		
50	100		
51	102		
52	104		
53	106		
54	108		
55	110		
56	112		
57	114	CSI Receive and Transmit Buffer Fill Levels	Read
58	116	Interrupt Status	Read
59	118	Physical Layer Alarms Received	Read
60	120		
61	122	Internal Buffer Overflow Interrupt Indication	Read
62	124	DMA Channel Activity Status	Read
63	126	BERR / DMA Interrupt Indication	Read

3.11. Additional / Modified Register Map

Control Register 0 – Not Used

Control Register 1 – General Framer Control

D15

P3	P2	P1	P0	N3	N2	N1	N0
LOOPBACK	STMDESC	STMSCR	TESTMODE	XMODE2	XMODE1	XMODE0	FRMENB

D0

FRMENB : Rx/Tx Framer Enable
0 : Disabled
1 : Enabled

XMODE2–0 : Transceiver mode
000 : Cell based
001 : SDH (STM–1)
010 : SONET (STS–3c)
011 : DS3 (with PLCP)
100 : E3
101 : SONET (STS–1)
110 : DS3 (non PLCP)

TESTMODE : Internal Testmode (User should set to zero)
0 : Disabled
1 : Enabled

STMSCR : $1+x^6+x^7$ frame scrambler
0 : Disabled
1 : Enabled

STMDESC : $1+x^6+x^7$ frame descrambler
0 : Disabled
1 : Enabled

LOOPBACK : TX to RX framer loopback
0 : Disabled
1 : Enabled

N3–N0 : Frame sync found count (1 – 15)

P3–P0 : Frame sync lost count (1 – 15)

Note : N3–0 and P3–0 are used on the following framing bytes :–

SDH & SONET : A1, A2
DS3 : F1, F2, F3, F4
E3 : FA1, FA2

Control Register 2 - Transmit Framer Overhead Access Bytes Block 1

D15 D8

D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D7 D0

Description :-

Overhead byte insert data register for :-

SDH / SONET :-
D15 - D8 : C1
D7 - D0 : R1

E3 :-
D15 - D8 : TR
D7 - D0 : NR

DS3 :-
D15 - D8 : 0
D7 - D5 : 0
D4 - D0 : Five of the C-bits

D4 = C1	(AIC)
D3 = C3	(FEAC)
D2 = C13	(DL)
D1 = C14	(DL)
D0 = C15	(DL)

Control Register 18 - Cell Receiver General Control

D15

TESTMODE							GFCIGN
PKIR3	PKIR2	PKIR1	PKIR0	INSPRI	CRC10GEN	CRC10CHK	CRXENB

D0

CRXENB :	Cell Receiver Enable	0 : Disabled 1 : Enabled
CRC10CHK :	OAM Cell CRC Check	0 : Disabled 1 : Enabled
CRC10GEN :	OAM Cell CRC Generate	0 : Disabled 1 : Enabled
INSPRI :	Cell Insert Priority	0 : User cells have priority 1 : Insert Buffer cells have priority
PKIR3-0 :	Peak cell insertion rate (from insert buffer)	0-11 : See Note below.
GFCIGN :	GFC field Ignore (predefined cells)	0 : 12-bit VPI 1 : 8-bit VPI
TESTMODE :	Internal Testmode (User should set to zero)	0 : Disabled 1 : Enabled

Note :

PKIR3-0 specifies the maximum cell insertion rate via the insert buffer.
The rate is defined by the following relationship :

1 inserted cell in $2^{(13-PKIR)}$ transmitted cells.

eg. For SDH / SONET (155.52 Mbps) :

PKIR = 0 :- Max insert rate = 1 in 2^{13} cells (ie equivalent to 19 Kbps)

PKIR = 11 :- Max insert rate = 1 in 2^{2} cells (ie equivalent to 38.9 Mbps)

Control Register 19 – Cell Receiver HEC/Descrambler Control

D15

ALPHA3	ALPHA2	ALPHA1	ALPHA0	DELTA3	DELTA2	DELTA1	DELTA0
			BALIGN	COREN	HECMASK		DESCR

D0

DESCR : Descramble Control
0 : disable
1 : $1 + x^{43}$

HECMASK : HEC Receive Mask
0 : Mask disabled
1 : Mask enabled (01010101)

COREN : Error Correction enable
0 : Disabled
1 : Enabled

BALIGN : Byte Alignment
0 : Non-byte aligned data
1 : Byte aligned data

DELTA3–0 : Cell sync found count (1 – 15)

ALPHA3–0 : Cell sync lost count (1 – 15)

Control Register 26 – Cell Transmitter General Control

D15

TESTMODE						UNASGEN	GFCIGN
PKIR3	PKIR2	PKIR1	PKIR0	INSPRI	CRC10GEN	CRC10CHK	CTXENB

D0

CTXENB :	Cell Transmitter Enable	0 : Disabled 1 : Enabled
CRC10CHK :	OAM Cell CRC Check	0 : Disabled 1 : Enabled
CRC10GEN :	OAM Cell CRC Generate	0 : Disabled 1 : Enabled
INSPRI :	Cell insert Priority	0 : User cells have priority 1 : Insert Buffer cells have priority
PKIR3–0 :	Peak cell insertion rate (from insert buffer)	0–11 : See Note below.
GFCIGN :	GFC field Ignore (predefined cells)	0 : 12-bit VPI 1 : 8-bit VPI
UNASGEN :	Cell Rate Decoupling generation	0 : Idle cells generated 1 : Unassigned cells generated
TESTMODE :	Internal Testmode (User should set to zero)	0 : Disabled 1 : Enabled

Note :

PKIR3–0 specifies the maximum cell insertion rate via the insert buffer.
The rate is defined by the following relationship :

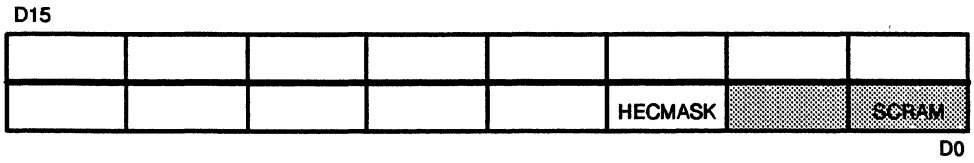
1 inserted cell in $2^{(13-PKIR)}$ transmitted cells.

eg. For SDH / SONET (155.52 Mbps) :

PKIR = 0 :– Max insert rate = 1 in 2^{13} cells (ie equivalent to 19 Kbps)

PKIR = 11 :– Max insert rate = 1 in 2^{2} cells (ie equivalent to 38.9 Mbps)

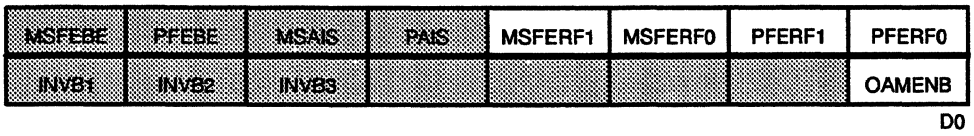
Control Register 27 – Cell Transmitter HEC/Scrambler Control



SCRAM : Scramble Control
0 : disable
1 : $1 + x^{43}$

HECMASK : HEC Transmit Mask
0 : Mask disabled
1 : Mask enabled (01010101)

Control Register 34 – OAM Alarm Control



OAMENB :	OAM Controller Enable	0 : Disabled 1 : Enabled
INVB1,2,3 :	Invert BIP (B1, B2, B3) (see below)	0 : Normal BIP 1 : Inverted BIP
PAIS :	Tx Path AIS	0 : Clear 1 : Set
MSAIS :	Tx Section AIS	0 : Clear 1 : Set
PFERF1,0 :	Tx Path FERF	00 : Clear 01 : Auto 10 : Set
MSFERF1,0 :	Tx Section FERF	00 : Clear 01 : Auto 10 : Set
PFEBE :	Tx Path FEBE (B3)	0 : Disabled 1 : Enabled
MSFEBE :	Tx Section FEBE (B2)	0 : Disabled 1 : Enabled

Note 1 :

INVB1,2,3 bits may be used for testing. Setting these bits will cause all the bits in the associated transmitted BIP field to be inverted.

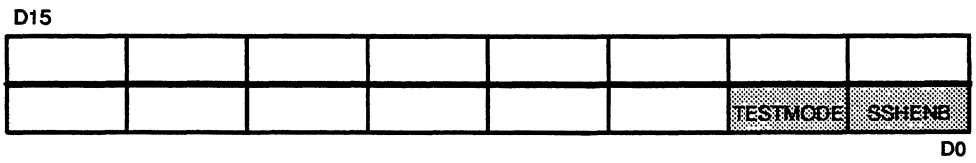
Note2 :

For *auto* modes, PFERF and MSFERF will be set depending on various received conditions, such as LOS, LOP, OCD, PAIS, etc, in accordance with specification I.610. However, no integration time is applied to any of these alarms.

Control Register 35 – Not Used

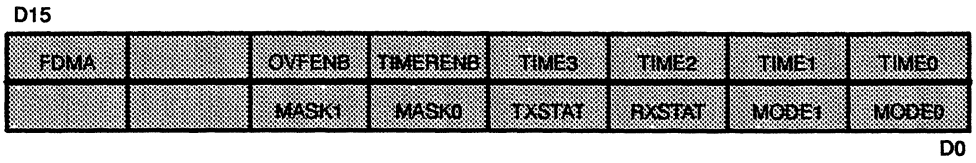
Control Register 36 – Not Used

Control Register 50 – Switch Statistics Handler Control



SSHENB :	Switch Statistics Handler Enable	0 : Disabled 1 : Enabled
TESTMODE :	Internal Testmode (User should set to zero)	0 : Disabled 1 : Enabled

Control Register 51 – Network Statistics Record General Control



MODE1, 0 :	Statistics Controller Mode (Table size)	00 : Disabled 01 : Header Only 10 : Header + 16 User entries 11 : Header + 32 User entries
RXSTAT :	Receive User Statistics	0 : Disabled 1 : Enabled
TXSTAT :	Transmit User Statistics	0 : Disabled 1 : Enabled
MASK1,0 :	VP/VC Filter Mask	00 : Mask Disabled 01 : Filter MASK enabled 10 : Invalid 11 : Filter $\overline{\text{MASK}}$ enabled
TIME3–0 :	Statistics DMA transfer timeout	
TIMERENB :	Timer Enable (DMA)	0 : Disable 1 : Enabled
OVFENB :	Overflow Enable (DMA)	0 : Disable 1 : Enabled
FDMA :	Force DMA transfer	0 : DMA based on other events above 1 : Force DMA

Note1 :

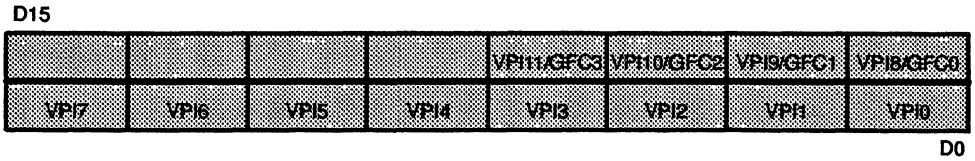
The FDMA bit will be automatically cleared whilst the DMA operation is being performed. This bit is not readable.

Note2 :

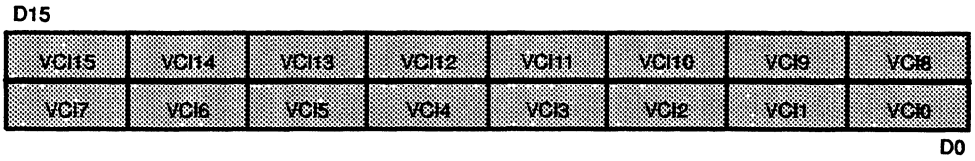
The TIME3–0 bits are used to provide a programmable timeout for the statistics data (NSR) to be sent to memory via DMA, for the situation where no other event has caused this to happen, ie no counter has reached its maximum value, or the table is not yet full.

The relationship is : Timeout Event = $2^{(26-\text{TIMEOUT})}$ x clock period

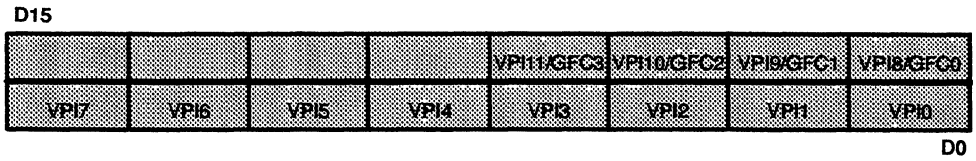
Control Register 52 – Statistics VP Filter XMASK



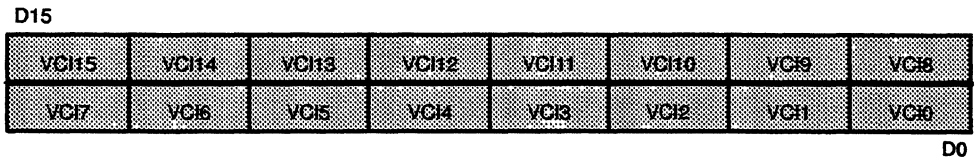
Control Register 53 – Statistics VC Filter XMASK



Control Register 54 – Statistics VP Filter SMASK



Control Register 55 – Statistics VC Filter SMASK

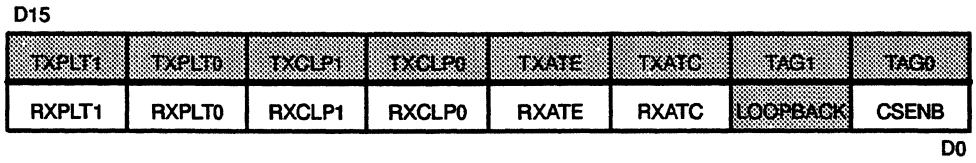


These registers are used for filtering the user statistics prior to being recorded into the NSR. The filter operation may work on cells which pass or fail the filter, or may be disabled. The relevent mode is controlled from CR51.
The filter works on both TX and RX paths. This filtering operation does not effect the total cells received/transmitted counts.

Any of the 28 VPI/VCI bits of the cell header may be defined as X, 0, or 1.

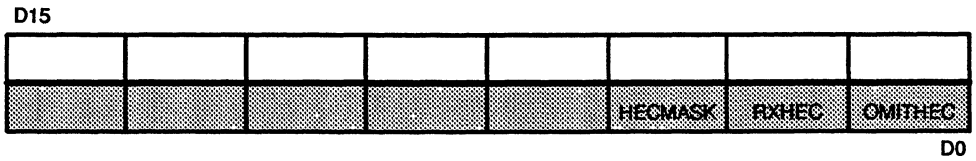
The XMASK is used to define X states for each bit.
When set to 1, they represent an X for that bit.
When set to 0, the filter will take the state defined in the SMASK.

Control Register 56 – Cell Stream Interface Control #1



CSENB :	Cell Stream Enable	0 : Disabled 1 : Enabled
LOOPBACK :	CSI Rx/Tx Loopback	0 : loopback disabled 1 : loopback enabled
RXATC : **TXATC :**	ATC enable	0 : ATC not present 1 : ATC present
RXATE : **TXATE :**	Address translation error	0 : discard ATE cells 1 : forward ATE cells
RXCLP1,0 : **TXCLP1,0 :**	CLP bit option	00 : old header value 01 : from address translation 10 : force to 0 11 : force to 1
RXPLT1,0 : **TXPLT1,0 :**	PLT congestion bit option	00 : old header value 01 : from address translation 10 : force to 0 11 : force to 1
TAG1,0 :	Routing Tag Byte Size	00 : 0 01 : 1 10 : 2 11 : 3

Control Register 57 – Cell Stream Interface Control #2



OMITHEC :	Omit HEC byte on transmit (Receive path)	0 : 53 byte cell transmission 1 : 52 byte cell transmission
RXHEC :	HEC Generator enable (Receive path)	0 : Disabled 1 : Enabled
HECMASK :	ACSI Rx path HEC Mask (Receive path)	0 : Mask disabled 1 : Mask enabled (01010101)

Control Register 58 – Interrupt Enable

D15

				BERR	SOFTX	SOVRX	SOFRX
	BUFFOVF	ICD	OCD	LOP	LOF	LOS	DMA

D0

DMA :	DMA Channel 0–5 Interrupt	0 : Interrupt masked 1 : Interrupt enabled
LOS :	Loss Of Signal	0 : Interrupt masked 1 : Interrupt enabled
LOF :	Loss Of Frame	0 : Interrupt masked 1 : Interrupt enabled
LOP :	Loss Of Pointer (STM–1)	0 : Interrupt masked 1 : Interrupt enabled
OCD :	Out of Cell Delineation	0 : Interrupt masked 1 : Interrupt enabled
ICD :	Into Cell Delineation	0 : Interrupt masked 1 : Interrupt enabled
BUFFOVF :	Internal Buffer Overflow	0 : Interrupt masked 1 : Interrupt enabled
SOFRX :	Start Of Frame (Receive)	0 : Interrupt masked 1 : Interrupt enabled
SOVRX :	Start Of VC–4 (Receive)	0 : Interrupt masked 1 : Interrupt enabled
SOFTX :	Start Of Frame (Transmit)	0 : Interrupt masked 1 : Interrupt enabled
BERR :	Bus Error	0 : Interrupt masked 1 : Interrupt enabled

Control Register 59 – Interrupt Under Service

D15

				BERR	SOFTX	SOVRX	SOFRX
	BUFFOVF	ICD	OCD	LOP	LOF	LOS	DMA

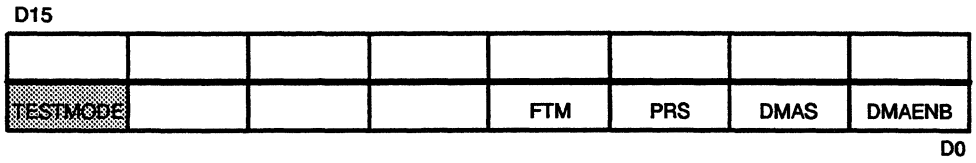
D0

These bits are set by the processor to indicate that the associated exception condition is being dealt with. This has two effects :

1. It will clear the associated interrupt request, and
2. Will inhibit any further interrupt requests of the associated type from being generated.

The associated bits should be set back to zero in order to enable further interrupts to be generated. The interrupt sources are identical to those shown in the Interrupt Enable Register.

Control Register 63 – DMA Mode



DMAENB :	DMA Controller Enable	0 : Disabled 1 : Enabled
DMAS :	DMA Stop	0 : DMA not stopped 1 : DMA stopped
PRS :	Priority Select	0 : Channel 0 has priority 1 : Channel 5 has priority
FTM :	Fast Transfer Mode	0 : Descriptor DMA cycle dependent on READY input 1 : Fast DMA cycle for descriptor transfer
TESTMODE :	Internal Testmode (User should set to zero)	0 : Disabled 1 : Enabled

Status Register 2 – Receive Framer Overhead Access Bytes Block 1

D15

D7	D7	D5	D4	D3	D2	D1	D0
D7	D6	D5	D4	D3	D2	D1	D0

D0

Overhead byte insert data register for :-

SDH / SONET :-
D15 - D8 : C1
D7 - D0 : R1

E3 :-
D15 - D8 : TR
D7 - D0 : NR

DS3 :-
D15 - D8 : 0
D7 - D5 : 0
D4 - D0 : Five of the C-bits

D4 = C1 (AIC)
D3 = C3 (FEAC)
D2 = C13 (DL)
D1 = C14 (DL)
D0 = C15 (DL)

Status Register 57 – CSI Receive / Transmit Buffer Fill Levels

D15

RXBUFF3	RXBUFF2	RXBUFF1	RXBUFF0	TXBUFF3	TXBUFF2	TXBUFF1	TXBUFF0
0	0	0	0	0	X	X	X

D0

This register shows the fill levels of both CSI cell buffers.
The count will be in cells (0–10)

The X bits will contain the settings of the control bits as set in CR57

Status Register 58 – Interrupt Status Register

D15

0	0	0	0	BERR	SOFTX	SOVRX	SOFRX
0	BUFFOVF	ICD	OCD	LOP	LOF	LOS	DMA

D0

This register shows the source of the interrupt. The bits are identical to CR58.

Status Register 59 – Physical Layer Alarms Received

D15

PJUST	NJUST	NDF	0	0	B3ERR	P-FERF	P-AIS
0	0	0	0	B2ERR	B1ERR	MS-FERF	MS-AIS

D0

	DS-3	SONET / SDH	E3
MS-FERF	X-bits = 0	K2 (6-8) = 110	MA (bit 1) = 1
MS-AIS	Info = 1010... C-bits = 0 X-bits = 1	K2 (6-8) = 111	
P-FERF	G1 (bit 5) = 1	G1 (bit 5) = 1	
P-AIS		pointer = 1	
B1ERR	received CP bits ≠ calculated BIP	received B1 byte ≠ calculated BIP	
B2ERR		received B2 byte ≠ calculated BIP	received EM byte ≠ calculated BIP
B3ERR	received B1 byte ≠ calculated BIP	received B3 byte ≠ calculated BIP	

Note1 :
For DS-3 mode, the PLCP (if enabled) carries the path alarms, whereas the DS-3 frame carries the section alarms.

Note 2 :
B1ERR, B2ERR, and B3ERR are set on receiving a B1/B2/B3 BIP count that disagrees with the calculated BIP. A corresponding FEBE will be transmitted back via the transmit framer, if the FEBE function is enabled in CR34.

Note 3 :
PJUST = positive justification event for SDH/SONET pointer
NJUST= negative justification event for SDH/SONET pointer
NDF = New Data Flag event for SDH/SONET pointer

Status Register 63 – BERR / DMA Interrupt Indication

D15

0	0	CHAN5	CHAN4	CHAN3	CHAN2	CHAN1	CHAN0
0	0	CHAN5	CHAN4	CHAN3	CHAN2	CHAN1	CHAN0

D0

This register shows which DMA channel generated either the DMA interrupt or which channel was curently active when the BERR interrupt was generated.

D13 – D8 : DMA Channel due to BERR interrupt

D5 – D0 : DMA Channel due to DIE descriptor bit being set