

## Fujitsu SCSI Products

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In this section we look at Fujitsu's MB8660X family of SCSI Protocol Controller (SPC) ICs. The MB8660X family offers an optimum balance of design flexibility and price/performance, and helps reduce time to market.

We break our discussion into two sections:

### I. The Features of the Core MB8660X Architecture

- External Interfaces
- Internal Processor
- Timer and Controllers
- Registers
- Data FIFO
- Status Buffers
- User Program Memory
- Error Reporting
- On-chip Debug Features

### II. The Individual Products in the MB8660X Family

- MB8660X Roadmap
- MB8660X Overview
- Special Focus: The MB86604L
- Special Focus: The MB86605
- Special Focus: The MB86606 (upcoming)

Let's begin by looking at the core MB8660X architecture.

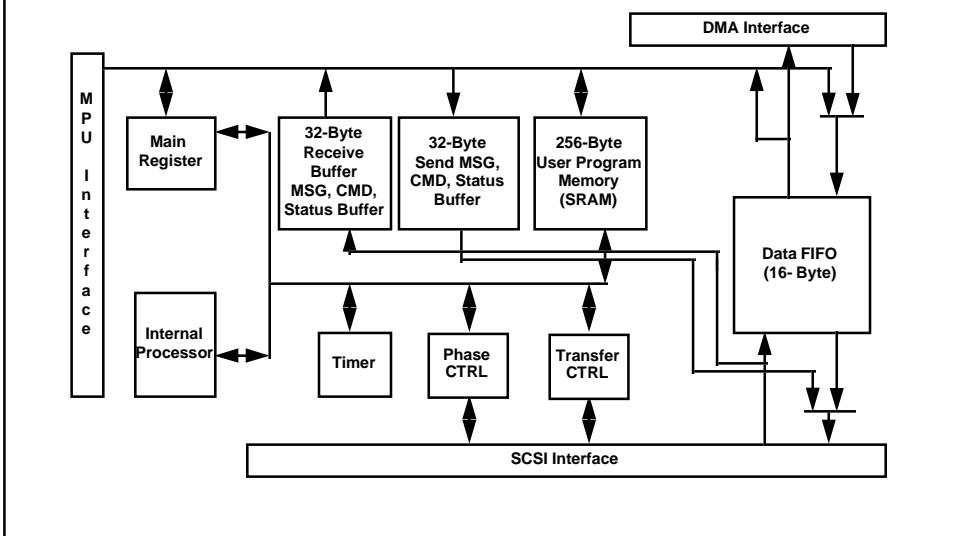
## I. The Core MB8660X Architecture

Fujitsu has taken a “core architecture” approach in developing the MB8660X family of SCSI protocol controllers (SPCs). That is, each SPC in the family is built around the same basic design and is software compatible.

This makes product development faster. It also makes it easier for customers to update their designs to accommodate new FMI products. When customers want to migrate their designs to a different Fujitsu SPC, they don’t have to completely rewrite their software driver. Minor upgrades or adjustments is all it takes to move within products in the MB8660X family.

The block diagram below illustrates the MB8660X core architecture. In the next few pages, we explain the purpose of each functional block in the diagram. As we do so, you may want to refer back to this page. A summary box of the most important MB8660X architecture features appears on page 12.

The Core MB8660X Architecture



## The Core Architecture: External Interfaces

**The MPU Interface** is the SPC's connection to the system's microprocessor unit (or MPU). The MPU interface is the access point for microprocessor commands entering the SPC. Microprocessors are typically associated with host computers, but many of today's "smart" peripherals have an on-board MPU as well. The MB8660X family can be used in either situation, a host computer or a peripheral. The MB8660X provides direct connection to the I/O signals of x86 (Intel/IBM) and 68xxx (Motorola/Apple) processors. (There is an input select mode that specifies which environment the SPC will be used in.) Direct microprocessor connection reduces chip count and lowers overall cost. MB8660X SPCs also support RISC processors like those found in high-performance workstations. In these systems, additional logic may be required to optimize the SPC/processor connection.

**The DMA Interface** is the SPC's connection to the system's direct memory access (or DMA). In a host computer, for instance, memory-resident data enters the SPC through the DMA interface.

**The SCSI Interface** is the SPC's connection to the SCSI bus. SCSI commands, messages and payload data entering and exiting the SPC use the SCSI interface as their access point to and from the SPC.

### External Interfaces

- MPU interface connects SPC to host computer's or peripheral's microprocessor.
  - MB8660X offers direct connection to 80 (Intel/IBM) and 68 (Motorola/Apple) MPU families; good for host adapter cards.
- DMA interface connects SPC to host computer's or peripheral's system memory.
- SCSI interface connects SPC to SCSI bus.

## The Core Architecture: Internal Processor

**The Internal Processor**, a key feature of the MB8660X core architecture, is a specialized microprocessor embedded in the SPC. It delivers two important benefits. First, the internal processor makes the overall system more efficient. The internal microprocessor oversees the SCSI operation, providing sequence control between each phase of the SCSI protocol. It can take on tasks that would otherwise have to be performed by the external microprocessor. The external processor doesn't have to baby-sit the SPC, because the SPC's internal processor manages the SCSI phases on its own. Second, the internal processor makes it possible to customize the SCSI operation. The design engineer can program the internal microprocessor to execute user-defined program strings. The programs consist of predefined SCSI commands that can be linked via conditional commands (such as Compare, And, Move, and so on). A program is then loaded into the SPC's memory and executed from within the chip using the program's start address. With this high-level programming feature, it is possible to execute an entire SCSI event from Bus Free to Command Complete without generating an interrupt. The SCSI processor will sequence through the various SCSI phases independent of the external processor, thus reducing system overhead. The internal processor increases overall performance and supports greater product differentiation.

### Internal Processor

- Frees up the external processor
  - Takes over SCSI operation so external processor can do other, system-related tasks.
  - Reduces external processor overhead, thus increasing overall system performance.
- Executes custom user programs
  - Lets design engineer link commands together for fewer interrupts and more intelligent operation
  - Allows for greater product differentiation



## The Core Architecture: Timer and Controllers

**The Timer** is a counter for the SCSI operations. It manages the time it takes for each SCSI function, generating a “timed out” error if the operation takes longer than specified by the SCSI protocol. The timer looks at each event on the SCSI bus and determines if it falls within the time parameters specified by ANSI. If the operation takes too long, the timer generates an interrupt, thus preventing the SPC from being “hung” in mid-operation.

**The Phase Controller** is used to control and execute the SCSI bus phases (see *Tutorial*). Once the SCSI operation has been selected and the data transfer is ready to begin, the transfer controller takes over.

**The Transfer Controller** is used to control the flow of data to and from the SCSI bus. It interacts with the SCSI interface and the DMA interface. On the SCSI interface side, it controls asynchronous and synchronous data transfers. On the DMA interface side, it controls the flow of incoming data. The transfer controller offers terabyte transfer counting, for very large data transfer operations.

### Timer and Controllers

- On-chip Timer
  - Monitors SCSI bus, checking for operations that take longer than expected. Generates “timed out” interrupt if operation goes overtime.
- Phase Controller
  - Supervises transition through bus selection phases (Bus Free, Arbitration, etc.)
- Transfer Controller
  - Supervises flow of data to and from the SCSI bus.
  - Offers terabyte transfer counter for large data transfer operations.

## The Core Architecture: Registers

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**The Main Register Block** is a series of registers that lets the engineer specify parameters for particular SCSI operations.

On-chip registers simplify driver design because they specify information that would otherwise have to be specified in the driver. The driver for an SPC with a full-featured, flexible register set (such as the one provided with MB8660X SPCs) is smaller, more streamlined and easier to develop.

Like the internal processor, the register set is a key feature of the MB8660X architecture.

### Registers

- Registers store information that specifies how and what the SPC will do.
- Working with the on-board microprocessor, registers can be used to improve SCSI performance.
- Registers simplify driver design, because they store information that would otherwise have to be specified in the driver.

## The Core Architecture: Data FIFO

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**The Data FIFO** makes synchronous transfer more efficient. It is used to temporarily store the data waiting to be sent during a synchronous transfer (see *Tutorial*).

FIFO (First In First Out) size varies within the MB8660X family from 32 bytes to 512 bytes. The size of the FIFO is determined by the data offset supported during synchronous transfer. In the MB86604L, for example, there is a 32-byte FIFO that corresponds to the 32-byte data offset it supports. Data enters the MB86604L through the DMA interface, and collects in the FIFO. The FIFO holds up to 32 bytes of data, in preparation for delivery to the SCSI bus when the next batch of data is required.

### Data FIFO

- Makes data transfers more efficient
- Temporarily stores data to be sent during synchronous transfer
- Size of FIFO varies within MB8660X family
  - 32 bytes to 512 bytes
- Size determined by data offset supported
  - MB86604L supports 32-byte data offset, and has a 32-byte FIFO

## The Core Architecture: Status Buffers

**The Two Status Buffers**, 32-byte receive and 32-byte send, are used to store the messages (MSG), commands (CMD) and status data that enter and exit the SPC. They are, in effect, the “in” and “out” boxes of the SPC. They make the overall SCSI operation more efficient.

### 32-byte Receive Buffer

The 32-byte receive buffer is the SPC’s “In Box.” It receives and temporarily stores any messages, commands and status information being sent to the SPC over the SCSI bus. In a host adapter, the data is typically being received from a peripheral; in a peripheral, the data is typically being received from the host computer. In either case, the system’s external processor uses the MPU interface to check the contents of the receive buffer.

### 32-byte Send Buffer

The 32-byte send buffer is the SPC’s “Out Box.” It temporarily stores and then sends messages, commands and status information issued by the host system’s microprocessor. In a host computer, the data is typically being sent to a peripheral; in a peripheral, the data is typically being sent to the host computer. In either case, the system’s external microprocessor uses the MPU interface to deposit information into the send buffer. The send buffer then uses the SCSI interface to put the data onto the SCSI bus for transmission.

### Status Buffers

- Used to temporarily store messages, commands and status data
- 32-byte Receive Buffer (“In Box”)
  - Accepts messages, commands and status data entering from SCSI bus (via the SCSI interface)
  - Temporarily stores information before it is delivered to the system’s external microprocessor
- 32-byte Send Buffer (“Out Box”)
  - Accepts messages, commands and status data entering from external microprocessor (via the MPU interface)
  - Temporarily stores information before it is sent over the SCSI bus

## The Core Architecture: User Program Memory

**The User Program Memory**, another key feature of the MB8660X architecture, provides on-chip RAM for storing user-defined command strings and command queuing tags.

Stringing together separate (or “discrete”) commands creates a user-defined program to be stored in the on-chip RAM. Normally, an interrupt is generated at the end of each SCSI command. Linking commands together in a user program can eliminate interrupts, thus reducing processor intervention in the SCSI operation. A typical user program, also called a routine, can run all the way from selection to final message with only a single interrupt. The design engineer might program the SPC, for instance, to do a full read from disk with only one command complete interrupt. Note that user program code is a part of the SCSI driver.

Command Queuing (discussed in the Tutorial section) is a SCSI 2 feature that lets the external MPU process tagged commands out of order. The incoming command tag, called a command descriptor block or CDB, is stored in a predefined location in the on-chip RAM. The CDB sits in RAM waiting to be processed. The number of CDBs that can be stored is determined by the available RAM. RAM size varies within the MB8660X family, ranging from 256 bytes to 2 KB.

### User Program Memory

- On-chip RAM used with internal processor and registers to customize SPC performance
- Supports linked commands
  - Stores user-defined program (series of discrete commands)
  - User-defined program makes processing faster, more efficient
  - User program is a part of the SCSI driver
- Supports command queuing
  - Stores command tags waiting to be processed
  - Command queuing makes processing more efficient
- Size of RAM runs from 512 bytes to 2 Kbytes

## Core Architecture: Error Reporting

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The next two features we cover, error reporting and on-chip debug features tools, are not shown in the block diagram of the core architecture. However, both are important features of the MB8660X family as a whole, so we include them in our core architecture description.

The **error reporting system** makes it easier to troubleshoot errors in transmission and identify problem areas in the design. The MB86605, for instance, provides 256 predefined interrupt codes to cover transfer errors, phase errors, reporting errors, selection/reselection errors and auto selection/reselection errors. In each of these categories, there are at least seven differential error conditions the SPC will acknowledge. Later generation MB8660X products support programmable interrupts, which means the design engineer can pick and choose the errors to be reported in a particular design. Non-critical errors can be masked or disabled in a design, to lessen the number of interrupts and reduce microprocessor intervention.

The main register block is used to support error reporting. Processor interrupt conditions are reported in the interrupt status registers, while SPC error conditions are reported in the command step registers. Together, these registers provide a precise description of the error and the condition of the SPC when the error occurred.

### Error Reporting Scheme

- Comprehensive reporting scheme makes it easier to troubleshoot errors in transmission and identify problem areas in the design.
- Programmable interrupts: non-critical errors aren't reported, so they don't slow down processing.
- Error conditions reported in main register block.
- System provides precise description of the error and the conditions under which it occurred.

## On-Chip Debug Features

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Each SPC in the MB8660X family offers on-chip debug features that make development and production easier, thus reducing time to market.

The **on-chip debug features** can be used during development to identify errors in the user program code. The MB8660X family allows control of individual signals on the SCSI bus. The design engineer can “wiggle” signals on the SCSI bus, and get a clearer picture of SPC performance.

Once the design is in production, the on-chip debug features can be used again to test fully programmed SPCs before they are shipped to a customer. A SCSI bus emulator on-board the SPC lets it be tested in isolation, so individual ICs can be tested at incoming inspection.

### On-Chip Debug Features

- Used at two points in the development process
- During user program development
  - Design engineer can “wiggle” SCSI signals on the bus
  - Gives clearer picture of SPC performance and isolates problems
- During incoming inspection after production
  - Test engineer can emulate SCSI bus
  - Simplifies testing because IC be tested in isolation, without being hooked up to a board
- Main benefit: speeds time to market

## Core Architecture: Summary

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The summary box below lists the primary features that support these benefits. These features are applicable to all the ICs in the MB8660X.

In the next half of this section, we look at the individual products that make up the MB8660X family, highlighting their special features and outlining their performance specifications. We begin with a look at the MB8660X roadmap.

### MB8660X Architecture: Key Features

- Features that let the engineer create a better design:
  - *Internal microprocessor* executes user programs and reduces system overhead.
  - *Registers* let the engineer specify parameters for particular operations, and reduce size/complexity of driver software.
  - *User program memory* stores custom SCSI operations on-chip, for increased flexibility and performance.
- Features that reduce development time:
  - *Core architecture approach* makes it easier to move up performance path for next generation products
  - *Informative error reporting system* makes it easier to isolate design errors.
  - *On-chip debug features* make it easier to fine-tune a design, and simplify production test.

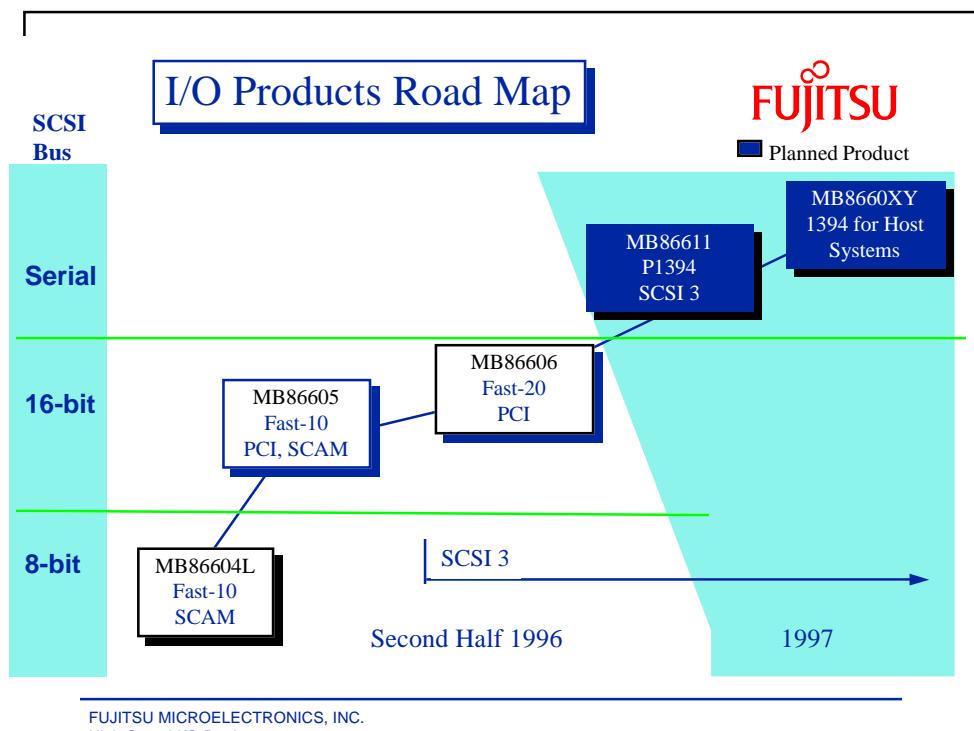
## II. Individual MB8660X Products

The roadmap shown below gives a complete picture of the MB8660X family, from its early beginnings to its future direction.

The MB86601 is the original Fujitsu SCSI 2 SPC. It is the kernel from which the other products are derived. The 601, 602 and 603 products are still in wide use today.

For new designs, the 604L and 605 provide improved performance. These SCSI 2 products are the focus for new designs. The next generation of Fujitsu SPCs, currently under development, begins with the 606 product, and continues with the SCSI 3 offering. It is an Ultra SCSI product (it uses a parallel bus) that is pin-for-pin and software compatible with the 605. The 606 offers a simple migration path for designs that need to move to SCSI 3 performance levels.

In the next few pages, we provide a summary of Fujitsu's most recently developed products, the 604L, 605 and 606 SPCs.



## **Individual Products: MB8660X Interface Distinctions**

The SCSI bus interface and MPU interface are the two main features that distinguish the 604L, 605, 606 and future 60Y devices. The chart below shows the interfaces for each parallel bus product. (Serial bus development will begin later in 96/97, as shown in the roadmap on the previous page).

The MB86604L is an 8-bit, Fast -10 SCSI 2 product with a generic MPU interface.

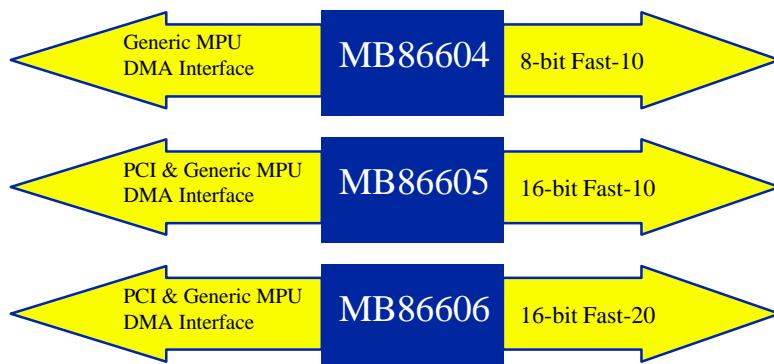
The MB86605 is a 16-bit, Fast-10 SCSI 2 product with options for either a generic MPU interface or a PCI bus interface. (We explain the PCI bus interface when we describe the specific features of the MB86605, on page 16.) The MB86605 marks the end of Fujitsu's SCSI 2 development.

The MB86606 is a 16-bit Fast-20 (parallel ) SCSI 3 product with options for either a generic MPU interface or a PCI bus interface. The MB86606, slated for introduction later in 1996, will mark the beginning of Fujitsu's SCSI 3 development.

### **MB86600 Family of SCSI ICs**

#### System Interface

#### SCSI Bus Interface



## Individual Products: MB86604L

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The summary chart below highlights the key features of the MB86604L SPC.

The MB86604L is an 8-bit Fast-10 SCSI 2 IC featuring on-chip open collector drivers for single-ended configurations.

The MB86604L (as well as the 605 and 606) features a high-speed internal clock that lets the device execute programs and phase changes more quickly than the MB86601. Clock speeds are available in 20-, 30- and 40-MHz ranges.

The MB86604L offers a maximum synchronous transfer rate of 10 MB/sec.

It is pin-for-pin compatible with its predecessor, the MB86601A, and is upward compatible in terms of software. (The MB86601A is still in production, but not recommended for new designs.)

Note also that although the MB86604L is a SCSI 2 product, it is fully compatible with the original SCSI standard.

### MB86604L

- 8-bit Fast-10 SCSI 2 SPC
- Asynchronous transfer = 5 MB/sec
- Synchronous transfer = 10 MB/sec
- 20-, 30- or 40-MHz clock
- 16-bit MPU interface
- 256-byte user program memory (RAM)
- 32-byte data FIFO
- 100-pin plastic QFP package

## Individual Products: MB86605

The summary chart below highlights the key features of the MB86605 SPC.

The MB86605 is a 16-bit Fast-10 SCSI 2 IC featuring the 16-bit MPU interface as well as a high-speed Peripheral Component Interconnect (PCI) interface. PCI is a bus standard, created by Intel, that offers higher performance than other commonly used bus interfaces, such as ISA. Used in virtually all high-end PCs, PCI brings peripheral devices closer to the host microprocessor. Beginning with the 605 product, PCI support is a standard feature of MB8660X products. The MB86605 incorporates a feature, called multiple ID response, that is useful in disk array applications. In the SCSI 2 standard, ANSI specifies a special option for expanding the SCSI bus to support more than 16 devices. Using multiple ID response, the SCSI bus can be configured such that multiple devices can use a single ID line. In a disk array, the many logical units (LUNs) that make up the array (i.e., the multiple internal hard drives) can be configured to access a single bus. In the case of the 605 (and 606), up to 32 LUNs can be attached to a single ID line.

The MB86605 is a new and improved version of the 603 product, and is upward compatible in terms of software. (The 603 is still in production, but not recommended for new designs.) Note also that the 605, a SCSI 2 product, is fully compatible with the original SCSI standard.

### MB86605

- 16-bit Fast-10 SCSI 2 SPC
- Asynchronous transfer = 10 MB/sec
- Synchronous transfer = 20 MB/sec
- 16-bit MPU interface or PCI interface
- 2K user program memory (RAM)
- 64-byte data FIFO
- 144-pin plastic SQFP package
- Multiple ID response for disk array applications

## Individual Products: MB86606

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The summary chart below highlights the key features of the MB86606 SPC.

The MB86606, due to be introduced later in 1996, is a 16-bit Fast-20 parallel SCSI 3 IC. It is Fujitsu's first SCSI 3 product (Note that parallel Fast-20 SCSI 3 is often called Ultra SCSI -- see *Tutorial*.).

Like the 605, the 606 incorporates a PCI bus interface and supports multiple ID response. The 606 is pin-for-pin and fully software compatible with the 605. It provides an easy migration path for designs that want to move to Ultra SCSI performance levels.

What distinguishes the 606 from the other MB8660X products is transfer speed. Using Fast-20 technology, the 606 offers synchronous data transfer rates of up to 40 MB/sec. The 606 is fully software compatible with the 605. This simplifies the migration path from the 605 and SCSI 2 to the 606 and SCSI 3.

### MB86606

- 16-bit Fast 20 SCSI 3 SPC
- Asynchronous transfer = 10 MB/sec
- Synchronous transfer = 40 MB/sec
- 16-bit MPU interface or PCI interface
- 2K user program memory (RAM)
- 512-byte data FIFO
- 144-pin plastic SQFP package
- Multiple ID response for disk array applications

## Conclusion

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The MB8660X product line offers several features and benefits:

- Core architecture approach for faster, easier migration. Pin-for-pin and software compatibility means faster performance upgrades.
- Internal processor, user program memory and on-chip registers for better designs.
- Extensive interrupt reporting and on-chip debug tools for faster development.
- Product-specific features (such as PCI bus interface and multiple ID response) for high-performance PC and disk array applications.
- Strong roadmap of Fast SCSI products today with Ultra SCSI and Serial SCSI versions for tomorrow.

In the next section, Design Tools, we present the software tools used to design with Fujitsu's MB8660X family of SPCs.

	MB86604L	MB86605	MB86606
Implementation	Parallel Fast-10 SCSI 2	Parallel Fast-10 SCSI 2	Parallel Fast-20 SCSI 3 (Ultra SCSI)
SCSI Bus Width	8-bit	16-bit	16-bit
Asynchronous Transfer	5 MB/sec	10 MB/sec	10 MB/sec
Synchronous Transfer	10 MB/sec	20 MB/sec	40 MB/sec
PCI Interface	No	Yes	Yes
User RAM	256 Byte	2K Byte	2K Byte
Data FIFO	32 Byte	64 Byte	512 Byte
SCAM Support	Yes	Yes	Yes
Multiple ID Response	No	Yes	Yes
Package Type	100 plastic QFP	144 plastic SQFP	144 plastic SQFP