Serial Communications Adapter

Description

The HD64570 Serial Communications Adapter (hereinafter referred to as SCA) is a high-speed, high-performance data communication controller providing efficient, high-performance communication protocol processing at low cost.

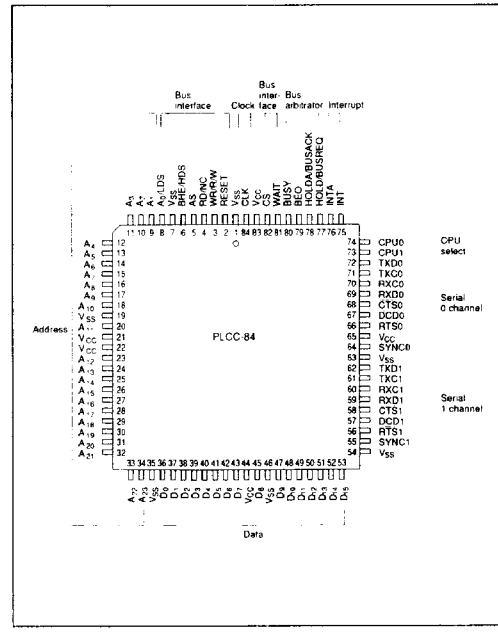
The SCA incorporates powerful key functions such as a two-channel multiprotocol serial communications interface (MSCI), a four-channel direct memory access controller (DMA controller) with chained-block transfer function, and a four-channel timer. The built-in MSCI, supporting various communication protocol modes such as asynchronous, byte synchronous, and bit synchronous modes, allows serial communications using protocols such as HDLC. In addition, the SCA supports four types of 8/16-bit bus interfaces, allowing a direct interface with the host MPU. This bus interface capability combined with 32-byte deep receive and transmit FIFOs in the MSCI can provide high throughput for many communication systems. Accordingly, the SCA can be widely adopted to a computer communication controller that requires multi-channel serial communications, PBXs, and office automation equipment such as personal computers and facsimiles.

*For details about HD64570 specifications, please refer to "HD64570 SCA User's Manual" (Order Number M50T007).

SCA Features

- Multiprotocol Serial Communications Interface (MSCI)
  - —Two full duplex channels
  - —Asynchronous, byte synchronous (mono-sync, bi-sync, or external synchronous), or bit synchronous (HDLC or loop) modes
  - —32-byte deep for both receive and transmit buffers
  - —Transmission and reception control using modem control signals ($\overline{RTS}$, $\overline{CTS}$, and $\overline{DCD}$)
  - —Advanced digital PLL (ADPLL) function
    - —Clock extraction
    - —Noise suppression for receive data and receive clock
  - —Baud rate generator
  - —Interrupt request
  - —Maximum transfer rate: 7.1 Mbps (f = 10 MHz)
- Direct Memory Access Controller (DMA Controller)
  - —Four channels
  - —DMA transfer between memory and built-in MSCI
  - —Chained block transfer in bit synchronous mode
  - —Programmable channel priority
  - —Programmable bus release and channel switch conditions
- Timer
  - —Four channels
  - —16-bit reloadable upcounter timer
  - —Interrupt request
- Wait State Controller
  - —Wait state control using an external pin or software
- Interrupt Controller
  - —Interrupt request to the MPU
  - —20 interrupt sources
  - —Programmable acknowledge cycle
- Bus Arbitrator
  - —Bus arbitrator between the built-in DMA controller and external bus masters
  - —Multiple serial channels realized by daisy chain structure
- Bus Interface
  - —HD641016, HD64180, and other two other types of 16-bit bus interfaces available by mode switching through external pins
  - —8-bit or 16-bit programmable bus width
  - —Byte swap function
  - —16 Mbytes of address space
- Maximum operation frequency
  - —10 MHz
- Package
  - —CP-84 (84-pin PLCC)

SCA Pin Arrangement



The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Table 2-1 CP-84 Pin Configuration

Pin No.	Pin Name CPU Mode 0	CPU Mode 1	CPU Mode 2	CPU Mode 3
1	V_{SS}			
2	$\overline{RESET}$			
3	$\overline{WR}$	$\overline{WR}$	R/$\overline{W}$	R/$\overline{W}$
4	$\overline{RD}$	$\overline{RD}$	N.C.	N.C.
5	$\overline{AS}$			
6	$\overline{BHE}$	N.C.	$\overline{HDS}$	$\overline{HDS}$
7	V_{SS}			
8	A_0	A_0	$\overline{LDS}$	$\overline{LDS}$
9	A_1			
10	A_2			
11	A_3			
12	A_4			
13	A_5			
14	A_6			
15	A_7			
16	A_8			
17	A_9			
18	A_{10}			
19	V_{SS}			
20	A_{11}			
21	V_{CC}			
22	V_{CC}			
23	A_{12}			
24	A_{13}			
25	A_{14}			
26	A_{15}			
27	A_{16}			
28	A_{17}			
29	A_{18}			
30	A_{19}			
31	A_{20}			
32	A_{21}			
33	A_{22}			
34	A_{23}			
35	V_{SS}			
36	D_0			
37	D_1			
38	D_2			
39	D_3			
40	D_4			
41	D_5			
42	D_6			

Pin No.	Pin Name CPU Mode 0	CPU Mode 1	CPU Mode 2	CPU Mode 3
43	D_7			
44	V_{CC}			
45	D_8			
46	V_{SS}			
47	D_9			
48	D_{10}			
49	D_{11}			
50	D_{12}			
51	D_{13}			
52	D_{14}			
53	D_{15}			
54	V_{SS}			
55	$\overline{SYNC1}$			
56	$\overline{RTS1}$			
57	$\overline{DCD1}$			
58	$\overline{CTS1}$			
59	RxD1			
60	RxC1			
61	TxC1			
62	TxD1			
63	V_{SS}			
64	$\overline{SYNC0}$			
65	V_{CC}			
66	$\overline{RTS0}$			
67	$\overline{DCD0}$			
68	$\overline{CTS0}$			
69	RxD0			
70	RxC0			
71	TxC0			
72	TxD0			
73	CPU1			
74	CPU0			
75	$\overline{INT}$			
76	$\overline{INTA}$			
77	HOLD	$\overline{BUSREQ}$	$\overline{BUSREQ}$	$\overline{BUSREQ}$
78	HOLDA			
79	$\overline{BEO}$			
80	$\overline{BUSY}$			
81	WAIT			
82	$\overline{CS}$			
83	V_{CC}			
84	CLK			

Note: Refer to section 2.2, Pin Functions, for details on CPU modes.

2.2 Pin Functions

The SCA pin functions are summarized in table 2-2.

Table 2-2 SCA Pin Functions

Type	Symbol	I/O	Function
Power supply	V_{CC}	I	Power supply
	V_{SS}	I	Ground
Clock	CLK	I	System clock
Reset	$\overline{RESET}$	I	Reset
Address bus	A_0 to A_7	I/O	Address bus
	A_8 to A_{23}	O	Address bus
Address bus	D_0 to D_{15}	I/O	Data bus
Bus interface	$\overline{RD}$	I/O	Read
	$\overline{WR}$	I/O	Write
	R/$\overline{W}$	I/O	Read/write
	$\overline{HDS}$	I/O	Higher data strobe
	$\overline{LDS}$	I/O	Lower data strobe
	$\overline{BHE}$	I/O	Higher byte access strobe
	WAIT	I/O	Wait request
	$\overline{CS}$	I	Chip select
	$\overline{AS}$	I/O	Address strobe
System control	$\overline{BUSREQ}$	O	Bus request
	$\overline{BUSACK}$	I	Bus request acknowledge
	HOLD	O	Hold request
	HOLDA	I	Hold request acknowledge
	$\overline{BEO}$	O	Bus enable
	$\overline{BUSY}$	I/O	Bus busy
	CPU0, CPU1	I	Bus interface mode selection (Refer to table 2-3.)
Interrupt	$\overline{INT}$	O	Interrupt request
	$\overline{INTA}$	I	Interrupt request acknowledge
MSCI	TXD0, TXD1	O	Transmit data
	RXD0, RXD1	I	Receive data
	TXC0, TXC1	I/O	Transmit clock
	RXC0, RXC1	I/O	Receive clock
	$\overline{RTS0}$, $\overline{RTS1}$	O	Modem control ($\overline{RTS}$)
	$\overline{DCD0}$, $\overline{DCD1}$	I	Modem control ($\overline{DCD}$)
	$\overline{CTS0}$, $\overline{CTS1}$	I	Modem control ($\overline{CTS}$)
	$\overline{SYNC0}$, $\overline{SYNC1}$	I/O	Synchronization

Table 2-3 CPU Mode (Bus Interface Mode) Selection by CPU0 and CPU1

CPU0	CPU1	CPU Mode
0	0	Mode 0 (80 series 16-bit CPU)
0	1	Mode 1 (HD64180)
1	0	Mode 2 (HD641016)
1	1	Mode 3 (68 series 16-bit CPU)

SCA Block Diagram