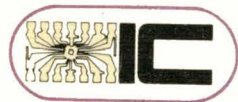
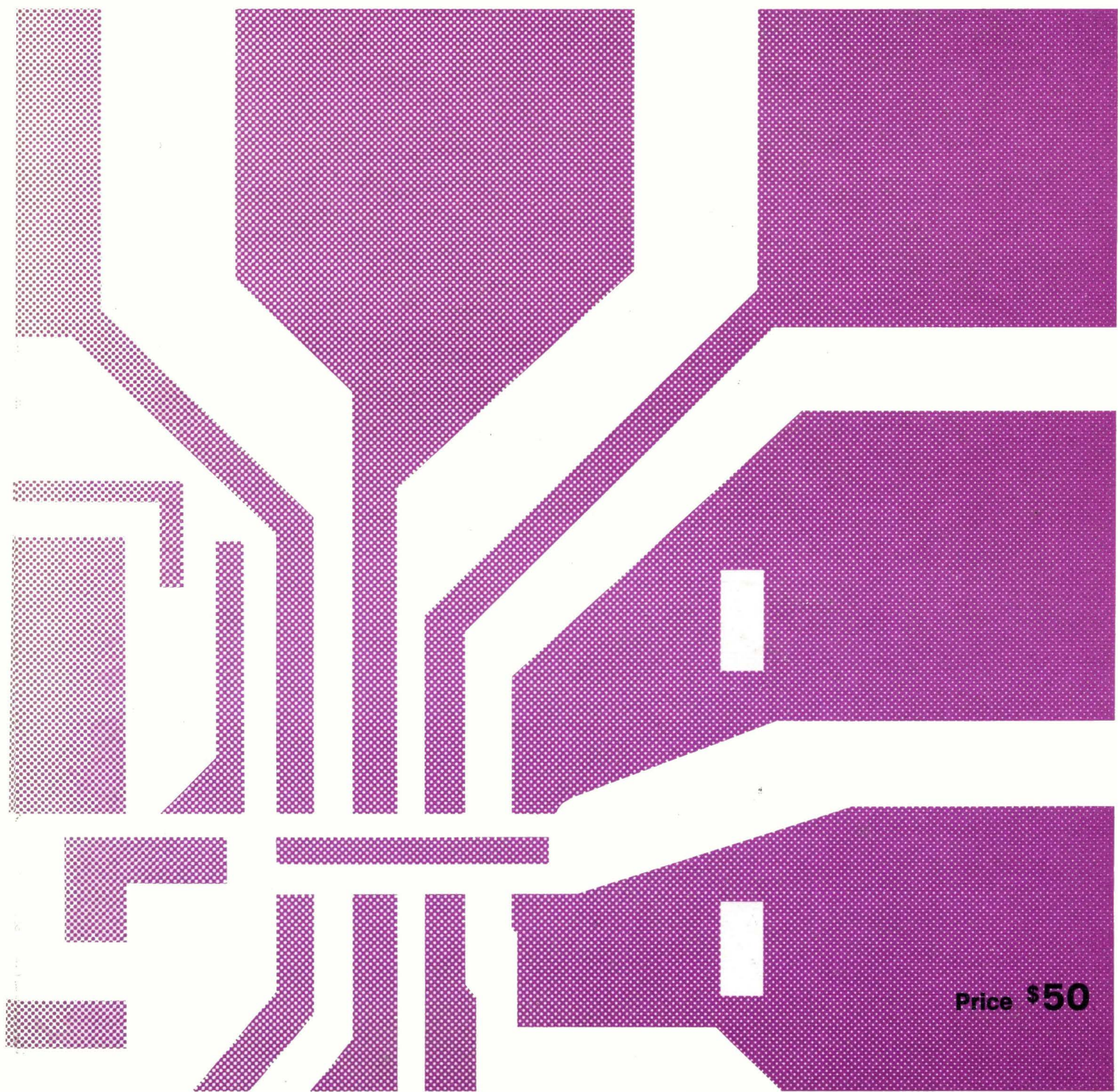


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THE FIRST STEP

For more than two years, the editorial/research staff of one of the largest publishers in the electronics industry has been gathering, correlating and updating the rapidly changing product profile of the IC industry.

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The Alternate Source Directory starts on page 1030.

APPLICATION NOTE DIRECTORY This is the most complete directory of its kind. It permits you to survey rapidly this entire field of literature, and locate any and all information on any device.

The Application Note Directory provides a synopsis and source for both application notes and microprocessor design books. The notes are arranged by subject and cross referenced by device number in the Part Number and Product Indexes. This permits you to find information either by topic or part number.

The Application Note Directory starts on page 66.

MANUFACTURERS & DISTRIBUTORS DIRECTORY This directory is literally your communications guide for ICs. It places at your fingertips the names and phone numbers of manufacturers, field sales offices, representatives and distributors. In addition, if you need to contact the manufacturer directly, it provides special information on where and whom to call to quickly and efficiently obtain the information you need.

The Manufacturers and Distributors Directory starts on page 1084.

PART NUMBER GUIDE The Part Number Guide describes each manufacturer's system of prefixes and suffixes. It allows you to decode the manufacturer's model numbers into temperature range, packages, functions, etc.

MILITARY PARTS DIRECTORY The Military Parts Directory shows which manufacturers will test devices to MIL-STD-883 and/or perform other environment screening. This directory also provides a translation of the Defense Electronic Centers Qualified Products List. It shows all the devices on the list, translates the military numbers into commercial equivalents, gives functional titles and tells which manufacturers are currently authorized to supply each type.

The Part Number Guide starts on page 57.

The Military Parts Directory starts on page 123.

PART NUMBER INDEX This index strips away the prefixes and suffixes and lists all ICs in numerical sequence. The index shows the complete model number, manufacturer, and page locations on which each item appears. It covers device listings in both the reference and data portions of the Master Selection Guide as well as the Application Note Directory, and tells you quickly and concisely where to find information on any IC listed in the Master.

The Part Number Index begins on page 4.

PRODUCT INDEX The Product Index is similar to the Part Number Index but is arranged by manufacturer. All of a manufacturer's products listed in the Master are indicated here along with convenient page and line references.

The Product Index starts on page 1122.

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For the first time, in a single source reference, you have at your fingertips the identity of each individual IC you will want to consider for a given application, and data on the most important ones. Inevitably, it will be your first source of information when you are looking for a product.

DETAILED INFORMATION ON MANUFACTURERS' MOST SIGNIFICANT PRODUCTS

Many manufacturers have submitted detailed information on their latest and most significant products. This

data has been included in the MASTER, and we know it will help you select the ICs you need.

Of course, the more complete the information supplied, the more useful a tool the MASTER will be. A number of firms have made the investment to inform you. We know they would appreciate feedback from you on what they've done and how they could improve their presentations in future issues.

Some firms did not submit data sheets for inclusion in this edition of the MASTER. You may find this lack of data an inconvenience. Don't hesitate to give them your opinion.

We expect future editions of the MASTER to contain more of the kind of information you need and want, on an even greater representation of manufacturers and product lines. But only if you tell them what you think.

DIGITAL

- CMOS
- ECL
- HNIL/HTL
- Industrial/Consumer Circuits
- TTL
- TTL — High Speed
- TTL — Low Power Schottky
- TTL — Schottky
- Special

INTERFACE

- Analog Switches
- A/D Converters
- D/A Converters
- Display Drivers
- Error Checking Circuits
- Keyboard Encoders
- Line Drivers, Receivers, and Transceivers
- Memory and Peripheral Drivers
- Sense Amplifiers
- Serial Transmitters-Receivers

LINEAR

- Amplifiers, Special Purpose
- Arrays
- Comparators
- Followers
- Industrial/Consumer Circuits
- Operational Amplifiers
- Phase Locked Loop Circuits
- Telecommunication Circuits
- Timers
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MEMORY

- Character Generators
- Code Converters
- EAROMs
- FIFOs, LIFOs
- PROMs
- RAMs
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PART NUMBER INDEX

This index shows the page and line on that page where each device appears in the Master Selection Guide and the Application Note Directory. The list is prepared by a computer from the data in these sections so every device in them is listed. The devices are arranged in order by basic numbers so similarly numbered devices from various manufacturers are grouped together. Bold faced listings lead to the data supplied by the manufacturers. Use this index to locate key operational characteristics, application notes, and devices data whenever you have a model number.

how to use the part number index

This Part Number Index is arranged in alpha-numeric sequence, ignoring the manufacturer's prefixes and suffixes and using the basic model numbers. This basic number sequence is sorted by reading the digits from **left to right**, assuming that letters come before numbers. (As an example, these numbers would appear in the following order: 5301, 531, 54H01, 54139, 5414.) Under each basic number, the manufacturer's name and full model number is listed. The page references to 69 through 120 lead to application notes. Page references saying "see page —" lead to manufacturers' data. Each page number is followed by a dash number that indicates the location on the page where the data appears.

The arrangement of this index by base number gives you several advantages. It allows you to find a device by its basic number whether or not you know the name of the manufacturer or the manufacturer's prefixes. Also it groups similar devices together so that when you are looking for data you can quickly determine if the data has been provided in the book by any of the manufacturers and where that data is. Similarly it groups any references to application notes close together so that you do not need to guess which manufacturer might publish application notes on a device before you can locate them.

Once you become familiar with the alpha-numeric numbering sequence, you'll find that this index is very easy to use.

Note: Devices identified by Alpha characters only, are listed first.

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9374	Fairchild	9374C	515- 8				246-116		Fairchild	9624M	235- 48
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9377	Fairchild	9377	82- 13		Fairchild	96S02M	250-126		Fairchild	9625M	235- 37
9383	Fairchild	9383	82- 13	9600	AMD	9600C	233- 64	9627	Fairchild	9627	80- 4
9386	Fairchild	9386C	230-133		AMD	9600M	233- 65		Fairchild	9627C	522- 27
	Fairchild	9386M	230-134		Fairchild	9600	82- 13		Fairchild	9627M	522- 28
9390	Fairchild	9390	82- 13		Fairchild	9600C	233- 68	9634	Fairchild	9634	80- 4
9391	Fairchild	9391	82- 13		Fairchild	9600M	233- 69	9635	Fairchild	9635	80- 4
9392	Fairchild	9392	82- 13	9601	AMD	9601C	233- 47	9636	Fairchild	9636	80- 4
9393	Fairchild	9393	82- 13		AMD	9601M	233- 48	9637	Fairchild	9637	80- 4
9394	Fairchild	9394	82- 13		Fairchild	9601	82- 13	9638	Fairchild	9638	80- 4
9395	Fairchild	9395	82- 13		Fairchild	9601C	233- 49	9640	Fairchild	9640	80- 4
9396	Fairchild	9396	82- 13		Fairchild	9601M	233- 50	9650	Fairchild	9650	97- 7
9400	GI	AY3-9400	611- 43		ITT	ITT9601-1	233- 51	9651	AMI	S9651	
9401	AMD	9401C	698- 47		ITT	ITT9601-5	233- 52				see page 254
	AMD	9401M	698- 48		Motorola	MC9601	233- 54	9660	AMI	S9660	
	Fairchild	9401C	236- 8		National	DM9601	233- 56				see page 254
			517- 2		Raytheon	RF9601	233- 58	9664	Fairchild	9664C	516- 43
	Fairchild	9401M	236- 9		SW	SW9601	233- 62	97C09	National	AM97C09C	499- 41
			517- 3	9602	AMD	9602C	233- 88	97C10	National	AM97C10C	499- 52
9403	Fairchild	9403C	250- 45		AMD	9602M	233- 89	97C11	National	AM97C11C	499- 7
			680- 20				233- 92	97C12	National	AM97C12C	499- 18
	Fairchild	9403M	250- 46		Fairchild	9602	82- 13	9702	AMD	9702	683- 23
			680- 21		Fairchild	9602C	233- 95		AMD	9702-1	683- 20
9404	Fairchild	9404C	248- 5		Fairchild	9602M	233- 96	9709	National	AM9709C	499- 42
			680- 54		ITT	ITT9602-1	233- 97	9710	National	AM9710C	499- 53
	Fairchild	9404M	248- 6		ITT	ITT9602-5	233- 98	9711	National	AM9711C	499- 8
			680- 55		Motorola	MC9602	233-100	9712	National	AM9712C	499- 19
9405	Fairchild	9405	853- 1		National	DM9602	233-102	9900	TI	TMS9900	861- 1
	Fairchild	9405C	248- 28		Raytheon	RF9602	233-104	9996	AMI	S9996	
	Fairchild	9405M	248- 29		Signetics	N9602	233-105				see page 706
9410	Fairchild	9410C	231-163		Signetics	S9602	233-106				
			687- 84		SW	SW9602	233-107				
	Fairchild	9410M	231-164	9603	Fairchild	9603	82- 13				
	GI	AY3-9410	611- 44	9607	Fairchild	9607	525- 72				
9411	AMI	S9411	73- 6	96101	Fairchild	96101	226-139				
9412	AMI	S9412	73- 7	9612	Fairchild	9612	80- 4				
			73- 8		Fairchild	9612C	519- 4				
					Fairchild	9612EC	519- 6				
					Fairchild	9612M	519- 5				
				9613	Fairchild	9613	80- 4				
					Fairchild	9613C	522- 17				
					Fairchild	9613M	522- 18				
				9614	AMD	9614	74- 14				
					AMD	9614C	519- 7				
					AMD	9614M	519- 8				
9414	AMI	S9414			Fairchild	9614	80- 4				
			see page 254		Fairchild	9614C	519- 9				
95h00	Fairchild	95H00C	699- 78		Fairchild	9614M	519- 10				
95H90	Fairchild	95H90C	610- 56		ITT	ITT9614-1	519- 11				
	Fairchild	95H90M	252- 64		ITT	ITT9614-5	519- 12				
			610- 57	9615	AMD	9615	74- 14				
9500	GI	AY5-9500	611- 45		AMD	9615C	522- 3				
95000	Fairchild	F95000	216- 24		AMD	9615M	522- 4				
95002	Fairchild	F95002	216- 12		Fairchild	9615	80- 4				
95003	Fairchild	F95003	216- 14		Fairchild	9615C	522- 5				
95004	Fairchild	F95004	216- 10		Fairchild	9615M	522- 6				
9501	Collins	CRC9501	503- 13		ITT	ITT9615-1	522- 7				
95010	Fairchild	F95010	216- 2		ITT	ITT9615-5	522- 8				
95016	Fairchild	F95016	216- 1	9616	AMD	9616C	518- 34				
9502	Collins	CRC9502	503- 14		Fairchild	9616	80- 3				
95029	Fairchild	F95029	216- 3				80- 4				
9503	Collins	CRC9503	69- 6		Fairchild	9616C	518- 35				
			253- 6		Fairchild	9616E	518- 36				
9504	Collins	CRC9504	69- 6								
			253- 5								
9509	Collins	CRC9509	499- 92								
9510	Collins	CRC9510	499-103								
95101	Fairchild	F95101	216- 17								
95102	Fairchild	F95102	216- 16								
95103	Fairchild	F95103	216- 15								
95105	Fairchild	F95105	216- 13								

Pages from: 69 through 120 indicate APPLICATION NOTES.
 Pages from: 201 through 1029 indicate MASTER SELECTION GUIDE listings.

ABBREVIATIONS OF COMPANY NAMES

AD	Analog Devices
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
AMS	Advanced Memory Systems
Analogic	Analogic Corp.
Beckman	Beckman Instruments, Helipot Division
Burr-Brown	Burr-Brown Research
Cermetek	Cermetek
CMA	Consumer Microcircuits of America
Collins	Collins Radio
Datel	Datel Systems
DDC	ILC Data Devices Corp.
EA	Electronic Arrays
EMM/Semi	EMM Semi, Div. of Electronic Memories & Magnetics
Exar	Exar Integrated Systems
Fairchild	Fairchild Semiconductor
Ferranti	Ferranti Electric
GI	General Instrument
Harris	Harris Semiconductor
Hitachi	Hitachi America, Ltd.
Hughes	Hughes Aircraft Co., MOS Division
Hybrid Sys.	Hybrid Systems
IMI	International Microcircuits, Inc.
Intech	Intech
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
IPI	Integrated Photomatrix, Inc.
ITT	ITT Semiconductors
Lithic Sys.	Lithic Systems
Litronix	Litronix
LSI Comp.	LSI Computer Systems
Micro Net	Micro Networks
Micropac	Micropac Industries
Micro Power	Micro Power Systems
Mitsubishi	Mitsubishi International
MMI	Monolithic Memories, Inc.
MOS	MOS Technology
Mostek	Mostek
Motorola	Motorola Semiconductor
National	National Semiconductor
NCR	National Cash Register, Microelectronics Div.
NEC	NEC Microcomputers
Nippon	Nippon Electric Co.
Nitron	Nitron
Nortec	Nortec Electronics
NPC	Nucleonic Products Co.
OKI	OKI Electronics of America, Inc.
Panasonic	Panasonic, Matsushita Electric Corp.
Plessey	Plessey Semiconductors
PMC	Power Monolithics Co.
PMI	Precision Monolithics, Inc.
Ragen	Ragen Semiconductor
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
Reticon	Reticon
Rockwell	Rockwell International, Microelectronic Div.
Sanken	Sanken Electric
SGS	SGS-ATES Semiconductor
Signetics	Signetics
Silicon G	Silicon General
Siliconix	Siliconix
SMC	SMC Microsystems Corp.
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSS	Solid State Scientific
SW	Stewart-Warner Microcircuits
Synertek	Synertek
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
TI	Texas Instruments
TMX	TMX, Inc.
Toshiba	Toshiba
TRW	TRW
Transitron	Transitron Electronics
Western	Western Digital

PART NUMBER GUIDE

Each IC manufacturer has his own unique method of identifying products, usually through a system of device number prefixes and suffixes. This Part Number Guide is arranged alphabetically by manufacturer and describes each company's part number system. JAN nomenclature is also covered.

Manufacturer		Part Number		Example		
		Prefix	Suffix	Prefix	Device	Suffix
ADVANCED MEMORY SYSTEMS	Classification	Package		Device: AMS 6003		
	IC Circuits - 91	3A 16 Pin Flat Pack		91	6 003	11 6DP
	Sub Category	3B 22 Pin Flat Pack		Classification	Device	Suffix
	0 Custom MOS	6A 14 Pin DIP				
	1 Bipolar RAM	6B 16 Pin DIP		Sub-Category	Device	Suffix
	2 Bipolar	6C 24 Pin DIP				
	3 Bipolar ROM	6D 22 Pin DIP		Test Spec	Device	Suffix
	4 CMOS	6E 18 Pin DIP				
	5 SOS	P Plastic		Package Code	Device	Suffix
	6 PMOS					
7 NMOS						
ADVANCED MICRO DEVICES	Functional Group	Package		Prefix	Device	Suffix
	25 MSI	D Hermetic DIP		AM25	S 05	D M
	26 Computer Interface	P Molded		Functional Group	Device	Suffix
	27 Bipolar Memory	F Flat				
	28 MOS	X Dice		Type	Device	Suffix
	90 MOS	Temperature Range				
	91 MOS	C Commercial		Device Number	Device	Suffix
	Type	M Military				
	L Low Power			Package	Device	Suffix
	S Schottky					
LS Low Power Schottky			Temperature Range	Device	Suffix	
(Blank) Standard						
AMERICAN MICROSYSTEMS	Family	Package Type		Prefix	Device	Suffix
	S Standard	1 Plastic		S	1103X	2 P
		2 Cer-DIP		Family	Device	Suffix
		3 SLAM				
		4 Ceramic (Three Layer)		Version	Device	Suffix
		5 TO Type				
		Package/Pins		Package Type	Device	Suffix
		C 22 Pin Plastic or Cer-DIP				
		D 14 Pin Plastic or Ceramic		Number of Pins	Device	Suffix
		F 12 Pin TO				
	H 16 Pin Cer-DIP, SLAM, or Ceramic					
	I 28 Pin Cer-DIP or SLAM					
	L 24 Pin Cer-DIP					
	M 40 Pin SLAM					
	P 18 Pin Plastic or Cer-DIP					
	T 40 Pin Plastic					
	U 16 Pin Plastic					
	W 24 Pin Plastic					
	Z 28 Pin Plastic					
ANALOG DEVICES	AD Analog Devices	Temperature Range		Prefix	Device	Suffix
		J,K,L Commercial Grade		AD	7516	JM
		S,T Military Grade		Temperature Range	Device	Suffix
		Package				
		DN Ceramic DIP		Package	Device	Suffix
		D 8 Pin Ceramic DIP				
		E 14 Lead Plastic DIP				
		F Ceramic Flatpack				
		H TO-5 type Can				
		N Plastic DIP				
COLLINS RADIO		Package		Prefix	Device	Suffix
		1 Ceramic DIP		CRC	1504	-1 -2
		2 Flatpack		Package	Device	Suffix
		3 Plastic DIP				
		Temperature		Temperature Range	Device	Suffix
		1 -55°C to 125°C				
		2 -25°C to 85°C				
		3 0°C to 70°C				

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Manufacturer		Prefix	Part Number	Suffix	Example		
DATEL	Family		Package		Prefix	Device	Suffix
	ADC A/D Converters		1 14 Pin DIP		AM	490	2 A
	AM Amplifiers		2 TO-99				
	SHM Sample-Hold						
			Temperature				
			C 0°C to 70°C		DAC	HY12B	C
			M -55°C to 125°C				
ELECTRONIC ARRAYS	Family		Package		Prefix	Device	Suffix
	10 Static Shift Register		D Hermetic DIP		EA	1500A	DM
	12 Dynamic Shift Register		F Flat Pack				
	15 N Channel RAM		P Molded DIP				
	20 Keyboard Encoder		T TO-Can				
	3X Dynamic ROM		X Dice				
	4X Static ROM						
			Temperature Range				
			C 0°C to 70°C				
			I -55°C to 85°C				
			L -55°C to 100°C				
			M -55°C to 125°C				
			X Other				
Note: Alternate source devices follow original manufacturer's part number and marking system:							
EMM/SEMI			Package	Temperature Range	Prefix	Device	Suffix
A. Semi Product			D Dice	C 0°C to 70°C	SEMI	4402	X X
			C Dual in Line, Ceramic	S -25°C to 85°C			
			P Dual in Line, Plastic	M -55°C to 125°C			
			F Flat Package, Ceramic				
			S Special Packages				
B. General Instrument Second Source Marking		Family	Package		Prefix	Device	
		RO ROM	3 Dual in Line		SEMI	RA-3-4256	
		RA RAM					
		CP Microprocessor					
EXAR INTEGRATED SYSTEMS	XR Exar		Grade		Prefix	Device	Suffix
			C Commercial		XR	567	CP
			M Military (Ceramic package and -55°C to 125°C)				
			() The absence of C or M indicates a commercial part with tighter specs				
			Package				
			P Plastic				
			N Ceramic (Dice available)				
FAIRCHILD	Family		Package		Prefix	Device	Suffix
	F Fairchild		C Chip (Dice)		μA	741	AHM
	SH Hybrid		D Ceramic DIP				
	μA Linear		E Plastic Can				
			F Flat Pac				
			H Metal Can				
			J Metal Power Package (TO-66)				
			K Metal Power Package (TO-3)				
			P Plastic DIP				
			T Mini DIP				
			U Power Package (Molded, TO-220)				
			W Plastic TO-92				
			Temperature — Check Device Data for Specific Values				
			C 0°C to 70°C/75°C (CMOS -40°C to 85°C)				
			L MOS -55°C to 85°C Hybrid -20°C to 85°C				
			M -55°C to 125°C				
Alternate source devices may follow original manufacturer's part number and marking systems.							

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Manufacturer	Part Number	Prefix	Suffix	Example	
GENERAL INSTRUMENT	Designation		Package Identification (Not Marked on Plg.)	Prefix Device Suffix	
	CU Array		01 Dice	RO-6 WXYZ (XX)	
	AY Array		12 8 Lead DIP	Designation	
	DL Shift Register Dynamic \geq 50 Bits		14 TO-5 4 Lead		
	DS Shift Register Dynamic $<$ 50 Bits		15 TO-78 8 Lead	Temp. & Processing	
	LC Linear Circuit		16 TO-5 8 Lead		
	LG Logic Cells		17 TO-5 8 Lead High Profile	Description	
	MEN N an P Channel FETs		21 TO-5 10 Lead		
	MU Multiplexer		22 TO-5 10 Lead Isolated	Package Identification	
	RA RAM		23 TO-100 10 Lead		
	RO ROM		29 24 Lead Plastic DIP		
	SL Shift Register Static \geq 50 Bits		30 14 Lead Plastic DIP		
	SS Shift Register Static $<$ 50 Bits		31 16 Lead Plastic DIP		
	Temperature and Processing				
	0 MTOS -55°C to 85°C		32 24 Lead Plastic DIP		
	1 MTOS 0°C to 70°C		33 40 Lead Plastic DIP		
	4 N Channel		35 36 Lead Plastic Flat Pack		
	5 MTNS 0°C to 70°C		51 TO-8 12 Lead Low Profile		
	6 -55°C to 125°C		55 16 Lead DIP		
	7 MTNS		60 10 Lead Flat Pack		
	8 Silicon Gate -55°C to 125°C		61 14 Lead Flat Pack		
	9 Silicon Gate 0°C to 70°C		62 16 Lead Flat Pack		
	Description				
	Multiplexers				
	WX Indicates Typical R_{ds} (on) in hundred ohms steps:		63 20 Lead Flat Pack		
	01 \leq 100 ohms		64 24 Lead Flat Pack		
	02 \leq 200 ohms		65 40 Lead Flat Pack		
	03 \leq 300 ohms, etc.		66 36 Lead		
	YZ Total Number of Channels		68 44 Lead Flat Pack		
	Custom				
	Custom Number Assigned		69 14 Lead DIP		
	ROM/RAM				
	WXYZ Total Number of Bits		71 16 Lead DIP		
	Shift Registers				
	W Indicates the number of redundant configurations:		72 24 Lead DIP .6 MIL Centers		
	1 Single 3 Triple		73 24 Lead DIP .5 MIL Centers		
	2 Dual 4 Quad, etc.		74 40 Lead DIP .6 MIL Centers		
	XYZ Total number of bits per configuration		75 40 Lead DIP 1.05 MIL Centers		
	Arrays/Linear/Logic				
	WXYZ Arbitrary Number Assigned		76 28 Lead DIP		
			77 18 Lead DIP		
			79 24 Lead DIP .6 MIL Centers		
			80 14 Lead Ceramic RIP		
			81 16 Lead Ceramic DIP		
	HARRIS	Family		Temperature Range	Prefix Device Suffix
A Analog			2 -55°C to 125°C	H M I . 7620 5	
D Digital			4 -25°C to 85°C	Family	
I Interface			5 0° to 75°C		
M Memory			6 100% 25°C Probe (Dice only)	Package	
Package					
1 DIP			8 Dash 8 Program, MIL-STD-883, Class B	Temperature Range	
2 TO-5 Type			Example: HA-2700-8		
7 Mini DIP			9 -40°C to 85°C (4000 Series CMOS)		
9 Flat Pack			Exceptions		
0 Chip Form			The 54C/74C CMOS Family temperature designation is contained in the Part Number		
Exceptions					
HPROMX-0152-X			Example:		
HPROMX-1024-X			54CXX -55°C to 125°C		
HPROMX-8256-X			74CXX 0°C to 70°C		
ITT SEMICONDUCTOR	ITT		Temperature Range	Prefix Device Suffix	
	SAK		1 -55°C to 125°C	ITT 709A 1D	
	SAH		5 0°C to 70°C	Temperature Range	
	TAA		(0°C to 75°C Digital)		
	Package				
B Flat Package		C TO-5 Style	Package		
D Ceramic DIP		N Plastic DIP			
INTEL	Package			Prefix Device Suffix	
	C Ceramic (Metal Lid) DIP (Hermetic)			P 1101A	
	D CerDIP (Glass Seal) DIP (Hermetic)			Package	
	F Flat Package				
	P Plastic DIP				
M Metal Can Package (Hermetic)					
INTERNATIONAL MICROCIRCUITS	MM			Prefix Suffix	
	Master MOS Array			MM 6 013 B-P 20	
	SCC			Family	
	Special Custom Circuit				
	Family				
	1 Small Chip		Package	Metal Option	
	2 Special Size		C Ceramic		
	3 Medium Chip		P Plastic DIP	Change Level	
	6 Large Chip		S Special		
	Package				
				Package	
				No. of Pins	

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Manufacturer		Prefix	Part Number	Suffix	Example
INTERSIL	Temperature		Package		Prefix Device Suffix
	A. Hybrid	1 -55°C to 125°C 4 0°C to 70°C	(see last example)		DG 1 26A D D
	Characteristics	5 Analog 7 Digital 9 Interface	Pins (see last example)		Analog Gate Temperature Package No. of Pins
	General Type	0 Gates 1 Amplifiers	Package (see last example)		Prefix Device Suffix
			Pins (see last example)		IH 5 0 01 P A
					Intersil Hybrid Characteristics General Type Package No. of Pins
B. Linear, Low Power, Watch & Clock Circuits	Circuit	L Linear CM Watch, Clock	Temperature		Prefix Device Suffix
			C Commercial (0°C to 70°C) I Industrial (-20°C to 70°C) M Military (-55°C to 125°C)		IC X 8001 C T Z
			Package (see last example)		Intersil Circuit Temperature Package No. of Pins
			Pins (see last example)		
C. Memory Circuits	Process	5 Bipolar 6 CMOS 7 MOS	Temperature		Prefix Suffix
	General Type	0 to 4 Digital 5 Random Access Memory (RAM) 6 Programmable Read Only Memory (PROM) 7 Shift Register	C Commercial (0°C to 75°C) M Military (-55°C to 125°C) N Reduced Military (-20°C to 125°C)		I M 7 6 01 XX C D E
			Package		Intersil Memory Circuit Process General Type Specific Type ROM Pattern Identification (Applicable to ROM only) Temperature Package No. of Pins
			Pins (No. of)		
			H 6 F 22 A 8 G 24 B 10 I 28 C 12 J 32 D 14 K 36 E 16 L 40 N 18 V 8, .230" Pin Circle W 10, .230" Pin Circle Y 8, No. 4 Lead Connected to Case Z 10, No. 5 Lead Connected to Case		

JAN NOMENCLATURE		Device Class	Prefix	Device	Suffix
JAN } M38510	Qualified Device	A Missiles and Manned Spacecraft	JM38510	/XXXXX	B C B
	Military Designation	B General Military			
	Device	C Less Critical Military Applications			
	The "Slash" numbering signifies the specification and specifies the device type. See Military Parts Directory.	Case Outline			
		A 1/4" x 1/4" Flat Pack, 14-Pin B 1/8" x 1/4" Flat Pack, 14-Pin C 1/4" x 3/4" Dual-In-Line, 14-Pin D 1/4" x 3/8" Flat Pack, 14-Pin E 1/4" x 3/4" Dual-In-Line, 16-Pin F 1/4" x 3/8" Flat Pack, 16-Pin G 8-Lead Can H 1/4" x 1/4" Flat Pack, 10-Lead I 10-Lead Can J 1/2" x 1 1/4" Dual-In-Line, 24-Pin K 3/8" x 1/2" Flat Pack, 24-Pin			
		Lead Finish			
		A Kovar or Alloy 42, with Hot Solder Dip B Kovar or Alloy 42, with Bright Acid Tin Plate C Kovar or Alloy 42, with Gold Plate			

PART NUMBER GUIDE

Manufacturer		Part Number			Example			
		Prefix	Suffix		Prefix	Device	Suffix	
LITHIC SYSTEMS	Device Type	(Proprietary Devices)			Prefix	Device	Suffix	
	LA Array	A	Premium	LP	2000	C		
	LP Proprietary	B	Super Premium	Device Type				
	LSS Second Source	C	Commercial					
		E	Entertainment					
MICRO NETWORKS	MN Micro Networks	Temperature Range			Prefix	Device	Suffix	
		(No suffix) 0°C to 70°C			MN	3000	H B	
		E -55°C to 85°C			Temperature Range			
		H -55°C to 125°C			Processing			
	B Processing to 883A Method 5004.2							
MONOLITHIC MEMORIES	Type	Package			Prefix	Device	Suffix	
	0 Character Generator	D	Ceramic (Metal Cap)	H 5 2	05	D		
	2 ROM	F	Flatpac	Performance				
	3 PROM	J	CERDIP	Temperature				
	5 RAM	N	Epoxy	Type				
	7 Computer Logic				Package			
Temperature	Performance							
5 Military TTL	A	And Enable						
6 Commercial TTL	H	High Speed						
	L	Low Power						
MOSTEK	MK Mostek	Package			Prefix	Device	Suffix	
		E	Leadless Chip Carrier	MK	4096	P		
		M	Plastic Flat Package	Package				
		N	Plastic Dual In-line					
	P	Ceramic Dual In-line						
MOTOROLA	Description	Package			Prefix	Device	Suffix	
	MC Packaged Integrated Circuits	F	Flat Ceramic Package	MC	14510	AL		
	MCB Packaged Beam-lead Integrated Circuits. (Followed by F suffix when in flat pack.)	G	Metal Can Package (TO-5 types)	Description				
	MCBC Beam-lead Integrated Circuit Chips	K	Metal Power Package (TO-3 types)	Package				
	MCC Unencapsulated Integrated Circuit Chips	L	Ceramic Dual-In-Line Case					
	MCCF Flip-Chip Linear Integrated Circuits	P	Plastic Package					
	MCE Dielectrically Isolated Integrated Circuits	PQ	IC's Packaged in Staggered-Lead Plastic DIP Packages					
	MCM Integrated Circuit Memories	R	Metal Power Packages (TO-66 types)					
	MFC Low Cast Integrated Circuits packaged in Motorola's unique "Functional-Circuits" plastic package. (Package suffix not used in this device series.)	U	Ceramic Package					
	MLM Pin-for-pin equivalent to Linear Integrated Circuits made by National Semiconductor.							
	NATIONAL	Description	Characteristics			Prefix	Device	Suffix
		AH Analog Hybrid	A	Improved Electrical Specs	LM	101	A F	
		AM Analog Monolithic	C	Reduced Temperature Range	Characteristics			
		CD CMOS	Package			Package		
DH Digital Hybrid		D	Glass/Metal DIP					
DM Digital Monolithic		F	Flat Pack (0.25" wide)					
DS Digital Special		G	TO-8 (12 lead) Metal Can					
LF Linear FET Monolithic		H	TO-5 (multi-lead) Metal Can					
LH Linear Hybrid		J	Glass/Glass					
LM Linear Monolithic		K	TO13 Power Pack					
LX Transducer		M	Wide Trak Power Pack					
MH MOS Hybrid		N	Molded DIP					
MM MOS Monolithic		P	TO-202 Plastic Power Pack					
Linear Devices		R	Low Temperature Ceramic Pack					
With proprietary linear circuits, a 1-2-3 numbering system is employed. The 1 denotes a Military temperature range device (-55°C to 125°C), the 2 denotes an Industrial device (-25°C to 85°C), and the 3 denotes a Commercial device (0°C to 70°C). i.e. LM101/LM201/LM301. Exceptions to this are the LM1800 Series; some hybrid circuits which employ a "C" suffix; and second-source products which follow the original manufacturers numbering system.		S	14 Lead Power Pack SGS Power Pack					
		T	TO-220 Plastic Power Pack					
		W	Flat Pack (0.275" wide)					
		Z	TO-92					
DEVICE NUMBER (for Digital Devices): CDXXX-CMOS — C suffix — 40°C to 85°C, M suffix — 55°C to 125°C. DM54XX — All numbers beginning with 5 denote — 55°C to 125°C temperature operation. DM74XX — If the "74" is indicated, the operating temperature is 0°C to 70°C. DM7XXX — All other numbers beginning with 7 (besides the "74" shown above) are NSC proprietary products and a 7 here indicates — 55°C to 125°C. DM8XXX — All numbers beginning with 8 denote 0°C to 70°C temperature operation.								

IC UPDATE MASTER

		Part Number		
Manufacturer	Prefix		Suffix	Example
NEC	μ P Micropackage	Package	Prefix	Suffix
	Family	C Plastic	μ P F	xxxxx P S
	A Discrete	D Ceramic	Family	
	B Digital Bipolar		Package	
	C Linear		Modification	
D Digital CMOS				
NITRON	Description		Prefix	Device
	NC Packaged IC's (non-memory)		NC	7010
	NCM Packaged Memory IC's		Description	
NIT Memory Modules				
NORTEC	NE Nortec Electronics	Electrical Selections	Prefix	Device
	NE 6003BZD	11	NE	6003
	NE 1103-1460	BZ } 146 } etc. }	Electrical Selections	11 D
		Package	Package	
		D Ceramic DIP		
	F Flatpack			
	H Metal Can			
	J CerDIP			
	N Molded DIP			
	P 8-Pin DIP			
	Y Dice			
PANASONIC	Description		Prefix	Device
	AN Analog		DN	830
	DN Digital Bipolar			
	J Development Type			
	MN MOS			
PLESSEY	Description	Characteristics	Prefix	Device
	ML MOS Linear (w/gate protection)	A-D Electrical/Temperature Variations	SL	421
	MP MOS Digital	Package	Elec/Temp	
	MT MOS Linear (without gate protection)	E DIP	Package	
	NOM MNOS Memory Elements and Arrays	F Flatpack		
SAA, SBA Alternate Sourced Consumer Devices	P Power			
SL Bipolar Linear	Q Quad In-Line			
SP Bipolar Digital	S Stud			
	T T0-5 and T0-18			
PRECISION MONOLITHICS	Description	Package (Last Alphabetical Character)	Prefix	Device
	SSS Second Source Devices	G 6-Pin T0-18	DAC	01
	DAC Digital to Analog Converter	H 6-Pin T0-78	Package	
	AD Analog to Digital Converter	J 8-Pin T0-99		
	MAT Matched Transistors	K 10-Pin T0-100		
	OP Operational Amplifier	L 10-Pin Flatpack		
	CMP Voltage Comparator	M 14-Pin Flatpack		
		N 24-Pin Flatpack		
		P 14-Pin Metal DIP		
		Q 16-Pin Metal DIP		
		R 22-Pin Hermetic DIP — .400" Centers		
		S 14-Pin Plastic DIP		
		T 16-Pin Plastic DIP		
		U 18-Pin Hermetic DIP		
		V 24-Pin Hermetic DIP — .600" Centers		
		W 40-Pin Hermetic DIP — .600" Centers		
		X 40-Pin Flatpack		
		Y 14-Pin CerDIP		
		Z 16-Pin CerDIP		

PART NUMBER GUIDE

Manufacturer	Part Number		Example			
	Prefix	Suffix	Prefix	Device	Suffix	
RAYTHEON SEMICONDUCTOR	Temperature					
	LH1, LM1	-55°C to 125°C		54	153	DD
	LH2, LM2	-25°C to 85°C		RC	4136	DP
	LH3, LM3	0°C to 70°C		LM	118	H
	RC	0°C to 70°C		Temperature		
	RM	-55°C to 125°C		Package		
	RV	-40°C to 85°C				
	54	-55°C to 125°C				
	74	0°C to 70°C				
	Package					
	Most Devices					
		BL	Beam Lead Chip			
		BLB	BL Chip, Military Visual			
		CG	Gold-Backed Chip			
		CH	Standard Chip			
	D	14-Pin Glass/Metal DIP (Linears Only)				
	DC	14-Pin Ceramic DIP				
	DD	16-Pin Ceramic DIP				
	DN	8-Pin Plastic DIP				
	DP	14-Pin Plastic DIP				
	G	10-Pin Flatpack, 1/4" x 1/4" (Linears Only)				
	J	14-Pin Glass/Metal Flatpack				
	L	16-Pin Glass/Metal Flatpack				
	LK	TO-3 Power Pack				
	M	16-Pin Glass/Metal DIP				
	MP	16-Pin Plastic DIP				
	N	24-Pin Glass/Metal Flatpack				
	Q	10-Pin Flatpack, 1/4" x 1/4" (Linears Only)				
	R	24-Pin Ceramic DIP				
	T	3, 8, 10 or 12-Pin TO-5 Can				
	TK	9-Pin TO-66 Power Pack				
	Y	TO-220 Plastic Power Pack				
LH, LM Series						
	F	Flat Pack (1/4" Wide)				
	H	3, 8 or 10-Pin TO-5 Can				
	K	TO-3 Power Pack				
	N	Plastic DIP				

Manufacturer	Description	Version	Example			
			Prefix	Device	Suffix	
RCA	CA	Linear IC's	CD	4070	BD	
	CD	Digital IC's	Version			
	MW	MOS IC's	Package			
			A	Modified Version, Unilaterally Interchangeable with Prototype		
			B	Modified Version, Unilaterally Interchangeable with A Version, and with Prototype		
			C	Modified Version, Unilaterally Interchangeable with B, A, and Prototype Versions		
	Package					
		D	White Ceramic DIP			
		E	Plastic DIP			
		F	Ceramic DIP, frit seal			
		G	Hermetic Chip in Plastic Package			
		H	Chip			
		K	Ceramic Flat Package			
		L	Beam-Lead Device			
		Q	Quad-In-Line Plastic Package			
	S	TO-5 Package with DIL-CAN				
	T	TO-5 Package				
	X	Ceramic DIP, frit seal				

Manufacturer	Code	Example		
		Prefix	Device	Suffix
RETICON	RA	No. of columns and lines		
	RL	No. of elements		
	SAD	No. of storage elements		
	SAM	No. of storage elements		
	SAP	No. of storage elements		
	TAD	No. of Taps		
		RA	50x50	A
		RL	1024	C
		TAD	12	
		Code		
	Revision			

Manufacturer	Prefixes assigned by the European Association "PRO ELECTRON"	Example	
		Prefix	Device
SGS-ATES SEMICONDUCTOR	H	TDA	1200
	HBF	CMOS	
	L	Linear	
	M	MOS	
	TAA	Linear	
	TBA	Linear	
	TCA	Linear	
	TDA	Linear	

IC UPDATE MASTER

Manufacturer		Prefix	Part Number	Suffix	Example		
SIGNETICS	Temperature Range		Package		Prefix Device Suffix		
	N 0°C to 70°C (N8 Series 0°C to 75°C)		A 14-Pin Plastic DIP		NE 555 T		
	S -55°C to 125°C		B 16-Pin Plastic DIP		Temperature		
			DA TO-3 Solid Header, Can		Package		
			DB TO-5 Solid Header, Can				
			F 14- 16- 24-Pin Ceramic DIP				
			I 14- 28- 40-Pin Ceramic DIP				
			K 10-Lead, TO-5 Header, Short Can				
			L 10-Lead, TO-5 Header, Long Can				
			N 24-Pin Plastic DIP				
			Q 10- 14- 16- 24-Pin Ceramic Flatpack				
			T 8-Lead, TO-5 Header, Can				
			V 8-Pin Plastic DIP				
		W 10- 14- 16-Pin Ceramic Flatpack					
		X 18- 22-Pin Plastic DIP					
SILICONIX	Description	Temperature	A -55°C to 125°C	Prefix	Device	Suffix	
	D Driver for FET Switch	B -20°C to 85°C	B -20°C to 85°C	DG	200	BA-X	
	DG Driver with FET Switches	C 0°C to 70°C	C 0°C to 70°C	Temperature			
	DGM Driver with FET Switches (Monolithic Version of Hybrid Device)	Package	A Metal Can	Package			
	G Multi-Channel FET Switches	F Flatpack	F Flatpack	MIL Process Option			
	H High Voltage (28 v) Logic	J Plastic DIP	J Plastic DIP				
	L Linear IC	L Flatpack	L Flatpack				
	LD A/D Converter	P Hermetic DIP	P Hermetic DIP				
	LH Hybrid Linear IC (2nd Source)	R Hermetic DIP	R Hermetic DIP				
	LM Linear IC (2nd Source)	MIL Process Option					
	SI 2nd Source Part	1 MIL-883, Class A					
		2 MIL-883, Class B					
		3 MIL-883, Class C					
	4 In-House Screening Plus 168 Hr. Burn-In						
SMC MICROSYSTEMS	Family	Package		Prefix	Device	Suffix	
	CG Character Generator	P Plastic		COM	2502	P	
	COM Communications	C Ceramic		Family			
	KR Keyboard Encoding	Temperature		Package			
		T -25°C to 85°C		Temperature Range			
	(Blank) 0°C to 70°C						
	An H in the Suffix Indicates High Speed						
SOLID STATE SCIENTIFIC	Reliability	A MIL 883-A	Process	A AL Gate Bulk	Prefix	Device	Suffix
	B MIL 883-B	B High Voltage AL Gate	B High Voltage AL Gate	SCL	4000	AE +	
	C MIL 883-C	S Silicon on Sapphire	S Silicon on Sapphire	Reliability			
	S Standard	Package	C Ceramic DIP	Process			
	Other Letters	CM CMOS	D Ceramic DIP	Package			
	C Complementary	L Logic	E Epoxy DIP	Special Screening			
	L Logic	M Memory	H Chip				
	M Memory	F Flat Pack	F Flat Pack				
	T TO5	T TO5					
SOLITRON	CM CMOS	Package Style, Temperature Range		Prefix	Device	Suffix	
		AD Ceramic DIP, -55°C to 125°C		CM	4000	AD	
		AE Epoxy Encapsulated DIP, -40°C to 85°C		Package/Temperature			
	AF CerDIP, -55°C to 125°C						
SPRAGUE ELECTRIC	Family	C CMOS	Package		Prefix	Device	Suffix
	D Display Drivers	D Display Drivers	A Plastic DIP	ULN	2111	A	
	L Linear Circuits	L Linear Circuits	C Chip	Family			
	Temperature		D TO-99	Temperature			
	N Limited Temperature Range, -25°C to 70°C		E 8-Pin Plastic DIP with pins 1, 4, 5, & 8 only	Package			
	S Extended Temperature Range		F TO-86 or 30 Lead Flat Package				
			G TO-91				
			H 14-Pin Hermetic DIP				
			J TO-87				
			K TO-100				
			L TO-100				
			M 8-Pin Plastic DIP				
			N 14-Pin Plastic Quad-In-Line				
		P Batwing DIP					
		Q Batwing Quad-In-Line					
		R 8-Lead DIP with Unformed Leads					
		S 4-Pin SIP					
		W TO-100 with Miniature Tube Base Adapter					
B. UH Series		Package	C Hermetic Flatpack	Prefix	Device		
		D Hermetic DIP	D Hermetic DIP	UHP	400		
		P Plastic DIP	P Plastic DIP	Package			

PART NUMBER GUIDE

STEWART-WARNER	SW Stewart-Warner	Series DTL 7XX to 93X	Prefix SW	Device 7495	Suffix N
		Package 2M Commercial (0°C to 70°C) Plastic DIP 2P Commercial (0°C to 70°C) Ceramic DIP 1P Military (-55°C to 125°C) Ceramic DIP 1F Military (-55°C to 125°C) Ceramic Flat Pack	Series	Package/Temperature	
		Series DTL 18XX to 19XX	Package M Plastic P Ceramic F Flat Pack		
		Series TTL 74XX to 9XXX	Package N, PC Plastic J, DC Ceramic		
		Series CMOS 4XXX	Package AE Plastic/Epoxy B (-40°C to 85°C)		

TELEDYNE SEMICONDUCTOR	Temperature/Electrical	Device	Suffix
	A -55°C to 125°C, Selected Electrical Performance (HiNIL -30°C to 70°C)	709	BE
	B -55°C to 125°C, Premium Electrical Performance	Temperature/Electrical	
	C 0°C to 70°C, Industrial Electrical Performance (HiNIL -30°C to 85°C)	Package	
	M -55°C to 125°C		
Package E Metal Can H Flat Pack J Plastic DIP, 14- 16-Pin L CerDIP, 14- 16-Pin N Ceramic DIP, 14- 16-Pin P Plastic Mini DIP, 8 Lead Y Dice			

For alternate source devices, the original manufacturer's part number and marking system is used.

TEXAS INSTRUMENTS	Description	Package	Prefix	Device	Suffix
	RSN Radiation Hardened Circuit SBP Bipolar Processor SN Standard Prefix SNM High Reliability, Level I SNA High Reliability, Level II SNC High Reliability, Level III SNH High Reliability, Level IV TMS MOS	FA Flat Package J Ceramic Flat Package JA DIP JB DIP JP DIP L Metal Can LA Metal Can N Plastic DIP ND Plastic DIP with Tab P Plastic DIP RA Flat Package SB Flat Package T Metal Flat Package W Ceramic Flat Package	A. SN 74	S188	J
	Temperature (Most Devices) 52 Series -55°C to 125°C 54 Series -55°C to 125°C 55 Series -55°C to 125°C 62 Series -25°C to 85°C 72 Series 0°C to 70°C 74 Series 0°C to 70°C 75 Series 0°C to 70°C TF Series -40°C to 85°C TP Series -55°C to 125°C TMS C Series -25°C to 85°C TMS L Series 0°C to 70°C TMS R Series -55°C to 85°C		Description	Temperature Range	Package
			B. Prefix	Device	Suffix
			TMS	4030	JL

TOSHIBA	Description	Package	Prefix	Device	Suffix
	TA Bipolar Linear TC CMOS TD Bipolar Digital TM MOS	P Plastic M Metal A Improved Type	TA	7173	AP

WESTERN DIGITAL	Package	Prefix	Device	Suffix
	A 40 Lead DIP, Ceramic B 40 Lead DIP, Plastic C 24 Lead DIP, Ceramic D 24 Lead DIP, Plastic E 28 Lead DIP, Ceramic F 28 Lead DIP, Plastic G 22 Lead DIP, Ceramic H 22 Lead DIP, Plastic	TR1602	A	01
		Package		
		Special Parameter		

ABBREVIATIONS OF COMPANY NAMES

AD	Analog Devices
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
AMS	Advanced Memory Systems
Analogic	Analogic Corp.
Beckman	Beckman Instruments, Helipot Division
Burr-Brown	Burr-Brown Research
Cermetek	Cermetek
CMA	Consumer Microcircuits of America
Collins	Collins Radio
Datel	Datel Systems
DDC	ILC Data Devices Corp.
EA	Electronic Arrays
EMM/Semi	EMM Semi, Div. of Electronic Memories & Magnetics
Exar	Exar Integrated Systems
Fairchild	Fairchild Semiconductor
Ferranti	Ferranti Electric
GI	General Instrument
Harris	Harris Semiconductor
Hitachi	Hitachi America, Ltd.
Hughes	Hughes Aircraft Co., MOS Division
Hybrid Sys.	Hybrid Systems
IMI	International Microcircuits, Inc.
Intech	Intech
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
IPI	Integrated Photomatrix, Inc.
ITT	ITT Semiconductors
Lithic Sys.	Lithic Systems
Litronix	Litronix
LSI Comp.	LSI Computer Systems
Micro Net	Micro Networks
Micropac	Micropac Industries
Micro Power	Micro Power Systems
Mitsubishi	Mitsubishi International
MMI	Monolithic Memories, Inc.
MOS	MOS Technology
Mostek	Mostek
Motorola	Motorola Semiconductor
National	National Semiconductor
NCR	National Cash Register, Microelectronics Div.
NEC	NEC Microcomputers
Nippon	Nippon Electric Co.
Nitron	Nitron
Nortec	Nortec Electronics
NPC	Nucleonic Products Co.
OKI	OKI Electronics of America, Inc.
Panasonic	Panasonic, Matsushita Electric Corp.
Plessey	Plessey Semiconductors
PMC	Power Monolithics Co.
PMI	Precision Monolithics, Inc.
Ragen	Ragen Semiconductor
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
Reticon	Reticon
Rockwell	Rockwell International, Microelectronic Div.
Sanken	Sanken Electric
SGS	SGS-ATES Semiconductor
Signetics	Signetics
Silicon G	Silicon General
Siliconix	Siliconix
SMC	SMC Microsystems Corp.
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSS	Solid State Scientific
SW	Stewart-Warner Microcircuits
Synertek	Synertek
Teledyne C	Teledyne Crystallonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
TI	Texas Instruments
TMX	TMX, Inc.
Toshiba	Toshiba
TRW	TRW
Transitron	Transitron Electronics
Western	Western Digital

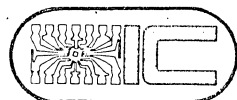
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APPLICATION NOTE DIRECTORY

The Application Note Directory is a comprehensive guide to the many IC application notes available. It lists the devices covered, describes each note, and tells who publishes each one.

how to use the application note directory

The application notes in this directory can be located by function, device number, or manufacturer.

1. To find out what is published by function, locate the closest topics in the index below, turn to the pages indicated, and scan through the listings.

2. To find all the application notes covering a given device, look up the device in the Part Number Index at the front of this book. The page references to pages 67 through 120 lead to application notes.

3. To find out what application notes are available from a particular manufacturer, look up the manufacturer in the table at the end of this section. The table gives you the titles and the page locations for each manufacturer's application notes in this directory.

The application note descriptions are organized under the headings: Digital, Linear, Memory and Microprocessor. Beneath those headings are functional and applications categories arranged alphabetically. Within each category the notes are arranged in alphabetical sequence by manufacturer. The mixing of functions and applications is necessary, since application notes do not lend themselves to classification entirely by function or entirely by application. When an application note

fits under several categories, it is listed in one and cross referenced by the others. This may mean that you have to spend five minutes checking a number of categories to be sure you've found everything you want, but finding suitable information can save you considerable design time.

If an application note covers specific devices or it shows in some detail how certain devices are used, these device numbers are listed in parentheses just below the title. If any of these device numbers are in bold face type, data on them is presented in The Master Selection Guide Data Sections.

The application note descriptions are as short as possible. They are designed to save you time in reading while giving an overall sense of the contents. The length of each note is indicated in parentheses on the last line; if the note is bound into a book, the last line will show that it is part of a handbook, databook, catalog, etc.

Once you have determined which application notes you need, contact the manufacturer's sales office or write to the manufacturer. Be sure to give both the title and the application note number. Addresses and phone numbers are listed in the Manufacturers and Distributors Directory.

APPLICATION NOTE SUBJECTS

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DIGITAL

Arithmetic

- 1 **"A Successive Approximation Register"**
(AM2502, AM2503, AM2504, AM25L02, AM25L03, AM25L04)
Operation, logic, coding of these 8 and 12 bit TTL devices. Describes applications in systems performing recursive arithmetic operations; as ring counters; serial-to-parallel converters.
Advanced Micro Devices Data Book, Catalog (11 pg.)
- 2 **"The Am2506 - A Latching ALU"**
(AM2506)
Combines four-bit arithmetic logic unit and four-bit latch. Describes application in high-speed multiple word adder, multiple master-slave registers, 16-word arithmetic register, multiplication at 16 MHz rate.
Advanced Micro Devices Data Book, Catalog (4 pg.)
- 3 **"TTL MSI Arithmetic Logic Units"**
(AM2506, 9340, 9341, 9342, SN54181, SN54182, SN74181, SN74182)
Functional descriptions, logic diagrams of 9340, 9341, 2506 parallel four-bit units incorporating 9342 look ahead carry circuit. Reviews adder operation and binary arithmetic. Discusses ALUs.
Advanced Micro Devices Data Book, Catalog (20 pg.)
- 4 **"The Am25S05, Am2505 and Am25L05 Schottky, Standard and Low Power TTL 2's Complement Digital Multipliers"**
(AM2505, AM25L05, AM25S05)
Discusses multiplication, two's complement notation, Booth's algorithm, iterative arrays, time-sequenced multipliers, integer and fractional multiplication, round-off, truncation and one's complement multiplication. Application to digital filters, square rooting and division.
Advanced Micro Devices Data Book (24 pg.)
- 5 **"Am25S10 Four-Bit Shifter"**
(AM25S10)
Provides functional description and discusses logic equivalents. Applications: up-shift, down and around end shifts, scaling and fixed multiplication.
Advanced Micro Devices Data Book (10 pg.)
- 6 **"MNOS Digital Differential Analyzer"**
(CRC1502, CRC1503, CRC1504, CRC9503, CRC9504)
Describes theory of operation of a DDA integrator for the real time solution of differential equations. Covers use of 3 LSI devices including mapping, scaling, initializing, and coding to simulate a given set of algebraic or differential equations.
Collins Radio Application Notes (7 pg.)
- 7 **"Applications of the TTL/MSI 93S43 4-Bit by 2-Bit Two's Complement Multiplier"**
(93S43)
How to implement a combinatorial multiplication array of any size for two's complement numbers. How to multiply in other number representations. Speed/hardware tradeoffs, normalization of floating point numbers after multiplying, rounding or truncation of double length products.
Fairchild Application, Note 329 (15 pg.)

Arithmetic (cont)

- 8 **"High-Speed Addition Using Lookahead Carry Techniques"**
Describes use of TTL and ECL to perform lookahead carry addition. Explains operation of adders in detail and gives examples of lookahead carry adders using MC5400/7400, MC3000/3100, and MC1000/1200 series circuits.
Motorola AN-488 (11 pg.)
- 9 **"High Speed Binary Multiplication using the MC10181"**
See listing under High Speed Logic
(Motorola)
- 10 **"MECL 10,000 Arithmetic Elements MC10179, MC10180, MC10181"**
See listing under High Speed Logic (Motorola)
- 11 **"NBCD Sign and Magnitude Adder/Subtractor"**
(MC14560, MC14561)
Describes CMOS parallel adder/subtractors for both signed and unsigned natural binary coded decimal (NBCD) numbers.
Motorola AN-738 (7 pg.)
- 12 **"Applications of the DM7200/DM8200 Digital Comparator"**
(DM7200, DM8200)
Describes use in word comparison, associative memory, bit exclusion, modulo N divider and servo system applications.
National AN-12 (6 pg.)
- 13 **"High-Speed TTL Adders"**
(DM7283, DM8283)
Describes 16-bit parallel adders, using the DM7283/DM8283, and connections for ripple-carry parallel addition. Also describes BCD adder techniques implemented with these devices. Shows how devices can be used to improve the performance of MOS storage systems.
National Semiconductor AN-35 (6 pg.)
- 14 **"Arithmetic Arrays Using Standard COS/MOS Building Blocks"**
(CD4001A, CD4008A, CD4011A, CD4013A, CD4019A)
Describes design of a 32-bit full adder/arithmetic logic system. Discusses four-bit full adder, quad AND-OR select gate, dual D-type flip-flop, input NAND gates, input NOR gates, and arithmetic register.
RCA SSD-203 COS/MOS Digital Databook, ICAN-6600 (6 pg.)
- 15 **"COS/MOS Rate Multipliers-Versatile Circuits for Synthesizing Digital Functions"**
(CD4089, CD4527)
Describes operation of a rate multiplier, and the effects of cascading. Covers addition, subtraction, multiplication, division, square and higher order roots, frequency ratios, and integration. Also discusses symmetric operation.
RCA SSD-203 COS/MOS Databook, ICAN-6739 (12 pg.)

DIGITAL

Arithmetic (cont)	CMOS (cont)
<p>1 "BCD Arithmetic" (N82S82, N82S83, S82S82, S82S83, N7483) Discussion of BCD and serial or parallel arithmetic: application of the 82S82/83 as a bit serial BCD adder and as a bit parallel, digit serial adder. Signetics Applications Handbook (4 pg.)</p>	<p>10 "Minimizing Gate Oxide Failures Due to Handling" Describes oxide failure mechanisms, evaluates input protection techniques, and recommends handling procedures to avoid failure. Harris Applications Report 208 (3 pg.)</p>
<p>2 "BCD Arithmetic Unit" (N82S82, S82S82) Gives description and logic diagram of 82S82. Applications - 2 decade adder/subtractor; high speed BCD adder/subtractor using fast carry, sign and magnitude generation. Signetics Applications Handbook (4 pg.)</p>	<p>11 "Using Junction Isolated CMOS" Covers problems and application rules related to forward biasing CMOS inputs and outputs. Harris Application Note 210 (4 pg.)</p>
<p>3 "BCD Adder" (N82S83, S82S83) Gives logic diagram of 82S83. Covers applications as four decade BCD adder and bit parallel-word serial BCD multiplier. Signetics Applications Handbook (3 pg.)</p>	<p>12 "MasterMos, a custom CMOS System" (MasterMos) Describes the construction of these devices which are customized by changing the metalization pattern. International Microcircuits (2 pg.)</p>
<p>4 "Gated Full Adder" (N8268, N8270, S8268, S8270) Provides logic diagram and discusses application of 8268 as n-bit parallel add, n-bit binary subtract, serial binary add/subtract, and serial BCD add/subtract devices. Signetics Applications Handbook (5 pg.)</p>	<p>13 "A New CMOS Analog Gate Technology" See listing under (Linear) Switches. (Intersil)</p>
<p>5 "Arithmetic Logic Element, Fast Carry Extender" (N8260, N8261, S8260, S8261) Describes lookahead carry principle and implementation of various adder systems using 8260 and 8261. Signetics Applications Handbook (9 pg.)</p>	<p>14 "NBCD Sign and Magnitude Adder/Subtractor" See listing under Arithmetic (Motorola)</p>
<p>6 "Converting To and From Binary Using the SN74184 and SN74185A" (SN74184, SN74185A, SN74283, SN74284, SN74285) Compares conventional shift and add technique to conversion from binary to BCD using the 74185A. Tells how to interconnect these converter packages for 6-bit through 20-bit binary inputs and 4, 5 or 6 decade BCD inputs. Describes conversion of fractions using the 74283, 74284 and 74285. Texas Instruments Application Report CA-171 (19 pg.)</p>	<p>15 "A 3^{1/2} Digit DVM Using an Integrated Circuit Dual Ramp System" See listing under Linear-Instrumentation (Motorola)</p>
<p>7 "Fast Multipliers Using TTL Read Only Memories" See listing under (Memory) ROMs. (Texas Instruments)</p>	<p>16 "Noise Immunity Comparison of CMOS Versus Popular Bipolar Logic Families" Compares the noise immunities of TTL, DTL, HTL, and CMOS logic families. Discusses common noise sources, precautions against noise, noise specification, and standard noise tests. Motorola AN-707 (8 pg.)</p>
<p>8 "SN7497 Binary Rate Multiplier" (SN5497, SN7497) Covers principles and internal operation of the binary rate multiplier (BRM); shows add, subtract, multiply, divide and square root operations with a minimum of control logic. Discusses the use of the BRM to solve differential equations and to generate functions. Texas Instruments Application Report CA-160 (13 pg.)</p>	<p>17 "Introduction To CMOS Integrated Circuits With Three-State Outputs" (MC14500 Series) Describes a wide variety of CMOS ICs incorporating transmission gates with standard logic. Gives design rules. Covers applications in analog switching and multiplexing, digital multiplexing, and data bussing. Motorola AN-715 (19 pg.)</p>
<p>CMOS</p>	<p>18 "Scanning Logic for RF Scanner-Receiver Using CMOS Integrated Circuits" Describes rf scanner-receiver control functions using standard CMOS devices. Covers crystal switching and priority channel monitoring with mention of phase-locked loop designs. Motorola AN-753 (7 pg.)</p>
<p>9 "CMOS: Some Application Guidelines" Presents General Guidelines when using CMOS. Harris Application Note 209 (7 pg.)</p>	<p>19 "CMOS, the Ideal Logic Family" (MM54C/74C Series) Describes characteristics of CMOS circuits. Discusses system considerations, such as unused inputs, data bussing, paralleling circuits for extra drive, and interface to other logic families. National AN-77 (8 pg.)</p>

DIGITAL

CMOS (cont)

- 1 **"CMOS Linear Applications"**
(MM74C00, MM74C02, MM74C04)
Describes use of CMOS devices biased to operate at the midpoint of the transfer characteristics.
National AN-88 (3 pg.)
- 2 **"CMOS Oscillators"**
Describes square wave oscillators that can be built with CMOS logic elements.
National AN-118 (4 pg.)
- 3 **"CMOS Schmitt Trigger - A Uniquely Versatile Design Component"**
(MM54C14, MM54C914, MM74C14, MM74C914)
Describes CMOS Schmitt trigger ICs with emphasis on the advantages over TTL versions, including high input impedance, wide threshold range, high noise immunity and low power consumption.
National AN-140 (6 pg.)
- 4 **"Using the CMOS Dual Monostable Multivibrator"**
(MM54C221, MM74C221)
Gives MM54C/MM74C221 circuit characteristics and operating suggestions. Shows use in a retriggerable one-shot, frequency magnitude comparator, Linear VCO and an analog multiplier/divider.
National AN-138 (6 pg.)
- 5 **"MM54C/74C Voltage Translation/Buffering"**
See listing under Interface (National)
- 6 **"54C/74C Family Characteristics"**
(MM54C/74C Series)
Discusses output, noise and temperature characteristics, power consumption, and propagation delay for the 54C/74C logic family.
National AN-90 (6 pg.)
- 7 **"OKI's CMOS and it's Applications"**
Describes device construction, general characteristics, covers in general terms counter, camera and clock applications.
OKI (16 pg.)
- 8 **"Accelerated Testing of COS/MOS Integrated Circuits"**
(CD4000 Series)
Describes accelerated testing through the use of increased stress, constant and step stress methods, and application to CMOS.
RCA (3 pg.)
- 9 **"Gate-Oxide Protection Circuit In RCA COS/MOS Digital Integrated Circuits"**
(CD4000 Series)
Gives description and schematics for the protection circuits.
RCA SSD-203 COS/MOS Digital Databook, ICAN-6218 (2 pg.)
- 10 **"Interfacing COS/MOS with Other Logic Families"**
(CD4000A Series)
Describes conditions governing interface of CMOS 4000A series with other logic families.
RCA SSD-203, COS/MOS Digital Databook, ICAN-6602 (12 pg.)

CMOS (cont)

- 11 **"Battery-Powered Digital-Display Clock/Timer and Metering Applications Utilizing the RCA CD4026A and CD4033A Decade Counters-7 Segment Output Types"**
(CD4009A, CD4010A, CD4026A, CD4033A)
Describes the CD4026A/33A ICs and their use with 7-segment display units. Discusses interface packages and methods to help the designer optimize his system. Includes a discussion of battery-operated systems for digital clocks and watches.
RCA SSD-203, COS/MOS Digital Databook, ICAN-6733 (16 pg.)
- 12 **"Radiation Resistance of the COS/MOS CD4000A Series"**
(CD4000A Series)
Provides a graph plotting permanent radiation, resistance of CD4000A series. Discusses design considerations for increasing resistance.
RCA SSD-203 COS/MOS Digital Databook, ICAN-6224 (2 pg.)
- 13 **"Astable and Monostable Oscillators Using RCA COS/MOS Digital Integrated Circuits"**
Describes techniques to compensate for normal threshold variation of MOS devices in the design of stable multivibrator circuits for operation at frequencies up to 1MHz. Describes applications, including VCOs, voltage controlled pulse-width circuits, frequency multipliers, and modulator/demodulators (envelope detectors).
RCA Digital Databook SSD-203 COS/MOS Application Note ICAN-6267 (8 pg.)
- 14 **"COS/MOS MSI Counter and Register Design and Applications"**
(CD4006A, CD4014A, CD4015A, CD4017A, CD4018A, CD4020A, CD4021A, CD4022A, CD4024A)
Includes logic and schematic diagrams for these counters and shift registers. Outlines circuit designs, discusses device-design tradeoffs and summarizes performance criteria.
RCA SSD-203 COS/MOS Digital Databook ICAN-6166 (16 pg.)
- 15 **"COS/MOS Interfacing Simplified"**
See listing under Interface (RCA)
- 16 **"COS/MOS Rate Multipliers-Versatile Circuits for Synthesizing Digital Functions"**
See listing under Arithmetic (RCA)
- 17 **"Noise Immunity of COS/MOS Integrated-Circuit Logic Gates"**
(CD4000A, CD4001A)
Evaluates noise immunity of the CD4000A/01A gates with respect to external noise, crosstalk, transmission-line reflections, power-line noise, and ground-line noise. Includes schematics and logic diagrams.
RCA SSD-203B COS/MOS Digital Databook, ICAN-6176 (8 pg.)

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CMOS (cont)	CMOS (cont)
<p>1 "Micropower Crystal-Controlled Oscillator Design Using RCA COS/MOS Inverters" (CD4007) Describes in depth the design of low power crystal controlled oscillators and the exact frequency of oscillation. RCA Application Note ICAN-6539 (8 pg.)</p>	<p>8 "Application of CD4016A Quad Bilateral Switch" See "Transmission and Multiplexing of Analog or Digital Signals Using the CD4016A Quad Bilateral Switch" Under Data Transmission. (RCA)</p>
<p>2 "A Typical Data-Gathering & Processing System Using CD4000A-Series COS/MOS Parts" (CD4000A Series) Describes data-gathering and processing system using CMOS circuits. Includes discussion of input signal conditioning and transmission, the digital processor unit, receiver, memory, arithmetic unit, display unit, output buffer, output transmitter, receiver, and control unit. RCA SSD-203 COS/MOS Digital Databook, ICAN-6210 (11 pg.)</p>	<p>9 "A COS/MOS PCM Telemetry and Remote Data Acquisition Design" (CD4000A Series) Describes data transmission formats and the following data acquisition sections: analog and digital multiplexers, A/D converters, transmission formatters and system programmers. RCA SSD-203 COS/MOS Digital Databook, ICAN-6289 (12 pg.)</p>
<p>3 "Power-Supply Considerations for COS/MOS Devices" (CD4000 Series) Includes discussion of quiescent device dissipation, switching characteristics, ac dissipation and ac performance characteristics, calculating system power, power supply regulation and filtering requirements. RCA SSD-203 COS/MOS Digital Databook, ICAN-6576 (6 pg.)</p>	<p>10 "Power Supplies for COS/MOS" (CD4000A Series) Discusses the factors involved in the selection of CMOS supply voltages including the system operating frequency, noise immunity and power dissipation. Examples of simple power supply circuits are also given. RCA SSD-203 COS/MOS Digital Databook, ICAN-6304 (5 pg.)</p>
<p>4 "Using the CD4047A In COS/MOS Timing Applications" (CD4047A) Compares this monostable/astable multivibrator with simpler types of oscillator circuits and discusses applications, including a noise discriminator, low-pass and band-pass filters, a frequency discriminator, and a pulse generator. RCA SSD-203 COS/MOS Digital Databook, ICAN-6230 (13 pg.)</p>	<p>11 "Applications of the RCA-CD4093B COS/MOS Schmitt Trigger" (CD4093A/B) Describes characteristics of the CD4093 quad 2-input Schmitt trigger. Covers applications in waveshaping (sinewave to squarewave, edge delay, edge detection), power-on reset, astable multivibrators and use as a Schmitt trigger for noise immunity. RCA Application Note ICAN-6346 (6 pg.)</p>
<p>5 "Handling and Operating Considerations for MOS Integrated Circuits" Discusses handling of unmounted chips and subassembly boards, working with automatic handling equipment, storing of p-c boards, operating voltage, connections to unused inputs, interfacing with other logic families, noise immunity, and device characteristics of CMOS ICs. RCA SSD-203 COS/MOS Digital Databook, ICAN-6000 (6 pg.)</p>	<p>12 "CMOS Expandable Gates" (SCL4402A, SCL4412A) Compares the transfer characteristics of ordinary CMOS gates to those gates using double buffered output. Includes performance characteristics and discusses expansion of SCL4412A and SCL4402A to 12-input NOR, 16-input OR, and other combinations. Solid State Scientific AN-102 (3 pg.)</p>
<p>6 "Design of Fixed and Programmable Counters Using the RCA 4018A COS/MOS Presettable Divide-by-"N" Counter" See listing under Counters. (RCA)</p> <p>7 "The RCA COS/MOS Phase Locked-Loop—A Versatile Building Block for Micro- Power Digital and Analog Applications" See listing under (Linear) Phase Locked Loops. (RCA)</p>	<p>13 "CMOS Wave Shaping and Level Detection" Describes methods to obtain modified transfer characteristics of double buffered NAND gates, by connecting inputs together, connecting extra inputs to V_{cc}, etc. Shows how to obtain variable amounts of hysteresis, and describes systems of level detection using trigger circuits. Solid State Scientific AN-109 (5 pg.)</p> <p>14 "Using Complementary MOS Circuits" (SCL4013A, SCL4046A, SCL4018A, SCL4026A, SCL4029A, SCL4404A) Reviews CMOS operation, cost, and reliability. Discusses application of the SCL4018A in a three decade rate multiplier; the SCL4029A in counting devices; the SCL4404A and SCL4031A in A/D converters; and SCL4016A in analog switching. Solid State Scientific AN-101 (6 pg.)</p> <p>15 "Applications of CMOS Integrated Circuits In Communications Equipment" (SCL4000 Series) Uses of SCL4000 Series circuits as frequency synthesizers, digital frequency displays, frequency scanners, and squelch circuits. Solid State Scientific AN-108 (4 pg.)</p>

DIGITAL

CMOS (cont)

- 1 **"A Simplified Approach to Testing CMOS Inverters and Gates"**
Bench tests using a power supply and a V-O-M are described. They include continuity, input leakage, quiescent device current, output voltage, noise immunity, output drive current, and threshold voltage.
Solid State Scientific AN-107 (4 pg.)
- 2 **"Improved CMOS Gate Design"**
(SCL4000 Series)
Description of the output buffering of the SCL4000 Series
Solid State Scientific AN-105 (3 pg.)
- 3 **"Interfacing with CMOS"**
(SCL4000 Series)
Describes electrical characteristics of CMOS inputs and outputs. Discusses interfacing CMOS with CMOS, PMOS, NMOS, DTL/TTL, HTL, and ECL.
Solid State Scientific AN-104 (5 pg.)
- 4 **"CMOS Integrated Circuits in Automotive Applications"**
General discussion, also includes discussion of high current circuits, constant current or constant impedance circuit, digital time delay circuit, digital low-pass filter.
Solid State Scientific AN-103 (5 pg.)

Consumer

- 5 **"S2144 8-digit, 4-function Calculator"**
(S2144)
Describes calculator circuit with parts list and cost estimate.
American Microsystems AP74-3 (2 pg.)
- 6 **"S9411 8-digit, 5-function Calculator"**
(S9411)
Describes complete calculator circuit with parts list and cost estimate.
American Microsystems AP75-4A (2 pg.)
- 7 **"S9412 8-digit, Multi-function Calculator with Fluorescent Display"**
(S9412)
Describes complete calculator circuit with parts list and cost estimate.
American Microsystems AP74-6 (2 pg.)
- 8 **"S9412 8-digit, Multi-function Calculator with LED Display"**
(S9412)
Describes complete calculator circuit with parts list and cost estimate.
American Microsystems AP74-5 (2 pg.)
- 9 **"A Navigation Receiver That Uses A Digital Frequency Synthesizer"**
(μ A719)
Gives schematics for a navigation receiver. Discusses the digital frequency synthesizer, varactor tuned RF amplifier, AGC amplifier, mixer, IF amplifier, and detector portions.
Fairchild Application Note 178 (6 pg.)

Consumer (cont)

- 10 **"Industrial Clock/Timer Featuring Back-up Power Supply Operation"**
Describes the design and operation of a clock timer with digital readout suitable for industrial control applications. CMOS circuits are used for reduced power.
Motorola Application Note AN-718A
- 11 **"Calculator Learns to Keep Time"**
(MM5736)
Describes stopwatch and keyboard controlled interval timing functions using the MM5736 calculator chip.
National AN-119 (8 pg.)
- 12 **"Handheld Calculator Battery Systems"**
Describes the tradeoffs in battery performance for 6.5-9.5v calculators driven by 2, 3 and 4 cell as well as a 9v, batteries.
National AN-149 (pg.)
- 13 **"High Voltage Shift Registers Move Displays"**
See listing under (Memory) Shift Registers (National)
- 14 **"Timekeeping Advances Through COS/MOS Technology"**
Discusses basic oscillator design considerations, practical oscillator circuits, and some typical timing-circuit applications, including wristwatches, wall clocks, and auto clocks.
RCA SSD-203 COS/MOS Digital Datebook, ICAN-6086 (12 pg.)
- 15 **"CMOS Integrated Circuits in Automotive Applications"**
See listing under CMOS. (Solid State Scientific)

Converters

- 16 **"Binary D/A Converters Can Provide BCD-Coded Conversion"**
(MC1408, MC1508)
Describes the MC1508 D/A converter used as a 2 or 2 1/2 digit BCD converter. Describes application in a 2 1/2 digit digital voltmeter.
Motorola AN-713 (4 pg.)

Counters

- 17 **"Using the MK5009P MOS Counter Time-Base Circuit"**
(MK5009)
Describes the use of the MK5009 along with complete circuits for a digital frequency meter, pulse generator and digitally-programmable one-shot. Discusses operation of the units oscillator circuit.
Mostek AN-104 (4 pg.)
- 18 **"Application Information Using Mostek's Six-Decade Counter/Display Totalizer"**
(MK50395)
Covers circuit operation and input/output requirements. Describes use in a batch control system, a position measurement system and greater than-less than detection.
Mostek (8 pg.)

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Counters (cont)	Counters (cont)
<p>1 "Programmable Counters Using the MC10136 and MC10137 MECL Universal Counters" (MC10136, MC10137) Circuit operation and use in programmable counters with no external gating. Also use in high-frequency counters operating up to 110 MHz. Motorola AN-584 (4 pg.)</p>	<p>9 "Synchronous Up/Down Counters" (N8284, N8285, S8284, S8285) Provides logic diagrams and discusses operation of 8284/85. Applications: cascading counters, 1's complement generator, synchronous and 1-out-of-N decoding, magnitude and sign generator, frequency multiplier, and variable modulus counter. Signetics Applications Handbook (11 pg.)</p>
<p>2 "Battery-Powered 5-MHz Frequency Counter" Describes a battery operated 5 MHz counter built with CMOS for low power operation. Discusses methods to minimize power consumption. Motorola Application Note AN-717 (9 pg.)</p>	<p>10 "Asynchronous MSI Counters/Storage Element" (N8280, N8281, N8288, N8290, N8291, N8292, N8293, N82S90, N82S91) Gives logic diagrams for 8200 series ripple counters, signal processing input clock requirements, ac characteristics, and includes a discussion of cascading asynchronous counters. Signetics Applications Handbook (12 pg.)</p>
<p>3 "Five Digit Accumulator/Elapsed Time Indicator" (MC14534) Describes in detail the circuit for a CMOS 5 digit elapsed time indicator and a 99,999 count accumulator with a 1-999 prescaler. Motorola AN-743 (5 pg.)</p>	<p>11 "Using the SN74160 Family of Synchronous Counters" (SN74160, SN74161, SN74162, SN74163) Describes carry circuit operation, cascading and programming. Texas Instruments Application Report CA-174 (7 pg.)</p>
<p>4 "The Logical Design of Shift Counters" Presents two techniques to aid in designing shift-register counters. Gives results for "sequence tree" and "count multiplication" techniques for cycle lengths of 30 or less. Shows solutions for both "D" flip-flops and J-K flip-flops as the input elements of the shift register. Motorola AN-576 (8 pg.)</p>	<p>12 "ECL High Speed Counters" Discusses design considerations when constructing high speed counters using the TI ECL 2500 Series. Texas Instruments Application Report CA-147 (8 pg.)</p>
<p>5 "A 200 MHz Autoranging MECL-McMOS Frequency Counter" (MC10138, MC14518) Presents the principles of autoranging counters. Describes a counter using ECL for prescaling and the first two dividers. Covers the input buffer and ECL-CMOS translation. Motorola AN-742 (10 pg.)</p>	<p style="text-align: center;">Data Transmission</p>
<p>6 "An MSI 500 MHz Frequency Counter Using MECL and MTTL" See listing under High Speed Logic. (Motorola)</p>	<p>13 "A Typical Data-Gathering and Processing System using CD4000A-Series COS/MOS Parts" See listing under CMOS (RCA)</p>
<p>7 "Calculator Chip Makes A Counter" (MM5736, MM5739) Discusses use of the MM5736 calculator chip as a counter operating up to 120 MHz. National AN-112 (6 pg.)</p>	<p>14 "Line Drivers and Receivers" (AM2614, AM2615, 9614, 9615, 9620, 9621, DM7831, DM8831) Discusses single ended, differential, unbalanced differential digital communications systems and line matching methods. Describes the above circuits and their use in systems. Advanced Micro Devices Data Book, (12 pg.)</p>
<p>8 "Design of Fixed and Programmable Counters Using the RCA 4018A COS/MOS Presettable Divide-by-"N" Counter" (CD4018A) Describes the use of this device in single-decade and multi-decade fixed and programmable divide-by-"N" counters. System considerations, such as switch simplifications, components minimization, and speed are also discussed. RCA SSD-203 COS/MOS Digital Databook, ICAN-6498 (6 pg.)</p>	<p>15 "Using the Data Concentrator in Data Communications" (AY5-1016) Describes counter, decoding matrix, and multiplexer switch sections of the AY-5-1016 data concentrator. Describes commutator-decommutator and polling system applications plus use as a digitally programmable gain amplifier, and as a clock generator. General Instrument Microelectronics (11 pg.)</p>
	<p>16 "The AY-5-1011 Terminal Transmitter for Key-To-Tape Data Accumulation System and Other Applications" (AY5-1011) Describes features of this parallel-to-serial converter and discusses its use in key-to-tape systems. General Instrument Microelectronics (6 pg.)</p>

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Data Transmission (cont)

- 1 **"Using the UAR/T in Data Communications"**
(AY5-1013)
Describes this full duplex receiver/transmitter and discusses its application in computer, terminal and slow speed device interfacing. Also covers use in polling.
General Instrument Microelectronics (4 pg.)
- 2 **"High Speed Digital Communications"**
(HD245, HD246, HD545, HD546)
Describes the use of the HD-245 family in a current mode digital communication system (up to 2 Mbs over 1,000-ft-long line.)
Harris Application Note 205 (4 pg.)
- 3 **"Receiver/Transmitter Noise Immunity"**
(HD245, HD246, HD545, HD546)
Discusses HD-245 transmitter/receiver system noise: External magnetic and capacitive effects, crosstalk, and ground line noise. Includes a comparison with voltage mode and differential voltage switching type systems.
Harris Application Note 207 (4 pg.)
- 4 **"Error Detection and Correction Using Exclusive-OR Gates and Parity Trees"**
(MC1030, MC4008, MC4010, MC10107, MCM10146, MC10160)
Discusses the use of Exclusive-Or gates and the parity trees available in the RTL,TTL,DTL, and ECL families for simple parity and single-error Hamming parity detection/correction circuits.
Motorola AN-496A (9 pg.)
- 5 **"Line Driver And Receiver Considerations"**
(MC1488, MC1489, MC75107, MC75110, MC75113)
Briefly describes transmission line systems using line drivers and receivers. Covers differential and single-ended systems. Discusses noise and line considerations.
Motorola AN-708 (14 pg.)
- 6 **"Bussing with MECL 10,000 Integrated Circuits"**
(MC10111, MC10123)
Describes use of MECL 10,000 circuits in high speed data transmission systems with emphasis on transmission line construction and termination.
Motorola AN-726 (6 pg.)
- 7 **"Device Operation and System Implementation of the Asynchronous Communications Interface Adapter (MC6850)"**
(MC6850)
Provides information on ACIA transmitter and receiver operation, initialization, status register bits, use in a microcomputer based communications system, software requirements, and transmission subroutines.
Motorola AN-754 (11 pg.)
- 8 **"Low Speed Modem Fundamentals"**
(MC6860)
Describes interface circuitry and performance of the MC6860 low speed modem. Evaluation of the system performance in the presence of Gaussian noise is given, as well as a brief description of data couplers.
Motorola Application Note AN-731 (15 pg.)

Data Transmission (cont)

- 9 **"Low-Speed Modem System Design Using the MC6860"**
(MC6860)
Describes the MC6860 modem. Provides filter design tables and equations to develop a complete 100 series compatible system.
Motorola AN-747 (13 pg.)
- 10 **"Operational Aspects of Motorola's Data Terminal Transmitter and Receiver"**
(MC2257, MC2259, MC2260)
Describes in detail the input and output signals for the synchronous/asynchronous operation of these parallel to serial transmitters and the serial to parallel receiver.
Motorola Application Note AN-724 (24 pg.)
- 11 **"Transmission Line Characteristics"**
(DM7400, DS7820A, DS7830, DS75452)
Describes the characteristics of digital signals in transmission lines and the characteristics of the line that effect transmission quality. Also compares the performance of unbalanced and balanced circuits in digital systems.
National Interface Handbook, AN-108 (6 pg.)
- 12 **"Integrated Circuits for Digital Data Transmission"**
(DS7830, DS7820)
Describes the operation and use of the DS7830 line driver and DS7820 line receiver for transmission systems using twisted-pair lines. Includes a mathematical design analysis of this line receiver.
National Interface Handbook, AN-22 (16 pg.)
- 13 **"Data Bus and Differential Line Drivers and Receivers"**
(DS7820, DS7830, DS7831, DS7832, DS7833, DS7834, DS7835, DS7836, DS7837, DS7838, DS7839, DS1488, DS1489)
Includes schematics and describes the operation of these line drivers, receivers and transceivers.
National AN-83 (12 pg.)
- 14 **"Operational Aspects of Nitron's Data Terminal Transmitter and Receiver"**
(NC2257, NC2259, NC2260)
Discusses basic operation of the NC2257/2259/2260 IC's, and application in various types of communications systems.
Nitron Communications Note 1 (24 pg.)
- 15 **"Using High Speed Memory in Pulse Code Modulated Systems for Switching Applications"**
Discusses digital message switching and implementation with a conventional digital crossbar switch as well as with a switch using high speed memory and data multiplexing.
Nortec Applications Note No. 29 (4 pg.)

DIGITAL

Data Transmission (cont)	Data Transmission (cont)
<p>1 "Transmission and Multiplexing of Analog or Digital Signals Utilizing the CD4016A Quad Bilateral Switch" (CD4016A) Describes features and operation of this switch. Discusses applications, including switching, gating digital or analog signals, multiplexing and demultiplexing, D/A conversion, sample and hold, and squelch-control. RCA SSD-203 COS/MOS Digital Databook, ICAN-6601 (12 pg.)</p>	<p>11 "Data Transmission with SN55107 Series" (SN55107, SN55108, SN55109, SN55110, SN75107, SN75108, SN75109, SN75110, SN55107 Series) Demonstrates the use of these line drivers and receivers in solving two multiplexing problems: a party line addressing system; and data/clock signals in a bipolar line. Receiver and driver characteristics are provided. Texas Instruments Application Report CA-146 (8 pg.)</p>
<p>2 "A COS/MOS PCM Telemetry and Remote Data Acquisition Design" See listing under CMOS (RCA)</p>	<p>12 "Line Drivers and Receivers" (SN55107, SN55108, SN55109, SN55110, SN75107, SN75108, SN75109, SN75110) Circuit operation, circuit characteristics, and system applications are covered. Typical performance using different types and lengths of line are provided, as well as notes on selecting a transmission system. Also mentions use as a comparator, line repeater, window detector and temperature controller. Texas Instruments Application Report CA-130 (33 pg.)</p>
<p>3 "9-Bit Parity Generator and Checker" (N8262, S8262) Discusses examples of parity generator connections, even parity generator/checker as well as 27- and 12-bit word expansion using the 8262. Signetics Applications Handbook (3 pg.)</p>	<p>13 "Asynchronous Receiver/Transmitter" (TR1602) General description of asynchronous transmission and operation of TR1602, which is capable of full or half duplex operation. Describes application in distributed computer networks. Western Digital Application Report 1 (12 pg.)</p>
<p>4 "8T23 Line Driver/8T24 Line Receiver" (N8T23, N8T24) Provides device description, circuit characteristics and system considerations. Signetics Applications Handbook (4 pg.)</p>	<hr/> <p style="text-align: center;">Decoders</p> <hr/> <p>See also Interface.</p>
<p>5 "Quad Bus Driver/Receiver" (N8T26) Provides 8T26 description and covers applications in high speed memory buffer, differential data transmission, bus and MOS interface. Signetics Applications Handbook (5 pg.)</p>	<p>14 "Applications of the 9538 ECL/MSI High Speed Decoder" See listing under High Speed Logic (Fairchild) See also Interface.</p>
<p>6 "8T09 Quad Bus Driver/8T10 Quad D-Type Bus Flip-Flop" (N8T09, N8T10, S8T09, S8T10) Gives general description. Applications include bidirectional data bus, bus-organized minicomputer, and quad D-type bus flip-flop. Signetics Applications Handbook (6 pg.)</p>	<p>15 "MTTL Designers Note — The MC4006/MC4007 Decoders" (MC4006, MC4007) Discusses basic modes of operation and expansion capabilities of the MC4006 binary to one-of-eight decoder and the MC4007 dual binary to one-of-four decoder. Describes use in various memory systems. Motorola AN-465 (7 pg.)</p>
<p>7 "8T13 Line Driver/8T14 Line Receiver" (N8T13, N8T14, S8T13, S8T14) Gives circuit description and covers application to party-lines. Signetics Applications Handbook (6 pg.)</p>	<p>16 "Driving 7-Segment Gas Discharge Display Tubes With National Semiconductor Circuits" (DS7880, DS8880, DS8884A, DS8885, DS8887, DM8889) Describes decoder/driver circuits and applications, including interfacing 7-segment fully decoded MOS chips to digit displays and interfacing with numeric display tubes. National AN-84 (4 pg.)</p>
<p>8 "8T15 Line Driver/8T16 Line Receiver" (N8T15, N8T16) Covers circuit description, logic diagram, and applications including data transmission plus Schmitt trigger and sine-to-square wave converter. Tables summarize EIA Standard RS-232B, C, MILSTD-188 and CCITT v 24 requirements. Signetics Applications Handbook (6 pg.)</p>	<p>17 "Features and Applications of RCA-CD2500E-Series MSI BCD-to-7-Segment Decoder-Drivers" (CD2500, CD2501, CD2502, CD2503) Discusses logic levels, operating characteristics, display-lamp turn-on characteristics, static drive applications, time multiplex systems, and a fail-safe circuit. RCA SSD-202 Linear Application Note Databook, ICAN-6294 (11 pg.)</p>
<p>9 "ECL 10,000 Series 10124/10125" See listing under High Speed Logic (Signetics)</p>	
<p>10 "Quad Bus Receiver With Hysteresis Schmitt Trigger" See listing under Trigger Circuits. (Signetics)</p>	

DIGITAL

Decoders (cont)

- 1 **"Octal/Decade Decoders"**
(N8250, N8251, N8252, S8250, S8251, S8252)
Provides general description and covers applications of 8250/1/2, including arbitrary 4-bit decoding, code conversion, demultiplexing.
Signetics Applications Handbook (6 pg.)
- 2 **"8T04/5/6 Seven Segment Decoder/Driver"**
(N8T04, N8T05, N8T06, S8T04, S8T05, S8T06)
Covers circuit characteristics, and use with LED incandescent and electroluminescent displays. Discusses ripple blanking, intensity modulation, floating decimal point applications and multiplexing of displays.
Signetics Applications Handbook (10 pg.)
- 3 **"8T01 Nixie Decoder/Driver"**
(N8T01, S8T01)
One-out-of-ten decoder for multiplex operation of Nixie tubes and for driving relays or other high voltage interface circuitry. Provides discussion of one 8T01 operating a 16 Nixie tube subsystem.
Signetics Applications Handbook (5 pg.)

DTL/RTL

- 4 **"Using MDTL Logic Blocks"**
(DTL, RTL)
Discusses applications of MDTL components, such as gates and flip-flops, emphasizing positive logic OR, NOR, NAND, and Exclusive-OR functions. Cites use as timing circuits, gated oscillators, monostables, latches. Discusses interfacing with other logic families.
Motorola AN-519 (11 pg.)

Encoders

- 5 **"Using the AY-5-9100 in Telephone Equipment"**
(AY5-9100)
Describes use of this four phase dynamic logic circuit in mains powered dialers, line powered telephones, card readers, and in standard multifrequency tone dialer keyboards.
General Instrument Microelectronics (10 pg.)
- 6 **"Designing with the HD-0165 Keyboard Encoder"**
(HD0165)
The organization and truth table for this encoder are presented. The use of two circuits for encoding up to 256 keys, battery operation, examples of a tele-typewriter keyboard and universal keyboard encoders are described.
Harris Application Note 204 (8 pg.)
- 7 **"90 Keyboard Encoder Arrays"**
(MCS1009, MCS1020, MCS1021)
Describes the operation of these keyboard arrays and illustrates their application in keyboard encoding systems.
MOS Technology Application Note AN1 (22 pg.)
- 8 **"64 Key Keyboard Encoder Arrays"**
(MCS1007, MCS1010)
Describes operation and optional features of these keyboard encoders.
MOS Technology Application Note AN2 (21 pg.)

Encoders (cont)

- 9 **"Using the MM5704 Keyboard Interface In Keyboard Systems"**
(MM5704)
Discusses features, operation, and programming of this device. Discusses use with the MM5702 timing and control chip of the Microprogrammable Arithmetic Processing System, and in a standard ASCII encode system.
National AN-52 (11 pg.)
- 10 **"MOS Encoder Plus PROM Yield Quick Turnaround Systems"**
(MM5740)
Describes use of a binary coded keyboard encoder with a PROM to build prototype or small volume keyboard systems.
National AN-139 (4 pg.)
- 11 **"MOS Keyboard Encoding"**
(MM5740)
Describes circuit and operation of the MM5740 keyboard interface circuit, including input-output interface, the repeat function key, data strobe control and output enable. Discusses applications, including a polling system for localized keyboards and a complete ASR-33 keyboard.
National MOS Handbook AN-80 (11 pg.)

Filters

- 12 **"Digital Filters"**
Summarizes four filter types covering transfer response, difference equations, and implementation in 5 arrays: multiplier, input/output, timing control, storage, and a MOS to MOS buffer.
Discusses general operational features, such as input/output word sample rate and word size. Describes operation of a two pole bandpass filter implemented with these arrays.
Collins Radio Application Note (14 pg.)

Gates

- 13 **"MSI Gating Arrays"**
(N8233, N8234, N8235, N8266, N8267, S8233, S8234, S8235, S8266, S8267)
Describes applications of these devices, including 2- and 4-input 4-bit multiplexers, and a high speed 8-bit binary adder-subtractor.
Signetics Applications Handbook (5 pg.)
- 14 **"MSI Gating Arrays"**
(N8241, N8242, S8241, S8242)
Describes applications of these quad exclusive OR/NOR gates as high speed equality comparators, parity tester/generators, binary or BCD adders, and conditional complementors.
Signetics Applications Handbook (8 pg.)
- 15 **"A Simplified Approach to Testing CMOS Inverters and Gates"**
See listing under CMOS. (Solid State Scientific)

General

- 16 **"MOS 100-Bit Word Generator"**
Describes how to build a 100-bit word generator using MOS ICs.
National MOS Brief 1 (2 pg.)
- 17 **"MOS Clock Savers"**
Design and use of MOS Clock-Drive Networks. Offers tips for saving power and lowering component costs.
National MOS Brief 5 (2 pg.)

DIGITAL

High Speed Logic	High Speed Logic (cont)
<p>1 "Applications of the 9538 ECL/MSI High Speed Decoder" (9538) Includes applications of this 1 of 8 decoder in demultiplexing, code decoding, memory decoding, function generation. Fairchild Applications Note 308 (10 pg.)</p>	<p>10 "Using Shift Registers As Pulse Delay Networks" (MC10135) Discusses a high-speed delay shift register using the MC10135 flip flop. Motorola AN-565 (3 pg.)</p>
<p>2 "F10,000 Series ECL" (ECL Series) Operation and circuit parameters are described for the Fairchild ECL series. Fairchild Application Note 330 (6 pg.)</p>	<p>11 "High Speed Binary Multiplication Using the MC10181" (MC10181) Describes a 4-bit by 4-bit multiplier using this arithmetic unit. Shows expansion to 8-by-8-bit or 17-by-17-bit systems. Motorola AN-566 (3 pg.)</p>
<p>3 "Measure Frequency and Propagation Delay with High-Speed MECL Circuits" (MECL) Describes ECL frequency counter useful to 160 MHz and a propagation delay measuring circuit capable of 100-picosecond resolution. Motorola AN-586 (2 pg.)</p>	<p>12 "MECL Positive and Negative Logic" (MECL) Describes equivalences between positive and negative ECL logic and provides guides for converting between them. Motorola AN-567 (2 pg.)</p>
<p>4 "A High Speed FIFO Memory Using the MECL MC10143 Register File" (MCM10143) Describes the required features of a high speed FIFO design. Different approaches are compared and a design is shown using the MC10143 Multiport Register File. Motorola Application Note AN-730 (6 pg.)</p>	<p>13 "Interfacing With MECL 10,000 Integrated Circuits" (MC1650, MC1692, MC10115, MC10116, MC10124, MC10125, MC10128, MC10129, MC10216) Discusses circuits to interface ECL with TTL, TTL and IBM busses, MOS, low level signals, and LEDs. Motorola AN-720 (9 pg.)</p>
<p>5 "Testing MECL 10,000 Integrated Logic Circuits" (MECL) Describes AC and DC tests in a 50 ohm transmission-line environment for measuring logic levels or noise margins, circuit current, input currents, propagation delays, edge speeds, and flip-flop toggle rates. Motorola AN-579 (6 pg.)</p>	<p>14 "The MC1600 Series MECL III Gates" (MC1660, MC1661, MC1662, MC1663, MC1664, MC1665) Gives typical operating characteristics and explains the operation of various gates in the MECL III family. Describes recommended layout, breadboarding, and testing procedures. Motorola AN-504 (14 pg.)</p>
<p>6 "An MSI 500 MHz Frequency Counter Using MECL and MTTL" (MECL) Describes design of 8-digit LED readout counter using MECL III, 10,000 and TTL. Discusses two prescalers using MECL, two input amplifier designs, and a time-base controller for the counter's multiphase clock. Motorola AN-581 (9 pg.)</p>	<p>15 "IC Crystal Controlled Oscillators" (MC1023, MC1662, MC10101, MC10116) Describes use of MC1023 OR/NOR gate as an amplifier and oscillator. Discusses square wave oscillator circuits with crystal control capable of output frequencies up to 150 MHz. Examples use MC10116/10101, AND MC1662. Motorola AN-417A (4 pg.)</p>
<p>7 "A 200 MHz Autoranging MECL-McMOS Frequency Counter" See listing under Counters (Motorola)</p>	<p>16 "High Speed Monostable Multivibrators Designed With MECL Integrated Circuits" (MC1023, MC1026) Discusses two configurations using the MC1023 clock driver and a delay element that offer performance in excess of 70 MHz and pulse widths of 4 nanoseconds. Covers methods of obtaining the delay. Motorola AN-418 (5 pg.)</p>
<p>8 "Bussing with MECL 10,000 Integrated Circuits" See listing under Data Transmission (Motorola)</p>	<p>17 "MECL 10,000 Arithmetic Elements MC10179, MC10180, MC10181" (MC10179, MC10180, MC10181) Describes 10180 dual adder/subtractor, 10181 4-bit arithmetic logic unit/function generator, and 10179 lookahead carry block. Discusses their operation in parallel adders, in both ripple and lookahead systems. Motorola AN-709 (11 pg.)</p>
<p>9 "Interconnection Techniques For Motorola's MECL 10,000 Series Emitter Coupled Logic" (MECL) Describes some of the characteristics of high digital signal lines and gives wiring rules for MECL 10,000 circuits. Discusses p-c board interconnects, board-to-board interconnects, and wirewrapping techniques. Motorola AN-556 (22 pg.)</p>	

Bold face indicates additional data is provided on the page noted.

DIGITAL

High Speed Logic (cont)

- 1 **"Simulate MECL System Interconnections With A Computer Program"**
Develops a basic computer program that allows the user to simulate the performance of signal lines and to analyze termination techniques. Applies to ECL and other high speed digital systems.
Motorola AN-700 (10 pg.)
- 2 **"Understanding MECL 10,000 DC and AC Data Sheet Specifications"**
(MECL)
Discusses basic MECL 10,000 gate structure, transfer curve and dc levels. Covers specifications data sheet, including power supply drain current, high and low output voltages, propagation delay, rise and fall times, and toggle frequency.
Motorola AN-701 (7 pg.)
- 3 **"AC Noise Immunity of MECL 10,000 Integrated Circuits"**
(MECL)
Discusses ac noise immunity. Describes test circuits for measuring this immunity and the results to be expected for MECL 10,000 circuits.
Motorola AN-592 (6 pg.)
- 4 **"ECL 10,000 Series/10124, 10125"**
(10124, 10125)
Discussion of the transfer characteristics of the 10124 Translator/Driver and 10125 Translator/Receiver. Covers TTL/DTL to ECL level translation, TTL to ECL interface, differential line driver and receiver for TTL systems, terminations for differential data transmission.
Signetics Applications Handbook (4 pg.)

High Speed TTL

- 5 **"The MC3000/MC3100 Series Transistor-Transistor Logic Flip-Flops"**
(MC3150, MC3151, MC3152, MC3160, MC3161, MC3162, MC54H79, MC54H115, MC54H116, MC54H117, MC54119, MC54120)
Describes basic operation of the various flip-flops available in the MC3000/3100 (54H/79H) series and gives typical operating characteristics of each.
Motorola AN-493 (14 pg.)
- 6 **"Series 54S/74S Schottky TTL Applications"**
(SN54S Series, SN74S Series)
Analyzes Schottky clamping techniques and circuits, reviews circuit performance, including discussion of transfer characteristics, switching times, and a-c noise. Discusses power supply considerations, line driving and receiving, noise sources and their abatement. Normalized loading/driving capability information and the pinouts of ICs are discussed.
Texas Instruments Application Report CA-176 (45 pg.)

HNIL/HTL

- 7 **"Converting Relay Control Systems To Digital I/C's"**
(MC660 Series)
Defines and discusses basic Boolean algebra and logic functions and presents method of converting relay diagrams to logic diagrams. Gives examples of conversion method using High Threshold Logic circuits and presents a system design to accomplish this.
Motorola AN-524 (14 pg.)

HNIL/HTL (cont)

- 8 **"Using Motorola High Threshold Logic"**
(MC660 Series)
Describes MC660 series ICs and provides many of the characteristics of these units. Application examples include logic translation, line driving, and trigger circuits.
Motorola AN-467 (11 pg.)
- 9 **"Operation and Application of MHTL I/C Flip-Flops"**
(MC663, MC664)
Describes operation and characteristics of the J-K MC663P and the master-slave R-S MC664P flip-flops. Discusses applications as ripple and decade shift counters.
Motorola AN-414 (8 pg.)
- 10 **"Noise Immunity With Motorola High Threshold Logic"**
(MC660 Series)
Compares noise immunity characteristics between High Threshold Logic (HTL) and standard saturated logic devices. Discusses noise injection and noise reduction techniques.
Motorola AN-298 (5 pg.)
- 11 **"High Noise Immunity Logic -- Powerful, Versatile, and Growing"**
(300 Series)
Generally describes the HiNIL family use and features. Covers interface to other families, noise immunity, operating considerations and input protection.
Teledyne Semiconductor Digital Application Note No. 5 (5 pg.)
- 12 **"The HiNIL 347-A Dual Retriggerable One Shot with High Noise Immunity"**
(347)
Description and application details for this device are provided along with diagrams showing its use in pulse generators, coincidence detectors, frequency dividers, voltage to frequency and frequency to voltage converters, a pulse absence detector and an ac line presence detector.
Teledyne Semiconductor Digital Application Note No. 6 (6 pg.)
- 13 **"HiNIL 375 Universal Shift Register"**
(375)
Operation and applications of this synchronous 4-bit device as a 4 and 8-bit shift-left, shift-right register, 7 and 8-bit parallel-to-serial and serial-to-parallel converters and various counters.
Teledyne Semiconductor HiNIL Application Note 4 (10 pg.)
- 14 **"High Noise Immunity Logic"**
(300 Series)
Discussion includes noise immunity, loading rules, fanout, passive pull-up loading, collector or-ing, second level gating, driver pull-up, system interfaces.
Teledyne Semiconductor HiNIL Catalog (7 pg.)
- 15 **"Design Techniques with HiNIL 367 Quad Schmitt Trigger"**
(367)
General discussion of Schmitt Trigger and the differences of the 367, which ignores open inputs and offers 3.5 v noise immunity. Applications include line receivers, pulse stretchers, ac detectors, free-running and voltage-controlled oscillators.
Teledyne Semiconductor HiNIL Application, Note 2 (4 pg.)

DIGITAL

HNIL/HTL (cont)

- 1 **"Designing Programmable Controllers with HiNIL"**
(380)
Applications of the HiNIL 380 BCD to decade decoder including the generation of odd sequences of output pulses, the controlling of more than one load, and the switching on and off of loads.
Teledyne Semiconductor Digital Microcircuits Application, Note 3 (4 pg.)

- 2 **"Using the CD4520B to Design Dividers with Symmetrical Outputs"**
(CD4520A/B)
Describes how to use this CMOS counter to divide an input frequency by N where N is any integer from 2 to 256 and obtain outputs with approximately 50% duty cycles.
RCA Application Note ICAN-6362 (10 pg.)

Interface

See also Decoders.

- 3 **"9616/9617 EIA Interface Driver and Receiver"**
(9616, 9617)
Gives performance characteristics for these devices and describes their use in data communications equipment. Describes EIA standard RS232-C.
Fairchild Application Note 320 (6 pg.)
- 4 **"The Interface Handbook, Line Drivers and Receivers"**
(9612, 9613, 9614, 9615, 9616, 9617, 9627, 9634, 9635, 9636, 9637, 9638, 9640, 8T13, 8T14, 8T23, 8T24, 55107, 55108, 55109, 55110, 55121, 55122, 75107, 75108, 75109, 75110, 75112, 75121, 75122, 75123, 75124, 75154, 75207, 75208)
This comprehensive book covers the basics of transmission line theory along with methods for determining signal quality. Major chapters are titled: Data Transmission Lines and their Characteristics; Reflections, Computations and Waveforms; Long Transmission Lines and Data Signal Quality; and Forms of Operation (single/differential, direction of flow, analysis of common interfaces, etc.)
Fairchild Interface Handbook (1.18 pg.)
- 5 **"Interfacing with MECL 10,000 Integrated Circuits"**
See listing under High Speed Logic (Motorola)
- 6 **"Interface Techniques Between Industrial Logic and Power Devices"**
(MC660 Series, MC14000 Series)
Presents worst case design approaches to illustrate methods of interfacing CMOS and MHTL logic to various ac and dc power load levels. Gives examples using transistors and thyristors as load drivers. Covers direct coupled and level translation interfacing as well as opto-electronic coupling for high isolation.
Motorola AN-712A (18 pg.)
- 7 **"Semiconductors For Plated-Wire Memories"**
(MC4006, MC4007, MC4038 MC4040, MC4043, MC1514, MC1546)
Discusses operation and electrical characteristics of plated wire memories. Covers applications of drivers, sense amplifiers, and decoders as interface circuits. Also discusses memory organization and memory-related semiconductor applications.
Motorola AN-533 (15 pg.)

Interface (cont)

- 8 **"CMOS: A New Logic Type for Control Systems"**
Includes interface to HTL, L TTL, TTL, and DTL.
Motorola AN-574 (4 pg.)
- 9 **"Interface Techniques Between Industrial Logic and Power Devices"**
Presents worst case design approaches to illustrate methods of interfacing CMOS and MHTL logic to various ac and dc power load levels.
Motorola Applications Report AN-712A (19 pg.)
- 10 **"Interface Considerations for Numeric Display Systems"**
(MC14511, MC14543)
Gives basic information on LCD, LED, gas discharge, fluorescent and incandescent displays. Discusses interfacing 7 segment displays to logic with emphasis on multiplexed systems.
Motorola AN-741 (25 pg.)
"MM54C/MM74C Voltage Translation/Buffering" (MM54C901, MM54C902, MM54C903, MM54C904, MM74C901, MM74C902, MM74C903, MM74C904)
Interfacing PMOS to CMOS, CMOS to CMOS with different voltage levels, and CMOS to two standard TTL loads, are illustrated using 74C901 series devices.
National MB-14 (2 pg.)
- 11 **"Interfacing With MECL 10,000 Integrated Circuits"**
See listing under High Speed Logic (Motorola)
- 12 **"Driving 7-Segment LED Displays with National Semiconductor Circuits"**
(DM5446A, DM5447A, DM5448A, DM7446A, DM7447A, DS75491, DS75492, DS7856, DS7858, DS8856, DS8857, DS8858, DS8861, DS8863, DS8864, DS8865, DS8866)
Discusses configurations and construction of 7-segment LEDs and drive modes. Describes BCD to 7-segment decoder drivers, BCD to 7-segment LED drivers, MOS to LED segment drivers, four and five segment drivers, as well as digit drivers. Describes calculator and digital clock applications.
National Interface Handbook, AN-99 (12 pg.)
- 13 **"Using the MM5704 Keyboard Interface in Keyboard Systems"**
See listing under Encoders. (National)
- 14 **"TTL/MOS/DTL Interfaces"**
Techniques for coupling the above devices and characteristics of the interfaces.
National MOS Brief 7 (2 pg.)
- 15 **"COS/MOS Interfacing Simplified"**
(CD4000 Series)
Covers interfacing 4000A and B series with TTL, DTL, ECL, NMOS, PMOS, industrial and power control circuits, op amps and displays.
RCA Application Note ICAN-6315 (7 pg.)

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Interface (cont)

- 1 **"Applications of the RCA-CD4093B COS/MOS Schmitt Trigger"**
See listing under CMOS (RCA)
- 2 **"Interfacing COS/MOS with Other Logic Families"**
See listing under CMOS (RCA)
- 3 **"Constant Current LED Drivers"**
(N8T51, N8T54, N8T59, N8T71, N8T74, N8T75, N8T79)
Covers logic diagram, truth table and applications of 8T50/70 drivers, including driving common anode LEDs, common cathode LEDs, lamp test, and use with frequency counters.
Signetics Applications Handbook (4 pg.)
- 4 **"8T80, 8T90 and 8T18 Interface Elements"**
(N8T18, N8T80, N8T90, S8T18, S8T80, S8T90)
Describes applications including high level buffer, relay driver, lamp driver, Miller integrator, quad gate, TTL-MOS-TTL interface, and voltage translation.
Signetics Applications Handbook (8 pg.)
- 5 **"ECL 10,000 Series 10124/10125"**
See listing under High Speed Logic
(Signetics)
- 6 **"Interfacing with CMOS"**
See listing under CMOS. (Solid State Scientific)
- 7 **"Completely Monolithic IC Series for Gas Discharge Display Interface"**
(UDN-6144, UDN-6164, UDN-6184, UDN-7183, UDN-7184, UDN-7186)
Describes operation of high voltage IC's to drive the digits and segments of 200v (Panaplex) gas discharge displays.
Sprague Electric Microcircuit Application Report MAR75-1 (8 pg.)
- 8 **"Using Bipolar Logic to Improve Performance in CMOS and Microprocessor Systems"**
Suggests the use of HiNIL for improving noise performance, input protection, and output drive, and of LP Schottky for improved speed/power.
Teledyne Semiconductor Digital Application Note 7 (4 pg.)
- 9 **"TTL to MOS and MOS to TTL Interface Circuits"**
(SN7400, SN75107, SN75207, SN75270, SN75370, SN75450, SN75451, TMS1103, TMS4062)
Describes MOS/TTL interface circuits using bipolar transistors, JFETS, MOSFETS, and ICs.
Texas Instruments Application Report CA-170 (11 pg.)
- 10 **"Monolithic Interfacing in Computers"**
(SN7520 Series, SN75107, SN75109, SN75308, SN75324)
Discusses linear integrated circuits for computer interface applications including line circuits, memory drivers, and sense amplifiers.
Texas Instruments Application Report CA-122 (12 pg.)

Interface (cont)

- 11 **"Peripheral Interface Circuits with the SN75450"**
(SN75450)
A variety of logic level translation, lamp driving and power control circuits are given using SN75450 series peripheral drivers.
Texas Instruments Application Report CA-150 (6 pg.)

Low Power Logic

- 12 **"A Designer's Guide to Low-Power MSI"**
(93L Series)
Discusses characteristics of Am93L family: input-output currents, logic levels, switching considerations, loading rules.
Advanced Micro Devices Data Book, Catalog (4 pg.)

LSI, General

- 13 **"Advances in LSI Using Silicon Gate Technology"**
Discusses the silicon gate process and silicon gate devices in general. Compares silicon gate with other MOS technologies with respect to device characteristics, the effects of these characteristics, chip interconnection, chip area, and device fabrication.
Fairchild Semiconductor Application Note 307 (6 pg.)
- 14 **"Design of Custom LSI Circuitry for Modern Digital Systems"**
Discusses design of LSI devices. Covers size considerations, number of input/output connections, number of output drivers, use of repetitive patterns, use of computer aided design techniques, speed versus size and power, and interfacing.
General Instrument Microelectronics (7 pg.)

Multiplexers

- 15 **"TTL MSI Multiplexers and Demultiplexers"**
(DM7210, DM7842, DM8210, DM8842)
Describes features of DM7210 multiplexer and DM7842 demultiplexer and discusses their use in a synchronous digital data transmission system, a keyboard entry decoder, and as interterm generators.
National AN-37 (8 pg.)
- 16 **"3-Input, 4 Bit Multiplexers"**
(N8263, N8264, S8263, S8264)
Describes logic diagrams for 8263/4, data outputs for each selection code, and expansion for six 4-bit inputs.
Signetics Applications Handbook (3 pg.)
- 17 **"8-Input Digital Multiplexers"**
(N8230, N8231, N8232, S8230, S8231, S8232)
Covers expansion of these multiplexers and use as variable frequency counters or Boolean function generators.
Signetics Applications Handbook (6 pg.)

PLAs

- 18 **"How To Design With Programmable Logic Arrays"**
(DM8575, DM8576)
Discusses operation of PLAs and use as code converters, decode elements in digital processors and sequential controllers.
National AN-89 (8 pg.)

DIGITAL

PLAs (cont)

- 1 **"MOS Programmable Logic Arrays"**
(TMS2000 Series, TMS2200 Series)
Describes TMS2000 and TMS2200 Series programmable logic arrays. Describes their internal logic and operation. Provides ordering instructions.
Texas Instruments Application Report CA-158 (13 pg.)

Pulse Handling

- 2 **"Nanosecond Pulse Handling Techniques in I/C Interconnections"**
Discusses problems of pulse transmission and measurement for TEM mode on coax, stripline, and above-ground wire systems.
Motorola AN-270 (6 pg.)

Scalers

- 3 **"Eight-Bit Position Scaler"**
(N8243, S8243)
Provides general description and discusses applications of the 8243 as a bidirectional 7-position scaler and sequence generator, 24-bit 8-position shift right/left scaling array, and as a demultiplexer.
Signetics Applications Handbook (11 pg.)

Trigger Circuits

- 4 **"Quad Bus Receiver With Hysteresis Schmitt Trigger"**
(N8T380, S8T380)
Covers these applications: bus interface Schmitt trigger, frequency measurement, frequency division with square wave output, digital clock, variable modulus and high speed counters.
Signetics Applications Handbook (7 pg.)
- 5 **"Dual Zero-Crossing Detector"**
(N8T363)
Describes applications of 8T363 as a zero crossing detector, frequency doubler, high stability or bi-directional one-shot, low frequency oscillator, frequency to voltage converter, and a linear amplifier.
Signetics Applications Handbook (6 pg.)
- 6 **"8T14 as a Schmitt Trigger"**
(N8T14, S8T14)
Describes applications as a sine-to-square wave converter, a monostable multivibrator, and an oscillator.
Signetics Applications Handbook (2 pg.)
- 7 **"8T20 Bi-Directional One-Shot"**
(N8T20, S8T20)
Provides device description and describes applications in disc, drum and tape playback systems, a di-phase to binary receiver, and a binary to di-phase transmitter.
Signetics Applications Handbook (10 pg.)
- 8 **"Retriggerable Monostable Multivibrator"**
(N8T22)
Covers operation and application of the 8T22, including oscillator circuits, delayed pulse generation, missing or double pulse detector, voltage to frequency converter, and pulse duration transmission systems.
Signetics Applications Handbook (8 pg.)
- 9 **"Design Techniques with HiNIL 367 Quad Schmitt Trigger"**
See listing under HNIL/HTL (Teledyne Semiconductor)

Trigger Circuits (cont)

- 10 **"The HiNIL 347 - A Dual Retriggerable One Shot with High Noise Immunity"**
See listing under HNIL/HTL (Teledyne Semiconductor)
- 11 **"TTL One-Shot: SN74121"**
(SN74121)
Brief description of the SN74121 monostable multivibrator or "one-shot". Applications: stable gated clock pulse generator and a digital frequency-to-voltage converter.
Texas Instruments Application Report CA-128 (4 pg.)

TTL, General

- 12 **"The Control Engineers Guide to IC Applications"**
See listing under (Linear) Industrial Control (Motorola)
- 13 **"The TTL Applications Handbook"**
(9300, 9301, 9302, 9304, 9305, 9307, 9308, 9309, 9310, 9311, 9312, 9313, 9314, 9315, 9316, 9317, 9318, 9321, 9322, 9324, 9328, 9334, 9338, 9340, 9341, 9342, 93S43, 9344, 9345, 9348, 9350, 9352, 9353, 9354, 9356, 9357, 9358, 9359, 9360, 9366, 9368, 9369, 9370, 93H72, 9375, 9377, 9383, 9390, 9391, 9392, 9393, 9394, 9395, 9396, 9600, 9601, 9602, 9603, 74121, 12122, 7442, 7443, 7444, 7446, 7447, 7448, 7449, 7475, 7477, 7483, 7490, 7491, 7492, 7493, 7494, 7495, 7496, 74123, 74141, 74150, 74153, 74164, 74165, 74181, 74182, 74192, 74193, 7488A, 93141, 93150, 93153, 93164, 93165, 93406, 93410, 93415, 93434)
Gives diagrams and short descriptions of many IC applications grouped under the following categories: multiplexers, decoders, displays, encoders, operators (adders/subtractors, multipliers/dividers, comparator systems, error detection/correction, code conversion), latches, memories, registers, counters, small scale integration, low power TTL, Schottky TTL, monostable multivibrators and transmission line interface elements. The introduction discusses the advantages of MSI and general design rules. The final chapter covers electrical properties, physical system considerations, and interfacing with other forms of logic. Each application is brief, and various uses are shown for the ICs.
Fairchild Semiconductor TTL Applications Handbook (355 pg.)
- 14 **"Medium Scale Integration In the Numerical Control Field"**
(MC4016, MC4018, MC4024, MC4044, MC4324, MC4344)
Discusses operation of MC4016 decade programmable cascadeable counter, MC4324/4024 dual voltage controlled multivibrator, and MC4344/4044 frequency phase detector. Describes applications of these devices in audio frequency comparator, frequency synthesizer, and motor speed control circuits.
Motorola AN-541 (10 pg.)
- 15 **"TTL Integrated Circuits -- Applications of MSI Devices"**
Covers counters, modulo-N dividers, decoders, switches, adders, comparators, parity generators, shift registers and bus-ORable flip-flop. Describes many applications, including up/down counters, a stepping waveform generator, shift registers, frequency synthesizers, digital data demultiplexer, analog commutator, minterm generator, ripple carry parallel adder and tape position locator.
National AN-36 (23 pg.)
- 16 **"Tri-State Logic In High-Speed Memories of Microprogrammed Computers"**
(DM8551)
Discusses tri-state logic in general and its use in scratchpad memories. Covers storage of microinstructions and program constants in high-speed ROMs.
National AN-47 (5 pg.)

DIGITAL

TTL, General (cont)

- 1 **"Tri-State Logic Applied In a Computer System Can Reduce System Cost and Provide Added Performance"**
(DM8556)
Analyzes Tri-State characteristics using the DM8556 counter/register as an example. Shows how performance of PDP-8 can be improved using TSL.
National AN-73 (7 pg.)
- 2 **"Characteristics and Applications of Tri-State IC's"**
(DM7093, DM7490, DM7214, DM7230, DM7551, DM7598, DS7831)
Describes application of the general configuration of the Tri-State logic family and discusses application of the following: quad bus-buffer gates, dual 4:1 multiplexer, demultiplexer and bus-interchange switch, quad-D flip-flop, expandable 256-bit ROM, and quad driver.
National AN-45 (12 pg.)
- 3 **"Tri-State Logic In Modular Systems"**
(DM8093, DM8094, DM8214, DM8230, DM8551, DM8552, DM8598, DS8831, DM8840, DM8842, DM8846)
Discusses output drive characteristics, logical control, safety factors in Tri-State Logic circuits. Describes applications, including complex switching functions, driving and transmitting, multiplexing, data storage, decoding, and data manipulation.
National AN-43 (16 pg.)

LINEAR

Active Filters

- 4 **"Active Filter Design Examples Using Universal Active Filters"**
(UAF11, UAF15, UAF21, UAF25)
Shows calculation of external component values for low pass and band reject filters.
Burr-Brown Application Note AN-61 (4 pg.)
- 5 **"High Q Notch Filter"**
(LM102, LM202, LM302)
Describes use of LM102 connected to a twin "T" network to form a high Q, 60Hz notch filter.
National Linear Applications LB-5 (2 pg.)

Amplifiers, Current

- 6 **"Application of the LH0002 Current Amplifier"**
(LH0002)
Circuit operation. Describes uses in a differential input-output op amp, booster amplifier, level shifter, pulse transformer driver, and transmission line driver.
National Linear Applications Handbook, AN-13 (4 pg.)

Amplifiers, Differential

- 7 **"AD520 Monolithic Instrumentation Amplifier"**
(AD520)
Describes performance of this instrumentation amplifier. Covers application as a bridge amplifier, ground loop eliminator, and floating measurement amp. Appendix compares instrumentation amplifier to several multiple op amp circuits.
Analog Devices (6 pg.)
- 8 **"Instrumentation Amplifiers-versatile differential input gain blocks"**
(3660, 3670)
Describes the features and general operation of instrumentation amplifiers. Depicts their use in bridge circuits, in reducing ground loop interference, and in driven guard input circuits.
Burr-Brown Application Note AN-75 (6 pg.)
- 9 **"Instrumentation Amplifier"**
(LM101A, LM102, LM107)
Describes a differential-input instrumentation amplifier using LM102 and LM107 and variable gain version that also uses LM101A.
National Linear Applications LB-1 (2 pg.)
- 10 **"A General Purpose IC Differential Output Operational Amplifier"**
(MC1420, MC1520)
Discusses application of the MC1520 as a wideband non-inverting operational amplifier, as well as inverting operational amplifier, a differential amplifier with either single-ended input or differential input/output. Also discusses circuit operation, power connections, frequency compensation and feedback.
Motorola AN-407 (5 pg.)

Amplifiers, Differential (cont)

- 11 **"Application of the RCA-CA3000 Integrated-Circuit DC Amplifier"**
(CA3000)
Describes circuit and application as modulated oscillator, crystal oscillator, low-frequency mixer, cascaded RC-coupled feedback amp, narrow-band tuned amp, and Schmitt trigger.
RCA SSD-202B Linear Application Notes Databook, ICAN-5030 (11 pg.)

Amplifiers, Operational

- 12 **"Specifying Selected Op Amps and Comparators"**
See listing under Comparators (National)
- 13 **"Radiation testing of Linear Microcircuits"**
See listing under (Linear) General (Fairchild)
- 14 **"AD513, AD516 IC FET Input Operational Amplifiers"**
(AD513, AD514)
Describes the circuit and operation. Applications include: comparator, precision clipper, current-to-voltage converter, and a timer.
Analog Devices Technical Bulletin (4 pg.)
- 15 **"Applying the AD504 Precision IC Operational Amplifier"**
(AD504)
Describes this amplifier and offers notes on its noise, thermal and dynamic performance. Applications: instrumentation amplifier, stable reference regulator, instrument input amplifier and high gain ac amplifier.
Analog Devices Technical Bulletin (7 pg.)
- 16 **"High Speed Op Amps—How Fast is Fast?"**
Comments on op-amp characteristics, including slew rate, settling time, stability and phase margin.
Analog Devices Reprint (6 pg.)
- 17 **"IC FET Input Operational Amplifiers"**
(AD503, AD506)
Describes these devices and their circuit characteristics. Applications: triangle and square wave generator, charge amplifier, track and hold amplifier, D. C. voltmeter, peak rectifier, bridge amplifier and current-to-voltage converters.
Analog Devices Technical Bulletin (6 pg.)
- 18 **"Combine Two Op Amps to Avoid the Speed Accuracy Compromise"**
(3521)
Discusses interconnecting low drift and wideband op amps to form a composite op amp.
Burr-Brown Application Note AN-64 (2 pg.)

LINEAR

Amplifiers, Operational (cont)	Amplifiers, Operational (cont)
<p>1 "Check Five Op Amp Specs in One Test" Describes a test circuit that generates signals providing measurements of open loop gain, offset voltage, input bias current, quiescent current, and output voltage swing. Burr-Brown Application Note AN-65 (1 pg.)</p>	<p>10 "Operational Amplifiers as Inductors" (μA777) Includes derivation of equivalent circuit and necessary component values to obtain inductances from millihenries to kilohenries, using the μA777 as an example. Describes application in voltage controlled sinewave oscillators and in bandpass and notch filters. Fairchild Application Note 321 (5 pg.)</p>
<p>2 "Protect Op Amps from Overloads" Discusses protection from power-supply faults, keeping input voltages at safe levels, and limiting output currents. Burr-Brown Application Note AN-60 (3 pg.)</p>	<p>11 "Applications of the μA749 Dual Operational Amplifier" (μA749) Describes applications as a dual level comparator, positive or negative peak detector, peak-to-peak detector, and as an offset null circuit. Fairchild Application Note 268 (2 pg.)</p>
<p>3 "A Non-Inverting Differentiator" Bootstrapping an RC differentiator yields a precision differentiator without the phase inversion of a conventional op amp circuit. Discusses technique and operation. Burr-Brown Application Note AN-67 (1pg.)</p>	<p>12 "The μA776, An Operational Amplifier with Programmable Gain, Bandwidth, Slew-Rate, and Power Dissipation" (μA776) Describes methods for setting the master bias current, discusses amplifier frequency response as a function of this current. Discusses applications, including a 600 nanowatt amplifier, a low-cost sample and hold circuit, a current controlled oscillator, multiplexing, and phase shifting. Fairchild Application Note 218 (5 pg.)</p>
<p>4 "Using Op Amps in Low Noise Applications" Discusses shot noise and noise from source resistances. Burr-Brown AN-68 (2 pg.)</p>	<p>13 "The μA749 Dual Operational Amplifier" (μA749) Discusses the circuit, input voltage range, latch-up, output voltage range, power dissipation, noise, separation, high frequency compensation, and output capability. Fairchild Application Note 269 (8 pg.)</p>
<p>5 "A Simplified Precision Rectifier with Variable Gain" Operational amplifiers are used to build a rectifier circuit with variable gain. Burr-Brown AN-78 (2 pg.)</p>	<p>14 "The μA715 -- A Versatile High Speed Operational Amplifier" (μA715) Describes application as an image orthicon head amplifier, general purpose video amplifier, 40dB high input impedance amplifier, and high speed sample and hold circuit. Fairchild Application Note 265 (4 pg.)</p>
<p>6 "Design of a Unique Precision Controlled Current Source" Diagrams a current source using an op amp and a complementary FET pair to form a current source with differential input and bipolar current output. Burr-Brown AN-74 (2 pg.)</p>	<p>15 "A Low Drift, Low Noise Monolithic Operational Amplifier For Low Level Signal Processing" (μA725) Describes operation of μA725, which offers low offset drifts, low input currents, low noise performance, and massive open loop gain. Shows how to minimize offset voltage drift with temperature in IC operational amplifiers and how to improve the common-mode rejection. Fairchild Application Note 277 (10 pg.)</p>
<p>7 "The μA739 - A Low-Noise Dual Operational Amplifier" (μA739) Describes the circuit and operating characteristics. Covers d-c circuit performance, low-frequency analysis, power consumption, noise, short-circuit protection, amplifier isolation, and compensation techniques. Fairchild Application Note 175 (8 pg.)</p>	<p>16 "An Improved Sample and Hold Circuit Using the μA740" (μA740) Basic discussion of acquisition and hold times. Description of circuit using this op amp as the buffer amplifier. Fairchild Application, Note 297 (3 pg.)</p>
<p>8 "Applications of the μA741 Operational Amplifier" (μA741) Describes applications of this amplifier as a unity gain voltage follower, integrator, differentiator, voltage regulator reference amplifier, high voltage regulated power supply control element, clipping amplifier, and a comparator. Fairchild Semiconductor Application Note 289/1 (4 pg.)</p>	<p>9 "Applications of the μA777" (μA777) Discusses use of this operational amplifier as a pulse amplifier, Wein Bridge oscillator, variable gain differential amplifier, power amplifier. Fairchild Application Note 300 (3 pg.)</p>

LINEAR

Amplifiers, Operational (cont)	Amplifiers, Operational (cont)
<p>1 "Frequency Compensation Techniques for an Integrated Operational Amplifier" (μA702A) Presents design techniques for frequency compensation of μA702A which are applicable to other IC operational amplifiers. Fairchild Application Bulletin 117/2 (8 pg.)</p>	<p>8 "Test Procedures for Operational Amplifiers" Circuit for measuring offset voltage, bias current, offset current, open loop voltage gain, common mode and power supply rejection ratios, output voltage/current, power dissipation, and making continuity checks. Harris Application Note 508 (2 pg.)</p>
<p>2 "The HA-2530/2535 Wideband High Slew Inverting Amplifier" (HA-2530, HA-2535) Briefly discusses internal circuit. Shows how closed-loop frequency response can be predicted. Describes application as a fast settling coaxial driver, a 10 MHz coaxial line driver, a wide range signal separator, a high frequency triangular wave generator, and a current-to-voltage converter. Harris Application Note 516 (11 pg.)</p>	<p>9 "A Simple Comparator Using the HA-2620" (HA-2620) Describes op amp comparator circuit capable of driving approximately ten logic gates. Harris Application Note 509 (1 pg.)</p>
<p>3 "Applications of a Monolithic Sample-and-Hold/Gated Operational Amplifier" (HA-2420, HA-2425) Describes HA-2420/2425 circuit. Applications include various track-and-hold/sample-and-hold configurations, an A/D converter, a demultiplexer, an integrated-hold-reset amplifier, a gated operational amplifier, and a peak detector with reset. Harris Application Note 517 (8 pg.)</p>	<p>10 "A Simple Square-Triangle Waveform Generator" (HA-2510, HA-2600, HA-2620) Circuit for waveform generator using three op amps. Harris Application Note 510 (2 pg.)</p>
<p>4 "The HA-2900 Monolithic Chopper Stabilized Amplifier" (HA-2900) Discusses offset voltage and current drift and chopper stabilization, then describes the circuit. Applications include a high impedance differential instrumentation amplifier, use as an integrator, and several wide bandwidth configurations. Harris Application Note 518 (8 pg.)</p>	<p>11 "HA-909 Operational Amplifier" (HA-909, HA-911) Discusses applications as a unity gain breadboard op amp, servo preamplifier, high-Q bandpass filter, Wien bridge oscillator, and phase-delay filters. Harris Application Note 501 (2 pg.)</p>
<p>5 "The HA-2400 PRAM Four Channel Operational Amplifier" (HA-2400, HA-2405) This is a programmable input stage, operational amplifier. This note describes its applications including an analog multiplexer with buffered input and output, an inverting or non inverting amplifier with programmable gain, a sine wave oscillator with programmable frequency, and a track and hold/ sample and hold circuit. Harris Application Note 514 (8 pg.)</p>	<p>12 "HA-909 Operational Amplifiers Performance Tailoring" (HA-909, HA-911) Discusses how to optimize HA-909's offset, power dissipation, bandwidth, large signal bandwidth, slew rate, transient response, and stability with reactive loads. Harris Application Note 502 (3 pg.)</p>
<p>6 "Operational Amplifier Stability: Input Capacitance Considerations" (HA-2600, HA-2605) Discusses overcoming stray capacitance in op amps, such as the HA-2600. Harris Application Note 515 (2 pg.)</p>	<p>13 "Automatic Phase Margin Testing" (HA-2600) How to test op amps using an HA-2600 comparator, the 8405A vector voltmeter and a sweep generator. Harris Application Note 504 (2 pg.)</p>
<p>7 "A Simple Function Generator Using Operational Amplifiers" (HA-2600, HA-2510) Describes square and triangular waveform generator using HA-2600 and HA-2510 op amps. Harris Application Note 507 (2 pg.)</p>	<p>14 "A High Impedance Hysteresis Circuit" (HA-2520, HA-2620) Describes HA-2520/HA-2620 used as a hysteresis amplifier and covers output voltage limiting. Harris Application Note 505 (2 pg.)</p>
	<p>15 "Equivalent Input Noise Measurements on High Gain Monolithic Operational Amplifiers" (HA-709, HA-909, HA-2520, HA-2600) Broadband noise versus bandwidth measurements for HA-709,909, 2520, and 2600 op amps. Harris Application Note 506 (2 pg.)</p>
	<p>16 "The 8007 - A High Performance FET-Input Operational Amplifier" (8007) Circuit description, applications as log and antilog amplifiers, photocell amplifier, peak detector, sample and hold circuits, high impedance buffer, and Wien Bridge oscillator. Intersil Application Bulletin A005 (6 pg.)</p>

LINEAR

Amplifiers, Operational (cont)

- 1 **"The 8043 - A Low Cost Dual FET-Input Operational Amplifier"**
(8043)
Summary of circuit characteristics. Applications as automatic offset suppression circuit, staircase generator, sample and hold circuit, and instrumentation amplifier. Intersil Application Bulletin A008 (6 pg.)
- 2 **"Ultra Low Bias Current Operational Amplifier"**
(ICH8500, ICH8500A)
Brief discussion of ICH8500 and ICH8500A circuit characteristics. Describes applications as pico ammeter, sample and hold circuit, and gated integrator. Intersil Application Bulletin H001 (4 pg.)
- 3 **"The MC1556 Operational Amplifier and Its Applications"**
(MC1456, MC1556)
Gives characteristics and describes operation. Discusses application as a voltage follower, high impedance bridge amplifier, and a logarithmic amplifier. Motorola AN-522 (8 pg.)
- 4 **"Single Power Supply Operation of IC Operational Amplifiers"**
(MC1430, MC1431, MC1433, MC1530, MC1531, MC1533, MC1709, MC1709C)
Describes a split zener biasing technique that permits the use of these operational amplifiers from a single power supply. Discusses general circuit as well as specific ac and dc device considerations to minimize operating and design problems. Motorola AN-403 (3 pg.)
- 5 **"The MC1539 Operational Amplifier and Its Applications"**
(MC1439, MC1539)
Discusses dc and ac operation and the performance of this amplifier. Describes a high frequency feed-forward scheme and application as a comparator, voltage follower, differential amplifier, and a summing amplifier. Motorola AN-439 (22 pg.)
- 6 **"A Simple Technique for Extending Op Amp Power Bandwidth"**
(MC1433, MC1533)
Describes a method of reducing loop gain and using only as much compensation as needed to increase the power bandwidth. Cites the MC1533G as an example. Motorola AN-459 (3 pg.)
- 7 **"Using Transient Response To Determine Operational Amplifier Stability"**
(MC1439, MC1539)
Describes a technique for evaluating the stability of any feedback amplifier configuration by analyzing its response to a step-function input. Includes a theoretical analysis and an example using the MC1539 operational amplifier. Motorola AN-460 (9 pg.)

Amplifiers, Operational (cont)

- 8 **"The MC1535 Monolithic Dual Operational Amplifier"**
(MC1435, MC1535)
Gives complete ac and dc circuit analysis and discusses electrical characteristics. Discusses applications in a differential input/differential output circuit configuration, and as a signal level envelope detector. Describes an input compensation scheme for fast slew rate. Motorola AN-411 (9 pg.)
- 9 **"Getting More Value Out Of An Integrated Operational Amplifier Data Sheet"**
(MC1439, MC1539)
Describes operational amplifier open loop characteristics and significance to overall circuit operation. Discusses loop gain stability and bandwidth, also reviews offset voltage and current and resultant drift effects for closed loop operation. Uses MC1439/1539 as examples. Motorola AN-273A (9 pg.)
- 10 **"The MC1533 Monolithic Operational Amplifier"**
(MC1433, MC1533)
Analyses function of each stage of the circuit. Discusses methods for frequency compensating, and dc biasing. Describes application as a follower, twin tee filter and oscillator, voltage regulator, and a high input impedance voltmeter. Motorola AN-248 (11 pg.)
- 11 **"The MC1530, MC1531 Integrated Operational Amplifiers"**
(MC1430, MC1431, MC1530, MC1531)
Describes the function of each stage in the circuit, methods of frequency compensating and dc biasing. Discusses application as a summing circuit, integrator, dc comparator, and a transfer function simulator. Motorola AN-204A (13 pg.)
- 12 **"Analysis and Design of the Op/Amp Current Source"**
Develops expressions for the transfer function and output impedances of voltage controlled op amp current source using both ideal and non-ideal models. Discusses effects of parameter and temperature variations on performance. Motorola AN-587 (7 pg.)
- 13 **"An Applications Guide for Operational Amplifiers"**
(LH101, LH201, LM101, LM201, LM301)
Discusses applications of operational amplifiers, grouping them in five categories: simple amplifiers, operational circuits, transducer amplifiers, wave shapers and generators, and power supplies. National Linear Applications AN-20 12 pg.)
- 14 **"A Simplified Test Set for Operational Amplifier Characterization"**
(LM101, LM201, LM301, LM709)
Gives a functional description of set that allows quantitative characterization of the dc operational amplifier parameters for the LM101 and LM709. Discusses the circuit, includes construction information, and gives a layout for the tester circuit boards. National Linear Applications AN-24 (12 pg.)

LINEAR

Amplifiers, Operational (cont)

- 1 **"IC Op Amp Beats FETs on Input Current"**
(LM108, LM208, LM308)
Describes LM108 operation and performance. Applications: sample and hold circuit, integrator, sine wave oscillator, capacitance multiplier, instrumentation amplifier, logarithmic converter, transducer amplifier, current source and voltage comparator. Discusses PC board construction.
National Linear Applications AN-29 (20 pg.)

- 2 **"Logarithmic Converters"**
(LM101A, LM102, LM108)
Describes log generators, anti-log generators, cube generators, and multiplier/dividers, using the LM101A and LM108 op amps.
National Linear Applications AN-30 (4 pg.)

- 3 **"Op Amp Circuit Collection"**
(LM101A, LM102, LM107, LM108)
Gives schematics only for some 90 circuits using one or more of the following operational amplifiers: LM101A, LM102, LM107, LM108. Includes basic, signal generation and signal processing circuits.
National Linear Applications AN-31 (20 pg.)

- 4 **"New Design Techniques for FET Op Amps"**
(LH0022, LH0022C, LH0042C, LH0052, LH0052C)
Gives parameters for LH0022, LH0042 and LH0052 operational amplifiers. Discusses rationale for FETs in these devices, describes the circuits. Describes application as voltage followers, integrators, sample/hold amplifiers, comparators, instrumentation and charge amplifiers.
National Linear Applications AN-63 (12 pg.)

- 5 **"Micropower Circuits Using the LM4250 Programmable Op Amp"**
(LM4250, LM4250C)
Describes LM4250 circuit and bias current setting procedure. Applications: 500 nano-watt amplifier, micro-power comparator meter amplifier, pulse generator, instrumentation amplifier, and a 5V regulator for CMOS logic circuits.
National Linear Applications AN-71 (8 pg.)

- 6 **"The LM3900 -- A New Current-Differencing Quad of \pm Input Amplifiers"**
(LM3900)
Describes Norton "current mirror" circuit. Emphasizes the amplifiers' application in circuits for single power supply systems. Discusses use in ac and dc amplifiers, voltage regulators, RC active filters, waveform generators, phase locked loops, and voltage controlled oscillators.
Also covers designing digital and switching circuits, and special applications, including tachometers, squaring amplifiers, positive feedback oscillators, line operated audio amplifiers, and power circuits.
National Linear Applications AN-72 (39 pg.)

Amplifiers, Operational (cont)

- 7 **"Applications For A High Speed FET Input Op Amp"**
(LH0062, LH0062C)
Describes circuit, performance, compensation techniques for LH0062. Discusses applications in high speed sample and hold circuit, high speed peak detector, programmable integrator, and wide band ac voltmeter. Covers heat sinking, guarding, and bootstrapping.
National Linear Applications AN-75 (4 pg.)

- 8 **"Feedforward Compensation Speeds Op Amp"**
(LM101A, LM201A, LM301A)
Compares standard frequency compensation with feedforward frequency compensation of LM101A. Charts open loop response for both compensation networks. Shows fast integrator circuit.
National Linear Applications LB-2 (2 pg.)

- 9 **"Fast Compensation Extends Power Bandwidth"**
(LM101A, LM201A, LM301A)
Describes frequency compensation technique that extends power bandwidth of LM101A for non-inverting gains of unity to ten and also reduces gain error at moderate frequencies.
National Linear Applications LB-4 (2 pg.)

- 10 **"Precision AC/DC Converters"**
(LM101A, LM201A, LM301A)
Describes the use of the LM101A in a circuit for eliminating diode threshold potential, use as a precision clamp, as a fast half wave rectifier, and precision AC to DC converter.
National Linear Applications LB-8 (2 pg.)

- 11 **"Universal Balancing Techniques"**
Describes offset voltage adjustment: for inverting amplifiers using less than 10 K source resistance or using any type of feedback element, for non-inverting amplifiers, for voltage followers, and for differential amplifiers.
National Linear Applications LB-9 (2 pg.)

- 12 **"Speed Up the LM108 With Feedforward Compensation"**
(LM108, LM208, LM308)
Describes simple feedforward network for use with LM108 to achieve a factor of five improvement in speed.
National Linear Applications LB-14 (2 pg.)

- 13 **"Easily Tuned Sine Wave Oscillators"**
(LM101A, LM111, LM201A, LM211, LM301A, LM311)
Describes a circuit using the LM101A and LM111 that provides both a sine and square wave output for frequencies for below 20 Hz to above 20KHz. Also describes low distortion sine wave oscillator using two LM101As.
National Linear Applications LB-16 (2 pg.)

- 14 **"LM118 Op Amp Slews 70 V/ μ S"**
(LM118, LM218, LM318)
Describes this operational amplifier with 15 MHz bandwidth. Covers a compensation scheme to approximately double bandwidth and slew rate, and one for minimum settling time.
National Linear Applications LB-17 (2 pg.)

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Amplifiers, Operational (cont)	Amplifiers, Operational (cont)
<p>1 "Predicting Op Amp Slew Rate Limited Response" Discusses slew rate limiting and gives curves for sine wave and step voltage response. National Linear Applications LB-19 (2 pg.)</p>	<p>10 "Noise Specs Confusing?" Explanation of terms and factors contributing to noise; calculation of noise figure and signal to noise ratio. Gives points on selecting low noise amplifiers. National AN-104 (8 pg.)</p>
<p>2 "Low Power Operational LH0001 Amplifier" (LH0001) Operation of circuit offering 0.2 mv typical offset voltage at 25°C and quiescent supply currents in 100 μA range. National Linear Applications Handbook, AN-10 (4 pg.)</p>	<p>11 "Use the LM158/LM358 Dual, Single Supply OP Amp" (LM158, LM258, LM358) Proposes using this dual op amp with a single supply in place of the MC1458/MC1558 with a split supply. National AN-116 (4 pg.)</p>
<p>3 "Monolithic Operational Amplifiers - The Universal Linear Component" (LM101, LM102) Applications of the LM101 and, in some cases, the LM102, include free-running multivibrator, level shifting amplifier, voltage comparator, servo preamplifier, and computing circuits. Frequency compensation techniques are discussed in detail. National Linear Applications Handbook, AN-4 (10 pg.)</p>	<p>12 "Simple Precision Millivolt Reference Uses No Zeners" (OP-05) Describes — 3.5 mv to 3.5 mv reference built with instrumentation op amp and a potentiometer. Precision Monolithics Application Note AN-10 (1 pg.)</p>
<p>4 "Drift Compensation Techniques for Integrated DC Amplifiers" Op amp bias current and offset voltage compensation are discussed. Current compensation techniques for high impedance levels and methods to achieve chopper-stabilized drift performance at low impedance levels are covered. National Linear Applications Handbook, AN-3 (4 pg.)</p>	<p>13 "The monoOP-07 Ultra-Low Offset Voltage Op Amp—A Bipolar Op Amp That Challenges Choppers, Eliminates Nulling" (OP-07) Describes circuit design, compares performance to other devices. Covers application in a voltage reference, a high accuracy buffer, a D/A test system, a composite summing amplifier, an absolute value circuit, an analog computer building block, and as a thermocouple amplifier. Precision Monolithics Application Note AN-13 (12 pg.)</p>
<p>5 "True RMS Detector" Describes circuit using operational amplifiers that provide dc output equal to rms value of input with 2% accuracy for a 20 $V_{p,p}$ input signal from 50Hz to 100kHz. National Linear Brief-25 (2 pg.)</p>	<p>14 "Minimization of Noise in Operational Amplifier Applications" (OP-07) Describes internal and external sources of noise. Helps to locate noise sources by frequency. Gives examples of noise calculation using the OP-07 as an example. Precision Monolithics AN-15 (11 pg.)</p>
<p>6 "Instrumentational Amplifiers" (LM114, LM118) Discusses general purpose instrumentation amplifier, using LM114 matched transistors ahead of an LM118 op amp that is optimized for wide bandwidth. National Linear Brief-21 (2 pg.)</p>	<p>15 "Applications of the RCA CA3048 Integrated Circuit Amplifier Array" (CA3048) Discusses operating parameters for this 4-amplifier array and covers applications, including Hartley and Colpitts oscillators, an astable multivibrator, four-channel linear mixer, and a gain-controlled amplifier. RCA SSD-202B Linear Application Note Databook, ICAN-4072 (8 pg.)</p>
<p>7 "Low Drift Amplifiers" (LM121, LM725, LM741, LM308) Discusses problems causing circuit drift in amplifiers and recommends solutions. Includes discussion of thermal and electrical shielding, resistor choice, circuit layout, and offset balancing. National Linear Brief-22 (2 pg.)</p>	<p>16 "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers" (CA3080, CA3080A) This device has additional control terminal for flexibility. Circuit operation is discussed. Applications covered: communications and industrial systems, modulators, multiplexers, sample and hold circuits, gain control circuits, and micropower comparators. Appendix discusses current mirrors. RCA SSD-202B Linear Application Note Databook, ICAN-6668 (16 pg.)</p>
<p>8 "Versatile IC Preamp Makes Thermocouple Amplifier With Cold Junction Compensation" See listing under Pre-amplifiers. (National)</p> <p>9 "IC Preamp Challenges Choppers On Drift" See listing under Pre-amplifiers. (National)</p>	

LINEAR

Amplifiers, Operational (cont)	Amplifiers, Power
<p>1 "Application of the RCA CA3015 and CA3016 Integrated-Circuit Operational Amplifiers" (CA3015, CA3016) Describes operating characteristics at ± 12 v. Applications covered are: 50-dB amplifier; twin-T bandpass amplifier; 20-dB, 10-MHz bandpass amplifier; and voltage follower. RCA SSD-202 Linear Application Notes Databook, ICAN-5213 (6 pg.)</p> <p>2 "Application of RCA CA3033 and CA3033A High Performance Integrated-Circuit Operational Amplifiers" (CA3033, CA3033A) Describes the basic circuit and operation. Covers application as a 250 mw. power amplifier and shows use in a DVM as a multivibrator, staircase generator, and comparator. RCA SSD-202 Linear Application Notes Databook, ICAN-5641 (8 pg.)</p> <p>3 "Measurement of Burst (Popcorn) Noise In Linear Integrated Circuits" Discusses "pass-fail" criteria and describes a test set up for measuring burst noise. The setup includes a high gain amplifier-filter, a bipolar comparator, and a counter-latch-timer control circuit. RCA SSD-202 Linear Application Notes Databook, ICAN 6732 (8 pg.)</p>	<p>7 "The MC1554 One-Watt Monolithic Integrated Circuit Power Amplifier" (MC1554) Describes the circuit, including dc characteristics, frequency response, and distortion. Shows how to calculate package power dissipation using the curves on the data sheet. Describes application, as one watt non-inverting, inverting, pulse power, and three-watt differential output amplifiers. Motorola AN-401 (7 pg.)</p> <p>8 "LM380 Power Audio Amplifier" See listing under Consumer, Audio. (National)</p> <p>9 "LM377, LM378, LM379 Dual Two, Four and Six Watt Power Amplifiers" Discusses operation, choice and use of these circuits in audio applications. Covers distortion and heat dissipation. Also covers use in a bridge configuration, plus use as a Wein bridge power oscillator, motor drive, power comparator, relay and lamp driver. National AN-125 (11 pg.)</p> <p>10 "Application of the RCA CA3020 and CA3020A Integrated Circuit Multi-Purpose, Wide-Band Power Amplifiers" (CA3020, CA3020A) Circuit description and operation. Both circuits operate from single supply voltage as low as +3 v, offer voltage gains over 60 dB with a 3 dB bandwidth of 8 MHz. Discussion of audio, broadband and video amplifier, video line driver, motor controller and servo amp applications. RCA SSD-202 Linear Application Notes Databook, ICAN-5766 (8 pg.)</p>
<p>4 "Application of the RCA CA3008 and CA3010 Integrated-Circuit Operational Amplifiers" (CA3008, CA3010) Describes operating characteristics of two op. amps and their application in video amplifiers, frequency-shaping amplifiers, comparators, integrators, differentiators, scaling adders. Also covers the addition of a power output stage and/or input emitter followers. RCA SSD-202 Linear Application Notes Databook ICAN-5015 (15 pg.)</p> <p>5 "Fast Slewing Operational Amplifier" (NE531, SE531) Includes a schematic for the NE/SE531 and discusses applications in sample and hold circuits, active filters, precision rectifiers, voltage controlled amplifiers, and high speed inverters. Signetics Applications Handbook (6 pg.)</p> <p>6 "L144 Programmable Micro-Power Triple Op Amp" (L144) Describes device function, elements of programming, effects of slew rate limiting. Applications discussed include instrumentation amplifier, tone detectors, triple-amplifier active filters, and a micropower double-ended limit detector. Siliconix Application Note AN73-6 (6 pg.)</p>	<p style="text-align: center;">Amplifiers, RF</p> <p>11 "An Integrated Circuit AGC IF Amplifier" (μA757) Describes circuit and performance of μA757, which is recommended for applications in military and industrial equipment, also speech compressor amplifiers. Fairchild Semiconductor Application Note 204 (4 pg.)</p> <p>12 "A High Gain Integrated Circuit RF-IF Amplifier With Wide Range AGC" (MC1590G) Describes operation and Y parameters of the MC1590G. Applications include mixers plus IF, video, single and two-stage RF amplifiers. Motorola AN-513 (10 pg.)</p> <p>13 "An Integrated Circuit RF-IF Amplifier" (MC1550) Discusses MC1550 ac and dc operation, noise figure, and Y-parameters for calculating optimum power and voltage gain. Describes application as a tuned IF amplifier, oscillator, video-audio amplifier, and as a modulator. Motorola AN-247A (16 pg.)</p>

LINEAR

Amplifiers, RF (cont)

- 1 **"A Complete Monolithic AM/FM/SSB IF Strip"**
See listing under Consumer, AM/FM (National)
- 2 **"Applications of the LM173/LM273/LM373"**
(LM173, LM273, LM373)
Discusses FM, AM, and SSB operation of this multi-mode IF amplifier/detector.
National Linear Applications LB-13 (2 pg.)
- 3 **"Tuned Circuit Design Using Monolithic RF/IF Amplifiers"**
(LM171, LM703)
Discusses operating parameters for the LM171 and LM703 in emitter-coupled and cascode configurations. Brief description of 10.7 MHz emitter-coupled stage and 100 MHz cascode amplifier.
National Linear Applications Handbook, AN-6 (6 pg.)
- 4 **"Logarithmic IF Strips Using Monolithic Integrated Circuits"**
(SL521)
Describes operation of this log amplifier in successive detection type IF strips with center frequencies from 10 to 100 MHz. Covers broadband and narrow band circuits and describes in detail a 60 MHz wide-range logarithmic amplifier.
Plessey Semiconductor Technical Communication (3 pg.)
- 5 **"Application of the RCA-CA3002 Integrated-Circuit IF Amplifier"**
(CA3002)
Describes circuit, operating modes, characteristics, and application as an envelope detector, product detector, and a Schmitt trigger.
RCA SSD-202 Linear Application Notes Databook, ICAN-5036 (9 pg.)
- 6 **"Principal Features and Applications of the RCA-CA3040 Integrated-Circuit Wideband Amplifier"**
(CA3040)
Discusses bias modes, characteristics and ratings, stability, mounting, connections, and typical wideband amplifier circuits.
RCA SSD-202 Linear Application Notes Databook, ICAN-5977 (11 pg.)
- 8 **"Application of the RCA-CA3028A and CA3028B Integrated-Circuit RF Amplifiers in the HF and VHF Ranges"**
(CA3028A, CA3028B)
Describes circuits and operating modes. Covers use as an RF amp, autodyne converter, IF amp, and limiter.
RCA SSD-202 Linear Application Notes Databook, ICAN-5337 (10 pg.)
- 9 **"Application of the RCA CA3021, CA3022, and CA3023 Integrated-Circuit Wideband Amplifiers"**
(CA3021, CA3022, CA3023)
Describes circuit and operating characteristics. Covers video, 10 MHz IF, 455 KHz IF, 28 MHz two-stage limiter, and 500 kHz limiting amplifier applications.
RCA SSD-202 Linear Application Notes Databook, ICAN-5338 (12 pg.)

Amplifiers, RF (cont)

- 10 **"Application of the RCA CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers"**
(CA3004, CA3005, CA3006)
Discusses operating modes, Y parameters, noise performance, video amp capabilities, gain control, cross modulation and modulation distortion. Covers application as single-ended RF amplifier, tuned IF amplifier, mixer, suppressed-carrier modulator and product detector.
RCA SSD-202 Linear Application Notes Databook ICAN-5022 (26 pg.)

Amplifiers, Sense

- 11 **"Semiconductors for Plated-Wire Memories"**
See listing under (Digital) Interface
- 12 **"The MC1541, A Gated Dual-Channel Sense Amplifier For Core Memories"**
(MC1441, MC1541)
Discusses circuit operation, design considerations, interface problems, and applications.
Motorola AN-474 (10 pg.)
- 13 **"An Integrated Sense Amplifier For Core Memories"**
(MC1440, MC1540)
Discusses core memories and design considerations for a sense amplifier. Establishes performance and environmental specs for amplifier design, analyzes design of MC1540, and discusses measured performance.
Motorola AN-245A (7 pg.)
- 14 **"Dual Sense Amplifier"**
(N8T25)
Provides 8T25 description and covers applications in MOS memory systems.
Signetics Applications Handbook (4 pg.)
- 15 **"High-Speed Dual Differential Comparator/Sense Amp"**
See listing under Comparators. (Signetics)

Amplifiers, Video

- 16 **"Gated Video Amplifier Applications—The MC1545"**
(MC1445, MC1545)
Reviews basic operation and discusses applications, including several modulators, gated multivibrators, gated oscillators and FSK systems. Also discusses AGC, single supply operation, and temperature compensation of the active gate.
Motorola AN-491 (15 pg.)
- 17 **"An IC Wideband Video Amplifier With AGC"**
(MC1550)
Describes uses of the MC1550, including a single stage amplifier with 28 dB gain and 22 MHz bandwidth also as a 79 dB video amplifier with 10 MHz bandwidth. Gives AGC properties.
Motorola AN-299 (5 pg.)

LINEAR

Amplifiers, Video (cont)

- 1 **"Using the MC1545, A Monolithic Gated Video Amplifier"**
(MC1445, MC1545)
Describes ac and dc operation and discusses applications as a video switch, amplitude modulator, balanced modulator, pulse amplifier, frequency shift keyer and wideband differential amplifier.
Motorola AN-475 (7 pg.)

- 2 **"A Wide Band Monolithic Video Amplifier"**
(MC1552G, MC1553G)
Describes basic operation of the MC1552G and MC1553G, and the characteristics obtained as a function of the devices' operating modes. Applications: pulse amplifier, summing/scaling amplifier, oscillator, and tuned amplifier.
Motorola AN-404 (13 pg.)

- 3 **"Television Video IF Amplifier Using Integrated Circuits"**
See listing under Consumer, TV. (Motorola)

- 4 **"Application of the RCA-CA3001 Integrated-Circuit Video Amplifier"**
(CA3001)
Describes circuit and operating characteristics. Covers cascaded stages and use as a Schmitt trigger.
RCA SSD-202 Linear Application Notes Databook, ICAN-5038 (9 pg.)

- 5 **"The SG1401 Video Amplifier"**
(SG1401)
Discussion of fixed and variable gain. The high frequency stability is discussed to aid in optimizing the various configurations for this device.
Silicon General Linear IC Product Guide (2 pg.)

Arrays

- 6 **"Application of the RCA CA3018 Integrated Circuit Transistor Array"**
(CA3018)
Array of two isolated silicon epitaxial transistors plus two transistors with emitter-base common connections, suited for closely matched device requirements or interconnections with non-integrable components. Applications covered include IF-RF, video, agc, audio and dc amplifiers.
RCA SSD-202 Linear Application Note Databook, ICAN-5296 (5 pg.)

- 7 **"Application of the RCA-CA3019 Integrated-Circuit Diode Array"**
(CA3019)
Describes circuit configuration, operating characteristics and applications, including balanced modulator, high-speed gates, balanced mixer, and a ring modulator.
RCA SSD-202 Linear Application Notes Databook, ICAN-5299 (6 pg.)

- 8 **"Designing With An IC Transistor Array Containing Matched Super-Beta Transistors"**
(CA3095)
Describes CA3095 IC array. Applications: low frequency amplifier, low noise video amplifier, long-delay monostable multivibrator, low-input-bias current comparator, analog timer for long delays, high-input impedance dc-voltmeter circuit, and tape-head preamplifier.
RCA SSD-202 Linear Application Notes Databook, ICAN-6222 (9 pg.)

Arrays (cont)

- 9 **"Monolithic Darlington Arrays Reduce Interface Cost and Complexity"**
(ULN-2001A, ULN-2002A, ULN-2003A)
Discusses packaging and heat dissipation of these 50v, 100-350 ma units. Covers parallel operation, input currents and control of up to 125 watts.
Sprague Electric Microcircuit Application Report MAR 75-2 (8 pg.)

Communications

- 10 **"A Monolithic Microtransmitter"**
(LP2000)
Describes operation of the rf power generation, rf amplification, modulation and regulator portions of this IC suitable for HF to VHF, am/pulse modulation. Applications: 27 MHz AM transmitter, 72 MHz telemetry transmitter.
Lithic Systems Application Note LAN-102 (3 pg.)

- 11 **"Communication System Transmission Losses"**
Derives equations for computing insertion losses for components in a communication system. Gives computer generated tables, series resistance and reactance plus parallel resistance and reactance for various system impedances.
Motorola AN-710 (5 pg.)

- 12 **"A Unique Monolithic AGC/Squelch Amplifier"**
(LM170, LM270, LM370)
Describes operation of LM170. Applications: agc circuits with peak or with transistor detectors, squelch preamplifier with hysteresis, voice-operated-relay controls, Wein bridge oscillators, decade tunable oscillators, and a modulated 455 kHz signal generator.
National Linear Applications AN-51 (12 pg.)

- 13 **"SL600 Series - Integrated Circuits for Radio Communications"**
(SL600 Series)
Describes circuits and applications for the following: RF/IF amplifiers; limiting RF amplifier/detector; AGC generators; AF amplifier, VOGAD side tone amplifier; AM detector, AGC amplifier and SSB demodulator; multimode detector; microphone/headphone amplifier; double balanced modulators; and a square log device. Describes synchrodyne, superhet, SSB and multimode receivers; SSB and AM transmitters; SSB transceiver; a multi-mode transceiver and a Morse keyer.
Plessey Semiconductor Applications Manual (92 pg.)

- 14 **"Applications of CMOS Integrated Circuits and Communications Equipment"**
See listing under (Digital) CMOS. (Solid State Scientific)

- 15 **Modems**
See listings under (Digital) Data Transmission

LINEAR

Comparators

- 1 **"A New High-Speed Comparator - the Am685"**
(685)
Circuit design of wideband device with under 10 ns propagation delay for application in A to D converters, data acquisition system, and optical isolators.
Advanced Micro Devices Data Book, Catalog (8 pg.)
- 2 **"Varying Comparator Hysteresis without Shifting Initial Trip Point"**
Describes adding a positive feedback circuit to introduce precise variable hysteresis into the usual comparator switching action.
Burr-Brown Application Note AN-62 (1 pg.)
- 3 **"The μ A760 -- A High Speed Monolithic Voltage Comparator"**
(μ A760)
Gives a functional description and cites typical performance characteristics. Discusses applications, including level detectors and line receivers, zero crossing detectors, high speed A/D converters, pulse width modulators, and fast peak detectors.
Fairchild Application Note 311 (8 pg.)
- 4 **"The μ A750 Dual Comparator Subsystem"**
(μ A750)
Discusses the circuit, design considerations and applications, including use in a combined heater/air conditioner control, a malfunction indicator, an analog status indicator and display, and a minimum frequency detector.
Fairchild Application Note 315 (7 pg.)
- 5 **"Voltage Comparator Applications Using the μ A734"**
(μ A734)
Discusses application of this comparator as a wide range phase meter, VCO, pulse width discriminator, free running oscillator, and sine wave frequency divider with phase adjustment.
Fairchild Applications Note 323 (3 pg.)
- 6 **"Radiation Testing of Linear Microcircuits"**
Includes the 702. See listing under (Linear) General. (Fairchild)
- 7 **"The Operation and Use of a Fast Integrated Circuit Comparator"**
(μ A710, μ A711)
Describes circuits of μ A710 comparator and μ A711 dual comparator. Discusses dc accuracy and response time of both. Discusses applications in line receivers, double-ended limit detectors, multivibrators, switching regulators, and switching power amplifiers. Appendices cover accuracy as a function of component matching, and test methods.
Fairchild Application Note 116 (14 pg.)
- 8 **"A High Speed Dual Differential Comparator -- the MC1514"**
(MC1414, MC1514)
Describes circuit operation and applications, including level and limit detectors, multivibrators, line receivers, sense amplifiers, zero crossing pulse generator and a peak voltage detector.
Motorola AN-547 (13 pg.)

Comparators (cont)

- 9 **"Precision IC Comparator Runs from 5V Logic Supply"**
(LM111, LM211, LM311)
Describes the LM111 circuit. Applications: photodiode level detector, zero crossing detectors, digital interface circuits, multivibrators, oscillators, and a frequency doubler. Includes application hints.
National Linear Applications AN-41 (6 pg.)
- 10 **"LM139/LM239/LM339 A Quad of Independently Functioning Comparators"**
(LM139, LM239, LM339)
Describes LM139 circuit. Applications: comparators with hysteresis, limit comparators with lamp drivers, zero crossing detectors, oscillators, MOS clock drivers, wide range VCO, AND/NAND gates, OR/NOR gates, multivibrators, time delay generators, pulse width modulator, temperature alarm, tape reader and peak detector.
National Linear Applications AN-74 (16 pg.)
- 11 **"Fast Voltage Comparators with Low Input Current"**
(LM102, LM106, LM202, LM206, LM302, LM306)
Describes use of LM102 to buffer the input of the LM106 comparator. Applications: comparators for fast A/D converters, for zero crossing detectors, and for ac coupled signals.
National Linear Applications LB-6 (2 pg.)
- 12 **"An IC Voltage Comparator For High Impedance Circuitry"**
(LM111, LM211, LM311)
Describes LM111 circuit and comparison to LM106/LM710. Applications: zero crossing detector driving an analog switch, detector for a magnetic transducer, comparator for a low level photodiode, and driving a ground-referred load.
National Linear Applications LB-12 (2 pg.)
- 13 **"Specifying Selected Op Amps and Comparators"**
Discusses the most common parameters that are tested on operational amplifiers and comparators and the relative difficulty of testing on high speed equipment. Gives a guideline to tightened specifications.
National Linear Applications LB-26 (2 pg.)
- 14 **"Comparing the High Speed Comparators"**
(LM160, LM161, LM260, LM261, LM360, LM361)
Compares LM360 to μ A760 and LM261 to NE529. Covers application as a peak detector for tape and disk file channels and in a high-speed 3-bit A/D converter.
National AN-87 (6 pg.)
- 15 **"Interfacing Precision Monolithics Digital-to-Analog Converters with CMOS Logic"**
(DAC-100, DAC-01)
Analyzes input circuits of these DACs and CMOS interfaces. Describes a complete 10-bit DAC and an 8 bit A/D.
Precision Monolithics Applications Note AN-14 (4 pg.)

LINEAR

Comparators (cont)

- 1 **"High Speed Dual Differential Comparator/Sense Amp"**
(NE521, NE522, SE521, SE522)
Discusses applications of the 521/522 comparators as level detectors, line receivers, sense amplifiers, peak detectors, double ended limit detectors, A/D converters, and oscillators.
Signetics Applications Handbook (5 pg.)
- 2 **"A Simple Comparator Using the HA2620"**
See listing under Amplifiers, Operational (Harris)

Consumer, AM/FM

- 3 **"A Fully Integrated High Quality AM/FM Stereo Receiver"**
(μ A706, μ A720, μ A739, μ A753, μ A758, μ A3075)
Describes receiver using ICs with a comparison to discrete design.
Fairchild Application Note 328/1 (6 pg.)
- 4 **"Integrated Circuits For FM Receivers"**
(μ A703, μ A753, μ A758, μ A3075)
Describes ICs capable of performing all basic functions of an FM stereo receiver, except the front end. Discusses 753 IF block, CA3075 2nd end IF block, 758 stereo multiplex decoder, 706 audio power amplifier.
Fairchild Application Note 318 (7 pg.)
- 5 **"The μ A758, A Phase Locked Loop FM Stereo Multiplex Decoder"**
(μ A758)
Gives functional description of this device, including input buffer/amplifier and bias supply, demodulator, stereo switch and lamp driver, VCO, frequency dividers, and pilot phase and amplitude detectors. Discusses operating characteristics, testing and alignment.
Fairchild Application Note 319 (11 pg.)
- 6 **"The A732 and μ A767 Integrated Circuit Stereo Multiplex Decoders"**
(μ A732, μ A767)
Discusses stereo demodulation, stereo/monaural switching, and interstation audio mute switching sections of these devices. Describes performance characteristics, external components required, alignment and user options.
Fairchild Application Note 286 (8 pg.)
- 7 **"The μ A720 — An AM Radio IC"**
(μ A720)
Describes RF amplifier, oscillator, converter mixer, IF amplifier, AGC detector, and regulator of this IC. Discusses applications in automobile and table radios.
Fairchild Application Note 325 (7 pg.)
- 8 **"2 Watt Sound System"**
(ITT3701)
Describes the use of this FM Detector/Amplifier in FM and TV sound systems.
ITT Semiconductor 3701 Application Note (15 pg.)

Consumer, AM/FM (cont)

- 9 **"Integrated Circuit IF Amplifiers For AM/FM and FM Radios"**
(MC1350, MC1355, MC1357, MFC4010, MFC6010)
Discusses the use of ICs in four IF amplifiers: a high performance FM, a quadrature detector FM, A COMPOSITE AM/FM, and an economy model FM receiver.
Motorola AN-543 (14 pg.)
- 10 **"A Complete Monolithic IF Strip for AM/AGC Applications"**
(LM172, LM272)
Circuit operation of LM172/LM272. Covers application in superheterodyne and low frequency T.R.F. receivers.
National Linear Applications Handbook, AN-15 (6 pg.)
- 11 **"Scanning Logic for RF Scanner-Receivers Using CMOS Integrated Circuits"**
See listing under CMOS (Motorola)
- 12 **"A Complete Monolithic AM/FM/SSB IF Strip"**
(LM273, LM373, LM274, LM374)
Discusses LM273/LM373, AND LM274/LM374 IF amplifier/detectors. Includes description of FM, SSB, and AM detection. Applications include: FM slope detector, double conversion IF strip, and coherent phase locked receiver. Also includes application hints.
National Linear Applications AN-54 (8 pg.)
- 13 **"LM1800 (LM1310, LM1310E) Phase Locked Loop FM Stereo Demodulator"**
(LM1310, LM1310E, LM1800)
Describes this demodulator and discusses typical performance.
National AN-81 (11 pg.)
- 14 **"Low Cost IC Stereo Receiver"**
(LM1800, LM1820, LM3089)
Describes the complete circuit and performance of an AM/FM/Stereo receiver.
National AN-147 (4 pg.)
- 15 **"FM Remote Speaker System"**
Describes an FM transmitter which couples to its companion receiver thru the power lines. The system transmits speech or music and is suitable for home use as well as some factory applications.
National AN-146 (4 pg.)
- 16 **"An IC for AM Radio Applications"**
(CA3088)
Describes CA3088E and application as a basic subsystem in AM broadcast receivers, as a 10.7 MHz IF amp, and as a general-purpose amplifier array.
RCA SSD-202 Linear Application Notes Databook, ican-6022 (4 pg.)
- 17 **"Integrated Circuits For FM Broadcast Receivers"**
(CA3005, CA3011, CA3012, CA3013, CA3014)
Discusses circuits for FM tuner, IF amplifier, limiter, and detector applications.
RCA SSD-202 Linear Application Notes Databook, ICAN-5269 (7 pg.)

LINEAR

Consumer, AM/FM (cont)

- 1 **"Integrated-Circuit Frequency-Modulation IF Amplifiers"**
(CA3012, CA3028)
Describes CA3012 and CA3028 differential amplifiers and application in IF-Amplifier strips.
RCA SSD-202 Linear Application Notes Databook, ICAN-5380 (7 pg.)

- 2 **"Application of the CA3089E FM-IF Subsystem"**
(CA3089)
Discusses stability considerations and following circuits: quadrature-detector, audio and AFC, mute, tuning meter and rf-agc, if amplifier/detector system and stereo decoder. Also covers operation at frequencies other than 10.7 MHz.
RCA Application Note, ICAN-6257 (8 pg.)

- 3 **"Integrated-Circuit Stereo Decoder Using the CA3090AQ Stereo Multiplex Demodulator"**
(CA3090AQ)
Gives circuit description. Describes the LC oscillator, reactance, stereo defeat, dc coupled flip-flop, preamplifier and phase splitter circuits.
RCA Application Note, ICAN-6259 (10 pg.)

- 4 **"A Demonstration Integrated Circuit FM Stereo Receiver"**
(ULN-2136, ULN-2209, ULN-2277, ULN-2244)
Describes the design and performance of a receiver using these ICs.
Sprague Electric Microcircuit Application Report MAR 73-4 (10 pg.)

- 5 **"Monolithic Integrated Circuits For Stereo Processing"**
(ULN-2120, ULN-2122)
Discusses use of the ULN-2120/22 to perform various functions in FM stereo receivers ranging from those with automatic mute and stereo mono-switching to those with no muting and manually activated switching.
Sprague Electric Engineering Bulletin 27109.1 (8 pg.)

Consumer Audio

- 6 **"MOS Circuit for Electronic Organs"**
(S2193, S2470, S5255, S5256)
Describes the use of ICs for various electronic organ circuits
American Microsystems AP74-10 (7 pg.)

- 7 **"Applications of the μ A739 and μ A749 Dual Preamplifier Integrated Circuits In Home Entertainment Equipment"**
(μ A739, μ A749)
Describes circuit operation. Discusses d-c and a-c considerations, compensation and noise performance. Covers applications as a stereo tape amplifier, a high fidelity phonograph preamplifier, and a TV remote control amplifier.
Fairchild Application Note 171 (7 pg.)

Consumer Audio (cont)

- 8 **"A High Output Power, (5 Watt), Low Distortion, IC Audio Amplifier"**
(μ A706)
Describes circuit, functions, design considerations of the μ A706. Discusses applications as an audio amplifier with the speaker load connected to ground, with the speaker load between supply and output, and discusses use in an FM stereo receiver.
Fairchild Application Note 317 (6 pg.)

- 9 **"Designing a Basic Organ System Using the MK50240"**
(MK50240)
Describes an organ system using the MK50240 Top Octave Generator for each octave.
Mostek (3 pg.)

- 10 **"LM380 Power Audio Amplifier"**
(LM380)
Describes the circuit and general operating characteristics. Applications: phono amplifier, bridge amplifier, and intercom.
National Linear Applications AN-69 (7 pg.)

- 11 **"Application of the RCA-CA3007 Integrated- Circuit Audio Amplifier"**
(CA3007)
Describes circuit. Covers application as dual- supply audio driver in a direct-coupled audio amp, and as single-supply audio driver in a capacitor- coupled audio amp.
RCA SSD-202 Linear Application Notes Databook, ICAN-5037 (4 PG.)

- 12 **"The ULN-2280 Amplifier"**
(ULN-2280)
Describes this single power amplifier circuit and discusses applications as a low-cost phonograph amplifier, amplifier with tone controls, common mode amplifier, full bridge amplifier, and in a mono FM receiver.
Sprague Electric Microcircuit Application Report MAR 73-2 (8 pg.)

- 13 **"Low-Cost-Dual Class B Driver"**
(ULN-2277, ULN-2278)
Describes the ULN-2277/78 ICs and describes use in dual 2-watt and dual 15-watt amplifiers.
Sprague Electric Microcircuit Application Report MAR 73-5 (3 pg.)

Consumer, Medical

- 14 **"A Personalized Heart-Rate Monitor With Digital Readout"**
(MC1776, MC14013, MC14040, MC14572)
Describes digital heart-rate monitor using the MC1776 op amp and CMOS digital ICs.
Motorola AN-714 (4 pg.)

Consumer, TV

- 15 **"The μ A780, μ A781 AND μ A746 Integrated Circuit Color TV Chroma Processing System"**
(μ A780, μ A781, μ A746)
Describes operation of μ A780 chroma sub-carrier regenerator and μ A781 chroma IF amplifier. Discusses their application along with the μ A746 chroma demodulator as a complete IC chroma processing system for NTSC color TV receivers.
Fairchild Application Note 210 (10 pg.)

LINEAR

Consumer, TV (cont)	Consumer, TV (cont)
<p>1 "The μA746 Color TV Chroma Demodulator" (μA746) Reviews NTSC color system, the requirements and the operation of a chroma demodulator. Describes circuit and function of this demodulator which contains two doubly-balanced synchronous detectors and a decoder matrix. Fairchild Application Note 276 (5 pg.)</p>	<p>10 "Application of the RCA-CA3044 and CA3044V1 Integrated Circuits In Automatic-Fine-Tuning Systems" (CA3044) Describes circuits, operating characteristics and dynamic performance of this wide-band amplifier for AFC applications. RCA SSD-202 Linear Application Notes Databook, ICAN-5831 (5 pg.)</p>
<p>2 "2 Watt Sound System" See listing under Consumer, AM/FM (ITT Semiconductor)</p>	
<p>3 "Television Video IF Amplifier Using Integrated Circuits" (MC1330, MC1350, MC1352, MC1353) Discusses requirements of the video IF section of a TV receiver. Describes MC1350/2/3 amplifier and MC1330 detector circuits. Includes design for a practical TV IF amplifier and detector. Motorola AN-545 (11 pg.)</p>	<p>11 "Feedback-Type Volume-Control Circuits for RCA-CA3041 and CA3042 Integrated Circuits" (CA3041, CA3042) Describes several types of volume controls for television receivers using these ICs, with a detailed discussion of feedback control. RCA SSD-202 Linear Application Notes Databook, ICAN-5841 (4 pg.)</p>
<p>4 "Hybrid Modules For CATV Line Extender and Trunk Amplifiers" (MHW560, MHW561, MHW562) Covers circuit, packaging, and thermal considerations of MHW560/1 and 2 hybrid modules. Motorola AN-563 (5 pg.)</p>	<p>12 "A Single IC for the Complete PIX-IF-System in TV Receivers" (CA3068) Gives a detailed description of the circuit functions of the CA3068 and its use in color and b/w TV receivers. RCA SSD-202 Linear Application Notes Databook, ICAN-6303 (17 pg.)</p>
<p>5 "A Synthetic Spectrum Tuning System for TV" Describes a tuning system which generates a complete spectrum of TV channel markers to achieve precise tuning on any channel. Motorola AN-739 (12 pg.)</p>	<p>13 "A Flexible Integrated-Circuit Color Demodulator for Color Television" (CA3067) Describes circuit operation of the CA3067, including its output amplifiers, demodulator, demodulator preamp, and tint control amplifier. Describes use of this circuit in a red-green-blue system. RCA SSD-202 Linear Application Notes Databook, ICAN-6724 (8 pg.)</p>
<p>6 "Television Horizontal APC/AFC Loops: The Last 10 Percent" Discusses some of the common problems that may be encountered in the design of Horizontal APC/AFC loops and methods to avoid or overcome them. Motorola Application Note AN-727 (15 pg.)</p>	
<p>7 "A Disassociated Intercarrier Television Video IF Amplifier" (MC1331) Discusses a video IF system using the MC1331 low level multiplier detector. Motorola AN-751 (9 pg.)</p>	<p>14 "Application of the CA3126Q Chroma-Processing IC Using Sample-And-Hold Circuit Techniques" (CA3126Q) Detailed circuit description of this device, which requires only one adjustment; a trimmer capacitor to tune the crystal filter. Discusses performance data, the phase detector, sample and hold circuits, the VCO loop, first chroma amplifier and ACC servo loop, and the second chroma amplifier. RCA SSD-202 Linear Application Notes Databook, ICAN-6247 (8 pg.)</p>
<p>8 "A Medium Cost PLL Varactor Tuning System Utilizing Off-the-Shelf Logic" Describes a frequency domain tuning scheme for varactor TV tuners. Motorola AN-729 (14 pg.)</p>	
<p>9 "A Phase-Locked Loop Tuning System for Television" Describes a frequency domain tuning system using direct digital count down of the local oscillator. Motorola AN-744 (10 pg.)</p>	<p>15 "Description and Application of the RCA-CA3120E Integrated-Circuit TV-Signal Processor" (CA3120) Describes the operation and application of this device which includes TV video noise processor, agc and sync separator circuits. RCA SSD-202 Linear Application Notes Databook, ICAN-6302 (9 pg.)</p>

LINEAR

Consumer, TV (cont)

- 1 **"An Approach to a Unified Chroma System"**
Describes design approach that will eventually allow fabrication of a complete single-chip chroma system.
Sprague Electric TP 74-3 (9 pg.)

Converters

- 2 **"Beckman Model 845 Digital-to-Analog Converter"**
(845)
Discusses basic D/A converter performance including interface and transfer characteristics, then covers the performance of the 845 series.
Beckman Instruments (9 pg.)
- 3 **"Sample and Hold, Or High-Speed A/D Converters, How Do You Decide?"**
Uses 64-channel digital data-acquisition system as an example to discuss tradeoffs between converters. Covers dependency of sampling rate on input bandwidths, evaluation of system error budgets, and determination of the maximum system aperture.
Burr-Brown Application Note AN-56 (4 pg.)
- 4 **"D/A Converter Differential Linearity Error -- It Really Shows Up"**
Discusses differential linearity, the difference in analog output for a change between two successive digital input codes. Gives graphs of two examples with the same linearity specification.
Burr-Brown-Research Application Note AN-58 (2 pg.)
- 5 **"Don't Forget D/A Converter Tempco "**
Discusses offset, gain and linearity drift with temperature.
Burr-Brown Application Note AN-59 (3 pg.)
- 6 **"Principles of Data Acquisition and Conversion"**
Discusses basic principles of analog to digital systems including sampling rate, aperture error, accuracy, resolution, throughput, and codes.
Burr-Brown AN-79 (5 pg.)
- 7 **"Applications of the μ A9650 4-Bit High Speed Precision Current Source"**
(9650)
Describes electrical characteristics, input circuit design considerations, basic biasing. Covers applications, including 8, 10, and 12-bit D/A and A/D converters, sample and hold circuits, servo or tracking converters, and voltage-to-frequency converters.
Fairchild Application Note 324 (15 pg.)
- 8 **"Counter Type A to D Converter"**
(HI1080)
Circuit details of an A to D converter employing a unidirectional digital counter and the HI-1080 eight-bit D to A converter to generate a ramp voltage.
Harris Application Note 512 (3 pg.)

LINEAR—Converters (cont)

- 9 **"Digital-to-Analog Converter Applications"**
(HI1080, HI1085)
Operating modes and applications of HI-1080 converter, which features resistor ladder network and switching devices on same chip. Discusses cascaded D to A converter as well as up-down counter and successive approximation A to D converters.
Harris Application Note 511 (7 pg.)
- 10 **"Digital To Analog Converter Circuits Using the 8018A"**
(8018A, 8019A, 8020A)
Discusses D/A converters, both in general and their electrical specifications. Describes circuit operation for 8018A and covers its expansion to 8 and 12 bit units. Also discusses generating reference currents using zeners, pnp transistors or high-gain operational amplifiers as references. Describes system interface requirements.
Intersil Application Bulletin A010 (8 pg.)
- 11 **"Voltage Transients (Glitches)"**
(MN3008)
Discusses D/A converter analog voltage spikes appearing in the output following a change of input code.
Micro Networks AN-101 (2 pg.)
- 12 **"Truncation of A/D Converters"**
Describes how to reduce or to program the number of bits converted.
Micro Networks AN-102 (2 pg.)
- 13 **"When Should a Sample Hold Amplifier Be Used?"**
Covers the use of sample-hold amplifiers with A/D converters. Discusses use with dynamically changing signals and the droop rate of the sample-hold circuit.
Micro Networks AN-103 (2 pg.)
- 14 **"MN312 Connections for Bipolar Output"**
(MN312)
Shows use of an external op amp to convert a unipolar output to bipolar.
Micro Networks AN-104 (2 pg.)
- 15 **"Serial to Parallel Conversion"**
(MN502, MN5200, MN5210)
Covers timing considerations in the conversion of A/D converter output from serial to parallel form.
Micro Networks AN-106 (2 pg.)
- 16 **"Analog-To-Digital Cyclic Converter"**
(MC1456)
Discusses circuits and operation of medium speed-medium accuracy converter that uses successive approximation technique in which unknown analog input voltage is successively compared to reference voltage to determine each bit of digital output. A comparison of gray and binary code operation and an error analysis are provided.
Motorola AN-557 (10 pg.)
- 17 **"A Single Ramp Analog-To-Digital Converter"**
Discusses an A/D converter which incorporates a calibration cycle to insure 12 bit accuracy. Briefly covers errors encountered in the converter described.
Motorola AN-559 (9 pg.)

LINEAR

Converters (cont)	Converters (cont)
<p>1 "Generate Custom Waveforms Digitally" (MC1406, MC1458, MC74193) Describes method using a read only memory and off-the shelf ICs, including MC74193 TTL up-down counter, MC1406L D/A converter, and MC1458CP, which acts as output buffer and polarity switch. Applications include standard as well as non-standard waveforms. Motorola AN-589 (5 pg.)</p>	<p>10 "A Low Cost, Easy-to-Build Successive Approximation Analog-to Digital Converter" (DAC-100, CMP-01) General discussion of feedback A/D converters. Operation of A/D converter capable of 8-bit conversions in 6 us. The system is expandable to 10-bit resolution. It uses aimDAC100, monoCMP-01, and a successive approximation register. Precision Monolithics Application Notes AN-11 (8 pg.)</p>
<p>2 "High Speed Digital-To-Analog And Analog-To-Digital Techniques" Gives overview that includes voltage and current output D/As; parallel (flash), tracking, successive approximation, and parallel ripple A/Ds as well as nonsynchronous and synchronous VTF A/D, Glossary of terms. Motorola AN-702 (14 pg.)</p>	<p>11 "A Low Cost, High-Performance Tracking A/D Converter" (DAC-100, CMP-01) Basic operation of 8-bit tracking converter that uses aimDAC100 series 10-bit D/A converter, monoCMP-01 series comparator, and 4-bit MSI up/down counters. Precision Monolithics Application Notes AN-6 (8 pg.)</p>
<p>3 "Analog-To-Digital Conversion Techniques" Discusses open-loop and feedback techniques: frequency, pulse width, cascade, ramp, counter, successive approximation, multiple comparison subranging, nonlinear conversion, double and triple ramp conversion. Motorola AN-471 (21 pg.)</p>	<p>12 "DAC-08 Applications Collection" (DAC-08) Discusses the dual output, and high compliance. Covers use in a CRT display driver, bridge transducer control system, A/D converter, waveform generator, digital addition/subtraction with analog output, digital attenuator and microprocessor controlled A/D converter. Precision Monolithics AN-17 (12 pg.)</p>
<p>4 "Successive Approximation A/D Conversion" (MC1408, MC14559) Describes advances in successive approximation techniques with emphasis on SARs (Successive Approximation Registers.) Shows both a normal and a high speed A/D using these methods. Motorola Application Note AN-716 (8 pg.)</p>	<p>13 "Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC" (CD4007A) Discusses resistance networks for DAC's and a voltage-follower amp for single-supply operation. Describes a 9-bit COS/MOS DAC. RCA SSD-202 Linear Application Notes Databook, ICAN-6080 (6 pg.)</p>
<p>5 "Binary D/A Converters Can Provide BCD-Coded Conversion" See listing under (Digital) Converters (Motorola)</p>	<p>14 "Function and Application of 3 1/2 Digit A/D Converter Set" (LD110, LD111) Describes the operation of the LD110 digital processor and the LD111 analog processor. Various DVM circuits are shown including circuits for ratio, current, ac voltage and frequency measurements. A detailed error analysis is provided. Siliconix Application Note AN74-1 (12 pg.)</p>
<p>6 "Binary-to-BCD and BCD-to-Binary Conversion with Complex IC Functions" See listing under (Digital) Converters (Motorola)</p>	<p>Drivers</p>
<p>7 "Applications of the MC1405/MC14435 in Digital Meters" See listing under Instrumentation (Motorola)</p>	<p>15 "PIN Diode Drivers" See listing under Switches. (National)</p> <p>16 "Driver Circuits for the JFET Analog Switch" See listing under Switches. (Siliconix)</p>
<p>8 "Logarithmic Converters" See listing under Amplifiers, Operational. (National)</p> <p>9 "Low Cost, High Speed Analog-to-Digital Conversion with the DAC-08" (DAC-08) Discusses the successive approximation technique to A/D and describes three designs with conversion times of 1, 2 and 4 μ sec. Precision Monolithics Application Note AN-16 (8 pg.)</p>	<p>17 "Monolithic Memory Driver" (SN75324) Describes this monolithic memory driver and illustrates its use in addressing and driving a magnetic memory. Notes on circuit-board precautions and proper operation are provided. Texas Instruments Application Report CA-107 (6 pg.)</p>

LINEAR

Followers

- 1 **"A Fast Integrated Voltage Follower with Low Input Current"**
(LM102)
Circuit description. Use of the LM102 for analog commutator, sample and hold, ac amplifier and active filter applications.
National Linear Applications Handbook, AN-5 (11 pg.)
- 2 **"The LM110 -- An Improved IC Voltage Follower"**
(LM110, LM210, LM310)
Compares LM102 and LM110 circuits. Shows diagrams of LM110 as a high pass active filter, high Q notch filter, bandpass filter, and low drift sample and hold circuit.
National Linear Applications LB-11 (2 pg.)
- 3 **"Monolithic Operation Amplifiers - The Universal Linear Component"**
See Amplifiers, Operational (National)
- 4 **"Applications for a New Ultra-High Speed Buffer"**
(LH0033, LH0033C)
Describes LH0033 fast voltage follower/buffer, Applications; high speed dual limit comparator for MOS logic, instrumentation shield/line driver, high speed sample and hold circuit, 4.5 MHz notch filter, high input impedance AC coupled amplifier, output buffer.
National Linear Applications AN-48 (4 pg.)

General

- 5 **"Radiation Testing of Linear Microcircuits"**
(μ A702, μ A709, μ A710, μ A711)
Describes tested performance of μ A702 and μ A709 operational amplifiers and μ A710 and μ A711 comparators after having been irradiated with fast neutrons of energies greater than 0.01 MeV.
Fairchild Application Note 195 (13 pg.)
- 6 **"Solid State Gas/Smoke Detector Systems"**
Describes semiconductor and ionization chamber systems with some discussion of the use of these with CMOS ICs.
Motorola Application Note AN-735 (9 pg.)
- 7 **"CMOS Linear Applications"**
See listing under (Digital) CMOS National
- 8 **"MOS Analog Function Generator"**
Describes using MOS devices to construct an Analog Function Generator. The coding is stored in ROM.
National MOS Brief 3 (2 pg.)
National MOS Brief 4 (5 pg.)
- 9 **"Surface Acoustic Wave Technology"**
Presents surface acoustic wave fundamentals and use in delay lines, pulse compression filters, bandpass filters, oscillators and discriminators.
Plessey Semiconductor (10 pg.)

Industrial Control

- 10 **"Electronic Controller with an Equilibrium Sustaining Mode"**
(3500 series)
Discusses a controller formed with two operational amplifiers in a pulse width modulation circuit with feedback. The feedback operates from a heater through the medium being heated to sense amplifiers.
Burr-Brown Application Note AN-63 (2 pg.)
- 11 **"The Control Engineer's Guide to IC Applications"**
For digital ICs discusses types of logic, selection of package type, and designing ICs into circuits. For linear ICs covers cost factors, basic types, such as operational amplifiers and voltage regulators, and some circuit functions, such as limit detection.
Motorola AN-552 (21 pg.)
- 12 **"Variable Speed Control System For Induction Motors"**
(MC673, MC688)
Describes control scheme implemented with discrete components and IC logic coupled by an LED and a photo transistor. Gives example of a circuit used to drive a Class F, 60 Hz, permanent-split, capacitor induction motor with a 13 oz. in. load rating.
Motorola AN-575A (5 pg.)
- 13 **"A ROM-Digital Approach to PWM-Type Speed Control of AC Motors"**
Describes a pulse width modulation scheme to control motor speed. Shows a CMOS-ROM system to provide variable frequency drive for 1, 2 or 3 phase motors.
Motorola Application Note AN-733 (12 pg.)
- 14 **"Temperature Measurement Method Based on Matched Transistor Pair Requires No Reference"**
(monoMAT-01, monoOP-10)
Discusses properties of matched transistor pairs, then describes temperature measuring systems built with a matched pair, constant current sources, and a differential amplifier (monoOP-10)
Precision Monolithics Application Notes, AN-12 (6 pg.)

Instrumentation

- 15 **"Monolithic Thermal Converter Permits Wideband RMS AC Measurement"**
Describes (4131) monolithic thermal converter with a matched pair of npn transistors and diffused resistors. Discusses application as rms to dc converter and rms-voltage regulation.
Burr-Brown AN-76 (6 pg.)
- 16 **"Application Notes AN-205"**
(FX205)
Describes use of the FX205 pseudo sinewave generator as a tone generator, tone-burst generator, a divide by eight sinewave source and an fsk generator.
Consumer Microcircuits of America AN-205 (16 pg.)

LINEAR

Instrumentation (cont)	Instrumentation (cont)
<p>1 "A Digital Voltmeter Using the AY-5-3507" (AY5-3507) Gives schematics for the analog section, reference voltage generator, clock oscillator, and display circuitry required in addition to this logic IC to build a 3 1/2 digit voltmeter. General Instrument Microelectronics (5 pg.)</p> <p>2 "Everything You Always Wanted To Know About the 8038" (8038) Includes a detailed schematic and a series of questions and answers about using this function generator, which produces sine, square, triangular, sawtooth and pulse waveforms. Intersil Application Bulletin A013 (4 pg.)</p> <p>3 "A Precision Waveform Generator and Voltage Controlled Oscillator" (8038) Discusses the 8038 circuit and operation. Covers external adjustments, power-supply connections, frequency modulation, sweeping, and use in phase locked loops. Intersil Application Bulletin A012 (8 pg.)</p> <p>4 "A Synchronously Gated N-Decade Sweep Oscillator" (MC838P, MC856P, MC3061P) Describes prototype oscillator that can be swept over five decades. Discusses options that allow preselection of any one, two or five frequency decades between 10 Hz and 10 MHz, whether sequential or not. Motorola AN-540 (13 pg.)</p> <p>5 "Applications of MC1405/MC14435 in Digital Meters" (MC1405, MC14435) Provides a detailed applications reference for this two chip, dual slope A/D converter system. Motorola AN-748 (18 pg.)</p>	<p>9 "Precise Tri-Wave Generation" (LM118, LM119) Describes triangle-wave generator consisting of the LM118 integrator and two LM119 comparators. Discusses applications including VCO, regulator and operational amplifier testing. National Semiconductor Linear Brief-23 (2 pg.)</p> <p>10 "Solid State Altimeter for Transponder Applications" (LX3702) Describes a solid state altimeter using a pressure transducer. The unit provides an altitude transmission code for use with transponders, plus digital readout. National Transducer Handbook AN-109 (8 PG.)</p> <p>11 "Wide Range Function Generator" Constructing a function generator for sine waves as well as square and triangular waveforms that operates below 10 Hz up to 1 MHz, with usable output to approximately 2 MHz. Design technique; circuit design, and construction directions. National AN-115 (4 pg.)</p> <p>12 "Opto-Electronic Fault Indicator for Logic Circuits" Proposes use of visible-light-emitting-diodes (VLEDs) as logic indicators. Discusses VLED characteristics, applications and typical circuits. Texas Instruments Application Report CA-153 (4 pg.)</p> <p>13 "EPN2100 Thermal Printer" (EPN2100) Detailed discussion of this solid state thermal printer and its interface requirements. Texas Instruments Application Report CA-163 (6 pg.)</p> <p>14 "EPN2500 Thermal Printer" (EPN2500, SN74492, SN74495, TMS2502) Discusses this thermal printer and its interface requirements. Includes a description of the SN75495 Row Driver and the SN75492 Digit Driver to interface the printhead to MOSFET logic circuits, and the TMS2502 character generator for providing alphanumeric characters. Texas Instruments Application Report CA-175 (10 pg.)</p>
<p>6 "A 3 1/2 Digit DVM Using an Integrated Circuit Dual Ramp System" (MC1405, MC14435) Describes a complete digital voltmeter based on the MC1405/14435 device pair. Includes input buffers and autopolarity. Motorola AN-746 (6 pg.)</p> <p>7 "Generate Custom Waveforms Digitally" See listing under Converters. (Motorola)</p> <p>8 "A Fully Differential Input Voltage Amplifier (Instrumentation Amplifier)" (LM3900) Describes operation of instrumentation amplifier built with LM3900. Also shows how a transducer bridge amplifier system can be developed with LM3900. National Linear Applications LB-20 (2 pg.)</p>	<p>Modulators</p> <hr/> <p>15 "MC1596 Balanced Modulator" (MC1496, MC1596) Describes device operation and applications, including modulators and demodulators for AM, SSB, and suppressed carrier AM; frequency doublers; and HF/VHF double balanced mixers. Motorola AN-531 (12 pg.)</p> <hr/> <p>Multipliers</p> <hr/> <p>16 "AD530 Complete Monolithic Multiplier, Divider, Square Root-er" (AD530) Describes the device, its circuit, external connections and adjustments. Applications include use in a precision rectifier, a phase sensitive demodulator, an automatic level control, a voltage controlled filter, a voltage controlled oscillator, an amplitude modulator and a frequency discriminator. Analog Devices Technical Bulletin (11 pg.)</p>

Bold face indicates additional data is provided, see the Product Index.

LINEAR

Multipliers (cont)	Phase Locked Loops (cont)
<p>1 "Analog Modules Multiply User's Options" Discusses various types of multipliers, logarithmic converters, dividers and square rooters, peak detectors and comparing circuits. Applications: electron beam welder, 3-mode carriage control, position control, fog visiometer, optical measuring system, and lab pressure standard. Burr-Brown Application Note AN-55 (6 pg.)</p>	<p>9 "The μA758, a Phase-Locked Loop FM Stereo Multiplex Decoder" See listing under Consumer, AM/FM. (Fairchild)</p>
<p>2 "A Primer on Analog Multiplier Specifications" Discusses dc and dynamic performance specifications, including output and input offset, gain error, linearity, small signal and full power frequency response, output slewing rate, and settling time. Burr-Brown Application Note AN-51 (6 pg.)</p>	<p>10 "Introduction to the Phase Locked Loop" (HA-2820) General discussion of phase locked loops. Describes applications including a band-pass filter, FM receivers, data modems and synchronizers, a motor speed control, and a frequency synthesizer. Discusses features of HA-2800 and 2820 PLL. Harris Application Note 601 (7 pg.)</p>
<p>3 "Using IC Multipliers" Covers the use as a divider, square root generator, polynomial generator, sine generator, voltage tuned filter. Cites some applications where other ICs should be chosen. Burr-Brown Application Note AN-73 AN-73 (4 pg.)</p>	<p>11 "A General Analysis of the Phase Locked Loop" Discusses a linear model, stability considerations and steady state response for phase locked loops. Harris Application Note 602 (8 pg.)</p>
<p>4 "Analog Shpaing" (4301) Describes the use of the 4301 multifunction circuit which has the transfer function XY/Z. Includes rms to dc conversion, exponentiation, trigonometric functions, vector computation, and use as a log amp. Burr-Brown AN-70 (5 pg.)</p>	<p>12 "The HA-2820/2825 Low Frequency Phase Locked Loop" (HA-2820, HA-2825) Explains circuitry of these phase locked loops in 0.1 Hz to 3 MHz operation. Discusses methods for obtaining parameters of a linear model from device's performance curves. External connections are illustrated with an FM demodulator circuit. Harris Application Note 605 (7 pg.)</p>
<p>5 "A Precision Four Quadrant Multiplier" (8013) Describes the 8013 circuit, operation, and use in multiplication, division, squaring, square root, and variable gain. Intersil Application Bulletin A011 (5 pg.)</p>	<p>13 "A Frequency Synthesizer For Aircraft Automatic Direction Finding Systems" (MC4016, MC4044, MC1658) Describes a phase locked loop frequency synthesizer, which includes a MC4016 programmable decade counter, a MC4044 phase detector, and a MC1658 voltage controlled multivibrator. Motorola AN-594 (10 pg.)</p>
<p>6 "Analysis and Basic Operation of the MC1595" (MC1495, MC1595) Gives equations for the analysis of this linear four-quadrant multiplier and discusses characteristic performance. Covers multiplication, division, mean squares, square roots, roots and powers. Motorola AN-489 (14 pg.)</p>	<p>14 "A New Generation Of Integrated Avionic Synthesizers" Discusses several different types of servo phase locked loop systems and describes a synthesizer for avionic equipment. Motorola AN-553 (9 pg.)</p>
<p>7 "Wideband Amplifier/Multiplier" (SG1402) Operation and applications of the SG1402. Describes use as a single-ended variable gain amplifier, a modulator, and a demodulator. Silicon General Linear IC Product Guide (4 pg.)</p>	<p>15 "MITTL and MECL Avionics Digital Frequency Synthesizer" Describes phase detector, emitter coupled oscillator, prescaler, programmable counter and gives phase locked loop analysis, for a 118 MHz to 136 MHz synthesizer. Motorola AN-532A (10 pg.)</p>
<p>Phase Locked Loops</p>	<p>16 "Phase-Locked Loop Design Fundamentals" (MC4016, MC4024, MC4044, MC4316, MC4324, MC4344) Outlines fundamental design concepts for phase locked loops implemented with ICs. Gives equations using Laplace Transforms needed to evaluate the basic loop performance and briefly describes a design using MC4000 series devices. Motorola AN-535 (11 pg.)</p>
<p>8 "Precision PLL Systems Using the XR2207 and the XR2208" (XR2207, XR2208) Defines phase locked loop parameters and describes this two-chip PLL system. Includes circuit interconnections for both single supply and split-supply operation. Also gives PLL design equations. Exar Integrated Systems TB-1002 (6 pg.)</p>	

LINEAR

Phase Locked Loops (cont)	Phase Locked Loops (cont)
<p>1 "An ADF Frequency Synthesizer Utilizing Phase-Lock-Loop ICs" (MC1648, MC3062, MC4016, MC4018, MC4044, MC7400) Describes circuit for a synthesizer suitable for the local oscillator function in aircraft Automatic Direction Finder equipment. Covers programming, trouble shooting, power supply requirements, performance, circuit modifications, and circuit construction. Motorola AN-564 (9 pg.)</p>	<p>8 "Phase Locked Loop Applications" (NE560, NE561, NE562, NE565, SE565, NE566, SE566, NE567, SE567) Includes a glossary of phase locked loop terminology, a discussion of phase locked loop operation, and an analysis of the building blocks, including general comments about usage in applications such as demodulators and filters. Discusses the general loop setup, including center frequency selection, capture range, and the choice of input level. Describes measurement techniques. Gives a detailed description of monolithic phase locked loops, including schematic diagrams, and discusses interfacing. Covers expansion of loop capability, including a discussion of extending the operating frequency to 60 MHz. Applications covered: FM IF amplifier/demodulator with muting, FM demodulator, translation loop for precise FM, FSK demodulators, analog light-coupled isolators, phase modulators, dual tone decoders, a Touch-Tone decoder, ramp generators, saw-tooth and pulse generators, single tone burst generators. RF-FM generators, precision power inverter, aircraft VHF Omnidirectional Range (VOR) receiver, FSK data converter for a cassette recorder, self-resetting digital clock, tape recorder flutter meter, and a phase locked loop fluid flowmeter. Signetics Applications Handbook (64 pg.)</p>
<p>2 "A Medium Cost PLL Varactor Tuning System Utilizing Off-the-Shelf Logic" See listing under Consumer, TV (Motorola)</p>	<p>Photosensitive devices</p>
<p>3 "A Phase-Locked Loop Tuning System for Television" See listing under Consumer, TV (Motorola)</p>	<p>9 "Application of Reticon Photodiode Arrays in Electron and X-Ray Detectors" (RL Series) Describes the use of self-scanning photodiode arrays for detecting soft X-rays (1 to 10A) and electrons in the 10 to 100 KeV range. Reticon Application Note 101 (4 pg.)</p>
<p>4 "The Phase Locked Loop IC as a Communication System Building Block" (LM565, LM1596) Discusses basic phase locked loop operation, design considerations, noise performance and describes the LM565 circuit. Applications; IRIG channel demodulator, FSK demodulator, and weather satellite picture demodulator. National Linear Applications AN-46 (12 pg.)</p>	<p>Power Control</p>
<p>5 "SL650 Phase-Locked Loop Applications" (SL650, SL651) Describes the circuit and application of this device that can operate to 0.5 MHz. Applications: Modulators-AM, FM, FSK, PAM, SCAM, tone burst, phase shift, delta, PWM; Waveform Generators-sine, triangle, mark/space ratio, staircase; Demodulators; Modem Systems, and a Digital Voltmeter. Plessey Semiconductor SL650 Applications (32 pg.)</p>	<p>10 "A Monolithic Zero-Crossing AC Trigger (Trigac) For Thyristor Power Controls" (μA742) Describes the μA742 zero-crossing ac trigger, which minimizes radio frequency interference generation. Discusses the circuit and operation of this device. Covers application with an SCR in a half wave circuit, full wave circuits, isolated system connections, and multi-phase power systems. Fairchild Application Note 208 (5 pg.)</p>
<p>6 "Low-Power Digital Frequency Synthesizers Utilizing COS/MOS ICs" (CD4000 Series) Reviews digital phase-locked loops. Describes their implementation with CMOS for use in FM receiver synthesizers, both heterodyne and prescaling types. RCA SSD-203, COS/MOS Digital Databook, ICAN-6716 (15 pg.)</p>	<p>11 "Servo Motor Drive Amplifiers" Discusses design of transformerless, AC servo amps using power Darlington transistors and IC op amps. Describes two power amplifiers, one using a 28 v power supply, the other, high voltage transistors. Also covers four op amp preamps and 90° phase shifters. Motorola AN-590 (7 pg.)</p>
<p>7 "The RCA COS/MOS Phase-Locked-Loop — A Versatile Building Block for Micro-Power Digital and Analog Applications" (CD4046A) Discusses fundamentals of phase-locked-loops. Presents a detailed description of the CD4046A. Describes applications, including FM demodulators, frequency synthesizers, split-phase data synchronizers and decoders, and lock detection. RCA SSD-203 COS/MOS Digital Databook, ICAN-6101 (8 pg.)</p>	<p>12 "Pulse Width Modulation For Small DC Motor Control" (MC1458, MC1709, MC14010, MC14011) Discusses several circuits, using discrete, operational amplifier and IC devices, for developing pulse width modulation drive signals. Describes how these signals can control the speed of small motors, primarily permanent magnet types. Motorola AN-705 (4 pg.)</p>

LINEAR

Power Control (cont)

- 1 **"Power Control Using the Zero Voltage switch"**
(MFC8070)
Discusses zero voltage detector, pulse gate, input control, and charging circuit sections of the MFC8070. Describes application in a temperature controller that incorporates CMOS logic and optical couplers.
Motorola AN-597 (7 pg.)
- 2 **"A 20 KHz, 1 KW Line Operated Inverter"**
Describes application in 208-volt, line-operated, computer main-frame power supply. The output capability of the inverter is 5 v at 200 amp.
Motorola AN-588 (6 pg.)
- 3 **"Phase Control of AC Power with the SL440"**
(SL440)
Describes the operation of the SL440 power control circuit, and supply requirements. Applications include use with inductive loads, three phase systems, lighting, heating, motor and power supply control.
Plessey Semiconductor (38 pg.)
- 4 **"Power Switching Using Solid-State Relay"**
(CA3059)
Discusses advantages of triac over electro-mechanical relays. Covers basic parameters, such as surge in-rush currents, transient-voltages, suppression networks, turn-off considerations, and various modes of triac gating.
Also discusses ac power control by various circuit designs for ON/OFF control, zero-voltage switching, and line-voltage isolation.
RCA SSD-206 Thyristor, Rectifier Databook, AN-6141 (5 pg.)
- 5 **"Triac Power Controls For Three-Phase Systems"**
(CA3059)
Describes basic approach to designing triac control circuits for use in the switching of three-phase power. Outlines basic design rules and describes CA3059 zero-voltage switch. Discusses methods of isolation of dc logic circuitry. Covers recommended configurations for power control circuits.
RCA SSD-206 Thyristor, Rectifier Databook, AN-6054 (6 pg.)
- 6 **"Solid-State Approaches To Cooking Range-Control"**
(CA3059, CA3080, CA3079, CD4013A, CD4015A)
Discusses application of ICs to cooking range control, both top burner and oven/broiler controls. Covers low-resistance sensors, zero-voltage switching and central processor control.
RCA SSD-206 Thyristor, Rectifier Databook AN-6096 (8 pg.)
- 7 **"Some Applications of a Programmable Power Switch/Amplifier"**
(CA3094)
Brief circuit description of CA3094. Device delivers three watts average power, 10 watts peak power to external load. Applications include Class A power amplifiers and driver amplifiers for complementary transistors, wideband power multivibrators, oscillators, comparators, voltage regulators, analog timers, and motor-speed controllers.
RCA SSD-202 Linear Application Notes Databook ICAN-6048 (12 pg.)

Power Control (cont)

- 8 **"Features and Applications of RCA IC Zero-Voltage Switches"**
See listing under Switches. (RCA)
- 9 **"A Monolithic Amplifier-Detector SCR Firing Circuit"**
(ULN-2300)
Describes the operation of the ULN-2300 linear differential amplifier with integral SCR. Covers response, impedance characteristics and closed loop characteristics, open loop gain vs. temperature, and describes use as a sensitive control, as a drive amplifier in a typical control system and as a control for counters, relays, motors.
Sprague Electric TP69-4 (12 pg.)
- 10 **"Applications of High-Voltage/High-Current Monolithic Interface Circuits"**
(060, UHP-400 Series UHP-500 Series)
Application of Series 060 Dual Darlington Switch and Series 400/500 Power Drivers in aircraft lamp drive circuit, solenoid printer, and 4-phase bipolar stepping motor.
Sprague Electric TP 72-4 (5 pg.)
- 11 **"Programmable Trigger Circuit for Triac Phase Control"**
The circuit uses an operational amplifier and external components. Provides notes on operation and a circuit description. Applications: motor control, temperature control, switching rate control, and frequency controlled lighting.
Texas Instruments Application Report CA-137 (7 pg.)

Power Converters

- 12 **"+5 To -15 Volts DC Converter"**
(LM311)
Describes use of the LM311 comparator for this voltage conversion.
National Linear Applications LB-18 (2 pg.)
- 13 **"Switched Mode Power Supplies- Highlighting a 5-V, 40-A Inverter Design"**
Discusses advantages of various approaches to regulator circuits. Describes in detail an 80% efficient 5v, 40a inverter which includes CMOS logic and an opto-electronic coupler.
Motorola AN-737 (16 pg.)

Power Transistor IC

- 14 **"Fast IC Power Transistor with Thermal Protection"**
(LM195)
Circuit design of the LM195 IC power transistor, a three terminal device with safe area protection plus current and thermal limiting. Applications: 6 amp variable output switching regulator, 1 amp positive and negative voltage regulators, time delay circuit, and optically controlled switch, power amplifier and voltage follower.
National AN-110 (6 pg.)

LINEAR

Preamplifiers

- 1 **"Applications of the μ A739 and μ A749 Dual Preamplifier Integrated Circuits In Home Entertainment Equipment"**
See listing under Consumer, Audio. (Fairchild)

- 2 **"IC Preamp Challenges Choppers On Drift"**
(LM108A, LM121)
Describes circuit of the LM121 preamplifier and discusses offset balancing, achieving of low drift, and typical operating performance. Also covers effects of the associated operational amplifier citing the LM108A as an example
National AN-79 (8 pg.)

- 3 **"Versatile IC Preamp Makes Thermocouple Amplifier With Cold Junction Compensation"**
(LM321, LM308A)
Discusses use of LM321 preamp with LM308A operational amplifier to form a precision, low-drift operational amplifier that also acts as a cold junction compensator.
National Linear Brief-24 (2 pg.)

- 4 **"LM381 Low Noise Dual Preamplifier"**
(LM381)
Describes the circuit. Discusses application as various tape amplifiers, phono preamplifier, and an audio mixer.
National Linear Applications AN-64 (12 pg.)

- 5 **"LM381A Dual Preamplifier for Ultra-Low Noise Applications"**
(LM381)
Gives detailed description of circuit operation of LM381A.
National Linear Applications AN-70 (4 pg.)

Regulators

- 6 **"More Voltage Regulator Applications Using the μ A723"**
(μ A723)
Describes foldback current limiting in positive and negative regulators, negative shunt regulation, and other techniques applicable to use of this device.
Fairchild Application Note 276 (4 pg.)

- 7 **"The μ A7800 Series, Three-Terminal Positive Voltage Regulators"**
(μ A7800)
Discusses the circuit and operation of this 3-lead, 15-watt regulator series. Discusses variable output voltage, high output current negative voltage regulation and use as an audio amplifier.
Fairchild Application Note 312 (6 pg.)

Regulators (cont)

- 8 **"The Voltage Regulator Applications Handbook"**
(μ A104, μ A105, μ A109, μ A723, μ A7600, μ A7800, μ A78L00, μ A78M00, μ A79E00)
Gives specifications and parameters for various IC regulators and includes a selection guide. It devotes two chapters to each major regulator family, the first chapter describes design and electrical characteristics, the second discusses electrical and thermal considerations which are useful as application guidelines.
Includes appendices covering switching regulator and power supply design and a guide to the selection and operation of suitable power transistors. Applications of 7800 and 78M00 include fixed output, current and dual polarity regulators.
The 79E00 applications include use as a high current negative voltage regulator. The 723 is discussed in 150 mA maximum, positive shunt regulators with high line rejection or high input voltage, floating positive regulators, medium/high output current negative regulators, and several other applications.
The 104, 105, and 109 applications include high current, switching and floating regulators.
Fairchild Voltage Regulator Applications Handbook (96 pg.)

- 9 **"Development, Analysis, and Basic Operation of the MC1560-61 Monolithic Voltage Regulators"**
(MC1460, MC1461, MC1560, MC1561)
Discusses the basic operation of these regulators, gives data sheet parameters, and identifies problems in specifying a monolithic voltage regulator. Also covers basic circuit configurations and typical performance.
Motorola AN-500 (8 pg.)

- 10 **"Shutdown Techniques For the MC1560/61/69 Monolithic Voltage Regulators"**
(MC1460, MC1461, MC1469, MC1560, MC1561, MC1569)
Discusses the ways the MC1560 shutdown control can be used, including logic control, short circuit detection, over voltage detection, junction temperature control, and thermal feedback. Also covers current foldback and methods of restarting automatically from the shutdown state.
Motorola AN-499 (7 pg.)

- 11 **"Voltage and Current Boost Techniques Using the MC1560-61"**
(MC1460, MC1461, MC1560, MC1561)
Discusses stability requirements for these current boosted regulators. Describes internal and external compensation techniques, gives heatsink design information, provides typical circuits, and covers a voltage boost circuit.
Motorola AN-498 (11 pg.)

- 12 **"Designing Digitally-Controlled Power Supplies"**
(MC1406, MC1408, MC1466, MC1723)
Discusses two approaches to designing power supplies, one using the MC1723 voltage regulator, the other using the MC1466 floating regulator with optoelectronic isolation. Also discusses BCD-to-binary converter and memory options.
Motorola AN-703 (8 pg.)

LINEAR

Regulators (cont)

- 1 **"A Monolithic High-Power Series Voltage Regulator"**
(MC1560, MC1561)
Describes a regulator capable of delivering 1/2 ampere of current. Discusses ac reference shifting circuit, voltage and current reference generation, tracking current sources and biasing its lateral p-n-p current sources.
Motorola AN-473 (7 pg.)
- 2 **"A New Approach to Switching Regulators"**
Describes a 24 volt 3 ampere switching mode supply which operates at 20 kHz from a 120 volt AC line with 70% efficiency. Briefly discusses load-line shaping to reduce power losses and to reduce noise.
Motorola AN-719 (11 pg.)
- 3 **"LM340 Series Three Terminal Positive Regulators"**
(LM340)
Describes this 1 ampere regulator circuit. Applications: constant current source, high current regulator with short circuit current limit, 5 v regulator for TTL, adjustable output voltage regulators, tracking dual regulator, and high voltage regulators.
National AN-103 (12 pg.)
- 4 **"Designs for Negative Voltage Regulators"**
(LM104, LM204, LM304)
Describes the LM104 and covers pitfalls that cause unexpected failures as well as protection schemes. Includes discussions of high current regulators, symmetrical power supplies, high voltage regulators, switching and high current switching regulators, and driven switching regulators.
National Linear Applications AN-21 (16 pg.)
- 5 **"The LM105 -- An Improved Positive Regulator"**
(LM105, LM205, LM305)
Describes the circuit of this regulator, power limitations, using booster transistors, foldback current limiting, and dominant failure mechanisms.
National Linear Applications AN-23 (8 pg.)
- 6 **"IC Provides On-Card Regulation for Logic Circuits"**
(LM109)
Discusses design of regulators in general and describes the LM109. Covers application as a fixed 5V regulator, adjustable-output regulator, current regulator and high stability regulator.
National Linear Applications AN-42 (6 pg.)
- 7 **"1.2 Volt Reference"**
(LM113)
Describes the LM113 temperature compensated shunt regulator diode. Applications: low voltage regulator circuits, bias current source for a differential amplifier, and an electronic thermometer circuit.
National Linear Applications AN-56 (4 pg.)

Regulators (cont)

- 8 **"Worst Case Power Dissipation in Linear Regulators"**
(LM100, LM104, LM200, LM204, LM300, LM304)
Discusses problems of excessive dissipation in regulators and suggests solutions using LM100 and LM104.
National Linear Applications LB-3 (2 pg.)
- 9 **"Tracking Voltage Regulators"**
(LM104, LM105, LM204, LM205, LM304, LM305)
Describes adjusting several regulator voltages with one potentiometer, tracking positive and negative regulators using the LM104 as an amplifier, and tracking regulators with different output voltages.
National Linear Applications LB-7 (2 pg.)
- 10 **"IC Regulators Simplify Power Supply Design"**
(LM104, LM105, LM204, LM205, LM304, LM305)
Describes use of LM104 and LM105, IN 0.2 and 2A regulator circuits. Provides circuit construction hints.
National Linear Applications LB-10 (2 pg.)
- 11 **"High Stability Regulators"**
(LM108A, LM109, LM208A, LM209, LM308A, LM309)
Describes design and gives schematics for high stability positive and negative regulators using LM109 and LM108A.
National Linear Applications LB-15 (2 pg.)
- 12 **"New Uses for the LM100 Regulator"**
(LM100)
Applications include shunt regulator, switching regulator with overload shutoff, temperature controller, power amplifier, SSB transmitter, light-intensity regulator, and photomultiplier tube supply.
National Linear Applications Handbook, AN-8 (12 pg.)
- 13 **"A Versatile, Monolithic Voltage Regulator"**
(LM100)
Circuit operation. Applications for the LM100 between 2 v to 30 v (up to 2 amps with two external transistors) are discussed. Includes high power, switchback current limiting, negative voltage, temperature compensating, and switching regulators.
National Linear Applications Handbook, AN-1 (11 pg.)
- 14 **"Designing Switching Regulators"**
(LM100)
LM100 applications discussed include high current, driven switching, current limiting, negative and high voltage regulators, as well as switching and linear regulator combinations.
National Linear Applications Handbook, AN-2 (12 pg.)
- 15 **"LM125/LM126/LM127 Precision Dual Tracking Regulators"**
(LM125, LM126, LM127)
Circuit description, operation and applications, including current boosting, are discussed along with charts depicting external current limiting characteristics and a discussion of foldback current limiting. Electronic turn-off of the output without removing the input voltage is also described.
National Applications Report AN82 (15 pg.)

LINEAR

Regulators (cont)	Switches (cont)
<p>1 "The 4195 Regulator" (RC4195, RM4195) Describes application as a ± 15 v, 100 ma regulator; a ± 2.5 a regulator; a ± 15 to ± 50 v unit, or a complementary ± 3 to ± 27 v device. Raytheon Semiconductor Application Note (9 pg.)</p>	<p>6 "The IH5009 Series of Low Cost Analog Switches" (IH5009 Series) Describes circuit parameters, logic compatibility, and virtual ground switching applications including 4-channel multiplexer, gain ranging circuit, gain programmable amplifier and 16-channel multiplexer. Intersil Application Bulletin A004 (8 pg.)</p>
<p>2 "Applications of the CA3085 Series Monolithic IC Voltage Regulators" (CA3085) Circuit description of positive regulators with output currents up to 100 milliamperes from -55°C to $+125^{\circ}\text{C}$. Applications include high-current and constant-current regulators; switching, dual-tracking and high-voltage regulators. Use as a general purpose amplifier, and various methods of current limiting are mentioned. RCA SSD-202 Linear Application Notes Databook, ICAN-6157 (11 pg.)</p>	<p>7 "A New CMOS Analog Gate Technology" General discussion of "latch up". Describes "floating body" process, which eliminates this problem. Intersil Application Note A006 (2 pg.)</p>
<p>3 "Dual-Polarity Tracking Regulators" (SG1501, SG1501A, SG1502, SG1568) Operating parameters and circuit configurations for the 1501, 1501A, 1502 and 1568 regulators. Voltage adjustments are described, including the use as $-12, 6$ v power source for 710 and 711 comparators. Silicon General Linear IC Product Guide (4 pg.)</p>	<p>8 "Understanding and Applying the Analog Switch" (IH5001, IH5009, IH5025, IH5040) Compares parameters of analog switches. Applications of several switch families are discussed, including 3-channel differential multiplexer, gain programmable amplifier, gain ranging circuit, sample and hold circuit. Intersil Application Bulletin A003 (16 pg.)</p>
<p>4 "723/823 Voltage Regulators" (723, 823) Discusses characteristic device parameters, bias limitations, improvement of ripple rejection, external voltage sensing, thermal effects, protection, limiting and increasing the output current. Applications: switching regulator, tracking regulator, current sinking power supplies, precision current source, light intensity control, phase shift oscillator. Teledyne Semiconductor Linear Application Note 2 (17 pg.)</p>	<p>9 "The MISER - A Monolithic Integrated Stored Energy Regulator" (LP1000) Describes the operation of this 3 terminal, low voltage, threshold detector and switch. Emphasizes capacitor charging circuits with slow charge, rapid discharge characteristics. Applications: LED flasher, tone generator, relaxation oscillator. Lithic Systems Application Note LAN-101 (3 pg.)</p>
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<p>Switches</p>	<p>10 "High-Speed MOS Commutators" (MM451, MM453, MH454) Discusses the lowered threshold voltages in commutators, on and off resistances, switching speed, noise and high-frequency noise control. National Linear Applications AN-28 (8 pg.)</p>
<p>5 "Applications of the $\mu\text{A}742$ TRIGAC -- A Zero Crossing AC Trigger" ($\mu\text{A}742$) Describes this TRIGAC circuit. Includes a discussion of the transfer characteristics and performance plus operation from ac and dc supplies. Applications: 110 V ac single threshold control; single phase, 110 V ac dual threshold control with hysteresis; 110 V ac dual threshold control with time proportioning; with time proportioning for Y or Δ loads; operating with transformer isolation between control circuit and ac line; output pulse amplifier with transformer; output pulse inverter; period extender for time proportioning; initial cycle delay; sensor failure detection circuit; time delay "relay" circuit; 208 V ac dual threshold control 110 V ac, 400 Hz dual threshold control with single TRIGAC for Y loads. Also includes a section listing parts and component location diagrams for these applications and discusses operation with a fixed dc supply. Covers use of the TRIGAC with nonresistive loads, discusses thyristor cells, and full wave output power switches for use with the device. Fairchild (30 pg.)</p>	<p>11 "Applications of MOS Analog Switches" (LH0014, LH0019) Discusses basic commutation circuits and describes the use of the LH0014 and LH0019 in linear amplifier applications, including reset functions and chopper circuits. Covers use of MOS switches as suppressed carrier double-sideband modulators and double-sideband demodulators. Also describes a circuit for a phase-locked loop AM-FM detector without tuned circuits. National Linear Applications, also Interface Handbook AN-38 (8 pg.)</p>
<p>12 "Analog-Signal Commutation" (MM450, MM451, MM454, MM550, MM551, MM552) Describes dc characteristics involved in MOS IC switching of analog signals when the signal input range varies between ± 10 v. National Linear Applications and also Interface Handbooks, AN-33 (6 pg.)</p>	<p>13 "High Speed Analog Switches" (AM1000, AM1001, AM1002) Discusses time domain multiplexing, current mode multiplexing, the switching characteristics of the AM1000 J-FET switches, and drive circuits. National Interface Handbook, AN-53 (6 pg.)</p>

Bold face indicates additional data is provided, see the Product Index.

LINEAR

Switches (cont)	Switches (cont)
<p>1 "PIN Diode Drivers" (DH0035, DH0035C) Describes PIN diode switching requirements and application of DH0035 as a driver. Includes discussion of anode ground and cathode ground designs and of repetition rate considerations. National Linear Applications, also Interface Handbook AN-49 (6 pg.)</p>	<p>8 "FETs as Analog Switches" General discussion of FET operation; detailed discussion of factors affecting switch performance, including specific load problems and applicable driver circuits. Siliconix Application Note AN72-2 (12 pg.)</p>
<p>2 "Applications of the RCA-CA3062 IC Photo-Detector and Power Amplifier in Switching Circuits" (CA3062) Describes circuit operation and application in a latched memory circuit, a light activated triac control, a triac control with automatic shut off and alarm, and a triac intrusion alarm system. RCA SSD-202 Linear Application Notes Databook ICAN-6538 (6 pg.)</p>	<p>9 "Analog Switches in Sample and Hold Circuits" Covers the effects of FET analog switch current handling capability on settling time and the effects of offset characteristics on sample and hold system accuracy. Describes inverting and non-inverting sample and hold circuits. Siliconix Application Note AN74-2 (4 pg.)</p>
<p>3 "Features and Applications of RCA IC Zero-Voltage Switches" (CA3058, CA3059, CA3079) Discusses zero-voltage switch operation in general. Operation primarily with thyristors in ac power control and switching applications, including electric heating, oven/broiler control, machine control, light control and industrial systems. RCA SSD-202 Linear Application Notes Databook, ICAN-6182 (28 pg.)</p>	<p>10 "Driving the JFET Switch" (DG126, DG139) Circuit operation of the DG126L and DG139L series driver-switches. Siliconix Application Note AN69-1 (4 pg.)</p>
<p>4 "Some Applications of a Programmable Power Switch/Amplifier" See listing under Power Control. (RCA)</p>	<p>11 "D129/132 Quad Decode Driver" (D129, D132) Describes basic level shifting uses including MOS switch, gas tube and lamp drive applications. Siliconix Application Tip (4 pg.)</p>
<p>5 "CMOS Analog Switches-A Powerful Design Tool" Describes CMOS switch construction, characteristics and operating precautions. Applications include: a four channel switch to multiplex a scope input, a low pass filter with digitally controlled frequency response, an amplifier with programmable inputs and gain, a sample and hold circuit, a latching switch, high frequency switching and multiplexer systems. Siliconix Application Note AN75-1 (16 pg.)</p>	<p>12 "Designing with Monolithic FET Switches" Describes MOSFET and JFET switch operation, plus driver considerations. Siliconix Technical Article TA73-2 (4 pg.)</p>
<p>6 "Switching High-Frequency Signals with FET Integrated Circuits" (DG133, DG171, DG181, DG200) Discussion of DG133/171/181/200 as rf switches. Gives equivalent circuits, "Off" isolation and "On" performance data. Applications: control of video monitor and switching between two video cameras. Siliconix Application Note AN73-3 (16 pg.)</p>	<p>13 "Modes of Actuation for Type ULN-3006 'Hall Effect' Switches" (ULN-3006) Describes magnetic operation of this non-contact, switching device. Sprague Electric Application Note 27404.1 (4 pg.)</p>
<p>7 "Driver Circuits for the JFET Analog Switch" Discussion and comparison of resistor-coupled diode charge transfer, space transistor charge transfer, and switched resistor driver circuits for JFET switches. Siliconix Application Note AN73-5 (12 pg.)</p>	<p>14 "Suggested Output Loads for Type ULN-3006 'Hall Effect' Switches" (ULN-3006) Diagrams connections to use the open collector output to drive transistors, thyristors, TTL and MOS circuits. Sprague Electric Application Note 27404.2 (2 pg.)</p>
	<p>Thermal Considerations</p>
	<p>15 "Thermal Evaluation of Integrated Circuits" Describes four methods for thermal evaluation, including reverse biasing substrate diodes. Fairchild Application Note 205 (8 pg.)</p>
	<p>16 "Transient Thermal Resistance -- General Data and Its Use" Discusses transient thermal resistance and its use and describes methods using various degrees of approximations to determine the junction temperature rise of a device. Also covers the concept of a duty cycle family of curves to simplify calculation of junction temperature rise under a repetitive pulse train. Motorola AN-569 (15 pg.)</p>

LINEAR

Thermal Considerations (cont)

- 1 **"Mounting Techniques For Metal Packaged Power Semiconductors"**
Discusses preparation of mounting surfaces, using thermal compounds, and fastening techniques. Gives typical interface thermal resistance for a number of packages. Motorola AN-599 (5 pg.)
- 2 **"Mounting Procedure For, And Thermal Aspects Of, Thermopad Plastic Power Devices"**
Covers various methods of mounting and heat-sinking Motorola case number 77, 90, and 199 plastic power devices. Also discusses thermal resistance considerations, lead forming, and circuit board cleaning. Motorola AN-290B (9 pg.)
- 3 **"Micropower Thermometer"**
See listing under Transducers. (National)
- 4 **"Thermal Resistance of Integrated Circuit Packages"**
Describes method of measuring package thermal resistance while package is immersed in constant-temperature, circulating oil bath that acts as an infinite heat sink. Sprague Electric TP 72-7 (5 pg.)
- 5 **"Thermal Design for Plastic Integrated Circuits"**
(ULN-2277)
Discussion of chip power dissipation -- using amplifier as an example -- heat dissipation, ULN-2277 dual 2-watt audio power heat sinks, heat sink finishes, and forced air cooling. Sprague Electric TP 74-1 (7 pg.)
- 6 **"New Heat Sinking Techniques for Hermetic DIPs"**
Describes use of stamped and extruded heat sinks and method of reversing IC die and bonding chip directly to Kovar base. Sprague Electric TP 74-4 (4 pg.)

Timers

- 7 **"Single-Chip Frequency Synthesizer Employing the XR2240"**
(XR2240)
Describes use of this timer/counter as a single-chip frequency synthesizer: $f_o = f_r / (m/n + 1)$ where $f_o < 200\text{kHz}$. Describes generating 100 Hz synchronized to 60 Hz line. Exar Integrated Systems TB-1003 (3 pg.)
- 8 **"Versatile Timer Operates From Microseconds to Hours"**
(LM122)
Describes the LM122 circuit and its operation. Includes discussion of pin functions, timing errors and noisy environments. Discusses use as various timers, as a pulse width detector, a comparator, an oscillator, a two-terminal time delay switch, and a frequency to voltage converter. National AN-97 (12 pg.)

Timers (cont)

- 9 **"Timers"**
(NE555, NE556, SE555, SE556)
Describes monostable operation of timers and discusses application as a missing pulse detector, frequency divider, pulse width modulator, pulse position modulator, test sequencer, and a tone burst generator. Circuits are shown for a touch control, burglar alarm, photographic timer, speed warning device, switching regulator, washer timer and an automobile burglar alarm. Signetics Applications Handbook (13 pg.)

Transducers

- 10 **"Micropower Thermometer"**
(LX5600)
Describes use of the LX5600 as a thermometer whose output is a current proportional to temperature and can drive a meter for direct readout. National Linear Brief-27 or Transducer Handbook TB-11 (2 pg.)
- 11 **"Pressure Transducers as Accelerometers"**
(LX1700G)
Discusses uses of accelerometers and describes scheme of converting LX series pressure transducers to cover ranges from fractions to thousands of g's. National Transducer Handbook AN-96 (4 pg.)
- 12 **"LX Series Pressure Transducers: Design and Applications Information"**
(LX1600A, LX1601A, LX1602A)
Describes hybrid transducer circuit and applications, including pressure to frequency converter, latching altitude detector, digital readout barometer and altimeter. National AN-94 (8 pg.)
- 13 **"Pressure Transducer Load Cell"**
(LX1700G)
Describes use of LX1700G pressure transducer to measure weight. National Transducer Handbook AN-95 (4 pg.)
- 14 **"The LX1602A Pressure Transducer and Altimeter Applications"**
(LX1602A)
Describes how to use this transducer along with additional electronics to build an altimeter that operates over a range of -1,000 feet to +50,000 feet. National AN-91 (3 pg.)
- 15 **"Transducers in Fluid Flow Applications"**
(LX1602A)
Discusses application of LX1602A in pressure vessel, open flow and closed flow applications. National Transducer Handbook AN-93 (8 pg.)
- 16 **"Transducer Sensor Diaphragm 15 Million Cycle Life Test"**
Findings in the continuing test of National's transducer sensing elements—a silicon membrane approx. 1 mil thick. National Transducer Brief 3 (1 pg.)

LINEAR

Transducers (cont)

- 1 **"Use of the SK1007 Pressure Transducer Kit in Vault Alarm Systems"**
Describes application of this multi-level switch kit with a pressure transducer in vault alarm systems.
National Transducer Brief 7 (2 pg.)

- 2 **"Transducer Fluid Filled Option"**
Describes the "Fluid-Filled" methods of protecting transducers from hostile environments. Rates the resistance of silicone rubber to some common fluids.
National Transducer Brief 8 (2 pg.)

- 3 **"Installation Ideas for Pressure Transducers"**
(LX1600, LX1700, LX1400, LX1701AR, LX3700)
Provides suggestions for mounting National transducers for various applications. Includes diagrams and typical mounting configurations.
National Transducer Handbook AN-92 (4 pg.)

- 4 **"Zeroing Transducer Output Voltage"**
(LX1600 Series)
Shows how to set the supply voltages to provide an output starting at 0v.
National Transducer Handbook TB-2 (2 pg.)

- 5 **"Externally Zeroing Transducer Output Voltage"**
(LX1603G, LX1604G)
Describes how to use external components to zero the transducer output voltage. Tables compare output of the LX1603G and LX1604G devices.
National Transducer Handbook TB-5 (2 pgs.)

- 6 **"Automatic Zeroing Circuit"**
Diagrams an auto-zeroing system and describes its operation. Lists specifications and sensitivity.
National Transducer Handbook TB-12 (1 pg.)

- 7 **"Pressure to Current Converter (3 Wire)"**
(LX Series)
Describes the use of any LX series pressure transducer to obtain a pressure to current translator.
National Transducer Handbook TB-4 (2 pg.)

- 8 **"Current Sourcing and Sinking"**
(LX Series)
Offers a method that utilizes any LX()02() 0 to 15 psi transducer that sinks a standard 4 to 20 mA output (1:5 range) for a 3 to 15 psi pressure input (ratio 1:5 range)
National Transducer Handbook TB-15 (1 pg.)

- 9 **"Pressure to Frequency Converter"**
Shows how to take advantage of the hybrid construction of a pressure transducer and how to construct a self-contained voltage controlled oscillator.
National Transducer Handbook TB-13 (1 pg.)

Transducers (cont)

- 10 **"The Multi-Level Switch Kit, Part No. SK1007"**
Details the use of any LX series pressure transducer to produce a high level analog output as well as three independent switch points.
National Transducer Handbook TB-1 (2 pgs.)

- 11 **"Flow Velocity Measurement by Analog Shaping"**
(LX Series)
Discusses using an LX series pressure transducer to determine a fluid's flow velocity by extracting the square root of the transducer's analog voltage output.
National Transducer Handbook TB-20 (1 pg.)

- 12 **"Latching Altitude Detector"**
(LX1602A)
Uses the LX1602A absolute pressure transducer to construct an altitude detector that latches on when a given pressure is exceeded.
National Transducer Handbook TB-17 (1 pg.)

- 13 **"Solid State Barometers"**
(LX3700 Series)
Describes how to use thermostatically controlled pressure transducers as barometers with readout in inches of mercury, TORR or millibars.
National Transducer Handbook TB-21 (2 pg.)

- 14 **"Thermometer Using Pressure Transducers"**
(LX3700 Series)
Describes how to use a pressure transducer, to construct a constant volume gas, or "hot bulb", thermometer as an alternative to conventional electronic thermometers.
National Transducer Handbook TB-18 (2 pg.)

- 15 **"Acoustic Applications of Pressure Transducers"**
(LX Series)
Describes use of an LX series transducer as a microphone and sound pressure level meter, and the advantages over ordinary cardioid types.
National Transducer Handbook TB-19 (2 pg.)

- 16 **"Pressurized-Cable Fault Detection and Location"**
(LX1603A)
Describes the use of transducers in pressurized-cable control systems as early warning and break location alarms.
National Transducer Handbook AN-121 (3 pg.)

- 17 **"Medical Applications"**
Describes the use of Pressure Transducers for protecting electronic equipment and operators; constructing blood pressure monitoring systems, respirators, kidney dialysis machines and other medical related applications.
National Transducer Handbook AN-122 (3 pg.)

LINEAR, MEMORY

Transducers (cont)	Interface
<p>1 "Automotive Applications" Describes the use of pressure transducers in automotive electronics for fuel metering, ignition management and other applications. National Transducer Handbook AN-120 (4 pg.)</p>	<p>CAMs</p>
<p>2 "Calibrating the LX5600" (LX5600) Discusses the accuracy of the LX5600 temperature transducer as well as three types of error—offset, slope and linearity. National Transducer Handbook TB-9 (1 pg.)</p>	<p>8 "Content Addressable Memory Element (CAM)" (N8220) Discussion of CAMs; logic diagram, functional description of 8220; applications including information retrieval, learning memory, masked searches, and search for maximum or minimum values. Signetics Applications Handbook (8 pg.)</p>
<p>3 "IC Transducers Simplify Temperature Control Circuits" (LX5600) Describes the advantages of this temperature transducer device in on/off temperature control applications. Also discusses construction of a temperature controller. National Transducer Handbook TB-10 (3 pg.)</p>	<p>Character Generators</p>
<p>4 "A New Interfacing Concept; The Monolithic Temperature Transducer" (LX5600, LX5700) Covers alternate methods of powering the LX5600, load isolation and an unusual active thermal shield (the shield tracks the surface temperature of the sensor.) Describes use as a thermal transducer, temperature to frequency converter, and a temperature controller with rate-of-change sensing. Discusses use of differential temperature measurements for liquid or moving air detection (including wind) and for position sensing (using a heat source as a position reference.) National AN-132 (10 pg.)</p>	<p>9 "A CRT Display System Using NMOS Memories" (MC6565, MCM6570, MCM6571) Discusses basic crt operation, character formation and describes the 8K-bit MCM6570 character generators. Describes a 128-character system in detail, including counter and retrace control, memory select, and address register sections. Motorola AN-706A (15 pg.)</p>
<p>5 "Manual Control With Load Cells" Advocates the use of pressure transducers in force actuated controls for a better man-machine interface. National Transducer Handbook TB-16 (1 pg.)</p>	<p>10 "American and European Fonts In Standard Character Generators" (MM4240, MM5240, MM4241, MM5241) Depicts the standard 64 character subsets for these devices. National MOS Handbook AN-57 (6 pg.)</p>
<p>MEMORY</p>	<p>11 "The Systems Approach to Character Generators" See listing under ROMs. (National)</p>
<p>Analog</p>	<p>12 "Digital Display Generators" Using TTL compatible MOS ROMs to generate displays. Gives circuit diagrams and a sample readout. National MOS Brief 8 (2 pg.)</p>
<p>6 "Principles of Analog Discrete-Time Signal Processing Devices" (SAD, SAM, SAP, TAD) Describes a family of devices that effectively sample and store analog signals, quantizing time but retaining analog signal values. Different readout sequences result in processing the stored signals. Covers use as fixed and variable time delay, filters, correlation, convolution, time base modification, and video time base correction. Reticon Application Note 102 (17 pg.)</p>	<p>13 "7 X 9 Display Character Generator" Uses three MOS ROMs and some TTL logic to create a font of 64 7X 9 dot-type characters. A circuit diagram and a suggested character forms are provided. National MOS Brief 13 (2 pg.)</p>
<p>7 "Applications of Reticon TAD-12 Tapped Analog Delay" (TAD-12) Describes the use of this clock controlled analog delay line in low pass and bandpass filter applications. Includes mathematical discussion of second order filter design. Briefly covers correlation and pattern recognition. Reticon Application Note 103 (9 pg.)</p>	<p>Interface</p>
	<p>14 "The Recovery of Recorded Digital Information in Drum, Disk and Tape Systems" Reviews methods for converting the analog signal obtained from a magnetic recording into digital format. Motorola Application Note AN-711 (10 pg.)</p>
	<p>15 "Applying Modern Clock Drivers to MOS Memories" (DS0025, DS0026) Covers use of 0025/26 drivers in MOS memory systems. Information includes selection of packages and heat sinks, power dissipation, rise and fall time, power supply decoupling, system clock line ringing and crosstalk, input coupling techniques, and sample calculations. National MOS Handbook AN-76 (12 pg.)</p>

Bold face indicates additional data is provided on the page noted.

MEMORY

Interface (cont)

- 1 **"Interfacing Circuits for MOS Dynamic Random Access Memories"**
Discusses interfacing methods employing level shifters (TTL to MOS levels) with boosters, level shifters (MOS to TTL levels), and sense amplifiers.
Nortec Applications Note No. 25 Rev. A (3 pg.)
- 2 **"Charge Pump Driver for 7001 RAMs"**
(SN75450B)
Defines a method for driving the charge storage pump input of a 7001 RAM. Provides a description of the basic storage pump RAM cell and the charge pump circuit diagram. Gives performance curves.
Texas Instruments Application Report CA-178 (6 pg.)
- 3 **"High Speed TTL Interfacing for 7001 Static RAMs"**
(SN75261, SN75365)
Illustrates interface techniques for driving the 7001 RAM chip-select input, and sensing the memory output.
Texas Instruments Application Report CA-179 (8 pg.)

Microprogramming

- 4 **"Tri-State Logic in High-Speed Memories of Microprogrammed Computers"**
See listing under (Digital) TTL, General. (National)
- 5 **"Design of Microprogrammable Systems"**
Discusses building a simple system using read only storage (ROS). Gives example of the arithmetic unit of a System 360, reviews terminology, covers ROS addressing techniques and microinstruction word encoding, and writeable control storage.
Signetics Application Handbook pg. 5-24 (14 pg.)
- 6 **"Microprogramming and System Applications for Read Only Storage"**
Discusses fundamentals and advantages of microprogramming and applications of ROS in table look up, pattern generation, program storage, and microprogrammable devices (acting as control memories to control function of logic networks.)
Signetics Applications Handbook pg. 5-38 (7 pg.)
- 7 **"Cache Type Scratchpad Approach Improves CPU Throughput"**
Presents diagram with 4K by 32 main memory, ALU with 32 x 2 scratchpad, 32 x 12 CAM, and microprogrammed control.
Signetics Applications Handbook pg. 5-45 (2 pg.)
- 8 **"Economic Advantages of Microprogramming"**
Describes advantages, costs, and savings of microprogramming.
Signetics Applications Handbook pg. 5-19 (5 pg.)

PROMs

- 9 **"HPROM-0512 Bipolar PROM"**
(HPROM0512)
Covers basic programming considerations, automatic and custom programming of this 64-word by 8-bit memory.
Harris Application Note 202 (8 pg.)
- 10 **"Programming the HPROM-0512 In An Expanded Configuration"**
(HPROM0512)
Describes normal and expanded bit/word programming with sample calculations for a 256-word system. Describes programming expanded ROMs installed in a logic system.
Harris Application Note 203 (4 pg.)
- 11 **"Designing with Intel PROMs and ROMs"**
(1302, 1602A, 1702A, 3301A, 3404A, 3322, 3324A, 3601, 3604, 3622, 3624)
Describes technologies used to build PROMs, nichrome problems and advantages of polysilicon. Covers operation and use of Intels ROMs, PROMs and U. V. erasable PROMs.
Intel Application Note AP-6 (18 pg.)
- 12 **"Use of Bipolar ROM and PROMs"**
See listing under ROMs (Monolithic Memories)
- 13 **"ROM in Sequential & Combinatorial Logic"**
(6300, 6330)
Discusses combinatorial and sequential logic functions. Covers use of PROMs as synchronous counters, multiphase clock generators, character generators, octal decoders, parity generators, multiplexers, D/A converters, scalars, and 4-bit comparators.
Monolithic Memories Application Note 102 (8 pg.)
- 14 **"Programming the MCM5003/5004 Programmable Read Only Memory"**
(MCM5003, MCM5004)
Discusses programming methods for this 64 x 8 bit memory, describes circuit and operation. Describes a simple programmer using five ICs and a more sophisticated version using 25 ICs offering automatic sequencing.
Motorola AN-550 (12 pg.)

RAMs

- 15 **"AMS7001 Basic Storage Module High Speed Memories"**
(AMS7001)
Discusses AMS7001 storage module operation, backplane wiring, addressing scheme, and power requirements.
Advanced Memory Systems Application Note 35 (18 pg.)
- 16 **"Using the TM-200 Semiconductor Memory Card"**
(AMS7001)
Describes this memory card using the AMS7001 RAM. Includes detailed diagrams.
Advanced Memory Systems Application Note 36 (22 pg.)

MEMORY—

RAMs (cont)	RAMs (cont)
<p>1 "The Am9338 Multiple Port Memory" (9338) Describes applications for this 8-word by 1-bit three-address memory, including the working store for high-speed, three address computers; first in, first out (asynchronous buffer) memory; and direct address/indirect address memory. Advanced Micro Devices Data Book, Catalog (4 pg.)</p>	<p>9 "Understanding the FIFO" (3351) Covers 3351 FIFO operation, cascading, plus use in data rate buffering, parallel operation, and burst operation. Fairchild APP 332 (8 pg.)</p>
<p>2 "Designing with 1103 Memories" (S1103) Discusses 1103 RAM timing requirements, voltage limits and the effects of noise on refresh time. American Microsystems AP75-9 (5 pg.)</p>	<p>10 "Designing High Speed, Low Cost Memory Systems with the Intel 2105" (2105, 3210, 3211, 3207A) Describes the 2105 operation, driving and sensing the unit plus power supply, voltage distribution, and decoupling considerations. Intel Application Note (23 pg.)</p>
<p>3 "Dynamic RAMs are Easy and Economical" (S4006) Compares 1024 bit dynamic RAMs with static ones. Describes how to apply and to test the S4006. American Microsystems AP75-8 (14 pg.)</p>	<p>11 "Memory System Design with the Intel 2107B 4K RAM" (2107B, 3210, 3225) Describes the operation and performance of the 2107B and memory systems considerations such as drivers, buffers, timing, layout, decoupling, debugging and power calculations. Intel Application Note AP-10 (36 pg.)</p>
<p>4 "Testing Dynamic RAMs" (S146, S1103) Describes test procedures used for the AMI 1103 series RAMs. American Microsystems AP75-11 (8 pg.)</p>	<p>12 "Designing Non-Volatile Memory Systems with Intel's 5101 RAM" (5101) Describes internal circuits and operation of the RAM. Outlines circuit techniques for battery supported non-volatile operation. Describes use of the device with the MCS-40 microcomputer. Intel Application Note AP-12 (28 pg.)</p>
<p>5 "Application of First-In First-Out Memories" (Am2812, Am2813, Am2841, 3341) Describes the function of a first-in first-out memory, methods of constructing FIFO buffers and the operation of the above P-channel MOS devices. Discusses storage and control, expansion methods, interfacing, and applications in an N-bit shift register and as a key encoder on key matrix. Advanced Micro Devices Data Book, (9 pg.)</p>	<p>13 "Which Way for 4K - 16, 18 OR 22 PIN?" Describes trade-offs in building 16, 18 and 22 pin 4K RAMs. Intel Application Brief AP-11 (9 pg.)</p>
<p>6 "Micro Power Operation of Static RAMs" (1212, 1217, 1218, 1220, 1221) Covers the operation of these NMOS memories in a pulsed power mode with the resultant power savings. EMM Applications Note APL-N-200 (4 pg.)</p>	<p>14 "Designing with Intel's Static MOS RAMs" (2101, 2102A, 2111, 2112, 5101) Outlines internal operation of these static RAMs. Describes how they are used and covers design considerations. Intel Application Note AP-8 (19 pg.)</p>
<p>7 "93400 TTL Random Access Memories For High-Speed Applications" (7481, 7489) Summarizes the uses for the 7481/93403 (general purpose); 7489/93407, 93433, and 93435 (highest speed); and 93400 (lower-cost, medium-to high speed). Discusses application in memory systems. Fairchild Application Note 219 (9 pg.)</p>	<p>15 "Designing Memory Systems With the Intel 2107A 4K RAM" (2107A) Describes the application of this 4096x1 RAM. Includes driving, sensing and power considerations. Intel Application Note AP4 (16 pg.)</p>
<p>8 "TTL/MSI 9334 8-Bit Addressable Latch" (9334) Describes operation and applications, including 16 and 32-bit addressable latches, 16-word by 4-bit memory, demultiplexer and decoder, 8-bit A/D converter and a 16-bit serial-to parallel converter. Fairchild Application Note 220 (8 pg.)</p>	<p>16 "Design and Application of Intel's 2416 16K Charge Coupled Device" (2416) Describes the internal organization and operation of this 16, 384x1 device. Covers application in memory systems including driver and control circuits as well as use on a megabit storage card. Intel Application Note AP-14 (39 pg.)</p> <p>17 "CMOS RAMs" (IM6508, IM6523, IM6524) Provides a block diagram and describes the operation and interface requirements for these 256x1 and 1024x1 CMOS RAMs. Intersil Application Bulletin M002 (8 pg.)</p>

Bold face indicates additional data is provided, see the Product Index.

MEMORY—

RAMs (cont)	RAMs (cont)
<p>1 "12/16K Memory System for the MK5065 Microprocessor" See listing under Microprocessors Systems (Mostek)</p>	<p>10 "MOS Scratch Pad/Content Addressable Memory System" Describes a 64-bit Scratch Pad/Content Addressable Memory using MOS devices. Includes circuit diagrams and discusses circuit operations. National MOS Brief 11 (2 pg.)</p>
<p>2 "Considerations for Designing a High Density, Low Power Memory System" (MK4200) Describes a 16Kx8 memory array using the MK4200 4K RAM and CMOS logic. Mostek (3 pg.)</p>	<p>11 "A Method of Implementing Stacks With Existing Minicomputer Memory" Gives detailed description of a controller for a stack of programmable size up to 256 words for a 16-bit minicomputer with less than 16 k of memory. Tells how stack size can be increased to 4096 words by adding ten ICs. National AN-60 (4 pg.)</p>
<p>3 "MK4096 Application Information" (MK4096) Describes the MK4096 operation, shows details necessary for system design, describes interface with PDP-11 processor. Mostek (8 pg.)</p>	<p>12 "Designing Memory Systems Using the MM5262" (MM4262, MM5262) Provides a detailed description of this 2048x1 PMOS dynamic RAM, operating instructions, and a diagram of a 16K x 10 memory using the device. National AN-144 (14 pg.)</p>
<p>4 "The Design of an N-Channel 16K x 16 Bit Memory System for the PDP-11" (MCM6605, MC3450, MC3452, MC3459, MC3460) Briefly describes operation of the MCM6605 NMOS RAM, the details the design of a PDP-11 add-on mainframe memory using this device. The interface ICs and system performance are also discussed. Motorola AN-740 (15 pg.)</p>	<p>13 "A Simple Power Saving Technique for the MM5262 2k RAM" (MM5262) Describes method for decoding the clocks of unselected chips in a memory array to save power. Discusses application in 8k x 16 memory. National MOS Handbook AN-86 (4 pg.)</p>
<p>5 "Semiconductor for Plated Wire Memories" See listing under (Digital) Interface. (Motorola)</p>	<p>14 "Memory Systems Built with the Nortec 6002" (6002) Describes circuits for the bit driver/sense amplifier required to interface the 6002 with TTL. Discusses external support circuit parameters and internal circuit operations that affect system performance. Nortec Applications Note No. 28 (4 pg.)</p>
<p>6 "MTTL Designer's Note—The MC4004/MC4005, A 16-Bit Random Access Memory" (MC4004, MC4005) Discusses operation of this memory including typical read-write sequences, plus typical dc and switching characteristics as a function of temperature, power supply, and output load. Also gives examples of high-speed, non-destructive readout memory systems using this 16-bit memory as the basic cell. Motorola AN-464 (10 pg.)</p>	<p>15 "Memory Systems Built with the Nortec 6002" (6002) Describes use of this 1024-bit RAM in building a general purpose memory module with 425,984 bit capacity. Nortec Applications Note No. 30 (14 pg.)</p>
<p>7 "A High Speed FIFO Memory Using the MECL MC10143 Register File" See listing under (Digital) High Speed Logic (Motorola)</p>	<p>16 "Printed Circuit Layout Considerations for Dynamic Memory Arrays" Gives P.C. layout guidelines for MOS dynamic memories (also applicable to standard TTL circuits.) Nortec Applications Note No. 31 (2 pg.)</p>
<p>8 "A Non-volatile Microprocessor Memory Using 4K N-channel MOS RAMs" (MCM6605, MC6800) Describes the design of a 9192-byte non-volatile memory using the MCM6605 4K x 1 RAM and CMOS control logic to reduce the power requirement in the standby mode. Motorola Application Note AN-732A (17 pg.)</p>	
<p>9 "Using Tri State™ Logic For 'Rubber Band' Memories" Describes the construction and use of scratch/pad memories to store data at a rapid rate and then release it as required. They serve as buffers between systems operating at different clock rates. National Applications Report AN68 (4 pg.)</p>	

MEMORY

RAMs (cont)	ROMs (cont)
<p>1 "Designing Memory Systems with the Nortec 6003 RAM" (6003) Describes operation of this 2048-bit RAM, including a discussion of memory timing, refresh control, array control signals, device output sensing, and array driver circuits. Nortec Applications Note No. 32 (9 pg.)</p>	<p>9 "ROM in Sequential and Combinatorial Logic" See listing under PROMs (Monolithic Memories)</p>
<p>2 "Applications Information for the RCA MW7001D RAM" (MW7001D) Discusses operation of the RAM's charge pump, input loading and recommended interface circuits. RCA ICAN-6401 (5 pg.)</p>	<p>10 "Applications of the 93434 Read Only Memory" (93434, 7488) Describes features of this 32 x 8 memory. Discusses applications in memory systems and use as a decoder, and as a character generator for a 5 x 8 dot matrix. Fairchild Application Note 168/1 (6 pg.)</p>
<p>3 "Memory Systems Characteristics and Applications for the CD4061A" (CD4061A) Describes basic device operation, application in memory systems, and testing including construction of an all CMOS memory tester. RCA ICAN-6445</p>	<p>11 "Monolithic Diode Matrices" Describes programming and use of diode matrices. Applications: teletypewriter coding matrix, decimal decode for displays, nines complement-BCD, shift register matrices, and ROMs. Harris Application Note 206 (16 pg.)</p>
<p>4 "1024-Bit Static Memory" (2602) Discusses support circuitry for the 2602 RAM. Also covers power requirements, chip select gating, write operations, waveforms, and the basic memory cell. Signetics Applications Handbook (4 pg.)</p>	<p>12 "Use of Bipolar ROM And PROMs" (6225, 6240, 6260, 6300, 6335) Describes applications including code converters, emulators, transducer error correctors, submarine identifiers, paper tape interpreters. Also BCD adders, multipliers, character generators, binary dividers, vector generators, voice synthesizers, microprogrammed timing generators, and sequence controllers. Monolithic Memories Application Note 110 (10 pg.)</p>
<p>5 "A High Speed Read-While-Write RAM" (N82S21) Describes operation of the 82S21. Covers use as buffer register in an accumulator section, and in a 32 word by 2 byte memory with byte parity maintained. Signetics Applications Handbook pg.5-15 (4 pg.)</p>	<p>13 "MCS2026-002" (MCS2026-002) Describes connections to use this demonstrator version of the 16K (2048x8) dynamic ROM, which can be used as an adder, counter, encoder, decoder or shift register. MOS Technology Application Note MCS2026-002 (8 pg.)</p>
<p>6 "256 Bit Bipolar Random Access Storage Applications" (N82S06, N82S07) General discussion of the use of Bipolar memory including peripheral, terminal and main memory applications, memory protection, memory maps and virtual memory. Briefly describes use of 82S06/7 in 256 x 8 and 16394 x 1 memories. Signetics Applications Handbook (6 pg.)</p>	<p>14 "Code Conversion With Semiconductor Read Only Memories" (MCM4000) Describes methods for converting data from binary to BCD and vice versa, from the Hollerith to the common 8-bit codes, and from one 8-bit code to another. Motorola AN-506 (13 pg.)</p>
<p>7 "Driving the TMS4030 RAM using the SN75363 or SN75322" (SN75322, SN7536, TMS4030) Driving the TMS4030 chip enable clock with these ICs, switching speeds versus system size, general performance characteristics and performance comparisons are provided. Texas Instruments Application Report CA-181 (7 pg.)</p>	<p>15 "Replacing Sequential Logic with ROMs" Describes design methods for using ROMs to replace sequential logic, that is to replace designs that would require random or combinational logic with feedback loops. Motorola Application Note AN-722 (19 pg.)</p>
<p>ROMs</p>	<p>16 "Saving ROMs in High-Resolution Dot-Matrix Displays and Printers" (MM5232, MM5240, MM5241, DM8596, MM8597) Describes two-stage, column-generation approach called "intermediate coding" that saves more than 25% of ROM capacity when several ROMs are needed to store a font. National MOS Handbook AN-85 (8 pg.)</p>
<p>8 "Designing with Intel PROMs and ROMs" See listing under PROMs (Intel)</p>	

Bold face indicates additional data is provided, see the Product Index.

MEMORY

ROMs (cont)

- 1 **"The Application of ROMs"**
(MM5203, MM5230, MM5232, MM5240)
Describes applications of read only memories in table look up, code conversion and generation, character generation, random logic generation, and microprogramming. National AN-61 (12 pg.)
- 2 **"Custom ROM Programming"**
Gives forms for submitting truth tables for various National read only memories. National MOS Handbook AN-100 (8 pg.)
- 3 **"The Systems Approach to Character Generators"**
(MM5240, MM5241)
Discusses use of MM5240 and MM5241 ROMs in character generation. Includes discussion of CRT raster scan displays, refresh memory modulation, control logic, bipolar compatibility, printing applications, and raster scan systems. National MOS Handbook AN-40 (12 pg.)
- 4 **"Trig Function Generators"**
Instead of simply cascading ROM to increase resolution and accuracy of the look-up tables, this note describes interpolation techniques to increase trig function accuracy with less memory. National MOS Handbook, MOS Brief 10 (2 pg.)
- 5 **"MOS Goes Bipolar"**
See listing under Shift Registers (National)
- 6 **"Read-Only Memory"**
(2526)
Discusses input and output circuits of the 2526 static 5,184-bit ROM. Covers address decoding, timing, memory organization, and organization for use as a character generator. Signetics Applications Handbook (4 pg.)
- 7 **"Fast Multipliers Using TTL Read Only Memories"**
(SN74182, SN74H183, SN74283, SN74284, SN74285)
Reviews fundamental algorithm of binary multiplication. Shows use of ROMs for multiplication, two's complement multiplication, and truncated multiplications. Texas Instruments Application Report CA-172 (11 pg.)

Shift Registers

- 8 **"A Random Pattern Generator for Testing Digital Delay Elements"**
Describes the use of a linear feedback shift register for digital testing. Advanced Micro Devices Data Book (3 pg.)
- 9 **"Applications of Dynamic Shift Registers"**
(1402A, 1403A, 1404A, 1405A, Am2802, Am2803, Am2804, Am2805, Am2806, Am2807, Am2808)
Discusses dynamic shift register storage in general, clock timing, circuits for clock drivers, interfacing with TTL, and recirculating registers. Advanced Micro Devices Data Book, (7 pg.)

Shift Registers (cont)

- 10 **"Schottky TTL MSI Registers"**
(AM25S07, AM25S08, AM25S09, SN54S174, SN54S175, SN54S194, SN54S195, SN74S174, SN74S175, SN74S194, SN74S195)
Describes these 4 and 6-bit registers, their operation and applications. Contains logic diagrams and function tables. Applications covered include: longer words, use with dynamic shift registers, selective bus storage, use as a LIFO memory, pseudo random feedback, unique counting codes, permutation of inputs, and use in arithmetic. Advanced Micro Devices Application Note (16 pg.)
- 11 **"The MSI 9328 Dual 8-Bit Shift Register"**
(9328)
Describes operation of this device and discusses applications, including variable-length shift registers, serial memories, counters. Fairchild Application Note 182 (7 pg.)
- 12 **"9338 Eight-Bit Multiple Port Register"**
(9338)
Describes the features of this device, the TTL/MSI equivalent and parallel serial expansion capabilities. Covers use as three address arithmetic unit with eight registers, and use in a first-in first-out memory. Fairchild Application Note 294 (6 pg.)
- 13 **"Design and Application of Intel's 2416 16K Charge Coupled Device"**
See listing under RAMs (Intel)
- 14 **"Using Shift Registers as Pulse Delay Networks"**
See listing under (Digital) High Speed Logic (Motorola)
- 15 **"The MC7491A Eight-Bit Serial Shift Register and the MC7495 Four-Bit Shift Register"**
(MC5491A, MC5495, MC7491A, MC7495)
Describes operation of these devices and discusses application as shift counters, delay lines, buffers, serial-parallel converters, parallel-serial converters, ring counters, and parallel arithmetic units. Also describes use in a teletypewriter-computer interface system. Motorola AN-530A (9 pg.)
- 16 **"The MC4012, An MTTL 4-Bit Shift Register"**
(MC4012)
Discusses circuit operation and applications, including serial to parallel conversion, divide-by-N counting, programmable frequency division, and programmable burst generation. Motorola AN-505 (11 pg.)
- 17 **"The Logical Design of Shift Counters"**
See listing under (Digital) Counters. (Motorola)

MEMORY, MICROPROCESSORS

Shift Registers (cont)

- 1 **"Programmable Divider Applications"**
(DM7520, DM8520)
Describes basic operation of DM7520/DM8520 divider. Covers optimum speed operation, programming, operating mode connections, applications as a speed controller for a two phase synchronous motor, and as a pseudo-random bit generator.
National AN-17 (8 pg.)
- 2 **"New MOS Clock Driver For MOS Shift Register"**
(MH0007)
Describes NH0007 circuit, turn-on characteristics, turn-off speed, power dissipation, and discusses application as a two-phase MOS clock system.
National AN-18 (8 pg.)
- 3 **"Low Power MOS Clock-Modulated Memory Systems"**
(MM400, MM402, MM406, MM451, MM482)
Presents several memory techniques to save power. Tabulates and compares methods for relative power utilization.
National AN-19 (7 pg.)
- 4 **"Design Considerations of MOS Dynamic Shift Registers With Tri-State Outputs"**
(MM4012, MM4013, MM5012, MM5013)
Describes operation of MOS shift registers with Tri-State push-pull outputs. Includes discussion of the dynamic characteristics and maximum clock frequency.
National AN-65 (4 pg.)
- 5 **"MOS Analog Function Generator"**
Describes the use of shift registers as delay lines. Shows methods to increase the clock rates and describes treating a long loop as several short ones to improve access.
National MOS Brief 4 (2 pg.)
- 6 **"MOS Delay Lines"**
(MM506)
Describes the characteristics of static and dynamic shift registers used in delay line. Discusses application as series/parallel delay lines and as substitutes for magnetic drum memories. Also covers specialized clocking techniques, such as two-speed clocking.
National AN-25 (8 pg.)
- 7 **"Low Frequency Operation With Dynamic Shift Registers"**
Discusses operation of two forms of dynamic shift registers: ratioless and ratio. Recommends techniques, such as keeping clock amplitudes high, to design added margin into systems. Discusses temperature considerations, packaging.
National MOS Handbook AN-55 (4 pg.)
- 8 **"Mask Programming Specializes MOS Shift Register Designs"**
(MM4007, MM4019, MM5007, MM5019)
Describes customizing MOS shift register bit lengths by programming a metalization mask used to manufacture these devices. Dual registers from 20 to 256 bits, and single registers from 40 to 512 bits are available. Describes single register tapped output options.
National MOS Handbook, MOS Brief 14 (2 pg.)

Shift Registers (cont)

- 9 **"Double-Clocking Cuts Standard Registers to Non-Standard Sizes"**
Describes a method of double-clocking for N data input periods to make the register appear shortened by N bits. When this is achieved, the clock rate resumes normal frequency.
National MOS Handbook, MOS Brief 16 (2 pg.)
- 10 **"MOS Goes Bipolar"**
Shows what voltages are required to combine MOS Shift Registers and Read Only Memories with bipolar devices. Presents interface diagrams.
National MOS Brief 12 (2 pg.)
- 11 **"Static Shift Register Operating Curves"**
How to use the minimum/maximum clock pulse width operating curves included in National's static shift register data sheets.
National MOS Brief 15 (2 pg.)
- 12 **"High Voltage Shift Registers Move Displays"**
(MM5081)
Describes use of the MM5081 high voltage shift register for driving gas discharge or lamp displays, ie. moving messages or moving graphics.
National AN-44 (14 PG.)
- 13 **"COS/MOS MSI Counter and Register Design and Applications"**
See listing under (Digital) CMOS (RCA)
- 14 **"Shift Registers and I/O Buffer Registers"**
(N8200, N8201, N8202, N8203, N8270, N8271, N8275, N8276, S8200, S8201, S8202, S8203, S8270, S8271, S8275, S8276)
Discussion of devices and applications, including ring counter, variable 4-bit modulo N counter, error correcting code generator, and bi-directional shift register.
Signetics Applications Handbook (16 pg.)
- 15 **"HiNIL 375 Universal Shift Register"**
See listing under (Digital) HNIL/HTL (Teledyne Semiconductor)
- 16 **"8-Bit Position Scaler"**
See listing under (Digital) Scaler. (Signetics)

MICROPROCESSORS

Applications

- 17 **"Disc Controller Design Uses New Bipolar Microcomputer LSI Components"**
(3000)
Describes the design of a 2310/5440 moving head disk controller using the 3000 series bipolar microprocessor devices. Detailed diagram.
Intel Application Note AP-7 (10 pg.)
- 18 **"M6800 Microprocessor Application Manual"**
(M6800)
Describes the use of the 6800 family of parts. Gives details of practical applications including the development of hardware and software, design of a point of sale terminal and interfaces to peripherals.
Motorola \$25.00 (716 pg.)

MICROPROCESSORS

Applications (cont)

- 1 **"Data Handling with the IMP-8"**
(IMP-8, IMP-16)
Covers basic concepts for transferring data from a memory to peripherals.
National AN-117 (4 pg.)
- 2 **"Microprocessor Mates with MOS/LSI Keyboard Encoder"**
(IMP-16)
Shows how to interface a keyboard to the IMP-16 microprocessor for text editing.
National AN-128 (6 pg.)
- 3 **"The IMP-16 in Communication Applications"**
(IMP-16)
Discusses communication processor functions, requirements for communications microprocessors and system considerations. Gives programming examples including status monitoring, data transmission, message routing, interrupt handling and error control.
National AN-134 (6 pg.)
- 4 **"The IMP-8C as a Data Concentrator"**
(IMP-8C)
Describes the use of this microprocessor in data concentrator applications. Covers use with a full duplex modem, and the terminal controller interface.
National AN-113 (6 pg.)
- 5 **"Multiple Microprocessors in Instrument Systems"**
(IMP-8, IMP-16)
Discusses systems built with central microcomputers plus peripheral microprocessors to distribute intelligence. Illustrates concepts with a data acquisition and setpoint control system.
National AN-106 (8 pg.)

General

- 6 **"A Non-volatile Microprocessor Memory Using 4K N-channel MOS RAMs"**
See listing under (Memory) RAMs (Motorola)
- 7 **"Microprocessors - An Introduction"**
Shows system components, defines terms and describes operation of an elementary computer system.
National AN-114 (4 pg.)
- 8 **"Timesharing Users Manual"**
(IMP-8, IMP-16)
Gives user information to assemble IMP-8 or IMP-16 programs using Tymshare, Inc. services, or IMP-16 programs using the General Electric Computer Timesharing facility.
National (35 pg.)
- 9 **"Microprocessors—Why They Evolved and What They Are"**
Offers background material and describes common microprocessor terms.
National Imp Brief 1 (2 pg.)

General (cont)

- 10 **"An Introduction to Microprocessors and RCA COSMAC COS/MOS Microprocessor"**
(CDP1800)
Gives a general description of microprocessor operation with some specific description of the COSMAC (CDP1800)
RCA ICAN-6416 (8 pg.)

Program Control

- 11 **"IMP-16 Interrupts"**
(IMP-16)
Describes various type of interrupts, including an overview of interrupt structure, example of interrupt request and service, multilevel and control panel interrupts.
National AN-107 (23 pg.)
- 12 **"IMP-8 Utilities Reference Manual"**
(IMP-8)
Provides information on the IMP-8 debugging program, loader programs, the standard teletype and I/O package, and the paper tape-punch package.
National (57 pg.)
- 13 **"Increasing the Number of Control Flags and Jump Conditions in the IMP-16C"**
(IMP-16C)
Describes simple and economical method of increasing the number of testable jump conditions and the number of control flags on the IMP-16C microprocessor.
National AN-101 (4 pg.)

Programming

- 14 **"S6800 Software Data Book"**
(S6800)
Description of instruction set.
American Microsystems (15 pg.)
- 15 **"S6800 Assembly Language Programming Manual"**
(S6800)
Extensive material on programming and use of the instruction set.
American Microsystems \$15.00 (244 pg.)
- 16 **"Intellec 8/Mod 80 Microcomputer Development System Reference Manual"**
(8080)
Discusses the design concepts and the use of the components of this system which can simplify the development of systems using the 8080 microprocessor.
Intel. Available with system. (152 pg.)
- 17 **"Intellec 8/Mod 8 Microcomputer System Operator's Manual"**
(8008)
Describes how to operate and run programs on the INTELLEC 8 computer, which is a system development tool for 8008 microcomputer users.
Intel. Available with system. (145 pg.)
- 18 **"Interp/80 User's Manual"**
(8080)
Describes the use of a FORTRAN IV program called INTERP/80. The program provides software simulation of the 8080 CPU along with execution monitoring commands to aid program development for the MCS-80.
Intel \$2.00 (32 pg.)

MICROPROCESSORS

Programming (cont)	Programming (cont)
<p>1 "Series 3000 Cross Microprogramming System CROMIS Reference Specification" (3000) Describes the CROMIS microprogramming system for the 3000 series computing elements. It supports the user who wants to generate microcode. Intel \$5.00 (77 pg.)</p>	<p>11 "IMP-4 Programming Techniques" Discusses subtle considerations for programming the IMP-4 including subroutines, using the address register, decimal add and multi-precision arithmetic. National AN-136 (6 pg.)</p>
<p>2 "8008 and 8080 PL/M Programming Manual" (8008, 8080) Tutorial introduction to PL/M language as it applies to these processors. Intel. Price not available (70 pg.)</p>	<p>12 "IMP-8 Assembler Manual" (IMP-8) Presents preliminary information on the use of IMP-8 assembler language. National (60 pg.)</p>
<p>3 "8080 Assembly Language Programming Manual" (8080) Discusses the assembly language format and tells how to write assembly language programs for the 8080 microprocessor. Intel \$5.00 (85 pg.)</p>	<p>13 "IMP-8 Programming Manual" (IMP-8) Provides information for the programming of the IMP-8 family of microprocessors and microcomputers. National (111 pg.)</p>
<p>4 "8008 PL/M Compiler Operators Manual" (8008) Describes operation of the 8008 PL/M cross compiler. Intel. Price not available (42 pg.)</p>	<p>14 "IMP-16 Assembler Program Description Manual" (IMP-16) Describes the internal structure of the IMP-16 Assembler. It covers the general organization, functions required for conversion to operate on a different machine, and a detailed subroutine and data description. National (105 pg.)</p>
<p>5 "8080 PL/M Compiler Operators Manual" (8080) Discusses the two distinct programs that must be executed consecutively to perform a compilation of a PL/M source program. Intel. Price not available (45 pg.)</p>	<p>15 "IMP-16 Microsymbolic Assembler" (IMP-16) The microsymbolic assembler is a collection of routines that make it possible to write microprograms for the IMP-16 in symbolic language. This manual describes the statements, character set and basic programming elements. National (21 pg.)</p>
<p>6 "IM6100 CMOS Microprocessor Basic 4K Software" (IM6100) Describes use of the Digital Equipment Corp. PDP-8 software. Intersil Application Bulletin M003 (7 pg.)</p>	<p>16 "Installation of IMP-16 Assembler on System 360/370 Operator Manual" (IMP-16) Provides information for installing the IMP-16 assembler and punch programs on an IBM 360/370 computer. National (18 pg.)</p>
<p>7 "F8 Programmer's Guide" (F8) Describes how to write programs for the F8 microprocessor system which cause the system to function as a discrete logic element. Mostek \$5.95 (304 pg.)</p>	<p>17 "Program Development Guide for the COSMAC Microprocessor" (COSMAC) This manual reviews the system architecture, describes two levels of COSMAC assembly language and describes the COSMAC software development package. RCA MPM-102 \$10.00 (97 pg.)</p>
<p>8 "ROM Based Subroutine Calls with the IM6100" (IM6100) Describes two methods for returning to the proper program location after executing a subroutine. Intersil Application Bulletin M008 (6 pg.)</p>	<p>18 "IMP-16 Programming Techniques" (IMP-16) Discusses several aspects of the instruction set to enable programmer to code more efficiently. Includes discussion of subroutines, subroute parameter passing, recursive subroutines, as well as sample programs. National AN-111 (6 pg.)</p>
<p>9 "M6800 Evaluation Module Users Guide" (M6800) Provides general information, installation instructions, preparation and operating procedures for the M6800 evaluation module. Motorola \$5.00 (150 pg.)</p>	<hr/> <p>Systems</p> <hr/>
<p>10 "A Microprogram Development System" (IMP-16) Describes the application of microprogramming to LSI processors and the advantages of a microprogram development system for hardware and software. National AN-123 (6 pg.)</p>	<p>19 "S6800 Microprocessor Hardware Book" (S6800) Provides System description and data sheets. American Microsystems (72 pg.)</p>

Bold face indicates additional data is provided, see the Product Index.

MICROPROCESSORS—

Systems (cont)

- 1 **"S6800 Hardware Reference Manual"**
(S6800)
Detailed descriptions of the system operation.
American Microsystems \$15.00 (225 pg.)
- 2 **"F8 Microprocessor Application Manual"**
(F8)
Covers details concerning bit manipulation, RAM expansion, extension of the I/O ports, subroutines and boot strap loaders.
Fairchild Semiconductor
- 3 **"Central Processor Designs Using the Intel Series 3000 Computing Elements"**
(3000)
Gives a systematic procedure for designing central processors using the series 3000 devices. (Microprogram control unit and central processing element.)
Intel Application Note AP-13 (57 pg.)
- 4 **"Intellec 8/Mod 80 Operators Manual"**
(Intellec 8)
Describes how to operate and run programs on the Intellec 8 computer, a design development tool 8080 microcomputer users.
Intel (available with system) (143 pg.)
- 5 **"M6800 System Reference and Data Sheet Handbook"**
Describes the family of parts including data sheets.
Motorola. (68 pg.)
- 6 **"Static Memory Systems for the IM6100"**
(IM6100)
Describes CMOS, nonvolatile CMOS and NMOS memory systems for the IM6100.
Intersil Application Bulletin M004 (14 pg.)
- 7 **"Teletype Interface for the IM6100 CMOS Microprocessor"**
(IM6100)
Describes a teletype interface using the IM6100 and a UART.
Intersil Application Bulletin M005 (10 pg.)
- 8 **"IM6100 Operator Console"**
(IM6100)
Describes the 6900-CONTRL console for the prototyping system.
Intersil Application Bulletin M006 (17 pg.)
- 9 **"IM6100 CMOS Microprocessor Memory Extension"**
(IM6100)
Discusses a memory extension controller to increase the memory from 4096 to 32,768 words.
Intersil Application Bulletin M007 (6 pg.)
- 10 **"12/12K Memory System for the MK5065 Microprocessor"**
(MK4096, MK5065)
Describes a complete 12Kx8 or 16Kx8 memory system for use with the MK5065 microprocessor.
Mostek (6 pg.)

Systems (cont)

- 11 **"F8 Preliminary Data Book"**
(F8)
Describes the timing, signal sequences, and chip interactions as well as provides detailed system information.
Mostek (125 pg.)
- 12 **"Device Operation and System Implementation of the Asynchronous Communications Interface Adapter (MC6850)"**
See listing under Digital-Data Transmission (Motorola)
- 13 **"GCP/P Product Description"**
(GCP/P)
Delineates the system, gives a functional description of the CROM and RALU devices, and presents the general purpose macroinstruction set. Appendices cover a microprogram to implement the IMP-16 instructions and the use of the RALU status flag.
National (61 pg.)
- 14 **"IMP-4 Technical Description"**
(IMP-4)
Describes the general purpose instruction set, gives functional and system descriptions, describes the development system and shows specific programming examples.
National (77 pg.)
- 15 **"Designing with the IMP Chip Set"**
(IMP-16)
Describes some of the major considerations in the implementation of 4 to 32 bit systems using the IMP series of devices. A 16 bit system is covered in detail.
National AN-141 (10 pg.)
- 16 **"IMP-4A Base Memory Architecture"**
(IMP-4A)
Describes a memory that taxes the capabilities of the IMP-4A microprocessor system.
National AN-137 (4 pg.)
- 17 **"IMP-8C Application Manual"**
(IMP-8)
Describes the IMP-8C's operational features, functional and logic operation, and input/output interfacing in sufficient detail to permit the user to adapt the card to various applications.
National (119 pg.)
- 18 **"IMP-8C/200 Microprocessor, IMP-8P Microcomputer Product Description"**
(IMP-8)
Describes the IMP-8C microprocessor card and the IMP-8P prototyping tool (microcomputer) as systems.
National (10 pg.)
- 19 **"IMP-16C Peripheral Interfacing Simplified"**
(IMP-16C)
Explores techniques for interfacing peripheral devices to the microprocessor.
National AN-124 (4 pg.)

MICROPROCESSORS

Systems (cont)

- 1 **"IMP-16L Product Description"**
Describes the features of the IMP-16L general microcomputer system.
National (8 pg.)
- 2 **"PACE Technical Description"**
(PACE)
Defines and explains how to use the hardware and software items that support the PACE system.
National (96 pg.)
- 3 **"Applications of LSI Processors"**
(IMP-16)
Describes system architecture and operation of IMP-16C, 16-bit parallel processor with self-contained memory. Describes applications in a data communication link analyzer, in point-of-sales and in retailing systems.
National AN-98 (8 pg.)
- 4 **"POWR I/O CROM Technical Description"**
(IMP-16)
Describes the instruction repertoire and use of this unit which expands the variety of memory and input/output operations of the IMP-16.
National (22 pg.)
- 5 **"Using a Microprocessor Beyond Apparant Speed"**
(IMP-16)
Covers the concept of cycle stealing, a technique in which a peripheral device communicates directly with memory or another peripheral device while the CPU is doing work other than using the data and address buses.
National AN-142 (6 pg.)
- 6 **"User Manual for the COSMAC Microprocessor"**
(COSMAC)
Describes the COSMAC microprocessor architecture and its instructions with examples of each instruction. Illustrates methods of adding external memory and describes machine coding techniques.
RCA MPM-101 \$5.00 (65 pg.)

Timing

- 7 **"Clock-Hold Schemes For the IMP Microprocessor Family"**
(IMP-8C, IMP-16C)
Presents scheme to extend the clock-hold function for additional periods of the main system clock, using the DM8570 shift register.
National AN-105 (4 pg.)

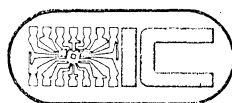
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ABBREVIATIONS OF COMPANY NAMES

AD	Analog Devices
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
AMS	Advanced Memory Systems
Analogic	Analogic Corp.
Beckman	Beckman Instruments, Helipot Division
Burr-Brown	Burr-Brown Research
Cermetek	Cermetek
CMA	Consumer Microcircuits of America
Collins	Collins Radio
Datel	Datel Systems
DDC	ILC Data Devices Corp.
EA	Electronic Arrays
EMM/Semi	EMM Semi, Div. of Electronic Memories & Magnetics
Exar	Exar Integrated Systems
Fairchild	Fairchild Semiconductor
Ferranti	Ferranti Electric
GI	General Instrument
Harris	Harris Semiconductor
Hitachi	Hitachi America, Ltd.
Hughes	Hughes Aircraft Co., MOS Division
Hybrid Sys.	Hybrid Systems
IMI	International Microcircuits, Inc.
Intech	Intech
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
IPI	Integrated Photomatrix, Inc.
ITT	ITT Semiconductors
Lithic Sys.	Lithic Systems
Litronix	Litronix
LSI Comp.	LSI Computer Systems
Micro Net	Micro Networks
Micropac	Micropac Industries
Micro Power	Micro Power Systems
Mitsubishi	Mitsubishi International
MMI	Monolithic Memories, Inc.
MOS	MOS Technology
Mostek	Mostek
Motorola	Motorola Semiconductor
National	National Semiconductor
NCR	National Cash Register, Microelectronics Div.
NEC	NEC Microcomputers
Nippon	Nippon Electric Co.
Nitron	Nitron
Nortec	Nortec Electronics
NPC	Nucleonic Products Co.
OKI	OKI Electronics of America, Inc.
Panasonic	Panasonic, Matsushita Electric Corp.
Plessey	Plessey Semiconductors
PMC	Power Monolithics Co.
PMI	Precision Monolithics, Inc.
Ragen	Ragen Semiconductor
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
Reticon	Reticon
Rockwell	Rockwell International, Microelectronic Div.
Sanken	Sanken Electric
SGS	SGS-ATES Semiconductor
Signetics	Signetics
Silicon G	Silicon General
Siliconix	Siliconix
SMC	SMC Microsystems Corp.
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSS	Solid State Scientific
SW	Stewart-Warner Microcircuits
Synertek	Synertek
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
TI	Texas Instruments
TMX	TMX, Inc.
Toshiba	Toshiba
TRW	TRW
Transitron	Transitron Electronics
Western	Western Digital

MILITARY PARTS DIRECTORY

This section is divided into three parts: a table of those manufacturers willing to perform MIL-STD-883 screening, a two way military to commercial cross reference index, and the Qualified Parts List broken down into functions. It not only shows what devices are on the list and which manufacturers supply them, but also it decodes the military numbers into familiar terms.

how to use the military parts directory

The next page contains a table showing the manufacturers who have advised that they want to screen devices to MIL-STD-883 and/or perform other environmental screening. The table also indicates which companies are currently qualified to supply one or more devices on the QPL list. Such achievement is apt to indicate that these companies are well equipped to perform 883 testing. The following page provides convenient cross references between M38510 numbers and their commercial equivalents; all these devices are listed in the latest QPL.

The heart of this section is the functional QPL parts list. It is based on the latest Defense Electronics Supply Center Qualified Products List (QPL-38510-XX) at the time of publication. The revision and date of this list are indicated at the bottom of each page. Like the Master Selection

Guide, the devices are classified by major functions; within each function the devices are arranged in alphanumeric order, which automatically groups CMOS together, 5400 Series together, etc.

A complete military part number includes a three letter suffix signifying the device class and packaging. The definitions of these letters are given in the Part Number Guide under "JAN Nomenclature." All the devices listed here meet class B and C requirements, a few devices (CMOS) meet class A specifications. The package styles and lead finishes that each manufacturer is qualified to supply can be determined by consulting the official QPL or by contacting the individual manufacturers. Once you have found the names of the companies you need to contact, you can reach them by using the information in the Manufacturers and Distributors Directory.

MILITARY DEVICE TESTING

MANUFACTURER	MIL-M-38510 QPL				MIL-STD-883 SCREENING			OTHER SCREENING	
	Linear	TTL	Other Bipolar	CMOS	Class A	Class B	Class C	Military	Industrial
Advanced Memory Systems						X	X	X	X
Advanced Micro Devices	X	X			X	X	X	X	X
American Microsystems, Inc.						X	X	X	X
Analog Devices						X	X		
Beckman Instruments					X	X	X	X	X
Burr-Brown Research						X	X	X	X
Collins Radio					X	X	X	X	X
Electronic Arrays						X	X	X	X
EMM/Semi					X	X	X	X	X
Exar Integrated Systems					X	X	X	X	X
Fairchild Semiconductor	X	X	DTL		X	X	X	X	X
General Instrument						X	X		X
Harris Semiconductor			PROM		X	X	X	X	X
Hybrid Systems					X	X	X	X	X
Intel						X	X	X	X
International Microcircuits								X	X
Intersil					X	X	X	X	X
ITT Semiconductor		X	DTL		X	X	X	X	X
Micro Networks						X	X	X	X
Micropac					X	X	X		
Monolithic Memories					X	X	X	X	X
Motorola Semiconductor	X	X			X	X	X	X	X
National Semiconductor	X	X		X	X	X	X	X	X
NEC Microcomputers						X	X		
Nitron						X	X	X	X
Nortec						X	X	X	X
Plessey Semiconductor					X	X	X		
Precision Monolithics					X	X	X	X	X
Ragen Semiconductor					X	X	X	X	X
Raytheon Semiconductor					X	X	X	X	X
RCA Solid State				X	X	X	X	X	X
Signetics		X			X	X	X	X	X
Silicon General					X	X	X	X	X
Siliconix					X	X	X	X	X
Solid State Scientific						X	X	X	X
Sprague Electric						X	X		
Teledyne Philbrick					X	X	X	X	X
Teledyne Semiconductor						X	X	X	X
Texas Instruments	X	X			X	X	X	X	X
Transitron					X	X	X	X	X

Explanation:

The "MIL-M-38510" section indicates the IC manufacturers currently providing Q.P.L. ICs. More detailed information on the specific devices is given in the Qualified Products lists which follow.

The "MIL-STD-883 Screening" section lists those manufacturers who are both set up and actively want to screen devices to the levels indicated.

"Other Screening" shows those who report that they want business calling for special military and industrial environment screening procedures.

Based on QPL-38510-21, 29 October 1975.

IC UPDATE MASTER

MILITARY PARTS INDEX — DEVICE/QPL

Cross Reference Military to Commercial				Cross Reference Commercial to Military			
Device	M38510/	Device	M38510/	Device	M38510/	Device	M38510/
HPROM0512	20101	5416	00802	00101	5430	02102	54L72
101A	10103	54160	01303	00102	5420	02103	54L73
108A	10104	54161	01306	00103	5410	02104	54L78
4000	05201	54162	01305	00104	5400	02105	54L74
4001	05202	54163	01304	00105	5404	02201	54H72
4002	05203	54164	00903	00106	5412	02202	54H73
4006	05701	5417	00804	00107	5401	02203	54H74
4007	05301	54174	01701	00108	5405	02204	54H76
4009	05501	54175	01702	00109	5403	02205	54H101
4010	05502	54180	01901	00201	5472	02206	54H103
4011	05001	54181	01101	00202	5473	02301	54H30
4012	05002	54182	01102	00203	54107	02302	54H20
4013	05101	54194	00905	00204	5476	02303	54H10
4014	05702	54195	00906	00205	5474	02304	54H00
4015	05703	5420	00102	00206	5470	02305	54H04
4017	05601	5423	00402	00207	5479	02306	54H01
4018	05602	5425	00403	00301	5440	02307	54H22
4019	05302	5426	00805	00302	5437	02401	54H40
4020	05603	5427	00404	00303	5438	02701	54L02
4021	05704	5430	00101	00401	5402	03001	930
4022	05604	5437	00302	00402	5423	03002	935
4023	05003	5438	00303	00403	5425	03003	936
4024	05605	5440	00301	00404	5427	03004	946
4025	05204	5442	01001	00501	5450	03005	962
4027	05102	5443	01002	00502	5451	04001	54H50
4031	05705	5444	01003	00503	5453	04002	54H51
4049	05503	5445	01004	00504	5454	04003	54H53
4050	05504	5446	01006	00601	5482	04004	54H54
54H00	02304	5447	01007	00602	5483	04005	54H55
54H01	02306	5448	01008	00603	9304	05001	4011
54H04	02305	5449	01009	00701	5486	05002	4012
54H10	02303	5450	00501	00801	5406	05003	4023
54H101	02205	5451	00502	00802	5416	05101	4013
54H103	02206	5453	00503	00803	5407	05102	4027
54H20	02302	5454	00504	00804	5417	05201	4000
54H22	02307	5470	00206	00805	5426	05202	4001
54H30	02301	5472	00201	00901	5495	05203	4002
54H40	02401	5473	00202	00902	5496	05204	4025
54H50	04001	5474	00205	00903	54164	05301	4007
54H51	04002	5475	01501	00905	54149	05302	4019
54H53	04003	5476	00204	00906	54195	05501	4009
54H54	04004	5477	01502	01001	5442	05502	4010
54H55	04005	5479	00207	01002	5443	05503	4049
54H72	02201	5482	00601	01003	5444	05504	4050
54H73	02202	5483	00602	01004	5445	05601	4017
54H74	02203	5485	15001	01005	54145	05602	4018
54H76	02204	5486	00701	01006	5446	05603	4020
54L00	02004	5490	01307	01007	5447	05604	4022
54L02	02701	5492	01301	01008	5448	05605	4024
54L03	02006	5493	01302	01009	5449	05701	4006
54L04	02005	5495	00901	01101	54181	05702	4014
54L10	02003	5496	00902	01102	54182	05703	4015
54L20	02002	55107	10401	01201	54121	05704	4021
54L30	02001	55108	10402	01202	54122	05705	4031
54L71	02101	55113	10405	01203	54123	07001	54S00
54L72	02102	55114	10403	01301	5492	10101	741
54L73	02103	55115	10404	01302	5493	10102	747
54L74	02105	710	10301	01303	54160	10103	101A
54L78	02104	723	10201	01304	54163	10104	108A
54S00	07001	741	10101	01305	54162	10201	723
5400	00104	747	10102	01306	54161	10301	710
5401	00107	930	03001	01307	5490	10401	55107
5402	00401	9304	00603	01401	54150	10402	55108
5403	00109	9309	01404	01402	9312	10403	55114
5404	00105	9312	01402	01403	54153	10404	55115
5405	00108	9322	01405	01404	9309	10405	55113
5406	00801	9336	03002	01405	9322	10405	55107
5407	00803	935	03002	01501	5475	15001	5485
5408	01601	936	03003	01502	5477	20101	HPROM0512
5409	01602	946	03004	01601	5408		
5410	00103	962	03005	01602	5409		
54107	00203			01701	54174		
5412	00106			01702	54175		
54121	01201			01901	54180		
54122	01202			02001	54L30		
54123	01203			02002	54L20		
54145	01005			02003	54L10		
54150	01401			02004	54L00		
54153	01403			02005	54L04		
				02006	54L03		
				02101	54L71		

Based on QPL-38510-21, 29 October 1975.

IC UPDATE MASTER

DIGITAL				Counters				Drivers (cont)			
Arithmetic Functions				Device	M38510/	Description	Source	Device	M38510/	Description	Source
Device	M38510/	Description	Source	54L04	02005	Hex Inverter	National	5417	00804	Hex Buffer/Driver with Open Collector High Voltage Output	Fairchild ITT Motorola TI
9304	00603	Dual Full Adder	Motorola	4017	05601	Decade Counter/Divider, Decoded Output	RCA	Flip-Flops			
5482	00601	2-Bit Binary Full Adder	ITT Motorola	4018	05602	Presettable Divide-by-N Counter	RCA	4013	05101	Dual "D" Flip-Flop with Set/Reset	National RCA
5483	00602	4-Bit Binary Full Adder (Look-Ahead Carry)	ITT Signetics TI	4020	05603	14-Bit Binary Counter	RCA	4027	05102	Dual J-K Master-Slave Flip-Flop	RCA
5485	15001	4-Bit Magnitude Comparator	Signetics	4022	05604	Divide-by-8 Counter/divider, Decoded Output	RCA	5470	00206	Positive Edge-Triggered J-K Flip-Flop	Fairchild ITT Motorola Signetics TI
54181	01101	High-Speed Arithmetic Logic	AMD Motorola TI	4024	05605	7-Bit Binary Counter	RCA	5472	00201	J-K Master Slave Flip-Flop (AND Inputs)	ITT Motorola National Signetics TI
54182	01102	Look-Ahead Carry Generator	Signetics	5490	01307	Decade Counter, Ripple	ITT Motorola Signetics	5473	00202	Dual J-K Master Slave Flip-Flop	ITT Motorola National Signetics TI
Buffers, Inverters				5492	01301	Divide-By-Twelve Counter (Divide-By-Two and Divide-By-Six)	ITT Motorola	5474	00205	Dual D-Type Edge-Triggered Flip-Flop	Fairchild ITT National Signetics TI
935	03002	Hex Inverter	ITT	5493	01302	4-Bit Binary Counter	ITT Motorola Signetics	5476	00204	Dual J-K Master Slave Flip-Flop with Preset and Clear	ITT National Signetics TI
936	03003	Hex Inverter	ITT	54160	01303	Synchronous Counter	Decade Signetics	5479	00207	Dual D-Type Flip-Flop	Motorola
4007	05301	Dual Complementary Pair plus Inverter	RCA	54161	01306	Synchronous 4-Bit Binary Counter	Signetics	54107	00203	Dual J-K Master Slave Flip-Flop	Motorola National Signetics TI
4009	05501	Hex Buffer/Converter, Inverting	RCA	54162	01305	Fully Synchronous Decade Counter	Signetics	54174	01701	Hex D-Type Flip-Flop	Signetics
4010	05502	Hex Buffer/Converter, Non-Inverting	National RCA	54163	01304	Fully Synchronous 4-Bit Binary Counter	Signetics	54175	01702	Quad D-Type Flip-Flop	Signetics
4049	05503	Hex Buffer/Converter, Inverting	National RCA	Decoders				54H72	02201	J-K Master-Slave Flip-Flop (AND Inputs)	Motorola Signetics
4050	05504	Hex Buffer/Converter, Non-Inverting	RCA	5442	01001	BCD-To-Decimal Decoder	ITT Motorola Signetics	54H73	02202	Dual J-K Master-Slave Flip-Flop	Signetics Motorola
5404	00105	Hex Inverter	Fairchild ITT Motorola National Signetics TI	5443	01002	Excess 3-To-Decimal Decoder	Motorola Signetics	54H74	02203	Dual D-Type Edge-Triggered Flip-Flop	Signetics
5405	00108	Hex Inverter with Open Collector Output	Fairchild ITT Motorola National Signetics TI	5444	01003	Excess 3-Gray-To-Decimal Decoder	Motorola Signetics	54H76	02204	Dual J-K Flip-Flop	TI
5437	00302	Quadruple 2-Input NAND Buffer	ITT Motorola Signetics TI	5446	01006	BCD to Seven Segment Decoder/Driver	Signetics TI	54H101	02205	J-K Negative Edge-Triggered Flip-Flop (AND-OR Inputs)	Motorola Signetics
5438	00303	Quadruple 2-Input NAND Buffer with Open Collector Outputs	Fairchild Motorola Signetics TI	5447	01007	BCD to Seven Segment Decoder/Driver	Signetics	54H103	02206	Dual J-K Negative Edge Triggered Flip-Flop	Motorola Signetics
5440	00301	Dual 4-Input NAND Buffer	Fairchild ITT Motorola Signetics TI	5448	01008	BCD to Seven Segment Decoder/Driver with 30 V Output	Motorola	54L71	02101	J-K Master-Slave Flip-Flop (AND-OR Inputs)	National
54H04	02305	Hex Inverter	Fairchild Motorola Signetics TI	Drivers				54L72	02102	J-K Master-Slave Flip-Flop (AND Inputs)	National
54H40	02401	Dual 4-Input NAND Buffer	Motorola Signetics TI	5406	00801	Hex Inverter Buffer/Driver with Open Collector High Voltage Output	Fairchild ITT Motorola TI	54L73	02103	Dual J-K Master-Slave Flip-Flop	National
				5407	00803	Hex Buffer/Driver with Open Collector High Voltage Output	Fairchild ITT Motorola TI	54L74	02105	Dual D-Type Edge-Triggered Flip-Flop	National
				5416	00802	Hex Inverter Buffer/Driver with Open Collector High Voltage Output	Fairchild ITT Motorola TI	54L78	02104	Dual J-K Master-Slave Flip-Flop	National

Gates, AND/NAND			
Device	M38510/	Description	Source
930	03001	Expandable Dual 4-Input NAND Gate	Fairchild ITT
946	03004	Quad 2-Input NAND Gate	Fairchild ITT
962	03005	Triple 3-Input NAND Gate	Fairchild ITT
4011	05001	Quad 2-Input NAND Gate	National RCA
4012	05002	Dual 4-Input NAND Gate	National RCA
4023	05003	Triple 3-Input NAND Gate	National RCA
5400	00104	Quadruple 2-Input NAND Gate	Fairchild ITT Motorola National Signetics TI
5401	00107	Quadruple 2-Input NAND Gate with Open Collector Output	Fairchild ITT Motorola National Signetics TI
5403	00109	Quadruple 2-Input NAND Gate with Open Collector Output	Fairchild ITT Motorola National Signetics TI
5408	01601	Quadruple 2-Input AND Gate	Fairchild Motorola Signetics
5409	01602	Quad 2-Input AND Gate with Open Collector Output	Fairchild Motorola Signetics
5410	00103	Triple 3-Input NAND Gate	Fairchild ITT Motorola National Signetics TI
5412	00106	Triple 3-Input NAND Gate with Open Collector Output	TI
5420	00102	Dual 4-Input NAND Gate	Fairchild ITT Motorola National Signetics TI
5426	00805	Quad 2-Input NAND Gate with Open Collector Output	Signetics
5430	00101	8-Input Nand Gate	Fairchild ITT Motorola National Signetics TI
54H00	02304	Quadruple 2-Input NAND Gate	Fairchild Motorola Signetics TI

Gates, AND/NAND (cont)			
Device	M38510/	Description	Source
54H01	02306	Quadruple 2-Input NAND Gate with Open Collector Output	Motorola Signetics TI
54H10	02303	Triple 3-Input NAND Gate	Fairchild Motorola Signetics TI
54H20	02302	Dual 4-Input NAND Gate	Fairchild Motorola Signetics TI
54H22	02307	Dual 4-Input NAND Gate with Open Collector Output	Motorola Signetics
54H30	02301	8-Input NAND Gate	Fairchild ITT Motorola Signetics TI
54L00	02004	Quadruple 2-Input NAND Gate	National
54L03	02006	Quadruple 2-Input NAND Gate with Open Collector Output	National
54L10	02003	Triple 3-Input NAND Gate	National
54L20	02002	Dual 4-Input NAND Gate	National
54L30	02001	8-Input NAND Gate	National
54S00	07001	Quadruple 2-Input NAND Gate	Signetics
Gates, AND-OR/AND-OR-Invert			
4019	05302	Quad AND-OR Select Gate	RCA
5450	00501	Expandable Dual 2-Wide 2-Input AND-OR-Invert Gate	ITT Motorola National Signetics TI
5451	00502	Expandable Dual 2-Wide 2-Input AND-OR-Invert Gate	ITT Motorola National Signetics TI
5453	00503	Expandable 4-Wide 2-Input AND-OR-Invert Gate	ITT Motorola National Signetics TI
5454	00504	4-Wide 2-Input AND-OR-Invert Gate	ITT Motorola National Signetics TI
54H50	04001	Expandable Dual 2-Wide 2-Input AND-OR-Invert Gate	Signetics TI
54H51	04002	Dual 2-Wide 2-Input AND-OR-Invert Gate	Signetics TI
54H53	04003	Expandable 2-2-2-3 Input AND-OR-Invert Gate	Signetics.
54H54	04004	2-2-2-3 Input AND-OR-Invert Gate	Signetics
54H55	04005	Expandable 2-Wide 4-Input AND-OR-Invert Gate	Signetics

Gates, Exclusive OR/NOR			
Device	M38510/	Description	Source
5486	00701	Quad 2-Input Exclusive OR Gate	Fairchild ITT Motorola Signetics TI
Gates, OR/NOR			
4000	05201	Dual 3-Input NOR Gate plus Inverter	RCA
4001	05202	Quad 2-Input NOR Gate	National RCA
4002	05203	Dual 4-Input NOR Gate	National RCA
4025	05204	Triple 3-Input NOR Gate	RCA
5402	00401	Quadruple 2-Input NOR Gate	Fairchild ITT Motorola National Signetics TI
5423	00402	Expandable Dual 4-Input NOR Gate with Strobe	Motorola TI
5425	00403	Dual 4-Input NOR Gate with Strobe	Motorola TI
5427	00404	Triple 3-Input NOR Gate	Fairchild Motorola TI
54L02	02701	Quadruple 2-Input NOR Gate	National
Latches			
5475	01501	Quad Bistable Latch, Complementary Output	Motorola Signetics
5477	01502	Quad Bistable Latch	Motorola Signetics
Multiplexers			
9309	01404	Dual 4-Input Multiplexer	AMD ITT Motorola Signetics
9312	01402	8-Channel Data Selector/Multiplexer	AMD ITT Motorola
9322	01405	Quadruple 2-Input Data Selector/Multiplexer (Non-Inverting)	AMD ITT Motorola Signetics
54150	01401	16-Channel Data Selector/Multiplexer	Signetics TI
54153	01403	Dual 4-Channel Data Selector/Multiplexer	Motorola Signetics
Multivibrators			
54121	01201	Monostable Multivibrator	ITT Signetics
54122	01202	Retriggerable Monostable Multivibrator with Clear	Motorola
54123	01203	Dual Retriggerable Monostable Multivibrator with Clear	AMD Motorola Signetics

Miscellaneous

Device	M38510/	Description	Source
54180	01901	9-Bit Odd/Even Parity Generator/Checker	Signetics

INTERFACE

Line Drivers and Receivers

55113	10405	Dual Differential Line Driver, Three-State	TI
55114	10403	Dual Differential Line Driver	AMD Fairchild
55115	10404	Dual Differential Line Receiver	AMD Fairchild TI

LINEAR

Amplifiers

101A	10103	Operational Amplifier	AMD
108A	10104	Operational Amplifier	AMD Fairchild National
741	10101	Operational Amplifier	AMD Fairchild Motorola
747	10102	Dual Operational Amplifier	Fairchild National

Comparators

710	10301	Voltage Comparator	Fairchild
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Voltage Regulators

723	10201	Voltage Regulator	Fairchild
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MEMORY

PROM

Device	M38510/	Description	Source
HPROM0512	20101	512-Bit Programmable Read Only Memory	Harris

Shift Registers

4006	05701	18-Bit Static Shift Register	RCA
4014	05702	8-Bit Static Shift Register (Synchronous)	RCA
4015	05703	Dual 4-Bit Static Shift Register	RCA
4021	05704	8-Bit Static Shift Register (Asynchronous)	RCA
4031	05705	64-Bit Static Shift Register	RCA
5495	00901	4-Bit Parallel Access Shift Register	Signetics
5496	00902	5-Bit Shift Register	ITT Signetics
54164	00903	8-Bit Serial-In Parallel-Out Shift Register	Signetics
54194	00905	4-Bit Universal Shift Register	Signetics Signetics
54195	00906	4-Bit Parallel Access Shift Register	Signetics

INTRODUCTION TO DIGITAL

The Master Selection Guide provides sufficient information to make initial product selections, to lead you to a group of device numbers and manufacturers' names. It enables you to find the products which are most appropriate to fulfill your major requirements and then provides data for many of the more important products.

All devices that appear in this section, both in the initial selection guide and in the data pages, are included in the Part Number and Product Indexes. These index listings lead to the page and the line on that page where each device appears.

The first two pages of the digital section present comparisons of the performance of the major digital families to help you choose between families. These are followed by lists of the devices in each family arranged into functional groups (arithmetic, buffers/inverters, etc.). Within each group you can readily determine all of the various circuits available, surveying the entire IC industry so that you know all your options. The initial

selection lists are followed by the device data pages which have been provided for you by the manufacturers. When such data is in the book, the page numbers are given with the initial selection listings.

Some digital circuits — calculator, watch chips, and electronic organ circuits — are not listed by model number, but the manufacturers are listed in Industrial/Consumer section. Digital circuits which do not fall into one of the major logic families are listed at the end of the selection information under the heading Digital-Other Devices. This section is not complicated by reference to package styles; the package style suffixes are usually deleted. For more information on each companies' suffixes, see the Part Number Guide. Throughout the Master Selection Guide, each full military temperature range (-55°C to 125°C) device is indicated by a dagger (†) before the manufacturer's name. Manufacturers' names are normally spelled out; however, a few are abbreviated and the abbreviations are explained on page 200.

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The manufacturers listed above are providing detailed information on their latest and most significant products. They have made this investment to help you. Some chose not to.

If you want to see more data in future editions, tell the manufacturers through their salesmen and distributors.

WHICH DIGITAL FAMILY?

Edited from material published in Fairchild Progress magazine, Peter Alfke, author.

With several digital families available, the logical question is — which are the best ICs for my particular application?

To answer the question, you need to evaluate the pros and cons of the various logic families. These tradeoffs are listed in Tables I-IV. You will need to establish your speed requirements. Since speeds are characterized by the clock rate of registers and counters, this discussion is divided into four groups based on clock rates.

Very High Speed	Clock Rate	> 100 MHz	ECL
High Speed	Clock Rate	30 to 100 MHz	ECL, S-TTL
Medium Speed	Clock Rate	5 to 50 MHz	LS-TTL, TTL
Low Speed	Clock Rate	< 5 MHz	LS-TTL, CMOS

VERY HIGH SPEED SYSTEMS — Clock Rate > 100 MHz

There is only one reasonable IC logic family for use in very high speed systems — Emitter Coupled Logic, ECL. Originally, this technology presented considerable electrical problems such as voltage and temperature sensitivity and fast edge rates that caused reflection and cross-talk problems. In recent years, however, ECL development has become more user-oriented and there is better compatibility between circuit characteristics and interconnection techniques.

The modern popular ECL line is the 10,000 Series, manufactured in uncompensated, in voltage-compensated, or in both voltage and temperature-compensated forms. The latter form of compensation assures that significant parameters such as logic levels, noise margins and speed remain constant over a wide range of temperature and power supply voltage. These 10K and 95K logic circuits have deliberately slowed-down edge rates to make them easier to use and they can also drive terminated transmission lines whenever required by the interconnection length.

HIGH SPEED SYSTEMS — Clock Rate 30 to 100 MHz (Table II)

Here, you have a choice between ECL and Schottky TTL. H-TTL is really obsolete since it consumes more power than Schottky TTL, has similar interconnection problems and offers only half the speed. Also, it is not significantly faster than the best Low Power Schottky TTL. So, this narrows down your choice to ECL and Schottky TTL.

MEDIUM SPEED SYSTEMS — Clock Rate 5 to 50 MHz (Table III)

Standard TTL has been the obvious choice for medium speed systems for many years. Many designs will increasingly use Low Power Schottky TTL as it becomes more available, multiple sourced, and as the price premium decreases. You can mix standard and LS-TTL to solve most fan-out problems.

SLOW SPEED SYSTEMS — Clock Rate < 5 MHz (Table IV)

If you design slow speed systems you are faced with the largest number of attractive alternatives. Traditionally, TTL and DTL has been used. Now you can save power, cost and avoid heat

and reliability problems by changing to LS-TTL, without affecting the logic design and perhaps not even changing the PC board layout.

If the system speed permits, you can switch to CMOS and save even more power and simplify the power supply, but now you must cope with a family of different logic elements and a hodgepodge of MSI elements, far less systems oriented than the better TTL circuits. Also you will notice wide parameter differences between the "same" products from different vendors.

The greatest challenge, however, is to examine the traditional hard-wired system design and decide whether or not it can be implemented with a microprocessor. If the requirements are both complicated and slow enough, this approach might save manufacturing cost, design time, and service time, as well as improve reliability, provide additional flexibility, and perhaps allow additional features at no extra cost.

MOS (p-channel, n-channel, either metal or silicon gate, also silicon on sapphire) does not compete directly with LS-TTL and CMOS. The MOS logic elements (gates and flip-flops) are very small but the input and output buffers are so large and relatively slow that MOS cannot be cost/performance competitive at MSI complexity (below 200 gates). MOS is therefore meaningful only in LSI circuits, where it has proven to be not only competitive, but dominating. These areas are:

- LSI memories, RAMs, ROMs, and shift registers of 500 to 4096 bits at clock rates below 5 MHz.
- Specialized, inherently slow LSI functions produced in very large volume (calculators, clocks, some instrument circuits like DVMs).
- Custom LSI circuits where the manufacturing volume is high enough or the weight/space saving valuable enough to absorb the development cost.
- Microprocessors, where a very carefully designed, standard circuit performs specialized tasks through ROM-stored programming.

SUMMARY

The proliferation of digital circuits and technologies gives you a new degree of freedom, but it also challenges your judgement and imagination. You are faced with an almost overwhelming number of competing technologies, each with its strong and weak points. The basic component speed requirement and the available power will quickly narrow your choice down to two or three different logic families; the tables presented here will make your final decision easier.

You should not forget, however, that the component speed requirement is also affected by your choice of architecture. A parallel approach requires more, but slower components, while a serial architecture requires fewer but faster components. The versatility of modern MSI circuits makes it easy to explore these alternatives. It is very important to choose the IC logic family at an early stage in the system design, since the full cost, speed and reliability advantages can only be gained by designing in accordance with the device features, taking advantage of their logic and organization.

TABLE I: COMPARISON OF ELECTRICAL CHARACTERISTICS

	CMOS 5 V SUPPLY	CMOS 10 V SUPPLY	74LS LOW POWER SCHOTTKY	9LS LOW POWER SCHOTTKY	STANDARD TTL	SCHOTTKY TTL	10K ECL
PROPAGATION DELAY	35 ns	25 ns	10 ns	5 ns	10 ns	3 ns	2 ns
FLIP-FLOP TOGGLE FREQUENCY	5 MHz	10 MHz	40 MHz	80 MHz	35 MHz	100 MHz	200 MHz
QUIESCENT POWER ¹	10 nW	10 nW	2 mW	2 mW	10 mW	25 mW	25 mW
NOISE IMMUNITY	2 V	4 V	0.8 V	0.8 V	1 V	0.9 V	0.2 V
FAN OUT (within family)	> 50 ²	> 50 ²	20	20	10	10	> 50

¹Note the change from nanowatts to milliwatts.

²Or as determined by allowable propagation delay.

TABLE II. COMPARISON OF DIGITAL LOGIC FAMILY CHARACTERISTICS FOR HIGH SPEED SYSTEMS (CLOCK RATE 30 TO 100 MHz)

10K AND 95K SERIES ECL	SCHOTTKY TTL
Advantages	Disadvantages
Short delays allow propagation through more logic levels in a clock cycle. Compatibility with even faster families currently in development makes future system upgrading easy.	Component delays are about twice as long as with ECL and will not be improved in the foreseeable future.
Low output impedance drives all types of interconnections including terminated transmission lines.	Outputs are not capable of driving terminated transmission lines without causing severe fan-out compromises.
High output drive capability and complementary outputs accommodate differential transmission over tested pairs.	Has the fastest output transitions of any logic family, causing reflection problems even with relatively short interconnection lengths, and causing cross-talk problems.
Slow edge rate minimizes reflection problems.	
Complementary outputs on many elements add design flexibility.	
Wired-OR capability simplifies logic design.	
Compensated circuits simplify power supply and temperature regulation.	Generates fast power supply load changes, requires good decoupling.
High input impedance minimizes loading, allows high fan-out.	Input thresholds and output low levels are slightly offset from conventional TTL, causing some loss of noise immunity.
Disadvantages	Advantages
Unfamiliar type of circuitry, logic, nomenclature, and pinouts.	Compatible with popular TTL, same supply voltage, almost identical signal levels, same SSI and MSI logic, nomenclature, pinouts. Ideal to speed up critical paths in standard TTL systems.
Not level-compatible with TTL and CMOS, requires additional interface elements.	Outputs require no pull-up (or down) resistors.
Requires external pull-down resistors on all used outputs.	
Has less absolute noise margin.	Large signal swing and large absolute noise immunity cause less problems with temperature or supply voltage variations and gradients, resistive drops along supply lines, and outside noise.
Higher ground current requires heavier distribution busses.	
Has one less logic pin per package due to double ground.	
Has higher power consumption at low frequencies than equivalent S-TTL circuits.	Has lower system power consumption at moderate speed.

TABLE III. COMPARISON OF DIGITAL LOGIC FAMILY CHARACTERISTICS FOR MEDIUM SPEED SYSTEMS (CLOCK RATE 5 TO 50 MHz)

STANDARD TTL	LOW POWER SCHOTTKY TTL
Advantages	Disadvantages
Large number of SSI and MSI functions.	Fewer device types available, but this is changing rapidly.
Low prices.	Presently higher priced than standard TTL.
Available from many suppliers.	Presently available from only a few suppliers.
Disadvantages	Advantages
High power consumption (10 mW per gate, 200 to 500 mW per MSI package.)	Saves 75% of the power of equivalent standard TTL.
Large, heavy, expensive, hot power supply and regulator.	Smaller, lighter, cheaper, cooler power supply and regulator.
Heat density problems when using predominantly MSI.	No heat density problem. Cooler, therefore more reliable.
Not fully compatible with most CMOS and MOS.	May eliminate the need for fans and filters.
	Compatible with CMOS and MOS.
	Generates less noise than standard TTL.

TABLE IV. COMPARISON OF DIGITAL LOGIC FAMILY CHARACTERISTICS FOR LOW SPEED SYSTEMS (CLOCK RATE 5 MHz)

STANDARD OR LOW POWER SCHOTTKY TTL	CMOS
Advantages	Disadvantages
Well designed, system-oriented MSI.	Some of the original CMOS circuits are poorly defined and not systems oriented.
Adequate speed, tight tolerances.	Low speed, delays depend on supply voltage and capacitive loading.
Low impedance outputs give good immunity against capacitively coupled noise.	Poor current noise immunity (capacitively coupled noise.)
Familiar functions, logic, pinouts.	New functions, logic pinouts.
Standard TTL available from many suppliers, low cost.	Large parameter variations between different vendors.
Disadvantages	Advantages
Relatively high static consumption and heat generation.	Extremely low static power consumption, very little heat generated at moderate speed.
Tight power supply voltage requirements (5 V ±5% commercial, ±10% military grade).	Very wide range of supply voltages (theoretically 3 . . . 20 V, practically 5 . . . 12 V).
Not well-suited for portable battery operation.	Ideally suited for battery operation.
More expensive power supply.	Low cost power supply. Less cost, weight, heat, size than for any other family.
Lower voltage noise immunity.	High voltage noise immunity, an advantage with inductively coupled noise.
LS-TTL available from only a few suppliers.	Available from many suppliers.

ABBREVIATIONS OF COMPANY NAMES

AD	Analog Devices
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
AMS	Advanced Memory Systems
Analogic	Analogic Corp.
Beckman	Beckman Instruments, Helipot Division
Burr-Brown	Burr-Brown Research
Cermetek	Cermetek
CMA	Consumer Microcircuits of America
Collins	Collins Radio
Datel	Datel Systems
DDC	ILC Data Devices Corp.
EA	Electronic Arrays
EMM/Semi	EMM Semi, Div. of Electronic Memories & Magnetics
Exar	Exar Integrated Systems
Fairchild	Fairchild Semiconductor
Ferranti	Ferranti Electric
GI	General Instrument
Harris	Harris Semiconductor
Hitachi	Hitachi America, Ltd.
Hughes	Hughes Aircraft Co., MOS Division
Hybrid Sys.	Hybrid Systems
IMI	International Microcircuits, Inc.
Intech	Intech
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
IPI	Integrated Photomatrix, Inc.
ITT	ITT Semiconductors
Lithic Sys.	Lithic Systems
Litronix	Litronix
LSI Comp.	LSI Computer Systems
Micro Net	Micro Networks
Micropac	Micropac Industries
Micro Power	Micro Power Systems
Mitsubishi	Mitsubishi International
MMI	Monolithic Memories, Inc.
MOS	MOS Technology
Mostek	Mostek
Motorola	Motorola Semiconductor
National	National Semiconductor
NCR	National Cash Register, Microelectronics Div.
NEC	NEC Microcomputers
Nippon	Nippon Electric Co.
Nitron	Nitron
Nortec	Nortec Electronics
NPC	Nucleonic Products Co.
OKI	OKI Electronics of America, Inc.
Panasonic	Panasonic, Matsushita Electric Corp.
Plessey	Plessey Semiconductors
PMC	Power Monolithics Co.
PMI	Precision Monolithics, Inc.
Ragen	Ragen Semiconductor
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
Reticon	Reticon
Rockwell	Rockwell International, Microelectronic Div.
Sanken	Sanken Electric
SGS	SGS-ATES Semiconductor
Signetics	Signetics
Silicon G	Silicon General
Siliconix	Siliconix
SMC	SMC Microsystems Corp.
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSS	Solid State Scientific
SW	Stewart-Warner Microcircuits
Synertek	Synertek
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
TI	Texas Instruments
TMX	TMX, Inc.
Toshiba	Toshiba
TRW	TRW
Transitron	Transitron Electronics
Western	Western Digital

DIGITAL—CMOS

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line
Arithmetic Functions				Arithmetic Functions (cont)				Buffers/Inverters (cont)			
2 x 2 Bit (Parallel) Binary Multiplier	MC14554A	† Motorola		Look-Ahead Carry Block	F4582C	Fairchild		Hex Buffer/Converter (Non-Inverting) - Improved	F4050C	Fairchild	
	MC14554C	Motorola			F4582M	† Fairchild	50		F4050M	† Fairchild	
4-Bit Full Adder	F4008C	Fairchild			MC14582A	† Motorola			MEM4050D	GI	
	F4008M	† Fairchild			MC14582C	Motorola			MEM4050P	GI	
	F40283C	Fairchild			CD40182A/B	† RCA			HD4050A-2	† Harris	100
	F40283M	† Fairchild			see page 375				HD4050A-9	Harris	
	HD4008A-2	† Harris			CD40182A/BE	RCA			MC14050A	† Motorola	
	HD4008A-9	Harris			see page 375				MC14050C	Motorola	
	HD54C83	† Harris			SCL4582A	SSS			CD4050C	National	
	see page 266				TF4582A	† TI			CD4050M	National	
	HD74C83	Harris	10		TP4582A	TI			CD4050A/B	† RCA	
	see page 266			4-Bit Magnitude Comparator					see page 375		
	MC14008A	† Motorola			F40085C	Fairchild			CD4050A/BE	RCA	
	MC14008C	Motorola			F40085M	† Fairchild			see page 375		
	MM54C83	† National			HD54C85	† Harris	60		HBF4050AE	SGS	
	MM74C83	National			see page 266				SCL4050A	† SSS	
	CD4008A/B	† RCA			HD74C85	Harris			SCL4050AE	SSS	
	see page 375				see page 266				CM4050A	† Solitron	110
	CD4008A/BE	RCA			MC14585A	† Motorola			CM4050AE	Solitron	
	see page 375				MC14585C	Motorola			SW4050AE	SW	
	HBF4008AE	SGS			MM54C85	† National			CD4050	Teledyne S	
	SCL4008A	† SSS	20		MM74C85	National			TF4050A/B	† TI	
	SCL4008AE	SSS			CD4063A/B	† RCA			TP4050A/B	TI	
	CM4008A	† Solitron			see page 375				TC4050	Toshiba	
	CM4008AE	Solitron			CD4063A/BE	RCA					
	TF4008A	† TI			see page 375			Hex Buffer, Open Drain (Active pull down)			
	TP4008A	TI			SCL4585A	† SSS			HD54C906	† Harris	
	TC4008	Toshiba			SCL4585AE	SSS			HD74C906	Harris	
Triple Serial Adder (Positive Logic) With Internal Carry	MC14032A	† Motorola			TC4585	Toshiba			MM54C906	† National	
	MC14032C	Motorola							MM74C906	National	
	CD4032A	† RCA		NBCD Adder (Natural Binary Coded Decimal)	MC14560A	† Motorola	70				
	see page 375				MC14560C	Motorola					
	CD4032AE	RCA						Hex Buffer, Open Drain (Active pull up)			
	see page 375								HD54C907	† Harris	120
	CM4032A	† Solitron							HD74C907	Harris	
	CM4032AE	Solitron	30						MM54C907	† National	
	TC4032	Toshiba							MM74C907	National	
Triple Serial Adder (Negative Logic) With Internal Carry	MC14038A	† Motorola									
	MC14038C	Motorola		Nines Complementer	MC14561A	† Motorola					
	CD4038A	† RCA			MC14561C	Motorola					
	see page 375										
	CD4038AE	RCA		Data Path Switch	F4704C	Fairchild					
	see page 375				F4704M	† Fairchild					
	CM4038A	† Solitron						Hex Buffer Three-State			
	CM4038AE	Solitron							F40097C	Fairchild	
	TC4038	Toshiba							F40097M	† Fairchild	
4-Bit Arithmetic Array	CD4057A	† RCA							HD70C95	Harris	
	see page 375								HD70C97	Harris	
4-Bit Arithmetic Logic Unit	MC14581A	† Motorola	40						HD80C95	Harris	
	MC14581C	Motorola							HD80C97	Harris	
	CD40181A/B	† RCA		Arithmetic Logic Register Stack	F4705C	Fairchild			MC14503	Motorola	130
	see page 375				F4705M	† Fairchild			MM70C95	† National	
	CD40181A/BE	RCA							MM70C97	† National	
	see page 375								MM80C95	National	
	SCL4581A	† SSS							MM80C97	National	
	SCL4581AE	SSS									
	TF4581A	† TI									
	TP4581A	TI									
				Buffers/Inverters							
				Quad Low Impedance Buffer	SCL4441A	† SSS	80				
					SCL4441AE	SSS					
				Hex Buffer/Converter (Non-Inverting)							
					CD4010C	National					
					CD4010M	† National					
					CD4010A/B	† RCA					
					see page 375						
					CD4010A/BE	RCA					
					see page 375						
					HBF4010AE	SGS					
					SCL4010A	† SSS					
					SCL4010AE	SSS					
					CM4010A	† Solitron					
					CM4010AE	Solitron	90				
					TF4010A/B	† TI					
					TP4010A/B	TI					
					TC4010	Toshiba					
								Hex Buffer/Converter (Inverting)			
									CD4009C	National	
									CD4009M	† National	
									CD4009A/B	† RCA	
									see page 375		
									CD4009A/BE	RCA	
									see page 375		
									HBF4009AE	SGS	
									SCL4009A	† SSS	140
									SCL4009AE	SSS	
									CM4009A	† Solitron	
									CM4009AE	Solitron	
									TF4009A/B	† TI	
									TP4009A/B	TI	
									TC4009	Toshiba	
								Hex Buffer/Converter (Inverting) - Improved			
									F4049C	Fairchild	
									F4049M	† Fairchild	
									(continued)		

† Military Temperature Range (-55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

DIGITAL—CMOS (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line	
Buffers/Inverters (cont)				Buffers/Inverters (cont)				Counters, Binary (cont)				
Hex Buffer/Converter (Inverting) - Improved (continued)				Hex Inverter/Buffer Three-State Strobed (continued)				7-Stage Binary Counter (continued)				
	MEM4049D	† GI			CD4502A/BE	RCA			SW4024AE	SW		
	MEM4049P	GI			see page 375			TF4024A	† TI			
	HD4049A-2	† Harris			SCL4502A	† SSS		TP4024A	TI			
	HD4049A-9	Harris			SCL4502AE	SSS		TC4024	Toshiba			
	MC14049A	† Motorola		Hex CMOS Compatible Buffer				8-Stage Synchronous Binary Counter				
	MC14049C	Motorola			DS1630	† National			SCL4404A	† SSS	110	
	CD4049C	National			DS3630	National	60		SCL4404AE	SSS		
	CD4049M	† National		Dual Complementary Pair plus Inverter				12-Stage Binary Counter				
	CD4049A/B	† RCA			F4007C	Fairchild			F4040C	Fairchild		
	see page 375				F4007M	† Fairchild			F4040M	† Fairchild		
	CD4049A/BE	RCA	10		MEM4007D	† GI			HD4040A-2	† Harris		
	see page 375				MEM4007P	GI			HD4040A-9	Harris		
	HBF4049AE	SGS			HD4007A-2	† Harris			MC14040A	† Motorola		
	SCL4049A	† SSS			HD4007A-9	Harris			MC14040C	Motorola		
	SCL4049AE	SSS			MC14007A	† Motorola			CD4040C	National		
	CM4049A	† Solitron			MC14007C	Motorola			CD4040M	† National		
	CM4049AE	Solitron			CD4007C	National			CD4040A	† RCA	120	
	SW4049AE	SW			CD4007M	† National	70		see page 375			
	CD4049	Teledyne S			CD4007A	† RCA			CD4040AE	RCA		
	TF4049A/B	† TI			see page 375				see page 375			
	TP4049A/B	TI			CD4007AE	RCA			CDS4040	† RCA		
	TC4049	Toshiba	20		see page 375				CDS4040E	RCA		
Hex Inverter					HBF4007AE	SGS			SCL4040A	† SSS		
	F4069C	Fairchild			SCL4007A	† SSS			SCL4040AE	SSS		
	F4069M	† Fairchild			SCL4007AE	SSS			CM4040A	† Solitron		
	HD54C04	† Harris			CM4007A	† Solitron			CM4040AE	Solitron		
	HD74C04	Harris			CM4007AE	Solitron			TF4040A	† TI		
	MC14069BA	† Motorola			TF4007A	† TI			TP4040A	TI		
	MC14069BC	Motorola			TP4007A	TI			TC4040	Toshiba	130	
	MC14572A	† Motorola			TC4007	Toshiba	80	14-Stage Binary Counter				
	MC14572C	Motorola		Quad True/Complement Buffer						F4020C	Fairchild	
	CD4069BC	National			F4041C	Fairchild			F4020M	† Fairchild		
	MM54C04	† National	30		F4041M	† Fairchild			HD4020A-2	† Harris		
	CD4069BM	† National			CD4041A/B	† RCA			see page 266			
	CD4069A/B	† RCA			see page 375				HD4020A-9	Harris		
	see page 375				CD4041A/BE	RCA			see page 266			
	CD4069A/BE	RCA			see page 375				MC14020A	† Motorola		
	see page 375				SCL4041A	† SSS			MC14020C	Motorola		
	SCL4069	SSS			SCL4041AE	SSS			CD4020C	National		
	SCL4069A	† SSS			CM4041A	† Solitron			CD4020M	† National		
	SCL4069AE	SSS			CM4041AE	Solitron			CD4020A	† RCA		
	SCL4449A	† SSS		Counters, Binary						see page 375		
	SCL4449AE	SSS			Divide by 2, 8 or 16 Counters					CD4020AE	RCA	
	CM4069A/B	† Solitron			MM54C93	† National			see page 375		140	
	CM4069A/BE	Solitron	40		MM74C93	National	90		CDS4020	† RCA		
	MM54C04	† Teledyne S		7-Stage Binary Counter						CDS4020E	RCA	
	MM74C04	Teledyne S			F4024C	Fairchild			HBF4020AE	SGS		
	TF4315A	† TI			F4024M	† Fairchild			SCL4020A	† SSS		
	TP4315A	TI			HD4024A-2	† Harris			SCL4020AE	SSS		
	TC4069	Toshiba			HD4024A-9	Harris			CM4020A	† Solitron		
	TC7404	Toshiba			MC14024A	† Motorola			CM4020AE	Solitron		
Hex Inverter Three-State					MC14024C	Motorola			SW4020AE	SW		
	F40098C	Fairchild			CD4024C	National			TF4020A	† TI		
	F40098M	† Fairchild			CD4024M	† National			TP4020A	TI	150	
	HD80C96	Harris			CD4024A	† RCA			TC4020	Toshiba		
	HD80C98	Harris	50		see page 375			14-Stage Binary Counter and Oscillator				
	MM80C96	National			CD4024AE	RCA	100		CD4060A	† RCA		
	MM80C98	National			see page 375				see page 375			
Hex Inverter/Buffer Three-State Strobed					HBF4024AE	SGS			CD4060AE	RCA		
	MC14502A	† Motorola			SCL4024A	† SSS			see page 375			
	MC14502C	Motorola			SCL4024AE	SSS			CDS4060	† RCA		
	CD4502A/B	† RCA			CM4024A	† Solitron			CDS4060E	RCA		
	see page 375				CM4024AE	Solitron			SCL4060A	† SSS		
	(continued)				(continued)				(continued)			

† Military Temperature Range (—55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

DIGITAL—CMOS (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line
Counters, Binary (cont)				Counters, Binary (cont)				Counters, Decade (cont)			
14-Stage Binary Counter and Oscillator (continued)				Presetable Binary Up/Down Counter (continued)				Presetable Fully Synchronous Decade Counter, Synchronous Clear (continued)			
	SCL4060AE	SSS		MC14516C	Motorola			MM74C162	Teledyne S		
Presetable Synchronous Binary Counter, Asynchronous Clear				CD40193C	National			TF4362A	† TI		
F40161C	Fairchild			CD40193M	† National			TP4362A	TI		
F40161M	† Fairchild			CD4516C	National						
HD54C161	† Harris			CD4516M	† National						
see page 266				MM54C193	† National		60				
HD74C161	Harris			MM74C193	National			Dual Synchronous Decade Counter			
see page 266				CD40193A/B	† RCA			F4518C	Fairchild		
MC14161BA	† Motorola			see page 375				F4518M	† Fairchild		
MC14161BC	Motorola			CD40193A/BE	RCA			HD14518-2	† Harris		
MM54C161	† National		10	see page 375				HD14518-9	Harris		
MM74C161	National			CD4516A/B	† RCA			MC14518A	† Motorola		
MM54C161	† Teledyne S			see page 375				MC14518C	Motorola		
MM74C161	Teledyne S			CD4516A/BE	RCA			CD4518C	National		110
TF4361A	† TI			see page 375				CD4518M	† National		
TP4361A	TI			SCL4516A	† SSS			CD4518A/B	† RCA		
				SCL4516AE	SSS			see page 375			
				MM54C193	† Teledyne S			CD4518A/BE	RCA		
				MM74C193	Teledyne S			see page 375			
				TC4516	Toshiba			CDS4518	† RCA		
Presetable Fully Synchronous Binary Counter, Synchronous Clear				Presetable 8-bit Binary Down Counter				Decade Counter/Divider, Decoded Output			
F40163C	Fairchild			CD40103A/B	† RCA		70	F4017C	Fairchild		
F40163M	† Fairchild			see page 375				F4017M	† Fairchild		
HD54C163	† Harris			CD40103A/BE	RCA			HD4017A-2	† Harris		
HD74C163	Harris			see page 375				HD4017A-9	Harris		
MC14163BA	† Motorola			Programmable Binary Divide-by-N 4-Bit Counter				MC14017A	† Motorola		
MC14163BC	Motorola			F4526C	Fairchild			MC14017C	Motorola		
MM54C163	† National		20	F4526M	† Fairchild			CD4017C	National		
MM74C163	National			MC14526A	† Motorola			CD4017M	† National		130
MM54C163	† Teledyne S			MC14526C	Motorola			CD4017A	† RCA		
MM74C163	Teledyne S			TF4526A	† TI			see page 375			
TF4363A	† TI			TP4526A	TI			CD4017AE	RCA		
TP4363A	TI			Counters, Decade				see page 375			
				Presetable Decade Counter (Sets to 0 or 9, divides by 2, 5 or 10)				CD4017AE	RCA		
				MM54C90	† National			CDS4017	† RCA		
				MM74C90	National			CDS4017E	RCA		
				Presetable Synchronous Decade Counter, Asynchronous Clear				HBF4017AE	SGS		
				F40160C	Fairchild		80	SCL4017A	† SSS		
				F40160M	† Fairchild			SCL4017AE	SSS		
				HD54C160	† Harris			CM4017A	† Solitron		
				see page 266				CM4017AE	Solitron		
				HD74C160	Harris			SW4017AE	SW		140
				see page 266				TF4017A	† TI		
				MC14160BA	† Motorola			TP4017A	TI		
				MC14160BC	Motorola			TC4017	Toshiba		
				MM54C160	† National			Presetable Decade Up/Down Counter			
				MM74C160	National			F40192C	Fairchild		
				MM54C160	† Teledyne S			F40192M	† Fairchild		
				MM74C160	Teledyne S			F4510C	Fairchild		
				TF4360A	† TI		90	F4510M	† Fairchild		
				TP4360A	TI			HD14510-2	† Harris		
				Presetable Fully Synchronous Decade Counter, Synchronous Clear				HD14510-9	Harris		
				F40162C	Fairchild			HD54C192	† Harris		150
				F40162M	† Fairchild			see page 266			
				HD54C162	† Harris			HD74C192	Harris		
				see page 266				see page 266			
				HD74C162	Harris			MC14510A	† Motorola		
				see page 266				MC14510C	Motorola		
				MC14162BA	† Motorola			CD40192BC	National		
				MC14162BC	Motorola			(continued)			
				MM54C162	† National						
				MM74C162	National						
				MM54C162	† Teledyne S		100				
				(continued)							

† Military Temperature Range (-55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

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DIGITAL—CMOS (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line
Counters, Decade (cont)				Counters, Decade (cont)				Counters, Miscellaneous (cont)			
Presettable Decade Up/Down Counter (continued)	CD40192BM	† National	10	3 Decade Counter, Multiplexed Output (continued)	MC14553C	Motorola	50	Divide-By-8-Counter/Divider, Decoded Output (continued)	N4022	Signetics	100
	CD4510C	National		4 Decade Counter	TC5001	Toshiba			NBF4022AE	SGS	
	CD4510M	† National		4 Decade Counter, Multiplexed Output	HD54C925	† Harris			SCL4022A	† SSS	
	MM54C192	† National		HD54C926	† Harris	CM4022A			† Solitron		
	MM74C192	National		HD74C925	Harris	CM4022AE			Solitron		
	CD40192A/B	† RCA		HD74C926	Harris	TF4022A			† TI		
	CD40192A/BE	RCA		MM54C925	† National	TP4022A		TI			
	CD4510A/B	† RCA		MM74C925	National	TC4022		Toshiba			
	CD4510A/BE	RCA		MM54C926	† National	Divide-by-60-Counter, BCD Output (Industrial Time Base Generator)					
	CD4510A/BE	RCA		MM74C926	National	MC14566A		† Motorola			
SCL4510A	† SSS			MC14566C	Motorola						
SCL4510AE	SSS			Presettable Divide-by-N Counter							
MM54C192	† Teledyne S			F4018C	Fairchild	110					
MM74C192	Teledyne S			F4018M	† Fairchild						
TC4510	Toshiba			HD4018A-2	† Harris						
Presettable 2-Decade Down Counter				4 Digit Counter, Multiplexed Output, left digit counts to 2 (Maximum count 1999.)	HD54C928		† Harris				
CD40102A/B	† RCA			HD74C928	Harris						
CD40102A/BE	RCA			MM54C928	† National						
Programmable Decade Divide-By-N 4-Bit Counter				5 Decade Counter, Multiplexed Output	MC14534A		† Motorola				
F4522C	Fairchild			MC14534C	Motorola						
F4522M	† Fairchild			7 Decade Counter, Multiplexer, Display Driver, 2-6 v Supply							
MC14522A	† Motorola			ICM7208	Intersil						
MC14522C	Motorola	20		Counters, Miscellaneous							
TF4522A	† TI			Presettable Up/Down Binary or Decade Counter							
TP4522A	TI			F4029C	Fairchild	70					
4-Decade Divide-by-N Counter				F4029M	† Fairchild						
CD4059A	† RCA			HD4029A-2	† Harris						
Decade Counter/Divider — 7 Segment Display Output and Display Enable				HD4029A-9	Harris						
HD4026A-2	† Harris			CD4029C	National						
HD4026A-9	Harris			CD4029M	† National						
CD4026A	† RCA			CD4029A	† RCA						
CD4026AE	RCA			CD4029AE	RCA						
SCL4026A	† SSS			HB4029AE	SGS						
SCL4026AE	SSS	30		SCL4029A	† SSS						
SCL4426A	† SSS			SCL4029AE	SSS						
SCL4426AE	SSS			CM4029A	† Solitron						
CM4026A	† Solitron			CM4029AE	Solitron						
CM4026AE	Solitron			SW4029AE	SW						
Decade Counter/Divider — 7 Segment Display Output and Ripple Blanking				TF4029A/B	† TI	80					
CD4033A	† RCA			TP4029A/B	TI						
CD4033AE	RCA			TC4029	Toshiba						
HB4033AE	SGS			Divide-By-8-Counter/Divider, Decoded Output							
SCL4033A	† SSS			F4022C	Fairchild						
SCL4033AE	SSS			F4022M	† Fairchild						
SCL4433A	† SSS			HD4022A-2	† Harris						
SCL4433AE	SSS	40		HD4022A-9	Harris						
CM4033A	† Solitron			MC14022A	† Motorola						
CM4033AE	Solitron			MC14022C	Motorola						
3-1/2 Digit Counter to BCD Driver				CD4022C	National	90					
CM4102A	† Solitron			CD4022M	† National						
CM4102AE	Solitron			CD4022A	† RCA						
3 Decade Counter, Multiplexed Output				CD4022AE	RCA						
F4553C	Fairchild			CD4022AE (continued)							
F4553M	† Fairchild			Decoders							
MC14553A	† Motorola			BCD-to-Decimal Decoder							
(continued)				F4028C	Fairchild		130				
				F4028M	† Fairchild						
				HD4028A-2	† Harris						
				HD4028A-9	Harris						
				HD54C42	† Harris						
				HD74C42	Harris						
				MC14028A	† Motorola						
				MC14028C	Motorola						
				CD4028C	National						
				MM54C42	† National						
				CD4028M	† National						
				MM74C42	National						
				CD4028A	† RCA						
				CD4028AE	RCA						
				HB4028AE	SGS						
				SCL4028A	† SSS						
				SCL4028AE	SSS						
				CM4028A	† Solitron						
				CM4028AE	Solitron						
				SW4028AE	SW						
				(continued)							

† Military Temperature Range (–55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

DIGITAL—CMOS (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line				
Decoders (cont)				Decoders (cont)				Drivers (cont)							
BCD-to-Decimal Decoder (continued)				4-Line-to-16-Line Decoder/De-Multiplexer (continued)				Dual and Quad Line Drivers— See Miscellaneous							
	MM54C42	† Teledyne S			HD74C154	Harris	50	Flip-Flops							
	MM74C42	Teledyne S			MM54C154	† National		Dual "D" Flip-Flop							
	TF4028A	† TI			MM74C154	National			F4013C	Fairchild					
	TP4028A	TI			MM54C154	† Teledyne S			F4013M	† Fairchild					
	TC4028	Toshiba			MM74C154	Teledyne S			MEM4013D	† GI					
BCD-to-7-Segment Decoder				1 of 8 Strobed Decoder						MEM4013P	GI				
	HD54C48	† Harris			SCL4428AE	SSS			HD4013A-2	† Harris					
	HD74C48	Harris			SCL4428A	† SSS			HD4013A-9	Harris	100				
	MC14558A	† Motorola		Drivers						HD54C74	† Harris				
	MC14558C	Motorola		BCD-to-7-Segment Latch/Decoder/Driver						HD74C74	Harris				
	MM54C48	† National	10		F4511C	Fairchild			MC14013A	† Motorola					
	MM74C48	National			F4511M	† Fairchild			MC14013C	Motorola					
	MM54C48	† Teledyne S			HD14511-2	† Harris	60		CD4013C	National					
	MM74C48	Teledyne S			HD14511-9	Harris			CD4013M	† National					
	TC5002	Toshiba			MC14511A	† Motorola			MM54C74	† National					
4-Bit Latch/4-to-16-Line Decoder (High)						MC14511C	Motorola		MM74C74	National					
	F4514C	Fairchild			CD4511C	National			CD4013A/B	† RCA	110				
	F4514M	† Fairchild			CD4511A/B	† RCA			see page 375						
	MC14514A	† Motorola			see page 375				CD4013A/BE	RCA					
	MC14514C	Motorola			CD4511A/BE	RCA			see page 375						
	CD4514A/B	† RCA			see page 375				HBF4013AE	SGS					
	CD4514A/BE	RCA	20		SCL4511A	† SSS			SCL4013A	† SSS					
	see page 375				SCL4511AE	SSS			SCL4013AE	SSS					
	SCL4514A	† SSS			CM4511B	† Solitron	70		CM4013A	† Solitron					
	CM4514B	† Solitron			CM4511BE	Solitron			CM4013AE	Solitron					
	CM4514BE	Solitron			BCD-to-7-Segment Latch/Decoder/Driver (for liquid Crystal Displays)					SW4013AE	SW				
	TC4514	Toshiba				HD14543-2	† Harris		MM54C74	† Teledyne S					
4-Bit Latch/4-to-16-Line Decoder (Low)						HD14543-9	Harris		MM74C74	Teledyne S					
	F4515C	Fairchild			MC14543A	† Motorola			TF4013A/B	† TI	120				
	F4515M	† Fairchild			MC14543C	Motorola			TP4013A/B	TI					
	MC14515A	† Motorola			SCL4543	SSS			TC4013	Toshiba					
	MC14515C	Motorola			BCD-to-7-Segment Liquid Crystal Decoder/Driver with "Display Frequency Output"					Quad "D" Flip-Flop					
	CD4515A/B	† RCA				CD4055A/B	† RCA			F40175C	Fairchild				
	see page 375					see page 375				F40175M	† Fairchild				
	CD4515A/BE	RCA	30			CD4055A/BE	RCA			HD54C175	† Harris				
	see page 375					see page 375				HD74C175	Harris				
	SCL4515A	† SSS			BCD-to-7-Segment Liquid Crystal Decoder/Driver with Strobed-Latch Function						MC14175BA	† Motorola			
	CM4515B	† Solitron				CD4056A/B	† RCA			MC14175BC	Motorola				
	CM4515BE	Solitron				see page 375				MM54C175	† National				
	TC4515	Toshiba				CD4056A/BE	RCA			MM74C175	National				
						see page 375			Quad "D" Flip-Flop Three-State						
Dual Binary to 1 of 4 Decoder/Demultiplexer (High)											F4076C	Fairchild	130		
	F4555C	Fairchild			4-Line Liquid Crystal Display Driver							F4076M	† Fairchild		
	F4555M	† Fairchild				CD4054A/B	† RCA	80			HD54C173	† Harris			
	MC14555A	† Motorola				see page 375					HD74C173	Harris			
	MC14555C	Motorola				CD4054A/BE	RCA				MC14076A	† Motorola			
	CD4555A/B	† RCA				see page 375					MC14076C	Motorola			
	see page 375										MM54C173	† National			
	CD4555A/BE	RCA	40		3 1/2-Digit Liquid Crystal Display Driver							MM74C173	National		
	see page 375					CM4117A	† Solitron				CD4076BC	National			
	SCL4555A	SSS									CD4076BM	† National			
Dual Binary to 1 of 4 Decoder/Demultiplexer (Low)						4-Digit Liquid Crystal Display Driver							CD4076A/B	† RCA	140
	F4556C	Fairchild				5201	Intel					see page 375			
	F4556M	† Fairchild				5204	Intel					CD4076A/BE	RCA		
	MC14556A	† Motorola				5202	Intel					see page 375			
	MC14556C	Motorola				5015	Nortec					SCL4076AE	SSS		
	CD4556A/B	† RCA				SCL5424	SSS					SCL4076A	† SSS		
	see page 375					SCL5441	SSS					CM4076A/B	† Solitron		
	CD4556A/BE	RCA			8-Digit LED Display Driver							CM4076A/BE	Solitron		
	see page 375					SCL5440A	† SSS					MM54C173	† Teledyne S		
	SCL4556A	SSS			Dual High Voltage Driver, Source 250 ma							MM74C173	Teledyne S		
4-Line-to-16-Line Decoder/De-Multiplexer															
	HD54C154	† Harris				HD54C908	† Harris	90							
	see page 266 (continued)					HD74C908	Harris								
						MM74C908	National								
						MM74C918	National								

† Military Temperature Range (–55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

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DIGITAL—CMOS (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line	
Flip-Flops (cont)				Gates, AND/NAND				Gates, AND/NAND (cont)				
Hex "D" Flip-Flop				Dual 4-Input AND Gate				8-Input NAND Gate (continued)				
	F40174C	Fairchild			F4082C	Fairchild			SCL4412A	† SSS		
	F40174M	† Fairchild			F4082M	† Fairchild			SCL4412AE	SSS		
	HD54C174	† Harris			MC14082BA	† Motorola			CM4068A/B	† Solitron		
	HD74C174	Harris			MC14082BC	Motorola			CM4068A/BE	Solitron		
	MC14174BA	† Motorola			CD4082A/B	† RCA			TC4068	Toshiba		
	MC14174BC	Motorola			see page 375							
	MM54C174	† National			CD4082A/BE	RCA						
	MM74C174	National			see page 375							
	TF4370A	† TI			SCL4082A	SSS	60					
	TP4370A	TI	10		SCL4082AE	† SSS						
					TC4082	Toshiba						
Dual "J-K" Flip-Flop				Triple 3-Input AND Gate				Dual 4-Input NAND Gate				
	F4027C	Fairchild			F4073C	Fairchild			F4012C	Fairchild		
	F4027M	† Fairchild			F4073M	† Fairchild			F4012M	† Fairchild	110	
	HD4027A-2	† Harris			MC14073BA	† Motorola			HD4012A-2	† Harris		
	HD4027A-9	Harris			MC14073BC	Motorola			HD4012A-9	Harris		
	HD54C76	† Harris			CD4073A/B	† RCA			HD54C20	† Harris		
	HD74C76	Harris			see page 375				HD74C20	Harris		
	MC14027A	† Motorola			CD4073A/BE	RCA			MC14012A/BA	Motorola †		
	MC14027C	Motorola			see page 375				MC14012C/BC	Motorola		
	CD4027C	National			SCL4073A	† SSS			CD4012C	National		
	CD4027M	† National	20		SCL4073AE	SSS			CD4012M	† National		
	MM54C76	† National			CM4073A/B	† Solitron	70		MM54C20	† National		
	MM74C76	National			CM4073A/BE	Solitron			MM74C20	National	120	
	CD4027A/B	† RCA			TF4073B	† TI			CD4012A/B	† RCA		
	see page 375				TP4073B	TI			see page 375			
	CD4027A/BE	RCA			TC4073	Toshiba			CD4012A/BE	RCA		
	see page 375								see page 375			
	HBF4027AE	SGS			Quad 2-Input AND Gate					HBF4012AE	SGS	
	SCL4027A	† SSS			F4081C	Fairchild			SCL4012A	† SSS		
	SCL4027AE	SSS			F4081M	† Fairchild			SCL4012AE	SSS		
	CM4027A	† Solitron			HD54C08	† Harris			CM4012A	† Solitron		
	CM4027AE	Solitron			HD74C08	Harris			CM4012AE	Solitron		
	SW4027AE	SW	30		MC14081A/BA	Motorola †			SW4012AE	SW		
	MM54C76	† Teledyne S			MC14081C/CB	Motorola	80		MM54C20	† Teledyne S	130	
	MM74C76	Teledyne S			MM54C08	† National			MM74C20	Teledyne S		
	TF4027A	† TI			MM74C08	National			TF4012A/B	† TI		
	TP4027A	TI			CD4081A/B	† RCA			TP4012A/B	TI		
	TC4027	Toshiba			see page 375				TC4012	Toshiba		
	TC7476	Toshiba			CD4081A/BE	RCA			TC7420	Toshiba		
					see page 375							
					SCL4081A	† SSS			Dual 2-Input NAND Gate (Driver)			
					SCL4081AE	SSS			CD40107A/B	† RCA		
					CM4081A/B	† Solitron			see page 375			
					CM4081A/BE	Solitron			CD40107A/BE	RCA		
					TF4081B	† TI			see page 375			
					TP4081B	TI	90					
					TC4081	Toshiba						
Dual "J-K" Flip-Flop W/O Preset				8-Input NAND Gate				Dual 4-Input Expandable NAND Gate				
	HD54C73	† Harris			F4068C	Fairchild			SCL4412A	† SSS		
	HD74C73	Harris			F4068M	† Fairchild			SCL4412AE	SSS		
	HD54C107	† Harris			HD54C30	† Harris						
	HD74C107	Harris	40		HD74C30	Harris			Triple 3-Input NAND Gate			
	MM54C73	† National			MC14068BA	† Motorola			F4023C	Fairchild		
	MM74C73	National			MC14068BC	Motorola			F4023M	† Fairchild	140	
	MM54C107	† National			MC14501A	† Motorola			HD4023A-2	† Harris		
	MM74C107	National			MC14501C	Motorola			HD4023A-9	Harris		
	MM54C73	† Teledyne S			MM54C30	† National			HD54C10	† Harris		
	MM74C73	Teledyne S			MM74C30	National			HD74C10	Harris		
	MM54C107	† Teledyne S			CD4068A/B	† RCA			MC14023A/BA	Motorola †		
	MM74C107	Teledyne S			see page 375				MC14023C/BC	Motorola		
					CD4068A/BE	RCA			CD4023C	National		
					see page 375				CD4023M	† National		
					CD4068A/BE	RCA	100		MM54C10	† National		
					(continued)				MM74C10	National	150	
									CD4023A/B	† RCA		
									see page 375			
									CD4023A/BE	RCA		
									see page 375			
									HBF4023AE	SGS		
									SCL4023A	† SSS		
									SCL4023AE	SSS		
									CM4023A	† Solitron		
									(continued)			

† Military Temperature Range (−55°C to 125°C)

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DIGITAL—CMOS (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line			
Gates, AND/NAND (cont)				Gates, AND-OR/AND-OR-Invert (cont)				Gates, Exclusive OR/NOR (cont)						
Triple 3-Input NAND Gate (continued)	CM4023AE	Solitron		Quad AND-OR Select Gate (continued)	MC14519C	Motorola		Quad Exclusive OR Gate (continued)	CD4030A	† RCA				
	SW4023AE	SW				CD4019C		National				see page 375		
	MM54C10	† Teledyne S				CD4019M		† National				CD4030AE	RCA	
	MM74C10	Teledyne S				CD4019A		† RCA				see page 375		
	TF4023A/B	† TI				see page 375						CD4070A/B	† RCA	
	TP4023A/B	TI				CD4019AE		RCA				see page 375		
	TC4023	Toshiba				see page 375						CD4070A/BE	RCA	
	TC7410	Toshiba				HBF4019AE		SGS				see page 375		
						SCL4019A		† SSS				HBF4030AE	SGS	
Quad 2-Input NAND Gate	F4011C	Fairchild	10		SCL4019AE	SSS	60		SCL4030A	† SSS	110			
	F4011M	† Fairchild				CM4019A		† Solitron				SCL4070A	† SSS	
	MEM4011D	† Gl				CM4019AE		Solitron				SCL4070AE	SSS	
	MEM4011P	Gl				SW4019AE		SW				CM4030A	† Solitron	
	HD4011A-2	† Harris				TF4019A		† TI				CM4030AE	Solitron	
	HD4011A-9	Harris				TP4019A		TI				CM4070A/B	† Solitron	
	HD54C00	† Harris				TC4019		Toshiba				CM4070A/BE	Solitron	
	HD74C00	Harris										SW4030AE	SW	
	MC14011A/BA	Motorola †			Quad AND-OR Select Gate, Three-State	CD40257A/B		† RCA	70			MM54C86	† Teledyne S	
	MC14011C/BC	Motorola †			see page 375					MM74C86	Teledyne S			
	CD4011C	National	20		CD40257A/BE	RCA			TF4030A/B	† TI	120			
	CD4011M	† National				see page 375				TP4030A/B		TI		
	MM54C00	† National			Dual 2-Wide 2-Input AND-OR-Invert Gate	F4085C	Fairchild			TF4507		† TI		
	MM74C00	National				F4085M	Fairchild					TP4507	TI	
	CD4011A/B	† RCA				MC14506A	† Motorola					TF4519A	† TI	
	see page 375					MC14506C	Motorola					TP4519A	TI	
	CD4011A/BE	RCA				CD4085A/B	† RCA					TC4030	Toshiba	
	see page 375					see page 375								
	HBF4011AE	SGS				CD4085A/BE	RCA			Quad Exclusive NOR Gate		F4077C	Fairchild	130
	SCL4011A	† SSS			see page 375					F4077M	† Fairchild			
	SCL4011AE	SSS								F4519C	Fairchild			
	CM4011A	† Solitron			4 Wide 2-Input Expandable AND-OR-Invert Gate	F4086C	Fairchild		F4519M	† Fairchild				
	CM4011AE	Solitron				F4086M	† Fairchild		HD14519-2	† Harris				
	SW4011AE	SW				CD4086A/B	† RCA		HD14519-9	Harris				
	MM54C00	† Teledyne S				see page 375			MC14519A	† Motorola				
	MM74C00	Teledyne S				CD4086A/BE	RCA		MC14519C	Motorola				
	TF4011A/B	† TI				see page 375			CD4077A/B	† RCA				
	TP4011A/B	TI							see page 375					
	TF4311A	† TI			Quad 4-2-2-1-Input AND-OR-Invert Gate	TF4302A	TI		CD4077A/BE	RCA				
	TP4311A	TI				TP4302A	TI		see page 375					
	TC4011	Toshiba			Quad 2-4-4-1-Input AND-OR-Invert Gate	TF4303A	TI		CM4077A/B	† Solitron				
	TC7400	Toshiba				TP4303A	TI		CM4077A/BE	Solitron				
Gates, AND-OR/AND-OR-Invert				Gates, Exclusive OR/NOR				Gates, OR/NOR						
Triple AND-OR Bi-Phase Pairs	CD4037A	† RCA	40	Quad Exclusive OR Gate	F4030C	Fairchild	90	Dual 4-Input OR Gate	F4072C	Fairchild	140			
	see page 375					F4030M		† Fairchild				F4072M	† Fairchild	
	CD4037AE	RCA				F4070C		Fairchild				MC14072BA	† Motorola	
	see page 375					F4070M		† Fairchild				MC14072BC	Motorola	
	CM4037A	† Solitron			HD4030A-2	† Harris				CD4072A/B		† RCA		
	CM4037AE	Solitron			see page 266					see page 375				
Quad AND-OR Select Gate	F4019C	Fairchild	50		HD4030A-9	Harris				CD4072A/BE		RCA		
	F4019M	† Fairchild				see page 266						see page 375		
	F4519C	Fairchild				HD54C86		† Harris			SCL4072A	† SSS		
	F4519M	† Fairchild				HD74C86		Harris			SCL4072AE	SSS		
	HD14519-2	† Harris				MC14507A		† Motorola			TC4072	Toshiba		
	HD14519-9	Harris				MC14507C		Motorola						
	HD4019A-2	† Harris				CD4030C		National		triple 3-Input OR Gate	F4075C	Fairchild		
	see page 266					CD4030M		† National			F4075M	† Fairchild		
	HD4019A-9	Harris				CD4070BC	National			MC14075BA	† Motorola			
	see page 266					CD4070BM	† National			MC14075BC	Motorola			
	MC14519A	† Motorola			MM54C86	† National			CD4075A/B	† RCA				
	(continued)				MM74C86	National			see page 375					
					(continued)				(continued)					

† Military Temperature Range (-55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

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DIGITAL—CMOS (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line
Gates, OR/NOR (cont)				Gates, OR/NOR (cont)				Gates, OR/NOR (cont)			
Triple 3-Input OR Gate (continued)				Dual 4-Input NOR Gate (continued)				Quad 2-Input NOR Gate (continued)			
	CD4075A/BE	RCA			CD4002A/B	† RCA			MM54C02	† Teledyne S	
	see page 375				see page 375				MM74C02	Teledyne S	
	SCL4075A	† SSS			CD4002A/BE	RCA			TF4001A/B	† TI	110
	SCL4075AE	SSS			see page 375				TP4001A/B	TI	
	TC4075	Toshiba			HBF4002AE	SGS			TF4301A	† TI	
quad 2-Input OR Gate				Dual 4-Input Expandable NOR Gate				Gates, Miscellaneous			
	F4071C	Fairchild			SCL4002A	† SSS		8-Input Expandable Multifunction Gate			
	F4071M	† Fairchild			CM4002A	† Solitron	60	CD4048C National			
	HD54C32	† Harris			CM4002AE	Solitron		CD4048M † National			
	HD74C32	Harris			SW4002AE	SW		CD4048A † RCA			
	MC14071A/BA	Motorola †			TF4002A/B	† TI		see page 375			
	MC14071C/BC	Motorola	10		TP4002A/B	TI		CD4048AE RCA			
	MM54C32	† National			TC4002	Toshiba		see page 375			
	MM74C32	National		Dual 4-Input Expandable NOR Gate				CD4048AE RCA			
	CD4071A/B	† RCA			SCL4402A	† SSS		see page 375			
	see page 375				SCL4402AE	SSS		SCL4402A † SSS			
	CD4071A/BE	RCA		Triple 3-Input NOR Gate				SCL4402AE SSS			
	see page 375				F4025C	Fairchild		CM4048A † Solitron			
	SCL4071A	† SSS			F4025M	† Fairchild		Solitron			
	SCL4071AE	SSS			HD4025A-2	† Harris		CM4048AE Solitron			
	CM4071A/B	† Solitron			HD4025A-9	Harris		Triple Gate (dual 4-input NAND and 2-input OR/NOR)			
	CM4071A/BE	Solitron			MC14025A/BA	Motorola †	70	MC14501A † Motorola			
	TF4071B	† TI			MC14025C/BC	Motorola		MC14501C Motorola			
	TP4071B	TI	20		CD4025C	National		Hex Function Gate			
	TC4071	Toshiba			CD4025M	† National		MC14572A † Motorola			
8-Input NOR Gate					CD4025A/B	† RCA		MC14572C Motorola			
	F4078C	Fairchild			see page 375			Dual 5-Input Majority Logic Gate			
	F4078M	† Fairchild			CD4025A/BE	RCA		MC14530A † Motorola			
	MC14078BA	† Motorola			see page 375			MC14530C Motorola			
	MC14078BC	Motorola			HBF4025AE	SGS		Latches			
	CD4078A/B	† RCA			SCL4025A	SSS		8-Bit AND Gated Addressable Latch			
	see page 375				SCL4025AE	SSS		F4724C Fairchild			
	CD4078A/BE	RCA			CM4025A	Solitron		F4724M † Fairchild			
	see page 375				CM4025AE	Solitron	80	CD4099A/B † RCA			
	SCL4402A	† SSS			SW4025AE	SW		see page 375			
	SCL4402AE	SSS			TF4025A/B	† TI		CD4099A/BE RCA			
	CM4078A/B	† Solitron	30		TP4025A/B	TI		see page 375			
	CM4078A/BE	Solitron		Quad 2-Input NOR Gate				Quad Clocked "D" Latch			
	TC4078	Toshiba			F4001C	Fairchild		F4042C Fairchild			
Dual 3-Input NOR Gate plus Inverter					F4001M	† Fairchild		F4042M † Fairchild			
	HD4000A-2	† Harris			MEM4001D	† GI		HD4042A-2 † Harris			
	HD4000A-9	Harris			MEM4001P	GI		MC14042A † Motorola			
	MC14000A	† Motorola			HD4001A-2	† Harris		MC14042C Motorola			
	MC14000C	Motorola			HD4001A-9	Harris		CD4042C National			
	CD4000A/B	† RCA			HD54C02	† Harris		CD4042M † National			
	see page 375				HD74C02	Harris		CD4042A/B † RCA			
	CD4000A/BE	RCA			MC14001A/BA	Motorola †	90	see page 375			
	see page 375				MC14001C/BC	Motorola		CD4042A/BE RCA			
	SCL4000A	† SSS			CD4001C	National		see page 375			
	SCL4000AE	SSS	40		CD4001M	† National		HBF4042AE SGS			
	CM4000A	Solitron			MM54C02	† National		N4042B Signetics			
	CM4000AE	Solitron			MM74C02	National		SCL4042A † SSS			
	TF4000A/B	† TI			CD4001A/B	† RCA		SCL4042AE SSS			
	TP4000A/B	TI			see page 375			CM4042A † Solitron			
Dual 4-Input NOR Gate					CD4001A/BE	RCA	100	CM4042AE Solitron			
	F4002C	Fairchild			see page 375			TF4042A/B † TI			
	F4002M	† Fairchild			HBF4001AE	SGS		TP4042A/B TI			
	HD4002A-2	† Harris			SCL4001A	† SSS		TC4042 Toshiba			
	HD4002A-9	Harris			SCL4001AE	SSS		Quad NAND R/S Latch			
	MC14002A/BA	Motorola †			CM4001A	† Solitron		F4044C Fairchild			
	MC14002C/BC	Motorola	50		CM4001AE	Solitron		F4044M † Fairchild			
	CD4002C	National			SW4001AE	SW		HD4044A-2 † Harris			
	CD4002M	† National			(continued)			HD4044A-9 Harris			
	(continued)							MC14044BA † Motorola			
								(continued)			

† Military Temperature Range (-55°C to 125°C)

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DIGITAL—CMOS (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line		
Latches (cont)				Memories (cont)				Memories (cont)					
Quad NAND R/S Latch (continued)	MC14044BC CD4044C CD4044M CD4044A/B CD4044A/BE SCL4044A SCL4044AE CM4044A TF4044A/B TP4044A/B TC4044	Motorola National † National † RCA RCA † SSS SSS † Solitron † TI TI Toshiba	10	16-Bit Multiport Register File (4x4 Read While Write RAM)	MC14580A MC14580C CD40108A/B CD40108A/BE SCL4580	† Motorola Motorola † RCA RCA SSS	50	512-Bit RAM (512x1) (continued)	2222 2222A N2222 S2222	Nortec Nortec Signetics † Signetics			
Quad NAND Latch	TF4376B TP4376B	† TI TI		64-Bit CAM (8x8 Content Addressable Memory)	SCM5533	† SSS		1,024-Bit RAM (256x4)	S5101 F4721 5101 M5101-4 MWS5040 MWS5540 MW7040 SCM5501S	AMI Fairchild Intel † Intel RCA RCA RCA † SSS	100		
Quad NOR R/S Latch	F4043C F4043M HD4043A-2 HD4043A-9 MC14043BA MC14043BC CD4043C CD4043M CD4043A/B CD4043A/BE SCL4043A SCL4043AE CM4043A CM4043AE TF4043A/B TP4043A/B TC4043	Fairchild † Fairchild † Harris Harris † Motorola Motorola National † National † RCA RCA † SSS SSS † Solitron Solitron † TI TI Toshiba	20	32-Bit RAM (Direct Word Line Addressing)	CD4039A CD4039AE CM4039A CM4039AE	† RCA RCA † Solitron Solitron		1,024-Bit RAM (1,024x1)	IM6508C IM6508M IM6518C IM6518M MWS5001 MWS5501 MWS5002 MWS5502 MW7001I SCM5502S SY5101 TC5006	Intersil † Intersil Intersil Intersil RCA RCA RCA RCA RCA † SSS Synertek Toshiba	110		
Quad NOR Latch	TF4377B TP4377B	† TI TI		32-Bit RAM (Binary Addressing)	CD4036A CD4036AE CM4036A CM4036AE	† RCA RCA † Solitron † Solitron	60	64-Bit RAM (64x1)	MCM14505A MCM14505C	† Motorola Motorola			
Dual 4-Bit Latch	MC14508A MC14508C CD4508A/B CD4508A/BE CM4508B CM4508BE TC4508	† Motorola Motorola † RCA RCA † Solitron Solitron Toshiba		64-Bit RAM (16x4)	F4725C F4725M HD54/74C89 MM54C89 MM74C89 SCL5589 MM54C89 MM74C89	Fairchild † Fairchild † Harris † National National † SSS † Teledyne S Teledyne S	70	64-Bit RAM (16x4 clocked RAM, three state output register)	F4710	Fairchild			
Dual 4-Bit Addressable Latch	F4723	Fairchild	40	256-Bit RAM (256x1)	F4720 HD54/74C200 IM6523 MCM14537A MCM14537C MM54C200 MM74C200 CD4061A CD40061AE CD40061 SCM5520S MM54C200 MM74C200 TC4061	Fairchild † Harris † Intersil † Motorola Motorola † National National † RCA RCA RCA † SSS † Teledyne S Teledyne S Toshiba	80	1,024-Bit ROM (256x4)	MCM14524A MCM14524C TC5007	† Motorola Motorola Toshiba	120		
Memories				Multiplexers, Digital				Multiplexers, Digital					
For additional information see Master Selection Guide - Memory Sections.				See also Interface—Analog Switches				See also Interface—Analog Switches					
16-Bit FIFO (4x4)	CD40105B CD40105BE	† RCA RCA		Quad 2-Input Multiplexer	F4519C F4519M HD14519-2 HD14519-9 HD54C157 HD74C157 MC14519A MC14519C MM54C157 MM74C157 MM54C157 MM74C157 TF4519A TP4519A	† RCA RCA † Harris Harris † Harris Harris † Motorola Motorola † National National † Teledyne S Teledyne S † TI TI		Dual 4-Channel Digital Multiplexer	F4539C F4539M MC14539A MC14539C TC4539	Fairchild † Fairchild † Harris Harris † Harris Harris † Motorola Motorola † National National † Teledyne S Teledyne S † TI TI	130		
64-Bit FIFO (16x4)	F4703C F4703M	Fairchild † Fairchild		256-Bit RAM (64x4)	MCM14552A MCM14552C MM54C910 MM74C910 SCM5555D	† Motorola Motorola † National National SSS	90	Dual 4-Channel Digital Multiplexer	F4539C F4539M MC14539A MC14539C TC4539	Fairchild † Fairchild † Motorola Motorola Toshiba	140		
64-Bit Program Stack (16x4 FIFO)	F4706C F4706M	Fairchild † Fairchild		512-Bit RAM (512x1)	S2222 S2222A	AMI AMI							

† Military Temperature Range (-55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

DIGITAL—CMOS (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line	
Multiplexers, Digital (cont)				Oscillators/Dividers (cont)				Shift Registers (cont)				
8-Channel Data Selector				Oscillator/2 ³ Divider (2-5v supplies)				4-Bit Parallel In/Parallel Out Shift Register (continued)				
	F4512C	Fairchild			7209	Intersil			TP4035A/B	TI		
	F4512M	† Fairchild		Oscillator/2 ⁹ Divider					TC4035	Toshiba		
	HD14512-2	† Harris			5801	Intel		4-Bit Parallel Shift Register				
	HD14512-9	Harris			5016	Nortec			F40195C	Fairchild		
	MC14512A	† Motorola		Oscillator/2 ¹¹ to 2 ¹⁹ Divider				50		F40195M	† Fairchild	
	MC14512C	Motorola			MC14451	Motorola			HD54/74C195	† Harris		
	SCL4512A	† SSS		Oscillator/2 ¹³ and 2 ¹⁵ Divider (2-5v supplies)						see page 266		
	SCL4512AE	SSS			7038A	Intersil		4-Bit Bidirectional Shift Register				
	TF4512	† TI		Oscillator/2 ¹³ and 2 ¹⁷ Divider (Also 2 ¹⁷ x10, 2-5v supplies)						F40194C	Fairchild	
	TP4512	TI	10		7213	Intersil			F40194M	† Fairchild		
	TC4512	Toshiba		Oscillator/2 ¹⁶ Divider/Buffer						HD54/74C95	† Harris	
8-Channel Digital Multiplexer					MC14450	Motorola			see page 266			
	HD54C151	† Harris			SCL5411	SSS			MC14194BA	† Motorola		
	see page 266			Oscillator/2 ²¹ Divider/Buffer						MC14194BC	Motorola	
	HD74C151	Harris			CD4045A	† RCA			MM54C95	National		
	see page 266				see page 375				MM74C95	† National		
	MM54C151	† National			CD4045AE	RCA			MM54C195	† National		
	MM74C151	National			see page 375				MM74C195	† Teledyne S		
	MM54C151	† Teledyne S			HBF4045AE	SGS			MM74C195	Teledyne S		
	MM74C151	Teledyne S			SCL4445A	† SSS	60					
Dual 8-Channel Digital Multiplexer					SCL4445AE	SSS						
	TF4321A	† TI			CM4045A	† Solitron						
	TP4321A	TI			Solitron							
16-Channel Digital Multiplexer					Oscillator/2 ²² Divider (with 1 second and 1 minute pulses using 4.193 MHz crystal, 2-5v supplies)							
	TF4320A	† TI	20		7213	Intersil			CD40194A/B	† RCA		
	TP4320A	TI		Oscillator/2 ²³ Divider						see page 375		
Multivibrators					SCL5419	SSS			CD40194A/BE	RCA		
Monostable/Astable Multivibrator					Oscillator/2 ²⁴ Divider					see page 375		
	F4047C	Fairchild			HD14521-2	† Harris			MM54C95	† Teledyne S		
	F4047M	† Fairchild			HD14521-9	Harris			MM74C95	Teledyne S		
	CD4047A	† RCA			MC14521A	† Motorola						
	see page 375				MC14521C	Motorola						
	CD4047AE	RCA		Frequency Divider (9-Stage)								
	see page 375				SCL5425A	SSS						
	CM4047A	† Solitron			SCL5427A	SSS	70					
	CM4047AE	Solitron			SCL5437A	SSS						
	TC4047	Toshiba		Divider, divide by 5/6								
Dual Monostable Multivibrator					RED5/6	LSI Comp						
	F4528C	Fairchild		Divider, divide by 6								
	F4528M	† Fairchild			D6	LSI Comp						
	HD14528-2	† Harris		Divider, divide by 50/60								
	HD14528-9	Harris			RED50/60	LSI Comp						
	HD54C221	† Harris		Divider, divide by 60								
	HD74C221	Harris			D60	LSI Comp						
	MC14528A	† Motorola		Divider, divide by 3000/3600								
	MC14528C	Motorola	30		RED3000/3600	LSI Comp						
	MM54C221	† National		Divider, divide by 3600								
	MM74C221	National			D3600	LSI Comp						
	CD4098A/B	† RCA		Shift Registers								
	see page 375			4-Bit Parallel In/Parallel Out Shift Register								
	CD4098A/BE	RCA			F4035C	Fairchild						
	see page 375				F4035M	† Fairchild						
	SCL4528A	† SSS			HD4035A-2	† Harris						
	SCL4528AE	SSS			see page 266							
	TC4528	Toshiba			HD4035A-9	Harris						
Oscillators/Dividers					see page 266							
Oscillator/Divider (Programmable Timer)					MC14035A	† Motorola	80					
	MC14541A	† Motorola			MC14035C	Motorola						
	MC14541C	Motorola			CD4035C	National						
Clock Generator, Oscillator to 10MHz, 8:1 divider, for microprocessors					CD4035M	† National						
	ICM7209	† Intersil			CD4035A	† RCA						
					see page 375							
					CD4035AE	RCA						
					see page 375							
					HBF4035AE	SGS						
					SCL4035A	† SSS	90					
					SCL4035AE	SSS						
					CM4035A	† Solitron						
					CM4035AE	Solitron						
					TF4035A/B	† TI						
					(continued)							

† Military Temperature Range (-55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

DIGITAL—CMOS (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line				
Shift Registers (cont)				Shift Registers (cont)				Translators (cont)							
8-Bit Synchronous Parallel In/Serial Out Shift Register (continued)	CD4014C	National	10	8-Bit Bidirectional Parallel/Serial Input/Output Bus Register (continued)	TC4034	Toshiba	60	Quad Voltage Up Level Translator (continued)	MEM4900P	GI	100				
	CD4014M	† National			CD4094A/B	† RCA			CM4104A	† Solitron		CD40109A/B	† RCA		
	CD4014A	† RCA		see page 375	CD4094A/BE	RCA	CM4104AE	Solitron	see page 375	CD40109A/BE	RCA				
	CD4014AE	RCA		see page 375	18-Bit Static Shift Register	F4006C	Fairchild	60	Quad Level Shifter (low to high voltage)	CD40109A/B	† RCA	110			
	HBF4014AE	SGS		M5612		† Ragen	see page 375			HD54C901	† Harris				
	SCL4014A	† SSS		SCL4006A		† SSS	CD4006A		† RCA	see page 375	HD74C901	Harris			
	SCL4014AE	SSS		SCL4006AE		SSS	CD4006AE		RCA	see page 375	MM54C901	† National			
	CM4014A	† Solitron		CM4006A		† Solitron	CD4006M		† National	Hex TTL Buffer (Non-Inverting) (CMOS To TTL)	HD54C902	† Harris			
	CM4014AE	Solitron		CM4006AE		Solitron	CD4006A		† RCA		see page 375	HD74C902	Harris		
	TF4014A/B	† TI		CD4006A		† Solitron	CD4006AE		RCA	see page 375	MM54C902	† National			
	TP4014A/B	TI		CM4006A		† Solitron	CD4006M		† National	Hex PMOS Buffer (Inverting) (PMOS To CMOS or TTL)	MM74C902	National			
	TC4014	Toshiba		CM4006AE		Solitron	CD4006A		† RCA		see page 375	HD54C903	† Harris		
	8-Bit (Asynchronous parallel or synchronous serial operation) Parallel In/Serial Out Shift Register	F4021C		Fairchild		20	32-Bit Bidirectional Serial In/Serial Out Shift Register		CD40100A/B	† RCA	70	Hex PMOS Buffer (Non-Inverting) (PMOS To CMOS or TTL)	HD54C904	† Harris	110
		F4021M		† Fairchild					CD40100A/BE	RCA			HD74C904	Harris	
HD4021A-2		† Harris	see page 266	64-Bit Static Shift Register			F4031C		Fairchild	80	HNIL/HTL is Suitable for Translation/input protection. See HNIL/HTL section	MM54C903	† National		
HD4021A-9		Harris	see page 266				F4031M		† Fairchild			MM74C903	National		
MC14021A		† Motorola	MC14021C	Motorola			MC14557A		† Motorola	Dual 64-Bit Static Shift Register	Phase-Locked Loop	F4046C	Fairchild	120	
CD4021C		National	CD4021M	† National	MC14557C		Motorola	F4046M	† Fairchild						
CD4021A		† RCA	see page 375	CD4021A	† Solitron		CD4031C	National	MC14046A		† Motorola				
CD4021AE		RCA	see page 375	CM4021A	Solitron		CD4031M	† National	MC14046C		Motorola				
SCL4021A		† SSS	SCL4021AE	SSS	CD4031A		† RCA	see page 375	CD4046A		† RCA				
CM4021A		† Solitron	CM4021AE	Solitron	CD4031AE		RCA	see page 375	see page 375		CD4046AE	RCA			
CM4021AE		Solitron	SW4021AE	SW	CD4031M		† National	see page 375	SCL4046A		† SSS				
SW4021AE		SW	TF4021A/B	† TI	CD4031A		† RCA	see page 375	SCL4046AE		SSS				
TF4021A/B		† TI	TP4021A/B	TI	CD4031AE		RCA	see page 375	SCL4446		SSS				
TP4021A/B		TI	TC4021	Toshiba	CD4062A		† RCA	see page 375	CMOS Transistor Array (See also 4007 Dual Complementary Pair and Inverter-listed under Buffers/Inverters)		CA3600E	† RCA			
TC4021	Toshiba	30	200 Bit Dynamic Shift Register	MC14517A	† Motorola	Quad 64-Bit Static Shift Register, Separate Clock	Hex Contact Bounce Eliminator	MC14490			Motorola				
8-Bit Serial In/Parallel Out Shift Register	HD54/74C164	† Harris	30	MC14517C	Motorola			128-Bit Static Shift Register	8-Bit Priority Encoder		MC14490E	† Motorola			
	MM54C164	† National		SCL4517	SSS	MC14562A	† Motorola				Binary Rate Multiplier	CD4089A/B	† RCA		
	MM74C164	National		MM74C164	Teledyne S	MC14562C	Motorola	96-Bit Variable Length Elastic Shift Register	see page 375			see page 375			
	MM54C164	† Teledyne S		MM74C164	Teledyne S	200 Bit Dynamic Shift Register	CD4062A		† RCA	128-Bit Static Shift Register, W/Control Logic		F4532C	Fairchild		
	MM74C164	Teledyne S		80	CD4062AE		RCA	see page 375	250-Bit Variable Length Dynamic Shift Register			F4532M	† Fairchild		
	8-Bit Parallel In/Serial Out Shift Register	HD54/74C165		† Harris	40	Quad 64-Bit Static Shift Register, Separate Clock	F4731	Fairchild		90		8-Bit Priority Encoder	MC14532A	† Motorola	
		MM54C165		† National			64-Bit Variable Length Shift Register	MC14557A	† Motorola				250-Bit Variable Length Dynamic Shift Register	MC14532C	Motorola
		MM74C165		National		MC14557C	Motorola	MS618	† Ragen	CD4532A/B		† RCA			
		8-Bit Bidirectional Parallel/Serial Input/Output Bus Register		F4034C		Fairchild	50	96-Bit Variable Length Elastic Shift Register	MS618			† Ragen	see page 375	CD4532A/BE	RCA
				F4034M		† Fairchild			128-Bit Static Shift Register, W/Control Logic	MS625		† Ragen			see page 375
				MC14034A		† Motorola		250-Bit Variable Length Dynamic Shift Register		SC370		Siliconix	50	Binary Rate Multiplier	
				MC14034C		Motorola			Translators	Quad Voltage Up Level Translator		F4104C			Fairchild
				SCL4034A		† SSS		F4104M				† Fairchild	MEM4900D	† GI	CD4089A/BE
				SCL4034AE		SSS		CD4034A	† RCA	(continued)		(continued)	see page 375	see page 375	
CM4034A			† Solitron	CD4034AE		Solitron									
CM4034AE			Solitron	see page 375		50									
CD4034A			† RCA	see page 375											
CD4034AE			RCA	see page 375											
(continued)				(continued)											

† Military Temperature Range (–55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

DIGITAL—CMOS (cont)

Function	Device	Source	Line	Function	Device	Source	Line
Miscellaneous (cont)				Miscellaneous (cont)			
BCD Rate Multiplier	HD14527-2	† Harris		Hex Schmitt Trigger (continued)	MM54C14	† National	
	HD14527-9	Harris			MM54C914	† National	
	MC14527A	† Motorola			MM74C14	National	
	MC14527C	Motorola			MM74C914	National	
	CD4527A/B	† RCA			TF4304A	† TI	
	see page 375				TP4304A	TI	
	CD4527A/BE	RCA	60	Quad 2-Input NAND Schmitt Trigger	CD4093A/B	† RCA	
	see page 375				see page 375	CD4093A/BE	RCA
Bit Rate Generator	F4702C	Fairchild	10	Binary to Pulse Converter	MC14408	Motorola	
	F4702M	† Fairchild			MC14409	Motorola	
	MC14411	Motorola					
Dual Differential Line Driver	HD88C30	Harris		Modem (0-600 bps)	MC14412	Motorola	
	MM78C30	† National					
	MM88C30	National					
Quad Single Ended Line Driver	HD88C29	Harris		Tone Encoder (4x4 input, 2 Outputs)	MC14410	Motorola	
	MM78C29	† National					
	MM88C29	National					
Dual Line Receiver	MM78C20	† National		2 of 8 Keyboard to Binary Encoder	MC14419	Motorola	
	MM88C20	National					
Successive Approximation Register	HD54C905	† Harris	20	Programmable Timer	MC14536A	† Motorola	
	HD74C905	Harris			MC14536C	Motorola	
	MC14559A	† Motorola			MC14541A	† Motorola	
	MC14559C	Motorola			MC14541C	Motorola	
	MM54C905	† National					
	MM74C905	National					
Successive Approximation Register, Cascadable	MC14549A	† Motorola		Quad Precision Timer/Driver (Inputs cause outputs to switch state for 100 clock pulses)	MC14415	Motorola	
	MC14549C	Motorola			MC14415E	† Motorola	
Digital Logic (for 3½ digit A/D Systems)	MC14435	Motorola		Standardized CMOS Array, to build custom circuits by changing final metalization	MasterMOS	IMI	
	MC14435E	† Motorola			MonochipM	Interdesign	
9-Bit Parity Generator and Checker	CD40101A/B	† RCA	30	Low voltage CMOS devices (Counters, Display Drivers, Counter-Timers) not usually mixed with 5-20v CMOS logic are listed under Digital-Special			
	see page 375						
	CD40101A/BE	RCA					
	see page 375						
12-Bit Parity Tree	F4531C	Fairchild					
	F4531M	† Fairchild					
	MC14531A	† Motorola					
	MC14531C	Motorola					
	SCL4531A	SSS					
	TF4531A	† TI					
Dual Schmitt Trigger	MC14583A	† Motorola	40				
	MC14583C	Motorola					
	TC4583	Toshiba					
Quad Schmitt Trigger	HD54C909	† Harris					
	HD74C909	Harris					
	MM54C909	† National					
	MM74C909	National					
Hex Schmitt Trigger	F40014C	Fairchild	50				
	F40014M	† Fairchild					
	HD54C14	† Harris					
	HD54C914	† Harris					
	HD74C14	Harris					
	HD74C914	Harris					
	CD40106BC	National					
	CD40106BM	† National					
(continued)							

† Military Temperature Range (–55°C to 125°C)

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DIGITAL—ECL

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line
ECL-10000 Series				Counters, Decade (cont)				Flip-Flops (cont)			
The ECL-10000, 95000, 100K and III - Series are presented as separate groups in that sequence.				Decade Counter				Dual "D" Master-Slave Flip-Flop (continued)			
				F10010C Fairchild				HD10131 Hitachi			
				F10010M † Fairchild				MC10131 Motorola			
				Universal Decade Counter				MC10231 Motorola 100			
				F10137 Fairchild				MC10531 † Motorola			
				MC10137 Motorola				MC10631 † Motorola			
				MC10537 † Motorola 50				SP10131 Plessey			
				SP10137 Plessey				10131 Signetics			
				10137 Signetics				10231 Signetics			
				SN10137 TI				SN10131 TI			
								SN10231 TI			
Arithmetic Functions				Decoders				Quad "D" Master-Slave Flip-Flop (with Common Reset)			
Dual High Speed Adder/Subtractor				Binary to 1-8 Decoder (High)				SN10304 TI			
F10180 Fairchild				F10162 Fairchild							
F10580 † Fairchild				F10562 † Fairchild				Hex "D" Master-Slave Flip-Flop			
HD10180 Hitachi				HD10162 Hitachi				F10176 Fairchild			
MC10180 Motorola				MC10162 Motorola				F10576 † Fairchild 110			
10180 Signetics				MC10562 † Motorola				MC10176 Motorola			
MC10580 † Motorola				SP10162 Plessey				MC10576 † Motorola			
SN10180 TI				10162 Signetics				10176 Signetics			
				SN10162 TI				SN10176 TI			
2-Bit Arithmetic Logic Unit/Function Generator				Binary to 1-8 Decoder (Low)				Hex "D" Master-Slave Flip-Flop (With Common Reset)			
MC10182 Motorola				F10161 Fairchild				F10186 Fairchild			
				F10561 † Fairchild				F10586 † Fairchild			
4-Bit Arithmetic Logic Unit/Function Generator				HD10161 Hitachi				MC10186 Motorola			
F10181 Fairchild				MC10161 Motorola				10186 Signetics			
F10581 † Fairchild				MC10561 † Motorola							
HD10181 Hitachi				SP10161 Plessey				Dual "J-K" Master-Slave Flip-Flop			
MC10181 Motorola				10161 Signetics				SN10302 TI			
MC10581 † Motorola				SN10161 TI				Dual "J-K" Master-Slave Flip-Flop			
10181 Signetics								F10135 Fairchild			
SN10181 TI								F10535 † Fairchild			
								MC10135 Motorola			
2-Bit Multiplier, High Speed				Dual Binary to 1-4 Decoder (High)				MC10535 † Motorola			
MC10287 Motorola				F10172 Fairchild				10135 Signetics			
				F10572 † Fairchild							
4x2-Bit Multiplier				MC10172 Motorola				Quad 2-Input Gate (3 AND, 1 AND/NAND)			
MC10183 Motorola				MC10572 † Motorola				F10104 Fairchild			
				SP10172 Plessey				F10509 † Fairchild			
Look-Ahead Carry Circuit				SP10161 Plessey				HD10104 Hitachi			
F10179 Fairchild				10161 Signetics				MC10104 Motorola			
F10579 † Fairchild				SN10161 TI				MC10504 † Motorola			
HD10179 Hitachi								10104 Signetics			
MC10179 Motorola								SN10104 TI			
MC10579 † Motorola											
10179 Signetics											
SN10179 TI											
5-Bit Comparator				Dual Binary to 1-4 Decoder (Low)				Gates, AND/NAND			
F10166 Fairchild				F10171 Fairchild				Hex AND Gate			
F10566 † Fairchild				F10571 † Fairchild				MC10197 Motorola			
MC10166 Motorola				MC10171 Motorola				Dual 4-Input AND/NAND Gate			
				MC10571 † Motorola				10108 Signetics			
				SP10171 Plessey				SN10108 TI			
				10171 Signetics							
				SN10171 TI							
Buffers				Drivers							
Hex Buffer				Dual TTL/MST Bus Driver							
10188 Signetics				MC10128 Motorola							
Hex Inverter				10128 Signetics							
10189 Signetics				Triple 4-3-3 Input Bus Driver							
Hex Inverter/Buffer				F10123 Fairchild							
MC10195 Motorola				F10523 † Fairchild							
10195 Signetics				MC10123 Motorola							
				MC10523 † Motorola							
				10123 Signetics							
				SN10123 TI							
Counters, Binary				Quad Bus Driver				Gates, Exclusive OR/NOR			
4-Bit Binary Counter				F10192 Fairchild				Quad Exclusive OR Gate			
F10016C Fairchild				10192 Signetics				F10113 Fairchild			
F10016M † Fairchild								F10513 † Fairchild			
MC10178 Motorola								MC10113 Motorola			
10178 Signetics								10113 Signetics			
								SN10113 TI			
4-Bit Universal Binary Counter								Triple 2-Input Exclusive OR/NOR Gate			
F10136 Fairchild								F10507 † Fairchild			
HD10136 Hitachi								HD10107 Hitachi			
MC10136 Motorola								F10107 Fairchild			
MC10536 † Motorola								MC10107 Motorola			
SP10136 Plessey								MC10507 † Motorola			
10136 Signetics								SP10107 Plessey			
SN10136 TI								10107 Signetics			
								SN10107 TI			
Counters, Decade				Flip-Flops							
Bi-Quinary Counter				Dual "D" Master-Slave Flip-Flop							
MC10138 Motorola				F10131 Fairchild							
10138 Signetics				F10231 Fairchild							
				F10531 † Fairchild							
				F10631 † Fairchild							
				(continued)							

† Military Temperature Range (-55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

DIGITAL—ECL (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line
Gates, OR/NOR				Gates, OR/NOR (cont)				Gates, OR-AND/OR-AND-Invert (cont)			
(Sequence OR, NOR, OR/NOR, Combinations)				Triple 2-3-2 Input OR/NOR Gate				4-Wide 3-Input OR-AND/OR-AND-Invert Gate (continued)			
Dual 3-Input 3-Output OR Gate (Line Driver)				F10105 Fairchild				SN10121 TI			
F10210 Fairchild				F10505 † Fairchild				Dual 2-Wide 2-3 Input OR-AND/OR-AND-Inverter Gate			
F10510 † Fairchild				HD10105 Hitachi				F10117 Fairchild			
F10610 † Fairchild				MC10105 Motorola				F10517 † Fairchild			
HD10110 Hitachi				MC10505 † Motorola				HD10117 Hitachi			
MC10110 Motorola				DM10105 National				MC10117 Motorola			
MC10210 Motorola				SP10105 Plessey				MC10517 † Motorola			
SP10110 Plessey				10105 Signetics				DM10117 National			
10110 Signetics				SN10105 TI				SP10117 Plessey			
10210 Signetics				Quad 2-Input OR/NOR Gate (One Input Common)				10117 Signetics			
SN10110 TI				F10101 Fairchild				SN10117 TI			
SN10210 TI				F10501 † Fairchild				Latches			
Dual 3-Input 3-Output NOR Gate (Line Driver)				HD10101 Hitachi				Dual "D" Clocked Latch			
F10111 Fairchild				MC10101 Motorola				F10130 Fairchild			
F10211 Fairchild				MC10501 † Motorola				F10530 † Fairchild			
F10511 † Fairchild				SP10101 Plessey				HD10130 Hitachi			
F10611 † Fairchild				10101 Signetics				MC10130 Motorola			
HD10111 Hitachi				SN10101 TI				MC10530 † Motorola			
MC10111 Motorola				Quad 2-Input Gate (3 OR, 1 OR/NOR)				SP10130 Plessey			
MC10211 Motorola				F10103 Fairchild				10130 Signetics			
DM10111 National				F10503 † Fairchild				SN10130 TI			
SP10111 Plessey				MC10103 Motorola				Quad "D" Latch, Gated Output; Active High Enable			
10111 Signetics				SP10103 Plessey				F10133 Fairchild			
10211 Signetics				10103 Signetics				F10533 † Fairchild			
SN10111 TI				SN10103 TI				HD10133 Hitachi			
SN10211 TI				Quad 2-Input Gate (3 NOR, 1 OR/NOR)				MC10133 Motorola			
Triple 4-3-3 Input NOR Gate				F10102 Fairchild				MC10533 † Motorola			
F10106 Fairchild				F10502 † Fairchild				10133 Signetics			
F10506 † Fairchild				HD10102 Hitachi				SN10133 TI			
HD10106 Hitachi				MC10102 Motorola				Quad "D" Latch, Gated Output, Active Low Enable			
MC10106 Motorola				MC10502 † Motorola				F10153 Fairchild			
MC10506 † Motorola				SP10102 Plessey				F10553 † Fairchild			
DM10106 National				10102 Signetics				MC10153 Motorola			
SP10106 Plessey				SN10102 TI				SN10153 TI			
10106 Signetics				Gates, OR-AND/OR-AND-Invert				Quad Latch, Common Clock, Separate Output Enable			
SN10106 TI				4-Wide 4-3-3 Input OR-AND Gate				F10168 Fairchild			
Quad 3-Input NOR Gate (One Input Common)				F10119 Fairchild				F10568 † Fairchild			
F10100 Fairchild				F10519 † Fairchild				MC10168 Motorola			
MC10100 Motorola				HD10119 Hitachi				SN10168 TI			
SP10100 Plessey				MC10119 Motorola				Quint Latch			
10100 Signetics				MC10519 † Motorola				F10175 Fairchild			
SN10100 TI				MC10519 Motorola				F10575 † Fairchild			
Dual 3-Input 3-Output (1 OR, 2 NOR) Gate (Line Driver)				DM10119 National				HD10175 Hitachi			
F10212 Fairchild				SP10119 Plessey				MC10175 Motorola			
MC10212 Motorola				10119 Signetics				MC10575 † Motorola			
DM10112 National				SN10119 TI				10175 Signetics			
SP10112 Plessey				Dual 2-Wide 3-Input OR-AND Gate				SN10175 TI			
10112 Signetics				F10118 Fairchild				Dual 2 to 1 Multiplexer-Latch, Common Reset			
10212 Signetics				F10518 † Fairchild				F10132 Fairchild			
SN10112 TI				HD10118 Hitachi				F10532 † Fairchild			
SN10212 TI				MC10118 Motorola				HD10132 Hitachi			
Dual 4-5 Input OR/NOR Gate				MC10518 † Motorola				MC10132 Motorola			
F10109 Fairchild				DM10118 National				10132 Signetics			
F10509 † Fairchild				SP10118 Plessey				SN10132 TI			
HD10109 Hitachi				10118 Signetics				Dual 2 to 1 Multiplexer-Latch			
MC10109 Motorola				SN10118 TI				F10134 Fairchild			
MC10509 † Motorola				4-Wide 3-Input OR-AND/OR-AND-Invert Gate				F10534 † Fairchild			
DM10109 National				F10121 Fairchild				HD10134 Hitachi			
SP10109 Plessey				F10521 † Fairchild				MC10134 Motorola			
10109 Signetics				HD10121 Hitachi				10134 Signetics			
SN10109 TI				MC10121 Motorola				SN10134 TI			
				MC10521 † Motorola				Quad 2-Input Multiplexer-Latch			
				DM10121 National				F10173 Fairchild			
				10121 Signetics				F10573 † Fairchild			
				(continued)				MC10173 Motorola			
								(continued)			

† Military Temperature Range (-55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

DIGITAL—ECL (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line
Latches (cont)				Multiplexers (cont)				Miscellaneous (cont)			
Quad 2-Input Multiplexer-Latch (continued)	10173 SN10173	Signetics TI		Quad 2 to 1 Multiplexer (Non-inverting)	F10158 F10558 MC10158 10158 SN10158	Fairchild † Fairchild Motorola Signetics TI		Triple Differential Line Receiver (continued)	HD10116 MC10114 MC10116 MC10216 MC10516 MC10514 MC10616 DM10116 10114 10116 10216 SN10114 SN10116 SN10216	Hitachi Motorola Motorola Motorola † Motorola † Motorola National Signetics Signetics Signetics TI TI TI	110
Memories				Quad 2 to 1 Multiplexer (Inverting With Enable)	F10159 F10559 MC10159 10159 SN10159	Fairchild † Fairchild Motorola Signetics TI	60	Quad Differential Line Receiver	F10115 F10515 MC10115 MC10515 DM10115 SP10115 10115 SN10115	Fairchild † Fairchild Motorola † Motorola National Plessey Signetics TI	120
For additional information, see Master Selection Guide—Memory sections				Shift Registers				Quad Bus Receiver	MC10129 10129	Motorola Signetics	
RAM (8x2) Simultaneous Read-Write	MCM10143	Motorola		4-Bit Shift Register	F10000C F10000M	Fairchild † Fairchild		Dual Simultaneous Bus Transceiver	MC10194	Motorola	
RAM (16x4)	F10145AC F10545AM HD10145 MCM10145 10145 SN10145	Fairchild † Fairchild Hitachi Motorola Signetics TI	10	4-Bit Universal Shift Register	F10141 MC10141 MC10541 10141 SN10141	Fairchild Motorola † Motorola Signetics TI		8-Input Priority Encoder	F10165 F10565 HD10165 MC10165 10165	Fairchild † Fairchild Hitachi Motorola Signetics	130
RAM (64x 1)	MCM10142 SN10142	Motorola TI		4-Bit Universal Shift Register, with Reset	SN10303	TI		9-Bit Parity Circuit (2 Carry Inputs)	F10170 F10570 MC10170 10170	Fairchild † Fairchild Motorola Signetics	
RAM (64x1) 50 Ohm Drive	HD10148 MCM10148 10148 SN10148	Hitachi Motorola Signetics TI		Translators				12-Bit Parity Generator/Checker	F10160 F10560 HD10160 MC10160 MC10560 10160 SN10160	Fairchild † Fairchild Hitachi Motorola † Motorola Signetics TI	140
RAM (64x1) 90 Ohm Drive	MCM10140 10140 SN10140	Motorola Signetics TI		Dual ECL to MOS Translator	10127	Signetics	70	Error Detection/Correction Circuit	MC10163 MC10193	Motorola Motorola	
RAM (64x1) Read-while-Write	10151	Signetics	20	Dual ECL to MOS/TTL Translator	MC75358 MC75368 SN75358	Motorola Motorola TI		Active Terminator	F10014	Fairchild	
RAM (128x1)	F10405C MCM10147 SN10147	Fairchild Motorola TI		Triple ECL to NMOS Translator	MC10177 SN10177	Motorola TI					
RAM (256x1)	F10410C MCM10144 10144 RC10144 R10144 SN10144	Fairchild Motorola Signetics Raytheon Raytheon TI		Quintuple ECL to MST Translator	SN10184	TI					
RAM (1024x1)	F10415C 10146	Fairchild Signetics	30	Hex ECL to MST Translator	MC10191 10191	Motorola Signetics					
PROM (32x8)	10139 see page 831 SN10139	Signetics TI		Quad ECL to TTL Translator (Differential Input)	F10125 F10525 HD10125 MC10125 MC10525 10125 SN10125	Fairchild † Fairchild Hitachi Motorola † Motorola Signetics TI	80				
PROM (256x4)	F10416 10149 MCM10149 10149	Fairchild MMI Motorola Signetics		Quad Differential Receiver/MST to ECL Translator	MC10190 10190	Motorola Signetics					
Multiplexers				Hex MST to ECL Translator	SN10185	TI					
8 to 1 Multiplexer	F10164 F10564 HD10164 MC10164 MC10564 10164 SN10164	Fairchild † Fairchild Hitachi Motorola † Motorola Signetics TI	40	Quad TTL to ECL OR/NOR Translator	F10124 F10524 HD10124 MC10124 MC10524 DM10124 SP10124 10124 SN10124	Fairchild † Fairchild Hitachi Motorola † Motorola National Plessey Signetics TI	90				
Dual 4 to 1 Multiplexer	F10174 F10574 HD10174 MC10174 10174 SN10174 MC10574	Fairchild † Fairchild Hitachi Motorola Signetics TI † Motorola	50	Miscellaneous				Triple Differential Line Receiver	F10114 F10116 F10514 F10516 (continued)	Fairchild Fairchild † Fairchild † Fairchild	100

† Military Temperature Range (–55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

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DIGITAL—ECL (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line	
ECL-95000 Series				Translators				ECL—100K Series				
Counters				Miscellaneous				Arithmetic Functions				
Binary Counter	F95016	Fairchild		Quad TTL to ECL OR/NOR Translator	F95124	Fairchild		4-Bit Binary/Decade Arithmetic Logic Unit	F100181	Fairchild		
Decade Counter	F95010	Fairchild		Triple Differential Line Receiver	F95116	Fairchild		Counters				
Flip-Flops				Quad Differential Line Receiver				Multipurpose Counting Register				
"J-K" Flip-Flop	F95029	Fairchild		F95115	Fairchild		F100136	Fairchild				
Dual "D" Master-Slave Flip Flop	F95231	Fairchild		Gates, Exclusive OR/NOR				Decoders				
Gates, Exclusive OR/NOR				Triple 2-Input Exclusive OR/NOR Gate				Universal Decoder				
(Sequence OR, NOR, OR/NOR,)				F95107				F100170				30
Gates, OR/NOR				Dual 3-Input 3-Output OR Gate (Line Driver)				Drivers				
Dual 3-Input 3-Output OR Gate (Line Driver)				F95110				Quad Driver				
Dual 3-Input 3-Output NOR Gate (Line Driver)				F95111				F100131				Fairchild
Triple 4-3-3 Input NOR Gate				F95106				Hex Bus Driver				
Quad 2-Input NOR (With Enable)				F95004				F100151				Fairchild
Dual 4-5 Input OR/NOR Gate				F95109				Gates, AND-OR-Invert				
Dual 4-Input OR/NOR Gate (With Enable)				F95002				Triple AND-OR-Invert Gate				
Triple 2-3-2 Input OR/NOR Gate				F95105				F100117				Fairchild
Triple 2-Input OR/NOR Gate (With Enable)				F95003				5-Wide AND-OR-Invert Gate				
Quad 2-Input Gate (3 OR, 1 OR/NOR)				F95103				F100118				Fairchild
Quad 2-Input Gate (3 NOR, 1 OR/NOR)				F95102				Gates, Exclusive OR/NOR				
Quad 2-Input OR/NOR Gate (One Input Common)				F95101				Quintuple Exclusive OR/NOR Gate				
Latches				Latches				Gates, OR/NOR				
Dual "D" Clocked Latch				F95130				Triple 5-Input OR/NOR Gate				
Memories				Memories				F100101				Fairchild
For additional information, See Master Selection Guide—Memory sections				RAM, Scratch pad (4x4)				Quintuple 2-Input OR/NOR Gate				
RAM, Scratch pad (4x4)				F95401C				F100102				Fairchild
RAM (16x4)				F95400C				Latches				
RAM (256x1)				F95410C				Triple D Latch				
RAM (1024x1)				F95415C				F100130				Fairchild
Shift Registers				Shift Registers				Hex D Latch				
4-Bit Shift Register				F95000				F100150				Fairchild
								Memories				
								RAM (16x4 Register File)				
								F100145				Fairchild
								RAM (1024x1)				40
								F100415				Fairchild
								Multiplexers				
								16-Input Multiplexer				
								F100164				Fairchild
								Triple 4-Input Multiplexer				
								F100171				Fairchild
								Quad 2-Input Multiplexer with Latch				
								F100155				Fairchild
								Shift Registers				
								8-Bit Universal Shift Register				
								F100141				Fairchild
								8-Bit Shift Matrix				
								F100158				Fairchild
								Miscellaneous				
								Quintuple Line Receiver				
								F100114				Fairchild
								Dual 9-Bit Parity Generator/Checker				
								F100160				Fairchild
								Universal Priority Encoder				
								F100165				Fairchild

† Military Temperature Range (–55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

DIGITAL—ECL (cont)

Function	Device	Source	Line	Function	Device	Source	Line
ECL-III Series				Multivibrators			
Counters				Voltage Controlled Multivibrator			
Binary Counter	MC1654	Motorola			11C58	Fairchild	
Divide by 4 Counter (1 GHz)	11C05C	Fairchild			MC1658	Motorola	
	11C05M	Fairchild			SP1658	Plessey	
	MC1697	Motorola		Shift Registers			
	MC1699	Motorola		4-Bit Shift Register			
Divide by 4 Prescaler (1 GHz)	MC1697	Motorola			MC1694	Motorola	
Bi-Quinary Counter	MC1678	Motorola		Miscellaneous			
Decade Counter (1 GHz)	MC1696	Motorola		Dual Analog/Digital Comparator			
Flip-Flops					MC1650	Motorola	
Master-Slave "D" Flip-Flop	11C70	Fairchild	10		MC1651	Motorola	
	MC1670	Motorola			SP1650	Plessey	
	SP1670	Plessey			SP1651	Plessey	50
	SP1671	Plessey			Triple Line Receiver		
Master-Slave "D" Flip-Flop (UHF Prescaler)	11C06	Fairchild			MC1604	Motorola	
	MC1690	Motorola		Quad Line Receiver			
	SP1690	Plessey			MC1692	Motorola	
Dual Master-Slave "D" Flip-Flop	MC1605	Motorola			SP1692	Plessey	
Dual, Clocked "R-S" Flip-Flop	MC1666	Motorola		Voltage Controlled Oscillator			
	SP1666	Plessey			MC1648	Motorola	
	SP1667	Plessey			SP1648	Plessey	
Gates, Exclusive OR/NOR							
Triple 2-Input Exclusive OR GATE	MC1672	Motorola	20				
	SP1672	Plessey					
	SP1673	Plessey					
Triple 2-Input Exclusive NOR Gate	MC1674	Motorola					
	SP1674	Plessey					
	SP1675	Plessey					
Gates, OR/NOR							
Quad 2-Input OR Gate	MC1664	Motorola					
	SP1664	Plessey					
	SP1665	Plessey					
Quad 2-Input NOR Gate	MC1662	Motorola	30				
	SP1662	Plessey					
	SP1663	Plessey					
Dual 4-Input OR/NOR Gate	MC1660	Motorola					
	SP1660	Plessey					
	SP1661	Plessey					
Dual 4-5 Input OR/NOR Gate	11C01	Fairchild					
	MC1603	Motorola					
	MC1688	Motorola					
Triple 2-2-3-Input OR/NOR Gate	MC1602	Motorola					
Quad 2-Input OR/NOR Gate	MC1601	Motorola					
Latches							
Dual Clocked Latch	MC1668	Motorola	40				
	SP1668	Plessey					
	SP1669	Plessey					

† Military Temperature Range (-55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

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DIGITAL—Industrial/Consumer Circuits

Function	Source	Line	Function	Source	Line
Calculator			Timekeeping (cont)		
Calculating Circuits	S9414 S9651 see page 254		Clocks	AMI EA Fairchild GI Hitachi IMI Intersil ITT Litronix Mostek Motorola National Nortec OKI RCA Signetics Synertek SSS Sprague	50
	Exetron EA GI Hitachi Hughes Intel ITT Litronix MOS Mostek National NEC Nitron Nortec OKI Panasonic Rockwell Signetics Synertek TI Western	10	Clock Radio Circuits	Fairchild Mostek National	
			Watch, Digital	S1998A see page 260 AMI Harris Hitachi ITT Hughes Intel IMI Intersil Litronix Micro Pwr Mostek Motorola National Nortec Panasonic RCA Rockwell Ragen Siliconix SSS Sprague Synertek	60
Electronic Organ					70
Delay Circuits	Reticon				
Frequency Dividers	S2193 S2470 see page 254				80
	GI ITT Lithic Sys Motorola Mostek National NPC SGS	30			
Tone Generators	see page 255 S1424A S2555 S2556 S2566 S2567 S8890 S9660		Watch, Analog (Hands)	Hughes Hitachi Intersil ITT Micro Pwr Motorola Panasonic SSS Synertek	90
	GI ITT Lithic Sys Motorola Mostek National Nitron NPC	40			
Timekeeping					
Appliance Timers	AMI Motorola National				

† Military Temperature Range (–55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

DIGITAL—HNIL/HTL

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line
Arithmetic Functions				Decoders/Drivers (cont)				Gates, AND/NAND (cont)			
4-Bit Comparator	343A/C 343B/M	Teledyne S † Teledyne S		BCD to Decimal Decoder/Lamp Driver, Open Collector (continued)	380A/C 380B/M	Teledyne S † Teledyne S	50	Triple 3-Input NAND Gate	MC670 MC671 H103	Motorola Motorola SGS	100
Buffers/Inverters				BCD to Decimal Decoder/Driver (for Gas Discharge Display Tubes)				Quad 2-Input NAND Gate			
See also: Gates, Miscellaneous				MC676 Motorola H158 SGS 382A/C Teledyne S 382B/M † Teledyne S				ITT303-1 † ITT ITT303-5 ITT ITT321-1 † ITT ITT321-5 ITT ITT324-1 † ITT ITT324-5 ITT MC668 Motorola MC672 Motorola H102 SGS H122 SGS 303A/C Teledyne S 303B/M † Teledyne S 321A/C Teledyne S 321B/M † Teledyne S 324A/C Teledyne S 324B/M † Teledyne S			
Hex Inverter	MC680 MC690 H118 332A/C 332B/M	Motorola Motorola SGS Teledyne S † Teledyne S		Dual Power AND Driver, Open Collector and Open Emitter	MC699	Motorola		Quad 2-Input NAND Gate, Open Collector			
Hex Inverter, Open Collector	MC681 MC689 H112	Motorola Motorola SGS	10	Dual 4-Input AND Driver, Expandable	H109	SGS		ITT302-1 † ITT ITT302-5 ITT ITT323-1 † ITT ITT323-5 ITT 302A/C Teledyne S 302B/M † Teledyne S			
Hex Inverter, Strobed	ITT335-1 ITT335-5 MC677 H119 335A/C 335B/M	† ITT ITT Motorola SGS Teledyne S † Teledyne S		Dual 4-Input NAND Line Driver, Expandable	MC662	Motorola		Quad 2,2,3,3-Input NAND Gate			
Hex Inverter, Strobed, Open Collector	ITT334-1 ITT334-5 MC678 H115 334A/C 334B/M	† ITT ITT Motorola SGS Teledyne S † Teledyne S	20	Dual 5-Input Power NAND Driver	301A/C 301B/M	Teledyne S † Teledyne S	60	ITT325-1 † ITT ITT325-5 ITT ITT326-1 † ITT ITT326-5 ITT 325A/C Teledyne S 325B/M † Teledyne S 326A/C Teledyne S 326B/M Teledyne S			
Counters				Flip-Flops				Gates, OR/NOR			
Binary Counter	ITT372-1 ITT372-5 MC685 H156 372A/C 372B/M	† ITT ITT Motorola SGS Teledyne S † Teledyne S		Quad D Flip-Flop	ITT370-1 ITT370-5 370A/C 370B/M	† ITT ITT Teledyne S † Teledyne S		Dual 2-Input OR Interface Buffer			
Binary Up/Down Counter	374A/C 374B/M	Teledyne S † Teledyne S	30	Master-Slave R-S Flip-Flop	MC664	Motorola		393	Teledyne S		
Decade Counter	ITT371-1 ITT371-5 MC684 H157 371A/C 371B/M	† ITT ITT Motorola SGS Teledyne S † Teledyne S		Master/Slave J-K or Set-Reset Flip-Flop	ITT311-1 ITT311-5 311A/C 311B/M	† ITT ITT Teledyne S † Teledyne S	70	Dual 2-Input NOR Interface Buffer			
Decade Up/Down Counter	373A/C 373B/M	Teledyne S † Teledyne S		Dual "J-K" Flip-Flop with Preset	H110	SGS		394	Teledyne S		
Decoders/Drivers				Gates, AND/NAND				Gates, AND-OR-Invert			
BCD to Seven Segment Decoder/Driver	383A/C 383B/M	Teledyne S † Teledyne S	40	Dual "J-K" Flip-Flop with Preset and Clear	H111	SGS		Quad 2-Input NOR Gate			
BCD to Decimal Decoder, Open Collector	ITT381-1 ITT381-5 381A/C 381B/M	† ITT ITT Teledyne S † Teledyne S		Dual "J-K" Flip-Flop with Reset	MC663	Motorola		306A/C Teledyne S 306B/M † Teledyne S			
BCD to Seven Segment Driver, Gas Discharge Driver	384A/C 384B/M	Teledyne S † Teledyne S		Dual "J-K" or Set-Reset Flip-Flop	ITT312-1 ITT312-5 MC688 312A/C 312B/M 313A/C 313B/M	† ITT ITT Motorola Teledyne S † Teledyne S Teledyne S † Teledyne S	80	Quad 2-Input NOR Gate, Open Collector			
BCD to Decimal Decoder/Lamp Driver, Open Collector	ITT380-1 ITT380-5 (continued)	† ITT ITT		Dual 2-Input AND Interface Buffer	391	Teledyne S		307A/C Teledyne S 307B/M † Teledyne S			
				Gates, AND/NAND				Gates, Exclusive OR			
				Dual 2-Input AND Interface Buffer				Expandable AND-OR-Invert			
				391				344A/C Teledyne S 344B/M † Teledyne S			
				Dual 4-Input AND Interface Buffer				Dual 2-Wide, 2-Input AND-OR-Invert Gate			
				390				MC673 Motorola MC674 Motorola 341A/C Teledyne S 341B/M † Teledyne S			
				Dual 4-Input NAND Gate				Dual 2-Wide, 2-Input AND-OR-Invert Gate, Expandable			
				MC660 Motorola MC661 Motorola				H105 SGS			
				Dual 2-Input NAND Interface Buffer				Gates, Exclusive OR			
				392				Quad 2-Input Exclusive OR Gate			
				Dual 4-Input NAND Interface Buffer				MC683 Motorola			
				395							
				Dual 4-Input NAND Gate, Expandable							
				H104 SGS H124 SGS							
				Dual 5-Input NAND Gate							
				ITT301-1 † ITT ITT301-5 ITT ITT 322-1 † ITT ITT 322-5 ITT 301A/C Teledyne S 301B/M † Teledyne S 322A/C Teledyne S 322B/M † Teledyne S							

† Military Temperature Range (–55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

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DIGITAL—HNIL/HTL (cont)

Function	Device	Source	Line	Function	Device	Source	Line
Gates, Miscellaneous				Translators (cont)			
Hex Inverter/Gate (Quad Inverter, Dual NAND Gate)	ITT333-1 ITT333-5 333A/C 333B/M	† ITT ITT Teledyne S † Teledyne S		Hex Inverter/Interface (Low to High: TTL, CMOS to HTL, CMOS)	MC691	Motorola	
Hex Inverter/Gate (Quad Inverter, Dual NAND Gate) Open Collector	ITT332-1 ITT332-5 332A/C 332B/M	† ITT ITT Teledyne S † Teledyne S		Miscellaneous			
Dual 4-Input Gate Expander (for 600 Series)	MC669	Motorola		Dual Pulse Stretcher	MC675 349A/C 349B/M	Motorola Teledyne S † Teledyne S	
Dual 5-Input Gate Expander (for 300 Series)	331A/C 331B/M CA3094 CA3094A CA3094B	Teledyne S † Teledyne S † RCA † RCA † RCA	10	Quad Schmitt Trigger/Line Receiver	367A/C 367B/M	Teledyne S † Teledyne S	
Latches				Quad Schmitt Trigger/Line Receiver, Open Collector	368A/C 368B/M	Teledyne S † Teledyne S	
Quad Latch	MC682	Motorola		Multiplexers			
Multiplexers				8-Bit Multiplexer	350A/C 350B/M	Teledyne S † Teledyne S	
Dual 4-Input Gate Expander (for 600 Series)	MC669	Motorola		Dual 4-Input Gate Expander (for 300 Series)	351A/C 351B/M	Teledyne S † Teledyne S	
Multivibrators				Multivibrators			
Monostable Multivibrator	H117	SGS	20	Monostable Multivibrator	H117	SGS	20
Dual Monostable Multivibrator	ITT342-1 ITT342-5 MC667 342A/C 342B/M	ITT ITT Motorola Teledyne S † Teledyne S		Dual Retriggerable Monostable Multivibrator	347A/C 347B/M	Teledyne S † Teledyne S	
Shift Registers				Shift Registers			
4-Bit Parallel In Parallel Out Shift Register	MC686 375A/C 375B/M	Motorola Teledyne S † Teledyne S	30	Translators			
Translators				Dual Low to High Interface (TTL to HNIL)	362A/C 362B/M	Teledyne S † Teledyne S	
Dual Low to High Interface (TTL to HNIL)	362A/C 362B/M	Teledyne S † Teledyne S		Triple Low to High Translator (TTL to HTL)	MC666	Motorola	
Triple Low to High Translator (TTL to HTL)	MC666	Motorola		Quad Low to High Interface (TTL to HNIL)	H114 363A/C 363B/M	SGS Teledyne S † Teledyne S	
Quad Low to High Interface (TTL to HNIL)	H114 363A/C 363B/M	SGS Teledyne S † Teledyne S		Dual High to Low Interface (HNIL to DTL, TTL)	361A/C 361B/M	Teledyne S † Teledyne S	
Dual High to Low Interface (HNIL to DTL, TTL)	361A/C 361B/M	Teledyne S † Teledyne S		Dual Interface Element, (Line Driver, Receiver, ECL to TTL, MOS to TTL)	MC696	Motorola	
Dual Interface Element, (Line Driver, Receiver, ECL to TTL, MOS to TTL)	MC696	Motorola		Triple High to Low Translator (HTL to TTL)	MC665	Motorola	40
Triple High to Low Translator (HTL to TTL)	MC665	Motorola	40	Quad High to Low Converter (Open Collector)	H113	SGS	
Quad High to Low Converter (Open Collector)	H113	SGS					

† Military Temperature Range (−55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

DIGITAL—TTL

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line					
Arithmetic Functions				Arithmetic Functions (cont)				Arithmetic Functions (cont)								
Gated Full Adder	5480	† Fairchild	10	Dual Full Adder (continued)	MC9304	† Motorola	60	High Speed Arithmetic Logic Unit/Function Generator (continued)	N74181	Signetics	120					
	7480	Fairchild			RC9304	Raytheon			S54181	† Signetics						
	ITT5480	† ITT			RM9304	† Raytheon			SW7481	SW						
	ITT7480	ITT		9344C	Fairchild	SN54181	† TI									
	MC5480	† Motorola		9344M	† Fairchild	SN74181	TI									
	MC7480	Motorola		Binary (4x2) Multiplier				Two's Complement Multiplier (4x2)								
	N7480	Signetics		AM2505C	AMD	AM2505M	† AMD	9342C	AMD	9342M	† AMD	130				
	N8268	Signetics		AM2505M	† AMD	RC2505	Raytheon	SN54182	† AMD	SN74182	AMD					
	S5480	† Signetics		RC2505	Raytheon	RM2505	† Raytheon	9342C	Fairchild	9342M	† Fairchild					
	S8268	† Signetics		RM2505	† Raytheon	4-Bit-by-4-Bit Parallel Binary Multiplier (used with 54/74285)				54182	† Fairchild					
	SW7480	SW		54284	† MMI	74284	MMI	74182	Fairchild	HD2562	Hitachi					
	SN5480	† TI		DM54284	† National	SN74284	TI	HD2562	Hitachi	ITT54182	† ITT					
	SN7480	TI		4-Bit-by-4-Bit Parallel Binary Multiplier (used with 54/74284)				4-Bit Multiplier, Three-State (two ICs to a set 7875A and 7875B)					ITT74182	ITT		
	2-Bit Binary Full Adder				4-Bit ALU with Lookahead Carry				4-Bit Magnitude Comparator							
	5482	† Fairchild		20	9340C	AMD	80	DM7200	† National	DM8200	National		N8269	Signetics		
7482	Fairchild	9340M	† AMD		DM8200	National										
ZN5482	† Ferranti	9340C	Fairchild		N8269	Signetics										
ZN7482	Ferranti	9340M	† Fairchild		S8269	† Signetics										
HD2513	Hitachi	Arithmetic Logic Element				4-Bit Magnitude Comparator, Separate A=B Output, Expandable										
ITT5482	† ITT	MC7260	Motorola		150	9324C		AMD	160	9324M	† AMD		150			
ITT7482	ITT	MC8260	† Motorola			5485		† Fairchild								
SW7482	SW	RC8260	Raytheon			7485		Fairchild								
SN5482	† TI	RM8260	† Raytheon			9324C		Fairchild								
SN7482	TI	N8260	Signetics			9324M		† Fairchild								
4-Bit Binary Full Adder,						Fast Carry Extender (for 8260)				4-Bit Magnitude Comparator, Separate A=B Output, Expandable						
5483	† Fairchild	30	MC7261			Motorola		90		9324C	AMD	150		9324M	† AMD	160
7483	Fairchild		MC8261			† Motorola				5485	† Fairchild					
54283	† Fairchild		RC8261			Raytheon				7485	Fairchild					
ZN5483A	† Ferranti		RM8261			† Raytheon				9324C	Fairchild					
ZN7483A	Ferranti		N8261	Signetics		9324M	† Fairchild									
HD2535	Hitachi		S8261	† Signetics		ZN5485	† Ferranti									
ITT5483	† ITT		High Speed Arithmetic Logic Unit/Function Generator				Dual 4-Bit Magnitude Comparator									
ITT7483	ITT		9341C	AMD		100	MC4022			Motorola	Dual 4-Bit Magnitude Comparator Open Collector			MC4021	Motorola	
MC5483	† Motorola		9341M	† AMD			6-Bit Identity Comparator									
MC7483	Motorola		AM2506C	AMD	DM7160		† National		DM8160	National	170					
DM5483	† National		AM2506M	† AMD	10-Bit Identity Comparator											
DM7483	National		SN54181	† AMD	DM7130		† National		DM8130	National						
5483	† Raytheon		SN74181	AMD												
7483	Raytheon		7341C	Fairchild												
54283	† Raytheon		9341C	Fairchild												
74283	Raytheon	9341M	† Fairchild													
N7483	Signetics	54181	† Fairchild													
S5483	† Signetics	74181	† Fairchild													
SW7483	SW	ZN54181	† Ferranti													
SN5483A	† TI	ZN74181	Ferranti													
SN7483A	TI	HD2547	Hitachi													
SN54283	† TI	MC54181	Motorola													
SN74283	TI	MC74181	Motorola													
4-Bit Full Adder with Output Latch				Dual Full Adder												
AM2506C	AMD	9304C	AMD													
AM2506M	AMD	9304M	† AMD													
NBCD Adder (Natural Binary Coded Decimal)				Dual Full Adder												
MC54456	† Motorola	9304C	Fairchild													
MC74456	Motorola	9304M	† Fairchild													
Dual Full Adder				Dual Full Adder												
9304C	AMD	ITT9304-1	† ITT													
9304M	† AMD	ITT9304-5	ITT													
9304C	Fairchild	MC8304	Motorola													
9304M	† Fairchild	(continued)														
ITT9304-1	† ITT															
ITT9304-5	ITT															
MC8304	Motorola															
(continued)																

† Military Temperature Range (-55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

DIGITAL—TTL (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line
Arithmetic Functions (cont)				Buffers/Inverters (cont)				Counters, Binary, Count-Up (cont)			
6-Bit, Unified Bus Comparator, Active Pull Up				Hex Inverter (continued)				Binary Counter, Ripple (continued)			
	DM7131	† National		MC5404	† Motorola				HD2520	Hitachi	
	DM8131	National		MC7404	Motorola				HD7493	Hitachi	
6-Bit Unified Bus Comparator, Open Collector					DM5404	† National	60		ITT5493	† ITT	
	DM7136	† National		DM7404	National				ITT7493	ITT	
	DM8136	National		5404	† Raytheon				MC5493	† Motorola	120
Buffers/Inverters					7404	Raytheon			MC7493	Motorola	
Quad Gated Buffer, Three-State					N7404	Signetics			DM5493	† National	
	54125	† Fairchild		S5404	† Signetics			DM7493	National		
	74125	Fairchild		SW7404	SW			N7493	Signetics		
	HD74125	Hitachi		SN5404	† TI			S5493	† Signetics		
	DM7093	† National		TD3404	Toshiba			SN7493	SW		
	DM8093	National		SN7404	TI		70	SN5493A	† TI		
	DM54125	† National	10	7404	TRW			SN7493A	TI		
	DM74125	National						SN54293	† TI		
	N74125	Signetics						SN74293	TI		
	S54125	† Signetics		Hex Inverter, Three-State					TD3493	Toshiba	130
	SN54125	† TI		DM7096	† National			7493	TRW		
	SN54425	† TI		DM7098	† National			74293	TRW		
	SN74125	TI		DM8096	National						
	SN74425	TI		DM8098	National			Dual 4-Bit Binary Counter, Ripple (Dual 54/7493A)			
Quad Gated Buffer, Three-State (Inverted Control)					DM54366	† National			SN54393	† TI	
	54126	† Fairchild		DM75366	National			SN74393	TI		
	74126	Fairchild		DM54368	† National			Binary (Divide-By-2 and Divide-By-8) Counter/Latch, Ripple, Preset Input			
	HD74126	Hitachi		DM74368	National				54177	† Fairchild	
	DM7094	† National	20	N8T96	Signetics				54197	Fairchild	
	DM8094	National		SN54366	† TI		80		74177	Fairchild	
	DM54126	† National		SN54368	† TI				74197	Fairchild	
	DM74126	National		SN74366	TI				ZN54197	† Ferranti	
	N74126	Signetics		SN74368	TI				ZN74197	Ferranti	140
	S54126	† Signetics		Hex Inverter, Open Collector					HD2573	Hitachi	
	SN54126	† TI		5405	† Fairchild			MC7281	Motorola		
	SN74126	TI		7405	Fairchild			MC8281	Motorola		
	SN54426	† TI		9017C	Fairchild			MC54177	† Motorola		
	SN74426	TI	30	9017M	† Fairchild			MC74177	Motorola		
Hex Buffer, Three-State					ZN5405	Ferranti		DM7281	† National		
	DM7095	† National		ZN7405	Ferranti			DM7291	† National		
	DM7097	† National		HD2523	Hitachi			DM8281	National		
	DM8095	National		HD7405	Hitachi			DM8291	National		
	DM8097	National		ITT5405	† ITT			DM54197	† National	150	
	DM54365	† National		ITT7405	ITT			DM74197	National		
	DM74365	National		MC5405	† Motorola			DM54177	† National		
	DM54367	† National		MC7405	Motorola			DM74177	National		
	DM74367	National		DM5405	† National			RC8281	Raytheon		
	DM74367	National		DM7405	National			RC8291	Raytheon		
	N8T95	Signetics		5405	† Raytheon			RM8281	† Raytheon		
	N8T97	Signetics		7405	Raytheon			RM8291	† Raytheon		
	SN54365	† TI		7405	Raytheon			N8281	Signetics		
	SN54367	† TI		N7405	Signetics		100	N8291	Signetics		
	SN74365	TI		S5405	† Signetics			N74177	Signetics	160	
	SN74367	TI		SW7405	SW			S54177	† Signetics		
Hex Inverter					SN5405	† TI		S8281	† Signetics		
	5404	† Fairchild		SN7405	TI			S8291	† Signetics		
	7404	Fairchild		TD3405	Toshiba			SN54177	† TI		
	9016C	Fairchild		7405	TRW			SN54197	† TI		
	9016M	† Fairchild		Counters, Binary, Count-Up					SN74177	TI	
	ZN5404	† Ferranti		Binary Counter, Ripple					SN74197	TI	
	ZN7404	Ferranti						Dual Binary Counter, Synchronous			
	HD2522	Hitachi		5493	† Fairchild				MC54453	† Motorola	
	HD7404	Hitachi		7493	Fairchild				MC74453	Motorola	
	ITT5404	† ITT		9305C	Fairchild			Binary Counter, Synchronous, Preset Input (Synchronous Clear)			
	ITT7404	ITT		9305M	† Fairchild		110		SN54163	† AMD	170
	ITT9012	† ITT		9356C	Fairchild				SN74163	AMD	
	ITT9016-1	† ITT		74293	Fairchild				54163	† Fairchild	
	ITT9016-5	ITT		ZN5493	† Ferranti				74163	Fairchild	
	(continued)			ZN7493	Ferranti				(continued)		
				(continued)							

† Military Temperature Range (−55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

DIGITAL—TTL (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line		
Counters, Binary, Count-Up (cont)				Counters, Binary, Count-Up/Down (cont)				Counters, Decade, Count Up (cont)					
Binary Counter, Synchronous, Preset Input (Synchronous Clear) (continued)				Binary Up/Down Counter, Synchronous Preset Input with Mode Control				Decade Counter, Ripple (continued)					
	ZN54163	† Ferranti	10		SN54191	† AMD	60		MC5490	† Motorola	120		
	ZN74163	Ferranti			SN74191	AMD				MC7490		Motorola	
	HD74163	Hitachi			54191	† Fairchild				DM5490		† National	
	ITT54163	† ITT			74191	Fairchild				DM7490		National	
	ITT74163	ITT			ZN54191	† Ferranti				N7490		Signetics	
	DM54163	† National			ZN74191	Ferranti				S5490		† Signetics	
	DM74163	National			HD74191	Hitachi				SW7490		SW	
	54163	† Raytheon			ITT54191	† ITT				SN54290		† TI	
	74163	Raytheon			ITT74191	ITT				SN5490A		† TI	
	N74163	Signetics			DM54191	† National				SN74290		TI	
	S54163	Signetics		DM74191	National			SN7490A	TI				
	SN54163	† TI		54191	† Raytheon			TD3490	Toshiba				
	SN74163	TI		74191	Raytheon			7490	TRW				
	74163	TRW		SN54191	† TI			74290	TRW				
Binary Counter, Synchronous, Preset Input (Asynchronous Clear)				Binary Up/Down Counter, Synchronous, Preset Input (2 Clocks)				Dual Decade Counter, Ripple (Dual 54/7490A)					
	SN54161	† AMD	20		9366C	AMD	70		SN54390	† TI	130		
	SN74161	AMD			9366M	† AMD				SN54490		† TI	
	9316C	AMD			SN54193	† AMD				SN74390		TI	
	9316M	† AMD			SN74193	AMD				SN74490		TI	
	9316C	Fairchild			9366C	Fairchild				Decade (Divide-By-2 and Divide-By-5) Counter/Latch, Ripple, Preset Input			
	9316M	† Fairchild			9366M	† Fairchild				54176		† Fairchild	140
	54161	† Fairchild			54193	† Fairchild				74176		Fairchild	
	74161	Fairchild			74193	Fairchild				54196		† Fairchild	
	ZN54161	† Ferranti			54193	† Fairchild				74196		Fairchild	
	ZN74161	Ferranti			74193	Fairchild				MC7280		† Motorola	
	HD74161	Hitachi		ZN54193	† Ferranti			MC54176	† Motorola				
	ITT9316	ITT		ZN74193	Ferranti			MC74176	Motorola				
	ITT54161	† ITT		HD2542	Hitachi			DM7280	† National				
	ITT74161	ITT		ITT54193	† ITT			DM7290	† National				
	MC8316	Motorola		ITT74193	ITT			DM8280	National				
	MC9316	† Motorola		MC54193	† Motorola			DM8290	National				
	DM54161	† National		MC74193	Motorola			DM54176	† National				
	DM74161	National		DM7563	† National			DM54196	† National				
	RC9316	Raytheon		DM8563	National			DM74176	National				
	RM9316	† Raytheon		DM54193	† National			DM74196	National				
	54161	† Raytheon		DM74193	National			RC8280	Raytheon				
	74161	Raytheon		RC9366	Raytheon			RC8290	Raytheon				
	N74161	Signetics		MR9366	† Raytheon			RM8280	† Raytheon				
	S54161	† Signetics		54193	† Raytheon			RM8290	† Raytheon				
	SN29316	TI		74193	Raytheon			N8280	Signetics				
	SN39316	† TI		N74193	Signetics			N8290	Signetics				
	SN54161	† TI		S54193	† Signetics			N74176	Signetics				
	SN74161	TI		SW74193	SW			S8280	† Signetics				
	74161	TRW		SN54193	† TI			S8290	† Signetics				
				SN74193	TI			S54176	† Signetics				
				TD34193	Toshiba			SN54176	† TI				
								SN54196	† TI				
								SN74176	TI				
								SN74196	TI				
Binary Counter, Synchronous, Preset, Input Low-Power				Dual Binary Up/Down Counter, Synchronous, Preset Input				Dual Decade Counter, Synchronous					
	N8293	Signetics	40		MC54455	† Motorola	100		MC54452	† Motorola	160		
	S8293	† Signetics			MC74455	Motorola			MC74452	Motorola			
Binary Counter, Synchronous (both conventional and three state outputs) Preset Input				Counters, Decade, Count Up				Decade Counter, Synchronous, Preset Input (Asynchronous Clear)					
	DM7556	† National	50	Decade Counter, Ripple					9310C	AMD	170		
	DM8556	National			9350C	Fairchild		9310M	† AMD				
Counters, Binary, Count-Up/Down					9350M	† Fairchild		SN54160	† AMD				
Binary Up/Down Counter, Synchronous with mode control					5490	† Fairchild		SN74160	AMD				
	N8284	AMD		7490	Fairchild		9310C	Fairchild					
	S8284	† AMD		74290	Fairchild		9310M	† Fairchild					
	AM2501C	AMD		ZN5490	† Ferranti		54160	† Fairchild					
	AM2501M	† AMD		ZN7490	Ferranti		74160	Fairchild					
	RC8284	Raytheon		HD2519	Hitachi		HD74160	Fairchild					
	RM8284	† Raytheon		HD7490	Hitachi		HD74160	Hitachi					
	N8284	Signetics		ITT5490	† ITT		ITT54160	† ITT					
	S8284	† Signetics		ITT7490	ITT		(continued)	(continued)					

† Military Temperature Range (−55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

DIGITAL—TTL (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line	
Counters, Decade, Count Up (cont)				Counters, Decade, Count Up/Down (cont)				Counters, Miscellaneous (cont)				
Decade Counter, Synchronous, Preset Input (Asynchronous Clear) (continued)				Decade Up/Down Counter, Synchronous, Preset with Mode Control (continued)				Programmable Modulo-N Binary Counter				
	ITT74160	ITT	10				60		MC4018	Motorola	120	
	MC8310	Motorola			74190	Raytheon				MC4019		Motorola
	MC9310	Motorola			SN54190	† TI				MC4318		† Motorola
	DM54160	† National			SN74190	TI				MC4319		† Motorola
	DM74160	National								Programmable Modulo-N Decade Counter		
	54160	† Raytheon								MC4016		Motorola
	74160	Raytheon								MC4017		Motorola
	RC9310	Raytheon								MC4316		† Motorola
	RM9310	† Raytheon								MC4317		† Motorola
	N74160	Signetics			Decade Up/Down Counter, Synchronous, Preset Input (2 clocks)							
	S54160	† Signetics	20				70				130	
	SN29310	TI			9360C	AMD				Binary Counter/Latch, Three-State		
	SN39310	TI			9360M	† AMD				DM7554		† National
	SN54160	† TI			SN54192	† AMD				DM8554		National
	SN74160	TI			SN74192	AMD				Decade Counter/Latch, Three-State		
	74160	TRW			54192	† Fairchild				DM7552		† National
Decade Counter, Synchronous, Preset Input (Asynchronous Clear)					74192	Fairchild			DM8552	National		
	SN54162	† AMD			ZN54192	† Ferranti				Programmable Modulo-N Divider (Divide by 2 to 15, Cascadable)		
	SN74162	AMD			ZN74192	Ferranti				DM7520		† National
	54162	† Fairchild			HD2541	Hitachi				DM8520		National
	74162	Fairchild		ITT74192	ITT			4-Bit Variable Modulo Counter (2 and 4, 5, 6, 7, 8, or 10, 12, 14, 16)				
	HD74162	Hitachi		MC54192	† Motorola			9305C	Fairchild			
	ITT54162	† ITT		MC74192	Motorola			9305M	† Fairchild			
	ITT74162	ITT		DM7560	† National			Decade Counter/Latch/7 Segment Decoder				
	DM54162	† National		DM8560	National			MC4050	Motorola			
	DM74162	National		DM54192	† National			MC4051	Motorola			
	54162	† Raytheon		DM74192	National			MC4350	† Motorola			
	74162	Raytheon		54192	† Raytheon			Decade Counter/Latch/Decoder (Nixie Driver)				
	N74162	Signetics		74192	Raytheon			SN74142	TI			
	S54162	† Signetics		RC9360	Raytheon			Decade Counter/Latch LED/Lamp Driver (High Current Output)				
	SN54162	† TI		RM9360	† Raytheon			SN54144	† TI			
	SN74162	TI		N74192	† Signetics			SN74144	TI			
	74162	TRW		S74192	Signetics			Decade Counter/Latch, LED/Lamp Driver (Constant Current Output)				
Decade Counter, Synchronous, Preset Input Low-Power					SN54192	† TI		SN54143	† TI			
	N8292	Signetics		SN74192	TI		SN74143	TI				
	S8292	† Signetics		TD34192	Toshiba							
Decade Counter, Synchronous (both conventional and three state outputs), Preset Inputs					Dual Decade Up/Down Counter, Synchronous, Preset Input							
	DM7555	† National			MC54454	Motorola						
	DM8555	National			MC74454	Motorola						
Counters, Decade, Count Up/Down					Four Decade Counter/Latch/Display Driver (Synchronous up/down count, BCD and segment drives)							
					ZN1040	Ferranti						
Decade Up/Down Counter, Synchronous					Counters, Miscellaneous							
	N8285	AMD		4-Bit Universal Counter								
	S8285	† AMD			MC4023	Motorola						
	RC8285	Raytheon		Divide-By-12 Counter (Divide-By-Two and Divide-By-6), Ripple								
	RM8285	† Raytheon										
	N8285	Signetics			5492	† Fairchild						
	S8285	† Signetics			7492	Fairchild						
Decade Up/Down Counter, Synchronous, Preset with Mode Control						ZN5492	† Ferranti					
	SN54190	† AMD			ZN7492	Ferranti						
	SN74190	AMD			HD2521	Hitachi						
	9306C	AMD			HD7492	Hitachi						
	9306M	† AMD			ITT5492	† ITT						
	9360C	Fairchild			ITT7492	ITT						
	9360M	† Fairchild			MC5492	† Motorola						
	54190	† Fairchild			MC7492	Motorola						
	74190	Fairchild			DM5492	† National						
	HD74190	Hitachi			DM7492	National						
	ITT54190	† ITT			N7492	Signetics						
	ITT74190	ITT			S5492	† Signetics						
	DM54190	† National			SW7492	SW						
	DM74190	National			SN5492A	† TI						
	54190	† Raytheon			SN7492A	TI						
	(continued)				TD3492	Toshiba						
					7492	TRW						
					Divide-By-12 (Divide by 2 and 6) Counter, Preset Input							
					DM7288	† National						
					DM8288	National						
					N8288	Signetics						
					S8288	† Signetics						
					Excess 3-To-Decimal (1 of 10) Decoder							
					5443	† Fairchild						
					7443	Fairchild						
					HD2537	Hitachi						
					HD7443	Hitachi						
					ITT5443	† ITT						
					ITT7443	ITT						
					MC5443	† Motorola						
					MC7443	Motorola						
					5443	† Raytheon						
					7443	Raytheon						
					N7443	Signetics						
					S5443	† Signetics						
					SW7443	SW						
					SN5443A	† TI						
					SN7443A	TI						
					Excess 3 Gray-To-Decimal (1 of 10) Decoder							
					5444	† Fairchild						
					7444	Fairchild						
					HD2538	Hitachi						
					HD7444	Hitachi						
					ITT5444	† ITT						
					ITT7444	ITT						
					MC5444	† Motorola						
					MC7444	Motorola						
					5444	† Raytheon						
					7444	Raytheon						
					S5444	† Signetics						
					N7444	Signetics						
					SW7444	SW						
					SN5444A	† TI						
					SN7444A	TI						

† Military Temperature Range (-55°C to 125°C)

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DIGITAL—TTL (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line	
Decoders (cont)				Decoders (cont)				Decoders (cont)				
BCD-To-Decimal (1 of 10) Decoder	9301M	†AMD	10	BCD-To-Decimal Decoder/Driver, Open Collector, 15v (continued)	S54145	† Signetics	70	Dual 2-Line to 4-Line Decoder/Demultiplexer, Open Collector (or 3-Line to 8-Line Decoder/Demultiplexer) (continued)	54156	† Raytheon	120	
	9301C	AMD				SW74145		SW		74156		Raytheon
	5442	† Fairchild				SN54145		† TI		N74156		Signetics
	7442	Fairchild			BCD-To-Decimal/Decoder Driver, Open Collector to 30v Output	74145	TRW		S54156	† Signetics		
	9301C	Fairchild				5445	† Fairchild		SW74156	SW		
	9301M	† Fairchild				7445	Fairchild		SN54156	† TI		
	9302C	Fairchild				HD2531	Hitachi		SN74156	TI		
	9302M	† Fairchild				ITT5445	† ITT		74156	TRW		
	ZN5442	† Ferranti				ITT7445	ITT					
	ZN7442	Ferranti				MC5445	† Motorola		Dual 2-Line to 4-Line Decoder/Demultiplexer (or 3-Line to 8-Line Decoder/Demultiplexer) Three-State	54255	† Raytheon	130
	HD2536	Hitachi				MC7445	Motorola			74255	Raytheon	
	HD7442	Hitachi				DM5445	† National		Binary To Octal (1 of 8) Decoder			
	ITT5441	† ITT				DM7445	National		9301	Fairchild		
	ITT7441	ITT				5445	† Raytheon		9301M	† Fairchild		
	ITT5442	† ITT				7445	Raytheon		MC4006	Motorola		
	ITT7442	ITT				N7445	Signetics		MC4306	† Motorola		
	ITT9301-1	† ITT				S5445	† Signetics		MC7250	Motorola		
	ITT9301-5	ITT				SW7445	SW		MC8250	† Motorola		
	MC5442	† Motorola		20		SN5445	† TI	80	RC8250	Raytheon		
	MC7442	Motorola				SN7445	TI		RM8250	† Raytheon		
	MC8301	Motorola			7445	TRW		N8250	Signetics			
	MC9301	† Motorola						S8250	† Signetics			
	DM5442	† National		Dual 1-of-4 Decoder/Demultiplexer (Independent Address)	9321C	AMD		Binary to Octal Decoder, Non-Inverting	MC4048	Motorola		
	DM7442	National			9321M	† AMD		Binary to Octal Decoder, Inverting/Non-Inverting, Open Collector	MC4038	Motorola		
	DM8301	National			9321C	Fairchild		1-Line to 8-Line Demultiplexer	DM7223	† National		
	DM9301	† National			9321M	† Fairchild			DM8223	National		
	5442	† Raytheon		Dual Binary to One-Of-Four Line Gated Decoder	MC4007	Motorola		Binary to 2-of-8 Decoder, Open Collector	MC4040	Motorola		
	7442	Raytheon			MC4307	† Motorola		4-Line to 16-Line Decoder/Demultiplexer				
	RC8251	Raytheon						9311C	AMD			
	RC8252	Raytheon	30					9311M	† AMD			
	RM8251	† Raytheon						SN54154	† AMD			
	RM8252	† Raytheon		Demultiplexer, (2-Lines In - 2 of 4 Out) Three-State	DM7230	† National	90	SN74154	AMD			
	N7442	Signetics			DM8230	National		9311C	Fairchild			
	N8251	Signetics						9311M	† Fairchild			
	N8252	Signetics						54154	† Fairchild			
	S5442	† Signetics						74154	Fairchild			
	S8251	† Signetics		Dual 2-Line To 4-Line Decoder/Demultiplexer, Totem Pole Output (or 3-Line to 8-Line Decoder/Demultiplexer)	54155	† Fairchild		ZN54154	† Ferranti			
	S8252	† Signetics			74155	Fairchild		ZN74154	Ferranti			
	SW7442	SW			ZN54155	† Ferranti		HD2580	Hitachi			
	SN29301	TI	40		ZN74155	Ferranti		ITT9311-1	† ITT			
	SN39301	† TI			HD75155	Hitachi		ITT9311-5	ITT			
	SN5442A	† TI			ITT54155	† ITT		ITT54154	† ITT			
	SN7442A	TI			ITT74155	ITT		ITT74154	ITT			
	TD3441	Toshiba			MC54155	† Motorola		MC8311	Motorola			
	TD3442	Toshiba			MC74155	Motorola		MC9311	† Motorola			
BCD-to-Binary and Binary-to-BCD Converter, Open Collector								DM54154	† National			
	MC4001	Motorola			DM74155	National		DM74154	National			
BCD-To-Decimal Decoder/Driver, Open Collector, 15v								RC9311	Raytheon			
	54145	† Fairchild	50		54155	† Raytheon		RM9311	† Raytheon			
	74145	Fairchild				74155	Raytheon		54154	† Raytheon		
	93145C	Fairchild				N74155	Signetics		74154	Raytheon		
	93145M	† Fairchild				S54155	† Signetics		N74154	Signetics		
	HD2555	† Hitachi				SW74155	SW		S54154	† Signetics		
	ITT54145	† ITT				SN54155	† TI		SW74154	SW		
	ITT74145	ITT				SN74155	TI		SN29311	TI		
	MC54145	† Motorola				74155	TRW		SN39311	† TI		
	MC74145	Motorola			Dual 2-Line to 4-Line Decoder/Demultiplexer, Open Collector (or 3-Line to 8-Line Decoder/Demultiplexer)	54156	† Fairchild	110	SN54154	† TI		
	DM54145	† National				74156	Fairchild		SN74154	TI		
	DM74145	National				HD74156	Hitachi		74154	TRW		
	54145	† Raytheon				ITT54156	† ITT					
	74145	Raytheon			ITT74156	ITT						
	N74145	Signetics	60		MC54156	† Motorola						
	(continued)				MC74156	Motorola						
					DM54156	† National						
					DM74156	National						
					(continued)							

† Military Temperature Range (— 55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

DIGITAL—TTL (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line		
Decoders (cont)				Drivers (cont)				Drivers (cont)					
4-Line To 16-Line Decoder/Demultiplexer, Open Collector Output				Hex Inverter Buffer/Driver Open Collector High Voltage Output, to 15v (continued)				4-Input NAND High Voltage, High Current Driver (40 to 50v, sinks 150 to 500 ma) (continued)					
	54159	† Raytheon			N7416	Signetics			SH2002M	† Fairchild			
	74159	Raytheon			S5416	† Signetics			SH2200C	Fairchild			
	SN54159	† TI			SN7416	SW			SH2200M	† Fairchild			
	SN74159	TI			SN5416	† TI	60						
					SN7416	TI							
					TD3416	Toshiba							
					7416	TRW							
Drivers				Hex Inverter Buffer/Driver, Open Collector High Voltage Output, to 30v.				Dual 4-Input AND Power Driver Open Collector (to 100v, sinks 250 ma)					
Quad Predriver, Open Collector				5406				† Fairchild	UHP-420				Sprague
	MC4042	Motorola			7406	Fairchild		UHP-520				Sprague	
Quad Driver, Common Enable Active Pull-Up (sinks to 120ma)				HD7406				Hitachi	Dual AND-OR Power Driver, Open Collector (to 100v, sinks 250ma)				
	IM5001	Intersil			ITT5406	† ITT		UHP-451				Sprague	
	IM5001M	† Intersil			ITT7406	ITT		UHP-459				Sprague	
	IM5011	Intersil			MC5406	† Motorola	70	UHP-551				Sprague	
	IM5011M	† Intersil			MC7406	Motorola		UHP-559				Sprague	
Quad 2-Input AND Buffer, Open Collector, to 15v Output (High voltage 54/74109)				DM5406				† National	Quad 2-Input AND Power Driver, Open Collector (to 100v, sinks 250 ma)				
	ITT54131	† ITT	10		DM7406	National		UHC/D-400				† Sprague	
	ITT74131	ITT			N7406	Signetics		UHC/D-406				† Sprague	
	DS7819	† National			S5406	† Signetics		UHC/D-500				† Sprague	
	DS8819	National			SN7406	† TI		UHC/D-506				† Sprague	
Hex Buffer/Driver, Open Collector High Voltage Output, to 15v				SN7406				TI	UHP-400				Sprague
	5417	† Fairchild			TD3406	Toshiba		UHP-406				Sprague	
	7417	Fairchild			7406	TRW		UHP-500				Sprague	
	HD7417	Hitachi						UHP-506				Sprague	
	ITT5417	† ITT		Hex High Voltage Interface Driver, Open Collector, to 35v					Quad 2-Input NAND Power Driver, Open Collector (to 100v, sinks 250 ma)				
	ITT7417	ITT			HD235	† Harris	80	UHC/D-407				† Sprague	
	MC5417	† Motorola			HD535	Harris		UHC/D-408				† Sprague	
	MC7417	Motorola		Quad 2-Input AND Buffer, Open Collector, to 30v Output					UHC/D-507				† Sprague
	DM5417	† National	20		ITT54130	† ITT		UHC/D-508				† Sprague	
	DM7417	National			ITT74130	ITT		UHP-407				Sprague	
	N7417	Signetics		Quad 2-Input NAND Buffer, Open Collector, to 15v Output					UHP-408				Sprague
	S5417	† Signetics			5426	† Fairchild		UHP-507				Sprague	
	SN7417	TI			7426	Fairchild		UHP-508				Sprague	
	SN7417	TI			HD2560	Hitachi		Quad 2-Input NAND Bus Driver, Open Collector, 80 ma					
	TD3417	Toshiba			HD7426	Hitachi		96101				Fairchild	
	7417	TRW			ITT5426	† ITT		Quad 2-Input OR Power Driver, Open Collector (to 100v, sinks 250 ma)					
Hex Buffer/Driver, Open Collector High Voltage Output, to 30v					ITT7426	ITT		UHC/D-402				† Sprague	
	5407	† Fairchild	30		MC5426	† Motorola	90	UHC/D-403				† Sprague	
	7407	Fairchild			MC7426	Motorola		UHC/D-502				† Sprague	
	HD7407	Hitachi			DM5426	† National		UHC/D-503				† Sprague	
	ITT5407	† ITT			DM7426	National		UHP-402				Sprague	
	ITT7407	ITT			DS7810	† National		UHP-403				Sprague	
	MC5407	† Motorola			DS7811	† National		UHP-502				Sprague	
	MC7407	Motorola			DS8810	National		UHP-503				Sprague	
	DM5407	† National			DS8811	National		Quad 2-Input NOR Power Driver, Open Collector (to 100v, sinks 250 ma)					
	DM7407	National			N7426	Signetics		UHC/D-432				† Sprague	
	N7407	Signetics			S5426	† Signetics	100	UHC/D-433				† Sprague	
	S5407	† Signetics	40		SN7426	SW		UHC/D-532				† Sprague	
	SN5407	† TI			SN5426	† TI		UHC/D-533				† Sprague	
	SN7407	TI			SN7426	TI		UHP-432				Sprague	
	TD3407	Toshiba			TD3426	Toshiba		UHP-433				Sprague	
	7407	TRW			7426	TRW		UHP-532				Sprague	
Hex Inverter Buffer/Driver Open Collector High Voltage Output, to 15v					7426	TRW		UHP-533				Sprague	
	5416	† Fairchild		Quad 2-Input NAND Buffer, Open Collector, to 30v Output					Quad 2-Input NOR 75-Ohm/50-Ohm Line Driver				
	7416	Fairchild			N8T80	Signetics		SN54128				† TI	
	HD7416	Hitachi			S8T80	† Signetics		SN74128				TI	
	ITT5416	† ITT		Quad 2-Input OR Buffer, Open Collector, to 15v Output					Hex Interface Inverter, Open Collector, to 50v or to 50 ma)				
	ITT7416	ITT			ITT54139	† ITT		HD234				† Harris	
	MC5416	† Motorola			ITT74139	ITT		HD334				† Harris	
	MC7416	Motorola		Quad 2-Input OR Buffer, Open Collector, to 30 v Output					HD534				Harris
	DM5416	† National	50		ITT54138	† ITT	110	Quad Bus Driver, Three-State					
	DM7416	National			ITT74138	ITT		RC8T09				Raytheon	
	DM7812	† National		4-Input NAND High Voltage, High Current Driver (40 to 50v, sinks 150 to 500 ma)					RM8T09				† Raytheon
	DS8812	National			SH2001C	Fairchild		N8T09				Signetics	
	(continued)				SH2001M	† Fairchild		S8T09				† Signetics	
					SH2002C	Fairchild		Hex Bus Driver, Gated Enable, Three-State					
					(continued)			DM54365				† National	
								DM74365				National	
								SN54365				† TI	
								SN74365				TI	

† Military Temperature Range (-55°C to 125°C)

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DIGITAL—TTL (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line					
Drivers (cont)				Flip-Flops (cont)				Flip-Flops (cont)								
Hex Bus Driver, Gated Enable, Inverted Three-State Output	DM54366	† National		AND Gated, Edge Triggered J-K Flip-Flop with Preset and Clear (continued)	DM7470	National	60	Dual J-K Master-Slave Flip-Flop with Preset and Clear	5476	† Fairchild	120					
	DM74366	National			N7470	Signetics			7476	Fairchild						
	SN54366	† TI			N8270	Signetics			9022C	Fairchild						
	SN74366	TI			S5470	† Signetics			9022M	† Fairchild						
Hex Bus Driver, 2-Line and 4-Line Enable, Three-State	DM54367	† National			S8270	† Signetics				ZN5476		† Ferranti	ZN7476	Ferranti		
	DM74367	National			SW7470	SW				HD2516		Hitachi				
	SN54367	† TI			SN5470	† TI				ITT5476		† ITT				
	SN74367	TI			SN7470	TI				ITT7476		ITT				
Hex Bus Driver, 2-Line and 4-Line Enable, Inverted Three-State Output	DM54368	† National	10		Dual J-K Positive-Edge Triggered Flip-Flop Preset and Clear	9024C			Fairchild	70		ITT9022-1	ITT	MC5476	† Motorola	130
	DM74368	National				9024M			† Fairchild			MC7476	Motorola			
	SN54368	† TI		74109		Fairchild	DM5476	† National								
	SN74368	TI		ITT9024-1		† ITT	DM7476	National								
Flip-Flops	J-K Master-Slave Flip-Flop	9000C	Fairchild	Dual J-K Master-Slave Flip-Flop		DM74109	National	80	ITT9024-5		ITT	N7476	Signetics	140		
		9000M	† Fairchild			DM74109	National		S5476		† Signetics					
		9001C	Fairchild			N74109	Signetics		SN7476		SW					
		9001M	† Fairchild			S54109	† Signetics		SN5476		† TI					
		54104	† Fairchild			SN54109	† TI		SN7476		TI					
		54105	† Fairchild			SN74109	TI		TD3476		Toshiba					
		74104	Fairchild		9020C	Fairchild	7476		TRW							
		74105	Fairchild		9020M	† Fairchild	Dual J-K Master-Slave Flip-Flop with Data Lockout		SN54111	† TI	140					
		ITT54104	† ITT		ITT9020-1	† ITT			SN74111	TI						
		ITT54105	† ITT		ITT9020-5	ITT			74111	TRW						
ITT74104	ITT	Dual J-K Master-Slave Flip-Flop with Clear	5473	† Fairchild	Dual Gated Master-Slave J-K/D Flip-Flop	DM7512		† National	150							
ITT74105	ITT		7473	Fairchild		DM8512	National									
SW74104	SW		54107	† Fairchild		Quad J-K Edge Triggered Flip-Flop with Clear	SN54376	† TI		140						
AND Gated J-K Master-Slave Flip-Flop with Preset and Clear	5472		† Fairchild	74107			Fairchild	SN74376			TI					
	7472	Fairchild	ZN5473	† Ferranti	Quad J-K Edge-Triggered Flip-Flop with Preset and Clear		SN74276	TI								
	ZN5472	† Ferranti	ZN7473	Ferranti			Dual D-Type Flip-Flop	MC5479	† Motorola							
	ZN7472	Ferranti	ZN54107	† Ferranti		MC7479		Motorola								
	HD2529	Hitachi	ZN74107	Ferranti		Dual D-Type Positive Edge-Triggered Flip-Flop with Preset and Clear		5474	† Fairchild	150						
	HD7472	Hitachi	HD2515	Hitachi	7474			Fairchild								
	ITT5472	† ITT	HD2530	Hitachi	ZN5474		† Ferranti									
	ITT7472	ITT	HD74107	Hitachi	ZN7474		Ferranti									
	MC5472	† Motorola	ITT5473	† ITT	HD2510		Hitachi									
	MC7472	Motorola	ITT7473	ITT	HD7474		Hitachi									
DM5472	† National	ITT54107	† ITT	ITT5474	† ITT											
DM7472	National	ITT74107	ITT	ITT7474	ITT											
N7472	Signetics	MC5473	† Motorola	DM5474	† National											
S5472	† Signetics	MC7473	Motorola	DM7474	National											
SW7472	SW	MC54107	† Motorola	5474	† Raytheon											
SN5472	† TI	MC74107	Motorola	7474	Raytheon											
SN7472	TI	DM5473	† National	N7474	Signetics											
TD3472	Toshiba	DM7473	National	S5474	† Signetics											
7472	TRW	DM54107	† National	SW7474	SW											
AND-Gated J-K Master-Slave Flip-Flop with Data Lockout	SN54110	† TI		DM74107	National	100	SN5474	† TI	160							
	SN74110	TI		DM74107	National											
AND Gated, Edge Triggered J-K Flip-Flop with Preset and Clear	5470	† Fairchild	50	N7473	Signetics	110	SN7474	TI	170							
	7470	Fairchild		N74107	Signetics		TD3474	Toshiba								
	ZN5470	† Ferranti		S5473	† Signetics		7474	TRW								
	ZN7470	Ferranti		S54107	† Signetics		Dual Gated D Flip-Flop	DM7511		† National						
	HD2539	Hitachi		SW7473	SW			DM8511		National						
	ITT5470	† ITT		SN5473	† TI			Quad Gated D Flip-Flop		DM7613	† National					
	ITT7470	ITT		SN7473	† TI					DM8613	National					
	MC5470	† Motorola		SN54107	† TI		Quad D-Type Flip-Flop, Common Clock			MC4015	Motorola					
	MC7470	Motorola		SN74107	TI					RL4015	Raytheon					
	DM5470	† National		TD3473	Toshiba											
	(continued)			TD34107	Toshiba											

† Military Temperature Range (–55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

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DIGITAL—TTL (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line		
Flip-Flops (cont)				Gates, AND/NAND (cont)				Gates, AND/NAND (cont)					
Quad D-Type Flip-Flop, Three-State				Dual 4-Input AND Gate (continued)				8-Input NAND Gate (continued)					
	DM54173	† National	10		N7421	Signetics	60		ZN5430	† Ferranti	120		
	DM74173	National			S5421	† Signetics			ZN7430	Ferranti			
	DM7551	† National			TD3421	Toshiba			HD2508	Hitachi			
	DM8551	National							HD7430	Hitachi			
	RC8T10	Raytheon			Triple 3-Input AND Gate					ITT5430		† ITT	
	RM8T10	† Raytheon				5411		† Fairchild		ITT7430		ITT	
	N8T10	Signetics				7411		Fairchild		MC5430		† Motorola	
	S8T10	† Signetics				ITT5411		† ITT		MC7430		Motorola	
	SN54173	† TI				ITT7411		ITT		DM5430		† National	
	SN74173	TI				DM5411		† National		DM7430		National	
Quad D-Type Edge-Triggered Flip-Flop with Clear, Complementary Output					DM7411	National		N7430	Signetics		130		
	SN54175	† AMD	20		5411	† Raytheon		S5430	† Signetics				
	SN74175	AMD				7411	Raytheon		SW7430	SW			
	54175	† Fairchild				N7411	Signetics		SN5430	† TI			
	74175	Fairchild				S5411	† Signetics		SN7430	TI			
	ZN54175	† Ferranti			Triple 3-Input AND Gate, Open Collector					TD3430		Toshiba	
	ZN74175	Ferranti				5415	† Raytheon		7430	TRW			
	HD74175	Hitachi				7415	Raytheon						
	DM54175	† National			Quad 2-Input AND Gate								
	DM74175	National				5408	† Fairchild		Dual 4-Input NAND Gate				
	54175	† Raytheon				7408	Fairchild			5420	† Fairchild	140	
	74175	Raytheon			ZN5408	† Ferranti			7420	Fairchild			
	N74175	Signetics			ZN7408	Ferranti			9004C	Fairchild			
	S54175	† Signetics			HD2550	Hitachi			9004M	† Fairchild			
	SW74175	SW			ITT5408	† ITT			ZN7420	Ferranti			
	SN54175	† TI			ITT7408	ITT			ZN5420	† Ferranti			
	SN74175	TI			MC5408	† Motorola			HD2504	Hitachi			
					MC7408	Motorola			HD7420	Hitachi			
					DM5408	† National			ITT5420	† ITT			
					DM7408	National			ITT7420	ITT			
Quad I/O Register, Three-State (two terminals per flip-flop can be used as input or output)					5408	† Raytheon			ITT9004-1	ITT	150		
	DM7542	† National	30		7408	Raytheon			ITT9004-5	† ITT			
	DM8542	National				N7408	Signetics			MC5420		† Motorola	
Quad, Selectable Input, Edge-Triggered Flip-Flop					S5408	† Signetics			MC7420	Motorola			
	54298	† Fairchild				SW7408	SW			DM5420		† National	
	74298	Fairchild				SN5408	† TI			DM7420		National	
	SN54298	† TI				SN7408	TI			DM9004C		National	
	SN74298	TI				TD3408	Toshiba			5420		† Raytheon	
						7408	TRW			7420		Raytheon	
										N7420		Signetics	
										S5420	† Signetics		
Hex D-Type, Edge-Triggered Flip-Flop with Clear									SW7420	SW	160		
	SN54174	† AMD	40	Quad 2-Input AND Gate, Open Collector					SN5420	† TI			
	SN74174	AMD				5409	† Fairchild		SN7420	TI			
	54174	† Fairchild				7409	Fairchild		TD3420	Toshiba			
	74174	Fairchild				ZN5409	Ferranti		7420	TRW			
	93174C	Fairchild				ZN7409	Ferranti		Dual 4-Input NAND Buffer				
	ZN54174	† Ferranti				HD2551	Hitachi			5440		† Fairchild	
	ZN74174	Ferranti				ITT5409	† ITT			7440		Fairchild	
	HD74174	Hitachi				ITT7409	ITT			9009C		Fairchild	
	DM54174	† National				MC5409	† Motorola			9009M		† Fairchild	
	DM74174	National				MC7409	Motorola			ZN5440	† Ferranti		
	54174	† Raytheon			DM5409	† National			ZN7440	Ferranti			
	74174	Raytheon			DM7409	National			HD2501	Hitachi			
	N74174	Signetics			5409	† Raytheon			HD7440	Hitachi			
	S54174	† Signetics			7409	Raytheon			ITT5440	† ITT			
	SW74174	SW			N7409	Signetics			ITT7440	ITT			
	SN54174	† TI			S5409	† Signetics			ITT9009-1	† ITT			
	SN74174	TI			SW7409	SW			ITT9009-5	ITT			
					SN5409	† TI			MC5440	† Motorola			
Octal D-Type, Edge-Triggered Flip-Flop, with Clear					SN7409	TI			MC7440	Motorola	170		
	SN74273	TI	50		TD3409	Toshiba			DM5440	† National			
Gates, AND/NAND					7409	TRW			DM7440	National			
Dual 4-Input AND Gate					8-Input NAND Gate					DM9009C		National	
	5421	† Fairchild	110		5430	† Fairchild			(continued)	(continued)			
	7421	Fairchild				7430	Fairchild						
	ITT5421	† ITT				9007C	Fairchild						
	ITT7421	ITT				9007M	† Fairchild						
	5421	† Raytheon				(continued)							
	7421	Raytheon											
	(continued)												

† Military Temperature Range (–55°C to 125°C)

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Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line				
Gates, AND/NAND (cont)				Gates, AND/NAND (cont)				Gates, AND/NAND (cont)							
Dual 4-Input NAND Buffer (continued)	N7440	Signetics		Quad 2-Input NAND Gate (continued)	9002M	† Fairchild	60	Quad 2-Input NAND Gate, Open Collector (continued)	MC7401	Motorola	120				
	S5440	† Signetics			ZN5400	† Ferranti			MC7403	Motorola					
	SW7440	SW			ZN7400	Ferranti			DM5401	† National					
	SN5440	† TI			HD2503	Hitachi			DM5403	† National					
	SN7440	TI			HD7400	Hitachi			DM7401	National					
	TD3440	Toshiba			ITT5400	† ITT			DM7403	National					
	7440	TRW			ITT7400	ITT			DM9012C	National					
Dual 4-Input NAND Gate, Open Collector	5422	† Fairchild	10		ITT9002-1	† ITT			5401	† Raytheon					
	7422	Fairchild				ITT9002-5	ITT		7401	Raytheon					
	HD7422	Hitachi				MC5400	† Motorola	70	5403	† Raytheon	130				
	5422	† Raytheon				MC7400	Motorola		7403	Raytheon					
	7422	Raytheon				DM5400	† National		S5401	† Signetics					
	SN5422	† TI				DM7400	National		S5403	† Signetics					
	SN7422	TI			DM9002C	National	S7401		Signetics						
Dual 5-Input NAND Gate	DM7092	† National			5400	† Raytheon		S7403	Signetics						
	DM8092	National			7400	Raytheon		SW7401	SW						
Triple 3-Input NAND Gate	5410	† Fairchild	20	Quad 2-Input NAND Buffer	5437	† Fairchild	80	Quad 2-Input NAND Buffer, Open Collector	5438	† Fairchild	150				
	7410	Fairchild				7437		Fairchild		7438		Fairchild			
	9003C	Fairchild				ZN5437		† Ferranti		7439		Fairchild			
	9003M	† Fairchild				HD2552		Hitachi		ZN5438		† Ferranti			
	ZN5410	† Ferranti				ITT5437		† ITT		ZN7438		Ferranti			
	ZN7410	Ferranti				ITT7437		ITT		HD2544		Hitachi			
	HD2507	Hitachi				MC5437		† Motorola	90	ITT5438		† ITT			
	HD7410	Hitachi				MC7437		Motorola				ITT7438	ITT		
	ITT5410	† ITT				DM5437		† National				MC5438	† Motorola		
	ITT7410	ITT				DM7091		† National				MC7438	Motorola		
	ITT9003-1	† ITT				DM7437		National				DM5438	† National		
	ITT9003-5	ITT				DM8091		National				DM7438	National		
	MC5410	† Motorola		30		N7437		Signetics				N7438	Signetics		
	MC7410	Motorola						S5437		† Signetics			N7439	Signetics	
	DM5410	† National						SW7437		SW			S5438	† Signetics	
	DM7410	National						SN5437		† TI			S5439	† Signetics	
	DM9003C	National						SN7437		TI		100	S5439	† Signetics	
	5410	† Raytheon						TD3437		Toshiba				SN7438	SW
	7410	Raytheon						7437		TRW				SN5438	† TI
	N7410	Signetics							SN7438	TI					
	S5410	† Signetics	40						TD3438	Toshiba					
	SW7410	SW								7438	TRW				
	SN5410	† TI													
	SN7410	TI													
	TD3410	Toshiba													
	7410	TRW													
Triple 3-Input NAND Gate, Open Collector	5412	† Fairchild	50	Quad 2-Input NAND Gate, Open Collector	5401	† Fairchild	110	Gates, AND-OR-Invert							
	7412	Fairchild				5403		† Fairchild		2-2-2-3-Input AND-OR-Invert Gate, Expandable					
	ZN5412	† Ferranti				7401		Fairchild		9008C	Fairchild				
	ZN7412	Ferranti				7403		Fairchild		9008M	† Fairchild				
	HD7412	Hitachi				9012C		Fairchild		ITT9008-1	† ITT				
	ITT5412	† ITT				9012M		† Fairchild		ITT9008-5	ITT				
	ITT7412	ITT				ZN5401		† Ferranti		DM9008C	National	170			
	5412	† Raytheon				ZN7401		Ferranti		4-Wide 2-Input AND-OR-Invert Gate					
	7412	Raytheon				HD2509		Hitachi		5454	† Fairchild				
	N7412	Signetics				HD2528		Hitachi		7454	Fairchild				
	S5412	† Signetics				HD7403		Hitachi		ZN5454	† Ferranti				
	SN5412	† TI				ITT5401		† ITT		ZN7454	Ferranti				
	SN7412	TI				ITT5403		† ITT		HD2514	Hitachi				
	7412	TRW			ITT7401	ITT		HD7454	Hitachi						
					ITT7403	ITT		(continued)							
Quad 2-Input NAND Gate	5400	† Fairchild			MC5401	† Motorola									
	7400	Fairchild			MC5403	† Motorola									
	9002C	Fairchild			(continued)										
	(continued)														

† Military Temperature Range (–55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

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Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line				
Gates, AND-OR-Invert (cont)				Gates, AND-OR-Invert (cont)				Gates, Exclusive OR/NOR (cont)							
4-Wide 2-Input AND-OR-Invert Gate (continued)	ITT5454	† ITT	10	Dual 2-Wide 2-Input AND-OR-Invert Gate (one gate is expandable) (continued)	HD7450	Hitachi	60	Quad 2-Input Exclusive-OR Gate (continued)	N7486	Signetics	120				
	ITT7454	ITT				ITT5450		† ITT				N8241	Signetics		
	MC5454	† Motorola				ITT7450		ITT				S5486	† Signetics		
	MC7454	Motorola				ITT9005-1		† ITT				S8241	† Signetics		
	DM5454	† National				ITT9005-5		ITT				SW7486	SW		
	DM7454	National				MC5450		† Motorola				SN5486	† TI		
	N7454	Signetics				MC7450		Motorola				SN7486	TI		
	S5454	† Signetics				DM5450		† National				7486	TRW		
	SW7454	SW				DM7450		National				Quad 2-Input Exclusive OR Gate (two of the outputs are complemented)			
	SN5454	† TI				DM9005C		National	70			9014C	Fairchild		
	SN7454	TI				N7450		Signetics					9014M	† Fairchild	
	7454	TRW				S5450		† Signetics				Quad 2-Input Exclusive-OR Gate, Open Collector			
4-Wide 2-Input AND-OR-Invert Gate, Expandable	5453	† Fairchild		20	Dual 4-Input Expander (for 54/7423, 54/7450, 54/7453)	SW7450		SW					HD74136	Hitachi	130
	7453	Fairchild				SN5450	† TI				54136	† Raytheon			
	ZN5453	† Ferranti				SN7450	TI				74136	Raytheon			
	ZN7453	Ferranti				TD3450	Toshiba				SN54136	† TI			
	HD2512	Hitachi				7450	TRW				SN74136	TI			
	HD2578	Hitachi									74136	TRW			
	HD7453	Hitachi								Quad Exclusive NOR Gate, Open Collector					
	ITT5453	† ITT				5460	† Fairchild				9386C	Fairchild			
	ITT7453	ITT				7460	Fairchild				9386M	† Fairchild			
	MC5453	† Motorola				ZN5460	† Ferranti	80			MC7242	Motorola			
	MC7453	Motorola				ZN7460	Ferranti				MC8242	† Motorola			
	DM5453	† National				HD2502	Hitachi				RC8242	Raytheon			
	DM7453	National				HD7460	Hitachi				RM8242	† Raytheon			
	N7453	Signetics			ITT5460	† ITT				N8242	Signetics				
	S5453	† Signetics			ITT7460	ITT				S8242	† Signetics				
	SW7453	SW			MC5460	† Motorola			Gates, OR/NOR						
	SN5453	† TI			MC7460	Motorola			(Sequence OR, NOR, OR/NOR,)						
	SN7453	TI	30		DM5460	† National			Quad 2-Input OR Gate						
	7453	TRW				DM7460	National				5432	† Fairchild			
Dual 2-Wide 2-Input AND-OR-Invert Gate	5451	† Fairchild				N7460	Signetics				7432	Fairchild			
	7451	Fairchild				S5460	† Signetics		90		ZN5432	† Ferranti			
	ZN7451	Ferranti				SW7460	SW					ZN7432	Ferranti		
	ZN5451	† Ferranti				SN5460	† TI				HD7432	Hitachi			
	HD2505	Hitachi				SN7460	TI				ITT5432	† ITT			
	HD7451	Hitachi				TD3460	Toshiba				ITT7432	ITT			
	ITT5451	† ITT				7460	TRW				DM5432	† National			
	ITT7451	ITT									DM7432	National			
	MC5451	† Motorola									N7432	Signetics			
	MC7451	Motorola		40	Dual 4-Input Extender (for 9005, 9008)	9006C	Fairchild				S5432	† Signetics			
	DM5451	† National					9006M	† Fairchild				SW7432	SW		
	DM7451	National				DM9006C	National				SN5432	† TI			
	N7451	Signetics									SN7432	TI			
	S5451	† Signetics			Gates, Exclusive OR/NOR						2-2-2-4 Input NOR Gate				
	SW7451	SW				Quad 2-Input Exclusive-OR Gate				9015C	Fairchild				
	SN5451	† TI				5486	† Fairchild	100		9015M	† Fairchild				
	SN7451	TI				7486	Fairchild			Dual 4-Input NOR Gate, with Strobe					
	TD3451	Toshiba				ZN5486	† Ferranti				5425	† Fairchild			
	7451	TRW	50			ZN7486	Ferranti				7425	Fairchild			
Dual 2-Wide 2-Input AND-OR-Invert Gate (one gate is expandable)	5450	† Fairchild					HD2526		Hitachi			ZN5425	† Ferranti		
	7450	Fairchild					HD7486		Hitachi			ZN7425	Ferranti		
	5460	† Fairchild					ITT5486		† ITT			ITT5425	† ITT		
	7460	Fairchild				ITT7486	ITT				ITT7425	ITT			
	9005C	Fairchild				MC5486	† Motorola				DM5425	† National			
	9005M	† Fairchild				MC7241	Motorola				DM7425	National			
	ZN5450	† Ferranti				MC7486	Motorola				SW7425	SW			
	ZN7450	Ferranti				MC8241	† Motorola		110		SN5425	† TI			
	HD2506	Hitachi				DM5486	National					SN7425	TI		
	(continued)					DM7486	National			Dual 4-Input NOR Gate, with Strobe, Expandable (see 54/7460 Expander)					
						5486	† Raytheon				5423	† Fairchild			
						7486	Raytheon				7423	Fairchild			
					RC8241	Raytheon				DM5423	† National				
					RM8241	† Raytheon				(continued)					
					(continued)										

† Military Temperature Range (-55°C to 125°C)

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Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line	
Gates, OR/NOR (cont)				Latches (cont)				Latches (cont)				
Dual 4-Input NOR Gate, with Strobe, Expandable (see 54/7460 Expander) (continued)				8-Bit Latch, Three-State (input and output through the same leads)				Quad Set-Reset Latch				
	DM7423	National			DM7553	† National			54279	† Fairchild		
	SN7423	SW			DM8553	National			74279	Fairchild		
	SN5423	† TI		Dual 4-Bit Latch					S54279	† Signetics		
	SN7423	TI			MC54100	† Motorola			N74279	Signetics		
Triple 3-Input NOR Gate					MC74100	Motorola		Hex Set-Reset Latch (Common Reset)				
	5427	† Fairchild			N74100	Signetics	60		ZN54118	† Ferranti		
	7427	Fairchild			S54100	† Signetics			ZN54119	† Ferranti		
	ZN5427	† Ferranti			SN74100	SW			ZN74118	Ferranti	120	
	ZN7427	Ferranti			SN54100	† TI			ZN74119	Ferranti		
	HD7427	Hitachi		Dual 4-Bit Latch with Clear						ITT54118	† ITT	
	DM5427	† National	10		9308C	AMD		Memories				
	DM7427	National			9308M	† AMD		For additional information on these and larger TTL compatible memories, see the Master Selection Guide—Memory section				
	SN7427	SW			9308C	Fairchild		8-Bit (4x2) Content Addressable Memory				
	SN5427	† TI			9308M	† Fairchild			N8220	Signetics		
	SN7427	TI			54116	† Fairchild			N8222	Signetics		
Quad 2-Input NOR Gate (54/7428 devices are also buffers)					74116	Fairchild			S8222	† Signetics		
	5402	† Fairchild		Quad 4-Bit Latch with Clear					8-Bit Multiport Register (RAM with simultaneous Read/Write)			
	7402	Fairchild			9314C	AMD			9338C	AMD		
	ZN5428	† Ferranti			9314M	† AMD	80		9338M	† AMD		
	ZN7428	Ferranti			9314C	Fairchild			9338C	Fairchild	130	
	HD2511	Hitachi			9314M	† Fairchild		16-Bit Active Element Memory				
	HD7402	Hitachi	20		MC8314	Motorola			93407C	Fairchild		
	ITT5402	† ITT			MC9308	† Motorola			93407M	† Fairchild		
	ITT7402	ITT			RM9308	† Raytheon			93433C	† Fairchild		
	ITT5428	† ITT			RC9308	Raytheon			HM2501	Hitachi		
	ITT7428	ITT			SN29308	TI			MC4004	Motorola		
	MC5402	† Motorola			SN39308	† TI			MC4005	Motorola		
	MC7402	Motorola			SN54116	† TI			MC4304	† Motorola		
	DM5402	† National		Quad Multifunction Latch						MC4305	† Motorola	140
	DM7402	National			9314C	AMD			5481	† Raytheon		
	N7402	Signetics			9314M	† AMD	80		7481	Raytheon		
	S5402	† Signetics			9314C	Fairchild		16-Bit Active Element Memory, Gated Write				
	SN7402	SW	30		9314M	† Fairchild			SN5484A	† TI		
	SN5402	† TI			MC8314	Motorola			SN7484A	TI		
	SN5428	† TI			MC9314	† Motorola		16-Bit (4x4) Register File, Simultaneous Read/Write				
	SN7402	TI			Quad Bistable Latch, Single Output					54170	† Fairchild	
	SN7428	TI				5477	† Fairchild		74170	Fairchild		
	7402	TRW				7477	Fairchild		ZN54170	† Ferranti	150	
Quad 2-Input NOR Buffer, Open Collector						MC5477	† Motorola		ZN74170	Ferranti		
	ITT5433	† ITT			MC7477	Motorola			HD2540	Hitachi		
	ITT7433	ITT			N7477	Signetics			DM74170	National		
	SN5433	† TI			S5477	† Signetics	90		54170	† Raytheon		
	SN7433	TI	40		SN5477	† TI			74170	Raytheon		
					SN7477	TI			N74170	Signetics		
Gates, Miscellaneous									S54170	† Signetics		
Quad Inverter and Dual 2-Input NAND Gate									SN54170	† TI		
	DM7090	† National		Quad Bistable Latch, Complementary Outputs					SN74170	TI		
	DM8090	National			5475	† Fairchild		16-Bit (8x2) Multiport Register File, Simultaneous Read/Write, Three-State				
Dual Majority Logic Gate						7475	Fairchild			N74172	Signetics	160
	MC4062	Motorola			ZN5475	† Ferranti			SN74172	TI		
Latches						ZN7475	Ferranti		16-Bit (4x4) Content Addressable Memory			
8-Bit Addressable Latch, with Clear						HD2517	Hitachi			3104	Intel	
	9334C	AMD			HD7475	Hitachi		64-Bit (16x4) RAM with output register				
	9334M	† AMD			ITT5475	† ITT	100		9410C	Fairchild		
	SN54259	† AMD			ITT7475	ITT			9410M	† Fairchild		
	SN74259	AMD			MC5475	† Motorola						
	9334C	Fairchild			MC7475	Motorola						
	9334M	† Fairchild			DM5475	† National						
	DM8334	National	50		DM7475	National						
	DM9334	† National			N7575	Signetics						
	SN54259	† TI			S5475	† Signetics						
	SN74259	TI			SN7475	SW						
					SN5475	† TI						
					SN7475	TI						
					TD3475	Toshiba	110					
					7475	TRW						

† Military Temperature Range (–55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

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Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line
Multiplexers				Multiplexers (cont)				Multiplexers (cont)			
Quad 2-Input Multiplexer, Non-Inverting	9322C	AMD	10	Quad 2-Input Multiplexer, Inverting, Open Collector	RC8234	Raytheon	60	8-Input Multiplexer, Inverted Output (continued)	DM7211	† National	120
	9322M	† AMD			RM8234	† Raytheon			DM8210	National	
	SN54157	† AMD			N8234	Signetics			DM8211	National	
	SN74157	AMD		S8234	† Signetics	54152	† Raytheon				
	9322C	Fairchild		Quad 2-Input Multiplexer, Conditional Complementing, Open Collector	N8235	Signetics	74152		Raytheon		
	9322M	† Fairchild			S8235	† Signetics	S54152		† Signetics		
	54157	† Fairchild			Quad 3-Input Multiplexer, Conditional Complementing	RC8263	Raytheon		SN54152A	† TI	
	74157	Fairchild		RC8263		Raytheon	74152		TRW		
	ZN54157	† Ferranti		RM8263		† Raytheon	8-Input Multiplexer, Complementary Output		9312C	AMD	
	ZN74157	Ferranti		N8263	Signetics	9312M			† AMD		
	HD74157	Hitachi		S8263	† Signetics	9312C		Fairchild			
	ITT9322-1	ITT		Quad 3-Input Multiplexer, Open Collector, Conditional Complementing, Output Enable	RC8264	Raytheon		9312M	† Fairchild		
	ITT9322-5	ITT			RM8264	† Raytheon		ITT9312-1	† ITT		
	ITT74157	ITT			N8264	Signetics		ITT9312-5	ITT		
	ITT54157	† ITT		S8264	Signetics	MC8312		Motorola	130		
	MC9322	† Motorola		Dual 4-Input Multiplexer	SN54153	† AMD		MC9312		† Motorola	
	MC8322	Motorola			SN74153	AMD		DM8312		National	
	MC54157	† Motorola			54153	† Fairchild		DM9312		† National	
	MC74157	Motorola		74153	Fairchild	RC8230	Raytheon	140			
	DM8322	National		ZN54153	† Ferranti	RC8232	Raytheon				
	DM9322	† National		ZN74153	Ferranti	RC9312	Raytheon				
	DM54157	† National		HD2564	Hitachi	RM8230	† Raytheon				
DM74157	National	ITT54153	† ITT	RM8232	† Raytheon						
RC8233	Raytheon	ITT74153	ITT	RM9312	† Raytheon	140					
RM8233	† Raytheon	MC4000	Motorola	N8230	Signetics						
RC9322	Raytheon	MC4300	† Motorola	N8232	Signetics						
RM9322	† Raytheon	MC54153	† Motorola	S8230	† Signetics						
54157	† Raytheon	MC74153	Motorola	S8232	† Signetics						
74157	Raytheon	DM54153	† National	SN29312	TI						
N8233	Signetics	DM74153	National	SN39312	† TI						
S8233	† Signetics	54153	† Raytheon	8-Input Multiplexer, Complementary Output, Strobe	54151		† Fairchild				
N74157	Signetics	74153	Raytheon		74151		Fairchild				
S54157	† Signetics	N74153	Signetics		ZN54151		† Ferranti				
SN74157	SW	S54153	† Signetics		ZN74151	Ferranti					
SN54157	† TI	SN74153	SW		HD2549	Hitachi					
SN74157	TI	SN54153	† TI		HD2571	Hitachi					
Quad 2-Input Multiplexer, (Three-State 54/74157)	DM7123	National	30		SN74153	TI	HD74151	Hitachi			
	DM8123	† National			74153	TRW	ITT54151	† ITT			
Quad 2-Input Multiplexer with Storage	54298	† Fairchild	40		Dual 4-Input Multiplexer (Three-State 54/74153)	DM7214	† National	150			
	74298	Fairchild				DM8214	National				
	SN54298	† TI		Dual 4-Input Multiplexer, Complementary Output		9309C	AMD				
	SN74298	TI				9309M	† AMD				
Quad 2-Input, Multiplexer (for adder, register input)	MC7266	Motorola	9309C			Fairchild					
	MC8266	† Motorola	9309M	† Fairchild							
	RC8266	Raytheon	ITT9309-1	† ITT							
RM8266	† Raytheon	ITT9309-5	ITT	100							
N8266	Signetics	MC8309	Motorola								
S8266	† Signetics	MC9309	† Motorola								
Quad 2-Input, Multiplexer, Open Collector (for adder, register input)	MC7267	Motorola	DM8309		National						
	MC8267	† Motorola	DM9309		National						
	RC8267	Raytheon	N9309		Signetics						
	RM8267	† Raytheon	S9309		† Signetics						
	N8267	Signetics	SN29309		TI						
S8267	† Signetics	SN39309	† TI		110						
Quad 2-Input Multiplexer, Inverting	54158	† Raytheon	8-Input Multiplexer, Inverted Output			54152	† Fairchild	170			
	74158	Raytheon		74152	Fairchild						
	N74158	Signetics		MC54152	† Motorola						
	S54158	† Signetics		MC74152	Motorola						
	Quad 2-Input Multiplexer, (Three-State 54/74151)	DM7121		† National	DM7210	† National					
		DM8121		National	(continued)						
Quad 2-Input Multiplexer, Inverted Output (continued)	9313C	Fairchild	8-Input Multiplexer, Complementary Output, Open Collector	9313C	Fairchild	170					
	9313M	† Fairchild		9313M	† Fairchild						
	RC8231	Raytheon		RC8231	Raytheon						
	RM8231	† Raytheon		RM8231	† Raytheon						
	N8231	Signetics		N8231	Signetics						
	S8231	† Signetics		S8231	† Signetics						

† Military Temperature Range (–55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

DIGITAL—TTL (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line
Multiplexers (cont)				Multivibrators (cont)				Multivibrators (cont)			
8-Input Multiplexer, Three-State Strobe	DM54251	† National		Retriggerable Monostable Multivibrator (continued)	RF8601	Raytheon		Dual Retriggerable Monostable Multivibrator with Clear (AND Triggered) (continued)	ZN74123	Ferranti	
	DM74251	National			RF9601	† Raytheon	60		HD2561	Hitachi	
	SN54251	† TI			RC8T22	Raytheon			DM54123	† National	
	SN74251	TI			RM8T22	† Raytheon			DM74123	National	
Dual 8-Input Multiplexer (two 8-to-1 sections)	SN74351	TI			N8T22	Signetics			54123	† Raytheon	120
16-Input Multiplexer, Inverted Output, Strobe	54150	† Fairchild		Retriggerable Monostable Multivibrator, with Reset	9600C	AMD			74123	Raytheon	
	74150	Fairchild	10		9600M	† AMD			N74123	Signetics	
	ZN54150	† Ferranti			AM2600C	AMD			S54123	† Signetics	
	ZN74150	Ferranti			AM2600M	† AMD			SW74123	SW	
	HD2548	Hitachi			9600C	Fairchild			SN54123	† TI	
	HD74150	Hitachi			9600M	† Fairchild			SN74123	TI	
	ITT54150	† ITT							74123	TRW	
	ITT74150	ITT		Retriggerable Monostable Multivibrator with Clear	54122	† Fairchild	70	Dual Monostable Multivibrator (Double-Edge)	DM7853	† National	
	MC54150	† Motorola			74122	Fairchild			DM8853	National	
	MC74150	Motorola			ZN54122	† Ferranti		Dual Voltage-Controlled Multivibrator	11C24C	Fairchild	
	DM54150	† National			ZN74122	Ferranti			MC4024	Motorola	130
	DM74150	National			ITT54122	† ITT			MC4324	† Motorola	
	54150	† Raytheon			ITT74122	ITT		Universal Pulse Generator	ITT54124	† ITT	
	74150	Raytheon			N74122	Signetics			ITT74124	ITT	
	N74150	Signetics	20		SW74122	SW		Shift Registers			
	S54150	† Signetics		Bidirectional Monostable Multivibrator (Low Level Input)	RC8T20	Raytheon	80	4-Bit Parallel Input, Parallel Output Shift Register	9300C	AMD	
	SW74150	SW			RM8T20	† Raytheon			9300M	† AMD	
	SN54150	† TI			N8T20	Signetics			SN54195	† AMD	
	SN74150	TI			S8T20	† Signetics			SN74195	AMD	
	74150	TRW							9300C	Fairchild	
16-Input Multiplexer (Three-State 54/74150)	DM7219	† National		Dual Monostable Multivibrator, Schmitt-Trigger Input (Dual 54/74121)	SN54221	† AMD			9300M	† Fairchild	140
	DM8219	National			SN74221	AMD			54195	† Fairchild	
Multivibrators					SN54221	† TI			74195	Fairchild	
Monostable Multivibrator, Schmitt Trigger Input	54121	† Fairchild			SN74221	TI			ITT9300-1	† ITT	
	74121	Fairchild	30	Dual Retriggerable Monostable Multivibrator with Reset (OR Triggered)	9602C	AMD			ITT9300-5	ITT	
	ZN54121	† Ferranti			9602M	† AMD	90		ITT54195	† ITT	
	ZN74121	Ferranti			96L02C	Fairchild			ITT74195	ITT	
	HD2543	Hitachi			96L02M	† Fairchild			MC8300	Motorola	
	HD74121	Hitachi			9602M	† AMD			MC9300	† Motorola	
	ITT54121	† ITT			AM2602C	AMD			MC54195	† Motorola	
	ITT74121	ITT			AM2602M	† AMD			MC74195	Motorola	
	MC54121	† Motorola			9602C	Fairchild			DM8300	National	150
	MC74121	Motorola			9602M	† Fairchild			DM9300	† National	
	DM54121	† National			ITT9602-1	† ITT			DM54195	† National	
	DM74121	National			ITT9602-5	ITT			DM74195	National	
	N74121	Signetics	40		MC8602	Motorola			RC9300	Raytheon	
	S54121	† Signetics			MC9602	† Motorola	100		RM9300	† Raytheon	
	SW74121	SW			DM8602	National			54195	† Raytheon	
	SN54121	† TI			DM9602	† National			74195	Raytheon	
	SN74121	TI			RF8602	Raytheon			N9300	Signetics	
	TD34121	Toshiba			RF9602	† Raytheon			N74195	Signetics	
	74121	TRW			N9602	Signetics			S9300	† Signetics	160
Retriggerable Monostable Multivibrator	9601C	AMD			S9602	† Signetics			S54195	† Signetics	
	9601M	† AMD			SW9602	SW			SN29300	TI	
	9601C	Fairchild		Dual Retriggerable Monostable Multivibrator with Clear (AND Triggered)	AM26123C	AMD			SN39300	† TI	
	9601M	† Fairchild	50		AM26123M	† AMD			SN54195	† TI	
	ITT9601-1	ITT			SN74123	AMD			SN74195	TI	
	ITT9601-5	† ITT			54123	† Fairchild			4-Bit Parallel-In, Parallel Out, Right/Left Shift Register		
	MC8601	Motorola			74123	Fairchild			5495	† Fairchild	
	MC9601	† Motorola			ZN54123	† Ferranti			7495	Fairchild	
	DM8601	National			(continued)				ZN5495A	† Ferranti	
	DM9601	† National							ZN7495A	Ferranti	
(continued)									HD2534	Hitachi	
									(continued)		170

† Military Temperature Range (-55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

DIGITAL—TTL (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line			
Shift Registers (cont)				Shift Registers (cont)				Shift Registers (cont)						
4-Bit Parallel-In, Parallel Out, Right/Left Shift Register (continued)	ITT5495	† ITT	10	4-Bit Parallel-In, Serial-Out, Shift Register, with Reset, Complementary Output for last bit (continued)	RM8271	† Raytheon	60	8-Bit Parallel-In, Serial-Out Shift Register, Complementary Output (continued)	SN74165	TI	120			
	ITT7495	ITT			N8271	Signetics			8-Bit Parallel-In, Serial Out Shift Register with Clear	54166		† Fairchild		
	MC4012	Motorola			S8271	† Signetics				74166		Fairchild		
	MC5495	† Motorola			SN54179	† TI				ZN54166		† Ferranti		
	MC7495	Motorola		SN74179	TI	ZN74166	Ferranti							
	DM5495	† National		5-Bit Parallel-In, Parallel-Out, Shift Register	5496	† Fairchild	HD74166		Hitachi	70		DM54166	† National	130
	DM7495	National			7496	Fairchild	DM74166		National					
	N7495	Signetics			ZN5496	† Ferranti	54166		† Raytheon					
	S5495	† Signetics			ZN7496	Ferranti	74166		Raytheon					
	SW7495	SW		HD2546	Hitachi	ITT5496	† ITT		80	N74166		Signetics	140	
	SN5495A	† TI		HD7496	Hitachi	ITT7496	ITT							
	SN7495A	TI		ITT5496	† ITT	MC5496	† Motorola							
TD3495	Toshiba	ITT7496	ITT	MC7496	Motorola									
4-Bit Universal Bidirectional Shift Register	SN54194	† AMD	20	8-Bit Parallel-In, Parallel-Out, Unidirectional Shift Register	54199	† Fairchild	90	8-Bit Gated Serial-In, Parallel-Out Shift Register	54164	† AMD	150			
	SN74194	AMD			74199	Fairchild			74164	AMD				
	54194	† Fairchild			HDP4199	Hitachi			54164	† Fairchild				
	74194	Fairchild			DM54199	† National			74164	Fairchild				
	ZN54194	† Ferranti		DM74199	National	74164			Fairchild	140		ZN54164	† Ferranti	
	ZN74194	Ferranti		54199	† Raytheon	HD74164			Hitachi					
	HD74194	Hitachi		74199	Raytheon	ZN74164			Ferranti					
	ITT54194	† ITT		N74199	Signetics	ITT54164			† ITT					
	ITT74194	ITT		SN54199	† Signetics	ITT74164			ITT	150		MC54164	† Motorola	
	DM54194	† National		SN54199	† Signetics	MC74164			Motorola					
	DM74194	National		SN74199	TI	DM7570			† National					
	54194	† Raytheon		4-Bit, Parallel-In, Serial-Out, Shift Register	5494	† Fairchild			DM8570			National		
74194	Raytheon	7494	Fairchild		DM54164	† National								
N74194	Signetics	ZN5494	† Ferranti		DM74164	National	160	54164	† Raytheon					
S54194	† Signetics	ZN7494	Ferranti		74164	Raytheon								
SN54194	† TI	HD2533	Hitachi	N74164	Signetics									
SN74194	TI	ITT5494	† ITT	S54164	† Signetics									
4-Bit, Parallel-In, Serial-Out, Shift Register	5494	† Fairchild	40	8-Bit Parallel-In, Parallel Out, Right/Left Shift Register	54198	† Fairchild	100	8-Bit Serial-In, Serial-Out Shift Register	5491	† Fairchild	170			
	7494	Fairchild			74198	Fairchild			7491	Fairchild				
	ZN5494	† Ferranti			HD74198	Hitachi			ZN5491	† Ferranti				
	ZN7494	Ferranti			DM54198	† National			ZN7491	Ferranti				
	HD2533	Hitachi		DM74198	National	HD2524			Hitachi					
	ITT5494	† ITT		54198	† Raytheon	ITT5491A			† ITT	160		ITT7491A	ITT	
	ITT7494	ITT		74198	Raytheon	ITT7491A			ITT					
	MC5494	† Motorola		N74198	Signetics	MC5491			† Motorola					
	MC7494	Motorola		S54198	† Signetics	MC7491			Motorola					
	N7494	Signetics		SN54198	† TI	DM5491A			† National	170		DM7491A	National	
	S5494	† Signetics		SN54198	† TI	DM7491A			National					
	SW7494	SW		SN74198	TI	N7491			Signetics					
SN5494	† TI	8-Bit Universal Shift Register, Three-State	DM7546	† National	N8276	Signetics								
SN7494	TI		DM8546	National	S5491	† Signetics								
4-Bit Parallel-In, Serial-Out, Shift Register, (with load, shift, hold control)	54178		† Fairchild	50	8-Bit Parallel-In, Serial-Out Shift Register, Complementary Output	54165	† Fairchild	110	10-Bit Parallel-In, Parallel Out Buffer Register, with Reset (clocked flip-flops)	RC8202	Raytheon			
	74178		Fairchild			74165	Fairchild			RM8202	† Raytheon			
	MC7270	Motorola	ZN54165			† Ferranti	N8202			Signetics				
	MC8270	† Motorola	ZN74165			Ferranti	S8202			† Signetics				
	RC8270	Raytheon	DM54165		† National	4-Bit Parallel-In, Serial-Out, Shift Register, with Reset, Complementary Output for last bit (continued)	54179			† Fairchild	50		54179	Fairchild
	RM8270	† Raytheon	DM74165		National		74179			Fairchild				
	S8270	† Signetics	54165		† Raytheon		MC7271			Motorola				
	N8270	Signetics	74165		Raytheon		MC8271			† Motorola				
	SN54178	† TI	N74165		Signetics	RC8271	Raytheon							
	SN74178	TI	DM74165		National	(continued)	(continued)			(continued)	(continued)			

† Military Temperature Range (–55°C to 125°C)

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DIGITAL—TTL (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line
Shift Registers (cont)				Translators (cont)				Miscellaneous (cont)			
10-Bit Parallel-In, Parallel-Out Buffer Register, with Reset, Inverting Output (clocked flip-flops)	RC8203 RM8203 N8203 S8203	Raytheon † Raytheon Signetics † Signetics		Dual 2-Input NAND TTL to MOS Voltage Translator (continued)	SN75180	TI		6-Bit Synchronous Binary Rate Multiplier (continued)	SN7497	TI	
10-Bit Parallel-In, Serial-Out Shift Register	RC8274 RM8274 N8274 S8274	Raytheon † Raytheon Signetics Signetics		Hex TTL to MOS Voltage Translator	DS7812 DS8812 DS78L12 DS88L12 D123A D123B D125A D125B	† National National † National National † Siliconix Siliconix † Siliconix Siliconix	60	Synchronous Decade Rate Multiplier	SN54167 SN74167	† TI TI	110
10-Bit Serial-In, Parallel-Out Shift Register	RC8273 RM8273 N8273 S8273	Raytheon † Raytheon Signetics † Signetics	10	Quad 2-Input NAND TTL to MOS Voltage Translators	DS7810 DS8810 DS7811 DS8811	† National National † National National		4-Bit Priority Register, Cascadable	SN54278 SN74278	† TI TI	
Dual 5-Bit Parallel-In, Parallel Out Buffer Register, (clocked flip-flops)	RC8200 RM8200 N8200 S8200	Raytheon † Raytheon Signetics † Signetics		Quad 2-Input AND TTL to MOS Voltage Translators	DS7819 DS8819	† National National		8-Input Priority Encoder	9318C 9318M 9318M 9318M HD74148 MC8318 MC9318 DM54148 DM74148 N74148 S54148 SN29318 SN39318 SN54148 SN74148	AMD † AMD Fairchild † Fairchild Hitachi Motorola † Motorola † National National Signetics † Signetics TI † TI † TI TI	120
Dual 5-Bit Parallel-In, Parallel-Out, Buffer Register, Inverting Output (clocked flip-flops)	RC8201 RM8201 N8201 S8201	Raytheon † Raytheon Signetics † Signetics	20	Dual ECL to MOS Driver (also ECL to TTL)	MC75358 MC75368 SN75368	Motorola Motorola TI	70	10-Input Priority Encoder	HD74147 DM54147 DM74147 N74147 S54147 SN54147 SN74147	Hitachi † National National Signetics † Signetics † TI TI	130
Dual 8-Bit Serial In, Serial Out, Shift Register	9328C 9328M 9328C 9328M ITT9328-1 ITT9328-5 MC8328 MC9328 RC8277 RM8277 N8277	AMD † AMD Fairchild † Fairchild † ITT ITT Motorola † Motorola Raytheon † Raytheon Signetics	30	For other translators, see Interface-Sense Amplifiers				8-Bit Parity Tree	MC4008 MC4308 MC54408 MC74408	Motorola † Motorola † Motorola Motorola	
Translators				Miscellaneous							
Hex DTL to TTL Inverter	9109C 9109M	Fairchild † Fairchild		Programmable Logic Array (mask programmed)	5775 6775 5776 6776 DM7575 DM7576 DM8575 DM8576	† MMI MMI † MMI MMI † National † National National National	80	Dual 4-Bit Parity Tree	MC4010 MC4310	Motorola † Motorola	140
Hex TTL to DTL Inverter	9112C 9112M	Fairchild † Fairchild		Programmable Logic Arrays, Field Programmable	IM5200 5870 6870 5871 6871 82S100 82S101	Intersil † MMI MMI † MMI MMI Signetics Signetics		9-Bit Parity Generator/Checker	DM7220 DM8220 RC8262 RM8262 N8262 S8262	† National National Raytheon † Raytheon Signetics † Signetics	
Dual MOS to TTL Level Converter	9625C 9625M	Fairchild † Fairchild		8-Bit Successive Approximation Register	AM2502C AM2502M AM2503C AM2503M DM2502 DM2502C DM2503 DM2503C	AMD † AMD AMD † AMD † National National † National National	90	9-Bit Odd/Even Parity Generator/Checker	54180 74180 ZN54180 ZN74180 HD2525 HD74180 ITT54180 ITT74180 MC54180 MC74180 DM54180 DM74180	† Fairchild Fairchild † Ferranti Ferranti Hitachi Hitachi † ITT ITT † Motorola Motorola † National National	150
Dual MOS-to-TTL Level Translator, Three-State	MC54468 MC74468	† Motorola Motorola		12-Bit Successive Approximation Register	AM2504C AM2504M DM2504 DM2504C	AMD † AMD † National National	100	6-Bit Synchronous Binary Rate Multiplier	54180 74180 RC8262 RM8262 N8262 S8262 S54180	† Raytheon Raytheon Raytheon † Raytheon Signetics † Signetics † Signetics	160
7-Unit MOS to TTL Level Converter	SN75270	TI	40	8-Bit Position Scaler (The output is shifted with respect to the input up to 8 positions as determined by a 3-bit selector code.)	RC8243 RM8243 N8243 S8243	Raytheon † Raytheon Signetics † Signetics		(continued)	(continued)		
Dual 2-Input NAND Gate, High Voltage to TTL Interface, to 30v Input	N8T18 S8T18	Signetics † Signetics		6-Bit Synchronous Binary Rate Multiplier	5497 7497 SN5497	† Fairchild Fairchild † TI		(continued)	(continued)		
Dual TTL to MOS Voltage Translator	D130A D130B D139A D139B	† Siliconix Siliconix † Siliconix Siliconix									
Dual 2-Input NAND TTL to MOS Voltage Translator	9624C 9624M DH0034 DH0034C DS7800 DS8800 SN55180	Fairchild † Fairchild † National National † National National † TI	50								

† Military Temperature Range (-55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

DIGITAL—TTL (cont)

Function	Device	Source	Line	Function	Device	Source	Line		
Miscellaneous (cont)				Miscellaneous (cont)					
9-Bit Odd/Even Parity Generator/Checker (continued)	N74180	Signetics		Dual 4-Input NAND Schmitt-Trigger (continued)	7413	TRW			
	SW74180	SW			Quad 2-Input NAND Schmitt Trigger	54132	† Fairchild	60	
	SN54180	† TI		74132		Fairchild			
	SN74180	TI		HD74132		Hitachi			
	74180	TRW		ITT54137		† ITT			
12-Input Odd/Even Parity Checker/Generator	9348C	Fairchild		ITT74137		ITT			
	9348M	† Fairchild		DM54132		† National			
				DM74132		National			
Cyclic Redundancy Checker	9401C	Fairchild		N74132		Signetics			
	9401M	† Fairchild		S54132		† Signetics			
4-Bit Universal Presettable Polynomial Generator	MC8504	Motorola	10	SN54132		† TI			
				SN74132	TI				
Polynomial Generator	MC8506	Motorola		Quad 2-Input NOR Schmitt Trigger	N74232	Signetics			
					S54232	† Signetics			
Single Error Hamming Code Detector and Generator	MC4041	Motorola		Hex Schmitt Trigger, Inverting	5414	† Fairchild	70		
					7414	Fairchild			
BCD-To-Binary/Binary-To-BCD Number Converter	MC4001	Motorola			HD7414	Hitachi			
					ITT54135	† ITT			
BCD-To-Binary Converter	ZN54184	† Ferranti			ITT74135	ITT			
	ZN74184	Ferranti			DM5414	† National			
	DM54184	† National			DM7414	National			
	DM74184	National			N7414	Signetics			
	SN54184	† TI			S5414	† Signetics			
	SN74184	TI			SN5414	† TI			
BCD-to-Binary Converter (Three-State 54/74184)	DM8898	National	20	SN7414	TI	80			
	Binary-To-BCD Converter	DM54185A	† National		Decade Sequencer (sequential 1 of 10 decoder)	9319C	Fairchild		
		DM74185A	National			9319M	† Fairchild		
		SN54185A	† TI			9320C	Fairchild		
SN74185A		TI		9320M		† Fairchild			
Binary-to-BCD Converter	DM8899	National		Bus Transfer Switch (transmit-receive connections to 4 bus terminals)	MC54460	† Motorola			
					MC74460	Motorola			
Dual Pulse Synchronizer/Driver	SN54120	† TI		Quad Power Strobe (V_{cc} strobe or digit driver)	HD6600-2	† Harris	30		
	SN74120	TI			HD6600-5	Harris			
Phase-Frequency Detector	11C44C	Fairchild			HD6605-2	† Harris			
	MC4044	Motorola			HD6605-5	† Harris			
	MC4344	† Motorola							
Contact Bounce Eliminator	DM7544	† National							
	DM8544	National							
Quad Complementary-Output Elements (for symmetrical generation of complementary outputs)	SN54265	† TI							
	SN74265	TI							
Dual Zero Crossing Detector	N8T363	Signetics							
	S8T363	† Signetics	40						
MOS Dynamic Memory Refresh Logic Circuit	MC8505	Motorola							
Dual 4-Input NAND Schmitt-Trigger	5413	† Fairchild	50						
	7413	Fairchild							
	ZN5413	† Ferranti							
	ZN7413	Ferranti							
	HD2545	Hitachi							
	ITT5413	† ITT							
	ITT7413	ITT							
	DM5413	† National							
	DM7413	National							
	N7413	Signetics							
	S5413	† Signetics							
	SW7413	SW							
	SN5413	† TI							
	SN7413	TI							
(continued)									

† Military Temperature Range (–55°C to 125°C)

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DIGITAL—TTL - High Speed

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line
Arithmetic Functions				Flip-Flops (cont)				Flip-Flops (cont)			
Dual Full Adder	54H183	† Fairchild		J-K Master Slave Flip-Flop, AND-OR Input (continued)	S54H71	† Signetics		J-K Negative Edge-Triggered Flip-Flop, AND-OR Input	54H101	† Fairchild	110
	74H183	Fairchild			N74H71	Signetics			74H101	Fairchild	
	SN54H183	† TI			SN54H71	† TI			S54H101	† Signetics	
	SN74H183	TI			SN74H71	TI			N74H101	Signetics	
Arithmetic Logic Unit/Function Generator	54R181	† Raytheon		J-K Master-Slave Flip-Flop, AND Input with Preset and Clear	54H72	† Fairchild		Dual J-K Negative Edge- Triggered Flip-Flop, with Clear	54H103	† Fairchild	
	74R181	Raytheon			74H72	Fairchild			74H103	Fairchild	
Look ahead Carry Generator	54R182	† Raytheon			ITT54H72	† ITT			DM54H103	† National	
	74R182	Raytheon			ITT74H72	ITT	60		DM74H103	National	120
Buffers/Inverters				Dual J-K Master-Slave Flip-Flop with clear				Dual J-K Negative Edge- Triggered Flip-Flop, with Preset and Clear			
Hex Inverter	54H04	† Fairchild	10		54H73	† Fairchild			54H106	† Fairchild	
	74H04	Fairchild			74H73	Fairchild			74H106	Fairchild	
	HD2563	Hitachi			ITT54H73	† ITT			DM54H106	† National	
	ITT54H04	† ITT			ITT74H73	ITT			DM74H106	National	
	ITT74H04	ITT			MC3061	Motorola			54R112	† Raytheon	
	MC3008	Motorola			MC3062	Motorola			74R112	Raytheon	
	MC3108	† Motorola			MC3063	Motorola			54R112	Raytheon	
	DM54H04	† National			MC3161	† Motorola	80		S54H106	† Signetics	130
	DM74H04	National			MC3162	† Motorola			N74H106	Signetics	
	54H04	† Raytheon			MC3163	† Motorola			SN54H106	† TI	
	54R04	† Raytheon			DM54H73	† National			SN74H106	TI	
	74H04	Raytheon	20		DM74H73	National			Dual J-K Negative Edge- Triggered Flip-Flop, Pre-set, Common Clear, Common Clock		
	74R04	Raytheon			S54H73	† Signetics			54H108	† Fairchild	
	S54H04	† Signetics			N74H73	Signetics			74H108	Fairchild	
	N74H04	Signetics			SN54H73	† TI			DM54H108	† National	
	SN54H04	† TI			SN74H73	TI			DM74H108	National	
	SN74H04	TI			Dual J-K Master-Slave Flip-Flop with Preset and Clear				54R114	† Raytheon	
Hex Inverter, Open Collector	54H05	† Fairchild			54H76	† Fairchild			74R114	Raytheon	
	74H05	Fairchild			74H76	Fairchild			S54H108	† Signetics	140
	ITT54H05	† ITT			ITT54H76	† ITT			N74H108	Signetics	
	ITT74H05	ITT			ITT74H76	ITT			SN54H108	† TI	
	MC3009	Motorola			DM54H76	† National			SN74H108	TI	
	MC3109	† Motorola			DM74H76	National			Dual J-K Negative Edge-Triggered Flip-Flop, Separate Preset and Clock, (no Clear)		
	DM54H05	† National			N74H76	Signetics			54R113	† Raytheon	
	DM74H05	National			S54H76	† Signetics			74R113	Raytheon	
	54H05	† Raytheon			SN54H76	† TI			AND Input JJ-KK Flip-Flop		
	54R05	† Raytheon			SN74H76	TI			MC3052	Motorola	
	74H05	Raytheon			Dual J-K Master-Slave Flip-Flop, Preset, Common Clear, Common Clock				MC3152	† Motorola	
	74R05	Raytheon			54H78	† Fairchild			D Type Double Edge-Triggered Master-Slave Flip-Flop		
	S54H05	† Signetics			74H78	Fairchild			MC3053	Motorola	
	N74H05	Signetics			DM54H78	† National			MC3153	† Motorola	
	SN54H05	† TI			DM74H78	National			Dual D Flip-Flop		
	SN74H05	TI	40		SN54H78	† TI			54H74	† Fairchild	150
Drivers					SN74H78	TI			74H74	Fairchild	
Dual 3-Input 3-Output AND Series Terminated Line Driver	MC3028	Motorola			DM74H78	National			ITT54H74	† ITT	
	MC3128	† Motorola			SN54H78	† TI			ITT74H74	ITT	
Dual 3-Input 3-Output NAND Series Terminated Line Driver	MC3029	Motorola			SN74H78	TI			MC3060	Motorola	
	MC3129	† Motorola			Dual J-K Master-Slave Flip-Flop, Preset, Common Clear, Common Clock				MC3160	† Motorola	
Flip-Flops					54H78	† Fairchild			MC54H74	† Motorola	
J-K Master Slave Flip-Flop, AND-OR Input	54H71	† Fairchild			74H78	Fairchild			MC74H74	Motorola	
	74H71	Fairchild			DM54H78	† National	100		DM74H74	† National	
	MC3054	Motorola			SN54H78	† TI			DM74H74	National	
	MC3154	† Motorola			J-K Negative Edge-Triggered Flip-Flop, AND Input				54H74	† Raytheon	160
	DM54H71	† National			54H102	† Fairchild			54R74	† Raytheon	
	DM74H71	National	50		74H102	Fairchild			74H74	Raytheon	
(continued)					S54H102	† Signetics			74R74	Raytheon	
					N74H102	Signetics			S54H74	† Signetics	
					SN54H102	† TI			N74H74	Signetics	
					SN74H102	TI			SN54H74	† TI	
									SN74H74	TI	

† Military Temperature Range (-55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

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DIGITAL—TTL - High Speed (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line		
Gates, AND/NAND				Gates, AND/NAND (cont)				Gates, AND/NAND (cont)					
Dual 4-Input AND Gate	54H21	† Fairchild	10	8-Input NAND Gate (continued)	S54H30	† Signetics	60	Triple 3-Input NAND Gate (continued)	DM74H10	National	120		
	74H21	Fairchild				N74H30		Signetics		54H10		† Raytheon	
	ITT54H21	† ITT				SN54H30		† TI		54R10		† Raytheon	
	ITT74H21	ITT				SN74H30		TI		74H10		Raytheon	
	MC3011	Motorola			Dual 4-Input NAND Gate	54H20	† Fairchild	70		74R10		Raytheon	
	MC3111	† Motorola				74H20	Fairchild			S54H10		† Signetics	
	DM54H21	† National				ITT54H20	† ITT			N74H10		Signetics	
	DM74H21	National				ITT74H20	ITT			SN54H10		† TI	
	S54H21	† Signetics				MC3010	Motorola			SN74H10		TI	
	N74H21	Signetics				MC3110	† Motorola			Triple 3-Input NAND Gate, Open Collector			
	SN74H21	† TI			DM54H20	† National			MC3007	Motorola			
	SN74H21	TI			DM74H20	National			MC3107	† Motorola			
Dual 4-Input AND Power Gate	MC3026	Motorola			54H20	† Raytheon	80		Quad 2-Input NAND Gate	54H00	† Fairchild	130	
	MC3126	† Motorola			54R20	† Raytheon				74H00	Fairchild		
Triple 3-Input AND Gate	54H11	† Fairchild	20		74H20	Raytheon			ITT54H00	† ITT			
	74H11	Fairchild				74R20		Raytheon		ITT74H00	ITT		
	ITT54H11	† ITT				S54H20		† Signetics		MC3000	Motorola		
	ITT74H11	ITT				N74H20		Signetics		MC3100	† Motorola		
	MC3006	Motorola				SN54H20		† TI		DM54H00	† National		
	MC3106	† Motorola				SN74H20		TI		DM74H00	National		
	DM54H11	† National			Dual 4-Input NAND Gate, Open Collector	54H22		† Fairchild	90		54R00		† Raytheon
	DM74H11	National				74H22		Fairchild			54R00		† Raytheon
	54H11	† Raytheon				MC3012	Motorola			74H00	Raytheon		
	54R11	† Raytheon				MC3112	† Motorola			74R00	Raytheon		
	74H11	Raytheon			DM54H22	† National		S54H00		† Signetics			
	74R11	Raytheon			DM74H22	National		N74H00		Signetics			
	S54H11	† Signetics			54H22	† Raytheon		SN54H00		† TI			
	N74H11	Signetics			54R22	† Raytheon		SN74H00		TI			
	SN54H11	† TI			74H22	Raytheon	100	Quad 2-Input NAND Gate, Open Collector		54H01	† Fairchild	140	
	SN74H11	TI			74R22	Raytheon				54H01	† Fairchild		
Triple 3-Input AND Gate Open Collector	54H15	† Fairchild	30		S54H22	† Signetics			ITT54H01	† ITT			
	74H15	Fairchild				N74H22		Signetics		ITT74H01	ITT		
	54H15	† Raytheon				SN54H22		† TI		MC3004	Motorola		
	54R15	† Raytheon				SN74H22		TI		MC3104	† Motorola		
	74H15	Raytheon			Dual 4-Input NAND Buffer	54H40		† Fairchild	110		DM54H01		† National
	74R15	Raytheon				74H40		Fairchild			DM74H01		National
	SN54H15	† TI				ITT54H40		† ITT			54H01		† Raytheon
	SN74H15	TI				ITT74H40		ITT			74H01		Raytheon
Quad 2-Input AND Gate	54H08	† Fairchild		40		MC3024	Motorola	100		54R03	† Raytheon		
	74H08	Fairchild					MC3025			Motorola		74R03	Raytheon
	MC3001	Motorola				MC3124	† Motorola				S54H01	† Signetics	
	MC3101	† Motorola				MC3125	† Motorola				N74H01	Signetics	
	DM54H08	† National				DM54H40	† National				SN54H01	† TI	
	DM74H08	National				DM74H40	National				SN74H01	TI	
	S54H08	† Signetics				54H40	† Raytheon			Gates, AND-OR/AND-OR-Invert			
	N74H08	Signetics				54R40	† Raytheon			2-2-2-3-Input AND-OR Gate, Expandable			
Quad 2-Input AND Gate (Open Collector)	54H09	† Fairchild	50			74H40	Raytheon		110	54H52	† Fairchild		
	74H09	Fairchild					74R40			Raytheon		74H52	Fairchild
8-Input NAND Gate	54H30	† Fairchild				74R40	Raytheon			MC3031	Motorola		
	74H30	Fairchild				S54H40	† Signetics			MC3131	† Motorola		
	ITT54H30	† ITT				N74H40	Signetics			DM54H52	† National		
	ITT74H30	ITT				SN54H40	† TI			DM74H52	National		
	MC3015	Motorola				SN74H40	TI			S54H52	† Signetics		
	MC3016	Motorola			Triple 3-Input NAND Gate	54H10	† Fairchild	120		N74H52	Signetics		
	MC3115	† Motorola				74H10	Fairchild				SN54H52	† TI	
	MC3116	† Motorola				ITT54H10	† ITT				SN74H52	TI	
	DM54H30	† National			ITT74H10	ITT			2-2-2-3-Input AND-OR-Invert Gate				
	DM74H30	National			MC3005	Motorola			54H54	† Fairchild			
(continued)					MC3015	† Motorola			74H54	Fairchild			
					DM54H10	† National			ITT54H54	† ITT			
					(continued)				ITT74H54	ITT			
									(continued)				

† Military Temperature Range (−55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

DIGITAL—TTL - High Speed (cont)

Function	Device	Source	Line	Function	Device	Source	Line
Gates, AND-OR/AND-OR-Invert (cont)				Gates, Exclusive, OR/NOR			
2-2-2-3-Input AND-OR-Invert Gate (continued)	MC3033	Motorola		Quad 2-Input Exclusive OR Gate	MC3021	Motorola	60
	MC3133	† Motorola			MC3121	† Motorola	
	DM54H54	† National		Quad 2-Input Exclusive NOR Gate	MC3022	Motorola	
	DM74H54	National			MC3122	† Motorola	
	S54H54	† Signetics		Gates, OR/NOR			
	N74H54	Signetics		Quad 2-Input OR Gate	MC3003	Motorola	
	SN54H54	† TI			MC3103	† Motorola	
SN74H54	TI	Quad 2-Input NOR Gate	MC3002	Motorola			
2-2-2-3-Input AND-OR-Invert Gate, Expandable			MC3102	† Motorola			
54H53	† Fairchild		54R02	† Raytheon			
74H53	Fairchild		74R02	Raytheon			
ITT54H53	† ITT	Miscellaneous					
ITT74H53	ITT	4-Bit True/Complement Zero/One Element					
MC3032	Motorola	54H87	† Fairchild	70			
MC3132	† Motorola	74H87	Fairchild				
DM54H53	† National	SN54H87	† TI				
DM74H53	National	SN74H87	TI				
S54H53	† Signetics	Dual 4-Input Expander (for H50, H53, H55)					
N74H53	Signetics	54H60	† Fairchild	80			
SN54H53	† TI	74H60	Fairchild				
SN74H53	TI	ITT54H60	† ITT				
2-2-3-4-Input AND-OR-Invert Gate		ITT74H60	ITT				
54R64	† Raytheon	MC3030	Motorola				
74R64	Raytheon	MC3130	† Motorola				
2-2-3-4-Input AND-OR-Invert Gate, Open Collector		DM54H60	† National				
54R65	† Raytheon	DM74H60	National				
74R65	Raytheon	S54H60	† Signetics				
2-Wide 4-Input AND-OR-Invert Gate, Expandable		N74H60	Signetics				
54H55	† Fairchild	SN54H60	† TI				
74H55	Fairchild	SN74H60	TI				
MC3034	Motorola	Triple 3-Input Expander (for H52)					
MC3134	† Motorola	54H61	† Fairchild	90			
DM54H55	† National	74H61	Fairchild				
DM74H55	National	MC3019	Motorola				
S54H55	† Signetics	MC3119	† Motorola				
N74H55	Signetics	DM54H61	National				
SN54H55	† TI	S54H61	† Signetics				
SN74H55	TI	N74H61	Signetics				
Dual 2-Wide 2-Input AND-OR-Invert Gate		SN54H61	† TI				
54H51	† Fairchild	SN74H61	TI				
74H51	Fairchild	3-2-2-3-Input AND-OR Expander (for H50, H53, H55)					
ITT54H51	† ITT	54H62	† Fairchild	100			
ITT74H51	ITT	74H62	Fairchild				
MC3023	Motorola	MC3018	Motorola				
MC3123	† Motorola	MC3118	† Motorola				
DM54H51	† National	DM54H62	† National				
DM74H51	National	DM74H62	National				
S54H51	† Signetics	S54H62	† Signetics				
N74H51	Signetics	N74H62	Signetics				
SN54H51	† TI	SN54H62	† TI				
SN74H51	TI	SN74H62	TI				
Dual 2-Wide 2-Input AND-OR-Invert Gate, Expandable							
54H50	† Fairchild						
74H50	Fairchild						
ITT54H50	† ITT						
ITT74H50	ITT						
MC3020	Motorola						
MC3120	† Motorola						
DM54H50	† National						
DM74H50	National						
S54H50	† Signetics						
N74H50	Signetics						
SN54H50	† TI						
SN74H50	TI						

† Military Temperature Range (-55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

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DIGITAL—TTL - Low Power Schottky

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line	
Arithmetic Functions				Arithmetic Functions (cont)				Buffers/Inverters (cont)				
4-Bit Binary Full Adder, Look-ahead Carry	9LS83C	Fairchild		8-Bit-by-1-Bit Serial/Parallel Multiplier	AM25LS14C	AMD		Hex Inverter, Three-State (continued)	SN54LS368	† TI		
	9LS83M	† Fairchild			AM25LS14M	† AMD			SN74LS368	TI		
	9LS283C	Fairchild		4-Bit Magnitude Comparator	N74LS85	Signetics	50	Counters, Binary				
	9LS283M	† Fairchild			see page 384			4-Bit Binary Counter	9LS93C	Fairchild	100	
	54LS83	† Fairchild			S74LS85	†			9LS93M	† Fairchild		
	74LS83	Fairchild			SN54LS85	† TI			54LS93	† Fairchild		
	54LS283	† Fairchild			SN74LS85	TI			74LS93	Fairchild		
	74LS283	Fairchild		Buffers/Inverters						54LS293	† Fairchild	
	54LS83A	† Raytheon		Quad Buffer, Three-State	54LS125	† Fairchild			74LS293	Fairchild		
	see page 282				74LS125	Fairchild			74LS293	Fairchild		
	54LS283	† Raytheon	10		54LS126	† Fairchild			N74LS93	Signetics		
	see page 282				74LS126	Fairchild			see page 384			
	N74LS83	Signetics			74LS126	Fairchild			S54LS93	† Signetics		
	S54LS83	† Signetics			SN54LS125	† TI			see page 384			
	N74LS283	Signetics			SN54LS126	† TI			N54LS293	Signetics		
	see page 384				SN74LS125	TI	60		S74LS293	† Signetics	110	
	S54LS283	† Signetics			SN74LS126	TI			SN54LS93	† TI		
	see page 384								SN54LS293	† TI		
	SN54LS83A	† TI		Hex Buffer, Three-State	54LS365	† Fairchild			SN74LS93	TI		
	SN74LS83A	TI			74LS365	Fairchild			SN74LS293	TI		
	SN54LS283	† TI			74LS367	† Fairchild						
	SN74LS283	TI			74LS367	Fairchild						
4-Bit ALU and 16-Word two-port Stack	AM2901C	AMD			SN54LS365	† TI		4-Bit Binary Counter, Synchronous	AM25LS163C	AMD		
	AM2901M	† AMD	20		SN74LS365	TI			AM25LS163M	AMD	†	
Arithmetic Logic Unit	AM25LS381C	AMD			SN54LS367	† TI			SN54LS163	† AMD		
	AM25LS381M	AMD	†		SN74LS367	Fairchild			SN74LS163	AMD		
	SN54LS381	† AMD			SN54LS367	† TI			9LS163C	Fairchild		
	SN74LS381	AMD			SN74LS367	TI			9LS163M	† Fairchild		
Arithmetic Logic Unit/Function Generator	AM25LS181C	AMD		Hex Inverter	9LS04C	Fairchild	70		54LS163	† Fairchild	120	
	AM25LS181M	AMD	†		9LS04M	† Fairchild			74LS163	Fairchild		
	SN54LS181	† AMD			54LS04	† Fairchild			54LS163	† Raytheon		
	SN74LS181	AMD			74LS04	Fairchild			see page 282			
	9LS181C	Fairchild			DM54LS04	† National			N74LS163	Signetics		
	9LS181M	† Fairchild	30		DM74LS04	National			see page 384			
	54LS181	† Fairchild			54LS04	† Raytheon			S54LS163	† Signetics		
	74LS181	Fairchild			see page 282				see page 384			
	54LS181	† Raytheon			N74LS04	Signetics			SN54LS163	† TI		
	see page 282				see page 384				SN74LS163	TI		
	N74LS181	Signetics			S54LS04	† Signetics						
	see page 384				see page 384							
	S54LS181	† Signetics			SN54LS04	† TI	80	4-Bit Binary Counter, Synchronous, Direct Clear	AM25LS161C	AMD		
	SN54LS181	† TI			SN74LS04	TI			AM25LS161M	AMD	†	
	SN74LS181	TI							SN54LS161	† AMD		
Register/Arithmetic Logic Unit	AM25LS281C	AMD		Hex Inverter, Open Collector	9LS05C	Fairchild			SN74LS161	AMD	130	
	AM25LS281M	AMD	†		9LS05M	† Fairchild			9LS161C	Fairchild		
	SN54LS281	† AMD			54LS05	† Fairchild			9LS161M	† Fairchild		
	SN74LS281	AMD	40		74LS05	Fairchild			54LS161	† Fairchild		
Quad Serial Adder/Subtractor	AM25LS15C	AMD			74LS05	Fairchild			74LS161	Fairchild		
	AM25LS15M	† AMD			DM54LS05	† National			54LS161	† Raytheon		
2-Bit-by-4 Bit Parallel Binary Multiplier, Serial Output	N74LS261	Signetics			DM74LS05	National			see page 282			
	see page 384				54LS05	† Raytheon			N74LS161	Signetics		
	S54LS261	† Signetics			see page 282				see page 384			
	see page 384				N74LS05	Signetics			S54LS161	† Signetics		
	SN54LS261	† TI			see page 384				see page 384			
	SN74LS261	TI			S54LS05	† Signetics			SN54LS161	† TI		
					see page 384				SN74LS161	TI		
					SN54LS05	† TI	90	Binary (Divide-by-2 and Divide-by-8) Counter/Latch, Preset Input	9LS197C	Fairchild	140	
					SN74LS05	TI			9LS197M	† Fairchild		
									54LS197	† Fairchild		
									74LS197	Fairchild		
									54LS197	† Raytheon		
									see page 282			
									S54LS197	† Signetics		
									see page 384			
									(continued)			

† Military Temperature Range (—55°C to 125°C)

DIGITAL—TTL - Low Power Schottky (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line
Counters, Binary (cont)				Counters, Decade (cont)				Counters, Decade (cont)			
Binary (Divide-by-2 and Divide-by-8) Counter/ Latch, Preset Input (continued)	N74LS197 see page 384	Signetics		Decade Counter, Synchronous, Direct Clear	AM25LS162C AM25LS162M SN54LS162 SN74LS162 9LS162C 9LS162M 54LS162 74LS162 54LS162 N74LS162 S54LS162 N74LS162 SN54LS162 SN74LS162	AMD AMD † AMD AMD Fairchild † Fairchild † Fairchild Fairchild † Raytheon Signetics see page 384 † Signetics see page 384 † TI TI	50	Decade Up/Down Counter, Synchronous, Preset Input Mode Control (continued)	54LS190 see page 282 N74LS190 see page 384 S54LS190 see page 384 SN54LS190 SN74LS190	† Raytheon Signetics † Signetics see page 384 † TI TI	
Binary Up/Down Counter, Synchronous, Preset Input	AM25LS193C AM25LS193M SN54LS193 SN74LS193 9LS193C 9LS193M 54LS193 74LS193 54LS193 N74LS193 S54LS193 SN54LS193 SN74LS193	AMD AMD † AMD AMD Fairchild † Fairchild † Fairchild Fairchild † Raytheon Signetics see page 384 Signetics see page 384 † TI TI	10	Decade Counter (Divide-by-2 and by 5)	9LS90C 9LS90M 54LS90 74LS90 54LS290 74LS290 N74LS90 S54LS90 N74LS290 S54LS290 SN54LS90 SN74LS90 SN54LS290 SN74LS290	Fairchild † Fairchild † Fairchild Fairchild † Fairchild Fairchild Signetics see page 384 † Signetics see page 384 † TI TI † TI TI	60	Decade Up/Down Counter, Counter, Synchronous, Preset Input, Mode Control, Look-ahead Carry	SN54LS168 SN74LS168	† TI TI	100
Binary Up/Down Counter, Synchronous, Preset Input, Mode Control	AM25LS191C AM25LS191M SN54LS191 SN74LS191 9LS191C 9LS191M 54LS191 74LS191 54LS191 N74LS191 S54LS191 SN54LS191 SN74LS191	AMD AMD † AMD AMD Fairchild † Fairchild † Fairchild Fairchild † Raytheon Signetics see page 384 † Signetics see page 384 † TI TI	20	Decade Up/Down Counter, Synchronous, Preset Input	AM25LS192C AM25LS192M SN54LS192 SN74LS192 9LS192C 9LS192M 54LS192 74LS192 54LS192 S54LS192 N74LS192 S74LS192 SN54LS192 SN74LS192	AMD AMD † AMD AMD Fairchild † Fairchild † Fairchild Fairchild † Raytheon see page 282 † Signetics see page 384 Signetics see page 384 † Signetics † TI TI	70	Decade (Divide-by-2 and Divide-by-5) Counter/ Latch, Preset Input	9LS196C 9LS196M 54LS196 74LS196 54LS196 N74LS196 S54LS196 SN54LS196 SN74LS196	Fairchild † Fairchild † Fairchild Fairchild † Raytheon see page 282 † Signetics see page 384 † TI TI	
Binary Up/Down Counter, Synchronous, Preset Input, Mode Control Look-ahead Carry	SN54LS169 SN74LS169	† TI TI	30	Counters, Miscellaneous							
Counters, Decade				Divide-by-Twelve Counter (Divide-by-2 and by 6)							
Decade Counter, Synchronous	AM25LS160C AM25LS160M SN54LS160 SN74LS160 9LS160C 9LS160M 54LS160 74LS160 54LS160 N74LS160 S54LS160 SN54LS160 SN74LS160	AMD AMD † AMD AMD Fairchild † Fairchild † Fairchild Fairchild † Raytheon see page 282 Signetics see page 384 † Signetics see page 384 † TI TI	40	54LS92 74LS92 N74LS92 S54LS92 SN54LS92 SN74LS92	† Fairchild Fairchild Signetics see page 384 † Signetics see page 384 † TI TI	110	Decoders/Drivers				
Decade Up/Down Counter, Synchronous, Preset Input Mode Control				BCD to 7-Segment Decoder/ Driver							
AM25LS190C AM25LS190M SN54LS190 SN74LS190 9LS190C 9LS190M 54LS190 74LS190 (continued)	AMD AMD † AMD AMD Fairchild † Fairchild † Fairchild Fairchild		90	SN54LS47 SN54LS48 SN54LS49 SN54LS247 SN54LS248 SN54LS249 SN74LS47 SN74LS48 SN74LS49 SN74LS247 SN74LS248 SN74LS249	† TI † TI † TI † TI † TI † TI TI TI TI TI TI TI	120	3-Line to 8-Line Decoder/Demultiplexer				
Decade Up/Down Counter, Synchronous, Preset Input Mode Control				AM25LS138C AM25LS138M SN54LS138 SN74LS138 9LS138C 9LS138M 54LS138 74LS138 54LS138 N74LS138 S74LS138 SN54LS138 SN74LS138 (continued)							
AM25LS190C AM25LS190M SN54LS190 SN74LS190 9LS190C 9LS190M 54LS190 74LS190 (continued)	AMD AMD † AMD AMD Fairchild † Fairchild † Fairchild Fairchild		90	AM25LS138C AM25LS138M SN54LS138 SN74LS138 9LS138C 9LS138M 54LS138 74LS138 54LS138 N74LS138 S74LS138 SN54LS138 SN74LS138 (continued)	AMD AMD † AMD AMD Fairchild † Fairchild † Fairchild Fairchild † Raytheon see page 282 Signetics see page 384 † Signetics see page 384 (continued)	130					

† Military Temperature Range (-55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

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Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line
Decoders/Drivers (cont)				Decoders/Drivers (cont)				Flip-Flops (cont)			
3-Line to 8-Line Decoder/Demultiplexer (continued)	S54LS138	† Signetics see page 384		Dual 2-Line to 4-Line Decoder/Demultiplexer, Common Address, (or 3-Line to 8-Line (continued))	SN54LS156	† TI		Dual "J-K" Negative Edge-Triggered Flip-Flop with Clear (continued)	S54LS73	† Signetics see page 384	
	SN54LS138	† TI			SN74LS156	TI			SN54LS73	† TI	90
	SN74LS138	TI							SN74LS73	TI	
3-Line to 8-Line Decoder/ Demultiplexer, Three-State	54LS255	† Raytheon see page 282		Flip-Flops							
	N74LS255	Signetics		Dual "J-K" Flip-Flop with Clear	DM54LS107	† National		Dual "J-K" Negative Edge-Triggered Flip-Flop with Preset	9LS113C	Fairchild	
	S54LS255	† Signetics			DM74LS107	National			9LS113M	† Fairchild	
BCD to 10-Line Decoder (one-of-ten)	9LS42C	Fairchild			54LS107	† Raytheon see page 282	50		54LS113	† Fairchild	
	9LS42M	† Fairchild			N74LS107	Signetics see page 384			74LS113	Fairchild	
	54LS42	† Fairchild			S54LS107	† Signetics see page 384			DM54LS113	† National	
	74LS42	Fairchild	10		SN54LS107	† TI			DM74LS113	National	
	N74LS42	Signetics see page 384			SN74LS107	TI			54LS113	† Raytheon see page 282	
	S54LS42	† Signetics see page 384							N74LS113	Signetics see page 384	
	SN54LS42	† TI		Dual "J-K" Flip-Flop with Preset and Clear	DM54LS76	† National			S54LS113	† Signetics see page 384	100
	SN74LS42	TI			DM74LS76	National			SN54LS113	† TI	
BCD-to-Decimal Decoder/Driver, Open Collector to 15 v	N74LS145	Signetics see page 384			54LS76	† Raytheon see page 282			SN74LS113	TI	
	S54LS145	† Signetics see page 384			N74LS76	Signetics see page 384					
	SN54LS145	† TI			S54LS76	† Signetics see page 384	60				
	SN74LS145	TI			SN54LS76	† TI					
					SN74LS76	TI					
Dual 2-Line to 4-Line Decoder/Demultiplexer	AM25LS139C	AMD		Dual "J-K" Flip-Flop with Preset, Common Clock and Common Clear	DM54LS78	† National			9LS112C	Fairchild	
	AM25LS139M	AMD	†		DM74LS78	National			9LS112M	† Fairchild	
	SN54LS139	† AMD			54LS78	Raytheon see page 282			54LS112	† Fairchild	
	SN74LS139	AMD			N74LS78	Signetics see page 384			74LS112	Fairchild	
	9LS139C	Fairchild			S54LS78	† Signetics see page 384			DM54LS112	† National	
	9LS139M	† Fairchild			SN54LS78	† TI			DM74LS112	National	
	54LS139	† Fairchild			SN74LS78	TI			54LS112	† Raytheon see page 282	
	74LS139	Fairchild							N74LS112	Signetics see page 384	110
	54LS139	† Raytheon see page 282							S54LS112	Signetics see page 384	
	N74LS139	Signetics see page 384		Dual "J-K" Flip-Flop with Preset and Clear	9LS109C	Fairchild			SN54LS112	† TI	
	S54LS139	† Signetics see page 384			9LS109M	† Fairchild	70		SN74LS112	TI	
	SN54LS139	† TI			54LS109	† Fairchild					
	SN74LS139	TI	30		74LS109	Fairchild					
Dual 2-Line to 4-Line Decoder/Demultiplexer, Common Address (or 3-Line to 8-Line Decoder/Demultiplexer)	9LS155C	Fairchild			DM54LS109	† National					
	9LS155M	† Fairchild			DM74LS109	National					
	54LS155	† Fairchild			54LS109	† Raytheon see page 282					
	74LS155	Fairchild			S54LS109	† Signetics see page 384					
	54LS155	† Raytheon see page 282			N74LS109	Signetics see page 384					
	N74LS155	Signetics see page 384			SN54LS109	† TI					
	S54LS155	† Signetics see page 384			SN74LS109	TI					
	SN54LS155	† TI									
	SN74LS155	TI	40								
Dual 2-Line to 4-Line Decoder/Demultiplexer, Common Address, (or 3-Line to 8-Line Decoder/Demultiplexer) Open Collector	9LS156C	Fairchild		Dual "J-K" Negative Edge-Triggered Flip-Flop with Clear	9LS73C	Fairchild					
	9LS156M	† Fairchild			9LS73M	† Fairchild	80		9LS74C	Fairchild	
	54LS156	† Fairchild			54LS73	† Fairchild			9LS74M	† Raytheon	
	74LS156	Fairchild			74LS73	Fairchild			54LS74	† Fairchild	
	54LS156	† Raytheon see page 282			74LS73	Fairchild			74LS74	Fairchild	
	(continued)				DM54LS73	† National			DM54LS74	† National	
					DM74LS73	National			DM74LS74	National	
					54LS73	† Raytheon see page 282			54LS74	† Raytheon see page 282	130
					N74LS73	Signetics see page 384			N74LS74	Signetics see page 384	
					N74LS73	Signetics see page 384			S54LS74	† Signetics see page 384	
					(continued)				(continued)		

† Military Temperature Range (-55°C to 125°C)

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Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line
Flip-Flops (cont)				Flip-Flops (cont)				Gates, AND/NAND (cont)			
Dual D-Type Positive Edge-Triggered Flip-Flop with Preset and Clear (continued)	SN54LS74	† TI		Hex D-Type Flip-Flop with Common Enable (continued)	SN54LS378	† TI		Quad 2-Input AND Gate, Open Collector (continued)	74LS09	Fairchild	100
	SN74LS74	TI			SN74LS378	TI			54LS09	† Raytheon	
										see page 282	
Quad D-Type Flip-Flop with Clear	AM25LS175C	AMD		Octal D-Type Flip-Flop with Clear	SN54LS273	† TI			N74LS09	Sigmetics	
	AM25LS175M	AMD	†		SN74LS273	TI				see page 384	
	SN54LS175	† AMD							S54LS09	† Sigmetics	
	SN74LS175	AMD		Octal D-Type Flip-Flop with Enable	SN54LS377	† TI	60			see page 384	
	9LS175C	Fairchild			SN74LS377	TI			SN54LS09	† TI	
	9LS175M	† Fairchild		Gates, AND/NAND					SN74LS09	† TI	
	54LS175	† Fairchild		Dual 4-Input AND Gate				8-Input NAND Gate	9LS30C	Fairchild	
	74LS175	Fairchild	10		9LS21C	Fairchild			9LS30M	† Fairchild	
	DM54LS175	† National			9LS21M	† Fairchild			54LS30	† Fairchild	
	DM74LS175	National			54LS21	† Fairchild			74LS30	Fairchild	
	54LS175	† Raytheon			74LS21	Fairchild			DM54LS30	† National	110
	N74LS175	Sigmetics			54LS21	† Raytheon			DM74LS30	National	
	see page 282				S54LS21	† Sigmetics			54LS30	† Raytheon	
	S54LS175	† Sigmetics			see page 384				see page 282		
	see page 384				N74LS21	Sigmetics			N74LS30	Sigmetics	
	SN54LS175	† TI			see page 384				see page 384		
	SN74LS175	TI			SN74LS21	TI			S54LS30	† Sigmetics	
					SN54LS21	† TI			see page 384		
Quad D-Type Flip-Flop with Common Clock Enable	AM25LS08C	AMD		Triple 3-Input AND Gate	9LS11C	Fairchild	70		SN54LS30	† TI	
	AM25LS08M	† AMD			9LS11M	† Fairchild			SN74LS30	TI	
	SN54LS379	† AMD	20		54LS11	† Fairchild					
	SN74LS379	AMD			74LS11	Fairchild			13-Input NAND Gate	54LS133	† Fairchild
	54LS298	† Fairchild			54LS11	† Raytheon				74LS133	Fairchild
	74LS298	Fairchild			see page 282						
Quad D-Type Flip-Flop with Multiplexed Dual Inputs	AM25LS209C	AMD			N74LS11	Sigmetics			Dual 4-Input NAND Gate	9LS20C	Fairchild
	AM25LS209M	AMD	†		see page 384					9LS20M	† Fairchild
	SN54LS399	† AMD			S54LS11	† Sigmetics				54LS20	† Fairchild
	SM74LS399	AMD			see page 384					74LS20	Fairchild
	9LS298C	AMD			SN54LS11	TI				DM54LS20	† National
	9LS298M	† AMD			SN74LS11	† TI				DM74LS20	National
	9LS298C	Fairchild	30							54LS20	† Raytheon
	9LS298M	† Fairchild			Triple 3-Input AND Gate, Open Collector	9LS15C	Fairchild			see page 282	
	SN54LS298	† TI				9LS15M	† Fairchild	80		N74LS20	Sigmetics
	SN74LS298	TI				54LS15	† Fairchild			see page 384	
	SN54LS399	† TI				74LS15	Fairchild			S54LS20	† Sigmetics
	SN74LS399	TI				54LS15	† Raytheon			see page 384	
						see page 282				SN54LS20	† TI
Hex D-Type Flip-Flop with Clear	AM25LS174C	AMD			N74LS15	Sigmetics				SN74LS20	TI
	AM25LS174M	AMD	†		see page 384				Dual 4-Input NAND Buffer	9LS40C	Fairchild
	SN54LS174	† AMD			S54LS15	† Sigmetics				9LS40M	† Fairchild
	SN74LS174	AMD			see page 384					54LS40	† Fairchild
	9LS174C	Fairchild	40		SN54LS15	† TI				74LS40	Fairchild
	9LS174M	† Fairchild			SN74LS15	TI				54LS40	† Raytheon
	54LS174	† Fairchild								see page 282	
	74LS174	Fairchild			Quad 2-Input AND Gate	9LS08C	Fairchild			N74LS40	Sigmetics
	DM54LS174	† National				9LS08M	† Fairchild			see page 384	
	DM74LS174	National				54LS08	† Fairchild	90		S54LS40	Sigmetics
	54LS174	† Raytheon				74LS08	Fairchild			see page 384	
	see page 282					54LS08	† Raytheon			SN54LS40	† TI
	N74LS174	Sigmetics				see page 282				SN74LS40	TI
	see page 384					N74LS08	Sigmetics				
	S54LS174	† Sigmetics				see page 384				Dual 4-Input NAND Gate, Open Collector	9LS22C
	see page 384					S54LS08	† Sigmetics				9LS22M
	SN54LS174	† TI				see page 384					54LS22
	SN74LS174	TI	50			SN54LS08	† TI				† Fairchild
						SN74LS08	TI				74LS22
											Fairchild
Hex D-Type Flip-Flop with Common Enable	AM25LS07C	AMD				Quad 2-Input AND Gate, Open Collector	9LS09C	Fairchild			DM54LS22
	AM25LS07M	† AMD					9LS09M	† Fairchild			DM74LS22
	SN54LS378	† AMD					54LS09	† Fairchild			National
	SN74LS378	AMD					(continued)				54LS22
	(continued)										† Raytheon
											see page 282
											(continued)

† Military Temperature Range (−55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

DIGITAL—TTL - Low Power Schottky (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line	
Gates, AND/NAND (cont)				Gates, AND/NAND (cont)				Gates, AND-OR-Invert (cont)				
Dual 4-Input NAND Gate, Open Collector (continued)				Quad 2-Input NAND Gate, Open Collector (continued)				2-Wide, 4-Input AND-OR-Invert Gate (continued)				
	S54LS22	† Signetics		9LS38M	† Fairchild				DM54LS55	† National		
	see page 384			54LS03	† Fairchild			DM74LS55	National		90	
	N74LS22	Signetics		74LS03	Fairchild			54LS55	† Raytheon			
	see page 384			DM54LS01	† National			see page 282				
	SN54LS22	† TI		DM74LS01	National	50		N74LS55	Signetics			
	SN74LS22	TI		DM54LS03	† National			see page 384				
Triple 3-Input NAND Gate				54LS01					S54LS55	† Signetics		
	9LS10C	Fairchild		see page 282	† Raytheon			SN54LS55	† TI			
	9LS10M	† Fairchild		54LS03	† Raytheon			SN74LS55	TI			
	54LS10	† Fairchild		see page 282								
	74LS10	Fairchild		54LS38	† Raytheon							
	DM54LS10	† National	10	see page 282								
	DM74LS10	National		N74LS01	Signetics							
	54LS10	† Raytheon		see page 384								
	see page 282			N74LS03	Signetics							
	N74LS10	Signetics		see page 384								
	see page 384			N74LS38	Signetics							
	S54LS10	† Signetics		see page 384								
	see page 384			S54LS01	† Signetics							
	SN54LS10	† TI		see page 384								
	SN74LS10	TI		S54LS03	† Signetics	60						
				see page 384								
Triple 3-Input NAND Gate, Open Collector				54LS38								
	DM54LS12	† National		see page 282								
	DM74LS12	National		N74LS01	Signetics							
	54LS12	† Raytheon		see page 384								
	see page 282			N74LS03	Signetics							
	N74LS12	Signetics		see page 384								
	see page 384			N74LS38	Signetics							
	S54LS12	† Signetics	20	see page 384								
	see page 384			S54LS01	† Signetics							
	SN54LS12	† TI		see page 384								
	SN74LS12	TI		S54LS38	† Signetics							
				see page 384								
Quad 2-Input NAND Gate				SN54LS01								
	9LS00C	Fairchild		† TI								
	9LS00M	† Fairchild		SN74LS01	TI							
	54LS00	† Fairchild		SN54LS03	† TI							
	74LS00	Fairchild		SN74LS03	TI							
	DM54LS00	† National		SN54LS38	† TI							
	DM74LS00	National		SN74LS38	TI							
	54LS00	† Raytheon										
	see page 282											
	N74LS00	Signetics	30									
	see page 384											
	S54LS00	† Signetics										
	see page 384											
	SN54LS00	† TI										
	SN74LS00	TI										
Quad 2-Input NAND Buffer				Quad 2-Input NAND Buffer, Open Collector				Dual 2-Wide 2/3-Input AND-OR-Invert Gate				
	9LS37C	Fairchild		9LS38C	Fairchild				9LS51C	Fairchild		
	9LS37M	† Fairchild		9LS38M	† Fairchild		70		9LS51M	† Fairchild		
	54LS37	† Fairchild		54LS38	† Fairchild				54LS51	† Fairchild		
	74LS37	Fairchild		74LS38	Fairchild				74LS51	Fairchild	110	
	54LS37	† Raytheon		N74LS38	Signetics				DM54LS51	† National		
	see page 282			see page 384					DM74LS51	National		
	N74LS37	Signetics		S54LS38	† Signetics				54LS51	† Raytheon		
	see page 384			see page 384					see page 282			
	S54LS37	† Signetics		SN54LS38	† TI				N74LS51	Signetics		
	see page 384			SN74LS38	TI				see page 384			
	SN54LS37	† TI							S54LS51	† Signetics		
	SN74LS37	TI							see page 384			
									SN54LS51	† TI		
									SN74LS51	TI		
Quad 2-Input NAND Gate, Open Collector				Quad 2-Input NAND Buffer, Open Collector, to 15 V				Gates, Exclusive OR/NOR				
	9LS03C	Fairchild		54LS26	† Fairchild			Quad 2-Input Exclusive OR Gate				
	9LS03M	† Fairchild		74LS26	Fairchild				9LS86C	Fairchild		
	9LS38C	Fairchild		DM54LS26	† National				9LS86M	† Fairchild		
	(continued)			DM74LS26	National				54LS86	† Fairchild	120	
				54LS26	† Raytheon		80		74LS86	Fairchild		
				see page 282					54LS86	† Raytheon		
				N74LS26	Signetics				see page 282			
				see page 384					54LS386	† Raytheon		
				S54LS26	† Signetics				see page 282			
				see page 384					N74LS86	Signetics		
				SN54LS26	† TI				see page 384			
				SN74LS26	TI				S54LS86	† Signetics		
									see page 384			
									N74LS386	Signetics		
									see page 384			
									S54LS386	† Signetics		
									see page 384			
									SN54LS86	† TI		
									SN74LS86	TI		
									SN54LS386	† TI	130	
									(continued)			

† Military Temperature Range (-55°C to 125°C)

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Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line	
Gates, Exclusive OR/NOR (cont)				Gates, OR/NOR (cont)				Memories				
Quad 2-Input Exclusive OR Gate (continued)				Triple 3-Input NOR Gate (continued)				16-Bit (4 x 4) Register File Simultaneous Read/Write				
	SN74LS386	TI			SN74LS27	TI			9LS170C	Fairchild		
Quad 2-Input Exclusive OR Gate, Open Collector				Quad 2-Input NOR Gate				9LS170M † Fairchild				
	9LS136C	Fairchild			9LS02C	Fairchild			54LS170	† Fairchild		
	9LS136M	† Fairchild			9LS02M	† Fairchild			74LS170	Fairchild		
	54LS136	† Fairchild			54LS02	† Fairchild			N74LS170	Signetics		
	74LS136	Fairchild			74LS02	Fairchild			see page 384			
	54LS136	† Raytheon			DM54LS02	† National			S54LS170	† Signetics		
	see page 282				DM74LS02	National			see page 384			
	N74LS136	Signetics			54LS02	† Raytheon	50		SN54LS170	† TI	90	
	see page 384				see page 282				SN74LS170	TI		
	S54LS136	† Signetics			N74LS02	Signetics		16-Bit (4 x 4) Register File, Simultaneous Read/Write, Three-State				
	see page 384				see page 384				9LS670C	Fairchild		
	SN54LS136	† TI			S54LS02	† Signetics			9LS670M	† Fairchild		
	SN74LS136	TI	10		see page 384				54LS670	† Fairchild		
Quad 2-Input Exclusive NOR Gate, Open Collector				Quad 2-Input NOR Buffer				74LS670 Fairchild				
	9LS266C	Fairchild			54LS28	† Raytheon			54LS670	† Raytheon		
	9LS266M	† Fairchild			see page 282				N74LS670	Signetics		
	54LS266	† Fairchild			N74LS28	Signetics			see page 384			
	74LS266	Fairchild			see page 384				S54LS670	† Signetics		
	54LS266	† Raytheon			S54LS28	† Signetics			see page 384			
	see page 282				see page 384				SN54LS670	† TI		
	N74LS266	Signetics			SN54LS28	† TI			SN74LS670	TI	100	
	see page 384				SN74LS28	TI		Multiplexers				
	S54LS266	† Signetics			Quad 2-Input NOR Buffer, Open Collector				Quad 2-Input Multiplexer, Non-Inverting			
	see page 384					54LS33	† Raytheon			AM25LS157C	AMD	
	SN54LS266	† TI				see page 282				AM25LS157M	AMD	†
	SN74LS266	TI				N74LS33	Signetics			SN54LS157	† AMD	
Gates, OR/NOR				Latches				SN74LS157 AMD				
Quad 2-Input OR Gate				8-Bit Addressable Latch				9LS157C Fairchild				
	9LS32C	Fairchild	20		54LS259	† Fairchild			9LS157M	† Fairchild		
	9LS32M	† Fairchild			74LS259	Fairchild			54LS157	† Fairchild		
	54LS32	† Fairchild			SN54LS259	† TI			74LS157	Fairchild		
	74LS32	Fairchild			SN74LS259	TI			54LS157	† Raytheon		
	54LS32	† Raytheon			Dual 4-Bit Addressable Latch					see page 282		
	see page 282					54LS255	† Fairchild		N74LS157	Signetics	110	
	N74LS32	Signetics				74LS255	Fairchild	70	see page 384			
	see page 384					SN54LS259	† TI		S54LS157	Signetics		
	S54LS32	† Signetics				SN74LS259	TI		see page 384			
	see page 384					Quad Bistable Latch, Complementary Output					SN54LS157	† TI
	SN54LS32	† TI					54LS255	† Fairchild		SN54LS157	† TI	
	SN74LS32	TI					74LS255	Fairchild		SN74LS157	TI	
Dual 5-Input NOR Gate				Dual 4-Bit Addressable Latch				Quad 2-Input Multiplexer, Non-Inverting, Three-State				
	54LS260	† Fairchild				54LS255	† Fairchild			AM25LS257C	AMD	
	74LS260	Fairchild	30			74LS255	Fairchild	70		AM25LS257M	AMD	†
	N74LS260A	Signetics				Quad Bistable Latch, Complementary Output					SN54LS257	† AMD
	see page 384						N74LS75	Signetics		SN74LS257	AMD	
	S54LS260A	† Signetics					see page 384			9LS257C	Fairchild	
	see page 384						S54LS75	† Signetics		9LS257M	† Fairchild	
	SN54LS32	† TI					see page 384			54LS257	† Fairchild	
	SN74LS32	TI					SN54LS75	† TI		74LS257	Fairchild	120
Triple 3-Input NOR Gate				Quad Bistable Latch				54LS257 † Fairchild				
	9LS27C	Fairchild				SN54LS77	TI		54LS257	† Raytheon		
	9LS27M	† Fairchild				Quad S-R Latch				see page 282		
	54LS27	† Fairchild					9LS279C	Fairchild		N74LS257	Signetics	
	74LS27	Fairchild					9LS279M	† Fairchild		see page 384		
	DM54LS27	† National					54LS279	† Fairchild		S54LS257	† Signetics	
	DM74LS27	National					74LS279	Fairchild		see page 384		
	54LS27	† Raytheon					SN54LS279	† TI		SN54LS257	† TI	
	see page 282						SN74LS279	TI		SN74LS257	TI	
	N74LS27	Signetics					9LS279C	Fairchild		Quad 2-Input Multiplexer, Inverting		
	see page 384						9LS279M	† Fairchild			AM25LS158C	AMD
	S54LS27	† Signetics					54LS279	† Fairchild			AM25LS158M	AMD
	see page 384						74LS279	Fairchild			SN54LS158	† AMD
	SN54LS27	† TI					SN54LS279	† TI			(continued)	
	(continued)						SN74LS279	TI				

† Military Temperature Range (-55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

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Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line	
Multiplexers (cont)				Multiplexers (cont)				Multiplexers (cont)				
Quad 2-Input Multiplexer, Inverting (continued)	SN74LS158	AMD	10	Dual 4-Input Multiplexer, Inverting	SN54LS352	† TI	60	8-Input Multiplexer, Strobe, Complementary Output, Three-State (continued)	N74LS251	Signetics	110	
	9LS158C	Fairchild				SN74LS352		TI		see page 384		
	9LS158M	† Fairchild			Dual 4-Input Multiplexer, Three-State	AM25LS253C		AMD		SN54LS251		† TI
	54LS158	† Fairchild				AM25LS253M		AMD	†	SN74LS251		TI
	74LS158	Fairchild				SN54LS253		† AMD				
	54LS158	† Raytheon				SN74LS253		AMD				
	see page 282					9LS253C		Fairchild				
	N74LS158	Signetics				9LS253M		† Fairchild				
	see page 384					54LS253		† Fairchild				
	S54LS158	† Signetics				74LS253		Fairchild				
	see page 384				DM54LS253	† National						
	SN54LS158	† TI			DM74LS253	National						
	SN74LS158	TI			SN54LS253	† National						
					SN74LS253	National						
					54LS253	† Raytheon						
					see page 282							
					N74LS253	Signetics						
					see page 384							
					S54LS253	† Signetics						
					see page 384							
					SN54LS253	† TI						
					SN74DC253	TI						
Quad 2-Input Multiplexer, Inverting Three State	AM25LS258C	AMD	20	8-Input Data Selector/Multiplexer, Single Output	9LS152C	Fairchild	70				120	
	AM25LS258M	AMD		†		9LS152M		† Fairchild				
	SN54LS258	† AMD				54LS152		† Fairchild				
	SN74LS258	AMD				74LS152		Fairchild				
	9LS258C	Fairchild				54LS152		† Raytheon				
	9LS258M	† Fairchild				see page 282						
	54LS258	† Fairchild				SN54LS152		† TI				
	74LS258	Fairchild				SN74LS152		TI				
	54LS258	† Raytheon										
	see page 282											
	N74LS258	Signetics										
	see page 384											
	S54LS258	† Signetics										
	see page 384											
	SN54LS258	† TI										
	SN74LS258	TI										
Quad 2-Input Multiplexer with Storage	9LS298C	AMD	30	8-Input Multiplexer, Strobe, Complementary Output	AM25LS151C	AMD	80				130	
	9LS298M	† AMD				AM25LS151M		AMD	†			
	AM25LS09C	AMD				SN54LS151		† AMD				
	AM25LS09M	† AMD				SN74LS151		AMD				
	SN54LS399	† AMD				9LS151C		Fairchild				
	SN74LS399	AMD				9LS151M		† Fairchild				
	9LS298C	Fairchild				54LS151		† Fairchild				
	9LS298M	† Fairchild				74LS151		Fairchild				
	54LS298	† Fairchild				DM54LS151		† National				
	74LS298	Fairchild				DM74LS151		National				
	SN54LS298	† TI			54LS151	† Raytheon						
	SN74LS298	TI			see page 282							
	SN54LS399	† TI			N74LS151	Signetics						
	SN74LS399	TI			see page 384							
					S54LS151	† Signetics						
					see page 384							
					SN54LS151	† TI						
					SN74LS151	TI						
Dual 4-Input Multiplexer	AM25LS153C	AMD	40	8-Input Multiplexer, Strobe, Complementary Output, Three-State	AM25LS251C	AMD	90				140	
	AM25LS153M	AMD		†		AM25LS251M		AMD	†			
	SN54LS153	† AMD				SN54LS251		† AMD				
	SN74LS153	AMD				SN74LS251		AMD				
	9LS153C	Fairchild				9LS251C		Fairchild				
	9LS153M	† Fairchild				9LS251M		† Fairchild				
	54LS153	† Fairchild				54LS251		† Fairchild				
	74LS153	Fairchild				74LS251		Fairchild				
	54LS153	† Raytheon				54LS251		† Raytheon				
	see page 282					see page 282						
	S54LS153	† Signetics			S54LS251	† Signetics						
	see page 384				see page 384							
	N74LS153	Signetics			(continued)							
	see page 384											
	SN54LS153	† TI										
	SN74LS153	TI										
			50									

† Military Temperature Range (-55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

DIGITAL—TTL - Low Power Schottky (cont)

Function	Device	Source	Line	Function	Device	Source	Line	
Shift Registers (cont)				Miscellaneous (cont)				
4-Bit Parallel In, Parallel Out, Right/Left Shift Register, Three-State (continued)	54LS295A	† Raytheon		Dual Voltage Controlled Oscillator (or Crystal Controlled)	SN54LS124	† TI		
	see page 282				SN74LS124	TI		
	N74LS295	Signetics		Hex Current Sensing Interface Gate	SN54LS63	† TI	50	
	S54LS295	† Signetics			SN74LS63	TI		
	SN54LS295A	† TI		-Bit Parity Generator/Checker	SN54LS280	† TI		
SN74LS295A	TI		SN74LS280		TI			
4-Bit Bidirectional Universal Shift Register	AM25LS194AC	AMD		Dual 4-Input NAND Gate, Schmitt Trigger	N74LS13	Signetics		
	AM25LS194AM	AMD	†		see page 384			
	SN54LS194A	† AMD			S54LS13	† Signetics		
	SN74LS194A	AMD			see page 384			
	9LS194C	Fairchild	10	SN54LS13	† TI		60	
	9LS194M	† Fairchild		SN74LS13	TI			
	54LS194	† Fairchild		Quad 2-Input NAND Gate, Schmitt Trigger	9LS132C	Fairchild		
	74LS194	Fairchild			9LS132M	† Fairchild		
	54LS194A	† Raytheon			54LS132	† Fairchild		
	see page 282				74LS132	Fairchild		
N74LS194A	Signetics		N74LS132	Signetics				
see page 384			see page 384					
S54LS194A	Signetics		S54LS132	† Signetics				
see page 384			see page 384					
SN54LS194A	† TI		SN54LS132	† TI				
SN74LS194A	TI		SN74LS132	TI				
5-Bit Parallel Out Shift Register	N74LS96	Signetics		Hex Schmitt Trigger Inverting	9LS14C	Fairchild	70	
	see page 384				9LS14M	Fairchild		
	S54LS96	† Signetics	20		54LS14	† Fairchild		
	see page 384				74LS14	Fairchild		
	SN54LS96	† TI			N74LS14	Signetics		
SN74LS96	TI		see page 384					
8-Bit Gated Serial In, Parallel Out Shift Register	AM25LS164C	AMD		S54LS14	† Signetics			
	AM25LS164M	AMD	†	see page 384				
	SN54LS164	† AMD		SN54LS14	† TI			
	SN74LS164	AMD		SN74LS14	TI			
	9LS164C	Fairchild		Microprogram Sequences	AM2909C	AMD		
	9LS164M	† Fairchild			AM2909M	† AMD		
	54LS164	† Fairchild						
	74LS164	Fairchild	30					
	N74LS164	Signetics						
	see page 384							
S54LS164	† Signetics							
see page 384								
SN54LS164	† TI							
SN74LS164	TI							
8-Bit Serial In, Serial Out Shift Register	SN54LS91	† TI						
	SN74LS91	TI						
8-Bit Bidirectional Shift Register	AM25LS22C	AMD						
	AM25LS22M	† AMD						
	AM25LS23C	AMD						
	AM25LS23M	† AMD						
	AM25LS299C	AMD						
	AM25LS299M	AMD	†					
	SN54LS299	† AMD						
	SN74LS299	AMD						
Miscellaneous								
Voltage Controlled Oscillator (or Crystal Controlled)								
	SN54LS324	† TI						
	SN74LS324	TI						

† Military Temperature Range (-55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

DIGITAL—TTL - Schottky

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line
Arithmetic Functions				Buffers/Inverters (cont)				Counters, Miscellaneous			
4-Bit Binary Adder	SN54S283 SN74S283	† TI TI		Hex Inverter (continued)	9S04AC 9S04AM HD74S04 DM74S04 N74S04 N8T93 SN54S04 SN74S04	Fairchild † Fairchild Hitachi National Signetics Signetics † TI TI		Variable Modulo Counter (Divide by 2, 4, 5, 6, 8, 10, 12, 14, 16)	93S05C 93S05M	Fairchild † Fairchild	100
4-Bit BCD Adder	N82S83	Signetics						Decoders, Drivers			
4-Bit BCD Arithmetic Unit (Add, Subtract, Compare)	N82S82	Signetics						3-Line to 8-Line Decoder			
Arithmetic and Logic Shift Matrix, Bit and Byte Masking	9404C 9404M	Fairchild † Fairchild		Hex Inverter, Open Collector	54S05 74S05 9S05AC 9S05AM HD74S05 DM74S05 N74S05 N8T94 SN54S05 SN74S05	† Fairchild Fairchild Fairchild † Fairchild Hitachi National Signetics Signetics † TI TI	60	3-Line to 8-Line Decoder/Demultiplexer			
Arithmetic Logic Unit/Function Generator (16 Function)	SN54S181 SN74S181 54S181 74S181 93S41C 93S41M HD74S181 N74S181 SN54S181 SN74S181	† AMD AMD † Fairchild Fairchild Fairchild † Fairchild Hitachi Signetics † TI TI	10					3-Line to 8-Line Decoder/Demultiplexer with Input Latches			
Arithmetic Logic/Function Generator (8 Function)	SN54S381 SN74S381	† TI TI		Octal (Dual Quad) Inverter (Driver) Hysteresis, Three State	SN74S240	TI	70	Dual 2-Line to 4-Line Decoder/Demultiplexer			
Accumulator, 4-Bit Parallel Binary (ALU, Shift; Expandable)	SN54S281 SN74S281	† TI TI	20	Counters, Binary				Dual 4-Line to 4-Line Decoder/Demultiplexer			
Carry Look-ahead Unit (for 54/74S181, 54/74S281, 74S381)	54S182 74S182 93S42C 93S42M N74S182 SN54S182 SN74S182	† Fairchild Fairchild Fairchild † Fairchild Signetics † TI TI		4-Bit Binary Synchronous Counter	SN54S161 SN74S161 93S16C 93S16M 93S16C 93S16M SN54S163 SN74S163	† AMD AMD AMD † AMD Fairchild † Fairchild † TI TI		BCD-to-Decimal Decoder			
4-Bit Microcontroller (ALU, Shift and Registers; Expandable Section of a CPU)	9405C 9405M 5701 6701	Fairchild † Fairchild † MMI MMI	30	4-Bit Binary Up/Down Counter, Synchronous	SN54S169 SN74S169	† TI TI	80	N82S52 Signetics			
2's Complement Multiplier (4-Bit x 2-Bit)	AM25S05C AM25S05M 93S43C 93S43M	AMD † AMD Fairchild † Fairchild		4-Bit Universal Shift Register, Binary Up/Down Counter, Synchronous	SN74S291	TI		Dual 4-Input Positive NAND 50 Ohm Line Driver			
4-By-4-Bit Binary Multiplier, Three-State	SN74S274	TI		Binary Counter (Divide by 2, 4, 8, 16) Asynchronous Preset Input	N74S197 N82S91 SN54S197 SN74S197	Signetics Signetics † TI TI		54S140 † Fairchild 74S140 † Fairchild HD74S140 Hitachi DM74S140 National N74S140 Signetics SN54S140 † TI SN74S140 TI			
7-Bit Slice Wallace Tree (to build multipliers)	SN54S275 SN74S275	† TI TI		Counters, Decade				Flip-Flops			
4-Bit Magnitude Comparator	SN54S85 SN74S85	† TI TI	40	Decade Synchronous Counter	SN54S160 SN74S160 93S10C 93S10M 93S10C 93S10M SN54S162 SN74S162	† AMD AMD AMD † AMD Fairchild † Fairchild † TI TI	90	Dual "J-K" Negative Edge-Triggered Flip-Flop with Individual Clock, Asynchronous Preset and Clear			
6-Bit Identity Comparator	93S46C 93S46M	Fairchild † Fairchild		Decade Up/Down Counter, Synchronous	SN54S168 SN74S168	† TI TI		54S112 † Fairchild 74S112 Fairchild HD74S112 Hitachi DM74S112 National N74S112 Signetics SN54S112 † TI SN74S112 TI			
6-Bit Identity Comparator, Open Collector	93S47C 93S47M	Fairchild † Fairchild		Decade Counter (Divide by 2 and Divide by 5), Asynchronous Preset Input	N74S196 N82S90 SN54S196 SN74S196	Signetics Signetics † TI TI		Dual "J-K" Negative Edge-Triggered Flip-Flop with Individual Preset and Clock			
Buffers/Inverters								54S113 † Fairchild 74S113 Fairchild HD74S113 Hitachi DM74S113 National N74S113 Signetics SN54S113 † TI SN74S113 TI			
Hex Buffer, Three-State	N8T95 N8T96 N8T97 N8T98	Signetics Signetics Signetics Signetics						Negative Edge-Triggered Flip-Flop with Common Clock and Common Clear			
Octal (Dual Quad), Buffer (Driver), Hysteresis, Three-State	SN74S241	TI						54S114 † Fairchild 74S114 Fairchild HD74S114 Hitachi DM74S114 National N74S114 Signetics SN54S114 † TI SN74S114 TI			
Hex Inverter	54S04 74S04 (continued)	† Fairchild Fairchild	50					140			

† Military Temperature Range (-55°C to 125°C)

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DIGITAL—TTL - Schottky (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line			
Flip-Flops (cont)				Gates, AND/NAND (cont)				Gates, AND/NAND (cont)						
Dual "J-K" Edge-Triggered Flip-Flop with Set and Clear	54S109 74S109	† Fairchild Fairchild		Quad 2-Input AND Gate (continued)	SN74S08	TI		Quad 2-Input NAND Gate	54S00 74S00 ZN54S00 ZN74S00 HD74S00 DM74S00 N74S00 SN54S00 SN74S00	† Fairchild † Fairchild † Ferranti Ferranti Hitachi National Signetics † TI TI	120			
Dual D-Type Edge-Triggered Flip-Flop with Preset and Clear	54S74 74S74 HD74S74 DM74S74 N74S74 SN54S74 SN74S74	† Fairchild Fairchild Hitachi National Signetics † TI TI		Quad 2-Input AND Gate, Open Collector	54S09 74S09 SN54S09 SN74S09	† Fairchild Fairchild † TI TI		Quad 2-Input NAND Gate (Buffer)	SN54S37 SN74S37	† TI TI				
Quad D-Type Flip-Flop, Standard TTL and Three-State Outputs	AM25S18C AM25S18M	AMD † AMD	10	2-2-3-3 Input AND Gate	9S41C 9S41M	Fairchild † Fairchild	60	Quad 2-Input NAND Gate, Open Collector	54S03 74S03 ZN54S03 ZN74S03 HD74S03 DM74S03 N74S03 SN54S03 SN74S03	† Fairchild Fairchild † Ferranti Ferranti Hitachi National Signetics † TI TI	130			
Quad D-Type Edge-Triggered Flip-Flop with Clear and Complementary Output	SN54S175 SN74S175 54S175 74S175 HD74S175 N74S175 SN74S175 SN54S175	† AMD AMD † Fairchild Fairchild Hitachi Signetics TI † TI		8-Input NAND Gate	54S30 74S30 DM74S30 SN54S30 SN74S30	† Fairchild Fairchild National † TI TI		Quad 2-Input NAND Gate, (Buffer), Open Collector	SN54S38 SN74S38	† TI TI				
Quad D-Type Edge-Triggered Flip-Flop with Common Clock Enable	AM25S08C AM25S08M	AMD † AMD	20	12-Input NAND Gate, Three-State	54S134 74S134 HD74S134 DM74S134 N74S134 SN54S134 SN74S134	† Fairchild Fairchild Hitachi National Signetics † TI TI	70	Quad 2-Input NAND Gate, (Buffer), Open Collector	SN54S38 SN74S38	† TI TI				
Quad Selectable Input D-Type Edge-Triggered Flip-Flop	AM25S09C AM25S09M	AMD † AMD		13-Input NAND Gate	54S133 HD74S133 74S133 DM74S133 N74S133 SN54S133 SN74S133	† Fairchild Hitachi Fairchild National Signetics † TI TI		Gates, AND/OR/AND-OR-Invert						
Hex D-Type Edge-Triggered Flip-Flop with Clear	SN54S174 SN74S174 54S174 74S174 HD74S174 N74S174 SN54S174 SN74S174	† AMD AMD † Fairchild Fairchild Hitachi Signetics † TI TI	30	Dual 4-Input NAND Gate	54S20 74S20 ZN54S20 ZN74S20 HD74S20 DM74S20 N74S20 SN54S20 SN74S20	† Fairchild Fairchild † Ferranti Ferranti Hitachi National Signetics † TI TI	80	Dual 2-4 Input AND-OR Gate	9S42C 9S42M	Fairchild Fairchild				
Hex D-Type Edge-Triggered Flip-Flop with Common Clock Enable	AM25S07C AM25S07M	AMD † AMD		Dual 4-Input NAND Buffer	54S40 74S40 HD74S40 DM74S40 N74S40 SN54S40 SN74S40	† Fairchild Fairchild Hitachi National Signetics † TI TI	90	4-2-3-2 Input AND-OR-Invert Gate	54S64 74S64 HD74S64 DM74S64 N74S64 SN54S64 SN74S64	† Fairchild † Fairchild Hitachi National † Signetics TI TI	140			
Octal D-Type Edge-Triggered Flip-Flop, Three-State	SN74S374	TI		Dual 4-Input NAND Gate, Open Collector	54S22 74S22 ZN54S22 ZN74S22 HD74S22 DM74S22 N74S22 SN54S22 SN74S22	† Fairchild Fairchild † Ferranti Ferranti Hitachi National Signetics † TI TI	100	4-2-3-2 Input AND-OR-Invert Gate, Open Collector	54S65 74S65 HD74S65 DM74S65 SN54S65 SN74S65	† Fairchild † Fairchild Hitachi National † TI TI				
Gates, AND/NAND				Dual 4-Input NAND Invert Gate				4-2-3-2 Input AND-OR-Invert Dual 2-Wide 2-Input AND-OR-Invert Gate						
Triple 3-Input AND Gate	54S11 74S11 HD74S11 DM74S11 N74S11 S54S11 SN54S11 SN74S11	† Fairchild Fairchild Hitachi National Signetics † Signetics † TI TI	40	Dual 4-Input NAND Invert Gate, Open Collector	54S20 74S20 ZN54S20 ZN74S20 HD74S20 DM74S20 N74S20 SN54S20 SN74S20	† Fairchild Fairchild † Ferranti Ferranti Hitachi National Signetics † TI TI	80	4-2-3-2 Input AND-OR-Invert Dual 2-Wide 2-Input AND-OR-Invert Gate	54S51 74S51 SN54S51 SN74S51	† Fairchild Fairchild † TI TI	150			
Triple 3-Input AND Gate, Open Collector	54S15 74S15 HD74S15 DM74S15 N74S15 S54S15 SN54S15 SN74S15	† Fairchild Fairchild Hitachi National Signetics † Signetics † TI TI	50	Triple 3-Input NAND Gate	54S10 74S10 HD74S10 DM74S10 N74S10 SN54S10 SN74S10	† Fairchild Fairchild Hitachi National Signetics † TI TI	110	Gates, Exclusive OR/NOR						
Quad 2-Input AND Gate	54S08 74S08 SN54S08 (continued)	† Fairchild Fairchild † TI		Quad 2-Input Exclusive-OR Gate			54S86 74S86 HD74S86 DM74S86 N82S41 S54S86 SN54S86 SN74S86	† Fairchild Fairchild Hitachi National Signetics † Signetics † TI TI	160	Quad 2-Input Exclusive-OR Gate, Open Collector		DM74S136	National	
				Quad 2-Input Exclusive NOR Gate, Open Collector				N82S42				Signetics		

† Military Temperature Range (-55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

DIGITAL—TTL - Schottky (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line		
Gates, Exclusive OR/NOR (cont)				Memories (cont)				Multiplexers (cont)					
Quad Exclusive OR/NOR Gate				80-Bit (16 x 5) First-In/First-Out Memory, Asynchronous, Three-State				8-Input Multiplexer					
	54S135	† Fairchild			SN74S225	TI			N82S30	Signetics			
	74S135	Fairchild							N82S31	Signetics			
	HD74S135	Hitachi							N82S32	Signetics			
	DM74S135	National		Multiplexers				8-Input Multiplexer, Strobe, Complementary Output					
	N74S135	Signetics		Quad 2-Input Digital Multiplexer (Suitable for Driving Adders, Registers)						SN54S151	† AMD		
	SN54S135	† TI			N82S33	Signetics			SN74S151	AMD			
	SN74S135	TI			N82S66	Signetics			54S151	† Fairchild			
Gates, OR/NOR				Quad 2-Input Multiplexer, Non-Inverting						74S151	Fairchild		
Quad 2-Input OR Gate					SN54S157	† AMD	50		93S12C	Fairchild			
	54S32	† Fairchild			SN74S157	AMD			93S12M	† Fairchild			
	74S32	Fairchild			93S22C	AMD			HD74S151	Hitachi	110		
	SN54S32	† TI			93S22M	† AMD			DM74S151	National			
	SN74S32	TI			54S157	† Fairchild			N74S151	Signetics			
Dual 5-Input NOR Gate					74S157	Fairchild			SN54S151	† TI			
	SN54S260	† TI			DM74S157	National			SN74S151	TI			
	SN74S260	TI			N74S157	Signetics		8-Input Multiplexer, Complementary Three-State Output					
Quad 2-Input NOR Gate					N82S33	Signetics				SN54S251	† AMD		
	54S02	† Fairchild			SN54S157	† TI	60			SN74S251	AMD		
	74S02	Fairchild			SN74S157	TI			54S251	† Fairchild			
	DM74S02	National		Quad 2-Input Multiplexer, Non-Inverting, Three-State						74S251	Fairchild		
	SN54S02	† TI			SN54S257	† AMD			HD74S251	Hitachi	120		
	SN74S02	TI			SN74S257	AMD			N74S251	Signetics			
Latches					54S257	† Fairchild		Dual Retriggerable, Resettable Monostable Multivibrator					
6-Bit Latch (Independent 2 and 4-Bit)					74S257	Fairchild				AM26S02C	AMD		
	3404	Intel			S54S257	† Signetics				AM26S02M	† AMD		
8-Bit Latch, Transparent D-Type, Three-State					N74S257	Signetics				96S02C	Fairchild		
	SN54S412	† TI	20		SN54S257	† TI				96S02M	† Fairchild		
	SN74S373	TI		Quad 2-Input Multiplexer, Inverting					Shift Registers				
	SN74S412	TI			SN54S158	† AMD	70	4-Bit Shifter, Three-State (Shifts 0, 1, 2, or 3 Bits Under 2-Line Select Control)					
Memories					SN74S158	AMD				AM25S10C	AMD		
16-Bit (8 x 2) Multiple Port Register File, Simultaneous Read/Write, Three-State					54S158	† Fairchild		4-Bit Parallel-In, Parallel-Out Shift Register					
	N74S172	Signetics			74S158	Fairchild				SN54S195	† AMD		
32-Bit (8 x 4) Multiport RAM					DM74S158	National				SN74S195	AMD	130	
	N82S12	Signetics			N74S158	Signetics				93S00C	Fairchild		
	see page 804, 806, 810, 825112	Signetics			N82S66	Signetics				93S00M	† Fairchild		
	N82S112	Signetics			SN54S158	† TI				54S195	Fairchild		
	see page 804, 806, 810,				SN74S158	TI				74S195	Fairchild		
64-Bit (16 x 4) Bipolar Read/Write RAM, Three-State					Quad 2-Input Multiplexer, Inverting, Open Collector						N74S179	Signetics	
	AM27S03C	AMD			N82S34	Signetics				N74S178	Signetics		
	AM27S03M	† AMD			N82S67	Signetics				N74S195	Signetics		
	SN54S189	† AMD			Quad 2-Input Multiplexer, Inverting, Three/State						N82S70	Signetics	
	SN74S189	AMD				SN54S258	† AMD	80		N82S71	Signetics		
	93405C	Fairchild				SN74S258	AMD			SN54S195	† TI	140	
	93405M	† Fairchild				54S258	† Fairchild			SN74S195	TI		
	SN54S189	† TI				74S258	Fairchild						
	SN74S189	TI	30			S54S258	† Signetics						
64-Bit (16 x 4) Bipolar Read/Write RAM, Open Collector						N74S258	Signetics						
	AM27S02C	AMD				SN54S258	† TI						
	AM27S02M	† AMD				SN74S258	TI						
	SN54S289	† AMD		Dual 4-Input Multiplexer									
	SN74S289	AMD				SN54S153	† AMD	90					
	93404C	Fairchild				SN74S153	AMD						
	93404M	† Fairchild				54S153	† Fairchild						
	3101A	Intel	40			74S153	Fairchild						
	SN54S289	† TI				DM74S153	National						
	SN74S289	TI				N74S153	Signetics						
64-Bit (32 x 2) Bipolar Write-While-Read RAM						SN54S153	† TI						
	DM86S21	National				SN74S153	TI						
	N82S21	Signetics		Dual 4-Input Multiplexer Three-State									
	see page 804, 806, 812,					SN54S253	† AMD						
						SN74S253	AMD						
64-Bit (16x4) First In/First Out Memory Asynchronous, Three-State						54S253	† Fairchild						
	9403C	Fairchild				74S253	Fairchild						
	9403M	† Fairchild				N74S253	Signetics	100					

† Military Temperature Range (-55°C to 125°C)

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DIGITAL—TTL - Schottky (cont)

Function	Device	Source	Line
Miscellaneous			
9-Bit Parity Generator and Checker	82S62C	AMD	
	82S62M	† AMD	
	93S62C	Fairchild	
	93S62M	† Fairchild	
	DM74S280	National	
	N74S280	Signetics	
	N82S62	Signetics	
	SN54S280	† TI	
	SN74S280	TI	
12-Bit Parity Generator and Checker	93S48C	AMD	10
	93S48M	† AMD	
	Voltage Comparator (Analog Input-Digital Output)		
686C	AMD		
	686M		† AMD
Dual Voltage Controlled Oscillator (Also can be crystal controlled)	SN54S124	† TI	
	SN74S124	TI	
	Quad 2-Input NAND Schmitt Trigger		
54S132	† Fairchild		
74S132	Fairchild		
SN54S132	† TI		
SN74S132	TI		
4-Bit Parallel Universal Bus Transceiver, Storage, Three-State	SN54S226	† TI	20
	SN74S226	TI	
	4-Bit Parallel Bus Transceiver, Open Collector Drivers		
AM26S10C	AMD		
AM26S10M	† AMD		
AM26S11C	AMD		
AM26S11M	† AMD		
AM26S12AC	AMD		
AM26S12C	AMD		
AM26S12AM	† AMD		
AM26S12M	† AMD		
4-Bit Parallel Bus Transceiver, Inverting Three-State	N8T26	AMD	30
	S8T26	† AMD	
	N8T26	Signetics	
	4-Bit Parallel Bus Transceiver, Non-inverting, Three-State		
N8T28	Signetics		

† Military Temperature Range (-55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

IC UPDATE MASTER

DIGITAL—Special

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line
Other Digital Devices				Other Digital Devices (cont)				Other Digital Devices (cont)			
Baud Rate Generator/Programmable Divider (ROM controlled divider; supply -12.5v)	MM5307 COM5016T COM5016	National SMC SMC		Elapsed Time Counter (0.01 seconds to 1 hour, supply 2-5v)	7205	Intersil	30	Dividers, 250 MHz to 1 GHz (Listed Device is one of several related units offering this performance.)			
Custom Arrays (Digital and Linear circuits customized in final metalization)	XR-III-CHIP see page 645 XR-CHIP ULA MONOCHIP MASTERMOS XC160 XC400 ECL-ARRAY IIL-ARRAY RTL-ARRAY	Exar Exar Ferranti Interdesign		Elapsed Time Counter (0.01 seconds to 24 hours, supply 2-5v)	7045	Intersil		(continued)	MC1690 SP8602 SP8630 SP8635 SP8640 SP8650	Motorola † Plessey † Plessey † Plessey † Plessey † Plessey	70
Calculators: See Digital-Industrial/Consumer for manufacturers				Programmable Diode Matrix, 5x5	HM-074 HM-075 HM-076	† Harris † Harris † Harris		Dividers, 1 GHz and above (Listed device is one of several related units offering this performance)	MC1699 MC1697 SP8665 SP8667	Motorola Motorola Plessey Plessey	
Counter, Decade, 1 GHz and above	MC1696	Motorola		Programmable Diode Matrix, 5x8	HM-010 HM-012 HM-013	† Harris † Harris † Harris		DVM Counter/Display Driver (for 3 1/2 and 4 1/2 digit DVMs; supply -14, -24v)	S1907A	AMI	
Counter, 4 Decade (Counts and stores, BCD Output, 0.5 MHz; supply -12.5v)	AY5-4057	GI		Programmable Diode Matrix, 8x5	HM-080 HM-081 HM-084	† Harris † Harris † Harris	40	DVM Logic, 3 1/2 Decade (for dual ramp integration DVM BCD or 7 Segment Output; supply -15v)	AY5-3507	GI	
Counter/Display Decoder, 4 Decade (7 segment and BCD outputs, 0.25 MHz; supply 5v)	MK5002 MK5005 MK5007	Mostek Mostek Mostek		Programmable Diode Matrix, 4x10	HM-090 HM-091 HM-093 HM-0110	† Harris † Harris † Harris Harris		DVM Logic, 3 1/2 Decade (ramp integration, supply -7.5, -15)	AY5-3500	GI	
Counter, 5 Decade (includes storage, multiplexed BCD output, 0.6 MHz, supply -12.5v)	3815	Fairchild	20	Programmable Diode Matrix, 10x4	HM-050 HM-051 HM-055 HM-0104	† Harris † Harris † Harris Harris		DVM Logic, 4 Digits (supply -17v)	MN6032	Panasonic	
Quad Counter (two 2-decade up/down counters, 1 MHz; supply -12, ±5 v)	M003T1 M003T2	SGS † SGS		Programmable Diode Matrix, 6x8	HM-030 HM-031 HM-034 HM-0168	† Harris † Harris † Harris Harris	50	DVM Logic, 4 1/2 Digit, (dual slope integration, supply -15.5)	MM5330	National	
Counter/Display Driver, 1 Decade (7 segment output, 1 MHz; supply -13, -17v)	MEM1056	GI		Programmable Diode Matrix, 8x6	HM-040 HM-041 HM-044 HM-0186	† Harris † Harris † Harris Harris		DVM Logic, 4 1/2 Decade (Multiplexed BCD output; supply -12.5v)	3814C	Fairchild	80
Counter/Display Driver, 1 Decade (7 segment and BCD Output, 1 MHz; supply -13, -17v)	MEM1056BCD	GI		Digital Filters (Four arrays: Multiplier, Input/Output, Storage and Timing, supply -12, -28v)	351-8006	† Collins		Electronic Organ Circuits: See Digital-Industrial/Consumer for manufacturers			
Counter/Display Driver, 1 Decade Up/Down, (7 segment and BCD Output, 0.5 MHz; supply -12, -27v)	MCS1003	† MOS		Divider, divide by 1/2, 1/525, supply -12v	MN115	Panasonic		Flip-Flop, D-Type (750 MHz, ECL or TTL supplies)	11C06C	Fairchild	
Counter/Display Driver, 4 Decade (7 segment Output, 0.4 MHz; supply -12.5v; BCD and serial output versions available)	AY5-4007	GI		Divider, divide by 1/2, 1/625, supply -12v	MN116	Panasonic		Flip-Flop, D-Type Master-Slave (ECL or TTL supplies)	11C70C	Fairchild	
Counter/Display Driver, 6 Decade Up/Down (7 segment and BCD output, 1 MHz, presettable compare register, latched output, LED drive, supply 12-18v)	MK50395	Mostek		Programmable Divider (any module from 3 to 262, 145, supply -12.5)	3816	Fairchild	60	Gate, Dual OR/NOR (5/4-Input, 700ns delay, ECL or TTL supplies)	11C01C	Fairchild	
Counter/Display Driver, 7 Decade (7 segment output, supply 2-6v)	ICM7208	Intersil		Dividers, 250 MHz to 1 GHz (Listed Device is one of several related units offering this performance.)	11C05C 11C06C 11C90C 95H90M	Fairchild Fairchild Fairchild † Fairchild		Hall Effect Switch (senses magnetic field)	DN830 DN831 DN834 DN837 ULN-3006 ULN-3008 ULN-3100 ULS-3006	Panasonic Panasonic Panasonic Panasonic Sprague Sprague Sprague Sprague	90
Counter Time-Base (Oscillator, programmable divider, 10 ¹ to 10 ⁸ , 2x10 ⁴ , 6x10 ⁷ , 6x10 ⁸ and 36x10 ⁸ ; supply 5v)	MK5009	Mostek		Multiplexer Decoder, 4-Decades (they are stored, then multiplexed to provide 10 line decoded outputs; supply -12.5v)	M004T1 M004T2	SGS † SGS					

† Military Temperature Range (-55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

DIGITAL—Special (cont)

Function	Device	Source	Line
Other Digital Devices (cont)			
Programmable Logic Array (64x20 bit storage accessible through 15 or 16 independent inputs; supply -12,5v)	CRC3506	Collins	
	CRC3507	Collins	
Pulse Group Encoder (2141) and Decoder (2151) for pulse width code systems (25 ³ codes programmed by RC networks)	TMX2141	TMX	
	TMX2151	TMX	
Quad Serial Summer (Adds and subtracts serial words, used with other ICs to solve differential equations; supply -12,5v)	CRC9504	Collins	
R-Adder (Adds and subtracts serial words, see Quad Serial Summer above)	CRC9503	Collins	
Schmitt Trigger, Complementary Open Collector Output; supply 2.2 to 6v	ULN-3303	Sprague	
Schmitt Trigger, Programmable	CA3098	† RCA	
	CA3099	† RCA	
Schmitt Trigger, Zener Clamped Output; supply 2.2 to 6v	ULN-3304	Sprague	10
Schmitt Trigger, Dual, Complementary Open Collector Outputs; supply 2.2 to 6v	ULN-3305	Sprague	
Schmitt Trigger, Dual, one Open Collector Output, one Zener Clamped Output; supply 2.2 to 6v	ULN-3306	Sprague	
Schmitt Trigger, Dual, Low voltage; 3.5v	SN76811	TI	
T.V. Camera Sync. Generator; supply -12,5v	3262A	Fairchild	
	3262B	Fairchild	
	MM4320	National	
	MM5320	† National	
TV Camera Sync. Generator, supply -15, -21v	MIN6060	Panasonic	
T.V. Camera Sync. Generator; supply 5v	ZNA103E	Ferranti	
T.V. Color Bar Generator	MM5332	National	20
Watch Circuits: See Digital-Industrial/Consumer for manufacturers.			

† Military Temperature Range (-55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

Calculator Circuits

Part No.	Digits	Output	Memory	%	Const. Factor	Sq. Root	Add Mode	Kbd Type	Micro. Prog.	Intl. Clock	Process	Page
S9414	12	Disp.	1	Yes	Yes	No	Yes	Bus.	Yes	Yes	P-SiGate	254
S9651 ⁽¹⁾	10 ⁽²⁾	Disp.	1	No	Yes	Yes	No	Alg.	Yes	Yes	P-SiGate	254
9209	8-12	Disp.	1	(3)	(3)	(3)	(3)	Prog.	Yes	Yes	P-SiGate	917

⁽¹⁾ Other features (Not listed above) - Pi (π). Change sign, Square Root, Reciprocal, Square, Register exchange, Memory exchange - Scientific notation or floating input and output.

⁽²⁾ Scientific notation - 8-Digit mantissa, 2-Digit exponent

⁽³⁾ Number of digits, features, and keyboard are all microprogrammable.

Consumer Circuits

Series	Description	Digits	Power Supply (V)	Process	Packaging		
					Chip	PC Board	DIP
Watch Circuits							
S1406	Two-function LCD Watch (Same as S1400, pinouts are mirror image of S1400)	3½	+1.5	CMOS	S1409	S1407	S1408
S1410	Four-function LCD Watch (Hrs/Min/Sec or Date)	3½	+1.5	CMOS	S1411	S1412	S1413 ⁽¹⁾
S1424A	Five-function LCD Watch (Hrs/Min or Sec or Month/Date with alternating time/date mode and voltage tripler display options)	3½	+1.5	CMOS	S1424A	S1426A	S1427A
Page 255							

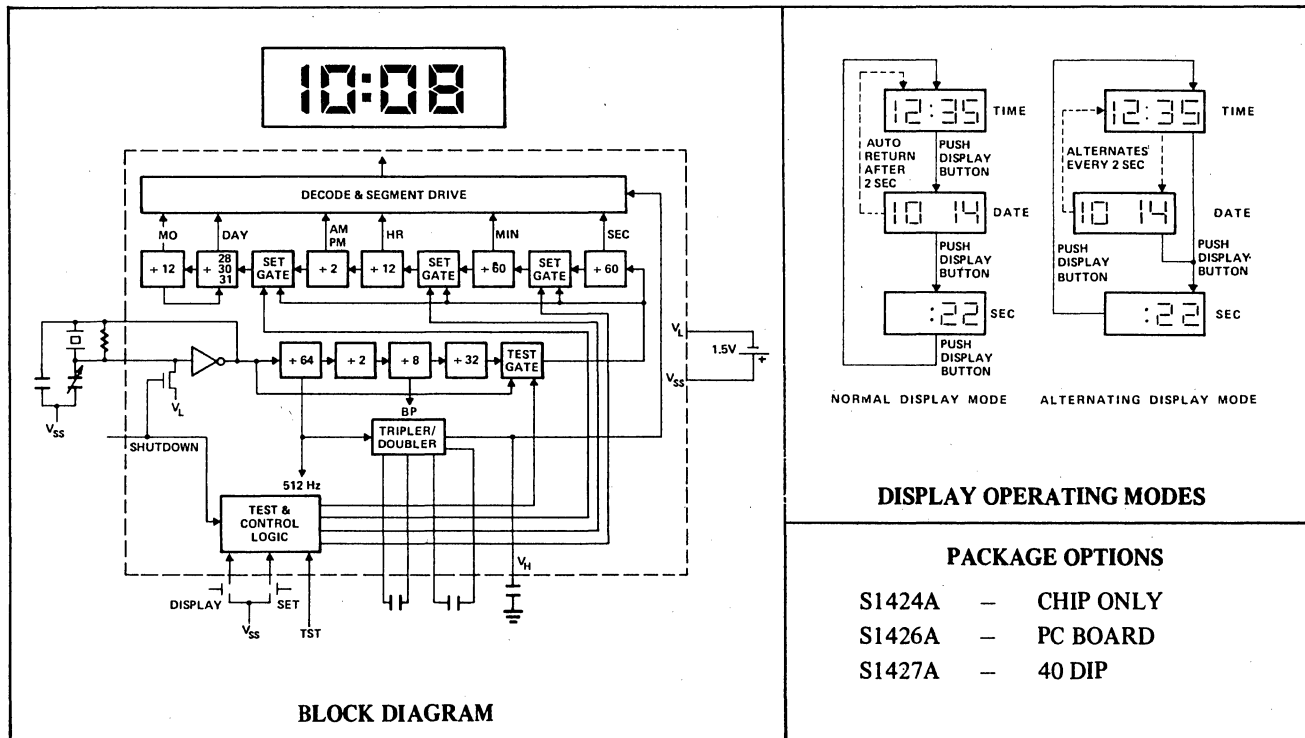
Part No.	Description	Power Supply (V)	I/O	Power Dissip. (mW)	Data Rate (MHz)	Process	Page
Clock and DVM Circuits							
S1856	LED/LCD Auto Clk. (3½ digits)	+6 to +16	MOS	70	0.256	P-I ²	254
S1907A	DVM Counter/Displ. Driver	+9, -9	MOS	50	0.5	P-I ²	254
S1998A	50/60 Hz Line Clk. (4 digits)	+8 to +29	MOS	300	50 x 10 ⁻³	P-I ²	260
Organ Circuits							
S2193	7 Stage Frequency Divider	-14, -28	MOS	300	0.1	P-I ²	254
S2470	6 Stage Frequency Divider	-10, -27	MOS	350	0.1	HI V _T	254
S2555	7 Out Frequency Synthesizer	-15, -27	MOS	400	2.1	HI V _T	254
S2556	6 Out Frequency Synthesizer	-15, -27	MOS	400	2.1	HI V _T	254
S2566	Rhythm Generator	-15, -27	MOS	300	0.1	HI V _T	254
S2567	Rhythm Generator	-15, -27	MOS	400	0.1	HI V _T	254
S50240/41/42	Top Octave Synthesizer	-14	MOS	360	2.5	P-I ²	254
S8890	Rhythm Generator	+12	MOS	400	0.01	P-I ²	254
S9660	Rhythm Generator	+12	MOS	400	0.008	P-I ²	254

⁽¹⁾ 48-lead DIP, similar to 3M

Complete Data Sheets on all Standard Products Available from Your Local AMI Sales Office Listed Inside the Front Cover.

it's
standard
at AMI®

5-FUNCTION LCD WATCH CIRCUIT



AMI

DISPLAY OPERATING MODES

PACKAGE OPTIONS

- S1424A - CHIP ONLY
- S1426A - PC BOARD
- S1427A - 40 DIP

FEATURES

- Drives Standard 3½ Digit Display
- 12 Month Calendar Memory
- One Push Button Controls Display
- Uses Single 1.5V Battery
- Displays Time, Month-Date, or Seconds
- Additional Alternating Time/Date Display Mode
- Voltage Doubler or Tripler LCD Drive Options

FUNCTIONAL DESCRIPTION

The AMI S1424A is a single chip, silicon gate CMOS watch circuit designed to drive a 3½ digit, field effect, liquid crystal display. Hour and minutes or seconds can be displayed continuously. Month and date are displayed on interrogation.

A continuous display alternating between time and date is also selectable (see operating modes above).

Only two single pole single throw switches are required to accomplish all display and setting functions. The circuit provides a full calendar function which needs to be reset only once every four years.

For a complete data sheet contact your nearest AMI Sales Office.

Display Operation is illustrated on page one. Operation in either the normal or alternating display mode is selected by the Set button during setting of the watch. When operating in the normal mode, the display initially shows hours and minutes. The absence of a colon distinguishes the Month-Date display from the Hour-Minute and Seconds display. The Seconds display is obvious as only the last two digits are used and the display is incrementing once per second.

All display and setting operations are controlled by two inputs, the Display input and the Set input. In Normal Operation only the Display input is used. Both inputs have an internal pulldown to $-V_L$ so that a single pole, single throw contact may be used.

DATE DISPLAY

The date is displayed in the normal operating mode by pushing the display button until the readout changes to Month-Date (1/2 sec. max.). The circuit will readout Month-Date for 2 to 3 seconds and return to Hours-Minutes automatically. If readout of Month-Date in excess of 2 seconds is desired, the display button is held in the depressed condition for the required time period. Upon release of the display button, the readout will return to Hour-Minute.

TESTING

A test input (TST) is furnished to facilitate high speed testing of the circuit. An internal pulldown to V_L allows this pin to float during normal operation.

SECONDS DISPLAY

In the normal operating mode the display button is pushed twice within two seconds to change from an Hour-Minutes readout to Seconds. The first press of the display button changes the readout to Month-Date. Pressing the display button again while Month-Date is being displayed causes the readout to change from Month-Date to Seconds. Once Seconds appears, the display button is released and Seconds will be shown continuously. Pressing the display button a third time will return the readout to Hours-Minutes. This scheme allows all information to be viewed using one push button input and Seconds to be viewed without continually pressing a button. Seconds display in the alternating display mode is described below.

ALTERNATING TIME/DATE DISPLAY

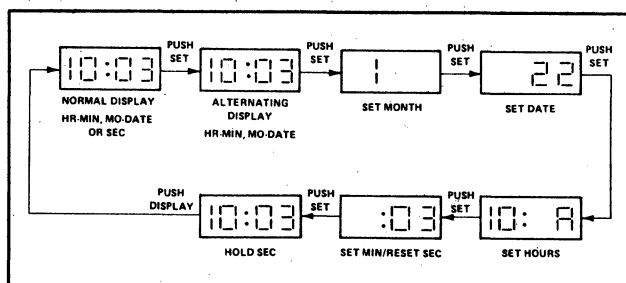
In the alternating display mode, the watch will alternately display Hours-Minutes then Month-Date for two seconds intervals. Pushing the display button will call up seconds. Another push restores the alternating Time/Date display.

SHUTDOWN

A shutdown input (SD) is provided to reduce power consumption of the watch module during storage. When this input is connected to V_{SS} the oscillator is stopped and all other node voltages within the CMOS chip are held constant.

SETTING OPERATION

Five setting states and two normal operating states are included in the setting sequence. Each state is uniquely identified by the display as shown below. Hours, minutes, and seconds are distinguished from month and date by the colon. In the hours set mode the fourth digit is either an A or P to indicate AM or PM.



Only the set input is required to select the desired setting state. Connecting the Set input repeatedly to V_{SS} causes the circuit to advance through its set and run states at the rate of one state per Set switch closure. When the display is in the desired setting state the display button is used to set the displayed quantity. Connecting the display input to V_{SS} causes the selected quantity (month, date, hours or minutes) to be advanced at the rate of one unit per second. In all setting states, timekeeping is not interrupted nor is any counter advanced until the display button is depressed. In all setting states except minutes, only the quantity being displayed can be changed and that change cannot happen until the display button is depressed. In the set minutes state, seconds are reset to zero and held when minutes are advanced. After minutes are set and the display is returned to the run mode, the colon is held on. Seconds counting is resumed from zero by pressing the display button.

SETTING OPERATION

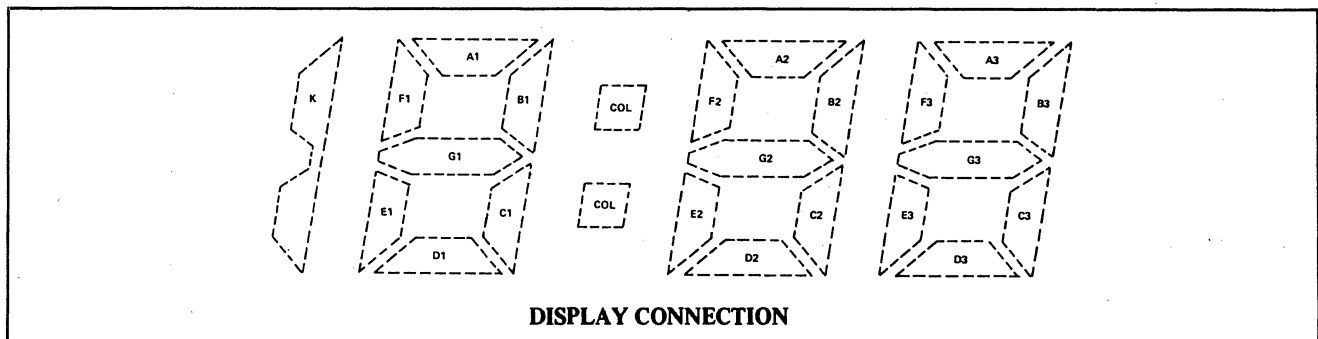
Detailed Procedure

To set the watch, use the following procedure (it is assumed the watch is in the Normal Operating state):

1. Depress the Set button. Circuit will advance to the alternating Time/Date operating mode.
2. Depress the Set button until the display shows Month (shown in left most digits). Release the Set button.
3. Depress the Display button to advance Month to the proper value. Release the Display button.
4. Depress the Set button until the display shows Date (in right most digits). Release the Set button.
5. Depress the Display button to advance Date to the proper value. Release the Display button.
6. Depress the Set button until the display shows Hours (shown in left most digits), and A or P (shown in right most digit). Release the Set button.
7. Depress the Display button to advance Hours to the proper value. Release the Display button.
8. Depress the Set button until the display shows minutes (shown in right most digits) and colon. Release the Set button.
9. Depress the Display button to advance minutes to approximately one minute past the present time. Release the Display button. Depressing the Display button also resets the seconds counter to zero and hold.
10. Depress Set button until the display shows hours and minutes. Release the Set button.
11. When time reaches the start of the minute set in step 9 (showing on display), depress the Display button. The seconds counter is then started and the watch is in normal operation.

FUNCTIONAL DESCRIPTION OF INPUTS/OUTPUTS

SET	- Setting Sequence Advance Button	TST	- High Speed Test Control Input
DISPLAY	- Date, Seconds Display/Counter Advance Button	BP	- 32 Hz Backplane Driver
SD	- Oscillator Shutdown Control	CAP 2, CAP 3	- Voltage Tripler Capacitor Connection
V _L	- Divider Voltage Supply (- 1.5V)	CAP 1, 512	- Voltage Doubler/Tripler Capacitor Connection
V _H	- LCD Driver Voltage Supply (- 4.5V)	OSC _{IN}	- Gate of Oscillator Inverter
V _{SS}	- Most Positive Voltage Supply	OSC _{OUT}	- Output of Oscillator Inverter
		256 Hz	- 256 Hz Upconverter Output*



*Available by special order only after April 1, 1976.

S1424A/S1426A/S1427A
5-FUNCTION LCD WATCH CIRCUIT



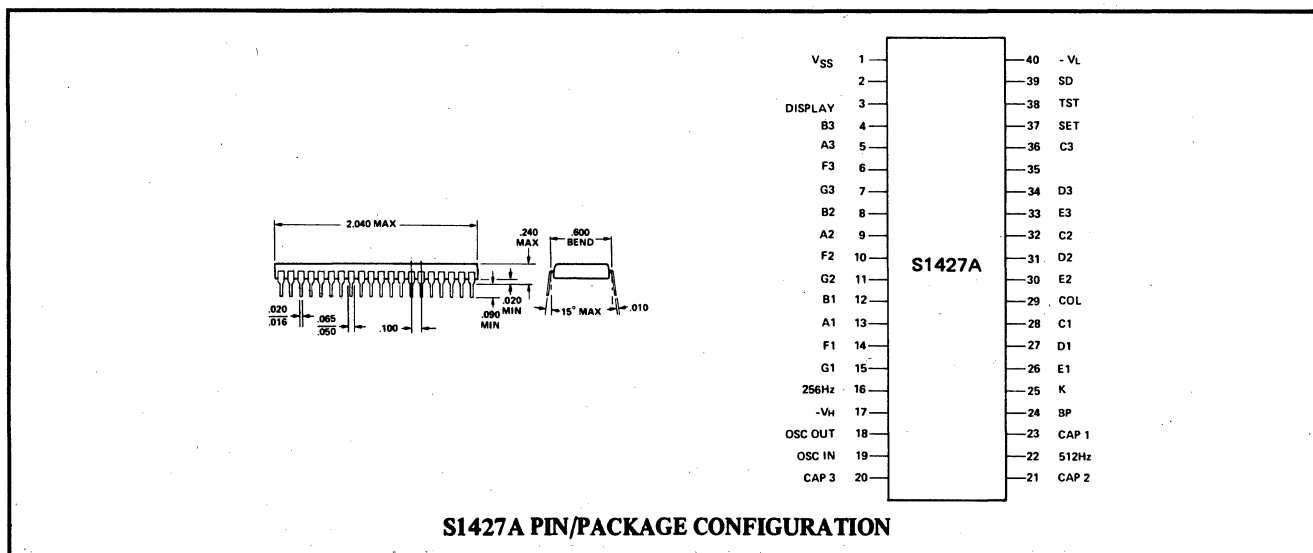
ABSOLUTE MAXIMUM RATINGS

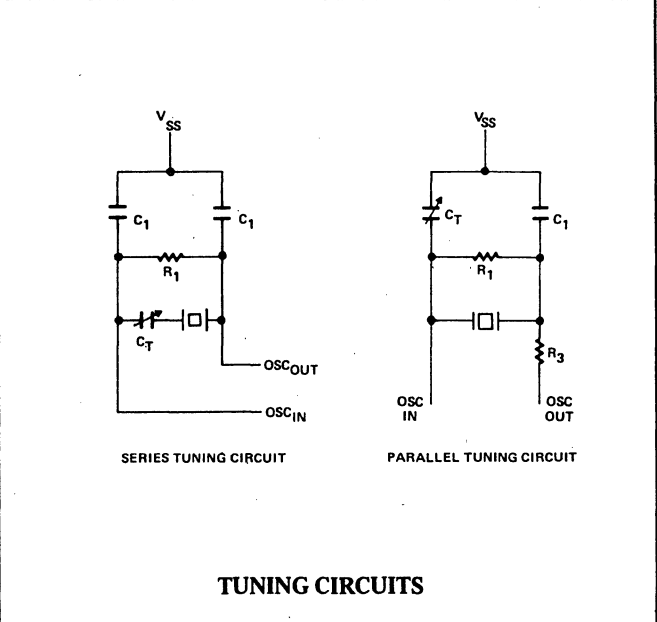
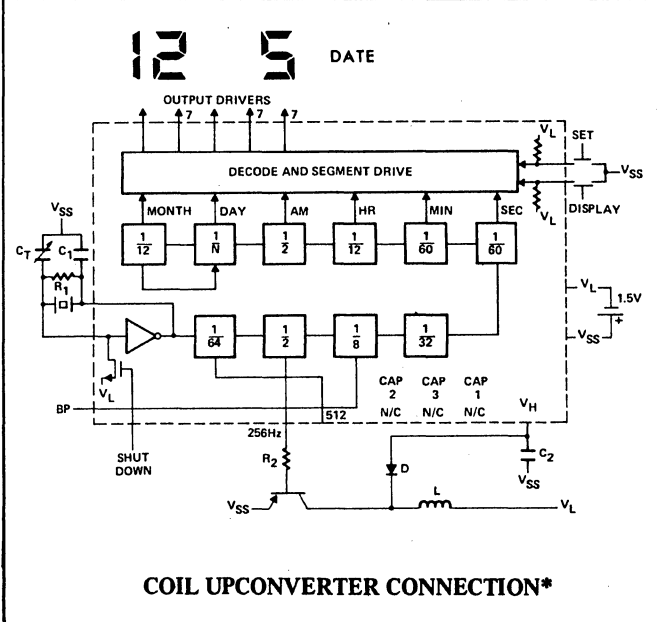
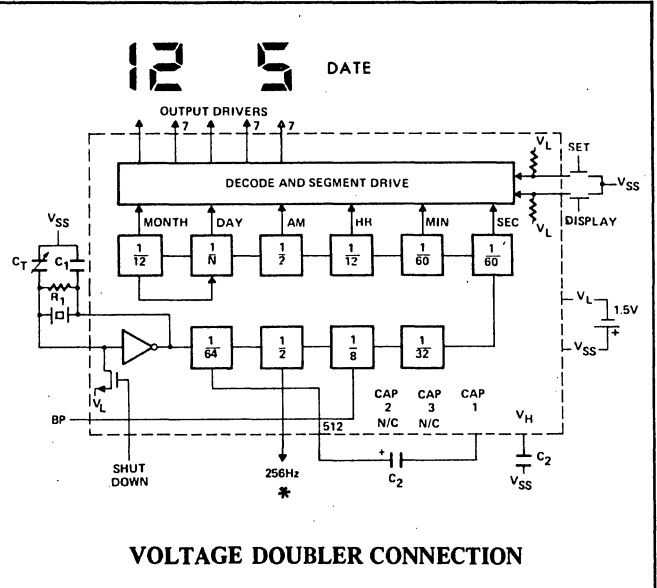
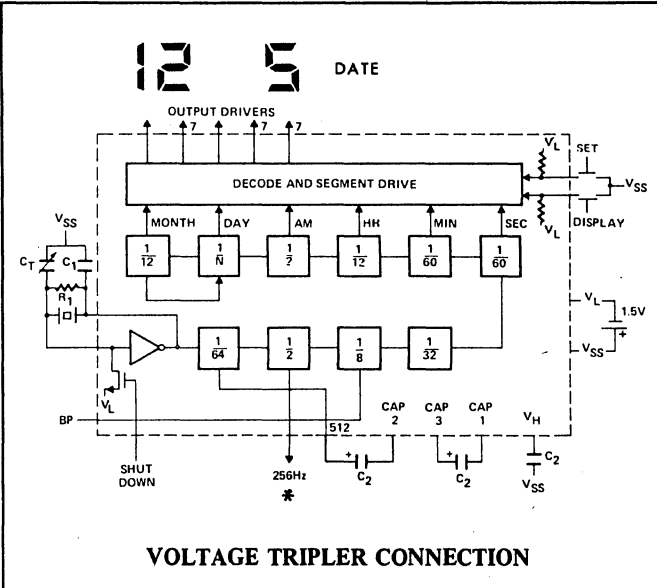
Storage chip temperature	- 55°C to + 150°C	Negative Voltage (on TST, 256 Hz, OSCOUT, OSCIN, 512Hz, DISPLAY, SET, SD)	$V_L - 0.3V$
Operating ambient temperature	- 10°C to + 70°C	Negative Voltage on all other pins	$V_H - 0.3V$
Positive Voltage on any pin	+ 0.3V		

SPECIFICATIONS

($T_A = 25^\circ C$, $V_L = 1.5 \pm 5\%$, $V_H = - 2.9V$ to $- 4.6V$, $V_{SS} = 0V$, FREQ = 32768 Hz)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_S	Starting Voltage	-1.45	-1.1		Volts	
R(SEG)	Segment Resistance Both States		20		Kohm	$I_0 = 10 \mu A$
R(BP)	Back Plate Resistance Both States		6	12	Kohm	$I_0 = 10 \mu A$ to V_H or V_{SS}
R(Pulse)	256 Hz Pulse Resistance to V_L			400	ohm	$I_0 = 10 \mu A$
PW(256)	Pulse Width		15.2		μs	
R _H (512)	512 Hz on Resistance to V_{SS}		5	17	Kohm	$I_0 = 10 \mu A$
R _L (512)	512 Hz on Resistance to V_L			13	Kohm	$I_0 = 10 \mu A$
PW(512)	Pulse Width		976		μs	
I_L	- V_L Supply Current			6.0	μA	
I_H	- V_H Supply Current			1.0	μA	Outputs open ckt
V_H	Display Drive Voltage		4.5	12.0	Volts	$C_2 = .05 \mu F$
I_{IN}	Input Current (Display Set) (Shutdown)			1.0 0.5	μA	Input connected to V_{SS} Input connected to V_{SS}
R _{INOSC IN}	Resistance to V_L		250		K Ω	During Shutdown





C ₁	33 pF
C _T	5 - 50 pF
C ₂	.05μF
R ₁	20 Mohms

R ₂	10K ohms
R ₃	100-300 Kohms
XTAL	32.768 kHz
D	IN914

EXTERNAL COMPONENT LIST

*Available on special order only after April 1, 1976.

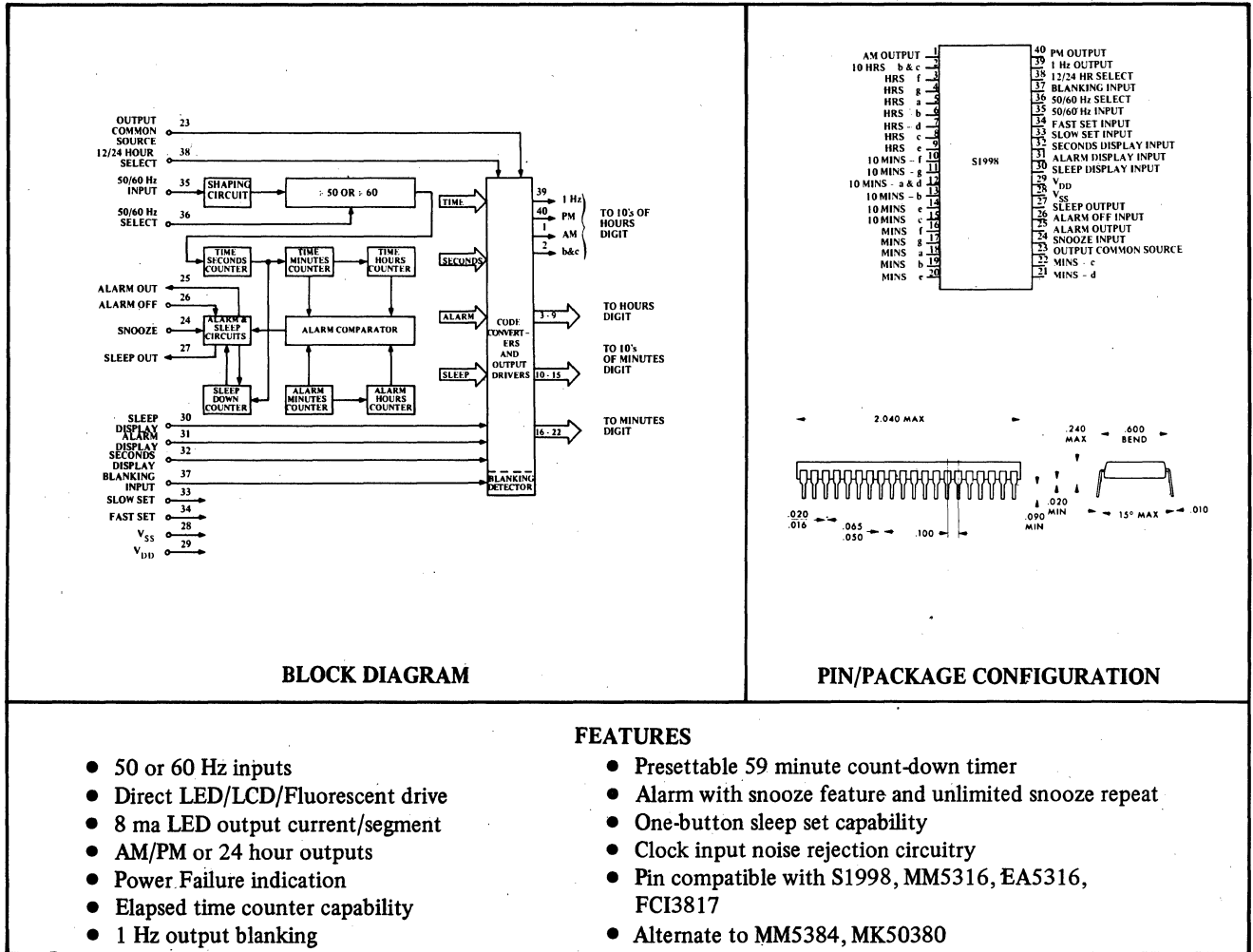
S1998A/B

DIGITAL ALARM CLOCK

AMI

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION



FUNCTIONAL DESCRIPTION

The S1998/B is an improved version of the industry-standard S1998 digital alarm clock radio circuit. The S1998A can be directly substituted for the S1998 in high current, low voltage display applications. (e.g. — LED displays) where the common source line is connected to V_{SS}. For higher voltage displays such as fluorescent or gas discharge, the S1998B should be selected. The circuit interfaces directly with both solid-state and fluorescent/gas discharge displays. The time-keeping function will operate from either a 50 Hz or 60 Hz input, and the display output may be in either 12 hour or 24-hour format.

Clock input noise rejection circuitry eliminates the need for externally filtering the line frequency input. Reset-to-zero circuitry is included for timer/elapsed time applications, and the blanking control allows use of several circuits in parallel with a single display (multiple event timing). The sleep set input can be modified through use of an external diode (Figure 9) to allow one button sleep counter setting.

TYPICAL APPLICATIONS

Alarm Clock, Clock Radio, Industrial Timer, Stop Watch, Photography Timers, Desk Clocks, Appliance Timers, Aircraft Elapsed Time Meters.

FUNCTIONAL DESCRIPTION

A block diagram of the S1998 digital alarm clock is shown on page 1. The various display modes provided by this clock are listed in Table 1. The functions of the setting controls are listed in Table 2. The following discussions are based on the Block Diagram.

50 or 60 Hz Input (pin 35): A shaping circuit is provided to square the 50 or 60 Hz input. This circuit allows use of a filtered sine wave input. A simple RC filter should be used to remove possible line-voltage transients that could either cause the clock to gain time or damage the device. The input should swing between V_{SS} and V_{DD} . The shaper output drives a counter chain which performs the timekeeping function.

50 or 60 Hz Select Input (pin 36): A programmable prescale counter divides the input line frequency by either 50 or 60 to obtain a 1-pps time base. This counter is programmed to divide by 60 simply by leaving pin 36 unconnected; pull-down to V_{DD} is provided by an internal $2.5\text{ M}\Omega$ resistor. Operation at 50 Hz is programmed by connecting pin 36 to V_{SS} .

Display Mode Select Inputs (pins 30 thru 32): In the absence of any of these three inputs, the display drivers present time-of-day information to the appropriate display digits. Internal $2.5\text{ M}\Omega$ pull-down resistors allow use of simple SPST switches to select the display mode. If more than one mode is selected, the priorities are as noted in Table 1. Alternate display modes are selected by applying V_{SS} to the appropriate pin. As shown in the Block Diagram the code converters receive time, seconds, alarm and sleep information from appropriate points in the clock circuitry. The display mode select inputs control the gating of the desired data to the code converter inputs and ultimately (via output drivers) to the display digits.

Time Setting Inputs (pins 33 and 34): Both fast and slow setting inputs are provided. These inputs are applied either singly or in combination to obtain the control functions listed in Table 2. Again, internal $2.5\text{ M}\Omega$ pull-down resistors are provided; application of V_{SS} to these pins effects the control functions. Note that the control functions proper are dependent on the selected display mode. For example, a hold-time control function is obtained by selecting seconds display and actuating the slow set input. As another example, for elapsed time or timer applications, the clock time may be reset to 00:00:00, in the 24-hour format (12:00:00 AM in the 12-hour format), by selecting seconds display and actuating both slow and fast set inputs.

Blanking Control Input (pin 37): Connecting this Schmitt trigger input to V_{DD} places all display drivers in a non-conducting, high-impedance state, thereby inhibiting the display. See Figure 4. Conversely, V_{SS} applied to this input enables the display.

Output Common Source Connection (pin 23): All display output drivers are open-drain devices with all sources common to pin 23 (Figure 4). When using fluorescent tube displays, V_{SS} or a display brightness control voltage is permanently connected to this pin. Since the brightness of a fluorescent tube display is dependent on the anode (segment) voltage, applying a variable voltage to pin 23 results in a display brightness control. This control is shown in Figure 6. However, when using liquid crystal displays, the lifetime of the display device is optimized when AC drive voltages are provided. The common source connection of the S1998 output drivers facilitates generating AC drive voltages. An interface circuit for driving liquid crystal display is shown in Figure 7.

When using low current LED displays the S1998 is connected as shown in Figure 9, to provide direct drive to the display. The 28V supply insures low output on resistance. The resistor provides a voltage drop across output drivers which limits internal power dissipation to less than 1000 mW.

12 or 24 Hour Select Input (pin 38): By leaving this pin unconnected, the outputs for the most-significant display digit (10's of hours) are programmed to provide a 12-hour display format. An internal $2.5\text{ M}\Omega$ pull-down resistor is again provided. Connecting this pin to V_{SS} programs the 24-hour display format. Also, the output connections (pins 1, 2 and 40) are different for each format. Figure 5 illustrates these differences. In addition to displaying 10's of hours, this digit provides an AM/PM indication (12-hour format only) and the power failure indication. In the 12-hour format, AM indication is provided by segment "f"; PM indication by segment "e." The power failure indication consists of a flashing of the AM or PM indicator at a 1-Hz rate. A fast or slow set input resets an internal power failure latch and returns the display to normal. In the 24-hour format, the power failure indication consists of flashing segments "a", "d", "e", "g" of the HR x 10 digit.

FUNCTIONAL DESCRIPTION (Con't.)

Alarm Operation and Output (pin 25): The alarm comparator (Figure 1) senses coincidence between the alarm counter (the alarm setting) and the time counters (real time). The comparator output is used to set a latch in the alarm and sleep circuits. The latch output enables the alarm output driver (Figure 4), the S1998 output that is used to control the external alarm sound generator. The alarm latch remains set for 59 minutes during which the alarm will sound if the latch output is not temporarily inhibited by another latch set by the snooze alarm input (pin 24) or reset by the alarm off input (pin 26).

Snooze Alarm Input (pin 24): Momentarily connecting pin 24 to V_{SS} inhibits the alarm output for between 8 and 9 minutes, after which the alarm will again be sounded. This input is pulled-down to V_{DD} by an internal 2.5 M Ω resistor. The snooze alarm feature may be repeatedly used during the period in which the alarm latch remains set.

Alarm Off Input (pin 26): Momentarily connecting pin 26 to V_{SS} resets the alarm latch and thereby silences the alarm. This

input is also returned to V_{DD} by an internal 2.5 M Ω resistor. The momentary alarm off input also readies the alarm latch for the next comparator output, and the alarm will automatically sound again in 24 hours (or at a new alarm setting). If it is desired to silence the alarm for a day or more, the alarm off input should remain at V_{SS} .

Sleep Timer and Output (pin 27): The sleep output at pin 27 can be used to turn off a radio after a desired time interval of up to 59 minutes. The time interval is chosen by selecting the sleep display mode (Table 1) and setting the desired time interval (Table 2). This automatically results in a current-source output via pin 27, which can be used to turn on a radio (or other appliance). When the sleep counter, which counts downwards, reaches 00 minutes, a latch is reset and the sleep output current drive is removed, thereby turning off the radio. This turn-off may also be manually controlled (at any time in the countdown) by a momentary V_{SS} connection to the snooze input (pin 24). The output circuitry is the same as the other outputs (Figure 4).

TABLE 1. S1998 Display Modes

*SELECTED DISPLAY MODE	DIGIT NO. 1	DIGIT NO. 2	DIGIT NO. 3	DIGIT NO. 4
Time Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Seconds Display	Blanked	Minutes	10's of Seconds	Seconds
Alarm Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Sleep Display	Blanked	Blanked	10's of Minutes	Minutes

*If more than one display mode input is applied, the display priorities are in the order of Sleep (overrides all others), Alarm, Seconds, Time (no other mode selected).

TABLE 2. S1998 Setting Control Functions

SELECTED DISPLAY MODE	CONTROL INPUT	CONTROL FUNCTION
*Time	Slow	Minutes Advance at 2 Hz Rate
	Fast	Minutes Advance at 60 Hz Rate
	Both	Minutes Advance at 60 Hz Rate
Alarm	Slow	Alarm Minutes Advance at 2 Hz Rate
	Fast	Alarm Minutes Advance at 60 Hz Rate
	Both	Alarm Resets to 12:00 AM (12-hour format)
	Both	Alarm Resets to 12:00 (24-hour format)
Seconds	Slow	Input to Entire Time Counter is Inhibited (Hold)
	Fast	Seconds and 10's of Seconds Reset to Zero Without a Carry to Minutes
	Both	Time Resets to 12:00:00 AM (12-hour format)
	Both	Time Resets to 00:00:00 (24-hour format)
Sleep	Slow	Subtracts Count at 2 Hz
	Fast	Subtracts Count at 60 Hz
	Both	Subtracts Count at 60 Hz

*When setting time sleep minutes will decrement at rate of time counter, until the sleep counter reaches 00 minutes (sleep counter will not recycle).

ABSOLUTE MAXIMUM RATINGS

Positive Voltage on any Pin	$V_{SS} + 0.3V$	Storage and Operating Chip Temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Negative Voltage on any Pin	$V_{SS} - 30V$	Operating Ambient Temperature	$0^{\circ}C$ to $+70^{\circ}C$

STATIC CHARACTERISTICS

($T_A = 25^{\circ}C$, $V_{SS} = +26V$, $V_{DD} = GROUND$)

	Min.	Typ.	Max.	Units	Conditions
I _{SS} Power Supply Current:		2	5	mA	$V_{SS} = +8V$ no output loads $V_{SS} = +26V$
		3	10	mA	
50/60 Hz Input:					
Frequency	DC	50 or 60	10K	Hz	
Voltage					
V _{IH} Logical High Level	$V_{SS} - 1$		V_{SS}	V	Internal 2.5 M Ω on all inputs except CLOCK
V _{IL} Logical Low Level	V_{DD}		$V_{DD} + 1$	V	
Power Failure Detect Voltage:	+8.5		+13.5	V	(V_{SS} Voltage)
Output Currents:					$V_{SS} = +21$ to $+26V$, $V_{DD} = 0V$
1Hz Display					
I _{OH} Logical High Level	24			mA	$V_{OH} = V_{SS} - 4V$
I _{OL} Logical Low Level			1	μA	$V_{OL} = V_{DD}$
10's of Hours (b & c), 10's of Minutes (a & d)					
I _{OH} Logical High Level	16			mA	$V_{OH} = V_{SS} - 4V$
I _{OL} Logical Low Level			1	μA	$V_{OL} = V_{DD}$
All Other Display					
I _{OH} Logical High Level	8			mA	$V_{OH} = V_{SS} - 4V$
I _{OL} Logical Low Level			1	μA	$V_{OL} = V_{DD}$
I _{OH} Alarm, Sleep	500			μA	$V_{OH} = V_{SS} - 2V$

FIGURE 4. OUTPUT CIRCUITS

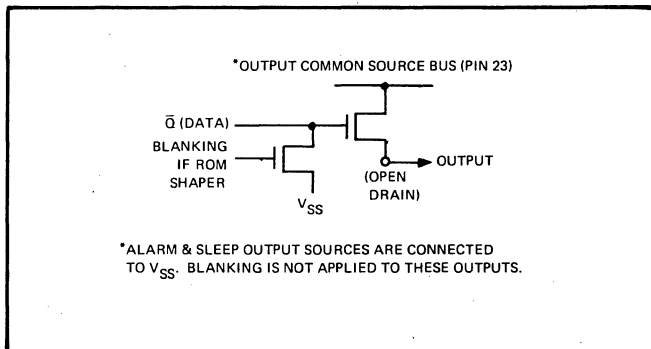


FIGURE 5. WIRING TEN'S OF-HOURS DIGIT

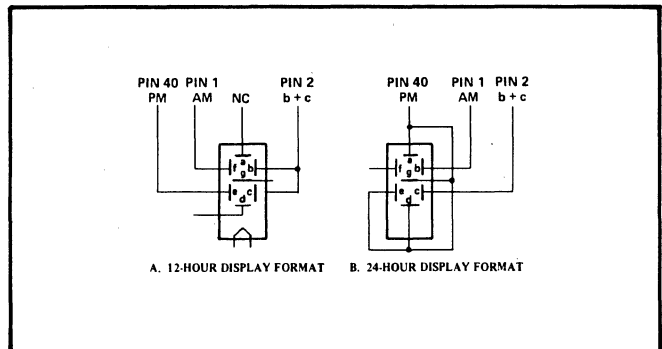


FIGURE 6. TUBE DISPLAY CLOCK

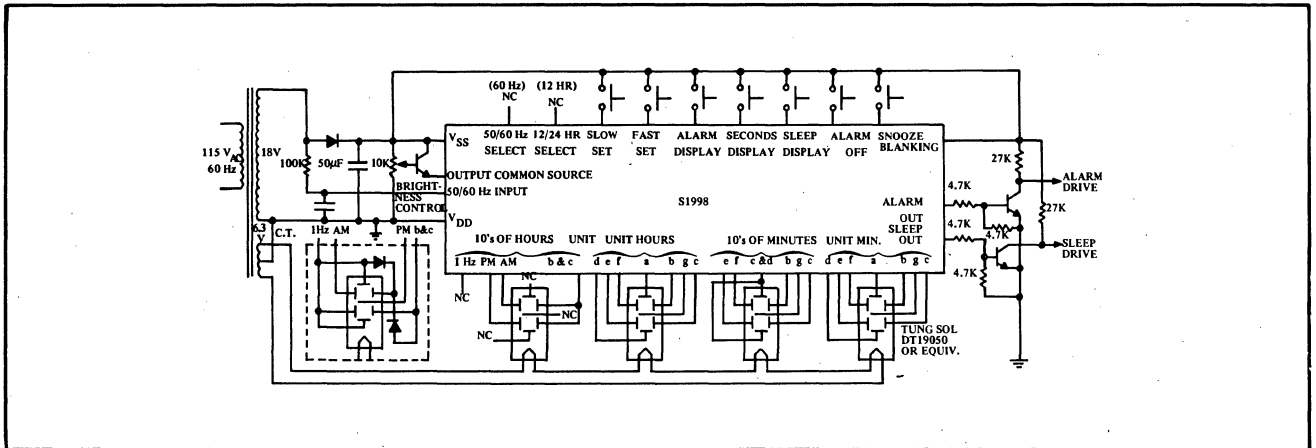


FIGURE 7 LCD DISPLAY CLOCK

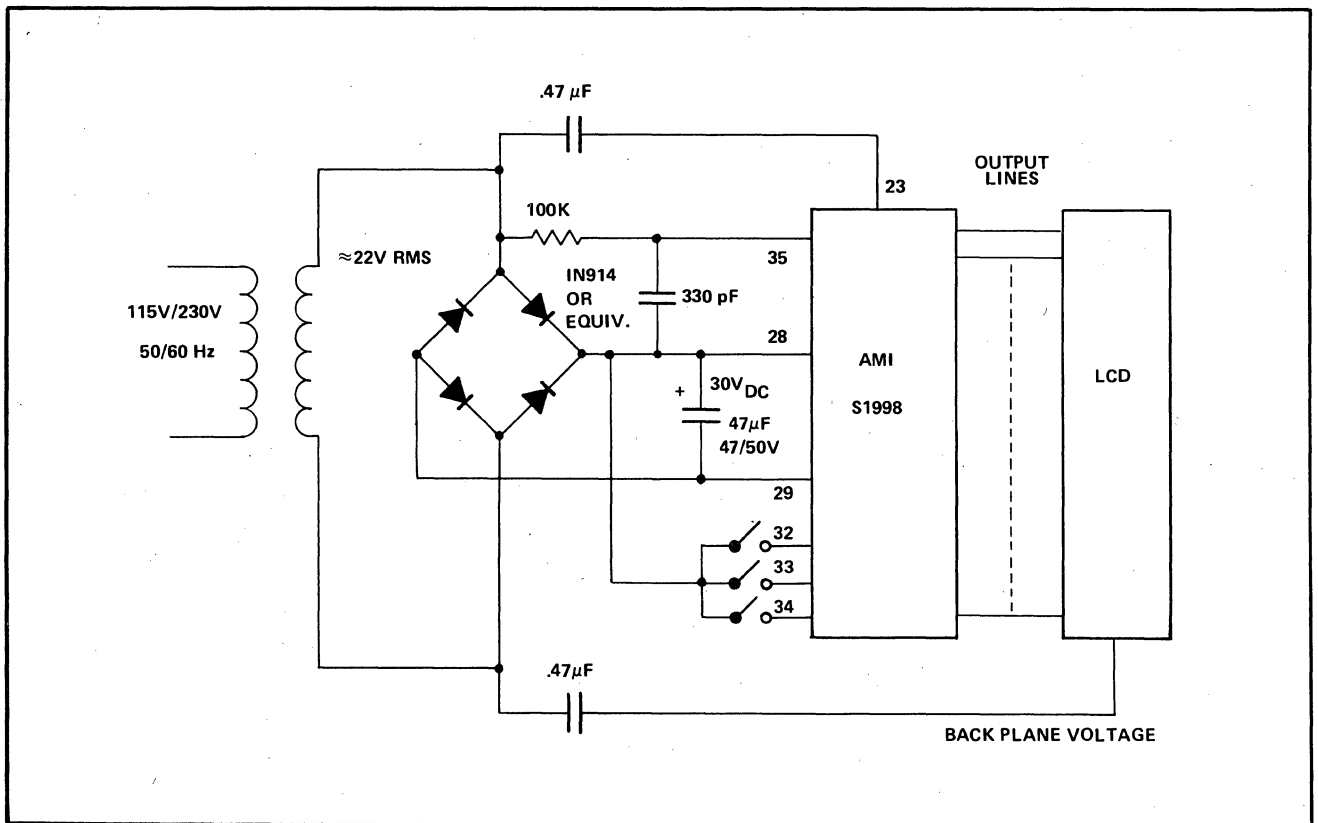


FIGURE 8. GAS DISCHARGE CLOCK (with "keep alive" voltage regulator)

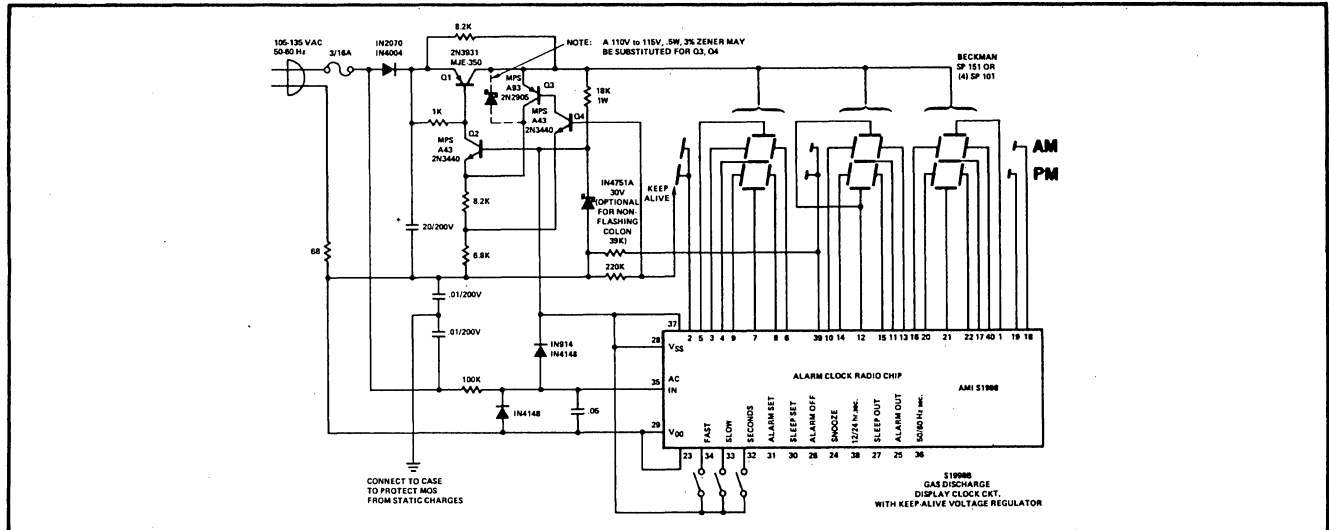
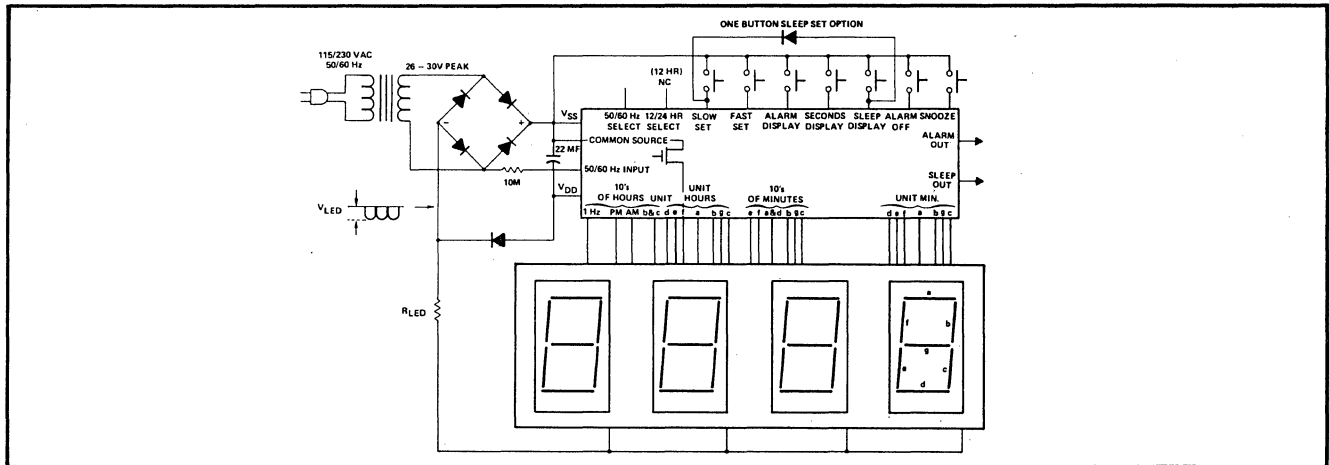


FIGURE 9. LED CLOCK (Common Cathode Design)



OPERATING CONDITIONS

Common Source (Pin 23):
LED Voltage Supply:
(V_{LED}) LED Power Supply Voltage Peak:
LED Segment Voltage:

Temperature:
R_{LED}: (1)

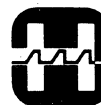
Connect to V_{SS} (Pin 28)
Full Wave Rectified Sine Wave (Pulsating)
30 Volts Max.
-20 Volts DC Min.
-30 Volts DC Max.
65 Degrees C Max.
To be determined

DEVICE CHARACTERISTICS

S1998A Segment Current:⁽²⁾
Power Dissipation:
Output on resistance

(22 Segments on) 8.0 mA Min. at V_{LED} = 22 Volts peak
1000 Milliwatts Max. @ 40°C and -30V
300 ohms at V_{DD} = 20V

- NOTES: 1. (R_{LED}) resistor connected between LED cathodes and LED full wave rectified voltage supply. R_{LED} limits power on chip to 1000 mW.
2. S1998B current is limited to 2.8 ma.



HARRIS is **BIG** in CMOS

All three major series...54C/74C, 4000, and 14500

Total availability in CMOS... more than 100 circuit-types, with more being added. Count on Harris to produce and deliver — any volume — at competitive prices.

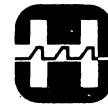
Harris now offers commercial devices in both CERDIP and Epoxy 410-B., rated for -40°C to 85°C. And high-rel versions—CERDIP and Flat-Pack for -55°C to 125°C. All devices available in chip form as well.

Immediate delivery of both families from these major distributors, Schweber, Hamilton/Avnet, R. V. Weatherford and Harvey Electronics.

In the following pages we feature complex MSI from both 54C/74C and 4000 Series, representative of our capability in CMOS.

FUNCTIONAL INDEX

Description	Device No.	Package Code	Page No.	Description	Device No.	Package Code	Page No.
ARITHMETIC FUNCTIONS				DECODERS/MULTIPLEXERS			
4-Bit Full Adder	HD-4008A	-	-	BCD to Decimal Decoder	HD-4028A	1W, 9L	271
4-Bit Binary Full Adder	HD-74C83*	1W, 9L	274	Single 8-Channel Multiplexer	HD-4051A	-	-
4-Bit Magnitude Comparator	HD-74C85*	1W, 9L	275	Differential 4-Channel Multiplexer	HD-4052A	-	-
COUNTERS				Triple 2-Channel Multiplexer	HD-4053A	-	-
Decade Counter/Divider	HD-4017A	-	-	Quad Bilateral Switch	HD-4066A	-	-
Presetable Divide-by-"N" Counter	HD-4018A	1U, 9V	269	BCD to Decimal Decoder	HD-74C42*	1W, 9L	274
14-Stage Binary/Ripple Counter	HD-4020A	1W, 9L	270	BCD to 7-Segment Decoder	HD-74C48*	-	-
Divide-by-8 Counter/Divider with 8 Decoded Outputs	HD-4022A	1W, 9L	271	8-Channel Digital Multiplexer	HD-74C151*	1W, 9L	276
7-Stage Binary/Ripple Counter	HD-4024A	-	-	4-Line to 16-Line Decoder/Demultiplexer	HD-74C154*	1U, 9V	276
Presetable Up/Down Counter	HD-4029A	1W, 9L	272	Quad 2-Input Multiplexer	HD-74C157*	-	-
12-Bit Binary Counter	HD-4040A	-	-	8-Channel Data Selector	HD-14512	-	-
Synchronous Decade	HD-74C160*	1W, 9L	277	Dual 4-Channel Analog Data Selector	HD-14529	-	-
Synchronous Binary	HD-74C161*	1W, 9L	277	FLIP-FLOPS			
Fully Synchronous Decade	HD-74C162*	1W, 9L	277	Dual "D" with Set/Reset	HD-4013A	-	-
Synchronous Up/Down Decade	HD-74C192*	1W, 9L	278	Dual J-K with Set/Reset	HD-4027A	-	-
Synchronous Up/Down Binary	HD-74C193*	1W, 9L	278	Quad Clocked "D" Latch	HD-4042A	-	-
4-Bit Counter/7-Segment Output	HD-74C925*	-	-	Quad Three State NOR Reset/Set Latch	HD-4043A	-	-
BCD Up/Down Counter	HD-14510	-	-	Quad Three State NAND Reset/Set Latch	HD-4044A	-	-
Binary Up/Down Counter	HD-14516	-	-	Dual "J-K" Master/Slave	HD-74C73	-	-
Dual BCD Up Counter	HD-14518	-	-	Dual "D" with Set/Reset	HD-74C74	-	-
Dual Binary Up Counter	HD-14520	-	-	Dual "J-K" Master/Slave Preset	HD-74C76	-	-
GATES/BUFFERS				Dual "J-K" (Quad Latch)	HD-74C173	-	-
Dual 3-Input NOR Gate	HD-4000A	-	-	Hex "D"	HD-74C174	-	-
Quad 2-Input NOR Gate	HD-4001A	-	-	Quad "D"	HD-74C175	-	-
Dual 4-Input NOR Gate	HD-4002A	-	-	SHIFT REGISTERS			
Dual Complementary Pair with Inverter	HD-4007A	-	-	18-Stage Static	HD-4006A	-	-
Quad 2-Input NAND Gate	HD-4011A	-	-	8 Stage Synchronous Parallel Input/Serial Output	HD-4014A	1W, 9L	268
Dual 4-Input NAND Gate	HD-4012A	-	-	Dual 4 Stage with Serial Input/Parallel Output	HD-4015A	1W, 9L	269
Quad AND/OR Select	HD-4019A	1W, 9L	270	8 Stage Asynchronous Parallel Input/Serial Output	HD-4021A	1W, 9L	270
Triple 3-Input NAND	HD-4023A	-	-	4 Stage with J-K Input and True/Complement Output	HD-4035A	1U, 9V	273
Triple 3-Input NOR	HD-4024A	-	-	4 Bit Right-Shift Left-Shift	HD-74C95*	1U, 9V	276
Quad 2-Input Exclusive OR	HD-4030A	1U, 9V	273	8 Bit Serial-In Parallel Out	HD-74C164*	1U, 9V	277
Hex Buffer/Converter, Inverting	HD-4049A	-	-	8 Stage Synchronous Parallel Input/Serial Output	HD-74C165*	1W, 9L	278
Hex Buffer/Converter, Non-Inverting	HD-4050A	-	-	4-Bit Parallel-In Parallel-Out	HD-74C195*	1W, 9L	279
Quad 2 Input NAND	HD-74C00*	-	-	12-Bit Successive Approximation Register	HD-74C905*	-	-
Quad 2 Input NOR	HD-74C02*	-	-	SPECIAL FUNCTION			
Hex Inverter	HD-74C04*	-	-	Hex Schmitt Trigger	HD-74C14*	-	-
Quad 2 Input AND	HD-74C08*	-	-	Quad Single-Ended Line Driver	HD-88C29	-	-
Triple 3 Input AND	HD-74C10*	-	-	Dual Differential Line Driver	HD-88C30	-	-
Dual 4 Input NAND	HD-74C20*	-	-	64 Bit Three State RAM	HD-74C89*	1W, 9L	275
8 Input NAND	HD-74C30*	-	-	256 Bit Three State RAM	HD-74C00*	1U, 9V	279
Quad 2 Input OR	HD-74C32*	-	-	Dual Monostable Multivibrator	HD-74C221*	1W, 9L	280
Quad 2 Input Exclusive OR	HD-74C86*	-	-	Hi-Voltage Driver	HD-74C908*	-	-
Three State Hex Buffer	HD-80C95**	-	-	Quad Comparator	HD-74C909*	-	-
Three State Hex Inverting Buffer	HD-80C96**	-	-	16-Key Keyboard Encoder	HD-74C922*	-	-
Three State Hex Buffer	HD-80C97**	-	-	20-Key Keyboard Encoder	HD-74C923*	-	-
Three State Hex Inverting Buffer	HD-80C98**	-	-	BCD to 7-Segment Latch/Decoder/Driver	HD-14511	-	-
Hex Buffer/Converter, Inverting	HD-74C901*	-	-	BCD Rate Multiplier	HD-14527	-	-
Hex Buffer/Converter, Non-Inverting	HD-74C902*	-	-	Dual One Shot	HD-14528	-	-
Hex Inverting PMOS Buffer	HD-74C903*	-	-	*All Listed 74C Devices Are Also Available As 54C.			
Hex Open Drain N-Channel Buffer	HD 74C906*	-	-	**All Listed 80C Devices Are Also Available As 70C.			
Hex Open Drain P-Channel Buffer	HD-74C907*	-	-				
4-Bit AND/OR Selector	HD-14519	-	-				



Family Features

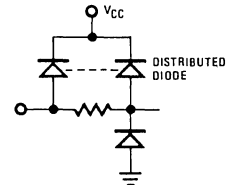
These circuits employ complementary MOS (CMOS) to achieve low power dissipation, high noise immunity and wide power supply voltage ranges with symmetric rise and fall times. Features such as these make the 4000 and 54C/74C families ideal for use in digital systems.

The 4000 series is popular because of the wide range of logic functions and readily abundant supply.

The 54C/74C series is ideal for "worse case" noise immunity design. Function and pin out compatibility with 54/74 TTL devices minimizes design time for those designers already familiar with that logic family.

- Wide Supply Voltage Range 3.0V to 15V
- Guaranteed Noise Margin 1.0V
- High Noise Immunity 0.45 V_{CC} Typ.
- Low Power 10nW Typ. for Gates
10 μW Typ. for MSI Circuits

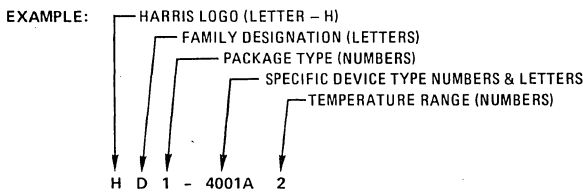
- All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND unless otherwise noted.



CMOS Product Code

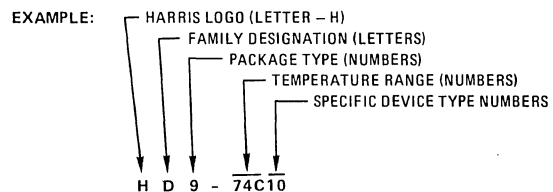
Harris CMOS Products are designated by "PRODUCT CODE". When ordering, please refer to products by the full code. Harris Products will always begin with "H". Specific device numbers will always be isolated by hyphens.

4000 SERIES



FAMILY (LETTERS)	PACKAGE (NUMBERS)	TEMPERATURE RANGE
D - DIGITAL	1 - DUAL IN-LINE CERAMIC 9 - FLAT PACKAGE	2 - -55°C to +125°C 9 - -40°C to +85°C

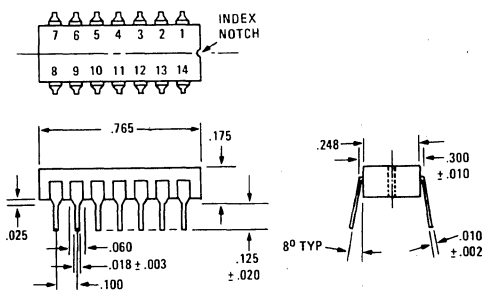
54C/74C SERIES



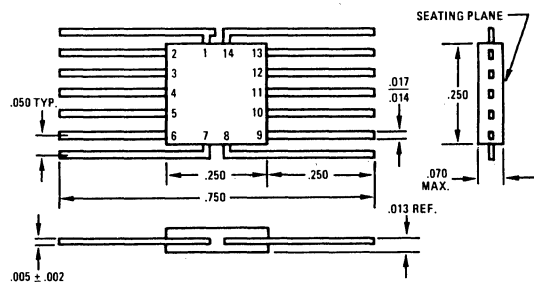
FAMILY (LETTERS)	PACKAGE (NUMBERS)	TEMPERATURE RANGE
D - DIGITAL	1 - DUAL IN-LINE CERAMIC 9 - FLAT PACKAGE	54C - -55°C to +125°C 74C - 0°C to +70°C

Packaging Code

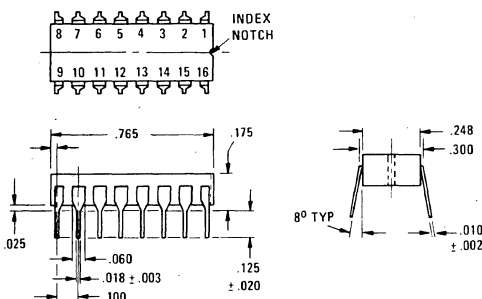
Code 1U 14 LEAD CERAMIC D.I.P. (CERDIP) *



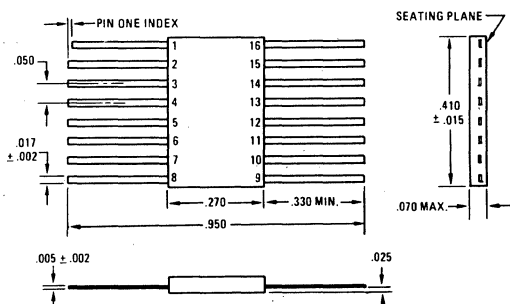
Code 9V TO-86 (METAL BOTTOM) BRAZED SEAL FLAT PACK *



Code 1W 16 LEAD CERAMIC D.I.P. (CERDIP) *



Code 9L 16 LEAD BRAZED SEAL FLAT PACK *



HD-4000A Series

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range, $V_{DD} - V_{SS}$
 Voltage at any Pin
 Storage Temperature Range
 Power Dissipation per Package
 Operating Temperature Range: HD-4000A-2
 HD-4000A-9

-0.5VDC to +15VDC
 $V_{SS} - 0.3VDC \leq V_{pin} \leq V_{DD} + 0.3VDC$
 -65°C to +150°C
 200mW
 -55°C to +125°C
 -40°C to +85°C

HD-4014A 8-Stage Static Shift Register

Description

- CLOCK RATE 5MHz (TYP.) $V_{DD} - V_{SS} = 10V$

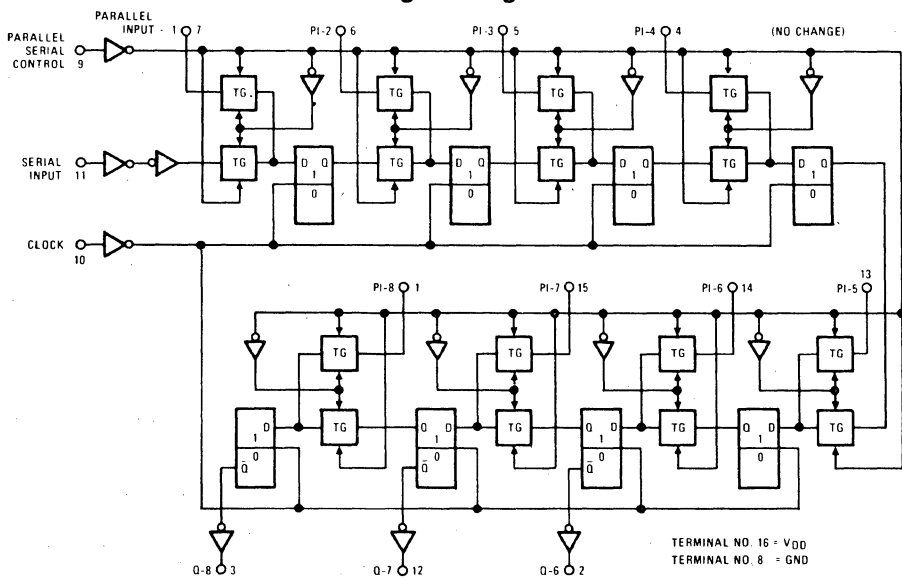
The HD-4014 is an 8 stage shift register with parallel or serial data input and serial data output capabilities.

The state of the parallel/serial input determines the data entry mode. With a high on the parallel/serial control, input data is loaded from the parallel inputs synchronous with the

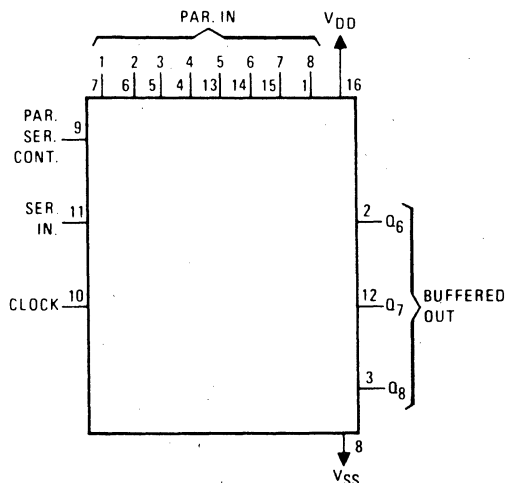
positive going clock input. A low on the parallel/serial control enables serial data entry synchronous with the positive going clock.

Parallel operation of two or more HD-4014's allows bit expansion beyond eight bits.

Logic Diagram



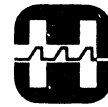
Connection Diagram



Truth Table

$C_L \Delta$	SER. IN	PAR. SER. CONTROL	PI-1	PI-n	Q_1 (INTERNAL)	Q_n
/	X	1	0	0	0	0
/	X	1	1	0	1	0
/	X	1	0	1	0	1
/	X	1	1	1	1	1
/	0	0	X	X	0	Q_{n-1}
/	1	0	X	X	1	Q_{n-1}
/	X	X	X	X	Q_1	Q_n

X = DON'T CARE CASE Δ = LEVEL CHANGE



HD-4015A Dual 4-Stage Static Shift Register

Description

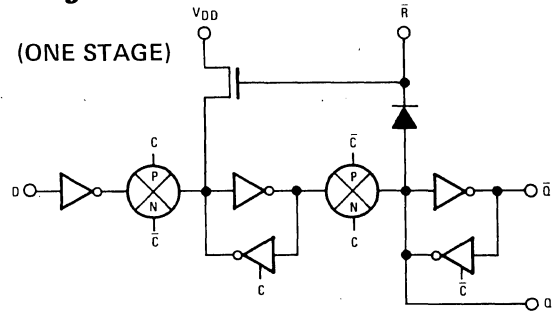
● CLOCK RATE 5 MHz (TYP.) $V_{DD} - V_{SS} = 10V$

The HD-4015 is a dual 4 stage static shift register. Both four bit segments are capable of independent operation. With an independent serial "Data", "Clock", and "Reset", input and "Q" output available from each stage.

Resetting either four bit segment occurs when its respective reset line is held at a high level. Data shifting occurs on the positive-going clock transition.

The shift register function provided by the HD-4015 can easily be expanded in multiples of four stages by paralleling additional units as required.

Circuit Diagram

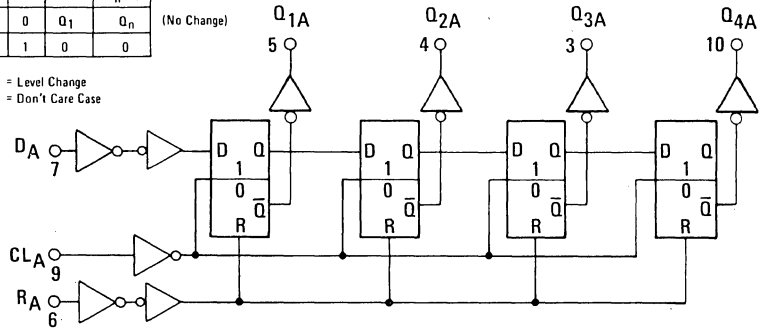


Block Diagram

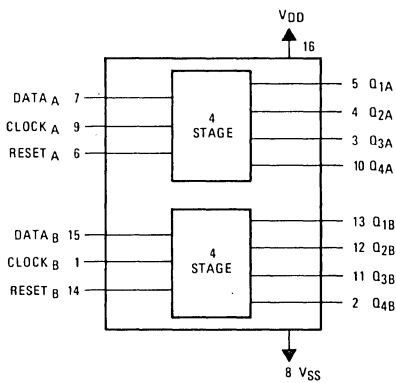
CL [▲]	D	R	Q ₁	Q _n
	0	0	0	Q _{n-1}
	1	0	1	Q _{n-1}
	X	0	Q ₁	Q _n
	X	X	1	0

(No Change)

▲ = Level Change
X = Don't Care Case



Connections



HD-4018A Presetable Divide-By-'N' Counter

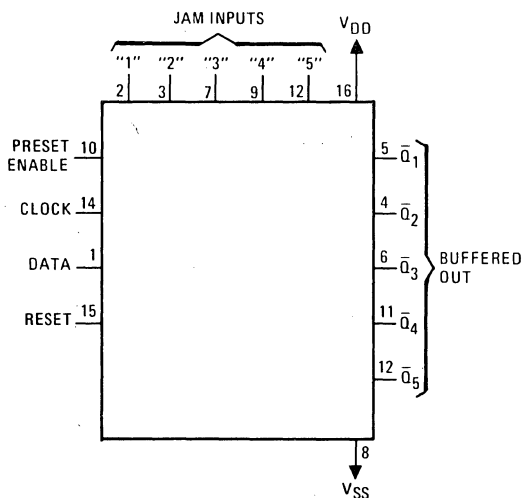
Description

The HD-4018 is a 5-bit Johnson counter incorporating reset and load capabilities. Fixed and programmable frequency division can be implemented by hard wiring or gating feedback to the data input. Divide by 10, 8, 6, 4, and 2 result from feedback of Q₅, Q₄, Q₃, Q₂ and Q₁ to the data input. Proper gating of feedback results in division by 9, 7, 5, or 3.

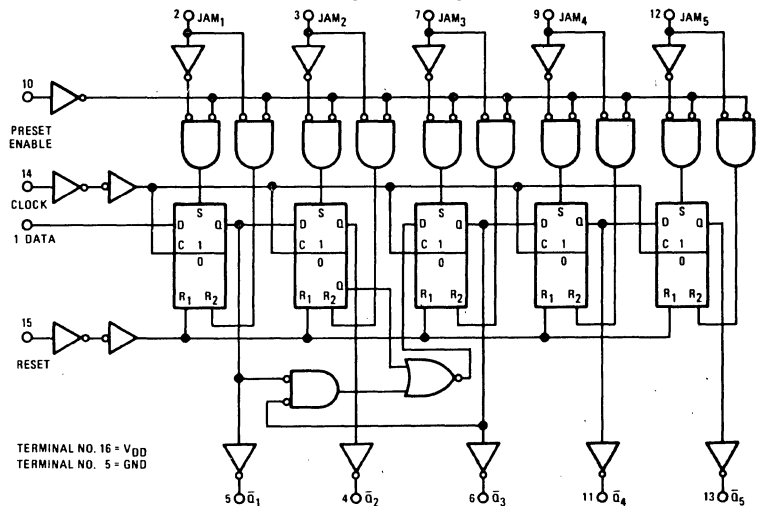
Division by numbers greater than 10 can be performed by using two or more HD-4018's.

Application of a "high" to the reset input clears the counter to the "zero" state. When the preset enable input is held high, data applied to the Jam inputs is loaded into the counter asynchronously with the clock. The counter increments synchronously with the positive-going clock transition.

Connections

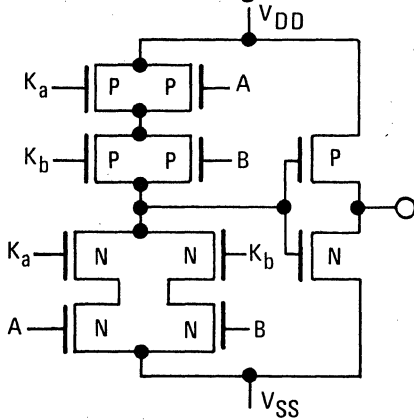


Logic Diagram

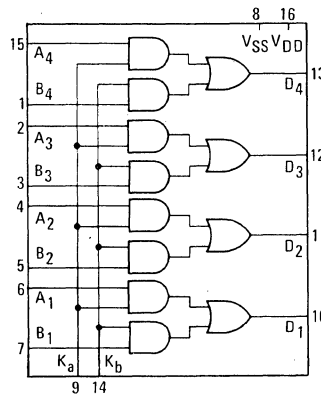


HD-4019A Quad AND-OR Select Gate

Circuit Diagram



Connections



Truth Table

CONTROL		OUTPUT
K_a	K_b	D_1
0	0	0
0	1	B_1
1	0	A_1
1	1	$A_1 + B_1$

LOGIC "1" → V_{DD}

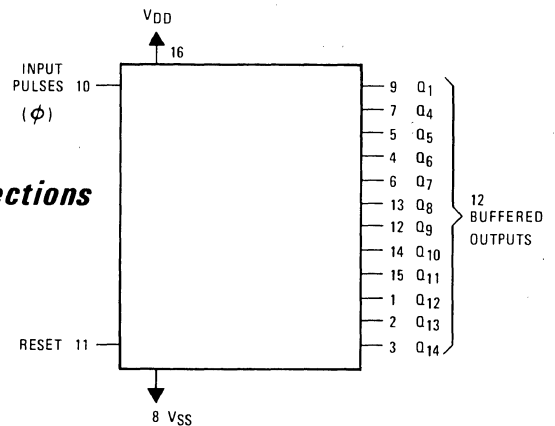
LOGIC "0" → V_{SS}

HD-4020A 14-Stage Ripple-Carry Binary Counter/Divider

Description

The HD-4020 is a 14 stage ripple-carry binary counter/divider. Buffered outputs are available from stage 1, and stages 4 through 14. The counter increments on the negative going edge of the input pulse. Resetting of the counter to the "zero" state occurs when a "high" is applied to the reset input.

Connections



HD-4021A 8-Stage Static Shift Register

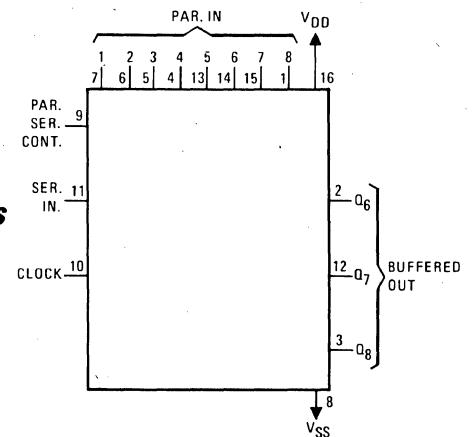
Description

The HD-4021 is an 8-stage parallel or serial input/serial output shift register. Inputs are provided for clock, parallel/serial control, serial data, and parallel data (8 inputs). "Q" outputs for the sixth, seventh, and eighth stages are also available.

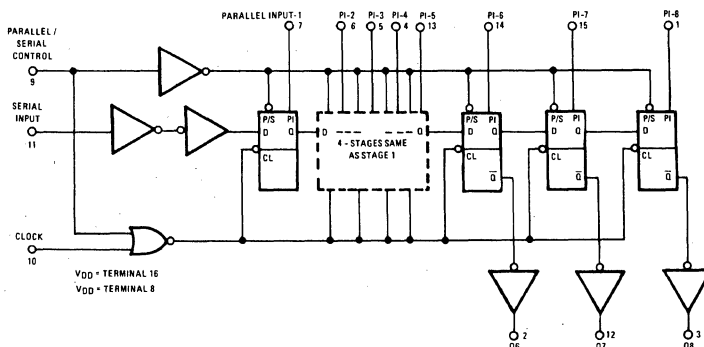
With the parallel/serial control high data is jammed into the register via the parallel input lines. With the parallel/serial input low data is shifted synchronously during the positive going clock.

The HD-4021 register function can be easily expanded in multiples of eight stages by paralleling additional units as required.

Connections



Logic Diagram

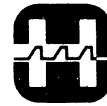


Truth Table

C_L	SERIAL INPUT	PARALLEL/SERIAL CONTROL	$PI-1$	$PI-n$	Q_1 (INTERNAL)	Q_n
X	X	1	0	0	0	0
X	X	1	0	1	0	1
X	X	1	1	0	1	0
X	X	1	1	1	1	1
↕	0	0	X	X	0	Q_{n-1}
↕	1	0	X	X	1	Q_{n-1}
↕	X	0	X	X	Q_1	Q_n

NO CHANGE

▲ = LEVEL CHANGE X = DON'T CARE CASE



HD-4022A Divide-By-8 Counter/Divider with 8 Decoded Outputs

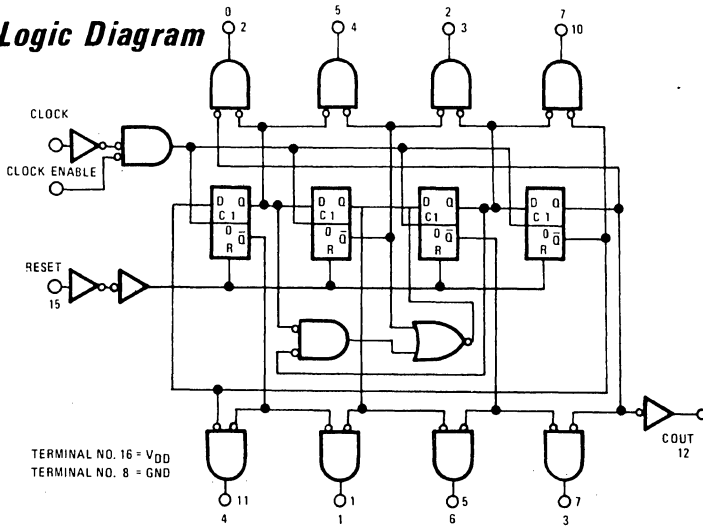
Description

The HD-4022 is a 4-stage Johnson counter with decoded outputs. The counter outputs internally drive the inputs of a one of eight decoder, with the decoder outputs available at the package pins. Buffered clock and reset pins are provided for maximization of circuit noise immunity and reduction of input capacitance. A clock enable pin is also available. The counter advances on the positive going clock signal if clock enable is low.

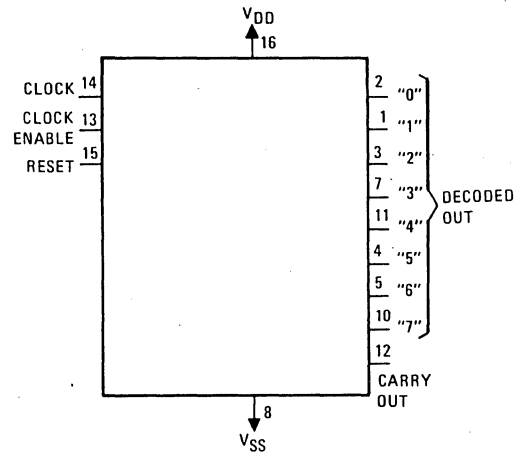
The Johnson counter configuration permits high speed spike-free operation with all counter stages clocking in parallel.

The normal state of an undecoded output is low, going high for one complete clock cycle when decoded. The carry-out signal goes high every 8 clock cycles, and can be used as a ripply carry input if two or more counters are used in parallel.

Logic Diagram



Connections

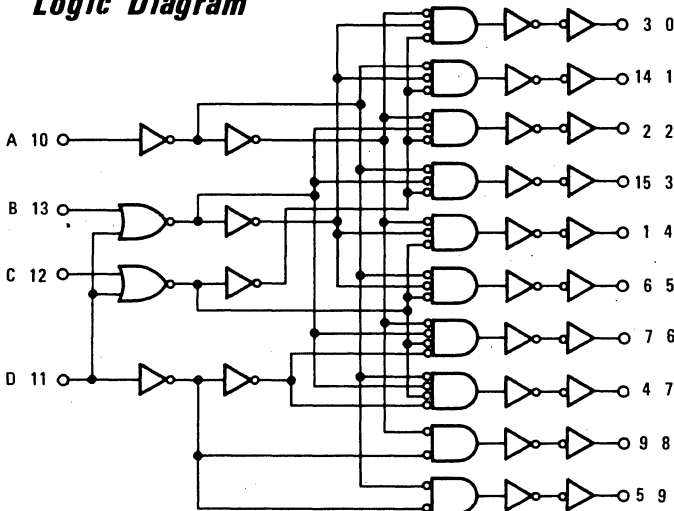


HD-4028A BCD-to-Decimal Decoder

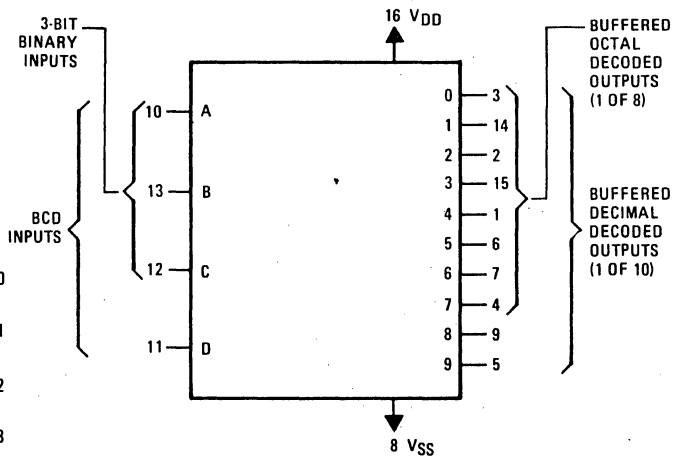
Description

The HD-4028 is a BCD - decimal decoder or binary to octal decoder. Application of BCD at inputs A, B, C, and D will result in 1 of 10 outputs being decoded as defined in the truth table. Octal code will be decoded at outputs 0 to 7 with a 3-bit binary code applied to inputs A, B, and C and input D held "low". An output, when decoded, will be "high" with all other outputs "low".

Logic Diagram



Connections



Truth Table

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1

Where: 1 = High Level
0 = Low Level

HD-4029A Presettable Up/Down Counter

Description

The HD-4029 is a four stage counter capable of counting up or down in either binary or BCD decade modes. Levels preset on the Jam inputs are loaded into the counter asynchronously with the clock when the Preset Enable input is "high". "Look ahead" carry capabilities are provided to facilitate high speed operation where two or more HD-4029's are used in parallel.

The counter toggles one count on the positive going clock input when the carry input and preset enable inputs are "low". If either carry input or preset enable are "high" clocking is inhibited.

The carry out signal is normally high, going low for one clock cycle under the following conditions providing the Carry Input signal is low:

The counter has reached its maximum count in the "Up" mode.

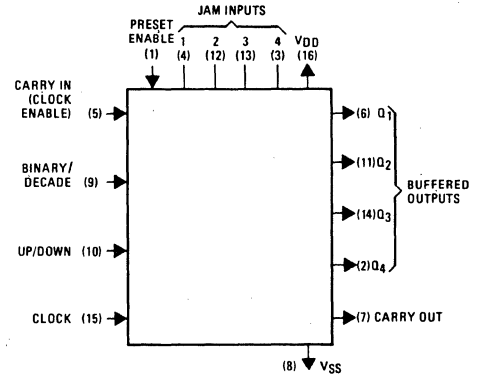
The counter has reached its minimum count in the "Down" mode.

The carry input signal functions as a clock enable permitting the counter to toggle only when "low". If the carry input is not used it must be tied to V_{SS}.

Operating modes for the HD-4029 are selected as follows:

- Binary/Decade input "high" Binary Counter
- Binary/Decade input "low" Decade Counter
- Up/Down input "high" "Up" Counter
- Up/Down Input "low" "Down" Counter

Connection Diagram



Truth Tables

CLOCK	TE	PE	J	Q	\bar{Q}
X	X	0	0	0	1
\bar{L}	1	1	X	\bar{Q}	Q
X	X	0	1	1	Q
\bar{L}	0	1	X	Q	\bar{Q} NC
\bar{L}	X	1	X	Q	\bar{Q} NC

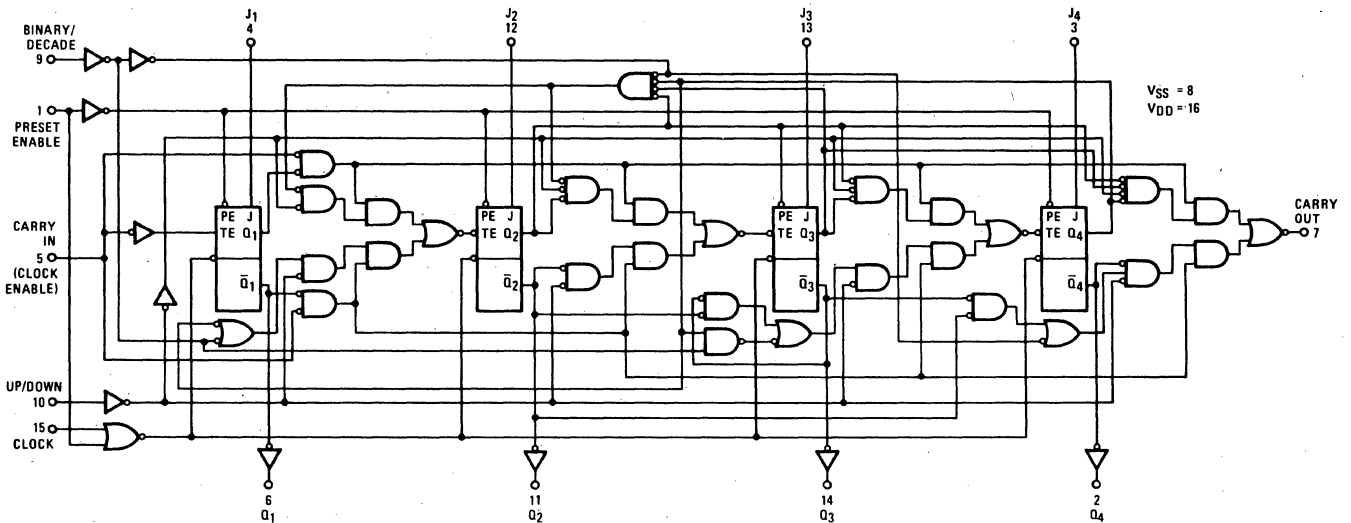
NC - No Change
TE - Toggle Enable
X - Don't Care

CLOCK	TE	PE	J	Q	\bar{Q}
X	X	0	0	0	1
\bar{L}	0	1	X	\bar{Q}	Q
X	X	0	1	1	0
\bar{L}	1	1	X	Q	\bar{Q} NC
\bar{L}	X	1	X	Q	\bar{Q} NC

NC - No Change
TE - Toggle Enable
X - Don't Care

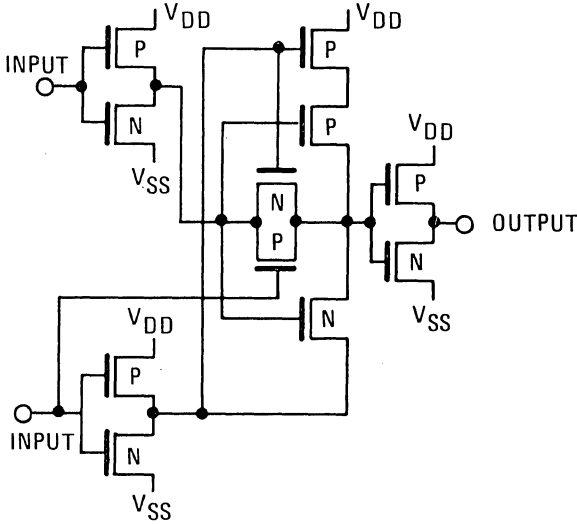
CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC (B/D)	1	BINARY COUNT
BIN/DEC (B/D)	0	DECADE COUNT
UP/DOWN (U/D)	1	UP COUNT
UP/DOWN (U/D)	0	DOWN COUNT
PRESET ENABLE (PE)	1	JAM IN
PRESET ENABLE (PE)	0	NO JAM
CARRY IN (CI) (CLOCK ENABLE)	1	NO COUNTER ADVANCE AT POS CLOCK TRANSITION
CARRY IN (CI) (CLOCK ENABLE)	0	ADVANCE COUNTER AT POS CLOCK TRANSITION

Logic Diagrams

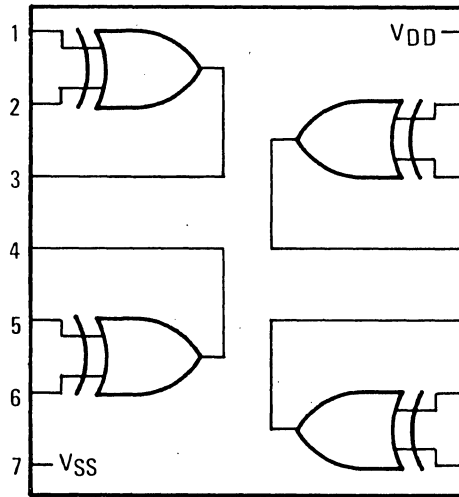


HD-4030A Quad Exclusive "OR" Gate

Circuit Diagram



Connections



Truth Table

INPUTS		OUTPUT
0	0	0
0	1	1
1	0	1
1	1	0

LOGIC "1" → V_{DD}
 LOGIC "0" → V_{SS}

HD-4035A 4 Stage with J-K Input and True/Complement Output Shift Register

Description

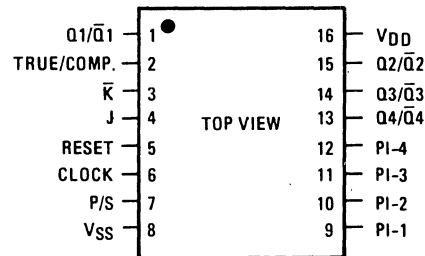
The HD-4035 is a four stage shift register capable of parallel input, serial input via J-K inputs and parallel output.

Data entry mode is controlled by the parallel/serial input. With P/S high, data is entered via the parallel inputs on the positive clock transition. Serial data is entered on the positive going clock with P/S low.

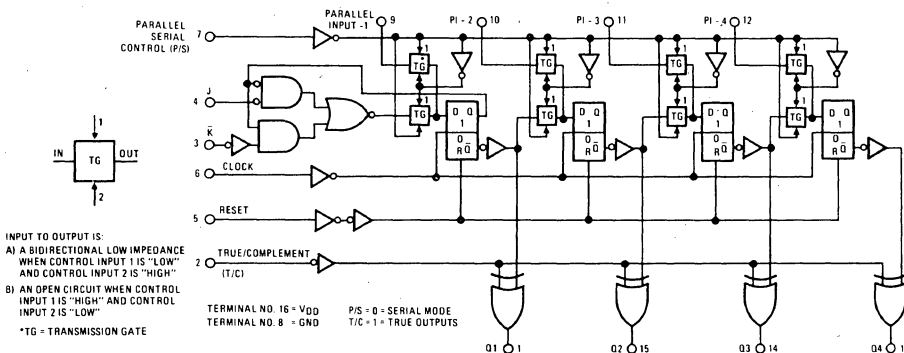
The True/complement input, when high, results in display of the true contents of the register at the outputs. When T/C is low, the complement of the register data is displayed.

The reset input, when high, asynchronously resets all four flip-flop stage.

Connection Diagrams



Circuit Diagram



Truth Table

CL	t _n - 1 (INPUTS)				t _n (OUTPUTS)	
	J	K̄	R	Q _{n-1}	Q _n	
0	0	X	0	0	0	
0	1	X	0	0	1	
0	X	0	0	1	0	
0	1	0	0	Q _{n-1}	Q _{n-1}	TOGGLE MODE
0	X	1	0	1	1	
0	X	X	0	Q _{n-1}	Q _{n-1}	
0	X	X	1	X	0	

HD-54C/74C Series

ABSOLUTE MAXIMUM RATINGS

Voltage at Any Pin	-0.3V to $V_{CC} + 0.3V$	Storage Temperature Range	-65°C to +150°C
Operating Temperature Range		Maximum V_{CC} Voltage	16V
54C	-55°C to +125°C	Package Dissipation	500mW
74C	-40°C to +85°C	Lead Temperature (Soldering, 10 Seconds)	300°C

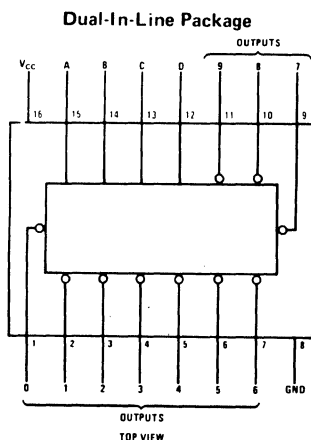
HD-54C42/HD-74C42 BCD to Decimal Decoder

Description

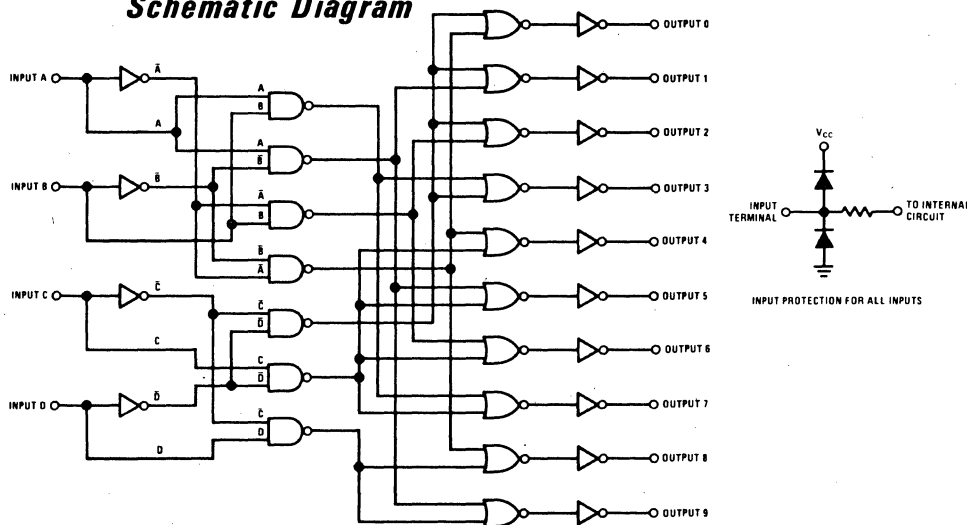
The HD-54C42/HD-74C42 one-of-ten decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. This decoder

produces a logical "0" at the output corresponding to a four bit binary input from zero to nine and a logical "1" at the other outputs. For binary inputs from ten to fifteen all outputs are logical "1".

Connection Diagram



Schematic Diagram

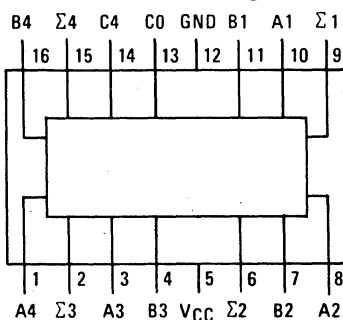


HD-54C83/HD-74C83 4-Bit Binary Full Adder

Description

The HD-54C83/HD-74C83 4-bit binary full adder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. This full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. The adders are designed so that logic levels of the input and output, including the carry, are in their true form. Thus the end-around carry is accomplished without the need for level inversion.

Connection Diagram



Truth Table

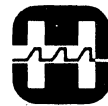
INPUT				OUTPUT							
				WHEN $C_0 = L$				WHEN $C_0 = H$			
A1	B1	A2	B2	$\Sigma 1$	$\Sigma 2$	C_2	$\Sigma 1$	$\Sigma 2$	C_2		
A3	B3	A4	B4	$\Sigma 3$	$\Sigma 4$	C_4	$\Sigma 3$	$\Sigma 4$	C_4		
L	L	L	L	L	L	L	H	L	L		
H	L	L	L	H	L	L	L	H	L		
L	H	L	L	L	H	L	L	H	L		
H	H	L	L	L	H	L	H	H	L		
L	L	H	L	L	H	L	H	H	L		
H	L	H	L	H	H	L	L	L	H		
L	H	H	L	H	H	L	L	L	H		
H	H	H	L	L	L	H	H	L	H		
L	L	L	H	L	H	L	H	H	L		
H	L	L	H	H	H	L	L	L	H		
L	H	L	H	L	L	H	H	L	H		
H	H	L	H	L	L	H	L	H	H		
L	L	H	H	H	L	H	L	H	H		
H	L	H	H	H	L	H	L	H	H		
L	H	H	L	H	H	H	H	H	H		

NOTE:

Input conditions at A3, A2, B2 and C0 are used to determine outputs $\Sigma 1$ and $\Sigma 2$ and the value of the internal carry C2. The values at C2, A3, B3, A4 and B4 are then used to determine outputs $\Sigma 3$, $\Sigma 4$ and C4.

H = High Level

L = Low Level

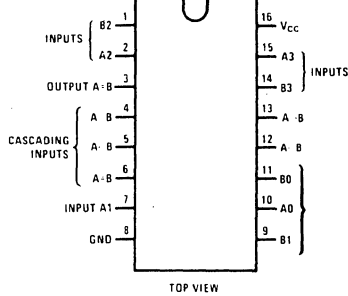


HD-54C85/HD-74C85 4-Bit Magnitude Comparator

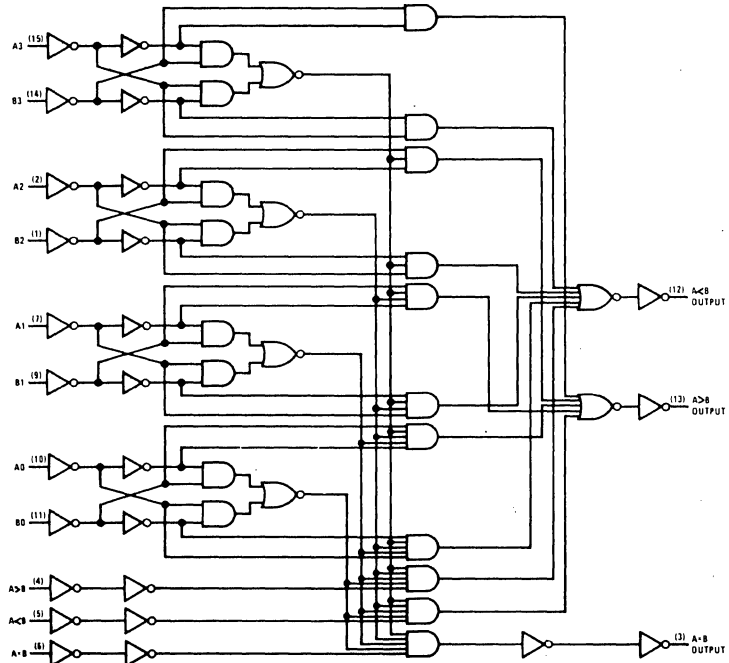
Description

The HD-54C85/HD-74C85 is a four-bit magnitude comparator which will perform comparison of straight binary or BCD codes. The circuit consists of eight comparing inputs (A0, A1, A2, A3, B0, B1, B2, B3), three cascading inputs (A>B, A<B and A = B), and three outputs (A>B, A<B and A = B). This device compares two four-bit words (A and B) and determines whether they are "greater than," "less than," or "equal to" each other by a high level on the appropriate output. For words greater than four-bits, units can be cascaded by connecting the outputs (A>B, A<B and A = B) of the least-significant stage to the cascade inputs (A<B, A<B and A = B) of the next-significant stage. In addition, the least significant stage must have a high level voltage (V_{IN(1)}) applied to the A = B input and low level voltages (V_{IN(0)}) applied to A>B and A<B inputs.

Connection Diagram



Logic Diagram



HD-54C89/HD-74C89 64-Bit Three-State Random Access Read/Write Memory

Description

The HD-54C89/HD-74C89 is a 16 word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a write enable line and a memory enable line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register, latches the address information on the positive to negative transition of the memory enable input. The four three state data output lines working in conjunction with the memory enable input provides for easy memory expansion.

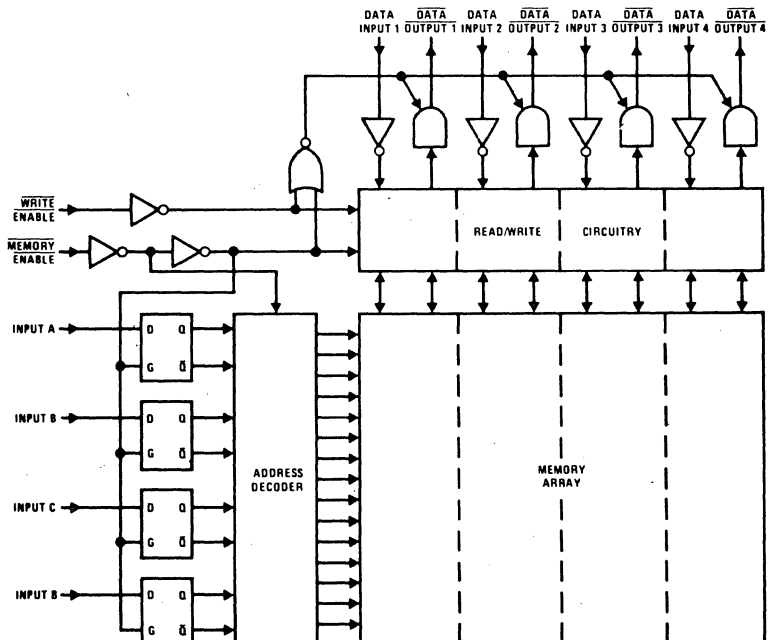
ADDRESS OPERATION: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable.)

WRITE OPERATION: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

READ OPERATION: The complement of the information which was written into the memory is nondestructively read out at the four outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

When the device is writing or disabled the output assumes a three state (HI-Z) condition.

Circuit Diagram

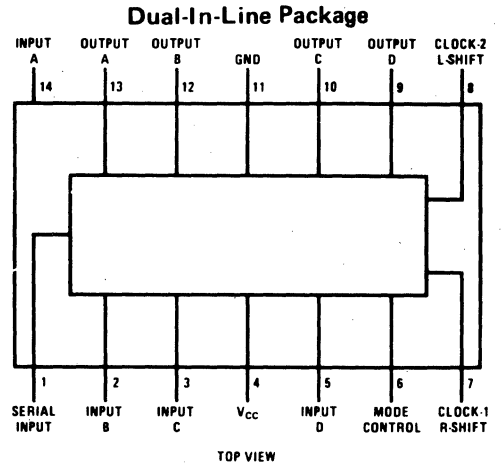


HD-54C95/HD-74C95 4-Bit Right-Shift, Left-Shift Register

Description

This four-bit shift register is a monolithic complementary MOS (CMOS) integrated circuit composed of four D flip-flops. This register will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an N-bit right-shift or left-shift register. When a logical "0" level is applied to the mode control input, the output of each flip-flop is coupled to the D input of the succeeding flip-flop. Right-shift operation is performed by clocking at the clock 1 input, and serial data entered at the serial input, clock 2 and parallel inputs A through D are inhibited. With a logical "1" level applied to the mode control, outputs to succeeding stages are decoupled and parallel loading is possible, or with external interconnection, shift-left operation can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop and serial data is entered at input D.

Connection Diagram

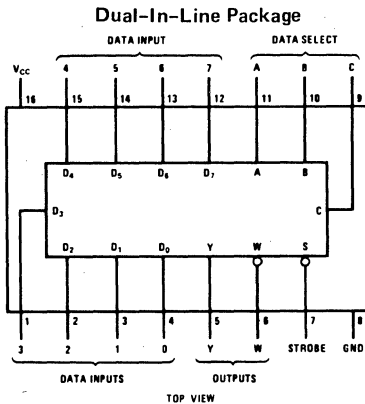


HD-54C151/HD-74C151 8 Channel Digital Multiplexer

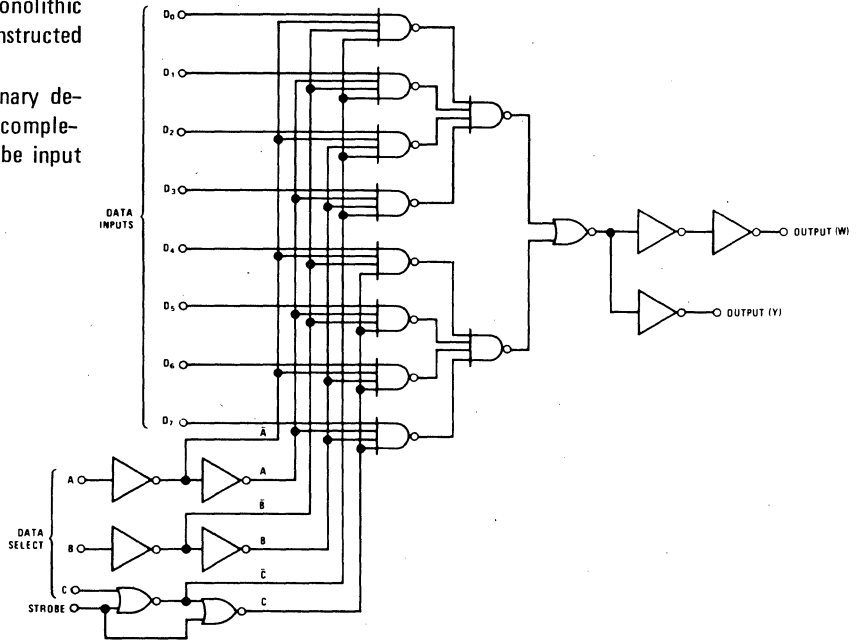
Description

The HD-54C151/HD-74C151 multiplexer is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P- channel enhancement transistors. This data selector/multiplexer contains on-chip binary decoding. Two outputs provide true (output Y) and complement (output W) data. A logical "1" on the strobe input forces W to a logical "1" and Y to a logical "0"

Connection Diagrams



Logic Diagrams



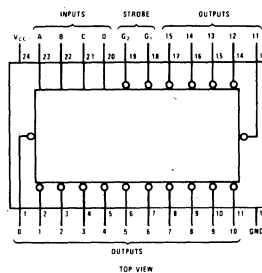
HD-54C154/HD-74C154 4-Line to 16-Line Decoder/Demultiplexer

Description

The HD-54C154/HD-74C154 one of sixteen decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The device is provided with two strobe inputs, both of which must be in the logical "0" state for normal operation. If either strobe input is in the logical "1" state, all 16 outputs will go to the logical "1" state.

To use the product as a demultiplexer, one of the strobe inputs serves as a data input terminal, while the other strobe input must be maintained in the logical "0" state. The information will then be transmitted to the selected output as determined by the four-line input address.

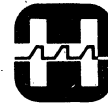
Connection Diagram



Truth Table

INPUTS				OUTPUTS																		
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

X = "Don't Care" Condition



HD-54C160/HD-74C160 Decade Counter with Asynchronous Clear
HD-54C161/HD-74C161 Binary Counter with Asynchronous Clear
HD-54C162/HD-74C162 Decade Counter with Synchronous Clear

Description

These (synchronous presettable up) counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. They feature an internal carry lookahead for fast counting schemes and for cascading packages without additional gating.

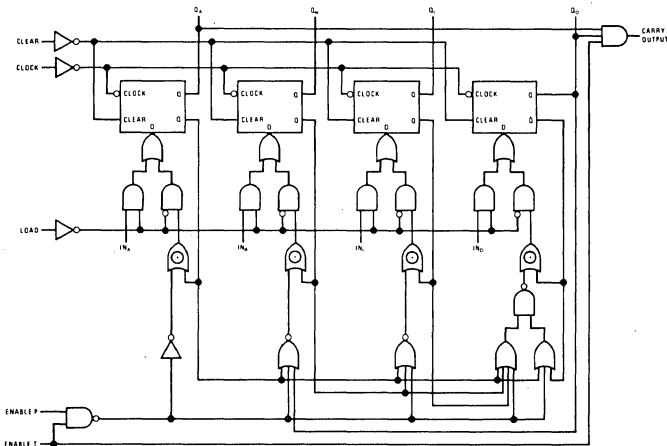
A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the C162 is synchronous and a low level at the clear input sets

all our outputs low after the next positive clock edge. The clear function for the C160 and C161 is asynchronous and a low level at the clear input sets all four outputs low regardless of the state of the clock.

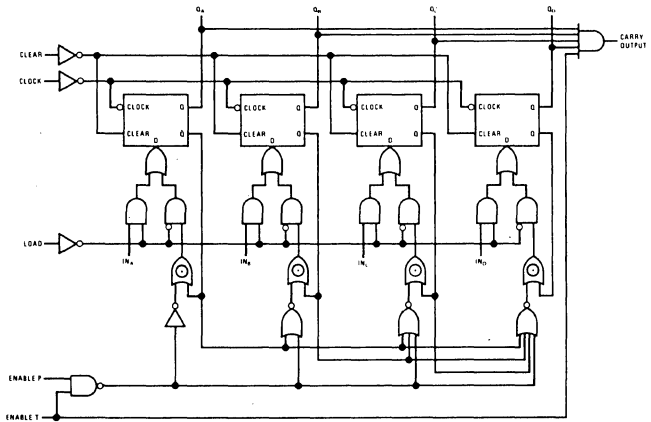
Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

Logic Diagrams

C160/C162; Clear is Synchronous for the C162



C161; Clear is Asynchronous



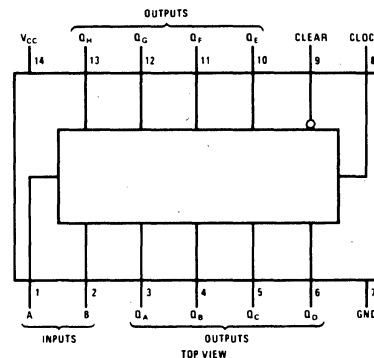
HD-54C164/HD-74C164 8-Bit Parallel-Out Serial Shift Register

Description

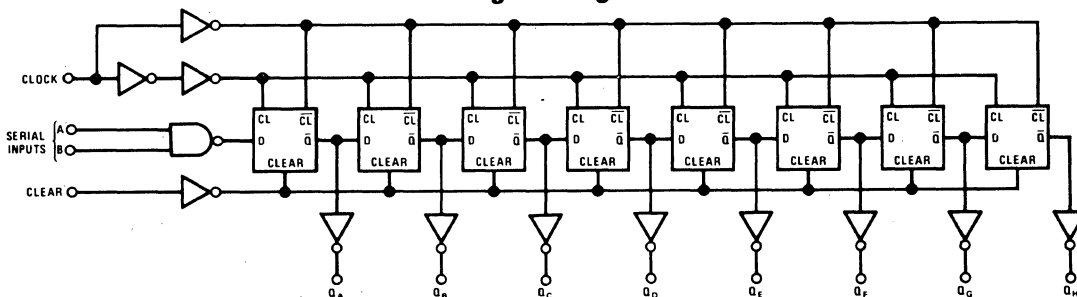
The HD-54C164/HD-74C164 shift registers are a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P- channel enhancement transistors. These 8-bit shift registers have gated serial inputs and clear. Each register bit is a D-type master/slave flip-flop. A high-level input enables the other input which will then determine the state of the flip-flop.

Data is serially shifted in and out of the 8-bit register during the positive going transition of clock pulse. Clear is independent of the clock and accomplished by a low level at the clear input. All inputs are protected against electrostatic effects.

Connection Diagram



Logic Diagram



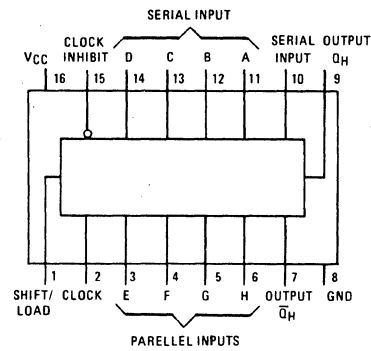
HD-54C165/HD-74C165 Parallel-Load 8-Bit Shift Register

Description

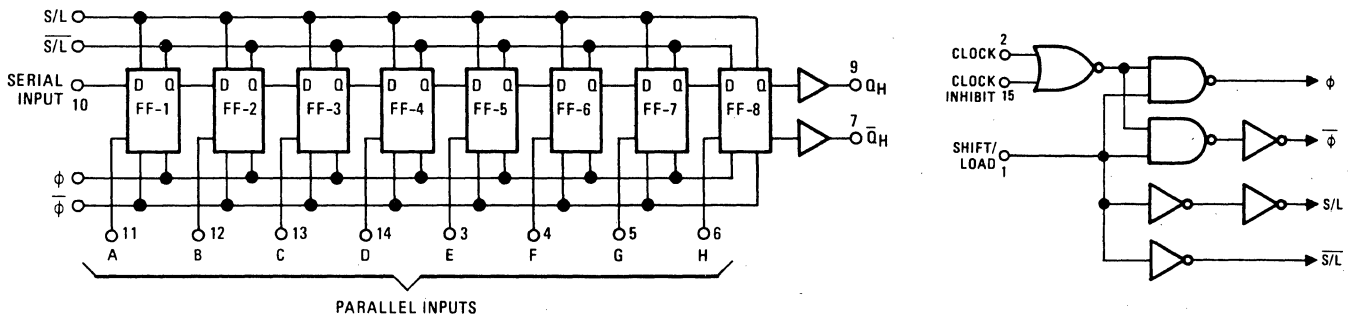
The HD54C165/HD74C165 is an 8-bit serial shift register which shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the shift/load input. Also included is a gated clock input and a complementary output from the eight-bit.

Clocking is accomplished through a 2-input NOR-gate permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the shift/load input high enables the other clock input. Data transfer occurs on the positive edge of the clock. The clock inhibit input should be changed to a high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

Connection Diagram



Block Diagram



HD-54C192/HD-74C192 Synchronous 4-Bit Up/Down Decade Counter

HD-54C193/HD-74C193 Synchronous 4-Bit Up/Down Binary Counter

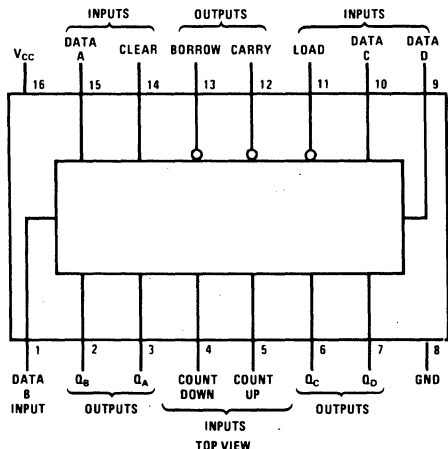
Description

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The HD-54C192 and HD-74C192 are BCD counters. While the HD-54C193 and HD-74C193 are binary counters.

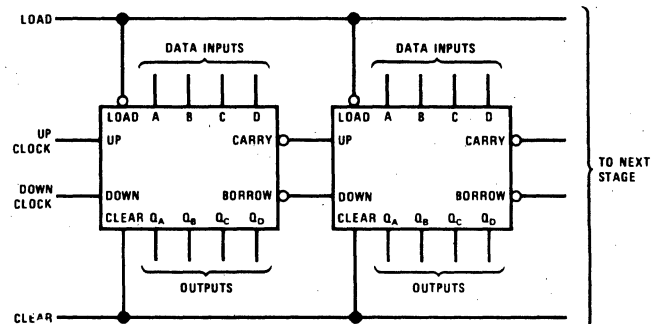
Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive going transition of this clock.

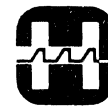
These counters feature preset inputs that are set when load is a logical "0" and a clear which forces all outputs to "0" when it is at logical "1". The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry.

Connection Diagram



Functional Diagram





HD-54C195/HD-74C195 4-Bit Registers

Description

The HD-54C195/HD-74C195 CMOS 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input and a direct overriding clear. The following two modes of operation are possible.

Parallel Load

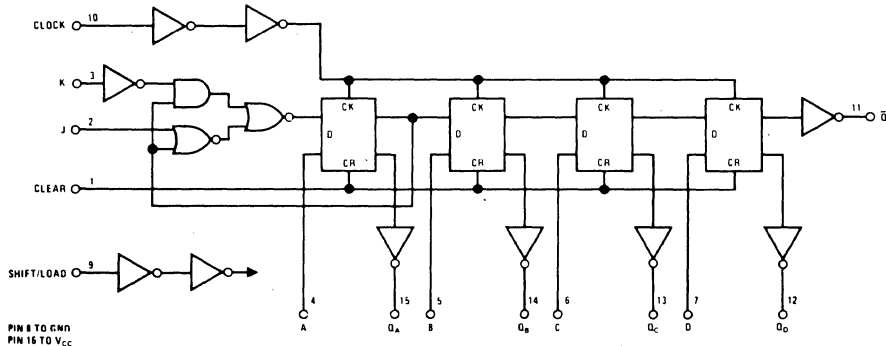
Shift in direction QA towards QD

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is

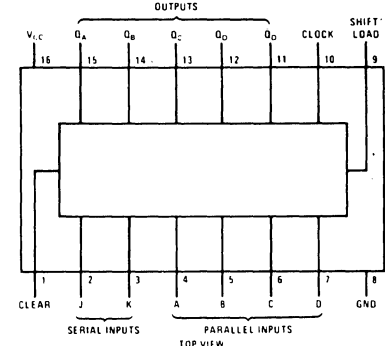
loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited.

Serial shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs allow the first stage to perform as a J-K, D or T-type flip-flop as shown in the truth table.

Circuit Diagram



Connection Diagram



Advanced Information HD-54C200/HD-74C200 256-Bit Three-State Random Access Read/Write Memory

Description

The HD-54C200/HD-74C200 is a 256-bit random access read/write memory. Inputs consist of eight address lines, a data input line, a write enable line, and three chip enables. The eight binary address inputs are decoded internally to select each of the 256 locations. An internal address register, latches and address information on the positive to negative edge of CE3 or CE2 inputs. The three state data output line working in conjunction with CE1 or CE2 inputs provides for easy memory expansion.

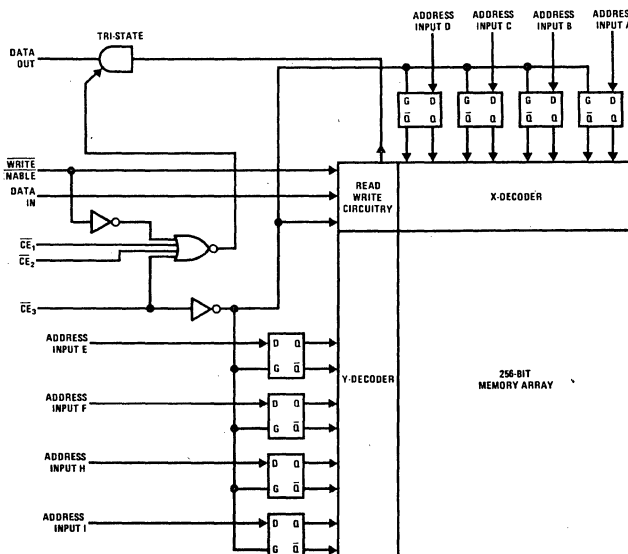
for more than t_{HA} after the memory is enabled (positive to negative transition).

READ OPERATION: The data is read out by selecting the proper address and bringing CE1, CE2 or CE3 low and write enable high. Holding CE1 or CE2 at a high level forces the output into three state. When used in bus organized systems, CE1, or CE2, a three state control, provides for fast access times by not disabling the chip.

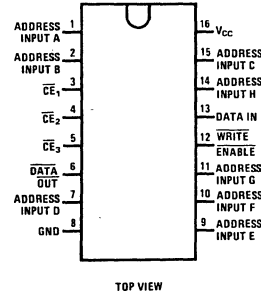
WRITE OPERATION: Data is written into the memory with CE2 and CE3 low and write enable low. The state of CE1 has no effect on the write cycle. The output assumes three state with write enable low.

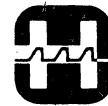
ADDRESS OPERATION: Address inputs must be stable t_{SA} prior to the positive to negative transition of CE3 or CE2. It is thus not necessary to hold address information stable

Logic and Connection Diagrams



Dual-In-Line Package





HD-54C221/HD-74C221 Dual Monostable Multivibrator

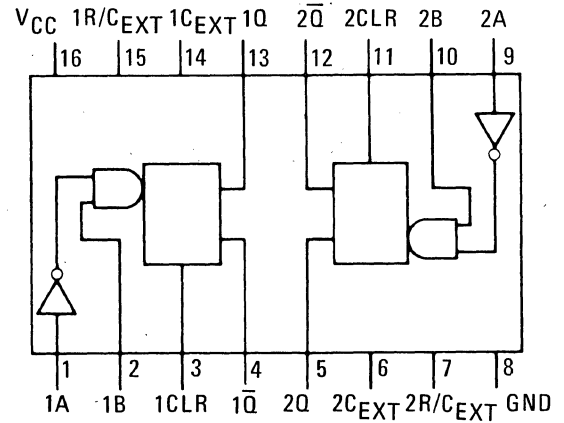
Description

The HD54C221/HD74C221 dual monostable multivibrators is monolithic complementary MOS integrated circuit. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input, and a clear input.

Once fired, the output pulses are independent of further transitions of the A and B inputs and are a function of the external timing components C_{EXT} and R_{EXT} . The pulse width is stable over a wide range of temperature and V_{CC} . Pulse stability will be limited by the accuracy of external timing components. The R_{EXT} ranges from 10k to 100k. Throughout these ranges the pulse width is approximately defined by the relationship $t_{W(OUT)} \approx C_{EXT} R_{EXT}$.

Connection Diagram

DUAL-IN-LINE PACKAGE



Truth Table

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎓	⏚
H	↓	H	⎓	⏚

H = High Level

L = Low Level

↑ = Transition from Low to High

↓ = Transition from High to Low

⎓ = One High Level Pulse

⏚ = One Low Level Pulse

X = Irrelevant

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645 Stewart Avenue
Garden City, New York 11530**

LOW-POWER SCHOTTKY

54LS

DESCRIPTION

The Raytheon 54LS Low-Power Schottky TTL family utilizes Schottky-barrier diode clamping, shallow diffusions and small geometries to achieve speeds comparable to 5400 at one-fifth the power and 54H at one-tenth the power. It is completely compatible with most of the popular TTL and DTL logic families and is equivalent in performance to the Fairchild 9LS series.

FEATURES

High Speed, Low Power

- 5 ns typical gate propagation delay time
- 2 mW typical gate power dissipation at 50% duty cycle = speed-power product of 10 pJ

Ease of System Design

- Switching times virtually insensitive to power supply, temperature variations
- Low noise generation
- High fan-out
- Schottky-diode-clamped inputs minimize high-speed termination effects
- Low output impedance gives low noise susceptibility, high capacitance drive capability
- Power dissipation remains relatively low at operating frequencies up to 30 MHz
- Smaller, lower-cost power supplies and cooling equipment

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Notes 1 and 2)	5.5 V
Interemitter voltage (see Note 3)	5.5 V
Output voltage (see Notes 1 and 4)	7 V
Operating free-air temperature range: 54LS	-55°C to 125°C
Storage temperature range	-65°C to 150°C

NOTES:

1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. Except 54LS74, 109, 181, 196, 197. For 54LS74, 109, 181, 196, 197, rating is 5.5 V.
3. This is the voltage between two emitters of a multiple-emitter transistor.
4. This is the maximum voltage which should be applied to any open-collector output when it is in the off state.

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54LS00 54LS04
54LS10 54LS20 54LS30

Positive-NAND Gates, Hex Inverters

PIN-OUT AND LOGIC DIAGRAMS

54LS00
QUADRUPLE 2-INPUT NAND GATE

Die Size .047 x .048

Positive logic: $Y = \overline{AB}$

54LS04
HEX INVERTER

Die Size .048 x .051

positive logic: $Y = \overline{A}$

54LS10
TRIPLE 3-INPUT NAND GATE

Die Size .052 x .054

positive logic: $Y = \overline{ABC}$

54LS20
DUAL 4-INPUT NAND GATE

Die Size .042 x .044

positive logic: $Y = \overline{ABCD}$

54LS30
8-INPUT NAND GATE

Die Size .042 x .044

positive logic: $Y = \overline{ABCDEFGH}$

NC — No internal connection



Positive-NAND Gates, Hex Inverters

54LS00 54LS04
54LS10 54LS20 54LS30

DIGITAL

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Recommended Operating Conditions

		Min	Nom	Max	Unit
Supply voltage, V_{CC}		4.5	5	5.5	V
Normalized fan-out from each output, N	High logic level	20			
	Low logic level	20			
Operating free-air temperature, T_A		-55		125	°C

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.7	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $I_{OH} = -400 \mu\text{A}$, $V_{IL} = 0.7 \text{ V}$	2.5	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$	0.3	0.45	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7.0 \text{ V}$			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.36	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-15		-100	mA
I_{CCH} Supply current, outputs high (average per gate)	$V_{CC} = \text{MAX}$, All inputs at 0 V	LS00,04,10,20	0.2	0.4	mA
		LS30	0.35	0.5	
I_{CCL} Supply current, outputs low (average per gate)	$V_{CC} = \text{MAX}$, All inputs at 4.5 V		0.6	1.1	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

Switching Characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

Parameter	Test Conditions		Min	Typ	Max	Unit
Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}$ $R_L = 2 \text{ k}\Omega$	LS00,04,10,20	3.0	5.0	10	ns
		LS30	4.0	7.0	12	
t_{PHL} Propagation delay time high-to-low-level output	See Fig. A on page 373	LS00,04,10,	3.0	5.0	10	ns
		LS20	4.0	8.0	12	
		LS30	6.0	13	20	



54LS01 54LS03
54LS05 54LS12 54LS22

Positive-NAND Gates, Hex Inverters With Open-Collector Outputs

PIN-OUT AND LOGIC DIAGRAMS

54LS01
QUADRUPLE 2-INPUT NAND GATE

Die Size .047 x .048

positive logic: $Y = \overline{AB}$

54LS03
QUADRUPLE 2-INPUT NAND GATE

Die Size .047 x .048

positive logic: $Y = \overline{AB}$

54LS05
HEX INVERTER

Die Size .048 x .051

positive logic: $Y = \overline{A}$

54LS12
TRIPLE 3-INPUT NAND GATE

Die Size .052 x .054

positive logic $Y = \overline{ABC}$

54LS22
DUAL 4-INPUT NAND GATE

Die Size .042 x .044

positive logic: $Y = \overline{ABCD}$

NC—No internal connection



Positive-NAND Gates, Hex Inverters With Open-Collector Outputs

54LS01 54LS03
54LS05 54LS12 54LS22

DIGITAL

Raytheon Semiconductor

Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC} (See Note 1)	4.5	5	5.5	V
High-level output voltage, V_{OH}			5.5	V
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	-55		125	°C

NOTE 1: Voltage values are with respect to network ground terminal.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit	
V_{IH} High-level input voltage		2			V	
V_{IL} Low-level input voltage				0.7	V	
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5	V	
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{OH} = 5.5 \text{ V}$			100	μA	
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$		$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
			$I_{OL} = 8 \text{ mA}$	0.3	0.45	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7.0 \text{ V}$			0.1	mA	
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20	μA	
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.36	mA	
I_{CCH} Supply current, outputs high (average per gate)	$V_{CC} = \text{MAX}$, All inputs at 0 V		0.2	0.4	mA	
I_{CCL} Supply current, outputs low (average per gate)	$V_{CC} = \text{MAX}$, All inputs at 4.5 V		0.6	1.1	mA	

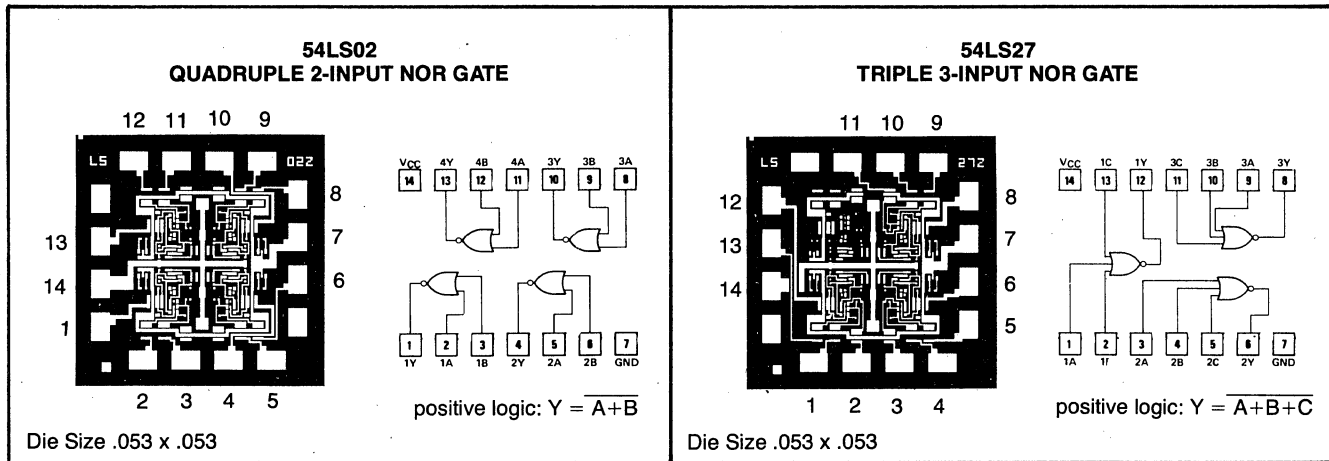
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

Switching Characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

Parameter	Test Conditions		Min	Typ	Max	Unit
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}$ $R_L = 2 \text{ k}\Omega$ See Fig. B on page 373	All Types	7.0	14	22	ns
t_{PHL} Propagation delay time, high-to-low-level output		All Types	4.0	10	18	ns



PIN-OUT AND LOGIC DIAGRAMS



Recommended Operating Conditions

		Min	Nom	Max	Unit
Supply voltage, V_{CC}		4.5	5	5.5	V
Normalized fan-out from each output, N	High logic level				20
	Low logic level				20
Operating free-air temperature, T_A		-55			125 °C

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.7	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, I_{OH} = -400 \mu\text{A}, V_{IL} = 0.7 \text{ V}$	2.5	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}$			0.25	0.4
				0.3	0.45
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.36	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-15		-100	mA
I_{CCH} Supply current, outputs high (Total)	$V_{CC} = \text{MAX}, \text{ All inputs at } 0 \text{ V}$	LS02	1.6	3.2	mA
		LS27	2.0	4.0	
I_{CCL} Supply current, outputs low (Total)	$V_{CC} = \text{MAX}, \text{ All inputs at } 5 \text{ V}$	LS02	2.8	5.4	mA
		LS027	3.4	6.8	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 ‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.
 §Not more than one output should be shorted at a time.

Switching Characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$	3.0	6.0	10	ns
t_{PHL} Propagation delay time, high-to-low-level output	See Fig. A on page 373	3.0	5.0	10	ns



PIN-OUT AND LOGIC DIAGRAMS

54LS08
QUADRUPLE 2-INPUT AND GATES

positive logic: $Y = AB$

Die Size .045 x .056

54LS11
TRIPLE 3-INPUT AND GATES

positive logic: $Y = ABC$

Die Size .052 x .054

54LS21
DUAL 4-INPUT AND GATES

positive logic: $Y = ABCD$

Die Size .042 x .044

NC—No internal connection

Recommended Operating Conditions

		Min	Nom	Max	Unit
Supply voltage, V_{CC}		4.5	5	5.5	V
Normalized fan-out from each output, N	High logic level				20
	Low logic level				20
Operating free-air temperature, T_A		-55			125 °C



Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Condition†	Min	Typ‡	Max	Unit
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.7	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $I_{OH} = -400 \mu\text{A}$	2.5	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = V_{IL\text{MAX}}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$	0.3	0.45	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7.0 \text{ V}$			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.36	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-15		-100	mA
I_{CCH} Supply current, outputs high (average per gate)	$V_{CC} = \text{MAX}$, All inputs at 4.5 V		0.6	1.2	mA
I_{CCL} Supply current, outputs low (average per gate)	$V_{CC} = \text{MAX}$, All inputs at 0 V		1.1	2.2	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

Switching Characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

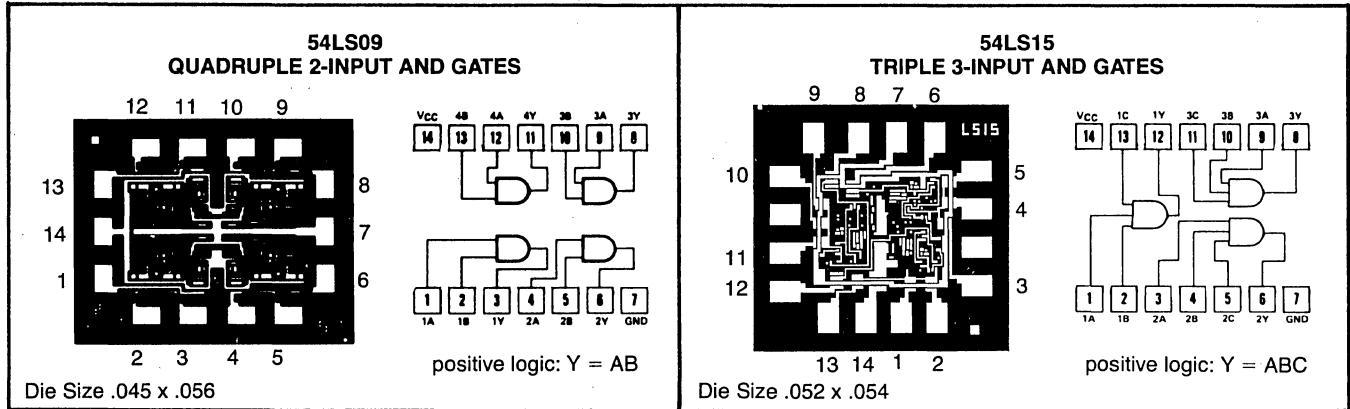
Parameter	Test Conditions		Min	Typ	Max	Unit
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}$ $R_L = 2 \text{ k}\Omega$	LS08, 11	4.0	8.5	13	ns
		LS21	5.0	10	15	
t_{PHL} Propagation delay time, high-to-low-level output	See Fig. A on page 373	LS08, 11	3.0	7.5	11	ns
		LS21	4.0	8.0	12	



Positive-AND Gates With Open-Collector Outputs

54LS09 54LS15

PIN-OUT AND LOGIC DIAGRAMS



Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC} (See Note 1)	4.5	5	5.5	V
High-level output voltage, V_{OH}			5.5	V
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	-55		125	°C

NOTE 1: Voltage values are with respect to network ground terminal.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit	
V_{IH} High-level input voltage		2			V	
V_{IL} Low-level input voltage				0.7	V	
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5	V	
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{OH} = 5.5 \text{ V}$			100	μA	
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = V_{IL \text{ MAX}}$		$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
			$I_{OL} = 8 \text{ mA}$	0.3	0.45	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7.0 \text{ V}$			0.1	mA	
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20	μA	
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.36	mA	
I_{CCH} Supply current, outputs high (average per gate)	$V_{CC} = \text{MAX}$, All inputs at 4.5 V		0.6	1.2	mA	
I_{CCL} Supply current, outputs low (average per gate)	$V_{CC} = \text{MAX}$, All inputs at 0 V		1.1	2.2	mA	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

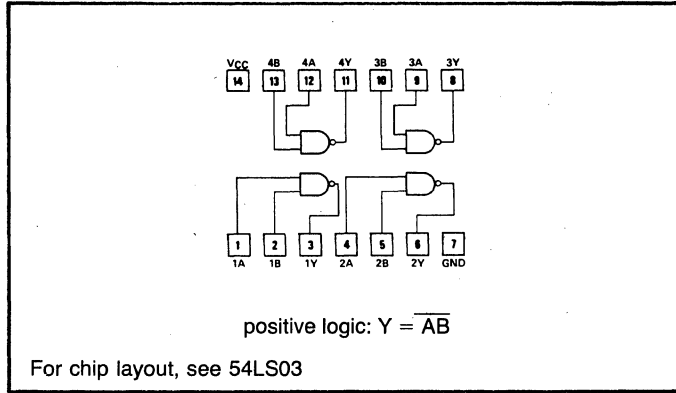
Switching Characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}$ $R_L = 2 \text{ k}\Omega$	7.0	13	20	ns
t_{PHL} Propagation delay time, high-to-low-level output	See Fig. B on page 373	5.0	10	15	ns



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PIN-OUT AND LOGIC DIAGRAM (OPEN-COLLECTOR OUTPUTS)



Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC} (See Note 1)	4.5	5	5.5	V
High-level output voltage, V_{OH}			-15	V
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	-55		125	°C

NOTE 1: Voltage values are with respect to network ground terminal.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.7	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_i = -18 \text{ mA}$			-1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{IL} = V_{IL \text{ max}}$	$V_{OH} = 12 \text{ V}$		50	μA
		$V_{OH} = 15 \text{ V}$		1	mA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$	0.3	0.45	
I_i Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_i = 7 \text{ V}$			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_i = 2.7 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_i = 0.4 \text{ V}$			-0.36	mA
I_{ICCH} Supply current, outputs high	$V_{CC} = \text{MAX}, \text{All inputs at } 0 \text{ V}$		0.8	1.6	mA
I_{CCL} Supply current, outputs low	$V_{CC} = \text{MAX}, \text{All inputs at } 4.5 \text{ V}$		2.4	4.4	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

Switching Characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega$	7.0	14	22	ns
t_{PHL} Propagation delay time, high-to-low-level output	See Fig. B on page 373	4.0	10	18	ns



PIN-OUT AND LOGIC DIAGRAMS

54LS28
QUADRUPLE 2-INPUT NOR BUFFER

positive logic: $Y = \overline{A+B}$

Die Size .045 x .052

54LS37
QUADRUPLE 2-INPUT NAND BUFFER

positive logic: $Y = \overline{AB}$

Die Size .045 x .052

54LS40
DUAL 4-INPUT NAND BUFFER

positive logic: $Y = \overline{ABCD}$

Die Size .045 x .052

Recommended Operating Conditions

		Min	Nom	Max	Unit
Supply voltage, V_{CC}		4.5	5	5.5	V
Normalized fan-out from each output, N	High logic level			60	
	Low logic level			60	
Operating free-air temperature, T_A		-55		125	°C



Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.7	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $I_{OH} = -1.2 \text{ mA}$, $V_{IL} = 0.7 \text{ V}$	2.5	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$	$I_{OL} = 12 \text{ mA}$	0.25	0.4	V
		$I_{OL} = 22 \text{ mA}$	0.35	0.5	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.36	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-30		-100	mA
I_{CCH} Supply current, outputs high (average per gate)	$V_{CC} = \text{MAX}$, All inputs at 0 V	LS28	0.45	0.9	mA
		LS37,40	0.23	0.5	
I_{CCL} Supply current, outputs low (average per gate)	$V_{CC} = \text{MAX}$, All inputs at 5 V	LS28	1.7	3.45	mA
		LS37,40	1.5	3.0	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

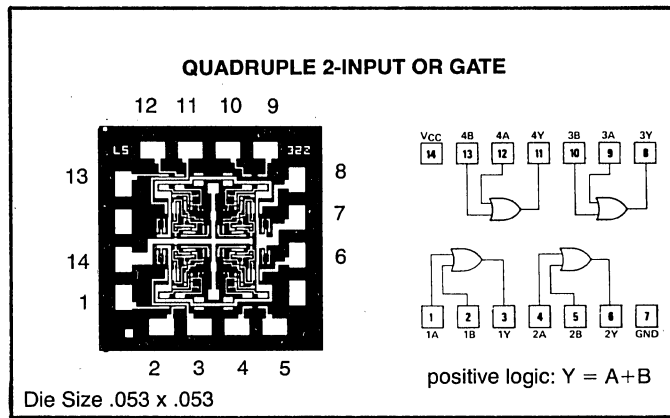
‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

Switching Characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 45 \text{ pF}$, $R_L = 667\Omega$	4.0	6	12	ns
t_{PHL} Propagation delay time, high-to-low-level output	See Fig. A on page 373	4.0	7	14	ns

PIN-OUT AND LOGIC DIAGRAM



Recommended Operating Conditions

		Min	Nom	Max	Unit
Supply voltage, V_{CC}		4.5	5	5.5	V
Normalized fan-out from each output, N	High logic level				20
	Low logic level				20
Operating free-air temperature, T_A		-55			125 °C

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.7	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $I_{OH} = -400 \mu\text{A}$	2.5	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$		$I_{OL} = 4 \text{ mA}$	0.25	0.4
			$I_{OL} = 8 \text{ mA}$	0.3	0.45
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.36	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-15		-100	mA
I_{CCH} Supply current, outputs high (Total)	$V_{CC} = \text{MAX}$, All inputs at 5 V		3.1	6.2	mA
I_{CCL} Supply current, outputs low (Total)	$V_{CC} = \text{MAX}$, All inputs at 0 V		4.9	9.8	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 ‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.
 §Not more than one output should be shorted at a time.

Switching Characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$,	3.0	7.0	11	ns
t_{PHL} Propagation delay time, high-to-low-level output	See Fig. A on Page 373	3.0	7.0	11	ns



NOR, NAND Buffers With Open-Collector Outputs

54LS33 54LS38

PIN-OUT AND LOGIC DIAGRAMS

54LS33
QUADRUPLE 2-INPUT NOR BUFFER

Die Size .045 x .052

54LS38
QUADRUPLE 2-INPUT NAND BUFFER

Die Size .045 x .052

Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	V
High-level output voltage, V_{OH}			5.5	V
Low-level output current, I_{OL}			22	mA
Operating free-air temperature, T_A	-55		125	°C

NOTE 1: Voltage values are with respect to network ground terminal.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.7	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{IL} = V_{IL\text{max}}$, $V_{OH} = 5.5 \text{ V}$			250	μA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 12 \text{ mA}$		0.25	0.4	V
	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 22 \text{ mA}$		0.35	0.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.36	mA
I_{CCH} Supply current, outputs high (Total)	$V_{CC} = \text{MAX}$, All inputs at 0 V	LS33	1.8	3.6	mA
		LS38	0.9	2.0	
I_{CCL} Supply current, outputs low (Total)	$V_{CC} = \text{MAX}$, All inputs at 4.5 V	LS33	6.9	13.8	mA
		LS38	6.0	12.0	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

Switching Characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 45 \text{ pF}$, $R_L = 667\Omega$	7.0	17	25	ns
t_{PHL} Propagation delay time, high-to-low-level output	See Fig. B on page 373	4.0	9	16	ns



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PIN-OUT AND LOGIC DIAGRAMS

54LS51
DUAL 2-WIDE AOI GATE

positive logic:
 $1Y = (1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)$
 $2Y = (2A \cdot 2B) + (2C \cdot 2D)$

Die Size .041 x .046

54LS54
4-WIDE 2-3-3-2-INPUT AOI GATE

positive logic:
 $Y = (AB) + (CDE) + (FGH) + (IJ)$

Die Size .041 x .046

54LS55
2-WIDE 4-INPUT AOI GATE

positive logic:
 $Y = (ABCD) + (EFGH)$

Die Size .041 x .046

Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC}	4.5	5	5.5	V
Normalized fan-out from each output, N	High logic level		20	
	Low logic level		20	
Operating free-air temperature, T_A	-55		125	°C



Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.7	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $I_{OH} = -400 \mu\text{A}$	2.5	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$	0.3	0.45	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.36	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-15		-100	mA
I_{CCH} Supply current, output high (Total)	$V_{CC} = \text{MAX}$, See Note 1	LS51	0.8	1.6	mA
		LS54	0.8	1.6	
		LS55	0.4	0.8	
I_{CCL} Supply current, output low (Total)	$V_{CC} = \text{MAX}$, See Note 2	LS51	1.4	2.8	mA
		LS54	1.0	2.0	
		LS55	0.7	1.3	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTES:

1. I_{CCH} is measured with all inputs grounded, and the outputs open.

2. I_{CCL} is measured with all inputs of one gate at 5 V, the remaining inputs grounded, and the outputs open.

Switching Characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$,	3.0	8.0	13	ns
t_{PHL} Propagation delay time, high-to-low-level output	See Fig. A on page 373	3.0	8.0	13	ns



Dual J-K Negative-Edge-Triggered Flip-Flops

54LS73 54LS76
54LS107 54LS112 54LS113

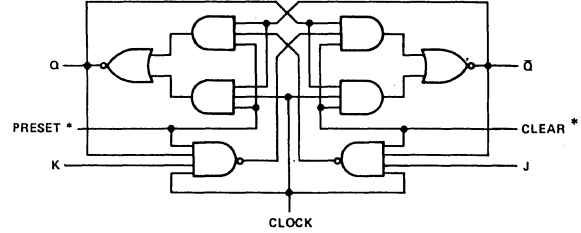
DIGITAL
Raytheon Semiconductor

•Pin-for-Pin and functional equivalents to 5473, 5476, 54107, 54S112, 54S113

DESCRIPTION

These monolithic dual J-K flip-flops feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC DIAGRAM (1/2)



	PRESET	CLEAR
LS73		X
LS76	X	X
LS107		X
LS112	X	X
LS113	X	

54LS73, 54LS107
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	Q̄
L	X	X	X	L	H
H	↓	L	L	Q ₀	Q̄ ₀
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	TOGGLE
H	H	X	X	Q ₀	Q̄ ₀

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q₀ = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

54LS76, 54LS112
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q ₀	Q̄ ₀
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q ₀	Q̄ ₀

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q₀ = the level of Q before the indicated steady-state input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

54LS113
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	Q̄
L	X	X	X	H	L
H	↓	L	↓	Q ₀	Q̄ ₀
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	TOGGLE
H	H	X	X	Q ₀	Q̄ ₀

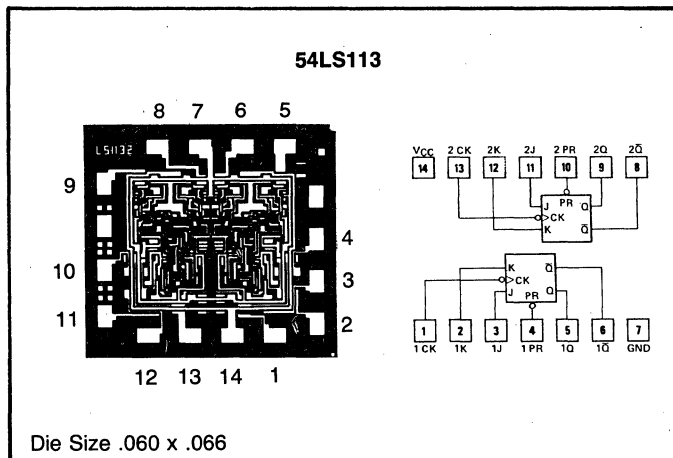
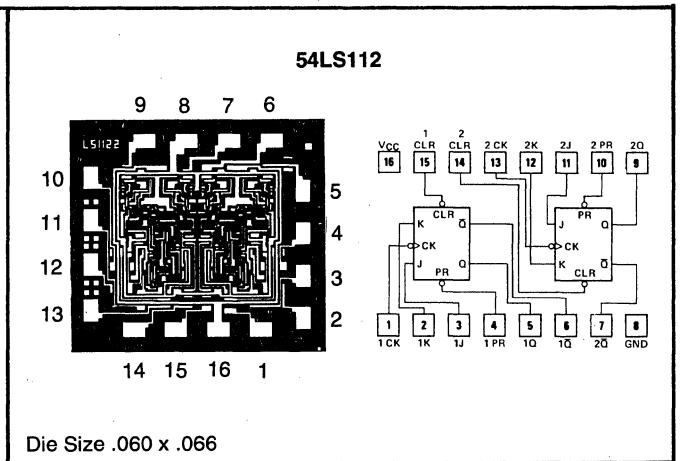
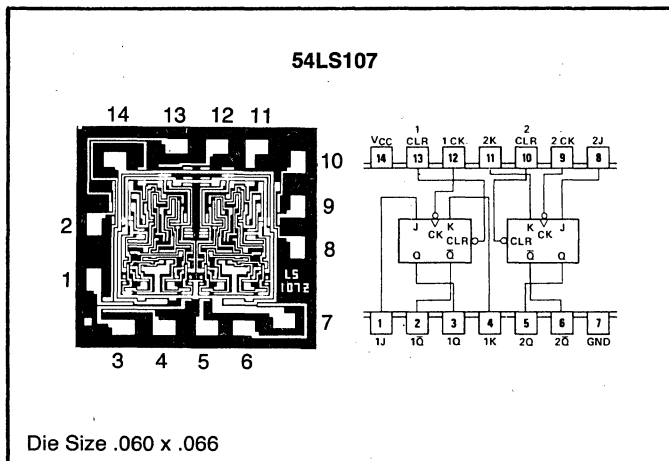
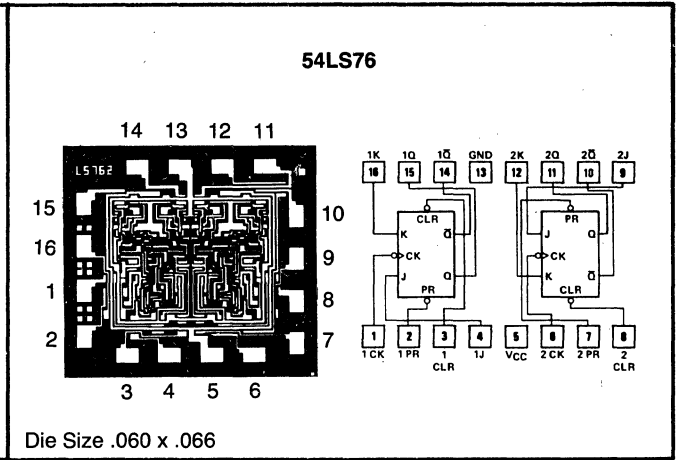
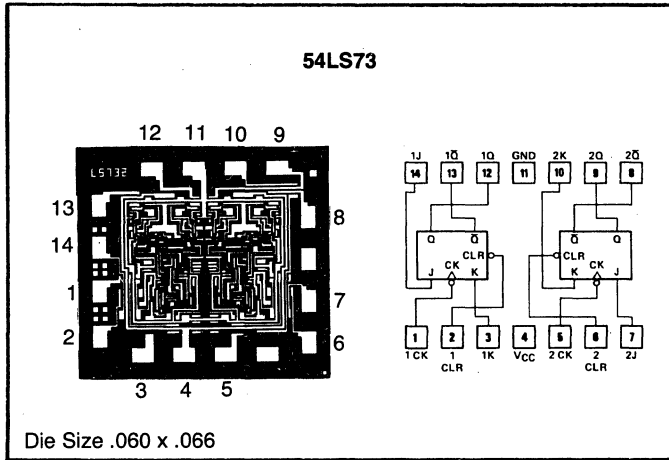
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q₀ = the level of Q before the indicated steady-state input conditions were established.
TOGGLE: Each output changes to the complement of its previous level of each ↓ clock transition.



54LS73 54LS76
54LS107 54LS112 54LS113

Dual J-K Negative-Edge-Triggered
Flip-Flops

PIN-OUT DIAGRAMS



Dual J-K Negative-Edge-Triggered Flip-Flops

54LS73 54LS76
54LS107 54LS112 54LS113

DIGITAL

Raytheon Semiconductor

Recommended Operating Conditions

		Min	Nom	Max	Unit
Supply voltage, V_{CC}		4.5	5	5.5	V
Normalized fan-out from each output, N	High logic level	20			
	Low logic level	20			
Clock frequency, f_{clock}		0		35	MHz
Width of clock pulse, $t_{w(clock)}$ (High)		15			ns
Width of preset pulse, $t_{w(preset)}$ (Low)		15			ns
Width of clear pulse, $t_{w(clear)}$ (Low)		15			ns
Input setup time, t_{setup}		15			ns
Input hold time, t_{hold}		0			ns
Operating free-air temperature, T_A		-55		125	°C

t_{setup} is the minimum time required for the correct logic level to be present at the J or K input prior to the falling edge of the clock in order to be recognized and transferred to the outputs.

t_{hold} is the minimum time required for the logic level to be maintained at the J or K input after the falling edge of the clock in order to insure recognition. These devices require no hold time.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions†		Min	Typ‡	Max	Unit
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.7	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}$,	$I_I = -18 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$,	$V_{IH} = 2 \text{ V}$, $V_{IL} = V_{ILmax}$,	2.5	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$,	$V_{IH} = 2 \text{ V}$,	$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
				$I_{OL} = 8 \text{ mA}$	0.3	0.45	
I_I	Input current at maximum input voltage	J or K	$V_{CC} = \text{MAX}$,	$V_I = 7 \text{ V}$		0.1	mA
		Clock			0.4		
		Preset or Clear			0.3		
I_{IH}	High-level input current	J or K	$V_{CC} = \text{MAX}$,	$V_I = 2.7 \text{ V}$		20	μA
		Clock			80		
		Preset or Clear			60		
I_{IL}	Low-level input current	J or K	$V_{CC} = \text{MAX}$,	$V_I = 0.4 \text{ V}$		-0.36	mA
		Clock			-0.72		
		Preset or Clear			-0.8		
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$		-15		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 1			4	8	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 1:

I_{CC} is measured with outputs open, with clock, J, K, and clear grounded and preset at 4.5 V; then with clock, J, K, and preset grounded and clear at 4.5 V.

Switching Characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

Parameter		Test Conditions		Min	Typ	Max	Unit
f_{max}	Maximum clock frequency			35	50		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear or preset	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Fig. A on page 373			9	16	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear or preset				11	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock				9	16	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock				11	20	ns



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Dual D-Type Positive-Edge-Triggered Flip-Flop

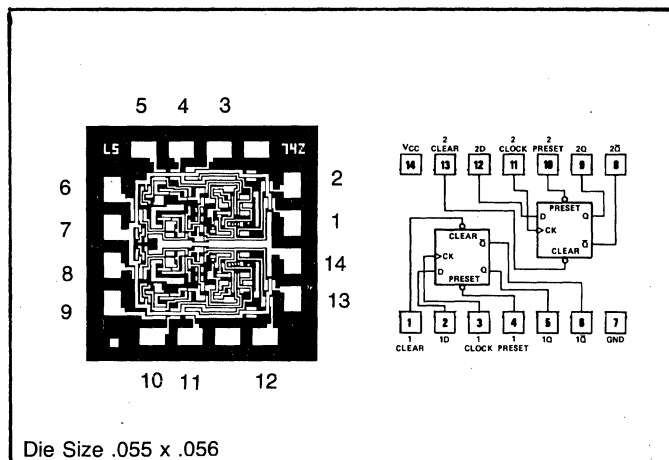
54LS74

DESCRIPTION

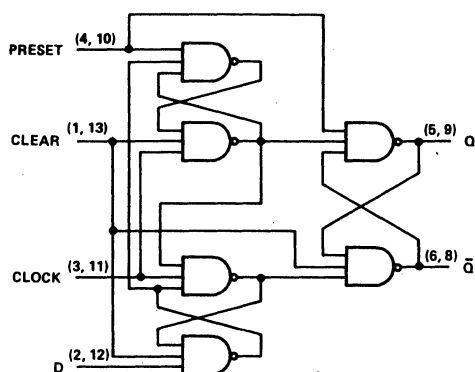
This monolithic dual edge-triggered D-type flip-flop features individual D, clock, preset, and clear inputs.

Preset and clear inputs are active-low and operate independently of the clock input. When preset and clear are inactive (high), information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect at the output.

PIN-OUT DIAGRAM



LOGIC DIAGRAM (1/2)



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	\bar{Q}_0

H = high level (steady state)
 L = low level (steady state)
 X = irrelevant
 ↑ = transition from low to high level
 Q₀ = the level of Q before the indicated steady-state input conditions were established.
 *This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V _{CC}	4.5	5	5.5	V
Normalized fan-out from each output, N	High logic level		20	
	Low logic level		20	
Clock frequency, f _{clock}	0		30	MHz
Width of clock pulse, t _{w(clock)} (High)	17			ns
Width of preset pulse, t _{w(preset)} (Low)	15			ns
Width of clear pulse, t _{w(clear)} (Low)	15			ns
Input setup time, t _{setup}	High-level data	10		ns
	Low-level data	10		
Input hold time, t _{hold}	0			ns
Operating free-air temperature, T _A	-55		125	°C

t_{setup} is the minimum time required for the correct logic level to be present at the D input prior to the rising edge of the clock in order to be recognized and transferred to the outputs.

t_{hold} is the minimum time required for the logic level to be maintained at the D input after the rising edge of the clock in order to insure recognition. This device requires no hold time.



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Dual D-Type Positive-Edge-Triggered Flip-Flop

54LS74

DIGITAL

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Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions†		Min	Typ‡	Max	Unit
V _{IH}	High-level input voltage			2			V
V _{IL}	Low-level input voltage					0.7	V
V _I	Input clamp voltage	V _{CC} = MIN,	I _I = -18 mA			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = V _{IL} max,	V _{IH} = 2 V, I _{OH} = -400 μA	2.5	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = V _{IL} max	V _{IH} = 2 V, I _{OL} = 4 mA		0.25	0.4	V
			I _{OL} = 8 mA		0.3	0.45	
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V	D input			0.1	mA
			Clock or preset			0.2	
			Clear			0.3	
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V	D input			20	μA
			Clock or preset			40	
			Clear			60	
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V	D input			-0.4	mA
			Clock or preset			-0.8	
			Clear			-1.2	
I _{OS}	Short-circuit output current§	V _{CC} = MAX		-15		-100	mA
I _{CC}	Supply current	V _{CC} = MAX,	See Note 1		4	8	mA

For condition shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

NOTE 1:

I_{CC} is measured with outputs open with D, clock, and preset grounded; then with D, clock, and clear grounded.

Switching Characteristics, V_{CC} = 5 V, T_A = 25°C

Parameter		Test Conditions		Min	Typ	Max	Unit
f _{max}	Maximum clock frequency			30	45		MHz
t _{PLH}	Propagation delay time, low-to-high-level output from clear or preset		C _L = 15 pF, R _L = 2 kΩ, See Fig. A on page 373		10	15	ns
t _{PHL}	Propagation delay time, high-to-low-level output from clear or preset	CK Low		18	24	ns	
		CK High		26	35		
t _{PLH}	Propagation delay time, low-to-high-level output from clock			12	18	ns	
t _{PHL}	Propagation delay time, high-to-low-level output from clock			14	22	ns	



Dual J-K Negative-Edge-Triggered Flip-Flops

54LS78 54LS114

DESCRIPTION

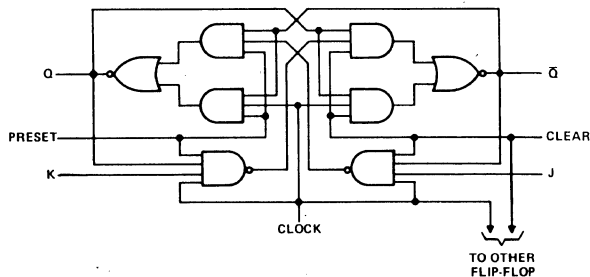
These monolithic dual J-K edge-triggered flip-flops feature individual J, K, and preset inputs plus common clock and common clear inputs. The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUTS	
PRESET	CLEAR	CLOCK	Q	\bar{Q}
L	H	X	H	L
H	L	X	L	H
L	L	X	H*	H*
H	H	↓	Q ₀	\bar{Q} ₀
H	H	↓	H	L
H	H	↓	L	H
H	H	↓	H	H
H	H	↓	TOGGLE	TOGGLE
H	H	H	Q ₀	\bar{Q} ₀

H = high level (steady state)
 L = low level (steady state)
 X = irrelevant
 ↓ = transition from high to low level
 Q₀ = the level of Q before the indicated steady-state input conditions were established.
 TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.
 *This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

LOGIC DIAGRAM (1/2)



PIN-OUT DIAGRAMS

54LS78

Die Size .060 x .066

54LS114

Die Size .060 x .066

Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V _{CC}	4.5	5	5.5	V
Normalized fan-out from each output, N	High logic level		20	
	Low logic level		20	
Clock frequency, f _{clock}	0		35	MHz
Width of clock pulse, t _{w(clock)} (High)	15			ns
Width of preset pulse, t _{w(preset)} (Low)	15			ns
Width of clear pulse, t _{w(clear)} (Low)	15			ns
Input setup time, t _{setup}	15			ns
Input hold time, t _{hold}	0			ns
Operating free-air temperature, T _A	-55		125	°C

t_{setup} is the minimum time required for the correct logic level to be present at the J or K input prior to the falling edge of the clock in order to be recognized and transferred to the outputs.
 t_{hold} is the minimum time required for the logic level to be maintained at the J or K input after the falling edge of the clock in order to insure recognition. These devices require no hold time.



Dual J-K Negative-Edge-Triggered Flip-Flops

54LS78 54LS114

DIGITAL

Raytheon Semiconductor

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions†		Min	Typ‡	Max	Unit
V _{IH}	High-level input voltage			2			V
V _{IL}	Low-level input voltage					0.7	V
V _I	Input clamp voltage	V _{CC} = MIN,	I _I = -18 mA			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN,	V _{IH} = 2 V,	2.5	3.4		V
		V _{CC} = V _{IL} max,	I _{OH} = -400 μA				
V _{OL}	Low-level output voltage	V _{CC} = MIN,	V _{IH} = 2 V,		0.25	0.4	V
				V _{IL} = V _{IL} max	I _{OL} = 4 mA		
					0.3	0.45	
I _I	Input current at maximum input voltage	V _{CC} = MAX,	V _I = 7 V	J or K		0.1	mA
				Preset		0.3	
				Clear		0.6	
				Clock		0.8	
I _{IH}	High-level input current	V _{CC} = MAX,	V _I = 2.7 V	J or K		20	μA
				Preset		60	
				Clear		120	
				Clock		160	
I _{IL}	Low-level input current	V _{CC} = MAX,	V _I = 0.4 V	J or K		-0.36	mA
				Preset		-0.8	
				Clear		-1.6	
				Clock		-1.44	
I _{OS}	Short-circuit output current§	V _{CC} = MAX		-15		-100	mA
I _{CC}	Supply current	V _{CC} = MAX,	See Note 1		4	8	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

NOTE 1: I_{CC} is measured with outputs open, with clock, J, K, and clear grounded and preset at 4.5 V; then with clock, J, K, and preset grounded and clear at 4.5 V.

Switching Characteristics, V_{CC} = 5 V, T_A = 25°C.

Parameter		Test Conditions		Min	Typ	Max	Unit
f _{max}	Maximum clock frequency			35	50		MHz
t _{PLH}	Propagation delay time, low-to-high-level output from clear or preset	C _L = 15 pF, R _L = 2 kΩ, See Fig. A on page 373			9	16	ns
t _{PHL}	Propagation delay time, high-to-low-level output from clear or preset			11	20	ns	
t _{PLH}	Propagation delay time, low-to-high-level output from clock			9	16	ns	
t _{PHL}	Propagation delay time, high-to-low-level output from clock			11	20	ns	

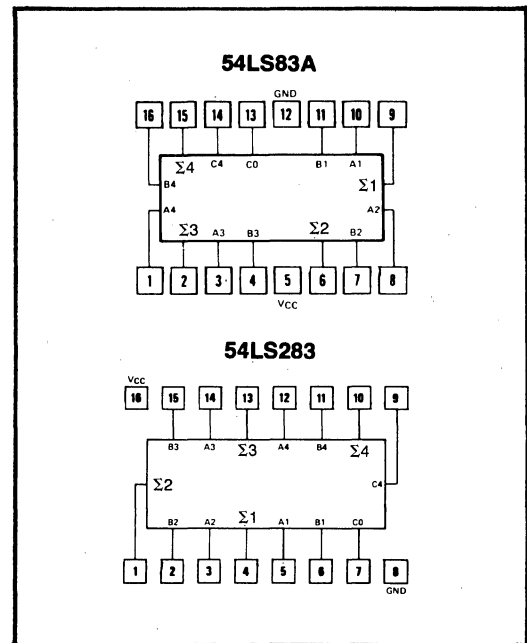
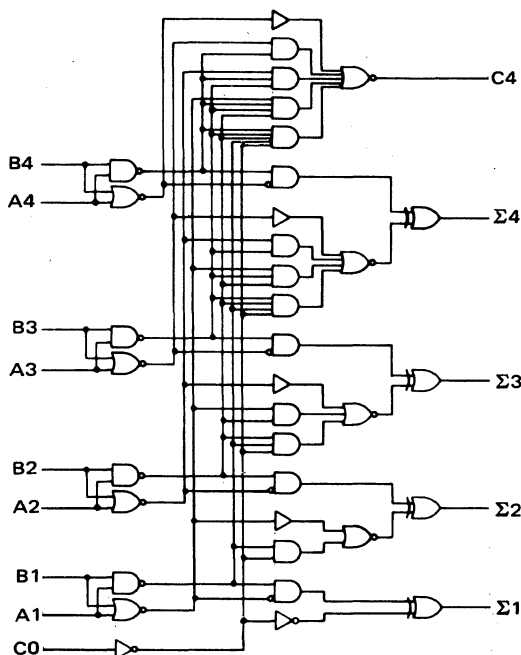


DESCRIPTION

These improved full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits generating the carry term in ten nanoseconds typically. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

The 54LS83A and the 54LS283 are identical in performance; only the pin-out is different. They are designed to replace the 5483A and the 54283 respectively. The 54LS283 is recommended for new designs; V_{CC} and ground on corner pins simplify board layout.

PIN-OUT DIAGRAMS**LOGIC DIAGRAM****FUNCTION TABLE**

INPUT		OUTPUT							
		WHEN $C_0 = L$		WHEN $C_0 = H$					
A_1	B_1	A_2	B_2	WHEN $C_2 = L$	WHEN $C_2 = H$				
				Σ_3	Σ_4	Σ_3	Σ_4	C_4	
L	L	L	L	L	L	H	L	L	
L	L	L	L	L	H	L	L	H	L
L	L	L	H	L	L	L	L	H	L
L	L	L	H	L	H	L	L	H	L
L	L	H	L	L	L	H	L	H	L
L	L	H	L	L	H	L	L	L	L
L	L	H	L	L	H	L	L	L	L
L	L	H	H	L	L	L	L	L	H
L	L	H	H	L	L	L	H	L	H
L	L	H	H	L	H	L	L	L	H
L	L	H	H	L	H	L	L	L	H
L	L	H	H	L	H	L	L	L	H
L	L	H	H	L	H	L	H	L	H
L	L	H	H	L	H	L	H	L	H
L	L	H	H	L	H	L	H	L	H
L	L	H	H	L	H	L	H	L	H

H = high level, L = low level

NOTE: Input conditions at A_1 , B_1 , A_2 , B_2 , and C_0 are used to determine outputs Σ_1 and Σ_2 and the value of the internal carry C_2 . The values at C_2 , A_3 , B_3 , A_4 , and B_4 are then used to determine outputs Σ_3 , Σ_4 , and C_4 .



Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			-400	μA
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	-55		125	$^{\circ}C$

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions†	Min	Typ‡	Max	Unit
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.7	V
V_i	Input clamp voltage	$V_{CC} = \text{MIN}, I_i = -18 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OH} = -400 \mu A, V_{IL} = V_{IL \text{ max}}$	2.5	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
			$I_{OL} = 8 \text{ mA}$	0.3	0.45	
I_i	Input current at maximum input voltage	Any A or B $V_{CC} = \text{MAX}, V_i = 7 \text{ V}$			0.2	mA
			C0			
I_{IH}	High-level input current	Any A or B $V_{CC} = \text{MAX}, V_i = 2.7 \text{ V}$			40	μA
			C0			
I_{IL}	Low-level input current	Any A or B $V_{CC} = \text{MAX}, V_i = 0.4 \text{ V}$			-0.8	mA
			C0			
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-15		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ Outputs open	All inputs grounded	22	39	mA
			All B low, other inputs at 4.5 V	19	34	
			All inputs at 4.5 V	19	34	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$.

§Only one output should be shorted at a time.

Switching Characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$

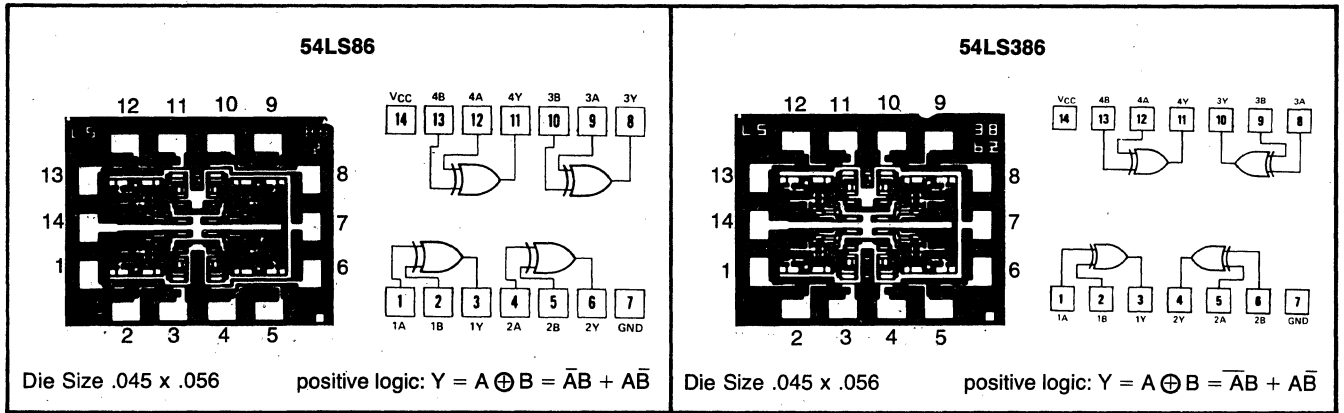
Parameter†	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Unit
t_{PLH}	C0	Any Σ	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Fig. A on page 373			24	ns
t_{PHL}						24	
t_{PLH}	A_i or B_i	Σ_i				24	ns
t_{PHL}						24	
t_{PLH}	C0	C4				17	ns
t_{PHL}						17	
t_{PLH}	A_i or B_i	C4				17	ns
t_{PHL}						17	

† t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output



PIN-OUT AND LOGIC DIAGRAMS



54LS86 and 54LS386 are electrically identical. The 54LS386 is a pin-for-pin replacement for the 54L386.

Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			-400	μA
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	-55		125	$^{\circ}C$

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.7	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu A$	2.5	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$		0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$	0.3	0.45	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.2	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.6	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-15		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2		6.1	10	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$.

§Not more than one output should be shorted at a time.

NOTE 2:

I_{CC} is measured with the inputs grounded and the outputs open.

Switching Characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$.

Parameter¶	From (input)	Test Conditions	Min	Typ	Max	Unit
t_{PLH}	A or B	Other input low $C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$				ns
t_{PHL}						
t_{PLH}	A or B	Other input high See Fig. A on page 373				ns
t_{PHL}						

¶ t_{PLH} = propagation delay time, low-to-high-level output
 § t_{PHL} = propagation delay time, high-to-low-level output

Tentative data, subject to change without notice



4-Bit Bi-Directional, Parallel-Access Shift Register

54LS95B

DESCRIPTION

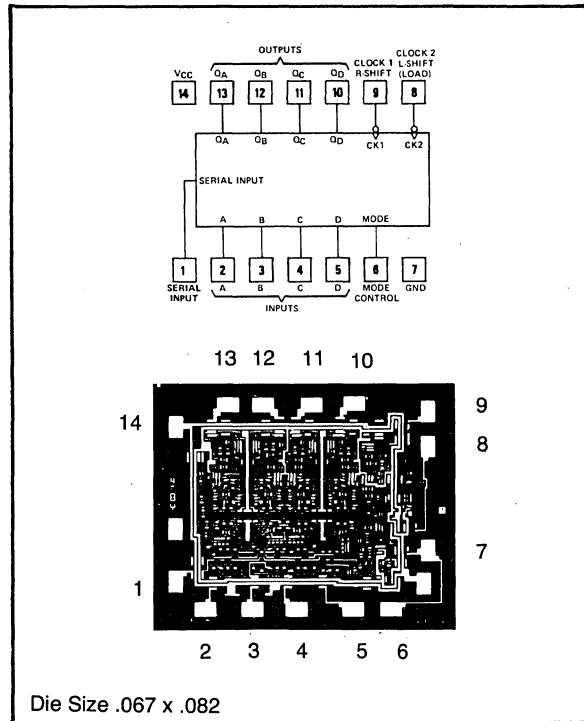
This 4-bit register features parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The register has three modes of operation:

- Parallel (broadside) load
- Shift right (the direction Q_A toward Q_D)
- Shift left (the direction Q_D toward Q_A)

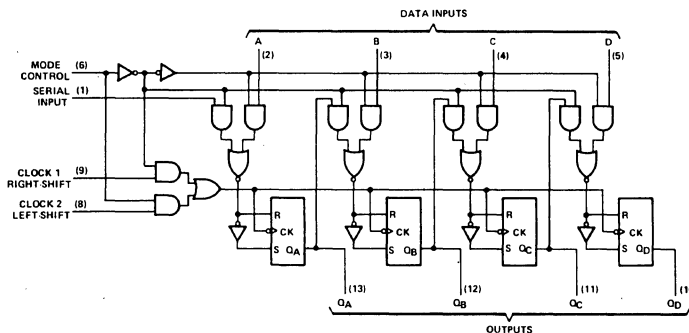
Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

PIN-OUT DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

MODE CONTROL	CLOCKS		INPUTS				OUTPUTS				
	2 (L)	1 (R)	SERIAL	PARALLEL			Q_A	Q_B	Q_C	Q_D	
				A	B	C	D				
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B^\dagger	Q_C^\dagger	Q_D^\dagger	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

↓ = transition from high to low level, ↑ = transition from low to high level

a, b, c, d = the level of steady-state input at input A, B, C, or D, respectively.

Q_{A0} , Q_{B0} , Q_{C0} , Q_{D0} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the indicated steady-state input conditions were established.

Q_{An} , Q_{Bn} , Q_{Cn} , Q_{Dn} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the most-recent transition of the clock.



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Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			-400	μA
Low-level output current, I_{OL}			8	mA
Clock frequency, f_{clock}	0			MHz
Width of clock pulse, $t_{w(clock)}$ (see Figure 1)	25			ns
Setup time, high-level or low-level data, t_{setup} (see Figure 1)	0			ns
Hold time, high-level or low-level data, t_{hold} (see Figure 1)	20			ns
Time to enable clock 1, $t_{enable 1}$ (see Figure 2)	20			ns
Time to enable clock 2, $t_{enable 2}$ (see Figure 2)	20			ns
Time to inhibit clock 1, $t_{inhibit 1}$ (see Figure 2)	10			ns
Time to inhibit clock 2, $t_{inhibit 2}$ (see Figure 2)	10			ns
Operating free-air temperature, T_A	-55		125	$^{\circ}C$

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions†	Min	Typ‡	Max	Unit
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.7	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu A$	2.5	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2V, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$		0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$		0.3	0.45	
I_I	Input current at maximum input voltage	Clock inputs Other inputs	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.2	mA
					0.1	
I_{IH}	High-level input current	Clock inputs Other inputs	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		40	μA
					20	
I_{IL}	Low-level input current	Clock inputs Other inputs	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.8	mA
					-0.4	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-15		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{ See Note 1}$		13	21	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$.

§Not more than one output should be shorted at a time.

NOTE: 1

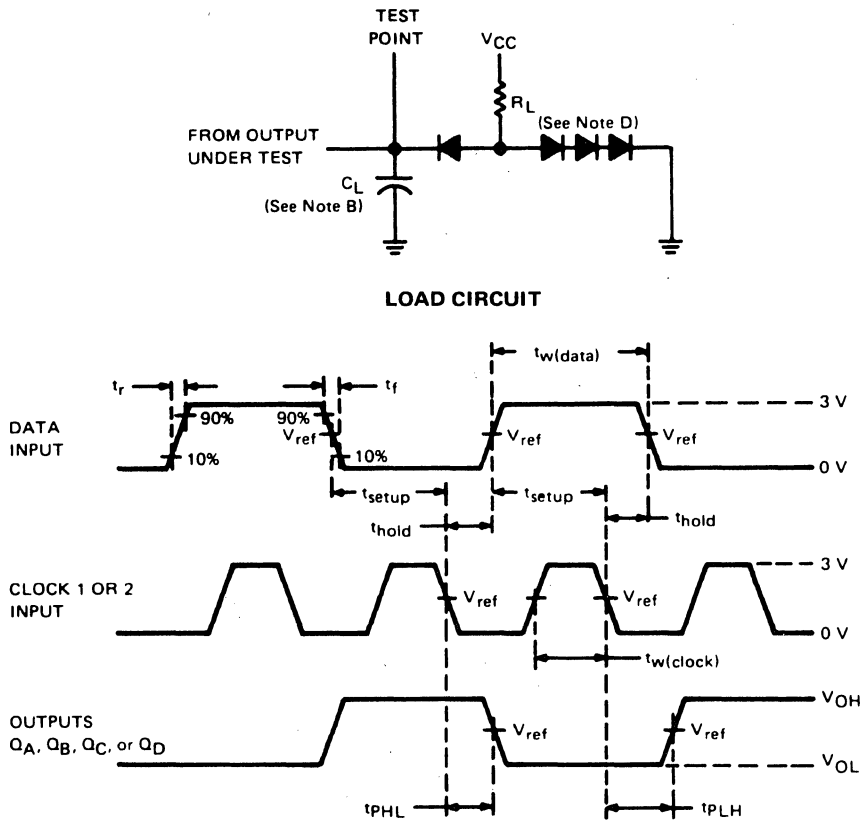
I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5 V; and a momentary 3 V, then ground, applied to both clock inputs.

Switching Characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$

Parameter		Test Conditions	Min	Typ	Max	Unit
f_{max}	Maximum clock frequency	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega$	20	30		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock	See Figure 1		27	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			30	40	ns

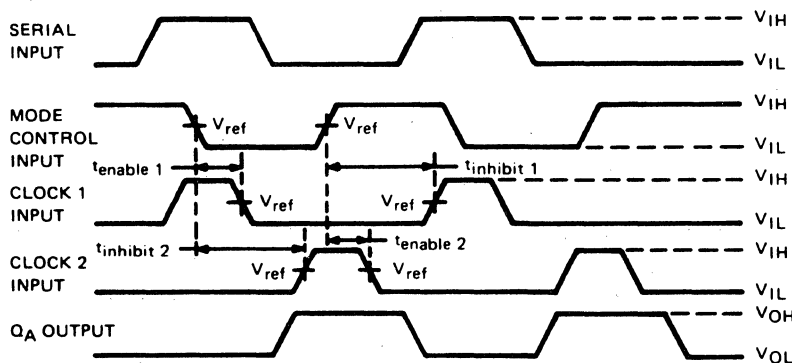


PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, and $Z_{out} \approx 50 \Omega$. For the data pulse generator, PRR = 500 kHz; for the clock pulse generator, PRR = 1 MHz. When testing f_{max} , vary PRR. $t_w(data) \geq 20$ ns, $t_w(clock) \geq 15$ ns.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N916 or 1N3064.
- D. $V_{ref} = 1.3$ V.

VOLTAGE WAVEFORMS
FIGURE 1—SWITCHING TIMES



- NOTES: A. Input A is at a low level.
- B. $V_{ref} = 1.3$ V.

VOLTAGE WAVEFORMS
FIGURE 2—CLOCK ENABLE/INHIBIT TIMES

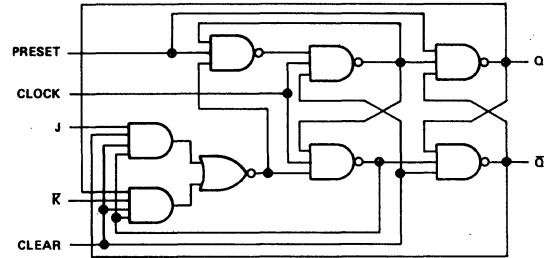


DESCRIPTION

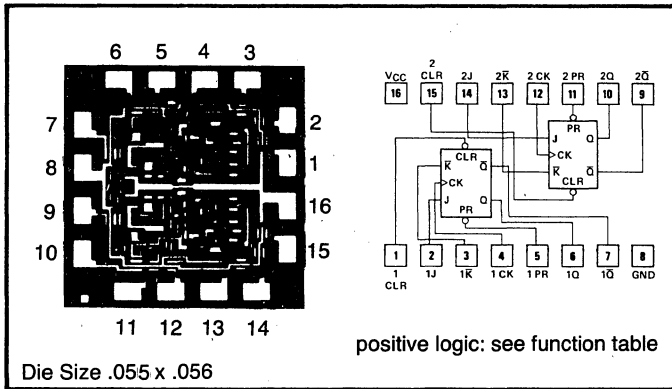
This monolithic dual J-K edge-triggered flip-flop features individual J, K, clock, preset, and clear inputs. A low level at preset or clear sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs.

The J and K data inputs simplify hardware design as a D-type flip-flop can be implemented by simply tying the J and K inputs together.

LOGIC DIAGRAM (1/2)



PIN-OUT DIAGRAM



FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q ₀	Q̄ ₀
H	H	↑	H	H	H	L
H	H	L	X	X	Q ₀	Q̄ ₀

H = high level (steady state)
 L = low level (steady state)
 X = irrelevant
 ↑ = transition from low to high level
 Q₀ = the level of Q before the indicated steady-state input conditions were established
 TOGGLE: each output changes to the complement of its previous level on each ↑ clock transition.
 *This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V _{CC}	4.5	5	5.5	V
Normalized fan-out from each output, N	High logic level		20	
	Low logic level		20	
Clock frequency, f _{clock}	0		30	MHz
Width of clock pulse, t _{w(clock)} (High)				ns
Width of preset pulse, t _{w(preset)} (Low)				ns
Width of clear pulse, t _{w(clear)} (Low)				ns
Input setup time, t _{setup}				ns
Input hold time, t _{hold}				ns
Operating free-air temperature, T _A	-55		125	°C

t_{setup} is the minimum time required for the correct logic level to be present at the J or K input prior to the rising edge of the clock in order to be recognized and transferred to the outputs.

t_{hold} is the minimum time required for the logic level to be maintained at the J or K input after the clock transition in order to insure recognition. This device requires no hold time.



Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions†		Min	Typ‡	Max	Unit
V _{IH}	High-level input voltage			2			V
V _{IL}	Low-level input voltage					0.7	V
V _I	Input clamp voltage	V _{CC} = MIN,	I _I = -18 mA			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = V _{IL max} ,	V _{IH} = 2 V, I _{OH} = -400 μA	2.5	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL max}	I _{OL} = 4 mA	0.25	0.4		V
			I _{OL} = 8 mA	0.3	0.45		
I _I	Input current at maximum input voltage	J or K	V _{CC} = MAX, V _I = 5.5 V			0.1	mA
		Clock or preset				0.2	
		Clear				0.4	
I _{IH}	High-level input current	J or K	V _{CC} = MAX, V _I = 2.7 V			20	μA
		Clock or preset				40	
		Clear				80	
I _{IL}	Low-level input current	J or K	V _{CC} = MAX, V _I = 0.4 V			-0.4	mA
		Clock or preset				-0.8	
		Clear				-1.6	
I _{OS}	Short-circuit output current§	V _{CC} = MAX		-15		-100	mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 1			4	8	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

NOTE 2:

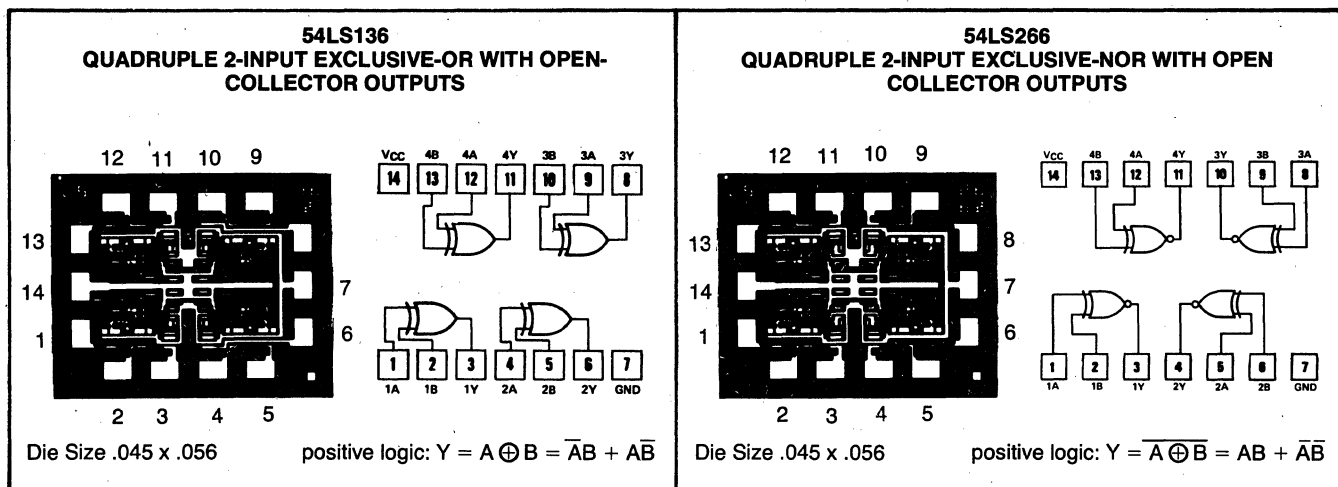
I_{CC} is measured with outputs open, clock grounded, and J, K, preset, and clear at 4.5 V.

Switching Characteristics, V_{CC} = 5 V, T_A = 25°C

Parameter		Test Conditions		Min	Typ	Max	Unit
f _{max}	Maximum clock frequency			30	45		MHz
t _{PLH}	Propagation delay time, low-to-high-level output from clear or preset				10	15	ns
t _{PHL}	Propagation delay time, high-to-low-level output from clear or preset	CK Low	C _L = 15 pF, R _L = 2 kΩ,		12	18	ns
		CK High			16	24	
t _{PLH}	Propagation delay time, low-to-high-level output from clock	See Fig. A on page 373			12	18	ns
t _{PHL}	Propagation delay time, high-to-low-level output from clock				14	22	ns



PIN-OUT AND LOGIC DIAGRAMS



Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output voltage, V_{OH}			5.5	V
Low-level output current, I_{OL}			18	mA
Operating free-air temperature, T_A	-55		125	°C

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.7	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, V_{OH} = 5.5 \text{ V}$			100	μA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$	0.3	0.45	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.2	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.6	mA
I_{CC} Supply current (LS266)	$V_{CC} = \text{MAX}, \text{ See Note 1}$		8	13	mA
I_{CC} Supply current (LS136)			6.1	10	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 1

I_{CC} is measured with one input of each gate at 4.5 V, the other inputs grounded, and the outputs open.

Switching Characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

Parameter*	From	Test Conditions	Min	Typ	Max	Unit
t_{PLH}	A or B	Other input low $C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$			23	ns
t_{PHL}					23	
t_{PLH}	A or B	Other input high See Fig. A on page 373			23	ns
t_{PHL}					23	

* t_{PLH} ≡ propagation delay time, low-to-high level output. t_{PHL} ≡ propagation delay time, high-to-low-level output.



FEATURES

- 54LS138: 3-Line-to-8-Line Decoder
1-of-8 Demultiplexer
- 54LS139: Dual 2-Line-to-4-Line Decoder
Dual 1-of-4 Demultiplexer
- 54LS138 is expandable to a 5-lines-to-32-lines decoder using 4 54LS138's and one inverter.

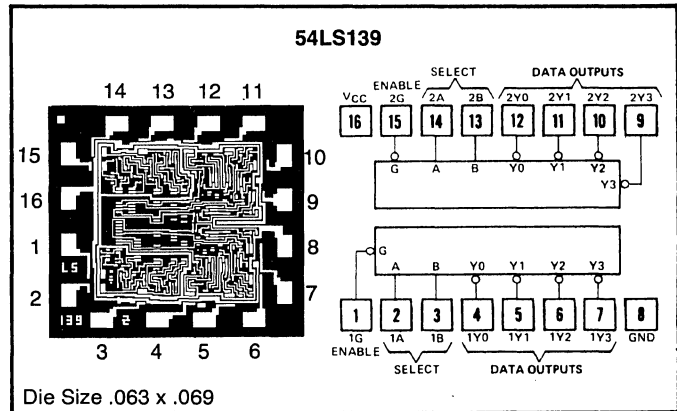
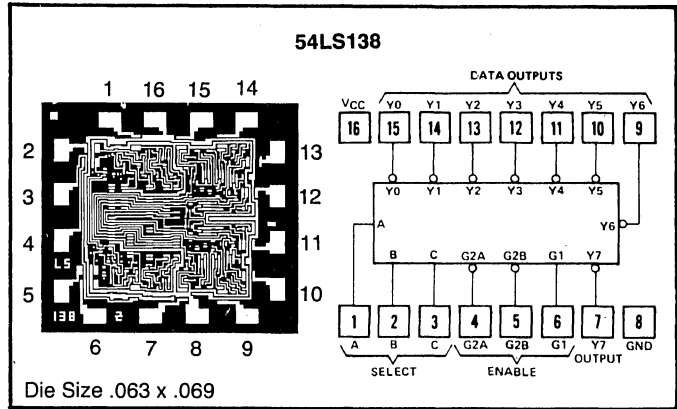
DESCRIPTION

The 54LS138 decodes one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The 54LS139 comprises two individual two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

These circuits are designed to be used in high-performance memory-decoding and data-routing applications requiring very short delay times.

PIN-OUT DIAGRAMS



54LS138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B
H = high level, L = low level, X = irrelevant

54LS139
FUNCTION TABLE (1/2)

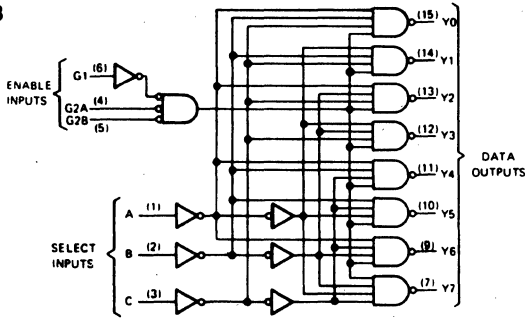
INPUTS			OUTPUTS			
ENABLE	SELECT					
	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

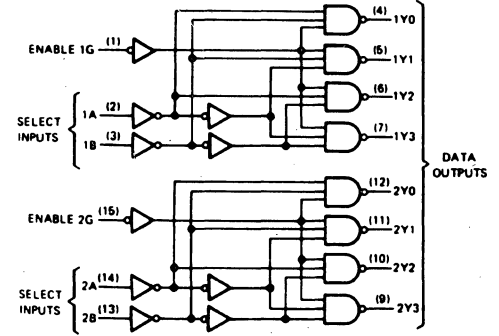


LOGIC DIAGRAMS

54LS138



54LS139



Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			-400	μA
Low-level output current, I_{OL}			18	mA
Operating free-air temperature, T_A	-55		125	$^{\circ}C$

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.7	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{ILmax}, I_{OH} = -400 \mu A$	2.5	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$		0.25	0.4	V
	$V_{IL} = V_{ILmax}, I_{OL} = 8 \text{ mA}$		0.3	0.45	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.36	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-6		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ Outputs enabled and open	'LS138	6.3	10	mA
		'LS139	6.8	11	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$.

§Not more than one output should be shorted at a time.

Switching Characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$

Parameter†	From (Input)	To (Output)	Levels of Delay	Test Conditions	54LS138			54LS139			Unit
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Binary Select	Any	2	$C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega,$ See Fig. A on page 373	11	16		12	17		ns
t_{PHL}					14	20		12	17		ns
t_{PLH}			3		16	24		15	22		ns
t_{PHL}					19	27		17	25		ns
t_{PLH}	Enable	Any	2		11	15		11	15		ns
t_{PHL}					16	24		11	16		ns
t_{PLH}			3		14	18					ns
t_{PHL}					22	28					ns

† t_{PLH} propagation delay time, low-to-high level output; t_{PHL} propagation delay time, high-to-low-level output.



8-Line-To-1-Line Multiplexers

54LS151 54LS152

DIGITAL

Raytheon Semiconductor

FEATURES

- Select one of eight data sources
- Perform parallel-to-serial conversion
- 54LS151 has complementary outputs;
- 54LS152 has inverting output only
- 54LS151 has strobe input

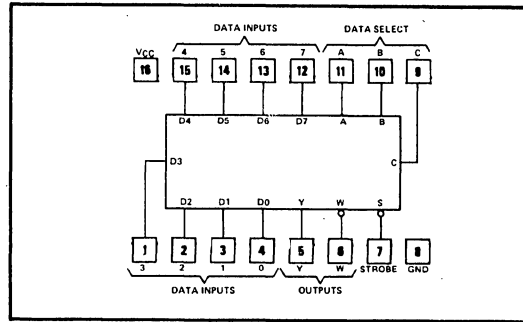
DESCRIPTION

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources. The 54LS151 has a strobe input which must be at a low logic level to enable the device. A high level at the strobe forces the W output high, and the Y output low.

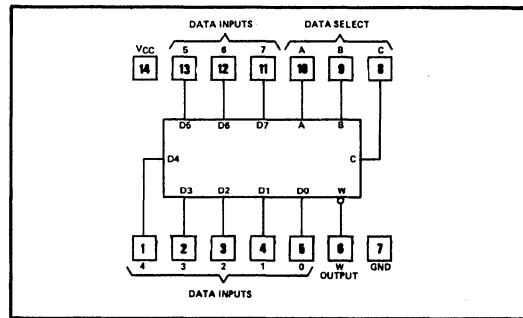
The 54LS151 features complementary W and Y outputs whereas the 54LS152 has an inverted (W) output only.

PIN-OUT DIAGRAMS

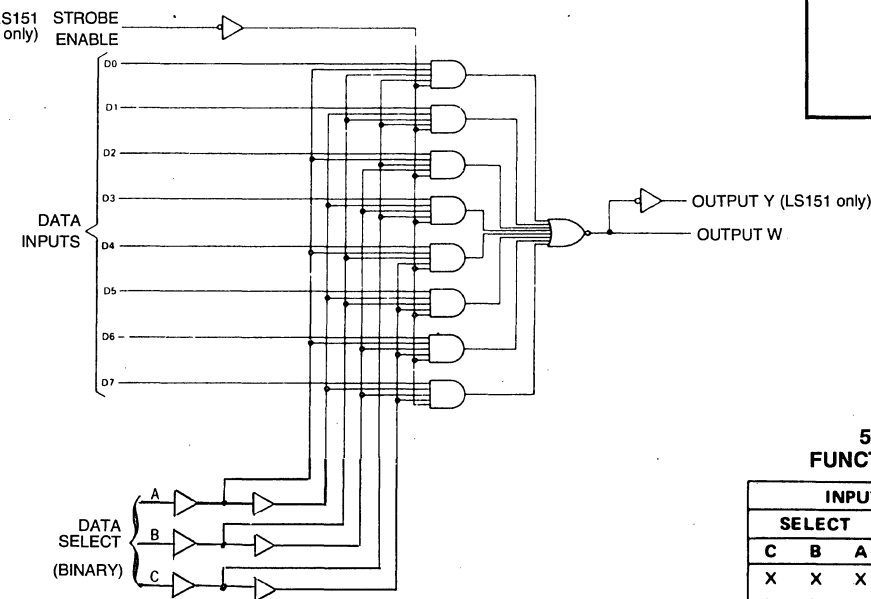
54LS151



54LS152



LOGIC DIAGRAM



54LS151
FUNCTION TABLE

SELECT			STROBE S	OUTPUTS	
C	B	A		Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

54LS152
FUNCTION TABLE

SELECT INPUTS			OUTPUT
C	B	A	W
L	L	L	$\overline{D0}$
L	L	H	$\overline{D1}$
L	H	L	$\overline{D2}$
L	H	H	$\overline{D3}$
H	L	L	$\overline{D4}$
H	L	H	$\overline{D5}$
H	H	L	$\overline{D6}$
H	H	H	$\overline{D7}$

H = high level, L = low level, X = irrelevant
D0, D1 . . . D7 = the level of the D respective input



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Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			-400	μA
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	-55		125	$^{\circ}C$

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.7	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL\text{max}}$, $I_{OH} = -400 \mu A$	2.5	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL\text{max}}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$	0.3	0.45	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.4	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-15		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, Outputs open, All inputs at 4.5 V	54LS151	6.0	10	mA
		54LS152	5.6	9	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}C$.

§Not more than one output should be shorted at a time.

Switching Characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}C$

Parameter†	From (Input)	To (Output)	Test Conditions	Min	Typ	Max *	Unit
t_{PLH}	A, B, or C (4 levels)	Y (54LS151 only)	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Fig. A on page 373			43	ns
t_{PHL}						30	
t_{PLH}	A, B, or C (3 levels)	W				23	ns
t_{PHL}						32	
t_{PLH}	Strobe	Y (54LS151 only)				42	ns
t_{PHL}						32	
t_{PLH}	Strobe	W (54LS151 only)				24	ns
t_{PHL}						30	
t_{PLH}	Any D	Y (54LS151 only)				32	ns
t_{PHL}						26	
t_{PLH}	Any D	W			21	ns	
t_{PHL}					20		

† t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

*Tentative data, subject to change without notice.

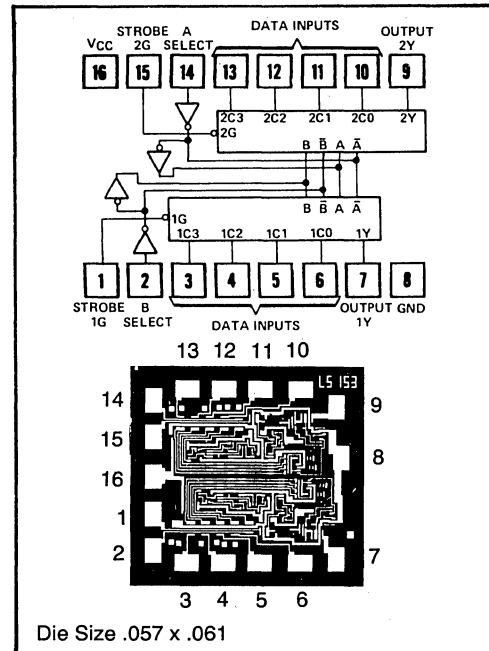
FEATURES

- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe (Enable) line provided for cascading (N lines to n lines)
- Non-inverting

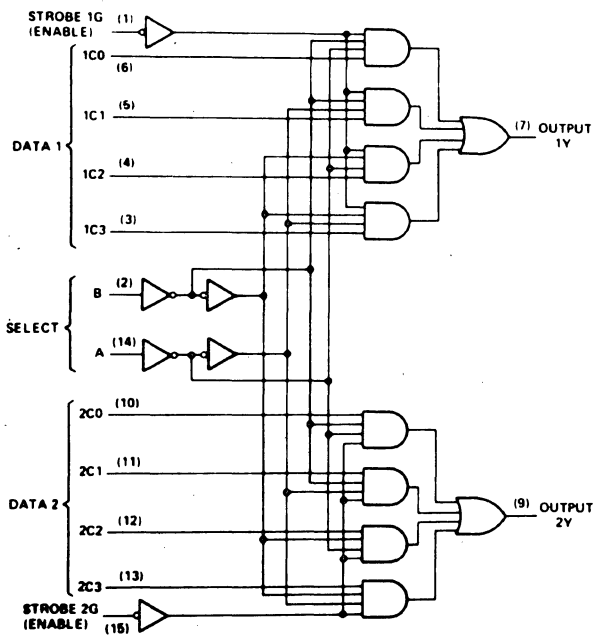
DESCRIPTION

The 54LS153 is a high speed Dual 4-Line-to-1-Line Multiplexer with common select inputs and separate strobe (enable) inputs for each half. Each half can select one bit of four and present it at the output in non-inverted form.

PIN-OUT DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant



Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			-400	μA
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	-55		125	$^{\circ}C$

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.7	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = V_{ILmax}$, $V_{IH} = 2 \text{ V}$, $I_{OH} = -400 \mu A$	2.5	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = V_{ILmax}$, $V_{IH} = 2 \text{ V}$		0.25	0.4	V
	$I_{OL} = 4 \text{ mA}$		0.3		
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7.0 \text{ V}$			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.36	mA
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	-6		-100	mA
I_{CCL} Supply current, output low	$V_{CC} = \text{MAX}$, See Note 1		6.2	10	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}C$.

§Not more than one output should be shorted at a time.

NOTE: 1

I_{CCL} is measured with the outputs open and all inputs grounded.

Switching Characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}C$

Parameter¶	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Unit
t_{PLH}	Data	Y	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Fig. A on page 373		7	13	ns
t_{PHL}	Data	Y			12	19	ns
t_{PLH}	Select	Y			16	24	ns
t_{PHL}	Select	Y			20	29	ns
t_{PLH}	Strobe	Y			13	20	ns
t_{PHL}	Strobe	Y			17	24	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output
 ¶ t_{PHL} = propagation delay time, high-to-low-level output

Dual 2-Line-To-4-Line Decoders/Demultiplexers

54LS155 54LS156

DIGITAL
Raytheon Semiconductor

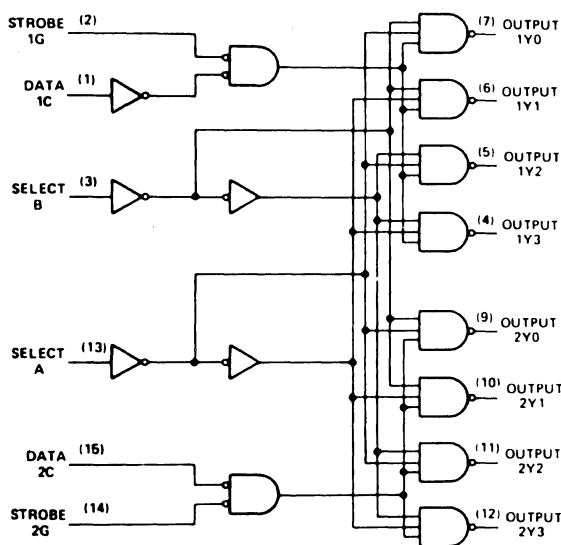
FEATURES

- 54LS156 has open-collector outputs
- Applications:
 - Dual 2-Line-to-4-Line Decoder
 - Dual 1-Line-to-4-Line Demultiplexer
 - 3-Line-to-8-Line Decoder
 - 1-Line-to-8-Line Demultiplexer

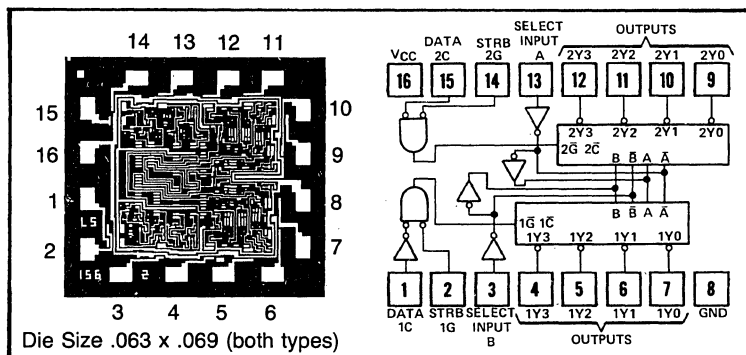
DESCRIPTION

These circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. Input clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design.

LOGIC DIAGRAM



PIN-OUT DIAGRAM



FUNCTION TABLES
2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT	STROBE	DATA					
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT	STROBE	DATA					
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

FUNCTION TABLE
3-LINE-TO-8-LINE DECODER
OR 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT	STROBE OR DATA										
C [†]	B	A	G [‡]	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	L	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H
L	H	H	L	L	H	H	H	L	H	H	H
H	L	L	L	L	H	H	H	H	L	H	H
H	L	H	L	L	H	H	H	H	H	L	H
H	H	L	L	L	H	H	H	H	H	H	L
H	H	H	L	L	H	H	H	H	H	H	L
X	X	X	H	L	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together
H = high level, L = low level, X = irrelevant



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54LS155 54LS156

Dual 2-Line-To-4-Line
Decoders/Demultiplexers

Recommended Operating Conditions

	54LS155			Unit	54LS156			Unit
	Min	Nom	Max		Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	V	4.5	5	5.5	V
High-level output current, I_{OH} ; or output voltage, V_{OH}			-400	μA			5.5	V
Low-level output, I_{OL}			8	mA			8	mA
Operating free-air temperature, T_A	-55		125	$^{\circ}C$	-55		125	$^{\circ}C$

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	54LS155			54LS156			Unit
		Min	Typ‡	Max	Min	Typ‡	Max	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.7	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $I_{OH} = -400 \mu A$	2.5	3.4					V
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$, $V_{OH} = 5.5 \text{ V}$						100	μA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL \text{ max}}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	0.25	0.4	V	
		$I_{OL} = 8 \text{ mA}$	0.3	0.45	0.3	0.45		
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.36			-0.36	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-6		-100				mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 1		6.1	10		6.1	10	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}C$.

§Not more than one output should be shorted at a time.

NOTE 1:

 I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.Switching Characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}C$

Parameter¶	From (Input)	To (Output)	Levels of Logic	Test Conditions	54LS155			54LS156			Unit
					Min	Typ	Max	Min	Typ	Max	
t_{PLH}	2C, 1G, or 2G	Y	2	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Figs. A & B on page 373		11	15		22	30	ns
t_{PHL}	2C, 1G, or 2G	Y	2			13	20		16	24	ns
t_{PLH}	A or B	Y	3			14	18		27	37	ns
t_{PHL}	A or B	Y	3			18	27		22	30	ns
t_{PLH}	1C	Y	3			13	18		25	34	ns
t_{PHL}	1C	Y	3			16	24		23	31	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output¶ t_{PHL} = propagation delay time, high-to-low-level output

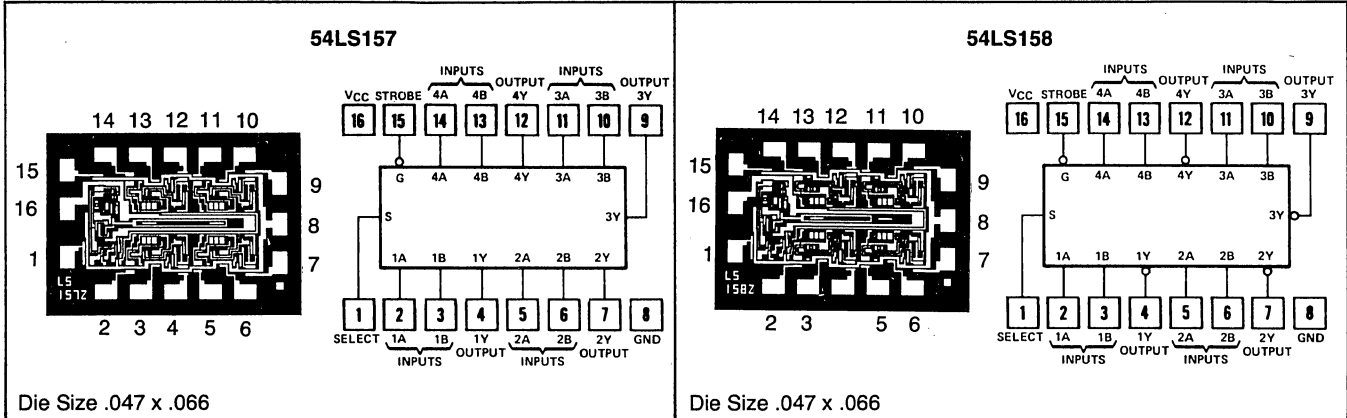
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DESCRIPTION

These data selectors/multiplexers select a 4-bit word from one of two sources and present it at the four outputs. The 54LS157 presents true data; the 54LS158 presents inverted data.

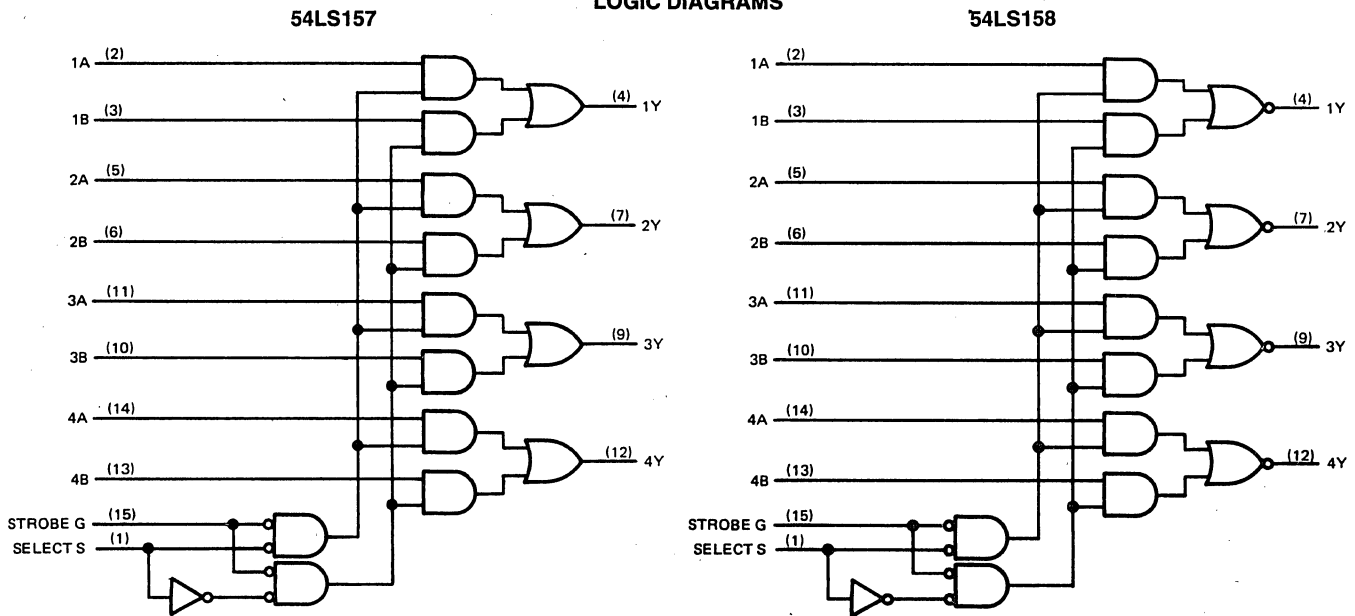
PIN-OUT DIAGRAMS



Die Size .047 x .066

Die Size .047 x .066

LOGIC DIAGRAMS



FUNCTION TABLE

STROBE	SELECT	INPUTS		OUTPUT Y	
		A	B	54LS157	54LS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = irrelevant
 Low level at S selects A inputs
 High level at S selects B inputs
 Strobe is active low



Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			-400	μA
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	-55		125	$^{\circ}C$

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions†		Min	Typ‡	Max	Unit
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.7	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN},$	$I_I = -18 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN},$ $V_{IL} = \text{MAX},$	$V_{IH} = 2 \text{ V},$ $I_{OH} = -400 \mu A$	2.5	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN},$ $V_{IL} = \text{MAX}$	$V_{IH} = 2 \text{ V},$ $I_{OL} = 4 \text{ mA}$		0.25	0.4	V
				$I_{OL} = 8 \text{ mA}$		0.3	
I_I	Input current at maximum input voltage	S or G input	$V_{CC} = \text{MAX},$ $V_I = 7 \text{ V}$			0.2	mA
		A or B input				0.1	
I_{IH}	High-level input current	S or G input	$V_{CC} = \text{MAX},$ $V_I = 2.7 \text{ V}$			40	μA
		A or B input				20	
I_{IL}	Low-level input current	S or G input	$V_{CC} = \text{MAX},$ $V_I = 0.4 \text{ V}$			-0.8	mA
		A or B input				-0.4	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$		-15		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 1		'LS157	9.7	16	mA
				'LS158	4.8	8	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
 ‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$.
 §Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.
 NOTE: 1
 I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

Switching Characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$

Parameter¶	From (Input)	Test Conditions	54LS157			54LS158			Unit
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Data	$C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega,$ See Fig. A on page 373	5	10		7	13	ns	
t_{PHL}			7	14		5	10		
t_{PLH}	Strobe		13	23		8	18	ns	
t_{PHL}			8	16		12	22		
t_{PLH}	Select		10	20		11	20	ns	
t_{PHL}			11	20		10	20		

¶ t_{PLH} = propagation delay time, low-to-high-level output
 ¶ t_{PHL} = propagation delay time, high-to-low-level output



Synchronous BCD Decade Counters

54LS160 54LS162

Synchronous 4-Bit Binary Counters

54LS161 54LS163

FEATURES

- 54LS160, 161: Synchronous with direct clear
- 54LS162, 163: Fully synchronous
- Synchronous counting and loading
- Expandable to N-Bit synchronous counter
- Edge-triggered operation

DESCRIPTION

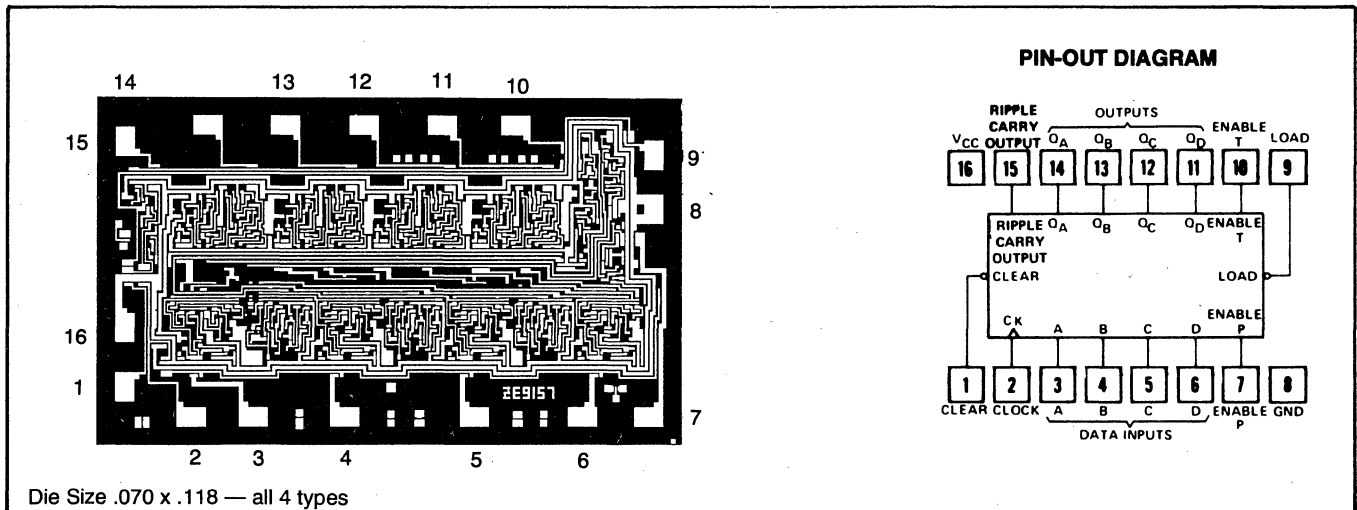
These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 54LS160 and 54LS162 are decade counters and the 54LS161 and 54LS163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the 54LS160 and 54LS161 is

asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function for the 54LS162 and 54LS163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages.

These counters feature a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.



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54LS160 54LS162

54LS161 54LS163

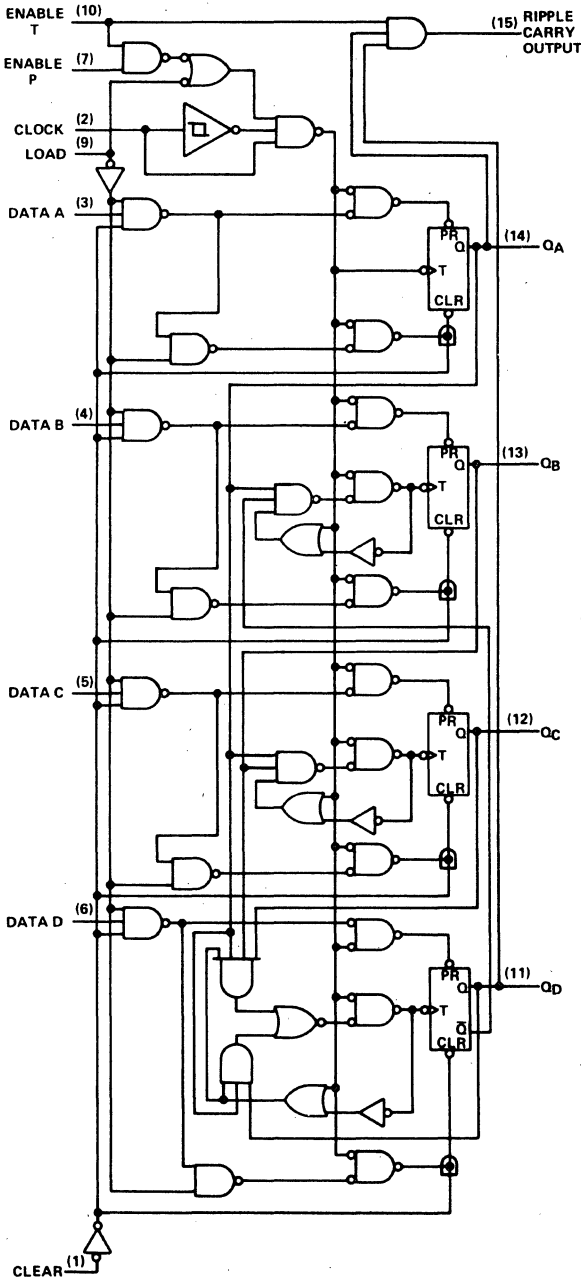
Synchronous BCD Decade Counters

Synchronous 4-Bit Binary Counters

LOGIC DIAGRAMS

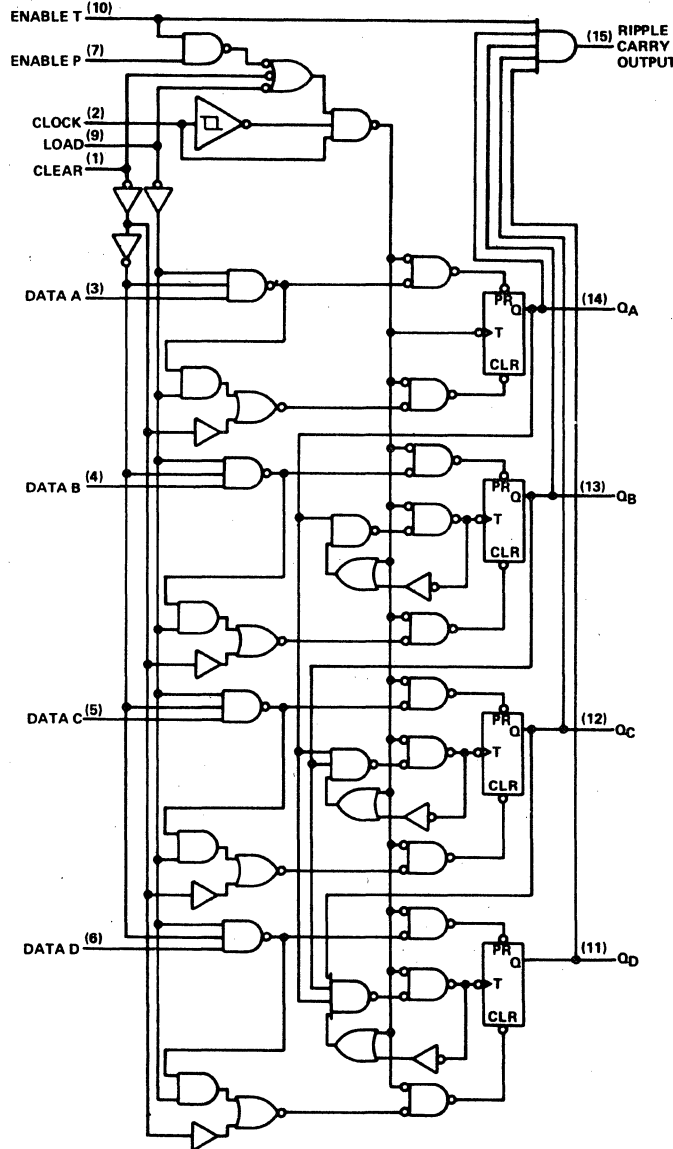
54LS160 Synchronous Decade Counter

The 54LS162 synchronous decade counter is similar, however the clear is synchronous as shown for the 54LS163 binary counter below.



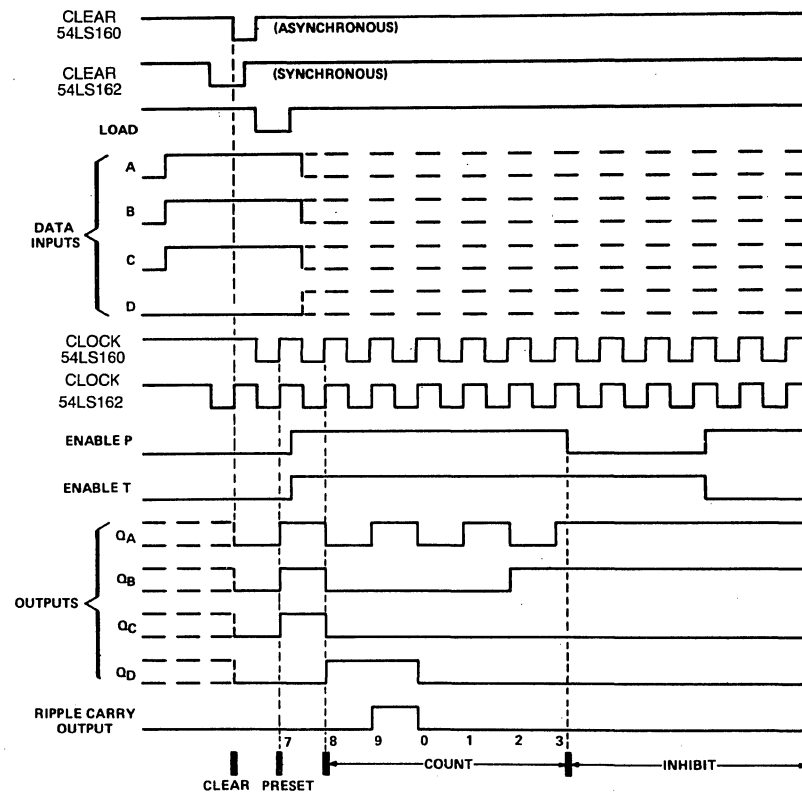
54LS163 SYNCHRONOUS BINARY COUNTER

The 54LS161 synchronous binary counter is similar, however the clear is asynchronous as shown for the 54LS160 decade counter below.



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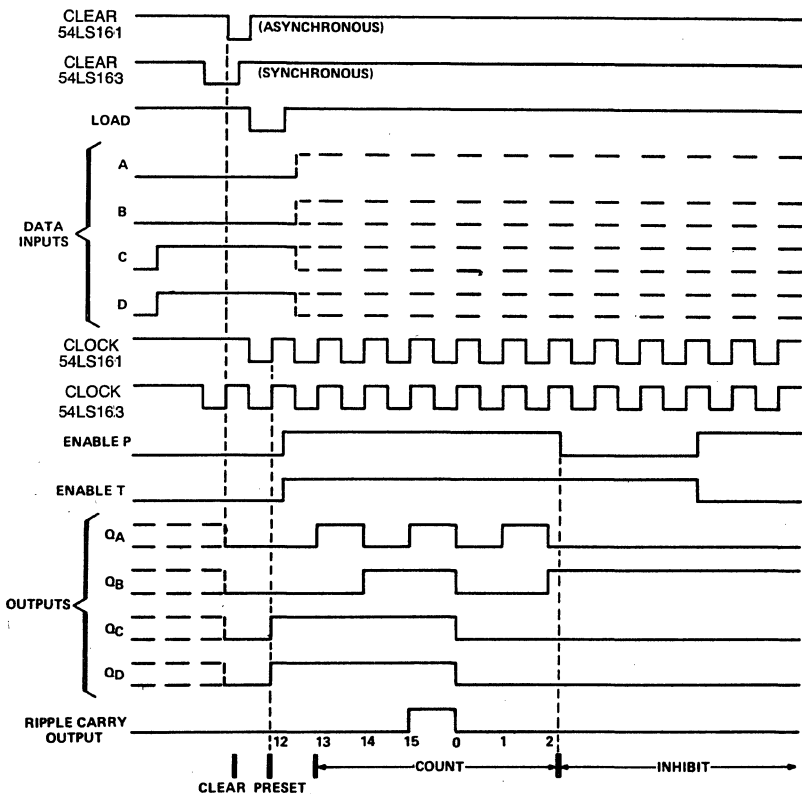
TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES



54LS160, 54LS162

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit



54LS161, 54LS163

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen; fourteen fifteen, zero, one, and two
4. Inhibit



54LS160 54LS162

Synchronous BCD Decade Counters

54LS161 54LS163

Synchronous 4-Bit Binary Counters

Recommended Operating Conditions

		Min	Nom	Max	Unit
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level output current, I_{OH}				-400	μA
Low-level output current, I_{OL}				4	mA
Clock frequency, f_{clock}		0		25	MHz
Width of clock pulse, $t_{w(clock)}$		25			ns
Width of clear pulse, $t_{w(clear)}$		20			ns
Setup time, t_{setup} (see Figures 1 and 2)	Data inputs A, B, C, D	0			ns
	Enable P or T	20			
	Load	20			
	Clear ^o	20			
Hold time, t_{hold}	Data inputs A, B, C, D	25 [¶]			ns
	Other inputs	10 [¶]			
Operating free-air temperature, T_A		-55		125	$^{\circ}C$

^oThis applies only for 54LS162 and 54LS163, which have synchronous clear inputs.

[¶]The minimum hold time is as specified or as long as the clock input takes to rise from 0.8 V to 2 V, whichever is longer.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions [†]		Min	Typ [‡]	Max	Unit		
V_{IH}	High-level input voltage			2			V		
V_{IL}	Low-level input voltage					0.7	V		
V_I	Input clamp voltage	$V_{CC} = \text{MIN},$	$I_I = -18 \text{ mA}$			-1.5	V		
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN},$	$V_{IH} = 2 \text{ V},$	2.5	3.4		V		
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN},$	$V_{IH} = 2 \text{ V},$			$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
						$I_{OL} = 8 \text{ mA}$	0.3	0.45	
I_I	Input current at maximum input voltage	Data or enable P	$V_{CC} = \text{MAX},$	$V_I = 7 \text{ V}$				mA	0.1
		Load, clock, or enable T							0.2
		Clear (LS160, LS161)							0.1
		Clear (LS162, LS163)							0.2
I_{IH}	High-level input current	Data or enable P	$V_{CC} = \text{MAX},$	$V_I = 2.7 \text{ V}$				μA	20
		Load, clock, or enable T							40
		Clear (LS160, LS161)							20
		Clear (LS162, LS163)							40
		Data or enable P							-0.4
I_{IL}	Low-level input current	Load, clock, or enable T	$V_{CC} = \text{MAX},$	$V_I = 0.4 \text{ V}$				mA	-0.8
		Clear (LS160, LS161)							-0.4
		Clear (LS162, LS163)							-0.8
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$		-15		-100	mA		
I_{CCH}	Supply current, all outputs high	$V_{CC} = \text{MAX},$ See Note 1			18	31	mA		
I_{CCL}	Supply current, all outputs low	$V_{CC} = \text{MAX},$ See Note 2			19	32	mA		

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$.

[§]Not more than one output should be shorted at a time.

NOTES:

- I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
- I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.



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Switching Characteristics, $V_{CC} = 5 V, T_A = 25^\circ C$

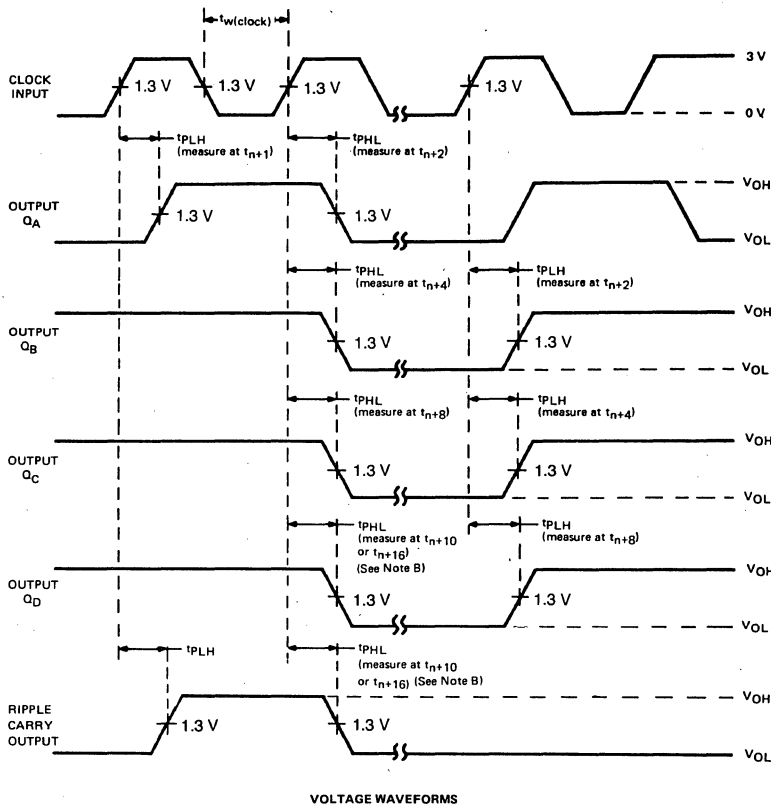
Parameter†	From (Input)	To (Output)	Test Conditions	Min	Typ	Max*	Unit
f_{MAX}				25	32		MHz
t_{PLH}	Clock	Ripple carry	$C_L = 15 pF,$ $R_L = 2 k\Omega,$ See Figures 1 and 2 and Notes 3 and 4		23	35	ns
t_{PHL}					23	35	
t_{PLH}	Clock (load input high)	Any Q			16	24	ns
t_{PHL}					18	27	
t_{PLH}	Clock (load input low)	Any Q			17	25	ns
t_{PHL}					19	29	
t_{PLH}	Enable T	Ripple carry		15	23	ns	
t_{PHL}				15	23		
t_{PHL}	Clear	Any Q		26	38	ns	

† f_{max} = Maximum clock frequency
 t_{PLH} = propagation delay time, low-to-high-level output.
 t_{PHL} = propagation delay time, high-to-low-level output.

*Tentative date, subject to change without notice

NOTES:
 3. Load circuit is shown on page
 4. Propagation delay for clearing is measured from the clear input for the 'LS160 and 'LS161 or from the clock input transition for the 'LS162 and 'LS163.

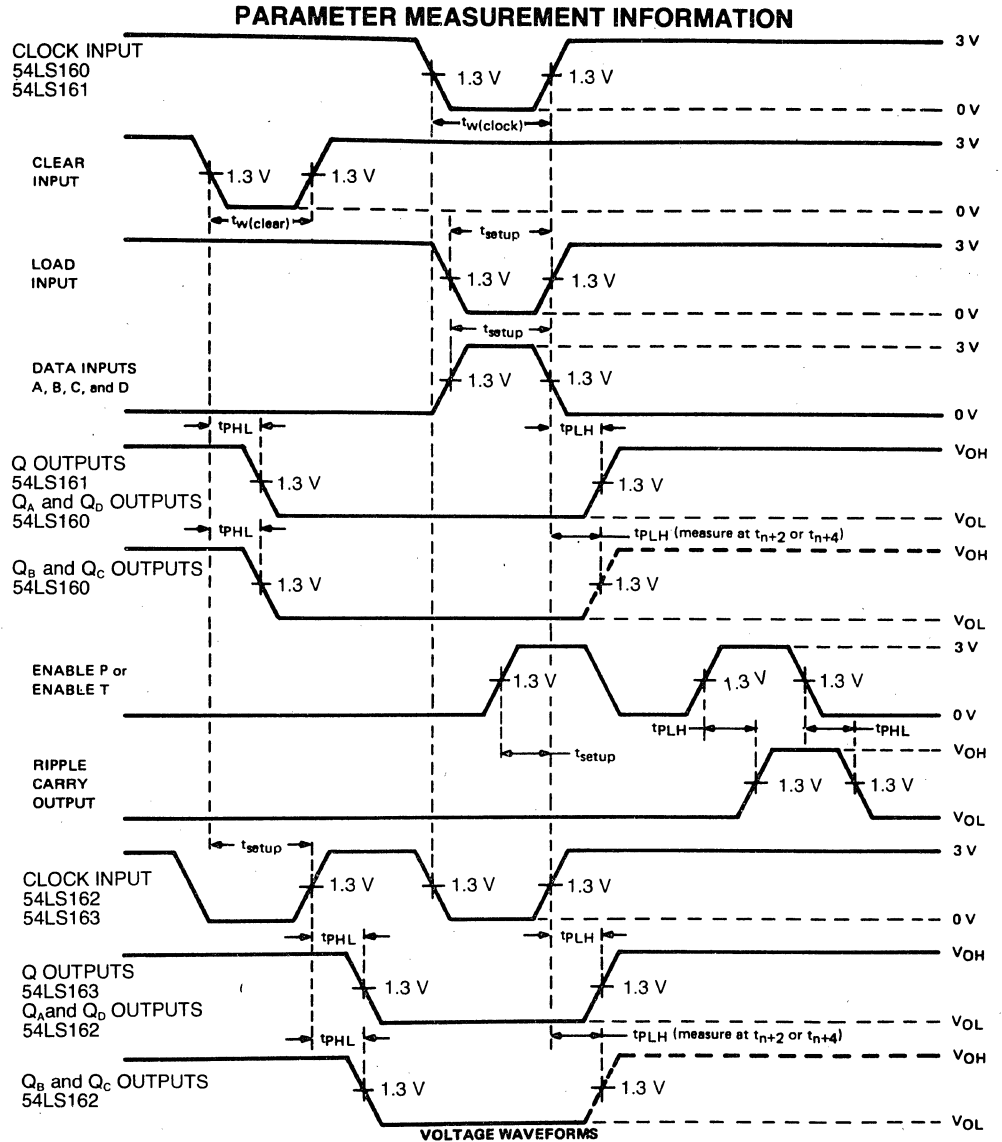
**FIGURE 1
PARAMETER MEASUREMENT INFORMATION**



NOTES:
 A. The input pulses are supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{out} \approx 50 \Omega$; $t_r \leq 15 ns$, $t_f \leq 6 ns$. Vary PRR to measure f_{max} .
 B. Outputs Q_n and carry are tested at t_{n+10} 54LS160, 54LS162, and at t_{n+16} for 54LS161, 54LS163 where t_n is the bit time when all outputs are low.



FIGURE 2



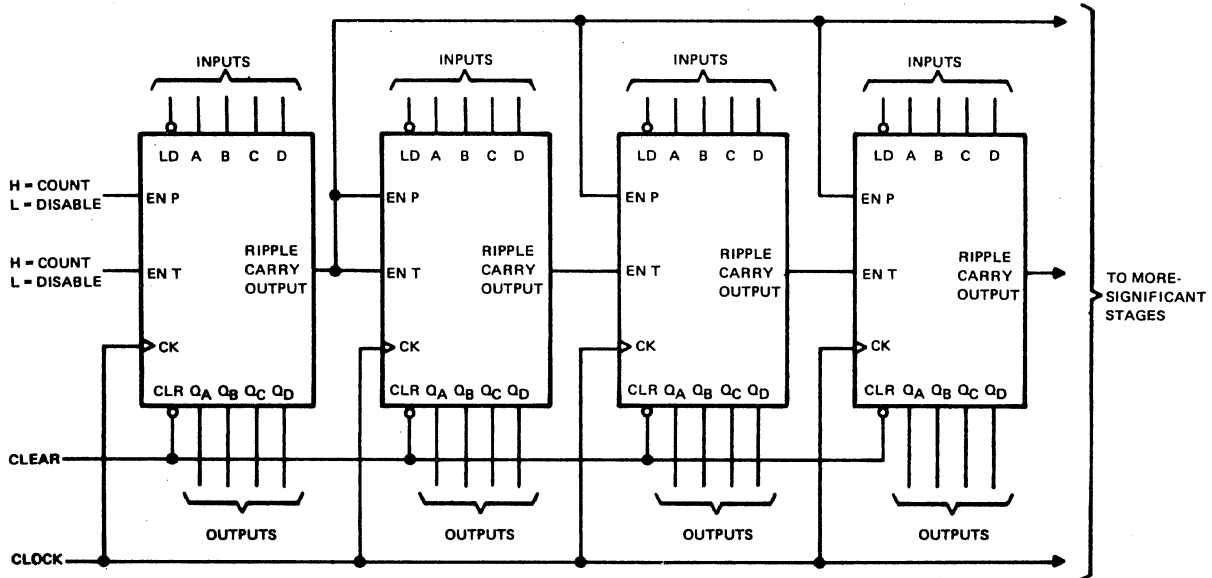
NOTES:

- A. The input pulses are supplied by generators having the following characteristics: $\text{PRR} \leq 1 \text{ MHz}$, $\text{duty cycle} \leq 50\%$, $Z_{\text{out}} \approx 50 \Omega$; $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$.
- B. Enable P and enable T setup times are measured at $t_n=0$.



N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 54LS160 or 54LS162 will count in BCD and the 54LS163 will count in binary. Virtually any count mode (modulo-N, N_1 -to- N_2 , N_1 -to-maximum) can be used with this fast look-ahead circuit.



DIGITAL

Raytheon Semiconductor



54LS174

Hex D-Type Flip-Flops With Clear

54LS175

Quadruple D-Type Flip-Flops With Clear

FEATURES

- Positive edge-triggered common clock
- Asynchronous common reset
- Clock-to-output delays of 14 ns

DESCRIPTION

The 54LS174 is a six-bit register with single-rail outputs and the 54LS175 is a four-bit register with complementary outputs. Both consist of D-type flip-flops with a buffered common clock and an asynchronous, active-Low buffered clear.

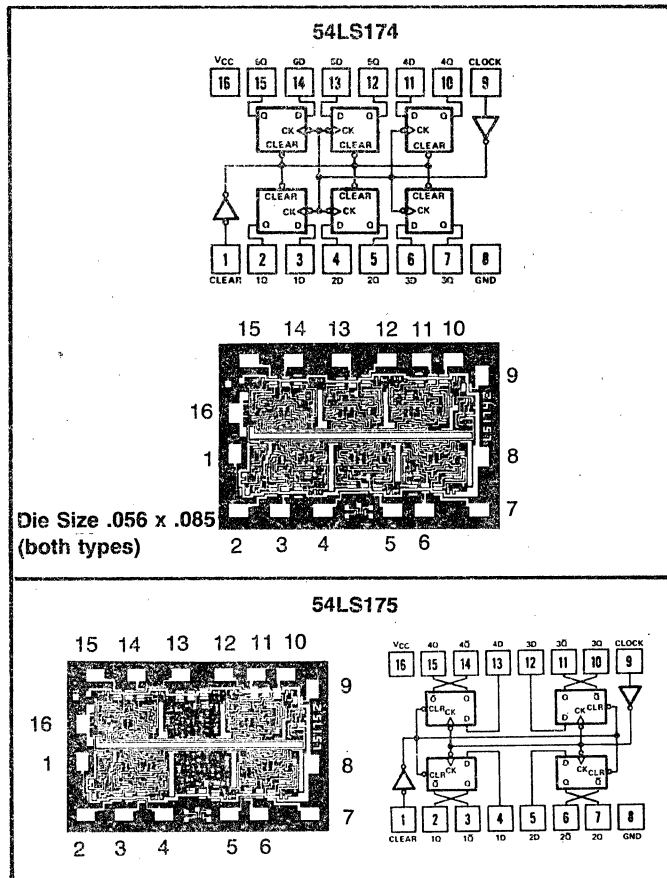
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

FUNCTION TABLE
(EACH FLIP-FLOP)

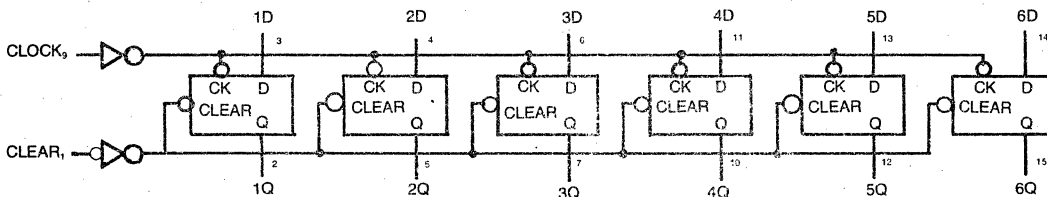
INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	\bar{Q} †
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q ₀	\bar{Q}_0

H = high level (steady state)
 L = low level (steady state)
 X = irrelevant
 ↑ = transition from low to high level
 Q₀ = the level of Q before the indicated steady-state input conditions were established.
 † = 54LS175 only

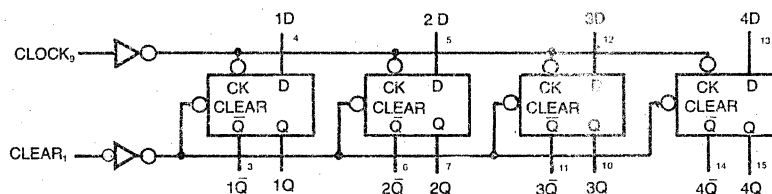
PIN-OUT DIAGRAMS



LOGIC DIAGRAMS
54LS174



54LS175



Recommended Operating Conditions

		Min	Nom	Max	Unit
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level output current, I_{OH}				-400	μ A
Low-level output current, I_{OL}				8	mA
Clock frequency, f_{clock}		0		35	MHz
Width of clock pulse, t_w (Low)		15			ns
Width of clear pulse, t_w (Low)		20			ns
Setup time	Data input, t_{setup}	10			ns
	Clear recovery, t_{rec}	12			ns
Data hold time, t_{hold}		5			ns
Operating free-air temperature, T_A		-55		125	$^{\circ}$ C

t_{setup} is the minimum time required for the correct logic level to be present at the data input prior to the rising edge of the clock in order to be recognized and transferred to the output.

t_{hold} is the minimum time required for the logic level to be maintained at the data input after the rising edge of the clock in order to insure recognition.

t_{rec} is the minimum time required between the end of the clear pulse and the rising edge of the clock in order to transfer High data to the Q output.

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions†		Min	Typ‡	Max	Unit	
V_{IH}	High-level input voltage			2			V	
V_{IL}	Low-level input voltage					0.7	V	
V_i	Input clamp voltage	$V_{CC} = \text{MIN},$	$I_i = -18 \text{ mA}$			-1.5	V	
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN},$	$V_{IH} = 2 \text{ V},$ $V_{IL} = V_{ILmax},$	2.5	3.5		V	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN},$ $V_{IL} = V_{ILmax}$	$V_{IH} = 2 \text{ V},$ $I_{OL} = 4 \text{ mA}$		0.25	0.4	V	
			$I_{OL} = 8 \text{ mA}$		0.3	0.45		
I_i	Input current at maximum input voltage	$V_{CC} = \text{MAX},$	$V_i = 7 \text{ V}$			0.1	mA	
I_{IH}	High-level input current	$V_{CC} = \text{MAX},$	$V_i = 2.7 \text{ V}$			20	μ A	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX},$	$V_i = 0.4 \text{ V}$	Clock, Clear		-0.4	mA	
				Other inputs		-0.36		
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$		-15		-100	mA	
I_{CC}	Supply current	$V_{CC} = \text{MAX},$	See Note 1	'LS174	45	6	26	mA
				'LS175	11	18		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}.$

§Not more than one output should be shorted at a time.

NOTE 1: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

Switching Characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

Parameter		Test Conditions	Min	Typ	Max	Unit
f_{max}	Maximum clock frequency		35	45		MHz
t_{PLH}	Propagation delay time, low-to-high level output clear (54LS175 only)	$C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega,$ See Fig. A on page 373		19	24	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	31	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			14	22	ns



FEATURES

- Provides 16 arithmetic operations
- Provides 16 logic operations
- Full look-ahead for high-speed arithmetic operation on long words

DESCRIPTION

The 54LS181 is an arithmetic logic unit (ALU)/function generator which has a complexity of 75 equivalent gates on a monolithic chip. This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the 54182, full carry look-ahead circuits, high-speed arithmetic operations can be performed.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The 54LS181 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	A ₀	B ₀	A ₁	B ₁	A ₂	B ₂	A ₃	B ₃	F ₀	F ₁	F ₂	F ₃	\bar{C}_n	\bar{C}_{n+4}	X	Y
Active-low data (Table 2)	\bar{A}_0	\bar{B}_0	\bar{A}_1	\bar{B}_1	\bar{A}_2	\bar{B}_2	\bar{A}_3	\bar{B}_3	F ₀	F ₁	F ₂	F ₃	C _n	C _{n+4}	\bar{F}	\bar{G}

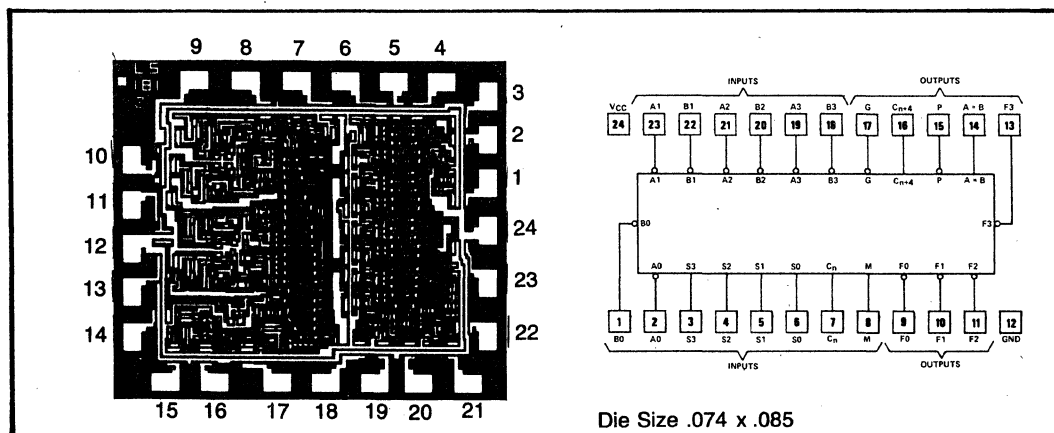
Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1 which requires an end-around or forced carry to provide A-B.

The 54LS181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F₀, F₁, F₂, F₃) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with $C_n = H$ when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S₃, S₂, S₁, S₀ at L, H, H, L, respectively.

INPUT \bar{C}_n	OUTPUT \bar{C}_{n+4}	ACTIVE-HIGH DATA (FIGURE 1)	ACTIVE-LOW DATA (FIGURE 2)
H	H	A ≤ B	A ≥ B
H	L	A > B	A < B
L	H	A < B	A > B
L	L	A ≥ B	A < B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S₀, S₁, S₂, S₃) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

PIN-OUT DIAGRAM



ALU SIGNAL DESIGNATIONS

The SN54LS181 and SN74LS181 can be used with the signal designations of either Figure 1 or Figure 2.

The logic functions and arithmetic operations obtained with signal designations as in Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

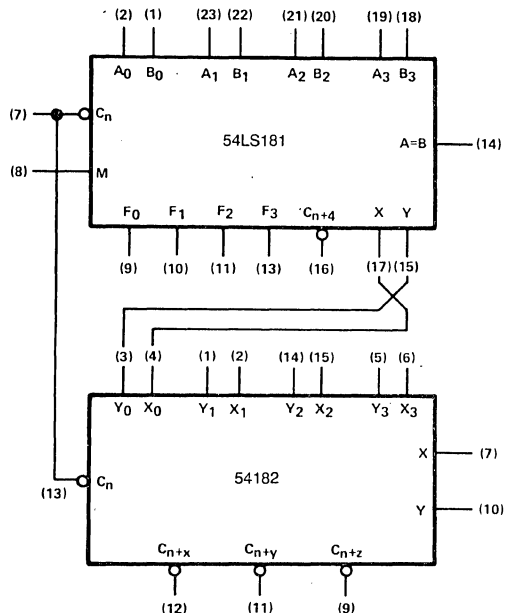


FIGURE 1
(FOR TABLE 1)

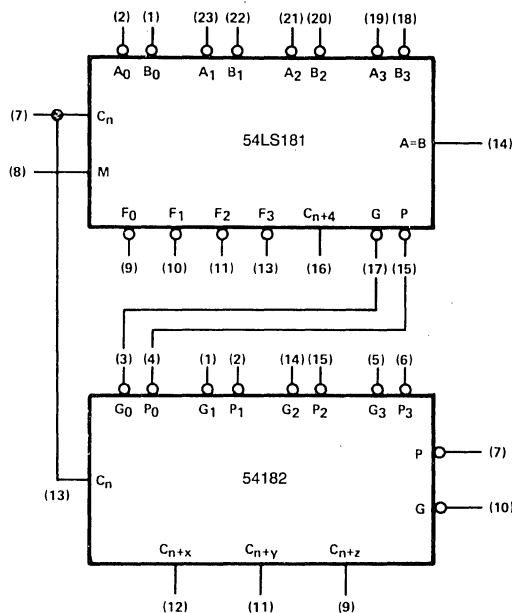


FIGURE 2
(FOR TABLE 2)

TABLE 1

SELECTION S ₃ S ₂ S ₁ S ₀	ACTIVE-HIGH DATA		
	M = H LOGIC FUNCTIONS	M = L: ARITHMETIC OPERATIONS	
		C _n = 0 = H (no carry)	C _n = 1 = H (with carry)
L L L L	F = \bar{A}	F = A	F = A PLUS 1
L L L H	F = $\bar{A} + \bar{B}$	F = A + B	F = (A + B) PLUS 1
L L H L	F = $\bar{A} B$	F = A + \bar{B}	F = (A + \bar{B}) PLUS 1
L L H H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L H L L	F = $\bar{A} \bar{B}$	F = A PLUS $\bar{A} \bar{B}$	F = A PLUS $\bar{A} \bar{B}$ PLUS 1
L H L H	F = $\bar{A} B$	F = (A + B) PLUS $\bar{A} \bar{B}$	F = (A + B) PLUS $\bar{A} \bar{B}$ PLUS 1
L H H L	F = A \odot B	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = $\bar{A} \bar{B}$	F = $\bar{A} \bar{B}$ MINUS 1	F = $\bar{A} \bar{B}$
H L L L	F = $\bar{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H L L H	F = $\bar{A} \odot B$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = (A + \bar{B}) PLUS AB	F = (A + \bar{B}) PLUS AB PLUS 1
H L H H	F = AB	F = AB MINUS 1	F = AB
H H L L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = A + \bar{B}	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H H H L	F = A + B	F = (A + \bar{B}) PLUS A	F = (A + \bar{B}) PLUS A PLUS 1
H H H H	F = A	F = A MINUS 1	F = A

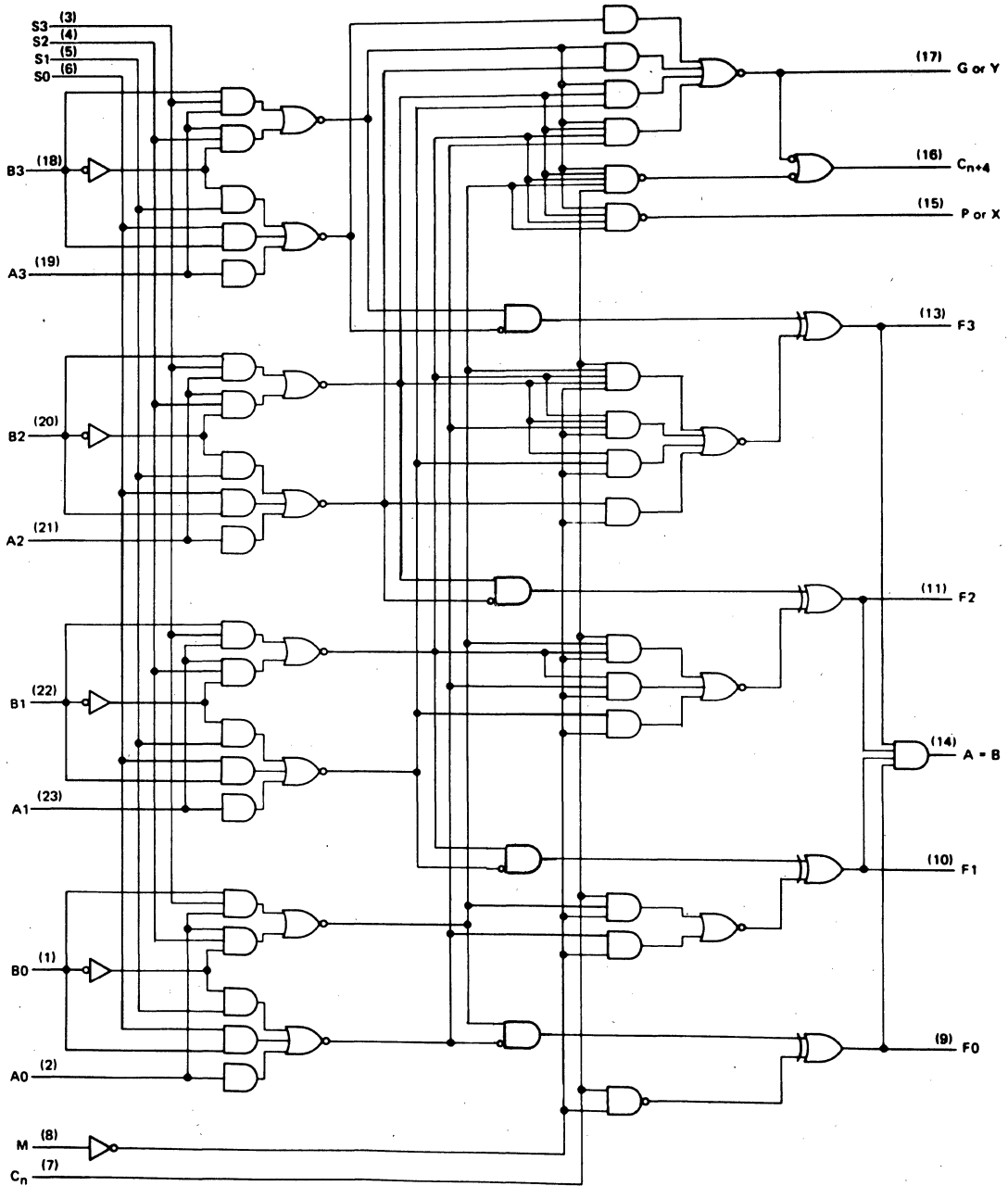
* Each bit is shifted to the next more significant position.

TABLE 2

SELECTION S ₃ S ₂ S ₁ S ₀	ACTIVE-LOW DATA		
	M = H LOGIC FUNCTIONS	M = L: ARITHMETIC OPERATIONS	
		C _n = 0 = L (no carry)	C _n = 1 = H (with carry)
L L L L	F = \bar{A}	F = A MINUS 1	F = A
L L L H	F = $\bar{A} \bar{B}$	F = AB MINUS 1	F = AB
L L H L	F = $\bar{A} + \bar{B}$	F = $\bar{A} \bar{B}$ MINUS 1	F = $\bar{A} \bar{B}$
L L H H	F = 1	F = MINUS 1 (2's COMPL)	F = ZERO
L H L L	F = $\bar{A} + B$	F = A PLUS (A + \bar{B})	F = A PLUS (A + \bar{B}) PLUS 1
L H L H	F = \bar{B}	F = AB PLUS (A + \bar{B})	F = AB PLUS (A + \bar{B}) PLUS 1
L H H L	F = $\bar{A} \odot B$	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A + \bar{B}	F = A + \bar{B}	F = (A + \bar{B}) PLUS 1
H L L L	F = $\bar{A} \bar{B}$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H L L H	F = A \odot B	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = $\bar{A} \bar{B}$ PLUS (A + B)	F = $\bar{A} \bar{B}$ PLUS (A + B) PLUS 1
H L H H	F = A + B	F = A + B	F = (A + B) PLUS 1
H H L L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = $\bar{A} \bar{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H H H L	F = AB	F = $\bar{A} \bar{B}$ PLUS A	F = $\bar{A} \bar{B}$ PLUS A PLUS 1
H H H H	F = A	F = A	F = A PLUS 1



LOGIC DIAGRAM



Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH} (All outputs except A = B)			-400	μA
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	-55		125	$^{\circ}C$

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions†		Min	Typ‡	Max	Unit
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.7	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}$,	$I_I = -18 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage, any output except A = B	$V_{CC} = \text{MIN}$,	$V_{IH} = 2 \text{ V}$, $V_{IL} = V_{ILmax}$,	2.5	3.4		V
I_{OH}	High-level output current, A = B output only	$V_{CC} = \text{MIN}$,	$V_{IH} = 2 \text{ V}$, $V_{IL} = V_{ILmax}$,			100	μA
V_{OL}	Low-level output voltage	All outputs	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{ILmax}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
				$I_{OL} = 8 \text{ mA}$	0.35	0.6	
	Output G			$I_{OL} = 16 \text{ mA}$	0.47	0.7	
I_I	Input current at max. input voltage	Mode input	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			0.1	mA
		Any A or B input			0.3		
		Any S input			0.4		
		Carry input			0.5		
I_{IH}	High-level input current	Mode input	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20	μA
		Any A or B input			60		
		Any S input			80		
		Carry input			100		
I_{IL}	Low-level input current	Mode input	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.36	mA
		Any A or B input			-1.08		
		Any S input			-1.44		
		Carry input			-2		
I_{OS}	Short-circuit output current, any output except A = B§	$V_{CC} = \text{MAX}$		-15		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$,	See Note 1	Condition A	20	32	mA
				Condition B	21	35	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}C$.

§Not more than one output should be shorted at a time.

NOTE 1:

With outputs open, I_{CC} is measured for the following conditions:

- A. S0 through S3, M, and A inputs are at 4.5 V, all other inputs are grounded.
- B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.



Switching Characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, ($C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$, see Fig A on page 373)

Parameter ¹	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Unit
t_{PLH}	C_n	C_{n+4}			14	24	ns
t_{PHL}				13	20		
t_{PLH}	Any A or B	C_{n+4}	$M = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$, $S_1 = S_2 = 0\text{ V}$ ($\overline{\text{SUM}}$ mode)		24	35	ns
t_{PHL}				17	30		
t_{PLH}	Any A or B	C_{n+4}	$M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$ $S_1 = S_2 = 4.5\text{ V}$ ($\overline{\text{DIFF}}$ mode)		24	38	ns
t_{PHL}				25	38		
t_{PLH}	C_n	Any F	$M = 0\text{ V}$ ($\overline{\text{SUM}}$ or $\overline{\text{DIFF}}$ mode)		12	24	ns
t_{PHL}				12	20		
t_{PLH}	Any A or B	G	$M = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$, $S_1 = S_2 = 0\text{ V}$ ($\overline{\text{SUM}}$ mode)		12	29	ns
t_{PHL}				15	23		
t_{PLH}	Any A or B	G	$M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ ($\overline{\text{DIFF}}$ mode)		20	30	ns
t_{PHL}				17	26		
t_{PLH}	Any A or B	P	$M = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$, $S_1 = S_2 = 0\text{ V}$, ($\overline{\text{SUM}}$ mode)		14	28	ns
t_{PHL}				20	30		
t_{PLH}	Any A or B	P	$M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ ($\overline{\text{DIFF}}$ mode)		20	30	ns
t_{PHL}				22	33		
t_{PLH}	A_i or B_i	F_i	$M = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$, $S_1 = S_2 = 0\text{ V}$ ($\overline{\text{SUM}}$ mode)		15	30	ns
t_{PHL}				13	20		
t_{PLH}	A_i or B_i	F_i	$M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ ($\overline{\text{DIFF}}$ mode)		21	32	ns
t_{PHL}				15	23		
t_{PLH}	A_i or B_i	F_i	$M = 4.5\text{ V}$ (logic mode)		17	30	ns
t_{PHL}				15	29		
t_{PLH}	Any A or B	A = B	$M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ ($\overline{\text{DIFF}}$ mode)		33	50	ns
t_{PHL}				29	45		

¹ t_{PLH} = propagation delay time, low-to-high-level output
¹ t_{PHL} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION

SUM MODE TEST TABLE

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
^t PLH	A _i	B _i	None	Remaining A and B	C _n	F _i	In-Phase
^t PHL							
^t PLH	B _i	A _i	None	Remaining A and B	C _n	F _i	In-Phase
^t PHL							
^t PLH	A _i	B _i	None	None	Remaining A and B, C _n	P	In-Phase
^t PHL							
^t PLH	B _i	A _i	None	None	Remaining A and B, C _n	P	In-Phase
^t PHL							
^t PLH	A _i	None	B _i	Remaining B	Remaining A, C _n	G	In-Phase
^t PHL							
^t PLH	B _i	None	A _i	Remaining B	Remaining A, C _n	G	In-Phase
^t PHL							
^t PLH	C _n	None	None	All A	All B	Any F or C _{n+4}	In-Phase
^t PHL							
^t PLH	A _i	None	B _i	Remaining B	Remaining A, C _n	C _{n+4}	Out-of-Phase
^t PHL							
^t PLH	B _i	None	A _i	Remaining B	Remaining A, C _n	C _{n+4}	Out-of-Phase
^t PHL							

DIFF MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
^t PLH	A _i	None	B _i	Remaining A	Remaining B, C _n	F _i	In-Phase
^t PHL							
^t PLH	B _i	A _i	None	Remaining A	Remaining B, C _n	F _i	Out-of-Phase
^t PHL							
^t PLH	A _i	None	B _i	None	Remaining A and B, C _n	P	In-Phase
^t PHL							
^t PLH	B _i	A _i	None	None	Remaining A and B, C _n	P	Out-of-Phase
^t PHL							
^t PLH	A _i	B _i	None	None	Remaining A and B, C _n	G	In-Phase
^t PHL							
^t PLH	B _i	None	A _i	None	Remaining A and B, C _n	G	Out-of-Phase
^t PHL							
^t PLH	A _i	None	B _i	Remaining A	Remaining B, C _n	A = B	In-Phase
^t PHL							
^t PLH	B _i	A _i	None	Remaining A	Remaining B, C _n	A = B	Out-of-Phase
^t PHL							
^t PLH	C _n	None	None	All A and B	None	C _{n+4} or any F	In-Phase
^t PHL							
^t PLH	A _i	B _i	None	None	Remaining A, B, C _n	C _{n+4}	Out-of-Phase
^t PHL							
^t PLH	B _i	None	A _i	None	Remaining A, B, C _n	C _{n+4}	In-Phase
^t PHL							

LOGIC MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
^t PLH	A _i	B _i	None	None	Remaining A and B, C _n	F _i	Out-of-Phase
^t PHL							
^t PLH	B _i	A _i	None	None	Remaining A and B, C _n	F _i	Out-of-Phase
^t PHL							



54LS190

Synchronous BCD Decade Up/Down Counter

54LS191

Synchronous 4-Bit Binary Up/Down Counter

FEATURES

- Single up/down count mode control line
- Asynchronous parallel load
- Count enable, parallel load control inputs
- Cascadable

DESCRIPTION

The 54LS190 and 54LS191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The 54LS191 is a 4-bit binary counter and the 54LS190 is a BCD counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

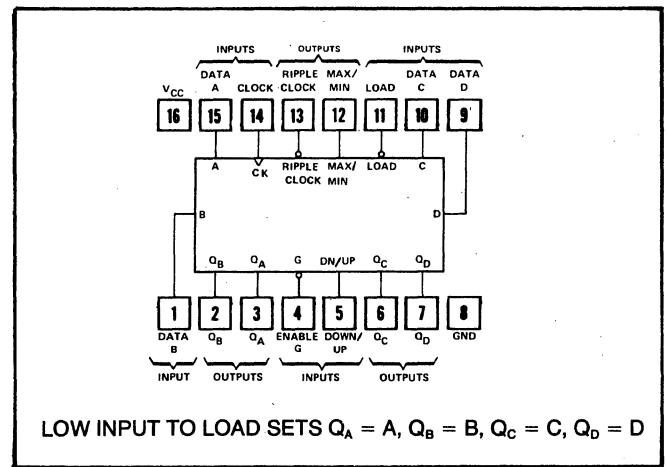
The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable and down/up inputs should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

PIN-OUT DIAGRAM



Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			-400	μA
Low-level output current, I_{OL}			8	mA
Input clock frequency, f_{clock}	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$	25			ns
Width of load input pulse, $t_{w(load)}$	35			ns
Data setup time, t_{setup} (See Figures 1 and 2)	20			ns
Enable to clock setup time, t_{setup}	20			ns
Data hold time, t_{hold}	0			ns
Operating free-air temperature, T_A	-55		125	$^{\circ}C$



Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions†		Min	Typ‡	Max	Unit
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.7	V
V_i	Input clamp voltage	$V_{CC} = \text{MIN}$,	$I_i = -18 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$,	$V_{IH} = 2 \text{ V}$,	2.5	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$,	$V_{IH} = 2 \text{ V}$,	$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
				$I_{OL} = 8 \text{ mA}$	0.3	0.45	
I_i	High-level input current at maximum input voltage	Enable	$V_{CC} = \text{MAX}$,	$V_i = 7 \text{ V}$		0.3	mA
		Others			0.1		
I_{IH}	High-level input current	Enable	$V_{CC} = \text{MAX}$,	$V_i = 2.7 \text{ V}$		60	μA
		Others			20		
I_{IL}	Low-level input current	Enable	$V_{CC} = \text{MAX}$,	$V_i = 0.4 \text{ V}$		-1.08	mA
		Others			-0.4		
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$,		-15		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$,	See Note 1		20	35	mA

†For conditions shown as MAX or MIN, use appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 1:

 I_{CC} is measured with all inputs grounded and all outputs open.Switching Characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

Parameter†	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Unit
f_{max}				20	25		MHz
t_{PLH}	Load	Q_A, G_B, Q_C, Q_D	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Figures 1 and 3 thru 7.		22	33	ns
t_{PHL}				33	50		
t_{PLH}	Data A, B, C, D	Q_A, Q_B, Q_C, Q_D			14	22	ns
t_{PHL}				35	50		
t_{PLH}	Clock	Ripple Clock			13	20	ns
t_{PHL}				16	24		
t_{PLH}	Clock	Q_A, Q_B, Q_C, Q_D			16	24	ns
t_{PHL}				24	36		
t_{PLH}	Clock	Max/Min			28	42	ns
t_{PHL}				37	52		
t_{PLH}	Down/Up	Ripple Clock			30	45	ns
t_{PHL}				30	45		
t_{PLH}	Down/Up	Max/Min		21	33	ns	
t_{PHL}			22	33			
t_{PLH}	Enable	Ripple Clock		21	33	ns	
t_{PHL}			22	33			

† f_{max} = maximum clock frequency t_{PLH} = propagation delay time, low-to-high-level output t_{PHL} = propagation delay time, high-to-low-level output

Tentative data, subject to change without notice.



54LS190

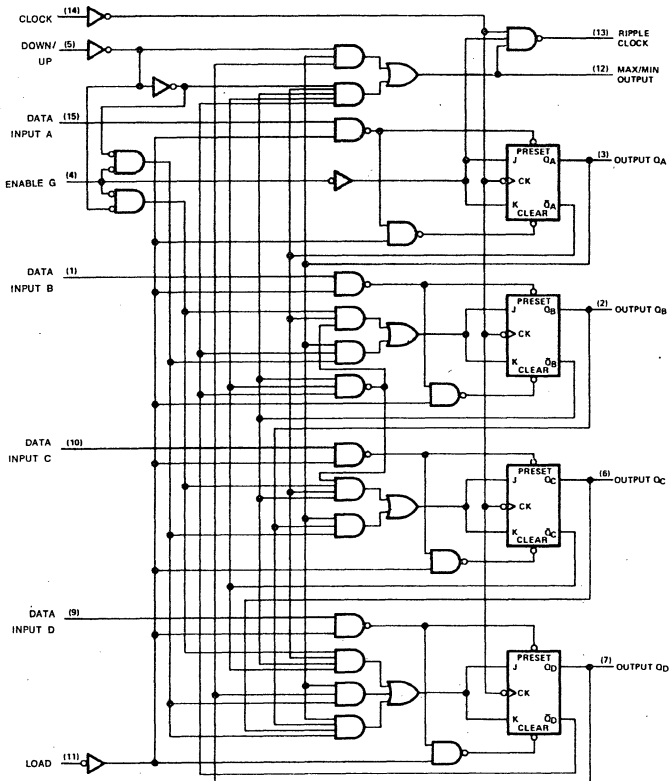
54LS191

Synchronous BCD Decade Up/Down Counter

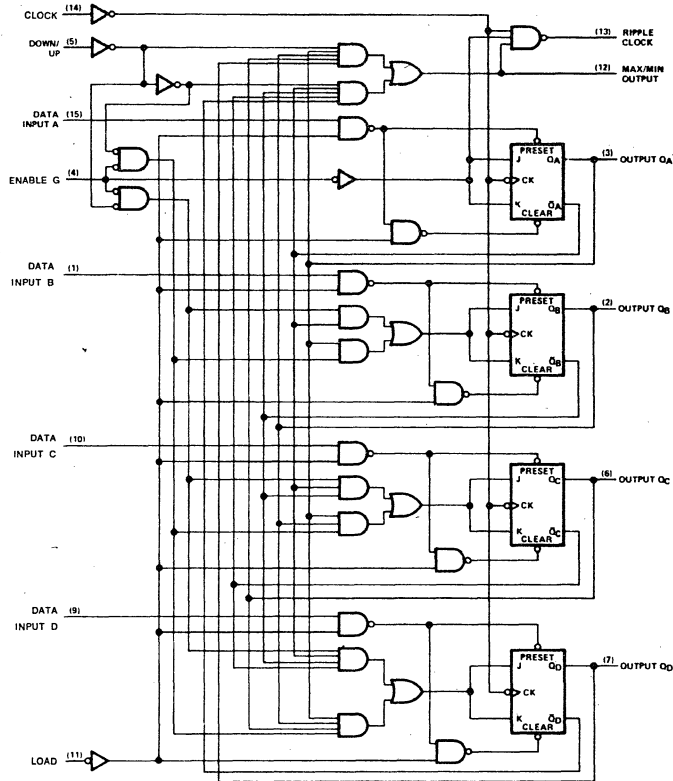
Synchronous 4-Bit Binary Up/Down Counter

LOGIC DIAGRAMS

54LS190



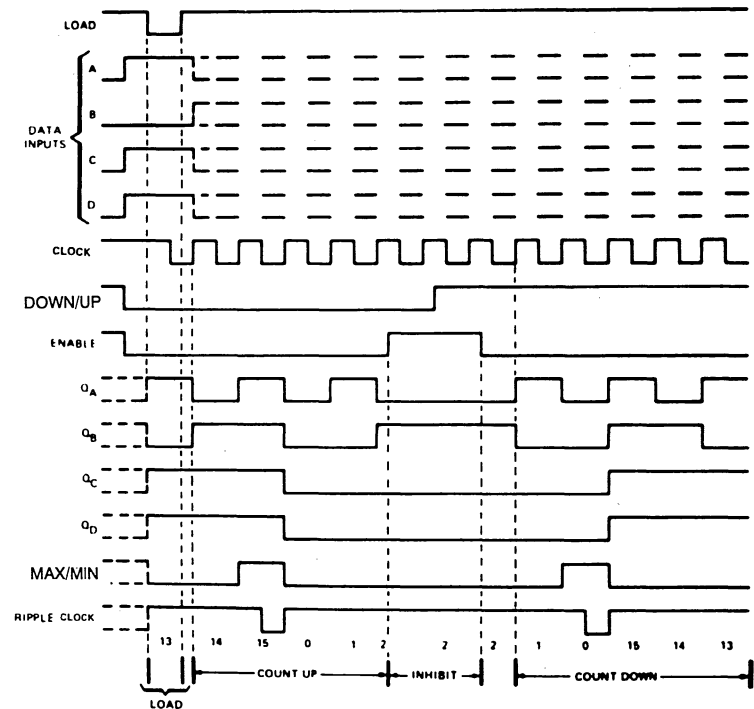
54LS191



54LS191 TYPICAL LOAD, COUNT AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

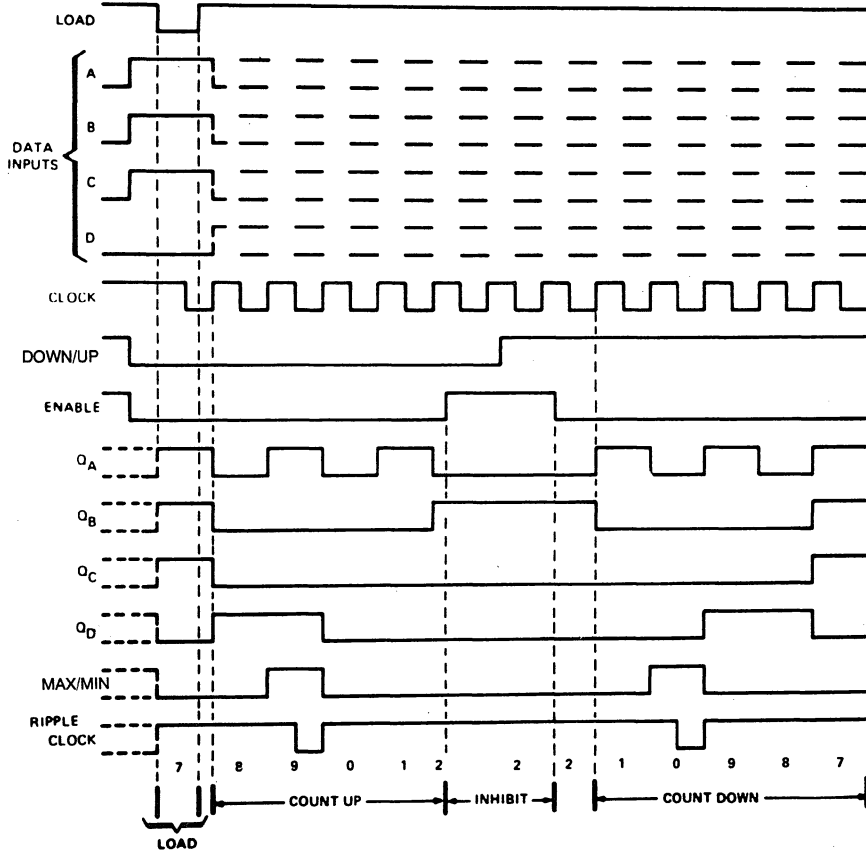
1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



54LS190 TYPICAL LOAD, COUNT AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



PARAMETER MEASUREMENT INFORMATION

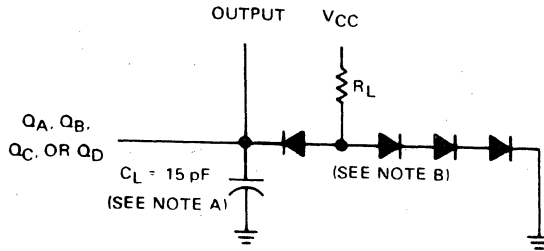
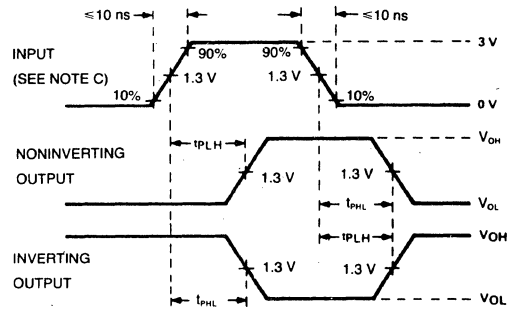


FIGURE 1—LOAD CIRCUIT FOR SWITCHING TIME MEASUREMENT



See waveform sequences in figures 4 through 7 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in figures 4 through 7.

FIGURE 3—GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES

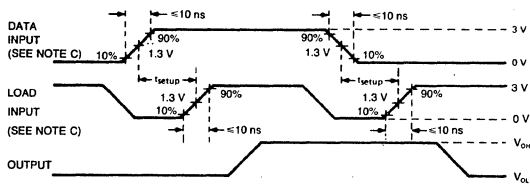
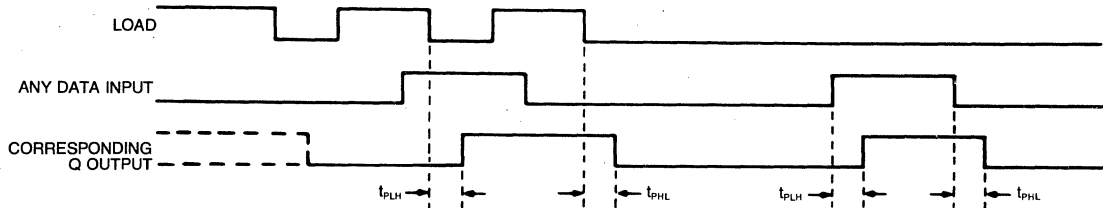


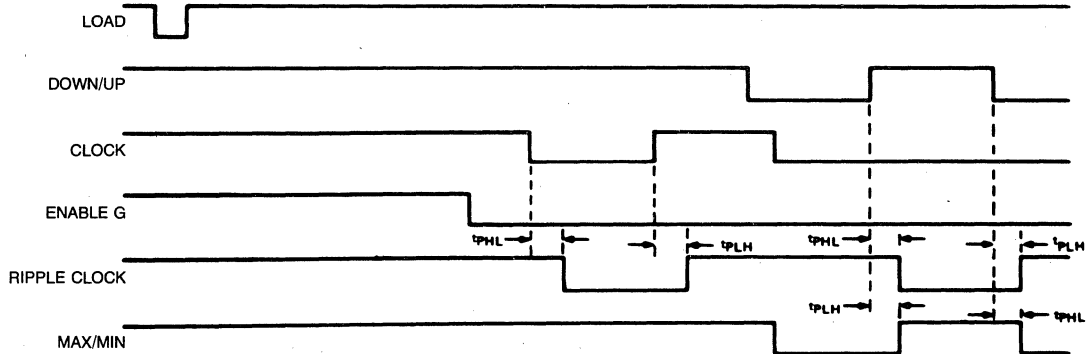
FIGURE 2—DATA SETUP TIME VOLTAGE WAVEFORMS

- NOTES A. C_L includes probe and μg capacitance.
 B. All diodes are 1N3064
 C. The input pulses are supplied by generators having the following characteristics. $Z_{OUT} = 50 \Omega$, duty cycle $\approx 50\%$, PRR $\le 1\text{ MHz}$.



NOTE E: Conditions on other inputs are irrelevant.

FIGURE 4 — LOAD TO OUTPUT AND DATA TO OUTPUT

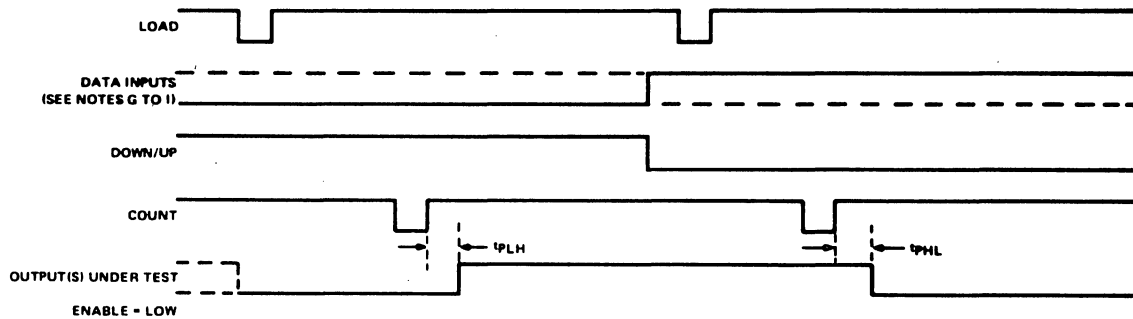


NOTE F: All data inputs are low.

FIGURE 5 — ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO MAX/MIN



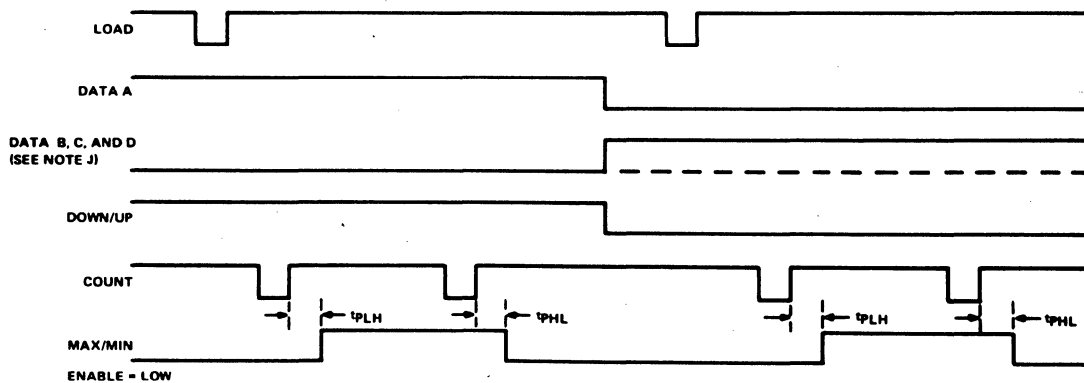
PARAMETER MEASUREMENT INFORMATION (Continued)



NOTES:

G. To test Q_A , Q_B , and Q_C outputs of 54LS190: Data inputs A, B, and C are shown by the solid line. Data input D is shown by the dashed line.
 H. To test Q_D output of 54LS190: Data inputs A and D are shown by the solid line. Data inputs B and C are held at the low logic level.
 I. To test Q_A , Q_B , Q_C , and Q_D outputs of 54LS191: All four data inputs are shown by the solid line.

FIGURE 6—CLOCK TO OUTPUT



NOTE J:

Data inputs B and C are shown by the dashed line for the 54LS190 and the solid line for the 54LS191: Data input D is shown by the solid line for both devices.

FIGURE 7—CLOCK TO MAX/MIN



54LS192

Synchronous BCD Decade Up/Down Counter

54LS193

Synchronous 4-Bit Binary Up/Down Counter

FEATURES

- Separate clock inputs for count-up, count-down
- Asynchronous parallel load and clear
- Cascadable

DESCRIPTION

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The 54LS192 is a BCD counter and the 54LS193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

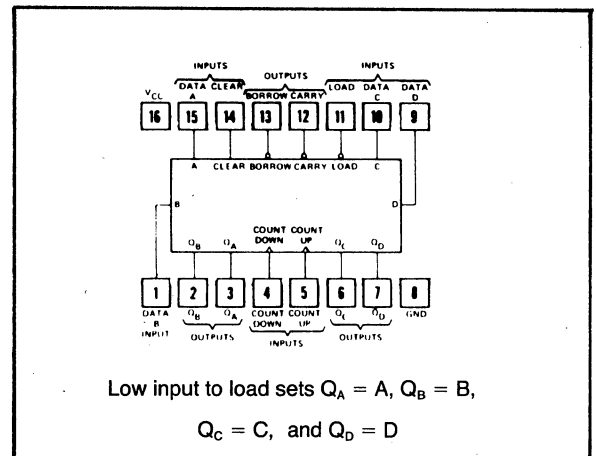
The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count inputs is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up-and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

PIN-OUT DIAGRAM



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Synchronous BCD Decade Up/Down Counter

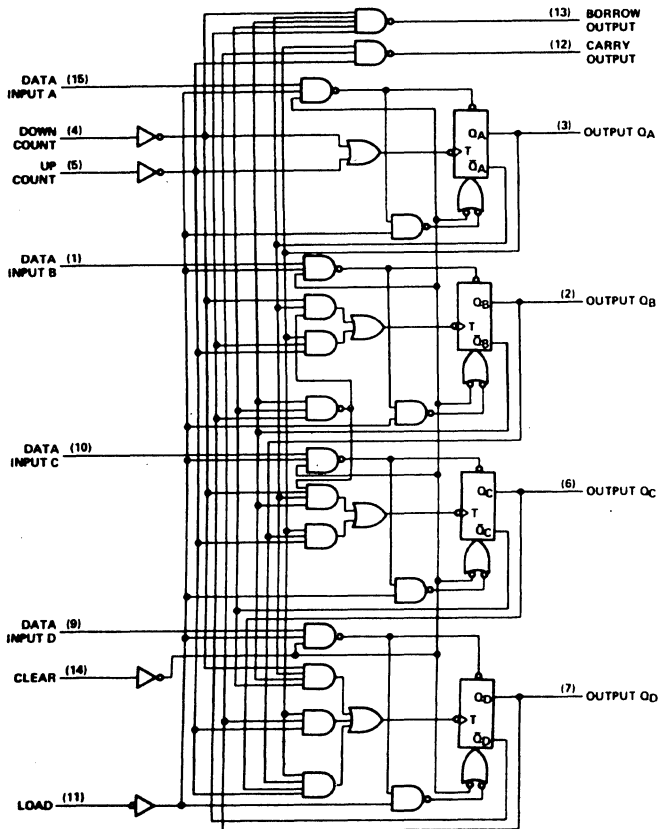
54LS192

Synchronous 4-Bit Binary Up/Down Counter

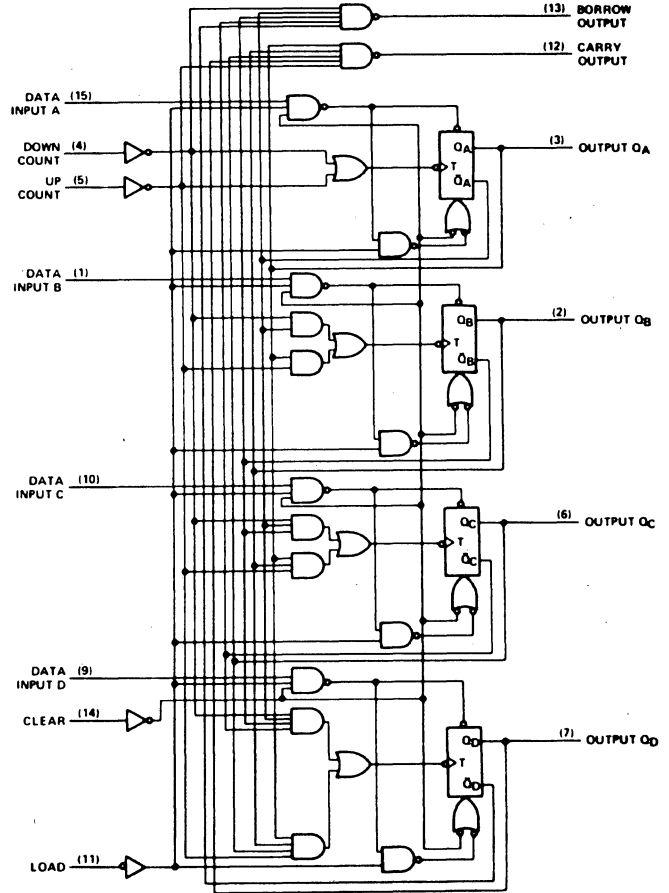
54LS193

LOGIC DIAGRAMS

54LS192



54LS193



Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			-400	μA
Low-level output current, I_{OL}			18	mA
Count frequency, f_{count}	0		25	MHz
Width of any input pulse, t_w	20			ns
Data setup time, t_{setup} (see Figure 1)	20			ns
Data hold time, t_{hold}	0			ns
Operating free-air temperature range, T_A	-55		125	$^{\circ}C$

DIGITAL

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54LS192

Synchronous BCD Decade Up/Down Counter

54LS193

Synchronous 4-Bit Binary Up/Down Counter

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.7	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18$		-1.5	V	
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL\text{max}}$, $I_{OH} = -400 \mu\text{A}$	2.5	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL\text{max}}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$	0.3	0.45	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.4	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-15		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 1		19	34	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 1:

 I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.Switching Characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

Parameter¶	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Unit
f_{max}				25	32		MHz
t_{PLH}	Count-up	Carry	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Figures 1 and 2		17	26	ns
t_{PHL}					16	24	
t_{PLH}	Count-down	Borrow			16	24	ns
t_{PHL}					16	24	
t_{PLH}	Either Count	Q			25	38	ns
t_{PHL}					31	47	
t_{PLH}	Load	Q			27	40	ns
t_{PHL}					29	40	
t_{PHL}	Clear	Q			22	35	ns

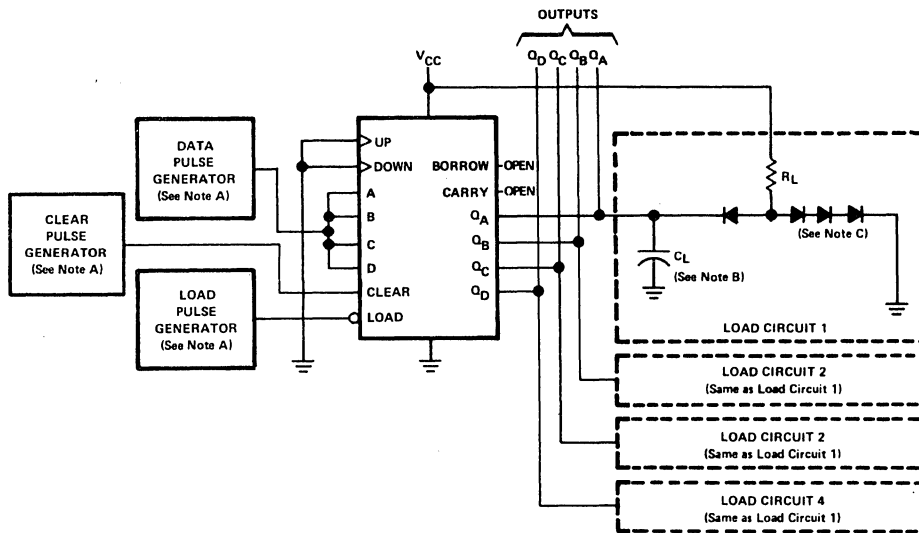
¶ f_{max} = maximum clock frequency¶ t_{PLH} = propagation delay time, low-to-high-level output¶ t_{PHL} = propagation delay time, high-to-low-level output

Tentative data, subject to change without notice

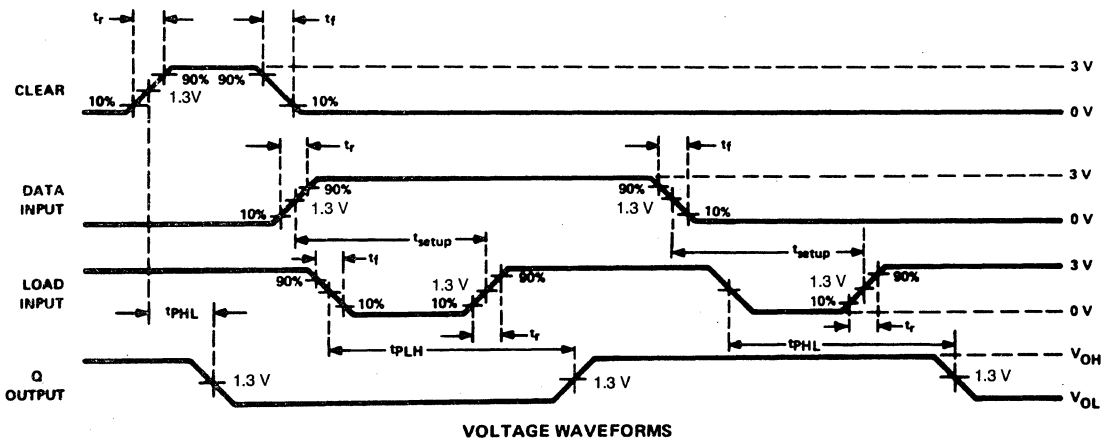
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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



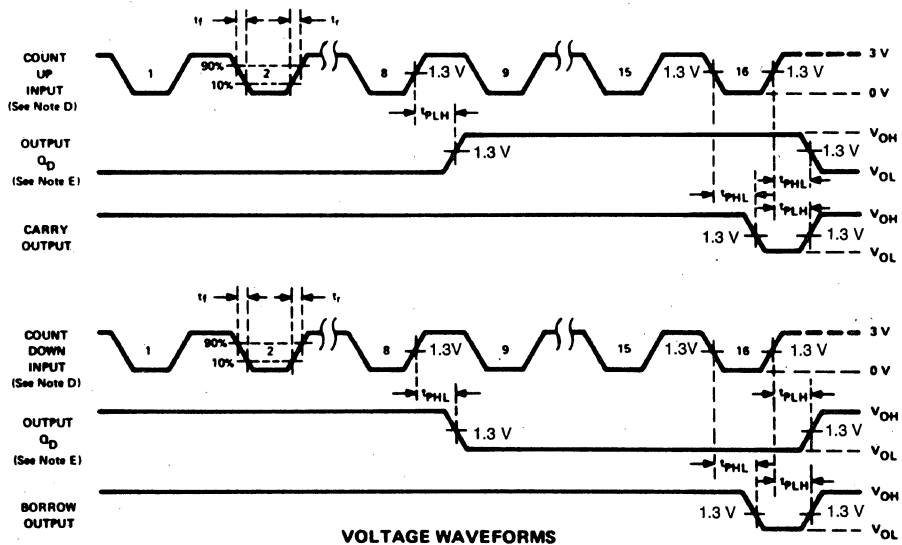
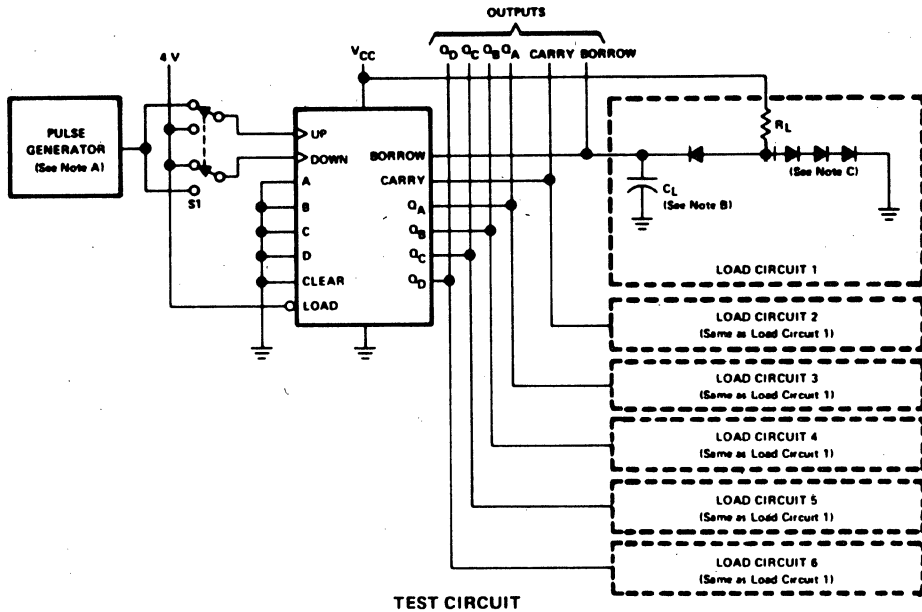
NOTES:

- A. The pulse generators have the following characteristics: $Z_{out} \approx 50 \Omega$ and for the data pulse generator PRR ≤ 500 kHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR, duty cycle = 50%.
- B. C_L includes probe and jig capacitance.
- C. Diodes are 1N3064.
- D. t_r and $t_f \leq 7$ ns.

FIGURE 1 — CLEAR, SETUP, AND LOAD TIMES



PARAMETER MEASUREMENT INFORMATION (Continued)



- NOTES:
 A. The pulse generator has the following characteristics: PRR \leq 1 MHz, $Z_{out} \approx 50 \Omega$, duty cycle = 50%.
 B. C_L includes probe and jig capacitance.
 C. Diodes are 1N3064.
 D. Count-up and count-down pulse shown is for the 54LS193 binary counter. Count cycle for 54LS192 decade counter is 1 through 10.
 E. Waveforms for outputs Q_A , Q_B , and Q_C are omitted to simplify the drawing.
 F. t_r and $t_f \leq 7$ ns.

FIGURE 2—PROPAGATION DELAY TIMES

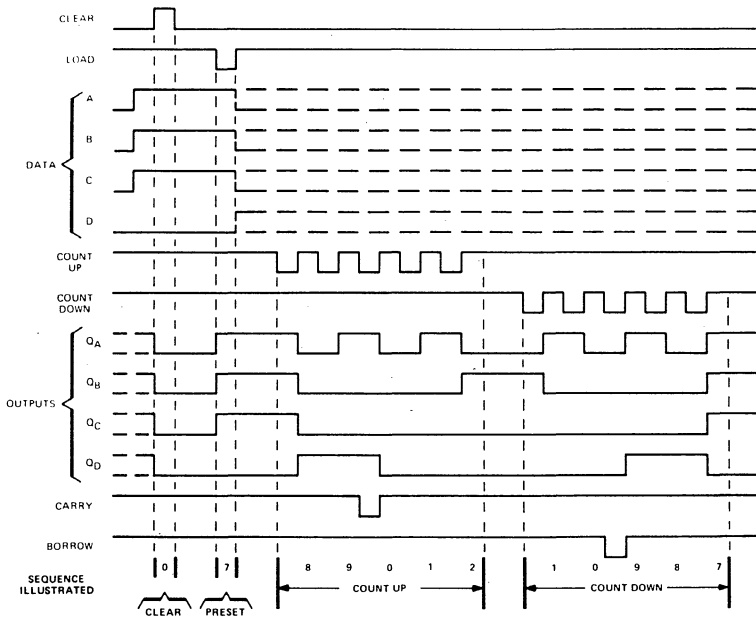


TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

54LS192

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.

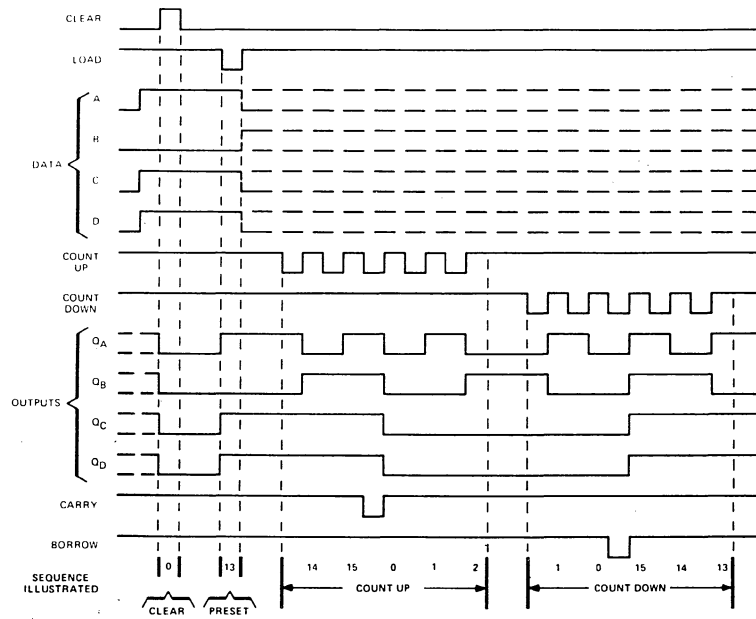


NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

54LS193

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.



DESCRIPTION

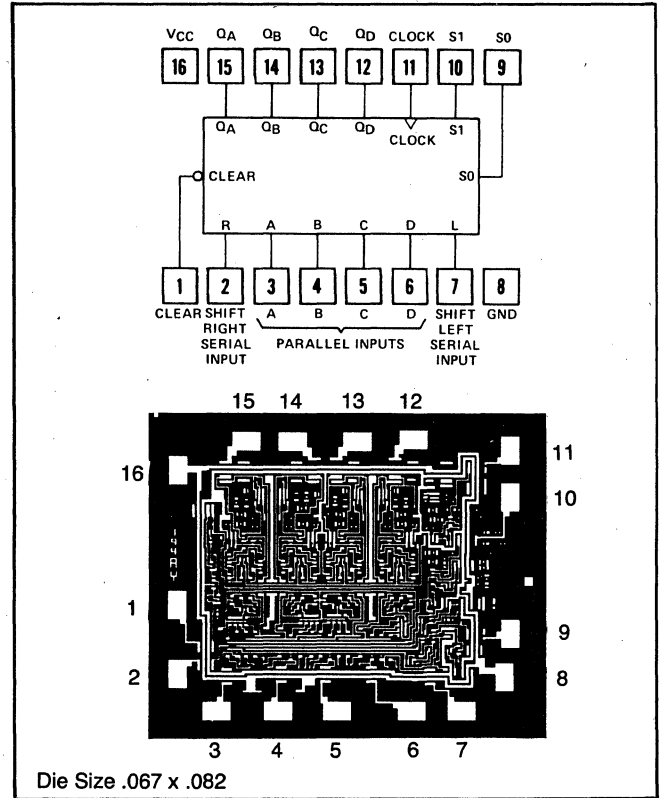
This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift inputs, operating-mode-control inputs, and a direct over-riding clear line. The register has four distinct modes of operation, namely:

- Parallel (broadside) load
- Shift right (in the direction Q_A toward Q_D)
- Shift left (in the direction Q_D toward Q_A)
- Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S_0 and S_1 , high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift-right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. Clocking of the flip-flop is inhibited when both mode control inputs are low.

PIN-OUT DIAGRAM

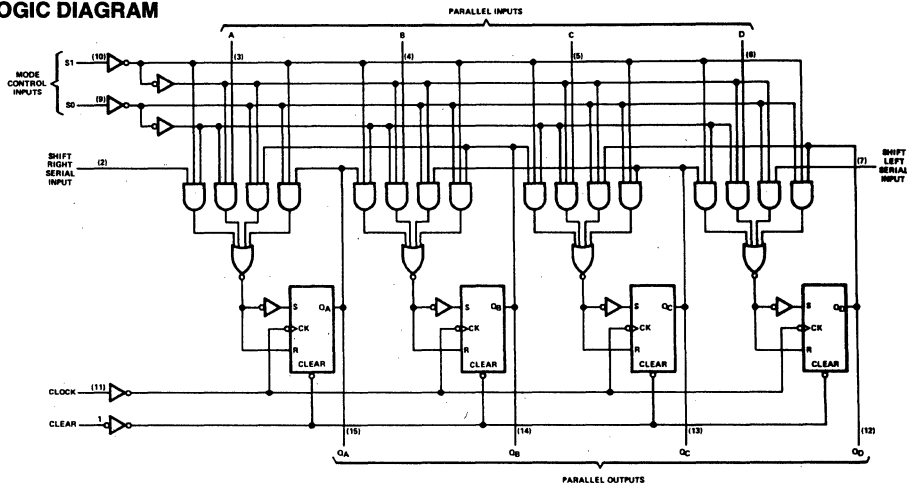


FUNCTION TABLE

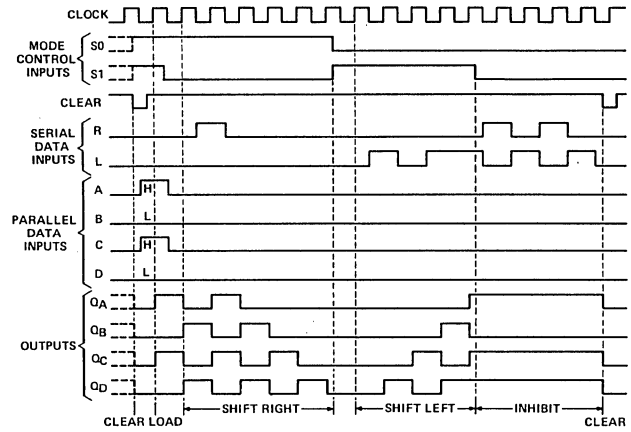
CLEAR	MODE		CLOCK	SERIAL				PARALLEL				OUTPUTS			
	S1	S0		LEFT		RIGHT		A	B	C	D	Q_A	Q_B	Q_C	Q_D
				RIGHT	LEFT	A	B								
L	X	X	X	X	X	X	X	X	X	X	L	L	L	L	
H	X	X	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	
H	H	H	↑	X	X	a	b	c	d	X	a	b	c	d	
H	L	H	↑	X	H	X	Q_{An}	Q_{Bn}	Q_{Cn}	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	
H	L	H	↑	X	L	X	Q_{An}	Q_{Bn}	Q_{Cn}	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	
H	H	L	↑	H	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H	
H	H	L	↑	L	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L	
H	L	L	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	

H = high level (steady state)
 L = low level (steady state)
 X = irrelevant (any input, including transitions)
 ↑ = transition from low to high level
 a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
 $Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}$ = the level of $Q_A, Q_B, Q_C,$ or Q_D , respectively, before the indicated steady-state input conditions were established.
 $Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}$ = the level of $Q_A, Q_B, Q_C,$ respectively, before the most-recent ↑ transition of the clock.

LOGIC DIAGRAM



TYPICAL TIMING SEQUENCES



Recommended Operating Conditions

		Min	Nom	Max	Unit
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level output current, I_{OH}				-400	μA
Low-level output current, I_{OL}				8	mA
Clock frequency, f_{clock}		0			MHz
Width of clock or clear pulse, t_w		30			ns
Setup time, t_{setup}	Mode control	30			ns
	Serial and parallel data	16			ns
	Clear inactive-state	18			ns
Hold time at any input, t_{hold}		0			ns
Operating free-air temperature, T_A		-55		125	$^{\circ}C$

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit	
V_{IH} High-level input voltage		2			V	
V_{IL} Low-level input voltage				0.7	V	
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5	V	
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{ILmax}$, $I_{OH} = -400 \mu A$	2.5	3.5		V	
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{ILmax}$		$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
			$I_{OL} = 8 \text{ mA}$	0.3	0.45	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1	mA	
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20	μA	
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.4	mA	
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-15		-100	mA	
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 1		15	23	mA	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}C$.

§Not more than one output should be shorted at a time.

NOTE 1:

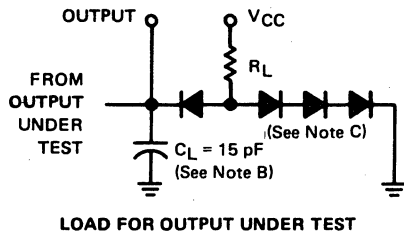
With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5 V, applied to clock.



Switching Characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

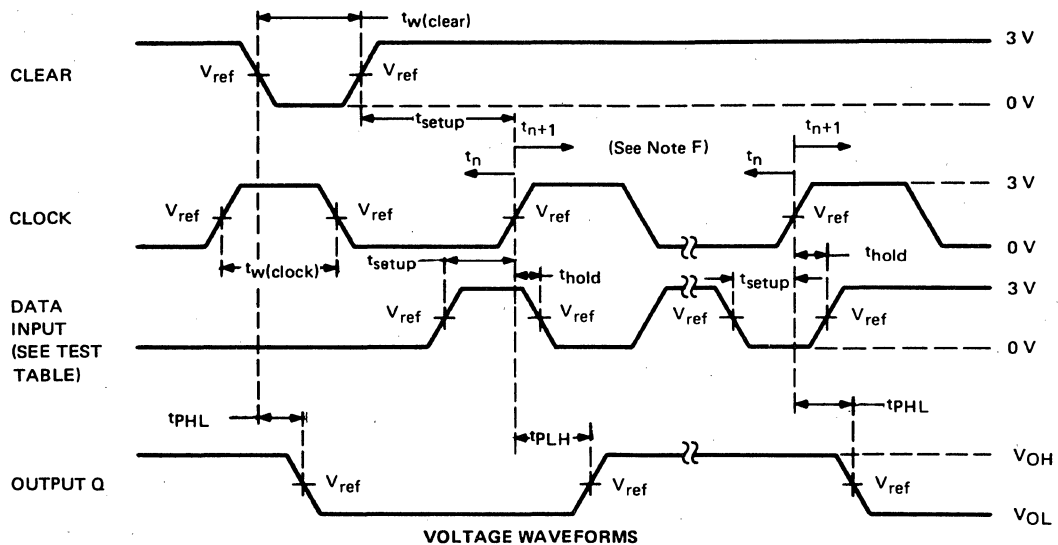
Parameter	Test Conditions	Min	Typ	Max	Unit
f_{max} Maximum clock frequency	$C_L = 15\text{ pF}$,	30	40		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear	$R_L = 2\text{ k}\Omega$,		24	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock	See Figure 1		11	18	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			15	22	ns

PARAMETER MEASUREMENT INFORMATION



TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S1	S0	OUTPUT TESTED (SEE NOTE E)
A	4.5 V	4.5 V	Q_A at t_{n+1}
B	4.5 V	4.5 V	Q_B at t_{n+1}
C	4.5 V	4.5 V	Q_C at t_{n+1}
D	4.5 V	4.5 V	Q_D at t_{n+1}
L Serial Input	4.5 V	0 V	Q_A at t_{n+4}
R Serial Input	0 V	4.5 V	Q_D at t_{n+4}



- NOTES:
- A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$ and $PRR \leq 1\text{ MHz}$, $t_r \leq 15\text{ ns}$ and $t_f \leq 6\text{ ns}$.
 - B. When testing f_{max} , vary PRR.
 - C. C_L includes probe and jig capacitance.
 - D. All diodes are 1N3064 or 1N916.
 - E. A clear pulse is applied prior to each test.
 - F. $V_{ref} = 1.3\text{ V}$.
 - G. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1} . Proper shifting of data is verified at t_{n+4} with a functional test.
- G. t_n = bit time before clocking transition.
 t_{n+1} = bit time after one clocking transition.
 t_{n+4} = bit time after four clocking transitions.

FIGURE 1



DESCRIPTION

This 4-bit register features parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The register has two modes of operation:

Parallel (broadside) load
Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the function table.

FUNCTION TABLE

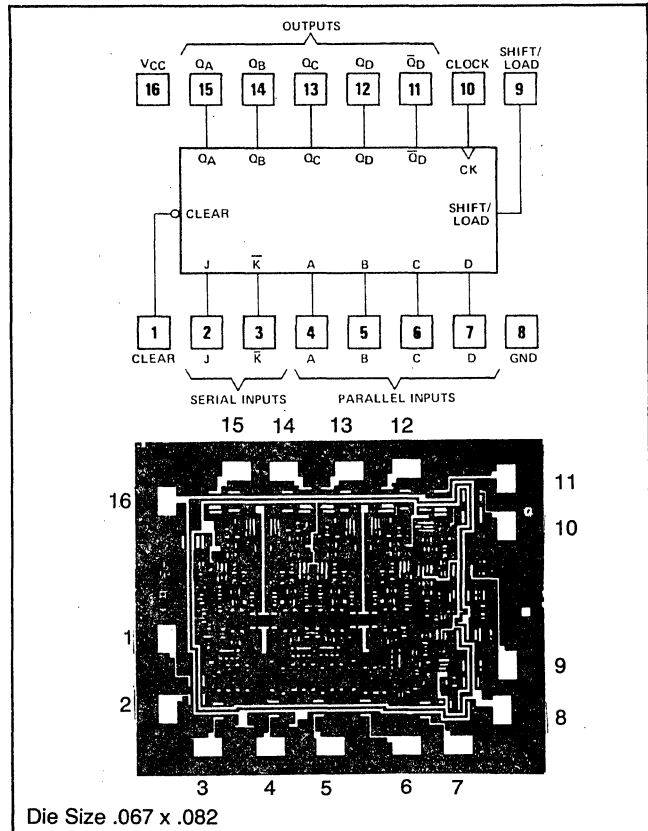
INPUTS					OUTPUTS								
CLEAR	SHIFT/LOAD	CLOCK	SERIAL		PARALLEL								
			J	K	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	\bar{a}
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	\bar{Q}_{D0}
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
H	H	↑	H	L	X	X	X	X	\bar{Q}_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at A, B, C, or D, respectively.

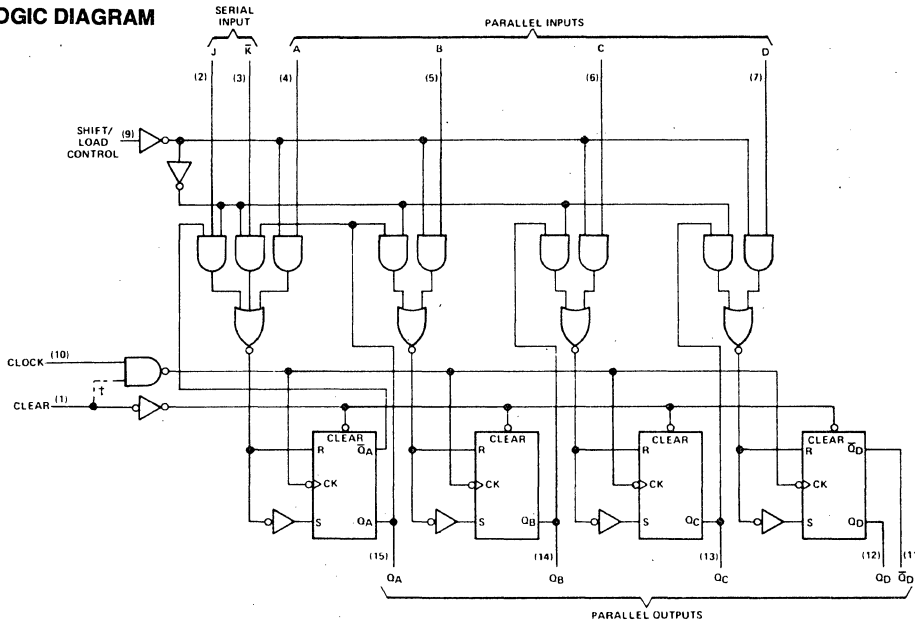
Q_{A0} , Q_{B0} , Q_{C0} , Q_{D0} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the indicated steady-state input conditions were established.

Q_{An} , Q_{Bn} , Q_{Cn} = the level of Q_A , Q_B , or Q_C , respectively, before the most-recent transition of the clock.

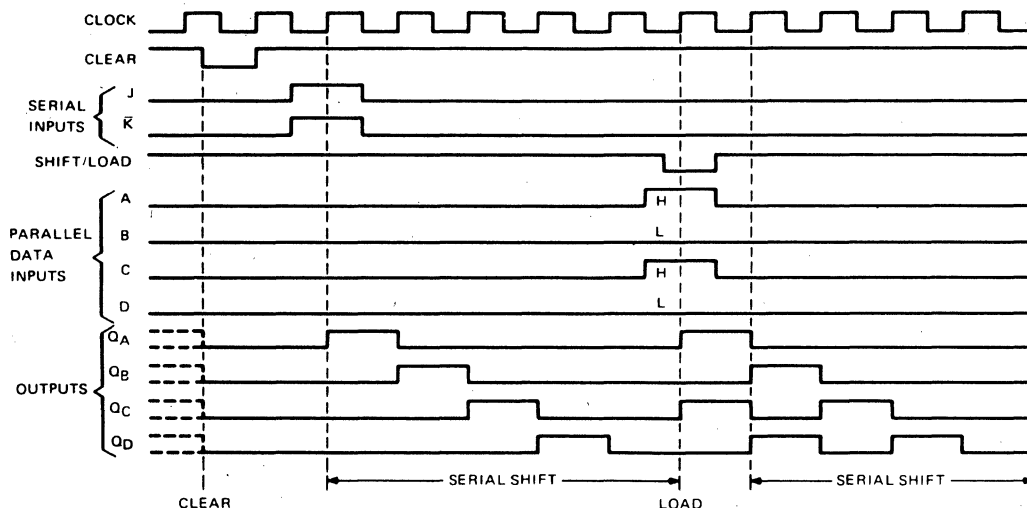
PIN-OUT DIAGRAM



LOGIC DIAGRAM



TYPICAL TIMING SEQUENCES



Recommended Operating Conditions

		Min	Nom	Max	Unit
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level output current, I_{OH}				-400	μA
Low-level output current, I_{OL}				8	mA
Clock frequency, f_{clock}		0			MHz
Width of clock pulse, $t_{w(clock)}$		18			ns
Width of clear input pulse, $t_{w(clear)}$		20			ns
Setup time, t_{setup} (see Figure 1)	Shift/load	25			ns
	Serial and parallel data	15			
	Clear inactive-state	25			
Shift/load release time, $t_{release}$ (see Figure 1)				0	ns
Serial and parallel data hold time, t_{hold} (see Figure 1)		0			ns
Operating free-air temperature, T_A		-55		125	$^{\circ}C$

Switching Characteristics, $V_{CC} = 5 V, T_A = 25^{\circ}C$.

Parameter	Test Conditions	Min	Typ	Max	Unit
f_{max} Maximum clock frequency	$C_L = 15 pF,$ $R_L = 2 k\Omega,$ See Figure 1	30	40		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear			27	35	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			10	17	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			13	20	ns



Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit	
V_{IH}	High-level input voltage	2			V	
V_{IL}	Low-level input voltage			0.7	V	
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.5	V	
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4	V	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
			$I_{OL} = 8 \text{ mA}$	0.3	0.45	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1	mA	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20	μA	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-0.4	mA	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$		-15	mA	
I_{CC}	Supply current	$V_{CC} = \text{MAX},$ See Note 1	14	21	mA	

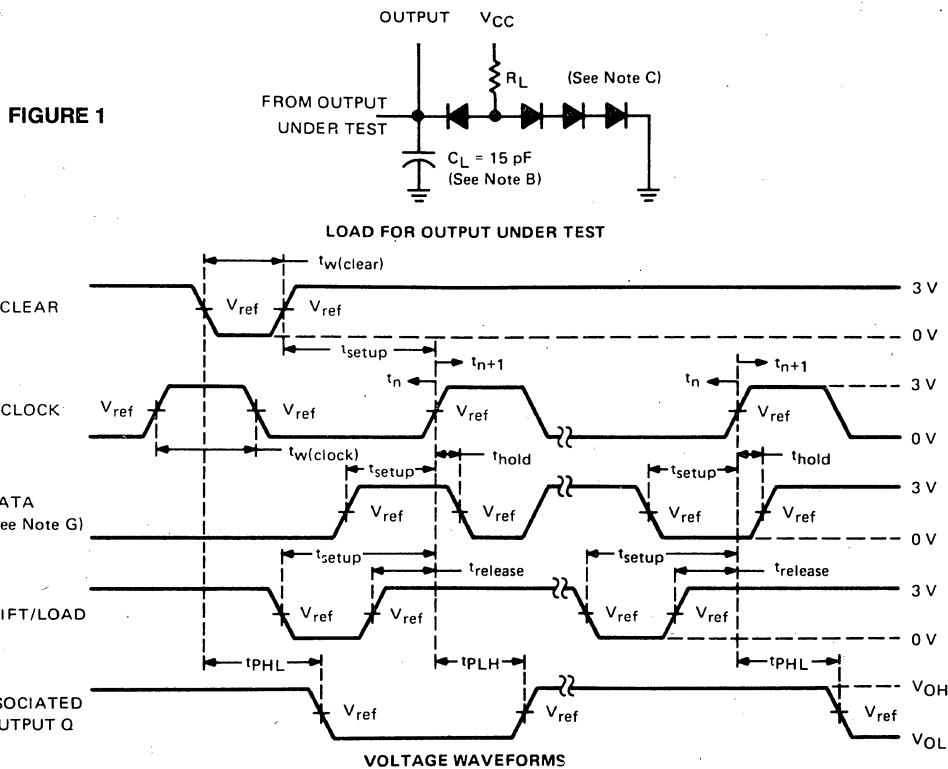
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 1: With all outputs open, shift/load grounded and 4.5 V applied to the J, \bar{K} , and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

PARAMETER MEASUREMENT INFORMATION



NOTES:

A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50 \Omega$ and $PRR \leq \text{MHz}$, $t_r \leq 15 \text{ ns}$ and $t_f \leq 6 \text{ ns}$. When testing t_{max} , vary the clock PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064.

D. A clear pulse is applied prior to each test.

E. $V_{ref} = 1.3 \text{ V}$.

F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1} . Proper shifting of data is verified at t_{n+4} with a functional test.

G. J and \bar{K} inputs are tested the same as data A, B, C, and D inputs except that shift/load input remains high.

H. t_n = bit time before clocking transition.

t_{n+1} = bit time after one clocking transition. t_{n+4} = bit time after four clocking transitions.



54LS196

Presettable BCD Decade Ripple Counter

54LS197

Presettable 4-Bit Binary Ripple Counter

FEATURES

- BCD, bi-quinary, binary counting modes
- Asynchronous clear
- Fully programmable
- May be used as 4-Bit latches

DESCRIPTION

These high-speed monolithic counters consist of four d-c coupled, master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (54LS196) or a divide-by-two and a divide-by-eight counter (54LS197). These four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

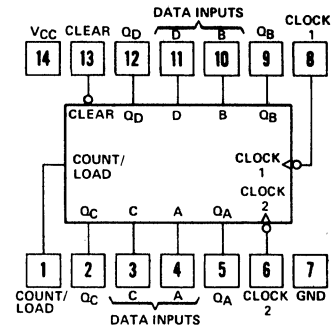
These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

TYPICAL COUNT CONFIGURATIONS 54LS196

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

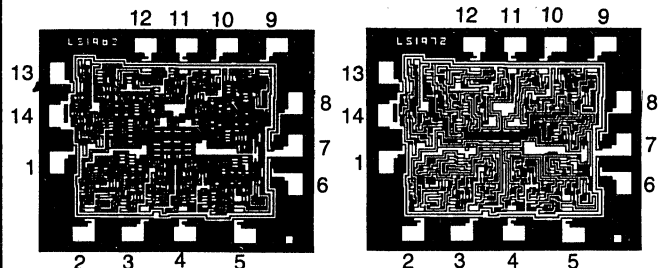
1. When used as a binary-coded-decimal decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence function table shown at the right.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary function table.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B , Q_C , and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

PIN-OUT DIAGRAM



54LS196

54LS197



Die Size .062 x .074

54LS196 FUNCTION TABLES

DECADE (BCD)
(See Note A)

COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUTS			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

H = high level, L = low level

NOTES: A. Output Q_A connected to clock-2 input.

B. Output Q_D connected to clock-1 input.



Presettable BCD Decade Ripple Counter

54LS196

Presettable 4-Bit Binary Ripple Counter

54LS197

54LS197

The output of flip-flop A is not internally connected to the succeeding flip-flops, therefore the counter may be operated in two independent modes:

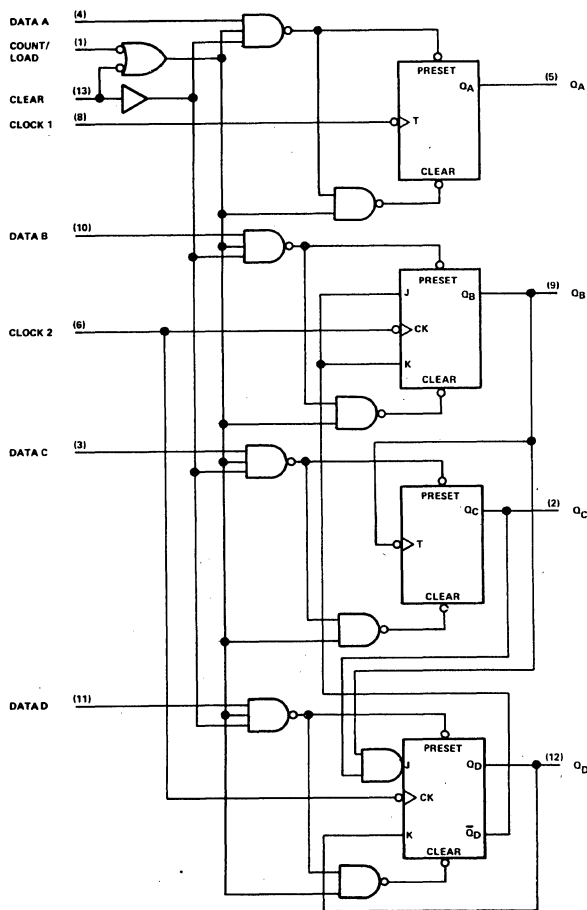
1. When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A , Q_B , Q_C , Q_D output as shown in the function table at right.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B , Q_C , and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

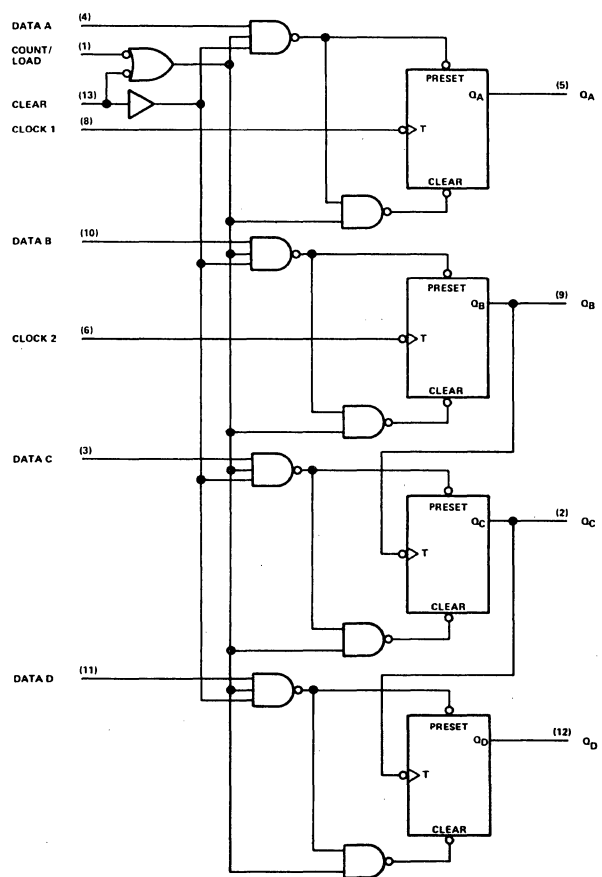
54LS197
FUNCTION TABLE
(See Note A)

H = high level, L = low level
NOTE A: Output Q_A connected to clock-2 input.

LOGIC DIAGRAM 54LS196



LOGIC DIAGRAM 54LS197



54LS196

Presetable BCD Decade Ripple Counter

54LS197

Presetable 4-Bit Binary Ripple Counter

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions†		Min	Typ‡	Max	Unit
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.7	V
V_I	Input clamp voltage	$V_{CC} = \text{MIN}$,	$I_I = -18 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$,	$V_{IH} = 2 \text{ V}$,		2.5	3.4	V
		$V_{IL} = V_{IL\text{max}}$,	$I_{OH} = -400 \mu\text{A}$				
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$,	$V_{IH} = 2 \text{ V}$,		0.25	0.4	V
		$V_{IL} = V_{IL\text{max}}$	$I_{OL} = 4 \text{ mA}^{\parallel}$				
I_I	Input current at maximum input voltage	Data, count /load	$V_{CC} = \text{MAX}$,	$V_I = 5.5 \text{ V}$		0.1	mA
		Clear, clock 1				0.2	
		Clock 2 of 'LS196				0.4	
		Clock 2 of 'LS197				0.2	
I_{IH}	High-level input current	Data, count /load	$V_{CC} = \text{MAX}$,	$V_I = 2.7 \text{ V}$		20	μA
		Clear, clock 1				40	
		Clock 2 of 'LS196				80	
		Clock 2 of 'LS197				40	
I_{IL}	Low-level input current	Data, count /load	$V_{CC} = \text{MAX}$,	$V_I = 0.4 \text{ V}$		-0.36	mA
		Clear				-0.72	
		Clock 1				-2.4	
		Clock 2 of 'LS196				-2.8	
		Clock 2 of 'LS197				-1.3	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$		-6		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$,	See Note 2		12	20	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

¶ I_{OL} outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while maintaining full fan-out capability.

NOTE 2:

 I_{CC} is measured with all inputs grounded and all outputs open.

Pre-settable BCD Decade Ripple Counter

54LS196

Pre-settable 4-Bit Binary Ripple Counter

54LS197

DIGITAL

Raytheon Semiconductor

Recommended Operating Conditions

		Min	Nom	Max	Unit
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level output current, I_{OH}				-400	μA
Low-level output current, I_{OL}				4	mA
Count frequency	Clock-1 input	0			MHz
	Clock-2 input	0			
Pulse width, t_w	Clock-1 input	20			ns
	Clock-2 input	30			
	Clear	15			
	Load	20			
Input hold time, t_{hold}	High-level data	$t_w (load)$			ns
	Low-level data	$t_w (load)$			
Input setup time, t_{setup}	High-level data	10			ns
	Low-level data	15			
Count enable time, t_{enable} (See Note 1)		20			ns
Operating free-air temperature, T_A		-55		125	$^{\circ}C$

NOTE 1:
Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

Switching Characteristics, $V_{CC} = 5 V, T_A = 25^{\circ}C$

Parameter	From (Input)	To (Output)	Test Conditions†	54LS196			54LS197			Unit	
				Min	Typ	Max	Min	Typ	Max		
f_{max}	Clock 1	Q_A	$C_L = 15 pF,$ $R_L = 2 k\Omega,$ See Fig. A on page 373	45	70		45	60		MHz	
t_{PLH}	Clock 1	Q_A			8	12		8	12		ns
t_{PHL}					12	16		12	16		
t_{PLH}	Clock 2	Q_B			11	15		10	15		ns
t_{PHL}					14	19		13	18		
t_{PLH}	Clock 2	Q_C			22	34		22	34		ns
t_{PHL}					29	40		26	34		
t_{PLH}	Clock 2	Q_D			11	18		34	50		ns
t_{PHL}					16	20		40	55		
t_{PLH}	A, B, C, D	Q_A, Q_B, Q_C, Q_D			12	18		21	18		ns
t_{PHL}					21	34		21	34		
t_{PLH}	Load	Any			20	30		20	30		ns
t_{PHL}					31	45		31	45		
t_{PHL}	Clear	Any			32	45		32	45		ns

† f_{max} = maximum input count frequency.
 t_{PLH} = propagation delay time, low-to-high-level output, t_{PHL} = propagation delay time, high-to-low-level output.



54LS251

8-Line-To-1-Line Multiplexer With Three-State Outputs

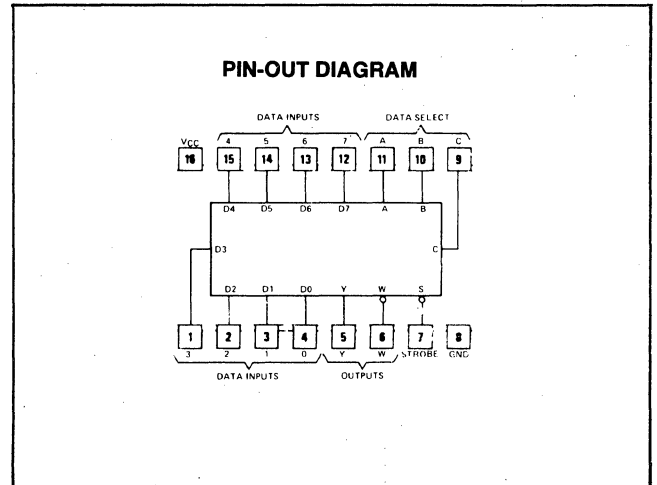
FEATURES

- Selects one of eight data sources
- Performs parallel-to-serial conversion
- Complementary 3-state outputs

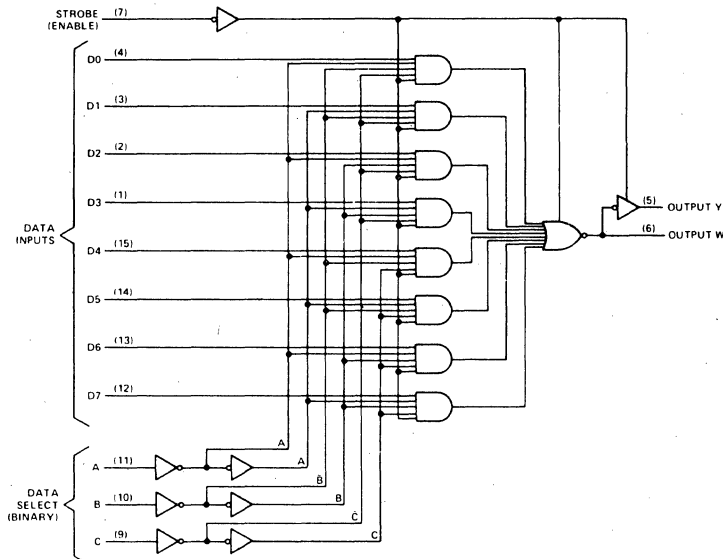
DESCRIPTION

This monolithic data selector/multiplexer contains full on-chip binary decoding to select one-of-eight data sources and features a strobe-controlled three-state output. The strobe must be at a low logic level to enable this device. The three-state outputs permit a number of outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.



LOGIC DIAGRAMS



FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = low logic level
 X = irrelevant, Z = high impedance (off)
 D0, D1 . . . D7 = the level of the respective D input

Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			-1	mA
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	-55		125	°C



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8-Line-To-1-Line Multiplexer With Three-State Outputs

54LS251

DIGITAL

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Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit
V _{IH} High-level input voltage		2			V
V _{IL} Low-level input voltage				0.7	V
V _I Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = MAX	2.5	3.4		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OL} = 4 mA		0.25	0.4	V
				0.3	
I _{O(off)} Off-state (high-impedance-state) output current	V _{CC} = MAX, V _{IH} = 2 V			20	μA
				-20	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V			0.1	mA
I _{IH} High-level input current	V _{CC} = MAX, V _I = 2.7 V			20	μA
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-0.4	mA
I _{OS} Short-circuit output current§	V _{CC} = MAX	-15		-100	mA
I _{CC} Supply current	V _{CC} = MAX, See Note 1	Condition A	6.1	10	mA
		Condition B	7.1	12	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

NOTE 1:

I_{CC} is measured with the outputs open and all data and select inputs at 4.5 V under the following conditions:

A. Strobe grounded.

B. Strobe at 4.5 V.

Switching Characteristics, V_{CC} = 5 V, T_A = 25°C.

Parameter¶	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Unit
t _{PLH}	A, B, or C (4 levels)	Y	C _L = 15 pF, R _L = 2 kΩ, See Fig. C on page 373		29	45	ns
t _{PHL}					28	45	
t _{PLH}	A, B, or C (3 levels)	W			20	33	ns
t _{PHL}					21	33	
t _{PLH}	Any D	Y			17	28	ns
t _{PHL}					18	28	
t _{PLH}	Any D	W			10	15	ns
t _{PHL}					9	15	
t _{ZH}	Strobe	Y			17	27	ns
t _{ZL}					26	40	
t _{ZH}	Strobe	W			17	27	ns
t _{ZL}					24	40	
t _{HZ}	Strobe	Y	C _L = 5 pF, R _L = 2 kΩ, See Fig. C on page 373		30	45	ns
t _{LZ}					15	25	
t _{HZ}	Strobe	W			30	45	ns
t _{LZ}					15	25	

¶t_{PLH} = Propagation delay time, low-to-high-level output.

t_{PHL} = Propagation delay time, high-to-low-level output.

t_{ZH} = Output enable time to high level.

t_{ZL} = Output enable time to low level.

t_{HZ} = Output disable time from high level.

t_{LZ} = Output disable time from low level.

Tentative data, subject to change without notice



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Dual 4-Line-To-1-Line Multiplexer With Three-State Outputs

54LS253

FEATURES

- Three-state version of 54LS153
- Non-inverting
- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion

DESCRIPTION

The 54LS253 is a high-speed dual 4-line-to-1-line multiplexer with common select inputs and separate output control inputs for each half. Each half can select one bit of four and present it at the output in non-inverted form.

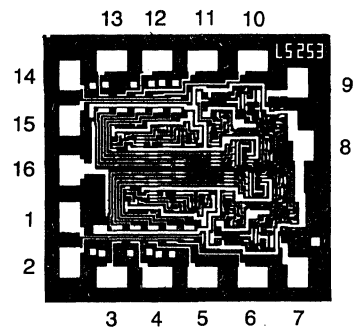
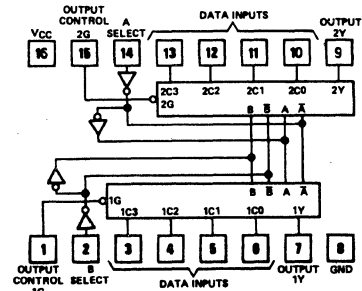
The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

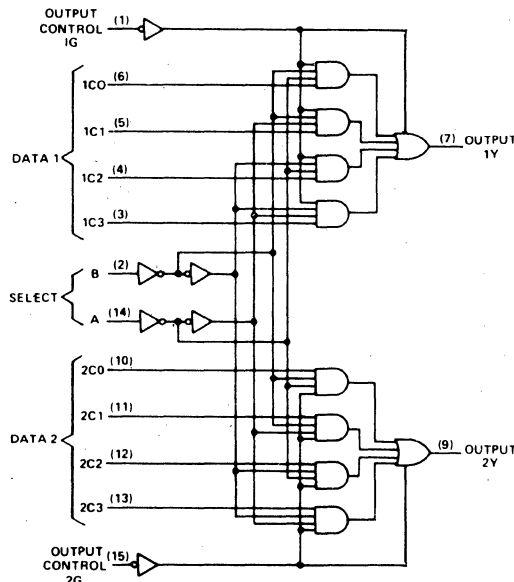
Address inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

PIN-OUT DIAGRAM



Die Size .057 x .061

LOGIC DIAGRAM



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Dual 4-Line-To-1-Line Multiplexer With Three-State Outputs

54LS253

DIGITAL

Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			-1	mA
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	-55		125	°C

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.7	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL\text{max}}$, $I_{OH} = \text{MAX}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL\text{max}}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$	0.3	0.45	
$I_{O(\text{off})}$ Off-State (high-impedance state) output current	$V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$	$V_O = 2.7 \text{ V}$		20	μA
		$V_O = 0.4 \text{ V}$		-20	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.36	mA
I_{OS} Short-circuit output current‡§	$V_{CC} = \text{MAX}$	-6		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 1	Condition A	7	12	mA
		Condition B	8.5	14	

§For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE: 1

I_{CC} is measured with the outputs open under the following conditions:

A. All inputs grounded.

B. Output control at 4.5 V, all inputs grounded.

Switching Characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

Parameter†	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Unit
t_{PLH}	Data	Y	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Fig. C on page 373		7	12	ns
t_{PHL}					12	17	
t_{PLH}	Select	Y			18	25	ns
t_{PHL}					18	27	
t_{ZH}	Output Control	Y			10	16	ns
t_{ZL}					13	18	
t_{HZ}	Output Control	Y	$C_L = 5 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Fig. C on page 373		7	15	ns
t_{LZ}					12	19	

† t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

t_{ZH} = Output enable time to high level

t_{ZL} = Output enable time to low level

t_{HZ} = Output disable time from high level

t_{LZ} = Output disable time from low level



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Dual 2-Line-To-4-Line Decoder/Demultiplexer With Three-State Outputs

54LS255

FEATURES

- Three-state version of 54LS155
- Applications:
 - Dual 2-Line-to-4-Line Decoder
 - Dual 1-Line-to-4-Line Demultiplexer
 - 3-Line-to-8-Line Decoder
 - 1-Line-to-8-Line Demultiplexer

DESCRIPTION

The 54LS255 features dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the output controls, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual controls permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. Input clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design.

**FUNCTION TABLE
3-LINE-TO-8-LINE DECODER
OR 1-LINE-TO-8-LINE DEMULTIPLEXER**

INPUTS				OUTPUTS			
SELECT	CONTROL	DATA					
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	Z	Z	Z	Z
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

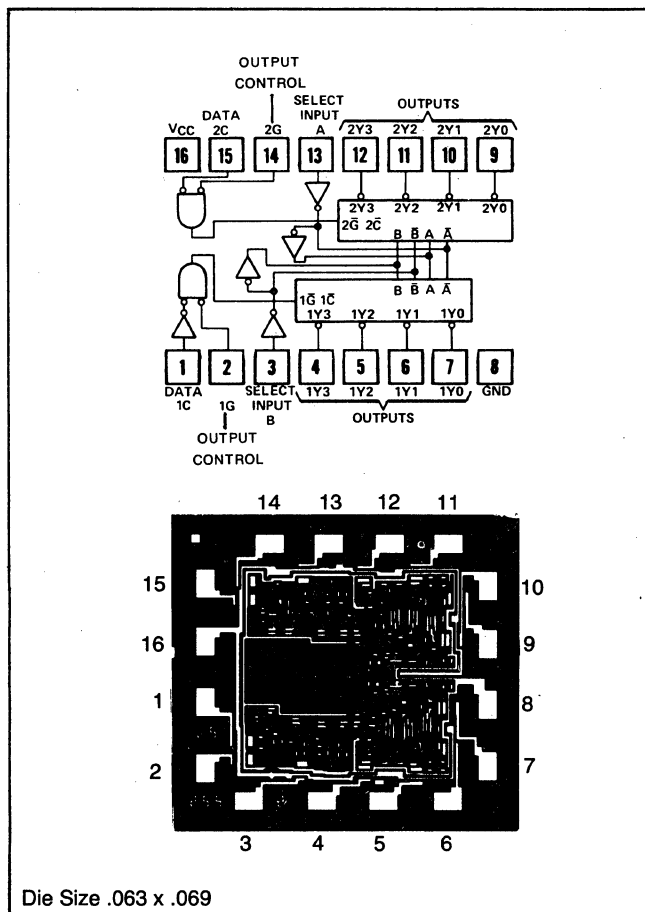
INPUTS				OUTPUTS			
SELECT	CONTROL	DATA					
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	Z	Z	Z	Z
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

**FUNCTION TABLES
2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER**

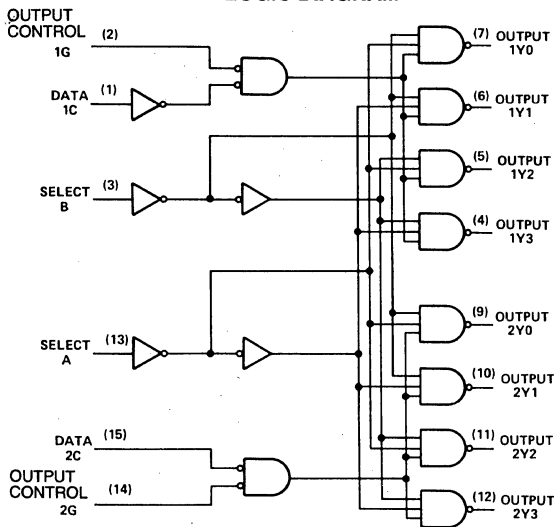
INPUTS				OUTPUTS							
SELECT	CONTROL OR DATA			(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together
 ‡G = inputs 1G and 2G connected together
 H = high level, L = low level, X = irrelevant, Z = high impedance (off)

PIN-OUT DIAGRAM



LOGIC DIAGRAM



Dual 2-Line-To-4-Line Decoder/Demultiplexer With Three-State Outputs

54LS255

Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			-1	mA
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	-55		125	°C

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.7	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL\text{max}}, I_{OH} = \text{MAX}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL\text{max}}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$	0.3	0.45	
$I_{O(\text{off})}$ Off-State (high-impedance state) output current	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}$	$V_O = 2.7 \text{ V}$		20	μA
		$V_O = 0.4 \text{ V}$		-20	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.36	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-6		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 1	Condition A	6	10	mA
		Condition B	11	17	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 1:

I_{CC} is measured with the outputs open under the following conditions:

A. A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

B. Same as Condition A except inputs 1G and 2G at 4.5 V.

Switching Characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

Parameter¶	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Unit
t_{PLH}	A, B, 1C or 2C	Y	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Fig. C on page 373		13	18	ns
t_{PHL}					16	22	
t_{PLH}	A or B (3 levels)	Y			16	22	ns
t_{PHL}					20	26	
t_{ZH}	Output Control	Y			10	15	ns
t_{ZL}					12	18	
t_{HZ}	Output Control	Y	$C_L = 5 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Fig. C on page 373		9	15	ns
t_{LZ}					15	20	

¶ t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

t_{ZH} = Output enable time to high level

t_{ZL} = Output enable time to low level

t_{HZ} = Output disable time from high level

t_{LZ} = Output disable time from low level



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Quadruple 2-Line-To-1-Line Multiplexers With Three-State Outputs

54LS257 54LS258

DESCRIPTION

These data selectors/multiplexers select a 4-bit word from one of two sources and present it at the four outputs. The 54LS257 presents true data; the 54LS258 presents inverted data. With Output Control HIGH, the outputs are forced to a high impedance state.

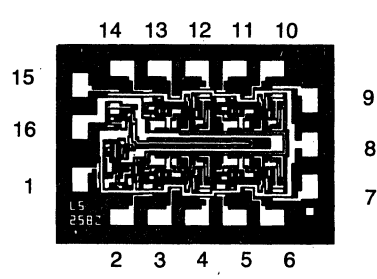
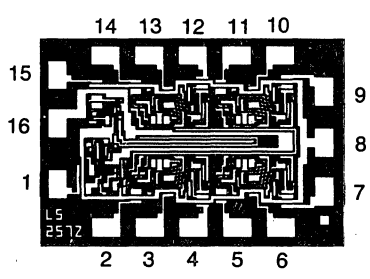
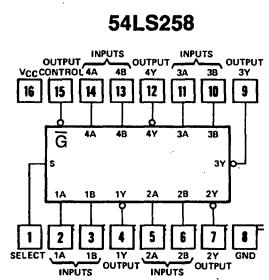
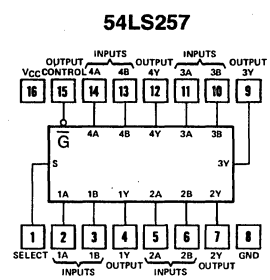
FUNCTION TABLE

OUTPUT CONTROL	INPUTS			OUTPUT Y	
	SELECT	A	B	54LS257	54LS258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

Low level at S selects A inputs.
High level at S selects B inputs.

PIN-OUT DIAGRAMS



Die Size .047 x .066

Die Size .047 x .066

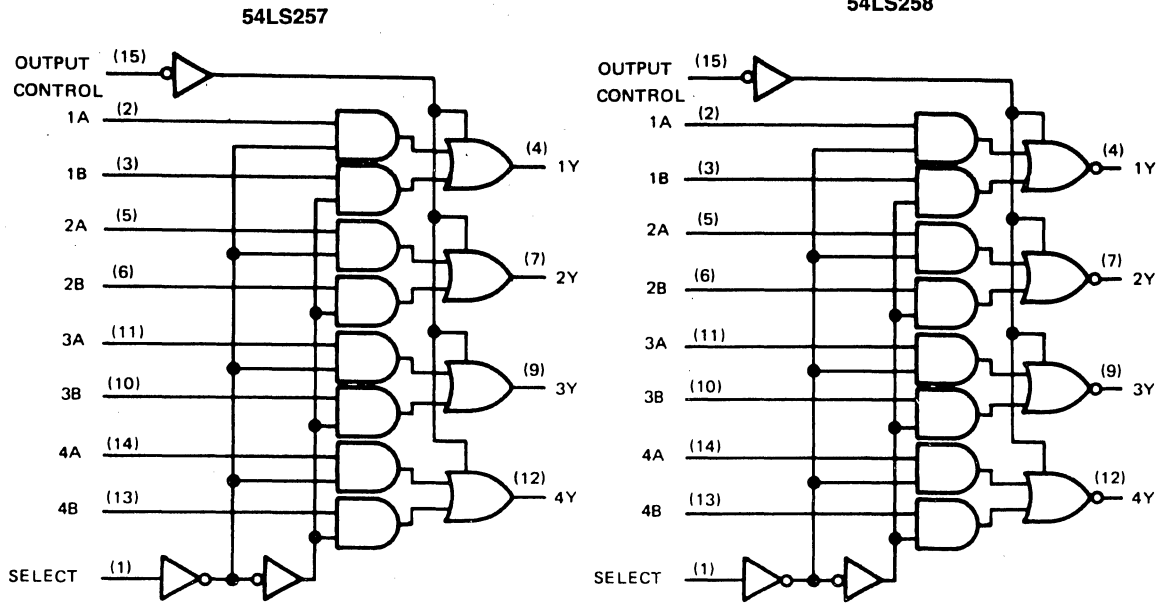


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Quadruple 2-Line-To-1-Line Multiplexers With Three-State Outputs

54LS257 54LS258

LOGIC DIAGRAMS



Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			-1	mA
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	-55		125	°C

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Quadruple 2-Line-To-1-Line Multiplexers With Three-State Outputs

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter		Test Conditions†	Min	Typ‡	Max	Unit	
V _{IH}	High-level input voltage		2			V	
V _{IL}	Low-level input voltage				0.7	V	
V _I	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5	V	
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{ILmax} , I _{OH} = MAX	2.4	3.4		V	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{ILmax}	I _{OL} = 4 mA	0.25	0.4	V	
			I _{OL} = 8 mA	0.3	0.45	V	
I _{OZH}	Off-state output current, high-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.4 V			20	μA	
I _{OZL}	Off-state output current, low-level voltage applied	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V			-20	μA	
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V	S input		0.2	mA	
			Any other		0.1		
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V	S input		40	μA	
			Any other		20		
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V	S input		-0.8	mA	
			Any other		-0.4		
I _{OS}	Short-circuit output current§	V _{CC} = MAX	-15		-100	mA	
I _{CC}	Supply current	V _{CC} = MAX, See Note 1	54LS257	All outputs high	5.9	10	mA
				All outputs low	9.2	16	
			All outputs off	10	17		
			54LS258	All outputs high	4.1	7	
				All outputs low	6.2	11	
			All outputs off	7.0	12		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC}=5 V, T_A=25°C.

§Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

NOTE: 1

I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

Switching Characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 2 kΩ

Parameter†	From (Input)	To (Output)	Test Conditions	54LS257			54LS258			Unit
				Min	Typ	Max	Min	Typ	Max	
t _{PLH}	Data	Any	C _L = pF, See Fig C on page 373	6	12		8	14	ns	
t _{PHL}				7	12		5	12		
t _{PLH}	Select	Any		12	18		12	18	ns	
t _{PHL}				12	18		10	18		
t _{ZH}	Output Control	Any		10	18		10	18	ns	
t _{ZL}				10	16		11	18		
t _{HZ}	Output Control	Any	C _L = 5 pF, See Fig C	10	15		9	15	ns	
t _{LZ}			10	18		8	15			

†t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{ZH} = output enable time to high level

t_{ZL} = output enable time to low level
t_{HZ} = output disable time from high level
t_{LZ} = output disable time from low level



4-Bit Bi-Directional Shift Register With Three-State Outputs

54LS295A

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FEATURES

- Three-state version of 54LS95B parallel-access shift register

DESCRIPTION

This 4-bit register features parallel inputs, parallel outputs, and clock, serial, mode, and output control inputs. The register has three modes of operation:

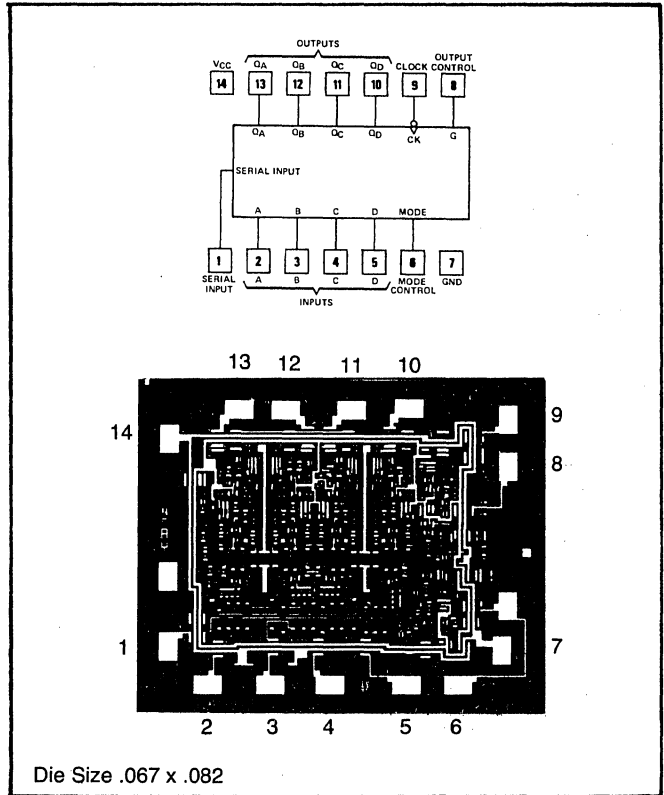
- Parallel (broadside) load
- Shift right (the direction Q_A toward Q_D)
- Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

Shift right is accomplished when the mode control is low; shift left is accomplished when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D.

When the output is high, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a low logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the register is not affected.

PINOUT DIAGRAM



FUNCTION TABLE

MODE CONTROL	CLOCK	SERIAL	INPUTS				OUTPUTS			
			A	B	C	D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	a	b	c	d	a	b	c	d
H	↓	X	$Q_{B†}$	$Q_{C†}$	$Q_{D†}$	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}

When the output control is low, the outputs are disabled to the high-impedance state; however, sequential operation of the registers is not affected.

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

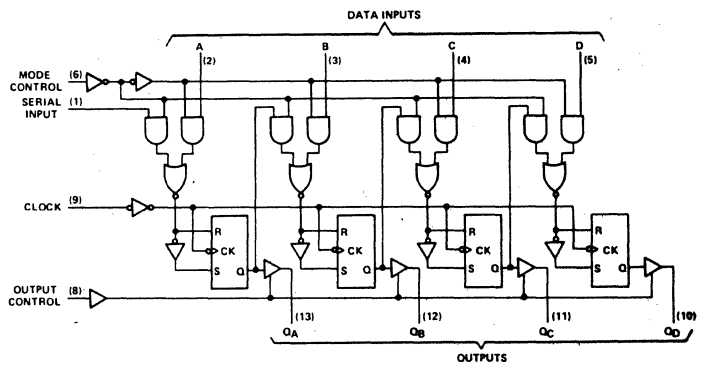
↓ = transition from high to low level.

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{A0} , Q_{B0} , Q_{C0} , Q_{D0} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the indicated steady-state input conditions were established.

Q_{An} , Q_{Bn} , Q_{Cn} , Q_{Dn} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the most-recent transition of the clock.

LOGIC DIAGRAM



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Recommended Operating Conditions

	Min	Nom	Max	Unit
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			-1	mA
Low-level output current, I_{OL}			8	mA
Clock frequency, f_{clock}	0		30	MHz
Width of clock pulse, $t_{w(clock)}$	20			ns
Setup time, high-level or low-level data, t_{setup}	10			ns
Hold time, high-level or low-level data, t_{hold}	10			ns
Operating free-air temperature, T_A	-55		125	°C

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions†	Min	Typ‡	Max	Unit
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.7	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{ILmax}$, $I_{OH} = \text{MAX}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{ILmax}$				V
				$I_{OL} = 4 \text{ mA}$	0.25
				$I_{OL} = 8 \text{ mA}$	0.3
I_{OZH} Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}$, $V_{IH} = V_{ILmax}$, $V_O = 2.7 \text{ V}$			20	μA
I_{OZL} Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $V_O = 0.4 \text{ V}$			-20	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.4	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-15		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 1				mA
			Condition A	14	23
			Condition B	15	25

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE: 1

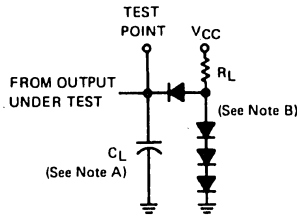
 I_{CC} is measured with the outputs open, the serial input and mode control at 4.5 V, and the data inputs grounded under the following conditions:

A. Output control at 4.5 V and a momentary 3 V, then ground, applied to clock input.

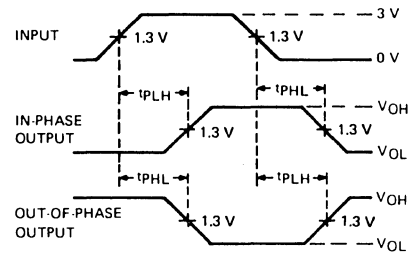
B. Output control and clock input grounded.

Switching Characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

Parameter	Test Conditions	Min	Typ	Max	Unit
f_{max} Maximum clock frequency		30	40		MHz
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}$		27	35	ns
t_{PHL} Propagation delay time, high-to-low-level output	$R_L = 2 \text{ k}\Omega$		35	45	ns
t_{ZH} Output enable time to high level	See Fig. C		10	18	ns
t_{ZL} Output enable time to low level	on page 373		10	18	ns
t_{HZ} Output disable time from high level	$C_L = 5 \text{ pF}$, $R_L = 2 \text{ k}\Omega$		19	28	ns
t_{LZ} Output disable time from low level	See Fig. C on page 373		24	32	ns

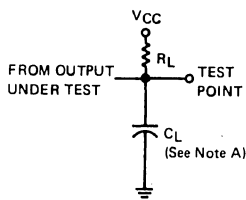


LOAD CIRCUIT

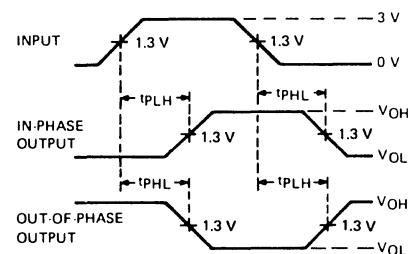


VOLTAGE WAVEFORMS

FIGURE A — FOR TOTEM-POLE OUTPUTS

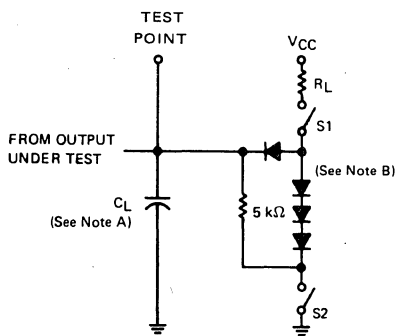


LOAD CIRCUIT

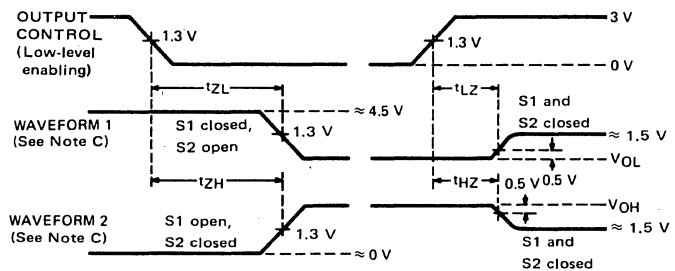


VOLTAGE WAVEFORMS

FIGURE B — FOR OPEN-COLLECTOR OUTPUTS



LOAD CIRCUIT



VOLTAGE WAVEFORMS

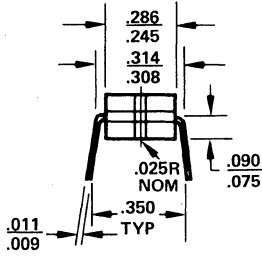
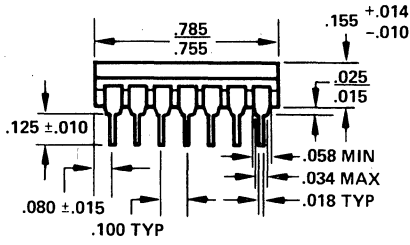
FIGURE C — FOR THREE-STATE OUTPUTS

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All diodes are 1N3064.
 - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 - E. All input pulses are supplied by generators having the following characteristics: $t_r \leq 15$ ns, $t_f \leq 6$ ns, $PRR \leq 1$ MHz, $Z_{out} \approx 50 \Omega$, and $t_w = 100$ ns.

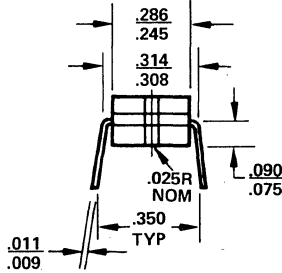
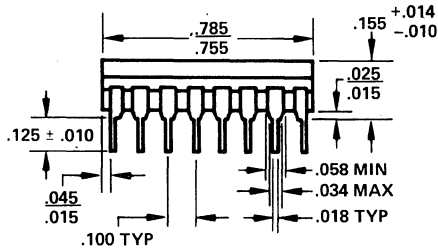


Packages Ordering Information

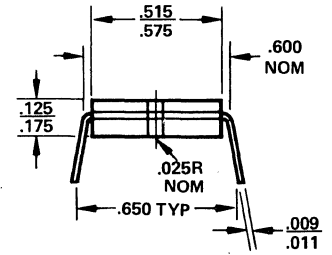
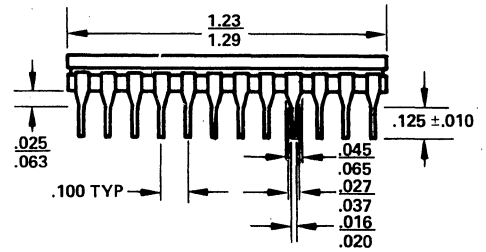
14-PIN CERDIP



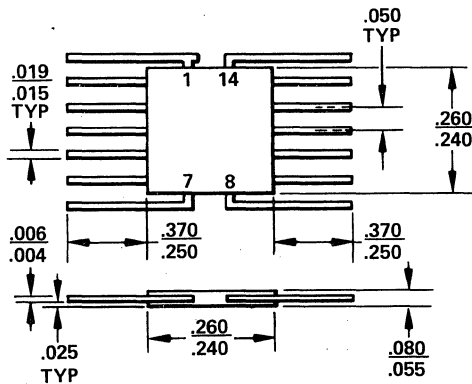
16-PIN J CIRDIP



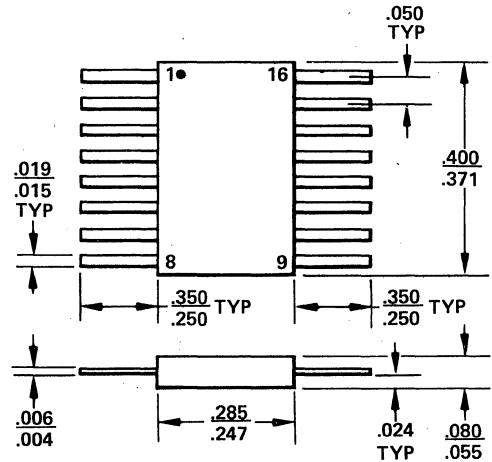
24-PIN J CERDIP



14 PIN W CERPAK



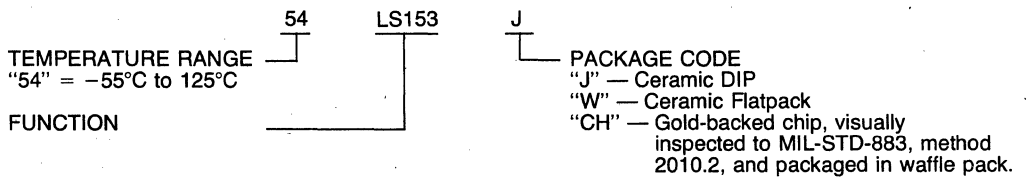
16 PIN W CERPAK



NOTES:

1. All dimensions in inches.
2. Leads are bright tin-plated.
3. Pin 1 orientation is by a notch in the pin 1 end of the J packages, by a tab on pin 1 of the 14 pin W package, and by a dot on the 16-pin W.

ORDERING INFORMATION



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RCA CD4000A-Series and CD4000B-Series Types COS/MOS Digital Integrated Circuits

Ratings, Operating Conditions, Static Characteristics Common To All Types

MAXIMUM RATINGS, Absolute-Maximum Values:

STORAGE-TEMPERATURE RANGE (T_{stg})	-65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):		
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPES E, Y	-40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})		
(Voltages referenced to V_{SS} Terminal):		
STANDARD "A"-SERIES TYPES	-0.5 to +15 V
HIGH-VOLTAGE "B"-SERIES TYPES	-0.5 to +20 V
POWER DISSIPATION PER PACKAGE (P_D):		
FOR $T_A = -40$ to +60°C (PACKAGE TYPES E, Y)	500 mW
FOR $T_A = +60$ to +85°C (PACKAGE TYPES E, Y)	Derate Linearly at 12 mW/°C to 200 mW
FOR $T_A = -55$ to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR $T_A = +100$ to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR		
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD} + 0.5$ V
LEAD TEMPERATURE (DURING SOLDERING):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

ELECTRICAL CHARACTERISTICS, Full-Temperature Range: $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$

CD4000A Standard Series

See pages 376 to 381

Conditions V_{DD} V	Output Voltage (At Indicated V_{IN} and V_{DD})				Maximum Input Current (I_{IL}, I_{IH}) μA	
	V_{IN} V	Low-Level (V_{OL}) Max. V		High-Level (V_{OH}) Min. V		
		Inverted	Non-Inverted	Inverted		Non-Inverted
5 10	0	-	0.05	4.95	-	
	0	-	0.05	9.95	-	
5 10	5	0.05	-	-	4.95	
	10	0.05	-	-	9.95	
15	-	-	-	-	±1	

CD4000B High-Voltage Series

See pages 380 to 383

Conditions V_{DD} V	V_{IN} V	Output Voltage (At Indicated V_{IN} and V_{DD})				Maximum Input Current (I_{IL}, I_{IH}) μA
		Low-Level (V_{OL}) Max. V		High-Level (V_{OH}) Min. V		
		Inverted	Non-Inverted	Inverted	Non-Inverted	
5 10 15	0	-	0.05	4.95	-	
	0	-	0.05	9.95	-	
	0	-	0.05	14.95	-	
5 10 15	5	0.05	-	-	4.95	
	10	0.05	-	-	9.95	
	15	0.05	-	-	14.95	
20	-	-	-	-	±1	

Conditions V_{DD} V	V_{IN} V	Noise Immunity (At $I_O = 10 \mu\text{A}$ and Indicated V_{IN} and V_{DD})				Minimum Noise Margin (V_{NM}) V
		(V_O) Min. V		(V_O) Max. V		
		Inverted	Non-Inverted	Inverted	Non-Inverted	
5 10	1.5	4.5	-	-	0.5	
	2	9	-	-	1	
5 10	3.5	-	4.5	0.5	-	
	8	-	9	1	-	
15	-	-	-	-	-	

Conditions V_{DD} V	V_{IN} V	Noise Immunity (At $I_O = 10 \mu\text{A}$ and Indicated V_{IN} and V_{DD})				Minimum Noise Margin (V_{NM}) V
		(V_O) Min. V		(V_O) Max. V		
		Inverted	Non-Inverted	Inverted	Non-Inverted	
5 10 15	1.5	4.5	-	-	0.5	
	2	9	-	-	1	
	2.5	13.5	-	-	1.5	
5 10 15	3.5	-	4.5	0.5	-	
	8	-	9	1	-	
	12.5	-	13.5	1.5	-	
20	-	-	-	-	-	

CD4000A Standard Series, Static Electrical Characteristics

COS/MOS "A" Series Type		Static, T _A = 25°C																		Max. "ON" Resistance	
		Max. Quiescent Device Current						Min. Output Drive Current													
		D,F,K,T Packages			E,Y Packages			D,F,K,T Packages						E,Y Packages							All Packages
		(I _L) μA			(I _L) μA			N Channel (Sink)(I _{DN}) mA			P-Channel (Source)(I _{DP}) mA			N-Channel (Sink)(I _{DN}) mA			P-Channel (Source)(I _{DP}) mA				
V _{DD} (V)	5	10	15	5	10	15	5	5	10	5	10	5	5	10	5	10	R _L = 10 kΩ				
V _O (V)							0.4	0.5	0.5	4.5	9.5	-0.4	0.5	0.5	4.5	9.5					
CD4000	0.05	0.1	50	0.5	5	50	0.4	-	0.9	-0.5▲	-0.5	0.3	-	0.6	-0.3▲	-0.25	-				
CD4001	0.05	0.1	50	0.5	5	50	0.4	-	0.9	-0.5▲	-0.5	0.3	-	0.6	-0.3▲	-0.25	-				
CD4002	0.05	0.1	50	0.5	5	50	0.4	-	0.9	-0.5▲	-0.5	0.3	-	0.6	-0.3▲	-0.25	-				
CD4006	0.5	1	500	5	10	500	-	0.125	0.25	-0.1	-0.2	-	0.06	0.125	-0.05	-0.1	-				
CD4007	0.05	0.1	50	0.5	1	50	0.6	-	1.3	-1.4▲	-1.1	0.3	-	1.0	-1.1▲	-0.55	-				
CD4008	5	10	500	50	100	500	-	0.25	0.75	-0.25	-0.75	-	0.13	0.5	-0.13	-0.5	-				
CD4009	0.3	0.5	50	3	5	50	3	-	8	-1.25▲	-0.6	3	-	8	-1.25▲	-0.6	-				
CD4010	0.3	0.5	50	3	5	50	3	-	8	-1.25▲	-0.6	3	-	8	-1.25▲	-0.6	-				
CD4011	0.05	0.1	50	0.5	5	50	-	0.25	0.5	0.25	-0.6	-	0.12	0.25	-0.12	-0.3	-				
CD4012	0.05	0.1	50	0.5	5	50	-	0.12	0.25	-0.25	-0.6	-	0.06	0.13	-0.12	-0.3	-				
CD4013	1	2	500	10	20	500	-	0.5	1	-0.25	-0.65	-	0.3	0.6	-0.14	-0.33	-				
CD4014	5	10	500	50	100	500	-	0.12	0.25	-0.08	-0.20	-	0.06	0.1	-0.05	-0.1	-				
CD4015	5	10	500	50	100	500	-	0.12	0.25	-0.08	-0.20	-	0.06	0.1	-0.05	-0.1	-				
CD4016	-	0.5	50	-	0.5	50	-	-	-	-	-	-	-	-	-	-	2000 at V _{DD} =10V 850 at V _{DD} =15V				
CD4017	5	10	500	50	100	500	-	0.05	0.1	-0.03	-0.1	-	0.025	0.07	-0.015	-0.07	-				
CD4018	5	10	500	50	100	500	-	0.15	0.35	-0.15	-0.35	-	0.08	0.25	-0.08	-0.25	-				
CD4019	5	10	500	50	100	500	-	0.45	0.75	-0.25	-0.7	-	0.30	0.65	-0.12	-0.5	-				
CD4020	15	25	500	50	100	500	-	0.075	0.15	-0.09	-0.20	-	0.08	0.10	-0.06	-0.15	-				
CD4021	5	10	500	50	100	500	-	0.12	0.25	-0.08	-0.20	-	0.06	0.1	-0.05	-0.1	-				
CD4022	5	10	500	50	100	500	-	0.05	0.1	-0.03	-0.1	-	0.025	0.05	-0.015	-0.05	-				
CD4023	0.05	0.1	50	0.5	5	50	-	0.25	0.5	-0.25	-0.6	-	0.12	0.25	-0.12	-0.3	-				
CD4024	5	10	500	50	100	500	-	0.25	0.5	-0.15	-0.35	-	0.12	0.25	-0.12	-0.25	-				
CD4025	0.05	0.1	50	0.5	5	50	0.4	-	0.9	-0.5▲	-0.5	0.3	-	0.6	-0.3▲	-0.25	-				
CD4026	5	10	500	50	100	500	-	0.12	0.25	-0.14	-0.3	-	0.06	0.12	-0.07	-0.15	-				
CD4027	1	2	500	10	20	500	-	0.5	1	-0.25	-0.65	-	0.3	0.6	-0.14	-0.33	-				
CD4028	5	10	500	50	100	500	-	0.6	1.2	-0.45	-0.95	-	0.3	0.6	-0.22	-0.48	-				
CD4029	5	10	500	50	100	500	-	0.4	0.6	-0.12	-0.2	-	0.2	0.3	-0.06	-0.1	-				
CD4030	0.5	1	50	5	10	50	-	0.6	1.2	-0.3	-0.65	-	0.3	0.6	-0.15	-0.32	-				
CD4031	10	25	500	50	100	500	-	0.09	0.2	-0.09	-0.2	-	0.045	0.1	-0.045	-0.1	-				
CD4032	5	10	500	50	100	500	-	0.5	0.7	-0.15	-0.55	-	0.2	0.5	-0.1	-0.27	-				
CD4033	5	10	500	50	100	500	-	0.12	0.25	-0.14	-0.3	-	0.06	0.12	-0.07	-0.15	-				
CD4034	5	10	500	-	-	500	-	0.1	0.25	-0.05	-0.125	-	-	-	-	-	-				
CD4035	5	10	500	50	100	500	-	0.5	1.25	-0.25	-0.65	-	0.35	0.85	-0.18	-0.45	-				
CD4036	5	10	500	-	-	500	-	0.03	0.075	-0.03	-0.075	-	-	-	-	-	-				
CD4037	5	10	500	50	100	500	-	0.7	1.1	-0.55	-0.75	-	0.35	0.55	-0.3	-0.4	-				
CD4038	5	10	500	50	100	500	-	0.5	0.7	-0.15	-0.55	-	0.2	0.5	-0.1	-0.27	-				
CD4039	5	10	500	-	-	500	-	0.03	0.075	-0.03	-0.075	-	-	-	-	-	-				
CD4040	15	25	500	50	100	500	-	0.145	0.4	-0.1	-0.25	-	0.08	0.2	-0.06	-0.15	-				
CD4041	1	2	50	10	20	50	1.6	-	5	-1.4	-4	0.8	-	2.5	-0.7	-2	-				
CD4042	1	2	500	10	20	500	-	0.4	1	-0.35	-0.9	-	0.2	0.5	-0.175	-0.45	-				
CD4043	1	2	500	10	20	500	-	0.2	0.5	-0.175	-0.4	-	0.1	0.25	-0.09	-0.2	-				
CD4044	1	2	500	10	20	500	-	0.2	0.5	-0.175	-0.4	-	0.1	0.25	-0.09	-0.2	-				
CD4045	15	25	500	50	100	500	-	3.5	5.5	-2.5	-4.5	-	1.8	2.8	-1.3	-2.3	-				
CD4046	15	60	500	15	60	500	-	0.43	1.3	-0.3	-0.9	-	0.43	1.3	-0.3	-0.9	-				
CD4047	5	10	500	50	100	500	-	0.4	1	-0.4	-1	-	0.28	0.7	-0.28	-0.7	-				
CD4048	1	2	500	10	20	500	1.6	-	4.5	-1.6	-4.5	1.6	-	4.5	-1.6	-3.15	-				
CD4049	0.3	0.5	50	3	5	50	3	-	8	-0.5	-1.25	3	-	8	-0.5	-1.25	-				
CD4050	0.3	0.5	50	3	5	50	3	-	8	-0.5	-1.25	3	-	8	-0.5	-1.25	-				

▲ V_O = 2.5 V ✱ V_{DD} = 4.5 V

CD4000A Standard Series, Dynamic Electrical Characteristics

DIGITAL

RCA Solid State

Dynamic, $T_A = 25^\circ\text{C}$; $C_L = 15\text{ pF}$ Unless Otherwise Specified; $C_I = 5\text{ pF}$ $t_r, t_f = 20\text{ ns}$													
COS/MOS "A" Series Type	Condi- tions	Max. Propagation Delay				Max. Transition Time				Max. Clock Input Frequency			
		D,F,K,T Packages		E,Y Packages		D,F,K,T Packages		E,Y Packages		D,F,K,T Packages		E,Y Packages	
		(t_{PHL}, t_{PLH}) ns		(t_{PHL}, t_{PLH}) ns		(t_{THL}, t_{TLH}) ns		(t_{THL}, t_{TLH}) ns		(f_{CL}) MHz		(f_{CL}) MHz	
$V_{DD}(V)$	5	10	5	10	5	10	5	10	5	10	5	10	
$V_O(V)$													
CD4000		50,95	40,45	80,120	55,65	125,175	70,75	200,300	115,125	—	—	—	—
CD4001		50,95	40,45	80,120	55,65	125,175	70,75	200,300	115,125	—	—	—	—
CD4002		50,95	40,45	80,120	55,65	125,175	70,75	200,300	115,125	—	—	—	—
CD4006		400	200	500	250	400	200	500	250	1	2.5	0.6	2
CD4007		60	40	75	50	75	40	100	50	—	—	—	—
CD4008		1300	500	2000	650	2200	900	2900	1100	—	—	—	—
CD4009		55,80	30,55	70,100	40,70	45,125	40,100	60,160	50,120	—	—	—	—
CD4010		55,80	30,55	70,100	40,70	45,125	40,100	60,160	50,120	—	—	—	—
CD4011		75	40	100	50	100,125	60,75	125,150	75,100	—	—	—	—
CD4012		75,150	40,75	100,200	50,100	100,375	60,200	125,500	75,250	—	—	—	—
CD4013		300	110	350	125	125	70	150	75	2.5	7	1	5
CD4014		750	225	1000	300	300	125	400	150	1	3	0.6	2.5
CD4015		750	225	1000	300	300	125	400	150	1	3	0.6	2.5
CD4016		—	20*	—	20*	—	—	—	—	—	—	—	—
CD4017		1200	400	1600	500	900	350	1200	450	1	3	0.6	2
CD4018		1200	400	1600	500	900	350	1200	450	1	1	0.6	2
CD4019		225	100	300	125	200	65	275	80	—	—	—	—
CD4020		600	225	650	250	600	300	650	350	1.5	4	1	3
CD4021		750	225	1000	300	300	125	400	150	1	3	0.6	2.5
CD4022		1200	400	1600	800	900	250	1200	500	1	3	0.6	2
CD4023		75	40	100	50	100,125	60,75	125,150	75,100	—	—	—	—
CD4024		350	150	400	150	225	150	250	150	1.5	4	1	3
CD4025		50,95	40,45	80,120	55,65	125,175	70,75	200,300	115,125	—	—	—	—
CD4026		1700	500	2200	700	900	350	1200	450	1.5	3	1	2
CD4027		300	110	400	150	125	70	250	140	1.5	4.5	1	3
CD4028		480	180	700	290	150	75	300	150	—	—	—	—
CD4029		650	230	1300	460	200	100	400	200	1.5	3	1	2
CD4030		200	100	300	150	150	75	300	150	—	—	—	—
CD4031		800	400	1600	800	150	60	300	120	0.8	2	0.4	1.0
CD4032		2200	500	2400	600	375	150	425	200	1.5	3	1	2
CD4033		1700	500	2200	700	900	350	1200	450	1.5	3	1	2
CD4034		1200	480	—	—	750	300	—	—	1.5	3	—	—
CD4035		500	200	700	300	200	100	300	150	1.5	3	1	2
CD4036		1000	400	1000	400	400	200	400	200	—	—	—	—
CD4037		500,450	150,180	700,650	200,250	80,150	30,120	120,200	40,180	—	—	—	—
CD4038		2200	500	2400	600	375	150	425	200	1.5	3	1	2
CD4039		1000	400	1000	400	400	200	400	200	—	—	—	—
CD4040		900	450	950	475	300	150	350	175	1	3.5	0.9	3.25
CD4041		100,100	45,40	125,125	65,60	60,55	40,40	80,75	50,50	—	—	—	—
CD4042		300	125	400	200	200	100	300	150	—	—	—	—
CD4043		350	175	400	200	200	100	250	125	—	—	—	—
CD4044		350	175	400	200	200	100	250	125	—	—	—	—
CD4045		4.4 [□]	2.4 [□]	5.5 [□]	3.3 [□]	800	650	900	750	4.4	8.5	3.5	6.5
CD4046		—	—	—	—	—	—	—	—	—	—	—	—
CD4047		1200	600	1600	800	125	75	150	100	—	—	—	—
CD4048		1300	400	1600	500	140,250	50,60	170,300	65,75	—	—	—	—
CD4049		55,80	30,55	110,140	55,85	45,100	40,60	45,100	40,60	—	—	—	—
CD4050		55,80	30,55	110,140	55,85	45,100	40,60	45,100	40,60	—	—	—	—

* Typical

□ μs

CD4000A Standard Series, Static Electrical Characteristics

COS/MOS "A" Series Type	Static, T _A = 25°C																	Max. "ON" Resistance	
	Condi- tions	Max. Quiescent Device Current						Min. Output Drive Current											All Packages
		D,F,K,T Packages			E,Y Packages			D,F,K,T Packages					E,Y Packages						
		(I _L) μA			(I _L) μA			N-Channel (Sink)(I _{DN}) mA		P Channel (Source)(I _{DP}) mA			N-Channel (Sink)(I _{DN}) mA		P-Channel (Source)(I _{DP}) mA				
V _{DD} (V)	5	10	15	5	10	15	5	5	10	5	10	5	5	10	5	10	R _L = 10 kΩ		
V _O (V)							0.4	0.5	0.5	4.5	9.5	0.4	0.5	0.5	4.5	9.5			
CD4051	5	10	500	50	100	500	-	-	-	-	-	-	-	-	-	-	-	2500 at V _{DD} =5V 400 at V _{DD} =10V 280 at V _{DD} =15V	
CD4052	5	10	500	50	100	500	-	-	-	-	-	-	-	-	-	-	-		
CD4053	5	10	500	50	100	500	-	-	-	-	-	-	-	-	-	-	-		
CD4054	-	10	20	-	10	20	-	-	0.9	-	0.45	-	-	0.6	-	-0.3	-	-	
CD4055	-	10	20	-	10	20	-	-	0.9	-	0.45	-	-	0.6	-	-0.3	-	-	
CD4056	-	10	20	-	10	20	-	-	0.9	-	0.45	-	-	0.6	-	-0.3	-	-	
CD4057	5	10	500	-	-	500	-	0.09	0.05	0.02	0.05	-	-	-	-	-	-	-	
CD4059	10	25	500	50	100	500	2	-	4	-0.4	-0.9	2	-	4	-0.4	-0.9	-	-	
CD4060	15	25	500	50	100	500	-	0.18	0.36	-0.125	-0.25	-	0.18	0.36	-0.125	-0.25	-	-	
CD4061	5	10	500	-	-	500	1.6	-	3.5	-0.4	-0.9	-	-	-	-	-	-	-	
CD4062	12	25	500	-	-	500	1.3	-	4	-0.25	-0.7	-	-	-	-	-	-	-	
CD4063	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4066	-	0.5	50	-	5	50	-	-	-	-	-	-	-	-	-	-	-	Note 1	
CD4067	5	10	500	50	100	500	-	-	-	-	-	-	-	-	-	-	-	Note 2	
CD4068	0.5	1	50	5	10	50	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4069	0.5	1	50	5	10	50	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4070	0.5	1	50	5	10	50	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4071	0.5	1	50	5	10	50	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4072	0.5	1	50	5	10	50	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4073	0.5	1	50	5	10	50	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4075	0.5	1	50	5	10	50	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4076	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4077	0.5	1	50	5	10	50	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4078	0.5	1	50	5	10	50	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4081	0.5	1	50	5	10	50	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4082	0.5	1	50	5	10	50	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4085	0.5	1	50	5	10	50	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4086	0.5	1	50	5	10	50	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4089	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4093	0.5	1	50	5	10	50	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4094	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4095	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4096	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4097	5	10	500	50	100	500	-	-	-	-	-	-	-	-	-	-	-	2500 at V _{DD} =5V 400 at V _{DD} =10V 280 at V _{DD} =15V	
CD4098	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4099	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4502	0.5	1	50	5	10	50	3.2	-	7.2	-0.4	-0.9	3.2	-	7.2	-0.4	-0.9	-	-	
CD4508	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4510	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4511	5	10	500	50	100	500	0.4	-	0.9	20‡	20‡	0.4	-	0.9	-20‡	-20‡	-	-	
CD4514	5	10	500	-	-	500	0.4	-	0.9	-0.2	-0.5	0.4	-	0.9	-0.2	-0.5	-	-	
CD4515	5	10	500	-	-	500	0.4	-	0.9	-0.2	-0.5	0.4	-	0.9	-0.2	-0.5	-	-	
CD4516	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4518	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	
CD4520	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	-	

Note 1: 5000 at V_{DD} = 5 V, 500 at V_{DD} = 10 V, 280 at V_{DD} = 15 V
 Note 2: 2500 at V_{DD} = 5 V, 400 at V_{DD} = 10 V, 280 at V_{DD} = 15 V

‡ V_O = 8.6 V

‡ V_O = 3.4 V

‡ V_{DD} = 4.5 V

CD4000A Standard Series, Dynamic Electrical Characteristics

DIGITAL

RCA Solid State

Dynamic, $T_A = 25^\circ\text{C}$; $C_L = 15\text{ pF}$ Unless Otherwise Specified; $C_1 = 5\text{ pF}$, $t_r, t_f = 20\text{ ns}$													
COS/MOS "A" Series Type	Condi- tions	Max. Propagation Delay				Max. Transition Time				Max. Clock Input Frequency			
		D,F,K,T Packages		E,Y Packages		D,F,K,T Packages		E,Y Packages		D,F,K,T Packages		E,Y Packages	
		$(t_{PHL}, t_{PLH})_{ns}$		$(t_{PHL}, t_{PLH})_{ns}$		$(t_{THL}, t_{TLH})_{ns}$		$(t_{THL}, t_{TLH})_{ns}$		$(f_{CL})_{MHz}$		$(f_{CL})_{MHz}$	
$V_{DD}(V)$	5	10	5	10	5	10	5	10	5	10	5	10	
$V_O(V)$													
CD4051		325 [•]	135 [•]	325 [•]	135 [•]	—	—	—	—	—	—	—	—
CD4052		325 [•]	135 [•]	325 [•]	135 [•]	—	—	—	—	—	—	—	—
CD4053		325 [•]	135 [•]	325 [•]	135 [•]	—	—	—	—	—	—	—	—
CD4054		900	600	1200	800	80	60	110	80	—	—	—	—
CD4055		900	600	1200	800	80	60	110	80	—	—	—	—
CD4056		900	600	1200	800	80	60	110	80	—	—	—	—
CD4057		3900	720	—	—	2775	1275	—	—	—	—	—	—
CD4059		360	180	360	180	70,200	40,100	70,200	40,100	—	—	—	—
CD4060		900	450	950	475	300	150	350	175	1	3	0.9	2.75
CD4061		750	380	—	—	100,60	75,40	—	—	1/1200	1/500	—	—
CD4062		1500	600	—	—	400,200	200,100	—	—	1.25	2.5	—	—
CD4063		1250	500	1250	500	200	100	200	100	—	—	—	—
CD4066		—	35 [•]	—	35 [•]	—	—	—	—	—	—	—	—
CD4067		325 [•]	135 [•]	325 [•]	135 [•]	—	—	—	—	—	—	—	—
CD4068		650,500	260,200	650,500	260,200	200	100	200	100	—	—	—	—
CD4069		125	80	125	80	200	100	200	100	—	—	—	—
CD4070		175 [•]	75 [•]	175 [•]	75 [•]	200	100	200	100	—	—	—	—
CD4071		500,350	200,140	500,350	200,140	200	100	200	100	—	—	—	—
CD4072		500,350	200,140	500,350	200,140	200	100	200	100	—	—	—	—
CD4073		320,420	130,170	320,420	130,170	200	100	200	100	—	—	—	—
CD4075		500,350	200,140	500,350	200,140	200	100	200	100	—	—	—	—
CD4076		600	250	600	250	200	100	200	100	—	—	—	—
CD4077		175 [•]	75 [•]	175 [•]	75 [•]	200	100	200	100	—	—	—	—
CD4078		400,850	160,340	400,850	160,340	200	100	200	100	—	—	—	—
CD4081		320,420	130,170	320,420	130,170	200	100	200	100	—	—	—	—
CD4082		320,420	130,170	320,420	130,170	200	100	200	100	—	—	—	—
CD4085		450,620	180,250	450,620	180,250	200	100	200	100	—	—	—	—
CD4086		450,700	180,280	450,700	180,250	200	100	200	100	—	—	—	—
CD4089		180 [•]	90 [•]	180 [•]	90 [•]	200	100	200	100	2 [•]	5 [•]	2 [•]	5
CD4093		600	300	600	300	200	100	200	100	—	—	—	—
CD4094		840	390	840	390	200	100	200	100	2.5	5	2.5	5
CD4095		500	200	500	200	200	100	200	100	3.5	8	3.5	8
CD4096		500	200	500	200	200	100	100	100	3.5	8	3.5	8
CD4097		325 [•]	135 [•]	325 [•]	135 [•]	—	—	—	—	—	—	—	—
CD4098		350 [•]	125 [•]	350 [•]	125 [•]	200	100	200	100	—	—	—	—
CD4099		220 [•]	90 [•]	220 [•]	90 [•]	200	100	200	100	—	—	—	—
CD4502		135,295 [•]	55,130 [•]	135,295 [•]	55,130 [•]	40,100 [•]	20,50 [•]	40,100 [•]	20,50 [•]	—	—	—	—
CD4508		220	90	220	90	200	100	200	100	—	—	—	—
CD4510		315 [•]	130 [•]	315 [•]	130 [•]	200	100	200	100	1.5	3	1.5	3
CD4511		720,640 [•]	290,250 [•]	720,640 [•]	290,250 [•]	125,40 [•]	75,30 [•]	125,40 [•]	75,30 [•]	—	—	—	—
CD4514		1100	450	1100	450	200,400	100,200	200,400	100,200	—	—	—	—
CD4515		1100	450	1100	450	200,400	100,200	200,400	100,200	—	—	—	—
CD4516		315 [•]	130 [•]	315 [•]	130 [•]	200	100	200	100	1.5	3	1.5	3
CD4518		560	230	560	230	200	100	200	100	1.5	3	1.5	3
CD4520		560	230	560	230	200	100	200	100	1.5	3	1.5	3

Note: $C_L = 50\text{ pF}$ for type CD4063 and for types CD4067 through CD40257.

** $V_{DD} = 12\text{ V}$, $V_{CC} = 5\text{ V}$, $V_{SS} = 0$

• Typical value

CD4000A Standard Series, Static Electrical Characteristics

COS/MOS "A" Series Type		Static, T _A = 25°C																Max. "ON" Resistance All Packages
		Max. Quiescent Device Current						Min. Output Drive Current										
		D,F,K,T Packages			E,Y Packages			D,F,K,T Packages					E,Y Packages					
		(I _L) μA			(I _L) μA			N-Channel (Sink)(I _{DN}) mA			P-Channel (Source)(I _{DP}) mA		N-Channel (Sink)(I _{DN}) mA			P-Channel (Source)(I _{DP}) mA		
V _{DD} (V)	5	10	15	5	10	15	5	5	10	5	10	5	5	10	5	10	R _L = 10 kΩ	
V _O (V)							0.4	0.5	0.5	4.5	9.5	0.4	0.5	0.5	4.5	9.5		
CD4527	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	
CD4532	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	
CD4555	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	
CD4556	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	
CD40100	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	
CD40101	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	
CD40102	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	
CD40103	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	
CD40104	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	
CD40107	0.5	1	50	5	10	50	12.8	-	28.8	-	-	12.8	-	28.8	-	-	-	
CD40108	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	
CD40109	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	
CD40181	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	
CD40182	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	
CD40192	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	
CD40193	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	
CD40194	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	
CD40257	5	10	500	50	100	500	0.4	-	0.9	-0.4	-0.9	0.4	-	0.9	-0.4	-0.9	-	

CD4000B High-Voltage Series, Static Electrical Characteristics

COS/MOS "B" Series Type		Static, T _A = 25°C																Max. "ON" Resistance All Packages
		Max. Quiescent Device Current						Min. Output Drive Current										
		D,F,K,T Packages			E,Y Packages			All Packages										
		(I _L) μA			(I _L) μA			N-Channel (Sink)(I _{DN}) mA					P-Channel (Source)(I _{DP}) mA					
V _{DD} (V)	5	10	15	20	5	10	15	20	5	10	15	5	5	10	15	R _L = 10 kΩ		
V _O (V)									0.4	0.5	1.5	2.5	4.6	9.5	13.5			
CD4000	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4001	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4002	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4008	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4009	0.5	1	2	50	5	10	20	50	1.6	3.6	12	-0.8	-0.2	-0.45	-1.5	-		
CD4010	0.5	1	2	50	5	10	20	50	1.6	3.6	12	-0.8	-0.2	-0.45	-1.5	-		
CD4011	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4012	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4013	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4016	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	2000 at V _{DD} =10 V 850 at V _{DD} =15 V		
CD4023	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4025	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4027	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4041	0.5	1	2	50	5	10	20	50	1.6	3.6	12	-6.4	-1.6	-3.6	-12	-		
CD4042	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4043	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4044	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4049	0.5	1	2	50	5	10	20	50	3.2	7.2	32	-1.6	-0.4	-0.9	-3	-		
CD4050	0.5	1	2	50	5	10	20	50	3.2	7.2	32	-1.6	-0.4	-0.9	-3	-		

CD4000A Standard Series, Dynamic Electrical Characteristics

COS/MOS "A" Series Type	Dynamic, T _A = 25°C; C _L = 15 pF Unless Otherwise Specified; C _I = 5 pF t _r , t _f = 20 ns												
	Condi- tions	Max. Propagation Delay				Max. Transition Time				Max. Clock Input Frequency			
		D,F,K,T Packages		E,Y Packages		D,F,K,T Packages		E,Y Packages		D,F,K,T Packages		E,Y Packages	
		(t _{PHL} , t _{PLH}) ns		(t _{PHL} , t _{PLH}) ns		(t _{THL} , t _{TLH}) ns		(t _{THL} , t _{TLH}) ns		(f _{CL}) MHz		(f _{CL}) MHz	
	V _{DD} (V)	5	10	5	10	5	10	5	10	5	10	5	10
	V _O (V)												
CD4527		180*	90	180*	90	200	100	200	100	—	—	—	—
CD4532		440	220	440	220	200	100	200	100	—	—	—	—
CD4555		440	190	440	190	200	100	200	100	—	—	—	—
CD4556		440	190	190	190	200	100	200	100	—	—	—	—
CD40100		350*	125*	350*	125*	200	100	200	100	3*	6*	3*	6*
CD40101		350*	125*	350*	125*	200	100	200	100	—	—	—	—
CD40102		250*	100*	250*	100*	200	100	200	100	2*	5*	2*	5*
CD40103		250*	100*	250*	100*	200	100	200	100	2*	5*	2*	5*
CD40104		350*	125*	350*	125*	200	100	100	100	3*	6*	3*	6*
CD40107		100,100*	40,60*	100,100*	40,60*	40,40*	20,35*	40,40*	20,35*	—	—	—	—
CD40108		350*	125*	350*	125*	200	100	200	100	—	—	—	—
CD40109		← 350	150*	→ 200	100	200	100	200	100	—	—	—	—
CD40181		715*	250*	715*	250*	200	100	200	100	—	—	—	—
CD40182		345*	140*	345*	140*	200	100	200	100	—	—	—	—
CD40192		775*	310*	775*	310*	200	100	200	100	3*	6*	3*	6*
CD40193		775*	310*	775*	310*	200	100	200	100	3*	6*	3*	6*
CD40194		350*	125*	350*	125*	200	100	200	100	3*	6*	3*	6*
CD40257		150*	75*	150*	75*	200	100	200	100	—	—	—	—

Note: C_L = 50 pF for type CD4063 and for types CD4067 through CD40257.

* Typical value

CD4000B High-Voltage Series, Dynamic Electrical Characteristics

COS/MOS "B" Series Type	Dynamic, T _A = 25°C; C _L = 50 pF; C _I = 5 pF; t _r , t _f = 20 ns										
	Condi- tions	Max. Propagation Delay			Max. Transition Time			Max. Clock Input Frequency			
		All Packages									
		(t _{PHL} , t _{PLH}) ns			(t _{THL} , t _{TLH}) ns			(f _{CL}) MHz			
	V _{DD} (V)	5	10	15	5	10	15	5	10	15	
	V _O (V)										
CD4000		75*	35*	25*	200	100	80	—	—	—	
CD4001		75*	35*	25*	200	100	80	—	—	—	
CD4002		75*	35*	25*	200	100	80	—	—	—	
CD4008		400*	160*	115*	200	100	80	—	—	—	
CD4009		30,80*	15,40*	10,30*	40,100*	20,50*	15,40*	—	—	—	
CD4010		40,80*	20,40*	15,30*	40,100*	20,50*	15,40*	—	—	—	
CD4011		75*	35*	25*	200	100	80	—	—	—	
CD4012		75*	35*	25*	200	100	80	—	—	—	
CD4013		175*	75*	50*	200	100	80	7*	16*	24*	
CD4016			40*	—	—	—	—	—	—	—	
CD4023		75*	35*	25*	200	100	80	—	—	—	
CD4025		75*	35*	25*	200	100	80	—	—	—	
CD4027		175*	75*	50*	200	100	80	7*	16*	24*	
CD4041		75*	35*	25*	75*	35*	25*	—	—	—	
CD4042		220*	90*	60*	200	100	80	—	—	—	
CD4043		220*	90*	60*	200	100	80	—	—	—	
CD4044		220*	90*	60*	200	100	80	—	—	—	
CD4049		30,80*	15,40*	10,30*	40,100*	20,50*	15,40*	—	—	—	
CD4050		40,80*	20,40*	15,30*	40,100*	20,50*	15,40*	—	—	—	

* Typical value

CD4000B High-Voltage Series, Static Electrical Characteristics

DIGITAL

RCA Solid State

COS/MOS "B" Series Type	Static, T _A = 25°C																Max. "ON" Resistance All Packages R _{ON} Ω R _L = 10 KΩ	
	Condi- tions	Max. Quiescent Device Current								Min. Output Drive Current								
		D,F,K,T Packages				E,Y Packages				All Packages								
		(I _L) μA				(I _L) μA				N-Channel (Sink)(I _{DN}) mA			P-Channel (Source)(I _{DP}) mA					
V _{DD} (V)	5	10	15	20	5	10	15	20	5	10	15	5	5	10	15			
CD4051	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4052	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4053	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4054	5	10	20	500	50	100	200	500	0.4	0.9	3	-0.8	-0.2	-0.45	-1.5	2500 at V _{DD} =5 V		
CD4055	5	10	20	500	50	100	200	500	0.4	0.9	3	-0.8	-0.2	-0.45	-1.5	400 at V _{DD} =10 V		
CD4056	5	10	20	500	50	100	200	500	0.4	0.9	3	-0.8	-0.2	-0.45	-1.5	280 at V _{DD} =15 V		
CD4063	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.45	-1.5	-		
CD4067	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.45	-1.5	2500 at V _{DD} =5 V 400 at V _{DD} =10 V 280 at V _{DD} =15 V		
CD4068	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.45	-1.5	-		
CD4069	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4070	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4071	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4072	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4073	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4075	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4076	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4077	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4078	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4081	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4082	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4085	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4086	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4089	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4093	0.5	1	2	50	5	10	20	50	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4094	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4095	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4096	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4097	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	2500 at V _{DD} =5 V 400 at V _{DD} =10 V 280 at V _{DD} =15 V		
CD4098	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4099	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4502	0.5	1	2	50	5	10	20	50	3.2	7.2	32	-1.6	-0.4	-0.9	-3	-		
CD4508	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4510	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4511	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-20 [‡]	-20 [‡]	-3	-		
CD4514	5	10	20	500	50	100	200	500	0.4	0.9	3	-0.8	-0.2	-0.45	-1.5	-		
CD4515	5	10	20	500	50	100	200	500	0.4	0.9	3	-0.8	-0.2	-0.45	-1.5	-		
CD4516	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4518	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4520	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4527	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4532	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4555	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD4556	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD40100	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD40101	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD40102	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD40103	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD40104	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD40105	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD40107	0.5	1	2	50	5	10	20	50	12.8	28.8	96	Open Drain				-		
CD40108	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD40109	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD40181	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD40182	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD40192	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD40193	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD40194	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		
CD40257	5	10	20	500	50	100	200	500	0.4	0.9	3	-1.6	-0.4	-0.9	-3	-		

‡ V_O = 8.6 V † V_O = 3.4 V

CD4000B High-Voltage Series, Dynamic Electrical Characteristics

COS/MOS "B" Series Type	Dynamic, $T_A = 25^\circ\text{C}$; $C_L = 50\text{ pF}$; $C_I = 5\text{ pF}$; $t_r, t_f = 20\text{ ns}$									
	Condi- tions	Max. Propagation Delay			Max. Transition Time			Max. Clock Input Frequency		
		All Packages								
	$V_{DD}(V)$	(t_{PHL}, t_{PLH}) ns			(t_{THL}, t_{TLH}) ns			(f_{CL}) MHz		
		$V_O(V)$	5	10	15	5	10	15	5	10
CD4051		325*	135*	95*	-	-	-	-	-	-
CD4052		325*	135*	95*	-	-	-	-	-	-
CD4053		325*	135*	95*	-	-	-	-	-	-
CD4054		-	800	500	-	200	150	-	-	-
CD4055		-	1300	750	-	200	150	-	-	-
CD4056		-	1300	750	-	200	150	-	-	-
CD4063		1250	500	350	200	100	80	-	-	-
CD4067		325*	135*	95*	-	-	-	-	-	-
CD4068		650,500	260,200	200,150	200	100	80	-	-	-
CD4069		125	80	60	200	100	80	-	-	-
CD4070		175	75	50	200	100	80	-	-	-
CD4071		500,350	200,140	150,110	200	100	80	-	-	-
CD4072		500,350	200,140	150,110	200	100	80	-	-	-
CD4073		320,420	130,170	100,130	200	100	80	-	-	-
CD4075		500,350	200,140	150,110	200	100	80	-	-	-
CD4076		600	250	180	200	100	80	-	-	-
CD4077		175*	75*	50*	200	100	80	-	-	-
CD4078		400,850	160,340	120,240	200	100	80	-	-	-
CD4081		320,420	130,170	100,130	200	100	80	-	-	-
CD4082		320,420	130,170	100,130	200	100	80	-	-	-
CD4085		450,620	180,250	130,180	200	100	80	-	-	-
CD4086		450,700	180,280	120,200	200	100	80	-	-	-
CD4089		220*	90*	60*	200	100	80	2*	5*	7.5*
CD4093		600	300	240	200	100	80	-	-	-
CD4094		840	390	270	200	100	80	2.5	5	6
CD4095		500	200	150	200	100	80	3.5	8	12
CD4096		500	200	150	200	100	80	3.5	8	12
CD4097		325*	135*	95*	-	-	-	-	-	-
CD4098		350*	125*	90*	200	100	80	-	-	-
CD4099		220*	90*	60*	200	100	80	-	-	-
CD4502		135,295*	55,130*	40,95*	40,100*	20,50*	15,40*	-	-	-
CD4508		220*	90*	60*	200	100	80	-	-	-
CD4510		315*	130*	100*	200	100	80	1.5	3	4
CD4511		720,640*	290,250*	200,180*	125,40*	75,30*	65,25*	-	-	-
CD4514		1100	450	300	200,400	100,200	80,160	-	-	-
CD4515		1100	450	300	200,400	100,200	80,160	-	-	-
CD4516		315*	130*	100*	200,400	100,200	80,160	1.5	3	4
CD4518		560	230	160	200	100	80	-	-	-
CD4520		560	230	160	200	100	80	-	-	-
CD4527		220*	90*	60*	200	100	80	3*	7*	10*
CD4532		440	220	170	200	100	80	-	-	-
CD4555		440	190	140	200	100	80	-	-	-
CD4556		440	190	140	200	100	80	-	-	-
CD40100		350*	125*	90*	200	100	80	3*	6*	9*
CD40101		350*	125*	90*	200	100	80	-	-	-
CD40102		250*	100*	75*	200	100	80	2*	5*	7.5*
CD40103		250*	100*	75*	200	100	80	2*	5*	7.5*
CD40104		350*	125*	90*	200	100	80	3*	6*	9*
CD40105		6000*	3000*	2000*	200	100	80	3*	6*	9*
CD40107		100,100*	40,60*	30,45*	40,40*	20,35*	15,30*	-	-	-
CD40108		350*	125*	90*	200	100	80	-	-	-
CD40109		350,150**			200	100	80	-	-	-
CD40181		715*	250*	180*	200	100	80	-	-	-
CD40182		345*	140*	110*	200	100	80	-	-	-
CD40192		775*	310*	235*	200	100	80	3*	6*	9*
CD40193		775*	310*	235*	200	100	80	3*	6*	9*
CD40194		350*	125*	90*	200	100	80	3*	6*	9*
CD40257		150*	75*	50*	200	100	80	-	-	-

* Typical

** $V_{DD} = 12\text{ V}$, $V_{CC} = 5\text{ V}$, $V_{SS} = 0$

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INTRODUCTION TO SIGNETICS LS

FEATURES OF LOW POWER SCHOTTKY TTL

Low Power, High Speed Operation

- 9.5ns typical gate propagation delay time (avg.)
- 2mw per gate power dissipation at 50% duty cycle — speed-power product = 19 picojoules typ.
- 45 MHz typical J-K Flip-Flop maximum clock frequency (D.C. coupled)

54/74 TTL performance at one fifth the power makes it possible to reduce size and cost of power supplies and eliminate cooling fans in 7400 type system designs. Manufacturing costs can be reduced by up to \$.10 per package by using Signetics Low Power Schottky in place of 54/74. The speed-power characteristics of Low Power Schottky are also such that many systems previously designed with a combination of 54/74 and 54L/74L can be immediately upgraded with 54LS/74LS resulting in little or no increase in power and possible reduction in component cost.

Fully Compatible with Other TTL Families

- Fan out of 5 7400 (2.5 5400) inputs or 4 74S/74H (2 54S/54H) loads.
- Low input current (.36 mA max) zero level input current.
- Pin, function speed compatible with 54/74.

Low Power Schottky has sufficient drive capability to interface with other TTL families in most applications without the need for buffer circuits. Thus it is possible to upgrade designs to Low Power Schottky as functions become available, using 5400/7400 functions where 54LS/74LS functions aren't yet available. The low input currents of Low Power Schottky make it an ideal interface between TTL compatible MOS devices and other systems.

versus 54LS/74LS geometries is shown in Figure 2. These techniques result in Low Power Schottky die areas being 60 to 75 percent the area of the equivalent 5400/7400 function. For example, the die size of the 54LS/74LS181 4-bit ALU is:

72 mils by 84 mils or 6048 square mils versus 90 mils by 92 mils, or 8280 square mils for the 54181/74181, or 75 percent of the area.

Future Trends

High circuit density, high speed and low power make Signetics Low Power Schottky a natural choice for high performance bipolar LSI designs such as microprocessors and large custom logic blocks. An example of an LSI product that has been developed by Signetics is a custom logic chip containing 270 equivalent logic gates on a 140x160 mil chip containing 1,590 components. This design resulted in a 40% improvement in performance, 80% reduction in power and 2:1 reduction in manufacturing cost. (see Table 1)

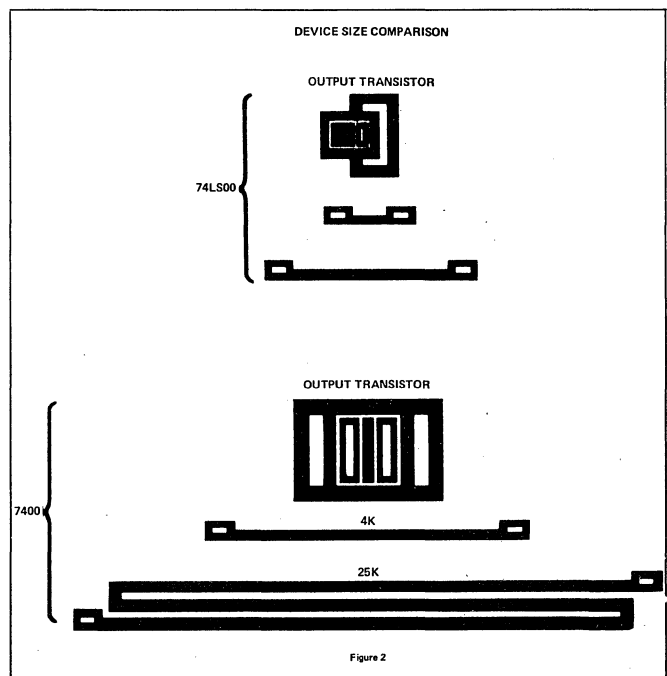
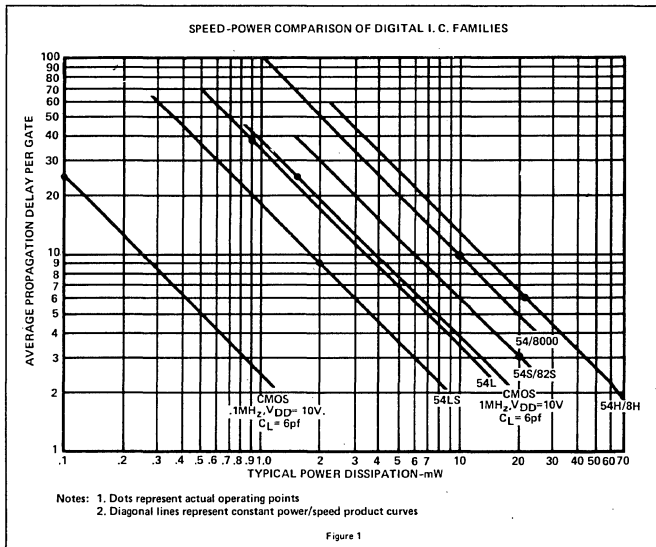
Table 1
COMPARISON OF TTL LSI VS. STANDARD TTL

	LSI	STD
Packages	1	26
Equivalent Gates	270	270
Power Dissipation	.65 watts	2.7 watts
Power/Gate	2.4 mW typ.	10.0 mW typ.
Speed	7ns/gate typ.	12ns /gate typ.

Thermal Considerations

TTL technology has now reached the level where maximum circuit complexity is often limited by package power capabilities. When standard TTL circuit designs are done with Low Power Schottky, circuit complexities can increase by a factor of five greater than standard designs without exceeding package power limitations as shown by Table 1.

Low Power Schottky's reduced power can also have a significant impact on component reliability in a system. For example, if we compare the reliability of a typical MSI function in a system with an operating ambient temperature of 55°C a four times improvement in component failure rate can result from the lower junction temperature of a Low Power Schottky function versus a standard 5400/7400 function. The Table 3 below and Figure 3 show a specific example of this improvement.



The high output current capability of 54LS/74LS Low Power Schottky enables it to drive a wide range of capacitive loads with minimum affect on device performance. This low impedance output characteristic also enables Low Power Schottky to drive reasonably long lines (up to 36 inches) without the need for terminated, controlled impedance lines.

ADVANTAGES OF LOW POWER SCHOTTKY

Circuit Density

74LS is fabricated using a thin epitaxial process to reduce parasitic capacitance. Low internal currents permit design of transistor geometries and metal widths to be the smallest allowable using state of the art mask and fabrication techniques. Further circuit density improvements are made by the use of ion implanted resistors. Greater than five times reduction in resistor geometries is made possible by this technique. A comparison of 5400/7400 geometries

Table 2
Military Commercial

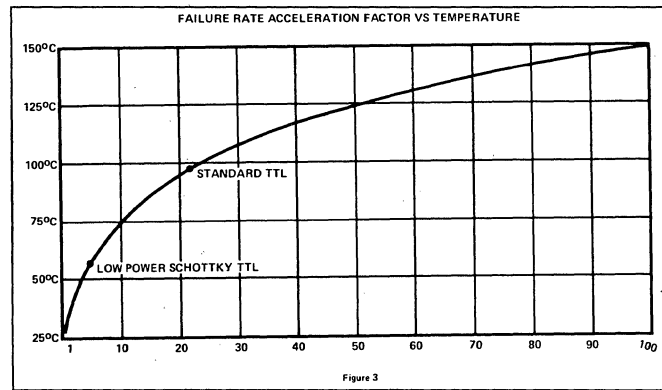
Maximum junction temperature	175°C	150°C
Maximum ambient temperature	125°C	70°C
Allowable thermal rise ambient to junction	50°C	80°C
Maximum allowable power dissipation	330 mw plastic ¹ 500 mw Cerdip ²	500 mw plastic ¹ 800 mw Cerdip ²
Maximum numbers of 5400 gates (at 10 mw/gate)	33 plastic	50 Cerdip
Maximum number of 54LS gates (at 2 mw/gate)	165 Plastic	80 Cerdip
	250 Cerdip	250 Plastic
		400 Cerdip

¹ ja for plastic = 160° C/watt (16 pin) ² ja for Cerdip = 100° C/watt (16 pin)

Table 3
Standard 54/74 54/74LS

Device Power	250mW	50 mW
Thermal impedance	150°C/watt	160°C/watt
Thermal rise	40°C	8°C
Junction temperature	95°C	63°C
Reliability factor*	22.5	5

*The reliability factor = $\frac{\text{Failure rate at operating junction temperature}}{\text{Failure rate at 25°C junction temperature}}$



COST REDUCTION

In comparing the cost of designing a system with a particular logic family, the project engineer should compare the total cost including reductions in manufacturing cost which may offset higher prices of a particular family. With low power logic, the cost savings associated with smaller, lower cost power supplies can be significant. As an example, a comparison will be made for the same system, using 54/74 logic, 54/74LS logic, CMOS logic and 54/74L. For purposes of comparison, a controller will be used. It consists of 500 packages, 200 quad NAND gates, 150 dual type D flip-flops and 150 presettable decade counters. It will be assumed that half of the system will operate at 200 kHz and half at 1 MHz. The CMOS system will operate at V_{DD} = 10 Volts with 15 pf. capacitance on each output. The part types used are shown in table 4.

Table 4

DEVICE	QUANTITY	54/74LS TYPE	STD TYPE	CMOS TYPE
Quad NAND Gate	200	54/74LS00	54/7400	4011
Dual D Flip-Flop	150	54/74LS74	54/7474	4013
Presettable Counter	150	54/74LS196	8280	4018

Table 5

DEVICE POWER REQUIREMENTS — Per Package (mW)

	54/74LS	STD TTL	CMOS	54/74L
Quad NAND Gate	8mW	40mW	Static-.05μWatt 200kHz-2.4mW 1MHz-10mW	4mW
Dual D Flip-Flop	20mW	85mW	Static-.2μWatt 200kHz-1.2mW 1MHz-4mW	10mW
Presettable Counter	60mW	185mW	Static-10μWatts 200kHz-1.2mW 1MHz-7mW	30mW

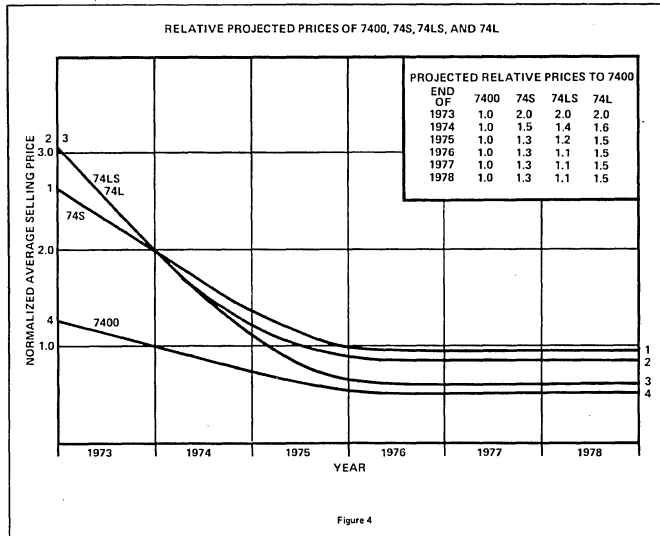
Table 6

SYSTEM POWER CONSUMPTION

		54/74LS	STD TTL	CMOS	54/74L
Gates	Static	1.6watts	8watts	.01mW	.8watts
	Dynamic	1.6watts	8watts	1.3watts	.8watts
Flip-Flops	Static	3watts	12.8watts	.03mW	1.5watts
	Dynamic	3watts	12.8watts	.4watts	1.5watts
Counters	Static	3watts	27.8watts	1.5watts	4.5watts
	Dynamic	9watts	27.8watts	.4watts	4.5watts
Total	Static	13.6watts	48.6watts	1.5mW	6.8watts
	Dynamic	13.6watts	48.6watts	2.1watts	6.8watts
Cost of Power	Static	\$13.60	\$48.60	0	\$6.80
	Dynamic	\$13.60	\$48.60	\$2.10	\$6.80
Cost of Power Per Package		\$.027	\$.097	\$.004	\$.014

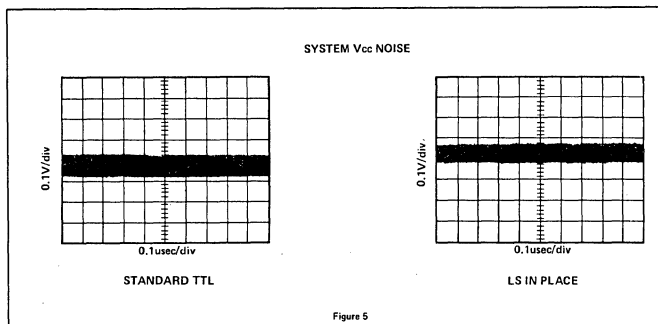
* Assume Power Costs \$1.00 Per Watt.

Although standard TTL is the lowest priced logic available today, and probably will be for some time to come, Signetics Low Power Schottky is the *most cost effective* form of logic to design your system with. Low Power Schottky prices are rapidly approaching 7400 as shown by Figure 4. Over the production life of your system, Low Power Schottky will result in the lowest overall manufacturing cost. If you are presently using low power TTL in your design you can affect an immediate cost reduction by replacing it with Low Power Schottky. Similarly, before designing a system with CMOS for lowest power supply costs, compare prices with Low Power Schottky. The difference in price may well offset the power supply savings. You also don't have the easy upgradability with CMOS.



UPGRADING A SYSTEM TO LOW POWER SCHOTTKY

To verify that 54/74LS can be plugged directly into a 54/74 system design, an experiment was conducted using an actual operating system. The system used for the experiment was a communications adapter that is designed to plug into a mini-computer frame. The board contains 103 TTL packages of which two thirds were MSI. All of the 7400 gates and flip-flops were replaced with equivalent 74LS types. System operation was not affected by the use of 74LS in place of 7400 in these sockets. In fact, in addition to the five to one reduction in power requirements for the devices replaced, the system power supply noise was reduced 25% from 80 millivolts to 60 millivolts as shown by Figure 5.



Based on results from this experiment and the characteristic data shown in the section on electrical characteristics, it is concluded that by observing a few simple guidelines, any system can be easily upgraded from 7400 to 74LS resulting in significant reduction in power consumption, system cooling requirements, and improved component reliability in the system.

DESIGN RULES FOR UPGRADING 54/74 SYSTEM TO 54/74LS

1. Check fan out requirements at each output node where a 54/74LS device may have to drive a 54/7400 device. Do not exceed 5 7400 loads or 2.5 5400 loads.
2. Check system set up and hold times for sequential functions to assure that data is available at the correct time for Low Power Schottky functions. These specifications are sometimes slightly different for 54/74LS types than they are for the corresponding 54/74 type.
3. Use standard 54/74 where it is necessary to drive heavy capacitive loads greater than 100pf—150pf.

Three benefits can be derived from the ability to upgrade 5400/7400 designs to 54/74LS.

1. The ability to immediately eliminate thermal heating problems in systems where it has been necessary to put a lot of logic in a small package such as terminals, point of sale systems, etc. A substantial reduction in heat generation can be affected by simply plugging in 54/74LS.
2. Redesign system to reduce power supply cost.
3. Upgrade system capability by adding plug in logic boards without having to redesign the power supply.

DESIGN RULES FOR UPGRADING 54/74L SYSTEM TO 54/74LS

1. Check power supply capability. 54/74LS SSI functions consume approximately twice the power of 54/74 SSI. However, a great many systems are a mix of 54/74L and standard 54/74. In these systems total power can often be reduced by replacing both the standard 54/74 and the 54L/74L with 54/74LS.
2. Check loading rules. The loading rules for 54/74L are almost identical to 54/74LS (See Tables 8 & 9). Generally, the only areas of concern are inputs from non-TTL elements such as linear devices, MOS, memories, CMOS or other devices with limited drive capability.
3. Check system timing. 54/74LS logic is much faster than 54/74L. Therefore, the designer should verify that no race conditions will be created which could affect system operation.

BENEFITS FROM REPLACING 54/74L WITH 54/74LS

1. Cost reduction — 54/74LS is less expensive than 54/74L. The cost difference will become even more significant in the future. (See Figure 4).
2. Availability — 54/74L is an obsolete logic family. Future availability of these devices could be a problem as IC manufacturers phase out production.
3. Inventory — By placing both 54/74 and 54/74L with 54/74LS, the total number of different devices to be tested and stored can be reduced.

CIRCUIT DESIGN

The standard gate circuit for the Signetics 54/74LS00 is shown in Figure 6. The threshold level is set at 1.5V at 25°C by the three base emitter diodes up from ground minus the input diode. This threshold provides a zero level noise immunity of 1.5—0.3 = 1.2V at 25°C by subtracting the low output level of the driving gate. At 125°C the noise immunity becomes 1.05—0.20 = .85V which is the worst case zero level. The worst case "one" level noise immunity is $V_{OH} - V_{THRESH}$ or 2.80—1.70 = 1.10V at -55°C. This circuit allows the guarantee of 0.8V for low level input voltage over the -55° to +125°C temperature range including open collector inverters specified at 100 micro amps high level output current. The combination of high threshold and fast turn-on speed is achieved with "kicker" transistor Q₂ which supplies an initial current surge during turn-on. D₃ also helps turn-on by supplying a quick dis-

charge path of the ISO transistor Q₆. The active pull down circuit consisting of Q₄, R₆, and R₇, provides a good V_{in} vs V_{out} characteristic for best noise immunity. The ISO resistor R₃ is low at 120 ohms. The ISO current is typically 30mA which makes it near the capability of standard 7400 in charging highly capacitive bus lines. The base drive to the output transistor Q₅ is at least 0.3mA. With a typical beta of 40 the output sink current will generally be more than 12 mA through a collector resistance of 20 ohm.

D.C. CHARACTERISTICS

Low Power Schottky has basically the same input and output voltage levels as standard TTL. Input current requirements are reduced to 0.36mA for logic "0" state and -20µa for logic "1" state. Output currents are also reduced to 4mA/8mA for 54/74LS in logic "0" state and 400µA for logic "1" state. Table 7 shows the d.c. characteristics for both 54/74LS and 54/74.

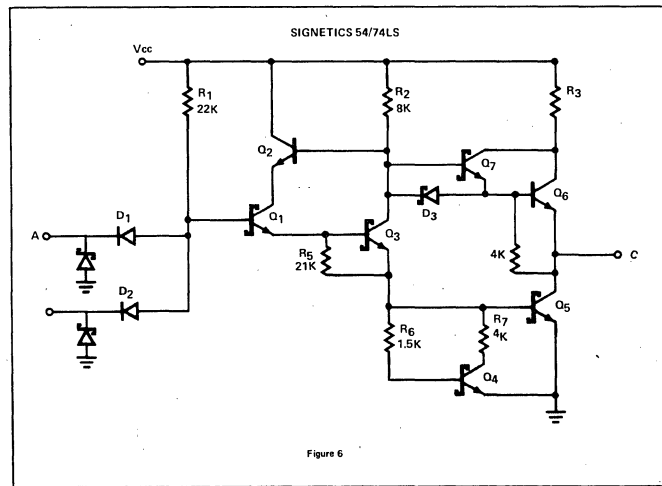


Figure 6

Table 7

PARAMETER	54LS	74LS	54	74	UNIT
V _{IH} High level input voltage	2 (min)	2 (min)	2 (min)	2 (min)	V
V _{IL} Low level input voltage	0.8 (max)	0.8 (max)	0.8 (max)	0.8 (max)	V
V _{OH} High level output voltage	2.5 (min)	2.7 (min)	2.4 (min)	2.4 (min)	V
V _{OL} Low level output voltage	0.4 (max)	0.5 (max)	0.4 (max)	0.4 (max)	V
I _{IH} High level input current	20 (max)	20 (max)	40 (max)	40 (max)	µA
I _{IL} Low level input current	-0.36 (max)	-0.36 (max)	-1.6 (max)	-1.6 (max)	mA
I _{OH} High level output current	-400 (min)	-400 (min)	-400 (min)	-400 (min)	µA
I _{OL} Low level output current	4 (min)	8 (min)	16 (min)	16 (min)	mA

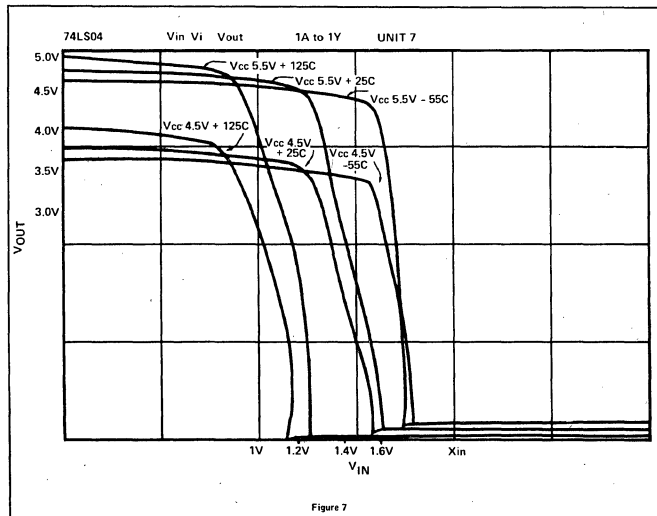


Figure 7

DC NOISE MARGIN

54/74LS devices have slightly higher minimum logic "1" input voltage while maintaining the same maximum logic "1" output voltage, therefore noise margin for 54/74LS in the logic "1" state is improved over that of 54/74. Noise margin in logic "0" state remains the same except for 74LS devices, which have a maximum of 0.5V output, instead of 0.4V, thus have a reduction of 100mv in logic "0" state. Table 10 shows the noise margin for both families.

Table 8 D.C. NOISE MARGIN (VOLTS)

	54	74	54LS	74LS
Logic "1"	0.4	0.4	0.7	0.5
Logic "0"	0.4	0.4	0.4	*0.3

*74LS NOISE MARGIN IS 0.4V at 4ma out (11 loads)

UNUSED INPUTS OF POSITIVE AND/NAND GATES

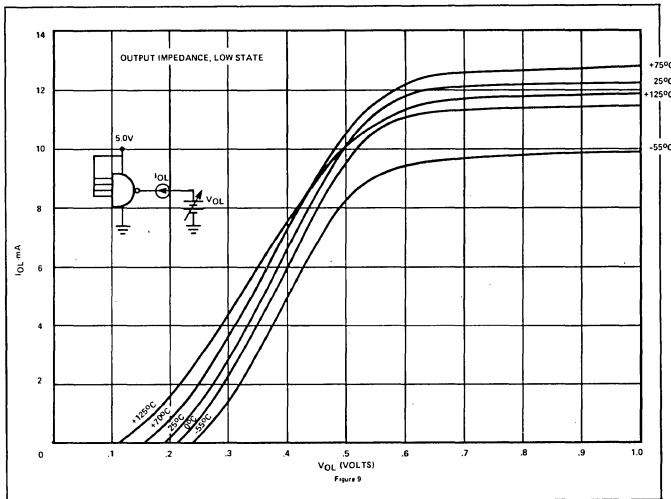
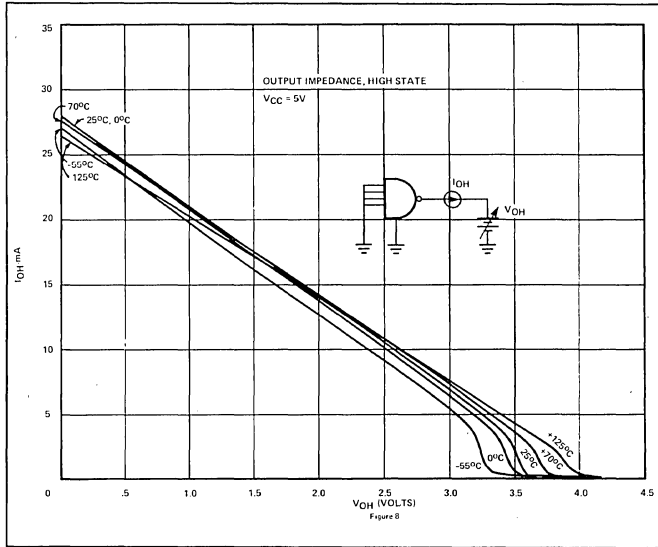
For optimum switching times and minimum noise susceptibility, unused inputs of AND or NAND gates should be maintained at a voltage greater than 2.7V, but not exceed the absolute maximum rating of 5.5V. This eliminates the distributed capacitance associated with the floating input, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times.

Possible ways of handling unused inputs are:

1. Connect unused inputs to an independent supply voltage. Preferably this voltage should be between 2.7V and 3.5V.
2. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each additional input presents a full load to the driving output at a high level voltage but adds no loading at a low level voltage.
3. Connect unused inputs to V_{CC} through a 1K ohm resistor so that if a transient which exceeds the 5.5V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1K ohm resistor.
4. Connect unused inputs to the output of an inverter that has its input grounded.

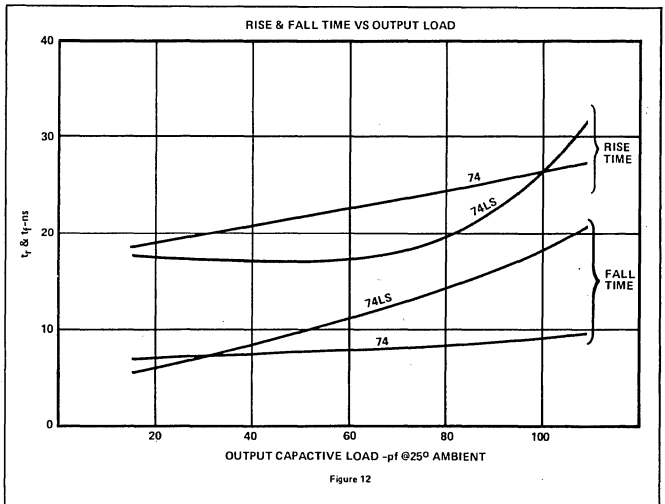
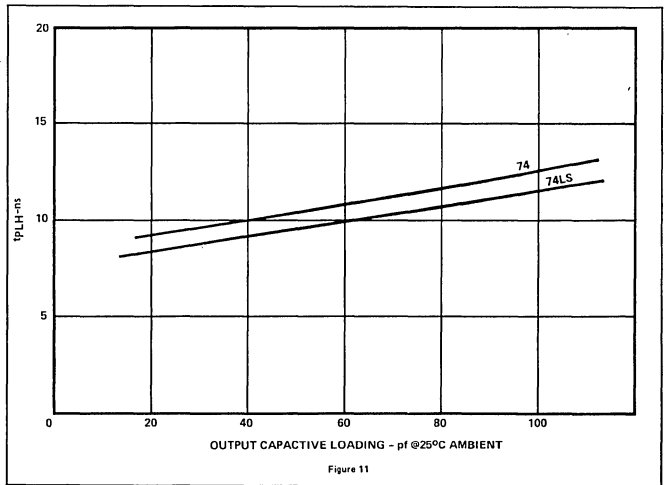
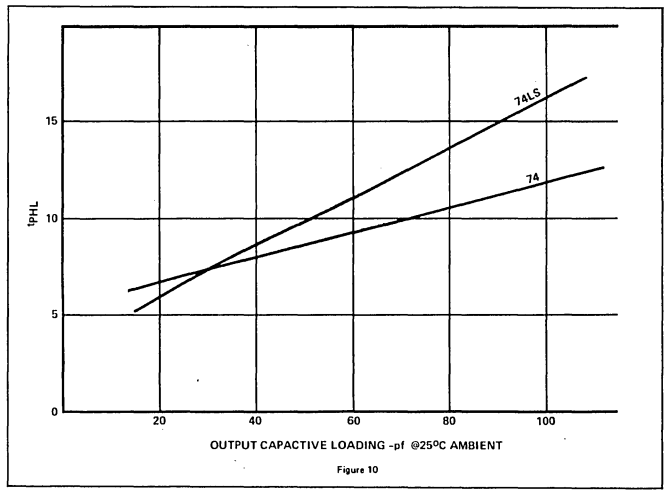
LINE DRIVING AND RECEIVING

The Low Power Schottky displays similar line driving and receiving capability as the standard TTL logic. Low Power Schottky is slightly more sensitive to the transmission line effect when driving longer lines due to the low output impedance of the circuit. Figures 15 through 22 show the driving and receiving capability of the LS and standard TTL over 12 and 36 inch lines. Even though the LS is more sensitive to transmission line effects, the point to be noted is that the LS output of the receiver display has a much cleaner waveform than the standard logic. The ringing effect of the standard logic is almost negligible in the LS. Test configuration is shown as follows with $V_{CC} = 5.0V$, $T_A = 25^\circ C$, and $C_L = 15pf$.



A.C. CHARACTERISTICS

Fig. 10 to 14 illustrate the propagation delays, rise and fall times, and AC over temperature. The LS devices display similar transfer characteristics as standard TTL and meet all the worst case conditions. Propagation delays are similar on turn off and faster on turn on. Edge speed is generally slower in LS than standard, thus creates less cross-talk, V_{CC} noise, etc.



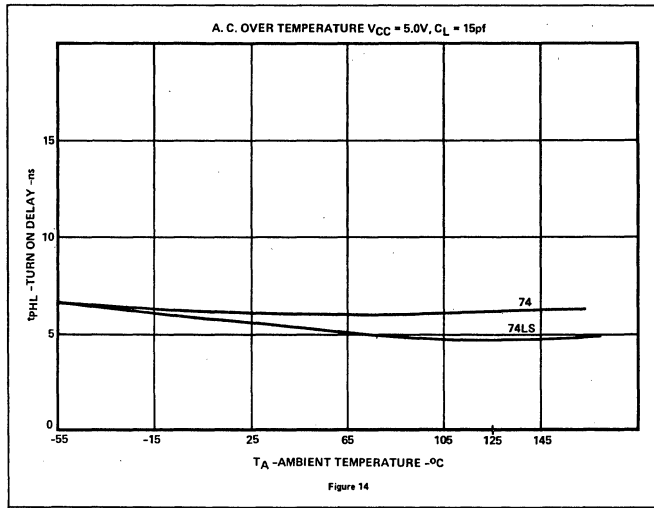
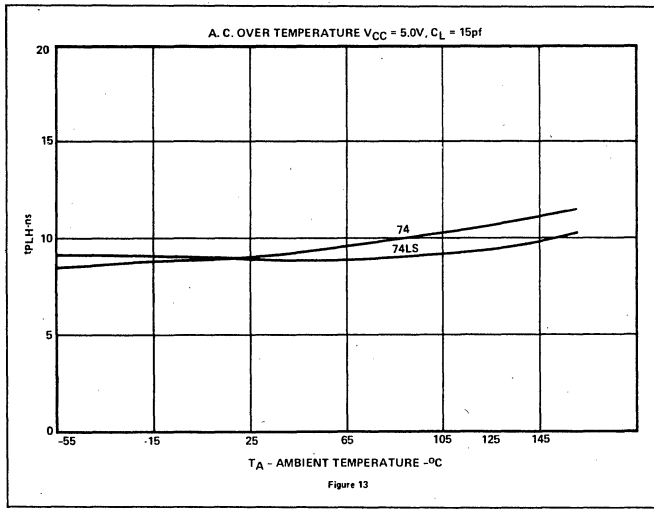


TABLE 9
FANOUT (0° — $70^{\circ}C$) LOGIC 1/LOGIC 0
DRIVING GATES

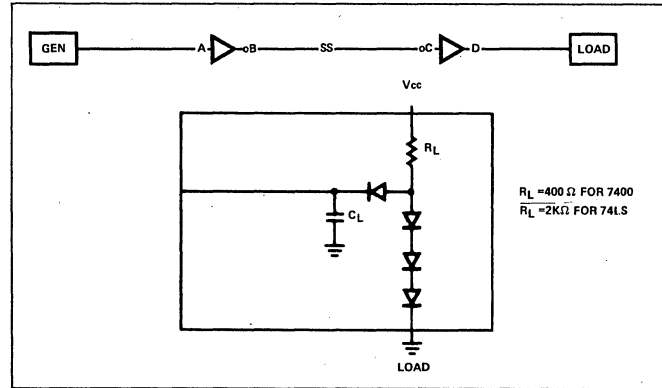
	74	74L	74LS
74	10/10	5/2	10/5
74L	40/89	20/20	40/44
74LS	20/44	10/10	20/22

DRIVEN GATES

TABLE 10
FANOUT ($-55^{\circ}C$ TO $+125^{\circ}C$) LOGIC 1/LOGIC 0
DRIVING GATES

	54	54L	54LS
54	10/10	2/1	10/2
54L	40/89	10/11	40/22
54LS	20/44	5/5	20/11

DRIVEN GATES



DESIGN GUIDELINES

Fanout Capabilities

Low Power Schottky has high fan-out capabilities both in the logic "0" and logic "1" state. Within the family Low Power Schottky can fan-out to 22 in logic "0" state and 20 in logic "1" state.

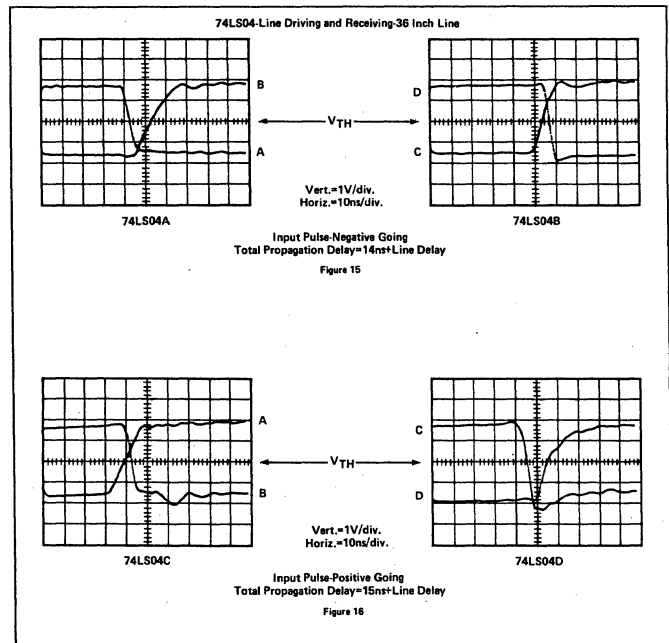
Fan-out capability is calculated by dividing the output current of the driving gate by the input current of the driven gate. For example, if a 74 gate is driving another 74 gate, the fan-out capability would be:

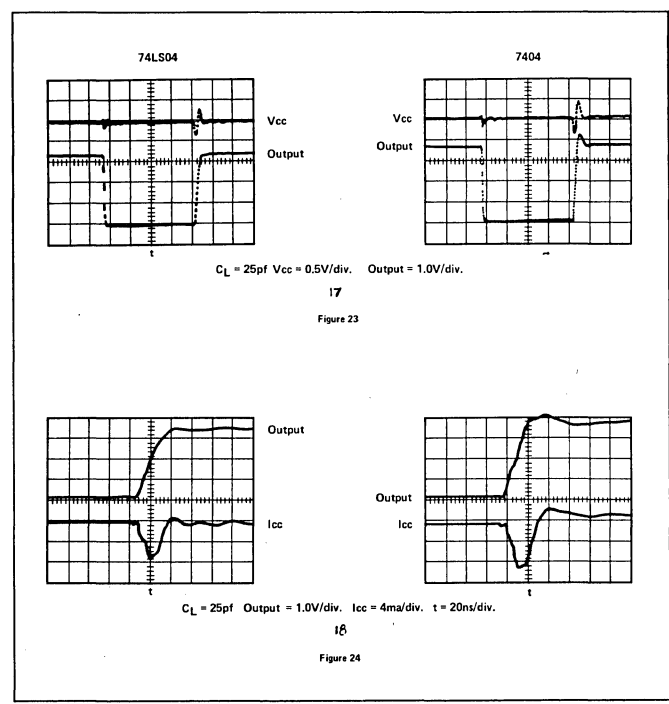
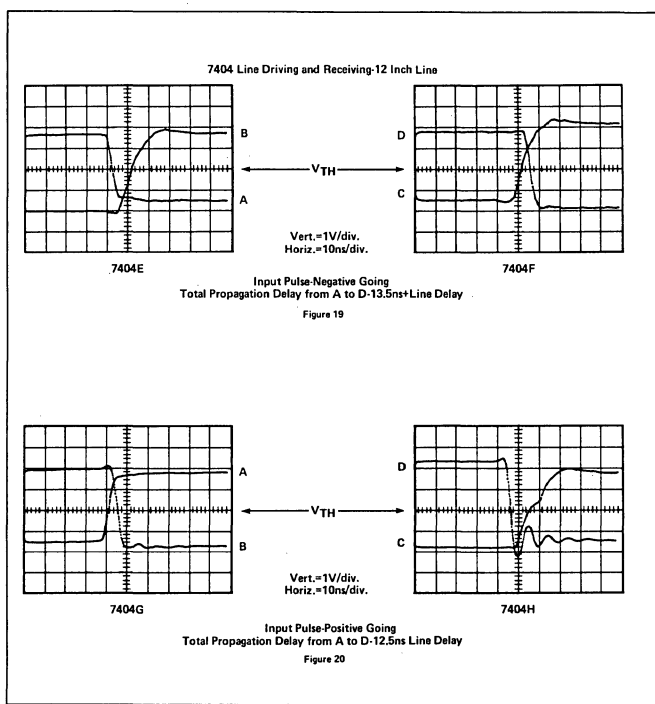
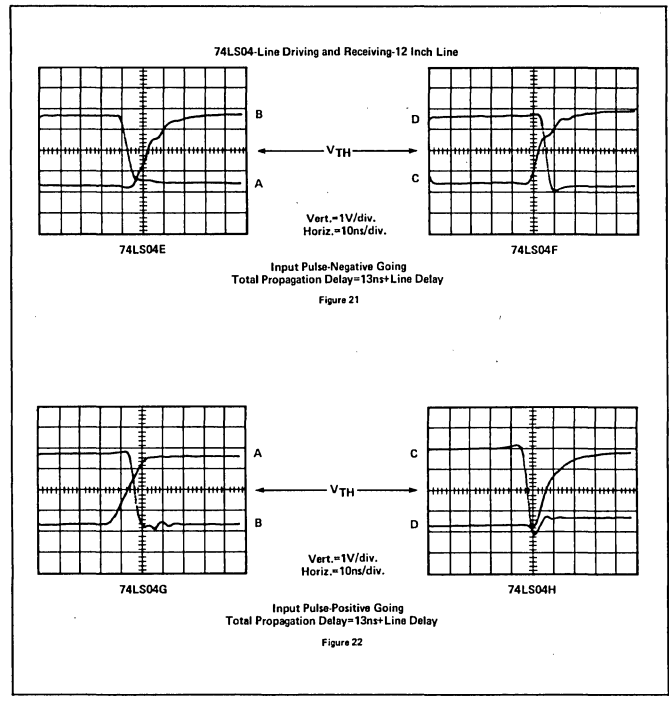
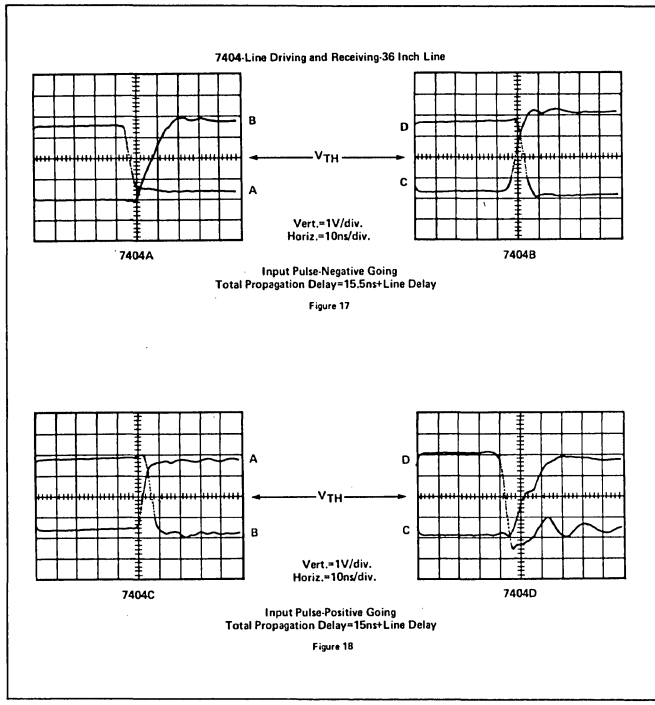
$$F.O. = \frac{16ma}{1.6ma} = 10 \text{ for logic "0" state}$$

and

$$F.O. = \frac{400\mu a}{40\mu a} = 10 \text{ for logic "1" state}$$

Referring to Table 7 for current requirements, we can calculate the fan-out for 54/74LS and 54/74 families. Tables 8 and 9 show the fan-out capabilities between these two families.



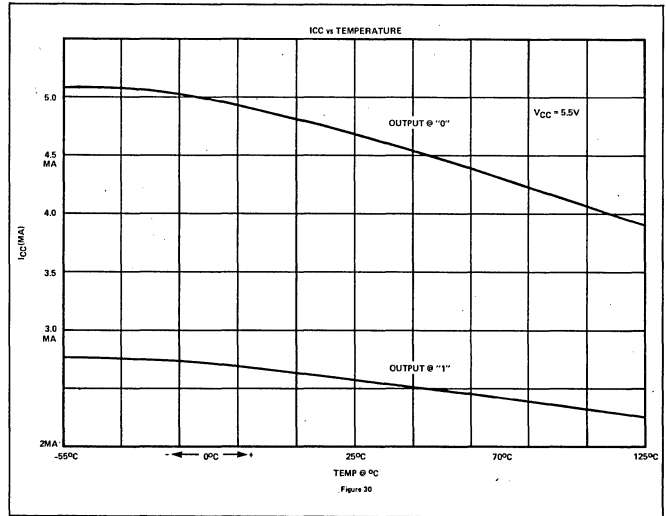
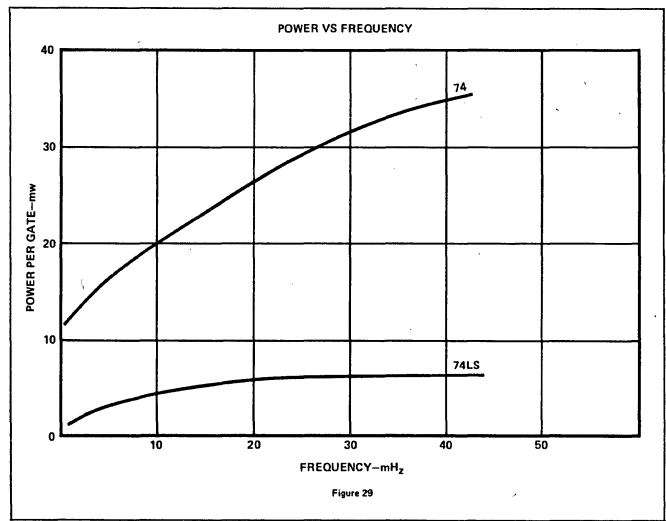
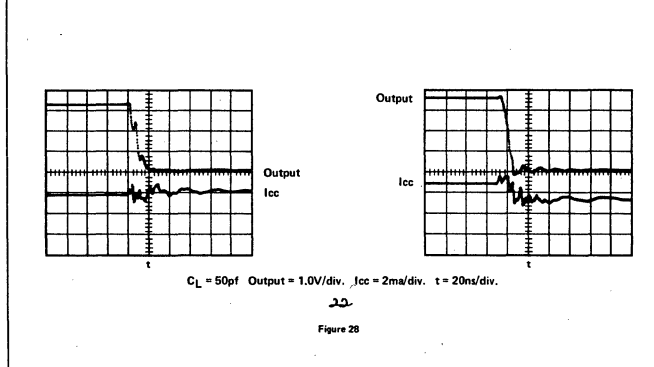
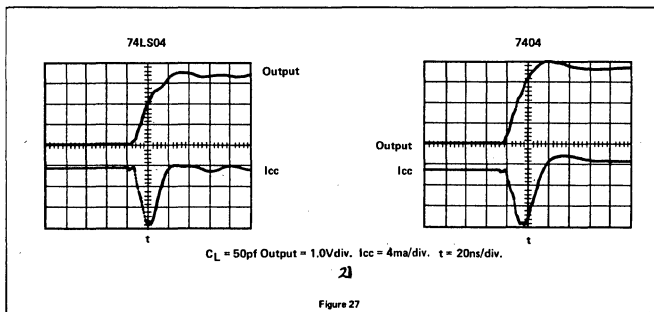
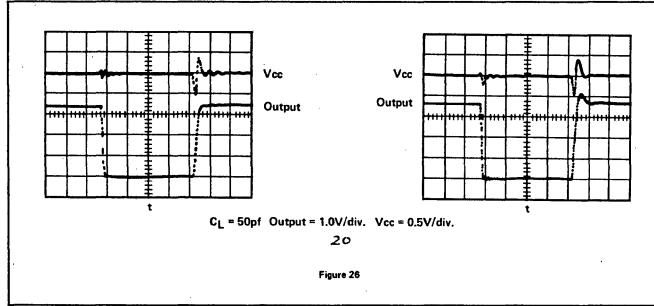
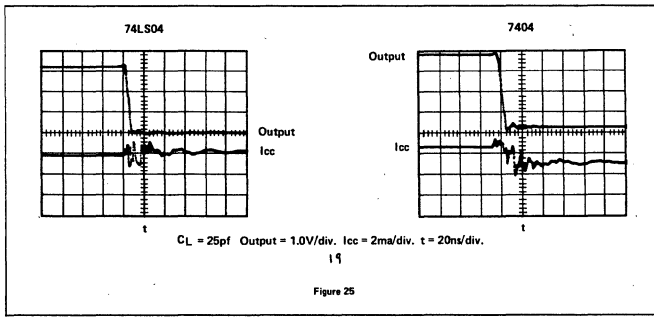


POWER SUPPLY CONSIDERATIONS

Decoupling

Current spiking and V_{CC} noise are generated internally within the circuits due to overlap in conduction of the upper and lower transistors in the totem pole outputs, the difference in I_{CH} and I_{CL} and the changing of load capacitances. The power supply decoupling rules for standard TTL apply to Low Power Schottky also, i.e. 0.01uF per synchronously driven gate and at least 0.1uF per 20 gates regardless of synchronization.

Figure 17 to 22 display the current spikes and V_{CC} noise generated by a 7404 and 74LS04 with two different capacitive loading @ $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$. In both cases, the LS device generates less V_{CC} noise and smaller current spikes for 25 pf. and 50 pf. capacitive loading. This is because Low Power Schottky generally switches approximately 25% of the current as a standard TTL would, thus less current spiking and less V_{CC} noise generated.



ON-BOARD REGULATION

In most digital systems, there is a large current requirement, and the current supplied usually comes from a main supply. TTL logic tends to generate current spikes during switching due to the overlap in conduction of both upper and lower transistors, thus creating VCC noise. An on-board voltage regulator could be used not only to regulate the power supplied to the circuits on-board, but also would isolate the noise otherwise propagated to the rest of the system. Systems designed using this technique would not need tight regulation on the main power supply.

Most voltage regulator circuits can supply up to 1 Amp of current. For systems with large boards (150 or more IC's), two or three regulator circuits might be needed to supply enough current to standard TTL logic. However, for Low Power Schottky systems, one regulator per board should be sufficient. This represents approximately 1 cent per package of Low Power Schottky vs 5 cents per package for standard TTL for large boards.

ABSOLUTE MAXIMUM RATINGS

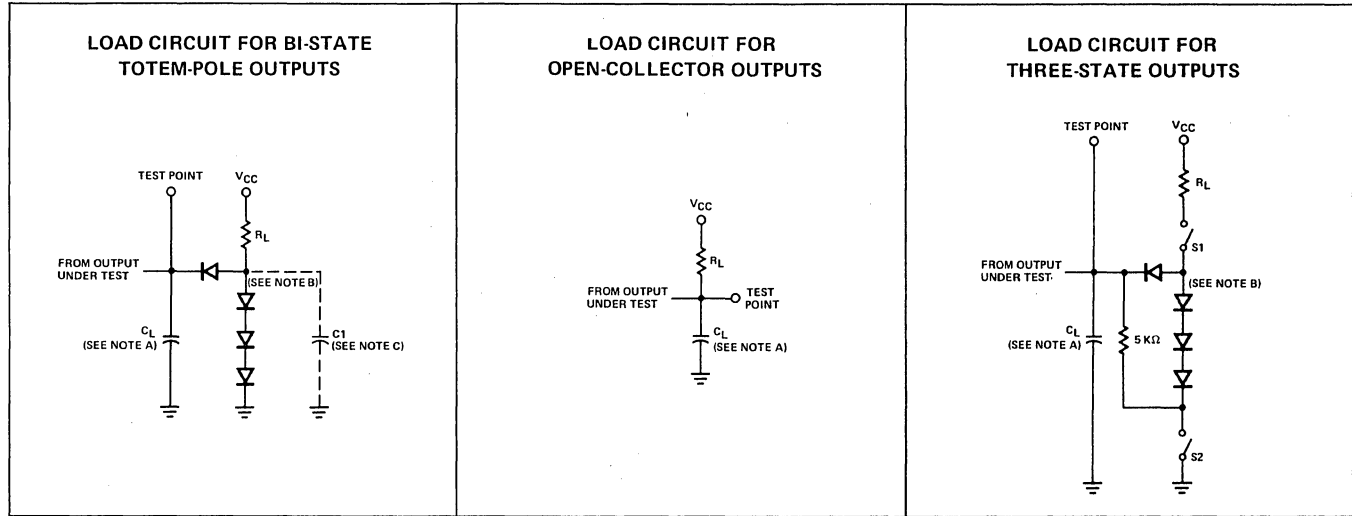
(Over Operating Free-Air Temperature Range Unless Otherwise Noted)

V _{CC}	Supply Voltage ¹	7V
V _{IN}	Input Voltage ¹	5.5V
	Interrmitter Voltage ²	5.5V
T _A	Operating Free-Air Temperature Range	
	Series 54 Circuits	- 55 C to 125 C
	Series 74 Circuits	0 C to 70 C
	Storage Temperature Range	- 65 C to 150 C

NOTES

1. Voltage values, except intermitter voltage, are with respect to network ground terminals.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. Output sink current tests one output at a time.

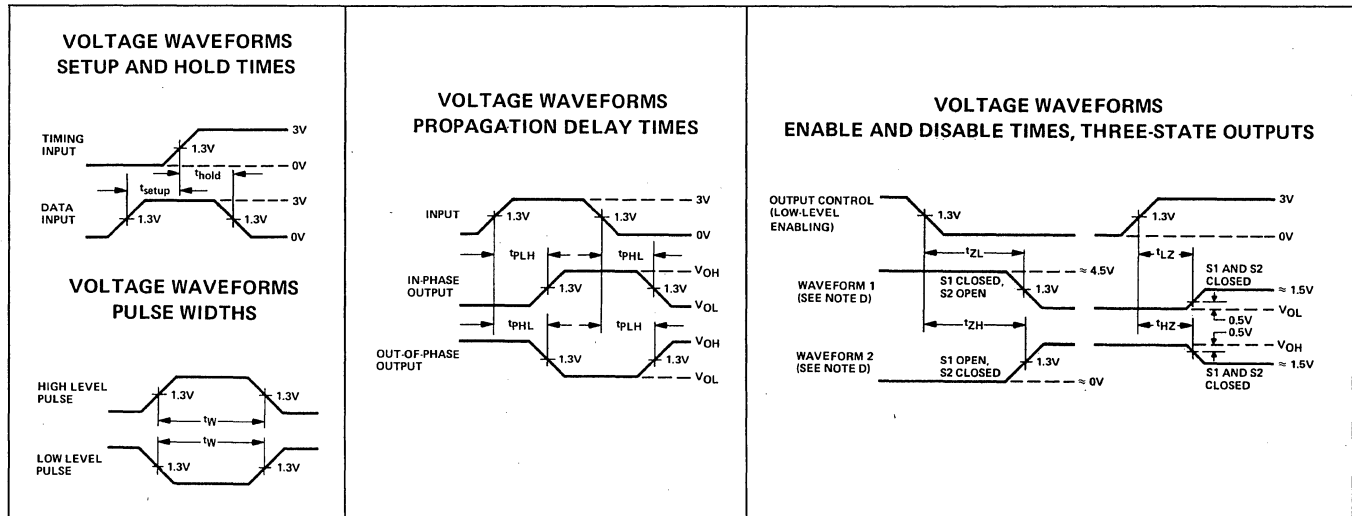
TEST CIRCUITS



NOTES

- A. C_L includes probe and jig capacitance.
- B. All diodes are 1N916 or 1N3064.

WAVEFORMS



NOTES

- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_{out} ≈ 50Ω and t_r ≤ 15 ns, t_f ≤ 6 ns.

PARAMETER	INPUT VOLTAGE (V)						OUTPUT VOLTAGE (V)				INPUT CURRENT (mA)							
	V _{IL} LOW LEVEL		V _{IH} HIGH LEVEL		V _{IC} CLAMP VOLTAGE		V _{OL} LOW LEVEL		V _{OH} HIGH LEVEL		I _{IL} LOW LEVEL			I _{IH} (μ A) HIGH LEVEL				
											V _{CC} =MAX V _{IL} =4.0V			V _{CC} =MAX V _{IH} =2.7V				
TEST CONDITIONS					V _{CC} =MIN I _{IN} =18mA		V _{CC} =MIN V _{IN} =* I _{OL} =4mA@V _{OL} =0.4V I _{OL} =8mA@V _{OL} =0.5V		V _{CC} =MIN V _{IN} =* I _{OH} =-400 μ A									
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74LS00	54 74	54 74	0.7 0.8	2		-1.5	54/74 74	0.4 0.5	2.5 2.7	3.4 3.4					-0.36			20
54/74LS01	54 74		0.7 0.8	2		-1.5	54/74 74	0.4 0.5		N/A					-0.36			20
54/74LS02	54 74		0.7 0.8	2		-1.5	54/74 74	0.4 0.5	2.5 2.7	3.4 3.4					-0.36			20
54/74LS03	54 74		0.7 0.8	2		-1.5	54/74 74	0.4 0.5		N/A					-0.36			20
54/74LS04	54 74		0.7 0.8	2		-1.5	54/74 74	0.4 0.5	2.5 2.7	3.4 3.4					-0.36			20
54/74LS05	54 74		0.7 0.8	2		-1.5	54/74 74	0.4 0.5		N/A					-0.36			20
54/74LS08	54 74		0.7 0.8	2		-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.4 3.4				-0.36			20
54/74LS09	54 74		0.7 0.8	2		-1.5	54/74 74	0.4 0.5		N/A					-0.36			20
54/74LS10	54 74		0.7 0.8	2		-1.5	54/74 74	0.4 0.5	2.5 2.7	3.4 3.4					-0.36			20
54/74LS11	54 74		0.7 0.8	2		-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.4 3.4				-0.36			20
54/74LS12	54 74		0.7 0.8	2		-1.5	54/74 74	0.25 0.35	0.4 0.5						-0.36			20
54/74LS13	54 74	See Data		Sheet		-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.4 3.4				-0.4			20
54/74LS14	54 74	See Data		Sheet		-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.4 3.4				-0.4			20
54/74LS15	54 74		0.7 0.8	2		-1.5	54/74 74	0.4 0.5		N/A					-0.36			20
54/74LS20	54 74		0.7 0.8	2		-1.5	54/74 74	0.4 0.5	2.5 2.7	3.4 3.4					-0.36			20
54/74LS21	54 74		0.7 0.8	2		-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.4 3.4				-0.36			20
54/74LS22	54 74		0.7 0.8	2		-1.5	54/74 74	0.4 0.5		N/A					-0.36			20
54/74LS26	54 74		0.7 0.8	2		-1.5	54/74 74	0.25 0.35	0.4 0.5					-15	-0.36			20
54/74LS27	54 74		0.7 0.8	2		-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.4 3.4				-0.36			20
54/74LS28	54 74		0.7 0.8	2		-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.4 3.4				-0.36			20
54/74LS30	54 74		0.7 0.8	2		-1.5	54/74 74	I _{OL} +12mA I _{OL} =24mA	0.4 0.5	2.5 2.7	3.4 3.4				-0.36			20
54/74LS32	54 74		0.7 0.8	2		-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.4 3.4				-0.36			20
54/74LS33	54 74		0.7 0.8	2		-1.5	54/74 74	0.4 0.5		N/A					-0.36			20
54/74LS37	54 74		0.7 0.8	2		-1.5	54/74 74	I _{OL} =12mA I _{OL} =24mA	0.4 0.5	2.5 2.7	3.4 3.4				-0.36			20
54/74LS38	54 74		0.7 0.8	2		-1.5	54/74 74	0.4 0.5		N/A					-0.36			20
54/74LS39	54 74		0.7 0.8	2		-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.4 3.4				-0.36			20
54/74LS40	54 74		0.7 0.8	2		-1.5	54/74 74	0.4 0.5	2.5 2.7	3.4 3.4					-0.36			20
54/74LS42	54 74		0.7 0.8	2		-1.5	54/74 74	0.25 0.35	0.4 0.5	2.5 2.7	3.5 3.5				-0.4			20

PARAMETER	INPUT CURRENT (mA)			OUTPUT CURRENT (mA)			POWER SUPPLY CURRENT (mA)						OFF-STATE OUTPUT CURRENT (μA)								
	I_{IN}			I_{OS}			I_{CCL}		I_{CCH}		$I_{OH}(\mu A)$		I_{OZL}			I_{OZH}					
	SHORT CIRCUIT			LOW LEVEL			HIGH LEVEL		LEAKAGE		LOW LEVEL VOLTAGE SUPPLIED			HIGH LEVEL VOLTAGE SUPPLIED							
TEST CONDITIONS	$V_{CC} = \text{MAX}$ $V_{IN} = 7.0V$						$V_{CC} = \text{MAX}$ $V_{IH} = 4.5V$ $V_{IL} = 0.5V$ as appropriate						$V_{CC} = \text{MAX}$ $V_{IN} = *$ $V_{OH} = 5.5V$			$V_{CC} = \text{MAX}$ $V_O = 0.4V$			$V_{CC} = \text{MAX}$ $V_O = 2.7V$		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74LS00	54 74	$V_I = 5.5V$		0.1	-15	-100		2.4	4.4		0.8	1.6		N/A			N/A			N/A	
54/74LS01	54 74	$V_I = 5.5V$		0.1	N/A			2.4	4.4		0.8	1.6		100			N/A			N/A	
54/74LS02	54 74	$V_I = 5.5V$		0.1	-15	-100		2.8	5.4		1.6	3.2		N/A			N/A			N/A	
54/74LS03	54 74	$V_I = 5.5V$		0.1	N/A			2.4	4.4		0.8	1.6		100			N/A			N/A	
54/74LS04	54 74	$V_I = 5.5V$		0.1	-15	-100		3.6	6.6		1.2	2.4		N/A			N/A			N/A	
54/74LS05	54 74	$V_I = 5.5V$		0.1	N/A			3.6	6.6		1.2	2.4		100			N/A			N/A	
54/74LS08	54 74	$V_I = 5.5V$		0.1	-15	-100		6.8	8.8		2.4	4.8		N/A			N/A			N/A	
54/74LS09	54 74	$V_I = 5.5V$		0.1	N/A			4.4	8.8		2.4	4.8		100			N/A			N/A	
54/74LS10	54 74	$V_I = 5.5V$		0.1	-15	-100		1.8	3.3		0.6	1.2		N/A			N/A			N/A	
54/74LS11	54 74	$V_I = 5.5V$		0.1	-15	-100		3.3	6.6		1.8	3.6		N/A			N/A			N/A	
54/74LS12	54 74	$V_I = 5.5V$		0.1	N/A			1.8	3.3		0.7	1.4		100			N/A			N/A	
54/74LS13	54 74			0.1	-15	-100		4.1	7		2.9	6		N/A			N/A			N/A	
54/74LS14	54 74			0.1	-15	-100		4.1	7		8.6	16		N/A			N/A			N/A	
54/74LS15	54 74	$V_I = 5.5V$		0.1	N/A			3.3	6.6		1.8	3.6		100			N/A			N/A	
54/74LS20	54 74			0.1	-15	-100		1.2	2.2		0.4	0.8		N/A			N/A			N/A	
54/74LS21	54 74			0.1	-15	-100		2.2	4.4		1.2	2.4		N/A			N/A			N/A	
54/74LS22	54 74			0.1	N/A			1.2	2.2		0.4	0.8		100			N/A			N/A	
54/74LS26	54 74			0.1	-15	-100		2.4	4.4		0.8	1.6					N/A			N/A	
																	$V_{IL} = 0.7V$				
																	$V_{OH} = 12V$	50			
																	$V_{OH} = 15V$	1mA			
54/74LS27	54 74	$V_I = 5.5V$		0.1	-15	-100		3.4	6.8		2.0	4.0		N/A			N/A			N/A	
54/74LS28	54			0.1	-15	-100		6.9	13.8		1.8	3.6		N/A			N/A			N/A	
54/74LS30	54 74			0.1	-15	-100		0.6	1.1	0.35		0.5		N/A			N/A			N/A	
54/74LS32	54 74	$V_I = 5.5V$		0.1	-15	-100		4.9	9.8		3.1	6.2		N/A			N/A			N/A	
54/74LS33	54 74			0.1	N/A			6.9	13.8		1.8	3.6		250			N/A			N/A	
54/74LS37	54 74			0.1	-15	-100		6.0	12.0		0.9	2.0		N/A			N/A			N/A	
54/74LS38	54 74			0.1	N/A			6.0	12.0		0.9	2.0		250			N/A			N/A	
54/74LS39	54 74			0.1	-15	-100		N/A			6.8	11.0		N/A			N/A			N/A	
54/74LS40	54 74			0.1	-15	-100		3	6		0.45	1		N/A			N/A			N/A	
54/74LS42	54 74			1	-15	-100		N/A			7	13		N/A			N/A			N/A	

PARAMETER	INPUT VOLTAGE (V)						OUTPUT VOLTAGE (V)						INPUT CURRENT (mA)					
	V _{IL} LOW LEVEL		V _{IH} HIGH LEVEL		V _{IC} CLAMP VOLTAGE		V _{OL} LOW LEVEL			V _{OH} HIGH LEVEL			I _{IL} LOW LEVEL			I _{IH} (μ A) HIGH LEVEL		
TEST CONDITIONS					V _{CC} =MIN I _{IN} =18mA		V _{CC} =MIN V _{IN} =* I _{OL} =4mA@V _{OL} =0.4V I _{OL} =8mA@V _{OL} =0.5V			V _{CC} =MIN V _{IN} =* I _{OH} =-400 μ A			V _{CC} =MAX V _{IL} =4.V			V _{CC} =MAX V _{IH} =2.7V		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74LS51	54	0.7	2			-1.5	54/74	0.25	0.4	2.5	3.4							20
	74	0.8					74	0.35	0.5	2.7	3.4				-0.36			
54/74LS54	54	0.7	2			-1.5	54/74	0.25	0.4	2.5	3.4							20
	74	0.8					74	0.35	0.5	2.7	3.4				-0.36			
54/74LS55	54	0.7	2			-1.5	54/74	0.25	0.4	2.5	3.4							20
	74	0.8					74	0.35	0.5	2.7	3.4				-0.36			
54/74LS73	54	0.7	2			-1.5	54/74	0.25	0.4	2.5	3.4	J/K Input	-0.36	J/K Input				20
	74	0.8					74	0.35	0.5	2.7	3.4	Clear	-0.8	Clear				60
												Clock	-0.72	Clock				80
54/74LS74	54	0.7	2			-1.5	54/74	0.25	0.4	2.5	3.4	D Input	-0.36	D Input				20
	74	0.8					74	0.35	0.5	2.7	3.4	Clk/Preset	-0.8	Clk/Preset				60
												Clear	-1.15	Clear				60
54/74LS75	54	0.7	2			-1.5	54/74	0.25	0.4	2.5	3.4	D Input	-0.4	D Input				20
	74	0.8					74	0.35	0.5	2.7	3.4	G Input	-1.6	G Input				80
54/74LS76	54	0.7	2			-1.5	54/74	0.25	0.4	2.5	3.4	J/K Input	-0.36	J/K Input				20
	74	0.8					74	0.35	0.5	2.7	3.4	Clock	-0.72	Clock				80
												Preset/Clr	-0.8	Preset/Clr				60
54/74LS78	54	0.7	2			-1.5	54/74	0.25	0.4	2.5	3.4	J/K Input	-0.36	J/K Input				20
	74	0.8					74	0.35	0.5	2.7	3.4	Preset	-0.8	Preset				60
												Clear	-1.6	Clear				120
												Clock	-1.44	Clock				160
54/74LS83	54	0.7	2			-1.5		0.2	0.4	2.4	3.4				-1.6		V _I =5.5V	40
	74	0.8																
54/74LS85	54	0.7	2			-1.5	54/74	0.25	0.4	2.4	3.4	A,B,A,B	-0.4	A,B,A,B				20
	74	0.8					74	0.35	0.5			Others	-1.2	Others				60
54/74LS86	54	0.7	2			-1.5	54/74	0.25	0.4	2.5	3.4							40
	74	0.8					74	0.35	0.5	2.7	3.4				-0.6			
54/74LS90	54	0.7	2			-1.5	54/74	0.25	0.4	2.5	3.4	Any Reset	-0.4	Any Reset				20
	74	0.8					74	0.35	0.5	2.7	3.4	A Input	-2.4	A Input				120
												B Input	-3.2	B Input				40
54/74LS92	54	0.7	2			-1.5	54/74	0.25	0.4	2.5	3.4	Any Reset	-0.4	Any Reset				20
	74	0.8					74	0.35	3.4	2.7	3.4	A Input	-2.4	A Input				120
												B Input	-3.2	B Input				40
54/74LS93	54	0.7	2			-1.5	54/74	0.25	0.4	2.5	3.4	Any Reset	-0.4	Any Reset				20
	74	0.8					74	0.35	0.5	2.7	3.4	A Input	2.4	A Input				120
												B Input	-1.6	B Input				40
54/74LS95B	54	0.7	2			-1.5	54/74	0.25	0.4	2.5	3.5	Clock	-0.8	Clock				40
	74	0.8					74	0.35	0.5	2.7	3.5	Other	-0.4	Other				20
54/74LS96	54	0.7	2			-1.5	54/74	0.25	0.4	2.5	3.5	Preset	-2.0					20
	74	0.8					74	0.35	0.5	2.7	3.5	Enable						
												Others	-0.4					
54/74LS107	54	0.7	2			-1.5	54/74		0.4	2.5	3.4	J/K Input	-0.36	J/K Input				20
	74	0.8					74		0.5	2.7	3.4	Clear	-0.8	Clear				60
												Clock	-0.72	Clock				80
54/74LS109	54	0.7	2			-1.5	54/74		0.4	2.5	3.4	J or K	-0.4	J or K				20
	74	0.8					74		0.5	2.7	3.4	Clk/Preset	-0.8	Clk/Preset				40
												Clear	-1.6	Clear				80
54/74LS112	54	0.7	2			-1.5	54/74		0.4	2.5	3.4	J/K Input	-0.36	J/K Input				20
	74	0.8					74		0.5	2.7	3.4	Clock	-0.72	Clock				80
												Preset/Clr	-0.08	Preset/Clr				60
54/74LS113	54	0.7	2			-1.5	54/74		0.4	2.5	3.4	J/K Input	-0.36	J/K Input				20
	74	0.8					74		0.5	2.7	3.4	Preset	-0.8	Preset				60
												Clock	-0.72	Clock				80
54/74LS114	54	0.7	2			-1.5	54/74		0.4	2.5	3.4	J/K Input	-0.36	J/K Input				20
	74	0.8					74		0.5	2.7	3.4	Preset	-0.8	Preset				60
												Clear	-1.6	Clear				120
												Clock	-1.44	Clock				160
54/74LS132	54	See Data	Sheet			-1.5	54/74	0.25	0.4	V _I =0.6V				-0.4				20

PARAMETER	INPUT CURRENT (mA)			OUTPUT CURRENT (mA)			POWER SUPPLY CURRENT (mA)									OFF-STATE OUTPUT CURRENT (μ A)					
	I_{IN}			I_{OS}			LOW LEVEL			HIGH LEVEL			$I_{OH}(\mu A)$ LEAKAGE			LOW LEVEL VOLTAGE SUPPLIED			HIGH LEVEL VOLTAGE SUPPLIED		
	$V_{CC} = \text{MAX}$ $V_{IN} = 7.0V$			SHORT CIRCUIT			$V_{CC} = \text{MAX}$ $V_{IH} = 4.5V$ $V_{IL} = 0.5V$ as appropriate			$V_{CC} = \text{MAX}$ $V_{IH} = 4.5V$ $V_{IL} = 0.5V$ as appropriate			$V_{CC} = \text{MAX}$ $V_{IN} = *$ $V_{OH} = 5.5V$			$V_{CC} = \text{MAX}$ $V_O = 0.4V$			$V_{CC} = \text{MAX}$ $V_O = 2.7V$		
TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74LS51	54			0.1	-15	-100	1.4	2.8		0.8	1.6				N/A			N/A			N/A
74																					
54/74LS54	54			0.1	-15	-100	1.0	2.0		0.8	1.6				N/A			N/A			N/A
74																					
54/74LS55	54			0.1	-15	-100	0.7	1.3		0.4	0.8				N/A			N/A			N/A
74																					
54/74LS73	54	$V_I = 5.5V$ J/K Input		0.1	-15	-100	N/A			2.0	4.0				N/A			N/A			N/A
74		Clear		0.3						NOTE 2											
		Clock		0.4																	
54/74LS74	54	D Input		0.1	-15	-100	N/A			2.0	4.0				N/A			N/A			N/A
74		Clk Preset		0.2						NOTE 2											
		Clear		0.3																	
54/74LS75	54	D Input		0.1	-15	-100	N/A			6.3	12.0				N/A			N/A			N/A
74		G Input		0.4						NOTE 1											
54/74LS76	54	$V_I = 5.5V$ J/K Input		0.1	-15	-100	N/A			2.0	4.0				N/A			N/A			N/A
74		Clock		0.4						NOTE 2											
		Preset/Clr		0.3																	
54/74LS78	54	$V_I = 5.5V$ J/K Input		0.1	-15	-100	N/A			2.0	4.0				N/A			N/A			N/A
74		Preset		0.3																	
		Clear		0.6																	
		Clock		0.8																	
54/74LS83	54	$V_I = 5.5V$		1	-15	-100	N/A			N/A					N/A			N/A			N/A
74																					
54/74LS85	54	AB, AB		0.1	-15	-100	N/A			10.4	20.0				N/A			N/A			N/A
74		Others		0.3						NOTE 3											
54/74LS86	54			0.2	-15	-100	N/A			6.1	10.0				N/A			N/A			N/A
74										NOTE 1											
54/74LS90	54	$V_I = 7V$ Any Reset		0.1	-15	-100	N/A			9.0	15.0				N/A			N/A			N/A
74		$V_I = 5.5V$ A Input		0.4						NOTE 4											
		B Input		0.8																	
54/74LS92	54	$V_I = 7V$ Any Reset		0.1	-15	-100	N/A			9.0	15.0				N/A			N/A			N/A
74		$V_I = 2.5V$ A Input		0.4						NOTE 4											
		B Input		0.8																	
54/74LS93	54	$V_I = 7V$ Any Reset		0.1	-15	-100	N/A			9.0	15.0				N/A			N/A			N/A
74		$V_I = 5.5V$ A or B Input		0.4						NOTE 4											
54/74LS95B	54	$V_I = 7V$ Clock		0.2	-15	-100	N/A			12.0	20.0				N/A			N/A			N/A
74		Other		0.1						NOTE 6											
54/74LS96	54	$V_I = 7V$		0.1	-15	-100	N/A			12.0	20.0				N/A			N/A			N/A
74										NOTE 6											
54/74LS107	54	J/K Input		0.1	-15	-100	N/A			2.0	4.0				N/A			N/A			N/A
74		Clear		0.3						NOTE 2											
		Clock		0.4																	
54/74LS109	54	J or K		0.1	-15	-100	N/A			2.0	4.0				N/A			N/A			N/A
74		Clk/preset		0.2						NOTE 2											
		Clear		0.4																	
54/74LS112	54	$V_I = 5.5V$ J/K Input		0.1	-15	-100	N/A			2.0	4.0				N/A			N/A			N/A
74										NOTE 2											

PARAMETER	INPUT VOLTAGE (V)			OUTPUT VOLTAGE (V)			INPUT CURRENT (mA)					
	V _{IL} LOW LEVEL	V _{IH} HIGH LEVEL	V _{IC} CLAMP VOLTAGE	V _{OL} LOW LEVEL	V _{OH} HIGH LEVEL	I _{IL} LOW LEVEL	I _{IH} (μ A) HIGH LEVEL					
TEST CONDITIONS	V _{CC} =MIN I _{IN} =18mA			V _{CC} =MIN V _{IN} =* I _{OL} =4mA@V _{OL} =0.4V I _{OL} =8mA@V _{OL} =0.5V	V _{CC} =MIN V _{IN} =* I _{OH} =-400 μ A	V _{CC} =MAX V _{IL} =4.V			V _{CC} =MAX V _{IH} =2.7V			
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
74				74	0.35	0.5		2.5	3.4			
54/74LS136	54	0.7	2	54/74	0.25	0.4		2.7	3.4			40
	74	0.8		74	0.35	0.5		N/A			-0.6	
54/74LS138	54	0.7	2	54/74	0.25	0.4		2.5	3.4			20
	74	0.8		74	0.35	0.5		2.7	3.4		-0.36	
54/74LS145	54	0.7	2	54/74	I _{OL} =12MA	0.4		N/A				20
	74	0.8		74	I _{OL} =24MA	0.5					-0.4	
				74	I _{OL} =80MA	1.7						
54/74LS151	54	0.7	2	54/74	0.25	0.4		2.5	3.4			20
	74	0.8		74	0.35	0.5		2.7	3.4		-0.4	
54/74LS153	54	0.7	2	54/74	0.25	0.4		2.5	3.4			20
	74	0.8		74	0.35	0.5		2.7	3.4		-0.36	
54/74LS157	54	0.7	2	54/74	0.25	0.4		2.5	3.4	S/G Inputs	-0.8	S/G
	74	0.8		74	0.35	0.5		2.7	3.4	A/B Inputs	-0.4	A/B
54/74LS158	54	0.7	2	54/74	0.25	0.4		2.5	3.4	S/G Inputs	-0.8	40
	74	0.8		74	0.35	0.5		2.7	3.4	A/B Inputs	-0.4	20
54/74LS160	54	0.7	2	54/74	0.25	0.4		2.5	3.4	D/EP	-0.4	D/EP
	74	0.8		74	0.35	0.5		2.7	3.4	LD, ET	-0.8	LD,CLK,ET
									CLR	-0.4	CLR	
									CLK	-1.2	20	
54/74LS161	54	0.7	2	54/74	0.25	0.4		2.5	3.4	D/EP	-0.4	D/EP
	74	0.8		74	0.35	0.5		2.7	3.4	LD, ET	-0.8	LD,CLK,ET
									CLR	-0.4	CLR	
									CKT	-1.2	20	
54/74LS162	54	0.7	2	54/74	0.25	0.4		2.5	3.4	D/EP	-0.4	D/EP
	74	0.8		74	0.35	0.5		2.7	3.4	LD, ET	-0.8	LDCLK,ET
									CLR	-0.8	CLR	
									CLK	-1.2	40	
54/74LS163	54	0.7	2	54/74	0.25	0.4		2.5	3.4	D/EP	-0.4	D/EP
	74	0.8		74	0.35	0.5		2.7	3.4	LD, ET	-0.8	LDCLK,ET
									CLR	-0.8	CLR	
									CLK	-1.2	40	
54/74LS164	54	0.7	2	54/74	0.25	0.4		2.5	3.5		-0.4	20
	74	0.8		74	0.35	0.5		2.7	3.5			
54/74LS170	54	0.7	2	54/74	0.25	0.4		N/A		Any D,R,W	-0.4	Any D,R,W
	74	0.8		74	0.35	0.5				G _R or G _W	-0.8	G _R or G _W
54/74LS174	54	0.7	2	54/74	0.25	0.4		2.5	3.5	Clock Input	-0.4	20
	74	0.8		74	0.35	0.5		2.7	3.5	Other Inputs	-0.36	
54/74LS175	54	0.7	2	54/74	0.25	0.4		2.5	3.5	Clock Input	-0.4	20
	74	0.8		74	0.35	0.5		2.7	3.5	Other Inputs	-0.36	
54/74LS181	54	0.7	2	54/74	0.25	0.4		2.5	3.4	Mode Input	-0.36	Mode Input
	74	0.8		74	0.35	0.5		2.7	3.4	A/B Inputs	-1.08	A/B Inputs
									S Inputs	-1.44	S Inputs	
									Carry Input	-2	Carry Input	
54/74LS190	54	0.7	2	54/74	0.25	0.4		2.5	3.4	Enable	-1.08	Enable
	74	0.8		74	0.35	0.5		2.7	3.4	Others	-0.4	Others
54/74LS191	54	0.7	2	54/74	0.25	0.4		2.5	3.4	Enable	-1.08	Enable
	74	0.8		74	0.35	0.5		2.7	3.4	Others	-0.4	Others
54/74LS192	54	0.7	2	54/74	0.25	0.4		2.5	3.4		-0.4	20
	74	0.8		74	0.35	0.5		2.7	3.4			
54/74LS193	54	0.7	2	54/74	0.25	0.4		2.5	3.4		-0.4	20
	74	0.8		74	0.35	0.5		2.7	3.4			
54/74LS194A	54	0.7	2	54/74	0.25	0.4		2.5	3.4		-0.4	20
	74	0.8		74	0.35	0.5		2.7	3.4			
54/74LS195A	54	0.7	2	54/74	0.25	0.4		2.5	3.4	CLK	-0.44	20
	74	0.8		74	0.35	0.5		2.7	3.4	Others	-0.36	

PARAMETER	INPUT CURRENT (mA)			OUTPUT CURRENT (mA)			POWER SUPPLY CURRENT (mA)									OFF-STATE OUTPUT CURRENT (μA)								
	I _{IN}			I _{OS}			I _{CCL}			I _{CCH}			I _{OH} (μA)			I _{OZL}			I _{OZH}					
	SHORT CIRCUIT			LOW LEVEL			HIGH LEVEL			LEAKAGE			LOW VOLTAGE SUPPLIED			HIGH VOLTAGE SUPPLIED								
TEST CONDITIONS	V _{CC} =MAX V _{IN} =7.0V						V _{CC} =MAX V _{IH} =4.5V V _{IL} =0.5V as appropriate									V _{CC} =MAX V _{IN} =* V _{OH} =5.5V			V _{CC} =MAX V _O =0.4V			V _{CC} =MAX V _O =2.7V		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
			0.4																					
			0.3																					
54/74LS113	54	V _I =5.5		-15	-100		N/A		2.0	4.0			N/A			N/A								
	74	J/K Input							NOTE 2															
		Preset																						
		Clock																						
54/74LS114	54	V _I =5.5		-15	-100		N/A		2.0	4.0			N/A			N/A								
	74	J/K Input							NOTE 2															
		Preset																						
		Clear																						
		Clock																						
54/74LS132	54		0.1	-15	-100		8.2	14		5.9	11			N/A			N/A							
	74																							
54/74LS136	54		0.2	-15	-100		N/A			6.1	10.0			N/A			N/A							
	74									NOTE 8														
54/74LS138	54		0.1	-15	-100		N/A			6.3	10.0			N/A			N/A							
	74									NOTE 1														
54/74LS145	54		0.1		N/A		N/A			7.0	13.0				250			N/A						
	74									NOTE 1														
54/74LS151	54		0.1	-15	-100		N/A			6.0	10.0			N/A			N/A							
	74									NOTE 8														
54/74LS153	54		0.1	-15	-100		N/A			6.2	10.0			N/A			N/A							
	74																							
54/74LS157	54	S/G Inputs	0.2	-15	-100		N/A			9.7	16.0			N/A			N/A							
	74	A/B Inputs	0.1							NOTE 8														
54/74LS158	54	S/G Inputs	0.2	-15	-100		N/A			4.8	8.0			N/A			N/A							
	74	A/B Inputs	0.1							NOTE 8														
54/74LS160	54	D/EP	0.1	-15	-100		19	32		18	31			N/A			N/A							
	74	LD,CLK,ET	0.2																					
		CLR	0.1																					
54/74LS161	54	D/EP	0.1	-15	-100		19	32		18	31			N/A			N/A							
	74	LD,CLK,ET	0.2							NOTE 10														
		CLR	0.1																					
54/74LS162	54	D/EP	0.1	-15	-100		19	32		18	31			N/A			N/A							
	74	LD,CLK,ET	0.2							NOTE 10														
		CLR	0.2																					
54/74LS163	54	D/EP	0.1	-15	-100		19	32		18	31			N/A			N/A							
	74	LD,CLK,ET	0.2							NOTE 10														
		CLR	0.2																					
54/74LS164	54		0.1	-15	-100		N/A			16.0	27.0			N/A			N/A							
	74																							
54/74LS170	54	Any D,R,W	0.1		N/A		N/A			26.0	40.0				20			N/A						
	74	G _R or G _w	0.2							NOTE 12														
54/74LS174	54		0.1	-15	-100		N/A			16.0	26.0			N/A			N/A							
	74									NOTE 7														
54/74LS175	54		0.1	-15	-100		N/A			11.0	18.0			N/A			N/A							
	74									NOTE 7														
54/74LS181	54	Mode Input	0.1	-15	-100		N/A		Cond.A	20.0	32.0		A=B Output	100										
	74	A/B Inputs	0.3						Cond.B	21.0	35.0													
		S Inputs	0.4						NOTE 13															
			0.5																					
54/74LS190	54	Enable	0.3	-15	-100		20.0	35.0						N/A			N/A							
	74	Others	0.1				NOTE 1			N/A								N/A						
54/74LS191	54	Enable	0.3	-15	-100		20.0	35.0						N/A			N/A							
	74	Others	0.1				NOTE 1			N/A								N/A						
54/74LS192	54		0.1	-15	-100		20.0	34.0						N/A			N/A							
	74						NOTE 14			N/A								N/A						

PARAMETER	INPUT VOLTAGE (V)			OUTPUT VOLTAGE (V)			INPUT CURRENT (mA)				
	V _{IL} LOW LEVEL	V _{IH} HIGH LEVEL	V _{IC} CLAMP VOLTAGE	V _{OL} LOW LEVEL	V _{OH} HIGH LEVEL	I _{IL} LOW LEVEL	I _{IH} (μ A) HIGH LEVEL				
TEST CONDITIONS	V _{CC} =MIN I _{IN} =18mA			V _{CC} =MIN V _{IN} =* I _{OL} =4mA@V _{OL} =0.4V I _{OL} =8mA@V _{OL} =0.5V			V _{CC} =MAX V _{IL} =4.4V				
	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	MIN TYP MAX			
54/74LS196	54 74	0.7 0.8	2	-1.5	54/74 74	0.4 0.5	2.5 3.4 2.7 3.4	Data, Count/Load Clear Clock 1 Clock 2	-0.36 -0.72 -2.4 -2.8	Data, Count/Load Clear, Clock 1 Clock 2	20 40 80
54/74LS197	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.4 0.35 0.5	2.5 3.4 2.7 3.4	Data, Count/Load Clear Clock 1 Clock 2	-0.36 -0.72 -2.4 -1.3	Data, Count/Load Clear, Clock 1 Clock 2	20 40 40
54/74LS221	See Data Sheet for Electrical Characteristics										
54/74LS251	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.4 0.35 0.5	2.5 3.4 2.7 3.4		-0.4		20
54/74LS253	54 74	0.7 -3 0.8	2	-1.5	54/74 74	0.25 0.4 0.35 0.5	2.4 3.4 2.4 3.4		-0.36		20
54/74LS257	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.4 0.35 0.5	2.4 3.4 2.4 3.4	S Input Others	-0.8 -0.4	S Input Others	40 20
54/74LS258	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.4 0.35 0.5	2.4 3.4 2.4 3.1	S Input Others	-0.8 -0.4	S Input Others	40 20
54/74LS260	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.4 0.35 0.5	2.5 3.4 2.7 3.4		0.36		20
54/74LS261	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.4 0.35 0.5	2.5 3.4 2.7 3.4	M ₀₁ M ₁	-0.8 -0.4	M ₀₁ M ₁	40 20
54/74LS266	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.4 0.35 0.5	N/A		-0.6		40
54/74LS283	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.4 0.35 0.5	2.5 3.6 2.4 5.6	Any A or B CO	-0.8 -0.4	Any A or B CO	40 20
54/74LS290	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.4 0.35 0.5	2.5 3.4 2.7 3.4	Any Reset A Input B Input	-0.4 -2.4 -3.2	Any Reset A Input B Input	20 120 80
54/74LS293	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.4 0.35 0.5	2.5 3.4 2.7 3.4	Any Reset A Input B Input	-0.4 -2.4 -1.6	Any Reset A Input B Input	20 120 40
54/74LS295A	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.4 0.35 0.5	2.4 3.4 2.4 3.1		-0.4		20
54/74LS386	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.4 0.35 0.5	2.5 3.4 3.7 3.4		-0.6		40
54/74LS670	54 74	0.7 0.8	2	-1.5	54/74 74	0.25 0.4 0.35 0.5	2.4 3.4 2.4 3.1	Any D,R,W GW Input GR Input	-0.4 -0.8 -1.2	Any D,R,W CW Input GR Input	20 40 60

PARAMETER	INPUT CURRENT (mA)			OUTPUT CURRENT (mA)			POWER SUPPLY CURRENT (mA)									OFF-STATE OUTPUT CURRENT (μA)								
	I_{IN}			I_{OS} SHORT CIRCUIT			I_{CCL} LOW LEVEL			I_{CCH} HIGH LEVEL			$I_{OH}(\mu A)$ LEAKAGE			I_{OZL} LOW LEVEL VOLTAGE SUPPLIED			I_{OZH} HIGH LEVEL VOLTAGE SUPPLIED					
TEST CONDITIONS	$V_{CC} = \text{MAX}$ $V_{IN} = 7.0V$						$V_{CC} = \text{MAX}$ $V_{IH} = 4.5V$ $V_{IL} = 0.5V$ as appropriate						$V_{CC} = \text{MAX}$ $V_{IN} = *$ $V_{OH} = 5.5V$			$V_{CC} = \text{MAX}$ $V_O = 0.4V$			$V_{CC} = \text{MAX}$ $V_O = 2.7V$					
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
54/74LS193 54 74			0.1	-15	-100		20.0	34.0			N/A		N/A		N/A		N/A		N/A		N/A		N/A	
54/74LS194A 54 74			0.1	-15	-100		15.0	23.0			N/A		N/A		N/A		N/A		N/A		N/A		N/A	
54/74LS195A 54 74	$V_I = 5.5V$		0.1	-15	-100		14.0	21.0			N/A		N/A		N/A		N/A		N/A		N/A		N/A	
54/74LS196 54 74	Data, Count/Load Clear, Clock 1 Clear, Clock 2		0.1 0.2 0.4	-15	-100		16.0	27.0			N/A		N/A		N/A		N/A		N/A		N/A		N/A	
54/74LS197 54 74	$V_I = 5.5V$ Data, Count/Load Clear, Clock 1 Clock 2	0.1 0.2 0.4		-15	-100		16.0	27.0			N/A		N/A		N/A		N/A		N/A		N/A		N/A	
54/74LS251 54 74				0.1	-15	-100	N/A		Cond A 6.1 10.0 Cond B 7.1 12.0			N/A		$V_{CC} = \text{MAX}$		-20		$V_{CC} = \text{MAX}$			20			
54/74LS253 54 74			0.1	-15	-100		N/A		Cond A 7.0 12.0 Cond B 8.5 14.0			N/A		$V_{CC} = \text{MAX}$		-20		$V_{CC} = \text{MAX}$			20			
54/74LS257 54 74	S Input Others	0.2 0.1		-15	-100		N/A		Cond.A 9.2 16.0 Cond.B 5.9 10.0 Cond.C 10.0 17.0			N/A		$V_O = 0.5V$		-50		$V_O = 2.4V$			-50			
54/74LS258 54 74	S Input Others	0.2 0.1		-15	-100		N/A		Cond.A 6.2 11.0 Cond.B 4.1 7.0 Cond.C 7.0 12.0			N/A		$V_O = 0.5V$		-50		$V_O = 2.4V$			-50			
54/74LS260 54 74	$V_I = 5.5V$		0.1	-15	-100		2.6	5.2			1.4	2.7		N/A				N/A			N/A			
54/74LS261 54 74	M_0, M_1 $V = 5.5V$	0.2 0.1		-15	-100		N/A			22.0	38.0		N/A		N/A			N/A			N/A			
54/74LS266 54 74	$V_I = 5.5V$	0.2	N/A				N/A			8.0	13.0			100				N/A			N/A			
54/74LS283 54 74	Any A or B CO	0.2 0.1		-15	-100		N/A		Cond.A 22.0 39.0 Cond.B&C 19.0 34.0			N/A		N/A				N/A			N/A			
54/74LS290 54 74	$V_I = 5.6V$ Any Reset A Input B Input	0.1 0.4 0.8		-15	-100		N/A			29.0	42.0		N/A		N/A			N/A			N/A			
54/74LS293 54 74	$V_I = 7.0$ Any Reset A Input B Input	0.1 0.4 0.4		-15	-100		N/A			26.0	39.0		N/A		N/A			N/A			N/A			
54/74LS295A 54 74			0.1	-15	-100		N/A		Cond.A 14.0 23.0 Cond.B 15.0 25.0			N/A		N/A				N/A			N/A			
54/74LS386 54 74			0.2	-15	-100		N/A			6.1	10.0		N/A		N/A			N/A			N/A			
54/74LS670 54 74	Any D,R,W GW Input GR Input	0.1 0.2 0.3		-15	-100		N/A			30.0	50.0		N/A		$V_{CC} = \text{MAX}$		-20		$V_{CC} = \text{MAX}$		20			

ELECTRICAL CHARACTERISTICS NOTES

1. All inputs grounded, outputs open.
2. With all outputs open, I_{CC} is measured with Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.
3. I_{CC} is measured with outputs open, A=B grounded, and all other inputs at 4.5V.
4. I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5V and all other inputs grounded.
5. I_{CC} is measured with all outputs and serial inputs open; A,B,C and D inputs grounded, mode control at 4.5V and a momentary 3V, then ground, applied to both clock inputs.
6. I_{CC} is measured with clear input grounded and all other inputs and outputs open.
7. I_{CC} is measured with outputs open and 4.5V applied to all data and clear inputs. The measurement is made after a momentary ground, then 4.5V is applied to the clock.
8. I_{CC} is measured with inputs at 4.5V, outputs open.
9. I_{CCL} is measured with clock input high, then again with the clock input low with all other inputs low and all outputs open.
10. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
11. I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4V, and a momentary ground, then 4.5V applied to clear.
12. I_{CC} is measured under the following worst case conditions: 4.5V are applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.
13. With outputs open, I_{CC} is measured for the following conditions:
Condition A — S_0 through S_3 , M and A inputs are at 4.5V, all other inputs grounded.
Condition B — S_0 through S_3 and M are at 4.5V, all other inputs are grounded.
14. I_{CC} is measured with outputs open, clear and load inputs grounded, and all other inputs at 4.5V.
15. With all outputs open, inputs A through D grounded, and 4.5V applied to S_0 , S_1 , clear and the serial inputs, I_{CC} is tested with a momentary ground then 4.5V applied to the clock.
16. With all outputs open, shift/load grounded and 4.5V applied to the J, \bar{K} and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5V to clear, then applying a momentary ground followed by 4.5V to clock.
17. I_{CC} is measured with the outputs open and all data and select inputs at 4.5V under the following conditions:
Condition A — Strobe grounded
Condition B — Strobe grounded
18. I_{CC} is measured with the outputs open and all data and select inputs at 4.5V under the following conditions:
Condition A — All inputs grounded.
Condition B — Output control at 4.5V, all inputs grounded.
19. I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.
20. I_{CC} is measured with one input of each gate at 4.5V, the other inputs grounded, and the outputs open.
21. I_{CC} is measured with the outputs open under the following conditions:
Condition A — All inputs grounded.
Condition B — All B inputs low, other at 4.5V
Condition C — All inputs at 4.5V.
22. I_{CC} is measured with the outputs open, the serial input and mode control at 4.5V, and the data inputs grounded under the following conditions:
Condition A — Output control at 4.5V and a momentary 3v then ground applied to clock input.
Condition B — Output control and clock input grounded.

QUAD 2-INPUT NAND BUFFER

54/74LS37

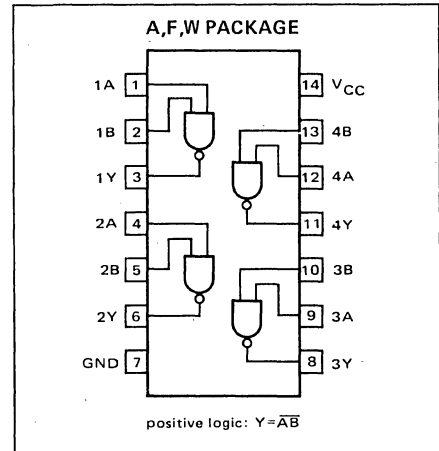
54LS37-F,W • 74LS37-A,F

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 45pF, R_L = 667\Omega$		12	24	ns
t_{PHL} Propagation delay time, high-to-low-level output			12	24	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION



QUAD 2-INPUT NAND BUFFER W/OPEN COLLECTOR OUTPUTS

54/74LS38

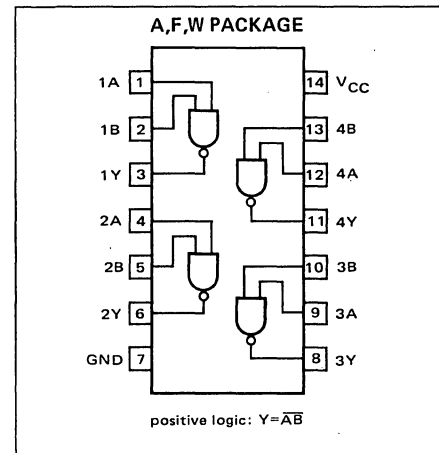
54LS38-F,W • 74LS38-A,F

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 45pF, R_L = 667\Omega$		20	32	ns
t_{PHL} Propagation delay time, high-to-low-level output			18	28	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION



DUAL 4-INPUT NAND BUFFER

54/74LS40

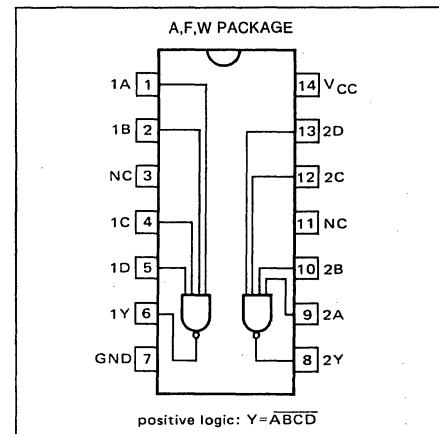
54LS40-F,W • 74LS40-A,F

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

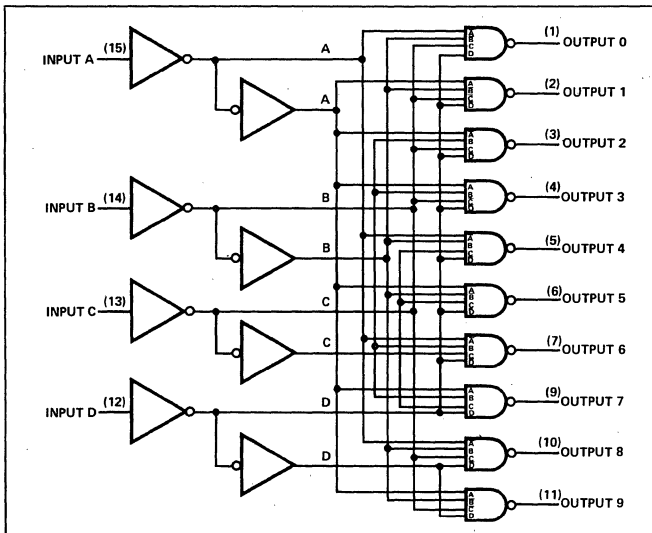
PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 45pF, R_L = 667\Omega$		12	24	ns
t_{PHL} Propagation delay time, high-to-low-level output			12	24	ns

Load circuit and typical waveforms are shown at the front of book.

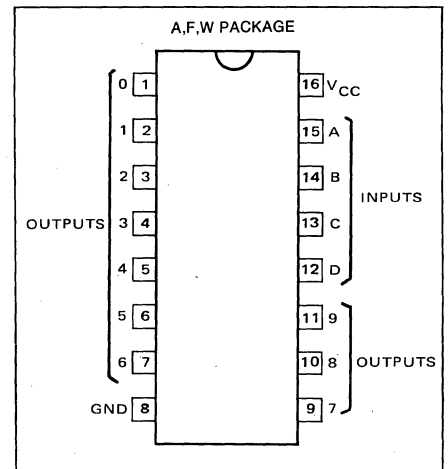
PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



FUNCTION TABLE

NO.	BCD INPUT				DECIMAL OUTPUT										
	D	C	B	A	0	1	2	3	4	5	6	7	8	9	
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

SWITCHING CHARACTERISTICS $V_{CC}=5V, T_A=25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
t_{PHL} Propagation delay time, high-to-low-level output from A,B,C, or D through 2 levels of logic	$C_L = 15pF, R_L = 2k\Omega$		14	25	ns
t_{PHL} Propagation delay time, high-to-low-level output from A,B,C, or D through 3 levels of logic			17	30	ns
t_{PHL} Propagation delay time, low-to-high-level output from A,B,C, and D through 2 levels of logic			10	25	ns
t_{PLH} Propagation delay time, low-to-high-level output from A,B,C, and D through 3 levels of logic			17	30	ns

Load circuit and waveforms shown at front of book (totem pole outputs)

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE

54/74LS51

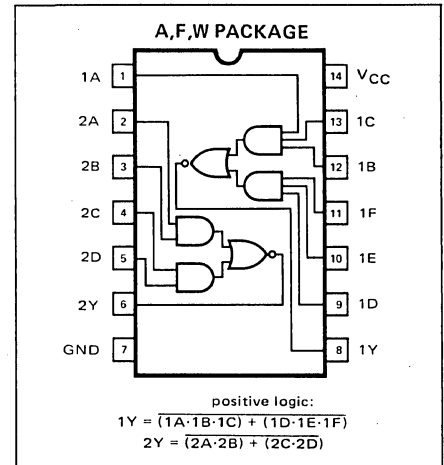
54LS51-F,W • 74LS51-A,F

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15pF, R_L = 2k\Omega$		9	15	ns
t_{PHL} Propagation delay time, high-to-low-level output			9.5	15	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION



4-WIDE 2-INPUT AND-OR-INVERT GATE

54/74LS54

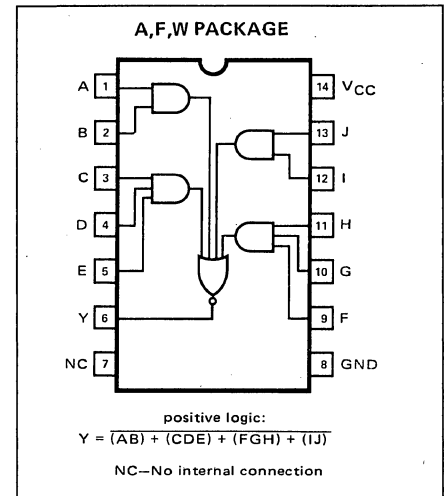
54LS54-F,W • 74LS54-A,F

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15pF, R_L = 2k\Omega$		7.0	20	ns
t_{PHL} Propagation delay time, high-to-low-level output			11.5	20	ns

Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION



2-WIDE 4-INPUT AND-OR-INVERT GATE

54/74LS55

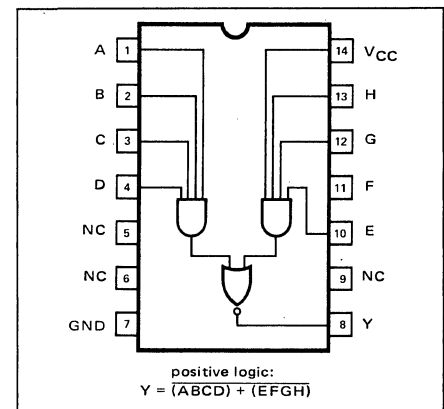
54LS55-F,W • 74LS55-A,F

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15pF, R_L = 2k\Omega$		7.0	20	ns
t_{PHL} Propagation delay time, high-to-low-level output			11.5	20	ns

Load circuit and typical waveforms are shown at the front of book.

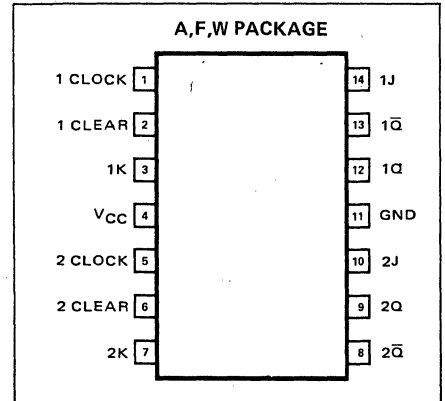
PIN CONFIGURATION



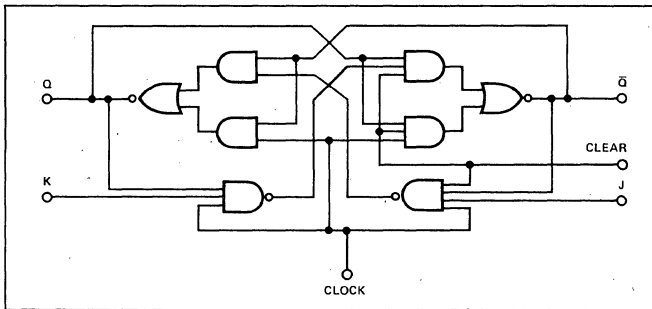
DESCRIPTION

This monolithic edge-triggered dual J-K flip-flop features individual J, K, clock, and clear inputs to each flip-flop. A low logic level at the clear input resets the Q output to a low level regardless of the levels at the other inputs. With clear inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table, as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE (Each Flip-Flop)

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	Q̄
L	X	X	X	L	H
H	↓	L	L	Q ₀	Q̄ ₀
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	TOGGLE
H	H	X	X	Q ₀	Q̄ ₀

H = high level (steady state)
 L = low level (steady state)
 X = irrelevant
 ↓ = transition from high to low level
 Q₀ = the level of Q before the indicated input conditions were established.
 TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

SWITCHING CHARACTERISTICS V_{CC}=5V, T_A=25°C

PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
f _{Clock}	Clock frequency	30	45		MHz
t _{w(Clock)}	Width of clock pulse (high)	20			ns
t _{w(Clear)}	Width of clear pulse (low)	25			ns
t _{Setup}	Input setup time	20			ns
t _{Hold}	Input hold time	0			ns
t _{PLH}	Propagation delay time, low-to-high-level output from clear or clock (as appropriate)		11	20	ns
t _{PHL}	Propagation delay time, high-to-low-level output from clear or clock (as appropriate)		15	30	ns

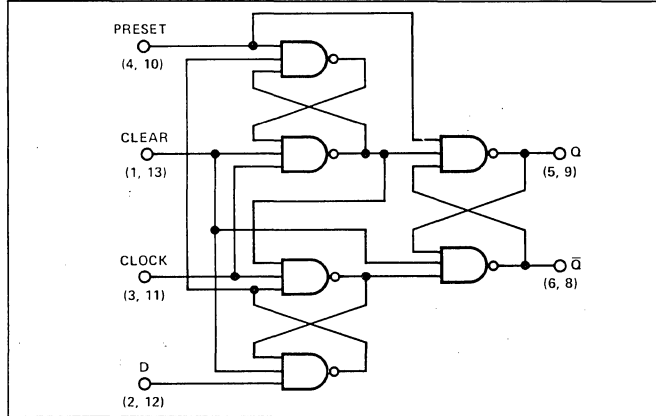
Load circuit and typical waveforms are shown at the front of book.

DESCRIPTION

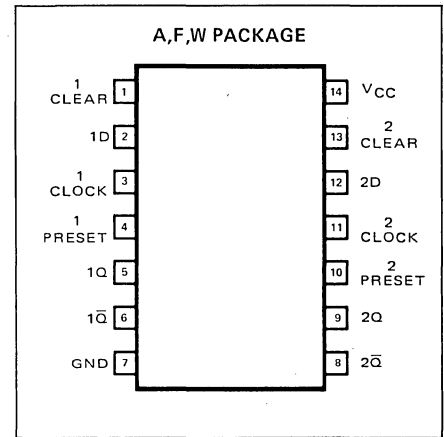
These monolithic dual edge-triggered D-type flip-flops feature individual D, clock, preset, and clear inputs.

Preset and clear inputs are active-low and operate independently of the clock input. When preset and clear are inactive (high), information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect at the output.

FUNCTIONAL BLOCK DIAGRAM (Each Flip-Flop)



PIN CONFIGURATION



FUNCTION TABLE (Each Flip-Flop)

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
H	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	Q̄ ₀

H = high level (steady state) L = low level (steady state)

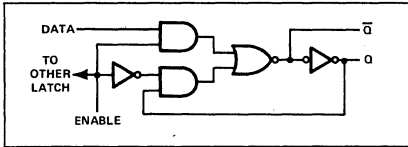
SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS				
		MIN	TYP	MAX	UNIT	
f_{Clock} Clock frequency	$C_L = 15pF, R_L = 2k\Omega$	25	33		ns	
$t_w (Clock)$ Width of clock pulse		25			ns	
$t_w (Preset)$ Width of preset pulse		25			ns	
$t_w (Clear)$ Width of clear pulse		25			ns	
t_{Setup} Input setup time		High level data	25			ns
		Low level data	20			ns
t_{Hold} Input hold time		0			ns	
t_{PLH} Propagation delay time, low-to-high-level output from clear or preset				8	25	ns
t_{PHL} Propagation delay time, high-to-low-level output from clear, preset or clock (whichever is applicable)				16	40	ns

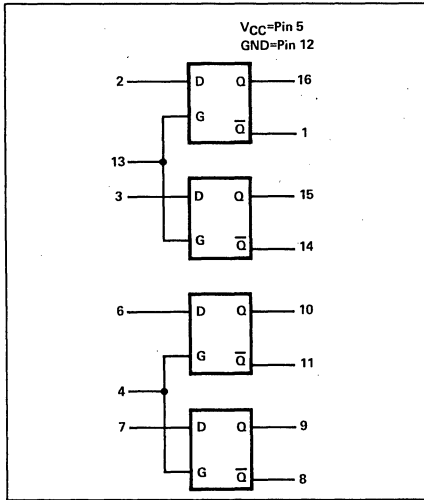
DESCRIPTION

This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

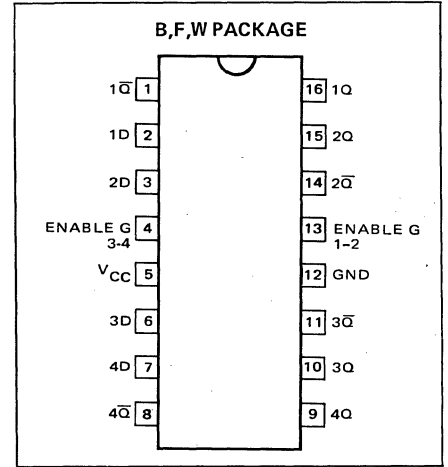
FLIP-FLOP LOGIC DIAGRAM



BLOCK DIAGRAM



PIN CONFIGURATION



SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
t_w				20			ns
t_{Setup}				20			ns
t_{Hold}				0			ns
Propagation delay time			$C_L = 15pF, R_L = 2k\Omega$				ns
t_{PLH}	D	Q			15	27	ns
t_{PHL}	D	\bar{Q}			9	17	ns
t_{PLH}	D	\bar{Q}			12	20	ns
t_{PHL}	D	Q			7	15	ns
t_{PLH}	G	Q			15	27	ns
t_{PHL}	G	\bar{Q}			14	25	ns
t_{PLH}	G	\bar{Q}			16	30	ns
t_{PHL}	G	Q			7	15	ns

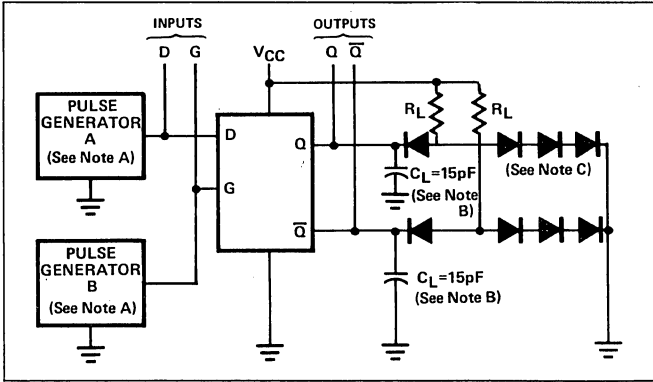
FUNCTION TABLE

(Each Latch)

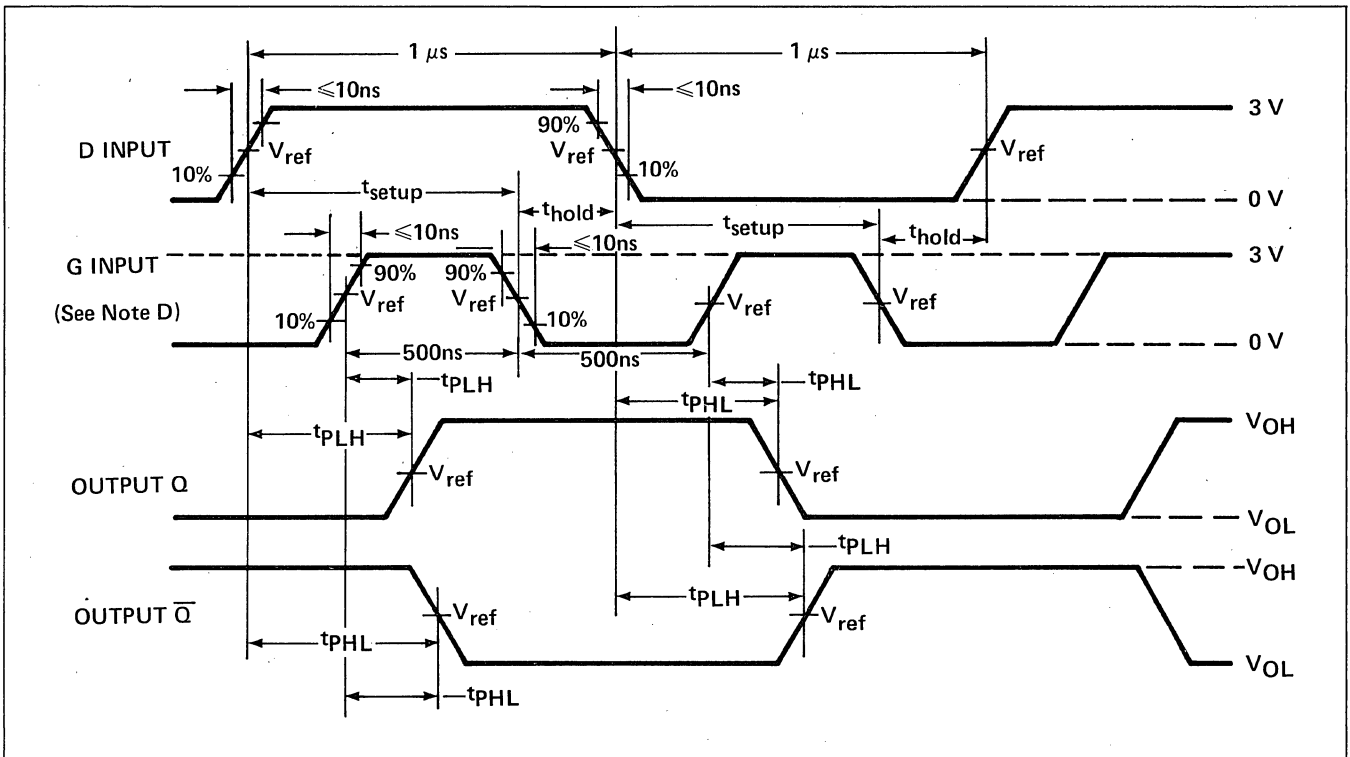
INPUTS		OUTPUTS	
D	G	Q	\bar{Q}
L	H	L	H
H	H	H	L
X	L	Q_0	\bar{Q}_0

H = high level, L = low level, X = irrelevant
 Q_0 = the level of Q before the high-to-low transition of G

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

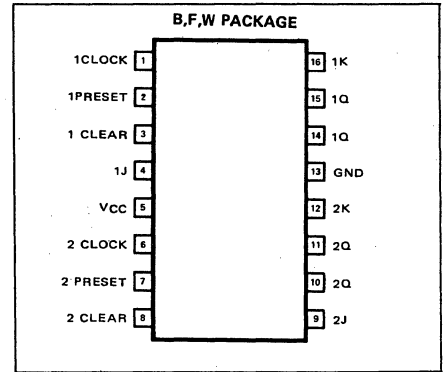
NOTES:

- A. The pulse generators have the following characteristics: $Z_{out} = 50 \Omega$; for pulse generator A, $PRR \leq 500 \text{ kHz}$; for pulse generator B, $PRR \leq 1 \text{ MHz}$. Positions of D and G input pulses are varied with respect to each other to verify setup times.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064.
- D. When measuring propagation delay times from the D input, the corresponding G input must be held high.
- E. $V_{ref} = 1.3V$.

DESCRIPTION

This monolithic dual J-K flip-flop features individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

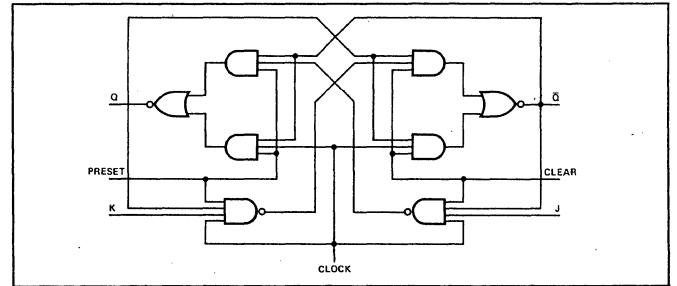
PIN CONFIGURATION



FUNCTION TABLE (Each Flip Flop)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	\bar{H}^*
H	H	↓	L	L	Q ₀	\bar{Q}_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q ₀	\bar{Q}_0

FUNCTIONAL BLOCK DIAGRAM



H = high level (steady state)
 L = low level (steady state)
 X = irrelevant
 ↓ = transition from high to low level
 Q₀ = the level of Q before the indicated steady-state input conditions were established.
 TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.
 *This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

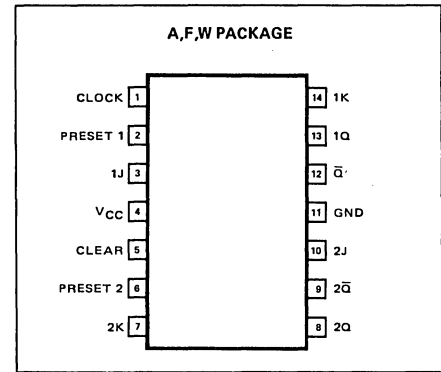
PARAMETER	TEST CONDITIONS	LIMITS				
		MIN	TYP	MAX	UNIT	
f _{Clock} Clock frequency	C _L = 15pF, R _L = 2kΩ	30	45		MHz	
t _{w(Clock)} Width of clock Pulse		20			ns	
t _{w(Preset)} Width of preset pulse		25			ns	
t _{w(Clear)} Width of clear pulse		25			ns	
t _{Setup} Input setup time		20↓			ns	
t _{Hold} Input hold time		0↓			ns	
t _{PLH} Propagation delay time, low-to-high-level output from clear, preset or clock (as appropriate)				11	20	ns
t _{PHL} Propagation delay time, high-to-low-level output from clear, preset or clock (as appropriate)				15	30	ns

54LS78-F,W • 74LS78-A,F

DESCRIPTION

This monolithic dual J-K edge-triggered flip-flop features individual J, K, and preset inputs plus common clock and common clear inputs. The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION



FUNCTION TABLE (Each Flip-Flop)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q ₀	Q̄ ₀
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q ₀	Q̄ ₀

H = high level (steady state)

L = low level (steady state)

X = irrelevant

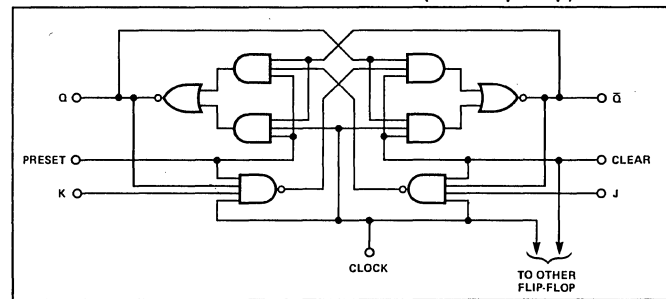
↓ = transition from high to low level

Q₀ = the level of Q before the indicated steady-state input conditions were established

TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

*This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

FUNCTIONAL BLOCK DIAGRAM (Each Flip-Flop)

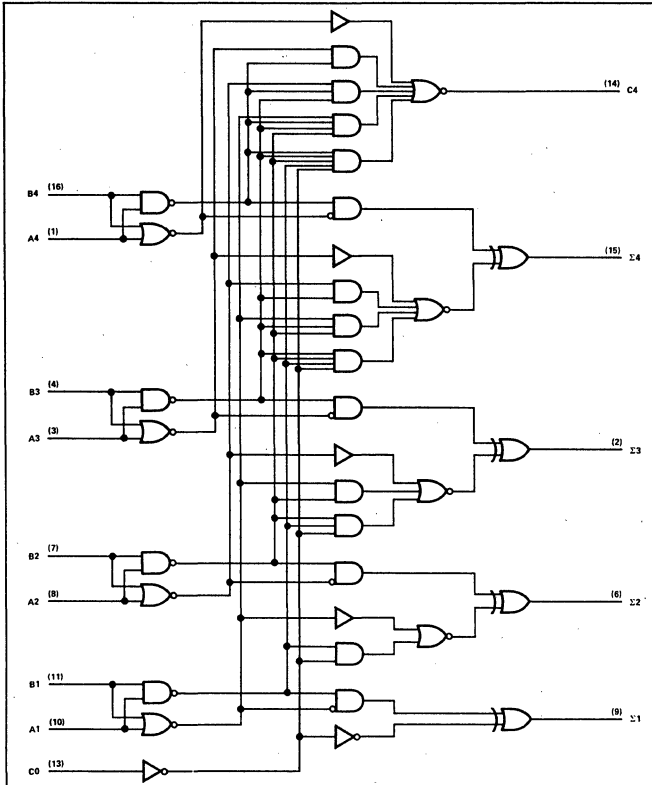


SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

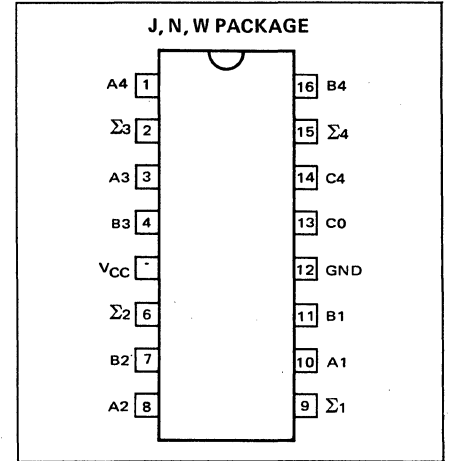
PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
f _{Clock}	Clock frequency	30	45		MHz
t _{w(Clock)}	Width of clock pulse (high)	20			ns
t _{w(Preset)}	Width of preset pulse (low)	25			ns
t _{w(Clear)}	Width of clear pulse (low)	25			ns
t _{Setup}	Input setup time	20↓			ns
t _{Hold}	Input hold time	0↓			ns
t _{PLH}	Propagation delay time, low-to-high-level output from clear, preset or clock (as appropriate)		11	20	ns
t _{PHL}	Propagation delay time, high-to-low-level output from clear, preset or clock (as appropriate)		15	30	ns

Load circuit and waveforms are shown at the front of book.

BLOCK DIAGRAM



PIN CONFIGURATION



FUNCTION TABLE

INPUT				OUTPUT							
				WHEN CO = L				WHEN CO = H			
A1	B2	A2	B2	Σ1	Σ2	C2	Σ1	Σ2	C2		
A3	B3	A4	B4	Σ3	Σ4	C4	Σ3	Σ4	C4		
L	L	L	L	L	L	L	H	L	L		
H	L	L	L	H	L	L	L	H	L		
L	H	L	L	H	L	L	L	H	L		
H	H	L	L	L	H	L	H	H	L		
L	L	H	L	L	H	L	H	H	L		
H	L	H	L	H	H	L	L	L	H		
L	H	H	L	H	H	L	L	L	H		
H	H	H	L	L	L	H	H	L	H		
L	L	L	H	L	H	L	H	H	L		
H	L	L	H	H	H	L	L	L	H		
L	H	L	H	H	H	L	L	L	H		
H	H	L	H	L	L	H	H	L	H		
L	L	H	H	L	L	H	H	L	H		
H	L	H	H	H	L	H	L	H	H		
L	H	H	H	H	L	H	L	H	H		
H	H	H	H	L	H	H	H	H	H		

H = high level, L = low level

NOTE: Input conditions at A1, B1, A, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4, are then used to determine outputs Σ3, Σ4, and C4.

Load circuit and waveforms are shown at the front of book.

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
t_{PLH}	C0	Any Σ	$C_L = 15pF, R_L = 2k\Omega$		16	24	ns
t_{PHL}					15	24	
t_{PLH}	A_i or B_i	Σ_i			15	24	ns
t_{PHL}					15	24	
t_{PLH}	C0	C4			11	17	ns
t_{PHL}					11	17	
t_{PHL}	A_i or B_i	C4			11	17	ns
t_{PHL}					12	17	

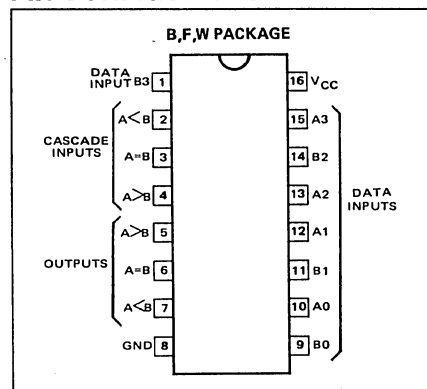
* t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

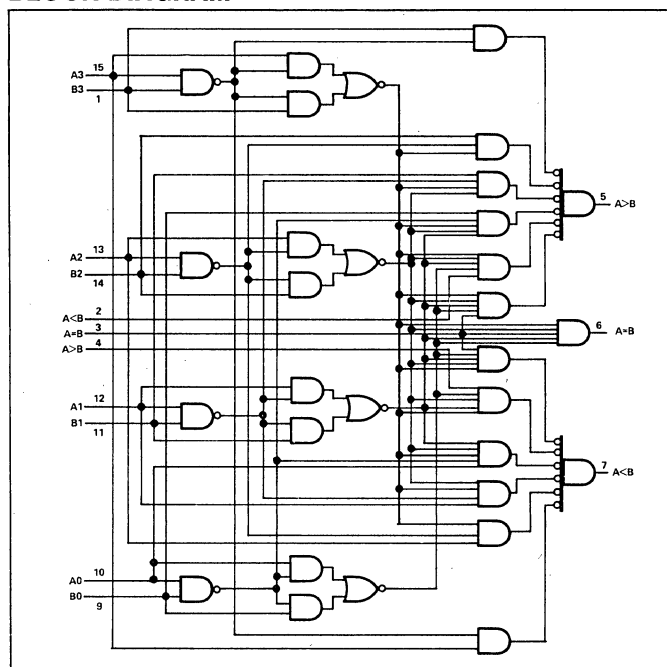
DESCRIPTION

This four-bit magnitude comparator performs comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The $A > B$, $A < B$ and $A = B$ outputs of a stage handling less-significant bits are connected to the corresponding $A > B$, $A < B$, and $A = B$ inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the $A = B$ input. The cascading path is implemented with only a two-gate-level delay to reduce overall comparison times for long words. An alternate method of cascading which further reduces the comparison time is shown in the typical application data.

PIN CONFIGURATION



BLOCK DIAGRAM



FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

H = high level, L = low level, X = irrelevant

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER*	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	LIMITS				
					MIN	TYP	MAX	UNIT	
t_{PLH}	Any A or B data input	A < B, A > B	1	$C_L = 15pF, R_L = 2k\Omega$			14		ns
			2				19		
		3	24				36		
		4	23				40		
t_{PHL}	Any A or B data input	A < B, A > B	1				11		
			2				15		
		3	20				30		
		4	20				30		
t_{PLH}	A < B or A = B	A > B	1	14	22	ns			
t_{PHL}	A < B or A = B	A > B	1	11	17	ns			
t_{PLH}	A = B	A = B	2	13	20	ns			
t_{PHL}	A = B	A = B	2	11	17	ns			
t_{PLH}	A > B or A = B	A < B	1	14	22	ns			
t_{PHL}	A > B or A = B	A < B	1	11	17	ns			

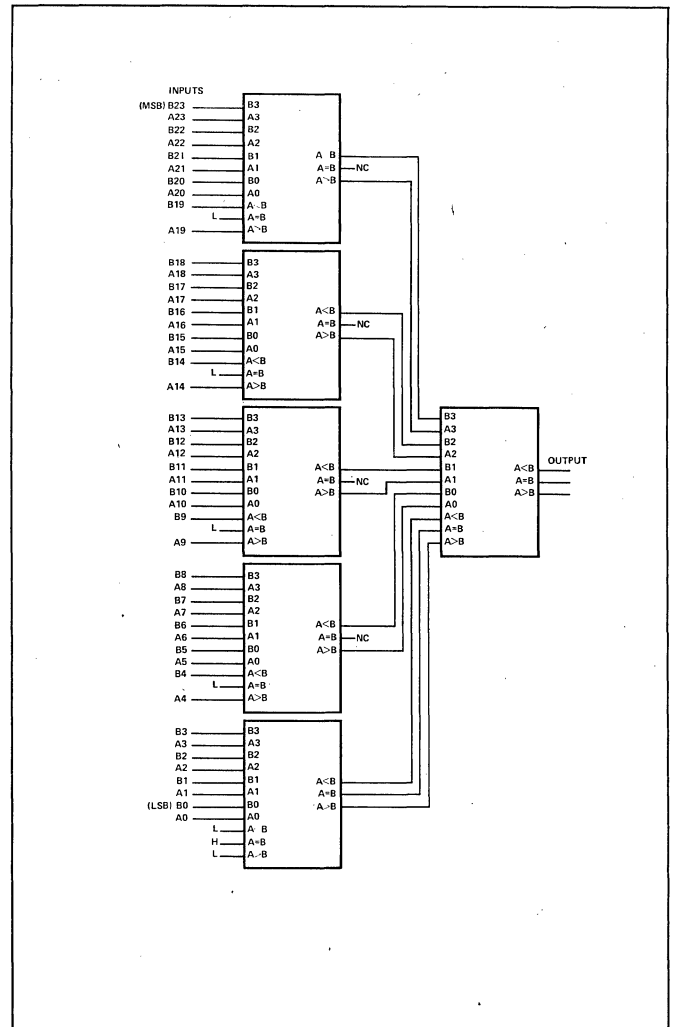
* t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output
 Load circuit and waveforms are shown at the front of the book.

TYPICAL APPLICATION DATA

COMPARISON OF TWO N-BIT WORDS

This application demonstrates how these magnitude comparators can be cascaded to compare longer words. The example illustrated shows the comparison of two 24-bit words; however, the design is expandable to n-bits. As an example, one comparator can be used with five of the 24-bit comparators illustrated to expand the word length to 120-bits. Typical comparison times for various word lengths using the 54/74LS85 are:

WORD LENGTH	NUMBER OF PKGS	
1-4 bits	1	24 ns
5-24 bits	2-6	48 ns
25-120 bits	8-31	72 ns



QUAD 2-INPUT EXCLUSIVE-OR GATE

54/74LS86

54LS86-F,W • 74LS86-A,F

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER*	FROM (INPUT)	TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low		12	23	ns
t_{PHL}	A or B	Other input high		10	17	
t_{PLH}	A or B	Other input high	$C_L = 15pF,$ $R_L = 2k\Omega$	10	30	ns
t_{PHL}	A or B			18	22	

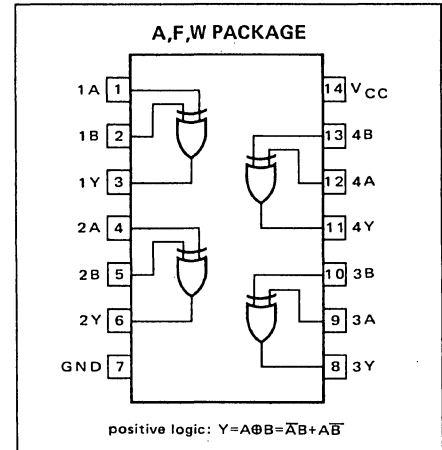
FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

* t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output
 Load circuit and voltage waveforms are shown at front of book

PIN CONFIGURATION



DECADE COUNTER

54/74LS90

54LS90-F,W • 74LS90-A,F

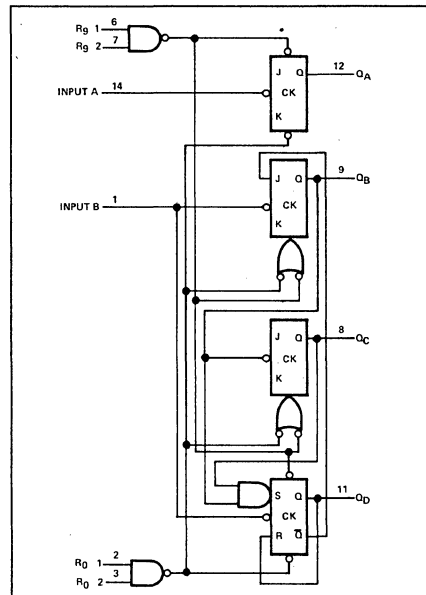
DESCRIPTION

This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

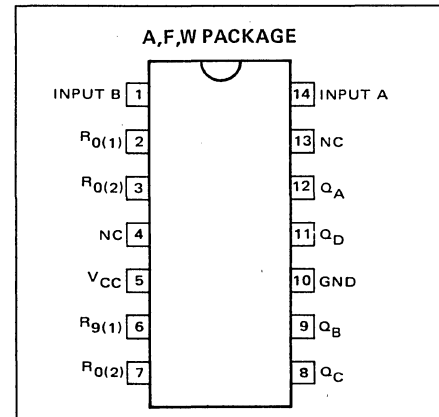
The 54/74LS90 also has a gated zero reset and gated set-to-nine inputs for use in BCD nine's complement applications.

To use its maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table. A symmetrical divide-by-ten count can be obtained by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A .

BLOCK DIAGRAM



PIN CONFIGURATION



BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
R ₀₍₁₎	R ₀₍₂₎	R ₉₍₁₎	R ₉₍₂₎	Q _D	Q _C	Q _B	Q _A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

NOTES:

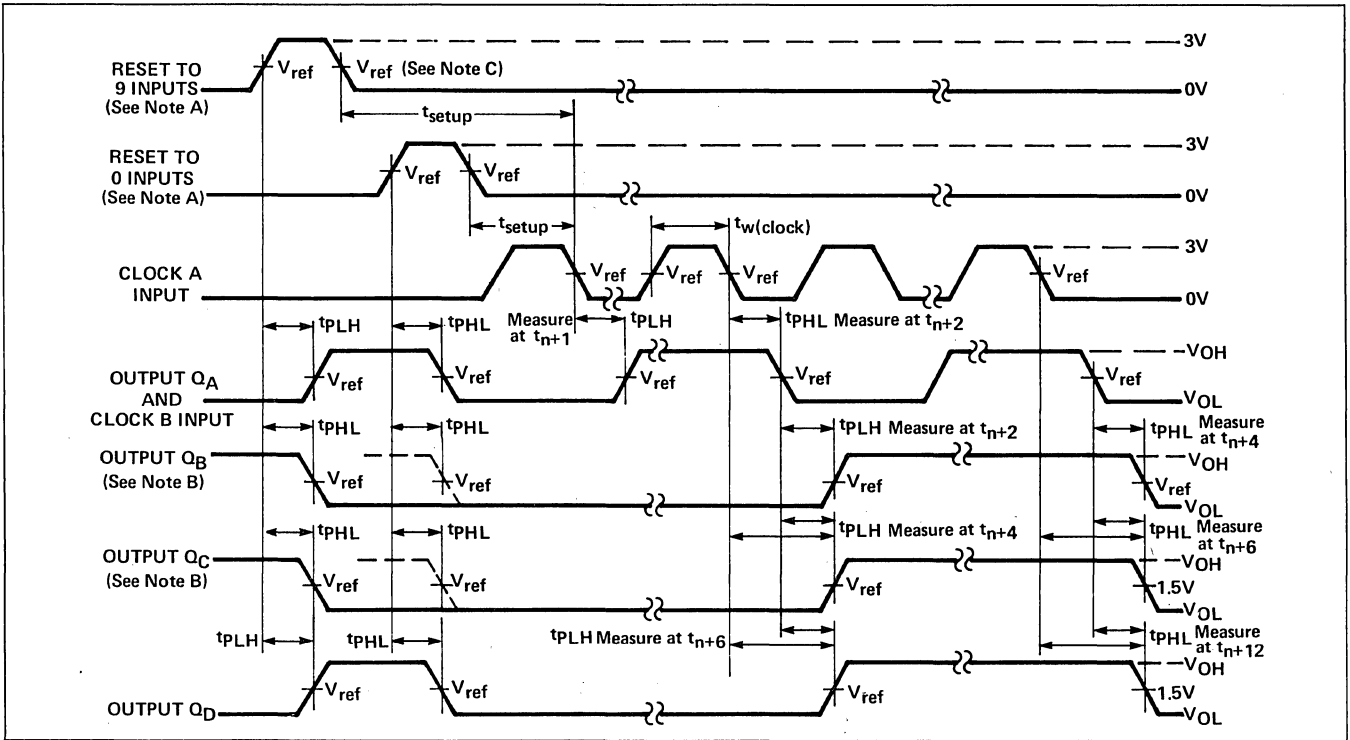
- A. Output Q_A is connected to input B for BCD count.
- B. Output Q_D is connected to input A for bi-quinary count.
- C. Output Q_A is connected to input B.
- D. H = high level, L = low level, X = irrelevant

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
f _{Count}	A	Q _A	C _L = 15pF, R _L = 2kΩ See Figure 1	32	42		MHz
	B	Q _B		16			
t _w Pulse width	A	Q		15			ns
	B	Q		30			ns
	Reset	Q		15			ns
t _{Setup}	Reset inactive-state setup time			25			ns
t _{PLH}	A	Q _A		10	16		ns
t _{PHL}	A	Q _A		12	18		ns
t _{PLH}	A	Q _D		32	48		ns
t _{PHL}	A	Q _D		34	50		ns
t _{PLH}	B	Q _B		10	16		ns
t _{PHL}	B	Q _B		14	21		ns
t _{PLH}	B	Q _C		21	32		ns
t _{PHL}	B	Q _C		23	35		ns
t _{PLH}	B	Q _D		21	32		ns
t _{PHL}	B	Q _D		23	35		ns
t _{PHL}	Set-to-0	Any	26	40		ns	
t _{PLH}	Set-to-9	Q _A , Q _D	20	30		ns	
t _{PHL}		Q _B , Q _C	26	40		ns	

*f_{max} = maximum count frequency
 t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

- A. Each reset input is tested separately with the other reset at 4.5 V.
 - B. Reference waveforms are shown with dashed lines.
 - C. $V_{ref} = 1.3$ V.
- Load circuit is shown at front of book (for totem pole outputs).

DIVIDE-BY-TWELVE COUNTER

54/74LS92

54LS92-F,W • 74LS92-A,F

DESCRIPTION

This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three stage binary counter for which the count cycle length is divide-by-six.

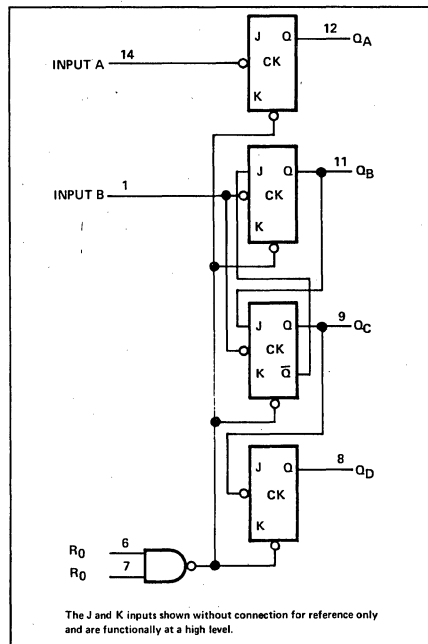
To use its maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table.

COUNT SEQUENCE

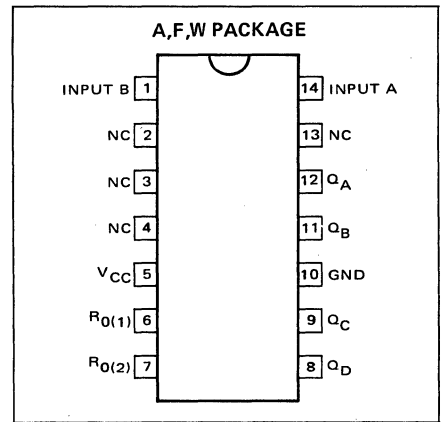
COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

Output Q_A is connected to Input B.

BLOCK DIAGRAM



PIN CONFIGURATION



RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
R ₀ (1)	R ₀ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

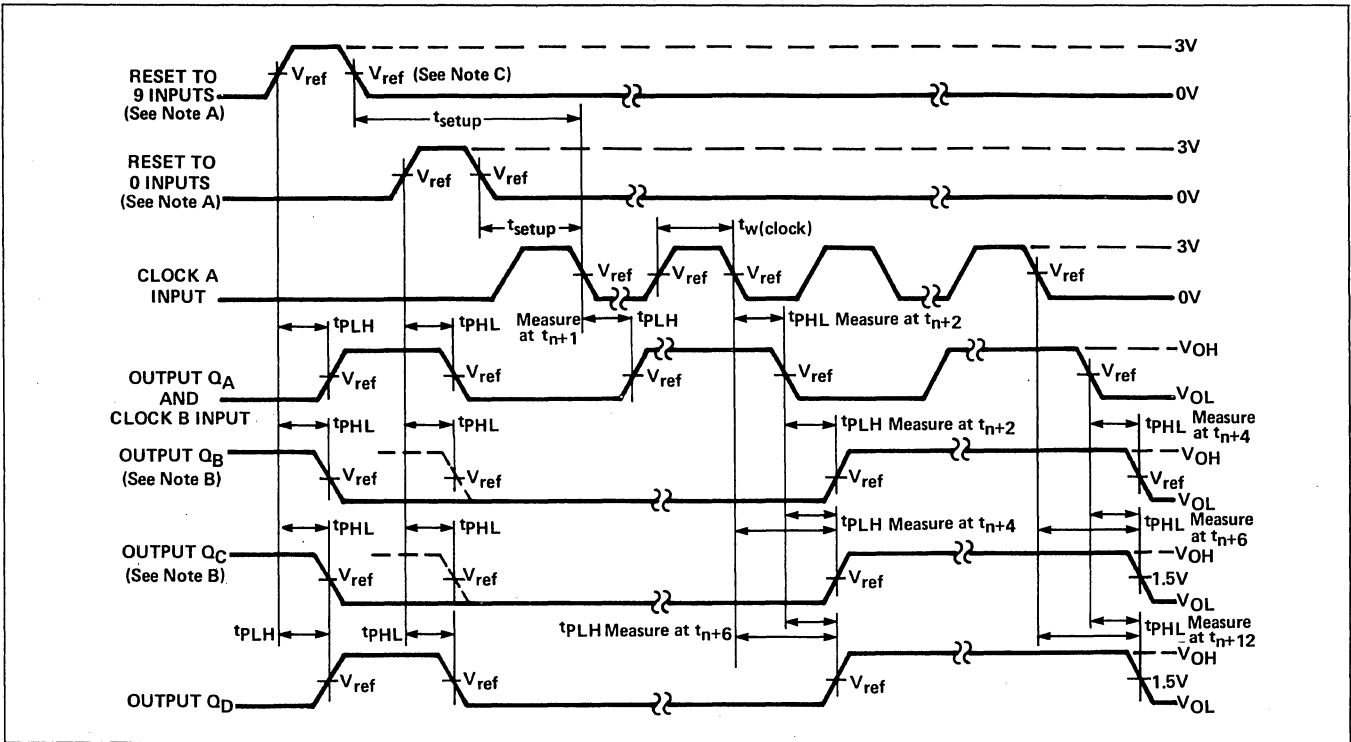
PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
t _{Count}	A	Q _A		32	42		MHz
	B	Q _B		16			
t _w Pulse width	A	Q		15			ns
	B	Q		30			ns
	Reset	Q		15			ns
t _{Setup}	Reset inactive-state setup time			25			ns
t _{PLH}	A	Q _A	C _L = 15pF, R _L = 2kΩ See Figure 1		10	16	ns
t _{PHL}					12	18	
t _{PLH}	A	Q _D			32	48	ns
t _{PHL}					34	50	
t _{PLH}	B	Q _B			10	16	ns
t _{PHL}					14	21	
t _{PLH}	B	Q _C			10	16	ns
t _{PHL}					14	21	
t _{PLH}	B	Q _D			21	32	ns
t _{PHL}					23	35	
t _{PHL}	Set-to-0	Any		26	40	ns	
t _{PLH}	Set-to-9	Q _A , Q _D				ns	
t _{PHL}			Q _B , Q _C				

*t_{max} = maximum count frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

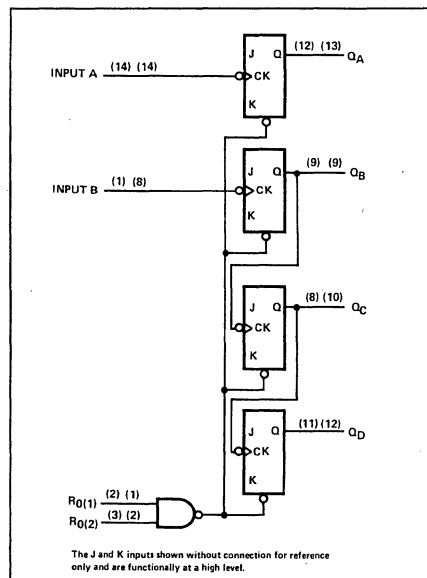
- NOTES:
 A. Each reset input is tested separately with the other reset at 4.5 V.
 B. Reference waveforms are shown with dashed lines.
 C. $V_{ref} = 1.3$ V.
 Load circuit is shown at front of book (for totem pole outputs).

DESCRIPTION

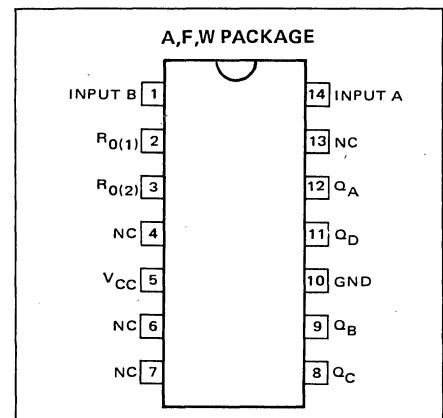
This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three stage binary counter for which the count cycle length is divide-by-eight.

To use its maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table.

BLOCK DIAGRAM



PIN CONFIGURATION



SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

COUNT SEQUENCE

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
t_{Count}	A	Q _A	$C_L = 15pF, R_L = 2k\Omega$ See Figure 1	32	42		MHZ
	B	Q _B		16			
t_w Pulse width	A	Q		15			ns
	B	Q		30			ns
	Reset	Q		15			ns
t_{Setup}	Reset inactive-state-setup time			25			ns
t_{PLH}	A	Q _A			10	16	ns
t_{PHL}					12	18	
t_{PLH}	A	Q _D			46	70	ns
t_{PHL}					46	70	
t_{PLH}	B	Q _B			10	16	ns
t_{PHL}					14	21	
t_{PLH}	B	Q _C			21	32	ns
t_{PHL}					23	35	
t_{PLH}					34	51	ns
t_{PHL}	B	Q _D			34	51	
t_{PHL}	Set-to-0	Any		26	40	ns	

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

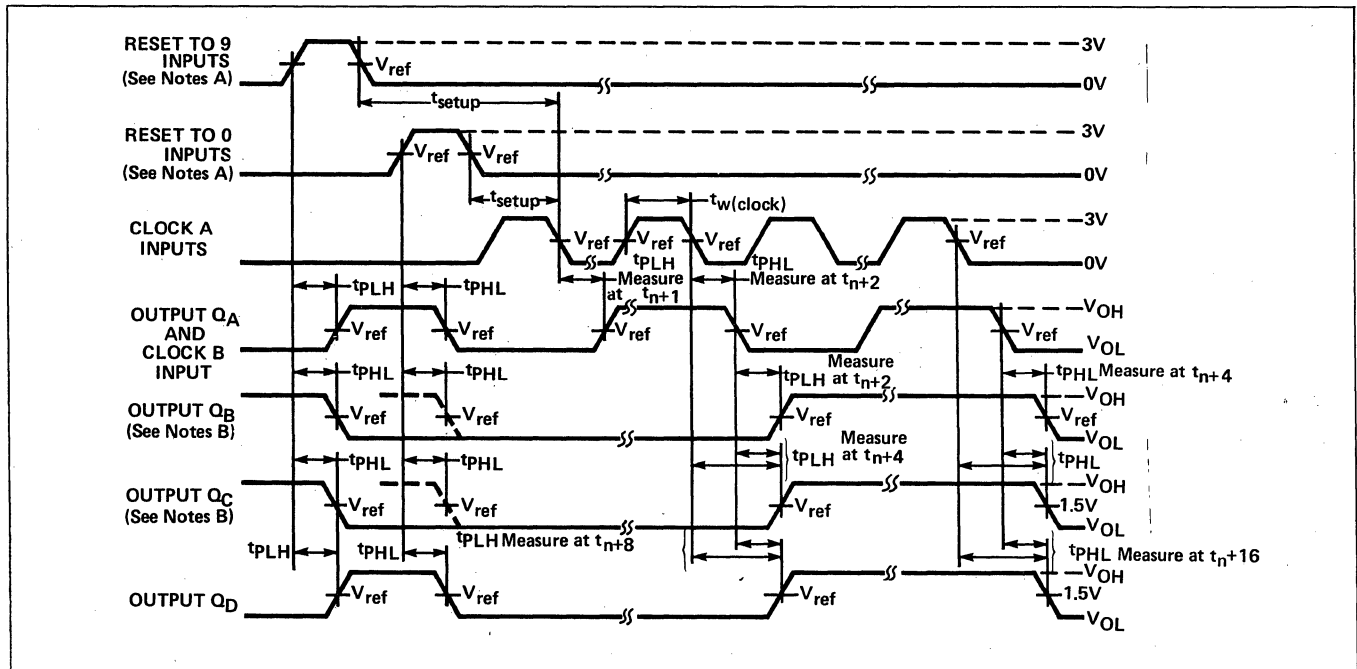
Output Q_A Is Connected To Input B.

RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
R ₀ (1)	R ₀ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X				COUNT
X	L				COUNT

* t_{max} = maximum count frequency
 t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:
 A. Each reset input is tested separately with the other reset at 4.5 V.
 B. Reference waveforms are shown with dashed lines.
 C. $V_{ref} = 1.8 V$.
 Load circuit shown at front of book (for totem pole outputs).

DESCRIPTION

This 4-bit register features parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The register has three modes of operation:

- Parallel (broadside) load
- Shift right (the direction Q_A toward Q_D)
- Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

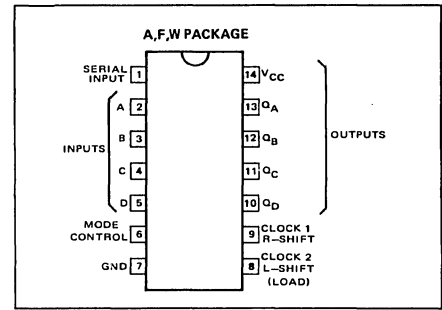
Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

FUNCTION TABLE

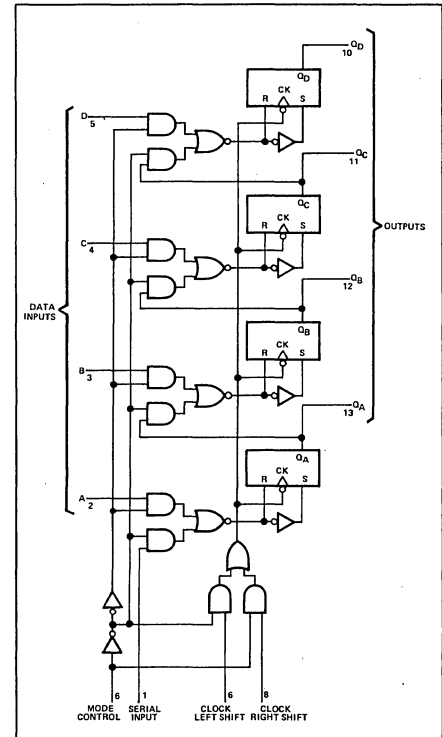
MODE CONTROL	INPUTS			OUTPUTS							
	CLOCKS		SERIAL	PARALLEL				Q_A	Q_B	Q_C	Q_D
	2(L)	1(R)		A	B	C	D				
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_{B^*}	Q_{C^*}	Q_{D^*}	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

*Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.
 H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
 ↓ = transition from high to low level, ↑ = transition from low to high level
 a, b, c, d = the level of steady-state input at Inputs A, B, C, or D, respectively.
 $Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}$ = the level of $Q_A, Q_B, Q_C,$ or $Q_D,$ respectively, before the indicated steady state input conditions were established.
 $Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}$ = the level of $Q_A, Q_B, Q_C,$ or $Q_D,$ respectively, before the most-recent ↓ transition of the clock.

PIN CONFIGURATION



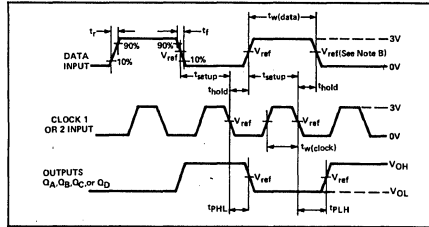
FUNCTIONAL BLOCK DIAGRAM



SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
$f_{(Clock)}$ Clock frequency	$C_L = 15pF, R_L = 2k\Omega$	25	36		MHz
$t_{w(Clock)}$ Width of clock pulse	See Figure 1	25			ns
t_{Setup} Input setup time, high level or low level data	See Figure 1	20↓			ns
t_{Hold} Input hold time, high level or low level data	See Figure 1	10↓			ns
$t_{Enable 1}$ Time to enable clock 1	See Figure 2	20↓			ns
$t_{Enable 2}$ Time to enable clock 2	See Figure 2	20↓			ns
$t_{Inhibit 1}$ Time to inhibit clock 1	See Figure 2	20↓			ns
$t_{Inhibit 2}$ Time to inhibit clock 2	See Figure 2	20↓			ns
t_{PLH} Propagation delay time, low-to-high-level output from clock	See Figure 1		18	27	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock	See Figure 1		21	32	ns

PARAMETER MEASUREMENT INFORMATION

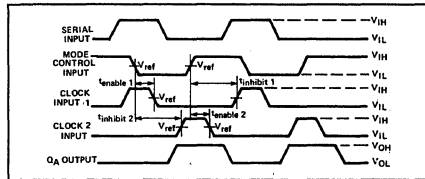


NOTES:

- A. When testing f_{Clock} vary PRR. $t_{w(Data)} \geq 20$ ns.
- $t_{w(Clock)} \geq 15$ ns.
- B. $V_{ref} = 1.3V$

Load circuit shown at front of book (totem pole outputs).

VOLTAGE WAVEFORMS
FIGURE 1—SWITCHING TIMES



NOTES:

- A. Input A is at a low level.
- B. $V_{ref} = 1.3V$.

VOLTAGE WAVEFORMS
**FIGURE 2—CLOCK ENABLE/
INHIBIT TIMES**

DESCRIPTION

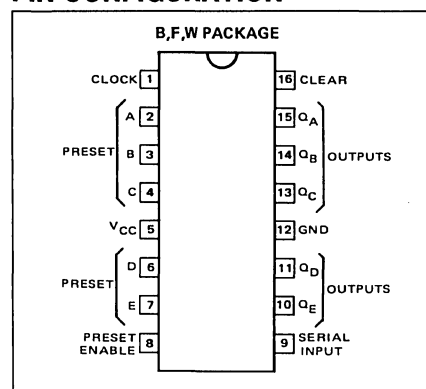
This shift register consists of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is inactive (low). Clearing is independent of the level of the clock input.

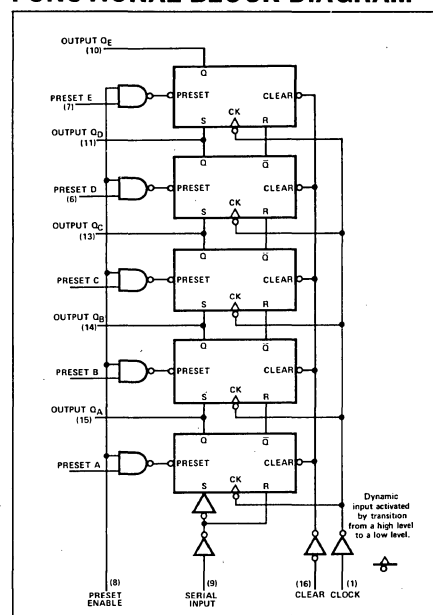
The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting like clearing is independent of the level of the clock input.

Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

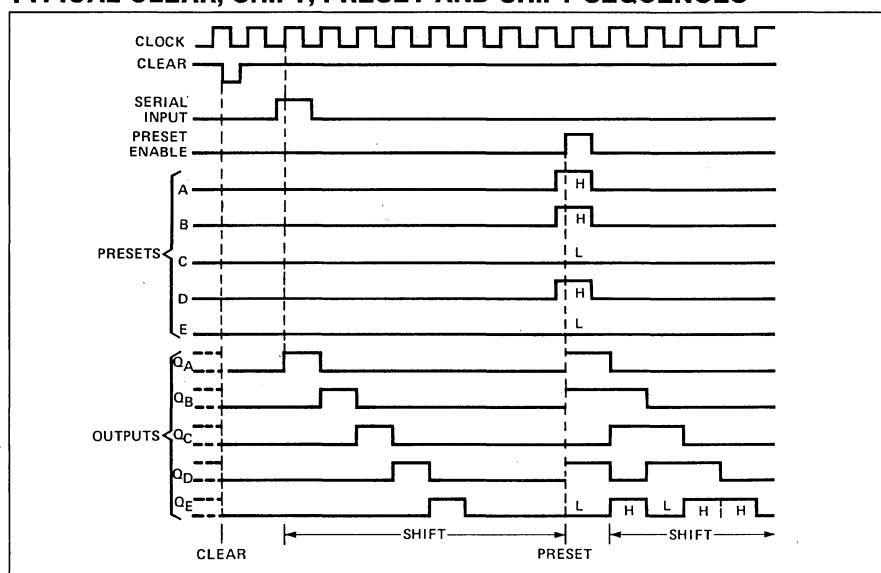
PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



TYPICAL CLEAR, SHIFT, PRESET AND SHIFT SEQUENCES



FUNCTION TABLE

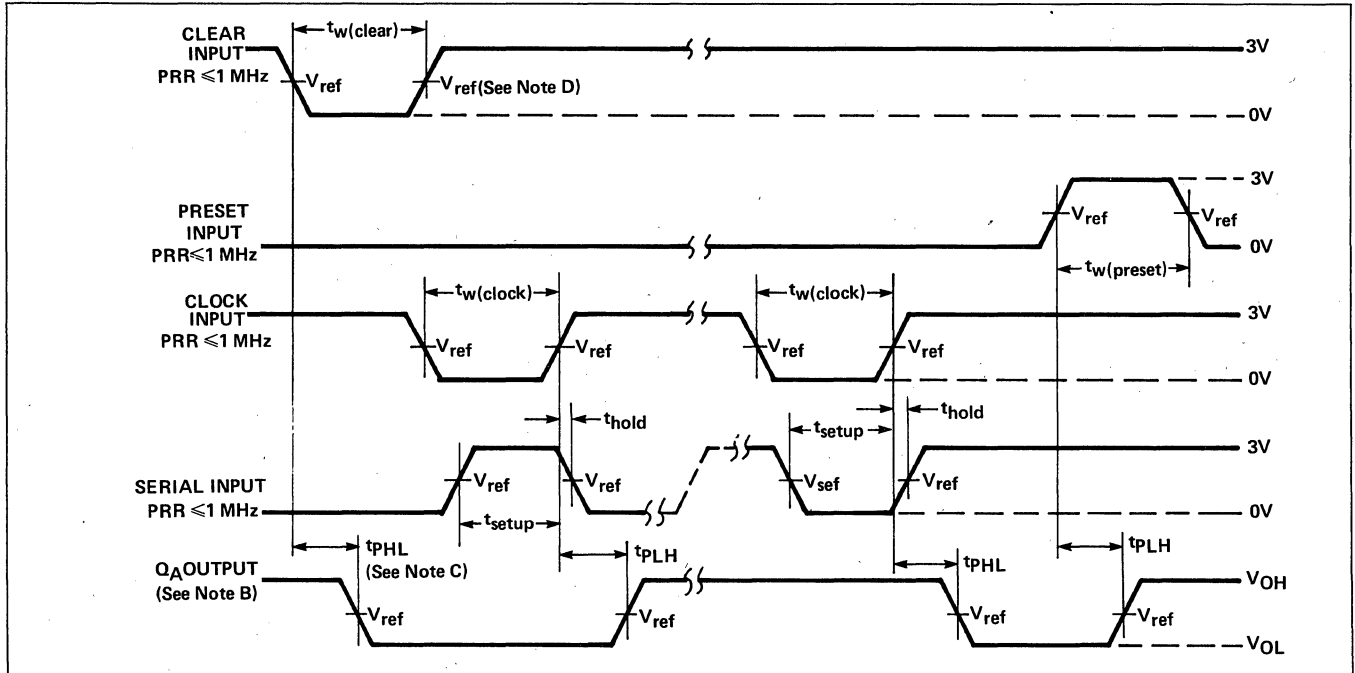
INPUTS		PRESET					CLOCK	SERIAL	OUTPUTS				
CLEAR	PRESET ENABLE	A	B	C	D	E			QA	QB	QC	QD	QE
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	QA0	QB0	QC0	QD0	QE0
H	H	H	L	H	L	H	L	X	H	QB0	H	QD0	H
H	L	X	X	X	X	X	L	X	QA0	QB0	QC0	QD0	QE0
H	L	X	X	X	X	X	↑	H	H	QAn	QBn	QCn	QDn
H	L	X	X	X	X	X	↑	L	L	QAn	QBn	QCn	QDn

H = high level (steady state), L = low level (steady state)
 X = irrelevant (any input, including transitions)
 † = transition from low to high level
 QA0, QB0, etc = the level of QA, QB, etc, respectively before the indicated steady-state input conditions were established.
 QAn, QBn, etc = the level of QA, QB, etc, respectively before the most recent † transition of the clock.

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
f_{Clock} Clock frequency		10			MHz
$t_{w(Clock)}$ Width of clock input pulse		35			ns
t_w Width of preset and clear input pulse		30			ns
t_{Setup} Serial input setup time		30 \uparrow			ns
t_{Hold} Serial input hold time	$C_L = 15pF, R_L = 2k\Omega$	0 \uparrow			ns
t_{PLH} Propagation delay time, low-to-high-level output from clock	See Figure 1		25	40	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			25	40	ns
t_{PLH} Propagation delay time, low-to-high-level output from preset or preset enable			28	35	ns
t_{PHL} Propagation delay time, high-to-low-level output from clear				55	ns

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

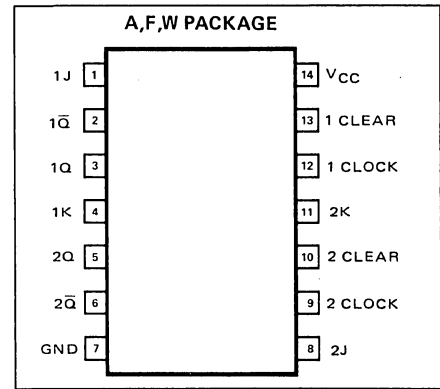
NOTES:

- A. Preset may be tested by applying a high-level voltage to the individual preset inputs and pulsing the preset enable or by applying a high-level voltage to the preset enable and pulsing the individual preset inputs.
 - B. Q_A output is illustrated. Relationship of serial input to other Q outputs is illustrated in the typical shift sequence.
 - C. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.
 - D. $V_{\text{ref}} = 1.3V$
- Load circuit shown at front of book (totem pole outputs).

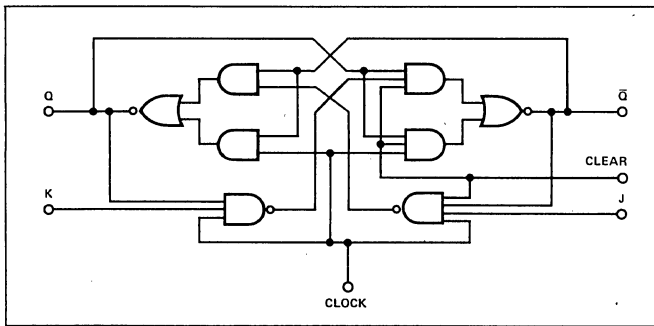
DESCRIPTION

A low logic level at the clear input resets the Q output to a low level regardless of the levels at the other inputs. With clear inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table, as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE (Each Flip-Flop)

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	Q̄
L	X	X	X	L	H
H	↓	L	L	Q ₀	Q̄ ₀
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	TOGGLE
H	H	X	X	Q ₀	Q̄ ₀

H = high level (steady state)
 L = low level (steady state)
 X = irrelevant
 ↓ = transition from high to low level
 Q₀ = the level of Q before the indicated input conditions were established.
 TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
f _{Clock} Clock frequency		30	45		MHz
t _{w(Clock)} Width of clock pulse (high)		20			ns
t _{w(Clear)} Width of clear pulse (low)					ns
t _{Setup} Input setup time	C _L = 15pF, R _L = 2kΩ	25			ns
t _{Hold} Input hold time		20↓			ns
t _{PLH} Propagation delay time, low-to-high-level output from clear or clock (as appropriate)		0↓	11	20	ns
t _{PHL} Propagation delay time, high-to-low-level output from clear or clock (as appropriate)			15	30	ns

Load circuit and typical waveforms are shown at the front of book.

DUAL J-K POSITIVE EDGE-TRIGGERED FLIP-FLOP

54/74LS109

54LS109-F,W • 74LS109-B,F

DESCRIPTION

A low level at preset or clear sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and \bar{K} inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the J and \bar{K} inputs may be changed without affecting the levels at the outputs.

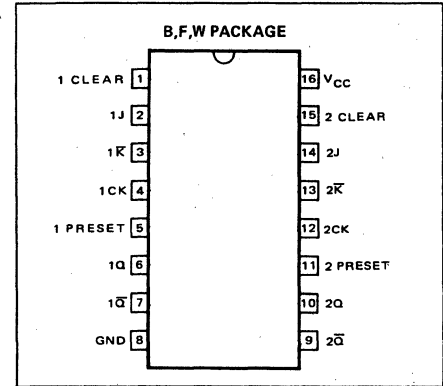
The J and \bar{K} data inputs simplify hardware design as a D-type flip-flop can be implemented by simply tying the J and K inputs together.

FUNCTION TABLE (Each Flip-Flop)

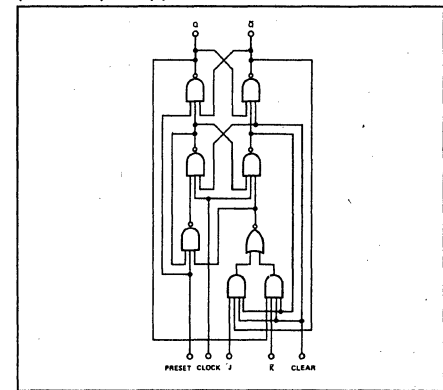
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	\bar{K}	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q ₀	\bar{Q} ₀
H	H	↑	H	H	H	\bar{L}
H	H	L	X	X	Q ₀	\bar{Q} ₀

H = high level (steady state)
 L = low level (steady state)
 X = irrelevant
 ↑ = transition from low to high level
 Q₀ = the level of Q before the indicated steady-state input conditions were established
 TOGGLE: Each output changes to the complement of its previous level on each ↑ clock transition.
 *This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM (Each Flip-Flop)



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LIMITS				
		MIN	TYP	MAX	UNIT	
f _{Clock} Clock frequency	C _L = 15pF, R _L = 2kΩ	25	33		MHz	
t _{w(Clock)} Width of clock pulse (high)		25			ns	
t _{w(Preset)} Width of preset pulse		25			ns	
t _{w(Clear)} Width of clear pulse		25			ns	
t _{Setup} Input setup time		20↑			ns	
t _{Hold} Input hold time		5↑			ns	
t _{PLH} Propagation delay time, low-to-high-level output from clear, preset or clock (as appropriate)				8	25	ns
t _{PHL} Propagation delay time, high-to-low-level output from clear, preset or clock (as appropriate)				16	40	ns

Load circuit and typical waveforms are shown at the front of this section.

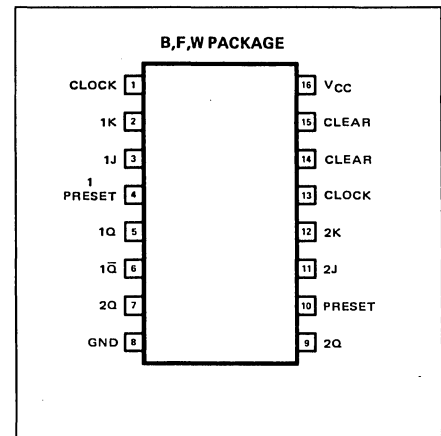
(Separate clock, preset and clear inputs)

54LS112-F,W • 74LS112-B,F

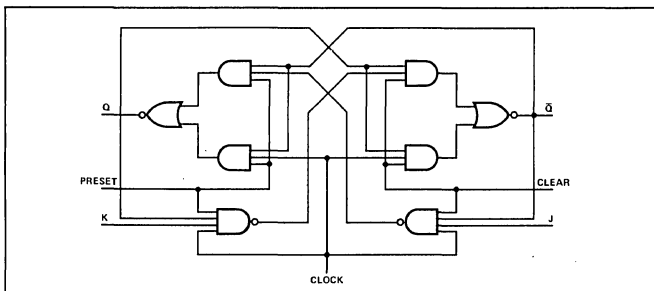
DESCRIPTION

The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL TABLE (Each Flip-Flop)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q ₀	Q̄ ₀
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q ₀	Q̄ ₀

H = high level (steady state)

L = low level (steady state)

X = irrelevant

↓ = transition from high to low level

Q₀ = the level of Q before the indicated steady-state input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

*This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS				
		MIN	TYP	MAX	UNIT	
f _{Clock} Clock frequency	C _L = 15pF, R _L = 2kΩ	30	45		MHZ	
t _{w(Clock)} Width of clock pulse		20			ns	
t _{w(Preset)} Width of preset pulse		25			ns	
t _{w(Clear)} Width of clear pulse		25			ns	
t _{Setup} Input setup time		20↓			ns	
t _{Hold} Input hold time		0↓			ns	
t _{PLH} Propagation delay time, low-to-high-level output from clear, preset or clock (as appropriate)				11	20	ns
t _{PHL} Propagation delay time, high-to-low-level output from clear, preset or clock (as appropriate)				15	30	ns

Load circuit and typical waveforms are shown at the front of book.

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOP

54/74LS113

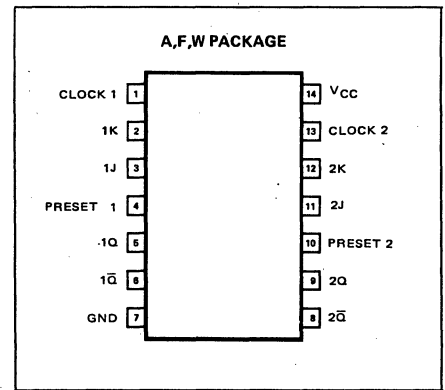
(Separate clock and preset inputs)

54LS113-F,W • 74LS113-A,F

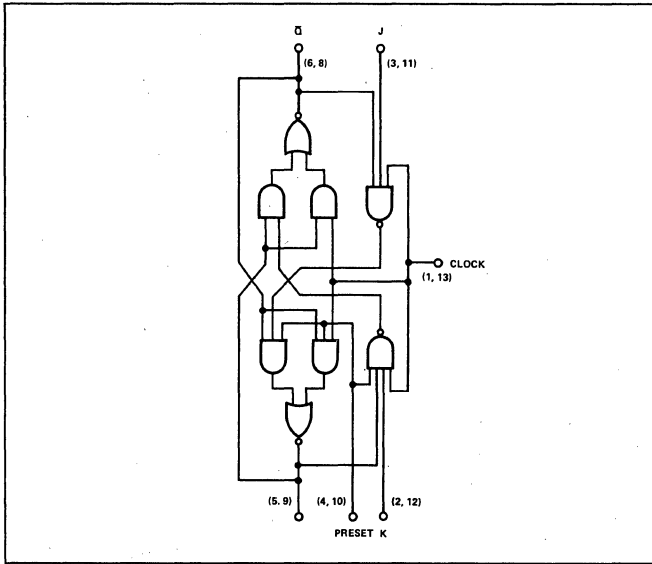
DESCRIPTION

A low level at the preset input sets the Q output high regardless of the levels at the other inputs. When preset is inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM (Each Flip-Flop)



FUNCTION TABLE (Each Flip-Flop)

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	Q̄
L	X	X	X	H	L
H	↓	L	L	Q ₀	Q̄ ₀
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	TOGGLE
H	H	X	X	Q ₀	Q̄ ₀

H = high level (steady state)
 L = low level (steady state)
 X = irrelevant
 ↓ = transition from high to low level
 Q₀ = the level of Q before the indicated steady-state input conditions were established
 TOGGLE: Each output changes to the complement of its previous level of each ↓ clock transition.

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS				
		MIN	TYP	MAX	UNIT	
f_{Clock} Clock frequency	$C_L = 15pF, R_L = 2k\Omega$	30	45		MHz	
$t_{w(Clock)}$ Width of clock pulse		20			ns	
$t_{w(Preset)}$ Width of preset pulse		25			ns	
t_{Setup} Input setup time		20↓			ns	
t_{Hold} Input hold time		0↓			ns	
t_{PLH} Propagation delay time, low-to-high-level output from preset or clock (as appropriate)				11	20	ns
t_{PHL} Propagation delay time, high-to-low-level output from preset or clock (as appropriate)				15	30	ns

Load circuit and waveforms are shown at the front of book.

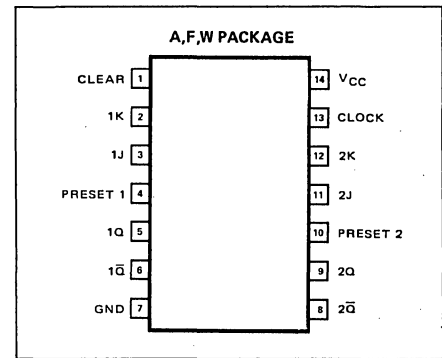
(Separate preset, common clock and clear)

54LS114-F,W • 74LS114-A,F

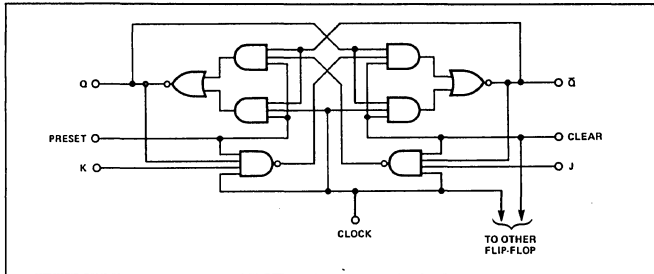
DESCRIPTION

The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM (Each Flip-Flop)



FUNCTION TABLE (Each Flip-Flop)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q ₀	Q̄ ₀
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q ₀	Q̄ ₀

H = high level (steady state)

L = low level (steady state)

X = irrelevant

↓ = transition from high to low level

Q₀ = the level of Q before the indicated steady-state input conditions were established

TOGGLE: = Each output changes to the complement of its previous level on each ↓ clock transition.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS				
		MIN	TYP	MAX	UNIT	
$f_{(Clock)}$ Clock frequency	$C_L = 15pF, R_L = 2k\Omega$	30	45		MHz	
$t_{w(Clock)}$ Width of clock pulse		20			ns	
$t_{w(Preset)}$ Width of preset pulse		25			ns	
$t_{w(Clear)}$ Width of clear pulse		20			ns	
t_{Setup} Input setup time		20↓			ns	
t_{Hold} Input hold time		0↓			ns	
t_{PLH} Propagation delay time, low-to-high-level output from clear, preset or clock (as appropriate)				11	20	ns
t_{PHL} Propagation delay time, high-to-low-level output from clear, preset or clock (as appropriate)				15	30	ns

Load circuit and typical waveforms are shown at the front of this section.

DESCRIPTION

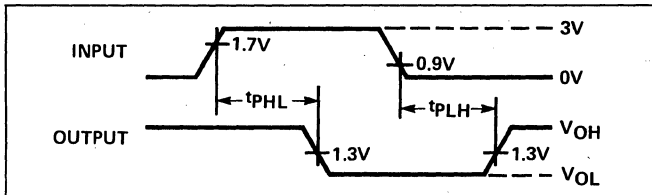
Each circuit functions as a NAND gate, but because of the Schmitt action, it has different input threshold levels for positive- and negative-going signals. The hysteresis or backlash, which is the difference between the two threshold levels, is typically 800 millivolts.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15pF, R_L = 2k\Omega$		15	22	ns
t_{PHL} Propagation delay time, high-to-low-level output			15	22	ns

PARAMETER MEASUREMENT INFORMATION



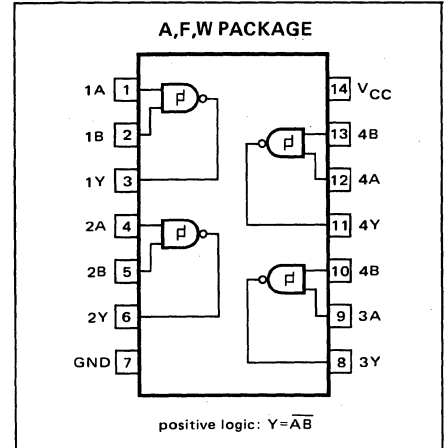
VOLTAGE WAVEFORMS

NOTES:

A. The input waveform is supplied by a generator with the following characteristics: $Z_{out} = 50 \Omega$ and $PRR \leq 1 \text{ MHz}$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$.

Load circuit and waveforms are shown at the front of book.

PIN CONFIGURATION



SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

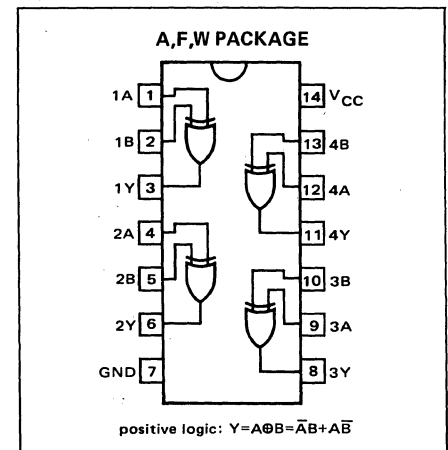
PARAMETER*	FROM (INPUT)	TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low $C_L = 15pF,$ $R_L = 2k\Omega$		18	30	ns
t_{PHL}				18	30	
t_{PLH}	A or B	Other input high		18	30	ns
t_{PHL}					18	

* t_{PLH} = propagation delay time, low-to-high level output

t_{PHL} = propagation delay time, high-to-low-level output

Load circuit and typical waveforms shown in front of book.

PIN CONFIGURATION



FUNCTION TABLE

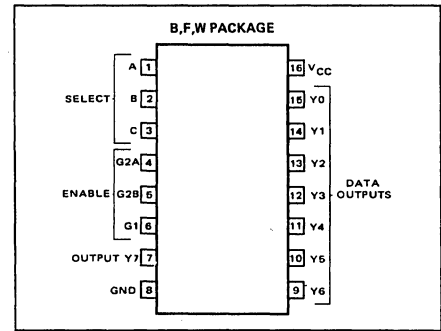
INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

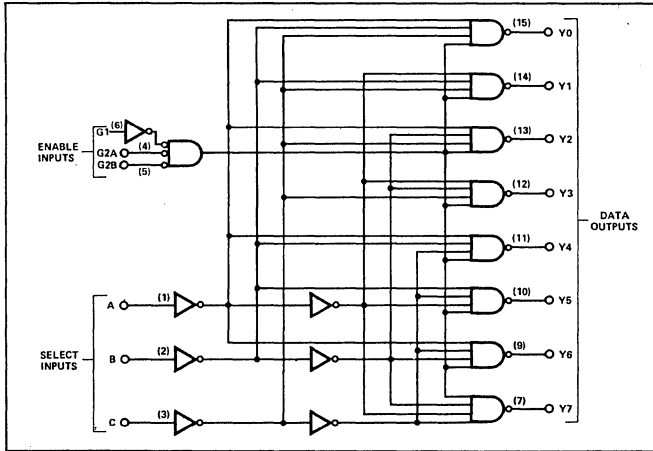
DESCRIPTION

The S54LS138 and N74LS138 decode one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications. Typical delay time through the three-level address circuitry is 22 nanoseconds. Typical power dissipation is 32 milliwatts.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

ENABLE		SELECT			OUTPUTS							
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B
H = high level, L = low level, X = irrelevant

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	LIMITS				
					MIN	TYP	MAX	UNIT	
t_{PLH} t_{PHL} t_{PLH} t_{PHL}	Binary Select	Any	2	$C_L = 15pF,$ $R_L = 2k\Omega$			14	20	ns
			3				20	41	ns
			3				18	27	ns
			3				20	39	ns
t_{PLH} t_{PHL} t_{PLH} t_{PHL}	Enable	Any	2				17	18	ns
			3				15	32	ns
			3				21	26	ns
			3				19	28	ns

¹ t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output. Load circuit and typical waveforms are shown at the front of book.

DUAL 2-TO-4 LINE DECODER/DEMULTIPLEXER

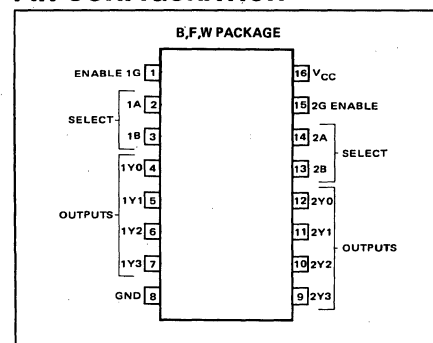
54/74LS139

54LS139-F,W • 74LS139-B,F

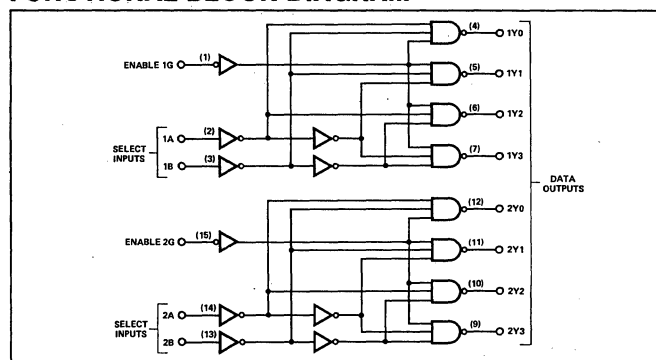
DESCRIPTION

The S54LS139 and N74LS139 comprise two individual two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications. Typical total delay time is 22 nanoseconds through the three-gate-level address circuitry and power consumption is typically 34 milliwatts total.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE (Each Decoder/Demultiplexer)

INPUTS			OUTPUTS			
ENABLE	SELECT		Y0	Y1	Y2	Y3
G	B	A				
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H=high level, L=low level, X=irrelevant

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	LIMITS			
					MIN	TYP	MAX	UNIT
t_{PLH}	Binary	Any	2	$C_L = 15pF, R_L = 2k\Omega$		13	20	ns
t_{PHL}	Select					22	33	ns
t_{PLH}	Enable	Any	3			18	29	ns
t_{PHL}						25	38	ns
t_{PLH}	Enable	Any	2			16	24	ns
t_{PHL}						21	32	ns

¹ t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output. Load circuit and typical waveforms are shown at the front of book.

BCD-TO-DECIMAL DECODER/DRIVER

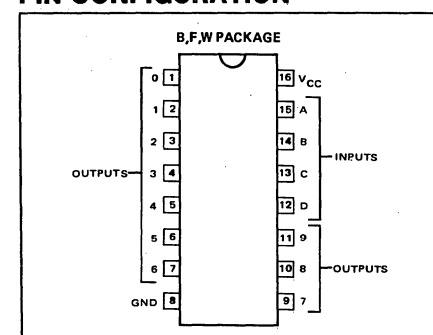
54/74LS145

54LS145-F,W • 74LS145-B,F

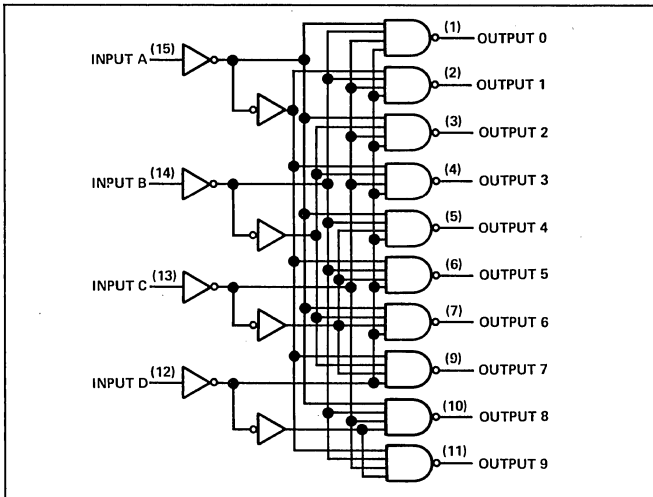
DESCRIPTION

This monolithic BCD-to-decimal decoder/driver consists of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. This decoder features high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (15 volts) will sink up to 80 milliamperes of current. Each input is one standard load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 35 milliwatts.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

NO.	INPUTS				OUTPUTS										
	D	C	B	A	0	1	2	3	4	5	6	7	8	9	
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H

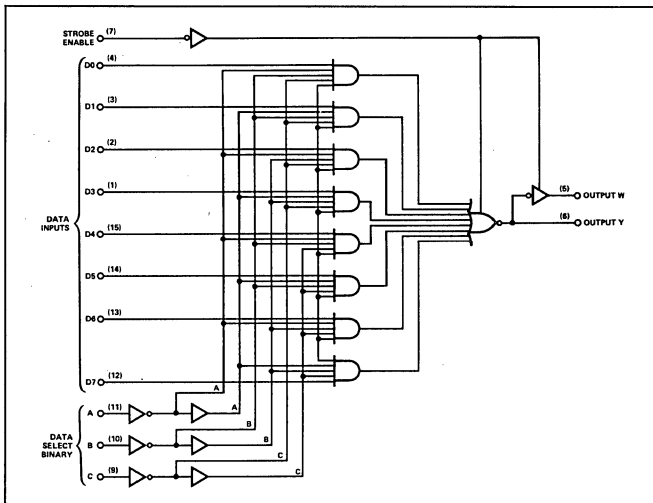
H = high level, (off), L = low level (on)

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
t_{PLH}	$C_L = 45pF, R_L = 665 \Omega$			50	ns
t_{PHL}				50	ns

Load circuit and waveforms are shown at front of book.

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		
SELECT			STROBE S	Y	W	
C	B	A				
X	X	X	H	L	H	
L	L	L	L	D0	$\overline{D0}$	
L	L	H	L	D1	$\overline{D1}$	
L	H	L	L	D2	$\overline{D2}$	
L	H	H	L	D3	$\overline{D3}$	
H	L	L	L	D4	$\overline{D4}$	
H	L	H	L	D5	$\overline{D5}$	
H	H	L	L	D6	$\overline{D6}$	
H	H	H	L	D7	$\overline{D7}$	

H = high level, L = low level, X = irrelevant

$E0, E1 \dots E15$ = the complement of the level of the respective E input

$D0, D1 \dots D7$ = the level of the D respective input

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

54/74LS151

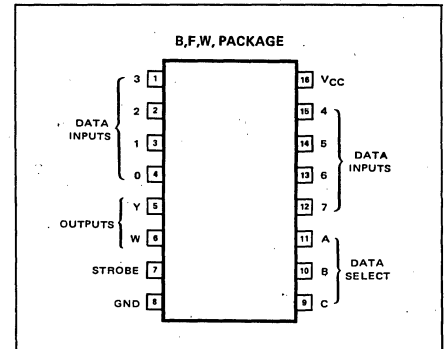
54LS151-F,W • 74LS151-B,F

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
t_{PLH}	A, B, or C	Y	$C_L = 15pF, R_L = 2k\Omega$		27	43	ns
t_{PHL}	(4 levels)				31	50	
t_{PLH}	A, B, or C	W			24	39	ns
t_{PHL}	(3 levels)				20	32	
t_{PLH}	Strobe	Y			23	37	ns
t_{PHL}					25	42	
t_{PLH}	Strobe	W			19	31	ns
t_{PHL}					16	26	
t_{PLH}	Any D	Y			16	26	ns
t_{PHL}					20	32	
t_{PLH}	Any D	W			13	21	ns
t_{PHL}					9	15	

¹ t_{PLH} = Propagation delay time, low-to-high-level output
 t_{PHL} = Propagation delay time, high-to-low-level output
 Load circuit and typical waveforms are shown at front of book.

PIN CONFIGURATION



DUAL 4-LINE TO 1-LINE MULTIPLEXER

54/74LS153

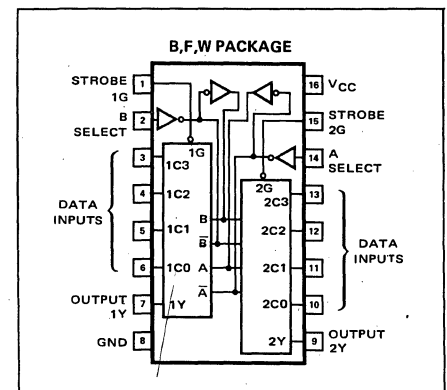
54LS153-F,W • 74LS153-B,F

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MIN	UNIT
t_{PLH}	Data	Y	$C_L = 15pF, R_L = 2k\Omega$		10	15	ns
t_{PHL}	Data				17	26	
t_{PLH}	Select	Y			19	29	ns
t_{PHL}	Select				25	38	
t_{PLH}	Strobe	Y			16	24	ns
t_{PHL}	Strobe				21	32	

¹ t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output
 Load circuit and typical waveforms are shown at the front of book.

PIN CONFIGURATION

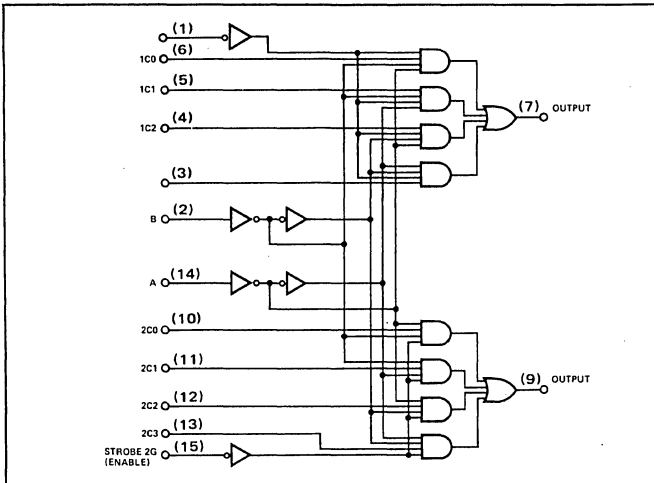


DUAL 4-LINE TO 1-LINE MULTIPLEXER

54/74LS153

54LS153-F,W • 74LS153-B,F

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

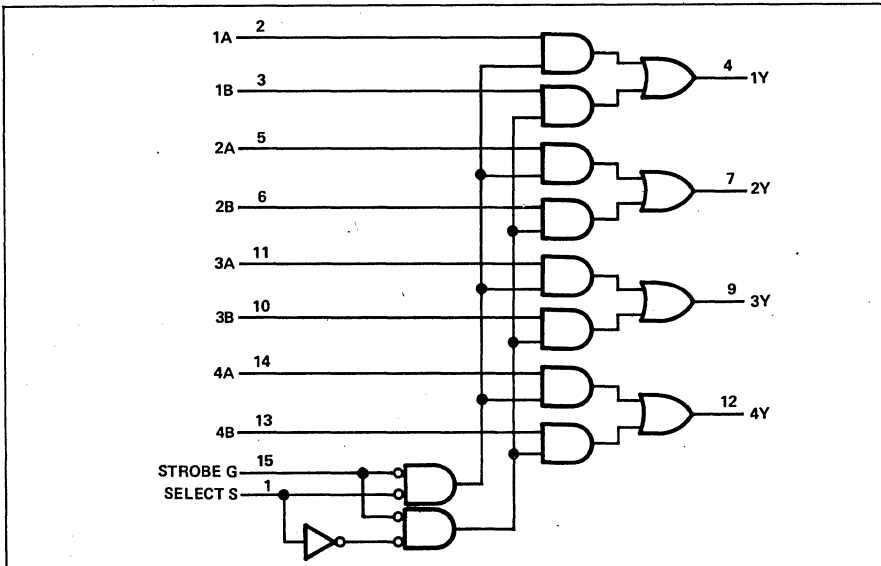
Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

QUAD 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER (NON-INV.)

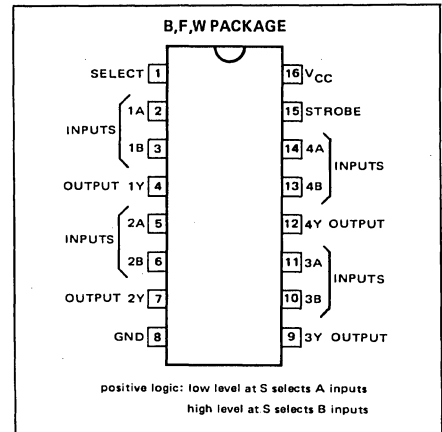
54/74LS157

54LS157-F,W • 74LS157-B,F

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



FUNCTION TABLE

INPUTS		OUTPUT Y		
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

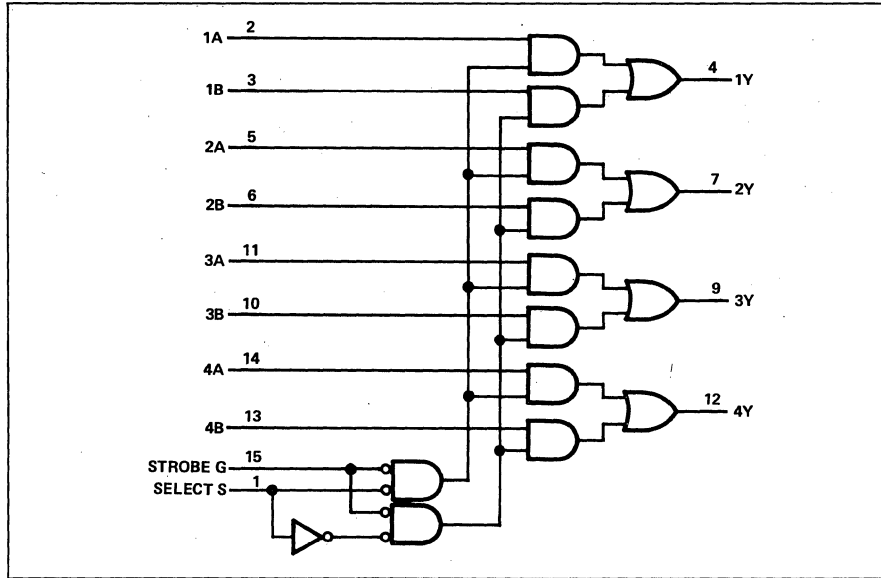
PARAMETER*	FROM (INPUT)	TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
t_{PLH}	Data	$C_L = 15pF,$ $R_L = 2k\Omega,$		9	14	ns
t_{PHL}				12	19	
t_{PLH}	Strobe			16	25	ns
t_{PHL}				17	27	
t_{PLH}	Select			16.5	26	ns
t_{PHL}				19	30	

* t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output

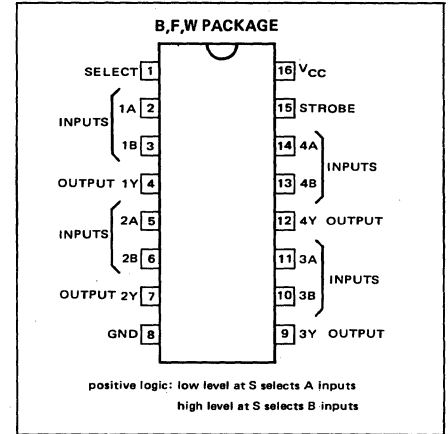
Load circuit and waveforms are shown in front of book.

Signetics

BLOCK DIAGRAM



PIN CONFIGURATION



SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER*	FROM (INPUT)	TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
t_{PLH}	Data	$C_L = 15pF, R_L = 2k\Omega$		8	13	ns
t_{PHL}				8	13	
t_{PLH}	Strobe			14	25	ns
t_{PHL}				16	27	
t_{PLH}	Select			13	20	ns
t_{PHL}				16	24	

★ t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output
 Load circuits and waveforms are shown at the front of the book.

FUNCTION TABLE

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = high level, L = low level, X = irrelevant

DESCRIPTION

This synchronous presettable decade counter features an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the 54/74LS160 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

The 54/74LS160 features a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

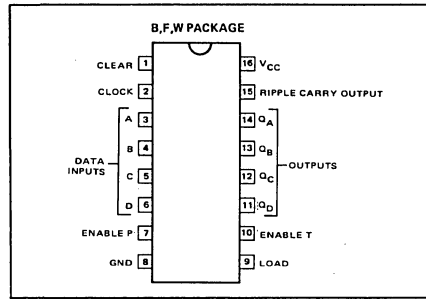
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			UNIT
				MIN	TYP	MAX	
f _{Clock}				25	32		MHZ
t _{w(Clock)}	Width of clock pulse			25			ns
t _{w(Clear)}	Width of clear pulse			20			ns
t _{Setup}	Input setup time	A,B,C,D	C _L = 15pF, R _L = 2kΩ See Figures 1 and 2 and Note 1	0↑			
		Enable Port		20↑			ns
		Load		20↑			ns
t _{Hold}	Input hold time	A,B,C,D		25↑ ²			ns
		Others		10↑ ²			ns
t _{PLH} t _{PHL}		Clock	Ripple carry		23	35	ns
		Clock	Any		16	24	
		(load input high)	Q		18	27	ns
		Clock	Any		17	25	
		(load input low)	Q		19	29	ns
		Enable T	Ripple carry		15	23	ns
		Clear	Any Q		26	38	ns

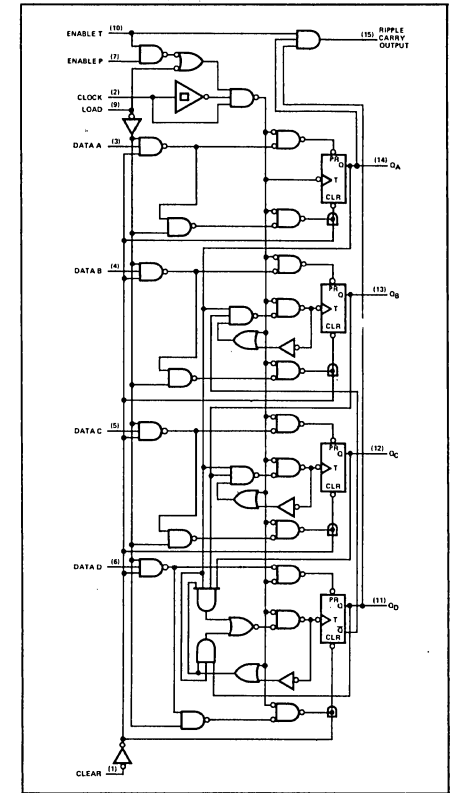
* f_{max} = Maximum clock frequency
 t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output

NOTES:
 1. Propagation delay for clearing is measured from the clear input.
 2. The minimum hold time is as specified or as long as the clock input takes to rise from 0.8V. to 2.0V., whichever is longer.

PIN CONFIGURATION



BLOCK DIAGRAM



DIGITAL

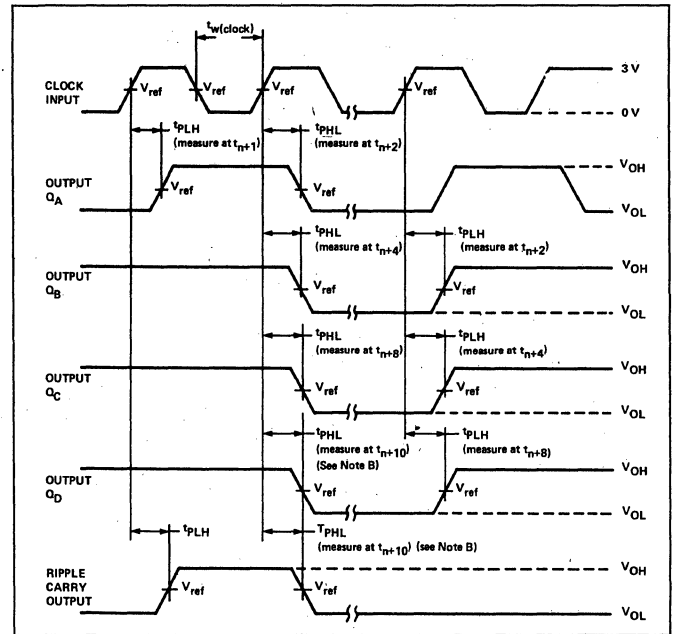
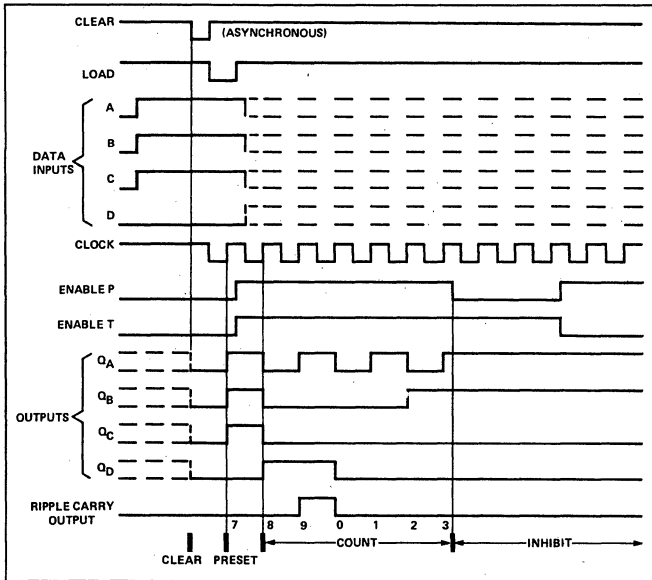
Signetics

PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit



VOLTAGE WAVEFORMS

NOTES:

- The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\Omega$, $t_r \leq 15ns$, $t_f \leq 6ns$.
- Outputs Q_D and carry are tested at t_n+10 , where t_n is the bit time when all outputs are low.
- $V_{ref} = 1.3V$.

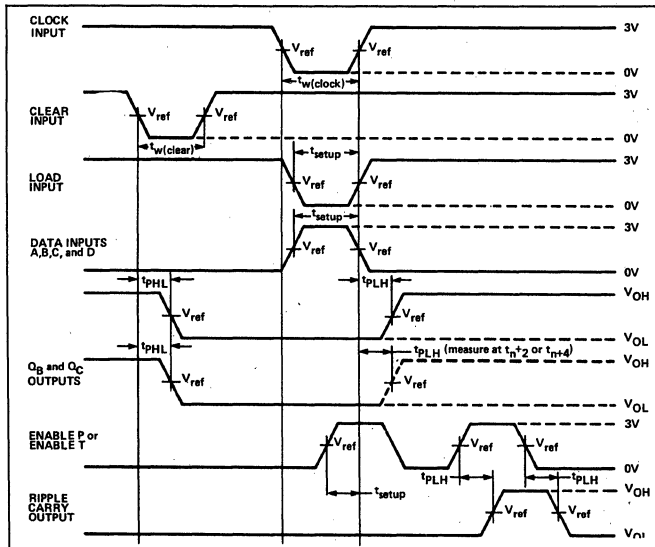
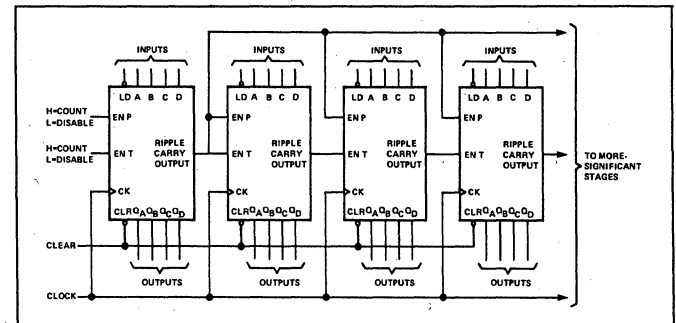
Load circuit is shown at front of book (totem pole outputs).

FIGURE 1—SWITCHING TIMES

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 54/74LS160 will count in BCD. Virtually any count mode (modulo-N, N_1 -to- N_2 , N_1 -to-maximum) can be used with this fast look-ahead circuit.

TYPICAL APPLICATION DATA



VOLTAGE WAVEFORMS

NOTES:

- The input pulses are supplied by generators having the following characteristics. PRR ≤ 1MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\Omega$, $t_r \leq 15ns$, $t_f \leq 6ns$.
- Enable P and enable T setup times are measured at $t_N + 0$
- $V_{ref} = 1.3V$.

Load circuit is shown at front of book (totem pole outputs).

FIGURE 2—SWITCHING TIMES

DESCRIPTION

This synchronous presettable binary counter features an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the 54/74LS161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

The 54/74LS161 features a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

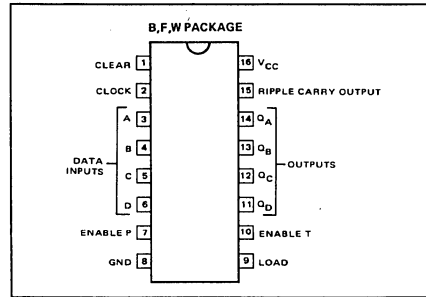
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
f _{Clock}				25	32		MHz
t _w (Clock)	Width of clock pulse			25			ns
t _w (Clear)	Width of clear pulse			20			ns
t _{Setup}	Input setup time	Q	C _L = 15pF, R _L = 2kΩ, See Figures 1 and 2 and Note 1	0†			
		Q		20†			ns
		Q		20†			ns
		Ripple carry		25† ²			ns
t _{Hold}	Input hold time			10† ²			ns
t _{PLH}					23	35	
t _{PHL}	Clock	Ripple carry			23	35	ns
t _{PLH}					16	24	
t _{PHL}	Clock (load input high)	Any Q			18	27	ns
t _{PLH}					17	25	
t _{PHL}	Clock (load input low)	Any Q			19	29	ns
t _{PLH}					15	23	
t _{PHL}	Enable T	Ripple carry			15	23	ns
t _{PHL}	Clear	Any Q			26	38	ns

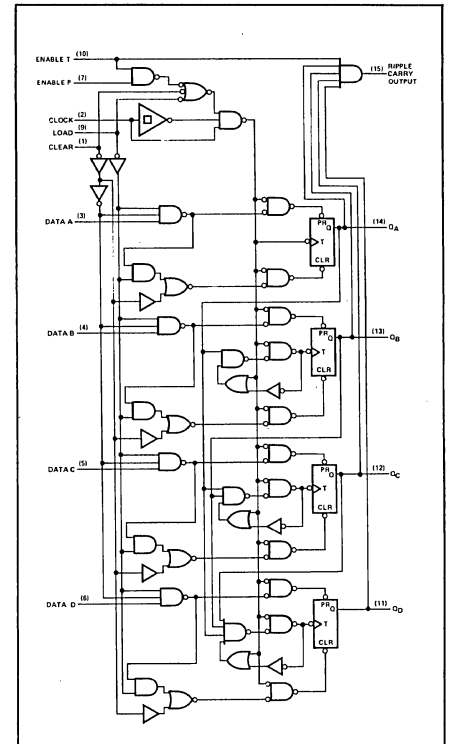
* f_{max} = Maximum clock frequency
 †_{PLH} = propagation delay time, low-to-high-level output
 †_{PHL} = propagation delay time, high-to-low-level output

NOTES:
 1. Propagation delay for clearing is measured from the clear input.
 2. The minimum hold time is as specified or as long as the clock input takes to rise from 0.8V. to 2.0V., whichever is longer.

PIN CONFIGURATION



BLOCK DIAGRAM

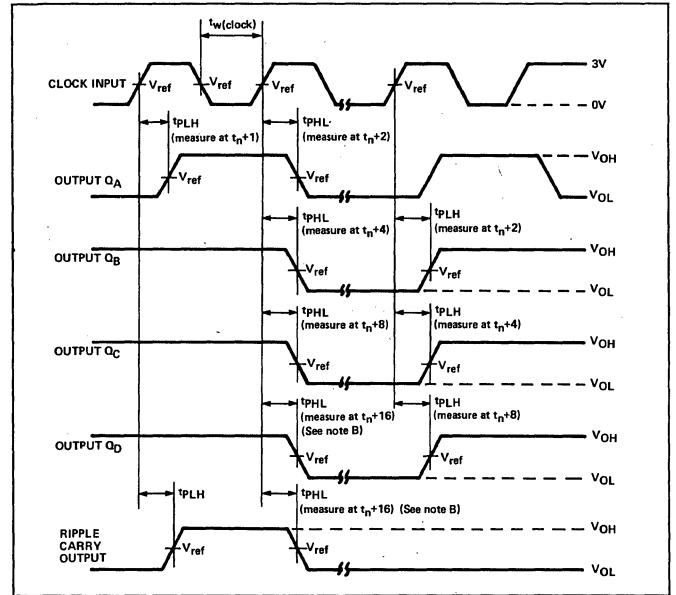
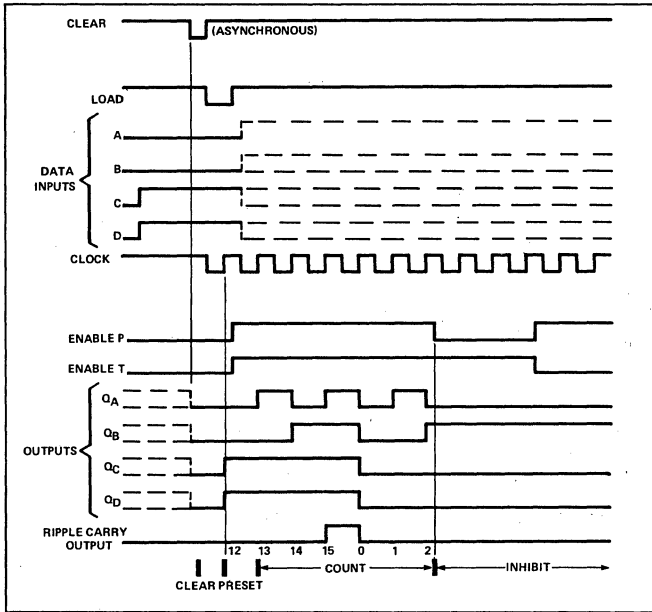


PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit



VOLTAGE WAVEFORMS

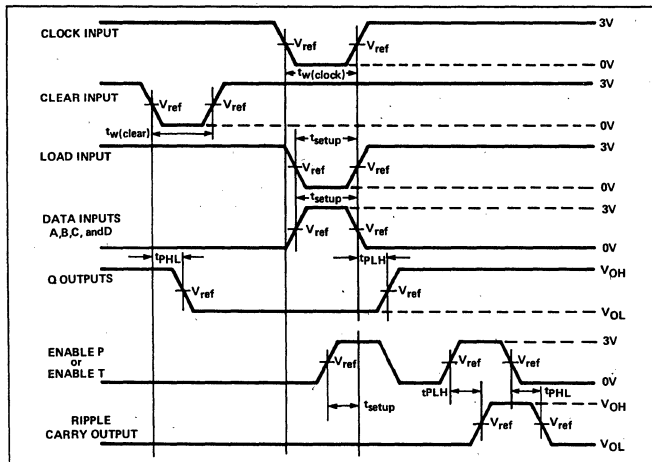
NOTES

- The input pulses are supplied by a generator having the following characteristics: PRR \leq 1MHz, Duty Cycle \leq 50%, $Z_{out} \approx 50\Omega$, $t_r \leq 15ns$, $t_f \leq 6ns$.
- Outputs Q_D and carry are tested at t_{n+16} , where t_n is the bit time when all outputs are low.
- $V_{ref} = 1.3V$.

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 54/74LS161 will count in binary. Virtually any count mode (modulo-N, N_1 -to- N_2 , N_1 -to-maximum) can be used with this fast look-ahead circuit.

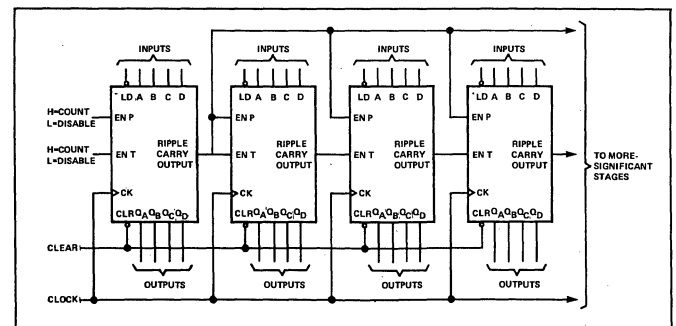


VOLTAGE WAVEFORMS

NOTES

- The input pulses are supplied by generators having the following characteristics: PRR \leq 1MHz, Duty cycle \leq 50%, $Z_{out} \approx 50\Omega$, $t_r \leq 15ns$, $t_f \leq 6ns$.
- Enable P and T setup times are measured at t_{n+0} .
- $V_{ref} = 1.3V$.

Load circuit is shown at front of book (totem pole outputs)



DESCRIPTION

This synchronous presettable decade counter features an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveforms.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the 54/74LS162 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

The 54/74LS162 features a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable set up and hold times.

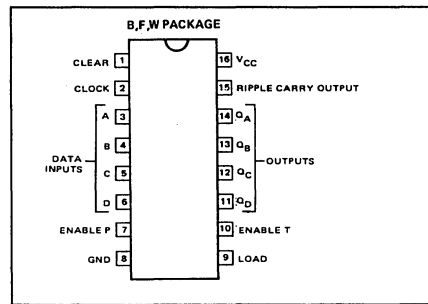
SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			UNIT
				MIN	TYP	MAX	
f_{Clock}				25	32		MHz
t_w Clock	Width of Clock Pulse			25			ns
t_w (Clear)	Width of Clear Pulse			20			ns
t_{Setup}	Input Setup Time	A,B,C,D Enable P or T Load Clear	Q Q Q Q	0† 20† 20† 20†			ns
t_{Hold}	Input Hold Time	A,B,C,D Others		25† ² 10† ²		ns	ns
t_{PLH}			Ripple carry		23	35	ns
t_{PHL}		Clock			23	35	
t_{PLH}		Clock	Any		16	24	ns
t_{PHL}		Clock (load input high)	Q		18	27	
t_{PLH}		Clock	Any		17	25	ns
t_{PHL}		Clock (load input low)	Q		19	29	
t_{PLH}		Enable T	Ripple carry		15	23	ns
t_{PHL}					15	23	
t_{PHL}		Clear	Any Q		26	38	ns

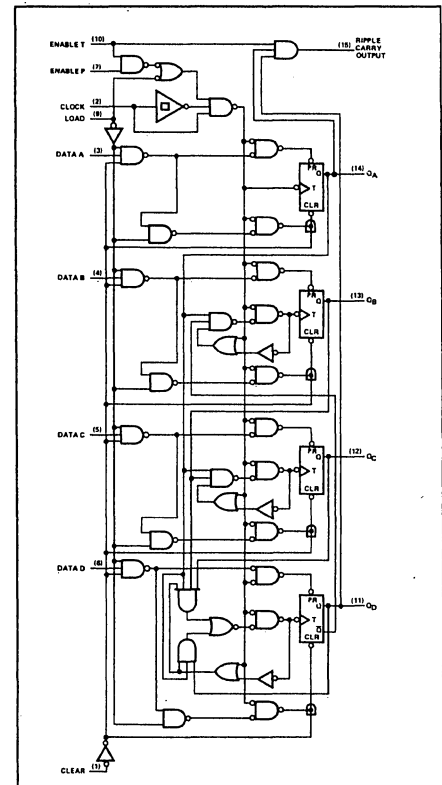
* t_{max} = Maximum clock frequency
 t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output

NOTES:
 1. Propagation delay for clearing is measured from the clock input transition.
 2. The minimum hold time is as specified or as long as the clock input takes to rise from 0.8V to 2.0V., whichever is longer.

PIN CONFIGURATION



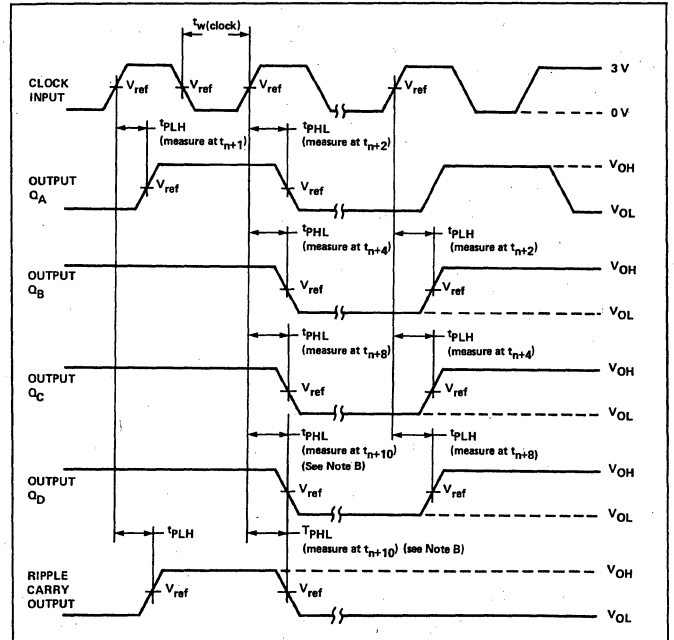
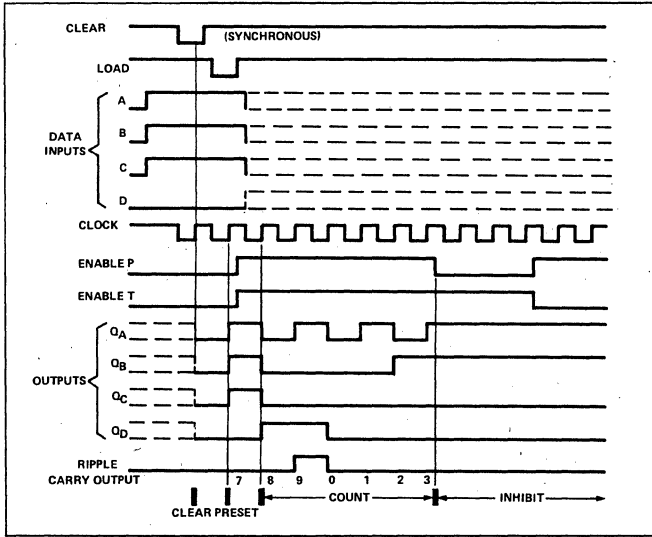
BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION
TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit



VOLTAGE WAVEFORMS

NOTES:

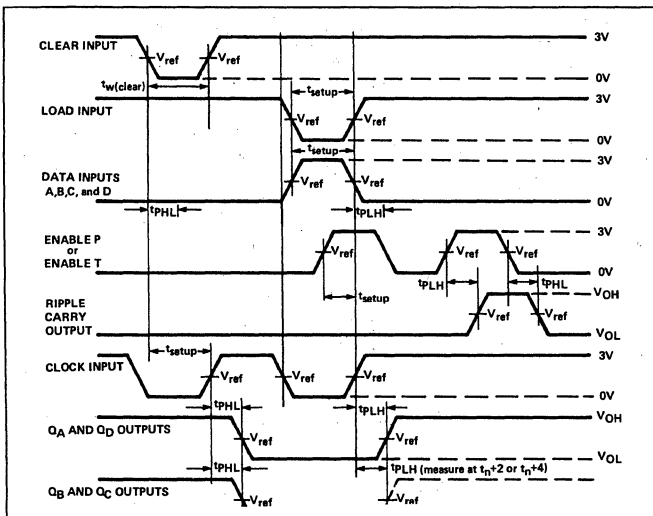
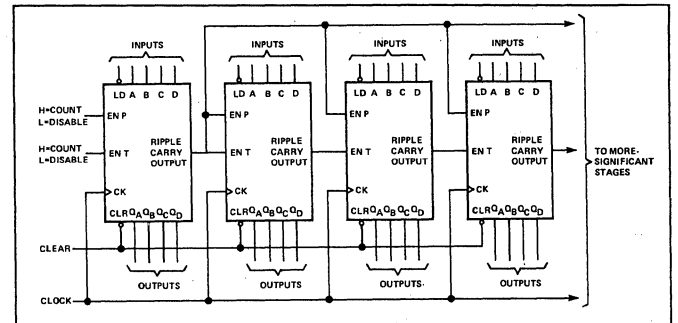
- The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1MHz, duty cycle ≤ 50%, $Z_{out} \approx 50 \Omega$; $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$; vary PRR to measure f_{max} .
 - Outputs Q_D and carry are tested at t_{n+10} where t_n is the bit time when all outputs are low.
 - $V_{ref} = 1.5 \text{ V}$.
- Load Circuit information is shown at the front of the book.

FIGURE 1-SWITCHING TIMES

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 54/74LS162 will count in BCD. Virtually any count mode (modulo-N, N_1 -to- N_2 , N_1 -to-maximum) can be used with this fast look-ahead circuit.



VOLTAGE WAVEFORMS

NOTES:

- The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50 \Omega$; $t_r < 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$.
- Enable P and enable T setup times are measured at t_{n+0} .
- $V_{ref} = 1.3 \text{ V}$.

FIGURE 2-SWITCHING TIMES

DESCRIPTION

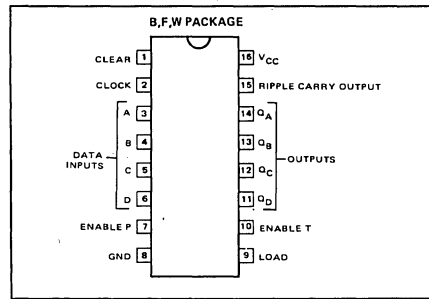
This synchronous presettable binary counter features an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveforms.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the 54/74LS163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

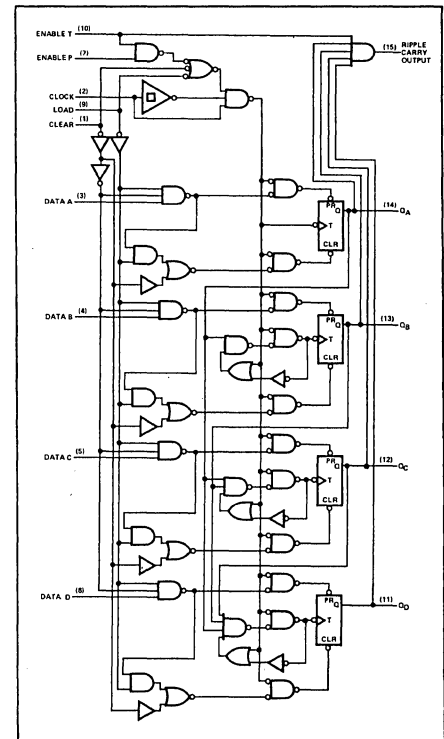
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

The 54/74LS163 features a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

PIN CONFIGURATION



BLOCK DIAGRAM



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

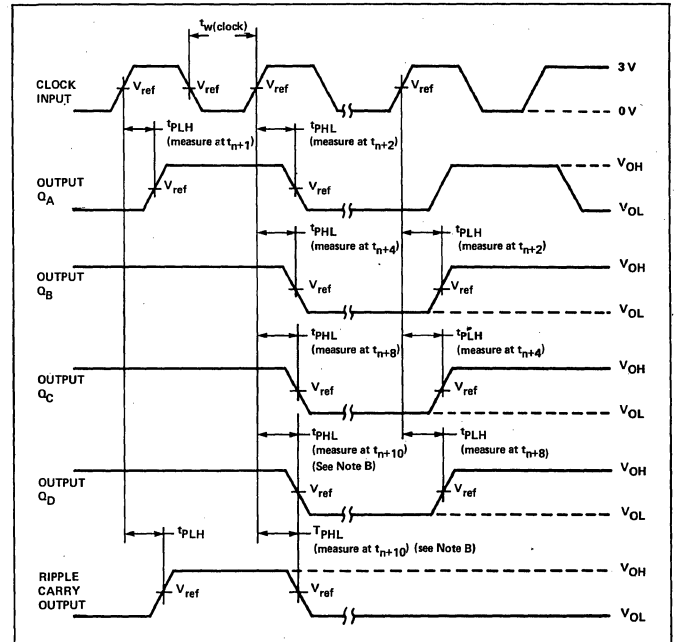
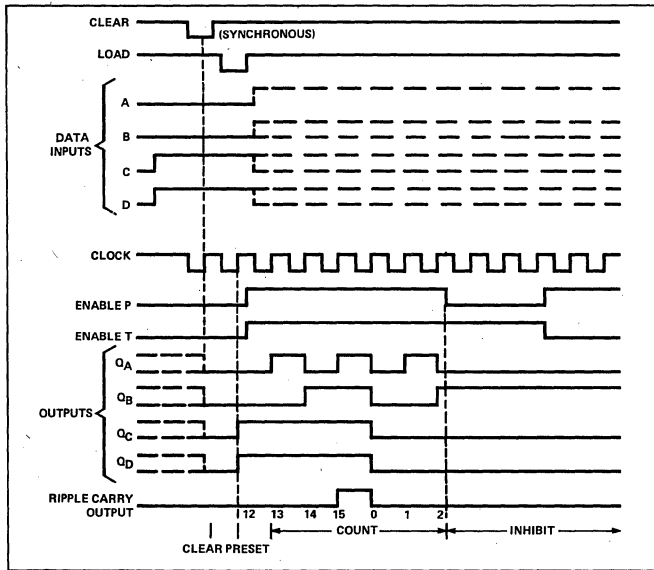
PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
f _{Clock}				25	32		MHz
t _{w(Clock)}	Width of clock pulse			25			ns
t _{w(Clear)}	Width of clear pulse			20			ns
t _{Setup}	Input setup time	A,B,C,D		0†			ns
		Enable Port		20†			ns
		Load		20†			ns
		Clear		20†			ns
t _{Hold}	Input hold time	A,B,C,D	C _L = 15pF, R _L = 2kΩ, See Figures	25†+			ns
		Others		10 ¹²		ns	
t _{PLH}		Ripple carry	1 and 2 and Note 1		23	35	ns
t _{PHL}		Ripple carry			23	35	ns
t _{PLH}		Any			16	24	ns
t _{PHL}		Q			18	27	ns
t _{PLH}		Any			17	25	ns
t _{PHL}		Q			19	29	ns
t _{PLH}		Ripple carry			15	23	ns
t _{PHL}		Ripple carry			15	23	ns
t _{PHL}		Any Q			26	38	ns

* f_{max} = Maximum clock frequency
 t_{PLH} = propagation delay time, low-to-high-level output.
 t_{PHL} = propagation delay time, high-to-low-level output

NOTES:
 1. Propagation delay for clearing is measured from the clock input transition.
 2. The minimum hold time is as specified or as long as the clock input takes to rise from 0.8V_I to 2.0V_I, whichever is longer.

PARAMETER MEASUREMENT INFORMATION
TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES
 Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit

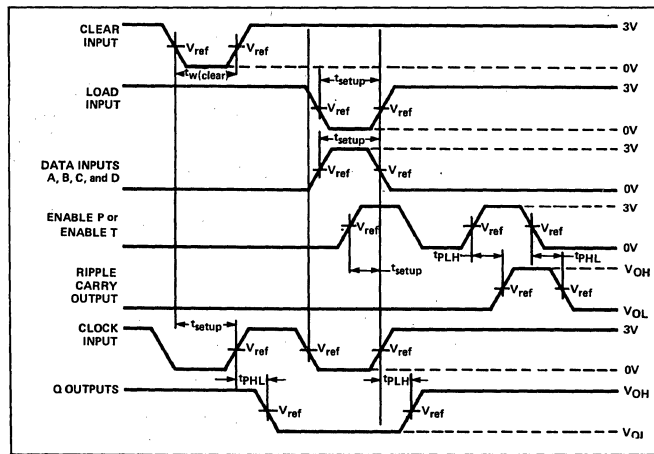


VOLTAGE WAVEFORMS

NOTES:

- The input pulses are supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{out} \approx 50 \Omega$; $t_r \leq 15$ ns, $t_f \leq 6$ ns. Vary PRR to measure f_{max} .
 - Outputs Q_D and carry are tested at t_{n+16} where t_n is the bit time when all outputs are low.
 - $V_{ref} = 1.3$ V.
- Load circuit is shown at the front of the book.

FIGURE 1—SWITCHING TIMES



VOLTAGE WAVEFORMS

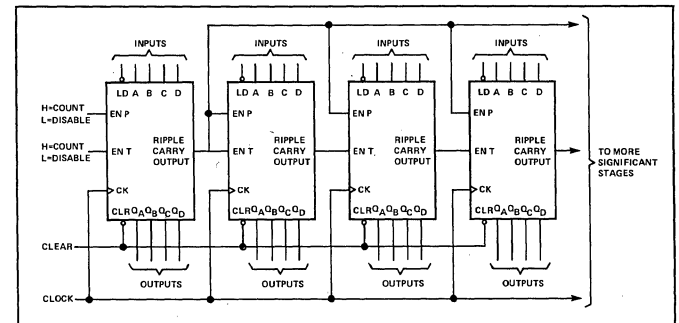
NOTES:

- The input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $Z_{out} \approx 50 \Omega$; '163, $t_r \leq 10$ ns, $t_f \leq 10$ ns; and for 'LS160 thru 'LS163, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
- Enable P and enable T setup times are measured at t_{n+0} .
- $V_{ref} = 1.3$ V.

FIGURE 2—SWITCHING TIMES

TYPICAL APPLICATION DATA
N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 54/74LS163, will count in binary. Virtually any count mode (modulo-N, N_1 -to- N_2 , N_1 -to-maximum) can be used with this fast look-ahead circuit.



8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

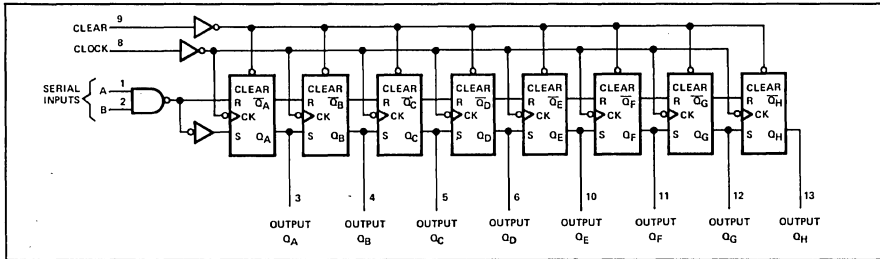
54/74LS164

54LS164-F, W • 74LS164-A, F

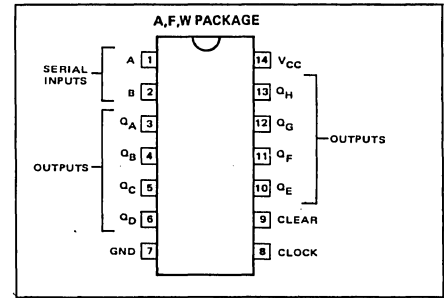
DESCRIPTION

This 8-bit shift register features gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but the only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



FUNCTION TABLE

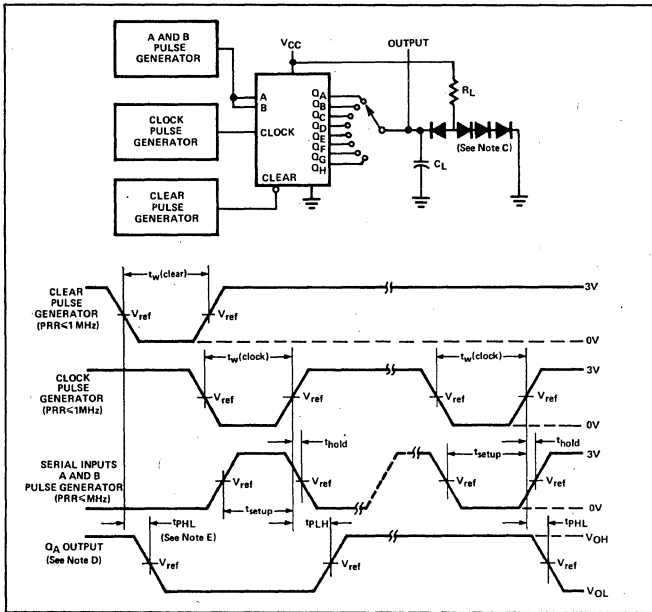
INPUTS		OUTPUTS				
CLEAR	CLOCK	A	B	QA	QB	QH
L	X	X	X	L	L	L
H	L	X	X	QA0	QB0	QH0
H	↑	H	H	H	QAn	QGn
H	↑	L	X	L	QAn	QGn
H	↑	X	L	L	QAn	QGn

H = high level (steady state), L = low level (steady state)
 X = irrelevant (any input, including transitions)
 ↑ = transition from low to high level.
 QA0, QB0, QH0 = the level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established.
 QAn, QGn = the level of QA or QG before the most-recent ↑ transition of the clock; indicates a one-bit shift.

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS				
		MIN	TYP	MAX	UNIT	
f_{Clock} Clock frequency	$C_L = 15pF, R_L = 2k\Omega,$ See Figure 1	25	36		MHz	
t_w Width of clock or clear input pulse		20			ns	
t_{Setup} Input setup time		15↑			ns	
t_{Hold} Input hold time		5↑			ns	
t_{PHL} Propagation delay time, high-to-low-level Q outputs from clear input				24	36	ns
t_{PLH} Propagation delay time, low-to-high-level Q outputs from clock input				17	27	ns
t_{PHL} Propagation delay time, high-to-low-level Q outputs from clock input				21	32	ns

PARAMETER MEASUREMENT INFORMATION

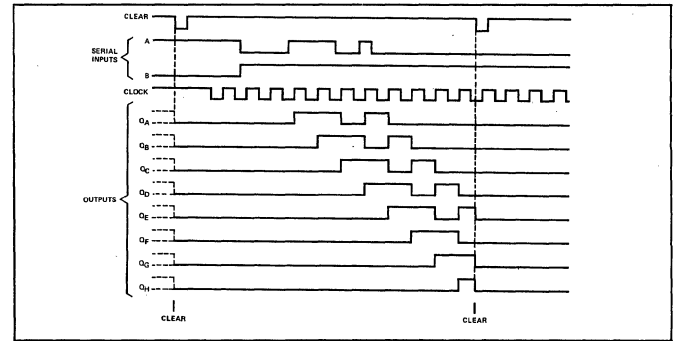


VOLTAGE WAVEFORMS

NOTES:

- A. The pulse generators have the following characteristics: duty cycle $\leq 50\%$, $Z_{out} \approx 50\Omega$; $t_r \leq 15$ ns, $t_f \leq 6$ ns.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or 1N916.
- D. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
- E. Outputs are set to the high level prior to the measure of t_{PHL} from the clear input.
- F. $V_{ref} = 1.3V$.

TYPICAL CLEAR, SHIFT, AND CLEAR SEQUENCES



DESCRIPTION

The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

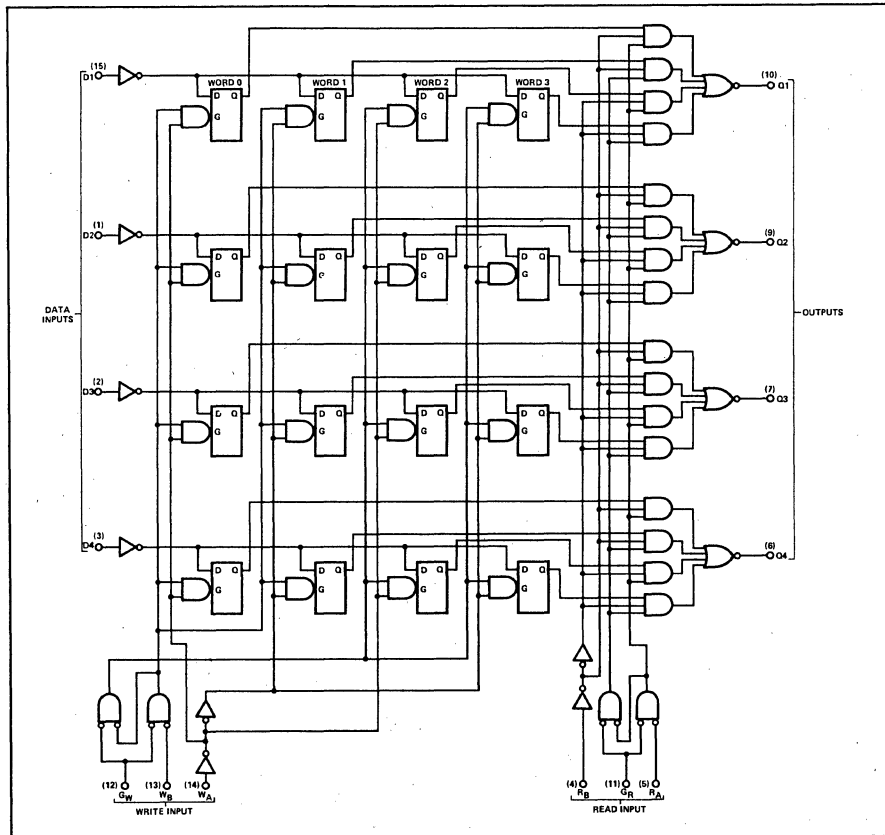
Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W , is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R , is high, the data outputs are inhibited and remain high.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

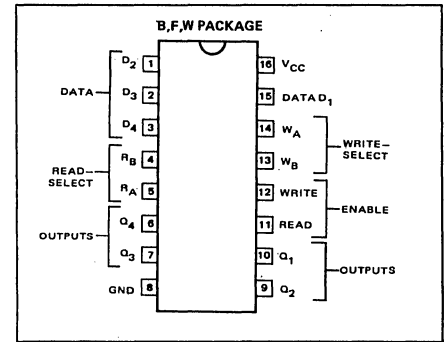
This arrangement—data-entry addressing separate from data read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (30 nanoseconds typical) and the read time (25 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

All inputs except the read enable and write enable of the 54/74LS170 are buffered to lower the drive requirements to one Series 54LS/74LS standard load, respectively. Input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



READ FUNCTION TABLE

(See Notes A and D)

READ INPUTS			OUTPUTS			
R _B	R _A	G _R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

WRITE FUNCTION TABLE

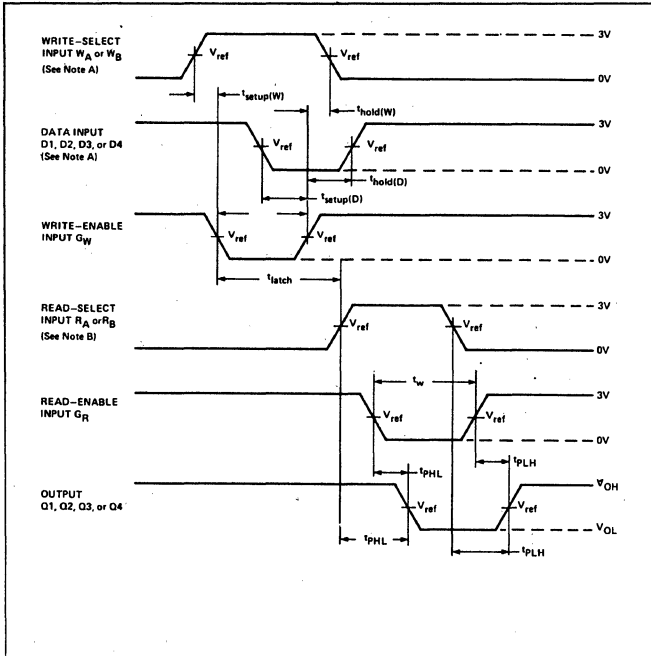
(See Notes A, B, and C)

WRITE INPUTS			WORD			
W _B	W _A	G _W	0	1	2	3
L	L	L	Q = D	Q ₀	Q ₀	Q ₀
L	H	L	Q ₀	Q = D	Q ₀	Q ₀
H	L	L	Q ₀	Q ₀	Q = D	Q ₀
H	H	L	Q ₀	Q ₀	Q ₀	Q = D
X	X	H	Q ₀	Q ₀	Q ₀	Q ₀

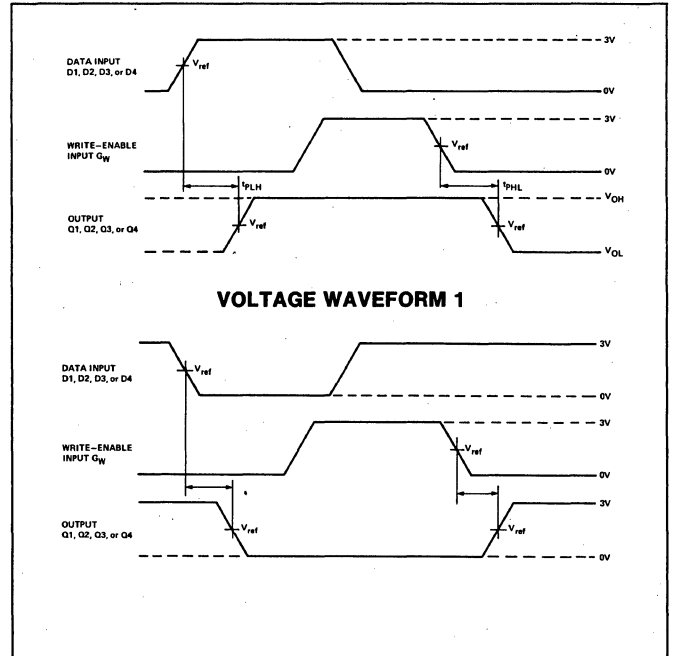
NOTES:

- A. H = high level, L = low level, X = irrelevant.
- B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
- C. Q₀ = The level of Q before the indicated input conditions were established.
- D. W0B1 = The first bit of word 0, etc.

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS
FIGURE 1



VOLTAGE WAVEFORM 2
FIGURE 2

NOTES:

- A. High-level input pulses at the select and data inputs are illustrated in Figure 2; however, times associated with low-level pulses are measured from the same reference points.
- B. When measuring delay times from a read-select input, the read-enable input is low. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.
- C. In Figure 2, each select address is tested. Prior to the start of each of the above tests, both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test G_R is low.
- D. $V_{ref} = 1.3V$.

Load circuits are shown at the front of book (open collector outputs).

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
t_w	Width of write-enable or read-enable pulse			25			ns
t_{Setup}	Input setup time (See fig. 2)	Data input Write-select		10 15			ns ns
t_{Hold}	Input hold time (See notes 3 & fig. 2)	Data input Write select	$C_L = 15pF, R_L = 2k\Omega$	15 5			ns ns
t_{Latch}	Latch time for new data			25			
t_{PLH} t_{PHL}	Read enable	Any Q	$C_L = 15pF, R_L = 2k\Omega$ See Figure 1	20 20	20	30 30	ns ns
t_{PLH} t_{PHL}	Read select	Any Q		25 24	25	40 40	ns ns
t_{PLH} t_{PHL}	Write-enable	Any Q	$C_L = 15pF, R_L = 2k\Omega$ See Figure 2	30 26	30	45 40	ns ns
t_{PLH} t_{PHL}	Data	Any Q		30 22	30	45 35	ns ns

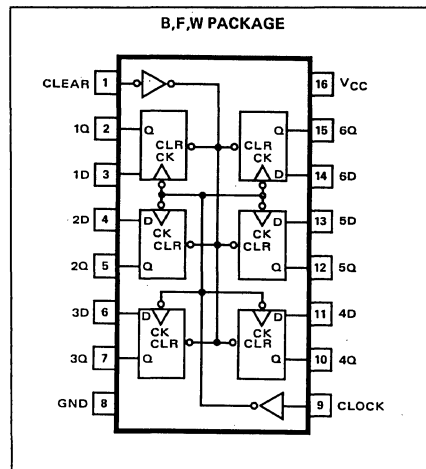
NOTE:

- 1. t_{PLH} = propagation delay time, low-to-high-level output
- t_{PHL} = propagation delay time, high-to-low-level output

DESCRIPTION

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the input signal has no effect at the output.

PIN CONFIGURATION



FUNCTION TABLE (Each Flip-Flop)

INPUTS			OUTPUTS
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀

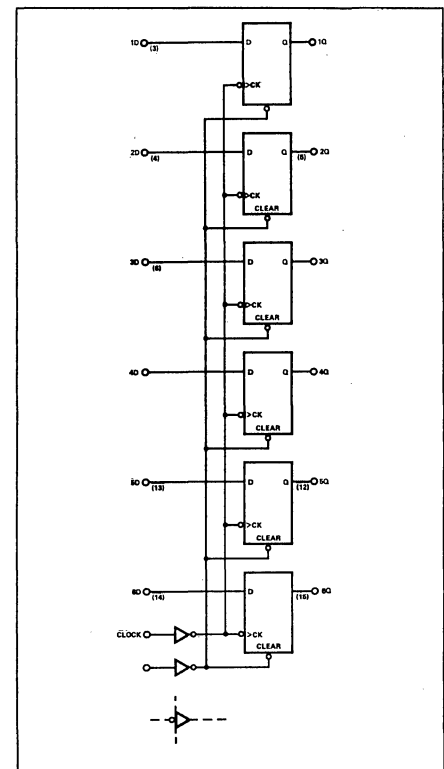
H = high level (steady state)
 L = low level (steady state)
 X = irrelevant
 ↑ = transition from low to high level
 Q₀ = the level of Q before the indicated steady-state input conditions were established

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
f _{Clock}	Clock frequency	30	40		MHz
t _w	Width of clock or clear pulse	20			ns
t _{Setup}	Input setup time				
	Data input	20↑			ns
t _{Hold}	Clear inactive-state	25↑			ns
	Input hold time	5↑			ns
t _{PHL}	Propagation delay time, high-to-low-level output from clear		23	35	ns
t _{PLH}	Propagation delay time, low-to-high-level output from clock		20	30	ns
t _{PHL}	Propagation delay time, high-to-low-level output from clock		21	35	ns

Load circuit and typical waveforms are shown at the front of book.

FUNCTIONAL BLOCK DIAGRAM



QUAD D-TYPE EDGE-TRIGGERED FLIP-FLOP

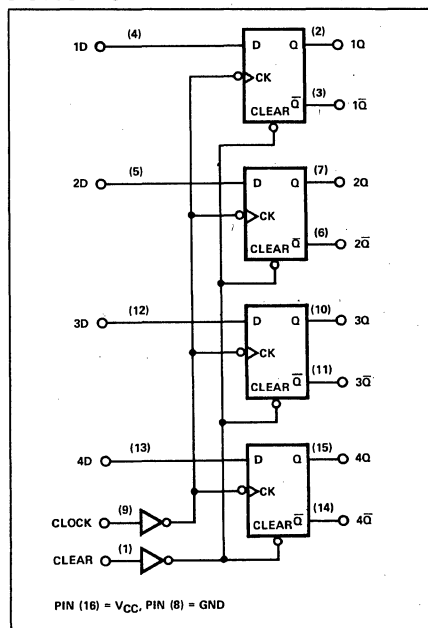
54/74LS175

54LS175-F,W • 74LS175-B,F

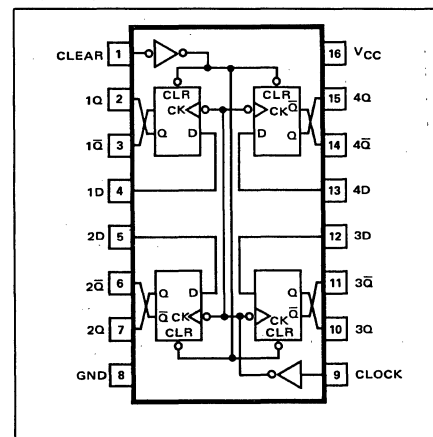
DESCRIPTION

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
f_{Clock} Maximum clock frequency		30	40		MHz
t_w Width of clock or clear pulse		20			ns
t_{Setup} Input setup time					
Data input		20			ns
Clear inactive-state		25			ns
t_{Hold} Input hold time		5			ns
t_{PLH} Propagation delay time, low-to-high-level output from clear	$C_L = 15pF, R_L = 2k\Omega$		16	25	ns
t_{PHL} Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			20	30	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			21	30	ns

FUNCTION TABLE (Each Flip-Flop)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	\bar{Q}
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	\bar{Q}_0

H = high level (steady state)
 L = low level (steady state)
 X = irrelevant
 ↑ = transition from low to high level
 Q_0 = the level of Q before the indicated steady-state input conditions were established

Load circuit and typical waveforms are shown at the front of book.

DESCRIPTION

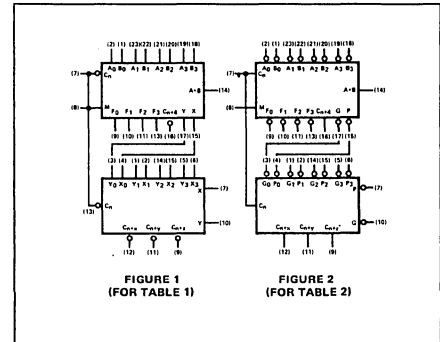
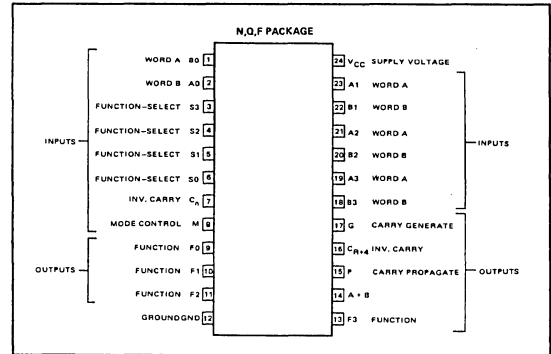
The S54/N74LS181 arithmetic logic unit (ALU)/function generators have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the 182 full carry look-ahead circuit, high-speed arithmetic operations can be performed.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The S54/N74LS181 will accommodate active-high or active-low data if the pin designations are interpreted as follows: Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is $A - B - 1$ which requires an end-around or forced carry to provide $A - B$.

The S54/74LS181 can also be utilized as a comparator. The $A = B$ output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality ($A = B$). The ALU should be in the subtract mode with $C_n = H$ when performing this comparison. The $A = B$ output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1 S0 at L, H, H, L, respectively.

PIN CONFIGURATION



INPUT C_n	OUTPUT C_{n+4}	ACTIVE-HIGH DATA (FIGURE 1)	ACTIVE-LOW DATA (FIGURE 2)
H	H	$A \leq B$	$A \geq B$
H	L	$A > B$	$A < B$
L	H	$A < B$	$A > B$
L	L	$A \geq B$	$A \leq B$

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

ALU SIGNAL DESIGNATIONS

The S54/N74LS181 can be used with the signal designations of either Figure 1 or Figure 2.

The logic functions and arithmetic operations obtained with signal designations as in Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-high data (Table 1)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	\bar{C}_n	\bar{C}_{n+4}	X	Y
Active-low data (Table 11)	\bar{A}_0	\bar{B}_0	\bar{A}_1	\bar{B}_1	\bar{A}_2	\bar{B}_2	\bar{A}_3	\bar{B}_3	\bar{F}_0	\bar{F}_1	\bar{F}_2	\bar{F}_3	C_n	C_{n+4}	\bar{P}	\bar{G}

TABLE 1

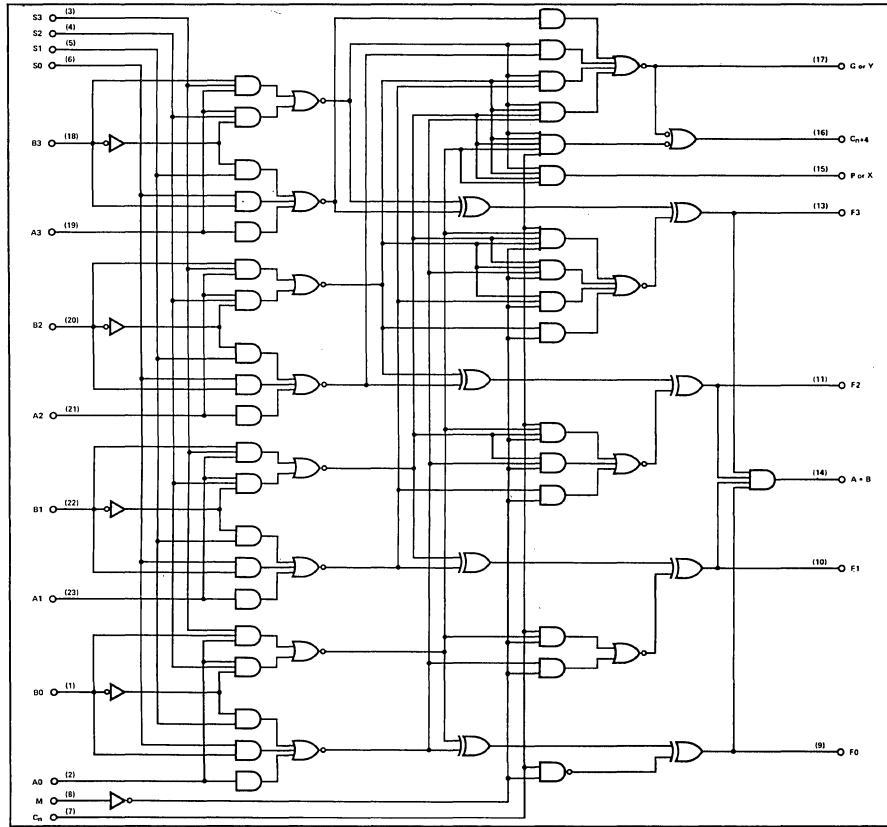
SELECTION				ACTIVE-HIGH DATA		
				M=H LOGIC FUNCTIONS	M=L: ARITHMETIC OPERATIONS	
S3	S2	S1	S0		C _n =H (NO CARRY)	C _n =L (WITH CARRY)
L	L	L	L	$F=\bar{A}$	$F=A$	$F=A \text{ PLUS } 1$
L	L	L	H	$F=\overline{A+B}$	$F=A+B$	$F=(A+B) \text{ PLUS } 1$
L	L	H	L	$F=\bar{A}B$	$F=A+\bar{B}$	$F=(A+\bar{B}) \text{ PLUS } 1$
L	L	H	H	$F=0$	$F=\text{MINUS } 1 \text{ (2's COMPL)}$	$F=\text{ZERO}$
L	H	L	L	$F=\overline{AB}$	$F=A \text{ PLUS } \bar{A}\bar{B}$	$F=A \text{ PLUS } \bar{A}\bar{B} \text{ PLUS } 1$
L	H	L	H	$F=\bar{B}$	$F=(A+B) \text{ PLUS } \bar{A}\bar{B}$	$F=(A+B) \text{ PLUS } \bar{A}\bar{B} \text{ PLUS } 1$
L	H	H	L	$F=A+B$	$F=A \text{ MINUS } B \text{ MINUS } 1$	$F=A \text{ MINUS } B$
L	H	H	H	$F=\overline{AB}$	$F=\bar{A}\bar{B} \text{ MINUS } 1$	$F=\bar{A}\bar{B}$
H	L	L	L	$F=\bar{A}+B$	$F=A \text{ PLUS } AB$	$F=A \text{ PLUS } AB \text{ PLUS } 1$
H	L	L	H	$F=\overline{A+B}$	$F=A \text{ PLUS } B$	$F=A \text{ PLUS } B \text{ PLUS } 1$
H	L	H	L	$F=B$	$F=(A+\bar{B}) \text{ PLUS } AB$	$F=(A+\bar{B}) \text{ PLUS } AB \text{ PLUS } 1$
H	L	H	H	$F=AB$	$F=AB \text{ MINUS } 1$	$F=AB$
H	H	L	L	$F=1$	$F=A \text{ PLUS } A^*$	$F=A \text{ PLUS } A \text{ PLUS } 1$
H	H	L	H	$F=A+\bar{B}$	$F=(A+B) \text{ PLUS } A$	$F=(A+B) \text{ PLUS } A \text{ PLUS } 1$
H	H	H	L	$F=A+B$	$F=(A+B) \text{ PLUS } A$	$F=(A+\bar{B}) \text{ PLUS } A \text{ PLUS } 1$
H	H	H	H	$F=A$	$F=A \text{ MINUS } 1$	$F=A$

* Each bit is shifted to the next more significant position.

TABLE 2

SELECTION				ACTIVE-HIGH DATA		
				M=H LOGIC FUNCTIONS	M=L: ARITHMETIC OPERATIONS	
S3	S2	S1	S0		C _n =L (NO CARRY)	C _n =H (WITH CARRY)
L	L	L	L	$F=\bar{A}$	$F=A \text{ MINUS } 1$	$F=A$
L	L	L	H	$F=\overline{AB}$	$F=AB \text{ MINUS } 1$	$F=AB$
L	L	H	L	$F=\bar{A}+B$	$F=\bar{A}\bar{B} \text{ MINUS } 1$	$F=\bar{A}\bar{B}$
L	L	H	H	$F=1$	$F=\text{MINUS } 1 \text{ (2's COMPL)}$	$F=\text{ZERO}$
L	H	L	L	$F=\overline{A+B}$	$F=A \text{ PLUS } (A+\bar{B})$	$F=A \text{ PLUS } (A+\bar{B}) \text{ PLUS } 1$
L	H	L	H	$F=\bar{B}$	$F=AB \text{ PLUS } (A+\bar{B})$	$F=AB \text{ PLUS } (A+\bar{B}) \text{ PLUS } 1$
L	H	H	L	$F=\overline{A+B}$	$F=A \text{ MINUS } B \text{ MINUS } 1$	$F=A \text{ MINUS } B$
L	H	H	H	$F=A+\bar{B}$	$F=A+\bar{B}$	$F=(A+\bar{B}) \text{ PLUS } 1$
H	L	L	L	$F=\bar{A}B$	$F=A \text{ PLUS } (A+B)$	$F=A \text{ PLUS } (A+B) \text{ PLUS } 1$
H	L	L	H	$F=A+B$	$F=A \text{ PLUS } B$	$F=A \text{ PLUS } B \text{ PLUS } 1$
H	L	H	L	$F=B$	$F=\bar{A}\bar{B} \text{ PLUS } (A+B)$	$F=\bar{A}\bar{B} \text{ PLUS } (A+B) \text{ PLUS } 1$
H	L	H	H	$F=A+B$	$F=A+B$	$F=(A+B) \text{ PLUS } 1$
H	H	L	L	$F=0$	$F=A \text{ PLUS } A^*$	$F=A \text{ PLUS } A \text{ PLUS } 1$
H	H	L	H	$F=\bar{A}\bar{B}$	$F=AB \text{ PLUS } A$	$F=AB \text{ PLUS } A \text{ PLUS } 1$
H	H	H	L	$F=AB$	$F=\bar{A}\bar{B} \text{ PLUS } A$	$F=\bar{A}\bar{B} \text{ PLUS } A \text{ PLUS } 1$
H	H	H	H	$F=A$	$F=A$	$F=A \text{ PLUS } 1$

FUNCTIONAL BLOCK DIAGRAM



SWITCHING CHARACTERISTICS $V_{CC}=5V, T_A=25^\circ C, C_L=15pF, R_L=2k\Omega$

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
t _{PLH} t _{PHL}	C _n	C _{n+4}			18 13	27 20	ns
t _{PLH} t _{PHL}	Any A or B	C _{n+4}	M=0V, S ₀ =S ₃ =4.5V, S ₁ =S ₂ =0V (SUM mode)		25 25	38 38	ns
t _{PLH} t _{PLH}	Any A or B	C _{n+4}	M=0V, S ₀ =S ₃ =0V S ₁ =S ₂ =4.5V (DIFF mode)		27 27	41 41	ns
t _{PLH} t _{PHL}	C _n	Any F	M=0V (SUM or DIFF mode)		17 13	26 20	ns
t _{PLH} t _{PHL}	Any A or B	G	M=0V, S ₀ =S ₃ =4.5V, S ₁ =S ₂ =0V (SUM mode)		19 15	29 23	ns
t _{PLH} t _{PHL}	Any A or B	G	M=0V, S ₀ =S ₃ =0V, S ₁ =S ₂ =4.5V (DIFF mode)		21 17	32 26	ns
t _{PLH} t _{PHL}	Any A or B	P	M=0V, S ₀ =S ₃ =4.5V, S ₁ =S ₂ =0V (SUM mode)		20 20	30 30	ns
t _{PLH} t _{PHL}	Any A or B	P	M=0V, S ₀ =S ₃ =0V, S ₁ =S ₂ =4.5V (DIFF mode)		20 22	30 33	ns
t _{PLH} t _{PHL}	A _i or B _i	F _i	M=0V, S ₀ =S ₃ =4.5V, S ₁ =S ₂ =0V (SUM mode)		21 13	32 20	ns
t _{PLH} t _{PHL}	A _i or B _i	F _i	M=0V, S ₀ =S ₃ =0V, S ₁ =S ₂ =4.5V DIFF mode)		21 15	32 23	ns
t _{PLH} t _{PHL}	A _i or B _i	F _i	M=4.5V (logic mode)		22 19	33 29	ns
t _{PLH} t _{PHL}	Any A or B	A=B	M=0V, S ₀ =S ₃ =0V, S ₁ =S ₂ =4.5V (DIFF mode)		33 41	50 62	ns

¹t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
Load circuit and typical waveforms are shown at front of book

DESCRIPTION

The 54/74LS190 is a synchronous, reversible up/down counter having a complexity of 58 equivalent gates. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

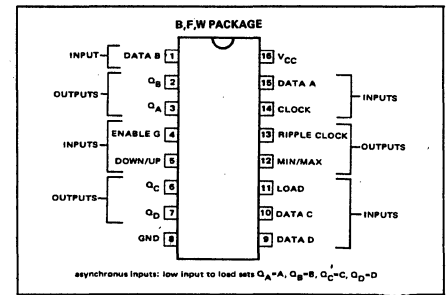
The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

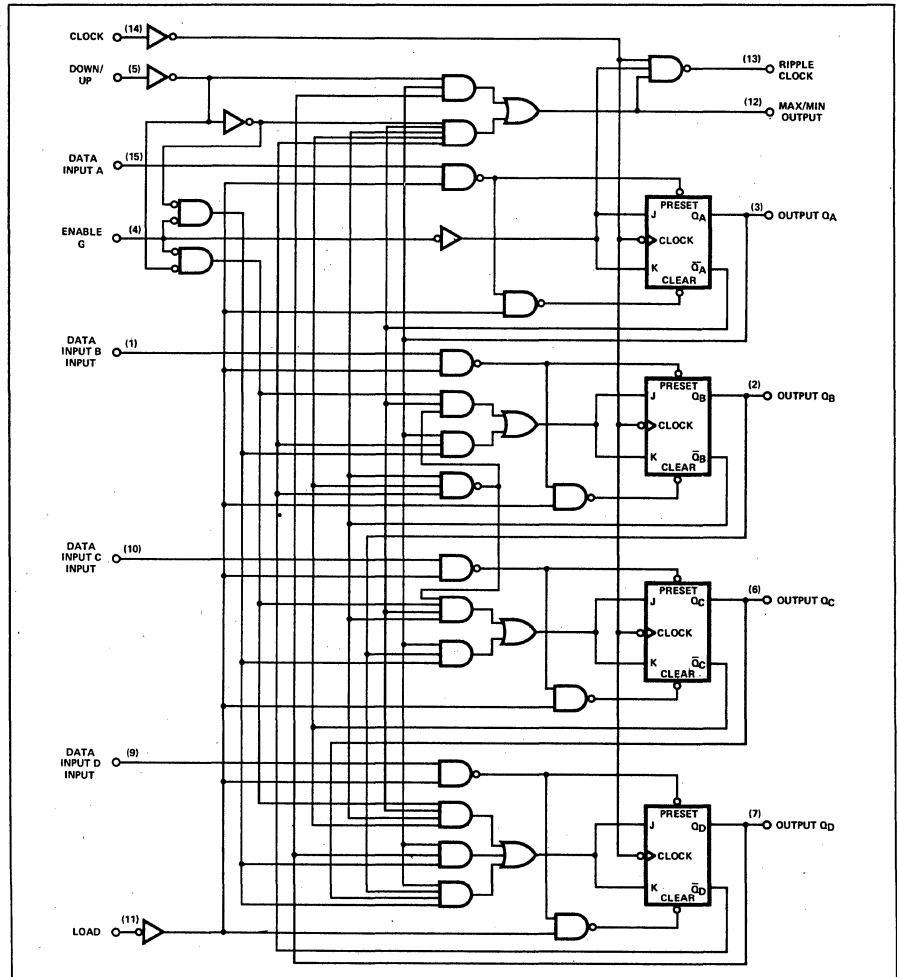
The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

PIN CONFIGURATION



BLOCK DIAGRAM



SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
f_{Clock}				20	25		MHz
$t_{w(Clock)}$	Width of clock input pulse			25			ns
$t_{w(Load)}$	Width of load input pulse			35			ns
t_{Setup}	Input setup time			20 \uparrow			ns
t_{Hold}	Input hold time			0 \uparrow			ns
t_{Enable}	Enable time to cycle			20 \uparrow			
t_{PLH}	Load	Q_A, Q_B, Q_C, Q_D	$C_L = 15pF, R_L = 2k\Omega,$ See Figures 1 and 3 thru 7		22	33	ns
t_{PHL}					33	50	
t_{PLH}	Data A,B,C,D	Q_A, Q_B, Q_C, Q_D			14	22	ns
t_{PHL}					35	50	
t_{PLH}	Clock	Ripple clock			13	20	ns
t_{PHL}					16	24	
t_{PLH}	Clock	Q_A, Q_B, Q_C, Q_D			16	24	ns
t_{PHL}					24	36	
t_{PLH}	Clock	Max/min			28	42	ns
t_{PHL}					37	52	
t_{PLH}	Down/up	Ripple clock			30	45	ns
t_{PHL}					30	45	
t_{PLH}	Down/up	Max/min			21	33	ns
t_{PHL}					22	33	
t_{PLH}	Enable E	Ripple clock		21	33	ns	
t_{PHL}				22	33	ns	

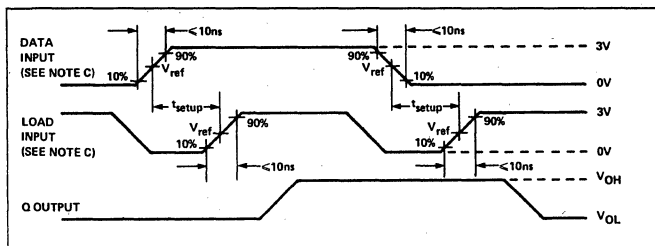
* f_{max} = maximum clock frequency
 t_{PLH} = propagation delay time, low-to-high level output
 t_{PHL} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION

TYPICAL LOAD, COUNT, AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.

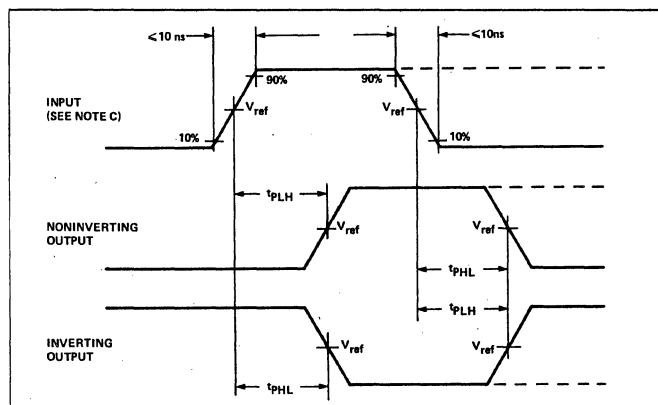


VOLTAGE WAVEFORMS

FIGURE 1 — DATA SETUP TIME VOLTAGE WAVEFORMS

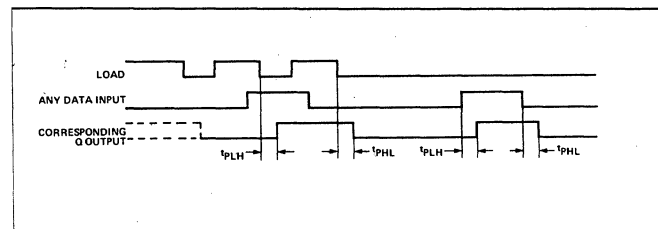
NOTES:

- C_i includes probe and jig capacitance.
- All diodes are 1N3064.
- The input pulses are supplied by generators having the following characteristics: $Z_{out} = 50 \Omega$, duty cycle $\leq 50\%$, $PRR \leq 1 \text{ MHz}$.
- $V_{ref} = 1.3V$.



See waveform sequences in figures 3 through 6 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in figures 3 through 6.

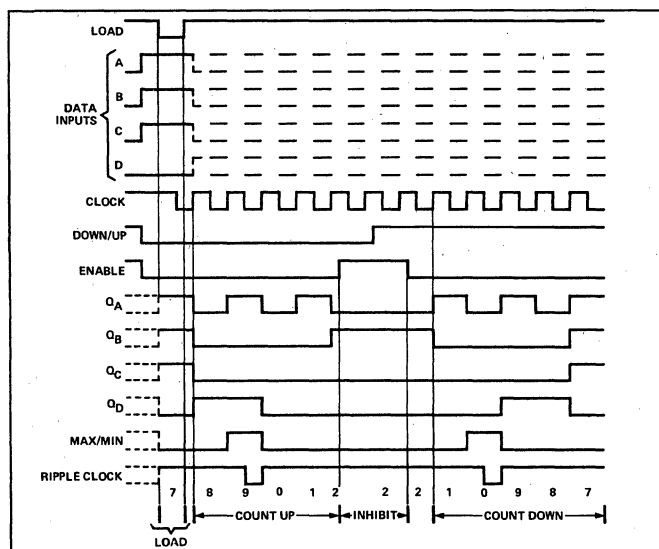
FIGURE 2 — GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES



NOTE:

E. Conditions on other inputs are irrelevant.

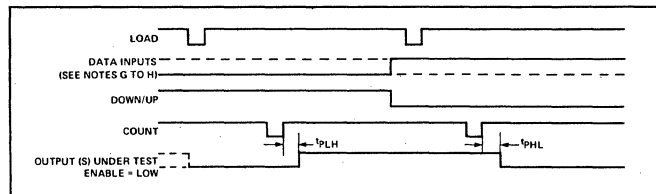
FIGURE 3 — LOAD TO OUTPUT AND DATA TO OUTPUT



NOTE:

F. All data inputs are low.

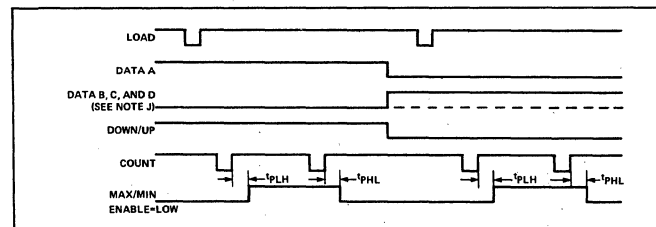
FIGURE 4 — ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO RIPPLE CLOCK, AND DOWN/UP TO MAX/MIN



NOTES:

- To test Q_A , Q_B , and Q_C outputs: Data inputs A, B, and C are shown by the solid line. Data input D is shown by the dashed line.
- To test Q_D output: Data inputs A and D are shown by the solid line. Data inputs B and C are held at the low logic level.

FIGURE 5 — CLOCK TO OUTPUT



NOTE:

J. Data inputs B and C are shown by the dashed line. Data input D is shown by the solid line.

FIGURE 6 — CLOCK TO MAX/MIN

SYNCHRONOUS BINARY UP/DOWN COUNTER

54/74LS191

54LS191-F.W • 74LS191-B.F

DESCRIPTION

The 54/74LS191 is a synchronous, reversible binary up/down counter having a complexity of 58 equivalent gates. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

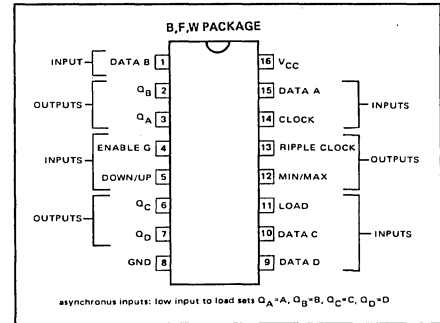
The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulu-N dividers by simply modifying the count length with the preset inputs.

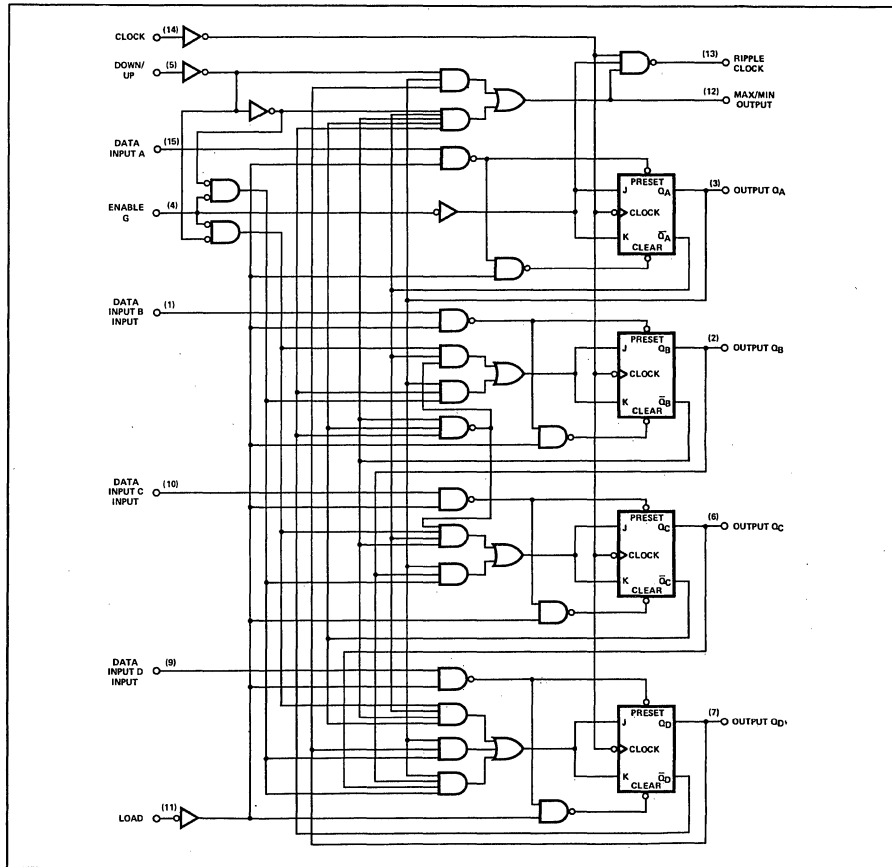
The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

PIN CONFIGURATION



BLOCK DIAGRAM



SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
f_{Clock}				20	25		MHz
$t_{w(Clock)}$ Width of clock input pulse				25			ns
$t_{(Load)}$ Width of load input pulse				35			ns
t_{setup} Input setup time				20†			ns
t_{Hold} Input hold time				0†			ns
t_{Enable} Enable time to cycle				20†			
t_{PLH}	Load	Q_A, Q_B, Q_C, Q_D			22	33	ns
t_{PHL}					33	50	
t_{PLH}	Data A,B,C,D	Q_A, Q_B, Q_C, Q_D			14	22	ns
t_{PHL}					35	50	
t_{PLH}	Clock	Ripple clock	$C_L = 15pF, R_L = 2k\Omega,$ See Figures 1 and 3 thru 7		13	20	ns
t_{PHL}						16	24
t_{PLH}	Clock	Q_A, Q_B, Q_C, Q_D			16	24	ns
t_{PHL}					24	36	
t_{PLH}	Clock	Max/min			28	42	ns
t_{PHL}					37	52	
t_{PLH}	Down/up	Ripple clock			30	45	ns
t_{PHL}					30	45	
t_{PLH}	Down/up	Max/min			21	33	ns
t_{PHL}					22	33	
t_{PLH}	Enable	Ripple clock			21	32	ns
t_{PHL}	E				22	33	ns

* f_{max} = maximum clock frequency
 t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION

TYPICAL LOAD, COUNT, AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.

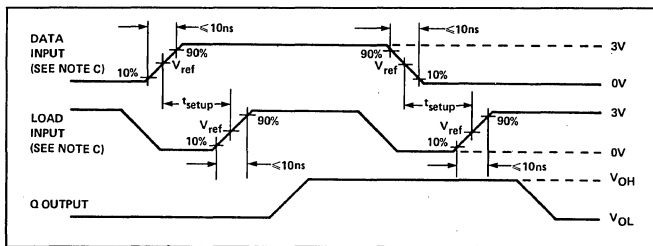
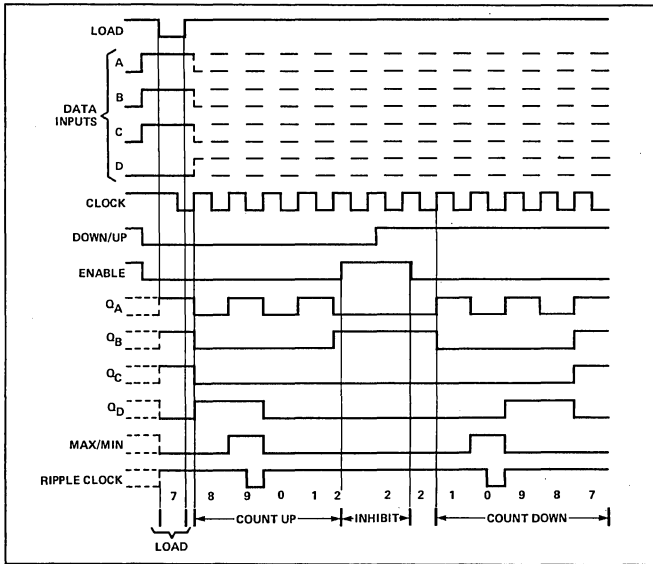
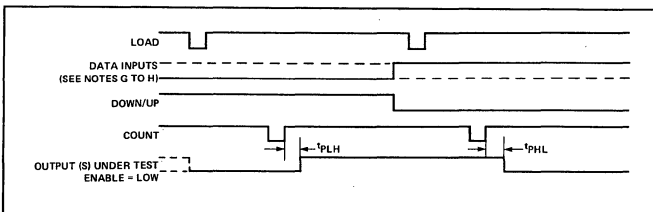


FIGURE 1 — DATA SETUP TIME VOLTAGE WAVEFORMS

NOTES:

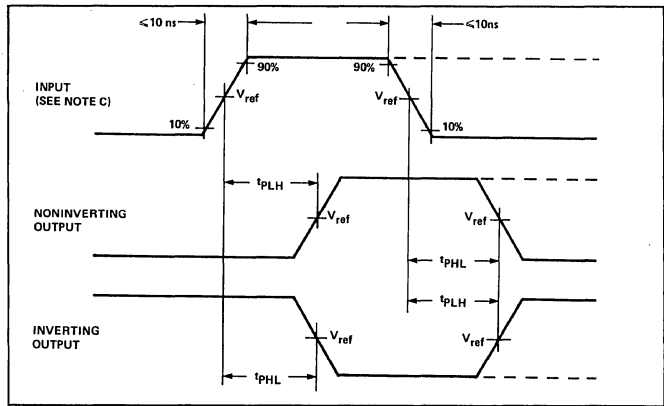
- A. C_L includes probe and jig capacitance.
- B. All diodes are 1N3064.
- C. The input pulses are supplied by generators having the following characteristics: $Z_{out} = 50 \Omega$, duty cycle $\le 50\%$, PRR ≤ 1 MHz.
- D. $V_{ref} = 1.3$ V.



NOTE:

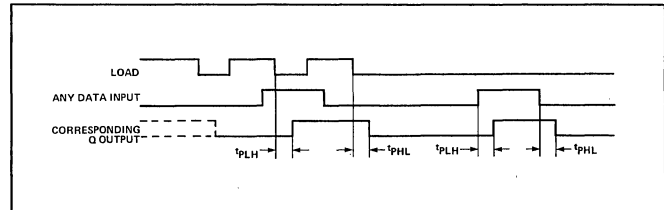
G. To test Q_A , Q_B , Q_C , and Q_D outputs: All four data inputs are shown by the solid line.

FIGURE 5 — CLOCK TO OUTPUT



See waveform sequences in figures 4 through 7 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in figures 4 through 7.

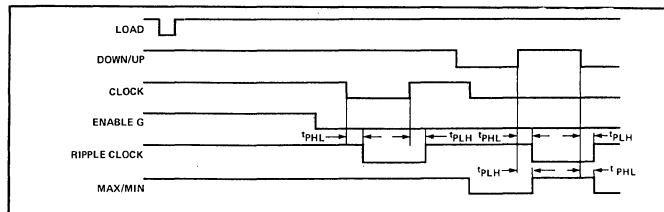
FIGURE 2 — GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES



NOTE:

E. Conditions on other inputs are irrelevant.

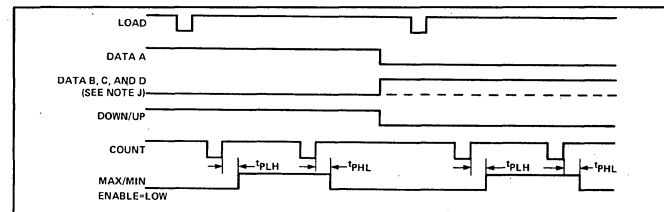
FIGURE 3 — LOAD TO OUTPUT AND DATA TO OUTPUT



NOTE:

F. All data inputs are low.

FIGURE 4 — ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO RIPPLE CLOCK, AND DOWN/UP TO MAX/MIN



NOTE:

H. Data inputs B and C are shown by the dashed line for the '191 and 'LS190 and the solid line for the '191 and 'LS191: Data input D is shown by the solid line for both devices.

FIGURE 6 — CLOCK TO MAX/MIN

SYNCHRONOUS DECADE UP/DOWN COUNTER

54/74LS192

54LS192-F,W • 74LS192-B,F

DESCRIPTION

This monolithic circuit is a synchronous reversible (up/down) counter having a complexity of 55 equivalent gates. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

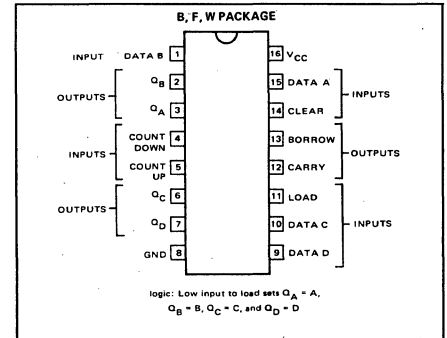
The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count inputs is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

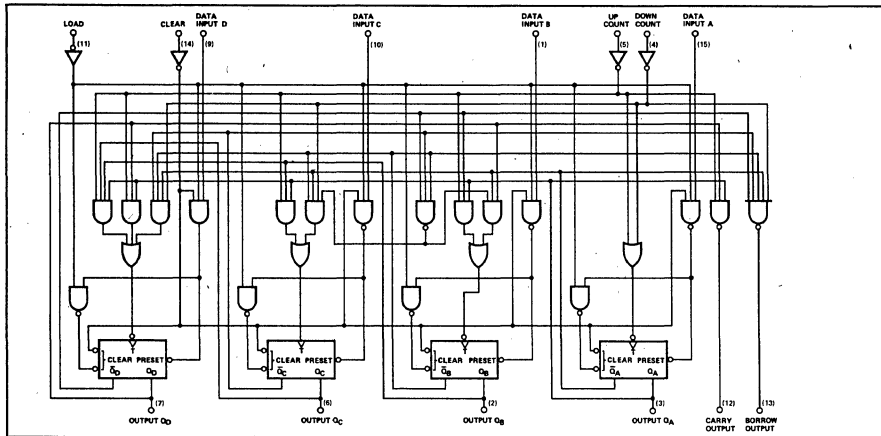
A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

PIN CONFIGURATION



BLOCK DIAGRAM



TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

Illustrated below is the following sequence:

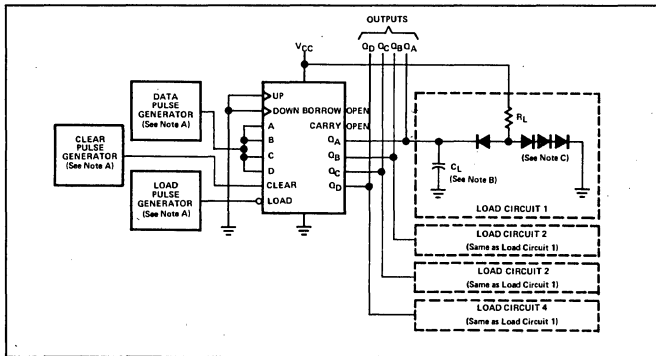
1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
f_{Count}				25	32		MHz
t_w Input pulse width				20			ns
t_{setup} Input setup time				20†			ns
t_{hold} Input hold time				0†			ns
t_{PLH}	Count-up	Carry	$C_L = 15pf,$ $R_L = 2k\Omega,$ See Figures 1 and 2		17	26	ns
t_{PHL}	Count-up	Carry			16	24	ns
t_{PLH}	Count-down	Borrow			16	24	ns
t_{PHL}	Count-down	Borrow			16	24	ns
t_{PLH}	Either count	Q		25	38		ns
t_{PHL}	Either count	Q		31	47		ns
t_{PLH}	Load	Q		27	40		ns
t_{PHL}	Load	Q		29	40		ns
t_{PLH}	Clear	Q		22	35		ns
t_{PHL}	Clear	Q					ns

* f_{max} = maximum clock frequency
 t_{PLH} = propagation delay time, low-to-high level output
 t_{PHL} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION

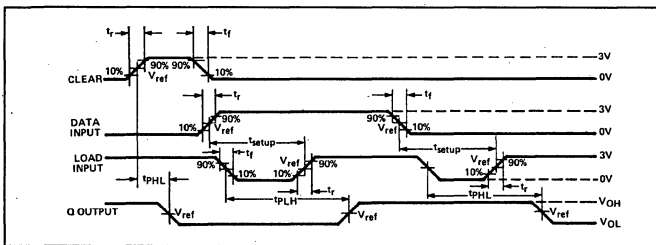


TEST CIRCUIT

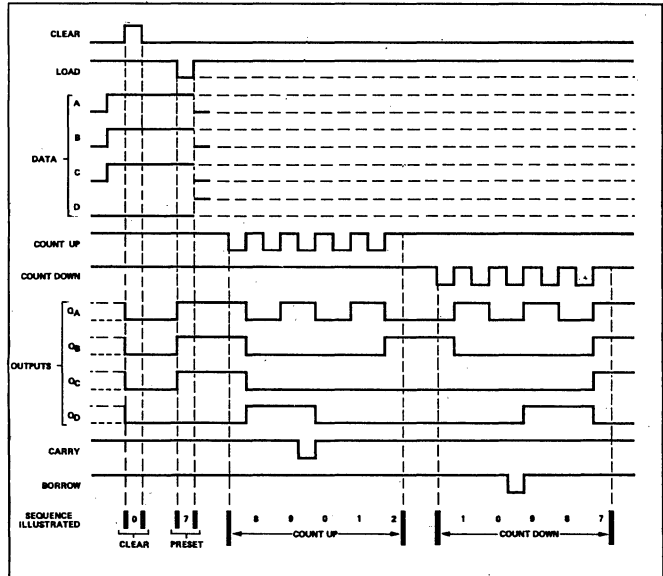
NOTES:

- A. The pulse generators have the following characteristics: $Z_{out} \approx 50 \Omega$, and for the data pulse generator $PRR \leq 500$ kHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR , duty cycle = 50%.
- B. C_L includes probe and jig capacitance.
- C. Diodes are 1N3064.
- D. t_r and $t_f \leq 7$ ns
- E. V_{ref} is 1.3 volts

FIGURE 1—CLEAR, SETUP, AND LOAD TIMES



VOLTAGE WAVEFORMS



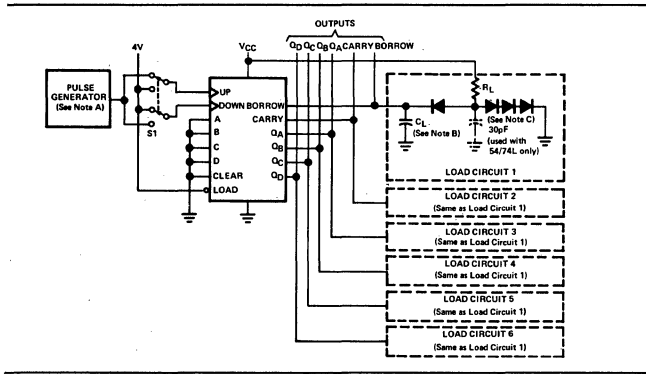
NOTES:

- A. Clear overrides load, data, and count inputs.
- B. When counting up, count-down input must be high; when counting down, count-up input must be high.

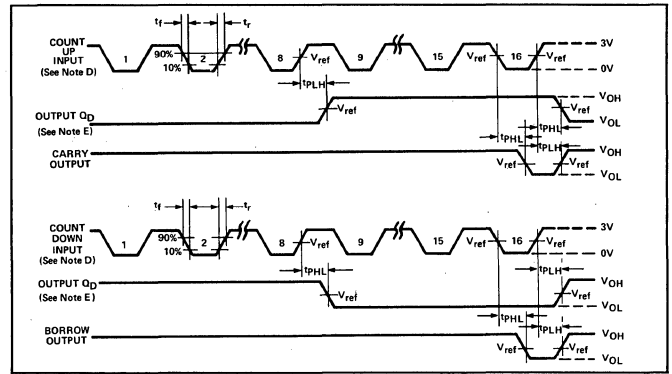
SYNCHRONOUS DECADE UP/DOWN COUNTER

54/74LS192

54LS192-F, W • 74LS192-B, F



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

- A. The pulse generator has the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_{out} \approx 50 \Omega$, duty cycle = 50%.
- B. C_L includes probe and jig capacitance.
- C. Diodes are 1N3064
- D. Count cycle is 1 through 10.
- E. Waveforms for outputs Q_A , Q_B , and Q_C are omitted to simplify the drawing.
- F. t_r and $t_f \leq 7 \text{ ns}$
- G. V_{ref} is 1.3 volts

FIGURE 2—PROPAGATION DELAY TIMES

SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER

54/74LS193

54LS193-F, W • 74LS193-B, F

DESCRIPTION

This monolithic circuit is a synchronous reversible (up/down) counter having a complexity of 55 equivalent gates. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

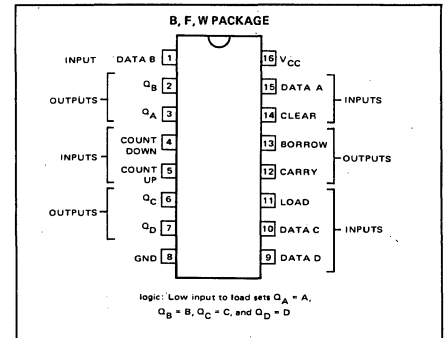
The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count inputs is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

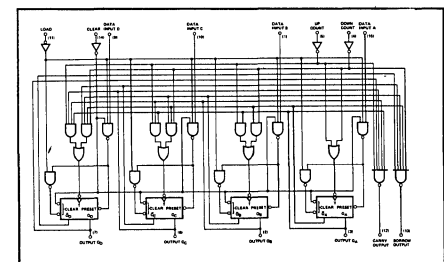
A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

PIN CONFIGURATION



BLOCK DIAGRAM



SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

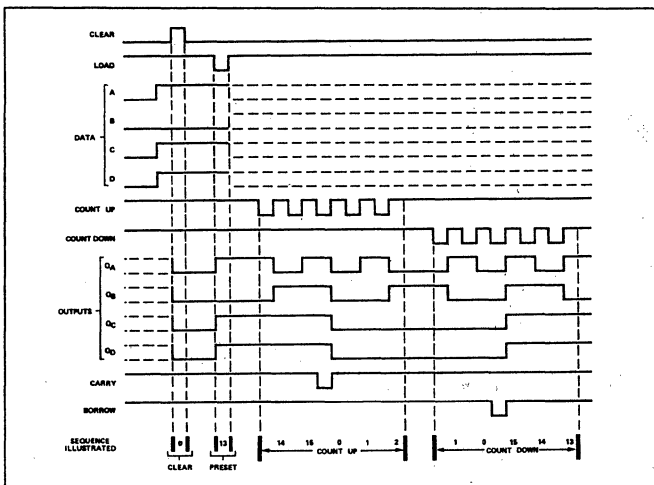
PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
f_{Count}				25	32		MHz
t_w Input pulse width				20			ns
t_{Set-up} Input setup time				20↑			ns
t_{Hold} Input hold time				0↑			ns
t_{PLH}	Count-up	Carry	$C_L = 15pF,$ $R_L = 2k\Omega,$ See Figures 1 and 2		17	26	ns
t_{PHL}					16	24	
t_{PLH}	Count-down	Borrow			16	24	ns
t_{PHL}					16	24	
t_{PLH}	Either count	Q			25	38	ns
t_{PHL}					31	47	
t_{PLH}	Load	Q			27	40	ns
t_{PHL}					29	40	
t_{PHL}	Clear	Q			22	35	ns

* f_{max} = maximum clock frequency
 t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



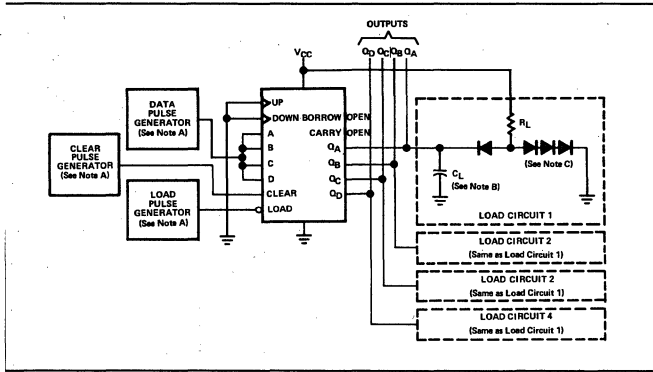
NOTES:
 A. Clear overrides load, data, and count inputs.
 B. When counting up, count-down input must be high; when counting down, count-up input must be high.

SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER

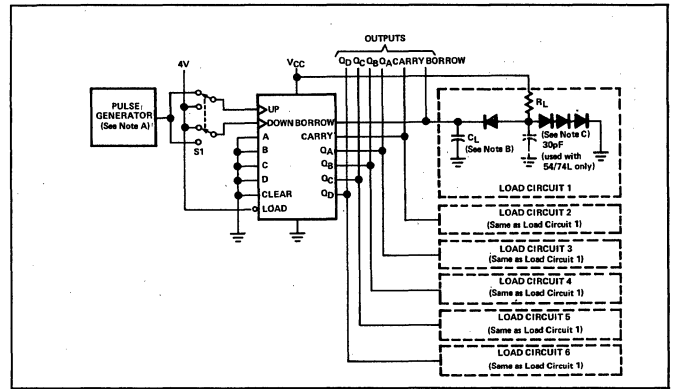
54/74LS193

54LS193-F,W • 74LS193-B,F

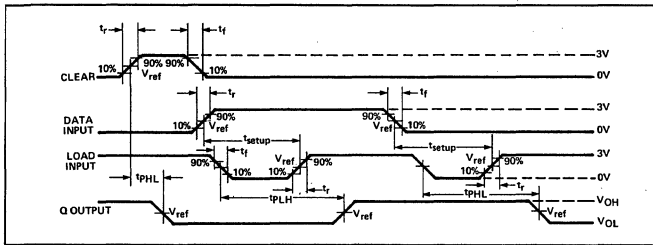
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



TEST CIRCUIT

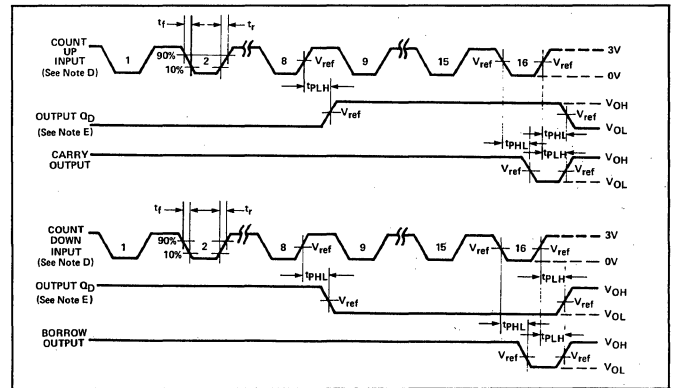


VOLTAGE WAVEFORMS

NOTES:

- A. The pulse generators have the following characteristics: $Z_{out} \approx 50 \Omega$ and for the data pulse generator PRR ≤ 500 kHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR, duty cycle = 50%.
- B. C_L includes probe and jig capacitance.
- C. Diodes are 1N3064
- D. t_r and $t_f \leq 7$ ns
- E. V_{ref} is 1.3 volts

FIGURE 1—CLEAR, SETUP, AND LOAD TIMES



VOLTAGE WAVEFORMS

NOTES:

- A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50 \Omega$, duty cycle = 50%.
- B. C_L includes probe and jig capacitance.
- C. Diodes are 1N3064
- D. Waveforms for outputs Qa, Qb, and Qc are omitted to simplify the drawing.
- E. t_r and $t_f \leq 7$ ns
- F. V_{ref} is 1.3 volts

FIGURE 2—PROPAGATION DELAY TIMES

DESCRIPTION

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 45 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

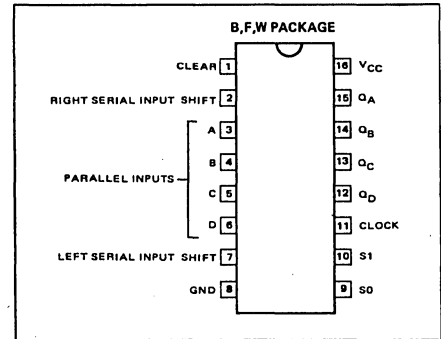
- Parallel (broadside) load
- Shift right (in the direction Q_A toward Q_D)
- Shift left (in the direction Q_D toward Q_A)
- Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S_0 and S_1 , high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift-right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls of the S54-194/N74-194 should be changed only while the clock input is high.

PIN CONFIGURATION

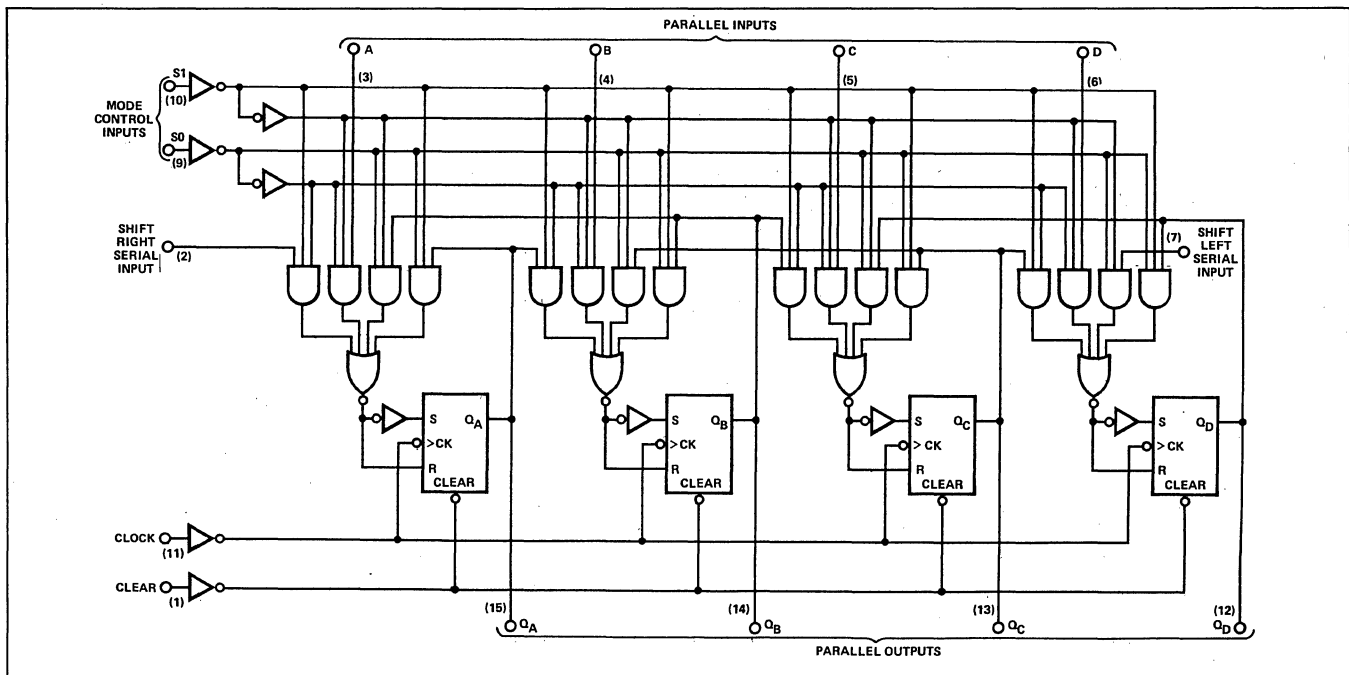


H = high level (steady state)
 L = low level (steady state)
 X = irrelevant (any input, including transitions)
 † = transition from low to high level
 a, b, c, d = the level of steady state input at inputs A, B, C, or D, respectively
 $Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}$ = the level of $Q_A, Q_B, Q_C,$ or Q_D , respectively, before the indicated steady state input conditions were established
 $Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn}$ = the level of $Q_A, Q_B, Q_C,$ respectively, before the most recent † transition of the clock

FUNCTION TABLE

CLEAR	MODE		CLOCK	INPUTS		SERIAL				PARALLEL				OUTPUTS			
	S1	S0		LEFT	RIGHT	A	B	C	D	Q_A	Q_B	Q_C	Q_D	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	X	X	X	X	X	X	X	X	L	L	L	L	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	†	X	X	a	b	c	d	a	b	c	d	a	b	c	d
H	L	H	†	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	L	H	†	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	H	L	†	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	†	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

BLOCK DIAGRAM

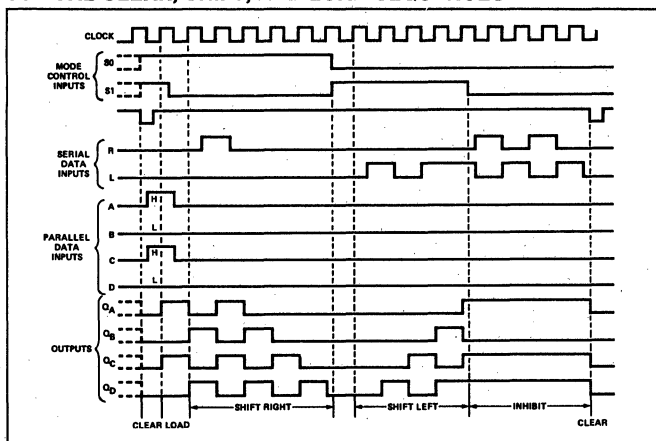


SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency	25	36		MHz
t_w	Width of clock or clear pulse	20			ns
t_{Setup}	Input setup time Mode control Serial & parallel data Clear inactive-state	30↑ 20↑ 25↑			ns
t_{Hold}	Input hold time	0↑			ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear		19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		17	22	ns

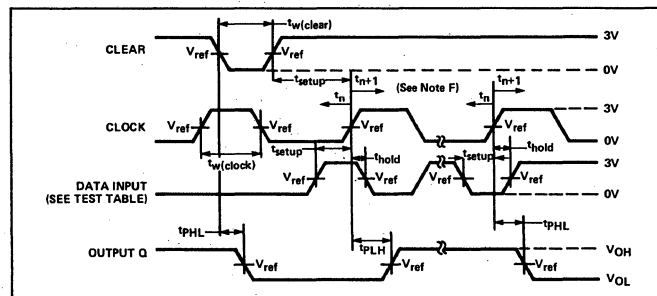
PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, SHIFT, AND LOAD SEQUENCES



TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S1	S0	OUTPUT TESTED (SEE NOTE E)
A	4.5V	4.5V	Q_A at t_{n+1}
B	4.5V	4.5V	Q_B at t_{n+1}
C	4.5V	4.5V	Q_C at t_{n+1}
D	4.5V	4.5V	Q_D at t_{n+1}
L Serial Input	4.5V	0V	Q_A at t_{n+4}
R Serial Input	0V	4.5V	Q_D at t_{n+4}



VOLTAGE WAVEFORMS

NOTES:

- The clock pulse generator has the following characteristics; $Z_{out} \approx 50 \Omega$ and $PRR \leq MHz$, $t_r \leq 15 ns$ and $t_f \leq 6 ns$. When testing t_{max} , vary PRR.
- C_L includes probe and jig capacitance.
- All diodes are 1N3064 or 1N916.
- A clear pulse is applied prior to each test.
- $V_{ref} = 1.3V$.
- Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1} . Proper shifting of data is verified at t_{n+4} with a functional test.
- t_n = bit time before clocking transition.
 t_{n+1} = bit time after one clocking transition.
 t_{n+4} = bit time after four clocking transitions.

FIGURE 1—SWITCHING TIMES

54LS195A-F,W • 74LS195A-B,F

DESCRIPTION

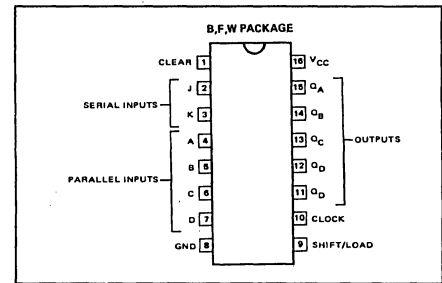
This 4-bit register features parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

- Parallel (Broadside) Load
- Shift (In direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the function table.

PIN CONFIGURATION

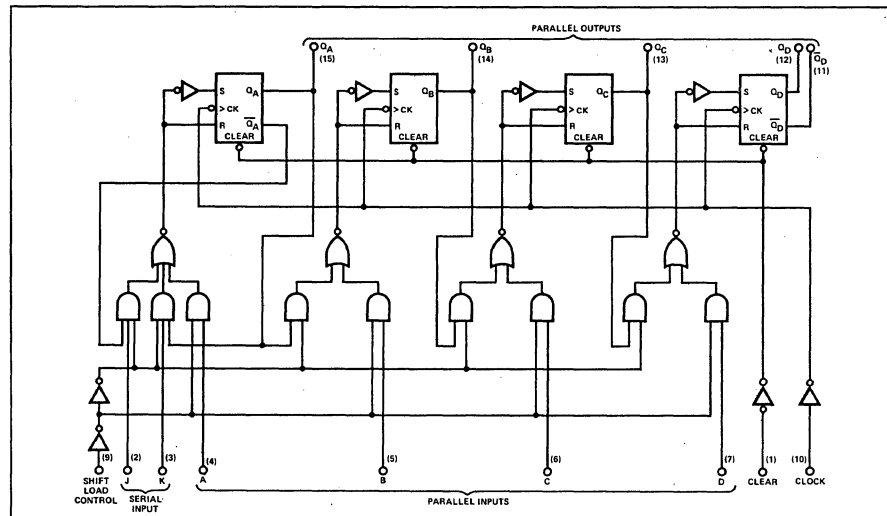


FUNCTION TABLE

CLEAR	SHIFT/LOAD	CLOCK	INPUTS				OUTPUTS							
			SERIAL		PARALLEL		Q_A	Q_B	Q_C	Q_D	\bar{Q}_D			
			J	\bar{K}	A	B	C	D						
L	X	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	\uparrow	X	X	a	b	c	d		a	b	c	d	\bar{d}
H	H	L	X	X	X	X	X	X		Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	\bar{Q}_{D0}
H	H	\uparrow	L	H	X	X	X	X		Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
H	H	\uparrow	L	L	X	X	X	X		L	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
H	H	\uparrow	H	H	X	X	X	X		H	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
H	H	\uparrow	H	L	X	X	X	X		\bar{Q}_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}

H = high level (steady state)
 L = low level (steady state)
 X = irrelevant (any input, including transitions)
 \uparrow = transition from low to high level
 a,b,c,d = the level of steady-state input at A,B,C, or D, respectively
 $Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0}$ = the level of $Q_A, Q_B, Q_C,$ or Q_D respectively, before the indicated steady-state input conditions were established
 Q_{An}, Q_{Bn}, Q_{Cn} = the level of $Q_A, Q_B,$ or Q_C , respectively, before the most recent transition of the clock

FUNCTIONAL BLOCK DIAGRAM

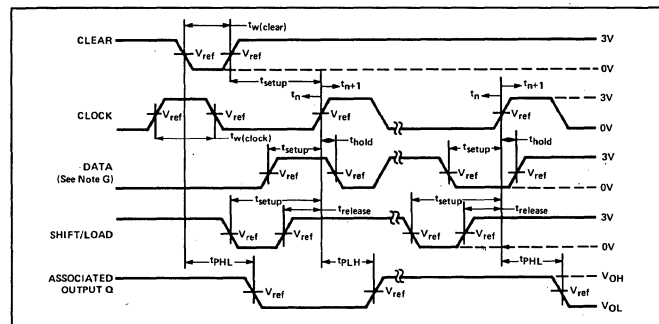
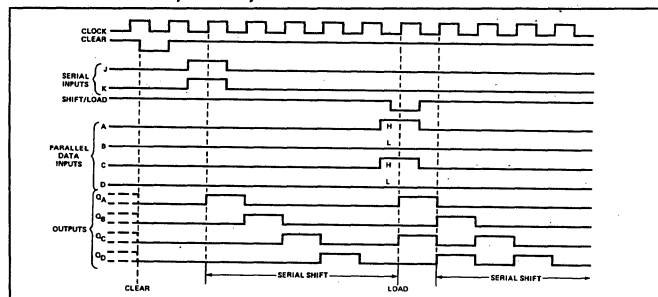


SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
f_{Clock} Clock frequency		20	28		MHz
$t_{w(Clock)}$ Width of clock input pulse		16			ns
$t_{w(Clear)}$ Width of clear input pulse		12			ns
t_{setup} Input setup time					
Shift/Load		25↑			
Serial and parallel data		15↑			ns
Clear inactive-state		25↑			
$t_{Release}$ Shift/load release time	$C_L = 15pF, R_L = 2k\Omega,$			10↑	ns
t_{Hold} Serial and parallel data hold time		0↑			ns
t_{PHL} Propagation delay time, high-to-low-level output from clear			31	47	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			19	29	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			23	35	ns

PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, SHIFT, AND LOAD SEQUENCES



VOLTAGE WAVEFORMS

NOTES:

- The clock pulse generator has the following characteristics: $Z_{out} \approx 50 \Omega$ and $PRR \leq 1 \text{ MHz}$
 $t_r \leq 15 \text{ ns}$ and $t_f \leq 6 \text{ ns}$. When testing t_{max} , vary the clock PRR.
- C_L includes probe and jig capacitance.
- All diodes are 1N3064.
- A clear pulse is applied prior to each test.
- $V_{ref} = 1.3V$.
- Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1} . Proper shifting of data is verified at t_{n+4} with a functional test.
- J and K inputs are tested the same as data A, B, C, and D inputs except that shift/load input remains high.
- t_n = bit time before clocking transition.
 t_{n+1} = bit time after one clocking transition.
 t_{n+4} = bit time after four clocking transitions.

FIGURE 1—SWITCHING TIMES

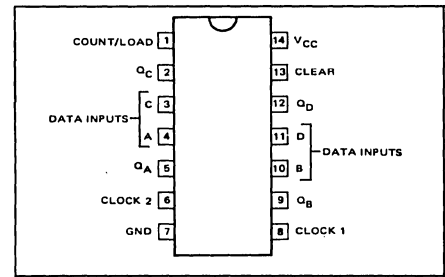
DESCRIPTION

This high-speed monolithic counter consists of four DC coupled, master-slave flip-flops which are internally interconnected to provide a divide-by-two and a divide-by-five counter S54/N74LS196. This counter is fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. This counter features a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

This counter may also be used as a 4-bit latch by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

PIN CONFIGURATION



SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

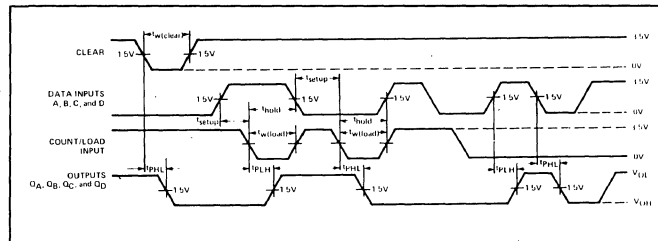
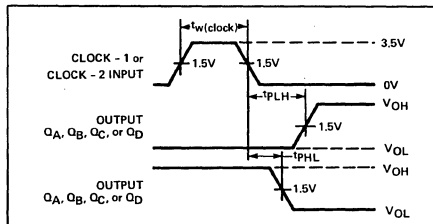
PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
f_{Clock}	Clock 1 Clock 2	Q _A Q _A		30 15	40		MHz
t_w	Input pulse-width			20 30			ns
t_{Hold}	Input hold time			15 20			
t_{Setup}	Input setup time					$t_w(Load) \downarrow$ $t_w(Load) \downarrow$	
t_{Enable} (Note 3)	Count enable time		$C_L = 15pF$ $R_L = 2k\Omega$	10 15 20			ns ns ns
t_{PLH}					8	15	
t_{PHL}	Clock 1	Q _A			13	20	ns
t_{PLH}					16	24	
t_{PHL}	Clock 2	Q _B			22	33	ns
t_{PLH}					38	57	
t_{PHL}	Clock 2	Q _C			41	62	ns
t_{PLH}					12	18	
t_{PHL}	Clock 2	Q _D			30	45	ns
t_{PLH}					20	30	
t_{PHL}	A,B,C,D	Q _A , Q _B , Q _C , Q _D			29	44	ns
t_{PLH}					27	41	
t_{PHL}	Load	Any			30	45	ns
t_{PHL}	Clear	Any			34	51	ns

¹ f_{max} = maximum input count frequency
 t_{PLH} = propagation delay time, low-to-high-level output, t_{PHL} = propagation delay time, high-to-low-level output.

NOTE:

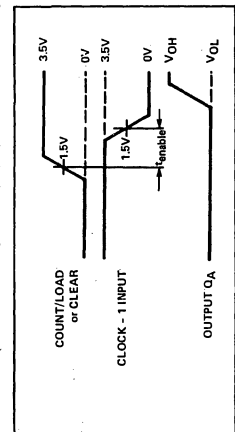
3. Count enable time is the internal immediately preceding the negative - going edge of the clock pulse during which internal the count/load and clear inputs must be high to ensure counting.

PARAMETER MEASUREMENT INFORMATION



CLEAR AND LOAD VOLTAGE WAVEFORMS

FIGURE 1



CLOCK ENABLE TIME VOLTAGE WAVEFORMS

NOTES:

- A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $t_r <$ 5 ns, and unless specified, $t_f <$ 5 ns. When testing t_{max} , vary PRR.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064.
- D. Unless otherwise specified, Q_A is connected to clock 2.



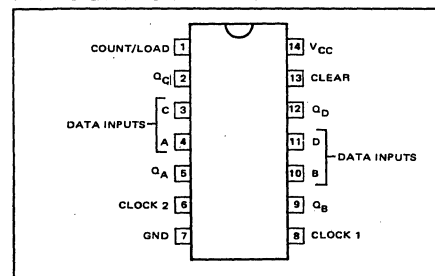
DESCRIPTION

This high-speed monolithic counter consists of four DC coupled, master-slave flip-flops which are internally interconnected to provide a divide-by-two and a divide-by-eight counter S54/N74LS197. These four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

PIN CONFIGURATION

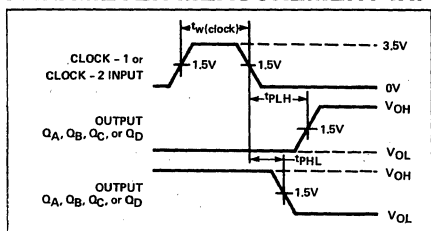


SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

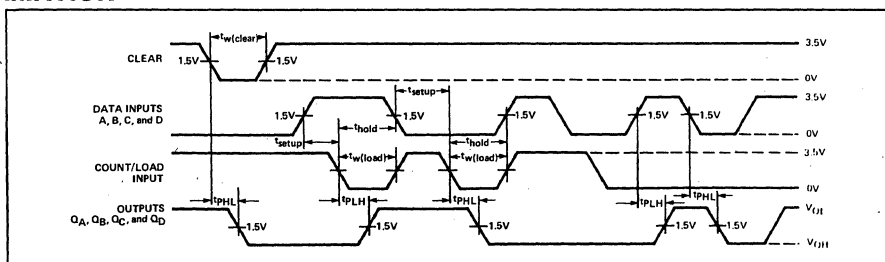
PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
f_{Count}	Clock 1	QA	$C_L = 15pF$ $R_L = 2k\Omega$	30	40		MHz
	Clock 2	QA		15			
t_{PLH}	Clock 1	QA			8	15	ns
t_{PHL}					14	21	
t_{PLH}	Clock 2	QB			12	19	ns
t_{PHL}					23	35	
t_{PLH}	Clock 2	QC			34	51	ns
t_{PHL}					42	63	
t_{PLH}	Clock 2	QD			55	78	ns
t_{PHL}					63	95	
t_{PLH}	A,B,C,D	QA, QB, QC, QD			18	27	ns
t_{PHL}					29	44	
t_{PLH}	Load	Any		26	39	ns	
t_{PHL}				30	45		
t_{PHL}	Clear	Any		34	51	ns	

¹ f_{max} = maximum input count frequency
 t_{PLH} = propagation delay time, low-to-high-level output, t_{PHL} = propagation delay time, high-to-low-level output.

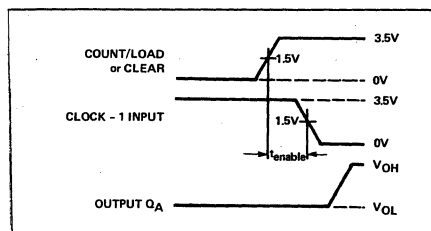
PARAMETER MEASUREMENT INFORMATION



CLOCK MODE



CLEAR AND LOAD



CLOCK ENABLE



DESCRIPTION

The 54/74LS221 is a monolithic dual multivibrator which features a negative-transition-triggered input either of which can be used as an inhibit input. Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2V. A high immunity to Vcc noise of typically 1.5V is also provided by internal latching circuitry.

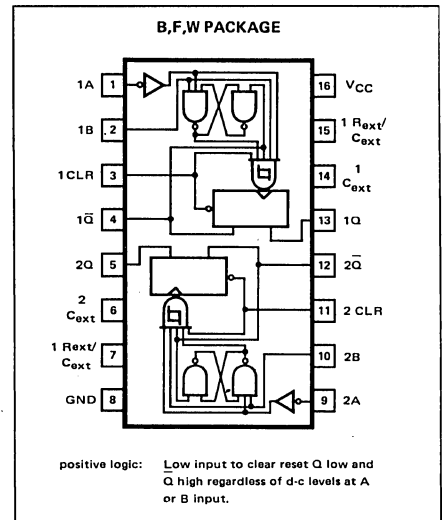
Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulse can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35ns to 49s (54LS221) or 70s (74LS221) by choosing appropriate timing components. With $R_{ext} = 2k\Omega$ and $C_{ext} = 0$, an output pulse of typically 30ns is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are illustrated as a part of the switching characteristics waveforms.

Pulse width stability is achieved through internal compensation and is virtually independent of Vcc and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and Vcc ranges for more than six decades of timing capacitance (10pF to 10μF) and more than one decade of timing resistance (2kΩ to 70kΩ for the 54LS221, and 2kΩ to 100kΩ for the 74LS221). Throughout these ranges, pulse width is defined by the relationship: $t_w(out) = C_{ext}R_{ext}$. In 20.7 $C_{ext}R_{ext}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000μF and timing resistance as low as 1.4k may be used. Also, the range of jitter-free output pulse widths is extended if Vcc is held to 5V and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R₁. High duty cycles are available if a certain amount pulse width jitter is allowed. The variance in output pulse width from device to device is typically less than ±0.5% for given external timing components.

Pin assignments for this device are identical to those of the 54LS123/74LS123 so that the 54/74LS221 can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext}.

54LS221-F,W • 74LS221-B,F
PIN CONFIGURATION

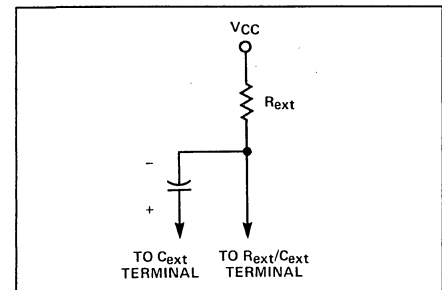


FUNCTION TABLE
(EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q-bar
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	↓	H		

Also see description and switching characteristics

- H = high level (steady state)
- L = low level (steady state)
- ↑ = transition from low to high level
- ↓ = transition from high to low level
- = one high level pulse
- = one low level pulse
- X = irrelevant



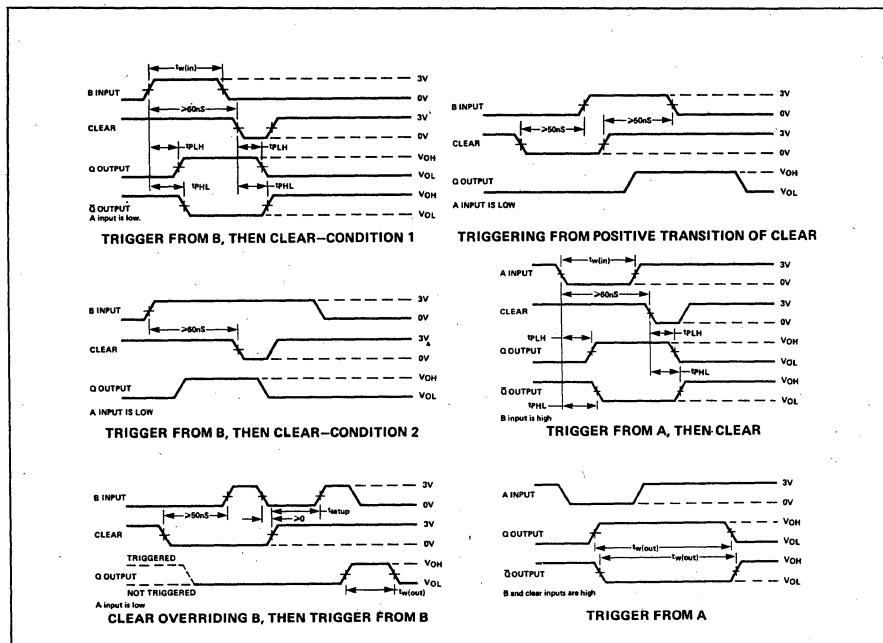
TIMING COMPONENT CONNECTIONS

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
dv/dt			$C_{ext} = 80pF, R_{ext} = 2k\Omega$	1			V/s
				1			V/ μs
$t_{w(in)}$				40			ns
$t_{w(out)}$	A or B	Q or \bar{Q}	$C_{ext} = 80pF, R_{ext} = 2k\Omega$	70	120	150	ns
			$C_{ext} = 0, R_{ext} = 2k\Omega$	20	47	70	ns
			$C_{ext} = 100pF, R_{ext} = 10k\Omega$	600	670	750	ns
			$C_{ext} = 1\mu F, R_{ext} = 10k\Omega$	6.0	6.7	7.5	ns
$t_{w(Clear)}$			$C_L = 15pF, R_L = 2k\Omega$	40			ns
t_{Setup}			See Figure 1	15 \uparrow			ns
R_{ext}			and Note 3	1.4		70	K Ω
				1.4		100	K Ω
C_{ext}				0		1000	μF
						67	%
						90	%
t_{PLH}	A	Q		45	70		ns
	B	Q		35	55		ns
t_{PHL}	A	\bar{Q}		50	80		ns
	B	\bar{Q}		40	65		ns
t_{PHL}	Clear	Q				55	ns
t_{PLH}	Clear	\bar{Q}				65	ns

* t_{PLH} = Propagation delay time, low-to-high-level output
 t_{PHL} = Propagation delay time, high-to-low-level output
 $t_{w(out)}$ = Output pulse width

PARAMETER MEASUREMENT INFORMATION



NOTES:

- A. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50 \Omega$; $t_r \leq 15$ ns, $t_f \leq 6$ ns.
- B. All measurements are made between the 1.3V points of the indicated transitions

FIGURE 1—SWITCHING CHARACTERISTICS

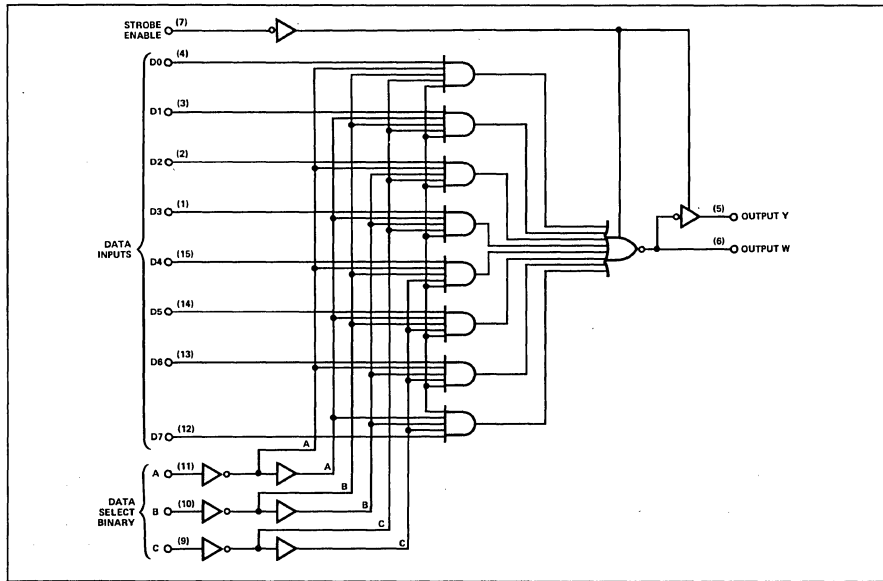


DESCRIPTION

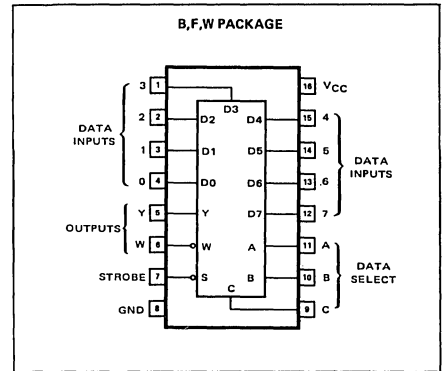
These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources and feature a strobe-controlled three-state output. The strobe must be at a low logic level to enable these devices. The three-state outputs permit up to 49 54LS251 and 129 74LS251 outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



FUNCTION TABLE¹

INPUTS				OUTPUTS	
SELECT			STROBE S	Y	W
C	B	A			
X	X	X	H	Z	Z
L	L	L	L	D0	D0
L	L	H	L	D1	D1
L	H	L	L	D2	D2
L	H	H	L	D3	D3
H	L	L	L	D4	D4
H	L	H	L	D5	D5
H	H	L	L	D6	D6
H	H	H	L	D7	D7

H = high logic level, L = low logic level
 X = irrelevant, Z = high impedance (off)
 D0, D1 . . . D7 = the level of the respective D input

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS				
				MIN	TYP	MAX	UNIT	
t_{PLH} t_{PHL}	A, B, or C (4 levels)	Y	$C_L = 15pF$ $R_L = 2k\Omega$		29	45	ns	
t_{PLH} t_{PHL}	A, B, or C (3 levels)	W			20	33	ns	
t_{PLH} t_{PHL}	Any D	Y			17	28	ns	
t_{PLH} t_{PHL}	Any D	W			18	28	ns	
t_{PLH} t_{PHL}	Strobe	Y			10	15	ns	
t_{PLH} t_{PHL}	Strobe	W			9	15	ns	
t_{ZH} t_{ZL}	Strobe	Y			17	45	ns	
t_{ZH} t_{ZL}	Strobe	W			26	40	ns	
t_{ZH} t_{ZL}	Strobe	Y			17	27	ns	
t_{ZH} t_{ZL}	Strobe	W			24	40	ns	
t_{HZ} t_{LZ}	Strobe	Y		$C_L = 5pF$ $R_L = 2k\Omega$		30	45	ns
t_{HZ} t_{LZ}	Strobe	W				15	25	ns

¹ t_{PLH} = Propagation delay time low-to-high-level output
 t_{PHL} = Propagation delay time, high-to-low-level output
 t_{ZH} = Output enable time to high level
 t_{ZL} = Output enable time to low level

t_{HZ} = Output disable time from high level
 t_{LZ} = Output disable time from low level
 Load circuit and waveforms are shown at front of book.

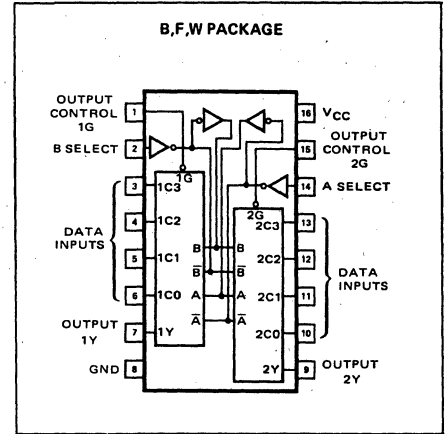


DESCRIPTION

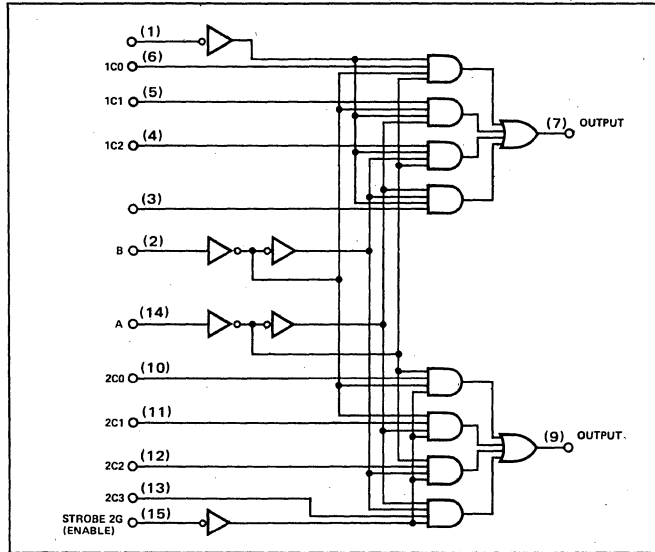
Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H ¹	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level. L = low level. X = irrelevant. Z = high impedance (off)

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	$C_L = 15pF, R_L = 2k\Omega$		11	25	ns
t_{PHL}					13	20	
t_{PLH}	Select	Y			20	45	ns
t_{PHL}					21	32	
t_{ZH}	Output	Y			11	23	ns
t_{ZL}	Control	Y			15	23	
t_{HZ}	Output	Y	$C_L = 5pF, R_L = 2k\Omega$		27	41	ns
t_{LZ}				Control		12	

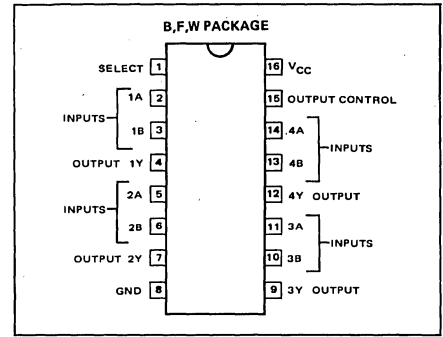
¹ t_{PLH} = Propagation delay time, low-to-high-level output
 t_{PHL} = Propagation delay time, high-to-low-level output
 t_{ZH} = Output enable time to high level
 t_{ZL} = Output enable time to low level
 t_{HZ} = Output disable time from high level
 t_{LZ} = Output disable time from low level
 Load circuit and typical waveforms are shown at the front of book.

DESCRIPTION

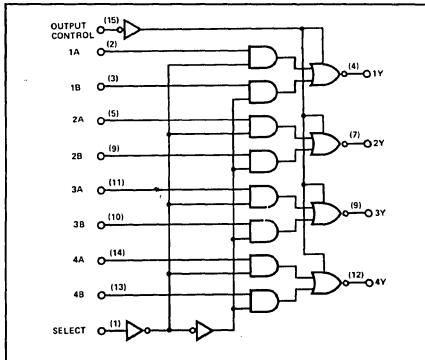
This Schottky-clamped high-performance multiplexer features three-state outputs that can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output-enable circuitry is designed such that the output disable times are shorter than the output enable times.

This three-state output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

OUTPUT CONTROL	INPUTS		OUTPUT Y		'LS257 'S257	'LS258 'S258
	SELECT	A	B			
H	X	X	X	Z	Z	Z
L	L	L	X	L	H	H
L	L	H	X	H	L	L
L	H	X	L	L	H	H
L	H	X	H	H	L	L

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			UNIT	
				MIN	TYP	MAX		
t_{PLH}	Data	Any	$C_L = 15pF$		12	18	ns	
t_{PHL}					14	21		
t_{PLH}	Select	Any			20	30	ns	
t_{PHL}					20	30		
t_{ZH}	Output	Any		$C_L = 5pF$		14	30	ns
t_{ZL}						14	35	
t_{HZ}	Control	Any					ns	
t_{LZ}								

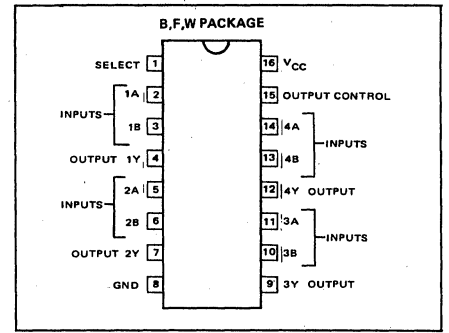
* t_{PLH} = Propagation delay time, low-to-high-level output
 t_{PHL} = Propagation delay time, high-to-low-level output
 t_{ZH} = Output enable time to high level
 t_{ZL} = Output enable time to low level
 t_{HZ} = Output disable time from high level
 t_{LZ} = Output disable time from low level
 Load circuits and waveforms are shown at the front of the book.

DESCRIPTION

This Schottky-clamped high-performance multiplexer features three-state outputs that can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output-enable circuitry is designed such that the output disable times are shorter than the output enable times.

This three-state output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

PIN CONFIGURATION



SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
t_{PLH}	Data	Any	$C_L = 15pF$		12	18	ns
t_{PHL}					12	18	
t_{PLH}	Select	Any			14	21	ns
t_{PHL}					14	21	
t_{ZH}	Output	Any			20	30	ns
t_{ZL}					20	30	
t_{HZ}	Output Control	Any	$C_L = 5pF$		14	20	ns
t_{LZ}					14	21	

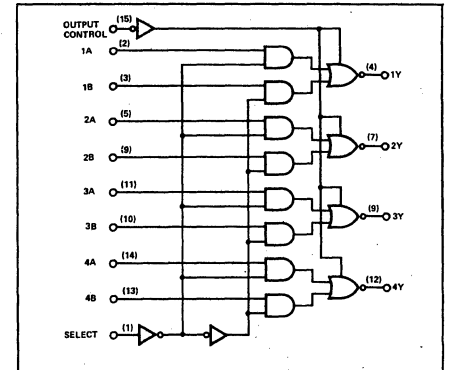
* t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output
 t_{ZH} = output enable time-to-high-level
 t_{ZL} = output enable time-to-low-level
 t_{HZ} = output disable time-from-high-level
 t_{LZ} = output disable time-from-low-level
 Load circuits and waveforms are shown at the front of the book.

FUNCTION TABLE

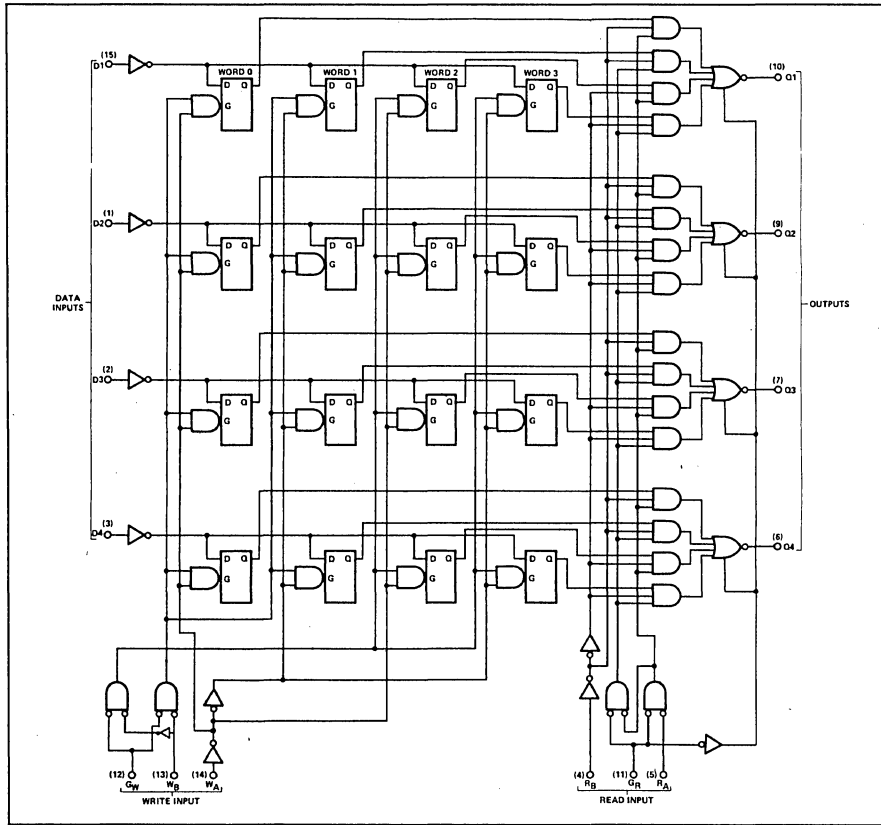
INPUTS		OUTPUT Y		
OUTPUT CONTROL	SELECT	A	B	
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

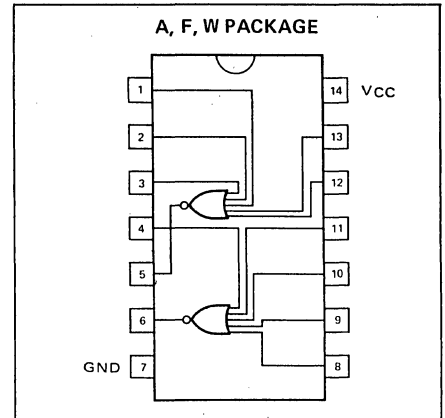
BLOCK DIAGRAM



BLOCK DIAGRAM



PIN CONFIGURATION



SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15pF, R_L = 2k\Omega$		10	15	ns
t_{PHL} Propagation delay time, high-to-low-level output			10	15	ns

DESCRIPTION

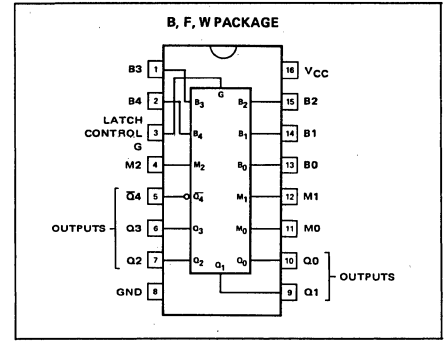
These low-power Schottky circuits are designed to be used in parallel multiplication applications. They perform binary multiplication in two's-complement form, two bits at a time.

The M inputs are for the multiplier bits and the B inputs are for the multiplicand. The Q outputs represent the partial product as a recoded base-4 number. This recoding effectively reduces the Wallace-tree hardware requirements by a factor of two.

The outputs represent partial products in one's-complement form generated as a result of multiplication. A simple rounding scheme using two additional gates is needed for each partial product to generate two's complement.

The leading (most significant) bit of the product is inverted for ease in extending the sign to square (left justify) the partial-product bits.

PIN CONFIGURATION

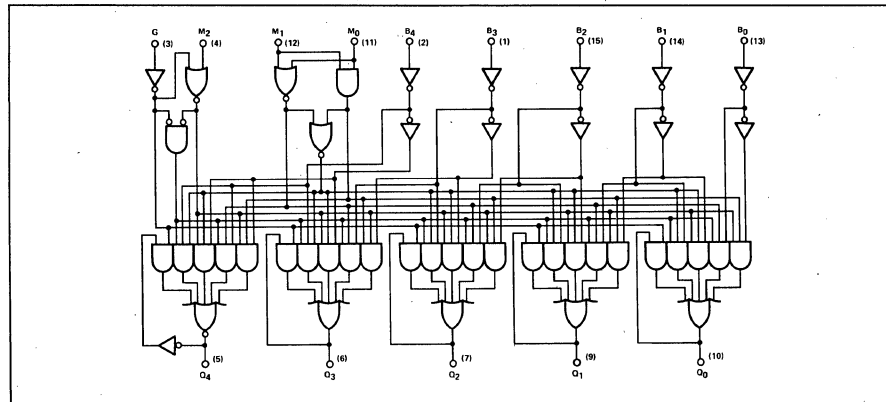


FUNCTION TABLE

INPUTS				OUTPUTS				
LATCH CONTROL G	MULTIPLIER			\bar{Q}_4	Q3	Q2	Q1	Q0
	M2	M1	M0					
	L	X	X					
H	L	L	L	\bar{H}	L	L	L	L
H	L	L	H	\bar{B}_4	B4	B3	B2	B1
H	L	H	L	\bar{B}_4	B4	B3	B2	B1
H	L	H	H	\bar{B}_4	\bar{B}_3	\bar{B}_2	\bar{B}_1	\bar{B}_0
H	H	L	L	B4	\bar{B}_3	\bar{B}_2	\bar{B}_1	\bar{B}_0
H	H	L	H	B4	B4	\bar{B}_3	\bar{B}_2	\bar{B}_1
H	H	H	L	B4	\bar{B}_4	B3	\bar{B}_2	\bar{B}_1
H	H	H	H	H	L	L	L	L

H = high level, L = low level, X = irrelevant
 $Q_{4_0} \dots Q_{0_0}$ = The logic level of the same output before the high-to-low- transition of G.
 $B_4 \dots B_0$ = The logic level of the indicated multiplicand (b) input.

BLOCK DIAGRAM



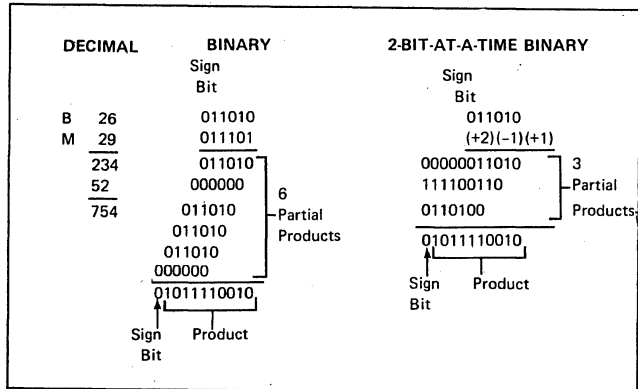
SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
t_w	Width of enable pulse			25			ns
t_{setup}	Input setup time	Any M input	Q	17↓			ns
		Any B input	Q	15↓			ns
t_{Hold}	Input hold time	Any M input	Q	0↓			ns
		Any B input	Q	0↓			ns
t_{PLH}	Propagation delay time Low-to-high-level output	Enable G	Any Q		22	35	ns
t_{PHL}	Propagation delay time High-to-low-level output	Enable G	Any Q		20	30	ns
t_{PLH}	Propagation delay time Low-to-high-level output	Any M input	Any Q		25	40	ns
t_{PHL}	Propagation delay time High-to-low-level output	Any M input	Any Q		22	35	ns
t_{PLH}	Propagation delay time Low-to-high-level output	Any B input	Any Q		27	42	ns
t_{PHL}	Propagation delay time High-to-low-level output	Any B input	Any Q		24	37	ns

Load circuit and waveforms are shown at the front of book.

TYPICAL APPLICATION DATA

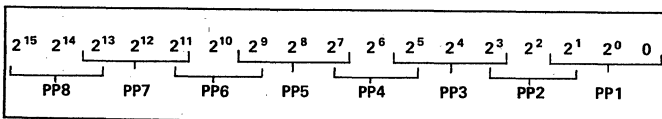
Multiplication of the numbers 26 (multiplicand) by 29 (multiplier) in decimal, binary, and 2-bit-at-a-time-binary is shown here:



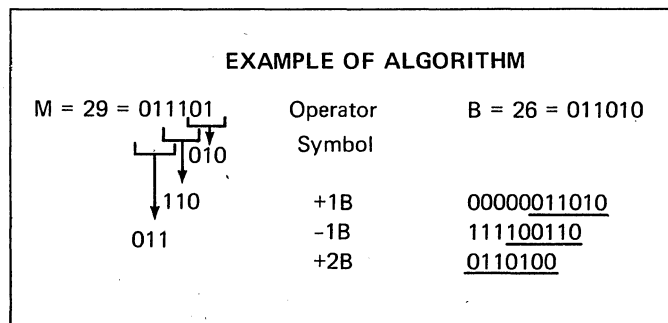
Two points should be noted in the 2-bit-at-a-time-binary example above. First, in positioning the partial products beneath each other for final addition, each partial product is shifted two places to the left of the partial products above it instead of one place as is done in regular multiplication. Second, the msb of the partial product (the sign bit) is extended to the sign-bit column of the final answer. A substantial reduction of multiplication time, cost, and power is obtained by implementing a parallel partial-product-generation scheme using a 2-bit-at-a-time algorithm, followed by a Wallace Tree summation.

Partial-product-generation rules of the algorithm are:

1. Examine two bits of multiplier M plus the next lower bit. For the first partial product (PP1) the next lower bit is zero.



2. Generate partial product (PPi) as shown in the following table:
3. Weight the partial products by indexing each two places left relative to the next-less-significant product.
4. Extend the most-significant bit of the partial product to the sign-bit place value of the final product.



The summation of these partial products was shown in the 2-bit-at-a-time binary multiplication example above.

The 54/74LS261 generates partial products according to this algorithm with two exceptions:

1. The one's complement is generated for the cases requiring the two's complement. The two's complement can be obtained by adding one to the one's complement; this rounding can be done by using one NAND gate and one AND gate as shown in Figure B.
2. The most-significant bit is complemented to reduce the hardware required to extend the sign bit. This extension can be accomplished by adding a hard-wired logic 1 in bit position 2^{2i+15} of each partial product and also in bit position 2^{16} of the first partial product (PP1).

MULTIPLIER BITS FROM STEP 1			OPERATOR SYMBOL	TO OBTAIN PARTIAL PRODUCT
2^{2i-1}	2^{2i-2}	2^{2i-3}		
0	0	0	0	Replace multiplicand by zero
0	0	1	+1B	Copy multiplicand
0	1	0	+1B	Copy multiplicand
0	1	1	+2B	Shift multiplicand left one bit
1	0	0	-2B	Shift two's complement of multiplicand left one bit
1	0	1	-1B	Replace multiplicand by two's complement
1	1	0	-1B	Replace multiplicand by two's complement
1	1	1	0	Replace multiplicand by zero

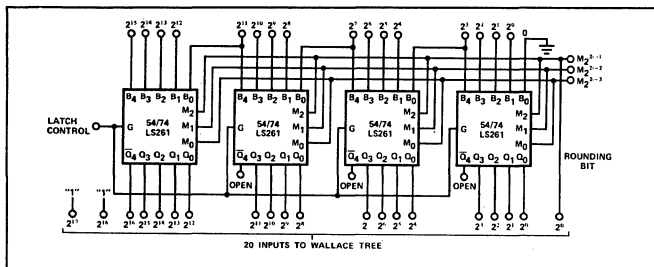


FIGURE A—FIRST PARTIAL PRODUCT, PP1

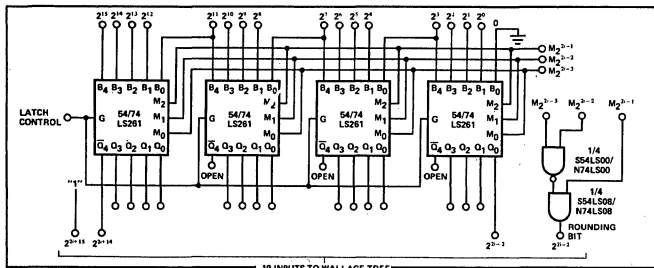


FIGURE B—OTHER PARTIAL PRODUCTS, PPI

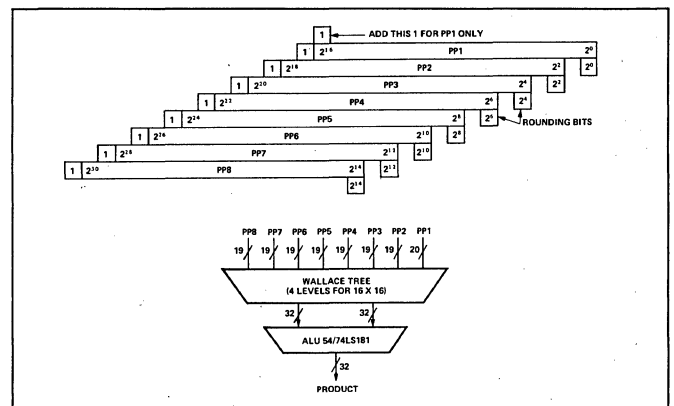


FIGURE C — MANIPULATION OF PARTIAL PRODUCTS FOR ENTRY INTO WALLACE TREE

In general, the 4 x 2 bit 54/74LS261 can be expanded for use in 4m x 2n bit multipliers. Partial-product generation uses m x n 54/74LS261s, m x n ÷ 16 54/74LS00s, and m x n ÷ 16 54/74LS08s. The size of the Wallace Tree and ALU requirements vary depending on the size of the problem. The count for the 16 x 16 bit multiplier is:

- 32 S54LS261/N74LS261
- 2 S54LS00/N74LS00
- 2 S54LS08/N74LS08
- 56 54H183/74H183*
- 7 S54LS181/N74LS181
- 2 S54LS182/N74LS182*

*Not currently available from Signetics.

QUAD 2-INPUT EXCLUSIVE-NOR GATE W/OPEN COLLECTOR OUTPUTS 54/74LS266

54LS266-F,W • 74LS266-A,F

DESCRIPTION

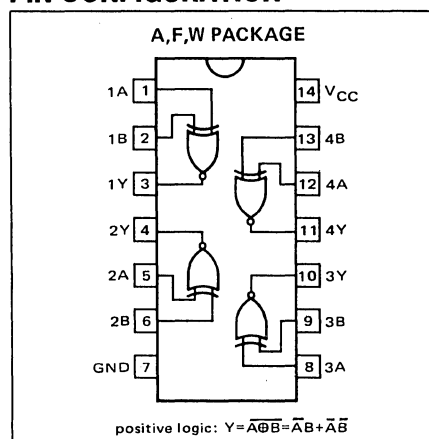
The 54/74LS266 is comprised of four independent 2-input exclusive-NOR gates with open-collector outputs. The open-collector outputs permit tying outputs together for multiple-bit comparisons.

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER*	FROM (INPUT)	TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	A or B	Other input low $C_L = 15pF,$ $R_L = 2k\Omega$		18	30	ns
t_{PLH} t_{PHL}	A or B	Other input high		18	30	ns

* t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output
 Load circuit and waveforms are shown at the front of the book.

PIN CONFIGURATION



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

H = high level, L = low level

4-BIT BINARY ADDER

54/74LS283

54LS283-F,W • 74LS283-B,F

DESCRIPTION

This improved full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. This adder features full internal look ahead across all four bits generating the carry term in ten nanoseconds typically. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

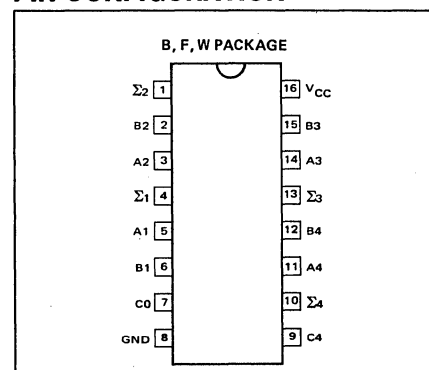
The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

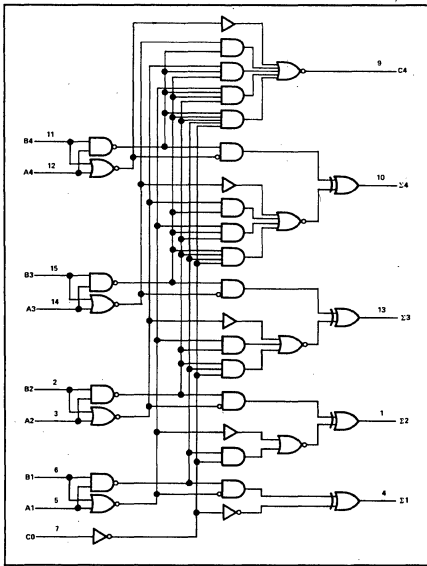
PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	C_0	Any Σ			16	24	ns
t_{PLH} t_{PHL}	A_i or B_i	Σ_i	$C_L = 15pF,$ $R_L = 2k\Omega$		15	24	ns
t_{PLH} t_{PHL}	C_0	C_4			11	17	ns
t_{PLH} t_{PHL}	A_i or B_i	C_4			11	22	ns

* t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output
 Load circuit and waveforms are shown at the front of the book.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

INPUT				OUTPUT						
				WHEN CO = L			WHEN CO = H			
				WHEN C2 = L			WHEN C2 = H			
A1 A3	B2 B3	A2 A4	B2 B4	Σ1 Σ3	Σ2 Σ4	C2 C4	Σ1 Σ3	Σ2 Σ4	C2 C4	
L	L	L	L	L	L	L	H	L	L	
H	L	L	L	H	L	L	L	H	L	
L	H	L	L	H	L	L	L	H	L	
H	H	L	L	L	H	L	H	H	L	
L	L	H	L	L	H	L	L	H	L	
H	L	H	L	H	H	L	L	L	H	
L	H	H	L	H	H	L	L	L	H	
H	H	H	L	L	L	H	H	L	H	
L	L	L	H	L	H	L	H	H	L	
H	L	L	H	H	H	L	L	L	H	
L	H	L	H	H	H	L	L	L	H	
H	H	L	H	L	L	H	H	L	H	
L	L	H	H	L	L	H	H	L	H	
H	L	H	H	H	L	H	L	H	H	
L	H	H	H	H	L	H	L	H	H	
H	H	H	H	L	H	H	H	H	H	

H = high level, L = low level

NOTE: Input conditions at A1, B1, A, B2, and CO are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4, are then used to determine outputs Σ3, Σ4, and C4.

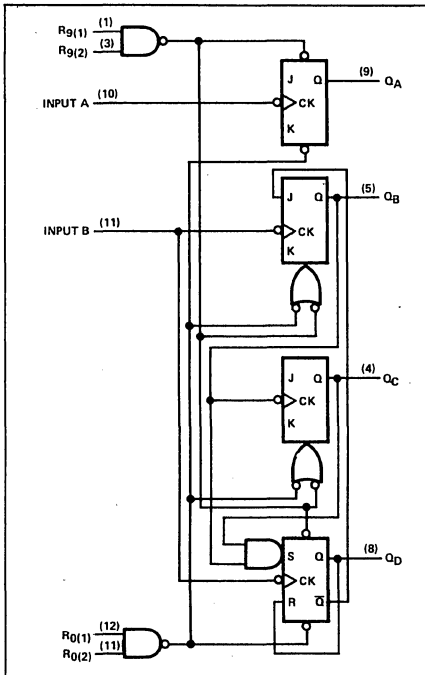
DESCRIPTION

This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

The 54/74LS290 has a gated zero reset and has gated set-to-nine inputs for use in BCD nine's complement applications.

To use the maximum count length (decade or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table. A symmetrical divide-by-ten count can be obtained by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

FUNCTIONAL BLOCK DIAGRAM



The J and K inputs shown without connection are for reference only and are functionally at a high level.

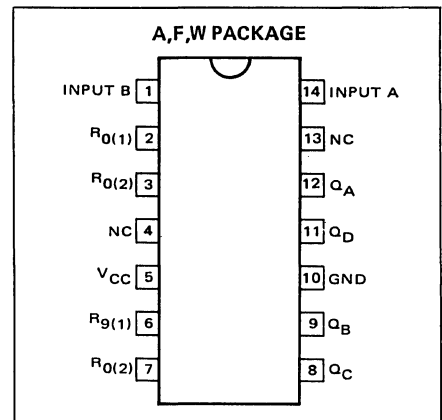
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

PIN CONFIGURATION



RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
R ₀ (1)	R ₀ (2)	R ₉ (1)	R ₉ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

NOTES:

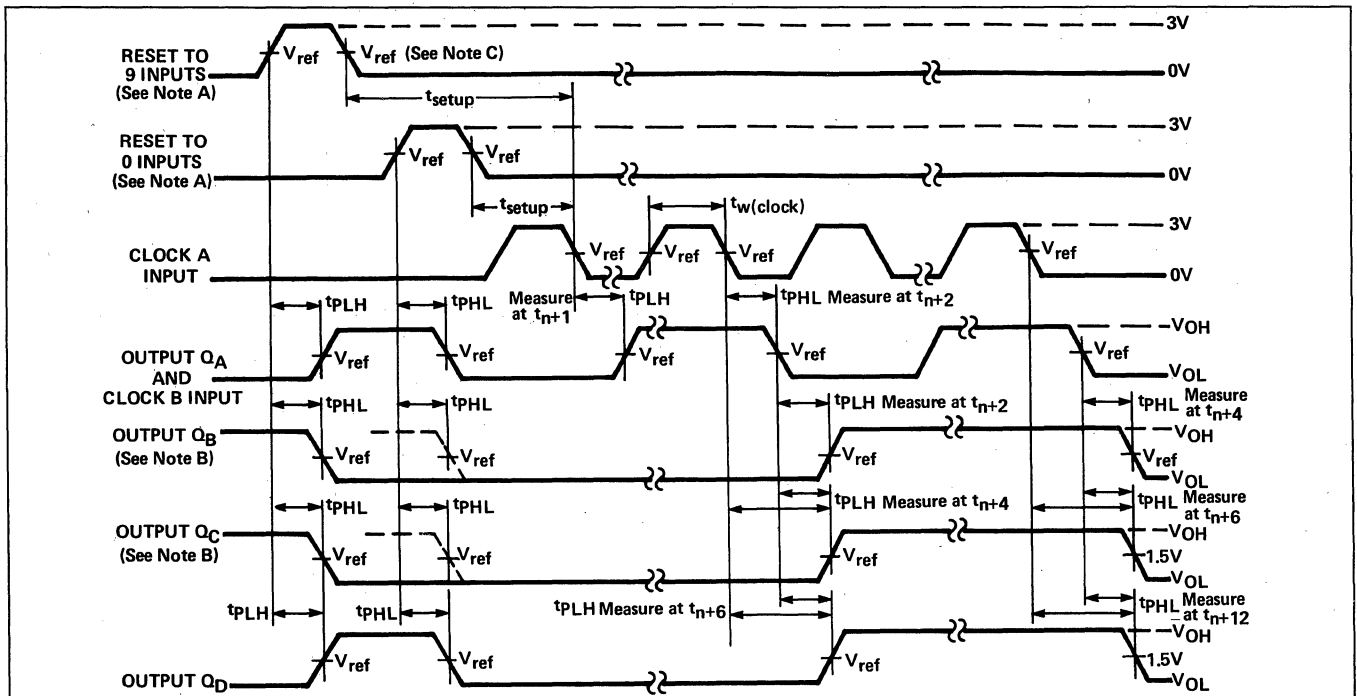
- A. Output Q_A is connected to input B for BCD count.
- B. Output Q_D is connected to input A for bi-quinary count.
- C. Output Q_A is connected to input B.
- D. H = high level, L = low level, X = irrelevant

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
f_{Count}	A B	QA QB		32 16	42		MHZ
t_w Input pulse width	A B Reset	Q Q Q		15 30 15			ns ns ns
t_{Setup} Input setup time				25↓			ns
t_{PLH}	A	QA	$C_L = 15pF,$ $R_L = 400\Omega$		10	16	ns
t_{PHL}	A	QA			12	18	ns
t_{PLH}	A	QD			32	48	ns
t_{PHL}	A	QD			34	50	ns
t_{PLH}	B	QB			10	16	ns
t_{PHL}	B	QB			14	21	ns
t_{PLH}	B	QC			21	32	ns
t_{PHL}	B	QC			23	35	ns
t_{PLH}	B	QD			21	32	ns
t_{PHL}	B	QD			23	35	ns
t_{PHL}	Set-to-0	Any			26	40	ns
t_{PLH}	Set-to-9	QA, QD			20	30	ns
t_{PHL}	Set-to-9	QB, QC			26	40	ns

* f_{max} = maximum count frequency.
 t_{PLH} = propagation delay time, low-to-high-level output
 t_{PHL} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:

- A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 15ns, t_f \leq 5ns, PRR = 1 MHz, duty cycle = 50\%, Z_{out} \approx 50 ohms.$
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N916 or 1N3064.
- D. Each reset input is tested separately with the other reset at 4.5V.
- E. Reference waveforms are shown with dashed lines.
- F. $V_{ref} = 1.3V.$



DESCRIPTION

This monolithic counter contains four master-slave flip-flops and a gated zero reset to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-eight.

To use the maximum count length (decade or four-bit binary) of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table.

RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

NOTES:

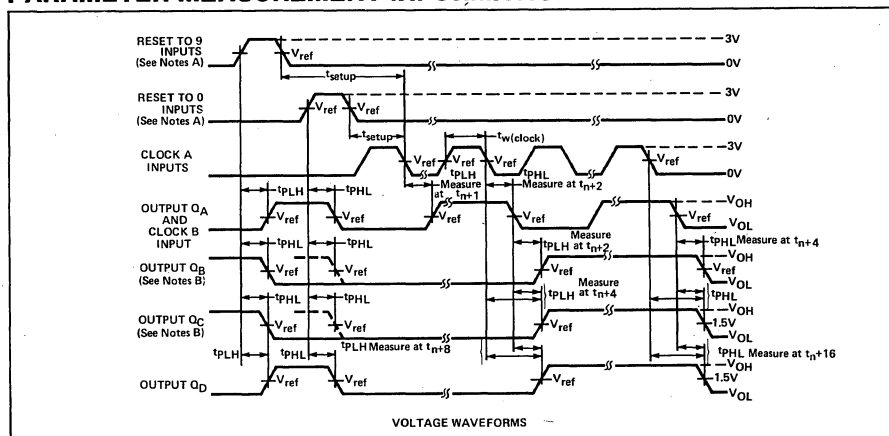
- A. Output Q_A is connected to input B for BCD count.
- B. Output Q_D is connected to input A for bi-quinary count.
- C. Output Q_A is connected to input B.
- D. H = high level, L = low level, X = irrelevant

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
f_{Count}	A	Q_A		32	42		MHz
t_w Input pulse width	A	Q_B		15			ns
	B	Q		30			ns
	Reset	Q		15			ns
t_{Setup} Input setup time				25↓			ns
t_{PLH}	A	Q_A	$C_L = 15pF, R_L = 400\Omega$		10	16	ns
t_{PHL}	A	Q_D			46	70	ns
t_{PLH}	B	Q_B			10	16	ns
t_{PHL}	B	Q_C			21	32	ns
t_{PLH}	B	Q_D			34	51	ns
t_{PHL}	Set-to-0	Any			26	40	ns

- * f_{max} = maximum count frequency
- t_{PLH} = propagation delay time, low-to-high-level output
- t_{PHL} = propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION

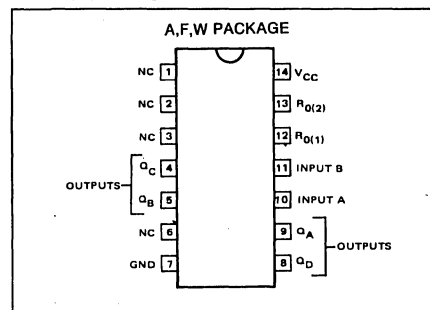


VOLTAGE WAVEFORMS

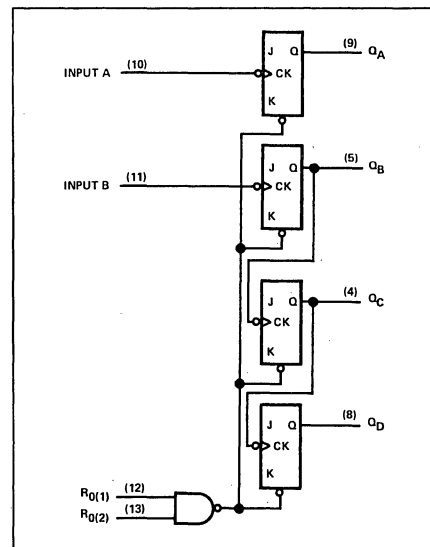
- NOTES:
- A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 15$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N916 or 1N3064.
- D. Each reset input is tested separately with the other reset at 4.5 V.
- E. Reference waveforms are shown with dashed lines.
- F. $V_{ref} = 1.3$ V.

54LS293-F,W • 74LS293-A,F

PIN CONFIGURATION



BLOCK DIAGRAM



The J and K inputs shown without connection are for reference only and are functionally at a high level.

COUNT SEQUENCE

(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

DESCRIPTION

These 4-bit registers feature parallel inputs, parallel outputs, and clock, serial, mode, and output control inputs. The registers have three modes of operation:

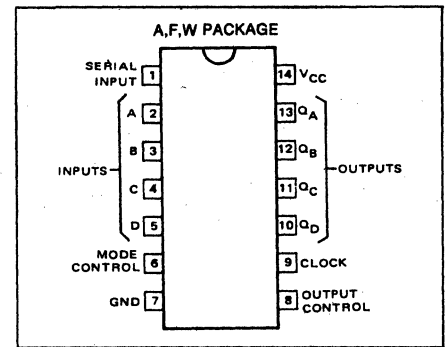
- Parallel (broadside) load
- Shift right (the direction Q_A toward Q_D)
- Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

Shift right is accomplished when the mode control is low; shift left is accomplished when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D.

When the output control is high, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a low logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the registers is not affected.

PIN CONFIGURATION



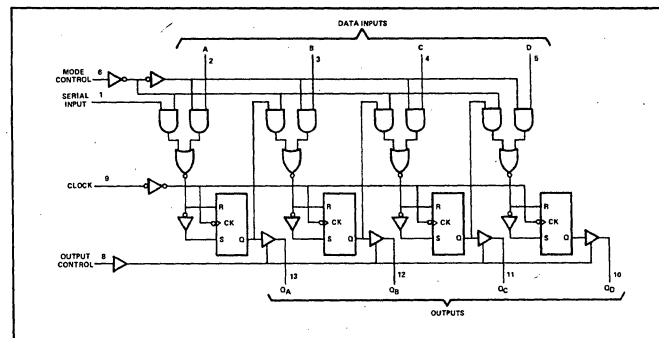
FUNCTION TABLE

MODE CONTROL	CLOCK	SERIAL	INPUTS				OUTPUTS			
			A	B	C	D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	a	b	c	d	a	b	c	d
H	↓	X	Q_{Bt}	Q_{Ct}	Q_{Dt}	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}

When the output control is low, the outputs are disabled to the high impedance state, however, sequential operation of the registers is not affected.

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.
 H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
 ↓ = transition from high to low level.
 a, b, c, d = the level of steady state input at inputs A, B, C, or D, respectively.
 Q_{A0} , Q_{B0} , Q_{C0} , Q_{D0} = the level of Q_A , Q_C , or Q_D , respectively, before the indicated steady state input conditions were established.
 Q_{An} , Q_{Bn} , Q_{Cn} , Q_{Dn} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the most recent ↓ transition of the clock.

FUNCTIONAL BLOCK DIAGRAM



SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			
		MIN	TYP	MAX	UNIT
f_{Clock} Clock frequency		20	28		MHz
$t_{w(Clock)}$ Width of clock pulse		25			ns
t_{Setup} Input setup time, high or low level		20↓			ns
t_{Hold} Input hold time, high or low level		20↓			ns
t_{PLH} Propagation delay time, low-to-high-level output	$C_L = 15pF,$		40	60	ns
t_{PHL} Propagation delay time, high-to-low-level output	$R_L = 2k\Omega$		47	70	ns
t_{ZH} Output enable time to high level			15	25	ns
t_{ZL} Output enable time to low level			21	30	ns
t_{HZ} Output disable time from high level			39	60	ns
t_{LZ} Output disable time from low level			32	50	ns

Load circuit and waveforms are shown at the front of the book.

QUAD 2-INPUTS EXCLUSIVE-OR GATE

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER*	FROM (INPUT)	TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low		10	23	ns
t_{PHL}				10	17	
t_{PLH}	A or B	Other input high		10	30	ns
t_{PHL}				10	22	

* t_{PLH} = propagation delay time, low-to-high-level output

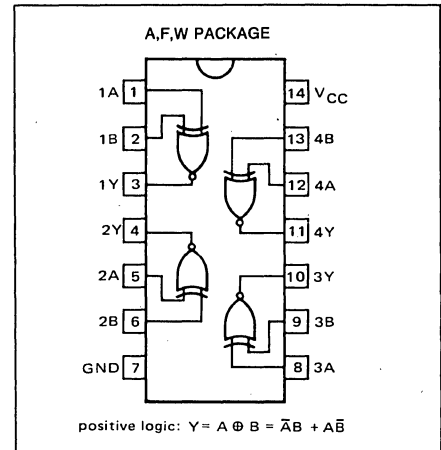
t_{PHL} = propagation delay time, high-to-low-level output

FUNCTION TABLE
(EACH GATE)

INPUTS		OUTPUT
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

H = high level
L = low level

PIN CONFIGURATION



54LS670-F,W • 74LS670-B,F

DESCRIPTION

The S54LS670 and N74LS670 MSI 16-bit TTL register files incorporate the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

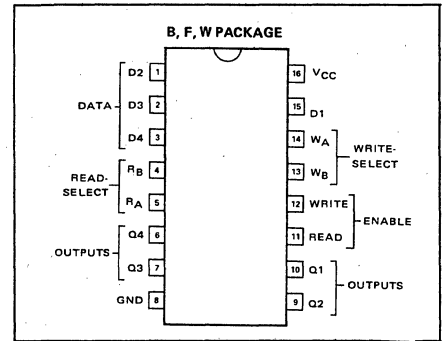
Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W , is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R , is high, the data outputs are inhibited and go into the high-impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

All inputs except read enable and write enable are buffered to lower the drive requirements to one Series 54LS/74LS standard load, and input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and have high-sink-current, three-state outputs. Up to 128 of these outputs may be wire-AND connected for increasing the capacity up to 512 words. Any number of these registers may be paralleled to provide n-bit word length.

PIN CONFIGURATION

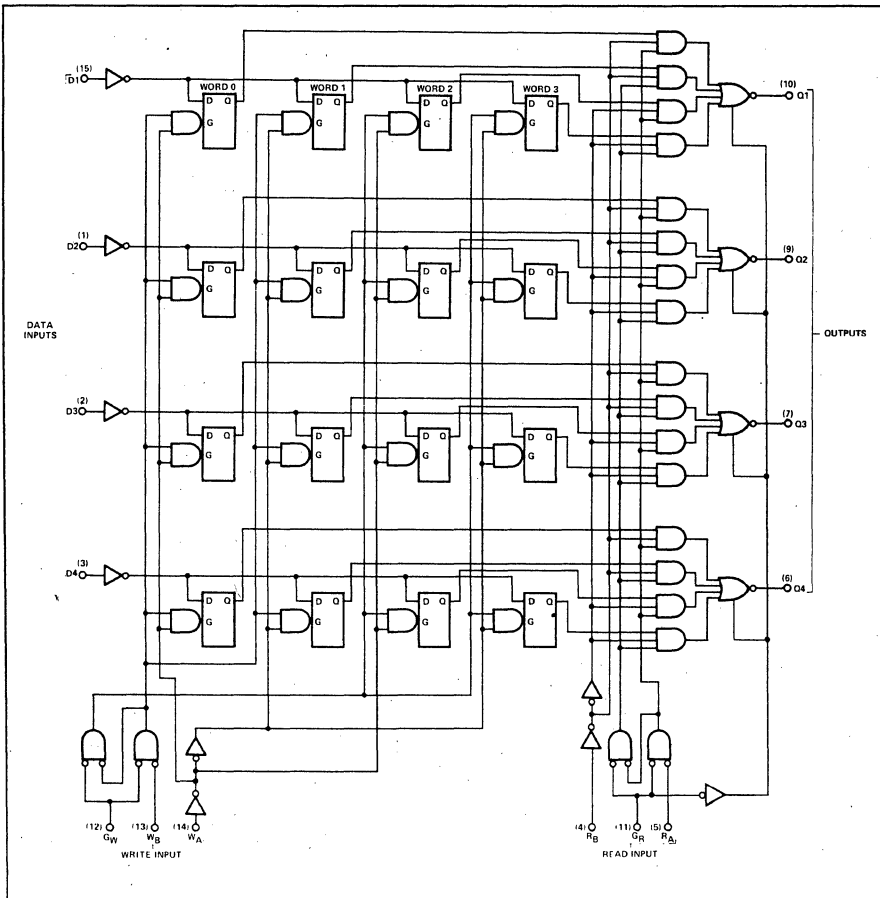


WRITE FUNCTION TABLE

(See Notes A, B and C)

WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	$Q=D$	Q_0	Q_0	Q_0
L	H	L	Q_0	$Q=D$	Q_0	Q_0
H	L	L	Q_0	Q_0	$Q=D$	Q_0
H	H	L	Q_0	Q_0	Q_0	$Q=D$
X	X	H	Q_0	Q_0	Q_0	Q_0

FUNCTIONAL BLOCK DIAGRAM



READ FUNCTION TABLE

(See Notes A and D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q_1	Q_2	Q_3	Q_4
L	L	L	W_0B_1	W_0B_1	W_0B_3	W_0B_4
L	H	L	W_1B_1	W_1B_2	W_1B_3	W_1B_4
H	L	L	W_2B_1	W_2B_2	W_2B_3	W_2B_4
H	H	L	W_3B_1	W_3B_2	W_3B_3	W_3B_4
X	X	H	Z	Z	Z	Z

NOTES:

- A. H = high level, L = low level, X = irrelevant, Z = high impedance (off).
- B. ($Q = D$) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
- C. Q_0 = the level of Q before the indicated input conditions were established.
- D. W_0B_1 = The first bit of word 0, etc.

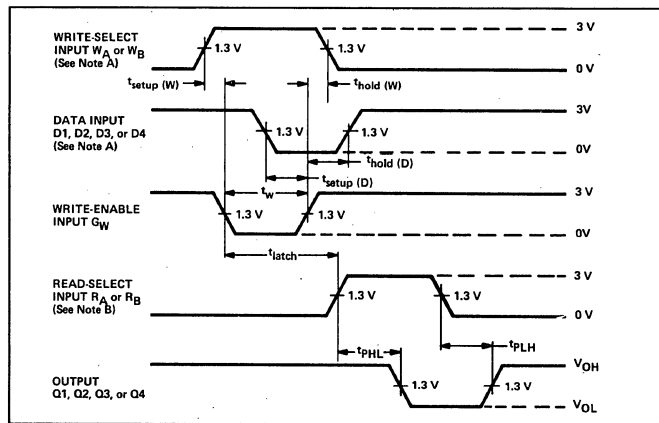
SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS			
				MIN	TYP	MAX	UNIT
t_w	Width of write-enable or read-enable pulse			25			ns
t_{Setup}	Input setup time (See fig. 2)	Write-enable Write-select		10 15			ns
t_{Hold}	Input hold time (See note 2 & fig. 2)	Write-enable Write-select		15 5			ns
t_{Latch}	Latch time for new data (Note 3)			25			ns
Propagation delay time							
t_{PHL}	Low-to-high	Read select	$C_L = 15pF, R_L = 2k\Omega$		23	40	ns
t_{PHL}	High-to-low				25	45	
t_{PLH}	Low-to-high	Write enable			26	45	ns
t_{PHL}	High-to-low				28	50	
t_{PLH}	Low-to-high	Data			25	45	ns
t_{PHL}	High-to-low				23	40	
t_{ZH}	Output enable time to high level				15	35	ns
t_{ZL}	Output enable time to low level				22	40	
t_{HZ}	Output disable time from high level				30	50	ns
t_{LZ}	Output disable time from low level				16	35	

NOTES:

- Voltage values are with respect to network ground terminal.
- Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{Setup(w)}$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{Hold(w)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.
- Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

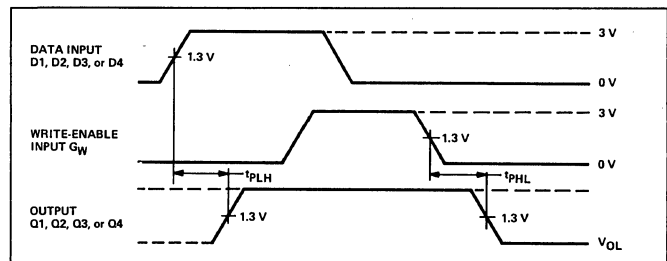
PARAMETER MEASUREMENT INFORMATION



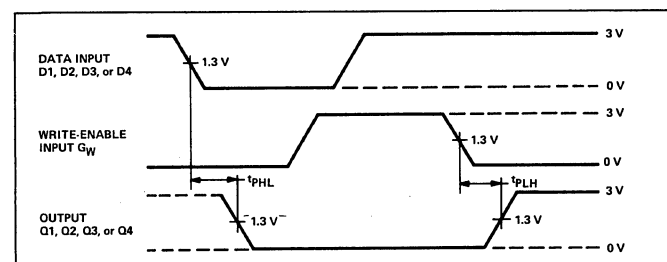
VOLTAGE WAVEFORMS (S1 AND S2 ARE CLOSED)

NOTES:

- High-level input pulses at the select and data inputs are illustrated; however, times associated with low-level pulses are measured from the same reference points.
- When measuring delay times from a read-select input, the read-enable input is low.
- Input waveforms are supplied by generators having the following characteristics: PRR ≤ 2 MHz, $Z_{out} \approx 50 \Omega$, duty cycle $\leq 50\%$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.



VOLTAGE WAVEFORM 1 (S1 AND S2 ARE CLOSED)



VOLTAGE WAVEFORM 2 (S1 AND S2 ARE CLOSED)

NOTES:

- Each select address is tested. Prior to the start of each of the above tests both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test G_P is low.
- Input waveforms are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50 \Omega$, duty cycle $\leq 50\%$, $t_r \leq 15$ ns, $t_f \leq 6$ ns. Load circuit is shown at front of book (for three state outputs).

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INTRODUCTION TO INTERFACE

The Master Selection Guide provides sufficient information to make initial product selections, to lead you to a group of device numbers and manufacturers' names. It enables you to find the products which are most appropriate to fulfill your major requirements and then provides data for many of the more important products.

All devices that appear in this section, both in the initial selection guide and in the data pages, are included in the Part Number and Product Indexes. These index listings lead to the page and the line on that page where each device appears.

In the Interface Section the selection parameters differ drastically for each category; therefore, each has its own format. The analog to digital converter category has two formats: one for binary output devices and another for decimal units. Some of the products in this section, primarily analog to digital and digital to analog converters, are hybrids; the ones listed are those packaged to be compatible with IC's.

This section is not complicated by reference to package styles; the package style suffixes are usually deleted. For more information on each companies' suffixes, see the Part Number Guide. Throughout the Master Selection Guide, each full military temperature range (-55°C to 125°C) device is indicated by a dagger (†) before the manufacturer's name. Manufacturers' names are normally spelled out; however, a few are abbreviated and the abbreviations are explained on page 200.

Category	Page
Analog Switches	
Switches with Drivers	492
Switches without Drivers	498
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Analog to Digital Converters	
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American Microsystems Inc.	532
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The manufacturers listed above are providing detailed information on their latest and most significant products. They have made this investment to help you. Some chose not to.

If you want to see more data in future editions, tell the manufacturers through their salesmen and distributors.

INTERFACE—Analog Switches

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source			
Switches with Drivers							Switches with Drivers (cont)									
SPST	CMOS	75	±11	±15,5	1109	DDC	2xSPST	JFET	10	±10	-20,10,5	DG180A	† Siliconix see page 552, 554			
					H15040-2	† Harris						DG180B	Siliconix see page 552, 554			
					H15040-5	Harris						DG151A	† Intersil			
					IH5040C	Intersil						AM0151C	† National			
					IH5040M	† Intersil						DG151A	† Siliconix see page 551			
					CAG10A	† Teledyne C						DG141B	Intersil			
	JFET	6	-5 to 4	±15,5	CAG6	† Teledyne C						DG441	Intersil			
					-5 to 10	±15						CAG6-10	† Teledyne C	DG141B	Siliconix see page 551	
												10	-5 to 4	±15,5	CAG10C	† Teledyne C
					-5 to 10	±15									CAG6-10	† Teledyne C
		30	±5	±5,5								CAG10	† Teledyne C	DG151B	Siliconix see page 551	
					±8	-18,12						IH5001	Intersil	DG151B	Siliconix see page 551	
		50	±8	-18,12								IH5002	Intersil	DG151B	Siliconix see page 551	
					-10 to 4	±15,5						CAG10B	† Teledyne C	DG151B	Siliconix see page 551	
-10 to 5	±15,5	CAG14	Teledyne C	DG151B			Siliconix see page 551									
		60	±10	±18,5	CAG30	† Teledyne C	DG151B	Siliconix see page 551								
2xSPST	CMOS	30	±11	±15,5	IH5048C	Intersil	DG151B	Siliconix see page 551								
					IH5048M	† Intersil	DG151B	Siliconix see page 551								
		50	±15	±15,5	IH5048-2	† Harris	DG151B	Siliconix see page 551								
					IH5048-5	Harris	DG151B	Siliconix see page 551								
		70	±11	±15	DG200A	† Intersil	DG151B	Siliconix see page 551								
					±15	±15	AD7513S	† AD see page 546	DG151B	Siliconix see page 551						
		75	±15	±15,5			IH200-2	† Harris	DG151B	Siliconix see page 551						
					80	±11	±15	DG200A	† Siliconix see page 559, 560	DG151B	Siliconix see page 551					
		±15	±15	1110				DDC	DG151B	Siliconix see page 551						
				IH5041-2	† Harris	IH5041-5	Harris	DG151B	Siliconix see page 551							
IH5041C	Intersil	IH5041M	† Intersil			DG151B	Siliconix see page 551									
		80	±11	±15	DG200B	Intersil	DG151B	Siliconix see page 551								
±15	±15				AD7513J	AD see page 546	DG151B	Siliconix see page 551								
		JFET	6	-6 to 10	-18,15	AD7513K	AD see page 546	DG151B	Siliconix see page 551							
10	-6 to 10					-18,15	IH200-5	Harris	DG151B	Siliconix see page 551						
		-7.5 to 15	±15,5	DG200B	Siliconix see page 559, 560		DG151B	Siliconix see page 551								
±10	-18,12			DG200C	Siliconix see page 559, 560	DG151B	Siliconix see page 551									
		DG180A	† Siliconix see page 552, 554	DG151B	Siliconix see page 551											
DG180B	Siliconix see page 552, 554	DG151B	Siliconix see page 551													
DG141A	† Intersil	DG151B	Siliconix see page 551													
IH5005	† Intersil	DG151B	Siliconix see page 551													
AM0141	† National	DG151B	Siliconix see page 551													
AM0141C	National	DG151B	Siliconix see page 551													
DG141A	† Siliconix see page 551	DG151B	Siliconix see page 551													

† Military Temperature Range (-55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

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INTERFACE—Analog Switches (cont)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source
Switches with Drivers (cont)						
2xSPST (continued)	JFET	50	±10	-18,15	CAG45A CAG48 CAG48A	† Teledyne C Teledyne C Teledyne C
			±10	-18,12	IH5004	Intersil
			-12.5 to 10 -20,10,- 5		DG181B IH181C DG181B	Intersil Intersil Siliconix see page 552, 554
	75		-10 to 15	±15,5	DG182A IH182M DG182A	† Intersil † Intersil † Siliconix see page 552, 554
			-15 to 10 -20,10,- 5		DG182A IH182M DG182A	† Intersil † Intersil † Siliconix see page 552, 554
	80		±8	-18,12	DG4344A	Intersil
			±10	-18,12	DG134A IH5007 AH0134 AH0134C DG134A	† Intersil Intersil † National National † Siliconix see page 551
	100		±5.5	±15	DG452 DG152B	Intersil Siliconix see page 551
				±8	-18,12	DG134B DG134B
			±15,5	-10 to 15	DG182B IH182C DG182B	Intersil Intersil Siliconix see page 552, 554
-15 to 10 -20,10,- 5					DG182B IH182C DG182B	Intersil Intersil Siliconix see page 552, 554
PMOS	75-200	-5 to 10	±15,5	DGM111A	† Siliconix see page 557, 558	
			±10	-20,10,5	DGM111A	† Siliconix see page 557, 558
	75-250	-5 to 10	±15,5	DGM111B	Siliconix see page 557, 558	
			±10	-20,10,5	DGM111B	Siliconix see page 557, 558
	100-450	±10	-20,10,5	DG111 DG112	† Intersil † Intersil	
4xSPST	CMOS	80	±15	±15	HI201-2	† Harris
		80*	±5		CDS4016 CDS4016E	RCA RCA
		100	±15	±15	HI201-5 AD7510J AD7510K	Harris AD AD see page 546 see page 546 (continued)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source
Switches with Drivers (cont)						
4xSPST (continued)	CMOS	100	±15	±15	AD7510S	† AD see page 546
					AD7510DIJ	AD see page 546
					AD7510DIK	AD see page 546
					AD7510DIS	† AD see page 546
					AD7511J	AD
					AD7511K	AD
					AD7511S	† AD see page 546
					AD7511D1J	AD see page 546
					AD7511D1K	AD see page 546
					AD7511D1S	† AD see page 546
		175	±15	±15	DG201A	† Siliconix see page 559, 560
		200	±15	±15	DG201B DG201C	Siliconix see page 559, 560 Siliconix see page 559, 560
		280	±7.5	±7.5	AD7516K AD7516T F4066C F4066M HD4066A-2 HD4066A-9 CD4066C CD4066M MC14066BA MC14066BC CD4066A CD4066AE HBF4066AE N4066A SCL4066A SCL4066AE CD4066 TC4066	AD † AD see page 546 Fairchild † Fairchild † Harris Harris National † National † Motorola Motorola † RCA see page 375 RCA see page 375 SGS Signetics † SSS SSS Teledyne C Toshiba
		400	±7.5	±7.5	AD7516J AD7516S	AD see page 546 † AD see page 546
					MC14016A MC14016C SCL4016A SCL4016AE CM4016A CM4016AE TF4016A/B TP4016A/B TF4316A TP4316A	† Motorola Motorola † SSS SSS † Solitron Solitron TI † TI TI † TI (continued)

† Military Temperature Range (-55°C to 125°C)

DT1 means four terminals with a pair of normally open and normally closed contacts.

INTERFACE—Analog Switches (cont)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source	
Switches with Drivers (cont)							
4xSPST (continued)	CMOS	400	±7.5	±7.5	TC4016	Toshiba	
		800	±7.5	±7.5	F4016C F4016M	Fairchild † Fairchild	
		850	±7.5	±7.5	MEM4016D MEM4016P CD4016C CD4016M CD4016A/B † see page 375 CD4016A/BE † see page 375 N4016 SCL4086A SCL4086AE CM4016A CM4016AE CM4116A CM4016AE SW4016AE	† GI GI National † National † RCA RCA Signetics † SSS SSS † Solitron Solitron † Solitron Solitron SW	
Inverted control		±7.5	±7.5	SCL4416A SCL4416AE	† SSS SSS		
4xSPST	JFET	200	±10	±15,5	Various Combinations of normally on/off	LF12201 LF13201 LF12202 LF13202 LF12331 LF13331 LF12332 LF13332 LF12333 LF13333	National National National National National National National National National National
						250	±10
4xSPST	PMOS	100-450	±10	-20,10 -20,10,5	DG116	† Intersil	
					DG118	† Intersil	
		150-450	±10	-20,10,5	DG172A	† Siliconix see page 557, 558	
		150-500	±10	-20,10,5	DG172B	Siliconix see page 557, 558	
200-600	±10	-20,10,5	AH0015 AH0015C DG172C	† National National Siliconix see page 557, 558			
			5xSPST	PMOS	100-450	±10	-20,10
Common output	±10	-20,10,5	DG125 DG125A	† Intersil † Siliconix see page 551			

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source		
Switches with Drivers (cont)								
5X SPST	PMOS	125-500	±10	-20,10	DG123B DG123B	Intersil Siliconix see page 551		
				±10	-20,10,5	DG125B DG125B	Intersil Siliconix see page 551	
SPDT ¹	CMOS	30	±11	±15,5	IH5050C IH5050M	Intersil † Intersil		
				50	±15	±15,5	HI5050-2 HI5050-5	† Harris Harris
				75	±15	±15,5	1111 HI5042-2 HI5042-5 IH5042C IH5042M	† DDC † Harris Harris Intersil † Intersil
JFET	6	-5 to 10	±15	CAG7	† Teledyne S			
				10	±10	-15,5	CDA23	† Teledyne S
				-5 to 10	CAG7-10	† Teledyne S		
				±15	-7.5 to 15	±15,5	DG186A see page 552, 554 DG186B see page 552, 554	† Siliconix Siliconix see page 552, 554
				±10	-18,12	DG146A AH0146 AH0146C DG146A	† Intersil † National National Siliconix see page 551	
				-12.5 to 10 -20,10, 5	DG186A see page 552, 554 DG186B see page 552, 554	† Siliconix Siliconix see page 552, 554		
				±7.5	±15	DG161A AH0161 AH0161C DG161A	† Intersil † National National Siliconix see page 551	
				±8	-18,12	DG146B DG446A DG146B	Intersil Intersil Siliconix see page 551	
				±5.5	±15	DG461A DG161B	Intersil Siliconix see page 551	
				30	-7.5 to 15	±15,5	DG187A IH187M DG187A	† Intersil † Intersil † Siliconix see page 552, 554
				±10	-18,12	DG144A AH0144 AH0144C DG144A	† Intersil † National National † Siliconix see page 551	
				-12.5 to 10 -20,10, 5	DG187A IH287M DG187A	† Intersil † Intersil † Siliconix see page 552, 554		

† Military Temperature Range (-55°C to 125°C) * — Typical Values

Bold face indicates additional data is provided on the page noted.

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INTERFACE—Analog Switches (cont)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source
Switches with Drivers (cont)						
SPDT [†]	JFET				DG444A	Intersil
		50	±7.5	±15	DG162A AH0162 AH0162C DG162A	† Intersil † National National † Siliconix see page 551
			-7.5 to 15	±5.5	DG187B IH187C DG187B	Intersil Intersil Siliconix see page 552, 554
			±8	-18,12	DG144B DG144B	Intersil Siliconix see page 551
			-12.5 to 10	-20,10,-5	DG187B IH187C DG187B	Intersil Intersil Siliconix see page 552, 554
		75	-10,15	±15,5	DG188A IH188M DG188A	† Intersil † Intersil † Siliconix see page 552, 554
			-15,10	-20,10,5	DG188A IH188M DG188A	† Intersil † Intersil † Siliconix see page 552, 554
		80	±8	-18,12	DG443	Intersil
			±10	-18,12	DG143 AH0143 AH0143C DG143A	† Intersil † National National † Siliconix see page 551
		100	±5.5	±15	DG162B	Siliconix see page 551
			±8	±15	DG462A	Intersil
			±10	±15	AH2114	† National
			±10	-18,12	DG143B	Siliconix see page 551
			-10 to 15	±15,5	DG188B IH188C DG188B	Intersil Intersil Siliconix see page 552, 554
			-15 to 10	-20,10,-5	DG188B IH188C DG188B	Intersil Intersil Siliconix see page 552, 554
		125	±10	±15	AH2114C	National
SPDT	JFET	50	±10	-15,5	CDA18	Teledyne C
SPDT (for D/A)	NPN-PNP					
		10	10	10	CDA4A	† Teledyne C
			-0 to -10	-15	CDA1-3	Teledyne C
			±10	±15	CDA6	Teledyne C
SPDT [†]	PMOS	75-200	-5 to 15	±15	DG175A	† Siliconix see page 557, 558

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source
Switches with Drivers (cont)						
SPDT [†]	PMOS	75-200	±10	-20,10,5	DG175A	† Siliconix see page 557, 558
		75-250	-5 to 15	±15	DG175B	Siliconix see page 557, 558
			±10	-20,10,5	DG175B	Siliconix see page 557, 558
SPDT	PMOS	100-400	±10	-20,10	SI3002A SI3002B	† Siliconix see page 551 Siliconix see page 551
		200*	±10	-20,10	SH3002C SH3002M	Fairchild † Fairchild
2xSPDT [†]	CMOS	30	±11	±15,5	IH5051C IH5051M	Intersil † Intersil
		50	±15	±15,5	IH5051-2 IH5051-5	† Harris Harris
		75	±15	±15,5	1112 IH5043-2 IH5043-5 IH5043C IH5043M	† DDC † Harris Harris Intersil † Intersil
2xSPDT	CMOS	100	±15	±15	AD7512J AD7512K AD7512S AD7512DIJ AD7512DIK AD7512DIS	AD AD see page 546 † AD see page 546 AD see page 546 † AD see page 546
2xSPDT [†]	JFET	10	-7.5 to 15	±15,5	DG189A DG189B	† Siliconix see page 552, 554 Siliconix see page 552, 554
			±12.5 to 15	-20,15,-5	DG189A DG189B	† Siliconix see page 552, 554 Siliconix see page 552, 554
		30	-7.5 to 15	±15,5	DG190A IH190M DG190A	† Intersil † Intersil † Siliconix see page 552, 554
			-12.5 to 15	-20,15,-5	DG190A IH190M DG190A	† Intersil † Intersil † Siliconix see page 552, 554
		50	-7.5 to 15	±15,5	DG190B	Siliconix see page 552, 554
			-12.5 to 15	-20,10,-5	DG190B	Siliconix see page 552, 554

† Military Temperature Range (-55°C to 125°C)

DT[†] means four terminals with a pair of normally open and normally closed contacts.

INTERFACE—Analog Switches (cont)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source
Switches with Drivers (cont)						
2xSPDT [†]	JFET	75 – 10 to 15 ± 15,5			DG191A	† Intersil
					IH191M	† Intersil
					DG191A	† Siliconix see page 552, 554
			– 15 to 10 – 20,10,- 5		DG191A	† Intersil
					IH191M	† Intersil
					DG191A	† Siliconix see page 552, 554
		100	– 10 to 15 ± 15,5		DG191B	Intersil
					IH191C	Intersil
					DG191B	Siliconix see page 552, 554
2xSPDT [†]	JFET	100	– 15 to 10 – 20,10,- 5		DG191B	Intersil
					IH191C	Intersil
					DG191B	Siliconix see page 552, 554
3xSPDT	CMOS	280	± 7.5	± 7.5	F4053C	Fairchild
					F4053M	† Fairchild
					HD4053A-2	† Harris
					HD4053A-9	Harris
					MEM4053D	† GI
					MEM4053P	GI
					MC14053BA	† Motorola
					MC14053BC	Motorola
					CD4053C	National
					CD4053M	† National
					CD4053A/B	† RCA see page 375
					CD4053A/BE	RCA see page 375
					SCL4053A	† SSS
					SCL4053AE	SSS
					CM4053A	† Solitron
					CM4053AE	Solitron
TF4053A/B	† TI					
TF4053A/B	TI					
TC4053	Toshiba					
	PMOS	200-800	± 10	– 20,10,5	DG170A	† Siliconix see page 557, 558
		250-850	± 10	– 20,10,5	DG170B	Siliconix see page 557, 558
					DG170C	Siliconix see page 557, 558
4xSPDT (for D/A)	CMOS	100	0.1	8	AD7519J	AD see page 546
					NMOS	—
	NPN	—	– 10 to – 3 ± 15		ULN-2140	Sprague
					ULN-2141	Sprague
					ULN-2142	Sprague
					ULS-2140	† Sprague
					ULS-2141	† Sprague
					ULS-2142	† Sprague
	NPN-PNP	7	0 to – 10 – 15		CDA11-512	Teledyne C
		10	0 to – 10 – 15		CDA11	Teledyne C

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source
Switches with Drivers (cont)						
4xSPDT (for D/A)	NPN	—	—	—	AD550	† AD
					AD555	AD
	PNP	—	—	—	3240	Teledyne P
10xSPDT (for D/A)	NMOS	—	—	8	DG516A	† Siliconix
					DG516B	Siliconix
					DG516C	Siliconix
DPST	CMOS	75	± 15	± 15,5	1113	† DDC
					IH5044-2	† Harris
					IH5044-5	Harris
					IH5044C	Intersil
					IH5044M	† Intersil
2xDPST	CMOS	30	± 11	± 15,5	IH4049C	Intersil
					IH4049M	† Intersil
		50	± 15	± 15,5	IH5049-2	† Harris
					IH5049-5	Harris
		75	± 15	± 15,5	1114	† DDC
					IH5045-2	† Harris
					IH5045-5	Harris
					IH5045C	Intersil
					IH5045M	† Intersil
2xDPST	CMOS	200	± 15	± 15,5	IH1800A-2	† Harris
					IH1800A-5	Harris
2xDPST	JFET	10	– 7.5 to 15 ± 15,5	± 15,5	DG183A	† Siliconix see page 552, 554
					DG183B	Siliconix see page 552, 554
			± 10	– 18,12	DG140A	† Intersil
					AH0140	† National
					AH0140C	National
					DG140A	† Siliconix see page 551
			– 12.5 to 10 – 20,10,-		DG183A	† Siliconix see page 552, 554
					DG183B	† Siliconix see page 552, 554
		15	± 7.5	± 15	DG153A	† Intersil
					AH153	† National
					AH153C	National
					DG153A	† Siliconix see page 551
			± 8	– 18,12	DG440A	Intersil
					DG140B	Siliconix see page 551
			± 10	– 18,15	CS4R	Teledyne C
					CD4RA	† Teledyne C
		20	± 5.5	± 15	DG153B	Intersil
					DG453	Intersil
					DG153B	Siliconix see page 551
		30	– 6 to 10 – 18,15		CAG21	† Teledyne C
			– 7.5 to 15 ± 15,5		DG184A	† Intersil
					IH184M	† Intersil
					DG184A	† Siliconix see page 552, 554

† Military Temperature Range (–55°C to 125°C) * — Typical Values

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INTERFACE—Analog Switches (cont)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source	
Switches with Drivers (cont)							
2xDPST	JFET	-18,12			DG129A † Intersil	† National National † Siliconix see page 551	
					AH0129 † National		
					AH0129C † National		
				DG129A † Siliconix			
				-12.5 to 10 -20,10,-5		DG184A † Intersil	† Intersil † Intersil † Siliconix see page 552, 554
					IH184M † Intersil		
					DG184A † Siliconix		
					see page 552, 554		
				35 ±8 -18,12		DG429A Intersil	
				50 ±7.5 ±15		DG154A † Intersil	† National National † Siliconix see page 551
			AH0154 † National				
			AH0154C † National				
			DG154A † Siliconix				
			±7.5 to 15 ±15,5	DG184B Intersil	Intersil Intersil Siliconix see page 552, 554		
				IH184C Intersil			
				DG184B Siliconix			
				see page 552, 554			
			±8 -18,12	DG129B Siliconix	see page 551		
			-12.5 to 15 -20,10,-5	DG184B Intersil	Intersil Intersil Siliconix see page 552, 554		
				IH184C Intersil			
				DG184B Siliconix			
				see page 552, 554			
			75 -10 to 15 ±15,5	DG185A † Intersil	† Intersil † Intersil † Siliconix see page 552, 554		
				IH185M † Intersil			
				DG185A † Siliconix			
				see page 552, 554			
			-15 to 10 -20,10,-5	DG185A Intersil	Intersil † Intersil † Siliconix see page 552, 554		
				IH185M † Intersil			
				DG185A † Siliconix			
				see page 552, 554			
			80 ±8 -18,12	DG426A Intersil			
			±10 -18,12	DG126A † Intersil	† National National † Siliconix see page 551		
				AH0126 † National			
				AH0126C † National			
				DG126A † Siliconix			
				see page 551			
			100 ±5.5 ±15	DG154B Intersil	Intersil Intersil Siliconix see page 551		
				DG454A Intersil			
				DG154B Siliconix			
				see page 551			
			±8 -18,12	DG126B Siliconix	see page 551		
			-10 to 15 ±15,5	DG185B Intersil	Intersil Intersil Siliconix see page 552, 554		
				IH185C Intersil			
				DG185B Siliconix			
				see page 552, 554			
			-15 to 10 -20,10,-5	DG185B Intersil	Intersil Intersil Siliconix see page 552, 554		
				IH185C Intersil			
				DG185B Siliconix			
				see page 552, 554			

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source
Switches with Drivers (cont)						
2xDPST Common output	PMOS	100-450	±10	-20,10,5	DGM122A † Siliconix	see page 557, 558
		125-500	±10	-20,10,5	DGM122B Siliconix	see page 557, 558
		200-600	±10	-20,10,5	AH0019 † National	AH0019C National
3xDPST Common output	PMOS	100-450	±10	-20,10	DG120 † Intersil	
			±10	-20,10,5	DG121 † Intersil	
DPDT ¹	CMOS	50	±15	±15,5	HI5046A-2 † Harris	HI5046A-5 Harris
		75	±15	±15,5	1115 † DDC	HI5046-2 † Harris
					HI5046-5 Harris	
					IH5046C Intersil	
					IH5046M † Intersil	
	JFET	10	±10	-18,12	DG145A † Intersil	AH0145 † National
					AH0145C National	
					DG145A † Siliconix	see page 551
		15	±7.5	±15	DG163A † Intersil	AH0163 † National
					AH0163C National	
					DG163A † Siliconix	see page 551
			±8	-18,12	DG445A Intersil	DG145B Siliconix
					see page 551	
		20	±5.5	±15	DG163B Intersil	DG463A Intersil
					DG163B Siliconix	see page 551
		30	±10	-18,12	DG139A † Intersil	AH0139 † National
					AH0139C National	
					DG139A † Siliconix	see page 551
		35	±8	-18,12	DG439A Intersil	
		50	±7.5	±15	DG164A † Intersil	AH0164 † National
					AH0164C National	
					DG164A † Siliconix	see page 551
			±8	-18,12	DG139B Siliconix	see page 551
		80	±8	-18,12	DG442A Intersil	
			±10	-18,12	DG142A † Intersil	AH0142 † National
					AH0142C National	
					DG142A † Siliconix	see page 551
		100	±5.5	±15	DG164B Intersil	DG464A Intersil
					DG164B Siliconix	see page 551

† Military Temperature Range (-55°C to 125°C)

DT¹ means four terminals with a pair of normally open and normally closed contacts.

INTERFACE—Analog Switches (cont)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source
Switches with Drivers (cont)						
DPDT [†]	JFET	100	±10	-18,12	DG142B see page 551	Siliconix
DPDT	PMOS	150-450	±10	-20,10,5	DG173A see page 557, 558	† Siliconix
		150-500	±10	-20,10,5	DG173B see page 557, 558	Siliconix
		200-600	±10	-20,10,5	AH0014 AH0014C	† National National
		200-275	±10	-28,5,12	CRC9005	Collins
4PST	CMOS	50	±15	±15,5	HI5047A-2 HI5047A-5	† Harris Harris
		75	±15	±15,5	HI5047-2 HI5047-5 1116 IH5047C IH5047M	† Harris Harris † DDC Intersil † Intersil
4PST (for D/A)	JFET	10	±10	±15,5	CDA28A CDA28B	† Teledyne C Teledyne C
Switches without Drivers						
SPST	JFET	30	±10		AM1000	† National
		50	±15		AM1001	† National
		100	±0.2		IH5021C IH5021M IH5023C IH5023M	Intersil † Intersil Intersil † Intersil
			0 to (Drive-4)		1105C-1 1105M-1 IH5037C IH5037M	DDC † DDC Intersil † Intersil
			±10		AM1002	† National
			±0.2		1101C-1 1101M-2 1101C-2 1101M-2 IH5022C IH5022M IH5024C IH5024M	DDC † DDC DDC † DDC Intersil † Intersil Intersil † Intersil
		0 to (Drive-4)		1105C-2 1105M-2 IH5038C IH5038M	DDC † DDC Intersil † Intersil	
		150	±0.2		IH5017C IH5017M	Intersil † Intersil
			0 to (Drive-4)		1106C-3 1106M-3 IH5033 IH5033M	DDC † DDC Intersil † Intersil
			±0.2		1102C-2 1102M-1 IH5020C IH5020M	DDC † DDC Intersil † Intersil
0 to (Drive-4)						

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source
Switches without Drivers (cont)						
2xSPST	JFET	150	0 to (Drive-4)		1106C-2 1106M-2 IH5036C IH5036M	DDC † DDC Intersil † Intersil
2xSPST Common output	JFET	100	±0.2		IH5019C IH5019M	Intersil † Intersil
			0 to (Drive-4)		1106C-1 1106M-1 IH5035C IH5035M	DDC † DDC Intersil † Intersil
		150	±0.2		1102C-1 1102M-1 IH5018C IH5018M	DDC † DDC Intersil † Intersil
			0 to (Drive-4)		1106C-4 1106M-4 IH5034C IH5034M	DDC † DDC Intersil † Intersil
			±0.2		IH5015C IH5051M AH5051C	Intersil † Intersil National
			0 to (Drive-4)		1107C-1 1107M-1 IH5031C IH5031M	DDC † DDC Intersil † Intersil
		150	±0.2		1103C-2 1103M-2 IH5016C IH5016M AH5016C	DDC † DDC Intersil † Intersil National
			0 to (Drive-4)		1107C-2 1107M-2	DDC † DDC
			±0.2		IH5013C IH5013M AH5013C	Intersil † Intersil National
			0 to (Drive-4)		1107C-3 1107M-3 IH5029C IH5029M	DDC † DDC Intersil † Intersil
		150	±0.2		1103C-1 1103M-1 IH5014C IH5014M AH5014C	DDC † DDC Intersil † Intersil National
			0 to (Drive-4)		1107C-4 1107M-4 IH5030C IH5030M	DDC † DDC Intersil † Intersil
			±0.2		MM455 MM555 MM455 MM555 SI455 SI555	† Intersil Intersil † National National † Siliconix Siliconix
			0 to (Drive-4)			
4xSPST	DMOS	45	±5		SD5001	Signetics

† Military Temperature Range (-55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

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INTERFACE—Analog Switches (cont)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source
Switches without Drivers (cont)							Switches without Drivers (cont)						
4xSPST	DMOS	45	±10		SD5000	Signetics	4xSPST	JFET	—			G129	† Intersil
4xSPST	DMOS	45	±5		SD5101	Signetics	Common output					G130	† Intersil
Common output			±10		SD5100	Signetics						G131	† Intersil
4xSPST	JFET	100	±0.2		IH5011C	Intersil						G132	† Intersil
					IH5011M	† Intersil						G1350	Intersil
					AH5011C	National						G1360	Intersil
					AM97C11C	National						G129A	† Siliconix
					AM9711C	National						G129B	Siliconix
				0 to (Drive-4)								G130A	† Siliconix
					1108C-1	DDC						G130B	Siliconix
					1108M-1	† DDC						G131A	† Siliconix
					IH5027C	Intersil						G131B	Siliconix
					IH5027M	† Intersil						G132A	† Siliconix
												G132B	Siliconix
		150	±0.2		1104C-2	DDC	4xSPST	JFET	—			G123	Intersil
					1104M-2	† DDC	Two outputs						
					IH5012C	Intersil	4xSPST	PMOS	—			MM452	† Intersil
					IH5012M	† Intersil	Common output					MM552	Intersil
					AH5012C	National							
					AM97C12C	National	4xSPST	PMOS	—			MM451	† Intersil
					AM9712C	National	Common output						
				0 to (Drive-4)								MM551	Intersil
					1108C-2	DDC						MM451	† National
					1108M-2	† DDC						MM551	National
					IH5028C	Intersil	4xSPST	PMOS	—			G123A	† Siliconix
					IH5028M	† Intersil	Two outputs					G123B	Siliconix
					G125	† Intersil	5xSPST	PMOS	—			G116C	Intersil
					G126	† Intersil	Common output						
					G127	† Intersil						G116M	† Intersil
					G128	† Intersil						G114A	† Siliconix
					G1330	Intersil						G114B	Siliconix
					G1340	Intersil						G116A	† Siliconix
					G125A	† Siliconix						G116B	Siliconix
					G125B	Siliconix							
					G126A	† Siliconix	5xSPST	PMOS	—			G117C	Intersil
					G126B	Siliconix	Common output plus						
					G127A	† Siliconix						G117M	† Intersil
					G127B	Siliconix	output switch						
					G127A	† Siliconix						G117A	† Siliconix
					G128A	† Siliconix						G117B	Siliconix
					G128B	Siliconix							
4xSPST	JFET	100	±0.2		IH5009C	Intersil	6xSPST	PMOS	—			AM2009	† National
Common output					IH5009M	† Intersil	Common output					CRC9509	Collins
					AH5009C	National						AM2009C	National
					AM97C09C	National						MM5504	† National
					AM9709C	National						MM4504	National
				0 to (Drive-4)								G115	Intersil
					1108C-3	DDC						G118C	Intersil
					1108M-3	† DDC						G118M	† Intersil
					IH5025C	Intersil						G115A	† Siliconix
					IH5025M	† Intersil						G115B	Siliconix
		150	±0.2		1104C-1	DDC	10xSPST					G118A	† Siliconix
					1104M-1	† DDC						G118B	Siliconix
					IH5010C	Intersil							
					IH5010M	† Intersil	2xDPST	PMOS	—			G122A	† Siliconix
					AH5010C	National	Common output						
					AM97C10C	National						G122B	Siliconix
					AM9710C	National						MM450	† Intersil
				0 to (Drive-4)								MM550	Intersil
					1108C-4	DDC						MM450	† National
					1108M-4	† DDC						MM550	National
					IH5026C	Intersil	3xDPST	PMOS	—			G119C	Intersil
					IH5026M	† Intersil	Common output						

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† Military Temperature Range (−55°C to 125°C)

DT† means four terminals with a pair of normally open and normally closed contacts.

INTERFACE—Analog Switches (cont)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source
Switches without Drivers (cont)						
Common output						
					G119M	† Intersil
					G119A	† Siliconix
					G119B	Siliconix
Multiplexers						
4 channel differential CMOS						
		270	±7.5	±7.5	HD14529-2	† Harris
					HD14529-9	Harris
					MC14529A	† Motorola
					MC14529C	Motorola
		280	±7.5	±7.5	F4052C	Fairchild
					F4052M	† Fairchild
					HD4052A-2	† Harris
					HD4052A-9	Harris
					HD4052-5	Harris
					MC14052BA	† Motorola
					MC14052BC	Motorola
					CD4052C	National
					CD4052M	† National
					CD4052A/B	† RCA
						see page 375
					CD4052A/BE	RCA
						see page 375
					SCL4052A	† SSS
					SCL4052AE	SSS
					CM4052A	† Solitron
					CM4052AE	Solitron
					TF4052A/B	† TI
					TP4052A/B	TI
					TC4052	Toshiba
		300	±15	±15	AD7502J	AD
						see page 548
					AD7502K	AD
						see page 548
					AD7502S	† AD
						see page 548
		400	±15	±15	HI1828A-2	† Harris
					HI1828A-5	Harris
					DG509A	† Intersil
					DG509A	† Siliconix
						see page 561, 563
		450	±15	±15	DG509B	Intersil
					DG509C	Intersil
					DG509B	Siliconix
						see page 561, 563
					DG509C	Siliconix
						see page 561, 563
		1500	±15	±15	HI509A-2	† Harris
		1800	±15	±15	HI509A-5	Harris
	JFET	300	±10	±15.5	LF11306	† National
					LF12306	National
					LF13306	National
	PMOS	175-600	±10	-20,10	DG511A	† Siliconix
		200-700	±10	-20,10	DG511B	Siliconix
4 Sequential Commutator PMOS						
		200-600	±10	-24,12	MM454	† National
					MM554	National

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source
Multiplexers (cont)						
6 channel						
	JFET	60	±10	-18,2.8	CAM601	Teledyne C
					CAM601A	† Teledyne C
8 channel						
	CMOS	150	±8	±8	MS504	Ragen
		270	±7.5	±7.5	HD4529-2	† Harris
					HD4529-5	Harris
					MC14529A	† Motorola
					MC14529C	Motorola
		280	±7.5	±7.5	F4051C	Fairchild
					F4051M	† Fairchild
					HD4051A-2	† Harris
					HD4051A-9	Harris
					MEM4051D	† GI
					MEM4051P	GI
					MC14051BA	† Motorola
					MC14051BC	Motorola
					CD4051C	National
					CD4051M	† National
					CD4051A/B	† RCA
						see page 375
					CD4051A/BE	RCA
						see page 375
					SCL4051A	† SSS
					SCL4051AE	SSS
					CM4051A	† Solitron
					CM4051AE	Solitron
					TF4051A/B	† TI
					TP4051A/B	TI
					TC4051	Toshiba
		300	±15	±15	AD7501J	AD
						see page 548
					AD7501K	AD
						see page 548
					AD7501S	† AD
						see page 548
					AD7503J	AD
						see page 548
					AD7503K	AD
						see page 548
					AD7503S	† AD
						see page 548
		400	±15	±15.5	HI1818A-2	† Harris
					HI1818A-5	Harris
				±15	DG508A	† Intersil
					DG508A	† Siliconix
						see page 561, 563
		450	±15	±15	DG508B	Intersil
					DG508C	Intersil
					DG508B	Siliconix
						see page 561, 563
					DG508C	Siliconix
						see page 561, 563
		1500	±15	±15	MN4708	Analogic
					HI508A-2	† Harris
		1800	±15	±15	HI508A-5	Harris
	JFET	300	±10	±15.5	LF11305	† National
					LF12305	National
					LF13305	National

† Military Temperature Range (-55°C to 125°C)

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INTERFACE—Analog Switches (cont)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source
Multiplexers (cont)						
8 channel	PMOS	150-250	±5	-20,5	DG501A	† Siliconix see page 552, 554
					DG501B	Siliconix see page 552, 554
					DG501C	Siliconix see page 555, 556
		150-400	±5	-20,5	3705	Fairchild
					SI3705	Siliconix see page 551
		150-800	±10	-20,10	DG503A	† Siliconix
		200-600	±5	-15,5	DG503B	Siliconix
DG501A	† Siliconix see page 552, 554					
200-800	±5	-15,5	DG501B	Siliconix see page 552, 554		
250-400	±5	-15,5	DG501C	Siliconix see page 555, 556		
			AM3705	† National National		
450	-15	-20	AM3705	† National National		
8 channel differential	CMOS	400	±15	±15	3708	Fairchild ITT
					ITT3708	ITT
8 channel differential	CMOS	400	±15	±15	AD7507J	AD see page 548
					AD7507K	AD see page 548
450	±15	±15	HI507-2	† Harris		
			HI507-5	Harris		
8 channel (DPST)	PMOS	500 and 6800	±5,±4	-12,5	IH5070M	† Intersil
					DG507A	† Siliconix see page 561, 563
with ring counter	PMOS	500 and 6800	±5,±4	-12,5	AD7507S	† AD see page 548
					AD7507T	† AD see page 548
8 channel differential	CMOS	1500	±15	±15	IH5070C	Intersil
					DG507B	Siliconix see page 561, 563
8 channel (DPST)	PMOS	500 and 6800	±5,±4	-12,5	DG507C	Siliconix see page 561, 563
					CRC2002	Collins
8 channel differential	CMOS	1500	±15	±15	1507M	† DDC
					HI507A-2	† Harris
with storage/counter	PMOS	1000	0 to -10	-28	MN4708D	Analogic
					1507C	DDC
16 channel	CMOS	400	±15	±15	HI507A-5	Harris
					4551	Teledyne P

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range, V	Supply Voltage	Device	Source
Multiplexers (cont)						
16 channel (continued)	CMOS	400	±15	±15	IH5060M	† Intersil
					DG506A	† Siliconix see page 561, 563
		450	±15	±15	AD7506J	AD see page 548
					AD7506K	AD see page 548
		1500	±15	±15	IH5060C	Intersil
DG506B	Siliconix see page 561, 563					
1800	±15	±15	DG506C	Siliconix see page 561, 563		
			AD7506	Siliconix		
16 channel with storage counter	PMOS	1000	0 to -18	-28	1506M	† DDC
					HI506A-2	† Harris
Crosspoint	PMOS	1000	0 to -18	-28	MN4716	Analogic
					1506C	DDC
Drivers	PMOS	1000	0 to -18	-28	HI506A-5	Harris
					4552	Teledyne P
CRC2001	Collins	4552	Teledyne P	4552	CRC2001	Collins
					RC4444	Raytheon see page 659, 660
RM4444	† Raytheon	see page 659, 660	MC3416	Motorola	SD5300	Signetics
					SD5300	Signetics
Drivers						
2 channel					D112C	Intersil
					D112M	† Intersil
					D113C	Intersil
					D113M	† Intersil
					D120C	Intersil
					D120M	† Intersil
					D121C	Intersil
					D121M	† Intersil
					D130A	† Siliconix
					D130B	Siliconix
					D139A	† Siliconix
					D139B	Siliconix
					D139C	Siliconix
					4 channel	
D129A	† Siliconix					
D129B	Siliconix					
4 channel for DMOS					SD5200	Signetics
4 channel with Decoder					D132A	† Siliconix
					D132B	Siliconix
6 channel					D123C	Intersil
					D123M	† Intersil
					D125C	Intersil
					D125M	† Intersil
					D123A	† Siliconix
					D123B	Siliconix
					D125A	† Siliconix
					D125B	Siliconix
					CDR125A	† Teledyne S
					CDR125B	Teledyne S

INTERFACE
Master Selection Guide

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† Military Temperature Range (-55°C to 125°C)

DT1 means four terminals with a pair of normally open and normally closed contacts.

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INTERFACE—Analog to Digital Converters

No. of Bits	Code	Full Temperature Range			Input Voltage Range	Reference Voltage	Supply Voltage	Comments	Device	Source
		Total Conversion Time μ s	Linearity Error \pm %FS	Total Error \pm %FS						
A/D Converters - Binary Output										
8	Binary	6	0.2	0.4	0 to -10	Internal	\pm 15.5	Successive Approx.	MN5123	Micro Net
		12	0.2	0.4	0 to -10	Internal	\pm 15.5	Successive Approx.	MN502	Micro Net
					0 to -10	Internal	\pm 12.5	Successive Approx.	MN508	Micro Net
					0 to -10	Internal	\pm 15.5	Successive Approx.	MN510	Micro Net
				0.8	0 to -10	Internal	\pm 12.5	Successive Approx.	MN508H	† Micro Net
					0 to -10	Internal	\pm 15.5	Successive Approx.	MN502H MN510H	† Micro Net † Micro Net
		40	0.2	—	—	External	-12.5	Successive Approx.	MM4356 MM5356	† National National
		100	0.2	0.8	0 to -10	Internal	12	Successive Approx.	MN5061 MN5061H	Micro Net † Micro Net
		1250	0.2	(0.5*)		20 μ a	\pm 5	Integrating	8700	Teledyne S
		—	—	—	0 to -10	-10	-12,-28	Requires resistors, comparators	CRC9501 CRC9502	Collins Collins
Complementary Binary 1.5										
			0.2	0.4	Various	Internal	\pm 15.5	Successive Approx.	MN5100 MN5100H	Micro Net Micro Net
		12	0.2	0.4	0 to 10	Internal	\pm 15.5	Successive Approx.	MN504	Micro Net
				0.8	0 to 10	Internal	\pm 15.5	Successive Approx.	MN504H	† Micro Net
		100	0.2	0.8	0 to 10	Internal	12.5-12	Successive Approx.	MN5066 MN5066H	Micro Net † Micro Net
Complementary Offset Binary										
		6	0.2	0.4	0 to -10	Internal	\pm 15.5	Successive Approx.	MN5120	Micro Net
		12	0.2	0.4	5 to -5	Internal	\pm 15.5	Successive Approx.	MN503 MN511	Micro Net Micro Net
					5 to -5	Internal	\pm 12.5	Successive Approx.	MN509	Micro Net
					10 to -10	Internal	\pm 15.5	Successive Approx.	MN507	Micro Net
				0.8	5 to -5	Internal	\pm 15.5	Successive Approx.	MN503H MN511H	† Micro Net † Micro Net
		100	0.2	0.8	5 to -5	Internal	12.5-12	Successive Approx.	MN5065 MN5065H	Micro Net † Micro Net
Offset Binary										
		6	0.2	0.4	-5 to 5	Internal	\pm 15.5	Successive Approx.	MN5121	Micro Net
					-10 to 10	Internal	\pm 15.5	Successive Approx.	MN5122	Micro Net
		100	0.2	0.8	5 to -5	Internal	12	Successive Approx.	MN5060 MN5060H	Micro Net † Micro Net

Military Temperature Range (-55°C to 125°C)

Note: The total error is the manufacturers specified value. If that isn't stated, the value shown in parentheses is calculated by summing the linearity error, the temperature error (temperature coefficients times the maximum temperature deviation from 25°C) plus 1/2 LSB quantizing error.

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INTERFACE—Analog to Digital Converters (cont)

No. of Bits	Code	Full Temperature Range			Input Voltage Range	Reference Voltage	Supply Voltage	Comments	Device	Source										
		Total Conversion Time μ s	Linearity Error \pm %FS	Total Error \pm %FS																
A/D Converters - Binary Output (cont)																				
8	Complementary Binary/Complementary Offset Binary	2.5	0.5	(0.37)	Various	Internal	$\pm 15,5$	Successive Approx.	ADC82	Burr-Brown										
	Binary/Complementary Binary	8	0.2	(0.67-1.6)	Various	Internal	$\pm 15,5$	Successive Approx.	AD-02	PMI										
10	Binary	16*	0.2	(0.4)	0 to 10	-10	5-15,15	Successive Approx., 8-bit resolution	AD7570J see page 543	AD										
		20*	0.05	(0.15)	0 to 10	-10	5-15,15	Successive Approx.	AD7570L see page 543	AD										
	5000	0.05	(0.18*)	10 μ a	20 μ a	± 5	Integrating	8701	Teledyne S											
	Complementary Binary/ Complementary Offset Binary	21	0.048	(0.29)	Various	Internal	$\pm 15,5$	Successive Approx.	ADC80A-10	Burr-Brown										
11	Binary	12	—	0.32	0 to 10	Internal	$\pm 15,5$	Successive Approx.	876-U10	† Beckman										
	Offset Binary	12	—	0.32	-5 to 5	Internal	$\pm 15,5$	Successive Approx.	876-B5	† Beckman										
					-10 to 10	Internal	$\pm 15,5$	Successive Approx.	876-B10	† Beckman										
12	Binary	13	0.0125	0.1	0 to -10	-10	$\pm 15,5$	Successive Approx.	MN5213 MN5213H	Micro Net † Micro Net										
					0 to -10	Internal	$\pm 15,5$	Successive Approx.	MN5210 MN5210H	Micro Net † Micro Net										
		15	—	0.02	10 or ± 10		$\pm 15,5$	Building Block	AD1000	National										
		50	0.0125	0.1	0 to -10	-10	$\pm 15,5$	Successive Approx.	MN5203 MN5203H	Micro Net † Micro Net										
											0.4	0 to -10	Internal	$\pm 15,5$	Successive Approx.	MN5200	Micro Net			
		50	0.012	—	—		3 to 15	Bipolar or Unipolar	AD1210	National										
		175	0.0125	0.4	0 to -10	Internal	$\pm 12,5-12$	Successive Approx.	MN5250 MN5250H	Micro Net Micro Net										
											20ms	0.0125	(0.11*)	10 μ a	20 μ a	± 5	Integrating	8702	Teledyne S	
			0.012	(0.44*)	± 10		$\pm 15,5$	Dual Slope, Analog and Digital Chips	LF11300 MM5863	National National										
		Complementary Binary	13	0.0125	0.4	0 to 10	Internal	$\pm 15,5$	Successive Approx.	MN5216 MN5216H	Micro Net † Micro Net									
												50	0.0125	0.4	0 to 10	Internal	$\pm 15,5$	Successive Approx.	MN5206 MN5206H	Micro Net † Micro Net
												175	0.0125	0.4	0 to 10	Internal	$\pm 12,5-12$	Successive Approx.	MN5253 MN5253H	Micro Net † Micro Net
30	Complementary Offset Binary	13	0.0125	0.1	-5 to +5	-10	$\pm 15,5$	Successive Approx.	MN5214 MN5214H	Micro Net † Micro Net										
					-10 to +10	-10	$\pm 15,5$	Successive Approx.	MN5215 MN5215H	Micro Net † Micro Net										

† Military Temperature Range (-55°C to 125°C) * — Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE—Analog to Digital Converters (cont)

No. of Bits	Code	Full Temperature Range			Input Voltage Range	Reference Voltage	Supply Voltage	Comments	Device	Source							
		Total Conversion Time μ s	Linearity Error \pm %FS	Total Error \pm %FS													
A/D Converters - Binary Output (cont)																	
12	Complementary Offset Binary	-5 to +5	Internal	± 15.5	Successive Approx.	Internal	± 15.5	Successive Approx.	MN5211 MN5211H MN5212 MN5212H	Micro Net † Micro Net Micro Net † Micro Net							
					-10 to +10				-10	Successive Approx.	MN5204 MN5204H	Micro Net † Micro Net					
		50	0.0125	0.1	-5 to +5	-10 to +10	-10	± 15.5	Successive Approx.	MN5205 MN5205H	Micro Net † Micro Net						
					-5 to +5	Internal	± 15.5	Successive Approx.	MN5201 MN5201H	Micro Net † Micro Net							
		175	0.0125	0.4	-5 to +5	-10 to +10	Internal	± 15.5	Successive Approx.	MN5202 MN5202H	Micro Net † Micro Net						
					5 to -5	Internal	$\pm 12.5-12$	Successive Approx.	MN5251 MN5251H	Micro Net † Micro Net							
			10 to -10	Internal	$\pm 12.5-12$	Successive Approx.	MN5252 MN5251H	Micro Net † Micro Net									
12	Complementary Binary/Complementary Offset Binary	6	0.048	(0.19)	Various	Internal	± 15.5	10 bit resolution	ADC85-10	Burr-Brown							
				(0.24)	Various	Internal	± 15.5	10 bit resolution	ADC85C-10	Burr-Brown							
		8	0.0125	(0.21)	Various	Internal	± 15.5	Successive Approx.	ADC-HY12	Datel							
					Various	Internal	± 15.5	12 bit resolution	ADC85-12	Burr-Brown							
		10	0.012	(0.12)	Various	Internal	± 15.5	12 bit resolution	ADC85C-12	Burr-Brown							
					(0.14)	Various	Internal	± 15.5	12 bit resolution	ADC85C-12	Burr-Brown						
25	0.012	(0.22)	Successive Approx.	Various	Internal	± 15.5		ADC80A-12	Burr-Brown								
	Binary, Offset Binary, two's Complement	24*	0.1	(0.32)	-2.5 to +2.5 -5 to +5 -10 to +10	Internal	± 15.5	Successive Approx.	AD124-09CW3	PMI							
16	Binary	250 ms	—	—	-15 to 4	Internal	± 15.5	Dual Slope, two device set	ICL7104 ICL8052	Intersil Intersil							
									Any	—	—	—	Internal	± 15.5	Building Block	ICL8052 ICL8053	Intersil Intersil
A/D Converters - Digital Output																	
2 ^{1/2}	1000	± 1.99	Internal	-15,5	V to f converter, LED Output	DM7700 DM8700	† National National										
						2 ^{1/2} -4 ^{1/2}	0 to 2	Internal	5 to 15	Ramp Type	MC1405 MC1505 MC14435 MC14435E	Motorola † Motorola Motorola † Motorola					
3 ^{1/2}	Adjustable	± 2	$\pm 2 \mu$ a	± 15	Dual Slope Multiplexed Output	MN2301	Analogic										
						50	-15 to +4	Internal	± 15.5	Dual Slope	ICL7101 ICL8052	Intersil Intersil					
10	80 ms $\pm 0.2, \pm 2$	± 7	± 12.5	± 12.5	Ramp Type Multiplex output	LD110 LD111	Siliconix Siliconix										
						$\pm 0.2, \pm 2$	± 7	± 12.5	Ramp Type Serial or multiplexed parallel BCD output	LD111 LD114	Siliconix Siliconix						
										300	$\pm 0.2, \pm 2$	Current	± 14	Dual Slope	MC904	IPI	
4 ^{1/2}	166	-15 to +4	Internal	± 15.5	Dual Slope	ICL7103	Intersil										
						—	± 10	Internal	± 15.5	Dual Slope, separate analog and digital	LF1130 MM5330	National National					

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Master Selection Guide

† Military Temperature Range (-55°C to 125°C) * — Typical Values

Note: The total error is the manufacturers specified value. If that isn't stated, the value shown in parentheses is calculated by summing the linearity error, the temperature error (temperature coefficients times the maximum temperature deviation from 25°C) plus 1/2 LSB quantizing error.

ABBREVIATIONS OF COMPANY NAMES

AD	Analog Devices
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
AMS	Advanced Memory Systems
Analogic	Analogic Corp.
Beckman	Beckman Instruments, Helipot Division
Burr-Brown	Burr-Brown Research
Cermetek	Cermetek
CMA	Consumer Microcircuits of America
Collins	Collins Radio
Datel	Datel Systems
DDC	ILC Data Devices Corp.
EA	Electronic Arrays
EMM/Semi	EMM Semi, Div. of Electronic Memories & Magnetics
Exar	Exar Integrated Systems
Fairchild	Fairchild Semiconductor
Ferranti	Ferranti Electric
GI	General Instrument
Harris	Harris Semiconductor
Hitachi	Hitachi America, Ltd.
Hughes	Hughes Aircraft Co., MOS Division
Hybrid Sys.	Hybrid Systems
IMI	International Microcircuits, Inc.
Intech	Intech
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
IPI	Integrated Photomatrix, Inc.
ITT	ITT Semiconductors
Lithic Sys.	Lithic Systems
Litronix	Litronix
LSI Comp.	LSI Computer Systems
Micro Net	Micro Networks
Micropac	Micropac Industries
Micro Power	Micro Power Systems
Mitsubishi	Mitsubishi International
MMI	Monolithic Memories, Inc.
MOS	MOS Technology
Mostek	Mostek
Motorola	Motorola Semiconductor
National	National Semiconductor
NCR	National Cash Register, Microelectronics Div.
NEC	NEC Microcomputers
Nippon	Nippon Electric Co.
Nitron	Nitron
Nortec	Nortec Electronics
NPC	Nucleonic Products Co.
OKI	OKI Electronics of America, Inc.
Panasonic	Panasonic, Matsushita Electric Corp.
Plessey	Plessey Semiconductors
PMC	Power Monolithics Co.
PMI	Precision Monolithics, Inc.
Ragen	Ragen Semiconductor
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
Reticon	Reticon
Rockwell	Rockwell International, Microelectronic Div.
Sanken	Sanken Electric
SGS	SGS-ATES Semiconductor
Signetics	Signetics
Silicon G	Silicon General
Siliconix	Siliconix
SMC	SMC Microsystems Corp.
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSS	Solid State Scientific
SW	Stewart-Warner Microcircuits
Synertek	Synertek
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
TI	Texas Instruments
TMX	TMX, Inc.
Toshiba	Toshiba
TRW	TRW
Transitron	Transitron Electronics
Western	Western Digital

INTERFACE—Digital to Analog Converters

No. of Bits	Code	Full Temperature Range			Output Voltage	Reference Voltage	Supply Voltage	Comments	Device	Source	
		Settling Time ($\pm 1/2$ LSB) μ s	Linearity Error \pm %FS	Total Error \pm %FS							
D/A Converters											
6	Binary	0.25*	0.78	(0.88*)	0 to -2 ma	2 ma	-15, 5	Multiplying, Current output. No output op amp	SSS1408A-6	PMI	
		0.3*	0.78	(0.88*)	0 to -2 ma	2 ma	-15, 5	Multiplying, Current output. No output op amp	MC1408-6	Motorola	
	Complementary Binary	0.3	0.78	(1.18)	2 to 0 ma	2 ma	-15, 5	Multiplying, Current output. No output op amp	MC1406	Motorola	
				(1.68)	2 to 0 ma	2 ma	-15, 5	Multiplying, Current output. No output op amp	MC1506	† Motorola	
	3	0.3	0.3	(0.7)	-5 to +5 -10 to +10	Internal	\pm (12-18)	Unipolar or Bipolar	DAC-01A	† PMI	
				(1.17)	-5 to +5 -10 to +10 0 to +10	Internal Internal	\pm (12-18) \pm (12-18)	Unipolar or Bipolar Unipolar	DAC-01C DAC-01H	PMI PMI	
		(1.25)	-5 to +5 -10 to +10 0 to +10	Internal Internal	\pm (12-18) \pm (12-18)	Unipolar or Bipolar Unipolar	DAC-01	† PMI			
							DAC-01F	† PMI			
		(1.65)	-5 to +5 -10 to +10	Internal	\pm (12-18)	Unipolar or Bipolar	DAC-01B	† PMI			
		23*	0.78	(1.58)	0 to -10 -5 to +5	Internal	\pm 15, 5	Bipolar or Unipolar	MN301 MN301H	Micro Net Micro Net	
	7	Binary	0.25*	0.39	(0.49*)	0 to -2 ma	2 ma	-15, 5	Multiplying, Current output. No output op amp	SSS1408A-7	PMI
			0.3*	0.39	(0.49*)	0 to -2 ma	2 ma	-15, 5	Multiplying, Current output. No output op amp	MC1408-7	Motorola
Binary/Complementary Binary		0.1*	0.39	(0.78)	2 ma	2 ma	\pm (5-18)	Multiplying, Complementary current output	DAC-08CZ	PMI	
8	BCD	23	0.5	0.5			0 to -9.900 Internal \pm 15 Unipolar	MN3010	Micro Net		
								MN3010H	† Micro Net		
	Binary	0.25*	0.19	(0.29*)	0 to -2 ma	2 ma	-15, 5	Multiplying, Current output. No output op amp	SSS1408A-8	PMI	
				(0.39*)	0 to -2 ma	2 ma	-15, 5	Multiplying, Current output. No output op amp	SSS1508A-8	† PMI	
		0.3*	0.19	(0.29)	0 to -2 ma	2 ma	-15, 5	Multiplying, Current output. No output op amp	AD559K see page 538	AD	
				(0.39)	0 to -2 ma	2 ma	-15, 5	Multiplying, Current output. No output op amp	DAC-IC8BC MC1408-8	Datel Motorola	
	10	—	0.2	0.2	+10, \pm 5y, 2 ma	Internal	\pm 15	Unipolar or Bipolar	DA800	National	
									1	0.2	0.4
			1.0	0 to +3.984	Internal	\pm 15	Unipolar	MN3008H	† Micro Net		

† Military Temperature Range (-55°C to 125°C) * Typical values

Note: Total Error is the manufacturer's specified value. Where that wasn't available, the value shown in parentheses is sum of the linearity error plus the temperature error (temperature coefficients times the maximum temperature deviation from 25°C).

INTERFACE—Digital to Analog Converters (cont)

No. of Bits	Code	Full Temperature Range			Output Voltage	Reference Voltage	Supply Voltage	Comments	Device	Source
		Setting Time ($\pm 1/2$ LSB) μ s	Linearity Error \pm %FS	Total Error \pm %FS						
D/A Converters (cont)										
8	Binary	23	0.19	0.39	0 to 10	Internal	± 15	Unipolar	MN3002	Micro Net
			0.2	—	0 to +10	Internal	15, 5	Unipolar, storage register	MN328	Micro Net
		27	0.19	(0.28)	0 to 5	Internal	± 15	Unipolar	845-U5	Beckman
	52	0.19	(0.28)	0 to 10	Internal	± 15	Unipolar	845-U10	Beckman	
	Complementary Binary	0.1	0.2	0.39	0 to -9.961	+10	5, 15	Unipolar. No output op amp	MN306	Micro Net
					(0.59)	0 to -10	Internal	$\pm 5, 15$	Unipolar. No output op amp	MN333
		0.225*	0.2	(0.47)	$\pm 5, 10$ or $\pm 2.5, 5$	Internal	$\pm (6-18)$	Unipolar or Bipolar. No output amplifier	DAC-100CCT	PMI
					(0.56)	$\pm 5, 10$ or $\pm 2.5, 5$	Internal	$\pm (6-18)$	Unipolar or Bipolar. No output amplifier	DAC-100CCQ
		0.3	(0.84)	$\pm 5, 10$ or $\pm 2.5, 5$	Internal	$\pm (6-18)$	Unipolar or Bipolar. No output amplifier	DAC-100DDT	PMI	
					(1.02)	$\pm 5, 10$ or $\pm 2.5, 5$	Internal	$\pm (6-18)$	Unipolar or Bipolar. No output amplifier	DAC-100DDQ
	23	0.19	0.39	0 to -10	Internal	± 15	Unipolar	MN3000	Micro Net	
	Offset Binary	23	0.19	0.39	5 to -5	Internal	± 15	Bipolar	MN3001	Micro Net
					10 to -10	Internal	± 15	Bipolar	MN3006	Micro Net
		0.2	—	-4.961 to +5	Internal	$\pm 15, 5$	Bipolar, storage register	MN328B	Micro Net	
		45	0.19	—	10 to -10	Internal	$\pm 15, 5$	Bipolar	MN335 MN335H	Micro Net † Micro Net
52		0.19	(0.28)	-5 to +5	Internal	± 15	Bipolar	845-B5	Beckman	
102	0.19	(0.28)	-10 to +10	Internal	± 15	Bipolar	845-B10	Beckman		
Binary/Complementary Binary	0.135	0.1	(0.29)	2 ma	2 ma	$\pm (5-18)$	Multiplying, Complementary current output	DAC-08AZ	† PMI	
				0.1*	0.19	(0.36)	2 ma	2 ma	$\pm (5-18)$	Multiplying, Complementary current output
	3.0	0.2	(0.3)	4 ma	-10 to +10	3-10	Multiplying	DAC331-8	† Hybrid Sys	
Complementary Binary/Complementary Offset Binary	0.2	0.2	0.2	$\pm 2, 4$	Internal	± 15	Unipolar or Bipolar	DAC90L DAC90T	Burr-Brown † Burr-Brown	
				8 Bit plus Sign or 9 bit Binary	23	0.2	—	$+1/2$ Vref to $-1/2$ Vref	-13 to +13	± 15
Binary Ladder	1.5*						Switch/Ladder Network	HI1085	Harris	
	3						Switch/Ladder Network	HI1080	† Harris	
9	Complementary Binary	0.300	0.1	(0.19)	$\pm 5, 10$ or $\pm 2.5, 5$	Internal	$\pm (6-18)$	Unipolar or Bipolar. No output amplifier	DAC-100AAQ	† PMI
				(0.28)	$\pm 5, 10$ or $\pm 2.5, 5$	Internal	$\pm (6-18)$	Unipolar or Bipolar. No output amplifier	DAC-100BBQ	† PMI

† Military Temperature Range (-55°C to 125°C) * Typical values

Bold face indicates additional data is provided on the page noted.

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INTERFACE—Digital to Analog Converters (cont)

No. of Bits	Code	Full Temperature Range			Output Voltage	Reference Voltage	Supply Voltage	Comments	Device	Source
		Settling Time ($\pm 1/2$ LSB) μ s	Linearity Error \pm %FS	Total Error \pm %FS						
D/A Converters (cont)										
9	Complementary Binary	0.300	0.1	(0.37*)	$\pm 5,10$ or $\pm 2,5,5$	Internal	$\pm(6-18)$	Unipolar or Bipolar. No output amplifier	DAC-100BCT	PMI
				(0.46)					DAC-100BCQ	† PMI
				(0.82)					DAC-100BDQ	† PMI
9	9 Bits plus Sign Offset Binary	15	0.1	(0.3)	$+V_{ref}$ to $-V_{ref}$	-13 to +13	$\pm 15,5$	Multiplying, Bipolar	MN411 MN411H	Micro Net Micro Net
				(0.3)					$+V_{ref}$ to $-V_{ref}$	-13 to +13
10	BCD	23	0.05	—	0 to -9.975	Internal	$\pm 5, 15$	Unipolar	MN319	Micro Net
	Binary	23	0.05	0.4	0 to +10	Internal	± 15	Unipolar	MN3005 MN3005H	Micro Net † Micro Net
		1.5*	—	—	0 to 5 or 10	Internal	$\pm(12$ to $18)$	Monotonicity- various model, 8-10 bits	DAC-03	PMI
	Complementary Binary	0.1	0.05	—	0 to -10	Internal	$\pm 15, 5$	Unipolar. No output op amp	MN325	Micro Net
		0.375	0.05	(0.14)	$\pm 5,10$ or $\pm 2,5,5$	Internal	$\pm(6-18)$	Unipolar or Bipolar. No output amplifier	DAC-100AAQ	† PMI
	(0.23)			DAC-100ABQ					† PMI	
	(0.32)			DAC-100ACT					PMI	
	(0.41)			DAC-100ACQ					† PMI	
	(0.77)			DAC-100ADQ					† PMI	
		2*	0.05	(0.1)	-1 to 1 ma 0 to -2 ma	Internal	± 15	Bipolar current output	DAC345I-10-BP	Hybrid Sys
				Internal		± 15	Unipolar current output	DAC345I-10-UP	Hybrid Sys	
		5*	0.05	(0.1*)	-5 to +5 0 to +10	Internal	± 15	Bipolar	DAC346V-10-BP	Hybrid Sys
				Internal		± 15	Unipolar	DAC346V-10-BP DAC346V-10-UP	† Hybrid Sys Hybrid Sys	
		23	0.05	0.4	0 to -10	Internal	± 15	Unipolar	MN3003 MN3003H	Micro Net † Micro Net
	Offset Binary	23	0.05	0.4	-5 to +5	Internal	± 15	Bipolar	MN3004 MN3004H	Micro Net † Micro Net
		45	0.05	0.4	-10 to +10	Internal	± 15	Bipolar	MN3007 MN3007H	Micro Net † Micro Net
	Binary/Offset Binary/Complement	0.5*	0.05	(0.11)	1 ma	-10 to +10	5-15	Multiplying, 10 bit linearity	AD7520L see page 541	AD
				(0.17)					1 ma	-10 to +10

† Military Temperature Range (-55°C to 125°C) * Typical values

Note: Total Error is the manufacturer's specified value. Where that wasn't available, the value shown in parentheses is sum of the linearity error plus the temperature error (temperature coefficients times the maximum temperature deviation from 25°C).

INTERFACE—Digital to Analog Converters (cont)

No. of Bits	Code	Full Temperature Range			Output Voltage	Reference Voltage	Supply Voltage	Comments	Device	Source								
		Settling Time ($\pm 1/2$ LSB) μ s	Linearity Error \pm %FS	Total Error \pm %FS														
D/A Converters (cont)																		
10	Binary/Offset Binary/Complement	1 ma	-10 to +5015	Multiplying, 9 bit linearity	1 ma	-10 to +10	5-15	Multiplying, 9 bit linearity	AD7520K	AD								
									see page 541	† AD								
		0.2	(0.25)	1 ma	-10 to +10	5-15	Multiplying, 8 bit linearity	AD7520T	† AD									
								see page 541										
		0.2	(0.32)	1 ma	-10 to +10	5-15	Multiplying, 8 Bit Linearity	AD7520J	AD									
								see page 541										
	3.0	0.05	(0.15)	4 ma	-10 to +10	3-10	Multiplying	DAC331-10	† Hybrid Sys									
	Binary, Magnitude and Sign	1.5*	0.1	(0.37)	± 5 or ± 10	Internal	$\pm(12-18)$	Monotonicity-10 bits	DAC-02AC	PMI								
					± 5 or ± 10	Internal	$\pm(12-18)$	Monotonicity-9 bits	DAC-02BC	PMI								
			0.2	(0.47)	± 5 or ± 10	Internal	$\pm(12-18)$	Monotonicity-8 bits	DAC-02CC	PMI								
									DAC-02DD	PMI								
Two's or One's Complement	1.5*	0.1	(0.37)	-5 to +5	Internal	$\pm(12-18)$	Monotonicity-10 bits	DAC-04AC	PMI									
				-10 to +10	Internal	$\pm(12-18)$	Monotonicity-9 bits	DAC-04BC	PMI									
		0.2	(0.47)	± 5 or ± 10	Internal	$\pm(12-18)$	Monotonicity-8 bits	DAC-04CC	PMI									
	DAC-04DD							PMI										
	11	Binary	4.5	0.05	0.25	0 to 10	Internal	± 15	Unipolar	848-U10	† Beckman							
										Offset Binary	4.5	0.05	0.25	-5 to 5	Internal	± 15	Bipolar	848-B5
7.5																		0.05
Offset Binary, 11 Bits plus sign	15	0.025	0.05	+Vref to -Vref	-10 to +10	$\pm 15, 5$	Multiplying type, Bipolar No output op amp	MN413	Micro Net									
								MN413H	† Micro Net									
	45	0.025	0.05	+Vref to -Vref	-10 to +10	$\pm 15, 5$	Multiplying type, Bipolar	MN412	Micro Net									
								MN412H	† Micro Net									
12	BCD	0.3/3*	0.025	(0.18)	Various	Internal	$\pm 15, 5$	Voltage and Current Outputs	DAC-HY12DC	Datel								
									0.05	(0.14)	Various	Internal	$\pm 15, 5$	Voltage and Current Outputs	DAC85C/CCD	Burr-Brown		
			(0.18)	Various	Internal	$\pm 15, 5$	Voltage and Current Outputs	DAC80/CCD DAC85/CCD DAC-S-CCD							Burr-Brown † Burr-Brown DDC			
	0.5	0.05	—	0 to +0.999	Internal	± 15	Unipolar. No output op amp	MN311	Micro Net									
								MN311H	† Micro Net									
	1.2	0.025	(0.11)	0 to -2 ma, -1 to +1 ma	Internal	-15,5-15	Multiplying	AD563K/BCD	AD									
								see page 540										

† Military Temperature Range (-55°C to 125°C) * Typical values

Bold face indicates additional data is provided on the page noted.

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INTERFACE—Digital to Analog Converters (cont)

No. of Bits	Code	Full Temperature Range			Output Voltage	Reference Voltage	Supply Voltage	Comments	Device	Source	
		Setting Time ($\pm 1/2$ LSB) μ s	Linearity Error \pm %FS	Total Error \pm %FS							
D/A Converters (cont)											
12	BCD	1.2	0.025	(0.12)	0 to -2 ma, -1 to +1 ma	Internal	-15,5-15	Multiplying	AD563T/BCD see page 540	† AD	
				(0.32)	0 to -2 ma, -1 to +1 ma				Internal	-15,5-15	Multiplying
		3.5	0.01	(0.1)	0 to -2 ma, -1 to +1 ma	+10	-15,5-15	Unipolar or Bipolar, current output	AD562SD/BCD see page 539	† AD	
									AN562ID/BCD	Analogic	
		0.05	(0.1)	0 to -2 ma, -1 to +1 ma	+10	-15,5-15	Unipolar or Bipolar, current output	AD562AD/BCD see page 539	AD		
								AD562KD/BCD see page 539	AD		
		AN562AD/BCD	Analogic								
			AN562KD/BCD	Analogic							
		35	0.05	0.3	0 to -10/10	Internal	± 15	Unipolar	MN3202	Micro Net	
									Binary	0.5	0.0125
MN312H	† Micro Net										
3	0.0125	1.0	0 to -1.5 ma	+10	$\pm 15, 5$	Unipolar, current output	MN366	Micro Net			
							0.025	1.0	0 to -1.5 ma	+10	$\pm 15, 5$
5	0.012	—	10, $\pm 10y$ 2 ma	Internal	$\pm 15,5$	Unipolar or Bipolar	DAC1200	National			
							4 ms	0.0125	—	Pulse width	Internal
Binary/Offset Binary/Complement- s	0.5*	0.05	(0.11)	Current	-10 to +10	5-15	Multiplying, 10 bit linearity	AD7521L see page 541	AD		
								Current	-10 to +10	15,5-15	Multiplying, 10 bit linearity
				(0.17)	Current	-10 to +10	5-15	Multiplying, 10 bit linearity	AD7521U see page 541	† AD	
									Current	-10 to +10	15,5-15
				0.1	(0.16)	Current	-10 to +10	5-15	Multiplying, 9 bit linearity	AD7521K see page 541	AD
										Current	-10 to +10
				(0.22)	Current	-10 to +10	5-15	Multiplying, 9 bit linearity	AD7521T see page 541	† AD	

† Military Temperature Range (-55°C to 125°C) * Typical values

Note: Total Error is the manufacturer's specified value. Where that wasn't available, the value shown in parentheses is sum of the linearity error plus the temperature error (temperature coefficients times the maximum temperature deviation from 25°C).

INTERFACE—Digital to Analog Converters (cont)

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No. of Bits	Code	Full Temperature Range			Output Voltage	Reference Voltage	Supply Voltage	Comments	Device	Source		
		Settling Time ($\pm 1/2$ LSB) μ s	Linearity Error \pm %FS	Total Error \pm %FS								
D/A Converters (cont)												
12	Binary/Offset	Current	—10 to +10	0.15	0.15	Multiplying, 9 bit linearity			AD7522T see page 542	† AD		
				0.2	(0.25)	Current	—10 to +10	5-15	Multiplying, 8 bit linearity	AD7521J see page 541	AD	
						Current	—10 to +10	15,5-15	Multiplying, 8 bit linearity	AD7522J see page 542	AD	
				(0.32)		Current	—10 to +10	5-15	Multiplying, 8 bit linearity	AD7521S see page 541	† AD	
						Current	—10 to +10	15,5-15	Multiplying, 8 bit linearity	AD7522S see page 542	† AD	
			1.2*	0.006	(0.14)	—2/+1 ma	Internal	—15,5-15	Multiplying	AD7563K/BIN	AD	
					(0.21)	—2/+1 ma	Internal	—15,5-15	Multiplying	AD563T/BIN see page 540	† AD	
					(0.41)	—2/+1 ma	Internal	—15,5-15	Multiplying	AD563S/BIN see page 540	† AD	
				0.012	(0.19)	—2/+1 ma	Internal	—15,5-15	Multiplying	AD563J/BIN see page 540	AD	
				3.5	0.006	(0.11)	0 to —2 ma —1 to +1 ma	+10	—15,5-15	Unipolar or Bipolar	AD562SD/BIN see page 539	† AD
										AN562SD/BIN	† Analogic	
					0.0125	(0.05)	0 to —2 ma —10 to +1 ma	+10	—15,5-15	Unipolar or Bipolar	AD562KD/BIN see page 539	AD
										AN562KD/BIN	Analogic	
					(0.06)	0 to —2 ma —10 to +1 ma	+10	—15,5-15	Unipolar or Bipolar	AD562AD/BIN see page 539	AD	
										AN562AD/BIN	Analogic	
	Binary/Complementary Binary	35	0.0125	0.3	0 to —10/10	Internal	± 15	Unipolar	MN3200	Micro Net		
	Binary/Offset Binary	75	0.024	—	0 to 10	—10 to 10	Internal	± 15	Unipolar or Bipolar	872-D1	† Beckman	
					0 to 10	—10 to 10	Internal	± 15	Unipolar or Bipolar	872-D2	† Beckman	
	Complementary Binary	2*	0.0125	(0.1*)	0 to —2 ma	Internal	± 15	Unipolar	DAC345I-12-UP	Hybrid Sys		
		5*	0.0125	(0.1*)	0 to +10	Internal	± 15	Unipolar	DAC346V-12-UP DAC346V-12-UP	Hybrid Sys † Hybrid Sys		
		7	0.0125	0.1	0 to +9.9976	+10	$\pm 15, 5$	Unipolar	MN362	Micro Net		
			0.025	0.25	0 to +9.9976	+10	$\pm 15, 5$	Unipolar	MN362H	Micro Net		
		70	0.0125	0.5	0 to +10	Internal	± 15	Unipolar	MN371	Micro Net		
									MN371H	† Micro Net		

† Military Temperature Range (—55°C to 125°C) * Typical values

Bold face indicates additional data is provided on the page noted.

INTERFACE—Digital to Analog Converters (cont)

No. of Bits	Code	Full Temperature Range			Output Voltage	Reference Voltage	Supply Voltage	Comments	Device	Source			
		Setting Time ($\pm 1/2$ LSB) μ s	Linearity Error \pm %FS	Total Error \pm %FS									
D/A Converters (cont)													
12	Complementary Binary/Offset Binary	5*	0.0125	—	5/10/ $\pm 2.5/\pm 5/\pm 10$	Internal	± 15	Unipolar or Bipolar	MN3850 MN3850H	Micro Net † Micro Net			
	Complementary Offset Binary	1*	0.0125	(0.1*)	-1 to +1 ma	Internal	± 15	Bipolar, current output	DAC345I-12-BP DAC345I-12-BP	Hybrid Sys † Hybrid Sys			
		35	0.0125	0.3	$\pm 5/\pm 10$	Internal	± 15	Bipolar	MN3201	Micro Net			
	Complementary/Complementary Offset Binary	3/3*	0.012	(0.07)	Various V/I	Internal	$\pm 15, 5$	Unipolar or Bipolar	DAC85LD/CBI	Burr-Brown			
					(0.1)	Various V/I	Internal	$\pm 15, 5$	Unipolar or Bipolar	DAC85C/CBI DAC-S-CBI	Burr-Brown DDC		
					(0.13)	Various V/I	Internal	$\pm 15, 5$	Unipolar or Bipolar	DAC85/CBI	Burr-Brown		
					(0.15)	Various V/I	Internal	$\pm 15, 5$	Unipolar or Bipolar	DAC80/CBI DAC-SC-CBI	Burr-Brown DDC		
					(0.21)	Various V/I	Internal	± 15	Unipolar or Bipolar	DAC-HY12BC	Datel		
	Offset Binary	3	0.0125	1.0	+0.75 to -0.75 ma	+10	$\pm 15, 5$	Bipolar, current output	MN364	Micro Net			
					0.025	1.0	+0.75 to -0.75 ma	+10	$\pm 15, 5$	Bipolar, current output	MN364H	† Micro Net	
		5*	0.0125	(0.1*)	-5 to +5	Internal	± 15	Bipolar	DAC346V-12-BP DAC346V-12-BP	Hybrid Sys † Hybrid Sys			
		7	0.0125	0.1	-10 to +9.9951	+10	$\pm 15, 5$	Bipolar	MN360	Micro Net			
					0.025	0.25	-10 to +9.9951	+10	$\pm 15, 5$	Bipolar	MN360H	† Micro Net	
		70	0.0125	0.5	-10 to +10	Internal	± 15	Bipolar	MN370 MN370H	Micro Net † Micro Net			
		13	Binary	20	—	0.1	± 10	± 10	$-25, \pm 15$	Multiplying	877-69CD2 877-69MD2	Beckman † Beckman	
0.25	± 10					± 10	$-25, \pm 15$	Multiplying	877-69CD1 877-69MCD1	Beckman † Beckman			
Complementary Binary/Complementary Offset Binary	0.1/0.37		0.0125	0.0125	Various	Internal	$\pm 5, 15$		SDAC-12	DDC			
					0.025	0.025	Various	Internal	$\pm 5, 15$		SDAC-11	DDC	
					0.05	0.05	Various	Internal	$\pm 5, 15$		SDAC-10	DDC	
16	BCD		35	0.005	0.3	-5, -10, 5, 1-0	Internal	± 15	Unipolar	MN3300	Micro Net		
		100*				0.03	(0.004)	0 to -2 ma	Internal	$\pm 15, 5$	Unipolar	DAC70/CCD	Burr-Brown
						0.005	(0.006)	0 to -2 ma	Internal	$\pm 15, 5$	Unipolar	DAC70C/CCD	Burr-Brown
	Complementary Binary	100*	0.003	(0.004)	0 to -2 ma	Internal	$\pm 15, 5$	Unipolar	DAC70/CSB	Burr-Brown			

† Military Temperature Range (-55°C to 125°C) * Typical values

Note: Total Error is the manufacturer's specified value. Where that wasn't available, the value shown in parentheses is sum of the linearity error plus the temperature error (temperature coefficients times the maximum temperature deviation from 25°C).

INTERFACE—Digital to Analog Converters (cont)

No. of Bits	Code	Full Temperature Range			Output Voltage	Reference Voltage	Supply Voltage	Comments	Device	Source
		Settling Time ($\pm 1/2$ LSB) μ s	Linearity Error \pm %FS	Total Error \pm %FS						
D/A Converters (cont)										
16	Complementary Binary	0 to -2 ma	Internal	$\pm 15,5$	Unipolar				DAC70C/CSB	Burr-Brown
	Complementary Offset Binary	100*	0.003	(0.004)	± 1 ma	Internal	$\pm 15,5$	Bipolar	DAC70/COB	Burr-Brown
			0.005	(0.006)	± 1 ma	Internal	$\pm 15,5$	Bipolar	DAC70C/COB	Burr-Brown

† Military Temperature Range (-55°C to 125°C)

* Typical values

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INTERFACE—Display Drivers (cont)

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Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line
Display Drivers (cont)				Display Drivers (cont)				Display Drivers (cont)			
3-Digit Gas Discharge Display Anode Driver	MC3495 MC3496	Motorola Motorola		6-Digit MOS to LED Cathode Driver (continued)	LBC1060 MC75492 DS75492 DS75494 DS8870 DS8892 N583 SN75492 SN75494	Litronix Motorola National National National National Signetics TI TI		5-Segment MOS to LED Anode Driver	DS8861	National	100
4-Digit Gas Discharge Display Anode Driver	UDN-6144A	Sprague						8-Segment MOS to LED Anode Driver	HD2902 ITT509 LBC1070 LBC1071 MC676 DS8867	Hitachi ITT Litronix Litronix Motorola National	
5-Digit Gas Discharge Display Anode Driver	UHD-490 UHP-490	† Sprague Sprague						BCD-To-Decimal Decoder/Driver (Nixie Driver)	5441 7441 HD2518 MC5441 MC676 MC7441 DM5441A DM7441A H158 N7441 382A/C 382B/M	† Fairchild Fairchild Hitachi † Motorola Motorola Motorola † National National SGS Signetics Teledyne S † Teledyne S	110
6-Digit Gas Discharge Display Anode Driver	ITT512 DS7891 DS8891 UDN-6164A UHD-491 UHP-491 UHP-495 SN75481	ITT † National National Sprague † Sprague Sprague Sprague TI	10	7-Digit MOS to LED Cathode Driver	ITT546A DS8844 SN75497	ITT National TI	60				
7-Digit Gas Discharge Display Anode Driver	MC34090 MC34094	Motorola Motorola		7-Digit MOS to LED Cathode Driver, with low battery indicator	DS8866 DS8877	National National		BCD-To-Decimal Decoder/Driver with Blanking (for cold cathode indicator tubes)	74141 HD2558 ITT54141 ITT74141 DM54141 DM74141 N74141 SN74141	Fairchild Hitachi † ITT ITT † National National Signetics TI	120
8-Digit Gas Discharge Display Anode Driver	DS7887 DS8887 DS7897 DS8897 UDN-6184A	† National National † National National Sprague	20	8-Digit MOS to LED Cathode Driver	HD2903 ITT508 ITT514 ITT525 LBC1050 DS8863 DS8865 DS8871 DS8963	Hitachi ITT ITT ITT Litronix National National National National	70				
10-Digit Gas Discharge Display Anode Driver	ITT504	ITT		8-Digit LED Driver (for use with G.I. C550-554 Calculator Series)	ITT7103	ITT		BCD-To-Decimal Decoder/Driver (for lamps)	ITT380-1 ITT380-5 380A/C 380B/M 381A/C 381B/M	† ITT ITT Teledyne S † Teledyne S Teledyne S † Teledyne S	130
5-Segment Gas Discharge Display Cathode Driver	DVR-01 UHP-480	PMI Sprague		9-Digit MOS to LED Cathode Driver	ITT526 ITT548 DS8855 DS8973 DS8974 SN75498	ITT ITT National National National TI	80				
7-Segment Gas Discharge Display Cathode Driver, with BCD Decoder	DS7885 DS8885 UHP-481	† National National Sprague		9-Digit MOS to LED Cathode Driver, with low battery indicator	DS8864	National					
7-Segment Gas Discharge Display Cathode Driver, with BCD Decoder	DS7880 DS8880 DS8884 DM8880 SN75480	† National National National Signetics TI	30	9-Digit MOS to LED Cathode Driver with shift register decoding	DS8874 DS8876 DS8879	National National National					
8-Segment Gas Discharge Display Cathode Driver	ITT505 MC3491 DS7889 DS8889 UDN-7183A UDN-7186A ULN-7184A UHP-482	ITT Motorola † National National Sprague Sprague Sprague Sprague		12-Digit MOS to LED Cathode Driver (for National Calculators)	DS8868 DS8873	National National					
4-Digit CMOS to LED Cathode Driver	DS8658	National	40	4-Segment MOS to LED Anode Driver	75491C ITT491 ITT501 ITT503 ITT507 ITT517 MC75491 DS7895 DS8895 DS75491 DS75493 SN75491 SN75493	Fairchild ITT ITT ITT ITT ITT Motorola † National † National National National TI TI	90				
7-Segment CMOS to LED Driver	DS8651 DS8659	National National									
6-Digit MOS to LED Cathode Driver	9664C 75492C ITT492 ITT500 ITT502 ITT506 ITT510 LS1060 (continued)	Fairchild Fairchild ITT ITT ITT ITT ITT Lithic Sys	50								

† Military Temperature Range (-55°C to 125°C)

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Interface—Error Checking Circuits, Encoder-Decoders

Function		Max. Serial Data Rate KHz	Supply Voltage	Device	Source		
Error checking Circuits							
Programmable CRC (Cyclic Redundancy Character) Encoder-Decoder. Generates and checks up to 8 different polynomials of up to 16 terms each.		1	-12,5	S9544	AMI		
CRCC Generator				9401C 9401M MC8500	Fairchild † Fairchild Motorola		
Deskew-Queue Register				MC8520	Motorola		
Error Detection/Correction Circuit (ECL)		—	-5.2	MC10163 MC10193	Motorola Motorola		
ERROR Pattern Register				MC8501	Motorola		
LRCC Data Register				MC8502	Motorola		
Single Error Hamming Code Detector and Generator		—	5	MC4041	Motorola		
Polynomial Generator				MC8506	Motorola		
Universal Polynomial Generator				MC8503	Motorola		
Universal Polynomial 4 Bit Generator				MC8504	Motorola		
No. of Keys	No. of Output Bits	Code	Max. Clock Rate KHz	Comments	Supply Voltage	Device	Source
Keyboard Encoder-Decoders							
16	4	1 of 16		Strobe output, Key rollover output	5	HD-0165	Harris
				2 of 8 keyboard to binary encoder, one of four row inputs and column inputs (telephone key pads) give binary output, strobe.	5	MC14419	Motorola
28	8 plus Parity	Mask, Programmable	50	4 X 8 matrix, N Key rollover, 2 Levels. Independent or expander for MCS1007. Repeat.	-12,5	MCS1008	MOS
48	4 lines			Keyboard Buffer, 8 x 6 matrix, 2 key rollover, 4 line data bus output		S2299	AMI
64	8 Plus Parity	Mask, Programmable	50	Odd Parity, N Key rollover, 9 X 8 matrix, 4 levels Repeat.	-12,5	MCS1007	MOS
88	8 plus Parity	Mask, Programmable	100	Programmable parity, strobe width, strobe Delay. Two key rollover. 8 X 11 matrix, 3 levels.	-12,5	AY52376 KR2376	GI SMC
90	10	Mask, Programmable	50	Two units give 180 keys. 9 X 10 matrix, N key rollover, 4 levels. Repeat	-12,5	MCS1009	MOS
90	9	Mask, Programmable	200	Programmable strobe width. 9 X 10 matrix. N or two key rollover. 4 levels. Repeat.	-12,5	MM5740	National
	10	Mask, Programmable		90 Key, 4 Mode, N Key rollover	-12,5	AY53600 KR3600	GI SMC
99	10	Mask, Programmable	250	9 X 9 matrix. N key rollover, 4 levels. No repeat.	-12,5	EA2000 EA2007	EA EA
	10			99 Key, 4 Mode Encoder	-12,5	EA2030	EA

† Military Temperature Range (-55°C to 125°C)

Major functions arranged alphabetically. See list at beginning of this section.

INTERFACE—Line Circuits

No. Per Device	Output	Party Line	Power Supply	Comments	Device	Source
Line Drivers—Single Ended						
2	±6v	No	±12	4 Input; RS232B, C; MIL188	N8T15	Signetics
	±8v	No	±12	RS232C; MIL188; CCITT V.24	75150C DS75150 RC75150 RM55150 SN75150	Fairchild National Raytheon † Raytheon TI
	TTL	No	5, 12	130 Ohm Twisted Pair	9621C 9621M 9621C 9621M RC9621 RM9621	AMD † AMD Fairchild † Fairchild Raytheon † Raytheon
	High Current	Yes	5	Emitter Follower Coax/Twisted Pair	8T13C 8T13M 55121M 75121C MC8T13 DS55121 DS75121 RC8T13 RM8T13 N8T13 S8T13 SN55121 SN75121	Fairchild † Fairchild † Fairchild Fairchild Motorola † National National Raytheon † Raytheon Signetics † Signetics † TI TI
				Coax/Twisted Pair; IBM360, 370	8T23C 75123C MC8T23 DS75123 RC8T23 RM8T23 N8T23 SN75123	Fairchild Fairchild Motorola National Raytheon † Raytheon Signetics TI
3	±6v	No	±12	RS232B/C, CCITT, MIL188	9616C 9616C 9616E 9616M	AMD Fairchild Fairchild † Fairchild
4	±6 to 9v	No	±9 to ±15	RS232C, CCITT V.24	MC1488 XR1488 HD1488 ITT1488 MC1488 DS1488 RC1488 MC1488 SG1488 SN75188	AMD Exar Harris ITT Motorola National Raytheon Signetics Silicon G TI
					TTL	No
		Yes	5	Three-State	RC8T09 RM8T09 N8T09 S8T09	Raytheon † Raytheon Signetics † Signetics
				4 Input AND, NAND; Three-State	DM7831 DM8831 DS7831	† AMD AMD † National (continued)

† Military Temperature Range (–55°C to 125°C) * Typical values

Bold face indicates additional data is provided on the page noted.

INTERFACE—Line Circuits (cont)

No. Per Device	Output	Party Line	Power Supply	Comments	Device	Source		
Line Drivers—Single Ended (cont)								
4	TTL	Yes		4 Input AND, NAND; Three-State (continued)	DS8831	National		
				DS7831 w/o V _{cc} Clamp	DS7832 DS8832	† National National		
Line-Drivers—Differential								
2	High-Current TTL	No	5	40 ma, Active Pull-up/Pull-down	9612C 9612M	Fairchild † Fairchild		
				50 ma, Active Pull-up/Pull-down	9612EC	Fairchild		
				40 ma, Open Collector/Active Pull-up	9614C 9614M 9614C 9614M	AMD † AMD Fairchild † Fairchild		
					ITT9614-1 ITT9614-5 SN55114 SN75114	† ITT ITT † TI TI		
				Yes	5	40 ma, Open Collector/Active Pull-up, Three State	SN55113 SN75113	† TI TI
				No	5	40 ma, 4 Input AND, NAND	DM7830 DM8830 54S140 74S140 HD74S140 DM74S140 DS7830 DS8830 DM7830 DM8830 N74S140 SN54S140 SN55183 SN74S140 SN75183	† AMD AMD † Fairchild Fairchild Hitachi National † National National † Signetics Signetics Signetics † TI † TI TI TI
		Yes	5	40 ma, 4 Input AND, NAND; Three State	DM7831 DM8831 DS7831 DS8831	† AMD AMD † National National		
				DS7831 w/o V _{cc} Clamp	DM7832 DM8832 DS7832 DS8832	† AMD AMD † National National		
			High-Current CMOS	No	3-15	CMOS 50 ma, 4-Input AND, NAND	MM78C30 MM88C30	† National National
			6 ma	Yes	±5	Twisted Pair; Level Shifting	SN55109 SN75109 55109M 75109C ITT55109 ITT75109 MC75109 DS55109 DS75109 RC75109 RM55109 SN55109 SN75109	† AMD AMD † Fairchild Fairchild † ITT ITT Motorola † National National Raytheon † Raytheon † TI TI

INTERFACE

Master Selection Guide

† Military Temperature Range (–55°C to 125°C) * Typical values

INTERFACE—Line Circuits (cont)

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Master Selection Guide

No. Per Device	Output	Party Line	Power Supply	Comments	Device	Source
Line-Drivers—Differential (cont)						
2	12 ma	Yes	±5	Twisted Pair; Level Shifting	SN55110 SN75110 55110M 75110C ITT55110 ITT75110 MC75110 DS55110 DS75110 RM55110 RC75110 SN55110 SN75110	† AMD AMD † Fairchild Fairchild † ITT ITT Motorola † National National † Raytheon Raytheon † TI TI
	24 ma	Yes	±5	Higher current 75110	SN75112	TI
	±20 ma	Yes	-6,5	Push-Pull Output	MC75113	Motorola
3	2 ma	Yes	5	Constant Current	HD245 HD545	† Harris Harris
4	11 ma	Yes	±5	Quad 75110	MC3453	Motorola
	High Current TTL	No	5	50 ohm lines	SN74128	TI
				75 ohm lines	SN54128	TI
		Yes	5	RS-422, Three-State	DS1688 DS3688	† National National
	High Current CMOS	No	3-15	CMOS, 25 ma	MM78C29 MM88C29	† National National
See also Drivers under digital logic families.						
No. Per Device	Receiver Input Threshold	Common Mode Voltage	Supply Voltage	Comments	Device	Source
Line Receivers—Single Ended						
2	Ref ±0.1v		5	Ext. Reference Adjustable from 1.5 to 3.5 v	MC75140 SN75140	Motorola TI
				Ext. Ref. Adj. 1.5 to 3.5v with optional internal 2.5v Reference	SN55142 SN75142	† TI TI
	0.4 to 2.4	±15	5	Differential Input, Single Ended Data	AM2615C AM2615M	AMD † AMD
	±2.0		5	RS232B	DS7822 DS8822	† National National
3	0.7 to 1.7		5	Hysteresis, IBM 360/370	8T24C 75124C MC8T24 DS75124 RC8T24 RM8T24 N8T24 SN75124	Fairchild Fairchild Motorola National Raytheon † Raytheon Signetics TI
	0.75 to 2.25		5	Hysteresis, RS232C, CCITT V.24	9617C 9617C	AMD Fairchild
	0.8 to 2.0 v		5	Hysteresis, High-Speed	8T14C 8T14M 55122M 75122C MC8T14 DS55122 DS75122 RC8T14	Fairchild † Fairchild † Fairchild Fairchild Motorola † National National Raytheon (continued)

† Military Temperature Range (-55°C to 125°C) * Typical values

Bold face indicates additional data is provided on the page noted.

INTERFACE—Line Circuits (cont)

No. Per Device	Receiver Input Threshold	Common Mode Voltage	Supply Voltage	Comments	Device	Source
Line Receivers—Single Ended (cont)						
3	0.8 to 2.0 v		5	Hysteresis, High-Speed (continued)	RM8T14 N8T14 S8T14 SN55122 SN75122	† Raytheon Signetics † Signetics † TI TI
4	±3/0.8 to 3		5 or 12	RS232C, Hysteresis, Fail Safe Option	75154 DS75154 SN75154 RM55154 RC75154	Fairchild National TI † Raytheon Raytheon
	0.75 to 1.5v		5	RS232C, Programmable Threshold, Hysteresis	1489 HD1489 ITT1489 MC1489 DS1489 RC1489 SG1489 SN75189	AMD Harris ITT Motorola National Raytheon Silicon G TI
	0.75 to 2.25		5	RS232C, Programmable Threshold, Hysteresis	1489A XR1489A ITT1489A HD1489A MC1489A DS1489A RC1489A SG1489A SN75189A	AMD Exar ITT Harris Motorola National Raytheon Silicon G TI
	0.97 to 2.65		5	Hysteresis, 120 Ohm System	DS7836	† National
	1.05 to 2.5		5	Hysteresis, 120 Ohm System	DS8836	National
	1.2 to 1.8		5	120 Ohm System, No Hysteresis, NOR Input	DS7640	† National
	1.3 to 1.7		5	120 Ohm System, No Hysteresis, NOR Input	DS8640	National
	1.5 to 2.0		5	Hysteresis, 2-Input	DS8640 N8T380	National Signetics
	5 to 7.5		15	Hysteresis, Interface to CMOS	367A 367M	Teledyne S † Teledyne S
				Hysteresis, Open Collector, Interface to CMOS	368A 368M	Teledyne S † Teledyne S
	5.5 to 8		12	Hysteresis, Interface to CMOS	367B 367C	Teledyne S † Teledyne S
				Hysteresis, Open Collector, Interface to CMOS	368B 368C	† Teledyne S † Teledyne S
6	0.97 to 2.65		5	Hysteresis, 120 Ohm System	DS7837	† National
	1.05 to 2.50		5	Hysteresis, 120 Ohm System	MC3437 DS8837 N8T37	Motorola National Signetics
Line Receivers—Differential						
2	±0.35/0.3 to 3		5	ADJ. RS232B, C, MIL-188	N8T16	Signetics
	±0.2/0.3	±10/15	5	Twisted Pair, ±15v CMV, Response Control	DS78LS20 DS88LS20	† National National
	±0.5/2	±0/15	5,12	±15 v CMV	9620M 9620M	† AMD † Fairchild

† Military Temperature Range (–55°C to 125°C) * Typical values

INTERFACE—Line Circuits (cont)

No. Per Device	Receiver Input Threshold	Common Mode Voltage	Supply Voltage	Comments	Device	Source
Line Receivers—Differential (cont)						
2	$\pm 0.5/2$	$\pm 0/12$	5, 12	± 12 v CMV	9620C 9620C	AMD Fairchild
	$\pm 0.5/1$	$\pm 0/15$	5	± 15 v CMV, Response Control	9615C 9615M 9615C 9615M ITT9615-1 ITT9615-5 SN55115 SN75115	AMD † AMD Fairchild † Fairchild † ITT ITT † TI TI
				Twisted Pair, ± 15 v CMV, Response Control	DM7820 DM8820 DS7820 DS8820 DM7820 DM8820	† AMD AMD † National National † Signetics † Signetics Signetics
		$\pm 5/15$	5	± 15 v CMV	9613C 9613M	Fairchild † Fairchild
		$\pm 3/15$	5	Twisted Pair, $\pm 3/15$ v CMV, Response Control	DM7820A DM8820A DS7820A DS8820A DM7820A DM8820A SN55182 SN75182	† AMD AMD † National National † Signetics Signetics † TI TI
	$\pm 0.5/3$	± 25	± 12	Adjusts RS232C/MIL-188, ± 25 v CMV, Hysteresis	9627C 9627M SN75152	Fairchild † Fairchild TI
	± 2	± 10	-10, 5	130 ohm Termination	9622C 9622M RC9622 RM9622	Fairchild † Fairchild Raytheon † Raytheon
	± 0.010	± 3	± 5	10 mv, MOS Sense Active Pull-up	55207M 75207C ITT75207 DS75207 SN75207	† Fairchild Fairchild ITT National TI
				10 mv, MOS Sense, Three State	DS3604	National
				10 mv, MOS Sense, Open Collector	55208M 75208C ITT75208 DS75208 SN75208	† Fairchild Fairchild ITT National TI
	± 0.025	± 3	± 5	25 mv, Active Pull-up	55107AM 75107AC ITT55107A ITT75107 MC55107 MC75107 DS55107A DS75107A RC75107A RM55107A SN55107A SN75107A	† Fairchild Fairchild † ITT ITT † Motorola Motorola † National National Raytheon † Raytheon † TI TI

† Military Temperature Range (-55°C to 125°C)

* Typical values

Bold face indicates additional data is provided on the page noted.

INTERFACE—Line Circuits (cont)

No. Per Device	Receiver Input Threshold	Common Mode Voltage	Supply Voltage	Comments	Device	Source								
Line Receivers—Differential (cont)														
2	±0.025	±3		25 mv, 3 State 55107	DS1603 DS3603	† National National								
				25 mv, Open Collector	55108AM 75108AC ITT55108A ITT75108A MC55108 MC75108 DS55108A DS75108A RC75108A RM55108A SN55108A SN75108A	Fairchild Fairchild † ITT ITT † Motorola Motorola † National National Raytheon † Raytheon † TI TI								
				55107A w/Diode Protected Input Stage	SN55107B SN75107B 55107BM 75107BC ITT55107B ITT75107B DS55107 DS75107 SN55107B SN75107B	† AMD AMD † Fairchild Fairchild † ITT ITT † National National † TI TI								
				55108A w/Diode Protected Input Stage	SN55108B SN75108B 55108BM 75108BC DS55108 DS75108 SN55108B	† AMD AMD † Fairchild Fairchild † National National † TI								
				3	±0.075		±5	100 ohm Twisted Pair, Shielded	HD248 HD548	† Harris Harris				
								±1.5 ma	±5	100 ohm Twisted Pair, Shielded	HD246 HD249 HD546 HD549	† Harris † Harris Harris Harris		
								4	±0.025	±3	±5	Four 75107, Active Pull-up	MC3450 DS3650	Motorola National
												Four 75108, Open Collector	MC3452 DS3652	Motorola National
								3 State	DS3651	National				
					±0.2	±15	5	50 mv Hysteresis	DS1689 DS3689 DS1690 DS3690 DS3651	† National National † National National National				
				See also Receivers-listed under ECL and HNIL/HTL Miscellaneous sections										

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† Military Temperature Range (–55°C to 125°C) * Typical values

IC UPDATE MASTER

No. Per Device	Receiver Input Threshold	Device Output	Supply Voltage	Comments	Device	Source
2	MOS/TTL	MOS/TTL	5	Transceiver/Port Controller	N8T30	Signetics
4	0.8 to 2.0	TTL	5	General Purpose Interface Bus, Open Collector, 100 ma Output	MC3440 MC3441 MC3443 DS7641 DS8641 DS8642 6605C	Motorola Motorola Motorola † National National National Teledyne S
				General Purpose Bus, Open Collector, 100 ma, for 50 ohm system	DS8642	National
	0.85 to 2.0	TTL	5	Three-State	N8T26	Signetics
	0.97 to 2.65	TTL	5	Open Collector, 1 v Hysteresis	DS7838	† National
	1.05 to 2.50	TTL	5	Open Collector, 1 v Hysteresis	MC3438 DS8838 N8T38	Motorola National Signetics
	1.0 to 2.45 v	TTL	5	Open Collector, Hysteresis	AM26S12AM AM26S12AC	† AMD AMD
	1.2 to 2.2 v	TTL	5	Open Collector, Hysteresis	AM26S12M AM26S12C	† AMD AMD
	1.5 to 3.2 v	TTL	5	Open Collector, 100 ma Output	SN55138	† TI
	1.6 to 2.4v	TTL	5	Open Collector, 100 ma Output	AM26S10M AM26S11M	† AMD † AMD
	1.75 to 2.25v	TTL	5	Open Collector, 100 ma Output	AM26S10C AM26S11C	AMD AMD
	1.8 to 2.9 v	TTL	5	Open Collector, 100 ma Output	SN75138	TI
	1.05 to 2.50	TTL	5	Three-State, T/R Disables, Hysteresis	DS7833 DS8833	† National National
				Inverting 7833/8833	DS7835 DS8835	† National National
				Three-State, NOR Gate Transmit Disable, Hysteresis	DS7839 DS8839	† National National
				Inverting 7839/8839	DS7834 DS8834 N8T34	† National National Signetics

Line Transceivers—Differential

1	$\pm 0.5/\pm 1v$	TTL	5	Independent Three-State 55113 Driver and 55115 receiver	SN55116 SN75116	† TI TI
				Three-State 8 Pin, 40 ma,	SN55117 SN75117	† TI TI
				Same as 55116 with Three-State receiver	SN55118 SN75118	† TI TI
				Same as 55117 with Three-State receiver	SN55119 SN75119	† TI TI

INTERFACE—Memory and Peripheral Drivers

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line	
Memory & Peripheral Drivers				Memory & Peripheral Drivers (cont)				Memory & Peripheral Drivers (cont)				
MOS Dynamic Memory, Address Refresh Logic Circuitry	MC8505	Motorola		Quad MOS Clock Driver, Decodes input address	DS3643 DS3673	National National		Memory Driver Dual, 400ma Sink/Source, Decode (for magnetic memories) (continued)	SN75324	TI		
Clock Generator/Oscillator, to 10 MHz, 8:1 Divider, for Microprocessors	ICM7209	† Intersil		6-Bit MOS Refresh Counter/Driver	DS1676 DS3676	† National National		Memory Driver, Quad, 600ma Sink, Decode	55326M 75326C ITT75326	† Fairchild Fairchild ITT	110	
MOS Clock Driver	MH0007 MH0012 MH0007C MH0012C	† National † National National National		Quad TTL to NMOS Memory Driver (For 7001, etc.)	MC3466	Motorola		Memory Driver, Quad, 600ma Source Decode	55327M 75327C ITT75327	† Fairchild Fairchild ITT	120	
Dual MOS Clock Driver	0026 0026C 0056 0056C SH013C SH013M MC1585 MMH0026 MMH0026C MH0009 MH0009C MH0013 MH0013C DS0025 DS0025C DS0026 DS0026C DS0056 DS0056C SN75369	† AMD AMD † AMD AMD Fairchild † Fairchild Motorola † Motorola Motorola † National National † National National † National National † National National † National National National National † National National TI	10 20	Quad TTL to NMOS Memory Driver (for 2105, 2107, etc.)	3225	Intel		Memory Driver, Dual, 600ma Sink/Source, Decode	55325M 75325C ITT55325 ITT75325	† Fairchild Fairchild ITT ITT	130	
Dual MOS Clock Driver (for PMOS Memories)	IM5013AC IM5013AM	Intersil † Intersil		Dual NAND TTL to MOS Driver (PMOS memory interface)	ITT75361A MC75361 DS75360 DS75361 DS75364 MH8805 SN75361A SN75362	ITT Motorola National National National National TI TI	60	Memory Decoder/Driver 8-Channel, (for core)	SN55329	† TI	140	
Quad MOS Clock Driver (for PMOS Memories)	IM5003AC IM5003AM	Intersil † Intersil	30	Dual AND TTL to MOS Driver (NMOS Memory interface)	SN75322 SN75363	TI TI		Quad Multiplexer/Driver, for MOS systems	DS1648 DS3648 DS1678 DS3678	† National National † National National		
4 Phase MOS Clock Driver	M002	SGS		Dual Channel TTL to MOS Memory Interface (for TMS4062, AMS6002, etc)	ITT75370 SN75370	ITT TI	70	Hex Inverter/MOS Driver, Three-State	DS1649 DS3649 DS1679 DS3679	† National National † National National		
Two Phase Oscillator/Clock Driver (for MOS systems)	DS7803 DS7807 DS8803 DS8807 DS8813 DS8817	† National † National National National National National		Quad NAND TTL to MOS Driver (MOS memory interface-1103 clock driver)	9607 3207A 3207A-1 ITT75365 MC75365 DS75365 3207A 3207A-1 SN75365	Fairchild Intel Intel ITT Motorola National Signetics Signetics TI	80	Hex Inverter/MOS Driver, disable causes logic 1 state	DS16149 DS36149 DS16179 DS36179	† National National † National National	140	
Quad NMOS Memory Driver	MC3459 MC3460 DS3644 DS3674	Motorola Motorola National National	40	Dual Channel ECL to MOS Driver (MOS memory interface; also ECL to TTL driver)	ITT75368 MC75358 MC75368 SN75368	ITT Motorola Motorola TI		Dual AND Driver, HN1L, 250 ma, Open Collector	391	Teledyne S		
Quad MOS Driver (for clock inputs 2416 CCD Memory)	5244	Intel		ECL and NMOS Level Shifters (4) and High Voltage Clock Driver (1) for 2105, 2107, etc.	3211	Intel		Dual Peripheral AND Driver	55450M 55451M 55460M 55461M 55470M 55471M 75450C 75451C 75460C 75461C 75470C 75471C HD2574 HD2575 ITT55450 ITT55460	† Fairchild † Fairchild † Fairchild † Fairchild † Fairchild † Fairchild Fairchild Fairchild Fairchild Fairchild Fairchild Fairchild Hitachi Hitachi † ITT † ITT	150	
Quad Part Driver, for MM5270 RAM	DS1640 DS3640 DS1670 DS3670	† National National † National National		Dual MOS Logic to MOS Memory Driver	SN75364	TI		Memory Driver Dual, 400ma Sink/Source, Decode (for magnetic memories)	DS3629 DS75324 RC75324 RM55324	National National Raytheon † Raytheon		
Dual MOS Clock Driver, bootstrapped for single supply systems	DS1642 DS3642 DS1671 DS3671 DS1672 DS3672	† National National † National National † National National	50	Quad MOS Memory I/O Register	DS1647 DS3647 DS1677 DS3677 DS16147 DS36147 DS16177 DS36177	† National National † National National † National National † National National	90	Quad Predriver, Open Collector, 50 ma Sink (for magnetic memories)	MC4042	Motorola		
				Dual Memory Driver, 400 ma Sink (for magnetic memories)	MC4043	Motorola	100					

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† Military Temperature Range (-55°C to 125°C)

INTERFACE—Memory and Peripheral Drivers (cont)

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line			
Memory & Peripheral Drivers (cont)				Memory & Peripheral Drivers (cont)				Memory & Peripheral Drivers (cont)						
Dual Peripheral AND Driver (continued)	ITT75450	ITT	10	Dual AND-OR Power Driver, Open Collector (to 100v, sinks 250 ma)	UHP-451	Sprague	60	Dual Peripheral NAND Driver (continued)	SN55462	† TI	120			
	ITT75451	ITT				UHP-459		Sprague		SN75462		TI		
	ITT75460	ITT				UHP-551		Sprague		SN55472		† TI		
	MC75450	Motorola				UHP-559		Sprague		SN75472		TI		
	MC75451	Motorola		20	4-Input AND Current Driver (45v, to 1.5A peak)	DH0006	† National	70	Dual 4-Input NAND Driver, HNIL, 250 ma, Open Collector	395	Teledyne S			
	MC75461	Motorola					DH0006C		National					
	DS3611	National				4-Input AND High Voltage— High Current Driver (45v, to 3A peak)	DH0008	† National	70	Dual Peripheral NAND Driver, to 80v, 300 ma	DS1612	† National		
	DS55450	† National					DH0008C	National				DS3612	National	
	DS75450	National			30	Quad 2-Input AND Driver (to 0v, sinks 300 ma)	UDN-5706A	Sprague	80	Dual Peripheral NAND Driver, for CMOS	DS1632	† National		
	DS75460	National										DS3632	National	
	DS75451	National				Quad 2-Input AND Power Driver, Open Collector (to 100v, sinks 250 ma)	UHC/D-400	† Sprague	90	4-Input NAND High Voltage, High Current Drivers (40v, 0.15 to 0.25A)	DH0011	† National		
	DS75461	National					UHC/D-406	† Sprague				DH0011C	National	
	RC75450	Raytheon				Quad 2-Input NAND Driver (to 70v, sinks 300 ma)	UHC/D-500	Sprague			4-Input NAND High Voltage, High Current Driver (50, 70 or 100v, 0.25 to 0.5A)	DH0016C	National	
	RC75451	Raytheon					UHC/D-506	Sprague				DH0017C	National	
	RM55450	† Raytheon		Dual NAND Driver, HNIL, 250 ma, Open Collector		UHP-400	Sprague	130		Quad 2-Input NAND Power Driver, Open Collector (to 100v, sinks 250 ma)	DH0018C	National		
	RM55451	† Raytheon				UHP-406	Sprague					UHC/D-407	† Sprague	
	75450	Signetics				UHP-500	Sprague					UHC/D-507	† Sprague	
	75450A	Signetics				UHP-506	Sprague					UHC/D-508	† Sprague	
	75451	Signetics		4-Input NAND High Voltage, High Current Driver (40 to 50v, sinks 150 to 500 ma)	SH2001C	Fairchild	140				UHP-407	Sprague		
	75451A	Signetics			SH2001M	† Fairchild						UHP-408	Sprague	
	SG55450	† Silicon G			SH2002C	Fairchild					UHP-507	Sprague		
	SG55451	† Silicon G			SH2200C	Fairchild			150	Relay Driver, to 65v, sinks 300 ma, OR Input for 48v telephone relays	DS1686	† National		
	SG55460	† Silicon G			SH2200M	† Fairchild						DS1687	† National	
	SG55461	† Silicon G		Dual Peripheral NAND Driver	55452M	† Fairchild						DS3686	National	
	SG75450	Silicon G			55462M	† Fairchild					DS3687	National		
	SG75451	Silicon G	40		55472M	† Fairchild		90		Dual OR Driver, HNIL, 250 ma, Open Collector	393	Teledyne S		
	SG75452	Silicon G				75452C				Fairchild		Dual Peripheral OR Driver	55453M	† Fairchild
	SG75460	Silicon G				75462C				Fairchild			55463M	† Fairchild
	SG75461	Silicon G				75472	Fairchild					55473M	† Fairchild	
	SG75451	Silicon G				HD2577	Hitachi					75463C	Fairchild	
	SG75452	Silicon G				ITT75452	ITT					75469C	Fairchild	
	SG75453	Silicon G				ITT75462	ITT				55453	† Hitachi		
	SG75454	Silicon G				MC75452	Motorola				55463	Hitachi		
	SG75455	Silicon G				MC75462	Motorola				75453	Hitachi		
	SG75456	Silicon G				DS3612	National				75463	Hitachi		
	SG75457	Silicon G			DS55452	† National			ITT75453	ITT				
	SG75458	Silicon G			DS55462	† National			ITT75463	ITT				
	SG75459	Silicon G			DS75462	National			MC75453	Motorola				
	SG75460	Silicon G			RC75452	Raytheon			MC75463	Motorola				
	SG75461	Silicon G			RM55452	† Raytheon			DS3613	National				
	SG75462	Silicon G			75452	Signetics			DS55453	† National				
	SG75463	Silicon G			SG55452	† Silicon G	100		DS55463	† National				
	SG75464	Silicon G			SG55462	† Silicon G				DS75453	National			
	SG75465	Silicon G			SG75452	Silicon G				DS75463	National			
	SG75466	Silicon G			SG75462	Silicon G				RC75453	Raytheon			
	SG75467	Silicon G			75452	Teledyne S				RM55453	† Raytheon			
	SG75468	Silicon G			75452B	Teledyne S				75453	Signetics			
	SG75469	Silicon G			75462	Teledyne S				75453	Teledyne S			
	SG75470	Silicon G			SN75402	TI				75453B	Teledyne S			
	SG75471	Silicon G			SN75412	TI				75463	Teledyne S			
	SN55450B	† TI			SN75412	TI				SN55453B	† TI			
	SN55451B	† TI			SN55452B	† TI	110		SN55463	† TI				
	SN55460	† TI			SN75452B	TI				SN55473	† TI			
	SN55461	† TI			(continued)					(continued)				
	SN55461	† TI												
	SN55470	† TI												
	SN55471	† TI												
	SN75401	TI												
	SN75411	TI												
	SN75450B	TI												
	SN75451B	TI												
	SN75460	TI												
	SN75461	TI												
	SN75470	TI												
	SN75471	TI												
Dual Peripheral AND Driver, to 80v, 300 ma	DS1611	† National	50	Dual Peripheral AND Driver, to 80v, 300 ma	DS1611	† National	50	Dual Peripheral AND Driver, to 80v, 300 ma	DS1611	† National	50			
	DS3611	National				DS3611		National				DS3611	National	
Dual Peripheral AND Driver, for CMOS	DS1631	† National	100	Dual Peripheral AND Driver, for CMOS	DS1631	† National	100	Dual Peripheral AND Driver, for CMOS	DS1631	† National	100			
	DS3631	National				DS3631		National				DS3631	National	
Dual 4-Input AND Power Driver Open Collector (to 100v, sinks 250 ma)	UHP-420	Sprague	110	Dual 4-Input AND Power Driver Open Collector (to 100v, sinks 250 ma)	UHP-420	Sprague	110	Dual 4-Input AND Power Driver Open Collector (to 100v, sinks 250 ma)	UHP-420	Sprague	110			
	UHP-520	Sprague				UHP-520		Sprague				UHP-520	Sprague	
Dual 4-Input AND Driver, HNIL, 250 ma Open Collector	390	Teledyne S		Dual 4-Input AND Driver, HNIL, 250 ma Open Collector	390	Teledyne S		Dual 4-Input AND Driver, HNIL, 250 ma Open Collector	390	Teledyne S				

† Military Temperature Range (–55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

INTERFACE—Memory and Peripheral Drivers (cont)

Function	Device	Source	Line	Function	Device	Source	Line
Memory & Peripheral Drivers (cont)				Memory & Peripheral Drivers (cont)			
Dual Peripheral OR Driver (continued)	SN75403	TI		Dual Peripheral NOR Driver, for CMOS	DS1634 † National DS3614 National		
	SN75413	TI		Quintuple High Voltage Interface (Outputs can accept high negative voltages in "off" state)	SP1404 Plessey		
	SN75453B	TI		Quad 2-Input NOR Driver (to 70v, sinks 300 ma)	UDN-5733A Sprague		
	SN75463	TI		Quad 2-Input NOR Power Driver, Open Collector (to 100v, sinks 250 ma)	UHC/D-432 † Sprague UHC/D-433 † Sprague UHC/D-532 † Sprague UHC/D-533 † Sprague UHP-432 Sprague UHP-433 Sprague UHP-532 Sprague UHP-533 Sprague	60	
	SN75473	TI		Quintuple Driver (to 5v, 200 ma) Open Collector	SP762B Plessey		
Dual Peripheral OR Driver, to 80v, 300 ma	DS1613 † National DS3613 National			Quintuple Driver (to 12v, 150 ma) Open Collector	SP761B Plessey		
Dual Peripheral OR Driver, for CMOS	DS1633 † National DS3633 National			Quad Darlington Switch (to 50v, 1.5a)	ULN-2064A Sprague ULN-2074A Sprague		70
Quad 2-Input OR Driver (to 70v, sinks 300 ma)	UDN-5703A Sprague		10	Hammer Driver (to 6A- pulsed output)	DH0028C National		
Quad 2-Input OR Power Driver, Open Collector (to 100v, sinks 250 ma)	UHC/D-402 † Sprague UHC/D-403 † Sprague UHC/D-502 † Sprague UHC/D-503 † Sprague UHP-402 Sprague UHP-403 Sprague UHP-502 Sprague UHP-503 Sprague			Hammer Driver, 7 Channel, CMOS, TTL Input	ITT556 ITT		
Dual NOR Driver, HNIL, 250 ma, Open Collector	394 Teledyne S			Hammer Driver, 7 Channel, MOS, TTL Input	ITT552 ITT		
Dual Peripheral NOR Driver	55454M † Fairchild 55464M † Fairchild 55474M † Fairchild 75454C Fairchild 75464C Fairchild 75474C Fairchild HD2579 Hitachi ITT75454 ITT ITT75464 ITT MC75454 Motorola MC75464 Motorola DS3614 National DS55454 † National DS55464 † National DS75454 National DS75464 National RC75454 Raytheon RM55454 † Raytheon 75454 Signetics SG55454 † Silicon G SG55464 † Silicon G SG75454 Silicon G SG75464 Silicon G 75454 Teledyne S 75454B Teledyne S 75464 Teledyne S SN55454B † TI SN55464 † TI SN55474 † TI SN75404 TI SN75414 TI SN75454B TI SN75464 TI SN75474 TI		20	Hammer Driver, 7 Channel, PMOS Input	ITT554 ITT		
				Printer Driver, 7 channel	FD1021 Hitachi		
				Printer Driver, 10 channel	FD1018 Hitachi ULN-2001A Sprague ULN-2002A Sprague ULN-2003A Sprague ULN-2004A Sprague		80
				Printing Calculate Circuits	DS8654 National DS8655 National DS8656 National DS8692 National DS8693 National DS8694 National		
Dual Peripheral NOR Driver, to 80v, 300 ma	DS1614 † National DS3614 National						

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† Military Temperature Range (–55°C to 125°C)

Interface—Sense Amplifiers

Function	Device	Source	Line	Function	Device	Source	Line	Function	Device	Source	Line					
Sense Amplifiers				Sense Amplifiers (cont)				Sense Amplifiers (cont)								
One Channel Sense Amplifier (for core memories)	MC1440 MC1540	Motorola Motorola		Dual Core Memory Sense Amplifier, Single Open Collector Output (continued)				Dual Core Memory Sense Amplifier, Separate Open Collector Outputs	5534M 5535M 55232M 55233M 7534C 7535C 75232C 75233C ITT5534 ITT5535 ITT7534 ITT7535 MC5534 MC5535 MC7534 MC7535 DS5534 DS5535 DS7534 DS7535 SG7534 SG7535 SN55232 SN55233 SN75232	† Fairchild † Fairchild † Fairchild † Fairchild Fairchild Fairchild Fairchild Fairchild † ITT † ITT ITT ITT † Motorola † Motorola Motorola Motorola † National † National National National National † Motorola † Motorola † Motorola † National † National National National † ITT † ITT † TI	120					
Dual Channel Gated Sense Amplifier (for core memories)	MC1441 MC1541 CA1541	Motorola † Motorola † RCA			DS7523 SN7522 SN7523 SG7522 SG7523 SN5522 SN5523 SN7522 SN7523	National Signetics Signetics Silicon G Silicon G † TI † TI TI TI	60		IT7534 IT7535 MC5534 MC5535 MC7534 MC7535 DS5534 DS5535 DS7534 DS7535 SG7534 SG7535 SN55232 SN55233 SN75232	† Motorola † Motorola Motorola Motorola † National † National National National Silicon G Silicon G † TI † TI TI	130					
Dual Core Memory Sense Amplifier, Separate Outputs	5524M 5525M 7524C 7525C ITT5524 ITT5525 ITT7524 ITT7525 MC5524 MC5525 MC7524 MC7525 DS5524 DS5525 DS7524 DS7525 SN7524 SN7525 SG7524 SG7525 SN5524 SN5525 SN7524 SN7525	† Fairchild † Fairchild Fairchild Fairchild † ITT † ITT ITT ITT † Motorola † Motorola Motorola Motorola † National † National National National Signetics Signetics Silicon G Silicon G † TI † TI TI TI	10		Dual Core Memory Sense Amplifier, Output Register	SN7526 SN7527	TI TI			Dual Core Memory Sense Amplifier, Separate Outputs, Test Points	5528M 5529M 7528C 7529C ITT5528 ITT5529 ITT7528 ITT7529 MC5528 MC5529 MC7528 MC7529 DS5528 DS5529 DS7528 DS7529 SG7528 SG7529 SN5528 SN5529 SN7528 SN7529	† Fairchild † Fairchild Fairchild Fairchild † ITT † ITT ITT ITT † Motorola † Motorola Motorola Motorola † National † National National National Silicon G Silicon G † TI † TI TI TI	70	5538M 5539M 7538C 7539C ITT5538 ITT5539 MC5538 MC5539 MC7538 MC7539 DS5538 DS5539 DS7538 DS7539 SG7538 SG7539	† Fairchild † Fairchild Fairchild Fairchild † ITT † ITT † Motorola † Motorola Motorola Motorola † National † National National National Silicon G Silicon G	140
Dual Core Memory Sense Amplifier, Complementary Output, Latch Capability	ITT5520 ITT5521 ITT7520 ITT7521 DS5520 DS5521 DS7520 DS7521 SN7520 SN7521 SG7520 SG7521 SN5520 SN5521 SN7520 SN7521	† ITT † ITT ITT ITT † National † National National National Signetics Signetics Silicon G Silicon G † TI † TI TI TI	30		Dual Core Memory Sense Amplifier, Separate Inverted Outputs	SN75234 SN75235 55234M 55235M 75234C 75235C ITT55234 ITT75234 ITT55235 ITT75235 SN55234 SN55235 SN75234 SN75235	AMD AMD † Fairchild † Fairchild Fairchild Fairchild † ITT ITT † ITT ITT † TI † TI TI TI		90	Dual Sense Amplifier/Data Register (for core memories)	ITT3671-1 ITT3671-5 ITT55236 ITT75236 ITT55237 ITT75237 SN55236 SN55237 SN75236 SN75237	† ITT ITT † ITT ITT † ITT ITT † TI † TI TI TI	160			
Dual Core Memory Sense Amplifier, Single Open Collector Output	ITT5522 ITT5523 ITT7522 ITT7523 MC5522 MC5523 MC7522 MC7523 DS5522 DS5523 DS7522 (continued)	† ITT † ITT ITT ITT † Motorola † Motorola Motorola Motorola † National † National National	50		Dual Core Memory Sense Amplifier, Separate Inverted Outputs, Test Points	55238M 55239M 75238C 75239C SN55238 SN55239 SN75238 SN75239	† Fairchild † Fairchild Fairchild Fairchild † TI † TI TI TI		110	MOS to TTL Level Converter, High Speed, Three-State	MC4000 MC4300	Motorola † Motorola				
										Dual Sense Amplifier (for MOS memory or line receiver)	LM163 LM363 LM363A (continued)	† AMD AMD AMD				

† Military Temperature Range (-55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

Interface—Sense Amplifiers (cont)

Function	Device	Source	Line
Sense Amplifiers (cont)			
Dual Sense Amplifier (for MOS memory or line receiver) (continued)	75207 75208 DS1604 DS3604 DS1603 DS3603 DS75207 DS75208 75S207 75S208 SN75207 SN75208	Fairchild Fairchild † National National † National National National National Signetics Signetics TI TI	10
Dual Sense Amplifier (NMOS memories to ECL 10K)	MC3461 SN75261	Motorola TI	
Dual MOS to TTL Level Converter, Latch, Three-State (Sense Amp)	MC54468 MC74468 DS3625 DS7802 DS7806 DS8802 DS8806 N8T25	† Motorola Motorola National † National † National National National National Signetics	20
See also Digital—TTL (Translators)			
Quad Sense Amplifier, Three-State	MC3430 MC3431 MC3432 MC3433 DS3651 DS3653	Motorola Motorola Motorola Motorola National National	
Hex MOS Sense Amplifier (MOS to TTL Converter) Three-State	DS1605 DS1606 DS1607 DS1608 DS3605 DS3606 DS3607 DS3608	† National † National † National † National National National National National	30
Hex MOS Sense Amplifier, Open Collector (for 1103)	3208A	Intel	
Hex MOS Sense Amplifiers with Latches, Three-State	3408A	Intel	
4-Channel AC Coupled Sense Amplifier (decoded input channel selection)	SN55244 SN75244	† TI TI	40
4-Input Sense Amplifier (for plated wire or thick thin film memories)	MC1444 MC1544	Motorola † Motorola	

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† Military Temperature Range (–55°C to 125°C)

INTERFACE—Serial Transmitters - Receivers

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Function	Max. Serial Data Rate KHz	Supply Volts	Device	Source
Serial Transmitters-Receivers				
(ACIA) Asynchronous Communications Interface Adapter (Links 8-bit bidirectional data bus to serial asynchronous data communications, including to 6860)	50	5	S6850 MC6850	AMI Motorola
Digital Modem (Modulation, demodulation and supervisory control, up to 600bps.)			S6860 MC6860	AMI Motorola
PSAR (Programmable Synchronous-Asynchronous Receiver) Synchronous/Asynchronous serial to parallel converter with programmable character length and programmable serial data rate.	640	-12,±5	MC2259 NC2259 PT1472B PT1472B-01	Motorola Nitron Western Western
PSAT (Programmable Synchronous-Asynchronous Transmitter) Synchronous/Asynchronous parallel to serial converter that has programmable character length and programmable serial data rate.			MC2257 MC2260 NC2257 NC2260 PT1482B PT1482B-01	Motorola Motorola Nitron Nitron Western Western
PSART (Programmable Synchronous-Asynchronous Receiver-Transmitter) Serial to parallel and parallel to serial converter that can operate in Full Duplex Mode.	50	5	8251	Intersil
	—	—	3843	Fairchild
UART (Universal Asynchronous Receiver-Transmitter) complete serial to parallel and parallel to serial interface.	1.2	-12,5	10371	Rockwell
	10	5 -12,±5	AY3-1014 S1757	GI AMI
	12.5	-12,5	S1883	AMI
	20	-12,5	AY6-1013 TR1602	† GI Western
	30	-12,5	AY5-1013 TR1602-03	GI Western
	40	-12,5	AY5-1013A MP1013A TR1602-09	GI Plessey Western
	50	5	AY5-1014A	GI
		-12,5	TR1602-05	Western
	200	5	HM6402-2 HM6402-9 HM6403-2 HM6403-9 IM6402 IM6402M IM6403 IM6403M	† Harris Harris † Harris Harris Intersil † Intersil Intersil † Intersil
		-12,5	TMS6011	TI
400	5	HM6402A-2 HM6402A-9 HM6403A-2	† Harris Harris † Harris	
		(continued)		

† Military Temperature Range (-55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

INTERFACE—Serial Transmitters - Receivers (cont)

Function	Max. Serial Data Rate KHz	Supply Volts	Device	Source
Serial Transmitters-Receivers (cont)				
(continued)			HM6403A-9	Harris
		-12,5	COM2502 COM2017	SMC SMC
	600	-12,5	COM2502H COM2017H	SMC SMC
USRT (Universal Synchronous Receiver-Transmitter) Complete serial to parallel and parallel to serial interface.	250	-12,5	COM2601	SMC
	500	5	S2350 see page 905	AMI
Asynchronous/synchronous receiver/transmitter to interface serial communications channel with a parallel digital system (i.e. microprocessors)		±12,±5	UR1671	Western

INTERFACE

Master Selection Guide

† Military Temperature Range (-55°C to 125°C)

Communications Circuits

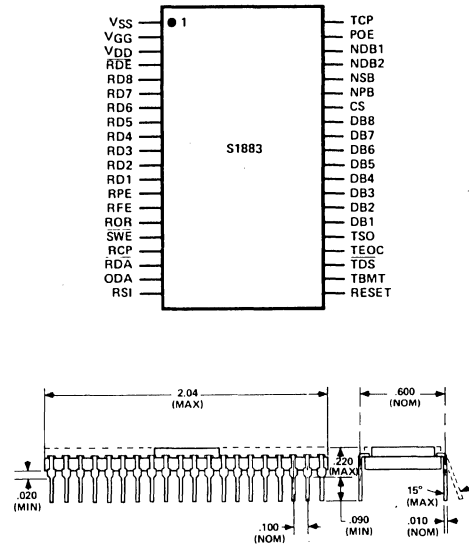
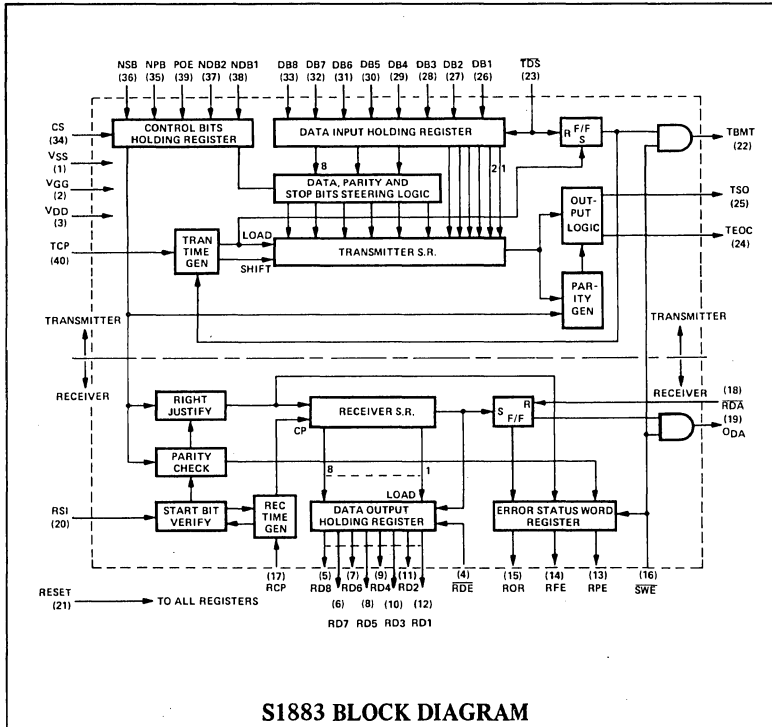
Part No.	Description	Word Length (Bits)	Max. Clock Freq. (kHz)	Input/Output	Power Supply (V)	Process	Page
S1757	Asynchronous Receiver/Transmitter	5, 6, 7, 8	160	MOS	-12, \pm 5	P-1 ²	532
S1883	Asynchronous Receiver/Transmitter	5, 6, 7, 8	200	TTL	-12, \pm 5	P-1 ²	533
S2350	Synchronous Receiver/Transmitter	5, 6, 7, 8	500	TTL	+5	N-SiGate	906
S6850	Asynchronous Receiver/Transmitter	7, 8	800	TTL	+5	N-SiGate	895

INTERFACE

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INTERFACE

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FEATURES

- 12.5 K Baud Data Rates
- 5-8 Bit Word Length
- Parity Generation/Checking Odd, Even, None
- Framing and Overflow Error Detection
- 1, 1.5, or 2 Stop Bits
- Double Buffered Input/Output
- Independent Transmit/Receive Rates
- Start and Stop Bits Generated and Detected
- Interchangeable with TMS6011, COM2017, TR1602, AY-5-1013
- Tri-State Outputs

FUNCTIONAL DESCRIPTION

The S1883 Universal Asynchronous Receiver Transmitter (UART) is a single chip MOS/LSI device that totally replaces the asynchronous parallel to serial and serial to parallel conversion logic required to interface a word parallel controller or data terminal to a bit serial communication network. For asynchronous data transmission with a non-contiguous data bit stream, the UART automatically inserts a START bit preceding each character and under program control 1, 1.5, or 2 stop bits at the end of each character. To detect incoming characters in a noisy environment the UART employs a START bit detection network and allows errorless recovery of data with up to 42% distortion.

The UART will transmit or receive data characters of 5, 6, 7, or 8 bit length. Options allow the generation and checking of

odd, even parity or no parity. The odd or even parity bit is automatically added to the character length for transmission. The parity bit is removed, checked and an error flag set if incorrectly received.

The data or baud rate at the receiver input and transmitter output are determined independently by external clock inputs. The clock inputs must be 16 times the data rate required at the serial input and output. The independent clocks allow for either half or full duplex operation.

The UART provides a buffer register in both the transmitter and receiver to allow a full character time for responding to a received data ready or transmit data request signal. The UART generates a MARK signal if the transmit register is not loaded with a data character and also indicates an overflow error if two characters are received without a RDA input.

TYPICAL APPLICATIONS

- Computer Peripherals
- Communication Concentrators
- Integrated Modems
- Industrial Data Transmission
- TTY Terminals
- Time Division Multiplexing

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +150°C
Positive Voltage on Any Pin with Respect to VSS	+3 Volt
Negative Voltage on Any Pin with Respect to VSS	-20.0 Volt

NOTE: Stresses greater than those listed as Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operation section of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC (STATIC) CHARACTERISTICS $T_A = 0^\circ - +70^\circ\text{C}$, $V_{SS} = +5 \text{ Volt} \pm 5\%$, $V_{GG} = -12 \text{ Volt} \pm 5\%$

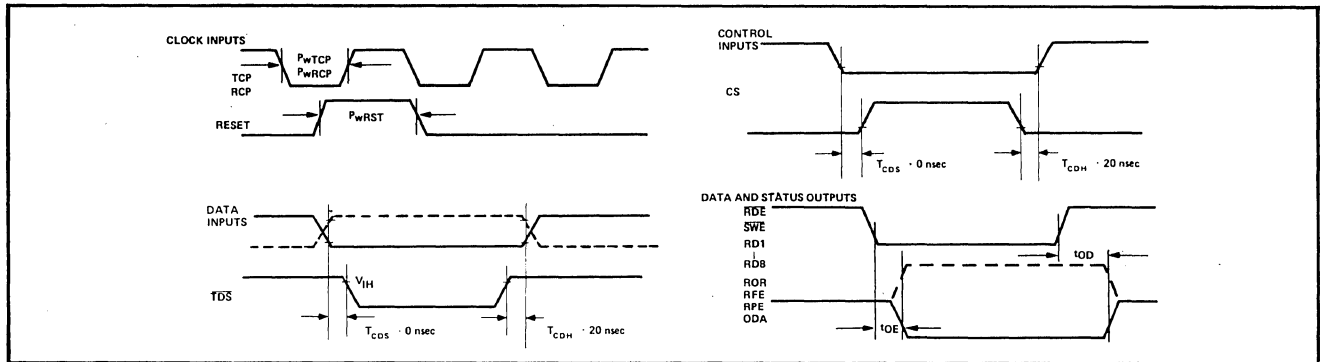
Symbol	Parameter	Min	Max	Unit	Condition
V _{IH}	Input High Voltage	V _{SS} - 1.0	V _{SS} + 0.3	Volt	Internal Pull-up Resistor Provided
V _{IL}	Input Low Voltage	V _{GG}	0.8	Volt	
I _{LI}	Input Load Current		-1.2	mamp	V _{IN} = 0 Volt
V _{OH}	Output High Voltage	2.4		Volt	I _{OH} = - 100 uamp
V _{OL}	Output Low Voltage		.4	Volt	I _{OL} = 1.6 mamp
C _{IN}	Input Capacitance		20	pf	V _{IN} = V _{SS}
C _{OUT}	Output Capacitance		10	pf	V _{OUT} = V _{SS}
I _{SS}	V _{SS} Supply Current		30	mamp	$\overline{SWE} = \overline{RDE} = V_{IL}$
I _{GG}	V _{GG} Supply Current		40	mamp	ITTL Load

AC (DYNAMIC) CHARACTERISTICS $T_A = 0^\circ\text{C} - +70^\circ\text{C}$; $V_{SS} = +5 \text{ Volt} \pm 5\%$; $V_{GG} = -12 \text{ Volt} \pm 5\%$

Symbol	Parameter	Min	Max	Unit	Condition
TCP, RCP	Clock Frequency	DC	200	KHz	
Input Pulse Widths					
PWTCP	Transmit Clock	2.5		usec	C _L = 20pf 1 TTL Load
PWRCP	Receive Clock	2.5		usec	
PWCS	Control Strobe	250		nsec	
PWTDS	Transmit Data Strobe	250		nsec	
PWRST	RESET	1.0		μsec	
PWSWE	Status Word Enable	500		nsec	
PWRDA	Reset Data Available	500		nsec	
PWRDE	Receive Data Enable	250		nsec	
Switching Characteristics					
t _{CDS}	Control Set Up Time	0		nsec	Figure 1
t _{CDH}	Control Hold Time	20		nsec	Figure 1
t _{OE}	Output Enable Time		500	nsec	
t _{OD}	Output Disable Time		500	nsec	

INTERFACE
AMI

TIMING WAVEFORMS (Figure 1)



PIN DEFINITIONS

Pin	Label	Function																																													
(1)	VSS	+5 Volt ± 5%																																													
(2)	VGG	-12 Volt ± 5%																																													
(3)	VDD	Ground																																													
(21)	RESET	The transmitter status outputs TBMT and TEOC are set to VOH indicating the input transmitter buffer register is empty. The TSO output generates VOH or MARK until a valid data character has been loaded into the transmitter and valid data transmission begins. The receiver status output ODA, is reset to the VOL state.																																													
(38)	NDB1	Number Data Bits/Character																																													
(37)	NDB2	Number Data Bits/Character																																													
(36)	NSB	Number Stop Bits The bit length of each data character and the number of stop bits added to each transmitted character are defined by these three inputs. The character word length does not include the parity bit and is common to both the transmitter and receiver if operating in the full duplex mode.																																													
		<table border="1"> <thead> <tr> <th>NSB</th> <th>NDB2</th> <th>NDB1</th> <th>BITS/CHARACTER</th> <th>STOP BITS</th> </tr> </thead> <tbody> <tr> <td>VIL</td> <td>VIL</td> <td>VIL</td> <td>5</td> <td>1</td> </tr> <tr> <td>VIL</td> <td>VIL</td> <td>VIH</td> <td>6</td> <td>1</td> </tr> <tr> <td>VIL</td> <td>VIH</td> <td>VIL</td> <td>7</td> <td>1</td> </tr> <tr> <td>VIL</td> <td>VIH</td> <td>VIH</td> <td>8</td> <td>1</td> </tr> <tr> <td>VIH</td> <td>VIL</td> <td>VIL</td> <td>5</td> <td>1.5</td> </tr> <tr> <td>VIH</td> <td>VIL</td> <td>VIH</td> <td>6</td> <td>2</td> </tr> <tr> <td>VIH</td> <td>VIH</td> <td>VIL</td> <td>7</td> <td>2</td> </tr> <tr> <td>VIH</td> <td>VIH</td> <td>VIH</td> <td>8</td> <td>2</td> </tr> </tbody> </table>	NSB	NDB2	NDB1	BITS/CHARACTER	STOP BITS	VIL	VIL	VIL	5	1	VIL	VIL	VIH	6	1	VIL	VIH	VIL	7	1	VIL	VIH	VIH	8	1	VIH	VIL	VIL	5	1.5	VIH	VIL	VIH	6	2	VIH	VIH	VIL	7	2	VIH	VIH	VIH	8	2
NSB	NDB2	NDB1	BITS/CHARACTER	STOP BITS																																											
VIL	VIL	VIL	5	1																																											
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VIH	VIH	VIL	7	2																																											
VIH	VIH	VIH	8	2																																											
(35)	NPB	NO PARITY BIT. A VIH eliminates the PARITY bit from being transmitted causing the STOP bit(s) to immediately follow the last data bit. The receiver assumes the bit(s) following the last data bit to be STOP bits. The RPE output is also forced to a VOL condition.																																													
(39)	POE	PARITY ODD/EVEN. If the NPB input is VIL, the parity mode is ODD if POE is VIL and EVEN if POE is VIH. The parity mode is the same for both the transmitter and receiver.																																													
(34)	CS	CONTROL STROBE. A VIH loads POE, NDB1, NDB2, NPB, NSB into the CONTROL HOLDING REGISTER. To load the control inputs for static operation CS can be hard-wired to VIH.																																													
(26)	DB1	TRANSMITTER DATA BITS. Input data on DB1-DB8 are strobed into the DATA INPUT HOLDING REGISTER by TDS. Input data is assumed right justified so DB1 is always the least significant bit and is the bit																																													
(27)	DB2																																														
(28)	DB3																																														
(29)	DB4																																														
(30)	DB5																																														

INTERFACE

AMI

Pin	Label	Function
(31)	DB6	transmitted following the START bit. For data words less than eight bits, the unused bits are don't care inputs.
(32)	DB7	
(33)	DB8	
(23)	\overline{TDS}	TRANSMITTER DATA STROBE. A V_{IL} enters data on the DB1-DB8 inputs into the INPUT HOLDING REGISTER. If the transmitter is in the idle state with both TBMT and TEOC at V_{OH} , the START bit will be generated on the first negative transition of the input clock TCP following the return of \overline{TDS} to a V_{IH} state.
(25)	TSO	TRANSMITTER SERIAL OUTPUT. Data entered on DB1-DB8 are serially transmitted on TSO. A START (SPACE) bit precedes each character. A PARITY bit, if selected, and the correct number of STOP bits follow the last valid data bit. The TSO output is V_{OH} (MARK) when a valid character is not being transmitted.
(22)	TBMT	TRANSMITTER BUFFER EMPTY. A V_{OH} indicates the character in the INPUT HOLDING REGISTER has been transferred into the transmitter and a new character may be loaded into the INPUT HOLDING REGISTER. One complete character time (START BIT, DATA BITS, PARITY BIT, AND STOP BIT(S)) is available to load the next character. If a \overline{TDS} is not generated within the time allotted, the TSO output will go into an idle state of V_{OH} or a MARK condition. TBMT will remain in the tri state mode unless \overline{SWE} is a U_{ZL} .
(24)	TEOC	TRANSMITTER END OF CHARACTER. A V_{OL} to V_{OH} transition indicates the transmission of the character and stop bits have been completed. The V_{OH} is maintained until the leading edge of the next START bit (MARK to SPACE transition) is generated.
(40)	TCP	TRANSMITTER CLOCK PULSE. The transmitter input clock must be 16 times faster than the desired baud rate at TSO.
(17)	RCP	RECEIVER CLOCK PULSE. The receiver input clock must be 16 times the baud rate of data received on RSI.
(20)	RSI	RECEIVER SERIAL INPUT. Serial input data is received on RSI at a baud rate 1/16th the rate of RCP. The V_{IH} to V_{IL} (MARK to SPACE) transition beginning each START bit synchronizes the receiver to the incoming data. Data is assumed to be received least significant bit first.
(12)	RD1	RECEIVER DATA. Data outputs from the DATA OUTPUT HOLDING REGISTER are active only when RDE is a V_{IL} . The eight data outputs are in a tri-state mode if RDE is a V_{IH} . Data is presented at the outputs right justified with RDI the least significant bit. For data word lengths less than 8 bits the unused bits will appear as V_{OL} .
(11)	RD2	
(10)	RD3	
(9)	RD4	
(8)	RD5	
(7)	RD6	
(6)	RD7	
(5)	RD8	
(4)	\overline{RDE}	RECEIVER DATA ENABLE. A V_{IL} enables data in the DATA OUTPUT HOLDING REGISTER to the RECEIVER DATA output pins. For an output configuration not requiring a tri-state condition for RD1-RD8 the RDE input can be tied directly to ground enabling the data outputs at all times.
(19)	ODA	OUTPUT DATA AVAILABLE. A V_{OH} indicates a complete character has been received and transferred to the DATA OUTPUT HOLDING REGISTER. The ODA output will be in the tri-state mode unless \overline{SWE} is a V_{IL} . For contiguous data inputs on RSI data will remain in the holding register one character time before being lost.
(18)	\overline{RDA}	RESET DATA AVAILABLE. A V_{IL} resets the ODA to a V_{OL} . If ODA is not reset by \overline{RDA} the ROR will be set when the next complete character is received and transferred to the DATA OUTPUT HOLDING REGISTER.
(15)	ROR	RECEIVER OVERRUN. A V_{OH} indicates a second character has been received and transferred to the DATA OUTPUT HOLDING REGISTER without an intervening \overline{RDA} . If the previously received character has not been unloaded from the register the next character will be loaded and the first character lost. ROR will remain in the tri-state mode unless \overline{SWE} is a V_{IL} .
(14)	RFE	RECEIVER FRAMING ERROR. A V_{OH} indicates a correct STOP bit was not received following the START bit and correct number of data bits. RFE will remain in the tri-state mode unless \overline{SWE} is a V_{IL} .

Pin	Label	Function
(13)	RPE	RECEIVER PARITY ERROR. A V_{OH} indicates the accumulated parity on the received character does not compare with the parity mode set by POE. RPE will remain in the tri-state mode unless \overline{SWE} is a V_{IL} .
(16)	\overline{SWE}	STATUS WORD ENABLE. A V_{IL} enables the status outputs ODA, ROR, RFE, RPE and TBMT on the respective output lines. When \overline{SWE} is V_{IH} all status outputs are in the tri-state mode. For output configurations not requiring a tri-state condition for the status outputs, \overline{SWE} may be tied directly to ground.

APPLICATION DATA

Asynchronous data communications is typified by low data rates, non-contiguous data messages, and a MARK condition on the line between characters. As a result, each data character must be framed for recognition by START and STOP bits. The S1883 UART provides all the logic required to provide a complete full-duplex (transmit and receive simultaneously) asynchronous communication channel for baud rates up to 9600 bps. Included in the S1883 capabilities are; automatic START and STOP bit generation and detection; PARITY generation and detection on variable length characters; tri-state outputs for data and status for data bus configurations, double buffering for less critical timing, and a receiver allowing acceptance of data with up to 42% distortion.

RECEIVER OPERATION

Asynchronous communication line discipline dictates that each character, regardless of width, must be preceded by a START bit. The receiver input logic detects the V_{IH} to V_{IL} (MARK to SPACE) transition on the RSI line that is the leading edge of the START bit. For one half bit time after the leading edge, RSI is sampled for a V_{IL} to insure a proper START bit was present. The following data bits are then clocked into the receiver in the center of each bit period. If RSI returns to the V_{IH} condition before the mid-point of the START bit, the receiver returns to a search for a MARK to SPACE transition.

If at the time of transfer ODA has not been reset by a \overline{RDA} , indicating the previous character has not been read, the ROR error flag is set to V_{OH} . The previous data character and status will be lost as the new character is loaded. One full character time is available, assuming contiguous data input at RSI, after ODA is set to read the output character. The data is available at the outputs RD1-RD8 right justified with RD1 the least

significant bit. For character widths less than 8 bits the unused outputs are forced to V_{OL} .

For data bus configurations the output data and status are tri-state lines enabled by \overline{RDE} and \overline{SWE} respectively. For polled systems \overline{SWE} can be strobed for detection of ODA and error conditions prior to reading data. For interrupt driven systems \overline{SWE} can be tied directly to ground and ODA used as a data ready interrupt input. A minimum of one character time is available to test the remaining error status bits and input the data character. Typically the same signal can be used for \overline{RDE} and \overline{RDA} .

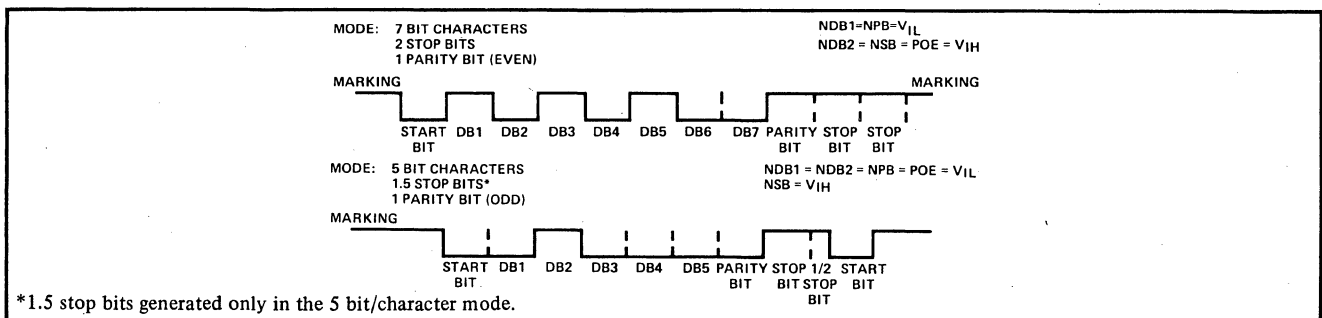
TRANSMITTER OPERATION

The transmit section of the S1883 is reset to a MARK condition with V_{OH} on TSO after receiving a pulse on RESET. Additionally, the transmitter is reset to a character request mode with TBMT and TEOC both at V_{OH} . If the character format is not static, the word length NDB1 and NDB2, parity mode NPB and POE, and number of stop bits NSB should be strobed into the UART with CS.

If both the DATA INPUT HOLDING REGISTER and the TRANSMITTER SHIFT REGISTER are empty the transmitter is in the idle state with TSO, TBMT and TEOC all at V_{OH} . The START bit for a data character loaded with a \overline{TDS} pulse during the idle state is generated at the first negative transition of the TCP following the trailing edge of \overline{TDS} . TBMT goes to V_{OL} with the first \overline{TDS} . As soon as the character is transferred from the INPUT HOLDING REGISTER to the SHIFT REGISTER, TBMT returns to a V_{OH} and a second character can be loaded. Each character is transmitted with a START bit and 1, 1.5 or 2 stop bits controlled by the respective inputs.

The TEOC is set to V_{OH} after the generation of the last STOP bit indicating the complete character has been transmitted.

TYPICAL DATA FORMAT



PRELIMINARY TECHNICAL DATA

FEATURES

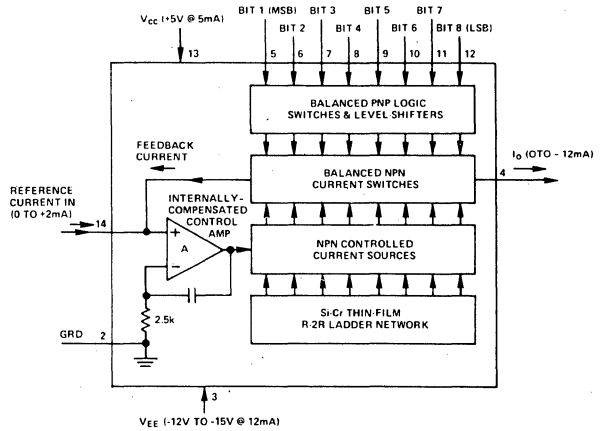
- Replaces the Motorola 1408/1508 8-Bit DAC
- Guaranteed Monotonicity Over Full Temperature Range
- Single Chip Monolithic Construction
- Hermetic 16 Pin Ceramic DIP
- TTL/DTL and CMOS Compatibility
- High Stability SiCr Thin Film Resistors
- Low Cost

PRODUCT DESCRIPTION

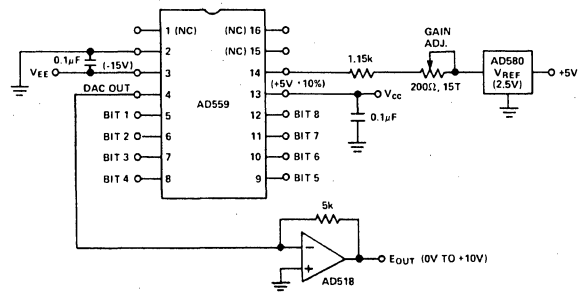
The AD559 is a low cost integrated circuit 8-bit digital-to-analog converter consisting of specially designed, precision bipolar switches, a control amplifier, and high stability silicon chromium thin-film resistors, all on a single monolithic chip. The single chip is mounted in a hermetically-sealed ceramic 16 lead dual in-line package.

A unique combination of advanced circuit design, and high stability SiCr thin film resistor processing provides the AD559 with true 8-bit accuracy at low I.C. costs. The maximum error at +25°C is limited to 1/2LSB (K version) and the gain temperature coefficient is limited to 20ppm/°C max. Monotonicity is guaranteed over the full operating temperature range of the devices.

The AD559 is recommended for all low cost, 8-bit DAC requirements and as a replacement for the Motorola 1408/1508 8-bit DAC, in most applications. The AD559K is specified for operation over the 0 to +70°C temperature range and the AD559S for operation over the full extended temperature range, -55 to +125°C.



AD559 Block Diagram



Unipolar Output

ORDERING INFORMATION

MODEL	TEMP. RANGE (°C)	ACCURACY (LSB MAX)
AD559K/BIN	0 to +70	±1/2
AD559S/BIN	-55 to +125	±1/2

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 West Coast Mid-West Texas
 213/595-1783 312/894-3300 214/231-5094

INTERFACE

Analog Devices

PRELIMINARY TECHNICAL DATA

FEATURES

- Low Cost: \$39 (100's, AD562K)
- True 12-Bit Accuracy ($\pm 1/4$ LSB)
- All Active Elements On Single LSI Linear Chip
- Guaranteed Monotonicity Over Full Temperature Range
- Hermetic 24-Pin DIP
- TTL/DTL and CMOS Compatibility

PRODUCT DESCRIPTION

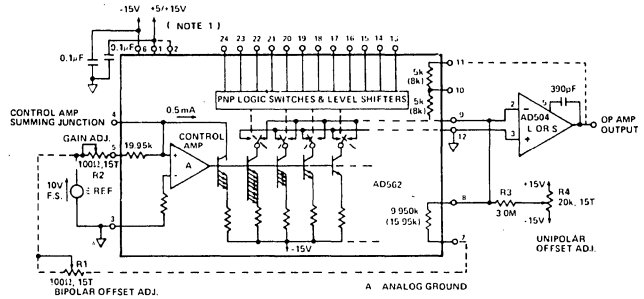
The AD562 is an integrated circuit 12-bit digital-to-analog converter consisting of a specially designed precision bipolar switch and control amplifier chip and a compatible high stability silicon chromium thin film resistor chip. The two IC chips are internally connected and mounted in a hermetically-sealed ceramic 24-lead dual-in-line package.

A unique combination of advanced circuit design, high stability SiCr thin film resistor processing, and laser trimming technology provides the AD562 with true 12-bit accuracy. The maximum error at +25°C is limited to 1/4 LSB (K, A, and S versions) and the gain temperature coefficient is limited to 3ppm/°C max. Monotonicity is guaranteed over the full operating temperature range of the devices.

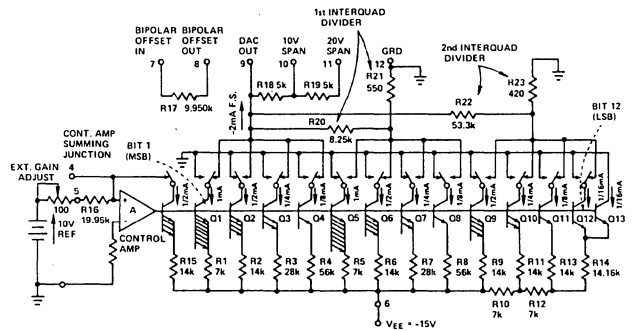
The AD562 is recommended for all high accuracy 12-bit D/A converter applications where true 12-bit performance is required and small size and low cost are primary considerations. The AD562 is also ideal for use in constructing A/D conversion systems and as a building block for higher resolution D/A systems. The AD562K is specified for operation over the 0 to +70°C temperature range, the AD562A for operation over the -25 to +85°C temperature range, and the AD562S for operation over the full extended temperature range of -55 to +125°C.

ORDERING INFORMATION

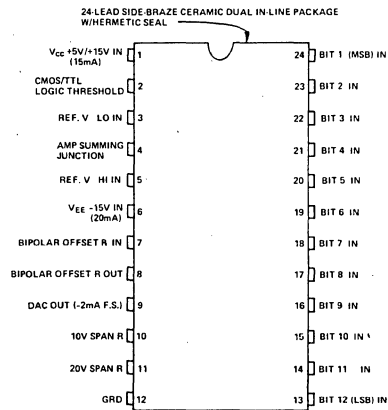
MODEL	TEMP. RANGE (°C)	ACCURACY (LSB MAX)	PRICE (100's) (\$)
AD562K/BIN	0 to +70	$\pm 1/4$	\$ 39.00
AD562K/BCD	0 to +70	$\pm 1/4$	\$ 39.00
AD562A/BIN	-25 to +85	$\pm 1/4$	\$ 49.00
AD562A/BCD	-25 to +85	$\pm 1/4$	\$ 49.00
AD562S/BIN	-55 to +125	$\pm 1/4$	\$100.00
AD562S/BCD	-55 to +125	$\pm 1/4$	\$100.00



AD562 Functional Schematic



Ladder Network and Inter-Quad Divider Current Scaling



**PIN CONFIGURATION
TOP VIEW**

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West Coast Mid-West Texas
213/595-1783 312/894-3300 214/231-5094

INTERFACE
Analog Devices

PRELIMINARY TECHNICAL DATA

FEATURES

- Extremely Low Cost: \$27 (100's, AD563J)
- True 12-Bit Accuracy: $\pm 1/2$ LSB max (AD563K, S, T)
- Guaranteed Differential Nonlinearity: $\pm 1/2$ LSB max
- Positive True Logic
- Includes Internal Reference
- Guaranteed Monotonicity Over Full Temperature Range
- Low Overall Gain T.C.: 10ppm/ $^{\circ}$ C max (AD563T)
- 30ppm/ $^{\circ}$ C max (AD563J)

Hermetic 24 pin DIP
TTL/DTL and CMOS Compatibility

PRODUCT DESCRIPTION

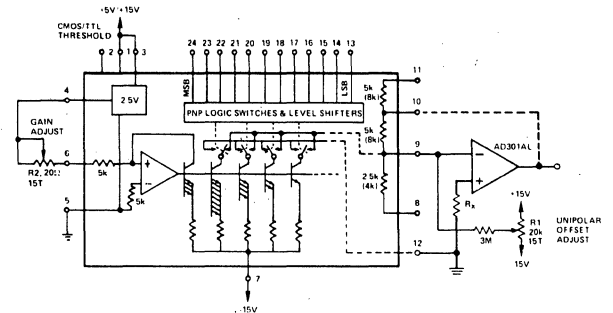
The AD563 is an integrated circuit 12-bit digital-to-analog converter consisting of a specially designed precision bipolar switch and control amplifier chip, a compatible high stability silicon chromium thin film resistor chip, and a low drift, voltage reference chip. The three I.C. chips are internally connected and mounted in a hermetically-sealed, ceramic 24 lead dual-in-line package to produce a self contained current output DAC.

A unique combination of advanced circuit design, high stability SiCr thin film resistor processing and laser trimming technology, provides the AD563 with true 12-bit accuracy. The maximum error at +25 $^{\circ}$ C is limited to $1/4$ LSB (K, S and T versions) with the gain temperature coefficient limited to 10ppm/ $^{\circ}$ C max, including the effects of the internal reference. Monotonicity on all versions is guaranteed over the full operating temperature range.

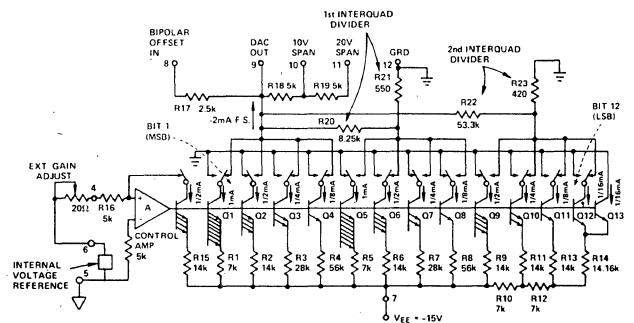
The AD563 is recommended for all high accuracy 12-bit D/A converter applications where true 12-bit performance is required, but low cost and small size are considerations. The AD563 is also ideal for use in constructing A/D conversion systems and as a building block for higher resolution D/A systems. The AD563J and K are specified for operation over the 0 to +70 $^{\circ}$ C temperature range, the AD563S and T for operation over the military temperature range, -55 $^{\circ}$ C to +125 $^{\circ}$ C.

ORDERING INFORMATION

MODEL	TEMP. RANGE ($^{\circ}$ C)	ACCURACY (LSB MAX)	PRICE (100's) (\$)
AD563J/BIN	0 to +70	$\pm 1/2$	\$ 27.00
AD563J/BCD	0 to +70	$\pm 1/2$	\$ 27.00
AD563K/BIN	0 to +70	$\pm 1/4$	\$ 42.00
AD563K/BCD	0 to +70	$\pm 1/4$	\$ 42.00
AD563S/BIN	-55 to +125	$\pm 1/4$	\$110.00
AD563S/BCD	-55 to +125	$\pm 1/4$	\$110.00
AD563T/BIN	-55 to +125	$\pm 1/4$	\$140.00
AD563T/BCD	-55 to +125	$\pm 1/4$	\$140.00

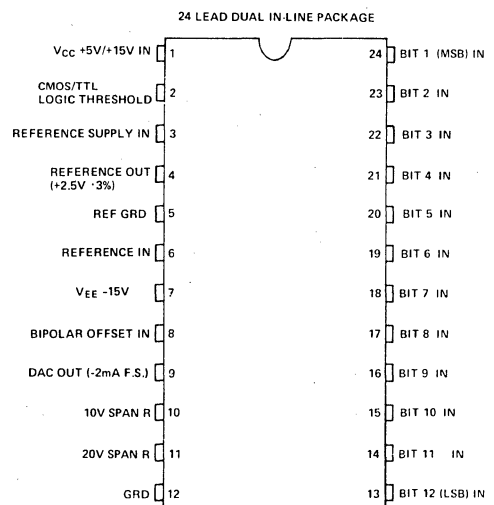


AD563 in Typical Unipolar Connection Scheme



Ladder Network and Inter-Quad Divider Current Scaling

PIN CONFIGURATION



TOP VIEW

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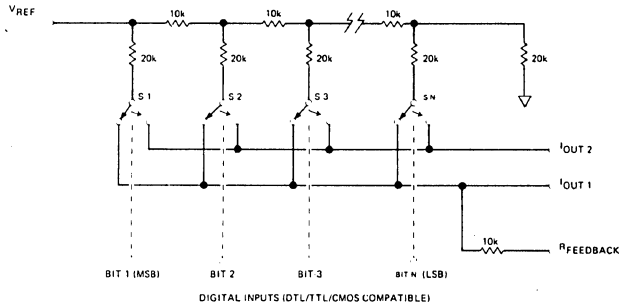
Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
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AD7520, AD7521

FEATURES

AD7520:	10 Bit Resolution
AD7521:	12 Bit Resolution
Linearity:	8, 9 and 10 Bit
Nonlinearity Tempco:	2 ppm of FSR/°C
Low Power Dissipation:	20 mW
Current Settling Time:	500 ns
Feedthrough Error:	1/2 LSB @ 100 kHz
TTL/DTL/CMOS Compatible	

FUNCTIONAL DIAGRAM



AD7520: N=10
AD7521: N=12
Logic: A switch is closed to IOUT 1 for its digital input in a "HIGH" state.

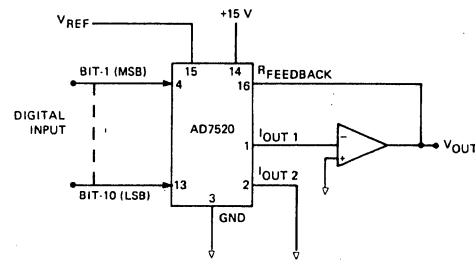
GENERAL DESCRIPTION

The AD7520 (AD7521) is a low cost, monolithic 10-bit (12-bit) multiplying digital-to-analog converter packaged in a 16-pin (18-pin) DIP. The devices use advanced CMOS and thin film technologies providing up to 10-bit accuracy with TTL/DTL/CMOS compatibility.

The AD7520 (AD7521) operates from +5V to +15V supply and dissipates only 20 mW, including the ladder network.

Typical AD7520 (AD7521) applications include: digital/analog multiplication, CRT character generation, programmable power supplies, digitally controlled gain circuits, etc.

TYPICAL APPLICATION



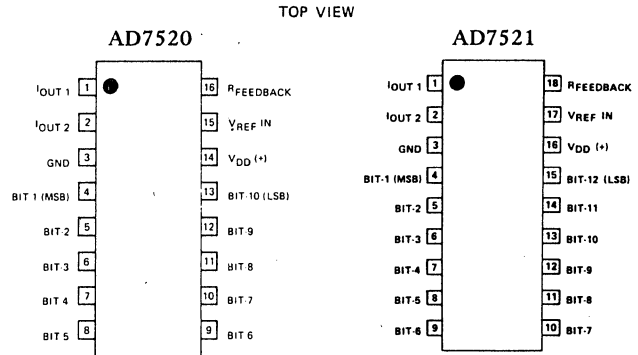
ORDERING INFORMATION

Nonlinearity	Temperature Range	
	0 to +75°C	-55°C to +125°C
0.2% (8-BIT)	AD7520JD AD7520JN AD7521JD AD7521JN	AD7520SD AD7521SD
0.1% (9-BIT)	AD7520KD AD7520KN AD7521KD AD7521KN	AD7520TD AD7521TD
0.05% (10-BIT)	AD7520LD AD7520LN AD7521LD AD7521LN	AD7520UD AD7521UD

PACKAGE IDENTIFICATION

Suffix D: Ceramic DIP package
 Suffix N: Plastic DIP package

PIN CONFIGURATION



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FEATURES

- 10-Bit Resolution
- 8, 9, & 10-Bit Linearity
- Microprocessor Compatible
- Double Buffered Inputs
- Serial or Parallel Loading
- DTL/TTL/CMOS Direct Interface
- Nonlinearity Tempco: 2ppM of FSR/°C
- Gain Tempco: 10ppM of FSR/°C
- Very Low Power Dissipation
- Very Low Feedthrough

GENERAL DESCRIPTION

The AD7522 is a monolithic CMOS 10-bit multiplying D/A converter, with an input buffer and a holding register, allowing direct interface with microprocessors. Most applications require the addition of only an operational amplifier and a reference voltage.

The key to easy interface to a data bus is the AD7522's ability to load the input buffer in two bytes (an 8-bit and a 2-bit byte), and subsequently move this data to a holding register, where the digital word is converted into an analog current or voltage (with external operational amplifier). The input loading of either 8 or 10 bits can be done in a parallel or serial mode.

The AD7522 is packaged in a 28-pin DIP, and operates with a +15V main supply at 2mA max, and a logic supply of +5V for TTL interface, or +10 to +15V for CMOS interface.

A thin film on high density CMOS process, using silicon nitride passivation, ensures high reliability and excellent stability.

ORDERING INFORMATION

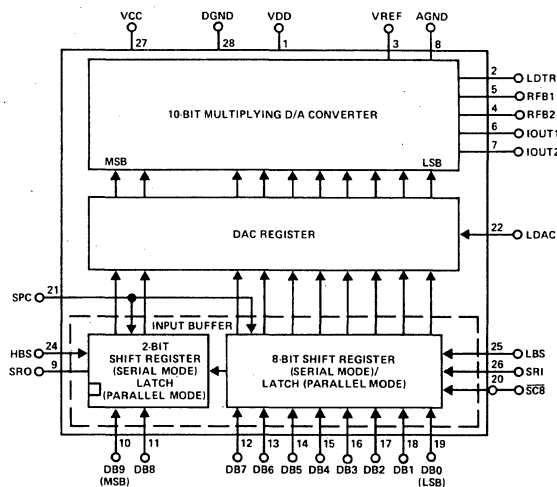
Nonlinearity	Temperature Range	
	0°C to +75°C	-55°C to +125°C
0.2% FSR (8-Bit)	AD7522JD AD7522JN	AD7522SD
0.1% FSR (9-Bit)	AD7522KD AD7522KN	AD7522TD
0.05% FSR (10-Bit)	AD7522LD AD7522LN	AD7522UD

PACKAGE IDENTIFICATION

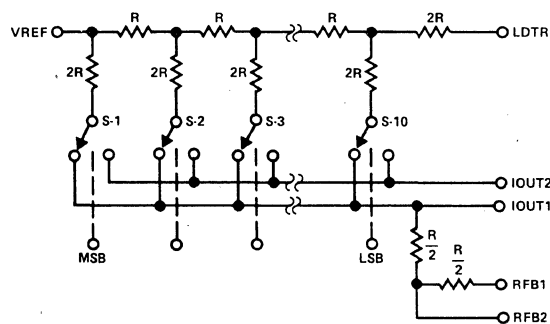
- Suffix "D": Ceramic DIP Package
- Suffix "N": Plastic DIP Package

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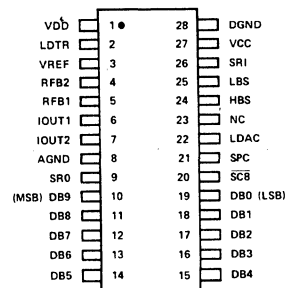
FUNCTIONAL DIAGRAM



D/A CONVERTER DIAGRAM



PIN CONFIGURATION



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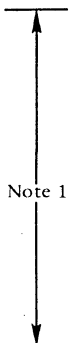
INTERFACE

Analog Devices

Pin Function Description

PIN	MNEMONIC	DESCRIPTION
1	VDD	+15V (nominal) Main Supply.
2	LDTR	R-2R Ladder Termination Resistor. Normally grounded for unipolar operation or terminated at IOUT2 for bipolar operation.
3	VREF	Reference Voltage Input. Since the AD7522 is a multiplying DAC, VREF may vary over the range of $\pm 10V$.
4	RFB2	$R_{feedback} \div 2$; gives full scale equal to $VREF/2$.
5	RFB1	$R_{feedback}$, used for normal unity gain (at full scale) D/A conversion.
6	IOUT1	DAC Current OUT-1 Bus. Normally terminated at virtual ground of output amplifier.
7	IOUT2	DAC Current OUT-2 Bus, terminated at ground for unipolar operation, or virtual ground of op amp for bipolar operation.
8	AGND	Analog Ground. Back gate of DAC N-channel SPDT current steering switches.
9	SRO	Serial Output. An auxiliary output for recovering data in the input buffer.
10	DB9	Data Bit 9. Most significant parallel data input.
11	DB8	Data Bit 8.
12	DB7	Data Bit 7.
13	DB6	Data Bit 6.
14	DB5	Data Bit 5.
15	DB4	Data Bit 4.
16	DB3	Data Bit 3.
17	DB2	Data Bit 2.
18	DB1	Data Bit 1.
19	DB0	Data Bit 0. Least significant parallel data input.
20	SC8	8-Bit Short Cycle Control. When in serial mode, if SC8 is held to logic "0," the two least significant input latches in the input buffer are bypassed to provide proper serial loading of 8-bit serial words. If SC8 is held to logic "1," the AD7522 will accept a 10-bit serial word. Data bits 0(LSB) and DB1 are in a parallel load mode when SC8 = 0, and should be tied to a logic low state to prevent false data from being loaded.

Note 1



PIN	MNEMONIC	DESCRIPTION
21	SPC	Serial/Parallel Control. If SPC is a logic "0," the AD7522 will load parallel data appearing on DB0 through DB9 into the input buffer when the appropriate strobe inputs are exercised (see HBS and LBS). If SPC is a logic "1," the AD7522 will load serial data appearing on Pin 26 into the input buffers. Each serial data bit must be "strobed" into the buffer with the HBS and LBS.
22	LDAC	Load DAC: When LDAC is a logic "0," the AD7522 is in the "hold" mode, and digital activity in the input buffer is locked out. When LDAC is a logic "1," the AD7522 is in the "load" mode, and data in the input buffer loads the DAC register.
23	NC	No Connection.
24	HBS	High Byte Strobe. When in "parallel load" mode (SPC = 0), parallel data appearing on the DB9 (MSB) and DB8 data inputs will be "clocked" into the input buffer on the positive going edge of HBS. When in "serial load" mode (SPC = 1), serial data bits appearing at the serial input terminal, Pin 26, will be "clocked" into the input buffer on the positive going edges of HBS and LBS. (HBS and LBS must be clocked simultaneously when in "serial load" mode.)
25	LBS	Low Byte Strobe. When in "parallel load" mode (SPC = 0), parallel data appearing on the DB0 (LSB) through DB7 inputs will be "clocked" into the input buffer on the positive going edge of the LBS. When in "serial load" mode (SPC = 1), serial data bits appearing at the serial input terminal, Pin 26, will be "clocked" into the input buffer on the positive going edge of HBS and LBS. (HBS and LBS must be clocked simultaneously when in "serial load" mode.)
26	SRI	Serial Input.
27	VCC	Logic Supply. If +5V is applied, all digital inputs/outputs are TTL compatible. If +10V to +15V is applied, digital inputs/outputs are CMOS compatible.
28	DGND	Digital Ground.

Note 1: Logic "1" applied to a data bit steers that bit's current to the IOUT1 terminal.

FEATURES

- 8 and 10-Bit Resolution
- 20 μ sec Conversion Time
- Microprocessor Compatibility
- Very Low Power Dissipation
- Parallel and Serial Outputs
- Ratiometric Operation
- TTL/DTL/CMOS Logic Compatibility
- CMOS Monolithic Construction

GENERAL DESCRIPTION

The AD7570 is a monolithic CMOS 10-bit successive approximation A/D converter on a 120 by 135 mil chip, requiring only an external comparator, reference and passive clocking components. Ratiometric operation is inherent, since an extremely accurate multiplying DAC is used in the feedback loop.

The AD7570 parallel output data lines and Busy line utilize three-state logic to permit bussing with other A/D output and control lines or with other I/O interface circuitry. Two enables are available, one controls the two MSB's, the second controls the remaining 8 LSB's. This feature provides the control interface for most microprocessors which can accept only an 8-bit byte.

The AD7570 also provides a serial data output line to be used in conjunction with the serial synchronization line. The clock can be driven externally or, with the addition of a resistor and a capacitor, can run internally as high as 0.6 MHz allowing a total conversion time (8-bits) of typically 20 μ sec. An 8-bit short cycle control pin stops the clock after exercising 8 bits, normally used for the "J" version (8-bit resolution).

The AD7570 requires two power supplies, a +15V main supply and a +5V (for TTL/DTL logic) to +15V (for CMOS logic) supply for digital circuitry. Both analog and digital grounds are available.

The AD7570 is a monolithic device using a proprietary CMOS process featuring a double layer metal interconnect, on-chip thin-film resistor network and silicon nitride passivation ensuring high reliability and excellent long term stability.

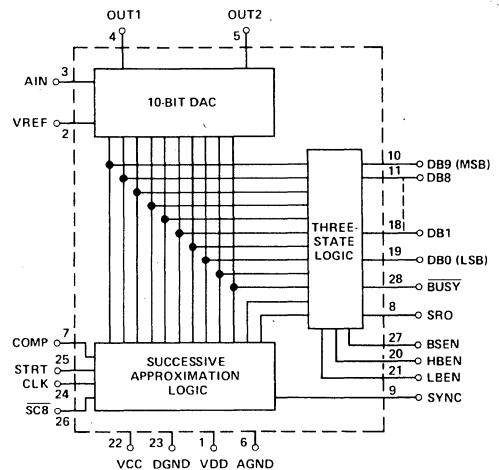
ORDERING INFORMATION

Resolution	Temperature Range
	0 to +75°C
8-Bit	AD7570J
10-Bit	AD7570L

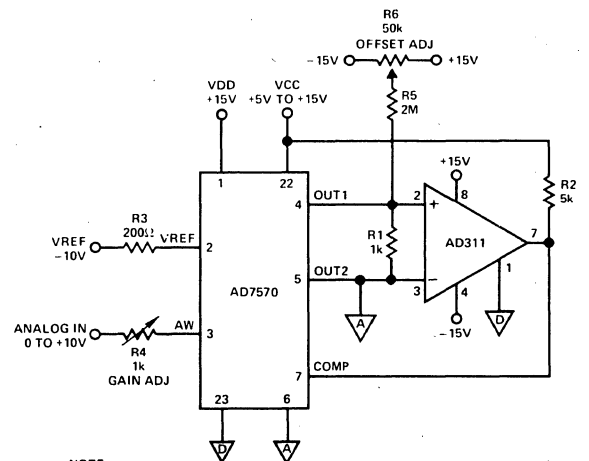
Suffix D: Ceramic Package

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FUNCTIONAL DIAGRAM

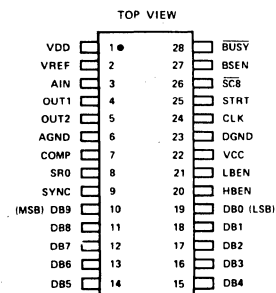


TYPICAL APPLICATION



NOTE:
IF POSITIVE VREF IS USED, THE ANALOG INPUT RANGE IS 0 TO -VREF, AND THE COMPARATOR'S (-) INPUT SHOULD BE CONNECTED TO OUT1 (PIN 4) OF THE AD7570.

PIN CONFIGURATION



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West Coast
213/595-1783

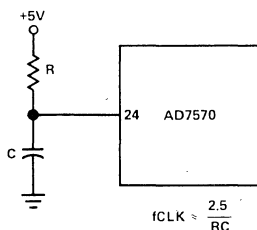
Mid-West
312/894-3300

Texas
214/231-5094

Pin Function Description

INPUT CONTROLS

1. Convert Start (pin 25 – STRT)
When the start input goes to logical 1, the MSB data latch is set to logic 1 and all other data latches are set to logic 0. When the start input returns low, the conversion sequence begins. The start command must remain high for at least 500 nanoseconds. If a start command is reinitiated *during* conversion, the conversion sequence starts over.
2. High Byte Enable (pin 20 – HBEN)
This is a three-state enable for the bit-9 (MSB) and bit 8. When the control is low, the output data lines for bits 9 and 8 are floating. When the control is high, digital data from the latches appears on the data lines.
3. Low Byte Enable (pin 21 – LBEN)
Same as High Byte Enable pin, but controls bits 0 (LSB) through 7.
4. Busy Enable (pin 27 – BSEN)
This is an interrogation input which requests the status of the converter, i.e., conversion in process or convert complete. The converter status is addressed by applying a logic 1 to the Busy Enable. (See Busy under Output Functions.)
5. Short Cycle 8-Bits (pin 26 – SC8)
With a logic 0 input, the conversion stops after 8 bits reducing the conversion time by 2 clock periods. This control should be exercised for proper operation of the “J” version. When a logic 1 is applied, a complete 10-bit conversion takes place (“L” version).
6. Clock (pin 24 – CLK)
With an external RC connected, as shown in the Figure below, clock activity begins upon receipt of a Convert-Start command to the A/D, and ceases upon completion of conversion. An external clock (CMOS or TTL/DTL levels) can directly drive the clock terminals, if required.



Generating Internal Clock Frequency

7. VDD (pin 1)
VDD is the positive supply for all analog circuitry plus some digital logic circuits that are not part of the TTL compatible input/output lines (back-gates to the P-channel devices). Nominal supply voltage is +15V.

8. VCC (pin 22)
VCC is the logic power supply. If +5V is used, all control inputs/outputs (with the exception of comparator terminal) are DTL/TTL compatible. If +15V is applied, control inputs/outputs are CMOS compatible.

OUTPUT FUNCTIONS

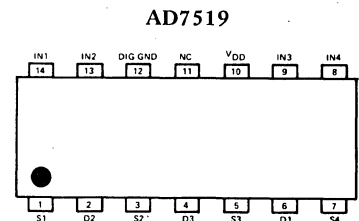
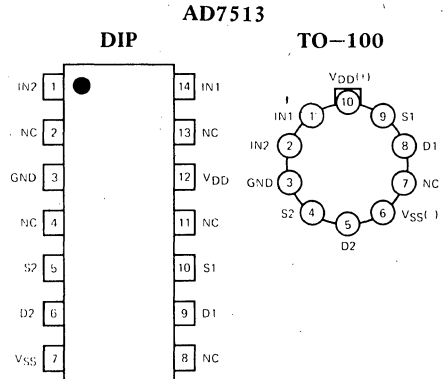
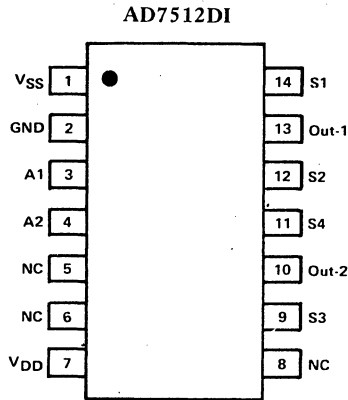
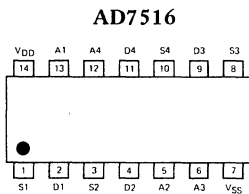
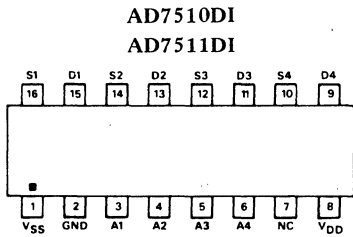
1. Busy (pin 28 – $\overline{\text{BUSY}}$)
The Busy line indicates whether conversion is complete or in process. Busy is a three-state output and floats until the Busy-Enable line is addressed with a logic 1. When addressed, Busy will indicate either a 1 (conversion complete) or a 0 (conversion in process).
2. Serial Output (pin 8 – SRO)
Provides output data in serial format. Data is available only during conversion. When the A/D is not converting, the Serial Output line “floats.” The Serial Sync (see next function) *must* be used, along with the Serial Output terminal to avoid misinterpreting data.
3. Serial Synchronization (pin 9 – SYNC)
Provides 10 positive edges, which are synchronized to the Serial Output pin. Serial Sync is floating if conversion is not taking place.

Note that all digital inputs/outputs are TTL/DTL compatible when VCC is +5V, and CMOS compatible when VCC is +15V.

Table 1. Function Table

PIN NO.	MNEMONIC	FUNCTION
1	VDD	Positive Supply (+15V)
2	VREF	Voltage REFERENCE ($\pm 10V$)
3	AIN	Analog INput
4	OUT1	DAC Current OUTput 1
5	OUT2	DAC Current OUTput 2
6	AGND	Analog GROUND
7	COMP	COMPARator
8	SRO	SeRIal Output
9	SYNC	Serial SYNChronization
10	DB9	Data Bit 9 (MSB)
11	DB8	Data Bit 8
12	DB7	Data Bit 7
13	DB6	Data Bit 6
14	DB5	Data Bit 5
15	DB4	Data Bit 4
16	DB3	Data Bit 3
17	DB2	Data Bit 2
18	DB1	Data Bit 1
19	DB0	Data Bit 0 (LSB)
20	HBEN	High Byte ENable
21	LBEN	Low Byte ENable
22	VCC	Logic Supply (+5V to +15V)
23	DGND	Digital GROUND
24	CLK	CLock
25	STRT	STaRT
26	$\overline{\text{SC8}}$	Short Cycle 8 Bits
27	$\overline{\text{BSEN}}$	BuSy ENable
28	$\overline{\text{BUSY}}$	BUSY

PIN CONFIGURATIONS (TOP VIEW)



PACKAGE INFORMATION

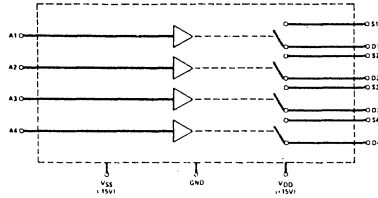
Suffix D – Ceramic DIP
 Suffix N – Plastic DIP
 Suffix H – TO-100

PERFORMANCE SELECTION TABLE (T_A = +25°C)

Parameter	Units	AD7510DI		AD7511DI		AD7512DI		AD7513		AD7516		AD7519
		AD7510	AD7511	Commercial	Military	Commercial	Military	Commercial	Military	Commercial	Military	Commercial
R _{ON} (MAX)	ohms		100			100		80	70	400		100
I _D (I _s) (MAX)	nA	5	3			5	3	5	2	125 ¹		---
I _{OUT} (MAX)	nA	---	---			15	9	---	---	---		---
t _{ON} (TYP)	μs		1μs			---	---	700		0.02		0.02
t _{OFF} (TYP)	μs		0.8μs			---	---	400		0.02		0.03
t _{transition} (TYP)	μs		---			1.2		---		---		---
I _{DD} ² (MAX)	mA	0.5	0.8			0.5	0.8	1	1	0.0005		0.001
I _{SS} ² (MAX)	mA	0.1	0.8			0.1	0.8	1	1	0.0005		---
Nominal Pwr. Supply	V		±15V			±15V		±15V		(V _{DD} -V _{SS}) = 15V		+8V

NOTES: ¹ For (V_{DD}-V_{SS}) = 10V
² For all digital inputs high (worst case).

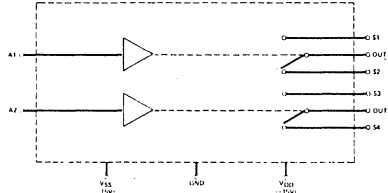
AD7510, AD7511
Quad SPST
Power Dissipation: $30\mu\text{W}$
TTL/DTL/CMOS Direct Interface
"Break-Before-Make" Switching
(AD7511)



AD7510: Address "HIGH" closes switch

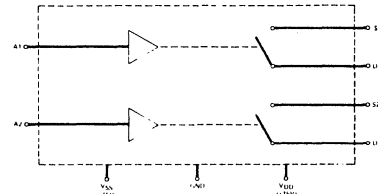
AD7511: Address "LOW" closes switch

AD7512
Dual SPDT
TTL/DTL/CMOS Direct Interface
Power Dissipation: $30\mu\text{W}$



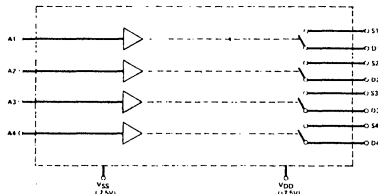
Address "HIGH" makes S-1 to OUT-1 and S-3 to OUT-2

AD7513
Dual SPST
TTL/DTL/CMOS Direct Interface



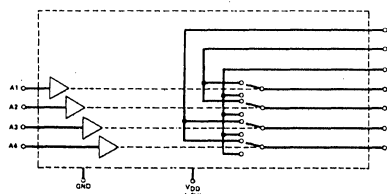
Address "LOW" Closes Switch

AD7516
Quad SPST
Switching Time: 20ns
Power Dissipation: $10\mu\text{W}$
CMOS Compatible



Address "HIGH" Closes Switch

AD7519
Quad SPDT Current Switch
Switching Time: 20ns
Power Dissipation: $8\mu\text{W}$
CMOS Compatible



Address "HIGH" Steers Current to D3 buss

INTERFACE

Analog Devices

Indestructible Analog CMOS Switches

AD7510DI
AD7511DI
AD7512DI

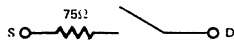
Pin For Pin
Spec For Spec
With

AD7510
AD7511
AD7512

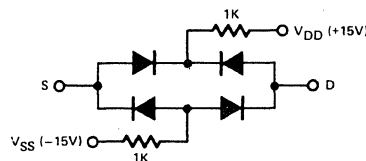
Latch Proof
and
Overvoltage Proof
without
Compromise!

EQUIVALENT CIRCUITS

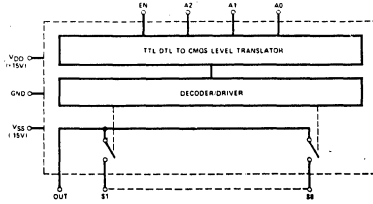
Signals Within The Power Supply Voltages



Signals Beyond The Power Supply Voltages



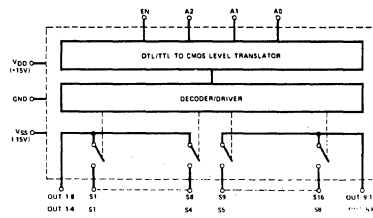
AD7501, AD7503
 8-Channel MUX
 TTL/DTL/CMOS Direct Interface
 Output "Enable" Control
 Power Dissipation: 30 μ W
 AD7503 Replaces HI-1818



AD7501				
A ₂	A ₁	A ₀	E _N	"ON"
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8
X	X	X	0	None

AD7503				
A ₂	A ₁	A ₀	E _N	"ON"
0	0	0	0	1
0	0	1	0	2
0	1	0	0	3
0	1	1	0	4
1	0	0	0	5
1	0	1	0	6
1	1	0	0	7
1	1	1	0	8
X	X	X	1	None

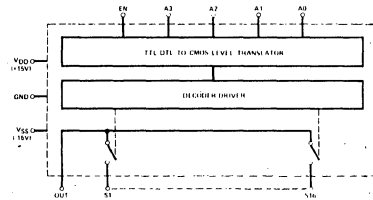
AD7502, AD7507
 4- & 8-Channel Differential MUX
 TTL/DTL/CMOS Direct Interface
 Output "Enable" Control
 AD7507 is superior plug-in replacement for DG-507



AD7502			
A ₁	A ₀	E _N	"ON"
0	0	1	1 & 5
0	1	1	2 & 6
1	0	1	3 & 7
1	1	1	4 & 8
X	X	0	None

AD7507				
A ₂	A ₁	A ₀	E _N	"ON"
0	0	0	1	1 & 9
0	0	1	1	2 & 10
0	1	0	1	3 & 11
0	1	1	1	4 & 12
1	0	0	1	5 & 13
1	0	1	1	6 & 14
1	1	0	1	7 & 15
1	1	1	1	8 & 16
X	X	X	0	None

AD7506
 16-Channel MUX
 TTL/DTL/CMOS Direct Interface
 Output "Enable" Control
 Power Dissipation: 1.5 mW
 Superior replacement for DG-506



AD7506				
A ₃	A ₂	A ₁	A ₀	E _N "ON"
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16
X	X	X	X	0 None

PERFORMANCE SELECTION TABLE (T_A = +25°C)

Parameter	Units	AD7501		AD7502		AD7506		AD7507	
		Commercial	Military ¹	Commercial	Military	Commercial	Military	Commercial	Military
R _{ON} (MAX)	ohms	300		300		450	400	450	400
I _S (MAX)	nA	2	0.5	2	0.5	5	1	5	1
I _{OUT} (MAX)	nA	10	5	5	3	20	10	10	5
t _{transition} (TYP)	μs	0.8		0.8		0.7		0.7	
I _{DD} ² (MAX)	mA	0.5	0.8	0.5	0.8	1		1	
I _{SS} ² (MAX)	mA	0.1	0.8	0.1	0.8	1		1	

NOTES: ¹ "Commercial" and "Military" refer to operating temperature ranges.
² For all digital inputs high (worst case).

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PRODUCT PROFILE

MOS/LSI

Siliconix offers a number of technologies in the MOS/LSI area, with a line of both standard and custom devices. Processing capability includes low V_{TH} in PMOS (metal gate), high-voltage CMOS (10 V – 30 V, metal gate) and low voltage CMOS (3 V – 15 V, metal gate). The most significant recent additions to our LSI product line are one-chip and two-chip (analog and digital) Integrated Circuits for A/D conversion.

FET Analog Switches

Siliconix's J-FET, MOS FET and Integrated Circuit technology has been utilized to produce an extensive family of Analog Switches. These Integrated Circuits are used in many high-reliability military and aerospace applications, such as the Mercury, Gemini, Apollo and Skylab manned space programs.

High performance multi-chip J-FET switches packaged with Integrated Circuit drivers offer low ON resistance, high OFF isolation, fast switching speed and excellent frequency response.

Since 1968, monolithic multi-channel PMOS switches with Integrated Drivers have been an integral part of the Siliconix Analog Switch family.

Most recent additions to the family have been CMOS switches and multiplexers of up to sixteen channels. These devices will switch analog voltages up to 30 Volts peak-to-peak.

Field Effect Transistors

Siliconix has maintained technical leadership in P- and N-Channel Junction FETs, and offers the most complete product line in the industry. FETs are characterized for such applications as low-drive d-c amplifiers, low-noise low-frequency

amplifiers, high-frequency amplifiers (to 1 GHz), low gate current circuits (10^{-13} A), and analog switching (ON resistance as low as 2Ω).

Both N- and P-Channel MOS FETs are also available, with applications aimed mainly at analog switching. P-Channel enhancement mode devices are offered with ON resistance ranging from 20Ω to $1K \Omega$, and with breakdown voltages as high as 75 V. N-Channel MOS FETs are available in either enhancement or depletion mode structures. Depletion mode devices are also used in amplifiers with very low input currents ($r_{DS} 10^{13} \Omega$).

High Reliability Devices

Siliconix capability in providing high-reliability devices to meet stringent military or aerospace applications is amply demonstrated by the company's qualification as a supplier for Mercury, Gemini, Apollo and the Viking 75 Mars orbiter/lander. Siliconix has a number of standard Hi-Rel screening options that can be applied to standard products. These options include MIL-STD-883 for microcircuits and MIL-STD-750 for discrete FETs. In addition, Siliconix offers certain JEDEC-registered FETs with JAN or JANTX processing, and has the capability of doing JANTXV processing. If other screening options are required to meet individual customer requirements, Siliconix can provide special additional inspections and controls to meet the most exacting demands.

The company has an in-house Scanning Electron Microscope facility and maintains many on-going product and process evaluation programs for standard products. Siliconix can supply SEM qualified products to meet individual customer requirements.

ANALOG SWITCH CONDENSED SPECIFICATIONS

Basic Part No. (Notes 1 & 2)	Switch Type	r _{DS(on)} Max (Ω) (Note 3)	Analog Voltage Range (p-p V) (Note 3)	Switching Time (μsec)		Logic State for ON Switch	Logic Levels (V)		Opt. Sup. Voltage (V)			Comments
				t _{ON}	t _{OFF}		V _{INL}	V _{INH}	(+) Sup. V ₁	(-) Sup. V ₂	Logic Sup. V _L	
TWO CHANNEL SPST												
*DGM111	PMOS	75-200	20	0.3	1.0	0	0.5	4.6	10	-20	5	-
DG133	N-JFET	30	20	0.6	1.6	1	0.8	2.5	12	-18	-	0
DG134	N-JFET	80	20	0.6	1.6	1	0.8	2.5	12	-18	-	0
DG141	N-JFET	10	20	1.0	2.5	1	0.8	2.5	12	-18	-	0
DG151	N-JFET	15	15	1.0	2.5	1	0.8	2.5	15	-15	-	0
DG152	N-JFET	50	15	0.8	1.6	1	0.8	2.5	15	-15	-	0
*DG180	N-JFET	10	20	0.3	0.25	0	0.8	2.0	10	-20	5	0
		10	15	0.3	0.25	0	0.8	2.0	15	-15	5	0
*DG181	N-JFET	30	20	0.15	0.13	0	0.8	2.0	10	-20	5	0
		30	15	0.15	0.13	0	0.8	2.0	15	-15	5	0
*DG182	N-JFET	75	20	0.25	0.13	0	0.8	2.0	10	-20	5	0
		75	20	0.25	0.13	0	0.8	2.0	15	-15	5	0
*DG200	CMOS	70	30	1.0	0.5	0	0.8	2.4	15	-15	-	(Note 9)
FOUR CHANNEL SPST												
*DG172	PMOS	150-450	20	0.3	0.75	0	0.8	2.0	10	-20	5	0
*DG201	CMOS	175	30	1.0	0.5	0	0.8	2.4	15	-15	-	(Note 9)
FIVE CHANNEL SPST												
DG123	PMOS	100-450	20	0.3	2.0	1	0.4	1 mA(6)	10	-20	-	0
DG125	PMOS	100-450	20	0.3	2.0	0	0.5	4.6	10	-20	5	-
ONE CHANNEL SPDT												
DG143	N-JFET	80	20	0.8	1.6	(Note 4)	2.0	3.0	12	-18	-	0
DG144	N-JFET	30	20	0.8	1.6	(Note 4)	2.0	3.0	12	-18	-	0
DG146	N-JFET	10	20	1.0	2.5	(Note 4)	2.0	3.0	12	-18	-	0
DG161	N-JFET	15	15	1.0	2.5	(Note 4)	2.0	3.0	15	-15	-	0
DG162	N-JFET	50	15	0.8	1.6	(Note 4)	2.0	3.0	15	-15	-	0
*DG175	PMOS	75-200	20	0.2	0.5	(Note 5)	0.8	2.0	10	-20	5	0
*DG186	N-JFET	10	20	0.3	0.25	(Note 5)	0.8	2.0	10	-20	5	0
		10	15	0.3	0.25	(Note 5)	0.8	2.0	15	-15	5	0
*DG187	N-JFET	30	20	0.15	0.13	(Note 5)	0.8	2.0	10	-20	5	0
		30	15	0.15	0.13	(Note 5)	0.8	2.0	15	-15	5	0
*DG188	N-JFET	75	20	0.25	0.13	(Note 5)	0.8	2.0	10	-20	5	0
		75	20	0.25	0.13	(Note 5)	0.8	2.0	15	-15	5	0
*SI3002	PMOS	100-400	20	1.0	1.5	(Note 5)	0.8	2.0	10	-20	-	0
TWO CHANNEL SPDT												
*DG189	N-JFET	10	20	0.3	0.25	(Note 5)	0.8	2.0	10	-20	5	0
		10	15	0.3	0.25	(Note 5)	0.8	2.0	15	-15	5	0
*DG190	N-JFET	30	20	0.15	0.13	(Note 5)	0.8	2.0	10	-20	5	0
		30	15	0.15	0.13	(Note 5)	0.8	2.0	15	-15	5	0
*DG191	N-JFET	75	20	0.25	0.13	(Note 5)	0.8	2.0	10	-20	5	0
		75	20	0.25	0.13	(Note 5)	0.8	2.0	15	-15	5	0
THREE CHANNEL SPDT												
*DG170	PMOS	200-800	20	0.3	0.4	(Note 5)	0.8	2.0	10	-20	5	0
TWO CHANNEL DPST												
*DGM122	PMOS	100-450	20	0.3	2.0	1	0.4	1 mA(6)	10	-20	5	0
DG126	N-JFET	80	20	0.6	1.6	1	0.8	2.5	12	-18	-	0
DG129	N-JFET	30	20	0.6	1.6	1	0.8	2.5	12	-18	-	0
DG140	N-JFET	10	20	1.0	2.5	1	0.8	2.5	12	-18	-	0
DG153	N-JFET	15	15	1.0	2.5	1	0.8	2.5	15	-15	-	0
DG154	N-JFET	50	15	0.6	1.6	1	0.8	2.5	15	-15	-	0
*DG183	N-JFET	10	20	0.3	0.25	1	0.8	2.0	10	-20	5	0
		10	15	0.3	0.25	1	0.8	2.0	15	-15	5	0
*DG184	N-JFET	30	20	0.15	0.13	1	0.8	2.0	10	-20	5	0
		30	15	0.15	0.13	1	0.8	2.0	15	-15	5	0
*DG185	N-JFET	75	20	0.25	0.13	1	0.8	2.0	10	-20	5	0
		75	20	0.25	0.13	1	0.8	2.0	15	-15	5	0
ONE CHANNEL DPDT												
DG139	N-JFET	30	20	0.8	1.6	(Note 4)	2.0	3.0	12	-18	-	0
DG142	N-JFET	80	20	0.8	1.6	(Note 4)	2.0	3.0	12	-18	-	0
DG145	N-JFET	10	20	1.0	2.5	(Note 4)	2.0	3.0	12	-18	-	0
DG163	N-JFET	15	15	1.0	2.5	(Note 4)	2.0	3.0	15	-15	-	0
DG164	N-JFET	50	15	0.8	1.6	(Note 4)	2.0	3.0	15	-15	-	0
*DG173	PMOS	150-450	20	0.2	0.7	(Note 5)	0.8	2.0	10	-20	5	0
EIGHT CHANNEL MUX + ENABLE												
*DG501	PMOS	150-250	10	1.5	(Note 8)	(Note 7)	0.6	3.5	5	-20	-	0
*DG503	PMOS	150-800	20	1.5	(Note 8)	(Note 7)	0.6	8.5	10	-20	-	0
*DG508	CMOS	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	-	(Note 9)
SI3705	PMOS	150-400	10	1.5	(Note 8)	(Note 7)	0.6	3.5	5	-20	-	0
SIXTEEN CHANNEL MUX + ENABLE												
*DG506	CMOS	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	-	(Note 9)
FOUR CHANNEL DIFFERENTIAL MUX												
*DG509	CMOS	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	-	(Note 9)
*DG511	PMOS	175-600	20	1.2	(Note 8)	(Note 7)	0.8	2.0	10	-20	-	0
EIGHT CHANNEL DIFFERENTIAL MUX + ENABLE												
*DG507	CMOS	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	-	(Note 9)
FOUR CHANNEL SPDT D/A CONVERTER SUMMING NODE SWITCHES												
*DG515	NMOS	See Comments	-	120	170	(Note 5)	0.5	7.5	8.0	0	-	-
TEN CHANNEL SPDT D/A CONVERTER SUMMING NODE SWITCHES												
*DG516	NMOS	See Comments	-	120	170	(Note 5)	0.5	7.5	8.0	0	-	-

- NOTES:**
- (1) *Devices recommended for new designs are indicated in bold face type.
 - (2) The first suffix added to a basic part number indicates the device temperature range. The second suffix, the package type.
 - (3) Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. Values shown are for temperature suffix A (see Note 2).
 - (4) Input reference voltage of 2.5 V is required (see data sheets).
 - (5) See data sheet for switch state of differential switches.
 - (6) Current Driven Device - I_{INH} = 1 mA
 - (7) For truth table see data sheet.
 - (8) The appropriate switching characteristic for multiplexers is t_{TRANSITION}, not t_{ON}, t_{OFF}.
 - (9) V_{REF} = 1.5 V is used when supply voltages < ±15 V are used. Not needed when supply voltages of ±15 V are used.

DG180-185 – Two-Channel SPST
 DG183-185 – Two-Channel DPST
 DG186-188 – One-Channel SPDT
 DG189-191 – Two-Channel SPDT

Military (A Suffix) -55 to +125°C
 Industrial (B Suffix) -20 to +85°C

FEATURES

- Constant ON-Resistance over full Analog Range.
- Cross-Talk and Open Switch Isolation, > 80 dB at 1 MHz (75 Ohm Load).
- t_{off} , t_{on} Break-Before-Make Action.
- TTL, DTL, RTL, Direct Drive Compatibility.

ABSOLUTE MAXIMUM RATINGS

$V_{CC} - V_{EE}$	36 V
$V_{CC} - V_D$	33 V
$V_D - V_{EE}^{\dagger}$	33 V
$V_D - V_S$	± 22 V
$V_L - V_{EE}$	36 V
$V_L - V_{IN}$	8 V
$V_L - V_R$	8 V
$V_{IN} - V_R$	8 V
$V_R - V_{EE}$	27 V
$V_R - V_{IN}$	2 V
Current (Any Terminal) $\dagger\dagger$	30 mA
Power Dissipation*	
Metal Can**	450 mW
Flat Package***	750 mW
14 Pin DIP****	825 mW
16 Pin DIP $\dagger\dagger\dagger$	900 mW

*All leads welded or soldered to PC board.
 **Derate 6 mW/°C above 75°C.
 ***Derate 10 mW/°C above 75°C.
 ****Derate 11 mW/°C above 75°C.
 \dagger DG180, 83, 86, 89 – 30 V
 $\dagger\dagger$ DG180, 83, 86, 89 – S or D Terminals – 200 mA
 $\dagger\dagger\dagger$ Derate 12 mW/°C above 75°C.

POWER SUPPLY	ANALOG RANGE	
	DG180,181,183,184,186,187,189,190	DG182,185,188,191
± 15 V	-7.5V/+15V	-10V/+15V
10/-20V	-12V/+10V	-15V/+10V

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

TEST CONDITIONS, UNLESS NOTED:
 $V_{CC} = 15V$, $V_{EE} = -15V$, $V_L = 5V$, $V_R = 0$

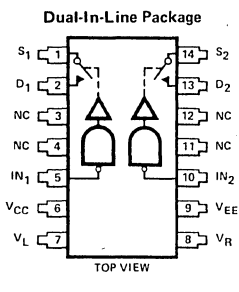
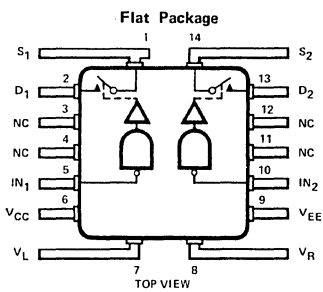
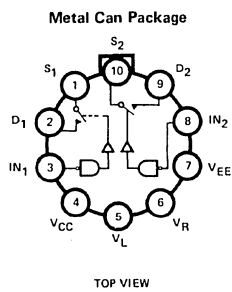
MAXIMUM LIMITS

Type (Temp. Suffix) ↓	$r_{DS(on)}$ - V_A MAX -10 mA		$I_{S(off)}/I_{D(off)}$		$I_{D(on)} + I_{S(on)}$ $V_D = V_S = -V_A$		t_{ON}	t_{OFF}	I_{CC} $V_{IN} = 0/V_{IN} = 5$	I_{EE} $V_{IN} = 0/V_{IN} = 5V$	I_L $V_{IN} = 0/V_{IN} = 5$
	Ω @ 25°C	nA @ 25°C	nA @ T MAX.	nA @ 25°C	nA @ T MAX.	ns @ 25°C	ns @ 25°C	mA @ 25°C	mA @ 25°C	mA @ 25°C	
TWO-CHANNEL SPST											
DG180A	10	10	1000	-2	-200	300	250	1.5	-5	4.5	
DG180B	15	15	300	-10	-200	350	300	1.5	-5	4.5	
DG181A	30	1	100	-2	-200	150	130	1.5	-5	4.5	
DG181B	50	5	100	-10	-200	180	150	1.5	-5	4.5	
DG182A	75	1	100	-2	-200	250	130	1.5	-5	4.5	
DG182B	100	5	100	-10	-200	300	150	1.5	-5	4.5	
ONE-CHANNEL SPDT											
DG186A	10	10	1000	-2	-200	300	250	0.8	-3	3.2	
DG186B	15	15	300	-10	-200	350	300	0.8	-3	3.2	
DG187A	30	1	100	-2	-200	150	130	0.8	-3	3.2	
DG187B	50	5	100	-10	-200	180	150	0.8	-3	3.2	
DG188A	75	1	100	-2	-200	250	130	0.8	-3	3.2	
DG188B	100	5	100	-10	-200	300	150	0.8	-3	3.2	
TWO-CHANNEL SPDT											
DG189A	10	10	1000	-2	-200	300	250	1.5	-5	4.5	
DG189B	15	15	300	-10	-200	350	300	1.5	-5	4.5	
DG190A	30	1	100	-2	-200	150	130	1.5	-5	4.5	
DG190B	50	5	100	-10	-200	180	150	1.5	-5	4.5	
DG191A	75	1	100	-2	-200	250	130	1.5	-5	4.5	
DG191B	100	5	100	-10	-200	300	150	1.5	-5	4.5	
TWO-CHANNEL DPST											
DG183A	10	10	1000	-2	-200	300	250	3/0.1	-4	4.5	
DG183B	15	15	300	-10	-200	350	300	3/0.1	-4	4.5	
DG184A	30	1	100	-2	-200	150	130	3/0.1	-4	4.5	
DG184B	50	5	100	-10	-200	180	150	3/0.1	-4	4.5	
DG185A	75	1	100	-2	-200	250	130	3/0.1	-4	4.5	
DG185B	100	5	100	-10	-200	300	150	3/0.1	-4	4.5	

DG180-191	$V_{INH(MIN)} - 2.0V$ $V_{INL(MAX)} - 0.8V$ $I_{INH}(V_{IN} = 5, T_{MIN}) - 10 \mu A$	$I_{INH}(V_{IN} = 5, T_{MAX}) - 20 \mu A$ $I_{INL}(V_{IN} = 0, T_{MIN} \text{ to } T_{MAX}) - -250 \mu A$ $I_R(V_{IN} = 0/V_{IN} = 5, @ 25^\circ C) = -2 \text{ mA}$
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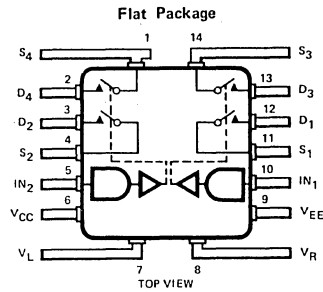
Siliconix INTERFACE

TWO-CHANNEL SPST (DG180-182)

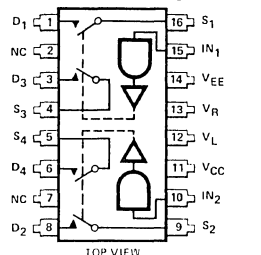


SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

TWO-CHANNEL DPST (DG183-185)

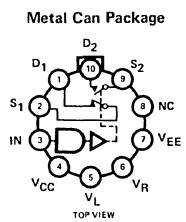


Dual-In-Line Package

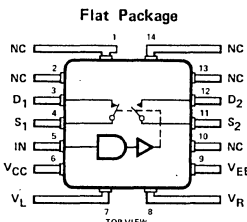


SWITCH STATES ARE FOR LOGIC "0" INPUT (POSITIVE LOGIC)

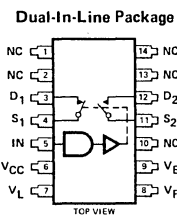
ONE-CHANNEL SPDT (DG186-188)



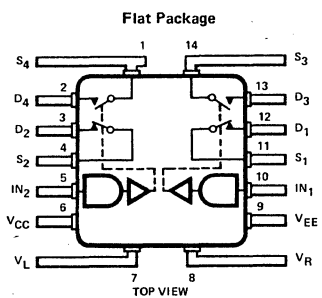
TO-100



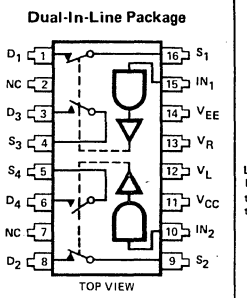
SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)



TWO-CHANNEL SPDT (DG189-191)

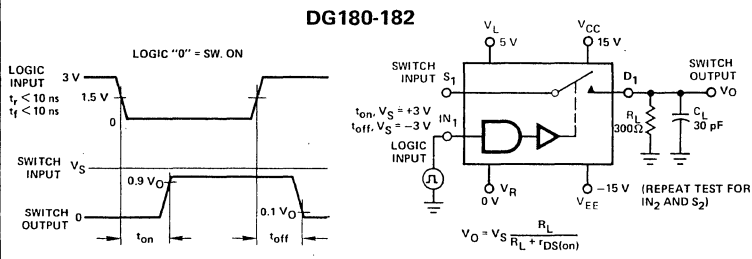


SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

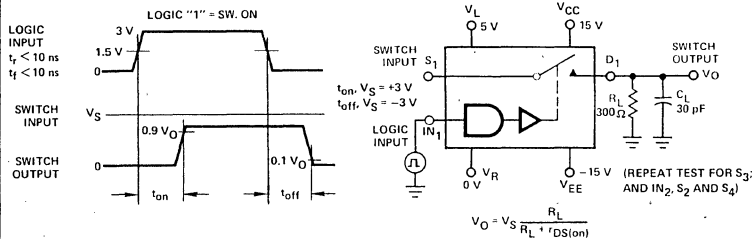


SWITCHING TIME TEST CIRCUIT

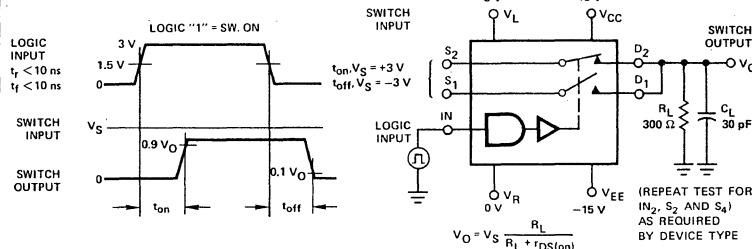
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



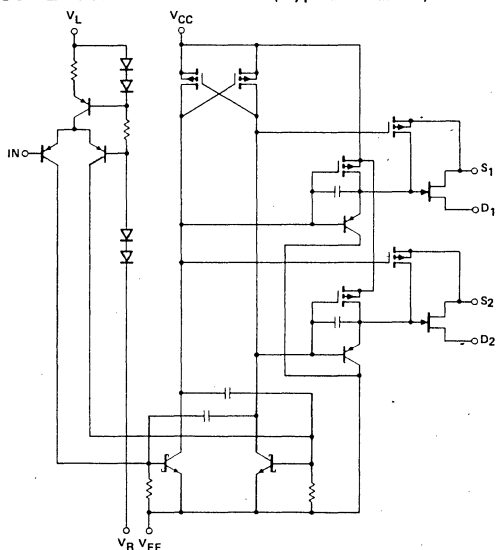
DG183-185



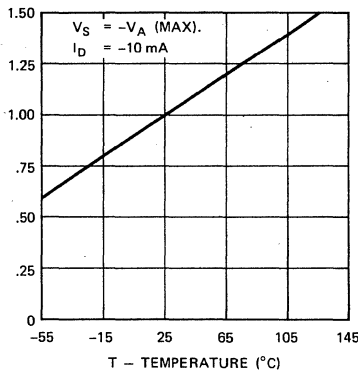
DG186-191



SCHEMATIC DIAGRAM (Typical Channel)

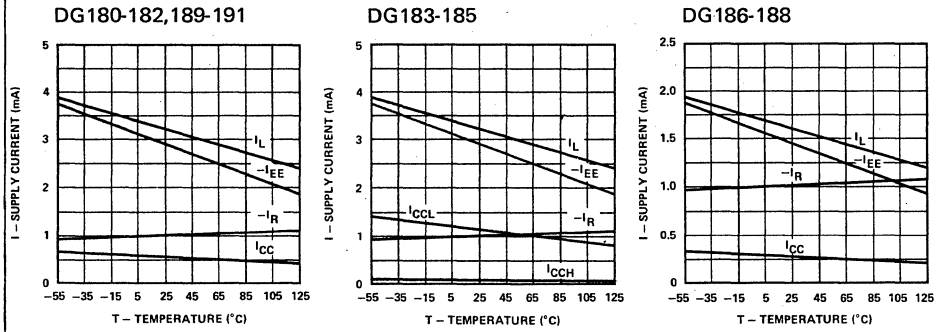


$I_{DS(on)}$ vs. Temperature

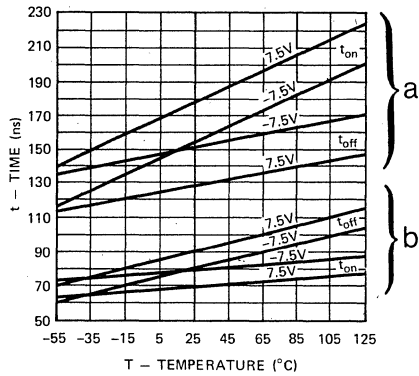


NORMALIZED CURVE

Supply Current vs. Temperature



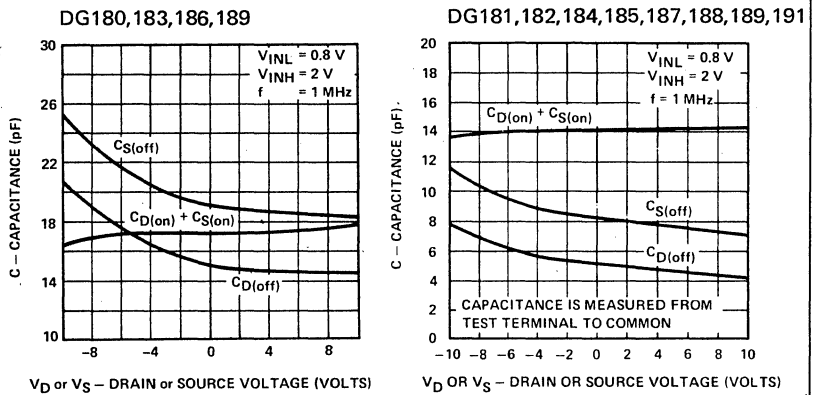
Switching Time vs. V_D and Temperature



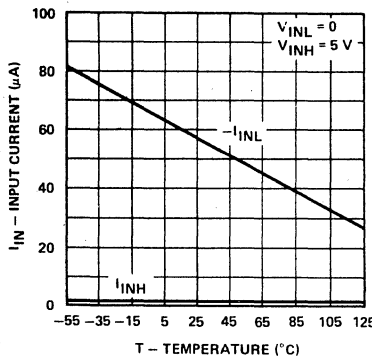
a-DG180,183,186,189

b-DG181,182,184,185,187,188,190,191

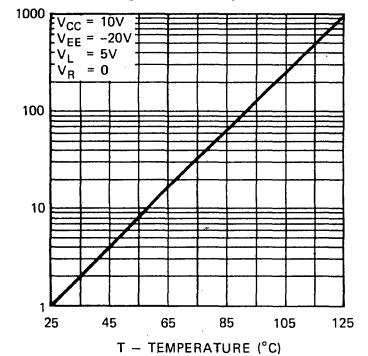
Capacitance vs. V_D or V_S



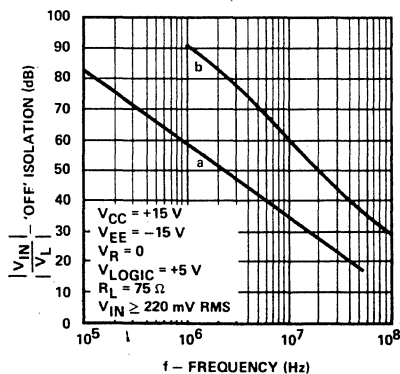
I_{IN} vs V_{IN} and Temperature



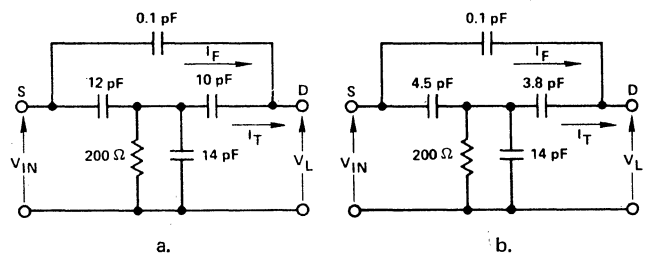
Leakage vs Temperature



"OFF" Isolation vs. Frequency



Equivalent "OFF" Circuit



a-DG180,183,186,189

b-DG181,182,184,185,187,188,190,191

DG501 8-CHANNEL MULTIPLEX SWITCH WITH DECODE

Military (A Suffix) -55 to +125°C
 Industrial (B Suffix) -20 to +85°C
 Commercial (C Suffix) 0 to +70°C

FEATURES

- Break-Before Make Switching
- One-Out-Of-Eight Decoder on the Chip
- Pull-Up Resistors On Inputs For TTL Compatibility
- Output Enable Control
- ±5V Analog Signal Range
- Voltage-Limiter Diodes Protect MOS Gates
- Zero Offset Voltage

ABSOLUTE MAXIMUM RATINGS

$V_{SS} - V_{DD}$	-0.3, +30V
$V_{SS} - V_A, V_{En}$	-0.3, +30V
$V_{SS} - V_D$ or V_S	-0.3, +30V
$V_D - V_S$	±25V
$V_A, V_{En} - V_{DD}$	30V
V_D or $V_S - V_{DD}$	30V
Current (Any Terminal)	-20 mA
Power Dissipation*	
16 Pin DIP**	825 mW
16 Pin Plastic DIP***	470 mW

*Device mounted with all leads welded or soldered to PC board.
 **Derate 11 mW/°C above 75°C.
 ***Derate 6.5 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

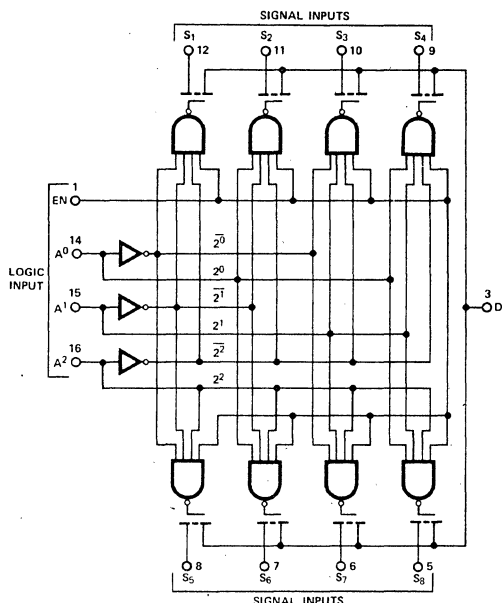
TEST CONDITIONS, UNLESS NOTED:
 $V_{DD} = -20V, V_{SS} = 5V, V_{En} = 3.5V$
 $V_{AL} = 0.6V, V_{AH} = 3.5V$

MAXIMUM LIMITS

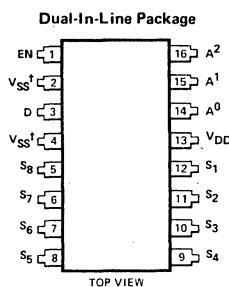
Type (Temp. Suffix)†	$r_{DS(on)}$		$I_{S(off)}/I_{D(off)}$		$I_{D(on)} + I_{S(on)}$		$I_{INL(MAX)}$	$I_{INH(MIN)}$	t_{TRANS}^1	I_{DD}	I_{SS}
	$V_S = -5V$ $V_{DD} = -20$ $I_S = -1$ mA	$V_{DD} = -15$ $I_S = -100$ μA	$V_S = -5, V_D = 5/V_D = -5, V_S = 5$	$V_D = V_S = 5V$	$V_{AL} = 0$	$V_{AH} = 3.5$	Sw. time of MUX $V_{DD} = -20/-15$	$V_{En} = 0/3.5$ All $V_{ADD} = 0$	$V_{En} = 0/3.5$ All $V_{ADD} = 0$		
	Ω @ 25°C	Ω @ 25°C	nA @ 25°C	nA @ T_{MAX}	nA @ 25°C	nA @ T_{MAX}	mA @ 25°C	μA @ 25°C	μS @ 25°C	mA @ 25°C	mA @ 25°C
DG501A	250	600	-1/-8	-1000/-4000	8	4000	-1.2	-150	1.5/2.5	-6	8/7
DG501B (-20° to +85°C) DG501C (0 to +70°C)	250	800	-3/-10	-150/-500	10	500	-1.2	-150	1.5/2.5	-6	8/7

† NOTE: $V_{S1} = ±1V, V_{S8} = ±1V, V_{S2-7} = gnd.$

FUNCTIONAL DIAGRAM



PIN CONFIGURATION

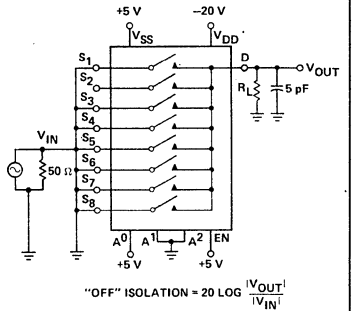
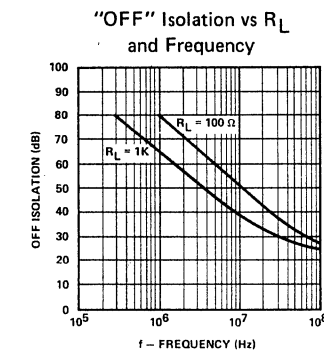
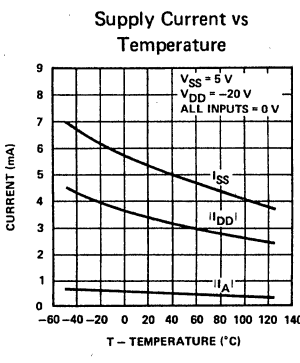
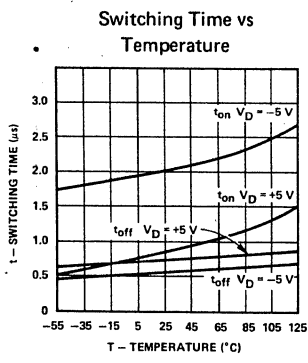
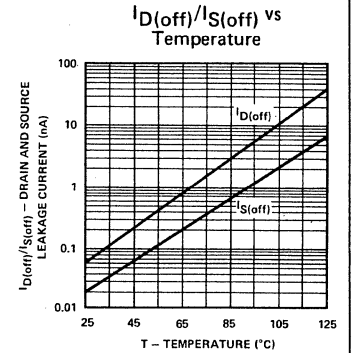
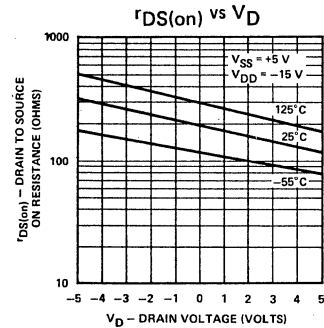
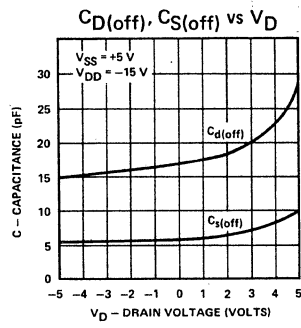
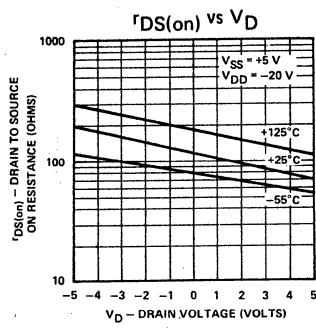


† Both V_{SS} lines are internally connected, either one or both may be used. V_{SS} common to substrate.

TRUTH TABLE

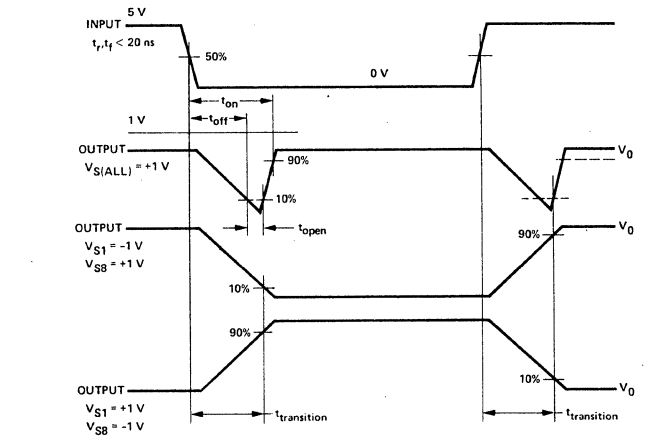
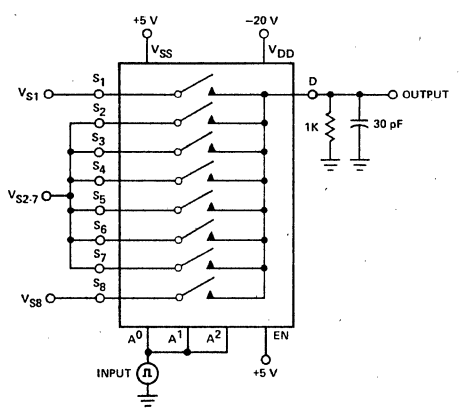
LOGIC INPUTS				CHANNEL
A^0	A^1	A^2	En	'ON'
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

TYPICAL CHARACTERISTICS



INTERFACE Siliconix

SWITCHING TIME TEST CIRCUIT



DGM111 2-CHANNEL SPST MOS SWITCH WITH DRIVER
 DGM122 2-CHANNEL DPST MOS SWITCH WITH DRIVER
 DG170 3 x SPDT MOX SWITCH WITH DRIVER
 DG172 4-CHANNEL MOS SWITCH WITH DRIVER
 DG173 DPDT MOS SWITCH WITH DRIVER
 DG175 SPDT MOS SWITCH WITH DRIVER

Military (A Suffix) -55 to +125°C
 Industrial (B Suffix) -20 to +85°C
 Commercial (C Suffix) 0 to +70°C

FEATURES

- P-Channel MOS FET Switches With Drivers
- Make-Before-Break Switch Function
- 20V Peak-to-Peak Signal Handling Capability
- TTL, DTL, RTL Direct Drive Compatibility — No Interface Components Required
- Voltage-Limiting Diodes Protect MOS Gates

ABSOLUTE MAXIMUM RATINGS

$V_{CC} - V_{EE}$	36V
$V_{CC} - V_D$	25V
$V_{CC} - V_D$ or V_S , DGM111	-0.5, 25V
$V_{CC} - V_S$	25V
$V_S - V_{EE}$	36V
$V_S - V_D$	±25V
$V_D - V_{EE}$	36V
$V_L - V_{EE}$	30V
$V_L - V_{EE}$, DGM122	25V
$V_L - V_{IN}$	±6V
$V_L - V_{IN}$, DG170	±12V
$V_L - V_{IN}$, DGM122	6V
$V_L - V_R$, DG170-175	±6V
$V_R - V_{EE}$	25V
$V_{IN} - V_R$, DG172-175	±6V
$V_{IN} - V_R$, DG170	+18 -6V
$V_{IN} - V_R$, DGM122	2V

CURRENT ANY TERMINAL

DGM111, DGM122	30 mA
DG172-175	20 mA
DG170	12 mA
PEAK I_S, I_D, I_D (DG170)	100 mA

(200µs pulse width, 100pps)

***POWER DISSIPATION**

TO-100 METAL CAN 1	450 mW
FLAT PACKAGE 2	750 mW
14-PIN DIP 3	825 mW
14-PIN PLASTIC DIP 4	470 mW
16-PIN DIP 3	825 mW
16-PIN PLASTIC DIP 5	470 mW

- *All leads welded or soldered to PC board.
- 1 Derate 6 mW/°C above 75°C
 - 2 Derate 10 mW/°C above 75°C
 - 3 Derate 11 mW/°C above 75°C
 - 4 Derate 6.3 mW/°C above 25°C
 - 5 Derate 6.5 mW/°C above +25°C

INTERFACE
Siliconix

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

TEST CONDITIONS, UNLESS NOTED
 $V_{CC} = 10V, V_{EE} = -20V, V_L^* = 5V, V_R = 0$
 * $V_L = 4.5V$ for DGM111, DGM122

MAXIMUM LIMITS

Type (Temp. Suffix)†	$r_{DS(on)}$ + V_A /- V_A -10 mA	$I_{S(off)}/I_{D(off)}$ - V_A			$I_{D(on)} + I_{S(on)}$ $V_D = V_C = +V_A$		I_{INL} T_{MIN} to T_{MAX} $V_{IN} = 0$	I_{INH} $V_{IN} = 5$		t_{ON}	t_{OFF}	I_{CC} $V_{IN} = 0/V_{IN} = 5$	$-I_{EE}$ $V_{IN} = 0/V_{IN} = 5$	I_L $V_{IN} = 0/V_{IN} = 5$	$-I_R$ $V_{IN} = 0/V_{IN} = 5$	
		Ω @ 25°C	nA @ 25°C	nA @ 85°C	nA @ 125°C	nA @ 25°C		nA @ T_{MAX}	mA							µA @ 25°C
DGM111A	75/200	-1		-1000	1	1000	-0.7 (0.5V)	1	10	300	1000	(0.5V/4.1V) 3 mA/10 µA 3.5 mA/10 µA				-
DGM111B	75/250	-5	-100		5	100	-1	10	10	300	1000	5 mA/0.20 µA ONE CHANNEL ON/ALL OFF				-
DGM122A	100/450	-1/-3		-1000/-3000	3	3000	1µA ($V_{IN} = 0.3$)	†		0.3	2	(0.4V/100 µA) 10 µA/3 mA 20 µA/6 mA				15 µA/1.5 mA
DGM122B	125/500	-5/-10	-100/-300		10	300	10µA ($V_{IN} = 0.3$)	†		0.5	2	20 µA/3 mA ALL CHANNELS OFF/ONE ON				25 µA/1.5 mA
DG170A	200/800	-1/-2		-1000/-2000	2	2000	-0.4	0.1	10	300	400	2 µA	8 mA/7 mA	7 mA/6 mA	0.8 mA	
DG170B	250/850	-5/-10	-100/-200		10	200	-0.4	0.1	10	300	400	2.4 µA	10 mA/9 mA	9 mA/8 mA	1 mA	
DG170C	250/850	-5/-10			10	200	-0.4	0.1	10	-	-	2.4 µA	10 mA/9 mA	9 mA/8 mA	1 mA	
DG172A	150/450	-1/-4		-1000/-4000	4	4000	-0.5	0.1	10	300	750	All channels on/all off				3.6 mA/4.5 mA
DG172B	150/500	-5/-10	-100/-300		10	300	-1	0.1	10	500	1000	All channels on/off				3.6 mA/4.5 mA
DG172C	200/600	-10			10		-1 @ 25°C	0.1		-	-	All channels on/off				3.6 mA/4.5 mA
DG173A	150/450	-1/-2		-1000/-2000	2	2000	-1	0.1	10	200	700	All channels on/off				1 mA/2 mA
DG173B	150/500	-5/-10	-100/-300		10	300	-1	0.1	10	200	800	All channels on/off				1 mA/2 mA
DG175A	75/200	-1		-1000	1	1000	-1	0.1	10	200	500	One channel on/all off				1 mA/2 mA
DG175B	75/250	-5	-100		5	100	-1	0.1	10	200	500	One channel on/off				1 mA/2 mA

†DGM122-($V_{INH(MAX)}$). ($I_{IN} = 100 \mu A, @ 25^\circ C$) 1.3V
 DGM122A- $V_{INH(MAX)}$ ($I_{IN} = 100 \mu A, @ T_{MAX}$) 1V

DGM111, DGM122, DG170-175 $V_A (V_1 = 15, V_2 = -15)$ +15/-5V $V_A (V_1 = 10, V_2 = -20)$ +10/-10V DGM111 $V_{INH(MIN)}$ 4.6V $V_{INL(MAX)}$ 0.5V	DGM122 I_{INH} 100 µA $V_{INL(MAX)}$ 0.4V DG170-175 $V_{INH(MIN)}$ 2.0V $V_{INL(MAX)}$ 0.8V
--	--

DGM111

Flat Package

Dual-In-Line Package

14-PIN DIP

SWITCH STATES ARE FOR LOGIC "1" INPUTS

DGM122

Flat Package

Dual-In-Line Package

14-PIN DIP

SWITCH STATES ARE FOR LOGIC "0" INPUT (POSITIVE LOGIC)

DG170

Dual-In-Line Package

16-PIN DIP
16-PIN PLASTIC

SWITCH STATES ARE FOR LOGIC "1" INPUTS

DG172

Flat Package

Dual-In-Line Package

14-PIN DIP
14-PIN PLASTIC DIP

SWITCH STATES ARE FOR LOGIC "1" INPUTS

DG173

Flat Package

Dual-In-Line Package

14-PIN DIP

SWITCH STATES ARE FOR LOGIC "1" INPUTS

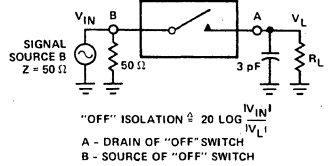
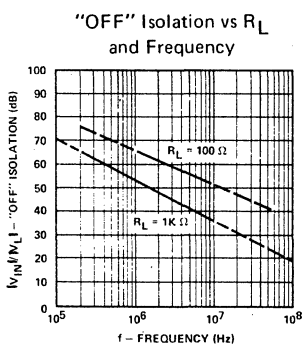
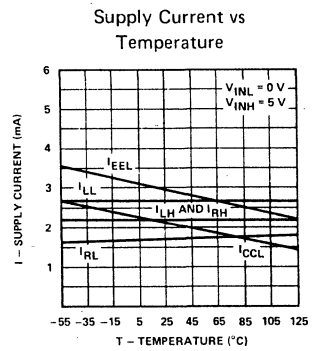
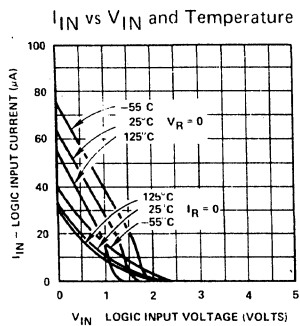
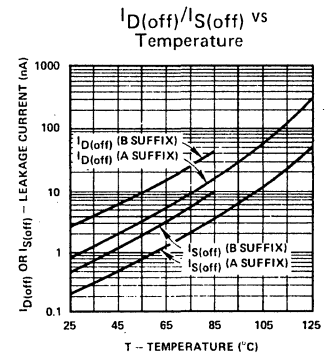
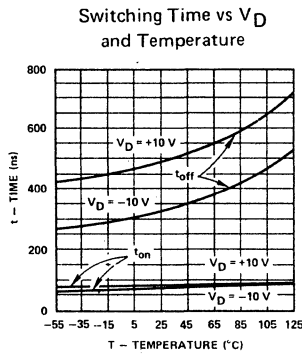
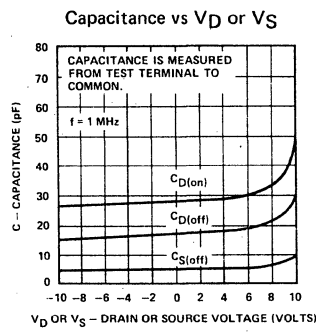
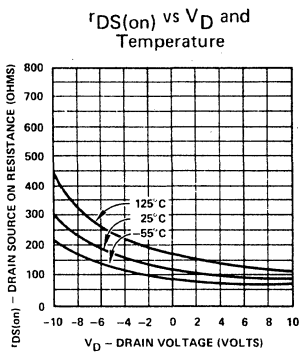
DG175

Metal Can Package

SWITCH STATES ARE FOR LOGIC "1" INPUTS

TYPICAL CHARACTERISTICS

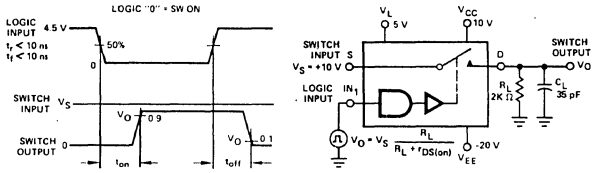
Curves for the other devices in this grouping are similar to those of the DG172



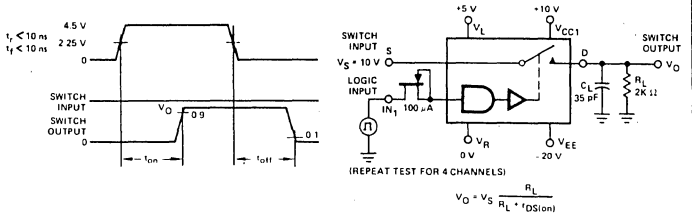
SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for $V_S = \text{constant}$ with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

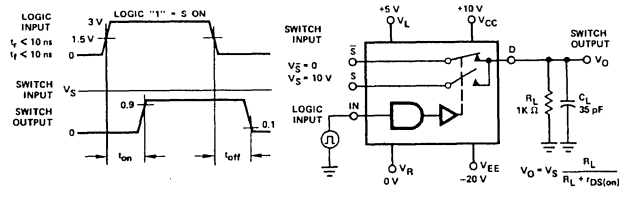
DGM111



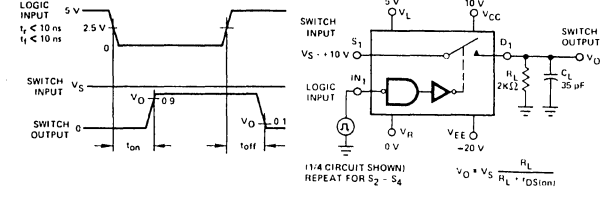
DGM122



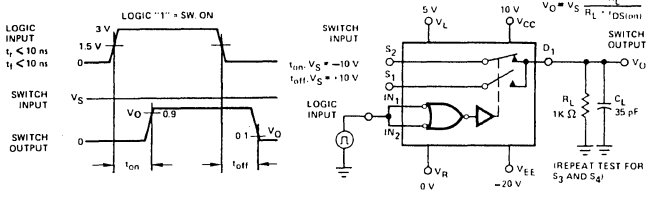
DG170



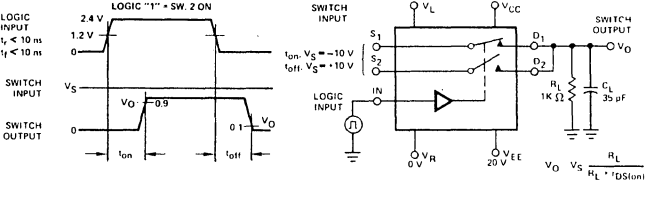
DG172



DG173



DG175



APPLICATION HINTS*

V_{CC} Positive Supply Voltage (V)	V_{EE} Negative Supply Voltage (V)	V_S Analog Signal Range (V)
10**	-20	-10 to +10
15	-15	-5 to +15
20	-10	0 to +20
+5	-15	-5 to +5
+5	-25	-15 to +5

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
**Electrical Characteristics are based on $V_{CC} = +10\text{V}$, $V_{EE} = -20\text{V}$ only.

DG200 DUAL SPST CMOS ANALOG TRANSMISSION GATE
DG201 DUAL SPST CMOS ANALOG TRANSMISSION GATE

Military (A Suffix) -55 to +125°C
 Industrial (B Suffix) -20 to +85°C
 Commercial (C Suffix) 0 to +70°C

features

- Impossible to Latch Up Under Any Circumstances
- ±15V Analog Signal Range with ±15V Supplies
- $r_{DS} < 100 \Omega$ Over Full Temperature and Signal Range - DG200
 $r_{DS} < 250 \Omega$ Over Full Temperature and Signal Range - DG201
- Break-Before-Make Switching Action
- TTL, DTL, and CMOS Direct Control Interface Over the Military Temperature Range Without the Need for Interface Components
- All Terminals Are Protected Against Static Electricity

ABSOLUTE MAXIMUM RATINGS

V_{IN} and V_{REF} to Ground	-0.3V, V_1
V_S or V_D to V_1	0, -32V
V_S or V_D to V_2	0, 32V
V_1 to Ground	16V
V_2 to Ground	-16V
Current, Any Terminal Except S or D	30 mA
Continuous Current, S or D	20 mA
Peak Current, S or D (pulsed at 1 msec, 10% duty cycle max) DG201	70 mA
Peak Current, S or D (pulsed at 1 msec, 10% duty cycle max) DG200	100 mA
Power Dissipation*	
Metal Can**	450 mW
Flat Package***	750 mW
14 Pin DIP****	825 mW
14 Pin Plastic DIP†	470 mW
16 Pin DIP****	825 mW
16 Pin Plastic DIP†	470 mW

*Device mounted with all leads welded or soldered to PC board.
 Derate 6 mW/°C above 75°C *Derate 11 mW/°C above 75°C
 ****Derate 10 mW/°C above 75°C †Derate 6.5 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

Test conditions, unless noted:
 $V_1 = 15V, V_2 = -15V, \text{Ground} = 0, V_{REF} = \text{Open}$

MAXIMUM LIMITS

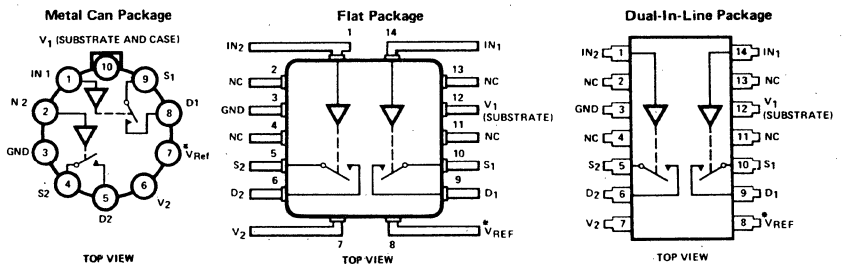
Type (Temp. Suffix)↓	$r_{DS(on)}$ $V_D = -10V$ $I_S = -1 \text{ mA}$		$I_{S(off)}/I_{D(off)}$				$I_{D(on)}$ $V_D = V_S = -15V$ $V_D = V_S = 15V$		$I_{INH(MAX)}$ $V_{IN} = 0$		$I_{INH(MIN)}$ $V_{IN} = 2.4V$ $V_{IN} = 15V$		t_{ON} See Test Circuit	t_{OFF} See Test Circuit	I_1/I_2 $V_{IN} = 0$	$I_1 \text{ Standby}/I_2 \text{ Standby}$ $V_{IN} = 5$
	Ω @ 25°C	Ω @ T_{MAX}	nA @ 25°C	nA @ T_{MAX}	nA @ 25°C	nA @ T_{MAX}	nA @ 25°C	nA @ T_{MAX}	μA @ 25°C	μA @ T_{MAX}	μA @ 25°C	μA @ T_{MAX}	μs @ 25°C	μs @ 25°C	mA @ 25°C	mA @ 25°C
DG200A DG200B	70 80	100 100	2/-2 5/-5	1000/-1000 500/-500	-2/2 -5/5	-1000/1000 -500/500	-2/2 -5/5	-1000/1000 -500/500	-1 -10	-10 -10	-1/1 -1/1	-10/10 -10/10	1 1	0.5 0.5	Both Channels ON 4/-4 4/-4	Both Channels OFF 2/-2 2/-2
DG201A DG201B DG201C	175 200 200	250 250 250	1/-1 5/-5 5/-5	500/-500 250/-250 250/-250	-1/1 -5/5 -5/5	-500/500 -250/250 -250/250	-1/1 -5/5 -5/5	-500/500 -250/250 -250/250	-1 -1 -1	-10 -10 -10	-1/1 -1/1 -1/1	-10/10 -10/10 -10/10	1 - -	0.5 - -	One Channel ON 4/-4 4/-4	Both Channels OFF 3/-3 3/-3

POWER SUPPLIES - ANALOG RANGE

V_1 Positive Supply Voltage (V)	V_2 Negative Supply Voltage (V)	V_{REF} Reference Pin Connection (V)	V_{IN} Logic Input Voltage $V_{INH} \text{ Min}/V_{INL} \text{ Max}$ (V)	V_S or V_D ** Analog Voltage Range (V)
+15*	-15	Open	2.4/0.8	-15 to +15
+12	-12	1.4V or 470K to V_1	2.4/0.8	-12 to +12
+10	-10	1.4V or 240K to V_1	2.4/0.8	-10 to +10

*Electrical Characteristics chart based on $V_1 = +15V, V_2 = -15V, V_{REF} = \text{Open}$
 **The analog signal should not exceed the actual supply voltages appearing at pins V_1 and V_2 .

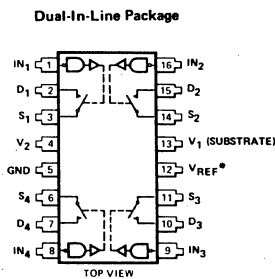
DG200 DUAL SPST



14-PIN DIP/14-PIN PLASTIC DIP

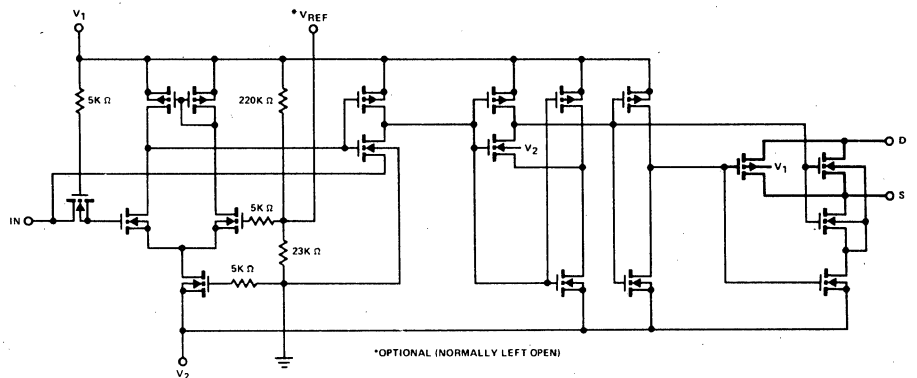
SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

DG201 QUAD SPST



16-PIN DIP/16-PIN PLASTIC DIP
 SWITCH STATES ARE FOR LOGIC "1" INPUT (POS. LOGIC)

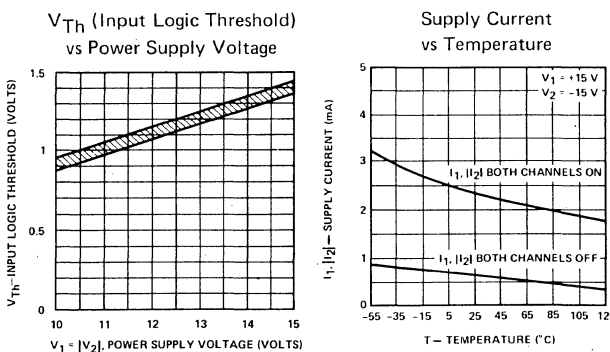
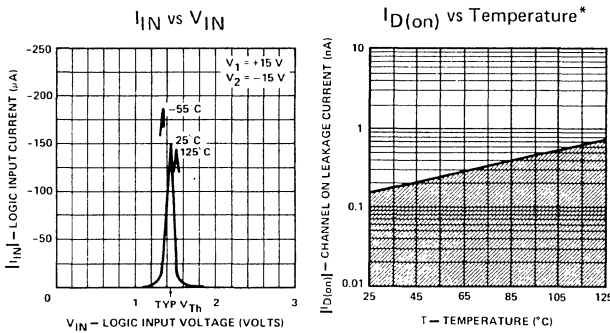
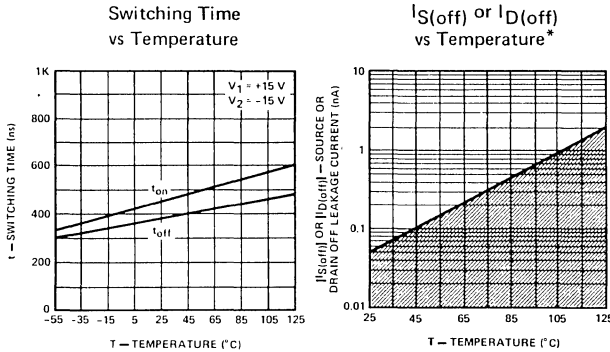
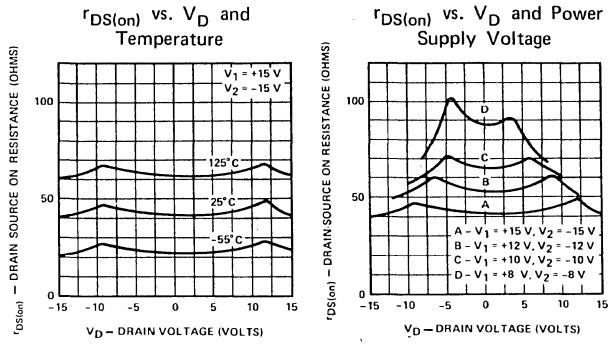
SCHEMATIC DIAGRAM (Typical Channel)



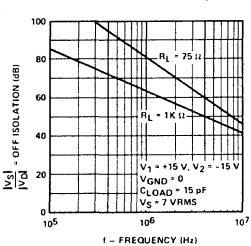
*OPTIONAL (NORMALLY LEFT OPEN)

TYPICAL CHARACTERISTICS

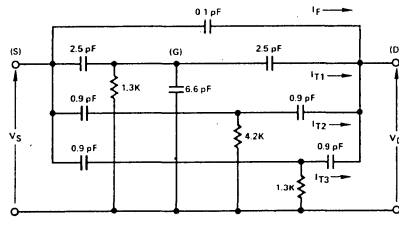
DG200



"OFF" Isolation vs. Frequency

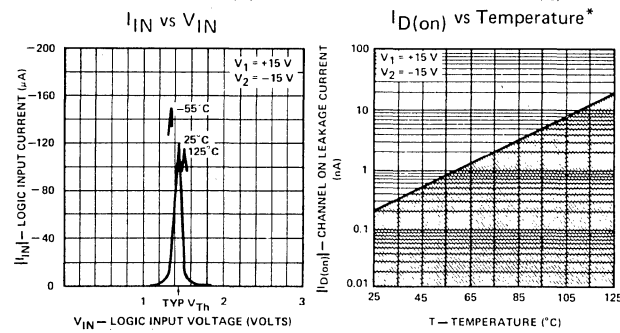
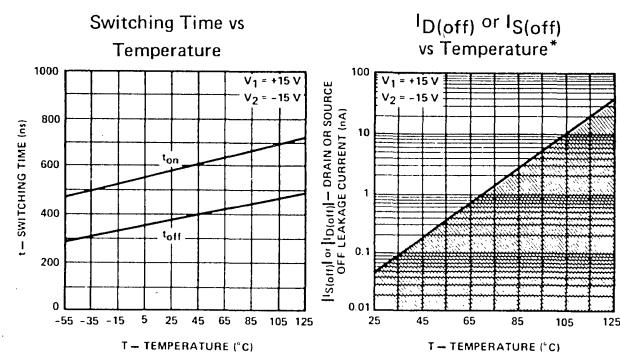
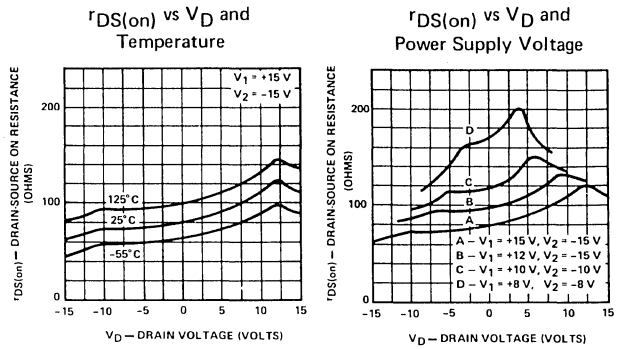


"OFF" Isolation Equivalent Circuit

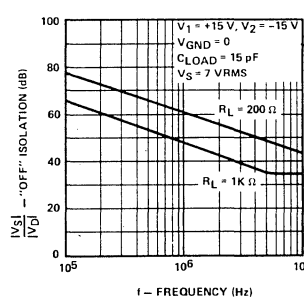


*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

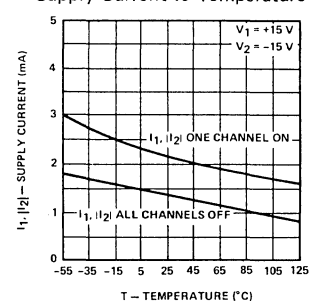
DG201



OFF Isolation vs Frequency

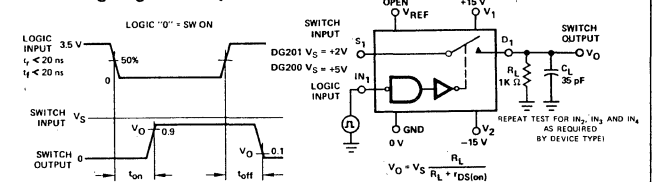


Supply Current vs Temperature



SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



INTERFACE Siliconix

DG506 16-CHANNEL ANALOG MULTIPLEXER
 DG507 8-CHANNEL DIFFERENTIAL ANALOG MULTIPLEXER
 DG508 8-CHANNEL ANALOG MULTIPLEXER
 DG509 4-CHANNEL DIFFERENTIAL ANALOG MULTIPLEXER

Military (A Suffix) -55 to +125°C
 Industrial (B Suffix) -20 to +85°C
 Commercial (C Suffix) 0 to +70°C

ABSOLUTE MAXIMUM RATINGS

$V_{IN}(A, EN)$ to Ground	-0.3V, V_1
V_S or V_D to V_1	0, -32V
V_S or V_D to V_2	0, 32V
V_1 to Ground	16V
V_2 to Ground	-16V
Current (Any Terminal, Except S or D)	30 mA
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 msec, 10% Duty Cycle Max)	40 mA

FEATURES

- Impossible to Latch Up Under Any Circumstances
- ±15V Analog Signal Range with ±15V Supplies
- $r_{ON} < 500$ Ohms Over Full Temperature and Signal Range
- Break-Before-Make Switching Action
- TTL, DTL, and CMOS Direct Control Interface Over Military Temperature Range Without Need For Interface Components
- Binary Inputs Select Channels
- Input (EN) Allows Output Line to be Common to Several Other Units
- 36 mW Typical Standby Power
- All Terminals are Protected Against Static Electricity

Power Dissipation*

16 Pin DIP**	825 mW
16 Pin Plastic DIP***	470 mW
28 Pin DIP†	1200 mW

* All leads soldered or welded to PC board.

** Derate 11 mW/°C above 75°C.

*** Derate 6.3 mW/°C above 25°C.

† Derate 10 mW/°C above 70°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

Test conditions, unless noted:
 $V_1 = 15V, V_2 = -15V, \text{Ground} = 0, V_{REF} = \text{Open}$

MAXIMUM LIMITS

Type (Temp. Suffix)↓	$r_{DS(on)}$ $V_D = -10$ $I_S = -200 \mu A$		$I_{S(off)}/I_{D(off)}$ $V_D = \mp 10, V_S = \pm 10$ $+ E_N = 0$		$I_{D(on)}$ $V_S = V_D = \pm 10V$		$t_{on}(EN)$ See Fig. 2	$t_{off}(EN)$ See Fig. 2	t_{TRANS} Sw. time of Mux.	I_1 or $-I_2$ All $V_A = 0$ $V_{EN} = 5/0V$
	Ω @ 25°C	Ω @ TMAX	nA @ 25°C	nA @ TMAX	nA @ 25°C	nA @ TMAX	μs @ 25°C	μs @ 25°C	μs @ 25°C	mA @ 25°C
DG506A	400	500	±1/±10	±50/±500	±10	±500	1.5	1	1	10/2.5
DG506B,C	450	550	±5/±20	±50/±500	±20	±500	—	—	—	10/2.5
DG507A	400	500	±1/±5	±50/±250	±5	±250	1.5	1	1	10/2.5
DG507B,C	450	550	±5/±10	±50/±250	±10	±250	—	—	—	10/2.5
DG508A	400	500	±1/±10	±50/±500	±10	±500	1.5	1	1	8/2.4
DG508B,C	450	550	±5/±20	±50/±500	±20	±500	—	—	—	8/2.8
DG509A	400	500	±1/±10	±50/±250	±10	±250	1.5	1	1	8/2.4
DG509B,C	450	550	±5/±20	±50/±250	±20	±250	—	—	—	8/2.8

DG506-509

I_{AH} ($V_{ADD} = 2.4, @ 25^\circ C$)	-10 μA
I_{AH} ($V_{ADD} = 15, @ 25^\circ C$)	10 μA
I_{AH} ($V_{ADD} = 2.4, @ T_{MAX}$)	-30 μA
I_{AH} ($V_{ADD} = 15, @ T_{MAX}$)	30 μA

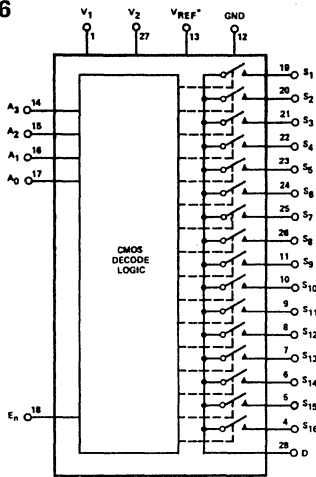
I_{AL} ($V_{EN} = 2.4, \text{All } V_{ADD} = 0 @ 25^\circ C$)	-10
I_{AL} ($V_{EN} = 2.4, \text{All } V_{ADD} = 0 @ T_{MAX}$)	-30
I_{EN} ($V_{EN} = 0, \text{All } V_{ADD} = 0 @ 25^\circ C$)	-10
I_{EN} ($V_{EN} = 0, \text{All } V_{ADD} = 0, @ T_{MAX}$)	-30

FUNCTIONAL DIAGRAM

PIN CONFIGURATIONS

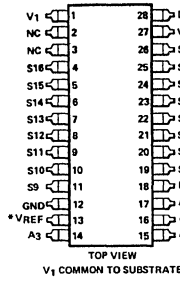
DECODE TRUTH TABLE

DG506



*Optional (normally left open)

Dual In-Line Package

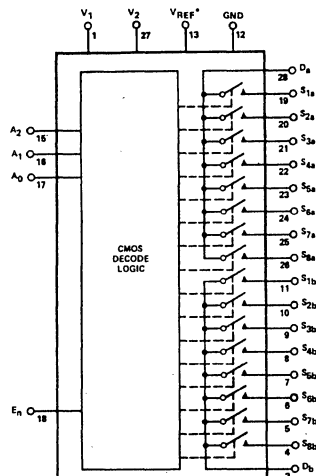


TOP VIEW
V₁ COMMON TO SUBSTRATE

A ₃	A ₂	A ₁	A ₀	E _n	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

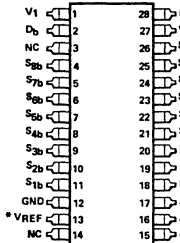
Logic "1" = V_{AH} ≥ 2.4 V
Logic "0" = V_{AL} ≤ 0.8 V

DG507



*OPTIONAL (NORMALLY LEFT OPEN)

Dual-In-Line Package

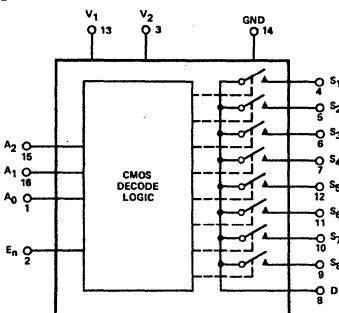


TOP VIEW
V₁ COMMON TO SUBSTRATE

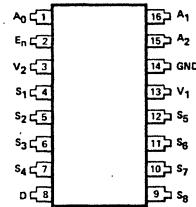
A ₂	A ₁	A ₀	E _n	ON SWITCH PAIR
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "1" = V_{AH} ≥ 2.4 V
Logic "0" = V_{AL} ≤ 0.8 V

DG508



Dual-In-Line Package

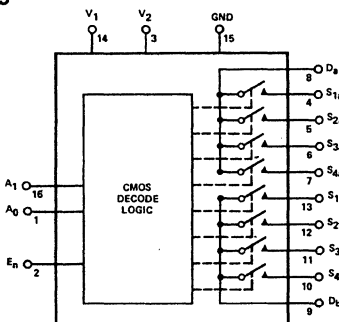


TOP VIEW
V₁ COMMON TO SUBSTRATE

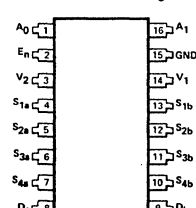
A ₂	A ₁	A ₀	E _n	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "1" = V_{AH} ≥ 2.4 V
Logic "0" = V_{AL} ≤ 0.8 V

DG509



Dual-In-Line Package



TOP VIEW
V₁ COMMON TO SUBSTRATE

A ₁	A ₀	E _n	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

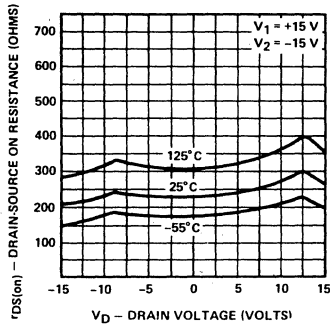
Logic "1" = V_{AH} > 2.4 V
Logic "0" = V_{AL} < 0.8 V

INTERFACE

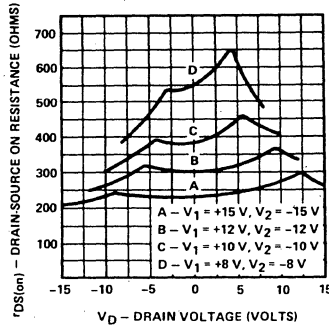
Siliconix

TYPICAL CHARACTERISTICS

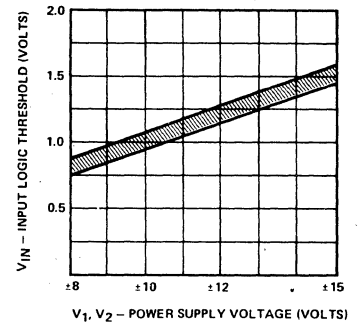
r_{DS(on)} vs V_D and Temperature



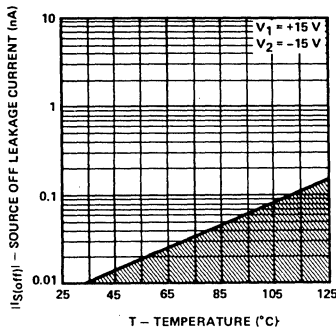
r_{DS(on)} vs V_D and Power Supply Voltage



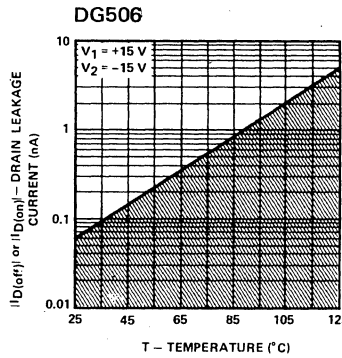
Logic Threshold vs Power Supply Voltage



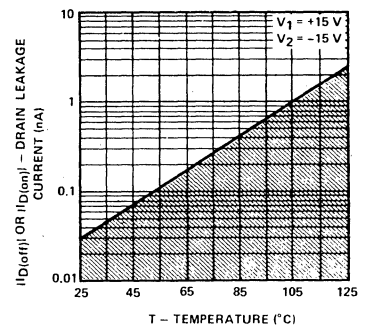
I_{S(off)} vs Temperature*



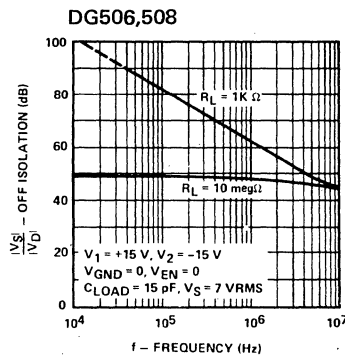
I_{D(off)} and I_{D(on)} vs Temperature*



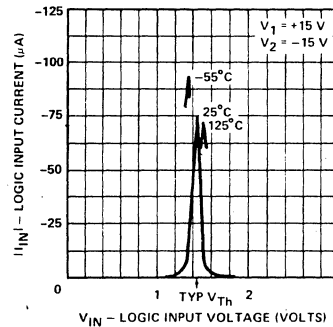
DG507,508,509



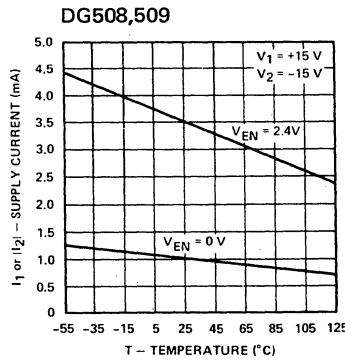
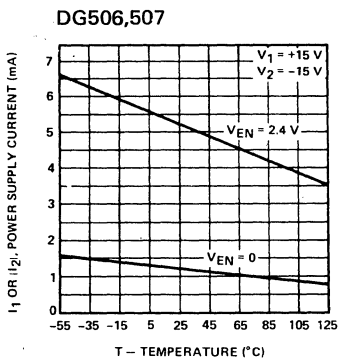
OFF Isolation vs Frequency



I_A vs V_A (Terminals A₀, A₁, A₂, A₃, EN)



Power Supply Current vs Temperature

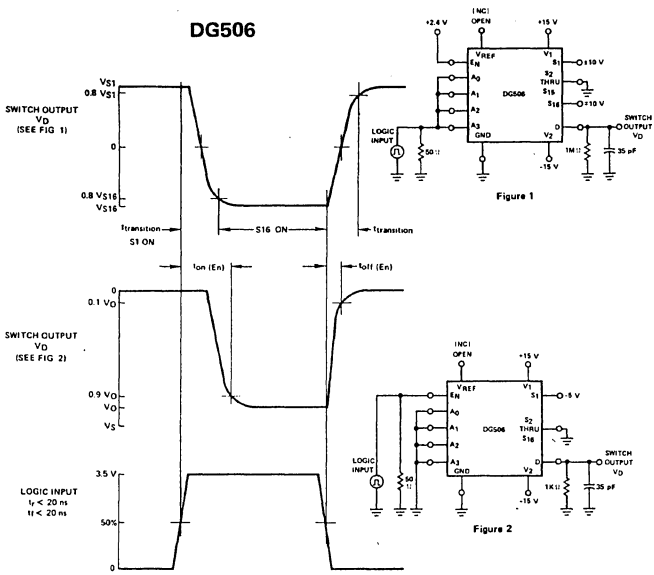


*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

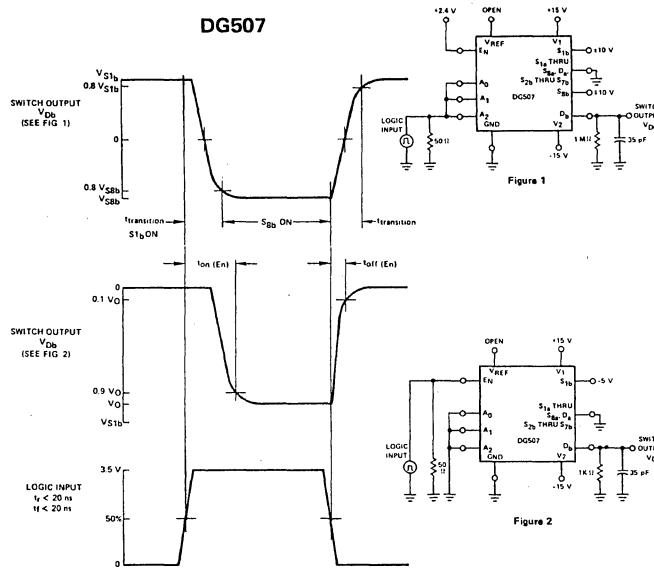
INTERFACE

Siliconix

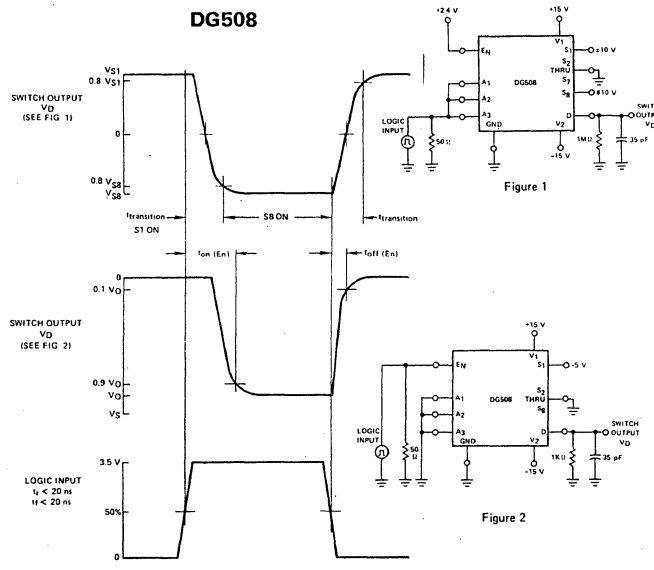
DG506



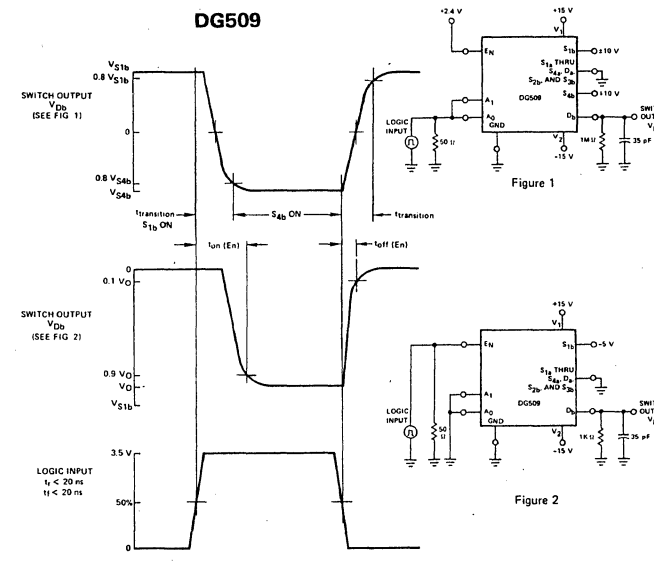
DG507



DG508



DG509



INTERFACE

Siliconix

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INTRODUCTION TO LINEAR

The Master Selection Guide provides sufficient information to make initial product selections, to lead you to a group of device numbers and manufacturers' names. It enables you to find the products which are most appropriate to fulfill your major requirements and then provides data for many of the more important products.

All devices that appear in this section, both in the initial selection guide and in the data pages, are included in the Part Number and Product Indexes. These index listings lead to the page and the line on that page where each device appears.

In the Linear section over 925 operational amplifiers are covered. Since there are so many devices, the operational amplifier entries have been given special consideration. Separate lists are provided for those which have High Speed, High Voltage capability, Wide Bandwidth, etc. Under General Purpose, three amplifier types are listed; these are the ones that the high volume manufacturers indicate are the most widely used; however, quad amplifiers should also be considered when appropriate. If you have located a device in a specialized category, you can review its characteristics by finding it in the Part Number or Product Indexes and looking it up in the Operational Amplifier Characteristics Section and in the Data Section.

Following the special lists, the "Operational Amplifier-Characteristics" listings, categorize amplifiers by input parameters. They are arranged in order of increasing bias current, offset voltage, offset current and then voltage drift (with bias current first, the FET input devices tend to be at the beginning of the list). The other parameters listed do not affect the sequence in which the devices are presented. The column labeled "Comp" indicates the number of external components normally used for compensation; for example, "0" means no compensation is required.

Consumer circuits such as audio amplifiers, AM, FM, and TV circuits are not covered by model number but the manufacturers of these functions are listed under the heading Industrial/Consumer Circuits. Linear devices and unusual circuits which do not fit elsewhere are listed under the heading "Other Linear Devices."

Category	Page
Amplifiers, Special Purpose	568
Arrays	
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Special	569
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Raytheon Semiconductor	647
RCA	661
Signetics	668

The manufacturers listed above are providing detailed information on their latest and most significant products. They have made this investment to help you. Some chose not to.

If you want to see more data in future editions, tell the manufacturers through their salesmen and distributors.

LINEAR—Amplifiers

Master Selection Guide

LINEAR

Function	Device	Source	Line	Function	Device	Source	Line
Special Purpose				Special Purpose (cont)			
AC Amplifier, Quad, Single Supply	CA3048	† RCA		Preamplifier, Temperature Controlled	μA727C μA727M	Fairchild † Fairchild	
Current Amplifier (unity gain, 100 ma Output)	LH0002 LH0002C	† National National		Preamplifier with automatic level control, for tape recorders	TDA1054 TA7055	SGS Toshiba	
Current Amplifier (unity gain, 200 ma output)	3553	† Burr-Brown		Programmable Channel Op Amp (one of 4 input stages can be connected to single output)	1454C 1454M HA-2400 HA-2404 HA-2405	DDC † DDC † Harris Harris Harris	
Current Amplifier (unity gain, 300 ma output)	MC1438 MC1538	Motorola † Motorola		Single-ended Input/Output Amplifier, Triple	CA3035	RCA	60
Current Amplifier (unity gain, 600 ma output)	1016C 1016M HA-2630 HA-2635	DDC † DDC † Harris Harris	10	Two Wire Transmitter (Sends current signal over same two lines from which it is powered)	LH0045 LH0045C	† National National	
Differential Input/Differential Output Amplifier	μA730C μA730M ITT730-1 ITT730-5	Fairchild † Fairchild ITT ITT		Wideband Amplifier with low level video detection (7 to 150 MHz)	SL521A SL521B SL521C SL613C	Plessey Plessey Plessey Plessey	
Instrumentation, (Differential Input, Independent Gain Adjustment)	AD520J AD520K AD520S AD521J AD521K AD521S 3660J 3660K 3660S LH0036 LH0036C LH0037 LH0037C	AD AD † AD AD AD † AD Burr-Brown Burr-Brown † Burr-Brown † National National † National National	20	Wideband Amplifier, logarithmic Limiting (4 to 85 MHz)	SL530C	Plessey	
Instrumentation, (Differential FET Input, Independent Gain Adjustment)	3670J 3670K 3670S	Burr-Brown Burr-Brown † Burr-Brown	30	Wideband Amplifier, Triple	CA3035	† RCA	
Log/Antilog Amplifiers (Antilog)	1452 8049C	DDC Intersil					
Log/Antilog Amplifiers, (Log)	4127 1451 8048C	Burr-Brown DDC Intersil					
Microphone/Headphone Amplifier	SL630C	Plessey					
Operational Transconductance Amplifier	CA3060 CA3060 CA3060A CA3060B CA3080 see page 666 CA3080A see page 666	RCA † RCA † RCA † RCA RCA † RCA † RCA	40				
Power Amplifier/Switch (equivalent to an operational amplifier with uncommitted Darlington power output transistor), Programmable Gain	CA3094 CA3094A CA3094B	† RCA † RCA † RCA					
Preamplifier J.F.E.T. (to precede op amps and comparators)	HA-2000 HA-2005	† Harris Harris					
Preamplifier, Precision (to precede operational amplifiers)	LM121 LM221 LM321	† National National National	50				

† Military Temperature Range (–55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

Linear—Arrays

Table with columns: Function, Device, Source, Line. It is divided into three main sections: Transistor Arrays, Transistor Arrays (cont), and Transistor Arrays (cont). Each section lists various transistor types (e.g., Dual Transistors, Darlington, Differential Amplifiers) with their respective device numbers and manufacturers. Some entries include line numbers (e.g., 10, 20, 30, 40, 50, 60, 70, 80, 90, 100, 110, 120, 130, 140, 150).

† Military Temperature Range (– 55°C to 125°C)

LINEAR—Comparators

Offset Voltage mv (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage	Device	Source
Comparators—Single									
0.8	50nA	3nA	230	11	200K		+5 to ±18	CMP-02 CMP-02E	† PMI PMI
	600nA	25nA	150	11	200K*		+5 to ±18	CMP-01 CMP-01E	† PMI PMI
1.0	15µA	1µA	60	5	1400		-6,12	RM710A	Raytheon
2.0	10µA	1µA	6.5	6	NA		-5,2,6	685L 685M	AMD † AMD
			12	6	NA	5	-6,5	686M	† AMD
2.0	20µA	3µA	40	5	40K*	10	-3 to -12,12	LM106 LM206 LM106 LM206 LM106 LM206 SN52106	† AMD AMD † National National † Raytheon Raytheon † TI
					1250	1	-6,12	µA710M MC1710 LM710 µA710 SG710 710B SFC2710	† Fairchild † Motorola † National † Signetics † Silicon G † Teledyne S † NPC
			60	5	1250	1	-6,12	RM710	† Raytheon
	75µA	3µA	80	5	12.5K		-6,12	SN52510 SN52810	† TI † TI
2.8	100nA	15nA	230	11	100K		±5 to ±10	CMP-02C	PMI
	900nA	80nA	150	11	100K		+5 to ±18	CMP-01C	PMI
3.0	5µA	2µA*	20	5	3K*	2	5, (-6,5 to ±15)	LM161 LM261	† National National
			12	6	NA	5	-6,5	686C	AMD
	100nA	10nA	200	10	35K		±5 to ±18	µA734M	† Fairchild
165*			30	200K*	5	5,0 to ±15	SN52111	† TI	
			200*	30	200K*	5	5,0 to ±15	AD111 AD211 µA111M HA-2111 HA-2211 111 211 MLM111 MLM211 LM111 LM211 SFC2111 SFC2211 CA111G CA211G LM111 LM211 LM111 LM211 SG111	† AD AD † Fairchild † Harris Harris † Intersil Intersil † Motorola Motorola † National National † NPC NPC † RCA see page 661 RCA see page 661 † Raytheon Raytheon † Signetics Signetics † Silicon G (continued)

† Military Temperature Range (-55°C to 125°C) * — Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR—Comparators (cont)

Offset Voltage mv (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage	Device	Source
Comparators—Single (cont)									
3.0 (continued)	100nA	10nA	200*	30	200K*	5	5,0 to ±15	SG211 LM111 LM211	Silicon G † Teledyne S Teledyne S
			250	30	200K*	5	5,0 to ±15	LM111 LM211	† AMD AMD
			20nA	250*	15	15K	5	5 to 15, ±5 to ±15	8001M
3.5	20µA	5µA	80	5	10K		-6,12	SN72510 SN72810	TI TI
4.0	2µA	0.5µA	26	5	5K*		5,(-6,5 to ±10)	SE527	† Signetics
	12µA	3µA	22	5	5K*		5,(-6,5 to ±10)	SE529	† Signetics
	50pA	25pA	200*	30	200K*	5	5,0 to ±15	LF111 LF211	† National National
5.0	10µA*	2µA*	20	5	3K*	2	(-6,5 to ±15)	LM361	National
	20µA	3µA	14*	5	3K*	4	±5	LM160 LM260 LM360	† National National National
	25µA	5µA	40	5	40K*	10	-3 to -12,12	LM306 LM306 SN72306	National Raytheon TI
			40K*	5	40*	10	-3 to -12,12	LM306	AMD
					1000	1	-6,12	µA710C MC1710C LM710C RC710 SG710 µA710 710C	Fairchild Motorola National Raytheon † Silicon G † Signetics Teledyne S
	35µA	5µA	48	5	NA	10	±5	NE526 SE526	Signetics † Signetics
	75µA	10µA	40*	5	750		-6,12	SN52710	† TI
	100nA	25nA	200*	10	35K		±5 to ±10	µA734C	Fairchild
	250nA	50nA	250*	15	15K		5 to 15, ±5 to ±15	8001C	Intersil
6.0	2µA	0.75µA	26	5	5K*		5,(-6,5 to ±10)	NE527	Signetics
	20µA	5µA	22	5	5K*		5(-6,5 to ±10)	NE529	Signetics
	60µA	7.5µA	16*	5	5K*	2	±4.5 to ±6.5	µA760M µA760C	† Fairchild Fairchild
	250nA	100nA	250	10	15K		±6 to ±18	AD351J AD351K AD351S	AD AD † AD
7.5	100µA	15µA	40*	5	700		-6,12	SN72710	TI
	250nA	50nA	165*	30	200K*	5	5,0 to ±15	SN72311	TI
			200*	30	200K*	5	5,0 to ±15	AD311 µA311C HA-2311 311 MLM311 LM311 SFC2311 CA311G see page 661 LM311 LM311 (continued)	AD Fairchild Harris Intersil Motorola National NPC RCA Raytheon Signetics

† Military Temperature Range (-55°C to 125°C) * — Typical Values

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LINEAR—Comparators (cont)

Offset Voltage mv (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage	Device	Source
Comparators—Single (cont)									
7.5 (continued)	250nA	50nA	200*	30	200K*	5	5.0 to ±15	SG311 LM311	Silicon G Teledyne S
			250	30	200K*	5	5.0 to ±15	LM311	AMD
10.0	150pA	75pA	200*	30	200K*	5	5.0 to ±15	LF311	National
Comparators—Dual									
1.5	15µA	1µA	40	5	1400	1	-6,12	RM711A	† Raytheon
2.0	10µA	1µA	8	6			-5,2,5	687AM	† AMD
			10	6			-5,2,5	687M	† AMD
	15µA	3µA	80	5	12.5K		-6,12	SN52514 SN52820	† TI † TI
3.0	10µA	1µA	30*	5	1250	1	-6,12	LM1514	† National
			40	5	40K*	10	-3 to -12,12	SN52506	† TI
			40*	5	1250		-6,12	MC1514 RM1514	† Motorola † Raytheon
3.0	100nA	10nA	8	6			-5,2,5	687AL	AMD
			10	6			-5,2,5	687L	AMD
	100nA	10nA	200*	30	200K*	5	5.0 to ±15	LH2111 LH2211 LH2111 LH2211	† National National † Signetics Signetics
			250	30	200K*		5.0 to ±15	1500M 1500L	† AMD AMD
3.5	20µA	3µA	80	5	12.5K		-6,12	SN52811	† TI
		5µA	80	5	10K		-6,12	SN72514 SN72820	TI TI
		75µA	10µA	40*	5	700	1	-6,12	MC1711
					750	1	-6,12	µA711M LM711 RM711 µA711 711B	† Fairchild † National † Raytheon † Signetics † Teledyne S
			60	5	750	1	-6,12	SG711	Silicon G
			80	5	750	1	-6,12	SN52711	† TI
4.0	500nA	75nA	80*	5	10K	2	5.0 to ±15	LM119 LM219 LM119 LM219	† National National † Signetics Signetics
5.0	25µA	5µA	28*	5	40*	10	-3 to -12,12	SN72506	TI
			30*	5	1000	1	-6,12	LM1414	National
			40*	5	1000		-6,12	MC1414 RC1414	Motorola Raytheon
	30µA	5µA	33*	5	10K		-6,12	SN75811	TI
	100µA	15µA	40*	5	700	1	-6,12	µA711C MC1711C SFC2711 LM711C RC711 µA711C SG711C SN72711 (continued)	Fairchild Motorola NPC National Raytheon Signetics Silicon G TI

† Military Temperature Range (-55°C to 125°C) * — Typical Values

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LINEAR—Comparators (cont)

Offset Voltage mv (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage	Device	Source		
Comparators—Dual (cont)											
5.0 (continued)	100µA	15µA	40*	5	700	1	-6,12	711C	Teledyne S		
			65*	5	700	1	-6,12	HA17711	Hitachi		
7.5	20µA	5µA	18	6	5K*	10	±5	NE521	Signetics		
			25	6	5K*	10	±5	NE522	Signetics		
	100µA	15µA	40*	5	700		-6,12	SN72720	TI		
			250nA	50nA	200*	30	200K*	5	5,0 to ±15	LH2311	National
					250	30	200K*		5,0 to ±15	1500C	AMD
8.0	1µA	0.2µA	80*	5	8K	2	5,0 to ±15	LM319 LM319	National Signetics		
10.0	2µA		150	10		10	5,±12	L132	Siliconix		
Comparators—Quad											
2.0*	20µA	1µA*	55	5	1.2K*	10	±5	MC3430 MC3431	Motorola Motorola		
			65	5	1.2K*	10	±5	MC3432 MC3433	Motorola Motorola		
2.0	100nA	25nA	1300*	36	50K	2	2 to 36/±1 to ±18	LM139A	† National		
						2	2 to 36/±1 to ±18	CA139AG LM139A	† RCA † Teledyne S		
	250nA	50nA			50K	2	2 to 36/±1 to ±18	CA239AG CA339AG	RCA RCA		
						2	2 to 36/±1 to ±18	LM239A LM339A LM239A LM339A	National National Teledyne S Teledyne S		
5.0	100nA	25nA	1300*	36	200K*	2	2 to 36/±1 to ±18	µA139M LM139 LM139	† Fairchild † Raytheon † National		
						2	2 to 36/±1 to ±18	CA139G LM139 LM139 SN52139	† RCA † Signetics † Teledyne S † TI		
	250nA	50nA			50K	2	2 to 36/±1 to ±18	µA339C LM239 LM339 LM239 LM339	Fairchild National National Raytheon Raytheon		
						2	2 to 36/±1 to ±18	CA239G CA339G LM239 LM339 LM239 LM339 SN72339	RCA RCA Signetics Signetics Teledyne S Teledyne S TI		
7.0	250nA	50nA	1300*	36	50K	2	2 to 36/±1 to ±18	LM2901 LM2901 LM2901 (continued)	National Raytheon Teledyne S		

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† Military Temperature Range (-55°C to 125°C) * — Typical Values

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LINEAR—Comparators (cont)

Offset Voltage mv (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage	Device	Source
Comparators—Quad (cont)									
7.0 (continued)	250nA	50nA	1300*	36	50K	2	2 to 36/±1 to ±18	LM2901	TI
9.0	300nA	70nA	1300*	36			2 to 36/±1 to ±18	μA775C	Fairchild
20	500nA	3nA*	2000*	V _{CC}	2K	1	2 to 28	MC3302 μA3302C RC3302 3302 3302	Motorola Fairchild Raytheon Teledyne S TI
		100nA	1300*	V _{CC}	2K	2	5 to ±15	LM3302	National

Special purpose comparators (Alarm Circuits; Comparators, Programmable; Level Detectors; Voltage Sensors, etc.) are listed under LINEAR—Other Devices

† Military Temperature Range (–55°C to 125°C) * — Typical Values

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LINEAR—Followers

Bias Current na 25°C	Offset Voltage mv 25°C	Voltage Drift $\mu\text{V}/^\circ\text{C}$	Unity Gain Bandwidth min	Slew Rate v/ μs	Output v @ ma	Supply Range	Comments	Device	Source	
Followers										
0.15	20	25*	100*	1000	9 @ 90	± 5 to ± 20	Fast Follower	LH0033C	National	
0.1	10	25*	100*	1000	9 @ 90	± 5 to ± 20	Fast Follower	LH0033	† National	
0.2	25	300*	200*	2000	10 @ 200	± 5 to ± 20	Very Fast Follower	LH0063	† National	
	50	300*	200*	2000	10 @ 200	± 5 to ± 20	Very Fast Follower	LH0063C	National	
2.0*	50	300*	300*	2000	10 @ 200	± 5 to ± 20	Gain 0.94 into 50 ohm	3553 LH0063C	† Burr-Brown National	
3	4.0	6*	12*	30*	10 @ 1	± 5 to ± 18	Follower, replaces 102	SG210	Silicon G	
			20*	30*	10 @ 1	± 5 to ± 18	Follower, replaces 102	LM210 MLM210 LM210	AMD Motorola National	
							Dual 210 Follower	LH2210	National	
			10*	20*	30*	10 @ 1	± 5 to ± 18	Follower, replaces 102	110 210	† Intersil Intersil
			12*	30*	10 @ 1	± 5 to ± 18	Follower, replaces 102	SG110	† Silicon G	
				20*	30*	10 @ 1	± 5 to ± 18	Follower, replaces 102	LM110 $\mu\text{A}110\text{M}$ MLM110 LM110 SN52110	† AMD † Fairchild † Motorola † National † TI
							Dual 110 Follower	LH2110	† National	
7	7.5	10*	12*	30*	10 @ 1	± 5 to ± 18	Follower, replaces 102	SG310	Silicon G	
			20*	30*	10 @ 1	± 5 to ± 18	Follower, replaces 102	LM310 $\mu\text{A}310\text{C}$ 310 MLM310 LM310	AMD Fairchild Intersil Motorola National	
							Dual 310 Follower	LH2310	National	
10	5.0	6*	8*	10*	10 @ 1	± 15	Follower	SG102	† Silicon G	
			10*	10*	10 @ 1.25	± 12 to ± 18	Follower	LM102	† National	
			—	—	10 @ 1.25	± 15	Follower	$\mu\text{A}102\text{M}$ 102	† Fairchild † Intersil	
15	10.0	15*	8*	10*	10 @ 1	± 15	Follower	SG202	Silicon G	
			10*	10*	10 @ 1.25	± 12 to ± 18	Follower	LM202	National	
			—	—	10 @ 1.25	± 15	Follower	202	Intersil	
30	15.0	20*	8*	10*	10 @ 1	± 15	Follower	SG302	Silicon G	
			10*	10*	10 @ 1.25	± 12 to ± 18	Follower	LM302	National	
			—	—	10 @ 1.25	± 15	Follower	$\mu\text{A}302\text{C}$ 302	Fairchild Intersil	

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Master Selection Guide

LINEAR

Military Temperature Range (−55°C to 125°C) * — Typical Values

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LINEAR—Industrial/Consumer Circuits

Master Selection Guide

LINEAR

Function	Source	Line	Function	Source	Line	Function	Source	Line
Alarm			Automotive IC's (cont)			Electrical		
Intrusion Detectors	Lithic Sys National Signetics		Antiskid (continued)	Signetics SSS Sprague	60	Ground Fault Indicators	Fairchild Interdesign ITT Motorola National Raytheon Signetics	120
Smoke/Fire	Intersil Lithic Sys National Signetics		Ignition	AMI Fairchild Interdesign IMI ITT Motorola National Nippon OKI Raytheon Signetics Sprague	70	Motor Speed Controls	NPC Plessey SGS	
Sound Actuated	Interdesign Lithic Sys					Hearing Aid		
Audio						Amplifiers		
Preamplifiers	Exar Fairchild Hitachi Interdesign ITT Lithic Sys Mitsubishi Motorola National Nippon NPC Panasonic Plessey RCA SGS Signetics Sprague Toshiba	10	Position Sensing	Fairchild IMI National NPC Raytheon Signetics	80		Micro Pwr Panasonic Raytheon	130
Power Amplifiers	Beckman Fairchild Hitachi ITT Lithic Sys Mitsubishi Motorola National Nippon NPC Panasonic Plessey RCA Sanken Sprague Toshiba	30	Seatbelt	Fairchild IMI ITT National OKI Signetics SSS Sprague SW		Hobby		
Quadrasonic Decoders	Hitachi IMI Motorola Nippon Panasonic RCA Signetics Toshiba	50	Tachometer	Fairchild IMI ITT Motorola National NPC OKI Panasonic Raytheon Sanken Signetics SW	90	Model Airplane Controls	Hughes Exar Signetics	
Noise Processors	Signetics		Voltage Regulators	Beckman Fairchild Hitachi ITT Motorola National Nippon NPC OKI Raytheon RCA Signetics	110	Medica		
Automotive IC's			Light Bulb Fault	Raytheon		Pacemakers		
Antiskid	AMI IMI ITT Motorola National Raytheon (continued)		Camera			Micro Pwr		
			Flash Control	National Sprague		Receiver		
			Shutter Control	ITT National Sprague		AM Receivers		
							Fairchild Ferranti Hitachi Lithic Sys Motorola National Nippon Panasonic Plessey RCA SGS Signetics Sprague	140
						CATV Amplifiers		
							Motorola	150
						Communications Receiver		
							Lithic Sys Plessey	
						FM, Detectors		
							Fairchild Hitachi ITT Lithic Sys Motorola National Nippon Panasonic Plessey RCA Signetics Sprague Toshiba	160
						FM, IF/RF		
							Fairchild Hitachi ITT Lithic Sys Motorola National Nippon NPC (continued)	170

† Military Temperature Range (–55°C to 125°C) * — Typical Values

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LINEAR—Industrial/Consumer Circuits (cont)

Function	Source	Line	Function	Source	Line	Function	Source	Line
Receiver (cont)			Receiver (cont)			Transmitter (cont)		
FM, IF/RF (continued)	Panasonic Plessey RCA SGS Signetics Sprague Toshiba		TV, IF	Fairchild Hitachi ITT Mitsubishi Motorola National Nippon NPC Panasonic Plessey RCA SGS Signetics Sprague Toshiba	70	Transceivers	Lithic Sys	120
FM, Multiplex Decoders	Exar Fairchild Hitachi Interdesign Mitsubishi Motorola National Nippon Panasonic RCA Signetics Sprague Toshiba	10	TV, Remote Control	GI Hughes ITT Motorola National RCA Sprague Toshiba	80	Transmitters	Lithic Sys	
FM, Tuning Logic	AMI	20	TV, Sound System	Fairchild Hitachi ITT Motorola National Nippon NPC Panasonic Plessey RCA SGS Signetics Sprague Toshiba	90	Video Recorder		
Pocket Pagers	Micro Pwr		TV, Tuning Logic	AMI Fairchild Hitachi ITT National Plessey	100	VTR Circuits	Panasonic	
Single Sideband	Lithic Sys Plessey		Telephone			Weighing		
TV, AFT	Fairchild Hitachi ITT Motorola National Nippon NPC Panasonic Plessey RCA Sprague Toshiba	30	Baseband Amplifiers/Modulators	Lithic Sys Plessey		Electronic Scale	OKI	
TV, Chroma	Fairchild Hitachi ITT Mitsubishi Motorola National Nippon Panasonic Plessey RCA Sprague Toshiba	40	Cross-point Switches	Motorola Raytheon Signetics	110			
TV, Horizontal & Vertical Circuits	Fairchild Hitachi ITT Mitsubishi Motorola National Nippon NPC Panasonic Plessey RCA SGS Sprague Toshiba	50	Dialler Circuits	Collins GI ITT Motorola Nitron Plessey				
			Speaker Phone	Interdesign				
			Transmitter					
		60	Single Sideband Circuits	Lithic Sys Plessey				

† Military Temperature Range (-55°C to 125°C)

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LINEAR—Operational Amplifiers

Function	Device	Source	Line	Unity Gain Slew Rate (v/μs min)	Device	Source	Unity Gain Slew Rate (v/μs min)	Device	Source		
General Purpose				High Speed				High Speed (cont)			
The 101A series consists of the 101A (-55°C to 125°C), the 201A (-25°C to 85°C) and the 301 (0°C to 70°C). These units require an external compensation capacitor which permits the bandwidth to be optimized for particular applications.				50				400			
LM101A AMD				LM118 †AMD				LH0024 † National			
AD101A AD				LM218 AMD				500			
see page 625				LM318 AMD				1430 Teledyne P			
μA101A Fairchild				AD518J AD				1000			
101A Intersil				see page 624				825 † Beckman			
MLM101A Motorola				AD518K AD							
LM101A National				see page 624							
CA101AG RCA				AD518S †AD							
see page 661				see page 624							
LM101A Raytheon				AD528J AD							
LM101A Signetics				see page 624							
SG101A Silicon G				AD528K AD							
LM101A Siliconix				see page 624							
LM101A Teledyne S				AD528S †AD							
SN52101A TI				see page 624							
The performance of the 741 series is similar to the 101. These units include internal compensation to make the device stable and to eliminate the need for an external capacitor.				1009M †DDC							
741 AMD				HA-2510 †Harris				50			
AD741 AD				LH0062 † National							
see page 625				LH0062C National							
μA741 Fairchild				LM118 † National							
HA17741 Hitachi				LM218 National							
741 Intersil				LM318 National							
ITT741 ITT				SFC2118 †NPC							
MC1741 Motorola				SFC2218 NPC							
LM741 National				SFC2318 NPC							
SFC2741 NPC				LM118 † National				60			
SSS741 PMI				LM218 Raytheon							
CA741G RCA				LM318 Raytheon							
see page 661				SG118 † Silicon G							
RC741 Raytheon				SG218 Silicon G							
SG741 Silicon G				SG318 Silicon G							
μA741 Signetics				141410 Teledyne P							
SN72741 TI											
Dual Amplifiers.				65							
The 1458 (0°C to 70°C) and the 1558 (-55°C to 125°C) offer approximately the same performance as the 741. Compensation is built in.				3550J Burr-Brown							
XR1458 Exar				3550S † Burr-Brown							
1458 Fairchild				80							
MC1458 Motorola				AD509J AD							
LM1458 National				see page 624							
SSS1458 PMI				3507J Burr-Brown				70			
CA1458G RCA				1322 † Teledyne P							
RC1458 Raytheon				132201 Teledyne P							
MC1458 Signetics				100							
SG1458 Silicon G				AD509K AD							
1458 Teledyne S				see page 624							
SN72558 TI				AD509S †AD							
				see page 624							
				3550K Burr-Brown							
				HA-2520 † Harris							
				120							
				AD505J AD							
				AD505K AD							
				AD505S †AD							
				250							
				1010C DDC				80			
				HA-2535 Harris							
				LH0024C National							
				280							
				1010M †DDC							
				HA-2530 †Harris							
				350							
				LH0032 † National							
				LH0032C National							

† Military Temperature Range (-55°C to 125°C)

LINEAR—Operational Amplifiers (cont)

Maximum Supply Voltage	Device	Source	Voltage Drift ($\mu\text{V}/^\circ\text{C}$ Max)	Device	Source	Offset Voltage	Device	Source
High Voltage			Low Drift—Single			Low Offset		
± 30	MC1436C LM343 SG1436C	Motorola National Silicon G	0.4	HA-2904	Harris	0.025	AD510L see page 625 AD510S see page 625	AD † AD
± 34	MC1436 SG1436	Motorola Silicon G	0.5	AD504M see page 625 LH0044A LH0044AC LH0044B OP-05A	AD † National National National PMI		LH0044A LH0044AC OP-07A	† National National PMI
± 35	3580J	Burr-Brown	0.6	1012 SSS725A HA-2900 OP-05E OP-07A SSS725A SSS725E	† DDC † AMD † Harris PMI † PMI † PMI PMI	0.050	AD510K see page 625 HA-2904 LH0044 LH0044B	AD Harris † National National
± 40	3571AM 3572AM AM-464 HA-2640 HA-2645 MC1536 LH0004 LH0004C LM143 LM243 SG1536 1332	† Burr-Brown † Burr-Brown Datel † Harris Harris † Motorola † National National † National National National Silicon G Teledyne P	1.0	AD504S see page 625 3500E 3521L $\mu\text{A}725\text{A}$ $\mu\text{A}725\text{E}$ LH0044 LH0044C LM725A SSS725 SSS725B OP-05 142302	† AD Burr-Brown Burr-Brown † Fairchild Fairchild † National National National National † PMI PMI † PMI Teledyne P	0.060	1012M HA-2900	† DDC † Harris
± 75	3581J	† Burr-Brown	1.0 (Dual Unit)	OP-10 OP-10A OP-10E	† PMI † PMI PMI	0.075	OP-07 OP-07E	† PMI † PMI
± 150	3582J	† Burr-Brown	1.3	OP-07 OP-07E	† PMI PMI	0.080	1012C HA-2905 1340	DDC Harris Teledyne P
± 225 (5v Internal regulator) ZN417	Ferranti		1.5	OP-05C SSS725C	PMI PMI	0.10	SSS725A AD510J see page 625 AM-490-2A SSS725A	† AMD AD Datel † PMI
450 (5v internal regulator) ZN417	Ferranti		1.5 (Dual Unit)	OP-10C	PMI	0.15	OP-05A OP-07C	† PMI PMI
			1.6	OP-07C	PMI	0.25	3521J 3521K 3521L 3521R	Burr-Brown Burr-Brown Burr-Brown † Burr-Brown
			2.0	142301	Teledyne P			

† Military Temperature Range (–55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

LINEAR—Operational Amplifiers (cont)

Function	Device	Source	Supply Voltage	Device	Source	Supply Voltage	Device	Source	
Programmable			Single Supply			Quad (4 units per package) (cont)			
Adjustable Current/Performance Single (1 unit per package)	1003C	DDC	5 to 16	CA3130	† RCA	3 to 30 (continued)	LM124	† TI	
	1003M	† DDC		see page 664				LM224	TI
	HA-2720	† Harris		CA3130A	† RCA			LM324	TI
	HA-2725	Harris	see page 664					90	
	4250	† Intersil	CA3130B	† RCA		3 to 32	MLM2902 LM2902 RC4137 RM4137 RV4137 2902	Motorola Raytheon Raytheon † Raytheon Raytheon Teledyne S	
	4250C	Intersil	see page 664						
	8021C	Intersil							
	8021M	† Intersil							
	MC1776	† Motorola							
	MC1776C	Motorola		to 24	CA3094	† RCA			
	MC3776	Motorola		to 36	CA3094A	† RCA			
	LM4250	† National		to 44	CA3094B	† RCA			
	LM4250C	National		Dual (2 units per package)			3 to 36	XR3303 XR3403 XR3503 † Exar μA3303C Fairchild μA3403C Fairchild μA3503M † Fairchild MC3303 Motorola MC3403 Motorola MC3503 † Motorola RC3403 Raytheon see page 649 RM3403 Raytheon see page 649 RM3503 † Raytheon see page 649 RV3403 Raytheon	100
	CA3078	RCA		3 to 30	LM158	† National			
	see page 666				LM258	National			
	CA3078A	† RCA			LM358	National			
	see page 666				NE532	† Signetics			
	CA3080	RCA			SE532	Signetics			
	see page 666								
	CA3080A	† RCA		8 to 36	TBA231	SGS			
	see page 666			Quad (4 units per package)			4 to 36	μA2900 Fairchild LM2900 National LM3900 National LM2900 Raytheon LM3900 Raytheon	110
	CA3094	† RCA		4 to 18	μA3401C	Fairchild			
	CA3094A	† RCA			MC5401	Motorola			
	CA3094B	† RCA			CA3401G	† RCA			
SG1250	† Silicon G			RC3401	Raytheon				
SG2250	Silicon G		3 to 26	LM2902	National				
SG3250	Silicon G		4 to 28	XR124	† Exar				
SG4250	† Silicon G			XR224	Exar				
SG4250C	Silicon G			μA3301C	Fairchild				
				MC3301	Motorola				
				RC3301	Raytheon				
Dual (2 units per package)			Quad (4 units per package)			Quad (4 units per package) (cont)			
Dual (2 units per package)	μA776C	Fairchild	4 to 18	μA3401C	Fairchild	3 to 30	XR324 LM124 † Intersil LM224 Intersil LM324 Intersil MLM324 Motorola LM124 † National LM224 National LM324 National CA124G † RCA see page 661 CA224G RCA see page 661 CA324G RCA see page 661 LM124 † Raytheon LM224 Raytheon LM324 Raytheon LM124 † Signetics LM224 Signetics LM324 Signetics SG124 † Silicon G SG224 Silicon G SG324 Silicon G LM124 † Teledyne S LM224 Teledyne S LM324 Teledyne S (continued)	70	
	μA776M	† Fairchild							
	HA-2730	† Harris							
	HA-2735	Harris							
	8022C	Intersil							
	8022M	† Intersil							
	LH24250	† National							
LH24250C	National								
Triple (3 units per package)			Triple (3 units per package)			Triple (3 units per package)			
Triple (3 units per package)	8023C	Intersil	3 to 26	LM2902	National	3 to 30	XR324 LM124 † Intersil LM224 Intersil LM324 Intersil MLM324 Motorola LM124 † National LM224 National LM324 National CA124G † RCA see page 661 CA224G RCA see page 661 CA324G RCA see page 661 LM124 † Raytheon LM224 Raytheon LM324 Raytheon LM124 † Signetics LM224 Signetics LM324 Signetics SG124 † Silicon G SG224 Silicon G SG324 Silicon G LM124 † Teledyne S LM224 Teledyne S LM324 Teledyne S (continued)	70	
	8023M	† Intersil							
	CA3060	RCA							
	CA3060	† RCA							
	CA3060A	RCA							
	CA3060B	RCA							
	L144A	† Siliconix							
L144B	Siliconix								
L144C	Siliconix								
Quad (4 units per package)			Quad (4 units per package)			Quad (4 units per package)			
Quad (4 units per package)	XR4202	Exar	3 to 30	XR324	Exar	3 to 30	LM124	† Intersil	

† Military Temperature Range (−55°C to 125°C)

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LINEAR—Operational Amplifiers (cont)

Unity Gain Bandwidth (MHz)	Device	Source	
Wide Band			
30*	μ A702C μ A702M LH0003 LH0003C LH0005 LH0005A LH0005C RC702 RM702 SN52702 SN72702 SN72702A	Fairchild † Fairchild † National National † National National † National Raytheon † Raytheon † TI TI TI	10
30	Q25AH	† Teledyne P	
35	825	† Beckman	
35*	AD507J see page 624 AD507K see page 624 AD507S see page 624	AD AD † AD	
38*	CA3100 see page 667	† RCA	
50	HFS23	DDC	
50*	3551J 3551S CA3015 CA3015A CA3016 CA3016A CA3030 CA3030A CA3038 CA3038A	Burr-Brown † Burr-Brown † RCA † RCA † RCA † RCA RCA RCA † RCA † RCA	20
60*	1430	Teledyne P	30
65*	μ A715C μ A715M	Fairchild † Fairchild	
70*	LH0024 LH0024C LH0032 LH0032C	† National National † National National	
100	HFB7 HVA23	DDC DDC	

† Military Temperature Range (–55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

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LINEAR—Operational Amplifiers - Characteristics

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift μv/°C	Bandwidth MHz	Slew Rate v/μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source
Single-Unit Package													
0.00001	20.0	—	100		0.5*	12 @ 1.2	20K	60	0	± 18	Ultra Low Bias FET	ICH8500A	Intersil
0.000075	1.0	—	25	0.35	0.3	10 @ 5	50K	70	0	± 5 to ± 18	FET Electrometer	AD515L see page 624	AD
0.0001	0.5	0.00005	25	1*	0.6	10 @ 10	100K	80*	0	± 5 to ± 20	Ultra Low Bias FET	3523L	Burr-Brown
	20.0	—	—		0.5*	12 @ 1.2	20K	60	0	± 18	Ultra Low Bias FET	ICH8500	Intersil
0.00015	1.0	—	15	0.35	0.3	10 @ 5	100K	80	0	± 5 to ± 18	FET Electrometer	AD515K see page 624	AD
0.00025	0.5	0.0001	25	1*	0.6	10 @ 10	100K	80*	0	± 5 to ± 20	Ultra Low Bias FET	3523K	Burr-Brown
0.0003	3.0	—	50	0.35	0.3	10 @ 5	40K	66	0	± 5 to ± 18	FET Electrometer	AD515J see page 624	AD
0.0005	1.0	0.0001*	30	0.5	3	10 @ 5	40K	80		± 12 to ± 18	Ultra Low Bias FET	142901	Teledyne P
		0.0002	50	1*	0.6	10 @ 10	100K	80*	0	± 5 to ± 20	Ultra Low Bias FET	3523J	Burr-Brown
	10.0	—	—			10 @ 5	50K		0	± 5 to ± 20	Inverting Separate FET Input	L137AA	† Siliconix
0.001	0.5	0.0001	5	1*	1.5	10 @ 10	100K	80	0	± 5 to ± 20	Precision FET	LH0052	† National
	5.0	0.0003*	90	0.5	3	10 @ 5	20K	70		± 12 to ± 18	Ultra Low Bias FET	1429	Teledyne P
		0.0005*	25	1*	0.6	10 @ 10	50K	90*	0	± 5 to ± 20	Low Offset FET	3522L	Burr-Brown
	30.0	0.0002*	50	1*	2.5	10 @ 5	20K	86	0	± 5 to ± 18	Low Bias FET	1001M	† DDC
												8007AM	† Intersil
												8007AC	Intersil
		0.0005*	50	1*	2.5	10 @ 5	31K	86*	0	± 4 to ± 20	High Performance, Low Bias FET	3503C 3503T	Burr-Brown † Burr-Brown
—	50*	1*	6*	10 @ 5	20K	86	0	± 6 to ± 18	FET	1439	Teledyne P		
50.0	0.0005*	90	0.5*	3	10 @ 5	20K	70	0	± 5 to ± 18	Electrometer, FET	AD523J see page 624	AD	
0.005	0.5	0.001*	25	1*	0.6	10 @ 10	50K	90*	0	± 5 to ± 20	Low Offset FET	3522K	Burr-Brown
												3522S	Burr-Brown
	1.0	0.0002	10	1*	1	10 @ 10	75K	76	0	± 5 to ± 20	Precision FET	LH0052C	National
		0.002*	10	1	3	10 @ 5	50K	70		± 12 to ± 18	Low Bias Current, FET Low Drift	142502	Teledyne P
				1	3	10 @ 5	50K	70		± 12 to ± 18	Low Bias Current, FET	142501	Teledyne P
	—	10	1*	3	10 @ 5	75K	80	0	± 5 to ± 18	High Accuracy, FET	AD506L see page 624	AD	
	5.0	0.0006		2*	50*	0.35 ma		80	0	± 2 to ± 15	Micropower, Transconductance Amplifier	CA3080 see page 666 CA3080A see page 666	RCA † RCA
20.0	—		30	0.5*	3	10 @ 5	40K	80	0	± 5 to ± 18	Electrometer, FET	AD523K see page 624	AD

† Military Temperature Range (–55°C to 125°C) * — Typical Values

Arranged in order of increasing bias current, offset voltage, offset current, and voltage drift. "Comp" indicates number of compensation components required.

LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{V}/^\circ\text{C}$	Bandwidth MHz	Slew Rate $\text{V}/\mu\text{s}$	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source	
Single-Unit Package (cont)														
0.005	20.0	—	—			10 @ 5	25K		0	± 5 to ± 20	Inverting Separate FET Input	L137CA	Siliconix	
0.010	0.25	0.002*	1	1.5*	0.6	10 @ 10	100K	90*	0	± 5 to ± 20	Ultra Low Drift FET	3521L	Burr-Brown	
	1.0	0.002*	50	1*	0.6	10 @ 10	50K	90*	0	± 5 to ± 20	Low Offset FET	3522J	Burr-Brown	
		0.005*	25	1	3	10 @ 5	50K	70		± 12 to ± 18	Low Drift, FET	142601	Teledyne P	
				10*	65	10 @ 10	25K	70*	0	± 5 to ± 20	Fast Settling, 1 μs to 0.01%	3550J	Burr-Brown	
												3550S	† Burr-Brown	
				20*	100	10 @ 10	25K	70*	0	± 5 to ± 20	Fast Settling, 0.6 μs to 0.01%	3550K	Burr-Brown	
	1.0	—		25	4*	3	10 @ 5	25K	80*	0	± 10 to ± 22	General Purpose FET	ADM501B	AD
	1.5	—		25	1*	3	10 @ 5	50K	80	0	± 5 to ± 18	High Accuracy, FET	AD506K	AD
				50	1*	3	10 @ 5	50K	80	0	± 5 to ± 22	High Accuracy, FET	AD506S	† AD
													see page 624	
2.0	0.0005*	5	1*	6*	10 @ 5	20K	70	0	± 5 to ± 18	Highest Performance, see 1001C665	1001C113	DDC		
			1*	3	10 @ 5	50K	70	0	± 5 to ± 18	Low Offset Voltage, FET	8007C-1	Intersil		
			15	1*	6*	10 @ 5	50K	70	0	± 5 to ± 18	Highest Performance, see 1001M664	1001M313	† DDC	
				1*	3	10 @ 5	50K	70	0	± 5 to ± 18	Low Offset Voltage, FET	8007C-2	Intersil	
											8007M-2	† Intersil		
	0.005*	50	1	3	10 @ 5	50K	70		± 12 to ± 18	Low Bias Current, FET	1425	Teledyne P		
—		75	4*	3	10 @ 5	25K	80*	0	± 10 to ± 22	General Purpose FET	ADM501A	AD		
4.0	0.002	10	1*	1.5	10 @ 10	100K	80	0	± 5 to ± 20	High Performance FET	LH0022	† National		
10.0	0.0005*	10	1*	3	10 @ 5	50K	70	0	± 5 to ± 18	FET Input	8007C-4	Intersil		
			15	1*	3	10 @ 5	50K	70	0	± 5 to ± 18	FET Input	8007C-5	Intersil	
											8007M-5	† Intersil		
15.0	0.005	25	1	3	10 @ 10	100K	80		± 5 to ± 18	General Purpose, Low Drift	142102	Teledyne P		
20.0	0.002*	25	1*	2.5	10 @ 5	31K	86*	0	± 4 to ± 20	High Performance, Low Bias FET	3503B	Burr-Brown		
											3503S	† Burr-Brown		
—		25	0.75*	0.5*	10 @ 5	50K*	70	0	± 5 to ± 18	Low Noise FET	AD514L	AD		
											see page 624			
0.015	0.25	0.002*	2	1.5*	0.6	10 @ 10	100K	90*	0	± 5 to ± 20	Ultra Low Drift FET	3521K	Burr-Brown	
	1.0	—	25	10*	50	10 @ 5	50K	80	0	± 15	Fast Wideband, High Accuracy	AD528K	AD	
											AD528S	† AD		
											see page 624	see page 624		
3.5	—	75	1*	3	10 @ 5	20K	70	0	± 5 to ± 18	High Accuracy, FET	AD506J	AD		
											see page 624			
15.0	0.01	25	1	3	10 @ 10	100K	72	0	± 5 to ± 18	Low Noise	1421-25	Teledyne P		
			50	1	3	10 @ 10	100K	72		± 5 to ± 18	General Purpose, Low Drift	142101	Teledyne P	

† Military Temperature Range (—55°C to 125°C) * — Typical Values

Bold face indicates additional data is provided on the page noted.

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LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{V}/^\circ\text{C}$	Bandwidth MHz	Slew Rate $\text{V}/\mu\text{s}$	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source	
Single-Unit Package (cont)														
0.015	15.0	0.01*	50	5	8	10 @ 5	100K	72		± 12 to ± 18	Wideband, FET	142201	Teledyne P	
	50.0	—	75	1*	3	10 @ 5	20K	70	0	± 5 to ± 18	Low Cost FET Input	AD503J see page 624	AD	
0.020	0.25	0.002*	5	1.5*	0.6	10 @ 10	50K	90*	0	± 5 to ± 20	Ultra Low Drift FET	3521J 3521R	Burr-Brown † Burr-Brown	
	0.5	0.002*	10	1.5*	0.6	10 @ 10	50K	90*	0	± 5 to ± 20	Ultra Low Drift FET	3521H	Burr-Brown	
	1.5	—	25	1*	50*	10 @ 5	50K	80	1-3	± 5 to ± 18	High Speed, Laser Trim	AD516K	AD	
	—	—	50	1*	50*	10 @ 5	50K	80	1-3	± 5 to ± 18	High Speed, Laser Trim	AD516S	† AD	
	2.0	0.010	15	4*	10*	12 @ 6	50K	86	1	5 to 16	CMOS, Single Supply, Strobe	CA3130B	† RCA	
	3	0.020*	25	3*	20*	70 @ 30 145 @ 15	50K 100K	110*	0	± 32 to ± 75 ± 70 to ± 150	High Voltage FET High Voltage FET	3581J 3582J	† Burr-Brown † Burr-Brown	
4.0	0.0005*	30	1*	3	10 @ 5	50K	70	0	± 5 to ± 18	FET Input	8007C-3	Intersil		
12.0	0.02	20*	5*	10*	10 @ 5	80K	74	1	± 10 to ± 17	Wide Band, FET Input	HA-2060A	† Harris		
			40*	5*	10*	10 @ 5	80K	70	1	± 10 to ± 17	Wide Band, FET Input	HA-2065A	Harris	
14.0	0.02	20*	8*	40*	10 @ 5	7.5K	74	1	± 5 to ± 17	120V/ μs Gain = 3	HA-2050A 143401	† Harris † Teledyne P		
			40*	8*	40*	10 @ 5	7.5K	70	1	± 5 to ± 17	120V/ μs Gain = 3	HA-2055A 1434	Harris Teledyne P	
20.0	0.0005*	75	1*	6*	10 @ 5	50K	70	0	± 5 to ± 18	High Performance, FET	8007M	† Intel		
			—	25	1*	3	10 @ 5	50K	80	1-3	± 5 to ± 18	High Speed	AD513K	AD
					0.75*	0.5*	10 @ 5	50K*	70	0	± 5 to ± 18	Low Noise FET	AD514K see page 624	AD
—	50	1*	3	10 @ 5	50K	80	1-3	± 5 to ± 18	High Speed	AD513S	† AD			
												0.75*	0.5*	10 @ 5
25.0	0.02	50*	5*	10*	10 @ 5	80K	74	1	± 5 to ± 17	120V/ μs Gain = 3	1015M HA-2060 143301	† DDC † Harris † Teledyne P		
			8*	40*	10 @ 5	7.5K	74	1	± 10 to ± 17	High Slew Rate, FET	1014M HA-2050	† DDC † Harris		
50.0	—	75	1*	6*	10 @ 5	50K	70	0	± 5 to ± 18	Low Performance Limit, See 1001M111	1001M664	† DDC		
60.0	0.02	60*	5*	10*	10 @ 5	80K	70	1	± 5 to ± 17	Wideband, FET Input	AM-406 1015C HA-2065 1433	Datel DDC Harris Teledyne P		
			8*	40*	10 @ 5	7.5K	70	1	± 5 to ± 17	120V/ μs Gain = 3	AM-405 1014C HA-2055	Datel DDC Harris		

† Military Temperature Range (–55°C to 125°C) * — Typical Values

Arranged in order of increasing bias current, offset voltage, offset current, and voltage drift. "Comp" indicates number of compensation components required.

LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{v}/^\circ\text{C}$	Bandwidth MHz	Slew Rate v/ μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source	
Single-Unit Package (cont)														
0.025	0.5	0.01*	25	6	20	10 @ 5	100K	80	0	± 12 to ± 18	Fast Settling, FET	142701	Teledyne P	
	1.0	0.01*	5	1	3	10 @ 5	50K	70	0	± 12 to ± 18	Low Drift, FET	142603	Teledyne P	
			10	1	3	10 @ 5	50K	70	0	± 12 to ± 18	Low Drift, FET	142602	Teledyne P	
	2.0	0.01*	50	1	3	10 @ 5	100K	72		± 12 to ± 18	Low Drift, FET	1426	Teledyne P	
	5.0	0.002	25	15*	50	10 @ 10	50K	80	0	± 5 to ± 20	Precision, High Speed, FET	LH0062	† National	
	6.0	0.002	15	1*	1	10 @ 10	75K	70	0	± 5 to ± 20	High Performance FET	LH0022C	National	
	20.0	0.002*	50	1*	0.5*	10 @ 10	25K	80*	0		± 5 to ± 20	Low Noise	3542J	Burr-Brown
													3542S	† Burr-Brown
		0.010	20	1*	1.5	10 @ 10	50K	70	0	± 5 to ± 20	Low Cost FET	LH0042	† National	
		—	25	1*	6*	10 @ 5	50K	70	0	± 5 to ± 18	Low Cost FET Input	AD540K see page 624	AD	
	—	50	1*	6*	10 @ 5	50K	70	0	± 5 to ± 22	Low Cost FET Input	AD540S	† AD		
	—	60	0.5*	3	10 @ 5	40K	80	0	± 5 to ± 18	Electrometer, FET	AD523L see page 624	AD		
	—	50	1*	0.5*	10 @ 5	25K	80	0	± 5 to ± 20	FET	AD3542J	AD		
50.0	0.005*	75	1*	2.5	10 @ 5	20K	86*	0	± 4 to ± 20	High Performance, Low Bias FET	3503A 3503R	Burr-Brown † Burr-Brown		
0.030	1.0	0.01*	10	1	3	13 @ 2	10K	76	0	± 4 to ± 24	Battery, FET Micro-power	140202	Teledyne P	
	3.0	0.1*	50	1	3	13 @ 2	10K	76	0	± 4 to ± 24	Battery, FET Micro-power	1402	Teledyne P	
												—	50	10*
	3.5	—	75	1*	50*	10 @ 5	20K	70	1-3	± 5 to ± 18	High Speed, Laser Trim	AD516J	AD	
												0.02	10*	4*
	20.0	0.005*	20*	1*	6*	10 @ 5	50K	70	0	± 6 to ± 20	FET	SU536	Signetics	
	50.0	—	75	1*	3	10 @ 5	20K	70	1-3	± 5 to ± 18	High Speed	AD513J	AD	
0.050	0.05	0.0005*	75*	1*	6*	10 @ 5	20K	70	0	± 5 to ± 18	FET	3540J	Burr-Brown	
	1.0	0.01*	50	6	20	10 @ 5	100K	80	0	± 12 to ± 18	Fast Settling, FET	1427	Teledyne P	
	2.0	0.01	5	2.5*	3	12 @ 1.2	50K	85	0	± 5 to ± 20	Bipolar - JFET	LF155A	† National	
												LF355A	National	
				4	10	12 @ 1.2	50K	85	0	± 5 to ± 20	Wideband - JFET	LF156A	† National	
												LF356A	National	
					12 @ 1.2	50K	85	1	± 5 to ± 20	Wideband Uncompensated	LF157A LF357A	† National National		
3.0	0.015	—	1*	0.3*	13 @ 1.3	40K	80	0	± 3 to ± 20	High Performance, Low Input Current	LM216A LM316A LM216A LM316A LM216A LM316A	AMD AMD National National Raytheon Raytheon		

† Military Temperature Range (—55°C to 125°C) * — Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift μv/°C	Bandwidth MHz	Slew Rate v/μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source
Single-Unit Package (cont)													
0.050	5.0	0.025	55			10 @ 5	37K	60	0	±6 to ±22	FET Input 741	2740B	Teledyne S
	10.0	0.020*	30	3*	15*	30 @ 60	20K	86*	0	±18 to ±35	High Voltage FET	3580J	† Burr-Brown
		0.025	100			10 @ 5	37K	60	0	±6 to ±22	FET Input 741	2740C	Teledyne S
	15.0	0.025	50	1	3	10 @ 10	50K	72		±5 to ±18	General Purpose	1421	Teledyne P
						10 @ 10	50K	72	0	±5 to ±18	GLow Noise	1421-24	Teledyne P
		0.025*	50	5	8	10 @ 5	50K	72		±12 to ±18	Wideband, FET	1422	Teledyne P
		0.030	10*	4*	10*	12 @ 6	320K*	70	1	5 to 16	CMOS, Single Supply, Strobe	CA3130 see page 664	† RCA
	20.0	0.005	25	1*	1	10 @ 10	25K	70	0	±5 to ±20	Low Cost FET	LH0042C	National
		0.025	150			10 @ 5	20K	60	0	±6 to ±22	FET Input 741	2740D	Teledyne S
	—		25	1*	6*	10 @ 10	25K	70	0	±5 to ±18	Low Cost FET	AD0042C	AD
	50.0	0.0005*	75	1*	6*	10 @ 5	20K	70	0	±5 to ±18	High Performance, FET	3540J 1001 8007C	Burr-Brown DDC Intersil
				1*	6*	10 @ 5	20K	70		±12 to ±18	Low Cost FET	1424	Teledyne P
			75	0.75*	0.5*	10 @ 5	20K	70	0	±5 to ±18	Low Noise FET	AD514J see page 624	AD
				1*	6*	10 @ 5	20K	70	0	±5 to ±18	Low Cost FET	AD540J see page 624	AD
				1*	6*	10 @ 5	20K	70	0	±5 to ±18	Low Performance Lim- it See 1001C111	1001C665	DDC
0.065	15.0	0.005	35	15*	50	10 @ 10	25K	70	0	±5 to ±20	Precision, High Speed, FET	LH0062C	National
0.10	1.0	0.01	50	50*	250*	10 @ 10	100K	70*	1	±5 to ±20	Wideband, Fast Set- tling	3551J 3551S	Burr-Brown † Burr-Brown
	2.0	0.05*	40	0.5*	3	30 @ 1A	50K	80	1	±15 to ±40	High Current, High Power	3571A	Burr-Brown
				0.5*	3	30 @ 2A	50K	80	1	±15 to ±40	High Current, High Power	3572A	Burr-Brown
	3.0	—	75	35	1000	10 @ 100	25K	72	0	±12 to ±18	Fast Settling	825	† Beckman
	5.0	0.02	5*	2.5*	5*	12 @ 1.2	50K	85	0	±5 to ±20	Bipolar - JFET	LF155 LF255	† National National
				5*	15*	12 @ 1.2	50K	85	0	±5 to ±20	Wideband - JFET	LF156 LF256	† National National
						12 @ 1.2	50K	85	1	±5 to ±20	Wideband Uncompensated	LF157 LF257	† National National
		0.025	25*	70*	350	10 @ 10	1K	50	2	±5 to ±20	Ultra Fast FET	LH0032	† National
		0.01*	50	10*	50	10 @ 20	100K	74*		±10 to ±18	Fast Differential, FET settles to 0.01% in 1 μsec	141410	Teledyne P
	20.0	—	25	1*	3	10 @ 5	50K	80	0	±5 to ±18	Low Cost FET Input	AD503K see page 624	AD
				1*	3	10 @ 5	50K	80	0	±5 to ±22	Low Cost FET Input	AD503S see page 624	† AD

† Military Temperature Range (-55°C to 125°C) * — Typical Values

Arranged in order of increasing bias current, offset voltage, offset current, and voltage drift.
"Comp" indicates number of compensation components required.

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LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{V}/^\circ\text{C}$	Bandwidth MHz	Slew Rate v/ μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source
Single-Unit Package (cont)													
0.10	90.0	0.005*	30*	1*	6*	10 @ 5	50K	64	0	± 6 to ± 20	FET, High Input, High Impedance	NE536	Signetics
0.15	10.0	0.05	—	1*	0.3*	13 @ 1.3	20K	80	0	± 3 to ± 20	High Performance, Low Input Current	LM216 LM316 LM216 LM316 LM216 LM316	AMD AMD National National Raytheon Raytheon
		0.01	55	30	8	11 @ 22	20K	94		± 12 to ± 18	FET	Q25AH	† Teledyne P
0.20	10.0	0.05	5*	2.5	5*	12 @ 1.2	50K	80	0	± 5 to ± 18	Bipolar - JFET	LF355	National
				5	15*	12 @ 1.2	50K	80	0	± 5 to ± 18	Wideband - JFET	LF356	National
						12 @ 1.2	50K	80	1	± 5 to ± 18	Wideband Uncompensated	LF357	National
15.0	0.05	25*	50*	350	10 @ 10	1K	50	2		± 5 to ± 20	Ultra Fast FET	LH0032C	National
	0.10	5*	1*	6*	10 @ 5	50K	80	0		± 22	FET input	LH740A	† National
		15*	1*	6*	10 @ 5	50K	80	0		± 5 to ± 20	FET input	740	† Intersil
20.0	0.15	20*	3*	6*	10 @ 5	50K	64	0		± 5 to ± 22	High Slew Rate FET	$\mu\text{A}740\text{M}$	† Fairchild
		—	3*	6*	10 @ 5	50K	64	0		± 5 to ± 22	High Slew Rate FET	740	Intersil
			100	1000	10 @ 30	—	—	0		± 15	Wideband Inverting	HFB7	DDC
			25	100	600	10 @ 30	—	—	0	± 15	Wideband Inverting	HVA23	DDC
0.50	2.0	75	60*	500	10 @ 50	200K		0		± 10 to ± 18	Inverting, Fast Settling 0.01% in 200 ns	1430	Teledyne P
	20.0	0.15	5*	1*	6*	10 @ 5	50K	80	0	to ± 22	FET input	LH740AC	National
			15*	1*	6*	10 @ 5	50K	80	0	± 5 to ± 20	FET Input	740C	Intersil
1	0.05	0.5	0.4	3*	2.5*	10 @ 5	10M	130	0	± 12 to ± 20	Chopper Stabilized	HA-2904	Harris
	0.06	0.5	0.6	3*	2.5*	10 @ 5	1000K	120	0	± 12 to ± 20	Chopper Stabilized	1012M HA-2900	† DDC † Harris
	0.08	0.5	0.2*	3*	2.5*	10 @ 5	1000K	120	0	± 10 to ± 20	Chopper Stabilized	AM-490 1012C HA-2905 1340	Datel DDC Harris Teledyne P
2	0.025	2	0.6	1.2*	0.25*	10.5 @ 10.5	300K	110	0	± 3 to ± 18	Ultra Low Offset Voltage, Low Drift	OP-07A	† PMI
	0.15	2	0.9	1.2*	0.25*	10.5 @ 10.5	300K	114	0	± 3 to ± 22	Instrumentation	OP-05A	† PMI
	0.5	0.2	5	1*	0.3*	13 @ 1.3	80K	96	1	± 2 to ± 20	Precision Bipolar, Low Bias	LM108A LM208A AD108A AD208A $\mu\text{A}108\text{AM}$ $\mu\text{A}208\text{AM}$ 108A 208A LM108A LM208A	† AMD AMD † AD see page 625 AD see page 625 † Fairchild Fairchild † Intersil Intersil † National National

† Military Temperature Range (–55°C to 125°C) * — Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{v}/^\circ\text{C}$	Bandwidth MHz	Slew Rate v/ μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source	
Single-Unit Package (cont)														
2	0.5	0.2	5	1*	0.3*	13 @ 1.3	80K	96	1	± 2 to ± 20	Precision Bipolar, Low Bias (continued)	SFC2108A	† NPC	
												SFC2208A	NPC	
												LM108A	† Raytheon	
												LM208A	Raytheon	
												CA108A	† RCA	
												CA208A	RCA	
												LM108A	† Signetics	
												LM208A	Signetics	
												SG108A	† Silicon G	
												SG208A	Silicon G	
												SN52108A	† TI	
					0.3*	0.1	13 @ 1.3	80K	96	0	± 5 to ± 20	Compensated 108A	SG1118A	† Silicon G
												SG2118A	Silicon G	
2.0	0.2	0.2	15	1*	0.2*	13 @ 1.3	50K	85	0	± 2 to ± 20	Micropower, Supply Current 600 μa	LM112	† AMD	
												LM212	AMD	
												LM112	† National	
												LM212	National	
												LM112	† Raytheon	
												LM212	Raytheon	
					1*	0.1*	13 @ 1.3	50K	85	0	± 5 to ± 20	Compensated 108/208	SG1118	† Silicon G
												SG2118	Silicon G	
					1*	0.3*	13 @ 1.3	50K	85	1	± 2 to ± 20	Precision Bipolar	LM108	† AMD
												LM208	AMD	
												AD108	† AD	
												see page 625		
												AD208	AD	
												see page 625		
												$\mu\text{A}108\text{M}$	† Fairchild	
												$\mu\text{A}208\text{M}$	Fairchild	
												108	† Intersil	
												208	Intersil	
												LM108	† National	
												LM208	National	
												SFC2108	† NPC	
												SFC2208	NPC	
												CA108	† RCA	
												CA208	RCA	
												LM108	† Raytheon	
												LM208	Raytheon	
												LM108	† Signetics	
												LM208	Signetics	
												SG108	† Silicon G	
												SG108	Silicon G	
												LM108	† Teledyne S	
												LM208	Teledyne S	
					0.3*	0.3*	13 @ 1.3	50K	85	1	± 5 to ± 20	Low Noise 108	108LN	† Intersil
30*	0.06*		1*	6*	6*	10 @ 5	1000K	80*	0	± 5 to ± 22	High Slew Rate FET	$\mu\text{A}740\text{C}$	Signetics	
110.0	0.3	20*	1*	6*	6*	10 @ 5	20K	55	0	± 5 to ± 22	High Slew Rate FET	$\mu\text{A}740\text{C}$	Fairchild	

† Military Temperature Range (–55°C to 125°C) * — Typical Values

Arranged in order of increasing bias current, offset voltage, offset current, and voltage drift. "Comp" indicates number of compensation components required.

LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{V}/^\circ\text{C}$	Bandwidth MHz	Slew Rate v/ μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source										
Single-Unit Package (cont)																							
2	110.0	0.3	—	1*	6*	10 @ 5	20K	55	0	± 5 to ± 22	High Slew Rate FET	740C	Intersil										
3	0.075	2.8	1.3	1.2*	0.25*	10.5 @ 10.5	200K	110	0	± 3 to ± 18	Ultra Low Offset Voltage, Low Drift	OP-07	† PMI										
	0.5	2.8	2	1.2*	0.25*	10.5 @ 10.5	200K	114	0	± 3 to ± 22	Instrumentation	OP-05	† PMI										
	2.0	2	10	0.5*	0.1	10 @ 5	45K	100*	0	± 3 to ± 20	Low Bias Current	3501C 3501T	Burr-Brown † Burr-Brown										
4	0.075	3.8	1.3	1.2*	0.25*	10.5 @ 10.5	200K	106	0	± 3 to ± 18	Ultra Low Offset Voltage, Low Drift	OP-07E	PMI										
	0.5	3.8	2	1.2*	0.25*	10.5 @ 10.5	200K	110	0	± 3 to ± 22	Instrumentation	OP-05E	PMI										
	5.0	1	10	1*	0.5*	10 @ 5	20K	80	0	± 5 to ± 18	Low Input Current	AD502L see page 625	AD										
				0.5*	10 @ 5	15K	65	1	± 5 to ± 18	Low Input Current 709	AD801B	AD											
2	20	0.5*	10 @ 5	15K	65	1	± 5 to ± 18	Low Input Current 709	AD801A	AD													
			40	0.5*	10 @ 5	15K	65	1	± 5 to ± 18	Low Input Current 709	AD801S	† AD											
5	3.0	3	10*		0.1*	10 @ 2	40K	80	0	± 1.2 to ± 18	Programmable Amplifier	HA-2720	† Harris										
7	0.15	6	1.8	1.2*	0.25*	11.5 @ 5.7	120K	100	0	± 3 to ± 18	Ultra Low Offset Voltage, Low Drift	OP-07C	PMI										
	0.5	1	5	1*	0.3*	13 @ 1.3	80K	96	1	± 2 to ± 18	Precision Bipolar	LM308A AD308A see page 625 $\mu\text{A}308\text{AC}$ 308A LM308A CA308A LM308A LM308A SG308A	AMD AD Fairchild Intersil National RCA Raytheon Signetics Silicon G										
											0.3*	0.1	13 @ 1.3	80K	96	0	± 5 to ± 15	Compensated 308A	SG3118A	Silicon G			
											1.3	6	4.5	1.2*	0.25*	11.5 @ 5.7	120K	100	0	± 3 to ± 22	Instrumentation	OP-05C	PMI
											2.0	3	10	0.5*	0.1	10 @ 5	45K	100*	0	± 3 to ± 20	Low Bias Current	3501B 3501S	Burr-Brown † Burr-Brown
											5.0	4	20	1*	0.5*	10 @ 5	20K	80	0	± 5 to ± 18	Low Input Current	AD502K see page 625	AD
											7.5	1	30	1*	0.3*	13 @ 1.3	25K	80	0	± 2 to ± 18	Micropower, Supply Current 800 μa	LM312 LM312 LM312	AMD National Raytheon
											0.3*	0.1	13 @ 1.3	25K	80	0	± 5 to ± 18	Compensated 308	SG3118	Silicon G			
											1*	0.3*	13 @ 1.3	25K	80	1	± 2 to ± 18	Precision Bipolar	LM308 AD308 see page 625 $\mu\text{A}308\text{C}$ LM308 LM308 SFC2308 CA308 LM308	AMD AD Fairchild Intersil National NPC RCA Raytheon			

† Military Temperature Range (–55°C to 125°C) * — Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{V}/^\circ\text{C}$	Bandwidth MHz	Slew Rate $\text{V}/\mu\text{s}$	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source	
Single-Unit Package (cont)														
7	7.5	1		1*	0.3*	13 @ 1.3	25K	80	1	± 2 to ± 18	Precision Bipolar (continued)	LM308 SG308 LM308	Signetics Silicon G Teledyne S	
				0.3*	0.3*	13 @ 1.3	25K	80	1	± 5 to ± 18	Low Noise 308	308LN	Intersil	
7.5	3.0	3	—	.25*	0.16*	12 @ 1.2	100K	70	0	± 1 to ± 18	Programmable	4250 LM4250	† Intersil † National	
10	0.025	2.5	2	0.3*	0.1*	10 @ 5	1000K	110	0	± 5 to ± 18	Trimmed Offset	AD510L see page 625 AD510S see page 625	AD † AD	
	3.0	2	15	0.3*	0.13*	10 @ 5	50K	80	0	± 3 to ± 20	Micropower	RM4132	† Raytheon	
				12*	4	10 @ 5	100K	80	0	± 9 to ± 20	High Impedance	HA-2600	† Harris	
	4.0	10	5*	12*	4	10 @ 5	100K	80	0	± 5 to ± 20	High Impedance	1008M	† DDC	
	5.0	5	7*	1*	0.5*	10 @ 5	20K	70	0	± 1 to ± 18	Low Input Current	8008M	† Intersil	
				10*	0.1*	10 @ 2	25K	74	0	± 1.2 to ± 18	Programmable Amplifier	HA-2725	Harris	
		6	—	.25*	0.16*	12 @ 1.2	60K	70	0	± 1 to ± 18	Programmable	4250C LM4250C SG4250	Intersil National Silicon G	
12	3.0	5	4*		0.2*	11 @ 1.1	100K	70	0	± 0.75 to ± 18	Programmable	SG1250 SG2250	† Silicon G † Silicon G	
	3.5	2.5	6*		0.04*	13.7 @ 1.37	40K	80	1	± 0.75 to ± 15	Micropower	CA3078A see page 666	† RCA	
					0.04*	13.7 @ 1.37	40K	80	1	± 0.75 to ± 15	Low Noise, Micropower	CA6078A	† RCA	
13	0.05	4.0	1	0.3	0.1*	10 @ 5	1000K	110	0	± 5 to ± 18	Trimmed Offset	AD510K see page 625	AD	
15	0.025	2.5	0.5	0.4*	0.06*	13 @ 1.3	1000K	120	1	± 2 to ± 20	Precision, Low Noise	LH0044A LH0044AC	† National National	
	1.0	7*	3	1.5*	1	10 @ 10	45K	100*	0	± 3 to ± 20	Low Bias, Low Noise	3500C	† Burr-Brown	
			5	1.5*	1	10 @ 10	45K	100*	0	± 3 to ± 20	Low Bias, Low Noise	3500T	† Burr-Brown	
		7	—		1.5*		50K		0	± 22	Low Input Bias, High Slew Rate	ULS-2171	† Sprague	
	2.0	5	3	3	1.5	12 @ 6	40K	80	0	± 3 to ± 22	High Performance, High Gain	RM1556A	† Raytheon	
	3.0	15	15	35*	25	10 @ 5	100K	80	1	± 5 to ± 20	Wideband, General Purpose	AD507K see page 624	AD	
	4.0	2	15	4*	2*	12 @ 6	40K	80	0	± 3 to ± 22	High Performance, High Gain	RM1556	† Raytheon	
			—	1*	2.5*	12 @ 6	100K	80	0	± 3 to ± 22	High Performance	MC1556 SG1556	† Motorola † Silicon G	
		15	10*	35*	25	10 @ 15	100K	80	1	± 5 to ± 20	Wide Band, High Impedance	1018M HA-2620	† DDC † Harris	
				20	35*	20	10 @ 5	100K	80	1	± 5 to ± 20	Wideband, General Purpose	AD507S see page 624	† AD

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† Military Temperature Range (−55°C to 125°C) * — Typical Values

Arranged in order of increasing bias current, offset voltage, offset current, and voltage drift. "Comp" indicates number of compensation components required.

LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{v}/^\circ\text{C}$	Bandwidth MHz	Slew Rate v/ μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source	
Single-Unit Package (cont)														
15	5.0	5	20	0.5*	0.1	10 @ 5	45K	100*	0	± 3 to ± 20	Low Bias Current	3501A	Burr-Brown	
												3501R	† Burr-Brown	
												1660	AMD	
												SG1660	Silicon G	
	7.5	2	30		0.1	13 @ 1.3	25K	80	1	± 6 to ± 18	Precision	1660	AMD	
				0.3*	0.1	13 @ 1.3	25K	80	1	± 5 to ± 15	Improved 201, 301A	SG1660	Silicon G	
				0.3*	0.1	13 @ 1.3	25K	80	0	± 5 to ± 15	Improved 307, 741	SG1760	Silicon G	
20	2.0	10*	5	1.5*	1	10 @ 10	45K	100*	0	± 3 to ± 20	Low Bias, Low Noise	3500B	Burr-Brown	
												3500S	† Burr-Brown	
		3.0	2.5*	30*	1*	10	12 @ 10	200K	80	0	± 5.5 to ± 20	Micropower, High Output Current	132301	Teledyne P
													8	25
		7.5	5*	0.27*	0.16*	11 @ 1.1	50K	70	0	± 1 to ± 18	Low Power Adjustable Current	1003M	† DDC	
												8021M	† Intersil	
		10	5*	1*	10	12 @ 6	400K	86	0	± 5.5 to ± 20	Wide Response, Low Power	1011M	† DDC	
												HA-2700	† Harris	
												HA-2704	Harris	
		5.0	3	—	1*	2*	30 @ 6	100K	80	0	± 5 to ± 40	High Voltage	MC1536	† Motorola
	SG1536												† Silicon G	
	14.0	—	35*	20*	60	10 @ 10	40K*	90	0	± 5 to ± 17	High Slew Rate	14301	† Teledyne P	
												75*	20*	60
25	0.1	5	3	3*	0.1*	10 @ 5	250K	94	0	± 5 to ± 18	Trimmed Offset	AD510J	AD	
													see page 625	
		2.0	3	15	0.5	0.5*	10 @ 5	50K	80	1	± 5 to ± 18	Low Offset Current	$\mu\text{A}777\text{M}$	† Fairchild
													SG777	† Silicon G -
												SN52777	† TI	
		2.5	5	3	0.3*	0.12*	10 @ 5	250K	94	1	± 5 to ± 15	Chopperless, Low Drift	AD508J	AD
													see page 625	
		—	15*	4*	120	10 @ 5	200K		0	± 5 to ± 20	High Speed Inverting	AD505K	AD	
												AD505S	† AD	
		3.0	5	10*			5 @ 50	4K	60	3	± 9 to ± 20	Matched Transistors	LH0005A	† National
													4.0	12
		5.0	5	20	0.3*	0.13*	10 @ 5	50K	70	0	± 3 to ± 18	Micropower	RC4132	Raytheon
	25												10*	12*
												HA-2602	† Harris	
												HA-2605	Harris	
				35*	20	10 @ 5	80K	74	1	± 5 to ± 20	Wide Band, High Impedance	AM-462	Datel	
												1018C	DDC	
												HA-2622	† Harris	
												HA-2625	Harris	
				20*	12*	10 @ 10	80K	74	0	± 8 to ± 22	Wideband	3506J	Burr-Brown	
				30*	1	10 @ 10	80K	74	1	± 8 to ± 22	Wideband	3508J	Burr-Brown	

† Military Temperature Range (−55°C to 125°C) * — Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{V}/^\circ\text{C}$	Bandwidth MHz	Slew Rate v/ μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source			
Single-Unit Package (cont)																
25	5.0	25	10*	20	10 @ 10	80K	100*	1	± 8 to ± 22	Wide Band, High Gain	1321 132101	Teledyne P † Teledyne P				
				—	12*	4	10 @ 5	80K	74	0	± 5 to ± 20	High Impedance	1008C	DDC		
	6.0	10	6*	0.2*	11 @ 1.1	75K	70	0	± 0.75 to ± 18	Programmable	SG3250	Silicon G				
		12	40	1*	0.5*	10 @ 5	20K	80	0	± 5 to ± 18	Low Input Current	AD502J see page 625	AD			
		20	15*	0.5*	10 @ 5	20K	70	0	± 1 to ± 18	Low Input Current	8008C	Intersil				
25	15*	35*	20	10 @ 5	80K	74	1	± 5 to ± 20	Wideband, General Purpose	AD507J see page 624	AD					
30	0.05	5	0.5	0.4*	0.06*	12 @ 1.2	500K	114	1	± 2 to ± 20	Precision, Low Noise	LH0044B	National			
			1	0.4*	0.06*	12 @ 1.2	500K	114	1	± 2 to ± 20	Precision Low Noise	LH0044	† National			
35	0.5	2	8	0.8	0.25	12 @ 6	100K	90	0	± 5 to ± 20	General Purpose	OP-02A OP-02E	† PMI PMI			
			0.1	5	1	0.4*	0.06*	12 @ 1.2	500K	114	1	± 2 to ± 20	Precision, Low Noise	LH0044C	National	
	0.5	5	5	1*	0.25*	10 @ 5	80K	90	1	± 5 to ± 18	General Purpose	AD301AL see page 625	AD			
	0.7	2	5	2.5*	18*	12 @ 6	50K	90	0	± 5 to ± 22	High Speed	OP-01 OP-01H	† PMI PMI			
	1.0	7	10	0.1	0.12	13 @ 1	25K	94	0	± 2 to ± 18	Micropower	140411	Teledyne P			
	2.0	5	15	1.0	1.0	10 @ 5	100K	80	0	± 5 to ± 20	Improved 107	844B	† Teledyne S			
					1.0	10 @ 5	100K	80	1	± 5 to ± 20	Improved 101A	846B	† Teledyne S			
	5.0	7	20	0.1	0.12	13 @ 1	25K	94	0	± 2 to ± 18	Micropower	140410	Teledyne P			
					10	20	1.5	3	11 @ 5.5	40K	70	0	± 3 to ± 18	High Performance, High Gain	RC1556A	Raytheon
	15*	20	1.5*	0.6	10 @ 10	45K	100*	0	± 3 to ± 20	Low Bias, Low Noise	3500A 3500R	Burr-Brown † Burr-Brown				
					6.0	10	5*	0.27*	0.16*	11 @ 1.1	50K	70	0	± 1 to ± 18	Low Power Adjustable Current	1003 8021C
	30	15*	4*	5*	35 @ 10	100K	74	0	± 10 to ± 40	High Voltage	AM-464 HA-2645 1332	Datel Harris Teledyne P				
					10.0	10	20	4*	2*	11 @ 5.5	40K	70	0	± 3 to ± 18	High Performance, High Gain	RC1556
—					1*	2.5*	11 @ 5.5	70K	70	0	± 3 to ± 18	High Performance	MC1456 SG1456	Motorola Silicon G		
40	5.0	2.5	30*	1*	10	12 @ 10	200K	80	0	± 5.5 to ± 20	Micropower FET High Current Out	1323	Teledyne P			
					15	10	1*	10	12 @ 6	200K	80	0	± 5.5 to ± 20	Wide Response, Low Power	1011C HA-2705	DDC Harris
					20	0.5	0.2	2.5	10 @ 5	1 to 1000	70	1	± 5 to ± 18	Full Instrumentation	AD520K AD520S	AD † AD

† Military Temperature Range (–55°C to 125°C) * — Typical Values

Arranged in order of increasing bias current, offset voltage, offset current, and voltage drift. "Comp" indicates number of compensation components required.

LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{V}/^\circ\text{C}$	Bandwidth MHz	Slew Rate v/ μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source
Single-Unit Package (cont)													
40	10.0	10	—	1*	2*	20 @ 4	70K	70	0	± 5 to ± 34	High Voltage	MC1436 SG1436	Motorola Silicon G
50	0.5	5	5	1*	0.5*	10 @ 5	50K	90	0	± 5 to ± 22	Higher Accuracy 741	AD741L see page 625	AD
		30	1	1.5*	0.8	10 @ 10	100K*	100*	0	± 3 to ± 20	Low Drift	3500E	Burr-Brown
	2.0	5	8	2.5*	18*	12 @ 6	50K	80	0	± 5 to ± 22	High Speed	OP-01E OP-01F	PMI † PMI
		10	0.8	0.25		12 @ 6	50K	90	0	± 5 to ± 20	General Purpose	OP-02 OP-02C	† PMI PMI
	15	1*	0.4		10 @ 5	50K	80	0	± 8 to ± 22	High Performance, Low Drift	131901	† Teledyne P	
	2.2				10 @ 5	100K	80	0	± 5 to ± 20	High Performance 741	SSS741 SSS741	† AMD † PMI	
	—				0.6*		50K		0	to ± 22	General Purpose	ULS-2151	† Sprague
	10	15	4*	1.5		10 @ 5	25K	80	0	± 3 to ± 20	High Performance, High Gain	RM4131	† Raytheon
	50	25	1*	0.4		10 @ 5	50K	80	0	± 8 to ± 22	High Performance, Low Drift	1319	Teledyne P
	3.0	5	2.2			10 @ 5	50K	80	0	± 5 to ± 20	Higher Performance	SSS741B	PMI
	5.0	15	—	0.2	0.8*	10 @ 2	100K	70	0	± 1.2 to ± 18	Programmable Low Power	MC1776	† Motorola
	20	20*	—	0.8		10 @ 5	25K	80	0	± 3 to ± 20	General Purpose	1320	Teledyne P
			—	1.5*			25K		0	to ± 20	Low Input Bias, High Slew Rate	ULN-2171	Sprague
6.0	25	—	0.2	0.8*	10 @ 2	50K	70	0	± 1.2 to ± 18	Programmable Low Power	MC1776C	Motorola	
			0.8*	12 @ 1.2	50K	70	0	± 6 to ± 15	Programmable, Low Power	MC3476	Motorola		
10.0	20	20*			5 @ 50	2K	55	3	± 9 to ± 20	Matched Input Transistors	LH0005	† National	
70	0.1	1	0.6		11 @ 11	1000K	120	4	± 1.5 to ± 22	Instrumentation	SSS725A	† PMI	
			0.8		11 @ 11	1000K	120	4	± 3 to ± 22	High Performance 725	SSS725A	† AMD	
75	0.5	5	2	1	0.005*	10 @ 5	1000K	110	4	± 3 to ± 22	High Accuracy Instrumentation	$\mu\text{A}725\text{AM}$	† Fairchild
	2.0	10	15	1*	0.5*	10 @ 5	50K	80	0	± 5 to ± 20	General Purpose, Compensated	LM107 LM207 $\mu\text{A}107\text{M}$ $\mu\text{A}207\text{M}$ 107 207 MLM107 MLM207 LM107 LM207 SFC2107 SFC2207 LM107 LM207 CA107G see page 661 CA207G see page 661	† AMD AMD † Fairchild Fairchild † Intersil Intersil † Motorola Motorola † National National † NPC NPC † Raytheon Raytheon † RCA see page 661 RCA see page 661

† Military Temperature Range (−55°C to 125°C) * — Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{v}/^\circ\text{C}$	Bandwidth MHz	Slew Rate $\text{v}/\mu\text{s}$	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source
Single-Unit Package (cont)													
75	2.0	10	15	1*	0.5*	10 @ 5	50K	80	0	± 5 to ± 20	General Purpose, Compensated (continued)	LM107 LM207 SG107 SG207 LM107 LM207 SN52107	† Signetics Signetics † Silicon G Silicon G † Teledyne S Teledyne S † TI
				1*	0.5*	10 @ 10	50K	80	0	± 5 to ± 20	Higher Accuracy 741	AD741S 7411C	AD Intersil
				1*	0.5*	10 @ 5	50K	90	0	± 5 to ± 20	Higher Accuracy 741C	AD741K	† AD see page 625
				1*	0.5*	10 @ 5	50K	80	1	± 5 to ± 20	General Purpose, Improved 101, Uncompensated	LM101A LM201A AD101A AD201A $\mu\text{A}101\text{AM}$ $\mu\text{A}201\text{AM}$ 101A 201A MLM101A MLM201A LM101A LM201A LM101A LM201A CA101AG CA201AG LM101A LM201A SG101A SG201A LM101A LM201A LM101A LM201A SN52101A	† AMD AMD † AD see page 625 AD see page 625 † Fairchild Fairchild † Intersil Intersil † Motorola Motorola † National National † Raytheon Raytheon † RCA see page 661 RCA see page 661 † Signetics Signetics † Silicon G Silicon G † Siliconix Siliconix † Teledyne S Teledyne S † TI
				0.8*	0.5*	10 @ 5	50K	80	1	± 5 to ± 20	Low Noise 101A	101ALN	† Intersil
				30	1	10 @ 5	50K	70	0	± 5 to ± 15	Improved 307	844C	Teledyne S
					1	10 @ 5	50K	70	1	± 5 to ± 15	Improved 301A	846C	Teledyne S
			15*	4*	120	10 @ 5	100K		0	± 5 to ± 20	High Speed Inverting	AD505J	AD
80	0.75	5	1			11 @ 11	1000K	110	4	± 1.5 to ± 22	Instrumentation	SSS725B	PMI
			2.8*			11 @ 11	1000K	110	4	± 3 to ± 22	High Performance 725	SSS725B	AMD

† Military Temperature Range (−55°C to 125°C) * — Typical Values

Arranged in order of increasing bias current, offset voltage, offset current, and voltage drift. "Comp" indicates number of compensation components required.

LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{V}/^\circ\text{C}$	Bandwidth MHz	Slew Rate v/ μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source						
Single-Unit Package (cont)																			
80	0.75	5		1*	0.3*	10 @ 5	50K	80	0	± 5 to ± 22	High Performance	$\mu\text{A}741\text{AM}$	† Fairchild						
					0.44	0.3	10 @ 5	50K	80	0	± 5 to ± 22	High Performance	$\mu\text{A}741\text{EC}$	Fairchild					
	1.5	5					11 @ 11	1000K	120	4	± 1.5 to ± 22	Instrumentation	SSS725E	PMI					
							1	11 @ 11	1000K	120	4	± 15 to ± 22	Instrumentation	SSS725	† PMI				
							2	11 @ 11	1000K	120	4	± 3 to ± 22	High Performance 725	SSS725	† AMD				
							0.5*	0.005*	12 @ 6	1000K	120	4	± 3 to ± 22	Instrumentation	LM725A	† National			
	10						11 @ 11	1000K	120	4	± 3 to ± 22	High Performance 725	SSS725E	AMD					
							0.5	0.3*	0.12*	10 @ 5	1000K	110	1	± 5 to ± 18	Low Drift, Low Noise	AD504M	AD		
							1	0.3*	0.12*	10 @ 5	1000K	110	1	± 5 to ± 18	Low Drift, Low Noise	AD504L	AD		
								0.3*	0.12*	10 @ 5	1000K	110	1	± 5 to ± 22	Ultra Stable	AD504S	† AD		
	10.0	40	1000	0.2	2.5	10 @ 5	1 to 1000	65	1	± 5 to ± 18	Full Instrumentation	AD520J	AD						
90	12.0	25	—	1*	2*	20 @ 4	50K	50	0	± 5 to ± 30	High Voltage	MC1436C	Motorola						
															SG1436C	Silicon G			
		30	—	1*	2.5*	10 @ 5	25K	110*	0	± 3 to ± 18	High Performance	MC1456C	Motorola						
100	1.0	20	4*	1*	0.25*	10 @ 5	25K	70	2	± 5 to ± 20	General Purpose Low Quiescent Power	LH0001	† National						
						1*	0.25*	30 @ 15	30K	70	2	± 5 to ± 40	High Voltage	LH0004	† National				
						5		10 @ 5	1000K	110	4	± 5 to ± 22	Instrumentation	725	† AMD				
						1*	0.005*	10 @ 5	1000K	120	4	± 3 to ± 22	High Accuracy Instrumentation	$\mu\text{A}725\text{M}$	† Fairchild				
						0.5*	0.005*	10 @ 5	1000K	110	4	± 3 to ± 22	Instrumentation	LM725	† National				
							0.01*	10 @ 5	1000K	110	4	± 3 to ± 22	Instrumentation	RM725	† Raytheon				
						1.5	15	3	0.3*	0.12*	10 @ 5	500K	100	1	± 5 to ± 18	Low Drift, Low Noise	AD504K	AD	
								20	10			10 @ 5	500K	100	4	± 5 to ± 22	Instrumentation	725B	AMD
						2.5	20	3*	1*	0.25*	10 @ 5	25K	70	2	± 5 to ± 20	Micropower, High Performance	LH0001A	† National	
						3.0	20	5*		280	10 @ 5	100K	86	1	± 10 to ± 20	High Slew Rate Inverting	1010M	† DDC	
										HA-2530	† Harris								
5.0	20	10	2.5*	18*	12 @ 6	25K	80	0	± 5 to ± 20	High Speed	OP-01C	PMI							
										OP-01G	† PMI								
						30	1*	0.5*	10 @ 5	25K	70	1	± 5 to ± 18	Precision	777C	Fairchild			
							0.5	0.5*	10 @ 5	25K	70	1	± 5 to ± 15	Precision	SG777C	Silicon G			
								0.5*	10 @ 5	25K	70	1	± 5 to ± 18	Precision	SN72777	TI			
5.0	20	—				10 @ 5	50K	70	0	± 5 to ± 15	High Performance 741C	SSS741C	AMD						
		25	5			10 @ 5	50K	70	0	± 5 to ± 20	High Performance 741	SSS741G	† PMI						

† Military Temperature Range (–55°C to 125°C) * — Typical Values

Bold face indicates additional data is provided on the page noted.

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LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{v}/^\circ\text{C}$	Bandwidth MHz	Slew Rate v/ μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source	
Single-Unit Package (cont)														
100	6.0	25	6			10 @ 5	20K	70	0	± 5 to ± 18	High Performance 741C	SSS741C	PMI	
	10.0	25	25*			4 @ 40	2K	50	3	± 9 to ± 20	Matched Input Transistors	LH0005C	† National	
110	1.3	13	1.5			11.5 @ 5.7	500K	100	4	± 1.5 to ± 22	Instrumentation	SSS725C	PMI	
120	1.5	45	4*	1*	0.25*	30 @ 15	30K	70	2	± 5 to ± 40	High Voltage	LH0004C	National	
125	2.5	35	2*			10 @ 5	250K	96	4	± 5 to ± 22	Instrumentation	725C	AMD	
			2*	1*	0.005*	10 @ 5	250K	94	4	± 3 to ± 22	High Accuracy Instrumentation	725C LM725C RC725	Fairchild National Raytheon	
150	5.0	20	20	4*	2*	10 @ 5	25K	70	0	± 3 to ± 18	High Performance, High Gain	RC4131	Raytheon	
	—	—	25	50	400	10 @ 30		0	± 15	Fast Settling, Inverting		HFS23	DDC	
170	4.5	32	6*		0.04*	5 @ 0.5	25K	80	1	± 0.75 to ± 6	Micropower	CA3078 see page 666	RCA	
180	5.0	25	6.6*		3*	11 @ 38	22K	93	2	to ± 15	High Output Current	CA3033A	† RCA	
			—		3*	11 @ 38	22K	93	2	to ± 15	High Output Current	CA3047A	RCA	
200	1.0	50	6	1*	0.4*	10 @ 5	25K	80	3	± 5 to ± 18	General Purpose	RM709A	† Raytheon	
	2.0	50	10	5*	0.3*	10 @ 5	25K	80	3	± 9 to ± 15	General Purpose	μ A709AM ITT709-A MC1709A LM709A SFC2709A μ A709A SN52709A	† Fairchild † ITT † Motorola † National † NPC † Signetics † TI	
	2.5	40	5.0	0.3*	0.12*	10 @ 5	250K	94	1	± 5 to ± 18	Low Drift, Low Noise	AD504J see page 625	AD	
	3.0	50	20	1*	0.5*	10 @ 10	50K	80	0	± 5 to ± 18	Higher Accuracy 741C	AD741J see page 625	AD	
	3.0	50	20	1*	0.5*	10 @ 10	50K	80	0	± 5 to ± 18	High Current	AD512K	AD	
		25	1*	0.5*	0.5*	10 @ 10	50K	80	0	± 5 to ± 18	High Current	AD512S	† AD	
	4.0	50	15	12*	10	12 @ 6	50K	80	0	± 5 to ± 20	High Speed, Fast Settling	AD518K see page 624	AD	
			20	12*	10	12 @ 6	50K	80	0	± 5 to ± 20	High Speed, Fast Settling	AD518S see page 624	† AD	
			20	5*	250	10 @ 5	100K	80	1	± 10 to ± 20	High Slew Rate Inverting	101C HA-2535	DDC Harris	
			25	20*	12*	25	10 @ 5	20K	80	0	± 10 to ± 20	High Slew Rate	HA-2500	† Harris
			50	20*	8*	15*	10 @ 5	50K	80	1	± 10 to ± 20	Four Addressable Inputs Single Amplifier	454C 454M HA-2400 HA-2404	† DDC † DDC † Harris Harris
			60	3*	1*	0.25*	10 @ 5	25K	70	2	± 5 to ± 20	Micropower, High Performance	LH0001AC	National

† Military Temperature Range (–55°C to 125°C) * — Typical Values

Arranged in order of increasing bias current, offset voltage, offset current, and voltage drift. "Comp" indicates number of compensation components required.

LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{v}/^\circ\text{C}$	Bandwidth MHz	Slew Rate v/ μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source	
Single-Unit Package (cont)														
200	5.0	—	10*	10*	130	10 @ 5	25K	2	2 to ± 18	High Speed Inverting	8017M	† Intersil		
	7.0	10*	10*	10*	130*	10 @ 5	25K	2	to ± 18	High Speed Inverting	8017C	Intersil		
	8.0	25	20*	10*	50	10 @ 5	10K	80	0	± 10 to ± 20	High Slew Rate	1009M HA-2510	† DDC † Harris	
					10*	120*	10 @ 5	10K	80	1	± 10 to ± 20	High Slew Rate	HA-2520	† Harris
					30	20*	100	10 @ 5	10K	80	1	± 5 to ± 20	High Speed, Fast Settling	AD509K see page 624 AD509S † AD see page 624
250	2.5	50	10*	1*	0.25*	14.2 @ 47	100K	90	2	± 5 to ± 22	High Gain Instrumentation, 50 ma	LH0020	† National	
	4.0	50	—	15*	50	12 @ 6	50K	80	0	± 5 to ± 20	Precision High Speed	LM118	† AMD	
												LM218	AMD	
												LM118	† National	
												LM218	National	
												SFC2118	† NPC	
												SFC2218	NPC	
	5.0	20	20	1*	1*	0.5*	10 @ 5	25K	96	1	± 5 to ± 20	General Purpose	LM301A	Raytheon
	10 @ 5						25K	96	0	± 5 to ± 20	General Purpose	LM307	Raytheon	
		25	1*	1*	0.4	10 @ 5	50K	80	0	± 8 to ± 22	High Performance, Low Drift	1319	Teledyne P	
5.0	—											0.6*	25K	0
7.5	50	30	1*	0.5*	10 @ 5	25K	70	0	± 5 to ± 15	General Purpose, Uncompensated	LM307 LM307 $\mu\text{A}307\text{C}$ MLM307 LM307 SFC2307 CA307G see page 661 LM307 SG307 LM307 SN72307	AMD Fairchild Intersil Motorola National NPC RCA Signetics Silicon G Teledyne S TI		
				1*	0.5	10 @ 5	25K	70	1	± 5 to ± 15	General Purpose, Compensated	LM301A AD301A see page 625 $\mu\text{A}301\text{A}$ 301A MLM301A LM301A SFC2301A CA301AG see page 661 LM301A SG301A	AMD AD Fairchild Intersil Motorola National NPC RCA Signetics Silicon G	

† Military Temperature Range (–55°C to 125°C) * — Typical Values

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LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{v}/^\circ\text{C}$	Bandwidth MHz	Slew Rate v/ μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source
Single-Unit Package (cont)													
250	7.5	50		1*	0.5	10 @ 5	25K	70	1	± 5 to ± 15	General Purpose, Compensated (continued)	LM301A LM301A SN72301A	Siliconix Teledyne S TI
				0.8*	0.5*	10 @ 5	25K	70	1	± 5 to ± 15	Low Noise 301A	301ALN	Intersil
	8.0	50	20*	12*	20	10 @ 5	15K	74	0	± 10 to ± 20	High Slew Rate	AM-450 HA-2502 HA-2505	Datel † Harris Harris
				6*	20	10 @ 10	16K	74	0	± 8 to ± 20	Fast Slewing	3505J	Burr-Brown
	9.0	50	30*	8*	15*	10 @ 5	50K	74	1	± 10 to ± 20	Four Addressable Inputs Single Amplifier	HA-2405	Harris
	10.0	50	20*	20*	80	10 @ 5	7.5K	74	1	± 5 to ± 20	High Speed, Fast Setting	AD509J see page 624	AD
			25*	12*	40	10 @ 5	7.5K	74	0	± 10 to ± 20	High Slew Rate	HA-2512	† Harris
			20*	20*	80	10 @ 5	7.5K	74	1	± 10 to ± 20	80V/ μs Gain = 3	HA-2522	† Harris
			30*		80	10 @ 10	7K	74	1	± 8 to ± 20	Fast Slewing	3507J	Burr-Brown
			12*	40	10 @ 5	7.5K	74	0	± 10 to ± 20	High Slew Rate	HA-2515	Harris	
			12*	80	10 @ 5	7.5K	74	1	± 10 to ± 20	80V/ μs Gain = 3	AM-452 1009C HA-2525	Datel DDC Harris	
			20*	80	10 @ 10	7.5K	89*	1	± 8 to ± 20	High Slew Rate	1322 132201	Teledyne P † Teledyne P	
300	3.0	100	3*	1*	1.5*	13 @ 130	100K	70	0	± 5 to ± 18	0.2 amp Power	LH0041	† National
			10	1*	0.4*	10 @ 5	25K	70	3	± 5 to ± 18	High Gain	RM709	† Raytheon
			25	1*	1.5	11 @ 1100	100K	70	0	± 5 to ± 18	1.0 amp Power	LH0021	† National
	5.0	150	10*	7*	3.5	12 @ 6	25K	80	0	± 5 to ± 20	Low Noise	HA-909	† Harris
350	5.0	35	6.6*		2.7*	9 @ 18	16K	84	2	to ± 12	High Output Current	CA3033	† RCA
			—		2.7*	9 @ 18	16K	84	2	to ± 12	High Output Current	CA3047	RCA
400	3.0	30*	5	1*	1.2	10 @ 5	45K	90*	1	± 12 to ± 18	General Purpose	3051 3055	Burr-Brown Burr-Brown
500	3.0	60	5*	1*	34*	10 @ 10	50K	80	3	± 9 to ± 18	Fast General Purpose	133902	† Teledyne P
			—		4.2*		15K		2	to ± 18	High Slew Rate	ULS-2139	† Sprague
	75		3*	2*	4.2*	10 @ 10	50K	80	2	± 10 to ± 18	General Purpose	MC1539	† Motorola
	4.0	40*	10	0.9*	0.9	10 @ 5	45K	90*	1	± 12 to ± 18	General Purpose	3056	Burr-Brown
				1.0*	1.2	10 @ 10	45K	90*	1	± 12 to ± 18	General Purpose	3052	Burr-Brown
	5.0	200	3*	1*	0.5*	10 @ 5	50K	70	0	± 5 to ± 22	General Purpose Compensated	741M AD741 see page 625 $\mu\text{A}741\text{M}$ 741 ITT741-1 MC1741 LM741 (continued)	† AMD † AD † Fairchild † Intersil † ITT † Motorola † National

† Military Temperature Range (−55°C to 125°C) * — Typical Values

Arranged in order of increasing bias current, offset voltage, offset current, and voltage drift. "Comp" indicates number of compensation components required.

LINEAR—Operational Amplifiers - Characteristics (cont)

Master Selection Guide

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Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{V}/^\circ\text{C}$	Bandwidth MHz	Slew Rate v/ μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source
Single-Unit Package (cont)													
500	5.0	200	3*	1*	0.5*	10 @ 5	50K	70	0	± 5 to ± 22	General Purpose Compensated (continued)	CA741G see page 661	† RCA
												RM741	† Raytheon
												$\mu\text{A}741$	† Signetics
												SG741	† Silicon G
												741B	† Teledyne S
												SN52741	† TI
			3*	1*	0.5*	10 @ 5	50K	70	0	± 5 to ± 22	Low Noise 741	741LN	† Intersil
												CA6741	† RCA
			3*	1*	10	10 @ 5	50K	70	0	± 4 to ± 22	High Slew Rate 741	MC1741S	† Motorola
			3*	0.8*	5*	10 @ 5	50K	70	0	± 15	Wideband 741	SG1217	† Silicon G
			—	1*	0.7	10 @ 5	50K	70	0	± 5 to ± 18	High Speed 741	741MHS	† Intersil
			3*	1*	0.5*	10 @ 5	50K	70	0	± 5 to ± 20	Compensated 101	LH101	† National
												LH101	† Raytheon
												LH101	† Siliconix
			3*	1*	0.5*	10 @ 5	50K	70	1	± 5 to ± 20	General Purpose, Uncompensated	LM101	† AMD
												LM201	AMD
												$\mu\text{A}101$	† Fairchild
												LM101	† National
												CA101 see page 661	† RCA
												LM101	† Raytheon
												LM101	† Signetics
												SG101	† Silicon G
												LM101	† Siliconix
			3*	1*	0.5*	10 @ 5	50K	70	1	± 5 to ± 20	Uncompensated 741	748M	† AMD
												$\mu\text{A}748\text{M}$	† Fairchild
												MC1748	† Motorola
												LM748	† National
												LM748C	National
												CA748	† RCA
												RM748	† Raytheon
												$\mu\text{A}748$	† Signetics
												SG748	† Silicon G
												748B	† Teledyne S
												748C	Teledyne S
												SN52748	† TI
			3*	0.5*	0.3*	10 @ 5	25K	70	3	± 9 to ± 15	General Purpose	$\mu\text{A}709\text{M}$	† Fairchild
												ITT709-1	† ITT
												MC1709	† Motorola
												LM709	† National
												$\mu\text{A}709$	† Signetics
												709B	† Teledyne S
												SN52709	† TI
			—	0.5*	35	10 @ 5	50K	70	1	± 6 to ± 18	High Slew Rate	RM4531	† Raytheon
			—	1*	30*	10 @ 5	50K	70	1	± 5 to ± 18	High Slew Rate	NE531	Signetics

† Military Temperature Range (–55°C to 125°C) * — Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{v}/^\circ\text{C}$	Bandwidth MHz	Slew Rate v/ μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source									
Single-Unit Package (cont)																						
500	5.0	200	4*	30*	0.7*	to 100 ma	20K	70	2	to 24/ \pm 12 to 36/ \pm 18 to 44/ \pm 22	Programmable	CA3094	† RCA									
											Programmable	CA3094A	† RCA									
											Programmable	CA3094B	† RCA									
6.0	100	30	1*	1*	10 @ 1000	100K	70	0	\pm 5 to \pm 18	1.0 amp Power	LH0021C	National										
											200	—	1*	0.5*	10 @ 5*	20-50K	70	0	\pm 5 to \pm 18	General Purpose Compensated	AD741C see page 625	AD
												μ A741C	Fairchild									
												HA17741	Hitachi									
												741C	Intersil									
												ITT741-5	ITT									
												MC1741C	Motorola									
												LM741C	National									
												SF2741C	NPC									
												CA741CG see page 661	RCA									
												RC741	Raytheon									
												μ A741C	Signetics									
												SG741C	Silicon G									
												741C	Teledyne S									
												SN72741	TI									
			10*	1*	0.5*	10 @ 5	25K	70	0	\pm 5 to \pm 15	Low Noise 741	741CLN	Intersil									
			3*	1*	10	10 @ 5	20K	70	0	\pm 4 to \pm 18	High Slew Rate 741	MC1741SC	Motorola									
			5*	0.8*	5*	10 @ 5	20K	70	0	\pm 15	Wideband 741C	SG3217	Silicon G									
			—	1*	0.7	10 @ 5	25K	70	0	\pm 5 to \pm 18	High Speed 741	741CHS	Intersil									
			5*	1*	1	13 @ 130	100K	70	0	\pm 5 to \pm 18	0.2 amp Power	LH0041C	National									
			10*	1*	0.25	14 @ 47	100K	90	2	\pm 5 to \pm 18	High Gain, Instrumentation 50 ma Output	LH0020C	National									
			15*	0.2*	0.2*	11.5 @ 11.5	20K	70	0	\pm 5 to \pm 18	High Power	μ A791C	Fairchild									
			—	1*	0.5*	10 @ 5	20-50K	70	1	\pm 5 to \pm 18	General Purpose	748C	AMD									
												μ A748C	Fairchild									
												MC1748C	Motorola									
												SFC2748C	NPC									
												CA748C	RCA									
												RC748	Raytheon									
												μ A748C	Signetics									
												SG748C	Siliconix									
												SN72748	TI									
300	10*	7*	5*	11 @ 5.5	20K	74	0	\pm 5 to \pm 20	Low Noise	HA-911	Harris											
												10*	12*	50	12 @ 6	25K	70	0	\pm 5 to \pm 20	High Speed, Fast Settling	AD518J see page 624	AD
												—	15*	50	12 @ 6	25K	70	0	\pm 5 to \pm 20	Precision High Speed	LM318	AMD
												LM318	National									
												SFC2318	NPC									
600	6.0	60*	30	0.7*	0.6	10 @ 5	32K	90*	1	\pm 12 to \pm 18	General Purpose	3057	Burr-Brown									

† Military Temperature Range (—55°C to 125°C) * — Typical Values

Arranged in order of increasing bias current, offset voltage, offset current, and voltage drift. "Comp" indicates number of compensation components required.

LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{v}/^\circ\text{C}$	Bandwidth MHz	Slew Rate v/ μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source	
Single-Unit Package (cont)														
600	6.0	60*	30	0.9*	0.9	10 @ 10	45K	80*	1	± 12 to ± 18	General Purpose	3053	Burr-Brown	
	7.5	60	5*	1*	34*	10 @ 5	40K	80	3	± 9 to ± 18	Fast General Purpose	133901	Teledyne P	
	10.0	200	—	15*	50	12 @ 6	25K	70	2	± 5 to ± 18	Precision, High Speed	LM318	Raytheon	
750	5.0	250	6*	65*	15	10 @ 5	15K	74	3	± 6 to ± 18	High Speed High Gain	$\mu\text{A}715\text{M}$ 715	† Fairchild † AMD	
	10.0	50	5	5	5	10 @ 10	20K	80		± 8 to ± 22	Wideband	1317	† Teledyne P	
1000	7.5	100	12*	1*	34*	10 @ 5	15K	80	3	± 9 to ± 18	Fast General Purpose	1339	Teledyne P	
	150	3*	2*	4.2*	10 @ 5	15K	80	2	± 10 to ± 18	General Purpose	MC1439	Motorola		
1500	6.0	200	—	0.5*	35*	10 @ 5	20K	70	1	± 6 to ± 18	High Slew Rate	RC4531	Raytheon	
				1*	20*	10 @ 5	20K	70	1	± 5 to ± 22	High Slew Rate High Performance	SE531	† Signetics	
	7.5	250	6	65*	10	10 @ 5	10K	74	3	± 6 to ± 18	High Speed	715C $\mu\text{A}715\text{C}$	AMD Fairchild	
	500	6*	1*	0.5*	10 @ 5	20K	65	0	± 5 to ± 20	Compensated 201	LH201	National		
											LH201	Raytheon		
											LH201	Siliconix		
			1*	0.5*	10 @ 5	20K	65	1	± 5 to ± 20	General Purpose	LM301 $\mu\text{A}201\text{M}$ LM201	AMD Fairchild National		
											CA201 see page 661	RCA		
											LM201	Raytheon		
											LM201	Signetics		
											SG201	Silicon G		
											LM201	Siliconix		
			6-10*	1*	0.3*	10 @ 5	15K	65	3	± 9 to ± 15	General Purpose	$\mu\text{A}709\text{C}$ ITT709-5	Fairchild ITT	
											LM709C	National		
											RC709	Raytheon		
											$\mu\text{A}709\text{C}$	Signetics		
											709C	Teledyne S		
											SN72709	TI		
2000	3.0	200	4*	10*		10 @ 100	20K	70	0	± 5 to ± 20	General Purpose Wide Bandwidth	LH0003 LH0003C	† National National	
	5.0	400	—	38*	25*	9 @ 4.5	0.6K	76	1	± 7 to ± 18	Large Signal Wide-band	CA3100 see page 667	† RCA	
	7.5	100	—		4.2*		50K		2	to ± 18	High Slew Rate	ULN-2139	Sprague	
	10.0	100	2*	10*	5*	3.5 @ 0.5	1K	75	2	± 2 to ± 8	Differential Output	MC1520	† Motorola	
4000	2.0	1500	1.2*	15*	3*	22 @ 4.5*	0.7K	70	1	± 3 to ± 8	6 Volt, Wideband	CA3008A CA3010A CA3029A CA3037A	RCA † RCA RCA † RCA	
	15.0	200	2*	10*	5*	3.0 @ 0.43	0.75K	60	2	± 2 to ± 8	Differential Output	MC1420	Motorola	
	5000	2.0	500	2.5*	7*	1.5*	3.5 @ 0.35	2.5K	80	2	-3,6 to -6,12	Wideband	MC1712	† Motorola

† Military Temperature Range (-55°C to 125°C) * — Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{V}/^\circ\text{C}$	Bandwidth MHz	Slew Rate v/ μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source			
Single-Unit Package (cont)																
5000	2.0	500	10	30*	3.5*	3.5 @ 0.35	2.5K	80	3	-3,6 to -6,12	Wideband	$\mu\text{A}702\text{M}$ RM702 SN52702A	† Fairchild † Raytheon † TI			
6000	2.0	1600	1.2*	50*	7*	4.5 @ 9	2K	80	1	± 3 to ± 16	12 Volt, Wideband	CA3015A CA3016A CA3030A CA3038A	† RCA † RCA RCA † RCA			
7500	5.0	2000	5*	7*	1.5*	3.5 @ 0.35	2K	70	2	-3,6 to -6,12	Wideband	MC1712C	Motorola			
			20	30*	3.5*	3.5 @ 0.35	2K	70	3	-3,6 to -6,12	Wideband	$\mu\text{A}702\text{C}$ RC702	Fairchild Raytheon			
10000	5.0	2000	10*		1.7*	5 @ 0.05	1.4K	70	3	-3,6 to -6,12	General Purpose	SN52702 MC1530	† TI † Motorola			
12000	5.0	5000	1.2*	15*	3*	22 @ 4.5*	0.7K	70	1	± 3 to ± 8	6 Volt, Wideband	CA3008 CA3010 CA3029 CA3037	† RCA † RCA RCA † RCA			
			15000	10.0	5000	5*		1.7*	5 @ 0.05	1K	65	3	-3,6 to -6,12	General Purpose	SN72702	TI
			24000	5.0	5000	3.5*	50*	7*	4.5 @ 9	2K	80	1	± 3 to ± 16	12 Volt, Wideband	CA3015 CA3016 CA3030 CA3038	† RCA † RCA RCA † RCA
			30000	4.0	5000	20*	70*	400	12 @ 12	4K	60*	3	± 5 to ± 18	High Slew Rate	LH0024	† National
40000	8.0	15000	25*	70*	250	12 @ 12	3K	60*	3	± 5 to ± 18	High Slew Rate	LH0024C	National			
Dual-Unit Package																
0.02	20.0	0.0005*	75	1*	6*	10 @ 5	50K	70	0	± 5 to ± 18	FET Input Dual	1002M	† DDC			
												8043M	† Intersil			
0.05	50.0	0.0005*	75	1*	6*	10 @ 5	20K	70	0	± 5 to ± 18	FET Input Dual	1002C	DDC			
												8043C	Intersil			
2	0.5	0.2	15	1*	0.3*	13 @ 1.3	80K	96	1	± 5 to ± 20	Dual 108A	LH2108A	† National			
												LH2208A	National			
												LH2108A	† Signetics			
												LH2208A	Signetics			
	2.0	0.2	15	1*	0.3*	13 @ 1.3	50K	85	1	± 2 to ± 20	Dual 108	LH2108	† National			
												LH2208	National			
												LH2108	† Signetics			
												LH2208	Signetics			
3	0.5	2.8	2	1.2*	0.25*	10.5 @ 10.5	200K	114	0	to ± 22	Dual Matched Instrumentation	OP-10	† PMI			
												OP-10A	† PMI			
4	0.5	3.8	2	1.2*	0.25*	10.5 @ 10.5	200K	110	0	to ± 22	Dual Matched Instrumentation	OP-10E	PMI			
5	3.0	3	10*	25*	0.1*	10 @ 2	40K	80	0	± 1.2 to ± 18	Programmable	HA-2730	† Harris			
7	0.5	1	30	1*	0.3*	13 @ 1.3	80K	96	1	± 5 to ± 20	Dual 308A	LH2308A	National			

† Military Temperature Range (-55°C to 125°C) * — Typical Values

Arranged in order of increasing bias current, offset voltage, offset current, and voltage drift. "Comp" indicates number of compensation components required.

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LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{v}/^\circ\text{C}$	Bandwidth MHz	Slew Rate $\text{v}/\mu\text{s}$	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source
Dual-Unit Package (cont)													
7	1.3	6	4.5	1.2*	0.25*	12 @ 6	120K	100	0	to ± 22	Dual Matched Instrumentation	OP-10C	PMI
	7.5	1	30	1*	0.3*	13 @ 1.3	25K	80	1	± 2 to ± 18	Dual 308	LH2308	National
7.5	5.0	3	3*	1*	15*	12 @ 0.16	200K	70	0	± 1.2 to ± 18	Multi-Purpose Programmable	$\mu\text{A}776\text{M}$	† Fairchild
10	5.0	5	10*		0.1*	10 @ 2	25K	74	0	± 1.2 to ± 18	Programmable	HA-2735	Harris
	6.0	6	3*	1*	15*	12 @ 0.16	50K	70	0	± 1.2 to ± 18	Multi-Purpose Programmable	$\mu\text{A}776\text{C}$	Fairchild
15	3.0	5	—	.25*	0.16*	10 @ 1	100K	70	0	± 1 to ± 18	Programmable Dual LM4250	LH24250	† National
20	3.0	7.5	5*	0.27*	0.16*	11 @ 1.1	50K	70	0	± 1 to ± 18	Low Power Adjustable Current	8022M	† Intersil
30	6.0	10	5*	0.27*	0.16*	11 @ 1.1	50K	70	0	± 1 to ± 18	Low Power Adjustable Current	8022C	Intersil
	10	—	.25*	0.16*		10 @ 1	75K	70	0	± 1 to ± 18	Programmable Dual LM4250	LH24250C	National
50	2.0	5	—			10 @ 5	100K	80	1	± 5 to ± 20	Dual High Performance 741	SSS747 SSS747	† AMD † PMI
	25	5	1.5*	0.8		10 @ 10	100K*	100*		± 3 to ± 20	Matched Amplifier Pairs	3500MP	Burr-Brown
	3.0	5	—			10 @ 5	50K	80	0	± 5 to ± 20	Higher Performance	SSS747B	PMI
75	2.0	10	15	1*	0.5*	10 @ 5	50K	80	1	± 5 to ± 20	Dual LM101A High Performance	LH2101A LH2201A LH2101A LH2201A	† National National Signetics Signetics
80	3.0	30	15	0.44	0.3	10 @ 5	50K	80	0	± 5 to ± 22	Dual 741	$\mu\text{A}747\text{AM}$ $\mu\text{A}747\text{EC}$	† Fairchild Fairchild
100	3.0	30	8*	8*	2	13 @ 1.3	25K	80	0	± 2 to ± 20	High Slew Rate	HA-2650	† Harris
	5.0	25	—			10 @ 5	50K	70	0	± 5 to ± 20	Dual High Performance 741C	SSS747C SSS747C SSS747G SSS1458 SSS1558	AMD PMI † PMI PMI † PMI
	40	—	0.8*	0.5*		10 @ 1	4K	60	0	± 5 to ± 22	Low Power	SN52L022	† TI
200	5.0	60	8*	8*	2	13 @ 1.3	20K	74	0	± 2 to ± 20	High Slew Rate	HA-2655	Harris
	80	—	0.8*	0.5*		10 @ 1	1K	60	0	± 5 to ± 18	Low Power	SN72L022	TI
250	5.0	30		1*		10 ma	100K*	85*	0	3 to 30/ ± 1.5 to ± 15	Half LM124	LM158 SE532	† National † Signetics
	7.5	50	30	1*	0.5*	10 @ 5	25K	70	1	± 5 to ± 20	Dual High Performance	LH2301A	National
500	5.0	200	2-15*	1*	0.5*	10 @ 5	50K	70	0	± 5 to ± 22	Dual 741	747M XR1558 $\mu\text{A}747\text{M}$ $\mu\text{A}1558\text{M}$ MC1747 MC1558 LM747 LM1558 CA747G see page 661 (continued)	† AMD † Exar † Fairchild † Fairchild † Motorola † Motorola † National † National † RCA

† Military Temperature Range (—55°C to 125°C) * — Typical Values

Bold face indicates additional data is provided on the page noted.

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LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{v}/^\circ\text{C}$	Bandwidth MHz	Slew Rate v/ μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source
Dual-Unit Package (cont)													
500	5.0	200	2-15*	1*	0.5*	10 @ 5	50K	70	0	± 5 to ± 22	Dual 741 (continued)	CA1558G RM747 RM1558 $\mu\text{A}747$ SG747 SG1558 747B 1558 SN52747 SN52558	† RCA † Raytheon † Raytheon † Signetics † Silicon G † Silicon G † Teledyne S † Teledyne S † TI † TI
	6.0	200		1*	0.5*	10 @ 5	20-50K	70	0	± 5 to ± 18	Dual 741C	747C EX1458 $\mu\text{A}747\text{C}$ $\mu\text{A}1458\text{C}$ MC1747C LM747C LM1458 CA747CG CA1458G RC747 RC1458 $\mu\text{A}747\text{C}$ SG747C SG1458 747C 1458 SN72747 SN72558	AMD Exar Fairchild Fairchild Motorola National National RCA RCA Raytheon Raytheon Signetics Silicon G Silicon G Teledyne S Teledyne S TI TI
				3*	1*	10 @ 5	20K	70	0	± 3 to ± 18	Wideband 741	XR4558 RC4558 RC4558	Exar Raytheon TI
				3*	1*	10 @ 5	20K	70	0	± 3 to ± 18	Low Noise	XR4739 RC4739	Exar Raytheon
	7.0	50		1*		10 ma	100K*	85*	0	3 to 30/ ± 1.5 to ± 15	Half LM224	LM258 LM358 NE532	National National Signetics
700	10.0	300	6*	0.8*	0.3*	9 @ 4.5	20K	60	0	± 15	General Purpose	SG1458C	Silicon G
			15*	1.1*	0.8*	9 @ 4.5	20K	60	0	± 5 to ± 18	General Purpose	$\mu\text{A}1458\text{CC}$ MC1458C 1458C	Fairchild Motorola Teledyne S
1500	7.5	500	1.5*	1*	0.3*	10 @ 5	15K	65	3	± 9 to ± 18	Matched Dual 709	RC1437	Raytheon
				1*	0.25*	12 @ 1.2	15K	65	3	± 4 to ± 18	Matched Dual MC1709C	MC1437	Motorola
2000	6	1000	—		1*		6.5K	70	2	8 to 36/ ± 4 to ± 18	Single Supply	TBA231	SGS

† Military Temperature Range (–55°C to 125°C) * — Typical Values

Arranged in order of increasing bias current, offset voltage, offset current, and voltage drift. "Comp" indicates number of compensation components required.

LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{V}/^\circ\text{C}$	Bandwidth MHz	Slew Rate $\text{V}/\mu\text{s}$	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source
Triple-Unit Package													
30	3.0	7.5	5*	0.27*	0.16*	11 @ 1.1	50K	70	0	± 1 to ± 18	Low Power, Programmable	8023M	† Intersil
	6.0	10	5*	0.27*	0.16*	11 @ 1.1	50K	70	0	± 1 to ± 18	Low Power, Programmable	8023C	Intersil
50	20	25		0.5*		4vpp	4K	90*	0	6 to 450	Low input current amplifier of triple unit includes 5v regulator	ZN417	Ferranti
70	5.0	14		0.02*	0.1*	1.3 μa		70	0	to ± 18	Micropower, Transconductance Amplifier	CA3060B	† RCA
200	5.0	50	3.3*	0.6*	0.4*	10 @ 0.5	3K	80	0	± 1.5 to ± 15	Programmable	L144A	† Siliconix
												L144B	Siliconix
250	10.0	70	3.3*	0.6*	0.4*	10 @ 0.5	1K	70	0	± 1.5 to ± 15	Programmable	L144C	Siliconix
500	2.0	250	5*	10*		4vpp	4K	90*	0	6 to 450	Two amplifiers of Triple unit, includes 5v regulator	ZN417	Ferranti
550	5.0	100		0.045*	1*	15 μa		70	0	to ± 7	Micropower, Transconductance Amplifier	CA3060D	† RCA
5000	5.0	1000	0.11*	8*	0.15 ma			70	0	to ± 18	Micropower, Transconductance Amplifier	CA3060A	† RCA
												CA3060E	RCA
Quad-Unit Package													
100	5.0	25	1*	0.6*	10 @ 5	50K	70	0	± 5 to ± 22	Quad 741 with standard npn input stage		LM148	† Intersil
												LM248	Intersil
			LM148	† National									
			5*	3.5*	10 @ 5	50K	70	0	± 5 to ± 22	Wideband quad 741 for gains > 5	LM149	† National	
			40	0.8*	0.5*	10 @ 1	4K	60	0	± 2 to ± 22	Low Power	SN52L044	† TI
150	5.0	30	1*		10ma	50K	70	0	3 to 30/ ± 1.5 to ± 15	Single Supply; I/O Operates to ground		LM124	† Intersil
												LM124	† National
												LM124	† Raytheon
												CA124G	† RCA
												LM124	† Signetics
												SG124	† Silicon G
LM124	† Teledyne S												
LM124	† TI												
200	6.0	50	1*	0.6*	10 @ 5	25K	70	0	± 5 to ± 18	Quad 741 with standard npn input stage		LM348	Intersil
												LM348	National
			5*	3.5*	10 @ 5	25K	70	0	± 5 to ± 18	Wideband quad for gains > 5		LM349	National
			2.5*	0.5/20*	13.5 @ 2.6	1.2K		0	4 to 36	Current Mirror, Single Supply	$\mu\text{A}2900\text{C}$	Fairchild	
											$\mu\text{A}3900\text{C}$	Fairchild	
											LM2900	National	
											LM3900	National	
											LM2900	Raytheon	
											LM3900	Raytheon	
250	5.0	80	0.8	0.5*	10 @ 1	1K	60	0	± 2 to ± 18	Low Power	SN72L044	TI	

† Military Temperature Range (-55°C to 125°C) * — Typical Values

Bold face indicates additional data is provided on the page noted.

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LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{V}/^\circ\text{C}$	Bandwidth MHz	Slew Rate v/ μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments	Device	Source	
Quad-Unit Package (cont)														
250	7.0	50		1*		10ma	25K	65	0	3 to 30/ ± 1.5 to ± 15	Single Supply; I/O Operates to ground	XR324 LM234 LM334 MLM324 LM224 LM324 CA224G see page 661 CA324G see page 661 LM224 LM324 LM224 LM324 SG224 SG324 LM224 LM324 LM224 LM324	Exar Intersil Intersil Motorola National National RCA RCA Raytheon Raytheon Signetics Signetics Silicon G Silicon G Teledyne S Teledyne S TI TI	
300	5.0	30		1*	0.6	10 @ 5	50K	70	0	to ± 22	Quad 741	835B	† Teledyne S	
				1.5*	0.8	10 @ 5	50K	70	0	to ± 22	Quad 741	836B	† Teledyne S	
	—	—		4*	0.6*	3ma	1K		0	4 to 28	Current Mirror, Single Supply	μ A3301C MC3301 RC3301	Fairchild Motorola Raytheon	
				5*	0.6*	5ma	1K		0	5 to 18	Current Mirror, Single Supply	μ A3401C MC3401 CA3401G RC3401	Fairchild Motorola † RCA Raytheon	
400	4.0	50		5*	2.5*	1.3*	20ma	325K*	100*	0	± 3 to ± 18	Quad 741	HA-4741	Harris
				1*	1.2	10 @ 5	50K	70	0	3 to 36/ ± 1.5 to ± 18	LM124 with improved output	RM3503A see page 649	† Raytheon	
500	5.0	50		10*	1*	0.6*	10 @ 5	50K	70	0	3 to 36/ ± 1.5 to ± 18	Single Supply; I/O Operates to ground	XR3503 μ A3503M MC3503 RM3503 see page 649	† Exar † Fairchild † Motorola † Raytheon
				—	2	1.6	10 @ 5	20K	70	0	to ± 22	Quad 741	XR4212M see page 639	† Exar
					1.5*	10 @ 3	5K	70	0	± 1.5 to ± 18	Programmable Quad 741	XR4202	Exar	
			200		2	1.5*	10 @ 5	50K	70	0	± 3 to ± 18	Quad 741, High Gain	XR4136M see page 640 RM4136 see page 647 RM4136	† Exar † Raytheon † TI

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† Military Temperature Range (−55°C to 125°C) * — Typical Values

Arranged in order of increasing bias current, offset voltage, offset current, and voltage drift. "Comp" indicates number of compensation components required.

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LINEAR—Operational Amplifiers - Characteristics (cont)

Bias Current na.(25°C)	Offset Voltage mv(25°C)	Offset Current na.(25°C)	Voltage Drift $\mu\text{v}/^\circ\text{C}$	Bandwidth MHz	Slew Rate v/ μs	Output v @ ma	Voltage Gain v/v	CMRR db	Comp.	Supply Range	Comments -	Device	Source
Quad-Unit Package (cont)													
500	6.0	50		1*	1.2*	20ma	25K	70	0	3 to 36/ ± 1.5 to ± 18	LM324 with improved output	RC3403A see page 649 RV3403A	Raytheon Raytheon
				—	2	1.6	10 @ 5	5K	70	0 to ± 18	Quad 741	XR4212C see page 639	Exar
	100			1*	0.6*	10 @ 5	25K	70	0	to ± 18	Quad 741	835C	Teledyne S
	200			3*	1*	10 @ 5	20K	70	0	± 3 to ± 18	Quad 741	XR4136C see page 640 RC4136 see page 647 RC4136	Exar Raytheon † TI
	7.0	50				20ma	100K*	85*	0	3 to 32/ ± 1.5 to ± 16	Extended Temp LM224	MLM2902 LM2902 2902	Motorola Raytheon Teledyne S
	8.0	50	10*	1*	0.6*	10 @ 5	20K	70	0	3 to 36/ ± 1.5 to ± 18	Single Supply: I/O Operates to ground	XR3403 $\mu\text{A}3403\text{C}$ MC3403 RC3403 see page 649	Exar Fairchild Motorola Raytheon
	75	10*	1*	0.6*	10 @ 5	20K	20K	70	0	3 to 36/ ± 1.5 to ± 18	Supply: I/O Operates to ground	XR3303 $\mu\text{A}3303\text{C}$ MC3303	Exar Fairchild Motorola
	100			1.5*	1*	10 @ 5	25K	70	0	to ± 18	Quad 741	836C	Teledyne S
	10.0	50	10*	1*	0.6*	10 @ 5	20K	70	0	3 to 36/ ± 1.5 to ± 18	Single Supply; I/O Operates to ground	XR3403 3403 MC3403 RC3403 see page 649	Exar Fairchild Motorola Raytheon
	10.0	50	—	1*		20ma	100K*	85*	0	3 to 26/ ± 1.5 to ± 13	Single Supply; I/O Operates to ground	LM2902 LM2902	National TI
				1*	2*	20ma	15K	70	0	3 to 32/ ± 1.5 to ± 16	LM224 with improved output	RV3403A	Raytheon
600	10.0	300		3*	1*	10 @ 5	15K	60	0	± 3 to ± 18	Quad 741	RC4136C RC41363	Raytheon TI

† Military Temperature Range (—55°C to 125°C) * — Typical Values

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Linear—Phase Locked Loop, Telecommunication, Timers

Function	Device	Source	Function	Device	Source
Phase Locked Loop Circuits			Phase Locked Loop Circuits (cont)		
Note: Stereo Decoders are not listed			Two Modulus Prescaler ($\div 6/7$)	SP8741	Plessey
Counter Logic Control	SP8790	Plessey	Two Modulus Prescaler ($\div 8/9$)	SP8742	Plessey
Counter Control Logic (Use with MC12012 for high frequency programming)	MC12014	Motorola	Dual Tone Decoder	XR2567 XR2567C	† Exar Exar
Crystal Oscillator (0.1 to 2.0 MHz)	MC12060 MC12560	Motorola † Motorola	Tone Generator	FX205	CMA
Crystal Oscillator (2 to 20 MHz)	MC12061 MC12561	Motorola † Motorola	Two Modulus Prescaler ($\div 5/9, 10/11, 10/12$)	MC12012 MC12512	Motorola † Motorola
Current Controlled Oscillator and Phase Comparator	HA-2820 HA-2825	† Harris Harris	Two Modulus Prescaler ($\div 10/11$)	11C90C 11C90M 95H90C 95H90M MC12013 MC12513	Fairchild † Fairchild Fairchild † Fairchild Motorola † Motorola
Digital Mixer	MC12000	Motorola		SP8640 SP8641 SP8642 SP8643 SP8685 SP8690A SP8690B SP8695	Plessey Plessey Plessey Plessey Plessey Plessey Plessey Plessey
FSK Modulator/Demodulator	XR210 XR2211 see page 635 XR2211C see page 635	Exar † Exar Exar	Two Modulus Prescaler ($\div 248/256$)	11C83	Fairchild
Offset Control System (for synthesizer tuned transceivers)	MC12020 MC12021 MC12520 MC12521	Motorola Motorola † Motorola Motorola	VCO	11C58C MC1648 MC1658 SP1648 SP1658 SN54LS324 SN74LS324	Fairchild Motorola Motorola Plessey Plessey † TI TI
Phase-Frequency Detector	11C44C 11C44M MC4044 MC4344 MC12040 MC12540	Fairchild Fairchild Motorola † Motorola Motorola † Motorola	VCO—Function Generator	LM566 LM566C NE566 SE566	National † National Signetics † Signetics
Phase Locked Loop	XR215	Exar	VCO and Phase Comparator	XR2207 see page 632 XR2207C see page 632 LM565 LM565C NE560B NE561B NE562B NE565 SE565 TA7133	Exar Exar Exar National † National Signetics Signetics Signetics † Signetics Toshiba
Phase Locked Loop (CMOS)	F4046C F4046M MC14046A MC14046C CD4046A see page 375 CD4046AE see page 375 SCL4046A SCL4046AE SCL4446	Fairchild † Fairchild † Motorola Motorola † RCA RCA † SSS SSS SSS	VCO—Waveform Generator	1453C XR205 XR2206 see page 630 XR2206C 1453M 8038C 8038M LS8038C LS8038M	DDC Exar † Exar Exar † DDC Intersil † Intersil Lithic Sys † Lithic Sys
Tone Decoder	XR567 XR567C XR2211 see page 635 XR2211C see page 635 LM567 LM567C NE567 SE567	† Exar Exar † Exar Exar † National National Signetics † Signetics			
Two Modulus Prescaler ($\div 5/6$)	11C91C 11C91M 91H91C 91H91M SP8740	Fairchild † Fairchild Fairchild † Fairchild Plessey			

† Military Temperature Range (–55°C to 125°C) * — Typical Values

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Linear—Phase Locked Loop, Telecommunication, Timers (cont)

Function	Device	Source
Phase Locked Loop Circuits (cont)		
VCO, Amplifier, Analog Multiplier	XRS200 XR205	Exar Exar
VCO, Phase Comparator, Multiplier	SL651	† Plessey
VCO, Phase Comparator Multiplier, with Auxiliary Amplifier	SL650	† Plessey
Dual VCO	11C24C MC4024 MC4324 SN54LS124 SN54S124 SN74LS124 SN74S124	Fairchild Motorola † Motorola † TI † TI TI TI

Title	Function	Device	Source
Telecommunication Circuits			
Baseband Modulator/Demodulator	50db carrier suppression	SL1001	Plessey
Baseband channel Amplifier	24-27db amplifier	SL1020	Plessey
Coin box Circuit	Coin recognition for pay telephones	AY5-9300	GI
Comander (Signal Compressor/Expander)		XR2216	Exar
Push Button Telephone Dialer Circuit	Converts push button inputs to pulses.	CRC8000 AY5-9100 MP9100	Collins GI Plessey
Binary to Pulse Train Converter		MC14408 MC14409	Motorola Motorola
Repertory Dialer	Stores ten telephone numbers.	AY5-9200 MP9200	GI Plessey
Tone Decoder	Three tone (8 combinations) sequential code receiver	FX307	CMA
Tone Decoder	Operates from 0.01 Hz to 500 kHz	XR567 XR567C XR2211 see page 635 XR2211C see page 635 LM567 LM567C NE567 SE567	† Exar Exar † Exar Exar † National National Signetics † Signetics
Dual Tone Decoder	Operates from 0.01 Hz to 500 K Hz.	XR2567	Exar
Dual Tone Decoder		CRC8030	Collins
Relay Driver	For 48v Telephone relays	DS1686 DS1687 DS3686 DS3687	† National † National National National
Encoder (2 of 8 keyboard to Binary Encoder)	4 x 4 Key Input to 4 line output	MC14419	Motorola
Tone Encoder	Accepts 2 of 8 code (4 x 4 Key input), synthesizes 2 freq.	MK5085 MK5086 MC14410	Mostek Mostek Motorola

Title	Function	Device	Source
Telecommunication Circuits (cont)			
Bandpass Filter	Touchtone filters	882	† Beckman
Dual Tone Generator			
Generates 12-16 tone pairs		AY3-9400 AY3-9410 AY5-9500	GI GI GI
Modem	Frequency-Shift Keying Modulator/Demodulator—600 bps	MC14412	Motorola
Modem	For Serial Communications at up to 600 bps	MC6860	Motorola
Digital Filter Switch	Tone Decoder	FX105	CMA
Frequency Sensitive Switch	Provides two set points adjustable with external components.	FX101	CMA
Frequency Sensitive switch	Provides set points with widely adjustable hysteresis	FX305	CMA
Frequency Sensitive Switch	Provides two set points and three state outputs	FX401	CMA
Tone Operated Switch	Bistable tone operated switch	FX501	CMA
Tone Operated Monostable Timer	Tone operated for remote switching	FX601	CMA
Tone Transmitter	Three tone sequential code transmitter	FX207	CMA
Tone Transceiver	Decodes and encodes 5 sequential tones	FX407 FX507	CMA CMA
Tone Transceiver	Single tone transmitter-receiver -simplex.	FX107	CMA
Cross Point Array	Double 4 x 4 switch matrix	RC4444 see page 659, 660 RM4444 see page 659, 660	Raytheon Raytheon

Function	Device	Source
Timers		
Timer	NE555 SE555 XR555C NE555 NE555 SE555 LS555N LS555S MC1455 MC1555 LM555C LM555M CA555G see page 661 CA555CG see page 661 RC555 RM555 NE555 SE555 SG555 SG555C SN52555 SN72555	† AMD AMD Exar Fairchild Intersil † Intersil Lithic Sys † Lithic Sys Motorola † Motorola National † National † RCA RCA Raytheon † Raytheon Signetics † Signetics † Silicon G Silicon G † TI TI

Master Selection Guide

LINEAR

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Military Temperature Range (−55°C to 125°C)

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Linear—Phase Locked Loop, Telecommunication, Timers (cont)

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Function	Device	Source
Timers (cont)		
Timer, Internal Current Source	XR320	Exar
Timer, Low Power (supply 3v)	SN76812	TI
Timer, Precision	LM122 LM222 LM322 LM2905 LM3905	† National National National National National
Timer, Programmable (includes a counter for long time delays) Binary Control	XR2240C see page 637 XR2240M see page 637 2240 ZN1034E 8240 MC14541A MC14541C	Exar † Exar Fairchild Ferranti Intersil † Motorola Motorola
Timer, Programmable (includes counter) Decimal Control	XR2250C see page 637 XR2250M see page 637 8250	Exar † Exar Intersil
Timer, Programmable (includes counter) Hours/Minutes/Seconds Control	8260	Intersil
Dual Timer (dual 555)	NE556 SE556 XR556C XR556M NE556 NE556 SE556 LM556 RC556 RM556 556 NE556 SE556 SG556 SG556C	AMD † AMD Exar † Exar Fairchild Intersil † Intersil National Raytheon † Raytheon Teledyne S Signetics † Signetics † Silicon G Silicon G
Dual Timer (dual 555), pinout variations	XR2556C XR2556M LS555-2 D555	Exar † Exar Lithic Sys Teledyne S
Dual Monostable Timer	FX109	CMA
Quad Timer, Current Sink Output	NE553 SE553	Signetics † Signetics
Quad Timer, Current Source Output	NE554 SE554	Signetics † Signetics
Tone Triggered Timer	FX601	CMA

† Military Temperature Range (–55°C to 125°C)

ABBREVIATIONS OF COMPANY NAMES

AD	Analog Devices	Motorola	Motorola Semiconductor
AMD	Advanced Micro Devices	National	National Semiconductor
AMI	American Microsystems, Inc.	NCR	National Cash Register, Microelectronics Div.
AMS	Advanced Memory Systems	NEC	NEC Microcomputers
Analogic	Analogic Corp.	Nippon	Nippon Electric Co.
Beckman	Beckman Instruments, Helipot Division	Nitron	Nitron
Burr-Brown	Burr-Brown Research	Nortec	Nortec Electronics
Cermetek	Cermetek	NPC	Nucleonic Products Co.
CMA	Consumer Microcircuits of America	OKI	OKI Electronics of America, Inc.
Collins	Collins Radio	Panasonic	Panasonic, Matsushita Electric Corp.
Datel	Datel Systems	Plessey	Plessey Semiconductors
DDC	ILC Data Devices Corp.	PMC	Power Monolithics Co.
EA	Electronic Arrays	PMI	Precision Monolithics, Inc.
EMM/Semi	EMM Semi, Div. of Electronic Memories & Magnetics	Ragen	Ragen Semiconductor
Exar	Exar Integrated Systems	Raytheon	Raytheon Semiconductor
Fairchild	Fairchild Semiconductor	RCA	RCA Solid State Division
Ferranti	Ferranti Electric	Reticon	Reticon
GI	General Instrument	Rockwell	Rockwell International, Microelectronic Div.
Harris	Harris Semiconductor	Sanken	Sanken Electric
Hitachi	Hitachi America, Ltd.	SGS	SGS-ATES Semiconductor
Hughes	Hughes Aircraft Co., MOS Division	Signetics	Signetics
Hybrid Sys.	Hybrid Systems	Silicon G	Silicon General
IMI	International Microcircuits, Inc.	Siliconix	Siliconix
Intech	Intech	SMC	SMC Microsystems Corp.
Intel	Intel	Solitron	Solitron Devices
Interdesign	Interdesign	Sprague	Sprague Electric Company
Intersil	Intersil	SSS	Solid State Scientific
IPI	Integrated Photomatrix, Inc.	SW	Stewart-Warner Microcircuits
ITT	ITT Semiconductors	Synertek	Synertek
Lithic Sys.	Lithic Systems	Teledyne C	Teledyne Crystalonics
Litronix	Litronix	Teledyne P	Teledyne Philbrick
LSI Comp.	LSI Computer Systems	Teledyne S	Teledyne Semiconductor
Micro Net	Micro Networks	TI	Texas Instruments
Micropac	Micropac Industries	TMX	TMX, Inc.
Micro Power	Micro Power Systems	Toshiba	Toshiba
Mitsubishi	Mitsubishi International	TRW	TRW
MMI	Monolithic Memories, Inc.	Transitron	Transitron Electronics
MOS	MOS Technology	Western	Western Digital
Mostek	Mostek		

LINEAR—Voltage Regulators

Output Voltage	Output Current	Device	Source
Fixed, Positive			
2.6	100 ma	μ A78L26C 78L02C see page 673	Fairchild Signetics
5	100 ma	μ A78L05C LM3910-05 LM78L05C 78L05C see page 673 78L05C	Fairchild National National Signetics TI
	200 ma	MLM109G MLM209G MLM309G LM109H LM209H LM309H LM342-5 SFC2109 SFC2209 SFC2309 SL78L05 LM109H LM209H LM309H LM109DB LM209DB LM309DB SG109T SG209T SG309T SG705T SG705T SN52109 SN72309	Motorola Motorola Motorola † National National National National † NPC NPC NPC Plessey † Raytheon Raytheon Raytheon † Signetics Signetics Signetics † Silicon G Silicon G Silicon G † Silicon G Silicon G † TI TI
500 ma	500 ma	805V5 μ A78M05C μ A78M05M MC7705C MC78M05C LM341-5 78M05 78M05C	† Beckman Fairchild † Fairchild Motorola Motorola National † Signetics Signetics
	600 ma	L005T1	SGS
	750 ma	809V5	† Beckman
	850 ma	L129	SGS
	1 a	μ A109M μ A209M μ A309C μ A7805C μ A7805M MLM109 MLM209K MLM309 MC7805 LM109K LM209K LM309K LM340-5 LM7805 SFC2109M LM109K LM209K LM309K 7805 see page 668 (continued)	† Fairchild Fairchild Fairchild Fairchild † Fairchild † Motorola Motorola Motorola Motorola † National National National National National NPC † Raytheon Raytheon Raytheon † Signetics

Output Voltage	Output Current	Device	Source	
Fixed, Positive (cont)				
5 (continued)	1 a	7805C see page 668 LM109DA LM209DA LM309DA LM340-5 SG109K SG209K SG309K SG7805K SG7805KC 7805C	Signetics † Signetics Signetics Signetics † Silicon G Silicon G Silicon G † Silicon G Silicon G TI	
	1.5 a	PMC15K-5	PMC	
	3 a	SH0323 PMC14J-5 PMC14K-5 SI3554 LM123 LM223 LM323	Fairchild PMC PMC Sanken † National National National	
	5 a	μ A78H05 42050-055	Fairchild Micropac	
	10 a	42050-510	Micropac	
	6	100 ma	78L06C LM3910-06	National National
		200 ma	PC521 LM342-6 SL78L06 SG7806T SG7806TC	† GI National Plessey † Silicon G Silicon G
	500 ma	500 ma	805V6 μ A78M06C μ A78M06M MC7706C MC78M06 LM341-6	† Beckman Fairchild † Fairchild Motorola Motorola National
		750 ma	809V6	† Beckman
	1 a	1 a	μ A7806C μ A7806M MC7806C LM340-6 LM7806 SG7806KC SG7806K 7806 see page 668 7806C see page 668 LM340-6	Fairchild † Fairchild Motorola National National Silicon G † Silicon G † Signetics Signetics Signetics
1.5 a		PMC15K-6	PMC	
3 a		PMC14K-6	PMC	
10 a		42050-610	Micropac	
6.2		100 ma	78L62C 78L06C see page 673 78L06C	Fairchild Signetics TI
7	10 a	7806C	TI	
8	100 ma	42050-710	Micropac	
78L08C	100 ma	μ A78L08C LM3910-08 LM78L08C 78L08C see page 673	Fairchild National National Signetics	

† Military Temperature Range (−55°C to 125°C)

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LINEAR—Voltage Regulators (cont)

Output Voltage	Output Current	Device	Source
Fixed, Positive (cont)			
8	200 ma	LM342-8	National
		SL78L08	Plessey
	500 ma	SG7808T	† Silicon G
		SG7808TC	Silicon G
		μA78M08C	Fairchild
		μA78M08M	† Fairchild
	1 a	MC7708C	Motorola
			MC78M08
		LM341-8	National
		μA7808C	Fairchild
μA7808M			† Fairchild
MC7808C		Motorola	
		LM340-8	National
LM7808		National	
7808		† Signetics	
7808C		† Signetics	
see page 668			
LM340-8	Signetics		
SG7808KC	Silicon G		
SG7808K	† Silicon G		
1.5 a	PMC15K-8	PMC	
3 a	PMC14J-8	PMC	
	PMC14K-8	PMC	
10 a	42050-810	Micropac	
9	500 ma	801V9	† Beckman
	750 ma	809V9	† Beckman
10	100 ma	78L10C	National
		LM3910-10	National
	200 ma	LM342-10	National
	1.5 a	PMC15K-10	PMC
	3 a	PMC14J-10	PMC
		PMC14K-10	PMC
9 a	42050-109	Micropac	
12	50 ma	829B	† Teledyne S
		829C	Teledyne S
	100 ma	μA78L12C	Fairchild
		LM3910-12	National
		LM78L12C	National
		78L12C	† Signetics
	see page 673		
	78L12C	TI	
	200 ma	PC501	† GI
		LM342-12	National
SL78L12		Plessey	
SG7812TC		Silicon G	
500 ma	SG7812T	† Silicon G	
	801V12	† Beckman	
	μA78M12C	Fairchild	
	μA78M12M	† Fairchild	
	MC7712C	Motorola	
	MC78M12	Motorola	
LM341-12	National		
L036T1	SGS		
720 ma	L130	SGS	
750 ma	809V12	† Beckman	
1 a	μA7812C	Fairchild	
		μA7812M	† Fairchild
	MC7812C	Motorola	
	LM340-12	National	
	LM7812	National	
	SJ3120E	Sanken	
	(continued)		

Output Voltage	Output Current	Device	Source
Fixed, Positive (cont)			
(continued) 12	1 a	7812	† Signetics
		see page 668	
	7812C	† Signetics	
		see page 668	
	LM340-12	Signetics	
		SG7812K	† Silicon G
		SG7812KC	Silicon G
		7812C	TI
	1.5 a	PMC15K-12	PMC
	3 a	PMC14J-12	PMC
PMC14K-12		PMC	
8 a	42050-128	Micropac	
14	8 a	42050-148	Micropac
15	400 μa	L037T1	SGS
	50 ma	830B	† Teledyne S
830C		Teledyne S	
100 ma	μA78L15C	Fairchild	
	LM3910-15	National	
	LM78L15C	National	
	78L15C	† Signetics	
see page 673			
78L15C	TI		
200 ma	LM342-15	National	
	SL7815	Plessey	
	SG7815TC	Silicon G	
	SG7815T	† Silicon G	
500 ma	801V15	† Beckman	
	μA78M15C	Fairchild	
	μA78M15M	† Fairchild	
	MC7715C	Motorola	
	MC78M15C	Motorola	
	LM341-15	National	
600 ma	L131	SGS	
750 ma	809V15	† Beckman	
1 a	μA7815C	Fairchild	
	μA7815M	† Fairchild	
	MC7815C	Motorola	
	LM340-15	National	
	LM7815	National	
	SJ3150E	Sanken	
7815	† Signetics		
see page 668			
7815C	† Signetics		
see page 668			
LM340-15	Signetics		
SG7815KC	Silicon G		
SG7815K	† Silicon G		
7815C	TI		
1.5 a	PMC15K-15	PMC	
3 a	PMC14J-15	PMC	
	PMC14K-15	PMC	
8 a	42050-158	Micropac	
16	8 a	42050-168	Micropac
18	100 ma	LM3910-18	National
	LM78L18C	National	
200 ma	LM342-18	National	
	SL78L18	Plessey	
	SG7818TG	Silicon G	
SG7818T	† Silicon G		
500 ma	801V18	† Beckman	
	MC7718C	Motorola	
	MC78M18C	Motorola	
	(continued)		

† Military Temperature Range (–55°C to 125°C)

Regulator Sections: Fixed—Positive, Negative, Dual; Adjustable—Positive, Negative, Dual

LINEAR—Voltage Regulators (cont)

Master Selection Guide

Output Voltage	Output Current	Device	Source
Fixed, Positive (cont)			
18 (continued)	500 ma	LM341-18	National
	750 ma	809V18	† Beckman
	1 a	μA7818C	Fairchild
		μA7818M	† Fairchild
		MC7818C	Motorola
		LM340-18	National
		LM7818	National
	7818	† Signetics see page 668	
	7818C	Signetics see page 668	
	SG7818KC	Silicon G	
SG7818K	† Silicon G		
1.5 a	PMC15K-18	PMC	
3 a	PMC14J-18	PMC	
	PMC14K-18	PMC	
8 a	42050-188	Micropac	
20	200 ma	SL78L20	Plessey
	500 ma	μA78M20C	Fairchild
		μA78M20M	† Fairchild
		MC7720C	Motorola
		MC7820C	Motorola
78M20C	Signetics		
1.5 a	PMC15K-20	PMC	
3 a	PMC14J-20	PMC	
	PMC14K-20	PMC	
8 a	42050-208	Micropac	
21	500 ma	809V21	† Beckman
	750 ma	809V21	† Beckman
22	4 a	42050-224	Micropac
24	100 ma	LM3910-24	National
		LM78L24C	National
	200 ma	NC512	† GI
		PC502	† GI
		PC512	† GI
		LM342-24	National
		SL78L24	Plessey
	SG7824T	† Silicon G	
	SG7824TC	Silicon G	
	500 ma	803V24	† Beckman
		μA78M24C	Fairchild
		μA78M24M	† Fairchild
		MC7724C	Motorola
		MC78M24C	Motorola
	LM341-24	National	
78M24C	Signetics		
750 ma	809V24	† Beckman	
1 a	μA7824C	Fairchild	
	μA7824M	† Fairchild	
	MC7824C	Motorola	
	LM340-24	National	
	LM7824	National	
	SI3240E	Sanken	
	7824	† Signetics see page 668	
	7824C	Signetics see page 668	
	LM340-24	Signetics	
	SG7824K	† Silicon G	
SG7824KC	Silicon G		

Output Voltage	Output Current	Device	Source
Fixed, Positive (cont)			
24	1.5 a	PMC15K-24	PMC
	3 a	PMC14J-24	PMC
		PMC14K-24	PMC
4 a	42050-244	Micropac	
	26	4 a	42050-264
28	500 ma	803V28	† Beckman
	750 ma	809V28	† Beckman
	1.5 a	PMC15K-28	PMC
3 a	PMC14J-28	PMC	
	PMC14K-28	PMC	
4 a	42050-284	Micropac	
	30	200 ma	SL78L30
4 a	42050-304	Micropac	
	32	Shunt Reg.	AN155
500 ma	803V32	† Beckman	
	4 a	42050-324	Micropac
34	4 a	42050-344	Micropac
36	4 a	42050-364	Micropac
Fixed, Negative			
2	1 a	MC7902C	Motorola
	1.5 a	PMC18K-2	PMC
	2 a	79E02	† Fairchild
79E02C	† Fairchild		
4	1 a	MC7904C	Motorola
5	500 ma	855V5	† Beckman
		μA79M05C	Fairchild
		LM120H05	† National
		LM220H05	National
		LM320H05	National
	SG120-05T	† Silicon G	
	SG220-05T	Silicon G	
	SG320-05T	Silicon G	
	750 ma	859V5	† Beckman
	1 a	μA7905C	Fairchild
MC7905C	Motorola		
1.5 a	LM120K05	† National	
	LM220K05	National	
	LM320K05	National	
	LM320T05	National	
	PMC18K-5	PMC	
SG120-05K	† Silicon G		
SG220-05K	Silicon G		
SG320-05K	Silicon G		
2 a	79E05	† Fairchild	
	79E05C	† Fairchild	
3 a	LM145K5.0	† National	
	LM245K5.0	National	
LM345K5.0	National		
5 a	42051-055	Micropac	
5.2	500 ma	LM120H5.2	† National
		LM220H5.2	National
		LM320H5.2	National
	LM320M5.2	National	
	1 a	MC7905.2C	Motorola
1.5 a	LM120K5.2	† National	
	LM220K5.2	National	
	LM320K5.2	National	
LM320T05	National		
(continued)			

† Military Temperature Range (−55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

LINEAR—Voltage Regulators (cont)

Output Voltage	Output Current	Device	Source	
Fixed, Negative (cont)				
5.2 (continued)	1.5 a	PMC18K-5.2	PMC	
	3 a	LM145K5.2 LM245K5.2 LM345K5.2	† National National National	
6	200 ma	PC523	GI	
	500 ma	855V6 μA79M06C LM120H06 LM220H06 LM320H06 LM320M06	† Beckman Fairchild † National National National National	
	750 ma	859V6	† Beckman	
	1 a	μA7906C MC7906C	Fairchild Motorola	
	1.5 a	LM120K06 LM220K06 LM320K06 LM320T06 PMC18K-6	† National National National National PMC	
	5 a	42051-065	Micropac	
	7	5 a	42051-075	Micropac
8	500 ma	μA79M08C LM120H08 LM220H08 LM320H08 LM320M08	Fairchild † National National National National	
	1 a	μA7908C MC7908C	Fairchild Motorola	
	1.5 a	LM120K08 LM220K08 LM320K08 LM320T08 PMC18K-8	† National National National National PMC	
	5 a	42051-085	Micropac	
9	500 ma	851V9	† Beckman	
	750 ma	859V12	† Beckman	
	1.5 a	42051-095	Micropac	
10	1.5 a	PMC18K-10	PMC	
	5 a	42051-105	Micropac	
12	200 ma	PC503 LM120H12 LM220H12 LM320H12 SG120-12T SG220-12T SG320-12T	† GI † National National National † Silicon G Silicon G Silicon G	
	500 ma	851V12 μA79M12C	† Beckman Fairchild	
	750 ma	859V12	† Beckman	
	1 a	μA7912C MC7912C LM120K12 LM220K12 LM320K12 LM320T12 SG120-12K SG220-12K SG320-12K	Fairchild Motorola † National National National National † Silicon G Silicon G Silicon G	
	1.5 a	PMC18K-12	PMC	

Output Voltage	Output Current	Device	Source	
Fixed, Negative (cont)				
12	4 a	42051-124	Micropac	
14	4 a	42051-144	Micropac	
15	200 ma	LM120H15 LM220H15 LM320H15 LM320M15 SG120-15T SG220-15T SG320-15T	† National National National National † Silicon G Silicon G Silicon G	
	500 ma	851V15 μA79M15C	† Beckman Fairchild	
	750 ma	859V15	† Beckman	
	1 a	μA7915C MC7915C LM120K15 LM220K15 LM320K15 LM320T15 SG120-15K SG220-15K SG320-15K	Fairchild Motorola † National National National National † Silicon G Silicon G Silicon G	
	1.5 a	PMC18K-15	PMC	
	4 a	42051-154	Micropac	
	16	4 a	42051-164	Micropac
	18	200 ma	LM120H18 LM220H18 LM320H18	† National National National
		500 ma	851V18 LM320M18	† Beckman National
		750 ma	859V18	† Beckman
1 a		μA7918C MC7918C LM120K18 LM220K18 LM320K18 LM320T18	Fairchild Motorola † National National National National	
1.5 a		PMC18K-18	PMC	
20	500 ma	42051-184	Micropac	
	4 a	42051-204	Micropac	
	500 ma	μA79M20C	Fairchild	
21	1.5 a	PMC18K-20	PMC	
	3 a	42051-204	Micropac	
22	500 ma	851V21	† Beckman	
	750 ma	859V21	† Beckman	
24	3 a	42051-223	Micropac	
24	200 ma	PC514 LM120H24 LM220H24 LM320H24	GI † National National National	
	500 ma	853V24 μA79M24C LM320M24	† Beckman Fairchild National	
	1 a	μA7924C MC7924C LM120K24 LM220K24 LM320K24 LM320T24	Fairchild Motorola † National National National National	
	1.5 a	PMC18K-24	PMC	
	3 a	42051-243	Micropac	

† Military Temperature Range (−55°C to 125°C)

Regulator Sections: Fixed—Positive, Negative, Dual; Adjustable—Positive, Negative, Dual

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LINEAR—Voltage Regulators (cont)

Output Voltage	Output Current	Device	Source	
Fixed, Negative (cont)				
26	3 a	42051-263	Micropac	
27	500 ma	853V27	† Beckman	
	750 ma	859V27	† Beckman	
28	500 ma	853V28	† Beckman	
	750 ma	859V28	† Beckman	
	1.5 a	PMC18K-28	PMC	
	3 a	MIVR42051-283	Micropac	
30	3 a	42051-303	Micropac	
32	Shunt Reg.	AN155	Panasonic	
	500 ma	853V32	† Beckman	
	3 a	42051-323	Micropac	
34	3 a	42051-343	Micropac	
36	3 a	42051-363	Micropac	
Fixed, Dual				
±6	5 a	MIVR42051	Micropac	
±12	100 ma	LM126 LM226 LM326	† National National National	
	300 ma	843-V-12 844-V-12 844V-12	Beckman † Beckman † Beckman	
	300 ma	843V-12	Beckman	
-12.5	100 ma	LM127 LM227 LM327	† National National National	
	±15	100 ma	XR1468	Exar
			XR1568	† Exar
MC1468			Motorola	
MC1568			† Motorola	
LM125			† National	
LM225			National	
LM325			National	
RC4195			Raytheon	
see page 657, 658				
RM4195			† Raytheon	
see page 657				
SG1468	Silicon G			
SG1568	† Silicon G			
SG1501	† Silicon G			
SG2501	Silicon G			
SG3501	Silicon G			
SG4501	Silicon G			
200 ma	200 ma	SG1501A	† Silicon G	
		SG2501A	Silicon G	
		SG3501A	Silicon G	
300 ma	300 ma	843V-15	† Beckman	
		844V-15	† Beckman	

† Military Temperature Range (-55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

LINEAR—Voltage Regulators

Output Voltage Hi	Output Voltage Low	Output Current	Device	Source		
Adjustable, Positive						
7	1	50 ma	NC520	† GI		
		200 ma	NC521	† GI		
9	3	500 ma	806	† Beckman		
16	4	150 ma	NC109T	GI		
17	2.5	200 ma	MC1460G MC1560G	Motorola † Motorola		
		500 ma	MC1460R MC1560R	Motorola † Motorola		
19	4.1	200 ma	MFC4063A	Motorola		
			MFC4064A	Motorola		
			MFC6033A	Motorola		
			MFC6034A	Motorola		
20	2	20 ma	LM300	Intersil		
			LM300	National		
			SFC2300	NPC		
	10	800 ma	SG300	Silicon G		
			NC562	† GI		
21	9	500 ma	802	† Beckman		
26	1.8	12 ma	CA3085	† RCA		
30	4.5	12 ma	LM305	AMD		
			μA305C	Fairchild		
			305	Intersil		
			MLM305	Motorola		
			LM305	National		
			LM305	Raytheon		
			SG305	Silicon G		
			SN72305	TI		
			2	20 ma	100	† Intersil
					200	Intersil
		LM100	† National			
		LM200	National			
		SFC2100	† NPC			
		SFC2200	NPC			
		SG100	† Silicon G			
		SG200	Silicon G			
5	500 ma	μA78MG	Fairchild			
32	2.5	200 ma	MC1469G	Motorola		
			MC1461G	Motorola		
		500 ma	MC1461R MC1469R	Motorola Motorola		
20	500 ma	804	† Beckman			
35	4.1	200 ma	MFC4060A	Motorola		
			MFC4062A	Motorola		
			MFC6030A	Motorola		
			MFC6032A	Motorola		
2	4 a	MPC1000	Motorola			
36	1.7	100 ma	CA3085A	† RCA		
37	3	2 ma	NE550A	Signetics		
		50 ma	SE550	† Signetics		
2	150 ma	723	† AMD			
		723C	AMD			
		μA723C	Fairchild			
		μA723M	† Fairchild			
		HA17723	Hitachi			
		723	† Intersil			
		723C	Intersil			
		MC1723	† Motorola			
		MC1723C	Motorola			
		LM723	† National			
		LM723C	National			
		SFC2723C	† NPC			
		(continued)				

Output Voltage Hi	Output Voltage Low	Output Current	Device	Source
Adjustable, Positive (cont)				
37 (continued)	2	150 ma	SFC2723EC	NPC
			CA723	† RCA
			CA723C	RCA
			RC723	Raytheon
			RM723	† Raytheon
			μA723	† Signetics
			μA723C	Signetics
			SG723	† Silicon G
			SG723C	Silicon G
			723BE	† Teledyne S
	2.5	200 ma	MC1561G	† Motorola
			MC1569G	† Motorola
		500 ma	MC1561R	† Motorola
			MC1569R	† Motorola
	5	25 ma	μA376C	Fairchild
			LM376N	National
			LM376	Teledyne S
			SN72376	TI
38	8	250 ma	NC501	† GI
			NC530	† GI
			NC531	† GI
			NC511	† GI
			PC511	† GI
	12	625 ma	NC581	† GI
			13	250 ma
40	4.5	12 ma	LM105	AMD
			LM205	AMD
			μA105M	† Fairchild
			105	† Intersil
			205	Intersil
			MLM105	† Motorola
			MLM205	Motorola
			LM105	† National
			LM205	National
			SFC2105	† NPC
		45 ma	SFC2205	NPC
			LM105	† Raytheon
			LM205	Raytheon
			SG105	† Silicon G
			SG205	† Silicon G
			LM105	† Teledyne S
			LM205	Teledyne S
			SN52105	† TI
			LM305A	AMD
			μA305AC	Fairchild
305A	Intersil			
LM305A	National			
SFC2305	NPC			
SG305A	Silicon G			
LM305A	Raytheon			
LM305A	Teledyne S			
SN72305A	TI			
2	50 ma	NE550	Signetics	
3	50 ma	822BE	† Teledyne S	
2	150 ma	SE550L	† Signetics	
		823AE	† Teledyne S	
46	1.7	100 ma	CA3085B	† RCA
1000	0	100 ma	MC1466	Motorola
			MC1566	† Motorola

Master Selection Guide

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† Military Temperature Range (−55°C to 125°C)

Regulator Sections: Fixed—Positive, Negative, Dual; Adjustable—Positive, Negative, Dual

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LINEAR—Voltage Regulators (cont)

Output Voltage		Output Current	Device	Source	Output Voltage		Output Current	Device	Source
Hi	Low				Hi	Low			
Adjustable, Negative					Adjustable, Dual (cont)				
7	1	200 ma	N523	† GI	±37	±20	150 ma	RC4194TK see page 655	Raytheon
9	3	500 ma	856	† Beckman	±42	±.05	100 ma	RX4194M RM4194D see page 655	† Exar † Raytheon
21	9	500 ma	852	† Beckman			200 ma	XR4194MK RM4194TK see page 655	† Exar † Raytheon
30	.035	20 ma	LM304 MLM304G LM304 LM304 LM304	Fairchild Motorola National Raytheon Teledyne S					
	.015	20 ma	SN72304	TI					
	2.2	500 ma	79MG	Fairchild					
	4	5 a	MPC900	Motorola					
32	3.8	200 ma	MC1463G MC1463R	Motorola Motorola					
		500 ma	MC1463R	Motorola					
	20	500 ma	854	† Beckman					
37	3.6	200 ma	MC1563G	† Motorola					
		500 ma	MC1563R	† Motorola					
38	8	250 ma	NC503 NC513 PC513	GI GI GI					
	12	625 ma	NC583	† GI					
40	.015	20 ma	μA104HM LM104H LM204H SFC2104 SFC2204 LM104 LM204 LM104H LM204H	† Fairchild † National National † NPC NPC † Raytheon Raytheon † Teledyne S Teledyne S					
		20 ma	MLM104G MLM204G SN52104	† Motorola Motorola † TI					
Adjustable, Dual									
20	8	100 ma	XR1468 XR1568 MC1468L MC1568L SG1468J SG1568J	Exar † Exar Motorola † Motorola Silicon G † Silicon G					
	±14.5	100 ma	MC1568R MC1468R SG1468T SG1568T	† Motorola Motorola Silicon G † Silicon G					
±23	8	200 ma	SG3501A SG1501A SG2501A	Silicon G † Silicon G Silicon G					
	±10	100 ma	SG1501 SG2501 SG3501 SG4501 SG3502 SG1502 SG2502	† Silicon G Silicon G Silicon G Silicon G Silicon G † Silicon G Silicon G					
±32	±.05	100 ma	XR4194CN RC4194D see page 655	Exar Raytheon					
		200 ma	XR4194CK RC4194TK see page 655	Exar Raytheon					

† Military Temperature Range (−55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

LINEAR—Other Devices

Function	Device	Source
Other Linear Devices		
AC Amplifier, Quad, Single Supply	CA3048	RCA
AC Detector (Detects presence or absence of ac signals, includes adjustable threshold and time delay.)	3050	Intech
Active Filters	881 UAF21 UAF21H UAF25 UAF25H UAF31 8681	Beckman Burr-Brown † Burr-Brown Burr-Brown † Burr-Brown Burr-Brown DDC
Alarm Circuits, Triple Alert/Alarm (Each circuit has two inputs, when the first one is low an open collector LED driver is turned on. When the second one is low independent of the first the output is flashed at an adjustable rate).	3020	Intech
Alarm Circuits, Temperature	3030	Intech
Alarm Circuits, Tone Alarm (Comparator with ac output)	3010	Intech
Amplifiers—See Linear firing SCRs or operating relays)	ULN-2301	Sprague
Amplifier-SCR firing Circuit	ULN-2300	Sprague
Analog-Digital Control Circuit (Wide bandwidth op amp and high speed, dual threshold comparator)	MC1407 MC1507	Motorola † Motorola
Analog Shift Register, 130x2, with storage (See also Serial Analog Delay, Bucket Brigade below)	CCD311	Fairchild
Balanced Modulator/Demodulator	μA796C LS1496 LS1596 MC1496 MC1596 LM1496 LM1596 SL640C SL641C SL1001A SL1001B SL1496 SL1596 N5596 S5596 SG1496 SG1596	Fairchild Lithic Sys † Lithic Sys Motorola † Motorola National † National Plessey Plessey Plessey Plessey Plessey Plessey † Plessey Signetics † Signetics Silicon G Silicon G
Ring Modulator, four transistor	SL355	Plessey
Blowout Resistant Transistor (simulates 40 v transistor with special protection)	LM195 LM295 LM395	† National National National
Bucket Brigade Device (Special/Dual 512 stage, acts as a variable delay line in the audio frequency range)	MN3001 MN3002	Panasonic Panasonic
Crystal Oscillators	SP705 SL680	Plessey Plessey
Comparators, Programmable with Memory (High/Low Comparator)	CA3098 CA3099	† RCA † RCA
Customized Arrays (Linear and Digital circuits, customized in final metalization)	XR-CHIP EX-IIL-CHIP (continued)	Exar Exar

Function	Device	Source
Other Linear Devices (cont)		
Customized Arrays (Linear and Digital circuits, customized in final metalization) (continued)	ULA MONOCHIP ECL-ARRAY IIL-ARRAY RTL-ARRAY	Ferranti Interdesign Plessey Plessey Plessey
DC to DC Converter (2.5 to 12 v input; Output determined by external transformer)		
Dual Transistors, Monolithic, Matched, See Linear Array Section		
DVM Circuits—See Interface-Analog to Digital Converters, also Digital-Special		
Flasher (LED)	LP1000 LM3909	Lithic Sys National
Frequency/Tone Operated Devices—See Telecommunication Circuits		
Frequency to Voltage/Voltage to Frequency Converter	A8400 A8400	Intech † Intech
Hall Effect Devices (Sense magnetic field) See also Digital—Other Digital Devices	DN831 ULN-3008 ULN-3100	Panasonic Sprague Sprague
Image Sensor, 256 x 1, CCD	CCD110	Fairchild
Image Sensor, 500 x 1, CCD	CCD101	Fairchild
Image Sensor, 1728x1, CCD	CCD121	Fairchild
Image Sensor, Linear Self Scanning	IPL7050 IPL7064 IPL7100 IPL7128 IPL7256 M128 M256 M512 M768 M1024 RL16 RL64 RL128 RL256 RL512 RL936 RL1024 RL1872	IPI IPI IPI IPI IPI IPI IPI IPI IPI Reticon Reticon Reticon Reticon Reticon Reticon Reticon Reticon
Image Area Sensor, Self Scanning	RA32X32 RA50X50 RA100X100	Reticon Reticon Reticon
Image Area Sensor, Circular, Self Scanning	RO64	Reticon
Image Area Sensor, 100 x 100, CCD	CCD201	Fairchild
Level Detector, Precision (with internal reference)	SN72560	TI
Level Detector, Precision Dual	SN72D560	TI
Light to Frequency Converter	IPL13	IPI
Light Detector (with buffer amplifier)	IPL16 CA3062	IPI RCA

† Military Temperature Range (-55°C to 125°C)

Regulator Sections: Fixed—Positive, Negative, Dual; Adjustable—Positive, Negative, Dual

IC UPDATE MASTER

LINEAR—Other Devices (cont)

Function	Device	Source	Function	Device	Source
Other Linear Devices (cont)			Other Linear Devices (cont)		
Light Activated Switch	IPL15 IPL17 PS12 PS24	IPI IPI IPI IPI	PIN Diode Switch Driver	DH0035 DH0035C	† National National
Low Battery Indicator, triggers on 3dv (for use with 3 NiCd cells)	ICM7201	Intersil	Power Supply Control (Oscillator with variable mark/ space for switching supplies)	SL442	Plessey
Multipliers	AD532J AD532K AD532S XR2208 see page 634 8013C 8013M LS1495 LS1595 MC1494 MC1594 MC1495 MC1595 SL1495 SL1595 CD8091 SG1402 SG2402 SG3402 SG1495 SG1595	AD AD † AD Exar Intersil † Intersil Lithic Sys † Lithic Sys Motorola † Motorola Motorola † Motorola Plessey † Plessey † RCA † Silicon G Silicon G Silicon G Silicon G † Silicon G	Pressure Transducers	SH4207 LX1400 LX1600 LX1700 LX3700 LX3800	Fairchild National National National National National
Multipliers/Dividers	AD530J AD530K AD530L AD530S AD533J AD533K AD533L AD533S 4201J 4203J 4203K 4203S 4204J 4204K 4205J 4205K 4205S 1401	AD AD AD † AD AD AD AD † AD Burr-Brown Burr-Brown Burr-Brown † Burr-Brown Burr-Brown Burr-Brown Burr-Brown Burr-Brown † Burr-Brown † DDC	Radio Transmitter	LP2000 LP2001	Lithic Sys Lithic Sys
Multifunction Convertors (XY/Z) ^m	AD531J AD531K AD531L AD531S 4301 4302	AD AD AD † AD Burr-Brown Burr-Brown	Voltage Reference Diode (two terminal active circuit) 1.220v ± 5%	LM113 LM313	† National National
Motor Speed Regulator (for small dc motors)	SL440 TCA900 TCA910	Plessey SGS SGS	Voltage Reference, 2.5v	AD580	† AD
			Voltage Reference Source, 6.9v temperature stabilized	LM199 LM299 LM399	† National National National
			Voltage Reference Source, 10v	AD2700J/K/L AD2700S/T/U MN2000 MN2001 MN2002 MN2003	AD AD † Micro Net Micro Net Micro Net Micro Net
			Voltage Reference Source, ± 10v	MN2004 MN2005	Micro Net Micro Net
			Voltage Reference, Adjustable 2.5 to 33v	SN72499	TI
			Regulator Diode (two terminal active circuit) 1.8 to 5.6v	LM103	† National
			RMS to DC Converter	4340 4341	Burr-Brown Burr-Brown
			Sample and Hold Circuits	AD582 AD583 SHC23 SHC23ET SHC80 SHC85 SH85ET SHM-IC-1 1502 HA-2420 HA-2425 IH5110 IH5111 MN343 LH0023 LH0023C LH0043 LH0043C LH0053 LH0053C SHM6401 (continued)	AD AD Burr-Brown † Burr-Brown Burr-Brown Burr-Brown Burr-Brown Datel DDC Harris † Harris † Intersil † Intersil † Micro Net † National National † National National † National National National

† Military Temperature Range (−55°C to 125°C)

Bold face indicates additional data is provided on the page noted.

LINEAR—Other Devices (cont)

Function	Device	Source
Other Linear Devices (cont)		
Sample and Hold Circuits (continued)	4856	Teledyne P
SCR/TRIAC Control (Burst Control)	L121	SGS
SCR/TRIAC Control (Phase Control)	SL440 L121	Plessey SGS
Serial Analog Delay (Analog storage units with read in/read out shift register) (See also Analog Shift Registers, Bucket Brigade above)	SAD-100 SAD512 SAD-1024	Reticon Reticon Reticon
Serial Analog Memory (Analog storage with independent read-in and read-out shift registers)	SAM64 SAM128	Reticon Reticon
Serial Analog Processor (Analog storage with versatile input and output shift registers)	SAP-128	Reticon
Sinewave Generator	FX205	CMA
Square Law Device (two quadrant)	SL645	Plessey
Thermal Converter (matched transistors, differential resistors)	4131	Burr-Brown
Temperature Controlled Differential Pair	ITT726-1 ITT726-5 μ A726C μ A726M	† ITT ITT Fairchild † Fairchild
Temperature Transducers	LM3911 LX5600 LX5700	National † National † National
Dual Voltage Level Alarm (activated if either input differs by more than ± 5 to $\pm 25\%$ of selected value)	3041	Intech
Quad Voltage Level Monitor /Alarm (activated if any of 4 inputs differs by more than ± 5 , ± 10 or $\pm 20\%$ of selected value)	3040	Intech
Voltage to Frequency Converter	RC4151 see page 653 RM4151 see page 653 RV4151	Raytheon † Raytheon Raytheon
Voltage to Frequency/Frequency to Voltage Converter	A8400 A8900	Intech † Intech
Zero Voltage Switches	XR742 742C MFC8070 SL447 SL448 SL449 CA3058 CA3059 CA3079 SN72440	Exar Fairchild Motorola Plessey Plessey † Plessey RCA RCA RCA TI

† Military Temperature Range (–55°C to 125°C)

Regulator Sections: Fixed—Positive, Negative, Dual; Adjustable—Positive, Negative, Dual

FET INPUT IC OP AMPS

Analog Devices provides the broadest range of IC FET-INPUT OP AMPS in the industry. For use in applications where low bias current and high input impedance are imperative, ADS FET-input amplifiers are available in versions where low offset

voltage, speed, low noise, ultra-low bias current or cost are also design considerations. The newest addition to the ADS FET-INPUT OP AMP line is the AD515. With bias current as low as 75fA and offset voltage below 1.0mV, the AD515 represents the ultimate in FET amplifier design.

Type No	Temp Range	I _b pA	V _{OS} mV	$\Delta V_{OS}/\Delta T$ $\mu V/^\circ C$	V _{DIFF} @ Rated I _B $\pm V$	Gain	V _{OUT} $\pm V$ @ mA	CMRR dB	Frequency Unity Gain MHz	Response Slew Rate V/ μsec	Price (100's) (\$)	Package
AD503J	C	15	50	75	4.0(T)	20k	10/5	70	1.0(T)	3.0	11.40	H
AD503K	C	10	20	25	4.0(T)	50k	10/5	80	1.0(T)	3.0	16.00	H
AD503S	M	10	20	50	4.0(T)	50k	10/5	80	1.0(T)	3.0	20.00	H
AD506J	C	15	3.5	75	44.0(T)	20k	10/5	70	1.0(T)	3.0	9.50	H
AD506K	C	10	1.5	25	4.0(T)	50k	10/5	80	1.0(T)	3.0	11.00	H
AD506L	C	5	1.0	10	4.0(T)	75k	10/5	80	1.0(T)	3.0	16.00	H
AD506S	M	10	1.5	50	4.0(T)	50k	10/5	80	1.0(T)	3.0	17.60	H
AD515J	C	.300	3.0	50	20	40k	10/5	66	.35(T)	0.3	9.90	H
AD515K	C	.150	1.0	15	20	100k	10/5	80	.35(T)	0.3	14.00	H
AD515L	C	.075	1.0	25	20	50k	10/5	70	.35(T)	0.3	18.00	H
AD514J	C	50	50	75	20	20k	10/5	70	.75	0.5	5.90	H
AD514K	C	20	20	25	20	50k	10/5	70	.75	0.5	7.90	H
AD514L	C	10	20	25	20	50k	10/5	70	.75	0.5	9.90	H
AD514S	M	20	20	50	20	50k	10/5	70	.75	0.5	11.90	H
AD523J	C	1.0	50	90	4.0(T)	20k	10/5	70	0.5(T)	3.0	14.00	H
AD523K	C	0.5	20	30	4.0(T)	40k	10/5	80	0.5(T)	3.0	16.75	H
AD523L	C	0.25	20	60	4.0(T)	40k	10/5	80	0.5(T)	3.0	18.75	H
AD528J	C	30	3	50	20(T)	25k	10/5	70	10(T)	50	12.00	H
AD528K	C	15	1	25	20(T)	50k	10/5	80	10(T)	50	16.00	H
AD528S	M	15	1	25	20(T)	50k	10/5	80	10(T)	50	28.00	H
AD540J	C	50	50	75	20(T)	20k	10/5	70	1.0(T)	6.0(T)	4.45	H
AD540K	C	25	20	25	20(T)	50k	10/5	70	1.0(T)	6.0(T)	5.95	H
AD540S	M	25	20	50	20(T)	50k	10/5	70	1.0(T)	6.0(T)	9.95	H

FAST WIDEBAND IC OP AMPS

High Speed Op Amps are those characterized by wide bandwidth (>4MHz), high slew rate (>20V/micro second) and

low settling time. The devices listed below offer the user a variety of AC specifications for any applications including 8, 10 and 12-bit converters.

Type No	Temp Range	Gain	V _{OUT} $\pm V$ @ mA	Unity Gain MHz	Slew Rate V/ μsec	Settling Time μsec to 0.1%	V _{OS} mV	$\Delta V_{OS}/\Delta T$ $\mu V/^\circ C$	I _b nA	I _{OS} nA	CMRR dB	Price (100's) (\$)	Package
AD507J	C	80k	10/5	35(T)	20	0.9(T)	5.0	15(T)	25	25	25	6.95	H
AD507K	C	100k	10/5	35(T)	25	0.9(T)	3.0	15	15	15	80	10.00	H
AD507S	M	100k	10/5	35(T)	20	0.9(T)	4.0	20	15	15	80	15.00	H
AD509J	C	7.5k	10/5	20	80	0.2(T)	10.0	20	250	50	74	8.95	H
AD509K	C	10k	10/5	20	80	0.5(T)	8.0	30	200	25	80	12.50	H
AD509S	M	10k	10/5	20	100	0.5(T)	8.0	30	200	25	80	19.75	H
AD518J	C	25k	10/5	12	50	0.8(T)	10.0	10	500	200	70	1.95	H
AD518K	C	50k	10/5	12	50	0.8(T)	4.0	15	250	50	80	4.95	H
AD518S	M	50k	10/5	12	50	0.8(T)	4.0	20	250	50	80	11.95	H

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HIGH ACCURACY IC OP AMPS

Where low offset voltage, low drift, low noise and long term stability are paramount, Analog Devices provides a line of HIGH ACCURACY OP AMPS

at extremely low costs. As well as high performance versions of the popular 741 and 301 type amplifiers, ADS offers high accuracy devices with offset voltage laser-trimmed to 25 μ V max, drift below 25 μ V/ $^{\circ}$ C and voltage noise of 1 μ V p-p, such as the new AD510.

Type No	Temp Range	Gain	V _{OUT} ±V @ mA	V _{OS} mV	Δ V _{OS} / Δ T μ V/ $^{\circ}$ C	I _b nA	I _{OS} nA	CMRR dB	Noise μ V p-p (0.01 to 10Hz)	Frequency Response		Price (100's) (\$)	Package
										Unity Gain MHz	Slew Rate V/ μ sec		
AD301A1	C	80k	10/5	0.5	5.0	30	5.0	90	3.0(T)	1.0 to 8.0(T)*	0.5 to 10(T)*	6.00	H,N
AD504J	C	250k	10/5	2.5	5.0	200	40	94	1.0(T)	0.3 to 1.0(T)*	0.12 to 2.5(T)*	8.40	H
AD504K	C	500k	10/5	1.5	3.0	100	15	100	1.0(T)	0.3 to 1.0(T)*	0.12 to 2.5(T)*	15.30	H
AD504L	C	1000k	10/5	0.5	1.0	80	10	110	1.0(T)	0.3 to 1.0(T)*	0.12 to 2.5(T)*	20.40	H
AD504M	C	1000k	10/5	0.5	0.5	80	10	110	0.6**	0.3 to 1.0(T)*	0.12 to 2.5(T)*	22.00	H
AD504S	M	1000k	10/5	0.5	1.0	80	10	110	1.0(T)	0.3 to 1.0(T)*	0.12(T)*	24.00	H
AD508J	C	250k	10/5	2.5	3.0	25	5.0	94	1.0(T)	0.3 to 1.0(T)*	0.12 to 2.5(T)*	14.00	H
AD510J	C	250k	10/5	.100	3.0	25	5	94	1.0(T)	0.3(T)	0.10(T)	5.95	H
AD510K	C	1000k	10/5	.050	1.0	13	4	110	1.0(T)	0.3(T)	0.10(T)	9.95	H
AD510L	C	1000k	10/5	.025	0.5	10	2.5	110	1.0(T)	0.3(T)	0.10(T)	14.95	H
AD510S	C	1000k	10/5	.050	1.0	13	4	110	1.0(T)	0.3(T)	0.10(T)	24.50	H
AD741J	C	50k	10/10	3.0	20	200	50	80	3.0(T)	1.0(T)	0.5(T)	1.25	H,N
AD741K	C	50k	10/5	2.0	15	75	10	90	3.0(T)	1.0(T)	0.5(T)	2.25	H,N
AD741L	C	50k	10/5	0.5	5.0	50	5	90	3.0(T)	1.0(T)	0.5(T)	6.00	H,N
AD741S	M	50k	10/10	2.0	15	75	10	80	3.0(T)	1.0(T)	0.5(T)	3.30	H

*Parameter range with various external compensation schemes.

**100% tested and guaranteed from 0.1 to 10Hz.

GENERAL PURPOSE IC OP AMPS

Where only moderate performance is required, a good *General Purpose Op Amp* is the best price/performance choice. Analog

Devices provides the popular 741, 301 and 308 type devices with performance and reliability a cut above the standard general purpose op amp.

Type No	Temp Range	Gain	V _{OUT} ±V @ mA	Frequency Response		V _{OS} mV	Δ V _{OS} / Δ T μ V/ $^{\circ}$ C	I _b nA	I _{OS} nA	CMRR dB	Noise μ V p-p (0.01 to 10Hz)	Price (100's) (\$)	Package
				Unity Gain MHz	Slew Rate V/ μ sec								
AD101A	M	50k	10/5	1.0 to 8.0(T)	0.5 to 10(T)	2.0	15	75	10	80	3.0(T)	2.25	H
AD201A	I	50k	10/5	1.0 to 8.0(T)	0.5 to 10(T)	2.0	15	75	10	80	3.0(T)	1.75	H,N
AD301A	I	25k	10/5	1.0 to 8.0(T)	0.5 to 10(T)	7.5	30	250	50	70	3.0(T)	1.00	H,N
AD108	M	50k	13/1.3	0.3 to 3.0(T)	0.3 to 1.3(T)	2.0	15	2.0	0.2	85	2.0(T)	12.50	H
AD208	I	50k	13/1.3	0.3 to 3.0(T)	0.3 to 1.3(T)	2.0	15	2.0	0.2	85	2.0(T)	4.75	H
AD308	I	25k	13/1.3	0.3 to 3.0(T)	0.3 to 1.3(T)	7.5	30	7.0	1.0	80	2.0(T)	3.50	H
AD108A	M	80k	13/1.3	0.3 to 3.0(T)	0.3 to 1.3(T)	0.5	5.0	2.0	0.2	96	2.0(T)	17.50	H
AD208A	I	80k	13/1.3	0.3 to 3.0(T)	0.3 to 1.3(T)	0.5	5.0	2.0	0.2	96	2.0(T)	14.00	H
AD308A	I	80k	13/1.3	0.3 to 3.0(T)	0.3 to 1.3(T)	0.5	5.0	7.0	1.0	96	2.0(T)	7.00	H
AD502J	I	20k	10/5	1.0(T)	0.5(T)	6.0	40	25	12	80	15(T)	3.85	H
AD502K	I	20k	10/5	1.0(T)	0.5(T)	5.0	20	7	4	80	15(T)	7.75	H
AD502L	I	20k	10/5	1.0(T)	0.5(T)	5.0	10	4	1	80	15(T)	16.15	H
AD502S	M	20k	10/5	1.0(T)	0.5(T)	5.0	20	10	5	80	15(T)	12.85	H
AD741	M	50k	10/5	1.0(T)	0.5(T)	5.0	-	500	200	70	3.0(T)	2.00	H,N
AD741C	I	20k	10/5	1.0(T)	0.5(T)	6.0	-	500	200	70	3.0(T)	1.00	H,N

Specifications are min and max values unless specified as typical (T)

Package Designation: H - TO-99 can
N - 8 pin mini DIP

AD530, AD531, AD532, AD533

Analog Devices is the industry's leading supplier of Analog Functional Circuits. Utilizing the patented Gilbert Linearized Transconductance Technique, ADS has developed a line of low cost, monolithic circuits with multiplying, dividing, squaring and square rooting functions. The laser trimmed AD532 is the most recent development; it requires no external pots or adjustments making it the easiest-to-use device on the market.

The Analog Devices AD530 is the industry's first integrated circuit multiplier to include the transconductance multiplying element, stable reference, and output amplifier on a monolithic silicon chip. The AD530 multiplies in four (4) quadrants with a transfer function of $XY/10$, divides in two (2) quadrants with $10Z/X$ transfer function, and square roots in one (1) quadrant with a transfer function of $-\sqrt{10Z}$.

The AD531 is the first monolithic programmable multiplier/divider to provide the true transfer function $V_X \cdot V_Y/kI_Z$ without the need for an external level shifting op amp at the output. Not just a multiplier, the AD531 is truly a computation circuit that is ideally suited to such applications as automatic gain control (AGC), true RMS-to-DC conversion, ratio determination and vector operations; in addition, it provides the normal mathematical functions of four-quadrant multiplication, two-quadrant division and squaring, and square rooting. Flexibility of operation is achieved by means of the variable scale factor kI_Z , which can be set by an external resistor or varied dynamically by an externally derived reference current to obtain the overall transfer function $V_X \cdot V_Y/V_Z$.

SPECIFICATIONS (typical @ $V_S = \pm 15V$ and $T_A = +25^\circ C$ unless otherwise noted)

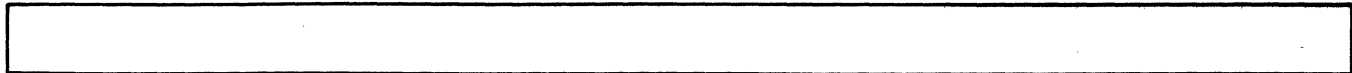
Models	530J (530K) (530L) (530S)	531J (531K) (531L) (531S)	532J (532K) (532S)
Full Scale Accuracy	2% (1%) (0.5%) (1%)	2% (1%) (0.5%) (1%)	2% (1%) (1%)
Divides and Square Roots	YES	YES	YES
Multiplication Characteristics			
Output Function	$XY/10$	XY/I_{REF}	$(X_1 - X_2)(Y_1 - Y_2)/10$
Accuracy vs. Temperature (\pm)	0.06(0.03)(0.01)(0.02 max)%/ $^\circ C$	0.06(0.03)(0.01)(0.02 max)%/ $^\circ C$	0.06(0.03)(0.02)%/ $^\circ C$
Accuracy vs. Supply (\pm)	0.2%/%	0.2%/%	0.2%/%
Output Offset (\pm)			
Initial	Adj. to zero	Adj. to zero	$\pm 50mV$ max($\pm 20mV$ max)($\pm 20mV$ max)
Average vs. Temperature 0 to $+70^\circ C$	0.2mV/ $^\circ C$	0.2mV/ $^\circ C$	0.7(0.7)(2.0 max)mV/ $^\circ C$
Scale Factor (\pm)	Fixed	Dynamically Variable	Fixed
Initial Error	Adj. to 1%(0.5%)(0.2%)(0.5%)	Adj. to 1%(0.5%)(0.2%)(0.5%)	Adj. to 1%(0.5%)(0.5%)
Nonlinearity (\pm)			
X Input (X = 20V p-p, Y = $\pm 10VDC$)	0.8%(0.5%)(0.3%)(0.5%)	0.8%(0.5%)(0.3%)(0.5%) ⁽¹⁾	0.8%(0.5%)(0.5%)
Y Input (Y = 20V p-p, X = $\pm 10VDC$)	0.3%(0.2%)(0.2%)(0.2%)	0.3%(0.2%)(0.2%)(0.2%) ⁽¹⁾	0.3%(0.2%)(0.2%)
Feedthrough			
X = 0, Y = 20V p-p 50Hz	—	—	150mV(100mV)(100mV)p-p max
with external trim	100mV(60mV)(30mV)(60mV)p-p max	150mV(80mV)(40mV)(80mV)p-p max ⁽¹⁾	—
Y = 0, X = 20V p-p 50Hz	—	—	200mV(100mV)(100mV)p-p max
with external trim	150mV(80mV)(40mV)(80mV)p-p max	100mV(60mV)(30mV)(60mV)p-p max ⁽¹⁾	—
Bandwidth			
-3dB Small Signal	1MHz	1MHz	1MHz
Full Power Response	750kHz	750kHz	750kHz
Slew Rate	45V/ μ sec	45V/ μ sec	45V/ μ sec
Output Characteristics			
Voltage at Rated Load (min)	$\pm 10V$	$\pm 10V$	$\pm 10V$
Current (min)	$\pm 5mA$	$\pm 5mA$	$\pm 5mA$
Input Resistance			
X/Y/Z Input ⁽²⁾	10M Ω /6M Ω /36k Ω	10M Ω /6M Ω /36k Ω	10M Ω /10M Ω /36k Ω
Input Bias Current			
X/Y/Z Input	2 μ A/2 μ A/5 μ A	2 μ A/2 μ A/5 μ A	2 μ A/3 μ A/5 μ A
Power Supply (V_S)			
Rated Performance	$\pm 15V$	$\pm 15V$	$\pm 15V$
Operating	± 12 to $\pm 18V$	± 12 to $\pm 18V$	± 10 to $\pm 18V$
Quiescent Current	$\pm 4mA$	$\pm 4.5mA$	$\pm 4mA$
Price (100's)	\$15.00(\$22.50)(\$27.50)(\$34.00)	\$8.90(\$13.35)(\$30.25)(\$35.85)	\$16.00(\$24.50)(\$32.50)

⁽¹⁾ I_{REF} = full scale.

⁽²⁾ Z input current is proportional to Z input voltage.

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The AD532 is the first pretrimmed single chip monolithic multiplier/divider. It guarantees a maximum multiplying error of $\pm 1.0\%$ and a $\pm 10V$ output voltage without the need for any external trimming resistors or output op amp. Because the AD532 is internally trimmed, its simplicity of use provides design engineers with an attractive alternative to modular multipliers, and its monolithic construction provides significant advantages in size, reliability and economy. Further, the AD532 can be used as a direct replacement for other IC multipliers that require external trim networks (such as the AD530).

The Analog Devices AD533 is a low cost integrated circuit multiplier comprised of a transconductance multiplying element, stable reference, and output amplifier on a monolithic silicon chip. Specified accuracy is easily achieved by the straightforward adjustment of feedthrough, output zero, and gain trim pots. The AD533 multiplies in four quadrants with a transfer function of $XY/10$, divides in two quadrants with a $10Z/X$ transfer function, and square roots in one quadrant with a transfer function of $-\sqrt{10Z}$.

533J (533K) (533L) (533S)

2% (1%) (0.5%) (1%)
YES

XY/10
0.04(0.03)(0.01)(0.01)%/°C
0.5%/%

Adj. to zero
0.7mV/°C
Fixed
Adj. to 1%

0.8%(0.5%)(0.5%)(0.5%)
0.3%(0.2%)(0.2%)(0.5%)

150mV(100mV)(50mV)(100mV)p-p max

200mV(100mV)(50mV)(100mV)p-p max

1MHz
750kHz
45V/ μ sec

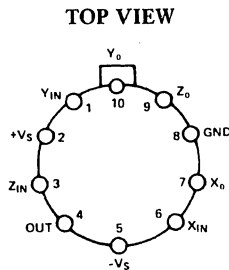
$\pm 10V$
 $\pm 5mA$

10M Ω /6M Ω /36k Ω

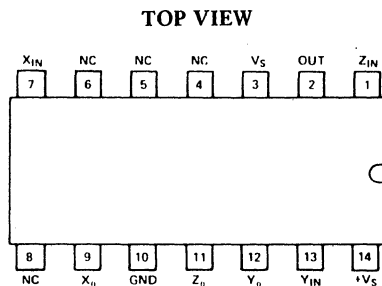
3 μ A(7.5 μ A max)(5 μ A max)(7.5 μ A max)

$\pm 15V$
 ± 12 to $\pm 18V$
 $\pm 4mA$
\$5.95(\$9.95)(\$25.00)(\$30.00)

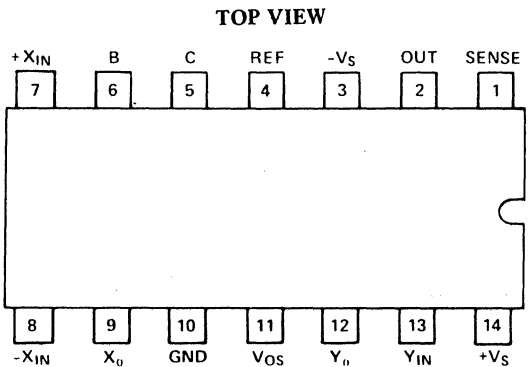
AD530, 532, 533
PIN OUT - TO-100



AD530, 532, 533
PIN OUT - TO-116



AD531
PIN OUT - TO-116



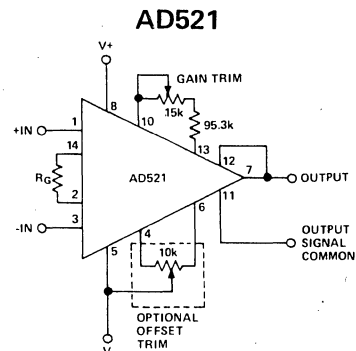
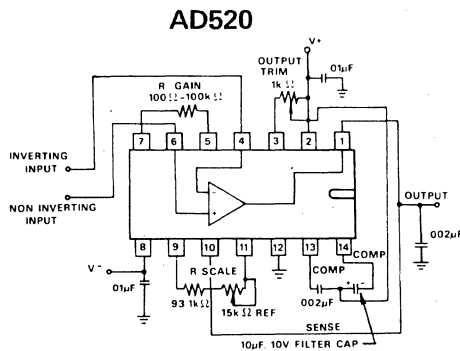
AD520, AD521

An *Instrumentation Amplifier* is a controlled gain block with differential inputs and an accurately programmable input/output gain relationship. Its excellent common mode rejection and low gain error make it a natural choice for extracting and amplifying low level signals in the presence of high common mode noise voltages. Instrumentation amplifiers are commonly used as transducer amplifiers for thermo couples, strain gauge bridges, current shunts, biological amplifiers, or simply as pre-amplifiers for processing small differential signals superimposed on common mode voltages.

Instrumentation amplifiers should not be confused with op amps even though Analog Devices offers op amps that can be used as building blocks in variable gain instrumentation amplifier circuits. An op amp is merely a high gain component requiring the addition of external feedback to complete the amplification function. Because of the limitations of resistor

matching in the external feedback circuit and the relatively low input impedance resulting from the input resistors, an instrumentation amplifier circuit designed around op amps frequently provides less than satisfactory performance. Instrumentation amplifiers manufactured by ADS, the AD520 and AD521, are complete amplification circuits which do not depend upon external resistor matching for input/output isolation, they maintain their high CMRR in any application. In addition, the high impedance inputs are fully protected against over voltages up to 15V greater than the supply voltage.

The AD520 and AD521 are the first instrumentation amplifiers to be manufactured in integrated circuit form; previously available commercial designs or user-made circuits were often costly, difficult to implement and often bulky. Now the benefits of a true instrumentation amplifier are available at a cost and ease of use that previously made them prohibitive.



SPECIFICATIONS (typical @ $V_S = \pm 15V$ and $T_A = +25^\circ C$ unless otherwise noted)

	AD520J	AD520K	AD520S	AD521J	AD521K	AD521S
GAIN						
Range	1 to 1000	*	*	1 to 1000	*	*
Equation	$G = R_G/R_G$ V/V	*	*	$G = R_G/R_G$ V/V	*	*
Nonlinearity	$\pm 0.5\%$ max	*	*	$\pm 0.2\%$ max	*	*
OUTPUT	$\pm 10V @ 5mA$ min	*	*	$\pm 10V @ 5mA$ min	*	*
BANDWIDTH ($\pm 3dB$)						
G = 1	200kHz	*	*	2MHz	*	*
G = 1000	25kHz	*	*	40kHz	*	*
SLEW RATE	2.5V/ μs	*	*	10V/ μs	*	*
VOLTAGE OFFSET, Output	MUST BE NULLED			(400 + 3 x G)mV max	(200 + 1.5G)mV max	**
DRIFT, Output @ G = 1	1mV/ $^\circ C$ max	0.5mV/ $^\circ C$ max	**	.415mV/ $^\circ C$ max	.205mV/ $^\circ C$ max	**
INPUT BIAS CURRENT	80nA max	40nA max	**	80nA max	40nA max	**
INPUT OFFSET CURRENT	40nA max	20nA max	**	20nA max	10nA max	**
INPUT IMPEDANCE						
Differential	$2 \times 10^9 \Omega$	*	*	$3 \times 10^9 \Omega$	*	*
Common Mode	$2 \times 10^9 \Omega$	*	*	$6 \times 10^9 \Omega$	*	*
CMRR						
G = 1	65dB min	70dB min	**	70dB min	74dB min	**
G = 100	95dB min	106dB min	**	100dB min	110dB min	**
TEMP RANGE	0 to +70 $^\circ C$	*	-55 to +125 $^\circ C$	0 to +70 $^\circ C$	*	-55 to +125 $^\circ C$
PRICE (100's)	\$12.00	\$16.00	\$22.00	\$8.50	\$12.00	\$20.00

*Same as J specifications.

**Same as K specifications.

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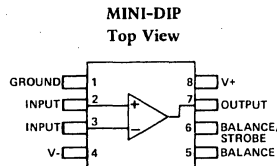
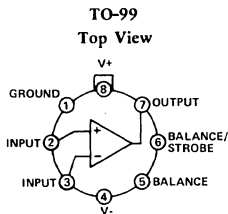
AD111, AD211, AD311, AD580, AD583

IC COMPARATOR

The AD111, AD211, and AD311 are precision voltage comparators designed for low level signal detection and high level output drive capability. Offering significant improvement over the earlier 710-type comparator in terms of bias currents and gain, the AD111 series operates on supply voltages from +5V (single ended) up to ±18V. TTL strobe capability is available with the addition of two external components. The AD311 is specified from 0 to +70°C, the AD211 from -25°C to +85°C and the AD111 over the full military temperature range -55°C to +125°C. All versions are available in the TO-99 can; the AD311 is also available in the 8 pin mini dip.

	AD311	AD211	AD111
Voltage Gain	200k	200k	200k
Offset Voltage (mV max)	7.5	3.0	3.0
Bias Current (nA max)	250	100	100
Maximum Output to -V _S	50V	50V	50V
Maximum Ground to -V _S	30V	30V	30V
Power Supply	+5V min*	+5V min*	+5V min*
Response Time, to TTL Logic Threshold (nsec)	200	200	200
Temp. Range (°C)	0 to +70	-25 to +85	-55 to +125

*Single Ended



IC SAMPLE-HOLD

The AD583 is a monolithic sample and hold circuit consisting of a high performance operational amplifier in series with an ultra-low leakage analog switch and a MOSFET input unity gain amplifier. An external holding capacitor, connected to the switch output, completes the sample-and-hold or track-and-hold function.

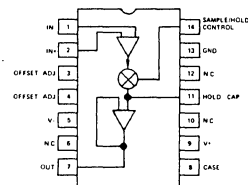
With the analog switch closed, the AD583 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open the capacitor holds the output at its previous level.

The AD583 may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.

	AD583K
Open Loop Gain	25k min
R _L = 2kΩ	
Output Swing	±10V min
Gain Bandwidth	2MHz
Acquisition Time (0.1%)	4μsec
A _V = 1, R _L = 2k, C _L = 50pF	
Aperture Time	50nsec
Drift Current	50pA max
Charge Transfer	20pC max
Operating Temp.	0 to +70°C
Price (100's)	\$14.85

PIN CONFIGURATION

TO-116 DIP



IC REFERENCE

The AD580 is a three-terminal, low cost, temperature compensated, bandgap voltage reference which provides a fixed 2.5V output voltage for inputs between 4.5V and 30V. A unique combination of advanced circuit design and sophisticated thin film resistor processing capability provides the AD580 with a temperature stability of better than 10ppm/°C and long term stability of better than 250μV. In addition, the low quiescent current drain of 1.0mA max offers a clear advantage over classical zener techniques.

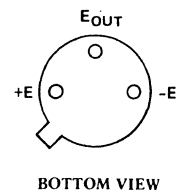
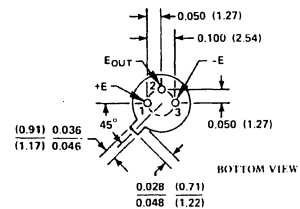
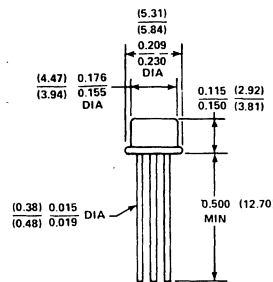
Model	Output Voltage	T.C. ppm/°C max	Temp. Range	Price
AD580J	2.500 ±3%	85	C	\$2.00
AD580K	2.500 ±2%	40	C	\$4.00
AD580L	2.500 ±2%	25	C	\$5.75
AD580M	2.500 ±1%	10	C	\$8.25
AD580S	2.500 ±3%	55	M	\$7.50
AD580T	2.500 +2%	25	M	\$12.00
AD580U	2.500 +1%	10	M	\$25.00

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OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

CASE 27 TO-52 PACKAGE



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Monolithic Function Generator

ELECTRICAL CHARACTERISTICS Preliminary

Test Conditions: Test Circuit of Fig. 2, $V^+ = 12V$, $T_A = 25^\circ C$, $C = 0.01 \mu F$, $R_1 = 100 K\Omega$, $R_2 = 10 K\Omega$, $R_3 = 25 K\Omega$ unless otherwise specified. S_1 open for triangle, closed for sinewave.

CHARACTERISTICS	XR-2206M, XR-2206			XR-2206C			UNITS	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Supply Voltage								
Single Supply	10		26	10		26	V	$R_1 \geq 10 K\Omega$
Split Supply	± 5		± 13	± 5		± 13	V	
Supply Current		12	17		14	20	mA	
Oscillator Section								
Max. Operating Frequency	0.5	1		0.5	1		MHz	$C = 1000 pF$, $R_1 = 1 K\Omega$
Lowest Practical Frequency		0.01			0.01		Hz	$C = 50 \mu F$, $R_1 = 2 M\Omega$
Frequency Accuracy		± 1	± 4		± 2		% of f_0	$f_0 = 1/R_1 C$
Temperature Stability		± 10	± 50		± 20		ppm/ $^\circ C$	$0^\circ C \leq T_A \leq 75^\circ C$, $R_1 = R_2 = 20 K\Omega$
Supply Sensitivity		0.01	0.1		0.01		%	$V_{LOW} = 10V$, $V_{HIGH} = 20V$, $R_1 = R_2 = 20 K\Omega$
Sweep Range	1000:1	2000:1			2000:1		$f_H = f_L$	$f_H @ R_1 = 1 K\Omega$ $f_L @ R_1 = 2 M\Omega$
Sweep Linearity								
10:1 Sweep		2			2		%	$f_L = 1 kHz$, $f_H = 10 kHz$
1000:1 Sweep		8			8		%	$f_L = 100 Hz$, $f_H = 100 kHz$
FM Distortion		0.1			0.1		%	$\pm 10\%$ Deviation
Recommended Timing Components								
Timing Capacitor: C	0.001		100	0.001		100	μF	See Figure 5
Timing Resistors: R_1 & R_2	1		2000	1		2000	$K\Omega$	
Triangle/Sinewave Output								
Triangle Output		160			160		mV/ $K\Omega$	See Note 1, Fig. .
Sinewave Output	40	60	80		60		mV/ $K\Omega$	Fig. 2 S_1 Open
Max. Output Swing		6			6		V _{pp}	Fig. 2 S_1 Closed
Output Impedance		600			600		Ω	
Triangle Linearity		1			1		%	
Amplitude Stability		0.5			0.5		dB	For 1000:1 Sweep
Sinewave Distortion								
Without Adjustment		2.5			2.5		%	$R_1 = 30 K\Omega$
With Adjustment		0.4	1.0		0.5	1.5	%	See Figure 11. See Figure 12
Amplitude Modulation								
Input Impedance	50	100		50	100		$K\Omega$	
Modulation Range		100			100		%	
Carrier Suppression		55			55		dB	
Linearity		2			2		%	For 95% modulation
Square Wave Output								Measured at Pin 11
Amplitude		12			12		V _{pp}	
Rise Time		250			250		nsec	$C_L = 10 pF$
Fall Time		50			50		nsec	$C_L = 10 pF$
Saturation Voltage		0.2	0.4		0.2	0.4	V	$I_L = 2 mA$
Leakage Current		0.1	20		0.1		μA	$V_{11} = 12V$
FSK Keying Level (Pin 9)	0.8	1.4	2.4	0.8	1.4	2.4	V	See Section on Circuit Controls
Reference Bypass Voltage	2.9	3.1	3.3	2.5	3	3.5	V	Measured at Pin 10.

Note 1: Output Amplitude is inversely proportional to the resistance R_3 on Pin 3. See Figure 3

APPLICATIONS INFORMATION

SINEWAVE GENERATION

A) Without External Adjustment

Figure 11 shows the circuit connection for generating a sinusoidal output from the XR-2206. The potentiometer R_1 at pin 7 provides the desired frequency tuning. The maximum output swing is greater than $V^+/2$ and the typical distortion (THD) is $< 2.5\%$. If lower sinewave distortion is desired, additional adjustments can be provided as described in the following section.

The circuit of Figure 11 can be converted to split supply operation simply by replacing all ground connections with V^- . For split supply operation, R_3 can be directly connected to ground.

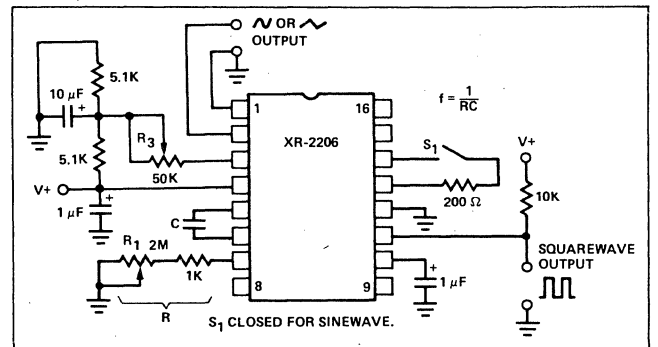


Figure 11. Circuit for Sinewave Generation Without External Adjustment. (See Fig. 3 for choice of R_3)

B) With External Adjustment

The harmonic content of sinusoidal output can be reduced to $\approx 0.5\%$ by additional adjustments as shown in Figure 12. The potentiometer R_A adjusts the sine-shaping resistor; and R_B provides the fine-adjustment for the waveform symmetry. The adjustment procedure is as follows:

1. Set R_B at mid-point and adjust R_A for minimum distortion.
2. With R_A set as above, adjust R_B to further reduce distortion.

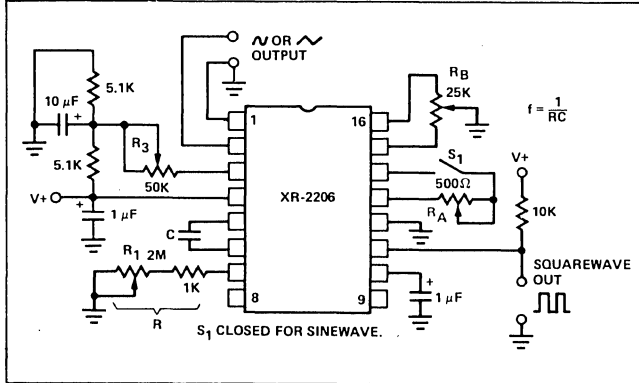


Figure 12. Circuit for Sinewave Generation With Minimum Harmonic Distortion. (R_3 Determines output Swing)

TRIANGLE WAVE GENERATION

The circuits of Figures 11 and 12 can be converted to triangle wave generation by simply open circuiting pins 13 and 14 (i.e., S_1 open). Amplitude of the triangle is approximately twice the sinewave output.

FSK GENERATION

Figure 13 shows the circuit connection for sinusoidal FSK signal generation. Mark and space frequencies can be independently adjusted by the choice of timing resistors R_1 and R_2 ; and the output is phase-continuous during transitions. The keying signal is applied to pin 9. The circuit can be converted to split-supply operation by simply replacing ground with V^- .

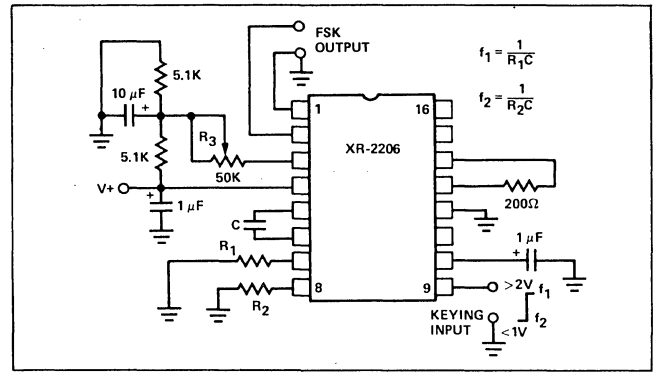


Figure 13. Sinusoidal FSK Generator

PULSE AND RAMP GENERATION

Figure 14 shows the circuit for pulse and ramp waveform generation. In this mode of operation, the FSK keying terminal (pin 9) is shorted to the square-wave output (pin 11); and the circuit automatically frequency-shifts itself between two separate frequencies during the positive and negative going output waveforms. The pulse-width and the duty cycle can be adjusted from 1% to 99% by the choice of R_1 and R_2 . The values of R_1 and R_2 should be in the range of 1 $K\Omega$ to 2 $M\Omega$.

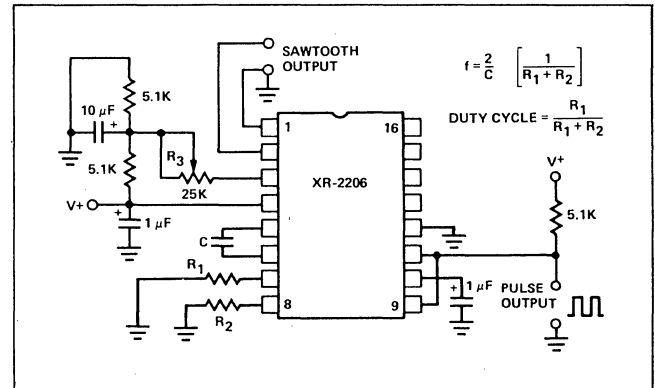
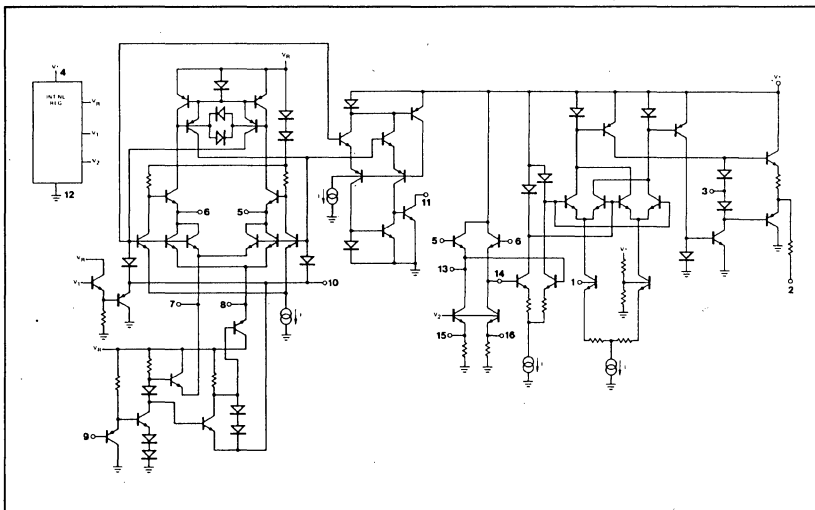
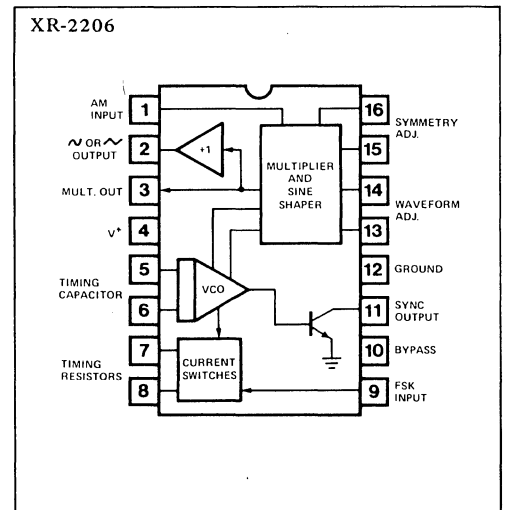


Figure 14. Circuit for Pulse and Ramp Generation

EQUIVALENT SCHEMATIC DIAGRAM



FUNCTIONAL BLOCK DIAGRAM





Voltage - Controlled Oscillator

ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of Figure 2, $V^+ = V^- = 6V$, $T_A = +25^\circ C$, $C = 5000 \text{ pF}$, $R_1 = R_2 = R_3 = R_4 = 20 \text{ K}\Omega$, $R_L = 4.7 \text{ K}\Omega$, Binary Inputs grounded, S_1 and S_2 closed unless otherwise specified.

PARAMETERS	XR-2207			XR-2207C			UNITS	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
GENERAL CHARACTERISTICS								
Supply Voltage Single Supply Split Supplies	8 ± 4		26 ± 13	8 ± 4		26 ± 13	V V	See Figure 3
Supply Current Single Supply		5	7		5	8	mA	Measured at pin 1, S_1 open see Figure 2
Split Supplies Positive Negative		5 4	7 6		5 4	8 7	mA mA	Measured at pin 1, S_1, S_2 open Measured at pin 12, S_1, S_2 open
OSCILLATOR SECTION - FREQUENCY CHARACTERISTICS								
Upper Frequency Limit	0.5	1.0		0.5	1.0		MHz	$C = 500 \text{ pF}$, $R_3 = 2 \text{ K}\Omega$
Lowest Practical Frequency		0.01			0.01		Hz	$C = 50 \text{ }\mu\text{F}$, $R_3 = 2 \text{ M}\Omega$
Frequency Accuracy		± 1	± 3		± 1	± 5	% of f_0	
Frequency Matching		0.5			0.5		% of f_0	
Frequency Stability Temperature Power Supply		20 0.15	50		30 0.15		ppm/ $^\circ C$ %/V	$0^\circ < T_A < 75^\circ C$
Sweep Range	1000:1	3000:1			1000:1		f_H/f_L	$R_3 = 1.5 \text{ K}\Omega$ for f_H $R_3 = 2 \text{ M}\Omega$ for f_L
Sweep Linearity 10:1 Sweep 1000:1 Sweep		1 5	2		1.5 5		%	$C = 5000 \text{ pF}$ $f_H = 10 \text{ kHz}$, $f_L = 1 \text{ kHz}$ $f_H = 100 \text{ kHz}$, $f_L = 100 \text{ Hz}$
FM Distortion		- 0.1			0.1		%	$\pm 10\%$ FM Deviation
Recommended Range of Timing Resistors	1.5		2000	1.5		2000	$\text{K}\Omega$	See Characteristic Curves
Impedance at Timing Pins		75			75		Ω	Measured at pins 4, 5, 6, or 7
DC Level at Timing Terminals		10			10		mV	
BINARY KEYING INPUTS								
Switching Threshold	1.4	2.2	2.8	1.4	2.2	2.8	V	Measured at pins 8 and 9, Refer to pin 10
Input Impedance		5			5		$\text{K}\Omega$	
OUTPUT CHARACTERISTICS								
Triangle Output Amplitude Impedance DC Level Linearity	4	6 10 +100 0.1		4	6 10 +100 0.1		V_{pp} Ω mV %	Measured at pin 13 Referenced to pin 10 from 10% to 90% of swing
Squarewave Output Amplitude Saturation Voltage Rise Time Fall Time	11	12 0.2 200 20	0.4	11	12 0.2 200 20	0.4	V_{pp} V nsec nsec	Measured at pin 13, S_5 closed Referenced to pin 12 $C_L \leq 10 \text{ pF}$ $C_L \leq 10 \text{ pF}$

APPLICATIONS

SPLIT SUPPLY OPERATION

Figure 1 is the recommended circuit connection for split supply operation. The frequency of operation is determined by the timing capacitor, C, and the activated timing resistors (R_1 through R_4). The timing resistors are activated by the logic signals at the binary keying inputs (pins 8 and 9), as shown in the logic table in Figure 9. If a single timing resistor is activated, the frequency is $1/RC$. Otherwise, the frequency is either $1/(R_1 \parallel R_2)C$ or $1/(R_3 \parallel R_4)C$.

The squarewave output is obtained at pin 13 and has a peak-to-peak voltage swing equal to the supply voltages. This output is an "open-collector" type and requires an external pull-up load resistor (nominally $5 \text{ K}\Omega$) to the positive supply. The triangle

waveform obtained at pin 14 is centered about ground and has a peak amplitude of $V/2$.

LOGIC LEVEL	SELECTED TIMING PINS	FREQUENCY	DEFINITIONS
8 9			
0 0	6	f_1	$f_1 = 1/R_3C$, $\Delta f_1 = 1/R_4C$
0 1	6 and 7	$f_1 + \Delta f_1$	$f_2 = 1/R_2C$, $\Delta f_2 = 1/R_1C$
1 0	5	f_2	Logic Levels: 0 = Ground
1 1	4 and 5	$f_2 + \Delta f_2$	1 = $> 3V$

TABLE 1. Logic Table for Binary Keying Controls

Note: For Single-Supply Operation, Logic Levels are Referenced to Voltage at Pin 10

The circuit operates with supply voltages ranging from $\pm 4V$ to $\pm 13V$. Minimum drift occurs with ± 6 volt supplies. For operation with unequal supply voltages, see Figure 3.

SINGLE SUPPLY OPERATION

The circuit should be interconnected as shown in Figure 2 for single supply operation. Pin 12 should be grounded, and pin 11 biased from V^+ through a resistive divider to a value of bias voltage between $V^+/3$ and $V^+/2$. Pin 10 is bypassed to ground through a $1 \mu F$ capacitor.

For single supply operation, the dc voltage at pin 10 and the timing terminals (pins 4 through 7) are equal and approximately $0.6V$ above V_B , the bias voltage at pin 11. The logic levels at the binary keying terminals are referenced to the voltage at pin 10.

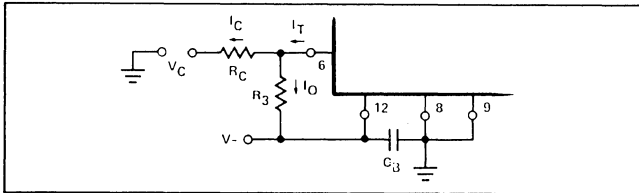


Figure 9. Frequency Sweep Operation

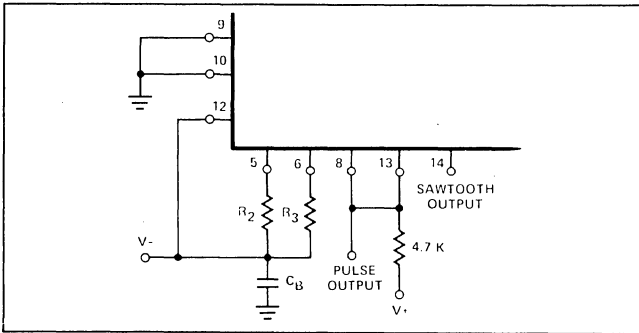
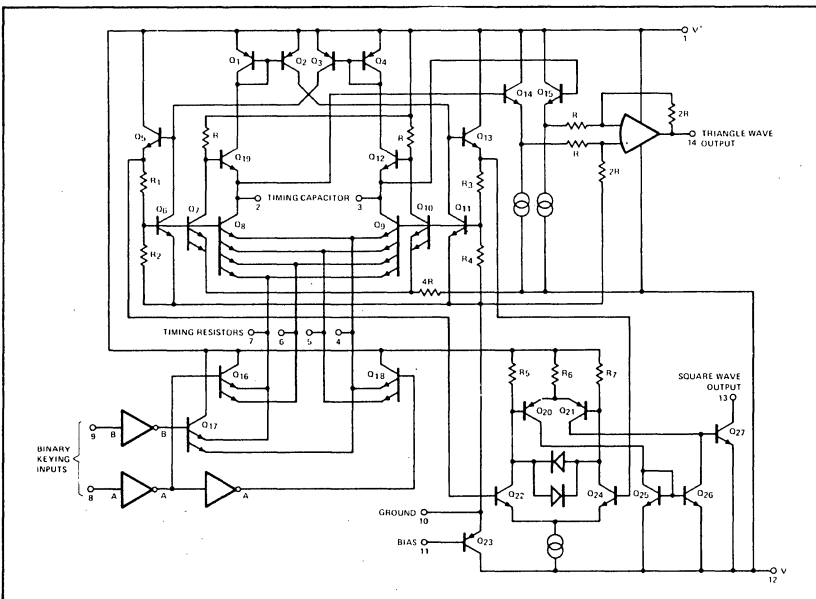


Figure 10. Pulse and Sawtooth Generation

FREQUENCY CONTROL (SWEEP AND FM)

The frequency of operation is controlled by varying the total timing current, I_T , drawn from the activated timing pins 4, 5, 6, or 7. The timing current can be modulated by applying a control voltage, V_C , to the activated timing pin through a series resistor R_C as shown in Figure 9.

EQUIVALENT SCHEMATIC DIAGRAM



For split supply operation, a *negative* control voltage, V_C , applied to the circuits of Figure 9 causes the total timing current, I_T , and the frequency, to increase.

As an example, in the circuit of Figure 9, the binary keying inputs are grounded. Therefore, only timing pin 6 is activated.

The frequency of operation is determined by:

$$f = \frac{1}{R_3 C} \left[1 - \frac{V_C R_3}{R_C V^-} \right] \text{ Hz}$$

PULSE AND SAWTOOTH GENERATION

The duty cycle of the output waveforms can be controlled by frequency shift keying at the end of every half cycle of oscillator output. This is accomplished by connecting one or both of the binary keying inputs (pins 8 or 9) to the squarewave output at pin 13. The output waveforms can then be converted to positive or negative pulses and sawtooth waveforms.

Figure 10 is the recommended circuit connection for duty cycle control. Pin 8 is shorted to pin 13 so that the circuit switches between the "0, 0" and the "1, 0" logic states given in Figure 9. Timing pin 5 is activated when the output is "high," and pin 6 is activated when the squarewave output goes to a low state.

The duty cycle of the output waveforms is given as:

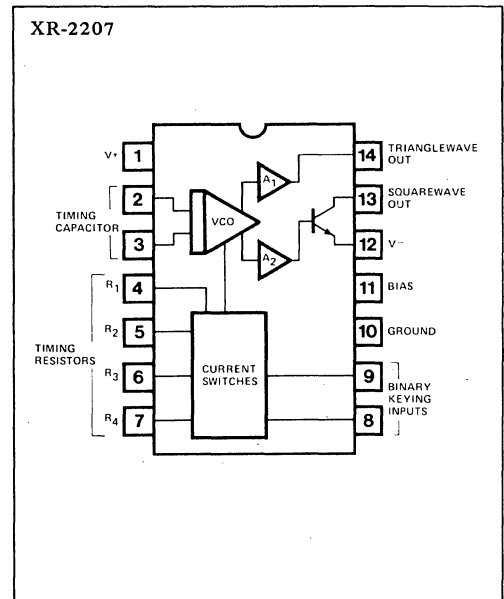
$$\text{Duty Cycle} = \frac{R_2}{R_2 + R_3}$$

and can be varied from 0.1% to 99.9% by proper choice of timing resistors. The frequency of oscillation, f , is given as:

$$f = \frac{2}{C} \left[\frac{1}{R_2 + R_3} \right]$$

The frequency can be modulated or swept without changing the duty cycle by connecting R_2 and R_3 to a common control voltage V_C , instead of to V^- . The sawtooth and the pulse output waveforms are shown in Figure 5.

FUNCTIONAL BLOCK DIAGRAM





Operational Multiplier

ELECTRICAL CHARACTERISTICS Test Conditions: Supply Voltage = $\pm 15V$, $T_A = 25^\circ C$, unless otherwise specified.

CHARACTERISTICS	XR-2208/XR-2208M			XR-2208C			UNITS	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
I. GENERAL								
Supply Voltage	± 4.5		± 16	± 4.5		± 16		
Supply Current		4	7		5	8		Measured at pin 16
II. MULTIPLIER SECTION								
Non-linearity (Output Error in % of Full Scale)		0.3 0.3 0.7	0.5 0.5 1.0		0.5 0.5 0.8	1.0 1.0	% % %	No external offset rim $V_y = \pm 10V, -10V < V_x < +10V$ $V_x = \pm 10V, -10V < V_y < +10V$ $T_{LOW} \leq T_A \leq T_{HIGH}$ (Note 1) $f = 50$ Hz
Feedthrough								
a) With Offset Adjustment								
X-input		45	80		70		mVp-p	$V_x = 20$ Vp-p, $V_y = 0$
Y-input		60	100		90		mVp-p	$V_y = 20$ Vp-p, $V_x = 0$
b) No Offset Adjustment								
X-input		120			200		mVp-p	$V_x = 20$ Vp-p, $V_x = 0$
Y-input		120			200		mVp-p	$V_y = 20$ Vp-p, $V_x = 0$
Temperature Coefficient of Scale Factor		± 0.07			± 0.07		%/°C	$T_{LOW} \leq T_A \leq T_{HIGH}$ (Note 1)
Input Bias Current								
X, Y input		2	6		3	8	μA	I_3, I_5
Common input		4	12		6	16	μA	I_4
Input Resistance	0.5	1.0			1.0		M Ω	Measured looking into pin 3 or pin 5
Output Offset Voltage		50	80		80	140	mV	Measured across pins 1 and 2
Average Temperature Drift		0.5			0.5		mV/°C	$T_{LOW} \leq T_A \leq T_{HIGH}$
Dynamic Response								See Definition Section
3-dB Bandwidth								
X-input	6	8		6	6	8	MHz	
Y-input	3	4		3	3	4	MHz	
3° Phase-Shift Bandwidth		1.2			1.2		MHz	
1% Absolute Error Bandwidth		30			30		kHz	
Transconductance Bandwidth		100			100		MHz	
Output Impedance		6			6		K Ω	Measured looking into pins 1 or 2
III. BUFFER AMPLIFIER								
Output Impedance		200			200		Ω	Measured looking into pin 15
Gain		1.0			1.0			
IV. OPERATIONAL AMPLIFIER								
Input Offset Voltage		1	3		2	6	mV	$R_S < 50\Omega$
Temperature Coefficient of Input Offset Voltage		6	20		9	30	$\mu V/^\circ C$	$T_{LOW} \leq T_A \leq T_{HIGH}$
Input Offset Current		4	75		10	100	nA	$I_{B1} - I_{B2}$
Input Bias Current		30	200		50	300	nA	$\frac{I_{B1} + I_{B2}}{2}$
Voltage Gain	70	75		70	75		dB	$R_L \geq 2K, V_O = \pm 10V, f = 20$ Hz
Differential Input Resistance	0.5	3			3		M Ω	
Output Voltage Swing	± 10	± 12		± 10	± 12		V	$R_L \geq 2K, T_{LOW} \leq T_A \leq T_{HIGH}$
Input Common Mode Range	+12	+14		+12	+14			
Mode Range	-10	-12		-10	-12		V	
Common Mode Rejection	70	90		70	90		dB	$f = 20$ Hz
Output Resistance		2			2		k Ω	
Slew Rate		0.5			0.5		V/ μs	Gain = 1, $R_L \geq 2K, C_L \leq 100$ pF $C_C = 20$ pF
Power Supply Sensitivity		30			30		$\mu V/V$	$R_S \leq 10K$

Note 1: $T_{LOW} = -55^\circ C$, $T_{HIGH} = +125^\circ C$ for XR-2208M $T_{LOW} = 0^\circ C$, $T_{HIGH} = +75^\circ C$ for XR-2208/XR-2208C

The XR-2208 operational multiplier combines a four-quadrant analog multiplier (or modulator), a high frequency buffer amplifier, and an operational amplifier in a monolithic circuit that is ideally suited for both analog computation and communications signal processing application. As shown in the functional block diagram, for maximum versatility the multiplier and operational amplifier sections are not internally connected. They can be interconnected, with a minimum

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number of external components, to perform arithmetic computation, such as multiplication, division, square-root extraction. The operational amplifier can also function as a pre-amplifier for low-level input signals, or as a post detection amplifier for synchronous demodulator applications. For signal processing, the high frequency buffer amplifier output is available at pin 15. This multiplier/buffer amplifier combination extends the small signal 3-db bandwidth to 8-MHz and the transconductance bandwidth to 100 MHz.

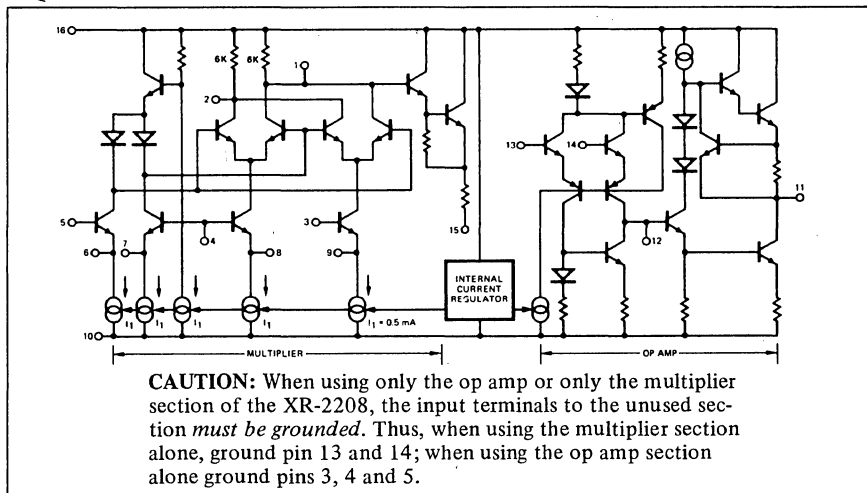
FEATURES

- Maximum Versatility
 - Independent Multiplier, Op Amp, and Buffer
- Excellent Linearity (0.3% typ.)
- Wide Bandwidth
 - 3 dB B.W. - 8 MHz typ.
 - 3° Phase Shift B.W. - 1.2 MHz typ.
 - Transconductance B.W. - 100 MHz typ.
- Simplified Offset Adjustments
- Wide Supply Voltage Range ($\pm 4.5V$ to $\pm 16V$)

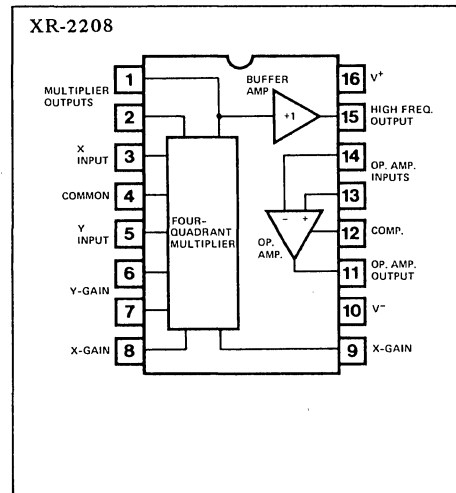
APPLICATIONS

- Analog Computation
 - Multiplication
 - Division
 - Squareing
 - Square-Root
- Signal Processing
 - AM Generation
 - Frequency Doubling
 - Frequency Translation
 - Synchronous AM Detection
- Triangle-to-Sinewave Converter
- AGC Amplifier
- Phase Detector
- Phase-Locked Loop (PLL) Applications
 - Motor Speed Control
 - Precision PLL
 - Carrier Detection
 - Phase-Locked AM Demodulation

EQUIVALENT SCHEMATIC DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



XR-2211

EXAR INTEGRATED SYSTEMS, INC.
750 Palomar Ave., Sunnyvale, CA 94086 Sales: (408) 733-7700



FSK Demodulator/Tone Decoder

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay.

FSK DECODING WITH CARRIER-DETECT:

The lock-detect section of XR-2211 can be used as a carrier-detect option, for FSK decoding. The recommended circuit connection for this application is shown in Fig. 10. The open-collector lock-detect output, Pin 6, is shorted to data output (Pin 7). Thus, data output will be disabled at "low" state, until there is a carrier within the detection band of the PLL, and the Pin 6 output goes "high", to enable the data output.

The value of lock-detect filter capacitance, C_D , can be calculated from design equation: $C_D \geq 50/f_0$ (Hz) μF .

LINEAR FM DETECTION:

XR-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for this applications is shown in Fig. 12. The demodulated output is taken from the loop phase detector output (Pin 11), through a post detection filter made up of R_F and C_F , and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at Pin 11. Normally, a non-inverting unity

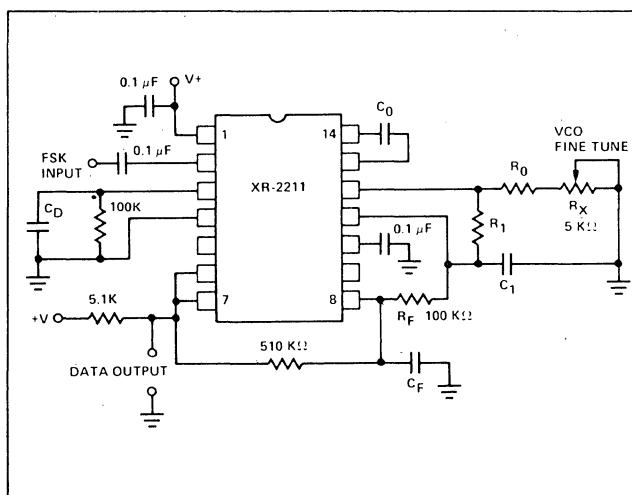


Figure 10. External Connections for FSK Demodulation with Carrier-Detect Capability.
Note: Data Output is "Low" When No Carrier is Present.

LINEAR Exar

gain op amp can be used as a buffer amplifier, as shown in Fig. 12.

The FM detector gain, i.e., the output voltage change per unit of FM deviation, can be given as:

$$V_{out} = R_1 V_R / 100 R_0 \text{ Volts}/\% \text{ deviation}$$

where V_R is the internal reference voltage. ($V_R = V^+ / 2 - 650 \text{ mV}$). For the choice of external components R_1 , R_0 , C_D , C_1 and C_F , see section on Design Equations.

ELECTRICAL CHARACTERISTICS --PRELIMINARY--

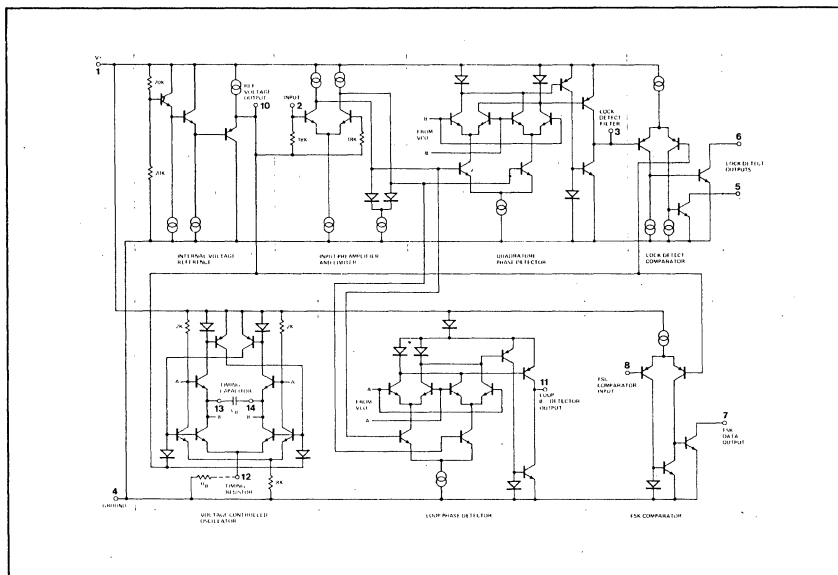
Test Conditions: $V^+ = +12\text{V}$, $T_A = +25^\circ\text{C}$, $R_0 = 30 \text{ K}\Omega$, $C_0 = 0.033 \mu\text{F}$. See Fig. 2 for component designation.

CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
GENERAL					
Supply Voltage	4.5		20	V	$R_0 \geq 10 \text{ K}\Omega$. See Fig. 4.
Supply Current		5	9	mA	
OSCILLATOR SECTION					
Frequency Accuracy		± 1		%	Deviation from $f_0 = 1/R_0 C_0$ $R_1 = \infty$ See Fig. 8.
Frequency Stability					
Temperature		± 20		ppm/ $^\circ\text{C}$	$V^+ = 12 \pm 1\text{V}$. See Fig. 7. $V^+ = 5 \pm 0.5\text{V}$. See Fig. 7.
Power Supply		0.05		%/V	
Upper Frequency Limit		0.2		%/V	$R_0 = 8.2 \text{ K}\Omega$, $C_0 = 400 \text{ pF}$
Lowest Practical		300		kHz	
Operating Frequency		0.01		Hz	$R_0 = 2 \text{ M}\Omega$, $C_0 = 50 \mu\text{F}$ See Fig. 5.
Timing Resistor, R_0					
Operating Range	5		2000	$\text{K}\Omega$	See Fig. 7 and 8.
Recommended Range	15		100	$\text{K}\Omega$	
LOOP PHASE DETECTOR SECTION					
Peak Output Current	± 100	± 200	± 300	μA	Measured at Pin 11.
Output Offset Current		± 2		μA	
Output Impedance		1		$\text{M}\Omega$	Referenced to Pin 10.
Maximum Swing	± 4	± 5		V	
QUADRATURE PHASE DETECTOR					Measured at Pin 3.
Peak Output Current		150		μA	
Output Impedance		1		$\text{M}\Omega$	
Maximum Swing		11		V _{pp}	
INPUT PREAMP SECTION					Measured at Pin 2.
Input Impedance		20		$\text{K}\Omega$	
Input Signal					
Voltage Required to Cause Limiting		2		mV rms	
Max. Input Voltage		3		V rms	
VOLTAGE COMPARATOR SECTIONS					Measured at Pins 3 and 8.
Input Impedance		2		$\text{M}\Omega$	$R_L = 5.1 \text{ K}\Omega$ $I_C = 3 \text{ mA}$ $V_0 = 12\text{V}$
Input Bias Current		100		nA	
Voltage Gain	55	70		dB	
Output Voltage Low		300		mV	
Output Leakage Current		10		nA	
INTERNAL REFERENCE					Measured at Pin 10.
Voltage Level	4.75	5.3	5.85	V	
Output Impedance		100		Ω	

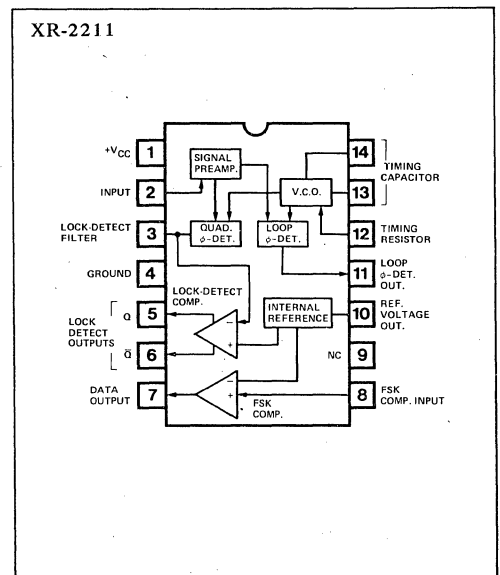
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EQUIVALENT SCHEMATIC DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



XR-2240

XR-2250

EXAR INTEGRATED SYSTEMS, INC.
750 Palomar Ave., Sunnyvale, CA 94086 Sales: (408) 733-7700



Programmable Timer/Counter

ELECTRICAL CHARACTERISTICS

Test Conditions: See Figure 3, $V^+ = 5V$, $T_A = 25^\circ C$, $R = 10\ k\Omega$, $C = 0.1\ \mu F$, unless otherwise noted.

PARAMETERS	XR-2240/2250			XR-2240C/2250C			UNIT	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Supply Voltage	4		15	4		15	V	For $V^+ < 4.5V$, Short Pin 15 to Pin 16
Supply Current		3.5	6		4	7	mA	$V^+ = 5V$, $V_{TR} = 0$, $V_{RS} = 5V$
Total Circuit		12	16		13	18	mA	$V^+ = 15V$, $V_{TR} = 0$, $V_{RS} = 5V$
Counter Only		1			1.5		mA	See Figure 4
Regulator Output, V_R	4.1	4.4		3.9	4.4		V	Measured at Pin 15, $V^+ = 5V$
	6.0	6.3	6.6	5.8	6.3	6.8	V	$V^+ = 15V$, See Figure 5
TIME BASE SECTION								
								See Figure 3
Timing Accuracy *		0.5	2.0		0.5	5	%	$V_{RS} = 0$, $V_{TR} = 5V$ $V^+ = 5V$, $0^\circ C \leq T \leq 75^\circ C$ $V^+ = 15V$
Temperature Drift		150	300		200		ppm/ $^\circ C$	
Supply Drift		80			80		ppm/ $^\circ C$	
Max Frequency	100	0.05	0.2		0.08	0.3	kHz	$V^+ \geq 8$ Volts $R = 1\ k\Omega$, $C = 0.007\ \mu F$
Modulation Voltage Level	3.00	3.50	4.0	2.80	3.50	4.20	V	Measured at Pin 12
		10.5			10.5		V	$V^+ = 5V$ $V^+ = 15V$
Recommended Range of Timing Components								See Figure 6
Timing Resistor, R	0.001		10	0.001		10	$M\Omega$	
Timing Capacitor, C	0.007		1000	0.01		1000	μF	
TRIGGER/RESET CONTROLS								
Trigger								Measures at Pin 11, $V_{RS} = 0$
Trigger Threshold		1.4	2.0		1.4	2.0	V	$V_{RS} = 0$, $V_{TR} = 2V$
Trigger Current		8			10		μA	
Impedance		25			25		$k\Omega$	
Response Time **		1			1		μsec	
Reset								$V_{TR} = 0$, $V_{RS} = 2V$
Reset Threshold		1.4	2.0		1.4	2.0	V	
Reset Current		8			10		μA	
Impedance		25			25		$k\Omega$	
Response Time **		0.8			0.8		μsec	
COUNTER SECTION								
								See Figure 5, $V^+ = 5V$
Max. Toggle Rate	0.8	1.5			1.5		MHz	$V_{RS} = 0$, $V_{TR} = 5V$ Measured at Pin 14
Input:								Measured at Pins 1 thru 8 $R_L = 3K\Omega$, $C_L = 10\ pF$
Impedance		20			20		$k\Omega$	
Threshold	1.0	1.4		1.0	1.4		V	
Output:								$V_{OL} \leq 0.4V$ $V_{OH} \leq 15V$
Rise Time		180			180		nsec.	
Fall Time		180			180		nsec.	
Sink Current	3	5		2	4		mA	
Leakage Current		0.01	8		0.01	15	μA	

*Timing error solely introduced by XR-2240, measured as % of ideal time-base period of $T = 1.00\ RC$.

**Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at pin 1.

APPLICATIONS INFORMATION (2240)

PRECISION TIMING (Monostable Operation)

In precision timing applications, the XR-2240 is used in its monostable or "self-resetting" mode. The circuit connection for this application is shown in Figure 9.

ASTABLE OPERATION

The XR-2240 can be operated in its astable or free-running

mode by disconnecting the reset terminal (pin 10) from the counter outputs. Two typical circuit connections for this mode of operation are shown in Figure 12. In the circuit connection of Figure 12(a), the circuit operates in its free-running mode, with external trigger and reset signals. It will start counting and timing subsequent to a trigger input until an external reset pulse is applied. Upon application of a positive-going reset signal to pin 10, the circuit reverts back to its rest state. The circuit of Figure 12(a) is essentially the same as that of Figure 6, with the feedback switch S_1 open.

LINEAR EXAR

The circuit of Figure 12(b) is designed for continuous operation. The circuit self-triggering automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely.

In stable or free-running operation, each of the counter outputs can be used individually as synchronized oscillators; or they can be interconnected to generate complex pulse patterns.

OPERATION WITH EXTERNAL CLOCK

The XR-2240 can be operated with an external clock or time-base, by disabling the internal time-base oscillator and applying the external clock input to pin 14. The internal time-base can

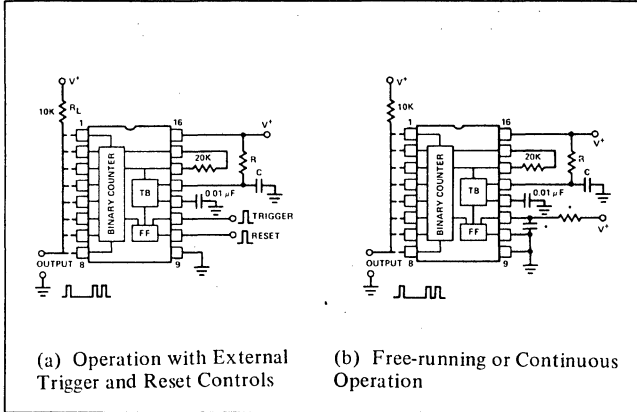
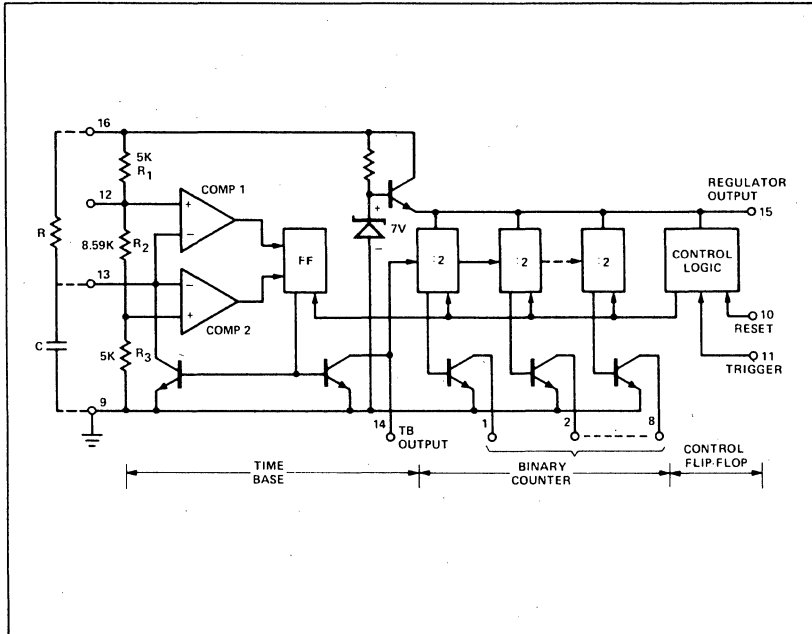


Figure 12. Circuit Connections for Astable Operation

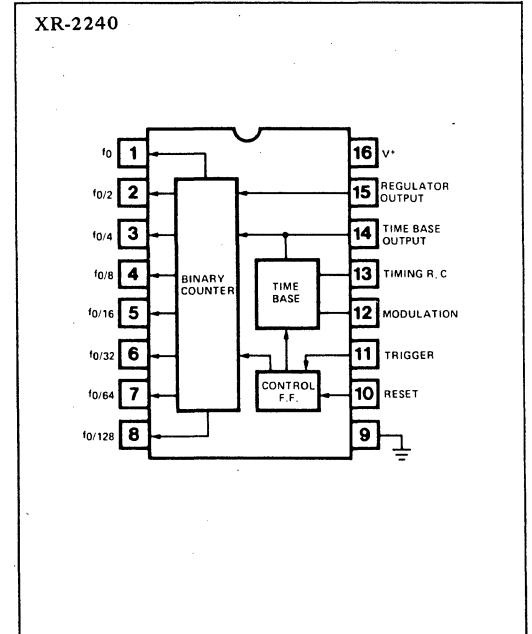
be de-activated by connecting a 1 KΩ resistor from pin 13 to ground. The counters are triggered on the negative-going edges of the external clock pulse. For proper operation, a minimum clock pulse amplitude of 3 volts is required. Minimum external clock pulse width must be ≥ 1 µS.

For operation with supply voltages of 6V or less, the internal time-base section can be powered down by open-circuiting pin 16 and connecting pin 15 to V+. In this configuration, the internal time-base does not draw any current, and the over-all current drain is reduced by ≈ 3 mA.

SIMPLIFIED SCHEMATIC DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



FREQUENCY SYNTHESIS WITH HARMONIC LOCKING: The harmonic synchronization property of the XR-2240 time-base can be used to generate a wide number of discrete frequencies from a given input reference frequency. The circuit connection for this application is shown in Figure 13. If the time base is synchronized to (m)th harmonic of input frequency where 1 ≤ m ≤ 10, as described in the section on "Harmonic Synchronization", the frequency f_o of the output waveform in Figure 25 is related to the input reference frequency f_R as:

$$f_o = f_R \frac{m}{(N+1)}$$

where m is the harmonic number, and N is the programmed counter modulus. For a range of 1 ≤ N ≤ 255, the circuit of Figure 13 can produce 1500 separate frequencies from a single fixed reference.

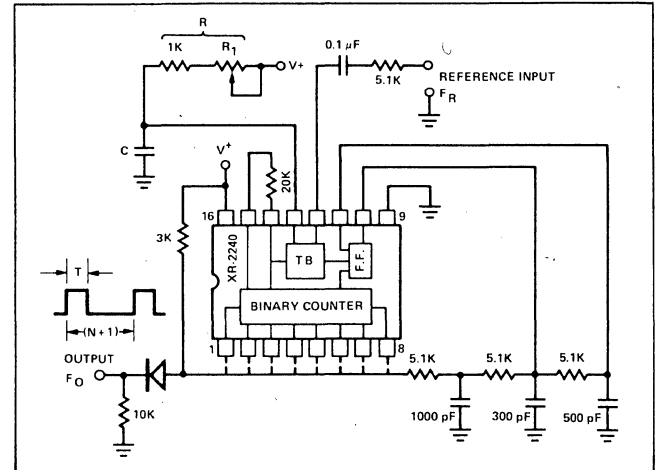


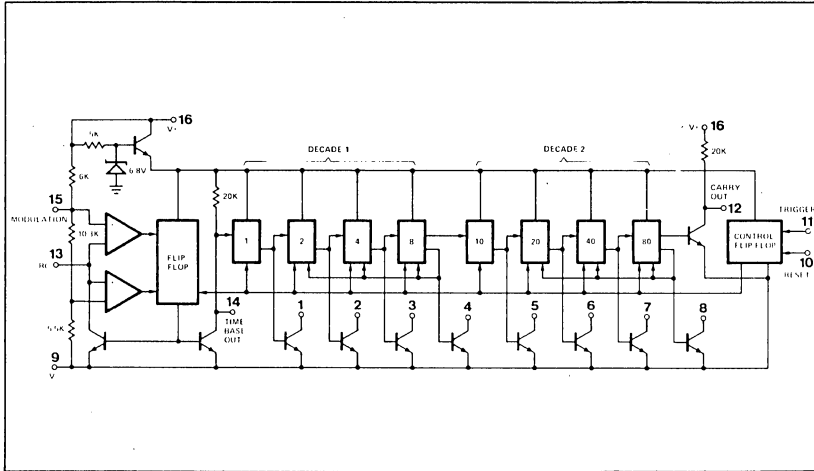
Figure 13. Frequency Synthesis by Harmonic Locking to an External Reference

One particular application of the circuit of Figure 13 is generating frequencies which are not harmonically related to a reference input. For example, by choosing the external R-C to set m = 10 and setting N = 5, one can obtain a 100 Hz output frequency synchronized to 60 Hz power line frequency.

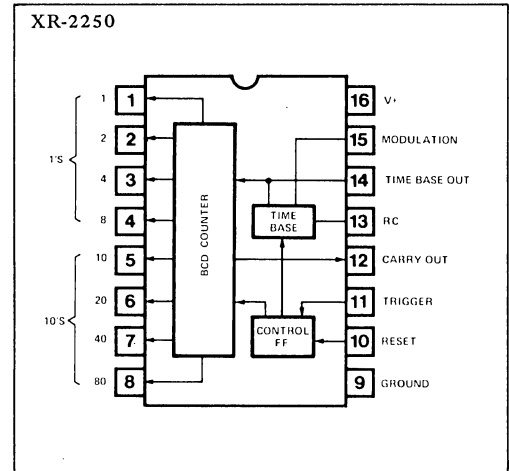
XR-2250 PROGRAMMABLE TIMER/COUNTER

The XR-2250 BCD Programmable Timer/Counter is a monolithic controller capable of producing ultra-long time delays without sacrificing accuracy. In most applications, it provides a direct replacement for mechanical or electromechanical timing devices and generates programmable time delays from micro-seconds up to 24 hours. Two timing circuits can be cascaded to generate time delays up to six months.

EQUIVALENT SCHEMATIC DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



XR-4136

XR-4212

EXAR INTEGRATED SYSTEMS, INC.

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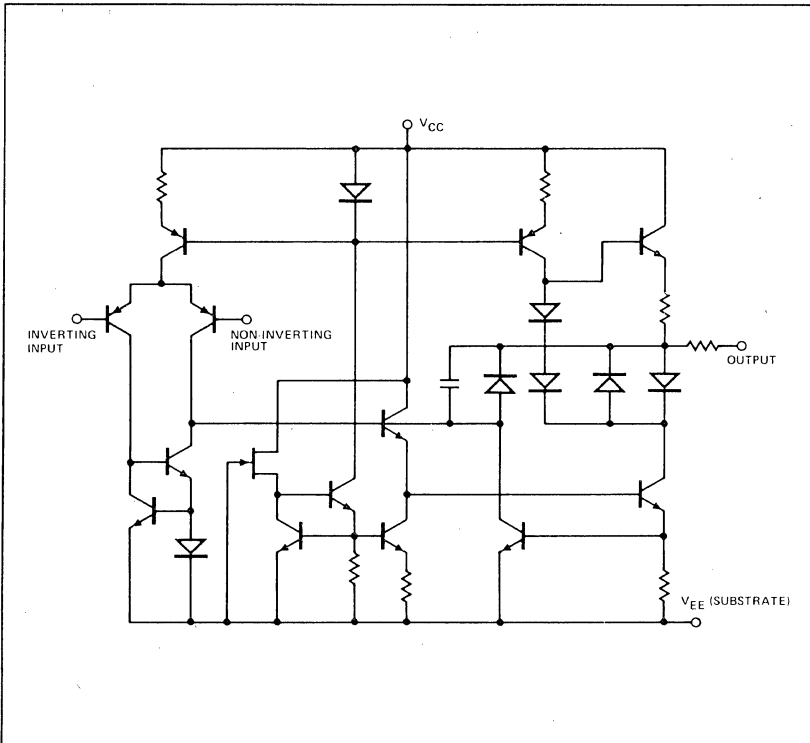


Quad Operational Amplifier

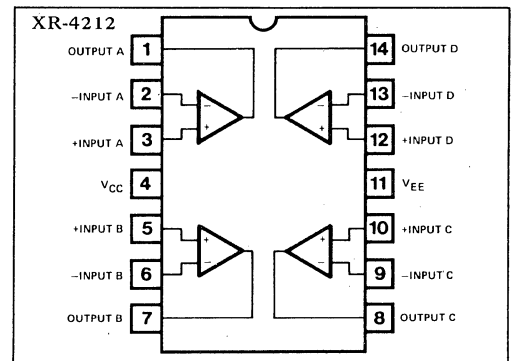
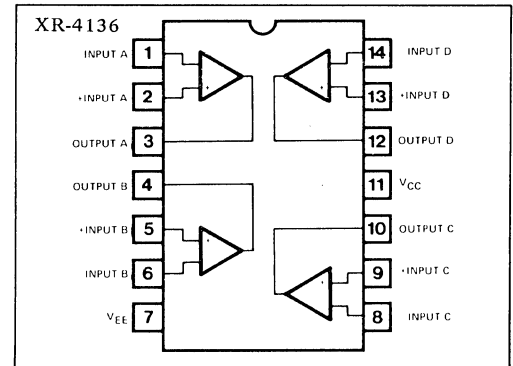
The XR-4136 is an array of four independent internally compensated operational amplifiers on a single silicon chip, each similar to the popular 741, but with a power consumption less than one 741. Good thermal tracking and matched gain-bandwidth products make these Quad Op-amps useful for active filter applications.

The XR-4212 is an array of four independent internally compensated operational amplifiers on a single silicon chip, each similar to the popular 741, but with a power consumption less than one 741. Good thermal tracking and matched gain-bandwidth products make these Quad Op-amps useful for active filter applications.

EQUIVALENT SCHEMATIC



FUNCTIONAL BLOCK DIAGRAM



CHARACTERISTICS	XR4136M/4212M			XR4136C/4212C			UNITS	SYMBOLS	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			
Input Offset Voltage		1	5.0		1	6.0	mV	$ V_{io} $	$R_S \leq 10\text{K}\Omega$
Input Offset Current		10	200		10	200	nA	$ I_{io} $	
Input Bias Current		80	500		80	500	nA	$ I_b $	
Input Resistance	0.3	1.8		0.3	1.8		M Ω	R_{in}	
Large Signal Voltage Gain	4136	50	60	20	40		V/mV	AVOL	$R_L \geq 2\text{K}\Omega$ $V_{out} = \pm 10\text{V}$
	4212	20	60	5	40				
Output Voltage Swing		± 12	± 14	± 12	± 14		V	V_{out}	$R_L \geq 10\text{K}\Omega$
		± 10	± 12	± 10	± 12		V	V_{out}	$R_L \geq 2\text{K}\Omega$
Input Voltage Range	± 12	± 13.5		± 12	± 13.5		V	V_{ICM}	
Common Mode Rejection Ratio	70	105		70	105		dB	CMRR	$R_S \leq 10\text{K}\Omega$
Supply Voltage Rejection Ratio		10	150		10	150	$\mu\text{V/V}$	PSRR	$R_S \leq 10\text{K}\Omega$
Power Consumption		50	120		50	120	mW	P_i	
Transient Response (unity gain)									$V_{in} = 20\text{mV}$ $R_L = 2\text{K}\Omega$ $C_L \leq 100\text{pF}$
	Risetime		0.07		0.07		μs	t_r	
Overshoot		20			20		%	t_o	
Unity Gain Bandwidth	2.0	3.0			3.0		MHz	BW	
Slew Rate (unity gain)		1.6			1.6		V/ μs	dV_{out}/dt	$R_L \geq 2\text{K}\Omega$
Channel Separation (open loop)		120			120		dB		$f = 10\text{KHz}$ $R_S = 1\text{K}\Omega$
	(Gain of 100)		105		105		dB		$f = 10\text{KHz}$ $R_S = 1\text{K}\Omega$

The following specifications apply for $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ for XR-4136M: $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ for XR-4136C

Input Offset Voltage			6.0			7.5	mV	$ V_{io} $	$R_S \leq 10\text{K}\Omega$
Input Offset Current			500			300	nA	$ I_{io} $	
Input Bias Current			1500			800	nA	I_b	
Large-Signal Voltage Gain	25			15			V/mV	AVOL	$R_L \geq 2\text{K}\Omega$ $V_{out} = \pm 10\text{V}$
Output Voltage Swing	± 10			± 10			V	V_{out}	$R_L \geq 2\text{K}\Omega$
Power Consumption			150			150	mW	P_i	$V_S = \pm 15\text{V}$
			200			200	mW	P_i	$T_A = \text{High}$ $T_A = \text{Low}$
Output Short-Circuit Current	5	17	35	5	17	35	mA	I_{SC}	

TYPICAL PARAMETER MATCHING:

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted

CHARACTERISTICS	XR4136M TYP.	XR4136C TYP.	UNITS	SYMBOLS	CONDITIONS
Input Offset Voltage	± 1.0	± 2.0	mV	$ V_{io} $	$R_S \geq 10\text{K}\Omega$
Input Offset Current	± 7.5	± 7.5	nA	$ I_{io} $	
Input Bias Current	± 15	± 15	nA	I_b	
Voltage Gain	± 0.5	± 1.0	dB	AVOL	$R_S \geq 2\text{K}\Omega$

XR-4202

Programmable Quad Operational Amplifier

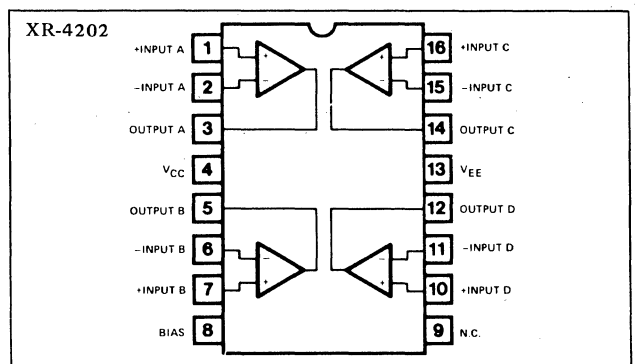
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750 Palomar Ave., Sunnyvale, CA 94086 Sales: (408) 733-7700



FEATURES

- Programmable
- Micropower Operation
- Wide Input Voltage and Common Mode Range
- Internal Frequency Compensation
- No Latch-Up
- Matched Parameters
- Short-Circuit Protection

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS HIGH POWER MODE ($V_S = \pm 15V$, $I_{SET} = 75 \mu A$ and $T_A = +25^\circ C$ unless otherwise specified)

CHARACTERISTICS	MIN	TYP	MAX	UNITS	SYMBOL	CONDITIONS
Short Circuit Current	5	17	30	mA	I_{SC}	$0^\circ C \leq T_A \leq 75^\circ C$
Supply Current	0.8	1.7	4.0	mA	I_S	Note 3
Input Offset Voltage		0.8	5.0	mV	V_{io}	$R_S \leq 10 K\Omega$
Input Bias Current		80	500	nA	I_b	
Input Off-set Current		10	50	nA	I_{jo}	
Input Resistance	0.1	0.6		M Ω	R_{in}	
Input Common Mode Voltage Range	12	± 14		$\pm V$	V_{iCM}	
Common Mode Rejection Ratio	70	110		dB	CMRR	
Voltage Supply Rejection Ratio		15	150	$\mu V/V$	PSRR	
Large Signal Voltage Gain	74	88		dB	A_{VOL}	$R_L = 3 K\Omega$; $\Delta V_O = \pm 10V$
Output Voltage Swing	± 10	± 13.6		$\pm V$	V_{out}	$R_L = 3 K\Omega$
Gain-Bandwidth Product		3.5		MHz	f_1	
Phase Margin		45		Deg.		
Rise Time		70		ns	t_R	$\Delta V_O = \pm 20 mV$
Overshoot		20		%	t_o	$\Delta V_O = \pm 20 mV$
Channel Separation		120		dB		Any amp. pair: freq. = 1 Hz, $R_L = 3 K\Omega$
		105		dB		Any amp. pair: freq. = 10 KHz, $R_L = 3 K\Omega$
Slew Rate		1.5		V/ μs	dV_{out}/dt	
Input Voltage Noise		25		nV/ \sqrt{Hz}	e_n	Bandwidth 100 Hz to 10 KHz

Note: Short circuit may be taken to either supply line or ground on only one amplifier at a time.

ELECTRICAL CHARACTERISTICS MICROPOWER MODE ($I_{SET} = 1 \mu A$, $V_S = \pm 1.5V$)

CHARACTERISTICS	MIN	TYP	MAX	UNITS	SYMBOL	CONDITIONS
Supply Current	20		40	μA	I_S	Note 3
Input Bias Current			100	nA	I_B	
Input Offset Current			10	nA	I_{OS}	
Input Offset Voltage		0.5	5	mV	V_{OS}	$R_S \leq 10 K\Omega$
Input Resistance	0.5			M Ω	R_{in}	
Input Common Mode Voltage Range	0.3	± 0.8		$\pm V$	V_{iCM}	
Common Mode Rejection Ratio	60	100		dB	CMRR	
Voltage Supply Rejection Ratio		20	200	$\mu V/V$	PSRR	
Large Signal Voltage Gain	66	80		dB	A_{VOL}	$R_L \geq 100 K\Omega$
Gain-Bandwidth Product		50		KHz	f_1	
Phase Margin		75		Deg.		
Slew-Rate		20		V/ms	dV_{out}/dt	
Rise Time		7		μs	t_R	$\Delta V_O = \pm 20 mV$
Overshoot		0		%	t_o	$\Delta V_O = \pm 20 mV$
Channel Separation		120		dB		Freq. = Hz: $R_L = 20 K\Omega$, $\Delta V_O = \pm 0.5V$
		120		dB		Freq. = 1 KHz: $R_L = 10 K\Omega$, $\Delta V_O = \pm 0.5V$
Equivalent Input Voltage Noise		200		nV/ \sqrt{Hz}	e_n	Bandwidth = 100 Hz to 10 KHz

PARAMETER MATCHING ($I_{SET} = 75 \mu A^{(2)}$)

CHARACTERISTICS	MIN	TYP	MAX	UNITS	SYMBOL	CONDITIONS
Input Offset Voltage		1		$\pm mV$	V_{OS}	$R_S \leq 10 K\Omega$
Input Bias Current		10		$\pm nA$	I_B	
Input Offset Current		2		$\pm nA$	I_{OS}	
Gain-Bandwidth Product		100		$\pm KHz$	f_1	
Slew Rate		0.2		$\pm V/\mu s$	dV_O/dt	

NOTES:

1. All tests refer to a single Op. amp unless otherwise specified.
2. Tests apply for parameter matching between any Op. amp pair.
3. Tests apply to four Op. amps and bias network.

EXAR-CHIP

Custom IC Design Kit

EXAR INTEGRATED SYSTEMS, INC.
750 Palomar Ave., Sunnyvale, CA 94086 Sales: (408) 733-7700



HOW THE XR-CHIP PROGRAM WORKS:

The XR-CHIP design approach involves only 6 simple steps, from the beginning of circuit design to completion of monolithic prototypes. The first three of these steps is done by the customer in consultation with Exar; the last three are performed by Exar:

Step 1

Customer designs and breadboards his circuit using XR-CHIP kit.

Customer purchases the XR-Chip Design Kit, made up of XR-Chip Instruction Manual and 33 monolithic kit parts or building blocks. Customer then breadboards his circuit and evaluates its performance using these kit parts. The electrical characteristics of kit parts are virtually identical to those which will be on the finished IC chip. Thus, this stage provides a true simulation of final IC performance.

Step 2

Customer does circuit layout.

After completion of breadboard evaluation, customer prepares a layout of the circuit on the selected XR-Chip by following the basic layout rules given in XR-Chip Instruction Manual. The layout is done simply by interconnecting appropriate device terminals with pen or pencil lines on oversize drawings of the XR-Chips supplied with the kit.

NOTE: As an option, Exar also offers a layout service, at a nominal charge.

Step 3

Submit layout to Exar for review:

Exar reviews the circuit layout and schematic to check:

- a) That basic circuit function is feasible
- b) No layout rules are violated
- c) Circuit layout accurately represents the circuit schematic.

NOTE: Steps 1, 2, and 3 are done at *no cost* to the customer, except for the nominal cost of the XR-Chip design kit. Exar offers free consulting service and design advice during these first three steps. The "formal" part of the program is initiated at the completion of Step 3.

Step 4

Exar generates custom interconnection pattern.

Using the XR-Chip circuit layout supplied by the customer, Exar generates a custom interconnection pattern, or "metal mask" to be applied to pre-fabricated XR-Chip wafers.

Step 5

Exar fabricates customized IC wafers.

Exar applies the custom interconnection patterns to pre-fabricated XR-Chip wafers. These wafers are then tested for semiconductor device characteristics (such as resistor values, diode and transistor characteristics) using special "test-patterns" etched on the wafer. The wafers are then accepted as a "qualified wafers" if these device parameters are within the specified limits (see Table of Electrical Characteristics listed on pages 6 and 7).

Step 6

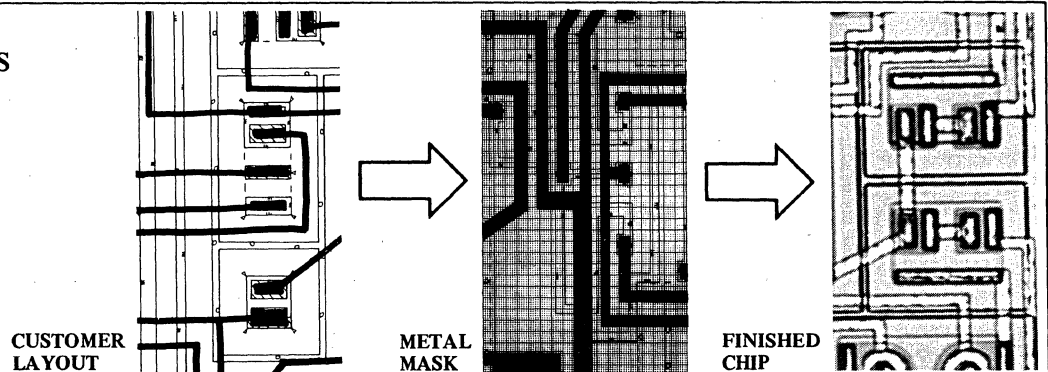
Exar assembles and delivers monolithic prototypes.

The customized IC wafers are scribed or cut into individual IC chips. After a visual inspection, a number of these custom IC chips are assembled in dual-in-line IC packages and delivered to the customer for electrical evaluation, to conclude the program.

In addition to the monolithic prototype IC's, the following technical information is also delivered to the customer:

- a) A computer printout of device characteristics measured in Step 5, using special "test-patterns" on the IC wafers.
- b) An enlarged photo-micrograph of the finished IC chip showing the custom interconnection pattern.

METAL MASK FABRICATION STEPS



Exar

LINEAR

ANSWERS TO MOST FREQUENTLY ASKED QUESTIONS:

Based on our long experience with the XR-Chip, we have compiled a comprehensive glossary of the "most often asked questions" concerning the program. The following is a list of these questions and their answers:

WHAT IS THE COST OF THE BASIC PROGRAM?

The approximate cost of the basic 6-step XR-Chip program as outlined on Page 3, is in the range of \$1,500 to \$2,200, depending on circuit complexity. The above prices also include the cost of 50 monolithic prototypes delivered at the completion of the program.

Additional untested prototypes for evaluation are available at a cost of \$3.50 each, in minimum quantities of 100 units. These cost examples are for budgetary purposes only, and are subject to change without notice.

WHAT IS THE DEVELOPMENT TIME?

Typical development time for the basic XR-Chip program, starting with the customer's XR-Chip layout and ending with the monolithic prototypes is *four to six* weeks.

WHAT IF ADDITIONAL DESIGN CYCLES ARE NEEDED?

Upon evaluation of 50 monolithic prototypes, if the customer desires to modify the design or the layout, a complete design iteration cycle can be completed within *four* weeks, starting with the modified layout and ending with 50 prototypes of the *modified* design. Typical cost of additional design cycles or iterations is \$1,000 per design cycle, including the cost of 50 additional prototypes.

IS THERE A SECOND-SOURCE FOR XR-CHIP IC'S?

In most high-volume production applications of IC's, the customer often requires more than one supplier of a given IC. Anticipating this "alternate-source" requirement, Exar has made contractual agreements with other IC manufacturers to provide a second-source for the XR-Chip custom IC's.

In addition, the XR-A100 and the XR-B100 chips of the XR-Chip product family are direct replacements for the "Monochip A" and the "Monochip B" products manufactured by Interdesign, Inc. of Sunnyvale, California.

WHAT ABOUT PRODUCTION PRICING?

The production pricing of monolithic IC's depend on three key factors:

- Circuit complexity (i.e., yield)
- Quantity
- Package type

In the case of a custom IC, it is impossible to anticipate the impact of these factors in advance, since each custom IC by definition, has some unique requirement or feature associated with it. However, based on experience, typical unit prices associated with a fully-tested medium complexity XR-Chip IC in 14- or 16-pin plastic dual-in-line package are in the range of \$3.50 at 1,000 piece-level; decreasing to \$2.00 at 10,000-piece level; and to \$1.20 at 100,000-piece level.

The above price estimates are for budgetary purposes only. After reviewing the circuit performance and quantity requirements, Exar shall provide the customer with a detailed proposal outlining the cost breakdown and production pricing for a given circuit.

CAN EXAR DO THE IC LAYOUT?

Exar also offers a circuit layout service to translate the customer's circuit schematic into an XR-Chip layout. Essentially, this corresponds to the "Step 2" of the 6-step XR-Chip program, outlined on page 3. The cost of this layout service is in the range of \$400 to \$1,000, depending on complexity.

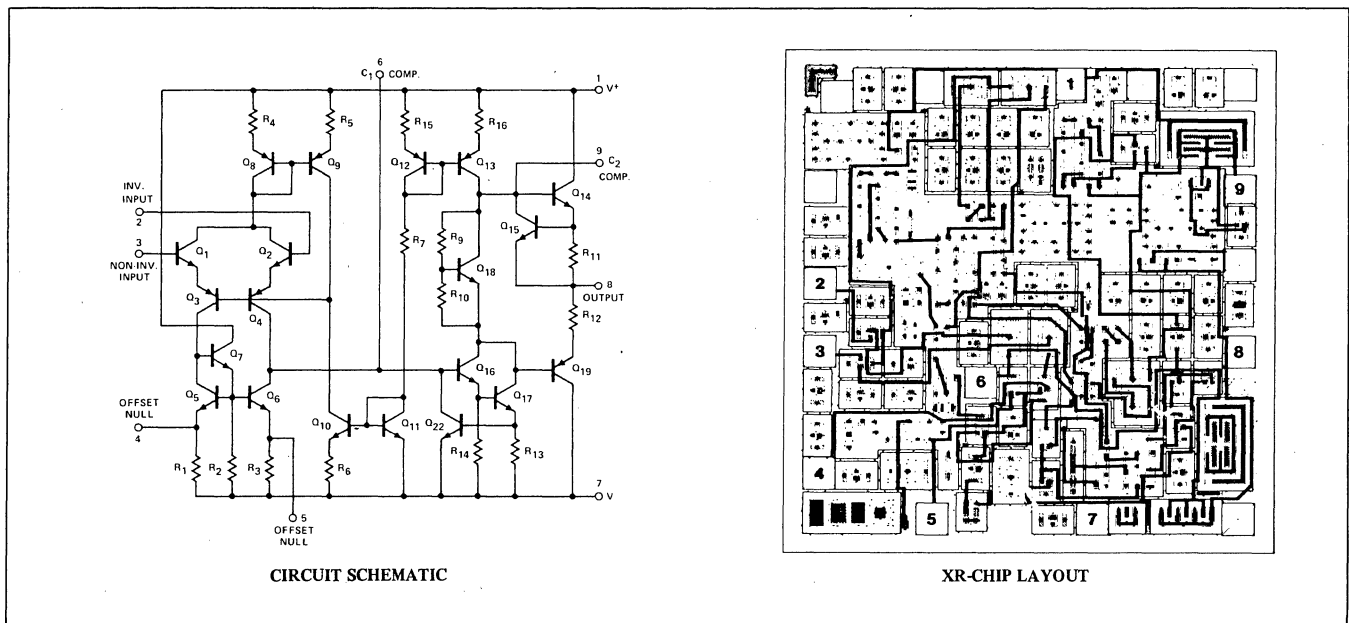
DOES EXAR HAVE OTHER XR-CHIPS FOR SPECIAL APPLICATIONS?

Exar also has over twenty different types of monolithic IC chips which have been originally developed as standard IC products. Many of these chips contain additional device types, such as high-current or high-voltage transistors and MOS capacitors. Some of these are shown on page 8.

Any one of these monolithic chips can also be used as a part of the XR-Chip program, by simply applying a custom metal interconnection pattern to it. For example, if a given circuit configuration does not fit on the conventional XR-A100, -B100, or -C100 chips because of lack of appropriate device types, such a circuit may still be fitted on any one of these twenty other chips available from Exar.

For further information on these additional XR-Chips and their characteristics, contact your Exar representative, or Exar Applications Department.

DESIGN EXAMPLE USING EXAR-CHIP APPROACH



XR-CHIP CUSTOM DESIGN KIT CONTENTS

ITEM	PART NO.	DESCRIPTION	KIT QUAN.	DEVICES PER ARRAY
1	XR-B101	Small Signal NPN Transistor Array	8	5
2	XR-B102	PNP Transistor Array	2	5
3	XR-C101	Small Signal NPN Transistor Array	8	5
4	XR-C102	PNP Transistor Array	2	5
5	XR-C103	Special Purpose NPN Transistors	4	5
6	XR-C104	Small Value Resistors	5	10
7	XR-C105	Large Value Resistors	3	8
8	XR-C106	Functional Building Blocks	1	3
		Total Arrays	33	
9		Design Manual	1	-

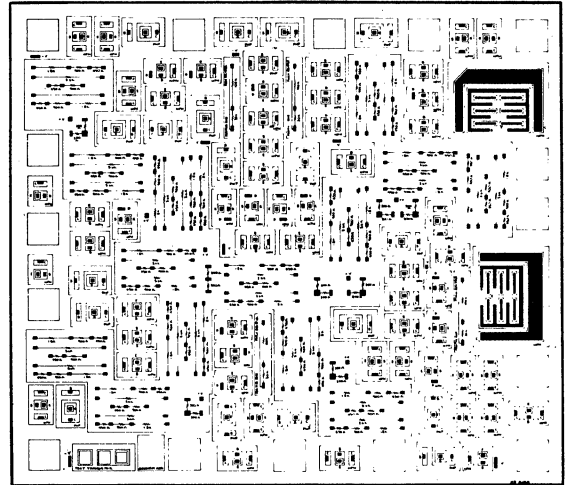
- Notes:
1. B-101 and B-102 arrays are suitable only for A-100 and B-100 Chips.
 2. C-101 and C-102 arrays are suitable only for C-100 Chip. However, substrate PNP transistors in C-102 are also available in A-100 Chip.
 3. C-103 thru C-106 devices are suitable for both B-100 and C-100 Chips.

TABLE OF COMPONENTS ON XR-CHIPS

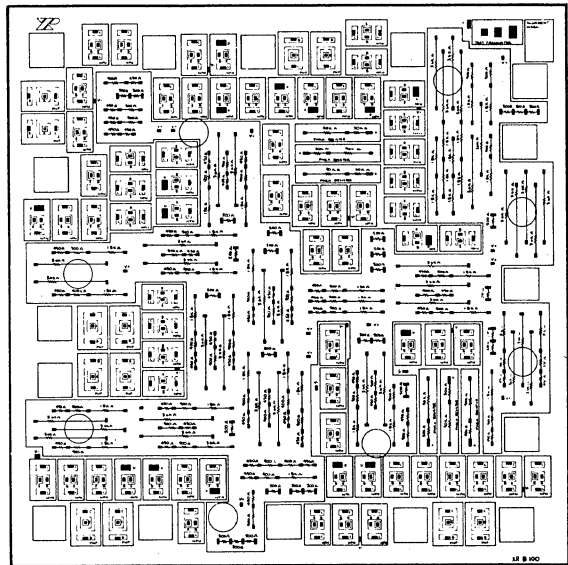
COMPONENT TYPE	A-100	B-100	C-100
Small NPN Transistors	58	53	46
Small NPN Transistors/Common Collector			8
Small NPN Transistor w/Schottky Diodes	15	16	3
100 mA NPN Transistors			2
200 mA NPN Transistors	2		
Lateral PNP Transistors	18	12	8
Vertical PNP			2
Resistors 50 Ohms			4
Resistors 100 Ohms			4
Resistors 150 Ohms			10
Resistors 200 Ohms	16	27	10
Resistors 400 Ohms			30
Resistors 450 Ohms	43	44	
Resistors 800 Ohms			29
Resistors 900 Ohms	43	46	
Resistors 1.6k Ohms			20
Resistors 1.8K	29	39	
Resistors 3.2K Ohms	29		15
Resistors 3.6K	28	39	
Resistors 5K			4
Resistors 30K Ohms Pinch	4	6	5
Resistors 100K Ohms Pinch	4	6	1
Maximum Number of Bonding Pads	16	24	19
+ V Contacts	7	12	10
- V Contacts	8	14	13
Component Total	260	288	201
Chip Size (Mils)	83x73	85x85	76x78

XR-CHIP LAYOUTS

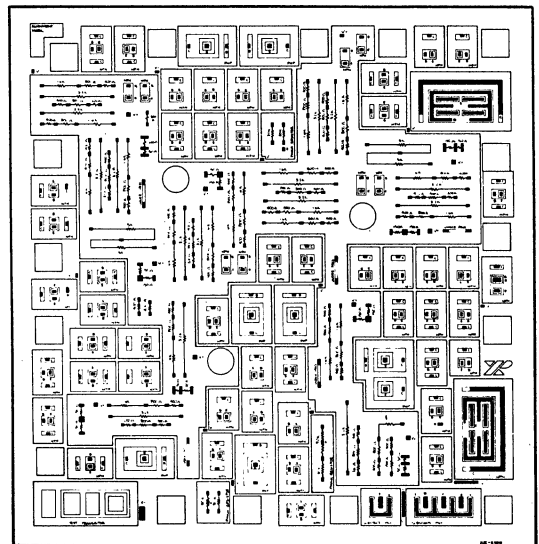
XR-A100



XR-B100



XR-C100



ELECTRICAL CHARACTERISTICS OF EXAR CHIP COMPONENTS

The following tables list the electrical characteristics of active and passive circuit components available on the XR-A100, XR-B100 and the XR-C100 custom IC chips. Whenever applicable, the worst-case tolerances and the parameter distributions are also listed. The parameter distributions are given in terms of the anticipated "Standard-deviation," σ .

1. Small NPN Transistors

Parameter	Typical Values
Current gain (h_{FE}) @ 1 mA, 5V	180
Temperature Coefficient of h_{FE} -55°C to 25°C	+0.5%/°C
25°C to 125°C	+1%/°C
Matching of h_{FE}	-
Breakdown voltage (LV_{CEO}) A-100/B-100	23V
C-100	27V
Collector-Base Leakage Current @ 20V	1 nA
Cutoff Frequency (f_T)	500 MHz
Storage Time (t_s)	50 nsec
Saturation Resistance One collector contact	100 Ohms
Two collector contact	50 Ohms

2. Large NPN Transistors (A-100/C-100 only)

Parameter	Typical Values
Current Gain (h_{FE}) @ 1 mA, 5V	180
@ 100 mA, 5V	100
Temperature Coefficient of h_{FE} -55°C to 25°C	+0.5%/°C
25°C to 125°C	+1%/°C
Matching h_{FE}	-
Breakdown Voltage (LV_{CEO})	27V
Collector-Base Leakage Current @ 20V	20 nA
Cutoff Frequency (f_T)	100 MHz
Storage Time (t_s)	200 nsec
Saturation Resistance	5 Ohms

3. Lateral PNP Transistors (All XR-Chips)

Parameters	Typical Values
Current Gain (h_{FE}) @ 100 μ A, 5V	20
Temperature Coefficient of h_{FE}	$\pm 0.1\%/^\circ\text{C}$
Matching of h_{FE}	-
Breakdown Voltage (LV_{CEO})	40V
Collector-Base Leakage Current @ 20V	5 nA
Cutoff Frequency (f_T)	5 MHz
Storage Time (t_s)	500 nsec
Saturation Resistance	600 Ohms

4. Vertical PNP Transistors (C-100 only)

Parameters	Typical Values
Current Gain (h_{FE}) @ 1 mA, 5V	20
Breakdown Voltage @ 150 μ A (LV_{CEO})	35V
Cutoff Frequency (f_T)	15 MHz

5. Transistors connected as diodes (collector and base shorted)

Parameters	Typical Values
Small NPN (All XR-Chips)	
Reverse Breakdown Voltage	6.7V
Forward Voltage Drop @ 1 mA, 25°C	0.74V
Forward Voltage Matching	-
Forward Voltage Tracking	-
Large NPN (A-100 and C-100 only)	
Reverse Breakdown Voltage	6.7V
Forward Voltage Drop @ 100 mA, 25°C	0.62V
Forward Voltage Matching	-
Forward Voltage Tracking	-
Lateral PNP (All XR-Chips)	
Reverse Breakdown Voltage	40V
Forward Voltage Drop @ 200 μ A, 25°C	0.70V
Forward Voltage Matching	-
Forward Voltage Tracking	-

6. NPN Base-Emitter Junctions used as Zener Diodes

Parameters	Typical Values
Small NPN Transistors	
A-100/B-100	
Breakdown Voltage @ 10 μ A	6.3V
@ 100 μ A	6.35V
@ 1 mA	6.45V
Temperature Co-Efficient @ 10 μ A	+2.4 mV/°C
@ 100 μ A	+2.5 mV/°C
@ 1 mA	+2.5 mV/°C
C-100	
Breakdown Voltage @ 10 μ A	6.68V
@ 100 μ A	6.75V
@ 1 mA	6.80V
Temperature Co-Efficient @ 10 μ A	+2.4 mV/°C
@ 100 μ A	+2.45 mV/°C
@ 1 mA	+2.5 mV/°C

7. Schottky-Barrier Diodes (All XR-Chips)

Parameters	Typical Values
Forward Voltage Drop @ 10 μ A	0.28V
Temperature Co-Efficient of Forward Voltage Drop	-1.5 mV/°C
Reverse Breakdown Voltage	30V
Leakage Current @ 20V	200 nA

8. Diffused Resistors (All XR-Chips)

Parameters	Typical Values
Absolute Values	-
Temperature Co-Efficients -55°C to -25°C	-650 ppm/°C
-25°C to 0°C	+150 ppm/°C
0°C to 25°C	+680 ppm/°C
25°C to 75°C	+1040 ppm/°C
75°C to 125°C	+1400 ppm/°C
Matching between resistors	
Identical values	-
200 - 450	-
200 - 900	-
200 - 1.8K	-
200 - 3.6K	-
450 - 900	-
450 - 1.8K	-
450 - 3.6K	-
900 - 1.8K	-
900 - 3.6K	-
1.8K - 3.6K	-

9. Typical capacitances (in pF) for the various junctions in Exar Chip.

	1V	5V
Small NPN Transistors		
Collector-Base	1.2 pF	0.85 pF
Emitter-Base	1.0	0.65
Collector-Substrate	1.5	1.2
Large NPN Transistors		
Collector-Base	7.5	6.3
Emitter-Base	12.5	9.9
Collector-Substrate	9.5	8.1
Lateral PNP Transistors		
Collector-Base	2.5	2.1
Emitter-Base	1.5	1.3
Base-Substrate	1.8	1.4
Schottky-Barrier Diodes		
Metal to N-layer	0.6	0.4
Resistors		
200 Ohms	1.2	0.85
450 Ohms	0.2	0.13
900 Ohms	0.4	0.28
1.8K Ohms	0.7	0.5
3.6K Ohms	1.5	1.0
Pinch	1.5	1.2



Custom I²L Design Kit

With the XR-400K I²L Design Kit, Exar now offers a unique method of manufacturing an almost unlimited variety of custom *linear* and *digital* circuits using I²L technology with greatly reduced cost and development time. Exar makes this possible by stocking I²L silicon wafers that are completely built except for the final process step of device interconnection. These pre-fabricated wafers are then customized by application of *two* additional "masking" steps, one to open the contact windows on the chip, and one to form the desired metal interconnection pattern.

WHAT IS THE EXAR I²L DESIGN KIT?

Exar's XR-400K I²L Design Kit is made up of 30 monolithic I²L logic blocks and bipolar transistor arrays. These monolithic IC's or "kit parts" comprise the basic building blocks for complex analog or digital LSI systems. The XR-400K I²L Design Kit also contains a comprehensive "Design and Applications Manual" which enables the kit user to breadboard his system with I²L logic, and develop his own custom LSI circuit.

The XR-400K I²L Design Kit contains all the basic building blocks used in system design, such as:

- I²L Gate Arrays
- I²L Flip/Flop and Counter Arrays
- Latches and Shift Registers
- TTL/I²L Input/Output Interface Circuits
- Bipolar NPN/PNP Transistor Arrays

The heart of the Exar I²L Design Kit is the XR-400 Master Chip, which contains a logic matrix made up of over 1000 I²L transistors and more than 200 conventional bipolar transistors and resistors. All of the logic building blocks, or kit parts, which comprise the Exar I²L Design Kit are derived from the XR-400 Master Chip, with different metal interconnection patterns. Thus, the performance of the circuit components in the Exar I²L Design Kit are virtually identical to those on the XR-400 Master Chip.

Once a complex analog or digital system is breadboarded using the I²L Design Kit components, Exar can convert the entire design into a monolithic custom LSI by applying a custom interconnection pattern to the XR-400 Master Chip. The availability of the I²L Design Kit allows the system designer to design and develop his custom I²L LSI at a fraction of the development cost and time associated

TABLE OF COMPONENT
XR-400 I²L MASTER CHIP

COMPONENT TYPE	QUANTITY
Quad I ² L Gates	256
High-Freq. I ² L Gates	16
Input/Output Buffers	23
Bipolar Transistors	103
Resistors	120
Under-passes	210
Bonding Pads	40
Chip Size	110 x 110 mils

with conventional custom IC programs. If the complexity of the LSI system exceeds the capability of the XR-400 Master Chip, then Exar can develop a complete custom design, using the I²L Kit components as "cells" in generating a full-custom LSI design.

EXAR'S CUSTOM I²L PROGRAM

Exar's custom I²L LSI program is based on the XR-400K design kit and the XR-400 Master Chip. The basic development program involves only 7 simple steps. The first four of these steps is done by the customer, using the I²L Design Kit, in consultation with Exar:

- Step 1: Customer designs and breadboards his system using I²L Design Kit.
- Step 2: Customer, in consultation with Exar, evaluates design feasibility.
- Step 3: Customer prepares circuit layout of his system on XR-400 Master Chip following basic instructions given in I²L Design Kit manual. Layout is done simply by interconnecting appropriate device terminals with pencil lines on oversize drawings of XR-400 chips.

NOTE: As an option, Exar offers layout service at nominal charge.

- Step 4: Customer submits his layout to Exar for final review.

NOTE: Steps 1, 2, 3 and 4 are done with no cost from EXAR to customer. The formal part of the program is initiated at the completion of Step 4.

- Step 5: Exar generates custom "contact" and "interconnection" patterns to be applied to pre-fabricated XR-400 wafers.
- Step 6: Exar fabricates customized I²L wafers from XR-400 chip, using tooling generated in Step 5.
- Step 7: Exar assembles and delivers monolithic prototypes of custom IC to complete the program.

ADDITIONAL INFORMATION ON EXAR'S CUSTOM I²L PROGRAM

Development Cost:

Typical development costs for initial prototypes are in the range of \$3,500 to \$5,000.

Development Time:

Typical development time to complete steps 5, 6 and 7 of development program is 8 weeks.

Additional Design Cycles:

If additional design cycles are needed, the typical cost is \$1,500 to \$2,000 per design iteration, which includes the cost of additional prototypes.

Layout Services:

Exar can perform the circuit layout (step 3) at a nominal charge of \$1,000 to \$2,000 depending on complexity.

Full Custom Design:

If the circuit complexity is in excess of the capability of XR-400 Master Chip, Exar can tool-up for a full-custom IC layout and design. In this case, the I²L kit parts used in circuit breadboarding get used as logic "cells" in the circuit layout. Typical full-custom design and fabrication cycle takes about 16 to 20 weeks.

QUAD 741 HIGH-GAIN OPERATIONAL AMPLIFIERS

4136

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	RM4136: $\pm 22V$ RC4136: $\pm 18V$
Internal Power Dissipation (Note 1)	800mW
Differential Input Voltage	$\pm 30V$
Input Voltage (Note 2)	$\pm 15V$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature Range	RM4136: $-55^{\circ}C$ to $+125^{\circ}C$ RC4136: $0^{\circ}C$ to $+70^{\circ}C$
Lead Temperature (Soldering, 60s)	$300^{\circ}C$
Output Short-Circuit Duration (Note 3)	Indefinite

ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}C$, $V_{CC} = \pm 15V$, unless otherwise specified)

PARAMETER	CONDITIONS	RM4136			RC4136			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10\text{ k}\Omega$		0.5	5.0		0.5	6.0	mV
Input Offset Current			5.0	200		5.0	200	nA
Input Bias Current			40	500		40	500	nA
Input Resistance		0.3	5.0		0.3	5.0		M Ω
Large-Signal Voltage Gain	$R_L \geq 2\text{ k}\Omega$ $V_{out} = \pm 10V$	50,000	300,000		20,000	300,000		
Output Voltage Swing	$R_L \geq 10\text{ k}\Omega$	± 12	± 14		± 12	± 14		V
	$R_L \geq 2\text{ k}\Omega$	± 10	± 13		± 10	± 13		V
Input Voltage Range		± 12	± 14		± 12	± 14		V
Common Mode Rejection Ratio	$R_S \leq 10\text{ k}\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\text{ k}\Omega$		30	150		30	150	$\mu V/V$
Power Consumption			210	340		210	340	mW
Transient Response (unity gain) Risetime	$V_{in} = 20\text{ mV}$ $R_L = 2\text{ k}\Omega$ $C_L \leq 100\text{ pF}$		0.13			0.13		μs
Transient Response (unity gain) Overshoot	$V_{in} = 20\text{ mV}$ $R_L = 2\text{ k}\Omega$ $C_L \leq 100\text{ pF}$		5.0			5.0		%
Unity Gain Bandwidth		2.0	3.0			3.0		MHz
Slew Rate (unity gain)	$R_L \geq 2\text{ k}\Omega$		1.5			1.0		V/ μs
Channel Separation (open loop) (Gain = 100)	$f = 10\text{ kHz}$ $R_S = 1\text{ k}\Omega$		105			105		dB
	$f = 10\text{ kHz}$ $R_S = 1\text{ k}\Omega$		105			105		dB

The following specifications apply for $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ for RM4136; $0^{\circ}C \leq T_A \leq +70^{\circ}C$ for RC4136.

Input Offset Voltage	$R_S \leq 10\text{ k}\Omega$			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1500			800	nA
Large-Signal Voltage Gain	$R_L \geq 2\text{ k}\Omega$ $V_{out} = \pm 10V$	25,000				15,000		
Output Voltage Swing	$R_L \geq 2\text{ k}\Omega$	± 10				± 10		V
Power Consumption	$V_S = \pm 15V$							
	$T_A = \text{High}$		180	300		180	300	mW
	$T_A = \text{Low}$		240	400		240	400	

NOTES:

- Rating applies for ambient temperature of $+25^{\circ}C$; derate linearly at $6.4\text{ mW}/^{\circ}C$ for ambient temperatures above $+25^{\circ}C$.
- For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.
- Short-circuit may be to ground, one amplifier only. $I_{sc} = 45\text{mA}$ (typical).



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DESIGN FEATURES

- Unity Gain Bandwidth 3MHz
- Continuous Short Circuit Protection
- No Frequency Compensation Required
- No Latch-up
- Large Common Mode and Differential Voltage Ranges
- Low Power Consumption
- Parameter Tracking Over Temperature Range
- Gain and Phase Match Between Amplifiers

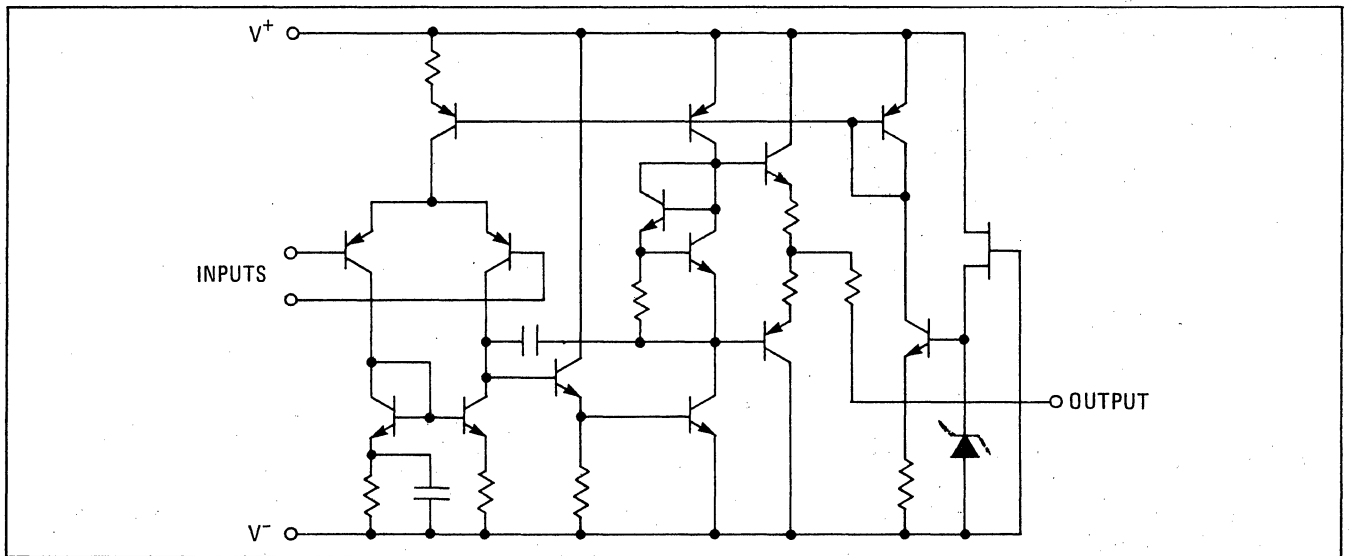
The RM4136/RC4136 include four independent high gain operational amplifiers internally compensated and constructed on a single silicon chip using the planar epitaxial processes.

These amplifiers meet or exceed all specifications for 741 type amplifiers. Excellent channel separation allows the use of the 4136 quad amplifier in all 741

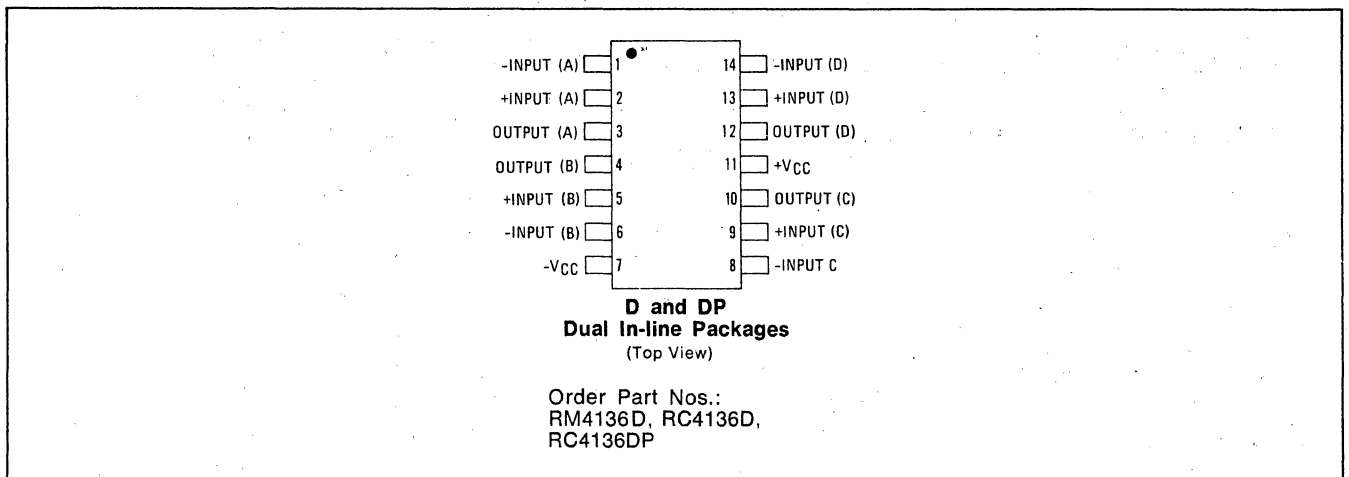
operational amplifier applications providing the highest possible packaging density.

The specially designed low noise input transistors allow the 4136 to be used in low noise signal processing applications such as audio preamplifiers and signal conditioners.

SCHEMATIC DIAGRAM



CONNECTION INFORMATION



TOTAL QUAD OPERATIONAL AMPLIFIER

3403A
3503A

Raytheon Semiconductor

LINEAR

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V^+	36V or $\pm 18V$
Differential Input Voltage	36V
Input Voltage	-0.3V to +36V
Power Dissipation	
"DB" package	500mW (molded DIP epoxy "B")
"DC" package	650mW (hermetic DIP)
Operating Temperature Range	
RM3503A	-55°C to +125°C
RC3403A	0°C to +70°C
RV3403A	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V$ and $T_A = 25^\circ C$ unless otherwise specified

PARAMETER	CONDITIONS	RM3503A			RC/RV3403A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S = 0\Omega$		2	4		2	6	mV
Input Bias Current	I_{in-} or I_{in+}		-150	-400		-150	-500	nA
Input Offset Current	I_{in-} or I_{in+}		± 30	± 50		± 30	± 50	nA
Input Common Mode Voltage Range		0		$V^+ - 2$	0		$V^+ - 2$	V
Supply Current	$R_L = \infty$ on all op-amps		3	4		3	5	mA
Large Signal Voltage Gain	$R_L > 2k\Omega$	50	100		25	100		V/mV
Output Voltage Swing	$R_L = 2k\Omega$	± 10	± 13		± 10	± 13		V
Common Mode Rejection Ratio	DC	70	90		70	90		dB
Channel Separation	± 1 kHz to 20 kHz (in ref)		-120			-120		dB
Output Source Current	$V_{IN+} = 1V, V_{IN-} = 0V$	20	40		20	40		mA
Output Sink Current		10	20		10	20		mA
Small Signal Bandwidth			1			1		MHz
Slew Rate	$A_v = 1, -10 < V_i < +10$		1.2			1.2		V/ μs
Distortion (crossover)	$f = 20$ kHz, $V_O = 10V_{pp}$		1			1		%
Power Bandwidth	$V_O = 10V_{pp}$		40			40		kHz
Power Supply Rejection Ratio			20	50		20	100	$\mu V/V$

LOW VOLTAGE ELECTRICAL CHARACTERISTICS $V_{CC} = +5V, V_{EE} = GND, T_A = 25^\circ C$ unless otherwise noted

PARAMETER	CONDITIONS	RM3503A			RC/RV3403A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S = 0\Omega$		2.0	5.0		2.0	10	mV
Input Bias Current	$I_{in-} + I_{in+} / 2$		-150	-500		-150	-500	nA
Input Offset Current	$I_{in-} - I_{in+}$		30	50		30	50	nA
Supply Current	$R_L = \infty$ all amplifiers		2.5	4.0		2.5	5.0	mA
Large Signal Voltage Gain	$R_L = 2k\Omega$	20	200		20	200		V/mV
Output Voltage Range ¹	$R_L = 10k\Omega$	3.5			3.5			V_{p-p}
Channel Separation	1 kHz $\leq F \leq 200$ kHz (input referred)		-120			-120		dB
Power Supply Rejection Ratio				50			150	$\mu V/V$

¹ Output will swing to ground.

ELECTRICAL CHARACTERISTICS GUARANTEED OVER TEMPERATURE

$V_{CC} = \pm 15V$

Range: RM3503A -55°C to +125°C
RC3403A 0°C to +70°C
RV3403A -40°C to +85°C

Raytheon reserves the right to change these specifications without notice.

PARAMETER	CONDITIONS	RM3503A		RC3403A		RV3403A		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Input Offset Voltage	$R_S = 0\Omega$		6.0		10.0		10.0	mV
Input Bias Current	$I_{in-} + I_{in+} / 2$		-1500		-800		-1500	nA
Input Offset Current	$I_{in-} - I_{in+}$		200		200		200	nA
Large Signal Voltage Gain	$R_L = 2k\Omega$	25		15		15		V/mV
Output Voltage Swing	$R_L = 2k\Omega$	± 10		± 10		± 10		V

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3403A
3503A

TOTAL QUAD OPERATIONAL AMPLIFIER

Raytheon Semiconductor

LINEAR

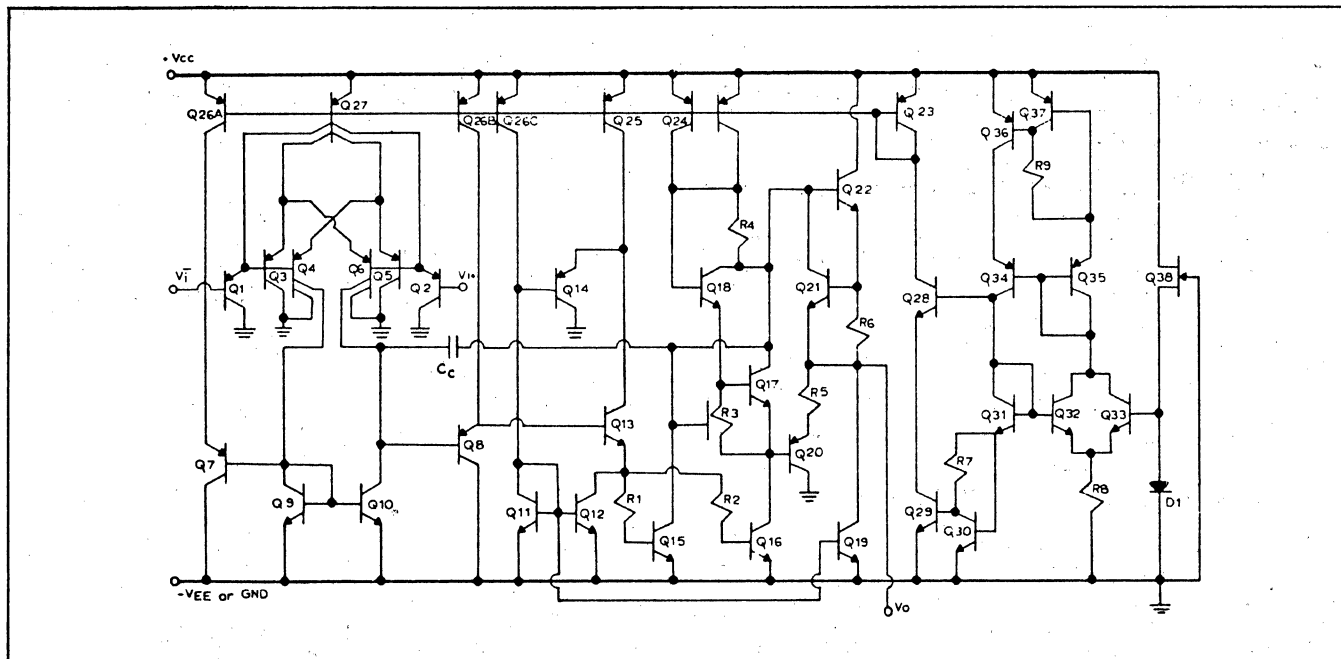
DESCRIPTION

The RC/RV3403A and RM3503A high performance quad op-amps feature improved worst case DC specifications equal to or better than the standard 741 type general purpose op-amp. The devices use a newly developed type of ground-sensing differential input stage which provides increased slew rate.

FEATURES

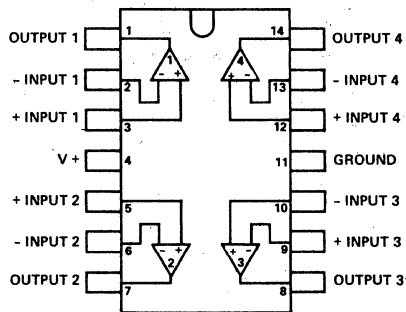
- Class AB output stage; no crossover distortion
- Output voltage swings to ground in single supply operation
- High slew rate: 1.2 V/ μ s
- Single or split supply operation
- Wide supply operation +2.5V to +36V or \pm 1.25V to \pm 18V
- Pin compatible with LM324 and MC3403
- Low power consumption: 0.8 mA/amplifier

SCHEMATIC DIAGRAM



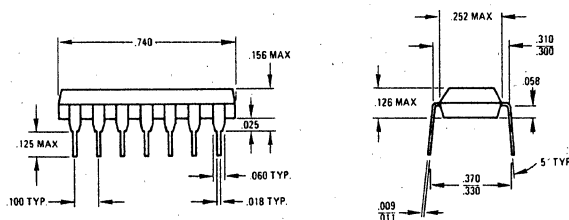
CONNECTION INFORMATION

DB AND DC DUAL-IN-LINE
(Top View)



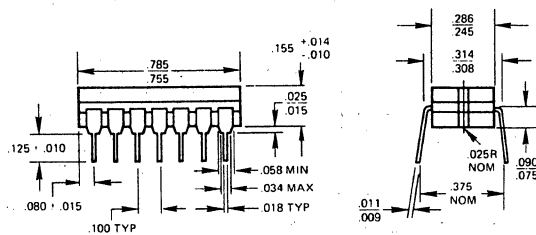
Order Numbers: RC3403ADB, RV3403ADB,
RC3403ADC, RM3503ADC

DB 14-PIN PLASTIC DUAL-IN-LINE



Thermal Resistance
 $\theta_{J-A} = 0.16^{\circ}\text{C}/\text{mW}$
 $\theta_{J-C} = 0.08^{\circ}\text{C}/\text{mW}$

DC 14-PIN CERAMIC DUAL-IN-LINE



Thermal Resistance
 $\theta_{J-A} = 0.120^{\circ}\text{C}/\text{mW}$
 $\theta_{J-C} = 0.06^{\circ}\text{C}/\text{mW}$



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MONOLITHIC DUAL HIGH GAIN OPERATIONAL AMPLIFIERS

RM4558
RC4558

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	(RM4558) $\pm 22V$ (RC4558) $\pm 18V$
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	$\pm 30V$
Input Voltage (Note 2)	$\pm 15V$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature Range	(RM4558) $-55^{\circ}C$ to $+125^{\circ}C$ (RC4558) $0^{\circ}C$ to $+70^{\circ}C$
Lead Temperature (Soldering, 60 sec)	$300^{\circ}C$
Output Short-Circuit Duration (Note 3)	Indefinite

ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}C$, $V_{CC} = \pm 15V$ unless otherwise specified)

PARAMETER	CONDITIONS	RM 4558			RC 4558			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_s \leq 10 \text{ k}\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			30	200		30	200	nA
Input Bias Current			200	500		200	500	nA
Input Resistance		0.3	1.0		0.3	1.0		M Ω
Large-Signal Voltage Gain	$R_L \geq 2 \text{ k}\Omega$ $V_{out} = \pm 10V$	50,000	200,000		20,000	100,000		
Output Voltage Swing	$R_L \geq 10 \text{ k}\Omega$	± 12	± 14		± 12	± 14		V
	$R_L \geq 2 \text{ k}\Omega$	± 10	± 13		± 10	± 13		V
Input Voltage Range		± 12	± 13		± 12	± 13		V
Common Mode Rejection Ratio	$R_s \leq 10 \text{ k}\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_s \leq 10 \text{ k}\Omega$		30	150		30	150	$\mu V/V$
Power Consumption			100	170		100	170	mW
Transient Response (unity gain)	$V_{in} = 20 \text{ mV}$ $R_L = 2 \text{ k}\Omega$ $C_L \leq 100 \text{ pF}$							
		Risetime		0.3		0.3		μs
		Overshoot		5.0		5.0		%
Slew Rate (unity gain)	$R_L \geq 2 \text{ k}\Omega$		0.5		0.5		V/ μs	
Channel Separation (open loop)	$f = 10 \text{ kHz}$ $R_s = 1 \text{ k}\Omega$		70			70		dB
	(Gain = 100) $f = 10 \text{ kHz}$ $R_s = 1 \text{ k}\Omega$		83			83		dB
The following specifications apply for $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ for RM4558; $0^{\circ}C \leq T_A \leq +70^{\circ}C$ for RC4558								
Input Offset Voltage	$R_s \leq 10 \text{ k}\Omega$			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1.5			800	nA
Large-Signal Voltage Gain	$R_L \geq 2 \text{ k}\Omega$ $V_{out} = \pm 10V$	25,000			15,000			
Output Voltage Swing	$R_L \geq 2 \text{ k}\Omega$	± 10			± 10			V
Power Consumption	$V_s = \pm 15V$ $T_A = +125^{\circ}C$ $T_A = -55^{\circ}C$		90	150		90	150	mW
			120	200		120	200	

MATCHING CHARACTERISTICS ($T_A = 25^{\circ}C$, $V = \pm 15V$ unless otherwise noted)

PARAMETER	CONDITIONS	RM 4558 TYP	RC 4558 TYP	UNITS
Voltage Gain	$R_L \geq 2 \text{ k}\Omega$	$\pm .5$	± 1.0	dB
Input Bias Current		± 15	± 15	nA
Input Offset Current		± 7.5	± 7.5	nA
Input Offset Voltage	$R_s \geq 10 \text{ k}\Omega$	$\pm .1$	$\pm .2$	mV

NOTE 1: Rating applies for case temperatures to $125^{\circ}C$; derate linearity at $6.5 \text{ mW}/^{\circ}C$ for ambient temperatures above $+75^{\circ}C$ for RM4558

NOTE 2: For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.

NOTE 3: Short circuit may be to ground or either supply. Rating applies to $+125^{\circ}C$ case temperature or $+75^{\circ}C$ ambient temperature for RC4558.

Raytheon cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in a Raytheon product. No other circuit patent licenses are implied.

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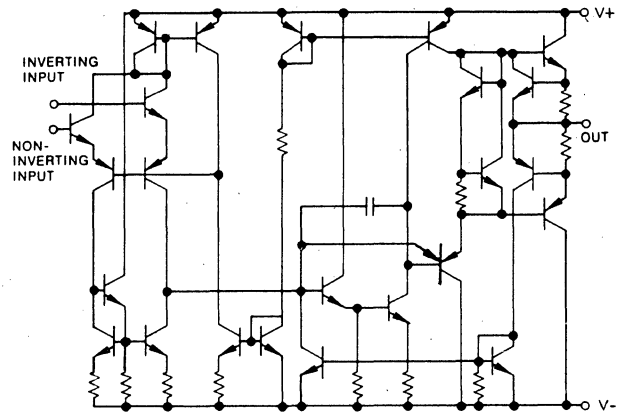
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The Raytheon RM4558 and RC4558 integrated circuits are high gain operational amplifiers internally compensated and constructed on a single silicon chip using the planar epitaxial process.

The military version, RM4558, operates over a temperature range from -55°C to $+125^{\circ}\text{C}$. The commercial version, RC4558 operates from 0°C to $+70^{\circ}\text{C}$.

Combining all of the outstanding features of the 741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics. Excellent channel separation allows the use of the dual device in all single 741 operational amplifier applications providing the highest possible packaging density. It is especially well suited for applications in differential-in, differential-out as well as in potentiometric amplifiers and where gain and phase matched channels are mandatory.

SCHEMATIC DIAGRAM



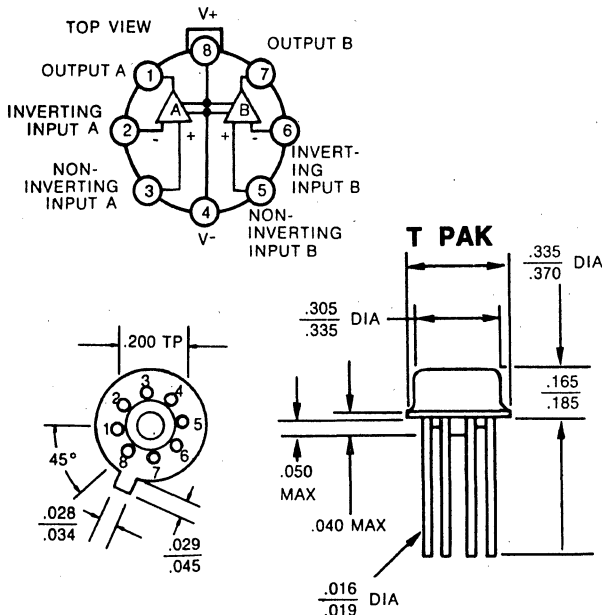
DESIGN FEATURES

- Supply voltage $\pm 22\text{V}$ for RM4558, $\pm 18\text{V}$ for RC4558
- Large common-mode and differential voltage ranges
- Continuous short circuit protection
- Low power consumption
- No frequency compensation required
- Parameter tracking over temperature range
- No latch-up
- Gain and phase match between amplifiers

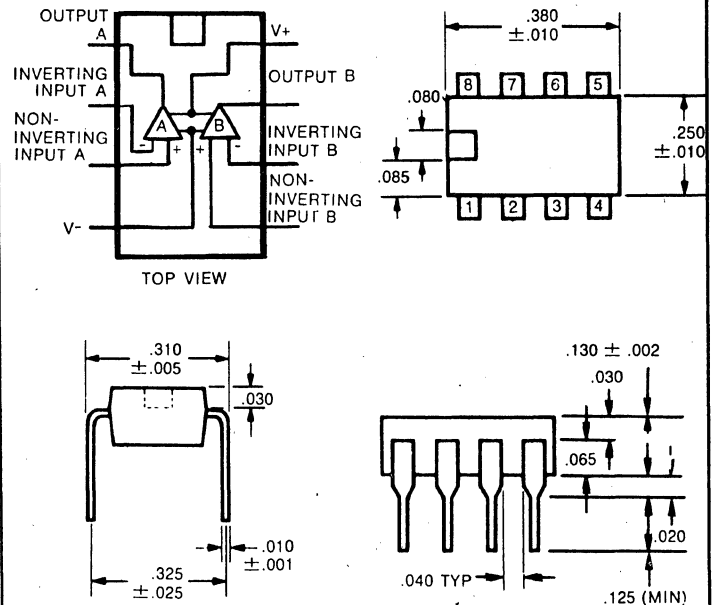
PACKAGE DATA

The RM4558 is available in the 8-pin TO-5 package and the RC4558 is available in the dual-in-line 8-pin mini-dip and the 8-pin TO-5 packages.

TO-5



8-PIN MOLDED DUAL-IN-LINE PACKAGE



VOLTAGE-TO-FREQUENCY CONVERTER

4151

ABSOLUTE MAXIMUM RATINGS

Supply voltages	+8.0 to +22V	
Output sink current	20mA	
Internal power dissipation	500mW	
Input voltage	-0.2V to +V _{CC}	
Output short circuit to ground	Continuous	
Temperature Range	Storage	Operating
	RM4151: -65°C to +150°C	-55°C to +125°C
	RV4151: -55°C to +125°C	-40°C to + 85°C
	RC4151: -55°C to +125°C	0°C to + 70°C

ELECTRICAL CHARACTERISTICS V_{CC} = +15V, T_A = +25°C, unless otherwise specified

PARAMETER	CONDITIONS	TYP	UNITS
SUPPLY CURRENT	8V < V _{CC} < 15V	4.0	mA
	15V < V _{CC} < 22V	6.0	mA
CONVERSION ACCURACY			
Scale Factor	Circuit Figure 2, V _I = 10V	1.00	kHz/V
Drift with Temperature	Circuit Figure 2, V _I = 10V	±50	ppM/°C
Drift with V _{CC}	Circuit Figure 2, V _I = 1.0V 8V < V _{CC} < 18V	0.2	%/V
INPUT COMPARATOR			
Offset Voltage		5	mV
Offset Current		±50	nA
Input Bias Current		-100	nA
Common Mode Range		0 to V _{CC} -2	V
ONE-SHOT			
Threshold Voltage, Pin 5		.667	xV _{CC}
Input Bias Current, Pin 5		-100	nA
Reset V _{SAT}	Pin 5, I = 2.2mA	0.15	V
CURRENT SOURCE			
Output Current	Pin 1, Figure 2, V = 0	138.7	μA
Change with Voltage	Pin 1, V = 0V to V = 10V	1.0	μA
Off Leakage	Pin 1, V = 0V	1	nA
REFERENCE VOLTAGE	Pin 2, Figure 2	1.9	V
LOGIC OUTPUT			
V _{SAT}	Pin 3, I = 3.0mA	0.15	V
V _{SAT}	I = 2.0mA	0.10	V
Off Leakage		.1	μA

Preliminary Specifications – Subject to change without notice.



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DESCRIPTION

The RC4151 and RM4151 provide a simple low-cost method of analog-to-digital conversion. They have all the inherent advantages of the voltage-to-frequency conversion technique. The output of the 4151 is a series of pulses of constant duration. The frequency of the pulses is proportional to the applied input voltage. These converters are designed for use in a wide range of data conversion and remote sensing applications.

PRINCIPLE OF OPERATION

Single Supply Mode VFC

In this application the RC/RM4151 functions as a stand-alone voltage to frequency converter operating on a single positive power supply. Refer to Figure 1, the simplified block diagram. The RC/RM4151 contains a voltage comparator, a one-shot, and a precision switched current source. A positive input voltage applied to pin 7 is compared to the voltage at pin 6. If the input voltage is higher, the input comparator will fire the one-shot. The output of the one-shot is connected to both the logic output and the precision switched current source. During the one-shot period, T , the logic output will go low and the current source will turn on with current I . At the end of the one-shot period the logic output will go high and the current source will shut off. At this time the current source has injected an amount of charge $Q = IT$ into the network R_B-C_B . If this charge has not increased the voltage V_B such that $V_B \geq V_I$, the comparator again fires the one-shot and the current source injects another lump of charge, Q , into the R_B-C_B network. This process continues until $V_B \geq V_I$. When this condition is achieved the current source remains off and the voltage V_B decays until V_B is again equal to V_I . This completes one cycle. The VFC will now run in a steady state mode. The current source

FEATURES

- Single supply operation (+8V to +22V)
- Pulse output compatible with all logic forms
- Programmable scale factor (K)
- Linearity $\pm 0.5\%$ typical - precision mode
- Temperature stability ± 50 ppm/ $^{\circ}\text{C}$ typical
- High noise rejection
- Inherent monotonicity
- Easily transmittable output
- Simple full scale trim
- Single-ended input, referenced to ground
- Also provides frequency-to-voltage conversion

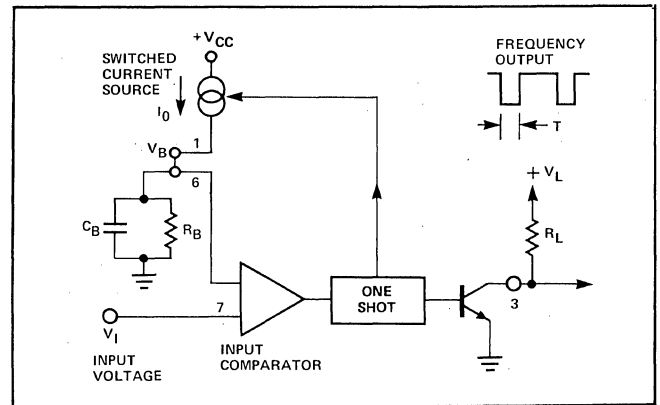


Figure 1. Simplified Block Diagram, Single Supply Mode

dumps lumps of charge into the capacitor C_B at a rate fast enough to keep $V_B \geq V_I$. Since the discharge rate of capacitor C_B is proportional to V_B/R_B , the frequency at which the system runs will be proportional to the input voltage.

TE (TO-5) METAL CAN (Top View)		NB MINIATURE DUAL-IN-LINE (Top View)		PIN	FUNCTION
				1	CURRENT SOURCE
				2	SCALE FACTOR
				3	LOGIC OUTPUT
				4	GROUND
				5	ONE-SHOT R, C
				6	REFERENCE
				7	INPUT VOLTAGE
				8	V_{CC}
Order Part Nos.: RC4151T, RM4151T		Order Part Nos.: RC4151NB, RV4151NB			
NOTE: PIN 4 CONNECTED TO CASE					



DUAL TRACKING VOLTAGE REGULATORS

4194

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LINEAR

ABSOLUTE MAXIMUM RATINGS

Input Voltage $\pm V$ to Ground	RM4194: $\pm 45V$ RC4194: $\pm 35V$
Input-Output Voltage Differential	RM4194: $\pm 45V$ RC4194: $\pm 35V$
Power Dissipation at $T_A = 25^\circ C$	
D Package	900mW
TK Package	3.0W
Load Current	
D Package	150mA
TK Package	250mA
Operating Junction Temperature Range	RM4194: $-55^\circ C$ to $+150^\circ C$ RC4194: $0^\circ C$ to $+125^\circ C$
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Lead Temperature (Soldering, 10s)	$+300^\circ C$

ELECTRICAL CHARACTERISTICS

($\pm 5 \leq V_{OUT} \leq V_{MAX}$ • RM4194: $-55^\circ C \leq T_i \leq +125^\circ C$; RC4194: $0^\circ C \leq T_i \leq +70^\circ C$)

PARAMETER	CONDITIONS	RM4194			RC4194			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	$\Delta V_{in} = 0.1V_{in}$		0.02	0.1		0.02	0.1	% V_{out}
Load Regulation	4194TK: $I_L = 1$ to 200mA 4194D: $I_L = 1$ to 100mA		.001	.002		.001	.004	% V_o / mA
TC of Output Voltage			0.002	0.015		0.003	0.015	%/ $^\circ C$
Stand-By Current Drain (Note 1)	$V_{in} = V_{max}, V_o = 0V$		+0.3	+1.0		+0.3	+1.5	mA
	$V_{in} = V_{max}, V_o = 0V$		-1.2	-2.0		-1.2	-3.0	
Input Voltage Range		± 9.5		± 45	± 9.5		± 35	V
Output Voltage Scale Factor	$R_{set} = 71.5K$ $T_i = 25^\circ C$	2.45	2.5	2.55	2.38	2.5	2.62	K Ω/V
Output Voltage Range	$R_{set} = 71.5K$	0.05		± 42	0.05		$\pm 32V$	V
Output Voltage Tracking				1.0			2.0	%
Ripple Rejection	$f = 120Hz, T_i = 25^\circ C$		70			70		dB
Input-Output Voltage Differential	$I_L = 50mA$	3.0			3.0			V
Output Short Circuit Current	$V_{in} = \pm 30V$ Max.		300			300		mA
Output Noise Voltage	$C_L = 4.7\mu F, V_o = \pm 15V$ $f = 10Hz$ to 100KHz		250			250		μV RMS
Internal Thermal Shutdown			175			175		$^\circ C$

THERMAL CHARACTERISTICS

PARAMETER	CONDITIONS	PACKAGE	
		D	TK (TO-66)
Power Dissipation	$T_A = 25^\circ C$	900mW	3W
	$T_C = 25^\circ C$	2.2W	17.5W
Thermal Resistance	Junction to Ambient, θ_{J-A}	128 $^\circ C/W$	41.6 $^\circ C/W$
	Junction to Case, θ_{J-C}	55 $^\circ C/W$	7.15 $^\circ C/W$

NOTE:
 $\pm I_{Quiescent}$ will increase by 50 $\mu A/V_{out}$ on positive side and 100 $\mu A/V_{out}$ on negative side.



SEMICONDUCTOR DIVISION • 350 ELLIS STREET • MOUNTAIN VIEW, CALIFORNIA 94040

DUAL TRACKING VOLTAGE REGULATORS

DESIGN FEATURES

- Simultaneously Adjustable Outputs With One Resistor to $\pm 42V$.
- Load Current $\pm 200mA$ with .2% Load Regulation

- Internal Thermal Shutdown at $T_j = 175^\circ C$
- External Balance for $\pm V_O$ Unbalancing
- 3W Power Dissipation

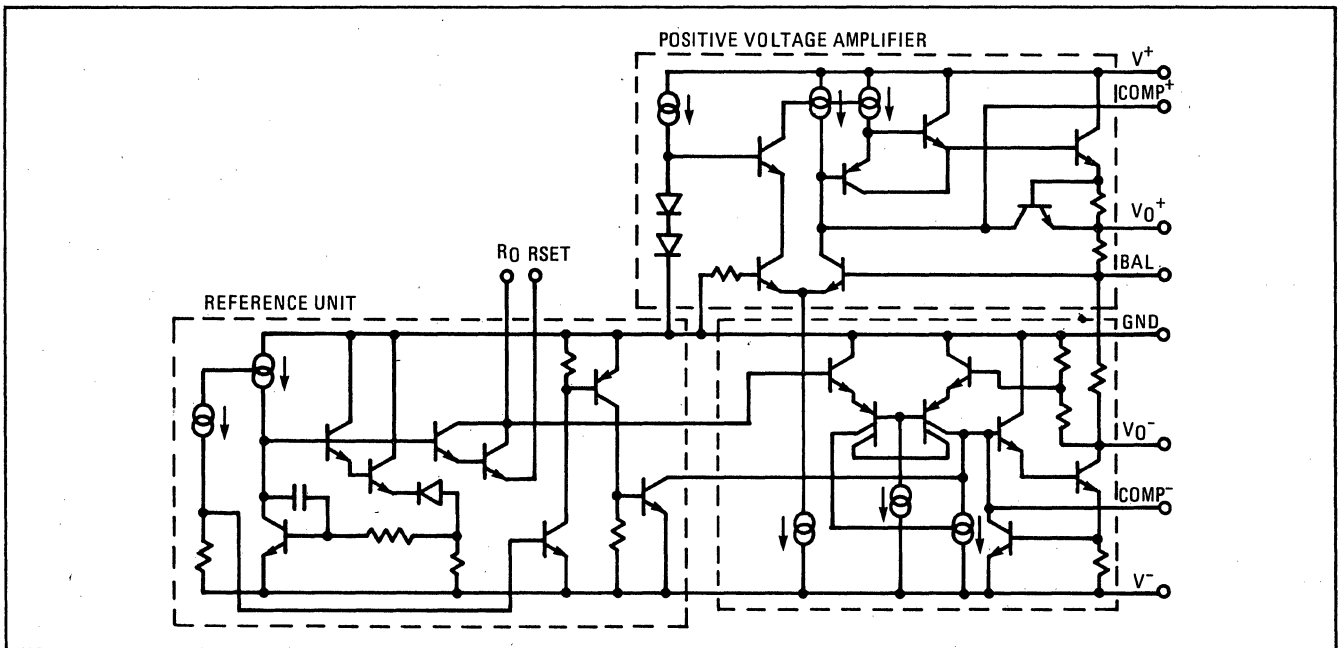
The RM4194 and RC4194 are dual polarity tracking regulators designed to provide balanced or unbalanced positive and negative output voltages at currents to 200mA. A single external resistor adjustment can be used to change both outputs between the limits of $\pm 50mV$ and $\pm 42V$.

These devices are designed for local "on-card" regulation, eliminating distribution problems associated

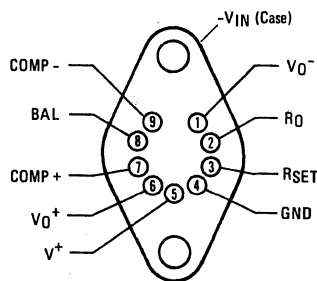
with single-point regulation. To simplify application the regulators require a minimum number of external parts.

The device is available in two package types to accommodate various power requirements. The TK (TO-66) power package can dissipate up to 3W at $T_A = 25^\circ C$. The D 14-pin dual in-line will dissipate up to 900mW.

SCHEMATIC DIAGRAM

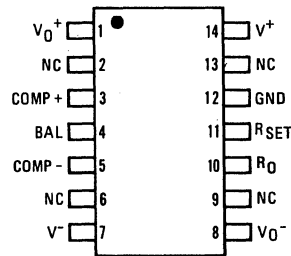


CONNECTION INFORMATION



TK (TO-66) Package
(Bottom View)

Order Part Nos.:
RC4194TK, RM4194TK



D Dual In-line Package
(Top View)

Order Part Nos.:
RC4194D, RM4194D



FIXED $\pm 15V$ DUAL-TRACKING VOLTAGE REGULATORS

4195

ABSOLUTE MAXIMUM RATINGS

Input Voltage $\pm V$ to Ground	$\pm 30V$
Power Dissipation @ $T_A = +25^\circ C$	
TK Package	2.4W
T Package	800mW
DN Package	600mW
Load Current	150mA
Operating Junction Temperature Range	RM4195: $-55^\circ C$ to $+150^\circ C$. RC4195: $0^\circ C$ to $+125^\circ C$
Storage Junction Temperature Range	RM4195: $-65^\circ C$ to $+150^\circ C$. RC4195: $-65^\circ C$ to $+125^\circ C$
Lead Temperature (Soldering, IO's)	$+300^\circ C$

ELECTRICAL CHARACTERISTICS ($I_L = 1mA, V_{CC} = \pm 20V, C_L = 10\mu T$ unless otherwise specified)

PARAMETER	CONDITIONS	RM4195			RC4195			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	$V_{in} = \pm 18$ to $\pm 30V$		2	20		2	20	mV
Load Regulation	$I_L = 1$ to $100mA$		5	30		5	30	mV
Output Voltage Temperature Stability			0.005	0.015		0.005	0.015	%/ $^\circ C$
Standby Current Drain	$V_{IN} = \pm 30V, I_L = 0mA$		± 1.5	± 2.5		± 1.5	± 3.0	mA
Input Voltage Range		18		30	18		30	V
Output Voltage	$T_i = +25^\circ C$	14.8	15	15.2	14.5	15	15.5	V
Output Voltage Tracking			± 50	± 150		± 50	± 300	mV
Ripple Rejection	$f = 120Hz, T_i = +25^\circ C$		75			75		dB
Input-Output Voltage Differential	$I_L = 50mA$	3			3			V
Short-circuit Current	$T_i = +25^\circ C$		220			220		mA
Output Noise Voltage	$T_i = +25^\circ C,$ $f = 100Hz$ to $10KHz$		60			60		μV RMS
Internal Thermal Shutdown			175			175		$^\circ C$

THERMAL CHARACTERISTICS

PARAMETER	CONDITIONS	PACKAGE			UNITS
		DN	T (TO-99)	TK (TO-66)	
Power Dissipation	$T_A = 25^\circ C$	0.6	0.8	2.4	W
	$T_C = 25^\circ C$		2.1	9	
Thermal Resistance	$\phi j-C$		70	17	$^\circ C/W$
	$\phi j-A$	210	185	62	



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Raytheon Semiconductor
LINEAR

FIXED $\pm 15V$ DUAL-TRACKING VOLTAGE REGULATORS

Raytheon Semiconductor

LINEAR

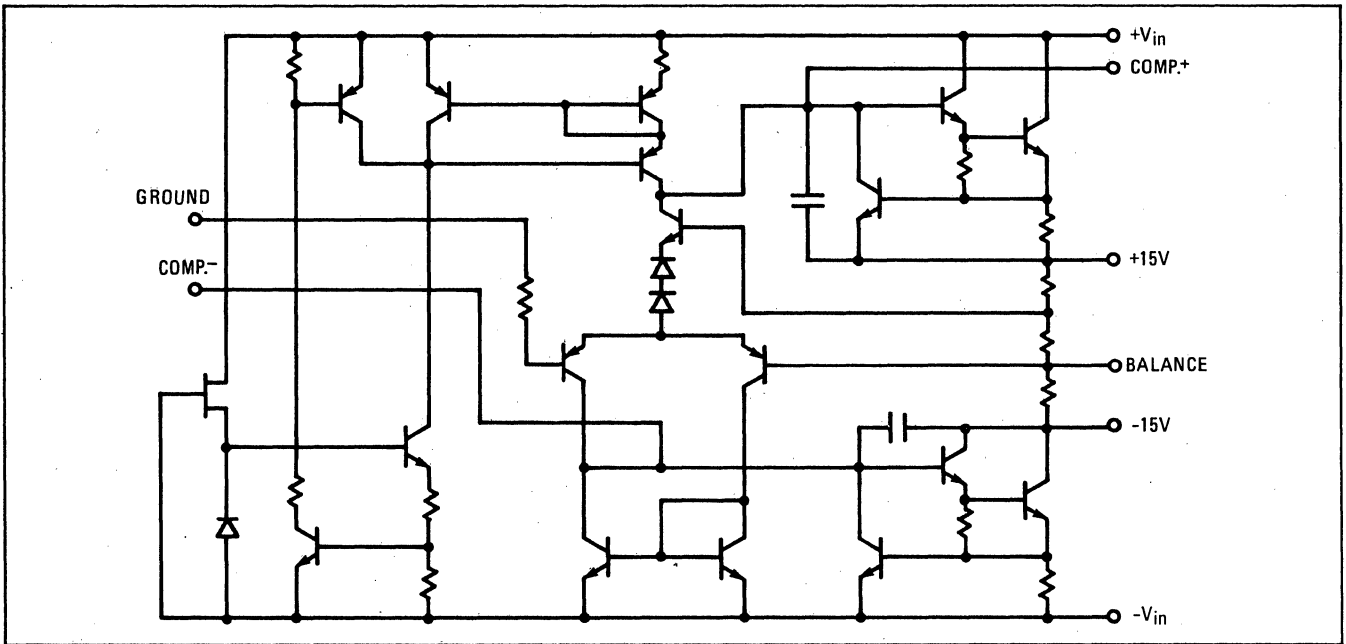
DESIGN FEATURES

- $\pm 15V$ Op-Amp power at reduced cost and component density
- Thermal shutdown at $T_j = +175^\circ C$ in addition to short-circuit protection

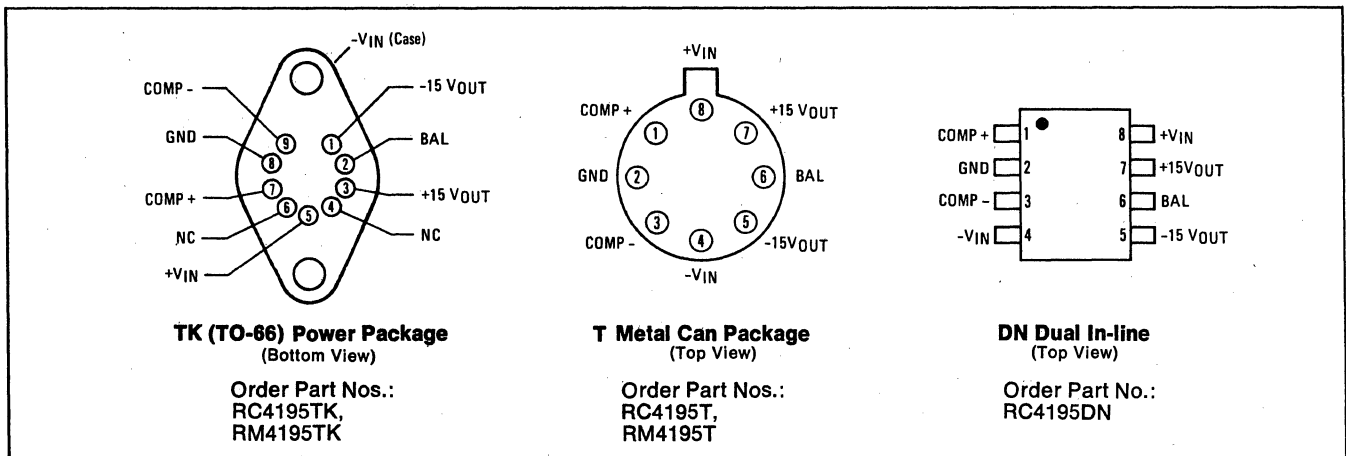
The RM4195 and RC4195 are dual polarity tracking regulators designed to provide balanced positive and negative 15 volt output voltages at currents to 100mA. These devices are designed for local "on-card" regulation eliminating distribution problems associated with single point regulation. The regulator is intended for

- Output currents to 100mA
 - May be used as single output regulator with up to +50V output
 - Available in TO-66, TO-99, and 8-pin plastic mini-DIP ease of application. Only two external components are required for operation (two $10\mu F$ bypass capacitors).
- The device is available in three package types to accommodate various applications requiring economy, high power dissipation, and reduced component density.

SCHEMATIC DIAGRAM



CONNECTION INFORMATION



SEMICONDUCTOR DIVISION • 350 ELLIS STREET • MOUNTAIN VIEW, CALIFORNIA 94040

4 × 4 × 2 BALANCED SWITCHING CROSSPOINT ARRAY

RC4444

ABSOLUTE MAXIMUM RATINGS

Operating Voltage ¹	25V
Internal Power Dissipation ²	900mW
Operating Current per Crosspoint ²	100mA
Storage Temperature Range	- 65°C to +150°C
Operating Temperature Range	0°C to + 70°C
Lead Temperature (Soldering, 60s)	300°C

ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	UNIT	MIN	TYP	MAX
Off resistance @ V _{AK} = 12V	R _{off}	MΩ	10		
On resistance @ 12mA	R _{on}	Ω	3	7	11
Max bias current	I _{AK}	mA			50
Holding current	I _H	mA	0.85	2.00	3.80
V _{on} at 12mA	V _{AK}	V			1.05
Gate firing current/SCR		mA	4		
Gate pulse width		μsec		6	10
Forward breakdown voltage	V _{AK}	V	20	30	
Reverse breakdown voltage	V _{KA}	V	20	30	
Rate firing limit	dv/dt	V/μs	300	500	
Capacitance	C _{AK}	pf		1.7	3
Insertion loss @1KHz		dB		0.2	0.25
I _B = 12mA, 600 Ω load					
Frequency response upper limit, 3dB rel to 1KHz		KHz	500		
Crosstalk isolation @ 1KHz		dB	90	100	
Base emitter forward voltage (PNP)		V		0.7	
Base emitter reverse breakdown voltage (PNP)		V	20		
Gate enabling voltage at 4mA (P+ to K _T or K _R)		V	3		
Forward breakdown voltage (P+ to K _T or K _R)		V			20
Reverse breakdown voltage (P+ to K _T or K _R)		V			20
Gate enabling voltage (P- to K _T or K _R)		V	3		
Reverse breakdown (P- to K _T or K _R)		V			20

NOTES:

1. Maximum voltage from anode to cathode
2. Package thermal resistance θ_{JA} typically .055-c/mW. Package power dissipation limited to 900 mW.



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4 × 4 × 2 BALANCED SWITCHING CROSSPOINT ARRAY

RC4444

DESIGN FEATURES

- Low Bi-Directional R_{on}
- High R_{off}
- Excellent Matching of Gates
- Low Capacitance
- High Rate Firing
- Predictable Holding Current

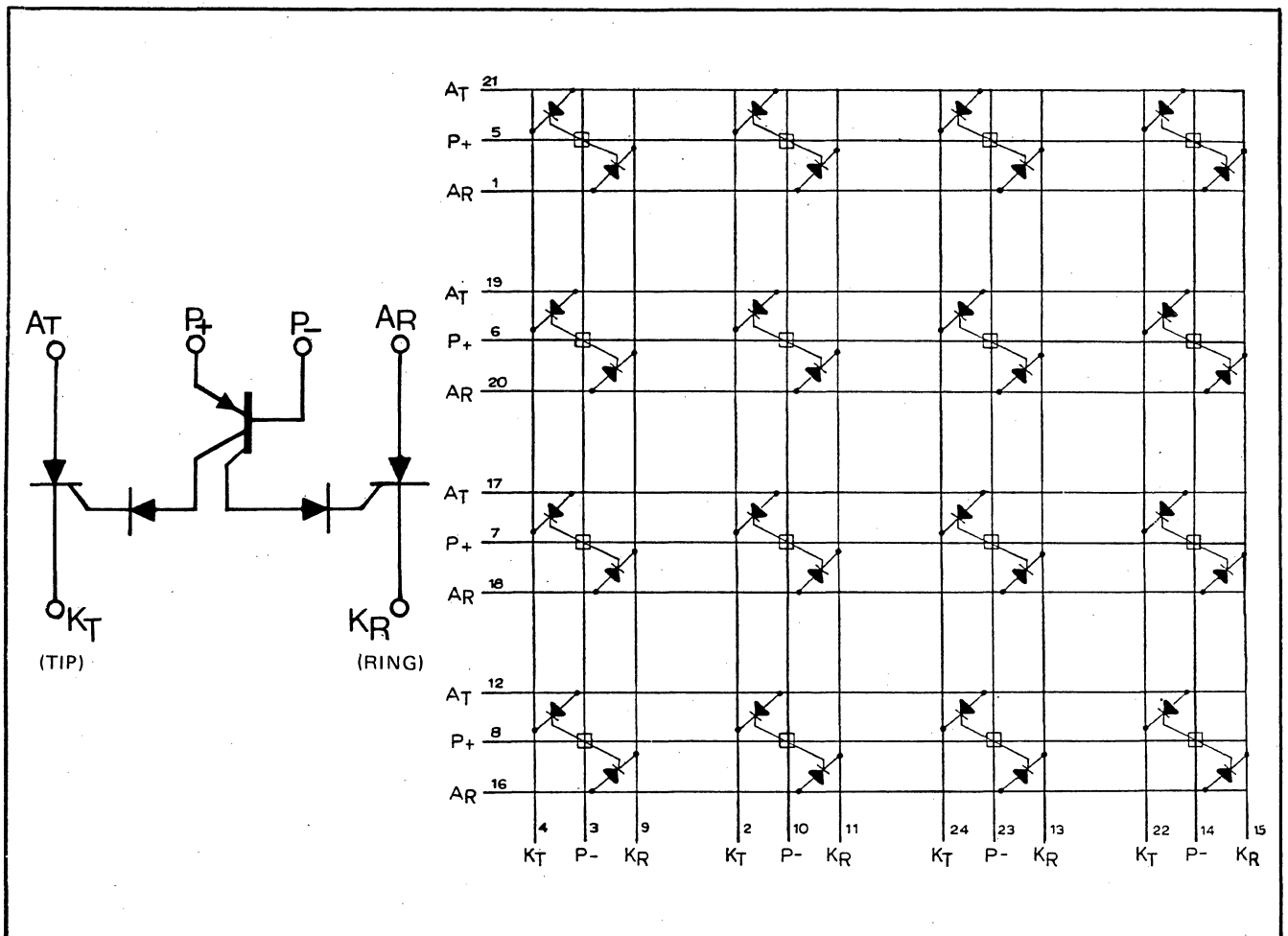
The RC4444 is a monolithic dielectrically isolated crosspoint array arranged into a 4 x 4 x 2 matrix. The primary applications are for balanced switching of 600 ohm transmission lines. The ring and tip are selected by selective biasing of the P+ and P- gate.

Designed to replace reed-relays in telephone switchboards, it does not require a constant gate

drive to keep the SCR in the "on" condition. It is several orders faster, with no bouncing, and has a much longer operating life than its mechanical counterpart.

The 16 SCR pairs with the gating system are packaged in a 24 pin dual-in-line package.

SCHEMATIC DIAGRAM



RAYTHEON

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Raytheon Semiconductor

LINEAR

RCA Gold CHIP Linear Integrated Circuits

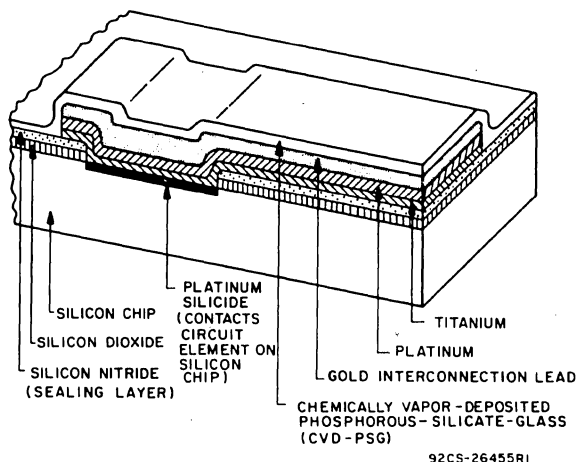
Chip Hermeticity In Plastic

RCA's hermetic IC gold-chip in-line plastic package system, identified by a "G" suffix, is a major technical and commercial innovation in dual-in-line plastic package styles. This new plastic package system, which introduces a gold-metallized hermetic chip encapsulated with RCA's proven plastic formulation, can provide hermetic performance. In other words, RCA's new G-series linear integrated circuits are impervious to moisture under high humidity and reverse-bias conditions and can withstand severe shock and vibration and elevated temperatures. This new package system offers economical improved reliability both in mass-produced equipment and in those critical industrial and military applications where hermeticity, resistance to shock and vibration, and operation over the temperature range of -55°C to $+125^{\circ}\text{C}$ are primary design requirements.

The new G-series circuits are available in 8-, 14-, and 16-lead dual-in-line configurations as required for specific types. The electrical and mechanical characteristics of the G-series types are identical to the characteristics of their non-hermetic counter-parts in similar packages.

Although RCA linear integrated circuits using conventional aluminum-metal chips encapsulated in plastic (epoxy) have demonstrated excellent performance in a wide range of applications over the temperature range of -55°C to $+125^{\circ}\text{C}$, these circuits are non-hermetic and are not completely impervious to moisture. To overcome susceptibility of the devices to the effects of moisture, RCA developed a hermetic gold chip which uses silicon nitride passivation and tri-metal processing involving three precious metals — titanium, platinum, and gold — rather than the traditional aluminum-metal system in the metallization step. This hermetic chip is assembled into the mechanically and chemically sound RCA plastic package to provide an improved reliability level (by at least one order of magnitude MTBF) not previously achievable with conventional dual-in-line plastic-package devices. (See page 2 for reliability test results on RCA hermetic IC gold chips.)

The silicon nitride passivation and the titanium/platinum/gold metallization system used in the processing of the hermetic IC gold chip are similar to that developed for beam-lead wafer technology up to the point at which the circuit-connecting metal film is applied. The cross-sectional view in Fig.1 shows the various metal and passivation layers in the construction of the gold chip, which begins with the conventional diffusion, epitaxial, and photolithographic steps. After the transistors, diodes, and resistors have been formed in the silicon wafer, the gold chip is processed in the sequence shown at the right of Fig.1.



1. A passivation layer of silicon nitride is deposited to protect the silicon surface from the deteriorating effects of both moisture and contaminants.
2. Low-resistance ohmic contacts are made to the device junctions using platinum silicide, an extremely stable, non-corrosive intermetallic compound.
3. A titanium layer is deposited to provide maximum adherence to contact regions and silicon nitride surfaces.
4. A platinum layer is deposited to act as a diffusion barrier between the titanium and the top layer of gold.
5. A gold layer is deposited which, in addition to its high reliability, is highly conductive, has readily bondable surface and exhibits an excellent step-coverage capability.
6. A second passivation ("overcoat") layer of phosphorus-doped, chemically vapor-deposited silicon dioxide glass is then deposited for device passivation and mechanical protection. Phosphorus eliminates stress cracking, and avoids shorting caused by electroplating phenomena.

Fig.1 — Cross-Sectional View of Silicon-Nitride-Passivated Hermetic IC Gold-Chip Structure.

The manufacturing processes used in packaging the hermetic gold chip in the dual-in-line plastic (epoxy) package are essentially similar to those used with conventional aluminum-metal non-hermetic chips. In the hermetic gold-chip package, gold wires are used to interconnect the gold-surfaced bonding pads on the IC chip and the gold-plated bonding surfaces on the package lead terminals.

Reliability

The actual improvement in reliability of the hermetic gold-chip system over the aluminum-metal chip system was determined from a reliability test program designed with special emphasis on those tests normally used to explore failure mechanisms associated with integrated circuits in plastic packages. Table I lists these tests, together with the test conditions proposed for this program. The linear circuits evaluated consisted of

Reliability (Cont'd)

product in the 14-lead dual-in-line plastic package. The results shown in Table I and in Figs.2 and 3, as well as the results of tests conducted at the U.S. Army's Tropical Test Center in the Panama Canal Zone, clearly demonstrate that hermetic gold-chip metallization is superior to aluminum metallization under the most severe environmental conditions, and that plastic-package devices utilizing hermetic gold chips are capable of being used in critical industrial and military equipment subjected to harsh environments.

Fig.2 shows the median-time-to-failure (MTF) estimates obtained from accelerated operating-life tests conducted on integrated circuits employing the silicon nitride passivation and titanium/platinum/gold metallization. These tests are plotted on Arrhenius paper as a function of junction temperature. Extrapolation of these data to the maximum rated operating temperature of +125°C indicates an MTF of approximately 3×10^7 hours.

Data obtained from both temperature-humidity-bias (THB) and pressure-cooker tests were plotted on a Weibull Probability Chart, as shown in Fig.3, for com-

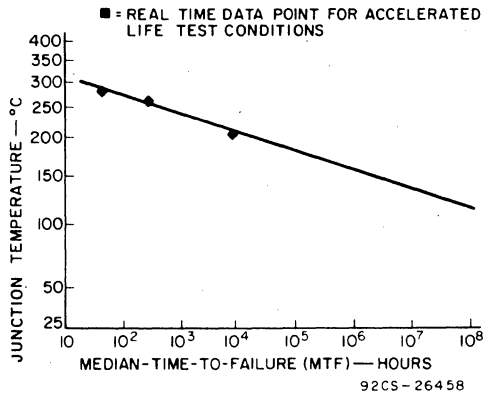


Fig.2 - MTF vs. Junction Temperature with Hermetic-Gold-Chip IC Metallization.

TABLE I - HERMETIC GOLD-CHIP RELIABILITY TEST RESULTS

Reliability Data Summary					
TEST	CONDITIONS	DURATION (HOURS/CYCLES)	TOTAL SAMPLE	UNIT HOURS OR UNIT CYCLES	FAILURES
Operating Life	$T_j = 167^\circ\text{C}$	2,000 hours	40	80,000	0
	$T_j = 158^\circ\text{C}$	1,000 hours	19	19,000	0
	$T_j = 127^\circ\text{C}$	2,000 hours	35	70,000	0
Temperature Humidity Bias (THB)	@ $85^\circ\text{C}/85\% \text{ R.H.}$	5,000 hours	200	1,000,000	0
	15 V Reverse Bias	3,000 hours	35	105,000	0
		2,000 hours	60	120,000	0
		1,000 hours	19	19,000	0
Thermal Fatigue	$T_{j \text{ on}} = 141^\circ\text{C}$ $t = 0.5 \text{ min.}$ $T_{j \text{ off}} = 28^\circ\text{C}$ $t = 2.5 \text{ min.}$	40,000 cycles	15	600,000	0

Accelerated Reliability Test-Data Summary					
TEST	CONDITIONS	DURATION (HOURS/CYCLES)	TOTAL SAMPLE	UNIT HOURS OR UNIT CYCLES	CATASTROPHIC FAILURES
Pressure Cooker	30 psia 121°C	250 hours	230	57,500	0
		200 hours	50	10,000	0
Thermal Shock	-65°C to $+150^\circ\text{C}$ MIL-STD-883 Method 1011C	600 cycles	230	138,000	0
		400 cycles	50	20,000	0
		200 cycles	183	36,000	0
Temperature Cycle	-65°C to $+150^\circ\text{C}$ MIL-STD-883 Method 1010C	1,000 cycles	230	230,000	0

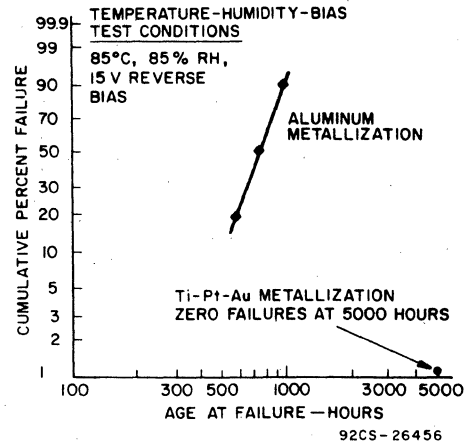


Fig.3 - Test Results for Hermetic Gold Chip vs. Aluminum Metallization.

parison with data taken on devices using aluminum-metal chips. All hermetic gold-chip devices passed 5000 hours of reverse-bias/humidity life testing without a single failure.

The Electronics Technology and Devices Laboratory of the U.S. Army Technical Command at Fort Monmouth, N.J., is evaluating RCA hermetic gold-chip plastic packages at the Army's Tropical Test Center, Panama Canal Zone. In these tests, devices were operated at the seashore and in the jungle under conditions in which the only protection offered was louvered wooden enclosures, similar to the housings used for weather instruments, to protect the devices and test racks from direct exposure to rain. The tests were conducted at 4.5 V reverse bias, 80°F (27°C) ambient temperature, and 90% to 98% relative humidity. According to the most current data, 63 devices have been operated continuously for 14,322 hours (per device) without a single failure. Based on the cumulative device time of 896,616 hours, the failure rate is less than 0.25% per 1000 hours with a 90% confidence level.

See Special RCA DATABOOK offer on inside back cover

G-Series Types

For Commercial, Industrial, and Military Applications
Full Military Operating-Temperature Range (-55°C to $+125^{\circ}\text{C}$)

Package Features

- Hermetic Gold Chip
- Gold Chip Interconnect Metallization and Gold Bonding Pads
- Gold Wires
- Rugged RCA Plastic Encapsulation
- Rated Over Full Military Temperature Range (-55°C to $+125^{\circ}\text{C}$)
- Standard Dual-In-Line Lead Arrangement
- Low Manufacturing Cost
- Readily Adapts to Automatic Chip Assembly Manufacturing

User Benefits

- Improved Mean Time Between Failure by at least 1 Order of Magnitude which means — less board rework, less field service calls, less equipment downtime, improved customer satisfaction.
- Can be designed into critical industrial and military equipment where *both* high mechanical shock and hermeticity are design requirements.
- Eliminates the number of different packaging styles required in inventory.
- Adapts readily to existing automatic insertion equipment
- Can now afford hermetic packaging even where hermeticity is not the critical factor but improved reliability is of concern.
- Portends even lower component costs in the near future.

Type Numbers	Description	Dual-In-Line Plastic Package
CA101AG, CA201AG, CA301AG CA107G, CA207G, CA307G CA741G, CA741CG CA1458G, CA1558G	Operational Amplifiers	8-Lead
CA747G, CA747CG		14-Lead
CA124G, CA224G, CA324G CA3401G	Quad Operational Amplifiers	14-Lead
CA111G, CA211G, CA311G	Voltage Comparators	8-Lead
CA139G, CA239G, CA339G CA139AG, CA239AG, CA339AG	Quad Voltage Comparators	14-Lead
CA3724G, CA3725G	1-A n-p-n Transistor Arrays	14-Lead
CA555G, CA555CG	Timers	8-Lead

See Special RCA DATABOOK offer on inside back cover

RCA-CA3130

COS/MOS Operational Amplifiers

With MOS/FET Input

RCA-CA3130T, CA3130S, CA3130AT, CA3130AS, CA3130BT, and CA3130BS are integrated-circuit operational amplifiers that combine the advantages of both COS/MOS and bipolar transistors on a monolithic chip.

Gate-protected p-channel MOS/FET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (COS/MOS) transistor pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3130 Series circuits operate at supply voltages ranging from 5 to 16 volts, or ± 2.5 to ± 8 volts when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA3130 Series is supplied in either the standard 8-lead TO-5-style package (T suffix) or in the 8-lead dual-in-line formed-lead TO-5-style package "DIL-CAN" (S suffix) and operates over the full military-temperature range of -55°C to $+125^{\circ}\text{C}$. The CA3130B is intended for applications requiring premium-grade specifications and with limits established for: input current, temperature coefficient of input-offset voltage, and gain over the range of -55°C to $+125^{\circ}\text{C}$. The CA3130A offers superior input characteristics over those of the CA3130.

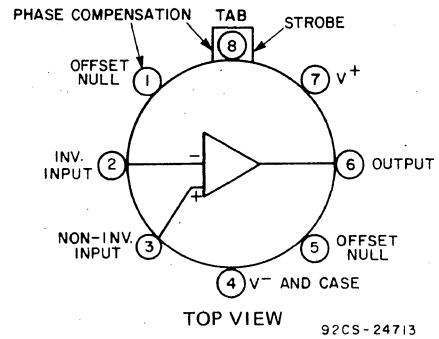
Features:

- MOS/FET input stage provides:
 - very high $Z_i = 1.5 \text{ T}\Omega$ ($1.5 \times 10^{12} \Omega$) typ.
 - very low $I_i = 5 \text{ pA}$ typ. at 15 V operation
 - 2 pA typ. at 5 V operation
 - Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail
 - COS/MOS output stage permits signal swing to either (or both) supply rails
- } Ideal for single-supply applications

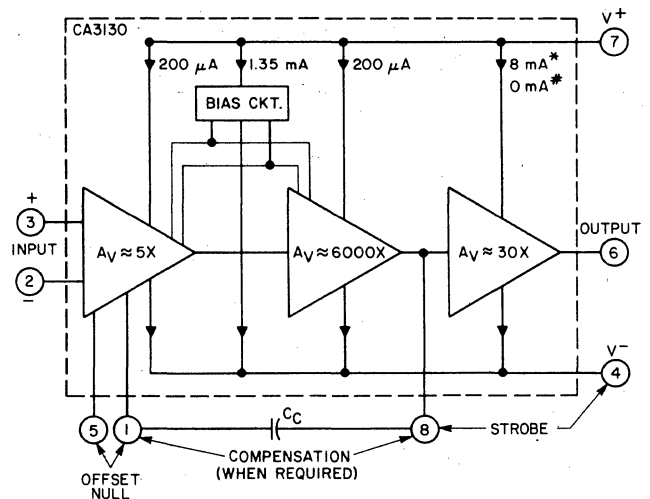
- Low V_{I0} : 2 mV max. (CA3130B)
- Wide BW: 15 MHz typ. (unity-gain crossover)
- High SR: 10 V/ μs typ. (unity-gain follower)
- High output current (I_O): 20 mA typ.
- High A_{OL} : 320,000 (110 dB) typ.
- Compensation with single external capacitor

Applications:

- Ground-referenced single-supply amplifiers
- Fast sample-hold amplifiers
- Long-duration timers/monostables
- High-input-impedance comparators
(ideal interface with digital COS/MOS)
- High-input-impedance wideband amplifiers
- Voltage followers
(e.g., follower for single-supply D/A converter)
- Voltage regulators
(permits control of output voltage down to zero volts)
- Peak detectors
- Single-supply full-wave precision rectifiers
- Photo-diode sensor amplifiers



Functional diagram of the CA3130 Series.



TOTAL SUPPLY VOLTAGE (FOR INDICATED VOLTAGE GAINS) = 15 V
 * WITH INPUT TERMINALS BIASED SO THAT TERM. 6 POTENTIAL IS +7.5 V ABOVE TERM. 4.
 * WITH OUTPUT TERMINAL DRIVEN TO EITHER SUPPLY RAIL.

92CS-24715

Block diagram of the CA3130 Series.

See Special RCA DATABOOK offer on inside back cover

MAXIMUM RATINGS, Absolute-Maximum Values

DC SUPPLY VOLTAGE
(BETWEEN V^+ AND V^- TERMINALS) 16 V
DIFFERENTIAL-MODE INPUT VOLTAGE ± 8 V
COMMON-MODE DC INPUT VOLTAGE ($V^+ + 8$ V) to ($V^- - 0.5$ V)
INPUT-TERMINAL CURRENT 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK—
UP TO 55°C 630 mW
ABOVE 55°C Derate linearly 6.67 mW/°C

WITH HEAT SINK—
AT 125°C 418 mW
BELOW 125°C Derate linearly 16.7 mW/°C
TEMPERATURE RANGE:
OPERATING -55 to +125°C
STORAGE -65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION* INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):
AT DISTANCE 1/16 \pm 1/32 INCH (1.59 \pm 0.79 MM)
FROM CASE FOR 10 SECONDS MAX. +265°C

*Short circuit may be applied to ground or to either supply.

ELECTRICAL CHARACTERISTICS – For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS $V^+ = 15$ V $V^- = 0$ V $T_A = 25^\circ$ C (Unless Specified Otherwise)	CA3130B			CA3130A			CA3130			UNITS
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	$ V_{IO} $	$V^\pm = \pm 7.5$ V	–	0.8	2	–	2	5	–	8	15	mV
Input Offset Current	$ I_{IO} $	$V^\pm = \pm 7.5$ V	–	0.5	10	–	0.5	20	–	0.5	30	pA
Input Current	I_I	$V^\pm = \pm 7.5$ V	–	5	20	–	5	30	–	5	50	pA
Large-Signal Voltage Gain	A_{OL}	$V_O = 10$ V _{p-p} $R_L = 2$ k Ω	100 k	320 k	–	50 k	320 k	–	50 k	320 k	–	V/V
			100	110	–	94	110	–	94	110	–	dB
Common-Mode Rejection Ratio	CMRR		86	100	–	80	90	–	70	90	–	dB
Common-Mode Input-Voltage Range	V_{ICR}		0	–0.5 to 12	10	0	–0.5 to 12	10	0	–0.5 to 12	10	V
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V^+$	$V^\pm = \pm 7.5$ V	–	32	100	–	32	150	–	32	320	μ V/V
	$\Delta V_{IO}/\Delta V^-$		–	32	100	–	32	150	–	32	320	
Maximum Output Voltage	V_{OM}^+	$R_L = 2$ k Ω	12	13.3	–	12	13.3	–	12	13.3	–	V
	V_{OM}^-		–	0.002	0.01	–	0.002	0.01	–	0.002	0.01	
	$ V_{OM}^+ $	$R_L = \infty$	14.99	15	–	14.99	15	–	14.99	15	–	
	$ V_{OM}^- $		–	0	0.01	–	0	0.01	–	0	0.01	
Maximum Output Current:	I_{OM}^+	$V_O = 0$ V	12	22	45	12	22	45	12	22	45	mA
			Sink	I_{OM}^-	$V_O = 15$ V	12	20	45	12	20	45	
Supply Current	I^+	$V_O = 7.5$ V $R_L = \infty$	–	10	15	–	10	15	–	10	15	mA
		$V_O = 0$ V $R_L = \infty$	–	2	3	–	2	3	–	2	3	
Input Current	I_I		–	Fig. 11	15	–	Fig. 11	–	–	Fig. 11	–	nA
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	$T_A = -55$ to 125° C $V^\pm = \pm 7.5$ V [▲] $V_O = 10$ V _{p-p} [*] $R_L = 2$ k Ω [*]	–	5	15	–	10	–	–	10	–	μ V/°C
Large-Signal Voltage Gain	A_{OL}		50 k	320 k	–	–	320 k	–	–	320 k	–	V/V
			94	110	–	–	110	–	–	110	–	dB

▲ Applies only to I_I and $\Delta V_{IO}/\Delta T$.

* Applies only to A_{OL} .

See Special RCA DATABOOK offer on inside back cover

LINEAR RCA Solid State

RCA-CA3078

Micropower Operational Amplifier

The RCA CA3078T and CA3078AT are high-gain monolithic operational amplifiers which can deliver milliamperes of current yet only consume microwatts of standby power. Their operating points are externally adjustable and frequency compensation may be accomplished with one external capacitor. The CA3078T and CA3078AT provide the designer with the opportunity to tailor the frequency response and improve the slew rate without sacrificing power. Operation with a single 1.5-volt battery is a practical reality with these devices.

Features:

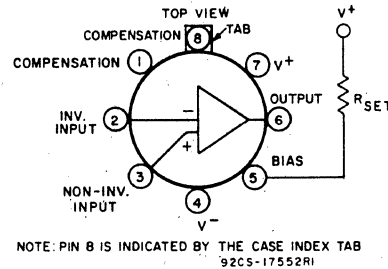
- Low standby power: as low as 700 nW
- Wide supply voltage range: ± 0.75 to ± 15 V
- High peak output current: 6.5 mA min.
- Adjustable quiescent current
- Output short-circuit protection

Applications:

- Portable electronics
- Medical electronics
- Instrumentation
- Telemetry

The CA3078AT is a premium device having a supply voltage range of $V^{\pm} = 0.75$ V to $V^{\pm} = 15$ V. The CA3078T has the same lower supply voltage limit but the upper limit is $V^{+} = +6$ V and $V^{-} = -6$ V.

The CA3078 and CA3078A are supplied in either the standard 8-lead TO-5 package ("T" suffix), or in the 8-lead dual-in-line formed-lead "DIL-CAN" package ("S" suffix).



Functional diagram of the CA3078T and CA3078AT.

RCA-CA3080

Operational Transconductance Amplifiers (OTA's)

Gateable-Gain Blocks

The RCA-CA3080 and CA3080A are Gateable-Gain Blocks which utilize the unique Operational Transconductance Amplifier (OTA) concept described in Application Note ICAN-6668, "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

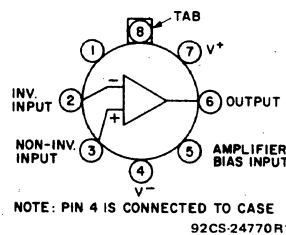
The CA3080 and CA3080A have differential input and a single-ended, push-pull, class A output. In addition, these types have an amplifier bias input which may be used either for gating or for linear gain control. These types also have a high output impedance and their transconductance (g_m) is directly proportional to the amplifier bias current (I_{ABC}).

The CA3080A is rated for operation over the full military-temperature range (-55 to $+125^{\circ}\text{C}$) and its characteristics are specifically controlled for applications such as sample-and-hold, gain-control, multiplex, etc.

These types are supplied in the 8-lead TO-5 style package (CA3080, CA3080A), and in the 8-lead TO-5 style package with dual-in-line formed leads ("DIL-CAN"; CA3080S, CA3080AS). The CA3080E is also supplied in the 8-lead dual-in-line plastic ("MINI-DIP") package (CA3080E), and in chip form (CA3080H).

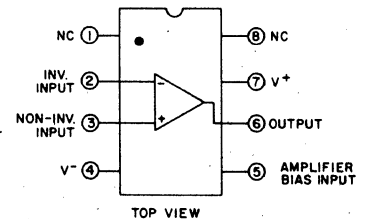
Features:

- Slew rate (unity gain, compensated): 50 V/ μ s
- Adjustable power consumption: 10μ W to 30 mW
- Flexible supply voltage range: ± 2 V to ± 15 V
- Fully adjustable gain: 0 to $g_m R_L$ limit
- Tight g_m spread: CA3080 (2:1), CA3080A (1.6:1)
- Extended g_m linearity: 3 decades



TOP VIEW

TO-5 Style Package



TOP VIEW

92CS-24771

TOP VIEW

Plastic Package (CA3080E)

See Special RCA DATABOOK offer on inside back cover

RCA-CA3095

Super-Beta Transistor Array

Differential Cascode Amplifier Plus 3 Independent Transistors

RCA-CA3095E is a monolithic array of transistors connected as a super-beta differential cascode amplifier with three independent n-p-n transistors.

The differential cascode amplifier incorporates two cascode amplifiers consisting of transistors Q1, Q3 and Q2, Q4, respectively, plus a voltage-limiting circuit, consisting of diodes D1, D2 and p-n-p transistor Q5. Two of these transistors, Q1 and Q2, are super-beta types that have an $h_{FE} > 1000$ and are capable of operating over a wide current range of $1 \mu\text{A}$ to 2mA . Each of these types comprises the input section of its respective cascode amplifier. The output

section of each cascode amplifier employs a conventional n-p-n transistor, Q3, Q4, respectively. The output signal is obtained at the collectors of these transistors.

The independent transistors, Q6, Q7 and Q8, are high-voltage silicon n-p-n conventional types for general use in signal processing systems in the frequency range from dc through vhf. Separate terminals for each of these transistors permit maximum flexibility in circuit design.

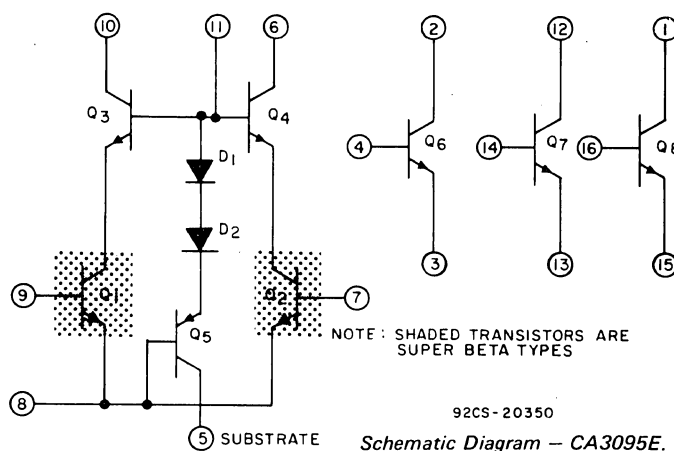
The CA3095E is supplied in a 16-lead dual-in-line plastic package and operates over the ambient temperature range of -40°C to $+85^\circ\text{C}$.

Features

- Two super-beta n-p-n transistors – $h_{FE} > 1000$
- Voltage-limiting circuitry (D1, D2, Q5)
- Operation possible at I_{IB} down to $< 1 \text{nA}$
- Matched pair (Q1 and Q2) –
 $V_{IO} = 5 \text{mV max. at } I_C = 100 \mu\text{A dc}$
 $I_{IO} = 20 \text{nA max. at } I_C = 100 \mu\text{A dc}$
- Wide current range – $< 1 \mu\text{A}$ to 2mA

Independent Transistors:

- $h_{FE} = 300$ typ. for each transistor
- Wide current range – $< 1 \mu\text{A}$ to 10mA
- Matched general-purpose transistors
- High voltage – $V_{CBO} = 45 \text{V max.}$



RCA-CA3100

Wideband Operational Amplifier

RCA-CA3100S, CA3100T is a large-signal wideband, high-speed operational amplifier which has a unity gain crossover frequency (f_T) of approximately 38MHz and an open-loop, 3dB corner frequency of approximately 110kHz . It can operate at a total supply voltage of from 14 to 36volts (± 7 to $\pm 18 \text{volts}$ when using split supplies) and can provide at least 18V p-p and 30mA p-p at the output when operating from $\pm 15 \text{volt}$ supplies. The CA3100 can be compensated with a

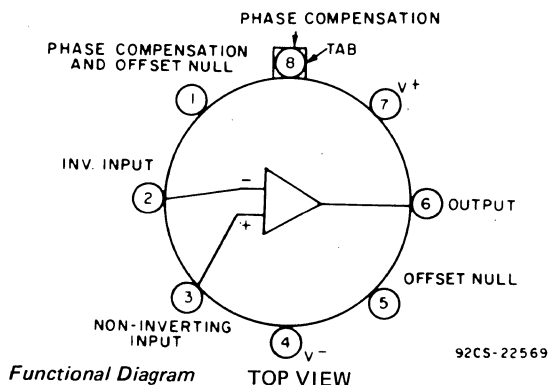
single external capacitor and has dc offset adjust terminals for those applications requiring offset null.

The CA3100 circuit contains both bipolar and P-MOS transistors on a single monolithic chip.

The CA3100 is supplied in either the standard 8-lead TO-5 package ("T" suffix), or in the 8-lead TO-5 dual-in-line formed-lead "DIL-CAN" package ("S" suffix).

Features:

- High open-loop gain at video frequencies – $42 \text{dB typ. at } 1 \text{MHz}$
- High unity-gain crossover frequency (f_T) – 38MHz typ.
- Wide power bandwidth – $V_O = 18 \text{V p-p typ. at } 1.2 \text{MHz}$
- High slew rate – $70 \text{V}/\mu\text{s (typ.) in } 20 \text{dB amplifier}$
 $25 \text{V}/\mu\text{s (typ.) in unity-gain amplifier}$
- Fast settling time – $0.6 \mu\text{s typ.}$
- High output current – $\pm 15 \text{mA min.}$
- LM118, 748/LM101 pin compatibility
- Single capacitor compensation
- Offset null terminals



See Special RCA DATABOOK offer on inside back cover

DESCRIPTION

The μA7800 series of monolithic Three-Terminal Positive Voltage Regulators employ internal current limiting, thermal shutdown and safe-area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. They are intended as fixed-voltage regulators in a wide range of applications including local, on-card regulation for elimination of distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and also as the power pass element in precision regulators.

FEATURES

- OUTPUT CURRENT IN EXCESS OF 1 AMP
- NO EXTERNAL COMPONENTS
- INTERNAL THERMAL OVERLOAD PROTECTION
- INTERNAL SHORT CIRCUIT CURRENT LIMITING
- OUTPUT TRANSISTOR SAFE-AREA COMPENSATION
- AVAILABLE IN THE TO-220 AND THE TO-3 PACKAGE
- OUTPUT VOLTAGES OF 5, 6, 8, 12, 15, 18, AND 24 VOLTS

ABSOLUTE MAXIMUM RATINGS

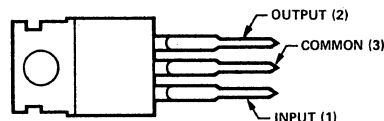
Input Voltage (5V through 18V)	35V
(24V)	40V
Internal Power Dissipation (Note 1)	Internally Limited
Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature Range (Note 2)	
7800	-55°C to +150°C
7800C	0°C to +125°C
Lead Temperature	
TO-3 Package	
(Soldering, 60 second time limit)	300°C
TO-220 Package	
(Soldering, 10 second time limit)	230°C

NOTES:

1. Thermal resistance of the packages (without a heat sink)
Junction to Case: TO-3 Package 4°C/W; TO-220 Package 2°C/W
Junction to Ambient: TO-3 Package 35°C/W; TO-220 Package 50°C/W
2. Operating Ambient Temperature Range 7800 -55°C to +125°C
7800C 0°C to +85°C

CONNECTION DIAGRAMS

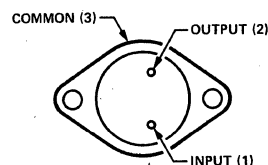
TO-220 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE U



ORDER INFORMATION

OUTPUT VOLTAGE	ORDER PART NO.
5V	7805CU
6V	7806CU
8V	7808CU
12V	7812CU
15V	7815CU
18V	7818CU
24V	7824CU

TO-3 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE DA

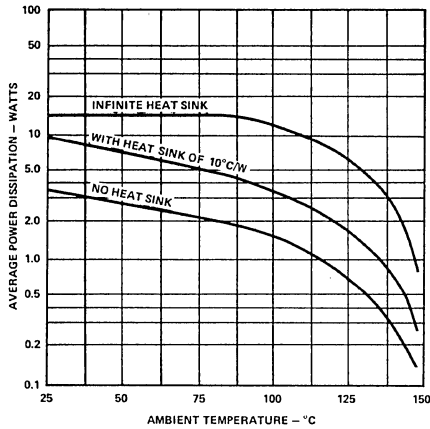


ORDER INFORMATION

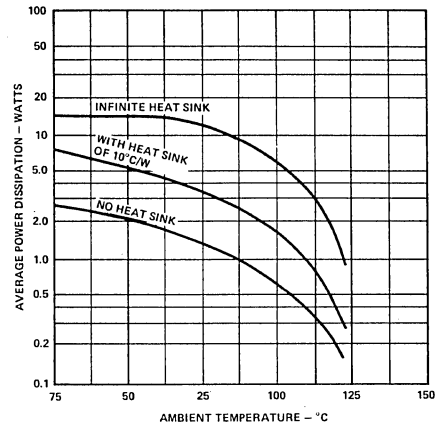
OUTPUT VOLTAGE	ORDER PART NO.
5V	7805DA
6V	7806DA
8V	7808DA
12V	7812DA
15V	7815DA
18V	7818DA
24V	7824DA
5V	7805CDA
6V	7806CDA
8V	7808CDA
12V	7812CDA
15V	7815CDA
18V	7818CDA
24V	7824CDA

TYPICAL CURVES FOR 7800 SERIES

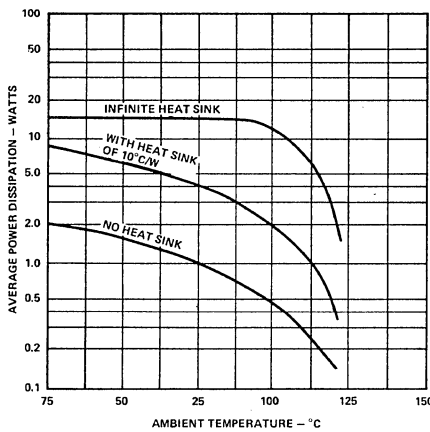
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3, 7800)



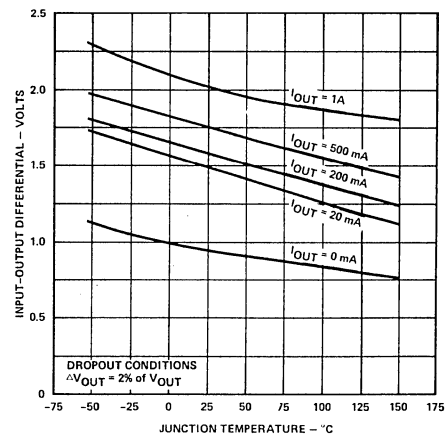
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3, 7800C)



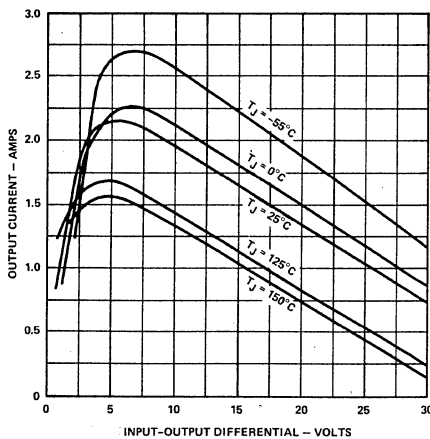
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-220, 7800C)



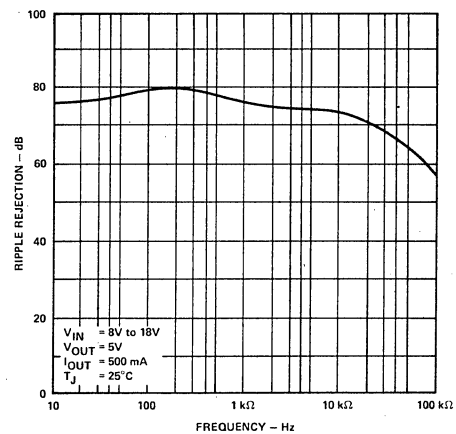
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT/OUTPUT DIFFERENTIAL VOLTAGE



RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

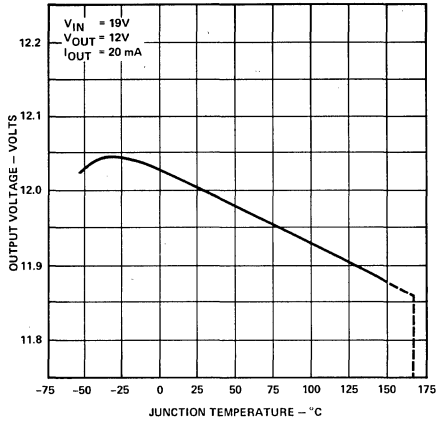


Signetics

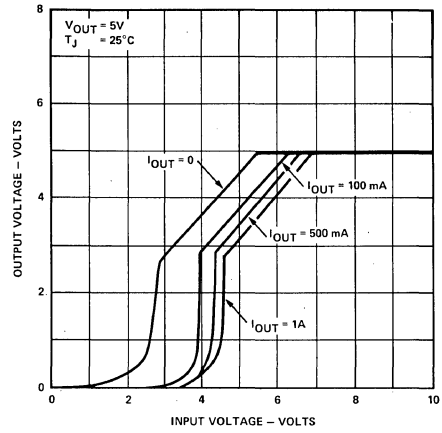
LINEAR

TYPICAL CURVES FOR 7800 SERIES (Continued)

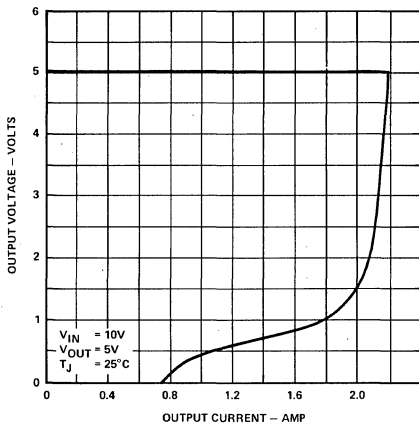
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



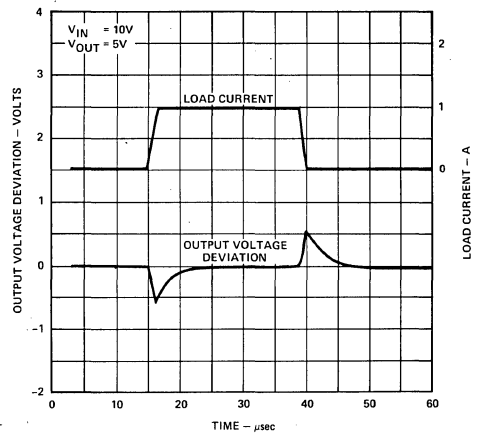
DROPOUT CHARACTERISTICS



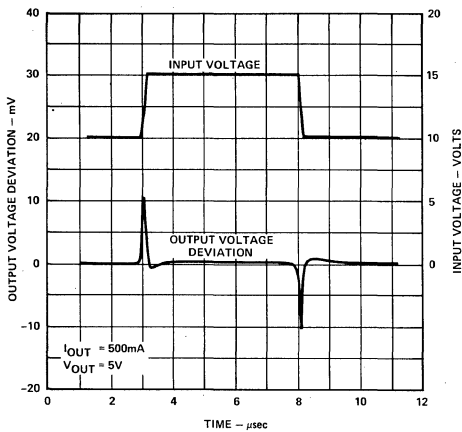
CURRENT LIMITING CHARACTERISTICS



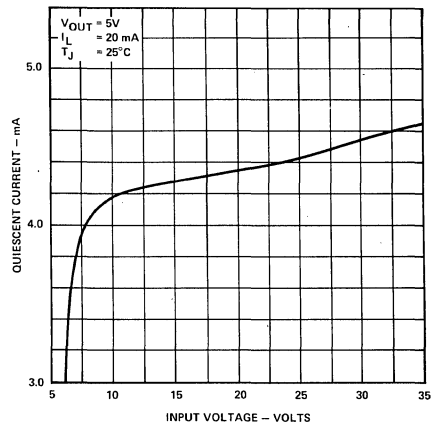
LOAD TRANSIENT RESPONSE



LINE TRANSIENT RESPONSE



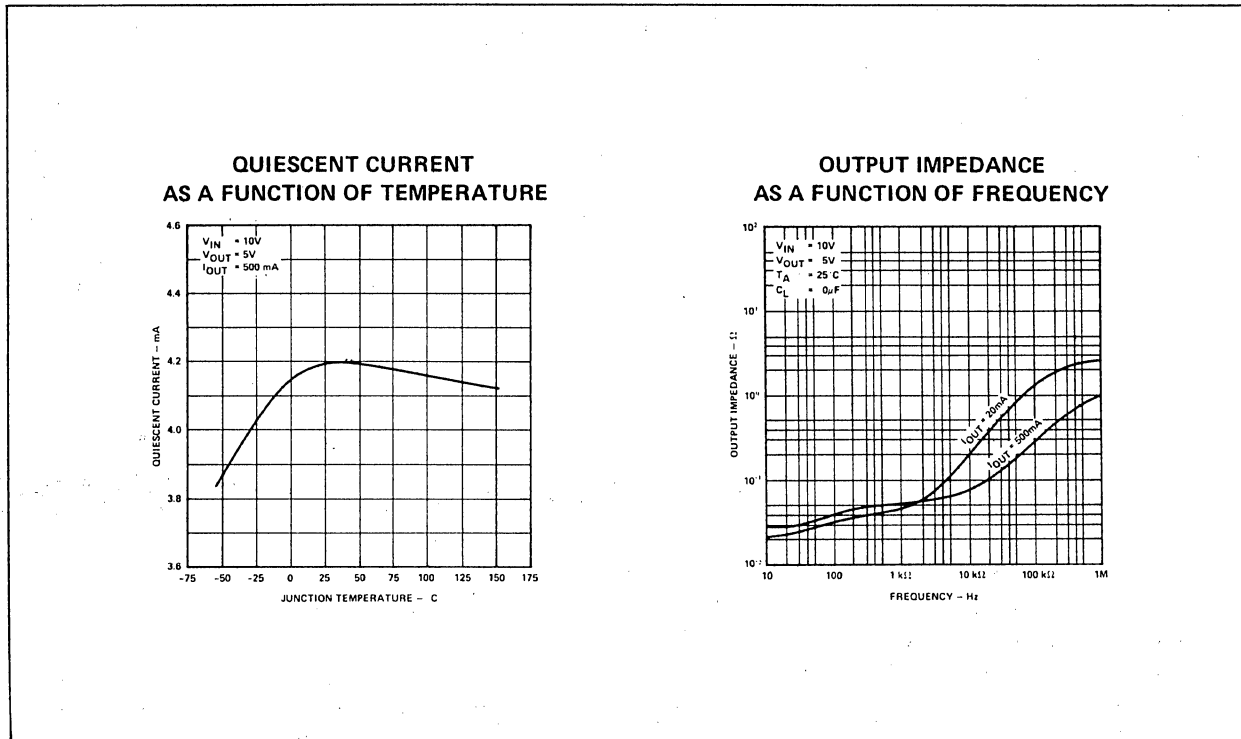
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



Signetics

LINEAR

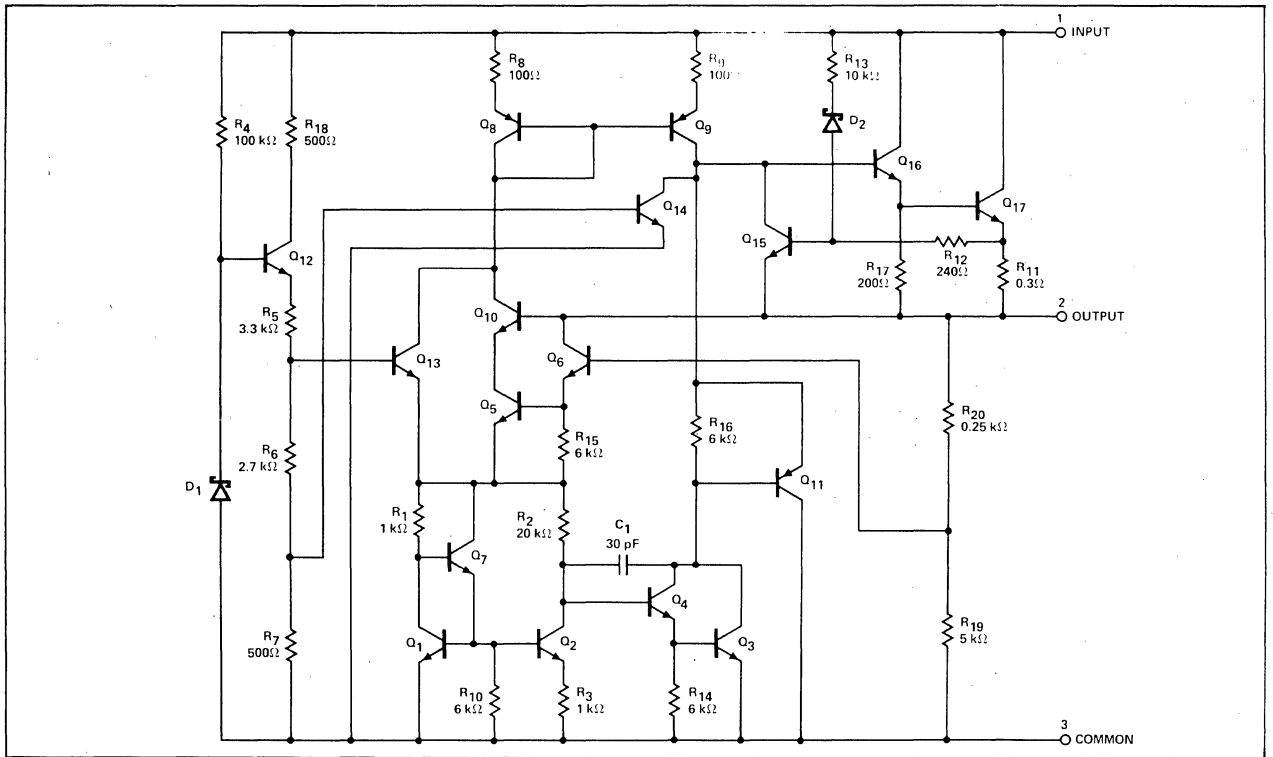
TYPICAL CURVES FOR 7800 SERIES (Continued)



ELECTRICAL CHARACTERISTICS $I_{OUT} = 40\text{mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, $C_{IN} = 0.33\mu\text{F}$, $C_{OUT} = 0.1\mu\text{F}$ (Unless Otherwise Specified)

OUTPUT VOLTAGE (V)	LINE REGULATION (mV)			LOAD REGULATION (mV)			OUTPUT VOLTAGE (V)	QUIESCENT CURRENT (mA)	QUIESCENT CURRENT CHANGE - mA					
	MIN	TYP	MAX	MIN	TYP	MAX				MIN	TYP	MAX		
$V_{IN} = 10\text{V}$ 7805 7805C	4.8	5.0	5.2	3	50	1	25	15	50	5	25	4.2	6.0	0.8
$V_{IN} = 11\text{V}$ 7806 7806C	5.75	6.0	6.25	5	60	1.5	30	14	60	4	30	4.3	6.0	0.8
$V_{IN} = 14\text{V}$ 7808 7808C	7.7	8.0	8.3	6	80	2	40	12	80	4	40	4.3	6.0	0.8
$V_{IN} = 19\text{V}$ 7812 7812C	11.5	12.0	12.5	10	120	3	60	12	120	4	60	4.3	6.0	0.8
$V_{IN} = 23\text{V}$ 7815 7815C	14.4	15.0	15.6	11	150	3	75	12	150	4	75	4.4	6.0	0.8
$V_{IN} = 27\text{V}$ 7818 7818C	17.3	18.0	18.7	15	180	5	90	12	180	4	90	4.5	6.0	0.8
$V_{IN} = 33\text{V}$ 7824 7824C	23.0	24.0	25.0	18	240	6	120	12	240	4	120	4.6	6.0	0.8

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Continued)

QUIESCENT CURRENT CHANGE - mA	OUTPUT NOISE VOLTAGE μ V	LONG TERM STABILITY mV	RIPPLE REJECTION dB	DROPOUT VOLTAGE V	OUTPUT RESISTANCE m Ω	SHORT CIRCUIT CURRENT mA	PEAK OUTPUT CURRENT A	AVERAGE TEMPERATURE COEFFICIENT OF INPUT VOLTAGE mV/ $^{\circ}$ C
WITH LOAD								
5mA < I _{OUT} < 1.0mA	T _A = 25 $^{\circ}$ C 10Hz - f - 100kHz		f = 120Hz 8V \cdot V _{IN} - 18V	T _J = 25 $^{\circ}$ C I _{OUT} = 1.0A	f = 1kHz	T _J = 25 $^{\circ}$ C	T _J = 25 $^{\circ}$ C	I _{OUT} = 5mA 0 $^{\circ}$ C < T _J < 150 $^{\circ}$ C
7805	0.5	40	20	68 78	2.0	17	750	2.2
7805C	0.5	40	20	62 78	2.0	17	750	2.2
7806	0.5	45	24	9V \cdot V _{IN} - 19V 65 75	2.0	19	550	2.2
7806C	0.5	45	24	59 75	2.0	19	550	2.2
7808	0.5	52	32	11.5V \cdot V _{IN} - 21.5V 62 72	2.0	16	450	2.2
7808C	0.5	52	32	56 72	2.0	16	450	2.2
7812	0.5	75	48	15V \cdot V _{IN} - 25V 61 71	2.0	18	350	2.2
7812C	0.5	75	48	61 71	2.0	18	350	2.2
7815	0.5	90	60	18.5V \cdot V _{IN} - 28.5V 60 70	2.0	19	230	2.1
7815C	0.5	90	60	60 70	2.0	19	230	2.1
7818	0.5	110	72	22V \cdot V _{IN} - 32V 59 69	2.0	22	200	2.1
7818C	0.5	110	72	59 69	2.0	22	200	2.1
7824	0.5	170	96	28V \cdot V _{IN} - 38V 56 66	2.0	28	150	2.1
7824C	0.5	170	96	56 66	2.0	28	150	2.1

Signetics

LINEAR

DESCRIPTION

The μA78L00 is a series of 3-Terminal Positive Voltage Regulators. These regulators employ internal current limiting and thermal shutdown, making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 100mA output current. They are intended as fixed voltage regulators in a wide range of applications including local or on card regulation for elimination of noise and distribution problems associated with single point regulation. In addition, they can be used with power pass elements to make high current voltage regulators. The μA78L00 used as a Zener diode/resistor combination replacement, offers an effective output impedance improvement of typically two orders of magnitude, along with lower quiescent current and lower noise.

FEATURES

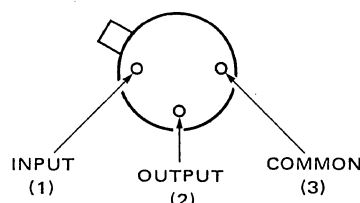
- OUTPUT CURRENT UP TO 100mA
- NO EXTERNAL COMPONENTS
- INTERNAL THERMAL OVERLOAD PROTECTION
- INTERNAL SHORT CIRCUIT CURRENT LIMITING
- AVAILABLE IN JEDEC TO-92 AND LOW PROFILE TO-39 PACKAGES
- OUTPUT VOLTAGES OF 2.6V, 5V, 6.2V, 12V AND 15V
- OUTPUT VOLTAGE TOLERANCES OF ±5% (78L00-AC) AND ±10% (78L00C) OVER THE TEMPERATURE RANGE

ABSOLUTE MAXIMUM RATINGS

Input Voltage		
2.6V, 5V and 6.2V		30V
12V and 15V		35V
Internal Power Dissipation	Internally Limited	
Storage Temperature Range		
Metal Can (TO-39 Type)		-65°C to +150°C
Molded TO-92		-55°C to +150°C
Operating Junction Temperature Range		0°C to +150°C
Lead Temperatures		
Metal Can (Soldering, 60 s time limit)		300°C
Molded TO-92 (Soldering, 10 s time limit)		260°C

CONNECTION DIAGRAMS

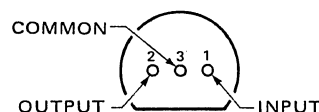
TO-39 TYPE METAL CAN
(TOP VIEW)
PACKAGE OUTLINE DB



ORDER INFORMATION

OUTPUT VOLTAGE	PART NO.
5V	78L05A DB
5V	78L05 DB
12V	78L12A DB
12V	78L12 DB
15V	78L15A DB
15V	78L15 DB

JEDEC (TO-92) PACKAGE
(TOP VIEW)
PACKAGE OUTLINE S



ORDER INFORMATION

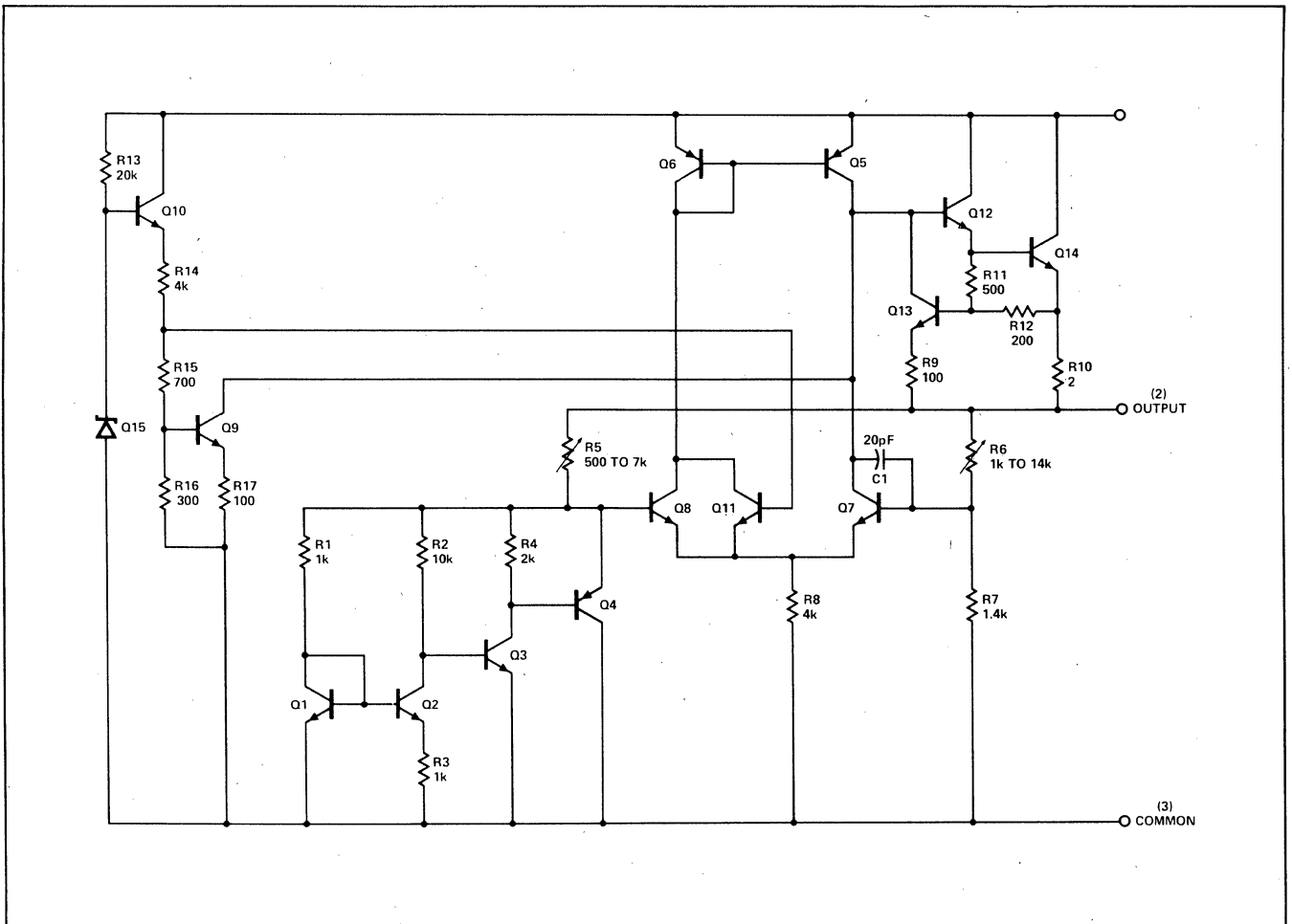
OUTPUT VOLTAGE	PART NO.
2.6V	78L02A S
2.6V	78L02 S
5V	78L05A S
5V	78L05 S
6.2V	78L06A S
6.2V	78L06 S
12V	78L12A S
12V	78L12 S
15V	78L15A S
15V	78L15 S

SIGNETICS 3-TERMINAL POSITIVE VOLTAGE REGULATOR ■ μ A78L00 SERIES

ELECTRICAL CHARACTERISTICS $I_{OUT} = 40\text{mA}$, $0^\circ\text{C} < T_J < +125^\circ\text{C}$, $C_{IN} = 0.33\mu\text{F}$, $C_{OUT} = 0.1\mu\text{F}$ (Unless Otherwise Specified)

	OUTPUT VOLTAGE (V)			LINE REGULATION mV						LOAD REGULATION mV						OUTPUT VOLTAGE V					
	$T_J = 25^\circ\text{C}$			$T_J = 25^\circ\text{C}$						$T_J = 25^\circ\text{C}$											
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
$V_{IN} = 9.0\text{V}$				4.75V $\cdot V_{IN} \cdot 20\text{V}$ 5V $\cdot V_{IN} \cdot 20\text{V}$						1mA $\cdot I_{OUT} \cdot 100\text{mA}$ 1mA $\cdot I_{OUT} \cdot 40\text{mA}$						1mA $\cdot I_{OUT} \cdot 70\text{mA}$ 1mA $\cdot I_{OUT} \cdot 40\text{mA}$					
78L02AC	2.5	2.6	2.7	40	100	30	75	10	50	4.0	25	2.45	2.75	2.45	4.75V $\cdot V_{IN} \cdot 20\text{V}$	2	2	2	2	2	2
78L02C	2.4	2.6	2.8	40	125	30	100	10	50	4.0	25	2.35	2.85	2.35	7V $\cdot V_{IN} \cdot 20\text{V}$	2	2	2	2	2	2
$V_{IN} = 10\text{V}$				7V $\cdot V_{IN} \cdot 20\text{V}$ 8V $\cdot V_{IN} \cdot 20\text{V}$												7V $\cdot V_{IN} \cdot 20\text{V}$					
78L05AC	4.8	5.0	5.2	55	150	45	100	11	60	5.0	30	4.75	5.25	4.75	8.5V $\cdot V_{IN} \cdot 20\text{V}$	5	5	5	5	5	5
78L05C	4.6	5.0	5.4	55	200	45	150	11	60	5.0	30	4.5	5.5	4.5	8.5V $\cdot V_{IN} \cdot 20\text{V}$	5	5	5	5	5	5
$V_{IN} = 12\text{V}$				8.5V $\cdot V_{IN} \cdot 20\text{V}$ 9V $\cdot V_{IN} \cdot 20\text{V}$												8.5V $\cdot V_{IN} \cdot 20\text{V}$					
78L06AC	5.95	6.2	6.45	65	175	55	125	13	80	6.0	40	5.90	6.5	5.90	14.5V $\cdot V_{IN} \cdot 27\text{V}$	11.4	12.6	11.4	11.4	11.4	11.4
78L06C	5.7	6.2	6.7	65	200	55	150	13	80	6.0	40	5.6	6.8	5.6	14.5V $\cdot V_{IN} \cdot 27\text{V}$	10.8	13.2	10.8	10.8	10.8	10.8
$V_{IN} = 19\text{V}$				14.5V $\cdot V_{IN} \cdot 27\text{V}$ 16V $\cdot V_{IN} \cdot 27\text{V}$												14.5V $\cdot V_{IN} \cdot 27\text{V}$					
78L12AC	11.5	12	12.5	120	250	100	200	20	100	10	50	11.4	12.6	11.4	17.5V $\cdot V_{IN} \cdot 30\text{V}$	14.25	15.75	14.25	14.25	14.25	14.25
78L12C	11.1	12	12.9	120	250	100	200	20	100	10	50	10.8	13.2	10.8	17.5V $\cdot V_{IN} \cdot 30\text{V}$	13.5	16.5	13.5	13.5	13.5	13.5
$V_{IN} = 23\text{V}$				17.5V $\cdot V_{IN} \cdot 30\text{V}$ 20V $\cdot V_{IN} \cdot 30\text{V}$												17.5V $\cdot V_{IN} \cdot 30\text{V}$					
78L15AC	14.4	15	15.6	130	300	110	250	25	150	12	75	14.25	15.75	14.25		15	15	15	15	15	15
78L15C	13.8	15	16.2	130	300	110	250	25	150	12	75	13.5	16.5	13.5		15	15	15	15	15	15

EQUIVALENT CIRCUIT



Signetics

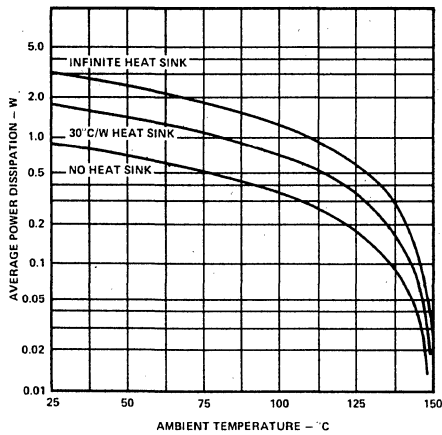
LINEAR

ELECTRICAL CHARACTERISTICS (Continued)

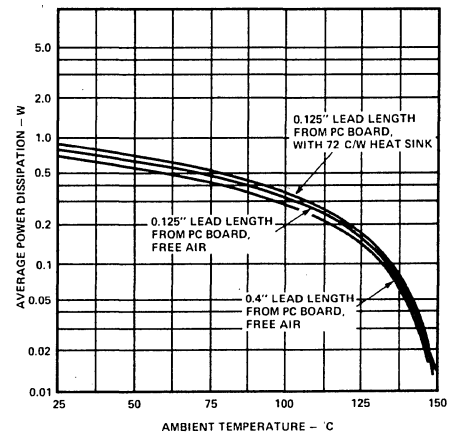
QUIESCENT CURRENT mA			QUIESCENT CURRENT CHANGE mA			OUTPUT NOISE VOLTAGE μ V	LONG TERM STABILITY mV	RIPPLE REJECTION dB	DROPOUT VOLTAGE V		
			WITH LINE	WITH LOAD							
$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$			$1\text{mA} \leq I_{OUT} \leq 40\text{mA}$			$T_J = 25^\circ\text{C}$ $10\text{Hz} \leq f \leq 100\text{kHz}$		$T_J = 25^\circ\text{C}$ $f = 120\text{Hz}$	$T_A = 25^\circ\text{C}$		
MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
			$5\text{V} \leq V_{IN} \leq 20\text{V}$						$6\text{V} \leq V_{IN} \leq 16\text{V}$		
3.6	6.0		5.5		2.5	0.1	30	10	43	51	1.7
3.6	6.0		5.5		2.5	0.2	30	10	42	51	1.7
			$8\text{V} \leq V_{IN} \leq 20\text{V}$						$8\text{V} \leq V_{IN} \leq 18\text{V}$		
3.8	6.0		5.5		1.5	0.1	40	12	41	49	1.7
3.8	6.0		5.5		1.5	0.2	40	12	40	49	1.7
			$9.0\text{V} \leq V_{IN} \leq 20\text{V}$						$10\text{V} \leq V_{IN} \leq 20\text{V}$		
3.9	6.0		5.5		1.5	0.1	50	14	40	46	1.7
3.9	6.0		5.5		1.5	0.2	50	14	39	46	1.7
			$16\text{V} \leq V_{IN} \leq 27\text{V}$						$15\text{V} \leq V_{IN} \leq 23\text{V}$		
4.2	6.5		6.0		1.5	0.1	80	24	37	42	1.7
4.2	6.5		6.0		1.5	0.2	80	24	36	42	1.7
			$20\text{V} \leq V_{IN} \leq 30\text{V}$						$18.5\text{V} \leq V_{IN} \leq 28.5\text{V}$		
4.4	6.5		6.0		1.5	0.1	90	30	34	39	1.7
4.4	6.5		6.0		1.5	0.2	90	30	33	39	1.7

DESIGN CONSIDERATIONS

MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE TO-39 TYPE PACKAGE



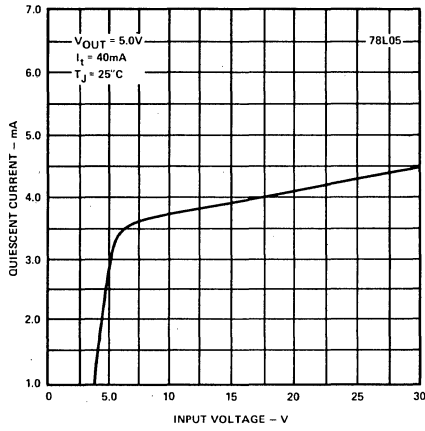
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE TO-92 TYPE PACKAGE



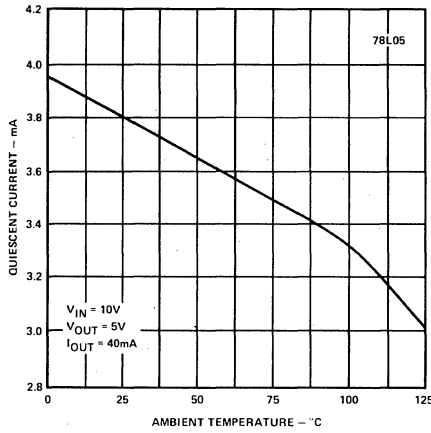
NOTE: Typical thermal resistance of the TO-39 type metal can package without a heat sink is junction to case of 40°C/W and junction to ambient of 140°C/W . Typical thermal resistance of the TO-92 package is junction to ambient of 180°C/W with .400 inch leads from PC board and 160°C/W with .125 inch lead length.

TYPICAL ELECTRICAL PERFORMANCE CURVES

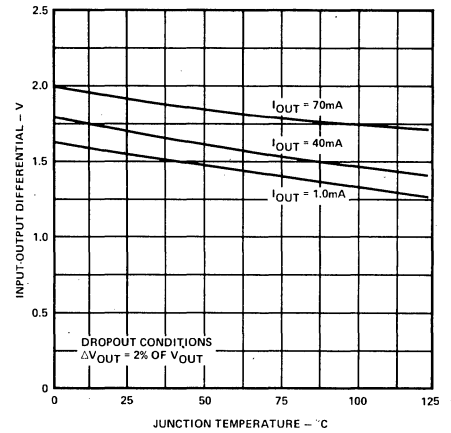
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



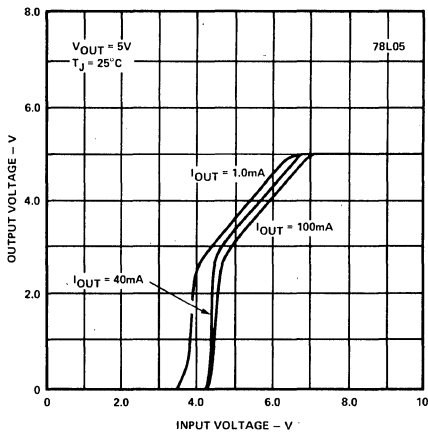
QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



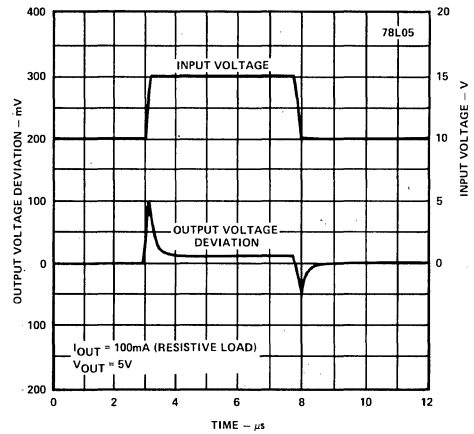
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



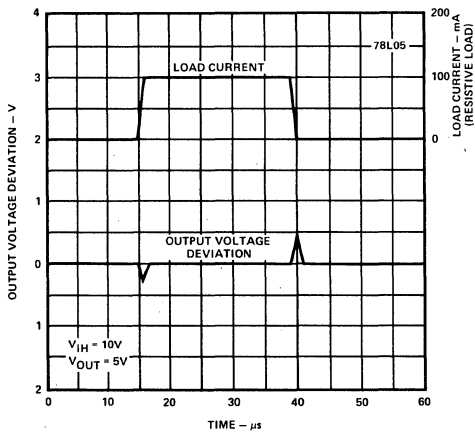
DROPOUT CHARACTERISTICS



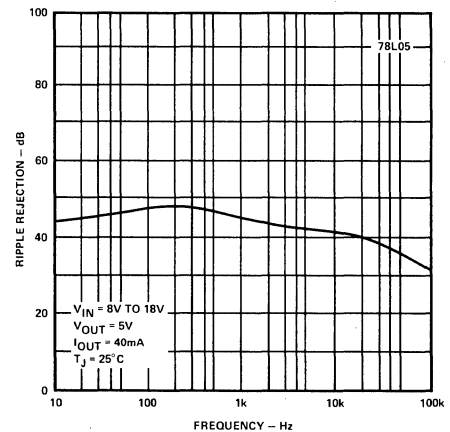
LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



NOTE: Other μ A78L00 Series Devices have similar curves.

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INTRODUCTION TO MEMORY

The Master Selection Guide provides sufficient information to make initial product selections, to lead you to a group of device numbers and manufacturers' names. It enables you to find the products which are most appropriate to fulfill your major requirements and then provides data for many of the more important products.

All devices that appear in this section, both in the initial selection guide and in the data pages, are included in the Part Number and Product Indexes. These index listings lead to the page and the line on that page where each device appears.

The Memory Section provides initial selection information and data on PROMs, RAMs, and ROMs as well as other memory devices. In these particular sections, the devices are characterized by organization (words and bits/words) and by access times. In order to assure that the access times are comparable, whenever possible the values have been shown in nanoseconds over the full rated temperature range for the devices (i.e., 0° to 70°C for commercial units and -55°C to 125°C for military units). The full temperature nanosecond value is marked "nsF." When this value isn't specified, the guaranteed nanosecond value at room temperature is listed followed by "nsR." In some cases a guaranteed value has not yet been established; then the typical value is shown followed by "ns*" (* means typical throughout this book). "Typical" values are invariably much faster than the guaranteed ones so that such listings place these memories higher on the list than they otherwise would appear.

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The manufacturers listed above are providing detailed information on their latest and most significant products. They have made this investment to help you. Some chose not to.

If you want to see more data in future editions, tell the manufacturers through their salesmen and distributors.

MEMORY—Character Generators

Format	Number of Output Lines	Input Logic Levels	Supply Voltage	Device	Source
Character Generators					
4 x 5	25	MOS	-12,14	4881	Nortec
5 x 5	25	MOS	-12,14	4881	Nortec
6 x 8	8	TTL	5 -12	MM4241 MMS241	† National National
5 x 7	5	MOS	-28 -28 ±12	NCM1121 NCM1122 4481	Nitron Nitron Nortec
		TTL	5 5 5 -12,±5 -12,5 -12,5 -12,5 -12,5	RO3-2513 6061 6055 2513 CRC3504 CRC3505 3258 RO3-2513 TMS2501	EMM/Semi MMI MMI Signetics Collins Collins Fairchild GI TI
	7	MOS	±12 ±12 ±14 ±14 ±14 ±14 ±14 -14,-28	MCS1004 MCS1005 NCM1130 NCM1131 NCM1132 TMS4103 MK2002	MOS MOS Nitron Nitron Nitron TI Mostek
		TTL	±12 -12,5 -12,5 -12,5	EA40105 3257 RO5-2240S MK2302	EA Fairchild GI Mostek
	8	TTL	5	N8205CB1016	Signetics
	10	TTL	-12,5	MK2408	Mostek
5 x 8	5	MOS	±12	MM4240	† National
7 x 8	4	TTL	5	N8228CB162	Signetics
	10	MOS	±12	EA4004	EA
	35	MOS	-12,14	4881	Nortec
7 x 9	7	MOS	±5	MCS2017	MOS
		TTL	±5	MCS2022	MOS
		TTL	-12,5 5 5 5 5 5 -3,5,12 -3,5,12 -3,5,12 -3,5,12 -3,5,12 -3,5,12 -3,5,12 -3,5,12 -3,5,12 -3,5,12 -3,5,12 -3,5,12 -3,5,12 -3,5,12 -3,5,12 -3,5,12 -3,5,12	3260 5297 6071 6072 6297 MCM6571 MCM6570 MCM6571A MCM6572 MCM6573 MCM6574 MCM6575 MCM6576 MCM6577 MCM6578 MCM6579 NCM6571 NCM6572	Fairchild † MMI MMI MMI MMI Motorola Motorola Motorola Motorola Motorola Motorola Motorola Motorola Motorola Motorola Motorola Motorola Motorola Motorola Motorola Motorola Nitron Nitron
	9	MOS	-12,-24 ±12	EA3815 EA4001	EA EA

Format	Number of Output Lines	Input Logic Levels	Supply Voltage	Device	Source
Character Generators (cont)					
7 x 9	9	MOS/TTL	±5	MCS2024	MOS
		TTL	5 5 -3,5,12 -3,5,12 -3,5,12 -3,5,12 -3,5,12	6074 6073 MCM6580 MCM6581 MCM6583 NCM6581 NCM6583	MMI MMI Motorola Motorola Motorola Nitron Nitron
7 x 10	7	MOS/TTL	±5	MSC2020	MOS
		TTL	±12	EA4016	EA
7 x 11	1	TTL	5	CG5004L	SMC
9 x 9	9	TTL	-12,5	RO5-5184	GI
9 x 9	9	TTL	5 5	5299 6299	† MMI MMI
10 x 12	10	MOS/TTL	±5 ±5	MCS2018 MCS2025	MOS MOS

MEMORY Master Selection Guide

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† Military Temperature Range (-55°C to 125°C) * — Typical Values

Bold face indicates additional data is provided on the page noted.

MEMORY—Code Converters

Code Conversion From To	Bits In	Bits Out	Process	Supply Voltage	Device	Source
Code Converters						
ASCII - BCDIC	6	6	PMOS	±12 ±12	MM4220LR MM5220LR	† National National
ASCII - EBCDIC	6	7	PMOS	±12 ±12	MM4220EK MM5220EK	† National National
			Bipolar	5	N8224CB180	Signetics
8	8	8	Bipolar	5	N8204YCB504	Signetics
10	PMOS	±12	EA4015	EA		
9	8	Bipolar	5	N8205CB175	Signetics	
ASCII - HOLLERITH	9	10	PMOS	-24	EA4035	EA
ASCII - SELECTRIC	7	7	PMOS	-12,5 -12,5 ±12 ±12	3512A 3514A/B MM4230KP MM5230KP	† Fairchild Fairchild National National
BCD - BINARY	6	6	Bipolar	5 5	SN54184 SN74184	† TI TI
BCDIC - ASCII	6	7	PMOS	±12 ±12 ±12 ±12	MM4220AP MM5220AP MM4220LR MM5220LR	† National National † National National
Baudot - ASCII	5	8	PMOS	±12 ±12	MM4220BL MM5220BL	† National National
BINARY - BCD	6	6	Bipolar	5 5	SN54185A SN74185A	† TI TI
EBCDIC - ASCII	8	8	Bipolar	5	N8204CB505	Signetics

Code Conversion From To	Bits In	Bits Out	Process	Supply Voltage	Device	Source
Code Converters (cont)						
			PMOS	(continued) -12,5	N2461/CM4030	Signetics
	9	9	PMOS	-12,5 -12,5	CRC3503-1-2 CRC3503-2-2	Collins Collins
	10	10	PMOS	±12	EA4015	EA
	9	8	PMOS	±12 5	N2430YCM000 N8205CB175	Signetics Signetics
	12	8	Bipolar	5	DM8576AAA	† National National
EBCDIC - DCDIC	7	6	PMOS	±12 ±12	MM4230JT MM5230JT	† National National
EBCDIC - HOLLERITH	9	10	MOS	-24	EA4034	EA
	12	8	PMOS	-24, -12 -24, -12	NCM1111 NCM1112	Nitron Nitron
			Bipolar	5 5	MCM4069A MCM4070A	Motorola Motorola
EBCDIC - SELECTRIC	8	8	PMOS	±12 ±12	MM4230FE MM5230FE	† National National
HOLLERITH - ASCII	8	8	PMOS	±12 ±12	MM4230BO MM5230BO	† National National
HOLLERITH - EBCDIC	8	8	PMOS	±12 ±12	MM4230QW MM5230QW	† National National
	9	10	PMOS	-24	EA4034	EA
Multiple SELECTRIC, HOLLERITH - EBCDIC - ASCII			NMOS	-3,5,12 -3,5,12 -3,5,12	MCM6561 MCM6562 NCM6561	Motorola Motorola Nitron
			NMOS	-3,5,12	MCM6591 NCM6591	Motorola Nitron
SELECTRIC - ASCII	8	10	PMOS	-24, -12	NCM1151	Nitron
SELECTRIC - EBCDIC	8	8	PMOS	±12 ±12	MM4230FE MM5230FE	† National National

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Master Selection Guide

MEMORY

† Military Temperature Range (-55°C to 125°C) * — Typical Values

IC UPDATE MASTER

MEMORY—EAROMs, FIFOs, LIFOs

Words	Bits/Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source
EAROMs Electrically Alterable, ROMs							
1	1	NMOS			±20	NOM201C	Plessey
	2	NMOS			±20	NOM202C	Plessey
	4	NMOS			±20	NOM204C	Plessey
8	8	MNOS			20	NOM401C	Plessey
	16	MNOS		Serial	±15	NC7030	Nitron
16	8	MNOS		Serial	±15	NC7030	Nitron
32	16	MNOS	4 μs		-29,5	ER2050	GI
64	1	MNOS	800 nsF		-30	NC7001	Nitron
100	4	MNOS	3.4 ms		-35	ER1400	GI
256	4	MNOS	2 μF		±12	1105 1105	GI NCR
512	2	MNOS	2 μs*	TS	-30	NC7002	Nitron
			25 μsR	TS	-30	NC7010	Nitron
1024	1	MNOS	2 μs*	TS	-30	NC7002	Nitron
			25 μsR	TS	-30	NC7010	Nitron NCR
	4	MNOS	2 μs		±5	ER2401	GI
Words	Bits/Word	Data Rate MHz (max)	Supply Voltage	Device	Source		
First-In First-Out							
4	4	—		CD40105B see page 375	† RCA		
				CD40105BE see page 375	RCA		
16	4	10.0	5	9403C 9403M	Fairchild † Fairchild		
	5	20.0	5	SN74S225	TI		
24	4	2.5	5-16	MS618	† Ragen		
32	8	0.25	-12,5	MP3812A MP3812B	† Plessey Plessey		
		0.5	-12,5 -12,5	AM2812C AM2812M	AMD † AMD		
		1.0	-12,5 -12,5	AM2812AC AM2812AM	AMD † AMD		
	9	0.25	-12,5	MP3813 MP3813A	Plessey † Plessey		
		0.5	-12,5 -12,5	AM2813C AM2813M	AMD † AMD		
		1.0	-12,5 -12,5	AM2813AC AM2813AM	AMD † AMD		
40	9	0.25	-12,5	FR1502E-02	Western		
		0.5	-12,5	FR1502E-01	Western		
		1.0	-12,5	FR1502E COM5014	Western SMC		
		2.0	-12,5 -12,5 -12,5	33511C 33511M 33512C	Fairchild † Fairchild Fairchild		
64	4	0.75	-12,5 -12,5	3341C 3341C	AMD Fairchild		
		1.0	-12,5 -12,5 -12,5 -12,5	AM2841C AM2841M 3341AC 3341AM	AMD † AMD Fairchild † Fairchild		
		2.0	-12,5 -12,5	ITT3341 ITT3342	ITT ITT		
		10.0	5 5	5741 6741	† MMI MMI		

Words	Bits/Word	Data Rate MHz (max)	Supply Voltage	Device	Source
First-In First-Out (cont)					
64	9	0.25	-12,5	TMS4024	TI
Last-In First-Out					
16	4	10.5	5	9404C 9404M	Fairchild † Fairchild

† Military Temperature Range (-55°C to 125°C)
OC—Open Collector

ns*—Nanoseconds Typical

nsF—Nanoseconds over Full Temperature Range
TS—Three-State

nsR—Nanoseconds at Room Temperature
OE—Open Emitte

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MEMORY—PROMs

Words	Bits/Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source
PROMs							
32	8	ECL	20 nsR	OE	-5.2	10139	† Signetics
				OE	-5.2	SN10139	TI
		TTL	40 nsF	OC	5	HM7602-5	Harris
						see page 746	see page 746
				TS	5	HM7603-5	Harris
						see page 746	see page 746
				OC	5	SN74S188	TI
				TS	5	SN74S288	TI
			50 nsF	OC	5	HM7602-2	† Harris
						see page 746	see page 746
				TS	5	HM7603-2	† Harris
						see page 746	see page 746
				OC	5	N82S23	Signetics
						see page 804, 826, 828,	see page 804, 826, 828,
				TS	5	N82S123	Signetics
						see page 804, 826, 828,	see page 804, 826, 828,
				OC	5	SN54S188	† TI
				TS	5	SN54S288	† TI
			50 nsR	OC	5	HPROM8256-2	Harris †
				OC	5	HPROM8256-5	Harris
				OC	5	IM5600C	Intersil
				OC	5	IM5600M	† Intersil
				TS	5	IM5610C	Intersil
				TS	5	IM5610M	† Intersil
				OC	5	5330	† MMI
				OC	5	6330	MMI
				TS	5	5331	† MMI
				TS	5	6331	MMI
				OC	5	DM7577	† National
				OC	5	DM8577	National
				TS	5	DM7578	† National
				TS	5	DM8578	National
				OC	5	SN54188A	† TI
				OC	5	SN74188A	TI
			55 nsF	OC	5	AM27LS08C	AMD
				TS	5	AM27LS09C	AMD
			65 nsF	OC	5	S82S23	† Signetics
						see page 804, 826, 828,	see page 804, 826, 828,
				TS	5	S82S123	† Signetics
						see page 804, 826, 828,	see page 804, 826, 828,
			70 nsR	OC	5	IM5600CF	Intersil
				TS	5	IM5610CF	Intersil
			75 nsF	OC	5	AM27LS08M	† AMD
				TS	5	AM27LS09M	† AMD
64	8	TTL	75 nsR	OC	5	JAN38510/201	Harris †
				OC	5	HPROM0512-2	Harris †
				OC	5	HPROM0512-5	Harris
				OC	5	MCM5003A	Motorola
					5	MCM5004A	Motorola
				OC	5	MCM5303A	† Motorola
					5	MCM5304A	† Motorola
				OC	5	SN54186	† TI
				OC	5	SN74186	TI
256	4	ECL	20 nsF	OE	-5.2	10149	Signetics
			25 nsR	OE	-5.2	MCM10149	Motorola
			25 ns*	OE	-5.2	10149	MMI

Words	Bits/Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source
PROMs (cont)							
256	4	ECL	50 ns*	OE	-5.2	F10416C	Fairchild
		TTL	40 nsF	OC	5	HM7610A-5	Harris
						see page 746	see page 746
				TS	5	HM7611A-5	Harris
						see page 746	see page 746
				OC	5	N82S27	Signetics
						see page 804, 826, 832,	see page 804, 826, 832,
			45 nsF	OC	5	93417C	Fairchild
				TS	5	93427C	Fairchild
			45 ns*	OC	5	DM54S387	† National
				TS	5	DM54S287	† National
			50 nsF	OC	5	3601-1	Intel
						see page 772, 773	see page 772, 773
				TS	5	3621-1	Intel
						see page 772, 773	see page 772, 773
				OC	5	DM74S387	National
				TS	5	DM74S287	National
				OC	5	N82S126	Signetics
						see page 804, 826, 835,	see page 804, 826, 835,
				TS	5	N82S129	Signetics
			60 nsF	OC	5	93417M	† Fairchild
				TS	5	93427M	† Fairchild
				OC	5	HM7610-5	Harris
						see page 746	see page 746
				TS	5	HM7611-5	Harris
						see page 746	see page 746
			60 nsR	OC	5	AM27LS10C	AMD
				OC	5	AM27LS10M	† AMD
				TS	5	AM27LS11C	AMD
				TS	5	AM27LS11M	† AMD
				OC	5	IM5603AC	Intersil
				OC	5	IM5603AM	† Intersil
				TS	5	IM5623C	Intersil
				TS	5	IM5623M	† Intersil
				OC	5	5300-1	† MMI
				OC	5	6300-1	MMI
				TS	5	5301-1	† MMI
				TS	5	6301-1	MMI
			65 nsF	OC	5	SN74S387	TI
				TS	5	SN74S287	TI
			70 nsF	OC	5	3601	Intel
						see page 772, 773	see page 772, 773
					5	3621	Intel
						see page 772, 773	see page 772, 773
				OC	5	S82S126	† Signetics
						see page 804, 826, 835,	see page 804, 826, 835,
				TS	5	S82S129	† Signetics
						see page 804, 826, 835,	see page 804, 826, 835,
			70 nsR	OC	5	HPROM1024A-2	Harris †
				OC	5	HPROM1024A-5	Harris
				TS	5	HPROM1024-2	Harris †
				TS	5	HPROM1024-5	Harris
			75 nsF	OC	5	HM7610-2	† Harris
						see page 746	see page 746
				TS	5	HM7611-2	† Harris
						see page 746	see page 746
				OC	5	SN54S387	† TI

† Military Temperature Range (-55°C to 125°C)
OC—Open Collector

ns*—Nanoseconds Typical

nsF—Nanoseconds over Full Temperature Range
TS—Three-State

nsR—Nanoseconds at Room Temperature
OE—Open Emitter

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MEMORY—PROMs (cont)

Bits/ Words	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source		
PROMs (cont)								
256	4 TTL	75 nsF	TS	5	SN54S287	† TI		
			OC	5	DM7573	† National		
			OC	5	DM8573	National		
			TS	5	DM7574	† National		
				TS	5	DM8574	National	
			90 nsF	OC	5	M3601	† Intel	
	8 TTL	60 nsF	TS	5	5	N82S114	Signetics see page 804, 826, 840,	
						SN74S470	TI	
				TS	5	5	SN74S471	TI
		80 nsF	OC	5	5	5	SN54S470	† TI
5							SN54S471	† TI
90 nsF		TS	5	5	5	S82S114	† Signetics see page 804, 826, 840,	
						5335-1	† MMI	
						6335-1	MMI	
						5336-1	† MMI	
			TS	5	5	6336-1	MMI	
PMOS Erasable	450 nsF	TS	-9,5	-9,5	1702A-1	Intel		
					MK3702	Mostek		
	650 nsF	TS	-9,5	-9,5	-9,5	1702A-2	Intel	
	750 nsF	TS	-9,5	-9,5	-9,5	9702-1	AMD	
						MM1702AQ-1	National	
	1 μsF	TS	-9,5	-9,5	-9,5	1702A	AMD	
						9702	AMD	
						1702A	Intel	
						MM1702AQ	National	
1 μsR	TS	-12,5	-12,5	-12,5	MM4203Q	National		
					MM5203Q	National		
1.3 μsF	TS	-9,5	-9,5	-9,5	8702A	AMD		
					8702A	Intel		
					see page 960			
		TS	-9,5	-9,5	MM8702A	National		
1.5 μsF	TS	-9,5	-9,5	-9,5	1702A-6	AMD		
					1702A-6	Intel		
					MM1702AQ-6	National		
1.7 μsF	TS	-10,5	-10,5	-10,5	4702A	AMD		
					4702A	Intel		
					MM4702A	National		
2.3 μsF	TS	-9,5	-9,5	-9,5	8702A-4	Intel		
					see page 960			
		TS	-9,5	-9,5	MM8702A-4	National		
PMOS	750 nsF	TS	-9,5	-9,5	1602A-1	Intel		
					MM1702AD-1	National		
	1 μsF	TS	-9,5	-9,5	-9,5	1602A	Intel	
						MM1702AD	National	
	1 μsR	TS	-12,5	-12,5	-12,5	MM4203D	National	
						MM5203D	National	
	1.5 μsF	TS	-9,5	-9,5	-9,5	1602A-6	Intel	
	512	4 TTL	50 nsF	OC	5	93436C	Fairchild	
				TS	5	93446C	Fairchild	
OC				5	HM7620A-5	Harris		
					see page 746			
TS				5	HM7621A-5	Harris		
					see page 746			
OC				5	N82S130	Signetics		
					see page 804, 826, 838,			

Bits/ Words	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source					
PROMs (cont)											
512	4 TTL	50 nsF	TS	5	N82S131	Signetics see page 804, 826, 838,					
			60 nsF	OC	5	93436M	† Fairchild				
				TS	5	93446M	† Fairchild				
			70 nsF	OC	5	5	HM7620-5	Harris			
							see page 746				
				TS	5	5	HM7621-5	Harris			
							see page 746				
			OC	5	5	3602	Intel				
						see page 774, 775					
TS	5	5	3622	Intel							
			see page 774, 775								
OC	5	5	S82S130	† Signetics							
			see page 804, 826, 838,								
TS	5	5	S82S131	† Signetics							
			see page 804, 826, 838,								
70 nsR	OC	5	5	5	5305-1	† MMI					
					6305-1	MMI					
					5306-1	† MMI					
					6306-1	MMI					
					IM5604C	Intersil					
					IM5604M	† Intersil					
					IM5624C	Intersil					
					IM5624M	† Intersil					
					85 nsF	OC	5	5	5	HM7620-2	† Harris
										see page 746	
	TS	5	5	5	HM7621-2	† Harris					
					see page 746						
90 nsF	OC	5	5	5	3602-4	Intel					
					see page 774, 775						
	TS	5	5	5	3622-4	Intel					
					see page 774, 775						
120 nsF	OC	5	5	5	3602L-6	Intel					
					3622L-6	Intel					
	TS	5	5	5	see page 774, 775						
PMOS Erasable	1 μsR	TS	-12,5	-12,5	-12,5	MM4203Q	National				
						MM5203Q	National				
						T3181A	Toshiba				
1.5 μsR	TS	-9,±5	-9,±5	-9,±5	T3181B	Toshiba					
PMOS	1 μsR	TS	-12,5	-12,5	-12,5	MM4203D	National				
						MM5203D	National				
8 TTL	55 nsF	OC	5	5	93438C	Fairchild					
			5	5	93448C	Fairchild					
			55 ns*	OC	5	5	5	SN54S473	† TI		
								SN74S473	TI		
								SN54S472	† TI		
								SN74S472	TI		
			70 nsF	OC	5	5	5	SN54S475	† TI		
								SN74S475	TI		
								SN54S474	† TI		
								SN74S474	TI		
60 nsF	TS	5	5	5	N82S115	Signetics					
					see page 804, 826, 840,						
93438M	† Fairchild	93448M	† Fairchild	HM7640-5	Harris						
						see page 746					

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Military Temperature Range (-55°C to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature C—Open Collector TS—Three-State OE—Open Emitter

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MEMORY—PROMs (cont)

Words	Bits/Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source
PROMs (cont)							
	70 nsF	TS	5			HM7641-5 see page 746	Harris
		OC	5			3604 see page 776, 777	Intel
		TS	5			3624 see page 776, 777	Intel
		OC	5			IM5605C	Intersil
		TS	5			IM5625C	Intersil
	80 nsF	OC	5			IM5605M	† Intersil
		TS	5			IM5625M	† Intersil
	85 nsF	OC	5			HM7640-2 see page 746	† Harris
		TS	5			HM7641-2 see page 746	† Harris
	90 nsF	TS	5			S82S115 see page 804, 826, 840,	† Signetics
	90 nsR	OC	5			5340-1	† MMI
		OC	5			6340-1	MMI
		TS	5			5341-1	† MMI
		TS	5			6341-1	MMI
	120 nsF	TS	5			3604L-6 see page 776, 777	Intel
	NMOS Erasable 450 nsF	TS	±5,12			2704 see page 770, 771	Intel
	1 μsF	TS	±5,12			2704-5 see page 770, 771	Intel
	PMOS Erasable 575 nsF	TS	-12,5			S6834 see page 912	AMI
	750 nsF	TS	-12,5			S5204A see page 706	AMI
	1 μsF	TS	-12,5			MM5204	National
	1.25 μsF	TS	-12,5			MM4204	National
1024	4 TTL	60 nsF	OC	5		6350	MMI
			TS	5		6351	MMI
			OC	5		N82S136	Signetics
			TS	5		N82S137	Signetics
		70 nsF	OC	5		HM7642-5	Harris
			TS	5		HM7643-5	Harris
			—	5		HM7644-5	Harris
			OC	5		3605	Intel
			TS	5		3625	Intel
		75 nsF	OC	5		5350	† MMI
			TS	5		5351	† MMI
		85 nsF	OC	5		HM7642-2	† Harris
			TS	5		HM7643-2	† Harris
			—	5		HM7644-2	† Harris
	8 NMOS Erasable 450 nsF	TS	±5,12			2708 see page 770, 771	Intel
	1 μsF	TS	±5,12			2708-5 see page 770, 771	Intel
	TTL	70 ns*	OC	5		5380	† MMI
			OC	5		6380	MMI
			TS	5		5381	† MMI
			TS	5		6381	MMI
Field Programmable Logic Arrays							
	48 Product Terms	55	OC			82S100/82S101 see page 845	Signetics
			TS				

Words	Bits/Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source
Field Programmable Logic Arrays (cont)							
1024	48 Product Terms					6870 6871	MMI MMI
			100	—	5	IM5200 5870 5871	Intersil † MMI † MMI

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† Military Temperature Range (-55°C to 125°C)
OC—Open Collector

ns*—Nanoseconds Typical

nsF—Nanoseconds over Full Temperature Range
TS—Three-State

nsR—Nanoseconds at Room Temperature
OE—Open Emitter

MEMORY—RAMs

Words	Bits/Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source	Words	Bits/Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source	
Dynamic								Dynamic (cont)								
1024	1	NMOS	60 nsF	±15 -5,12		EA1500A SY7103	EA Synertek	1024	1	PMOS	800 nsF		-12,5	S4008-9 see page 706	AMI	
			80 nsF	-5,12		2105-1	Intel									
			85 nsF	-5,2,12		2105-2	Intel	2048	1	PMOS	350 nsF		-15,8,5 -15,8,5	AMS600311 600311	AMS Nortec	
			95 nsF	-5,12		2105	Intel				365 nsF		-15,8,5,5	MM5262	National	
			120 nsF	±15		EA1500A-1	EA				420 nsF		-15,8,5,5	MM4262	† National	
	PMOS		100 nsF		19,22.5	SY1103A-X	Synertek				460 nsF		-15,8,5,5 -15,8,5,5	AMS600310 600314	AMS Nortec	
			110 nsF		19,22.5	1103A-X	Rockwell	4096	1	NMOS	150 nsF	TS	±5,12	MCM6605A-1	Motorola	
			120 nsF		19,22.5	S1103X see page 707	AMI					TS	±5,12	IM7505A-1	Intersil	
					19,22.5	ITT1103-X	ITT					TS	5,12	μPD411-3	NEC	
			125 nsF		19,22.5	S1103A-X see page 712	AMI				175 nsF	TS	±5,12	RM1701H-17	Western	
			145 nsF		19,22.5	S1103A-1 see page 712	AMI				200nsF	TS	±5,12	AMS7005	AMS	
					19,22.5	1103A-1	Fairchild					TS	±5,12	AMS7280	AMS	
					19,22.5	1103A-2	Fairchild					TS	-5,12	AMS7270	AMS	
					19,22.5	1103A-1	Intel					TS	-5,12	AMS7271	AMS	
					19,22.5	1103A-2	Intel					TS	-5,12	9060E	AMD	
					19,22.5	1103A-1	Rockwell					TS	±5,12	9050E	AMD	
					19,22.5	1103A-2	Rockwell					TS	-5,12	9107	AMD	
					19,22.5	SY1103A-1	Synertek					TS	±5,12	S4021-4 see page 722	AMI	
			150 nsF		19,22.5	S1103-1 see page 707	AMI					TS	±5,12	S4096 see page 728	AMI	
					20,22.5,7	AMS6002	AMS					TS	±5,12	S4096-4	AMI	
					19,22.5	11031C	Fairchild					TS	±5,12	EA4060	EA	
					19,22.5	HM3503-1	Hitachi					TS	±5,12	EA4116	EA	
					19,22.5	1103-1	Intel					TS	±5,12	EA4122-2	EA	
					19,22.5	ITT1103-1	ITT					TS	±5,12	4096-2	Fairchild	
					19,22.5	1103-1	Nortec					TS	±5,12	2107B see page 760, 765	Intel	
					20,22.5,7	6002	Nortec					TS	±5,12	IM7505A-2	Intersil	
					19,22.5	1103-1	Signetics					TS	±5,12	IM7507-2	Intersil	
					19,22.5	TMS1103-1	TI					TS	±5,12	2180	MMI	
					20,22,7	TMS4062	TI					TS	-5,12	2170	MMI	
					20,22,7	TMS4063	TI					TS	±5,12	MK4027	Mostek	
			205 nsF		19,22.5	S146	AMI					TS	±5,12	MCM6605A-2	Motorola	
					16,19.5	S1103A see page 712	AMI					TS	±5,12	MM5280	National	
					16,19.5	1103A	Fairchild					TS	±5,12	MM5270	National	
					16,19.5	1103A	Intel					TS	±5,12	MW4060V2	RCA	
					19,22.5	ITT1103-146	ITT					TS	-5,12	MW4050V2	RCA	
					19,22.5	1103-146	Nortec					TS	±5,12	1604-1	Rockwell	
					16,22.5	1103A	Rockwell					TS	-5,12	2670-1	Signetics	
					16,19.5	SY1103A	Synertek					TS	±5,12	TMS4030-2	TI	
			220 nsF		16,19.5	1103SC	Fairchild					TS	±5,12	TMS4060-2	TI	
						HM3503-2	Hitachi					TS	-5,12	TMS4050-2	TI	
			300 nsF		16,19.5	S1103 see page 707	AMI					TS	±5,12	RM1701H-20	Western	
					16,19.5	1103C	Fairchild					TS	-3,5,12			
					16,19.5	HM3503	Hitachi					TS	±5,12	220 nsF	TS	±5,12
					16,19.5	1103	Intel					TS	±5,12	250 nsF	TS	±5,12
					16,19.5	ITT1103	ITT					TS	±5,12	S4021-3 see page 722	AMI	
					16,19.5	1103	Nortec					TS	±5,12	S4096-3 see page 728	AMI	
					16,19.5	1103	Signetics					TS	±5,12	9060D	AMD	
					16,19.5	TMS1103	TI					TS	-5,12	9050D	AMD	
			400 nsF		-12,5	S4006 see page 706	AMI					TS	±5,12	EA4060-1	EA	
					-12,5	MK4006	Mostek					TS	±5,12	EA4122-1	EA	
					-12,5,7	MM5261	National					TS	±5,12	40963	Fairchild	
			450 nsF		-12,5,7	MM4261	† National					TS	±5,12			
			500 nsF		-12,5	S4008 see page 706	AMI					TS	±5,12			
					-12,5	MK4008	Mostek					TS	±5,12			

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Military Temperature Range (-55°C to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
C—Open Collector TS—Three-State OE—Open Emitter

MEMORY—RAMs (cont)

Words	Bits/Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source	Words	Bits/Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source			
Dynamic (cont)								Dynamic (cont)										
4096	1	NMOS	250 nsF	TS	±5,12	2104-2 see page 752, 759	Intel	4096	1	NMOS	350 nsF	TS	±5,12	2104 see page 752, 759	Intel			
				TS	±5,12	IM7507-1	Intersil					TS	±5,12	2107A-4	Intel			
				TS	±5,12	MK4096-6 see page 778, 781	Mostek					TS	±5,12	2107B-6 see page 760, 765	Intel			
				TS	±5,12	MCM6604-2	Motorola					TS	±5,12	2180	MMI			
				TS	±5,12	1604-2	Rockwell					TS	-5,12	2170	MMI			
				TS	-5,12	2670-2	Signetics					TS	±5,12	MK4096-11 see page 778, 781	Mostek			
				TS	-3,5,12	TMS4030-1	TI					TS	±5,12	MK4200-11 see page 783	Mostek			
				TS	±5,12	TMS4060-1	TI					TS	±5,12	MCM6604	Motorola			
					-5,12	TMS4050-1	TI					TS	±5,12	1604	Rockwell			
					-5,12	TMS4051-1	TI					TS	±5,12	RM1701H-35	Western			
				TS	±5,12	RM1701H-25	Western											
			270 nsF	TS	-5,12	9107-4	AMD				400 nsF	TS	±5,12	S4021 see page 722	AMI			
				TS	±5,12	2107B-4 see page 760, 765	Intel					TS	±5,12	RM1701H-40	Western			
				TS	±5,12	2180	MMI				420 nsF	TS	±5,12	2107A-5	Intel			
				TS	-5,12	2170	MMI					TS	±5,12	2107A-8	Intel			
				TS	±5,12	MW4060V1	RCA				450 nsF	TS	±5,12	RM1701H-45	Western			
				TS	±5,12	MW4050V1	RCA				510 nsF	TS	±5,12	S4096 see page 728	AMI			
			280 nsF	TS	±5,12	2107A-1	Intel											
			300 nsF	TS	±5,12	9060C	AMD				8192	1	NMOS	125 nsF	AMS7008			
					-5,12	9050C	AMD							±5,12	CCD460	Fairchild		
				TS	±5,12	S4021-2 see page 722	AMI				CCDR Memories							
				TS	±5,12	S4096-2 see page 728	AMI				9216-Bits (1024x9)							
				TS	±5,12	EA4060-2	EA				16384-Bits (128x32x4)							
				TS	±5,12	EA4122	EA				16384-Bits (256 x 64 x 1)							
				TS	±5,12	40964	Fairchild				Static							
				TS	±5,12	HM4503-1	Hitachi				4	4	CMOS	1 μsR	—	45-16	MC14580A	† Motorola
				TS	±5,12	HM4507	Hitachi							1.5 μsR	—	3-18	MC14580C	Motorola
				TS	±5,12	2104-4 see page 752, 759	Intel								3-18	SCL4580	SSS	
				TS	±5,12	2107A	Intel					TTL	30 nsF	OC	5	3104	Intel	
				TS	±5,12	IM7505A	Intersil							40 nsR	OC	5	54170	† Fairchild
				TS	±5,12	IM7507	Intersil									5	54LS170	† Fairchild
				TS	±5,12	MK4096-16 see page 778, 781	Mostek									5	54LS670	† Fairchild
				TS	±5,12	MK4200-16 see page 783	Mostek									5	74170	Fairchild
				TS	±5,12	MCM6604-4	Motorola									5	74LS170	Fairchild
				TS	±5,12	MCM6605A	Motorola									5	74LS670	Fairchild
				TS	±5,12	MW4060	RCA									5	54170	† Raytheon
				TS	±5,12	MW4050	RCA									5	74170	Raytheon
				TS	±5,12	2604 see page 793	Signetics									5	SN54170	† TI
				TS	-5,12	2670-3	Signetics									5	SN54LS170	† TI
				TS	±5,12	TMS4060	TI									5	SN54LS670	† TI
					-5,12	TMS4050	TI									5	SN54LS670	† TI
					-5,12	TMS4051	TI									5	SN74170	TI
				TS	-3,5,12	TMS4030	TI									5	SN74LS170	TI
				TS	±5,12	RM1701H	Western									5	SN74LS670	TI
				TS	±5,12	RM1701H-30	Western									5		
			350 nsF	TS	±5,12	9107-6	AMD				8	2	ECL	14.5 nsR	—	3-15	CD4036A see page 375	† RCA
				TS	±5,12	S4096-1 see page 728	AMI									3-15	CD4039A see page 375	† RCA
				TS	±5,12	4096-3	Fairchild									3-15	CM4036A	† Solitron
																3-15	CM4039A	† Solitron
											8	2	ECL	14.5 nsR	—	-5.2	MCM10143	Motorola
																5	SN74172	TI
																5	N82512 see page 804, 806, 810,	Signetics

† Military Temperature Range (-55°C to 125°C)
OC—Open Collector

ns*—Nanoseconds Typical

nsF—Nanoseconds over Full Temperature Range
TS—Three-State

nsR—Nanoseconds at Room Temperature
OE—Open Emitter

Bold face indicates additional data is provided on the page noted.

MEMORY—RAMs (cont)

Words	Bits/Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source			
Static (cont)										
8	4	TTL	30 nsF	TS	5	N82S112	Signetics see page 804, 806, 810,			
16	1	ECL	12 nsR	OE	12	HM2101	Hitachi			
				TTL	20 nsR	OC	5	5481	† Raytheon	
						OC	5	7481	Raytheon	
						OC	5	SN5481A	† TI	
						OC	5	SN5484A	† TI	
						OC	5	SN7481A	TI	
	OC	5	SN7484A	TI						
	4	CMOS	120 nsR	TS	3-5	F4710	Fairchild			
						280 nsR	TS	3-15	HD54C89	† Harris
									HD74C89	Harris
									MM54C89	† National
									MM74C89	National
									MM54C89	† Teledyne S
						MM74C89	† Teledyne S			
ECL						6 ns*	OE	-5.2	SN10145	TI
	10 ns*	OE	-5.2	HD10145	Hitachi					
				MCM10145	† Motorola					
	15 nsR	OE	-5.2	10145	Signetics					
25 nsF	-5.2	F95400C	Fairchild							
PMOS	400 ns*	—	-27,-15	CRC4001	Collins					
				TTL	35 nsF	OC	5	AM27S02M	† AMD	
AM27S03C	AMD									
SN74S189	AMD									
SN74S289	AMD									
93404C	Fairchild									
93404A	† Fairchild									
93405C	Fairchild									
93405M	† Fairchild									
3101A	Intel									
6560	MMI									
6561	MMI									
DM74S289	National									
DM74S189	National									
N3101A	Signetics see page 804, 806, 814,									
N74S189	Signetics									
SN74S189	TI									
SN74S289	TI									
35 nsR	TS	5	AM27S03M	† AMD						
45 nsF	OC	5	M3101A	† Intel						
45 nsR	OC	5	MC5484	† Motorola						
			MC7484	Motorola						
			DM7599	† National						
			DM8599	National						
			50 nsF	TS	5	SN54S189	† AMD			
OC	5	SN54S289	† AMD							
OC	5	DM54S289	† National							
TS	5	DM54S189	† National							
OC	5	N82S25	Signetics see page 804, 806, 814,							

Words	Bits/Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source				
Static (cont)											
16	4	TTL	50 nsF	OC	5	S3101A	† Signetics see page 804, 806, 814,				
							TS	5	S54S189	† Signetics	
									SN54S189	† TI	
				SN54S289	† TI						
				60 nsF	OC	5	3101	AMD			
							3101	Intel			
							5560	† MMI			
							5561	† MMI			
							60 nsR	OC	5	7489	Fairchild
				HM2502	Hitachi						
				IM5501C	Intersil						
				IM5501M	† Intersil						
				MCM4064L	Motorola						
				MCM4364	† Motorola						
DM5489	† National										
DM7489	National										
SN7489	TI										
7489	TRW										
75 nsF	OC	5	31013	† AMD							
			M3101	† Intel							
80 nsF	OC	5	L6560	MMI							
			L6561	MMI							
100 nsF	OC	5	L5560	† MMI							
			L5561	† MMI							
110 nsR	OC	5	31L01C	AMD							
			31L01M	† AMD							
150 nsR	OC	5	DM54L89A	† National							
			DM74L89A	National							
			DM76L99	† National							
			DM86L99	National							
16+1	4	TTL	19 nsF	TS	5	9410C	Fairchild				
32	2	TTL	50 nsF	OC	5	DM86S21	National				
				OC	5	N82S21	Signetics see page 804, 806, 812,				
64	1	CMOS	270 nsR	—	3-18	MCM14505A	† Motorola				
						350 nsR	—	4.5-16	MCM14505C	Motorola	
			ECL	10 nsR	OE	-5.2	SN10142	TI			
							12 nsR	OE	-5.2	MCM10140	Motorola
										MCM10142	Motorola
										MCM10148	Motorola
							15 nsR	OE	-5.2	10140	Signetics
										10148	Signetics
										10151	Signetics
										SN10140	TI
SN10148	TI										
4	CMOS	200 ns*	TS	5-15	5	SCM5555D	SSS				
					5	MM74C910	National				
					1.05 μsR	5-15	MCM14552A	† Motorola			
8	NMOS	450 nsF	TS	5	TMS4036-2	TI					
					650 nsF	TS	5	TMS4036-1	TI		
9	TTL	45 nsF	OC	5	93419C	Fairchild					
					OC	5	N82S09	Signetics see page 804, 806, 817,			

† Military Temperature Range (-55°C to 125°C)
OC—Open Collector

ns*—Nanoseconds Typical

nsF—Nanoseconds over Full Temperature Range
TS—Three-State

nsR—Nanoseconds at Room Temperature
OE—Open Emitter

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MEMORY—RAMs (cont)

Words	Bits/Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source	
Static (cont)								
64	9	TTL	60 nsF	OC	5	93419M	† Fairchild	
					5	6555	MMI	
			65 nsF	OC	5	S82S09	† Signetics	
			80 nsF		5	5555	† MMI	
128	1	ECL	12 nsR	OE	-5.2	MCM10147	Motorola	
			15 nsF	OE	-5.2	F10405C	Fairchild	
			15 nsR	OE	-5.2	SN10147	TI	
8	NMOS		500 nsF	TS	5	MCM6810A	Motorola	
			575 nsF	TS	5	S6810-1	AMI	
			1 μsF	TS	5	S6810	AMI	
256	1	CMOS	100 nsF	TS	3-15	SCM5520S	† SSS	
			100 ns*	TS	10	CD40061	RCA	
			200 ns*	TS	3-15	F4720	Fairchild	
					3-15	CD4061A	† RCA	
					see page 375			
			400 nsR	TS	3-15	HD54C200	† Harris	
				TS	3-15	HD74C200	Harris	
				TS	3-15	MM54C200	† National	
				TS	3-15	MM74C200	National	
				TS	3-15	MM54C200	† Teledyne S	
				TS	3-15	MM74C200	Teledyne S	
			500 nsR	—	3-7	IM6523C	Intersil	
					3-7	IM6523M	† Intersil	
			1.4 μsR	—	3-18	MCM14537A	† Motorola	
			2 μsR	—	3-16	MCM14537C	Motorola	
			ECL	30 nsF	OE	-5.2	F10410C	Fairchild
					OE	-5.2	10144	Signetics
			30 nsR	OE	-5.2	MCM10144	Motorola	
				35 nsF	OE	-4.25	F10411C	Fairchild
				OE	-5.2	HM2105	Hitachi	
				OE	-5.2	RC10144	Raytheon	
			35 nsR	OE	-5.2	SN10144	TI	
				40 nsF	OE	-5.2	F95410C	Fairchild
	OE	-5.2	HM2104	Hitachi				
	OE	-5.2	RI10144	Raytheon				
PMOS	500 nsF	TS	-9.5	MM1101A2	National			
		650 nsF	TS	-9.5	MM4250	† National		
		800 nsF	—	-7.5	IM7511C	Intersil		
		900 nsF	—	-12.5	MK4007	Mostek		
		1 μsF	TS	-9.5	1101A1	AMD		
			TS	-9.5	1101A1	Intel		
			TS	-7.5	IM7511M	† Intersil		
			TS	-9.5	MM1101A1	National		
			TS	-9.5	1101	Signetics		
		1.5 μsF	TS	-9.5	2501	Signetics		
TS	-12.5		N25L01	Signetics				
TS	-7.5		μA2556	† Solitron				
TS	TS	-9.5	1101A	AMD				
	TS	-10.5	1101AM	† AMD				
	TS	-9.5	1101A	Intel				
	TS	-7.5	IM7501C	Intersil				
	TS	-7.5	IM7501M	† Intersil				
	TS	-7.5	IM7512C	Intersil				
	TS	-9.5	MM1101A	National				

Words	Bits/Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source
Static (cont)							
256	1	PMOS	1.8 μsF	TS	-7.5	IM7512M	† Intersil
		TTL	36 nsF	TS	5	AM27LS00AC	AMD
			40 nsF	TS	5	93421AC	Fairchild
				TS	5	N82S116	Signetics
				OC	5	N82S117	Signetics
				see page 804, 806, 815,			
45 nsF				OC	5	AM27LS01C	AMD
				TS	5	AM27LS00C	AMD
				TS	5	AM27LS00AM	AMD
				OC	5	93410AC	Fairchild
				OC	5	93411AC	Fairchild
50 nsF				TS	5	93421C	Fairchild
				TS	5	RC5340	Raytheon
				OC	5	N82S17	Signetics
				TS	5	see page 804, 806, 815,	
				OC	5	N82S16	Signetics
				OC	5	see page 804, 806, 815,	
				TS	5	N74S301	Signetics
				TS	5	see page 804, 806, 815,	
				TS	5	N74S200	Signetics
				TS	5	N74S201	Signetics
				see page 804, 806, 815,			
50 ns*				OC	5	DM8582	† National
				TS	5	DM74S200	National
55 nsF				OC	5	AM27LS01M	† AMD
				TS	5	AM27LS00M	† AMD
				OC	5	93411C	Fairchild
				OC	5	93420M	† Fairchild
				OC	5	6530	MMI
60 nsF				TS	5	6531	MMI
				OC	5	RC5330	Raytheon
				OC	5	93410C	Fairchild
				TS	5	93421M	† Fairchild
				TS	5	3106A	Intel
				OC	5	3107A	Intel
				OC	5	IM5503AC	Intersil
				TS	5	IM5523AC	Intersil
				OC	5	IM5533AC	Intersil
				OC	5	DM74S206	National
65 nsF				OC	5	93411M	† Fairchild
				TS	5	HM2505	Hitachi
				OC	5	S93410A	† Signetics
				TS	5	SN74S201	TI
				OC	5	SN74S301	TI
70 nsF				OC	5	93410M	† Fairchild
				OC	5	IM5503AM	† Intersil
				TS	5	IM5523AM	† Intersil
				OC	5	IM5533AM	† Intersil
				OC	5	5530	† MMI
				TS	5	5531	† MMI
				TS	5	DM54S200	† National
				TS	5	RM5340	† Raytheon
				OC	5	S82S17	† Signetics
				TS	5	S82S16	† Signetics

† Military Temperature Range (-55°C to 125°C)
OC—Open Collector

ns*—Nanoseconds Typical

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TS—Three-State

nsR—Nanoseconds at Room Temperature
OE—Open Emitter

MEMORY—RAMs (cont)

Bits/ Words	Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source																																				
Static (cont)																																											
256	1	TTL	70 nsF	OC	5	S54S301 † Signetics see page 804, 806, 815, S54S200 † Signetics see page 804, 806, 815, S54S201 † Signetics see page 804, 806, 815,																																					
				TS	5																																						
				TS	5																																						
	75 nsF	OC	5	5	5	RM55330 † Raytheon																																					
								80 nsF	TS	5	5	3106-8 Intel																															
														OC	5	5	3107-8 Intel																										
																			TS	5	5	3106- Intel																					
																								OE	5	5	3107- Intel																
																			OC	5	5	IM5503C Intersil																					
								TS	5	5	IM5523C Intersil																																
													OC	5	5	IM5533C Intersil																											
								OC	5	5	DM54S206 † National																																
													80 nsR	OC	5	5	5	IM5503M † Intersil																									
	TS	5	5	IM5523M † Intersil																																							
						OC	5	5	IM5533M † Intersil																																		
	85 nsF	OC	5	5	5	SN54S301 † TI																																					
								TS	5	5	SN54S201 † TI																																
	90 nsF	TS	5	5	5	93L421C Fairchild																																					
								100 nsF	TS	5	5	93L421M † Fairchild																															
	115 nsF	OC	5	5	5	L6530 MMI																																					
TS								5	5	L6531 MMI																																	
130 nsF	OC	5	5	5	L5530 † MMI																																						
							TS	5	5	L5531 † MMI																																	
4	CMOS	100 nsF	TS	5	5	SCL5501S † SSS																																					
								100 nsR	TS	4-11	5	5	HM6551A-9 Harris																														
															TS	4-11	5	5	HM6561A-9 Harris																								
																					TS	4-11	5	5	HM6562A-9 Harris																		
																											TS	4-11	5	5	HM6551A-2 † Harris												
																																	TS	4-11	5	5	HM6561A-2 † Harris						
																																							TS	4-11	5	5	HM6562A-2 † Harris
								100 ns*	TS	10	5	5	MWS5540 RCA see page 786																														
								150 ns*	TS	5	5	5	MWS5040 RCA see page 786																														
								160 nsR	TS	4-11	5	5	5	HM6551C-9 Harris																													
																TS	4-11	5	5	5	HM6561C-9 Harris																						
																							TS	4-11	5	5	5	HM6562C-9 Harris															
																														TS	4-11	5	5	5	HM6551C-2 † Harris								
																																					TS	4-11	5	5	5	HM6561C-2 † Harris	
								305 nsF	TS	5	5	5	5	5	HM6551B-9 Harris																												
																	TS	5	5	5	5	5	HM6561B-9 Harris																				
																									TS	5	5	5	5	5	HM6562B-9 Harris												
																																	TS	5	5	5	5	5	HM6551B-2 † Harris				
																																									TS	5	5
TS	5	5	5	5	5	HM6562B-2 † Harris																																					
425 nsF	TS	5	5	5	5	5	HM6551-9 Harris																																				
									TS	5	5	5	5	5	HM6561-9 Harris																												
																	TS	5	5	5	5	5	HM6562-9 Harris																				
450 nsF	TS	5	5	5	5	5101-1 Intel see page 960																																					
465 nsF	TS	5	5	5	5	5	HM6551-2 † Harris																																				
									TS	5	5	5	5	5	HM6561-2 † Harris																												

Bits/ Words	Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source																																																																																
Static (cont)																																																																																							
256	4	CMOS	465 nsF	TS	5	5	HM6562-2 † Harris																																																																																
								650 nsF	TS	5	5	5	S5101 AMI see page 716																																																																										
														TS	5	5	5101 Intel see page 960																																																																						
																		TS	5	5	5101L Intel see page 960																																																																		
								TS	5	5	5	5	5101-3 Intel see page 960																																																																										
														TS	5	5	5	5	5101L-3 Intel see page 960																																																																				
								TS	5	5	5	5	SY5101 Synertek																																																																										
														TS	5	5	5	5	SY5111 Synertek																																																																				
								TS	5	5	5	5	SY5112 Synertek																																																																										
														800 nsF	TS	5	5	5	M5101-4 Intel																																																																				
								850 nsF	TS	5	5	5	5101-8 Intel see page 960																																																																										
														NMOS	150 nsF	TS	5	5	5	SY21H01-1 Synertek																																																																			
								TS	5	5	5	SY21H11-1 Synertek																																																																											
													TS								5	5	5	SY21H12-1 Synertek																																																															
								175 nsF	TS	5	5	5	5	SY21H01 Synertek																																																																									
TS	5	5	5	SY21H11 Synertek																																																																																			
					TS	5	5								5	SY21H12 Synertek																																																																							
200 nsF	TS	5	5	5	5	SY21H01-2 Synertek																																																																																	
							TS	5	5	5	SY21H11-2 Synertek																																																																												
200 ns*	TS	±5,12	5	5	5	MW7040 RCA																																																																																	
							250 nsF	TS	5	5	5	5	AMS7101 AMS																																																																										
TS	5	5	5	5	5	AMS7111 AMS																																																																																	
							TS	5	5	5	5	5	AMS7112 AMS																																																																										
TS	5	5	5	5	5	9101D AMD																																																																																	
							TS	5	5	5	5	5	9111D AMD																																																																										
TS	5	5	5	5	5	9112D AMD																																																																																	
							TS	5	5	5	5	5	SY2101A-2 Synertek																																																																										
TS	5	5	5	5	5	SY2111A-2 Synertek																																																																																	
							TS	5	5	5	5	5	SY2112A-2 Synertek																																																																										
300 nsF	TS	5	5	5	5	5								91L01C AMD																																																																									
							TS	5	5	5	5	5	5		9101C AMD																																																																								
																TS	5	5	5	5	5	5	9101CM † AMD																																																																
																								TS	5	5	5	5	5	5	91L11C AMD																																																								
																																TS	5	5	5	5	5	5	9111C AMD																																																
																																								TS	5	5	5	5	5	5	9111CM † AMD																																								
																																																TS	5	5	5	5	5	5	91L12C AMD																																
																																																								TS	5	5	5	5	5	5	9112C AMD																								
																																																																TS	5	5	5	5	5	5	9112CM † AMD																
																																																																								TS	5	5	5	5	5	5	EA2101 EA								
																																																																																TS	5	5	5	5	5	5	EA2111 EA
350 nsF	TS	5	5	5	5	5	3538F Fairchild																																																																																
								TS	5	5	5	5	5	SY2101A Synertek																																																																									
															TS	5	5	5	5	5	SY2111A Synertek																																																																		
																						TS	5	5	5	5	5	SY2112A Synertek																																																											
400 nsF	TS	5	5	5	5	5	91L01B AMD																																																																																
								TS	5	5	5	5	5	9101B AMD																																																																									
															TS	5	5	5	5	5	9101BM † AMD																																																																		
																						TS	5	5	5	5	5	91L11B AMD																																																											

60
70
80
90
100

MEMORY Master Selection Guide

† Military Temperature Range (-55°C to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY—RAMs (cont)

Words	Bits/ Word	Type	Access Time (Max.)	Output	Supply Voltage	Device		Source	Words	Bits/ Word	Type	Access Time (Max.)	Output	Supply Voltage	Device		Source														
						Device	Source								Device	Source															
Static (cont)									Static (cont)																						
10	256	4 NMOS	400 nsF	TS	5	9111B	AMD		256	4 NMOS	650 nsF	TS	5	RA3-4256-C	GI																
						9111BM	† AMD							RA-4256-E	GI																
						91L12B	AMD							2101-2	Intel																
						9112B	AMD							2111-2	Intel																
						9112BM	† AMD							2112-2	Intel																
						EA2101M	† EA							MM2101-2	National																
						EA2111M	† EA							MM2111-2	National																
						EA2112M	† EA							MM2112-2	National																
						35L38B	Fairchild							SY2101-2	Synertek																
	20	450 nsF	TS	5	3538-1	Fairchild		750 nsF	TS	5	2606	see page 798	Signetics																		
					RA3-4256-A1	GI																									
					RA3-4256-C1	GI																									
					RA3-4256-E1	GI																									
					SY2101A-4	Synertek																									
					SY2111A-4	Synertek																									
					SY2112A-4	Synertek																									
					TMS4039-2	TI																									
					TMS4042-2	TI																									
					TMS4043-2	TI																									
					30	500 nsF	TS							5	2101-1	AMD		1 μsF	TS	5	2101	AMD									
															2111-1	AMD					2111	AMD									
	2112-1	AMD		2112				AMD																							
	91L01A	AMD		RA3-4256				EMM/Semi																							
	9101A	AMD		RA3-4256B				EMM/Semi																							
9101AM	† AMD		2101	Intel																											
91L11A	AMD		2111	Intel																											
9111A	AMD		2112	Intel																											
9111AM	† AMD		MM2101	National																											
91L12A	AMD		MM2111	National																											
9112A	AMD		MM2112	National																											
40	500 nsF	TS	5	9112AM				† AMD		TTL	30 ns*	OC	5		93412C	Fairchild															
				RA3-4256	EMM/Semi		93422C	Fairchild																							
				35L38A	Fairchild		93412M	† Fairchild																							
				RA3-4256	GI		93422M	† Fairchild																							
				2101-1	Intel																										
				2111-1	Intel																										
				2112-1	Intel																										
				MM2101-1	National																										
				MM2111-1	National																										
				2606-1	Signetics																										
				SY2111	Synertek																										
				SY2112	Synertek																										
50	650 nsF	TS	5	SY2113	Synertek		8 NMOS	400 nsF	TS	5	3539-1	Fairchild																			
				SY2101-1	Synertek						500 nsF	TS	5	3539-2	Fairchild																
				SY2111-1	Synertek									600 nsF	TS	5	3539	Fairchild													
				SY2112-1	Synertek																										
				50	650 nsF	TS					5	2101-2	AMD		1 CMOS	200 nsF	10	S2222	see page 706	AMI											
												2111-2	AMD								400 nsF	10	S2222A	see page 706	AMI						
												2112-2	AMD													10	2222	Nortec			
												RA3-4256B	EMM/Semi																		
												RA3-4256A	EMM/Semi																		
												3538-2	Fairchild																		
												35L38	Fairchild																		
RA3-4256-A	GI																														
50	1024	1 CMOS	80 ns*				TS	10	MWS5501	see page 786		RCA	5 NMOS	450 nsF							TS	5	RO3-2560	GI							
									MWS5502	see page 786		RCA																			

† Military Temperature Range (–55°C to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
 OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY—RAMs (cont)

Words	Bits/Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source
Static (cont)							
1024	1	CMOS	150 nsF	TS	5	MWS5002 MWS5502 see page 786	RCA RCA
			160 nsR	TS	4-11	HM6508C-9	Harris
				TS	4-11	HM6518C-9	Harris
				TS	4-11	HM6508C-2	† Harris
				TS	4-11	HM6518C-2	† Harris
			250 nsF		3-10	IM6508C	Intersil
					3-10	IM6508M	† Intersil
					3-10	IM6518C	Intersil
					3-10	IM6518M	† Intersil
			305 nsF	TS	5	HM6508B-9	Harris
				TS	5	HM6518B-9	Harris
				TS	5	HM6508B-2	† Harris
				TS	5	HM6518B-2	† Harris
			425 nsF	TS	5	HM6508-9	Harris
				TS	5	HM6518-9	Harris
			465 nsF	TS	5	HM6508-2	† Harris
				TS	5	HM6518-2	† Harris
			1.5 μsF		5	TC5006	Toshiba
ECL							
			30 nsF		-4.5	F100415C	Fairchild
			35 nsF	OE	-5.2	F10415AC	Fairchild
			35 nsR	OE	-5.2	10146	Signetics
			60 nsF	OE	-5.2	F10415C	Fairchild
			75 nsF		-5.2	F95415C	Fairchild
NMOS							
			60 nsF		-3,7,15	AMS7001	AMS
					-3,7,15	MCM7001	Motorola
					-3,7,15	7001	Nortec
					-3,7,15	MW7001I	RCA
			70 nsF		-3,5,15	1802	EMM/Semi
					-3,5,15	RA3-1802	GI
				OC	5	2115-2	Intel
						see page 766, 769	
				TS	5	2125-2	Intel
						see page 766, 769	
			75 nsF		-3,7,15	MCM7001-1	Motorola
			90 nsF	TS	-3,5,15	1801	EMM/Semi
				TS	-3,5,15	RA3-1801	GI
				OC	5	2115	Intel
						see page 766, 769	
				TS	5	2125	Intel
						see page 766, 769	
			95 nsF	OC	5	2115L	Intel
				TS	5	2125L	Intel
						see page 766, 769	
			100 nsR	OC	5	IM5508C	Intersil
			100 nsF		-3,5,5,15	1218A	EMM/Semi
			120 nsF		-3,5,5,15	1218	EMM/Semi
				TS	5	3542-2	Fairchild
				OC	5	2115-4	Intel
						see page 766, 769	
				TS	5	2125-4	Intel
						see page 766, 769	
			135 nsF	TS	-3,5,5,15	1217A	EMM/Semi
			150 nsF	TS	5	3542	Fairchild
				TS	5	SY21H02-1	Synertek
				TS	5	SYMC21H02-1	Synertek †
			160 nsF	TS	-3,5,5,15	1217	EMM/Semi

Words	Bits/Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source
Static (cont)							
1024	1	NMOS	175 nsF	TS	5	SY21H02	Synertek
			200 nsF	TS	5	SY21H02-2	Synertek
				TS	5	SYMC21H02-2	Synertek †
			250 nsF	TS	5	91L02D	AMD
				TS	5	2102F2	Fairchild
				TS	5	2102A-2	Intel
				TS	5	21F02-2	Signetics
			275 nsF	TS	5	MK4102-6	Mostek
				TS	5	SY2102-6	Synertek
			300 nsF	TS	5	91L02C	AMD
				TS	5	91L02CM	† AMD
				TS	5	9102C	AMD
				TS	5	9102CM	† AMD
			350 nsF	TS	5	2102F	Fairchild
				TS	5	2102LF	Fairchild
				TS	5	HM7202C-5	Harris
				TS	5	2102A	Intel
				TS	5	21F02	Signetics
				TS	5	SY2102A	Synertek
				TS	5	SYMC2102A	† Synertek
			400 nsF	TS	5	91L02B	AMD
				TS	5	9102B	AMD
				TS	5	91L02BM	† AMD
				TS	5	9102BM	† AMD
				TS	5	HM7202C-2	† Harris
				TS	5	21L02-3	Signetics
				TS	5	SY21L02B	Synertek
				TS	5	SYMC21L02B	† Synertek
			450 nsF	TS	5	2102-1	Fairchild
				TS	5	2102L1	Fairchild
				TS	5	2102A-4	Intel
				TS	5	M2102A-4	† Intel
				TS	5	MK4102-1	Mostek
				TS	5	21F02-4	Signetics
				TS	5	M2102-4	† Signetics
				TS	5	TMS4033	TI
			500 nsF	TS	5	2102-1	AMD
				TS	5	9102A	AMD
				TS	5	9102AM	† AMD
				TS	5	91L02A	AMD
				TS	5	91L02AM	† AMD
				TS	5	MM7202B-2	† Harris
				TS	5	MM7202B-5	Harris
				TS	5	2102-1	Intel
				TS	5	IM7552-1C	Intersil
				TS	5	MM2102-1	National
				TS	5	M330	SGS
				TS	5	21L02-1	Signetics
				TS	5	2102-1	Signetics
				TS	5	2602-1	Signetics
						see page 790	
				TS	5	SY21L02-1	Synertek
				TS	5	SYMC21L02-1	Synertek †
			650 nsF	TS	5	2102-2	AMD
				TS	5	91L02	AMD

† Military Temperature Range (-55°C to 125°C)

ns—Nanoseconds Typical

nsF—Nanoseconds over Full Temperature Range

nsR—Nanoseconds at Room Temperature

OC—Open Collector

TS—Three-State

OE—Open Emitter

IC UPDATE MASTER

MEMORY—RAMs (cont)

Words	Bits/ Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source	Words	Bits/ Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source												
Static (cont)								Static (cont)																			
1024	1	NMOS	650 nsF	TS	5	2102	Fairchild	1024	1		65 nsF	TS	5	S82S11	† Signetics												
						21022C	Fairchild							93415C	AMD												
						2102L2	Fairchild							93415C	Fairchild												
						HM7202A-2	† Harris							93425C	Fairchild												
						HM7202A-5	Harris							HM2510	Hitachi												
						2102-2	Intel							IM55S08C	Intersil												
						M2102A-6	† Intel							IM55S18C	Intersil												
						IM7552-2C	Intersil							93415M	† AMD												
						MM2102-2	National							93415M	† Fairchild												
						M330B	SGS							93425M	† Fairchild												
						21L02-2	Signetics							IM55S08M	† Intersil												
						2102-2	Signetics							IM55S18M	† Intersil												
						2602-2	Signetics																				
						see page 790																					
						M2102-6	† Signetics																				
						TMS4034	TI																				
															650 nsR	TS	5	IM7552-2M	Intersil								
															1 μsF	TS	5	2102	AMD								
																TS	5	HM7202-2	† Harris								
																TS	5	HM7202-5	Harris								
																TS	5	2102	Intel								
																TS	5	IM7552C	Intersil								
																TS	5	MK4102	Mostek								
																TS	5	MM2102	National								
																TS	5	M330A	SGS								
				TS	5	21L02	Signetics																				
				TS	5	2102	Signetics																				
				TS	5	2602	Signetics																				
						see page 790																					
				TS	5	SY2102	Synertek																				
				TS	5	SY21L02	Synertek																				
				TS	5	TMS4035	TI																				
			1 μsR	TS	5	IM7552M	† Intersil																				
			1.5 μsF	TS	5	2102-8	Intel																				
TTL			30 ns*	OC	5	SN54S314	† TI																				
				OC	5	SN74S314	TI																				
				TS	5	SN54S314	† TI																				
				TS	5	SN74S314	TI																				
			35 ns*	OC																							
TTL			35 ns*	OC	5	RM5500	† Raytheon																				
				OC	5	RC5500	Raytheon																				
				OC	5	N82S110	Signetics																				
				TS	5	N82S111	Signetics																				
			45 nsF	OC	5	93415A	AMD																				
				OC	5	93415AC	Fairchild																				
				TS	5	93425AC	Fairchild																				
				OC	5	N82S10	Signetics																				
				TS	5	see page 804, 806, 818,																					
				TS	5	N82S11	Signetics																				
						see page 804, 806, 818,																					
				OC	5	N93415A	Signetics																				
				TS	5	see page 804, 806, 819,																					
				OC	5	N93425A	Signetics																				
				TS	5	see page 804, 806, 819,																					
			65 nsF	OC	5	S82S10	† Signetics																				
						see page 804, 806, 818,																					

† Military Temperature Range (−55°C to 125°C)

ns*—Nanoseconds Typical

nsF—Nanoseconds over Full Temperature Range

nsR—Nanoseconds at Room Temperature

OC—Open Collector

TS—Three-State

OE—Open Emitter

MEMORY—ROMs

Words	Bits/Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source	Words	Bits/Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source			
Dynamic								Static (cont)										
256	10	PMOS	550 nsF		-12,5	TMS2300	TI	256	4	PMOS	950 nsR		-12,5	MM4211	† National			
			800 nsR		-12,5	CRC3501	Collins						-12,5	MM4221	† National			
512	5	PMOS	800 nsR		-12,5	CRC3501	Collins						-12,5	MM5211	National			
	10	PMOS	450 nsF	TS	-12,5	S8771	AMI			TTL	40 nsR	OC		MCM4006A	Motorola			
						see page 706					45 nsF	OC	5	93457C	Fairchild			
1024	5	PMOS	500 nsF	TS	-12,5	TMS4200	TI					TS	5	93467C	Fairchild			
					±5	MCS2023	MOS				45 nsF	OC	5	H6200	MMI			
	12	PMOS	3.6 μsF		-12,-24	EA3800	EA					TS	5	H6201	MMI			
												OC	5	3301A	Intel			
2048	4	PMOS	1.3 μsF	TS	-12,5	S8865	AMI				50 nsF	OC	5	93406C	Fairchild			
			1.6 μsF		-12,5	RO5-8192	GI					OC	5	N82S226/229	Signetics			
						see page 706						TS	5	see page 822				
	8	NMOS	250 nsF	OC	12	MK29000	Mostek				50 nsR	OC	5	5200	† MMI			
						see page 783						OC	5	6200	MMI			
		PMOS	450 nsF		-12,5	MCS2026	MOS					OC	5	MCM4004A	Motorola			
			1.8 μsF	TS	-12,5	S9996	AMI				60 nsF	OC	5	93457M	† Fairchild			
						see page 706						TS	5	93467M	† Fairchild			
4096	4	NMOS	250 nsF	OC	12	MK29000	Mostek						5	M3301A	† Intel			
						see page 783						OC	5	H5200	† MMI			
		PMOS	1.8 μsF	TS	-12,5	S8996	AMI					TS	5	H5201	† MMI			
						see page 706					60 nsR	OC	5	DM54187	† National			
Static													OC	5	DM74187	National		
32	8	TTL	45 nsR	OC	5	SN5488A	† TI					TS	5	DM7597	† National			
				OC	5	SN7488A	TI					TS	5	DM8597	National			
			50 nsR	OC	5	93434C	Fairchild					OC	5	SN54187	† TI			
				OC	5	93434M	† Fairchild					OC	5	SN74187	TI			
				OC	5	6230	MMI				75 nsF	OC	5	S82S226/229	† Signetics			
				TS	5	6231	MMI					TS	5	see page 822				
				OC	5	5230	† MMI				90 nsF	OC	5	M3301A	† Intel			
				TS	5	5231	† MMI				130 nsR	TS	5	DM76L97	† National			
				OC	5	MCM4002L	† Motorola					TS	5	DM86L97	National			
				OC	5	MCM4002P	Motorola				5	TTL	60 nsR	OC	5	6210	MMI	
				OC	5	DM5488	† National						75 nsR	OC	5	5210	† MMI	
				OC	5	DM7488	National				8	PMOS	750 nsR		±12	MM4230	† National	
				TS	5	DM7598	† National								±12	MM5230	National	
				TS	5	DM8598	National								-12,-24	NCM1110	Nitron	
64	8	TTL	75 nsR		5	MCM4003A	Motorola							-12,5	MM4213	† National		
					5	MCM4303A	† Motorola							-12,5	MM5213	National		
			650 nsR		±12	MM4220	† National							-12,5	MM4231	† National		
					±12	MM5220	National							-12,5	MM5231	National		
			950 nsR		-12,5	MM4221	† National							-12,5	MM4231	† National		
					-12,5	MM5221	National							-12,5	MM5231	National		
128	8	PMOS	4 μsR		-27,-12	CRC3001	Collins							1 μsF	TS	-9,5	1302	Intel
					-13,-27	MM3501	National							1.5 μsR		±12	CRC3002	Collins
256	4	CMOS	1.8 μsR		3-15	MCM14524A	† Motorola							TS	-12,5	RO5-1302	GI	
					3-15	MCM14524C	Motorola											
		PMOS	650 nsR		±12	MM4210	† National											
					±12	MM4220	† National											
					±12	MM5210	National											
					±12	MM5220	National											
						N82S214	Signetics											
						see page 823												
						6235	MMI											
						70 nsF	OC	5										
						SN74S271	TI											

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Master Selection Guide

MEMORY

† Military Temperature Range (-55°C to 125°C)
OC—Open Collector

ns*—Nanoseconds Typical

nsF—Nanoseconds over Full Temperature Range
TS—Three-State

nsR—Nanoseconds at Room Temperature
OE—Open Emitter

MEMORY—ROMs (cont)

Words	Bits/ Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source
Static (cont)							
256	8	TTL	70 nsF	TS		SN74S371	TI
			75 nsR	OC	5	5235	† MMI
			90 nsF	TS	5	S82S214 see page 823	† Signetics
			95 nsF	OC	5	SN54S271	† TI
				TS	5	SN54S371	† TI
	180 nsR	OC	5	DM54L187A	† National		
		OC	5	DM74L187A	National		
	10	PMOS	600 nsF	TS	-12,5	MK2400	Mostek
			800 nsR		-12,-24	NCM1150	Nitron
	12	PMOS	1.4 μsF		-12,5	MM4229	† National
						MM5229	National
320	7	PMOS	700 nsR		-14,-28	MK2000	Mostek
			1 μsF		-12,5	MK2300	Mostek
384	8	PMOS	900 nsR	TS	-12,5	MM4241	† National
						MM5251	National
512	4	PMOS	725 nsR		±12	MM5230	National
						±12	MM4230
			800 nsR		-12,-24	NCM110	Nitron
				850 nsR	TS	-12,5	MM4213
			TS		-12,5	MM5213	National
	950 nsR		-12,5	MM4231	† National		
			-12,5	MM5231	National		
	1.5 μsR		±12	CRC3002	Collins		
	TTL	50 nsF	OC	5	5	93431C	Fairchild
					5	93441C	Fairchild
5					N82S230/231 see page 824	Signetics	
5							
5							
60 nsF	OC	5	5	5	93431M	† Fairchild	
				5	93441M	† Fairchild	
60 nsR	OC	5	5	5	6205	MMI	
				5	6206	MMI	
70 nsF	OC	5	5	5	3302	Intel	
				5	3322	Intel	
				5	S82S230/231 see page 824	† Signetics	
				5	SN74S270	TI	
				5	SN74S370	TI	
90 nsF	OC	5	5	5	3302-4	Intel	
				5	3322-4	Intel	
90 nsR	OC	5	5	5	5205	† MMI	
				5	5206	† MMI	
95 nsF	OC	5	5	5	SN54S270	† TI	
				5	SN54S370	† TI	
120 nsF	OC	5	5	5	3302L-6	Intel	
				5	3322L-6	Intel	
5	5	450 nsF	TS	5	RO3-2560	EMM/Semi	

Words	Bits/ Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source	
Static (cont)								
512	5	NMOS	450 nsF	TS	5	RO3-2560	GI	
			PMOS	500 nsR		±12	MM4240	† National
							MM5240	National
			800 nsR		-12,-24	NCM1150	Nitron	
				TTL	75 nsR	OC	5	6225
	100 nsR	OC	5		5225	† MMI		
	8	NMOS	500 nsF	TS	5	9214C	AMD	
					5	9214M	† AMD	
				TS	5	RO3-4096	EMM/Semi	
					5	RO3-4096	GI	
5				SY3514	Synertek			
5	SY5232	Synertek						
PMOS	600 nsF	TS		-12,5	3515	Fairchild		
				-12,5	ITT3514-1	ITT		
				700 nsF				
					-12,5	MK2500	Mostek	
					-12,5	MK2600	Mostek	
		-12,5	2530	Signetics				
800 nsR				-12,-28	NCM1140	Nitron		
				1 μsF	-12,5	S3514 see page 706	AMI	
					-12,5	S5232 see page 706	AMI	
				1 μsR	-12,5	ITT3514-2	ITT	
					-12,5	MM4214	† National	
		-12,5	MM4232	† National				
		-12,5	MM5214	National				
		-12,5	MM5232	National				
		-12,5	MM5233	National				
TTL	55 nsF	OC	5	5	93432C	Fairchild		
				5	93442C	Fairchild		
60 nsF	TS	5	N82S215 see page 823	Signetics				
70 nsF	OC	5	5	5	93432M	† Fairchild		
				5	93442M	† Fairchild		
				5	3304A	Intel		
				5	3324A	Intel		
75 nsR	OC	5	5	5	H6240	MMI		
				5	H6241	MMI		
90 nsF	TS	5	5	5	3304A-4	Intel		
				5	3324A-4	Intel		
				5	S82S215 see page 823	† Signetics		
90 nsR	OC	5	5	5	H5240	† MMI		
				5	H5241	MMI		
120 nsF	OC	5	3304AL-6	Intel				
150 nsF	OC	5	5	5	AM27S40	AMD		
				5	AM27S41	AMD		
150 nsR	OC	5	DM7595	† National				

† Military Temperature Range (-55°C to 125°C)
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TS—Three-State

nsR—Nanoseconds at Room Temperature
OE—Open Emitter

MEMORY—ROMs (cont)

Bits/ Words	Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source				
Static (cont)											
8	TTL	150 nsR	TS	5	5	DM7596	† National				
						DM7795	† National				
						DM7796	† National				
						DM8595	National				
						DM8596	National				
						DM8795	National				
						DM8796	National				
						175 nsR	OC	5	A5240	† MMI	
						TS	5	A5241	† MMI		
						OC	5	A6240	MMI		
TS	5	A6241	MMI								
180 nsF	OC	5	5	AM27S40M	† AMD						
				AM27S41M	† AMD						
10	NMOS	500 nsF	TS	5	5	RO3-5120	EMM/Semi				
						RO3-5120	GI				
PMOS	725 nsF	±12				EA4000	EA				
1024	4	700 nsF	TS	-12,5	-12,5	MK2500	Mostek				
						TS	-12,5	MK2600	Mostek		
			800 nsF		-14,-28				NCM1140	Nitron	
			1 μsR	TS	-12,5	-12,5	-12,5	-12,5	S5232	AMI	
									see page 706		
									MM4232	† National	
			MM5232	TS	-12,5				MM5232	National	
			TTL	75 nsF	5				N8228	Signetics	
8	NMOS	290 nsF	±5,12			NCM6560A	Nitron				
						350 nsF	TS				
						5	TS	-3,5,12	-3,5,12	EA4700	EA
										MCM6560	Motorola
										NCM6560	Nitron
						400 nsF	TS	5	5	EA2308A	EA
										EA4700-1	EA
										EA8308A	EA
						450 nsF	TS	5,12	±5,12	9208C	AMD
										TMS4700	TI
500 nsF	TS	5	±5,12	EA2308AM	† EA						
				2308	Intel						
				MCM6830A	Motorola						
550 nsF	TS	5				EA4700M	† EA				
575 nsF	TS	5	5	S6830	AMI						
				see page 887							
MCM6830	Motorola										
600 nsF	TS	5,12				9208M	† AMD				
650 nsF	TS	5	5			2608	Signetics				
						see page 801					
TTL	60 ns*	OC	5	5	5	93454C	Fairchild				
						93464C	Fairchild				

Bits/ Words	Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source								
Static (cont)															
1024	8	TTL	60 ns*	OC	5	93454M	† Fairchild								
						93464M	† Fairchild								
						125 nsF	OC	5	N82S280	Signetics					
									N82S281	Signetics					
						150 nsF	OC	5	AM27S80	AMD					
									AM27S81	AMD					
									6280	MMI					
									6281	MMI					
						175 nsR	OC					5280	† MMI		
												5281	† MMI		
180 nsF	OC	5	5	AM27S80M	† AMD										
				AM27S81M	† AMD										
9	TTL	150 nsR	OC	5	5	5260	† MMI								
						6260	MMI								
10	TTL	120 nsR	OC	5		5255	† MMI								
						6255	MMI								
12	CMOS	250 nsR	TS	4-11	4-11	HM6312A-2	† Harris								
						HM6312A-9	Harris								
			500 nsR	TS	5	5	HM6312-2	† Harris							
							HM6312-9	Harris							
PMOS	3 μsR	±12				MM5215	National								
						5 μsR	-12,5	MM5212	National						
2048	4	290 nsF	±5,12			NCM6560A	Nitron								
						350 nsF	TS	-3,5,12	-3,5,12	MCM6560	Motorola				
										NCM6560	Nitron				
						PMOS	450 nsF	TS	-12,5			RO1492C	Western		
												950 nsR	-12,5	2580	Signetics
						8	NMOS	450 nsF	TS	5,12	5,12	9216C	AMD		
												RO3-8316B	EMM/Semi		
								475 nsF		±5,12				NCM6590A	Nitron
								500 nsF	TS	5				S6831	AMI
														see page 706	
550 nsF	TS	5	±5,12	±5,12	±5,12			EA4600C	EA						
								MCM6832	Motorola						
								NCM6832	Nitron						
550 nsF	TS	5,12						RO3-8316B	GI						
600 nsF	TS	5						MK31000	Mostek						
600 nsF	TS	5,12				9216M	† AMD								
750 nsF	TS	5				EA4600M	† EA								
800 nsF	TS	-3,5,12	-3,5,12			MCM6590	Motorola								
						NCM6590	Nitron								
850 nsF	TS	5				RO3-8316A	EMM/Semi								
						see page 745									
RO3-8316A	GI														

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MEMORY

† Military Temperature Range (-55°C to 125°C)
OC—Open Collector

ns*—Nanoseconds Typical

nsF—Nanoseconds over Full Temperature Range
TS—Three-State

nsR—Nanoseconds at Room Temperature
OE—Open Emitter

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MEMORY—ROMs (cont)

Words	Bits/ Word	Type	Access Time (Max.)	Output	Supply Voltage	Device	Source				
Static (cont)											
10	2048	8	NMOS	850 nsF	TS	5	2316A	Intel			
				600 nsF		-12,5	MK28000	Mostek			
										see page 783	
				700 nsF		-12,5	TMS4800	TI			
				950 nsF		-12,5	EA4900C	EA			
				1.35 μsF		-12,5	EA4900L	EA			
		TTL	110 nsF	OC	5	6275	MMI				
				TS	5	6276	MMI				
			120 nsF	OC	5	5275	† MMI				
				TS	5	5276	† MMI				
4096	4	NMOS	550 nsF	TS	5	EA4600C	EA				
			750 nsF	TS	5	EA4600M	† EA				
			1 μsF	TS	5	RO3-16384	EMM/Semi				
				TS	5	RO3-16384	GI				
			600 nsF		-12,5	MK28000	Mostek				
								see page 783			
		700 nsF		±12,5	TMS4800	TI					
		950 nsF		-12,5	EA4900	EA					

Master Selection Guide

MEMORY

† Military Temperature Range (-55°C to 125°C)
OC—Open Collector

ns*—Nanoseconds Typical

nsF—Nanoseconds over Full Temperature Range
TS—Three-State

nsR—Nanoseconds at Room Temperature
OE—Open Emitter

MEMORY—Shift Registers

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source
Dynamic							
For analog memories, see Linear - Other Devices							
16	4	SS	PMOS	1.0 M	-12,5	CRC1504	Collins
				3.0 M	-28	EA1208	EA
32	4	SS	PMOS	1.0 M	-12,5 -12,5 -28	CRC1502 CRC1503 EA1201	Collins Collins EA
				3.0 M	-28	EA1200	EA
64	1	SS	PMOS	1.0 M	-14,-28	EA1203	EA
Elect. Variable				3.0 M	-14,-28	EA1202	EA
	2	SS	PMOS	0.1 M	-14 -14,-9	HD3213P HS3214P	Hitachi Hitachi
				2.5 M	-12,5 -12,5 -12,5 -12,5 -12,5	MM4001AH MM4010AH MM5001AH MM5010AH MM5011A	† National † National National National National
	3	SS	PMOS	0.1 M	-14	HD3214P	Hitachi
				2.5 M	-12,5 -12,5 -12,5	MM4015 MM4018 MM5015	† National † National National
	4	SS	PMOS	3.0 M	-12,5	MP3417	Plessey
				5.0 M	-12,5 ±5	TMS3417 HD3508	TI Hitachi
66	3	SS	PMOS	1.0 M	-14	CRC1505	Collins
				2.0 M	-24,-14	MTS1016	MOS
72	3	SS	PMOS	5.0 M	±5 ±5	HD3523 HD3524	Hitachi Hitachi
80	4	SS	PMOS	2.5 M	-12,5 -12,5	IM7780C MK1007	Intersil Mostek
				3.0 M	-12,5	MP3409	Plessey
				5.0 M	-12,5	TMS3409	TI
100	2	SS	PMOS	1.0 M	±5 ±5	HD3506 HD3507	Hitachi Hitachi
				2.0 M	-10 ±5 ±5 ±5 ±5 ±5 ±5 ±5	MTS1001 1406 1407 1506 1507 1406 1407 1506 1507	MOS † AMD † AMD AMD AMD † Intel † Intel Intel Intel
				2.5 M	-12,5 -12,5 -12,5 -12,5	MM4006 MM4007 MM5006 MM5007D	† National † National National National
				3.0 M	±5 ±5 ±5 ±5	MTS2013 2506 2507 2517	MOS Signetics Signetics Signetics

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source
Dynamic (cont)							
128	2	SS	PMOS	5.0 M	±5	HD3509	Hitachi
200	1	SS	CMOS	5.0 M	3-15	CD4062A	† RCA
						see page 375	
			pmos	1.0 M	-28	EA1221	EA
213	2	SS	PMOS	4.0 M	-6,5 -6,5	S1015A S1015B	† Siliconix Siliconix
256	1	SS	PMOS	1.0 M	-28	EA1205	EA
				2.0 M	-12,5	3383	Fairchild
				2.5 M	±5	HD3510	Hitachi
				3.0 M	-14	EA1204	EA
	2	SS	PMOS	2.5 M	-12,5 -12,5	MM4019 MM5019	† National National
				3.0 M	-14	EA1210	EA
	4	SS	PMOS	2.5 M	±5 ±5	SY1402B SY1402BR	Synertek Synertek
				5.0 M	±5 ±5 ±5 ±5 ±5 ±5 ±5 ±5	1402AC 1402AM HD3502 1402A MM1402A 1402 1402A M141 SY1402A SY1402AR	AMD † AMD Hitachi Intel National Nortec Nortec SGS Synertek Synertek
				8.0 M	±5	2502	Signetics
				10.0 M	±5 ±5 ±5	AM2802C AM2802M SY2802	AMD † AMD Synertek
64	SS	CCD		1.0 M	-5,12	2416	Intel
360	1	SS	PMOS	2.5 M	-12,5 -12,5	MM4104H MM5104H	† National National
480	2	SS	PMOS	1.0 M	-12,5	S1685	AMI
				5.0 M	-12,5	TMS3402	TI
512	1	SS	PMOS	2.0 M	±5	1405A	Intel
				2.5 M	±5 -12,5 -12,5	2505 MM4016 MM5016	Signetics † National National
				3.0 M	±5 ±5 ±5 ±5 -14	AM2805M AM2807M 2524 EA1212	† AMD † AMD Signetics EA
				4.0 M	±5 ±5	AM2805C AM2807C	AMD AMD
				5.0 M	±5 ±5 -12,5 -27	HD3505 MTS2100 TMS3401 EA1206	Hitachi MOS TI EA
	2	SS	PMOS	2.5 M	-12,5 -12,5 ±5 ±5	MM4017 MM5017 SY1403B SY1403BR	† National National Synertek Synertek

Military Temperature Range (-55°C to 125°C) * — Typical Values SS = Serial In, Serial Out PP = Parallel In, Parallel Out

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MEMORY—Shift Registers (cont)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source					
Dynamic (cont)												
512	2	SS	PMOS	5.0 M	±5	1403AC	AMD					
					±5	1403AM	† AMD					
					±5	HD3503	Hitachi					
					±5	1403A	Intel					
					±5	MM1403A	National					
					±5	1403A	Nortec					
					±5	M136	SGS					
					±5	SY1403A	Synertek					
					±5	SY1403AR	Synertek					
					±5	2503	Signetics					
1024	1	SS	NMOS	1.0 M	5	2405	Intel					
					5	SY2405	Synertek					
					5							
1024	1	SS	PMOS	2.5 M	±5	2512	Signetics					
					-12,5	MM4013	† National					
					-12,5	MM5013	National					
					±5	2525	Signetics					
					±5	SY1404B	Synertek					
					±5	SY1404BR	Synertek					
					±5	AM2806M	† AMD					
					±5	AM2808M	† AMD					
					±5	IM7712	Intersil					
					±5	IM7722	Intersil					
±5	2512	Nortec										
1024	1	SS	PMOS	4.0 M	±5	AM2806C	AMD					
					±5	AM2808M	AMD					
					±5	2512	Nortec					
					±5	1404AC	AMD					
					±5	1404AM	† AMD					
					±5	HD3504	Hitachi					
					±5	1404A	Intel					
					±5	MM1404A	National					
					±5	MM5024A	National					
					±5	1404A	Nortec					
5	SY1404A	Synertek										
5	SY1404AR	Synertek										
1024	1	SS	PMOS	8.0 M	±5	2504	Signetics					
					±5	M130	SGS					
					±5	AM2804C	AMD					
					±5	AM2804M	† AMD					
					±5	SY2804	Synertek					
					1024	2	SS	NMOS	1.0 M	5	AM2401	AMD
										5	2401	Intel
										5	SY2401	Synertek
										5	9401C	AMD
										5	9401M	† AMD
5	SY2401-1	Synertek										
1024	1	SS	PMOS	1.0 M						-12,5	MM4025	† National
										-12,5	MM4026	† National
										-12,5	MM5025	National
										-12,5	MM5026	National
					-12,5	SY5025	Synertek					
					-12,5	SY5026	Synertek					

† Military Temperature Range (-55°C to 125°C) SS = Serial In, Serial Out PP = Parallel In, Parallel Out

Bold face indicates additional data is provided on the page noted.

MEMORY—Shift Registers (cont)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source
Static (cont)							
4 (continued)	1	PP	Bipolar	25 M	5	54178	† Fairchild
					5	54179	† Fairchild
					5	54194	† Fairchild
					5	74178	Fairchild
					5	74179	Fairchild
					5	74194	Fairchild
					5	ITT5495	† ITT
					5	ITT54194	† ITT
					5	ITT7495	ITT
					5	ITT74194	ITT
					5	54194	† Raytheon
					5	74194	Raytheon
					5	S5495	† Signetics
					5	N7495	Signetics
					5	N74194	Signetics
					5	S54194	† Signetics
					5	SN5495A	† TI
					5	SN54178	† TI
					5	SN54179	† TI
					5	SN54194	TI
					5	SN7495A	TI
					5	SN74178	TI
					5	SN74179	TI
					5	SN74194	TI
				30 M	5	SN54195	† AMD
					5	SN74195	AMD
					5	54LS95	† Fairchild
					5	74LS95	Fairchild
					5	5495	† Fairchild
					5	7495	Fairchild
					5	54LS194	Fairchild
					5	74LS194	Fairchild
					5	54LS195	† Fairchild
					5	74LS195	Fairchild
					5	54LS295	† Fairchild
					5	74LS295	Fairchild
					5	ITT54195	† ITT
					5	ITT74195	ITT
					5	MC54195	† Motorola
					5	MC74195	Motorola
					5	DM8300	National
					5	DM9300	† National
					5	54195	† Raytheon
					5	74195	Raytheon
					5	N74195	Signetics
					5	S54195	† Signetics
					5	SN54195	† TI
					5	SN74195	TI
				31 M	5	MC5495	† Motorola
					5	MC7495	Motorola
				35 M	5	MC4012	Motorola
				38 M	5	9300C	Fairchild
					5	9300M	† Fairchild
				55 M	5	93H00C	† Fairchild
					5	93H00M	† Fairchild

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source
Static (cont)							
4	1	PP	Bipolar	60 M	5	93H72C	Fairchild
					5	93H72M	† Fairchild
					5	N82S70	Signetics
					5	N82S71	† Signetics
				70 M	5	SN54S194	† AMD
					5	SN54S195	† AMD
					5	SN74S194	AMD
					5	SN74S195	AMD
					5	93S00C	Fairchild
					5	93S00M	† Fairchild
					5	93S194C	Fairchild
					5	93S194M	† Fairchild
					5	SN54S194	† TI
					5	SN54S195	† TI
					5	SN74S194	TI
					5	SN74S195	TI
				75 M	5	S54S194	Signetics
					5	N74S194	Signetics
				150 M	-4.5	F10000	Fairchild
					-5.2	MC10141	Motorola
					-5.2	10141	Signetics
					-5.2	SN10141	TI
				190 M	-5.2	95H00C	Fairchild
				250 M	-5.2	F10141	Fairchild
		PS	Bipolar	1 M	11	MC794P	Motorola
				10 M	5	5494	† Fairchild
					5	7494	Fairchild
					5	ITT5494	† ITT
					5	ITT7494	ITT
					5	MC5494	† Motorola
					5	MC7494	Motorola
					5	N7494	Signetics
					5	S5494	Signetics
					5	SW7494	SW
					5	SN5494	† TI
					5	SN7494	TI
		SP		325 M	-5.2	MC1694L	† Motorola
		SS		0.5 M	15	MC686	Motorola
		PP	CMOS	2 M	3-15	34035M	† Fairchild
					3-15	340194M	† Fairchild
					3-15	340195M	† Fairchild
					3-15	HD4035A-9	† Harris
						see page 266	
					3-15	MC14035C	Motorola
					3-15	CD4035AE	RCA
						see page 375	
					3-15	SCL4035	SSS
					3-15	CM4035AE	Soliton
					3-15	TC4035	Toshiba
				3 M	3-15	34035C	Fairchild
					3-15	340194C	Fairchild
					3-15	340195C	Fairchild
					3-15	HD4035A-2	Harris
						see page 266	
					3-15	MC14035A	† Motorola
						(continued)	

† Military Temperature Range (-55°C to 125°C) SS = Serial In, Serial Out PP = Parallel In, Parallel Out

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MEMORY—Shift Registers (cont)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source
Static (cont)							
4 (continued)	1	PP	CMOS	3 M	3-15	CD4035A	† RCA
						see page 375	
						CM4035A	† Solitron
						TP4035A	TI
						CM4015AE Solitron	
						1.5 M 5 CM4015AD † Solitron	
						TP4015A TI	
						1.8 M 3-15 TF4015A † TI	
						2.5 M 3-15 34015C Fairchild	
						3-15 HD4015A-9 Harris	
	see page 266						
	3-16 MC14015C Motorola						
	3-15 CD4015C National						
	3-15 CD4015AE RCA						
	see page 375						
	3-15 TC4015 Toshiba						
	3 M 3-15 34015M † Fairchild						
	3-15 HD4015A-2 † Harris						
	see page 266						
	3-18 MC14015A † Motorola						
3-15 CD4015M † National							
3-15 CD4015A † RCA							
see page 375							
3-15 SCL4015A † SSS							
3-15 SCL4015AE SSS							
PP PMOS 1 M -12,5 SS5-2004 GI							
-12,5 SS6-2004 † GI							
5	1	PP	Bipolar	10 M	5	5496	† Fairchild
						7496	Fairchild
						ITT5496	† ITT
						ITT7496	ITT
						MC5496L	† Motorola
						MC7496P	Motorola
						DM5496	† National
						DM7496	National
						N7496	Signetics
						S5496	† Signetics
						SW5496	† SW
						SW7496	SW
						SN5496	† TI
						SN7496	TI
						7496	TRW
	2 PP Bipolar 35 M 5 HD2546 Hitachi						
	4	SS	CMOS	1.2 M	5	CM4006AE Solitron	
						1.5 M 5 CM4006AD † Solitron	
						2 M 3-15 CM4006 † Solitron	
						3-15 CM4006AE Solitron	
3-15 CD4006AE RCA							
see page 375							
2.5 M 3-15 CD4006A † RCA							
see page 375							
3 M 3-15 SCL4006A † SSS							
3-15 SCL4006A SSS							
Static (cont)							
5	4	SS	CMOS	4 M	5-15	MC14006C	Motorola
						7 M 5-15 MC14006A † Motorola	
						8 1 PP Bipolar 15 M 5 DM7576 † National	
						5 DM8576 National	
						25 M 5 54198 † Fairchild	
	5 54199 † Fairchild						
	5 74198 Fairchild						
	5 74199 Fairchild						
	5 DM54198 † National						
	5 DM54199 † National						
5 DM74198 National							
5 DM74199 National							
5 54198 † Raytheon							
5 54199 † Raytheon							
5 74198 Raytheon							
5 74199 Raytheon							
5 N74198 Signetics							
5 N74199 Signetics							
5 S54198 † Signetics							
5 S54199 † Signetics							
5 SN54198 † TI							
5 SN54199 † TI							
5 SN74198 TI							
5 SN74199 † TI							
70 M 5 SN74S299 TI							
PS 14 M 5 DM7590D † National							
5 DM8590N National							
20 M 5 54165 † Fairchild							
5 74165 Fairchild							
5 54165 † Raytheon							
5 74165 Raytheon							
5 S54165 † Signetics							
5 N74165 Signetics							
5 SN54165 † TI							
5 SN74165 TI							
25 M 5 54166 † Fairchild							
5 74166 Fairchild							
5 DM54166 † National							
5 DM74166 National							
5 54166 † Raytheon							
5 74166 Raytheon							
5 S54166 † Signetics							
5 N74166 Signetics							
5 SN54166 † TI							
5 SN74166 TI							
SP 12 M 5 SN54L164 † TI							
5 SN74L164 TI							
14 M 5 MC54164A † Motorola							
5 MC74164A Motorola							
5 DM7570 † National							
5 DM8570 National							
25 M 5 54164 † Fairchild							
5 74164 Fairchild							
5 54LS164 † Fairchild							
5 74LS164 Fairchild							
5 54164 † Raytheon							
(continued)							

† Military Temperature Range (-55°C to 125°C) SS = Serial In, Serial Out PP = Parallel In, Parallel Out

Bold face indicates additional data is provided on the page noted.

MEMORY—Shift Registers (cont)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source
Static (cont)							
8 (continued)	1	SP		25 M	5	74164	Raytheon
						N74164	Signetics
					5	S54164	† Signetics
		SS		3 M	5	SN54L91	† TI
					5	SN74L91	TI
				4 M	5	DM54L91	† National
					5	DM74L91	National
				10 M	5	5491	† Fairchild
					5	7491	Fairchild
					5	HD2524	Hitachi
					5	MC5491A	† Motorola
					5	MC7491A	Motorola
					5	N7491	Signetics
					5	S5491	† Signetics
					5	SW5491A	† SW
					5	SW7491A	SW
					5	SN5491A	† TI
					5	SN7491A	TI
				15 M	5	N8276	Signetics
	PP	CMOS		2.5 M	3-18	MC14034C	Motorola
					3-15	SCL4034AE	SSS
					5	CM4034AE	Solitron
				3 M	3-18	MC14034A	Motorola
					3-15	CD4034A	† RCA see page 375
					3-15	SCL4034A	† SSS
					5	CM4034A	† Solitron
					3-15	TC4034	Toshiba
	PS			1 M	3-15	34014C	Fairchild
					3-15	34021C	Fairchild
					3-15	CM4014AD	† Solitron
				1.3 M	3-15	TP4021A	TI
				1.8 M	3-15	TF4021A	† TI
				2.5 M	3-15	HD4014A-9	Harris see page 266
					3-15	HD4021A-9	Harris see page 266
					3-15	MC14021C	Motorola
					3-15	CD4014AE	RCA see page 375
					3-15	CD4021A	† RCA see page 375
					3-15	CD4021AE	RCA see page 375
					3-15	TC4014	Toshiba
					3-15	TC4021	Toshiba
				3 M	3-15	34014M	† Fairchild
					3-15	34021M	† Fairchild
					3-15	HD4014A-2	† Harris see page 266
					3-15	HD4021A-2	† Harris see page 266
					3-15	MC14021A	† Motorola
					3-15	CD4014A	† RCA see page 375 (continued)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source
Static (cont)							
8 (continued)	1	PS		3 M	3-15	CD4021A	† RCA see page 375
					3-15		SCL4014A
					3-15	SCL4021A	† SSS
					3-15	CM4021AD	† Solitron
	2	SS	Bipolar	10 M	5	93L28C	AMD
					5	93L28M	† AMD
					5	93L28M	† Fairchild
					5	93L28C	Fairchild
					5	MC8328	Motorola
					5	MC9328	† Motorola
				15 M	5	RC8277	Raytheon
					5	RM8277	† Raytheon
					5	N8277	Signetics
				20 M	5	9328C	AMD
					5	9328M	† AMD
					5	9328C	Fairchild
					5	9328M	† Fairchild
	16	SS	MNOS	0.5 M	5	NC7031	Nitron
10	1	PP	TTL	0.5 M	5	RC8274	Raytheon
					5	RM8274	† Raytheon
					5	N8274	Signetics
					5	S8274	† Signetics
				0.5 M	5	RC8273	Raytheon
					5	RM8273	† Raytheon
					5	N8273	Signetics
					5	S8273	† Signetics
16	2	SS	PMOS	2 M	-12,5	SS5-8211	GI
					-12,5	SS5-8212	GI
					-12,5	SS6-8211	† GI
					-12,5	SS6-8212	† GI
	3	SS	PMOS	252 K		M120T1	SGS
	4	SS	PMOS	2 M	-12,5	SL5-4016	GI
	8	SS	MNOS	0.5 M	-30	NC7030	Nitron
20	1	SP	PMOS	5 K	-14,9	HD32112	Hitachi
24	4	SS	CMOS	2.5 M	5-16	MS618	† Ragen
25	4	SS	PMOS	1 M	-12,5	SL5-4025	GI
					-12,5	SL6-4025	† GI
					-12,5	MCS2104	† MOS
32	1	SS	PMOS	1 M	-12,5	SS5-1032	GI
					-12,5	SS6-1032	† GI
	2	SS	PMOS	1 M	-16,-10	MTS1002	MOS
				1.5 M	-28	EA1003	EA
					-28	EA1007	EA
				2 M	-12,5	MTS2103	† MOS
4	SS	PMOS		1 M	-12,5	SL5-4032	GI
					-12,5	SL6-4032	† GI
6	SS	PMOS		1 M	-12,5	3348	Fairchild
					-12,5	3349	Fairchild
				2 M	-12,5	2518	Signetics
					-12,5	TMS3112	TI
					-12,5	TMS3122	TI
					-12,5	TMS3123	TI

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Master Selection Guide

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† Military Temperature Range (-55°C to 125°C) SS = Serial In, Serial Out PP = Parallel In, Parallel Out

IC UPDATE MASTER

MEMORY—Shift Registers (cont)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source				
Static (cont)											
40	6	SS	PMOS	2 M	-12,5	2519	Signetics				
50	2	SS	PMOS	1 M	-12,5 -12,5	SL5-2050 SL6-2050	GI † GI				
				1.5 M	-14, 12 -12,±5	EA1013 2059	EA Signetics				
				3 M	-14, 12	EA1012	EA				
64	1	SS	CMOS	1 M	3-15	CD4031AE	RCA				
				see page 375							
				2 M	3-15	CD4031A	† RCA				
				see page 375							
				2.7 M	3-16	MC14557A	† Motorola				
5 M	3-18	MC14557C	Motorola	10 M	5-16	MS612	† Ragen				
								2	SS	CMOS	4 M
2	SS	CMOS	PMOS	-12,5	-12,5	SL5-2064 SL6-2064	GI † GI				
				1.3 M	-12,5 -12,5	SI2064A SI2064C	† Siliconix Siliconix				
				2 M	-12,5	MTS2105	† MOS				
2.5 M	-12,5	TMS3103	TI	4	SS	CMOS	4 M	3-15	F4731	Fairchild	
							PMOS	1.5 M	-12,5	3342	Fairchild
								2 M	-12,5	ITT3342	ITT
2.5 M	-12,5	TMS3121	TI								
80	2	SS	PMOS	1 M	-12,5	TMS3102	TI				
				1.5 M	-14,12	EA1009	EA				
				2.5 M	-12,5 -12,5	AM2847M TMS3102	† AMD TI				
3 M	-12,5 -14,12	AM2847C EA1008	AMD EA	4	SS	NMOS	3 M	5	M142	SGS	
							SS	PMOS	1.5 M	-12,5 -12,5	3343 2532
2 M	-12,5	3357-2 ITT3347	Fairchild ITT								
2.5 M	-12,5 -12,5	AM2847M TMS3120	† AMD TI	3.0 M	-12,5 -12,5	AM2847C ITT3357	AMD ITT				
								4.0 M	-12,5	3357-1	Fairchild
9	SS	PMOS	1.5 M	-12,5	TMS3135	TI					
96	2	SS	PMOS	2.5 M	-12,5	TMS3126	TI				
				4	SS	PMOS	2.5 M	-12,5	AM2896M	† AMD	
3.0 M	-12,5	AM2896C	AMD								
100	1	SS	PMOS	1.5 M	-14, 12	EA1005	EA				
				2.5 M	-12,5 -12,5	TMS3101 TMS3127	TI TI				

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source			
Static (cont)										
100	1	SS	PMOS	3 M	-14,12	EA1004	EA			
				2	SS	PMOS	1 M	-28,-14	MTS1102	MOS
							1.5 M	-27,-13 -12,±5	M127 2510	SGS Signetics
2 M	-12,5 -12,5	MCS2102 SL5-C2100	† MOS GI	4	SS	PMOS	2.2 M	-12,5	MM5061	National
							9	SS	PMOS	1.5 M
128	1	SS	CMOS	5 M	12	MS625	† Ragen			
				2	SS	PMOS	1 M	-12,5 -12,5 -12,5	MK1002 MK1002 SL5-2128	AMD Mostek GI
1.5 M	-12,5 -12,5 -12,5	2521 MTS2107 MM5060AA	Signetics † MOS National							
2 M	-12,5 -12,5 -12,5	AM2809M AM2810 TMS3114 3343	† AMD AMD AMD	2	SS	PMOS	2 M	-12,5 -12,5 -12,5 -12,5 -12,5 -12,5	AM2809M AM2810 TMS3114 3343 SL5-C2128 MTS2108 TMS3114	† AMD AMD AMD Fairchild GI † MOS TI
							2.5 M	-12,5 -12,5 -12,5 -15,5	AM2809C AM2814M TMS3128 UC7325	AMD † AMD TI Solitron
1.5 M	-12,5	MM5055	National	2.5 M	-12,5	AM2814 AM2855 AM4055 AM5055	AMD AMD † AMD AMD			
								9	SS	PMOS
132	2	SS	PMOS	1.5 M	-12,5 -12,5	MM5060AB 2522	National Signetics			
				2.5 M	-12,5	TMS3129	TI			
9	SS	PMOS	1.5 M	-12,5	TMS3139	TI				
							133	2	SS	PMOS
1.5 M	-12,5	MM5060AC	National							
2 M	-12,5	TMS3113	TI							
2.5 M	-12,5	TMS3130	TI							
9	SS	PMOS	1.5 M	-12,5	TMS3140	TI				
136	2	SS	PMOS	2.5 M	-12,5	TMS3131	TI			
				9	SS	PMOS	1.5 M	-12,5	TMS3141	TI
144	2	SS	PMOS	1.5 M	-12,5	MM5060AD	National			
				2 M	-12,5	3346	Fairchild			
				2.5 M	-12,5	TMS3132	TI			
9	SS	PMOS	1.5 M	-12,5	TMS3142	TI				
200	2	SS	PMOS	1.5 M	-12,±5	2511	Signetics			

† Military Temperature Range (-55°C to 125°C) SS = Serial In, Serial Out PP = Parallel In, Parallel Out

Bold face indicates additional data is provided on the page noted.

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MEMORY—Shift Registers (cont)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	
Static (cont)								
240	2	SS	PMOS	1.5 M	-12,5	2529	Signetics	
250	2	SS	PMOS	1.5 M	-12,5	2528	Signetics	
256	1	SS	PMOS	2.5 M	-15,5	UC7325	Solitron	
				1.0 M	-12,5	MM4056	† National	
	2	SS	PMOS	1.5 M	-12,5	MM5056	National	
					-12,5	2527	Signetics	
				2.5 M	-12,5	AM2856C	AMD	
					-12,5	AM4056	† AMD	
					-12,5	AM5056	AMD	
480	2		NMOS	1.5 M	5	SY2535	Synertek	
				3.0 M	5	SY2535A	Synertek	
512	1	SS	PMOS	1.0 M	-12,5	MM4057	† National	
				1.5 M	-12,5	MM5057	National	
				2.5 M	-12,5	AM2857C	AMD	
	2			NMOS		-12,5	AM4057	† AMD
						-12,5	AM5057	AMD
					1.5 M	5	SY2534	Synertek
				3.0 M	5	SY2534A	Synertek	
1024	1	SS	NMOS	1.5 M	5	SY2533	Synertek	
				2 M	5	IM7733C	Intersil	
					5	IM7733M	† Intersil	
				3.0 M	5	SY2833A	Synertek	
				4.0 M	5	SY2833B	Synertek	
				PMOS	5.0 M	5	SY2833C	Synertek
					1.5 M	-12,5	AM2533C	AMD
						-12,5	2533	Fairchild
						-12,5	MM5058	National
						-12,5	2533	Signetics
	2 M	-12,5	AM2833C	AMD				
		-12,5	AM2833M	† AMD				
		-12,5	TMS3133	TI				
	4 M	-12,5	3355C	Fairchild				

† Military Temperature Range (-55°C to 125°C) SS = Serial In, Serial Out PP = Parallel In, Parallel Out

RAMs

Part No.	Organization	Process	T _{ACC} (ns)	R/W T _{Cycle} (ns)	Operating Power (mW)	Standby Power (mW)	Supplies (V)	I/O	Clocks	Page
S2222	512 Static	{ CMOS SiGate	200	470	7.5	0.002	+10	MOS	0	706
S2222A	512 Static		400	940	7.5	0.001	+10	MOS	0	706
S1103	1024 Dynamic	P-SiGate	310	580	450	-	+16, +19	MOS/Sense A	3	707
S146	1024 Dynamic	P-SiGate	210	390	550	-	+19, +22	MOS/Sense A	3	707
S1103-1	1024 Dynamic	P-SiGate	180	360	550	-	+19, +22	MOS/Sense A	3	707
S1103X	1024 Dynamic	P-SiGate	120	270	550	-	+19, +22	MOS/Sense A	3	707
S1103A	1024 Dynamic	P-SiGate	205	580	425	2.0	+16, +19	MOS/Sense A	2	712
S1103-1	1024 Dynamic	P-SiGate	145	340	660	0.2	+19, +22	MOS/Sense A	2	712
S1103A-X	1024 Dynamic	P-SiGate	125	285	660	0.2	+19, +22	MOS/Sense A	2	712
S4006	1024 Quasi-Static	P-I ²	400	650	450	50	-12, +5	TTL	0	706
S4008	1024 Quasi-Static	P-I ²	500	900	450	50	-12, +5	TTL	0	706
S4008-9	1024 Quasi-Static	P-I ²	800	1000	450	50	-12, +5	TTL	0	706
S4021-4	4096 Dynamic	N-SiGate	200	510	360	1.8	+12, ±5	TTL	1	722
S4021-3	4096 Dynamic	N-SiGate	250	560	360	1.8	+12, ±5	TTL	1	722
S4021-2	4096 Dynamic	N-SiGate	300	600	360	1.8	+12, ±5	TTL	1	722
S4021	4086 Dynamic	N-SiGate	400	1000	360	1.8	+12, ±5	TTL	1	722
S4096-3	4096 Dynamic	N-SiGate	250	510	400	6.0	+12, ±5	TTL	2	728
S4096-2	4096 Dynamic	N-SiGate	300	600	400	6.0	+12, ±5	TTL	2	728
S4096-1	4096 Dynamic	N-SiGate	350	675	400	6.0	+12, ±5	TTL	2	728
S5101	256 x 4 Static	{ CMOS Si-Gate	650	650	50	0.001	+5	TTL	0	716
S6810	128 x 8 Static	N-SiGate	1000	1000	650	N/A	+5	TTL	0	884
S6810-1	128 x 8 Static	N-SiGate	575	575	650	N/A	+5	TTL	0	884

AMI

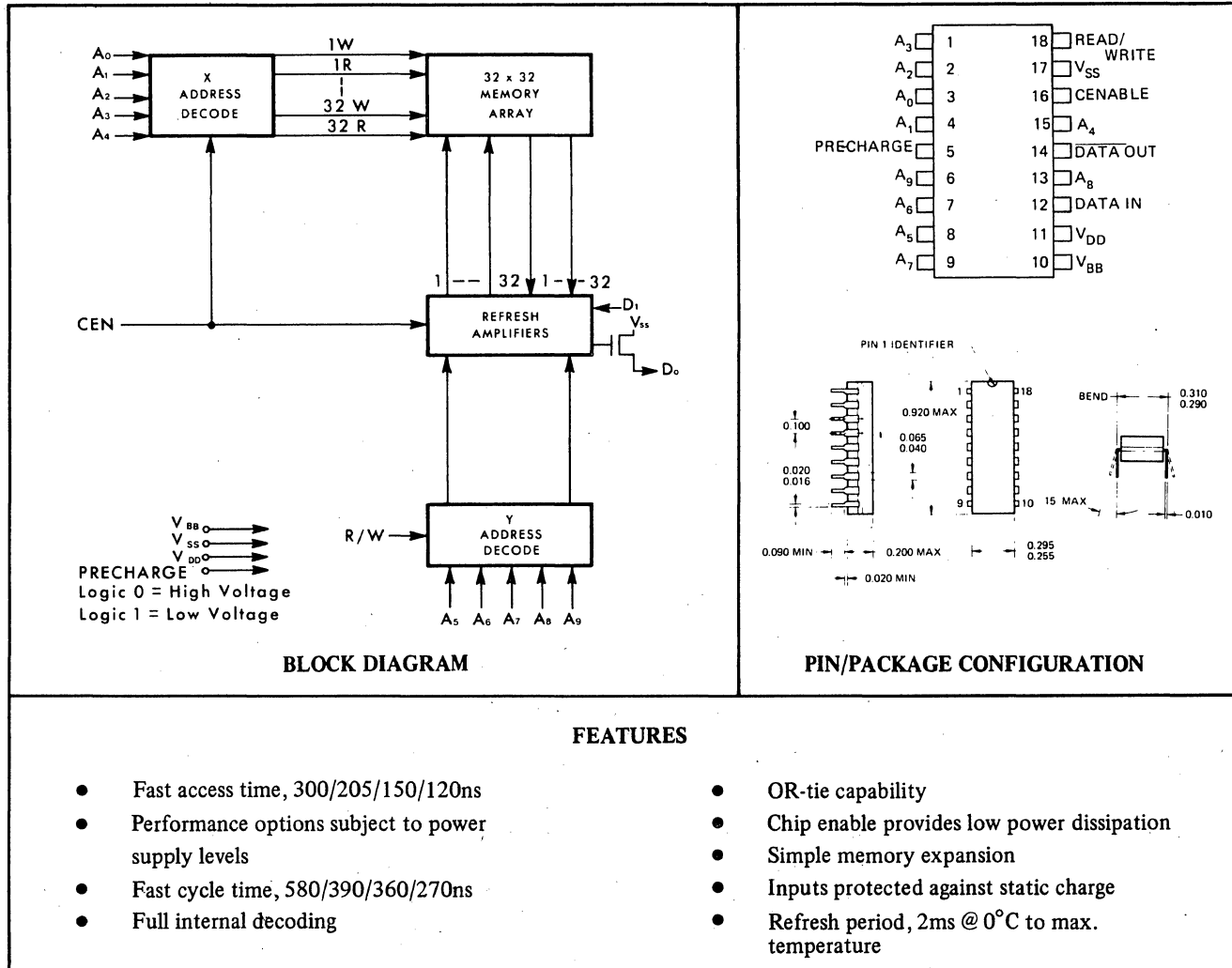
ROMs/PROMs

Part No.	Description	Organization	Max. Power Dissip. (mW)	Supplies (V)	Max. Access Time	Process	Page
S3514	4096 Bit Static ROM	512 x 8	500	+5, -12	1 μs	P-I ²	706
S5204A	2048 Bit Reprogrammable PROM	512 x 8	750	-12, +5	750 ns	P-SiGate	706
S5232	4096 Bit Static ROM	512 x 8 or 1024 x 4	500	+5, -12	1 μs	P-I ²	706
S6830	8192 Bit Static ROM	1024 x 8	650	+5	575 ns	N-SiGate	887
S6831	16,384 Bit Static ROM	2048 x 8	500	+5	500 ns	N-SiGate	706
S6834	2048 Bit Programmable PROM	512 x 8	750	-12, +5	575 ns	P-SiGate	912
S8771	5120 Bit ROM	512 x 10	1000	+5, -12	450 ns	P-I ²	706
S8865	8192 Bit ROM	2048 x 4	635	+6, -12	1.3 μs	P-I ²	706
S8996	16,384 Bit ROM	4096 x 4	368	+5, -12	1.8 μs	P-I ²	706
S9996	16,384 Bit ROM	2048 x 8	368	+5, -12	1.8 μs	P-I ²	706

MEMORY

Complete Data Sheets on all Standard Products Available from Your Local AMI Sales Office Listed Inside the Front Cover.

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FUNCTIONAL DESCRIPTION

The AMI S1103 family of random access memories are designed for applications where high performance, low cost and large bit storage are desired, such as main memories. It is a 1024 word by 1 bit array fabricated with low threshold, silicon gate technology. This high density process technology allows the design and production of extremely high performance memory devices.

The proven reliability of this process, and design, coupled with an extremely reliable plastic package, provide an exception-

al solution for many memory systems cost and performance problems. And now the Cerdip package offers the advantage of low cost in an hermetic package. The performance levels attainable are a function of the power supply levels used.

Some of the more important operational characteristics are discussed on the following page.

TYPICAL APPLICATIONS

Mainframe Memories, Cache Memories, Buffer Memories
 Minicomputer Memories, Mass Memories, Terminals.

For a complete data sheet contact your nearest AMI Sales Office

ABSOLUTE MAXIMUM RATINGS

Operating Ambient Temperature		
S1103	0° to 70°C	All Input or Output Voltages with respect to the most Positive Supply, V_{BB} -25V to 0.3V
S146/S1103-1/S1103X	0° to 55°C	
Storage Temperature	-65° to +150°C	Power Dissipation, max 425mW - S1103 660mW - S146/S1103-1/S1103X

Stresses above maximum ratings may cause permanent device damage. This is a stress rating only; functional operation of the device at any other condition above that indicated in this

specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATION

The block diagram, schematic, and timing diagram, assist in the understanding of the operation of the S1103 family. Some important characteristics relative to system design are:

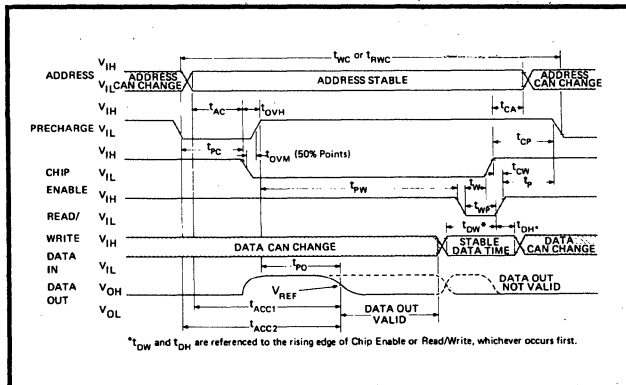
- a) Periodic refreshing is required due to dynamic operation. The device must be cycled through the 32 addresses of the A0 - A4 inputs at least every 2 ms.
- b) The memory precharge should be held positive on all but the enabled chips to reduce power dissipation. If the precharge input is negative and runs 30% duty cycle, at

minimum cycle time, the dissipation is typically 350 mW for the S1103 and 550 mW for the S146, S1103-1 or S1103X.

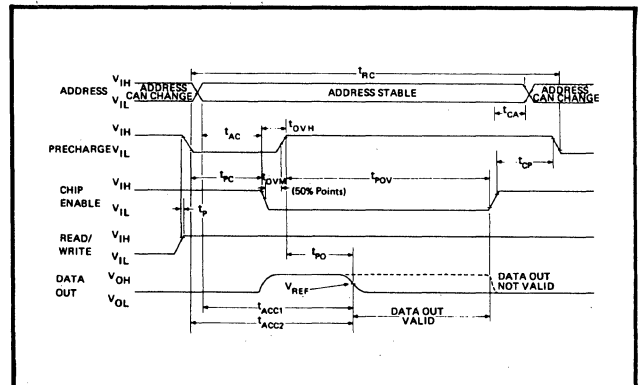
- c) Cell readout is non-destructive so the read/write cycle may be shortened for a read only or refresh only cycle, as the read/write pulse is only required for entry of new data. Thus a read only or refresh only cycle can be shorter than a read/write or a write only cycle.
- d) A high input (positive) is read as zero current out, and a low input written into the memory is read as current out.

MEMORY AMI

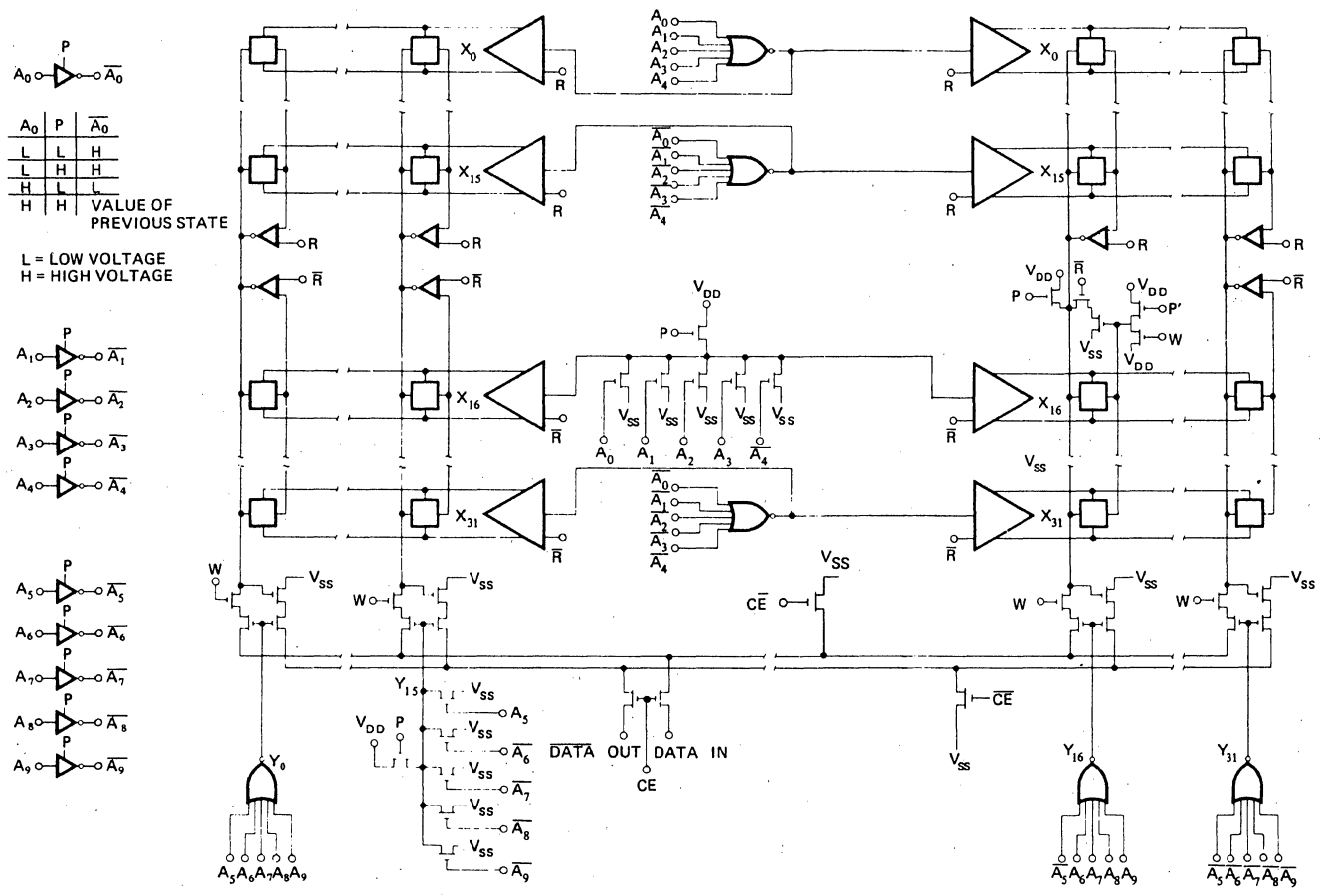
WRITE OR READ/WRITE CYCLE



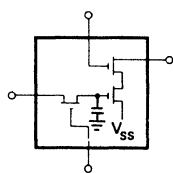
READ OR REFRESH CYCLE



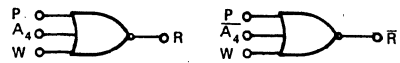
CIRCUIT DIAGRAM



BASIC MEMORY CELL



- P = PRECHARGE
- CE = CENABLE
- W = READ/WRITE
- LOGIC 0 = HIGH VOLTAGE (H)
- LOGIC 1 = LOW VOLTAGE (L)
- V_{BB} = SUBSTRATE VOLTAGE



CE	P	P'
L	L	H
L	H	H
H	L	L
H	H	L

VALUE OF PREVIOUS STATE

MEMORY AMI

OPERATING, AC AND DC CHARACTERISTICS

OPERATING CHARACTERISTICS		S1103		S146		S1103-1		S1103X		UNITS
SYMBOL	TEST DESCRIPTION									
T _A	Ambient Temperature	0 to 70		0 to 55		0 to 55		0 to 55		°C
V _{DD}	Negative Supply	0		0		0		0		V
V _{SS}	Positive Supply (1)	16 ± 0.8		19 ± 1		19 ± 1		19 ± 1		V
V _{BB} - V _{SS}	Substrate Supply (2)	3.5 ± 0.5		3.5 ± 0.5		3.5 ± 0.5		3.5 ± 0.5		V
C _L	Load Capacitance	100		100		50		50		pF
R _L	Load Resistance (3)	100		100		100		100		Ω
V _{REF}	Output Reference Voltage	40		80		80		80		mV
AC CHARACTERISTICS		S1103		S146		S1103-1		S1103X		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ, WRITE AND READ/WRITE CYCLE										
t _{REF}	Time between Refresh Cycles		2		2		2		2	ms
t _{AC}	Address to Chip Enable Setup Time	115		65		30		30		ns
t _{CA}	Chip Enable to Address Hold Time	10		10		10		10		ns
t _{PC}	Precharge to Chip Enable Delay	125		70		60		35		ns
t _{OVM}	Precharge and Chip Enable Overlap, Midpoint	45	95	25	65	25	50	13	35	ns
t _{OVH}	Precharge and Chip Enable Overlap		140		85		85		85	ns
t _{CP}	Chip Enable to Precharge Delay	85		50		40		40		ns
READ CYCLE										
t _{RC}	Read Cycle (4, 5)	480		330		300		238		ns
t _{POV}	Precharge to end of Chip Enable	165	500	130	500	115	500	114	500	ns
t _{PO}	Precharge to Output Delay		120		100		75		65	ns
t _{ACC1}	Address to Output Access (4, 6)		300		205		150		120	ns
t _{ACC2}	Precharge to Output Access (4, 7)		310		210		180		125	ns
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNITS
WRITE OR READ/WRITE CYCLE										
t _{WC}	Write Cycle (4, 8)	580		390		360		270		ns
t _{RWC}	Read/Write Cycle (4, 9)	580		390		360		270		ns
t _{PW}	Precharge to Write Delay	165	500	130	500	115	500	114	500	ns
t _{WP}	Write Pulse Width	50		40		40		20		ns
t _W	Write Setup Time	80		40		40		20		ns
t _{DW}	Data Setup Time (10)	105		40		40		25		ns
t _{DH}	Data Hold Time (11)	10		10		10		10		ns
t _{PO}	Precharge to Output Delay		120		100		75		65	ns
t _P	Time to Next Precharge	70		35		25		25		ns
t _{CW}	Chip Enable to Write		15		15		15		16	ns

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AC CHARACTERISTICS (Cont'd)

		TYP.	MAX.	UNITS	CONDITIONS		
CAPACITANCE (12)							
C _{AD}	Address	5	7	pF	V _{IN} = V _{SS}	All Unused Pins @ AC GND f ₀ = 1 MHz; V _{BB} = 3.0V	
C _{PR}	Precharge	15	18	pF	V _{IN} = V _{SS}		
C _{CE}	Chip Enable	15	18	pF	V _{IN} = V _{SS}		
C _{RW}	Read/Write	12	15	pF	V _{IN} = V _{SS}		
C _{IN1}	Data Input	5	7	pF	Enable = V _{DD} , V _{IN} = V _{SS}		
C _{IN2}	Data Input	3	5	pF	Enable = V _{SS} , V _{IN} = V _{SS}		
C _{OUT}	Data Output	3	4	pF	V _{IN} = V _{SS} V _{OUT} = V _{DD}		
DC CHARACTERISTICS		S1103		S146/S1103-1/S1103X		UNITS	CONDITIONS
		MIN.	MAX.	MIN.	MAX.		
I _{LI}	Input Leakage Current		1		1	μA	V _{IN} =V _{DD} } All Unused V _{OUT} =V _{DD} } Pins at V _{SS}
I _{LO}	Output Leakage Current		1		1	μA	
I _{BB}	Substrate Supply Current		100		100	μA	
I _{DD1}	Supply Current During T _{PC}		56		75	mA	Address Prechg=V _{DD} ; CE=V _{SS} ; T _A = 25°C
I _{DD2}	Supply Current During T _{OVM}		59		80	mA	Address=Prechg=CE= V _{DD} ; T _A = 25°C
I _{DD3}	Supply Current During T _{POV}		11		13	mA	Address=CE=V _{DD} ; Prechg=R/W=V _{SS} ; T _A = 25°C
I _{DD4}	Supply Current During T _{CP}		4.2		5	mA	Address=V _{DD} ; Prechg=CE=R/W=V _{SS} ; T _A = 25°C
I _{DDAVG}	Average Supply Current (13)		25		33	mA	All Timing Parameters @ Min. Condition; T _A =25°C
I _{OH}	Output High Current	500	4000	850	5000	μA	Over Temperature Range
I _{OL}	Output Low Current		400		800	μA	Over Temperature Range
V _{IL1}	Input Low Voltage (All Add/Data In) (14)	V _{DD}	V _{DD} +1	V _{DD}	V _{DD} +1	V	Over Temperature Range
V _{IL2}	Input Low Voltage (Precharge, CE, RW)	V _{DD}	V _{DD} +1	V _{DD}	V _{DD} +1	V	Over Temperature Range
V _{IH}	Input High Voltage (All Inputs)	V _{SS} -1	V _{SS} +1	V _{SS} -1	V _{SS} +1	V	Over Temperature Range
V _{OH}	Output High Voltage	50	400	85	500	mV	Over Temperature Range
V _{OL}	Output Low Voltage		40		80	mV	Over Temperature Range

NOTES:

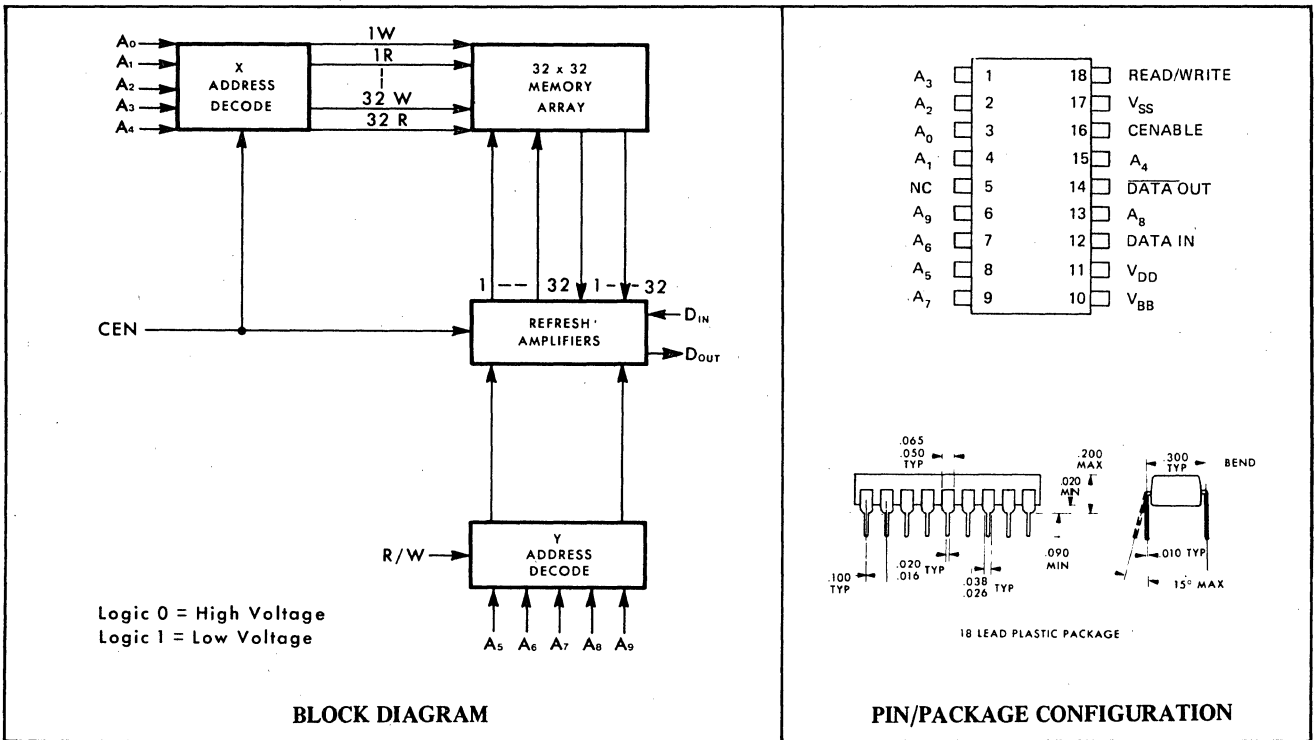
- V_{SS} current drain is equal to (I_{DD} + I_{OH}) or (I_{DD} + I_{OL})
- (V_{BB} - V_{SS}) supply should be applied before V_{SS}.
- R_L of 100 Ω is chosen for convenience. In application, R_L may range from 100 to 1000 Ω.
- t_T is defined as the time between the 10% and 90% point of any voltage transition (t_T ≤ 20ns) (t_T ≤ 12ns for S1103X)
- t_{RC} = t_{PC} + t_{OVM} + t_{POV} + t_{CP} + 3t_T
- t_{ACC1} = t_{AC} + t_{OVM} + t_{PO} + t_T
- t_{ACC2} = t_{PC} + t_{OVM} + t_{PO} + t_T
- t_{WC} = t_{PC} + t_{OVM} + t_{PW} + t_W + t_{CP} + 4t_T
- t_{RWC} = t_{PC} + t_{OVM} + t_{PW} + t_W + t_{CP} + 4t_T
- t_{DW} is referenced to the 90% (negative) point of the rising edge of Chip Enable or Read/Write whichever occurs first.
- t_{DH} is referenced to the 10% (positive) point of the rising edge of Chip Enable or Read/Write whichever occurs first.
- All capacitances are periodically sampled and not 100% tested. Capacitance values are for either plastic or ceramic packages.
- This parameter is periodically sampled and is not 100% tested.
- V_{IL} Max. and V_{IH} Min. are a linear function of T_A between 0°C to maximum temperature. Interim values may be calculated accordingly.

MEMORY AMI

**S1103A
S1103A-1
S1103A-X**



1024 X 1 RANDOM ACCESS MEMORY



Logic 0 = High Voltage
Logic 1 = Low Voltage

BLOCK DIAGRAM

PIN/PACKAGE CONFIGURATION

FEATURES

- Fast access time, 205/145/125 ns
- Performance options subject to power supply levels
- Fast cycle time, 580/340/285 ns
- No precharge required – critical precharge timing is eliminated
- Low standby power dissipation – 0.2 μ W/bit typical
- Address registers incorporated on the chip
- Simple memory expansion – cenable input lead
- Inputs protected against static charge
- Refresh period, 2 ms @ 0 to 70°C

FUNCTIONAL DESCRIPTION

The AMI S1103A family of random access memories are designed for applications where high performance, low cost and large bit storage are desired, such as main memories. It is a 1024 word by 1 bit array fabricated with low threshold, silicon gate technology. This high density process technology allows the design and production of extremely high performance memory devices.

S1103A systems may be simplified due to the elimination of the precharge clock, its associated circuitry, and critical

timing. Only one external clock, CENABLE, is required.

Information stored in the memory is non destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles (addressing A₀ to A₄) and is required every 2 milliseconds. The memory may be used in a low power standby mode by having cenable at V_{SS} potential.

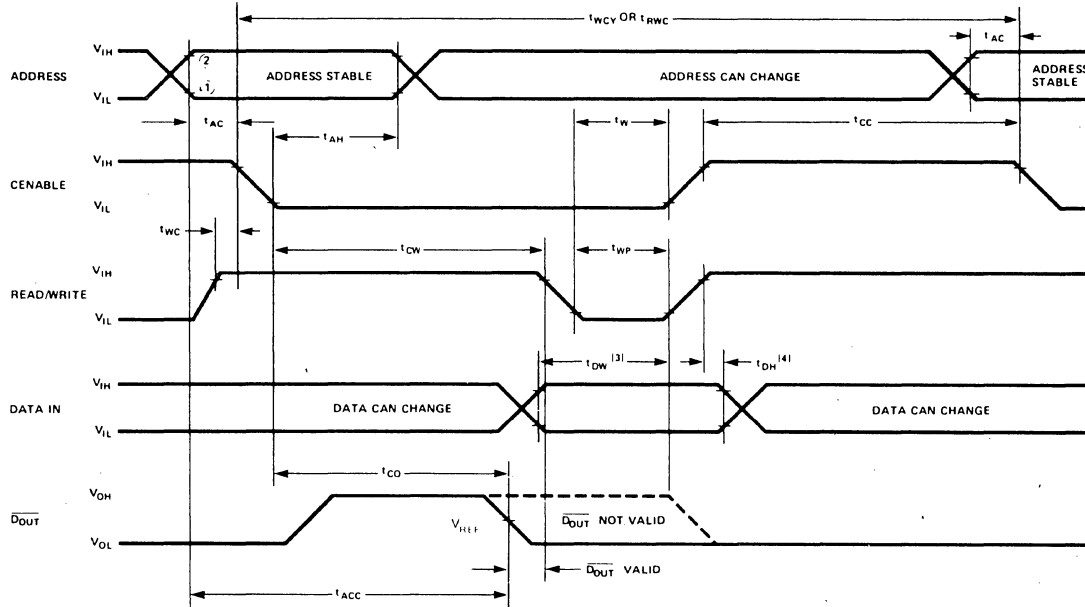
TYPICAL APPLICATIONS

Mainframe Memories, Cache Memories, Buffer Memories, Minicomputer Memories, Mass Memories, Terminals.

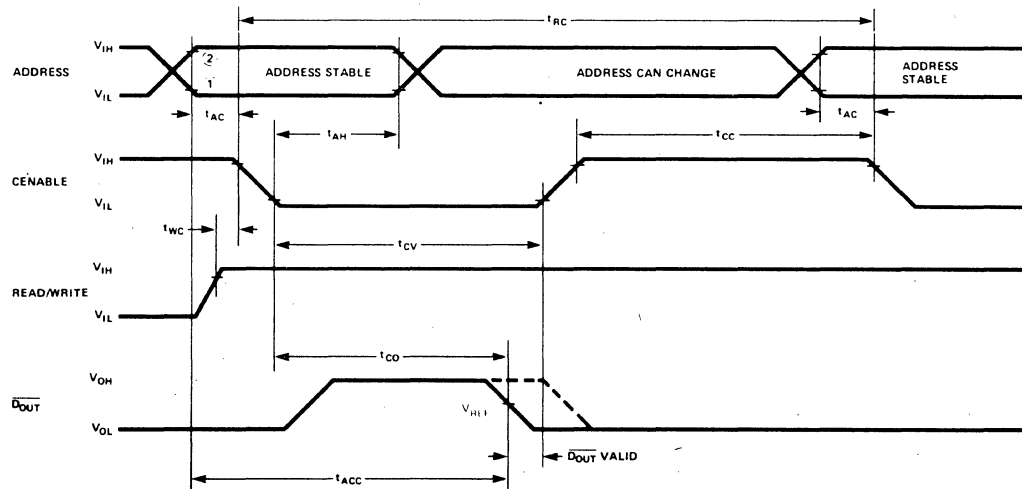
MEMORY AMI

WRITE CYCLE OR READ/WRITE CYCLE

Timing illustrated for minimum cycle.



READ CYCLE



NOTES:

1. 90% Point
2. 10% Point
3. t_{DW} is referenced to point 1 of the rising edge of cenable or Read/Write, whichever occurs first.
4. t_{DH} is referenced to point 2 of the rising edge of cenable or Read/Write, whichever occurs first.

OPERATING, AC AND DC CHARACTERISTICS

OPERATING CHARACTERISTICS		S1103A		S1103A - 1		S1103A-X		UNITS
SYMBOL	TEST DESCRIPTION							
T_A	Ambient Temperature	0 to 70		0 to 55		0 to 55		$^{\circ}\text{C}$
V_{DD}	Negative Supply	0		0		0		V
V_{SS} (5)	Positive Supply	16 ± 0.8		19 ± 1		19 ± 1		V
$V_{BB} - V_{SS}$ (6)	Substrate Supply	3.5 ± 0.5		3.5 ± 0.5		3.5 ± 0.5		V
C_L	Load Capacitance	100		50		50		pF
R_L (7)	Load Resistance	100		100		100		Ω
V_{REF}	Output Reference Voltage	40		80		80		mV
AC CHARACTERISTICS		S1103A		S1103A - 1		S1103A-X		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ, WRITE AND READ/WRITE CYCLE								
t_{REF}	Time between Refresh Cycles		2		2		2	ms
t_{AC}	Address to Chip Enable Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	100		50		50		ns
t_{CC}	Cenable Off Time	230		120		85		ns
READ CYCLE								
t_{RC} (8)	Read Cycle	480		300		305		ns
t_{CV}	Cenable on time	210	500	140	500	120	500	ns
t_{CO}	Cenable Output Delay		185		125		105	ns
t_{ACC} (9)	Address to Output Access		205		145		125	ns
WRITE OR READ/WRITE CYCLE								
t_{WCY} (10)	Write Cycle	580		340		285		ns
t_{RWC} (10)	Read/Write Cycle	580		340		285		ns
t_{CW}	Cenable to Read/Write Delay	210	500	140	500	120	500	ns
t_{WP}	Read/Write Pulse Width	50		20		20		ns
t_W	Read/Write Setup Time	80		20		20		ns
t_{DW}	Data Setup Time	105		40		40		ns
t_{DH}	Data Hold Time	10		10		10		ns
t_{CO}	Output Delay		185		125		105	ns
t_{WC}	Read/Write to Cenable	0		0		0		ns

NOTES:

5. V_{SS} current drain is equal to $(I_{DD} + I_{OH})$ or $(I_{DD} + I_{OL})$
6. $(V_{BB} - V_{SS})$ supply should be applied before V_{SS}
7. R_L of 100Ω is chosen for convenience. In application, R_L may range from 100 to 1000Ω
8. $t_{RC} = t_{CV} + t_{CC} + 2 t_T$
9. $t_{ACC} = t_{AC} + t_{CO} + t_T$
10. $t_{WCY} = t_{RWC} = t_{CW} + t_W + t_{CC} + 3 t_T$

AC CHARACTERISTICS (Cont'd)

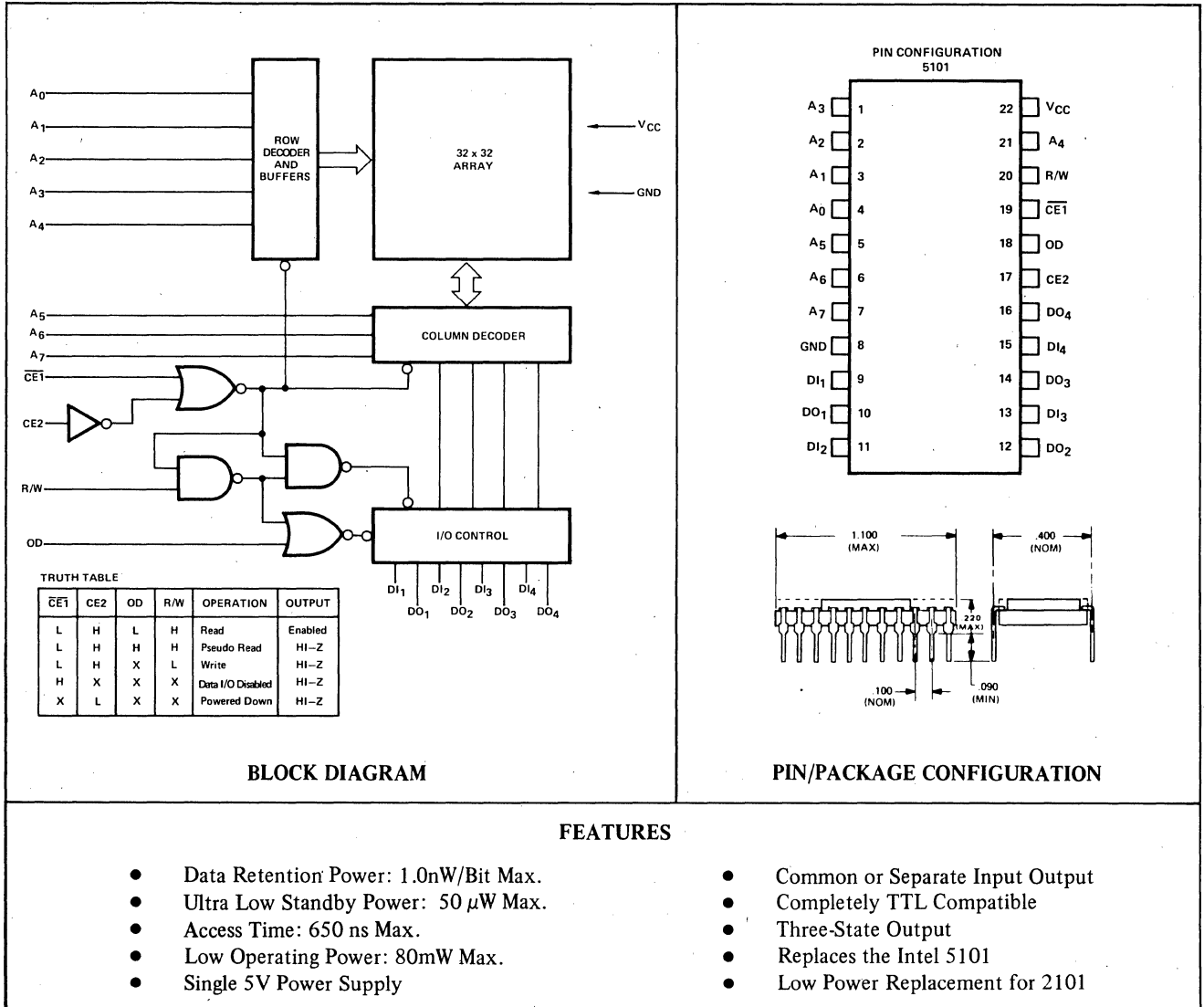
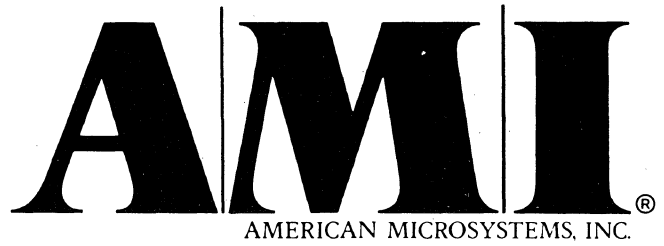
		PLASTIC		CERAMIC	UNIT	CONDITIONS	
		TYP	MAX	MAX			
CAPACITANCE (11)							
C _{AD}	Address	5	7	12	pF	$V_{IN} = V_{SS}$ $V_{IN} = V_{SS}$ $V_{IN} = V_{SS}$ $C_{enable} = 0V$ $V_{IN} = V_{SS}$ $C_{enable} = V_{SS}$ $V_{IN} = V_{SS}$ $V_{OUT} = 0V$	
C _{CE}	Chip Enable	22	25	28	pF		
C _{RW}	Read/Write	11	15	20	pF		
C _{IN1}	Data Input	4	5	8	pF		
C _{IN2}	Data Input	2	4	7	pF		
C _{OUT}	Data Output	2	3	7	pF		
							All Unused Pins @ AC GND $f_0 = 1 \text{ MHz}; V_{BB} = 3.0V, T_A = 25^\circ C$
DC CHARACTERISTICS		S1103A		S1103A-1, S1103A-X		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX		
I _{LI}	Input Leakage Current (All Input Pins)		1		10	μA	$V_{IN} = 0V$
I _{LO}	Output Leakage Current		1		10	μA	$V_{OUT} = 0V$
I _{BB}	Substrate Supply Current		100		100	μA	
I _{DD1}	Supply Current During Cenable On		11		11	mA	$\{ C_{enable} = 0V,$ $T_A = 25^\circ C$
I _{DD2}	Supply Current During Cenable Off		4		0.5	mA	$\{ C_{enable} = V_{SS},$ $T_A = 25^\circ C$
I _{DD AVG}	Average Supply Current		25		33	mA	Cycle Time = 580/ $T_A = 25^\circ C$ 340 ns
V _{IL}	Input Low Voltage	$V_{DD} - 1$	$V_{DD} + 1$	$V_{DD} - 1$	$V_{DD} + 1$	V	
V _{IH}	Input High Voltage	$V_{SS} - 1$	$V_{SS} + 1$	$V_{SS} - 1$	$V_{SS} + 1$	V	
I _{OH1}	Output High Current	600	4000	1150	7000	μA	$T_A = 25^\circ C$
I _{OH2}	Output High Current	500	4000	900	7000	μA	$T_A =$
I _{OL}	Output Low Current	See Note 12		See Note 12			$\left. \begin{matrix} \text{Max Temp} \\ R_L(10) = \\ 100\Omega \end{matrix} \right\}$
V _{OH1}	Output High Voltage	60	400	115	700	mV	$T_A = 25^\circ C$
V _{OH2}	Output High Voltage	50	400	90	700	mV	$T_A =$
V _{OL}	Output Low Voltage	See Note 12		See Note 12			Max Temp

NOTES:

- All capacitances are periodically sampled at worst case operating conditions and are not 100% tested.
- I_{OL} = leakage current of the 1103A plus external noise coupled with the output line from the clocks.
 $V_{OL} = I_{OL}$ across the load resistor.

S5101

1024 BIT (256 x 4)
STATIC CMOS RAM



FUNCTIONAL DESCRIPTION

The AMI S5101 family of 256 x 4 bit high speed CMOS RAMs offers ultra low power and fully static operation with a single 5 volt power supply. With data inputs and outputs on adjacent pins, either separate or common data I/O applications can be easily selected for maximum design flexibility. The very low power of these RAMs makes them an ideal choice where battery augmented non-volatile RAM storage is mandatory.

The S5101 family is totally static, making clocking unnecessary for a new address to be accepted. The stored

data is read-out non-destructively and in the same polarity as the original input data. The outputs are disabled with output disable (O.D.), either chip enable (\overline{CE}_1 or \overline{CE}_2) or during a write cycle ($R/W = LOW$). The read/write input or output disable input allow these RAMs to be used in common data I/O systems by forcing the output into a high impedance state during a write operation.

When deselected, the S5101A draws only 10 microamps from a 5.25 volt supply voltage. The S5101AL is identical to the S5101A with the additional benefit of guaranteed data retention at a power supply voltage of 2.0 volts with guaranteed power dissipation of less than 1.0 nanowatt/bit.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.3V to V _{CC} +1.0V
Maximum Power Supply Voltage	+11V
Power Dissipation	1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS FOR S5101

T_A - 0°C to 70°C, V_{CC} = 5V ± 5% Unless Otherwise Specified.

SYMBOL	PARAMETER	LIMIT		UNITS	TEST CONDITIONS
		MIN.	MAX.		
I _{LI}	Input Leakage Current	-1	1	μA	V _{IN} = 0V to V _{CC}
I _{LO}	Output HI - Z Leakage	-1	1	μA	CE1, R/W = V _{IL} and/or CE2, OD = V _{IH} V _O = 0 to V _{CC}
I _{CC}	Operating Supply Current		15	mA	CE1 = V _{IL} , CE2 = V _{IH} Outputs = OPEN, f _c = 1MHz
I _{CCL}	S5101A/AL		22	mA	
	S5101/L, S5101-3/L-3		22	mA	
I _{CC}	Standby Supply Current		10	μA	CE1 ≥ V _{CC} - 0.8V or CE2
	S5101A/AL, S5101/L		200	μA	≤ 0.8V, V _{IN} = V _O = 0V to V _{CC}
V _{IL}	Input Low Voltage	-0.3	0.8	V	
V _{IH}	Input High Voltage	2.2	V _{CC} + 0.3	V	
V _{OL}	Output Low Voltage		0.4	V	I _{OL} = 2mA
V _{OH}	Output High Voltage	2.4		V	I _{OH} = 1mA

LOW V_{CC} DATA RETENTION CHARACTERISTICS FOR S5101L,

T_A = 0°C to 70°C

SYMBOL	PARAMETER	LIMIT		UNITS	TEST CONDITIONS
		MIN.	MAX.		
V _{DR}	V _{CC} For Data Retention	2.0		V	CE1 ≥ V _{DR} - 0.2V or CE2 ≤ 0.2V, V _{CC} = V _{DR} , t _r = t _f = 20ns
I _{CCDR}	Data Retention Supply Current		0.5	μA	CE1 ≥ V _{DR} - 0.2V or CE2 ≤ 0.2V, V _{CC} = V _{DR} , t _r = t _f = 20ns
			15	μA	
			200	μA	
t _{CDR}	Chip Deselect to Data Retention Time	0		ns	
t _r	Operation Recovery Time	t _{RC}			t _{RC} = Read Cycle Time

MEMORY AMI

A.C. CHARACTERISTICS FOR S5101L

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$ Unless Otherwise Specified.

READ CYCLE

SYMBOL	PARAMETER	LIMIT		UNITS	TEST CONDITIONS
		MIN.	MAX.		
t_{RC}	Read Cycle Time	650		ns	See A.C. Conditions of Test and A.C. Test Load
t_{ACC}	Access Time		650	ns	
t_{CO1}	$\overline{CE1}$ to Output Delay		600	ns	
t_{CO2}	$\overline{CE2}$ to Output Delay		700	ns	
t_{OD}	Output Disable to Enabled Output Delay		350	ns	
t_{DF}	Output Disable to Output HI-Z State Delay	50	150	ns	
t_{DF1}	$\overline{CE1}$ to Output HI-Z Delay	50	220	ns	
t_{DF2}	$\overline{CE2}$ to Output HI-Z Delay	50	270	ns	
t_{OH}	Output Data Valid Into Next Cycle	50		ns	

A.C. CHARACTERISTIC FOR S5101 and S5101L

WRITE CYCLE 1 – SEPARATE OR COMMON DATA I/O USING OUTPUT DISABLE

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$ Unless Otherwise Specified

SYMBOL	PARAMETER	LIMIT		UNITS	TEST CONDITIONS
		MIN.	MAX.		
t_{WC}	Write Cycle Time	650		ns	See A.C. Conditions of Test and A.C. Test Load
t_{AW}	Address to Write Delay	150		ns	
t_{CW1}	$\overline{CE1}$ to End of Write Delay	550		ns	
t_{CW2}	$\overline{CE2}$ to End of Write Delay	550		ns	
t_{DW}	Data Set-Up to End of Write Time	400		ns	
t_{DH}	Data Hold After End of Write Time	100		ns	
t_{WP}	Write Pulse Width (For Write Cycle 1)	400		ns	
t_{WR}	End of Write to New Address Recovery Time	50		ns	
t_{DS}	Output Disable to Data-In Set-Up Time	150		ns	
t_{ODH}	Output Disable After Data-In Hold Time	0		ns	

WRITE CYCLE 2 – Additional Parameters to Guarantee Common I/O Operation with O.D. = V_{OL}
 T_A = 0°C to 70°C, V_{CC} = 5V ± 5% Unless Otherwise Specified

SYMBOL	PARAMETERS	LIMIT		UNITS	TEST CONDITIONS
		MIN.	MAX.		
t _{WF}	Write to Output HI-Z Delay Time		200	ns	See A.C. Conditions of Test and A.C. Test Load
t _{WS}	Write to Data Input Set-Up Time	200		ns	
t _{WDR}	Write to New Data Output Delay Time		300	ns	
t _{WP}	Write Pulse Width (For Write Cycle 2)	450		ns	
t _{AW}	Address to Write Date For Write Cycle 2	150		ns	

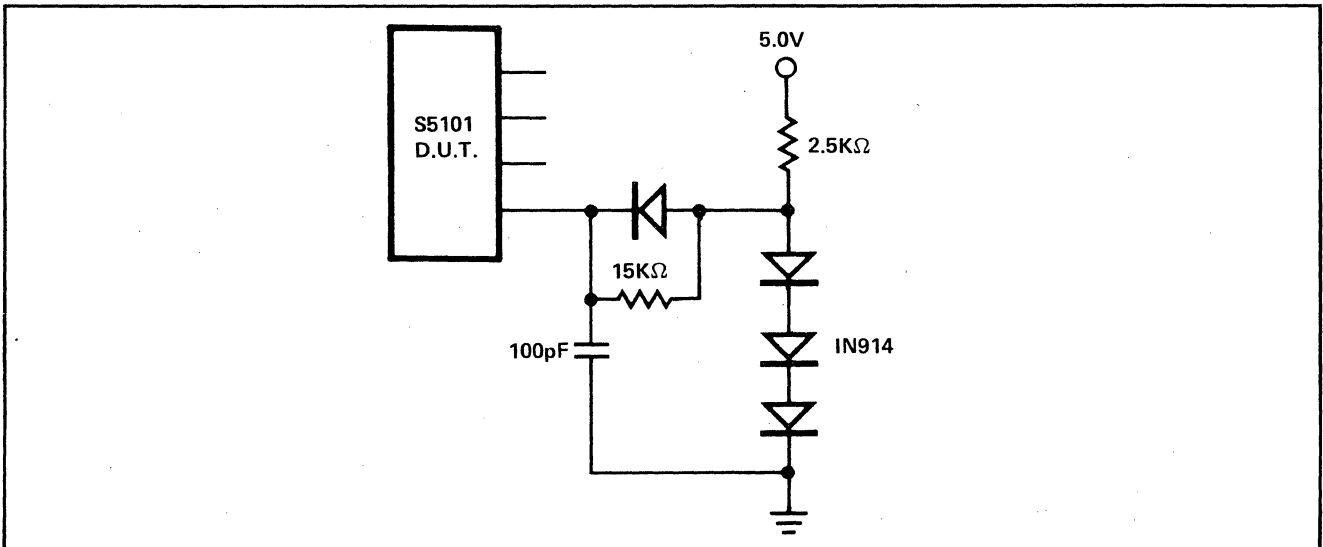
CAPACITANCE

SYMBOL	PARAMETERS	LIMIT		UNITS	TEST CONDITIONS
		MIN.	MAX.		
C _{IN}	Input Capacitance		8	pF	V _{IN} = 0V, on All Input Pin
C _O	Output Capacitance		12	pF	V _O = 0V

A.C. CONDITION OF TEST

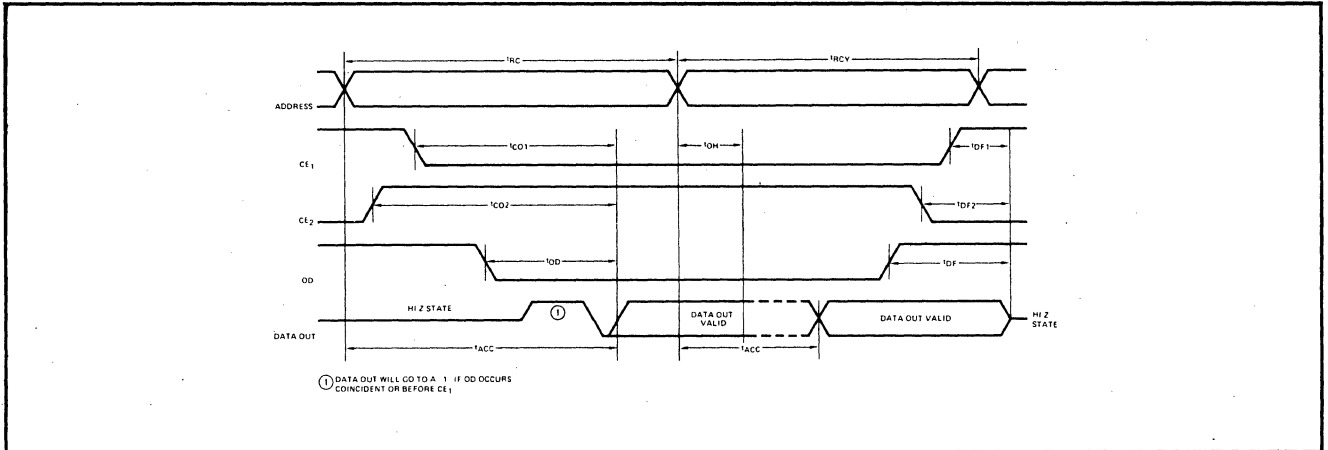
Input Levels	0.8 Volt to 2.2 Volt
Input Rise and Fall	20ns
Timing Measurement Reference Level	1.5 Volt

A.C. TEST LOAD

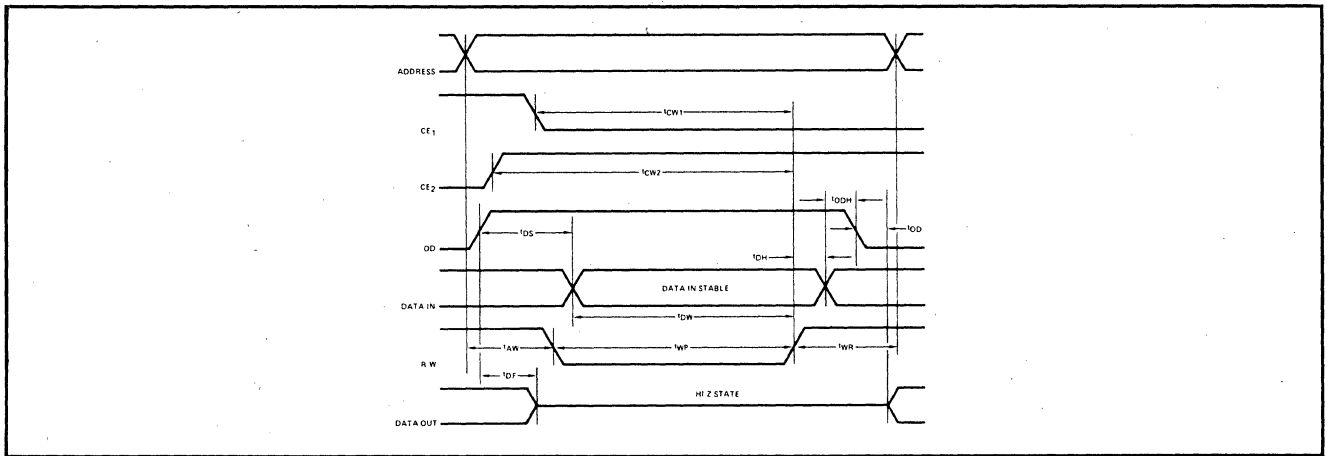


MEMORY AMI

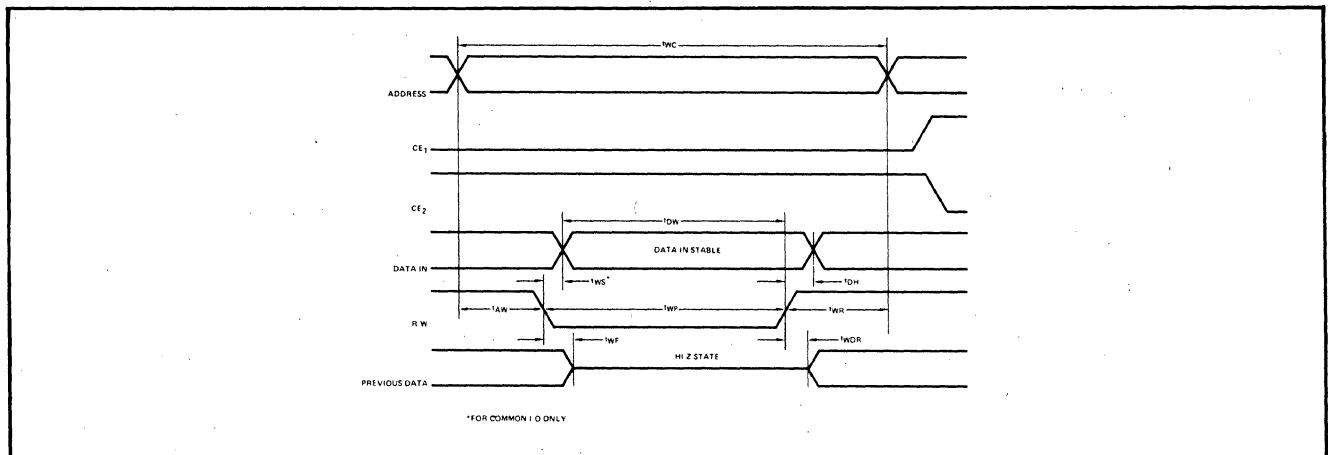
READ CYCLE



WRITE CYCLE 1 – FOR SEPARATE OR COMMON DATA I/O



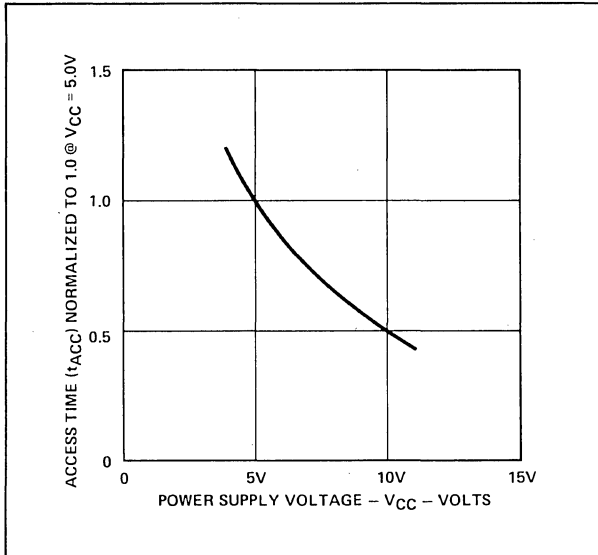
WRITE CYCLE 2 – FOR COMMON DATA I/O



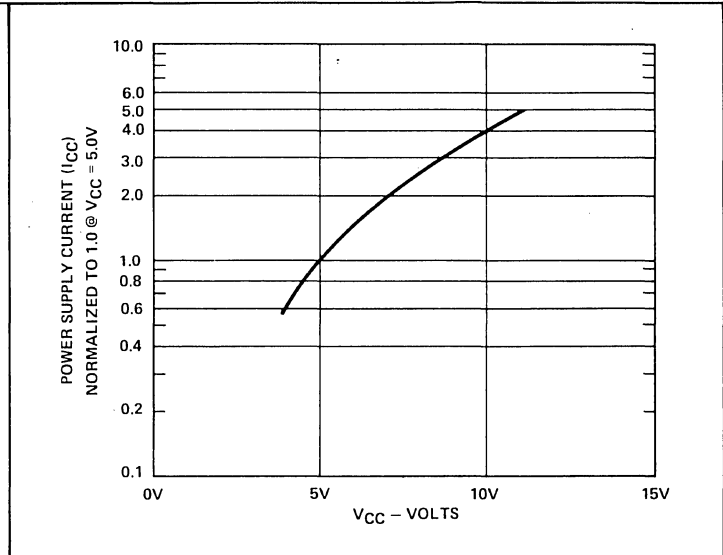
NOTE: OD is Low . *For Common I/O Only

MEMORY AMI

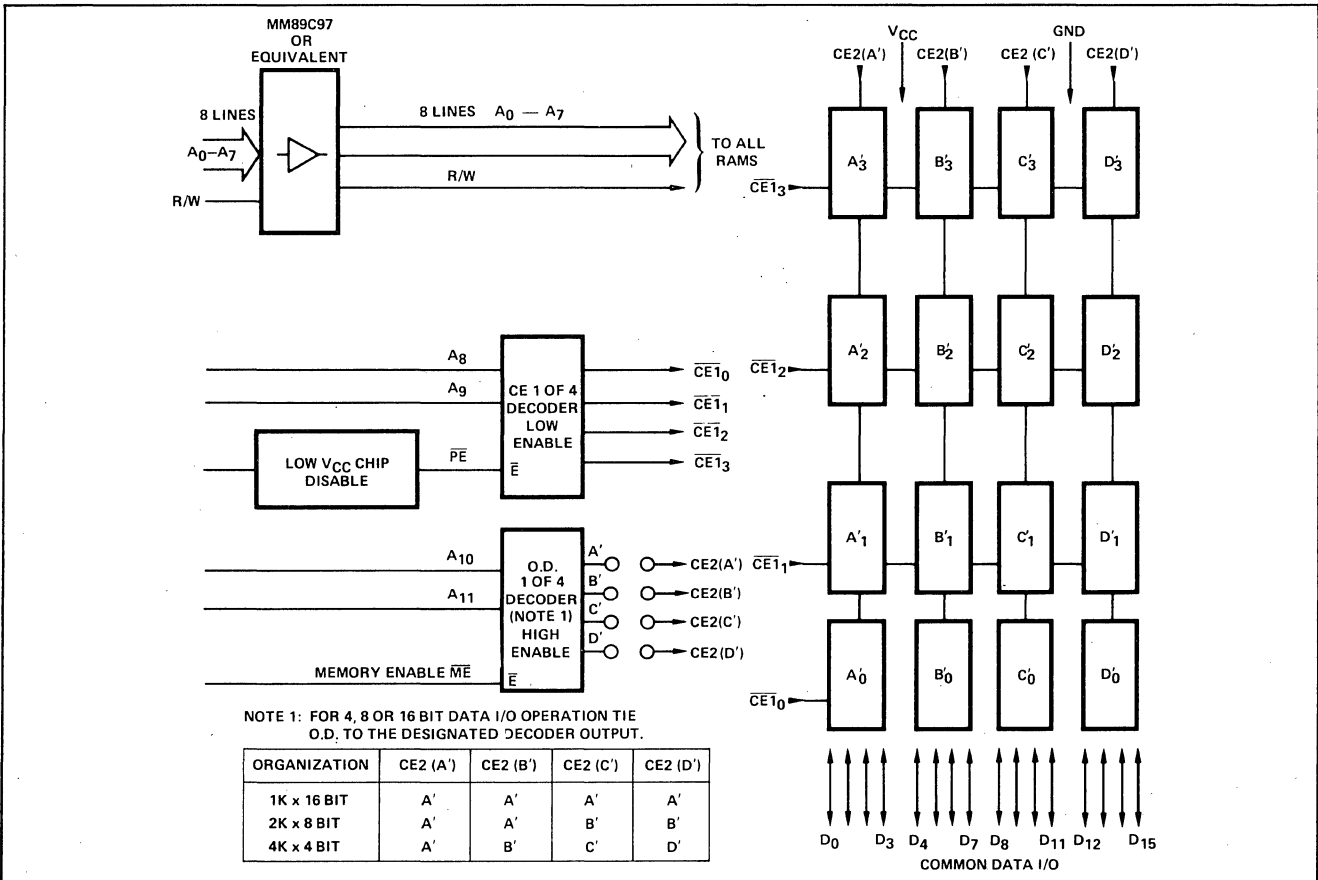
NORMALIZED ACCESS TIME VS. POWER SUPPLY VOLTAGE



NORMALIZED POWER SUPPLY CURRENT VS. POWER SUPPLY VOLTAGE OPERATING AT 1 MHz

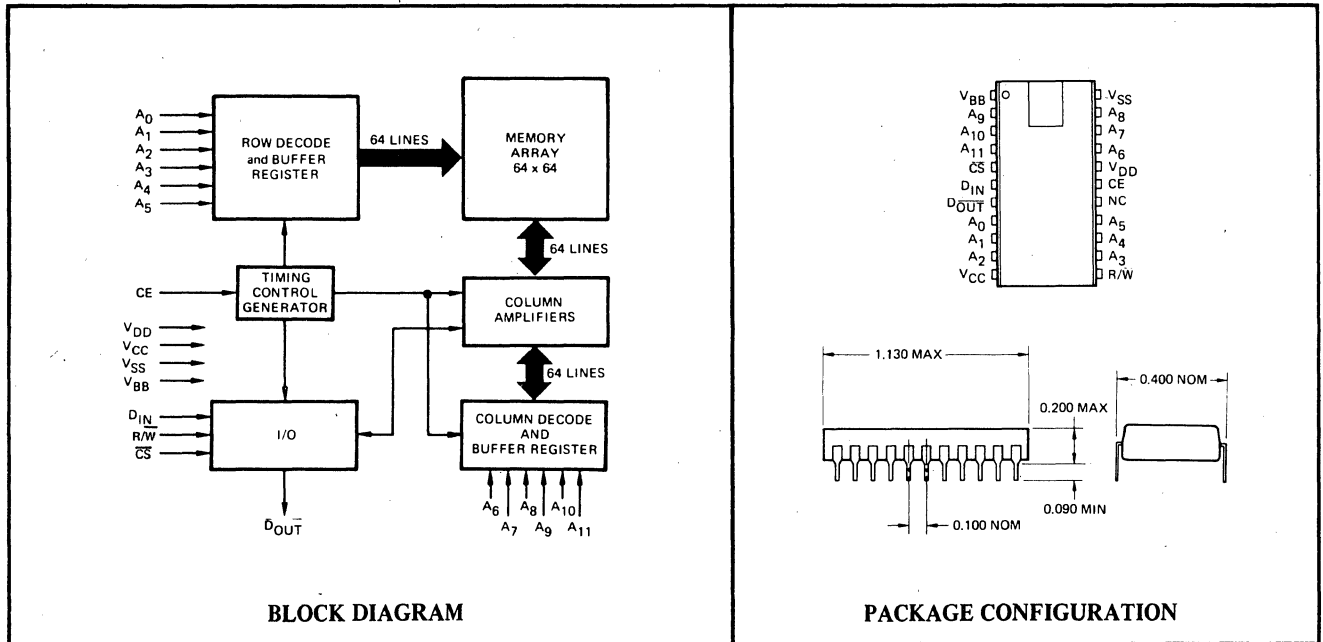


A 1024 x 16 BIT (or 2K x 8 or 4K x 4) CMOS READ/WRITE MEMORY



MEMORY AMI

4096 X 1
 RANDOM ACCESS MEMORY



BLOCK DIAGRAM

PACKAGE CONFIGURATION

FEATURES

- Fast Access Time – 200/250/300ns (max)
- Fast Read or Write Cycle Time – 400/430/470ns (min)
- Fast Read Modify Write Cycle Time – 580/640/710ns (min)
- Low Power Dissipation – 350 mw Operating (Typical)
 1.8mw Standby (Typical)
- Output – Three State and TTL Compatible
- All Inputs TTL Compatible Except Chip Enable Clock
- Refresh Period – 2ms
- 22 Pin Dual-In-Line Package
- Pin Compatible With TMS 4060 and 2107B
- N-Channel Silicon Gate Technology
- One Transistor Per Cell Design
- Smallest 4096 Bit Dynamic RAM

FUNCTIONAL DESCRIPTION

The AMI S4021 series of dynamic RAM memories is designed for applications where high performance, low cost, high reliability and large bit storage are required. The S4021 is a 4096 word by 1 bit array fabricated with N-channel silicon gate technology. The design uses the single transistor approach to achieve high performance and packing density for lower cost.

All addresses and control inputs are TTL compatible except for the chip enable clock (CE). All decoding is done on chip utilizing low power dynamic design techniques and

key control input signals have on-board registers which latch the present state on the chip and provide ease of use in a typical system.

The information read out is non-destructive. Refresh is accomplished by sequencing through the lower order addresses (A₀ - A₅) every 2 ms. This can be done in a single burst mode or by spacing the refresh cycles by 31.25 microseconds.

TYPICAL APPLICATIONS

- Main Frame Memory
- Buffer Memory
- Add-on Memory
- Peripheral Storage
- Terminals
- Controllers, etc.

ABSOLUTE MAXIMUM RATINGS

Voltage on any Pin Relative to Substrate	-0.3V to +20V
Operating Temperature Range	0°C to 70°C
Storage Temperature	-65°C to +150°C

COMMENT: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and is applicable to short duration transient voltages and is not intended to cover those conditions where the device is exposed to voltages equal to or greater than an absolute maximum rating for extended periods. Subjecting the device to voltages equal to or greater than the absolute maximum ratings for extended periods may have a hazardous affect upon the device reliability.

MEMORY AMI

OPERATION

CHIP ENABLE (CE)

The chip enable input is the only clock input to the circuit and with few exceptions is the master signal to which all other timing is related. It is also the only input which is not TTL compatible, requiring a high voltage input signal. (*) When the chip enable input is in the low state the circuit conditions itself, by precharging all internal dynamic nodes, for the subsequent address cycle. This is the low current or standby mode for the device and is the clock condition for which the S4021 dissipates minimum power. When the chip enable input is in the high state and all other inputs properly addressed the device will execute a read or write cycle. The clock high portion of a cycle is the operating segment, during which the device dissipates the maximum power dissipation. The S4021 however, typically, dissipates a low thirty (30) milliamps during the clock high portion of a cycle.

(*) Nominally to 12 volt transitions.

CHIP SELECT (CS)

The chip select input determines which devices in an array will actually execute the read or write cycle. This input controls the data-in, data-out and read/write circuitry on the device enabling or disabling these functions depending on its state. With the proper timing as set out in the timing tables, when chip select is in the low state the device is activated and may execute any designated cycle. When chip select is in the high state the output buffer is in its tri-state mode and the data-in buffer is inhibited from accepting new data. The chip select input buffer is fully TTL compatible and an on-board register is provided for this input so its state may be stored during a cycle execution. The chip select input may be placed in the low state permanently (wire grounded) thereby continuously selecting a particular device; in this mode of operation it is the chip enable input which will determine when the device executes a read or write cycle.

ADDRESS (A₀ - A₁₁)

The address inputs to the device collectively determine which memory bit will be read from or written into. By using an address map one can determine precisely which bit inside the device is being addressed; this being helpful when constructing test programs. The address inputs are all fully TTL compatible and also each input is provided with on board register so the address can be stored for one execution cycle, the details of this timing is in the timing diagrams.

READ/WRITE (R/ \overline{W})

The read/write input controls the mode in which the circuit operates, that is, whether the circuit will execute a read or write cycle. With the proper timing applied to the device and the read/write input in the high state the device will execute a read cycle; with the read/write input in the low state the device will execute a write cycle. Note that the read/write input can make a transition during one chip enable cycle thereby executing a read-modify-write. The read/write input is also fully TTL compatible, however, this input is not supplied with an on board register for data storage; this is done in order to assure operation of the device in the read-modify-write mode.

DATA-IN (DI)

The data-in terminal is the input where the data is written into the device. This input also is not provided with an on board register and therefore the timing of this signal to the device is critical. This input is fully TTL compatible and can be driven from standard TTL circuits without the use of pullup resistors.

DATA-OUT (\overline{DO})

The three state output buffer provides for direct TTL compatibility with the total capability of driving two TTL loads. The output in the deselected state is in the high impedance of floating mode. Data valid is always preceded by the output precharging to a low state. Data-out is inverted with respect to the data-in terminal.

REFRESH

Memory refresh must be performed every two milliseconds by cycling through the 64 combinations of the lower order address A₀ through A₅. This operation can take place with read/write (R/W) in either of its two configurations, however, care must be taken to deselect the device (CS in the high state) if the refresh is accomplished in the write mode. The status of the higher order addressed A₆ through A₁₁ is don't care during a refresh cycle. It is important to note that the two millisecond refresh rate is guaranteed over the full temperature range of 0°C to 70°C still air ambient.

NOTE: A refresh cycle cannot be prematurely aborted in order to accommodate system interrupts or other higher priority commands. Once the clock (CE) comes high for a refresh cycle the entire cycle must be completed.

D.C. OPERATING CHARACTERISTICS: Unless otherwise stated, the D.C. characteristics are valid over the voltage ranges of: $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 10\%$, $V_{BB} = -5V \pm 10\%$ and $V_{SS} = 0$ Volts

Symbol	Parameters	Test Condition	Limits			Units
			Min.	Typ*	Max.	
V_{IH}	High level input voltage (all inputs except chip enable)		2.4		V_{CC}	Volts
V_{IL}	Low level input voltage		0(1)		0.6	Volts
$V_{IH(CE)}$	High level input voltage for chip enable clock		$V_{DD} 0.6$		$V_{DD} + 1.0$	Volts
$V_{IL(CE)}$	Low level input voltage for chip enable clock		0(1)		0.6	Volts
t_{ref}	Refresh cycle time				2	ms
T_A	Operating free air temperature		0		70	°C
V_{OH}	High level output voltage	$I_{OH} = 2.0$ mA	2.4		V_{CC}	Volts
V_{OL}	Low level output voltage	$I_{OL} = 3.2$ mA	V_{SS}		0.4	Volts
I_{DD1}	Operating V_{DD} supply current after transient	$V_{BB} = -4.75V$, $V_{DD} = 12.6V$ $V_{CE} = V_{DD} + 1.0$, $V_{CC} = 5.25V$ $T_A = 0^\circ C$ All inputs 5.25V		30	45	mA
I_{DD2}	Standby V_{DD} supply current after transient				500	μA
I_{DD3}	V_{DD} supply transient with positive CE transition	Nominal condition		85		mA
I_{DD4}	V_{DD} supply transient with negative CE transition	Nominal condition		60		mA
I_{DD5}	Average current from V_{DD} supply	$V_{DD} = 12.6V$, $V_{BB} = -4.75V$, $V_{SS} = 0$ (duty cycle = 70%) $V_{CE} = 0.6$ to 13.6V		30	45	mA
I_{BB}	Supply current for V_{BB} supply	$V_{DD} = 12.6V$, $V_{BB} = 5.25V$, $V_{CE} = 13.6V$, $V_{SS} = 0V$			100	μA
I_{CC}	Average current from V_{CC} supply	$V_{CC} = 5.25V$ duty cycle = 70% from TTL loads			2	mA
I_I	Input leakage on all pins except CE	$V_{in} = 0.4$ to 5.25V			10	μA
$I_I(CE)$	Input leakage on CE	$V_{in} = 0.4$ to 13.6V			10	μA
I_{OZ}	Output leakage current	$V_{out} = 0$ to 5.25V $CS = 2.4V$, $CE = 13.6V$			10	μA

*All typical values are measured in a still air ambient of 25°C (room temperature).

NOTE (1): Minimum low levels on all inputs may be as negative as the value specified in the "Absolute Maximum Ratings" for a period of time not to exceed thirty (30) nanoseconds.

CAPACITANCE

Symbol	Parameters	Limits			Units
		Min.	Typ.	Max.	
C_{AD}	Address Capacitance		5	7	pf
C_{CE}	CE Capacitance		17	25	pf
C_{IN}	D_{IN} and R/W Capacitance		5	8	pf
C_{OUT}	D_{OUT} Capacitance		4	6	pf

All measurements made with a Boonton meter or equivalent at .25°C ambient temperature.

A.C. OPERATING CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C ; $V_{DD} = +12\text{V} \pm 5\%$, $V_{CC} = +5\text{V} +10\%$, $V_{BB} = -5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$
COMMON READ/WRITE CYCLE TIMING

Symbol	Parameter	S4021-4		S4021-3		S4021-2		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_C	Cycle Time	400		430		470		ns
t_{CEH}	Chip Enable High	230	4000	260	4000	300	4000	ns
t_{CEL}	Chip Enable Low	130		130		130		ns
t_R, t_F	Rise Time		20		20		20	ns
t_{AS}	Address Set Up	0		0		0		ns
t_{AH}	Address Hold	150		150		150		ns
t_{CSS}	Chip Sel. Set Up	0		0		0		ns
t_{CSH}	Chip Sel. Hold	150		150		150		ns

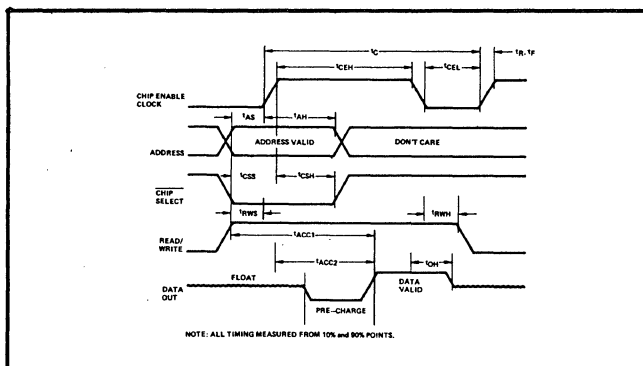
READ CYCLE TIMING

Symbol	Parameter	S4021-4		S4021-3		S4021-2		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RWS}	Read Set Up	0		0		0		ns
t_{RWH}	Read Hold	40		40		40		ns
t_{ACC1}	Access Time from Address		200		250		300	ns
t_{ACC2}	Access Time from Chip Enable High		180		230		280	ns
t_{OH}	Output Hold	0		0		0		ns

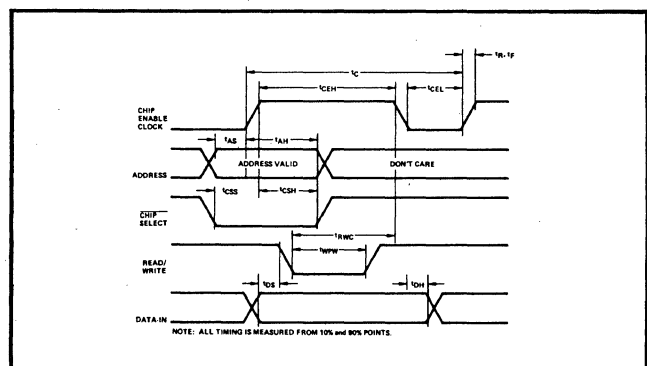
WRITE CYCLE TIMING

Symbol	Parameter	S4021-4		S4021-3		S4021-2		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WPW}	Write Pulse Width	180		190		200		ns
t_{RWC}	Write Set Up	210		220		240		ns
t_{DS}	Data Set Up	0		0		0		ns
t_{DH}	Data Hold	40		40		40		ns

READ CYCLE TIMING



WRITE CYCLE TIMING



A.C. OPERATING CHARACTERISTICS

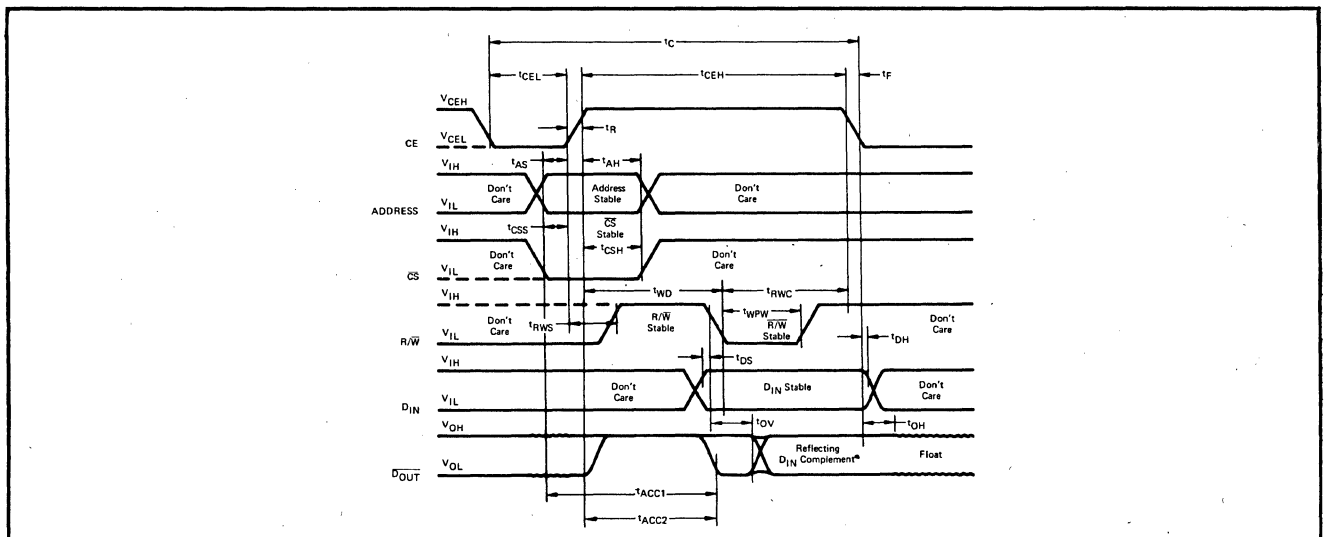
$T_A = 0^\circ\text{C}$ to 70°C ; $V_{DD} = +12\text{V} \pm 5\%$; $V_{CC} = +5\text{V} \pm 10\%$; $V_{BB} = -5\text{V} \pm 10\%$; $V_{SS} = 0\text{V}$

READ-MODIFY-WRITE CYCLE

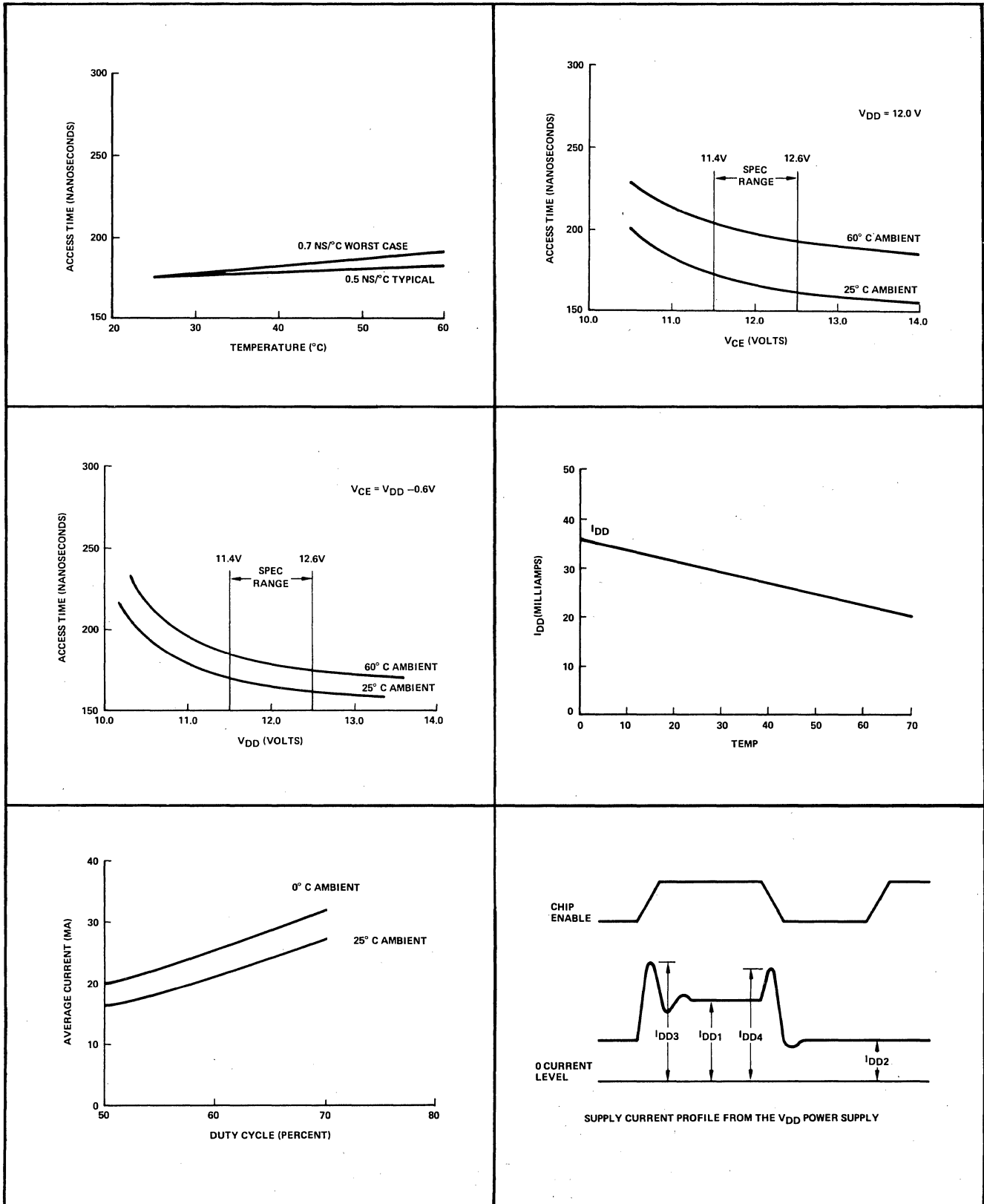
Symbol	Parameter	S4021-4		S4021-3		S4021-2		Units																																				
		Min.	Max.	Min.	Max.	Min.	Max.																																					
t_C	Cycle Time	580		640		710		ns																																				
t_{CEH}	Chip Enable High	410		470		540		ns																																				
t_{CEL}	Chip Enable Low	130		130		130		ns																																				
t_R, t_F	Rise Time and Fall Time		20		20		20	ns																																				
t_{AS}	Address Set Up	0		0		0		ns																																				
t_{AH}	Address Hold Time	150		150		150		ns																																				
t_{CSS}	Chip Select Set Up	0		0		0		ns																																				
t_{CSH}	Chip Select Hold	150		150		150		ns																																				
t_{RWS}	Read Set Up Time	0		0		0		ns																																				
t_{WPW}	Write Pulse Width	180		190		200		ns																																				
t_{RWC}	Write Pulse Set Up	210		220		240		ns																																				
t_{DS}	Data Set Up	0		0		0		ns </tr <tr> <td>t_{DH}</td> <td>Data Hold Past Chip Enable</td> <td>40</td> <td></td> <td>40</td> <td></td> <td>40</td> <td></td> <td>ns</td> </tr> <tr> <td>t_{ACC1}</td> <td>Access Time From Address</td> <td>200</td> <td></td> <td>250</td> <td></td> <td>300</td> <td></td> <td>ns</td> </tr> <tr> <td>t_{ACC2}</td> <td>Access Time From Chip Enable High</td> <td>180</td> <td></td> <td>230</td> <td></td> <td>280</td> <td></td> <td>ns</td> </tr> <tr> <td>t_{DV}</td> <td>Output Data Valid Past Write Set Up</td> <td>0</td> <td></td> <td>0</td> <td></td> <td>0</td> <td></td> <td>ns</td> </tr>	t_{DH}	Data Hold Past Chip Enable	40		40		40		ns	t_{ACC1}	Access Time From Address	200		250		300		ns	t_{ACC2}	Access Time From Chip Enable High	180		230		280		ns	t_{DV}	Output Data Valid Past Write Set Up	0		0		0		ns
t_{DH}	Data Hold Past Chip Enable	40		40		40		ns																																				
t_{ACC1}	Access Time From Address	200		250		300		ns																																				
t_{ACC2}	Access Time From Chip Enable High	180		230		280		ns																																				
t_{DV}	Output Data Valid Past Write Set Up	0		0		0		ns																																				

NOTE: (1) The falling edge of the read/write signal for the write cycle portion is 20 ns.
(2) All timing is measured between 10% and 90% points

READ-MODIFY-WRITE: TIMING DIAGRAM(2)

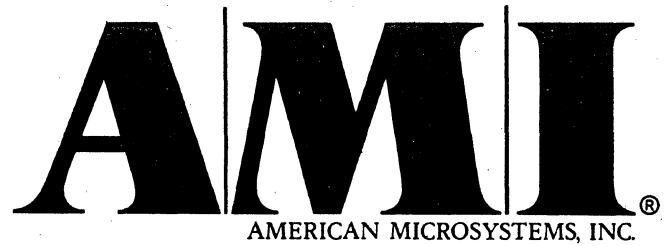


TYPICAL PERFORMANCE CHARACTERISTICS

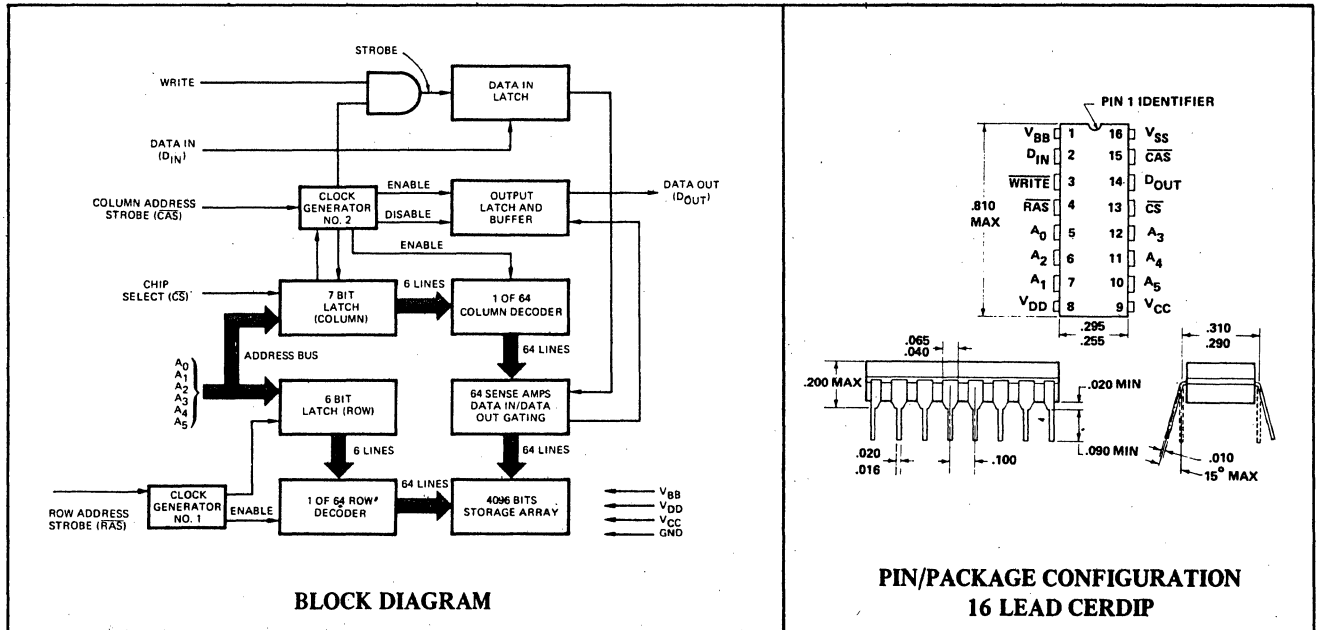


S4096-3
S4096-2
S4096-1

RANDOM ACCESS MEMORY



ADVANCED PRODUCT DESCRIPTION



FEATURES

- Fast Access Time – 250/300/350 nsec (max)
- Fast Read or Write Cycle – 375/425/475nsec
- Fast Read Modify Write Cycle 520/600/675nsec
- Low Power Dissipation – 400 MW Operating (Typ)
6MW Standby (Typ)
- All Inputs TTL Compatible
- Three State TTL Compatible Output
- On-Chip Latches for Addresses, Chip Select, and Data-In
- Refresh Period – 2 msec
- 16 Pin Dip
- N-Channel Silicon Gate Technology
- Industry Standard Pinout

FUNCTIONAL DESCRIPTION

The AMI S4096 series of dynamic N-Channel MOS RAM's are designed for applications where high performance, low cost and large bit storage are desired such as in mainframe, add-on, buffer memories and peripheral storage. The S4096 is a 4096 word by 1 bit array fabricated with selective oxidation N-Channel silicon gate technology. The S4096 has the same memory array structure and uses the identical process as the S4021, AMI's 22 Pin 4K RAM. The S4096 uses a single transistor cell design to achieve higher performance and smaller die size for low cost.

All inputs are TTL compatible, and the output is three-state TTL compatible. The two low voltage clocks are Row Address Strobe (RAS) and Column Address Strobe (CAS) which latch the six row address bits and six column address bits respectively. These twelve bits are multiplexed onto the six address pins. This technique permits packaging of the S4096 in a standard 16 Pin dual-in-line package. In addition, the S4096 has on chip buffers for easy interfacing and optimal input levels for maximum noise immunity and two chip select methods that allows the user to achieve maximum flexibility

in selecting the speed/power characteristics most beneficial to his memory system.

The information read out is non-destructive (NDRO). Refresh of the entire memory is accomplished by performing one active cycle on each of the 64 row addresses every 2 ms.

TYPICAL APPLICATIONS

Mainframe Memories, Buffer Memories, Add-On Memories, Minicomputers, Peripheral Storage, Terminals, Controllers, etc.

ADDRESSING

Addressing the cell location is accomplished by multiplexing the 12 address bits onto the 6 address pins. The 6 row address bits are strobed and latched by the Row Address Strobe (RAS) into the on-chip row buffers. Similarly, the 6 column address bits are, at a later time, strobed and latched by the Column Address Strobe ($\overline{\text{CAS}}$) into the on-chip column buffers. Chip Select signal is latched by $\overline{\text{CAS}}$ and therefore has no impact on system access or cycle time.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register. The data is strobed into the register by a combination of $\overline{\text{WRITE}}$ and $\overline{\text{CAS}}$. The last of these signals making its negative transition is the strobe for the Data In register. This flexibility in timing permits several options in the write timing. In a write cycle, if the $\overline{\text{WRITE}}$ input is activated at the beginning of a cycle, then the Data In is strobed by $\overline{\text{CAS}}$ and the set-up and hold time are referenced to this signal. In this instance the output will unconditionally go to a logic 1 at access time. If the cycle were a read-modify-write cycle, the $\overline{\text{WRITE}}$ input would not go to a logic 0 until after access time. But, because $\overline{\text{CAS}}$ is already at a logic 0, the Data In is strobed in by $\overline{\text{WRITE}}$ and the set-up and hold time are referenced to it. The only other timing constraint in write-type cycles besides Data In set-up and hold time is that both $\overline{\text{WRITE}}$ and $\overline{\text{CAS}}$ be at a logic 0 for a sufficient time to accomplish the write.

At the beginning of a memory cycle the state of the Data Out latch and buffer depends on the previous memory cycle. If during the previous cycle the chip was unselected, the output buffer will be in its open-circuit condition. If the previous cycle was a read or read-modify-write cycle and the chip was selected, then the output latch and buffer will contain the data read from the selected cell. This output data

has the same polarity (not inverted) as the input data. If the previous cycle was a write cycle and the chip was selected, then the output will remain high. Regardless of the state of the output it will remain valid until $\overline{\text{CAS}}$ goes negative. At that time the output will unconditionally go to its open-circuit state. It will remain open circuit until access time. At access time the output will assume the proper state for the type of cycle performed. If the chip is unselected, it will not accept a $\overline{\text{WRITE}}$ command and the output will remain in the open-circuit state.

INPUT/OUTPUT LEVELS

All inputs, including the two address strobes, are TTL compatible. The high impedance, low capacitance (< 10pF) input characteristics simplify input driver selection by allowing use of standard logic elements rather than specially designed driver elements. The three-state output buffer is a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The separate V_{CC} pin goes to the output buffer only and allows it to be powered from the supply voltage of the logic to which the chip is interfaced.

POWER DISSIPATION/STANDBY MODE

Most of the circuitry used in the S4096 is dynamic and draws only AC power. Power dissipation is therefore a function of operating frequency. Worst case power is less than 440 mW at a 500 nsec cycle time. To reduce the overall system power the Row Address Strobe ($\overline{\text{RAS}}$) must be decoded and supplied to only the selected chips. The $\overline{\text{CAS}}$ must be supplied to all chips (to turn off the unselected outputs). But those chips that did not receive a $\overline{\text{RAS}}$ will dissipate only the standby power. If the $\overline{\text{RAS}}$ is decoded and supplied to the selected chips, then the Chip Select input of all chips can be a logic 0. The chips that receive a $\overline{\text{CAS}}$ but no $\overline{\text{RAS}}$ will be unselected (output open-circuited) regardless of the Chip Select input. Thus, the standby mode of the chip is implemented when $\overline{\text{RAS}}$ is high regardless of the state of $\overline{\text{CAS}}$.

REFRESH

The S 4096 is refreshed by performing a memory cycle at each of the 64 row addresses every 2 milliseconds or less. Any read or read-modify-write cycle refreshes the selected row regardless of the state of the Chip Select. A write cycle can be used to refresh the selected row but the chip must be unselected, or the addressed cell will be written with new information.

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin Relative to Substrate	- 0.3V to + 20V	Operating Temperature Range	0°C to + 70°C
		Storage Temperature	- 65°C to + 150°C

COMMENT: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC & OPERATING CHARACTERISTICS

$T_A = 0^\circ - 70^\circ\text{C}$, $V_{DD} = + 12\text{V} \pm 5\%^{(1)}$; $V_{CC} = + 5\text{V} \pm 10\%^{(1)}$, $V_{BB} = - 5\text{V} \pm 10\%^{(1)}$, $V_{SS} = 0\text{V}^{(1)}$

SYMBOL	PARAMETER	MIN	LIMITS TYP	MAX	UNITS	COMMENTS
V_{IL}	Input Low Voltage. All Inputs	- 1.0		0.6	V	See Note 1
V_{IH}	Input High Voltage. All Inputs except $\overline{\text{RAS}}$, $\overline{\text{CAS}}$,	2.4		$V_{CC} + 1$	V	See Note 1
V_{IHC}	Input High Voltage: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$	3.0		$V_{CC} + 1$	V	See Note 1
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 2.0\text{ mA}$
V_{OH}	Output High Voltage	2.4		V_{CC}	V	$I_{OH} = - 3.0\text{ mA}$, See Note 6.
I_{IL}	Input Leakage Current			10	μA	See Note 4
I_{OL}	Output Leakage Current for High Impedance State			10	μA	See Note 5
I_{DDA}	Average V_{DD} to V_{SS} Current Active Mode			35	mA	See Note 8
I_{DDS}	Average V_{DD} to V_{SS} Current, Standby Mode			2	mA	$\overline{\text{RAS}}$ at V_{IHC} , $\overline{\text{CAS}}$, $\overline{\text{CS}}$ DON'T CARE
I_{CC}	V_{CC} Supply Current			10	μA	$\overline{\text{CS}} = 2.4\text{V}$ $\overline{\text{RAS}}$, $\overline{\text{CAS}} = \text{DON'T CARE}$
I_{BB}	V_{BB} Supply Current			75	μA	

CAPACITANCE

SYMBOL	PARAMETER	MAX	UNITS
C_C	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{CS}}$ Capacitance	10	pF
C_{IN}	Address, $\overline{\text{CS}}$, D_{IN} and $\overline{\text{WRITE}}$ Capacitance	7	pF
C_{OUT}	D_{OUT} Capacitance	8	pF

MEMORY AMI

AC OPERATING CHARACTERISTICS

$T_A = 0^\circ - 70^\circ\text{C}$, $V_{DD} = +12\text{V} \pm 5\%$,⁽¹⁾ $V_{CC} = +5\text{V} \pm 10\%$,^(4, 6) $V_{BB} = -5\text{V} \pm 10\%$,⁽¹⁾ $V_{SS} = 0\text{V}$ ⁽¹⁾

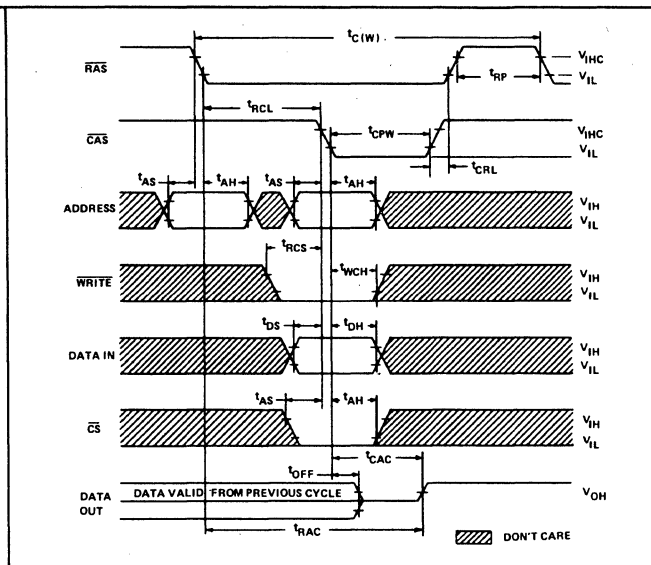
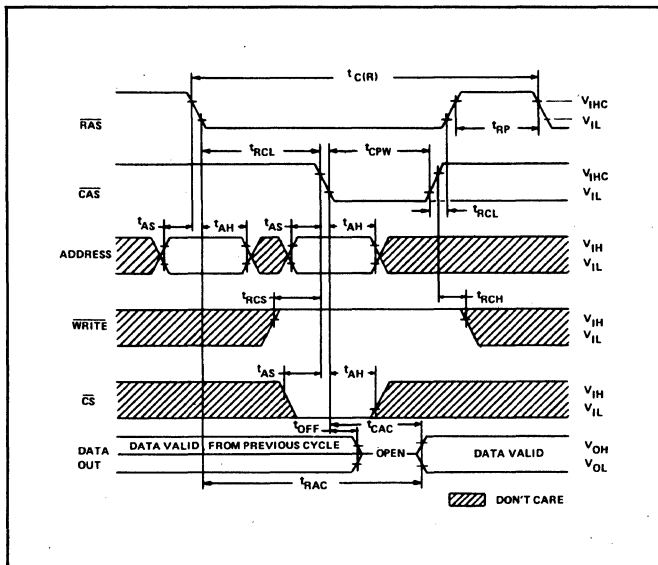
SYMBOL	PARAMETER	S4096-3		S4096-2		S4096-1		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{RAC}^{(7)}$	Access Time from $\overline{\text{RAS}}$		250		300		350	nsec
t_{CAC}	Access Time from $\overline{\text{CAS}}$		140		165		200	nsec
$t_{C(R)}$	Read Cycle Time	375		425		475		nsec
$t_{C(W)}$	Write Cycle Time	375		425		475		nsec
$t_{C(RMW)}$	Read Modify, Write Cycle Time	520		600		675		nsec
$t_{OFF}^{(3)}$	Output Buffer, Turn-Off Delay	0	60	0	80	0	100	nsec
t_{RP}	$\overline{\text{RAS}}$ Precharge Time	125		125		125		ns
t_{RCL}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Lead Time	70	110	90	130	110	150	ns
t_{CPW}	$\overline{\text{CAS}}$ Pulse Width	140		170		200		ns
t_{AS}	Address Set-Up Time	0		0		0		ns
t_{AH}	Address Hold Time	60		80		100		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		ns
t_{RCH}	Read Command Hold Time	0		0		0		ns
$t_{WCH}^{(2)}$	Write Command Hold Time	110		130		150		ns
t_{CRL}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Lead Time	-40	+40	-45	+45	-50	+50	ns
t_{DS}	Data In Set-Up Time	0		0		0		ns
t_{DH}	Data In Hold Time	110		130		150		ns
t_T	Rise and Fall Times	5	50	5	50	5	50	ns
t_{REF}	Time Between Refresh		2.0		2.0		2.0	ms
t_{MOD}	Modify Time	0	10	0	10	0	10	ns

NOTES:

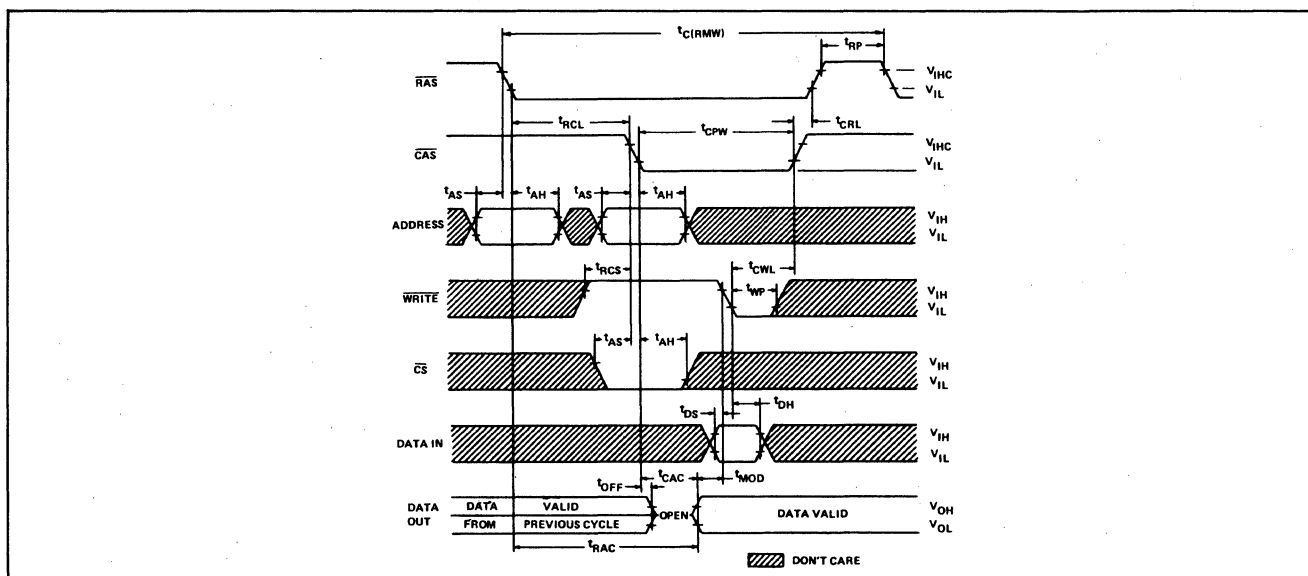
1. All voltages referenced to V_{SS}
2. Write Command Hold Time is important only when performing normal random write cycles. During read-write or read-modify write cycles, the Write Command Pulse Width is the limiting parameter.
3. Depends upon output loading.
4. All device pins at 0 volts except V_{BB} at -5 volts and pin under test which is at +10 volts.
5. Output disabled by chip select input.
6. Output voltage will swing from V_{SS} to V_{CC} independent of differential between V_{SS} and V_{CC}
7. Assumes t_{RCL} is minimum.
8. Typical V_{DD} current at 1.0 MHz cycle rate.

READ CYCLE TIMING

WRITE CYCLE TIMING



READ-MODIFY-WRITE TIMING



MEMORY AMI

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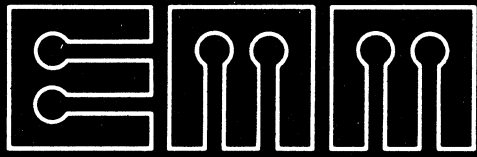
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4096x1

SEMI 4402A 200 NSEC, STATIC, DIFFERENTIAL OUTPUT N-MOS RAM

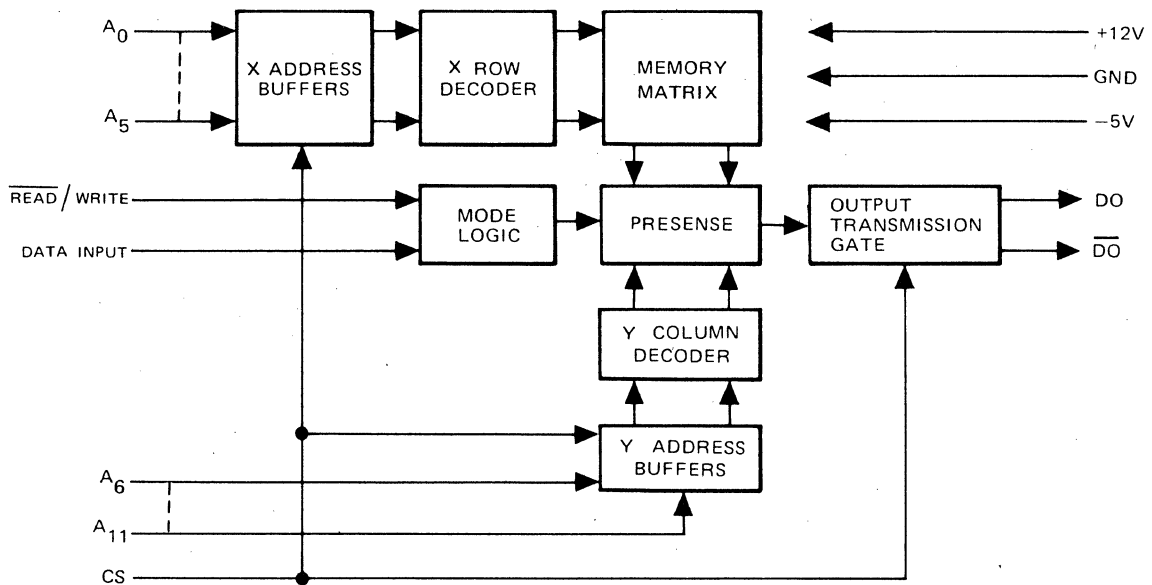
FEATURES

- STATIC – NO REFRESH OR CHARGE PUMP OSCILLATOR REQUIRED
- 4096 WORD x 1 BIT ORGANIZATION
- 200 NSEC ACCESS TIME
- 350 NSEC CYCLE TIME
- ON-CHIP ADDRESS REGISTER
- TTL COMPATIBLE ADDRESS AND DATA INPUTS
- LOW OPERATING POWER 400 MW TYP.
- DATA RETENTION TO $V_{DD} = 4V$
- STANDARD 22 PIN DIP, PIN AND VOLTAGE COMPATIBLE WITH POPULAR 4096 BIT DYNAMIC RAMS

EMM/SEMI

MEMORY

BLOCK DIAGRAM




ABSOLUTE MAXIMUM RATINGS (See Note 1) (Referenced to GND)

Rating	Symbol	Value	Unit
Supply Voltages	V_{DD}	-0.5 to +15	Vdc
	V_{SX}	+0.5 to -7	Vdc
Input & Output Voltages (except Chip Select)	V_I, V_O	V_{SX} to +15	Vdc
Chip Select Input Voltage	V_{CS}	V_{SX} to +15	Vdc
Power Dissipation	P_D	1.6 (Note 2)	W
Operating Ambient Temperature Range	T_{AMB}	0 to +70	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Note 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMEND OPERATING CONDITIONS. Exposure to higher than recommended or maximum voltages for extended periods of time could affect device reliability.

Note 2: At 25°C ambient, Derate 13.5mw/°C.

RECOMMENDED OPERATING CONDITIONS $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltages	V_{DD}	11.4	12	12.6	V
	V_{SX}	-4.5	-5	-5.5	V
Logic Levels					
Input High Voltage (except Chip Select)	V_{IH}	3	-	5.25	V
Input Low Voltage (except Chip Select)	V_{IL}	0	-	0.7	V
Chip Select High Voltage	V_{CH}	$V_{DD}-2$	V_{DD}	$V_{DD}+2$	V
Chip Select Low Voltage	V_{CL}	0	-	0.5	V

DC ELECTRICAL CHARACTERISTICS (Full Operating voltage & temperature range unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit	
Input Current (except Chip Select)	$V_{IH} = 5.0V$ ($V_{CS} = V_{CH}$)	I_{IH}	-	5	μA	
	$V_{IL} = 0.5V$ ($V_{CS} = V_{CH}$)	I_{IL}	-	-5	μA	
Chip Select High Input Current, DC ($V_{CS} = 12V$)	I_{CH}	-	2	3	mA	
Chip Select High Input Current, (Pulse Peak) $V_{CS} = 12V$, $T_{CR} = 25\text{ns}$	I_{CP}	-	70	-	mA	
Chip Select Low Input Current ($V_{CS} = 5V$)	I_{CL}	-	2	3	mA	
Supply Current, ($T_{AMB} = 25^\circ\text{C}$; V_{DD}, V_{SX} = nominal; all $V_I = \max V_{IL}$; $\overline{DO}, \overline{DQ}$)	Unselected (Chip Select = 0 V)	$I_{DDU} 25^\circ\text{C}$	-	1	5	mA
		$I_{DDU} 70^\circ\text{C}$	-	3	15	mA
	Selected CSW 200ns Cycle = 350ns	I_{SXU}	-	-2	-3	mA
		I_{DD}	-	36	50	mA
Standby Current at Reduced Voltages $V_{DD} = 4V, V_{SX} = -4.5V, V_{CS} = 0V$	25°C	I_{DDs}	-	.5	1.8	mA
	70°C	I_{DDs}	-	1.5	5.4	mA
Output Low Voltage CSW = 1 μsec	V_{OL}	-	0	.1	V	
Output High Voltage CSW = 1 μsec	V_{OH}	.35	1	2	V	
Output Disabled Current $V_{CS} = 0V, V_O = 2V$	I_{DO}	+10	-	-10	μA	

AC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range Unless Otherwise Noted)

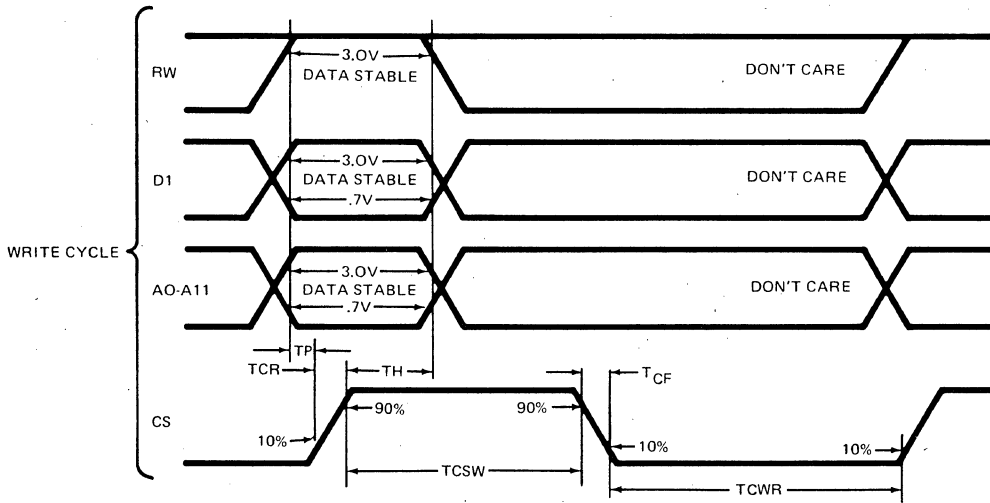
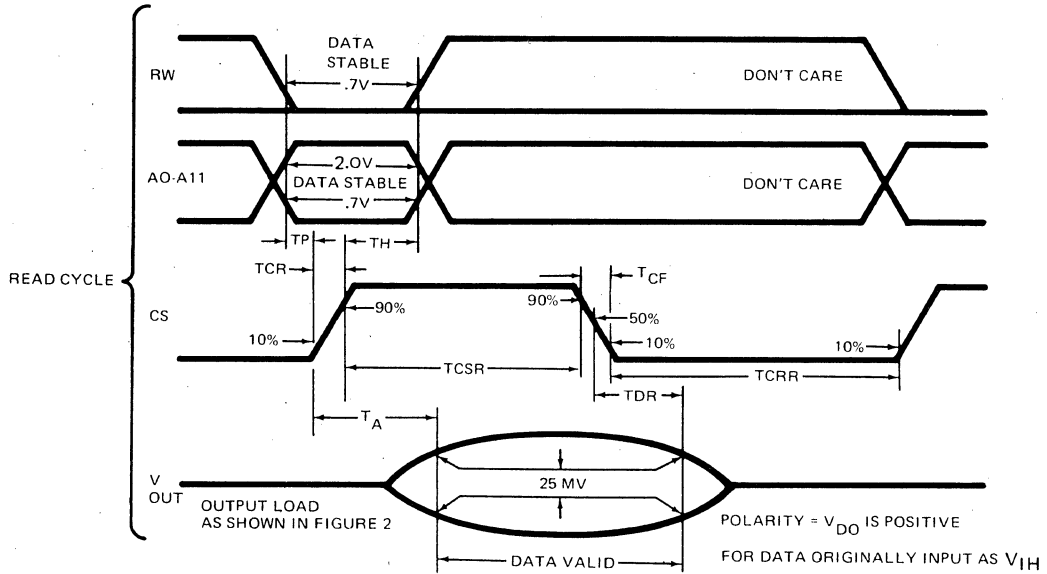
Characteristics	Symbol	Min	Typ	Max	Unit
Chip Select Read Pulse Width	T_{CSR}	200	-	∞	ns
Chip Select Read Recovery Time	T_{CRR}	125	-	∞	ns
Chip Select Write Pulse Width	T_{CSW}	200	-	∞	ns
Chip Select Write Recovery Time	T_{CWR}	125	-	∞	ns
Chip Select Rise Time	T_{CR}	-	10	50	ns
Chip Select Fall Time	T_{CF}	-	10	50	ns
Set Up Time	T_P	10	-	-	ns
Hold Time (Address and Data)	T_H	100	-	-	ns
Access Time ($T_{CR} = 10\text{ns}$)	T_A	-	-	200	ns
Cycle Time (Read or Write, $T_{CR} = 10\text{ns}, T_{CF} = 10\text{ns}$)	T_C	350	-	-	ns
Data Recovery	T_{DR}	10	15	-	ns

CAPACITANCE (Over Full Temperature Range and Worst Case Voltage Conditions)

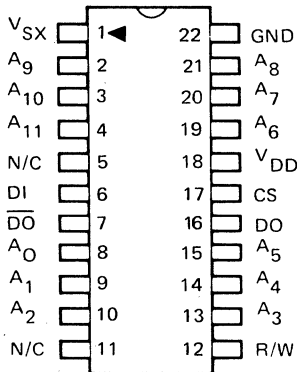
Characteristics	Symbol	Min	Typ	Max	Unit
Input Capacitance (except Chip Select) $V_I = 2.4V, V_{CS} = 12V$	C_I	-	6	-	pF
Chip Select Input Capacitance	C_{CS}	-	50	-	pF
Output Capacitance ($V_O = 2.0V, V_{CS} = 0V$)	C_O	-	5	-	pF



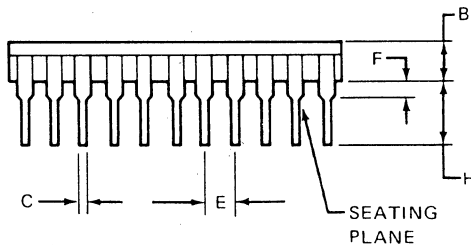
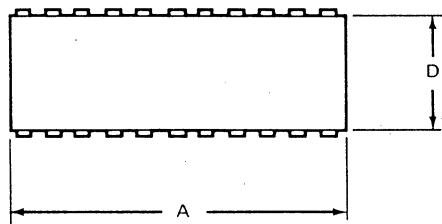
TIMING DIAGRAMS



TOP VIEW



PIN ASSIGNMENT



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	27.1	27.8	1.065	1.095
B	—	3.56	—	0.140
C	0.38	0.53	0.015	0.021
D	8.64	10.8	0.340	0.425
E	2.29	2.79	0.090	0.110
F	0.51	1.27	0.020	0.050
G	0.20	0.30	0.008	0.012
H	3.42	3.93	0.135	0.155
J	10.2 REF		0.4 REF	

PACKAGE DIMENSIONS



4096 x 1

SEMI 4402B

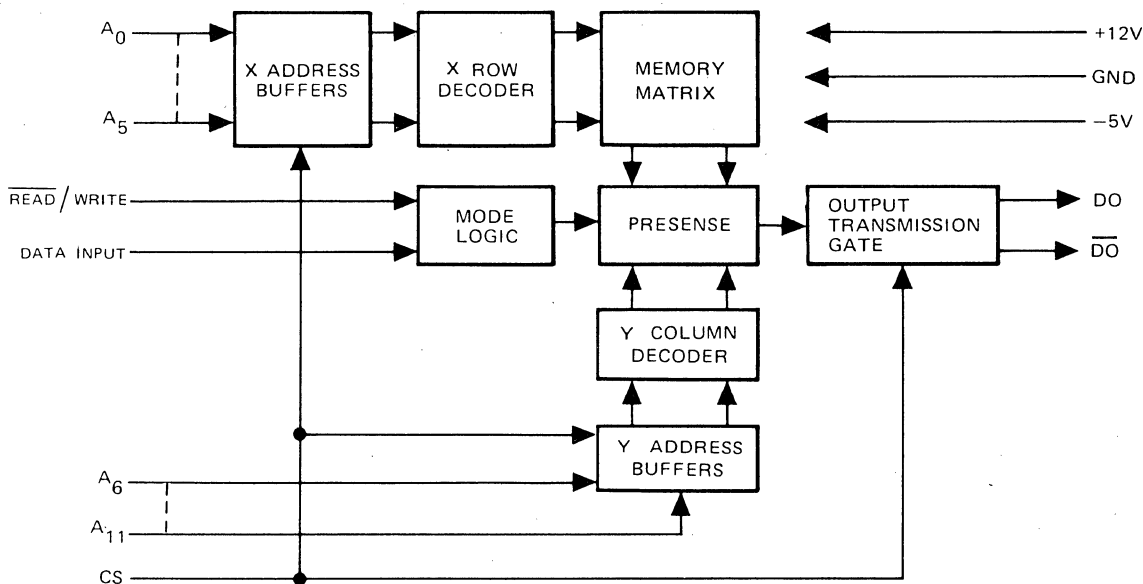
125 NSEC, STATIC, DIFFERENTIAL OUTPUT

N-MOS RAM

FEATURES

- STATIC – NO REFRESH OR CHARGE PUMP OSCILLATOR REQUIRED
- 4096 WORD x 1 BIT ORGANIZATION
- 125 NSEC ACCESS TIME
- 300 NSEC CYCLE TIME
- ON-CHIP ADDRESS REGISTER
- TTL COMPATIBLE ADDRESS AND DATA INPUTS
- LOW OPERATING POWER 400 MW TYP.
- DATA RETENTION TO $V_{DD} = 4V$
- STANDARD 22 PIN DIP, PIN AND VOLTAGE COMPATIBLE WITH POPULAR 4096 BIT DYNAMIC RAMS

BLOCK DIAGRAM



EMM/SEMI

MEMORY


ABSOLUTE MAXIMUM RATINGS (See Note 1) (Referenced to GND)

Rating	Symbol	Value	Unit
Supply Voltages	V _{DD}	-0.5 to +15	Vdc
	V _{SX}	+0.5 to -7	Vdc
Input & Output Voltages (except Chip Select)	V _I , V _O	V _{SX} to +15	Vdc
Chip Select Input Voltage	V _{CS}	V _{SX} to +15	Vdc
Power Dissipation	P _D	1.6 (Note 2)	W
Operating Ambient Temperature Range	T _{AMB}	0 to +70	°C
Storage Temperature Range	T _{STG}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Note 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMEND OPERATING CONDITIONS. Exposure to higher than recommended or maximum voltages for extended periods of time could affect device reliability.

Note 2: At 25°C ambient, Derate 13.5mw/°C.

RECOMMENDED OPERATING CONDITIONS T_A = 0°C to +70°C

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltages	V _{DD}	11.4	12	12.6	V
	V _{SX}	-4.5	-5	-5.5	V
Logic Levels:					
Input High Voltage (except Chip Select)	V _{IH}	3	-	5.25	V
Input Low Voltage (except Chip Select)	V _{IL}	0	-	0.7	V
Chip Select High Voltage	V _{CH}	V _{DD} -2	V _{DD}	V _{DD} +2	V
Chip Select Low Voltage	V _{CL}	0	-	0.5	V

DC ELECTRICAL CHARACTERISTICS (Full Operating voltage & temperature range unless otherwise noted)

Characteristics		Symbol	Min	Typ	Max	Unit
Input Current (except Chip Select)	V _{IH} = 5.0V (V _{CS} = V _{CH})	I _{IH}	-	5	25	μA
	V _{IL} = 0.5V (V _{CS} = V _{CH})	I _{IL}	-	-5	-25	μA
Chip Select High Input Current, DC (V _{CS} = 12V)		I _{CH}	-	2	3	mA
Chip Select High Input Current, (Pulse Peak) V _{CS} = 12V, T _{CR} = 25ns		I _{CP}	-	70	-	mA
Chip Select Low Input Current (V _{CS} = 5V)		I _{CL}	-	2	3	mA
Supply Current, (T _{AMB} = 25°C; V _{DD} , V _{SX} = nominal; all V _I = max V _{IL} : DO, D _O)	Unselected (Chip Select = 0 V)	I _{DDU} 25°C	-	1	5	mA
		I _{DDU} 70°C	-	3	15	mA
	Selected CSW 200ns Cycle = 350ns	I _{DD}	-	36	50	mA
		I _{SX}	-	-2	-3	mA
Standby Current at Reduced Voltages V _{DD} = 4V, V _{SX} = -4.5V, V _{CS} = 0V	25°C	I _{DDS}	-	.5	1.8	mA
	70°C	I _{DDS}	-	1.5	5.3	mA
Output Low Voltage	CSW ≤ 1μsec	V _{OL}	-	0	.1	V
Output High Voltage	CSW ≤ 1μsec	V _{OH}	.35	1	2	V
Output Disabled Current V _{CS} = 0V, V _O = 2V		I _{DO}	+10	-	-10	μA

AC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range Unless Otherwise Noted)

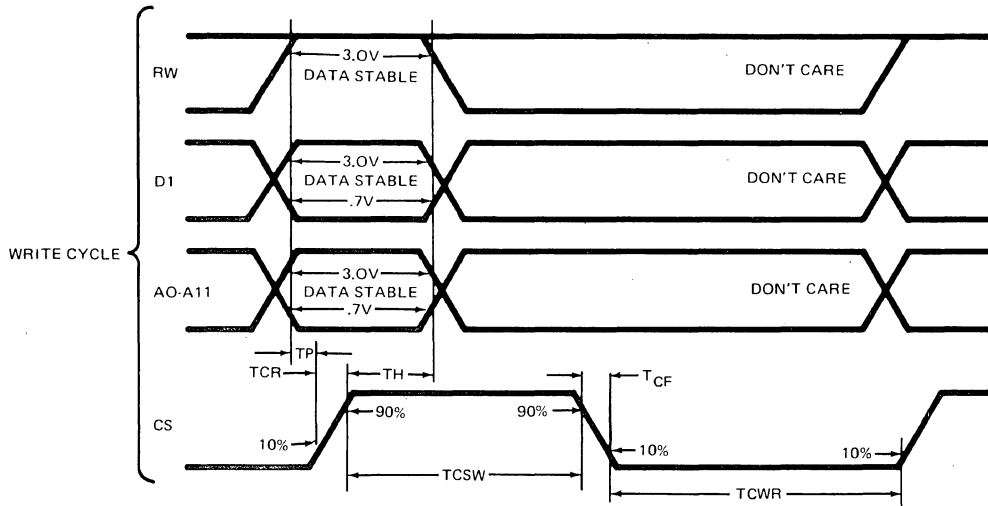
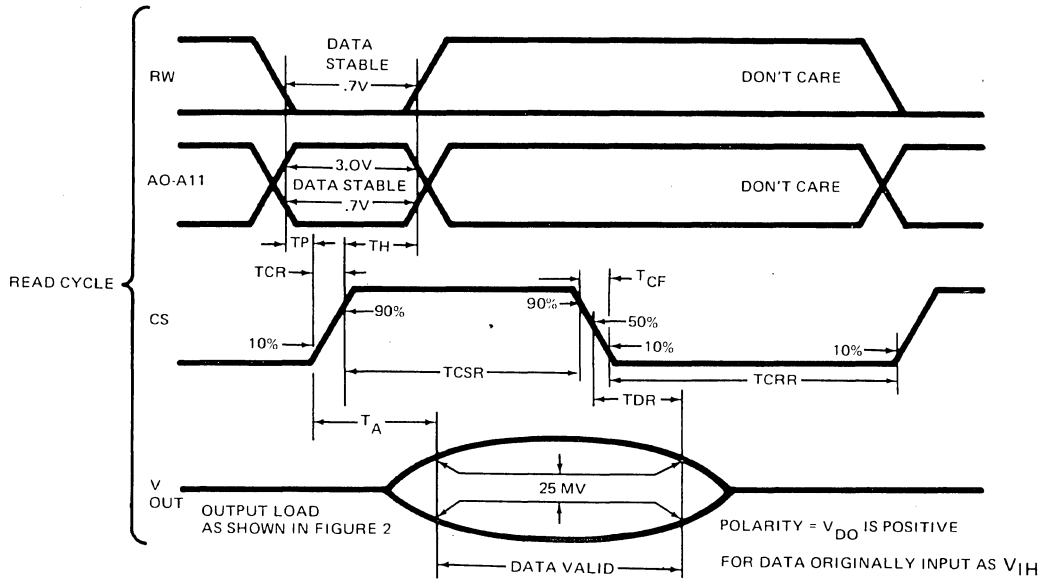
Characteristics	Symbol	Min	Typ	Max	Unit
Chip Select Read Pulse Width	T _{CSR}	125	-	∞	ns
Chip Select Read Recovery Time	T _{CRR}	135	-	∞	ns
Chip Select Write Pulse Width	T _{CSW}	125	-	∞	ns
Chip Select Write Recovery Time	T _{CWR}	135	-	∞	ns
Chip Select Rise Time	T _{CR}	-	10	50	ns
Chip Select Fall Time	T _{CF}	-	10	50	ns
Set Up Time	T _P	-	10	-	ns
Hold Time (Address and Data)	T _H	100	-	-	ns
Access Time (T _{CR} = 10ns)	T _A	-	-	125	ns
Cycle Time (Read or Write; T _{CR} = 10ns, T _{CF} = 10ns)	T _C	300	-	-	ns
Data Recovery	T _{DR}	10	15	-	ns

CAPACITANCE (Over Full Temperature Range and Worst Case Voltage Conditions)

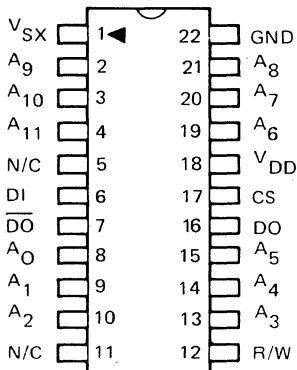
Characteristics	Symbol	Min	Typ	Max	Unit
Input Capacitance (except Chip Select) V _I = 2.4V, V _{CS} = 12V	C _I	-	6	-	pF
Chip Select Input Capacitance	C _{CS}	-	50	-	pF
Output Capacitance (V _O = 2.0V, V _{CS} = 0 V)	C _O	-	5	-	pF



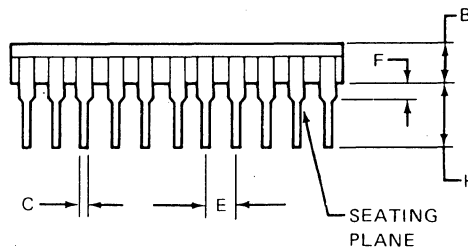
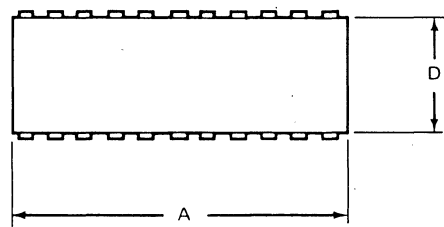
TIMING DIAGRAMS



TOP VIEW

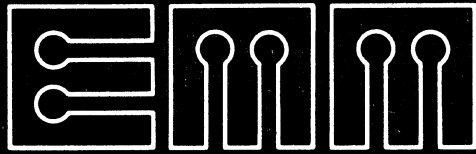


PIN ASSIGNMENT



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	27.1	27.8	1.065	1.095
B	—	3.56	—	0.140
C	0.38	0.53	0.015	0.021
D	8.64	10.8	0.340	0.425
E	2.29	2.79	0.090	0.110
F	0.51	1.27	0.020	0.050
G	0.20	0.30	0.008	0.012
H	3.42	3.93	0.135	0.155
J	10.2 REF		0.4 REF	

PACKAGE DIMENSIONS



4096x1

SEMI 4200 215 NSEC, STATIC, TTL OUTPUT N-MOS RAM

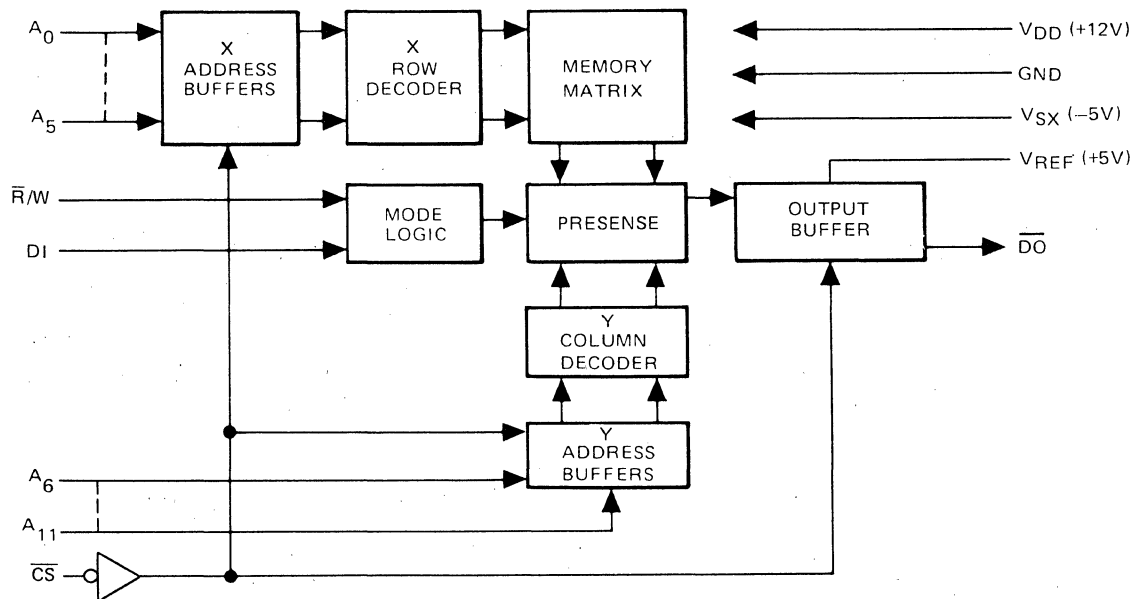
FEATURES

- COMPLETELY STATIC
- ACCESS TIME – 215 NSEC
- CYCLE TIME – 400 NSEC
- TYPICAL OPERATING POWER UNDER 450 mw.
- TYPICAL STANDBY POWER UNDER 35 mw.
- DATA RETENTION WITH LOW V_{DD}
- PIN AND VOLTAGE COMPATIBLE WITH STANDARD 22 PIN 4K DYNAMIC RAMS
- TTL COMPATIBLE TRI-STATE OUTPUTS
- FULLY DECODED
- ACTIVE LOW CHIP SELECT

EMM/SEMI

MEMORY

BLOCK DIAGRAM




ABSOLUTE MAXIMUM RATINGS (See Note 1) (Referenced to GND)

Rating	Symbol	Value	Unit
Supply Voltages	V _{DD}	-5 to +15	Vdc
	V _{RF}	-5 to +7	Vdc
	V _{SX}	+5 to -7	Vdc
Input & Output Voltages (Except Chip Select)	V _I , V _O	V _{SX} to +15	Vdc
Chip Select Input Voltage	V _{CS}	V _{SX} to +15	Vdc
Power Dissipation	P _D	1.6 (Note 2)	W
Operating Ambient Temperature Range	T _{AMB}	0 to +70	°C
Storage Temperature Range	-	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended or maximum voltages for extended periods of time could affect device reliability.

NOTE 2: At 25°C ambient. Derate 13.5m w/°C.

RECOMMENDED OPERATING CONDITIONS T_{AMB} = 0°C to 70°C

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V _{DD}	11.4	12.0	12.6	Vdc
Output Reference Voltage	V _{RF}	4.75	5.0	5.25	Vdc
Substrate Voltage	V _{SX}	-4.5	-5	-5.5	Vdc
Input High Level	V _{IH}	3	-	5.25	Vdc
Input Low Level	V _{IL}	0	-	0.8	Vdc
Chip Select High Level	V _{CH}	V _{DD} - 3	V _{DD}	V _{DD} + 3	Vdc
Chip Select Low Level	V _{CL}	0	-	0.5	Vdc

DC ELECTRICAL CHARACTERISTICS (Full Operating voltage & temperature range unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Input Current	I _{IN}	0	±10	±100	µA	V _{IN} = 0.5V or 5.0V
Chip Select Input Current	I _{CS}	-	±10	±100	µA	V _{CS} = 0.5V or 12V
Output "Low" Voltage	V _{OL}	-	0.3	0.5	Vdc	I _O = 2.0mA Fig. 5
Output "High" Voltage	V _{OH}	2.7	3.5	V _{RF}	Vdc	I _O = 500µA Fig. 5
Output Current (Unselected)	I _{DO}	-	-	-50	µA	V _{OL} = 2.7V, V _{CS} = +12V
Supply Current (Selected and Averaged over one cycle) CSW = 215 nsec TC = 400 nsec For Other Conditions, See Figure 3	I _{DD}	-	36	50	mA	V _{DD} = +12V V _{RF} = +5V V _{SX} = -5V T _{AMB} = 25°C
Supply Current (Unselected) T _{AMB} = 25°C	I _{DDU}	-	2	5	mA	V _{DD} = +12V V _{RF} = +5V V _{SX} = -5V V _{CS} = 12V
Supply Current (Unselected) T _{AMB} = 70°C	I _{DDU}	-	4.5	15	mA	
Substrate Current	I _{SX}	-	-2.2	-3	mA	
Reference Supply Current	I _{RF}	-	50	100	µA	
Standby Current at Reduced Voltages T _{AMB} = 25°C	I _{DDS}	-	0.8	2	mA	V _{CS} = 4V to 15V V _{DD} = 4V V _{SX} = -5V ±10% V _{RF} = 0V
Standby Current at Reduced Voltages T _{AMB} = 70°C	I _{DDS}	-	1.8	6	mA	

AC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range Unless Otherwise Noted)

Characteristics	Symbol	Min	Typ	Max	Unit	Figure
Chip Select Read Pulse Width	T _{CSR}	215ns	-	1ms	-	1
Chip Select Write Pulse Width	T _{CSW}	215ns	-	1ms	-	2
Chip Select Rise and Fall Time	T _{CR} , T _{CF}	-	10	50	ns	1&2
Set Up Time	T _p	0	-	-	ns	1&2
Access Time	T _A	-	-	215	ns	1
Cycle Time, T _{CR} = T _{CF} = 10ns (Read or Write)	T _C	400	-	-	ns	1&2
Data Hold Time	T _H	100	-	-	ns	1&2
Output Recovery Time	T _{DR}	10	15	-	ns	1
Read Recovery Time	T _{CRR}	150	-	-	ns	1
Write Recovery Time	T _{CWR}	150	-	-	ns	2

CAPACITANCE (Over Full Temperature Range and Worst Case Voltage Conditions)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Input Capacitance (Except Chip Select)	C _{IN}	-	6	-	pF	V _{IN} = 2.4V
Input Capacitance Chip Select	C _{CS}	-	20	-	pF	V _{CS} = 12V or 0V
Output Capacitance	C _O	-	8	-	pF	V _O = 2.7V V _{CS} = 12V

TIMING DIAGRAMS

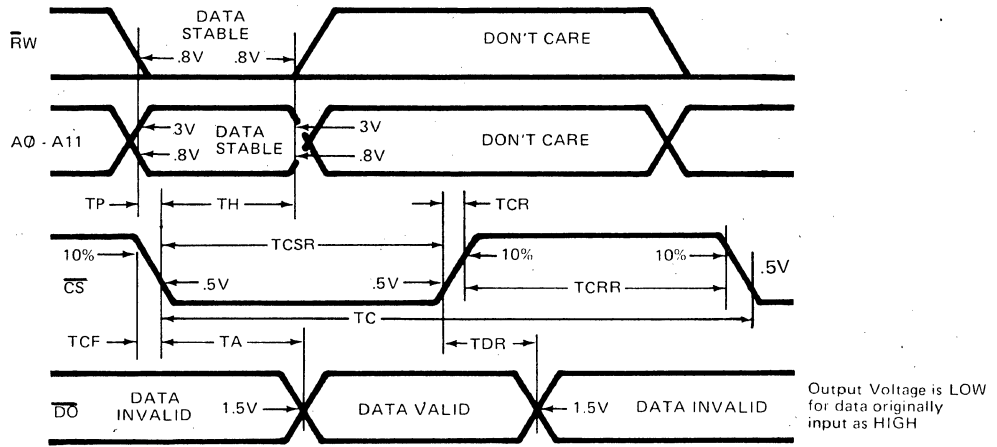


Figure 1 - Read Cycle

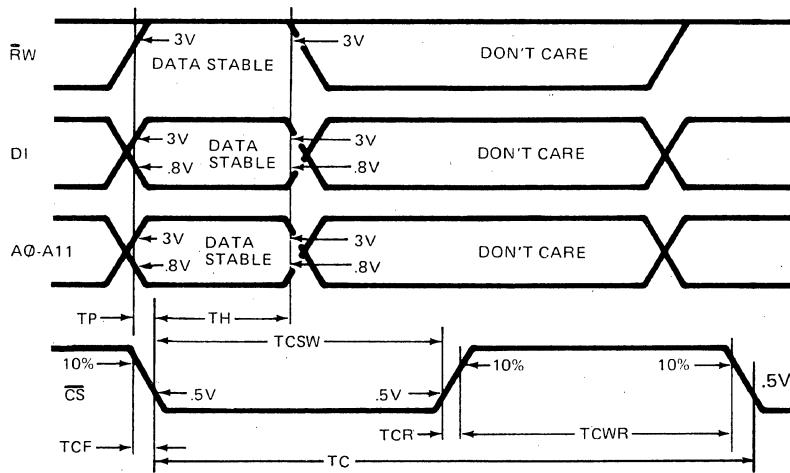
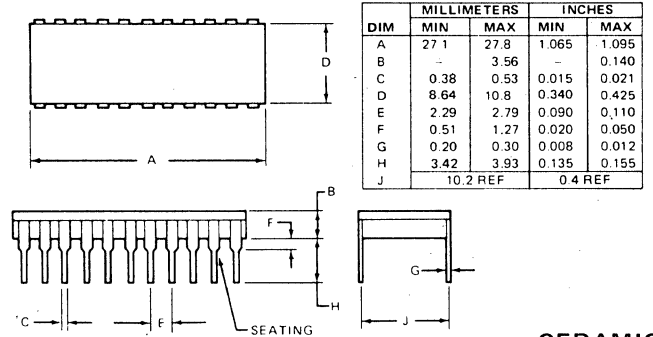
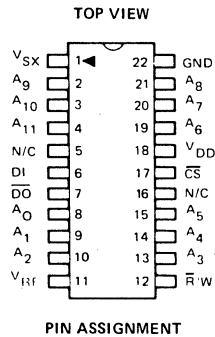


Figure 2 - Write Cycle

22 PIN DUAL IN-LINE

PIN	SYMBOL	FUNCTION
1	V _{SX}	Supply Voltage (-5V)
2	A ₉	Address Input
3	A ₁₀	Address Input
4	A ₁₁	Address Input
5	N/C	
6	D ₁	Data In
7	D ₀	Data Out
8	A ₀	Address Input
9	A ₁	Address Input
10	A ₂	Address Input
11	V _{RF}	Supply Voltage (5V)
12	R/W	Read/Write Input
13	A ₃	Address Input
14	A ₄	Address Input
15	A ₅	Address Input
16	N/C	
17	CS	Chip Select
18	V _{DD}	Supply Voltage (12V)
19	A ₆	Address Input
20	A ₇	Address Input
21	A ₈	Address Input
22	GND	Ground



CERAMIC PACKAGE DIMENSIONS



1024x4

SEMI 4104

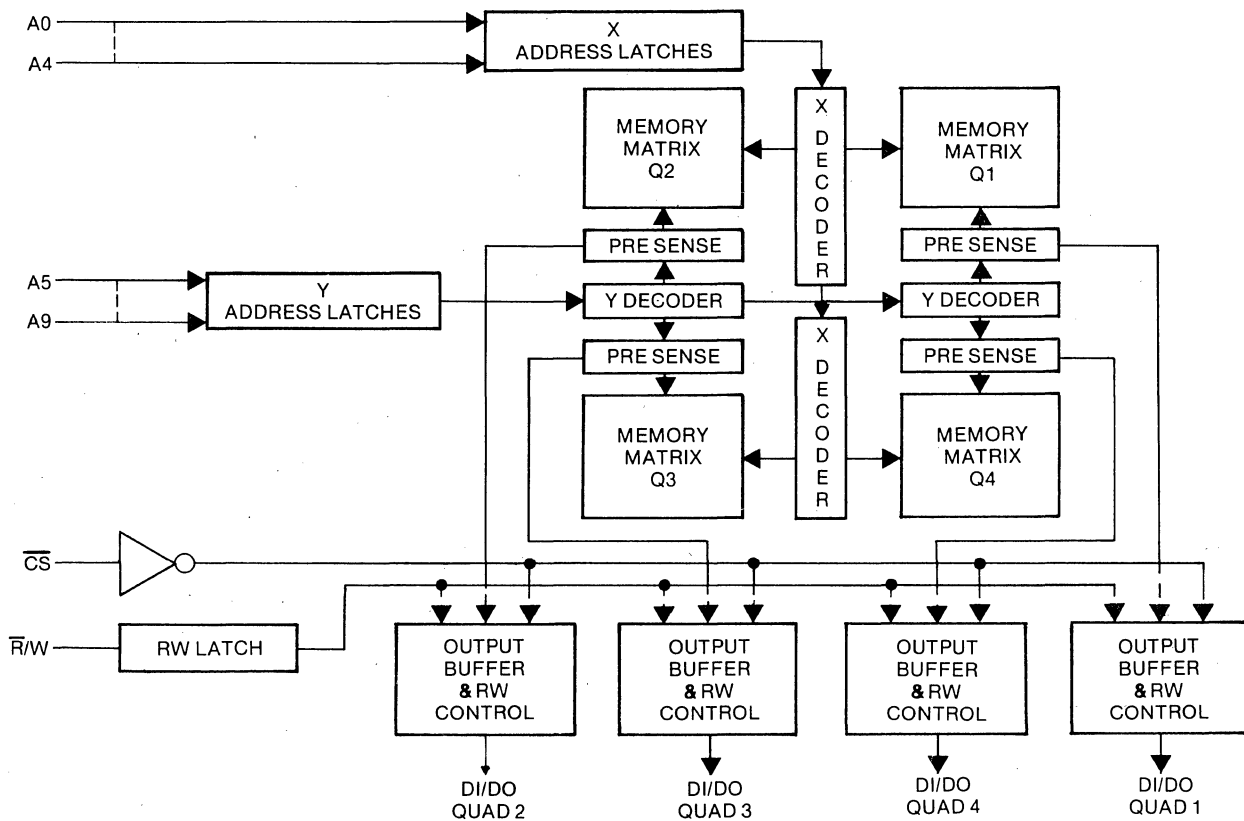
225 NSEC STATIC TTL OUTPUT

N-MOS RAM

FEATURES

- COMPLETELY STATIC
- ACCESS TIME – 225 NSEC
- CYCLE TIME – 400 NSEC
- TYPICAL OPERATING POWER UNDER 500 mw.
- TYPICAL STANDBY POWER UNDER 40 mw.
- DATA RETENTION WITH LOW V_{DD}
- TTL COMPATIBLE INPUTS
- ACTIVE LOW CHIP SELECT
- TRI-STATE OUTPUTS
- COMMON I/O BUSS

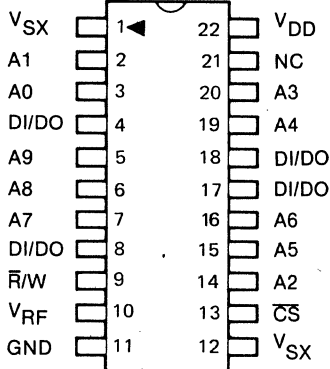
BLOCK DIAGRAM



EMM/SEMI
MEMORY

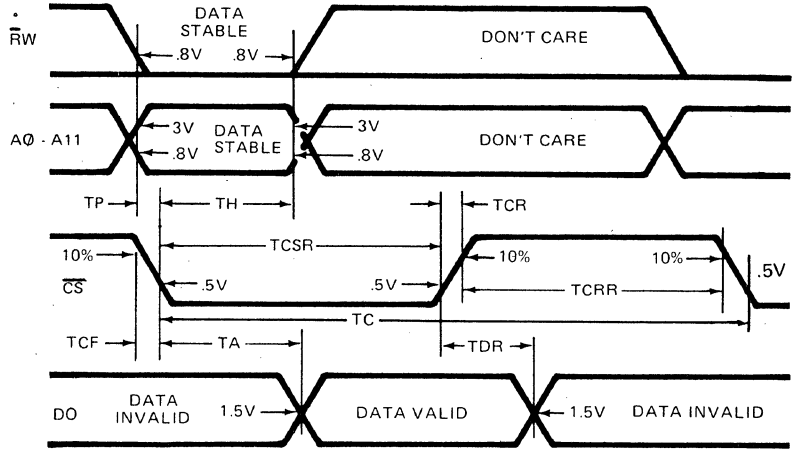


TOP VIEW



PIN ASSIGNMENT

TIMING DIAGRAM



Read Cycle

DYNAMIC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, Full Voltage Range

Chip Select Read Pulse Width	225ns min
Chip Select Write Pulse Width	225ns min
Chip Select Rise and Fall Time	50ns max
Set Up Time	0ns min
Access Time	225ns max
Cycle Time	400ns max
Data Hold Time	100ns min
Output Recovery Time	10ns min
Read Recovery Time	150ns min
Write Recovery Time	150ns min

MAXIMUM RATINGS

Supply Voltage	11.4 to 12.6 Vdc
Output Reference Voltage	4.75 to 5.25 Vdc
Substrate Voltage	-4.5 to -5.5 Vdc
Operating Temperature Range	0°C to 70°C
Input High Level	3.0 to 5.25 Vdc
Input Low Level	0.0 to 0.8 Vdc

EMM/SEMI

MEMORY



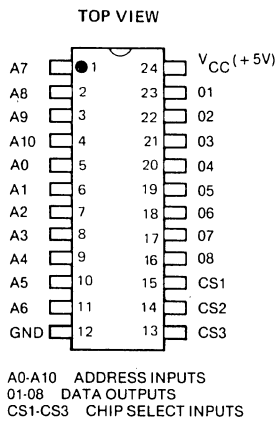
SEMI R0-3-8316A

16384 BIT STATIC NMOS ROM

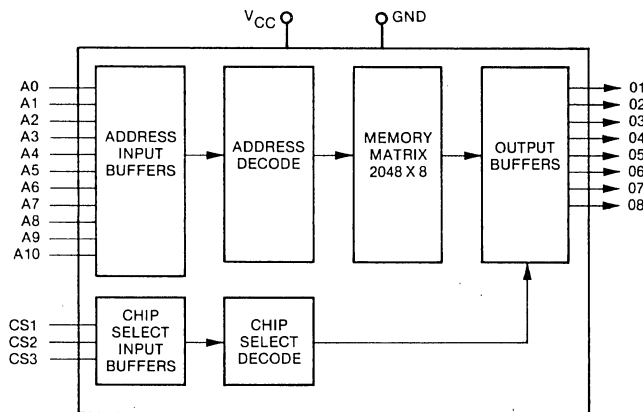
FEATURES

- 2048 X 8 Organization - ideal for microprocessor memory systems.
- Single + 5 Volt Supply.
- TTL Compatible - all inputs and outputs.
- Static Operation - no clocks required.
- 850ns Maximum Access Time.
- 200 mW Typical Power.
- Three-State Outputs - under the control of three mask-programmable Chip Select inputs to simplify memory expansion.
- Totally Automated Custom Programming.
- Zener Protected Inputs.
- Glass Passivation Protection.

PIN CONFIGURATION



BLOCK DIAGRAM



MAXIMUM RATINGS*

V_{CC} and input voltages (with respect to GND) -0.3V to +8.0V
 Storage temperature -65°C to +150°C
 Operating temperature 0°C to +70°C

*Exceeding these ratings could cause permanent damage to this device. Functional operation at these conditions is not implied - operating conditions are specified below.

ELECTRICAL CHARACTERISTICS

Standard conditions: V_{CC} = + 5 volts ±5%
 (unless otherwise noted) Temperature (TA) = 0°C to +70°C
 Output Loading: One TTL load, CL total = 30 pF.

DC CHARACTERISTICS	SYMBOL	MIN.	TYP. ¹	MAX.	UNITS	CONDITIONS
ADDRESS, CHIP SELECT INPUTS						
Logic "1"	V _{IH}	2.2	—	—	V	
Logic "0"	V _{IL}	—	—	0.65	V	
Leakage	I _{LI}	—	—	10	μA	
DATA OUTPUTS						
Logic "1"	V _{OH}	2.2	—	—	V	I _{OH} = 100 μA
Logic "0"	V _{OL}	—	—	0.45	V	I _{OL} = 1.9 mA
Leakage	I _{LO}	—	—	10	μA	
POWER SUPPLY CURRENT						
I _{CC}	—	—	40	66	mA	Outputs open

AC CHARACTERISTICS	SYMBOL	MIN.	TYP. ¹	MAX.	UNITS	CONDITIONS
ADDRESS, CHIP SELECT INPUTS						
Cycle Time	t _c	800	—	—	ns	f = 1MHz
Capacitance	C _I	—	5	8	pF	
DATA OUTPUTS						
Access Time	t _{acc}	—	600	850	ns	
Chip Select Response Time	t _R	—	200	300	ns	
Capacitance	C _o	—	8	10	pF	f = 1MHz

NOTE: 1. Typical values are at + 25°C and nominal voltages.

EMM/SEMI

MEMORY



HM-76XX

GENERIC PROM FAMILY

Harris/Semiconductor

MEMORY

ORGANIZATIONS			DESCRIPTION
<u>PART NO.</u>	<u>TOTAL BITS</u>	<u>WORDS x BITS PER WORD</u>	<p>The HM-76XX Generic PROM's comprise a completely compatible family having common D. C. electrical characteristics and identical programming requirements. They are fully decoded, high speed, field programmable ROM's and are available in all commonly used organizations, with both open-collector and three-state outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for a logical "0" (outputs low).</p> <p>The nichrome fuse technology is the same as is used in the JAN approved MIL 38510/201 PROM, and in all other Harris PROM's.</p> <p>The field programmable PROM can be custom programmed to any pattern using a simple programming procedure. Schottky Bipolar circuitry provides fast access time, and features temperature and voltage compensation to minimize access time variations.</p> <p>All pinouts are compatible to industry standard PROM's and ROM's.</p> <p>In addition to the conventional storage array, extra test rows and test columns are included to assure high programmability, and guarantee parametric and A. C. performance. Fuses in these test rows and columns are blown prior to shipment.</p>
HM-7602 (OC) -7603 (TS)	256	32 x 8	
HM-7610 (OC) -7611 (TS)	1024	256 x 4	
HM-7620 (OC) -7621 (TS)	2048	512 x 4	
HM-7640 (OC) -7641 (TS)	4096	512 x 8	
<p>* OC-Open-Collector Output * TS-Three-State Output</p>			
FEATURES			
<ul style="list-style-type: none"> Common D. C. Electrical Characteristics and Programming Procedure Simple, High Speed Programming Procedure (1 second per 1024 Bits) Expandable - "Open-Collector" or "Three-State" Outputs and Chip Enable Inputs Inputs and Outputs TTL Compatible <ul style="list-style-type: none"> ▶ Low Input Current-400 μA Logic "0", 40 μA Logic "1" ▶ Full Output Drive-15mA Sink, 2mA Source Fast Access Time-Guaranteed Over Commercial and Military Temperature and Voltage Ranges Pin Compatible With Industry Standard PROM's and ROM's 			

PACKAGES

HM-7602/7603, HM-7610/7611, HM-7620/7621

16 LEAD D. I. P. *

HM-7640/7641

24 LEAD D. I. P. *

ALL DIMENSIONS IN INCHES.
ALL DIMENSIONS \pm .010 UNLESS OTHERWISE SHOWN.

* Also Available in Flatpacks



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	7.0V
Supply Current	600mA
Address/Enable Input Voltage	5.5V
Address/Enable Input Current	-20mA
Output Sink Current	70mA
Storage Temperature	+ 150°C
Operating Temperature (Ambient)	+ 125°C
Maximum Junction Temperature	+ 175°C

Stresses above those listed under the "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

ELECTRICAL CHARACTERISTICS (OPERATING) HM-76XX-5 ($V_{CC} = 5.0V \pm 5\%$, $T_A = 0^\circ C$ to $70^\circ C$) HM-76XX-2, HM-76XX-8 ($V_{CC} = 5.0V \pm 10\%$, $T_A = -55^\circ C$ to $125^\circ C$)

D. C.

PARAMETER	SYMBOL	OPEN-COLLECTOR OUTPUT			THREE-STATE OUTPUT			UNITS	TEST CONDITIONS	
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			
Address/Enable Input Current	"1" "0"	I_{RA}/I_{FA} I_{RE}/I_{FE}	-0.1	*40 *-0.4		-0.1	*40 *-0.4	μA mA	$V_{IH}=V_{CC}$ Max $V_{IL}=0.45V$	
Input Threshold Voltage	"1" "0"	V_{IH} V_{IL}	2.0		2.0		0.8	V	$V_{CC}=V_{CC}$ Min $V_{CC}=V_{CC}$ Max	
Output Voltage	"1" "0"	V_{OH} V_{OL}	N/A	0.35	*2.4	3.4	0.35	V	$I_{OH}=-2.0mA, V_{CC}=V_{CC}$ Min $I_{OL}=+15mA, V_{CC}=V_{CC}$ Min	
Output Disabled Current	"1" "0"	I_{OH} I_{OL}		*100 N/A			*100 *-100	μA μA	$V_{OH}, V_{CC}=V_{CC}$ Max $V_{OL}=+0.3V, V_{CC}=V_{CC}$ Max	
Output Leakage	"1"	I_{OH}		*100			N/A	μA	$V_{OH}, V_{CC}=V_{CC}$ Max	
Input Clamp Voltage		V_{CL}		*-1.5			*-1.5	V	$I_{in} = -10mA$	
Output Short Circuit Current		I_{OS}	N/A	N/A	*15	23	30	mA	$V_{CC}=V_{CC}$ Max, $V_{OUT}=0.0V$ One output only for a Max of 1 sec	
Power Supply Current		I_{CC}		90	*130		90	*130	mA	$V_{CC}=V_{CC}$ Max All Inputs Grounded
				125	*170		125	*170	mA	

Typical Measurements at $T_A = 25^\circ C$, $V_{CC} = +5.0V$.

$\dagger I_{FE}$ Max. = -1.6mA, CS_3 and CS_4 Inputs (HM-7640/41 only).

*100% Tested for Dash 8.

A. C.

	SYMBOL	$V_{CC} = 5V \pm 5\%$		$V_{CC} = 5V \pm 10\%$		UNITS	TEST CONDITIONS
		$T_A = 0^\circ C$ to $70^\circ C$		$T_A = -55^\circ C$ to $125^\circ C$			
		TYP.	MAX.	TYP.	MAX.		
HM-7602/7603	T_{AA}	35	40	35	50	nS	V_{CC} and T_A Over Full Range
	T_{EA}	20	30	20	40		
HM-7610/7611	T_{AA}	40	60	40	75		
	T_{EA}	15	25	15	30		
HM-7620/7621	T_{AA}	45	70	45	85		
	T_{EA}	15	25	15	30		
HM-7640/7641	T_{AA}	48	70	48	85		
	T_{EA}	30	40	30	50		

T_{AA} - Address to Output Access Time.
 T_{EA} - Chip Enable Access Time.

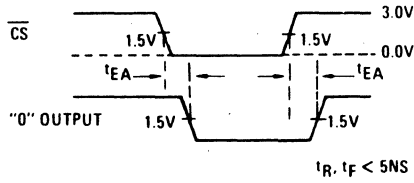
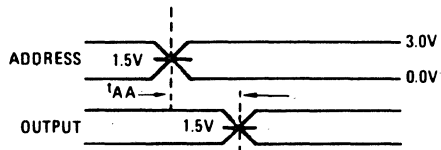
CAPACITANCE (1): $T_A = 25^\circ C$

PARAMETER	SYMBOL	TYP.	UNITS	TEST CONDITION
Add. Input Cap.	C_{INA}, C_{INCS}	8	pF	$V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz$
Output Cap.	C_{OUT}	8	pF	$V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz$

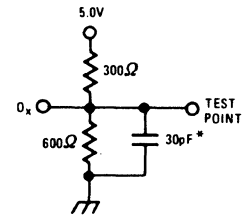
NOTE: (1) These parameters are only periodically sampled and are not 100% tested.



SWITCHING TIME DEFINITIONS



A.C. TEST LOAD



*Includes jig & probe total capacitance

PROGRAMMING

The Generic PROM's are manufactured with all bits/outputs Logical "1" (Output High). Any desired bit/output can be programmed to a Logical "0" (Output Low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in Table 1, or buy any of the commercially available programmers which meet these specifications. These PROM's can be programmed automatically or by the manual procedure shown below.

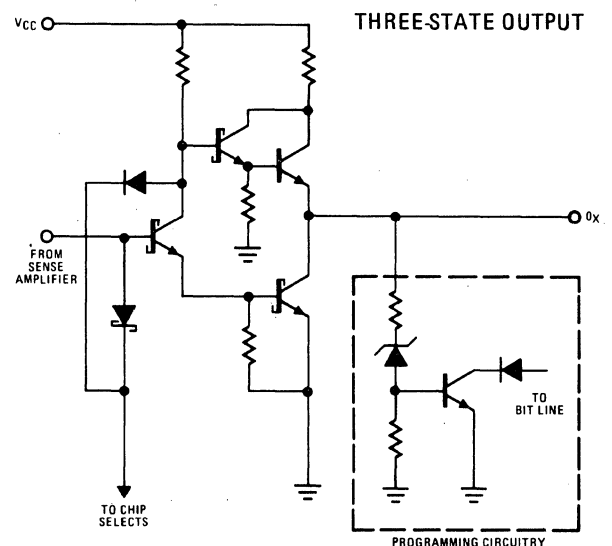
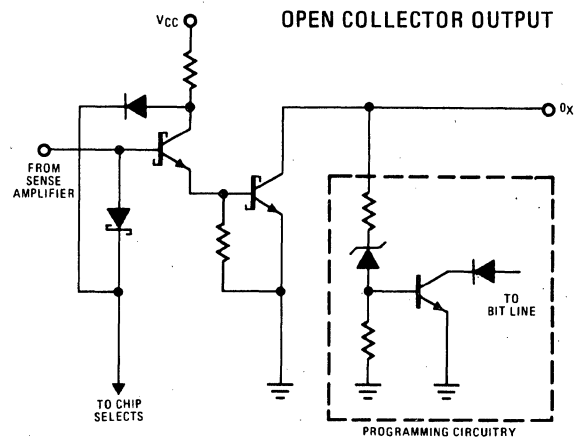
PROGRAMMING SPECIFICATIONS

TABLE 1

PARAMETER	SYMBOL	MIN.	RECOM-MEND VALUE	MAX.	UNITS
Address Input Voltage (1)	V_{IH}	2.4	5.0	5.0	V
	V_{IL}	0.0	0.4	0.8	V
Programming/Verify Voltage to V_{CC} (2)	V_{PH}	11.5	12.0	12.5	V
	V_{PL}	3.75	4.0	5.25	V
Programming Voltage Current Limit	I_{CCP}			600	mA
Programming (V_{CC}) Voltage Rise and Fall Time	t_r	1	1	10	μs
	t_f	1	1	10	μs
Programming Delay	t_d	10	10	100	μs
Programming Pulse Width - First Attempts	t_{p1}	100	100	200	μs
	t_{p2}	10	10	20	ms
Programming Duty Cycle	D.C.	-	10	50	%
Output Voltage Enable	V_{OPE}	9.5	10.0	10.5	V
Disable (3)	V_{OPD}	0	.45	5.5	V
Output Voltage Enable Current Limit	I_{OPE}			10	mA
Case Temp	T_C		25	75	$^{\circ}C$

1. Address and chip select should not be left open for V_{IH} .
2. Verification at $V_{CC} = 4.0 \pm .25$ Volts, $T_A = 25^{\circ}C$ is recommended to guardband performance over full temperature and voltage range.
3. Disable condition will be met with output open circuit.

SCHEMATIC DIAGRAMS





PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible. An open circuit should not be used to address the PROM.
2. Disable the chip by applying input highs (V_{IH}) to the \overline{CS} input(s). CS inputs (HM-7640/41 only) must remain at V_{IH} for program and verify. The chip select is TTL compatible. An open circuit should not be used to disable the chip.
3. Disable the programming circuitry by applying an Output Voltage Disable of less than V_{OPD} to the output of the PROM. The output may be left open circuit to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time equal to t_r .
5. After a delay equal to or greater than t_d , apply a pulse with amplitude equal to V_{OPE} and duration of t_{p1} to the output selected for programming. Note that the PROM is supplied with fuses intact generating an output high. Programming a fuse will cause the output to go low in the verify mode.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d .
7. Lower V_{CC} to $4.0 \pm .25$ Volts following a delay of t_d from the last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying a logic "0" (V_{IL}) to the \overline{CS} input(s).
9. If any bit does not verify as programmed, repeat steps 2 through 8 using an output enable pulse width of t_{p1} for up to 15 additional pulses to enhance programming speed. If the bit is still unprogrammed, follow with at least 16 repetitive pulses of t_{p2} in width, to achieve high programming yield. In the event that the bit is still unprogrammed, the part is considered a programming reject and should be returned to the factory. The address and incorrect and desired contents of a location in which a programming failure has occurred in any returned device must be included with that return.
10. Repeat steps 1 through 9 for all other bits to be programmed in the PROM.

RECOMMENDED PROGRAMMING CIRCUIT

The circuit and timing diagram shown in Figures 1 and 2 will establish the proper programming condition for the output enable pulse. This allows the use of standard TTL parts for all logic inputs to the PROM. Note the gate which senses the output must be input protected to withstand input up to 12.5 Volts during programming.

FIGURE 1

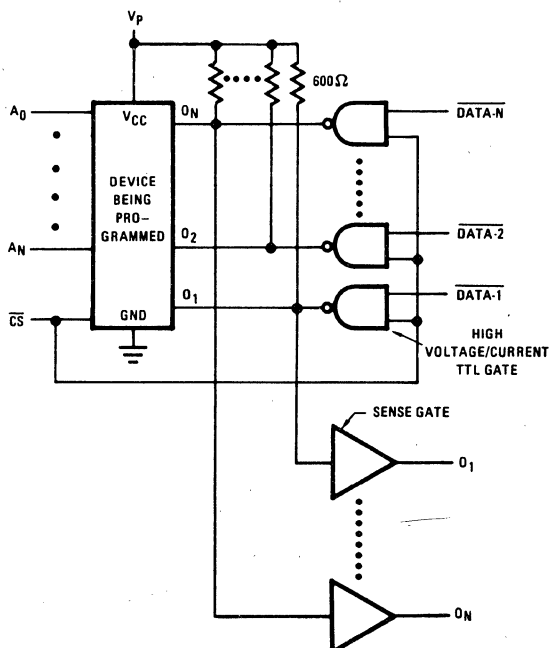
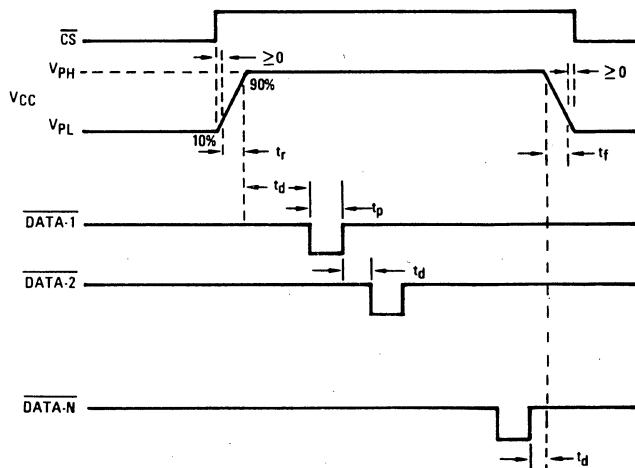


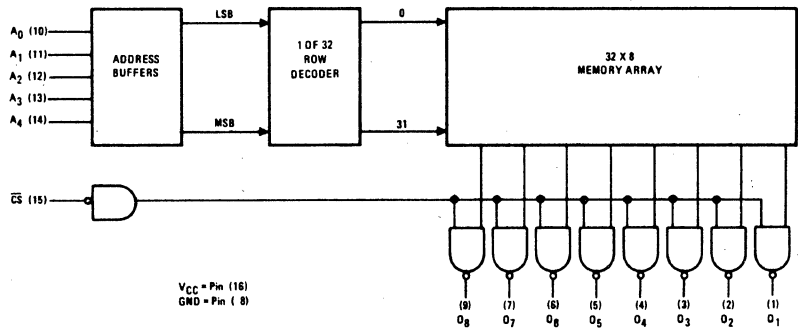
FIGURE 2



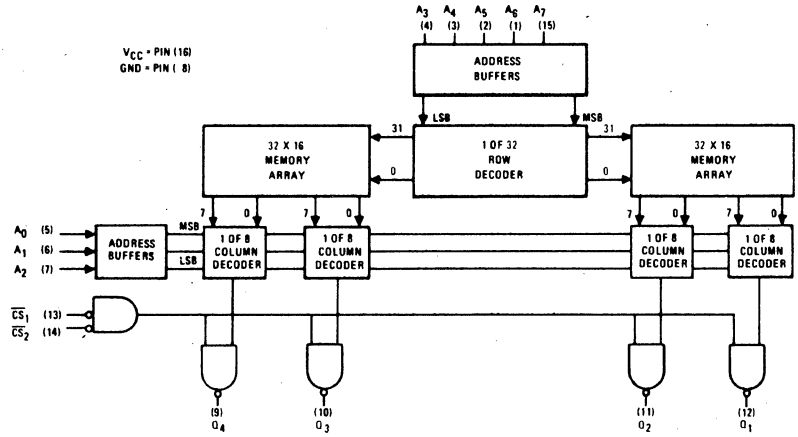


BLOCK DIAGRAMS

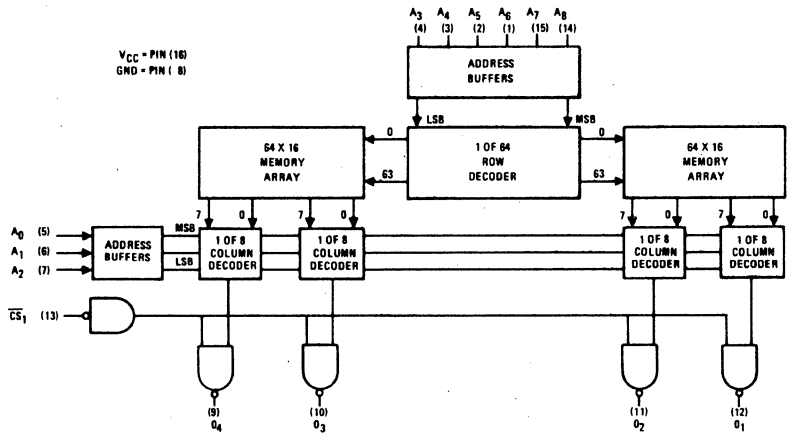
HM-7602/03 32 X 8



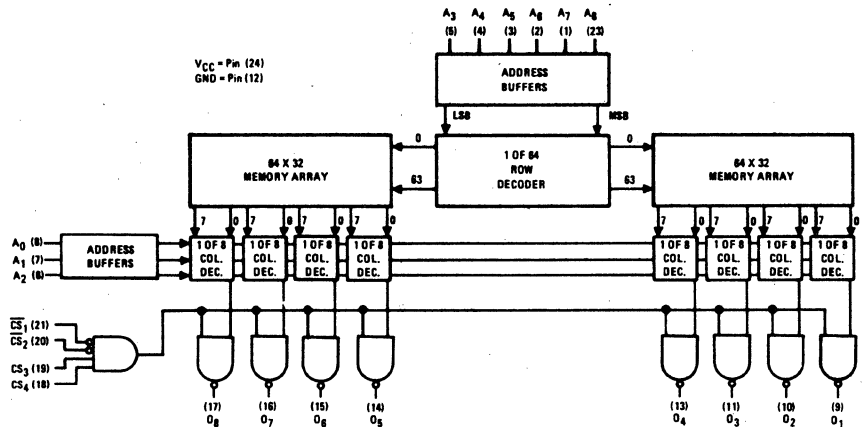
HM-7610/11 256 X 4



HM-7620/21 512 X 4



HM-7640/41 512 X 8



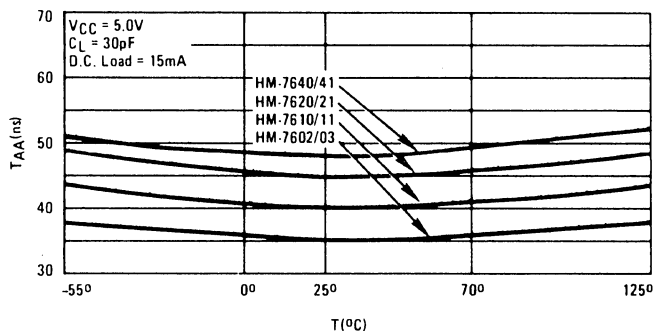
Harris/Semiconductor

MEMORY

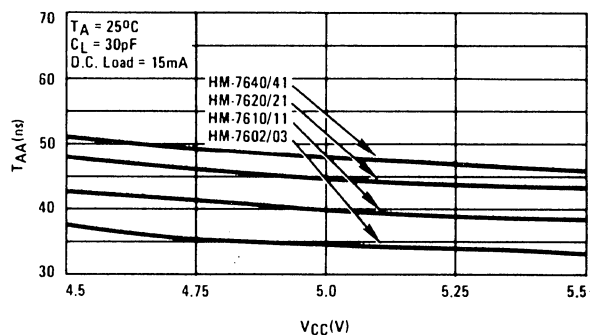


TYPICAL A.C. CHARACTERISTICS

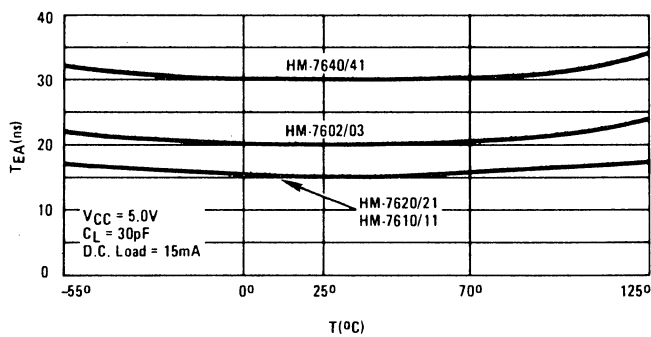
ADDRESS TO OUTPUT DELAY VS. TEMPERATURE



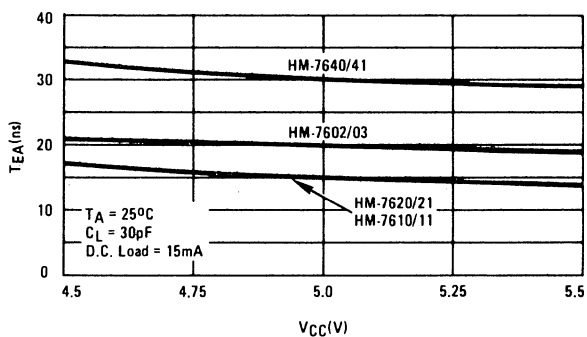
ADDRESS TO OUTPUT DELAY VS. SUPPLY VOLTAGE



CHIP SELECT TO OUTPUT DELAY VS. TEMPERATURE



CHIP SELECT TO OUTPUT DELAY VS. SUPPLY VOLTAGE



Harris/Semiconductor

MEMORY

SALES OFFICES-

SUITE 103
4014 LONG BEACH BLVD.
LONG BEACH, CALIF. 90807
(213) 426-7687

SUITE 230
1032 ELWELL COURT
PALO ALTO, CALIF. 94303
(415) 964-8443

SUITE 100
15 SPINNING WHEEL ROAD
HINSDALE, ILL. 60521
(312) 325-4242

SUITE 301
177 WORCESTER STREET
WELLESLEY HILLS, MASS. 02181
(617) 237-5430

SUITE 132
7710 COMPUTER AVENUE
MINNEAPOLIS, MINN. 55435
(612) 835-2505

3215 E. MAIN STREET
ENDWELL, N. Y. 13760
(607) 754-5464

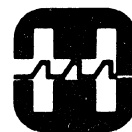
535 BROADHOLLOW ROAD
MELVILLE, L. I., N. Y. 11746
(516) 249-4500

SUITE 220
333 WEST FIRST STREET
DAYTON, OHIO 45402
(513) 226-0636

SUITE 325
650 E. SWEDES FORD ROAD
WAYNE, PENN. 19087
(215) 687-6680

SUITE 7G
777 S. CENTRAL EXPRESSWAY
RICHARDSON, TEXAS 75080
(214) 231-9031

P. O. BOX 883
MELBOURNE, FL. 32901
(305) 724-7430
TWX-510-959-6259



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Silicon Gate MOS 2104

HIGH DENSITY RANDOM ACCESS 4096 BIT DYNAMIC MEMORY

- * Access Time—350 ns Max.
- * Read, Write Cycle Times—500 ns Max.
- * Refresh Period—2 ms

- Highest Density 4K RAM—
Industry Standard 16 Pin Package
- Low Standby Power
- All Inputs Including Clocks
TTL Compatible
- Standard Power Supplies +12V,
+5V, -5V
- Read-Modify-Write Cycle Time—
700 ns
- On-Chip Latches for Addresses,
Chip Select and Data In.
- Simple Memory Expansion—
Chip Select
- Output is Three State, TTL
Compatible; Data is Latched
and Valid into Next Cycle

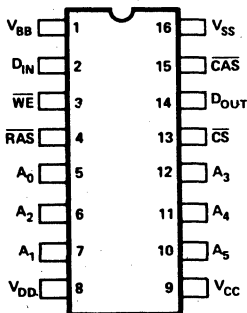
The Intel[®] 2104 is a 4096 word by 1 bit MOS RAM fabricated with N-channel silicon gate technology for high performance and high functional density. The 2104 uses a single transistor dynamic storage cell and dynamic circuitry to achieve high speed and low power dissipation.

The unique design of the 2104 allows it to be packaged in the industry standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

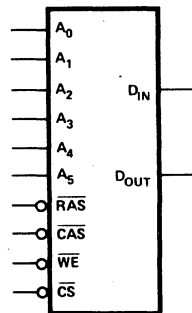
The use of the 16 pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the 2104 on 6 address input pins. The two 6 bit address words are latched into the 2104 by the two TTL clocks, Row Address Strobe (RAS) and Column Address Strobe (CAS). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

The single transistor dynamic storage cell provides high speed along with low power dissipation. The memory cell requires refreshing for data retention. Refreshing is most easily accomplished by performing a read cycle at each of the 64 row addresses every 2 milliseconds.

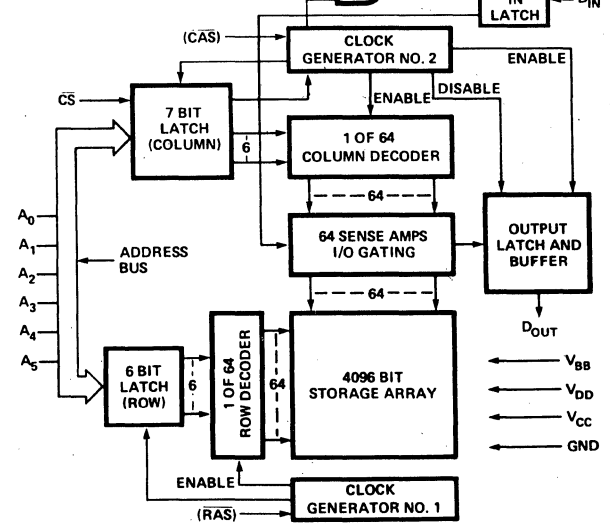
PIN CONFIGURATION



LOGIC DIAGRAM



BLOCK DIAGRAM



PIN NAMES

A ₀ - A ₅	ADDRESS INPUTS	WE	WRITE ENABLE
CAS	COLUMN ADDRESS STROBE	V _{BB}	POWER (-5V)
CS	CHIP SELECT	V _{CC}	POWER (+5V)
D _{IN}	DATA IN	V _{DD}	POWER (+12V)
D _{OUT}	DATA OUT	V _{SS}	GROUND
RAS	ROW ADDRESS STROBE		

Absolute Maximum Ratings*

Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB}	+25V to -0.3V
Supply Voltages V_{DD} , V_{CC} , and V_{SS} with Respect to V_{BB}	+20V to -0.3V
Power Dissipation	1.25W

***COMMENT:**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics [1]

$T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = +12\text{V} \pm 5\%$, $V_{CC} = +5\text{V} \pm 10\%$, $V_{BB} = -5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise noted.

Symbol	Parameter	Limits		Unit	Conditions
		Min.	Typ.[2]		
I_{LI}	Input Load Current (any input)			10	μA $V_{IN} = V_{IL\text{ MIN}}$ to $V_{IH\text{ MAX}}$
$ I_{LO} $	Output Leakage Current for high impedance state			10	μA Chip deselected.
$I_{DD1}^{[3]}$	V_{DD} Supply Current		1	2	mA $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ at V_{IH} . Chip deselected.
$I_{DD\text{ AV}}^{[3]}$	Average V_{DD} Current		45	59	mA Cycle time=500ns, $t_{RP} = 150\text{ns}$ $T_A = 25^\circ\text{C}$
$I_{CC1}^{[4]}$	V_{CC} Supply Current when deselected			10	μA
$I_{BB}^{[3]}$	Average V_{BB} Current			75	μA
V_{IL}	Input Low Voltage (any input)	-1.0		0.6	V
V_{IH}	Input High Voltage (any input)	2.4		$V_{CC}+1$	V
V_{OL}	Output Low Voltage	0.0		0.4	V $I_{OL} = 2.0\text{mA}$
V_{OH}	Output High Voltage	2.4		V_{CC}	V $I_{OH} = -5.0\text{mA}$

A.C. Characteristics [1]

$T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 12\text{V} \pm 5\%$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{BB} = -5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise noted.

Capacitance [5] $T_A = 25^\circ\text{C}$

Symbol	Test	Plastic And Ceramic Pkg.		Unit	Conditions
		Typ.	Max.		
C_{AD}	Address Capacitance		10	pF	$V_{IN} = V_{SS}$
C_C	$\overline{\text{CAS}}$, $\overline{\text{RAS}}$, $\overline{\text{CS}}$ Capacitance		7	pF	$V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance		8	pF	$V_{OUT} = 0\text{V}$
C_{IN}	D_{IN} and $\overline{\text{WE}}$ Capacitance		10	pF	$V_{IN} = V_{SS}$

- Notes:
1. All voltages referenced to V_{SS} . The only requirement for the sequence of applying voltages to the device is that V_{DD} , V_{CC} , and V_{SS} should never be 0.3V or more negative than V_{BB} .
 2. Typical values are for $T_A = 25^\circ\text{C}$ and nominal power supply voltages.
 3. The I_{DD} current flows to V_{SS} . The I_{BB} current is the sum of all leakage currents.
 4. When chip is selected V_{CC} supply current is dependent on output loading; V_{CC} is connected to output buffer only.
 5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:

$$C = \frac{I\Delta t}{\Delta V} \text{ with the current equal to a constant } 20\text{mA.}$$

A.C. Characteristics ^[1] $T_A=0^\circ\text{C}$ to 70°C , $V_{DD}=12\text{V} \pm 5\%$, $V_{CC}=5\text{V} \pm 10\%$, $V_{BB}=-5\text{V} \pm 10\%$, $V_{SS}=0\text{V}$, unless otherwise noted.

READ, WRITE, AND READ MODIFY WRITE CYCLES ^[3]

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		2	ms	
t_{RP}	$\overline{\text{RAS}}$ Precharge Time	150		ns	
t_{RCL}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Leading Edge Lead Time	110	2000	ns	See Note 2
t_{AS}	Address or $\overline{\text{CS}}$ Set-up Time	0		ns	
t_{AH}	Address or $\overline{\text{CS}}$ Hold Time	100		ns	
t_{AR}	$\overline{\text{RAS}}$ to Address Hold Time	250		ns	
t_{CRL}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Trailing Edge Lead Time	-10	+90	ns	Measured from $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$
t_{OFF}	Output Buffer Turn Off Delay	0	100	ns	
t_{CAC}	Access Time From $\overline{\text{CAS}}$		200	ns	1 TTL Load, $C_L = 50\text{pF}$, See Note 2
t_{RAC}	Access Time From $\overline{\text{RAS}}$		350	ns	1 TTL Load, $C_L = 50\text{pF}$, See Note 2

READ CYCLE ^[3]

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{CYC}	Random Read or Write Cycle Time	500		ns	
t_{CPW}	$\overline{\text{CAS}}$ Pulse Width	200	10,000	ns	
t_{RPW}	$\overline{\text{RAS}}$ Pulse Width	350	10,000	ns	
t_{RSH}	$\overline{\text{RAS}}$ Hold Time	200		ns	
t_{CSH}	$\overline{\text{CAS}}$ Hold Time	350		ns	
t_{RCH}	Read Command Hold Time	80		ns	
t_{RCS}	Read Command Setup Time	0		ns	

WRITE CYCLE ^[3]

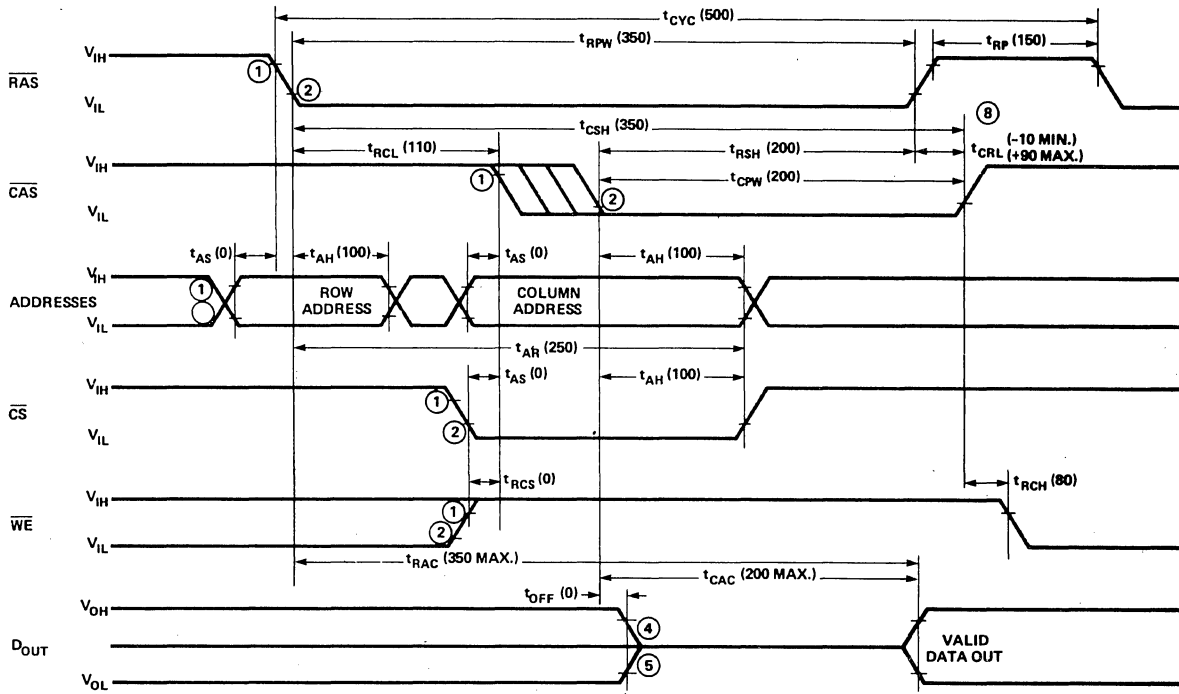
Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{CYC}	Random Read or Write Cycle Time	500		ns	
t_{CPW}	$\overline{\text{CAS}}$ Pulse Width	200	10,000	ns	
t_{RPW}	$\overline{\text{RAS}}$ Pulse Width	350	10,000	ns	
t_{RSH}	$\overline{\text{RAS}}$ Hold Time	200		ns	
t_{CSH}	$\overline{\text{CAS}}$ Hold Time	350		ns	
t_{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	200		ns	
t_{WCH}	Write Command Hold Time	150		ns	
t_{WP}	Write Command Pulse Width	200		ns	
t_{DS}	Data In Setup Time	0		ns	
t_{DH}	Data In Hold Time	200		ns	

Notes:

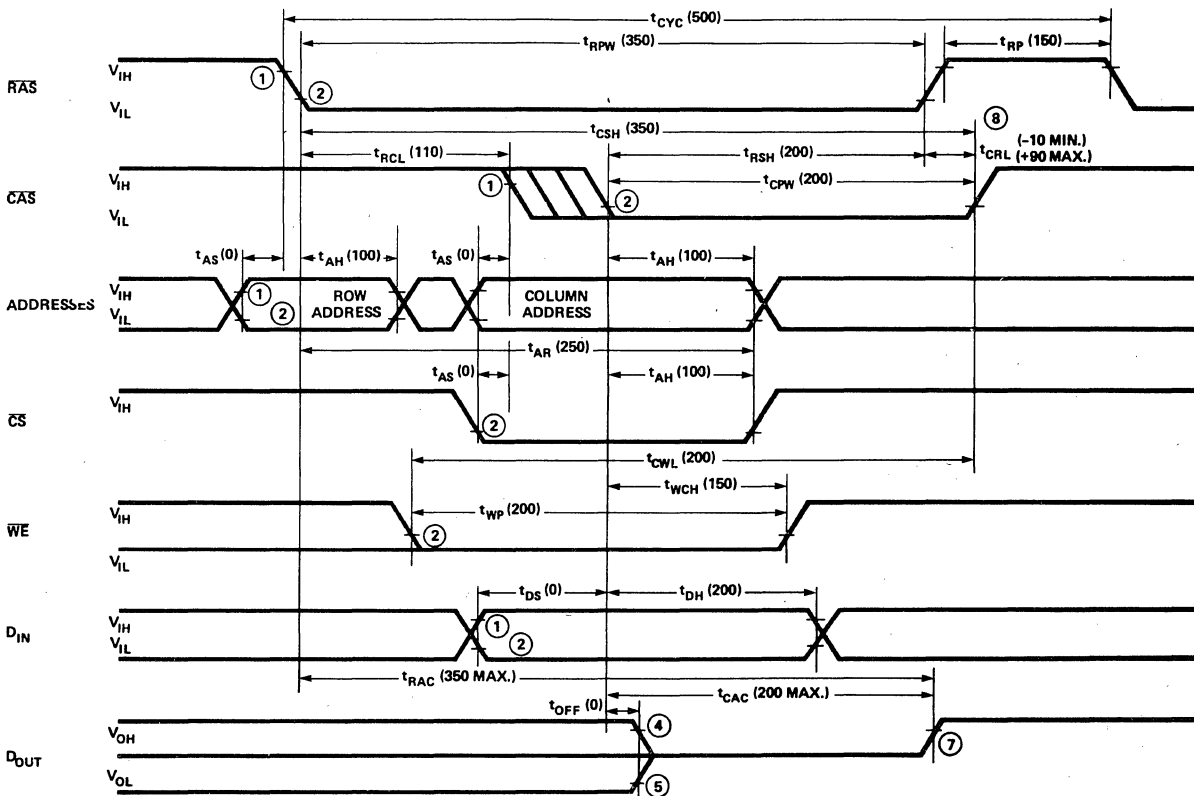
- All voltages referenced to V_{SS} .
- $\overline{\text{CAS}}$ must remain at V_{IH} a minimum of 110ns after $\overline{\text{RAS}}$ switches to V_{IL} . To achieve the minimum guaranteed access time of 350ns (t_{RAC}), $\overline{\text{CAS}}$ must switch to V_{IL} at or before 150 ns after $\overline{\text{RAS}}$ switches to V_{IL} . Refer to applications information in Read Cycle section.
- The minimum cycle timing does not allow for t_T or skews.

Waveforms

READ CYCLE (Numbers in parentheses are minimum values in nsec unless otherwise stated.) [6]



WRITE CYCLE (Numbers in parentheses are minimum values in nsec unless otherwise stated.) [6]



See next page for NOTES.

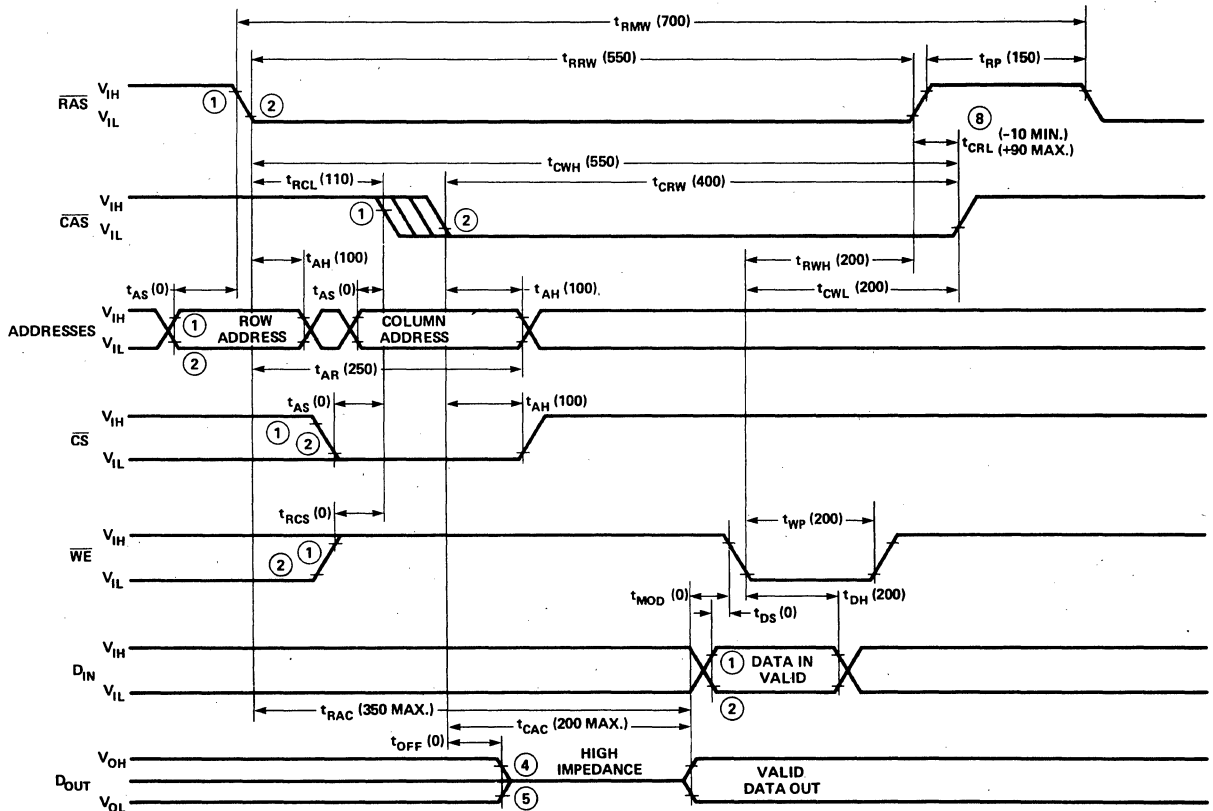
A.C. Characteristics ^[1] $T_A=0^{\circ}\text{C}$ to 70°C , $V_{DD}=12\text{V} \pm 5\%$, $V_{CC}=5\text{V} \pm 10\%$, $V_{BB}=-5\text{V} \pm 10\%$, $V_{SS}=0\text{V}$, unless otherwise noted.

READ MODIFY WRITE CYCLE ^[6]

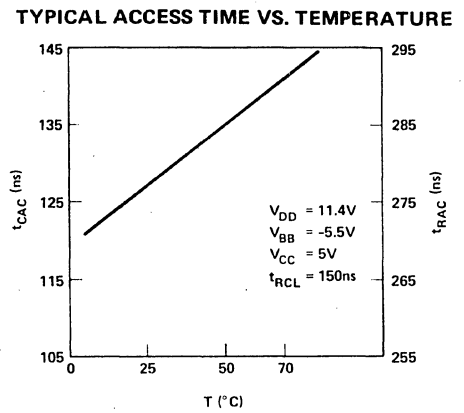
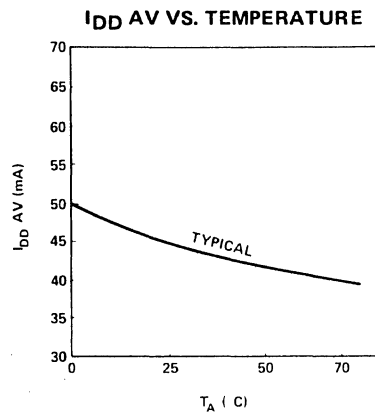
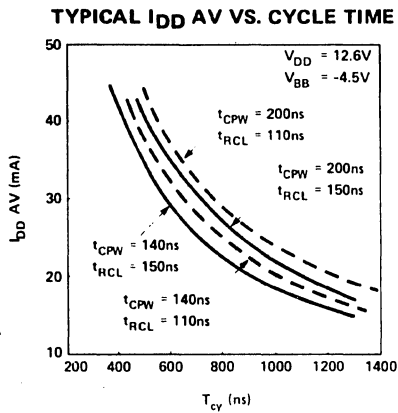
Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RMW}	Read Modify Write Cycle Time	700		ns	
t_{CRW}	RMW Cycle $\overline{\text{CAS}}$ Width	400	10,000	ns	
t_{RRW}	RMW Cycle $\overline{\text{RAS}}$ Width	550	10,000	ns	
t_{RWH}	RMW Cycle $\overline{\text{RAS}}$ Hold Time	200		ns	
t_{CWH}	RMW Cycle $\overline{\text{CAS}}$ Hold Time	550		ns	
t_{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	200		ns	
t_{WP}	Write Command Pulse Width	200		ns	
t_{RCS}	Read Command Setup Time	0		ns	
t_{MOD}	Modify Time	0		ns	
t_{DS}	Data In Setup Time	0		ns	
t_{DH}	Data In Hold Time	200		ns	

Waveforms

READ MODIFY WRITE CYCLE (Numbers in parentheses are minimum values in nsec unless otherwise stated.) ^[6]



- Notes:
- V_{IHMIN} and V_{ILMAX} are reference levels for measuring timing of input signals.
 - $\overline{\text{CAS}}$ must remain at V_{IH} a minimum of 110ns after $\overline{\text{RAS}}$ switches to V_{IL} . To achieve the minimum guaranteed access time of 350ns (t_{RAC}), $\overline{\text{CAS}}$ must switch to V_{IL} at or before 150ns after $\overline{\text{RAS}}$ switches to V_{IL} . Refer to applications information in Read Cycle section.
 - V_{OHMIN} and V_{OLMAX} are reference levels for measuring timing of D_{OUT} .
 - Minimum cycle timing does not allow for t_{T} or signal skew.
 - If $\overline{\text{WE}}$ goes low while $\overline{\text{CAS}}$ is low, D_{OUT} could go to either V_{OL} or V_{OH} after t_{CAC} . D_{OUT} will go to V_{OH} as shown on page 4 (Write Cycle Waveforms) if $\overline{\text{WE}}$ goes low before $\overline{\text{CAS}}$ goes low. In a Read-Modify-Write cycle, D_{OUT} is data read and does not change during the Modify-Write portion of the cycle.
 - For minimum cycle timing, t_{CRL} must be -0 to +90ns.



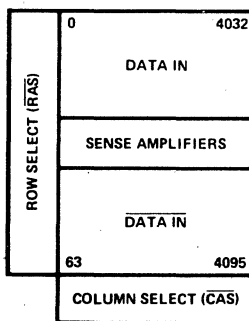
Applications

ADDRESSING

Two externally applied negative going TTL clocks, Row Address Strobe (\overline{RAS}), and Column Address Strobe (\overline{CAS}), are used to strobe the two sets of 6 addresses into internal address buffer registers. The first clock, \overline{RAS} , strobes in the six low order addresses (A_0-A_5) which selects one of 64 rows and begins the timing which enables the column sense amplifiers. The second clock, \overline{CAS} , strobes in the six high order addresses (A_6-A_{11}) to select one of 64 column sense amplifiers and Chip Select (\overline{CS}) which enables the data out buffer.

An address map of the 2104 is shown below. Address "0" corresponds to all addresses at V_{IL} . Note that data is stored in half of the memory as a logic inversion of the data presented at the input pin as shown. This inversion is completely transparent to the user (i.e., data stored in memory as a "1" or "0" at the input will when subsequently accessed, appear as a "1" or "0" respectively at the output).

2104 Address Map



DATA CYCLES/TIMING

A memory cycle begins with addresses stable and a negative transition of \overline{RAS} . See the waveforms on page 4. It is not necessary to know whether a Read or Write cycle is to be performed until \overline{CAS} becomes valid.

Note that Chip Select (\overline{CS}) does not have to be valid until the second clock, \overline{CAS} . It is, therefore, possible to start a memory cycle before it is known which device must be selected. This can result in a significant improvement in system access time since the decode time for chip select does not enter into the calculation for access time.

Both the \overline{RAS} and \overline{CAS} clocks are TTL compatible and do not require level shifting and driving at high voltage MOS levels. Buffers internal to the 2104 convert the TTL level signals to MOS levels inside the device. Therefore, the delay associated with external TTL-MOS level converters is not added to the 2104 system access time.

READ CYCLE

A Read cycle is performed by maintaining Write Enable (\overline{WE}) high during \overline{CAS} . The output pin of a selected device will unconditionally go to a high impedance state immediately following the leading edge of \overline{CAS} and remain in this state until valid data appears at the output at access time. The selected output data is internally latched and will remain valid until a subsequent \overline{CAS} is given to the device by a Read, Write, Read-Modify-Write or Refresh cycle. Data-out goes to a high impedance state for all non-selected devices.

Device access time, t_{ACC} , is the longer of two calculated intervals:

$$1. t_{ACC} = t_{RAC} \quad \text{OR} \quad 2. t_{ACC} = t_{RCL} + t_T + t_{CAC}$$

Access time from \overline{RAS} , t_{RAC} , and access time from \overline{CAS} , t_{CAC} , are device parameters. Row to column address strobe lead time, t_{RCL} , and transition time, t_T , are system dependent timing parameters. Substituting the device parameters and assuming a TTL level transition time of 5ns yields:

$$3. t_{ACC} = t_{RAC} = 350ns \text{ for } 110ns \leq t_{RCL} \leq 145ns$$

OR

$$4. t_{ACC} = t_{RCL} + t_T + t_{CAC} = t_{RCL} + 205ns \text{ for } t_{RCL} > 145ns.$$

Note that if $110ns \leq t_{RCL} \leq 145ns$, device access time is determined by equation 3 and is equal to $t_{RAC} > 145ns$ access time is determined by equation 4. This 35ns interval (shown in the t_{RCL} inequality in equation 3) in which the falling edge of \overline{CAS} can occur without affecting access time is provided to allow for system timing skew in the generation of \overline{CAS} . This allowance for a t_{RCL} skew is designed in at the device level to allow minimum access times to be achieved in practical system designs.

WRITE CYCLE

A Write Cycle is performed by bringing Write Enable (\overline{WE}) low before or during \overline{CAS} . If Write Enable goes low at or before \overline{CAS} goes low, the input data must be valid at or before the falling edge of \overline{CAS} . D_{OUT} will go to V_{OH} as shown

on page 4 (Write Cycle) if \overline{WE} goes low before \overline{CAS} goes low. If Write Enable goes low after \overline{CAS} , data in must be valid at or before the falling edge of \overline{WE} . Data out goes to a high impedance state following the leading edge of \overline{CAS} . If \overline{WE} goes low while \overline{CAS} is low, D_{OUT} could go to either V_{OL} or V_{OH} after t_{CAC} .

READ-MODIFY-WRITE CYCLE

A Read-Modify-Write Cycle is performed by bringing Write Enable (\overline{WE}) low after access time, t_{ACC} , with \overline{RAS} and \overline{CAS} low. Data in must be valid at or before the falling edge of \overline{WE} . In a read-modify-write cycle D_{OUT} is data read and does not change during the modify-write portion of the cycle.

\overline{CAS} ONLY (DESELECT) CYCLE

In some applications, it is desirable to be able to deselect all memory devices without running a regular memory cycle. This may be accomplished with the 2104 by performing a \overline{CAS} Only Cycle. Receipt of a \overline{CAS} without a \overline{RAS} deselects the 2104 and forces the Data Output to the high-impedance state. This places the 2104 in its lowest power, standby condition as will be discussed in the POWER DISSIPATION section below. The cycle timing and \overline{CAS} timing should be just as if a normal $\overline{RAS}/\overline{CAS}$ cycle was being performed.

CHIP SELECTION/DESELECTION

The 2104 is selected by driving \overline{CS} low during a Read, Write, or Read-Modify-Write cycle. A device is deselected by 1) driving \overline{CS} high during a Read, Write, or Read-Modify-Write cycle or 2) performing a \overline{CAS} Only cycle independent of the state of \overline{CS} .

REFRESH CYCLES

Each of the 64 rows internal to the 2104 must be refreshed every 2 msec to maintain data. Any data cycle (Read, Write, Read-Modify-Write) refreshes the entire selected row (defined by the low order row addresses). The refresh operation is independent of the state of chip select. It is evident, of course, that if a Write or Read-Modify-Write cycle is used to refresh a row, the device should be deselected (\overline{CS} high) if it is desired not to change the state of the selected cell.

$\overline{RAS}/\overline{CAS}$ TIMING

The device clocks, \overline{RAS} and \overline{CAS} , control operation of the 2104. The timing of each clock and the timing relationships of the two clocks must be understood by the user in order to obtain maximum performance in a memory system.

The \overline{RAS} and \overline{CAS} have minimum pulse widths as defined by t_{RPW} and t_{CPW} respectively. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle, once begun by driving \overline{RAS} and/or \overline{CAS} low, must not be ended or aborted prior to fulfilling the minimum clock signal pulse width(s). A new cycle must not begin until the minimum precharge time, t_{RP} , has been met.

The timing relationship of the leading edges of \overline{RAS} and \overline{CAS} is defined by t_{RCL} and is discussed in the READ CYCLE section above. The trailing edge relationship is defined by t_{RSH} , t_{CSH} , and t_{CRL} . The first two parameters define the

minimum time during a memory cycle that \overline{RAS} and \overline{CAS} are both low (minimum hold times). Both the minimum clock widths and hold times must be met for proper operation.

For example, using $t_T = 5ns$, $t_{RCL} = 110ns$, $t_{RPW} = 350ns$, and $t_{CPW} = 200ns$; the trailing edge of \overline{CAS} would occur at time (t) where:

$$t = t_{RCL} + t_T + t_{CPW} = 110ns + 5ns + 200ns = 315ns$$

however, $t_{CSH} = 350ns$, and, therefore, t_{CPW} would need to be lengthened such that:

$$t_{CPW} (\text{actual}) = 200ns + (350ns - 315ns) = 235ns$$

in order to meet the minimum t_{CSH} requirement.

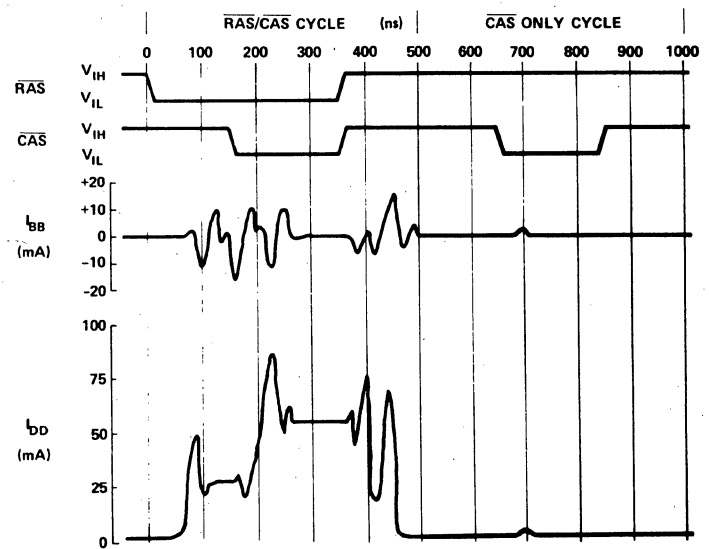
The third parameter, t_{CRL} , defines the lead (-) or lag (+) time allowable for \overline{CAS} with respect to \overline{RAS} . If all minimum timing requirements for \overline{RAS} and \overline{CAS} are met, the \overline{CAS} trailing edge may lead the \overline{RAS} trailing edge by up to 10ns or lag by up to 90ns. In a memory cycle with all minimum timing specifications used, \overline{CAS} may lag \overline{RAS} but cannot lead \overline{RAS} since t_{CSH} would be violated if \overline{CAS} led \overline{RAS} .

POWER DISSIPATION

OPERATING

The power dissipation of a continuously operating 2104 device is the sum of $V_{DD} \times I_{DDAV}$ and $V_{BB} \times I_{BB}$. For a cycle time of 500ns (including a t_{RP} of 150ns) the typical power dissipation is 540mW.

Typical power supply current waveforms versus time are shown below for both a $\overline{RAS}/\overline{CAS}$ cycle and a \overline{CAS} only cycle. It is evident from examination of the current waveforms that the major portion of the device power dissipation is the $V_{DD} \times I_{DDAV}$ component. Since the average value of I_{DD} is used to compute the power dissipation and I_{DD} is high only while \overline{RAS} and \overline{CAS} are low, minimum \overline{RAS} and \overline{CAS} pulse widths are preferred even with long cycle times to minimize power dissipation.



TYPICAL SUPPLY CURRENTS VS. TIME

SILICON GATE MOS 2104

STANDBY-REFRESH ONLY

The standby power-refresh only is calculated by the following equation:

$$5. P_{REF} = P_{OP} \times \left(64 \frac{t_{CYC}}{t_{REF}}\right) + P_{SB} \left(1 - 64 \frac{t_{CYC}}{t_{REF}}\right)$$

- Where:
- P_{REF} = Standby power-refresh only.
 - P_{OP} = Power dissipation-continuous operation.
 - t_{CYC} = Cycle time for a Refresh cycle.
 - t_{REF} = Time between refresh.
 - P_{SB} = Standby power dissipation.

The standby power dissipation P_{SB} is given by:

$$6. P_{SB} = V_{DD} \times I_{DD1} + V_{BB} \times I_{BB}$$

The typical power dissipated is a standby-refresh only mode with the device deselected (\overline{CS} high) is 20mW. If the device is selected (\overline{CS} low) during a refresh cycle, the typical power dissipated is 32mW. This is the result of the internal output buffer circuitry being turned on. Since needless power is dissipated for this condition, it is recommended that the device be deselected during standby-refresh only operation.

Note that when calculating the standby power for a 2104 memory system it is not necessary to include the power

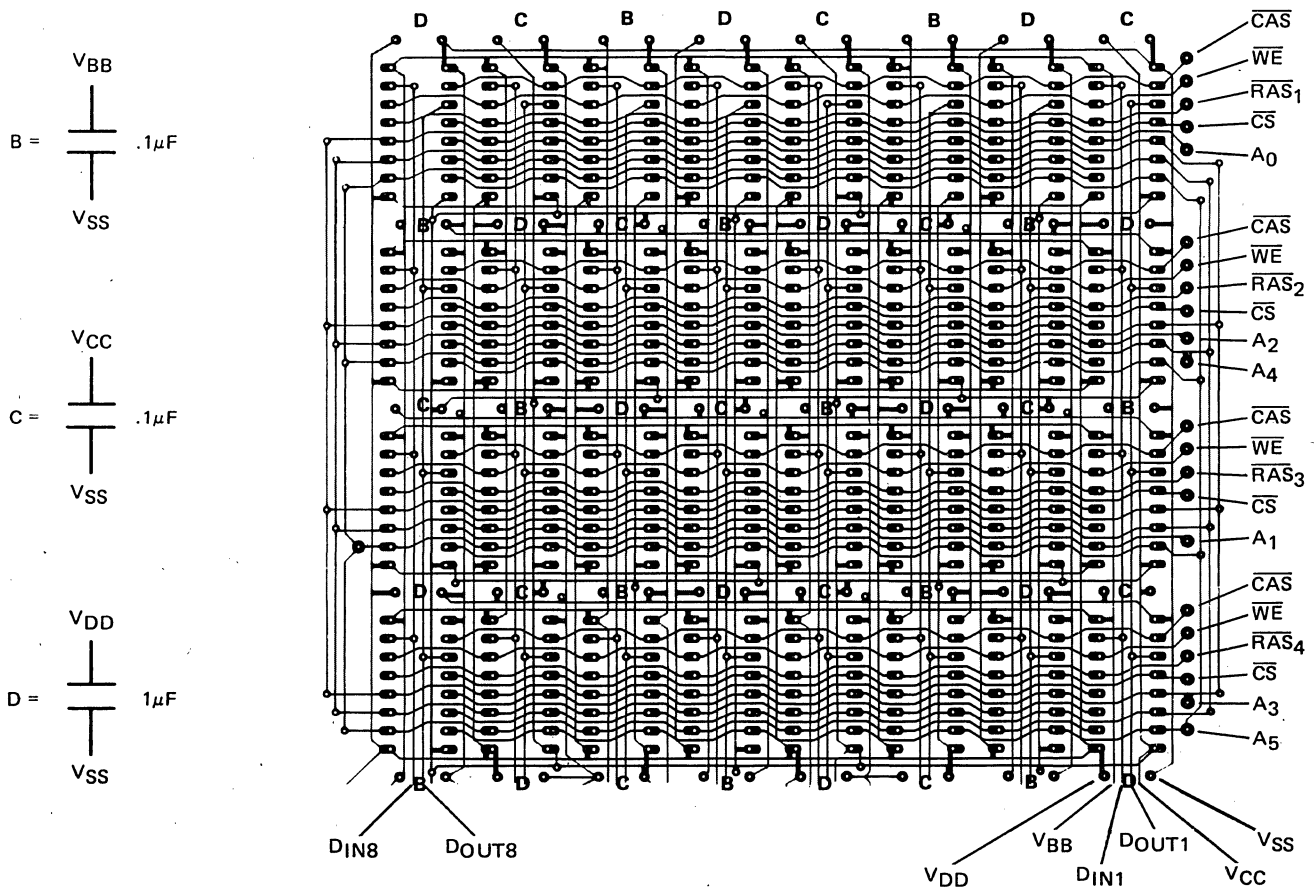
dissipated by TTL to MOS level converters. These converters are incorporated internally to the 2104 and are included in the previous power calculations.

SYSTEM LAYOUT AND DECOUPLING

A two sided memory array layout is shown below.

Decoupling is indicated by a "D" for V_{DD} to V_{SS} and "B" for V_{BB} to V_{SS} . I_{DD} and I_{BB} current surges at \overline{RAS} and \overline{CAS} make adequate decoupling of these supplies important. It is recommended that 1.0 μ F high frequency, low inductance capacitors be used between V_{DD} and V_{SS} on double sided boards. 0.1 μ F capacitors can be used between V_{BB} and V_{SS} . V_{CC} to V_{SS} decoupling is indicated by a "C" and 0.1 μ F capacitors are recommended. For each 36 devices a 100 μ F tantalum or equivalent capacitor should be placed from V_{DD} to V_{SS} near the array. An equal or slightly smaller bulk capacitor should be placed between V_{BB} and V_{SS} on the memory card.

Note that all power lines (including V_{SS}) are gridded both horizontally and vertically at each memory device. This minimizes the power distribution impedance and enhances the effect of the decoupling capacitors.



Two Sided Layout for 16K x 8 Memory

Intel
MEMORY



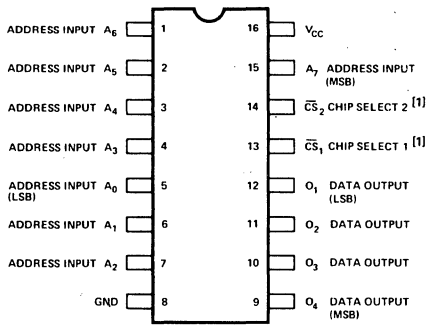
Schottky Bipolar 3601, 3621

HIGH SPEED 1K (256 x 4) PROM

- Fast Access Time — 50 nsec Maximum (3601-1, 3621-1)
- Fast Programming — 1 ms/bit Typically
- Three State Outputs (3621)
- Open Collector Outputs (3601)
- Standard Packaging — 16 Pin Hermetic Dual In-Line Lead Configuration

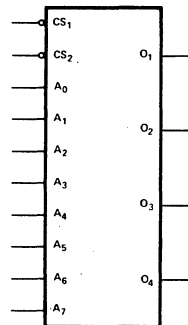
The 3601 and 3621 PROM families are organized as 256 words by 4-bits. The 3601 family is manufactured with all outputs initially low and the 3621 family with all outputs initially high.

PIN CONFIGURATION



NOTE 1. DURING PROGRAMMING THE PROGRAM PULSE MAY BE APPLIED TO EITHER CS₁ OR CS₂ FOR THE 3621 FAMILY ONLY.

LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-65°C to +150°C
Storage Temperature	-65°C to +160°C
Output or Supply Voltages	-0.5V to 7 Volts
All Input Voltages	-1.6V to 5.5V
Output Currents	100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All limits apply for V_{CC} = +5.0V ± 5%, T_A = 0°C to +75°C, unless otherwise specified.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ. [1]	Max.		
I _{FA}	Address Input Load Current		-0.05	-0.25	mA	V _{CC} = Max., V _A = 0.45V
I _{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V _{CC} = Max., V _S = 0.45V
I _{RA}	Address Input Leakage Current			40	μA	V _{CC} = Max., V _A = Max.
I _{RS}	Chip Select Input Leakage Current			40	μA	V _{CC} = Max., V _S = Max.
V _{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V _{CC} = Min., I _A = -10mA
V _{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V _{CC} = Min., I _S = -10mA
V _{OL}	Output Low Voltage		0.3	0.45	V	V _{CC} = Min., I _{OL} = 15mA
I _{CC}	Power Supply Current		90	130	mA	V _{CC} = Max., V _{A0} →V _{A7} = 0V CS ₁ = CS ₂ = 0V
V _{IL}	Input "Low" Voltage			0.85	V	V _{CC} = 5.0V
V _{IH}	Input "High" Voltage	2.0			V	V _{CC} = 5.0V
I _{CEX} [2]	Output Leakage Current			100	μA	V _{CC} = Max., V _{CE} = Max.
I _O [3]	Output Leakage for High Impedance Stage			40	μA	V _O = Max., or 0.45V, V _{CC} = 5.25V, CS ₁ = CS ₂ = 2.4V
I _{SC} [3,4]	Output Short Circuit Current	-15		-60	mA	V _{CC} = 5.00V, T _A = 25°C, V _O = 0V
V _{OH} [3]	Output High Voltage	2.4			V	I _{OH} = -2.4mA, V _{CC} = Min.

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2. This specification only applies to the 3601 family.

3. This specification only applies to the 3621 family.
4. Unmeasured outputs are open during this test.

SCHOTTKY BIPOLAR 3601, 3621

A. C. Characteristics $V_{CC} = +5V \pm 5\%$, $T_A = 0^\circ C$ to $+75^\circ C$

SYMBOL	PARAMETER	MAXIMUM LIMITS			UNIT	CONDITIONS
		0°C	25°C	75°C		
t_{A++} , t_{A--} t_{A+-} , t_{A-+}	Address to Output Delay (3601, 3621)	70	60	70	ns	Both C.S. lines must be at ground potential to activate the PROM.
t_{A++} , t_{A--} t_{A+-} , t_{A-+}	Address to Output Delay (3601-1, 3621-1)	50	50	50	ns	
t_{S++} , t_{S--}	Chip Select to Output Delay	25	25	25	ns	

Capacitance ⁽¹⁾ $T_A = 25^\circ C$

SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS
		TYP.	MAX.		
C_{INA}	Address Input Capacitance	4	10	pF	$V_{CC} = 5V$ $V_{IN} = 2.5V$
C_{INS}	Chip-Select Input Capacitance	6	10	pF	$V_{CC} = 5V$ $V_{IN} = 2.5V$
C_{OUT}	Output Capacitance	7	12	pF	$V_{CC} = 5V$ $V_{OUT} = 2.5V$

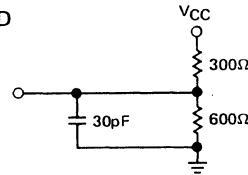
NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

Conditions of Test:

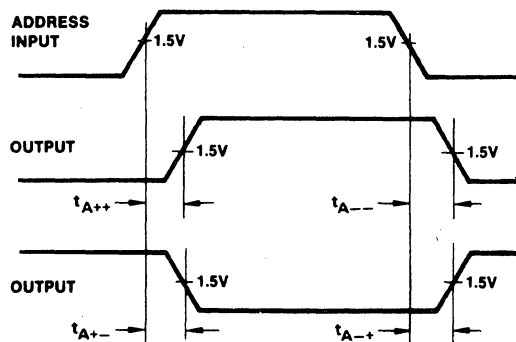
Input pulse amplitudes - 2.5V
 Input pulse rise and fall times of
 5 nanoseconds between 1 volt and 2 volts
 Speed measurements are made at 1.5 volt levels
 Output loading is 15 mA and 30 pF
 Frequency of test - 2.5 MHz

15 mA TEST LOAD

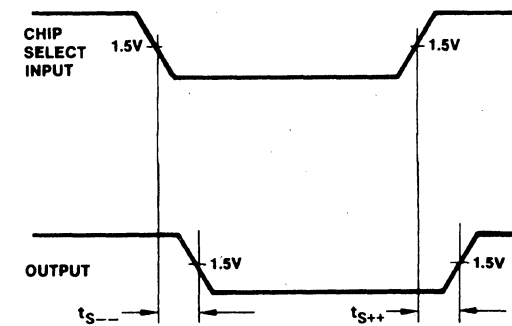


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY





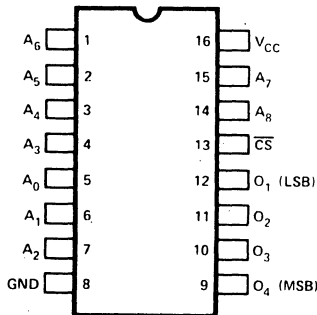
Schottky Bipolar 3602, 3602-4, 3602L-6, 3622, 3622-4, 3622L-6

HIGH SPEED 2K (512 x 4) PROM

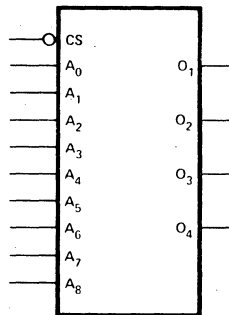
- Fast Access Time — 70ns (3602, 3622)
- Low Standby Power Dissipation (3602L-6, 3622L-6) — 115 μ W/bit
- Open Collector (3602, 3602-4, 3602L-6) or Three-State (3622, 3622-4, 3622L-6) Outputs

The 3602 and 3622 families are 512 words by 4 bit PROMs. The PROMs are manufactured with all outputs high and logic low levels can be electrically programmed in selected bit locations.

PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-65°C to +150°C
Storage Temperature	-65°C to +160°C
Output or Supply Voltages	-0.5V to 7 Volts
All Input Voltages	-1.6V to 5.6V
Output Currents	100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for $V_{CC} = +5V \pm 5\%$, $T_A = 0^\circ C$ to $+75^\circ C$, unless otherwise specified.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ. ^[1]	Max.		
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	$V_{CC} = 5.25V, V_A = 0.45V$
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	$V_{CC} = 5.25V, V_S = 0.45V$
I_{RA}	Address Input Leakage Current			40	μA	$V_{CC} = 5.25V, V_A = 5.25V$
I_{RS}	Chip Select Input Leakage Current			40	μA	$V_{CC} = 5.25V, V_S = 5.25V$
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	$V_{CC} = 4.75V, I_A = -10mA$
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	$V_{CC} = 4.75V, I_S = -10mA$
V_{OL}	Output Low Voltage		0.3	0.45	V	$V_{CC} = 4.75V, I_{OL} = 15mA$
$I_{CEX}^{[2]}$	Output Leakage Current			100	μA	$V_{CC} = 5.25V, V_{CE} = 5.25V$
I_{CC1}	Power Supply Current (3602, 3602-4, 3622, 3622-4)			140	mA	$V_{CC}=5.25V, V_{A0} \rightarrow V_{A8} = 0V, CS = 0V$
I_{CC2}	Power Supply Current (3602L-6, 3622L-6)	Active		110	mA	$V_{CC}=5.25V, CS = 0.45V$
		Standby		45	mA	$CS = 2.4V$
V_{IL}	Input "Low" Voltage			0.85	V	$V_{CC} = 5.0V$
V_{IH}	Input "High" Voltage	2.0			V	$V_{CC} = 5.0V$
$I_{O}^{[3]}$	Output Leakage for High Impedance Stage			40	μA	$V_O=5.25V$ or $0.45V, V_{CC}=5.25V, \overline{CS}=2.4V$
$I_{SC}^{[3,4]}$	Output Short Circuit Current	-15	-25	-60	mA	$V_{CC}=5.00V, T_A=25^\circ C, V_O = 0V$
$V_{OH}^{[3]}$	Output High Voltage	2.4			V	$I_{OH}=-2.4mA, V_{CC} = 4.75V$

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2. This specification only applies to the 3602 family.

3. This specification only applies to the 3622 family.
4. Unmeasured outputs are open during this test.

A. C. Characteristics $V_{CC} = +5V \pm 5\%$, $T_A = 0^\circ C$ to $+75^\circ C$

SYMBOL	PARAMETER	MAX. LIMIT			UNIT	CONDITIONS
		3602 3622	3602-4 3622-4	3602L-6 3622L-6		
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	70	90	90	ns	$\overline{CS} = V_{IL}$ to Select the PROM
t_{S++}	Chip Select to Output Delay	30	30	30	ns	
t_{S--}	Chip Select to Output Delay	30	30	120	ns	

Capacitance ⁽¹⁾ $T_A = 25^\circ C$, $f = 1$ MHz

SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS
		TYP.	MAX.		
C_{INA}	Address Input Capacitance	4	10	pF	$V_{CC} = 5V$ $V_{IN} = 2.5V$
C_{INS}	Chip-Select Input Capacitance	6	10	pF	$V_{CC} = 5V$ $V_{IN} = 2.5V$
C_{OUT}	Output Capacitance	7	12	pF	$V_{CC} = 5V$ $V_{OUT} = 2.5V$

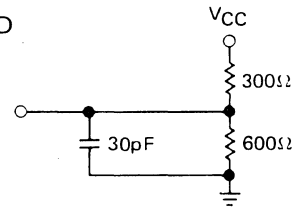
NOTE 1: This parameter is only periodically samp'ed and is not 100% tested.

Switching Characteristics

Conditions of Test:

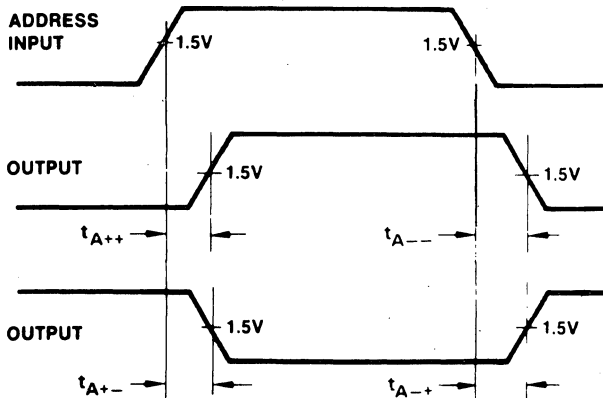
Input pulse amplitudes - 2.5V
 Input pulse rise and fall times of
 5 nanoseconds between 1 volt and 2 volts
 Speed measurements are made at 1.5 volt levels
 Output loading is 15 mA and 30 pF
 Frequency of test - 2.5 MHz

15 mA TEST LOAD

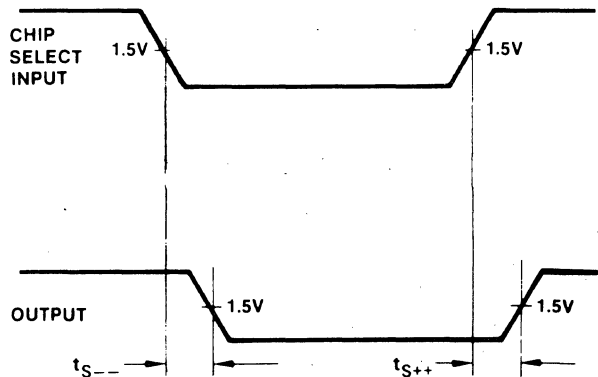


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



Intel

MEMORY



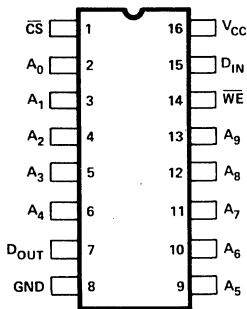
Silicon Gate MOS 2115, 2125

HIGH SPEED STATIC 1024 BIT RAM

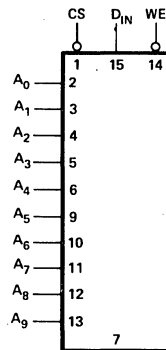
- Access Time (2115-2/2125-2): 60ns Typical
- Fully Pin Compatible to 93415 (2115) and 93425 (2125)
- Low Operating Power Dissipation: Typical 0.2mW/bit (2115L, 2125L)
- Single +5V Supply
- Uncommitted Collector (2115) and Three-State (2125) Output

The Intel® 2115 and 2125 family are fully static read/write random access memories organized as 1024 words by 1 bit. These RAMs are designed for buffer control storage and high performance main memory applications. They are compatible with TTL logic families in all respects: inputs, output, and a single +5V supply. Both uncommitted collector and three state output are available.

PIN CONFIGURATION



LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8
D_{OUT}

2115, 2125 FAMILY

	2115, 2125	2115-2, 2125-2	2115L, 2125L
Typ. T _{AA} (ns)	70	60	75
Typ. I _{CC} (mA)	75	100	50

D.C. Characteristics ^[1] V_{CC} = 5V ±5%, T_A = 0°C to 75°C

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
V _{OL1}	2115, 2115L Output Low Voltage			0.45	V	I _{OL} = 12mA
V _{OL2}	2115-2, 2125-2 Output Low Voltage			0.45	V	I _{OL} = 16mA
V _{OL3}	2125, 2125L Output Low Voltage			0.45	V	I _{OL} = 7mA
V _{IH}	Input High Voltage	2.1			V	
V _{IL}	Input Low Voltage			0.8	V	
I _{IL}	Input Low Current		-1	-40	μA	V _{CC} =Max., V _{IN} =0.4V
I _{IH}	Input High Current		1	40	μA	V _{CC} =Max., V _{IN} =4.5V
I _{CEX}	2115 Family Output Leakage Current		10	100	μA	V _{CC} =Max., V _{OUT} =4.5V
I _{OFF}	2125 Family Output Current (High Z)		10	50	μA	V _{CC} =Max., V _{OUT} =0.5V/2.4V
I _{OS} ^[2]	2125 Family Current Short Circuit to Ground			-100	mA	V _{CC} =4.5V
V _{OH}	2125 Family Output High Voltage	2.4			V	I _{OH} =-3.2mA
I _{CC1}	2115L, 2125L Power Supply Current		50	65	mA	All Inputs Grounded, Output Open
I _{CC1}	2115, 2125 Power Supply Current		75	100	mA	All Inputs Grounded, Output Open
I _{CC2}	2115-2, 2125-2 Power Supply Current			125	mA	All Inputs Grounded, Output Open

Notes:

1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:

θ_{JA} (@ 400 fpm air flow) = 45°C/W

θ_{JA} (still air) = 60°C/W

θ_{JC} = 25°C/W.

2. Duration of short circuit current should not exceed 1 second.

SILICON GATE MOS 2115, 2125

2115 Family A.C. Characteristics ^[1] $V_{CC} = 5V \pm 5\%$, $T_A = 0^\circ C$ to $75^\circ C$

READ CYCLE

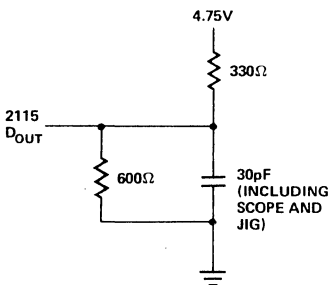
Symbol	Test	2115 Limits			2115-2 Limits			2115L Limits			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{ACS}	Chip Select Time	5		45	5		40	5		50	ns
t_{RCS}	Chip Select Recovery Time			40			40			40	ns
t_{AA}	Address Access Time		70	90		60	70		75	95	ns
t_{OH}	Previous Read Data Valid After Change of Address	10			10			10			ns

WRITE CYCLE

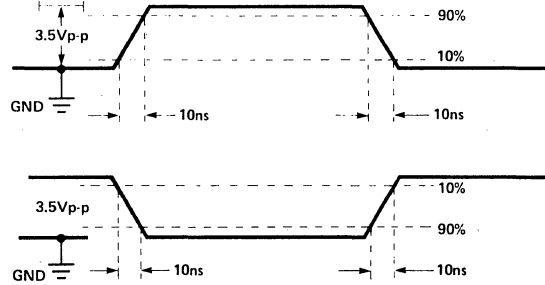
Symbol	Test	2115 Limits			2115-2 Limits			2115L Limits			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{WS}	Write Enable Time			40			40			40	ns
t_{WR}	Write Recovery Time	5		45	5		45	5		50	ns
t_W	Write Pulse Width	50			50			60			ns
t_{WSD}	Data Set-Up Time Prior to Write	5			5			15			ns
t_{WHD}	Data Hold Time After Write	5			5			15			ns
t_{WSA}	Address Set-Up Time	15			15			20			ns
t_{WHA}	Address Hold Time	5			5			15			ns
t_{WSCS}	Chip Select Set-Up Time	5			5			15			ns
t_{WHCS}	Chip Select Hold Time	5			5			15			ns

TEST CONDITIONS

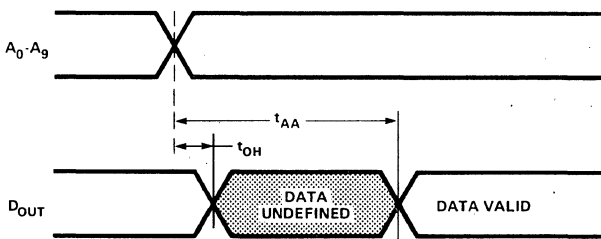
LOADING CONDITIONS



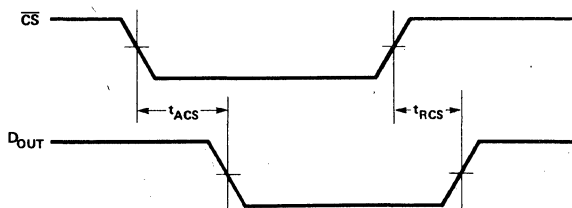
ALL INPUT PULSES



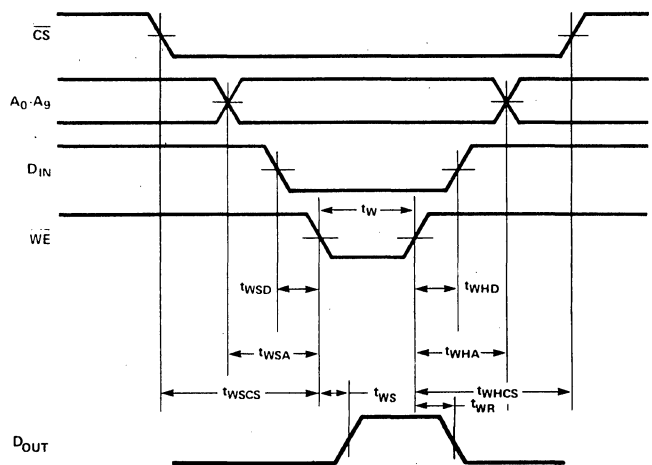
READ CYCLE



PROPAGATION DELAY FROM CHIP SELECT



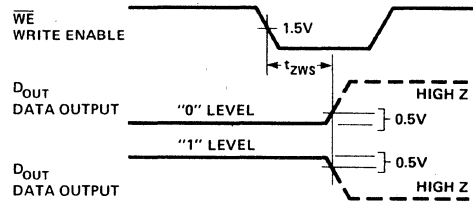
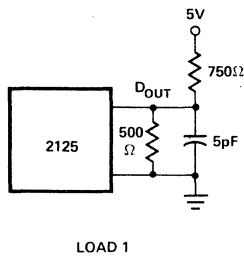
WRITE CYCLE



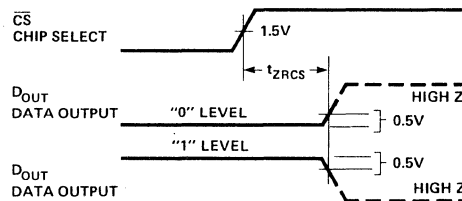
(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

SILICON GATE MOS 2115, 2125

2125 FAMILY WRITE ENABLE TO HIGH Z DELAY



2125 FAMILY PROPAGATION DELAY FROM CHIP SELECT TO HIGH Z



(All t_{ZXXX} parameters are measured at a delta of 0.5V from the logic level and using Load 1.)

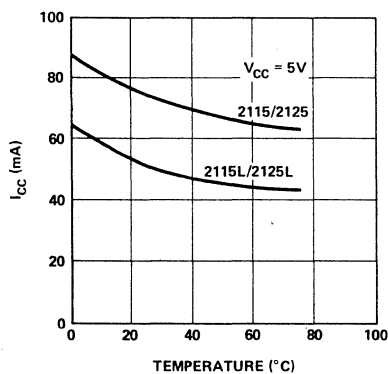
2115/2125 FAMILY CAPACITANCE* $V_{CC} = 5V, f = 1 \text{ MHz}, T_A = 25^\circ\text{C}$

Symbol	Test	2115 Family Limits		2125 Family Limits		Units	Test Conditions
		Typ.	Max.	Typ.	Max.		
C_I	Input Capacitance	3	5	3	5	pF	All Inputs = 0V, Output Open
C_O	Output Capacitance	5	8	5	8	pF	$\overline{CS} = 5V$, All other inputs = 0V, Output Open

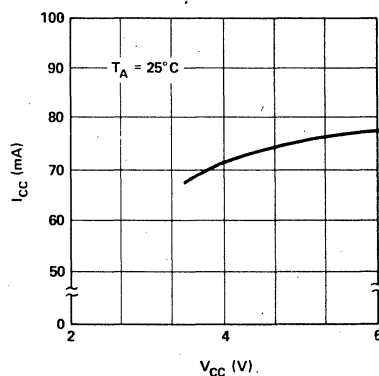
*This parameter is periodically sampled and is not 100% tested.

Typical Characteristics

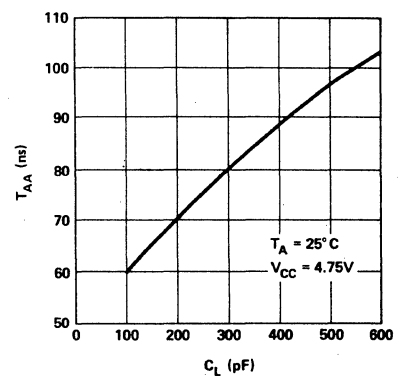
I_{CC} VS. TEMPERATURE



I_{CC} VS. V_{CC}



ACCESS TIME VS. CAPACITANCE



Intel

MEMORY

SILICON GATE MOS 2115, 2125

2125 Family A.C. Characteristics ^[1] $V_{CC} = 5V \pm 5\%$, $T_A = 0^\circ C$ to $75^\circ C$

READ CYCLE

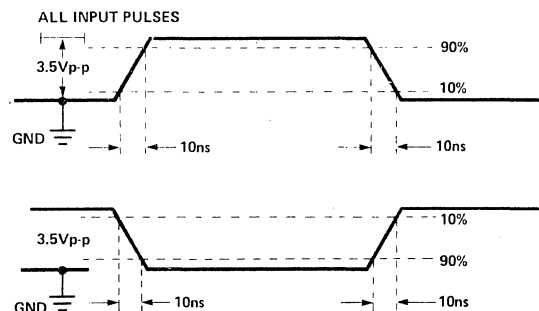
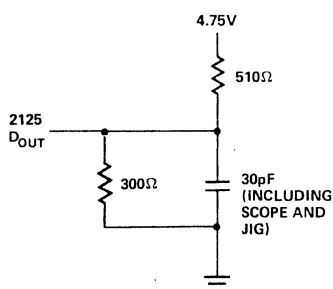
Symbol	Test	2125 Limits			2125-2 Limits			2125L Limits			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{ACS}	Chip Select Time	5		45	5		40	5		50	ns
t_{ZRCS}	Chip Select to HIGH Z			40			40			40	ns
t_{AA}	Address Access Time		70	90		60	70		75	95	ns
t_{OH}	Previous Read Data Valid After Change of Address	10			10			10			ns

WRITE CYCLE

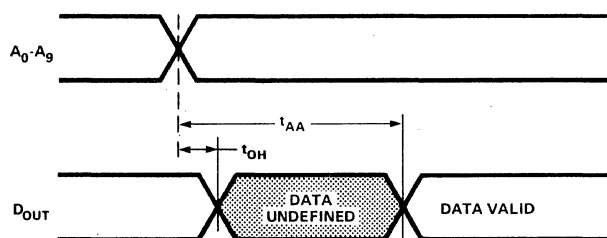
Symbol	Test	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
		t_{ZWS}	Write Enable to HIGH Z			40			40		
t_{WR}	Write Recovery Time	5		45	5		45	5		50	ns
t_W	Write Pulse Width	50			50			60			ns
t_{WSD}	Data Set-Up Time Prior to Write	5			5			15			ns
t_{WHD}	Data Hold Time After Write	5			5			15			ns
t_{WSA}	Address Set-Up Time	15			15			20			ns
t_{WHA}	Address Hold Time	5			5			15			ns
t_{WSCS}	Chip Select Set-Up Time	5			5			15			ns
t_{WHCS}	Chip Select Hold Time	5			5			15			ns

TEST CONDITIONS

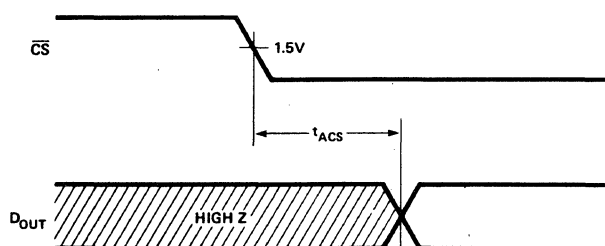
LOADING CONDITIONS



READ CYCLE

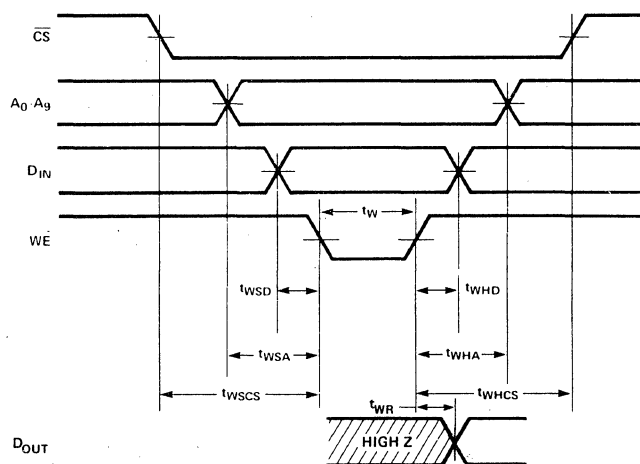


PROPAGATION DELAY FROM CHIP SELECT



(ALL ABOVE MEASUREMENTS REFERENCED TO 1.5V)

WRITE CYCLE



Intel

MEMORY



Silicon Gate MOS 2708/2704

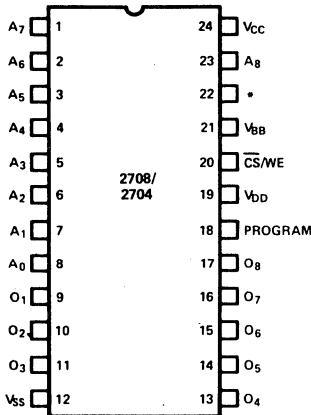
8192/4096 BIT ERASABLE AND ELECTRICALLY REPROGRAMMABLE READ ONLY MEMORY

- 2708 1024x8 Organization
- 2704 512x8 Organization

- Max Access Time — 450ns
- Static — No Clocks Required
- TTL Compatible
- Three-State Output

The 2708 and 2704 are packaged in a 24 pin dual-in-line package with a transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

PIN CONFIGURATIONS



*2704 = V_{SS}
2708 = A₉

Absolute Maximum Ratings*

Temperature Under Bias	-25°C to +85°C
Storage Temperature	-65°C to +125°C
V _{DD} With Respect to V _{BB}	+20V to -0.3V
V _{CC} and V _{SS} With Respect to V _{BB}	+15V to -0.3V
All Input or Output Voltages With Respect to V _{BB} During Read	+15V to -0.3V
CS/WE Input With Respect to V _{BB} During Programming	+20V to -0.3V
Program Input With Respect to V _{BB}	+35V to -0.3V
Power Dissipation	1.5W

*COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, V_{BB} = -5V ±5%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ. ^[1]	Max.	Unit	Conditions
I _{LI}	Address and Chip Select Input Load Current			10	μA	V _{IN} = 5.25V
I _{LO}	Output Leakage Current			10	μA	V _{OUT} = 5.25V, CS/WE = 5V
I _{DD}	V _{DD} Supply Current		50	65	mA	Worst Case Supply Currents: All Inputs High CS/WE = 5V; T _A = 0°C
I _{CC}	V _{CC} Supply Current		6	10	mA	
I _{BB}	V _{BB} Supply Current		30	45	mA	
V _{IL}	Input Low Voltage	V _{SS}		0.65	V	
V _{IH}	Input High Voltage	3.0		V _{CC} +1	V	
V _{OL}	Output Low Voltage			0.45	V	I _{OL} = 1.6mA
V _{OH1}	Output High Voltage	3.7			V	I _{OH} = -100μA
V _{OH2}	Output High Voltage	2.4			V	I _{OH} = -1mA
P _D	Power Dissipation			800	mW	T _A = 70°C

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltages.
2. The program input (Pin 18) is tied to V_{SS} during the read mode.

Intel

MEMORY

A.C. Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = +5\text{V} \pm 5\%$, $V_{DD} = +12\text{V} \pm 5\%$, $V_{BB} = -5\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ACC}	Address to Output Delay		280	450	ns
t_{CO}	Chip Select to Output Delay			120	ns
t_{DF}	Chip De-Select to Output Float	0		120	ns
t_{OH}	Address to Output Hold	0			ns

Capacitance^[1] $T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN}=0\text{V}$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT}=0\text{V}$

Note 1. This parameter is periodically sampled and not 100% tested.

A.C. Test Conditions:

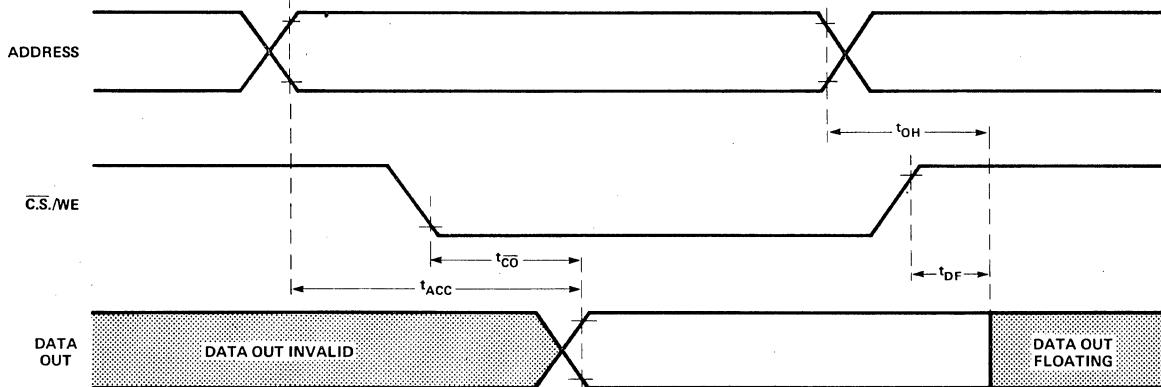
Output Load: 1 TTL gate and $C_L = 100\text{pF}$

Input Rise and Fall Times: $\leq 20\text{ns}$

Timing Measurement Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs

Input Pulse Levels: 0.65V to 3.0V

Waveforms



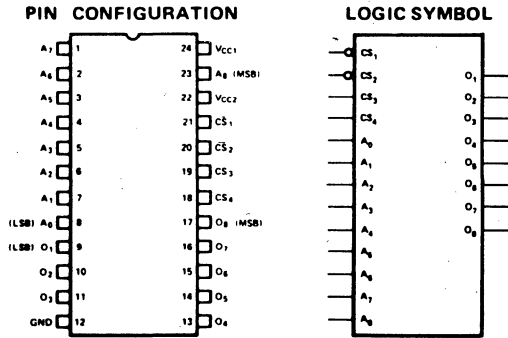


Schottky Bipolar 3604, 3604-4, 3604L-6, 3624, 3624-4

HIGH SPEED 4K (512 x 8) PROM

- **Fast Access Time — 70 ns (3604, 3624)**
- **Low Standby Power Dissipation (3604L-6) — 60 μ W/bit**
- **Open Collector (3604, 3604-4, 3604L-6) or Three-State (3624, 3624-4) Outputs**

The 3604 and 3624 family are 512 words by 8 bit PROMs. The PROMs are manufactured with all outputs high and logic low levels can be electrically programmed in selected bit locations.



Mode/Pin Connection	Pin 22	Pin 24
Read:	3604, 3604-4, 3604L-6	No Connect or 5V +5V No Connect
	3604, 3604-4, 3604L-6	Pulsed 12.5V Pulsed 12.5V Pulsed 12.5V
Standby Power:	3604L-6	Power dissipation is automatically reduced whenever the 3604L-6 is deselected.

D. C. Characteristics: All Limits Apply for $V_{CC}=+5.0V \pm 5\%$, $T_A=0^\circ C$ to $+75^\circ C$, unless otherwise specified.

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.[1]	Max.	Unit	
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	$V_{CC}=5.25V, V_A=0.45V$
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	$V_{CC}=5.25V, V_S=0.45V$
I_{RA}	Address Input Leakage Current			40	μA	$V_{CC}=5.25V, V_A=5.25V$
I_{RS}	Chip Select Input Leakage Current			40	μA	$V_{CC}=5.25V, V_S=5.25V$
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	$V_{CC}=4.75V, I_A=-10mA$
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	$V_{CC}=4.75V, I_S=-10mA$
V_{OL}	Output Low Voltage		0.3	0.45	V	$V_{CC}=4.75V, I_{OL}=15mA$
I_{CEX} [2]	Output Leakage Current			100	μA	$V_{CC}=5.25V, V_{CE}=5.25V$
I_{CC1}	Power Supply Current (3604, 3604-4)			190	mA	$V_{CC1}=5.25V, V_{A0} \rightarrow V_{A8}=0V, \overline{CS}_1=\overline{CS}_2=0V, CS_3=CS_4=5.25V$
I_{CC2}	Power Supply Current (3624, 3624-4)			190	mA	$V_{CC1}=5.25V, V_{A0} \rightarrow V_{A8}=0V, \overline{CS}_1=\overline{CS}_2=0V, CS_3=CS_4=5.25V$
I_{CC}	Power Supply Current (3604L-6)	Active		140	mA	$V_{CC2}=5.25V, V_{CC1}=Open, \overline{CS}_1=\overline{CS}_2=0.45V, CS_3=CS_4=2.4V$
		Standby		45	mA	$\overline{CS}_1=\overline{CS}_2=2.5V$
V_{IL}	Input "Low" Voltage			0.85	V	$V_{CC}=5.0V$
V_{IH}	Input "High" Voltage	2.0			V	$V_{CC}=5.0V$
$ I_{O} $ [3]	Output Leakage for High Impedance Stage			100	μA	$V_O=5.25V$ or $0.45V, V_{CC}=5.25V, \overline{CS}_1=\overline{CS}_2=2.4V$
I_{SC} [3-4]	Output Short Circuit Current	-15	-25	-60	mA	$V_{CC}=5.00V, T_A=25^\circ C, V_O=0V$
V_{OH} [3]	Output High Voltage	2.4			V	$I_{OH}=-2.4mA, V_{CC}=4.75V$

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2. This specification only applies to the 3604 family.

3. This specification only applies to the 3624 family.
4. Unmeasured outputs are open during this test.

SCHOTTKY BIPOLAR 3604, 3604-4, 3604L-6, 3624, 3624-4

A. C. Characteristics $V_{CC} = +5V \pm 5\%$, $T_A = 0^\circ C$ to $+75^\circ C$

SYMBOL	PARAMETER	MAX. LIMIT			UNIT	CONDITIONS
		3604 3624	3604-4 3624-4	3604L-6		
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	70	90	90	ns	$\overline{CS}_1 = \overline{CS}_2 = V_{IL}$ and $CS_3 = CS_4 = V_{IH}$ to Select the PROM.
t_{S++}	Chip Select to Output Delay	30	30	30	ns	
t_{S--}	Chip Select to Output Delay	30	30	120	ns	

Capacitance ⁽¹⁾ $T_A = 25^\circ C$, $f = 1$ MHz

SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS
		TYP.	MAX.		
C_{INA}	Address Input Capacitance	4	10	pF	$V_{CC} = 5V$ $V_{IN} = 2.5V$
C_{INS}	Chip-Select Input Capacitance	6	10	pF	$V_{CC} = 5V$ $V_{IN} = 2.5V$
C_{OUT}	Output Capacitance	7	15	pF	$V_{CC} = 5V$ $V_{OUT} = 2.5V$

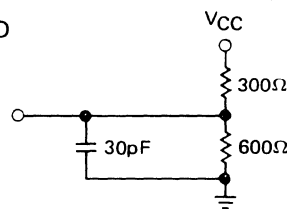
NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

Conditions of Test:

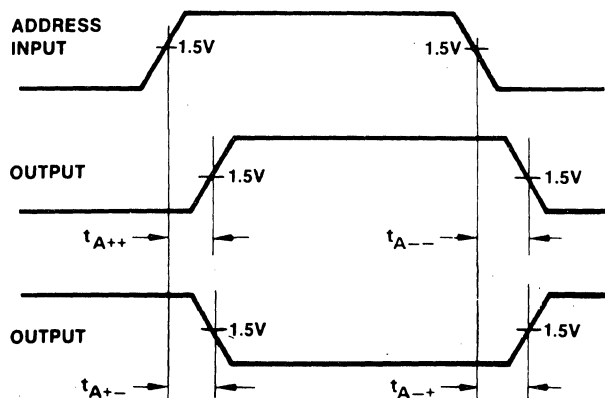
Input pulse amplitudes - 2.5V
 Input pulse rise and fall times of
 5 nanoseconds between 1 volt and 2 volts
 Speed measurements are made at 1.5 volt levels
 Output loading is 15 mA and 30 pF
 Frequency of test - 2.5 MHz

15 mA TEST LOAD

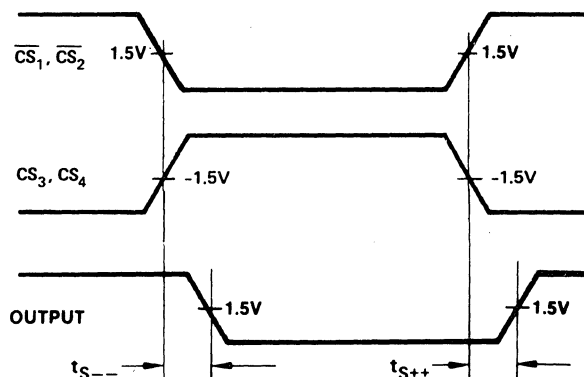


Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY





Silicon Gate MOS 2107B, 2107B-2, 2107B-4, 2107B-6

4096 BIT DYNAMIC RAM

	2107B	2107B-2	2107B-4	2107B-6
Access Time	200ns	220ns	270ns	350ns
Read,Write Cycle	400ns	470ns	470ns	800ns
RMW Cycle	520ns	680ns	590ns	960ns

- Low Cost Per Bit
 - Low Standby Power
 - Easy System Interface
 - Only One High Voltage Input Signal — Chip Enable
 - TTL Compatible — All Address, Data, Write Enable, Chip Select Inputs
 - Refresh Period — 2ms for 2107B, 2107B-2, 2107B-4, 1ms for 2107B-6
- Address Registers Incorporated on the Chip
 - Simple Memory Expansion — Chip Select Input Lead
 - Fully Decoded — On Chip Address Decode
 - Output is Three State and TTL Compatible
 - Industry Standard 22-Pin Configuration

The Intel[®]2107B is a 4096 word by 1 bit dynamic n-channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. The 2107B uses dynamic circuitry which reduces the standby power dissipation.

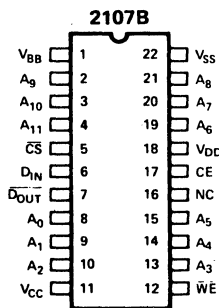
Reading information from the memory is non-destructive. Refreshing is most easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic one or a logic zero.

The 2107B is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than other MOS technologies. The 2107B uses a single transistor cell to achieve high speed and low cost. It is a replacement for the 2107A.

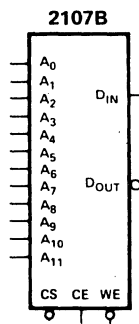
Intel

MEMORY

PIN CONFIGURATION



LOGIC SYMBOL

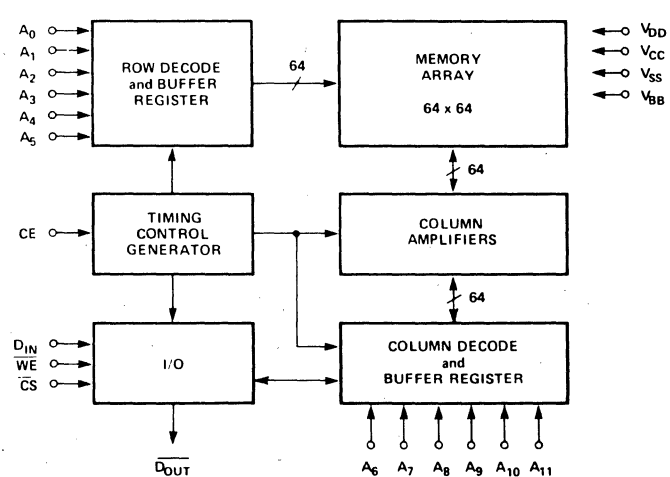


PIN NAMES

A ₀ -A ₁₁	ADDRESS INPUTS*	V _{BB}	POWER (-5V)
CE	CHIP ENABLE	V _{CC}	POWER (+5V)
CS	CHIP SELECT	V _{DD}	POWER (+12V)
D _{IN}	DATA INPUT	V _{SS}	GROUND
D _{OUT}	DATA OUTPUT	WE	WRITE ENABLE
NC	NOT CONNECTED		

*Refresh Address A₀-A₅.

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB}	+25V to -0.3V
Supply Voltages V_{DD} , V_{CC} , and V_{SS} with Respect to V_{BB}	+20V to -0.3V
Power Dissipation	1.25W

***COMMENT:**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = +12\text{V} \pm 5\%$, $V_{CC} = +5\text{V} \pm 10\%$, $V_{BB}^{(1)} = -5\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ. [2]	Max.		
I_{LI}	Input Load Current (all inputs except CE)		.01	10	μA	$V_{IN} = V_{IL\text{ MIN}}$ to $V_{IH\text{ MAX}}$ $CE = V_{ILC}$ or V_{IHC}
I_{LC}	Input Load Current		.01	2	μA	$V_{IN} = V_{IL\text{ MIN}}$ to $V_{IH\text{ MAX}}$
$ I_{LO} $	Output Leakage Current for high impedance state		.01	10	μA	$CE = V_{ILC}$ or $\overline{CS} = V_{IH}$ $V_O = 0\text{V}$ to 5.25V
I_{DD1}	V_{DD} Supply Current during CE off[3]		110	200	μA	$CE = -1\text{V}$ to $+6\text{V}$
I_{DD2}	V_{DD} Supply Current during CE on			60	mA	$CE = V_{IHC}$, $\overline{CS} = V_{IL}$
$I_{DD\text{ AV}}$	Average V_{DD} Current		38	54	mA	$\overline{CS} = V_{IL}$; $T_A = 25^\circ\text{C}$: Min cycle time, Min t_{CE}
I_{CC1} [4]	V_{CC} Supply Current during CE off		.01	10	μA	$CE = V_{ILC}$ or $\overline{CS} = V_{IH}$
I_{BB}	V_{BB} Supply Current		5	100	μA	
V_{IL}	Input Low Voltage	-1.0		0.6	V	$t_T = 20\text{ns}$
V_{IH}	Input High Voltage	2.4		$V_{CC}+1$	V	$t_T = 20\text{ns}$
V_{ILC}	CE Input Low Voltage	-1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	$V_{DD}-1$		$V_{DD}+1$	V	
V_{OL}	Output Low Voltage	0.0		0.45	V	$I_{OL} = 2.0\text{mA}$
V_{OH}	Output High Voltage	2.4		V_{CC}	V	$I_{OH} = -2.0\text{mA}$

NOTES:

- The only requirement for the sequence of applying voltage to the device is that V_{DD} , V_{CC} , and V_{SS} should never be .3V or more negative than V_{BB} .
- Typical values are for $T_A = 25^\circ\text{C}$ and nominal power supply voltages.
- The I_{DD} and I_{CC} currents flow to V_{SS} . The I_{BB} current is the sum of all leakage currents.
- During CE on V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

SILICON GATE MOS 2107B, 2107B-2, 2107B-4, 2107B-6

A. C. Characteristics $T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 12\text{V} \pm 5\%$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{BB} = -5\text{V} \pm 5\%$,

READ, WRITE, AND READ MODIFY/WRITE CYCLE $V_{SS} = 0\text{V}$, unless otherwise noted.

Symbol	Parameter	2107B		2107B-2		2107B-4		2107B-6		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{REF}	Time Between Refresh		2		2		2		1	ms	
t_{AC}	Address to CE Set Up Time	0		0		0		10		ns	3
t_{AH}	Address Hold Time	100		150		100		100		ns	
t_{CC}	CE Off Time	130		150		130		380		ns	
t_T	CE Transition Time	10	40	10	40	10	40	10	40	ns	
t_{CF}	CE Off to Output High Impedance State	0		0		0		0		ns	

READ CYCLE

Symbol	Parameter	2107B		2107B-2		2107B-4		2107B-6		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{CY}	Cycle Time	400		470		470		800		ns	4
t_{CE}	CE On Time	230	4000	280	4000	300	4000	380	4000	ns	
t_{CO}	CE Output Delay		180		200		250		320	ns	5
t_{ACC}	Address to Output Access		200		220		270		350	ns	6
t_{WL}	CE to \overline{WE}	0		0		0		0		ns	
t_{WC}	\overline{WE} to CE on	0		0		0		0		ns	

WRITE CYCLE

Symbol	Parameter	2107B		2107B-2		2107B-4		2107B-6		Units	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{CY}	Cycle Time	400		470		470		800		ns	4
t_{CE}	CE On Time	230	4000	280	4000	300	4000	380	4000	ns	
t_W	\overline{WE} to CE Off	150		140		150		200		ns	
t_{CW}	CE to \overline{WE}	150		150		150		150		ns	
t_{DW}	D_{IN} to \overline{WE} Set Up	0		0		0		0		ns	1
t_{DH}	D_{IN} Hold Time	0		0		0		0		ns	
t_{WP}	\overline{WE} Pulse Width	50		100		50		100		ns	

Capacitance ^[2] $T_A = 25^\circ\text{C}$

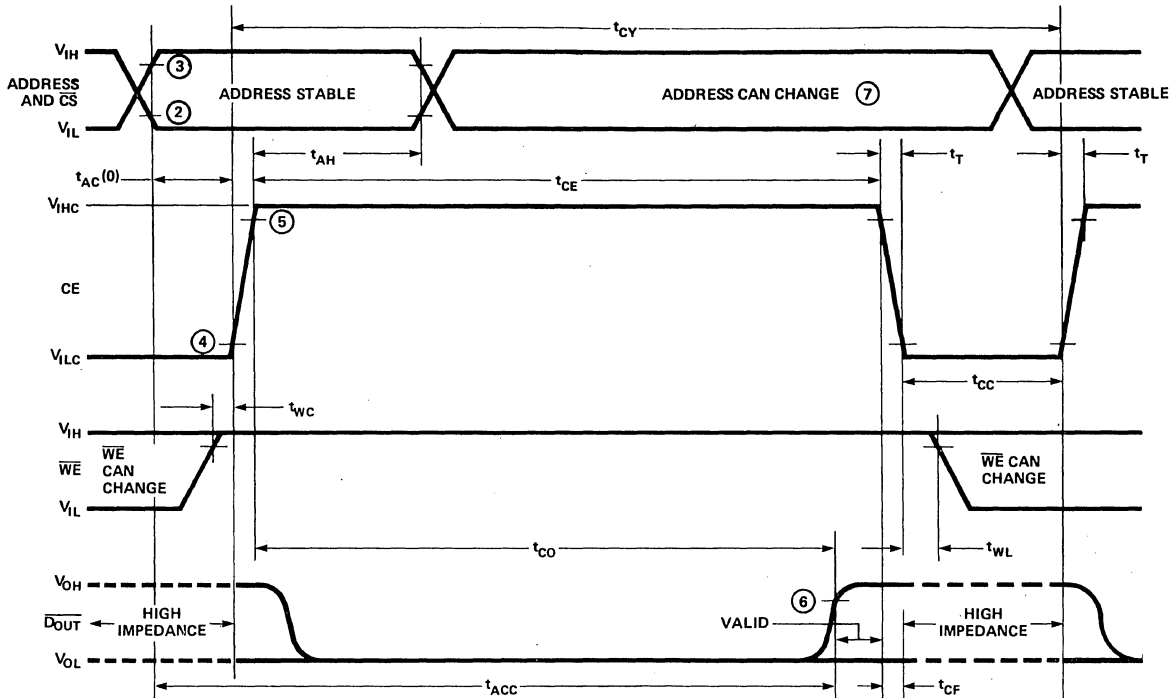
Symbol	Test	Plastic And Ceramic Pkg.		Unit	Conditions
		Typ.	Max.		
C_{AD}	Address Capacitance, \overline{CS}	4	6	pF	$V_{IN} = V_{SS}$
C_{CE}	CE Capacitance	17	25	pF	$V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance	5	7	pF	$V_{OUT} = 0\text{V}$
C_{IN}	D_{IN} and \overline{WE} Capacitance	8	10	pF	$V_{IN} = V_{SS}$

- Notes: 1. If \overline{WE} is low before CE goes high then D_{IN} must be valid when CE goes high.
 2. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation.

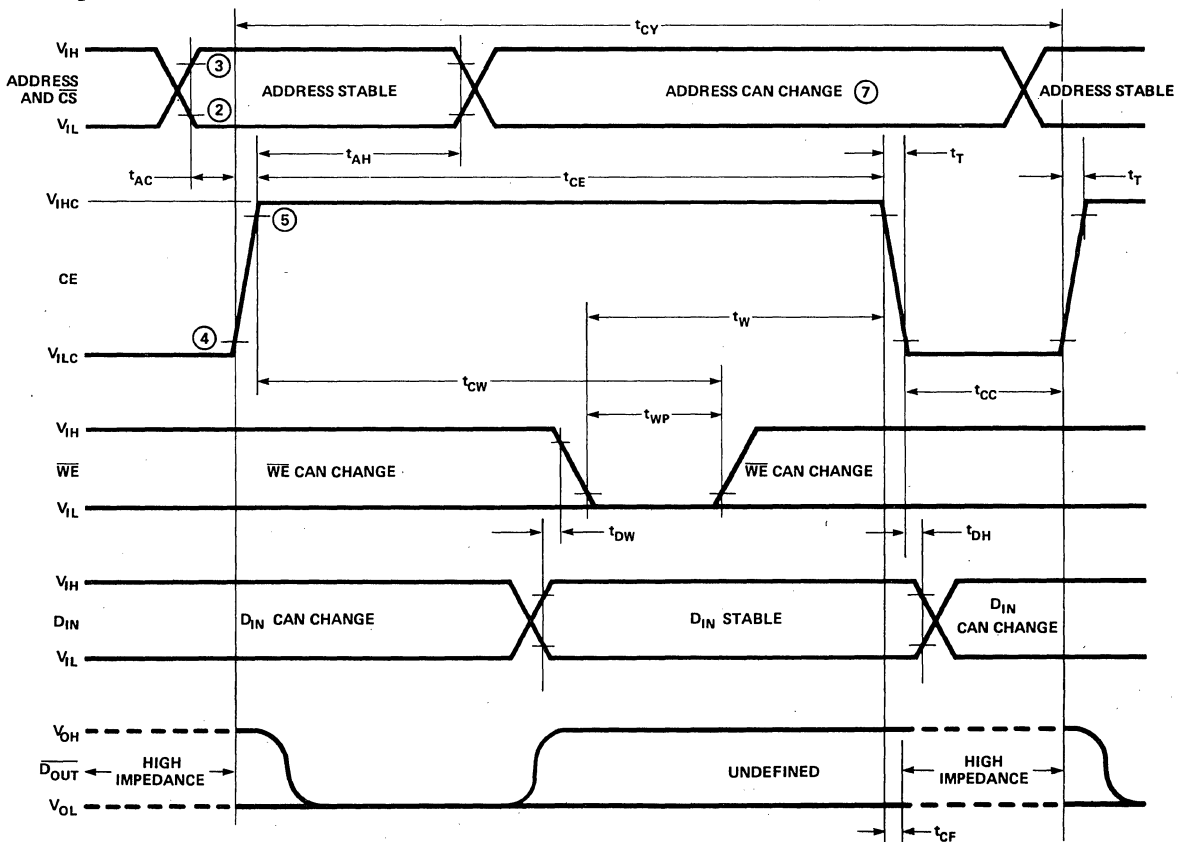
$$C = \frac{I \Delta t}{\Delta V} \text{ with the current equal to a constant } 20\text{mA.}$$

3. t_{AC} is measured from end of address transition.
 4. $t_T = 20\text{ns}$
 5. $C_{LOAD} = 50\text{pF}$, Load = One TTL Gate, Ref = 2.0V.
 6. $t_{ACC} = t_{AC} + t_{CO} + 1t_T$

Read and Refresh Cycle ^[1]



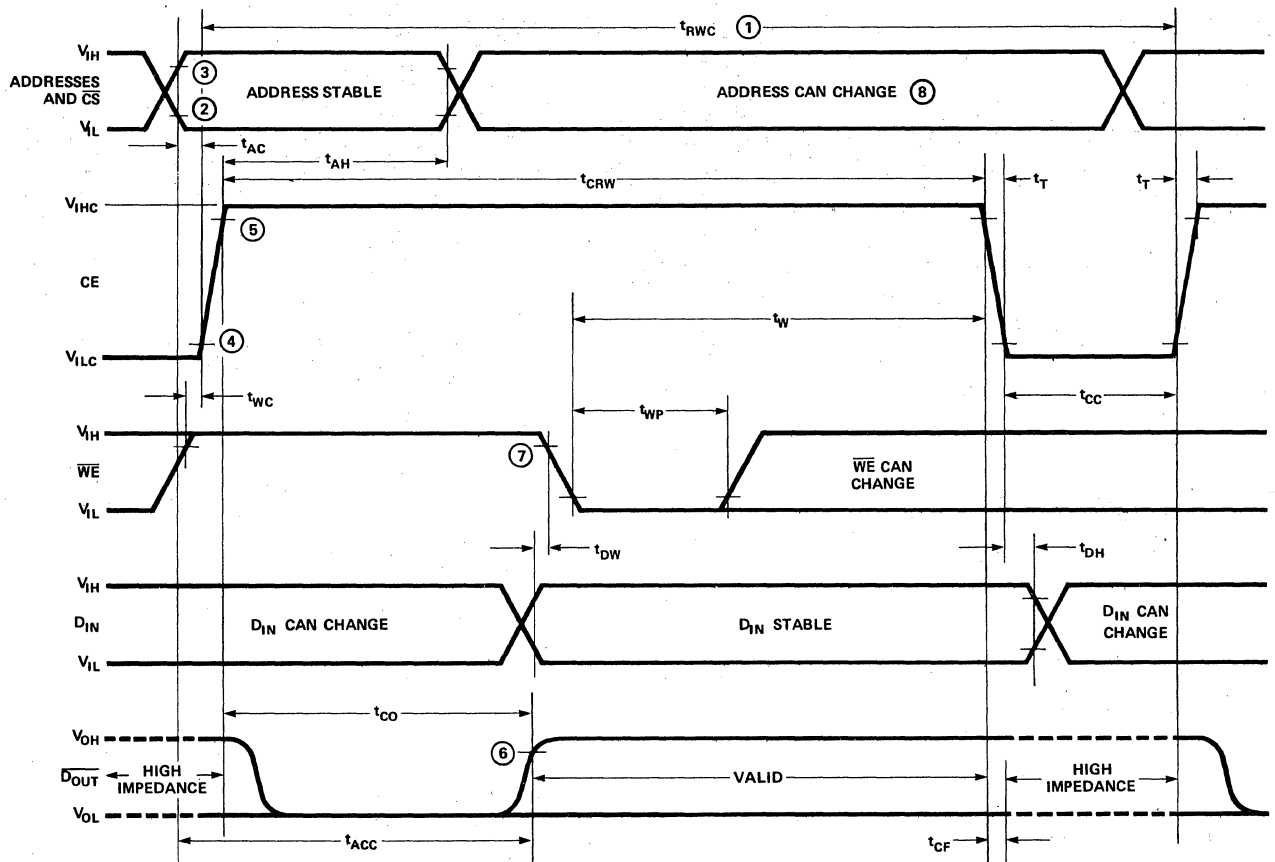
Write Cycle



- NOTES:
1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
 2. V_{IL} MAX is the reference level for measuring timing of the addresses, CS, WE, and D_{IN}.
 3. V_{IH} MIN is the reference level for measuring timing of the addresses, CS, WE, and D_{IN}.
 4. V_{SS} +2.0V is the reference level for measuring timing of CE.
 5. V_{DD} -2V is the reference level for measuring timing of CE.
 6. V_{SS} +2.0V is the reference level for measuring the timing of D_{OUT}.
 7. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

Read Modify Write Cycle ^[1]

Symbol	Parameter	2107B		2107B-2		2107B-4		2107B-6		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RWC}	Read Modify Write (RMW) Cycle Time	520		680		590		960		ns
t_{CRW}	CE Width During RMW	350	4000	490	4000	420	4000	540	3000	ns
t_{WC}	\overline{WE} to CE on	0		0		0		0		ns
t_W	\overline{WE} to CE off	150		140		150		200		ns
t_{WP}	\overline{WE} Pulse Width	50		100		50		100		ns
t_{DW}	D_{IN} to \overline{WE} Set Up	0		0		0		0		ns
t_{DH}	D_{IN} Hold Time	0		0		0		0		ns
t_{CO}	CE to Output Delay		180		200		250		320	ns
t_{ACC}	Access Time ($t_{ACC} = t_{AC} + t_{CO} + 1t_T$)		200		220		270		350	ns



- NOTES:
1. Minimum cycle timing is based on t_T of 20ns.
 2. V_{IL} MAX is the reference level for measuring timing of the addresses, \overline{CS} , \overline{WE} , and D_{IN} .
 3. V_{IH} MIN is the reference level for measuring timing of the addresses, \overline{CS} , \overline{WE} , and D_{IN} .
 4. $V_{SS} + 2.0V$ is the reference level for measuring timing of CE.
 5. $V_{DD} - 2V$ is the reference level for measuring timing of CE.
 6. $V_{SS} + 2.0V$ is the reference level for measuring the timing of $\overline{D_{OUT}}$. $C_{LOAD} = 50pF$. Load = One TTL Gate.
 7. \overline{WE} must be at V_{IH} until end of t_{CO} .
 8. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

Intel

MEMORY

Typical Characteristics

Fig. 1. I_{DD} AV VS. TEMPERATURE

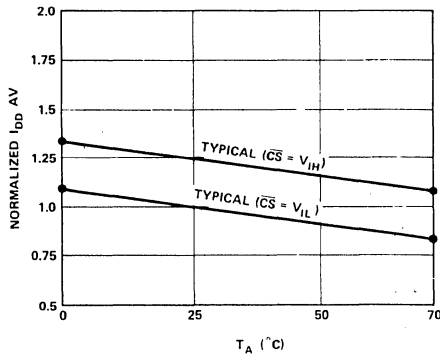


Fig. 2. TYPICAL I_{DD} AVERAGE VS. CYCLE TIME

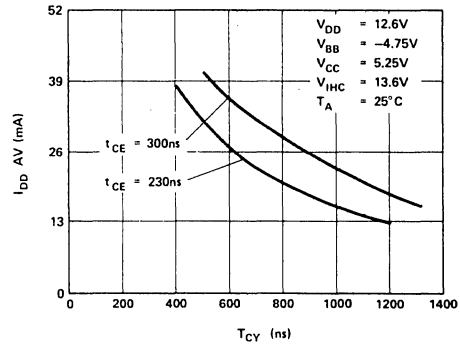


Fig. 3. I_{DD2} VS. TEMPERATURE

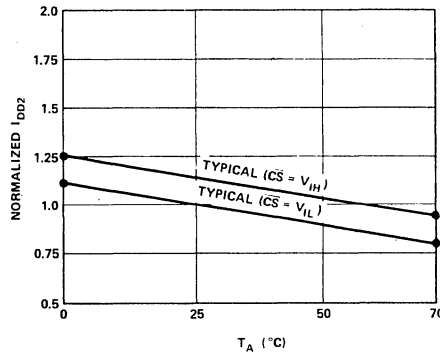
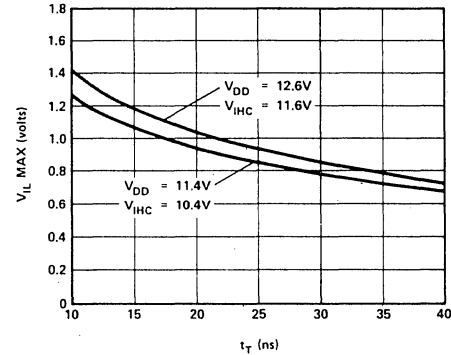
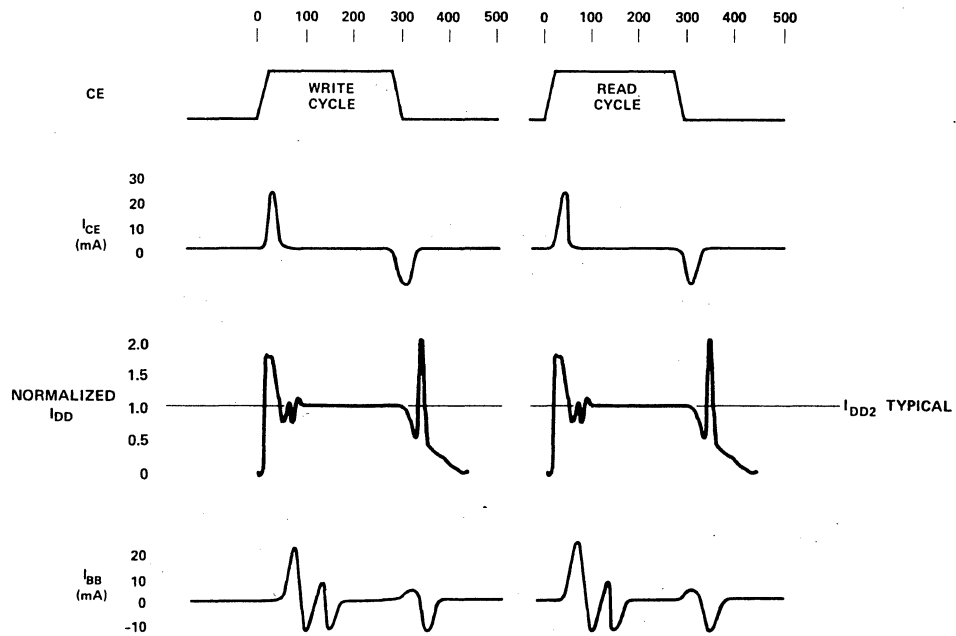


Fig. 4. TYPICAL V_{IL} MAX VS. CE RISE TIME



Typical Current Transients vs. Time



For additional typical characteristics and applications information please refer to Intel Application Note AP-10, "Memory System Design With the Intel 2107B 4K RAM" or Intel's Memory Design Handbook.

MOSTEK'S MEMORIES

MK 4096 P / 4096 x 1 Bit Dynamic Random Access Memory

FEATURES:

- Standard 16-pin DIP
- All inputs TTL compatible
- On-chip latches for addresses, chip select, and data in
- Three-State TTL compatible output
- Chip select decode does not add to access time
- Output data latched and valid into next cycle
- Read and write cycles of 375 nsec (-6)
425 nsec (-16), and 500 nsec (-11)
- Access times of 250 nsec (-6), 300 nsec (-16),
350 nsec (-11)
- Low power: active power under 380 mW (-16)
standby power under 24 mW

DESCRIPTION:

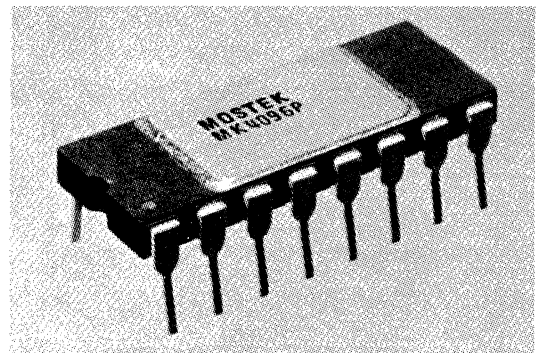
The MK 4096 is a 4096 x 1 bit dynamic random access memory circuit fabricated with MOSTEK's special Self-Aligned, Poly-Interconnect, N-Channel (SPIN) process to minimize cell area and optimize circuit performance. The single transistor cell uses a dynamic storage technique and each of the 64 row addresses requires refreshing every 2 milliseconds.

A unique multiplexing and latching technique for the address inputs permits the MK 4096 to be packaged in a standard 16-pin DIP on 0.3 inch centers. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

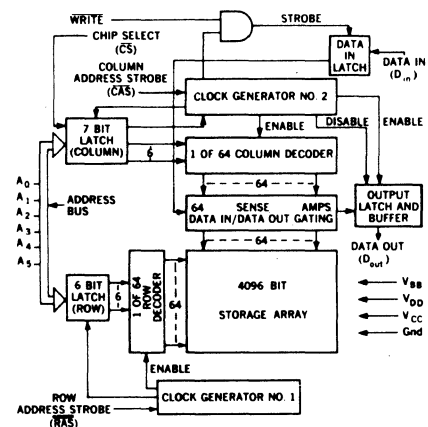
System oriented features on the MK 4096 include direct interfacing capability with TTL, 6 instead of 12 address lines to drive, on-chip registers which can eliminate the need for interface registers, input logic levels selected to optimize the noise immunity, and two chip select methods to allow the user to determine the speed/power characteristics of his memory system.

ADDRESSING:

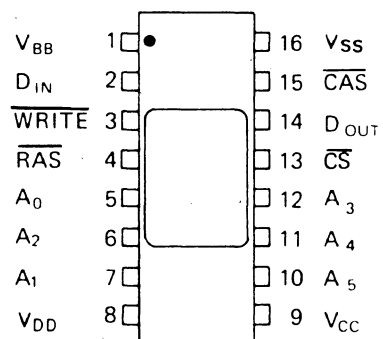
The 12 address bits required to decode 1 of 4096 cell locations are multiplexed onto the 6 address pins and latched into the on-chip row and column address latches. The Row Address Strobe (RAS) latches the 6 row address bits into the chip. The Column Address Strobe (CAS) latches the 6 column address bits plus Chip Select (CS) into the chip. Since the Chip Select signal is not required until well into the cycle, its decoding time does not add to the system access or cycle time.



FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB}	-0.5V to +25.0V
Operating Temperature T_A (Ambient)	0°C to 70°C
Storage Temperature (Ambient)	-55°C to 150°C

RECOMMENDED DC OPERATING CONDITIONS

(0° ≤ T_A ≤ 70°C)

	PARAMETER	MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage	11.4	12.0	12.6	volts
V_{CC}	Supply Voltage	V_{SS}	5.0	V_{DD}	volts
V_{SS}	Supply Voltage	0	0	0	volts
V_{BB}	Supply Voltage	-4.5	-5.0	-5.5	volts
V_{IH}	Logic 1 Voltage all inputs except RAS, CAS WRITE	2.4	5.0	7.0	volts
V_{IL}	Logic 0 voltage, all inputs	-1.0	0	.8	volts
V_{IHC}	Logic 1 Voltage RAS, CAS, WRITE	2.7	5.0	7.0	volts

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) ($V_{DD} = 12.0V \pm 5\%$; $V_{CC} = 5.0V \pm 10\%$; $V_{SS} = 0V$, $V_{BB} = -5.0V \pm 10\%$)

	PART NUMBER	4096-6		4096-11/16		UNITS
		MIN	MAX	MIN	MAX	
I_{DD1}	Average V_{DD} Power Supply Current		35		30	mA
I_{CC}	V_{CC} Power Supply Current					mA
I_{BB}	Average V_{BB} Power Supply Current		75		75	μA
I_{DD2}	Standby V_{DD} Power Supply Current		2		2	mA
$I_{I(L)}$	Input Leakage Current (any input)		10		10	μA
$I_{O(L)}$	Output Leakage Current		10		10	μA
V_{OH}	Output Logic 1 Voltage @ $I_{out} = -5$ mA	2.4		2.4		volts
V_{OL}	Output Logic 0 Voltage @ $I_{out} = 2$ mA		0.4		0.4	volts

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C) ($V_{DD} = 12.0V \pm 5\%$; $V_{CC} = 5.0V \pm 10\%$; $V_{SS} = 0V$, $V_{BB} = -5.0V \pm 10\%$)

	PART NUMBER	4096-6		4096-16		4096-11		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random Read or Write Cycle Time	375		425		500		nsec
t_{RAC}	Access Time from Row Address Strobe		250		300		350	nsec
t_{CAC}	Access Time from Column Address Strobe		140		165		200	nsec

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of WRITE and CAS. The last of these signals making its negative transition is the strobe for the Data In register. This permits several options in the write timing. In a write cycle, if the WRITE input is brought low prior to CAS, the Data In is strobed by CAS and the set-up and hold time are referenced to this signal. If the cycle is to be a read-write cycle, or read-modify-write cycle, then the WRITE input will not go to a logic 0 until after access time. But now, because CAS is already at a logic 0, the Data In is strobed in by WRITE and the set-up and hold time are referenced to it.

At the beginning of a memory cycle the state of the Data Out Latch and buffer depend on the previous memory cycle. If during the pervious cycle the chip was unselected, the output buffer will be in its open-circuit condition. If the previous cycle was a read, read-write, or read-modify-write cycle and the chip was selected, then the output latch and buffer will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the previous cycle was a write cycle (WRITE active low before access time) and the chip was selected, then the output latch and buffer will contain a logic 1. Regardless of the state of the output it will remain valid until CAS goes negative. At that time the output will unconditionally go to its open-circuit state. It will remain open circuit until access time. At access time the output will assume the proper state for the type of cycle performed. If the chip is unselected, it will not accept a WRITE command and the output will remain in the open-circuit state.

INPUT/OUTPUT LEVELS

All inputs, including the two address strobes, will interface with TTL. The high impedance, low capacitance input characteristics simplify input driver selection by allowing use of standard logic elements rather than specially designed driver elements. Even though the inputs may be driven directly by TTL gates, pull-up or termination resistors are normally required in a system to prevent ringing of the input signals due to line inductance and reflections. In high speed memory systems, transmission line techniques must be employed on the signal lines to achieve optimum system speeds. Series rather than parallel terminations may be employed at some degradation of system speed.

The three-state output buffer is a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The resistance to V_{CC} is 500-ohms maximum and 150-ohms ty-

pically. The resistance to V_{SS} is 200-ohms maximum and 100-ohms typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery stand-by operation, the V_{CC} pin may be unpowered without affecting the MK 4096P refresh operation. This allows all system logic except the RAS/CAS timing circuitry and the refresh address logic to be turned off during battery stand-by to conserve power.

REFRESH

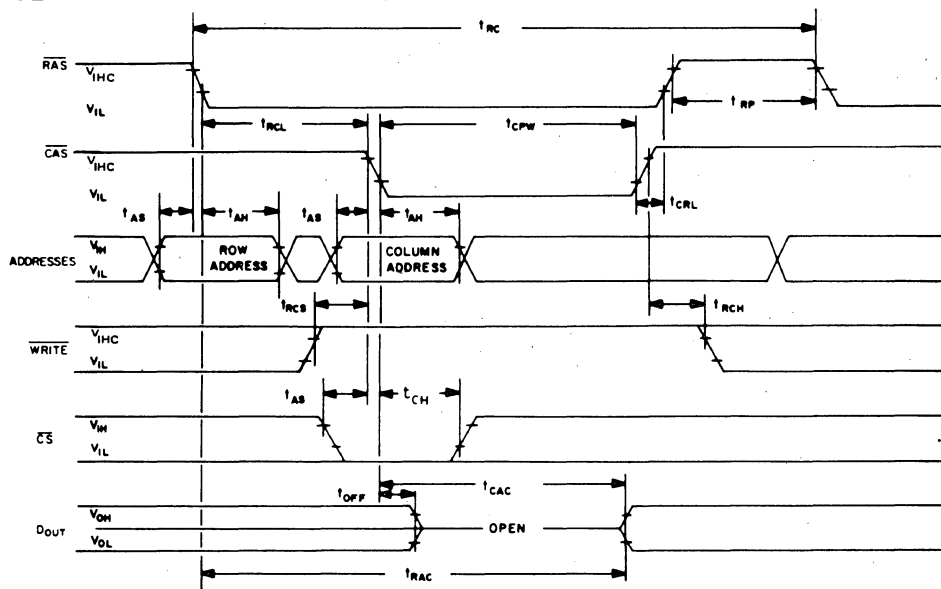
Refresh of the cell matrix is accomplished by performing a memory cycle at each 64 row addresses every 2 milliseconds or less. Any read cycle refreshes the selected row, regardless of the state of the Chip Select. A write, read-write, or read-modify-write cycle also refreshes the selected row but the chip should be unselected to prevent writing data into the selected cell.

POWER DISSIPATION/STANDBY MODE

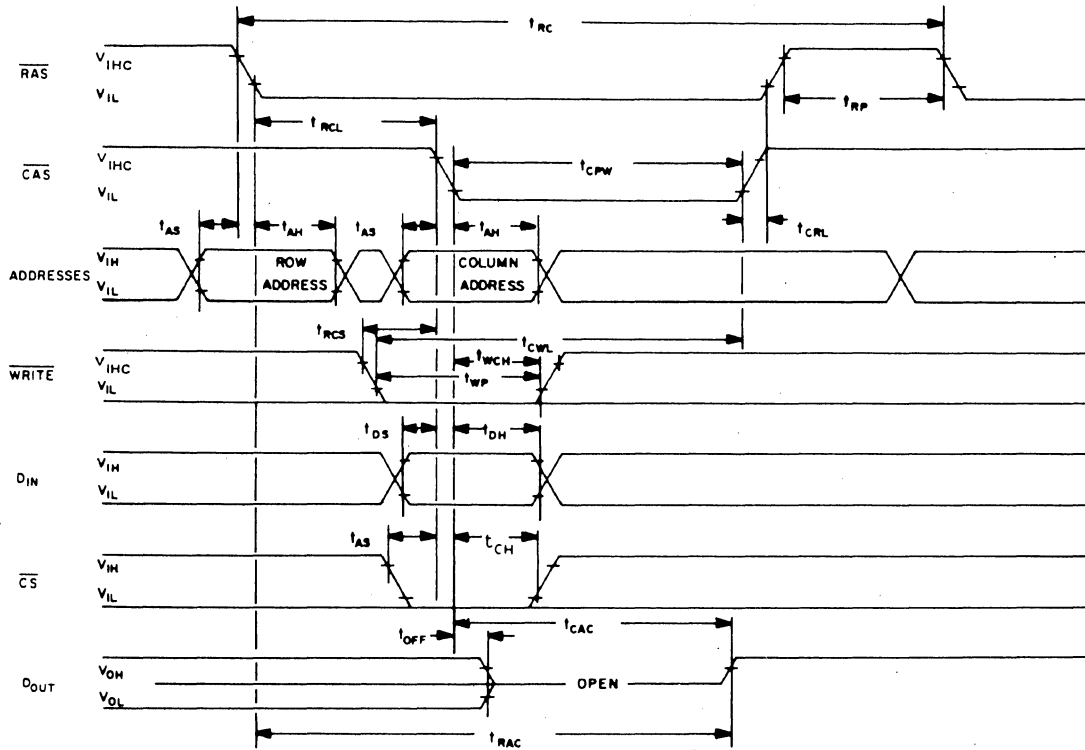
Most of the circuitry used in the MK 4096P is dynamic and draws power only as the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency. Typically, the power is 120mW at a 1 μ sec cycle time for the MK 4096P; with a worst case power of less than 380mW at a 425 nsec cycle time. To reduce the overall system power the Row Address Strobe (RAS) must be decoded and supplied to only the selected chips. The CAS must be supplied to all chips (to turn off the unselected outputs). But those chips that did not receive a RAS will not dissipate any power on the CAS edges, except for that required to turn off the output. If the RAS is decoded and supplied to the selected chips, then the Chip Select input of all chips can be at a logic 0. The chips that receive a CAS but no RAS will be unselected (output open-circuited) regardless of the Chip Select input.

The current waveforms for the current drawn from the V_{DD} and V_{BB} supplies are pulsed and proper power distribution and bypassing techniques are required to maintain system power supply noise levels at an acceptable level. Low inductance supply lines for V_{DD} and V_{SS} are desirable. A minimum of one 0.01 microfarad low inductance bypass capacitance per two MK 4096P devices and one 6.8 microfarad electrolytic capacitor per eight MK 4096P devices on each of the V_{DD} and V_{BB} supply lines is desirable. A noise level of less than 0.5 volts peak-to-peak on both V_{DD} and V_{BB} should be a design goal.

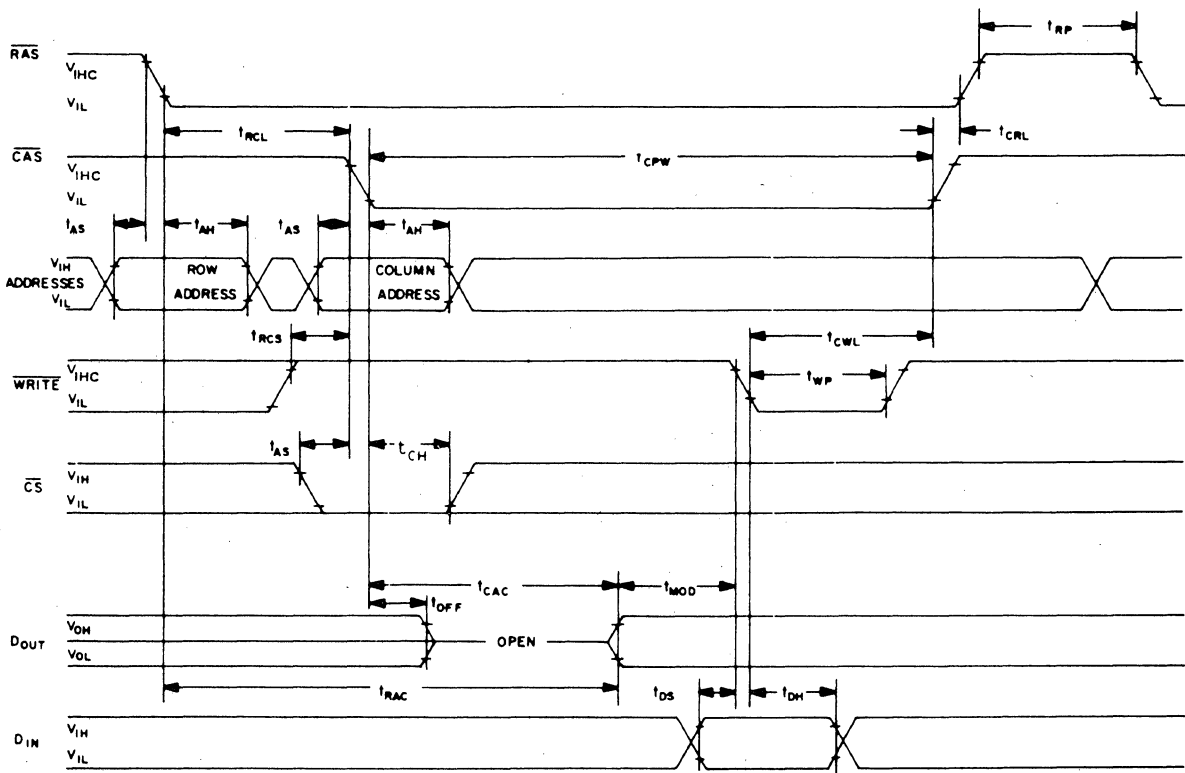
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



MK 4200 P-16/MK 4200 P-11

4096 x 1 Bit Dynamic

MOS Random Access Memory

Low Standby Power

FEATURES:

- Standard 16-pin DIP
- Inputs protected against static charge
- All inputs TTL compatible, except RAS
- On-chip latches for addresses, chip select, and data in
- Three-state TTL compatible output
- Chip select decode does not add to access time
- Output data latched and valid into next cycle
- Read and write cycles of 500 nsec (-11) 425 nsec (-16)
- Access times of 350 nsec (-11) 300 nsec (-16)
- Low power: active power under 300mW (-11)
standby power under .6mW

DESCRIPTION:

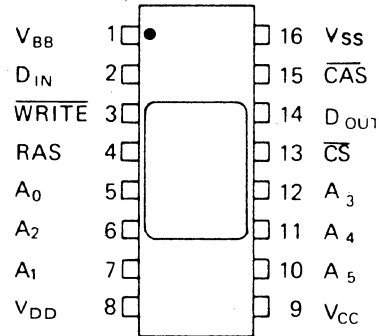
The MK 4200 is a 4096 x 1 bit dynamic random access memory circuit fabricated with MOSTEK's special Self-Aligned, Poly-Interconnect, N-Channel (SPIN) process to minimize cell area and optimize circuit performance. The single transistor cell uses a dynamic storage technique and each of the 64 row addresses requires refreshing every 2 milliseconds.

A unique multiplexing and latching technique for the address inputs permits the MK 4200 to be packaged in a standard 16-pin DIP on 0.3 each centers. This package size pro-

vides high system bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features on the MK 4200 include very low standby power dissipation, direct interfacing capability with TTL, 6 instead of 12 address lines to drive, on-chip registers input logic levels selected to optimize the noise immunity, and two chip select methods to allow the user to determine the speed/power characteristics of his memory system.

PIN CONNECTIONS



MK 28000 P/16K-Bit

MOS Read-Only Memory

FEATURES:

- 600 ns Maximum Access Time
- Low Power-Dissipation
Active—0.01 mW/bit Typ.
Inactive—.003 mW/bit Typ.
- EA 4900 and EA 4800 Hi-performance Replacement
- 100 μ sec Minimum Output Data Hold Time
- 2K x 8 or 4K x 4 organization with Open Drain Outputs
- Standard Supplies +5 volts, -12 volts
- Ion-Implanted for Full TTL/DTL Compatibility

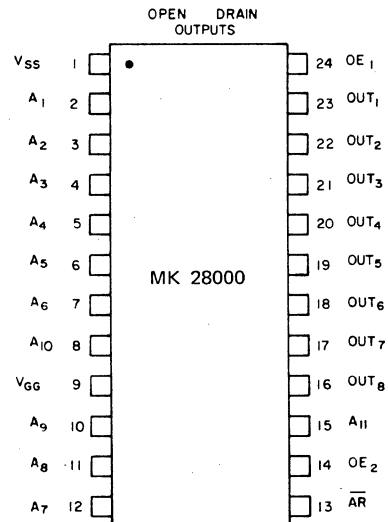
DESCRIPTION:

The MK 28000 is a mask programmable read only memory utilizing low-threshold Ion-Implant P-Channel technology. The MK 28000 is a Hi-performance replacement for the EA 4900. The MK 28000 may be organized as either a 2K x 8 or 4K x 4 memory.

The MK 28000 open drain outputs are divided into two groups with one Output Enable line controlling each group of outputs. This feature allows the MK 28000 to be either a 2K x 8 or a 4K x 4 memory without any internal mask changes. For a 2K x 8 organization, the Output Enables (OE₁, OE₂) are tied together. For a 4K x 4 organization, the four outputs associated with OE₁ are wire-ORed to the four outputs associated with OE₂. OE₁ and OE₂ are inverted with respect to each other and used as the twelfth address input in the 4K x 4 organization.

The internal circuitry of the MK 28000 is dynamic. This feature means low standby power consumption when the ROM is not being addressed.

PIN CONNECTIONS



All inputs are protected against static charge accumulation. Pullup resistors on all inputs are available as a programmable option.

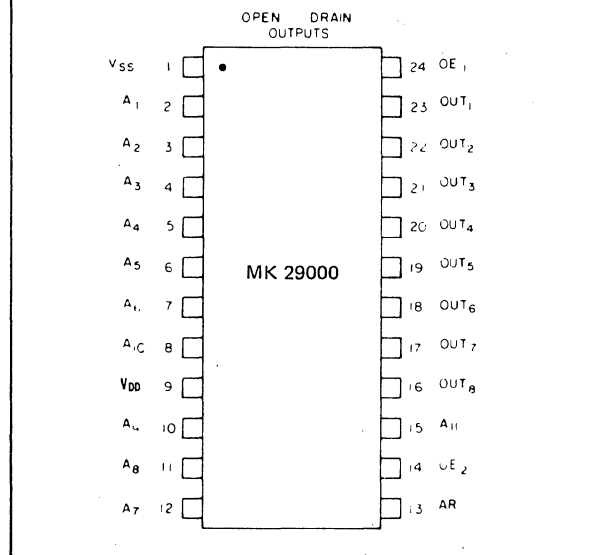
With no address lead time required, system design is simplified; address and AR may appear simultaneously.

MK 29000 P/16K-Bit MOS Read-Only Memory Fast Access Time

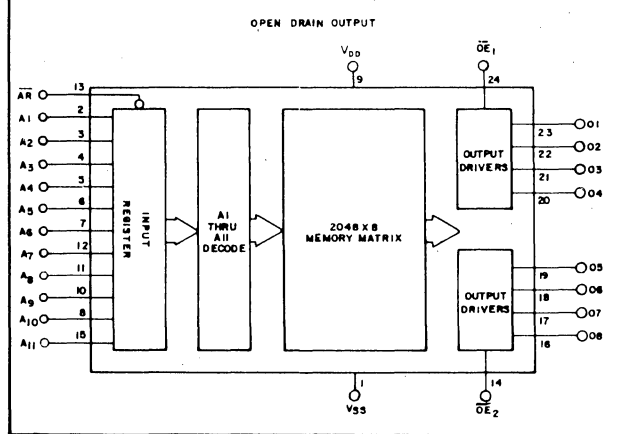
FEATURES:

- Fast Access, Less Than 250 ns Access Time
- Single +12 Volt Power Supply
- 2K x 8 or 4K x 4 Organization With Open-Drain Outputs
- Ion-Implanted for TTL/DTL Compatibility at All Inputs
- Low Power Dissipation
- On-Chip Address Latches

PIN CONFIGURATION



BLOCK DIAGRAM



DESCRIPTION:

The MK 29000 is a mask programmable dynamic, read only memory circuit fabricated with MOSTEK's special Self-Aligned, N-Channel, Metal Gate process to minimize chip size and optimize circuit performance. The MK 29000 is the first of a series of high performance ROM circuits designed to be competitive with many bipolar ROMs in speed, but excel in power dissipation and bit density. The timing requirements for the MK 29000 are such that the part will fit right into many high performance memory systems. The RAS and precharge timing requirements for the MK 4096, 4K dynamic RAM are identical to the AR and precharge requirements of the MK 29000.

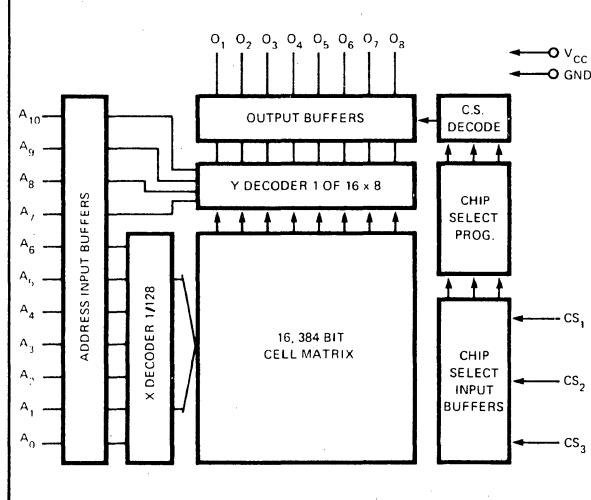
The MK 29001 is a preprogrammed version of the MK 29000 containing six character conversion codes (ASCII to Selectric, EBCDIC, and a modified 8-bit Hollerith>Selectric to ASCII, EBCDIC to ASCII, and a modified Hollerith to ASCII) as well as 128 USASCII characters using mixed character fonts of 5 x 7 and 7 x 7 dot matrices with extra check bits.

MK 31000 P/16K-Bit MOS Read-Only Memory

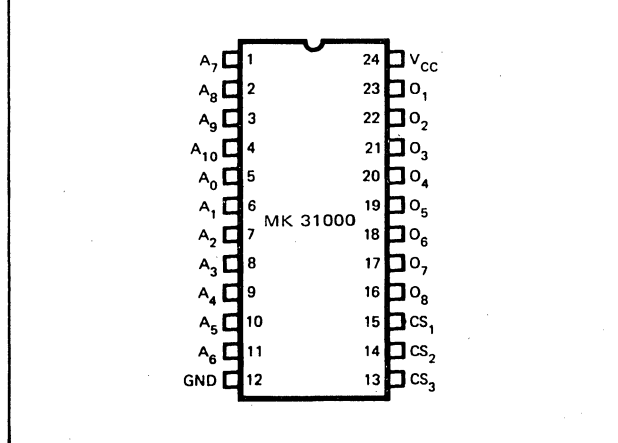
FEATURES:

- Single +5 volt power supply
- Completely static operation (no clocks required)
- Less than 600 ns Access Time
- Directly TTL compatible
- Three programmable chip select inputs
- Input protection against static charge

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



DESCRIPTION:

The MK 31000 is a 16,384 bit read only memory circuit designed as a high performance replacement for the INTEL 2316. The internal organization of the MK31000 is arranged as a 2K x 8 matrix to allow simple interface with eight-bit processor applications. The static operation of the MK 31000 coupled with three programmable chip select inputs provide an easily expandable, high performance memory circuit with extremely simple interface requirements.

The MK 31000 read only memory is fabricated with N-Channel silicon gate technology to minimize chip size and optimize circuit performance. Ion implantation allows TTL compatibility at both the inputs and the outputs.

RCA-MWS5001D SOS 1024-Bit COS/MOS LSI Static Random Access Memory

The RCA-MWS5001D is a 1024-word by 1-bit static random access memory designed for use in memory systems where high speed, low power, and ease of use are primary design requirements. These characteristics are obtained primarily from the use of self-aligned silicon-gate COS/MOS SOS technology.

The output state of the MWS5001D is a function of the input address and chip-select states only. Valid data will appear at the output in one access time following the latest address change to a selected chip. After valid data appears, the address may

then be changed immediately. It is not necessary to clock the chip select input or any other input terminal for fully static operation, therefore the chip select input may be used as an additional address input. When the device is in an unselected state ($\overline{CS}=1$), the internal write circuitry and output sense amplifier are disabled. This feature allows the three-state data outputs from many arrays to be OR-tied to a common bus for ease of memory expansion.

The MWS5001 is supplied in a hermetically sealed 16-lead dual-in-line ceramic package (D suffix) or in chip form (H suffix).

MAXIMUM RATINGS,

Absolute-Maximum Values:

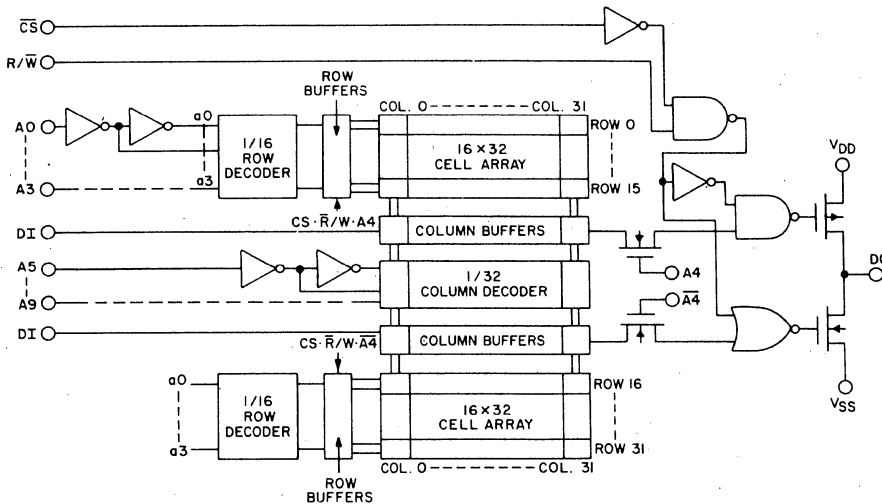
STORAGE TEMPERATURE RANGE	-65 to +150°C
OPERATING TEMPERATURE RANGE	-20 to +85°C
DC SUPPLY VOLTAGE RANGE	
($V_{DD}-V_{SS}$)	-0.5 to +6 V
ALL INPUTS	$V_{SS} \leq V_I \leq V_{DD}$
RECOMMENDED DC SUPPLY VOLTAGE	
($V_{DD}-V_{SS}$)	4.5 to 6 V
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch	
(1.59 ± 0.79 mm) from case	
for 10 seconds max.	265°C

Features:

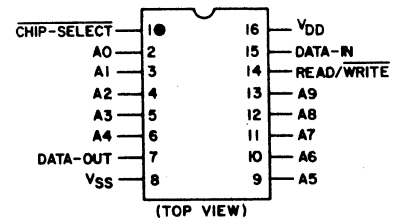
- Organization—1024 words by 1 bit
- Fully static operation—no external clocks required
- Access time—150 ns (typ.) @ $V_{DD} = 5 V$
- Cycle time—160 ns (typ.) @ $V_{DD} = 5 V$
- Low power dissipation:
 - 0.1 μW /Bit (typ.) standby @ $V_{DD} = 5 V$
 - 4 μW /Bit (typ.) operating @ $V_{DD} = 5 V$
- Operation from a single power supply— $V_{DD} = 4.5$ to 6 V
- High noise immunity—30% of V_{DD} (typ.)
- TTL output drive capability
- Three-state data output for bus-oriented systems

RCA Solid State

MEMORY



Functional block diagram.



92C5-27030

Terminal Assignment

92CM-27031

CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES	UNITS	
		V_O (V)			
Quiescent Device Current* I_L			20	μA	
Quiescent Device Dissipation* P_D			100	μW	
Output Voltage:					
Low Level	V_{OL}		0.01	V	
High Level	V_{OH}		4.99	V	
Noise Immunity	V_{NL}	All Inputs	3.6	V	
	V_{NH}	All Inputs	1.4	V	
Output Drive Current:					
N-Channel (Sink)	I_{DN}	Data Output (Sink)	0.4	2	mA
P-Channel (Source)	I_{DP}	Data Output (Source)	4.6	1	mA
Data Output Off-Resistance	$R_{O(Off)}$	Data Output High Impedance State	5	$\text{M}\Omega$	
Input Current	I_I	Any Input	1	nA	

* Standby current is independent of any input state.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{ V} \pm 5\%$

Input $t_r, t_f = 20\text{ ns}$, and $C_L = 30\text{ pF}$

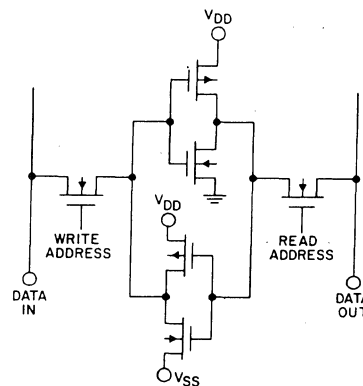
CHARACTERISTIC	TYPICAL VALUES	UNITS
Read Cycle Times:		
Read Access t_{RA}	150	ns
Read Cycle t_{RC}	160	ns
Output Enable t_{EN}	60	ns
Read/Write Hold t_{WH}	50	ns
Read/Write Set-Up t_{WS}	50	ns
Output Disable t_{DIS}	20	ns
Write Cycle Times:		
Write Cycle t_{WC}	160	ns
Read/Write Hold t_{WH}	50	ns
Read/Write Pulse Width t_W	60	ns
Read/Write Set-Up t_{WS}	50	ns
Input Data Set-Up t_{DS}	30	ns
Input Data Hold t_{DH}	30	ns
Read/Modify/Write Cycle Times:		
Read/Modify/Write Cycle t_{MC}	270	ns
Read Hold t_{RH}	160	ns
Read Access t_{RA}	150	ns
Output Enable t_{EN}	60	ns
Read/Write Pulse Width t_W	60	ns
Read/Write Set-Up t_{WS}	50	ns
Input Data Set-Up t_{DS}	30	ns
Input Data Hold t_{DH}	30	ns
Output Disable t_{DIS}	20	ns

TRUTH TABLE

INPUTS		OUTPUT
READ/ WRITE R/W	CHIP- SELECT CS	DATA OUTPUT DO
X	1	High Impedance
0	X	High Impedance
1	0	Contents of Addressed Cell

X = DON'T CARE

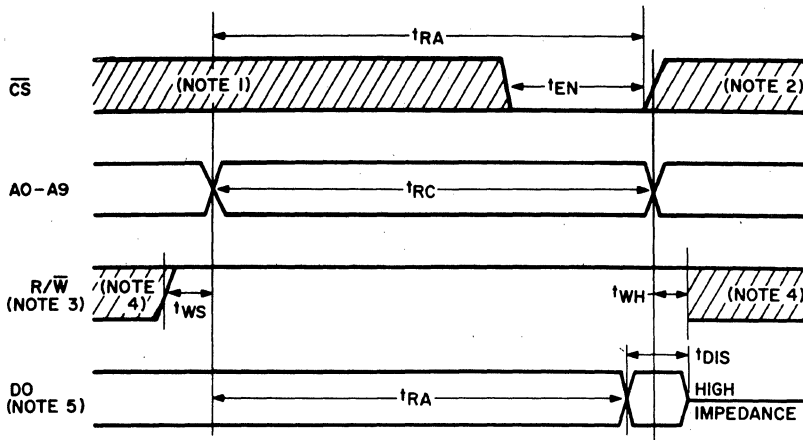
LOGIC 1 \equiv HIGH
LOGIC 0 \equiv LOW



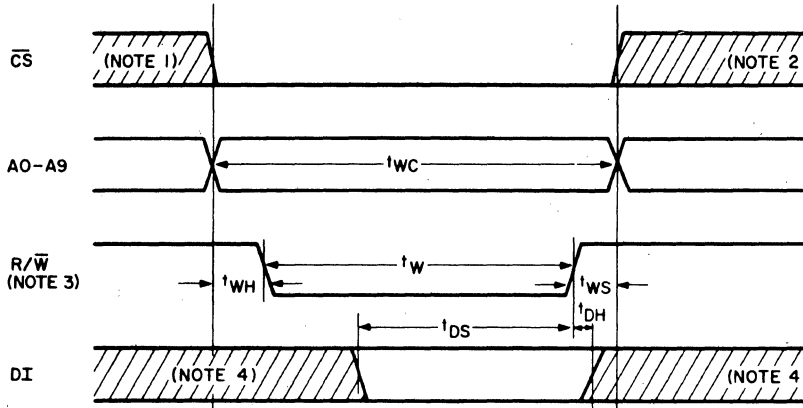
Memory cell configuration.

RCA Solid State

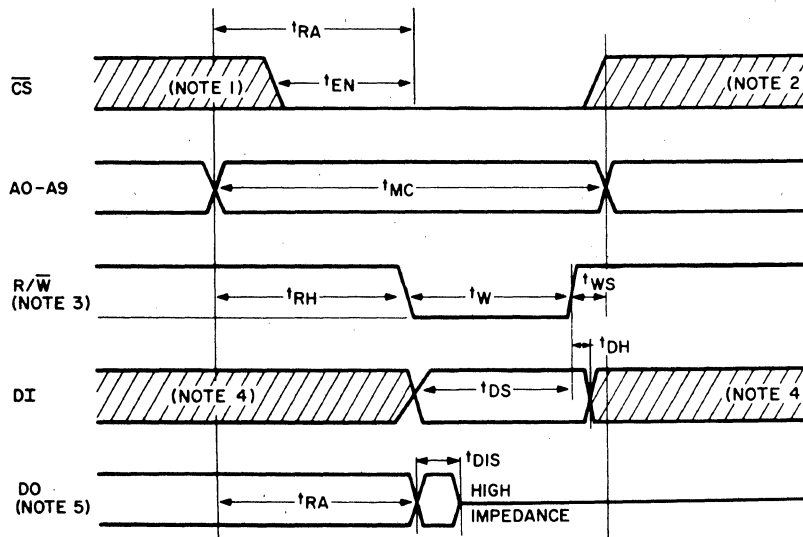
MEMORY



READ-CYCLE WAVEFORMS.



WRITE-CYCLE WAVEFORMS.



READ/MODIFY/WRITE-CYCLE WAVEFORMS.

92CL-27035

Read cycle, write cycle, and read/modify/write cycle waveforms.

- Note 1. Chip-Select (\overline{CS}) permitted to change from high to low level or remain low on a selected device.
- Note 2. Chip-Select (\overline{CS}) permitted to change from low to high level or remain low.
- Note 3. Read/Write (R/\overline{W}) must be at a high level during all address transitions.
- Note 4. Don't care.
- Note 5. Data-Out (DO) is a high impedance within t_{DIS} ns after the falling edge of R/\overline{W} or the rising edge of \overline{CS} .

Other RCA SOS Memories			
MWS501D	1024-Word x 1-Bit Static RAM with Three-State Output	16-lead dual-in-line ceramic package	
Access Time	80 (typ.)	ns	
Power Supply	+10	V	
Operating Power			
Dissipation	20	mW	
MWS5002D	1024-Word x 1-Bit Static RAM with Open-Drain Output	16-lead dual-in-line ceramic package	
Access Time	150 (typ.)	ns	
Power Supply	+5	V	
Operating Power			
Dissipation	3	mW	
MWS502D	1024-Word x 1-Bit Static RAM with Open-Drain Output	16-lead dual-in-line ceramic package	
Access Time	80 (typ.)	ns	
Power Supply	+10	V	
Operating Power			
Dissipation	20	mW	
MWS5040D	256-Word x 4-Bit Static RAM with Three-State Output	22-lead dual-in-line ceramic package	
Access Time	150 (typ.)	ns	
Power Supply	+5	V	
Operating Power			
Dissipation	3	mW	
MWS5540D	256-Word x 4-Bit Static Fully Decoded RAM with Three-State Output	22-lead dual-in-line ceramic package	
Access Time	80 (typ.)	ns	
Power Supply	+10	V	
Operating Power			
Dissipation	20	mW	

OBJECTIVE SPECIFICATION

2580-N,I

DESCRIPTION

The 2580 is an 8,192-Bit Read-Only Memory available in a 2048x4 organization. This device has TTL compatible inputs and outputs and requires +5V and -12V power supplies. A READ input controls the entry of data from the ROM into output latches. Three-state outputs allow OR tying for implementing larger memories. The outputs are enabled by a programmable four bit select code applied to four binary chip select terminals.

FEATURES

- 2048x4 ORGANIZATION
- 625ns TYPICAL ACCESS TIME
- OUTPUT LATCHES
- 1 OF 16 CHIP ENABLE DECODING
- TTL/DTL COMPATIBLE INPUTS AND OUTPUTS
- THREE-STATE OUTPUTS
- $V_{CC} = +5V$, $V_{GG} = -12V$, $V_{DD} = 0V$
- 24 PIN SILICONE DIP
- P-MOS SILICON GATE TECHNOLOGY

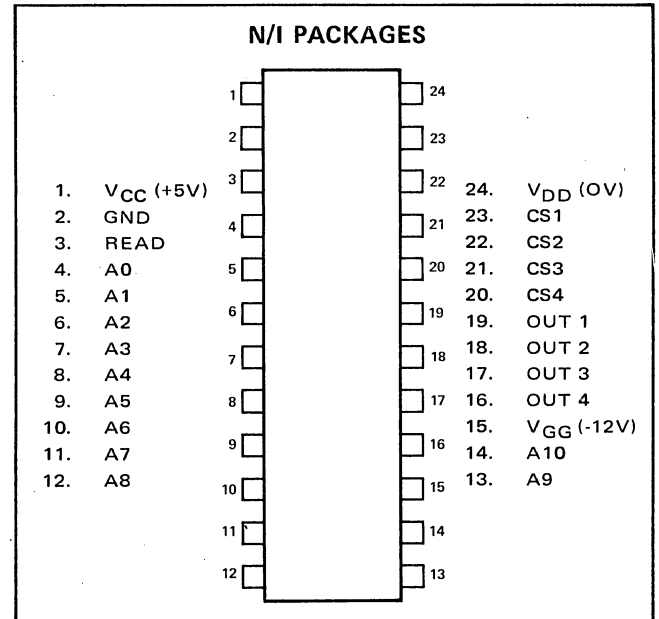
APPLICATIONS

- MICRO-PROGRAMMING
- LOOK-UP TABLES
- DATA STORAGE
- CODE CONVERSION
- RANDOM LOGIC SYNTHESIS
- CHARACTER GENERATION
- PROGRAM STORAGE

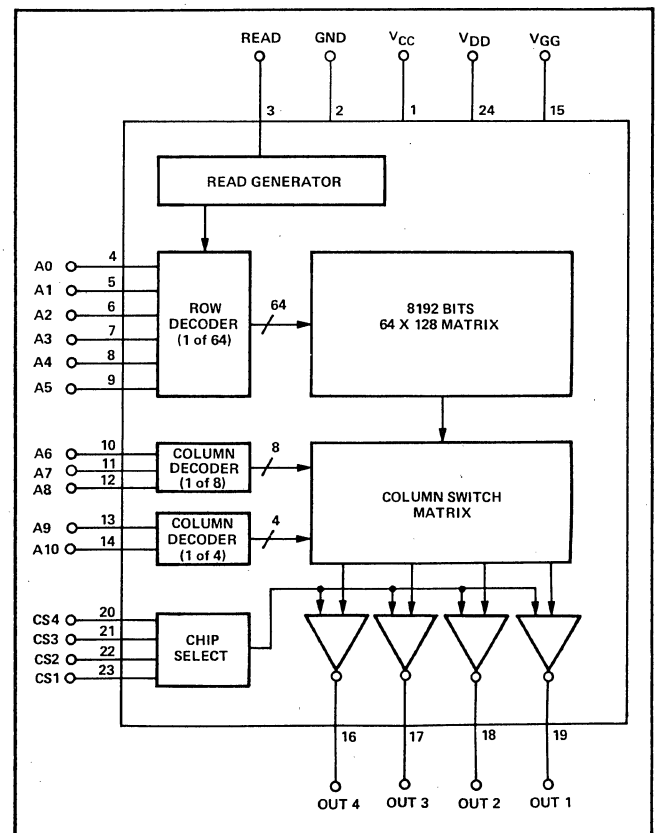
BIPOLAR COMPATIBILITY

All inputs of the 2580 can be driven directly by standard TTL level signals. The data output buffers are capable of sinking a minimum of 1.6mA sufficient to drive one standard TTL load.

PIN CONFIGURATION (TopView)



BLOCK DIAGRAM



DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V ±5%, V_{DD} = 0V, V_{GG} = -12V ±5% unless otherwise noted. (See notes 4, 5, 6, 7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I _{LI}	Input Load Current		10	500	nA	V _{IN} = -5.5V T _A = 25°C
I _{LO}	Output Leakage Current		10	1000	nA	V _{OUT} = 0V T _A = 25°C V _{CE} = V _{CC}
I _{CC}	V _{CC} Power Supply Current		23	35	mA	(8)
I _{GG}	V _{GG} Power Supply Current		23	35	mA	(8)
V _{IL}	Input Logic "0"			+0.6	V	} Note 12
V _{IH}	Input Logic "1"	+3.4		5.3	V	

AC CHARACTERISTICS

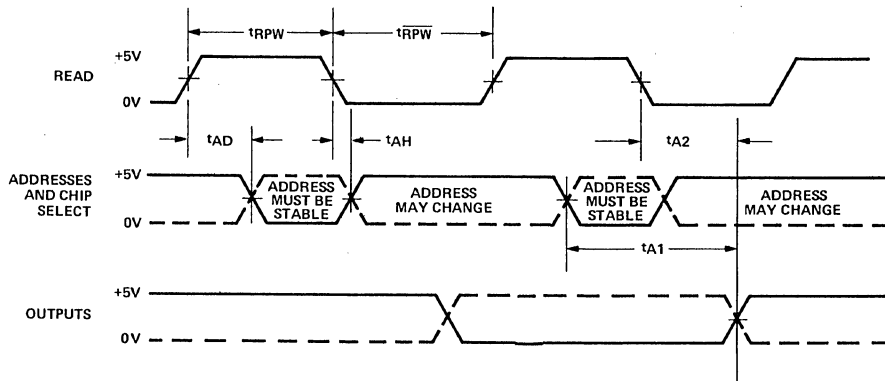
T_A = 25°C; V_{CC} = 5V ±5%, V_{DD} = 0V, V_{GG} = -12V ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V _{OL}	Output Logic "0"			+0.5	V	I _{OL} = 1.6mA I _{OH} = 100µA
V _{OH}	Output Logic "1"	+3.8			V	
t _{RPW} ¹⁰	Read Pulse Width	650	500		ns	
t _{RPW} ⁹	Read Pulse Width	500	400		ns	
t _{AD}	Address Delay Time (11)			50	ns	
t _{AH}	Address Hold Time	0			ns	
t _{A1}	Address to Output Delay		625	950	ns	
t _{A2}	End of Read Pulse to Output Delay		250	350		
C _{IN}	Input Capacitance			10	pF	f = 1MHz, V _{AC} = 25mV p-p V _{IN} = V _{CC}

NOTES:

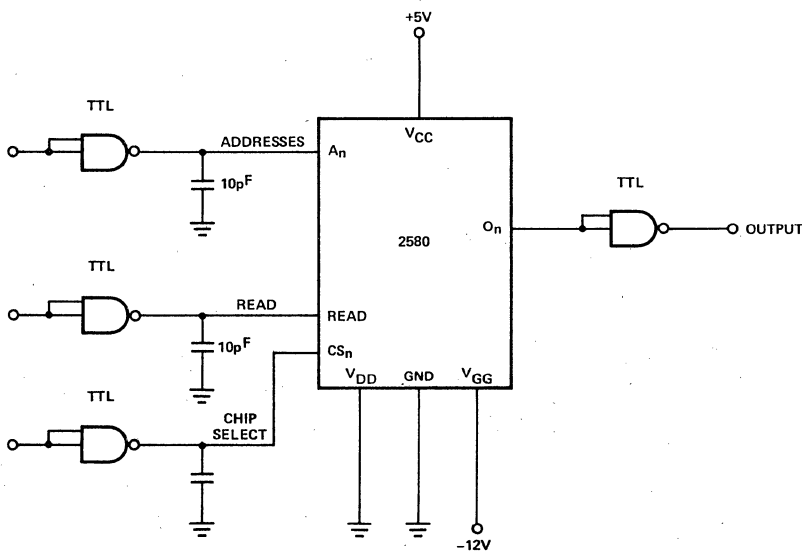
- Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
- For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
- All inputs are protected against static charge.
- Parameters are valid over operating temperature range unless specified.
- All voltage measurements are referenced to ground.
- Manufacturer reserves the right to make design and process changes and improvements.
- Typical values are at +25°C and nominal supply voltages.
- Outputs open, t_{RPW} = 500ns, t_{RPW} = 500ns.
- During t_{RPW} data is clocked into the output latches and the address decoders are precharged in preparation for the next cycle.
- During t_{RPW} addresses are decoded and sent to the memory matrix; and the stored memory data is moved to the data inputs of the output RS latches. This data is clocked into the output latches at the end (falling edge) of the READ pulse. After t_{A2}, data appears at the output terminals.
- Addresses must be stable within 50ns after the READ line rises and must remain stable until the READ line falls.
- Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to +70°C. Actual input requirements with respect to V_{CC} are V_{IH} = V_{CC} - 1.85V and V_{IL} = V_{CC} - 4.15V.

TIMING DIAGRAM



Note: All measurements made at 50% points.
Input $t_r = t_f = 10ns$.

AC TEST SETUP



2602 - 1, 2602 - 2 - B

DESCRIPTION

The Signetics 2602 is a static random access read/write memory offering a 1024x1 organization. Fabricated with low threshold N-Channel silicon gate technology, the 2602-2 offers an access and read cycle time of less than 650 ns. Write cycle time is 650 ns.

The 2602-2 is fully static, requiring no clocks and is completely DTL/TTL compatible including the single +5V power supply requirement.

FEATURES

- 1024x1 ORGANIZATION
- COMPLETELY STATIC OPERATION
- +5V POWER SUPPLY ONLY
- TTL COMPATIBLE INPUTS
- THREE-STATE TTL OUTPUT
- 16-PIN DIP PACKAGE
- 200 mW DISSIPATION TYPICAL
- N-CHANNEL SILICON GATE
- NO CLOCKS, NO REFRESHING, NO SENSING
- ACCESS TIMES: 2602 - 1 500ns
2602 - 2 650ns
- CYCLE TIMES: 2602 - 1 500ns
2602 - 2 650ns

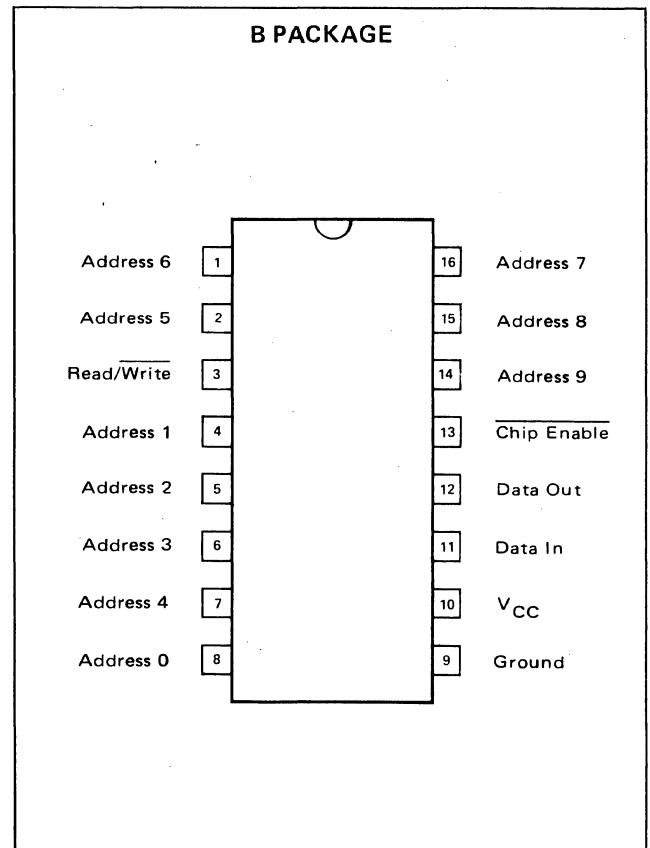
APPLICATIONS

PERIPHERAL MEMORIES
BUFFER MEMORIES
MINICOMPUTER MEMORY

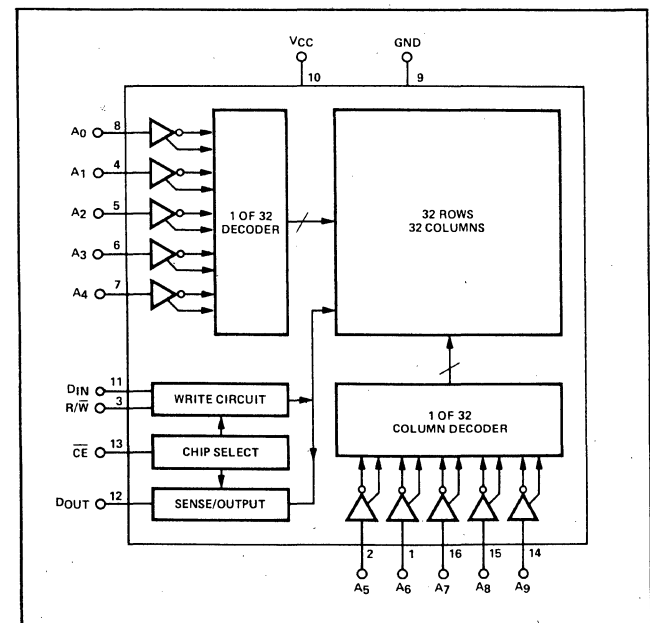
MAXIMUM GUARANTEED RATINGS⁽¹⁾

Operating Ambient Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Input, Output, and Supply Voltages with respect to ground	-0.5 V to +7 V
Package Power Dissipation ⁽²⁾ "B" Pkg.	640 mW

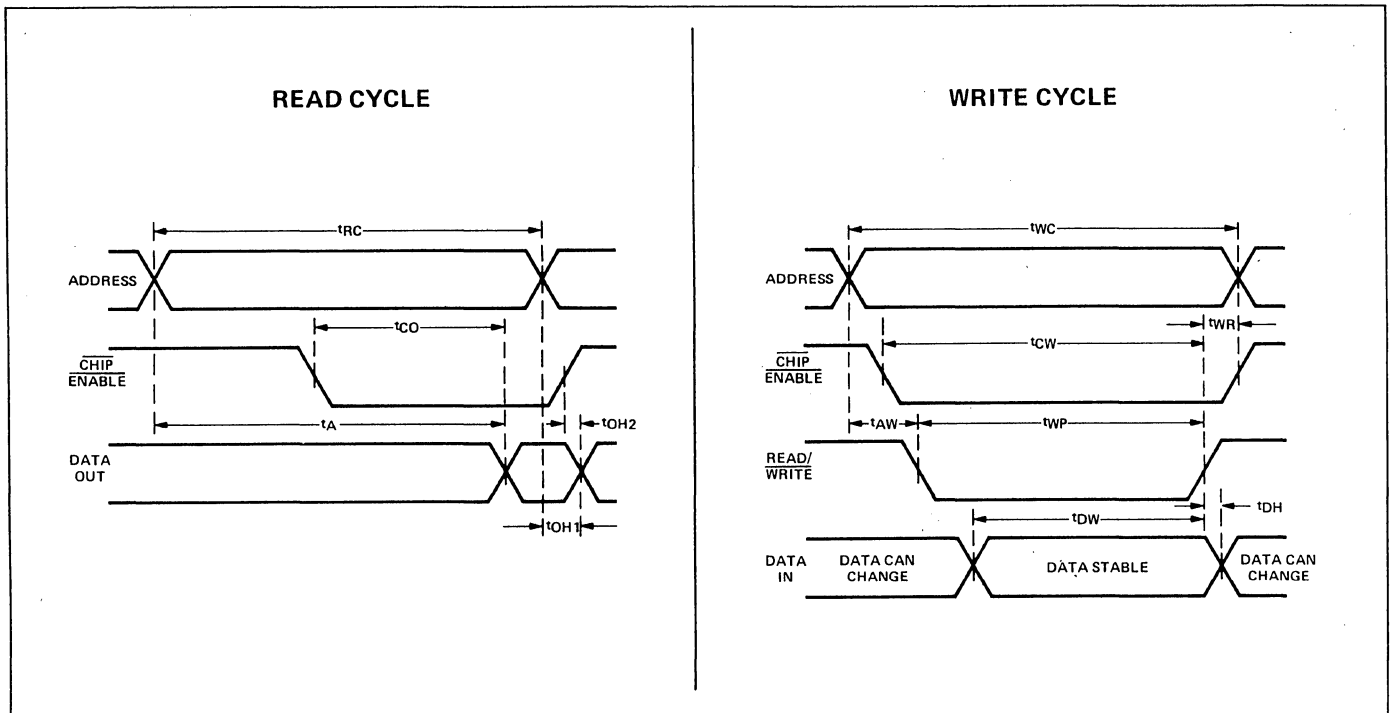
PIN CONFIGURATION



BLOCK DIAGRAM



TIMING DIAGRAMS



A.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified.

PARAMETER		LIMIT 2602-1			LIMIT 2602-2			
		MIN	TYP	MAX	MIN	TYP	MAX	
READ CYCLE								
t_{RC}	Read cycle	500			650			ns
t_A	Access time			500			650	ns
t_{CO}	Chip enable to output time			350			400	ns
t_{OH1}	Previous read data valid with respect to address	50			50			ns
t_{OH2}	Previous read data valid with respect to chip enable	0			0			ns
WRITE CYCLE								
t_{WC}	Write cycle	500			650			ns
t_{AW}	Address to write setup time	150			200			ns
t_{WP}	Write pulse width	300			400			ns
t_{WR}	Write recovery time	50			50			ns
t_{DW}	Data setup time	330			450			ns
t_{DH}	Data hold time	100			100			ns
t_{CW}	Chip enable to write setup time	400			550			ns

A.C. CONDITIONS OF TEST

Input Pulse Levels:

+0.65 Volt to +2.2 Volt

Input Pulse Rise and Fall Times:

20nsec

Timing Measurement Reference Level:

1.5 Volt

Output Load:

1 TTL Gate and $C_L = 100\text{ pF}$

D.C. OPERATING CHARACTERISTICS $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
I_{LI}	Input load current (All input pins)			10	μA
				10	μA
I_{LOH}	Output leakage current			10	μA
I_{LOL}	Output leakage current			-100	μA
I_{CC1}	Power supply current		30	60	mA
I_{CC2}	Power supply current			70	mA
V_{IL}	Input "low" voltage	-0.5		+0.65	V
V_{IH}	Input "high" voltage	2.2		V_{CC}	V
V_{OL}	Output "low" voltage			+0.45	V
V_{OH}	Output "high" voltage	2.4			V
C_{IN}	Input capacitance		3	5	pF
C_{OUT}	Output capacitance		7	10	pF

NOTES:

1. All inputs protected against static charge.

DESCRIPTION

Signetics 2604 is a high speed, fully decoded, dynamic, read/write, random access memory. It is organized as 4096 X 1 and achieves an access time of less than 300ns. All inputs except the CE Clock are fully TTL compatible and no special drivers or level shifters are required. The tri-state output buffers can drive 2 standard TTL loads.

The CE Clock is the only high level input required for the 2604. It is a low capacitance load and uses a nominal 12 volt signal swing. When the CE Clock goes low, internal signal nodes are pre-charged and the memory then assumes its standby mode and consumes very little power. All active operations are performed with the clock high.

The 2604 is a dynamic memory and each bit must be periodically refreshed. The internal organization allows refreshing to be accomplished by performing an operation at each of the 64 row addresses (derived from inputs A₀-A₅) every 2 milliseconds. The chip need not be selected during the refresh cycles.

FEATURES

- CAPACITY OF 4096-BITS
- ACCESS TIME 300ns MAXIMUM
- CYCLE TIME 470ns MAXIMUM
- ION-IMPLANTED N-CHANNEL SILICON GATE MOS TECHNOLOGY
- STANDARD SUPPLY VOLTAGES OF +12, +5, -5 VOLTS
- SINGLE LOW CAPACITANCE HIGH LEVEL CLOCK INPUT
- ADDRESS, CONTROL AND DATA INPUTS FULLY TTL COMPATIBLE
- LATCHES FOR ADDRESS AND CONTROL INPUTS PROVIDED ON CHIP
- TTL TRI-STATE OUTPUT BUFFER
- LOW POWER DISSIPATION
- STANDARD 22-PIN DUAL-IN-LINE PACKAGE

MAXIMUM GUARANTEED RATING*

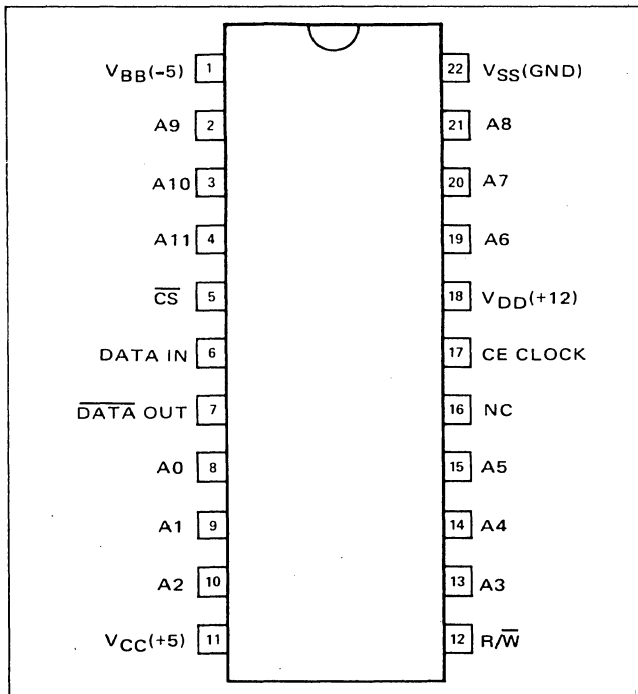
Operating Ambient Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Voltages With Respect To V _{BB}	-0.3 to +20 volts

*Stresses above those listed may cause permanent damage to the device. These are stress ratings only and functional operation under these conditions is not implied.

ORDER INFORMATION

For V_{BB} = -3.0V, Order No. is 2604A.
For V_{BB} = -5.0V, Order No. is 2604.

PIN CONFIGURATION



PIN DESCRIPTION

Chip Enable Clock

The master operating signal input is called the Chip Enable Clock. This signal is the only non-TTL-level input required to operate the 2604. Internal operations are executed while Chip Enable is in the "high" state. When Chip Enable is low, the 2604 is in the standby state (low power consumption) pre-charging internal nodes in preparation for the next memory cycle.

Chip Select

The data in, data out, and read/write functions are all affected by the Chip Select input. Data is not accepted on the Data In terminal unless Chip Select and Read/Write are low. The write state of the Read/Write terminal is not recognized unless Chip Select is low. The output drivers are disconnected (tri-state) unless Chip Select has gone low at the appropriate time in a given cycle. Chip Select may be changed to the low state any time during a cycle as long as the correct write pulse timing is maintained. However, if Chip Select goes low more than 80 nsec into the cycle, the access time is lengthened accordingly. Chip Select may go high anytime after the minimum Chip Select pulse width requirement has been met. The chip remains selected for the remainder of the cycle. As with all other inputs to the 2604 except Chip Enable, Chip Select responds to a standard TTL-level signal without an external pull-up resistor.

PIN DESCRIPTION (Continued)

Read/Write

Whether a given memory cycle is a read or a write cycle is determined by the Read/Write input. When Read/Write is high and the chip is selected, a read cycle is executed. When Read/Write is low and the chip is selected, a write cycle is executed. The internal write pulse width is determined by the falling edge of Chip Select or Read/Write, whichever is later, and the trailing edge of Read/Write.

Addresses

All address inputs respond to TTL-level signals. The addresses in a given cycle must be stable before Chip Enable goes high. Addresses are latched on the 2604 so that the address inputs can change after the address hold time requirements have been met.

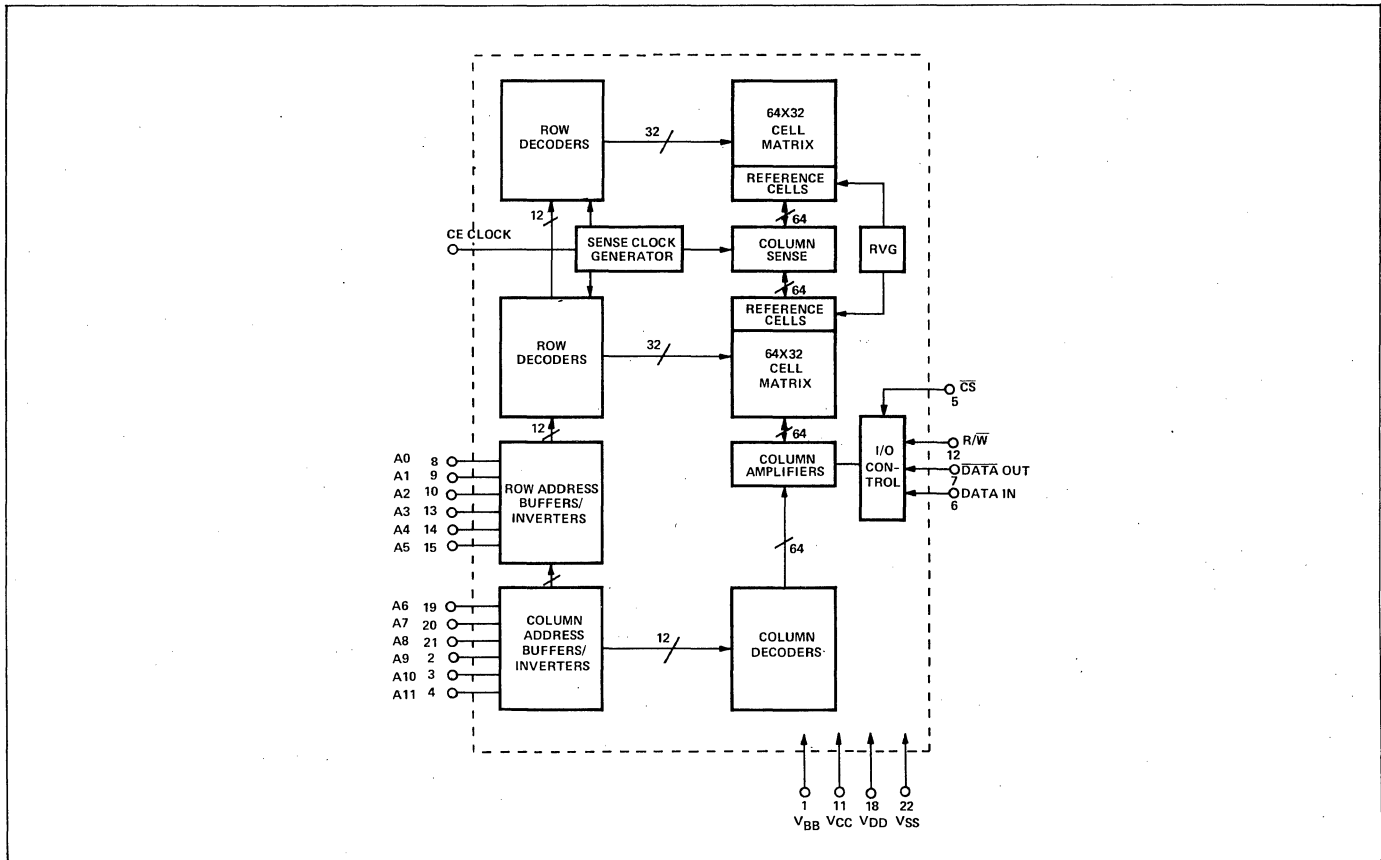
Data-in

Input data is supplied to the 2604 on the Data-in terminal. This TTL-compatible input is used during a write cycle or read-modify-write cycle.

Data-out

The output buffer is a totem-pole tri-state structure that will drive two standard TTL loads. The high impedance (disconnect) state occurs when Chip Enable is low or when the Chip Select input is high. When enabled, the output goes to a TTL "0" level before valid data appears. Output data is the complement of input data.

BLOCK DIAGRAM



RECOMMENDED SUPPLY VOLTAGES¹ (Measured with respect to V_{SS}.)

PARAMETER	LIMITS			UNIT
	MIN	TYP	MAX	
V _{DD}	11.4	12.0	12.6	V
V _{BB} (For 2604 only)	-4.5	-5.0	-5.5	V
V _{BB} (For 2604A only)	-2.7	-3.0	-3.3	V
V _{CC}	4.5	5	V _{DD}	V
V _{SS}		0.0		V

DC CHARACTERISTICS $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, See "Recommended Supply Voltages"

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP ²	MAX	
V_{IH} Input High Voltage (Non-clock inputs)		2.2		V_{DD}	V
V_{IL} Input Low Voltage (Non-clock inputs)		-0.6		0.6	V
V_{CH} Clock Input High Voltage		$V_{DD}-1$	V_{DD}	$V_{DD}+1$	V
V_{CL} Clock Input Low Voltage		-0.6		0.6	V
I_I Input Current (All inputs)	$V_{IN} = +5V$			10	μA
I_{LO} Output Leakage Current	$V_{OUT} = +5V$, Output Disabled			10	μA
I_{BB} V_{BB} Supply Current	$V_{BB} = -5V$, $V_{DD} = 12V$, $V_{SS} = 0V$			100	μA
I_{DD1} V_{DD} Supply Current During CE Clock High			40	60	mA
I_{DD2} V_{DD} Supply Current During CE Clock Low			0.2	0.5	mA
I_{DD3} Average V_{DD} Supply Current During t_{WC} or t_{RC}	$t_{CE} = 320\text{ns}$, $t_{WC} = t_{RC} = 470\text{ns}$		33		mA
I_{DD4} Average V_{DD} Supply Current During t_{RMWC}	$t_{CE} = 560\text{ns}$, $t_{RMWC} = 710\text{ns}$		35		mA
I_{CC1} V_{CC} Supply Current (Operating)	Noté 7				
I_{CC2} V_{CC} Supply Current				100	μA
V_{OH} Output High Voltage	$I_{OUT} = -2.0\text{mA}$	2.4		V_{CC}	V
V_{OL} Output Low Voltage	$I_{OUT} = 3.2\text{mA}$			0.4	V

CAPACITANCE $T_A = +25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP ²	MAX	
C_{IN1} Input Capacitance (Address and Read/Write)	$V_{CL} = 0V$, $V_{DD} = +12V$		5	7	pF
C_{IN2} Input Capacitance (Chip Select and Data In)	$V_{BB} = -5V$, $V_{CC} = +5V$, $f = 1\text{MHz}$		4	6	pF
C_{OUT} Output Capacitance	$V_{CL} = 0V$, $V_{DD} = +12V$		5	7	pF
C_{INC} Clock Input Capacitance	$V_{CH} = +12V$, $V_{BB} = -5V$		18	22	pF
	$V_{CL} = 0V$, $V_{CC} = +5V$, $F = 1\text{MHz}$		23	27	pF

AC CHARACTERISTICS $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, See "Recommended Supply Voltages"

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP ²	MAX	
READ, WRITE, AND READ-MODIFY-WRITE CYCLES					
t_{AS} Address Set-up Time		0			ns
t_{AH} Address Hold Time		150			ns
t_{CSS} Chip Select Set-up Time		240			ns
t_{CSW} Chip Select Pulse Width		150			ns
t_t Transition Time (Rise and Fall)				20	ns
t_{REF} Time Between Refresh				2	ms
t_{CE} Chip Enable Pulse Width		150			ns

AC CHARACTERISTICS (Continued) $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, See "Recommended Supply Voltages"

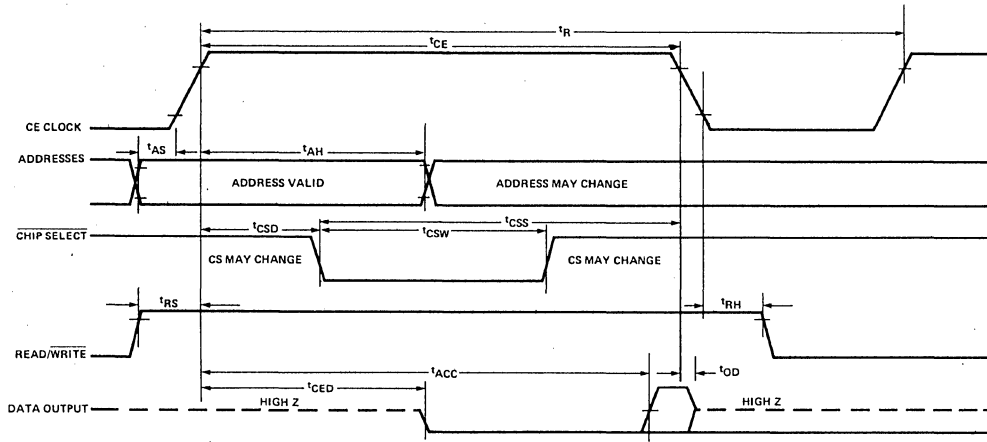
PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP ²	MAX	
READ CYCLE					
t_R Read Cycle Time		470			ns
t_{CE} Chip Enable Pulse Width		320			ns
t_{RS} Read Set-up Time		0			ns
t_{RH} Read Hold Time		40			ns
t_{CED} Chip Enable to Output Enabled	Note 3		150		
t_{OD} Chip Enable to Output High Impedance State		10			ns
t_{ACC} Chip Enable to $\overline{\text{DATA}}$ Valid				300	ns
t_{CSD} Chip Select Delay from CE Clock	Note 4			80	ns
WRITE CYCLE					
t_W Write Cycle Time		470			ns
t_{CE} Chip Enable Pulse Width		320			ns
t_{WS} Write Set-up Time		240			ns
t_{WW} Write Pulse Width		200			ns
t_{DS} Data Set-up Time with Respect to $\overline{\text{R/W}}$	Note 5	0			ns
t_{DH} Data Hold Time with Respect to CE Clock		40			ns
t_{WCH} Write to Chip Select Hold Time	Note 6	200			ns
READ-MODIFY-WRITE CYCLE					
t_{RMW} Read-Modify-Write Cycle Time		710			ns
t_{CE} Chip Enable Clock Pulse Width		560			ns
t_{RS} Read to Chip Enable Set-up Time		0			ns
t_{RH} Read to Chip Enable Hold Time		320			ns
t_{WW} Write Pulse Width		200			ns
t_{WS} Write Set-up Time		240			ns
t_{VW} Previous Data Valid with Respect to Write Pulse		50			ns
t_{CSD} Chip Select Delay from CE Clock	Note 4			80	ns
t_{DS} Data Set-up Time with Respect to Write Pulse		0			ns
t_{DH} Data Hold Time with Respect to CE Clock		40			ns
t_{OD} Chip Enable to Output Disabled		10			ns
t_{CED} Chip Enable to Output Enabled			150		ns
t_{ACC} Chip Enable to $\overline{\text{Data}}$ Valid				300	ns

NOTES:

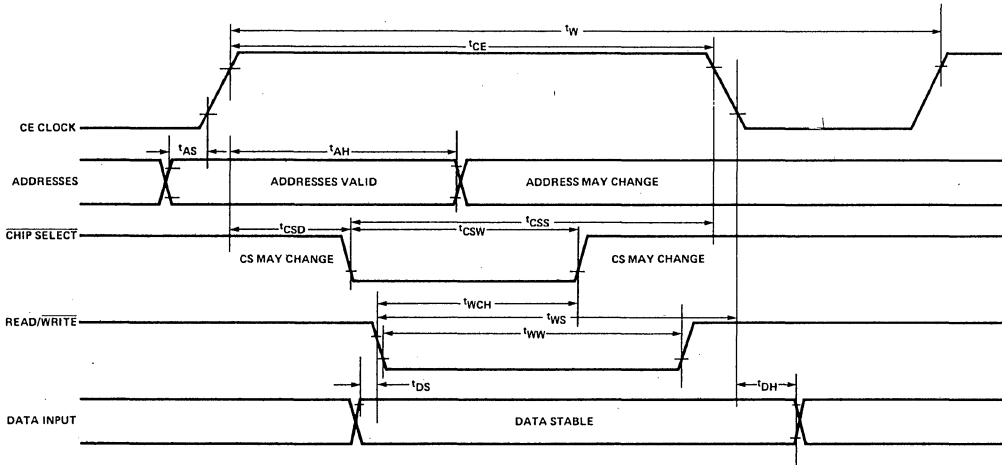
1. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltage larger than the rated maximum.
2. Typical values are at $+25^{\circ}\text{C}$ and nominal supply voltages.
3. Valid data is always preceded by a logic "0" output when the output buffers are enabled.
4. If CS goes low later than maximum t_{CSD} , data access time, and therefore cycle time, are increased accordingly.
5. If CS goes low after $\overline{\text{R/W}}$ goes low, t_{DS} is with respect to the falling edge of CS rather than $\overline{\text{R/W}}$.
6. The internal write signal is a combination of CS and $\overline{\text{R/W}}$. As a result, the internal write pulse width is a function of t_{WCH} as well as t_{WW} .
7. Depends on output loading. The V_{CC} supply is connected to the output buffer only.
8. Input rise and fall times of 20ns are used to measure the access and cycle times.

MEMORY Signetics

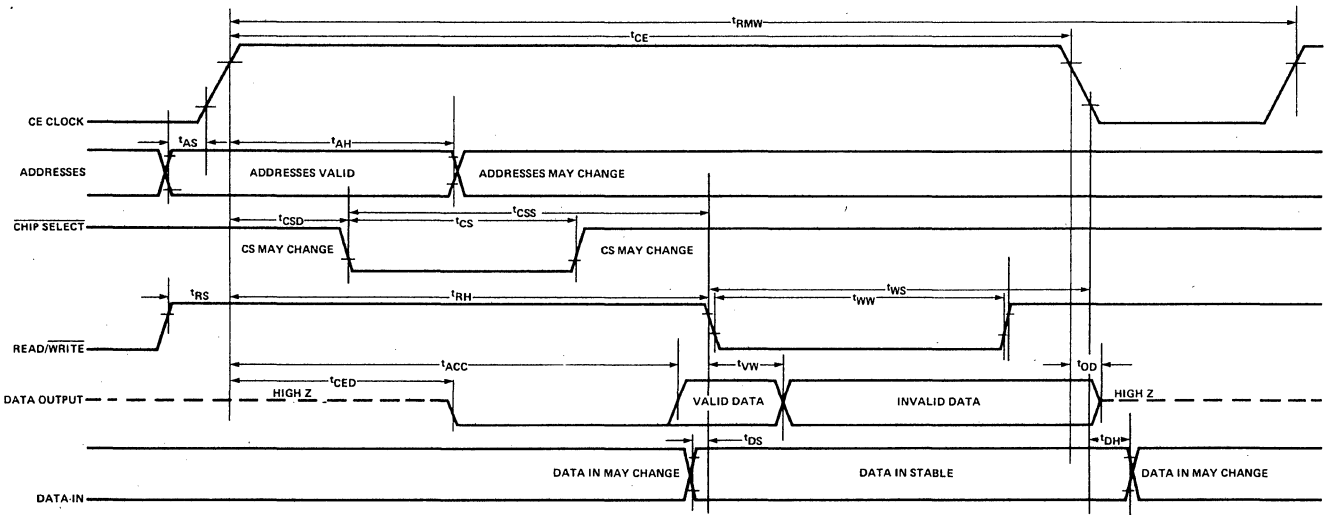
READ CYCLE TIMING



WRITE CYCLE TIMING



READ-MODIFY-WRITE CYCLE TIMING



PRELIMINARY SPECIFICATIONS

N CHANNEL SILICON GATE MOS 2600 SERIES

DESCRIPTION

Signetics' 2606 is a fully decoded, static, read/write, random access memory. It has a capacity of 1024 bits and is organized as 256 x 4. The 2606 is fabricated with N-Channel silicon gate MOS technology and achieves an access time of less than 750 nanoseconds. No clocks are required and all interface signals are directly TTL compatible including the power supply.

FEATURES

- 256 x 4 ORGANIZATION
- STATIC OPERATION
- ACCESS TIME: 2606 750ns
2606-1 500ns
- CYCLE TIME: 2606 750ns
2606-1 500ns
- SINGLE 5 VOLT POWER SUPPLY
- TTL COMPATIBLE INPUTS AND OUTPUTS
- 200mW TYPICAL POWER DISSIPATION
- MULTIPLEXED DATA BUS
- TRI-STATE OUTPUTS
- N-CHANNEL SILICON GATE TECHNOLOGY
- STANDARD 300-MIL 16 PIN PACKAGE

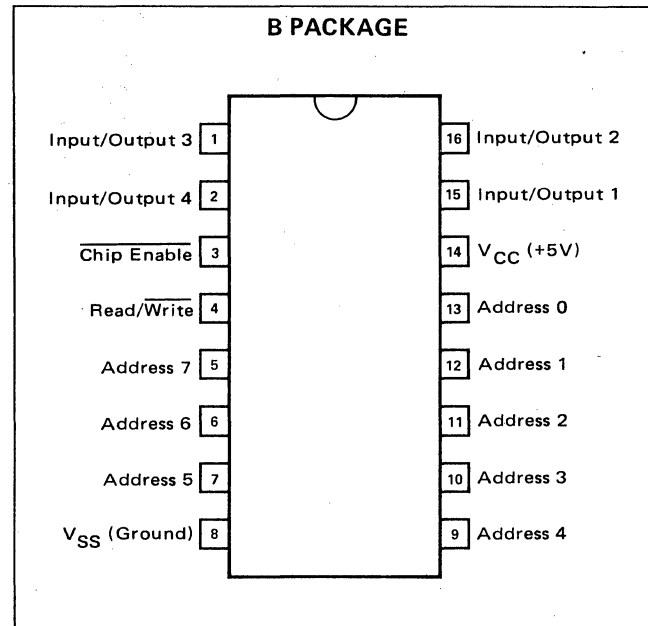
APPLICATIONS

MICROCOMPUTER MEMORIES
PERIPHERAL DEVICES
TERMINALS
DATA BUFFERS

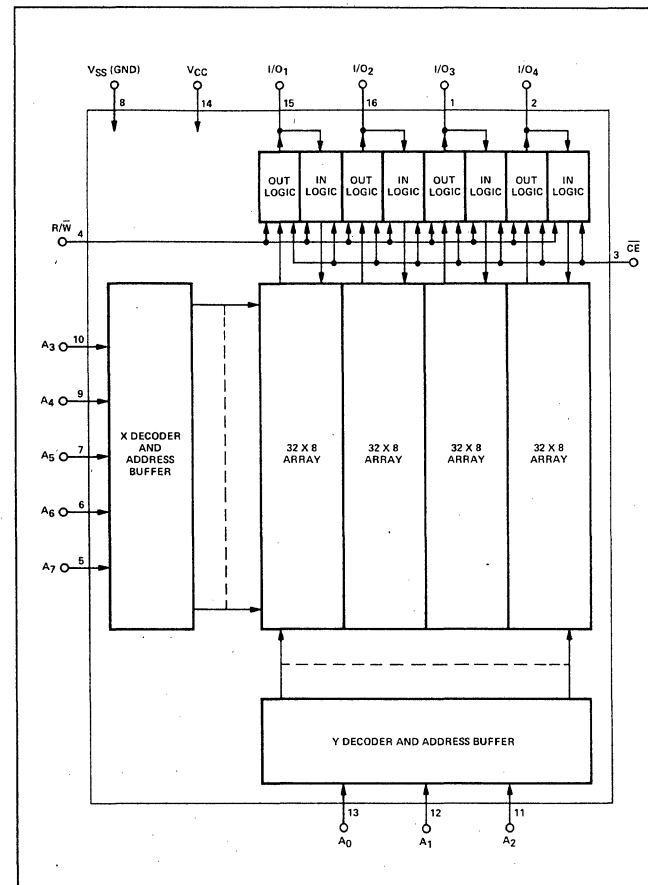
MAXIMUM GUARANTEED RATINGS(1)

Operating Ambient Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Input, Output, and Supply Voltages with respect to ground pin(3)	-0.5V to +6V
Package Power Dissipation(2) "B" Pkg.	640 mW

PIN CONFIGURATION



BLOCK DIAGRAM



SIGNETICS 256 x 4 RANDOM ACCESS READ/WRITE STATIC MEMORY ■ 2606

D.C. OPERATING CHARACTERISTICS

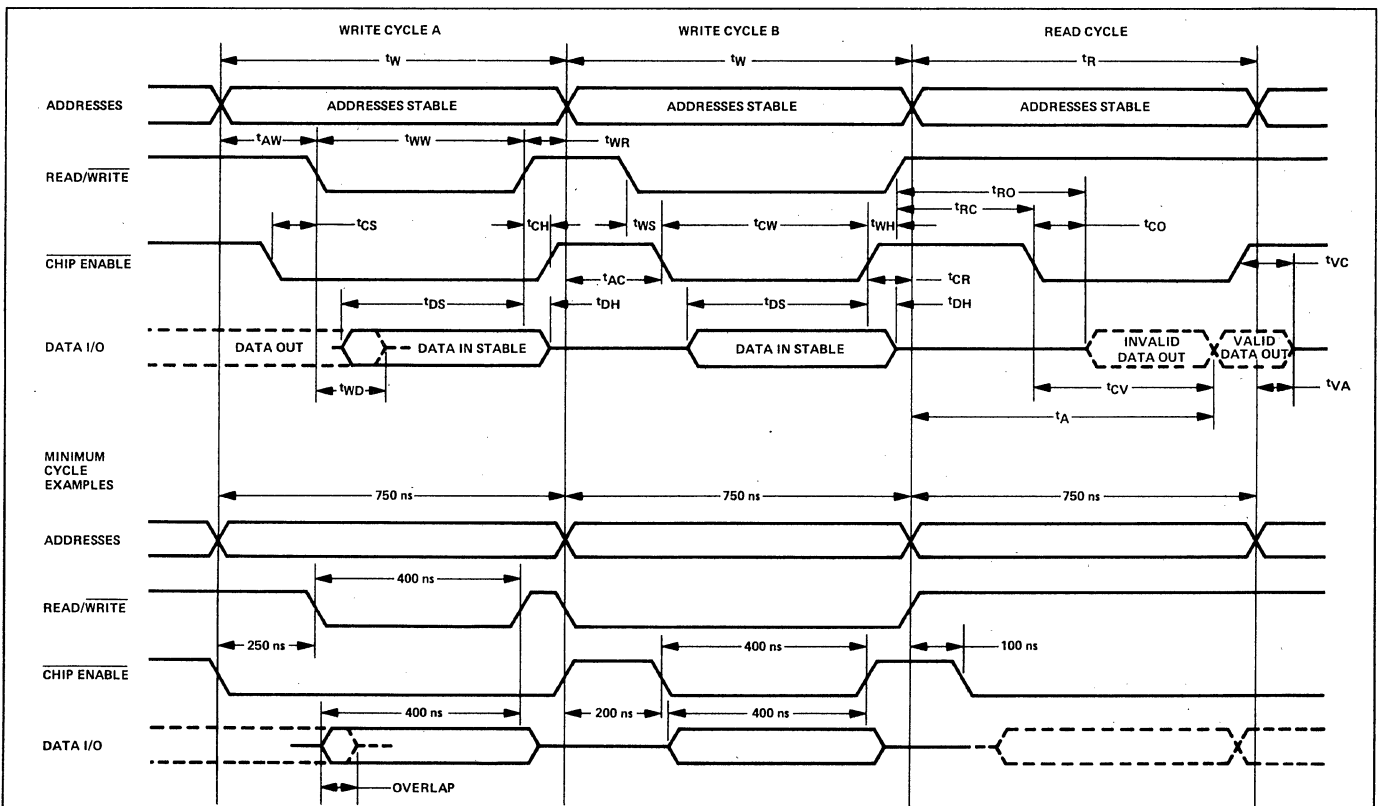
$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$ unless otherwise specified. See Notes 3, 4, 5, 6 & 7.

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
I_{LI}	Input load current			10	μA	$V_{IN} = 0$ to 5.25V
I_{BH}	Bus high current			10	μA	$\overline{CE} = 2.2\text{V}$, $V_{OUT} = 4.0\text{V}$
I_{BL}	Bus low current			-100	μA	$\overline{CE} = 2.2\text{V}$, $V_{OUT} = 0.45\text{V}$
I_{CC}	Power supply current		40	70 80	mA mA	All inputs = 5.25V Data Bus Open $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$
V_{IL}	Input low voltage	-0.5		+0.65	V	
V_{IH}	Input high voltage	2.2		V_{CC}	V	
V_{OL}	Output low voltage			+0.45	V	$I_{OL} = 1.9\text{mA}$
V_{OH}	Output high voltage	2.4			V	$I_{OH} = -100\mu\text{A}$
C_{IN}	Input capacitance		4	7	pF	$V_{IN} = 0\text{V}$
$C_{I/O}$	Data bus capacitance		7	10	pF	$V_{OUT} = 0\text{V}$

NOTES

- Stresses above those listed under "Maximum Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation sections of this specification is not implied.
- For operating at elevated temperatures the device must be derated based on a $+150^\circ\text{C}$ maximum junction temperature and a thermal resistance of $150^\circ\text{C}/\text{W}$ junction to ambient ("B" pkg.)
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
- Parameter valid over operating temperature range unless otherwise specified.
- All voltage measurements are referenced to ground.
- Manufacturer reserves the right to make a design and process changes and improvements.
- Typical values are at $+25^\circ\text{C}$, nominal supply voltages, and nominal processing parameters.

TIMING DIAGRAM



SWITCHING CHARACTERISTICS

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = +5\text{V} \pm 5\%$ unless otherwise specified. See Notes E, F, G & H.

		2606			2606-1	
WRITE CYCLE A		MIN	MAX	UNIT	MIN	MAX
t_{AW}	Address to write time	250		ns	150	
t_{WW}	Write pulse width	400		ns	300	
t_{WR}	Write recovery time	100		ns	50	
t_{CS}	Chip enable set-up	0		ns	0	
t_{CH}	Chip enable hold	0		ns	0	
t_{DS}	Data in set-up	380		ns	280	
t_{DH}	Data in hold (Note A)	0		ns	0	
t_{WD}	Write to data out disable delay (Note D)		125	ns		100
t_W	Write cycle time	750		ns	500	
WRITE CYCLE B						
t_{AC}	Address to chip enable time	250		ns	150	
t_{CW}	Chip enable pulse width	400		ns	300	
t_{CR}	Chip enable recovery time	100		ns	50	
t_{WS}	Write set-up (Note B)	200		ns	100	
t_{WH}	Write hold	0		ns	0	
t_{DS}	Data in set-up	380		ns	280	
t_{DH}	Data in hold (Note A)	0		ns	0	
t_W	Write cycle time	750		ns	500	
READ CYCLE						
t_R	Read cycle time	750		ns	500	
t_A	Access time		750	ns		500
t_{RO}	Read to output enable (Note C)	100		ns	75	
t_{CO}	Chip enable to output enabled (Note C)	0		ns	0	
t_{VC}	Previous data valid with respect to chip disable	0	150	ns	0	100
t_{VA}	Previous data valid with respect to address change	50		ns	50	
t_{CV}	Chip enable to data valid delay		400	ns		300
t_{RC}	Read to chip enable	100		ns	50	

NOTES

- Maximum t_{DH} governed by potential conflict with data out during next cycle.
- Write set-up required to prevent data overlap. For write cycle B the R/W line will typically change with the addresses.
- R/W must be high and CE must be low in order for output buffers to turn on.
- The output buffers will turn off within the specified time after write mode is selected.
- Input levels swing between 0.65 volt and 2.2 volts.
- Input signal transition times are 20 ns.
- Timing reference level is 1.5 volts.
- Bus load is 100pf, one TTL input and one TTL tristate output.

PRELIMINARY SPECIFICATIONS

N CHANNEL SILICON GATE MOS 2600 SERIES

DESCRIPTION

The 2608 is a fully decoded, static, mask programmable read-only memory. It has a capacity of 8192 bits organized 1024 X 8. The 2608 is fabricated with low threshold N-Channel silicon gate MOS technology which allows extreme ease of use with low voltage logic families such as transistor-transistor logic.

Requiring only 5 volts and ground power connections, the 2608 features a maximum access time of 650ns. Since the 2608 uses static logic throughout, no clocks are required. Four mask programmable chip selects are provided for easy word expansion. All 2608 inputs and outputs are TTL-compatible.

FEATURES

- 1024 X 8 ORGANIZATION
- STATIC OPERATION – NO CLOCKS
- 650ns ACCESS TIME
- SINGLE 5V POWER SUPPLY
- TTL COMPATIBLE INPUTS AND OUTPUTS
- 400mW MAXIMUM POWER DISSIPATION
- TRI-STATE OUTPUTS
- 4 MASK PROGRAMMABLE CHIP SELECTS FOR EASY WORD EXPANSION
- N-CHANNEL SILICON GATE TECHNOLOGY
- STANDARD 24-PIN PACKAGE

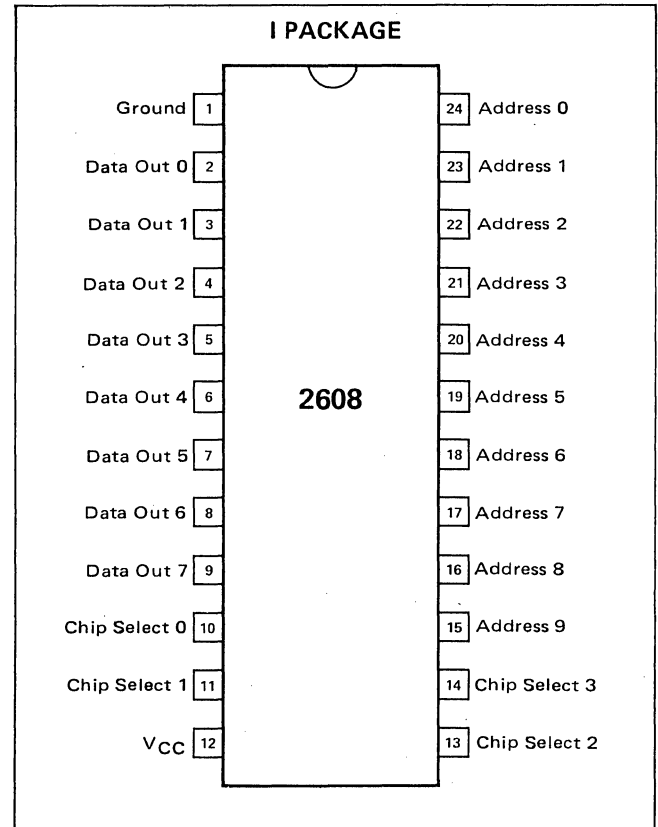
MAXIMUM GUARANTEED RATINGS¹

Operating Ambient Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Input, Output, and Supply Voltages with Respect to Ground Pin	-0.5V to +7V

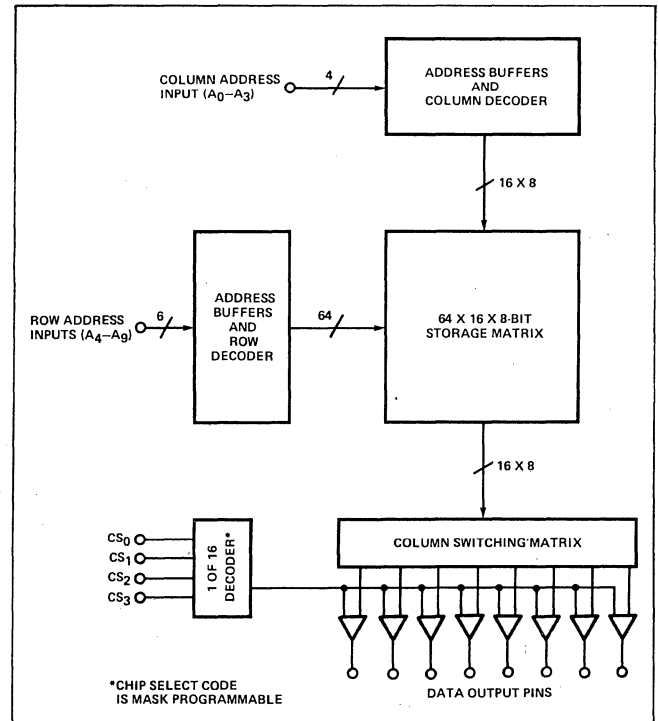
PART IDENTIFICATION

TYPE	OPERATING TEMPERATURE RANGE	PACKAGE
2608I	0°C – +70°C	24-pin ceramic dip

PIN CONFIGURATION



BLOCK DIAGRAM



DC OPERATING CHARACTERISTICS $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$ (Unless Otherwise Noted)^{3,4,5,6,7}

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
I_{IN} Input Load Current	$0 \leq V_{IN} \leq 5.25\text{V}$			10	μA
I_{LOH} Output Leakage Current	$V_O = 2.4\text{V}$, Device Deselected			10	μA
I_{LOL} Output Leakage Current	$V_O = 0.4\text{V}$, Device Deselected			10	μA
I_{CC} Supply Current	$V_{CC} = 5.25\text{V}$, $T_A = 0^\circ\text{C}$			80	mA
V_{IL} Input Low Voltage		-0.5		0.65	V
V_{IH} Input High Voltage		2.2			V
V_{OL} Output Low Voltage	$I_{OL} = 1.6\text{mA}$			0.45	V
V_{OH} Output High Voltage	$I_{OH} = -100\mu\text{A}$	2.4			V
C_{IN} Input Capacitance	$V_{IN} = 0\text{V}$			7.5	pF
C_{OUT} Output Capacitance	$V_{OUT} = 0\text{V}$			15	pF

NOTES:

- Stresses above those listed under "Maximum Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation sections of this specification is not implied.
- For operating at elevated temperatures the device must be derated based on a $+150^\circ\text{C}$ maximum junction temperature and a thermal resistance of 50°C/W junction to ambient.
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
- Parameter valid over operating temperature range unless otherwise specified.
- All voltage measurements are referenced to ground.
- Manufacturer reserves the right to make design and process improvements.
- Typical values are at $+25^\circ\text{C}$, nominal supply voltages, and nominal processing parameters.

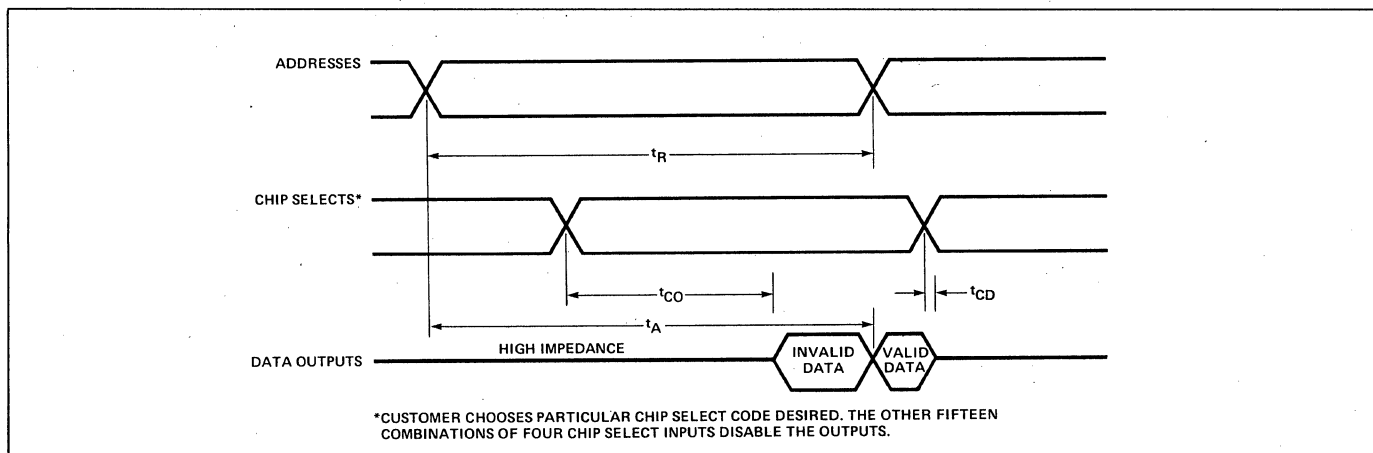
AC OPERATING CHARACTERISTICS $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$ (See Notes A, B & C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_R	Read Cycle Time	650		ns	
t_{CO}	Chip Select to Output Enable		300	ns	Note D
t_{CD}	Chip Select to Output Disable	10	150	ns	Note D
t_A	Access Time	100	650	ns	Note D

NOTES:

- Input levels swing between 0.65 volts and 2.2 volts.
- Input signal transition times are 20 nsec.
- Timing reference level is 1.5 volts.
- Output load is one standard TTL load plus 130pF.

TIMING DIAGRAM



ABSOLUTE MAXIMUM GUARANTEED RATINGS

PARAMETER		LIMITS		UNIT
		MIN	MAX	
T _A	Operating Ambient Temperature			°C
	S82S - Military Range	-55	+125	°C
	N82S - Commercial Range	0	+70	
T _{STG}	Storage Temperature	-65	+150	°C
	Package Power Dissipation @ 70°C			
	B Package		640	mW
	I Package		730	mW
	N Package		730	mW
V _{CC}	Power Supply Voltage		+7	Vdc

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation section of the device specifications is not implied.
2. For operating at elevated temperatures, the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. For operating at elevated temperatures, the devices must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.

SIGNETICS BIPOLAR ROMS, PROMS, RAMS PRODUCT INFORMATION

ELECTRICAL CHARACTERISTICS S82S DEVICES -- $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5$

N82S DEVICES -- $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.7\text{V} \leq V_{CC} \leq 5.25$

PARAMETER	INPUT VOLTAGE						OUTPUT VOLTAGE						INPUT CURRENT					
	V_{IL}^5 (V) LOW LEVEL			V_{IH}^5 (V) HIGH LEVEL			$V_{IC}^{1,5}$ (V) CLAMP VOLTAGE			V_{OL}^2 (V) LOW LEVEL			V_{OH} (V) HIGH LEVEL			I_{IL} (μA) LOW LEVEL		
TEST CONDITIONS	$V_{CC} = \text{MIN}$			$V_{CC} = \text{MAX}$			$I_{IN} = -18 \text{ mA}$ $V_{CC} = \text{MIN}$			$I_{OL} = -16 \text{ mA}$ $V_{CC} = \text{MIN}$			$I_{OUT} = -2.0 \text{ mA}$ $CE_1 = CE_2 = "0"$ "1" STORED			$V_{IN} = 0.45\text{V}$		
DEVICE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
8228			.85	2.0			-1.2			$I_{OUT} = 11.2 \text{ mA}$ 0.5			$I_{OUT} = -1.0 \text{ mA}$ 2.7					
82S09	S		.80	2.2			$I_{IN} = -12 \text{ mA}$ -1.0	-1.5		$I_{OL} = 6.4 \text{ mA}$ 0.35	0.50			5.5		-10	-150	
	N		.85	2.0						0.35	0.5					-10	-100	
82S10	S		.80	2.1			$I_{IN} = -12 \text{ mA}$ -1.0	-1.5		0.35	0.50			5.5		-10	-150	
	N		.85	2.1						0.35	0.45					-10	-100	
82S11	S		.80	2.1			$I_{IN} = -12 \text{ mA}$ -1.0	-1.5		0.35	0.50		2.4			-10	-150	
	N		.85	2.1						0.35	0.45					-10	-100	
82S12			0.85	2.0			-1.2			N/A								
82S16	S		0.8	2.0			$I_{IN} = -12 \text{ mA}$ -1.0	-1.5		0.35	0.5		$I_{OH} = -3.2 \text{ mA}$ 2.4			-10	-250	
	N		0.85	2.0						0.35	0.45		2.6			-10	-100	
82S17	S		0.8	2.0			$I_{IN} = -12 \text{ mA}$ -1.0	-1.5		0.35	0.5			5.5		-10	-250	
	N		0.85	2.0						0.35	0.45					-10	-100	
82S21			0.85	N/A			-1.2				.45		N/A					
82S23	S		0.8	2.0			-0.8	-1.2			0.5			5.5			-150	
	N		0.85	2.0			$I_{IN} = -12 \text{ mA}$ -1.0	-1.5		0.35	0.45					-10	-100	
82S25	S		.80	2.0			$I_{IN} = -12 \text{ mA}$ -1.0	-1.5		0.35	0.5			5.5		-10	-150	
	N		.85	2.0						0.35	0.45					-10	-100	
82S27			.80	2.0			$I_{IN} = -12 \text{ mA}$ -1.0	-1.5		0.45	0.50			5.5				
82S100			0.8	2			-0.8	-1.2		$I_{OL} = 9.6 \text{ mA}$ 0.35 ⁴	0.45		2.4			-10	-100	
82S101			0.8	2			-0.8	-1.2		$I_{OL} = 9.6 \text{ mA}$ 0.35	0.45		2.4			-10	-100	
82S112			0.85	2.0			-1.2			N/A			$I_{OUT} = -3.2 \text{ mA}$ 2.6				-250	
82S114			.85	2.0			-0.8	-1.2		$I_{OL} = 9.6 \text{ mA}$ 0.5		2.7	3.3				-100	
82S115			.85	2.0			-0.8	-1.2		$I_{OL} = 9.6 \text{ mA}$ 0.5		2.7	3.3				-100	
82S116			0.85	2.0			$I_{IN} = -12 \text{ mA}$ -1.0	-1.5		0.35	0.45		2.6	$I_{OH} = -3.2 \text{ mA}$			-10	
							$I_{IN} = -12 \text{ mA}$ -1.0	-1.5		0.35	0.45			5.5		-10	-100	
82S123	S		0.8	2.0			-0.8	-1.2			0.5		2.4			-150	-100	
	N		0.85	2.0						0.45						-100	-100	
82S126	S		.80	2.0			-0.8	-1.2			0.5			5.5		-150	-100	
	N		.85	2.0												-100	-100	
82S129	S		.80	2.0			-0.8	-1.2			0.5		2.4			-150	-100	
	N		.85	2.0												-100	-100	
82S130	S		.80	2.0			-0.8	-1.2			0.5			5.5		-150	-100	
	N		.85	2.0						0.45						-100	-100	
82S131	S		.80	2.0			-0.8	-1.2			0.5		2.4			-150	-100	
	N		.85	2.0						0.45						-100	-100	
82S214	S		.8	2.0			-0.8	-1.2		$I_{OUT} = 9.6 \text{ mA}$ 0.5		2.4	3.3			-150	-100	
	N		.85	2.0								2.7	3.3			-100	-100	
82S215	S		.8	2.0			-0.8	-1.2		$I_{OUT} = 9.6 \text{ mA}$ 0.5		2.4	3.3			-150	-100	
	N		.85	2.0								2.7	3.3			-100	-100	

- NOTES:
1. Test each input one at the time.
 2. Measured with the logic "0" stored. Output sink current is supplied through a resistor to V_{CC} .
 3. I_{CC} is measured with the write enable and memory enable input grounded, all other inputs at 4.5V, and the outputs open.
 4. Measured with V_{IH} applied to CE.
 5. All voltage values are with respect to network ground terminal.
 6. Duration of the short-circuit should not exceed one second.
 7. All sense outputs in "0" state.

SIGNETICS BIPOLAR ROMS, PROMS, RAMS PRODUCT INFORMATION

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	INPUT CURRENT			OUTPUT CURRENT						SUPPLY CURRENT			CAPACITANCE								
	I_{IH} (μ A) HIGH LEVEL			I_{OLK} (μ A) LEAKAGE $V_{CC} = \text{MAX}$ $V_{OUT} = 5.5V$ CE_1 OR $CE_2 = "1"$			I_O (OFF) HI-Z STATE $V_{CC} = \text{MAX}$ $V_{OUT} = 5.5V$			I_{OS} (mA) ⁶ SHORT-CIRCUIT $V_{OUT} = 0V$ $V_{CC} = \text{MAX}$			I_{CC} (mA) ⁶ $V_{CC} = \text{MAX}$			C_{IN} (pF) INPUT $V_{IN} = 0V$ $V_{CC} = 2.0V$			C_{OUT} ⁴ (pF) OUTPUT $V_{CC} = 5.0V$ $V_{OUT} = 2.0V$		
TEST CONDITIONS	$V_{IN} = 5.5V$			$V_{CC} = \text{MAX}$ $V_{OUT} = 5.5V$ CE_1 OR $CE_2 = "1"$			$V_{CC} = \text{MAX}$ $V_{OUT} = 5.5V$			$V_{OUT} = 0V$ $V_{CC} = \text{MAX}$			$V_{CC} = \text{MAX}$			$V_{IN} = 0V$ $V_{CC} = 2.0V$			$V_{CC} = 5.0V$ $V_{OUT} = 2.0V$		
DEVICE	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
8228										-20		-70									
82S09	S	1	40	1		60			N/A			N/A	150	200				5			8
	N	1	25	1		40			N/A			N/A	150	190							
82S10	S	1	40	1		60			N/A			N/A									
	N	1	25	1		40			N/A			N/A									
82S11	S	1	40			N/A		1	100									4			7
	N	1	25			N/A		1	60	-20		-100						4			7
								$V_{OUT} = 0.45V$	6												
								-1	-100												
								-1	-80												
82S12																					
82S16	S					N/A		1	50												
	N	1	25			N/A		1	40									5			8
								$V_{OUT} = 0.45V$													
								-1	-50	-20		-70									
								-1	-40												
82S17	S																	5			8
	N	1	25			40			N/A			N/A						5			8
82S21			25			40			N/A			N/A		N/A				N/A			N/A
82S23	S					50			N/A			N/A	65	85				5			8
	N		50			40			N/A			N/A	65	77							
82S25	S		25			$V_{CC} = \text{MIN}$															
	N		10			<1	100		N/A			N/A	80	120				5			8
													80	105							
82S27			1			100			N/A			N/A	120	140				5			8
		$V_{IN} = 2.4V$																			
			40																		
82S100		<1	25			N/A			N/A	-20		-70	120	170				5			8
82S101		<1	25			N/A			N/A			N/A	120	170				5			8
82S112			25			N/A			N/A			N/A	N/A					N/A			N/A
82S114			25			N/A															
										40											
										$V_{OUT} = 0.5V$	-40	-20	-70	135	185			5			8
82S115			25			N/A				40											
										$V_{OUT} = 0.5V$	-40	-20	-70	135	185			5			8
82S116		1	25			N/A				1	40	-20	-70	80	115			5			8
										$V_{OUT} = 0.4V$	-1	-40	-20	-70							
82S117		1	25			40				N/A								5			8
82S123	S									50	-20	-100	65	85							
	N		50			N/A				40	-20	-90	65	77				5			8
										$V_{OUT} = 0.5V$											
										-50											
										-40											
82S126	S		50			60							105	125							
	N		40			40				N/A			105	120				5			8
82S129	S		50							60	-15	-85	105	125							
	N		40			N/A				40	-20	-70	105	120				5			8
										$V_{OUT} = 0.5V$											
										-60											
										-40											
82S130	S		50			60															
	N		40			40				N/A								5			8
82S131	S		50							60	-15	-85									
	N		40			N/A				40	-20	-70	120	140				5			8
										$V_{OUT} = 0.5V$											
										-60											
										-40											
82S214	S		50							100	-15	-85	130	185							
	N		25			N/A				40	-20	-70	130	175				5			8
82S215	S		50							$V_{OUT} = 0.5V$	-100	-85	130	185							
	N		25			N/A				-40	-20	-70	130	175				5			8

Signetics



MEMORY

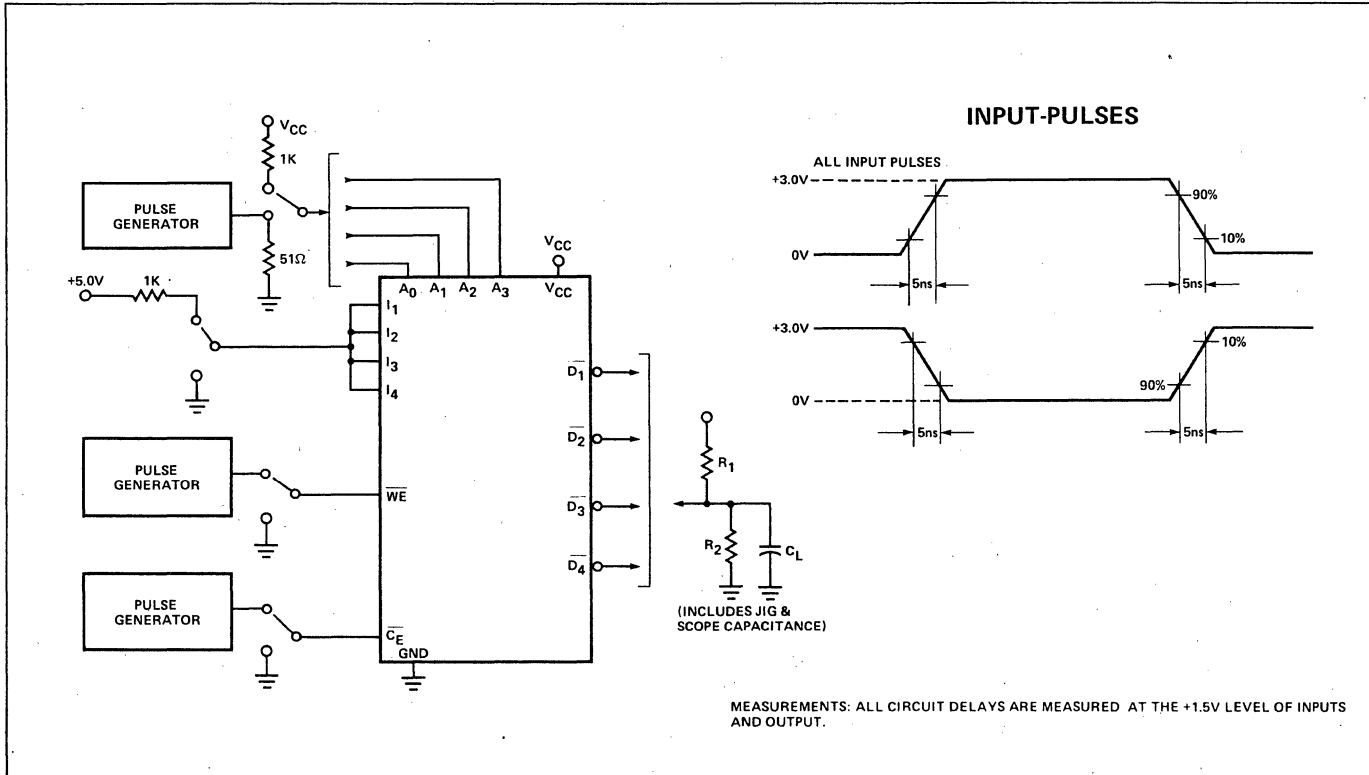
RAMS

Random Access Memories

Signetics offers a complete line of Schottky-clamped TTL, read/write memory arrays. All feature open collector or tri-state output options for optimization of word expansion in bussed organizations. Memory expansion is further enhanced by full on-chip address decoding, chip enable function, and PNP input transistors which reduce input loading requirements.

All devices offer high performance read access and write cycle times making these devices ideally suited in high speed memory applications such as "caches", buffers, scratch pads, writeable control store, main store, etc.

AC TEST LOAD AND WAVEFORMS



Signetics

MEMORY

SIGNETICS BIPOLAR RAMS PRODUCT INFORMATION

SWITCHING CHARACTERISTICS S82S $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
 N82S $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

# OF BITS	DEVICE	PROPAGATION DELAYS														
		T_{AA} (ns)			T_{CE} (ns)			T_{CD} (ns)			T_{WD} (ns)		T_{WR} (ns)			
		ADDRESS ACCESS TIME			CHIP ENABLE ACCESS TIME			CHIP DISABLE TIME			WRITE ENABLE TO OUTPUT DISABLE TIME		WRITE ENABLE TO OUTPUT DISABLE TIME			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
	$C_L = 30\text{ pF}$ $R_1 = 270\Omega$ $R_2 = 600\Omega$															
64	82S21		40	50		40	50		40	50		30	40			
	82S25	S	35	60		20	35		20	35		20	30		35	60
		N	35	50		20	35		20	35		20	25		35	50
	3101A	S	25	50		12	25		12	25		15	25		22	40
		N	10	35		5	17		5	17			20			35
256	82S16	S	40	70		30	40		30	40		30	55			
		N	40	50		30	40		30	40		30	40			
	82S17	S	40	70		30	40		30	40		30	55			
		N	40	50		30	40		30	40		30	40			
	82S116	N	30	40		15	25		15	25		30	40			
	82S117	N	30	40		15	25		15	25		30	40			
	$C_L = 15\text{ pF}$ $R_1 = 270\Omega$ $R_2 = 1\text{ k}\Omega$															
	54/74S200	54	40	70		45		30		40			50			
		74	40	50		35		20		30			40			
	54/74S201	54	40	70		45		30		40			50			
		74	40	50		35		20		30			40			
	54/74S301	54	40	70		45		30		40			50			
576		74	40	50		35		20		30			40			
	$C_L = 30\text{ pF}$ $R_1 = 600\Omega$ $R_2 = 900\Omega$															
	82S09	S	30	80		15	50		15	50		N/A				
1024		N	30	45		15	30		15	30						
	$R_1 = 270\Omega$ $R_2 = 600\Omega$															
	82S10	S	30	70		15	45		15	45		20	45		20	45
		N	30	45		15	30		15	30		20	30		20	30
	82S11	S	30	70		15	45		15	45		20	45		20	45
		N	30	45		15	30		15	30		20	30		20	30
	93415A		30	45		15	30		15	30		20	30		20	30
	93425A		30	45		15	30		15	30		20	30		20	30

MEMORY Signetics

SWITCHING CHARACTERISTICS (Continued)

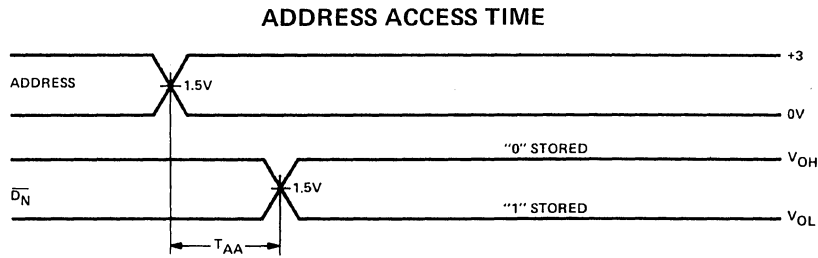
# OF BITS	DEVICE	WRITE SET-UP TIMES			WRITE HOLD TIMES											
		T _{WSA} (ns)		T _{WSD} (ns)		T _{WSC} (ns)		T _{WHA} (ns)		T _{WHD} (ns)		T _{WHC} (ns)		T _{Wp} (ns)		
		ADDRESS TO WRITE ENABLE		DATA IN TO WRITE ENABLE		CE TO WRITE ENABLE		ADDRESS TO WRITE ENABLE		DATA IN TO WRITE ENABLE		CE TO WRITE ENABLE		WRITE ENABLE PULSE WIDTH		
		MIN	TYP	MIN	TYP	MIN	TYP	MIN	TYP	MIN	TYP	MIN	TYP	MIN	TYP	
	C _L = 30 pF R ₁ = 270Ω R ₂ = 600Ω															
64	82S21		15 10	25		15 10		5 0		5 0		5 0		25		
	82S25	S	10 -8	25 5		0 -5		10 0		10 -3		5 0		30 18		
		N	0 -8	20		0 -5		5 0		5 -3		5 0		30 18		
	3101A	S	0	25		0		0		0		0		25 18		
256		N	0 -8	20 5		0 -5		0		0 -3		0		25 18		
	82S16	S	20 5	50 40		10 0		10 0		10 0		10 0		40 20		
		N	20 5	40 30		10 0		5 0		5 0		5 0		30 15		
	82S17	S	20 5	50 40		10 0		10 0		10 0		10 0		40 20		
		N	20 5	40 30		10 0		5 0		5 0		5 0		30 15		
	82S116	N	0 -5	25 15		0 -5		0 -5		0 -5		0 -5		25 15		
	82S117	N	0 -5	25 15		0 -5		0 -5		0 -5		0 -5		25 15		
		C _L = 15 pF R ₁ = 270Ω R ₂ = 1 kΩ														
	54/74S200	54	0	50		0		10		10		0		50		
		74	0	40		0		10		10		0		40		
576	54/74S201	54	0	50		0		10		10		0		50		
		74	0	40		0		10		10		0		40		
	54/74S301	54	0	50		0		10		10		0		50 25		
		74	0	40		0		10		10		0		40 25		
	82S09	S	10 0	50 25		10 0		10 0		5 0		10 0		50 25		
		N	5 0	35 25		5 0		5 0		5 0		5 0		35 25		
1024		R ₁ = 270Ω R ₂ = 600Ω														
	82S10	S	15 0	55 35		5 0		10 0		5 0		5 0		50 25		
		N	5 0	40 35		5 0		5 0		5 0		5 0		35 25		
	82S11	S	15 0	55 35		5 0		10 0		5 0		5 0		50 25		
		N	5 0	40 35		5 0		5 0		5 0		5 0		35 25		
	93415A		5 0	40 35		5 0		5 0		5 0		5 0		35 25		
93425A		5 0	40 35		5 0		5 0		5 0		5 0		35 25			

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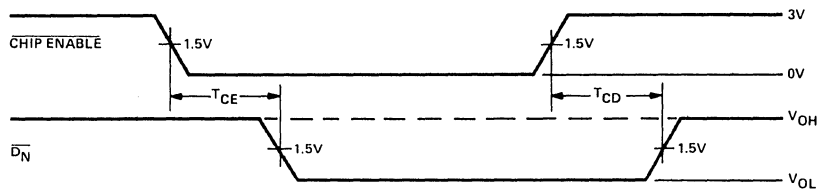
MEMORY

SWITCHING PARAMETERS MEASUREMENT INFORMATION

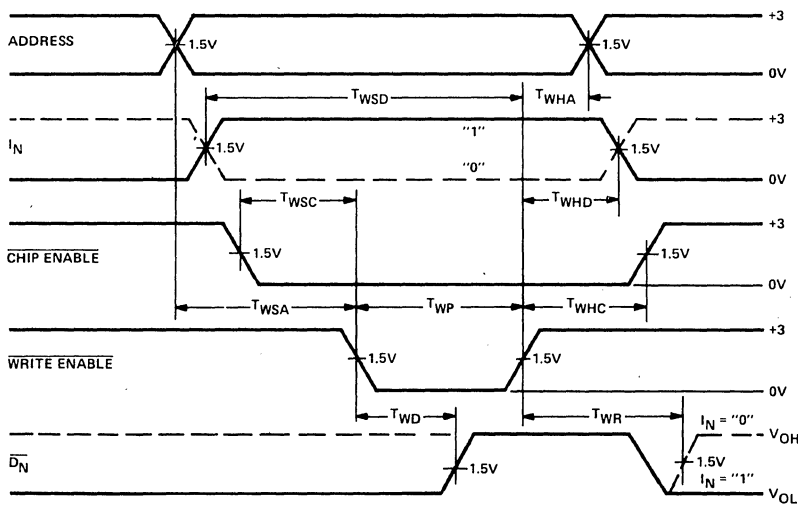
READ CYCLE



CHIP ENABLE/DISABLE TIMES



WRITE CYCLE



MEMORY TIMING DEFINITIONS

- T_{WR} Delay between end of WRITE ENABLE pulse and when DATA OUTPUT becomes valid. (Assuming ADDRESS still valid — not as shown.)
- T_{CE} Delay between beginning of CHIP ENABLE low (with ADDRESS valid) and when DATA OUTPUT becomes valid.
- T_{CD} Delay between when CHIP ENABLE becomes high and DATA OUTPUT is in off state.
- T_{AA} Delay between beginning of valid ADDRESS (with CHIP ENABLE low) and when DATA OUTPUT becomes valid.
- T_{WSC} Required delay between beginning of valid CHIP ENABLE and beginning of WRITE ENABLE pulse.

- T_{WHD} Required delay between end of WRITE ENABLE pulse and end of valid INPUT DATA.
- T_{WP} Width of WRITE ENABLE pulse.
- T_{WSA} Required delay between beginning of valid ADDRESS and beginning of WRITE ENABLE pulse.
- T_{WSD} Required delay between beginning of valid DATA INPUT and end of WRITE ENABLE pulse.
- T_{WD} Delay between beginning of WRITE ENABLE pulse and when DATA OUTPUT is in off state.
- T_{WHC} Required delay between end of WRITE ENABLE pulse and end of CHIP ENABLE.
- T_{WHA} Required delay between end of WRITE ENABLE pulse and end of valid ADDRESS.

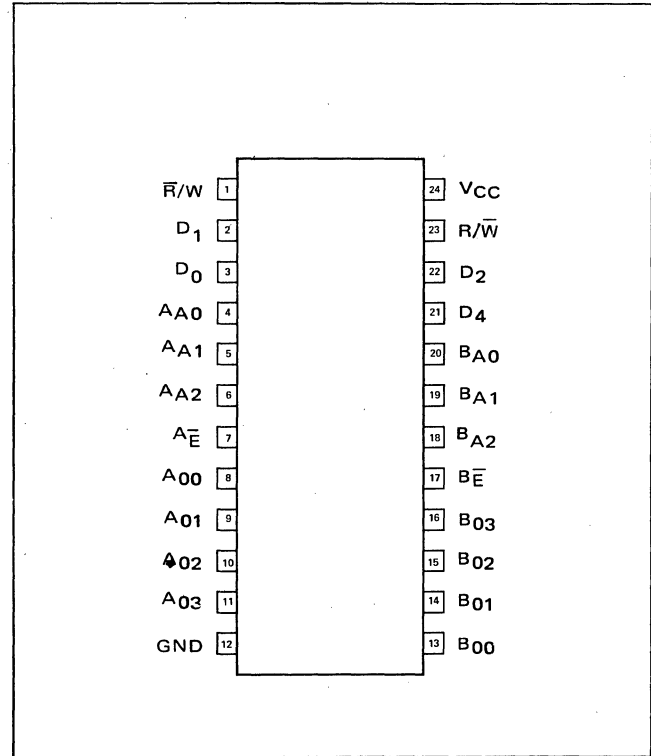
DESCRIPTION

The 82S12/112 is a Schottky TTL 32 bit multipoint memory organized in 8 words of 4 bits each. The device is ideally suited for high speed accumulators and buffer memories.

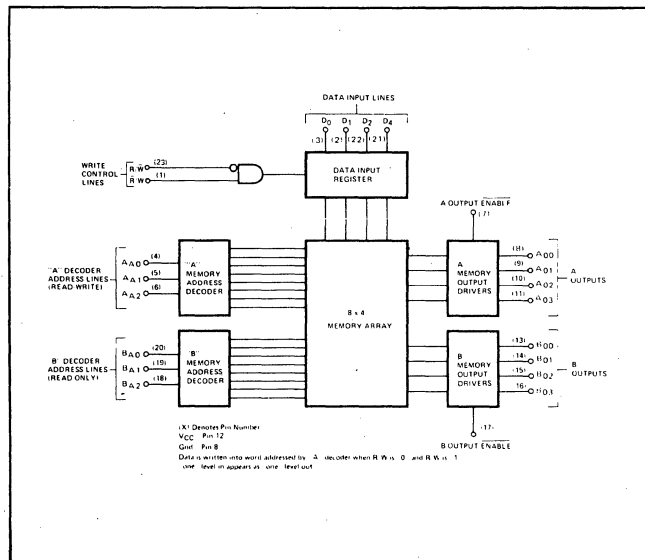
Stored data is addressed through 2 independent sets of 3-input decoders, and read out when the corresponding output enable line is low. Two separate word locations can, therefore, be read at the same time by enabling both the A and B output drivers. In addition, data can be read and written at the same time by utilizing the "A" address to specify the location of the word to be written, and the "B" address to specify the word to be read.

The 82S12/112 can be used in larger memory arrays since it includes all the control logic required to disable the chip and the outputs are open-collector devices suitable for "Wire-ORing."

PIN CONFIGURATION



BLOCK DIAGRAM



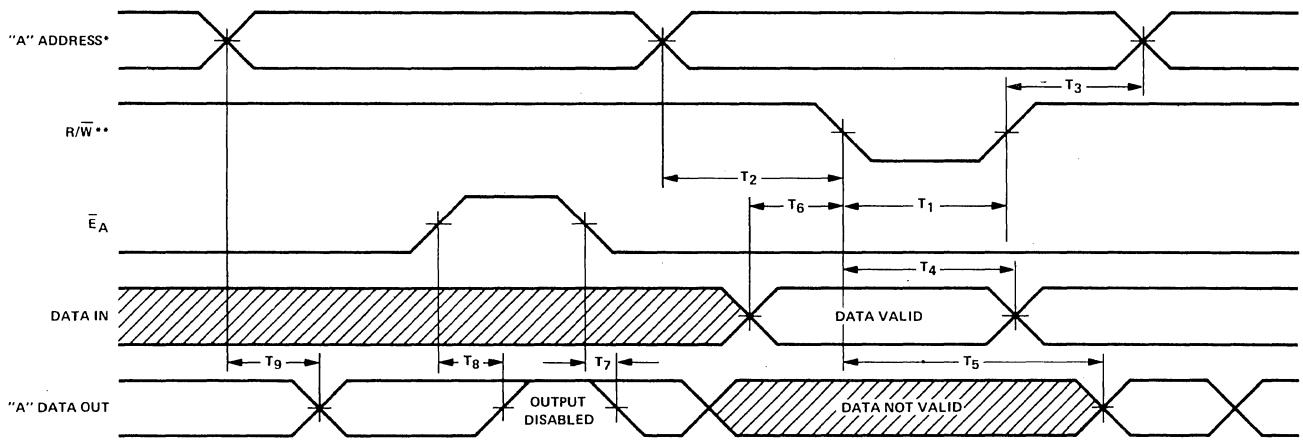
TRUTH TABLE

R/W	R/W-bar	A OUTPUT ENABLE	B OUTPUT ENABLE	MODE	OUTPUTS	
					A	B
0	X	1	1	Outputs Disabled	"1"	"1"
0	X	1	0	Read	"1"	Data
0	X	0	1	Read	Data	"1"
0	X	0	0	Read	Data	Data
1	1	1	1	Read	"1"	"1"
1	1	1	0	Read	"1"	Data
1	1	0	1	Read	Data	"1"
1	1	0	0	Read	Data	Data
1	0	1	1	Write	"1"	"1"
1	0	1	0	Write	"1"	Data
						Address
1	0	0	1	Write	Data Being Written	"1"
1	0	0	0	Write	Data Being Written	Data "B"

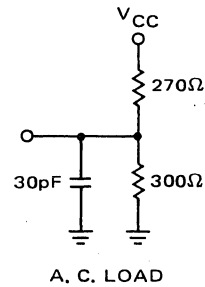
Signetics

MEMORY

TIMING DIAGRAM



- T₁ WRITE PULSE WIDTH – Width of write pulse (when R/W="1" and R/W="0")
- T₂ ADDRESS SETUP TIME – Required delay between beginning of valid Address and beginning of Write pulse.
- T₃ ADDRESS HOLD TIME – Required delay between end of Write pulse and end of valid Address.
- T₄ DATA INPUT HOLD TIME – Required delay between start of Write pulse and end of Valid Data input.
- T₅ WRITE ACCESS TIME – Delay between beginning of Write pulse and Data Out at new value.
- T₆ DATA INPUT SET-UP TIME – Required delay between beginning of Valid Data Input and start of Write pulse.
- T₇ OUTPUT ENABLE TIME – Delay between beginning of Output Enable high and when Data Output becomes valid.
- T₈ OUTPUT DISABLE TIME – Delay between when Output Enable becomes low and Data Output is in off state.
- T₉ ADDRESS ACCESS TIME – Delay between beginning of Valid Address (with Output Enable high, R/W high and R/W low) and when Data Output becomes valid.



NOTES

- **B** Address functions identically in read mode. No write mode through B address decoder.
- **R/W** input is either the reverse of R/W or held high.
- Outputs can be disabled during write cycle to penetrate a known output state during write.

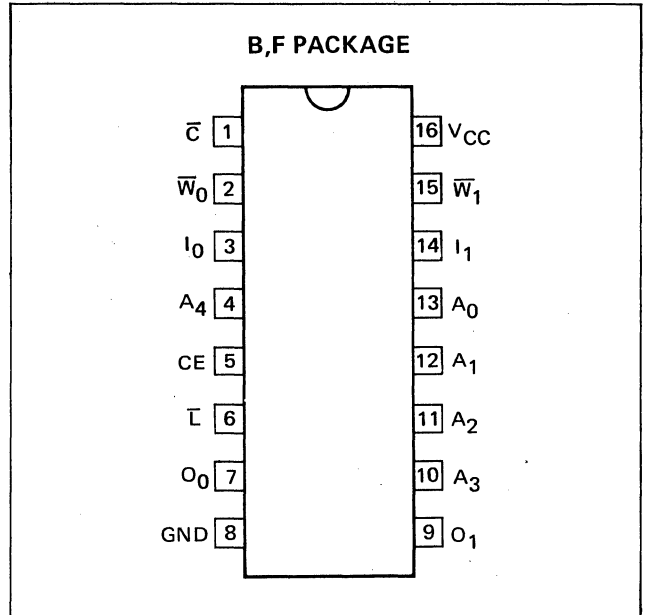
DESCRIPTION

The 82S21 is a TTL 64 bit Write-While-Read Random Access Memory organized in 32 words of 2 bits each. The 82S21 is ideally suited for high speed buffers and as the memory element in high speed accumulators.

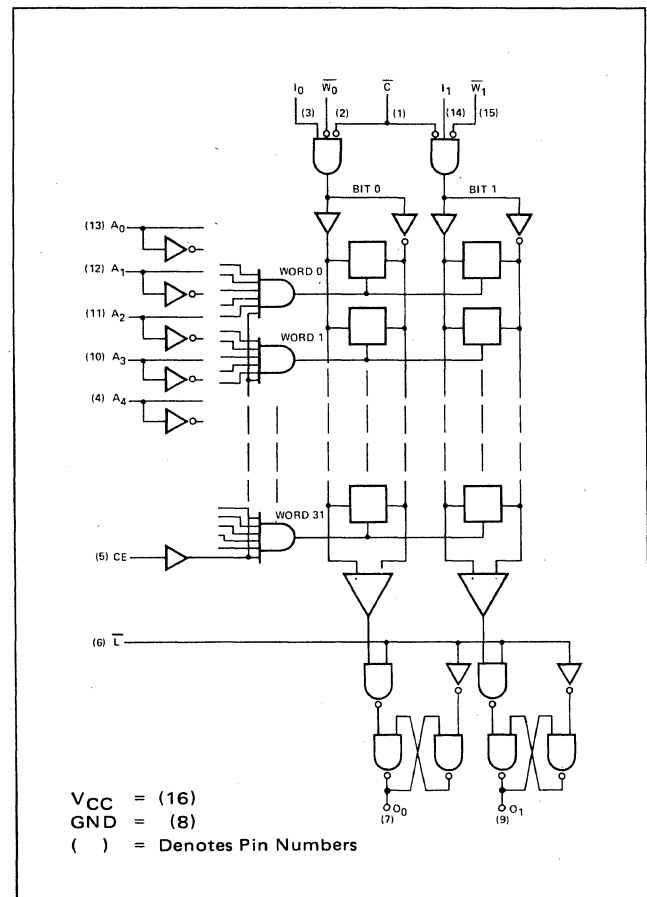
Words are selected through a 5 input decoder when the Read-Write enable input, \overline{CE} is at logic "1". $\overline{W_0}$ and $\overline{W_1}$ are the write inputs for bit 0 and bit 1 of the word selected. \overline{C} is the write control input. When $\overline{W_X}$ and \overline{C} are both at logic "0" data on the I_0 and I_1 data lines are written into the addressed word. The read function is enabled when either $\overline{W_X}$ or \overline{C} is at logic "1".

An internal latch is on the chip to provide the Write-While-Read capability. When the latch control line, \overline{L} , is logic "1" and data is being read from the 82S21, the latch is effectively bypassed. The data at the output will be that of the addressed word. When \overline{L} goes from a logic "1" to logic "0" the outputs are latched and will remain latched regardless of the state of any other address or control line. When \overline{L} goes from "0" to "1" the outputs unlatch and the outputs will be that of the present address word.

PIN CONFIGURATION



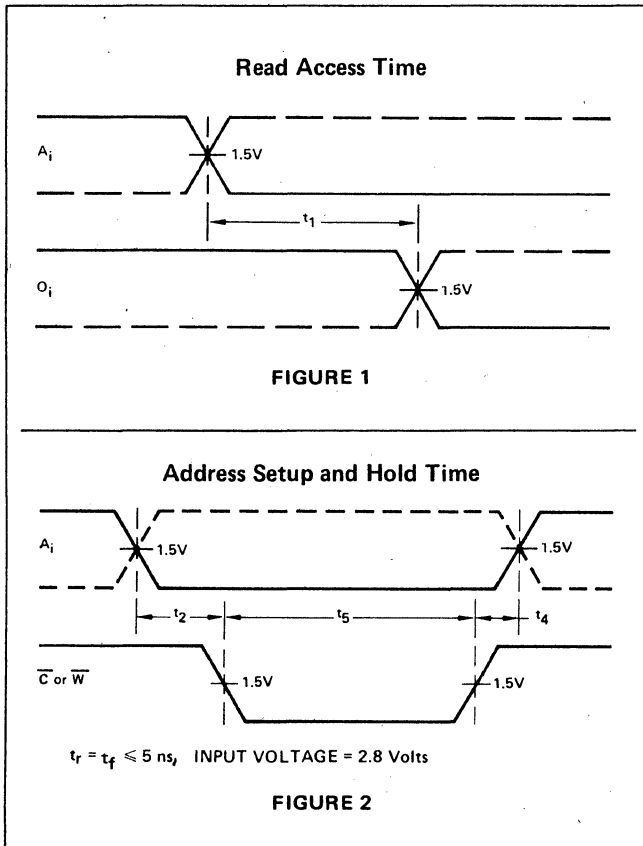
LOGIC DIAGRAM



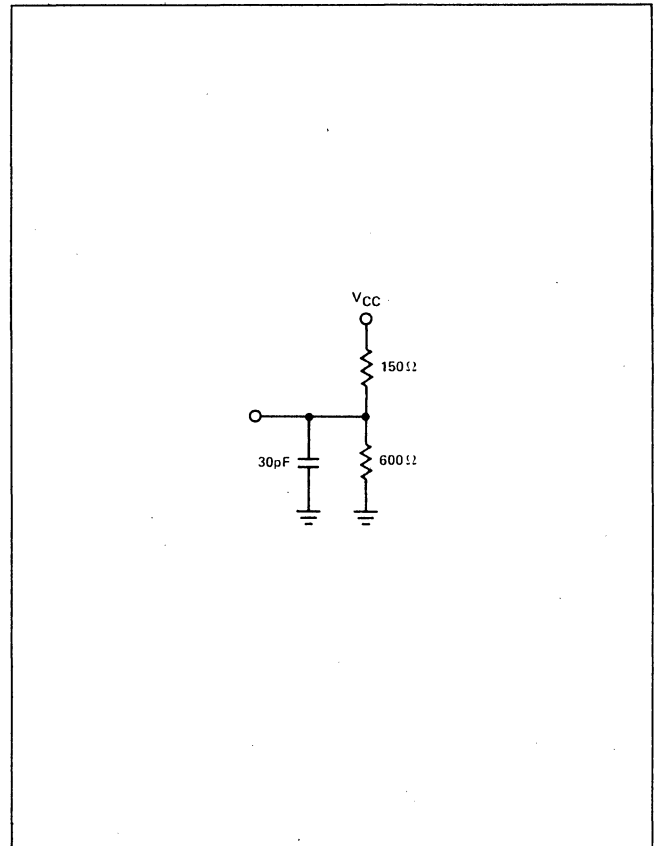
TRUTH TABLE

CE	\bar{C}	\bar{W}_0	\bar{W}_1	\bar{L}	Mode	Outputs
X	X	X	X	0	Output Hold	Data from last addressed word when CE = "1"
0	X	X	X	1	Read & Write Disabled	Disabled logic "1"
1	1	X	X	X	Read	Data stored in addressed word
1	0	1	1	X	Read	Data stored in addressed word
1	0	0	0	0	Write Data	Data from last word address when L went from "1" to "0"
1	0	0	0	1	Write Data	Data being written into memory
1	0	0	1	X	Write Data into Bit 0 Only	If $\bar{L} = 0$: Data from last word address when L went from "1" to "0"
1	0	1	0	X	Write Data into Bit 1 Only	If $\bar{L} = 1$: Data being written into the selected bit location and stored in other addressed location

AC WAVEFORM

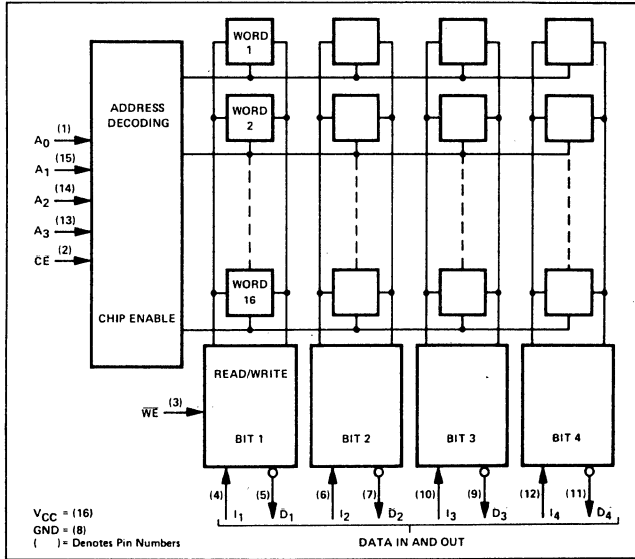


TEST LOAD

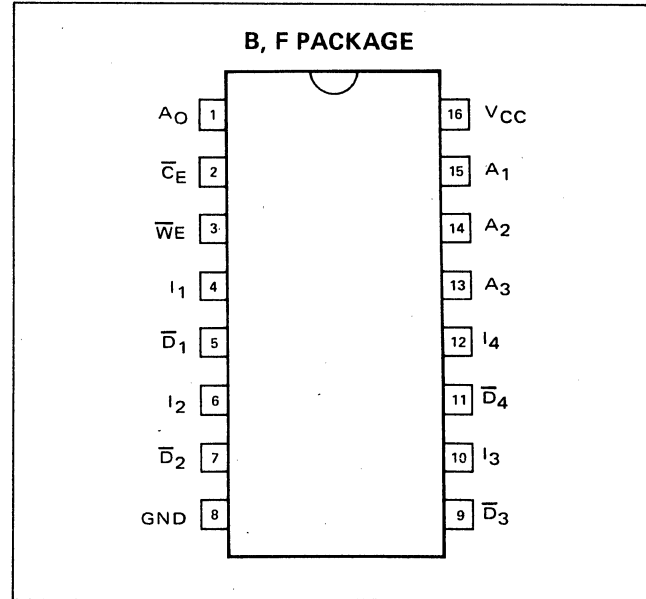


N82S25-B,F • S82S25-F
N3101A-B,F • S3101A-F

BLOCK DIAGRAM



PIN CONFIGURATION



TRUTH TABLE

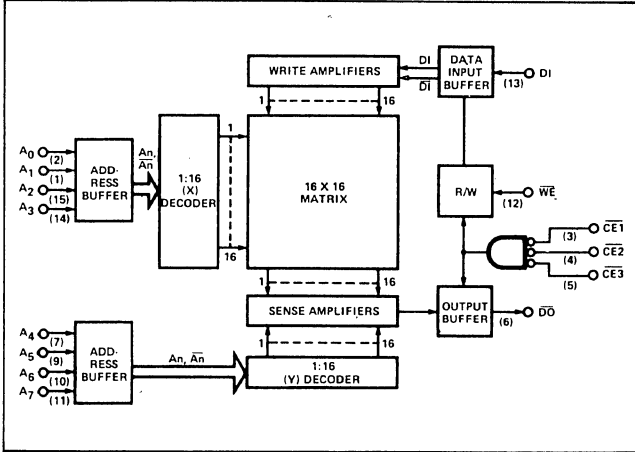
MODE	\overline{CE}	\overline{WE}	I_n	\overline{D}_n
Read	0	1	X	Complement of data stored
Write "0"	0	0	0	1
Write "1"	0	0	1	1
Disabled	1	X	X	1

X = Don't care.

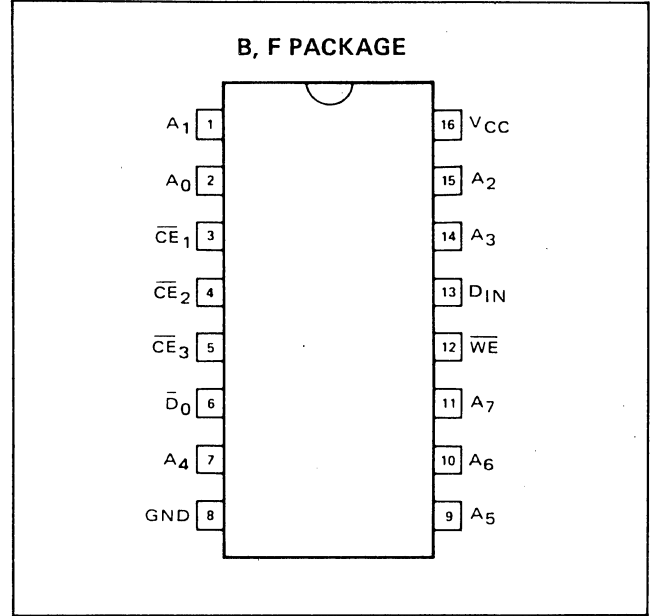
82S16
82S17
82S116
82S117
54/74S200
54/74S201
54/74S301

N82S16/17/116/117-B,F
54S200/201/301-F
74S200/201/301-B,F

BLOCK DIAGRAM



PIN CONFIGURATION



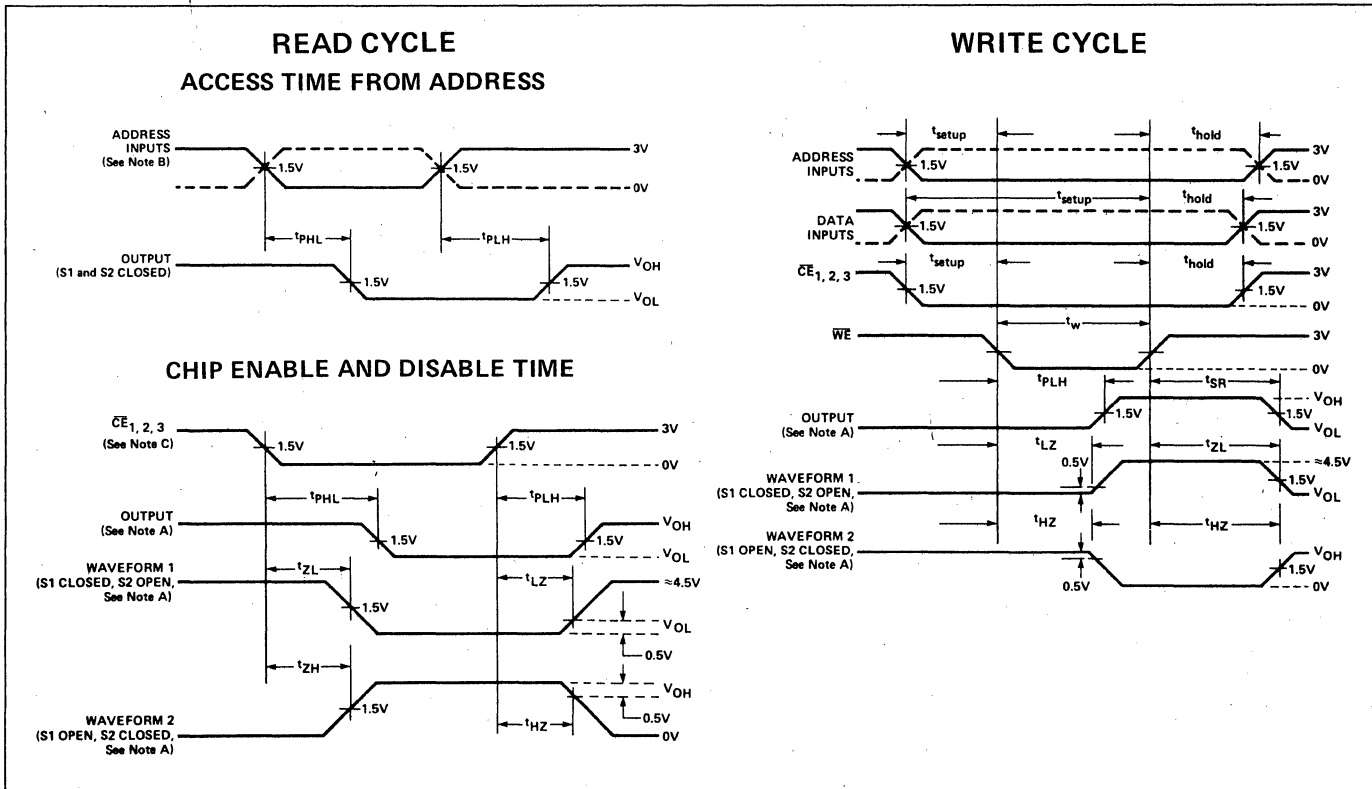
TRUTH TABLE

MODE	\overline{CE}^*	\overline{WE}	D _{IN}	\overline{DOUT}			
				82S16/116	82S17/117	54/74S 200/201	54/74S301
READ	0	1	X	STORED \overline{DATA}	STORED \overline{DATA}	STORED \overline{DATA}	STORED \overline{DATA}
WRITE "0"	0	0	0	1	1	HIGH-Z	1
WRITE "1"	0	0	1	0	0	HIGH-Z	1
DISABLED	1	X	X	High-Z	1	HIGH-Z	1

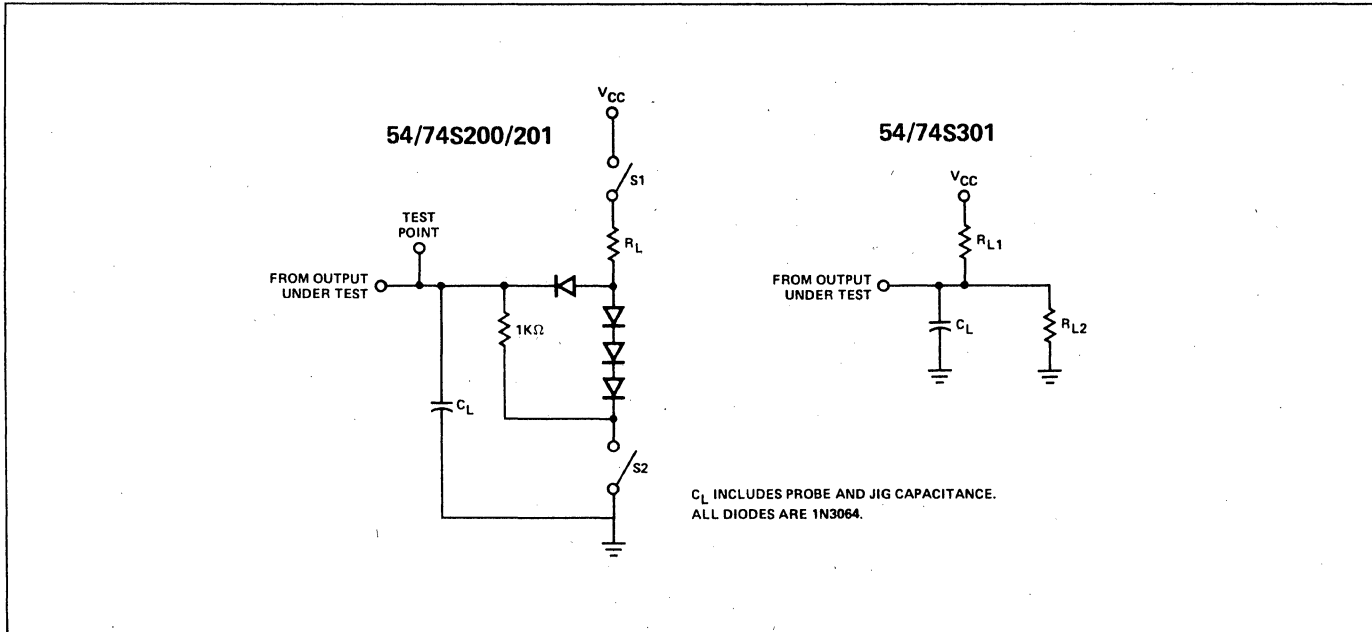
*"0" = All \overline{CE} inputs low; "1" = one or more \overline{CE} inputs high.

X = Don't care.

SWITCHING PARAMETER MEASUREMENT INFORMATION



AC TEST LOAD



NOTES:

- A. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
- B. When measuring delay times from address inputs, the chip enable inputs are low and the write enable input is high.
- C. When measuring delay times from chip enable inputs, the address inputs are steady-state and the write enable input is high.
- D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5\text{ns}$, $t_f \leq 2.5\text{ns}$, $\text{PRR} \leq 1\text{MHz}$, and $Z_{\text{out}} \approx 50\Omega$.
- E. t_{PLH} propagation delay time, low-to-high-level output, t_{PHL} propagation delay time, high-to-low-level output.
- F. t_{ZH} propagation delay time, hi-Z to high-level output, t_{ZL} propagation delay time, hi-Z to low-level output.
- G. t_{HZ} propagation delay time, high-level to hi-Z output, t_{LZ} propagation delay time, low-level to hi-Z output.
- H. Minimum required to guarantee a WRITE into the slowest bit.

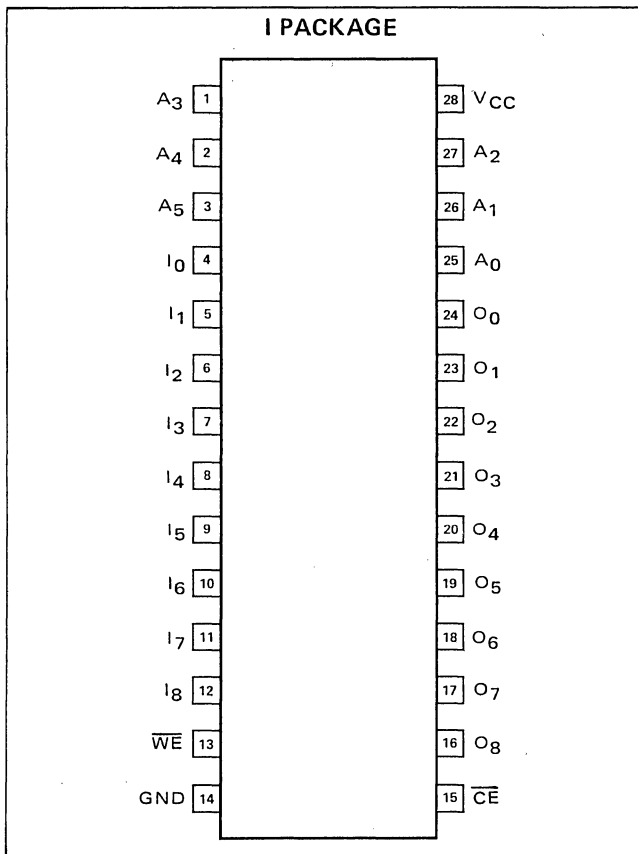
DESCRIPTION

The 82S09 is a 576-Bit, Schottky clamped TTL, random access memory, organized as 64X9. This organization allows byte manipulation of data, including parity. Where parity is not monitored, the ninth bit can be used as a flag or status indicator for each word stored. With a typical access time of 30ns, it is ideal for scratch-pad, push-down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09 is fully TTL compatible, and features open collector outputs, chip enable input, and a very low current PNP input structure to enhance memory expansion.

During WRITE operation, the logic state of the device output follows the complement of the data input being written. This feature allows faster execution of WRITE-READ cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a WRITE cycle.

PIN CONFIGURATION

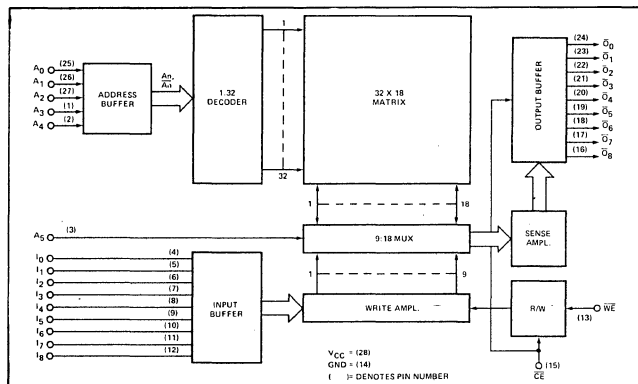


TRUTH TABLE

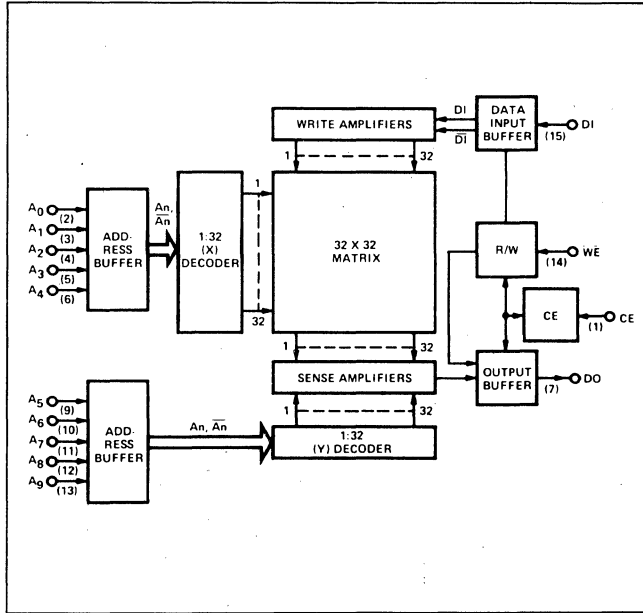
MODE	CE	WE	I _N	O _N
READ	0	1	X	Complement of Data Stored
WRITE "0"	0	0	0	1
WRITE "1"	0	0	1	0
DISABLED	1	X	X	1

X = Don't care.

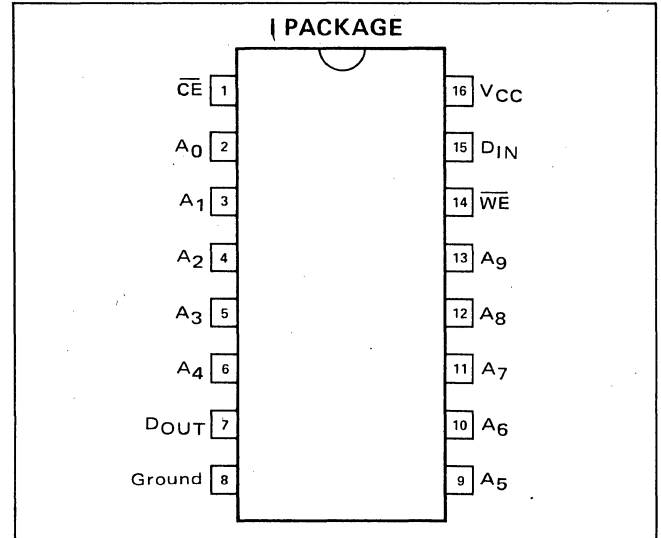
BLOCK DIAGRAM



BLOCK DIAGRAM



PIN CONFIGURATION



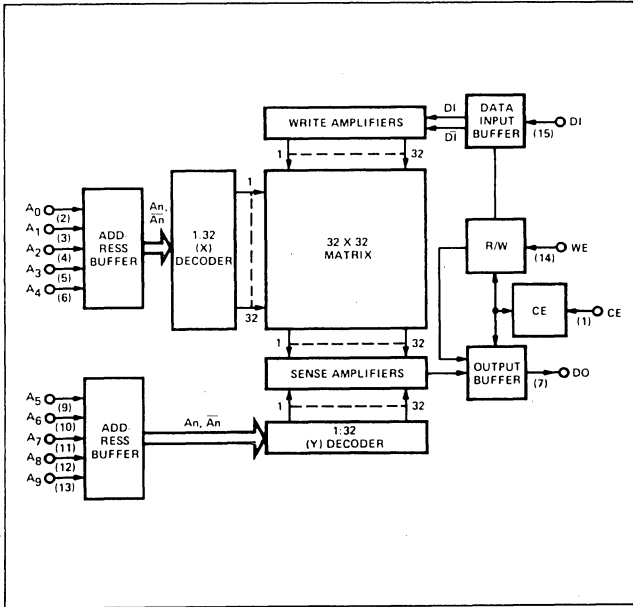
TRUTH TABLE

MODE	\overline{CE}	WE	D _{IN}	DOUT	
				82S10	82S11
READ	0	1	X	STORED DATA	STORED DATA
WRITE "0"	0	0	0	1	High-Z
WRITE "1"	0	0	1	1	High-Z
DISABLED	1	X	X	1	High-Z

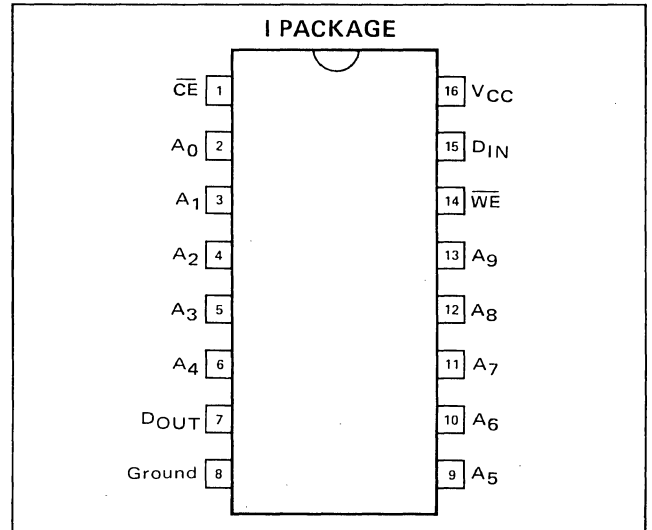
X = Don't care.

93415A-I, 93425A-I

BLOCK DIAGRAM



PIN CONFIGURATION



TRUTH TABLE

MODE	CE-bar	WE	D _{IN}	D _{OUT}	
				93415A	93425A
READ	0	1	X	STORED DATA	STORED DATA
WRITE "0"	0	0	0	1	High-Z
WRITE "1"	0	0	1	1	High-Z
DISABLED	1	X	X	1	High-Z

X = Don't care.

ROMS

Mask Programmable Read Only Memories

Signetics offers the industry's broadest line of High Performance Bipolar ROMs. Most Signetics ROMs have pin and performance compatible PROMs offering the user the ultimate in flexibility and long term cost reduction.

decoding and chip enable function for ease of memory expansion. Tri-state and open collector functions are available, and low input current requirements reduce the need for input buffering.

All ROMs are fully TTL compatible and include on-chip

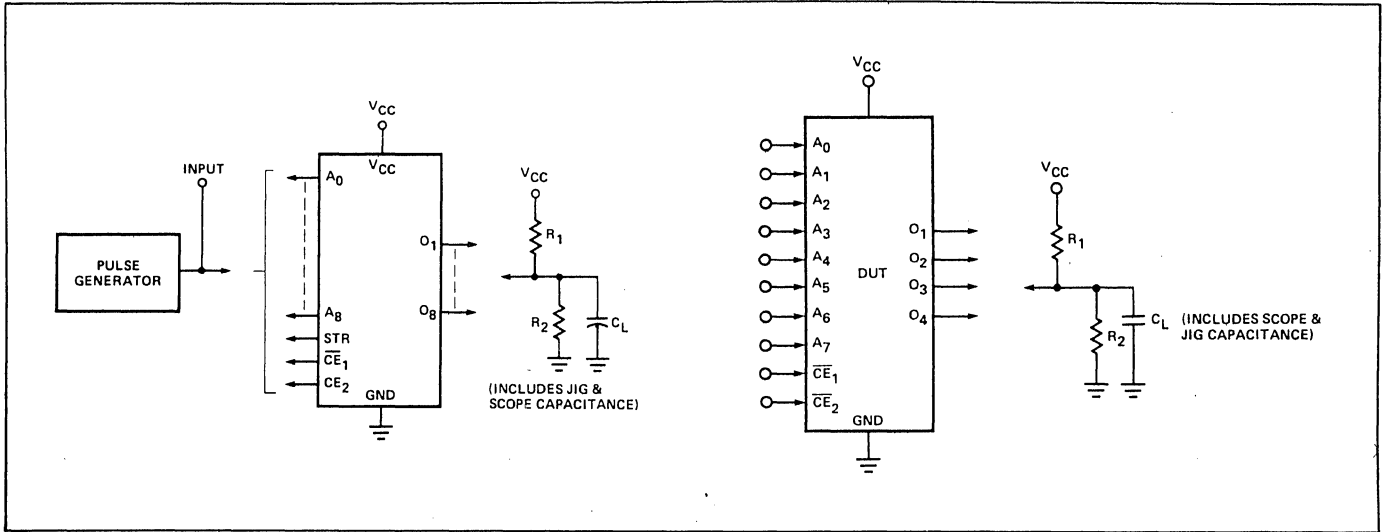
SWITCHING CHARACTERISTICS S82S $.55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
 N82S $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

# OF BITS	DEVICE	T_{AA} (ns)			T_{CE} (ns)			T_{CD} (ns)			
		ADDRESS ACCESS TIME			CHIP ENABLE ACCESS TIME			CHIP DISABLE TIME			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
1024	$C_L = 30\text{ pF}$ $R_1 = 270\Omega$ $R_2 = 600\Omega$ 82S226	S	35	70	15	35	15	35			
		N	35	50	15	20	15	20			
	82S229	S	35	70	15	35	15	35			
		N	35	50	15	20	15	20			
	2048	$R_1 = 470\Omega$ $R_2 = 1\text{k}\Omega$ 82S214	LATCHED OR TRANSPARENT READ ²			LATCHED OR TRANSPARENT READ ²			LATCHED OR TRANSPARENT READ ²		
			S	35	90	20	50	20	50		
82S215		N	35	60	20	40	20	40			
		S	35	90	20	50	20	50			
82S215		N	35	60	20	40	20	40			
		$R_1 = 270\Omega$ $R_2 = 600\Omega$ 82S230	S	40	70	20	30	20	30		
N			40	50	20	30	20	30			
82S231		S	40	70	20	30	20	30			
		N	40	50	20	30	20	30			
4096		8228	50	70 ⁴							

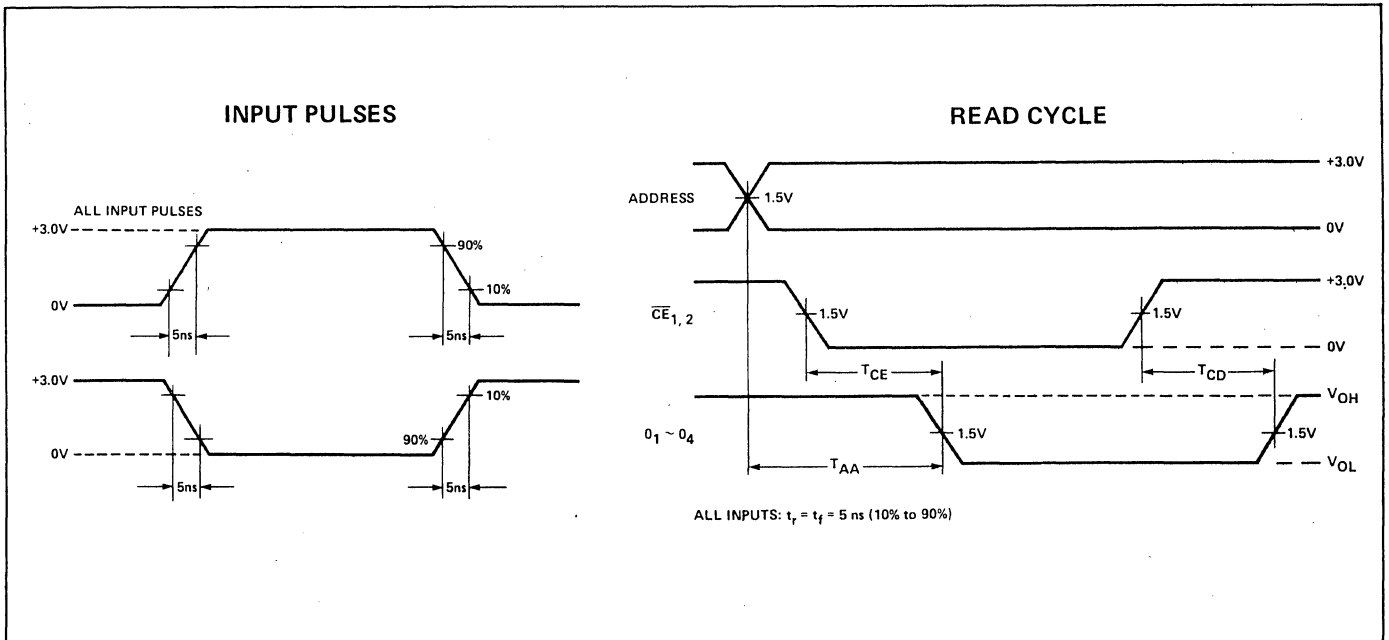
Signetics

MEMORY

AC TEST LOAD AND WAVEFORMS



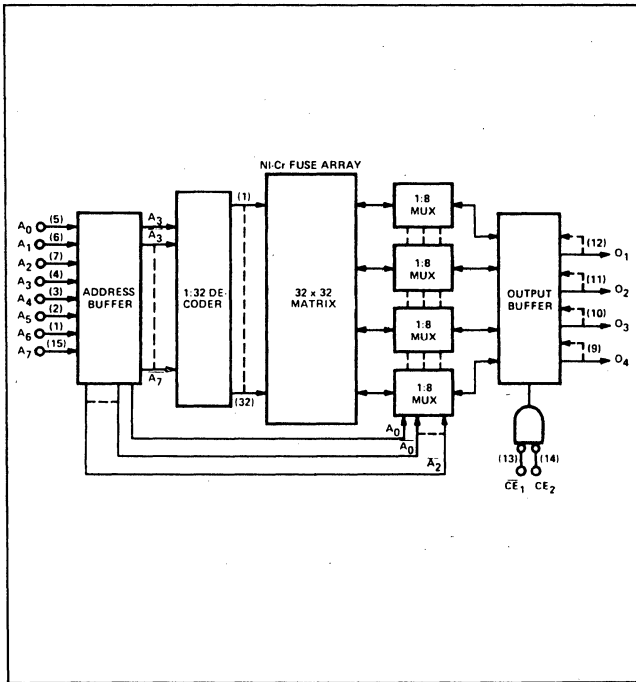
AC TEST FIGURE AND WAVEFORM



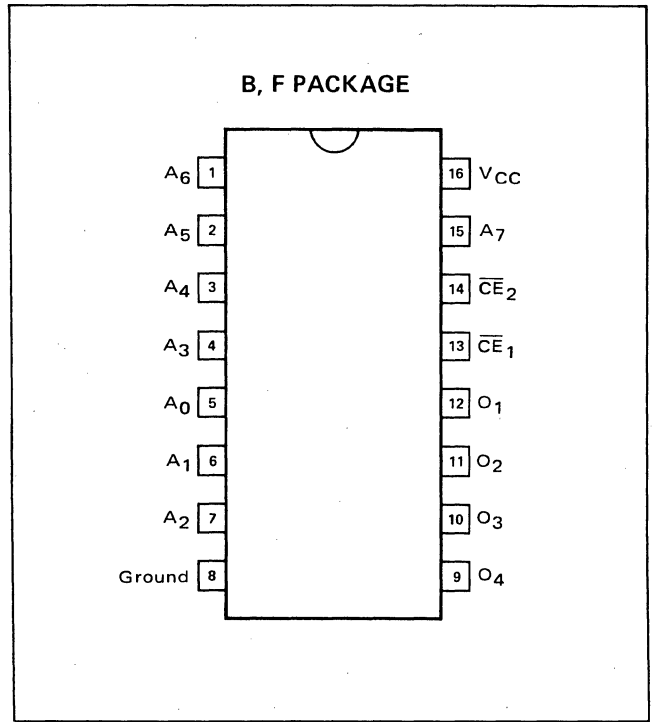
FULLY COMPATIBLE W/82S126

N82S226-B,F • S82S226-F

BLOCK DIAGRAM



PIN CONFIGURATION



FULLY COMPATIBLE W/82S114

N82S214-I • S82S214-I

DESCRIPTION

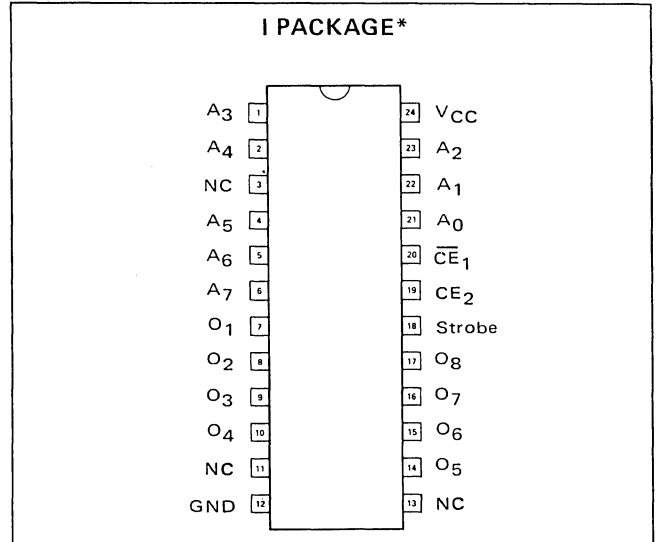
The 82S214 and 82S215 are Schottky-clamped Read Only Memories, incorporating on-chip data output registers.

The 82S214 and 82S215 are fully TTL compatible, and include on-chip decoding and two chip enable inputs for ease of memory expansion. They feature Tri-State outputs for optimization of word expansion in bussed organizations. A D-type latch is used to enable the Tri-State output drivers. In the TRANSPARENT READ mode, stored data is addressed by applying a binary code to the address inputs while holding STROBE high. In this mode the bit drivers will be controlled solely by $\overline{CE1}$ and CE2 lines.

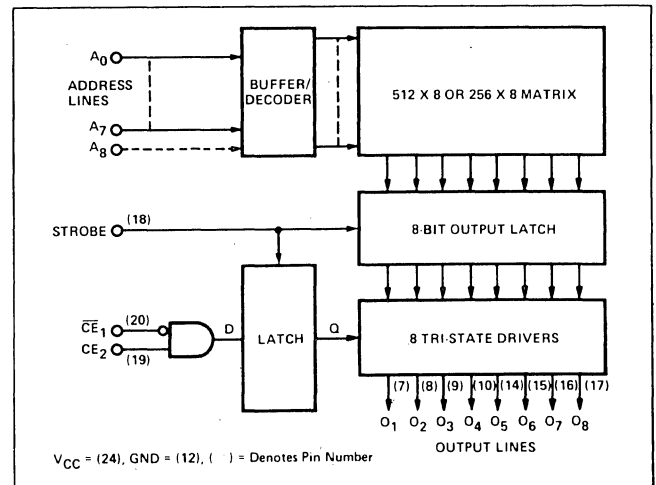
In the LATCHED READ mode, outputs are held in their previous state (1, 0, or high Z) as long as STROBE is low, regardless of the state of address or chip enable. A positive STROBE transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the high Z state if the chip is disabled.

A negative STROBE transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the high Z condition if the chip was disabled.

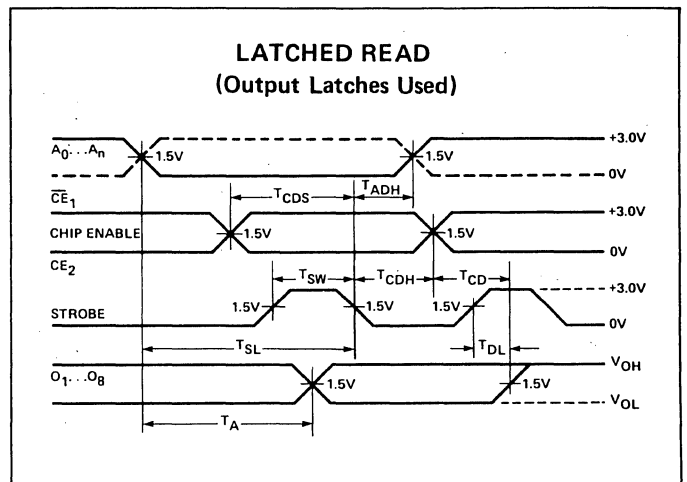
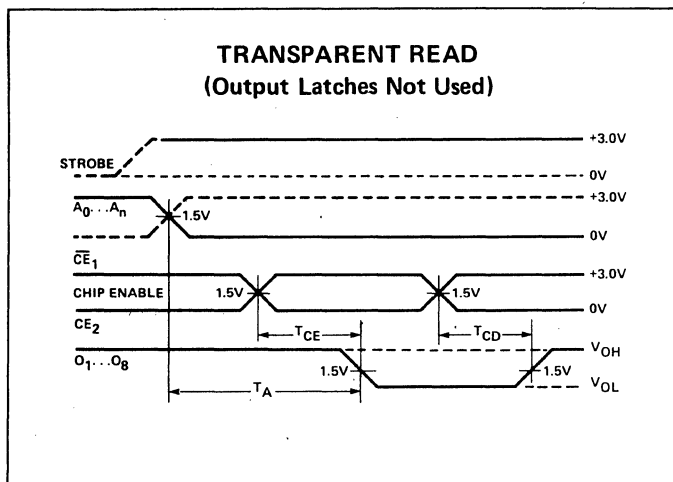
PIN CONFIGURATION



BLOCK DIAGRAM



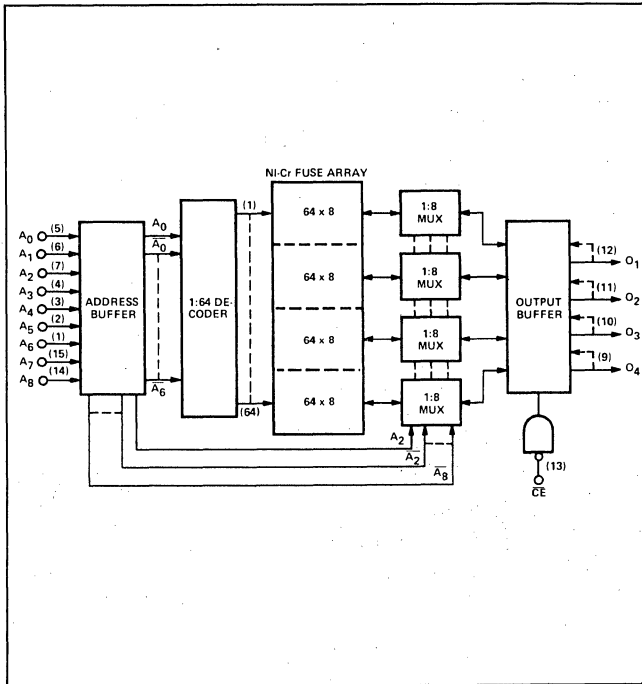
MEMORY TIMING



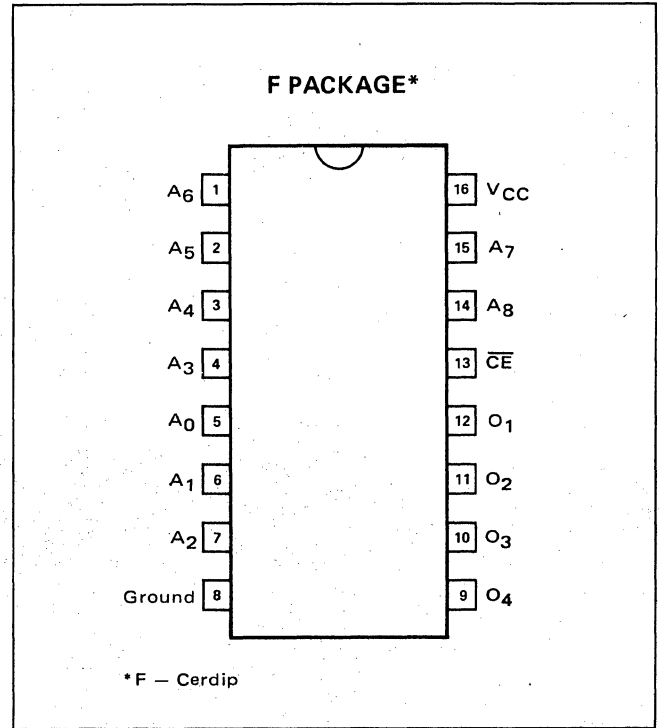
FULLY COMPATIBLE W/82S130

N82S230-F • S82S230-F

BLOCK DIAGRAM

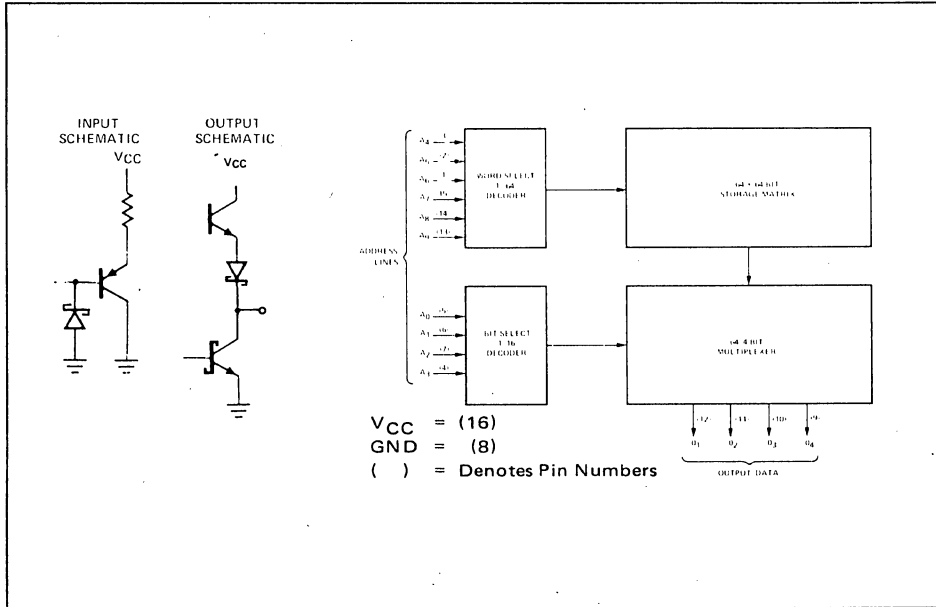


PIN CONFIGURATION

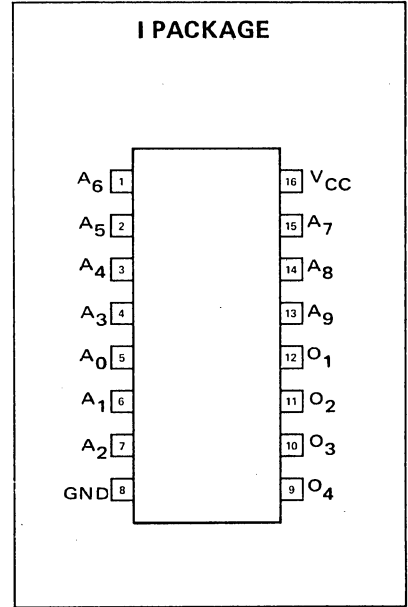


8228-1

BLOCK DIAGRAM



PIN CONFIGURATION



PROMS

Field Programmable Read Only Memories

Signetics offers the industry's broadest line of Bipolar High Performance PROMs. These PROMs are field programmable, which means that custom patterns are immediately available by following the provided fusing procedures. Signetics PROMs are supplied with all outputs at logical "0". Outputs are programmed to a logic "1" at any specified address by fusing a Ni-Cr link matrix.

decoding and chip enable functions for ease of memory expansion. Tri-state and open collector output functions are available, and low input currents reduce input buffer requirements.

Most Signetics PROMs also have pin and performance compatible ROMs, offering the user the ultimate in flexibility and cost reduction.

All PROMs are fully TTL compatible, and include on-chip

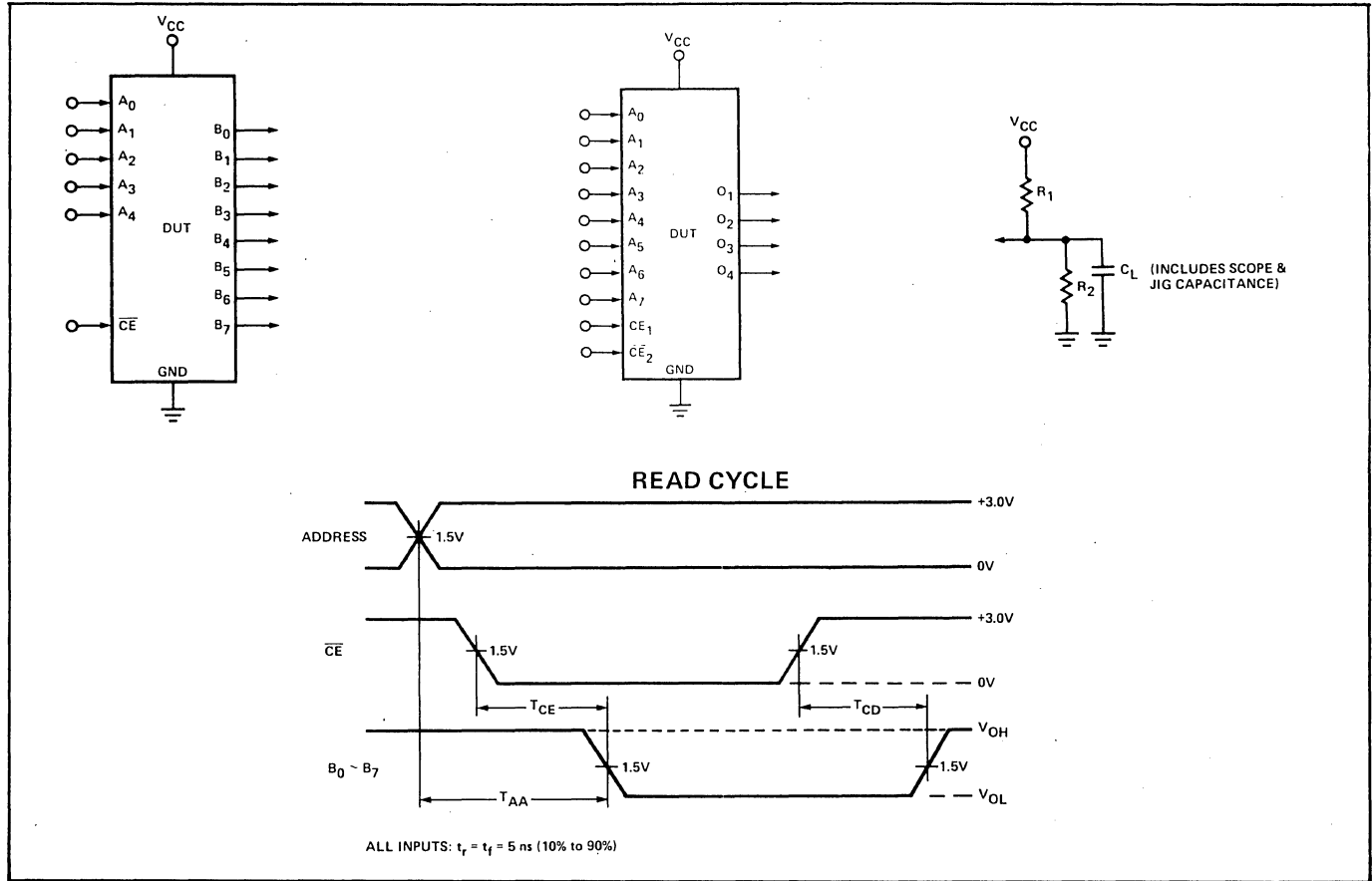
SWITCHING CHARACTERISTICS S82S $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
 N82S $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

			PROPAGATION DELAYS								
# OF BITS	DEVICE		T _{AA} (ns)			T _{CE} (ns)			T _{CD} (ns)		
			ADDRESS ACCESS TIME			CHIP ENABLE ACCESS TIME			CHIP DISABLE TIME		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
256	82S23	S		35	65		25	40		25	40
		N		35	50		25	35		25	35
	82S123	S		35	65		25	40		25	40
		N		35	50		25	35		25	35
	10139			15	20						
	1024	82S27	N		30	40		15	20		15
82S126		S		35	70		15	35		15	35
		N		35	50		15	20		15	20
82S129		S		35	70		15	35		15	35
		N		35	50		15	20		15	20
82S130		S		40	70		20	30		20	30
		N		40	50		20	30		20	30
82S131		S		40	70		20	30		20	30
		N		40	50		20	30		20	30
2048				LATCHED OR TRANSPARENT READ ²			LATCHED OR TRANSPARENT READ ²			LATCHED OR TRANSPARENT READ ²	
	82S114	N		35	60		20	40		20	40
	82S115	N		35	60		20	40		20	40

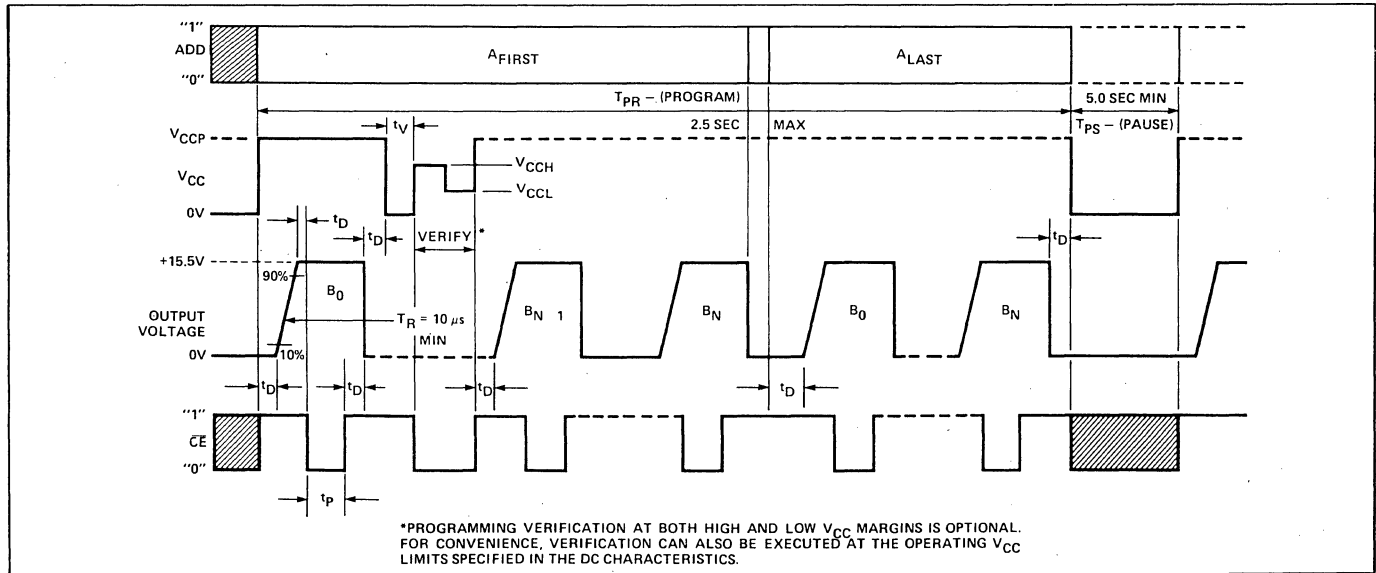
Signetics

MEMORY

AC TEST FIGURE AND WAVEFORM



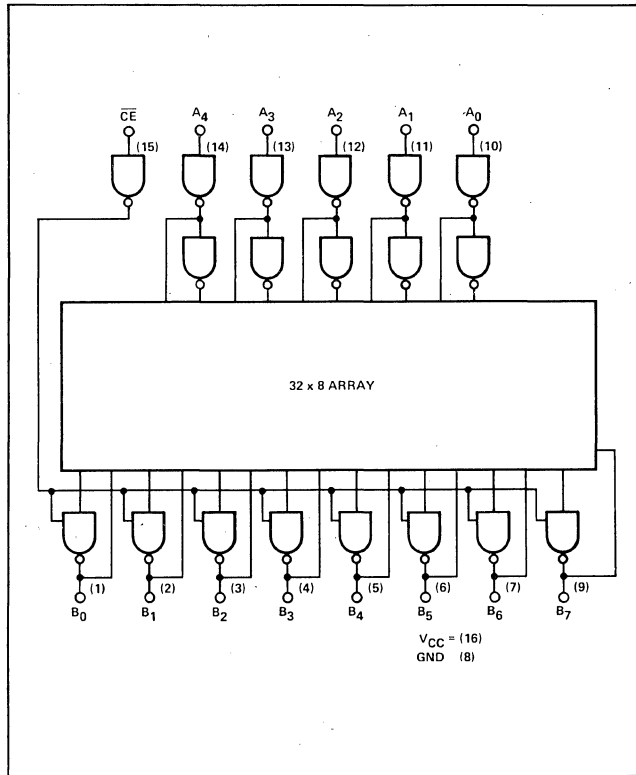
TYPICAL PROGRAMMING SEQUENCE



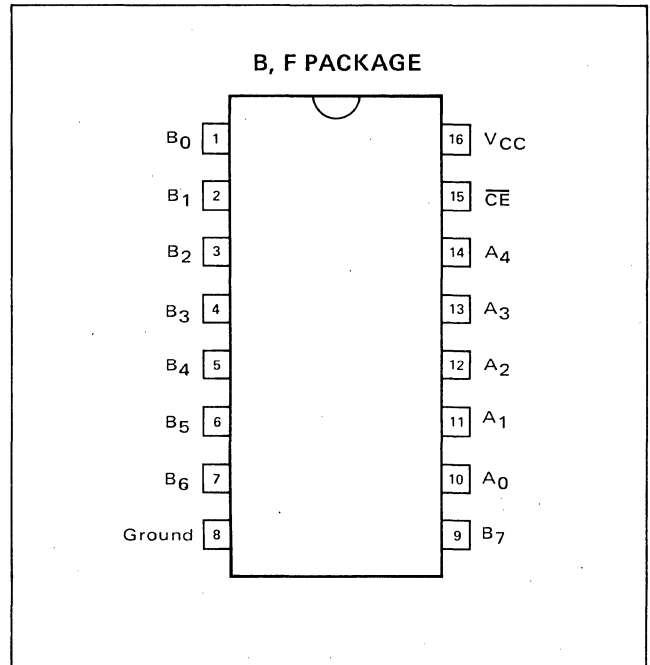
Signetics

MEMORY

LOGIC DIAGRAM

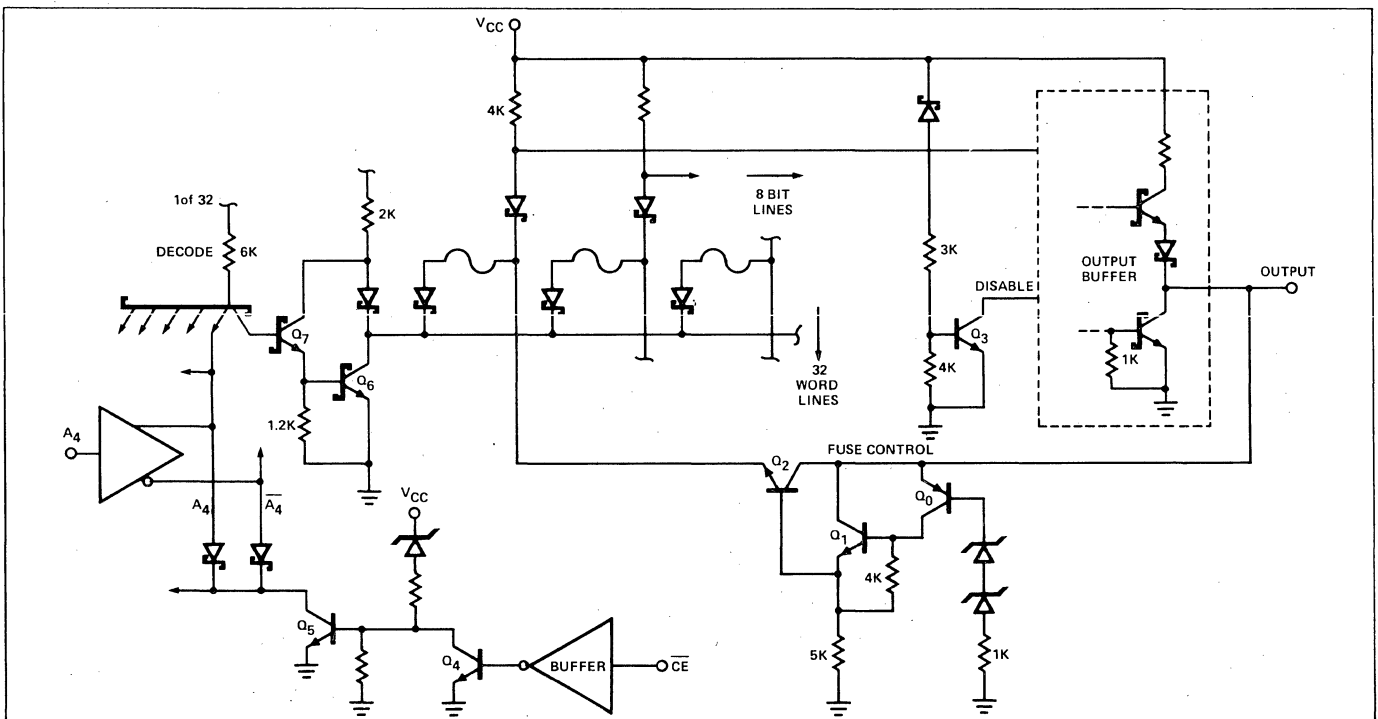


PIN CONFIGURATION



Signetics

TYPICAL FUSING PATH



MEMORY

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT		
		MIN	TYP	MAX			
Power Supply Voltage							
V_{CCP}^1	To Program	$I_{CCP} = 250 \pm 50\text{mA}$ (Transient or steady state)		9.5	10.0	10.5	V
V_{CCH}	Upper Verify Limit			5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit			4.3	4.5	4.7	V
V_S^3	Verify Threshold			0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +10.0 \pm 0.5\text{V}$		200	250	300	mA
Input Voltage							
V_{IH}	Logical "1"			2.4		5.5	V
V_{IL}	Logical "0"			0	0.4	0.8	V
Input Current							
I_{IH}	Logical "1"	$V_{IH} = +5.5\text{V}$				50	μA
I_{IL}	Logical "0"	$V_{IL} = +0.4\text{V}$				-500	μA
V_{OUT}^2	Output Programming Voltage	$I_{OUT} = 65 \pm 3\text{mA}$ (Transient or steady state)		15.0	15.5	16.0	V
I_{OUT}	Output Programming Current	$V_{OUT} = +15.5 \pm 0.5\text{V}$		62	65	68	mA
T_R	Output Pulse Rise Time			10		50	μs
t_p	$\overline{\text{CE}}$ Programming Pulse Width			1		2	ms
t_V	Verify Delay			50			μs
t_D	Pulse Sequence Delay			10			μs
T_{PR}	Programming Time	$V_{CC} = V_{CCP}$				2.5	sec
T_{PS}	Programming Pause	$V_{CC} = 0\text{V}$		5			sec
$\frac{T_{PR}^4}{T_{PR} + T_{PS}}$	Programming Duty Cycle					33	%

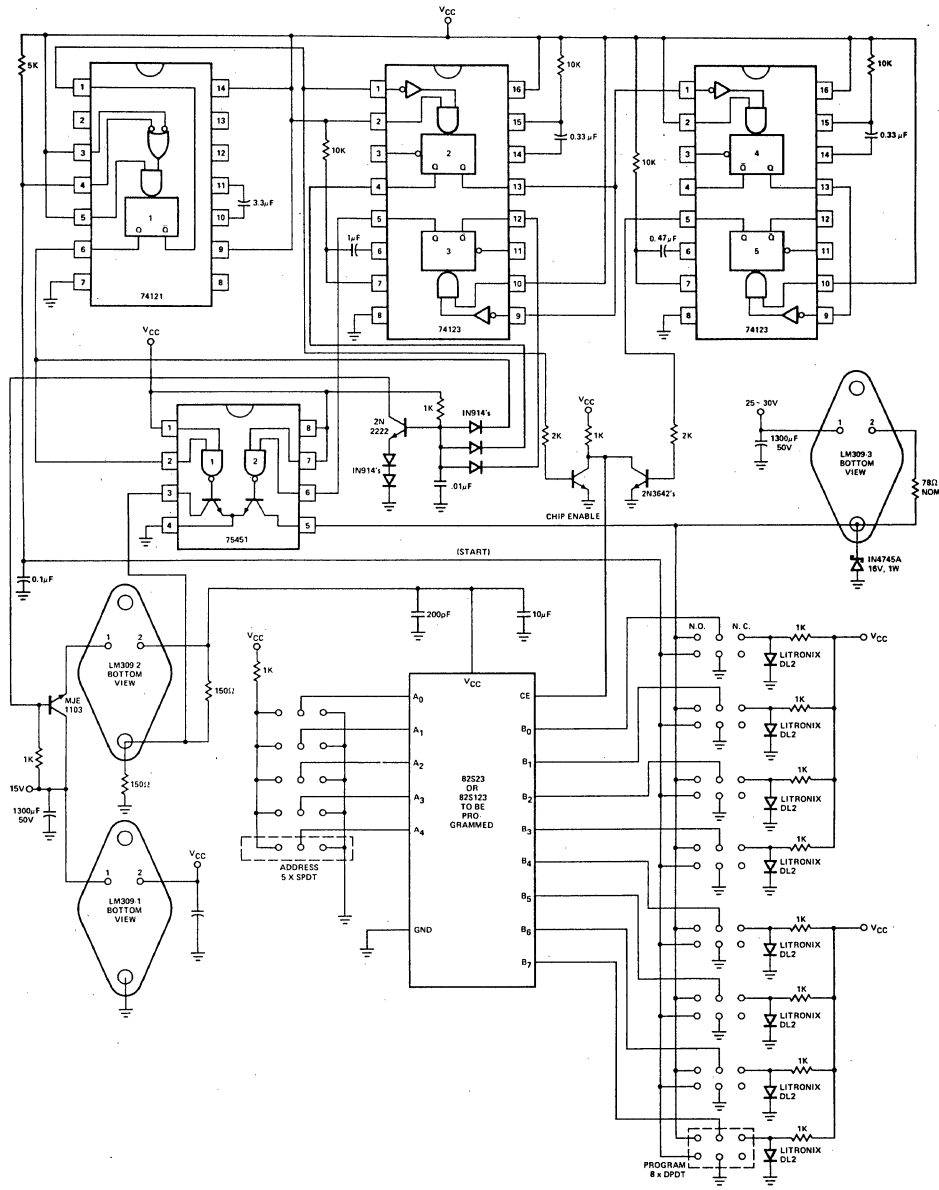
PROGRAMMING PROCEDURE

1. Terminate all device outputs with a $10\text{K}\Omega$ resistor to V_{CC} .
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = +10 \pm 0.5\text{V}$.
3. After $10\mu\text{s}$ delay, apply $I_{OUT} = 65 \pm 3\text{mA}$ to the output to be programmed. Program one output at a time.
4. After $10\mu\text{s}$ delay, pulse the $\overline{\text{CE}}$ input to logic "0" for 1 to 2 ms.
5. After $10\mu\text{s}$ delay, remove I_{OUT} from the programmed output.
6. After $10\mu\text{s}$ delay, return V_{CC} to 0V .
7. To verify programming, after $50\mu\text{s}$ delay, raise V_{CC} to $V_{CCH} = +5.5 \pm .2\text{V}$, and apply a logic "0" level to the $\overline{\text{CE}}$ input. The programmed output should remain in the "1" state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2\text{V}$, and verify that the programmed output remains in the "1" state.
8. Raise V_{CC} to $V_{CCP} = +10 \pm 0.5\text{V}$ and repeat steps 3 through 7 to program other bits at the same address.
9. After $10\mu\text{s}$ delay, repeat steps 2 through 8 to program all other address locations.

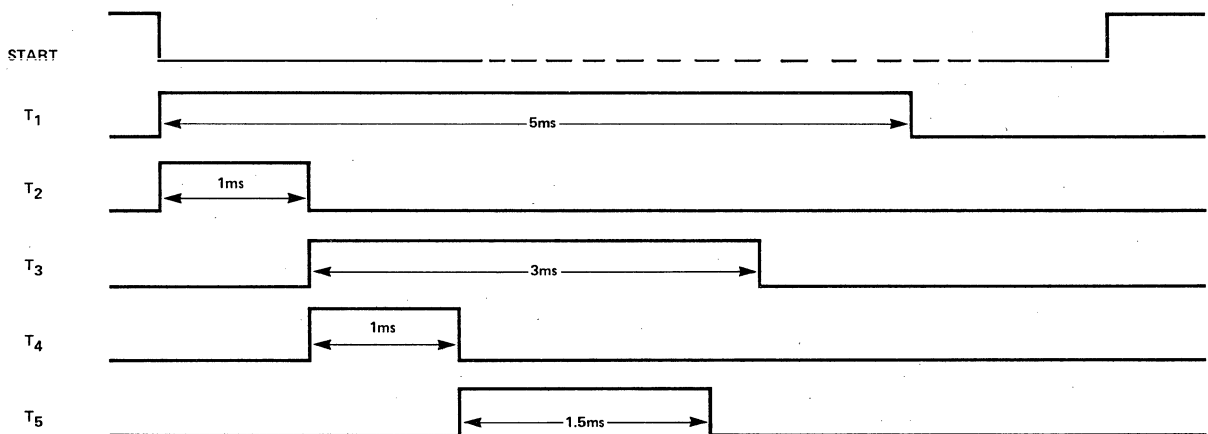
NOTES:

1. Bypass V_{CC} to GND with a $0.01\mu\text{F}$ capacitor to reduce voltage spikes.
2. Care should be taken to insure that $+15.5 \pm 0.5\text{V}$ output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period ($V_{CC} = 0\text{V}$) of 4ms.

MANUAL PROGRAMMER



TIMING SEQUENCE



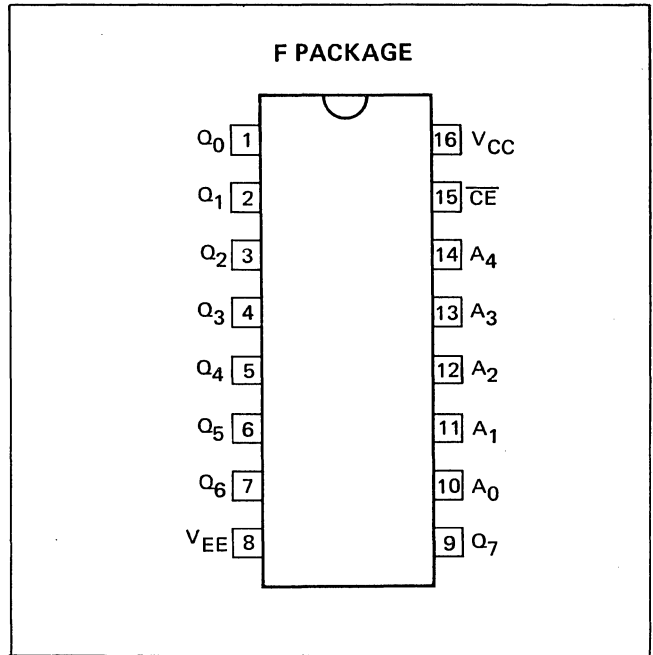
MEMORY Signetics

10139-F

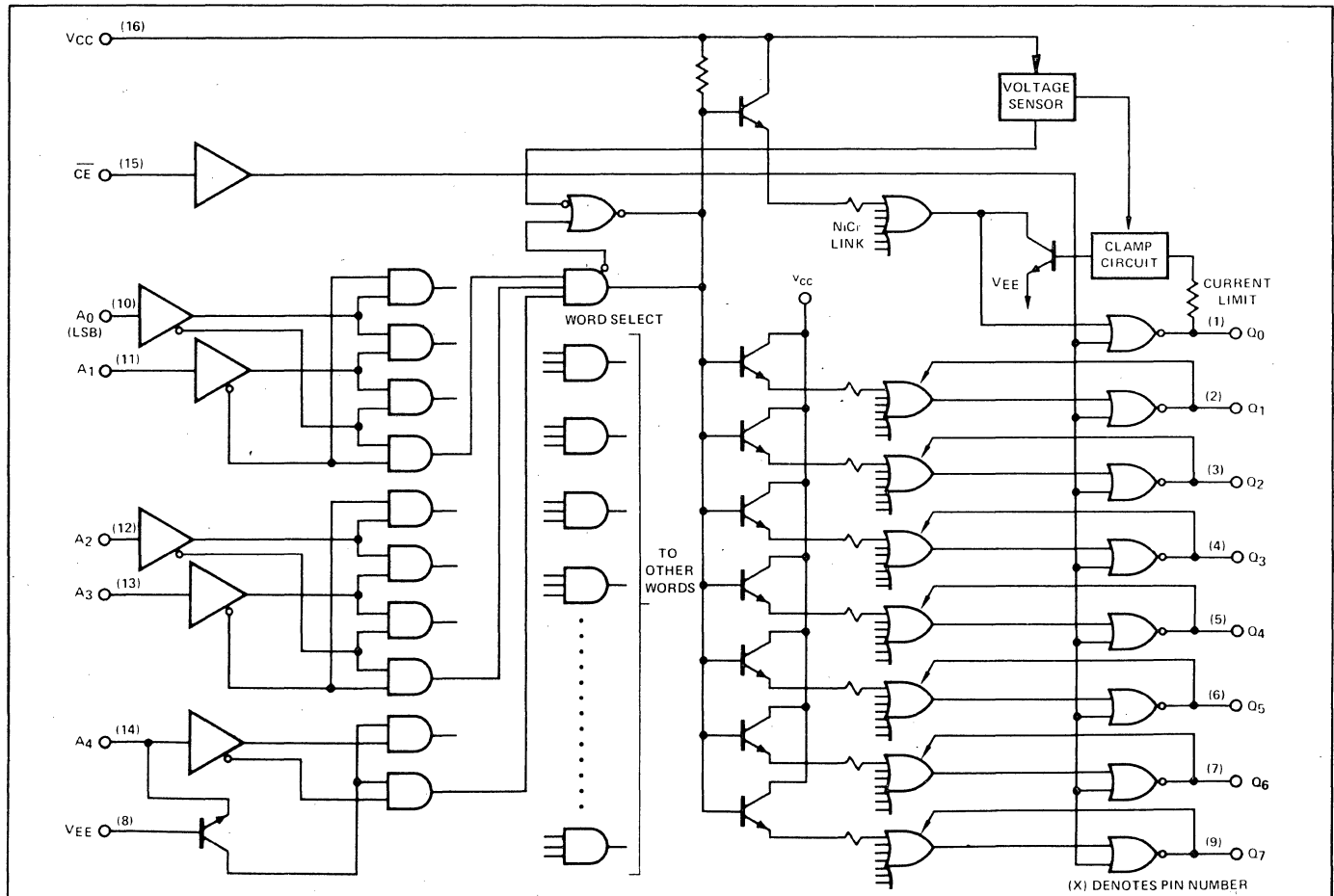
DESCRIPTION

The 10139 is an ECL 256-Bit Read Only Memory organized as 32 words with 8 bits per word. The words are selected by five binary address lines; full word decoding is incorporated on the chip. A chip enable input is provided for additional decoding flexibility, which causes all eight outputs to go to low state when the chip enable input is high. This device is fully compatible with all of Signetics series 10,000 products. Address to output access time is 15 ns typical. Power dissipation is 580 milliwatts typical with separate internal bond wires and metal systems for V_{CC1} and V_{CC2} . The 10139 may be programmed to any desired pattern by the user. The 10139 is suitable for use in high performance ECL systems.

PIN CONFIGURATION



BLOCK DIAGRAM



SWITCHING CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_{CC} = 0\text{V}$, $V_{EE} = -5.2\text{V}$, $R_L = 50\Omega$)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Chip Enable Prop Delay			10	15	ns
Output Rise Time (20 to 80%)			4.2		ns
Output Fall Time (20 to 80%)			4.2		ns
Access Time Address to Output	T_{AD}		15	20	ns

RECOMMENDED PROGRAMMING PROCEDURE

The 10139 is shipped with all bits at logical "0" (low). To write logical "1's", proceed as follows:

MANUAL (see Fig. 1)

STEP 1

Connect V_{EE} (Pin 8) to ground and V_{CC} (Pin 16) to +5.2 volts. Address the word to be programmed by applying 4.0 to 4.6 volts for a logic "1" and 0.0 to 1.0 volts for a logic "0" to the appropriate address inputs.

STEP 2

Raise V_{CC} (Pin 16) to 12 volts.

STEP 3

After V_{CC} has stabilized at 12 volts (including any ringing which may be present on the V_{CC} line) apply a current pulse of 2.5 mA to the output pin corresponding to the bit to be programmed to a logic "1".

STEP 4

Return V_{CC} to 5.2 volts.

CAUTION: To prevent excessive chip temperature rise, V_{CC} should not be allowed to remain at 12 volts for more than 1 second.

STEP 5

Verify that the selected bit has programmed by connecting a 460Ω resistor to ground and measuring the voltage at the output pin. If a logic "1" is not detected at the output, the procedure should be repeated once.

STEP 6

If verification is positive, proceed to the next bit to be programmed.

AUTOMATIC (see Fig. 2)

STEP 1

Connect V_{EE} (Pin 8) to ground and V_{CC} (Pin 16) to +5.2 volts. Apply the proper address data and raise V_{CC} (Pin 16) to 12 volts.

STEP 2

After a minimum delay of 100 μs and a maximum delay of 1.0 ms, apply a 2.5 mA current pulse to the first bit to be programmed ($0.5 \leq PW \leq 1 \text{ ms}$).

STEP 3

Repeat Step 2 for each bit of the selected word specified as a logic "1". (Program only one bit at a time; The delay between output programming pulses should be equal to or less than 1.0 ms.)

STEP 4

After all the desired bits of the selected word have been programmed, change address data and repeat Steps 2 and 3.

NOTE: If all the maximum times listed above are maintained, the entire memory will program in less than 1 second. Therefore, it would be permissible for V_{CC} to remain at 12 volts during the entire programming time.

STEP 5

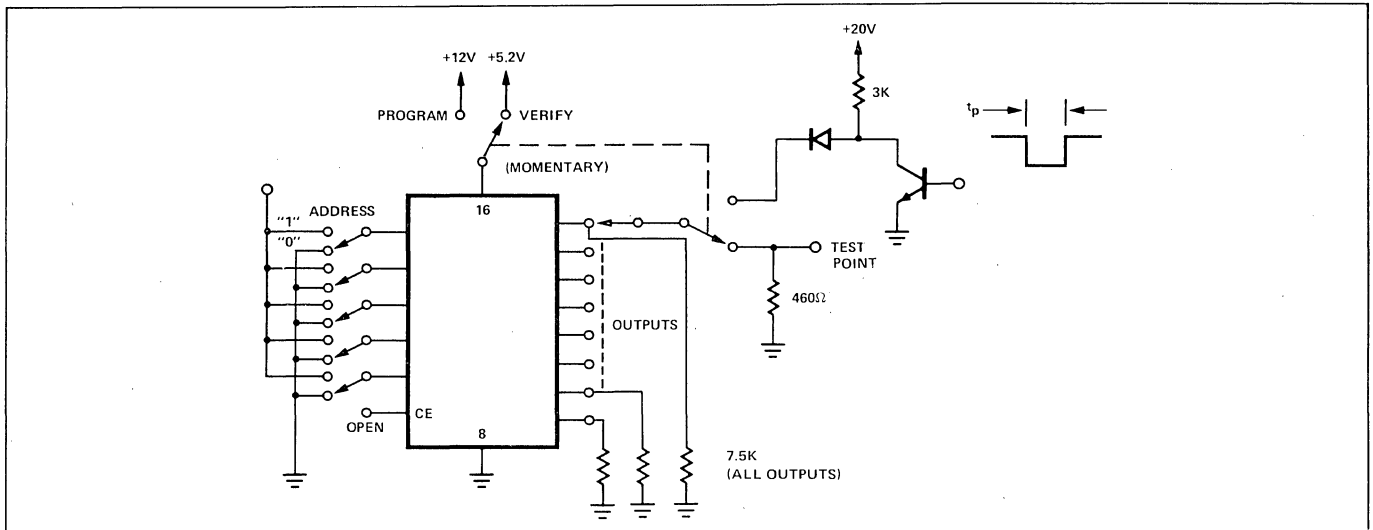
After stepping through all address words, return V_{CC} to +5.2 and verify that each bit has programmed. If one or more bits have not programmed, repeat the entire procedure once.

PROGRAMMING SPECIFICATIONS

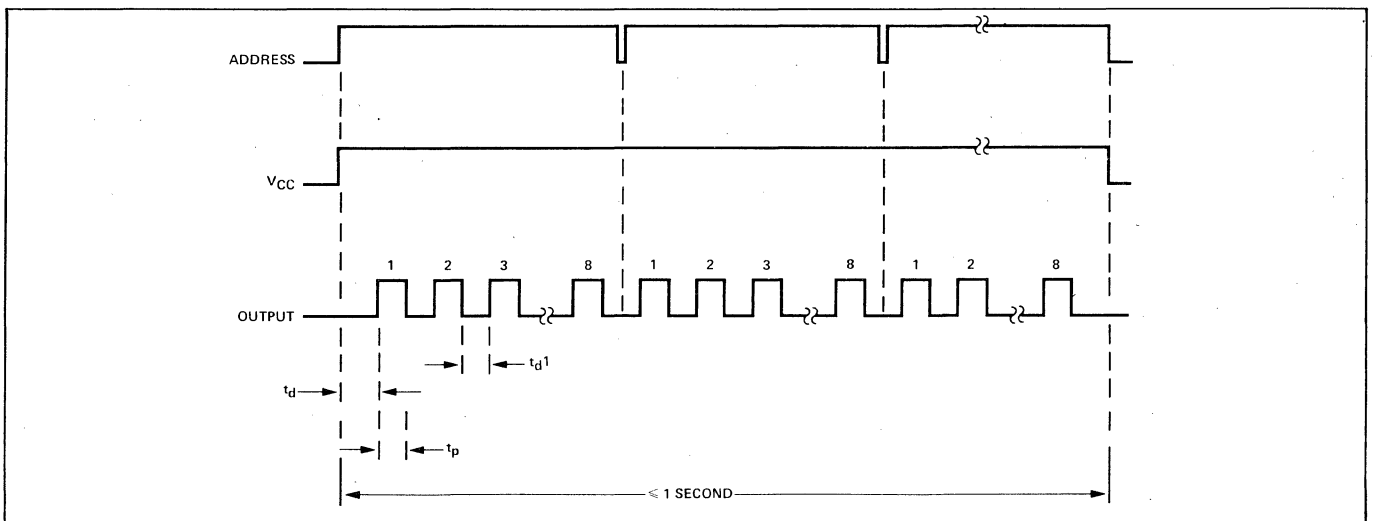
CHARACTERISTIC	SYMBOL	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
Power Supply Voltage To Program To Verify	V_{CCP}	11.5	12.0	12.5	Volts	
	V_{CCV}	5.0	5.2	5.4	Volts	
Programming Supply Current	I_{CCP}			250	mA	$V_{CC} = 12.0$ Volts
Address Voltage logical "1" logical "0"	V_{IH}	4.0		4.6	Volts	
	V_{IL}	0.0		1.0	Volts	
Max. Time at $V_{CC} = V_{CCP}$				1.0	Sec.	
Output Programming Current	I_{OP}	2.0	2.5	3.0	mA	
Output Program Pulse Width	t_p	0.5		1.0	ms	
Output Pulse Rise Time				10	μs	
Programming Pulse Delay (1) following V_{CC} change between output pulses	t_d	0.1		1.0	ms	
	t_{d1}	0.01		1.0	ms	

NOTE: (1) Maximum is specified to minimize the amount of time V_{CC} is at 12 volts.

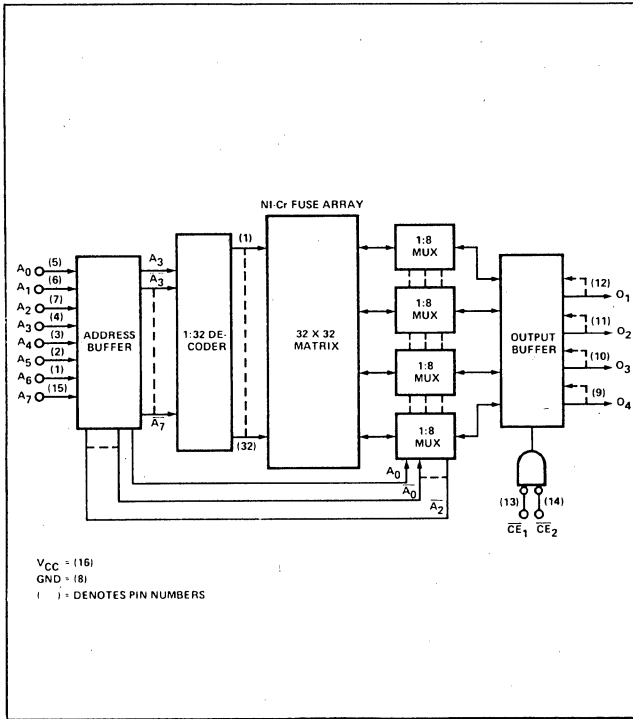
MANUAL PROGRAMMING CIRCUIT



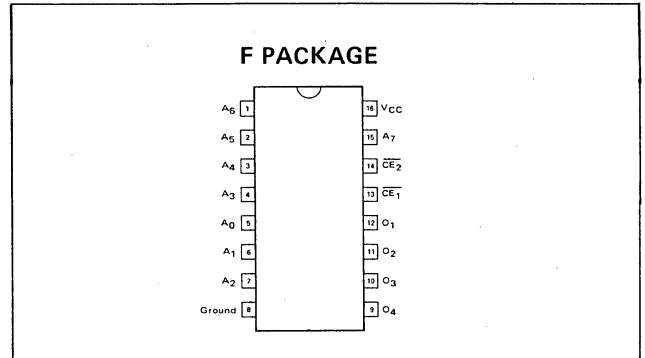
AUTOMATIC PROGRAMMING CIRCUIT



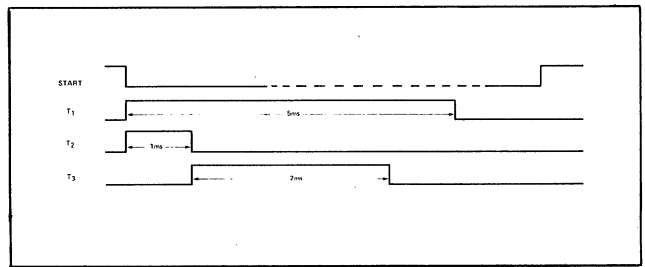
BLOCK DIAGRAM



PIN CONFIGURATION



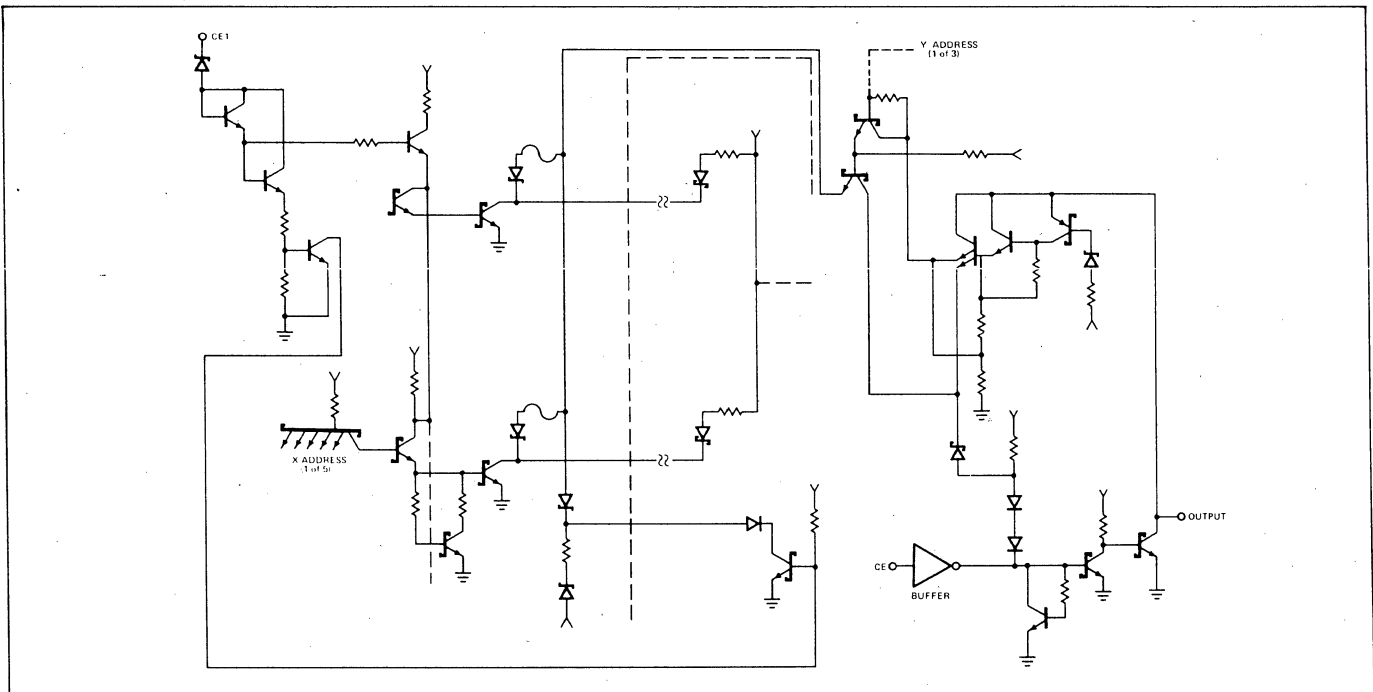
TIMING SEQUENCE



Signetics

MEMORY

TYPICAL FUSING PATH



PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
Power Supply Voltage					
V_{CCP}^1 To Program	$I_{CCP} = 300 \pm 50\text{mA}$ (Transient or steady state)	5.0		5.25	V
V_{CCH} Upper Verify Limit		5.0	5.25	5.5	V
V_{CCL} Lower Verify Limit		4.5	4.75	5.0	V
V_S^3 Verify Threshold		0.9	1.0	1.1	V
I_{CCP} Programming Supply Current	$V_{CCP} = +5.0 \pm 0.25\text{V}$	250	300	350	mA
Input Voltage					
V_{IH} Logical "1" (Except \overline{CE}_1)		3.0		5.0	V
V_{IN} Program Level (\overline{CE}_1 Only)		14.0	14.5	15.0	V
V_{IL} Logical "0"		0	0.4	0.5	V
Input Current					
I_{IH} Logical "1"	$V_{IH} = +3.0\text{V}$			100	μA
I_{IL} Logical "0"	$V_{IL} = +0.5\text{V}$			-1.6	mA
I_{IN} Program Level (\overline{CE}_1 Only)	$V_{IN} = +15.0\text{V}$			15	mA
V_{OUT}^2 Output Programming Voltage	$I_{OUT} = 115 \pm 10\text{mA}$ (Transient or steady state)	16.5	17.0	17.5	V
I_{OUT} Output Programming Current	$V_{OUT} = +17.0 \pm 0.5\text{V}$	105	115	125	mA
T_R^5 Output Pulse Rise Time		0.2		0.5	μs
t_P Programming Pulse Width		1		2	ms
t_D Pulse Sequence Delay		10			μs
T_{PR} Programming Time	$V_{CC} = V_{CCP}$			2.5	sec
T_{PS} Programming Pause	$V_{CC} = 0\text{V}$	5			sec
$\frac{T_{PR}^4}{T_{PR} + T_{PS}}$ Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

The 82S27 is shipped with all bits at logical "0" (low). To write logical "1", proceed as follows:

SET-UP

- Apply GND to pin 12.
- Terminate all device outputs with a $10\text{k}\Omega$ resistor to V_{CC} .
- Set \overline{CE}_2 to logic "0".

PROGRAM-VERIFY SEQUENCE

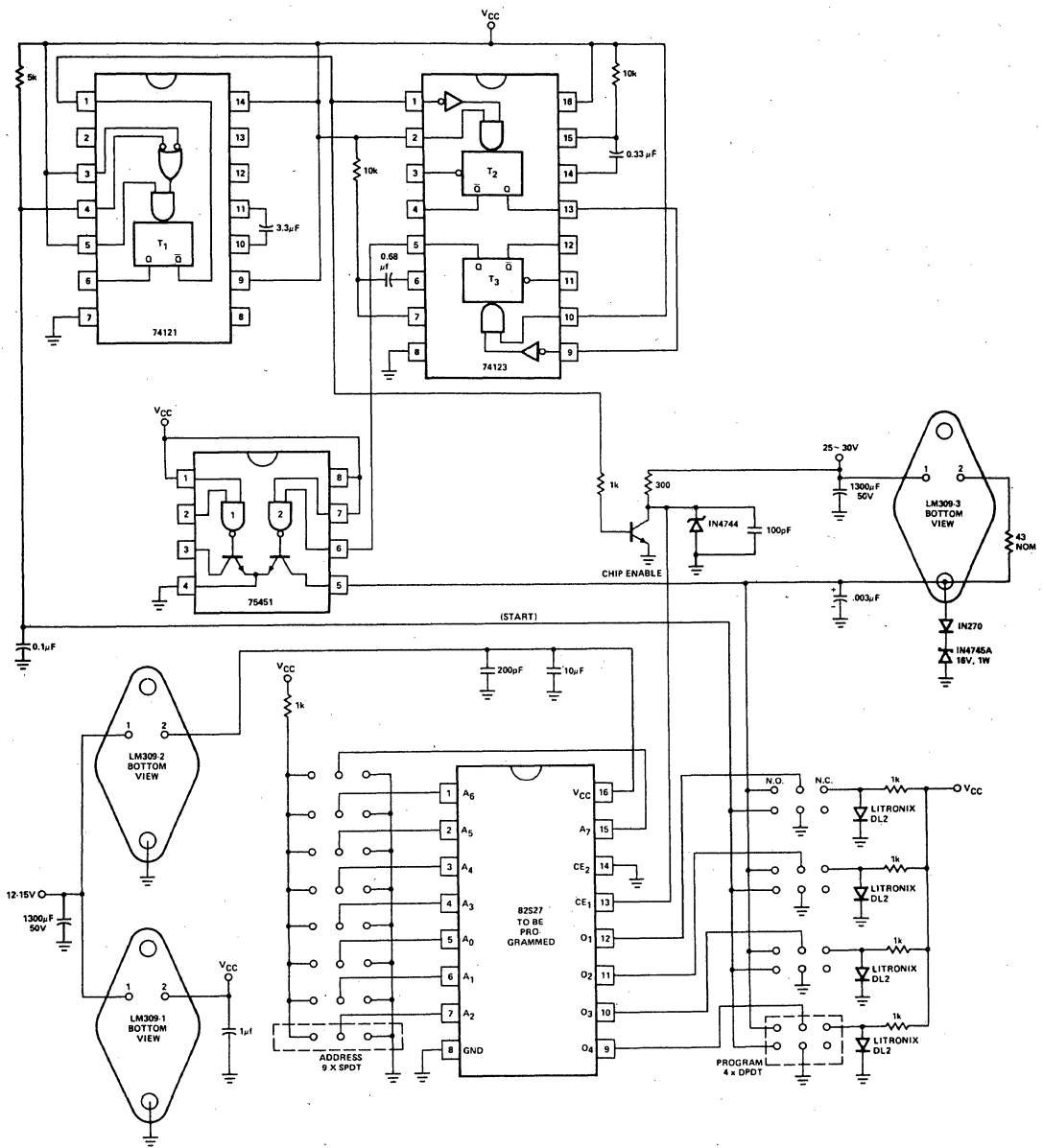
- Step 1 Raise V_{CC} to V_{CCP} , and address the word to be programmed by applying TTL "1" and "0" logic levels to the device address inputs.
- Step 2 After $10\mu\text{s}$ delay, apply to \overline{CE}_1 (pin 13) a voltage source of $14.5 \pm 0.5\text{V}$, with 15mA sourcing current capability.

- Step 3 After $10\mu\text{s}$ delay, apply a voltage source of $+17.0 \pm 0.5\text{V}$ to the output to be programmed. The source must have a current limit of 115mA . Program one output at the time.
- Step 4 After $10\mu\text{s}$ delay, remove $+17.0\text{V}$ supply from programmed output.
- Step 5 To verify programming, after $10\mu\text{s}$ delay, return \overline{CE}_1 to 0V . Raise V_{CC} to $V_{CCH} = +5.25 \pm .25\text{V}$. The programmed output should remain in the "1" state. Again, lower V_{CC} to $V_{CCL} = +4.75 \pm .25\text{V}$, and verify that the programmed output remains in the "1" state.
- Step 6 Raise V_{CC} to V_{CCP} , and repeat steps 2 through 5 to program other bits at the same address.
- Step 7 Repeat steps 1 through 6 to program all other address locations.

NOTES:

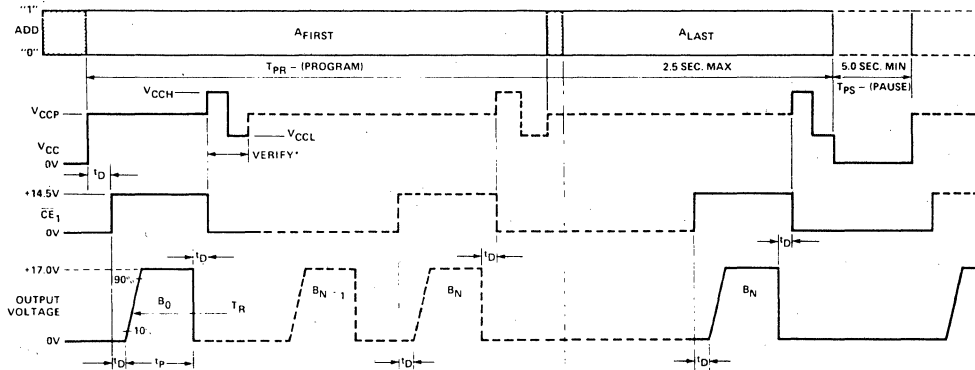
- Bypass V_{CC} to GND with a $0.01\mu\text{F}$ capacitor to reduce voltage spikes.
- Care should be taken to insure the $17 \pm 0.5\text{V}$ output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
- V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
- Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program Verify cycle with a Rest period ($V_{CC} = 0\text{V}$) of 4ms .
- Measured with a 1k dummy load connected across the fusing source.

MANUAL PROGRAMMER



NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

TYPICAL PROGRAMMING SEQUENCE

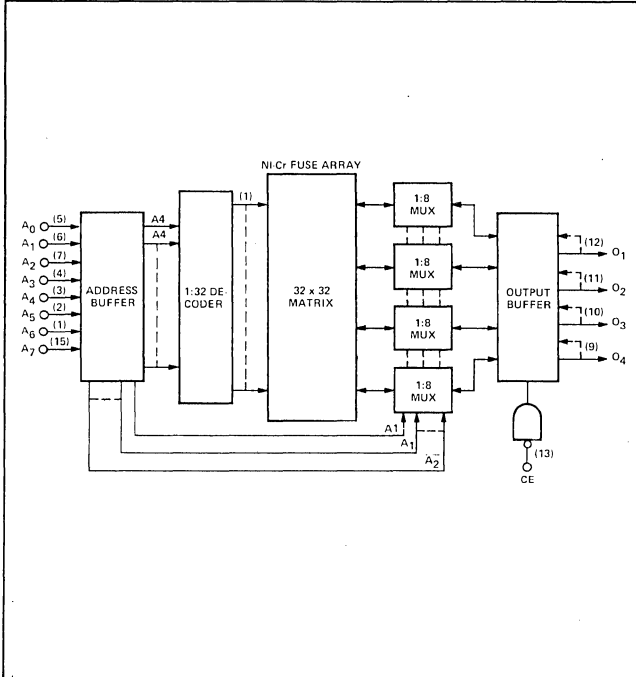


*PROGRAMMING VERIFICATION AT BOTH HIGH AND LOW V_{CC} MARGINS IS OPTIONAL. FOR CONVENIENCE, VERIFICATION CAN ALSO BE EXECUTED AT THE OPERATING V_{CC} LIMITS SPECIFIED IN THE DC CHARACTERISTICS.

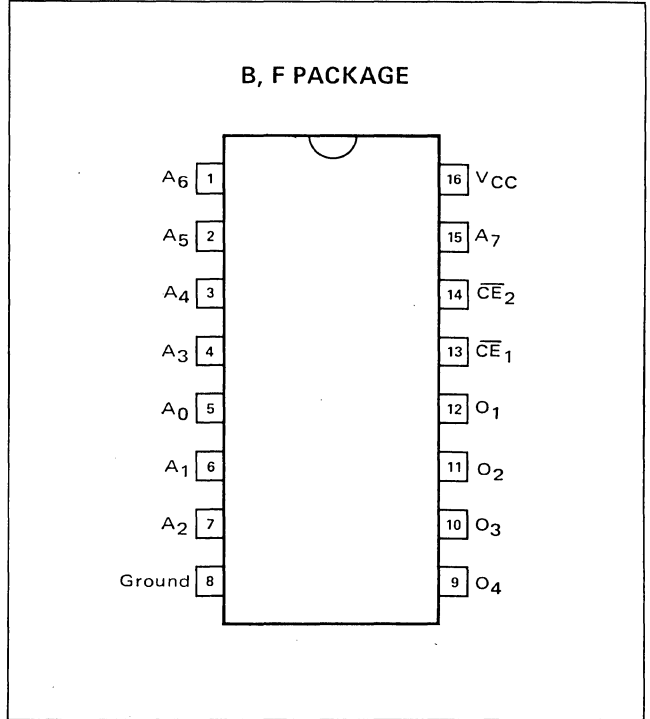
MEMORY Signetics

N82S126/129-B,F • S82S126/129-F

BLOCK DIAGRAM



PIN CONFIGURATION



PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT		
		MIN	TYP	MAX			
Power Supply Voltage							
V_{CCP}^1	To Program	$I_{CCP} = 350 \pm 50\text{mA}$ (Transient or steady state)		8.5	8.75	9.0	V
V_{CCH}	Upper Verify Limit	5.3	5.5	5.7			V
V_{CCL}	Lower Verify Limit	4.3	4.5	4.7			V
V_S^3	Verify Threshold	0.9	1.0	1.1			V
I_{CCP}	Programming Supply Current	$V_{CCP} = +8.75 \pm .25\text{V}$		300	350	400	mA
Input Voltage							
V_{IH}	Logical "1"	2.4		5.5			V
V_{IL}	Logical "0"	0	0.4	0.8			V
Input Current							
I_{IH}	Logical "1"	$V_{IH} = +5.5\text{V}$				50	μA
I_{IL}	Logical "0"	$V_{IL} = +0.4\text{V}$				-500	μA
Output Voltage							
V_{OUT}^2	Output Programming Voltage	$I_{OUT} = 200 \pm 20\text{mA}$ (Transient or steady state)		16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	$V_{OUT} = +17 \pm 1\text{V}$		180	200	220	mA
T_R	Output Pulse Rise Time	10		50			μs
t_p	\overline{CE} Programming Pulse Width	1		2			ms
t_D	Pulse Sequence Delay	10					μs
T_{PR}	Programming Time	$V_{CC} = V_{CCP}$				2.5	sec
T_{PS}	Programming Pause	$V_{CC} = 0\text{V}$		5			sec
$\frac{T_{PR}^4}{T_{PR} + T_{PS}}$	Programming Duty Cycle					33	%

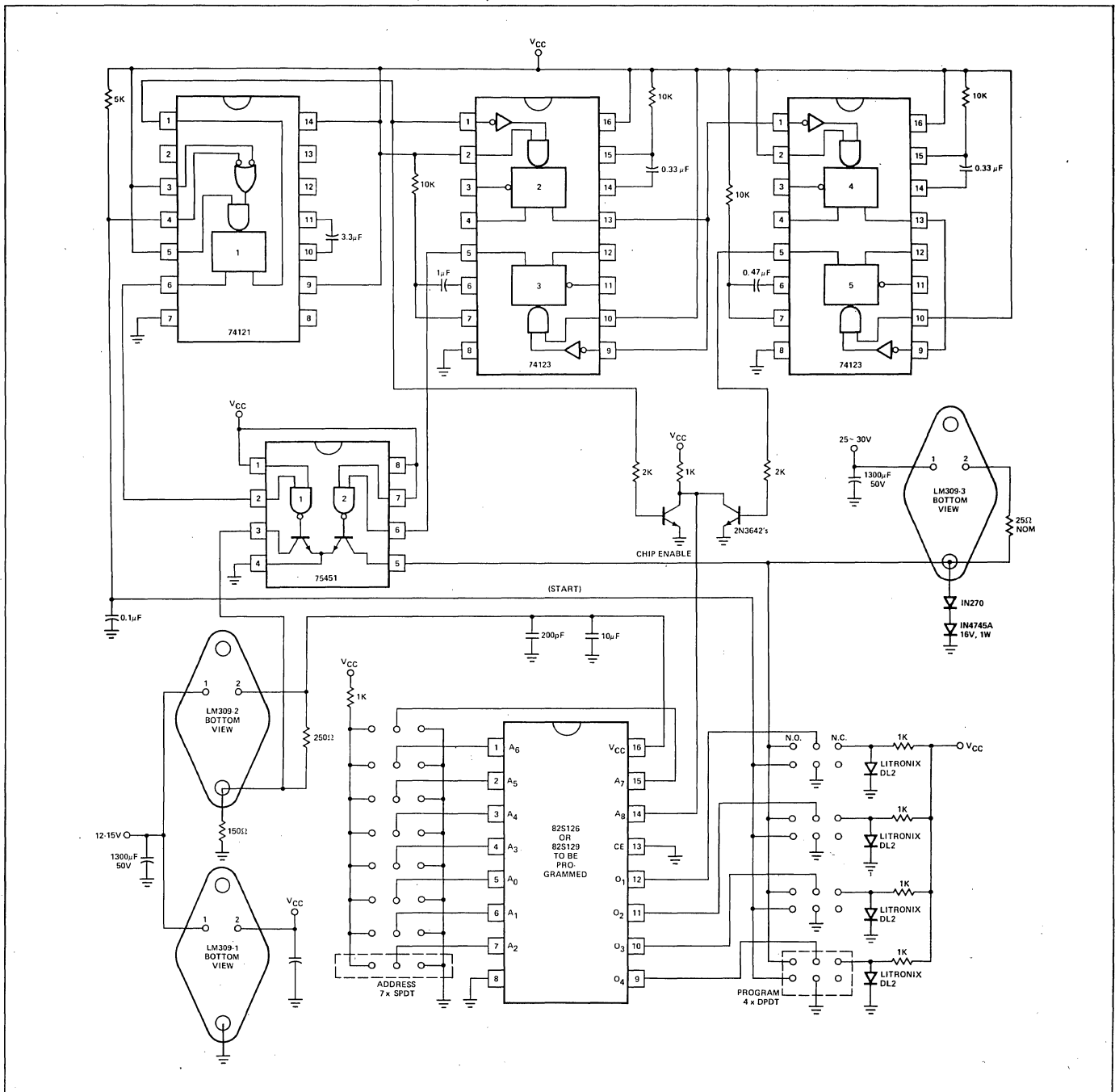
PROGRAMMING PROCEDURE

1. Terminate all device outputs with a $10\text{K}\Omega$ resistor to V_{CC} .
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = 8.75 \pm .25\text{V}$.
3. After $10\mu\text{s}$ delay, apply $V_{OUT} = +17 \pm 1\text{V}$ to the output to be programmed. Program one output at the time.
4. After $10\mu\text{s}$ delay, pulse both \overline{CE} inputs to logic "0" for 1 to 2 ms.
5. After $10\mu\text{s}$ delay, remove +17V from the programmed output.
6. To verify programming, after $10\mu\text{s}$ delay, lower V_{CC} to $V_{CCH} = +5.5 \pm .2\text{V}$, and apply a logic "0" level to both \overline{CE} inputs. The programmed output should remain in the "1" state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2\text{V}$, and verify that the programmed output remains in the "1" state.
7. Raise V_{CC} to $V_{CCP} = 8.75 \pm .25\text{V}$, and repeat steps 3 through 6 to program other bits at the same address.
8. After $10\mu\text{s}$ delay, repeat steps 2 through 7 to program all other address locations.

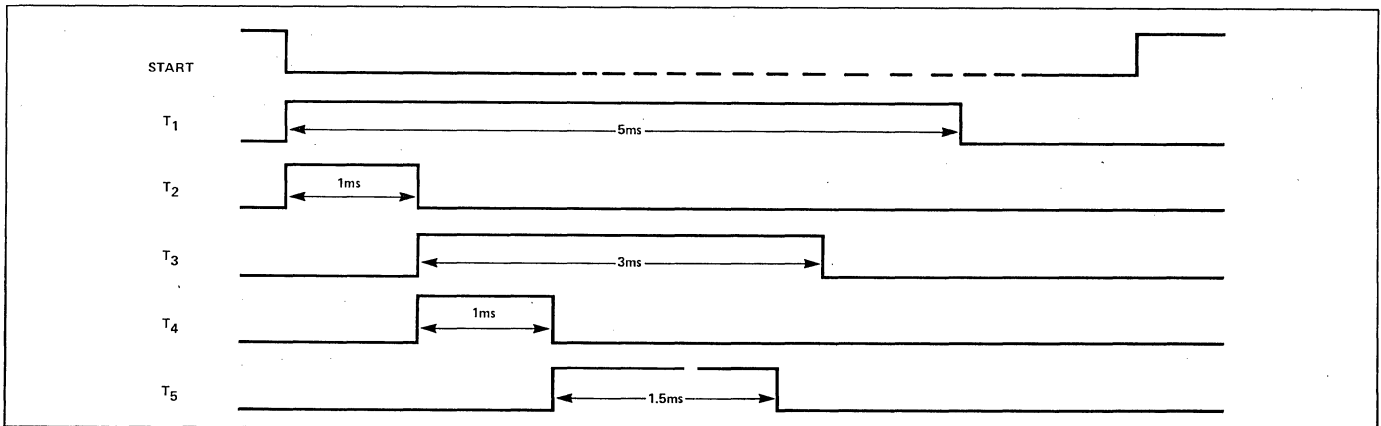
NOTES:

1. Bypass V_{CC} to GND with a $0.01\mu\text{F}$ capacitor to reduce voltage spikes.
2. Care should be taken to insure the $17 \pm 1\text{V}$ output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period ($V_{CC} = 0\text{V}$) of 4ms.

MANUAL PROGRAMMER

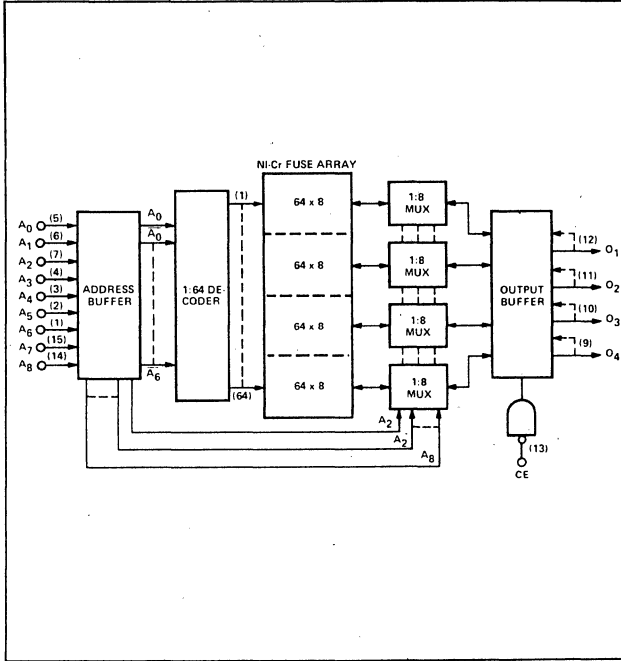


TIMING SEQUENCE

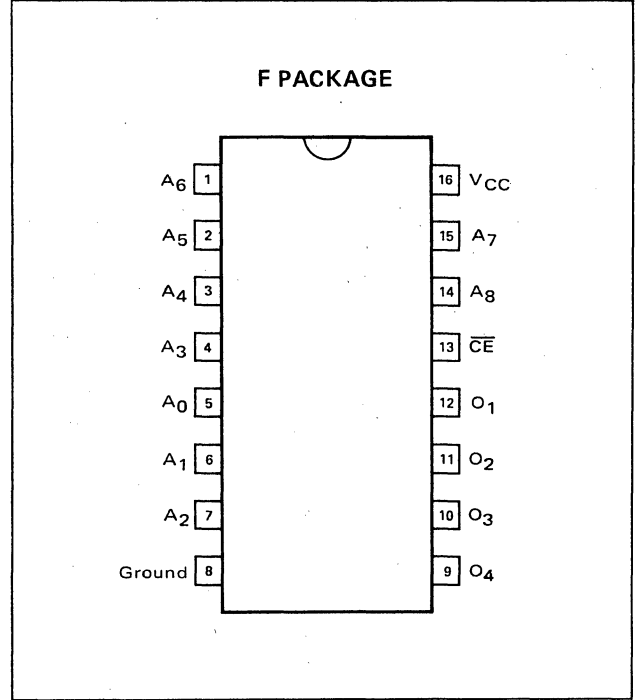


MEMORY Signetics

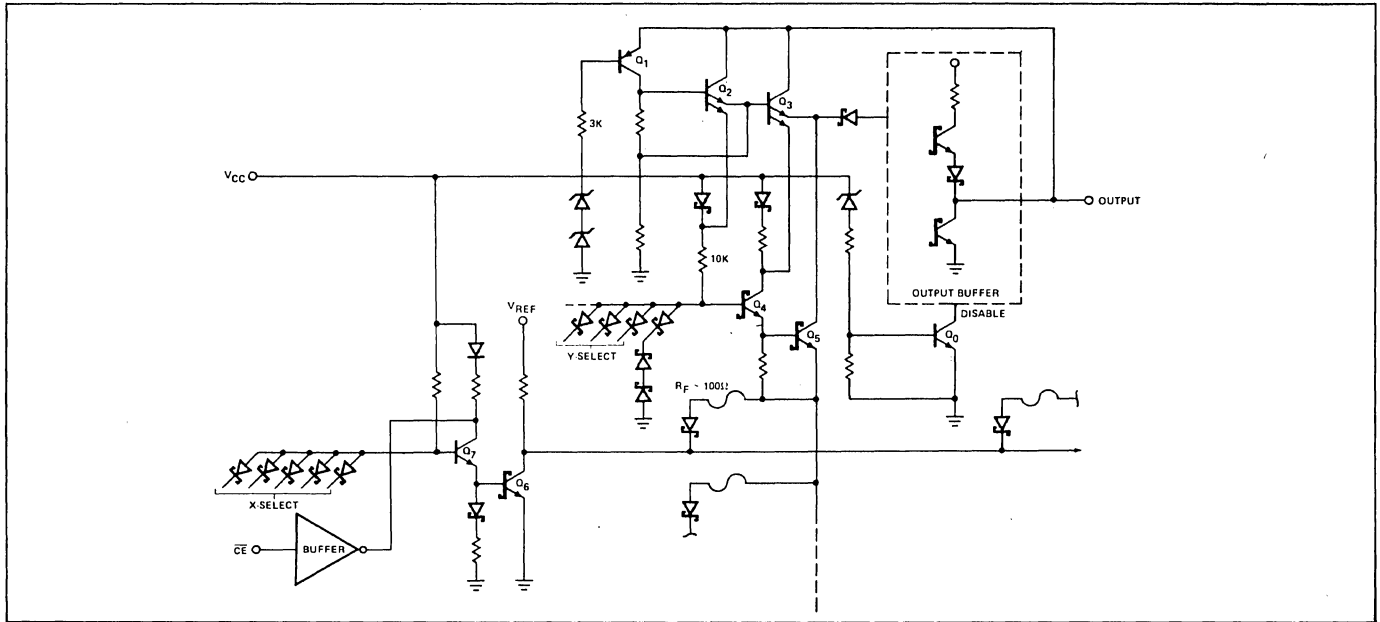
BLOCK DIAGRAM



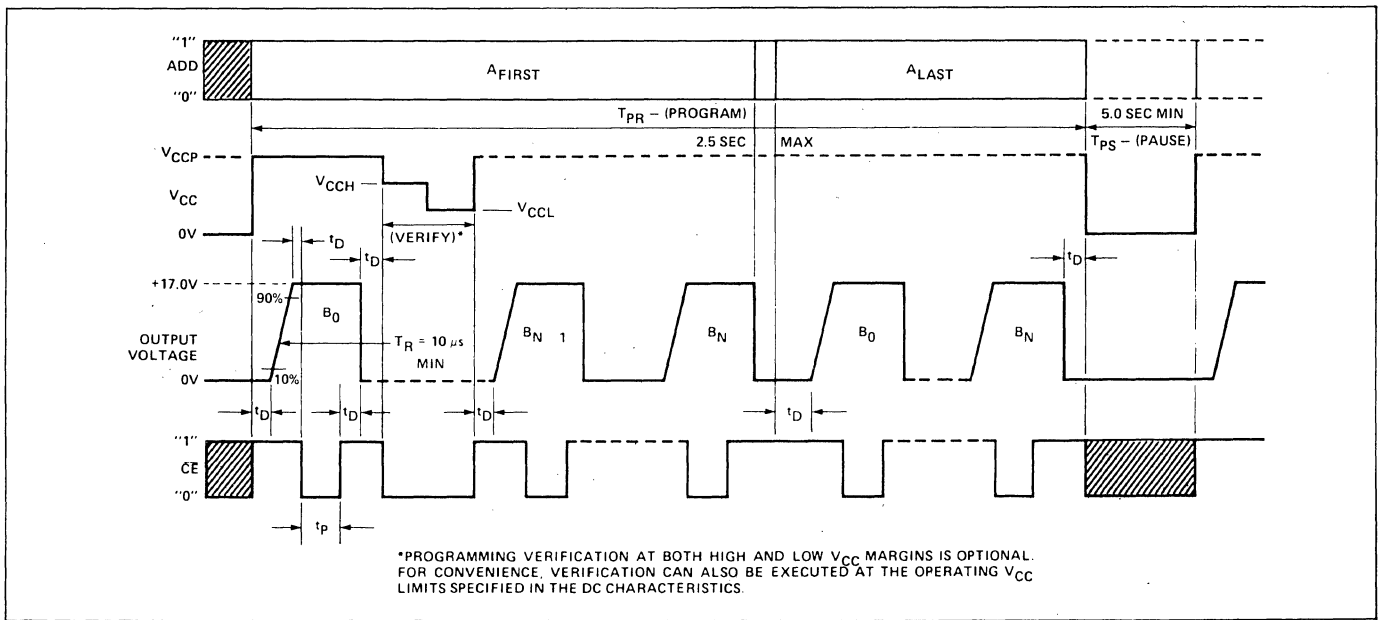
PIN CONFIGURATION



TYPICAL FUSING PATH



TYPICAL PROGRAMMING SEQUENCE



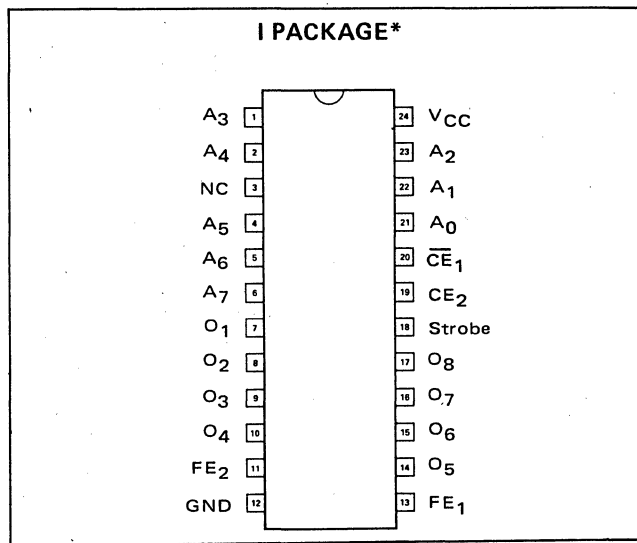
DESCRIPTION

The 82S114 and 82S115 are fully TTL compatible, and include on-chip decoding and two chip enable inputs for ease of memory expansion. They feature Tri-State outputs for optimization of word expansion in bussed organizations. A D-type latch is used to enable the Tri-State output drivers. In the TRANSPARENT READ mode, stored data is addressed by applying a binary code to the address inputs while holding STROBE high. In this mode the bit drivers will be controlled solely by $\overline{CE1}$ and CE2 lines.

In the LATCHED READ mode, outputs are held in their previous state (1, 0, or high Z) as long as STROBE is low, regardless of the state of address or chip enable. A positive STROBE transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the high Z state if the chip is disabled.

A negative STROBE transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the high Z condition if the chip was disabled.

PIN CONFIGURATION



RECOMMENDED PROGRAMMING PROCEDURE

The 82S114/115 are shipped with all bits at logical "0" (low). To write logical "1", proceed as follows:

SET-UP

- Apply GND to pin 12.
- Terminate all device outputs with a 10KΩ resistor to V_{CC}.
- Set $\overline{CE1}$ to logic "0", and CE2 to logic "1" (TTL levels).
- Set Strobe to logic "1" level.

PROGRAM-VERIFY SEQUENCE

- Raise V_{CC} to V_{CCP}, and address the word to be programmed by applying TTL "1" and "0" logic levels to the device address inputs.
- After 10μs delay, apply to FE1 (pin 13) a voltage source of +5.0 ± 0.5V, with 10 mA sourcing current capability.

- After 10μs delay, apply a voltage source of +17.0 ± 1.0V to the output to be programmed. The source must have a current limit of 200 mA. Program one output at the time.
- After 10μs delay, raise FE2 (pin 11) from 0V to +5.0 ± 0.5V for a period of 1ms, and then return to 0V. Pulse source must have a 10 mA sourcing current capability.
- After 10μs delay, remove +17.0V supply from programmed output.
- To verify programming, after 10μs delay, return FE1 to 0V. Raise V_{CC} to V_{CCH} = +5.5 ± .2V. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the "1" state.
- Raise V_{CC} to V_{CCP}, and repeat steps 2 through 6 to program other bits at the same address.
- Repeat steps 1 through 7 to program all other address locations.

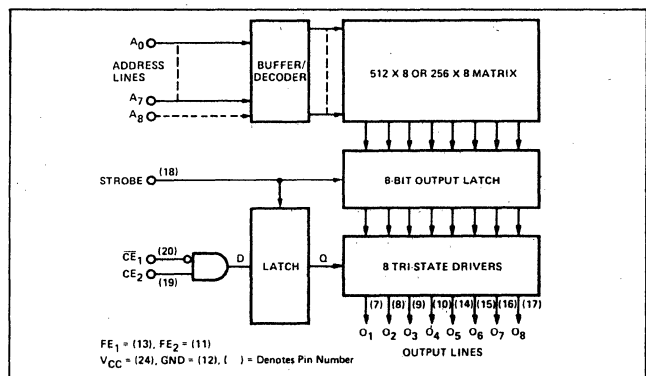
PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
Power Supply Voltage					
V_{CCP}^1	To Program	$I_{CCP} = 200 \pm 25 \text{ mA}$ (Transient or steady state)			V
V_{CCH}	Upper Verify Limit	5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit	4.3	4.5	4.7	V
V_S^3	Verify Threshold	0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +5.0 \pm .25\text{V}$			mA
Input Voltage					
V_{IL}	Low Level Input Voltage	0	0.4	0.8	V
V_{IH}	High Level Input Voltage	2.4		5.5	V
Input Current (FE₁ & FE₂ Only)					
I_{IL}	Low Level Input Current	$V_{IL} = +0.45\text{V}$			μA
I_{IH}	High Level Input Current	$V_{IH} = +5.5\text{V}$			mA
Input Current (Except FE₁ & FE₂)					
I_{IL}	Low Level Input Current	$V_{IL} = +0.45\text{V}$			μA
I_{IH}	High Level Input Current	$V_{IH} = +5.5\text{V}$			μA
V_{OUT}^2	Output Programming Voltage	$I_{OUT} = 200 \pm 20 \text{ mA}$ (Transient or steady state)			V
I_{OUT}	Output Programming Current	$V_{OUT} = +17 \pm 1\text{V}$			mA
T_R	Output Pulse Rise Time	10		50	μs
t_P	FE ₂ Programming Pulse Width	1		1.5	ms
t_D	Pulse Sequence Delay	10			μs
T_{PR}	Programming Time	$V_{CC} = V_{CCP}$			sec
T_{PS}	Programming Pause	$V_{CC} = 0\text{V}$			sec
T_{PR}^4	Programming Duty Cycle				%
$T_{PR}+T_{PS}$					

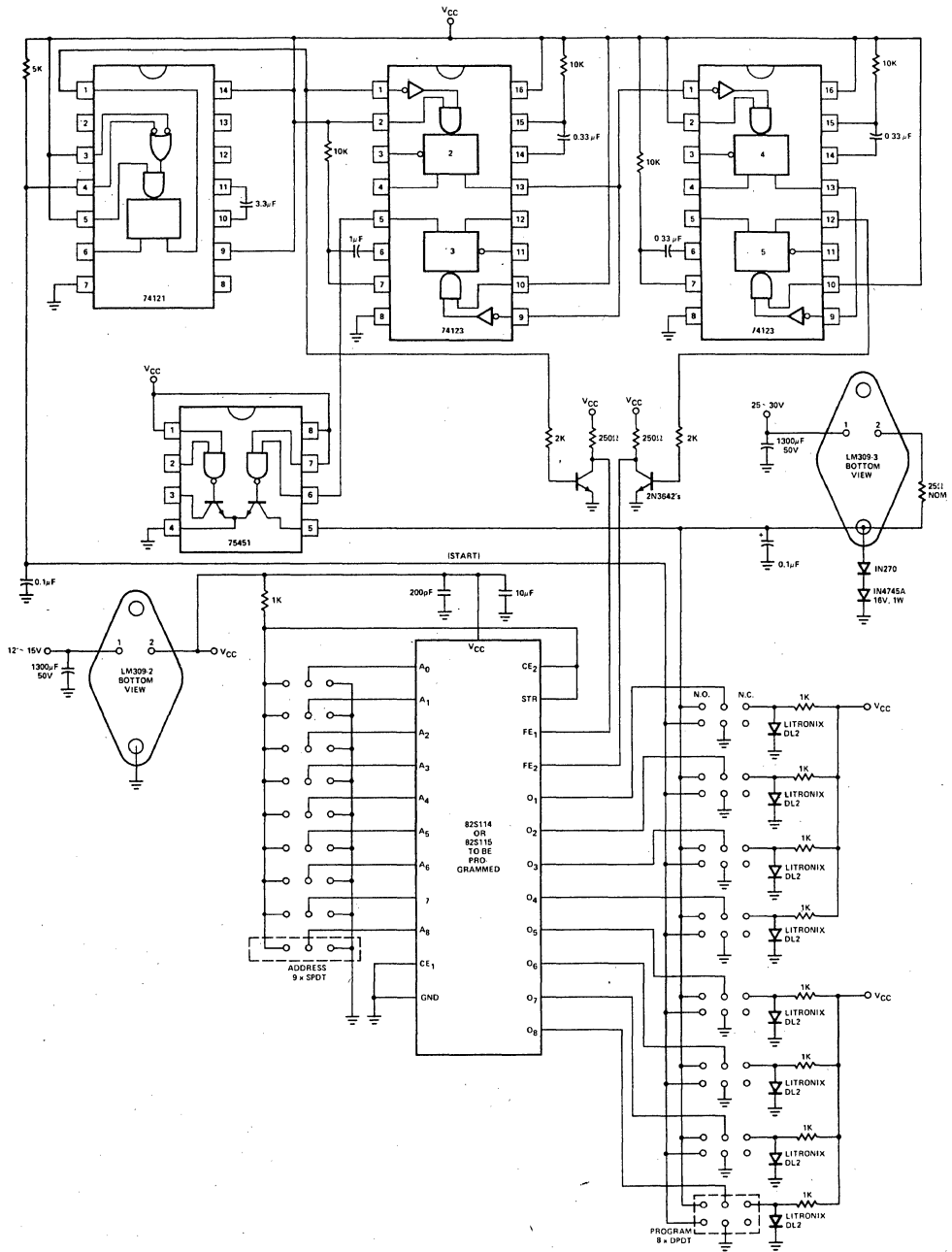
NOTES:

1. Bypass V_{CC} to GND with a 0.01 μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the $17 \pm 1\text{V}$ output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 60% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period ($V_{CC} = 0\text{V}$) of 3 ms.

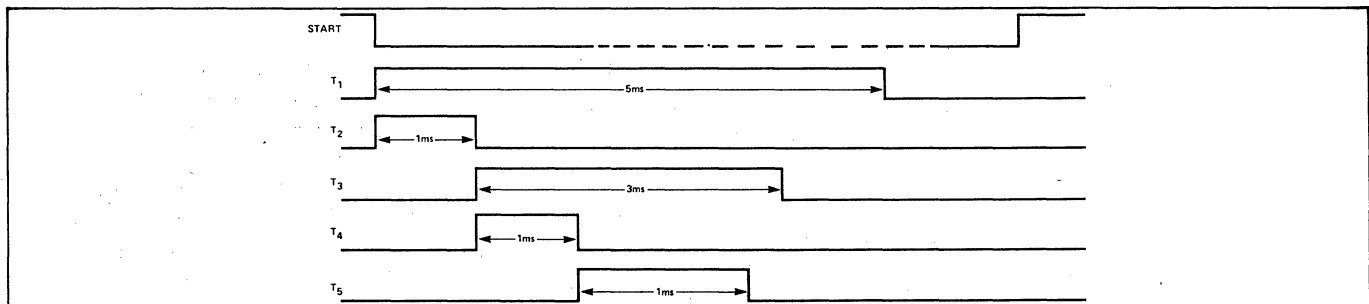
BLOCK DIAGRAM



82S114/115 MANUAL PROGRAMMER



TIMING SEQUENCE



MEMORY

Signetics

DESCRIPTION

The 82S100 (Tri-State Outputs) and the 82S101 (Open Collector Outputs) are Bipolar Programmable Logic Arrays, containing 48 Product terms (AND terms), and 8 output functions. Each output function can be programmed either true active-High (F_p), or true active-Low ($\overline{F_p}$). The true state of the output functions is controlled via an output Sum (OR) Matrix by a logical combination of 16-input variables, or their complements, up to 48 terms.

Both devices are field-programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

The 82S100 and 82S101 are fully TTL compatible, and include a chip-enable clocking input for output deskewing and inhibit. They feature either Open Collector or Tri-State outputs for ease of expansion of product terms and/or input variables.

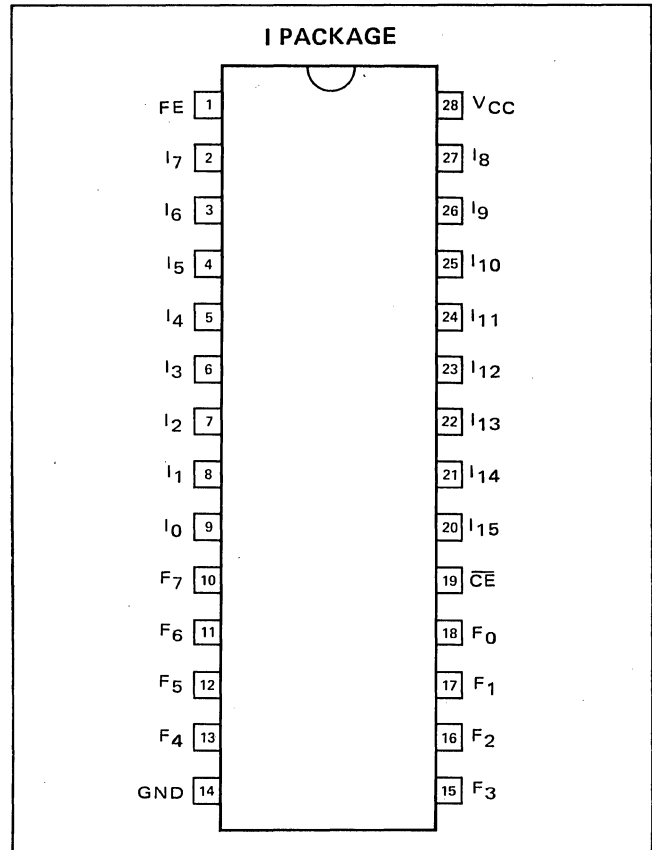
FEATURES

- FIELD PROGRAMMABLE (Ni-Cr LINK)
- INPUT VARIABLES – 16
- OUTPUT FUNCTIONS – 8
- PRODUCT TERMS – 48
- ADDRESS ACCESS TIME – 50ns, MAXIMUM
- POWER DISSIPATION – 600mW, TYPICAL
- INPUT LOADING – (-100µA), MAXIMUM
- OUTPUT OPTION:
TRI-STATE OUTPUTS – 82S100
OPEN COLLECTOR OUTPUTS – 82S101
- OUTPUT DISABLE FUNCTION:
TRI-STATE – Hi-Z
OPEN COLLECTOR – Hi
- CERAMIC DIP

APPLICATIONS

LARGE READ ONLY MEMORY
RANDOM LOGIC
CODE CONVERSION
PERIPHERAL CONTROLLERS
LOOK-UP AND DECISION TABLES
MICROPROGRAMMING
ADDRESS MAPPING
CHARACTER GENERATORS
SEQUENTIAL CONTROLLERS

PIN CONFIGURATION



TRUTH TABLE

LET:

$$P_n = \prod_0^{15} (k_m I_m + j_m \overline{I_m}) \quad ; \quad k = 0, 1, X \text{ (Don't Care)}$$

$$n = 0, 1, 2, \dots, 47$$

where:

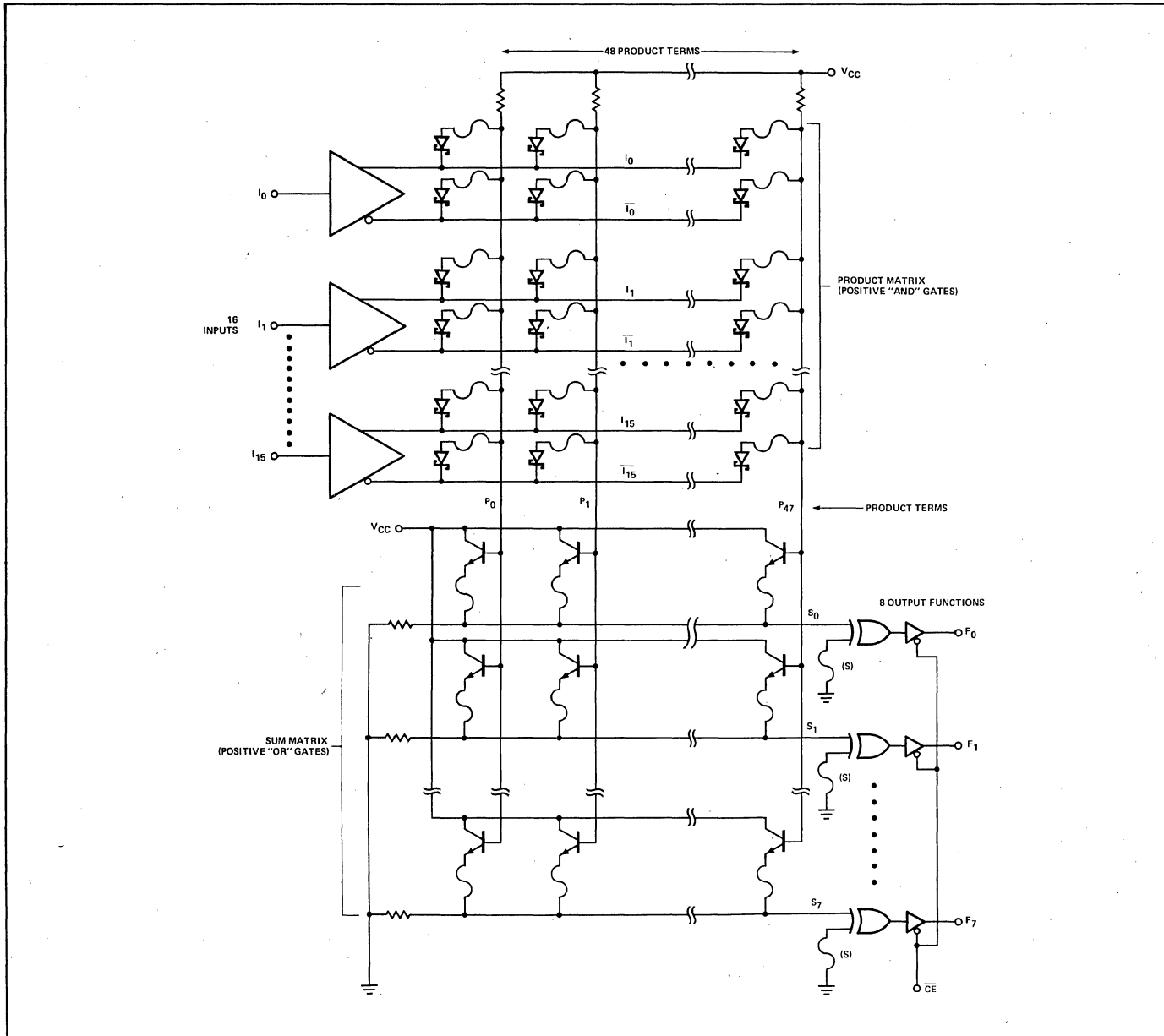
Unprogrammed state : $j_m = k_m = 0$

Programmed state : $j_m = \overline{k_m}$

$$S_r = f(\sum_0^{47} P_n) \quad ; \quad r \equiv p = 0, 1, 2, \dots, 7$$

MODE	P_n	\overline{CE}	F_p	F_p^*	$S_r \stackrel{?}{=} f(P_n)$
Disabled (82S101)	X	1	1	1	X
			Hi-Z	Hi-Z	
Read (82S100)	1	0	1	0	YES
	0	0	0	1	NO
	X	0	0	1	

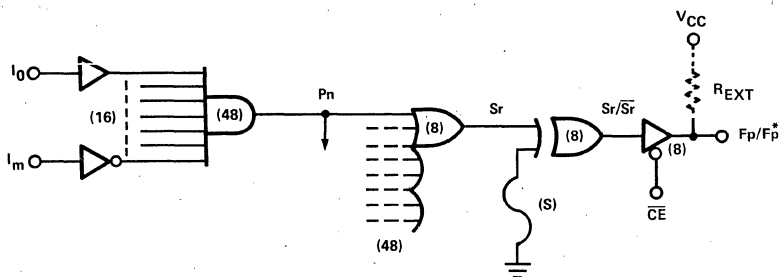
BLOCK DIAGRAM



Signetics

MEMORY

FPLA TYPICAL LOGIC PATH



NOTE:
FOR EACH OF THE 8 OUTPUTS, EITHER THE FUNCTION F_p (ACTIVE HIGH) OR F_p^* (ACTIVE LOW) IS AVAILABLE, BUT NOT BOTH. THE REQUIRED FUNCTION POLARITY IS USER PROGRAMMABLE VIA FUSE (S).

$$P_n = I_0 \bar{I}_1 I_2 \bar{I}_3 \dots \bar{I}_m$$

$$S_r = P_0 + P_1 + P_2 + \dots + P_n$$

$$\bar{S}_r = \bar{P}_0 \cdot \bar{P}_1 \cdot \bar{P}_2 \cdot \dots \cdot \bar{P}_n$$

$$F_p = (\bar{C}E) + (S_r) = (\bar{C}E) + (P_0 + P_1 + P_2 + \dots + P_n) @ S = \text{SHORT}$$

$$F_p^* = (\bar{C}E) + (\bar{S}_r) = (\bar{C}E) + (\bar{P}_0 \cdot \bar{P}_1 \cdot \bar{P}_2 \cdot \dots \cdot \bar{P}_n) @ S = \text{OPEN}$$

ABSOLUTE MAXIMUM RATINGS

PARAMETER ¹	RATING	UNIT
V _{CC} Power Supply Voltage	+7	Vdc
V _{in} Input Voltage	+5.5	Vdc
V _{OH} High Level Output Voltage (82S101)	+5.5	Vdc
V _O Off-State Output Voltage (82S100)	+5.5	Vdc
T _A Operating Temperature Range	0° to +75°	°C
T _{stg} Storage Temperature Range	-65° to +150°	°C

ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ 75°C; 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS	LIMITS			UNIT	NOTES
		MIN	TYP ²	MAX		
V _{IH} High-Level Input Voltage	V _{CC} = 5.25V	2			V	1
V _{IL} Low-Level Input Voltage	V _{CC} = 4.75V			0.8	V	1
V _{IC} Input Clamp Voltage	V _{CC} = 4.75V, I _{IN} = -18mA		-0.8	-1.2	V	1, 7
V _{OH} High-Level Output Voltage (82S100)	V _{CC} = 4.75V, I _{OH} = -2mA	2.4			V	1, 5
V _{OL} Low-Level Output Voltage	V _{CC} = 4.75V, I _{OL} = 9.6mA		0.35	0.45	V	1, 8
I _{OLK} Output Leakage Current (82S101)	V _{CC} = 5.25V V _{OUT} = 5.25V V _{OUT} = 0.45V		1	40	μA	6
I _{O(OFF)} Hi-Z State Output Current (82S100)			1	40	μA	6
			-1	-40	μA	6
I _{IH} High-Level Input Current	V _{IN} = 5.5V		<1	25	μA	
I _{IL} Low-Level Input Current	V _{IN} = 0.45V		-10	-100	μA	
I _{OS} Short-Circuit Output Current (82S100)	V _{CC} = 5.25V, V _{OUT} = 0V	-20		-70	mA	3, 7
I _{CC} V _{CC} Supply Current (82S100, 82S101)	V _{CC} = 5.25V		120	170	mA	4
C _{IN} Input Capacitance	V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5		pF	
C _O Output Capacitance				8		pF

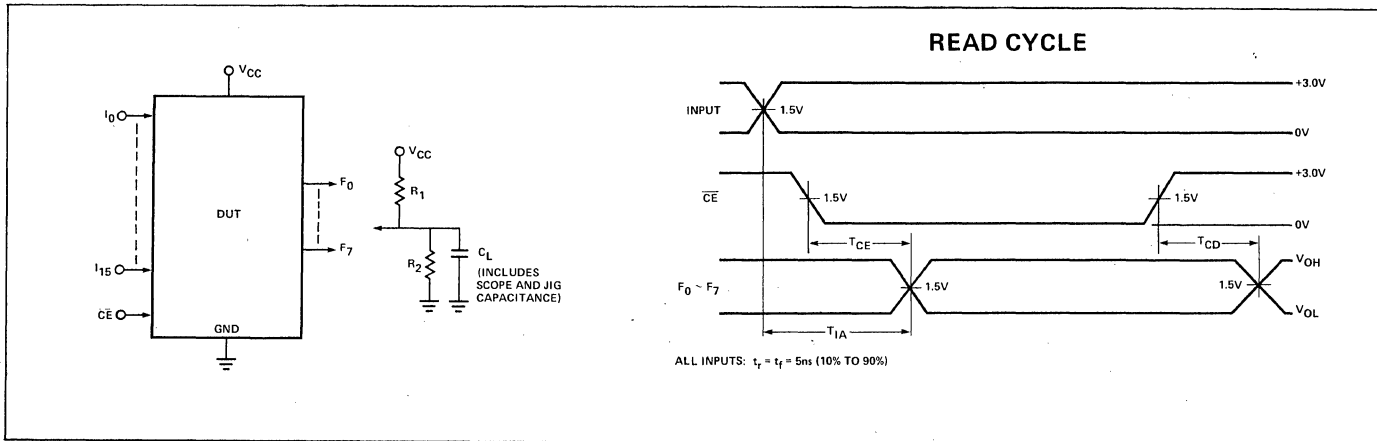
NOTES:

- All voltage values are with respect to network ground terminal.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Duration of short circuit should not exceed one second.
- I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.
- Measured with V_{IL} applied to \overline{CE} and a logic "1" stored.
- Measured with V_{IH} applied to \overline{CE} .
- Test each output one at the time.
- Measured with a programmed logic condition for which the output under test is at a "0" logic level. Output sink current is supplied thru a resistor to V_{CC}.

SWITCHING CHARACTERISTICS $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP ²	MAX	
Propagation Delay					
T_{IA}	Input to Output		35	50	ns
T_{CD}	Chip Disable to Output	$C_L = 30\text{pF}$	15	20	ns
T_{CE}	Chip Enable to Output	$R_1 = 270$ $R_2 = 600$	15	20	ns

AC TEST FIGURE AND WAVEFORM



NOTES:

1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC} = 5.0\text{V}$, and $T_A = +25^{\circ}\text{C}$.

OBJECTIVE PROGRAMMING PROCEDURE

The 82S100/101 are shipped in an unprogrammed state, characterized by:

- A. All internal Ni-Cr links are intact.
- B. Each product term (P-term) contains both true and complement values of every input variable I_m (P-terms always logically "FALSE").
- C. The Sum Matrix contains all 48 P-terms.
- D. The polarity of each output is set to active HIGH (F_p function).
- E. All outputs are at a LOW logic level.

To program each of 8 Boolean logic functions of 16 true or complement variables, including up to 48 P-terms, follow the Program/Verify procedures for the Product Matrix, Sum Matrix, and Output Polarity outlined below.

OUTPUT POLARITY

PROGRAM ACTIVE LOW (F_p^* Function)

Program output polarity before programming Product Matrix and Sum Matrix. Program one output at the time.

1. Set GND (pin 14) to 0V.
2. Do not apply power to the device (V_{CC} , pin 28, open).
3. Apply $V_{OUT} = +18\text{V}$ to the appropriate output for 1ms, and return to 0V.
4. Repeat step 3 to program other outputs.

VERIFY OUTPUT POLARITY

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to +5V.
2. Enable the chip by setting \overline{CE} (pin 19) to LOW logic level.
3. Disable input variables by applying $V_{IN} = +10\text{V}$ to all inputs I_0 through I_{15} .
4. Verify output polarity by sensing the logic state of outputs F_0 through F_7 . All outputs at a HIGH logic level are programmed active HIGH (F_p function), while all outputs at a LOW logic level are programmed active LOW (F_p^* function).
5. Remove $V_{IN} = +10\text{V}$ from inputs I_0 through I_{15} .

PRODUCT MATRIX

PROGRAM INPUT VARIABLE

Program one input at the time and one P-term at the time. All input variable links of unused P-terms are not required to be fused. However, unused input variables must be programmed as Don't Care for all programmed P-terms.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to +5V.
2. Disable the chip by setting \overline{CE} (pin 19) to HIGH logic level.
3. Disable input variables by applying $V_{IN} = +10\text{V}$ to all inputs I_0 through I_{15} .
4. Address the P-term to be programmed (No. 0 through 47) by applying the corresponding binary code to

outputs F_0 through F_5 with F_0 as LSB. Use standard TTL logic levels.

- 5a. If the P-term contains neither I_0 nor $\overline{I_0}$ (input is a Don't Care), fuse both I_0 and $\overline{I_0}$ links by executing both steps 5b and 5c, before continuing with step 7.
- 5b. If the P-term contains I_0 , set to fuse the $\overline{I_0}$ link by lowering the input voltage to I_0 from $V_{IN} = +10V$ to a HIGH logic level. Execute step 6.
- 5c. If the P-term contains $\overline{I_0}$, set to fuse the I_0 link by lowering the input voltage to I_0 from $V_{IN} = +10V$ to a LOW logic level. Execute step 6.
- 6a. After $10\mu s$ delay, raise FE (pin 1) from 0V to +17V. The source must have a current limit of 250mA, and rise time of 10 to $50\mu s$.
- 6b. After $10\mu s$ delay, pulse the \overline{CE} input to +10V for a period of 1ms.
- 6c. After $10\mu s$ delay, return FE input to 0V.
7. Return input I_0 to a disable state by applying $V_{IN} = +10V$.
8. Repeat steps 5 through 7 for all other input variables.
9. Repeat steps 4 through 8 for all other P-terms.
10. Remove $V_{IN} = +10V$ from all input variables.

VERIFY INPUT VARIABLE

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to +5V.
2. Enable F7 output by setting \overline{CE} to +10V.
3. Disable input variables by applying $V_{IN} = +10V$ to inputs I_0 through I_5 .
4. Address the P-term to be verified (No. 0 through 47) by applying the corresponding binary code to outputs F_0 through F_5 .
5. Interrogate input variable I_0 as follows:
 - A. Lower the input voltage to I_0 from $V_{IN} = +10V$ to a HIGH logic level, and sense the state of output F7.
 - B. Lower the input voltage to I_0 from a HIGH to a LOW logic level, and sense the logic state of output F7.

The state of I_0 contained in the P-term is determined in accordance with the following truth table:

I_0	F7	Input Variable State Contained In P-Term
0 1	1 0	$\overline{I_0}$
0 1	0 1	I_0
0 1	1 1	Dont Care
0 1	0 0	$(I_0), (\overline{I_0})$

Note that two tests are required to uniquely determine the state of the input variable contained in the P-term.

6. Return input I_0 to a disable state by applying $V_{IN} = +10V$.
7. Repeat steps 5 and 6 for all other input variables.
8. Repeat steps 4 through 7 for all other P-terms.
9. Remove $V_{IN} = +10V$ from all input variables.

SUM MATRIX PROGRAM PRODUCT TERM

Program one output at the time for one P-term at the time. All P_n links of unused P-terms in the Sum Matrix are not required to be fused.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to +8.5V.
2. Disable the chip by setting \overline{CE} (pin 19) to a HIGH logic level.
3. Address the P-term to be programmed (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5 , with I_0 as LSB. Use standard TTL levels.
- 4a. If the P-term is contained in output function F_0 ($F_0 = 1$ or $F_0^* = 0$), go to step 6.
- 4b. If the P-term is **not** contained in output function F_0 ($F_0 = 0$ or $F_0^* = 1$), set to fuse the P_n link by applying $V_{OUT} = +10V$ to output F_0 .
- 5a. After $10\mu s$ delay, raise FE (pin 1) from 0V to +17V.
- 5b. After $10\mu s$ delay, pulse the \overline{CE} input to +10V for a period of 1ms.
- 5c. After $10\mu s$ delay, return FE input to 0V.
6. Repeat steps 4 and 5 for all other output functions.
7. Repeat steps 3 through 6 for all other P-terms.
8. Remove +8.5V from V_{CC} .

VERIFY PRODUCT TERM

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to +8.5V.
2. Enable the chip by setting \overline{CE} (pin 19) to a LOW logic level.
3. Address the P-term to be verified (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5 , with I_0 as the LSB. Use standard TTL levels.
4. To determine the status of the P_n link in the Sum Matrix for each output function F_p or F_p^* , sense the state of outputs F_0 through F_7 . The status of the link is given by the following truth table:

Output		P-term Link
Active HIGH (F_p)	Active LOW (F_p^*)	
0	1	FUSED
1	0	PRESENT

5. Repeat steps 3 and 4 for all other P-terms.
6. Remove +8.5V from V_{CC} .

INTRODUCTION TO MICROPROCESSORS

This section briefly describes microprocessors from 22 manufacturers. It gives you an overview of all the products currently available, followed by detailed information from the manufacturers on key products.

The facts about each system are presented on the first 11 pages. They include a complete list of the parts in each microprocessor family available from that manufacturer. When the entry states "standard devices", the manufacturer offers non-specialized devices, usually RAM and ROM, that are suitable not only for use with the microprocessor but for general applications as well.

The extent of informations, support, and applications assistance available from manufacturers is an important factor in selecting microprocessors. Therefore, the detailed facts presented on these first 11 pages include descriptions of additional hardware and software items. The descriptions indicate whether complete operating cards are offered. They also indicate if "prototyping systems" or developmental operating systems are available. The listings also cover the availability of "in-system emulators". These units are usually black boxes that look to the system like a real time IC device. But using them the designer can modify the program and can effectively gain access to what would be interior portions of the integrated circuit to test, analyze, and debug the microprocessor while it is connected to the system.

With the rapid evaluation of microprocessors, new products are being introduced frequently. All these new products will be covered in the March, June, and September issues of the magazine IC UPDATE.

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MICROPROCESSORS

Manufacturer Model For Detailed Data See:	AMD 2901	AMD 9080A	AMI S6800 Page 862	AMI 9209 Page 917
General Structure	4-Bit Slice	8-Bit CPU	8-Bit CPU	4-Bit Microcontroller
Type	TTL	NMOS	NMOS	PMOS
No. of Devices per CPU		1	1	1
CPU Size (Pins)	40	40	40	40
Supply Voltage	5	±5, 12	5	-15
CPU Power Dissipation (mw)	925	780	600	160
Part Family (from this mfr.)				
CPU	2901	9080A	S6800	9209
Clock Driver		Standard Devices		On-chip oscillator
I/O Interface	2905/6/7 Bus Transceivers		S8620 Peripheral Interface Adaptor	
RAM	2950/51 (256x1) 2952 (1024x1)	Standard Devices	S6810 (128x8)	256-bits on-chip (64x4)
ROM	2960/61 (1024x8)	Standard Devices	S6830 (1024x8)	756x8 on-chip
PROM	2970/71 (256x4)	Standard Devices	S6834 (512x8)	
UART/USRT		Standard Devices	S6850 Async. Comm. Interface Adaptor	
Other System Parts	2909 Microprogram Sequencer		S6860 Modem	
Architecture				
Data Word Size (bits)	Multiple of 4	8	8	4
Instruction Word Size (bits)	9	8, 16, 24	8, 16, 24	8
Directly Addressable Instruction Words (No.)		65K	65K	756 (Internal)
Clock Frequency (Hz/ext. phases required)	to 10 MHz/1φ	to 3 MHz/1φ	1 MHz/2φ	500 kHz/0φ
Register to Register Add Time (μsec/data word)	0.125	2 (2 MHz clock)	2	15
No. of Registers Arithmetic	0	1	2	2
Index	0	0	1 (16 bit)	0
General Purpose	17	6	0	0
Return Stack Size (No. x bits)	4x4 (2909)	External RAM	External RAM	2x10
Interrupts	Optional	Standard	Standard	None
Type		Vectored 8 level	Vectored, Multilevel	
Direct Memory Access	Optional	Standard	Optional	None
BCD Arithmetic (Hardware)	No	Yes	Yes	Yes
Microprogrammable	Yes	No	No	Yes
Extended Temp. Range Available	-55°C to 125°C	-55°C to 125°C	No	No
Hardware Support				
Processor Cards (CPU system on a card)	No	No	Yes	No
Prototyping System (Hardware and software development system)	No	No	Yes	No
In-System Emulator (Tests system in place)	No	No	Yes	No
Software Support (from this manufacturer)				
Resident Assembler	No	No	Yes	No
Cross Assembler	No	No	Fortran IV	Yes
Simulator	No	No	Fortran IV	Yes
High Level Language	No	No	No	No
Programs Debug	No	No	Yes	
Diagnostic	No	No	Yes	
Edit	No	No	Yes	
User Library (> 25 programs from user)	No	No	No	No
Delivery Start (Qtr.-Year)	3 Qtr. 75	3 Qtr. 75	1 Qtr. 75	3 Qtr. 75
Alternate Sources	Raytheon 2901	Intel, TI 8080	Motorola MC6800	None
Comments		Priority interrupts with Intel 8214.	DMA through HALT and three state control.	

Tinted column indicates additional data is provided on the page noted.

MICROPROCESSORS (Cont'd)

Manufacturer Model For Detailed Data See:	Electronic Arrays EA9002	EMM/SEMI CP-1600/A	Fairchild F8 Page 923	Fairchild F4705
General Structure	8-Bit CPU	16-Bit CPU	8-Bit CPU	4-Bit Slice
Type	NMOS	NMOS	NMOS	CMOS
No. of Devices per CPU	1	1	1	Expandable
CPU Size (Pins)	28	40	40	24
Supply Voltage	5	-3, 5, 12	5, 12	3 to 15
CPU Power Dissipation (mw)	600	750	600	< 1.0
Part Family (from this mfr.)				
CPU	EA9002	CP-1600	3850 Central Processing Unit	F4705
Clock Driver	No		Oscillator on-chip	TTL or CMOS
I/O Interface			In CPU and PSU	Any CMOS 3-State Devices
RAM	64x8 on-chip, Standard Devices	Standard Devices	Standard Devices	F4720 (256x1)
ROM	Standard Devices	Standard Devices	3851 Program Storage Unit, Standard Devices	TTL or MOS
PROM	No	None	Standard Devices	TTL or MOS
UART/USRT	No		3843 USART	
Other System Parts			3852 Dynamic Memory Interface 3853 Static Memory Interface 3854, 3855 DMA	Macrologic CMOS F4704, F4706, F4707, F4710
Architecture				
Data Word Size (bits)	8	16	8	Multiple of 4
Instruction Word Size (bits)	8, 16	10, 20, 30	8, 16, 24	3 to 12
Directly Addressable Instruction Words (No.)	4K	65K	65K	
Clock Frequency (Hz/ext. phases required)	4 MHz/1 ϕ	5 MHz/2 ϕ	2 MHz/0 ϕ	2 MHz
Register to Register Add Time (μ sec/data word)	2	2.4	2	1.0
No. of Registers Arithmetic	1	0	1	8
Index	0	0	2	
General Purpose	8	8	64	8 + 16
Return Stack Size (No. x bits)	7x12	External RAM	33x16 or RAM	(4x16) F4706
Interrupts	Standard	Standard	Standard	None
Type	Vectored, 1 Level	Vectored, Multilevel	Vectored, 1 level/PSU	
Direct Memory Access	Optional	Standard	Optional (3854, 3855)	No
BCD Arithmetic (Hardware)	Yes	No	Yes	No
Microprogrammable	No	No	No	Yes
Extended Temp. Range Available			-55°C to 125°C	-55°C to 125°C
Hardware Support				
Processor Cards (CPU system on a card)	Yes	Yes	Yes	No
Prototyping System (Hardware and software development system)	No	Yes	Yes	No
In-System Emulator (Tests system in place)	No	No	Yes	No
Software Support (from this manufacturer)				
Resident Assembler	Yes	Yes	Yes	No
Cross Assembler	Fortran IV, Timesharing	Fortran IV	Fortran IV	No
Simulator	Yes	Fortran IV	Prototyping Sys, Fortran IV	No
High Level Language	No	No	No	No
Programs Debug	No	Yes	Yes	No
Diagnostic	No	Yes	Yes	No
Edit	No	Yes	Yes	No
User Library (> 25 programs from user)	No	No	Yes	No
Delivery Start (Qtr.-Year)	4 Qtr. 75	1 Qtr. 76	1 Qtr. 75	4 Qtr. 75
Alternate Sources	None	General Instrument CP-1600/A	Mostek F8	None
Comments	DMA through addition of three state level to address bus.	CP-1600 2.4 μ sec add time with 3.3 MHz clock	64 bytes of RAM in CPU, 1024 bytes of ROM in PSU, Programmable Timer.	

Tinted column indicates additional data is provided on the page noted.

MICROPROCESSORS (Cont'd)

Manufacturer Model For Detailed Data See:	Fairchild 9405	General Instrument ALPS	General Instrument CP-1600/A	Harris HM6100 Page 938
General Structure	4-Bit Slice	8-Bit CPU	16-Bit CPU	12-Bit CPU
Type	TTL	PMOS	NMOS	CMOS
No. of Devices per CPU	Expandable	1	1	1
CPU Size (Pins)	24	40	40	40
Supply Voltage	5	-12, 5	-3, 5, 12	5
CPU Power Dissipation (mw)	500	500	750	10
Part Family (from this mfr.)				
CPU	9405	LP8000	CP-1600	HM6100
Clock Driver	Any TTL	LP1030 Clock Drive		Not required
I/O Interface	Any TTL 3-State Devices	LP1000 I/O		HM6101 Parallel Interface Element
RAM	Standard Devices	Standard Devices	Standard Devices	HM6508 (1024x1) HM6518 (1024x1) HM6551 (256x4) HM6561 (256x4)
ROM	Standard Devices	LP6000	Standard Devices	HM6312 (1024x12)
PROM	Standard Devices	None	None	Standard Devices
UART/USRT		Standard Devices	Standard Devices	HM6402/03 UART
Other System Parts	Macrologic TTL 9404/06/07/10	LP1010 Memory Interface		
Architecture				
Data Word Size (bits)	Multiple of 4	8	16	12
Instruction Word Size (bits)	3 to 12	8, 16, 24	10, 20, 30	12
Directly Addressable Instruction Words (No.)		65K	65K	4K (Expandable to 32K)
Clock Frequency (Hz/ext. phases required)	10 MHz	720 kHz/1 ϕ	5 MHz/2 ϕ	4 MHz/0 ϕ
Register to Register Add Time (μ sec/data word)	0.2	5.5	2.4	5
No. of Registers Arithmetic	8	1	0	2
Index		0	0	0
General Purpose	8 + 16	48	8	4
Return Stack Size (No. x bits)	(4x16) 9406	1x8 or RAM	Standard	None
Interrupts	None	Standard	External RAM	Standard
Type		Vectored, 1 level	Vectored, Multilevel	Vectored, 1 level
Direct Memory Access	No	No	Standard	Standard
BCD Arithmetic (Hardware)	No	Yes	No	No
Microprogrammable	Yes	No	No	No
Extended Temp. Range Available	-55°C to 125°C			-55°C to 125°C
Hardware Support				
Processor Cards (CPU system on a card)	No	Yes	Yes	Yes
Prototyping System (Hardware and software development system)	No	Yes	Yes	Yes
In-System Emulator (Tests system in place)	No	No	No	No
Software Support (from this manufacturer)				
Resident Assembler	No	Yes	Yes	Yes
Cross Assembler	No	Fortran IV	Fortran IV	Fortran IV
Simulator	No	Fortran IV	Fortran IV	No
High Level Language	No	No	No	Focal, Basic, Fortran
Programs Debug	No	Yes	Yes	Yes
Diagnostic	No	Yes	Yes	Yes
Edit	No	Yes	Yes	Yes
User Library (> 25 programs from user)	No	No	No	
Delivery Start (Qtr.-Year)	2 Qtr. 75	2 Qtr. 75	3 Qtr. 74	1 Qtr. 76
Alternate Sources	None	None	EMM/SEMI CP-1600/A	Intersil IM6100
Comments			CP-1600 2.4 μ sec add time with 3.3 MHz clock	Processor executes programs written for the PDP8E (DEC minicomputer)

Tinted column indicates additional data is provided on the page noted.

MICROPROCESSORS (Cont'd)

Manufacturer Model For Detailed Data See:	Harris HM6100A Page 938	Intel 3002	Intel 4004	Intel 4040
General Structure	12-Bit CPU	2-Bit Slice	4-Bit CPU	4-Bit CPU
Type	CMOS	TTL	PMOS	PMOS
No. of Devices per CPU	1	≥ 2	1	1
CPU Size (Pins)	40	28 and 40	16	24
Supply Voltage	4-11	5	15 (or -10, 5)	15 (or -10, 5)
CPU Power Dissipation (mw)	40	800	450	1000
Part Family (from this mfr.) CPU	HM6100A	3001 Miprogram Control Unit 3002 Control Processing Element	4004	4040
Clock Driver	Not required		4201 Clock Generator	4201 Clock Generator
I/O Interface	HM6101A Parallel Interface Element		4207/9/11 General Purpose I/O	4207/9/11 General Purpose I/O
RAM	HM6508A (1024x1) HM6518A (1024x1) HM6551A (256x4) HM6561A (256x4)	Standard Devices	4002 (320 bit and I/O) 4101 (256x4 and I/O)	4002 (320 bit and I/O) 4101 (256x4 and I/O)
ROM	HM6312A (1024x12)	Standard Devices	4001 (256x8 and I/O) 4308 (1024x8), 4316 (2048x8)	4001 (256x8 and I/O) 4308 (1024x8), 4316 (2048x8)
PROM	Standard Devices	Standard Devices	4702 (256x8)	4702 (256x8)
UART/USRT	HM6402A/03A UART	None	8251 USART	8251 USART
Other System Parts		3003 Look-Ahead Carry Generator 3212 Multimode Latch Buffer 3214 Interrupt Control	4003 Shift Register 4008/9 Standard Memory Interface 4289 Standard Memory Interface	4003 Shift Register 4008/9 Standard Memory Interface 4289 Standard Memory Interface
Architecture				
Data Word Size (bits)	12	Multiple of 2	4	4
Instruction Word Size (bits)	12		8, 16	8, 16
Directly Addressable Instruction Words (No.)	4K (Expandable to 32K)	512 (Microinstructions)	4K	4K
Clock Frequency (Hz/ext. phases required)	8 MHz/0φ	to 6 MHz/1φ	500 to 750 kHz/2φ	740 kHz/2
Register to Register Add Time (μsec/data word)	2.5	0.15 (16 bits)	10.8	10.8
No. of Registers Arithmetic	2	2	1	1
Index	0	0	0	0
General Purpose	4	11	16	24
Return Stack Size (No. x bits)	None	None	3x12	7x12
Interrupts	Standard	Optional	None	Standard
Type	Vectored, 1 level	8 Level Priority (3214)		Vectored, 1 Level
Direct Memory Access	Standard	No	None	None
BCD Arithmetic (Hardware)	No	No	Yes	Yes
Microprogrammable	No	Yes	No	No
Extended Temp. Range Available	-55°C to 125°C	-55°C to 125°C	-55°C to 85°C	-55°C to 85°C
Hardware Support				
Processor Cards (CPU system on a card)	Yes	No	Yes	Yes
Prototyping System (Hardware and software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	No	Yes	No	No
Software Support (from this manufacturer)				
Resident Assembler	Yes	No	Yes	Yes
Cross Assembler	Fortran IV	CROMIS Microassembler	Fortran IV	Fortran IV
Simulator	No	No	Fortran IV	Fortran IV
High Level Language	Focal, Basic, Fortran	No	No	No
Programs Debug	Yes	No	Yes	Yes
Diagnostic	Yes	No	Yes	Yes
Edit	Yes	No	Yes	Yes
User Library (> 25 programs from user)		No	Yes	Yes
Delivery Start (Qtr.-Year)	1 Qtr. 76	3 Qtr. 74	2 Qtr. 71	4 Qtr. 74
Alternate Sources	Intersil IM6100	Signetics N3002	National	None
Comments	Processor executes programs written for the PDP8E (DEC minicomputer)			

Tinted column indicates additional data is provided on the page noted.

MICROPROCESSORS (Cont'd)

Manufacturer Model For Detailed Data See:	Intel 8008	Intel 8080A Page 958	Intersil IM6100	Monolithic Memories 5701-1/6101-1
General Structure	8-Bit CPU	8-Bit CPU	12-Bit CPU	4-Bit Slice
Type	PMOS	NMOS	CMOS	TTL
No. of Devices per CPU	1	1	1	
CPU Size (Pins)	18	40	40	40
Supply Voltage	-9, 5	±5, 12	5 to 10 (5 nominal)	5
CPU Power Dissipation (mw)	420	780	10	900
Part Family (from this mfr.)				
CPU	8008 500 kHz 8008-1 800 kHz	8080A (Commercial) M8080A (Military)	IM6100	5701 (Military) 6701 (Commercial)
Clock Driver	8201 Generator/Driver	8224 Generator/Driver	Not required	Not required
I/O Interface	8212 I/O Port 8216 Bus Driver 8255 Prog. Perif. Inter.	8212 I/O Port 8216/26 Bus Drivers 8255 Prog. Perif. Inter.	IM6101 Parallel Interface Element	6718 I/O Controller
RAM	8101 (256x4 with I/O) 8102A (1024x1), 8107B (4086x1), 8111 (256x4 with I/O)	8101 (256x4 with I/O) 8102A (1024x1), 8107B (4086x1), 8111 (256x4 with I/O)	Standard Devices	Standard Devices
ROM	8308 (1024x8) 8316 (2048x8)	8308 (1024x8) 8316A (2048x8)	IM6312, Standard Devices	Standard Devices
PROM	8604 (512x8), 8702 (256x8)	8604 (512x8), 8702A (256x8)	Standard Devices	Standard Devices
UART/USRT	8251 USART	8251 USART	IM6402 UART	None
Other System Parts	8205 1 of 8 Decoder 8210 Level Shifter/Clock Driver 8214 Priority Interrupt 8253 Interval Timer 8257 DMA Controller	8205 1 of 8 Decoder 8210/22 RAM Driver/Controller 8214 Priority Interrupt 8253 Interval Timer, 8257 DMA Controller 8259 Interrupt Cont. 8704 (512x8), 8708 (1024x8) Erasable PROMs		6710 Microprogram Control Unit 6717 DMA Controller 6716 Interrupt Control Unit 6780 FPLA
Architecture				
Data Word Size (bits)	8	8	12	Multiple of 4
Instruction Word Size (bits)	8, 16, 24	8, 16, 24	12	8
Directly Addressable Instruction Words (No.)	16K	65K	4K (Expandable to 32K)	
Clock Frequency (Hz/ext. phases required)	800 kHz/2φ	2 MHz/1φ (2.6 and 3 MHz opt.)	4 MHz/0φ	0 to 10 MHz/1φ
Register to Register Add Time (μsec/data word)	12.5	2 (2 MHz clock)	5 (2.5 at 10v)	0.085 typ.
No. of Registers Arithmetic	1	1	2	0
Index	0	0	0	0
General Purpose	6	6	4	17
Return Stack Size (No. x bits)	7x14	External RAM	None	6710 MCU
Interrupts	Standard	Standard	Standard	6716
Type	Vectored, 8 Level	Vectored, 8 Level (8214)	Vectored, 1 Level	8 Vectored
Direct Memory Access	Optional (8257)	Standard	Standard	6717
BCD Arithmetic (Hardware)	No	Yes	No	Microprogrammable
Microprogrammable	No	No	No	Yes
Extended Temp. Range Available	-55°C to 85°C	-55°C to 125°C	-55°C to 125°C	-55°C to 125°C
Hardware Support				
Processor Cards (CPU system on a card)	Yes	Yes	Yes	MMI 300 Minicomputer
Prototyping System (Hardware and software development system)	Yes	Yes	Yes	MMI 300 Minicomputer
In-System Emulator (Tests system in place)	No	Yes	No	No
Software Support (from this manufacturer)				
Resident Assembler	Yes	Yes	Yes	
Cross Assembler	Fortran IV	Fortran IV	Yes	
Simulator	Fortran IV	Fortran IV	Forpal III	
High Level Language	PL/M (Fortran IV)	PL/M (Fortran IV)	Yes	
Programs Debug	Yes	Yes	Yes	Yes (MMI 300)
Diagnostic	Yes	Yes	Yes	Yes (MMI 300)
Edit	Yes	Yes	Yes	
User Library (> 25 programs from user)	Yes	Yes	Yes (DEC)	No
Delivery Start (Qtr.-Year)	1 Qtr. 72	4 Qtr. 73	2 Qtr. 75	4 Qtr. 75
Alternate Sources	None	AMD 9080, T18080	Harris 6100	To be announced
Comments	8 level interrupts with 8214 Priority Interrupt IC.		Executive PDP-8, Instruction Set	RAM on-chip

Tinted column indicates additional data is provided on the page noted.

MICROPROCESSORS (Cont'd)

Manufacturer Model For Detailed Data See:	MOS Technology 6501/2/3/4	Mostek F8 Page 964	Mostek MK5065-1	Motorola M6800
General Structure	8-Bit CPU	8-Bit CPU	8-Bit CPU	8-Bit CPU
Type	NMOS	NMOS	PMOS	NMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	40 or 28	40	40	40
Supply Voltage	5	5, 12	-12, ±5	5
CPU Power Dissipation (mw)	200	600	600	600
Part Family (from this mfr.) CPU	6501 (2φ clock) 6502/3 (self clocking)	MK3850 Central Processing Unit	MK5065-1	MC6800
Clock Driver	Not required	Oscillator on-chip	None	MC6870/71 Clock Generators*
I/O Interface	Yes	In CPU and PSU		MC6820 Peripheral Interface Adaptor
RAM	Standard Devices	Standard Devices	Standard Devices	MCM6810A (128x8)
ROM	Standard Devices	MK3851 Program Storage Unit	Standard Devices	MCM6830A (1024x8)
PROM	No	Yes	None	No
UART/USRT	None	None	None	MC6850 Async. Comm. Interface Adaptor
Other System Parts	6530 Memory, I/O, Timer Array	MK3852 Dynamic Memory Interface MK3853 Static Memory Interface MK3854 DMA		MC6860 Modem
Architecture				
Data Word Size (bits)	8	8	8	8
Instruction Word Size (bits)	8, 16, 24	8, 16, 24	8, 16	8, 16, 24
Directly Addressable Instruction Words (No.)	65K	65K	32K	65K
Clock Frequency (Hz/ext. phases required)	to 2 MHz/1φ	2 MHz/0φ	2 MHz/3φ	1 MHz/2φ
Register to Register Add Time (μsec/data word)	1	2	7	2
No. of Registers Arithmetic	1	1	3	2
Index	2	2	0	1 (16 bit)
General Purpose	0	65	0	0
Return Stack Size (No. x bits)	External RAM	1x8 or RAM	External RAM	External RAM
Interrupts	Standard	Standard	Standard	Standard
Type	Vectored, 2 Level	Vectored, 1 Level/PSU	Vectored, 3 Level	Vectored, Multilevel
Direct Memory Access	Optional	Optional (MK3854)	Standard	Optional
BCD Arithmetic (Hardware)	Yes	Yes	No	Yes
Microprogrammable	No	No	No	No
Extended Temp. Range Available	-55°C to 85°C		No	No
Hardware Support				
Processor Cards (CPU system on a card)	Yes	Yes	Yes	Yes
Prototyping System (Hardware and software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	Yes	Yes	No	Yes
Software Support (from this manufacturer)				
Resident Assembler	Yes	Yes	Yes	Yes
Cross Assembler	Fortran IV	Fortran IV	Fortran IV	Fortran IV
Simulator	Fortran IV	Timesharing	Prototyping System	Fortran IV
High Level Language	No	No	No	No
Programs Debug	Yes	Yes	Yes	Yes
Diagnostic	Yes	Yes	Yes	Yes
Edit	No	Yes	Yes	Yes
User Library (▷ 25 programs from user)	No	No	No	No
Delivery Start (Qtr.-Year)	3 Qtr. 75	3 Qtr. 75	1 Qtr. 74	2 Qtr. 74
Alternate Sources	Synertek SY6501/2/3/4	Fairchild F8	None	AMI
Comments	DMA based on a stopping CPU, but address bus connections are not 3 state.	64 bytes of RAM in CPU, 1024 bytes of RCM in PSU, programmable timer.	Three level system services interrupts with multiple program counters and accumulators.	DMA through HALT and three state control *MC6870 and MC6871 from Motorola Component Products, Franklin Park, Ill.

Tinted column indicates additional data is provided on the page noted.

MICROPROCESSORS (Cont'd)

Manufacturer Model For Detailed Data See:	National IMP-4/8/16	National INS4004 (FIPS)	National IPC-16 (PACE) Page 970	National ISP500A (SCMP) Page 981
General Structure	4-Bit Slice	4-Bit CPU	16-Bit CPU	8-Bit CPU
Type	PMOS	PMOS	PMOS	PMOS
No. of Devices per CPU		1	1	1
CPU Size (Pins)	24	16	40	40
Supply Voltage	-12, 5	15 (or -10, 5)	-12, 5	-5, 9
CPU Power Dissipation (mw)		450	700	420
Part Family (from this mfr.)				
CPU	Register and Arithmetic Unit	INS4004	Processing and Control Element	
Clock Driver	Clock Generator		System Timing Element	On-chip Oscillator
I/O Interface	Interface Latches, 8/16-bit Transceivers		Bidirectional Transceiver Element	
RAM	Standard Devices	INS4002 (320 bit and I/O)	256x4	Standard Devices
ROM	Control ROM Standard Devices	INS4001 (256x8 and I/O)	1024x16	Standard Devices
PROM	Standard Devices		512x8	Standard Devices
UART/USRT			None	Standard Device
Other System Parts	Interface Logic Address Latches	INS4003 Shift Register INS4008/9 Standard Memory Interface	Address Latch, Interface Latch	
Architecture				
Data Word Size (bits)	4/8/16	4	8 or 16	8
Instruction Word Size (bits)	8, 12, 16, 20	8, 16	16	8, 16
Directly Addressable Instruction Words (No.)	4K/65K/65K	4K	65K	65K
Clock Frequency (Hz/ext. phases required)	to 700 kHz/4 ϕ	500 to 740 kHz/2 ϕ	2 MHz/2 ϕ	1 MHz/0 ϕ
Register to Register Add Time (μ sec/data word)	12/4.6/4.6	10.8	8	28
No. of Registers Arithmetic	4	1	0	1
Index	0	0	0	4
General Purpose	0	16	4	3
Return Stack Size (No. x bits)	16 x No. of bits	3x12	10x16	
Interrupts	Standard	None	Standard	Standard
Type	1/2/2 Level		Vectored, 6 Level	Vectored
Direct Memory Access	Optional	None	Optional	Standard
BCD Arithmetic (Hardware)	No	Yes	Standard	Standard
Microprogrammable	Yes	No	No	No
Extended Temp. Range Available	-55°C to 85°C			-25°C to 85°C
Hardware Support				
Processor Cards (CPU system on a card)	Yes	No	Yes	Yes
Prototyping System (Hardware and software development system)	Yes	No	Yes	Yes
In-System Emulator (Tests system in place)	No	No	No	No
Software Support (from this manufacturer)				
Resident Assembler	Yes	No	Yes	Yes
Cross Assembler	Fortran IV	No	Fortran IV	Fortran IV, Timesharing
Simulator	No	No	No	Yes
High Level Language	SM/PL	No	SM/PL	SM/PL
Programs Debug	Yes	No	Yes	Yes
Diagnostic	Yes	No	Yes	Yes
Edit	Yes	No	Yes	Yes
User Library (> 25 programs from user)	No	No	No	Yes
Delivery Start (Qtr.-Year)	1 Qtr. 73	3 Qtr. 75	3 Qtr. 75	1 Qtr. 76
Alternate Sources	None	Intel	None	Rockwell (Future)
Comments	DMA requires external controller.		DMA requires external controller.	

Tinted column indicates additional data is provided on the page noted.

MICROPROCESSORS (Cont'd)

Manufacturer Model For Detailed Data See:	Raytheon Semi 2901	RCA CDP1800 (COSMAC) Page 993	Rockwell PPS-4/2	Rockwell PPS-8
General Structure	4-Bit Slice	8-Bit CPU	4-Bit CPU	8-Bit CPU
Type	TTL	CMOS	PMOS	PMOS
No. of Devices per CPU		2	1	1
CPU Size (Pins)	40	28 or 40	42	42
Supply Voltage	5	3 to 15	17 (or -12, 5)	17 (or -12, 5)
CPU Power Dissipation (mw)	925	60	225	225
Part Family (from this mfr.)				
CPU	2901	CDP1801U Control CDP1801R Register	PPS-4	PPS-8
Clock Driver		Standard Devices	Clock Gen. or On-chip	Clock Generator
I/O Interface	2905/6/7 Bus Transceivers		GP I/O (12 bits) Bus Interface	GP I/O (12 bits) Bus Interface
RAM	2950/51 (256x1) 2952 (1024x1)	Standard Devices	256x4	256x8
ROM	2960/61 (102x8)	Standard Devices	1024x8, 2048x8	1024x8, 2048x8
PROM	2970/71 (256x4)	None	Elect. Alt. ROM	Elect. Alt. ROM
UART/USRT		None	Serial Data Controller, Telecommunications Data Interface (incl. Modem)	Serial Data Controller, Telecommunications Data Interface (incl. Modem)
Other System Parts	2909 Microprogram Sequencer		Display Controller (Panaplex) GP Keyboard Display, Keyboard Printer Control, Victor Printer Control	DMA Controller Parallel Data Controller Floppy Disc Controller Display Cont. (Panaplex), Keyboard Printer Control, Victor Printer Control
Architecture				
Data Word Size (bits)	Multiple of 4	8	4	8
Instruction Word Size (bits)	9	8	8, 16 (Multifunction Instr.)	8, 16, 24 (Multifunction Instr.)
Directly Addressable Instruction Words (No.)		65K	4K	16K
Clock Frequency (Hz/ext. phases required)	to 10 MHz/1 ϕ	0 to 4 MHz/1 ϕ	199 KHz/0 or 2 ϕ	256 KHz/2 ϕ
Register to Register Add Time (μ sec/data word)	0.125	6 (2.7 MHz clock)	5	4
No. of Registers Arithmetic	0	1	0	0
Index	0	0	0	0
General Purpose	17	32	3	6
Return Stack Size (No. x bits)	4x4 (2909)	External RAM	2x12	32x8
Interrupts	Optional	Standard	None	Standard
Type		1 Level		3 Level
Direct Memory Access	Optional	Standard (on-chip)	None	Optional DMA Controller
BCD Arithmetic (Hardware)	No	No	No	No
Microprogrammable	Yes	No	No	No
Extended Temp. Range Available	-55°C to 125°C	-55°C to 125°C Standard	-55°C to 125°C	-55°C to 125°C
Hardware Support				
Processor Cards (CPU system on a card)	No	No	Yes	Yes
Prototyping System (Hardware and software development system)	No	Yes	Yes	Yes
In-System Emulator (Tests system in place)	No	No	Yes	Yes
Software Support (from this manufacturer)				
Resident Assembler	No	Yes	Yes	Yes
Cross Assembler	No	Fortran IV, Timesharing	Fortran IV, Timesharing	Fortran IV, Timesharing
Simulator	No	Yes	Yes	Yes
High Level Language	No	No	No	No
Programs Debug	No	Yes	Yes	Yes
Diagnostic	No	Yes	Yes	Yes
Edit	No	Yes	Yes	Yes
User Library (> 25 programs from user)	No	No	Yes	No
Delivery Start (Qtr.-Year)	1 Qtr. 76	1 Qtr. 75	PPS-4 3 Qtr. 72, PPS-4/2 3 Qtr. 75	1 Qtr. 75
Alternate Sources	AMD 2901	None	National PPS-4 (Future)	National PPS-8 (Future)
Comments		DMA address pointer and control logic on chip.	The PPS-4/2 is 2 chip clock, direct display drive, expanded I/O on CPU chip; 128-4 RAM, 2048x8 ROM, 16 I/O ports on separate memory-I/O chip.	

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MICROPROCESSORS (Cont'd)

Manufacturer Model For Detailed Data See:	Signetics 2650 Page 997	Signetics N3002 Page 1007	Synertek SY6501/2/3/4	Texas Instruments SBP0400
General Structure	8-Bit CPU	2-Bit Slice	8-Bit CPU	4 Bit Slice
Type	NMOS	TTL	NMOS	I ² L
No. of Devices per CPU	1		1	
CPU Size (Pins)	40	28 and 40	40 or 28	40
Supply Voltage	5	5	5	200 mA at 0.85V
CPU Power Dissipation (mw)	500	800	200	170
Part Family (from this mfr.)				
CPU	2650	N3001 Microprogram Control Unit N3002 Control Processing Element	SY6501 (2 ϕ clock) SY6502/3 (self clocking)	SBP0400
Clock Driver	Standard Devices	Standard Devices	Not required	Standard Devices
I/O Interface	Standard Devices	Standard Devices	Yes	Standard Devices
RAM	Standard Devices	Standard Devices	Standard Devices	Standard Devices
ROM	Standard Devices	Standard Devices	Standard Devices	Standard Devices
PROM	Standard Devices	Standard Devices	No	Standard Devices
UART/USRT	None	None	None	Standard Devices
Other System Parts		N3214 Interrupt Control	SY6520 Peripheral Interface Adapter SY6530 (1K ROM, 64 bytes RAM, 16 I/O)	
Architecture				
Data Word Size (bits)	8	Multiple of 2	8	9 (Microinstruction Select)
Instruction Word Size (bits)	8, 16, 24	≥ 18	8, 16, 24	
Directly Addressable Instruction Words (No.)	32K	512	65K	(512 Microinstructions)
Clock Frequency (Hz/ext. phases required)	0 to 1.25 MHz/1 ϕ	to 6 MHz/1 ϕ	to 2 MHz/1 ϕ	to 2 MHz/1 ϕ
Register to Register Add Time (μ sec/data word)	4.8		1	0.5 (2 MHz clock)
No. of Registers Arithmetic	0	2	1	2
Index	0	0	2	0
General Purpose	7	10	0	8
Return Stack Size (No. x bits)	8x15	None	External RAM	None
Interrupts	Standard	Optional	Standard	Optional
Type	Vectored	8 Level Priority	Vectored, 2 Level	Optional
Direct Memory Access	Standard	No	Optional	Standard
BCD Arithmetic (Hardware)	Standard	No	Yes	Microprogrammable
Microprogrammable	No	Yes	No	(512 Microinstructions)
Extended Temp. Range Available	No	No	-55°C to 85°C	-55°C to 125°C
Hardware Support				
Processor Cards (CPU system on a card)	Yes	No	Yes	No
Prototyping System (Hardware and software development system)	Yes	No	Yes	Yes (hardware)
In-System Emulator (Tests system in place)	Yes	No	Yes	No
Software Support (from this manufacturer)				
Resident Assembler	No	No	Yes	No
Cross Assembler	Fortran IV, PDP-11	No	Fortran IV	Fortran microassembler
Simulator	Fortran IV	No	Fortran IV	No
High Level Language	No	No	No	No
Programs Debug	Yes	No	Yes	No
Diagnostic	Yes	No	Yes	No
Edit	Yes	No	No	No
User Library ($>$ 25 programs from user)	No	No	No	No
Delivery Start (Qtr.-Year)	2 Qtr. 75	3 Qtr. 75	4 Qtr. 75	1 Qtr. 75
Alternate Sources	None	Intel	MOS Technology 6501/2/3/4	None
Comments	Any of the general purpose registers can be used as an index register.	Uses 74S182 for Look-Ahead Carry.	DMA based on a stopping CPU, but address bus connections are not 3 state.	Current drain can be set from 0.001 to 200 mA.

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IC UPDATE

MICROPROCESSORS (Cont'd)

Manufacturer Model For Detailed Data See:	Texas Instruments TMS1000/1200	Texas Instruments TMS1070/1270	Texas Instruments TMS1100/1300	Texas Instruments TMS8080
General Structure	4-Bit Microcomputer	4-Bit Microcomputer	4-Bit Microcomputer	8-Bit CPU
Type	PMOS	PMOS	PMOS	NMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	28 or 40	28 or 40	28 or 40	40
Supply Voltage	15	15	15	±5, 12
CPU Power Dissipation (mw)	90	100	90	1500
Part Family (from this mfr.)				
CPU	TMS1000 (28 pin) TMS1200 (40 pin)	TMS1070 (28 pin) TMS1270 (40 pin)	TMS1100 (28 pin) TMS1300 (40 pin)	TMS8080
Clock Driver	On-chip Oscillator	On-chip oscillator	On-chip oscillator	None
I/O Interface	On-chip output encoder, addressable output latches.	On-chip output encoder, addressable output latches	On-chip output encoder, addressable output latches	SN74S412 I/O Port, TMS5501 Multifunction I/O Controller
RAM	64x4 on-chip	64x4	128x4 on-chip	Standard Devices
ROM	1024x8 on-chip	1024x8	2048x8 on-chip	Standard Devices
PROM	Not required	Not required	Not required	Standard Devices
UART/USRT	None	None	None	TMS5501, TMS6011
Other System Parts	None	None	None	SN74S240/241 Line Driver
Architecture				
Data Word Size (bits)	4	4	4	8
Instruction Word Size (bits)	8	8	8	8, 16, 24
Directly Addressable Instruction Words (No.)	1K	1k	2K	65K
Clock Frequency (Hz/ext. phases required)	300 kHz/0φ	300 kHz/0φ	300 kHz/0φ	2 MHz/2φ
Register to Register Add Time (μsec./data word)	34 (350 kHz clock)	34 (350 kHz clock)	34 (350 kHz clock)	2
No. of Registers Arithmetic	1	1	1	1
Index	0	0	0	0
General Purpose	1	1	1	6
Return Stack Size (No. x bits)	1x10	1x10	1x10	External RAM
Interrupts	None	None	None	Standard
Type				Vectored, 8 Level
Direct Memory Access	None	None	None	Standard
BCD Arithmetic (Hardware)	Microprogrammable	Microprogrammable	Microprogrammable	Yes
Microprogrammable	Yes	Yes	Yes	No
Extended Temp. Range Available		Yes	Yes	No
Hardware Support				
Processor Cards (CPU system on a card)	No	No	No	No
Prototyping System (Hardware and software development system)	Yes	Yes	Yes	No
In-System Emulator (Tests system in place)	Yes	No	Yes	No
Software Support (from this manufacturer)				
Resident Assembler	Yes	Yes	Yes	No
Cross Assembler	Timesharing	Yes	Yes	Timesharing
Simulator	Timesharing	Yes	Yes	Timesharing
High Level Language	No	No	No	No
Programs Debug	Yes	Yes	Yes	Yes
Diagnostic	Yes	Yes	Yes	Yes
Edit	Yes	Yes	Yes	Yes
User Library (> 25 programs from user)				No
Delivery Start (Qtr.-Year)	1 Qtr. 75	4 Qtr. 75	4 Qtr. 75	2 Qtr. 75
Alternate Sources	None	None	None	AMD 9080, Intel 8080
Comments	A 64 pin version, TMS1099/SE-1, permits use of external PROM, RAM or ROM for program development.	35v output drive capability.	A 64-pin version, TMS1098/SE-2 permits use of external PROM/RAM/ROM for program development.	

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MICROPROCESSORS (Cont'd)

Manufacturer Model For Detailed Data See:	Texas Instruments TMS9900	Toshiba TLCS-12A	Western Digital MP1600	Western Digital MCP1600
General Structure	16-Bit CPU	12-Bit CPU	16-Bit CPU	8-Bit CPU
Type	NMOS	PMOS	NMOS	NMOS
No. of Devices per CPU	1	1	3	3
CPU Size (Pins)	64	36	40/device	40/device
Supply Voltage	±5, 12	±5	±5, 12	±5, 12
CPU Power Dissipation (mw)	1000	800	600	600
Part Family (from this mfr.) CPU	TMS9900	T3190	MP1651 Data Chip MP1661 Control Chip	CP1611 Data Chip CP1621 Control Chip
Clock Driver	Standard Devices	Internal Oscillator	None	None
I/O Interface	Standard Devices	T3218 I/O Control Unit	CP1851 GPIO	CP1851 GPIO
RAM	Standard Devices	T3151 (128x4)	Standard Devices	Standard Devices
ROM	Standard Devices	Standard Devices	CP1631 Microm, Standard Devices	CP1631 Microm, Standard Devices
PROM	Standard Devices	T3181 Erasable ROM	Not required	Not required
UART/USRT	Standard Devices	No	Standard Devices	Standard Devices
Other System Parts		T3216 Memory Control Unit T320 General Purpose 4 + 8 bit I/O Register	DM1881 DMA, FD1771 Floppy Disk, UC1671 ASTRO	DM1881 DMA, FD1771 Floppy Disk, UC1671 ASTRO
Architecture				
Data Word Size (bits)	16	12	16	8 or 16
Instruction Word Size (bits)	16, 32, 48	12, 24	16	16
Directly Addressable Instruction Words (No.)	65K	4K	65K	65K (84 Microinstructions)
Clock Frequency (Hz/ext. phases required)	3 MHz/4φ	1.2 MHz/0φ	3.3 MHz/4φ	3.3 MHz/4φ
Register to Register Add Time (μsec/data word)	4.67	13	2.7	0.3 (8-bit), 0.6 (16-bit)
No. of Registers Arithmetic	16	0	4	0
Index	15	0	2	0
General Purpose	16 (in memory)	7	2	26
Return Stack Size (No. x bits)	None		External RAM	External RAM
Interrupts	Standard	Yes	Standard	Standard
Type	Vectored, 16 Level		Vectored	Vectored, 4 Level
Direct Memory Access	Standard	Optional	Standard	Standard
BCD Arithmetic (Hardware)	No	No	Standard	Microprogrammable
Microprogrammable	No	No	Yes	Yes
Extended Temp. Range Available	No		No	No
Hardware Support				
Processor Cards (CPU system on a card)	Yes 990/4	No	Yes	Yes
Prototyping System (Hardware and software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	No	No	No	Yes
Software Support (from this manufacturer)				
Resident Assembler	Yes		Yes	No
Cross Assembler	Timesharing	Yes	No	Timesharing, PDP-11
Simulator	Timesharing	Yes	No	Timesharing, PDP-11
High Level Language	Fortran, Cobol	Yes	No	No
Programs Debug	Yes	Yes	Yes	Yes
Diagnostic	Yes	Yes	Yes	Yes
Edit	Yes	Yes	Yes	Yes
User Library (> 25 programs from user)	Yes	Yes	No	No
Delivery Start (Qtr.-Year)	2 Qtr. 76	2 Qtr. 74	1 Qtr. 75	3 Qtr. 75
Alternate Sources	None	None	None	None
Comments	Instructions include hardware multiply and divide and are software compatible with 990 minicomputers.			Can cross assemble and simulate with DEC PDP-11. Microcontroller version avail.

Tinted column indicates additional data is provided on the page noted.

S6800: The whole Kit.

Smart Terminal.

Complete program editing through CRT and keyboard. Also includes Modem communication to remote computers.

Magnetic Tape.

Cross product software— assembler, loader, simulator.

S6800 Family.

It's all here: MPU, RAM, ROM, PIA, ACIA, PROM, USRT and Modem. By test, the best.

Evaluation Board.

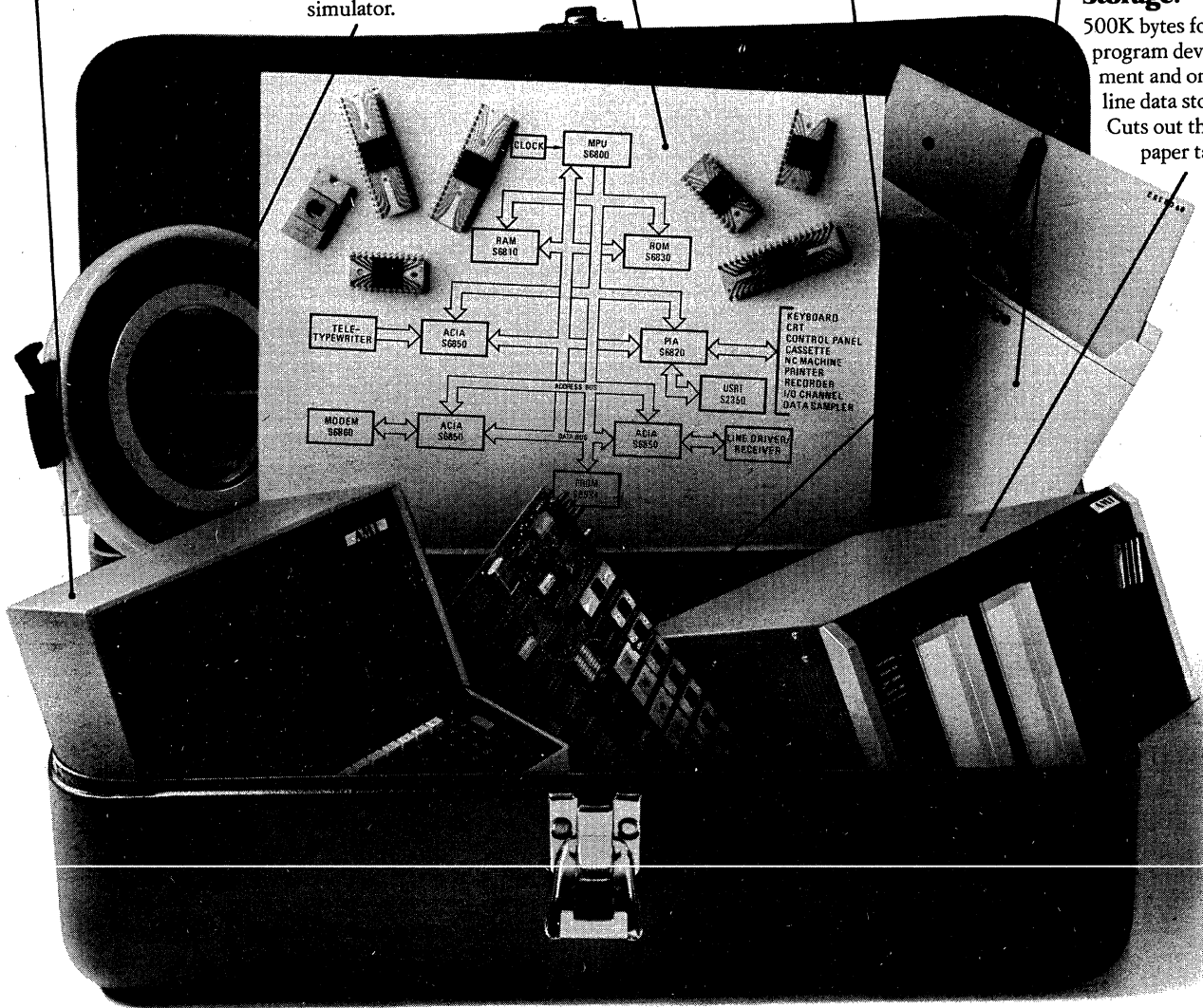
Includes everything you need to evaluate parts, program PROMs and, connected with a peripheral, run programs.

Dual Floppy Disk.

Storage for resident software— assembler, editor, etc.

Disk Program Storage.

500K bytes for program development and on-line data storage. Cuts out the paper tape!



Our S6800 Kit is a big step forward in simplifying your design, evaluation and test programs. For example, our intelligent CRT is simple to operate with either resident or remote software. It really is smart, because it contains an S6800! And it's planned to have an in-circuit emulator added later.

Our dual disk is extremely useful for developing programs, and saves you hours of paper tape shuffling. And our Evaluation Board is loaded with

all the parts you need to get your product on the market on time.

Now for the Caboodle. The dictionary calls it a "package." You'll call it the neatest set of instructions for any kit you've ever bought.

Now why don't you call your nearest AMI sales office or distributor, and ask them for the whole Kit and Caboodle. Or write AMI, 3800 Homestead Road, Santa Clara CA 95051. What could be easier?

Here's where you pickup your Kit.

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AMI

MICROPROCESSOR

And Caboodle.

Software Brochure.

A rundown on AMI software products including assembler, loader and simulator.

S6800 Brochure.

List of goodies. All you want to know about the S6800 family.

Evaluation Board Application Notes.

The why and wherefore of our Prototyping System, and how to make the most of it!

NCSS Users Manual.

All the magic necessary to work with National CSS time-sharing network.

Assembly Language Programming Manual.

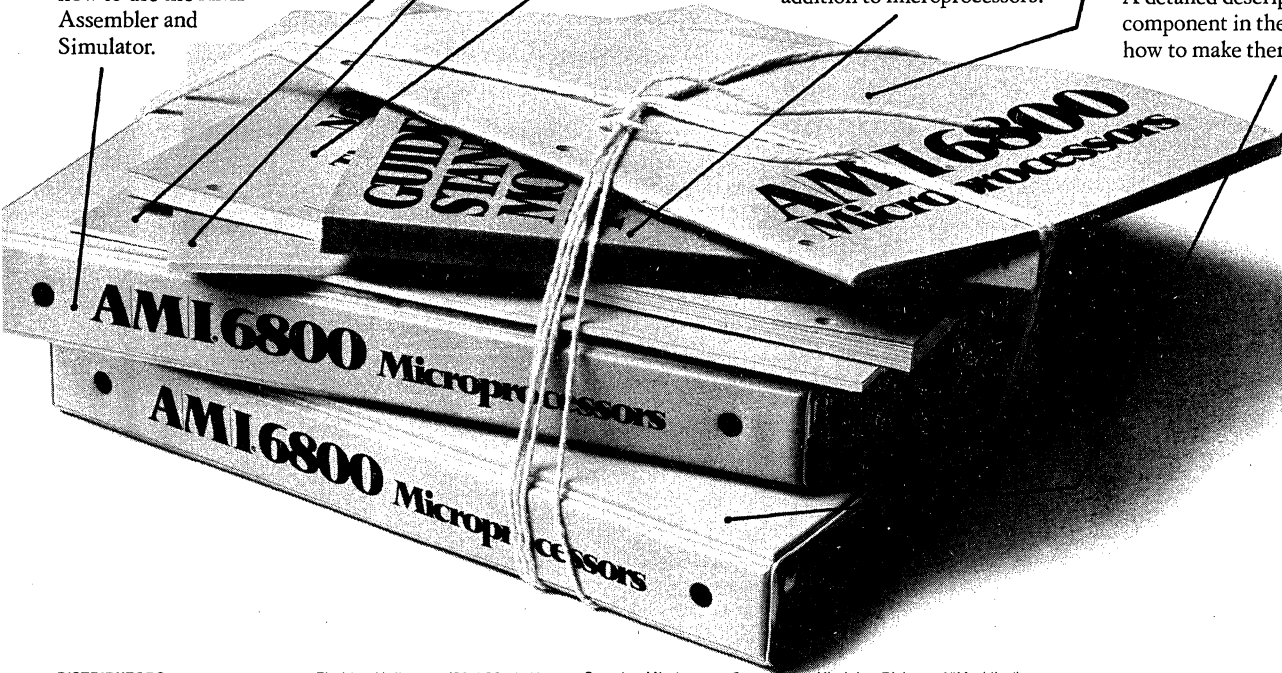
Describes the instruction set and how to use the AMI Assembler and Simulator.

AMI Guide to Standard Products.

All the MOS you might need in addition to microprocessors.

Hardware Reference Manual.

A detailed description of each component in the system, and how to make them work!



DISTRIBUTORS

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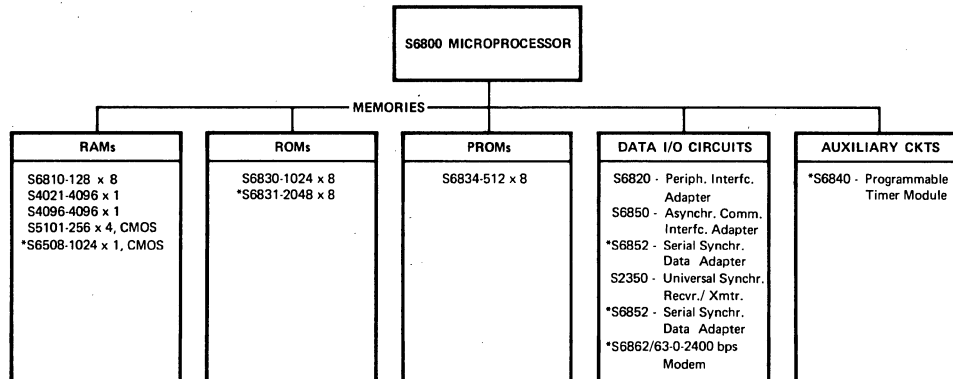
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it's standard at AMI.
AMERICAN MICROSYSTEMS, INC.

AMI
MICROPROCESSOR

S6800 Microcomputer Family



*Future Products - watch for the introduction of these and other S6800 Family products from AMI.

S6800 Microprocessor (MPU) - an 8-bit parallel processor, with the ability to address up to 65K bytes of memory, and execute instructions in 2 microseconds. It is manufactured using N-channel MOS technology and operates on a single +5V power supply. All inputs and outputs are TTL compatible. The MPU has six internal registers, four types of vectored interrupts and 72 basic instructions. The basic instructions can be used in different addressing modes to save instruction execution time and memory space.

S6810 Static Read/Write Memory, 128 x 8 - an N-channel MOS memory designed and organized to be compatible with the S6800 MPU. Its data, address and control line organization and functions match those of the MPU, all signal levels are TTL compatible and no clocks or refreshing are needed. There are two versions of this memory: S6810 with 1.0 μ sec maximum access time, and S6810-1 with 575 nsec. maximum access time.

ROMs - 1024 x 8 and 2048 x 8 - two N-channel MOS mask programmable read only memories that are used for storing the S6800 MPU operating programs. These ROMs have data, address, and control line organization compatible with that of the MPU; signal levels are TTL compatible and access times of 575 nsec. and 500 nsec., respectively.

S6820 Peripheral Interface Adapter (PIA) - a general purpose programmable interface circuit that provides the means for most any kind of peripheral device or circuit to communicate with the S6800 MPU. The PIA has two 8-bit input/output ports for communicating with the peripherals and the MPU can program either

port to send or receive data. Each port has two control lines associated with it. These also can be programmed by the MPU to handle interrupt and handshake routines with the peripherals.

S6850 Asynchronous Communication Interface Adapter (ACIA) - a general purpose communications interface that allows an asynchronous serial communications device to transmit data to and receive data from a S6800 microcomputer system. The ACIA can be programmed for handling different word lengths at various data rates; it also has parity generation and checking capability. For interfacing with the S6860 modem, the ACIA provides three status and command lines.

S6852 Serial Synchronous Data Adapter - a bus compatible high speed synchronous communications interface.

S6860 Modem - A 0-600 bps digital modem providing the necessary modulation, demodulation and supervisory controls to implement a serial data communications link over a voice grade channel. The modem is fully compatible with the S6800 microcomputer system, interfaces directly with the S6850 ACIA, and can be used in a wide variety of stand-alone modems, data communication terminals, I/O interfaces, and other data handling systems. N-channel silicon gate technology permits the modem to operate on a single +5V power supply and its inputs and outputs are TTL.

S6862/63 2400 Baud Modem - a two-chip synchronous high-speed modem.

S6800 SYSTEM COMPATIBLE COMPONENTS

S2350 Universal Synchronous Receiver/Transmitter (USRT) - a general purpose communications interface that allows a high speed synchronous communications device to transmit data to and receive data from a S6800 microcomputer system. It connects to the peripheral device via separate serial transmit and receive lines and to the S6800 system data and address bus through a S6820 PIA.

The USRT has separate internal receiver and transmitter sections, which can be clocked by two separate clocks. It has the capability to handle different word lengths, generate and check parity and

other conditions, detect sync during receive, and send a fill character during transmit operation.

RAMs - 4K (22-pin and 16-pin) - two N-channel Si-gate dynamic RAMs for large volume low cost read/write storage. Both have TTL compatible inputs and outputs, that can be easily interfaced to the S6800 system bus; access times as low as 200 nsec.

RAMs - 1K, CMOS - two silicon-gate CMOS RAMs for low power and non-volatile memory systems. TTL compatible I/O; can be operated either at +5V, or +10V.

S6800 Microcomputer Systems

THE FIRST FAMILY

The AMI S6800 Microcomputer Family is an LSI integrated circuit family for building microcomputers. In its hardware concept it is the same as the SSI and MSI families, except with SSI/MSI each integrated circuit is only an individual logic element (or segment of a larger random logic circuit), whereas in the LSI family each is a whole subsystem of a microcomputer.

By bringing to LSI microcomputer hardware the advantages of the family concept — a series of functionally and electrically matched circuits — the AMI S6800 allows the circuit designer to build complete microcomputer systems of different configurations by simply selecting from the matched subsystem circuits, interconnecting them with the microprocessor into a system, and providing the necessary operating voltages and clock signals. Such a method is superior to choosing an MPU and then matching different memory or I/O circuits to it through interfaces, as must be done with most microprocessor products. The matched LSI family makes the design task simple, fast, and the functional complexity of the system can be increased, while physical size is reduced.

The AMI S6800 Microcomputer Family is a leader in developing this family concept, because S6800 has a wider selection of compatible memory, I/O, and auxiliary circuits, has comprehensive hardware and software support, and wide user acceptance.

COMPLETE AND EASY

The AMI S6800 Microcomputer Family hardware includes the S6800 Microprocessor, a selection of RAM, ROM, and PROM memories, a wide variety of data input/output circuits, and various other support circuits. These components may be assembled in a building block manner into a simple or complex microcomputer system, for many general and special purpose applications. It remains to the user to integrate the microcomputer into his own larger system and to program it for a specific task.

One important design feature of the S6800 family is that within any microcomputer system all components are directly compatible in the system bus and I/O pro-

tol, as well as in individual signal functions, circuit performance characteristics, and logic levels. All operate on a single +5V power supply.

To facilitate system design and programming, AMI provides versatile and easy to use prototyping hardware, various software packages for program generation, an economical CRT/disc system for on-site program generation and debugging, comprehensive hardware and software reference documentation, and other applications support. Such backup is a continuous and expanding effort at AMI.

THE BASIC SYSTEM

A basic S6800 system is shown in Figure 1. In this system the S6800 Microprocessor (MPU) is supported by RAM and ROM (or PROM) memory and controls one input/output circuit. The 1024-byte ROM (or 512-byte erasable PROM) is used to store the operating program, the 128-byte RAM provides working storage for the MPU, and the Peripheral Interface Adapter (PIA) provides two independently programmable 8-bit input/output ports for communicating with two peripheral devices.

The S6800 system is bus oriented. Eight lines form the data bus and 16 more lines make up the address bus. The MPU controls the bus and all other devices — the memories and the PIA — attach to the bus and wait for instructions from the MPU to supply or receive data. In the system shown in Figure 1, the MPU uses address lines A2, A13, and A14 to select one of the three devices on the bus and uses the Read/Write and Valid Memory Address lines to instruct the devices to receive or send data to the MPU. When communicating with the PIA, address lines A0 and A1 are used to select among the two peripheral devices A and B; the CA1, CA2, CB1, and CB2 lines can be used to send out control signals to the peripherals, or receive service requests.

The basic system is a complete microcomputer, which can be used for a large variety of applications. It is simple but versatile. It can be easily reprogrammed by changing the ROM or using the erasable PROM instead. The user must provide only the two-phase clock signal source, a power-up/restart circuit, and a single +5V power supply to complete the hardware.

AN S6800 SYSTEM EXPANDS GRACEFULLY

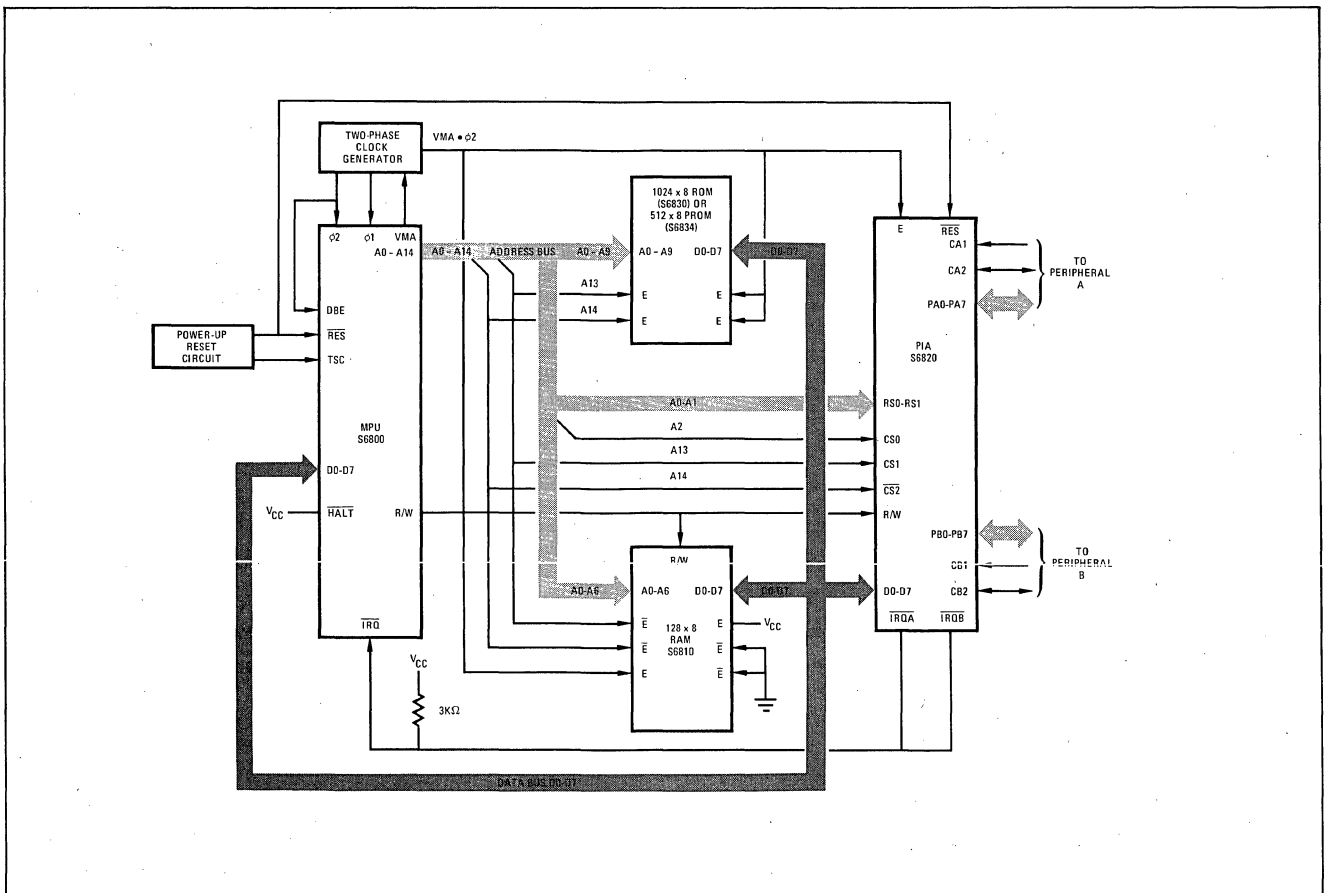
The S6800 Microcomputer Family is easy to expand. It has every one of the basic types of memories – RAM, ROM, and PROM – and all essential forms of interfaces for digital telecommunication and peripherals – serial, parallel, asynchronous, and synchronous. System memory is easy to expand because multiple addressing modes of the MPU make memory access fast and efficient; all I/O devices are designed for operational flexibility and efficiency in MPU cycle utilization. Memory, I/O, and other devices in the S6800 family are all compatible in load levels and the entire system can run on one common clock. Consequently, you often can eliminate all circuit design, save for the simple clock and power-up/restart circuits.

In general, the system can be expanded in a modular manner, by simply connecting onto the bus the required devices. These can be any combination of memory and input/output circuits. In this modular manner a system of nearly any complexity and con-

figuration can be assembled. Because you are designing with a small number of integrated circuits, your circuit layout task is simple and the entire microcomputer can be located on a single circuit card. (Systems with more than ten devices on the bus require the addition of address and data bus buffers to operate at full speed).

In some special purpose applications you may need to attach your own interface devices to the bus. As a result, more circuit design will be required, but you will find the S6800 MPU easy to work with. It has features that allow it to be used in many different modes of operation and in various systems. For example, by using the Halt, Three State Control, and Data Bus Enable lines you can easily design a direct memory access system, in which either the MPU or a peripheral device can read or write into the RAM and utilize the bus on a priority basis. You can also design a multiprocessor system, in which several MPUs are attached to the same bus and share processing assignments, as well as memory space.

FIGURE 1 BASIC S6800 MICROCOMPUTER SYSTEM



S6800 INPUT/OUTPUT

One other important advantage that S6800 has to offer in comparison with any other microcomputer system is input/output versatility. In any computer system, large or small, the CPU internal functions are determined by its architecture and the user usually has little opportunity or need to alter them. On the other hand, the I/O configuration is almost always determined by the user and subject to change as peripherals are added or other system alterations are introduced. The I/O configuration is important to the user because it affects the efficiency of the CPU itself, determines the ease and speed with which peripherals can interact with the system and determines the throughput rate of the system.

Therefore, the efficiency and versatility with which a CPU can handle its I/O – both in hardware and software – is an important criteria and of particular concern to the user. It is in this area that the S6800 MPU excels.

- In an S6800 system, the MPU relegates most of the I/O control to such I/O interfaces as the PIA or ACIA. Each of these circuits is programmable and can interface with peripheral devices without directly involving the MPU. For example, the MPU can preprogram a PIA to either input data into the MPU or to receive it. Thereafter, the PIA circuits assume all functions of interfacing with the peripherals and the MPU never has to look at the interface until service is required. It must service interrupts from the PIA, but never needs to wait for input data to become available or for output data to be accepted. This relieves the MPU of its I/O functions, makes it more efficient in its primary task of data processing, and significantly increases system throughput.
- The I/O interfaces and memory are both located in the same address space within the S6800 system. The MPU can access any I/O device the same as a memory location – with address lines, instead of separate I/O control lines. Therefore, it can manipulate data in the I/O interface registers with the same programmed instructions as it uses for memory locations. This adds programming flexibility and increases system efficiency.
- The S6800 Instruction Set complements the above I/O addressing capability with specific instructions

that can be used to access memory as well as I/O circuit registers and perform directly various manipulations on the data.

S6800 INSTRUCTION SET

The S6800 MPU has a set of 72 basic instructions. These include binary and decimal arithmetic functions, as well as logical, shift, rotate, load, store, branch, interrupt, and stack manipulation functions. Most of the instructions have several variations and most can be used with several memory addressing modes. Thus, the total complex of instructions available to the programmer actually is 197.

An instruction can be from one to three bytes long, depending on the addressing mode used with the instruction. In single byte instructions no memory address is required because the operation is performed on one of the internal MPU registers. In multiple byte instructions the second and third byte can be the operand, or a memory address for the operand.

A noteworthy feature of the S6800 MPU is that some of the instructions can operate directly on any memory location. In most computer systems it is common that the processor fetches an operand from memory, stores it in the accumulator, then executes the operation in the ALU, and finally writes the result back into the memory. The S6800 is able to accomplish the same with only a single instruction, because it operates with any external location in the same manner as with an internal register. For example, it can directly increment or decrement the contents of a memory location. Because the MPU addresses I/O devices just like a memory location, it can do the same with registers inside the PIA or ACIA.

HARDWARE/SOFTWARE SUPPORT.

The S6800 Microcomputer Family hardware is completely supported by an array of application program development software, various levels of hardware and software reference documentation, a software development station, and a hardware prototyping evaluation board. These comprehensive software and hardware aids have many advanced timesaving features that make the S6800 software/hardware support structure the most modern and convenient.

The program development software includes an Assembler, a Linking-Loader, and a Simulator program, all of which are suitable for direct implementation on large-scale computer systems and also are available through several timesharing networks. The reference documentation consists of

- The S6800 Microprocessor Brochure
- The Software Data Brochure
- Assembly Language Programming Manual
- Hardware Reference Manual
- Other Application and User Information

The software development station is a complete self-contained S6800 microcomputer/keyboard/CRT, with a separate floppy disc memory. Together, they provide the user with a complete, convenient, and economical program development facility. The disc memory contains the Resident Assembler and also has space for storage of programs in development, or other data.

The prototyping evaluation board is a fully functional microcomputer, with the MPU, ROM, RAM, and PROM memory, as well as several I/O provisions on the board. The S6800 bus extends to the edge connector, so that any amount of external I/O can be connected also. It has a resident operating system program stored in ROM and all PROM programming hardware is right on the board. This board can be used for circuit evaluation, PROM programming, or as a microprocessor board in low quantity systems.

Cross-Assembler. The AMI 6800 Cross-Assembler is designed to operate on large-scale computers and converts S6800 Assembly Language input statements into machine language for the purpose of generating application programs. It defines the form and syntax according to which the S6800 instruction set can be structured into statements and thus forms the backbone for the usage of the S6800 Microcomputer System. The Cross-Assembler contains many advanced programming features for convenience and efficiency.

- **Local Labels** – a directive which permits symbol definition within a local region. Since the symbol is only referenced within that region, the same symbol can be reused in a different local region.
- **Full Macro Capability** – a sequence of instructions and associated variable parameters can be designated by a symbolic label. The assembler will substitute the complete sequence for the label, wherever the label is called out.

- **Conditional Assembly** – when parts of a program are the same for different versions of the program, the conditional assembly feature can be used to instruct the assembler to automatically include only those parts needed for a particular version of the program.

Symbolic Expressions – symbolic labels can be used for memory locations as well as for program constants, thus generally simplifying the programmers task.

Relocatable Program Segments – the object code within a program segment is always defined with respect to the start of the segment, thus allowing the Linking Loader to assign actual memory addresses later. This gives maximum flexibility in final assembly.

- **Formatted Listings** – assembly listings are formatted into 11-inch pages, with a two line header identifying the page number, date and time of assembly, program name, and column labels for the assembly printout.

The Cross-Assembler is available for computers supporting standard ANSI FORTRAN IV. For low-cost, high-speed program development, it is also written in SYSTEM 360/370 BAL and is available through timesharing networks, such as National CSS, Inc.

Linking Loader. – The Linking Loader is a program used to assign fixed memory locations to programs generated by the Cross-Assembler and thus structure the users program for a particular memory configuration. The Linking Loader is programmed to operate on the same (large-scale) computer as the Cross-Assembler and is also available on timesharing networks (NCSS and others). It can be used to produce a listing of the external definitions and load map, and a program tape suitable for a prototype system hexadecimal loader or a PROM programmer. Alternatively, it can also generate memory image file for use by the AMI S6800 Simulator program described below.

Simulator. – The AMI S6800 Simulator program is a means by which the user can conveniently check out the operation of programs written for the S6800. It is a program that can be operated on a cross-computer (other than S6800) and cause that computer to respond the same as a S6800 would.

The simulator simulates all S6800 Microprocessor hardware. A complete set of commands is provided for loading and examining the simulated registers and memory, and for controlling the simulator.

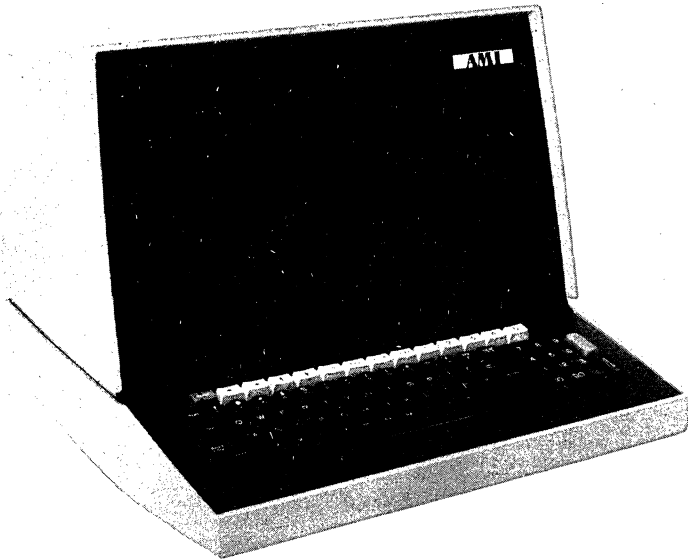
Hardware/Software Development Station

Basic Features

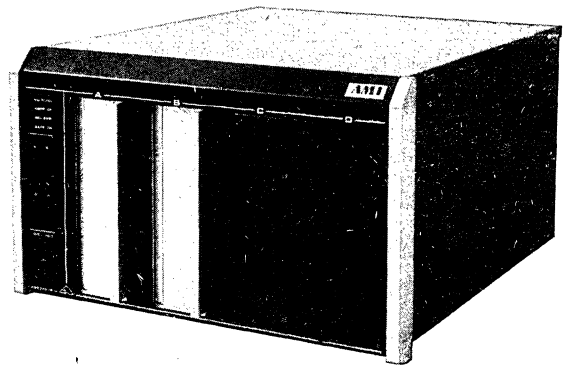
- Resident Assembler Software
- Floppy Disk Operating System
- Resident Debug Software
- 8K Bytes of User RAM
- RS-232 Interface
- System I/O Assigned to Upper Memory Locations
- Full ASCII Keyboard
- 25 x 80 Character CRT Display

Options

- Memory Expandable to 56K Bytes
- Additional PCB Positions Available for Customer Designed Interfaces
- In-circuit Emulation for Hardware Debugging
- PROM Programming Capability



The Hardware/Software Development Station is an intelligent CRT Terminal with the required software and memory space to enable you to develop, debug, and operate S6800 application programs. The CRT/Keyboard terminal contains an S6800 microcomputer, RAM, ROM and PROM memory, as well as interface circuits. The dual floppy disk stores the Basic Operating System, a Resident Assembler, and any other optional system software. It provides over 500K bytes of on-line memory, of which the basic system software takes up less than 25K bytes.

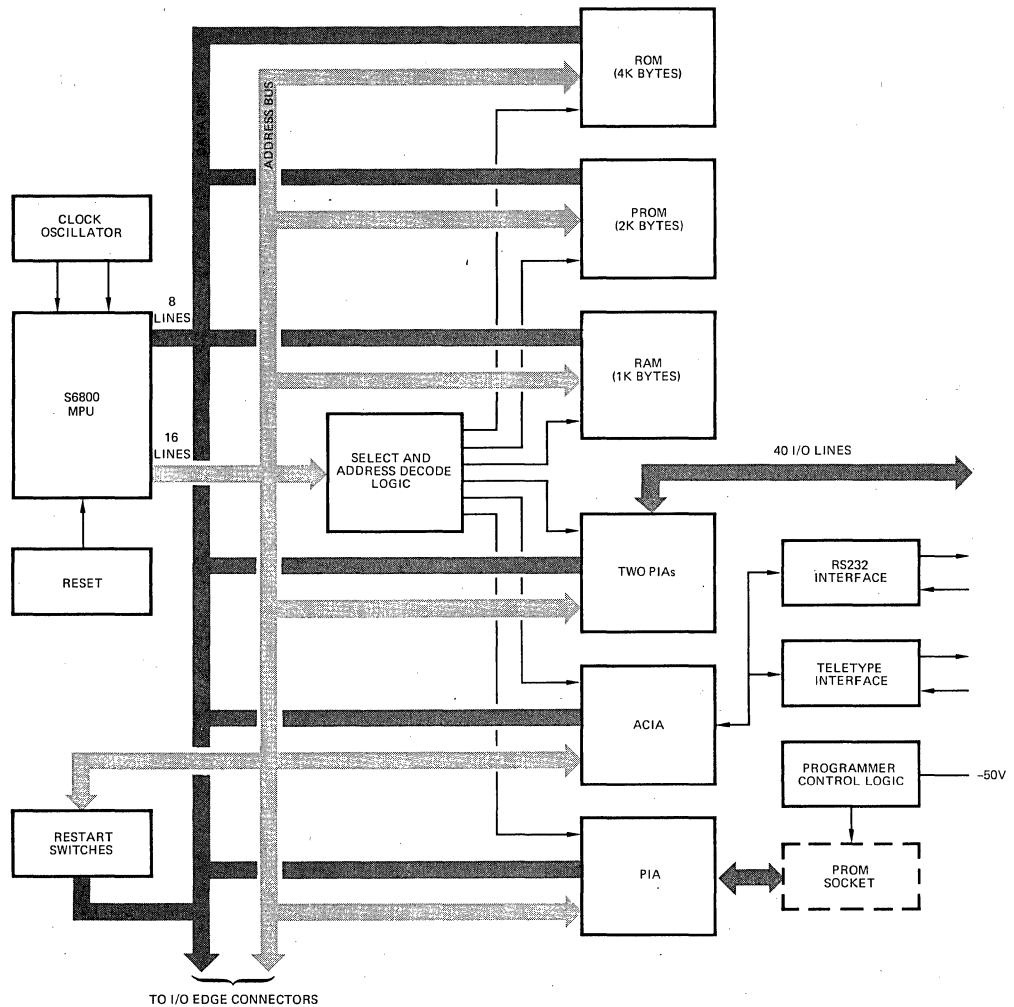


The Hardware/Software Development Station lets you enter source statements on the keyboard, debug your program while viewing it on the CRT, and store the final edited assembled version on the removable diskette.

Alternatively, you can use the CRT Terminal by itself to develop your program on a timeshared computer, then store segments of it in RAM, and debug off line.

Prototyping Evaluation Board

A complete S6800 Microcomputer System on one circuit board – with maximum operational flexibility, to make your hardware development easy.



Hardware Features

- CPU Fully Buffered
- Variable Frequency Clock (can also be locked to 1 MHz)
- On-board PROM Programmer
- Provisions for:
 - 4K bytes of ROM
 - 2K bytes of PROM
 - 1K bytes of RAM
- Two User Available PIAs
- Current-loop or RS-232 TTY Interfaces (50 to 19.2K Baud)
- Switch-changeable Restart Vector
- Three Types of DMA Available

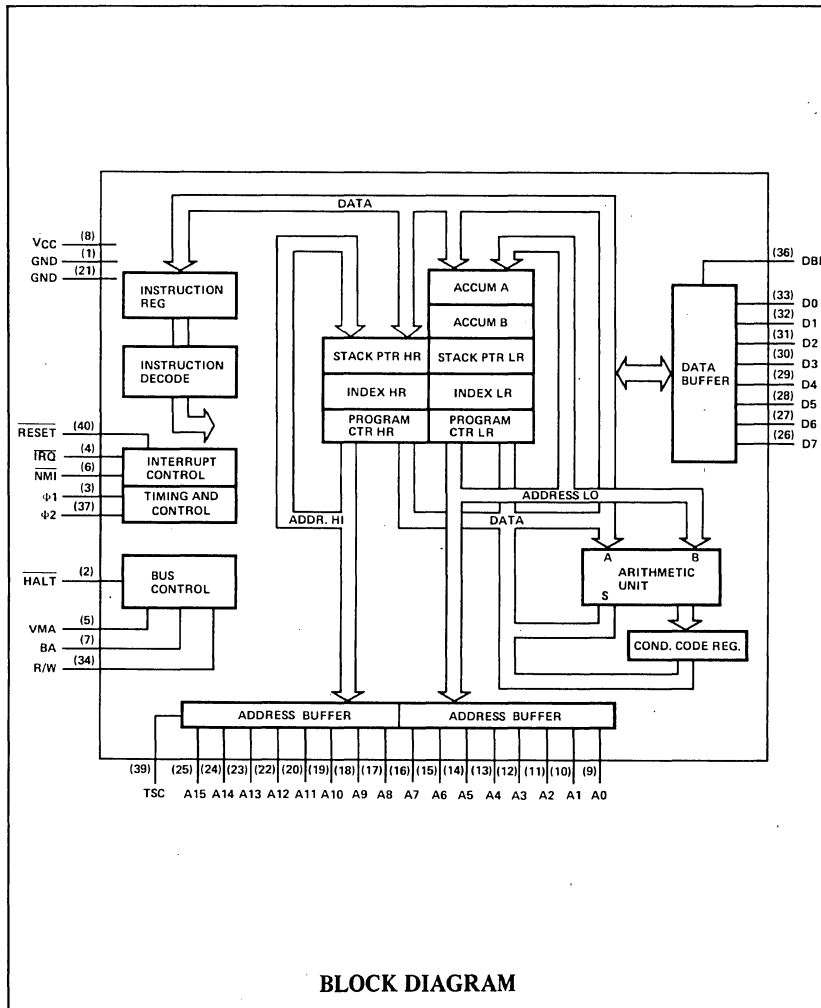
Resident Software

- Load Memory
- Display Memory
- Display MPU Registers
- Move Memory
- Read ROM or PROM
- Program PROM
- Verify PROM
- RS³ Subroutine Library
- Punch Tape
- Start Execution from Any Location

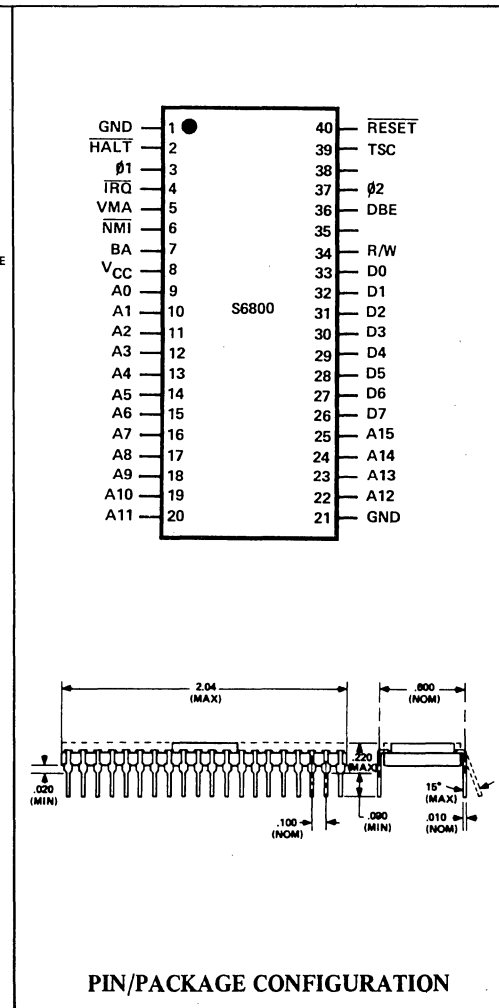
AMI

MICROPROCESSOR

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

FEATURES

- Eight-Bit Parallel Processing
- Bi-Directional Data Bus
- Sixteen-Bit Address Bus – 65536 Bytes of Addressing
- 72 Instructions – Variable Length
- Seven Addressing Modes – Direct, Relative, Immediate, Indexed, Extended, Implied and Accumulator
- Variable Length Stack
- Vectored Restart
- 2 Microsecond Instruction Execution
- Maskable Interrupt Vector
- Separate Non-Maskable Interrupt – Internal Registers Saved in Stack
- Six Internal Registers – Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- Direct Memory Access (DMA) and Multiple Processor Capability
- Clock Rates as High as 1 MHz
- Simple Bus Interface Without TTL
- Halt and Single Instruction Execution Capability

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	-0.3 to +7.0V
Input Voltage V_{in}	-0.3 to +7.0V
Operating Temperature Range T_A	0 to +70°C
Storage Temperature Range T_{stg}	-55 to +150°C

DC (STATIC) CHARACTERISTICS

($V_{CC} = 5.0 V \pm 5\%$, $T_A = 25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage (Normal Operating Levels) Logic $\phi 1, \phi 2$	V_{IH} V_{IHC}	+ 2.4 $V_{CC} - 0.3$	- -	V_{CC} $V_{CC} + 0.1$	Vdc
Input Low Voltage (Normal Operating Levels) Logic $\phi 1, \phi 2$	V_{IL} V_{ILC}	-0.3 -0.1	- -	+ 0.4 +0.3	Vdc
Clock Overshoot/Undershoot – Input High Level – Input Low Level	V_{OS}	$V_{CC} - 0.5$ -0.5	- -	$V_{CC} + 0.5$ +0.5	Vdc
Input High Threshold Voltage \overline{Reset} , \overline{NMI} , \overline{Halt} , \overline{IRQ} , Data	V_{IHT}	+ 2.0	-	-	Vdc
Input Low Threshold Voltage \overline{Reset} , \overline{NMI} , \overline{Halt} , \overline{IRQ} , Data	V_{ILT}	-	-	+ 0.8	Vdc
Input Leakage Current ($V_{in} = 0$ to 5.25 V, $V_{CC} = 5.25V$) Logic* $\phi 1, \phi 2$	I_{in}	- -	- -	2.5 100	μA_{dc}
Three-State (Off State) Input Current ($V_{in} = 0.4$ to 2.4 V, $V_{CC} = \max$) Data A0-A15, R/W	I_{TSI}	- -	- -	10 100	μA_{dc}
Output High Voltage ($I_{Load} = -100 \mu A_{dc}$, $V_{CC} = \min$)	V_{OH}	+ 2.4	-	-	Vdc
Output Low Voltage ($I_{Load} = 1.6 \text{ mA}_{dc}$, $V_{CC} = \min$)	V_{OL}	-	-	+ 0.4	Vdc
Power Dissipation	P_D	-	0.600	1.2	W
Capacitance** ($V_{in} = 0$, $T_A = 25^\circ C$, $f = 1.0 \text{ MHz}$) Logic Data, TSC $\phi 1, \phi 2$ A0-A15, R/W	C_{in} C_{out}	- - 80	- - 120	10 15 160 12	pF pF

*Except \overline{IRQ} and \overline{NMI} , which require 3 k Ω pullup load resistors for wire-OR capability at optimum operation.

**Capacitances are periodically sampled rather than 100% tested.

AC (DYNAMIC) CHARACTERISTICS

($V_{CC} = 5.0 \text{ volt} \pm 5\%$, $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min.	Typ	Max.	Unit
Frequency of Operation	f	0.1	—	1.0	MHz
Clock Timing for 1-MHz Operation (Figure 1) ($C_{\text{clock}} = 200 \text{ pF}$) Cycle Time	t_{cyc}	1.0	—	10	μs
Clock Pulse Width (Measured at $V_{CC} - 0.3 \text{ V}$) $\phi 1$ $\phi 2$	$PW_{\phi H}$	430 450	— —	4500 4500	ns
Total $\phi 1$ and $\phi 2$ UP Time	t_{ut}	940	—	—	ns
Rise and Fall Times $\phi 1, \phi 2$ (Measured between 0.3 V and $V_{CC} - 0.3 \text{ V}$)	t_r, t_f	5.0	—	50	ns
Delay Time or Clock Overlap (Measured at 0.5 V)	t_d	0	—	9100	ns
Overshoot/Undershoot Duration	t_{os}	0	—	40	ns

READ/WRITE TIMING

Figures 2 and 3, $f = 1.0 \text{ MHz}$, Loading = 130 pF and one TTL Load except VMA and BA Loading = 30 pF and one

Characteristic	Symbol	Min.	Typ	Max.	Unit
Read/Write Setup Time from MPU	T_{ASR}	—	100	300	ns
Address Setup Time from MPU	T_{ASC}	—	200	300	ns
Memory Read Access Time $t_{\text{cyc}} - (T_{\text{ASC}} + T_{\text{DSU}} + t_r)$	T_{ACC}	—	—	575	ns
Data Setup Time	T_{DSU}	100	—	—	ns
Address Setup Time from MPU for VMA	T_{VSC}	—	150	300	ns
Data Hold Time	T_{H}	10	30	—	ns
Enable High Time for DBE Input	T_{EH}	470	—	—	ns
Data Setup Time from MPU	T_{ASD}	—	150	200	ns

FIGURE 1 – CLOCK TIMING WAVEFORM

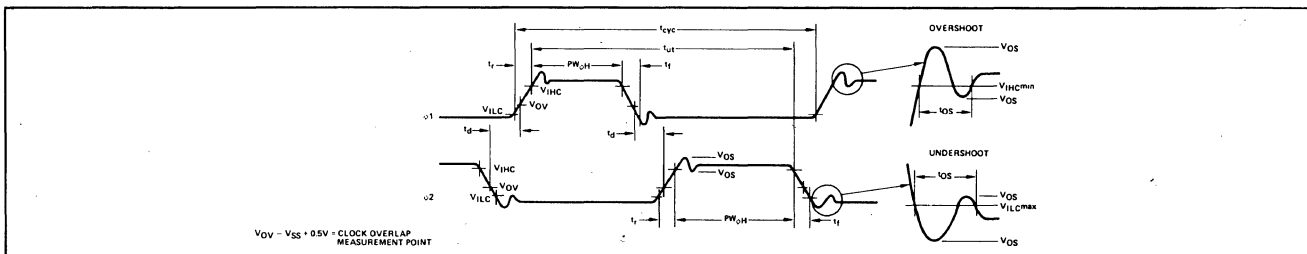


FIGURE 2 – READ DATA FROM MEMORY OR PERIPHERALS

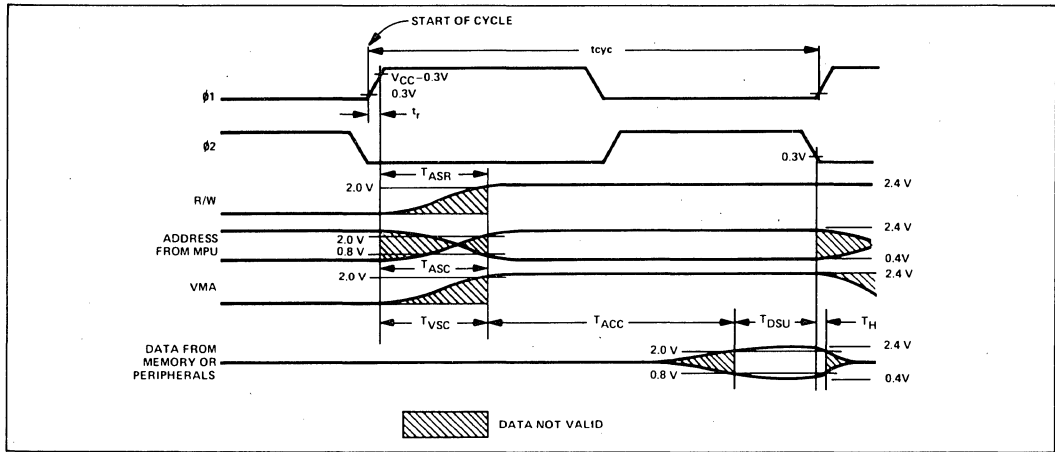
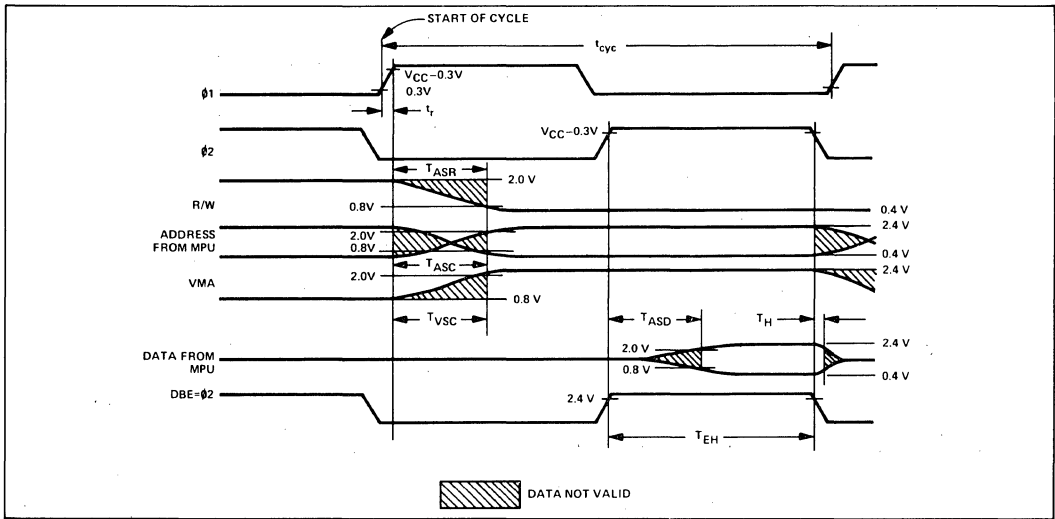


FIGURE 3 – WRITE DATA IN MEMORY OR PERIPHERALS



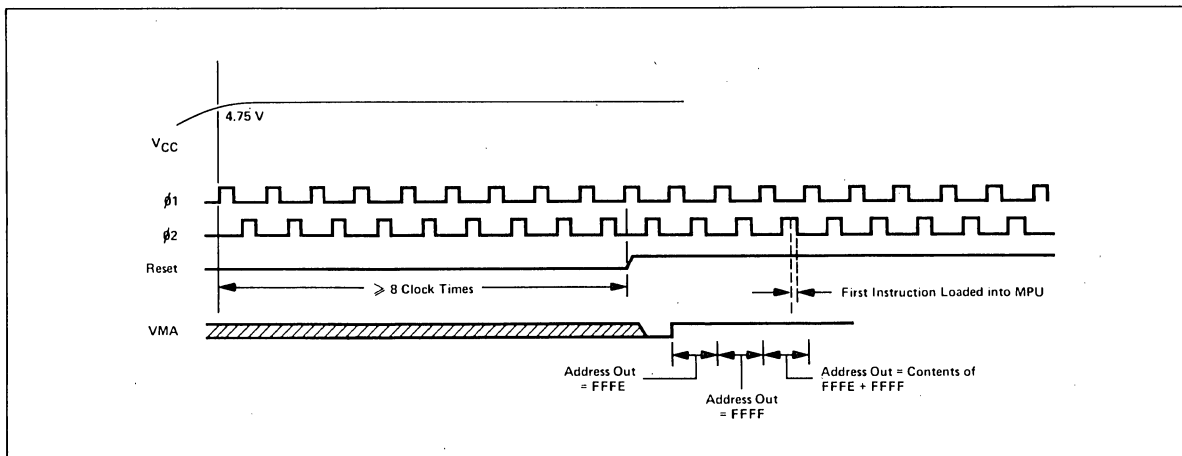
INTERFACE DESCRIPTION

Pin	Label	Function
phi1	(3)	Clocks Phase One and Phase Two – Two pins are used for a two-phase non-overlapping clock that runs at the VCC voltage level.
phi2	(37)	
RESET	(40)	Reset – This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start-up of the processor. If a positive edge is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by IRQ.

Reset – This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start-up of the processor. If a positive edge is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by IRQ.

Reset must be held low for at least eight clock periods after VCC reaches 4.75 volts (Figure 4). If Reset goes high prior to the leading edge of phi2, on the next phi1 the first restart memory vector address (FFFE) will appear on the address lines. This location should contain the higher order eight bits to be stored into the program counter. Following, the next address FFFF should contain the lower order eight bits to be stored into the program counter.

FIGURE 4 INITIALIZATION OF MPU AFTER RESTART



INTERFACE DESCRIPTION (CONT'D)

Pin	Label	Function
VMA	(5)	Valid Memory Address – This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 30 pF may be directly driven by this active high signal.
A0 • • • A15	(9) (25)	Address Bus – Sixteen pins are used for the address bus. The outputs are three-state bus drivers capable of driving one standard TTL load and 130 pF. When the output is turned off, it is essentially an open circuit. This permits the MPU to be used in DMA applications.
TSC	(39)	Three-State Control – This input causes all of the address lines and the Read/Write line to go into the off or high impedance state. This state will occur 500 ns after TSC = 2.4 V. The Valid Memory Address and Bus Available signals will be forced low. The data bus is not affected by TSC and has its own enable (Data Bus Enable). In DMA applications, the Three-State Control line should be brought high on the leading edge of the Phase One Clock. The phi1 clock must be held in the high state and the phi2 in the low state for this function to operate properly. The address bus will then be available for other devices to directly address memory. Since the MPU is a dynamic device, it can be held in this state for only 5.0 μs or destruction of data will occur in the MPU.
D0 • • D7	(33) (26)	Data Bus – Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. It also has three-state output buffers capable of driving one standard TTL load at 130 pF.
DBE	(36)	Data Bus Enable – This input is the three-state control signal for the MPU data bus and will enable the bus drivers when in the high state. This input is TTL compatible; however in normal operation, it can be driven by the phase two clock. During an MPU read cycle, the data bus drivers will be disabled internally. When it is desired that another device control the data bus such as in Direct Memory Access (DMA) applications, DBE should be held low.
R/W	(34)	Read/Write – This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high). Three-State Control going high will turn Read/Write to the off (high-impedance) state. Also, when the processor is halted, it will be in the off state. This output is capable of driving one standard TTL load and 130 pF.

INTERFACE DESCRIPTION (CONT'D)

Pin	Label	Function
$\overline{\text{HALT}}$	(2)	<p>$\overline{\text{Halt}}$ – When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be at a one level, Valid Memory Address will be at a zero, and all other three-state lines will be in the three-state mode.</p> <p>Transition of the $\overline{\text{Halt}}$ line must not occur during the last 250 ns of phase one. To insure single instruction operation, the $\overline{\text{Halt}}$ line must go high for one Phase One Clock cycle.</p>
BA	(7)	<p>Bus Available – The Bus Available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the $\overline{\text{Halt}}$ line is in the low state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit I = 0) or nonmaskable interrupt. This output is capable of driving one standard TTL load and 30 pF.</p>
$\overline{\text{IRQ}}$	(4)	<p>Interrupt Request – This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory.</p> <p>The $\overline{\text{Halt}}$ line must be in the high state for interrupts to be recognized.</p> <p>The $\overline{\text{IRQ}}$ has a high impedance pullup device internal to the chip; however a 3 kΩ external resistor to VCC should be used for wire-OR and optimum control of interrupts.</p>
$\overline{\text{NMI}}$	(6)	<p>Non-Maskable Interrupt – A low-going edge on this input requests that a non-mask interrupt sequence be generated within the processor. As with the $\overline{\text{Interrupt Request}}$ signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{\text{NMI}}$ signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{\text{NMI}}$. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away in the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a non-maskable interrupt routine in memory.</p> <p>$\overline{\text{NMI}}$ has a high impedance pullup resistor internal to the chip; however a 3 kΩ external resistor to VCC should be used for wire-OR and optimum control of interrupts.</p> <p>Inputs $\overline{\text{IRQ}}$ and $\overline{\text{NMI}}$ are hardware interrupt lines that are acknowledged during ϕ_2 and will start the interrupt routine on the ϕ_1 following the completion of an instruction.</p> <p>INTERRUPTS – As outlined in the interface description the S6800 requires a 16-bit vector address to indicate the location of routines for Restart, Non-maskable Interrupt, and Maskable Interrupt. Additionally an address is required for the Software Interrupt Instruction (SWI). The processor assumes the uppermost eight memory locations, FFF8 – FFFF, are assigned as interrupt vector addresses as defined in Figure 5.</p> <p>After completing the current instruction execution the processor checks for an allowable interrupt request via the $\overline{\text{IRQ}}$ or $\overline{\text{NMI}}$ inputs as shown by the simplified flow chart in Figure 6. Recognition of either external interrupt request or a Wait for Interrupt (WAI) or Software Interrupt (SWI) instruction causes the contents of the Index Register, Program Counter, Accumulators and Condition Code Register to be transferred to the stack as shown in Figure 7.</p>

FIGURE 5 MEMORY MAP FOR INTERRUPT VECTORS

Vector		Description
MS	LS	
FFFE	FFFF	Restart
FFFC	FFFD	Non-maskable Interrupt
FFFA	FFFB	Software Interrupt
FFF8	FFF9	Interrupt Request

FIGURE 6 – MPU FLOW CHART

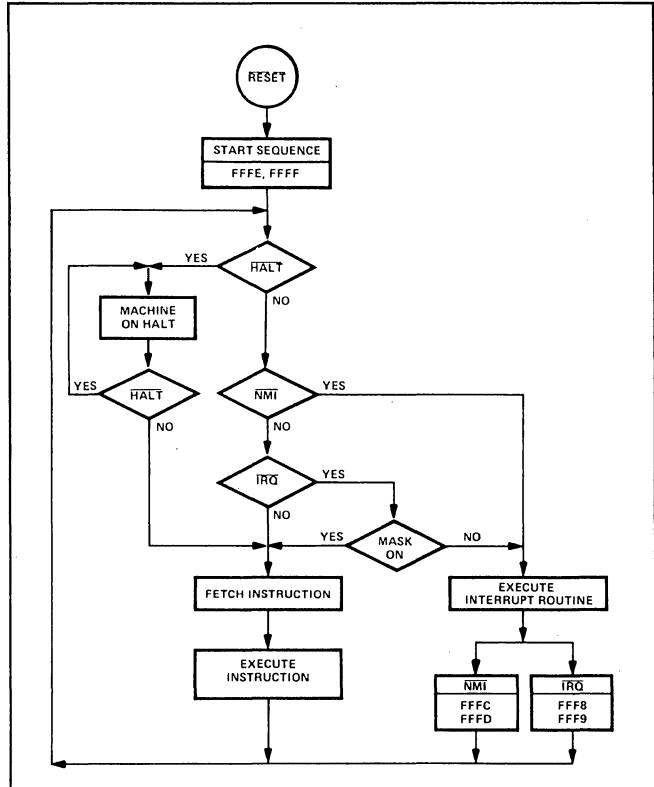


FIGURE 7 – SAVING THE STATUS OF THE MICROPROCESSOR IN THE STACK

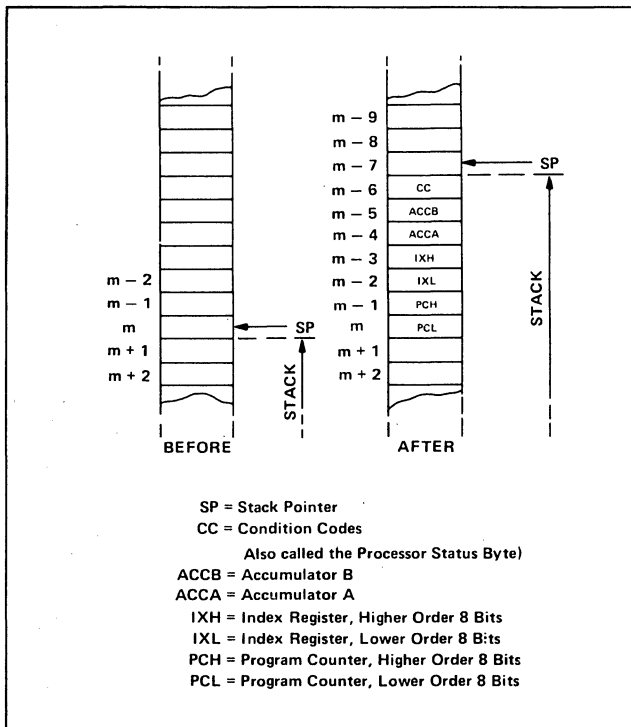
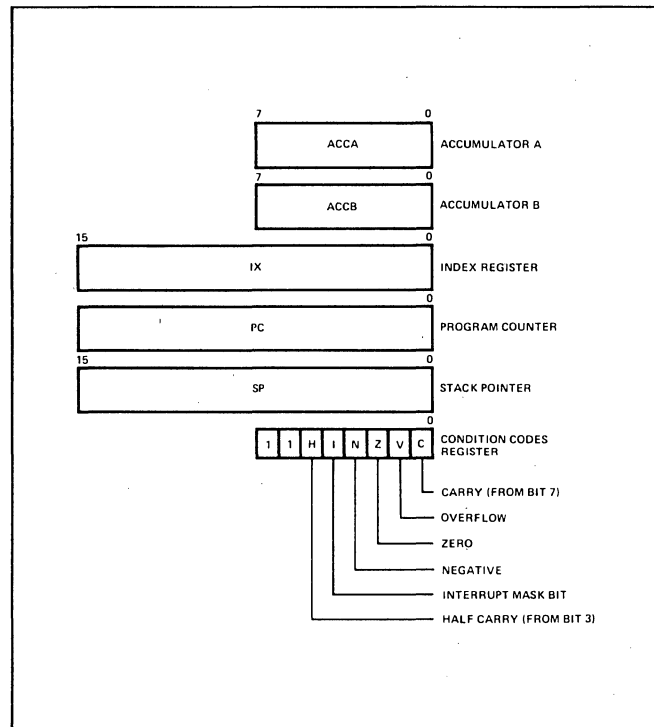


FIGURE 8 – PROGRAMMING MODEL OF THE MICROPROCESSOR



MPU REGISTERS

The MPU has three 16-bit registers and three 8-bit registers available for use by the programmer.

Program Counter – The program counter is a two byte (16-bits) register that points to the current program address.

Stack Pointer – The stack pointer is a two byte register that contains the address of the next available location in an external push-down/pop-up stack. This stack is normally a random access Read/Write memory that may have any location (address) that is convenient. In those applications that require storage of information in the stack when power is lost, the stack must be non-volatile.

Index Register – The index register is a two byte register that is used to store data or a sixteen bit memory address for the Indexed mode of memory addressing.

Accumulators – The MPU contains two 8-bit accumulators that are used to hold operands and results from the arithmetic logic unit (ALU).

Condition Code Register – The condition code register indicates the results of an Arithmetic Logic Unit operation: Negative (N), Zero (Z), Overflow (V), Carry from bit 7 (C), and half carry from bit 3 (H). These bits of the Condition Code Register are used as testable conditions for the conditional branch instructions. Bit 4 is the interrupt mask bit (I). The unused bits of the Condition Code Register (b6 and b7) are ones.

MPU ADDRESSING MODES

The S6800 eight-bit microprocessing unit has seven address modes that can be used by a programmer, with the addressing mode a function of both the type of instruction and the coding within the instruction. A summary of the addressing modes for a particular instruction can be found in Figure 9 along with the associated instruction execution time that is given in machine cycles. With a clock frequency of 1 MHz, these times would be microseconds.

ACCUMULATOR ADDRESSING (ACCX)

OP CODE

A single byte instruction addressing operands only in accumulator A or accumulator B.

IMPLIED ADDRESSING

OP CODE

Single byte instruction where the operand address is implied by the instruction definition (i.e., Stack Pointer, Index Register or Condition Register).

IMMEDIATE ADDRESSING

OP CODE	IMMEDIATE OPERAND
HIGHER	IMMEDIATE OPERAND LOWER

Two or three byte instructions with an eight or sixteen bit operand respectively. For accumulator operations the eight bit operand is contained in the second byte of a two byte instruction. For Index Register operations (e.g. LDX) sixteen bit operand is contained in the second and third byte of a three byte instruction.

DIRECT ADDRESSING

OP CODE	ADDRESS 0-255
---------	------------------

Two byte instructions with the address of the operand contained in the second byte of the instruction. This format allows direct addressing of operands within the first 256 memory locations.

EXTENDED ADDRESSING

OP CODE	ADDRESS HIGHER	ADDRESS LOWER
---------	-------------------	------------------

Three byte instructions with the higher eight bits of the operand address contained in the second byte and the lower eight bits of address contained in the third byte of the instruction. This format allows direct addressing of all 65,536 memory locations.

INDEXED ADDRESSING

OP CODE	INDEX ADDRESS
---------	------------------

Two byte instructions where the 8 bit unsigned address contained in the second byte of the instruction is added to the sixteen bit Index Register resulting in a sixteen bit effective address. The effective address is stored in a temporary register and the contents of the Index Register are unchanged.

RELATIVE ADDRESSING

OP CODE	RELATIVE ADDRESS
---------	---------------------

Two byte instructions where the relative address contained in the second byte of the instruction is added to the sixteen bit program counter plus two. The relative address is interpreted as a two's complement number allowing relative addressing within a range of -125 to +129 bytes of the present instruction.

FIGURE 9 - S6800 INSTRUCTION SET

Instruction	Mnemonic	Addressing Mode						Boolean/Arith Operation	Condition Reg																	
		Implied		Immediate		Direct			Extended		Indexed		Relative													
		OP	MC	PB	OP	MC	PB		OP	MC	PB	OP	MC	PB	OP	MC	PB	OP	MC	PB	H	I	N	Z	V	C
Load accumulator	LDAA				86	2	2	96	3	2	B6	4	3	A6	5	2										
	LDAB				C6	2	2	D6	3	2	F6	4	3	E6	5	2										
Load stack pointer	LDS				8E	3	3	9E	4	2	BE	5	3	AE	6	2										
Load index register	LDX				CE	3	3	DE	4	2	FE	5	3	EE	6	2										
Store accumulator	STAA							97	4	2	B7	5	3	A7	6	2										
	STAB							D7	4	2	F7	5	3	E7	6	2										
Store stack pointer	STS							9F	5	2	BF	6	3	AF	7	2										
Store index register	STX							DF	5	2	FF	6	3	EF	7	2										
Transfer accumulators	TAB	16	2	1																						
	TBA	17	2	1																						
Transfer Acc. to cond. reg.	TAP	06	2	1																						
Transfer cond. reg. to Acc.	TPA	07	2	1																						
Transfer stk ptr to index	TSX	30	4	1																						
Transfer index to stk ptr	TXS	35	4	1																						
Full data	PULA	32	4	1																						
	PULB	33	4	1																						
Push data	PSHA	36	4	1																						
	PSHB	37	4	1																						
Add accumulators	ABA	1B	2	1																						
Add	ADDA				8B	2	2	9B	3	2	BB	4	3	AB	5	2										
	ADDB				CB	2	2	DB	3	2	FB	4	3	EB	5	2										
Add with carry	ADCA	89	2	2	89	2	2	99	3	2	B9	4	3	A9	5	2										
	ADCB	C9	2	2	C9	2	2	D9	3	2	F9	4	3	E9	5	2										
Subtract accumulators	SBA	10	2	1																						
Subtract	SUBA				80	2	2	90	3	2	B0	4	3	A0	5	2										
	SUBB				C0	2	2	D0	3	2	F0	4	3	E0	5	2										
Subtract with carry	SBCA				82	2	2	92	3	2	B2	4	3	A2	5	2										
	SBCB				C2	2	2	D2	3	2	F2	4	3	E2	5	2										
Increment	INCA	4C	2	1																						
	INCB	5C	2	1																						
	!INC										7C	6	3	6C	7	2										
Increment stack pointer	INS	31	4	1																						
Increment index reg.	INX	08	4	1																						
Decrement	DECA	4A	2	1																						
	DECB	5A	2	1																						
	DEC										7A	6	3	6A	7	2										
Decrement stack pointer	DES	34	4	1																						
Decrement index register	DEX	09	4	1																						
Complement (1's)	COMA	43	2	1																						
	COMB	53	2	1																						
	COM										73	6	3	63	7	2										
Complement (2's)	NEGA	40	2	1																						
	NEGB	50	2	1																						
	NEG										70	6	3	60	7	2										
Decimal adjust accumulator	DAA	19	2	1																						

OP = Operation Code

MC = Number of MPU Cycles

PB = Number of Program Bytes

FIGURE 9 S6800 INSTRUCTION SET (CONT'D)

Instruction	Mnemonic	Addressing Mode							Boolean/Arith	Condition Reg																		
		Implied		Immediate		Direct		Extended			Indexed		Relative															
		OP	MC	PB	OP	MC	PB	OP	MC	PB	OP	MC	PB	OP	MC	PB	OP	MC	PB	Operation	H	I	N	Z	V	C		
Logical and	ANDA				84	2	2	94	3	2	B4	4	3	A4	5	2					A • M → A	•	•	•	•	R	•	
	ANDB				C4	2	2	D4	3	2	F4	4	3	E4	5	2					B • M → B	•	•	•	•	R	•	
Inclusive or	ORAA				8A	2	2	9A	3	2	BA	4	3	AA	5	2					A + M → A	•	•	•	•	R	•	
	ORAB				CA	2	2	DA	3	2	FA	4	3	EA	5	2					B + M → B	•	•	•	•	R	•	
Exclusive or	EORA				88	2	2	98	3	2	B8	4	3	A8	5	2					A ⊕ M → A	•	•	•	•	R	•	
	EORB				C8	2	2	D8	3	2	F8	4	3	E8	5	2					B ⊕ M → B	•	•	•	•	R	•	
Shift left arithmetic	ASLA	48	2	1																		•	•	•	•	6	•	
	ASLB	58	2	1																		•	•	•	•	6	•	
	ASL										78	6	3	68	7	2						•	•	•	•	6	•	
Shift right arithmetic	ASRA	47	2	1																		•	•	•	•	6	•	
	ASRB	57	2	1																		•	•	•	•	6	•	
	ASR										77	6	3	67	7	2						•	•	•	•	6	•	
Shift right logical	LSRA	44	2	1																		•	•	•	•	6	•	
	LSRB	54	2	1																		•	•	•	•	6	•	
Rotate left	ROLA	49	2	1																		•	•	•	•	6	•	
	ROLB	59	2	1																		•	•	•	•	6	•	
Rotate right	ROL										79	6	3	69	7	2						•	•	•	•	6	•	
	RORA	46	2	1																		•	•	•	•	6	•	
RORB	56	2	1																	•	•	•	•	6	•			
ROR										76	6	3	66	7	2					•	•	•	•	6	•			
Compare accumulators	CBA	11	2	1																	A - B	•	•	•	•	•	•	
Compare	CMPA				81	2	2	91	3	2	B1	4	3	A1	5	2					A - M	•	•	•	•	•	•	
	CMPB				C1	2	2	D1	3	2	F1	4	3	E1	5	2					B - M	•	•	•	•	•	•	
Compare index register	CPX				8C	3	3	9C	4	2	BC	5	3	AC	6	2					X _H - M, X _L - (M+1)	•	•	7	•	•	8	•
Test (zero or minus)	TSTA	4D	2	1																	A - 00	•	•	•	•	R	R	
	TSTB	5D	2	1																	B - 00	•	•	•	•	R	R	
	TST										7D	6	3	6D	7	2					M - 00	•	•	•	•	R	R	
Bit test	BITA				85	2	2	95	3	2	B5	4	3	A5	5	2					A • M	•	•	•	•	R	•	
	BITB				C5	2	2	D5	3	2	F5	4	3	E5	5	2					B • M	•	•	•	•	R	•	
TEST																				TEST	•	•	•	•	•	•		
Branch	BRA																20	4	2		•	•	•	•	•	•		
Branch if carry clear	BCC																24	4	2		C = 0	•	•	•	•	•	•	
Branch if carry set	BCS																25	4	2		C = 1	•	•	•	•	•	•	
Branch if overflow clear	BVC																28	4	2		V = 0	•	•	•	•	•	•	
Branch if overflow set	BVS																29	4	2		V = 1	•	•	•	•	•	•	
Branch if equal to zero	BEQ																27	4	2		Z = 1	•	•	•	•	•	•	
Branch if greater or equal to zero	BGE																2C	4	2		N ⊕ V = 0	•	•	•	•	•	•	
Branch if greater than zero	BGT																2E	4	2		Z + (N ⊕ V) = 0	•	•	•	•	•	•	
Branch if less than zero	BLT																2D	4	2		N ⊕ V = 1	•	•	•	•	•	•	
Branch if less than or equal to zero	BLE																2F	4	2		Z + (N ⊕ V) = 1	•	•	•	•	•	•	
Branch if not equal to zero	BNE																26	4	2		Z = 0	•	•	•	•	•	•	
Branch if minus	BMI																2B	4	2		N = 1	•	•	•	•	•	•	
Branch if plus	BPL																2A	4	2		N = 0	•	•	•	•	•	•	
Branch if higher	BHI																22	4	2		C + Z = 0	•	•	•	•	•	•	
Branch if lower or same	BLS																23	4	2		C + Z = 1	•	•	•	•	•	•	

OP = Operation Code

MC = Number of MPU Cycles

PB = Number of Program Bytes

FIGURE 9 S6800 INSTRUCTION SET (CONT'D)

Instruction	Mnemonic	Addressing Modes						Boolean/Arith Operation	Condition Reg.														
		Implied		Direct		Immediate			Extended		Indexed		Relative		5	4	3	2	1	0			
		OP	MC	PB	OP	MC	PB		OP	MC	PB	OP	MC	PB	OP	MC	PB	H	I	N	Z	V	C
Branch to subroutine	BSR												8D	8	2								
Jump to subroutine	JSR						BD	9	3				AD	8	2								
Jump	JMP						7E	3	3				6E	4	2								
Return from subroutine	RTS	39	5	1																			
Return from interrupt	RTI	3B	10	1																			
Software interrupt	SWI	3F	12	1																			
Wait for interrupt	WAI	3E	9	1																			
No operation	NOP	02	2	1																			
Clear	CLRA	4F	2	1																			
	CLRB	5F	2	1																			
	CLR						7F	6	3				6F	7	2								
Clear carry	CLC	0C	2	1																			
Clear interrupt mask	CLI	0E	2	1																			
Clear overflow	CLV	0A	2	1																			
Set carry	SEC	0D	2	1																			
Set interrupt mask	SEI	0F	2	1																			
Set overflow	SEV	0B	2	1																			

CONDITION CODE SYMBOLS:

- H Half-carry from bit 3;
- I Interrupt mask
- N Negative (sign bit)
- Z Zero (byte)
- V Overflow, 2's complement
- C Carry from bit 7
- R Reset Always
- S Set Always
- ‡ Test and set if true, cleared otherwise
- Not Affected

LEGEND:

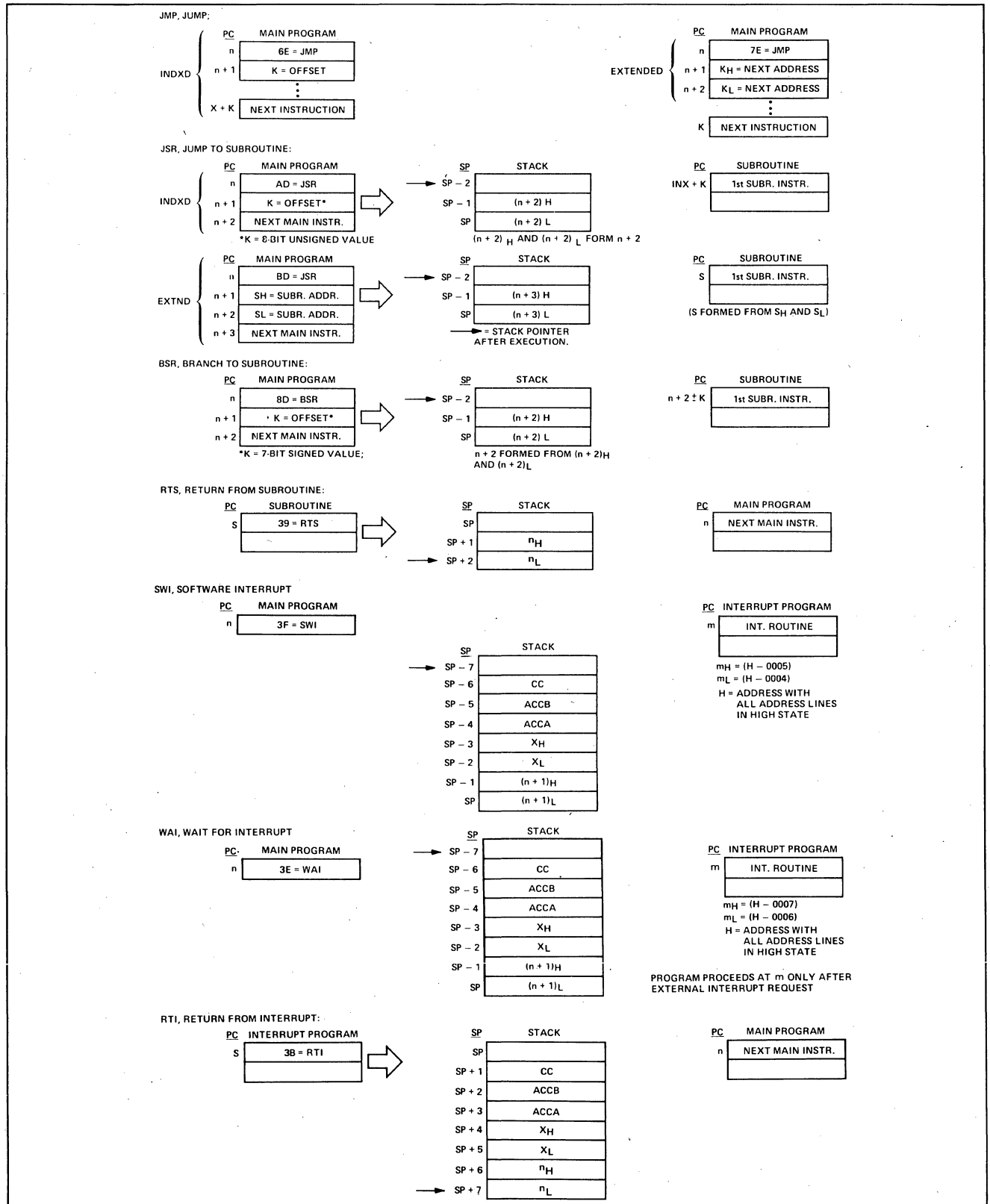
- OP Operation Code (Hexadecimal);
- MC Number of MPU Cycles;
- PB Number of Program Bytes;
- + Arithmetic Plus;
- Arithmetic Minus;
- Boolean AND;
- M_{SP} Contents of memory location pointed to by Stack Pointer;
- + Boolean Inclusive OR;
- ⊕ Boolean Exclusive OR;
- M Complement of M;
- Transfer Into;
- 0 Bit = Zero;
- 00 Byte = Zero;

Note - Accumulator addressing mode instructions are included in the IMPLIED addressing.

CONDITION CODE REGISTER NOTES:

- (Bit set if test is true and cleared otherwise)
- 1 (Bit V) Test: Result = 10000000?
- 2 (Bit C) Test: Result = 00000000?
- 3 (Bit C) Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.)
- 4 (Bit V) Test: Operand = 10000000 prior to execution?
- 5 (Bit V) Test: Operand = 01111111 prior to execution?
- 6 (Bit V) Test: Set equal to result of N * C after shift has occurred.
- 7 (Bit N) Test: Sign bit of most significant (MS) byte = 1?
- 8 (Bit V) Test: 2's complement overflow from subtraction of MS bytes?
- 9 (Bit N) Test: Result less than zero? (Bit 15 = 1)
- 10 (All) Load Condition Code Register from Stack. (See Special Operations)
- 11 (Bit I) Set when interrupt occurs, if previously set, a Non-Maskable Interrupt is required to exit the wait state.
- 12 (All) Set according to the contents of Accumulator A

SPECIAL OPERATIONS



SYSTEMS OPERATION

To demonstrate the great versatility of the functional building block concept, a typical system configuration is shown. This configuration will demonstrate how easily a basic system may be upgraded and expanded for a number of different applications.

The Microprocessing Unit (MPU) may be configured with a Read Only Memory (ROM), Random Access Memory (RAM), a Peripheral Interface Adapter (PIA), restart circuitry and clock circuitry to form a minimum functional system (Figure 10). Such a system can easily be adapted for a number of small scale applications by simply changing the content of the ROM.

TWO-PHASE CLOCK CIRCUITRY AND TIMING—The MPU requires a two-phase non-overlapping clock which has a frequency range as high as 1 MHz. In addition to the two phases, this circuit should also generate an enable signal E, and its complement \bar{E} , to enable ROMs, RAMs, PIAs and ACIAs. This Enable signal and its complement is obtained by ANDing $\phi 2$ and VMA (Valid Memory Address).

CHIP SELECTION AND ADDRESSING—The minimum system configuration permits direct selection of the ROM, RAM, ACIA and PIA without the use of special TTL select logic. This is accomplished by simply wiring the address lines A13 and A14 to the Enable or chip select lines on the memories and PIA. This permits the devices to be addressed as follows:

Device	A14	A13	Hex Addresses
RAM	0	0	0000–007F
PIA	0	1	2004–2007 (Registers)
ROM	1	1	6000–63FF

Other addressing schemes can be utilized which use any combination of two of the lines A10 through A14 for chip selection.

PERIPHERAL CONTROL—All control and timing for the peripherals that are connected to the PIA is accomplished by software routines under the control of the MPU.

RESTART AND NON-MASKABLE INTERRUPT—Since this basic system does not have a nonvolatile RAM, special circuitry to handle loss of power using NMI is not required. Circuitry is, however, required to insure proper initialization of the MPU when power is turned on. This circuit should insure that the Restart signal is held low for eight $\phi 1$ clock cycles after the VCC power supply reaches a voltage of approximately 4.75 volts DC. Also, in order to insure that a PIA or ACIA is not inadvertently selected during the power-on sequence, Three-State Control (TSC) should be held high until the positive transition of Restart.

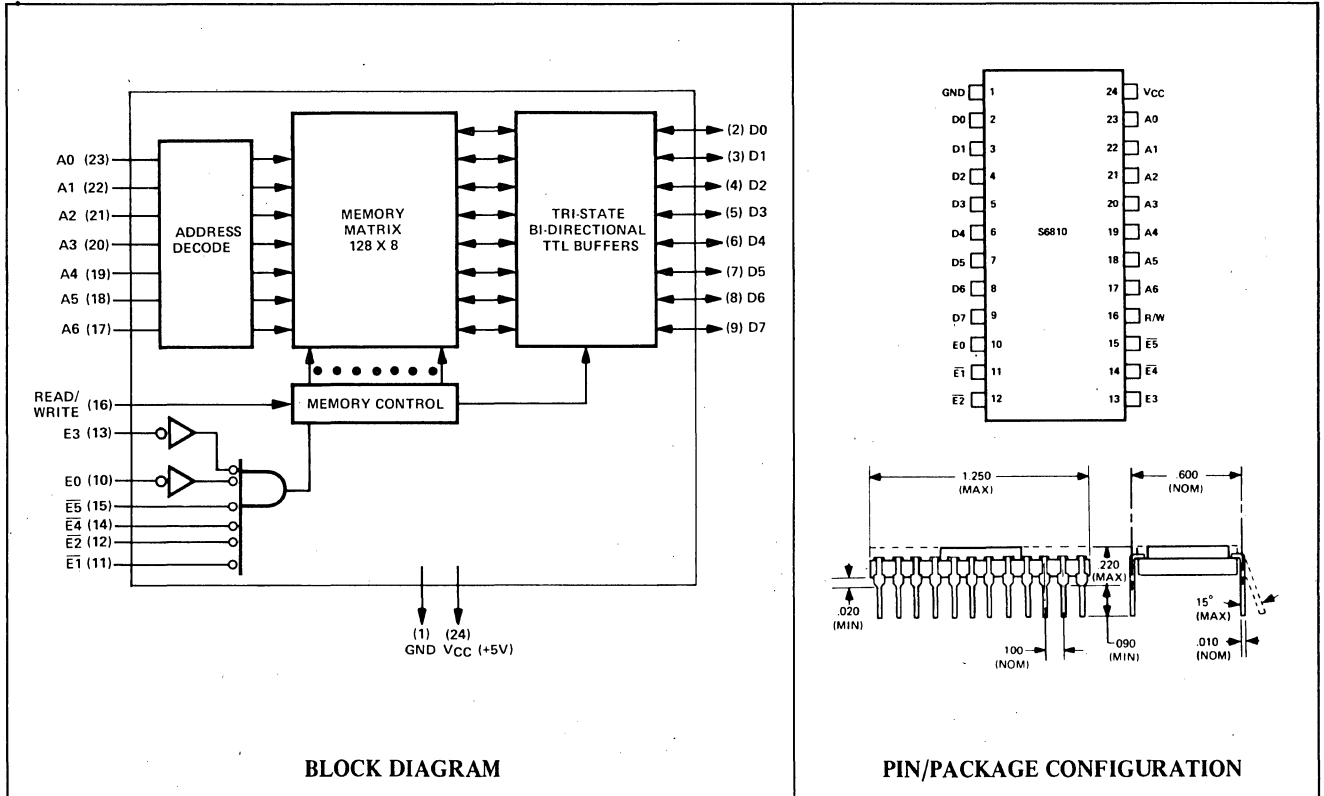
\bar{HALT} —The \bar{Halt} line is tied to VCC and will automatically place the MPU in the run state when power is turned on. This signal may be used to halt the MPU if a switch is used to tie the line to ground for HALT and to VCC for RUN.

S6810

128 x 8 STATIC
READ/WRITE MEMORY



ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM

PIN/PACKAGE CONFIGURATION

FEATURES

- Organized as 128 Bytes of 8 Bits
- Static Operation
- Bi-Directional Three-State Data Input/Output
- Six Chip Enable Inputs (Four Active Low, Two Active High)
- Single 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 1.0μs for S6810
575 ns for S6810-1

FUNCTIONAL DESCRIPTION

The S6810 is a static 128 x 8 Read/Write Memory designed and organized to be compatible with the S6800 Microprocessor. Interfacing to the S6810 consists of an 8 Bit Bi-directional Data Bus, Seven Address Lines, a single Read/Write

Control line, and six Chip Enable lines, four negative and two positive.

For ease of use, the S6810 is a totally static memory requiring no clocks or cell refresh. The S6810 is fabricated with N channel silicon gate technology to be fully DTL/TTL compatible with only a single +5 volt power supply required.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	-0.3 to +7.0V
Input Voltage V_{in}	-0.3 to +7.0V
Operating Temperature Range T_A	0 to +70°C
Storage Temperature Range T_{stg}	-55 to +150°C

DC (STATIC) CHARACTERISTICS

($V_{CC} = 5.0 \text{ Volt} \pm 5\%$; $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Condition
Input High Voltage (Normal Operating Levels)	V_{IH}	2.4	—	5.25	V	
Input Low Voltage (Normal Operating Levels)	V_{IL}	-0.3	—	0.4	V	
Input Current ($A_n, R/W, E_n, \bar{E}_n$) ($V_{in} = 0$ to 5.25 V)	I_{in}	—	—	2.5	μA	
Input High Threshold Voltage	V_{IHT}	2.0	—	—	V	
Input Low Threshold Voltage	V_{ILT}	—	—	0.8	V	
Output High Voltage ($I_{OH} = -100 \mu\text{A}$)	V_{OH}	2.4	—	—	V	
Output Low Voltage ($I_{OL} = 1.6 \text{ mA}$)	V_{OL}	—	—	0.4	V	
Output Leakage Current ($D0 - D7$) ($V_O = 2.4 \text{ V}, E = 0.4 \text{ V}, \bar{E} = 2.4 \text{ V}$)	I_{LIH}	—	—	10	μA	
Output Leakage Current ($D0 - D7$) ($V_O = 0.4 \text{ V}, E = 0.4 \text{ V}, \bar{E} = 2.4 \text{ V}$)	I_{LOL}	—	—	10	μA	
Supply Current ($V_{CC} = 5.25 \text{ V}, T_A = 0^\circ\text{C}$)	I_{CC}	—	—	130	mA	
Input Capacitance	C_{IN}	—	—	7.5	pF	$f = 1.0 \text{ MHz}, T_A = 25^\circ\text{C}$
Output Capacitance	C_{OUT}	—	—	15	pF	

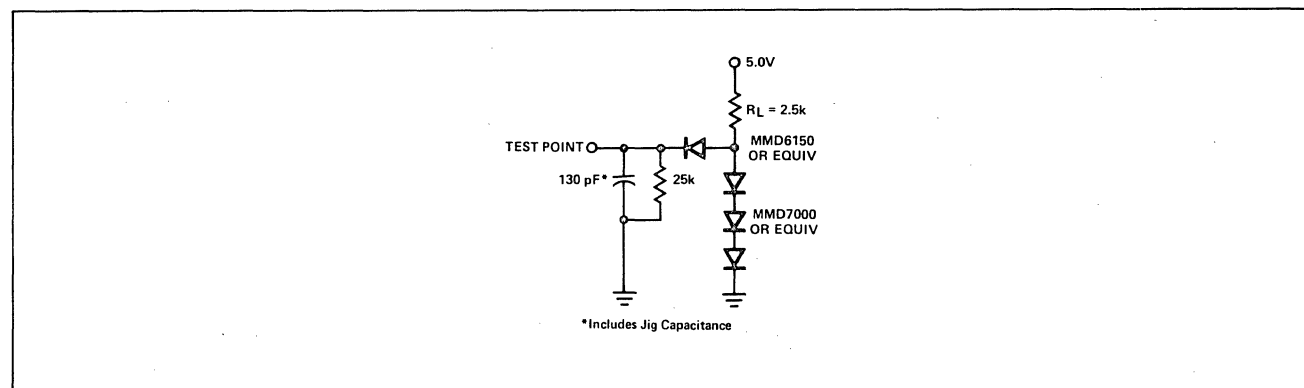
AC (DYNAMIC) CHARACTERISTICS

($V_{CC} = 5.0 \text{ Volt} \pm 5\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

Characteristic	Symbol	Min.	Max.	Unit
Address Setup Time	t_{AS}	30	—	ns
Address Hold Time	t_{AH}	0	—	ns
Chip Enable Pulse Width	t_{CS}	800 400	—	ns

S6810
S6810-1

FIGURE 1 – AC TEST LOAD



READ CYCLE

(All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

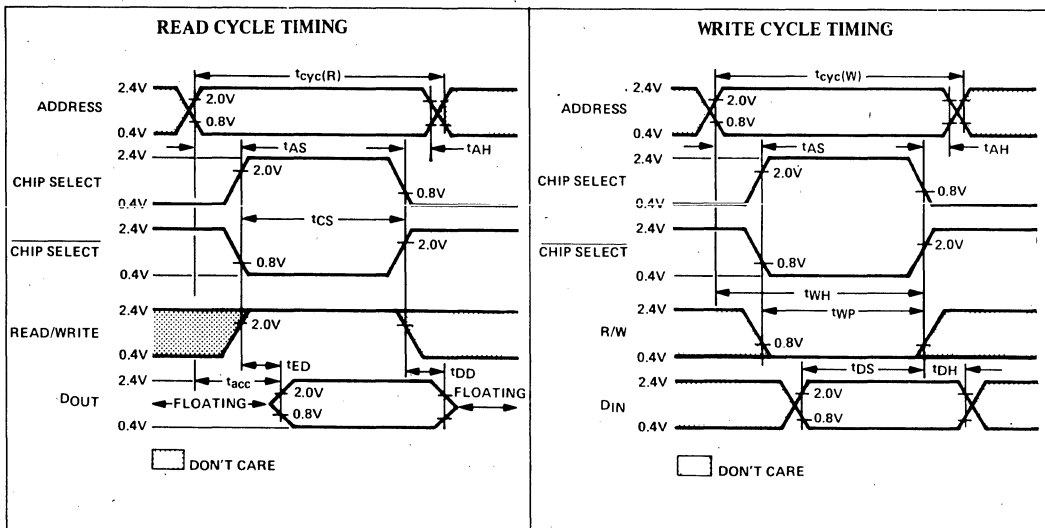
Characteristic	Symbol	Min.	Max.	Unit
Read Cycle Time	S6810	1000	—	ns
	S6810-1	575	—	ns
Output Enable Delay Time	S6810	—	400	ns
	S6810-1	—	300	ns
Output Disable Delay Time	S6810	10	200	ns
	S6810-1	10	150	ns
Read Access Time	S6810	—	1000	ns
	S6810-1	—	575	ns

WRITE CYCLE

(All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

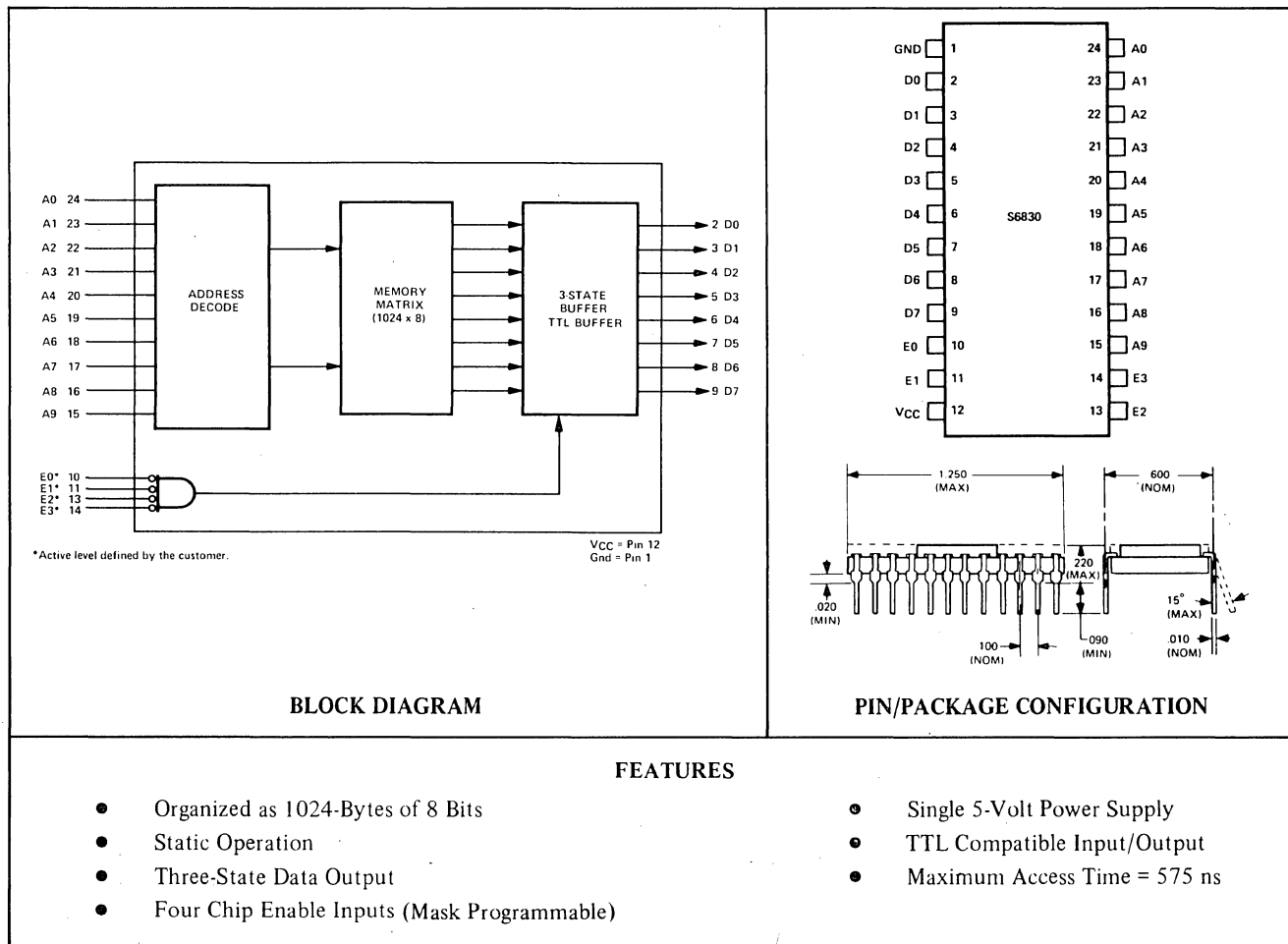
Characteristic	Symbol	Min.	Max.	Unit
Write Cycle Time	S6810	1000	—	ns
	S6810-1	500	—	ns
Write Pulse Width	S6810	800	—	ns
	S6810-1	400	—	ns
Write Pulse Hold Time	S6810	1000	—	ns
	S6810-1	500	—	ns
Data Setup Time	S6810	500	—	ns
	S6810-1	300	—	ns
Data Hold Time	S6810 S6810-1	0	—	ns

TIMING CHARACTERISTICS



MICROPROCESSOR AMI

ADVANCED PRODUCT DESCRIPTION



FUNCTIONAL DESCRIPTION

The S6830 is a mask programmable read only memory organized 1024 words x 8 bits for application in byte organized systems. The S6830 is totally bus compatible with the S6800 microprocessor. Interfacing to the S6830 consists

of an 8 bit three-state data bus, four mask programmable chip selects and ten address lines.

The S6830 is a totally static memory requiring no clocks. Access time is compatible with maximum data rates in a S6800 microprocessor system. The device operates from a single +5 volt power supply and is fabricated with N channel silicon gate technology.

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Supply Voltage V _{CC}	-0.3 to +7.0V
Input Voltage V _{in}	-0.3 to +7.0V
Operating Temperature Range T _A	0 to +70°C
Storage Temperature Range T _{stg}	-55 to +150°C

NOTE: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC (STATIC) CHARACTERISTICS

($V_{CC} = +5 \text{ Volt} \pm 5\%$; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$) **RECOMMENDED DC OPERATING CONDITIONS**

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage (Norm. Op. Levels)	V_{IH}	2.4	5.25	Vdc
Input Low Voltage (Norm. Op. Levels)	V_{IL}	-0.3	0.4	Vdc
Input Current ($V_{in} = 0$ to 5.25 V)	I_{in}	-	2.5	μA dc
Input High Threshold Voltage	V_{IHT}	2.0	-	Vdc
Input Low Threshold Voltage	V_{ILT}	-	0.65	Vdc
Output High Voltage ($I_{OH} = -100 \mu\text{A}$)	V_{OH}	2.4	-	Vdc
Output Low Voltage ($I_{OL} = 1.6 \text{ mA}$)	V_{OL}	-	0.45	Vdc
Output Leakage Current ($V_{OH} = 2.4 \text{ V}$, $E = 0.4 \text{ V}$, $\bar{E} = 2.4 \text{ V}$)	I_{LOH}	-	10	μA dc
Output Leakage Current ($V_{OH} = 0.4 \text{ V}$, $E = 0.4 \text{ V}$, $\bar{E} = 2.4 \text{ V}$)	I_{LOL}	-	10	μA dc
Supply Current ($V_{CC} @ 5.25\text{V}$, $T_A = 0^\circ\text{C}$)	I_{CC}	-	130	mAdc

CAPACITANCE

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Capacitance	C_{in}	-	-	7.5	pF	$f = 1.0 \text{ MHz}$ $T_A = 25^\circ\text{C}$
Output Capacitance	C_{out}	-	-	15	pF	

AC (DYNAMIC) CHARACTERISTICS READ CYCLE (All timing with $t_r = t_f = 20 \text{ ns}$, Load of Figure 1)

$V_{CC} = +5 \text{ Volt} \pm 5\%$; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$

Characteristic	Symbol	Min.	Max.	Unit
Read Cycle Time	$t_{cyc}(R)$	575	-	ns
Output Enable Delay Time	t_{ED}	-	300	ns
Output Disable Delay Time	t_{DD}	10	150	ns
Read Access Time	t_{acc}	-	575	ns

READ CYCLE TIMING

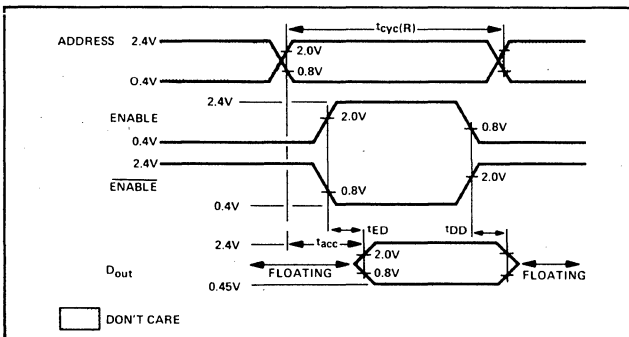
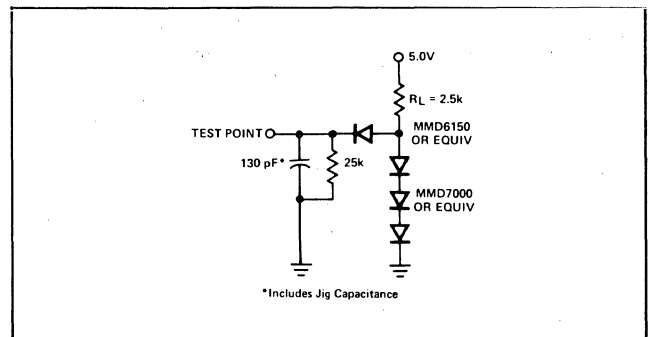
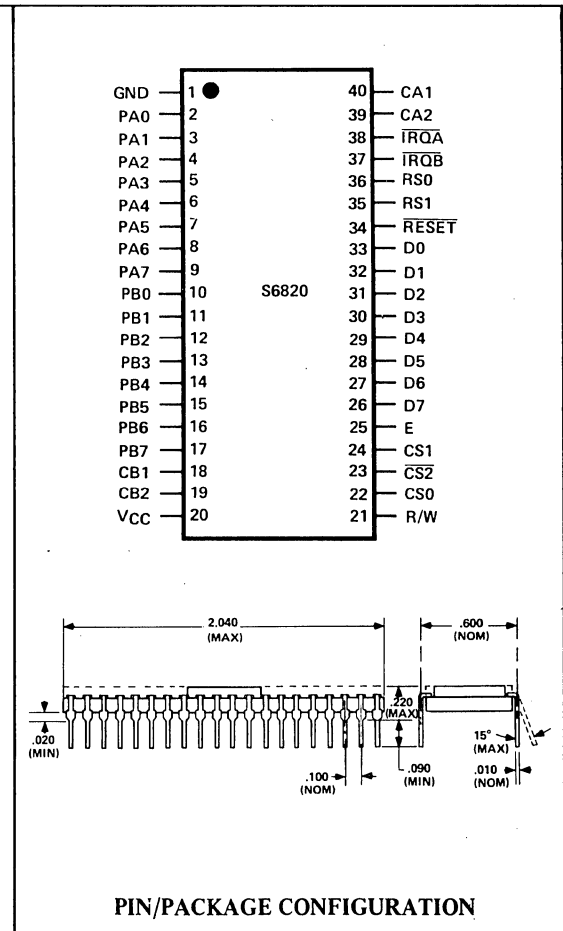
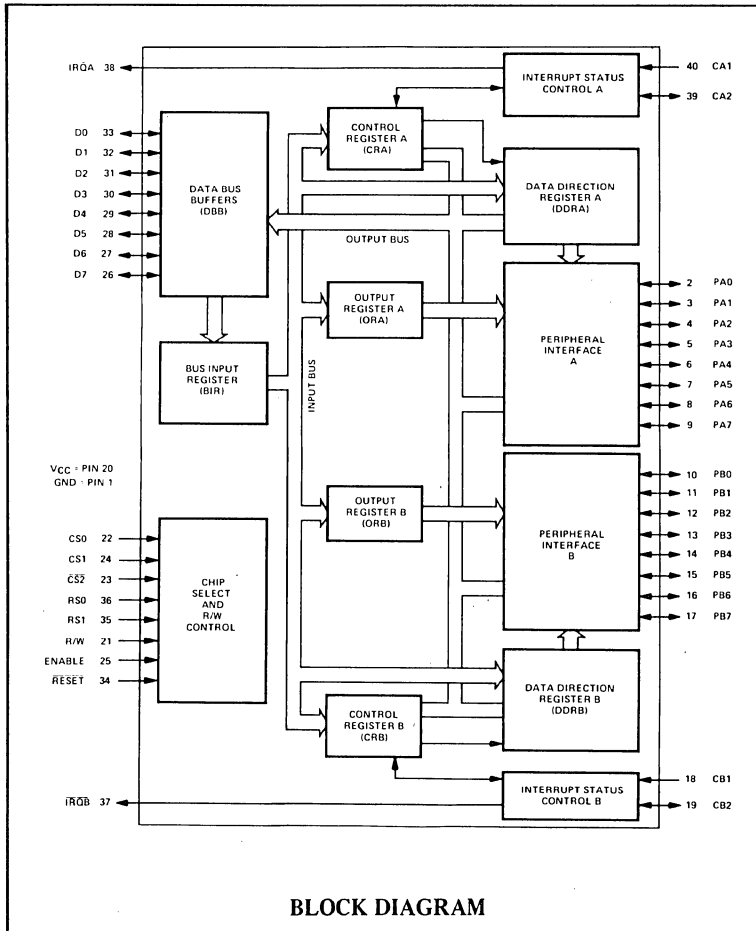


FIGURE 1 – AC TEST LOAD





FEATURES

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines; Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance 3-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Compatible Peripheral Lines

FUNCTIONAL DESCRIPTION

The S6820 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the S6800 Microprocessing Unit (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirec-

tional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and

FUNCTIONAL DESCRIPTION (CONT'D)

each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the over-all operation of the interface.

The PIA interfaces to the S6800 MPU with an eight-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals, in conjunction with the S6800 VMA output, permit the MPU to have complete control over the PIA. VMA may be utilized to gate the input signals to the PIA.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	-0.3 to +7.0V
Input Voltage V_{in}	-0.3 to +7.0V
Operating Temperature Range T_A	0 to +70°C
Storage Temperature Range T_{stg}	-55 to +150°C

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC (STATIC) CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$, $T_A = 25^\circ C$ unless otherwise noted.)

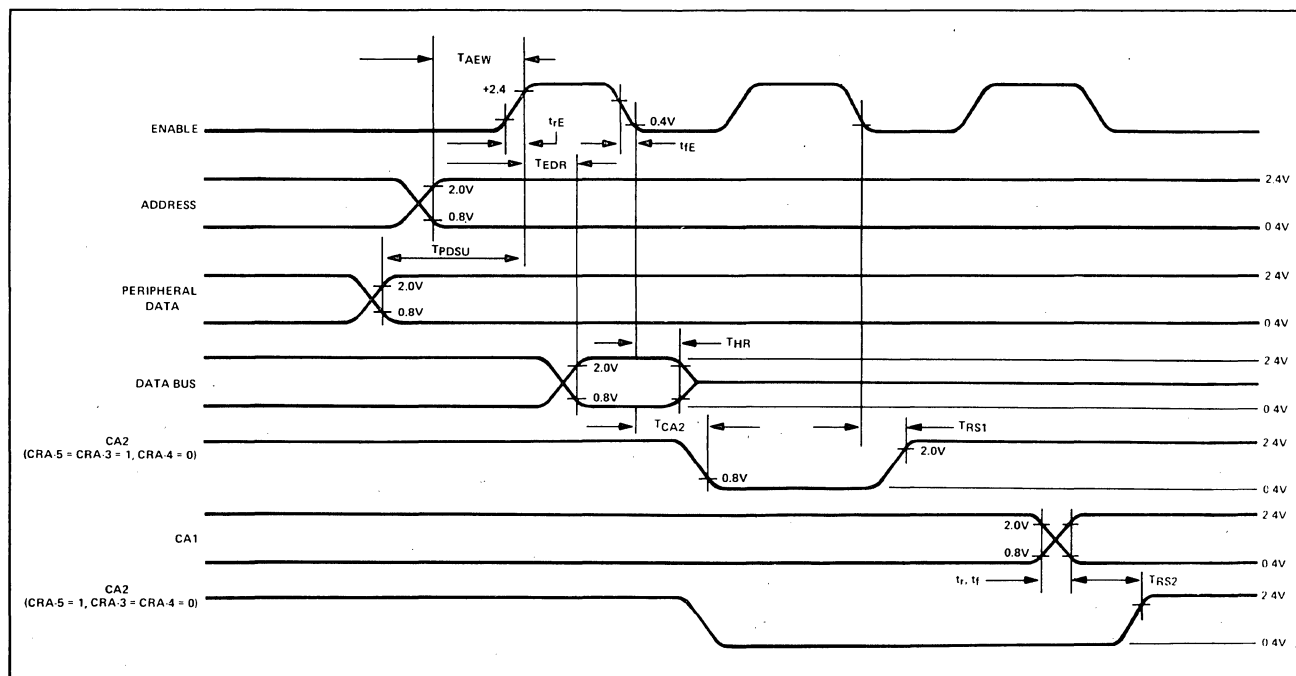
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.4	-	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	-0.3	-	+0.4	Vdc
Input High Threshold Voltage All Inputs Except Enable	V_{IHT}	+2.0	-	-	Vdc
Input Low Threshold Voltage All Inputs Except Enable	V_{ILT}	-	-	+0.8	Vdc
Input Leakage Current ($V_{in} = 0$ to 5.0 Vdc) R/W, \overline{Reset} , $\overline{RS0}$, $\overline{RS1}$, $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, CA1, CB1, Enable	I_{in}	-	1.0	2.5	μA_{dc}
Three-State (Off State) Input Current ($V_{in} = 0.4$ to 2.4 Vdc, $V_{CC} = \max$) D0-D7, PB0-PB7, CB2	I_{TSI}	-	2.0	10	μA_{dc}
Input High Current ($V_{IH} = 2.4$ Vdc) PA0-PA7, CA2	I_{IH}	100	250	-	μA_{dc}
Input Low Current ($V_{IL} = 0.4$ Vdc) PA0-PA7, CA2	I_{IL}	-	1.0	1.6	mAdc
Output High Voltage ($V_{CC} = \min$, $I_{Load} = -100 \mu A_{dc}$, Enable Pulse Width < 25 μs)	V_{OH}	+2.4	-	-	Vdc
Output Low Voltage ($V_{CC} = \min$, $I_{Load} = 1.6$ mAdc)	V_{OL}	-	-	+0.4	Vdc
Output High Current (Sourcing) ($V_{OH} = 2.4$ Vdc) ($V_{OH} = 1.5$ Vdc, the current for driving other than TTL, e.g., Darlington Base) PB0-PB7, CB2	I_{OH}	-100 -1.0	-1000 -2.5	-	μA_{dc} mAdc
Output Low Current (Sinking) ($V_{OL} = 0.4$ Vdc)	I_{OL}	1.6	-	-	mAdc
Output Leakage Current (Off State) \overline{IRQA} , \overline{IRQB}	I_{off}	-	1.0	10	μA_{dc}
Power Dissipation	P_D	-	300	600	mW
Input Capacitance ($V_{in} = 0$, $T_A = 25^\circ C$, $f = 1.0$ MHz) D0-D7, PA0-PA7, PB0-PB7, CA2, CB2 R/W, \overline{Reset} , $\overline{RS0}$, $\overline{RS1}$, $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, CA1, CB1 Enable	C_{in}	- - -	- - -	10 7.0 20	pF
Output Capacitance ($V_{in} = 0$, $T_A = 25^\circ C$, $f = 1.0$ MHz)	C_{out}	-	-	10	pF

AC (DYNAMIC) CHARACTERISTICS Loading = 30 pF and one TTL load for PA0-PA7, PB0-PB7, CA2, CB2
= 130 pF and one TTL load for D0-D7, IRQA, IRQB

READ TIMING CHARACTERISTICS (Figure 1)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Delay Time, Address valid to Enable positive transition	TAEW	180	—	—	ns
Delay Time, Enable positive transition to Data valid on bus	TEDR	—	—	395	ns
Peripheral Data Setup Time	TPDSU	300	—	—	ns
Data Bus Hold Time	THR	10	—	—	ns
Delay Time, Enable negative transition to CA2 negative transition	TCA2	—	—	1.0	μs
Delay Time, Enable negative transition to CA2 positive transition	TRS1	—	—	1.0	μs
Rise and Fall Time for CA1 and CA2 input signals	t _r , t _f	—	—	1.0	μs
Delay Time from CA1 active transition to CA2 positive transition	TRS2	—	—	2.0	μs
Rise and Fall Time for Enable input	t _{rE} , t _{fE}	—	—	25	μs

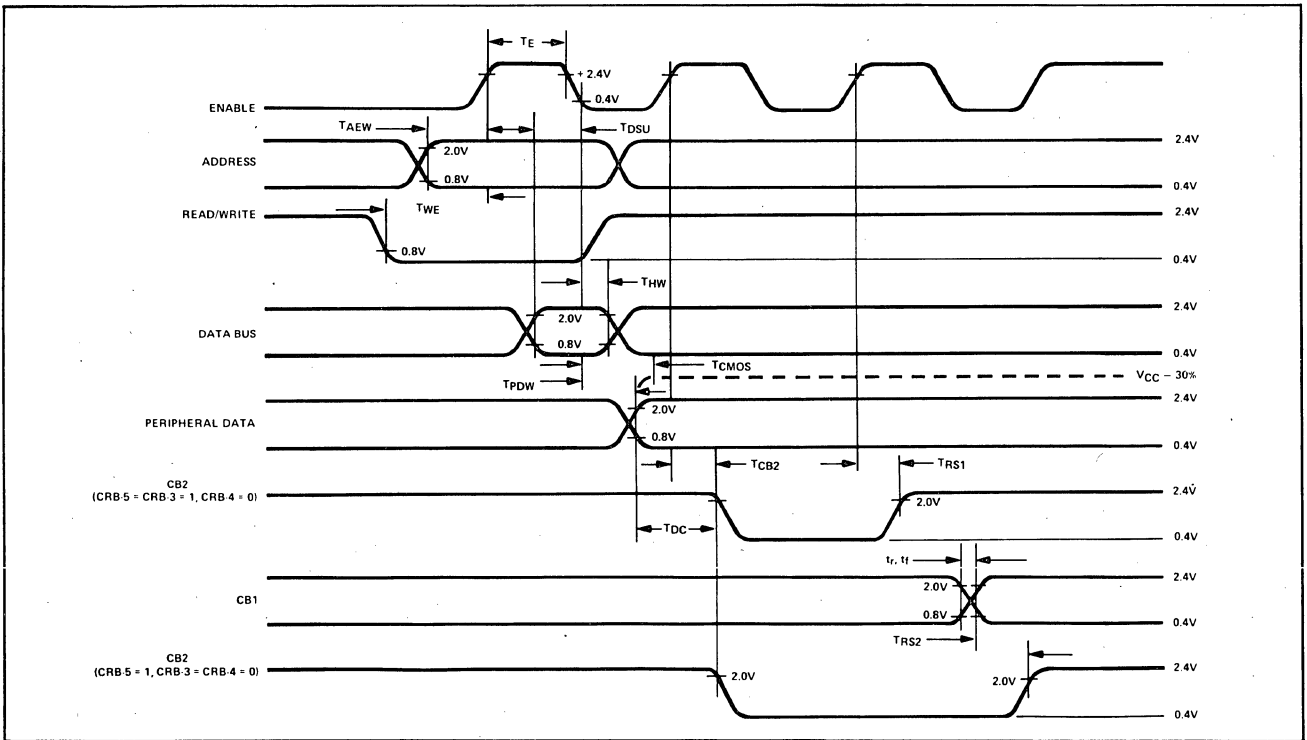
FIGURE 1 – READ TIMING CHARACTERISTICS



WRITE TIMING CHARACTERISTICS (Figure 2)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Enable Pulse Width	T_E	0.470	—	25	μs
Delay Time, Address valid to Enable positive transition	T_{AEW}	180	—	—	ns
Delay Time, Data valid to Enable negative transition	T_{DSU}	300	—	—	ns
Delay Time, Read/Write negative transition to Enable positive transition	T_{WE}	130	—	—	ns
Data Bus Hold Time	T_{HW}	10	—	—	ns
Delay Time, Enable negative transition to Peripheral Data valid	T_{PDW}	—	—	1.0	μs
Delay Time, Enable negative transition to Peripheral Data valid, CMOS ($V_{CC} - 30\%$)	T_{CMOS}	—	—	2.0	μs
Delay Time, Enable positive transition to CB2 negative transition	T_{CB2}	—	—	1.0	μs
Delay Time, Peripheral Data valid to CB2 negative transition	T_{DC}	0	—	1.5	μs
Delay Time, Enable positive transition to CB2 positive transition	T_{RS1}	—	—	1.0	μs
Rise and Fall Time for CB1 and CB2 input signals	t_r, t_f	—	—	1.0	μs
Delay Time, CB1 active transition to CB2 positive transition	T_{RS2}	—	—	2.0	μs

FIGURE 2 – WRITE TIMING CHARACTERISTICS



INTERFACE DESCRIPTION

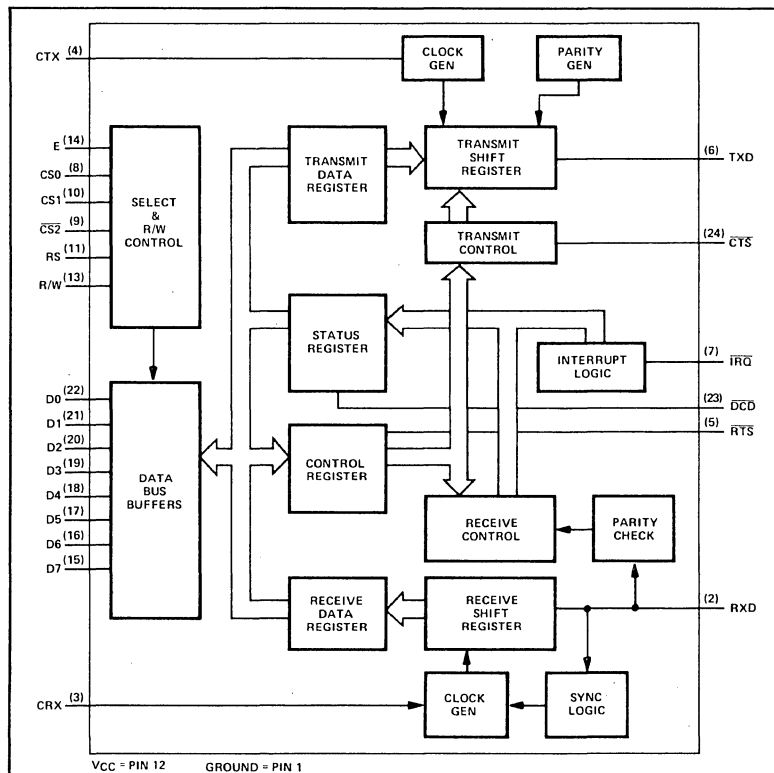
MPU/PIA INTERFACE

Pin	Label	Function
(33)	D0	Bi-Directional Data – The bi-directional data lines (D0-D7) allow the transfer of data between the MPU and the PIA. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs a PIA read operation. The Read/Write line is in the Read (high) state when the PIA is selected for a Read operation.
(32)	D1	
(31)	D2	
(30)	D3	
(29)	D4	
(28)	D5	
(27)	D6	
(26)	D7	
(25)	E	Enable – The enable pulse, E, is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse. This signal will normally be a derivative of the S6800 $\phi 2$ Clock. The E pulse is used to condition the interrupt/control lines CA1, CA2, CB1, and CB2. At least one E pulse must occur from the inactive edge to the active edge of the input signal to set the interrupt flag, when the lines are used as inputs.
(21)	R/W	Read/Write – This signal is generated by the MPU to control the direction of data transfers on the Data Bus. A low state on the PIA Read/Write line enables the input buffers and data is transferred from the MPU to the PIA on the E signal if the device has been selected. A high on the Read/Write line sets up the PIA for a transfer of data to the bus. The PIA output buffers are enabled when the proper address and the enable pulse E are present.
(34)	$\overline{\text{RESET}}$	Reset – The active low $\overline{\text{Reset}}$ line is used to reset all register bits in the PIA to a logical zero (low). This line can be used as a power-on reset and as a master reset during system operation.
(22)	CS0	Chip Select – These three input signals are used to select the PIA. CS0 and CS1 must be high and $\overline{\text{CS2}}$ must be low for selection of the device. Data transfers are then performed under the control of the Enable and Read/Write signals. The chip select lines must be stable for the duration of the E pulse.
(24)	CS1	
(23)	$\overline{\text{CS2}}$	
(36)	RS0	PIA Register Select – The two register select lines are used to select the various registers inside the PIA. These two lines are used in conjunction with internal Control Registers to select a particular register that is to be written or read. The Register select lines should be stable for the duration of the E pulse while in the read or write cycle.
(35)	RS1	
(38)	$\overline{\text{IRQA}}$	Interrupt Request – The active low Interrupt Request lines ($\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$) act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are “open source” (no load device on the chip) and are capable of sinking a current of 1.6 mA from an external source. This permits all interrupt request lines to be tied together in a wire-OR configuration. Each Interrupt Request line has two internal interrupt flag bits that will cause the Interrupt Request line to go low. Each flag bit is associated with a particular peripheral interrupt line. Also four interrupt enable bits are provided in the PIA which may be used to inhibit a particular interrupt from a peripheral device. Servicing an interrupt by the MPU is accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set. The Interrupt Flag is cleared (zeroed) as a result of an MPU Read Peripheral Data Operation.
(37)	$\overline{\text{IRQB}}$	

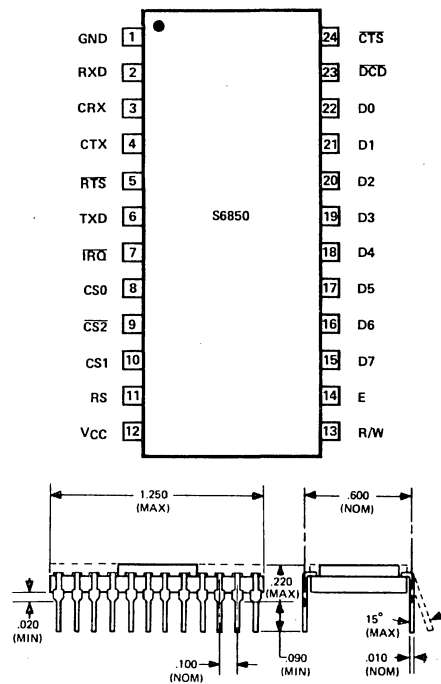
PIA/PERIPHERAL INTERFACE

Pin	Label	Function
(2)	PA0	<p>Section A Peripheral Data – Each of the peripheral data lines can be programmed to act as an input or output. This is accomplished by setting a “1” in the corresponding Data Direction Register bit for those lines which are to be outputs. A “0” in a bit of the Data Direction Register causes the corresponding peripheral data line to act as an input. During an MPU Read Peripheral Data Operation, the data on peripheral lines programmed to act as inputs appears directly on the corresponding MPU Data Bus lines. In the input mode the internal pullup resistor on these lines represents a maximum of one standard TTL load.</p> <p>The data in Output Register A will appear on the data lines that are programmed to be outputs. A logical “1” written into the register will cause a “high” on the corresponding data line while a “0” results in a “low”. Data in Output Register A may be read by an MPU “Read Peripheral Data A” operation when the corresponding lines are programmed as outputs. This data will be read properly if the voltage on the peripheral data lines is greater than 2.0 volts for a logic “1” output and less than 0.8 volt for a logic “0” output. Loading the output lines such that the voltage on these lines does not reach full voltage causes the data transferred into the MPU on a Read operation to differ from that contained in the respective bit of Output Register A.</p>
(3)	PA1	
(4)	PA2	
(5)	PA3	
(6)	PA4	
(7)	PA5	
(8)	PA6	
(9)	PA7	
(10)	PB0	
(11)	PB1	
(12)	PB2	
(13)	PB3	
(14)	PB4	
(15)	PB5	
(16)	PB6	
(17)	PB7	
(40)	CA1	<p>Interrupt Input – Peripheral Input lines CA1 and CB1 are input-only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.</p>
(18)	CB1	
(39)	CA2	<p>Peripheral Control – The peripheral control line CA2 can be programmed to act as an interrupt input or as a peripheral control output. As an output, this line is compatible with standard TTL; as an input the internal pullup resistor on this line represents one standard TTL load. The function of this signal line is programmed with Control Register A.</p>
(19)	CB2	<p>Peripheral Control – Peripheral Control line CB2 may also be programmed to act as an interrupt input or peripheral control output. As an input, this line has high input impedance and is compatible with standard TTL. As an output it is compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch. This line is programmed by Control Register B.</p>
(1)	GND	Ground
(20)	VCC	+5 Volts ± 5%

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

FEATURES

- 8 Bit Bidirectional Data Bus for Communication with MPU.
- False start bit deletion.
- Peripheral/modem control functions.
- Double buffered Receiver and Transmitter
- One or two stop bit operation.
- Eight and nine-bit transmission with optional even and odd parity.
- Parity, overrun and framing error checking.
- Programmable control register.
- Optional $\div 1$, $\div 16$, and $\div 64$ clock modes.
- Up to 500,000 bps transmission.

FUNCTIONAL DESCRIPTION

The S6850 Asynchronous Communications Interface Adapter (ACIA) provides the data formatting and control to interface serial asynchronous data communications to bus organized systems such as the S6800 Microprocessing Unit.

The S6850 includes select enable, read/write, interrupt and bus interface logic to allow data transfer over an eight bit

bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. Word lengths, clock division ratios and transmit control through the Request to Send output may be programmed. For modem operation three control lines are provided. These lines allow the ACIA to interface directly with the S6860 0-600 bps digital modem.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	-0.3 to +7.0V	Operating Temperature Range T_A	0 to +70°C
Input Voltage V_{in}	-0.3 to +7.0V	Storage Temperature Range T_{stg}	-55 to +150°C

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC (STATIC) CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$, $T_A = 25^\circ C$ unless otherwise noted.)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.4	-	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	-0.3	-	+0.4	Vdc
Input High Threshold Voltage All Inputs Except Enable	V_{IHT}	+2.0	-	-	Vdc
Input Low Threshold Voltage All Inputs Except Enable	V_{ILT}	-	-	+0.8	Vdc
Input Leakage Current ($V_{in} = 0$ to 5.0 Vdc) R/W, RS, CS0, CS1, $\overline{CS2}$, Enable	I_{in}	-	1.0	2.5	μ Adc
Three-State (Off State) Input Current ($V_{in} = 0.4$ to 2.4 Vdc, $V_{CC} = \text{max}$) D0-D7,	I_{TSI}	-	2.0	10	μ Adc
Output High Voltage ($I_{Load} = -100 \mu$ Adc, Enable Pulse Width < 25 μ s) All Outputs Except \overline{IRQ}	V_{OH}	+2.4	-	-	Vdc
Output Low Voltage ($I_{Load} = 1.6$ mAdc) Enable Pulse Width < 25 μ s	V_{OL}	-	-	+0.4	Vdc
Output Leakage Current (Off State) \overline{IRQ}	I_{LOH}	-	1.0	10	μ Adc
Power Dissipation	P_D	-	300	525	mW
Input Capacitance ($V_{in} = 0$, $T_A = 25^\circ C$, $f = 1.0$ MHz) D0-D7 R/W, RS, CS0, CS1, $\overline{CS2}$, RXD, CTX, CRX, \overline{CTS} , \overline{DCD} Enable	C_{in}	-	-	10	pF
Output Capacitance ($V_{in} = 0$, $T_A = 25^\circ C$, $f = 1.0$ MHz)	C_{out}	-	-	10	pF

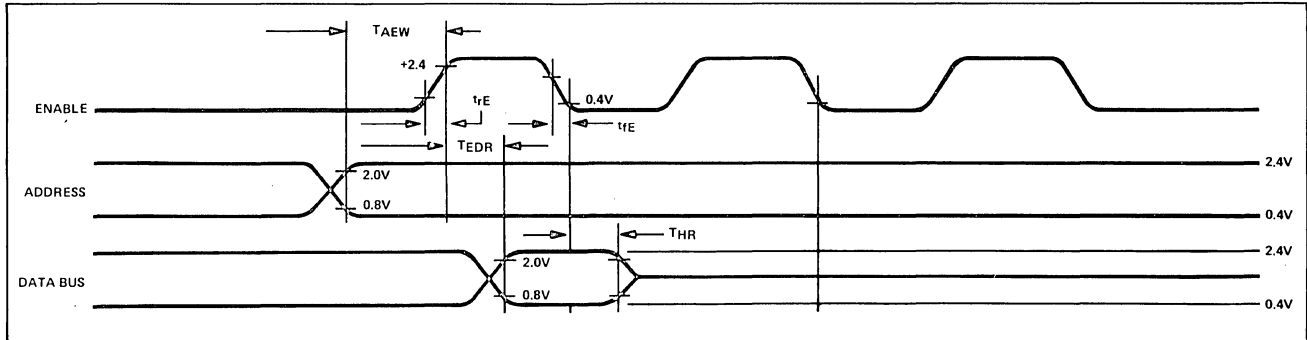
AC (DYNAMIC) CHARACTERISTICS

Loading = 130 pF and one TTL load for D0-D7 = 20pF and 1 TTL load for \overline{RTS} and TXD = 100pF and 3K Ω to V_{CC} for \overline{IRQ} .

READ TIMING CHARACTERISTICS (Figure 1)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Setup Time, Address valid to Enable positive transition	T_{AEW}	180	-	-	ns
Setup Time, Enable positive transition to Data valid on bus	T_{EDR}	-	-	395	ns
Data Bus Hold Time	T_{HR}	10	-	-	ns
Rise and Fall Time for Enable input	t_{rE} , t_{fE}	-	-	25	μ s

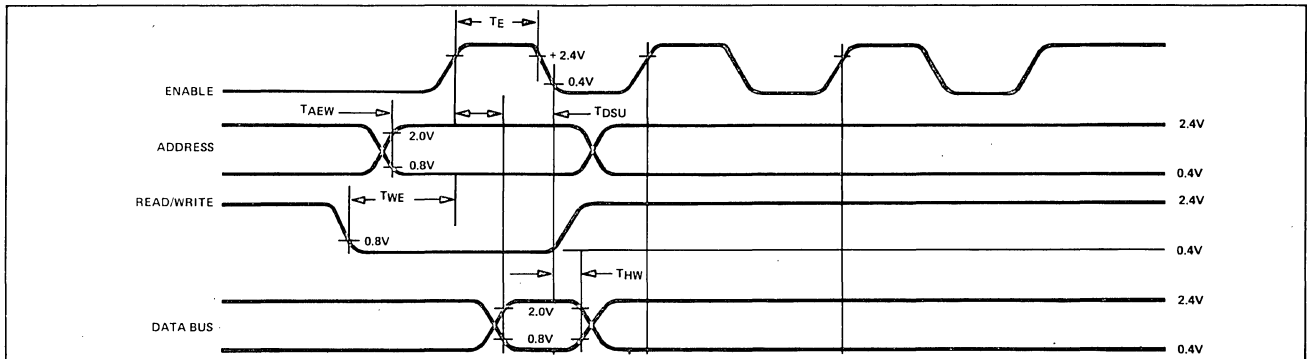
FIGURE 1 – READ TIMING CHARACTERISTICS



WRITE TIMING CHARACTERISTICS (Figure 2)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Enable Pulse Width	T _E	0.470	—	25	μs
Setup Time, Address valid to Enable positive transition	T _{AEW}	180	—	—	ns
Setup Time, Data valid to Enable netative transition	T _{DSU}	300	—	—	ns
Setup time, Read/Write negative transition to Enable positive transition	T _{WE}	130	—	—	ns
Data Bus Hold Time	T _{HW}	10	—	—	ns

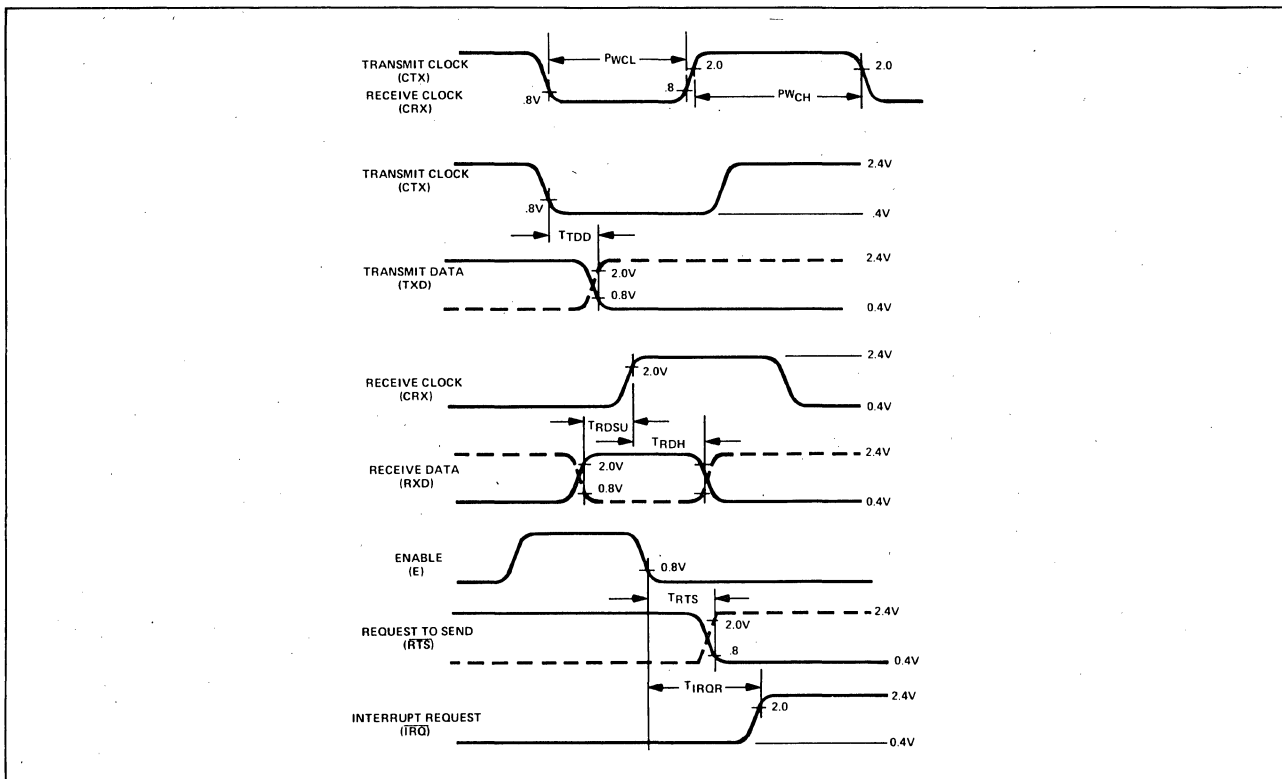
FIGURE 2 – WRITE TIMING CHARACTERISTICS



TRANSMIT/RECEIVE CHARACTERISTICS (Figure 3)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Clock Frequency ÷ 1 mode ÷ 16 mode ÷ 64 mode	f _C			500 800 800	KHz KHz KHz
Clock Pulse Width, Low State	PW _{CL}	600			nsec
Clock Pulse Width, High State	PW _{CH}	600			nsec
Delay Time, Transmit Clock to Data Out	TTDD			1.0	μsec
Set up Time, Receive Data	TRDSU	500			nsec
Hold Time, Receive Data	TRDH	500			nsec
Delay Time, Enable to $\overline{\text{IRQ}}$ Reset	T _{IRQR}			1.2	μsec
Delay Time, Enable to $\overline{\text{RTS}}$	T _{RTS}			1.0	μsec

FIGURE 3 – TRANSMIT/RECEIVE TIMING



MPU/ACIA INTERFACE

Pin	Label	Function
(22)	D0	ACIA BI-DIRECTIONAL DATA LINES —The bi-directional data lines (D0-D7) allow for data transfer between the ACIA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an ACIA read operation. The Read/Write line is in the read (high) state when the ACIA is selected for a read operation.
(21)	D1	
(20)	D2	
(19)	D3	
(18)	D4	
(17)	D5	
(16)	D6	
(15)	D7	
(14)	E	ACIA ENABLE SIGNAL —The Enable signal (E) is a high impedance TTL compatible input that enables the bus input/output data buffers and clocks data to and from the ACIA. This signal will normally be a derivative of the S6800 $\phi 2$ clock.
(13)	R/W	READ/WRITE CONTROL SIGNAL —The Read/Write line is a high impedance input that is TTL compatible and is used to control the direction of data flow through the ACIA's input/output data bus interface. When Read/Write is high (MPU Read cycle), the ACIA output driver is turned on and a selected register is read. When it is low, the ACIA output driver is turned off and the MPU writes into a selected register. Thus, the Read/Write signal is used to select the Read Only or Write Only registers within the ACIA.
(8)	CS0	CHIP SELECT SIGNALS —These three high impedance TTL compatible input lines are used to address an ACIA. A particular ACIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Transfers of data to and from ACIA are then performed under the control of Enable, Read/Write, and Register Select.
(10)	CS1	
(9)	$\overline{CS2}$	

MPU/ACIA INTERFACE (CONT'D)

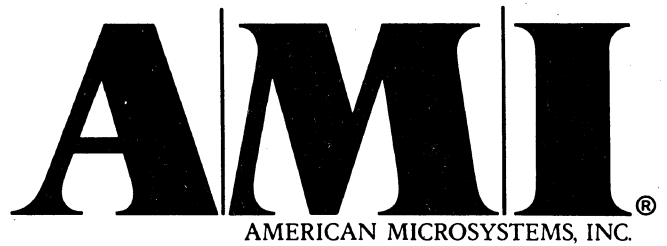
Pin	Label	FUNCTION
(11)	RS	REGISTER SELECT SIGNAL —The Register Select line is a high impedance input that is TTL compatible and is used to select the Transmit/Receive Data or Control/Status registers in the ACIA. The Read/Write signal line is used in conjunction with Register Select to select the Read Only or Write Only register in each register pair.
(7)	$\overline{\text{IRQ}}$	INTERRUPT REQUEST SIGNAL —Interrupt request is a TTL compatible, open drain active low output that is used to interrupt the MPU. The Interrupt Request remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set.

ACIA/MODEM OR PERIPHERAL INTERFACE

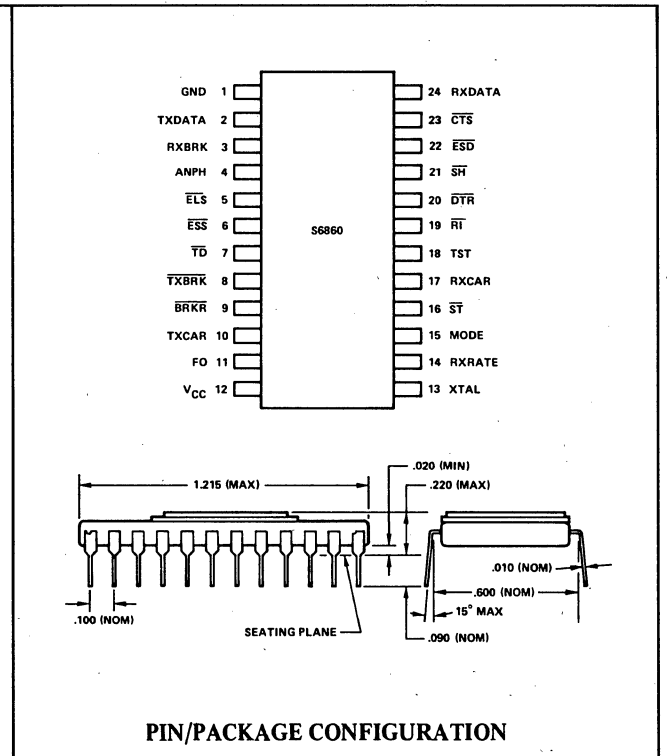
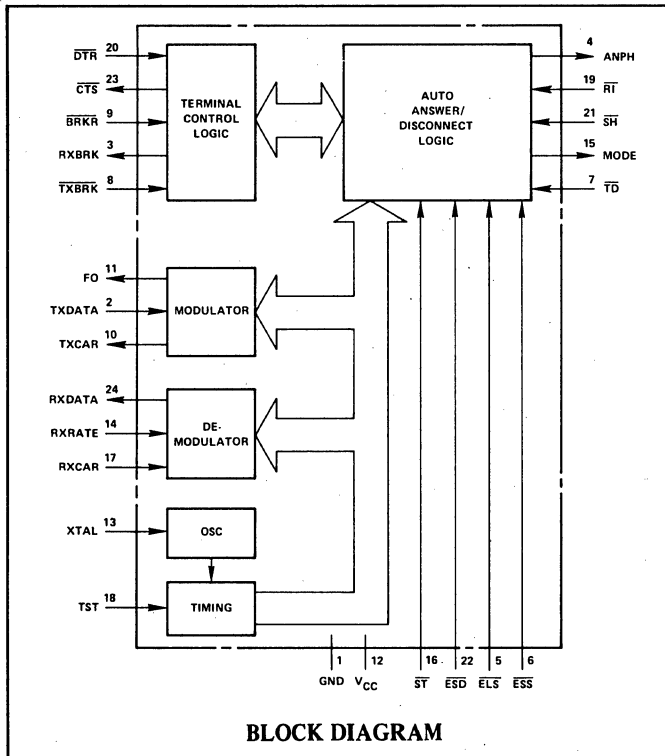
Pin	Label	FUNCTION
(4)	CTX	TRANSMIT CLOCK —The Transmit Clock is a high impedance TTL compatible input used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock. Clock frequency of 1, 16, or 64 times the data rate may be selected.
(3)	CRX	RECEIVE CLOCK —The Receive Clock is a high impedance TTL compatible input used for synchronization of received data. (In the $\div 1$ mode, the clock and data must be synchronized externally.) The receiver strobes the data on the positive transition of the clock. Clock frequency of 1, 16, or 64 times the data rate may be selected.
(2)	RXD	RECEIVED DATA —The Received Data line is a high impedance TTL compatible input through which data is received in a serial NRZ (Non Return to Zero) format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used. Data rates are in the range of 0 to 500 Kbps when external synchronization is utilized.
(6)	TXD	TRANSMIT DATA —The Transmit Data output line transfers serial NRZ data to a modem or other peripheral device. Data rates are in the range of 0 to 500Kbps when external synchronization is utilized.
(24)	$\overline{\text{CTS}}$	CLEAR-TO-SEND —This high impedance TTL compatible input provides automatic control of the transmitting end of a communications link via the modem's "clear-to-send" active low output by inhibiting the Transmitter Data Register Empty status bit (TDRE).
(5)	$\overline{\text{RTS}}$	REQUEST-TO-SEND —The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The active state is low. The Request-to-Send output is controlled by the contents of the ACIA control register.
(23)	$\overline{\text{DCD}}$	DATA CARRIER DETECTED —This high impedance TTL compatible input provides automatic control of the receiving end of a communications link by means of the modem "Data-Carrier-Detect" or "Received-Line-Signal Detect" output. The $\overline{\text{DCD}}$ input inhibits and initializes the receiver section of the ACIA when high. A low to high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the Receiver Interrupt Enable (RIE) is set.
(12)	VCC	+5 volts \pm 5%
(1)	GND	GROUND

S6860

0-600 BPS
DIGITAL MODEM



ADVANCED PRODUCT DESCRIPTION



FEATURES

- Full or half duplex operation
- Originate and answer mode
- Auto answer and disconnect
- Modem self test
- TTL compatible terminal interfaces
- Crystal/External reference control
- Compatible functions for 100 series data sets and 1001 A/B data couplers

FUNCTIONAL DESCRIPTION

The S6860 is a 0-600 bps Digital Modem circuit designed to be integrated into a wide range of equipment utilizing serial data communications.

The modem provides the necessary modulation, demodulation and supervisory control functions to implement a serial data communications link, over a voice grade channel, utilizing frequency shift keying (FSK) a bit rates up to 600 bps. The S6860 can be implemented into a wide range of data handling

systems, including stand alone modems, data storage devices, remote data communication terminals and I/O interfaces for minicomputers.

N-channel silicon gate technology permits the S6860 to operate using a single voltage supply and be fully TTL compatible.

The modem is compatible with the S6800 microcomputer family, interfacing directly with the Asynchronous Communications Interface Adapter (ACIA) to provide low-speed data communications capability.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	- 0.3 to +7.0V	Operating Temperature Range T_A	0 to 70°C
Input Voltage V_{IN}	- 0.3 to +7.0V	Storage Temperature Range T_{STG}	- 50 to 150°C

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

MICROPROCESSOR AMI

DC (STATIC) CHARACTERISTICS

($V_{CC} = 5.0V \pm 5\%$, $T_A = 25^\circ C$ unless otherwise noted.)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT
V_{IH}	Input High Voltage, All inputs Except Crystal	2.0	—	V_{CC}	Vdc
V_{IL}	Input Low Voltage, All inputs Except Crystal	-0.3	—	0.8	Vdc
V_{IN}	Crystal Input Voltage (Crystal Input Driven from an External Reference, Input Coupling Capacitor = 200 pF, Duty Cycle = $50 \pm 5\%$)	1.5	—	2.0	V_{p-p}
I_{IN}	Input Current ($V_{IN} = GND$) All Inputs Except RXCAR, TXDATA, \overline{TD} , TST, \overline{RI} , \overline{SH} \overline{RI} , \overline{SH} Inputs	—	—	-0.2 -1.6	mAdc
I_{IL}	Input Leakage Current ($V_{IN} = 0$ to 5.0 Vdc)	—	—	1.	μ Adc
V_{OH1}	Output High Voltage, All Outputs Except ANPH and TXCAR ($I_{OH1} = -0.04$ mAdc, Load A)	2.4	—	V_{CC}	Vdc
V_{OL1}	Output Low Voltage, All Outputs Except ANPH and TXCAR ($I_{OL1} = 1.6$ mAdc, Load A)	-0.3	—	0.4	Vdc
I_{OH2}	Output High Current, ANPH ($V_{OH2} = 0.8$ Vdc, Load B)	0.3	—	—	mAdc
V_{OL2}	Output Low Voltage, ANPH ($I_{OL2} = 0$, Load B)	-0.3	—	0.3	Vdc
C_{IN}	Input Capacitance ($f = 0.1$ MHz)	—	5.	—	pF
C_{OUT}	Output Capacitance ($f = 0.1$ MHz)	—	10	—	pF
V_{CO}	Transmit Carrier Output Voltage (Load C)	0.20	0.35	0.50	V(RMS)
V_{2H}	Transmit Carrier Output 2nd Harmonic (Load C)	-25	-32	—	dB
I_{DD}	V_{CC} Supply Current (All Inputs at GND & All Outputs Open)	—	30	65	mAdc

AC (DYNAMIC) CHARACTERISTICS

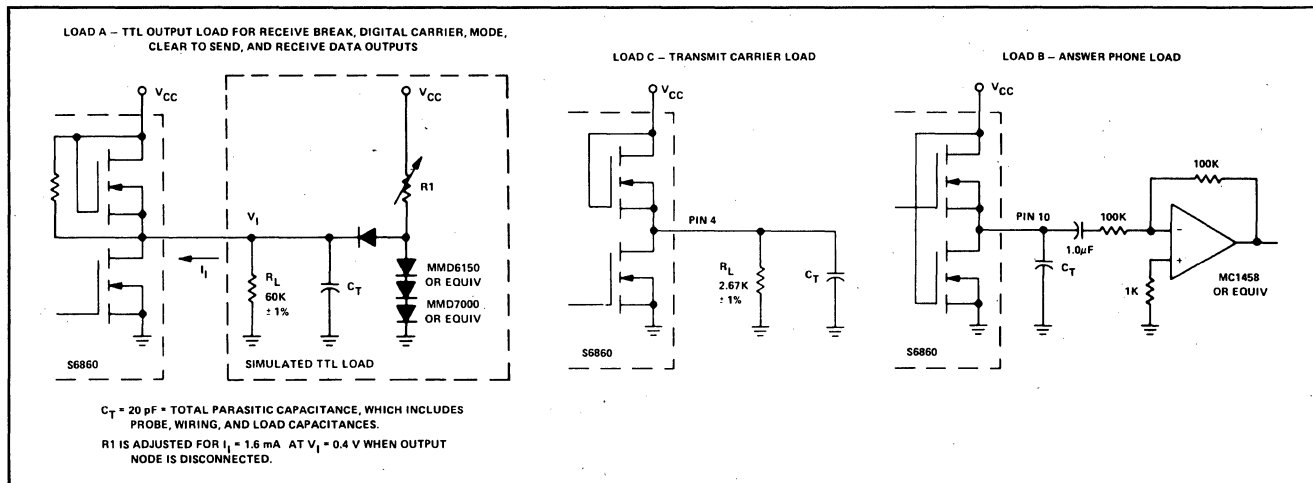
(Loading is as shown in Figure 1 unless otherwise noted.)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT
t_r t_f	Input Transition Times, All Inputs Except Crystal (Operating in the Crystal Input Mode; from 10% to 90% Points)	—	—	1.* 1.*	μ s
t_r t_f	Input Transition Times, Crystal Input (Operating in External Input Reference Mode)	—	—	30 30	ns
t_r t_f	Output Transition Times, All Outputs Except TXCAR (From 10% to 90% Points)	—	—	5. 5.	μ s

*Maximum Input Transition Times are $\leq 0.1 \times$ Pulse Width or the specified maximum of 1.0 μ s, whichever is smaller.

AC (DYNAMIC) CHARACTERISTICS (CONT'D)

FIGURE 1 TEST LOADING



MODEM/TERMINAL INTERFACE

PIN	LABEL	FUNCTION
(2)	TXDATA	Transmit Data – Serial data transferred to the modem via the ACIA for transmitting to the receiving terminal.
(8)	TXBRK	Transmit Break – Used to signal the remote modem to stop transmitting data. A Transmit Break (low) greater than 34 ms forces the modem to send a continuous space signal for 233 ms. Transmit Break must be initiated only after CTS has been established. This is a negative edge sense input. Prior to initiating TXBRK this input must be held high for a minimum of 34 ms.
(24)	RXDATA	Receive Data – The data resulting from demodulating the Receive Carrier signal. A high level is a mark.
(3)	RXBRK	Receive Break – Upon receipt of a continuous 150 ms space, the modem automatically clamps the Receive Break output high. This output is also clamped high until Clear-to-Send is established.
(9)	BRKR	Break Release – The Receive Break output (clamp high condition) can be removed by holding the Break Release signal low for at least 20 μs after receiving a minimum 150 ms space signal.
(20)	DTR	Data Terminal Ready – Enables the modem function when low. When DTR is held high for 34 ms minimum, a disconnect is initiated and will occur 3 sec. later.
(23)	CTS	Clear-to-Send – A low on the CTS output indicates the Transmit Data input has been unclamped from a steady Mark, thus allowing data transmission.
(16)	ST	Self Test – With this input at a low level, the demodulator is switched to the modulator frequency and demodulates the transmitted FSK signal. Channel establishment, which occurred during the initial handshake, is not lost during self test. The Mode Control output changes state during Self Test, permitting the receive filters to pass the local Transmit Carrier.

ST	SH	RT	MODE
H	L	H	H
H	H	L	L
L	L	H	L
L	H	L	H

(18)	TST	Test Clock – A high input signal decreases the modem test time. This input must be low for normal operation.
(11)	FO	Frequency Output – A test signal is output to decrease modem test time. The signal is a square wave at the transmit frequency.

EXTERNAL MODEM INTERFACE

PIN	LABEL	FUNCTION														
(12)	V _{CC}	+ 5 Volts ± 5%														
(1)	GND	Ground														
(22)	$\overline{\text{ESD}}$	Enable Space Disconnect – When $\overline{\text{ESD}}$ is strapped low and $\overline{\text{DTR}}$ is pulsed to initiate a disconnect, the modem transmits a space for either 3 s or until a loss of threshold is detected, whichever occurs first. If $\overline{\text{ESD}}$ is strapped high, data instead of a space is transmitted. A disconnect occurs at the end of 3 s.														
(5)	$\overline{\text{ELS}}$	Enable Long Space Disconnect – A strapping option which, when low, will automatically hang up the phone upon receipt of a continuous space for 1.5 s.														
(6)	$\overline{\text{ESS}}$	Enable Short Space Disconnect – A strapping option which, when low, will automatically hang up the phone upon receipt of a continuous space for 0.3 s. ESS and ELS must not be simultaneously strapped low.														
(13)	XTAL	Crystal – A 1.0 MHz crystal is required to use the on-chip oscillator. A 1.0 MHz square wave can also be applied to this pin to satisfy the clock requirements. Crystal parameters are as follows:														
<table border="1"> <thead> <tr> <th>Mode:</th> <th>Parallel</th> </tr> </thead> <tbody> <tr> <td>Frequency:</td> <td>1.0 MHz ± 0.1%</td> </tr> <tr> <td>Series Resistance:</td> <td>750 ohms max</td> </tr> <tr> <td>Shunt Capacitance:</td> <td>7.0 pF max</td> </tr> <tr> <td>Temperature:</td> <td>0 - 70°C</td> </tr> <tr> <td>Test Level:</td> <td>1.0 mW</td> </tr> <tr> <td>Load Capacitance:</td> <td>13 pF</td> </tr> </tbody> </table>			Mode:	Parallel	Frequency:	1.0 MHz ± 0.1%	Series Resistance:	750 ohms max	Shunt Capacitance:	7.0 pF max	Temperature:	0 - 70°C	Test Level:	1.0 mW	Load Capacitance:	13 pF
Mode:	Parallel															
Frequency:	1.0 MHz ± 0.1%															
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Shunt Capacitance:	7.0 pF max															
Temperature:	0 - 70°C															
Test Level:	1.0 mW															
Load Capacitance:	13 pF															
When using the 1.0 MHz crystal, external parasitic capacitance, including crystal shunt capacitance, must be ≤ 9 pF at the crystal input.																
(14)	RXRATE	Receive Data Rate – The demodulator has been optimized for signal-to-noise performance at 300 bps and 600 bps. The Receive Data Rate input must be low for 0-600 bps and should be high for 0-300 bps.														

MODEM/DATA COUPLER INTERFACE

PIN	LABEL	FUNCTION
(15)	MODE	Mode – Indicates the Originate (high) or Answer (low) status of the modem. This output changes when a Self Test ($\overline{\text{ST}}$) signal is applied.
(19)	$\overline{\text{RI}}$	Ring Indicator – The modem function will recognize the receipt of a call from the CBT if at least 20 cycles of the 20 - 47 Hz ringing signal (low level ≥ 50% of the duty cycle) are present. The CBS $\overline{\text{RI}}$ signal must be level-converted to TTL according to the EIA RS-232 specification before interfacing it with the modem function. The receipt of a call from the CBS is recognized if the $\overline{\text{RI}}$ signal is present for at least 51 ms. This input is held high except during ringing. A $\overline{\text{RI}}$ signal automatically places the modem function in the Answer Mode.
(21)	$\overline{\text{SH}}$	Switch Hook – Interfaces directly with the CBT type Data Coupler and via the EIA RS-232 level conversion for the CBS type. An $\overline{\text{SH}}$ signal automatically places the modem function in the Originate Mode. $\overline{\text{SH}}$ is low during origination of a call. The modem will automatically hang up 17 s after releasing $\overline{\text{SH}}$ if the handshaking routine has not been accomplished.

MODEM/DATA COUPLER INTERFACE (Continued)

PIN	LABEL	FUNCTION
(4)	ANPH	Answer Phone – Upon receipt of Ring Indicator or Switch Hook signal and Data Terminal Ready, the Answer Phone output goes high ($[SH + RI] \bullet DTR$). This signal drives the base of a transistor which activates the Off Hook and Data Transmission control lines in the data coupler. Upon call completion, the Answer Phone signal returns to a low level.
(7)	\overline{TD}	Threshold Detect – This input is derived from an external threshold detector. If the signal level is sufficient, the \overline{TD} input must be low for 20 μs at least once every 32 ms to maintain normal operation. An insufficient signal level indicates the absence of the Receive Carrier; an absence for less than 32 ms will not cause channel establishment to be lost; however, data during this interval will be invalid. If the signal is present and the level is acceptable at all times, then the threshold input can be low permanently. Loss of threshold for 51 ms or longer results in a loss of Cler-to-Send. The Transmit Carrier of the originate modem is clamped off and a constant Mark is transmitted from the answer modem.
(17)	RXCAR	Receive Carrier – The FSK input to the demodulators. The local Transmit Carrier must be balanced or filtered out prior to this input, leaving only the Receive Carrier in the signal. The Receive Carrier must also be hard limited. Any half cycle period greater than or equal to $429 \pm 1.0 \mu s$ for the low band or $235 \pm 1.0 \mu s$ for the high band is detected as a space.
(10)	TXCAR	Transmit Carrier – A digitally synthesized sine wave derived from a 1.0 MHz crystal reference (see Figure 2). Frequency characteristics are given in the following table.

MODE	DATA	FREQUENCY	TOLERANCE*
Originate	Mark	1270 Hz	- 0.15 Hz
Originate	Space	1070 Hz	- 0.09 Hz
Answer	Mark	2225 Hz	- 0.31 Hz
Answer	Space	2025 Hz	- 0.71 Hz

*The reference frequency tolerance is not included.

The proper output frequency is transmitted within 3.0 μs following a data bit change with no more than 2.0 μs phase discontinuity. The typical output level is 0.35 V (RMS) into a 100K-ohm load impedance.

The second harmonic is typically 32 dB below the fundamental (see Figure 3).

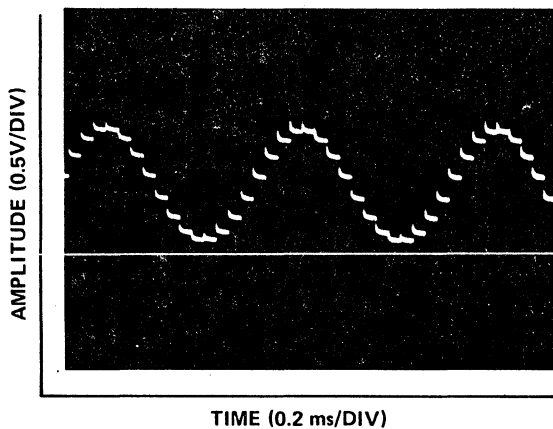


FIGURE 2 TRANSMIT CARRIER SINE WAVE

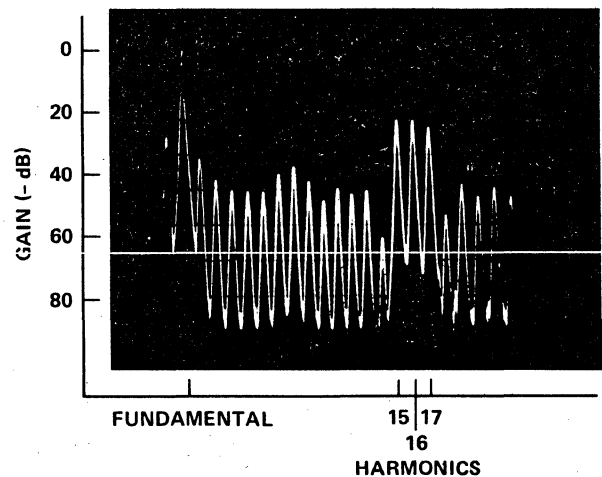
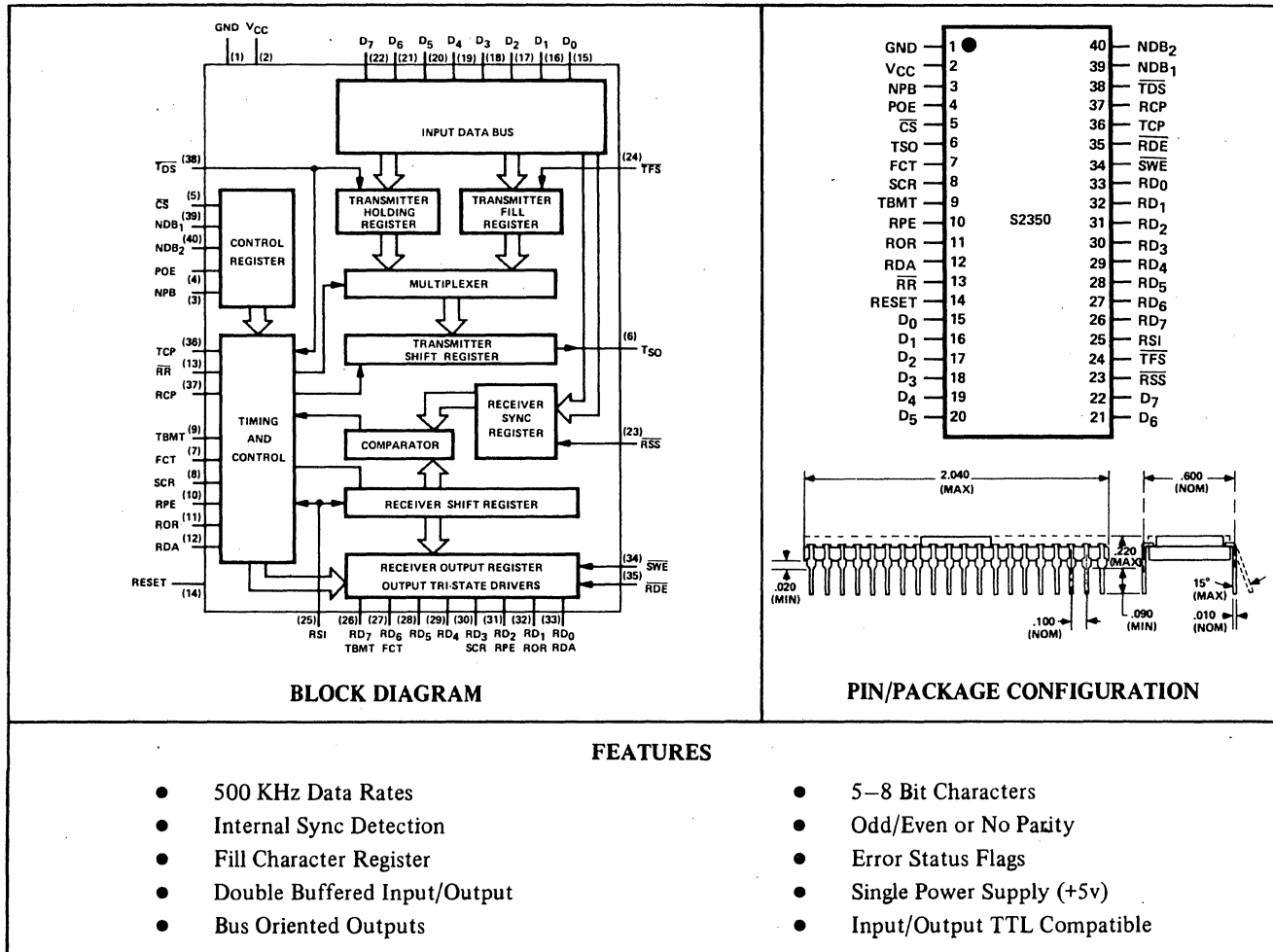


FIGURE 3 TRANSMIT CARRIER FREQUENCY SPECTRUM

ADVANCED PRODUCT DESCRIPTION



FUNCTIONAL DESCRIPTION

The S2350 Universal Synchronous Receiver Transmitter (USRT) is a single chip MOS/LSI device that totally replaces the serial to parallel and parallel to serial conversion logic required to interface a word parallel controller or data terminal to a bit-serial, synchronous communication network.

The USRT consists of separate receiver and transmitter sections with independent clocks, data lines and status. Common with the transmitter and receiver are word length and parity mode. Data is transmitted and received in a NRZ format at a rate equal to the respective input clock frequency.

Data messages are transmitted as a contiguous character stream, bit synchronous with respect to a clock and character synchronous with respect to framing or "sync" characters initializing each message. The USRT receiver compares the contents of the internal Receiver Sync Register with the incoming data stream in a bit transparent mode. When a compare is made, the receiver becomes character synchronous for-

matting a 5, 6, 7, or 8 bit character for output each character time. The receiver has an output buffer register allowing a full character time to transfer the data out. The receiver status outputs indicate received data available (RDA), receiver overrun (ROR), receive parity error (RPE) and sync character received (SCR). Status bits are available on individual output lines and can also be multiplexed onto the output data lines for bus organized systems. The data lines have tri-state outputs.

The USRT transmitter outputs 5, 6, 7, or 8 bit characters with correct parity at the transmitter serial output (TSO). The transmitter is buffered to allow a full character time to respond to a transmitter buffer empty (TBMT) request for data. Data is transmitted in a NRZ format changing on the positive transition of the transmitter clock (TCP). The character in the transmitter fill register is inserted into the data message if a data character is not loaded into the transmitter after a TBMT request.

TYPICAL APPLICATIONS

- Computer Peripherals
- High Speed Terminals
- Communication Concentrators
- Time Division Multiplexing
- Integrated Modems
- Industrial Data Transmission

ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0°C to + 70°C
Storage temperature	-65°C to +150°C
Positive voltage on any pin with respect to GROUND	+7 volt
Negative voltage on any pin with respect to GROUND	-0.5 volt
Power dissipation	0.75 watt

DC (STATIC) CHARACTERISTICS*

V_{CC} = +5V ±5%, T_A = 25°C unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Condition
V _{IH}	Input High Voltage	2.0	V _{CC}	Volt	V _{IN} = 0 TO V _{CC} Volts
V _{IL}	Input Low Voltage	- 0.5	+0.8	Volt	
I _{IL}	Input Leakage Current		10	µa	
V _{OH}	Output High Voltage	2.4		Volts	I _{OH} = -100µa I _{OL} = 1.6ma
V _{OL}	Output Low Voltage		+0.4	Volts	
C _{IN}	Input Capacitance		10	pf	} V _{IN} = 0 Volt f = 1.0 MHZ
C _{OUT}	Output Capacitance		12	pf	
I _{CC}	V _{CC} Supply Current		100	ma	No Load

*Electrical characteristics included in this advanced product description are objective specifications and may be subject to change.

AC (DYNAMIC) CHARACTERISTICS

V_{CC} = +5V ±5%, T_A = 25°C unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Condition
TCP, RCP	Clock Frequency	DC	500	KHz	

Input Pulse Widths

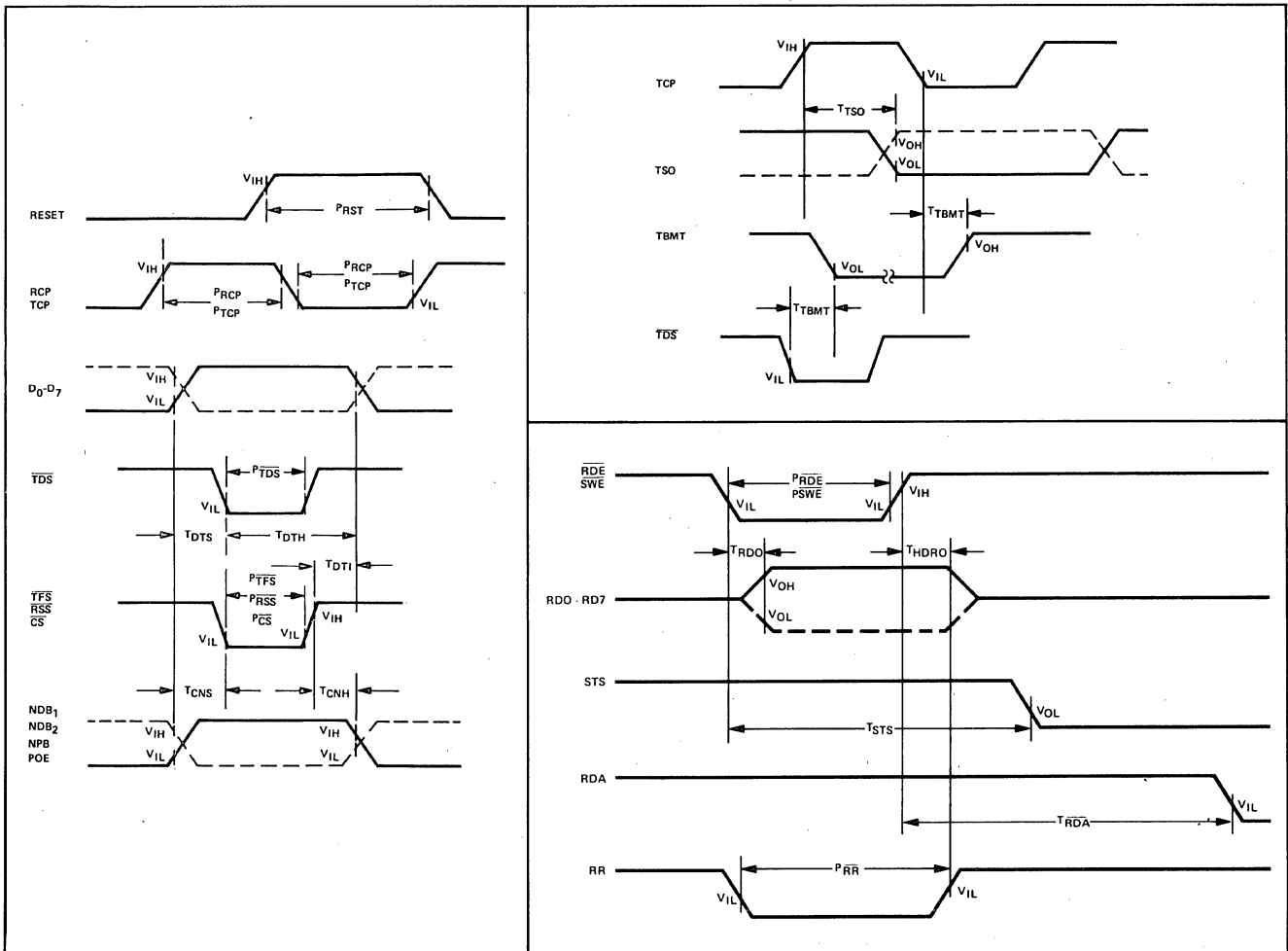
Symbol	Parameter	Min.	Max.	Unit	Condition
P _{TCP}	Transmit Clock	900		nsec	C _L = 20pf 1TTL Load
P _{RCP}	Receive Clock	900		nsec	
P _{RST}	Reset	500		nsec	
P _{TDS}	Transmit Data Strobe	200		nsec	
P _{TFS}	Transmit Fill Strobe	200		nsec	
P _{RSS}	Receive Sync Strobe	200		nsec	
P _{CS}	Control Strobe	200		nsec	
P _{RDE}	Receive Data Enable	400		nsec	Note 1
P _{SWE}	Status Word Enable	400		nsec	Note 1
P _{RR}	Receiver Restart	500		nsec	

AC (DYNAMIC) CHARACTERISTICS (CONT'D) SWITCHING CHARACTERISTICS

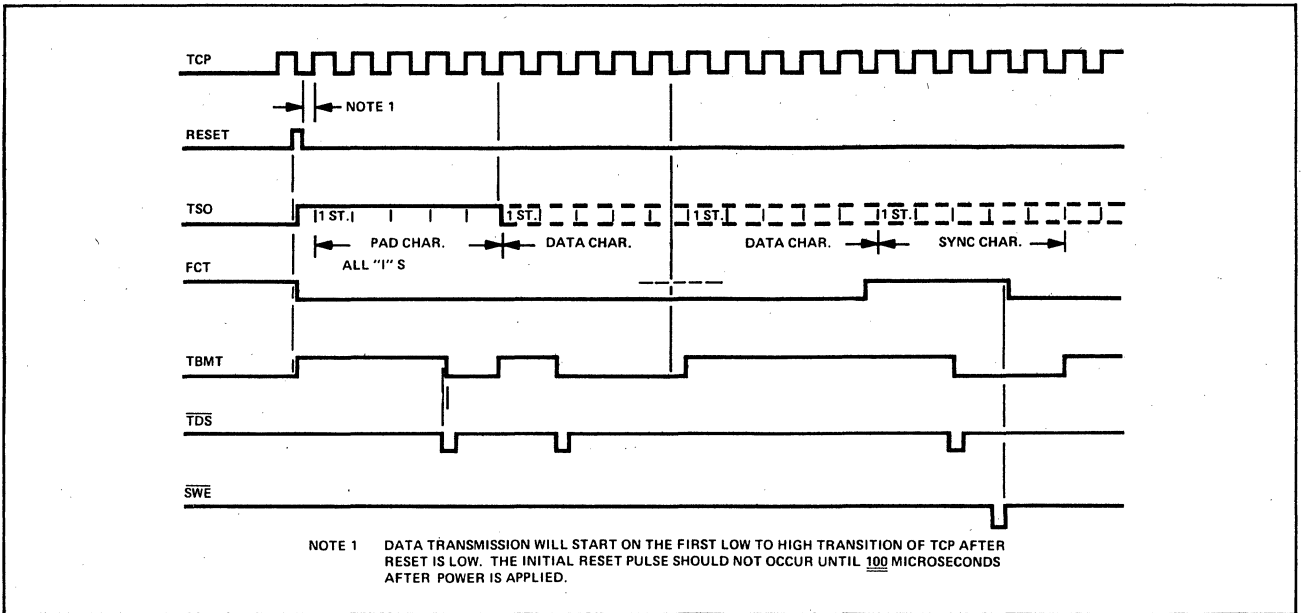
T _{TSO}	Delay, TCP Clock to Serial Data Out		700	nsec	1 TTL Load C _L = 130 pf
T _{TBMT}	Delay, TCP Clock to TBMT Output		1.4	μsec	
T _{TBMT}	Delay, \overline{TDS} to TBMT		700	nsec	
T _{TST}	Delay, \overline{SWE} to Status Reset		700	nsec	
T _{TRDO}	Delay, \overline{SWE} , \overline{RDE} to Data Outputs		400	nsec	
T _{THRDO}	Hold Time \overline{SWE} , \overline{RDE} to Off State		400	nsec	
T _{DTS}	Data Set Up Time \overline{TDS} , \overline{TFS} , \overline{RSS} , \overline{CS}	0		nsec	
T _{DTH}	Data Hold Time \overline{TDS}	700		nsec	
T _{DTI}	Data Hold Time \overline{TFS} , \overline{RSS}	200		nsec	
T _{CNS}	Control Set Up Time NDB1, NDB2, NPB, POE	0		nsec	
T _{CNH}	Control Hold Time NDB1, NDB2, NPB, POE	200		nsec	
T _{TRDA}	Delay \overline{RDE} to \overline{RDA} Output	700		nsec	

NOTE 1: Required to reset status and flags.

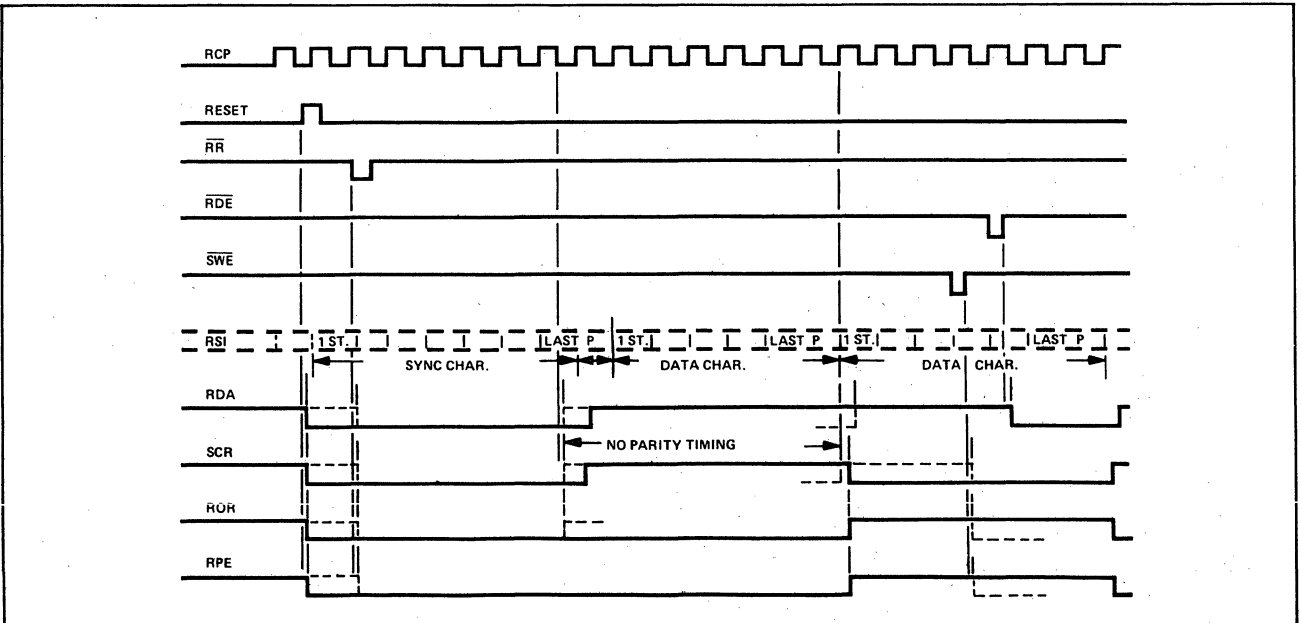
TIMING WAVEFORMS



TRANSMITTER TIMING DIAGRAM



RECEIVER TIMING DIAGRAM



MPU/ACIA INTERFACE (CONT'D)

Pin	Label	Function
(1)	GND	Ground
(2)	VCC	+5 VOLTS ±5%
(14)	RESET	<p>MASTER RESET A V_{IH} initializes both the receiver and transmitter. The Transmitter Shift Register is set to output a character of all logic 1's. FCT is reset to V_{OL} and TBMT set to V_{OH} indicating the Transmitter Holding Register is empty.</p> <p>The receiver status is initialized to a V_{OL} on RPE, SCR, and RDA. The sync character detect logic is inhibited until a RR pulse is received.</p>
(15)	D0	<p>DATA INPUTS Data on the eight data lines are loaded into the Transmitter Holding Register by \overline{TDS}, the Transmitter Fill Register by \overline{TFS}, and the Receiver Sync Register by \overline{RSS}. The character is right justified with the LSB at D0. For word lengths less than 8 bits, the unused inputs are ignored. Data transmission is LSB first.</p>
(16)	D1	
(17)	D2	
(18)	D3	
(19)	D4	
(20)	D5	
(21)	D6	
(22)	D7	
(38)	\overline{TDS}	<p>TRANSMIT DATA STROBE A V_{IL} loads data on D0-D7 into the Transmitter Holding Register and resets TBMT to a V_{OL}.</p>
(24)	\overline{TFS}	<p>TRANSMIT FILL STROBE A V_{IL} loads data on D0-D7 into the Transmitter Fill Register. The character in the Transmitter Fill Register is transmitted whenever a new character is not loaded in the allotted time.</p>
(23)	\overline{RSS}	<p>RECEIVER SYNC STROBE A V_{IL} loads data on D0-D7 into the Receiver Sync Register. SCR is set to V_{OH} whenever data in the Receiver Shift Register compares with the character in the Receiver Sync Register.</p>
(9)	TBMT	<p>TRANSMIT BUFFER EMPTY A V_{OH} indicates the data in the Transmitter Holding Register has been transferred to the Transmitter Shift Register and new data may be loaded. TBMT is reset to V_{OL} by a V_{IL} on \overline{TDS}. A V_{IH} on RESET sets TBMT to a V_{OH}.</p> <p>TBMT is also multiplexed onto the RD7 output (26) when \overline{SWE} is at V_{IL} and \overline{RDE} is at V_{IH}.</p>
(6)	TSO	<p>TRANSMITTER SERIAL OUTPUT Data entered on D0-D7 are transmitted serially, least significant bit first, on TSO at a rate equal to the Transmit Clock frequency, TCP. Source of the data to the transmitter shift register is the Transmitter Holding Register or Transmitter Fill Register.</p>
(36)	TCP	<p>TRANSMIT CLOCK Data is transmitted on TSO at the frequency of the TCP input in a NRZ format. A new data bit is started on each negative to positive transition (V_{IL} to V_{IH}) of TCP.</p>
(26)	RD7	<p>RECEIVED DATA OUTPUTS RDO-RD7 contain data from the Receiver Output Register or selective status conditions, depending on the state of \overline{SWE} and \overline{RDE} per the following table:</p>
(27)	RD6	
(28)	RD5	
(29)	RD4	
(30)	RD3	
(31)	RD2	
(32)	RD1	

MPU/ACIA INTERFACE (CONT'D)

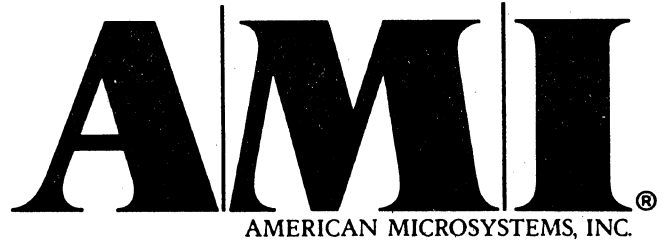
Pin	Label	Function																																																												
(33)	RD0	<table border="1"> <tr> <td>(34)</td> <td>(35)</td> <td>(33)</td> <td>(32)</td> <td>(31)</td> <td>(30)</td> <td>(39)</td> <td>(28)</td> <td>(27)</td> <td>(26)</td> </tr> <tr> <td>\overline{SWE}</td> <td>\overline{RDE}</td> <td>RD0</td> <td>RD1</td> <td>RD2</td> <td>RD3</td> <td>RD4</td> <td>RD5</td> <td>RD6</td> <td>RD7</td> </tr> <tr> <td>V_{IL}</td> <td>V_{IL}</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> <tr> <td>V_{IL}</td> <td>V_{IH}</td> <td>RDA</td> <td>ROR</td> <td>RPE</td> <td>SCR</td> <td>V_{OL}</td> <td>V_{OL}</td> <td>FCT</td> <td>TBMT</td> </tr> <tr> <td>V_{IH}</td> <td>V_{IL}</td> <td>DB0</td> <td>DB1</td> <td>DB2</td> <td>DB3</td> <td>DB4</td> <td>DB5</td> <td>DB6</td> <td>DB7</td> </tr> <tr> <td>V_{IH}</td> <td>V_{IH}</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>X</td> </tr> </table> <p>X Output is in the OFF or Tri-State condition DB0 LSB of Receiver Output Register DB7 MSB of Receiver Output Register The two unused outputs are held at V_{OL} in the output status condition.</p>	(34)	(35)	(33)	(32)	(31)	(30)	(39)	(28)	(27)	(26)	\overline{SWE}	\overline{RDE}	RD0	RD1	RD2	RD3	RD4	RD5	RD6	RD7	V _{IL}	V _{IL}	X	X	X	X	X	X	X	X	V _{IL}	V _{IH}	RDA	ROR	RPE	SCR	V _{OL}	V _{OL}	FCT	TBMT	V _{IH}	V _{IL}	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	V _{IH}	V _{IH}	X	X	X	X	X	X	X	X
(34)	(35)	(33)	(32)	(31)	(30)	(39)	(28)	(27)	(26)																																																					
\overline{SWE}	\overline{RDE}	RD0	RD1	RD2	RD3	RD4	RD5	RD6	RD7																																																					
V _{IL}	V _{IL}	X	X	X	X	X	X	X	X																																																					
V _{IL}	V _{IH}	RDA	ROR	RPE	SCR	V _{OL}	V _{OL}	FCT	TBMT																																																					
V _{IH}	V _{IL}	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7																																																					
V _{IH}	V _{IH}	X	X	X	X	X	X	X	X																																																					
(35)	\overline{RDE}	RECEIVE DATA ENABLE A V _{IL} enables the data in the Receiver Output Register onto the output data lines RD0–RD7. The trailing edge (V _{IL} to V _{IH} transition) of \overline{RDE} resets RDA to the V _{OL} condition.																																																												
(7)	FCT	FILL CHARACTER TRANSMITTED A V _{OH} on FCT indicates data from the Transmitter Fill Register has been transferred to the Transmitter Shift Register. FCT is reset to V _{OL} when data is transferred from the Transmitter Holding Register to the Transmitter Shift Register, or on the trailing edge (V _{IL} to V _{IH}) of the \overline{SWE} pulse, or when RESET is V _{IH} . FCT is multiplexed onto the RD6 output (27) when \overline{SWE} is at V _{IL} and \overline{RDE} is at V _{IH} .																																																												
(25)	RSI	RECEIVER SERIAL INPUT Serial data is clocked into the Receiver Shift Register, least significant bit first, on RSI at a rate equal to the Receive Clock frequency RCP.																																																												
(37)	RCP	RECEIVE CLOCK Data is transferred from RSI input to the Receiver Shift Register at the frequency of the RCP input. Each data bit is entered on the positive to negative transition (V _{IH} to V _{IL}) of RCP.																																																												
(12)	RDA	RECEIVED DATA AVAILABLE A V _{OH} indicates a character has been transferred from the Receiver Shift Register to the Receiver Output Register. RDA is reset to V _{OL} on the trailing edge (V _{IL} to V _{IH} transition) of \overline{RDE} , by a V _{IL} on \overline{RR} or a V _{IH} on RESET. RDA is multiplexed onto the RD0 output (33) when \overline{SWE} is V _{IL} and \overline{RDE} is V _{IH} .																																																												
(8)	SCR	SYNC CHARACTER RECEIVED A V _{OH} indicates the data in the Receiver Shift Register is identical to the data in the Receiver Sync Register. SCR is reset to a V _{OL} when the character in the Receiver Shift Register does not compare to the Receiver Sync Register, on the trailing edge (V _{IL} to V _{IH} transition) of \overline{SWE} , by a V _{IL} on \overline{RR} or a V _{IH} on RESET. SCR is multiplexed onto the RD3 output (30) when \overline{SWE} is a V _{IL} and \overline{RDE} is V _{IH} .																																																												

MPU/ACIA INTERFACE (CONT'D)

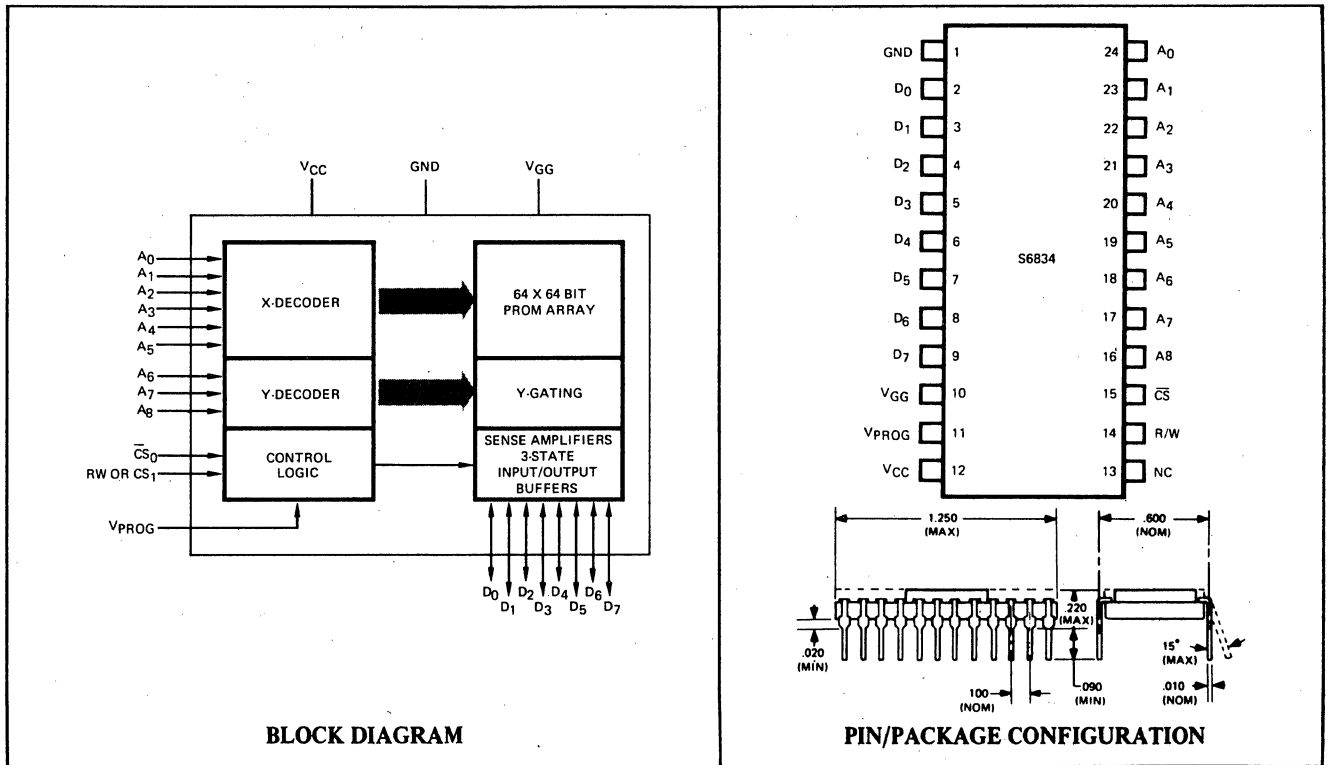
Pin	Label	Function															
(34)	$\overline{\text{SWE}}$	<p>STATUS WORD ENABLE A V_{IL} enables the internal status conditions onto the output data lines RD0–RD7.</p> <p>The trailing edge of $\overline{\text{SWE}}$ pulse resets FCT, ROR, RPE, and SCR to V_{OL}.</p>															
(11)	ROR	<p>RECEIVER OVERRUN A V_{OH} indicates data has been transferred from the Receiver Shift Register to the Receiver Output Register when RDA was still set to V_{OH}. The last data in the Output Register is lost.</p> <p>ROR is reset by the trailing edge (V_{IL} to V_{IH}) of $\overline{\text{SWE}}$, a V_{IL} on $\overline{\text{RR}}$, a V_{IH} on RESET or a V_{OL} to V_{OH} transition of RDA.</p> <p>ROR is multiplexed onto the RD1 output (32) when $\overline{\text{SWE}}$ is V_{IL} and $\overline{\text{RDE}}$ is V_{IH}.</p>															
(10)	RPE	<p>RECEIVER PARITY ERROR A V_{OH} indicates the accumulated parity on the received character transferred to the Output Register does not agree with the parity selected by POE.</p> <p>RPE is reset with the next received character with correct parity, the trailing edge (V_{IL} to V_{IH}) of $\overline{\text{SWE}}$, a V_{IL} on $\overline{\text{RR}}$ or a V_{IH} on RESET.</p> <p>RPE is multiplexed onto the RD2 output (31) when $\overline{\text{SWE}}$ is V_{IL} and $\overline{\text{RDE}}$ is V_{IH}.</p>															
(13)	$\overline{\text{RR}}$	<p>RECEIVER RESTART A V_{IL} resets the receiver section by clearing the status RDA, SCR, ROR, and RPE to V_{OL}. The trailing edge of $\overline{\text{RR}}$ (V_{IL} to V_{IH}) also puts the receiver in a bit transparent mode to search for a comparison, each bit time, between the contents of the Receiver Shift Register and the Receiver Sync Register. The number of data bits per character for the comparison is set by NDB1 and NDB2. After a compare is made SCR is set to V_{OH}, the sync character is transferred to the Receiver Output Register, and the receiver enters a word synchronous mode framing an input character each word time.</p> <p>NOTE: Parity is not checked on the first sync character but is enabled for every succeeding character.</p>															
(39)	NDB1	<p>NUMBER DATA BITS The number of Data Bits per character are determined by NDB1 and NDB2. The number of data bits does not include the parity bit.</p> <table border="1"> <thead> <tr> <th>NDB2</th> <th>NDB1</th> <th>CHARACTER LENGTH</th> </tr> </thead> <tbody> <tr> <td>V_{IL}</td> <td>V_{IL}</td> <td>5 Bits</td> </tr> <tr> <td>V_{IL}</td> <td>V_{IH}</td> <td>6 Bits</td> </tr> <tr> <td>V_{IH}</td> <td>V_{IL}</td> <td>7 Bits</td> </tr> <tr> <td>V_{IH}</td> <td>V_{IH}</td> <td>8 Bits</td> </tr> </tbody> </table> <p>For character lengths less than 8 bits, unused inputs are ignored and unused outputs are held to V_{OL}. Data is always right justified with D0 and RD0 being the least significant bits.</p>	NDB2	NDB1	CHARACTER LENGTH	V_{IL}	V_{IL}	5 Bits	V_{IL}	V_{IH}	6 Bits	V_{IH}	V_{IL}	7 Bits	V_{IH}	V_{IH}	8 Bits
NDB2	NDB1	CHARACTER LENGTH															
V_{IL}	V_{IL}	5 Bits															
V_{IL}	V_{IH}	6 Bits															
V_{IH}	V_{IL}	7 Bits															
V_{IH}	V_{IH}	8 Bits															
(3)	NPB	<p>NO PARITY BIT A V_{IH} eliminates generation of a parity bit in the transmitter and checking of parity in the receiver. With parity disabled, the RPE status bit is held at V_{OL}.</p>															
(4)	POE	<p>PARITY ODD/EVEN A V_{IH} directs both the transmitter and receiver to operate with even parity. A V_{IL} forces odd parity operation. NPB must be V_{IL} for parity to be enabled.</p>															
(5)	$\overline{\text{CS}}$	<p>CONTROL STROBE A V_{IL} loads the control inputs NDB1, NDB2, POE, and NPB into the Control Register. For static operation, $\overline{\text{CS}}$ can be tied directly to ground.</p>															

S6834

512 X 8 BIT
ERASEABLE AND
ELECTRICALLY REPROGRAMMABLE
READ ONLY MEMORY



ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM

PIN/PACKAGE CONFIGURATION

FEATURES

- On-Board Programmability
- Fast Access Time – 500 ns Typ.
- Pin Configuration Similar to the S6830
1K x 8 Bit ROM
- High Speed Programming – Less than 1 Minute for all 4096 Bits
- Programmed with R/W, CS and VPROG Pins
- Completely TTL Compatible – Excluding the VPROG Pin
- Ultraviolet Light Erasable – Less than 10 Minutes
- Static Operation – No Clocks Required
- Three-State Data I/O
- Standard Power Supplies +5V and -12V
- Mature P-Chan Process

FUNCTIONAL DESCRIPTION

The S6834 is a high speed, static, 512 x 8 bit, erasable and electrically programmable read only memory designed for use in bus-organized systems. Both input and output are TTL compatible during both read and write modes. Packaged in a 24 pin hermetically sealed dual in-line package the bit pattern can be erased by exposing the chip to an ultra-violet light source through the transparent lid, after which a new pattern can be written.

TYPICAL APPLICATIONS

- ROM Program Debugging
- Code Translation
- Microprogramming
- Look-up Tables
- Random Logic Replacement
- Programmable Waveforms
- Character Generation
- Electronic Keyboards

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} except the V_{PROG} pin	+0.3 to -20V
Voltage on the V_{PROG} pin relative to V_{SS}	+0.3 to -55V
Operating Temperature	0°C to +70°C
Storage Temperature (programmed)	-55°C to +85°C
Storage Temperature (unprogrammed)	-55°C to 150°C

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC (STATIC) CHARACTERISTICS ($V_{CC} = +5.0V \pm 5\%$, $V_{GG} = -12.0V \pm 5\%$, $T_A = 0 - 70^\circ C$ unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
V_{IL}	INPUT VOLTAGE LOW		0.8	V
V_{IH}	INPUT VOLTAGE HIGH	$V_{CC} - 2.25$	$V_{CC} - 0.3$	V
V_{OL}	OUTPUT VOLTAGE LOW $I_{OL} = 1.6 \text{ ma}$		0.4	V
V_{OH}	OUTPUT VOLTAGE HIGH $I_{OH} = 40 \mu a$	2.4		V
I_{LI}	INPUT LEAKAGE CURRENT		20	μa
I_{LO}	OUTPUT LEAKAGE CURRENT $CS = 5V$		10	μa
I_{GG}	V_{GG} SUPPLY CURRENT		45	ma
I_{CC}	V_{CC} SUPPLY CURRENT		50	ma
P_D	POWER DISSIPATION		750	mw

NOTE: Program input V_{PROG} may be tied to V_{CC} during the Read.

AC (DYNAMIC) CHARACTERISTICS (Loading is as shown in Figure 1 unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX		UNIT
			(6834)	(6834-1)	
T_{ACC}	ACCESS TIME		575	750	ns
T_{CO}	CHIP SELECT TO OUTPUT DELAY		300	400	ns
T_{DD}	CHIP DESELECT TO OUTPUT DELAY		250	325	ns

FIGURE 1 — TEST CONDITIONS

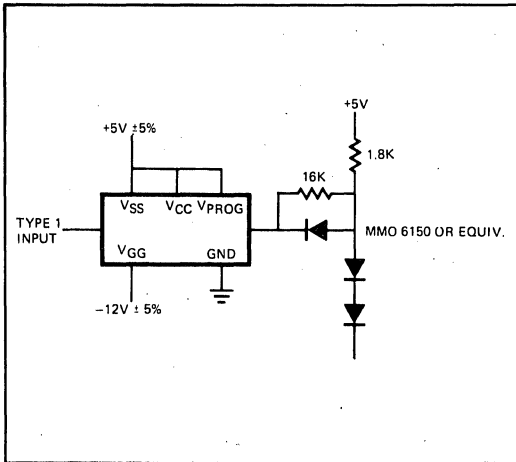
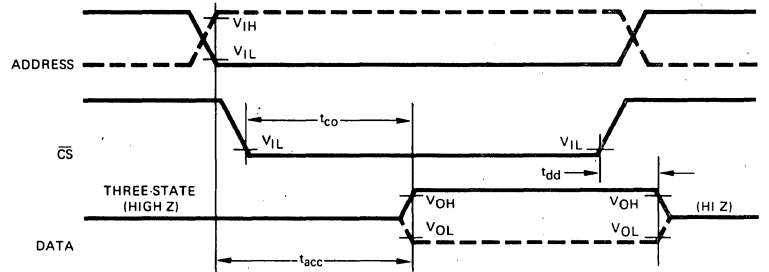


FIGURE 2 — READ CYCLE TIMING WAVEFORMS



PROGRAM CHARACTERISTICS (R/W G_{nd} , Program pulse rise and fall time (10% to 90%) are both at 1 μ s max).

SYMBOL	CHARACTERISTICS	MIN	MAX	UNIT
T_{AS}	ADDRESS SET UP TIME	10		μ s
T_{CSS}	CHIP SELECT SET UP TIME	10		μ s
T_{DS}	DATA SET UP TIME	10		μ s
T_{AH}	ADDRESS HOLD TIME	10		μ s
T_{CSH}	CHIP SELECT HOLD TIME	10		μ s
T_{DH}	DATA HOLD TIME	10		μ s
T_{PWL}	PROGRAM PULSE WIDTH LOW	3	5	ms
T_{PWH}	PROGRAM PULSE WIDTH HIGH	500		μ s
V_{PROG}	PROGRAM AMPLITUDE	-55	-50	V
I_{PROG}	PROGRAM CURRENT		35	ma
T_{WS}	WRITE SET UP TIME	10		μ s
T_{WH}	WRITE HOLD TIME	5		μ s
T_{RS}	READ SET UP TIME	10		μ s

FIGURE 3 — PROGRAMMING CYCLE TIMING WAVEFORMS

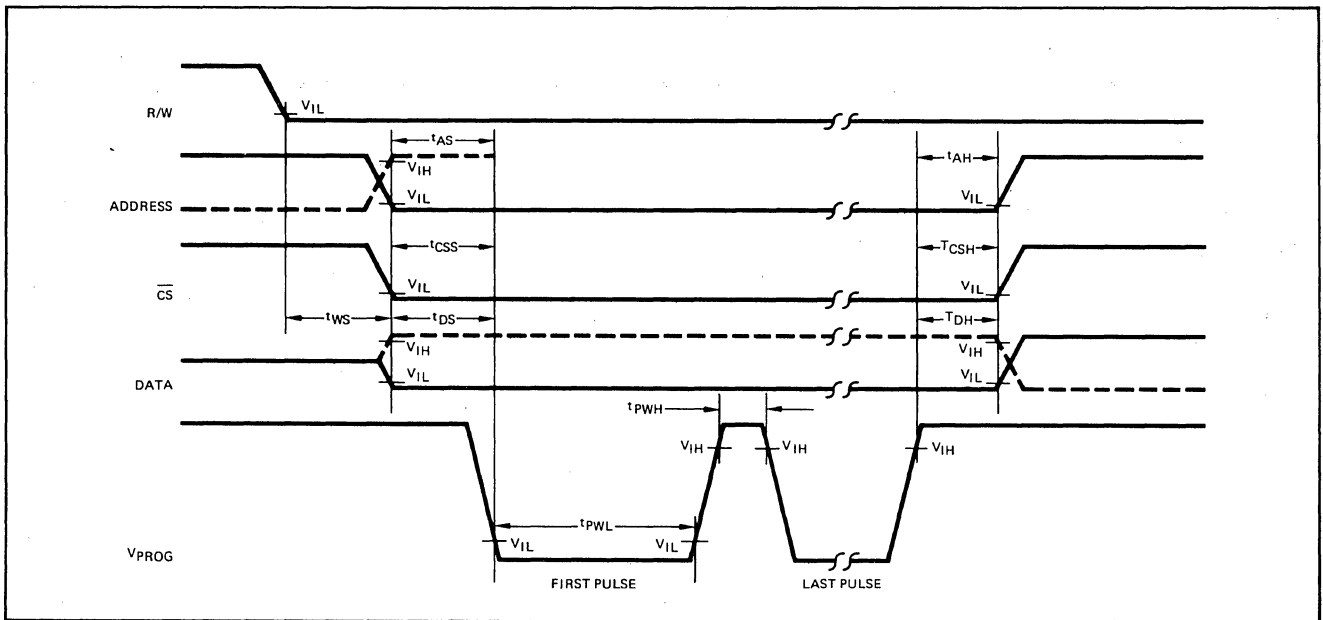
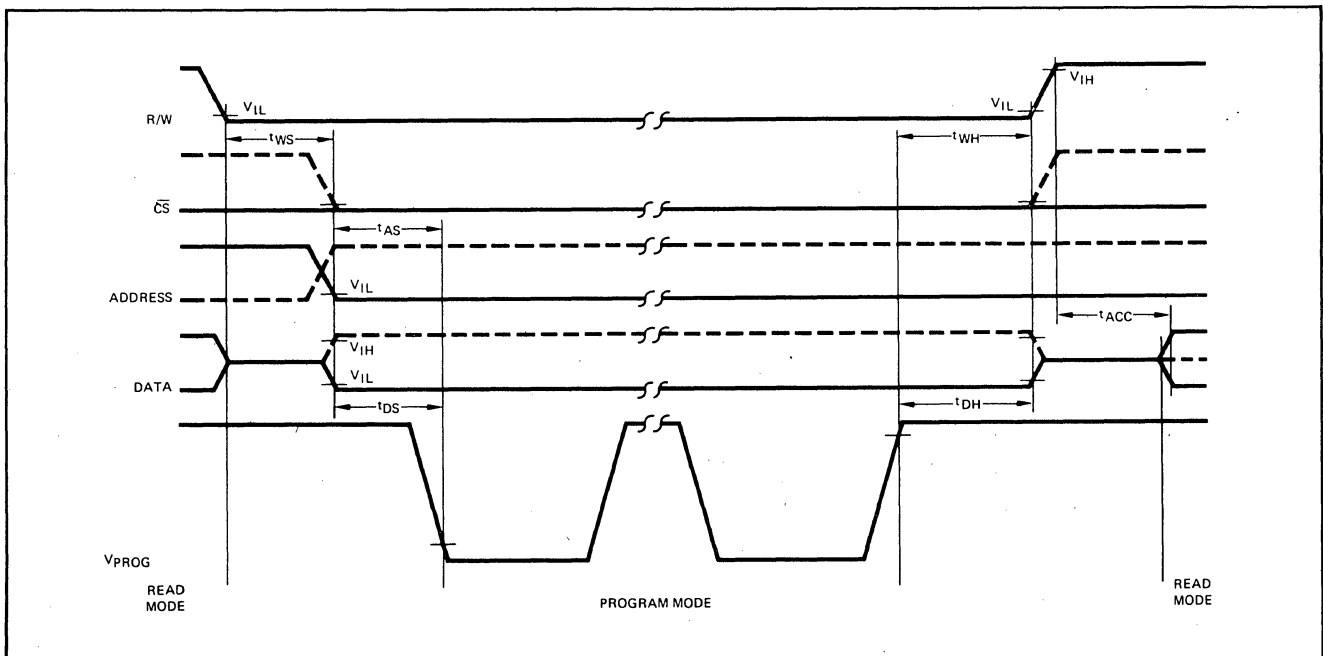


FIGURE 4 — READ/PROGRAM/READ CYCLE TIMING WAVEFORM



CONTROL FUNCTION TRUTH TABLE

CS	R/W	V _{PROG}	MODE	OUTPUTS
0	0	V _{PROG}	Write	Active Data Inputs
0	1	V _{CC}	Read	Active
1	X	X	Standby	Floating

OPERATION

Initially, and after each erasure, all bits of the 6834 are in the logic "0" state (output 0 volts). Data is stored by selectively programming a logic "1" into the desired bit locations. The R/W input (pin 14) is used to select the desired mode of operation. When the R/W input is at logic "0" the chip is in the write enable mode of operation. The outputs (O₁ - O₈) are disabled (floating) with the corresponding pins becoming the data inputs (O₁ → D_{IN 1} etc.). The word address is selected in the same manner as in the read mode. Data to be programmed are presented 8 bits in parallel and after the address and data are set up a programming pulse (V_P -50 volts) is applied. V_{PROG} electrically writes the data into the memory array. Writing may be inhibited by deselecting the chip with the CS input at a logic "1" during the write cycle. This feature allows true "on board" programming in bus organized systems where the R/W and V_{PROG} inputs are common and the device to be programmed is selected by means of the chip select input as during read operations.

The amount of program energy required to insure memory retention may be defined as a function of the number of program pulses (N) times the program pulse width (t_{pw}) (N x t_{pw} ≥ 60 msec). This means if a 3 ms pulse is used, 20 program pulses are required, and if a 5 ms pulse is used 12 program pulses are required.

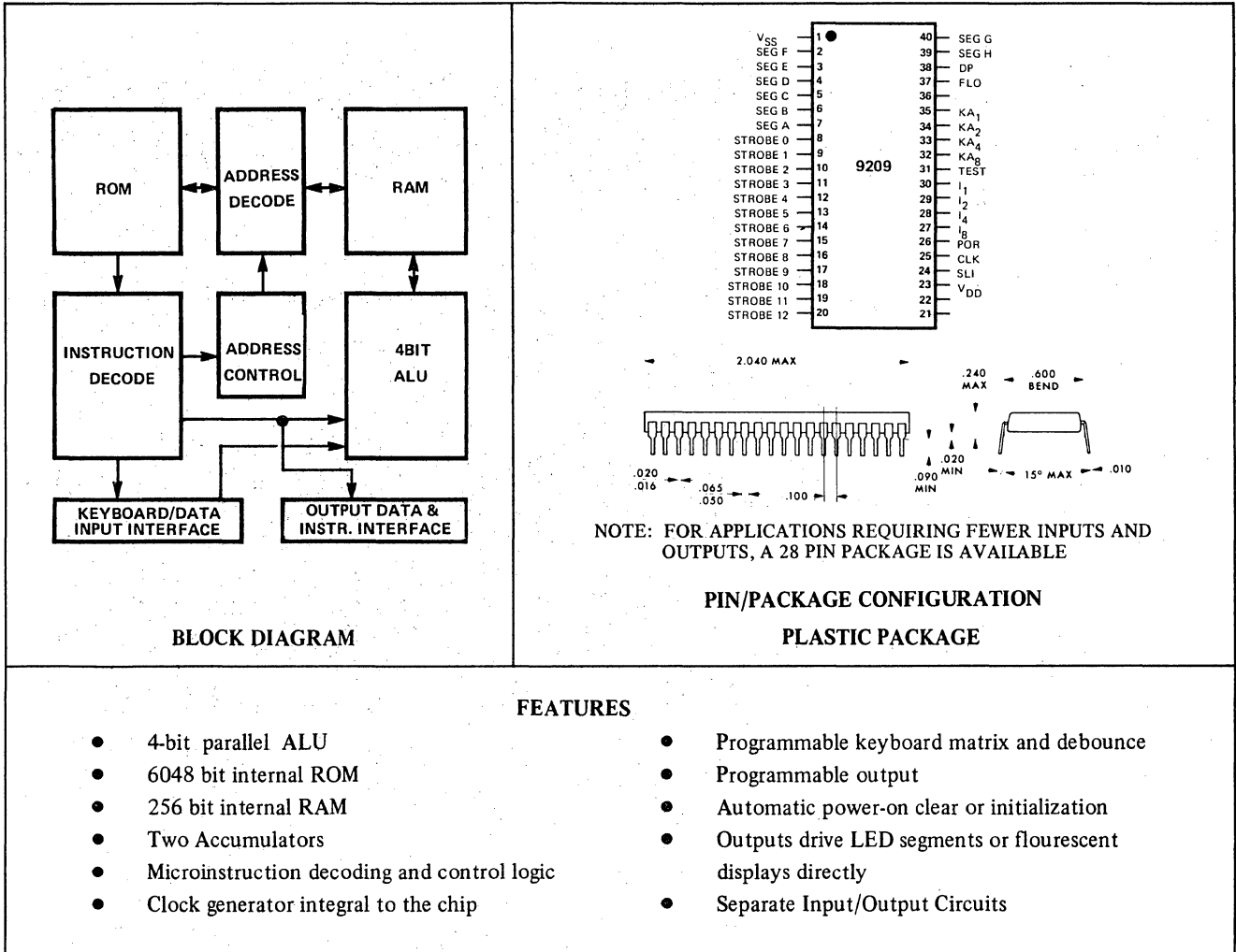
The read operation is accomplished by a logic "1" at the R/W input with the program input connected to V_{SS} potential. True data (data out = data in) is valid after the address is stable. The CS input will disable (float) the outputs when at a logic "1" to allow or tie capability.

Erasure is accomplished by exposing the array to a high intensity ultra-violet light source (such as, Ultra-Violet Products, Inc. Lamp Model S52 or UVS-54) for a period of 7 to 10 minutes. The clear optical lid should be approximately one inch away from the lamp tubes.

INTERFACE DESCRIPTION

Pin	Label	Function
(2)	D0	Data Lines - with the R/W line selected for Read (V _{IH}), the Data Lines (D0 through D7) are set to reflect the contents of the selected memory location. When the R/W line is set for Write (V _{IL}), the Data Lines are input to the addressed location of the 6834 when V _{PROG} is present. The Data Bus output drivers are three-state devices that remain in the high impedance (off) state whenever CS is in the V _{IH} state.
(3)	D1	
(4)	D2	
(5)	D3	
(6)	D4	
(7)	D5	
(8)	D6	
(9)	D7	
(14)	R/W	
(15)	CS	Chip Select - This input line must be set to V _{IL} for a Read or Write operation to be performed. When it is High (V _{IH}) the output data bus is set to a high-impedance three-state condition.
(11)	V _{PROG}	Program - In the Write mode, a programming pulse (-50V dc) at this input causes the data at the Data Lines to be stored in the selected address. This pin should be tied to V _{CC} for normal Read operations.
(24)	A0	Address Lines - These lines select the 8 bit word in memory for Read or Write operation
(23)	A1	
(22)	A2	
(21)	A3	
(20)	A4	
(19)	A5	
(18)	A6	
(17)	A7	
(16)	A8	

ADVANCED PRODUCT DESCRIPTION



FUNCTIONAL DESCRIPTION

The 9209 Microprogrammable Controller (MPC) provides a flexible method of creating a variety of calculator and display-oriented microprocessor circuits. Designed to handle numeric input/output and display of up to 12 digits, the MPC contains all the essential elements of a microcomputer on one MOS chip (see block diagram).

These elements—combined with an unusually versatile instruction set—allow the MPC to be used in a wide variety of calculator and non-calculator fixed program applications.

TYPICAL APPLICATIONS

The relatively low cost of the MPC combined with its on-chip ROM and RAM functions permits its use in a wide

variety of specialized systems requiring a nominal amount of data processing and data manipulation capability. Its area of application lies between special purpose (custom) LSI chips and standard high performance microprocessors.

The MPC can be used by itself or, with a small amount of external hardware, several may be connected in tandem for applications requiring increased capability. Figure 2 on the following page shows a typical multichip application in a high-end printing calculator using a 9209, a peripheral interface chip and a keyboard buffer chip.

Figure 3 shows the use of the 9209, a UART (Universal Asynchronous Receiver/Transmitter), and some TTL devices to implement a small terminal, used for the verification of

TYPICAL APPLICATIONS (Cont'd.)

credit sales and similar applications. All terminals in this network are periodically interrogated by the CPU and when a terminal receives its ID code (which is read in from the ID jumper matrix), it responds with "no transaction," or with the data which has been keyed in by the operator. In the latter case, the CPU responds with a discrete (OK, HOLD, WAIT, etc.) a credit limit, or other data such as a phone number to call, or a number sequence which must be given by the customer. Other applications include order entry and billing terminals.

A third application shown is the use of the 9209 MPC as the controller for a digital FM tuner. The system is capable of storing ten station frequencies and includes automatic and manual search modes. Preselected stations are called up by depressing a single pushbutton.

As station entries are made, they are checked to assure that a valid frequency entry has been made. The preselected

frequencies can be stored in the MPC's internal RAM, but normally are stored in a CMOS shift register with a separate battery supply to prevent loss of station data in the event of power failure.

In addition to the preceding, the main use of the MPC is in single and multichip calculator and counting systems. AMI offers as standard products the following calculators which use the MPC chip:

S9414 – 12 digit, five function display calculator with memory, item count, average and mark-up.

S9651 – 10 digit, 7 function "slide-rule" with scientific notation and memory, square root and reciprocals.

Examples of two of these are shown below, as a guide to the functional complexity possible with this chip.

FIGURE 1 TYPICAL KEYBOARD

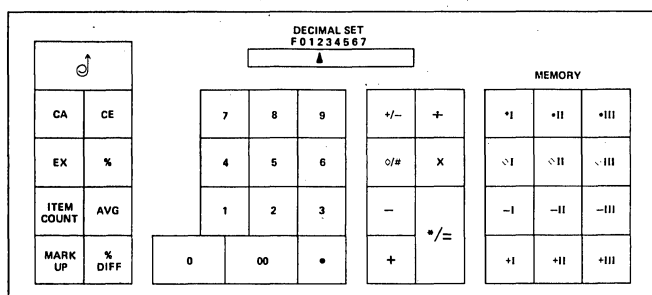


FIGURE 3 CREDIT VERIFICATION TERMINAL

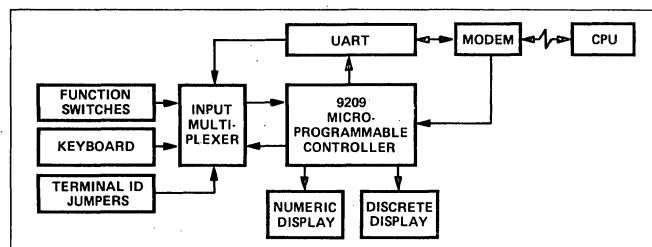


FIGURE 2 12-DIGIT PRINTING CALCULATOR SYSTEM

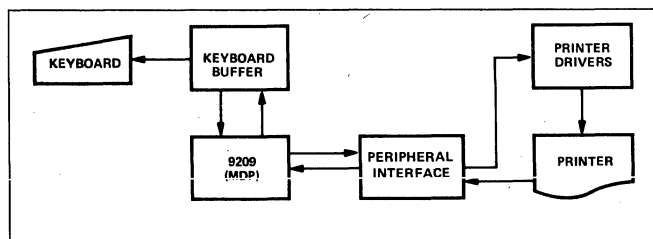


FIGURE 4 DIGITAL TUNER

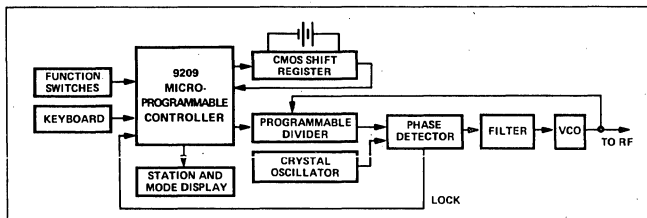
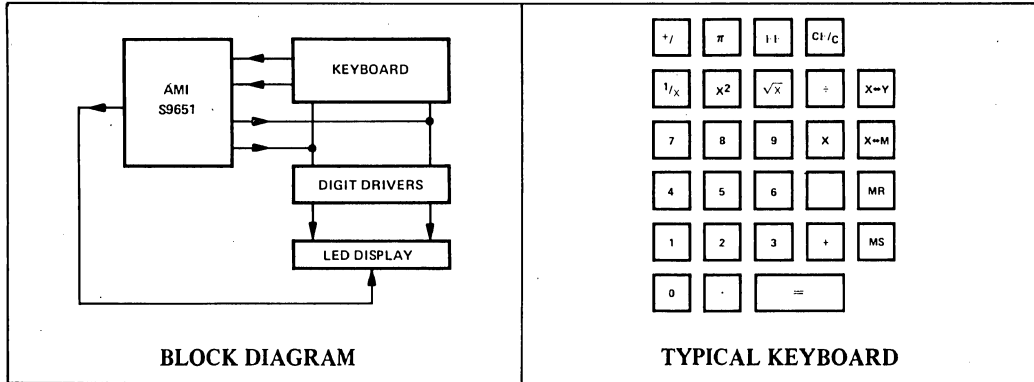


FIGURE 5 S9651 SLIDERULE CALCULATOR



DETAILED FUNCTIONAL DESCRIPTION

The detailed block diagram shows the major functional parts of the MPC. These are:

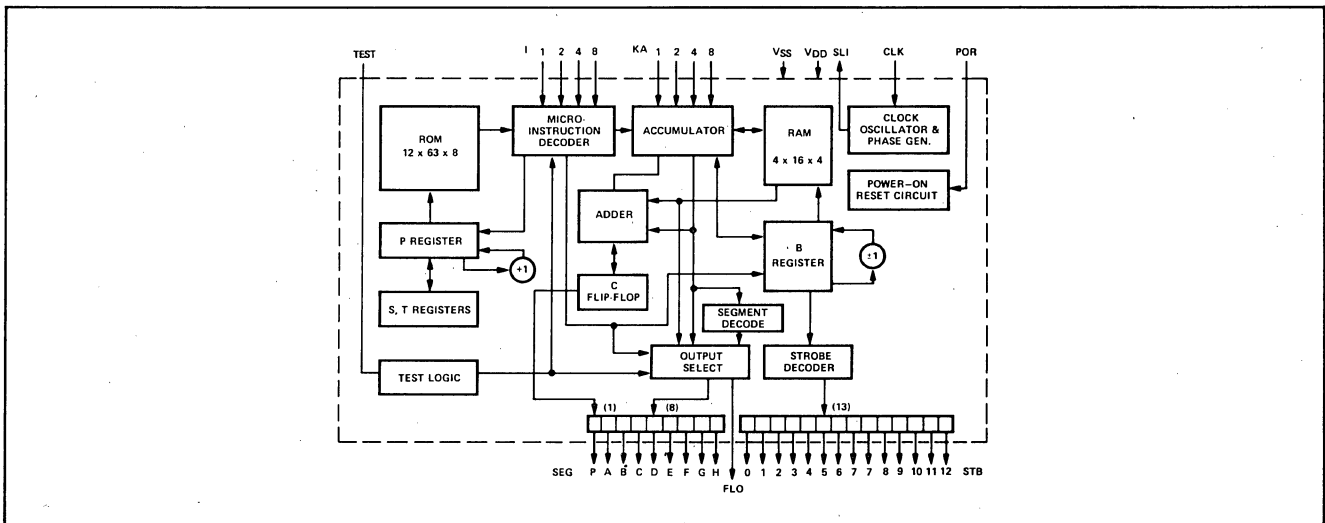
- A 6048-bit ROM containing microinstructions (12 x 63 x 8 organization).
- A 256-bit RAM memory for storing information (4 x 16 x 4 organization).
- A 4-bit parallel binary adder.
- Two 4-bit accumulators.
- A 6-bit RAM address register.
- A 10-bit ROM address register.
- Microinstruction decoding and control logic.
- A polynomial counter for incrementing the ROM address register.

- Two 10-bit address save registers.
- Input and output circuits.

The MPC is programmed by using microinstructions coded into the ROM. The ROM is organized into twelve "blocks" or "pages" each containing 63 words, which are addressed by the upper four bits of the address register. The lower 6 bits address the specific 8-bit word in each block.

The ROM addressing system consists of the P, S and T registers, each composed of an upper four bits and a lower six bits, a 6-bit polynomial counter, and two address control flip-flops. Normally, the polynomial counter is incremented once each instruction cycle and its contents transferred to the PL register to address the next ROM instruction. The counter can also be set to a specific starting address. The S and T registers form a stack used for storing return addresses when calling subroutines. The "pushing" and "popping" of the stack is controlled by the program.

FIGURE 6 9209 MPC DETAILED BLOCK DIAGRAM



DETAILED FUNCTIONAL DESCRIPTION (Cont'd.)

The RAM is used for storage of information in the processor. It is organized as four registers each containing sixteen 4-bit words. Data in the RAM can be loaded into the accumulator, exchanged with the accumulator, added to the accumulator or compared to the accumulator. Individual bits of the RAM can also be set, reset, and tested.

The adder is a parallel 4-bit binary adder having a carry input from the C flip-flop and two data inputs. The sum output is stored in the accumulator. The carry output can be stored in the C flip-flop and can be used by the control logic to skip microinstructions.

The main accumulator is a 4-bit register which can be loaded from the RAM, from the data input lines, from the ROM, from the adder or from the second accumulator. The latter is also a 4-bit register which can be loaded from the RAM.

The MPC also contains thirteen strobe outputs, which are under program timing and control. These outputs can be used for sampling a keyboard and/or driving a display. Segment data outputs for a display, four discrete data inputs, and an input for binary data into the accumulator are also available. Optionally data can be output in binary, together with a data sampling pulse (FLO) for external use.

Also included are an internal oscillator, clock generators, and a power-on initializing circuit.

INSTRUCTION SET

The MPC operation is programmed by use of instructions stored in the ROM. The instruction set includes arithmetic, load, test and flag, addressing, and miscellaneous groups, and is summarized in the table below. The instructions operate on digits (4 bits) or individual bits of the data stored in the RAM. Register handling instructions can be implemented by the use of subroutines.

The nominal instruction cycle time is 15 usec. All instructions are executed in one cycle, with the exception of transfer and return instructions, which require two cycles.

There are also several mask programmed options which control the operation of hardware portions of the chip and which define parameters for the instructions. These include coding of the segment ROM and specifying the register length for register operations.

9209 INSTRUCTION SET SUMMARY**ARITHMETIC**

ADD
ADD WITH CARRY
ADD IMMEDIATE
COMPLEMENT

LOAD A

LOAD IMMEDIATE
LOAD FROM RAM
EXCHANGE WITH RAM
EXCHANGE AND INCREMENT POINTER
EXCHANGE AND DECREMENT POINTER
LOAD FROM K INPUTS
LOAD FROM POINTER
LOAD FROM A2

TEST AND FLAG

SET, RESET, TEST C
SET, RESET, TEST BIT OF RAM
TEST A EQUAL RAM
TEST DISCRETE INPUTS
TEST KEY DOWN

ADDRESSING

JUMP
JUMP TO SUBROUTINE
JUMP TO MACROROUTINE
RETURN
RETURN AND SKIP
LOAD PAGE REGISTER

MISCELLANEOUS

SET POINTER
LOAD POINTER FROM A
LOAD STROBE OUTPUT
LOAD SEGMENT OUTPUTS FROM DECODE ROM
LOAD SEGMENT OUTPUTS FROM A AND RAM

PROGRAMMING SUPPORT

The following aids are available to assist in microprogram development for the MPC.

- Detailed hardware description and programming guide.
- Computer simulator.
- Cross-Assembler.

- Hardware simulator.
- Sentry test program generator.

The hardware and software simulators both include diagnostic capabilities to assist the debugging of microprograms. All software runs on AMI's internal B6700 computer system.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (All voltages measured with respect to V_{SS})

	Min.	Max.	Units
Storage Temperature	-55	+125	°C
Operating Temperature	0	+70	°C
Maximum Positive Voltage (any pin)		+0.3	V
Maximum Negative Voltage (any pin)		-30	V
Maximum Output Current (Segments)		11	mA
Maximum Output Current (Strobes)		5	mA

ELECTRICAL CHARACTERISTICS: $V_{DD} = -15 \pm 1V, T_A = 0 - 55^\circ C$ (All voltages measured with respect to V_{SS})

	Min.	Typ.	Max.	Units
Input High Level (Note 1)	-1.8		V_{SS}	V
Input Low Level (Note 1)	V_{DD}		-4.6V	V
Output High Level: (Note 6)				
Seg A - Seg H, DP; $I = 6.5$ mA	-3.0		V_{SS}	V
SO - S12, $I = 2.8$ mA; FLO, SL1, $I = 1.0$ mA	-1.5		V_{SS}	V
Output Low Current; $V_O = -10V$			25	μA
Supply Current		6.6	10.0	mA
Power Dissipation (Note 2)		100	160	MW
Power Reset Capacitor (Note 3)		560		pF
Oscillator Timing Resistor (Note 4)		24		K Ω
Oscillator Timing Capacitor (Note 5)		100		pF

NOTE 1. Inputs I1 - I8, KA1 - KA8. Each of these inputs has an internal resistor to V_{DD} . $R_{MIN} = 125$ K Ω .

NOTE 2. Does not include power dissipated in digit and segment drivers.

NOTE 3. Connected between POR pin and V_{SS} .

NOTE 4. Connected between CLK pin and V_{DD} .

NOTE 5. Connected between CLK pin and V_{SS} .

NOTE 6. All outputs are open drain MOS transistors to V_{SS} .

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FAIRCHILD

F8

MICROPROCESSOR

THINK F8 UNIVERSAL STANDARD MICROPROCESSOR

VERSATILE .. EFFICIENT .. COST EFFECTIVE

The ultimate goal, from F8 design concept through development and production, was to produce the most versatile, efficient, cost-effective microprocessor system available today. To accomplish this, five stringent parameters, based on user experience with other systems, were set forth as guidelines for the F8.

- Minimum Parts Count
- Cost Effectiveness
- Simple Peripheral Interfaces
- Easy Expansion through Modular Architecture
- Simplified Programming and Debugging

HOW WERE F8 GOALS MET ?

By . . . *unique system partitioning* the system functions have been divided among the various circuits of the F8 family to provide sophisticated modularity. As a result, it is now possible to build a minimum microprocessor system with only two devices. To this system PSU, RAM and I/O devices can be added to form medium size or memory intensive systems with a minimum use of external parts. And, finally, for

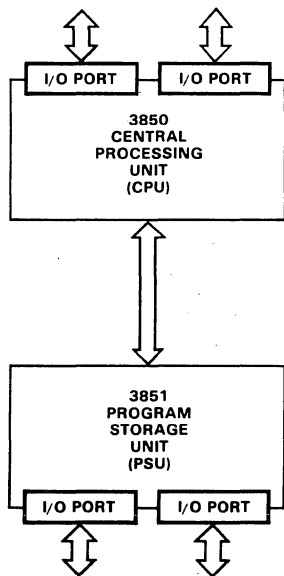
solving complex problems, the F8 devices can be connected as subsystems into a synergistic system of independent microprocessors.

By . . . *incorporating the I/O structure on the chips* so that the majority (95%) of the peripheral devices can be directly controlled without the need for special circuits. The trick is to accommodate the characteristics of a given peripheral device in the software. The I/O hardware structure includes a programmable timer, an efficient interrupt system and bidirectional I/O ports.

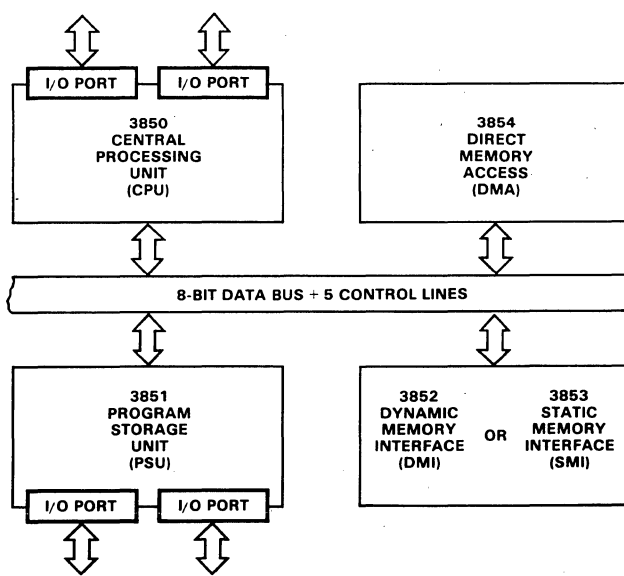
By . . . *providing carefully thought out software* for generating and debugging microprograms and a choice of three hardware modules for speeding up prototype development.

WHAT IS THE RESULT ?

. . . *a complete family of LSI circuits* that can be used as building blocks to construct versatile, efficient, cost effective systems from the most simple to the highly complex.



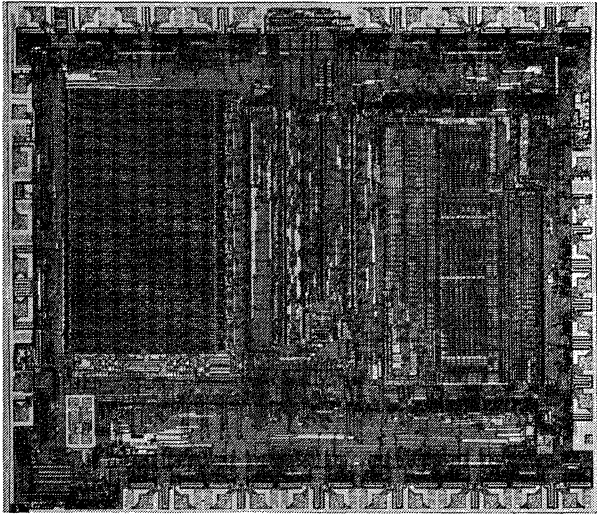
MINIMUM SYSTEM



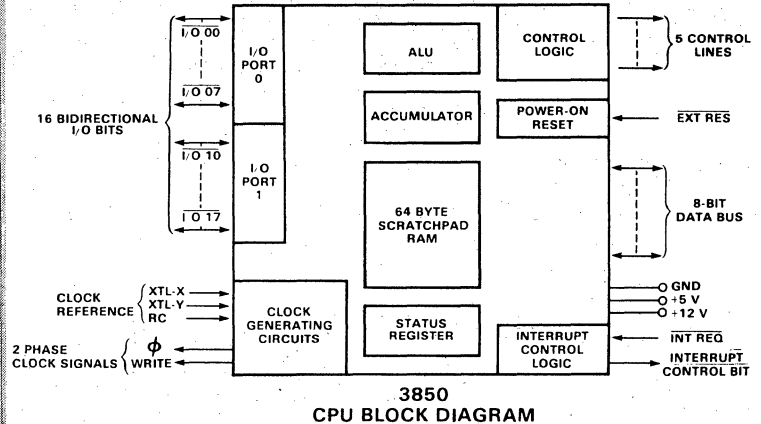
F8 DEVICE FAMILY

3850 CENTRAL PROCESSING UNIT

Fairchild's F8 Central Processing Unit (CPU) contains all of the functions of an ordinary central processor and adds some



time and money saving features uniquely its own. For instance, the 64 bytes of scratchpad RAM memory already included on the F8 CPU eliminate the need for external RAM circuits in many applications. Clock and power-on-reset circuitry, normally requiring additional integrated circuit packages, are included on-chip. Fairchild's CPU also contains 16 bits of fully bidirectional input and output lines internally latched (for storing output data) and capable of driving a standard TTL load.

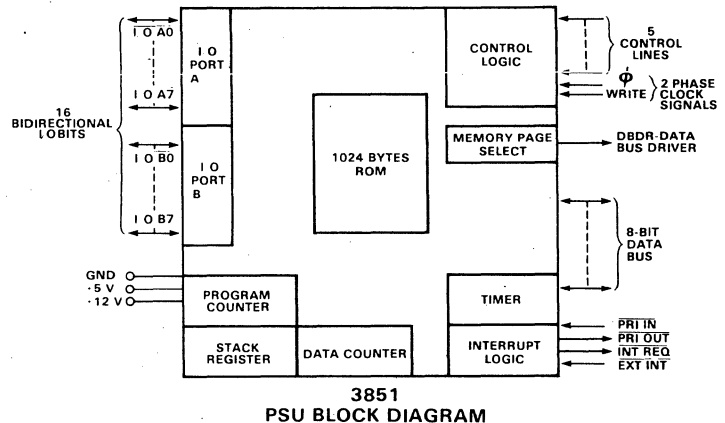
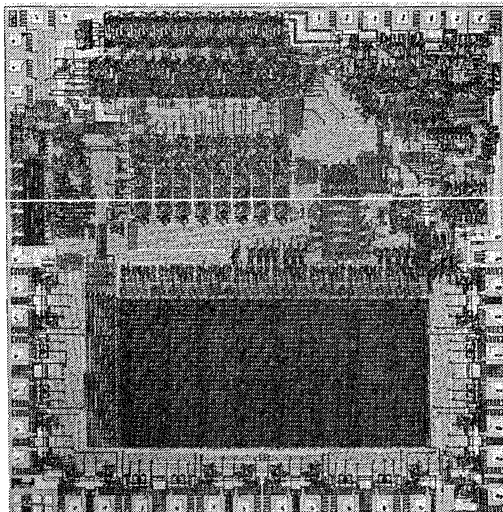


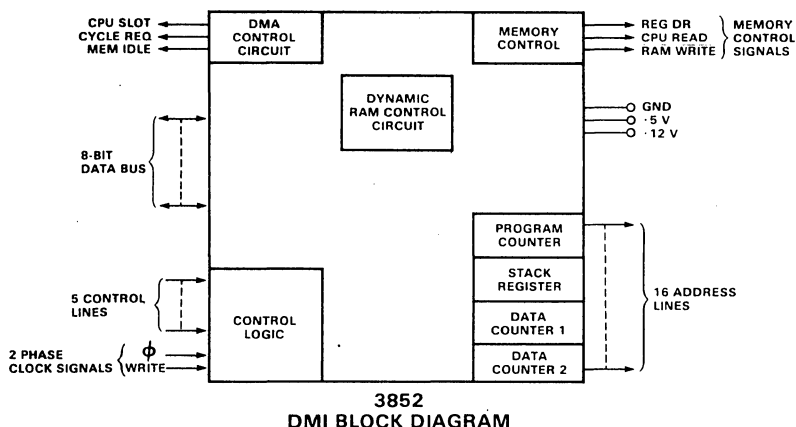
3851 PROGRAM STORAGE UNIT

It is important to note that Fairchild's Program Storage Unit (PSU) is not just a conventional Read Only Memory. In addition to containing 1024 bytes of mask programmable ROM for program and constant storage, the F8 PSU includes the

addressing logic for memory referencing, a Program Counter, an Indirect Address Register (the Data Counter) and a Stack Register. A complete vectored interrupt level, including an external interrupt line to alert the central processor, is provided. All of the logic necessary to request, acknowledge and reset the interrupt is on the F8 PSU. The 8-bit Programmable Timer is especially useful for generating real time delays. The PSU has an additional 16 bits of TTL compatible, bidirectional, fully latched I/O lines.

Systems requiring more program storage may be expanded by adding more PSU circuits. For example, one F8 CPU and three F8 PSUs will produce a microprocessor system complete with 64 bytes of RAM, 3072 bytes of ROM, 64 I/O bits, three interrupt levels, and three programmable timers. This complete system will require only four IC packages.

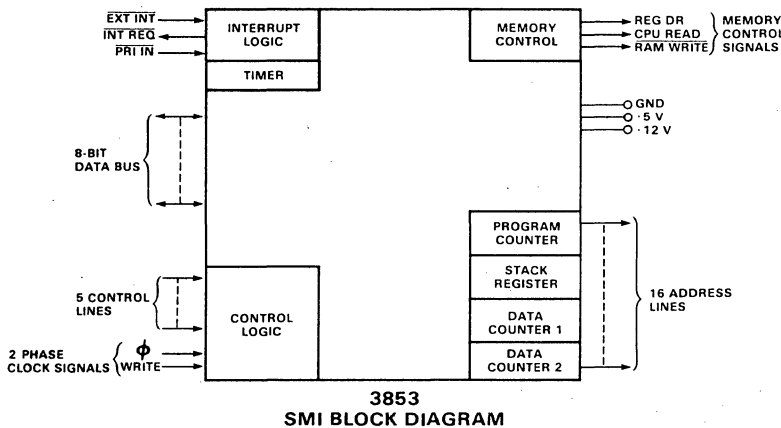




3852
DMI BLOCK DIAGRAM

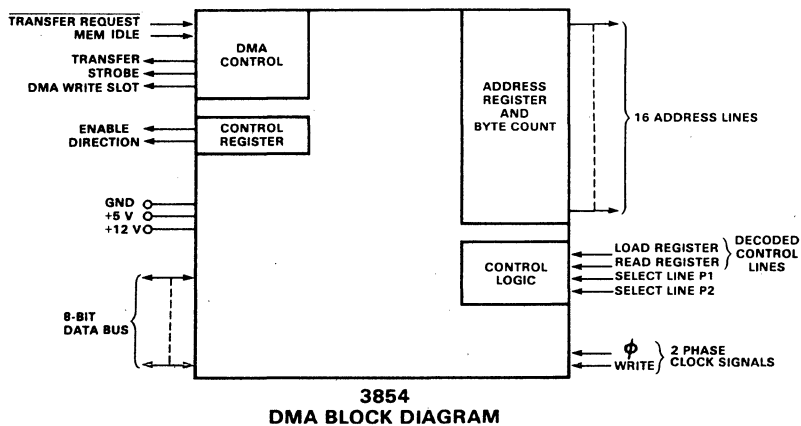
3852/3853 MEMORY INTERFACE

For applications requiring more than the 64 byte RAM located on the CPU, two memory interface circuits are included in the F8 set. Each device generates the 16 address lines and the signals necessary to interface with up to 65K bytes of RAM, PROM or ROM memory. Either device may be used in conjunction with standard static semiconductor memory devices.



3853
SMI BLOCK DIAGRAM

The Static Memory Interface (SMI) contains a full level of interrupt capability and a programmable timer. The Dynamic Memory Interface (DMI) contains all of the logic necessary to refresh MOS dynamic memories without degrading the system throughput time. The F8 DMI can also interface with static memories when desired.



3854
DMA BLOCK DIAGRAM

3854 DIRECT MEMORY ACCESS

Fairchild's Direct Memory Access (DMA) device sets up a high speed data path to link F8 memory with peripheral electronics. The F8 DMA circuit, when working in conjunction with the F8 DMI, does not require overhead electronics to keep track of memory addresses, bytes transferred and handshaking signals. The data transfer is initiated by the CPU under program control. Once started, the DMA transfer will continue without CPU intervention. The CPU can sense the enable line of the DMA to determine the completion of a transfer. The entire DMA transfer will take place without halting the central processor.



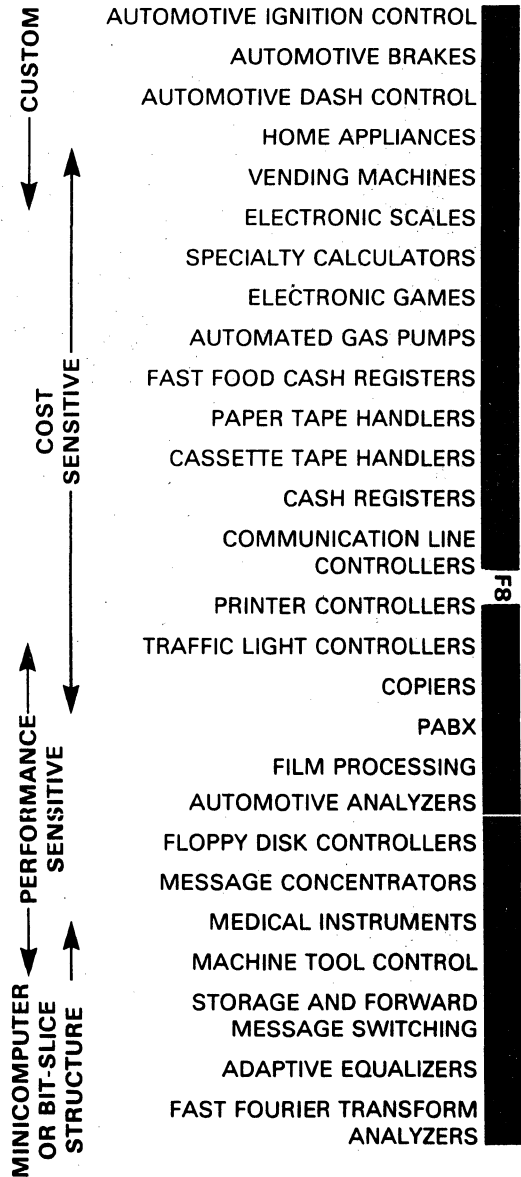
F8 MICROPROCESSOR APPLICATION SPECTRUM

Because of its unique system partitioning, the F8 device set can be applied across a wide range of applications. The minimum two-circuit system is the basis for a modular architec-

ture that can handle increasingly complex problems. A system of medium complexity can be designed by adding more F8 PSUs. The use of an F8 memory interface device allows up to 65K bytes of standard memories to be incorporated into the F8 system. For highly complex applications, independent F8 subsystems can be connected into a multiprocessing system in which each subsystem can operate independently yet can be controlled by one CPU that is the coordinator.

Fairchild

MICROPROCESSOR



A TWO-CIRCUIT SYSTEM

The two-circuit F8 microprocessor is suitable for small data terminals, controllers, and specialty calculators. The keyboard is connected directly to the F8 I/O ports without special interfaces. Switch-bounce protection, rollover, and key encoding are all under software control. Software also decodes signals for LED readouts.

As an appliance controller, for example, the two-circuit system can perform all input-output sensing, actuating, timing, and computation operations. A system like the combination washing-machine-and-dryer controller in *Figure 1* requires more than 250 components when other microprocessor device sets are used, but with the F8 devices uses only 55 components, including 28 LEDs and the power semiconductor devices and relays used to control the motors. A set of custom circuits would also require about 50 parts, but initial engineering expense is heavy and severe penalties are incurred if changes are required. With the F8 system changes can be made by merely changing the program.

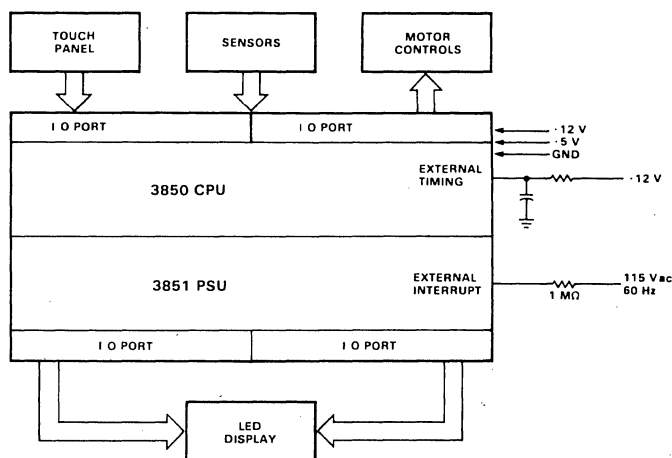


Fig. 1. Two-Circuit System

A MORE COMPLEX SYSTEM

The versatility of the F8 system is indicated by the traffic-light-controls system in *Figure 2*. The use of one CPU and two PSU circuits provides the designer with two timers, two interrupts, an onboard clock, onboard power-on reset, onboard switch decoding, and 48 bidirectional I/O bits. This system could be tied to vehicle detectors in the road, to monitor traffic for left-turn lanes as well as through-traffic flow in four directions. It would also react to interrupts from the pedestrian control buttons at each corner. There also is sufficient I/O capability to permit communication with and control of neighboring intersections and to allow the system to be operated manually or tested for proper operation.

Five F8 features are of particular interest for this type of application. One of the interrupts can eliminate the need for

such external circuits as a comparator to compare a count of the cars with a predetermined value to cause the light to change. (The CPU can handle the simple arithmetic of counting cars.) This interrupt also eliminates the need for continuous polling of traffic count by the microcomputer. The second interrupt would be ideal for permitting pedestrian control to override the automatic system. The internal clock, with an external crystal, can also control light routines.

The two timers permit simultaneous counting of delay for vehicle signals and flashing warning lights for pedestrians. The onboard power-on reset acts in case of power failure to start the system automatically when power is renewed. The bidirectional I/Os have built-in latches that eliminate the need for external latches for the job of "holding" commands for lights as well as the momentary commands provided by timers and sensors.

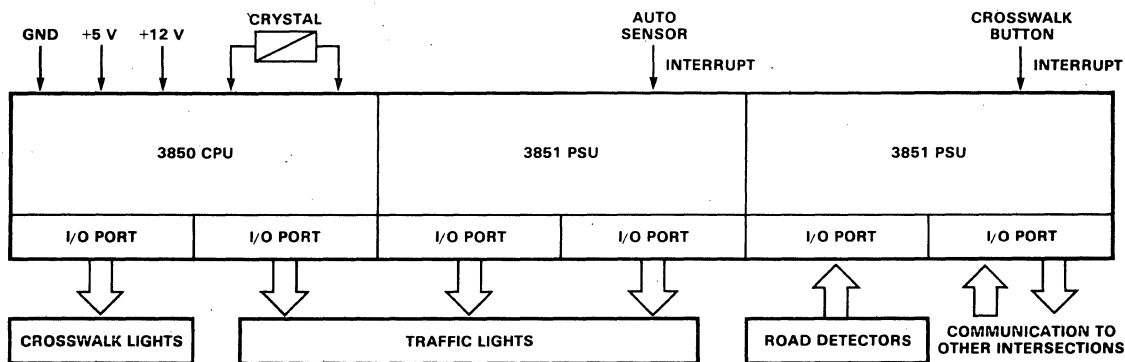


Fig. 2. Medium Complexity System

A MEMORY INTENSIVE SYSTEM

A typical application is a printing credit-verification terminal (Figure 3). Such a system requires high performance and yet must be low in cost if it is to reach a large market. Only four different F8 devices are required to handle a keyboard input, visual display, card reader, and printer as well as provide a

modem interface and memory interface for external RAM storage. This printing credit-verification system might be compared to a "bare mini-computer" in terms of utility; however, a detailed engineering evaluation would show that it costs less, has fewer parts and a more flexible I/O structure.

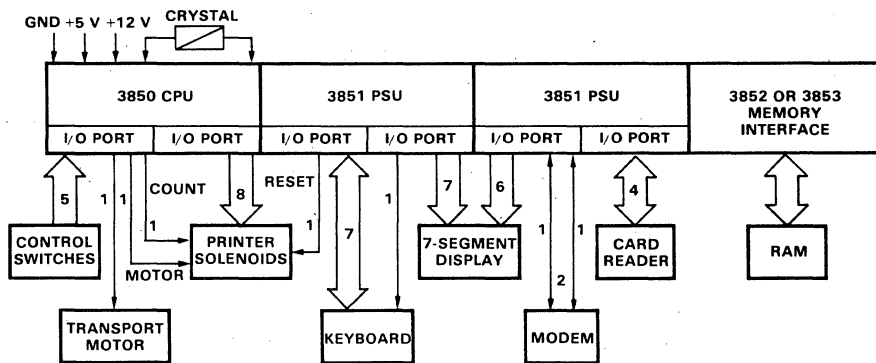


Fig. 3. Memory Intensive System

MULTI-MICROPROCESSOR SYSTEM

Figure 4 shows a specific application of the multi-processing concept as applied to a keyboard-to-floppy-disk system. Possibly this is the most cost-effective way of implementing this system, conservatively costing less than 50% of a conventional implementation. This system involves concurrent operation of three floppy disks, magnetic tape, CRT, keyboard, printer, and modem. While the low-speed devices (the keyboard, printer, and modem) can be adequately handled by the programmed I/O structure, the high-speed devices (disks, mag-

netic tape, and CRT) require separate F8 CPUs and PSUs.

This scheme provides simplicity of control, modularity, and freedom to expand. In this case, the units operating concurrently are: one magnetic-tape unit (25 μ s/byte); three floppy-disk units (32 μ s/byte each); and a CRT unit (71 μ s/byte). This combination requires an aggregate bandwidth of 0.1478 byte/ μ s. This is well within the F8's upper bandwidth limit of 0.5 byte/ μ s.

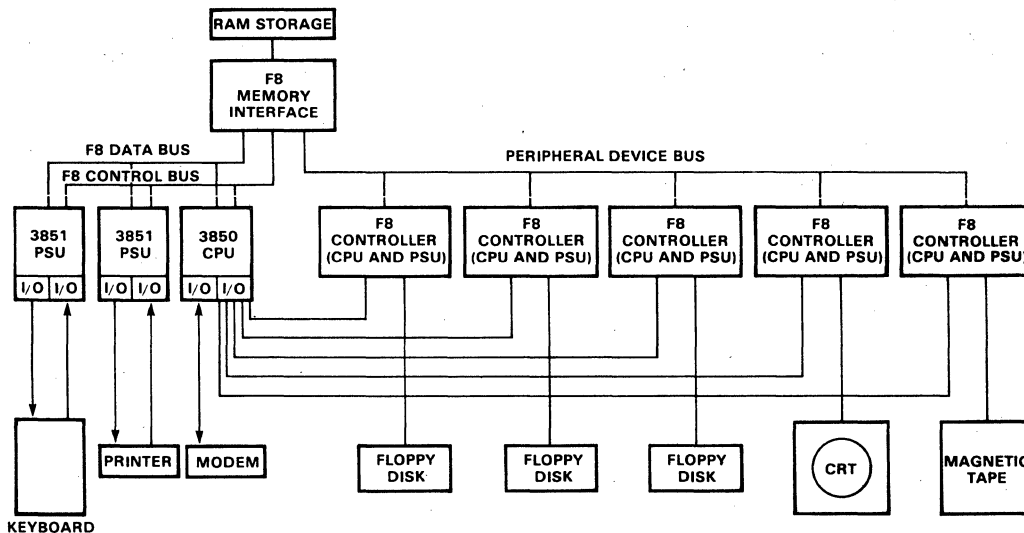


Fig. 4. Multi Microprocessor System

F8 MICROPROCESSOR SUPPORT DOCUMENTATION

F8 MICROPROCESSOR PROGRAMMER'S GUIDE

Provides tutorial instruction on microprocessor programming in general and, in particular, describes how to program Fairchild's F8 Microprocessor.

F8 CIRCUIT DATA BOOK

Provides electrical parameter data for all Fairchild F8 Microprocessor devices.

F8 TIMESHARE OPERATING SYSTEMS MANUAL

Explains how to assemble and debug F8 Microprocessor programs on NCSS and GE Timeshare Networks.

F8 CIRCUIT REFERENCE MANUAL

Describes the interactive timing and signal sequences which occur between devices in the F8 Microprocessor family.

F8S AND F8SEM USERS MANUALS

Describe how to assemble and debug microprocessor programs on the F8S and F8SEM hardware modules.

F8 FORMULATOR USERS AND REFERENCE MANUALS

Describe how to use and maintain Fairchild's F8 Formulator developmental hardware.

F8 MICROPROCESSOR DEVELOPMENT SUPPORT HARDWARE

Development support hardware is an integral part of Fairchild's F8 Microprocessor product concept. Fairchild's Microprocessor Support Engineering Group has developed an extensive set of design aids to enable customers to shorten their development cycle time and speed up programming. The F8 development support hardware provides a working model of the user's system and facilitates:

- Evaluation of F8 Microprocessor hardware operation
- Reduction of engineering time and development costs
- Preparation of system software and firmware programs
- Reduction of system hardware, software and firmware evaluation and debug time

F8 MICROPROCESSOR EVALUATION KIT

The lowest cost method for quick evaluation of the operation of the F8 Microprocessor hardware. Comes complete with a preprogrammed debug ROM device, PC card, complete instructions on the operation of all devices in the kit and all pertinent F8 literature.

F8M – MICROMODULE

A complete printed circuit subassembly capable of demonstrating the operation of a customer's program. Comes complete with F8M User's Manual and all pertinent F8 literature.

F8S – DEVELOPMENT MODULE

A complete printed circuit subassembly capable of developing, debugging and demonstrating the operation of a customer's program. Comes complete with F8S User's Manual and all pertinent F8 literature.

F8SEM – SYSTEM EXPANSION MODULE

A printed circuit subassembly designed to be used with the F8S Development Module to expand the system memory in 4K byte increments, and to expand the number of I/O ports in increments of four each.

F8SPDM – DEVELOPMENT MODULE SET

A combination set of modules containing one F8S Development Module, two F8SEM System Expansion Modules, an F8S Native Assembler, F8S and SEM User's Manuals and all other pertinent F8 literature. A more economical solution for the user requiring the expansion modules.

F8 FORMULATOR – COMPLETE MICRO- PROCESSOR DEVELOPMENT SYSTEM

A benchtop self-contained, modularized F8 development system, complete with front panel controls, cabinet, power supply, resident assembler and text editor, complete F8 Formulator Operating and System Reference manuals, and all other pertinent F8 literature.

F8 MICROPROCESSOR EVALUATION KIT

Fairchild's Microprocessor Evaluation Kit is designed for use by engineers, scientists and technicians in order to provide a straightforward method for constructing, using and evaluating prototype F8 microprocessor systems in real applications or training situations. It provides all of the semiconductor components, technical specifications, and instructions necessary to interconnect devices, demonstrate microprocessor programs up to 1K bytes in length, and to debug those programs.

The F8 Microprocessor Evaluation Kit contains the following semiconductor parts and documentation:

- 16 Semiconductor Devices, including
 - 1 - 3850 Central Processing Unit
 - 1 - 3851A* FAIR-BUG Programmed Storage Unit
 - 1 - 3853 Static Memory Interface
 - 8 - 2102-2 1K Static RAM Devices

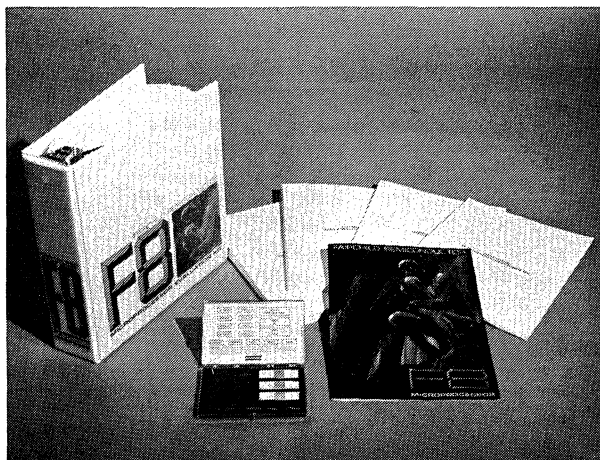
*The 3851 FAIR-BUG PSU is a fixed programmed Fairchild 3851 PSU which provides the programmer with all its I/O subroutines and allows the programmer to display or alter memory and register contents via a teletype terminal.

- 1 - 34001
 - 2 - 340097
 - 1 - 34023
 - 1 - 9N06 TTL Hex Inverter
- } CMOS Gates and Buffers

- 1 PC Card to Facilitate Device Hook-up
- F8 Microprocessor Brochure
- F8 Design Evaluation Kit Instruction Manual
- A Guide to Programming the Fairchild F8 Microprocessor
- F8 Microprocessor Data Book
- F8 Timesharing Systems Operators Guide

The F8 Microprocessor Evaluation Kit is available now from your local Fairchild Franchised Distributor.

Unit Price: \$295.00



F8M - MICROMODULE

The F8M Micromodule is an inexpensive prototyping subassembly for the development and breadboarding of F8 Microprocessor designs. It is a complete printed circuit subassembly, requiring only the addition of power supplies and connection to a teletypewriter to become fully operational.

Features of the F8M include:

- Switches and LEDs Provide Control and Monitor Functions
- 1K Bytes of Static MOS RAM
- Sockets for 2K Bytes of Bipolar PROM (Fairchild 93426)
- 2 Preprogrammed 93426 Devices Forming a Bootstrap Loader
- External Interrupt

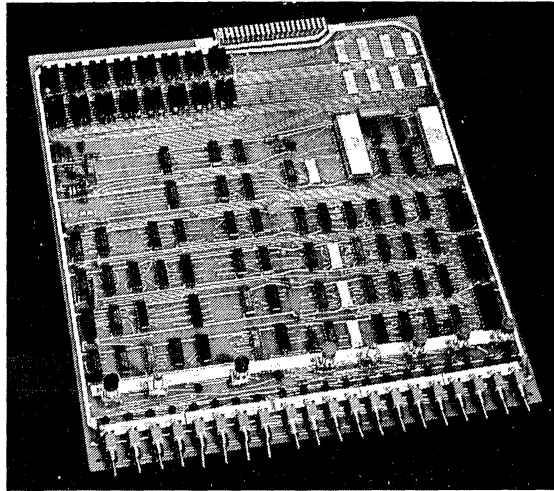
- 4 I/O Ports Available on the Edge Connector
- Programmable Interval Timer
- Serial Communications interface, RS232 Format, 20 mA Current Loop

The customer's system is ready to demonstrate after the connection of peripheral circuits and either loading an object program into the RAM, or plugging in preprogrammed PROMs. The program can be halted and single-stepped to demonstrate statically how the design functions. Any PROM or ROM memory location can be monitored by halting the program. RAM memory locations can be altered before resuming operation of the system.

The F8M is supported by a Cross Assembler available for purchase from Fairchild Semiconductor or through a National Timesharing Network. Contact your Fairchild Sales Representative for more information.

The F8M Micromodule is available off the shelf for immediate delivery from your Fairchild Franchised Distributor.

Unit Price: \$850.00



F8S – DEVELOPMENT MODULE

The F8S is an inexpensive F8 development and debugging subassembly. A self-contained complete printed circuit module, the F8S needs only power supply and connection to a teleprinter and the customer's peripheral circuits to form a complete F8 microcomputer system. Memory may be expanded to a maximum of 64K bytes with the system expansion modules described elsewhere in this brochure.

Features of the F8S include:

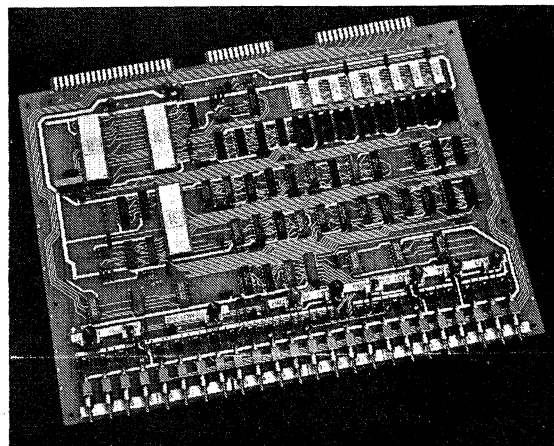
- Switches and LEDs Provide Control and Monitor Functions
- 64K Bytes of Addressable Memory Space (1K of Semiconductor Static RAM is Provided)
- Sockets for 2K Bytes of Bipolar PROM (Fairchild 93446)
- 2 External Interrupts
- 2 Programmable Interval Timers
- 4 Input/Output Ports (8 Bits Each)
- FAIR-BUG* Debugging Program

The F8S Development Module, with System Expansion Modules, allows source programs to be assembled inexpensively at the customer's location. Switches permit program RUN, HALT, and Single Step. Program breakpoints may be activated by changing instructions at the breakpoint locations. When a breakpoint is encountered, FAIR-BUG turns control over to you through the teleprinter. Commands consisting of single alphabetic allow you to examine or alter the contents of any memory location, group of locations or internal register of the CPU. Connection of peripheral circuits to the input/output ports enables the user to demonstrate his application.

The F8S is available now from your local Fairchild Franchised Distributor.

Unit Price: \$995.00

*The 3851 FAIR-BUG PSU is a fixed programmed Fairchild 3851 PSU which provides the programmer with all its I/O subroutines and allows the programmer to display or alter memory and register contents via a teletype terminal.



F8SEM – SYSTEM EXPANSION MODULE

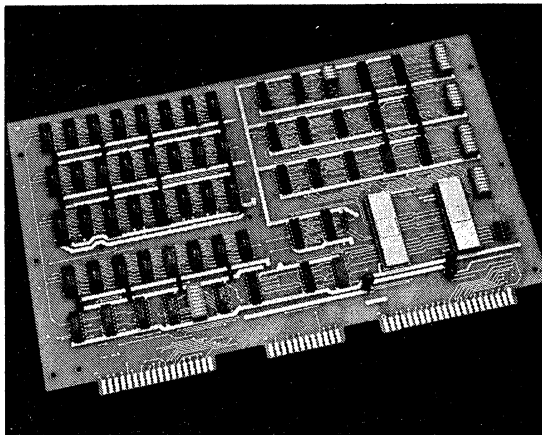
Designed to operate with the F8S Development Module, the F8SEM System Expansion Module adds 4K byte increments of memory to the F8 development system and four additional I/O ports. Switches contained on the module allow the user to select the active page address that the module will respond to, the addresses of the input/output ports and the interrupt addresses.

Features of the F8SEM System Expansion Module include:

- 4K Bytes of Static RAM
- Memory Page Selection

- 4 Input/Output Ports (8 Bits Each)
- Switch Selectable I/O Port Addresses
- 2 External Interrupts
- 2 Programmable Interval Timers
- Switch Selectable Interrupt Addresses

Unit Price: \$695.00

**F8SPDM – DEVELOPMENT MODULE SET**

The F8SPDM is a combination set of modules containing one F8S module card, two F8SEM module cards, a paper tape F8S Native Assembler, and all necessary users manuals and F8 documentation literature.

Unit Price: \$2,160.00

F8 FORMULATOR

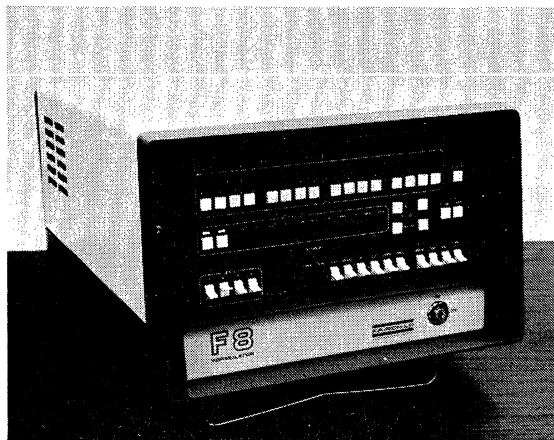
The F8 Formulator is a complete benchtop microprocessor development system designed to support every F8 application.

F8 Formulator features and capability include:

- F8 CPU Module
- Up to 64K Bytes of Addressable Memory
- Control and Monitor Console
- Virtually Unlimited Expansion of I/O Ports
- 2 External Interrupts Available for Every 4 I/O Ports
- Modular Construction
- Self-contained Power Supplies
- Resident Assembler
- Source Text Editor
- Complete Debug Capability

Standard memory modules and input/output modules permit expansion of the F8 Formulator to meet your need. Additional peripheral interfaces will also be available.

Contact your local Fairchild salesman, representative or franchised distributor for pricing information.



F8 INSTRUCTION SET SUMMARY

The F8 instruction set contains over 60 different instructions which may be subdivided into 10 categories: Accumulator, Scratchpad Register, Indirect Scratchpad Address Register, Memory Reference, Data Counter, Status Register, Program Counter, Branch, Interrupt Control and Input/Output instructions. Because 55% of the F8 instructions are only one byte long, programs are short and memory requirements significantly reduced. An alphabetic listing of the instructions is shown below. The following pages contain a complete description of the F8 instructions, including the cycle time. Each cycle is 2 μ s for a system with a 2 MHz clock frequency.

F8 ADDRESSING MODES

The F8 instruction set has eight modes of referencing either I/O, CPU registers or bulk memory.

Implied Addressing – The data for this one-byte instruction is implied by the actual instruction. For example, the POP instruction automatically implies that the content of the Program Counter will be set to the value contained in the Stack Register.

Direct Addressing – In these two-byte instructions, the address of the operand is contained in the second byte of the instruction. The Direct Addressing mode is used in the Input/Output class of instructions.

Short Immediate Addressing – Instructions whose addressing mode is Short Immediate have the instruction op code as the first four bits and the operand as the last four bits. They are all one-byte instructions.

Long Immediate Addressing – In these two-byte instructions, the first instruction byte is the op code and the second byte is the 8-bit operand.

Direct Register Addressing – This mode of addressing may be used to directly reference the Scratchpad Registers. By including the register number in the one-byte instruction, 12 of the 64 Scratchpad Registers may be referenced directly.

Indirect Register Addressing – All 64 Scratchpad Registers may be indirectly referenced, using the Indirect Scratchpad Register in the CPU. This 6-bit register, which acts as a pointer to the scratchpad memory, may either be incremented, decremented, or left unchanged while accessing the scratchpad register.

Indirect Memory Addressing – A 16-bit Indirect Address Register, the Data Counter, points to either data or constants in bulk memory. A group of one-byte instructions is provided to manipulate this area of memory. These instructions imply that the Data Counter is pointing to the desired memory byte. The Data Counter is self-incrementing, allowing for an entire data field to be scanned and manipulated without requiring special instructions to increment its content. The memory interface circuit contains two interchangeable data counters.

Relative Addressing – All F8 Branch Instructions use the relative addressing mode. Whenever a branch is taken, the Program Counter is updated by an 8-bit relative address contained in the second byte of the instruction. A branch may extend 128 locations forward or 127 locations back.

ALPHABETIC LIST OF INSTRUCTIONS

ADC	Add Data Counter with Accumulator	DCI	Load Data Counter Immediate	NI	Logical AND Accumulator Immediate
AI	Add Immediate with Accumulator	DI	Disable Interrupt	NM	Logical AND from Memory
AM	Add Binary Accumulator with Memory	DS	Decrement Scratchpad Register	NOP	No Operation
AMD	Add Decimal Accumulator with Memory	EI	Enable Interrupt	NS	Logical AND Scratchpad and Accumulator
AS	Add Binary Accumulator with Scratchpad Register	INC	Increment Accumulator	OI	Logical OR Immediate
ASD	Add Decimal Accumulator with Scratchpad Register	IN	Input	OM	Logical OR Memory with Accumulator
BC	Branch on Carry	INS	Input Short	OUT	Output
BF	Branch on False Condition	JMP	Jump	OUTS	Output Short
BM	Branch if Negative	LI	Load Accumulator Immediate	PI	Push Program Counter into Stack Register
BNC	Branch if no Carry	LIS	Load Accumulator Short	Set Program Counter to New Location	
BNO	Branch if no Overflow	LISL	Load ISAR – Lower 3 Bits	PK	Push Program Counter into Stack Register
BNZ	Branch if no Zero	LISU	Load ISAR – Upper 3 Bits	Set Program Counter from Scratchpad	
BP	Branch if Positive	LM	Load Memory	POP	Put Stack Register into Program Counter
BR	Unconditional Branch	LNK	Link Carry into Accumulator	SL	Shift Left
BR7	Branch if ISAR is not 7	LR	Load Register (5 Types)	SR	Shift Right
BT	Branch on True Condition		Scratchpad	ST	Store to Memory
BZ	Branch on Zero Condition		Program Counter	XDC	Exchange Data Counters
CI	Compare Immediate		ISAR	XI	Exclusive OR Immediate
CLR	Clear Accumulator		Status	XM	Exclusive OR Accumulator with Memory
CM	Compare with Memory		Data Counter	XS	Exclusive OR Accumulator with Scratchpad
COM	Complement Accumulator				

ACCUMULATOR GROUP INSTRUCTIONS

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS			
							OVF	ZERO	CRY	SIGN
ADD CARRY	LNK		ACC ← (ACC) + CRY	19	1	1	1/0	1/0	1/0	1/0
ADD IMMEDIATE	AI	ii	ACC ← (ACC) + H'ii'	24ii	2	2.5	1/0	1/0	1/0	1/0
AND IMMEDIATE	NI	ii	ACC ← (ACC) ∧ H'ii'	21ii	2	2.5	0	1/0	0	1/0
CLEAR	CLR		ACC ← H'00'	70	1	1	-	-	-	-
COMPARE IMMEDIATE	CI	ii	H'ii' + (ACC) + 1	25ii	2	2.5	1/0	1/0	1/0	1/0
COMPLEMENT	COM		ACC ← (ACC) ⊕ H'FF	18	1	1	0	1/0	0	1/0
EXCLUSIVE-OR IMMEDIATE	XI	ii	ACC ← (ACC) ⊕ H'ii'	23ii	2	2.5	0	1/0	0	1/0
INCREMENT	INC		ACC ← (ACC) + 1	1F	1	1	1/0	1/0	1/0	1/0
LOAD IMMEDIATE	LI	ii	ACC ← H'ii'	20ii	2	2.5	-	-	-	-
LOAD IMMEDIATE SHORT	LIS	i	ACC ← H'0i'	7i	1	1	-	-	-	-
OR IMMEDIATE	OI	ii	ACC ← (ACC) ∨ H'ii'	22ii	2	2.5	0	1/0	0	1/0
SHIFT LEFT ONE	SL	1	SHIFT LEFT 1	13	1	1	0	1/0	0	1/0
SHIFT LEFT FOUR	SL	4	SHIFT LEFT 4	15	1	1	0	1/0	0	1/0
SHIFT RIGHT ONE	SR	1	SHIFT RIGHT 1	12	1	1	0	1/0	0	1
SHIFT RIGHT FOUR	SR	4	SHIFT RIGHT 4	14	1	1	0	1/0	0	1

BRANCH INSTRUCTIONS In all conditional branches PC₀ ← (PC₀) + 2 if the test condition is not met. Execution is complete in 3.0 cycles.

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS											
							OVF	ZERO	CRY	SIGN								
BRANCH ON CARRY	BC	aa	PC ₀ ← [(PC ₀) + 1] + H'aa' if CRY = 1	82aa	2	3.5	-	-	-	-								
BRANCH ON POSITIVE	BP	aa	PC ₀ ← [(PC ₀) + 1] + H'aa' if SIGN = 1	81aa	2	3.5	-	-	-	-								
BRANCH ON ZERO	BZ	aa	PC ₀ ← [(PC ₀) + 1] + H'aa' if ZERO = 1	84aa	2	3.5	-	-	-	-								
BRANCH ON TRUE	BT	t, aa	PC ₀ ← [(PC ₀) + 1] + H'aa' if any test is true	8taa	2	3.5	-	-	-	-								
			t = TEST CONDITION															
			<table border="1"> <tr> <td>2²</td> <td>2¹</td> <td>2⁰</td> </tr> <tr> <td>ZERO</td> <td>CRY</td> <td>SIGN</td> </tr> </table>	2 ²	2 ¹	2 ⁰	ZERO	CRY	SIGN									
2 ²	2 ¹	2 ⁰																
ZERO	CRY	SIGN																
BRANCH IF NEGATIVE	BM	aa	PC ₀ ← [(PC ₀) + 1] + H'aa' if SIGN = 0	91aa	2	3.5	-	-	-	-								
BRANCH IF NO CARRY	BNC	aa	PC ₀ ← [(PC ₀) + 1] + H'aa' if CARRY = 0	92aa	2	3.5	-	-	-	-								
BRANCH IF NO OVERFLOW	BNO	aa	PC ₀ ← [(PC ₀) + 1] + H'aa' if OVF = 0	98aa	2	3.5	-	-	-	-								
BRANCH IF NOT ZERO	BNZ	aa	PC ₀ ← [(PC ₀) + 1] + H'aa' if ZERO = 0	94aa	2	3.5	-	-	-	-								
BRANCH IF FALSE TEST	BF	t, aa	PC ₀ ← [(PC ₀) + 1] + H'aa' if all tests are met	9taa	2	3.5	-	-	-	-								
			t = TEST CONDITION															
			<table border="1"> <tr> <td>2³</td> <td>2²</td> <td>2¹</td> <td>2⁰</td> </tr> <tr> <td>OVF</td> <td>ZERO</td> <td>CRY</td> <td>SIGN</td> </tr> </table>	2 ³	2 ²	2 ¹	2 ⁰	OVF	ZERO	CRY	SIGN							
2 ³	2 ²	2 ¹	2 ⁰															
OVF	ZERO	CRY	SIGN															
BRANCH IF ISAR (LOWER) ≠ 7	BR7	aa	PC ₀ ← [(PC ₀) + 1] + H'aa' if ISARL ≠ 7 PC ₀ ← (PC ₀) + 2 if ISARL = 7	8Faa	2	2.5 2.0	-	-	-	-								
BRANCH RELATIVE	BR	aa	PC ₀ ← [(PC ₀) + 1] + H'aa'	90aa	2	3.5	-	-	-	-								
JUMP*	JMP	aaaa	PC ₀ ← H'aaaa'	29aaaa	3	5.5	-	-	-	-								

*Privileged instruction

MEMORY REFERENCE INSTRUCTIONS

In all Memory Reference Instructions, the Data Counter is incremented DC ← DC + 1

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS			
							OVF	ZERO	CRY	SIGN
ADD BINARY	AM		ACC → (ACC) + ((DC))	88	1	2.5	1/0	1/0	1/0	1/0
ADD DECIMAL	AMD		ACC → (ACC) + ((DC))	89	1	2.5	1/0	1/0	1/0	1/0
AND	NM		ACC → (ACC) ∧ ((DC))	8A	1	2.5	0	1/0	0	1/0
COMPARE	CM		((DC)) + (ACC) + 1	8D	1	2.5	1/0	1/0	1/0	1/0
EXCLUSIVE OR	XM		ACC → (ACC) ⊕ ((DC))	8C	1	2.5	0	1/0	0	1/0
LOAD	LM		ACC → ((DC))	16	1	2.5	-	-	-	-
LOGICAL OR	OM		ACC → (ACC) ∨ ((DC))	8B	1	2.5	0	1/0	0	1/0
STORE	ST		(DC) → (ACC)	17	1	2.5	-	-	-	-

ADDRESS REGISTER GROUP INSTRUCTIONS

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS			
							OVF	ZERO	CRY	SIGN
ADD to DATA COUNTER	ADC		DC → (DC) + (ACC)	8E	1	2.5				
CALL to SUBROUTINE*	PK		PC ₀ U → (r12); PC ₀ L → (r13); PC ₁ → (PC ₀)	0C	1	4				
CALL to SUBROUTINE IMMEDIATE*	PI	aaaa	PC ₁ → (PC ₀); PC ₀ → H'aaaa	28aaaa	3	6.5				
EXCHANGE DC	XDC		(DC ₀) ↔ (DC ₁)	2C	1	2				
LOAD DATA COUNTER	LR	DC,Q	DCU → (r14); DCL → (r15)	0F	1	4				
LOAD DATA COUNTER	LR	DC,H	DCU → (r10); DCL → (r11)	10	1	4				
LOAD DC IMMEDIATE	DCI	aaaa	DC → H'aaaa	2Aaaaa	3	6				
LOAD PROGRAM COUNTER	LR	PO,Q	PC ₀ U → (r14); PC ₀ L → (r15)	0D	1	4				
LOAD STACK REGISTER	LR	P,K	PC ₁ U → (r12); PC ₁ L → (r13)	09	1	4				
RETURN FROM SUBROUTINE*	POP		PC ₀ → (PC ₁)	1C	1	2				
STORE DATA COUNTER	LR	Q,DC	r14 → (DCU); r15 → (DCL)	0E	1	4				
STORE DATA COUNTER	LR	H,DC	r10 → (DCU); r11 → (DCL)	11	1	4				
STORE STACK REGISTER	LR	K,P	r12 → (PC ₁ U); r13 → (PC ₁ L)	08	1	4				

SCRATCHPAD REGISTER INSTRUCTIONS

(Refer to Scratchpad Addressing Modes)

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS			
							OVF	ZERO	CRY	SIGN
ADD BINARY	AS	r	ACC → (ACC) + (r)	Cr	1	1	1/0	1/0	1/0	1/0
ADD DECIMAL	ASD	r	ACC → (ACC) + (r)	Dr	1	2	1/0	1/0	1/0	1/0
DECREMENT	DS	r	r ← (r) + H'FF'	3r	1	1.5	1/0	1/0	1/0	1/0
LOAD	LR	A,r	ACC → (r)	4r	1	1	-	-	-	-
LOAD	LR	A,KU	ACC → (r12)	00	1	1	-	-	-	-
LOAD	LR	A,KL	ACC → (r13)	01	1	1	-	-	-	-
LOAD	LR	A,QU	ACC → (r14)	02	1	1	-	-	-	-
LOAD	LR	A,QL	ACC → (r15)	03	1	1	-	-	-	-
LOAD	LR	r,A	r ← (ACC)	5r	1	1	-	-	-	-
LOAD	LR	KU,A	r12 → (ACC)	04	1	1	-	-	-	-
LOAD	LR	KL,A	r13 → (ACC)	05	1	1	-	-	-	-
LOAD	LR	QU,A	r14 → (ACC)	06	1	1	-	-	-	-
LOAD	LR	QL,A	r15 → (ACC)	07	1	1	-	-	-	-
AND	NS	r	ACC → (ACC) ∧ (r)	Fr	1	1	0	1/0	0	1/0
EXCLUSIVE OR	XS	r	ACC → (ACC) ⊕ (r)	Er	1	1	0	1/0	0	1/0

*Privileged instruction

MISCELLANEOUS INSTRUCTIONS

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS			
							OVF	ZERO	CRY	SIGN
DISABLE INTERRUPT	DI		RESET ICB	1A	1	2	-	-	-	-
ENABLE INTERRUPT*	EI		SET ICB	1B	1	2	-	-	-	-
INPUT	IN	aa	ACC ← (INPUT PORT aa)	26aa	2	4	0	1/0	0	1/0
INPUT SHORT	INS	a	ACC ← (INPUT PORT a)	Aa	1	4***	0	1/0	0	1/0
LOAD ISAR	LR	IS,A	ISAR ← (ACC)	0B	1	1	-	-	-	-
LOAD ISAR LOWER	LISL	a	ISARL ← a	01101a**	1	1	-	-	-	-
LOAD ISAR UPPER	LISU	a	ISARU ← a	01100a**	1	1	-	-	-	-
LOAD STATUS REGISTER*	LR	W,J	W ← (r9)	1D	1	2	1/0	1/0	1/0	1/0
NO-OPERATION	NOP		PC ₀ ← (PC ₀) + 1	2B	1	1	-	-	-	-
OUTPUT	OUT	aa	OUTPUT PORT aa ← (ACC)	27aa	2	4	-	-	-	-
OUTPUT SHORT	OUTS	a	OUTPUT PORT a ← (ACC)	Ba	1	4***	-	-	-	-
STORE ISAR	LR	A,IS	ACC ← (ISAR)	0A	1	1	-	-	-	-
STORE STATUS REG	LR	J,W	r9 ← (W)	1E	1	1	-	-	-	-

*Privileged instruction
 **3-bit octal digit
 ***2 machine cycles for CPU ports

NOTES

Each lower case character represents a Hexadecimal digit
 Each cycle equals 4 machine clock periods
 Lower case denotes variables specified by programmer

Function Definitions

- ← is replaced by
- () the contents of
- (-) Binary "1"s complement of
- + Arithmetic Add (Binary or Decimal)
- ⊕ Logical "OR" exclusive
- ∧ Logical "AND"
- ∨ Logical "OR" inclusive
- H Hexadecimal digit

Register Names

- a Address Variable
- A Accumulator
- DC Data Counter (Indirect Address Register)
- DC₀ Data Counter #0 (Indirect Address Register #0)
- DC₁ Data Counter #1 (Indirect Address Register #1)
- DCL Least significant 8 bits of Data Counter Addressed
- DCU Most significant 8 bits of Data Counter Addressed
- H Scratchpad Register #10 and #11
- i and ii immediate operand
- ICB Interrupt Control Bit
- IS Indirect Scratchpad Address Register
- ISAR Indirect Scratchpad Address Register
- ISARL Least Significant 3 bits of ISAR
- ISARU Most Significant 3 bits of ISAR
- J Scratchpad Register #9

- K Registers #12 and #13
- KL Register #13
- KU Register #12
- PC₀ Program Counter
- PC₀L Least Significant 8 bits of Program Counter
- PC₀U Most Significant 8 bits of Program Counter
- PC₁ Stack Register
- PC₁L Least Significant 8 bits of Program Counter
- PC₁U Most Significant 8 bits of Active Stack Register
- Q Registers #14 and #15
- QL Register #15
- QU Register #14
- r Scratchpad Register (any address thru 11)
- W Status Register

Scratchpad Addressing Modes (Machine Code Format)

- r = C (Hexadecimal), Register Addressed by ISAR (Unmodified)
- r = D (Hexadecimal), Register Addressed by ISAR; ISARL Incremented
- r = E (Hexadecimal), Register Addressed by ISAR; ISARL Decrementd
- r = F (No operation performed)
- r = 0 (Hexadecimal), Register 0 thru 11 addressed directly from
thru B the Instruction

Status Register

- No change in condition
- 1/0 is set to "1" or "0" depending on conditions
- CRY Carry Flag
- OVF Overflow Flag
- SIGN Sign of Result Flag
- ZERO Zero Flag

POWER REQUIREMENTS: $V_{DD} = +5.0\text{ V} \pm 5\%$; $V_{GG} = +12.0\text{ V} \pm 5\%$; $V_{SS} = 0\text{ V}$; $T_A = 0^\circ\text{C to } 70^\circ\text{C}$; $f = 2\text{ MHz}$

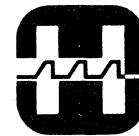
PART TYPE	SYMBOL	PARAMETER	TYP	MAX	UNITS	TEST CONDITIONS (Outputs Unloaded)
3850	I_{DD}	V_{DD} Current	30	80	mA	2 MHz
	I_{GG}	V_{GG} Current	15	25	mA	
3851	I_{DD}	V_{DD} Current	30	70	mA	2 MHz
	I_{GG}	V_{GG} Current	10	18	mA	
3852	I_{DD}	V_{DD} Current	35	70	mA	2 MHz
3853	I_{GG}	V_{GG} Current	13	30	mA	
3854	I_{DD}	V_{DD} Current	20	40	mA	2 MHz
	I_{GG}	V_{GG} Current	15	28	mA	

SIGNAL ELECTRICAL SPECIFICATIONS

$V_{DD} = +5.0\text{ V} \pm 5\%$; $V_{GG} = +12.0\text{ V} \pm 5\%$; $V_{SS} = 0\text{ V}$; $T_A = 0^\circ\text{C to } 70^\circ\text{C}$; $f = 2\text{ MHz}$

SIGNAL NAME (NUMBER, TYPE)	SOURCE OR RECEIVING DEVICE	V_{OH} MIN	V_{IH} MIN	V_{OL} MAX	V_{IL} MAX	LOAD
DATA BUS (8 INPUTS/OUTPUTS)	3850 3851 3852/3 3854	3.9	3.5	0.4	0.8	100 pF $I_{SOURCE} = 100\ \mu\text{A}$ $I_{SINK} = 900\ \mu\text{A}$
CONTROL BUS (5 OUTPUTS)	3850	3.9		0.4		100 pF, $I_{SINK} = 900\ \mu\text{A}$ $I_{SOURCE} = 100\ \mu\text{A}$
CONTROL BUS (5 INPUTS) ¹	3851 3852/3		3.5		0.8	
I/O PORTS (16 INPUTS/OUTPUTS)	3850 3851	2.9 (1 TTL) 3.9 (unloaded)	3.5 ²	0.4	0.8	100 pF plus 1 H-TTL Load
CLOCK REFERENCE (INPUT)	3850		4.0		0.8	
SYSTEM CLOCKS (PHI AND WRITE OUTPUTS)	3850	4.4		0.4		100 pF, $I_{SINK} = 900\ \mu\text{A}$ $I_{SOURCE} = 100\ \mu\text{A}$
SYSTEM CLOCKS (PHI AND WRITE INPUTS)	3851 3852/3 3854		4.0		0.8	
RESET (INPUT)	3850		3.5 ²		0.8	$I_{IL} = 0.3\text{ mA Max at } V_{IN} = V_{SS}$
INTERRUPT CONTROL BIT (OUTPUT)	3850	3.9		0.4		50 pF plus 100 μA I_{SOURCE} or I_{SINK}
INTERRUPT REQUEST (INPUT)	3850		3.5 ²		0.8	$I_{IL} = 1\text{ mA Max at } V_{IN} = 0.4$
INTERRUPT REQUEST (OUTPUT)	3851 3853	OPEN DRAIN		0.4		100 pF plus $I_{SINK} = 1\text{ mA}$
EXTERNAL INTERRUPT (INPUT)	3851 3853		3.5		1.2	
PRIORITY IN (INPUT)	3851 3853		3.5		0.8	
PRIORITY OUT (OUTPUT)	3851	3.9		0.4		50 pF plus 100 μA I_{SOURCE} or I_{SINK}
DBDR (OUTPUT)	3851	OPEN DRAIN ³		0.4		100 pF plus $I_{SINK} = 2.5\text{ mA}$
ADDRESS LINES and RAM WRITE (16 OUTPUTS)	3852/3 3854	4.0		0.4		500 pF plus 2 TTL Loads
REGDR (INPUT/OUTPUT)	3852/3	3.9	3.5	0.4	0.8	100 pF plus 1 H-TTL Load
CPU READ (OUTPUT)	3852/3	3.9		0.4		50 pF plus 1 H-TTL Load
MEM IDLE, CYCLE REQ and CPU SLOT (OUTPUTS)	3852	3.9		0.4		50 pF plus 1 H-TTL Load
MEM IDLE (INPUT)	3854		3.5		0.8	
ENABLE, DIRECTION, TRANSFER, DMA WRITE SLOT, STROBE (OUTPUTS)	3854	3.9		0.4		50 pF plus 1 H-TTL Load
XFER REQ, P1, P2 (INPUTS)	3854		3.5		0.8	
LOAD REG, READ REG (INPUTS)	3854		3.5		0.8	

¹3854 receives two control signals from external decoding device. ²Internal pull-up resistor to V_{DD} . ³External pull-up resistor required.



INTRODUCTION

HM6100 MICROPROCESSOR

The HM6100 and HM6100A are single address, fixed word length, parallel transfer microprocessors using 12-bit, two's complement arithmetic. The processors recognize the instruction set of Digital Equipment Corporation's PDP8/E minicomputer. The internal circuitry is completely static and is designed to operate at any speed between DC and the maximum operating frequency. Two pins are available to allow for an external crystal thereby eliminating the need for clock generators and level translators. The crystal can be removed and the processor clocked by an external clock generator. A 12-bit memory-accumulator ADD instruction is performed in 5 μ sec by the HM6100 using a +5 volt supply and in 2.5 μ sec by the HM6100A using a +10 volt supply. The device design is optimized to minimize the number of external components required for interfacing with standard memory and peripheral devices.

FEATURES

DESIGN

- Silicon Gate Complementary MOS
- Fully Static-0 to 8 MHz
- Single Power Supply
 - HM6100 $V_{cc}=5$ volts
 - HM6100A $V_{cc}=10$ volts
- Crystal Controlled On Chip Timing
- Low Power Dissipation < 10 mW @ 4 MHz @ 5 volts
- Single Power Supply $4V \leq V_{cc} \leq 11V$
- TTL Compatible at 5 Volts
- Excellent Noise Immunity
- -55°C to +125°C Operation

INTERFACE

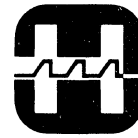
- Memory—Any Speed
- Control Panel
- Switch Register
- Asynchronous CPU—Memory and CPU—Device Communication
- 64 I/O Devices with PDP-8/E Compatible Interface
- Device Controlled Input-Output
- All Control Signals Produced By The CPU
- Power-on Initialize

ARCHITECTURAL

- Executes PDP-8/E, MP-12 and D-112 Instruction Set
- Direct, Indirect, and Autoindexed Memory Addressing
- 12-Bit Memory Accumulator ADD Instruction
 - HM6100 5 μ sec @ +5 volts
 - HM6100A 2.5 μ sec @ +10 volts
- Input-Output Instruction
 - HM6100 8.5 μ sec @ +5 volts
 - HM6100A 4.25 μ sec @ +10 volts
- Single-Clock, Single-Instruction Capability
- Direct Memory Access (DMA)
- Interrupt
- Dedicated Control Panel Features

APPLICATIONS

- Intelligent Computer Terminals
- POS Terminals
- Portable Terminals
- Aerospace/Satellite System
- Automotive Systems
- Remote Data Acquisition Systems
- Process Control
- Instrumentation
- Medical Electronics
- Displays
- Traffic Control
- Navigation



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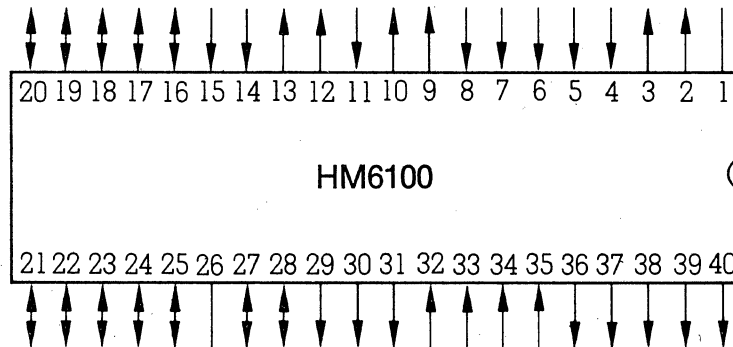
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PIN ASSIGNMENTS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1	V _{cc}		Supply voltage.
2	RUN	H	The signal indicates the runstate of the CPU and may be used to power down the external circuitry
3	DMAGNT	H	Direct Memory Access Grant—DX lines are three-state.
4	DMAREQ	L	Direct Memory Access Request—DMA is granted at the end of the current instruction. Upon DMA grant, the CPU suspends program execution until the DMAREQ line is released.
5	CPREQ	L	Control Panel Request—a dedicated interrupt which bypasses the normal device interrupt request structure.
6	RUN/HLT	L	Pulsing the Run/Halt line causes the CPU to alternately run and halt by changing the state of the internal RUN/HLT flip flop.
7	RESET	L	Clears the AC and loads 7777 _h into the PC. CPU is halted.
8	INTREQ	L	Peripheral device interrupt request.
9	XT _A	H	External coded minor cycle timing—signifies input transfers to the HM6100.

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
10	LXMAR	H	The Load External Address Register is used to store memory and peripheral address externally.
11	WAIT	L	Indicates that peripherals or external memory is not ready to transfer data. The CPU state gets extended as long as WAIT is active. The CPU is in the lowest power state with clocks running.
12	XT _B	H	External coded minor cycle timing—signifies output transfers from the HM6100.
13	XT _C	H	External coded minor cycle timing—used in conjunction with the Select Lines to specify read or write operations.
14	OSC OUT		Crystal input to generate the internal timing (also external clock input).
15	OSC IN		See Pin 14—OSC OUT (also external clock ground)
16	DX ₀		DataX—multiplexed data in, data out and address lines.
17	DX ₁		See Pin 16—DX ₀ .
18	DX ₂		See Pin 16—DX ₀ .
19	DX ₃		See Pin 16—DX ₀ .
20	DX ₄		See Pin 16—DX ₀ .



PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
21	DX ₅		See Pin 16—DX ₀ .
22	DX ₆		See Pin 16—DX ₀ .
23	DX ₇		See Pin 16—DX ₀ .
24	DX ₈		See Pin 16—DX ₀ .
25	DX ₉		See Pin 16—DX ₀ .
26	GND		Ground
27	DX ₁₀		See Pin 16—DX ₀ .
28	DX ₁₁		See Pin 16—DX ₀ .
29	LINK	H	Link flip flop.
30	DEVSEL	L	Device Select for I/O transfers.
31	SWSEL	L	Switch Register Select for the OR THE SWITCH REGISTER INSTRUCTION - (OSR). OSR is a Group 2 Operate Instruction which reads a 12 bit external switch register and OR's it with the contents of the AC.
32	C ₀	L	Control line inputs from the peripheral device during an I/O transfer (Table 5).

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
33	C ₁	L	See Pin 32—C ₀ .
34	C ₂	L	See Pin 32—C ₀ .
35	SKP	L	Skips the next sequential instruction if active during an I/O instruction.
36	IFETCH	H	Instruction Fetch Cycle
37	MEMSEL	L	Memory Select for memory transfers.
38	CPSEL	L	The Control Panel Memory Select becomes active, instead of the MEMSEL, for control panel routines. Signal may be used to distinguish between control panel and main memories.
39	INTGNT	H	Peripheral device Interrupt Grant
40	DATAF	H	Data Field pin indicates the execute phase of indirectly addressed AND, TAD, ISZ and DCA instructions so that the data transfers are controlled by the Data Field, DF, and not the Instruction Field, IF, if Extended Memory Control hardware is used to extend the addressing space from 4K to 32K words.

SPECIFICATIONS

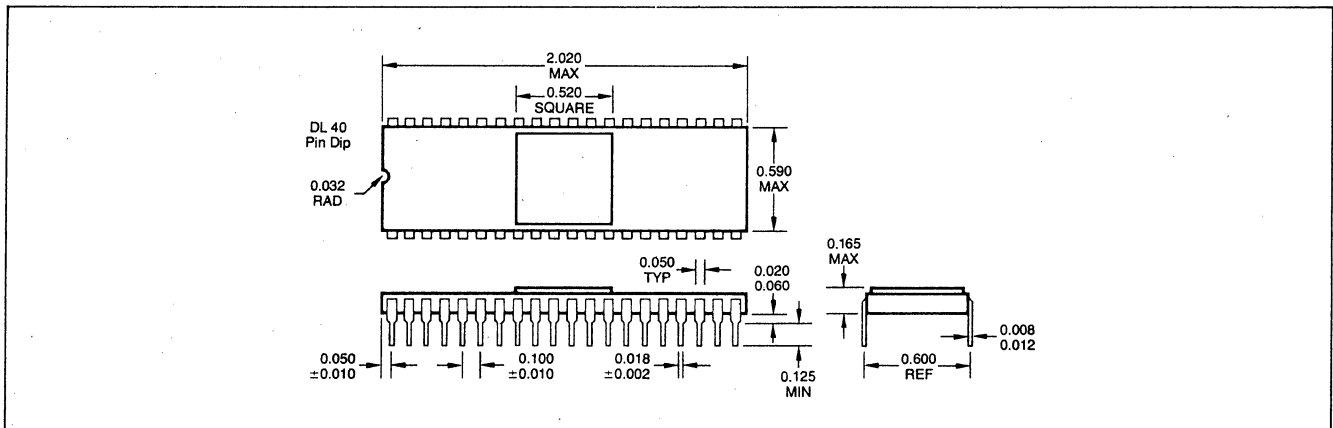
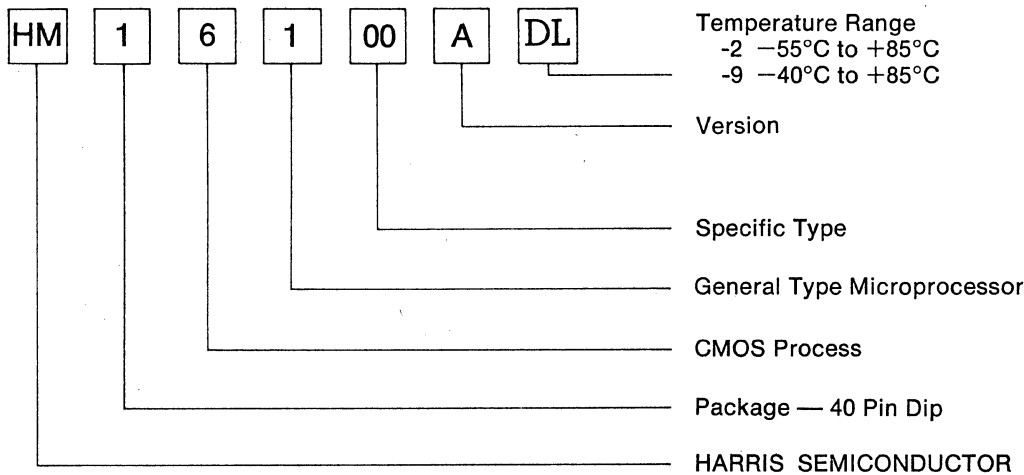
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	HM6100 +4.0V to +7.0V HM6100A +4.0V to 11.0V	Operating Temperature Range	
Input or Output Voltage Applied	GND -0.3V to $V_{CC} + 0.3V$	Industrial	-40°C to +85°C
Storage Temperature Range	-65°C to +125°C	Military	-55°C to +125°C

DC CHARACTERISTICS $V_{CC} = 5.0V \pm 10\%$ (HM6100), $10.0V \pm 10\%$ (HM6100A), $T_A =$ Industrial or Military

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		70% V_{CC}			V
Logical "0" Input Voltage	V_{IL}				20% V_{CC}	V
Input Leakage	I_{IL}	$0V \leq V_{IN} \leq V_{CC}$	-1.0		1.0	μA
Logical "1" Output Voltage	V_{OH2}	$I_{OUT} = 0$	$V_{CC} - 0.01$			V
Logical "1" Output Voltage	V_{OH1}	$I_{OH} = -0.2mA$	2.4			V
Logical "0" Output Voltage	V_{OL2}	$I_{OUT} = 0$			GND + 0.01	V
Logical "0" Output Voltage	V_{OL1}	$I_{OL} = 1.6mA$			0.45	V
Output Leakage	I_O	$0V \leq V_O \leq V_{CC}$	-1.0		1.0	μA
Supply Current	I_{CC}	$V_{IN} = GND$ or V_{CC} ; Output Open; $T_A = 25^\circ C$; $F_{clock} = 0$		400		μA
Input Capacitance	C_{IN}			5.0		pF
Output Capacitance	C_O			8.0		pF

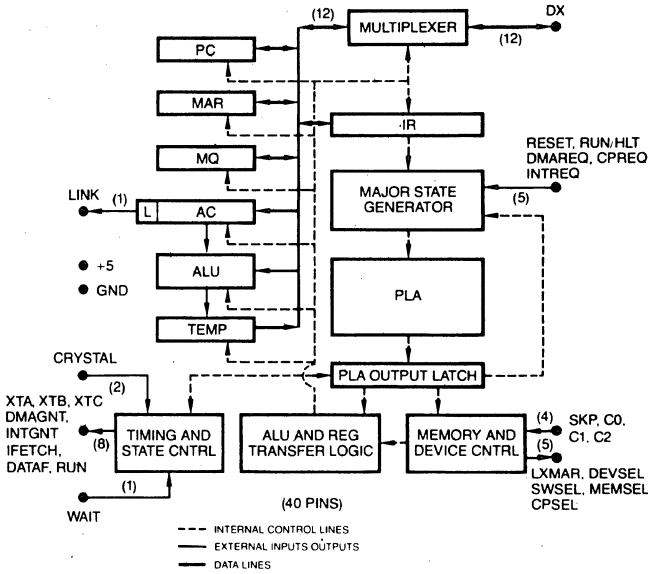
ORDERING INFORMATION Circuit marking and product code explanation



ARCHITECTURE

The HM6100/A has 6 twelve bit registers, a programmable logic array, an arithmetic and logic unit and associated gating and timing circuitry. A block diagram of the HM6100 is shown in Figure 1.

FIGURE 1



ACCUMULATOR (AC)

The AC is a 12-bit register with which arithmetic and logical operations are performed. Data words may be fetched from memory to the AC or stored from the AC into memory. Arithmetic and logical operations involve two operands, one held in the AC and the other fetched from the memory. The result of the operation is left in the AC. The AC may be cleared, complemented, tested, incremented or rotated under program control. The AC also serves as an input-output register. All programmed data transfers pass through the AC.

LINK (L)

The Link is a 1-bit flip-flop that serves as a high-order extension of the AC. It is used as a carry flip-flop for 2's complement arithmetic. A carry out of the ALU complements the Link. Link can be cleared, set, complemented and tested under program control and rotated as part of the AC.

MQ REGISTER (MQ)

The MQ is a 12-bit temporary register which is program accessible. The contents of AC may be transferred to the MQ for temporary storage. MQ can be OR'ed with the AC and the result stored in the AC. The contents of the AC and the MQ may also be exchanged.

MEMORY ADDRESS REGISTER (MAR)

While accessing memory, the 12-bit MAR register contains the address of the memory location that is currently selected for reading or writing. The MAR is also used as an internal register for microprogram control during data transfers to and from memory and peripherals.

PROGRAM COUNTER (PC)

The 12-bit PC contains the address of the memory location from which the next instruction is fetched. During an instruction fetch, the

PC is transferred to MAR and the PC is then incremented by 1. When there is a branch to another address in memory, the branch address is set into the PC. Branching normally takes place under program control. However, during an input-output operation, a device may specify a branch address. A skip (SKP) instruction increments the PC by 1, thus causing the next instruction to be skipped. The SKP instruction may be unconditional or conditional on the state of the AC and/or the Link. During an input-output operation, a device can also cause the next sequential instruction to be skipped.

ARITHMETIC AND LOGICAL UNIT (ALU)

The ALU performs both arithmetic and logical operations—2's complement binary addition, AND, OR and complement. The ALU can perform a single position shift either to the left or to the right. A double rotate is implemented in two single bit shifts. The ALU can also shift by 3 positions to implement a byte swap in two steps. The AC is always one of the inputs to the ALU. However, under internal microprogram control, AC may be gated off and all one's or all zero's gated in. The second input may be any one of the other registers under internal microprogram control.

TEMPORARY REGISTER (TEMP)

The 12-bit TEMP register latches the result of an ALU operation before it is sent to the destination register to avoid race conditions. The TEMP is also used as an internal register for microprogram control.

INSTRUCTION REGISTER (IR)

During an instruction fetch, the 12-bit IR contains the instruction that is to be executed by the CPU. The IR specifies the initial step of the microprogram sequence for each instruction and is also used as an internal register to store temporary data for microprogram control.

MULTIPLEXER (DX)

The 12-bit Input/Output Multiplexer handles data, address and instruction transfers, into and out of, the CPU, from or into, the main memory and peripheral devices on a time-multiplexed basis.

MAJOR STATE GENERATOR AND THE PROGRAMMED LOGIC ARRAY (PLA)

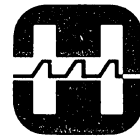
During an instruction fetch the instruction to be executed is loaded into the IR. The PLA is then used for the correct sequencing of the CPU for the appropriate instruction. After an instruction is completely sequenced, the major state generator scans the internal priority network. The state of the priority network decides whether the machine is going to fetch the next instruction in sequence or service one of the external request lines.

PLA OUTPUT LATCH

The PLA Output Latch latches the PLA output thereby permitting the PLA to be pipelined; it fetches the next control sequence while the CPU is executing the current sequence.

MEMORY AND DEVICE CONTROL, ALU AND REG TRANSFER LOGIC

The Memory and Device Control Unit provides external control signals to communicate with peripheral devices (DEVSEL), switch register (SWSEL), memory (MEMSEL) and/or control panel memory (CPSEL). During I/O instructions this unit also modifies the PLA outputs depending on the states of the four device control lines (SKP, C₀, C₁, C₂). The ALU and Register Transfer Logic provides the control signals for the internal register transfers and ALU operation.



TIMING AND STATE CONTROL

The HM6100/A generates all the timing and state signals internally. A crystal is used to control the CPU operating frequency. The CPU divides the crystal frequency by two. With a 4MHz crystal, the internal states will be of 500ns duration. The major timing states are described in Figure 2.

T₁ For memory reference instructions, a 12-bit address is sent on the DataX, DX, lines. The Load External Address Register, LXMAR, is used to clock an external register to store the address information externally, if required. When executing an Input-Output I/O instruction, the instruction being executed is sent on the DX lines to be stored externally. The external address register then contains the device address and control information.

Various CPU request lines are priority sampled if the next cycle is an Instruction Fetch cycle. Current state of the CPU is available externally.

T₂

Memory/Peripheral data is read for an input transfer (READ). WAIT controls the transfer duration. If WAIT is active during input transfers, the CPU waits in the T₂ state. The wait duration is an integral multiple of the crystal frequency—250ns for 4MHz.

For memory reference instructions, the Memory Select, MEMSEL, line is active. For I/O instructions the Device Select, DEVSEL, line is active. Control lines, therefore, distinguish the contents of the external register as memory or device address.

External device sense lines, C₀, C₁, C₂, and SKP, are sampled if the instruction being executed is an I/O instruction.

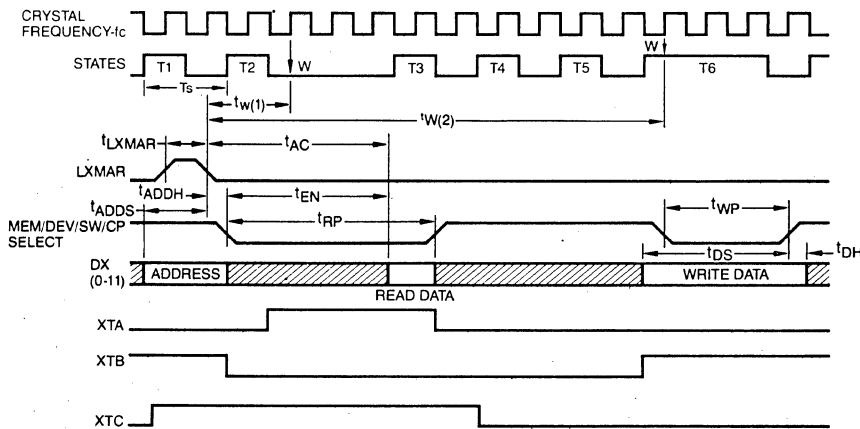
Control Panel Memory Select, CPSEL, and Switch Register Select, SWSEL, become active low for data transfers between the HM6100 and Control Panel Memory and the Switch Register, respectively.

T₃, T₄, T₅
T₆

ALU operation and internal register transfers.

This state is entered for an output transfer (WRITE). The address is defined during T₁. WAIT controls the time for which the Write data must be maintained.

FIGURE 2



HM6100 TIMING AND STATE SIGNALS

AC CHARACTERISTICS (T_A = 25° C)

PARAMETER	SYMBOL	HM6100	HM6100/A	UNITS
		V _{CC} = 5.0, f _c = 4MHz TYP	V _{CC} = 10.0, f = 8 MHz TYP	
Major State Time	T _S	500	250	ns
LXMAR Pulse Width	t _{LXMAR}	250	125	ns
Address Setup Time	t _{ADDS}	50	50	ns
Address Hold Time	t _{ADDH}	250	125	ns
Read WAIT Valid Time	t _{W(1)}	250	125	ns
Write WAIT Valid Time	t _{W(2)}	1800	900	ns
Access Time From CS	t _{AC}	450	225	ns
Output Enable Time	t _{EN}	300	150	ns
Read Pulse Width	t _{RP}	700	350	ns
Write Pulse Width	t _{WP}	250	125	ns
Data Setup Time	t _{DS}	250	125	ns
Data Hold Time	t _{DH}	100	50	ns

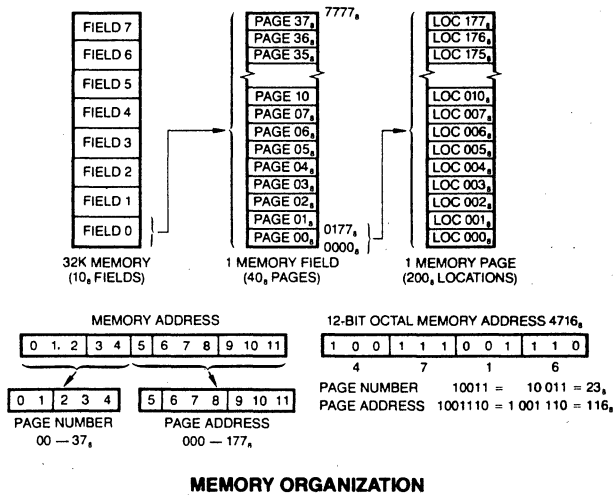
MEMORY AND PROCESSOR INSTRUCTIONS

The HM6100 instructions are 12-bit words stored in memory. The HM6100 makes no distinction between instructions and data; it can manipulate instructions as stored variables or execute data as instructions when it is programmed to do so. There are three general classes of HM6100 instructions. They are referred to as Memory Reference Instruction (MRI), Operate Instruction (OPR) and Input/Output Transfer Instruction (IOT).

Before proceeding further, we will discuss the Specific Memory Organization with which the HM6100 interfaces.

MEMORY ORGANIZATION

The HM6100 has a basic addressing capacity of 4096 12-Bit words. The addressing capacity may be extended by Extended Memory Control hardware. The memory system is organized in 4096 word blocks, called MEMORY FIELDS. The first 4096 words of memory are in Field 0. If a full 32K of memory is installed, the uppermost Memory Field will be numbered 7. In any given Memory Field every location has a unique 4 digit octal (12 bit binary) address, 0000₈ to 7777₈ (0000₁₀ to 4095₁₀). Each Memory Field is subdivided into 32 PAGES of 128 words each. Memory Pages are numbered sequentially from Page 00₈, containing addresses 0000-0177₈, to Page 37₈, containing addresses 7600₈-7777₈. The first 5 bits of a 12-bit MEMORY ADDRESS denote the PAGE NUMBER and the low order 7 bits specify the PAGE ADDRESS of the memory location within the given Page.



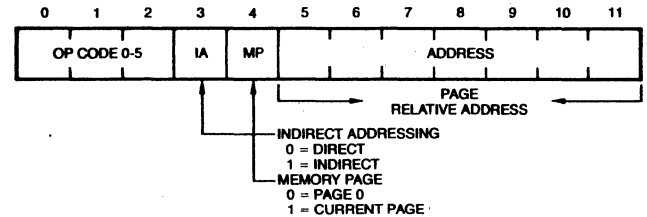
MEMORY ORGANIZATION

During an instruction fetch cycle, the HM6100 fetches the instruction pointed to by the PC. The contents of the PC are transferred to the MAR. The PC is incremented by 1. The PC now contains the address of the 'next' sequential instruction. The MAR contains the address of the 'current' instruction which must be fetched from memory. Bits 0-4 of the MAR identify the CURRENT PAGE, that is, the Page from which instructions are currently being fetched and bits 5-11 of the MAR identify the location within the Current Page. (PAGE ZERO (0), by definition, denotes the first 128 words of memory, 0000₈-0177₈.)

MEMORY REFERENCE INSTRUCTIONS (MRI)

The Memory Reference Instructions operate on the contents of a memory location or use the contents of a memory location to operate on the AC or the PC. The first 3 bits of a Memory Reference Instruction specify the operation code, or OPCODE, and the low order 9 bits, the OPERAND address, as shown in Figure 3.

FIGURE 3



MEMORY REFERENCE INSTRUCTION FORMAT

Bits 5 through 11, the PAGE ADDRESS, identify the location of the OPERAND on a given page, but they do not identify the page itself. The page is specified by bit 4, called the CURRENT PAGE OR PAGE 0 BIT. If bit 4 is a 0, the page address is interpreted as a location on Page 0. If bit 4 is a 1, the page address specified is interpreted to be on the Current Page.

For example, if bits 5 through 11 represent 123₈ and bit 4 is a 0, the location referenced is the absolute address 0123₈. However, if bit 4 is a 1 and the current instruction is in a memory location whose absolute address is 4610₈, the page address 123₈ designates the absolute address 4723₈, as shown below.

$$4610_8 = 100\ 110\ 001\ 000 = \text{PAGE } 10\ 011 = \text{PAGE } 23_8$$

Location 4610₈ is in PAGE 23₈. Location 123₈ in PAGE 23₈, CURRENT PAGE, will be:

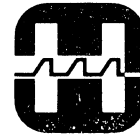
$$10\ 011, 1\ 010\ 011 = 100\ 111\ 010\ 011 = 4723_8$$

PAGE NUMBER 23₈ PAGE ADDRESS 123₈

By this method, 256 locations may be directly addressed, 128 on PAGE 0 and 128 on the CURRENT PAGE. Other locations are addressed by utilizing bit 3. When bit 3 is a 0, the operand address is a DIRECT ADDRESS. An INDIRECT ADDRESS (pointer address) identifies the location that contains the desired address (effective address). To address a location that is not directly addressable, not in PAGE 0 or in the CURRENT PAGE, the absolute address of the desired location is stored in one of the 256 directly addressable locations (pointer address). Upon execution, the MRI will operate on the contents of the location identified by the address contained in the pointer location.

It should be noted that locations 0010₈-0017₈ in PAGE 0 are AUTOINDEXED. If these locations are addressed indirectly, the contents are incremented by 1 and restored before they are used as the operand address. These locations may, therefore, be used for indexing applications.

Table 1 lists the mnemonics for the five memory reference instruction, their OPCODE, the operations they perform, the number of states and the execution time at +5.0V and +10.0V, assuming a crystal frequency of 4MHz and 8MHz or a state time period of 500 ns and 250ns, respectively.



It should be noted that the data is represented in Two's Complement Integer notation. In this system, the negative of a number is formed by complementing each bit in the data word and adding "1" to the complemented number. The sign is indicated by the most significant bit. In the 12-bit word used by the HM6100, when bit 0 is a "0", it denotes a positive number and when bit 0 is a "1", it denotes a negative number. The maximum number ranges for this system are 3777_8 (+2047) and 4000_8 (-2048).

Notations applied in Table 1, are defined as follows:

- () Denotes the contents of the register or location within the parenthesis. (EA) is read as "... the contents of the Effective Address".
- (()) Denotes the contents of the location pointed to by the contents of the location within the double parenthesis. ((PA)) is read as "... the contents of the location pointed to by the contents of the Pointer Address."
- ← Denotes "... is replaced by ..."
- ∧ Denotes, logical AND operation
- ∨ Denotes, logical OR operation

TABLE 1

MNE-MONIC	OP CODE	OPERATION	NUMBER OF STATES	EXECUTION TIME (μs)	
				HM6100 +5.0V	HM6100 +10.0V
AND	0 ₈	LOGICAL AND DIRECT (I = 0) Operation: (AC) ← -(AC) ∧ (EA) Description: Contents of the EA are logically AND'ed with the contents of the AC and the result is stored in AC.	10	5.0	2.50
		INDIRECT (I = 1, PA ≠ 0010-0017 ₈) Operation: (AC) ← -(AC) ∧ ((PA))	15	7.5	3.75
		AUTOINDEX (I = 1, PA = 0010-0017 ₈) Operation: (PA) ← -(PA) + 1; (AC) ← -(AC) ∧ ((PA))	16	8.0	4.00
TAD	1 ₈	BINARY ADD DIRECT (I = 0) Operation: (AC) ← -(AC) + (EA) Description: Contents of the EA are ADD'ed with the contents of the AC and the result is stored in the AC; carry out complements the LINK. If AC is initially cleared, this instruction acts as LOAD from Memory	10	5.0	2.50
		INDIRECT (I = 1, PA ≠ 0010-0017 ₈) Operation: (AC) ← -(AC) + ((PA))	15	7.5	3.75
		AUTOINDEX (I = 1, PA = 0010-0017 ₈) Operation: (PA) ← -(PA) + 1; (AC) ← -(AC) + ((PA))	16	8.0	4.00
ISZ	2 ₈	INCREMENT AND SKIP IF ZERO DIRECT (I = 0) Operation: (EA) ← -(EA) + 1; if (EA) = 0000 ₈ , PC ← -PC + 1 Description: Contents of the EA are incremented by 1 and restored. If the result is zero, the next sequential instruction is skipped.	16	8.0	4.00
		INDIRECT (I = 1, PA ≠ 0010-0017 ₈) Operation: ((PA)) ← -(PA) + 1; if ((PA)) = 0000 ₈ , PC ← -PC + 1	21	10.5	5.25
		AUTOINDEX (I = 1, PA = 0010-0017 ₈) Operation: (PA) ← -(PA) + 1; ((PA)) ← -(PA) + 1; if ((PA)) = 0000 ₈ , PC ← -PC + 1	22	11.0	5.50
DCA	3 ₈	DEPOSIT AND CLEAR THE ACCUMULATOR DIRECT (I = 0) Operation: (EA) ← -(AC); (AC) ← -0000 ₈ Description: The contents of the AC are stored in EA and the AC is cleared.	11	5.5	2.75
		INDIRECT (I = 1, PA ≠ 0010-0017 ₈) Operation: ((PA)) ← -(AC); (AC) ← -0000 ₈	16	8.0	4.00
		AUTOINDEX (I = 1, PA = 0010-0017 ₈) Operation: (PA) ← -(PA) + 1; ((PA)) ← -(AC); (AC) ← -0000 ₈	17	8.5	4.25
JMS	4 ₈	JUMP TO SUBROUTINE DIRECT (I = 0) Operation: (EA) ← -(PC); (PC) ← -EA + 1 Description: The contents of the PC are stored in the EA. The PC is incremented by 1 immediately after every instruction fetch. The contents of the EA now point to the next sequential instruction following the JMS (return address). The next instruction is taken from EA + 1.	11	5.5	2.75
		INDIRECT (I = 1, PA ≠ 0010-0017 ₈) Operation: ((PA)) ← -PC; (PC) ← -(PA) + 1	16	8.0	4.00
		AUTOINDEX (I = 1, PA = 0010-0017 ₈) Operation: (PA) ← -(PA) + 1; ((PA)) ← -PC; (PC) ← -(PA) + 1	17	8.5	4.25
JMP	5 ₈	JUMP DIRECT (I = 0) Operation: (PC) ← -EA Description: The next instruction is taken from the EA.	10	5.0	2.50
		INDIRECT (I = 1, PA ≠ 0010-0017 ₈) Operation: (PC) ← -(PA)	15	7.5	3.75
		AUTOINDEX (I = 1, PA = 0010-0017 ₈) Operation: (PA) ← -(PA) + 1; (PC) ← -(PA)	16	8.0	4.00

MEMORY REFERENCE INSTRUCTIONS

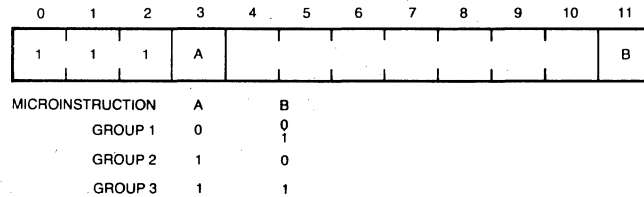
OPERATE INSTRUCTIONS

The Operate Instructions, which have an OPCODE of 7_8 (111), consists of 3 groups of microinstructions. Group 1 microinstructions, which are identified by the presence of a 0 in bit 3, are used to perform logical operations on the contents of the accumulator and link. Group 2 micro instructions, which are identified by the presence of a 1 in bit 3 and a 0 in bit 11, are used primarily to test the contents of the accumulator and then conditionally skip the next sequential instruction. Group 3 microinstructions have a 1 in bit 3 and a 1 in bit 11 and are used to perform logical operations on the contents of the AC and MQ.

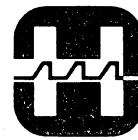
The basic OPR instruction format is shown in Figure 4.

Operate microinstructions from any group may be microprogrammed with other operate microinstructions of the same group. The actual code for a microprogrammed combination of two, or more, microinstructions is the bitwise logical OR of the octal codes for the individual microinstructions. When more than one operation is microprogrammed into a single instruction, the operations are performed in a prescribed sequence, with logical sequence number 1 microinstructions performed first, logical sequence number 2 microinstructions performed second, logical sequence number 3 microinstructions performed third and so on. Two operations with the same logical sequence number, within a given group of microinstructions, are performed simultaneously.

FIGURE 4



BASIC OPR INSTRUCTION FORMAT

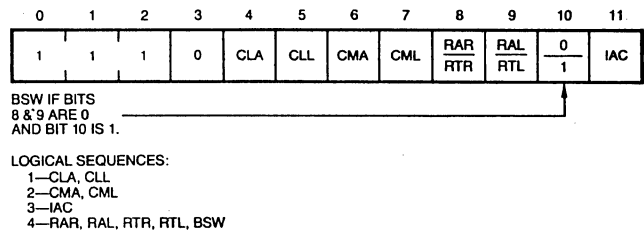


GROUP 1 MICROINSTRUCTIONS

Figure 5 shows the instruction format of a group 1 microinstruction. Any one of bits 4 to 11 may be set, loaded with a binary 1, to indicate a specific group 1 microinstruction. If more than one of these bits is set, the instruction is a microprogrammed combination of group 1 microinstructions, which will be executed according to the logical sequence shown in Figure 5.

Table 2 lists commonly used group 1 microinstructions, their assigned mnemonics, octal number, instruction format, logical sequence, the operation they perform, the number of states and the execution time at +5.0V and +10.0V, assuming a crystal frequency of 4 MHz and 8 MHz or a state time period of 500 ns and 250 ns, respectively. The same format is followed in Table 3 and 4 which correspond to group 2 and 3 microinstructions, respectively.

FIGURE 5



GROUP 1 MICROINSTRUCTION FORMAT

TABLE 2

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	OPERATION	NUMBER OF STATES	EXECUTION TIME (μ s)	
					IM6100 +5.0V	IM6100A +10.0V
NOP	7000	1	NO OPERATION —This instruction causes a 10 state delay in program execution, without affecting the state of the IM6100. It may be used for timing synchronization or as a convenient means of deleting an instruction from a program.	10	5.0	2.50
IAC	7001	3	INCREMENT ACCUMULATOR —The content of the AC is incremented by one (1) and carry out complements the Link (L).	10	5.0	2.50
RAL	7004	4	ROTATE ACCUMULATOR LEFT —The contents of the AC and L are rotated one binary position to the left. AC (1) is shifted to L and L is shifted to AC (11).	15	7.5	3.75
RTL	7006	4	ROTATE TWO LEFT —The contents of the AC and L are rotated two binary positions to the left. AC (1) is shifted to L and L is shifted to AC (10).	15	7.5	3.75
RAR	7010	4	ROTATE ACCUMULATOR RIGHT —The content of the AC and L are rotated one binary position to the right. AC (11) is shifted to L and L is shifted to AC (0).	15	7.5	3.75
RTR	7012	4	ROTATE TWO RIGHT —The contents of the AC and L are rotated two binary positions to the right. AC (10) is shifted to L and L is shifted to AC (1).	15	7.5	3.75
BSW	7002	4	BYTE SWAP —The right six (6) bits of the AC are exchanged or SWAPPED with the left six bits. AC (0) is swapped with AC (6), AC (1) with AC (7), etc. L is not affected.	15	7.5	3.75
CML	7020	2	COMPLEMENT LINK —The content of the link is complemented.	10	5.0	2.50
CMA	7040	2	COMPLEMENT ACCUMULATOR —The content of each bit of the AC is complemented having the effect of replacing the content of the AC with its one's complement.	10	5.0	2.50
CIA	7041	2,3	COMPLEMENT AND INCREMENT ACCUMULATOR —The content of the AC is replaced with its two's complement. Carry out complements the LINK.	10	5.0	2.50
CLL	7100	1	CLEAR LINK —The link is loaded with a binary 0.	10	5.0	2.50
CLL RAL	7104	1,4	CLEAR LINK—ROTATE ACCUMULATOR LEFT.	15	7.5	3.75
CLL RTL	7106	1,4	CLEAR LINK—ROTATE TWO LEFT.	15	7.5	3.75
CLL RAR	7110	1,4	CLEAR LINK—ROTATE ACCUMULATOR RIGHT.	15	7.5	3.75
CLL RTR	7112	1,4	CLEAR LINK—ROTATE TWO RIGHT.	15	7.5	3.75
STL	7120	1,2	SET THE LINK —The LINK is loaded with a binary 1 corresponding with a microprogrammed combination of CLL and CML.	10	5.0	2.50
CLA	7200	1	CLEAR ACCUMULATOR —The accumulator is loaded with binary 0's.	10	5.0	2.50
CLA IAC	7201	1,3	CLEAR ACCUMULATOR—INCREMENT ACCUMULATOR.	10	5.0	2.50
GLT	7204	1,4	GET THE LINK —The AC is cleared; the content of L is shifted into AC (11), a 0 is shifted into L. This is a microprogrammed combination of CLA and RAL.	15	7.5	3.75
CLA CLL	7300	1	CLEAR ACCUMULATOR—CLEAR LINK.	10	5.0	2.50
STA	7240	1,2	SET THE ACCUMULATOR —Each bit of the AC is set to 1 corresponding to a microprogrammed combination of CLA and CMA.	10	5.0	2.50

GROUP 1 OPERATION MICROINSTRUCTIONS

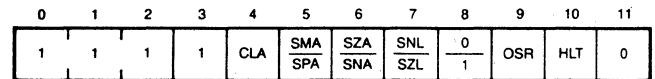
OPERATE INSTRUCTIONS CONTINUED

GROUP 2 MICROINSTRUCTIONS

Figure 6 shows the instruction format of group 2 microinstructions. Bits 4—11 may be set to indicate a specific group 2 microinstruction. If more than one of bits 4—7 or 9—10 is set, the instruction is a microprogrammed combination of group 2 microinstructions, which will be executed according to the logical sequence shown in Figure 6.

Skip microinstructions may be microprogrammed with CLA, OSR, or HLT microinstructions. Skip microinstructions which have a 0 in bit 8, however, may not be microprogrammed with skip microinstructions which have a 1 in bit 8. When two or more skip microinstructions are microprogrammed into a single instruction, the resulting condition on which the decision will be based is the logical OR of the individual conditions when bit 8 is 0, or, when bit 8 is 1, the decision will be based on the logical AND.

FIGURE 6



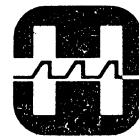
LOGICAL SEQUENCES:
 1 (Bit 8 is Zero) — SMA or SZA or SNL
 (Bit 8 is One) — SPA and SNA and SZL
 2 — CLA
 3 — OSR, HLT

GROUP 2 MICROINSTRUCTION FORMAT

TABLE 3

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	OPERATION	NUMBER OF STATES	EXECUTION TIME (μs)	
					HM6100 +5.0V	HM6100 +10.0V
NOP	7400	1	NO OPERATION—See GROUP 1 MICROINSTRUCTIONS	10	5.0	2.50
HLT	7402	3	HALT—Program stops at the conclusion of the current machine cycle. If HLT is combined with others in OPR 2, the other operations are completed before the end of the cycle.	10	5.0	2.50
OSR	7404	3	OR WITH SWITCH REGISTER—The content of the Switch Register if OR'ed with the content of the AC and the result is stored in the AC. The OSR INSTRUCTION TIMING is shown in Figure 7. The IM6100 sequences the OSR instruction through a 2-cycle execute phase referred to as OPR 2A and OPR 2B.	15	7.5	3.75
SKP	7410	1	SKIP—The content of the PC is incremented by 1, to skip the next sequential instruction.	10	5.0	2.50
SNL	7420	1	SKIP ON NON-ZERO LINK—The content of L is sampled, the next sequential instruction is skipped if L contains a 1. If L contains a 0, the next instruction is executed.	10	5.0	2.50
SZL	7430	1	SKIP ON ZERO LINK—The content of L is sampled, the next sequential instruction is skipped if L contains a 0. If the L contains a 1, the next instruction is executed.	10	5.0	2.50
SZA	7440	1	SKIP ON ZERO ACCUMULATOR—The content of the AC is sampled; the next sequential instruction is skipped if the AC has all bits which are 0. If any bit in the AC is a 1, the next instruction is executed.	10	5.0	2.50
SNA	7450	1	SKIP ON NON-ZERO ACCUMULATOR—The content of the AC is sampled; the next sequential instruction is skipped if the AC has any bits which are not 0. If every bit in the AC is 0, the next instruction is executed.	10	5.0	2.50
SZA SNL	7460	1	SKIP ON ZERO ACCUMULATOR, OR SKIP ON NON-ZERO LINK, OR BOTH	10	5.0	2.50
SNA SZL	7470	1	SKIP ON NON-ZERO ACCUMULATOR AND SKIP ON ZERO LINK	10	5.0	2.50
SMA	7500	1	SKIP ON MINUS ACCUMULATOR—If the content of AC (0) contains a 1, indicating that the AC contains a negative two's complement number, the next sequential instruction is skipped. If AC (0) contains a 0, the next instruction is executed.	10	5.0	2.50
SPA	7510	1	SKIP ON POSITIVE ACCUMULATOR—The contents of AC (0) are sampled. If AC (0) contains a 0, indicating that the AC contains a positive two's complement number, the next sequential instruction is skipped. If AC (0) contains a 1, the next instruction is executed.	10	5.0	2.50
SMA SNL	7520	1	SKIP ON MINUS ACCUMULATOR OR SKIP ON NON-ZERO LINK OR BOTH	10	5.0	2.50
SPA SZL	7530	1	SKIP ON POSITIVE ACCUMULATOR AND SKIP ON ZERO LINK	10	5.0	2.50
SMA SZA	7540	1	SKIP ON MINUS ACCUMULATOR OR SKIP ON ZERO ACCUMULATOR OR BOTH	10	5.0	2.50
SPA SNA	7550	1	SKIP ON POSITIVE ACCUMULATOR AND SKIP ON NON-ZERO ACCUMULATOR	10	5.0	2.50
SMA SZA SNL	7560	1	SKIP ON MINUS ACCUMULATOR OR SKIP ON ZERO ACCUMULATOR OR SKIP ON NON-ZERO LINK OR ALL	10	5.0	2.50
SPA SNA SZL	7570	1	SKIP ON POSITIVE ACCUMULATOR AND SKIP ON NON-ZERO ACCUMULATOR AND SKIP ON ZERO LINK	10	5.0	2.50
CLA	7600	2	CLEAR ACCUMULATOR—The AC is loaded with binary 0's.	10	5.0	2.50
LAS	7604	1,3	LOAD ACCUMULATOR WITH SWITCH REGISTER—The content of the AC is loaded with the content of the SR, bit for bit. This is equivalent to a microprogrammed combination of CLA and OSR.	15	7.5	3.75
SZA CLA	7640	1,2	SKIP ON ZERO ACCUMULATOR THEN CLEAR ACCUMULATOR	10	5.0	2.50
SNA CLA	7650	1,2	SKIP ON NON-ZERO ACCUMULATOR THEN CLEAR ACCUMULATOR	10	5.0	2.50
SMA CLA	7700	1,2	SKIP ON MINUS ACCUMULATOR THEN CLEAR ACCUMULATOR	10	5.0	2.50
SPA CLA	7710	1,2	SKIP ON POSITIVE ACCUMULATOR THEN CLEAR ACCUMULATOR	10	5.0	2.50

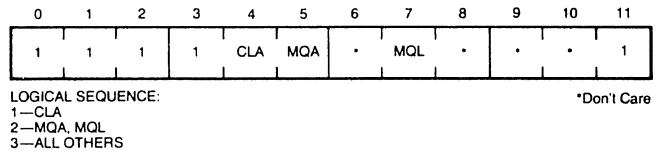
GROUP 2 OPERATE MICROINSTRUCTIONS



GROUP 3 MICROINSTRUCTIONS

Figure 7 shows the instruction format of group 3 microinstructions which requires bits 3 and 11 to contain a 1. Bits 4, 5 or 7 may be set to indicate a specific group 3 microinstruction. If more than one of the bits is set, the instruction is a microprogrammed combination of group 3 microinstructions following the logical sequence listed in Figure 7.

FIGURE 7



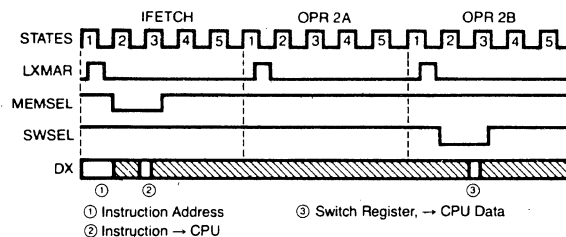
GROUP 3 MICROINSTRUCTION FORMAT

TABLE 4

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	OPERATION	NUMBER OF STATES	EXECUTION TIME (μ s)	
					HM6100 +5.0V	HM6100 +10.0V
NOP	7401	3	NO OPERATION—See Group 1 Microinstructions	10	5.0	2.50
MQL	7421	2	MQ REGISTER LOAD—The content of the AC is loaded into the MQ, the AC is cleared and the original content of the MQ is lost.	10	5.0	2.50
MQA	7501	2	MQ REGISTER INTO ACCUMULATOR—The content of the MQ is OR'ed with the content of the AC and the result is loaded into the AC. The original content of the AC is lost but the original content of the MQ is retained. This instruction provides the programmer with an inclusive OR operation.	10	5.0	2.50
SWP	7521	3	SWAP ACCUMULATOR AND MQ REGISTER—The content of the AC and MQ are interchanged accomplishing a microprogrammed combination of MQA and MQL.	10	5.0	2.50
CLA	7601	1	CLEAR ACCUMULATOR			
CAM	7621	3	CLEAR ACCUMULATOR AND MQ REGISTER—The content of the AC and MQ are loaded with binary 0s. This is equivalent to a microprogrammed combination of CLA and MQL.	10	5.0	2.50
ACL	7701	3	CLEAR ACCUMULATOR AND LOAD MQ REGISTER INTO ACCUMULATOR—This is equivalent to a microprogrammed combination of CLA and MQA.	10	5.0	2.50
CLA SWP	7721	3	CLEAR ACCUMULATOR AND SWAP ACCUMULATOR AND MQ REGISTER—The content of the AC is cleared. The content of the MQ is loaded into the AC and the MQ is cleared.	10	5.0	2.50

GROUP 3 OPERATE MICROINSTRUCTIONS

FIGURE 8



OSR INSTRUCTION TIMING

INPUT/OUTPUT TRANSFER INSTRUCTIONS (IOT)

The input/output transfer instructions, which have an OPCODE of 6_8 , are used to initiate the operation of peripheral devices and to transfer data between peripherals and the HM6100. Three types of data transfer may be used to receive or transmit information between the HM6100 and one or more peripheral I/O devices. PROGRAMMED DATA TRANSFER provides a straightforward means of communicating with relatively slow I/O devices, such as Teletypes, cassettes, card readers and CRT displays. INTERRUPT TRANSFERS use the interrupt system to service several peripheral devices simultaneously, on an intermittent basis, permitting computational operations to be performed concurrently with the data I/O operations. Both Programmed Data Transfers and Program Interrupt Transfers use the accumulator as a buffer, or storage area, for all data transfers. Since data may be transferred only between the accumulator and the peripheral, only one 12 bit word at a time may be transferred. DIRECT MEMORY ACCESS, DMA, transfers variable-size blocks of data between high-speed peripherals and the memory with a minimum of program control required by the HM6100.

IOT INSTRUCTION FORMAT

The Input/Output Transfer Instruction format, the number of states and the execution time at +5.0V and +10.0V, assuming a crystal frequency of 4 MHz and 8 MHz or a state time period of 500 ns and 250 ns, respectively is represented in Figure 9.

The first three bits, 0-2, are always set to 6_8 (110) to specify an IOT instruction. The next six bits, 3-8, contain the device selection code that determines the specific I/O device for which the IOT instruction is intended and, therefore, permit interface with up to 64 I/O devices. The last three bits, 9-11, contain the operation specification code that determines the specific operation to be performed. The nature of this operation for any given IOT instruction depends entirely upon the circuitry designed into the I/O device interface.

PROGRAMMED DATA TRANSFER

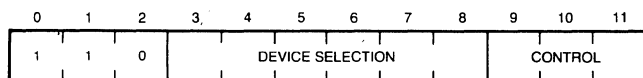
Programmed Data Transfer is the easiest, simplest, most convenient and most common means of performing data I/O. For micro-processor applications, it may also be the most cost effective

approach. The data transfer begins when the HM6100 fetches an instruction from the memory and recognizes that the current instruction is an IOT. This is referred to as IFETCH and consists of five (5) internal states. The HM6100 sequences the IOT instruction through a 2-cycle execute phase referred to as IOT_A and IOT_B . Bits 0-11 of the IOT instruction are available on DX 0-11 at $IOT_A \cdot LXMAR$. These bits must be latched in an external address register. DEVSEL is active low to enable data transfers between the HM6100 and the peripheral device(s). Input-Output Instruction Timing is shown in Figure 10. The selected peripheral device communicates with the HM6100 through 4 control lines— C_0 , C_1 , C_2 and SKP. In the HM6100 the type of data transfer, during an IOT instruction, is specified by the peripheral device(s) by asserting the control lines as shown in Table 5.

The control line SKP, when low during an IOT, causes the HM6100 to skip the next sequential instruction. This feature is used to sense the status of various signals in the device interface. The C_0 , C_1 , and C_2 lines are treated independently of the SKP line. In the case of a RELATIVE or ABSOLUTE JUMP, the skip operation is performed after the jump. The input signals to the HM6100, DX 0-11, C_0 , C_1 , C_2 , and SKP, are sampled at IOT_A during DEVSEL $\cdot XT_C$. The data from the HM6100 is available to the device(s) during DEVSEL $\cdot XT_C$. IOT_B cycle is internal to the HM6100 to perform the operations requested during IOT_A . Both IOT_A and IOT_B consist of six (6) internal states.

In summary, Programmed Data Transfer performs data I/O with a minimum of hardware support. The maximum rate at which programmed data transfers may take place is limited by the HM6100 instruction execution rate. However, the data rate of the most commonly used peripheral devices is much lower than the maximum rate at which programmed transfers can take place in the HM6100. The major drawback associated with Programmed Data Transfer is that the HM6100 must hang up in a waiting loop while the I/O device completes the last transfer and prepares for the next transfer. On the other hand, this technique permits easy hardware implementation and simple, economical interface design. For this reason, almost all devices except bulk storage units rely heavily on programmed data transfer for routine data I/O.

FIGURE 9



IOT INSTRUCTION FORMAT

Number of States	Execution Time (μs)	
	+5.0V	+10.0V
17	8.5	3.4

IOT NUMBER OF STATES/EXECUTION TIME

TABLE 5

CONTROL LINES			OPERATION	DESCRIPTION
C_0	C_1	C_2		
H	H	H	DEV \leftarrow AC	The contents of the AC is sent to the device.
L	H	H	DEV \leftarrow AC; CLA	The contents of the AC is sent to a device and then the AC is cleared.
H	L	H	AC \leftarrow AC V DEV	Data is received from a device, OR'ed with the data in the AC and the result is stored in the AC.
L	L	H	AC \leftarrow DEV	Data is received from a device and loaded into the AC.
*	H	L	PC \leftarrow PC + DEV	Data from the device is added to the contents of the PC. This is referred to as a RELATIVE JUMP.
*	L	L	PC \leftarrow DEV	Data is received from a device and loaded into the PC. This is referred to as an ABSOLUTE JUMP.

*Don't Care

PROGRAMMED I/O CONTROL LINES

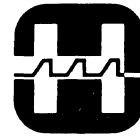
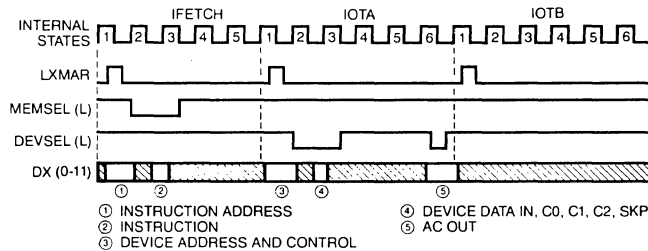


FIGURE 10



INPUT-OUTPUT INSTRUCTION TIMING

INTERRUPT TRANSFER

PROGRAM INTERRUPT TRANSFERS

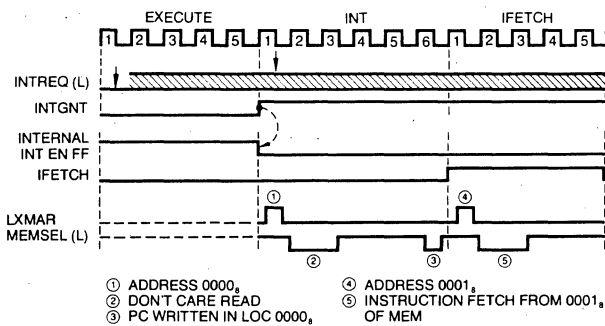
The program interrupt system may be used to initiate programmed data transfers in such a way that the time spent waiting for device status is greatly reduced or eliminated altogether. It also provides a means of performing concurrent programmed data transfers between the HM6100 and the peripheral devices. This is accomplished by isolating the I/O handling routines from the mainline program and using the interrupt system to ensure that these routines are entered only when an I/O device status is set, indicating that the device is actually ready to perform the next data transfer, or that it requires some sort of intervention from the running program.

The interrupt system allows certain external conditions to interrupt the computer program by driving the INTREQ input to the HM6100 Low. If no higher priority requests are outstanding and the interrupt system is enabled, the HM6100 grants the device interrupt at the end of the current instruction. After an interrupt has been granted, the

Interrupt Enable Flip-Flop in the HM6100 is reset so that no more interrupts are acknowledged until the interrupt system is re-enabled under program control.

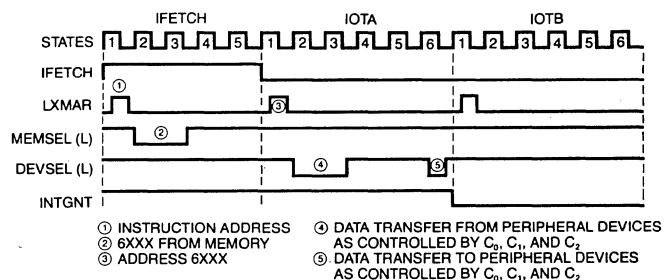
The current content of the Program Counter, PC, is deposited in location 0000₈ of the memory and the program fetches the instruction from location 0001₈. The return address is available in location 0000₈. This address must be saved in a software stack if nested interrupts are permitted. The INTGNT, Figure 11, signal is activated by the HM6100 when a device interrupt is acknowledged. This signal is reset by executing any IOT instruction as shown in Figure 12. The INTGNT signal is necessary to implement the Extended Memory Control hardware when more than 4K of memory is required. The INTGNT is also useful in implementing an External Vectored Priority Interrupt network.

FIGURE 11



DEVICE INTERRUPT GRANT TIMING

FIGURE 12



DEVICE INTERRUPT GRANT RESET TIMING

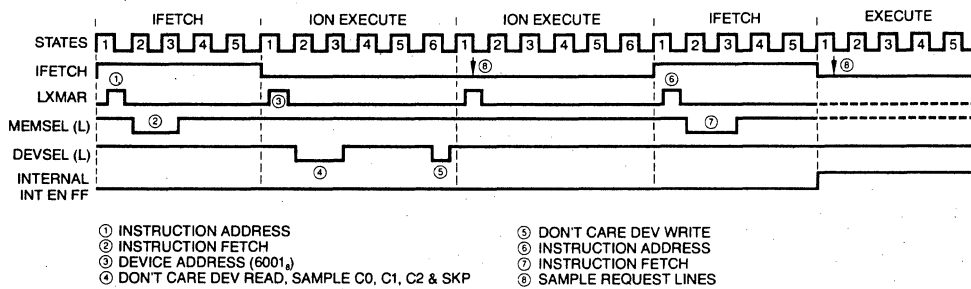
INPUT/OUTPUT TRANSFER INSTRUCTIONS (IOT) CONTINUED

TABLE 6

MNE-MONIC	OCTAL CODE	OPERATION
SKON	6000	SKIP IF INTERRUPT ON—If Interrupt system is enabled, the next sequential instruction is skipped. The Interrupt system is disabled.
ION	6001	INTERRUPT TURN ON—The internal interrupt acknowledge system is enabled. The interrupt system is enabled after the CPU executes the next sequential instruction. The INTERRUPT ENABLE TIMING is shown in Figure 13.
IOF	6002	INTERRUPT TURN OFF—The interrupt system is disabled. Note that the interrupt system is automatically disabled when the CPU acknowledges an INT request.
SRQ	6003	SKIP IF INT REQUEST—The next sequential instruction is skipped if the INT request bus is low.
GTF	6004	GET FLAGS—The following machine states are read into the indicated bits of AC. bit 0—Link bit 2—INT request bus bit 4—Interrupt Enable FF Other bits may be modified by external inputs (ex. Extended memory control).
RTF	6005	RETURN FLAGS—Link is restored from AC (0). Interrupt system is enabled after the next sequential instruction is executed. All AC bits are available externally to restore external states. (ex. Extended memory control).
SGT	6006	Operation is determined by external devices, if any.
CAF	6007	CLEAR ALL FLAGS—AC and Link are cleared. Interrupt system is disabled.

PROCESSOR IOT INSTRUCTIONS

FIGURE 13



INTERRUPT ENABLE FF ON (ION)

CONTROL PANEL INTERRUPT TRANSFER

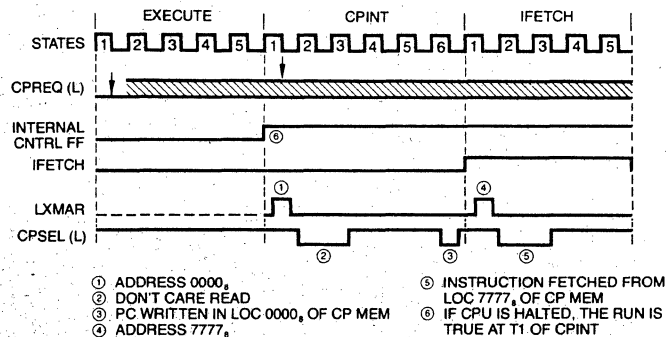
The HM6100 control panel is implemented in software. The software implementation of the control panel need not use any part of the main memory or change the processor state. This is an important feature since the final version of the system may not have a control panel and the system designer would like to use the entire capacity of the main memory for the specific system application.

The control panel communicates with the HM6100 with the Control Panel Request, CPREQ, line. The CPREQ is functionally similar to the INTREQ with some important differences. The CPREQ is granted even when the machine is in the HALT state. The HM6100 is temporarily put in the RUN state for the duration of the panel routine. The HM6100 reverts back to its original processor state after the panel routine has been executed.

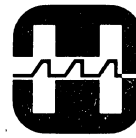
The CPREQ bypasses the interrupt enable system and the processor IOT instructions, ION and IOF, are ignored while the HM6100 is in the Control Panel Mode. Once a CPREQ is granted, the HM6100 will not recognize any DMAREQ or INTREQ until CPREQ has been fully serviced.

When a CPREQ is granted, Figure 14, the PC is stored in location 0000₈ of the Panel Memory and the HM6100 resumes operation at location 7777₈ of the Panel Memory. The Panel Memory would be organized with RAM's in the lower pages and PROM's in the higher pages. The control panel service routine would be stored in the higher pages in the nonvolatile PROM's, starting at 7777₈.

FIGURE 14



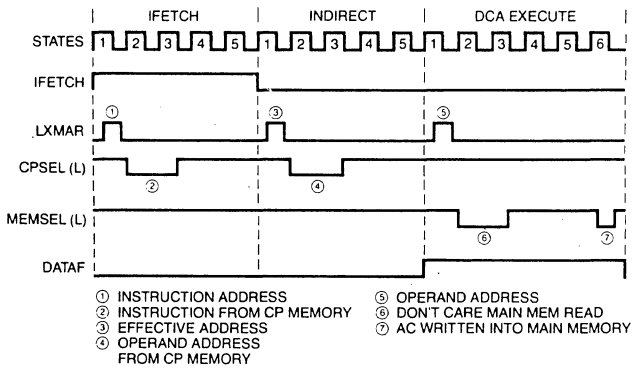
CONTROL PANEL INTERRUPT GRANT TIMING



A Control Panel Flip-Flop, CNTRL FF, which is internal to the HM6100, is set when the CPREQ is granted. The CNTRL FF prevents further CPREQ's from being granted.

As long as the CNTRL FF is set, the Control Panel Memory Select, CPSEL, is active instead of the Memory Select, MEMSEL, for memory references. The CPSEL signal may, therefore, be used to distinguish the Control Panel Memory from the Main Memory. However, during the Execute phase of indirectly addressed AND, TAD, ISZ or DCA instructions, the MEMSEL is made active. The instructions are always fetched from the control panel memory. The operand address for indirectly addressed AND, TAD, ISZ or DCA refers first to the control panel memory for an effective address, which, in turn, refers to a location in the main memory. A main memory location may, therefore, be examined and changed by indirectly addressed TAD and DCA instructions, Figure 15, respectively. Every location in the main memory is accessible to the control panel routine.

FIGURE 15



"DCA INDIRECT" IN CONTROL PANEL ROUTINE

Exiting from the control panel routine is achieved by executing the following sequence with reference made to Figure 16.

ION

JMP I 0000₈ (Loc 0000₈ in CPMEM)

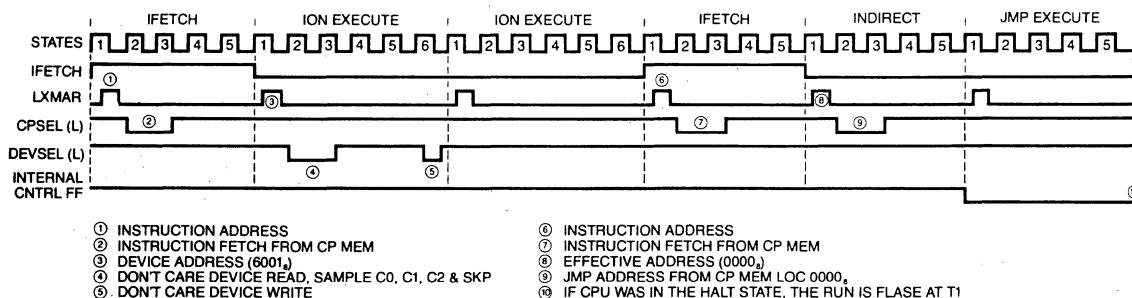
The ION, 6001₈, instruction will reset the CP FF after executing the next sequential instruction. The ION will not affect the interrupt system since the CNTRL FF is still active. Location 0000₈ of the CPMEM contains either the original return address deposited by the IM6100 when the CP routine was entered, or it may be a new starting address defined by the CP routine, for example, by activating the LOAD ADDRESS SWITCH. CPREQ's are normally generated by the manual actuation of the control switches. If the CPU registers must be displayed in real-time, the CPREQ's must be generated by a timer at fixed intervals.

The designer may also make use of the control panel features to implement Bootstrap loaders in the CP Memory so that the loader will be "transparent" to the main memory. Programs will be loaded by DCA I POINTER instruction, the pointer being developed in the CP RAM to point to the main memory location to be loaded.

Approximately 64 P/ROM locations are sufficient to implement all the functions of the PDP8/E Control Panel. The HM6100 provides for a 12 bit switch register which can be read by the HM6100 under program control with the OR THE SWITCH REGISTER, OSR, instruction even without a control panel.

An RTF, 6005₈, instruction also resets the internal CNTRL FF. Exiting from a panel routine can be achieved by activating the RESET line since RESET has a higher priority than CPREQ as shown in Figure 21. If the RUN/HLT line is pulsed while the HM6100 is in the panel mode, it will 'remember' the pulse(s) but defer any action until the HM6100 exits from the panel mode.

FIGURE 16



"ION; JMP I 0000" IN CONTROL PANEL ROUTINE

INPUT/OUTPUT TRANSFER INSTRUCTIONS CONTINUED

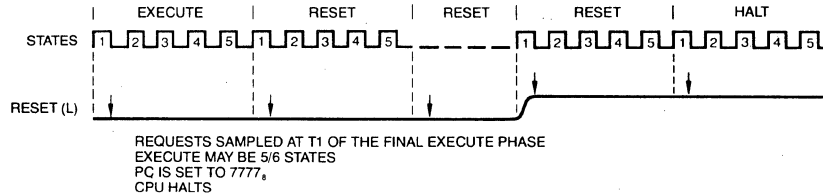
RESET

The Reset initializes all internal HM6100 flags and clears the AC and the LINK. The machine is halted.

The HM6100 remains in the Reset state as long as the Reset line is low as shown in Figure 17. The DX lines are three stated. The HM6100 continues to provide the external timing signals XT_A, XT_B and XT_C. All SEL lines are high.

The PC is set to 7777_h. In most applications, the higher memory locations utilize P/ROM's or ROM's. Therefore, a power-up routine starting at the highest memory location can be used to initialize the system.

FIGURE 17



RESET TIMING

RUN/HALT

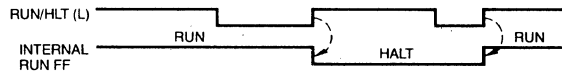
RUN/HLT changes the state of the HM6100's RUN/HLT flip-flop. Pulsing the line low causes the IM6100 to alternately run and halt as shown in Figure 18. The RUN/HLT line is normally high. The HM6100 recognizes the positive transition of the signal.

The RUN/HLT flip-flop can be put in the halt state under program control by executing the HLT, 7402_h, instruction. When the HM6100 is halted, RUN/HLT is functionally identical to the CONTINUE switch of the PDP8/E control panel.

If the HM6100 is in the halt state, the RUN signal is low. The RUN signal can be used to power down external circuitry for a low power system.

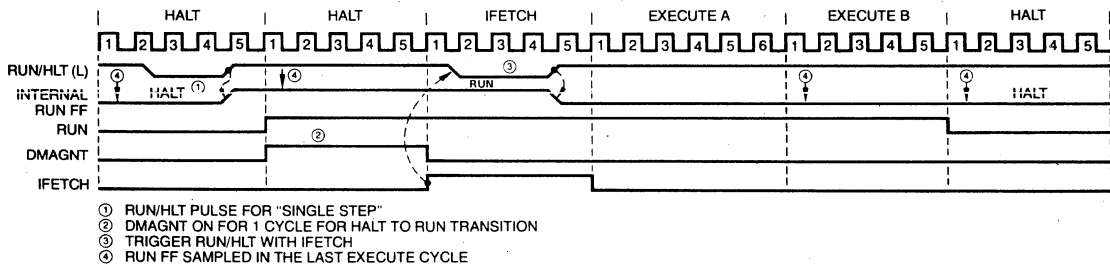
The RUN/HLT can also be used to make the HM6100 execute one instruction at a time as shown in Figure 19. The RUN/HLT combines the functional features of STOP, CONTINUE, and SINGLE INSTRUCTION as defined by the PDP8/E Control Panel.

FIGURE 18

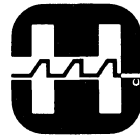


RUN/HALT TIMING

FIGURE 19



"SINGLE STEP" WITH RUN/HLT

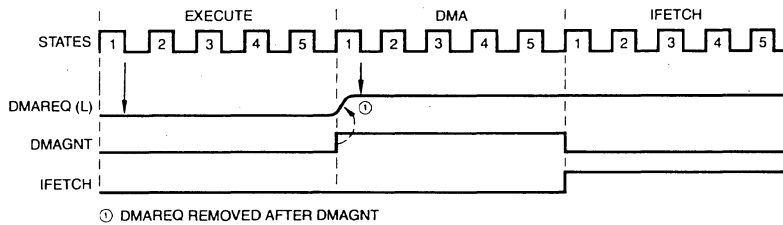


DIRECT MEMORY ACCESS (DMA)

Direct Memory Access, sometimes called data break, is the preferred form of data transfer for use with high-speed storage devices such as magnetic disk or tape units. The DMA mechanism transfers data directly between memory and peripheral devices. The HM6100 is involved only in setting up the transfer; the transfers take place with no processor intervention on a "cycle stealing" basis. The DMA transfer rate is limited only by the bandwidth of the memory and the data transfer characteristics of the device.

The device generates a DMA Request when it is ready to transfer data. The HM6100 grants the DMAREQ by activating the DMAGNT signal at the end of the current instruction as shown in Figure 20. The HM6100 suspends any further instruction fetches until the DMAREQ line is released. The DX lines are tri-stated, all SEL lines are high, and the external timing signals XT_A, XT_B, and XT_C are active. The device which generated the DMAREQ must provide the address and the necessary control signals to the memory for data transfers. The DMAREQ line can also be used as a level sensitive "pause" line.

FIGURE 20



① DMAREQ REMOVED AFTER DMAGNT

DIRECT MEMORY ACCESS (DMA)

INTERNAL PRIORITY STRUCTURE

After an instruction is completely sequenced, the major state generator scans the internal priority network as shown in Figure 21. The state of the priority network decides the next sequence of the HM6100

The request lines, RESET, CPREQ, RUN/HLT, DMAREQ and INTREQ, are sampled in the last cycle of an instruction execution, at time T1. The worst case response time of the HM6100 to an external request is, therefore, the time required to execute the longest instruction preceded by any 6-state execution cycle. For the HM6100, this is an autoindexed ISZ, 22 states, preceded by any 6-state execution cycle instruction. The worst case response time is, therefore, 28 states, 14 μ s at 5 volts.

When the HM6100 is initially powered up, the state of the timing generator is undefined. The generator is automatically initialized with a maximum of 68 clock pulses. The request inputs, as the HM6100 is powered on, must span at least 92 clock pulses to be recognized, 68 clocks for the counter to initialize and a maximum of two HM6100 cycles (20 to 24 clocks) for the state generator to sample the request lines.

The internal priority is RESET, CPREQ, RUN/HLT, DMAREQ, INTREQ, and IFETCH.

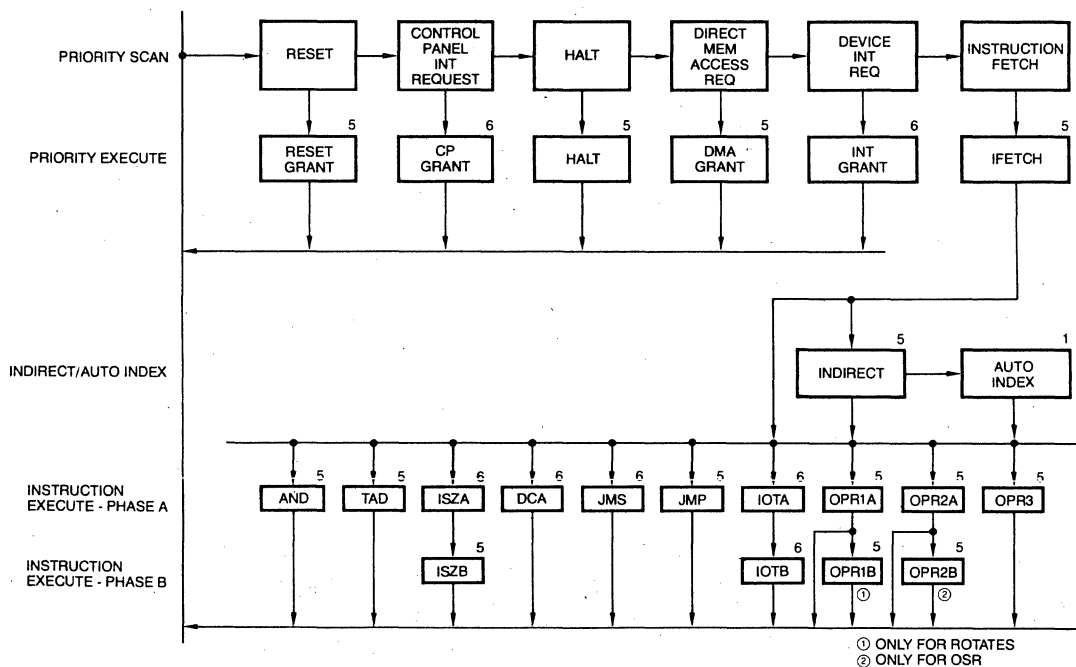
IFETCH

If no external requests are pending, the HM6100 fetches the next instruction pointed to by the contents of the PC. The IFETCH line is active during the cycle in which the instruction is fetched. External devices can monitor DX, 0-2, during IFETCH·XT_A to determine the functional class of the current instruction. For example, the external memory extension hardware must know when JMP or JMS instructions are fetched to implement the Extended Memory Control.

The Programmable Logic Array, PLA, in the HM6100 sequences the HM6100 to execute the fetched instruction. All INDIRECT and AUTOINDEX Memory Reference Instructions go through a common state sequence to generate the Effective Address, EA, of the operand. The subsequent sequence, referred to as the EXECUTE phase, is controlled by the functional class of the instruction. The EXECUTE phase of AND, TAD, DCA, JMS, JMP and OPR Group 3 Microinstruction consists of only one cycle. ISZ and IOT have a 2-cycle EXECUTE phase. OPR Group 1 and Group 2 Microinstructions have an optional second cycle, depending on the microcoding of the OPR instructions. An HM6100 cycle consists of 5 states, T₁, T₂, T₃, T₄, and T₅, with an optional sixth state, T₆, for Output Transfers (WRITE).

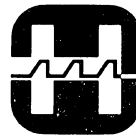
The state sequence for internal (processor) and external IOT instructions are identical. The Device Address and Control bits are available in the External Address Register for internal IOT instructions. External hardware, for example Extended Memory Control, can control the C-lines for data transfers to implement Get Flags (GTF), Return Flags (RTF), and Clear All Flags (CAF) instructions. External Control of the C-lines is necessary to implement these internal IOT instructions since the flag bits may be distributed both inside and outside the HM6100.

FIGURE 21



MAJOR PROCESSOR STATES AND NUMBER OF CLOCK CYCLES IN EACH STATE

PDP-8/E COMPATIBILITY



**HARRIS
SEMICONDUCTOR**
A DIVISION OF HARRIS CORPORATION

The HM6100 and the PDP-8/E MP12 and D112 are software compatible. The basic PDP-8/E paper-tape software system supplied by Digital Equipment Corporation will operate properly with the HM6100. This basic software package includes Binary Loaders, PAL III Assembler, Symbolic Editor, Dynamic Debugging Technique (DDT), Octal Debugging Technique (ODT), 23 Bit Floating Point Package and FOrmula CALculator (FOCAL)[®]. The HM6100 will execute the complete set of CPU diagnostics for PDP-8/E.

Since the bus structure of the HM6100 can be adapted to provide a subset of the PDP-8/E OMNIBUS[®] signals, all programmed I/O interfaces for the PDP-8/E, for example, Teletype, Papertape Reader/Punch, etc., will operate with the HM6100 without any hardware or software modification.

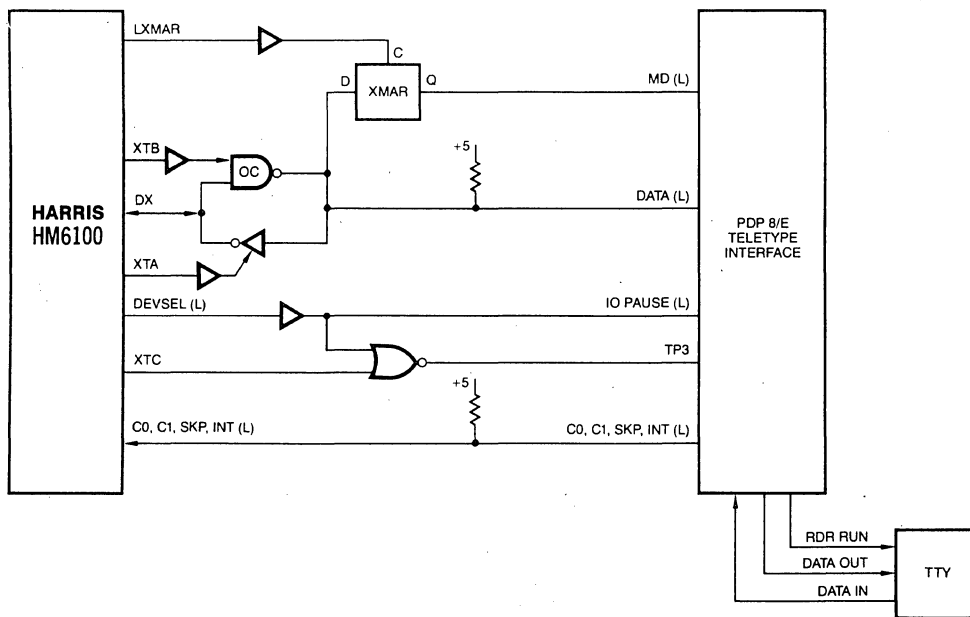
The Direct Memory Access, DMA, structure of the HM6100 and PDP-8/E are different, the HM6100 DMA structure is similar to the PDP-8 1-CYCLE BREAK, but not compatible.

The HM6100 handles 4K words of memory directly. Like the PDP-8/E, an external Extended Memory Control element can be used to extend the addressing space up to 32K. All necessary control and timing signals to implement the memory extension controller are generated by the HM6100.

The Extended Arithmetic Element, EAE, and the User Flag; UF, processor options of the PDP-8/E cannot be used with the HM6100. The EAE is used for hardwired Multiply/Divide and the UF for timesharing.

The HM6100 treats the Control Panel as a programmed I/O device with certain special features. The Control Panel has a dedicated INT request line to the HM6100 and the control panel program can reside in a separate memory, distinct from the normal program memory. The control panel service routine can be made transparent to the user and the user program can occupy the entire 4K of main memory. The bootstrap routines may also reside in the dedicated control panel memory. Unlike the PDP-8/E, the HM6100 bootstrap routines and the loaded user programs, can, therefore, share common address space.

FIGURE 22



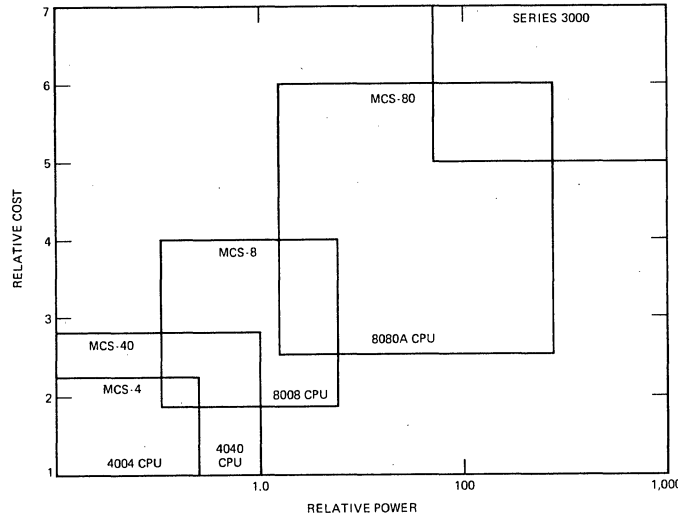
EXAMPLE OF A PDP-8/E PROGRAMMED I/O PERIPHERAL INTERFACE

[®]Registered Trademark of Digital Equipment Corporation

Why more engineers use the Intel 8080 system

Intel microcomputer systems.

Since 1971, equipment manufacturers have used Intel microcomputer systems to reduce the cost and increase the versatility of their products. These LSI systems have replaced hardwired assemblies in hundreds of applications, such as POS equipment, intelligent terminals, analytical instruments, process controls, communications systems, rapid transit toll systems, word processors and business equipment.



Today, Intel delivers five microcomputer system families. Four are based on MOS central processor units and the fifth on Series 3000 Schottky bipolar LSI central processor elements. All the microprocessors are supported with optional I/O, peripheral and memory building blocks, which provide a large variety of system configurations in each family.

As indicated by the graph above, Intel systems cover the broadest possible cost-performance range. This lets you produce the most cost-effective design, whether your application calls for low cost replacement of electromechanical controls or high performance processing.

Why more engineers choose the 8080 system.

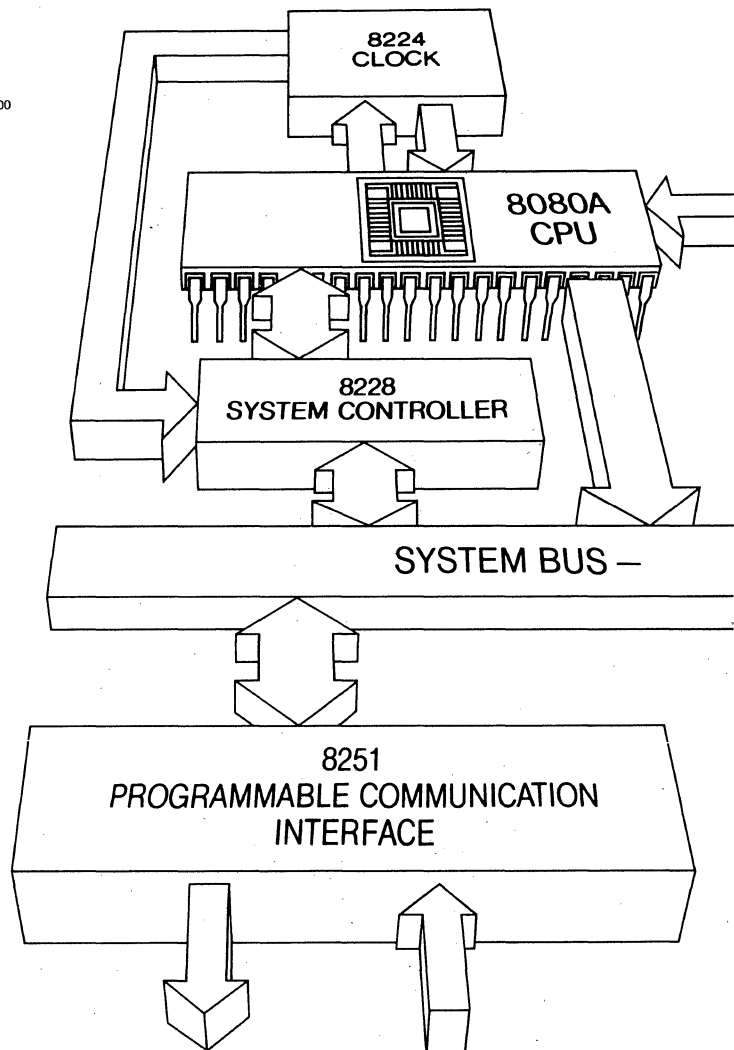
The broad center of the microcomputer cost-performance range is covered by the Intel® 8080 system — the 8080A CPU, other MCS-80™ system components, and nine software packages. First delivered in December, 1973, the 8080 system has become the basis for more new OEM products than all other microcomputers combined.

Some major reasons for the 8080 system's popularity are a powerful CPU group with four CPU options, five programmable I/O and peripheral devices, 21 other system components, production deliveries since April, 1974, major second sources, and the industry's most useful software and hardware development systems. These add up to higher profitability for the 8080 user.

How the 8080 system increases your profitability.

MCS-80™ systems feature a simple building block architecture and high performance, enabling them to replace hundreds of TTL packages and numerous discrete components in a great variety of control and processing applications.

With MCS-80™ building blocks, complete LSI systems are easy to design, program and modify. As a result, the 8080 system helps you get new products to market faster and at lower cost; sharply reduces documentation, production and maintenance overhead; and simplifies enhancement of your product line to meet changing market conditions.



Intel

MICROPROCESSOR

than all other microcomputers combined.

The system's completeness solves design problems.

MCS-80™ components form complete systems with many optional configurations. They eliminate the problems of hardwired design by integrating control and processing functions in LSI blocks that interface with one another through a standard system bus.

The systems building blocks include:

- The basic CPU Group, which defines and drives the bus — the 8080A CPU, 8224 Clock Generator and 8228 System Controller.
- Three CPU options for higher speed and extended temperature range applications.
- Twelve I/O and peripherals options, five are programmable LSI devices that control and communicate with external equipment in software selectable modes.
- Thirteen memory options, including 8K erasable PROMs, 16K ROMs, low power 1K CMOS RAMs, and low cost 4K RAMs — all with industry standard configurations for ease of use and economy.

You choose the blocks, program the CPU, check out the hardware and software, and then make the program part of the system by storing it in read-only memory. A program change is usually the only modification required to adapt the microcomputer system to changes and enhancements of your product line.

Intel support minimizes development time.

Intel has supported designers of microcomputer based products since 1971. Today, we back 8080 system users with:

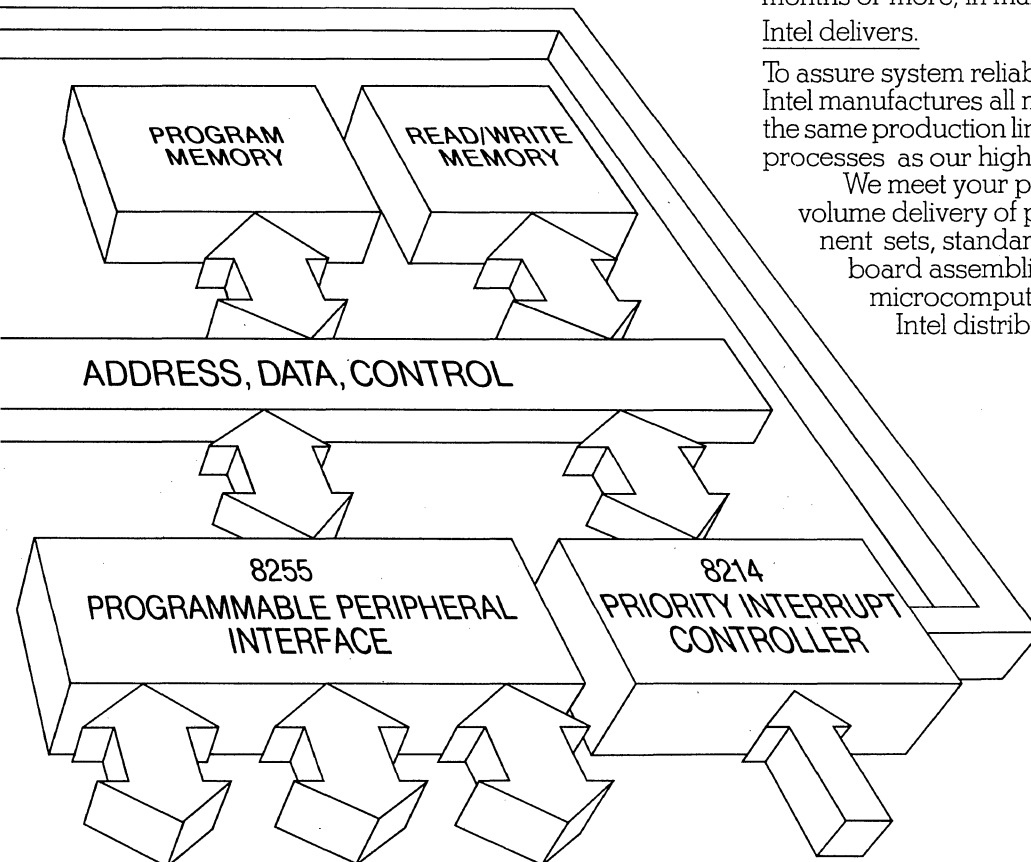
- A third-generation microcomputer development system — the Intellec® MDS-800. It is the first system to support simultaneous development of hardware and software. Moreover, with the MDS-800 you can now develop your system in its actual operating environment.
- Nine software packages — six Intellec® resident products and three cross products for rapid program design with symbolic and high level languages.
- System design kits — the new MCS-80™ kit provides a complete system's hardware, circuit card, control program and documentation.
- Seven reference and programming manuals — complete documentation of 8080 hardware, software and development systems.
- User's program library — over a hundred programs developed by 8080 system users.
- Training for engineers and programmers — courses and workshops at Intel regional centers, or on-site.
- Applications assistance — provided in the field by the industry's most experienced staff.

These systems and services eliminate repetitious debugging and help prevent false starts. They can cut months from your product development cycle — six months or more, in many cases.

Intel delivers.

To assure system reliability, economy and delivery, Intel manufactures all microcomputer components on the same production lines and with the same processes as our high volume memory products.

We meet your production requirements with volume delivery of performance matched component sets, standard board systems, or custom board assemblies. In addition, we stock microcomputer systems world-wide at Intel distributors.



The most complete hardware system.

MCS-80™ system components are performance matched to make system design, assembly and modification as easy as possible. Higher performance options include CPU instruction cycle times down to 1.3 microseconds or operation at -55 to +125°C.

The components interface with each other through a standard system bus, defined and controlled by the CPU Group. The group simplifies timing throughout the system by making all CPU inputs asynchronous in nature. Combined with performance matching, this approach results in a simple, building block architecture.

To provide complete systems in scores of configurations, there are 27 I/O, peripherals and memory options. You just choose the blocks needed to interface,

control and communicate with external equipment and connect them to the bus. All major blocks are software-configurable, so changes in product models usually require little or no change in an MCS-80™ system's hardware design.

Start with the powerful CPU Group.

The bus drive and system controls required for simple interface are built into the CPU Group, along with the auxiliary timing and control functions most designs require. Simple interface and high performance are assured by the use of two LSI technologies: silicon gate n-channel MOS in the 8080A CPU, and Schottky bipolar in the 8224 Clock Generator and 8228 System Controller.

The 8080A CPU is a byte processor with vectored interrupt, unlimited subroutine nesting and direct addressing of up to 512 I/O lines and 65 kilobytes of memory. An 8080 system can operate with almost any

	Part No.	MCS-80 System Components Description
CPU GROUP	8080A	8 bit CPU, 2 μsec Cycle Clock Generator System Controller
	8224	
	8228	
CPU OPTIONS	8080A-1	1.3 μsec cycle 1.5 μsec cycle 2 μsec cycle (-55 to +125°C)
	8080A-2	
	M8080A	
I/O	8212	8-bit I/O Port
	8251	Programmable Communications Interface
	8255	Programmable Peripheral Interface
PERIPHERALS	8205	1 of 8 Binary Decoder
	8210	Dynamic RAM Driver (8107B)
	8214	Priority Interrupt Control Unit
	8216	Bidirectional Bus Driver
	8226	Bidirectional Bus Driver
	8222	Dynamic RAM Refresh Controller (8107B)
	8253	Programmable Interval Timer
	8257	Programmable DMA Controller
8259	Programmable Interrupt Controller	
PROMs	8604	512 x 8, 100 ns 256 x 8 Erasable, 1.3 μs 512 x 8 Erasable, 450 ns 1K x 8 Erasable, 450 ns
	8702A	
	8704	
	8708	
ROMs	9302	256 x 8, 1μs 1K x 8, 450 ns 2K x 8, 850 ns
	8308	
	8316A	
RAMs	5101	256 x 4 Static CMOS, 650 ns 256 x 4 Static, 850 ns 1K x 1 Static, 650 ns 1K x 1 Static, 450 ns 256 x 4 Static, Common I/O, 850 ns 4K x 1 Dynamic, 420 ns
	8101-2	
	8102A-6	
	8102A-4	
	8111-2	
	8107B	

number of peripherals because the CPU is ideal for applications involving multilevel priority interrupts and DMA (direct memory address).

The crystal controlled 8224 generates TTL & MOS clocks, power-on reset and other timing functions. A high current, bidirectional bus driver and single-level interrupt control are integrated with the asynchronous bus control logic in the 8228 System Controller.

Add more versatile I/O and peripheral blocks.

The system's five programmable I/O and peripheral blocks eliminate the hardwired design normally required to operate external equipment. Each is a general purpose replacement for up to 75—or more—TTL packages.

System software can reconfigure these blocks "on the fly," dynamically adapting the system to changes in control and communications modes, interrupt priorities and other functions. Or, you can program predefined modes. Either way you get a lower cost, more versatile system with minimum inventory requirements.

Large system requirements for additional bus drive and expansion of memory and I/O are handled by Schottky bipolar components.

For maximum economy and ease of use, all MCS-80™ memory circuits have industry standard configurations. They are Intel standard products, selected for lowest cost and matched to system performance. The 15 options range from low power CMOS RAMs to high density PROMs and ROMs.

<p>Built into the CPU Group are the extra functions most designs require, as well as central logic and bus control:</p> <ul style="list-style-type: none"> • TTL & MOS crystal controlled clocks for system timing. • Auxiliary timing functions and single level interrupt control. • High current sinking capability to keep memory and I/O interfaces simple regardless of system size.
<p>Implements virtually any 8-bit I/O function with parallel latch/buffer and bus service request logic, Schottky bipolar for 15 mA output drive.</p> <p>Operates under program control in virtually all serial data transmission protocols in use today, including IBM Bi-Sync.</p> <p>Three 8-bit ports, software configurable for interface to printers, keyboards, displays, motor drives . . .</p>
<p>Expands memory and I/O address capability, Schottky bipolar for high speed.</p> <p>High voltage clock driver and quad address driver, two enable inputs simplify address or data decoding.</p> <p>Provides eight levels of interrupt control, cascades for simple expansion, current status register saves memory.</p> <p>Non-inverting 4-bit, Schottky bipolar driver, 50mA outputs drive long bus lines and terminations.</p> <p>Inverting version of 8216 Bidirectional Bus Driver.</p> <p>Controls refresh of large, asynchronous dynamic RAM system, has adjustable control oscillator and internal address multiplexer.</p> <p>Controls three active intervals with independent 16-bit counters at DC to 3 MHz, counts binary or BCD.</p> <p>Provides four channels of priority DMA request logic for direct access of peripherals & memories.</p> <p>Eight-level interrupt controller, priority algorithms can be varied with software, expandable to 64 levels.</p>
<p>All PROMs can be automatically programmed with the Intellec® MDS PROM programmer peripheral.</p> <ul style="list-style-type: none"> • High speed programming — 1ms/bit for 8604 bipolar Schottky PROM, and 8704, 8708 reprogrammable MOS PROMs. • All 2048 bits of 8702A reprogrammable MOS PROM can be programmed in 2 minutes.
<p>8302 2K ROM directly replaces 8702A PROM</p> <p>8308 8K ROM directly replaces 8704 or 8708 PROMs</p> <p>High density program storage with 8316A 16K ROM</p>
<p>CPU interfaces directly with static RAMs.</p> <ul style="list-style-type: none"> • 5101 CMOS RAM reduces standby power to 75nW/bit. • Static RAMs are the low-cost, easy to use approach for small and medium systems. <p>Dynamic 4K RAM reduces cost and improves speed of large systems.</p> <ul style="list-style-type: none"> • System design simplified by use of Intel drivers and refresh controllers.

The most useful development systems.

Intel supplies 8080 system users with the industry's most advanced development and software systems, complete documentation, design kits, training courses and application assistance. They support product development from initial concept through prototyping and into production.

Intellec® MDS-800 microcomputer development system.

Months can be cut from a product development cycle with the Intellec® MDS-800. It provides all the programming, prototyping and diagnostic resources required for rapid development. It also serves as an

automated instrument for troubleshooting production assemblies and for field engineering and programming.

As the first system to support simultaneous development of software and hardware, the Intellec® MDS-800 makes it practical to integrate hardware/software development early in the cycle. Furthermore, prototypes can be debugged in the actual product environment with the In-Circuit Emulator. These advances eliminate repetitious debugging and virtually guarantee that production models will operate properly. 8080 software packages work as a system.

Choose the optimum method of programming your system.

Compose programs with an efficient, symbolic assembly language. The Intellec® MDS-800 and resident software translate the programs into code and provide real-time emulation on 8080 hardware for checkout.

MICROCOMPUTER DEVELOPMENT SYSTEM	Intellec® MDS	With its ICE-80 In-Circuit Emulator module, the Intellec® MDS supports programming, prototyping and hardware/software debugging in the product's own environment. The mainframe is an 8080 system with expandable memory and I/O, DMA, interrupt logic, multiprocessor bus, clocks, and power supplies. Peripherals include diskette system, bipolar ROM simulator, universal PROM programmer, high speed paper tape reader, and standard interfacing for a CRT console, teletype-writer, high speed tape punch and line printer.
COMPREHENSIVE SOFTWARE PACKAGES	System Monitor	Supports the system's comprehensive diagnostic aids, controls the system and drives peripherals. Enables programs to be checked out in real time and supports simultaneous software/hardware debugging. Allows use of Intellec® MDS-800 hardware as prototyping resources, provides linkage to special peripherals, and loads developed programs into PROMs via PROM programmer.
	Macro Assembler	You can compose 8080 programs in a symbolic assembly language, which the macro assembler translates to machine code. There's no need to rewrite similar program segments. Like MAC-80, this package provides full macro and conditional assembly capabilities.
	Text Editor	A comprehensive tool for program entry and correction. Edits characters or lines of text. Commands include string search, substitution, insertion and deletion. The monitor provides I/O and other facilities required for easy entry and editing.
	DOS	Intel's new diskette operating system substantially reduces the time required to assemble, edit and execute programs. It's comprehensive file management capabilities enable program and data files to be represented symbolically. Disk files can be created, edited, assembled and executed easily and quickly, through simple commands from the system console.
	ICE-80	The In-Circuit Emulator ICE-80 provides a unique powerful tool for total hardware/software system debug through the Intellec® MDS. ICE-80 allows all the resources of the MDS to be used directly in the prototype environment to run it, debug it and perform final production and field testing. It also allows software to be developed simultaneously with the prototype and to run on the prototype from the earliest possible time.
	ROM-SIM	The Rom Simulator is a high speed, random access memory which simulates Intel bipolar PROMs and ROMs. Its 130 ns access time eliminates the necessity to program and use bipolar PROMs/ROMs when ultra high speed memory is required during prototype development.

TRAINING	Intel regional training centers give courses in system design and programming, and also conduct weekly workshops that provide hands-on experience. On-site courses and seminars are also available.
APPLICATIONS ASSISTANCE	Call the nearest Intel sales office. Assistance is available in the field through Intel field applications engineers and field marketing engineers.
PRODUCTION SUPPORT	Intel delivers standard subsystems, standard boards and custom boards, as well as system components. Standard products are stocked world-wide at Intel distributors.

Intel

MICROPROCESSOR

Design your software rapidly with Intel's PL/M high level language or cross macro assembler and simulator, using your own large computer or a time shared network.

Combine both methods. The resident and cross products work together as a system, using fully compatible assembly language and producing machine code which may be loaded on the Intellec® MDS-800.

Many 8080 system programmers prefer the third approach, since it allows high level design to be done with minimum computer charges and retains the advantages of integrated software/hardware development with the Intellec® MDS-800.

Design kits: the easiest way to get started.

The MCS-80™ System Design Kit contains all the components of a basic 8080 system, all board assembly parts including the PC board, a control program, and design manuals.

To order the MCS-80™ Design Kit call your nearest Intel franchised U.S. distributor: Almac/Stroum, Component Specialties, Cramer, Elmar, Hamilton-Avnet, Industrial Components, Liberty, Pioneer, Sheridan or L.A. Varah. In Europe or the Orient, contact the Intel Marketing Office for the name of your nearest Intel distributor.

Intellec® MDS Development Systems, software and all documentation are available now.

MCS-80 SYSTEM DESIGN KIT	<p>This kit contains all the components and software required to assemble and operate a basic 8080 system:</p> <ul style="list-style-type: none"> • CPU Group (8080A, 8224, 8228) • Two Programmable I/O blocks (8251 and 8255) • Two decoders (8205) • PROM and RAM memory (8708, two 8111) • Printed circuit board and connectors • Clock crystal and other required components • Control program (monitor stored in ROM) • 8080 system user's and programming manual
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CROSS PRODUCT SOFTWARE	PL/M™ Cross Compiler	Developed by Intel in 1973, PL/M is the only high level program language for microcomputer system software design. It has significantly reduced programming costs. It produces code that can be stored in ROM. Should you ever need to use machine language coding, PL/M also provides the mechanism for linking to assembly language routines.	Time Sharing Networks <u>United States:</u> United Computing GE Tymshare <u>Europe:</u> Tymshare Timesharing LTD Honeywell <u>Japan:</u> Dentsu <u>Canada:</u> GE <u>Australia:</u> Honeywell
	MAC-80 Cross Assembler	This powerful macro assembler simplifies software design and eliminates the need to write redundant code. It has full macro capability, coupled with conditional assembly directives. The assembly language is fully compatible with the Intellec® resident assembler.	
	INTERP/80 Simulator	INTERP/80 helps you to quickly debug your programs. It enables computers to simulate program execution by the 8080A CPU. The package has complete debugging facilities, including all timing details, breakpoints, full file buffered I/O, and a host of commands that permit you to examine and modify program execution.	
	Availability	All three cross products are written in ANSI standard FORTRAN IV. All run on medium or large scale computers, 32-bit Integer format. They can be purchased from Intel on magnetic tape or used via the computer time sharing networks listed at the right.	

USER'S LIBRARY	This large library contains hundreds of 8080 programs, such as floating point math package, multiple precision arithmetic routines, a quick-sort program, a floating point I/O conversion package, BCD to/from binary, binary to ASCII and gray to binary conversion. Members receive a manual documenting programs in the library, plus frequent updates. Memberships are free to users who submit accepted programs.
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DOCUMENTATION	<ul style="list-style-type: none"> • 8080 Microcomputer Systems User's Manual* • Intellec® MDS Hardware Reference Manual • Intellec® MDS Operator's Manual** • 8080 Assembly Language Programming Manual** *Includes MCS-80™ system design information and data sheets for system components. **Also documents resident software. • PL/M Programming Manual • MAC-80 User's Manual • INTERP/80 User's Manual
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intel® Microcomputers. First from the beginning.

Intel
MICROPROCESSOR

MOSTEK'S F8 ...The benchmark in programmable logic.

VERSATILE .. EFFICIENT .. COST EFFECTIVE

The ultimate goal, from F8 design concept through development and production, was to produce the most versatile, efficient, cost-effective microprocessor system available today. To accomplish this, five stringent parameters, based on user experience with other systems, were set forth as guidelines for the F8.

- Minimum Parts Count
- Cost Effectiveness
- Simple Peripheral Interfaces
- Easy Expansion through Modular Architecture
- Simplified Programming and Debugging

HOW WERE F8 GOALS MET ?

By . . . unique system partitioning the system functions have been divided among the various circuits of the F8 family to provide sophisticated modularity. As a result, it is now possible to build a minimum microprocessor system with **only two devices**. To this system PSU, RAM and I/O devices can be added to form medium size or memory intensive systems with a minimum use of external parts. And, finally, for

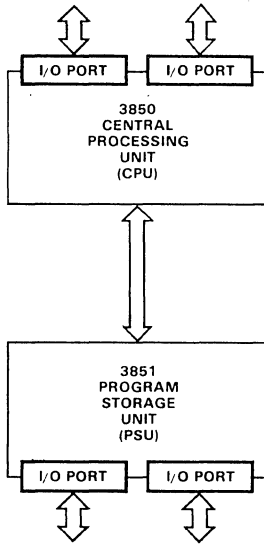
solving complex problems, the F8 devices can be connected as subsystems into a synergistic system of independent microprocessors.

By . . . incorporating the I/O structure on the chips so that the majority (95%) of the peripheral devices can be directly controlled without the need for special circuits. The trick is to accommodate the characteristics of a given peripheral device in the software. The I/O hardware structure includes a programmable timer, an efficient interrupt system and bidirectional I/O ports.

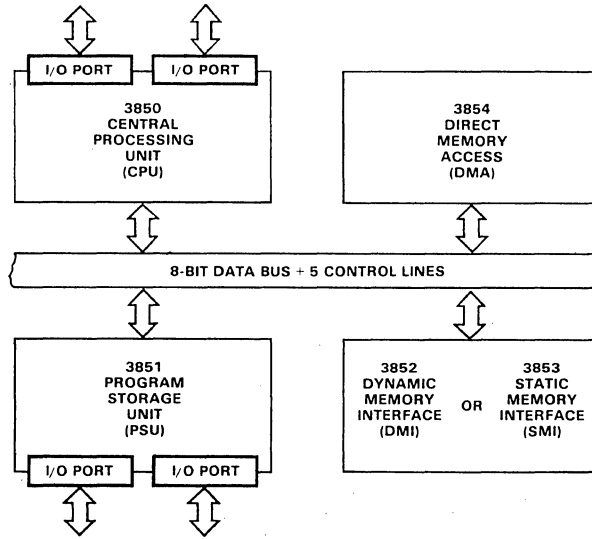
By . . . providing carefully thought out support software and hardware for generating and debugging microprograms.

WHAT IS THE RESULT ?

. . . a complete family of LSI circuits that can be used as building blocks to construct versatile, efficient, cost effective systems from the most simple to the highly complex.



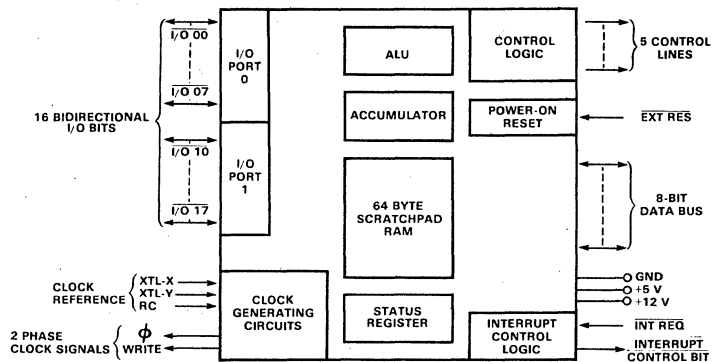
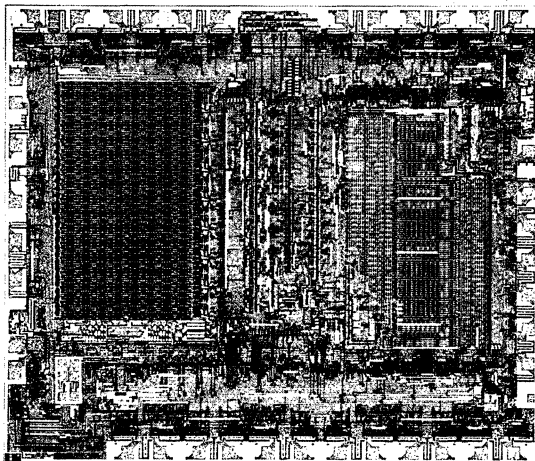
MINIMUM SYSTEM



F8 DEVICE FAMILY

MK 3850 CENTRAL PROCESSING UNIT

MOSTEK's F8 Central Processing Unit (CPU) contains all of the functions of an ordinary central processor and adds some time and money saving features uniquely its own. For instance, the 64 bytes of scratchpad RAM memory already included on the F8 CPU eliminate the need for external RAM circuits in many applications. Clock and power-on-reset circuitry, normally requiring additional integrated circuit packages, are included on-chip. MOSTEK's CPU also contains 16 bits of fully bidirectional input and output lines internally latched (for storing output data) and capable of driving a standard TTL load.



MK 3850 CPU BLOCK DIAGRAM

Mostek

MICROPROCESSOR

THE MOSTEK SURVIVAL KIT

The Mostek F8 Kit is comprised of the following parts: F8 CPU, Program Storage Unit (PSU), Static Memory Interface (SMI), 1K x 8 of random access memory, 2.00 MHz crystal, two CMOS buffers, and a 6.75" x 5.5" printed circuit board.

When assembled, the F8 Kit will form a basic F8 evaluation/development microcomputer with these features:

- 24 bits of I/O arranged in three 8 bit ports
- 1024 bits of Random Access Memory
- Full duplex TTY Interface (20 mA loop)
- Crystal control clock
- Automatic power on reset
- Hardware reset
- Non-volatile operating system in PSU firmware called designer development tool # 1 (DDT-1)

A user need only attach a 110 or 300 BAUD ASCII terminal (such as a teletype or CRT monitor system) and +5 and +12 V_{DC} power supply to begin operating the system. A user can then use DDT-1 to load, debug, and modify his own software in the 1K byte of RAM provided on the kit.

The operating system (DDT-1) provides the user with the following features that can be accessed from the ASCII terminal:

- Load command - used to load memory from paper tape
- Dump command - used to format data and output to paper tape punch
- Type command - used to examine blocks of memory

- Memory Display and Modify Command used to examine and modify memory one byte at a time
- Copy command - used to move blocks of memory from one location to another
- Port commands - used to display and modify the 24 I/O lines
- Hexadecimal arithmetic commands - used to perform Hexidecimal arithmetic
- Execute command - used to execute programs at a specific location
- Breakpoint command used in debugging users software

Using these DDT-1 features a user can immediately begin to write and execute his own software.

The F8 Kit comes with complete documentation including a detailed application note, programming guide, and a listing of the DDT-1 program.

The Mostek F8 Kit may be purchased in kit form (order MD 79001) or as an assembled tested unit (order MK 79002). A power supply box (order MK79003) that provides an edge card connector, all necessary power, switch selectable BAUD rate and a TTY cable is also available.

SOFTWARE AVAILABLE FOR THE F8

- Resident Assembler
- Resident Text Editor
- Fortran IV Cross Assembler
- Designer's Debugging Tool 1 (DDT-1) (included in the F8 Evaluation Kit)
- Designer's Debugging Tool 2 (DDT-2) (included with the Software Development Board)



THE EMULATOR FROM MOSTEK

The F8 PSU Emulator is a development aid for designing and field testing F8 microprocessor systems which utilize one or more MK 3851 program storage unit (PSU) chips. The Emulator is electrically equivalent to the PSU but is field programmable instead of mask programmable. This enables a user to obtain final hardware verification of all PSU programming prior to ordering custom PSU chips. Also, since the Emulator even "plugs in" like a PSU chip (via a male, 40 pin connector on the end of an "umbilical cord"), prototype systems can be converted to final production status by simply unplugging the Emulator(s) and plugging in the corresponding custom PSU(s).

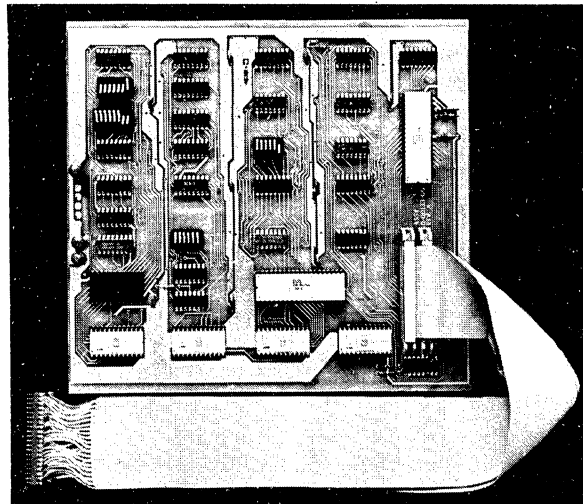
The MK 3851 itself, is a 40 pin integrated circuit that provides 1K bytes of ROM, two 8 bit latched I/O ports, a software programmable timer and interrupt circuitry for vectored addressing and priority control. Multiple MK 3851 PSU chips can be used in a single system, providing up to 128 bit I/O 64 timers, 64K of ROM, and 64 levels of interrupt.

The Emulator performs all the functions of the PSU:

- ROM
- INPUT/OUTPUT PORTS
- INTERRUPT VECTOR
- TIMER

The ROM section of the Emulator uses either four 256 x 8 bit ultraviolet eraseable PROMs or a single 1K x 8 bit ultraviolet eraseable PROM to provide non-volatile storage of the users' program. The PROM(s) should be programmed using a PROM programmer and then installed on the Emulator. The six ROM address select switches can then be used to establish the location of the PROM in the system memory map.

Input/output ports on the Emulator are implemented using an actual PSU. Six I/O port address assignment switches on the Emulator allow the user to



select the I/O port address desired for each Emulator. Also, since the PSU is available with three types of output driver circuits, the Emulator has three output options for the I/O ports:

- Standard current limited output
- Open drain outputs
- Pull-up driver outputs

While the Emulator is normally supplied with a PSU containing standard current limited output drivers, PSUs containing the other output options are also available for the Emulator.

Fifteen interrupt vector select switches on the Emulator allow the user to select the interrupt vector desired. Only fifteen switches are required because bit seven of the interrupt vector is set by the interrupt control logic. Bit seven is set to a logic zero if the timer interrupt is enabled and to a logic one if the external interrupt is enabled.

COMING SOON . . .

F8 ROM DEVELOPMENT BOARD (RDB)

The RDB is a sophisticated development aid for "in circuit" debugging of 3851 PSU firmware. The RDB is similar in function to the PSU emulator, with the exception that the 1K x 8 of program storage is located in RAM instead of in ultraviolet PROM. This permits the user to interactively monitor and debug his "PSU" software in the actual hardware configuration required for his application.

In normal use, the application hardware is breadboarded in the actual configuration for the final system, with empty sockets being substituted for each 3851 PSU chip to be used. RDBs are then connected to the system from the RDB interface cables to the corresponding PSU sockets. The RDBs are then inserted into a standard F8 development system which contains a single SDB for monitoring and controlling each of the RDBs.

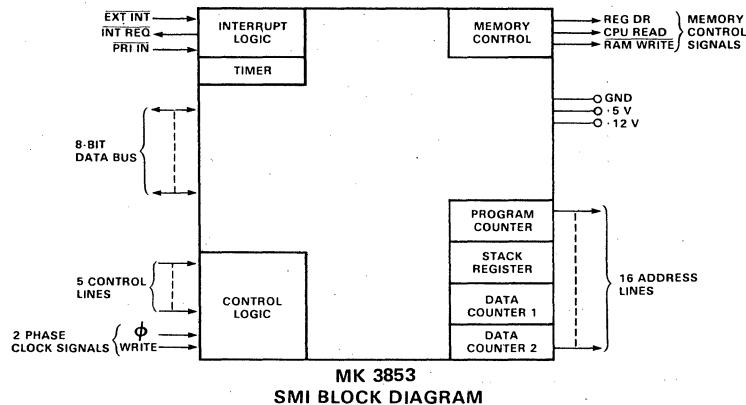
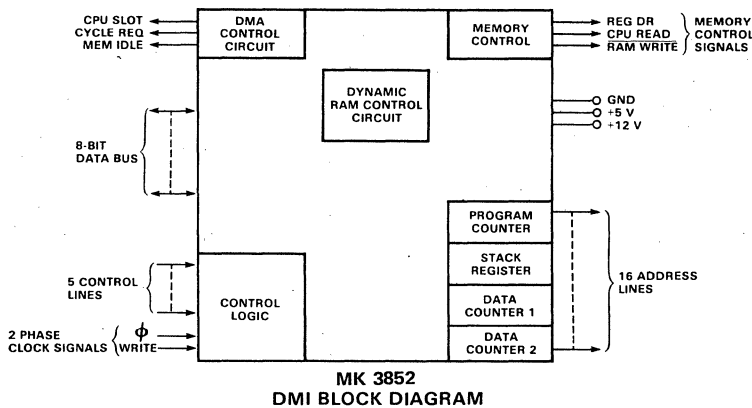
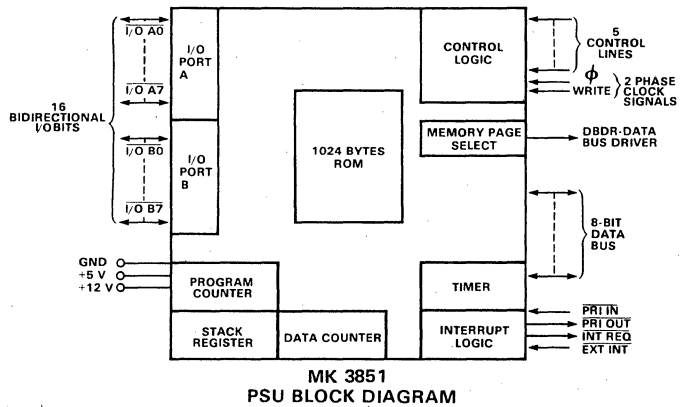
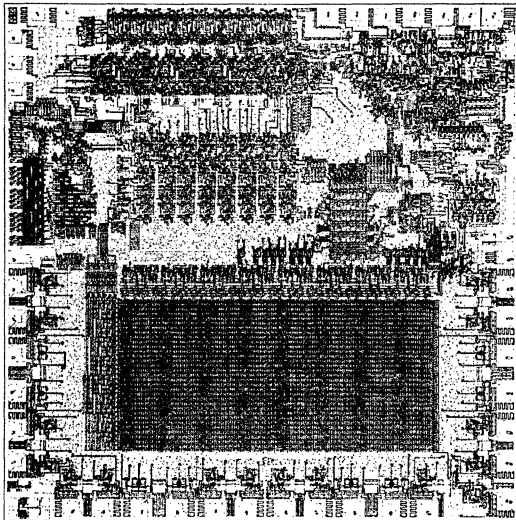
F8 SOFTWARE DEVELOPMENT BOARD (SDB)

The software Development Board is a complete F8 microprocessor system which has been designed to aid in developing and designing software for the F8. When combined with power supplies, card cage, and a TTY (or the equivalent), it will enable the user to develop the software for most types of F8 system applications. This not only includes the ability to execute and debug user software, but also the ability to create and edit "source" listings (using the resident text editor) and assemble them into corresponding "object" listings (using the resident assembler). Its other features include 8K x 8 of RAM (expandable with additional memory boards), a variable speed ASCII interface, and resident debugging and console routines (in two 3851 PSU's). Provisions have also been made for interfacing with additional peripherals, such as a high speed paper tape reader/punch.

MK 3851 PROGRAM STORAGE UNIT

It is important to note that MOSTEK's Program Storage Unit (PSU) is not just a conventional Read Only Memory. In addition to containing 1024 bytes of mask programmable ROM for program and constant storage, the F8 PSU includes the addressing logic for memory referencing, a Program Counter, an Indirect Address Register (the Data Counter) and a Stack Register. A complete vectored interrupt level, including an external interrupt line to alert the central processor, is provided. All of the logic necessary to request, acknowledge and reset the interrupt is on the F8 PSU. The 8-bit Programmable Timer is especially useful for generating real time delays. The PSU has an additional 16 bits of TTL compatible, bidirectional, fully latched I/O lines.

Systems requiring more program storage may be expanded by adding more PSU circuits. For example, one F8 CPU and three F8 PSUs will produce a microprocessor system complete with 64 bytes of RAM, 3072 bytes of ROM, 64 I/O bits, three interrupt levels, and three programmable timers. This complete system will require only four IC packages.



MK 3852/MK 3853 MEMORY INTERFACE

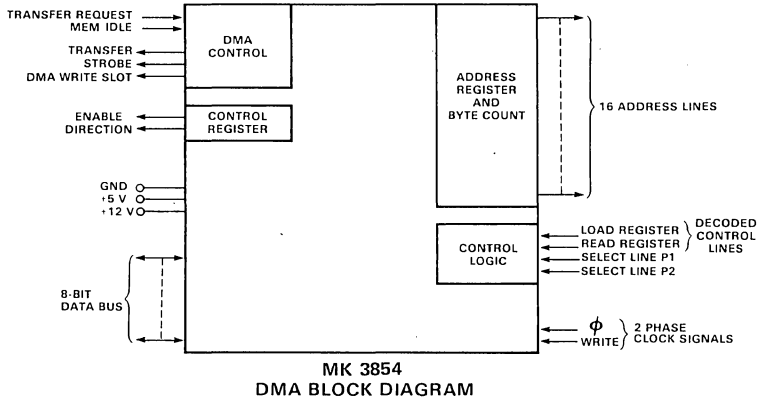
For applications requiring more than the 64 byte RAM located on the CPU, two memory interface circuits are included in the F8 set. Each device generates the 16 address lines and the signals necessary to interface with up to 65K bytes of RAM, PROM or ROM memory. Either device may be used in conjunction with standard static semiconductor memory devices.

The Static Memory Interface (SMI) contains a full level of interrupt capability and a programmable timer. The Dynamic Memory Interface (DMI) contains all of the logic necessary to refresh MOS dynamic memories without degrading the system throughput time. The F8 DMI can also interface with static memories when desired.

Mostek

MICROPROCESSOR

MK 3854 DIRECT MEMORY ACCESS



MOSTEK's Direct Memory Access (DMA) device sets up a high speed data path to link F8 memory with peripheral electronics. The F8 DMA circuit, when working in conjunction with the F8 DMI, does not require overhead electronics to keep track of memory addresses, bytes transferred and handshaking signals. The data transfer is initiated by the CPU under program control. Once started, the DMA transfer will continue without CPU intervention. The CPU can sense the enable line of the DMA to determine the completion of a transfer. The entire DMA transfer will take place without halting the central processor.

F8 MICROPROCESSOR SYSTEMS A TWO-CIRCUIT SYSTEM

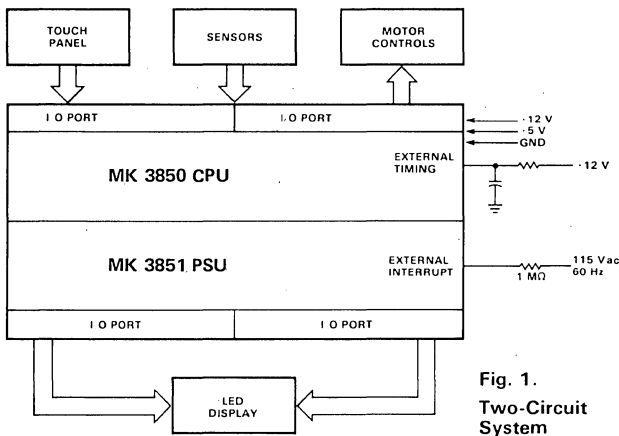


Fig. 1. Two-Circuit System

The two-circuit F8 microprocessor is suitable for small data terminals, controllers, and specialty calculators. The keyboard is connected directly to the F8 I/O ports without special interfaces. Switch-bounce protection, rollover, and key encoding are all under software control. Software also decodes signals for LED readouts.

As an appliance controller, for example, the two-circuit system can perform all input-output sensing, actuating, timing, and computation operations. A system like the combination washing-machine-and-dryer controller in *Figure 1* requires more than 250 components when other microprocessor device sets are used, but with the F8 devices uses only 55 components, including 28 LEDs and the power semiconductor devices and relays used to control the motors. A set of custom circuits would also require about 50 parts, but initial engineering expense is heavy and severe penalties are incurred if changes are required. With the F8 system changes can be made by merely changing the program.

A MORE COMPLEX SYSTEM

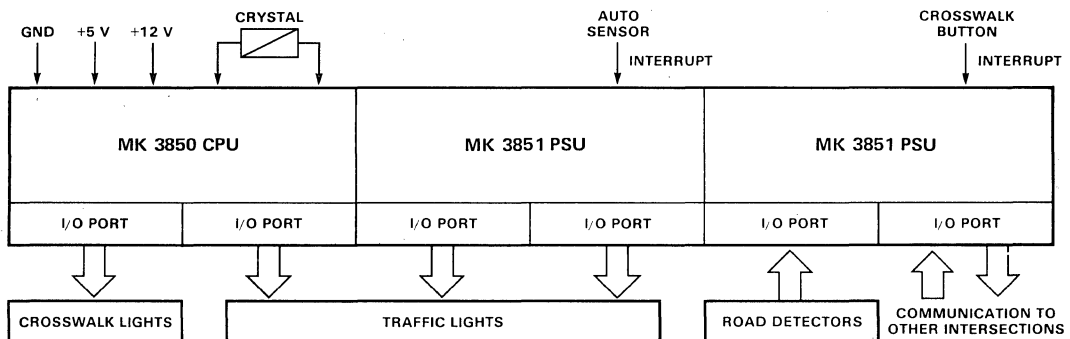
The versatility of the F8 system is indicated by the traffic-light-controls system in *Figure 2*. The use of one CPU and two PSU circuits provides the designer with two timers, two interrupts, an onboard clock, onboard power-on reset, onboard switch decoding, and 48 bidirectional I/O bits. This system could be tied to vehicle detectors in the road, to monitor traffic for left-turn lanes as well as through-traffic flow in four directions. It would also react to interrupts from the pedestrian control buttons at each corner. There also is sufficient I/O capability to permit communication with and control of neighboring intersections and to allow the system to be operated manually or tested for proper operation.

Five F8 features are of particular interest for this type of application. One of the interrupts can eliminate the need for

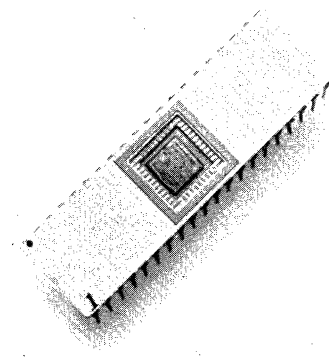
such external circuits as a comparator to compare a count of the cars with a predetermined value to cause the light to change. (The CPU can handle the simple arithmetic of counting cars.) This interrupt also eliminates the need for continuous polling of traffic count by the microcomputer. The second interrupt would be ideal for permitting pedestrian control to override the automatic system. The internal clock, with an external crystal, can also control light routines.

The two timers permit simultaneous counting of delay for vehicle signals and flashing warning lights for pedestrians. The onboard power-on reset acts in case of power failure to start the system automatically when power is renewed. The bidirectional I/Os have built-in latches that eliminate the need for external latches for the job of "holding" commands for lights as well as the momentary commands provided by timers and sensors.

Fig. 2. Medium Complexity System



PACE... THE FIRST SINGLE CHIP 16-BIT MICROPROCESSOR



National Semiconductor believes a new four-letter word is about to change the way you do things.

That word is PACE™; an acronym... a short way to say Processing And Control Element.

And the things PACE will help you do are things like... replacing complex, hard-wired-device systems for sequential logic operations... replacing all but very-high-speed minicomputers in even larger, more complex systems... replacing most other forms of programmable controllers. And PACE does these in applications such as small business

machines, cash registers, terminals, peripheral devices, traffic controllers, instrumentation, process and numerical control equipments, machine tools. You name it, and PACE will do it for you.

And PACE does it for you with fewer circuit boards and connectors, with smaller power supplies and cooling systems, with a reduced inventory, with a shorter design time and lower assembly and test costs, than has ever been possible with any other, comparable-power microprocessor.

For that is what PACE is—a microprocessor. But it's not just another microprocessor. No indeed. That's not the way National does things. Instead, PACE sets the pace as the industry's first single-monolithic-chip, 16-bit microprocessor.

On its single chip, PACE contains control logic, four working registers (accumulators), a ten-word stack and interrupt control circuitry. All you add are a single-phase true and complement clock driver, buffering system memory, and PACE is ready to go to work. All of these supporting elements are standard parts in the PACE product family.

And, if you change your mind about what you want your system to do, you can reconfigure a PACE-controlled system with software alone.

PACE... PLUS A COMPLETE FAMILY OF CHIPS

A standard, hermetic, 40-pin ceramic DIP houses the PACE single-chip CPU. It looks like any other LSI semiconductor component.

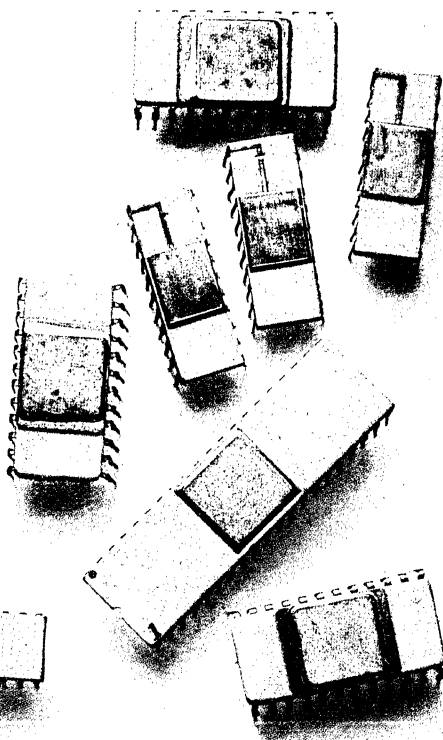
But the successful application of a microprocessor requires considerably more support than does any other semiconductor component. Proper support makes all the difference between the successful, short-term application of a microprocessor and a long-term series of frustrating and time consuming problems.

Thus we support our microprocessor products in a number of ways, one of which is an extensive array of software and hardware products. And most such PACE-oriented products are shared with our very compatible IMP-16 microprocessor family, for PACE is an extension of the IMP-16—albeit a highly sophisticated one. You may view PACE as a monolithic integration not only of the five IMP-16 MOS/LSI chips, but of the IMP-16's TTL-implemented functions as well.

In other words, you save money in design time, software and hardware with PACE because we have implemented everything on one chip—status and control circuitry, sense circuitry for conditional branches, interrupt logic and even the multiphase portion of the clock generation circuitry.

Even with presently available off-the-shelf components, you need only a dozen packages to implement a complete PACE microprocessor system—and we mean one with 16,384 bits of read-only program storage and a 16-bit TTL data bus interface.

But with our PACE-optimized support and memory products, you



can implement the same system even more simply, minimizing the system package count and greatly simplifying all system interfaces while providing a true-TTL, Tri-State® system data bus.

PACE Blue Chips These support the CPU, and include a System Timing Element (IPC-16A/502), an eight-bit Bidirectional Transceiver Element (IPC-16A/501) and a 16-bit Address Latch Element (IPC-16A/518).

The single-package clock and an external crystal provide complete system timing, eliminating all other discrete, passive components, while two bidirectional transceivers provide a complete, 16-bit TTL system address and bidirectional data bus. In a driver-only mode, a third bidirectional transceiver package may be used as the control bus buffer, generating seven TTL control signals and flags for distribution.

PACE Green Chips These peripheral interface chips, called Interface Latch Elements, provide storage and buffering between the PACE TTL system bus and user peripherals. They are available in eight-bit increments, as the ILE-8 (IPC-16A/503), and 16-bit increments, as the ILE-16 (IPC-16A/513), to accommodate PACE's unique ability to operate on both eight- and 16-bit data elements under software control.

PACE Memory Elements These too are specially designed for optimal use in PACE-based systems, and include: a 256x4 RAM (IPC-16A/504), which eliminates any need for address latches between PACE and the read/write memory (the chip includes address latches and latched chip enables); a 1024x16 ROM (IPC-16A/505), which alone provides sufficient control storage capacity for many applications, and which also includes on-chip address latches; and a 512x8 PROM (IPC-16A/506) that, in prototyping and preproduction use, does require a supplementary address latch such as our 16-bit Blue Chip Address Latch Element.

With such support and memory devices you can implement that twelve-package, 16,384-bit system mentioned above with fewer than eight packages. When you compare this number to the 30 and more packages needed for most previously available microprocessors, you'll see why PACE lets you implement your system far more easily than you ever thought possible.

PACE... A FULL FEATURE CPU

PACE is a true 16-bit central processor unit: it makes use of 16-bit instruction words and 16-bit data words, and features a powerful, efficient and flexible set of 45 instructions.

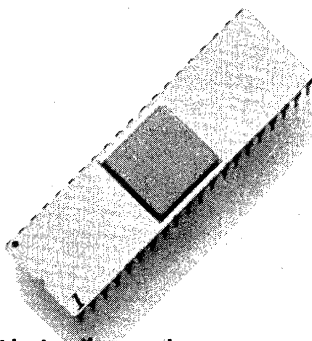
PACE operates with either eight- or 16-bit data words Only PACE lets you specify—via your program—either eight- or 16-bit operation.

In general, the ability of PACE to operate with 16-bit instruction words on both eight- and 16-bit data words brings significant benefits to your system. It means that PACE is highly

efficient in the handling of both eight- and 16-bit interfaces within the same microprocessor-based system. And even in systems dominated by eight-bit data element interfaces, PACE remains extremely cost effective.

In particular, PACE's 16-bit instruction words greatly increase the power of its instructions beyond those of eight-bit processors. Further, the full 16-bit PACE-generated addresses increase both efficiency and throughput over those of conventional eight-bit CPUs. This results from PACE's reduction in program memory overhead, and its elimination of multiple-precision operations generally required for eight-bit data elements.

In other words, while PACE is a true 16-bit processor, it extends the coding and address generation efficiencies found only in 16-bit microprocessors to eight-bit systems as well, and eliminates complex hardware interfaces and bookkeeping overhead in systems that require both eight-bit and 16-bit interfaces.



16-bit instruction word

8- or 16-bit data words

45 instructions

Common memory and peripheral addressing

Shares instructions with National's IMP-16

Four general purpose accumulators

Ten-word stack

Six vectored priority-interrupt levels

Programmer-accessible status register

Typical 10- μ s instruction execution

Can use 1k-by-16 ROM

Single-phase true and complement clock

+5V, -12V

Addressing flexibility, speed

Wide application

Efficient programming

Powerful I/O instructions

Allows software compatibility

Reduces memory data transfers

Interrupt processing/data storage

Simplifies interrupt service and hardware

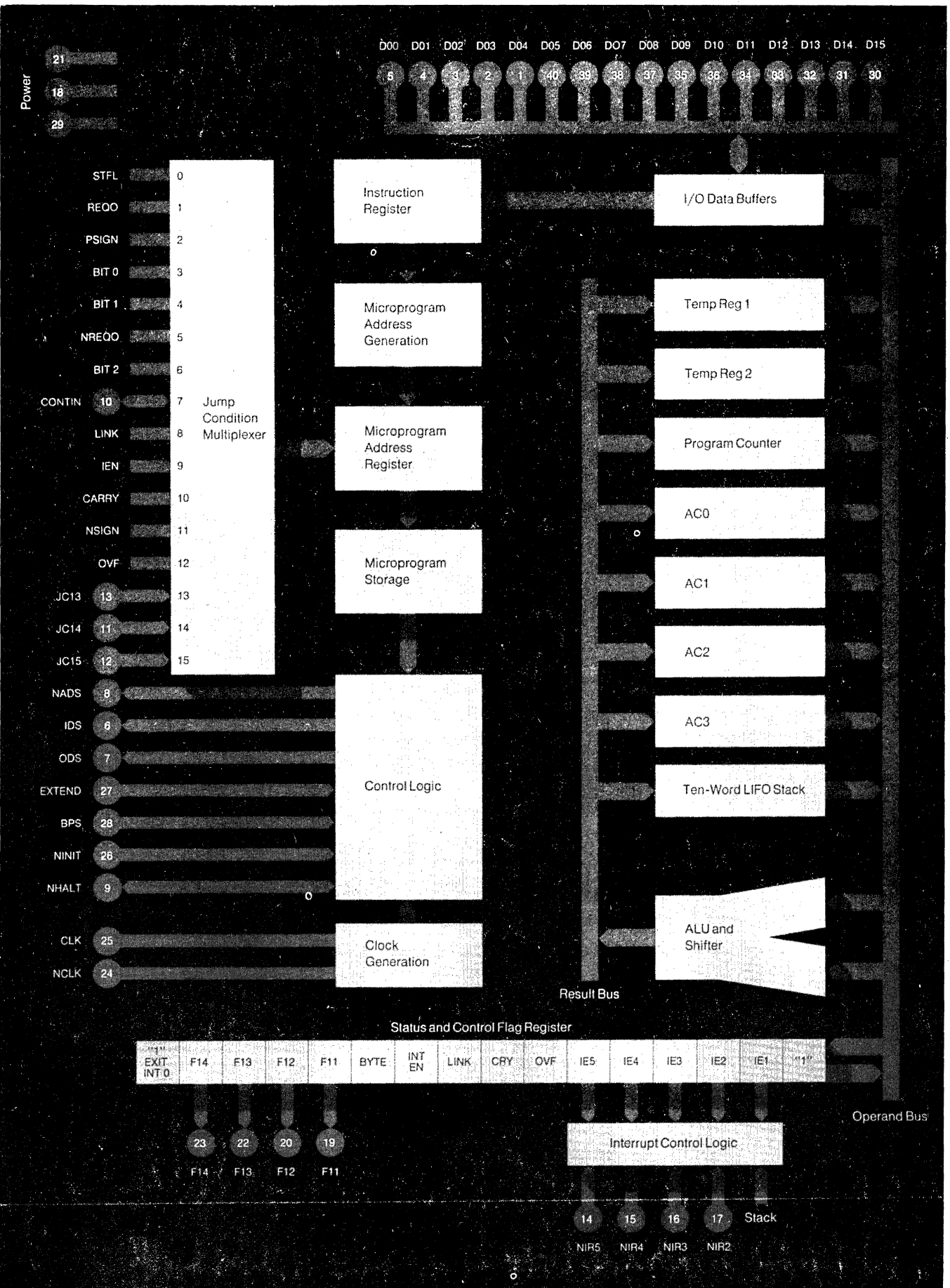
May be preserved, tested, or modified

High speed

Single memory package

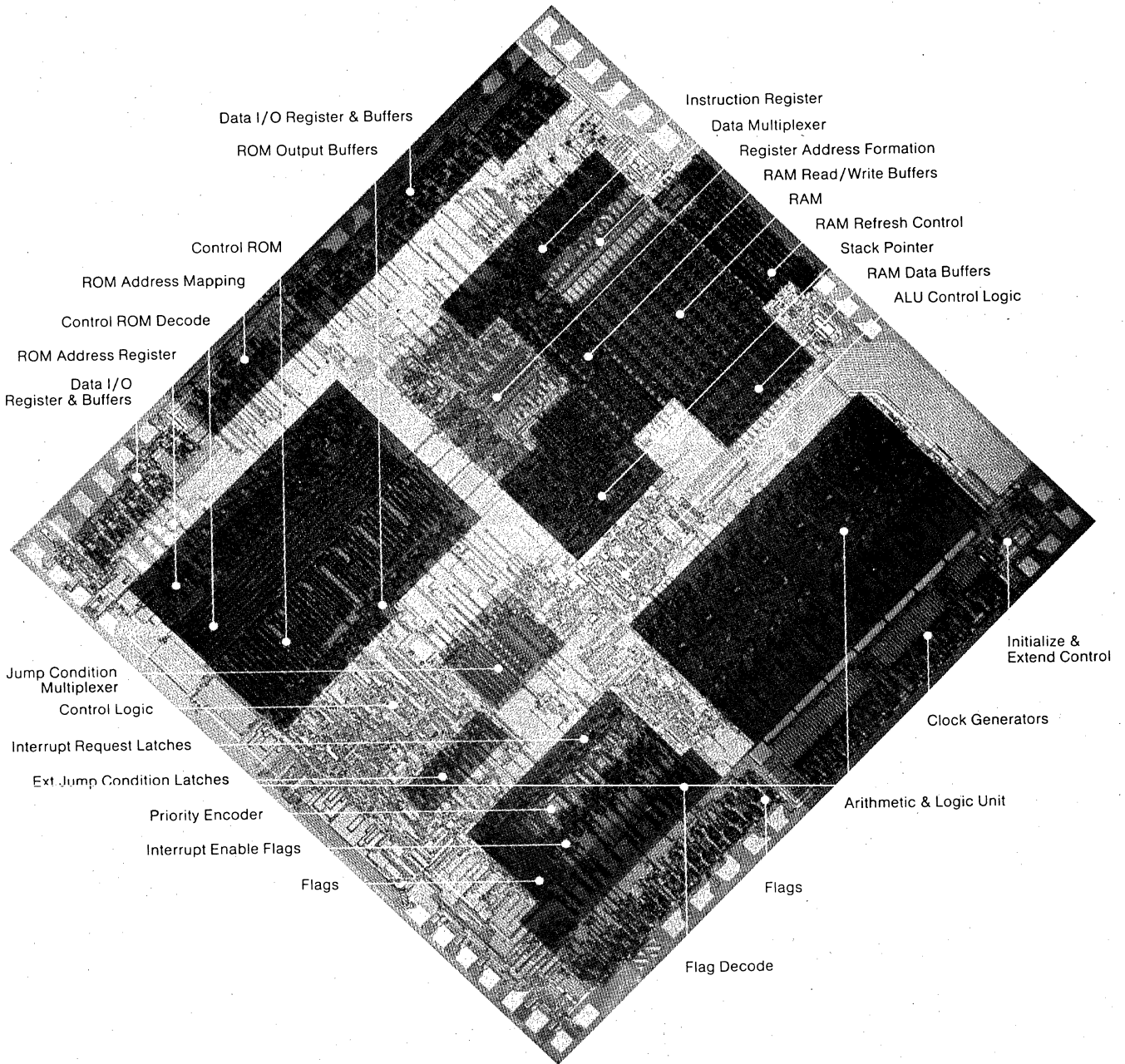
Minimum external components

Standard supplies



National Semiconductor

MICROPROCESSOR



PACE increases throughput, reduces memory overhead PACE has a number of resources that decrease system program and read/write storage needs, and increase throughput. Principal among these are its four, general-purpose 16-bit working registers and a ten-word (16-bit) last-in-first-out (LIFO) stack.

While PACE actually provides seven data registers, its design makes four of them available directly to the programmer, as accumulators. These reduce the number of memory load and store operations associated with saving temporary and intermediate results in system memory. And this means that your system shows increased throughput and a reduction in its program and data storage needs.

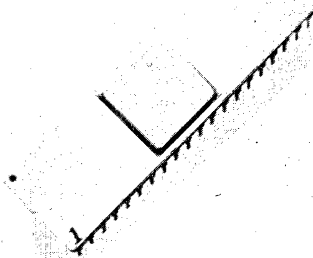
PACE's LIFO stack provides even more storage—up to ten 16-bit words more. You may use the LIFO stack to store program-counter contents or to store status information. In some applications (device controllers, for example) this ten-word stack, together with the on-chip registers, eliminate any need for off-chip read/write memory.

The point is that the LIFO stack further reduces program and read/write system storage overhead, while inherently reducing interrupt-response time (because it saves return addresses during interrupt servicing and subroutine execution). Again, memory overhead is reduced and throughput is increased.

PACE eliminates interrupt hardware

The PACE microprocessor gives you an on-chip, six level, vectored, priority-interrupt structure. This eliminates any need for external, off-chip interrupt hardware. And it gives you automatic interrupt identification, too, which again eliminates program storage overhead and saves time—the time that other processors usually require to poll peripherals in order to identify the interrupting device.

And if your system involves more than six interrupts, PACE lets you place more than one peripheral on a priority level by means of a simple, open-collector connection to the appropriate priority interrupt request line.



PACE provides quick access to system status information

A single, 16-bit status flag register provides all status and control bits for PACE. And because the contents of this register may be loaded from or into any accumulator, or the stack, you can conveniently test, modify or store status information.

Four of PACE's flags are made accessible so that you may assign specific, programmed functions to them. These flags drive output pins, through which you may directly control system functions or set software status indicators.

Note that the ability to provide status output directly, via the four control

flag outputs, requires no external hardware and lets you generate—through software—appropriate control signals.

Additionally, PACE provides convenient status sense capability with four, external, user-assigned sense inputs and twelve, internal, status sense conditions. These sixteen conditions are individually testable by a conditional branch instruction in software.

So PACE saves you hardware and program overhead as well as the throughput usually associated with the implementation, on the system data bus, of such control-flag output functions.

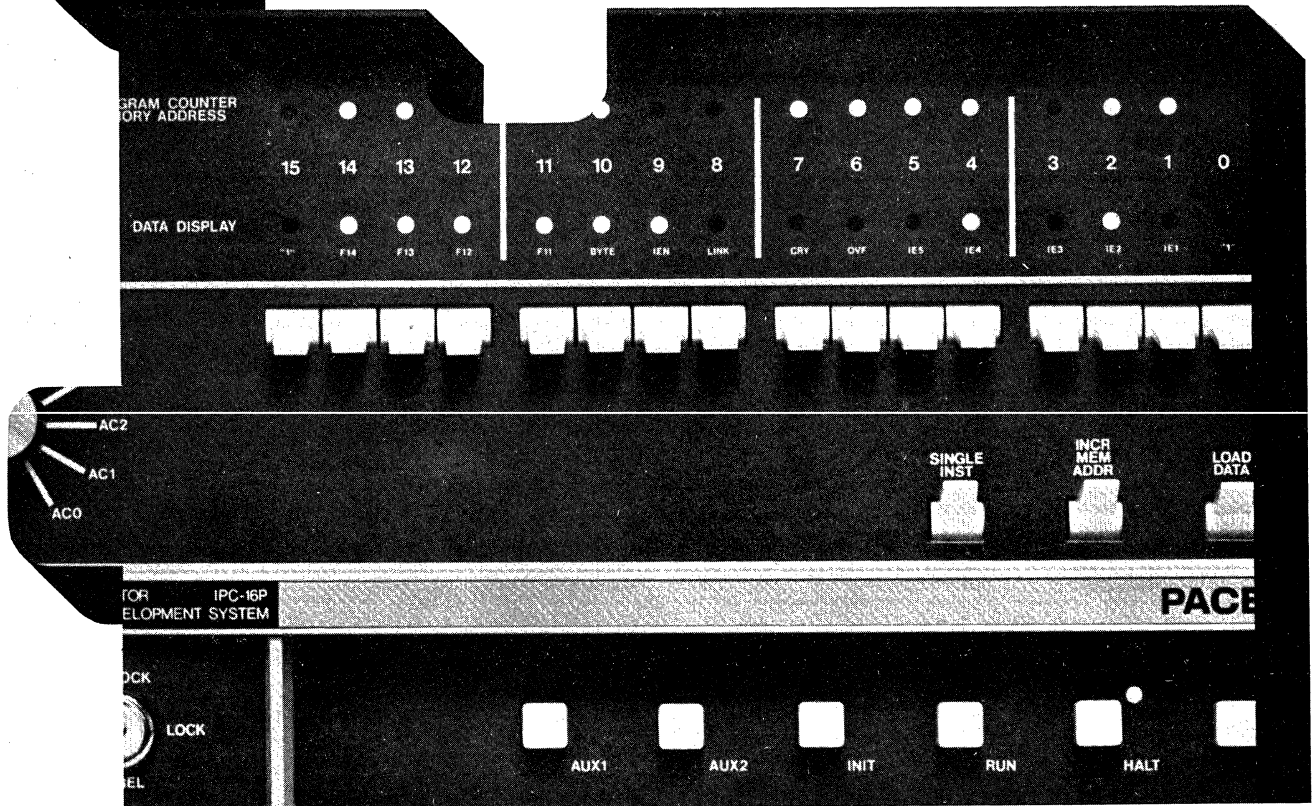
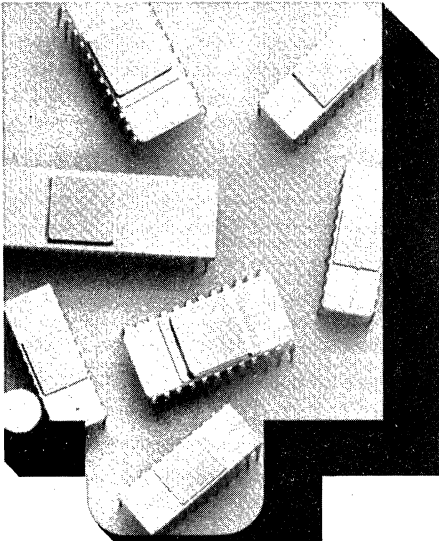
In brief, PACE's status sense inputs, interrupt request inputs and status register are structured to provide fast response to system status, and do so without any complicated algorithms or critical timing considerations.

With our PACE Development System not only can you completely evaluate the microprocessor itself, but you can actually develop a variety of OEM equipment, software and full-scale processing systems: it's a powerful tool indeed.

Now, even though PACE is basically a single component, we've developed a variety of application hardware for it. This hardware lets you perform rapid product evaluations, or you may choose to use it in preproduction systems. All of the hardware is on standard, 4.5-inch-square PC cards. These cards are compatible with the extensive line of breadboarding and interfacing cards and card hardware from Augat and a number of other sources.

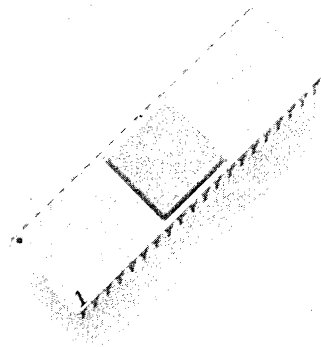
Standard PACE application hardware includes: a CPU card (IPC-16C/100), which holds a PACE CPU package,

a System Timing Element and crystal oscillator, and Bidirectional Transceiver Elements; a 1024x16 RAM card (IPC-16C/001) with on-chip address latches, and on-card cycle-extend circuitry that simplifies interfacing with the CPU card and permits the use of low-performance, low cost memory in PACE-based systems; a PROM/ROM card (IPC-16C/002P) with provision for 2048x16 storage; and a general purpose I/O card (IPC-16C/800) with four, eight-bit increments of the Interface Latch Element for connection to peripheral devices.



NATIONAL BACKS YOU UP

Along with PACE—the CPU itself—comes an immense array of backup support: hardware; software; advisory and maintenance services; and a range of components unmatched elsewhere in the industry, and yet so necessary to implement every part of a full system. Let's take it from the top.



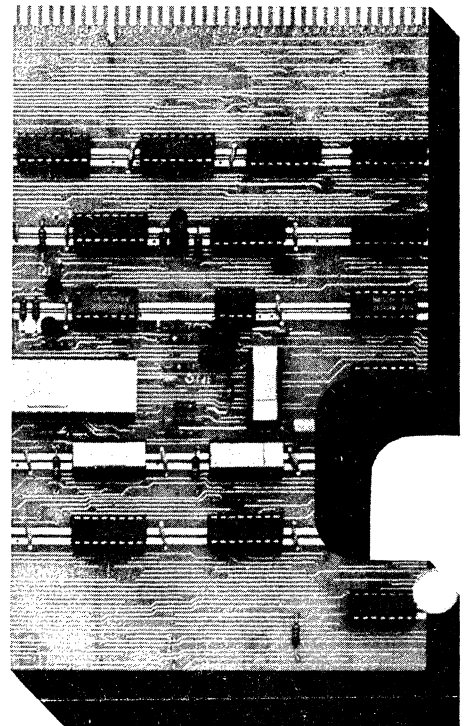
Hardware Support First off, we offer a complete PACE Development System, which makes use of an 8.5x11 inch Development CPU printed-circuit card.

This system gives you a way to develop and debug application hardware, and application software as well. Its control panel lets you examine or change the contents of the LIFO stack, of any register and of any memory location. And this same panel lets you execute one instruction at a time—and perform bootstrap loading operations as well—which is a very efficient way to develop a program. (Try program development on a microprocessor de-

velopment system without a control-panel interrupt feature and you'll see what we mean.)

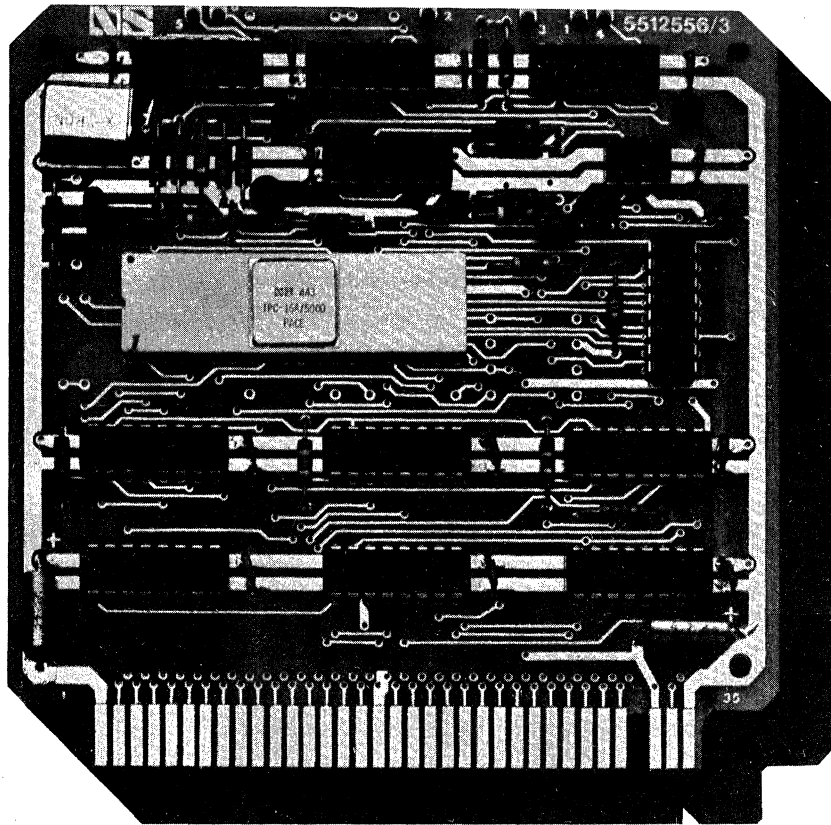
Although it provides for teletypewriter-like terminals, the PACE Development System also provides interfaces to a card reader, a line printer, a tape reader and a dual drive floppy disc—very important for high-speed input and output of data. Using such peripherals instead of a TTY can significantly reduce your program development time.

We even offer a PROM programming capability for the PACE Development System. And this means that you can complete all phases of a program development without any outside services and without buying any additional equipment.



National Semiconductor

MICROPROCESSOR



The size of PACE hardware cards assures that you'll have no trouble using them in physically-small equipments.

Software Support A wide variety of software is available, which directs your PACE-controlled system to do exactly what you want it to do when you want it to do so.

PACE resident software includes Assemblers, a Source Statement Editor, a DEBUG routine, Loaders, Utility (e.g., Teletypewriter) routines and Diagnostics (memory and CPU).

And, of course, because of the high degree of compatibility between PACE and our IMP-16 microprocessor family, PACE users have access to what is perhaps the most flexible and powerful array of software currently

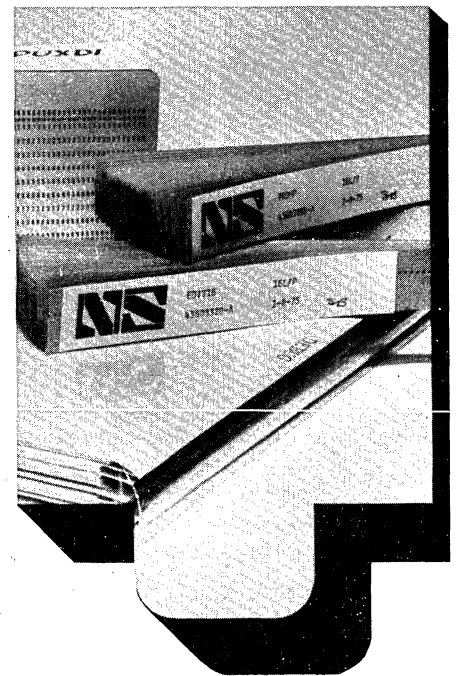
available. For example, current IMP-16 users can use that microprocessor's Source Statement Translator to make their IMP-16 software usable with PACE without incurring additional development costs.

Documentation National provides extensive documentation to support your microprocessor-based system design. Such documentation must serve a number of functions, and PACE documentation covers them all from start to finish. The PACE Product Description, for example, helps you determine the suitability of a microprocessor to the application in question. With suitability established, you use the PACE Technical Description to establish benchmarks and prepare your preliminary system design; this manual also aids you in the development of application programs and the detailed system implementation, including interfaces.

Finally, our PACE User's Manual helps you to debug the application programs and hardware interfaces, and to prepare your system's own hardware and software documentation.

Field Support Our Area System Specialists are engineers specially-trained in microprocessor systems. They fully understand the products—hardware and software—and their applications, and are at your service in numerous locations both domestically and internationally. Besides offering on-site assistance, many of these specialists have operating microprocessor systems in their offices for hands-on explanations and aid.

Back-up Applications Support At National's home base we have an experienced microprocessor applications group. While this group's main



mission is to support you technically through your local Area System Specialist, the group's members can help you directly, as well. All it takes is a letter or a telephone call to them in Santa Clara, California.

Factory Service We can and will repair anything that goes wrong with any National microprocessor product (things sometimes do go wrong; you know it, and we know it too). And this repair service is not only for the OEM user, but for his customer—the end user—as well.

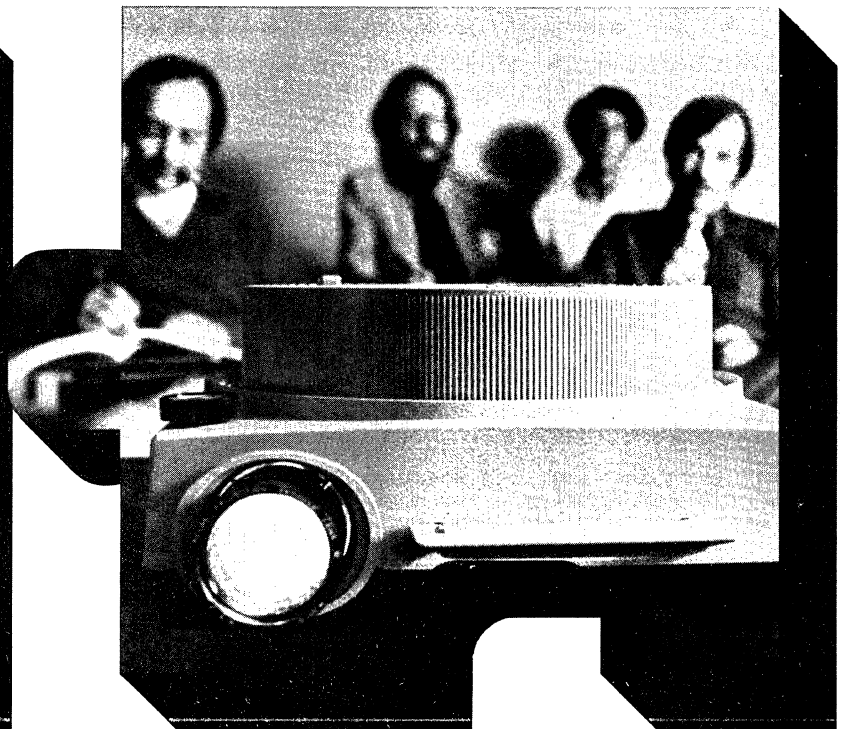
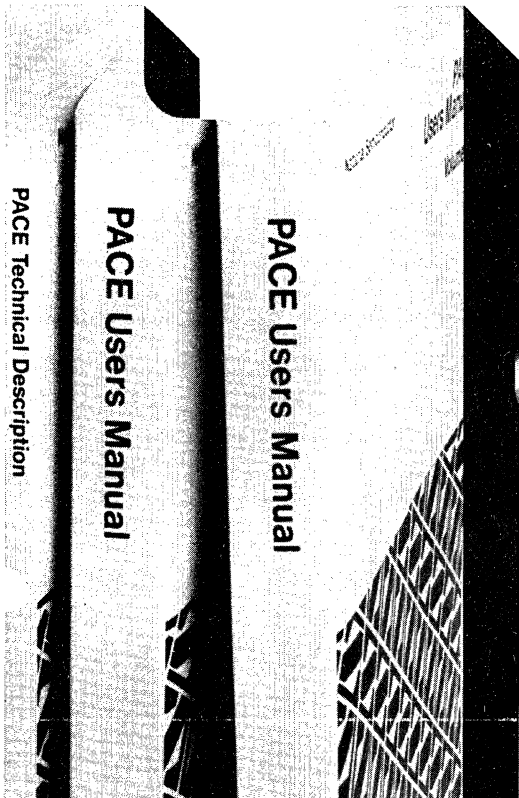
Training We offer complete, from-the-ground-up training courses. These customer workshops are not quickies; they are in-depth, 20-day courses of hands-on instruction divided into four sequential sessions of five days each, which take the student from the basics microprocessors right on up to the development of custom instruction sets through microprogramming.

Users Group The Users Group is an informal organization, with membership open to microprocessor users and those interested in the subject. It is a vehicle of communications between and among National and the group's members.

Our primary support of this group is in the form of a newsletter, which contains just about anything of interest to the group's members as it pertains to National microprocessors—articles, hints and kinks, editorials, letters from members, National announcements of all sorts (pertaining to microprocessors), even classified ads where you may advertise for sale anything you've got that's related to microprocessors.

If members in a given area set up local meetings, these are announced in the newsletter. There is also a Users Group Software Library, from which programs submitted by members are available to other members for the cost of reproduction only.

We want it clearly understood that National's unique working relationship with its customers—whether OEM or end user—helps us understand your problems. And we can help solve them. When you buy a microprocessor from National, you buy more than a chip and a data sheet.



National Semiconductor

MICROPROCESSOR

EVERYTHING YOU NEED... FROM NATIONAL

While a microprocessor capable of being easily and inexpensively tailored to new applications is one key to a fast, cost-effective solution to a problem, it is not the only one needed. The second key, just as important as the first, is a broadly-based supplier with expertise in design, production and application of microprocessors, interface elements, input sensors and all other system components.

National Semiconductor makes everything you'll need.

We make memories.

We make clocks and support logic.

We make bus interface elements.

We make multiplexers.

We make A/D and D/A converters.

We make keyboard encoders.

We make positive and negative regulators.

We make line drivers and receivers.

We make display drivers.

We make optoelectronic display devices.

We even make transducers.

We make everything you'll need. And we can help you with everything you'll use. Only National Semiconductor places such an extremely broad-based expertise at your service. When you start your next system design, we're ready to help.

An Industry Leader When you do business with National Semiconductor Corporation, you do business with an acknowledged leader in the semiconductor industry—one of the four largest semiconductor manufacturers in the United States.

National Semiconductor is also a worldwide corporation. We are multinational in our manufacturing operations, and in our marketing and distribution as well. And what does this mean to you? Just this: that wherever your products are manufactured or used...wherever you use our products...wherever you are in the world...National is near at hand to help you.

**There's More to Microprocessing
Than a Microprocessor.**

SC/MP

**Easy to use
sophistication
at the right
price—
from National,
of course**

If you design controls or control-related equipment and systems... if you use mechanical logic or hard-wired, discrete, semiconductor logic arrays... if you avoid the use of sophisticated electronics because it is either too powerful or too expensive for your applications...

...we have something new and very interesting for you.

And while this something new and very interesting is *internally* sophisticated, *externally*—that is, from *your* point of view—we've designed it to be easy to use, to be economical to use and to be powerful without invoking the brute force of overkill.

We're talking about a micro-processor, of course... but a very special one unlike any other available in the marketplace.

We call it SC/MP—a simple-to-use, cost-effective microprocessor.

SC/MP is the first microprocessor designed to fit the immense variety of applications in which 4-bit microprocessors are too difficult to use and for which currently-available 8-bit microprocessors are too powerful and expensive—applications that involve low-speed man/machine

interfaces in the industrial/commercial and consumer marketplaces.

In the industrial/commercial arena, for example, SC/MP fills the bill for electronic cash registers... traffic light controllers... elevator controllers... automatic, computing-type price/weight scales... food processing machinery... lumber and paper mill process controllers... measurement and instrument controllers... word processors.

On the consumer front, SC/MP is ideal for sophisticated calculators... electronic games... appliance controls... home air conditioning, heating and security systems... automatic tuners for TV receivers and mobile communication systems.

So get rid of your springs, levers, gears, switches, relays and discrete logic arrays by using SC/MP: a new concept in microprocessor control systems, which offers you a unique path to simpler, more economical and more efficient designs—a path not possible with any other microprocessor that you can buy today.

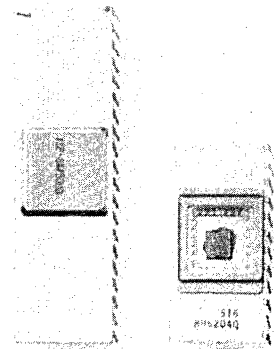
Wherever traditional microprocessors represent overkill... wherever economy is more important than the utmost in high-powered performance... SC/MP gives you exactly what you need to compete in today's markets—sophisticated yet easy-to-use electronic controls for your products at the right price, and cost-effective designs for customer satisfaction.

**Simple
implementation
of complex
control functions**

Pull together a power supply, a timing capacitor and a read-only memory (ROM). Connect these to a SC/MP CPU chip and... you've got a control system with three serial-data input ports and four serial-data output ports, commanded by a powerful set of 46 instructions.

We've just described a first-level, CMOS-compatible, SC/MP-based system, which may consist of as few as two integrated circuit packages: the SC/MP CPU chip and a standard ROM (or PROM) memory. Yet even with such a simple system you can implement the control logic for electronic games... traffic signals... simple industrial systems... appliances... vending machines... simple terminals.

With SC/MP, you move up to a higher level of operational capability by adding, to the first-level system, three more packages: a hex D flip-flop; an 8-channel digital multiplexer; and a 1-to-8 demultiplexer. These packages increase the number of serial-data input and output ports to eight each, and yield a system with four general-purpose, latched, control flags, a system that can address 4096 bytes of memory.



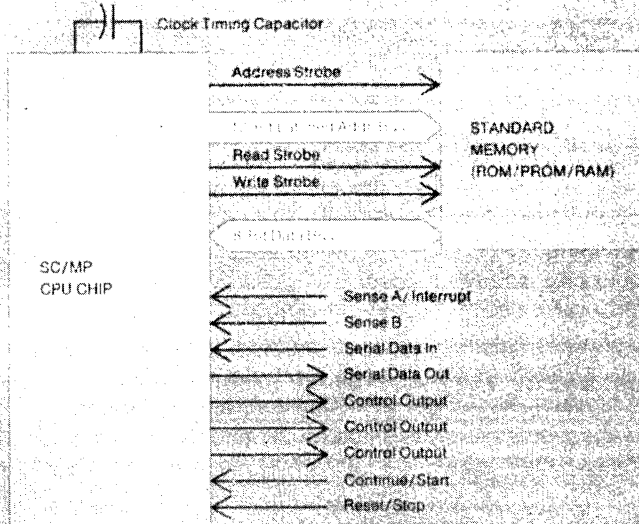
And with this second-level SC/MP system, you can implement direct digital controllers with up to eight process loops... on-board automotive computers... instrument controllers... complex traffic intersection controllers... electronic cash registers.

Finally, by adding to the SC/MP CPU chip our Interface Latch Elements, and some buffering, you move up to a very sophisticated system with high-speed, parallel data transfers—one that can address up to 65k bytes of memory to perform complex control functions as in credit card verification... business and accounting machines... text-editing typewriters... intelligent, stand-alone terminals... complex instrument/ measurement systems. But all still very easy to implement and use.

SC/MP systems are easy to use and externally uncomplicated because we've moved most of the needed logic into the very heart of the system—the SC/MP CPU chip itself. And the internal elements—the CPU features—come to life under software control to provide your SC/MP system with architectural characteristics such as...

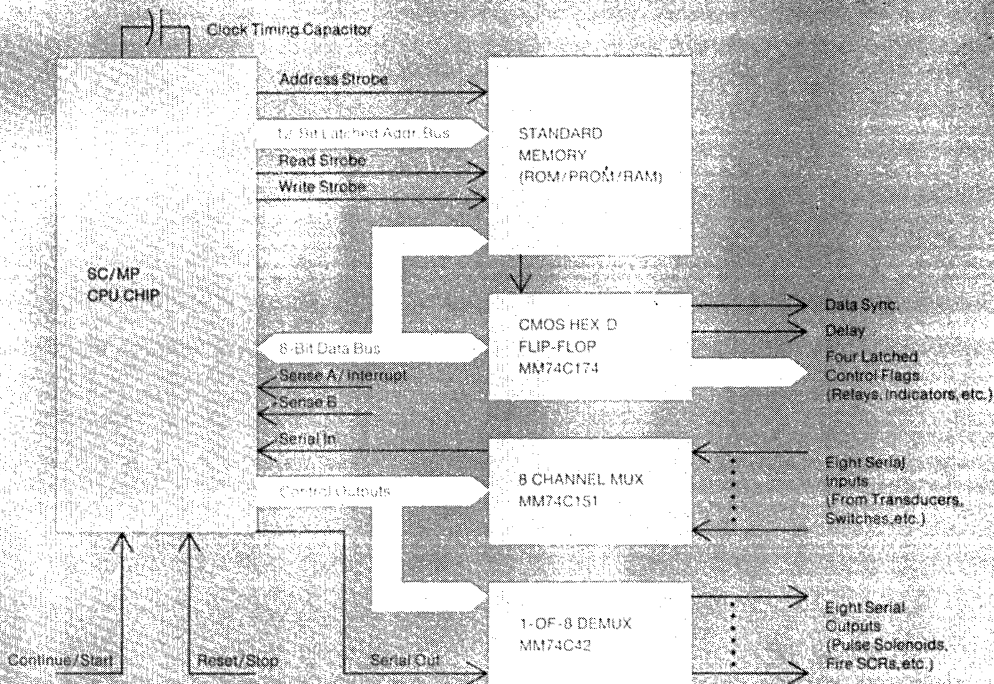
Simpler interfacing	Static operation; Bidirectional, Tri-State® 8-bit data bus, TTL or CMOS compatible options; Simple, yet powerful, interrupt function
Easy program development and debug	Fully supported by prototyping hardware and software;
Simpler I/O hardware	Separate serial-data input and output ports; Two sense inputs; Direct interfacing to standard memory parts; Direct interfacing to CMOS logic and memory
Direct condition testing	On-chip generation of asynchronous control signals for direct interfacing and a capability to use memories of any speed
Direct Memory Access (DMA) and multiprocessor capabilities	Separate bus access control
Direct control output	Three user-accessible control flag outputs
Simplified programming	Multiple addressing modes—program counter relative, pointer relative, immediate data and auto-index
Upward expandability	Address capability to 65k bytes of memory
High performance	2 μ s/microcycle instruction execution speed
Simplified multi-processor network design	On-chip multiprocessor network bus-allocation logic: Enable In, Enable Out, Bus Request

First-level SC/MP system



Electronic games
Simple traffic controllers
Appliance controls
Vending machine controllers
Simple terminals

Second-level SC/MP system



Direct multiloop digital controllers
On-board automotive computers
Instrument controllers
Complex traffic controllers
Electronic cash registers

We've provided SC/MP with an interrupt system that, though easy to use, is quite powerful: the interrupt entry-point is completely controlled by software, as is the Enable/Disable function. Your ability to modify this interrupt linkage means that in many types of applications—as in the control of a system based on the counting of events, for example—you can program SC/MP to save software overhead.

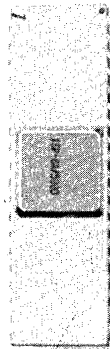
And speaking of savings, SC/MP lets you address peripherals in the same manner as memory. Thus, powerful memory-reference instructions (and addressing modes) may be used for peripheral data I/O as well. And SC/MP's straightforward "handshake" I/O allows simple interfacing in DMA and multiprocessor applications. The DMA feature means that fast, direct transfers are possible from memory to peripherals, peripherals to memory and peripheral to peripheral. For example, the use of a priority controller on the DMA bus lets the DMA peripherals move data in and out of the read/write memory

(RAM) at high speed, while SC/MP simply continues to chug along at human interface rates.

You can also use SC/MP's DMA lines to wire together several SC/MP CPU chips. This forms a multiprocessor system, in which the CPUs interface to the same address and data buses.

SC/MP has two control lines that provide for easy implementation of multiprocessor structures. Embedded in such structures, SC/MP waits for a non-busy bus, requests access and then waits for a Bus Enable signal. Until SC/MP receives the go-ahead it simply waits, with its address and data buses in their high-impedance states.

When SC/MP is the only bus controller in the system you can wire the Bus Enable line *high*, which lets SC/MP proceed with a bus I/O cycle whenever it is ready to do so.

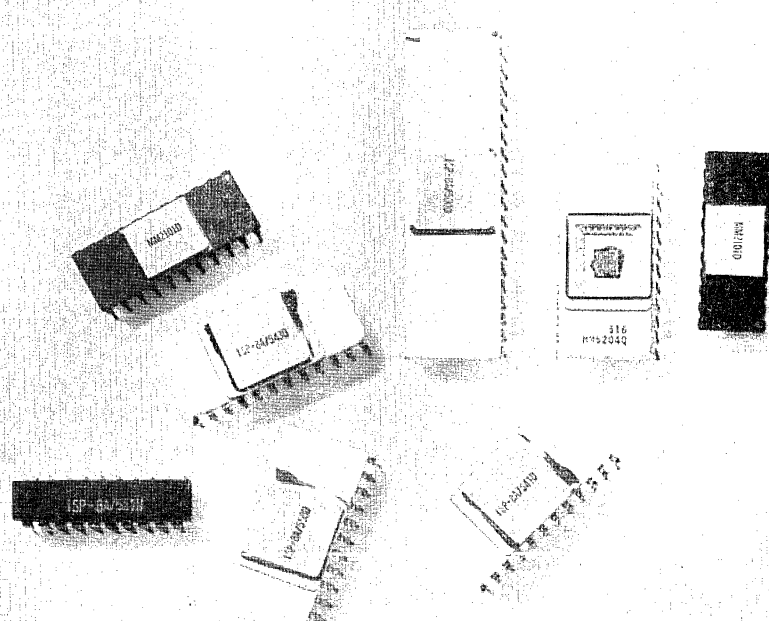
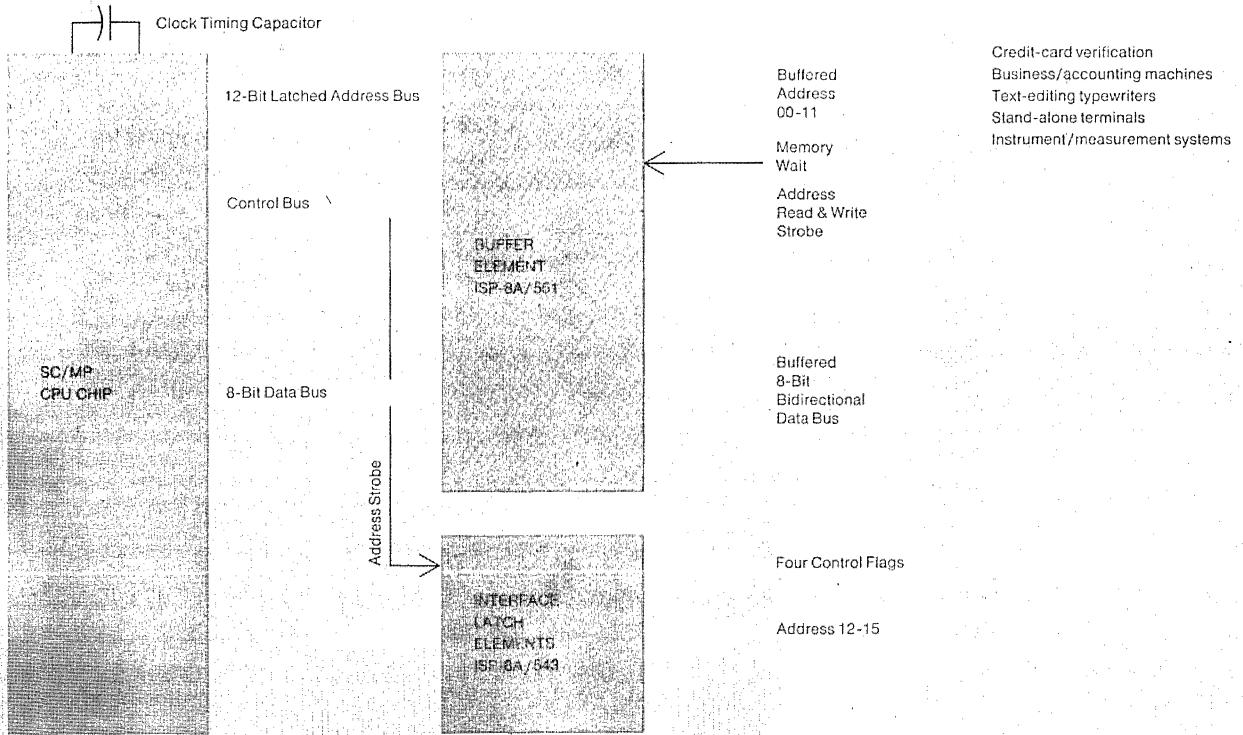


The SC/MP CPU chip

The SC/MP CPU chip is an 8-bit processing unit with 16-bit memory and peripheral addressing capabilities; its built-in features simplify your end of the design while letting SC/MP reach out and do its thing with everything connected to it.

For example, SC/MP provides flexible addressing to 65k bytes of memory or peripheral addresses by means of its four address-pointer registers. Also, you can use the status register's three flag outputs in several ways other than simply to supply internal software flags. By using them as encoded control lines, for instance, you can expand a SC/MP system's data I/O capabilities with input multiplexers and output demultiplexers, you can select particular banks of external memory and so on. And when you tell SC/MP what to do, its preprogrammed, on-chip, programmable logic array (PLA) assures proper instruction sequencing.

Expanded SC/MP system



MICROPROCESSOR National Semiconductor

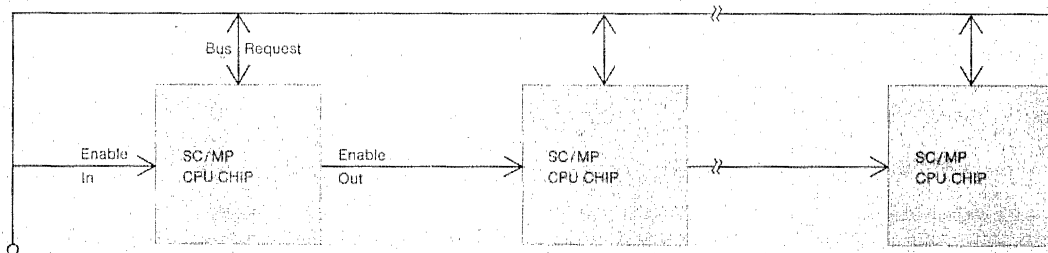
The significant CPU features, many of which are under your control through software, are shown in the table to the right.

The SC/MP CPU chip package features:

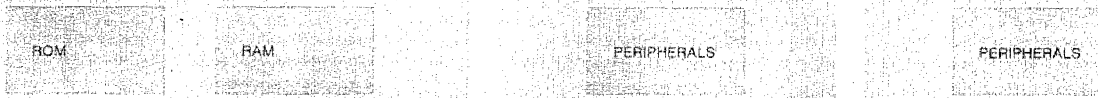
- The use of p-channel silicon-gate, depletion-load technology, which is a mature technology of good yield and low cost, and which is tolerant of power-supply variations
- Single power-supply operation of +10V to +14V, to facilitate direct CMOS interfacing
- A metal mask option for a TTL-compatible Tri-State I/O bus with 5-V logic swing
- A 40-pin dual-inline package available in ceramic or Epoxy B

Arithmetic/Logic Unit (ALU)	8-bit binary ADD, AND, OR, EXCLUSIVE OR; Two-digit BCD ADD
Data registers	8-bit accumulator; 8-bit extension register (provides separate serial I/O)
Address pointer registers	Four, 16-bits each; usable as stack pointers to external memory for unlimited subroutine nesting.
Status/flag register	8-bits wide; contents treatable as data or storable in memory
Address output register	16-bit address (65k bytes); 12-bits static (4k page); 4-bit output at address strobe time
Data I/O register	Buffers 8-bit data in and out
Instruction register	8-bit operations code
Instruction decode and control	Preprogrammed PLA structure assures proper instruction sequencing
Input/Output control	Handshake type for simplified interfacing and multiprocessing applications
Oscillator and timing generator	On-chip timing generation needs only external capacitor or crystal; Reduces component count in low-speed applications

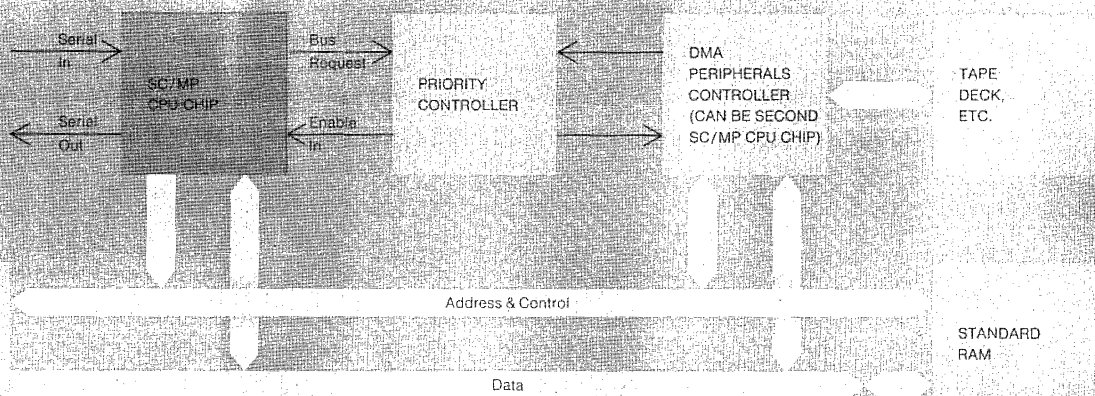
Multiprocessor network



Address & Control



DMA control using multiprocessor network



National backs you up

There's more to microprocessing than just the microprocessor, so your microprocessor supplier should be able to supply everything you'll need. National is such a supplier, because our philosophy is to sell solutions, not just parts.

Hardware Support We offer a complete Development System for SC/MP. Software is the key to the microprocessor approach to control system design, and our SC/MP Development System is the tool that will help you bring in your jobs on schedule and under budget.

The SC/MP Development System provides everything you'll need to develop, test and debug interfaces, application programs and even complete control systems. The Development System comes supplied with a microprocessor, peripheral interfaces, memory, power supply and chassis, and built-in DEBUG/System Monitor firmware. Its control panel lets you examine or change the contents of any memory location. And this same panel, because of the static design of the CPU, lets you step through your program one instruction at a time, which is a very efficient way to debug a program. (Try program development and debug on a microprocessor system without a control panel and you'll see what we mean.)

I/O to SC/MP's Development System is via teletypewriter or high-speed paper tape, and the system can address up to 65k bytes of memory.

We even offer a PROM programming option for the SC/MP Development System. And this means that you can complete all phases of a program development without any outside services and without buying any additional equipment.

Now, even though SC/MP is basically a single component—a microprocessor chip—we've developed a variety of application hardware for it. This hardware lets you perform rapid product evaluations, or you may choose to use it in preproduction systems. All of the application cards are on 4.38x4.86-inch standard PC cards, a size that assures you'll have no trouble using them in small equipment.

Standard SC/MP application hardware includes: a CPU card (ISP-8C/100), which holds a timing crystal, 256 bytes of RAM, 2k bytes of PROM, and all necessary buffering and address elements, control lines and so on; a 4k x 8 PROM/ROM card (ISP-8C/004P); and a 2k x 8 RAM card (ISP-8C/002).

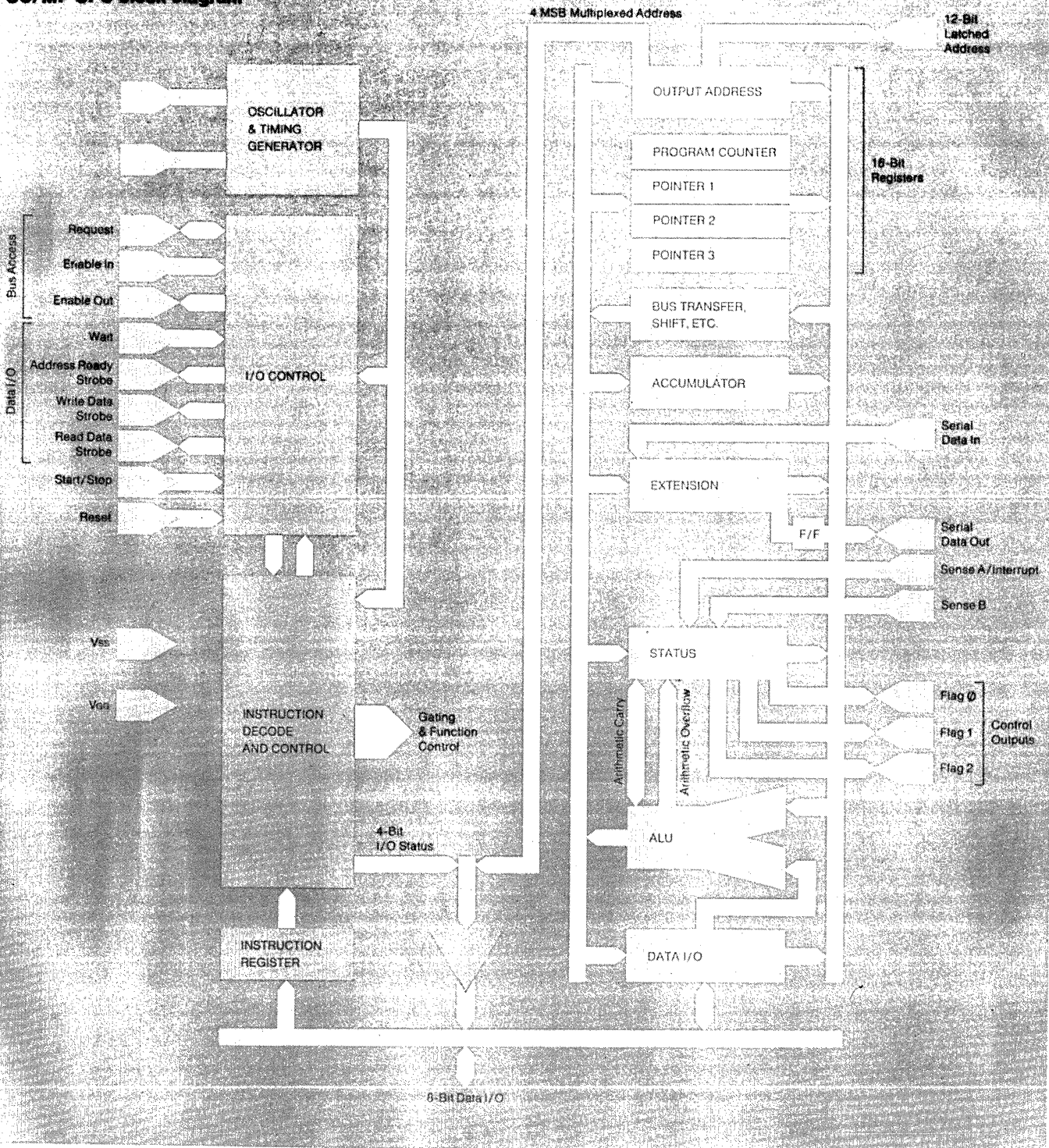
While SC/MP interfaces directly to CMOS devices, to provide CMOS-level system buses, many of today's interfaces are still TTL-level. And this is where our system support chips come in very handy. SC/MP's Blue Chips™ and Green Chips™ are designed specifically to help you build an efficient, economical microprocessor system with an absolute minimum package count, while still producing a true TTL system bus.

SC/MP's Blue Chip ISP-8A/551, for example, provides Tri-State buffering, while the Green Chip ILE/8 (ISP-8A/543) provides bidirectional interface latches.

Software/Firmware Support At National we consider software to be an integral part of microprocessing, not just an afterthought. So we offer a variety of software to support SC/MP in your system: DEBUG/System Monitor... Resident Conversational Assembler/Editor... System Diagnostics... Cross Assembler (available as a Fortran IV program and on timeshare services)... application routines (such as double-precision math, code conversions and so on). In addition, there are peripheral I/O drivers that let you interface your SC/MP system to high-speed paper tape, cassettes, printers and teletypewriters.

Documentation is still another aspect of support. The SC/MP Product Description, for example, fully specifies SC/MP in much the same way as does any component's data sheet. At the next level is the SC/MP Technical Description, which helps you establish system performance and prepare a preliminary system design; this manual also aids in the development of application programs and in the detailed system implementation, including interfaces. Then there is the SC/MP User's Manual, which not only helps you debug the application programs and hardware interfaces, but also helps you in the preparation of your system's own hardware and software documentation.

SC/MP CPU block diagram



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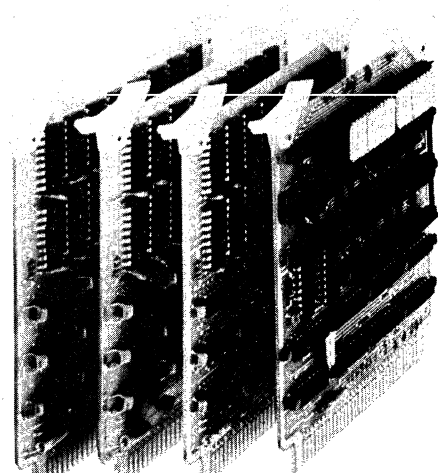
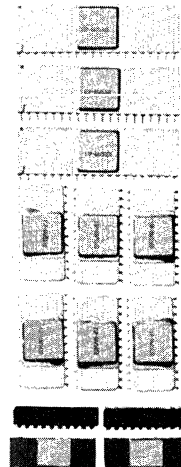
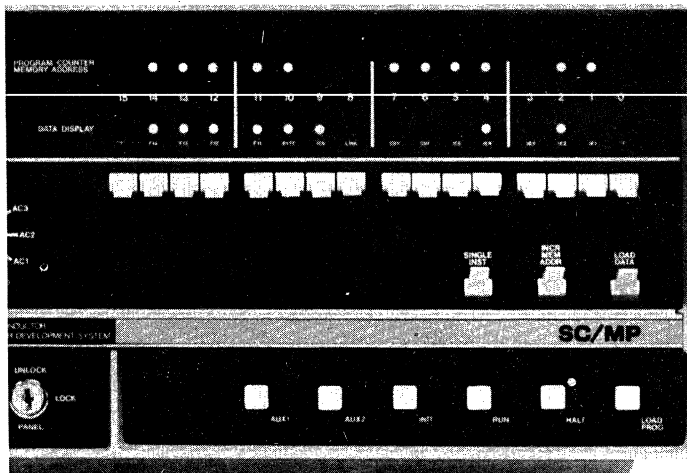
COMPUTE Our Club Of Microprocessor Programmers, Users and Technical Experts is an informal organization whose membership is composed of those who use, or are otherwise interested in, microprocessors. It is a vehicle of communications between and among National and COMPUTE's members.

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There is also a COMPUTE Software Library, from which programs submitted by members are available to other members for the cost of reproduction only.

National sells solutions. Our in-depth microprocessing experience helps us understand your problems. And we can help you to solve them... even to the point of providing a complete design service for your first system.

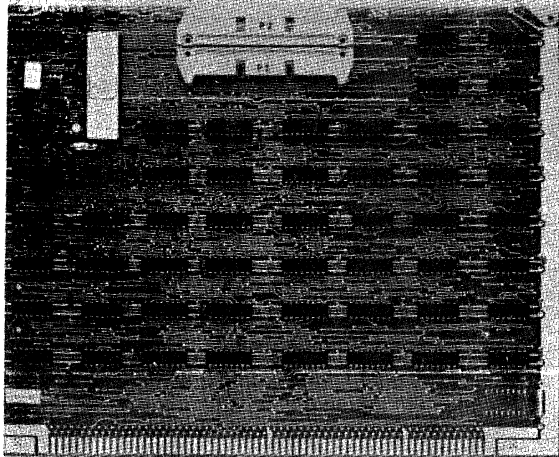
Remember: When you buy a microprocessor from National, you buy more than a chip and a data sheet.



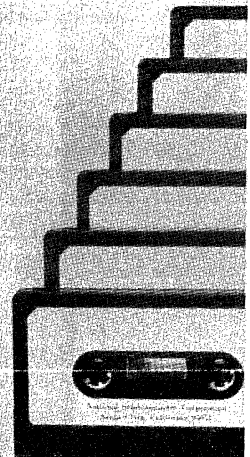
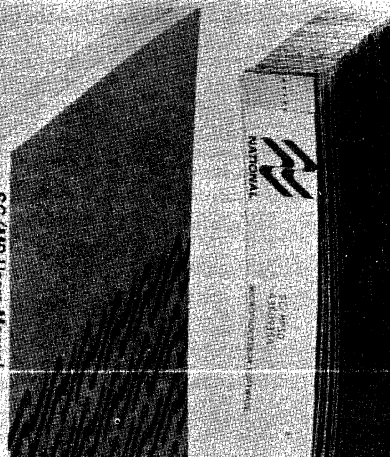
SC/MP instruction summary

(Typical execution time, 2 μ S/microcycle)

Double-byte instructions:		Execution time in microcycles	Single-byte instructions:		Execution time in microcycles	
Memory Reference	Load	18	Extension Register	Load AC from extension	6	
	Store	18		AND extension	6	
	AND	18		OR extension	6	
	OR	18		EXCLUSIVE OR extension	6	
	EXCLUSIVE OR	18	Decimal ADD extension	11		
	Decimal ADD	23	ADD extension	7		
	ADD	19	Complement and ADD extension	8		
Transfer	Complement and ADD	20	Pointer Register Move	Exchange pointer low	8	
	Jump	11		Exchange pointer high	8	
	Jump if positive	9, 11		Exchange pointer with PC	7	
	Jump if zero	9, 11	Shift, Rotate, Serial I/O	Serial I/O	5	
Jump if not zero	9, 11	Shift right		5		
Memory Increment/Decrement	Increment and load	22		Shift right with link	5	
	Decrement and load	22		Rotate right	5	
Immediate	Delay	3 to 132,096		Miscellaneous	Rotate right with link	5
					Halt	8
			Exchange AC and extension		7	
			Clear carry/link		5	
			Set carry/link		5	
			Disable interrupts		6	
Miscellaneous	Enable interrupts	6	Copy status to AC	5		
	Copy status to AC	5	Copy AC to status	6		
	Copy AC to status	6	No operation	5-10		
	No operation	5-10				



SC/MP Users Manual
SC/MP Technical Description



National Semiconductor

MICROPROCESSOR

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RCA-CDP1801 Microprocessor

The CDP1801 microprocessor is a CMOS 8-bit register-oriented central processing unit (CPU) designed for use as a general-purpose computing or control element in a wide range of stored-program systems or products. It is implemented by two LSI packages: the 40-lead CDP1801U control unit contains the arithmetic logic unit (ALU), the control logic, and various working registers; the 28-lead CDP1801R register unit contains the multi-purpose 16 x 16 register array, a buffer register, associated controls, and an increment/decrement circuit associated with the register array.

The CDP1801 microprocessor includes all the circuits required for fetching, interpreting, and executing instructions which have been stored in standard memories—RAM or ROM. An efficient one- or two-byte instruction format results in short efficient programs. Extensive input/output I/O control features are also provided to facilitate system design for lowest cost.

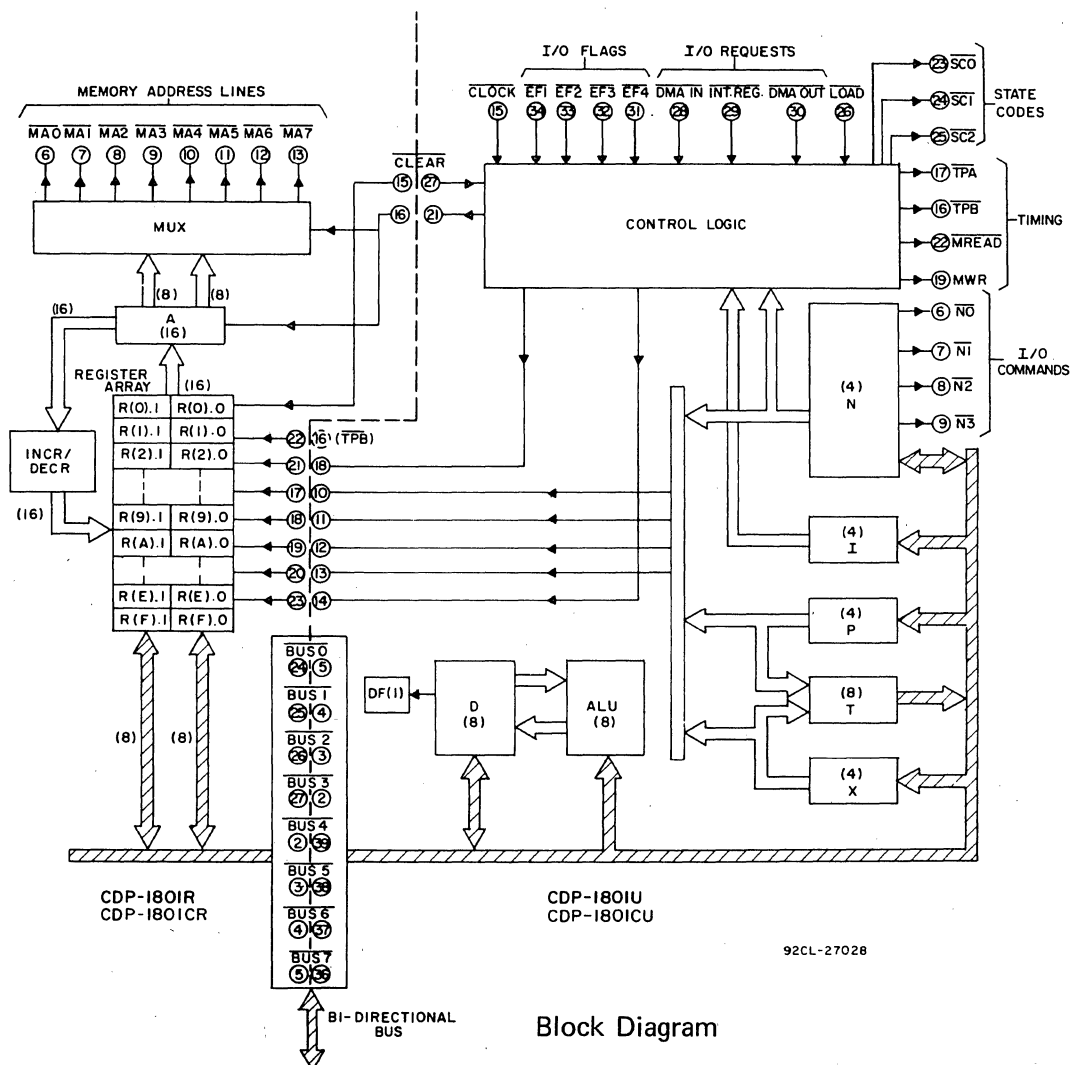
The CDP1801 also provides a synchronous interface to memories and external controllers for

I/O devices and minimizes the cost of interface controllers. The I/O interface is capable of supporting devices operating in polled, interrupt-driven, or direct-memory-access (DMA) modes.

The CDP1801 is available in two versions for different dc operating-voltage ranges. The basic unit operates over the complete range of 3 to 12 volts. The CDP1801C operates over a narrower range of 4 to 6 volts.

CMOS Technology

The CMOS technology used in the CDP1801 provides a high noise immunity so that the microprocessor can operate in electrically hostile environments. The units can be powered by unregulated power supplies over a wide operating-voltage range. The 1801 has two voltage supply pins so that it can operate at maximum speed while interfacing to various external circuit technologies, including TTL, at a lower voltage. Only a single-phase system clock is required, and the microprocessor power consumption



Block Diagram

See Special RCA DATABOOK offer on inside back cover

RCA-CDP1801 Microprocessor (cont'd)

is very low. Furthermore, the 1801 series is completely static, so that the system clock can be controlled to interface with slow memories or I/O devices. The units are capable of operating over the full -55°C to $+125^{\circ}\text{C}$ temperature range.

When operated from a typical power supply of from 10 to 12 volts, the CDP1801 can have a machine cycle time (8 clock pulses) of about 3 microseconds. If a 400-nanosecond RAM is used, the fetch-execute time for any instruction is 6 microseconds, the DMA rate is 333,000 bytes per second, and the interrupt response time is from 3 to 9 microseconds.

Easy-to-Use Instructions

The COSMAC microprocessor provides a set of simple, easy-to-use, general-purpose instructions. The on-chip scratchpad of sixteen general-purpose 16-bit registers may be used to provide multiple program counters, data pointers, and data storage. Three specific registers are treated by the hardware as an implicit DMA address pointer, a program counter for interrupt servicing, and an interrupt or subroutine stack pointer, respectively. A simple one-step program loading facility is provided on the chip. Unlimited subroutine or interrupt nesting is possible.

The I/O interface is designed to provide direct control of I/O devices so that over-all system complexity and cost can be reduced. Flexible, open-ended I/O instructions allow unlimited device attachment. The hardware I/O interface is capable of supporting devices operating in polled, interrupt-driven, and DMA modes.

The COSMAC Hardware Support Kit is a prototyping system for the development of systems based on the CDP1801 microprocessor. It is available in two versions. The basic Microkit (CDP18S001) is useful primarily for breadboard evaluation. A teletypewriter or equivalent terminal can be attached to this basic system. With such a terminal, the Microkit becomes a complete computer system. It is used primarily with RCA's CSDP—the powerful interactive COSMAC Software Development Package. In this mode of operation, the Microkit may be directly "down-loaded" from the CSDP computer by a single command.

A Stand-Alone Microkit (CDP18S002) is available for software development. This version contains additional RAM, allowing use of the COSMAC Resident Software System (CRSS). When a user-supplied terminal is provided, the Stand-Alone Microkit becomes a complete, self-contained microprocessor prototyping system.

Three software packages are available for use with the CDP1801 microprocessor. The COSMAC Software Development Package (CSDP) is the most versatile. It is available on GE Time-Share or in a Fortran IV version for installation on other interactive computer systems. The CSDP can also be used with the basic Microkit to provide a complete microprocessor prototyping system.

The Batch Assembler is a software program designed especially for users who have IBM-370 computers with virtual storage.

The COSMAC Resident Software System (CRSS) is designed expressly for use in the Stand-Alone Microkit.

OPERATING CONDITIONS AT $T_A = 25^{\circ}\text{C}$ Unless Otherwise Specified
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	CONDITIONS		LIMITS				UNITS
	V_{CC}^1 (V)	V_{DD} (V)	CDP1801		CDP1801C		
			Min.	Max.	Min.	Max.	
Supply-Voltage Range (At $T_A = \text{Full Package-Temperature Range}$)	—	—	3	12	4	6	V
Recommended Input Voltage	—	—	V_{SS}	V_{CC}	V_{SS}	V_{CC}	V
Clock Input Rise or Fall Time, t_r, t_f	3-15	3-15	—	15	—	15	μs
Instruction Time (See Fig. 4)	5	5	16	—	16	—	μs
	5-10	10	6	—	—	—	
Clock Input Frequency, f_{CL}	5	5	DC	1	DC	1	MHz
	5-10	10	DC	3	—	—	
Clock Pulse Width, t_{WL}, t_{WH}	5	5	500	—	500	—	ns
	5-10	10	160	—	—	—	
Clear Pulse Width	5	5	500	—	500	—	ns
	5-10	10	160	—	—	—	
Data Hold Time, t_{DH}	5	5	0	—	0	—	ns
	5-10	10	0	—	—	—	

Notes:

- $V_{CC} \leq V_{DD}$. For CD1801C $V_{DD} = V_{CC} = 5$ volts.
- Because a large number of nodes may be switching simultaneously, a 0.1 μF by-pass capacitor is recommended in the power supply.
- In order to maintain proper circuit operation, the CDP1801 intra-unit wiring capacitance should be less than 25 pF.

MAXIMUM RATINGS, Absolute-Maximum Values

- Storage-Temperature Range (T_{stg}) -65 to $+150^{\circ}\text{C}$
- Operating-Temperature Range (T_A) -55 to $+125^{\circ}\text{C}$
- DC Supply-Voltage Range (V_{CC}, V_{DD})
(All voltage values referenced to V_{SS} terminal)
 $V_{CC} \leq V_{DD}$:
CDP1801 0.5 to $+15$ V
CDP1801C 0.5 to $+7$ V
- Power Dissipation Per Package (P_D):
For $T_A = -55$ to $+100^{\circ}\text{C}$ 500 mW
For $T_A = +100$ to $+125^{\circ}\text{C}$ Derate Linearly to 200 mW
- Device Dissipation Per Output Transistor:
For $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ 100 mW
- Input Voltage Range, All Inputs -0.5 to $V_{DD} + 0.5$ V
- Lead Temperature (During Soldering):
At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max. $+265^{\circ}\text{C}$

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MICROPROCESSOR RCA Solid State

RCA-CDP1801 Microprocessor (cont'd)

Simple but Powerful Architecture:

- 8-bit parallel organization
- 8-bit bidirectional common data bus for input/output and memory
- multiple program counters
- multiple data registers
- multiple address registers
- immediate address mode
- indirect pointer address mode
- short efficient instructions to keep programs short
- ALU overflow bit testable by branch instructions

Easy-to-Use Instructions:

- one- or two-byte instruction format
- 57 easy to use instructions
- add, subtract, shift, and logical operations
- flexible subroutine nesting procedures
- simple 1-byte subroutine call

I/O Flexibility:

- general-purpose interface for any RAM/ROM memory
- separate memory address lines
- memory addressing up to 65,536 bytes
- program interrupt mode
- program-controlled interrupt mask (enable/disable)
- flexible programmed I/O
- four flag inputs directly testable by branch instructions
- separate 4-bit I/O control signal
- two I/O sync pulses provided
- single-pulse clear

- self-contained DMA control
- built-in program load mode
- TTL compatibility on inputs and outputs, if desired

CMOS Technology:

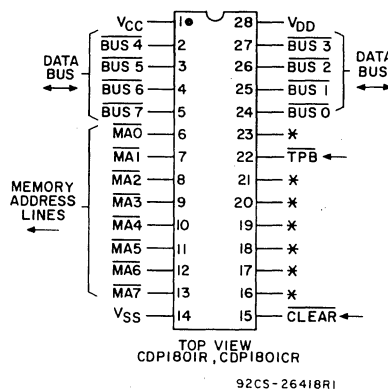
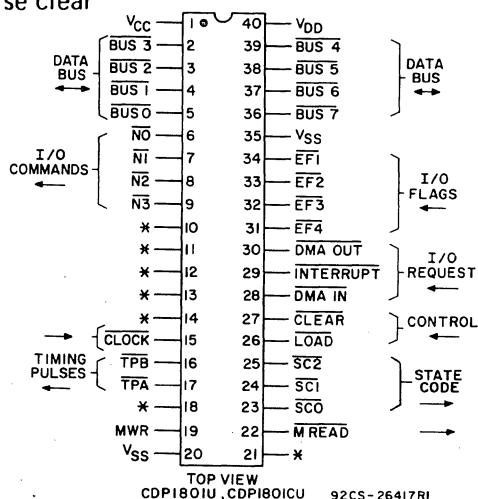
- static CMOS circuitry
- low power consumption
- single supply voltage option
- 3 - 12 V dc operating range (4 - 6 V dc for the CDP1801C)
- high noise immunity
- single-phase clock

Literature

Form No.	Title	Price
MPM-101	User Manual for the COSMAC Microprocessor	\$ 5.00
MPM-102	Program Development Guide for the COSMAC Microprocessor	10.00
MPM-103	COSMAC Microkit Operator's Manual	10.00
MPM-104	Installation Manual for the COSMAC Software Development Package	10.00
MPM-105	Installation Manual for the COSMAC Batch Assembler	10.00
*MPM-106	Library of COSMAC Arithmetic Subroutines	5.00
*MPM-107	Universal COSMAC I/O Design Manual	5.00
MPM-108	COSMAC Resident Software Manual	5.00

*Available 1976

Terminal Assignment Diagrams



Package Interconnections

Pin Terminals To:

	1	2	3	4	5	10	11	12	13	14	16	18	21	27	36	37	38	39	40
CDP1801U,CU	1	2	3	4	5	10	11	12	13	14	16	18	21	27	36	37	38	39	40
CDP1801R,CR	1	27	26	25	24	17	18	19	20	23	22	21	16	15	5	4	3	2	28

* These pins are for interchip connections only.

Notes:

- Any unused input pins should be connected to V_{DD} or V_{CC}.
- The DATA BUS lines are bi-directional and have three-state outputs. They may be individually connected to V_{CC} through external pull-up resistors (22 K Ω recommended) to prevent floating inputs.
- All inputs have the same noise immunity and level-shifting capability. All outputs have the same drive capability whether they have three-state outputs or not.
- For the CDP1801C, V_{CC} must be connected to V_{DD}.

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INTRODUCING THE 2650 FAMILY

*"5-VOLT SYSTEM REDUCES SYSTEM COSTS"
"2650 PUTS THE INTERFACE ON THE CHIP...NOT ON THE CIRCUIT BOARD"
"POWERFUL INSTRUCTION SET PROVIDES LOWER COST SYSTEMS"*

The greatly increased sophistication and rising production costs of today's logic systems force the system designer to use every available resource in order to economically produce his system. In keeping with this cost reduction goal, Signetics has developed a powerful general purpose integrated microprocessor called the 2650. The first Signetics microprocessor, in conjunction with Signetics MOS and Bipolar memory and interface product lines, offers the system designer a viable and attractive alternative to the hard-wired approach to system design. For many applications, the system designer can use this general purpose microprocessor and standard memory and interface circuits to implement systems with lower cost than the hard-wired logic approach without sacrificing performance.

By using the 2650 and compatible products, the system designer can obtain two other major benefits of microcomputer systems. These benefits are greatly enhanced system flexibility and minimized design or modification cycles compared with the hard-wired logic approach.

The requirements of the majority of applications for integrated microprocessors (logic replacement and control functions) have defined a general set of processor parameters based on system and device economies, ease of use, and speed requirements.

These characteristics include:

- Single chip
- Fixed instruction set
- Eight bit parallel structure
- TTL compatibility

In addition to these characteristics, the design of the 2650 has been optimized around three generalized objectives:

- Lowest system cost
- Ease of use
- Capable of a wide range of applications

The optimum technology choice for implementing these features is the low threshold ion-implanted N-Channel silicon gate process. This process has matured in the past few years, providing a combination of high density, low threshold voltage, moderate speed and good manufacturing yields. Using this technology, a total of 576 bits of ROM, approximately 250 bits of register and about 900 logic gates are used to implement the processor function on the 2650 chip.

The instruction set consists of 75 instructions, of which about 40% consists of arithmetic instructions. This class contains the Boolean, arithmetic, and compare operations, each of which may be executed using any one of eight addressing modes. Another 30% of the instruction set consists of branch instructions which incorporate six addressing modes. The remaining 30% of the instruction set includes, among others, I/O instructions, instructions for performing operations on the two status registers, a decimal adjust instruction and the HALT instruction.

Utilizing multiple addressing modes greatly increases coding efficiency, allowing functions to be performed using fewer instructions than less powerful machines. The resulting reduction in routine execution time and memory capacity requirements directly translates into improved system performance and reduced memory cost. In this way the powerful instruction set and addressing modes of the 2650 allow a significant reduction in the memory required to perform a given function, resulting in sizeable system cost savings without sacrificing performance.

PROCESSOR HARDWARE DESCRIPTION

ARCHITECTURE

GENERAL DESCRIPTION

A block diagram of the processor is shown in Figure 1. The first, second, and third bytes of instructions are read into the processor on the data bus and loaded into the Instruction Register, Holding Register, and Data Bus Register, respectively. The instructions are decoded through a combination of ROM and random logic.

The ALU performs arithmetic, Boolean, and combinatorial shifting functions. It operates on eight bits in parallel and utilizes carry-look-ahead logic. A second adder is used to increment the instruction address register and to calculate operand addresses for the indexed and relative addressing modes. This separate address adder allows complex addressing modes to be implemented with no increase in instruction execution time.

The General Purpose Register Stack and the Subroutine Return Address Stack are implemented with static RAM cells. The Register Stack consists of seven 8-bit registers. The Subroutine Stack can contain eight 15-bit addresses, thereby allowing eight levels of subroutine nesting. Placing the Subroutine Stack on the chip allows efficient ROM-only systems to be implemented in some applications. Separate 15-bit Instruction Address and Operand Address Registers are provided. The 2650 is an 8-bit binary processor with BCD capability. See Figure 2 for a diagram of the 2650 registers as seen by the programmer.

PROGRAM STATUS WORD

The Program Status Word (PSW) is a major feature of the 2650 with greatly increases its flexibility and processing power. The PSW is a special purpose register within the processor that contains status and control bits.

It is divided into two bytes called the Program Status Upper (PSU) and Program Status Lower (PSL). The PSW bits may be tested, loaded, stored, preset, or cleared using the instructions which affect the PSW. The bits are utilized as follows:

- PSU0, 1, 2 — SP — **Pointer** for the Return Address Stack.
- PSU5 — II — Used to **Inhibit** recognition of additional **Interrupts**.
- PSU6 — F — **Flag** is a latch directly driving the flag output.
- PSU7 — S — **Sense** equals the state of the sense input.
- PSL0 — C — **Carry** stores any carry from the high-order bit of the ALU.
- PSL1 — COM — **Compare** determines if a logical or arithmetic comparison is to be made.
- PSL2 — OVF — **Overflow** is set if a two's complement overflow occurs.
- PSL3 — WC — **With Carry** determines if the carry is used in arithmetic and rotate instructions.
- PSL4 — RS — **Register Select** identifies which bank of 3 GP registers is being used.
- PSL5 — IDC — **Inter Digit Carry** stores the bit-3-to-bit-4 carry in arithmetic operations.
- PSL6, 7 — CC — **Condition Code** is affected by compare, test and arithmetic instructions.

INTERRUPT HANDLING CAPABILITY

The 2650 has a single level hardware vectored interrupt capability. When an interrupt occurs, the 2650 finishes the current instruction and sets the

Interrupt Inhibit bit in the PSW. The processor then executes a Branch to Subroutine Relative to location Zero (ZBSR) instruction and sends out Interrupt Acknowledge and Operation Request signals. On receipt of the INTACK signal the interrupting device inputs an 8-bit address, the interrupt vector, on the data bus. The relative and relative indirect addressing modes combined with this 8-bit address allow interrupt service routines to begin at any addressable memory location.

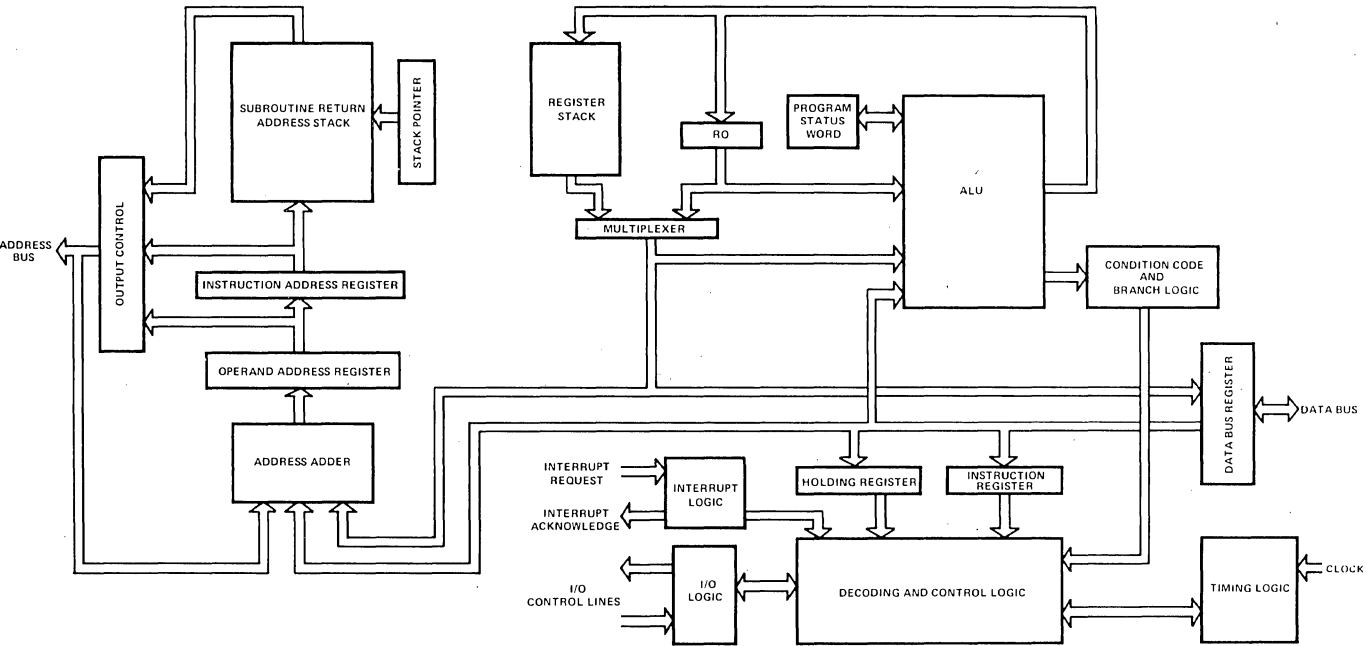
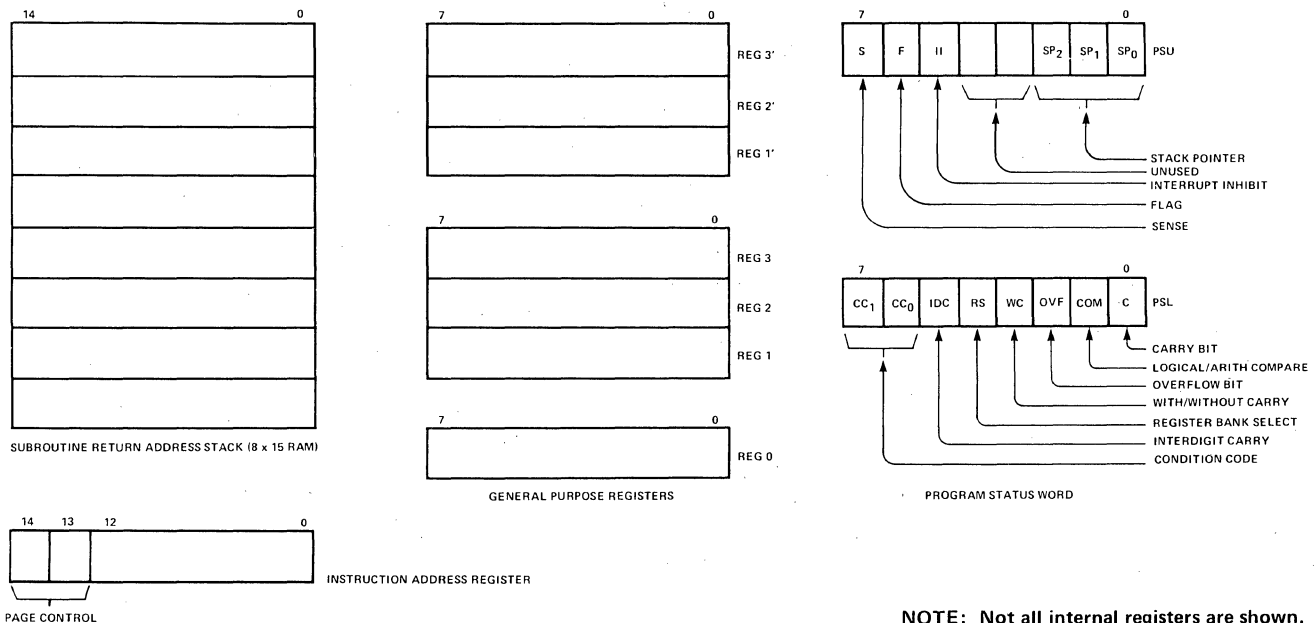


Figure 1. BLOCK DIAGRAM



NOTE: Not all internal registers are shown.

Figure 2. MAJOR 2650 REGISTERS

INTERFACING

INTRODUCTION TO INTERFACING WITH THE 2650

Five key concepts have been incorporated in the 2650 to make interfacing easy and inexpensive. The extent to which these concepts have been incorporated in the Signetics 2650 provides unique benefits of system density and low cost to the system designer.

1. SINGLE 5V POWER SUPPLY

Low threshold double ion-implanted Silicon Gate N-Channel MOS technology is used to allow operation from one +5V power supply with resultant cost savings and improved reliability. This reduces power consumption significantly compared with the multi-power supply approach.

2. INTERFACE CIRCUIT COMPATIBILITY

The 2650 inputs and outputs are specified to be compatible with widely available, standard, low cost logic families such as TTL, CMOS and Low-power STTL. This includes the single phase clock input which saves the cost of high level multiphase clock driver circuitry. Bus outputs are tri-state and capable of driving one 7400 TTL load or four 74LS loads. The 2650 is capable of driving several loads of pnp-buffered STTL inputs. Many MSI, Interface and Memory LSI circuits (for example, in Signetics 82S00 and 8T00 series) have these low current pnp inputs and are recommended for use in 2650 microcomputer systems. See Table 1 for DC characteristics of the 2650.

3. USE OF STANDARD MEMORIES

One of the major 2650 design achievements is to operate efficiently in a system using industry standard memories, for example 1024 X 1 and 256 X 4 N-channel RAMs and 1024 X 8 N-Channel ROMs. These standard memories are widely available and used in volume with corresponding low cost. Non-standard memories, particularly those produced by only one manufacturer will be less available, run in lower volume and often cost 2 to 3 times as much per bit as industry standard products. The 2650 operates successfully with memories of any access time, due to the completely asynchronous interface that is provided for this purpose. Memories which respond in less than 0.8 microseconds allow the processor to operate at maximum speed.

4. NO SPECIAL INTERFACE PRODUCTS

Similarly, another major achievement is to operate efficiently in a system using no special I/O products. This approach avoids the problems of a system requiring high cost specialized components with restricted availability.

TABLE 1. PRELIMINARY 2650 DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
I _{LI}	Input Load Current	V _{IN} = 0 to 5.25V		10	μA
I _{LOH}	Output Leakage Current	ADREN, DBUSEN = 2.2V, V _{OUT} = 4V		10	μA
I _{LOL}	Output Leakage Current	ADREN, DBUSEN = 2.2V, V _{OUT} = 0.45V		10	μA
I _{CC}	Power Supply Current	V _{CC} = 5.25V, T _A = 0°C		100	mA
V _{IL}	Input Low		-0.6	0.8	V
V _{IH}	Input High		2.2	V _{CC}	V
V _{OL}	Output Low	I _{OL} = 1.6 mA	0.0	0.45	V
V _{OH}	Output High	I _{OH} = -100 μA	2.4	V _{CC} -0.5	V
C _{IN}	Input Capacitance	V _{IN} = 0V		10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V		10	pF

Conditions: T_A = 0°C to 70°C, V_{CC} = 5V ±5%

5. POWERFUL MEMORY AND I/O INTERFACE

The following features characterize the memory and I/O interfaces:

- Both memory and input/output may operate in a completely asynchronous fashion. Consequently, devices operating at any speed up to the maximum data transfer rate may be connected without buffering. External latching of data from these interfaces is not required.
- Data paths are driven with tri-state buffers, allowing multiprocessor and Direct Memory Access (DMA) configurations to be designed.
- Eight-bit data paths communicate data in parallel.
- One- and two-byte I/O instructions provide maximum flexibility and efficiency when interfacing with I/O devices.

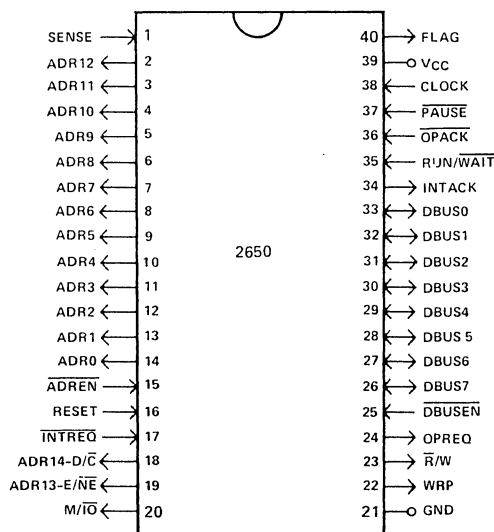


Figure 3. PIN CONFIGURATION

PIN CONFIGURATION AND INTERFACE SIGNAL DEFINITION

Refer to Figure 3 for the 2650 pin configuration. Signals are defined as follows:

- ADR0-ADR12 — The low order 13 bits of address for memory access are on these pins. ADR0-ADR7 are also used in two-byte I/O instructions. These outputs are tri-state buffers controlled by ADREN.
- ADR13-E/NE — This multiplexed output signal delivers the ADR13 address bit when M/IO is in the M phase or discriminates between Extended and Non-Extended I/O instructions when M/IO is in the I/O phase.
- ADR14-D/C — Address 14 or Data/Control is a multiplexed output signal. This pin delivers the ADR14 address bit when M/IO is in the M phase or discriminates between Data and Control I/O instructions when M/IO is in the I/O phase.
- ADREN — Address Bus Enable is an input providing the external control for the ADR0-ADR12 tri-state buffer drivers.
- DBUS0-DBUS7 — This is the 8-bit, bidirectional tri-state bus over which most data is communicated into or out of the processor.
- $\overline{\text{DBUSEN}}$ — Data Bus Enable is an input that controls the tri-state buffer drivers for DBUS0 to DBUS7.
- OPREQ — Operation Request is an output signal that informs external devices that the information on other output pins is valid.

OPACK	— Operation Acknowledge is an input which is used by external devices to end an I/O or memory signaling sequence.
M/IO	— Memory/Input-Output. This output informs external devices whether Memory or Input/Output functions are being performed.
R/W	— This output signal describes an I/O or memory operation as Read or Write, and defines whether the bidirectional DBUS is transmitting or receiving.
WRP	— This Write Pulse is generated during write sequences and may be used to strobe memory or I/O devices.
SENSE	— Is an input, independent of the other I/O signals, that provides a direct input to the processor.
FLAG	— This pin provides a direct output signal that is completely independent of the other I/O signals.
INTREQ	— Interrupt Request. This input is used by external devices to force the processor into the Interrupt sequence.
INTACK	— Interrupt Acknowledge is the signal used by the processor to inform external devices that it has entered an interrupt sequence.
PAUSE	— Pause is used to temporarily stop the processor at the end of the current instruction. It may stop processing for an indefinite length of time and is available to use for DMA (Direct Memory Access).
RUN/WAIT	— Informs external circuits as to the Run/Wait status of the 2650 processor.
RESET	— Is an input used to cause the 2650 to begin processing from a known state.
CLOCK	— This is the only clock input to the processor. It accepts standard TTL levels.
VCC	— +5V power.
GND	— The logic and power supply ground for the processor.

2650 TIMING

The clock input to the 2650 provides the basic timing information that the processor uses for all its internal and external operations. The clock rate determines the instruction execution time, except to the extent that external memories and devices slow the processor down. The maximum clock rate of the standard 2650 is 1.25 Megacycles (one clock period is 800ns minimum). One unique feature of the 2650 is that the clock frequency may be slowed down to DC, allowing complete timing flexibility for interfacing. This feature permits single stepping the clock which can greatly simplify system check-out. It also provides an easy method to halt the processor. Each 2650 cycle is comprised of three clock periods. Direct instructions require either 2, 3, or 4 processor cycles for execution and, therefore, vary from 4.8 to 9.6 μ s in duration.

A timing diagram for a memory read cycle is shown in Figure 4. OPREQ (Operation Request) is the master control signal that coordinates all operations external to the processor. When true, OPREQ indicates that other output signals are valid. During a memory read cycle M/IO is in the M (Memory) state and R/W is in the R (Read) state. The address lines and the control lines become valid before OPREQ rises. The data to be read may be returned anytime after OPREQ becomes valid. An OPACK (Operation Acknowledge) should accompany the read data from the memory. The Data and OPACK signals should remain valid for 50 ns after OPREQ falls.

INPUT/OUTPUT INTERFACE

The 2650 microprocessor has a set of versatile I/O instructions and can perform I/O operations in a variety of ways. One- and two-byte I/O instructions are provided, as well as a special single-bit I/O facility. The I/O modes provided by the 2650 are designated as Data, Control, and Extended I/O.

Data or Control I/O instructions are one byte long. Any general purpose register can be used as the source or destination. A special control line indicates if either a Data or Control instruction is being executed. Extended I/O is a two-byte read or write instruction. Execution of an extended I/O instruction will cause an 8-bit address, taken from the second byte of the instruction, to be placed on the low order eight address lines. The data, which can originate or terminate with any general purpose register, is placed on the data bus. This type of I/O can be used to simultaneously select a device and send data to it.

Memory reference instructions that address data outside of physical memory may also be used for I/O operations. When an instruction is executed, the address may be decoded by the I/O device rather than memory.

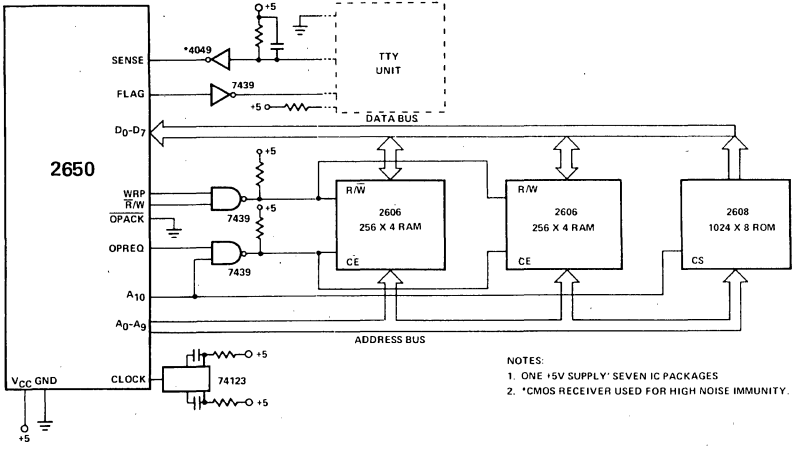
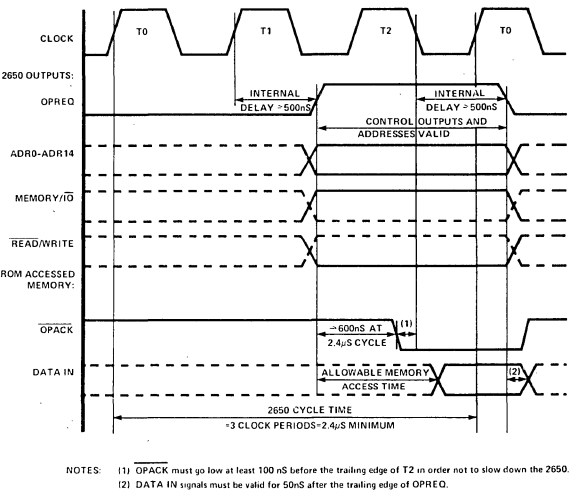
MEMORY INTERFACE

The memory interface consists of the address bus, the 8-bit data bus and several signals that operate in an interlocked or handshaking mode.

The Write Pulse signal is designed to be used as a memory strobe signal for any memory type. It has been particularly optimized to be used as the Chip Enable or Read/Write signal for the Signetics 2602 and 2606 RAMs.

INTERFACING – A MINIMAL SYSTEM EXAMPLE

The 2650 has been designed for low cost, easy interfacing, which is dramatically illustrated by a minimal system configuration shown in Figure 5. This system has a Teletype interface, 1024 bytes of ROM, and 256 bytes of RAM, yet requires only seven (7) standard integrated circuit packages. The ROM can contain a bootstrap loader and I/O driver programs for the Teletype. Other programs could reside in ROM or be read into RAM via the Teletype. An alternative to the 2608 N-Channel MOS ROM is the 82S115 Bipolar PROM which offers a 512 X 8 organization. Only one +5-volt power supply is required for this system. The advantages of conceptual simplicity and minimum system costs of the 2650 approach will be obvious to the system designer, particularly when compared to alternative microprocessor products.



- NOTES:
- 1. ONE +5V SUPPLY* SEVEN IC PACKAGES
- 2. *CMOS RECEIVER USED FOR HIGH NOISE IMMUNITY.

Figure 4. MEMORY READ CYCLE TIMING

Figure 5. SEVEN PACKAGE MINIMAL SYSTEM

MICROPROCESSOR

INSTRUCTION SET

It may be seen from examination of the 2650 instruction set that there are many powerful instructions which are all easily understood and are typical of larger computers. There are one-, two-, and three-byte instructions as a result of the multiplicity of addressing modes. See Table 2 for a complete listing and Figure 6 for instruction formats.

Automatic incrementing or decrementing of an index register is available in the arithmetic indexed instructions. All of the branch instructions except indexed branching can be conditional.

Register-to-register instructions are one byte; register-to-storage instructions are two or three bytes long. The two-byte register-to-memory instructions are either immediate or relative addressing types.

TABLE 2. INSTRUCTION SET

	MNEMONIC	OP CODE	FORMAT*	DESCRIPTION OF OPERATION	AFFECTS	CYCLES	
LOAD/STORE	LOD	Z	000 000	1Z	Load Register Zero	CC (Note 1)	2
		I	000 001	2I	Load Immediate	CC (Note 1)	2
		R	000 010	2R	Load Relative	CC (Note 1)	3
		A	000 011	3A	Load Absolute	CC (Note 1)	4
	STR	Z	110 000	1Z	Store Register Zero ($r \neq 0$)	CC (Note 1)	2
		R	110 010	2R	Store Relative	—	3
A		110 011	3A	Store Absolute	—	4	
ARITHMETIC	ADD	Z	100 000	1Z	Add to Register Zero w/wo Carry	C, CC (Note 1), IDC, OVF	2
		I	100 001	2I	Add Immediate w/wo Carry	C, CC (Note 1), IDC, OVF	2
		R	100 010	2R	Add Relative w/wo Carry	C, CC (Note 1), IDC, OVF	3
		A	100 011	3A	Add Absolute w/wo Carry	C, CC (Note 1), IDC, OVF	4
	SUB	Z	101 000	1Z	Subtract from Register Zero w/wo Borrow	C, CC (Note 1), IDC, OVF	2
		I	101 001	2I	Subtract Immediate w/wo Borrow	C, CC (Note 1), IDC, OVF	2
		R	101 010	2R	Subtract Relative w/wo Borrow	C, CC (Note 1), IDC, OVF	3
		A	101 011	3A	Subtract Absolute w/wo Borrow	C, CC (Note 1), IDC, OVF	4
	DAR		100 101	1Z	Decimal Adjust Register	CC (Note 2)	3
	LOGICAL	AND	Z	010 000	1Z	AND to Register Zero ($r \neq 0$)	CC (Note 1)
I			010 001	2I	AND Immediate	CC (Note 1)	2
R			010 010	2R	AND Relative	CC (Note 1)	3
A			010 011	3A	AND Absolute	CC (Note 1)	4
IOR		Z	011 000	1Z	Inclusive OR to Register Zero	CC (Note 1)	2
		I	011 001	2I	Inclusive OR Immediate	CC (Note 1)	2
		R	011 010	2R	Inclusive OR Relative	CC (Note 1)	3
		A	011 011	3A	Inclusive OR Absolute	CC (Note 1)	4
EOR		Z	001 000	1Z	Exclusive OR to Register Zero	CC (Note 1)	2
		I	001 001	2I	Exclusive OR Immediate	CC (Note 1)	2
		R	001 010	2R	Exclusive OR Relative	CC (Note 1)	3
		A	001 011	3A	Exclusive OR Absolute	CC (Note 1)	4
ROTATE COMPARE	COM	Z	111 000	1Z	Compare to Register Zero Arithmetic/Logical	CC (Note 3)	2
		I	111 001	2I	Compare Immediate Arithmetic/Logical	CC (Note 4)	2
		R	111 010	2R	Compare Relative Arithmetic/Logical	CC (Note 4)	3
		A	111 011	3A	Compare Absolute Arithmetic/Logical	CC (Note 4)	4
ROTATE COMPARE	RRR	010 100	1Z	Rotate Register Right w/wo Carry	C, CC, IDC, OVF	2	
	RRL	110 100	1Z	Rotate Register Left w/wo Carry	C, CC, IDC, OVF	2	
BRANCH	BCT	R	000 110	2R	Branch On Condition True Relative	—	3
		A	000 111	3B	Branch On Condition True Absolute	—	3
	BCF	R	100 110	2R	Branch On Condition False Relative	—	3
		A	100 111	3B	Branch On Condition False Absolute	—	3
	BRN	R	010 110	2R	Branch On Register Non-Zero Relative	—	3
		A	010 111	3B	Branch On Register Non-Zero Absolute	—	3
	BIR	R	110 110	2R	Branch On Incrementing Register Relative	—	3
		A	110 111	3B	Branch On Incrementing Register Absolute	—	3
	BDR	R	111 110	2R	Branch On Decrementing Register Relative	—	3
		A	111 111	3B	Branch On Decrementing Register Absolute	—	3
ZBRR		100 110 11	2ER	Zero Branch Relative, Unconditional	—	3	
BXA		100 111 11	3EB	Branch Indexed Absolute, Unconditional (Note 5)	—	3	

TABLE 2. INSTRUCTION SET (CONTINUED)

	MNEMONIC	OP CODE	FORMAT*	DESCRIPTION OF OPERATION	AFFECTS	CYCLES
SUBROUTINE BRANCH/RETURN	BST	R 001 110	2R	Branch To Subroutine On Condition True, Relative	SP	3
		A 001 111	3B	Branch To Subroutine On Condition True, Absolute	SP	3
	BSF	R 101 110	2R	Branch To Subroutine On Condition False, Relative	SP	3
		A 101 111	3B	Branch To Subroutine On Condition False, Absolute	SP	3
	BSN	R 011 110	2R	Branch To Subroutine On Non-Zero Register, Relative	SP	3
		A 011 111	3B	Branch To Subroutine On Non-Zero Register, Absolute	SP	3
	ZBSR	101 110 11	2ER	Zero Branch To Subroutine Relative, Unconditional	SP	3
BSXA	101 111 11	3EB	Branch To Subroutine, Indexed, Absolute Unconditional (Note 5)	SP	3	
RET	C 000 101	1Z	Return From Subroutine, Conditional	SP	3	
	E 001 101	1Z	Return From Subroutine and Enable Interrupt, Conditional	SP, II	3	
INPUT/OUTPUT	WRD	111 100	1Z	Write Data	—	2
	REDD	011 100	1Z	Read Data	CC (Note 1)	2
	WRTC	101 100	1Z	Write Control	—	2
	REDC	001 100	1Z	Read Control	CC (Note 1)	2
	WRTE	110 101	2I	Write Extended	—	3
	REDE	010 101	2I	Read Extended	CC (Note 1)	3
MISC.	HALT	010 000 00	1E	Halt, Enter Wait State	—	2
	NOP	110 000 00	1E	No Operation	—	2
	TMI	111 101	2I	Test Under Mask Immediate	CC (Note 6)	3
PROGRAM STATUS	LPS	U 100 100 10	1E	Load Program Status, Upper	F, II, SP	2
		L 100 100 11	1E	Load Program Status, Lower	CC, IDC, RS, WC, OVF, COM, C	2
	SPS	U 000 100 10	1E	Store Program Status, Upper	CC (Note 1)	2
		L 000 100 11	1E	Store Program Status, Lower	CC (Note 1)	2
	CPS	U 011 101 00	2EI	Clear Program Status, Upper, Masked	F, II, SP	3
		L 011 101 01	2EI	Clear Program Status, Lower, Masked	CC, IDC, RS, WC, OVF, COM, C	3
	PPS	U 011 101 10	2EI	Preset Program Status, Upper, Masked	F, II, SP	3
		L 011 101 11	2EI	Preset Program Status, Lower, Masked	CC, IDC, RS, WC, OVF, COM, C	3
TPS	U 101 101 00	2EI	Test Program Status, Upper, Masked	CC (Note 6)	3	
	L 101 101 01	2EI	Test Program Status, Lower, Masked	CC (Note 6)	3	

*FORMAT CODE: The number indicates the number of bytes. The letter(s) indicate the format type(s). See Fig. 6.

NOTES:

1. Condition code (CC1, CC0): 01 if positive, 00 if zero, 10 if negative.
2. Condition code is set to a meaningless value.
3. Condition code (CC1, CC0): 01 if $R0 > r$, 00 if $R0 = r$, 10 if $R0 < r$.
4. Condition code (CC1, CC0): 01 if $r > V$, 00 if $r = V$, 10 if $r < V$.
5. Index register must be register 3 or 3'.
6. Condition code (CC1, CC0): 00 if all selected bits are 1s, 10 if not all the selected bits are 1s.

PROGRAM STATUS WORD

PSU

7	6	5	4	3	2	1	0
S	F	II	Not Used	Not Used	SP2	SP1	SP0

S Sense
F Flag
II Interrupt Inhibit
SP2 Stack Pointer Two
SP1 Stack Pointer One
SP0 Stack Pointer Zero

PSL

7	6	5	4	3	2	1	0
CC1	CC0	IDC	RS	WC	OVF	COM	C

CC1 Condition Code One
CC0 Condition Code Zero
IDC Interdigit Carry
RS Register Bank Select
WC With/Without Carry
OVF Overflow
COM Logical/Arith. Compare
C Carry/Borrow

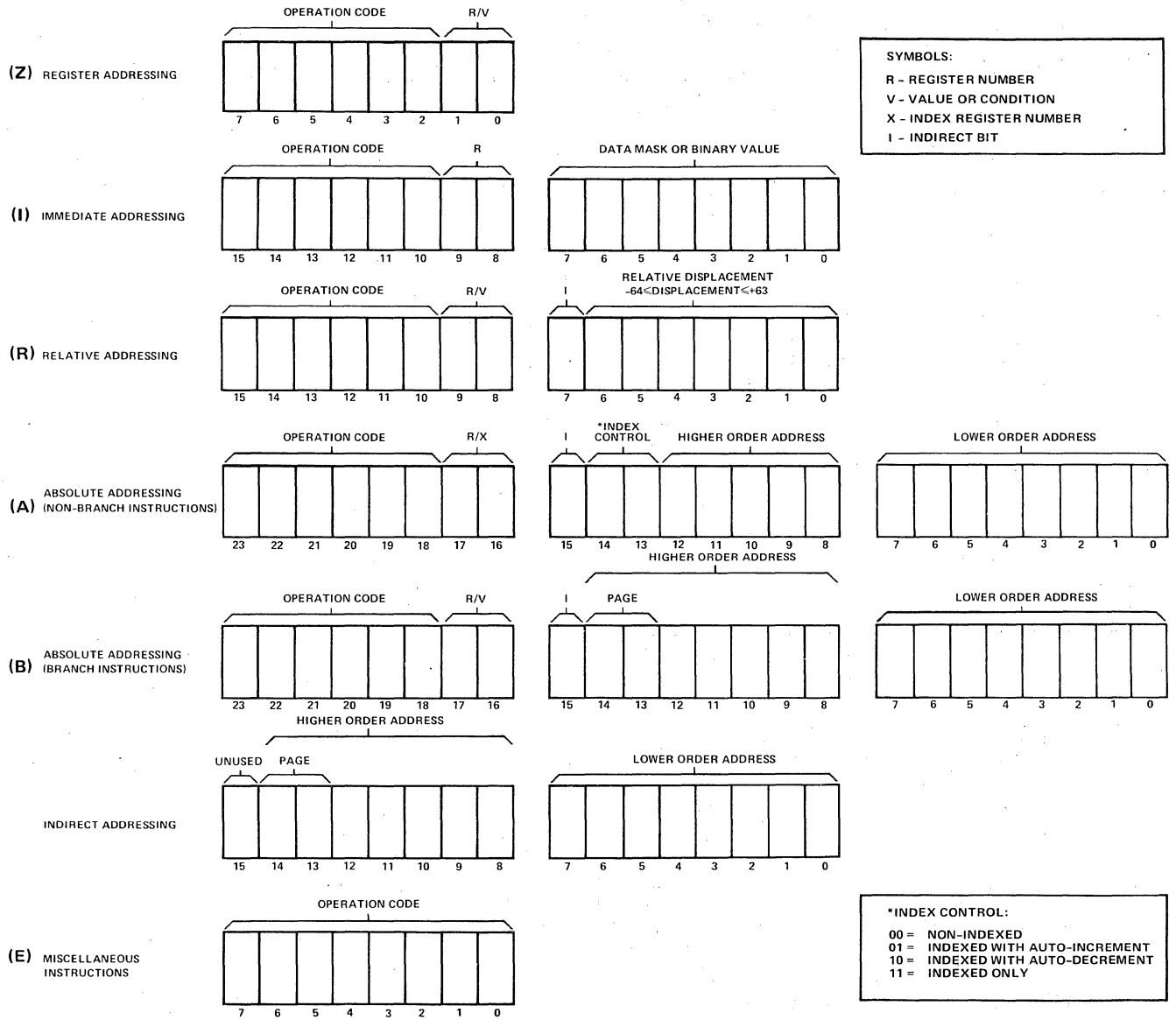


Figure 6. INSTRUCTION FORMATS

INTRODUCING THE SERIES 3000 BIPOLAR MICROPROCESSOR

The introduction of the Signetics Series 3000 Bipolar Microprocessor Chip Set has brought new levels of high performance to microprocessor applications not previously possible with MOS technology. Combining the Schottky bipolar N3001 Microprogram Control Unit (MCU) and N3002 Central Processing Element (CPE) with industry standard memory and support circuits, microinstruction cycle times of 100 nanoseconds are possible.

In the majority of cases, the choice of a bipolar microprocessor slice, as opposed to an MOS device, is based on speed or flexibility of microprogramming. Starting with these characteristics, the design of the Signetics Series 3000 Microprocessor has been optimized around the following objectives:

- Fast cycle time
- All memory and support chips are industry standard
- Cooler operation
- Lower total system cost

Futhermore, systems built with large-scale integrated circuits are much smaller and require less power than equivalent systems using medium and/or small scale integrated circuits.

The two components of the Series 3000 chip set, when combined with industry standard memory and peripheral circuits, allows the design engineer to construct high-performance processors and/or controllers with a minimum amount of auxillary logic. Features such as the multiple independent address and data buses, tri-state logic, and separate output enable lines eliminate the need for time-multiplexing of buses and associated hardware.

Each Central Processing Element represents a

complete 2-bit slice through the data processing section of a computer. Several CPE's may be connected in parallel to form a processor of any desired word length. The Microprogram Control Unit controls the sequence in which microinstructions are fetched from the microprogram memory (ROM/PROM), with these microinstructions controlling the step-by-step operation of the processor.

Each CPE contains a 2-bit slice of five independent buses. Although they can be used in a variety of ways, typical connections are:

- Input M-bus: Carries data from external memory
- Input I-bus: Carries data from input/output device
- Input K-bus: Used for microprogram mask or literal (constant) value input
- Output A-bus: Connected to CPE Memory Address Register
- Output D-bus: Connected to CPE accumulator.

As the CPE's are paralleled together, all buses, data paths, and registers are correspondingly expanded.

The microfunction input bus (F-bus) controls the internal operation of the CPE, selecting both the operands and the operation to be executed upon them. The arithmetic logic unit (ALU), controlled by the microfunction decoder, is capable of over 40 Boolean and binary operations as outlined in the FUNCTION DESCRIPTION section of the N3002 data sheet. Standard carry look-ahead outputs (X and Y) are generated by the CPE for use with industry standard devices such as the 74S182.

A typical processor configuration is shown in Figure 1. It should be remembered that in working with slice-oriented microprocessors, the final configuration may be varied to enhance speed, reduce component count, or increase data-processing capability. One method of maximizing

a processor's performance is called pipelining. To accomplish this, a group of D-type flip-flops or latches (such as the 74174 Hex D-type Flip-Flop) are connected to the microprogram memory outputs (excluding the address control field AC₀ - AC₆) to buffer the current microinstruction

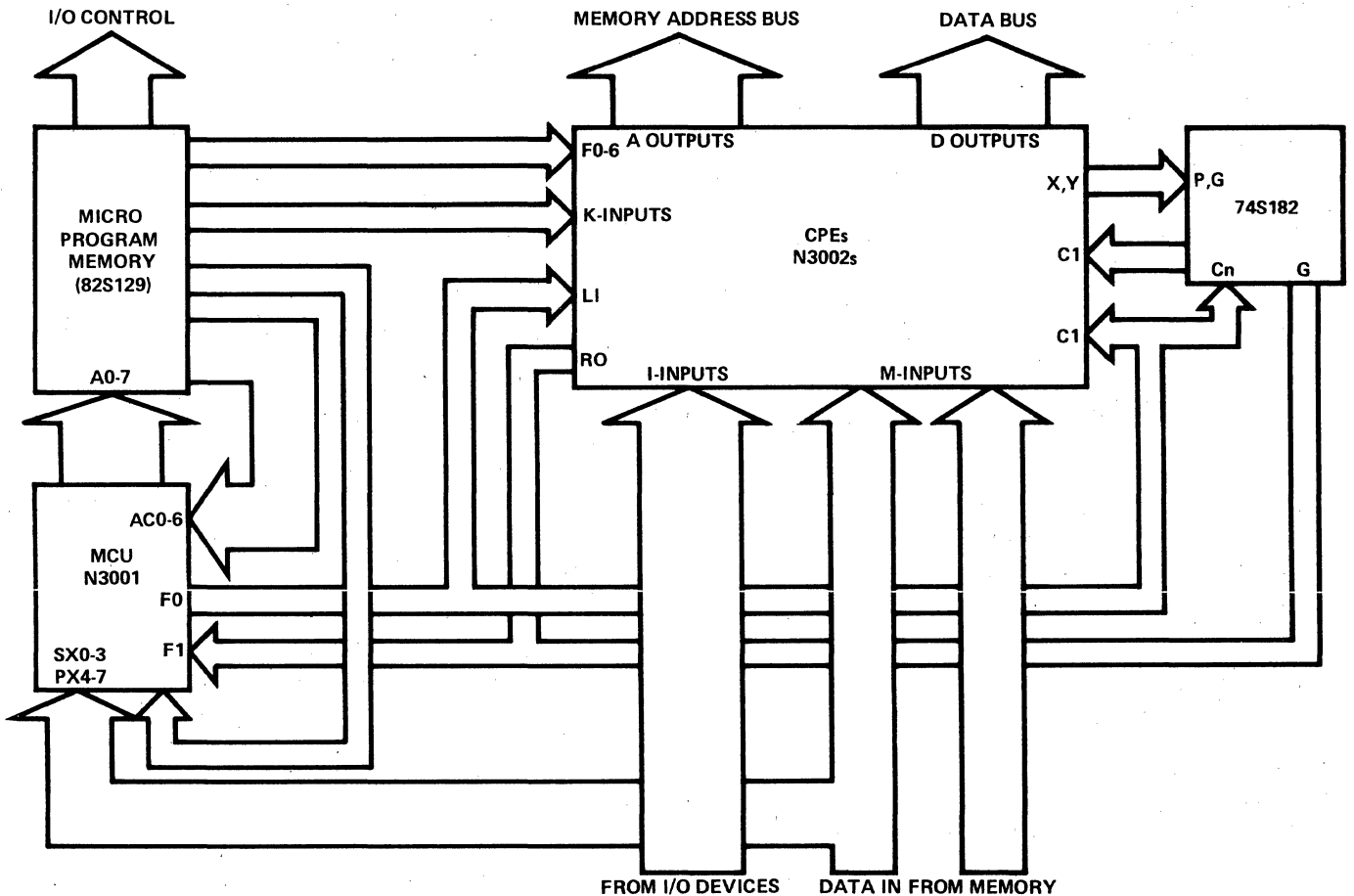


Figure 1: MICROCOMPUTER BLOCK DIAGRAM

Signetics

MICROPROCESSOR

and allow the MCU to overlap the fetch of the next instruction with the execution of the current one. The time saved in pipelining operations is the shorter of either the address set-up time to the microprogram memory (ROM/PROM) or the access time of the ROM/PROM. A convenient way of implementing pipelining is to use ROMs with on-board latches, such as the Signetics 82S115.

Figure 2 shows a typical microinstruction format using the 82S114 PROMs contained in the Signetics 3000 Microprocessor Designer's Evaluation Kit. Although this particular example is for a 48-bit word (6 PROMs), the allocation of bits for the mask (K-bus) and optional processor functions depends on the specific application of the system and the trade offs which the designer wishes to make.

In using the K-bus, it should be kept in mind that the K inputs are always ANDed with the B-multiplexer outputs into the ALU. Bit masking, frequently done in computer control systems, can be performed with the mask supplied to the K-bus directly from the microinstruction.

By placing the K-bus in either the all-one or all-zero condition (done with a single control bit in the microinstruction), the accumulator will either be selected or de-selected, respectively, in a given operation. This feature nearly doubles the amount of microfunctions in the CPE. A description of these various microfunctions can be found in the N3002 data sheet under the heading "FUNCTION DESCRIPTION" by referring to the K-bus conditions of all-ones (11) and all-zeros (00).

The MCU controls the sequence in which microinstructions are fetched from the microprogram memory (ROM/PROM). In its classical form, the MCU would use a next-address field in each microinstruction. However, the N3001 uses a modified classical approach in which the microinstruction field specifies conditional tests on the MCU bus inputs and registers. The next-address logic of the MCU also makes extensive use of a row/column addressing scheme, whereby the next address is defined by a 5-bit row address and 4-bit column address. Thus, from a particular address location, it is possible to jump unconditionally to any other location within that row or

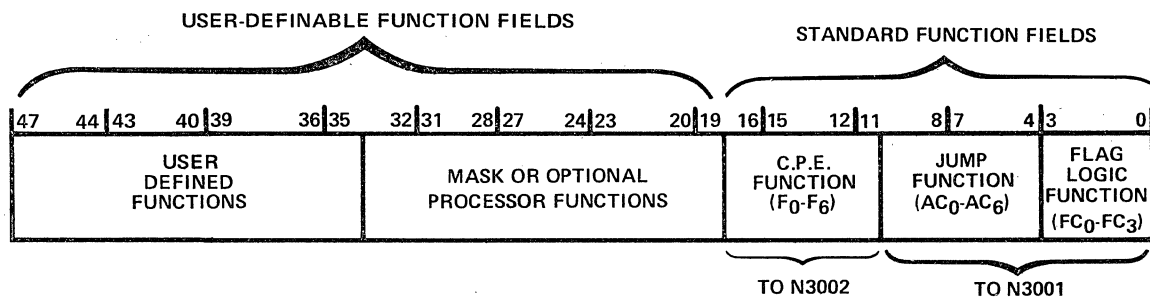


Figure 2: TYPICAL MICROINSTRUCTION FORMAT.

Note: The mask field need only be used during masking operations. At other times, it is entirely user definable.

column, or conditionally to other specified locations in one operation. Using this method, the processor functions can be executed in parallel with program branches.

As an example of this flexibility, let us assume a disk controller is being designed. As part of the sequence logic, three bits of the disk drive status word must be tested and all three must be true in order to proceed with the particular sequencing operation. In any sequencing operation using a status word for conditional branch information, there are innumerable combinations of bits which must be tested throughout the sequencing operation. Using discrete logic techniques, this would involve several levels of gating.

However, the entire operation can be done in two microinstructions. First, the mask (K-bus) field in the microinstruction format is encoded with a one for each corresponding status bit to be tested and a zero for each bit to be discarded. The status word is input via the I-bus and ANDed with the K-bus mask using the CPE microfunction operation from F-Group 2, R-Group III. Assuming we are using low-true logic (TRUE = 0 Volts), we now test the result, which is located in the accumulator AC, for all zeros using the CPE microfunction operation from F-Group 5, R-Group III. Depending on the zero/non-zero status of AC, a one or zero will be loaded into the carryout CO bit. This

bit can now be used as a condition for the next address jump calculation within the N3001 MCU. If the AC was zero (status word was true), we will jump to the next address within our controller sequence. If the AC was non-zero (status word not true), then a jump would be made back to the beginning of this two-microinstruction loop and the test sequence repeated until the status word (all three bits) is true.

Figure 3 shows a typical timing diagram for a system operating in the non-pipelined mode. Keep in mind that the maximum clock rate is dependent upon the total of propagation delay times plus required set-up times. It is at the designer's discretion to resolve the speed versus complexity trade-offs.

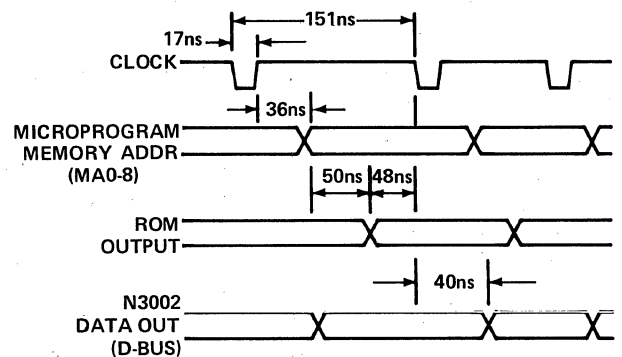


Figure 3: SYSTEM TIMING - NON-PIPELINED CONFIGURATION

BIPOLAR MICROPROCESSOR

DESCRIPTION

The N3001 MCU is one element of a bipolar microcomputer set. When used with the 3002, 74S182, ROM or PROM memory, a powerful microprogrammed computer can be implemented.

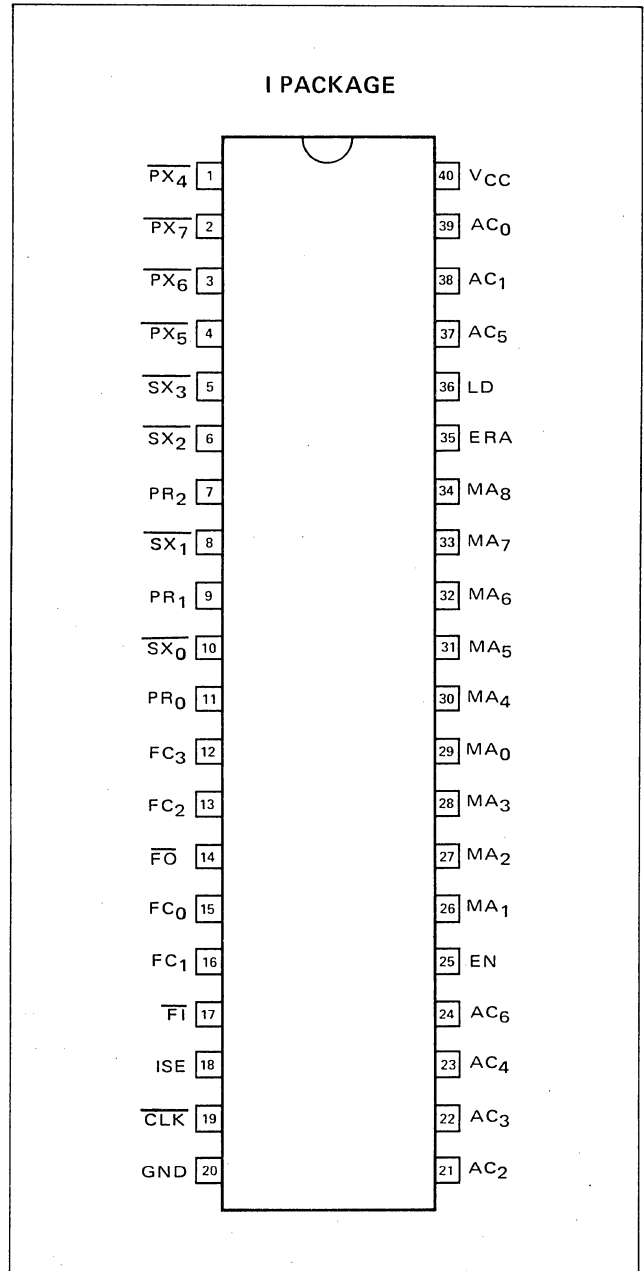
The 3001 MCU controls the fetch sequence of microinstructions from the microprogram memory. Functions performed by the 3001 include:

- Maintenance of microprogram address register
- Selection of next microinstruction address
- Decoding and testing of data supplied via several input busses
- Saving and testing of carry output data from the central processing (CP) array
- Control of carry/shift input data to the CP array
- Control of microprogram interrupts

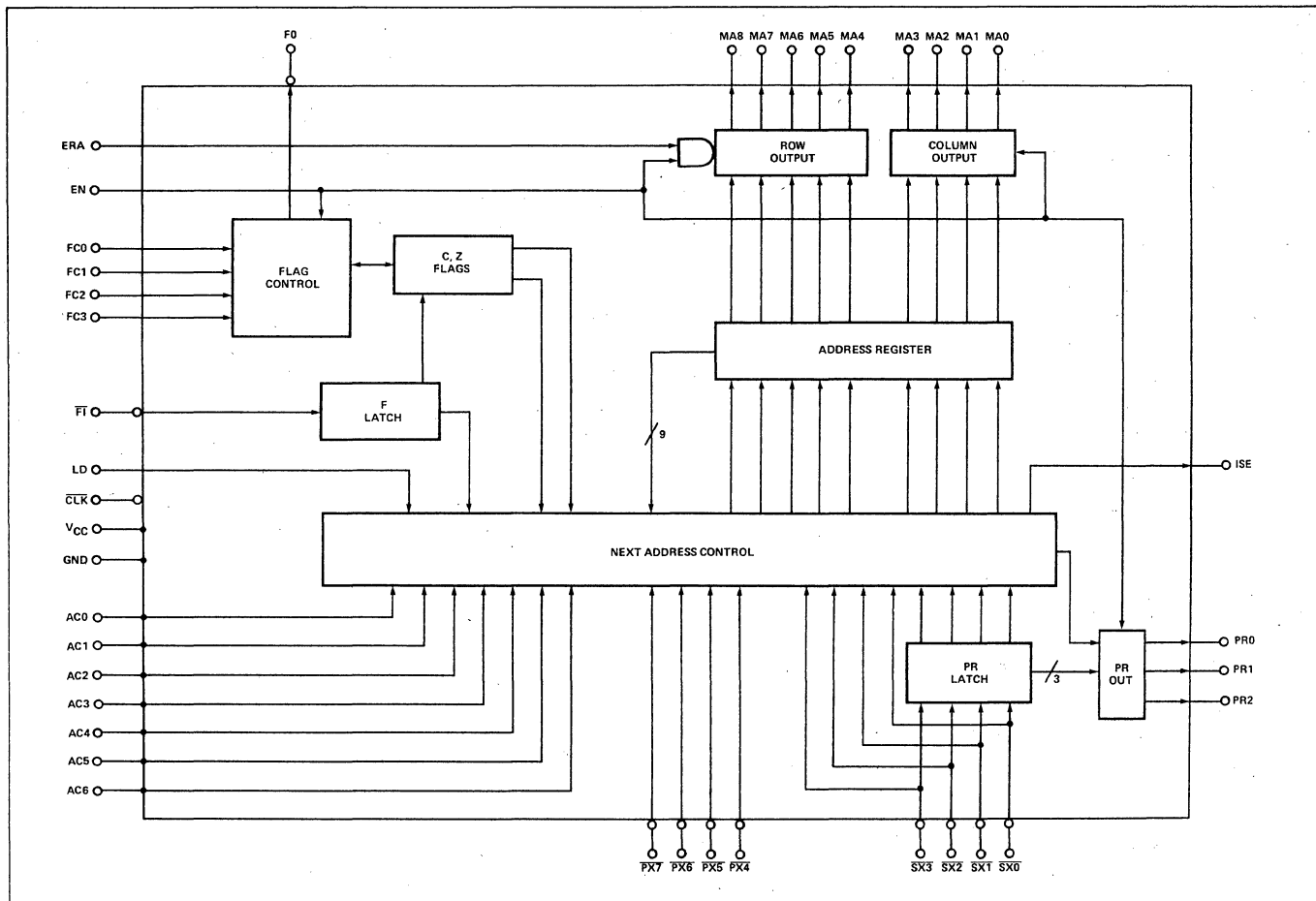
FEATURES

- SCHOTTKY TTL PROCESS
- 45ns CYCLE TIME (TYP.)
- DIRECT ADDRESSING OF STANDARD BIPOLAR PROM OR ROM
- 512 MICROINSTRUCTION ADDRESSABILITY
- ADVANCED ORGANIZATION:
 - 9-BIT MICROPROGRAM ADDRESS REGISTER AND BUS ORGANIZED TO ADDRESS MEMORY BY ROW AND COLUMN
 - 4-BIT PROGRAM LATCH
 - 2 FLAG REGISTERS
- 11 ADDRESS CONTROL FUNCTIONS:
 - 3 JUMP AND TEST LATCH FUNCTION
 - 16 WAY JUMP AND TEST INSTRUCTION
- EIGHT FLAG CONTROL FUNCTIONS:
 - 4 FLAG INPUT FUNCTIONS
 - 4 FLAG OUTPUT FUNCTIONS

PIN CONFIGURATION



N3001 BLOCK DIAGRAM



PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-4	$\overline{PX_4}-\overline{PX_7}$	Primary Instruction Bus Inputs Data on the primary instruction bus is tested by the JPX function to determine the next microprogram address.	Active LOW
5, 6, 8, 10	$\overline{SX_0}-\overline{SX_3}$	Secondary Instruction Bus Inputs Data on the secondary instruction bus is synchronously loaded into the PR-latch while the data on the PX-bus is being tested (JPX). During a subsequent cycle, the contents of the PR-latch may be tested by the JPR, JLL, or JRL functions to determine the next microprogram address.	Active LOW
7, 9, 11	PR ₀ -PR ₂	PR-Latch Outputs The PR-latch outputs (SX ₀ -SX ₂) are asynchronously enabled by the JCE function. They can be used to modify microinstructions at the outputs of the microprogram memory or to provide additional control lines.	Open Collector
12, 13, 15, 16	FC ₀ -FC ₃	Flag Logic Control Inputs The flag logic control inputs are used to cross-switch the flags (C and Z) with the flag logic input (FI) and the flag logic output (FO).	Active HIGH
14	\overline{FO}	Flag Logic Output The outputs of the flags (C and Z) are multiplexed internally to form the common flag logic output. The output may also be forced to a logical 0 or logical 1.	Active LOW Three-state
17	\overline{FI}	Flag Logic Input The flag logic input is demultiplexed internally and applied to the inputs of the flags (C and Z). Note: The flag input data is saved in the F-latch when the clock input (CLK) is low.	Active LOW

PIN DESCRIPTION (Cont'd)

PIN	SYMBOL	NAME AND FUNCTION	TYPE
18	ISE	Interrupt Strobe Enable Output The interrupt strobe enable output goes to logical 1 when one of the JZR functions are selected (see Functional Description). It can be used to provide the strobe signal required by interrupt circuits.	Active HIGH
19	$\overline{\text{CLK}}$	Clock Input	
20	GND	Ground	
21–24 37–39	AC ₀ –AC ₆	Next Address Control Function Inputs All jump functions are selected by these control lines.	Active HIGH
25	EN	Enable Input When in the HIGH state, the enable input enables the microprogram address, PR-latch and flag outputs.	
26–29	MA ₀ –MA ₃	Microprogram Column Address Outputs	Three-state
30–34	MA ₄ –MA ₈	Microprogram Row Address Outputs	Three-state
35	ERA	Enable Row Address Input When in the LOW state, the enable row address input independently disables the microprogram row address outputs. It can be used to facilitate the implementation of priority interrupt systems.	Active HIGH
36	LD	Microprogram Address Load Input When the active HIGH state, the microprogram address load input inhibits all jump functions and synchronously loads the data on the instructions busses into the microprogram register. However, it does not inhibit the operation of the PR-latch or the generation of the interrupt strobe enable.	Active HIGH
40	VCC	+5 Volt Supply	

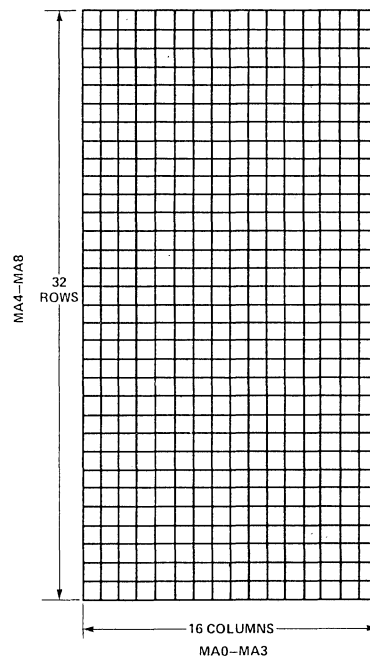
THEORY OF OPERATION

The MCU controls the sequence of microinstructions in the microprogram memory. The MCU simultaneously controls 2 flip-flops (C, Z) which are interactive with the carry-in and carry-out logic of an array of CPEs.

The functional control of the MCU provides both unconditional jumps to new memory locations and jumps which are dependent on the state of MCU flags or the state of the "PR" latch. Each instruction has a "jump set" associated with it. This "jump set" is the total group of memory locations which can be addressed by that instruction.

The MCU utilizes a two-dimensional addressing scheme in the microprogram memory. Microprogram memory is organized as 32 rows and 16 columns for a total of 512 words. Word length is variable according to application. Address is accomplished by a 9-bit address organized as a 5-bit row and 4-bit column address.

ADDRESSING ORGANIZATION



ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to +150°C
Supply Voltages	7V
All Input Voltages	+5.5V
Output Currents	100mA

NOTE:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

DC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP ¹	MAX	
V_C Input Clamp Voltage (All Input Pins)	$V_{CC} = 4.75, I_C = -5\text{mA}$		-0.8	-1.0	V
I_F Input Load Current: CLK Input EN Input All Other Inputs	$V_{CC} = 5.25\text{V}, V_F = 0.45\text{V}$		-0.075 -0.05 -0.025	-0.75 -0.50 -0.25	mA mA mA
I_R Input Leakage Current: CLK EN Input All Other Inputs	$V_{CC} = 5.25\text{V}, V_R = 5.25\text{V}$			120 80 40	μA μA μA
V_{IL} Input Low Voltage	$V_{CC} = 5.0\text{V}$			0.8	V
V_{IH} Input High Voltage		2.0			V
I_{CC} Power Supply Current	$V_{CC} = 5.25\text{V}^2$		170	240	mA
V_{OL} Output Low Voltage (All Output Pins)	$V_{CC} = 4.75\text{V}, I_{OL} = 10\text{mA}$		0.35	0.45	V
V_{OH} Output High Voltage (MA_0 - MA_8 , ISE, FO)	$V_{CC} = 4.75\text{V}, I_{OH} = -1\text{mA}$	2.4	3.0		V
I_{os} Output Short Circuit Current (MA_0 - MA_8 , ISE, FO)	$V_{CC} = 5.0\text{V}$	-15	-28	-60	mA
I_o (off) Off-State Output Current: PR_0 - PR_2 , MA_0 - MA_2 , FO MA_0 - MA_8 , FO	$V_{CC} = 5.25\text{V}, V_o = 0.45\text{V}$ $V_{CC} = 5.25\text{V}, V_o = 5.25\text{V}$			-100 -100	μA μA

NOTES:

1. Typical values are for $T_A = 25^\circ\text{C}$ and 5.0 supply voltage.
2. EN input grounded, all other inputs and outputs open.

FUNCTIONAL DESCRIPTION

The following is a description of each of the eleven address control functions. The symbols shown below are used to specify row and column addresses.

SYMBOL	MEANING
row _n	5-bit next row address where n is the decimal row address.
col _n	4-bit next column address where n is the decimal column address.

UNCONDITIONAL ADDRESS CONTROL (JUMP) FUNCTIONS

The jump functions use the current microprogram address (i.e., the contents of the microprogram address register prior to the rising edge of the clock) and several bits from the address control inputs to generate the next microprogram address.

MNEMONIC	FUNCTION DESCRIPTION
JCC	Jump in current column. AC ₀ –AC ₄ are used to select 1 of 32 row addresses in the current column, specified by MA ₀ –MA ₃ , as the next address.
JZR	Jump to zero row. AC ₀ –AC ₃ are used to select 1 of 16 column addresses in row ₀ , as the next address.
JCR	Jump in current row. AC ₀ –AC ₃ are used to select 1 of 16 addresses in the current row, specified by MA ₄ –MA ₈ , as the next address.
JCE	Jump in current column/row group and enable PR-latch outputs. AC ₀ –AC ₂ are used to select 1 of 8 row addresses in the current row group, specified by MA ₇ –MA ₈ , as the next row address. The current column is specified by MA ₀ –MA ₃ . The PR-latch outputs are asynchronously enabled.

FLAG CONDITIONAL ADDRESS CONTROL (JUMP/TEST) FUNCTIONS

The jump/test flag functions use the current microprogram address, the contents of the selected flag or latch, and several bits from the address control function to generate the next microprogram address.

MNEMONIC	FUNCTION DESCRIPTION
JFL	Jump/test F-latch. AC ₀ –AC ₃ are used to select 1 of 16 row addresses in the current row group, specified by MA ₈ , as the next row address. If the current column group, specified by MA ₃ , is col ₀ –col ₇ , the F-latch is used to select col ₂ or col ₃ as the next column address. If MA ₃ specifies column group col ₈ –col ₁₅ , the F-latch is used to select col ₁₀ or col ₁₁ as the next column address.

JCF Jump/test C-flag. AC₀–AC₂ are used to select 1 of 8 row addresses in the current row group, specified by MA₇ and MA₈, as the next row address. If the current column group specified by MA₈ is col₀–col₇, the C-flag is used to select col₂ or col₃ as the next column address. If MA₃ specifies column group col₈–col₁₅, the C-flag is used to select col₁₀ or col₁₁ as the next column address.

JZF Jump/test Z-flag. Identical to the JCF function described above, except that the Z-flag, rather than the C-flag, is used to select the next column address.

PX-BUS AND PR-LATCH CONDITIONAL ADDRESS CONTROL (JUMP/TEST) FUNCTIONS

The PX-bus jump/test function uses the data on the primary instruction bus (PX₄–PX₇), the current microprogram address, and several selection bits from the address control function to generate the next microprogram address. The PR-latch jump/test functions use the data held in the PR-latch, the current microprogram address, and several selection bits from the address control function to generate the next microprogram address.

MNEMONIC	FUNCTION DESCRIPTION
JPR	Jump/test PR-latch. AC ₀ –AC ₂ are used to select 1 of 8 row addresses in the current row group, specified by MA ₇ and MA ₈ , as the next row address. The four PR-latch bits are used to select 1 of 16 possible column addresses as the next column address.
JLL	Jump/test leftmost PR-latch bits. AC ₀ –AC ₂ are used to select 1 of 8 row addresses in the current row group, specified by MA ₇ and MA ₈ , as the next row address. PR ₂ and PR ₃ are used to select 1 of 4 column address in col ₄ through col ₇ as the next column address.
JRL	Jump/test rightmost PR-latch bits. AC ₀ and AC ₁ are used to select 1 of 4 high-order row addresses in the current row group, specified by MA ₇ and MA ₈ , as the next row address. PR ₀ and PR ₁ are used to select 1 of 4 possible column addresses in col ₁₂ through col ₁₅ as the next column address.
JPX	Jump/test PX-bus and load PR-latch. AC ₀ and AC ₁ are used to select 1 of 4 row addresses in the current row group, specified by MA ₆ –MA ₈ , as the next row address. PX ₄ –PX ₇ are used to select 1 of 16 possible column addresses as the next column address. SX ₀ –SX ₃ data is locked in the PR-latch at the rising edge of the clock.

FLAG CONTROL FUNCTIONS

The flag control functions of the MCU are selected by the four input lines designated FC₀–FC₃. Function code formats are given in "Flag Control Function summary".

The following is a detailed description of each of the eight flag control functions.

FLAG INPUT CONTROL FUNCTIONS

The flag input control functions select which flag or flags will be set to the current value of the flag input (FI) line. Data on FI is stored in the F-latch when the clock is low. The content of the F-latch is loaded into the C and/or Z flag on the rising edge of the clock.

MNEMONIC FUNCTION DESCRIPTION

- SCZ Set C-flag and Z-flag to FI. The C-flag and the Z-flag are both set to the value of FI.
- STZ Set Z-flag to FI. The Z-flag is set to the value of FI. The C-flag is unaffected.
- STC Set C-flag to FI. The C-flag is set to the value of FI. The Z-flag is unaffected.
- HCZ Hold C-flag and Z-flag. The values in the C-flag and Z-flag are unaffected.

FLAG OUTPUT CONTROL FUNCTIONS

The flag output control functions select the value to which the flag output (FO) line will be forced.

MNEMONIC FUNCTION DESCRIPTION

- FFO Force FO to 0. FO is forced to the value of logical 0.
- FFC Force FO to C. FO is forced to the value of the C-flag.
- FFZ Force FO to Z. FO is forced to the value of the Z-flag.
- FF1 Force FO to 1. FO is forced to the value of logical 1.

STROBE FUNCTIONS

The load function of the MCU is controlled by the input line designated LD. If the LD line is active HIGH at the rising edge of the clock, the data on the primary and secondary instruction busses, PX₄–PX₇ and SX₀–SX₃, is loaded into the microprogram address register. PX₄–PX₇ are loaded into MA₀–MA₃ and SX₀–SX₃ are loaded into MA₄–MA₇. The high-order bit of the microprogram address register MA₈ is set to a logical 0. The bits from the primary instruction bus select 1 of 16 possible column addresses. Likewise, the bits from the secondary instruction bus select 1 of the first 16 row addresses.

The MCU generates an interrupt strobe enable on the output line designated ISE. The line is placed in the active high state whenever a JZR to col₁₅ is selected as the address control function. Generally, the start of a macro-instruction fetch sequence is situated at row₀ and col₁₅ so the interrupt control may be enabled at the beginning of

ADDRESS CONTROL FUNCTION SUMMARY

MNEMONIC	DESCRIPTION	FUNCTION								NEXT ROW				NEXT COL			
		AC ₆	5	4	3	2	1	0	MA ₈	7	6	5	4	MA ₃	2	1	0
JCC	Jump in current column	0	0	d ₄	d ₃	d ₂	d ₁	d ₀	d ₄	d ₃	d ₂	d ₁	d ₀	m ₃	m ₂	m ₁	m ₀
JZR	Jump to zero row	0	1	0	d ₃	d ₂	d ₁	d ₀	0	0	0	0	0	d ₃	d ₂	d ₁	d ₀
JCR	Jump in current row	0	1	1	d ₃	d ₂	d ₁	d ₀	m ₈	m ₇	m ₆	m ₅	m ₄	d ₃	d ₂	d ₁	d ₀
JCE	Jump in column/enable	1	1	1	0	d ₂	d ₁	d ₀	m ₈	m ₇	d ₂	d ₁	d ₀	m ₃	m ₂	m ₁	m ₀
JFL	Jump/test F-latch	1	0	0	d ₃	d ₂	d ₁	d ₀	m ₈	d ₃	d ₂	d ₁	d ₀	m ₃	0	1	f
JCF	Jump/test C-flag	1	0	1	0	d ₂	d ₁	d ₀	m ₈	m ₇	d ₂	d ₁	d ₀	m ₃	0	1	c
JZF	Jump/test Z-flag	1	0	1	1	d ₂	d ₁	d ₀	m ₈	m ₇	d ₂	d ₁	d ₀	m ₃	0	1	z
JPR	Jump/test PR-latch	1	1	0	0	d ₂	d ₁	d ₀	m ₈	m ₇	d ₂	d ₁	d ₀	p ₃	p ₂	p ₁	p ₀
JLL	Jump/test left PR bits	1	1	0	1	d ₂	d ₁	d ₀	m ₈	m ₇	d ₂	d ₁	d ₀	0	1	p ₃	p ₂
JRL	Jump/test right PR bits	1	1	1	1	1	d ₁	d ₀	m ₈	m ₇	1	d ₁	d ₀	1	1	p ₁	p ₀
JPX	Jump/test PX-bus	1	1	1	1	0	d ₁	d ₀	m ₈	m ₇	m ₆	d ₁	d ₀	x ₇	x ₆	x ₅	x ₄

NOTE:

- d_n = Data on address control line n
- m_n = Data in microprogram address register bit n
- p_n = Data in PR-latch bit n
- x_n = Data on PX-bus line n (active LOW)
- f, c, z = Contents of F-latch, C-flag, or Z-flag, respectively

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STROBE FUNCTIONS Cont'd.

the fetch/execute cycle. The interrupt control responds to the interrupt by pulling the enable row address (ERA) input line low to override the selected next row address from the MCU. Then by gating an alternative next row address on to the row address lines of the microprogram memory, the microprogram may be forced to enter an interrupt handling routine. The alternative row address placed on the microprogram memory address lines does not alter the contents of the microprogram address register. Therefore, subsequent jump functions will utilize the row address in the register, and not the alternative row address, to determine the next microprogram address.

Note, the load function always overrides the address control function on AC₀–AC₆. It does not, however, override the latch enable or load sub-functions of the JCE or JPX instruction, respectively. In addition, it does not inhibit the interrupt strobe enable or any of the flag control functions.

FLAG CONTROL FUNCTION SUMMARY

TYPE	MNEMONIC	DESCRIPTION	FC ₁	0
Flag Input	SCZ	Set C-flag and Z-flag to f	0	0
	STZ	Set Z-flag to f	0	1
	STC	Set C-flag to f	1	0
	HCZ	Hold C-flag and Z-flag	1	1

TYPE	MNEMONIC	DESCRIPTION	FC ₃	2
Flag Output	FF0	Force FO to 0	0	0
	FFC	Force FO to C-flag	0	1
	FFZ	Force FO to Z-flag	1	0
	FF1	Force FO to 1	1	1

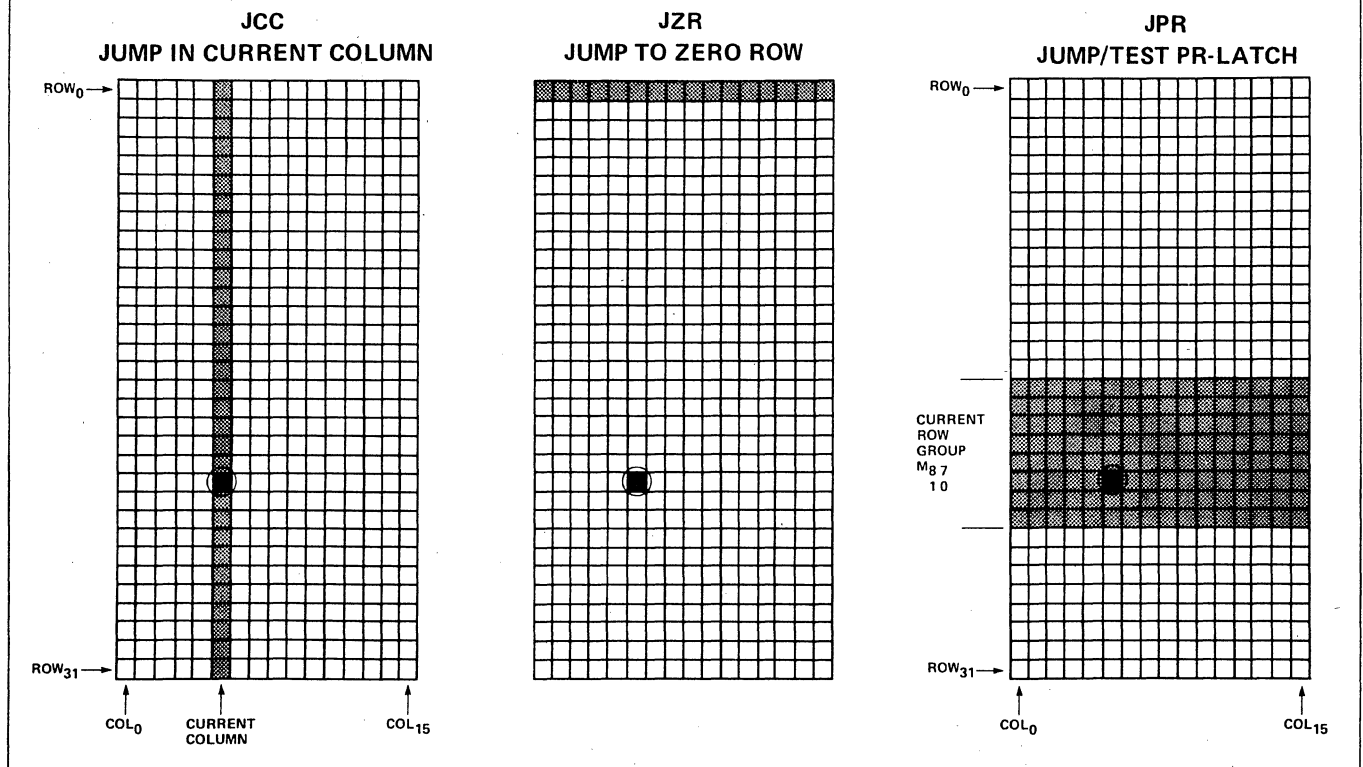
LOAD FUNCTION	NEXT ROW	NEXT COL
LD	MA ₈ 7 6 5 4 MA ₃	2 1 0
0	See address control function summary	
1	0 x ₃ x ₂ x ₁ x ₀	x ₇ x ₆ x ₅ x ₄

NOTE:
 f = Contents of the F-latch
 x_n = Data on PX- or SX-bus line n (active LOW)

JUMP SET DIAGRAMS

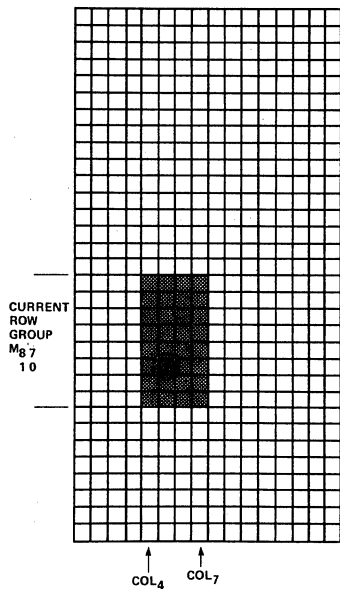
The following ten diagrams illustrate the jump set for each of the eleven jump and jump/test functions of the MCU. Location 341 indicated by the circled square, represents one current row (row₂₁) and current column (col₅)

address. The dark boxes indicate the microprogram locations that may be selected by the particular function as the next address.

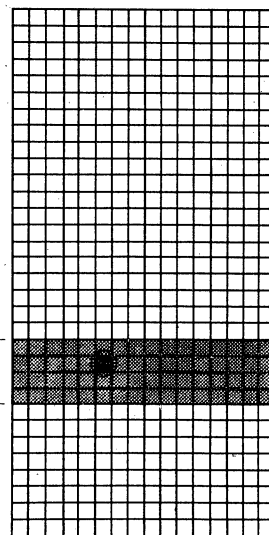


JUMP SET DIAGRAMS Cont'd.

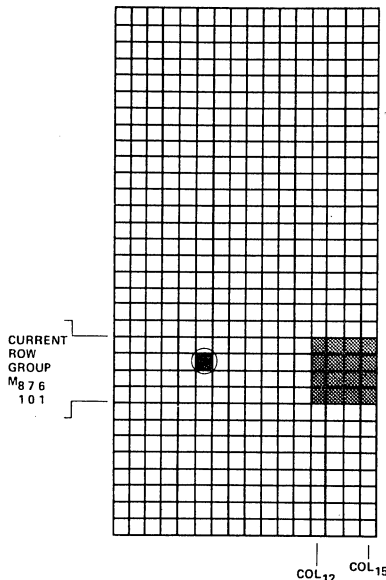
JLL
JUMP/TEST LEFT LATCH



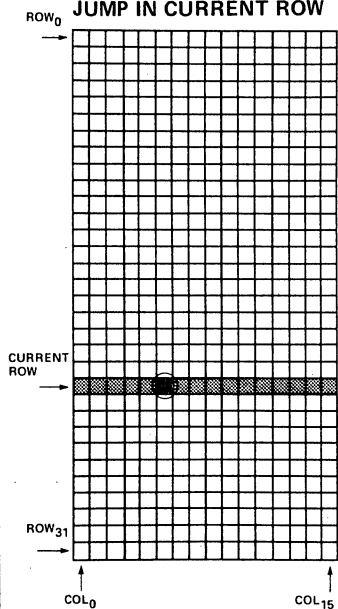
JPX
JUMP/TEST PX-BUS



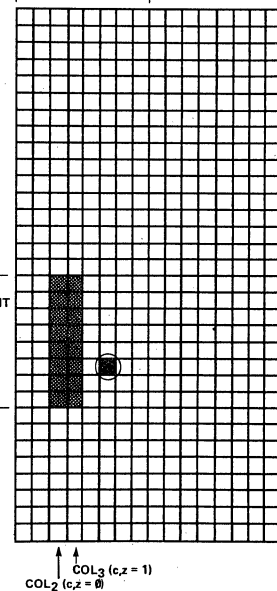
JRL
JUMP/TEST RIGHT LATCH



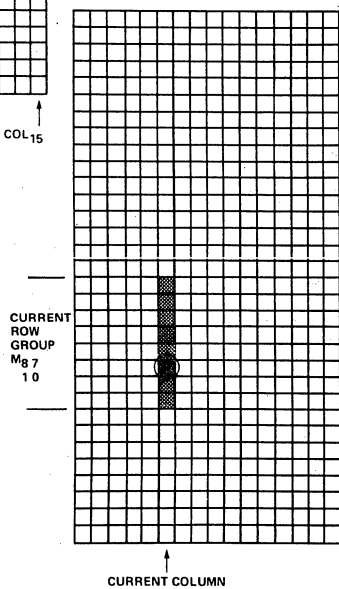
JCR
JUMP IN CURRENT ROW



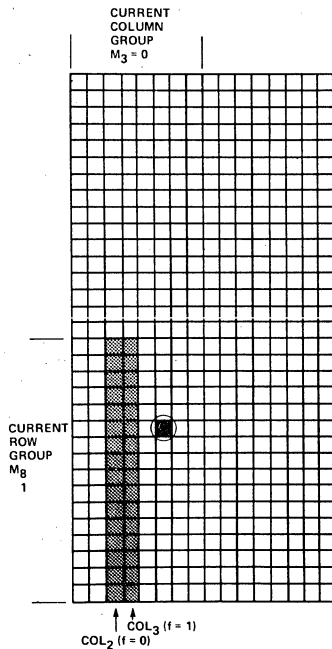
JCF, JZF
JUMP/TEST C-FLAG
JUMP/TEST Z-FLAG



JCE
JUMP COLUMN/ENABLE



JFL
JUMP/TEST F-LATCH



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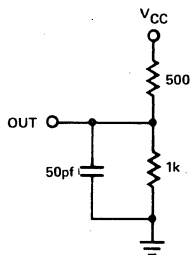
AC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0\text{V} + 5\%$

PARAMETER	LIMITS			UNIT
	MIN	TYP ¹	MAX	
t_{CY} Cycle Time	60	45		ns
t_{WP} Clock Pulse Width	17	10		ns
Control and Data Input Set-Up Times:				
t_{SF} LD, AC ₀ –AC ₆	7	0		ns
t_{SK} FC ₀ , FC ₁	7	0		ns
t_{SX} SX ₀ –SX ₃ , PX ₄ –PX ₇	28	20		ns
t_{SI} FI	12	0		ns
Control and Data Input Hold Times:				
t_{HF} LD, AC ₀ –AC ₆	4	0		ns
t_{HK} FC ₀ , FC ₁	4	0		ns
t_{HX} SX ₀ –SX ₃ , PX ₄ –PX ₇	16	0		ns
t_{HI} FI	16	6		ns
t_{CO} Propagation Delay from Clock Input (CLK) to Outputs (MA ₀ –MA ₈ , FO)		24	36	ns
t_{KO} Propagation Delay from Control Inputs FC ₂ and FC ₃ to Flag Out (FO)		13	24	ns
t_{FO} Propagation Delay from Control Inputs AC ₀ –AC ₆ to Latch Outputs (PR ₀ –PR ₂)		21	32	ns
t_{EO} Propagation Delay from Enable Inputs EN and ERA to Outputs (MA ₀ –MA ₈ , FO, PR ₀ –PR ₂)		17	26	ns
t_{FI} Propagation Delay from Control Inputs AC ₀ –AC ₆ to Interrupt Strobe Enable Output (ISE)		19	32	ns

NOTE:
1. Typical values are for $T_A = 25^\circ\text{C}$ and 5.0 supply voltage.

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

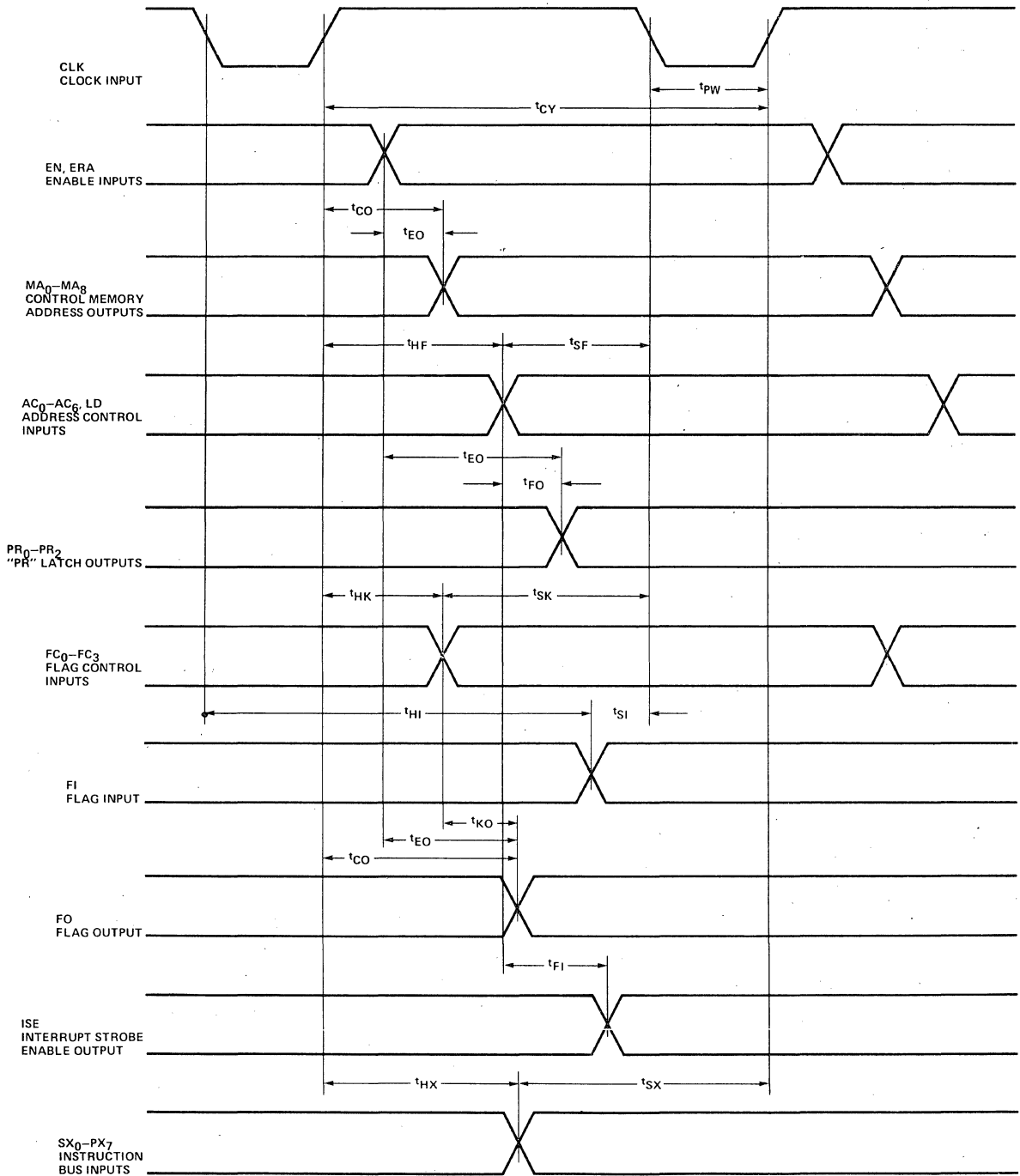


NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

TEST CONDITIONS

Input pulse amplitude of 2.5 volts.
Input rise and fall times of 5ns between 1 volt and 2 volts.
Output load of 10mA and 50pF.
Speed measurements are taken at the 1.5 volt level.

VOLTAGE WAVEFORMS



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BIPOLAR MICROPROCESSOR

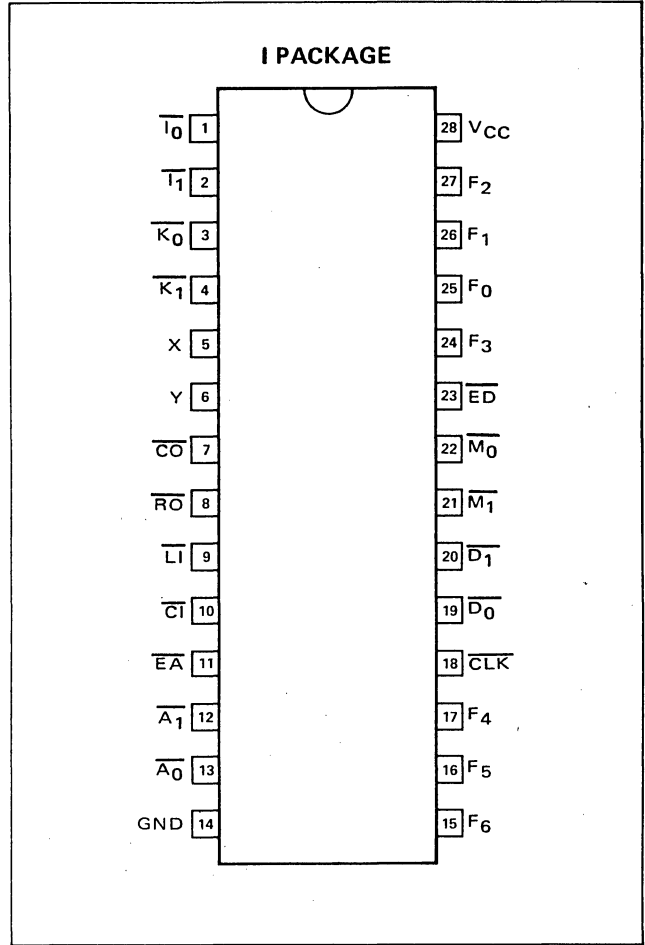
DESCRIPTION

The N3002 Central Processing Element (CPE) is one part of a bipolar microcomputer set. The N3002 is organized as a 2-bit slice and performs the logical and arithmetic functions required by micro-instructions. A system with any number of bits in a data word can be implemented by using multiple N3002s, the N3001 microcomputer control unit, the N74S182 carry look-ahead unit and ROM or PROM memory.

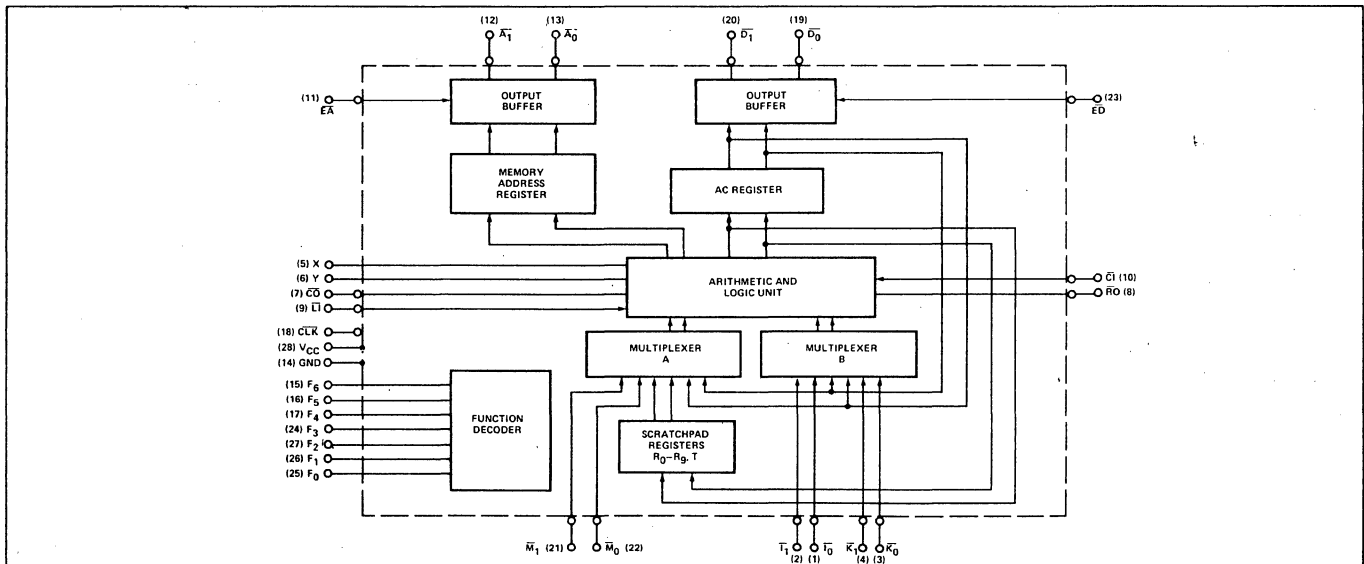
FEATURES

- 45ns CYCLE TIME (TYP.)
- EASY EXPANSION TO MULTIPLE OF 2 BITS
- 11 GENERAL PURPOSE REGISTERS
- FULL FUNCTION ACCUMULATOR
- USEFUL FUNCTIONS INCLUDE:
 - 2's COMPLEMENT ARITHMETIC
 - LOGICAL AND, OR, NOT, EXCLUSIVE-NOR
 - INCREMENT, DECREMENT
 - SHIFT LEFT/SHIFT RIGHT
 - BIT TESTING AND ZERO DETECTION
 - CARRY LOOK-AHEAD GENERATION
 - MASKING VIA K-BUS
 - CONDITIONED CLOCKING ALLOWING NON-DESTRUCTIVE TESTING OF DATA IN ACCUMULATOR AND SCRATCHPAD
- 3 INPUT BUSES
- 2 OUTPUT BUSES
- CONTROL BUS

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1, 2	$\overline{I_0}-\overline{I_1}$	External Bus Inputs The external bus inputs provide a separate input port for external input devices.	Active LOW
3, 4	$\overline{K_0}-\overline{K_1}$	Mask Bus Inputs The mask bus inputs provide a separate input port for the microprogram memory, to allow mask or constant entry.	Active LOW
5, 6	X, Y	Standard Carry Look-Ahead Cascade Outputs The cascade outputs allow high speed arithmetic operations to be performed when they are used in conjunction with the 74S182 Look-Ahead Carry Generator.	Active HIGH
7	\overline{CO}	Ripple Carry Output The ripple carry output is only disabled during shift right operations.	Active LOW Three-state
8	\overline{RO}	Shift Right Output The shift right output is only enabled during shift right operations.	Active LOW Three-state
9	\overline{LI}	Shift Right Input	Active LOW
10	\overline{CI}	Carry Input	Active LOW
11	\overline{EA}	Memory Address Enable Input When in the LOW state, the memory address enable input enables the memory address outputs (A_0-A_1).	Active LOW
12-13	$\overline{A_0}-\overline{A_1}$	Memory Address Bus Outputs The memory address bus outputs are the buffered outputs of the memory address register (MAR).	Active LOW Three-state
14	GND	Ground	
15-17, 24-27	F_0-F_6	Micro-Function Bus Inputs The micro-function bus inputs control ALU function and register selection.	Active-HIGH
18	CLK	Clock Input	
19-20	$\overline{D_0}-\overline{D_1}$	Memory Data Bus Outputs The memory data bus outputs are the buffered outputs of the full function accumulator register (AC).	Active LOW Three-state
21-22	$\overline{M_0}-\overline{M_1}$	Memory Data Bus Inputs The memory data bus inputs provide a separate input port for memory data.	Active LOW
23	\overline{ED}	Memory Data Enable Input When in the LOW state, the memory data enable input enables the memory data outputs (D_0-D_1).	Active LOW
28	V _{CC}	+5 Volt Supply	

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MICROPROCESSOR

SYSTEM DESCRIPTION

1. MICROFUNCTION DECODER AND K-BUS

Basic microfunctions are controlled by a 7-bit bus (F_0-F_6) which is organized into two groups. The higher 3 bits (F_4-F_6) are designated as F-Group and the lower 4 bits (F_0-F_3)

are designated as the R-Group. The F-Group specifies the type of operation to be performed and the R-Group specifies the registers involved.

SYSTEM DESCRIPTION (Continued)

The F-Bus instructs the microfunction decoder to:

- Select ALU functions to be performed
- Generate scratchpad register address
- Control A and B multiplexer

The resulting microfunction action can be:

- Data transfer
- Shift operations
- Increment and decrement
- Initialize stack
- Test for zero conditions
- 2's complement addition and subtraction
- Bit masking
- Maintain program counter

2. A AND B MULTIPLEXERS

A and B multiplexers select the proper two operands to the ALU.

A multiplexer selects inputs from one of the following:

- M-bus (data from main memory)
- Scratchpad registers
- Accumulator

B multiplexer selects inputs from one of the following:

- I-bus (data from external I/O devices)
- Accumulator
- K-bus (literal or masking information from micro-program memory)

3. SCRATCHPAD REGISTERS

- Contains 11 registers (R₀—R₉, T)
- Scratchpad register outputs are multiplexed to the ALU via the A multiplexer
- Used to store intermediate results from arithmetic/logic operations
- Can be used as program counter

4. ARITHMETIC/LOGIC UNIT (ALU)

The ALU performs the arithmetic and logic operations of the CPE.

Arithmetic operations are:

- 2's complement addition
- Incrementing
- Decrementing
- Shift left
- Shift right

Logical operations are:

- Transfer
- AND
- Inclusive-OR
- Exclusive-NOR
- Logic complement

ALU operation results are then stored in the accumulator and/or scratchpad registers. For easy expansion to larger arrays, carry look-ahead outputs (X and Y) and cascading shift inputs (LI, RO) are provided.

5. ACCUMULATOR

- Stores results from ALU operations
- The output of accumulator is multiplexed into ALU via the A and B multiplexer as one of the operands

6. INPUT BUSES

M-bus: Data bus from main memory

- Accepts 2 bits of data from main memory into CPE
- Is multiplexed into the ALU via the A multiplexer

I-bus: Data bus from input/output devices

- Accepts 2 bits of data from external input/output devices into CPE
- Is multiplexed into the ALU via the B multiplexer

K-bus: A special feature of the N3002 CPE

- During arithmetic operations, the K-bus can be used to mask portions of the field being operated on
- Select or remove accumulator from operation by placing K-bus in all "1" or all "0" state respectively
- During non-arithmetic operation, the carry circuit can be used in conjunction with the K-bus for word-wise-OR operation for bit testing
- Supply literal or constant data to CPE

7. OUTPUT BUSES

A-bus and Memory Address Register

- Main memory address is stored in the memory address register (MAR)
- Main memory is addressed via the A-bus
- MAR and A-bus may also be used to generate device address when executing I/O instructions
- A-bus has Tri-State outputs

D-bus: Data bus from CPE to main memory or to I/O devices

- Sends buffered accumulator outputs to main memory or the external I/O devices
- D-bus has Tri-State outputs

FUNCTION DESCRIPTION

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION	
0	I	XX	—	$R_n + (AC \wedge K) + CI \rightarrow R_n, AC$	Logically AND AC with the K-bus. Add the result to R_n and carry input (CI). Deposit the sum in AC and R_n .	
			00	ILR	$R_n + CI \rightarrow R_n, AC$	Conditionally increment R_n and load the result in AC. Used to load AC from R_n or to increment R_n and load a copy of the result in AC.
			11	ALR	$AC + R_n + CI \rightarrow R_n, AC$	Add AC and CI to R_n and load the result in AC. Used to add AC to a register. If R_n is AC, then AC is shifted left one bit position.
0	II	XX	—	$M + (AC \wedge K) + CI \rightarrow AT$	Logically AND AC with the K-bus. Add the result to CI and the M-bus. Deposit the sum in AC or T.	
			00	ACM	$M + CI \rightarrow AT$	Add CI to M-bus. Load the result in AC or T, as specified. Used to load memory data in the specified register, or to load incremented memory data in the specified register.
			11	AMA	$M + AC + CI \rightarrow AT$	Add the M-bus to AC and CI, and load the result in AC or T, as specified. Used to add memory data or incremented memory data to AC and store the sum in the specified register.
0	III	XX	—	$AT_L \wedge (I_L \wedge K_L) \rightarrow RO$ $LI \vee [(I_H \wedge K_H) \wedge AT_H] \rightarrow AT_H$ $[AT_L \wedge (I_L \wedge K_L)] \vee [AT_H \vee (I_H \wedge K_H)] \rightarrow AT_L$	None	
			00	SRA	$AT_L \rightarrow RO \quad AT_H \rightarrow AT_L \quad LI \rightarrow AT_H$	Shift AC or T, as specified, right one bit position. Place the previous low order bit value on RO and fill the high order bit from the data on LI. Used to shift or rotate AC or T right one bit.
1	I	XX	—	$K \vee R_n \rightarrow MAR$ $R_n + K + CI \rightarrow R_n$	Logically OR R_n with the K-bus. Deposit the result in MAR. Add the K-bus to R_n and CI. Deposit the result in R_n .	
			00	LMI	$R_n \rightarrow MAR \quad R_n + CI \rightarrow R_n$	Load MAR from R_n . Conditionally increment R_n . Used to maintain a macro-instruction program counter.
			11	DSM	$11 \rightarrow MAR \quad R_n - 1 + CI \rightarrow R_n$	Set MAR to all one's. Conditionally decrement R_n by one. Used to force MAR to its highest address and to decrement R_n .

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION	
1	II	XX	—	$K \vee M \rightarrow MAR$ $M + K + CI \rightarrow AT$	Logically OR the M-bus with the K-bus. Deposit the result in MAR. Add the K-bus to the M-bus and CI. Deposit the sum in AC or T.	
			00	LMM	$M \rightarrow MAR \quad M + CI \rightarrow AT$	Load MAR from the M-bus. Add CI to the M-bus. Deposit the result in AC or T. Used to load the address register with memory data for macro-instructions using indirect addressing.
			11	LDM	$11 \rightarrow MAR$ $M - 1 + CI \rightarrow AT$	Set MAR to all ones. Subtract one from the M-bus. Add CI to the difference and deposit the result in AC or T, as specified. Used to load decremented memory data in AC or T.
1	III	XX	—	$(\overline{AT} \vee K) + (AT \wedge K) + CI \rightarrow AT$	Logically OR the K-bus with the complement of AC or T, as specified. Add the result to the logical AND of specified register with the K-bus. Add the sum to CI. Deposit the result in the specified register.	
			00	CIA	$\overline{AT} + CI \rightarrow AT$	Add CI to the complement of AC or T, as specified. Deposit the result in the specified register. Used to form the 1's or 2's complement of AC or T.
			11	DCA	$AT - 1 + CI \rightarrow AT$	Subtract one from AC or T, as specified. Add CI to the difference and deposit the sum in the specified register. Used to decrement AC or T.
2	I	XX	—	$(AC \wedge K) - 1 + CI \rightarrow R_n$ (See Note 1)	Logically AND the K-bus with AC. Subtract one from the result and add the difference to CI. Deposit the sum in R_n .	
			00	CSR	$CI - 1 \rightarrow R_n$ (See Note 1)	Subtract one from CI and deposit the difference in R_n . Used to conditionally clear or set R_n to all 0's or 1's, respectively.
			11	SDR	$AC - 1 + CI \rightarrow R_n$ (See Note 1)	Subtract one from AC and add the difference to CI. Deposit the sum in R_n . Used to store AC in R_n or to store the decremented value of AC in R_n .
2	II	XX	—	$(AC \wedge K) - 1 + CI \rightarrow AT$ (See Note 1)	Logically AND the K-bus with AC. Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.	
			00	CSA	$CI - 1 \rightarrow AT$ (See Note 1)	Subtract one from CI and deposit the difference in AC or T. Used to conditionally clear or set AC or T.
			11	SDA	$AC - 1 + CI \rightarrow AT$ (See Note 1)	Subtract one from AC and add the difference to CI. Deposit the sum in AC or T. Used to store AC in T, or decrement AC, or store the decremented value of AC in T.

FUNCTION DESCRIPTION (CONT'D)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
2	III	XX	—	$(I \wedge K) - 1 + CI \rightarrow AT$ (See Note 1)	Logically AND the data of the K-bus with the data on the I-bus. Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.
		OO	CSA	$CI - 1 \rightarrow AT$	Subtract one from CI and deposit the difference in AC or T. Used to conditionally clear or set AC or T.
		11	LDI	$I - 1 + CI \rightarrow AT$	Subtract one from the data on the I-bus and add the difference to CI. Deposit the sum in AC or T, as specified. Used to load input bus data or decremented input bus data in the specified register.
3	I	XX	—	$R_n + (AC \wedge K) + CI \rightarrow R_n$	Logically AND AC with the K-bus. Add R_n and CI to the result. Deposit the sum in R_n .
		OO	INR	$R_n + CI \rightarrow R_n$	Add CI to R_n and deposit the sum in R_n . Used to increment R_n .
		11	ADR	$AC + R_n + CI \rightarrow R_n$	Add AC to R_n . Add the result to CI and deposit the sum in R_n . Used to add the accumulator to a register or to add the incremented value of the accumulator to a register.
3	II	XX	—	$M + (AC \wedge K) + CI \rightarrow AT$	Logically AND AC with the K-bus. Add the result to CI and the M-bus. Deposit the sum in AC or T.
		OO	ACM	$M + CI \rightarrow AT$	Add CI to M-bus. Load the result in AC or T, as specified. Used to load memory data in the specified register, or to load incremented memory data in the specified register.
		11	AMA	$M + AC + CI \rightarrow AT$	Add the M-bus to AC and CI, and load the result in AC or T, as specified. Used to add memory data or incremented memory data to AC and store the sum in the specified register.
3	III	XX	—	$AT + (I \wedge K) + CI \rightarrow AT$	Logically AND the K-bus with the I-bus. Add CI and the contents of AC or T, as specified, to the result. Deposit the sum in the specified register.
		OO	INA	$AT + CI \rightarrow AT$	Conditionally increment AC or T. Used to increment AC or T.
		11	AIA	$I + AT + CI \rightarrow AT$	Add the I-bus to AC or T. Add CI to the result and deposit the sum in the specified register. Used to add input data or incremented input data to the specified register.

FUNCTION TRUTH TABLE

FUNCTION GROUP	F ₆	F ₅	F ₄	
0	0	0	0	0
1	0	0	0	1
2	0	1	0	0
3	0	1	1	1
4	1	0	0	0
5	1	0	0	1
6	1	1	0	0
7	1	1	1	1

REGISTER GROUP	REGISTER	F ₃	F ₂	F ₁	F ₀
I	R ₀	0	0	0	0
	R ₁	0	0	0	1
	R ₂	0	0	1	0
	R ₃	0	0	1	1
	R ₄	0	1	0	0
	R ₅	0	1	0	1
	R ₆	0	1	1	0
	R ₇	0	1	1	1
	R ₈	1	0	0	0
	R ₉	1	0	0	1
T	1	1	0	0	
AC	1	1	0	1	
II	T	1	0	1	0
	AC	1	0	1	1
III	T	1	1	1	0
	AC	1	1	1	1

SYMBOL	MEANING
I, K, M	Data on the I, K, and M busses, respectively
CI, LI	Data on the carry input and left input, respectively
CO, RO	Data on the carry output and right output, respectively
R_n	Contents of register n including T and AC (R-Group I)
AC	Contents of the accumulator
AT	Contents of AC or T, as specified
MAR	Contents of the memory address register
L, H	As subscripts, designate low and high order bit, respectively
+	2's complement addition
-	2's complement subtraction
\wedge	Logical AND
\vee	Logical OR
\oplus	Exclusive-NOR
\rightarrow	Deposit into

NOTE:
1. 2's complement arithmetic adds 111 . . . 11 to perform subtraction of 000 . . . 01.

FUNCTION DESCRIPTION (CONT'D)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
4	I	XX	—	$CI \vee (R_n \wedge AC \wedge K) \rightarrow CO$ $R_n \wedge (AC \wedge K) \rightarrow R_n$	Logically AND the K-bus with AC. Logically AND the result with the contents of R_n . Deposit the final result in R_n . Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on the carry output (CO) line.
			00 CLR	$CI \rightarrow CO$ $0 \rightarrow R_n$	Clear R_n to all 0's. Force CO to CI. Used to clear a register and force CO to CI.
			11 ANR	$CI \vee (R_n \wedge AC) \rightarrow CO$ $R_n \wedge AC \rightarrow R_n$	Logically AND AC with R_n . Deposit the result in R_n . Force CO to one if the result is non-zero. Used to AND the accumulator with a register and test for a zero result.
4	II	XX	—	$CI \vee (M \wedge AC \wedge K) \rightarrow CO$ $M \wedge (AC \wedge K) \rightarrow AT$	Logically AND the K-bus with AC. Logically AND the result with the M-bus. Deposit the final result in AC or T. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on CO.
			00 CLA	$CI \rightarrow CO$ $0 \rightarrow AT$	Clear AC or T, as specified, to all 0's. Force CO to CI. Used to clear the specified register and force CO to CI.
			11 ANM	$CI \vee (M \wedge AC) \rightarrow CO$ $M \wedge AC \rightarrow AT$	Logically AND the M-bus with AC. Deposit the result in AC or T. Force CO to one if the result is non-zero. Used to AND M-bus data to the accumulator and test for a zero result.
4	III	XX	—	$CI \vee (AT \wedge I \wedge K) \rightarrow CO$ $AT \wedge (I \wedge K) \rightarrow AT$	Logically AND the I-bus with the K-bus. Logically AND the result with AC or T. Deposit the final result in the specified register. Logically OR CI with the word-wise OR of the final result. Place the value of the carry OR on CO.
			00 CLA	$CI \rightarrow CO$ $0 \rightarrow AT$	Clear AC or T, as specified, to all 0's. Force CO to CI. Used to clear the specified register and force CO to CI.
			11 ANI	$CI \vee (AT \wedge I) \rightarrow CO$ $AT \wedge I \rightarrow AT$	Logically AND the I-bus with AC or T, as specified. Deposit the result in the specified register. Force CO to one if the result is non-zero. Used to AND the I-bus to the accumulator and test for a zero result.
5	I	XX	—	$CI \vee (R_n \wedge K) \rightarrow CO$ $K \wedge R_n \rightarrow R_n$	Logically AND the K-bus with R_n . Deposit the result in R_n . Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
			00 CLR	$CI \rightarrow CO$ $0 \rightarrow R_n$	Clear R_n to all 0's. Force CO to CI. Used to clear a register and force CO to CI.
			11 TZR	$CI \vee R_n \rightarrow CO$ $R_n \rightarrow R_n$	Force CO to one if R_n is non-zero. Used to test a register for zero. Also used to AND K-bus data with a register for masking and, optionally, testing for a zero result.
5	II	XX	—	$CI \vee (M \wedge K) \rightarrow CO$ $K \wedge M \rightarrow AT$	Logically AND the K-bus with the M-bus. Deposit the result in AC or T, as specified. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
			00 CLA	$CI \rightarrow CO$ $0 \rightarrow AT$	Clear AC or T, as specified, to all 0's. Force CO to CI. Used to clear the specified register and force CO to CI.
			11 LTM	$CI \vee M \rightarrow CO$ $M \rightarrow AT$	Load AC or T, as specified, from the M-bus. Force CO to one if the result is non-zero. Used to load the specified register from memory and test for a zero result. Also used to AND the K-bus with the M-bus for masking and, optionally, testing for a zero result.
5	III	XX	—	$CI \vee (AT \wedge K) \rightarrow CO$ $K \wedge AT \rightarrow AT$	Logically AND the K-bus with AC or T, as specified. Deposit the result in the specified register. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
			00 CLA	$CI \rightarrow CO$ $0 \rightarrow AT$	Clear AC or T, as specified, to all 0's. Force CO to CI. Used to clear the specified register and force CO to CI.
			11 TZA	$CI \vee AT \rightarrow CO$ $AT \rightarrow AT$	Force CO to one if AC or T, as specified, is non-zero. Used to test the specified register for zero. Also used to AND the K-bus to the specified register for masking and, optionally, testing for a zero result.

FUNCTION DESCRIPTION (CONT'D)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
6	I	XX	—	$CI \vee (AC \wedge K) \rightarrow CO$ $R_n \vee (AC \wedge K) \rightarrow R_n$	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus. Place the result of the carry OR on CO. Logically OR R_n with the logical AND of AC and the K-bus. Deposit the result in R_n .
		OO	NOP	$CI \rightarrow CO$ $R_n \rightarrow R_n$	Force CO to CI. Used as a null operation or to force CO to CI.
		11	ORR	$CI \vee AC \rightarrow CO$ $R_n \vee AC \rightarrow R_n$	Force CO to one if AC is non-zero. Logically OR AC with R_n . Deposit the result in R_n . Used to OR the accumulator to a register and, optionally, test the previous accumulator value for zero.
6	II	XX	—	$CI \vee (AC \wedge K) \rightarrow CO$ $M \vee (AC \wedge K) \rightarrow AT$	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus. Place the carry OR on CO. Logically OR the M-bus with the logical AND of AC and the K-bus. Deposit the final result in AC or T.
		OO	LMF	$CI \rightarrow CO$ $M \rightarrow AT$	Load AC or T, as specified, from the M-bus. Force CO to CI. Used to load the specified register with memory data and force CO to CI.
		11	ORM	$CI \vee AC \rightarrow CO$ $M \vee AC \rightarrow AT$	Force CO to one if AC is non-zero. Logically OR the M-bus with AC. Deposit the result in AC or T, as specified. Used to OR M-bus with the AC and, optionally, test the previous value of AC for zero.
6	III	XX	—	$CI \vee (I \wedge K) \rightarrow CO$ $AT \vee (I \wedge K) \rightarrow AT$	Logically OR CI with the word-wise OR of the logical AND of the I-bus and the K-bus. Place the carry OR on CO. Logically AND the K-bus with the I-bus. Logically OR the result with AC or T, as specified. Deposit the final result in the specified register.
		OO	NOP	$CI \rightarrow CO$ $R_n \rightarrow R_n$	Force CO to CI. Used as a null operation or to force CO to CI.
		11	ORI	$CI \vee I \rightarrow CO$ $I \vee AT \rightarrow AT$	Force CO to one if the data on the I-bus is non-zero. Logically OR the I-bus to AC or T, as specified. Deposit the result in the specified register. Used to OR I-bus data with the specified register and, optionally, test the I-bus data for zero.
7	I	XX	—	$CI \vee (R_n \wedge AC \wedge K) \rightarrow CO$ $R_n \oplus (AC \wedge K) \rightarrow R_n$	Logically OR CI with the word-wise OR of the logical AND of R_n and AC and the K-bus. Place the carry OR on CO. Logically AND the K-bus with AC. Exclusive-NOR the result with R_n . Deposit the final result in R_n .
		OO	CMR	$CI \rightarrow CO$ $\overline{R_n} \rightarrow R_n$	Complement the contents of R_n . Force CO to CI.
		11	XNR	$CI \vee (R_n \wedge AC) \rightarrow CO$ $R_n \oplus AC \rightarrow R_n$	Force CO to one if the logical AND of AC and R_n is non-zero. Exclusive-NOR AC with R_n . Deposit the result in R_n . Used to exclusive-NOR the accumulator with a register.
7	II	XX	—	$CI \vee (M \wedge AC \wedge K) \rightarrow CO$ $M \oplus (AC \wedge K) \rightarrow AT$	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus and M-bus. Place the carry OR on CO. Logically AND the K-bus with AC. Exclusive NOR the result with the M-bus. Deposit the final result in AC or T.
		OO	LCM	$CI \rightarrow CO$ $\overline{M} \rightarrow AT$	Load the complement of the M-bus into AC or T, as specified. Force CO to CI.
		11	XNM	$CI \vee (M \wedge AC) \rightarrow CO$ $M \oplus AC \rightarrow AT$	Force CO to one if the logical AND of AC and the M-bus is non-zero. Exclusive-NOR AC with the M-bus. Deposit the result in AC or T, as specified. Used to exclusive-NOR memory data with the accumulator.
7	III	XX	—	$CI \vee (AT \wedge I \wedge K) \rightarrow CO$ $AT \oplus (I \wedge K) \rightarrow AT$	Logically OR CI with the word-wise OR of the logical AND of the specified register and the I-bus and K-bus. Place the carry OR on CO. Logically AND the K-bus with the I-bus. Exclusive-NOR the result with AC or T, as specified. Deposit the final result in the specified register.
		OO	CMA	$CI \rightarrow CO$ $\overline{AT} \rightarrow AT$	Complement AC or T, as specified. Force CO to CI.
		11	XNI	$CI \vee (AT \wedge I) \rightarrow CO$ $I \oplus AT \rightarrow AT$	Force CO to one if the logical AND of the specified register and the I-bus is non-zero. Exclusive-NOR AC with the I-bus. Deposit the result in AC or T, as specified. Used to exclusive-NOR input data with the accumulator.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +160°C
All Output and Supply Voltages	-0.5V to +7V
All Input Voltages	-1.0V to +5.5V
Output Currents	100mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

SIGNETICS CENTRAL PROCESSING ELEMENT ■ N3002

DC CHARACTERISTICS $T_A = 0^\circ\text{C to } +70^\circ\text{C}$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP ¹	MAX	
V_C Input Clamp Voltage (All Input Pins)	$V_{CC} = 4.75\text{V}, I_C = -5\text{mA}$		-0.8	-1.0	V
I_F Input Load Current: $F_0-F_6, \text{CLK}, K_0, K_1, \text{EA}, \text{ED}$ $I_0, I_1, M_0, M_1, \text{LI}$ CI	$V_{CC} = 5.25\text{V}, V_F = 0.45\text{V}$		-0.05	-0.25	mA
			-0.85	-1.5	mA
			-2.3	-4.0	mA
I_R Input Leakage Current: $F_0-F_6, \text{CLK}, K_0, K_1, \text{EA}, \text{ED}$ $I_0, I_1, M_0, M_1, \text{LI}$ CI	$V_{CC} = 5.25\text{V}, V_R = 5.25\text{V}$			40	μA
				60	μA
				180	μA
V_{IL} Input Low Voltage	$V_{CC} = 5.0\text{V}$			0.8	V
V_{IH} Input High Voltage		2.0			V
I_{CC} Power Supply Current	$V_{CC} = 5.25\text{V}^2$		145	190	mA
V_{OL} Output Low Voltage Except X and Y X and Y	$V_{CC} = 4.75\text{V}, I_{OL} = 10\text{mA}$ $V_{CC} = 4.75\text{V}, I_{OL} = 16\text{mA}$		0.3	0.45	V
			0.35	0.50	V
V_{OH} Output High Voltage (All Output Pins)	$V_{CC} = 4.75\text{V}, I_{OH} = -1\text{mA}$	2.4	3.0		V
I_{OS} Short Circuit Output Current (All Output Pins)	$V_{CC} = 5.0\text{V}$	-15	-25	-60	mA
$I_{O(\text{off})}$ Off State Output Current A_0, A_1, D_0 and D_1 Only	$V_{CC} = 5.25\text{V}, V_O = 0.45\text{V}$ $V_{CC} = 5.25\text{V}, V_O = 5.25\text{V}$			-100	μA
				100	μA

NOTES:

1. Typical values are for $T_A = 25^\circ\text{C}$ and typical supply voltage.
2. CLK input grounded, other inputs open.

SWITCHING CHARACTERISTICS $T_A = 0^\circ\text{C to } 70^\circ\text{C}, V_{CC} = 5\text{V} \pm 5\%$

SYMBOL	PARAMETER	MIN	TYP ¹	MAX	UNIT
t_{CY}	Clock Cycle Time	70	45		ns
t_{WP}	Clock Pulse Width	17	10		ns
t_{FS}	Function Input Set-Up Time (F_0 through F_6)	48	31		ns
t_{DS}	Data Set-Up Time:	40	24		ns
	$I_0, I_1, M_0, M_1, K_0, K_1$				
t_{SS}	LI, CI	21	7		ns
t_{FH}	Data and Function Hold Time:	4	0		ns
	F_0 through F_6				
t_{DH}	$I_0, I_1, M_0, M_1, K_0, K_1$	4	0		ns
t_{SH}	LI, CI	12	0		ns
t_{XF}	Propagation Delay to X, Y, RO from:	13	18-40	73	ns
	Any Function Input				
	Any Data Input				
	Trailing Edge of CLK				
t_{XL}	Leading Edge of CLK				ns
t_{CL}	Propagation Delay to CO from:	16	24-44	84	ns
	Leading Edge of CLK				
t_{CT}	Trailing Edge of CLK		40	56	ns
t_{CF}	Any Function Input		35	52	ns
t_{CD}	Any Data Input		23	44	ns
t_{CC}	CI (Ripple Carry)		13	20	ns
t_{DL}	Propagation Delay to A_0, A_1, D_0, D_1 from:		25	40	ns
	Leading Edge of CLK				
t_{DE}	Enable Input ED, EA		12	20	ns

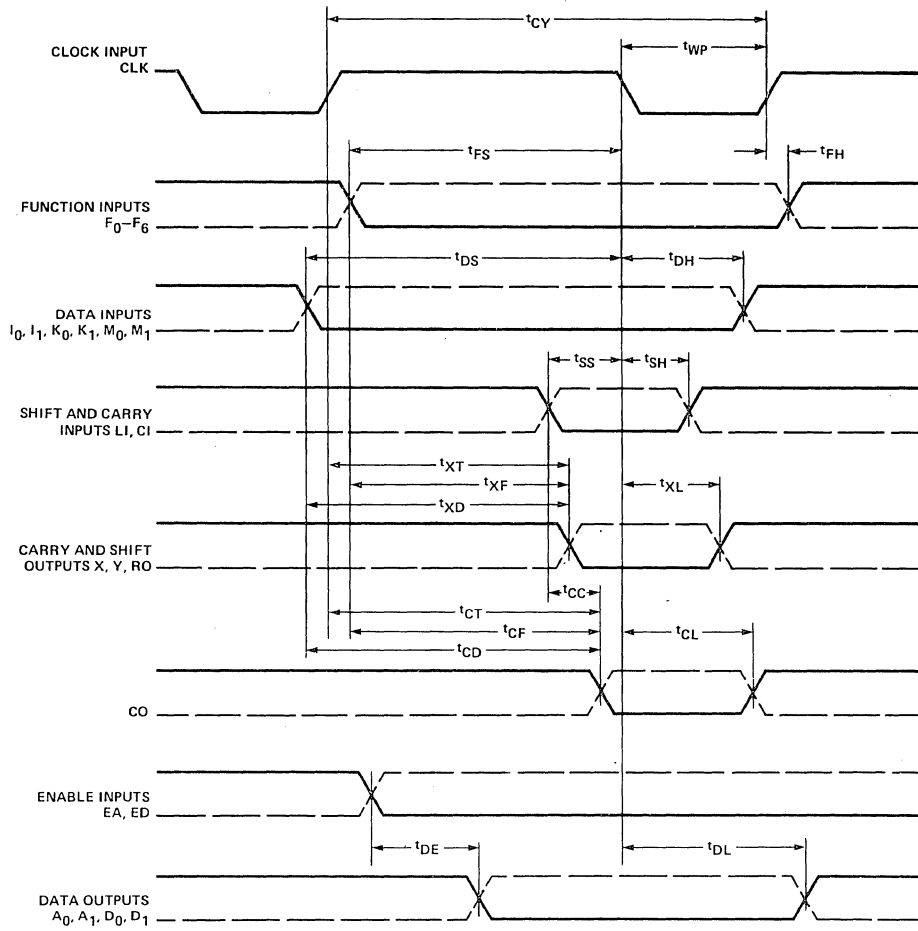
NOTE:

1. Typical values are for $T_A = 25^\circ\text{C}$ and typical supply voltage.

Signetics

MICROPROCESSOR

PARAMETER MEASUREMENT INFORMATION



ALTERNATE SOURCE DIRECTORY

The Alternate Source Directory is an industry wide cross reference of those devices which manufacturers claim are pin-for-pin and functional equivalents to IC's made by other firms. It is a compilation of many individual references and shows literally thousands of alternates that aren't implied by their model numbers, especially in the linear and memory areas. Unlike the usual alternate source guides this directory leads you to many alternate sources for any particular device, not just one. It is the most comprehensive alternate source directory ever published and contains over 14,000 cross references.

how to use the alternate source directory

The second column of this Alternate Source Directory shows devices which are replacements for those in the first column. Devices listed in bold face type have technical data in the Master Selection Guide. This information begins on the page listed below the bold face part numbers. Products preceded by a ¶ have been discontinued by the manufacturer. This section does include devices not listed in the Master Selection Guide e.g., discontinued items, consumer circuits, DTL and 54L devices.

This list is compiled from manufacturers' recommendations. Since there is a tendency for every company to only show itself as an alternate to the prominent manufacturers, and for the larger ones to ignore the little ones, not every device is referenced both ways to every other one. Therefore, if you are looking for alternates to a lesser known company's device, take the replacements you find, especially if they are made by prominent companies and look them up to see if you can find any other sources.

In order to maintain this list within some reason-

able bounds, the A and B suffixes indicating improved versions generally have been dropped. If this weren't done, for example, every higher speed selection conjured up by a memory manufacturer would result in a device that could replace many equal or slower competitors and this directory would become highly involved in slight performance variations. Moreover, improved performance is only important if your circuits take advantage of it.

One of the difficulties with any cross reference is that devices meant to be alternates do not necessarily perform the same in all circuits. Thus, it will be necessary for you to check specifications, or even to check circuit performance before deciding which alternates are right for you. A major benefit of this list is that it gives you more alternatives to study. But if you don't find what you need here, it may be possible to find additional alternates by locating the device in the Master Selection Guide. Particularly for digital circuits, the other products grouped with it will normally offer similar or identical performance.

ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	
Advanced Memory Systems												
AMS6002	Nortec	6002	LM107	National	LM107	LM307	Signetics	LM307	3101A	TI	SN74S289	
AMS6003	Nortec	6003	LM107	Raytheon	LM107	LM307	Teledyne S	LM307	3114	TI	TMS3114	
AMS7001	Motorola	MCM7001		RCA	CA107	LM308	AD	AD308	723	Intersil	723	
	Nitron	7001			see page 661			see page 625		Raytheon	RC723	
	RCA	MW7001	LM108	Teledyne S	LM107			Intersil		Raytheon	RM723	
	TI	TMS7001						Raytheon		RCA	CA723	
								Teledyne S		Teledyne S	723	
Advanced Micro Devices												
AM2071	Signetics	82S07	LM108	AD	AD108	LM310	Intersil	LM310	725	PMI	SSS725	
AM2505	Raytheon	RC2505			see page 625		Motorola	MLM310	741	Intersil	741	
AM2533	Signetics	2533	LM110	Intersil	LM110					PMI	SSS741	
	TI	TMS3133		Motorola	MLM110	LM311	Harris	HA-2311		Raytheon	RC741	
AM27LS00	Fairchild	93421		National	LM110		Intersil	LM311		Raytheon	RM741	
AM27LS01	Fairchild	93411	LM111	Harris	HA-2111	LM318	Intersil	LM311		RCA	CA741	
AM27LS10	Fairchild	93416		Intersil	LM111		Motorola	MLM311		see page 661		
	Harris	HPROM1024	LM111	Motorola	MLM111		Raytheon	LM311		Teledyne S	741	
	Intel	3601		National	LM111	NE555	RCA	CA311	747	PMI	SSS747	
		see page 772, 773			see page 661			see page 661		Raytheon	RC747	
AM27LS11	Synertek	3611	LM118	AD	AD518			see page 624		Raytheon	RM747	
AM27S02	Fairchild	93404			see page 624	SN54S189	TI	SN54S189		RCA	CA747	
	Intersil	IM5501		National	LM118			see page 661		Teledyne S	747	
	MMI	5560	LM201	AD	AD201	SN54S182	Fairchild	9342	9080	Intel	8080	
	MMI	6560			see page 625		Raytheon	54182		see page 950		
	TI	SN54S289		Intersil	LM201	SN54181		TI	SN74181	TI	TMS8080	
	TI	SN74S289		Motorola	MLM201			TI	SN74182		Mostek	MK4102
AM27S03	Fairchild	93405	LM202	Motorola	MLM210	SN5489	Intersil	IM5501	9102	Mostek	MK4102	
	MMI	5561			see page 625		MMI	5560		Signetics	2402	
	MMI	6561		National	LM201	SN74S160	Raytheon	5489		Synertek	SY2102	
	National	DM7599		Raytheon	LM201			5489		TI	TMS4033	
	National	DM8599		RCA	CA748	SN74S161	Fairchild	93S10	93L00	Fairchild	93L00	
	TI	SN54S189		Signetics	LM201		Fairchild	93S16	93L01	Fairchild	93L01	
	TI	SN74S189		Teledyne S	LM201	SSS725			93L08	Fairchild	93L08	
AM2700	Fairchild	93421	LM205	Intersil	LM205	1002	Mostek	MK1002	93L09	Fairchild	93L09	
	Intersil	IM5523		Motorola	MLM205	1101	Intersil	IM7501	93L10	Fairchild	93L10	
	MMI	6531		Raytheon	LM205		Intersil	IM7511	93L11	Fairchild	93L11	
	Signetics	IM82S16	LM207	Teledyne S	LM205	1402	Mostek	MK4007	93L12	Fairchild	93L12	
		see page 804, 806, 815,			see page 625			1402	93L14	Fairchild	93L14	
	Signetics	82S06		Intersil	LM207	1403	Nortec	1402	93L16	Fairchild	93L16	
	TI	SN54S201		Motorola	MLM207		Signetics	2502	93L18	Fairchild	93L18	
	TI	SN74S201		Raytheon	LM207	1404	Synertek	SY1402	93L21	Fairchild	93L21	
AM2701	Fairchild	93411	LM208	AD	AD208			1404	93L22	Fairchild	93L22	
	Intersil	IM5533			see page 625	1488	Exar	XR1488	93L24	Fairchild	93L24	
	MMI	6530		Intersil	LM208		Motorola	MC1488	93L28	Fairchild	93L28	
	Signetics	IM82S16		Raytheon	LM208	1489	National	DS1488	93L34	Fairchild	93L34	
		see page 804, 806, 815,		Teledyne S	LM207		Raytheon	RC1488	93L38	Fairchild	93L38	
	TI	SN74S301			see page 661	1498A	Exar	XR1489	93L40	Fairchild	93L40	
AM2715	Intersil	IM5523	LM210	Intersil	LM210		National	DS1489	93L41	Fairchild	93L41	
AM2802	Synertek	SY2802		Motorola	MLM210	1500	Raytheon	RC1489	93L60	Fairchild	93L60	
AM2803	Synertek	SY2803	LM211	Harris	HA-2211	1501	Motorola	MC1498A	93L66	Fairchild	93L66	
AM2804	Synertek	SY2804		Intersil	LM211	1600	Intersil	AM1500	9300	Fairchild	9300	
AM2814	TI	TMS3114		Motorola	MLM211	2101		AM1501	9300	Raytheon	RM9300	
AM2825	Synertek	SY5025		Raytheon	LM211			AM166039	9300	TI	SN54195	
AM2826	Synertek	SY5026		RCA	CA211	2101	EA	EA2101	9301	TI	SN74195	
AM2827	Synertek	SY2827			see page 661		Intel	2101	9301	Fairchild	9301	
AM2833	Synertek	SY2833	LM218	AD	AD518	2102	Synertek	SY2101	9304	TI	SN29301	
	TI	TMS3133			see page 624			see page 624		TI	SN39301	
AM4102	Mostek	MK4102		Raytheon	LM218	2111	Mostek	MK4102	9304	Fairchild	9304	
LM101	AD	AD101	LM301	AD	AD301			see page 625		Raytheon	RM9304	
		see page 625			see page 625	2112	EA	EA2111	9306	Fairchild	9306	
	Intersil	LM101		Intersil	LM301		Intel	2111	9308	Fairchild	9308	
	Motorola	MLM101		Motorola	MLM301	2112	Synertek	SY2111	9309	Raytheon	RM9308	
	National	LM101		Raytheon	LM301			2112		TI	SN29308	
	Raytheon	LM101		Signetics	LM301	2401	Synertek	SY2112	9309	TI	SN39308	
	RCA	CA101		Teledyne S	LM301			SY2401		Fairchild	9309	
		see page 661			see page 661	31L01	MMI	L5560	9309	TI	SN29309	
	Signetics	LM101	LM305	Intersil	LM305		MMI	L6560	9310	TI	SN39309	
	Teledyne S	LM101		Motorola	MLM305			see page 804, 806, 814,		Fairchild	9310	
LM105	Intersil	LM105		Raytheon	LM305	31L0101	Intersil	IM5501	9310	Raytheon	RM9310	
	Motorola	MLM105	LM307	Teledyne S	LM305		Signetics	N8225		TI	SN54160	
	National	LM105			see page 661	3101		see page 661		TI	SN74160	
	Raytheon	LM105		Intersil	LM307		AMI	S1685	9311	Fairchild	9311	
	Teledyne S	LM105		Motorola	MLM307		Fairchild	93403		Raytheon	RM9311	
LM107	Intersil	LM107		Raytheon	LM307		Intersil	IM5501		TI	SN54154	
	Motorola	MLM107		RCA	CA307		TI	SN7489		TI	SN74154	
					see page 661	3101A	TI	SN54S289	9312	Fairchild	9312	

† Discontinued

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Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device
Advanced Micro Devices (cont)		S2556	see page 254 Nitron NC1184	AD208	Teledyne S LM208	Electronic Arrays	
9312	Raytheon RM9312 TI SN29312 TI SN39312	† S2566	see page 254 Motorola MC1182 Nitron NC1182	AD211	National LM211 RCA CA211 see page 661 Signetics LM211 Teledyne S LM211	EA1004	TI TMS3003
9314	Fairchild 9314	S2567	see page 254 Nitron NC1181	AD301	see page 625 AMD LM301 Fairchild μA301 National LM301 Signetics LM301 Teledyne S LM301	EA1009	AMI S2181
9316	Fairchild 9316 Raytheon RM9316 TI SN54161 TI SN74161	S3102	TI TMS4035	AD308	see page 625 AMD LM308 Fairchild μA308 National LM308 Signetics LM308 Teledyne S LM308	† EA1012	TI TMS3002
9318	Fairchild 9318 TI SN54148 TI SN74148	S3102A	TI TMS4033	AD311	National LM311 RCA CA311 see page 661 Signetics LM311 Teledyne S LM311	EA1206	AMI S1685
9321	Fairchild 9321	S3102B	TI TMS4034	AD503	see page 624 National LH0042 Teledyne S 2740	EA12065	AMI S1685
9322	Fairchild 9322 Raytheon RM9322 TI SN54157 TI SN74157	S3103	Nortec 1103	AD506	see page 624 National LH0022	EA12105	AMI S1685
9324	Fairchild 9324	S4006	see page 706 Mostek MK4006	AD513	National LH0042	EA1212	AMI S1685
9328	Fairchild 9328	S4008	see page 706 Mostek MK4008	AD516	National LH0022	EA1400	AMI S4006 see page 706
9334	Fairchild 9334	S4021	see page 722 TI TMS4060	AD710	National LM710 Raytheon RM710 Signetics μA710 Teledyne S 710	† EA3000	AMI S8773
9338	Fairchild 9338	S4096	see page 728 EA EA4096 EMM/Semi RO3-4096 Fairchild 4096 GI, RO3-4096	AD711	National LM711 Raytheon RM711 Signetics μA711 Teledyne S 711	† EA3001	AMI S8773
9340	Fairchild 9340	S5232	see page 706 Mostek MK2500 Mostek MK2600 National MMS232	AD7505	Siliconix DG507 see page 561, 563, 564,	† EA3100	AMI S8773
9341	Fairchild 9341 Raytheon RM9341 TI SN54181 TI SN74181	S6800	see page 862 Motorola 6800	AD7506	see page 548 Siliconix DG506 see page 561, 563, 564,	† EA3101	AMI S8773
93415	Intel 2115 see page 766, 769 TI SN54S314 TI SN74S314	S6810	see page 884 Motorola MCM6810	AD7513	see page 546 Siliconix DG200 see page 559, 560	† EA3132	AMI S8773
9342	Fairchild 9342 Raytheon RM9342 TI SN54182 TI SN74182	S6820	see page 889 Motorola MC6820	LM101	Raytheon LM101	† EA3300	AMI S8772
9360	Fairchild 9360 Raytheon RM9360	S6830	see page 887 Motorola MCM6830	LM108	Raytheon LM108	† EA3307	AMI S8772
9366	Fairchild 9366 Raytheon RM9366	S6850	see page 895 Motorola MC6850	LM111	Raytheon LM111	EA3800	AMI S8773
9401	Synertek SY2401	S8499	Nitron NCM1130	LM201	Raytheon LM201	EA4000	AMI S8771 see page 706 GI RO3-5120
96L02	Fairchild 96L02	S8865	see page 706 GI RO5-8192	LM208	Raytheon LM208	EA4004	AMI S8771 see page 706
9600	Fairchild 9600	S8996	see page 706 EMM/Semi RO3-16384 GI RO3-16384 Nortec 8996	LM211	Raytheon LM211	EA4015	AMI S8771 see page 706
9601	Fairchild 9601 Raytheon RF9601 TI SN29601	Analog Devices		LM212	Raytheon LM212	EA4016	AMI S8771 see page 706
9602	Fairchild 9602 Raytheon RF9602	AD101	see page 625 AMD LM101 Fairchild μA101 National LM101 RCA CA101 see page 661 Signetics LM101 Teledyne S LM101	LM301	Raytheon LM301	EA4096	AMI S4096 see page 728 EMM/Semi RO3-4096 Fairchild 4096 GI RO3-4096 Mostek MK4096 see page 778, 781 Rockwell 1604
9614	Fairchild 9614	AD108	see page 625 AMD LM108 Fairchild μA108 National LM108 RCA CA108 Signetics LM108 Teledyne S LM108	LM308	Raytheon LM308	EA4900	Mostek MK28000 see page 783 TI TMS4800
9615	Fairchild 9615	AD111	National LM111 RCA CA111 see page 661 Signetics LM111 Teledyne S LM111	LM311	Raytheon LM311	EMM/Semi	
9616	Fairchild 9616	AD201	see page 625 AMD LM201 Fairchild LM201 National LM201 RCA CA201 see page 661 Signetics LM201 Teledyne S LM201	Burr-Brown Research		RA3-4256	GI RA3-4256
9617	Fairchild 9617	AD208	see page 625 AMD LM208 Fairchild μA208 National LM208 RCA CA208	3500	AD AD3500	RO3-16384	GI RO3-16384
9620	Fairchild 9620			3503	AD AD540 see page 624 Intersil ICL3503	RO3-4096	GI RO3-4096
9621	Fairchild 9621 Raytheon RM9621			3507	AD AD3509	RA3-4402	GI see page 734 RO3-4402
American Microsystems Inc.				3508	AD AD3507	RO3-5120	GI RO3-5120
S1103	see page 707 Intel 1103			3524	Intersil ICL3524	1217	GI RA3-1217
S146	Intel 1103-146 Signetics 2146			3542	AD AD3542	1218	GI RA3-1218
† S1670	Motorola MC1160			4201	AD AD530	1801	GI RA3-1801
S1757	see page 532			4550	Intersil ICL4550	1802	GI RA-1802
S1883	GI AY5-1013 Western TR1402 see page 533 GI AY5-1013 TI TMS6011 Western TR1602					Exar Integrated Systems	
† S2076	Intersil IM7780					XR1310	National LM1310
† S2102	Intersil IM7552					XR1800	National LM1800
† S2103	Motorola MCM6605					XR2240	see page 637 Fairchild 7240
S2222	see page 706 Nortec 2222 Signetics N2222 Signetics S2222					XR2556	Teledyne S D555
S2555	see page 254 Nitron NC1183					XR3503	Raytheon RM3503 see page 649
						XR4194	Raytheon RC4194 see page 655
						XR4558	Raytheon RC4558 see page 651
						XR555	Lithic Sys LS555
						XR556	Raytheon RC556
						XR742	Fairchild 742
						4136	Raytheon RC4136 see page 647 640
						555	Teledyne S 555
						556	Teledyne S 556
						Fairchild Semiconductor	
						μA1458	Motorola MC1458

† Discontinued

ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
Fairchild Semiconductor (cont)			F40160	TI	TP4360	F4042	Harris	HD4042
μA1558	Motorola	MC1558	F40161	Harris	HD54C161	F4043	Harris	HD4043
μA3018	Lithic Sys	LA3018	see page 266			F4044	Harris	HD4044
μA3018A	Lithic Sys	CA3018A	Harris HD74C161			F4049	Harris	HD4049
μA3026	Lithic Sys	LA3026	see page 266			F4050	Harris	HD4050
μA3045	Lithic Sys	LA3045	National		MM54C161	F4066	Harris	HD4066
μA3046	Lithic Sys	LA3046	National		MM74C161	F4510	Harris	HD4510
μA3086	Lithic Sys	LA3086	Teledyne S		MM54C161	F4512	Harris	HD4512
μA3403	Raytheon	RC3403	Teledyne S		MM74C161	F4516	Harris	HD4516
see page 649			TI		TF4361	F4518	Harris	HD4518
μA3503	Raytheon	RM3503	TI		TP4361	F4519	Harris	HD4519
see page 649			F40162	Harris	HD54C162	F4520	Harris	HD4520
μA733	Raytheon	RM733	see page 266			LM101	AMD	LM101
μA734	Intersil	734	Harris HD74C162			Intersil		LM101
μA739	Motorola	MC1303	see page 266			National		LM101
μA740	Intersil	LH0042	National		MM54C162	National		LM101
μA753	Sprague	ULN-2209	Teledyne S		MM54C162	Raytheon		LM101
μA754	National	LM1596	TI		TF4362	RCA		CA101
μA758	Exar	XR1800	TI		TP4362	see page 661		
μA760	National	LM160	F40163	Harris	HD54C163	Signetics		LM101
μA763	National	LM1496	Harris		HD74C163	Teledyne S		LM101
μA777	Intersil	777	National		MM54C163	TI		SN52101
μA78L02	Signetics	78L02C	National		MM74C163	LM102	AMD	LM102
see page 673			TI		TF4362	Intersil		LM102
μA78L05	Signetics	78L05C	TI		TP4362	National		LM102
see page 673			F4017	Harris	HD4017	LM104	National	LM104
μA78L06	Signetics	78L06C	F40174	Harris	HD54C174	Raytheon		LM104
see page 673			Harris		HD74C174	Teledyne S		LM104
μA78L08	Signetics	78L08C	National		MM54C174	LM105	AMD	LM105
see page 673			National		MM74C174	Intersil		LM105
μA78L12	Signetics	78L12C	F40175	Harris	HD54C175	National		LM105
see page 673			Harris		HD74C175	Raytheon		LM105
μA78M05	Teledyne S	78M05	National		MM54C175	Teledyne S		LM105
μA78M06	Teledyne S	78M06	National		MM74C175	LM107	AMD	LM107
μA78M12	Teledyne S	78M12	F4018	Harris	HD4018	Intersil		LM107
μA78M15	Teledyne S	78M15	see page 266			Motorola		MLM107
μA78M24	Teledyne S	78M24	F4019	Harris	HD4019	National		LM107
μA7805	Signetics	7805	see page 266			Raytheon		LM107
see page 668			F40192	Harris	HD54C192	Signetics		LM107
μA7806	Signetics	7806	see page 266			Teledyne S		SN52107
see page 668			Harris		HD74C192	TI		SN52307
μA7808	Signetics	7808	see page 266			LM108	AMD	LM108
see page 668			National		CD40192	Intersil		LM108
μA7812	Signetics	7812	National		MM54C192	National		LM108
see page 668			RCA		CD40192	Raytheon		LM108
μA7815	Signetics	7815	see page 375			RCA		CA108
see page 668			Teledyne S		MM54C192	Signetics		LM108
μA7818	Signetics	7818	Teledyne S		MM74C192	Teledyne S		LM108
see page 668			F40193	Harris	HD54C193	LM109	National	LM109
μA7824	Signetics	7824	see page 266			Raytheon		LM109
see page 668			Harris		HD74C193	TI		SN52109
μA795	Motorola	MC1495	see page 266			LM110	AMD	LM110
μA796	Motorola	MC1595	National		CD40193	Intersil		LM110
F10144	Motorola	MC1596	National		MM54C193	National		LM110
F10405	Signetics	10144	National		MM74C193	LM111	AMD	LM111
F10405	TI	SN10147	RCA		CD40193	Harris		HA-2111
F10410	TI	SN10144	see page 375			Intersil		LM111
F4001	Harris	HD4001	Teledyne S		MM54C193	Raytheon		LM111
F4006	Harris	HD4006	Teledyne S		MM74C193	RCA		CA111
F4007	Harris	HD4007	F4020	Harris	HD4020	see page 661		
F4008	Harris	HD4008	see page 266			Signetics		LM111
F40085	Harris	HD74C85	F4021	Harris	HD4021	Teledyne S		LM111
see page 266			see page 266			LM201	Intersil	LM201
F40097	National	MM74C85	F4022	Harris	HD4022	National		LM201
Harris		HD80C97	see page 266			Raytheon		LM201
National		MM80C97	F4023	Harris	HD4023	RCA		CA201
F40098	National	MM80C98	see page 661			Signetics		LM201
F4011	Harris	HD4011	Teledyne S		LM201	LM201		LM201
F4012	Harris	HD4012	F4024	Harris	HD4024	F4025	Harris	HD4025
F4013	Harris	HD4013	F4027	Harris	HD4027	F4028	Harris	HD4028
F4014	Harris	HD4014	see page 266			see page 266		
F4015	Harris	HD4015	F4028	Harris	HD4028	F4029	Harris	HD4029
see page 266			see page 266			see page 266		
F40160	Harris	HD546160	F4030	Harris	HD4030	LM207	Intersil	LM207
Harris		HD74C160	see page 266			National		LM207
National		MM54C160	F4035	Harris	HD4035	Raytheon		LM207
National		MM74C160	see page 266			Signetics		LM207
Teledyne S		MM54C160	F4040	Harris	HD4040	Teledyne S		LM207
Teledyne S		MM74C160	see page 266			LM208	Intersil	LM208
TI		TF4360				National		LM208

1 Discontinued

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Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
Fairchild Semiconductor (cont)			3501	Collins National	CRC3501 MM3501	54H22	Motorola Raytheon TI	MC54H22 54H22 SN54H22	5412	Motorola Raytheon TI	MC5412 5412 SN5412
SN5524	National	DS5524	3507	AMI	S8773	54H30	Motorola Signetics TI	MC54H30 S54H30 SN54H30	54121	Motorola TI	MC9603 SN54121
SN74152	TI	SN74152A	3512	AMI	S8773	54H40	Motorola Raytheon Signetics TI	MC54H40 54H40 S54H40 SN54H40	54123	Raytheon TI	54123 SN54123
SN75107A	National Raytheon	DS75107A RC75107A	3513	AMI	S8773	54H50	Motorola TI	MC54H50 SN54H50	54145	Motorola Raytheon TI	MC93145 54145 SN54145
SN75108A	National Raytheon	DS75108A RC75108A	3514	AMI AMI Mostek National National Synertek	S8772 53514 MK2600 MM4233 MM5233 SY3514	54H51	Motorola TI	MC54H51 SN54H51	5415	Raytheon	5415
SN75109	National Raytheon	DS75109 RC75109	3534	AMI	S2103	54H52	Motorola TI	MC54H52 SN54H52	54150	Motorola Raytheon TI	MC93150 54150 SN54150
SN75110	Raytheon	RC75110	3580	AMI	S8773	54H53	Motorola TI	MC54H53 SN54H53	54151	Motorola Raytheon TI	MC93151 54151 SN54151A
SN7524	National	DS7524	3705	Siliconix	SI3705 see page 551	54H54	Motorola TI	MC54H54 SN54H54	54152	Motorola Raytheon TI	MC93152 54152 SN54152A
SN7525	National	DS7525	3708	Siliconix	SI3705 see page 551	54H55	Motorola TI	MC54H55 SN54H55	54153	AMD Motorola Raytheon TI	SN54153 MC93153 54153 SN54153
1103	AMI	S1103A see page 712	3730	AMI	S1757 see page 532	54H60	Motorola TI	MC54H60 SN54H60	54154	AMD Motorola Raytheon TI	SN54154 MC9311 54154 SN54154
1800	SW SW TI TI	SW1800 SW1900 SN151800 SN151900	3731	AMI	S1757 see page 532	54H61	Motorola TI	MC54H61 SN54H61	54155	Raytheon TI	54155 SN54155
1802	SW SW TI TI	SW1802 SW1902 SN151802 SN151902	3850	Mostek	3850 see page 924	54H62	Motorola TI	MC54H62 SN54H62	54156	Raytheon TI	54156 SN54156
1805	TI TI	SN151805 SN151905	3851	Mostek	3851 see page 924	54H71	Motorola TI	MC54H71 SN54H71	54157	Motorola Raytheon TI	MC9322 54157
1806	SW SW TI TI	SW1806 SW1906 SN151806 SN151906	3852	Mostek	3852 see page 966	54H72	Motorola TI	MC54H72 SN54H72	54158	Raytheon TI	54158
1807	TI TI	SN151807 SN151907	3853	Mostek	3853 see page 966	54H74	Motorola Raytheon TI	MC54H74 54H74 SN54H74	54159	Raytheon TI	54159 SN54159
1808	SW SW TI TI	SW1808 SW1908 SN151808 SN151908	3854	Mostek	3854 see page 966	54H76	Signetics TI	S54H76 SN54H76	5416	Motorola TI	MC5416 SN5416
1810	SW SW TI TI	SW1810 SW1910 SN151810 SN151910	4096	AMI EA EMM/Semi GI Mostek Rockwell	S4096 EA4096 RO3-4096 RO3-4096 MK4096 1604	5400	Motorola Raytheon Signetics TI	MC5400 5400 S5400 SN5400	54160	AMD Motorola Raytheon TI	SN54160 MC9310 54160 SN54160
1812	SW SW TI TI	SW1812 SW1912 SN151812 SN151912	54H00	Motorola Raytheon Signetics TI	MC54H00 54H00 S54H00 SN54H00	5401	Motorola Raytheon Signetics TI	MC5401 5401 S5401 SN5401	54161	AMD Motorola Raytheon TI	SN54161 MC9316 54161 SN54161
1814	SW SW	SW1814 SW1914	54H01	Motorola Raytheon Signetics TI	MC54H01 54H01 S54H01 SN54H01	5402	Signetics TI	S5402 SN5402	54162	Raytheon TI	54162 SN54162
2136	Sprague	ULN-2136	54H04	Motorola Raytheon Signetics TI	MC54H04 54H04 S54H04 SN54H04	5403	Motorola Raytheon Signetics TI	MC5403 5403 S5403 SN5403	54164	AMD Motorola Raytheon TI	SN54164 MC93164 54164 SN54164
3002	Siliconix	SI3002 see page 551	54H05	Motorola Raytheon Signetics TI	MC54H05 54H05 S54H05 SN54H05	5404	Motorola Raytheon TI	MC5404 5404 SN5404	54166	Raytheon TI	54166 SN54166
3064	Sprague	ULN-2264	54H08	Motorola	MC54H08	5405	Motorola Raytheon Signetics TI	MC5405 5405 S5405 SN5405	54170	Raytheon TI	54170
3065	Sprague	ULN-2165	54H10	Motorola Raytheon Signetics TI	MC54H10 54H10 S54H10 SN54H10	5406	Motorola TI	MC5406 SN5406	54174	Raytheon TI	54174 SN54174
3067	Sprague	ULN-2267	54H101	Motorola TI	MC54H101 SN54H101	5407	Motorola TI	MC5407 SN5407	54175	Raytheon TI	54175 SN54175
3075	Sprague	ULN-2129	54H102	Motorola TI	MC54H102 SN54H102	5408	Motorola Raytheon Signetics TI	MC5408 5408 S5408 SN5408	54176	Motorola TI	MC93176 SN54176
3257	GI	RO5-2240S	54H108	Motorola TI	MC54H108 SN54H108	5409	Motorola Raytheon TI	MC5409 5409 SN5409	54177	Motorola TI	MC93177 SN54177
3260	AMI	S8564	54H11	Motorola Raytheon TI	MC54H11 54H11 SN54H11	5410	Motorola Raytheon Signetics TI	MC5410 5410 S5410 SN5410	54178	Motorola TI	MC93178 SN54178
3329	AMI	S1685	54H20	Motorola Raytheon Signetics TI	MC54H20 54H20 S54H20 SN54H20	54107	AMD Motorola TI	SN54107 MC54107 SN54107	54181	AMD Motorola Raytheon TI	SN54181 MC93181 54180 SN54180
3330	AMI	S1685	54H21	Motorola TI	MC54H21 SN54H21	5411	Raytheon Signetics	5411 S5411	54181	Motorola Raytheon	MC9341 54181
3331	AMI	S1685									
3337	AMI	S1685									
3341	AMD	3341									
3342	TI	TMS3121									
3343	AMI	S2181									
3344	AMI	S2181									
3347	AMI	S2182									
	Intersil	IM7780									
	Signetics	2518									
	TI	TMS3120									
3348	TI	TMS3112									
3349	TI	TMS3122									
3355	Synertek	SY2833									
	TI	TMS3133									
34001	SSS	SCL4001									
34002	SSS	SCL4002									
34011	SSS	SCL4011									
34012	SSS	SCL4012									
34013	SSS	SCL4013									
34019	SSS	SCL4019									
34023	SSS	SCL4023									
34025	SSS	SCL4025									
34027	SSS	SCL4027									
34030	SSS	SCL4030									
34049	SSS	SCL4049									
34050	SSS	SCL4050									
3501	AMI	S8457									

† Discontinued

ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
Fairchild Semiconductor (cont)			5451	TI	SN5451	5510	Raytheon TI	RM55110 SN55110	74H10	Raytheon Signetics	74H10 N74H10 SN74H10
54181	TI	SN54181	5453	Motorola Signetics TI	MC5453 S5453 SN5453	55235	Motorola	MC55325	74H101	Motorola TI	MC74H101 SN74H101
54182	AMD Motorola Raytheon TI	SN54182 MC9342 54182 SN54182	5454	Motorola Signetics TI	MC5454 S5454 SN5454	702	Motorola Raytheon Raytheon TI	MC1712 RC702 RM702 SN52702	74H102	Motorola TI	MC74H102 SN74H102
54190	Raytheon TI	54190 SN54190	5460	Motorola Signetics TI	MC5460 S5460 SN5460	703	National	LM703	74H105	Motorola	MC9001
54191	Raytheon TI	54191 SN54191	5470	Motorola Signetics TI	MC5470 S5470 SN5470	709	Motorola National Raytheon Raytheon Signetics	MC1709 LM709 RC709 RM709 μ A709	74H108	Motorola TI	MC74H108 SN74H108
54192	AMD Motorola Raytheon Signetics TI	SN54192 MC9360 54192 S54192 SN54192	5472	Motorola Signetics TI	MC5472 S5472 SN5472		Teledyne S TI	709 SN52709	74H11	Motorola Raytheon TI	MC74H11 74H11 SN74H11
54193	AMD Motorola Raytheon Signetics TI	SN54193 MC9366 54193 S54193 SN54193	5473	Motorola Signetics TI	MC5473 S5473 SN5473	710	Motorola National Raytheon Raytheon Signetics	MC1710 LM710 RC710 RM710 μ A710	74H20	Motorola Raytheon Signetics TI	MC74H20 74H20 N74H20 SN74H20
54194	Raytheon TI	54194 SN54194	5474	Motorola Raytheon Signetics TI	MC5474 5474 S5474 SN5474		Silicon G Teledyne S TI	SG710 710 SN52710	74H21	Motorola TI	MC74H21 SN74H21
54195	Raytheon TI	54195 SN54195	5475	Motorola Signetics TI	MC9375 S5475 SN5475	711	Motorola National Raytheon Raytheon Signetics	MC1711 LM711 RC711 RM711 μ A711	74H22	Motorola Raytheon TI	MC74H22 74H22 SN74H22
54198	Raytheon TI	54198 SN54198	5476	Motorola Signetics TI	MC5476 S5476 SN5476		Silicon G Teledyne S TI	SG711 711 SN52711	74H30	Motorola Signetics TI	MC74H30 N74H30 SN74H30
54199	Raytheon TI	54199 SN54199	5477	Motorola Signetics TI	MC9377 S5477 SN5477	715	AMD	715	74H40	Motorola Raytheon Signetics TI	MC74H40 74H40 N74H40 SN74H40
5420	Motorola Signetics TI	MC5420 S5420 SN5420	5480	Motorola Signetics TI	MC9380 S5480 SN5480	720	Sprague	ULN-2137	74H50	Motorola TI	MC74H50 SN74H50
5421	Raytheon TI	5421	5481	Motorola Raytheon TI	MC4304 5481 SN5481A	723	AMD Intersil Motorola National Raytheon Raytheon Signetics	723 723 MC1723 LM723 RC723 RM723 μ A723	74H51	Motorola TI	MC74H51 SN74H51
5422	Raytheon TI	5422	5482	Motorola TI	MC9382 S5482		Silicon G Teledyne S TI	SG723 723 SN52723	74H52	Motorola TI	MC74H52 SN74H52
5423	Motorola TI	MC5423 SN5423	5483	Motorola Raytheon Signetics TI	MC9383 5483 S5483 SN5483	7240	Exar	XR2240 see page 637	74H53	Motorola TI	MC74H53 SN74H53
5425	Motorola TI	MC5425 SN5425	5486	Raytheon Signetics TI	5486 S5486 SN5486	725	AMD PMI Raytheon Raytheon	725 SSS725 RC725 RM725	74H54	Motorola TI	MC74H54 SN74H54
5426	Motorola TI	MC5426 SN5426	5488	Motorola TI	MCM4002 SN5488A	729	National Sprague	LM1034 ULN-2122	74H55	Motorola TI	MC74H55 SN74H55
5427	Motorola TI	MC5427 SN5427	5489	AMD Motorola	SN5489 MC4064	732	National Sprague	LM1305 ULN-2120	74H56	Motorola TI	MC74H56 SN74H56
54283	Raytheon TI	54283 SN54283	5490	Motorola Signetics TI	MC9390 S5490 SN5490A	733	AMD Motorola National Raytheon Raytheon Signetics Silicon G TI	733 MC1733 LM733 RC733 RM733 μ A733 SG733 SN52733	74H60	Motorola TI	MC74H60 SN74H60
5430	Motorola Signetics TI	MC5430 S5430 SN5430	5491	Motorola Signetics TI	MC9391 S5491 SN5491A	734	Intersil	734	74H61	Motorola TI	MC74H61 SN74H61
5437	Motorola TI	MC5437 SN5437	5492	Motorola Signetics TI	MC9392 S5492 SN5492A	739	SGS	TBA231	74H62	Motorola TI	MC74H62 SN74H62
5438	Motorola TI	MC5438 SN5438	5493	Motorola Signetics TI	MC9393 S5493 SN5493A	74H00	Motorola Raytheon Signetics TI	MC74H00 74H00 N74H00 SN74H00	74H71	Motorola TI	MC74H71 SN74H71
5440	Motorola Signetics TI	MC5440 S5440 SN5440	5494	Motorola Signetics TI	MC9394 S5494 SN5494	74H01	Motorola Raytheon Signetics TI	MC74H01 74H01 N74H01 SN74H01	74H72	Motorola TI	MC74H72 SN74H72
5442	Motorola Raytheon Signetics TI	MC9352 5442 S5442 SN5442	5495	Motorola Signetics TI	MC9395 S5495 SN5495A	74H04	Motorola Raytheon Signetics TI	MC74H04 74H04 N74H04 SN74H04	74H73	Motorola Signetics TI	MC74H73 N74H73 SN74H73
5443	Motorola Raytheon Signetics TI	MC9353 5443 S5443 SN5443	5496	Motorola Signetics TI	MC9396 S5496 SN5496	74H05	Motorola Raytheon Signetics TI	MC74H05 74H05 N74H05 SN74H05	74H74	Motorola Raytheon TI	MC74H74 74H74 SN74H74
5444	Motorola Raytheon Signetics TI	MC9354 5444 S5444 SN5444	5497	Motorola Signetics TI	MC9397 S5497 SN5497A	74H08	Motorola	MC74H08	74H76	Signetics TI	N74H76 SN74H76
5445	Motorola Raytheon TI	MC9345 5445 SN5445	55107	AMD Raytheon TI	SN55107B RM55107 SN55107	74H08	Motorola	MC74H08	74S158	AMD TI	SN74S158 SN74S158
5446	Motorola TI	MC9357A SN5446A	55108	AMD Raytheon TI	SN55108 RM55108 SN55108	74H08	Motorola	MC74H08	74S175	AMD TI	SN74S175 SN74S175
5447	Motorola TI	MC9357B SN5447	55109	AMD Raytheon TI	SN55109 RM55109 SN55109	74H08	Motorola	MC74H08	74S194	AMD TI	SN74S194 SN74S194
5448	Motorola Signetics TI	MC9358 S5448 SN5448	55110	AMD	SN55110	74H10	Motorola	MC74H10	74S258	AMD TI	SN74S258 SN74S258
5449	Motorola TI	MC9359 SN5449							740	Intersil Signetics	740 μ A740
5450	Motorola Signetics TI	MC5450 S5450 SN5450							7400	Hitachi Motorola Raytheon Signetics TI	HD2503 MC7400 7400 N7400 SN7400
5451	Motorola Signetics	MC5451 S5451							7401	Hitachi Motorola Raytheon Signetics TI	HD2509 MC7401 7401 N7401 SN7401
									7402	Hitachi Motorola	HD2511 MC7402

† Discontinued

The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device
Fairchild Semiconductor (cont)							
7402	Signetics TI N7402 SN7402	74154	Raytheon TI 74154 SN74154	74198	Raytheon TI 74198 SN74198	746	Sprague ULN-2114
7403	Hitachi HD2528 Motorola MC7403 Raytheon 7403 Signetics N7403 TI SN7403	74155	Raytheon TI 74155 SN74155	74199	Raytheon TI 74199 SN74199	7460	Hitachi HD2502 Motorola MC7460 Signetics N7460 TI SN7460
7404	Hitachi HD2522 Motorola MC7404 Raytheon 7404 Signetics N7404 TI SN7404	74156	Raytheon 74156	742	Exar XR742	747	AMD 747 Motorola MC1747 National LM747 PMI SSS747 Raytheon RC747 Raytheon RM747 RCA CA747
7405	Hitachi HD2523 Motorola MC7405 Raytheon 7405 Signetics N7405 TI SN7405	74157	AMD SN74157 Motorola MC8322 Raytheon 74157 TI SN74157	7420	Hitachi HD2504 Motorola MC7420 Raytheon 7420 Signetics N7420 TI SN7420	see page 661	
7406	Motorola MC7406 TI SN7406	74158	Raytheon 74158	7421	Raytheon 7421	7470	Hitachi HD2539 Motorola MC7470 Signetics N7470 TI SN7470
7407	Motorola MC7407 TI SN7407	74159	Raytheon 74159 TI SN74159	7422	Raytheon TI 7422 SN7422	7472	Hitachi HD2529 Motorola MC7472 Signetics N7472 TI SN7472
7408	Hitachi HD2550 Motorola MC7408 Raytheon 7408 Signetics N7408 TI SN7408	7416	Motorola MC7416 TI SN7416	7423	Motorola MC7423 TI SN7423	7473	Hitachi HD2515 Motorola MC7473 Signetics N7473 TI SN7473
7409	Motorola MC7409 Raytheon 7409 TI SN7409	74160	AMD SN74160 Motorola MC8310 Motorola MC8316 Raytheon 74160 TI SN74160	7425	Motorola MC7425 TI SN7425	7474	Hitachi HD2510 Motorola MC7474 Raytheon 7474 Signetics N7474 TI SN7474
741	AMD 741 Intersil 741 Motorola MC1741 National LM741 PMI SSS741 Raytheon RC741 Raytheon RM741 RCA CA741	74161	Raytheon 74161 TI SN74161	7426	Motorola MC7426 TI SN7426	7475	Motorola MC8375 Signetics N7475 TI SN7475
	see page 661	74162	Raytheon 74162 TI SN74162	7427	Motorola MC7427 TI SN7427	7476	Hitachi HD2516 Motorola MC7476 Signetics N7476 TI SN7476
	Signetics μA741	74163	Raytheon 74163 TI SN74163	74283	Raytheon TI 74283 SN74283	7477	Motorola MC8377
	Silicon G SG741	74164	AMD SN74164 Motorola MC83164 Raytheon 74164 TI SN74164	7430	Hitachi HD2508 Motorola MC7430 Signetics N7430 TI SN7430	748	AMD 748 Intersil 748 Motorola MC1748 National LM101 National LM201 National LM748 Raytheon RC748 Raytheon RM748 RCA CA748 Signetics μA748 Silicon G SG748 Teledyne S 748 TI SN52748
	Teledyne S TI SN52741	74165	Motorola MC83165 Raytheon 74165 TI SN74165	7437	Motorola MC7437 TI SN7437	7480	Signetics N7480 TI SN7480
7410	Hitachi HD2551 Motorola MC7410 Raytheon 7410 Signetics N7410 TI SN7410	74166	Raytheon 74166 TI SN74166	7438	Motorola MC7438 TI SN7438	7481	Motorola MC4004 Raytheon 7481 TI SN7481A
74107	AMD SN74107 Hitachi HD2530 Motorola MC74H107 TI SN74107	7417	Motorola MC83177 TI SN74177	7440	Hitachi HD2501 Motorola MC7440 Signetics N7440 TI SN7440	7482	Hitachi HD2513 Motorola MC8382 TI SN7482
7411	Raytheon 7411 Signetics N7411	74176	Motorola MC83176 TI SN74176	7441	Motorola MC8315 Signetics N7441 TI SN74141	7483	Motorola MC8383 Raytheon 7483 Signetics N7483 TI SN7483A
7412	Raytheon 7412 TI SN7412	74177	Motorola MC83177 TI SN74177	7442	Motorola MC8352 Raytheon 7442 Signetics N7442 TI SN7442A	7486	Hitachi HD2526 Raytheon 7486 Signetics N7486 TI SN7486
74121	Motorola MC8603 TI SN74121	74178	Motorola MC83178 TI SN74178	7444	Motorola MC8354 Raytheon 7444 Signetics N7444 TI SN7444A	7488	Motorola MC4002 TI SN7488A
74123	Raytheon 74123 TI SN74123	74179	Motorola MC83179 TI SN74179	7445	Motorola MC8345 Raytheon 7445 TI SN7445	7489	AMD SN7489 Motorola MC4064 TI SN7489
74136	Raytheon 74136 TI SN74136	74180	Motorola MC83180 Raytheon 74180 TI SN74180	7446	Motorola MC8357 TI SN7446A	7490	Hitachi HD2519 Motorola MC8390 Signetics N7490 TI SN7490A
74141	Signetics N74141 TI SN74141	74181	AMD SN74181 Motorola MC8341 Raytheon 74181 TI SN74181	74464	Teledyne S 75464	7491	Hitachi HD2524
74145	Motorola MC83145 Raytheon 74145 TI SN74145	74182	AMD SN74182 Motorola MC8342 Raytheon 74182 TI SN74182	7447	Motorola MC8357 Signetics N7447 TI SN7447A		
7415	Raytheon 7415	74190	Raytheon 74190 TI SN74190	7448	Motorola MC8358 Signetics N7448 TI SN7448		
74150	Motorola MC83150 Raytheon 74150 TI SN74150	74191	Raytheon 74191 TI SN74191	7449	Motorola MC8359		
74151	Motorola MC83151 Raytheon 74151 TI SN74151A	74192	AMD SN74192 Motorola MC8360 Raytheon 74192 Signetics N74192 TI SN72192	7450	Hitachi HD2506 Motorola MC7450 Signetics N7450 TI SN7450		
74152	Motorola MC83152 Raytheon 74152	74193	AMD SN74193 Motorola MC8366 Raytheon 74193 Signetics N74193 TI SN74193	7451	Hitachi HD2505 Motorola MC7451 Signetics N7451 TI SN7451		
74153	AMD SN74153 Motorola MC83153 Raytheon 74153 TI SN74153	74194	Raytheon 74194 TI SN74194	7453	Hitachi HD2512 Motorola MC7453 Signetics N7453 TI SN7453		
74154	AMD SN74154 Motorola MC8311	74195	Raytheon 74195 TI SN74195	7454	Hitachi HD2514 Motorola MC7454 Signetics N7454 TI SN7454		
				746	National LM746 RCA CA3072		

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ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
Fairchild Semiconductor (cont)			75464	ITT National TI	ITT75464 DS75464 SN75464	9H01	National Signetics Signetics TI	DM74H01 N74H01 S54H01 SN54H01 SN74H01	9H21	TI TI	SN54H21 SN74H21
7491	Motorola Signetics TI	MC8391 N7491 SN7491A	75491	National TI	DS75491 SN75491	9H02	Motorola National National Signetics TI	MC54H22 MC74H22 DM54H22 DM74H22 N74H22 S54H22 SN54H22 SN74H22	9H22	Motorola Motorola National National Signetics TI	MC54H22 MC74H22 DM54H22 DM74H22 N74H22 S54H22 SN54H22 SN74H22
7492	Hitachi Motorola Signetics TI	HD2521 MC8392 N7492 SN7492A	75492	National TI	DS75492 SN75492	9H04	Motorola Motorola National National Signetics Signetics TI	MC54H04 MC74H04 DM54H04 DM74H04 N74H04 S54H04 SN54H04 SN74H04	9H30	Motorola Motorola National National Signetics TI	MC54H30 MC74H30 DM54H30 DM74H30 N74H30 S54H30 SN54H30 SN74H30
7493	Hitachi Motorola Signetics TI	HD2520 MC8393 N7493 SN7493A	758	Exar Sprague	XR1800 ULN-2244	9H05	Motorola Motorola National National Signetics Signetics TI	MC54H05 MC74H05 DM54H05 DM74H05 N74H05 S54H05 SN54H05 SN74H05	9H40	Motorola Motorola National National Signetics TI	MC54H40 MC74H40 DM54H40 DM74H40 N74H40 S54H40 SN54H40 SN74H40
7494	Motorola Signetics TI	MC8394 N7494 SN7494	760	National	LM160	9H08	Motorola Motorola National National Signetics Signetics TI	MC54H08 MC74H08 DM54H08 DM74H08 N74H08 S54H08	9H50	Motorola National National National Signetics TI	MC74H50 DM54H50 DM74H50 N74H50 S54H50 SN54H50 SN74H50
7495	Hitachi Motorola Signetics TI	HD2534 MC8395 N7495 SN7495A	763	National National	LM1496 LM1596	9H10	Motorola Motorola National National Signetics Signetics TI	MC54H10 MC74H10 DM54H10 DM74H10 N74H10 S54H10	9H51	Motorola Motorola National National Signetics TI	MC54H51 MC74H51 DM54H51 DM74H51 N74H51 S54H51 SN54H51 SN74H51
7496	Motorola Signetics TI	MC8396 N7496 SN7496	767	National Sprague	LM360 ULN-2128	9H101	Motorola Motorola National National Signetics Signetics TI	MC54H101 MC74H101 DM54H101 DM74H101 N74H101 S54H101	9H52	Motorola Motorola National National Signetics TI	MC54H52 MC74H52 DM54H52 DM74H52 N74H52 S54H52 SN54H52 SN74H52
75107	ITT	ITT75107	776	Harris Motorola National Silicon G	HA-2720 MC1776 LM4250 SG1250	9H102	Motorola Motorola National National Signetics Signetics TI	MC54H102 MC74H102 DM54H102 DM74H102 N74H102 S54H102	9H53	Motorola Motorola National National Signetics TI	MC54H53 MC74H53 DM54H53 DM74H53 N74H53 S54H53 SN54H53 SN74H53
75108	ITT	ITT75108	777	Intersil Motorola National Silicon G TI	777 MLM101 LM101 SG777 SN52777	9H103	Motorola Motorola National National Signetics Signetics TI	MC54H103 MC74H103 DM54H103 DM74H103 N74H103 S54H103	9H54	Motorola Motorola National National Signetics TI	MC54H54 MC74H54 DM54H54 DM74H54 N74H54 S54H54
75109	ITT	ITT75109	780	RCA Sprague	CA3070 ULN-2124	9H106	National National National National Signetics Signetics TI	DM54H106 DM74H106 N74H106 S54H106 SN54H106 SN74H106	9H55	Motorola Motorola National National Signetics TI	MC54H55 MC74H55 DM54H55 DM74H55 N74H55 S54H55 SN54H55 SN74H55
75110	ITT	ITT75110	7800	Silicon G	SG7800	9H108	Motorola Motorola National National Signetics Signetics TI	MC54H108 MC74H108 DM54H108 DM74H108 N74H108 S54H108 SN54H108 SN74H108	9H60	Motorola Motorola National National Signetics TI	MC54H60 MC74H60 DM54H60 DM74H60 N74H60 S54H60 SN54H60 SN74H60
75234	ITT	ITT75234	7805	Motorola National Silicon G TI	MC7805 LM340-5 SG7805 SN72905	9H11	Motorola Motorola National National Signetics Signetics TI	MC54H11 MC74H11 DM54H11 DM74H11 N74H11 S54H11 SN54H11 SN74H11	9H61	Motorola Motorola National National Signetics TI	MC54H61 MC74H61 DM54H61 DM74H61 N74H61 S54H61 SN54H61 SN74H61
75235	ITT	ITT75235	7806	Motorola National Silicon G TI	MC7806 LM340-6 SG7806 SN72906	9H21	Motorola Motorola National National Signetics Signetics TI	MC54H21 MC74H21 DM54H21 DM74H21 N74H21 S54H21 SN54H21 SN74H21	9H62	Motorola Motorola	MC54H62 MC74H62
7524	ITT Motorola National Signetics TI	ITT7524 MC7524 DS7524 N7524 SN7524	7808	Motorola National Silicon G TI	MC7808 LM340-8 SG7808 SN72908						
7525	ITT Motorola National Signetics TI	ITT7525 MC7525 DS7525 N7525 SN7525	781	RCA Sprague	CA3071 ULN-2127						
753	Sprague	ULN-2209	7812	Motorola National Silicon G TI	MC7812 LM340-12 SG7812 SN72912						
75325	Motorola National TI	MC75325 DS75325 SN5325	7815	Motorola National Silicon G TI	MC7815 LM340-15 SG7815 SN72915						
754	National	LM1596	7818	Motorola National Silicon G TI	MC7818 LM340-18 SG7818 SN72918						
75450	ITT National Signetics Teledyne S TI	ITT75450 DS75450 75450 75450 SN75450	7824	Motorola National Silicon G TI	MC7824 LM340-24 SG7824 SN72924						
75451	ITT National Signetics Teledyne S TI	ITT75451 DS75451 75451 75451 SN75451	795	Lithic Sys Lithic Sys	LS1495 LS1595						
75452	ITT National Signetics Teledyne S TI	ITT75452 DS75452 75452 75452 SN75452	796	Lithic Sys Lithic Sys Motorola National	LS1496 LS1596 MC1496 LM1496						
75453	National Signetics Teledyne S TI	DS75453 75453 75453 SN75453	8T13	National TI	DS55121 SN55121						
75454	ITT National Signetics Teledyne S TI	ITT75454 DS75454 75454 75454 SN75454	8T14	National TI	DS55122 SN55122						
75460	ITT National Teledyne S TI	ITT75460 DS75460 75460 SN75460	8T23	National TI	DS75123 SN75123						
75461	ITT National Teledyne S TI	ITT75461 DS75461 75461 SN75461	8T24	National TI	DS75124 SN75124						
75462	ITT National Teledyne S TI	ITT75462 DS75462 75462 SN75462	9H00	Motorola Motorola National National Signetics Signetics TI	MC54H00 MC74H00 DM54H00 DM74H00 N74H00 S54H00 SN54H00 SN74H00						
75463	National Teledyne S TI	DS75463 75463 SN75463	9H01	Motorola Motorola National	MC54H01 MC74H01 DM54H01						

† Discontinued

The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device
Fairchild Semiconductor (cont)		9LS151	Raytheon 54LS151 see page 282	9N00	Motorola MC5400 Motorola MC7400 National DM7400 Signetics N7400 Signetics S5400 TI SN5400 TI SN7400	9N11	National DM7411 Signetics N7411 Signetics S5411
9H62	National DM54H62 National DM74H62 Signetics N74H62 Signetics S54H62 TI SN54H62 TI SN74H62	9LS152	Raytheon 54LS152 see page 282	9N01	Motorola MC5401 Motorola MC7401 National DM7401 Signetics N7401 Signetics S5401 TI SN5401 TI SN7401	9N12	Motorola MC5412 TI SN5412 TI SN7412
9H71	Motorola MC54H71 Motorola MC74H71 National DM54H71 National DM74H71 Signetics N74H71 Signetics S54H71 TI SN54H71 TI SN74H71	9LS153	Raytheon 54LS153 see page 282	9N02	Motorola MC7402 National DM7402 Signetics N7402 Signetics S5402 TI SN5402 TI SN7402	9N122	National DM74122 TI SN54122 TI SN74122
9H72	Motorola MC54H72 National DM54H72 National DM74H72 Signetics N74H72 Signetics S54H72 TI SN54H72 TI SN74H72	9LS154	Raytheon 54LS154 see page 282	9N03	Motorola MC5403 Motorola MC7403 National DM7403 Signetics N7403 Signetics S5403 TI SN5403 TI SN7403	9N123	National DM74123 TI SN54123 TI SN74123
9H73	Motorola MC54H73 National DM54H73 National DM74H73 Signetics N74H73 Signetics S54H73	9LS155	Raytheon 54LS155 see page 282	9N04	Motorola MC5404 Motorola MC7404 National DM7404 Signetics N7404 Signetics S5404 TI SN5404 TI SN7404	9N13	National DM7413 TI SN5413 TI SN7413
9H74	Motorola MC54H74 Motorola MC74H74 National DM54H74 National DM74H74 Signetics N74H74 Signetics S54H74 TI SN54H74 TI SN74H74	9LS156	Raytheon 54LS156 see page 282	9N05	Motorola MC5405 Motorola MC7405 National DM7405 Signetics N7405 Signetics S5405 TI SN5405 TI SN7405	9N132	National DM74132 TI SN54132 TI SN74132
9H76	National DM54H76 National DM74H76 Signetics N74H76 Signetics S54H76 TI SN54H76 TI SN74H76	9LS157	Raytheon 54LS157 see page 282	9N06	Motorola MC5406 Motorola MC7406 National DM7406 Signetics N7406 Signetics S5406 TI SN5406 TI SN7406	9N14	National DM7414 TI SN5414 TI SN7414
9H78	National DM54H78 National DM74H78 TI SN54H78 TI SN74H78	9LS158	Raytheon 54LS158 see page 282	9N07	Motorola MC5407 Motorola MC7407 National DM7407 Signetics N7407 Signetics S5407 TI SN5407 TI SN7407	9N16	Motorola MC5416 Motorola MC7416 National DM7416 TI SN5416 TI SN7416
9LA38	Raytheon 54LS38 see page 282	9LS159	Raytheon 54LS159 see page 282	9N08	Motorola MC5408 Motorola MC7408 National DM7408 Signetics N7408 Signetics S5408 TI SN5408 TI SN7408	9N17	Motorola MC7417 Motorola MC9417 National DM7417 TI SN5417 TI SN7417
9LD27	Raytheon 54LS27 see page 282	9LS160	Raytheon 54LS160 see page 282	9N09	Motorola MC5409 Motorola MC7409 National DM7409 Signetics N7409 Signetics S5409 TI SN5409 TI SN7409	9N20	Motorola MC5420 Motorola MC7420 National DM7420 Signetics N7420 Signetics S5420 TI SN5420 TI SN7420
9LS00	Raytheon 54LS00 see page 282	9LS161	Raytheon 54LS161 see page 282	9N10	Motorola MC5410 Motorola MC7410 National DM7410 Signetics S5410 TI SN5410 TI SN7410	9N23	Motorola MC5423 Motorola MC7423 National DM7423 TI SN5423 TI SN7423
9LS02	Raytheon 54LS02 see page 282	9LS162	Raytheon 54LS162 see page 282	9N107	Motorola MC54107 Motorola MC74107 National DM74107 Signetics N74107 Signetics S54107 TI SN54107 TI SN74107	9N25	Motorola MC5425 Motorola MC7425 National DM7425 TI SN5425 TI SN7425
9LS03	Raytheon 54LS03 see page 282	9LS163	Raytheon 54LS163 see page 282			9N26	Motorola MC5426 Motorola MC7426 National DM7426 Signetics S5426 TI SN5426 TI SN7426
9LS04	Raytheon 54LS04 see page 282	9LS164	Raytheon 54LS164			9N27	Motorola MC5427 Motorola MC7427 National DM7427 TI SN5427 TI SN7427
9LS05	Raytheon 54LS05 see page 282	9LS174	Raytheon 54LS174 see page 282			9N30	Motorola MC5430 Motorola MC7430 National DM7430 Signetics N7430 Signetics S5430 TI SN5430 TI SN7430
9LS08	Raytheon 54LS08 see page 282	9LS175	Raytheon 54LS175			9N32	National DM7432 TI SN5432 TI SN7432
9LS10	Raytheon 54LS10 see page 282	9LS181	Raytheon 54LS181 see page 282			9N37	Motorola MC5437 Motorola MC7437 National DM7437 TI SN5437 TI SN7437
9LS109	Raytheon 54LS109 see page 282	9LS190	Raytheon 54LS190			9N38	Motorola MC5438 Motorola MC7438 National DM7438 TI SN5438 TI SN7438
9LS11	Raytheon 54LS11 see page 282	9LS191	Raytheon 54LS191 see page 282			9N40	Motorola MC5440 Motorola MC7440
9LS112	Raytheon 54LS112 see page 282	9LS192	Raytheon 54LS192 see page 282				
9LS113	Raytheon 54LS113 see page 282	9LS193	Raytheon 54LS193 see page 282				
9LS114	Raytheon 54LS114 see page 282	9LS194	Raytheon 54LS194A see page 282				
9LS132	Raytheon 54LS132	9LS195	Raytheon 54LS195A see page 282				
9LS136	Raytheon 54LS136 see page 282	9LS196	Raytheon 54LS196 see page 282				
9LS138	Raytheon 54LS138 see page 282	9LS199	Raytheon 54LS199 see page 282				
9LS139	Raytheon 54LS139 see page 282	9LS200	Raytheon 54LS200 see page 282				
9LS14	Raytheon 54LS14	9LS201	Raytheon 54LS201 see page 282				
9LS15	Raytheon 54LS15 see page 282	9LS202	Raytheon 54LS202 see page 282				
		9LS21	Raytheon 54LS21				
		9LS22	Raytheon 54LS22 see page 282				
		9LS251	Raytheon 54LS251 see page 282				
		9LS253	Raytheon 54LS253 see page 282				
		9LS257	Raytheon 54LS257 see page 282				
		9LS258	Raytheon 54LS258 see page 282				
		9LS266	Raytheon 54LS266 see page 282				
		9LS283	Raytheon 54LS283 see page 282				
		9LS295	Raytheon 54LS295A see page 282				
		9LS30	Raytheon 54LS30 see page 282				
		9LS32	Raytheon 54LS32 see page 282				
		9LS37	Raytheon 54LS37 see page 282				
		9LS40	Raytheon 54LS40 see page 282				
		9LS51	Raytheon 54LS51 see page 282				
		9LS54	Raytheon 54LS54 see page 282				
		9LS55	Raytheon 54LS55 see page 282				
		9LS670	Raytheon 54LS670				
		9LS74	Raytheon 54LS74 see page 282				
		9LS83	Raytheon 54LS83				
		9LS86	Raytheon 54LS86 see page 282				
		9LS95	Raytheon 54LS95B see page 282				

† Discontinued

ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
Fairchild Semiconductor (cont)			9N86	Signetics	N7486	9005	National	DM9005C	93S157	National	DM74S157
9N40	National	DM7440		Signetics	S5486		TI	SN29005		TI	SN54S167
	Signetics	N7440		TI	SN5486	9006	ITT	ITT9006		TI	SN74S167
	Signetics	S5440	9S00	National	DM74S00		Motorola	MC7460	93S16	AMD	93S16
	TI	SN5440		Signetics	N74S00	9007	National	DM9006C	93S21	AMD	93S21
	TI	SN7440		TI	SN54S00		TI	SN29007	93S22	AMD	93S22
9N50	Motorola	MC5450		TI	SN74S00	9008	ITT	ITT9008		National	DM74S22
	Motorola	MC7450	9S03	National	DM74S03		National	DM9008C		TI	SN54S157
	National	DM7450		Signetics	N74S03		TI	SN29008		TI	SN74S157
	Signetics	N7450		TI	SN54S03	9009	ITT	ITT9009	93S47	National	DM74S47
	Signetics	S5450		TI	SN74S03		Motorola	MC7440	93S48	AMD	93S48
	TI	SN5450	9S04	National	DM74S04		National	DM9009C	9300	AMD	9300
	TI	SN7450		Signetics	N74S04	9012	ITT	ITT9012		ITT	ITT9300
9N51	Motorola	MC5451		TI	SN54S04		National	DM9012C		Motorola	MC9300
	Motorola	MC7451		TI	SN74S04	9S05	ITT	SN29012		National	DM9300
	National	DM7451		National	DM74S05		ITT	ITT9016		Raytheon	RC9300
	Signetics	N7451		Signetics	N74S05		Motorola	MC7404		Raytheon	RM9300
	Signetics	S5451		TI	SN54S05		National	DM9016C		TI	SN54195
	TI	SN5451		TI	SN74S05	9017	ITT	ITT9017		TI	SN74195
	TI	SN7451	9S10	National	DM74S10		ITT	ITT9020	9301	AMD	9301
9N53	Motorola	MC5453		TI	SN54S10	9020	ITT	ITT9020		ITT	ITT9301
	Motorola	MC7453		TI	SN74S10		ITT	ITT9022		Motorola	MC9301
	National	DM7453	9S11	National	DM74S11	9022	ITT	ITT9022		National	DM9301
	Signetics	N7453		TI	SN54S11		ITT	ITT9024		TI	SN29301
	Signetics	S5453		TI	SN74S11	9024	National	DM74109		TI	SN29301
	TI	SN5453		TI	SN74S11		Signetics	N74109	9304	AMD	9304
	TI	SN7453	9S112	National	DM74S112		TI	SN54109		ITT	ITT9304
9N54	Motorola	MC5454		TI	SN54S112		TI	SN74109		Motorola	MC9304
	Motorola	MC7454		TI	SN74S112	9031	Signetics	N8252		Raytheon	RC9304
	National	DM7454		National	DM74S113	9033	Hitachi	HM2501		Raytheon	RM9304
	Signetics	N7454		TI	SN54S113		ITT	ITT9033	9306	AMD	9306
	Signetics	S5454		TI	SN74S113		TI	SN5481A		Motorola	MC9306
	TI	SN5454	9S114	National	DM74S114		TI	SN7481A			
	TI	SN7454		TI	SN54S114	9034	Fairchild	93434	9307	Motorola	MC9307
9N60	Motorola	MC5460		TI	SN74S114		Motorola	MCM4002			
	Motorola	MC7460		National	DM74S140		Signetics	N8224	9308	AMD	9308
	National	DM7460		TI	SN54S140		TI	SN5488A		ITT	ITT9308
	Signetics	N7460		TI	SN74S140		TI	SN7488A		Motorola	MC9308
	Signetics	S5460	9S15	National	DM74S15	9093	Hitachi	HD2211		Raytheon	RC9308
	TI	SN5460		TI	SN54S15		Raytheon	RM993		Raytheon	RM9308
	TI	SN7460		TI	SN74S15		SW	SW705		TI	SN29308
9N70	Motorola	MC5470		TI	SN74S15		TI	SN158093		TI	SN39308
	Motorola	MC7470	9S20	National	DM74S20		TI	SN159093	9309	AMD	9309
	National	DM7470		Signetics	N74S20	9094	Raytheon	RM994		Motorola	MC9309
	Signetics	N7470		TI	SN54S20		SW	SW708		National	DM9309
	Signetics	S5470		TI	SN74S20		TI	SN158094		TI	SN29309
	TI	SN5470	9S22	National	DM74S22		TI	SN159094		TI	SN39309
	TI	SN7470		Signetics	N74S22	9097	Raytheon	RM997	9310	AMD	9310
9N72	Motorola	MC5472		TI	SN54S22		SW	SW709		Motorola	MC8310
	Motorola	MC7472		TI	SN74S22		TI	SN158097		Motorola	MC9310
	National	DM7472	9S40	National	DM74S40		TI	SN159097		National	DM74160
	Signetics	N7472		Signetics	N74S40	9099	Hitachi	HD2210		Raytheon	RC9310
	Signetics	S5472		TI	SN54S40		Raytheon	RM999		Raytheon	RM9310
	TI	SN5472		TI	SN74S40		SW	SW706		TI	SN54160
	TI	SN7472	9S64	National	DM74S64		TI	SN158099		TI	SN74160
9N73	Motorola	MC5473		Signetics	N74S64	9157	SW	SN159099			
	Motorola	MC7473		TI	SN54S64		SW	SN957	9311	AMD	9311
	National	DM7473		TI	SN74S64		SW	SN958		ITT	ITT9311
	Signetics	N7473	9S65	National	DM74S65		AMD	93L00		Motorola	MC8311
	Signetics	S5473		Signetics	N74S65		AMD	93L01		Motorola	MC9311
	TI	SN5473		TI	SN54S65	93L01	AMD	93L01		Raytheon	RC9311
	TI	SN7473		TI	SN74S65	93L08	AMD	93L08		Raytheon	RM9311
9N74	Motorola	MC5474		TI	SN74S65	93L10	AMD	93L10		TI	SN54154
	Motorola	MC7474	9S74	National	DM74S74	93L11	AMD	93L11		TI	SN74154
	National	DM7474		ITT	ITT9000	93L12	AMD	93L12	9312	AMD	9312
	Raytheon	5474		ITT	ITT9001		AMD	93L14		ITT	ITT9312
	Signetics	N7474	9001	Motorola	MC3052		AMD	93L16		Motorola	MC9312
	Signetics	S5474		Motorola	MC9001	93L16	AMD	93L18		National	DM9312
	TI	SN5474		TI	SN29001	93L18	AMD	93L18		Raytheon	RC9312
	TI	SN7474		ITT	ITT9002	93L21	AMD	93L21		Raytheon	RM9312
9N75	Motorola	MC8375		Motorola	MC7400	93L22	AMD	93L22		Signetics	N8230
	TI	SN5475		National	DM9002C	93L24	AMD	93L24		TI	SN29312
	TI	SN7475		TI	SN29002	93L28	AMD	93L28	9314	AMD	9314
9N76	Motorola	MC5476		ITT	ITT9003	93L34	AMD	93L34		Motorola	MC9314
	Motorola	MC7476		Motorola	MC7410	93L38	AMD	93L38			
	National	DM7476		National	DM9003C	93L40	AMD	93L40	93141	National	DM74141
	Signetics	N7476		TI	SN29003		AMD	93L41		TI	SN74141
	Signetics	S5476	9004	ITT	ITT9004	93L41	AMD	93L41			
	TI	SN5476		Motorola	MC7420	93L60	AMD	93L60	93145	ITT	ITT74145
	TI	SN7476		National	DM9004C	93L66	AMD	93L66		Motorola	MC93145
9N86	National	DM7486		TI	SN29004	93S10	AMD	93S10		National	DM74145
	Raytheon	5486	9005	ITT	ITT9005	93S12	AMD	93S12		Raytheon	54145
				Motorola	MC7450	93S153	National	DM74S153		Raytheon	74145
										TI	SN54145

11 Discontinued

The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device
Fairchild Semiconductor (cont)		9317C	TI SN5446A SN7446A	93199	Raytheon TI SN54199 SN74199	93411	MMI Raytheon TI SN54S201 TI SN74S201
93145	TI SN74145	93170	National Raytheon TI SN54170 TI SN74170	9321	AMD 9321	93412	Intersil TI SN54S214 TI SN74S214
9315	Motorola MC8315 Motorola DM7441A National DM7741A Signetics N7441 TI SN74141	93174	AMD SN74174 National DM74174 Raytheon 54174 TI SN54174 TI SN74174	9322	AMD ITT ITT9322 Motorola MC8322 Motorola MC9322 National DM74157 Raytheon RC9322 Raytheon RM9322 Raytheon 54157 Raytheon 74157 TI SN54157 TI SN74157	93415	Intel see page 766, 769 Intersil IM5508 Raytheon RC5500 Raytheon RM5500 Signetics N82S10 see page 804, 806, 815, TI SN54S314 TI SN74S314
93150	ITT ITT74150 Motorola MC83150 Motorola MC93150 National DM74150 Raytheon 54150 Raytheon 74150 TI SN54150 TI SN74150	93175	AMD SN74175 National DM74175 Raytheon 54175 Raytheon 74175 TI SN54175 TI SN74175	9324	AMD 9324 Motorola MC9324	93416	Harris HPROM-1024A HPROM-1024A Intel 3601 see page 772, 773 Intersil IM5603 MMI 6300 National DM7573 National DM8573 Signetics N82S126 see page 804, 826, 835,
93151	ITT ITT74151 Motorola MC83151 Motorola MC93151 National DM74151 Raytheon 54151 Raytheon 74151 TI SN54151A TI SN74151A	93176	Motorola MC93176 National DM74176 TI SN54176 TI SN74176	9325	National DM74141 Signetics N74141 Signetics S54141 TI SN74141	93417	MMI 5300 National DN7573 TI SN54S387 TI SN74S387
93152	Motorola MC83152 Motorola MC93152 Raytheon 54152 Raytheon 74152 TI SN54152A	93177	Motorola MC83177 Motorola MC93177 National DM74177 TI SN54177 TI SN74177	9328	AMD 9328 ITT ITT9328 Motorola MC9328 Signetics N8277	9342	AMD 9342 ITT ITT74182 Motorola MC8342 Motorola MC9342 National DM74182 Raytheon RM9342 Raytheon 54182 Raytheon 74182 Signetics N74182 Signetics S54182 TI SN54182 TI SN74182
93153	ITT ITT74153 Motorola MC83153 Motorola MC93153 National DM74153 Raytheon 54153 Raytheon 74153 TI SN54153 TI SN74153	93178	Motorola MC83178 Motorola MC93178 TI SN54178 TI SN74178	9334	AMD 9334 Motorola MC9334 National DM9334 TI SN54259 TI SN74259	93421	Intersil IM5523 MMI 5531 MMI 6531 Raytheon RC5340 Raytheon RM5340 Signetics N82S16 see page 804, 806, 815, TI SN54S201 TI SN74S201
93155	National DM74155 Raytheon 54155 Raytheon 74155 TI SN54155 TI SN74155	93179	Motorola MC83179 Motorola MC93179 TI SN54179 TI SN74179	9338	AMD 9338	93425	Intel 2125 see page 766, 769
93156	National DM74156 Raytheon 54156 Raytheon 74156 TI SN54156 TI SN74156	93180	ITT ITT74180 Motorola MC83180 Motorola MC93180 National DM74180 Raytheon 54180 Raytheon 74180 TI SN54180 TI SN74180	9340	AMD 9340	93426	Harris HPROM-1024A Intersil IM5623 MMI 6301 National DM7574 National DM8574 Signetics N82S129 TI SN54S287 TI SN74S287
9316	AMD 9316 ITT ITT9316 Motorola MC8316 Motorola MC9316 National DM74161 Raytheon RC9316 Raytheon RM9316 TI SN54161 TI SN74161	93188	AMD 9318 Motorola MC9318 TI SN54148 TI SN74148	93403	AMD 93403 Intersil IM5501 MMI 6560 Motorola MCM4064 Motorola MC4064 National DM7489 Signetics N82S25 see page 804, 806, 814, TI SN7489	9343	Motorola MC4004 TI SN83433 TI SN93433
93163	Raytheon 54163 Raytheon 74163 TI SN54163 TI SN74163	93189	National DM74190 Raytheon 54190 Raytheon 74190 TI SN54190 TI SN74190	93406	Intersil IM5603 MMI 6200 Motorola MCM4006 National DM54187 National DM74187 Signetics N82S226 TI SN54187 TI SN74187	93434	Intersil IM5600 ITT ITT7488 ITT ITT7488A MMI 5230 MMI 6230 Motorola MCM4002 National DM5487 National DM7488 Signetics 8223 TI SN5488A TI SN7488A
93164	AMD SN74164 Motorola MC83164 Motorola MC93164 National DM74164 TI SN54164 TI SN74164	93191	National DM74191 Raytheon 54191 Raytheon 74191 TI SN54191 TI SN74191	93407	ITT ITT7481 Motorola MC4004 Motorola MC4304 TI SN5481A TI SN7481A	93435	MMI 5560
93165	ITT ITT74165 Motorola MC83165 National DM74165 Raytheon 54165 Raytheon 74165 TI SN54165 TI SN74165	93194	AMD SN74194 National DM74194 Raytheon 54194 Raytheon 74194 TI SN54194 TI SN74194	9341	AMD 9341 ITT ITT74181 Motorola MC8341 Motorola MC9341 National DM74181 Raytheon RC9341 Raytheon RM9341 Raytheon 54181 Raytheon 74181 Signetics N74181 Signetics S54181 TI SN54181 TI SN74181	93436	Motorola MC4004 TI SN83433 TI SN93433
93166	National DM74166 Raytheon 54166 Raytheon 74166 TI SN54166 TI SN74166	93196	Motorola MC7280 National DM74196 TI SN54196 TI SN74196	93410	Motorola MCM4056 Signetics N74S301 see page 804, 806, 815, Signetics N93410 Signetics S54S301 see page 804, 806, 815, Signetics S93410 TI SN54S301 TI SN74S301	93437	Motorola MC4004 TI SN83433 TI SN93433
9317B	National DM7447 TI SN5447A TI SN7447A	93197	Motorola MC8280 National DM74197 TI SN54197 TI SN74197	93411	Intersil IM5533 MMI MM16531 MMI 5530		
9317C	National DM7446	93199	National DM74199				

† Discontinued

ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
Fairchild Semiconductor (cont)			9360	National	DM74192	9393	Signetics	S5493	9933	TI	SN15833
93435	MMI	6560	Raytheon	RC9360		TI	SN5493	TI	TI	SN15933	
	Motorola	MC4064	Raytheon	RM9360		TI	SN7493		9935	Hitachi	HD2208
	TI	SN7489	Raytheon	54192		ITT	ITT7494	Raytheon	Raytheon	RM935	
93436	Intel	3602	Raytheon	74192		Motorola	MC8394	SW	TI	SN935	
	see page 774, 775		Signetics	N74192		Motorola	MC9394	TI	TI	SN15835	
	Intersil	IM5604	Signetics	S54192		Signetics	N7494	TI	TI	SN15935	
	MMI	5205	TI	SN54192		Signetics	S5494		9936	Hitachi	HD2206
	MMI	6205	TI	SN74192	9366	TI	SN5494	Raytheon	SW	SW936	
	TI	SN54S270	TI	SN74S270	AMD	TI	SN7494	TI	TI	SN15836	
	TI	SN74S270	ITT	ITT74193	Motorola	Motorola	MC8395	TI	TI	SN15936	
93438	TI	SN54S475	Motorola	MC8366	Motorola	Motorola	MC9395		9937	Raytheon	RM937
	TI	SN74S475	Motorola	MC9366	National	National	DM7495	Raytheon	SW	SW937	
93446	Intel	3622	National	DM74193	Signetics	Signetics	N7495	TI	TI	SN15839	
	see page 774, 775		Raytheon	RM9366	Signetics	Signetics	S5495	TI	TI	SN15937	
93448	TI	SN54S474	Raytheon	54193	TI	TI	SN5495		9941	Raytheon	RM941
	TI	SN74S474	Raytheon	74193	ITT	ITT7496	SN7495	SW	TI	SW941	
9345	ITT	ITT7445	Signetics	N74192	Motorola	Motorola	MC8396	TI	TI	SN15841	
	Motorola	MC9345	TI	S54192	Motorola	Motorola	MC9396	TI	TI	SN15941	
	National	DM7445	TI	SN54193	Motorola	National	DM7496		9944	Hitachi	HD2209
	Raytheon	5445	9375	ITT	ITT7475	Signetics	N7496	Hitachi	Raytheon	RM944	
	Raytheon	7445	Motorola	MC9375	Motorola	Signetics	S5496	SW	TI	SN944	
	Signetics	N7445	National	DM7475	National	Signetics	S5496	TI	TI	SN15844	
	Signetics	S5445	Signetics	S5475	Signetics	TI	SN5496	TI	TI	SN15944	
	TI	SN5445	TI	SN5475	95H90	Plessey	SP640	9945	Hitachi	HD2205	
	TI	SN7445	TI	SN7475	95H91	Plessey	SP641	Raytheon	SW	RM945	
9349	Raytheon	54180	9377	Motorola	MC8377	95H92	Plessey	SP642	SW	SW945	
	Raytheon	74180	Motorola	MC9377	Motorola	95H93	Plessey	SP643	TI	SN15845	
	Signetics	N74180	ITT	ITT7480	Motorola	9600	AMD	9600	TI	SN15945	
	Signetics	S54180	Motorola	MC8380	Motorola	9601	AMD	9601	Hitachi	HD2203	
	TI	SN54180	Motorola	MC9380	ITT	ITT9601	ITT	ITT9601	Raytheon	RM946	
	TI	SN74180	Signetics	N7480	Motorola	Motorola	MC9601	TI	TI	SN15846	
9352	ITT	ITT7442	Signetics	S5480	Motorola	National	DM9601	TI	TI	SN15946	
	Motorola	MC8352	TI	SN5480	Raytheon	Raytheon	RF8601		9948	Raytheon	RM948
	Motorola	MC9352	9382	ITT	ITT7482	TI	RF9601	SW	TI	SN948	
	National	DM7442	Motorola	MC8382	Motorola	ITT	ITT9602	TI	TI	SN15848	
	Signetics	N7442	Motorola	MC9382	Motorola	ITT	ITT9602	TI	TI	SN15849	
	Signetics	S5442	National	DM7482	National	National	DM9602	TI	TI	SN15949	
	TI	SN5442	TI	SN5482	TI	Raytheon	RF8602		9950	Raytheon	RM950
	TI	SN7442	TI	SN7482	9383	Raytheon	RF9602	SW	TI	SN950	
9353	ITT	ITT7443	ITT	ITT7483	Motorola	ITT	ITT74121	TI	TI	SN15850	
	Motorola	MC8353	Motorola	MC8383	Motorola	Motorola	MC8603		9951	Raytheon	RM951
	Motorola	MC9353	Motorola	MC9383	Motorola	Motorola	MC9603	SW	TI	SN951	
	Signetics	N7443	National	DM7483	National	Signetics	N74121	TI	TI	SN15851	
	Signetics	S5443	Signetics	N7483	Signetics	Signetics	S54121	TI	TI	SN15951	
	TI	SN5443	TI	SN5483	TI	TI	SN54121		9961	Raytheon	RM961
	TI	SN7443	TI	SN7483	9614	AMD	9614	SW	TI	SN961	
9354	ITT	ITT7444	9385	National	DM7485	ITT	ITT9614	TI	TI	SN15861	
	Motorola	MC8354	ITT	ITT7490	ITT	ITT9615	TI	TI	TI	SN15961	
	Motorola	MC9354	Motorola	MC8390	ITT	ITT9615		9962	Hitachi	HD2207	
	Signetics	N7444	Motorola	MC9390	TI	SN55114		Raytheon	RM962		
	Signetics	S5444	National	DM7490	9616	AMD	9616	SW	TI	SN962	
	TI	SN5444	Signetics	N7490	9617	AMD	9617	TI	TI	SN15862	
	TI	SN7444	Signetics	S5490	9620	AMD	9620	TI	TI	SN15962	
9355	Motorola	MC8355	TI	SN5490	9621	AMD	9621		9963	Raytheon	RM963
9357	Motorola	MC8357	9390	ITT	ITT7491	Raytheon	RC9621	SW	TI	SN963	
	Motorola	MC9357	Motorola	MC8391	Motorola	Raytheon	RM9621	TI	TI	SN15863	
9357A	ITT	ITT7446A	Motorola	MC9391	National	9622	Raytheon	RC9622	TI	SN15963	
	Motorola	MC9357A	Motorola	MC9391	National	Raytheon	RM9622	TI			
	National	DM7446A	National	DM7491	Signetics	9664	Signetics	N7524			
	Signetics	N7446	Signetics	N7491	Signetics	9665	Signetics	N7525			
	TI	SN5446A	TI	SN7491	98176	Motorola	MC83176				
	TI	SN7446A	9391	ITT	ITT7491	9930	Hitachi	HD2204			
9357B	ITT	ITT7447A	Motorola	MC8391	Motorola	Raytheon	RM930				
	Motorola	MC9357B	Motorola	MC9391	Motorola	SW	SW930				
	National	DM7447A	National	DM7491	National	TI	SN15830				
	Signetics	N7447	Signetics	N9392	Signetics	TI	SN15930				
	TI	SN5447A	TI	S9392	TI	9932	Hitachi	HD2201			
	TI	SN7447A	TI	SN5492	9933	Raytheon	RM932				
9358	ITT	ITT7448	TI	SN7492	Hitachi	SW	SW932				
	Motorola	MC8358	9392	ITT	ITT7492	TI	SN15832				
	Motorola	MC9358	Motorola	MC8392	Motorola	TI	SN15932				
	National	DM7448	Motorola	MC9392	Motorola	9933	Hitachi	HD2202			
	Signetics	N7448	National	DM7492	Motorola	Raytheon	RM933				
	TI	SN5448	Signetics	N9392	National	SW	SN933				
	TI	SN7448	TI	SN5492	Signetics	9933	SW	SN933			
9359	Motorola	MC8359	TI	SN7492	9393	ITT	ITT7493				
	Motorola	MC9359	9393	ITT	ITT7493	Motorola	MC8393				
9360	AMD	9360	Motorola	MC8393	Motorola	MC8393	MC8393				
	ITT	ITT74192	Motorola	MC9393	Motorola	MC8360	MC8360				
	Motorola	MC8360	National	DM7493	National	DM7493	DM7493				
	Motorola	MC9360	Signetics	N7493	Signetics	N7493	N7493				

General Instrument			
AY5-1012	TI		TMS6011
AY5-1013	AMI		S1003
	see page 533		
	TI		S1883
AY5-9100	Plessey		MP 9100
AY5-9200	Plessey		MP 9200
DL9-1402	Signetics		2502
RA3-1217	EMM/Semi		1217
RA3-1218	EMM/Semi		1218
RA3-4402	EMM/Semi		4402
	see page 734		
RA3-4256	EMM/Semi		RA3-4256
RA9-1101	Intersil		IM7501
	Intersil		IM7511

† Discontinued

The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device
Harris Semiconductor (cont)							
HPROM1024A	TI SN54S387 TI SN74S387	2102	Intersil IM7552 Mostek MK4102 Motorola MCM2102 National MM2102 Signetics 2602 see page 790	3601	see page 772, 773 Fairchild 93416 Harris HPROM-1024A Intersil IM5603 MMI 6300 National DM7573 National DM8573 Signetics N82S126 see page 804, 826, 835, TI SN54S387 TI SN74S387	AH0164	Siliconix DG164 see page 551
HPROM2048	Fairchild 93446 Intersil IM5624 Signetics N82S131 see page 804, 826, 838,	2104	see page 752, 759 Fairchild 4066 Mostek MK4096 see page 778, 781	3602	see page 774, 775 Fairchild 93436	DG111	Siliconix DGM111 see page 557, 558
HPROM2048A	AMD AM27S08 Fairchild 93436 Signetics N82S130 see page 804, 826, 838,	2107	AMI S4021 see page 722 TI TMS4030 TI TMS4060 Western RM1701	3604	see page 776, 777 MMI 6340	DG116	Siliconix DG116
HPROM8256	Intersil IM5600 MMI 5330 MMI 6330 National DM7577 National DM8577 Signetics N82S23 see page 804, 826, 828, TI SN54S188 TI SN54188 TI SN74S188 TI SN74188	2107B	see page 760, 765 TI TMS4060	3622	see page 774, 775 Fairchild 93446	DG118	Siliconix DG172 see page 557, 558
Intel		2111	AMD 2111 EA EA2111 Synertek SY2111 TI TMS4042	4001	National INS4001	DG123	Siliconix DG123 see page 551
INL3212	TI SN54S412 TI SN74S412	2112	AMD 2112 EA EA2112 Synertek SY2112 TI TMS4043	4002	National INS4002	DG125	Siliconix DG125 see page 551
INT3601	MMI 5300	2113	Synertek SY2113	4003	National INS4003	DG126	Siliconix DG126 see page 551
1101	AMD 1101 Intersil IM7501 Intersil IM7511 Mostek MK4007 National MM1101 Signetics 1101 Signetics 2501	2146	AMI S146	4004	National INS4003	DG129	Siliconix DG129 see page 551
1103	AMI S1103 see page 707 AMI S1103A see page 712 AMI S146 Fairchild 1103 Hitachi HM3503 Nortec 1103 Rockwell 1103 Synertek SY1103 TI TMS1103	2308	EA EA2308	4008	National INS4008	DG134	Siliconix DG134 see page 551
1301	AMI S8773	2316	EMM/Semi RO3-8316 GI RO3-8316 Mostek MK31000 see page 783	4009	National INS4009	DG139	Siliconix DG139 see page 551
1402	AMD 1402 AMI S2502A Nortec 1402 Signetics 2502 Synertek SY1402	2401	Synertek SY2401	4702	AMD 4702 National 4702	DG141	Siliconix DG141 see page 551
1403	AMD 1403 Nortec 1403 Signetics 2503 Synertek SY1403	2405	AMI S1685 Synertek SY2405	5201	SSS SCL5424	DG142	Siliconix DG142 see page 551
1404	AMD 1404 Nortec 1404 Signetics 2504 Synertek SY1404	3002	Signetics N3002 see page 1006	5801	SSS SCL5437	DG143	Siliconix DG143 see page 551
1405	AMD 1405 Signetics 2505	3101	AMD 3101 Intersil IM5501 MMI 5560 MMI 6560 Signetics N82S25 see page 804, 806, 814,	8000	see page 958 AMD 9080 TI TMS8080	DG144	Siliconix DG144 see page 551
1406	AMD 1406	3102	Fairchild 93400	8212	see page 960 TI SN54S412 TI SN74S412	DG145	Siliconix DG145 see page 551
1407	AMD 1407	3104	Fairchild 93402	8308	see page 960 EA EA8308	DG146	Siliconix DG146 see page 551
1504	AMI S1685	3106	Fairchild 93421 Intersil IM5523 MMI 6531 Raytheon RC5340 Raytheon RM5340 Signetics 82S16 TI SN54S201 TI SN74S201	8316	see page 960 GI RO3-8316	DG151	Siliconix DG151 see page 551
1506	AMD 1506	3107	Fairchild 93411 Intersil IM5533 MMI 5530 MMI 6530 Raytheon RC5330 Raytheon RM5330 Signetics N74S01 Signetics S82S17 Signetics 82S17 TI SN54S301 TI SN74S301	8702	AMD 8702 National 8702	DG152	Siliconix DG152 see page 551
1507	AMD 1507	3110	TI SN74S209	8702	AMD 8702 National 8702	DG153	Siliconix DG153 see page 551
1602	AMD 1602 National 1602	3202	Fairchild 93401	Intersil		DG154	Siliconix DG154 see page 551
1702	AMD 1702 National 1702	3301	AMD 74186 Fairchild 93406 Intersil IM5603 MMI H6200 MMI 5200 National DM54187 National DM74187 TI SN54187 TI SN74187	AH0126	Siliconix DG126 see page 551	DG161	Siliconix DG161 see page 551
2101	AMD 2101 EA EA2101 Hitachi HM2101 National MM2101 Synertek SY2101 TI TMS2101	33011	MMI H5200	AH0129	Siliconix DG129 see page 551	DG162	Siliconix DG162 see page 551
2102	AMD 2102 AMD 9102 EA 2102 Fairchild 2102	3304	MMI 6340	AH0133	Siliconix DG133 see page 551	DG163	Siliconix DG163 see page 551
				AH0134	Siliconix DG134 see page 551	DG164	Siliconix DG164 see page 551
				AH0139	Siliconix DG139 see page 551	DG182	Siliconix DG182 see page 552, 554
				AH0140	Siliconix DG140 see page 551	DG185	Siliconix DG182 see page 552, 554
				AH0141	Siliconix DG141 see page 551	DG188	Siliconix DG188 see page 552, 554
				AH0142	Siliconix DG142 see page 551	DG191	Siliconix DG191 see page 552, 554
				AH0143	Siliconix DG143 see page 551	DG426	Siliconix DG126 see page 551
				AH0144	Siliconix DG144 see page 551	DG464	Siliconix DG164 see page 551
				AH0145	Siliconix DG145 see page 551	D123	Siliconix D123
				AH0146	Siliconix DG146 see page 551	D125	Siliconix D125
				AH0151	Siliconix DG151 see page 551	G115	Siliconix G115
				AH0152	Siliconix DG152 see page 551	G116	Siliconix G116
				AH0153	Siliconix DG153 see page 551	G117	Siliconix G117
				AH0154	Siliconix DG154 see page 551	G118	Siliconix G118
				AH0161	Siliconix DG161 see page 551	G119	Siliconix G119
				AH0162	Siliconix DG162 see page 551	G123	Siliconix G123
				AH0163	Siliconix DG163 see page 551	G125	Siliconix G125
						G126	Siliconix G126
						G127	Siliconix G127
						G128	Siliconix G128
						G129	Siliconix G129
						G130	Siliconix G130
						G131	Siliconix G131
						G132	Siliconix G132
						IH5009	AMI MX52 National AH5009

Discontinued

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IC UPDATE MASTER

Manufacturer Device Replacement Source Device			Manufacturer Device Replacement Source Device			Manufacturer Device Replacement Source Device			Manufacturer Device Replacement Source Device		
Intersil (cont)											
IH5010	AMI National	MX52 AH5010	IM5600	TI	SN74S188	IM7712	Nortec Signetics	2512 2512	555	Lithic Sys National	LS555 LM555
IH5040	Harris	HI5040	IM5602	MMI	6340	IM7722	AMD Signetics	AM2808 2525		Raytheon Raytheon Teledyne S	RC555 RM555 555
IH5042	Harris Siliconix	HI5042 06188	IM5603	Fairchild Harris Intel	93416 HPROM-1024A 3601	IM7780	Mostek Signetics TI	MK1007 2532 TMS3409	723	National Raytheon Raytheon RCA Teledyne S	LM723 RC723 RM723 CA723 723
IH5043	Siliconix	DG191		MMI	5300	LM101	Teledyne S	LM101			
	see page 552, 554			MMI	6300	LM105	Teledyne S	LM105			
IH5044	Harris	HI5044		National	DM7573	LM107	Teledyne S	LM107	741	AD	AD741
IH50441	Harris	HI5041		National	DM8573	LM111	Teledyne S	LM111		see page 625	
IH5045	Harris Siliconix	HI5045 DG185	IM5604	Fairchild Intel	93436 3602	LM201	Teledyne S	LM201		Fairchild	741
	see page 552, 554			Intel	see page 774, 775	LM205	Teledyne S	LM205		National PMI	LM741 SSS741
IH5046	Harris	HI5046		MMI	5305	LM207	Teledyne S	LM207		Raytheon Raytheon RCA	RC741 RM741 CA741
IH5047	Harris	HI5047		MMI	6305	LM211	Teledyne S	LM211		see page 661	
IH5048	Siliconix	DG181		Signetics	N82S130	LM301	Teledyne S	LM301		Teledyne S	741
	see page 552, 554			see page 804, 826, 838,		LM305	Teledyne S	LM305			
IH5049	Harris Siliconix	HI5049 DG184	IM5605	Intel	3604	LM307	Teledyne S	LM307	747	RCA	CA747
	see page 552, 554			see page 776, 777		LM311	Teledyne S	LM311		see page 661	
IH5050	Harris Siliconix	HI5050 DG187		MMI	6340	LM723	Teledyne S	723	748	Fairchild National Raytheon Raytheon RCA Teledyne S	748 LM748 RC748 RM748 CA748 748
	see page 552, 554			TI	SN54S475	LM741	Teledyne S	741			
IH5051	Harris Siliconix	HI5051 DG190	IM5610	Harris	HM7603	LM748	Teledyne S	748	8007	AD	AD8007
	see page 552, 554			see page 746		MM452	Siliconix	S1452	8013	AD	AD530
IH5070	AD	AD7507		MMI	5331	MM455	Siliconix	S1455		AD	AD533
	see page 548			MMI	6331	MM552	Siliconix	S1552			
	Harris	HI507		Signetics	N82S123	MM555	Siliconix	S1555	NE555	Lithic Sys RCA	LS555 CA555
	Siliconix	DG507		see page 804, 826, 828,		SE555	Lithic Sys RCA	LS555 CA555		see page 661	
	see page 561, 563, 564,			TI	SN54S288	SSS1458	RCA	CA1458	8038	Lithic Sys	LS8038
				TI	SN74S288	SSS1558	RCA	CA1558	8101	RCA	CA748
IM5501	AMD	IM5501	IM5623	Fairchild	93426	101	AD	101A	8201	RCA	CA748
	MMI	5560		Harris	HPROM-1024		National	LM101	8741	RCA	CA741
	MMI	6560		Intel	3621		Raytheon	LM101		see page 661	
	TI	SN54S289		see page 772, 773			RCA	CA101			
	TI	SN74S289		MMI	5301		Teledyne S	LM101			
IM5502	TI	SN5481A		MMI	6301	107	RCA	CA107			
IM5503	MMI	6531		National	DM7574	108	see page 661				
	Signetics	N74S301		National	DM8574		AD	AD108			
	see page 804, 806, 815,			Signetics	N82S129		National	LM108			
	Signetics	N82S17		TI	SN54S287		Raytheon	LM108			
	see page 804, 806, 815,			TI	SN74S287		Teledyne S	LM101			
	TI	SN54S301		IM5624	Fairchild	93446		RCA	CA107		
	TI	SN74S301			Harris	HM7621		see page 661			
IM5508	Fairchild	93415		see page 746		Intel	3622	see page 661			
	Signetics	N82S1Q		see page 774, 775		MMI	5306	AD	AD108		
	see page 804, 806, 818,			MMI	6306		Signetics	N82S131			
	TI	SN74S209		see page 804, 826, 838,		Signetics	N82S131				
IM5512	TI	SN5481A		IM5625	Intel	3624		see page 661			
IM5523	Fairchild	93421			see page 776, 777		AD	201A			
	MMI	5531		MMI	6341	201	National	LM201			
	MMI	6531		TI	SN54S474		Raytheon	LM201			
	Raytheon	RC5340		TI	SN74S474		RCA	CA201			
	Raytheon	RC5540		IM5640	Harris	HM7620		see page 661			
	Raytheon	RM5340			see page 746		RCA	CA748			
	Signetics	N82S16		IM6100	Harris	HM6100		Teledyne S	LM201		
	see page 804, 806, 815,				see page 938		207	RCA	CA207		
	Signetics	S82S16			Harris	HM6100A		see page 661			
	TI	SN54S201			see page 938		208	AD	AD208		
	TI	SN74S201						see page 625			
IM5533	Fairchild	93411		IM7051	AMD	1101		National	LM208		
	MMI	5530			Signetics	2501		Raytheon	LM208		
	MMI	6530			Signetics	2602		RCA	CA208		
	Raytheon	RC5330			see page 790		211	RCA	CA211		
	Raytheon	RM5330						see page 661			
	Signetics	N82S17		IM7501	Mostek	MK4007					
	see page 804, 806, 815,										
	TI	SN54S301		IM7511	Mostek	MK4007		AD	301A		
	TI	SN74S301						National	LM301		
IM5543	Fairchild	93421		IM7512	Mostek	MK4007		Raytheon	LM301		
	TI	SN54S301						RCA	CA301		
	TI	SN74S301		IM7552	Mostek	MK4102		see page 661			
IM5553	Fairchild	93411			TI	TMS4033		Teledyne S	LM301		
IM5600	Fairchild	93434			TI	TMS4034		207	RCA	CA307	
	Harris	HPROM-8256			TI	TMS4035		see page 661			
	MMI	5330		IM7702	Nortec	1402		308	AD	AD308	
	MMI	6330			Signetics	2502		see page 625			
	National	DM7577		IM7703	Nortec	1403		National	LM308		
	National	DM8577			Signetics	2503		Raytheon	LM308		
	Signetics	N82S23		IM7704	Nortec	1404		Teledyne S	LM308		
	see page 804, 826, 828,				Signetics	2504					
	TI	SN54S188		IM7712	AMD	AM2806		311	RCA	CA311	
								see page 661			
								4250	National	LM4250	

ITT Semiconductors

ITT9000	Fairchild	9000
	TI	SN29000
ITT9001	Fairchild	9001
	TI	SN29001
ITT9002	Fairchild	9002
	TI	SN29002
ITT9003	Fairchild	9003
	TI	SN29003
ITT9004	Fairchild	9004
ITT9005	Fairchild	9005
	TI	SN29005
ITT9006	Fairchild	9006
ITT9007	Fairchild	9007
	TI	SN29007
ITT9008	Fairchild	9008
	TI	SN29008
ITT9009	Fairchild	9009
	TI	SN29009
ITT9014	Fairchild	9014
ITT9015	Fairchild	9015
ITT9016	Fairchild	9016
	TI	SN29016
ITT9017	Fairchild	9017
ITT9022	Fairchild	9022
ITT9024	Fairchild	9024
	TI	SN29024
ITT9033	Fairchild	9033
ITT9093	Motorola	MC853
	Motorola	MC953
	Raytheon	RM993
	SW	SW705
	TI	SN158093
	TI	SN159093
ITT9094	Motorola	MC856
	Motorola	MC956
	Raytheon	RM994
	SW	SW708
	TI	SN158094
	TI	SN159094
ITT9097	Motorola	MC855
	Motorola	MC955

† Discontinued

ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device
ITT Semiconductors (cont)							
ITT9097	Raytheon SW RM997 SW709	ITT946	Motorola MC846 Motorola MC946 Raytheon RM946 SW SW946 TI SN15846 TI SN15946	LS1495	Silicon G SG1495	5231	Intersil IM5610 National DM7598
ITT9099	Motorola MC852 Motorola MC952 Raytheon RM999 SW SW706 TI SN158099 TI SN159099	ITT948	Motorola MC848 Motorola MC948 Raytheon RM948 SW SW948 TI SN15848 TI SN15948	LS1496	Fairchild μ A796 Fairchild 796 Motorola MC1496 National LM1496 Signetics N5596 Silicon G SG1496	5240	National DM7795
ITT930	Motorola MC830 Motorola MC930 Raytheon RM930 SW SW930 TI SN15830 TI SN15930	ITT949	Motorola MC849 Motorola MC949 Raytheon RM949 SW SW949 TI SN15849 TI SN15949	LS1595	Fairchild μ A795 Fairchild 795 Motorola MC1595 Silicon G SG1595	5241	National DM7796
ITT9300	AMD 9300 Fairchild 9300 TI SN29300 TI SN39300	ITT950	Motorola MC850 Motorola MC950 Raytheon RM950 SW SW950 TI SN15850 TI SN15950	LS1596	Fairchild μ A796 Fairchild 796 Motorola MC1596 National LM1596 Signetics S5596 Silicon G SG1596	5300	Fairchild 93416 Harris HPR0M1024A Intel 3601 see page 772, 773 Intersil IM5603 National DM7573 National DM8573 Signetics S82S126 TI SN54S387
ITT9301	AMD 9301 Fairchild 9301 TI SN29301 TI SN39301	ITT951	Motorola MC851 Motorola MC951 Raytheon RM951 SW SW951 TI SN15851 TI SN15951	LS170	National LM170	5301	Fairchild 93406 Harris HPR0M1024 Intersil IM5623 National DM7574 Signetics S82S129 see page 804, 826, 835, TI SN54S287
ITT9304	AMD 9304 Fairchild 9304	ITT9601	AMD 9601 Fairchild 9601 TI SN29601	LS171	National LM171 Teledyne S 911A	5305	Fairchild 93436 Harris HM7620 see page 746 Intersil IM5604 Signetics S82S130 see page 804, 826, 838, TI SN54S287
ITT9309	AMD 9309 Fairchild 9309 TI SN29309 TI SN39309	ITT961	Motorola MC861 Motorola MC961 Raytheon RM961 SW SW961 TI SN15861 TI SN15961	LS270	National LM270	5306	Fairchild 93446 Harris HM7621 see page 746 Intersil IM5624 Signetics S82S130 see page 804, 826, 838, TI SN54S287
ITT931	Motorola MC831 Motorola MC931 TI SN15831 TI SN15931	ITT962	Motorola MC862 Motorola MC962 Raytheon RM962 SW SW962 TI SN15862 TI SN15962	LS271	National LM271 Teledyne S 911B	5330	AMD AM24508 AMD AM27509 Harris HM7602 see page 746 Harris HPR0M8256 Intel 3604 see page 776, 777 Intersil IM5533 Intersil IM5600 National DM7577 Signetics S82S23 see page 804, 826, 828, TI SN54S288 TI SN54S475 TI SN54188A
ITT9312	AMD 9312 Fairchild 9312 TI SN29312 TI SN39312	ITT963	Motorola MC1141 Motorola MC863 Motorola MC963 Raytheon RM963 SW SW963 TI SN5481A TI SN7481A	LS3028	National LM3028 RCA CA3028	5331	Harris HM7603 see page 746 Intersil IM5610 National DM7578 Signetics S82S123 see page 804, 826, 828, TI SN54S288
ITT9316	AMD 9316 Fairchild 9316 Raytheon RM9316 TI SN29316 TI SN39316	Lithic Systems		LS3053	National LM3053 RCA CA3053	5340	Harris HM7643
ITT932	Motorola MC832 Motorola MC932 Raytheon RM932 SW SW932 TI SN15832 TI SN15932	LA3018	Fairchild μ A3018 Fairchild CA3018 National LM3018 RCA CA3018 Silicon G SG3018	LS370	National LM370	5341	Intel 3624 see page 776, 777 TI SN54S474
ITT933	Motorola MC833 Motorola MC933 Raytheon RM933 SW SW933 TI SN15833 TI SN15933	LA3018A	Fairchild μ A3018A Fairchild CA3018A RCA CA3018A	LS371	National LM371 Teledyne S 911C	5350	Fairchild 93411 Raytheon RM5330 Signetics S82S17 SN54S301
ITT935	Motorola MC840 Motorola MC940 Raytheon RM935 TI SN15835 TI SN15935	LA3026	Fairchild μ A3026 Fairchild CA3026 RCA CA3026 Silicon G SG3822	LS555	Exar XR555 Intersil NE555 National LM555 Raytheon RC555 Signetics NE555 Silicon G SG555 Teledyne S 555 TI SN72555	5531	Fairchild 93421 Intersil IM5523 National DM54200 Raytheon RM5340 Signetics S82S16 TI SN54S201
ITT936	Motorola MC936 Raytheon RM936 SW SW936 TI SN15836 TI SN15936	LA3045	Fairchild μ A3045 Fairchild CA3045 Plessey SL3045 RCA CA3045 Silicon G SG3821	LS8038	Intersil 8038	5560	AMD AM27S02 Fairchild 93435 Intersil IM5501 National DM5489 Signetics S3101A see page 804, 806, 814, TI SN54S289
ITT937	Motorola MC837 Motorola MC937 Raytheon RM937 SW SW937 TI SN15837 TI SN15937	LA3086	Fairchild μ A3086 Fairchild CA3086 Plessey SL3086 RCA CA3086 Silicon G SG3886	Mitsubishi International Corp.		5561	AMD AM27S03 National DM7599 National DM76L99 TI SN54S189
ITT944	Motorola MC844 Motorola MC944 Raytheon RM944 SW SW944 TI SN15844 TI SN15944	LS1495	Fairchild μ A795 Fairchild 795 Motorola MC1495	M58531	Mostek MK4007	5660	Intel 3101
ITT945	Motorola MC845 Motorola MC945 Raytheon RM945 SW SW945 TI SN15845 TI SN15945			Monolithic Memories Inc.			
				A5240	National DM7795		
				A5281	AMD AM27581		
				A6240	National DM8795		
				A6280	AMD AM27S80		
				A6281	AMD AM27S81		
				H5200	Intel 33011		
				H6200	Intel 3301		
				L5560	AMD 31L01 National DM54L89A		
				L5561	National DM76L99		
				L6560	AMD 31L01 National DM74L89A		
				L6561	National DM8699		
				1702	National MM5202A		
				5200	Fairchild 93406 Fairchild 93416 Intel 3301 Intersil IM5603 National DM44187 National DM54187 Signetics S82S226 see page 804, 820, 822, TI SN54187		
				5201	Intersil IM5623 National DM7597 Signetics S82S229		
				5205	Intersil IM5604 TI SN54S270		
				5206	TI SN54S370		
				5230	Fairchild 93434 Intersil IM5600 National DM5488 TI SN5488 TI SN5488A		

* Discontinued

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IC UPDATE MASTER

Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device
Monolithic Memories Inc. (cont)		6530	Fairchild Intel 93411 3107 Intersil IM5533 National DM8582 Raytheon RC5330 Signetics N82S17 see page 804, 806, 815, SN74S206 TI	6531	Fairchild 93421 Intel 3106 Intersil IM5523 National DM74200	MCM10144	Fairchild F10410 Raytheon RC10144 Signetics 10144
6200	Fairchild 93406 Intersil IM5603 National DM74187 Signetics N82S226 TI SN74187	6560	AMD AM27S02 AMD MM6560 Fairchild 93435 Intel 3101 Intersil IM5501 National DM7489 Signetics N3101A see page 804, 806, 814, SN74S289 TI	MCM10145	Hitachi MD10145 Signetics 10145 TI SN10145	MCM10147	Fairchild F10405
6201	Intersil IM5623 National DM8597 Signetics N82S229	6561	AMD AM27S03 AMD MM6561 National DM8599	MCM10148	Signetics 10148 TI SN10147 TI SN10148	MCM1110	National MM5231 Nitron NCM1110 Signetics 2430 TI TMS2600
6205	Intersil IM5604 TI SN74S270	MCM1111	Nitron NCM1111	MCM1112	National MM4230 National MM5230 Nitron NCM1112	MCM1120	Nitron NCM1120
6206	TI SN74S370	MCM1121	Nitron NCM1121	MCM1122	Nitron NCM1122	MCM1130	Nitron NCM1130
6230	Fairchild 93434 Intersil IM5600 ITT ITT7488 Motorola MCM4002 National DM7488 Signetics 8223 TI SN7488A	MCM1131	AMI S8614 Nitron NCM1131	MCM1132	AMI S8614 TI TMS4103	MCM1140	Nitron NCM1140 TI TMS4300
6231	National DM8598	MCM1133	AMI S2103	MCM1173	AMI S2103	MCM4002	Fairchild 93434 Intersil IM5600 MMI 6230 National DM5488 National DM7488 TI SN7488
6240	National DM8795	MCM1134	Fairchild 93406 Fairchild 93407 Intersil IM5603 ITT ITT7481 MMI 6200 TI SN7481A	MCM4004	Fairchild 93406 Fairchild 93407 Intersil IM5603 ITT ITT7481 MMI 6200 TI SN7481A	MCM4005	Fairchild 93407 ITT ITT7481 TI SN7481A
6241	National DM8796	MCM1135	Fairchild 93407 Intersil IM5603 ITT ITT7481 MMI 6200 TI SN7481A	MCM4006	TI SN74S387	MCM4006	Fairchild 93407 ITT ITT7481 TI SN7481A
6246	Signetics N8204	MCM1136	Fairchild 93406 Fairchild 93407 Intersil IM5603 ITT ITT7481 MMI 6200 TI SN7481A	MCM4007	Intersil IM7501 Intersil IM7511	MCM4006	Fairchild 93406 Fairchild 93407 Intersil IM5603 ITT ITT7481 MMI 6200 TI SN7481A
6247	Signetics N8205	MCM1137	Fairchild 93406 Fairchild 93407 Intersil IM5603 ITT ITT7481 MMI 6200 TI SN7481A	MCM4008	AMI S4008 see page 706	MCM4006	Fairchild 93406 Fairchild 93407 Intersil IM5603 ITT ITT7481 MMI 6200 TI SN7481A
6300	Fairchild 93416 Harris HPRM1024A Intel 3601 see page 772, 773 Intersil IM5603 National DM8573 Signetics N82S126 see page 804, 826, 835, SN74S387 TI	MCM1138	Fairchild 93406 Fairchild 93407 Intersil IM5603 ITT ITT7481 MMI 6200 TI SN7481A	MCM4008	AMI S4008 see page 706	MCM4005	Fairchild 93407 ITT ITT7481 TI SN7481A
63006	Harris HM7621 see page 746	MCM1139	Fairchild 93406 Fairchild 93407 Intersil IM5603 ITT ITT7481 MMI 6200 TI SN7481A	MCM4009	see page 778, 781 AMI S4096 see page 728 EA EA4096 EMM/Semi RO3-4096 Fairchild 4096 GI RO3-4096 Rockwell 1604	MCM4005	Fairchild 93407 ITT ITT7481 TI SN7481A
6301	Fairchild 93426 Harris HPRM1024 Intersil IM5623 National DM8574 Signetics N82S129 TI SN74S387	MCM1140	Intersil IM7501 Intersil IM7511	MCM4009	see page 778, 781 AMI S4096 see page 728 EA EA4096 EMM/Semi RO3-4096 Fairchild 4096 GI RO3-4096 Rockwell 1604	MCM4005	Fairchild 93407 ITT ITT7481 TI SN7481A
6305	Fairchild 93436 Harris HM7621 see page 746 Intel 3602 see page 774, 775 Intersil IM5604 Signetics N82S130 see page 804, 826, 838, SN74S387	MCM1141	Intersil IM7501 Intersil IM7511	MCM4009	see page 778, 781 AMI S4096 see page 728 EA EA4096 EMM/Semi RO3-4096 Fairchild 4096 GI RO3-4096 Rockwell 1604	MCM4005	Fairchild 93407 ITT ITT7481 TI SN7481A
6306	Fairchild 93446 Intel 3622 see page 774, 775	MCM1142	Intersil IM7501 Intersil IM7511	MCM4009	see page 778, 781 AMI S4096 see page 728 EA EA4096 EMM/Semi RO3-4096 Fairchild 4096 GI RO3-4096 Rockwell 1604	MCM4005	Fairchild 93407 ITT ITT7481 TI SN7481A
6330	AMD AM27S08 Harris HPRM8256 Intersil IM5600 National DM8577 Signetics N82S23 see page 804, 826, 828, SN74188A TI	MCM1143	Intersil IM7501 Intersil IM7511	MCM4009	see page 778, 781 AMI S4096 see page 728 EA EA4096 EMM/Semi RO3-4096 Fairchild 4096 GI RO3-4096 Rockwell 1604	MCM4005	Fairchild 93407 ITT ITT7481 TI SN7481A
6331	AMD AM27S09 Harris HM7603 see page 746 Intersil IM5610 National DM8578 Signetics N82S123 see page 804, 826, 828, SN74S288 TI	MCM1144	Intersil IM7501 Intersil IM7511	MCM4009	see page 778, 781 AMI S4096 see page 728 EA EA4096 EMM/Semi RO3-4096 Fairchild 4096 GI RO3-4096 Rockwell 1604	MCM4005	Fairchild 93407 ITT ITT7481 TI SN7481A
6335	Fairchild 93436 Intel 3602 see page 774, 775	MCM1145	Intersil IM7501 Intersil IM7511	MCM4009	see page 778, 781 AMI S4096 see page 728 EA EA4096 EMM/Semi RO3-4096 Fairchild 4096 GI RO3-4096 Rockwell 1604	MCM4005	Fairchild 93407 ITT ITT7481 TI SN7481A
6340	Harris HM7644 Intel 3604 see page 776, 777 Intersil IM5605 TI SN74S475	MCM1146	Intersil IM7501 Intersil IM7511	MCM4009	see page 778, 781 AMI S4096 see page 728 EA EA4096 EMM/Semi RO3-4096 Fairchild 4096 GI RO3-4096 Rockwell 1604	MCM4005	Fairchild 93407 ITT ITT7481 TI SN7481A
6341	Intel 3624 see page 776, 777 Intersil IM5625 TI SN74S474	MCM1147	Intersil IM7501 Intersil IM7511	MCM4009	see page 778, 781 AMI S4096 see page 728 EA EA4096 EMM/Semi RO3-4096 Fairchild 4096 GI RO3-4096 Rockwell 1604	MCM4005	Fairchild 93407 ITT ITT7481 TI SN7481A
6500	Intersil IM5501	MCM1148	Intersil IM7501 Intersil IM7511	MCM4009	see page 778, 781 AMI S4096 see page 728 EA EA4096 EMM/Semi RO3-4096 Fairchild 4096 GI RO3-4096 Rockwell 1604	MCM4005	Fairchild 93407 ITT ITT7481 TI SN7481A
6501	Intersil IM5501	MCM1149	Intersil IM7501 Intersil IM7511	MCM4009	see page 778, 781 AMI S4096 see page 728 EA EA4096 EMM/Semi RO3-4096 Fairchild 4096 GI RO3-4096 Rockwell 1604	MCM4005	Fairchild 93407 ITT ITT7481 TI SN7481A
6523	Intersil IM5523	MCM1150	Intersil IM7501 Intersil IM7511	MCM4009	see page 778, 781 AMI S4096 see page 728 EA EA4096 EMM/Semi RO3-4096 Fairchild 4096 GI RO3-4096 Rockwell 1604	MCM4005	Fairchild 93407 ITT ITT7481 TI SN7481A
		Mostek Corp.					
		F8	see page 964 Fairchild F8 see page 923				
		MK1002	AMD 1002				
		MK1007	Intersil IM7780 TI TMS3409				
		MK2300	TI TMS2300				
		MK2302	GI RO5-2240S				
		MK2400	AMI S8773				
		MK2500	AMI S5232 see page 706				
		MK4006	AMI S4006 see page 706 Motorola MCM4006 TI SN74S387				
		MK4007	Intersil IM7501 Intersil IM7511				
		MK4008	AMI S4008 see page 706				
		MK4096	see page 778, 781 AMI S4096 see page 728 EA EA4096 EMM/Semi RO3-4096 Fairchild 4096 GI RO3-4096 Rockwell 1604				
		MK4102	Intersil IM7552 Signetics 2602 see page 790 TI TMS4033 TI TMS4035				
		3850	see page 965 Fairchild 3850 see page 924				
		3851	see page 965 Fairchild 3851 see page 924				
		3852	see page 966 Fairchild 3852 see page 925				
		3853	see page 966 Fairchild 3853 see page 925				
		3854	see page 966 Fairchild 3854 see page 925				
		Motorola Semiconductor					
		MCM10140	Signetics 10140 TI SN10140				
		MCM10142	TI SN10142				
		MCM10106	Fairchild F10106 Signetics 10106				
		MCM10107	Fairchild F10107 Signetics 10107				
		MCM10109	Fairchild F10109 Signetics 10109				
		MCM1011	Signetics N1011				
		MCM10110	Fairchild F10110 Signetics 10110				
		MCM10111	Fairchild F10111 Signetics 10111				
		MCM10113	Fairchild F10113 Signetics 10113				
		MCM10114	Fairchild F10114 Signetics 10114				
		MCM10115	Signetics 10115				
		MCM10116	Fairchild F10116 Signetics 10116				
		MCM10117	Fairchild F10117 Signetics 10117				
		MCM10118	Fairchild F10118 Signetics 10118				
		MCM10119	Fairchild F10119 Signetics 10119				
		MCM1012	Signetics N1012				
		MCM10121	Fairchild F10121 Signetics 10121				
		MCM10123	Motorola F10123 Signetics 10123				
		MCM10124	Fairchild F10124 Signetics 10124				
		MCM10125	Fairchild F10125 Signetics 10125				
		MCM10128	Signetics F10128				
		MCM10129	Signetics 10129				
		MCM1013	Signetics N1013				
		MCM10130	Fairchild F10130 Signetics 10130				
		MCM10131	Fairchild F10131 Signetics 10131				
		MCM10132	Fairchild F10132 Signetics 10132				
		MCM10133	Fairchild F10133 Signetics 10133				
		MCM10134	Fairchild F10134 Signetics 10134				
		MCM10135	Fairchild F10135 Signetics 10135				
		MCM10136	Fairchild F10136 Signetics 10136				
		MCM10137	Fairchild F10137 Signetics 10137				
		MCM10138	Signetics 10138				
		MCM10139	Intersil IM5600				
		MCM1014	Signetics N1014				
		MCM10141	Fairchild F10141 Signetics 10141				
		MCM10153	Fairchild F10153 Signetics 10153				
		MCM10158	Fairchild F10158 Signetics 10158				
		MCM10160	Signetics 10160				
		MCM10161	Fairchild F10161 Signetics 10161				
		MCM10162	Fairchild F10162 Signetics 10162				
		MCM10164	Signetics 10164				
		MCM10166	Fairchild F10166 Signetics 10166				
		MCM10168	Fairchild F10168 Signetics 10168				
		MCM10170	Fairchild F10170 Signetics 10170				
		MCM10171	Fairchild F10171 Signetics 10171				
		MCM10172	Fairchild F10172 Signetics 10172				
		MCM10173	Fairchild F10173 Signetics 10173				
		MCM10174	Signetics 10174				
		MCM10175	Fairchild F10175 Signetics 10175				
		MCM10176	Fairchild F10176 Signetics 10176				
		MCM10178	Fairchild F10178 Signetics 10178				

† Discontinued

ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device
Motorola Semiconductor (cont)							
MC10178	Signetics 10178	MC14001	SSS SCL4001 SW SN4001 TI TF4001 Toshiba TC4001	MC14013	TI TP4013 Toshiba TC4013	MC14024	RCA CD4024 see page 375 SGS HBF4024 SSS SCL4024
MC10179	Fairchild F10179 Signetics 10179			MC14014	National CD4015 RCA CD4014 see page 375 SSS SCL4014	MC14025	Fairchild F4025 Harris HD4025 National CD4025 RCA CD4025 see page 375 SGS HBF4025 SSS SCL4025 SW SW4025 TI TF4025 TI TP4025 Toshiba TC4025
MC10180	Fairchild F10180 Signetics 10180	MC14002	Fairchild F4002 Harris HD4002 National CD4002 RCA CD4002 see page 375 SGS HBF4002 SSS SCL4002 TI TF4002 TI TP4002 Toshiba TC4002	MC14015	Fairchild F4015 Harris HD4015 see page 266 RCA CD4015 see page 375 SGS HBF4015 SSS SCL4015 SW SW4015 TI TF4015 TI TP4015 Toshiba TC4015		
MC10181	Fairchild F10181 Signetics 10181			MC14016	National CD4016 RCA CD4016 see page 375 SSS SCL4016	MC14027	Fairchild F4027 Harris HD4027 National CD4027 RCA CD4027 see page 375 SGS HBF4027 SSS SCL4027 SW SW4027 TI TF4027 TI TP4027 Toshiba TC4027
MC10186	Fairchild F10186 Signetics 10186	MC14006	Fairchild F4006 Harris HD4006 National CD4006 RCA CD4006 see page 375 SSS SCL4006	MC14017	Fairchild F4017 Harris HD4017 National CD4017 RCA CD4017 see page 375 SGS HBF4017 SSS SCL4017 SW SW4017 TI TF4017 TI TP4017 Toshiba TC4017	MC14028	Fairchild F4028 Harris HD4028 see page 266 National CD4028 RCA CD4028 see page 375 SGS HBF4028 SSS SCL4028 SW SW4028 TI TF4028 TI TP4028 Toshiba TC4028
MC10190	Signetics 10190	MC14007	Fairchild F4007 GI MEM4007 National CD4007 National CD4008 RCA CD4007 see page 375 SGS HD4007 SSS SCL4007 TI TF4007 TI TP4007 Toshiba TC4007	MC14020	Fairchild F4020 Harris HD4020 see page 266 National CD4020 RCA CD4020 see page 375 SGS HBF4020 SSS SCL4020 SW SW4020 TI TF4020 TI TP4020 Toshiba TC4020	MC14032	RCA CD4032 see page 375 Toshiba TC4032
MC10191	Signetics 10191			MC14033	SGS HBF4033 SSS SCL4033 TI TF4033 TI TP4033 Toshiba TC4033	MC14034	Fairchild F4034 RCA CD4034 see page 375 SSS SCL4034 Toshiba TC4034
MC10195	Signetics 10195	MC14008	Fairchild F4008 Harris HD4008 RCA CD4008 see page 375 SSS SCL4008 TI TF4008 TI TP4008 Toshiba TC4008	MC14021	Fairchild F4021 Harris HD4021 see page 266 National CD4021 RCA CD4021 see page 375 SSS SCL4021 SW SW4021 TI TF4021 TI TP4021 Toshiba TC4021	MC14035	Fairchild F4035 Harris HD4035 see page 266 National CD4035 RCA CD4035 see page 375 SGS HBF4035 SSS SCL4035 TI TF4035 TI TP4035 Toshiba TC4035
MC10216	Signetics 10216	MC14009	National CD4009 RCA CD4009 see page 375 SSS SCL4009	MC14022	Fairchild F4022 Harris HD4022 see page 266 National CD4022 RCA CD4022 see page 375 SGS HBF4022 SSS SCL4022 TI TF4022 TI TP4022 Toshiba TC4022	MC14038	RCA CD4038 see page 375 Toshiba TC4038
MC10231	Signetics 10231	MC14010	National CD4010 RCA CD4010 see page 375 SSS SCL4010			MC14040	Fairchild F4040 Harris HD4040 National CD4040 RCA CD4040 see page 375 SSS SCL4040 TI TF4040 TI TP4040 Toshiba TC4040
MC1068	Signetics N1068	MC14011	Fairchild F4011 GI MEM4011 Harris HD4011 National CD4011 RCA CD4011 see page 375 SGS HBF4011 SSS SCL4011 SW SW4011 TI TF4011 TI TP4011 Toshiba TC4011	MC14023	Fairchild F4023 Harris HD4023 National CD4023 RCA CD4023 see page 375 SGS HBF4023 SSS SCL4023 SW SW4023 TI TF4023 TI TP4023 Toshiba TC4023	MC14042	Fairchild F4042 Harris HD4042 National CD4042 RCA CD4042 see page 375 SGS HBF4042 SSS SCL4042 TI TF4042 TI TP4042 Toshiba TC4042
MC1150	AMI MX53D	MC14012	Fairchild F4012 Harris HD4012 National CD4012 RCA CD4012 see page 375 SGS HBF4012 SSS SCL4012 SW SW4012 TI TF4012 TI TP4012 Toshiba TC4012	MC14024	Fairchild F4024 Harris HD4024 National CD4024 National MM4624	MC14046	Fairchild F4046 RCA CD4046 see page 375
MC1160	TI TMS3003						
MC1161	TI TMS4062	MC14013	AMI UL51L Fairchild F4013 GI MEM4013 Harris HD4013 National CD4013 National MM4613 SGS HBF4013 SSS SCL4013 SW SW4013 TI TF4013				
MC1180	AMI S2470 see page 254						
MC1181	AMI S2567 see page 254 Nitron NC1181						
MC1182	AMI S2566 see page 254 Nitron NC1182						
MC1183	AMI S2555 see page 254 Nitron NC1183						
MC1184	AMI S2556 see page 254 Nitron NC1184						
MC1303	Raytheon RC4739						
MC1304	Fairchild μ A732 Fairchild 732 National LM1304 Sprague ULN-2120						
MC1305	National LM1305 Sprague ULN-2122						
MC1307	Fairchild μ A767 National LM1307 Sprague ULN-2128						
MC1310	Exar XR1310 Signetics MC1310 Sprague ULN-2210						
MC1324	Sprague ULN-2224						
MC1328	RCA CA3072 Sprague ULN-2114 Sprague ULN-2228						
MC1339	Signetics PA239 Sprague ULN-2126						
MC1351	National LM1351						
MC1357	Fairchild 2136 RCA CA2111 Signetics ULN2111 Sprague ULN-2111 Sprague ULN-2113						
MC1358	Fairchild μ A3065 RCA CA3065 Sprague ULN-2165						
MC1364	Fairchild μ A3064 Sprague ULN-2264						
MC1370	Fairchild μ A780 Sprague ULN-2124						
MC1371	Fairchild μ A781 Sprague ULN-2127						
MC1398	RCA CA1398						
MC14000	Harris HD4000 National CD4000 RCA CD4000 see page 375 SSS SCL4000 TI TF4000 TI TP4000						
MC14001	Fairchild F4001 GI MEM4001 Harris HD4001 National CD4001 RCA CD4001 see page 375 SGS HBF4001						

† Discontinued

The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
Motorola Semiconductor (cont)			MC14512	Fairchild Harris TI Toshiba	F4512 HD4512 TF4512 TP4512 TC4512	MC14555	Fairchild RCA see page 375	F4555 CD4555	MC1556	TI	SN52771
MC14049	Fairchild GI Harris National RCA see page 375	F4049 MEM4049 HD4049 CD4049 CD4049	MC14514	Fairchild Harris RCA see page 375	F4514 SIL4514 CD4514	MC14556	Fairchild RCA see page 375	F4556 CD4556	MC1558	Fairchild Harris National PMI Raytheon Raytheon see page 651	μA1558 HA-2650 LM1558 SSS1558 RM1558 RM4558
	SGS SSS SW Teledyne S TI TI Toshiba	HBF4049 SCL4049 SW4049 CD4049 TF4049 TP4049 TC4049		SSS Solitron Toshiba	SCL4514 CM4514 TC4514	MC1456	Harris Raytheon Signetics Silicon G TI	HA-2605 RC1556 MC1456 SG1456 SN72771		CA1558 MC1558 SG1558 Teledyne S TI	1558 SN52558
MC14050	Fairchild Harris National RCA see page 375	F4050 HD4050 CD4050 CD4050	MC14515	Fairchild RCA see page 375	F4515 CD4515	MC14571	SSS	SCL4571	MC1568	Exar Silicon G	XR1568 SG1568
	SGS SSS SW Teledyne S TI TI Toshiba	HBF4050 SCL4050 SW4050 CD4050 TF4050 TP4050 TC4050		SSS Solitron Toshiba	SCL4515 CM4515 TC4515	MC1458	Fairchild Fairchild Harris National PMI Raytheon Raytheon see page 651	μA1458 1458 HA-2655 LM1458 SSS1458 RC1458 RC4558	MC1595	Lithic Sys Silicon G	LS1595 SG1595
MC14068	Fairchild RCA see page 375	F4068 CD4068	MC14516	Fairchild National RCA see page 375	F4516 CD4516 CD4516	MC14581	SSS TI TI	SCL4581 TF4581 TP4581	MC1596	Fairchild Lithic Sys National Signetics Silicon G	μA796 LS1596 LM1596 MC1596 SG1596
	Toshiba	TC4068		SSS Toshiba	SCL4516 TC4516	MC14582	Fairchild TI	F4582 TF4582 TP4582	MC1648	Plessey	SP1648
MC14069	Fairchild National RCA see page 375	F4069 CD4069 CD4069	MC14517	SSS	SCL4517	MC14588	AMD	MC1488	MC1650	Plessey	SP1650
	Toshiba	TC4069	MC14518	Fairchild Harris National RCA see page 375	F4518 HD4518 CD4518 CD4518	MC14588	ITT ITT	IT1488 IT1489	MC1651	Plessey	SP1651
MC14071	Fairchild RCA see page 375	F4071 CD4071		RCA SSS Solitron TI TI Toshiba	CD4518B SCL4518 CM4518 TF4518 TP4518 TC4518	MC14588	National SSS Toshiba	MM74C85 SCL4585 TC4585	MC1658	Fairchild Plessey	11C58 SP1658
	TI TI Toshiba	TF4071 TP4071 TC4071	MC14519	Fairchild Harris TI TI	F4519 HD4519 TF4519 TP4519	MC14588	ITT	IT1488	MC1660	Plessey	SP1660
MC14073	RCA see page 375	CD4073		Fairchild Harris National RCA SSS Solitron TI TI Toshiba	F4520 HD4520 CD4520 CD4520B SCL4520 CM4520 TF4520 TP4520 TC4520	MC14588	National SSS Toshiba	DS1488 RC1488 RM1488 SG1488 SN75188	MC1662	Plessey	SP1662
MC14076	Fairchild National RCA see page 375	F4076 CD4076 CD4076	MC14520	Fairchild Harris National RCA see page 375	F4520 HD4520 CD4520 CD4520B SCL4527 CD4527B	MC14588	ITT	IT1488	MC1664	Plessey	SP1664
	TI TI Toshiba	TF4076 TP4076 TC4076		RCA SSS Solitron TI TI Toshiba	CD4527	MC14588	National Raytheon Raytheon Silicon G TI	DS1488 RC1488 RM1488 SG1488 SN75188	MC1666	Plessey	SP1666
MC1408	AD see page 538	AD559	MC14521	Harris	HD4521	MC14588	AMD	MC1488	MC1668	Plessey	SP1668
	PMI	SSS1408	MC14522	Fairchild TI TI	F4522 TF4522 TP4522	MC14588	Exar Exar National Raytheon Raytheon Signetics Silicon G TI	XR1488 XR1489 DS1489 RC1489 RC1489A MC1489 SG1489 SN75189	MC1670	Plessey	SP1670
MC14081	Fairchild RCA see page 375	F4081 CD4081		Fairchild TI TI Toshiba	F4526 TF4526 TP4526	MC14588	ITT	IT1488	MC1672	Plessey	SP1672
	TI TI Toshiba	TF4081 TP4081 TC4081	MC14526	Fairchild TI TI	F4526 TF4526 TP4526	MC14588	ITT	IT1488	MC1674	Plessey	SP1674
MC1414	National Raytheon TI	LM1414 RC1414 SN72514	MC14527	RCA see page 375	CD4527	MC14588	Lithic Sys Silicon G	LS1495 SG1495	MC1690	Fairchild Plessey	11C06C SP1690
MC1436	Harris National Silicon G	HA-2645 LM1436 SG1436		RCA	CD4527B	MC14588	Fairchild Lithic Sys Signetics Silicon G	μA796 LS1496 MC1496 SG1496	MC1692	Plessey	MC1692
MC1437	Raytheon	RC1437	MC14528	Fairchild RCA Signetics SSS Toshiba	F4528 CD4528B N4528 SCL4528 TC4528	MC14588	AMD	AD559	MC1709	Fairchild National National Raytheon Raytheon Raytheon Signetics Teledyne S TI	μA709 LM1709 LM709 RC709 RM709 μA709 709 SN52709
MC1441	RCA	CA1541	MC14529	Harris	HD4529	MC14588	Exar Exar National Raytheon Raytheon Signetics Silicon G TI	XR1489 XR1489 DS1489 RC1489 RC1489A MC1489 SG1489 SN75189	MC1710	Fairchild National National Raytheon Raytheon Signetics Silicon G Teledyne S TI	μA710 LM1710 LM710 RC710 RM710 μA710 SG1710 710 SN52710
MC14502	RCA RCA SSS Solitron Toshiba	CD4502 CD4502B SCL4502 CM4508 TC4508	MC14531	Fairchild SSS TI TI	F4531 SC4531 TF4531 TP4531	MC14588	ITT	IT1488	MC1711	Fairchild Fairchild National National Raytheon Raytheon Signetics Silicon G Teledyne S TI	μA711 711 LM1711 LM711 RC711 RM711 μA711 SG1711 711 SN52711
MC14507	RCA TI	CD4070A TF4507		Fairchild SSS TI TI	F4531 SC4531 TF4531 TP4531	MC14588	National Raytheon TI	LM1514 RM1514 SN52514	MC1712	Fairchild Raytheon Raytheon TI	μA702 RC702 RM702 SN52702
MC14508	Harris	HD4508	MC14532	Fairchild RCA see page 375	F4532 CD4532	MC14588	Harris National Silicon G	HA-2640 LM1536 SG1536	MC1723	AMD	723
MC14510	Fairchild Harris National RCA SSS	F4510 HD4510 CD4510 CD4510B SCL4510		RCA Toshiba	CD4532B TC4532	MC14588	Raytheon	RM1537		Fairchild Intersil	μA723 723
MC14511	National RCA SSS Solitron	CD4511 CD4511B SCL4511 CM4511	MC14539	Fairchild Toshiba	F4539 TC4539	MC14588	RCA	CA1541		National National Raytheon Raytheon RCA	LM1723 LM723 RC723 RM723 CA723
			MC14543	Harris	HD4543	MC14588	Raytheon Signetics	RM555 SE555		Signetics Silicon G Teledyne S TI	SG1723 723 SN52723
			MC14553	Fairchild	F4553	MC14588	Harris Raytheon Raytheon Signetics Silicon G	HA-2600 RM1556 RM1556A MC1556 SG1556			

† Discontinued

ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device
Motorola Semiconductor (cont)							
MC1733	AMD 733 National LM1733 National LM733 Raytheon RC733 Raytheon RM733 Signetics μ A733 TI SN52733	MC1912	TI SN151912	MC3032	TI SN74H53	MC5003	TI SN74186
MC1741	AMD 741 Fairchild μ A741 Intersil 741 National LM1741 National LM741 PMI S55741 Raytheon RC741 Raytheon RM741 RCA CA741 see page 661 Signetics μ A741 Silicon G SG1741 Silicon G SG741 Teledyne S 741 TI SN52741	MC1914	SW SW1914	MC3033	Fairchild 74H54 Fairchild 9H54 ITT ITT74H54 TI SN74H54	MC5005	MMI 6300 TI SN74S387
MC1747	AMD 747 Raytheon RC747 Raytheon RM747 Signetics μ A747 Teledyne S 747	MC2257	Nitron NC2257	MC3034	Fairchild 74H55 Fairchild 9H55 TI SN74H55	MC5303	TI SN54186
MC1748	AMD 748 Fairchild μ A748 Intersil 748 National LM1748 National LM748 Raytheon RC748 Raytheon RM748 RCA CA748 Signetics μ A748 Silicon G SG1748 Teledyne S 748 TI SN52748	MC2259	Nitron NC2259	MC3054	Fairchild 74H71 Fairchild 9H71 TI SN74H71	MC5400	Raytheon 5400
MC1800	SW SW1800 TI SN151800	MC2260	Nitron NC2260	MC3055	Fairchild 74H72 Fairchild 9H72 TI SN74H72	MC5401	Raytheon 5401
MC1801	TI SN151801	MC3000	Fairchild 74H00 Fairchild 9H00 ITT ITT74H00 TI SN74H00	MC3060	ITT ITT74H74 TI SN74H74	MC5403	Raytheon 5403
MC1802	SW SW1802 TI SN151802	MC3001	Fairchild 74H08 Fairchild 9H08 ITT ITT7408 TI SN7408	MC3061	Fairchild 9S114 TI SN74S114	MC5404	Raytheon 5404
MC1803	TI SN151803	MC3003	ITT ITT7432 TI SN7432	MC3062	Fairchild 9S113 TI SN74S113	MC5405	Raytheon 5405
MC1804	SW SW1804 TI SN151804	MC3005	Fairchild 74H10 Fairchild 9H10 ITT ITT74H10 TI SN74H10	MC3063	Fairchild 74H73 Fairchild 9H73 ITT ITT74H73 TI SN74H73	MC5408	Raytheon 5408
MC1805	TI SN151805	MC3006	Fairchild 74H11 Fairchild 9H11 ITT ITT74H11 TI SN74H11	MC3100	TI SN54H00	MC5409	Raytheon 5409
MC1806	SW SW1806 TI SN151806	MC3008	Fairchild 74H04 Fairchild 9H04 ITT ITT74H04 TI SN74H04	MC3104	TI SN54H01	MC5410	Raytheon 5410
MC1807	TI SN151807	MC3009	Fairchild 74H05 Fairchild 9H05 ITT ITT74H05 TI SN74H05	MC3105	TI SN54H10	MC5411	Raytheon 5411
MC1808	SW SW1808 TI SN151808	MC3010	Fairchild 74H20 Fairchild 9H20 ITT ITT74H20 ITT ITT74H21 TI SN74H20	MC3106	TI SN54H11	MC5412	Raytheon 5412
MC1809	TI SN151809	MC3011	Fairchild 74H21 Fairchild 9H21 TI SN74H21	MC3108	TI SN54H04	MC5413	Raytheon 5413
MC1810	SW SW1810 TI SN151810	MC3012	Fairchild 74H22 Fairchild 9H22 TI SN74H22	MC3109	TI SN54H05	MC5414	Raytheon 5414
MC1811	TI SN151811	MC3015	TI SN74H30	MC3110	TI SN54H20	MC5415	Raytheon 5415
MC1812	SW SW1812 TI SN151812	MC3016	Fairchild 74H30 Fairchild 9H30 ITT ITT74H30	MC3111	TI SN54H21	MC5416	Raytheon 5416
MC1813	SW SW1813	MC3018	Fairchild 74H62 Fairchild 9H62 TI SN74H62	MC3112	TI SN54H22	MC5417	Raytheon 5417
MC1814	SW SW1814	MC3019	Fairchild 74H61 Fairchild 9H61 TI SN74H61	MC3116	TI SN54H30	MC5418	Raytheon 5418
MC1900	SW SW1900 TI SN151900	MC3020	Fairchild 74H50 Fairchild 9H50 ITT ITT74H50 TI SN74H50	MC3118	TI SN54H62	MC5419	Raytheon 5419
MC1901	TI SN151901	MC3021	TI SN74S86	MC3119	TI SN54H61	MC5420	Raytheon 5420
MC1902	SW SW1902 TI SN151902	MC3022	Fairchild 74H51 Fairchild 9H51 ITT ITT74H51 TI SN74H51	MC3120	TI SN54H50	MC5421	Raytheon 5421
MC1903	SW SW1903 TI SN151903	MC3024	Fairchild 74H40 Fairchild 9H40 ITT ITT74H40 TI SN74H40	MC3121	TI SN54S86	MC5422	Raytheon 5422
MC1904	SW SW1904 TI SN151904	MC3025	ITT ITT74H40 TI SN74H40	MC3123	TI SN54H51	MC5423	Raytheon 5423
MC1905	TI SN151905	MC3030	Fairchild 74H60 Fairchild 9H60 ITT ITT74H60 TI SN74H60	MC3124	TI SN54H40	MC5424	Raytheon 5424
MC1906	SW SW1906 TI SN151906	MC3031	Fairchild 74H52 Fairchild 9H52 TI SN74H52	MC3125	TI SN54H40	MC5425	Raytheon 5425
MC1907	TI SN151907	MC3032	Fairchild 74H53 Fairchild 9H53 ITT ITT74H53	MC3130	TI SN54H60	MC5426	Raytheon 5426
MC1908	SW SW1908 TI SN151908			MC3131	TI SN54H52	MC5427	Raytheon 5427
MC1909	TI SN151909			MC3132	TI SN54H53	MC5428	Raytheon 5428
MC1910	SW SW1910 TI SN151910			MC3133	TI SN54H54	MC5429	Raytheon 5429
MC1911	TI SN151911			MC3134	TI SN54H55	MC5430	Raytheon 5430
MC1912	SW SW1912			MC3154	TI SN54H71	MC5431	Raytheon 5431
				MC3155	TI SN54H72	MC5432	Raytheon 5432
				MC3160	TI SN54H74	MC5433	Raytheon 5433
				MC3162	TI SN54S113	MC5434	Raytheon 5434
				MC3163	TI SN54H73	MC5435	Raytheon 5435
				MC3301	Fairchild 3301 Raytheon LM2900 Raytheon RC3301	MC5436	Raytheon 5436
				MC3302	Raytheon RC3302 Teledyne S 3302	MC5437	Raytheon 5437
				MC3401	Fairchild 3401 Raytheon LM3900 Raytheon RC3401 RCA CA3401	MC5438	Raytheon 5438
				MC3403	Exar XR3403 Fairchild μ A3403C Raytheon RC3403 see page 649 Raytheon RC4137	MC5439	Raytheon 5439
				MC3503	Exar XR3503 Fairchild μ A3503M Raytheon RM3503 see page 649 Raytheon RM4137	MC5440	Raytheon 5440
				MC4005	Fairchild 93407 ITT ITT481 TI SN7481	MC5441	Raytheon 5441
				MC4015	Raytheon RL4015	MC5442	Raytheon 5442
				MC4024	Fairchild 11C24C	MC5443	Raytheon 5443
				MC4044	Fairchild 11C44C	MC5444	Raytheon 5444
				MC4064	MMI 6560 Signetics NB2S16 see page 804, 806, 815,	MC5445	Raytheon 5445
				MC4304	TI SN5481A	MC5474	Raytheon 5474
				MC4305	TI SN5481A	MC5481	Raytheon 5481
						MC5483	Raytheon 5483
						MC5486	Raytheon 5486
						MC55107	AMD SN55107B Fairchild 55107 National DS55107 Raytheon RM55107 Raytheon SN55107
						MC55108	AMD SN55108B Fairchild 55108 National DS55108 Raytheon RM55108 TI SN55108
						MC55109	AMD SN55109 Fairchild 55109 National DS55109 Raytheon RM55109 TI SN55109
						MC55110	AMD SN55110 Fairchild 55110 National DS55110 Raytheon RM55110 TI SN55110
						MC5520	National DS5520
						MC5521	National DS5521

† Discontinued

The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

IC UPDATE MASTER

Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
Motorola Semiconductor (cont)			MC74162	Raytheon	74162	MC75107	AMD	SN75107B	MC75452	TI	SN75452
MC5522	National	DS5522	MC74163	Raytheon	74163	Fairchild	75107	MC75453	ITT	ITT75453	
MC5523	National	DS5523	MC74164	Raytheon	74164	National	DS75107	National	National	DS75453	
MC5524	National	DS5524	MC74165	Raytheon	74165	Raytheon	RC75107A	Raytheon	Raytheon	RC75453	
MC5525	National	DS5525	MC74166	Raytheon	74166	MC75108	AMD	SN75108B	Teledyne S	75453	
MC574	Raytheon	5474	MC74170	Raytheon	74170	Fairchild	75108	TI	TI	SN75453	
MC6002	TI	TMS4062	MC74174	Raytheon	74174	National	DS75108	MC75454	ITT	ITT75454	
MC6800	AMI	S6800	MC74181	Raytheon	74181	Raytheon	RC75108A	MC75491	National	DS75490	
	see page 862		MC74182	Raytheon	74182	MC75109	AMD	SN75109	TI	SN75491	
MC6820	AMI	S6820	MC74190	Raytheon	74190	Fairchild	75109	MC75492	National	DS75492	
	see page 889		MC74191	Raytheon	74191	ITT	ITT75109	TI	TI	SN75492	
MC6850	AMI	S6850	MC74192	Raytheon	74192	National	DS75109	MC7805	National	LM340-5	
	see page 895		MC74193	Raytheon	74193	Raytheon	RC75109	Raytheon	Raytheon	RC7805	
MC6860	AMI	S6860	MC74194	Raytheon	74194	MC75110	AMD	SN75110	Silicon G	SG7805	
	see page 900		MC74195	Raytheon	74195	Fairchild	75110	MC7806	National	LM340-6	
MC7241	Raytheon	RC8241	MC74198	Raytheon	74198	ITT	ITT75110	Raytheon	Raytheon	RC7806	
	Signetics	N8241	MC74199	Raytheon	74199	National	DS75110	Silicon G	Silicon G	SG7806	
MC7242	Fairchild	9386	MC7420	Hitachi	HD2504	MC7520	ITT	ITT7520	MC7808	National	LM340-8
	Raytheon	RC8242	MC7421	Raytheon	7421	National	DS7520	Raytheon	Raytheon	RC7808	
	Signetics	N8242	MC7422	Raytheon	7422	Signetics	SN7520	Silicon G	Silicon G	SG7808	
MC7250	Raytheon	RC8250	MC74283	Raytheon	74283	Signetics	7520	MC7812	National	LM340-12	
	Signetics	N8250	MC7430	Hitachi	HD2508	TI	SN7520	Raytheon	Raytheon	RC7812	
MC7251	Raytheon	RC8251	MC7440	Hitachi	HD2501	MC7521	ITT	ITT7521	Silicon G	SG7812	
	Signetics	N8251	MC7441	Hitachi	HD2518	National	DS7521	MC7815	National	LM340-15	
MC7261	Raytheon	RC8261	MC7442	Raytheon	7442	Signetics	SN7521	Raytheon	Raytheon	RC7815	
	Signetics	N8261	MC7443	Raytheon	7443	Signetics	7521	Silicon G	Silicon G	SG7815	
MC74H00	Raytheon	74H00	MC7444	Raytheon	7444	TI	SN7521	MC7818	National	LM340-18	
MC74H01	Raytheon	74H01	MC7445	Raytheon	7445	MC7522	ITT	ITT7522	Raytheon	RC7818	
MC74H04	Raytheon	74H04	MC7446	Hitachi	HD2502	National	DS7522	Silicon G	Silicon G	SG7818	
MC74H05	Raytheon	74H05	MC7447	Hitachi	HD2515	Signetics	SN7522	MC7824	National	LM340-24	
MC74H10	Raytheon	74H10	MC7448	Raytheon	7448	TI	SN7522	Raytheon	Raytheon	RC7824	
MC74H11	Raytheon	74H11	MC7449	Raytheon	7449	MC7523	ITT	ITT7523	Silicon G	SG7824	
MC74H20	Raytheon	74H20	MC7450	Hitachi	HD2506	National	DS7523	MC8241	Raytheon	RM8241	
MC74H22	Raytheon	74H22	MC7451	Hitachi	HD2505	Signetics	SN7523	Signetics	Signetics	S8241	
MC74H40	Raytheon	74H40	MC7453	Hitachi	HD2512	TI	SN7523	MC8242	Fairchild	9386	
MC74H74	Raytheon	74H74	MC7454	Hitachi	HD2514	MC75234	ITT	ITT75234	Raytheon	RM8242	
MC7400	Hitachi	HD2503	MC7455	Hitachi	HD2516	TI	SN75234	Signetics	Signetics	S8242	
	Raytheon	7400	MC7456	Hitachi	HD2517	MC75235	ITT	ITT75235	MC8250	Raytheon	RM8250
	TI	SN7400	MC7457	Hitachi	HD2519	MC7524	ITT	ITT7524	Signetics	Signetics	S8250
MC7401	Hitachi	HD2509	MC7458	Hitachi	HD2520	National	DS7524	MC8251	Raytheon	RM8251	
	Raytheon	7401	MC7459	Hitachi	HD2521	Signetics	SN7524	Signetics	Signetics	S8251	
	TI	SN7401	MC7460	Hitachi	HD2522	TI	SN7524	MC8260	Raytheon	RM8260	
MC7402	Hitachi	HD2511	MC7461	Hitachi	HD2523	Signetics	7524	MC8261	Raytheon	RM8261	
	TI	SN7402	MC7462	Hitachi	HD2524	TI	SN7524	Signetics	Signetics	S8261	
MC7403	Raytheon	7403	MC7463	Hitachi	HD2525	MC7525	ITT	ITT7525	MC830	Hitachi	HD2204
MC7404	Hitachi	HD2522	MC7464	Hitachi	HD2526	National	DS7525	Signetics	Signetics	SW	SN930
	Raytheon	7404	MC7465	Hitachi	HD2527	Signetics	SN7525	Signetics	Signetics	TI	SN15930
	TI	SN7404	MC7466	Hitachi	HD2528	TI	SN7525	MC8300	AMD	9300	
MC7405	Hitachi	HD2523	MC7467	Hitachi	HD2529	MC75252	ITT	ITT75452	Fairchild	9300	
	Raytheon	7405	MC7468	Hitachi	HD2530	MC7528	ITT	ITT7528	Raytheon	RC9300	
	TI	SN7405	MC7469	Hitachi	HD2531	National	DS7528	TI	TI	SN74195	
MC7408	Raytheon	7408	MC7470	Hitachi	HD2532	MC7529	ITT	ITT7529	MC8301	AMD	9301
MC7409	Raytheon	7409	MC7471	Hitachi	HD2533	TI	SN7529	Fairchild	Fairchild	9301	
MC7410	Hitachi	HD2507	MC7472	Hitachi	HD2534	MC7529	ITT	ITT7529	Signetics	N8252	
	Raytheon	7410	MC7473	Hitachi	HD2535	TI	SN7529	TI	TI	SN29301	
	TI	SN7410	MC7474	Hitachi	HD2536	MC75325	Fairchild	75325	MC8304	AMD	9304
MC74107	Hitachi	HD2530	MC7475	Hitachi	HD2537	National	DS75325	Fairchild	Fairchild	9304	
	TI	SN74107	MC7476	Hitachi	HD2538	Raytheon	RC75325	Raytheon	Raytheon	RC9304	
MC7411	Raytheon	7411	MC7477	Hitachi	HD2539	TI	SN75325	MC8308	AMD	9308	
MC7412	Raytheon	7412	MC7478	Hitachi	HD2540	MC7534	National	DS7534	Fairchild	9308	
MC74121	Hitachi	HD2543	MC7479	Hitachi	HD2541	TI	SN7534	Raytheon	Raytheon	RC9308	
	TI	SN74121	MC7480	Hitachi	HD2542	MC7535	National	DS7535	TI	SN29308	
MC74123	Raytheon	74123	MC7481	Raytheon	7481	TI	SN7535	MC8309	AMD	9309	
MC74136	Raytheon	74136	MC7482	Raytheon	7482	MC7538	National	DS7538	Fairchild	9309	
MC74145	Raytheon	74145	MC7483	Raytheon	7483	TI	SN7538	Signetics	Signetics	SN29309	
MC7415	Raytheon	7415	MC7484	Raytheon	7484	MC7538	National	DS7538	MC831	SW	
MC74150	Hitachi	HD2548	MC7485	Raytheon	7485	TI	SN7538	TI	TI	SN931	
	Raytheon	74150	MC7486	Raytheon	7486	MC7539	National	DS7539	Signetics	SN15831	
	TI	SN74150	MC7487	Hitachi	HD2541	TI	SN7539	MC8310	AMD	9310	
MC74151	Hitachi	HD2549	MC7488	Hitachi	HD2542	MC7540	ITT	ITT75450	Fairchild	9310	
	Raytheon	74151	MC7489	Hitachi	HD2543	National	DS75450	Raytheon	Raytheon	RC9310	
	TI	SN74151A	MC7490	Hitachi	HD2544	Raytheon	RC75450	TI	TI	SN74160	
MC74152	Raytheon	74152	MC7491	Hitachi	HD2545	Teledyne S	75450	MC8311	AMD	9311	
MC74153	Raytheon	74153	MC7492	Signetics	N7492	TI	SN75450	Fairchild	Fairchild	9311	
MC74154	Raytheon	74154	MC7493	Hitachi	HD25	MC75451	ITT	ITT75451	Raytheon	RC9311	
MC74155	Raytheon	74155	MC7494	Hitachi	HD251	National	DS75451	TI	TI	SN74154	
MC74156	Raytheon	74156	MC7495	Hitachi	HD252	Raytheon	RC75451	MC8312	AMD	9312	
MC74157	Raytheon	74157	MC7496	Hitachi	HD253	Teledyne S	75451	Fairchild	Fairchild	9312	
MC74158	Raytheon	74158	MC7497	Hitachi	HD254	TI	SN75451	Raytheon	Raytheon	RC9312	
MC74159	Raytheon	74159	MC7498	Hitachi	HD255	MC75452	National	DS75452	Signetics	N8230	
MC74160	Raytheon	74160	MC7499	Hitachi	HD256	TI	SN75452	TI	TI	SN29312	
MC74161	Raytheon	74161	MC7500	Hitachi	HD257	Teledyne S	75452	MC8314	AMD	9314	

Discontinued

Bold face device number indicates additional data is provided in Catalog section

ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	
Motorola Semiconductor (cont)								
MC8316	AMD Fairchild Raytheon TI	9316 9316 RC9316 SN74161	MC9308 Raytheon TI	RM9308 SN39308	MC961 Raytheon SW TI	RM961 SN961 SN15961	MLM211 Harris Intersil National Raytheon RCA	HA-2211 LM211 LM211 LM211 CA211
MC8318	AMD TI	9318 SN29318	MC9310 AMD Raytheon TI	9310 RM9310 SN54160	MC962 Raytheon SW TI	RM962 SN962 SN15962	see page 661 Teledyne S	LM211
MC832	Hitachi SW TI	HD2201 SW932 SN15832	MC9311 AMD Raytheon TI	9311 RM9311 SN54154	MC963 Raytheon SW TI	RM963 SN963 SN15963	MLM301 AMD Fairchild Intersil National Raytheon RCA	LM301 μ A301 LM301 LM301 LM301 CA301
MC8328	AMD Fairchild Signetics	9328 9328 N82778	MC9312 AMD Raytheon Signetics TI	9312 RM9312 S8230 SN39312	MLM101 AMD Fairchild Intersil National Raytheon RCA	LM101 μ A101 LM101 LM101 LM101 CA101	see page 661 Signetics Teledyne S TI	LM301 LM301 LM301 LM301 SN72301
MC833	Hitachi SW TI	HD2202 SW933 SN15833	MC9314 AMD	9314	MC9316 AMD Raytheon TI	9316 RM9316 SN54161	see page 661 Signetics Teledyne S	LM301 LM301 LM304
MC834	TI	SN15834	MC9318 AMD TI	9318 SN39318	MLM104 National Raytheon Teledyne S	LM104 LM104 LM104	MLM304 National Raytheon Teledyne S	LM304 LM304 LM304
MC835	SW TI	SW936 SN15838	MC932 Raytheon SW TI	RM932 SW932 SN15939	MLM105 AMD Fairchild Intersil National Raytheon Teledyne S	LM105 μ A105 LM105 LM105 LM105	MLM305 AMD Fairchild Intersil National Raytheon Teledyne S	LM305 μ A305 LM305 LM305 LM305
MC836	Hitachi SW TI	HD2206 SW936 SN15836	MC9328 AMD Signetics	9328 N8277	MLM107 AMD Fairchild Intersil National Raytheon Teledyne S	LM107 μ A107 LM107 LM107 LM107	MLM307 AMD Fairchild Intersil National Raytheon RCA	LM307 μ A307 LM307 LM307 CA307
MC837	SW TI	SW937 SN15837	MC933 SW TI	SW933 SN15933	MLM109 Fairchild Fairchild National Raytheon	LM109 LM109 LM109 LM109	see page 661 Signetics Teledyne S	LM307 LM307 LM307
MC840	SW TI	SW935 SN15835	MC934 TI	SN15934	MLM110 AMD Intersil National	LM110 LM110 LM110	MLM310 AMD Intersil National	LM310 LM310 LM310
MC841	TI	SN15835	MC935 Raytheon SW TI	RM935 SW736 SN15938	MLM111 AMD Harris National Raytheon RCA	LM111 HA-2111 LM111 LM111 CA111	see page 661 Signetics Teledyne S	LM307 LM307 LM307 CA307
MC844	Hitachi SW	HD2209 SW844	MC936 Raytheon SW TI	RM936 SW936 SN15936	see page 661 Teledyne S	LM107	MLM308 RCA	LM307 μ A307 LM307 LM307
MC845	Hitachi SW TI	HD2205 SW945 SN15845	MC937 Raytheon SW TI	RM937 SW937 SN15937	MLM108 RCA	CA108	MLM309 AMD Fairchild National Raytheon	LM309 LM309 LM309 LM309
MC846	Hitachi SW TI	HD2203 SW946 SN15846	MC940 Raytheon SW TI	RM940 SW935 SN15935	MLM109 Fairchild Fairchild National Raytheon	μ A109 LM109 LM109 LM109	MLM310 AMD Intersil National	LM310 LM310 LM310
MC848	SW TI	SW948 SN15848	MC943 Fairchild	SH2001	MLM110 AMD Intersil National	LM110 LM110 LM110	MLM311 AMD Harris Intersil National Raytheon RCA	LM311 LM311 LM311 LM311 CA311
MC849	SW TI	SW949 SN15849	MC944 Raytheon SW TI	RM944 SW944 SN15944	MLM111 AMD Harris National Raytheon RCA	LM111 HA-2111 LM111 LM111 CA111	see page 661 Teledyne S	LM311
MC850	SW TI	SW850 SN15850	MC945 Raytheon SW TI	RM945 SW945 SN15945	see page 661 Teledyne S	LM111	MV14511 Fairchild MMI Signetics	F4511 10149 10149
MC851	SW TI	SW951 SN15851	MC946 Raytheon SW TI	RM946 SW946 SN15946	MLM201 Fairchild Intersil National Raytheon RCA	μ A201 LM201 LM201 LM201 CA201		
MC852	SW TI	SW706 SN158099	MC948 Raytheon SW TI	RM948 SW948 SN15948	MLM204 National Raytheon Teledyne S	LM204 LM204 LM204		
MC853	SW TI	SW705 SN158093	MC949 Raytheon SW TI	RM949 SW949 SN15949	MLM205 AMD Intersil National Raytheon Teledyne S	LM205 LM205 LM205 LM205		
MC855	SW TI	SW709 SN158097	MC950 Raytheon SW TI	RM950 SW950 SN15950	MLM207 AMD Fairchild Intersil National Raytheon Teledyne S	LM207 μ A207 LM207 LM207 LM207		
MC856	SW TI	SW708 SN158094	MC951 Raytheon SW TI	RM951 SW951 SN15951	MLM208 RCA	CA208		
MC857	Hitachi SW TI	HD2213 SW957 SN15857	MC952 Raytheon SW TI	RM952 SW952 SN159099	MLM209 AMD Fairchild National Raytheon	LM209 μ A209 LM209 LM209		
MC858	Hitachi SW TI	HD2214 SW958 SN15858	MC953 SW TI	SW953 SN159093	MLM210 AMD Intersil National	LM210 LM210 LM210		
MC8601	AMD Fairchild Raytheon Signetics TI	9601 9601 RF8601 N8722 SN29601	MC955 TI	SN159097	MLM211 AMD	LM211		
MC8602	AMD Raytheon	9602 RF8602	MC956 TI	SN159094				
MC861	SW TI	SW961 SN15861	MC957 Raytheon SW TI	RM957 SW957 SN15957				
MC862	Hitachi SW TI	HD2207 SW962 SN15862	MC958 Raytheon SW TI	RM958 SW958 SN15958				
MC863	SW TI	SW963 SN15863	MC9601 AMD Raytheon Signetics TI	9601 RF9601 S8722 SN29601				
MC930	Raytheon SW TI	RM930 SW930 SN15930	MC9602 AMD Raytheon	9602 RF9602				
MC9300	AMD Raytheon TI	9300 RM9300 SN54195						
MC9301	AMD TI	9301 SN39301						
MC9304	AMD Raytheon	9304 RM9304						
MC9308	AMD	9308						

Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device
National Semiconductor			
AH0126	Siliconix	DG126	see page 551
AH0129	Siliconix	DG129	see page 551
AH0133	Siliconix	DG133	see page 551
AH0134	Siliconix	DG134	see page 551
AH0139	Siliconix	DG139	see page 551
AH0140	Siliconix	DG140	see page 551
AH0141	Siliconix	DG141	see page 551
AH0142	Siliconix	DG142	see page 551
AH0143	Siliconix	DG143	see page 551
AH0144	Siliconix	DG144	see page 551
AH0145	Siliconix	DG145	see page 551
AH0146	Siliconix	DG146	see page 551

† Discontinued

The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device
National Semiconductor (cont)		CD4030	RCA CD4030 see page 375	DM5410	Signetics TI S5410 SN5410	DM5437	Signetics TI S5437 SN5437
AH0151	Siliconix DG151 see page 551	CD4035	Harris HD4035 see page 266 RCA CD4035 see page 375	DM54107	Signetics TI S54107 SN54107	DM5438	Signetics TI S5438 SN5438
AH0152	Siliconix DG152 see page 551	CD4049	Harris HD4049 RCA CD4049 see page 375	DM5411	Raytheon Signetics 5411 S5411	DM5440	Signetics TI S5440 SN5440
AH0153	Siliconix DG153 see page 551	CD4050	Harris HD4050 RCA CD4050 see page 375	DM5412	Raytheon 5412	DM5442	Raytheon 5442
AH0154	Siliconix DG154 see page 551	CD4066	Harris HD4066 RCA CD4066 see page 375	DM54123	Raytheon 54123	DM5443	Raytheon 5443
AH0161	Siliconix DG161 see page 551	DM10101	Motorola MC10101	DM5413	Signetics TI S5413 SN5413	DM5444	Raytheon 5444
AH0162	Siliconix DG162 see page 551	DM10102	Motorola MC10102	DM54136	Raytheon 54136	DM5445	Raytheon Signetics 5445 S5445
AH0163	Siliconix DG163 see page 551	DM10105	Motorola MC10105	DM54145	Raytheon 54145	DM5450	Signetics TI S5450 SN5450
AH0164	Siliconix DG164 see page 551	DM10106	Motorola MC10106	DM54150	Raytheon 54150	DM5451	Signetics TI S5451 SN5451
CD4001	Harris HD4001 RCA CD4001 see page 375	DM10107	Motorola MC10107	DM54151	Raytheon 54151	DM5453	Signetics TI S5453 SN5453
CD4002	Harris HD4002 RCA CD4002 see page 375	DM10109	Motorola MC10109	DM54152	AMD SN54153 Raytheon 54153 SN54153	DM5454	Signetics TI S5454 SN5454
CD4007	Harris HD4007 RCA CD4007 see page 375	DM10110	Motorola MC10110	DM54154	AMD SN54154 Raytheon 54154 SN54154	DM5460	Signetics TI S5460 SN5460
CD4009	RCA CD4009 see page 375	DM10111	Motorola MC10111	DM54155	Raytheon 54155	DM5472	Signetics TI S5472 SN5472
CD4010	RCA CD4010 see page 375	DM10115	Motorola MC10115	DM54156	Raytheon 54156	DM5473	Signetics TI S5473 SN5473
CD4011	RCA CD4011 see page 375	DM10116	Motorola MC10116	DM54157	AMD SN54157 Raytheon 54157 SN54157	DM5474	Raytheon Signetics 5474 S5474
CD4012	Harris HD4012 RCA CD4012 see page 375	DM10117	Motorola MC10117	DM54158	Raytheon 54158	DM5475	Signetics TI S5475 SN5475
CD4013	Harris HD4013 RCA CD4013 see page 375	DM10118	Motorola MC10118	DM54159	Raytheon 54159	DM5476	Signetics TI S5476 SN5476
CD4014	Harris HD4014 see page 266 RCA CD4014 see page 375	DM10119	Motorola MC10119	DM54160	Raytheon 54160	DM5481	Raytheon 5481
CD4015	Harris HD4015 see page 266 RCA CD4015 see page 375	DM10121	Motorola MC10121	DM54161	Raytheon 54161	DM5483	Raytheon 5483
CD4016	RCA CD4016 see page 375	DM10124	Motorola MC10124	DM54162	Raytheon 54162	DM5486	Raytheon Signetics 5486 S5486
CD4017	Harris HD4017 RCA CD4017 see page 375	DM10130	Motorola MC10130	DM54163	Raytheon 54163	DM5488	Fairchild Intersil MMI 93434 5230 SN5488A
CD4018	Harris HD4018 see page 266 RCA CD4018 see page 375	DM1800	Motorola MC1800 SW SW1800	DM54164	AMD SN54164 Raytheon 54164 SN54164	DM5489	AMD SN5489 AMD 31013 Intersil IM5501 MMI 5560 Raytheon 5489
CD4019	Harris HD4019 see page 266 RCA CD4019 see page 375	DM1801	Motorola MC1801	DM54165	Raytheon 54165	DM5490	Signetics TI S5490 SN5490A
CD4020	Harris HD4020 see page 266 RCA CD4020 see page 375	DM54H00	Fairchild 54H00 Raytheon 9H00 54H00	DM54166	Raytheon 54166	DM5491	Signetics TI S5491 SN5491A
CD4021	Harris HD4021 see page 266 RCA CD4021 see page 375	DM54H01	Raytheon 54H01	DM54167	Signetics TI S5417 SN5417	DM5492	Signetics TI S5492 SN5492A
CD4022	Harris HD4022 see page 266 RCA CD4022 see page 375	DM54H04	Raytheon 54H04	DM54170	Raytheon 54170	DM5493	Signetics TI S5493 SN5493A
CD4023	Harris HD4023 RCA CD4023 see page 375	DM54H20	Raytheon 54H20	DM54174	Raytheon 54174	DM7093	TI S54125
CD4025	Harris HD4025 RCA CD4025 see page 375	DM54H22	Raytheon 54H22	DM54175	Raytheon 54175	DM7094	TI S54126
CD4027	Harris HD4027 RCA CD4027 see page 375	DM54H40	Raytheon 54H40	DM54181	AMD SN54181 Raytheon 54181 SN54181	DM7095	TI S54365
CD4030	Harris HD4030 see page 266	DM54H74	Raytheon 54H74	DM54182	Raytheon 54182	DM7096	TI S54366
		DM54L187	Intersil IM5603	DM54187	Fairchild Intersil MMI 93406 IM5603	DM7097	TI S54367
		DM54L89	MMI L5560	DM54188	MMI 5200 TI SN54187	DM7098	TI S54368
		DM54S287	MMI 5401 TI SN54S287	DM54190	Raytheon 54190	DM71L22	TI S541157
		DM54S387	Intel 3601 see page 772, 773 MMI 5300 TI SN54S387	DM54191	Raytheon 54191	DM71S60	Fairchild 93S43
		DM5400	Fairchild 5400 Fairchild 9N00 Raytheon 5400 Signetics S5400	DM54192	AMD SN54192 Raytheon 54192 TI SN54192	DM7121	TI S54251
		DM5401	Raytheon 5401 Signetics S5401 TI SN5401	DM54193	AMD SN54193 Raytheon 54193 TI SN54193	DM74H00	Fairchild 74H00 Fairchild 9H00 Raytheon 74H00 Signetics N74H00 TI SN74H00
		DM5402	Signetics S5402 TI SN5402	DM54194	Raytheon 54194	DM74H01	Raytheon Signetics 74H01 N74H01
		DM5403	Raytheon Signetics 5403 S5403 TI SN5403	DM54195	AMD SN54195 Raytheon 54195 TI SN54195	DM74H04	Raytheon Signetics 74H04 N74H04 TI SN74H04
		DM5404	Raytheon Signetics 5404 S5404 TI SN5404	DM54198	Raytheon 54198	DM74H05	Raytheon Signetics 74H05 N74H05 TI SN74H05
		DM5405	Raytheon Signetics 5405 S5405 TI SN5405	DM54199	Raytheon 54199	DM74H08	Signetics N74H08
		DM5406	Signetics S5406 TI SN5406	DM5420	Raytheon Signetics 5420 S5420 TI SN5420	DM74H10	Raytheon Signetics 74H10 N74H10 TI SN74H10
		DM5408	Raytheon Signetics 5408 S5408 TI SN5408	DM54200	Intersil IM5523 MMI 5531 Raytheon RM5340 TI SN54S201	DM74H11	Raytheon 74H11
		DM5409	Raytheon Signetics 5409 S5409 TI SN5409	DM5421	Raytheon 5421		
		DM5410	Raytheon 5410	DM5422	Raytheon 5422		
				DM54283	Raytheon 54283		
				DM5430	Signetics S5420 TI SN5430		
				DM5432	Signetics S5432 TI SN5432		

Ⓜ Discontinued

ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
National Semiconductor (cont)			DM7411	Raytheon Signetics	7411 N7411	DM74170	TI	SN74170	DM7445	Raytheon Signetics	7445 N7445
DM74H11	Signetics TI	N74H11 SN74H11	DM7412	Raytheon	7412	DM74172	Signetics Signetics TI	N74S172 N74172 SN74172	DM7446	Hitachi	HD2553 SN7446A
DM74H20	Raytheon Signetics TI	74H20 N74H20 SN74H20	DM74121	Signetics TI	N74121 SN74121	DM74174	AMD Raytheon Signetics TI	SN74174 74174 N74174 SN74174	DM7447	Hitachi	HD2532 N7447 SN7447A
DM74H21	Signetics TI	N74H21 SN74H21	DM74123	AMD Raytheon Signetics TI	SN74123 74123 N74123 SN74123	DM74175	AMD Raytheon Signetics TI	SN74175 74175 N74175 SN74175	DM7448	Signetics TI	N7448 SN7448
DM74H22	Raytheon Signetics TI	74H22 N74H22 SN74H22	DM74125	Signetics TI	N74125 SN74425	DM74180	Signetics TI	N74180 SN74180	DM7450	Hitachi Signetics TI	HD2506 N7450 SN7450
DM74H30	Signetics TI	N74H30 SN74H30	DM74126	Signetics TI	N74126 SN74426	DM74181	AMD Raytheon Signetics TI	N74181 74181 N74181 SN74181	DM7451	Hitachi Signetics TI	HD2505 N7451 SN7451
DM74H40	Raytheon Signetics TI	74H40 N74H40 SN74H40	DM7413	Signetics TI	N7413 SN7413	DM74182	AMD Raytheon Signetics TI	SN74182 74182 N74182 SN74182	DM7453	Hitachi Signetics TI	HD2512 N7453 SN7453
DM74H50	Signetics TI	N74H50 SN74H50	DM74136	Raytheon	74136	DM74187	Fairchild Intersil MMI Signetics TI	93406 IM5603 6200 N82S226 SN74187	DM7454	Hitachi Signetics TI	HD2514 N7454 SN7452
DM74H51	Signetics TI	N74H51 SN74H51	DM74141	Signetics TI	N74141 SN74141	DM74190	Raytheon Signetics TI	74190 N74190 SN74190	DM7460	Signetics TI	N7460 SN7460
DM74H53	Signetics TI	N74H53 SN74H53	DM74145	Raytheon Signetics TI	74145 N74145 SN74145	DM74191	Raytheon Signetics TI	74191 N74191 SN74191	DM7472	Hitachi Signetics TI	HD2529 N7472 SN7472
DM74H54	Signetics TI	N74H54 SN74H54	DM7415	Raytheon	7415	DM74192	AMD Raytheon Signetics TI	SN74192 74192 N74192 SN74192	DM7473	Hitachi Signetics TI	HD2515 N7473 SN7473
DM74H55	Signetics TI	N74H55 SN74H55	DM74150	Raytheon Signetics TI	74150 N74150 SN74150	DM74193	AMD Raytheon Signetics TI	SN74193 74193 N74193 SN74193	DM7474	Hitachi Raytheon Signetics TI	HD2510 7474 N7474 SN7474
DM74H60	Signetics TI	N74H60 SN74H60	DM74151	Raytheon Signetics TI	74151 N74151 SN74151A	DM74194	Raytheon	74194	DM7475	Hitachi Signetics TI	HD2517 N7475 SN7475
DM74H62	Signetics TI	N74H62 SN74H62	DM74152	Raytheon	74152	DM74195	AMD Raytheon Signetics TI	SN74195 74195 N74195 SN74195	DM7476	Hitachi Signetics	HD2516 N7476
DM74H74	Raytheon	74H74	DM74153	AMD Hitachi Raytheon Signetics TI	SN74153 HD2564 74153 N74153 SN74153	DM74196	Raytheon Signetics TI	74196 N74196 SN74196	DM7481	Raytheon	7481
DM74L187	Intersil	IM5603	DM74154	AMD Hitachi Raytheon Signetics TI	SN74154 HD2580 74154 N74154 SN74154	DM74197	Hitachi Raytheon Signetics TI	HD2504 7420 N7420 SN7420	DM7483	Hitachi Raytheon Signetics TI	HD2535 7483 N7483 SN7483A
DM74L89	MMI	L6560	DM74155	Raytheon Signetics TI	74155 N74155 SN74155	DM74198	Raytheon Signetics TI	74198 N74198 SN74198	DM7486	Hitachi Raytheon Signetics TI	HD2526 7486 N7486 SN7486
DM74S200	Signetics	N74S200	DM74156	Raytheon Signetics TI	74156 N74156 SN74156	DM74199	Raytheon Signetics TI	74199 N74199 SN74199	DM7488	Intersil MMI TI	IM5600 6230 SN7488A
DM74S387	Intel	3601-1 see page 772, 773 MMI 6300 Signetics N82S126 see page 804, 826, 835, TI SN74S387	DM74157	AMD Raytheon Signetics TI	SN74157 74157 N74157 SN74157	DM7420	Hitachi Raytheon Signetics TI	HD2504 7420 N7420 SN7420	DM7490	Hitachi Signetics TI	HD2519 N7490 SN7490A
DM7400	Fairchild Fairchild Hitachi Raytheon Signetics TI	7400 9N00 HD2503 7400 N7400 SN7400	DM74158	Raytheon	74158	DM74200	Fairchild Intersil MMI Raytheon TI	93421 IM5523 6531 RC5340 SN74S201	DM7491	Signetics TI	N7491 SN7491A
DM7401	Hitachi Raytheon Signetics TI	HD2509 7401 N7401 SN7401	DM74159	Raytheon	74159	DM7421	Raytheon	7421	DM7492	Hitachi Signetics TI	HD2521 N7492 SN7492A
DM7402	Hitachi Signetics TI	HD2511 N7402 SN7402	DM7416	Signetics TI	N7416 SN7416	DM7422	Raytheon	7422	DM7493	Hitachi Signetics TI	HD2520 N7493 SN7493A
DM7403	Hitachi Raytheon Signetics TI	HD2528 7403 N7403 SN7403	DM74160	AMD Raytheon Signetics TI	SN74160 74160 N74160 SN74160	DM7426	Signetics TI	N7426 SN7426	DM7495	Hitachi Signetics TI	HD2534 N7495 SN7495A
DM7404	Hitachi Raytheon Signetics TI	HD2522 7404 N7404 SN7404	DM74161	Raytheon	74161	DM74283	Raytheon	74283	DM7496	Hitachi Signetics	HD2546 N7496
DM7405	Hitachi Raytheon Signetics TI	HD2523 7405 N7405 SN7405	DM74162	Raytheon Signetics TI	74162 N74162 SN74162	DM7430	Hitachi Signetics TI	HD2508 N7430 SN7430	DM7560	TI	SN540192
DM7407	Signetics TI	N7407 SN7407	DM74163	AMD Raytheon Signetics TI	SN74163 74163 N74163 SN74163	DM7440	Hitachi Signetics TI	HD2501 N7440 SN7440	DM75L60	TI	SN54L193
DM7408	Hitachi Raytheon Signetics TI	HD2550 7408 N7408 SN7408	DM74164	AMD Raytheon Signetics TI	SN74164 74164 N74164 SN74164	DM7441	Hitachi Signetics TI	HD2518 N7441 SN74141	DM75L63	TI	SN54L194
DM7409	Hitachi Raytheon Signetics TI	HD2551 7409 N7409 SN7409	DM74165	Raytheon Signetics TI	74165 N74165 SN74165	DM7442	Hitachi Raytheon Signetics TI	HD2536 7442 N7442 SN7442A	DM75491	TI	SN75491
DM7410	Hitachi Raytheon Signetics TI	HD2507 7410 N7410 SN7410	DM74166	Raytheon Signetics TI	74166 N74166 SN74166	DM7443	Raytheon	7443	DM75492	TI	SN75492
DM74107	Hitachi Signetics TI	HD2530 N74107 SN74107	DM7417	Signetics TI	N7417 SN7417	DM7444	Raytheon	7444	DM7551	TI	SN54173
			DM74170	Fairchild Hitachi Raytheon Signetics	74170 HD2540 74170 N74170				DM7560	TI	SN54192

† Discontinued

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Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
National Semiconductor (cont)											
DM7563	TI	SN54193	DM8309	AMD Fairchild TI	9309 9309 SN29309	DM8574	Intel see page 772, 773 Intersil Intersil MMI TI	3621 IM5603 IM5623 6301 SN74S287	DM8894	National	DS75494
DM7570	TI	SN54164	DM8310	AMD Fairchild Raytheon TI	9310 9310 RC9310 SN29310	DM8577	AMD Harris see page 746 TI	AM27S08 HM7602 SN74S188	DM9093	Motorola Raytheon SW TI	MC853 RM993 SW9093 SN158093
DM7573	Harris Intersil MMI TI	HPROM-1024A IM5603 5300 SN54S387	DM8311	AMD Fairchild Raytheon TI	9311 9311 RC9311 SN29311	DM8578	MMI Signetics see page 804, 826, 828, TI	6331 N82S123 SN74S288	DM9094	Motorola Raytheon SW TI	MC856 RM9094 SW9094 SN158094
DM7574	AMD Harris see page 746 Harris Intersil MMI TI	AM27S09 HM7602 HPROM-1024 IM5623 5301 SN54S188 SN54S287	DM8312	AMD Fairchild Raytheon TI	9312 9312 RC9312 SN29312	DM8579	ITT	ITT79164	DM9097	Motorola SW TI	MC855 SW9097 SN158097
DM7582	Intersil TI	IM5533 SN54S301	DM8316	AMD Fairchild Raytheon TI	9316 9316 RC9316 SN29316	DM8580	Fairchild Motorola Signetics TI	9395 MC7495 N7495 SN7495A	DM9099	Motorola Raytheon SW TI	MC852 RM999 SW9099 SN158099
DM7588	Intersil TI	IM5600 SN54S188	DM8322	AMD Fairchild Raytheon Raytheon	9322 9322 RC9322 74154 74157 SN29322	DM8582	Fairchild Intersil MMI TI	93411 IM5533 6530 SN74S301	DM930	Motorola Raytheon SW TI	MC830 RM930 SW930 SN15830
DM7590	TI	SN54165	DM85L60	TI	SN74L192	DM8588	Fairchild Intersil ITT TI	93434 IM5600 ITT7488A SN74S188	DM9301	AMD TI	9301 SN29301
DM7597	Intersil MMI TI	IM5623 5201 SN54S287	DM85L63	TI	SN74L193	DM8590	Fairchild ITT Raytheon TI	93165 ITT74165 74165 SN74165	DM9312	AMD TI	9312 SN29312
DM7598	Intersil MMI	IM5610 5231	DM85S99	AMD	SN74S189 SN74S189	DM8597	Intersil MMI TI	IM5623 6201 SN74S287	DM932	Motorola Raytheon SW TI	MC832 RM932 SW932 SN15838
DM7599	AMD AMD MMI TI	AM27S03 DM7599 5561 SN54S189	DM8500	Signetics TI	N7476 SN7476	DM8598	Intersil MMI TI	IM5610 6231 SN74S288	DM9322	AMD Raytheon Raytheon TI	9322 RM9322 54157 SN29322
DM76L97	Intersil	IM5623	DM8501	Signetics TI	N7473 SN7473	DM8599	AMD AMD MMI TI	AM27S03 DM8599 6561 SN74S189	DM935	Motorola Raytheon SW TI	MC840 RM935 SW935 SN15835
DM76L99	Intersil MMI	IM5501 L5561	DM8510	Signetics TI	N7474 SN7474	DM86L97	Intersil	IM5623	DM936	Motorola Raytheon SW TI	MC836 RM936 SW936 SN15836
DM7795	MMI	A5240	DM8530	Fairchild Motorola Signetics TI	9390 MC7490 N7490 SN7490A	DM8600	Motorola	MC8300	DM937	Motorola Raytheon SW TI	MC837 RM937 SW937 SN15837
DM7796	MMI	5241	DM8532	Fairchild Motorola Signetics TI	9392 MC7492 N7492 SN7492A	DM8601	AMD Fairchild Raytheon Signetics TI	9601 9601 RF8601 N8T22 SN29601	DM944	Motorola Raytheon SW TI	MC844 RM944 SW944 SN15844
DM7800	TI	SN55180	DM8533	Fairchild Motorola Signetics TI	9393 MC7493 N7493 SN7493A	DM8602	AMD Fairchild Raytheon	9602 9602 RF8602	DM945	Motorola Raytheon SW TI	MC845 RM945 SW945 SN15845
DM7810	TI	SN5426	DM8550	Fairchild Motorola Signetics TI	9375 MC7475 N7475 SN7475	DM8640	TI	SN74141	DM946	Motorola Raytheon SW TI	MC846 RM946 SW946 SN15846
DM7812	TI	SN5416	DM8551	TI	SN74173	DM8680	Signetics	N8280	DM948	Motorola Raytheon SW TI	MC848 RM948 SW948 SN15848
DM7860	National	DS55491	DM8553	Fairchild Hitachi ITT Motorola Raytheon Signetics TI	9360 HD2541 ITT74192 MC74192 74192 N74192 SN74192	DM8681	Signetics	N8281	DM949	Motorola Raytheon SW TI	MC849 RM949 SW949 SN15849
DM7862	National	DS55492	DM8556	Fairchild Hitachi ITT Motorola Raytheon Signetics TI	9366 HD2542 ITT74193 MC74193 74193 N74193 SN74193	DM8688	Signetics	N8288	DM951	Motorola Raytheon SW TI	MC851 RM951 SN15851
DM7893	National	DS55493	DM8570	Fairchild Motorola Raytheon TI	93164 MC74164 74164 SN74164	DM8795	MMI	A6240	DM9567	Motorola	MC857
DM7894	National	DS55494	DM8573	Fairchild Harris Intel see page 772, 773 Intersil MMI Signetics see page 804, 826, 835, TI	93416 HPROM-1024A 3601 IM5603 6300 N82S126 SN74S387	DM8796	MMI	6241	DM957	Raytheon SW TI	RM957 SW957 SN15857
DM8093	TI	SN74125	DM8574	Fairchild Harris	93426 HPROM-1024	DM8810	ITT	ITT7426	DM958	Motorola	MC858
DM8094	TI	SN74126				DM8840	Hitachi Motorola Signetics	HD2558 MC7441 N7441		Raytheon SW TI	RM958 SW958 SN15858
DM8095	TI	SN74365				DM8842	Motorola Signetics TI	MC7442 N7442 SN7442A			
DM8096	TI	SN74366				DM8844	Motorola TI	MC7446 SN7446A			
DM8097	TI	SN74367				DM8847	Motorola TI	MC7447 SN7447A			
DM8098	TI	SN74368				DM8848	Motorola TI	MC7448 SN7448			
DM81L22	TI	SN74L157				DM8850	Motorola Signetics TI	MC9601 N8T22 SN29601			
DM81S60	Fairchild	93S47				DM8860	National	DS75491			
DM8200	Signetics	N8269				DM8862	National	DS75492			
DM8213	Fairchild ITT Motorola Raytheon Signetics TI	9311 ITT74154 MC8311 RC9311 N74154 SN74154				DM8889	Motorola	MC3491			
DM8220	Hitachi	HD2525				DM8893	National	DS75493			
DM8280	Fairchild Raytheon Signetics TI	93176 RC8280 N8280 SN74176									
DM8281	Fairchild Raytheon Signetics TI	93177 RC8281 N8281 SN74177									
DM8283	Fairchild Motorola Signetics TI	9383 MC7483 N7483 SN7483A									
DM8288	Signetics	N8288									
DM8290	Fairchild Raytheon	93196 RC8290									
DM8291	Fairchild Raytheon TI	93197 RC8291 SN74197									
DM8296	TI	SN74196									
DM8300	AMD Fairchild Raytheon TI	9300 9300 RC9300 SN29300									
DM8301	AMD TI	9301 SN29301									

† Discontinued

ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device
National Semiconductor (cont)							
DM958	TI SN15858	DS75207	TI SN75207	DS75454	Raytheon Signetics Teledyne S TI RC75454 75454 SN75454	LM104	Fairchild Motorola NPC Raytheon Silicon G Teledyne S TI μ A104 MLM104 SFC2104 LM104 SG104 LM104 SN52104
DM9601	AMD Raytheon TI 9601 RF9601 SN29601	DS75208	TI SN75208	DS75460	TI SN75460		
DM9602	AMD Raytheon 9602 RF9602	DS7521	ITT Motorola Signetics Silicon G TI ITT7521 MC7521 SN7521 SG7521 SN7521	DS75461	TI SN75461		
DM961	Motorola Raytheon SW TI MC861 RM961 SW961 SN15861	DS7522	ITT Motorola Signetics Silicon G TI ITT7522 MC7522 SN7522 SG7522 SN7522	DS75462	TI SN75462	LM105	AMD Fairchild Intersil Motorola NPC Raytheon Silicon G Teledyne S TI LM105 μ A105 LM105 MLM105 DM7820 DM7820 SN55182
DM962	Motorola Raytheon SW TI MC862 RM962 SW962 SN15862	DS7523	ITT Motorola Signetics Silicon G TI ITT7523 MC7523 SN7523 SG7523 SN7523	DS7820	AMD Signetics TI DM7820 DM7820 SN55182		
DM963	Motorola Raytheon SW TI MC863 RM963 SW963 SN15863	DS7524	Fairchild ITT Motorola Signetics Silicon G TI 7524 ITT7524 MC7524 SN7524 SG7524 SN7524	DS7830	AMD Signetics TI DM7830 DM7830 SN55183	LM106	AMD Raytheon TI LM106 LM106 SN52106
DS0026	AMD Intersil MH0026 IM5013	DS7525	Fairchild ITT Motorola NPC Signetics Silicon G TI 7525 ITT7525 MC7525 SFC2525 SN7525 SG7525 SN7525	DS7831	AMD DM7831	LM107	AMD AD see page 625 Fairchild Intersil Motorola NPC Raytheon RCA see page 661 Signetics Silicon G Teledyne S TI LM107 AD741S LM107 LM107 LM107 CA107 LM107 SG107 LM107 SN52107
DS1488	AMD Exar Harris ITT Raytheon TI MC1488 XR1488 HD1488 ITT1488 RC1488 SN75188	DS7528	Fairchild ITT Motorola NPC Silicon G TI 7528 ITT7528 MC7528 SFC2528 SG7528 SN7528	DS8820	AMD AMD Signetics TI AM8820 DM8820 DM8820 SN75182		
DS1489	AMD Exar Harris ITT Motorola Raytheon Signetics TI MC1489 XR1489 HD1489 ITT1489 RC1489 SN75189	DS7529	Fairchild ITT Motorola Silicon G TI 7529 ITT7529 MC7529 SG7529 SN7529	DS8830	AMD AMD Signetics TI AM8830 DM8830 DM8830 SN75183		
DS55107	AMD Raytheon TI SN55107B RM55107A SN55107	DS75324	Raytheon TI RC75324 SN75324	DS8831	AMD DM8831	LM108	AMD AD see page 625 Fairchild Intersil Motorola Raytheon RCA Signetics Silicon G TI LM108 AD108 LM108 μ A108 LM108 MLM108 LM108 CA108 LM108 SG108 LM107 SN52108
DS55108	AMD Raytheon TI SN55108B RM55108A SN55108	DS75325	Fairchild ITT Motorola Raytheon 75325 ITT75325 MC75325 RC75325	DS8832	AMD DM8832		
DS55109	AMD Raytheon TI SN55109 RM55109 SN55109	DS7534	Fairchild Motorola TI 7534 MC7534 SN75232	DS8880	Signetics DM8880		
DS55110	AMD TI SN55110 SN55110	DS7535	Fairchild Motorola TI 7535 MC7535 SN75233	DS8881	AMD DM8881		
DS5520	TI SN5520	DS7538	Motorola MC7538	DS8882	AMD DM8882		
DS5521	TI SN5521	DS7539	Motorola MC7539	DS8883	AMD DM8883		
DS5522	TI SN5522	DS7540	Fairchild 75450	DS8880	Signetics DM8880		
DS5523	TI SN5523	DS75450	Fairchild Motorola Raytheon Signetics Teledyne S TI 75450 MC75450 RM75450 75450 75450 SN75450	INS4001	Intel 4001		
DS5524	TI SN5524	DS75451	Fairchild Motorola Raytheon Signetics Teledyne S TI 75451 MC75451 RC75451 75451 75451 SN75451	INS4002	Intel 4002		
DS5525	TI SN5525	DS75452	Fairchild Motorola Raytheon Signetics TI 75452 MC75452 RC75452 75452 75452 SN75452	INS4003	Intel 4003		
DS5528	TI SN5528	DS75453	Fairchild Motorola Raytheon Signetics TI 75453 MC75453 RC75453 75453 75453 SN75453	INS4004	Intel 4004		
DS5529	TI SN5529	DS75454	Fairchild 75454	INS4008	Intel 4008		
DS55325	TI SN55325			INS4009	Intel 4009		
DS5534	TI SN5534			LH0042	AD Intersil Teledyne S AD0042 LH0042 2740		
DS5535	TI SN5535			LH0052	AD see page 624 AD506		
DS75107	AMD ITT Motorola Raytheon TI SN75107B ITT75107 MC75107 RC75107A SN75107			LH0062	AD see page 624 AD528		
DS75108	AMD ITT Motorola Raytheon TI SN75108B ITT75108 MC75108 RC75108A SN75108			LH101	Raytheon TI LH101 SN52107		
DS75109	AMD ITT Motorola Raytheon TI SN75109 ITT75109 MC75109 RC75109 SN75109			LH201	Raytheon Siliconix LH201 LH201		
DS75110	AMD ITT Motorola Raytheon TI SN75110 ITT75110 MC75110 RC75110 SN75110			LH2101	Intersil LH2101		
DS7520	ITT Motorola Signetics Silicon G TI ITT7520 MC7520 SG7520 SN7520			LH2108	Intersil LH2108	LM110	AMD Fairchild Intersil Motorola Silicon G TI LM110 μ A110 LM110 MLM110 SG110 SN52110
				LH2110	Intersil LH2110		
				LH2111	Intersil LH2111		
				LH2301	Intersil LH2301		
				LH2308	Intersil LH2308		
				LH2310	Intersil LH2310		
				LH2311	Intersil LH2311	LM111	AMD Fairchild Harris Intersil Motorola NPC Raytheon RCA see page 661 Signetics Silicon G TI LM111 μ A111 HA-2111 LM111 MLM111 SFC2111 LM111 SFC2100 CA111 LM111 SN52111
				LH740	Fairchild Intersil Signetics μ A740 LH740 μ A740	LM112	AMD Raytheon LM112 LM112
				LM100	Intersil NPC Silicon G LM100 SFC2100 SG100		
				LM101	AMD AD see page 625 Fairchild Intersil Motorola NPC Raytheon RCA see page 661 Signetics Silicon G Siliconix Teledyne S TI LM101 AD101 μ A101 LM101 MLM101 SFC2101 LM101 CA101 CA748 LM101 SG101 LM101 LM101 SN52101	LM118	AMD AD see page 624 Signetics Raytheon TI LM118 AD518 LM118 SN52118
				LM102	AMD Fairchild Intersil Motorola Silicon G LM102 μ A102 LM102 MLM110 SG102	LM120	Fairchild Silicon G 78N00 SG120
						LM124	Intersil Raytheon RCA LM124 LM124 CA124 see page 661

† Discontinued

The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	
National Semiconductor (cont)												
LM124	Signetics	LM124	LM200	Intersil	LM200	LM212	AMD	LM212	LM3067	Sprague	ULN-2267	
	Silicon G	SG124		NPC	SFC2200		Raytheon	LM212				
	Teledyne S	LM124		Silicon G	SG200	LM216	AMD	LM216	LM307	AMD	LM307	
	TI	LM124	LM201	AMD	LM201		Raytheon	LM216		AD	AD741R	
LM1303	Motorola	MC1303		AD	AD201	LM218	AD	AD518		Fairchild	μA307	
	Raytheon	RC4739		see page 625			see page 624			Intersil	LM307	
LM1304	Motorola	MC1304		Fairchild	μA201	LM224	Intersil	LM224		Motorola	MLM307	
	Sprague	ULN-2120		Intersil	LM201		Raytheon	LM224		NPC	SFC2307	
LM1305	Motorola	MC1305		Motorola	MLM201		RCA	LM224		Raytheon	LM307	
	Sprague	ULN-2122		NPC	SFC2201		see page 661	RCA	CA307			
LM1307	Motorola	MC1307		Raytheon	LM201		Signetics	LM224		Signetics	LM307	
	Sprague	ULN-2128		RCA	CA201		Silicon G	SG224		Silicon G	SG307	
LM1310	Exar	XR1310		see page 661			Teledyne S	LM224		Teledyne S	LM307	
	Motorola	MC1310		RCA	CA748		TI	LM224		TI	SN72307	
	Sprague	ULN-2210		Signetics	LM201	LM239	Intersil	LM248	LM3070	Motorola	MC1370	
LM1351	Motorola	MC1351		Silicon G	SG201		Motorola	MC3302		Sprague	ULN-2124	
LM139	Raytheon	LM139	LM202	Intersil	LM202		Raytheon	LM239	LM3071	Motorola	MC1371	
	RCA	CA139		Motorola	MLM210		RCA	CA239		Sprague	ULN-2127	
	see page 661			Silicon G	SG202		see page 661		LM3075	Motorola	MC1375	
	Silicon G	SG139	LM204	Motorola	MLM204	LM249	Intersil	LM249		Sprague	ULN-2129	
	Teledyne S	LM139		NPC	SFC2204	LM258	Raytheon	LM258	LM308	AMD	LM308	
LM140-05	Silicon G	SG140-05		Raytheon	LM204					AD	AD308	
LM140-06	Silicon G	SG140-06		Silicon G	SG204	LM270	Lithic Sys	LS270		see page 625		
LM140-08	Silicon G	SG140-08		Teledyne S	LM204	LM271	Lithic Sys	LS271		Fairchild	LM308	
LM140-12	Silicon G	SG140-12	LM205	AMD	LM205	LM2900	Raytheon	LM2900		Intersil	LM308	
LM140-15	Silicon G	SG140-15		Intersil	LM205	LM2901	Raytheon	LM2901		Motorola	MLM308	
LM140-18	Silicon G	SG140-18		Motorola	MLM205	LM2901	Raytheon	LM2901		Raytheon	LM308	
LM140-24	Silicon G	SG140-24		NPC	SFC2205	LM2902	Teledyne S	LM2901		RCA	CA308	
LM1414	Motorola	MC1414		Raytheon	LM205		Motorola	MLM2902		Signetics	LM308	
	Raytheon	RC1414		Silicon G	SG205	LM300	Raytheon	LM2902		Silicon G	SG308	
	TI	SN72514		Teledyne S	LM205		Intersil	LM300	LM309	Fairchild	μA309	
LM1458	Harris	HA-2655	LM207	AMD	LM207		NPC	SFC2300		Motorola	MLM309	
	Motorola	MC1458		AD	AD741J	LM301	Silicon G	SG300		NPC	SFC2309	
	PMI	SSS1458		see page 625			AMD	LM301		Raytheon	LM309	
	Raytheon	RC1458		Fairchild	μA207		AD	AD301		Signetics	LM309	
	RCA	CA1458		Harris	HA-2207		see page 625			Silicon G	SG309	
	Signetics	MC1458		Intersil	LM207		Fairchild	μA301	LM310	TI	SN72309	
	Silicon G	SG1458		Motorola	MLM207		Harris	HA-2301		AMD	LM310	
	Teledyne S	1458		NPC	SFC2207		Intersil	LM301		Fairchild	μA310	
	TI	SN72558		Raytheon	LM207		Motorola	MLM301		Intersil	LM310	
LM148	Intersil	LM148		RCA	CA207		NPC	SFC2301		Motorola	MLM310	
LM1488	National	DS1488		see page 661			Raytheon	LM301		Silicon G	SG310	
LM1489	National	DS1489		Signetics	LM207		RCA	CA301		TI	SN72310	
LM149	Intersil	LM149		Silicon G	SG207		see page 661		LM311	AMD	LM311	
LM1496	Lithic Sys	LS1496	LM208	AMD	LM208		Signetics	LM301		Fairchild	μA311	
	Motorola	MC1496		AD	AD208		Silicon G	SG301		Raytheon	HA-2311	
	Signetics	MC1496		see page 625		LM3018	Teledyne S	LM301		Intersil	LM311	
	Silicon G	SG1496		Fairchild	μA208		TI	SN52301		Motorola	MLM311	
LM1514	Motorola	MC1514		Intersil	LM208	LM302	Lithic Sys	LA3018		NPC	SFC2311	
	Raytheon	RM1514		Motorola	MLM208		AMD	LM302		Raytheon	LM311	
	TI	SN56514		Raytheon	LM208		Fairchild	μA302		RCA	CA311	
LM1558	Fairchild	μA1558		RCA	CA208		Intersil	LM302		see page 661		
	Harris	HA-2650		Signetics	LM208		Motorola	MLM310		Signetics	LM311	
	Motorola	MC1558		Silicon G	SG208		Silicon G	SG302		Silicon G	SG311	
	PMI	SSS1558		Teledyne S	LM207		TI	SN72302		Teledyne S	LM311	
	Raytheon	RM1558		LM209	Fairchild	μA209	LM3028	Lithic Sys	LS3028		TI	SN72311
	RCA	CA1558		Motorola	MLM209				LM312	AMD	LM312	
	Signetics	MC1558		NPC	SFC2209		LM304	Fairchild		Raytheon	LM312	
	Silicon G	SG1558		Raytheon	LM209			Motorola				
	Teledyne S	1558		Silicon G	SG209			NPC				
	TI	SN52558		LM210	AMD	LM210		Raytheon				
LM158	Raytheon	LM158		Fairchild	μA210			Silicon G				
	Raytheon	RM4139		Intersil	LM210			Teledyne S				
LM1596	Lithic Sys	LS1596		Motorola	MLM210			TI				
	Motorola	MC1596						TI				
	Signetics	MC1596		LM211	AMD	LM211		TI				
	Silicon G	SG1596						TI				
LM160	Fairchild	μA760						TI				
LM1611	National	DS1611						TI				
LM1612	National	DS1612						TI				
LM1613	National	DS1613						TI				
LM1614	National	DS1614						TI				
LM1625	National	DS1615						TI				
LM163	National	DS1603						TI				
LM163A	National	DS1604						TI				
LM170	Lithic Sys	LS170						TI				
LM171	Lithic Sys	LS171						TI				
LM1800	Exar	XR1800						TI				
	Sprague	ULN-2244						TI				
LM1820	Fairchild	μA720						TI				
	Sprague	ULN-2137						TI				

† Discontinued

ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
National Semiconductor (cont)			LM5528	NPC	SFC2528	LM741	AD	AD741	MH0056	National	DS0056
LM339	Silicon G	SG339	LM5529	National	DS5529	see page 625	Fairchild	μ A741	MH7803	National	DS7803
	Teledyne S	LM339	LM55324	National	DS55324		Intersil	SSS741	MH7808	National	DS7808
LM340-05	Fairchild	μ A7805	LM55325	National	DS55325		Intersil	741	MH8803	National	DS8803
	Motorola	MC7805		Raytheon	RM55325		Motorola	MC1741	MH8808	National	DS8808
	Raytheon	RC7805	LM5534	National	DS5534		NPC	SFC2741	MMKJC904	Harris	HD54C904
	Silicon G	SG340-05	LM5535	National	DS5535		PMI	SSS741	MM1101	AMD	1101
	Ti	SN72905	LM5539	National	DS5539		Raytheon	RC741		Intersil	IM7501
LM340-06	Fairchild	μ A7806	LM5540	National	DS5540		Raytheon	RM741		Intersil	IM7511
	Motorola	MC7806	LM55450	National	DS55450		RCA	CA741		Intersil	IM7512
	Raytheon	RC7806	LM5539	National	DS5539		see page 661	Signetics	μ A741	Mostek	MK4007
	Silicon G	SG340-06	LM55450	National	DS55450		Silicon G	SG741		Signetics	2501
	Ti	SN72906	LM55451	National	DS55451		Teledyne S	741	MM1103	Signetics	1103
LM340-08	Fairchild	μ A7808	LM55452	National	DS55452	LM746	Motorola	MC1328	MM1402	AMD	1402
	Motorola	MC7808	LM55454	National	DS55454		Sprague	ULN-2114		AD	S2502
	Raytheon	RC7808	LM555	Exar	XR555	LM747	AMD	747	MM1403	AMD	1403
	Silicon G	SG340-08		Intersil	LM555		Fairchild	μ A747		AMI	S2503
	Ti	SN72908		Lithic Sys	LS555		Intersil	SSS747		Motorola	MC2385
LM340-12	Fairchild	μ A7812		Motorola	MC1455		Motorola	MC1747		Motorola	MC2385
	Motorola	MC7812		Motorola	MC1555		PMI	SSS747		Synertek	SY1403
	Raytheon	RC7812		Raytheon	RC555		Raytheon	RC747	MM1404	AMD	1404
	Silicon G	SG340-12		Raytheon	RM555		Raytheon	RM747		AMI	S2504
	Ti	SN72912		RCA	CA555		RCA	CA747		Motorola	MC2386
LM340-15	Fairchild	μ A7815		see page 661			see page 661	Signetics	μ A747	Synertek	SY1404
	Fairchild	μ A7818		Signetics	NE555		Silicon G	SG747	MM2102	Mostek	MK4102
	Motorola	MC7815		Ti	SN52555		Teledyne S	747	MM2521	AMD	AM2521
	Silicon G	SG340-15	LM565	Signetics	NE565		Ti	SN52747		Signetics	2521
	Ti	SN72915	LM566	Signetics	NE566	LM748	AMD	748	MM2522	Signetics	2522
LM340-18	Motorola	MC7818	LM567	Exar	XR567		Intersil	LM748	MM2533	AMD	AM2533
	Raytheon	RC7818		Signetics	NE567		Motorola	MC1748		Signetics	2533
	Silicon G	SG340-18	LM709	Fairchild	μ A709		NPC	SFC2748	MM2602	Signetics	2602
	Ti	SN72918		Motorola	MC1709		Raytheon	RC748	see page 790		
LM340-24	Fairchild	μ A7824		NPC	SFC2709		Raytheon	RM748	MM4020	Intersil	IM7780
	Motorola	MC7824		Raytheon	RC709		RCA	CA748	MM4060	Ti	TMS3128
	Raytheon	RC7824		Signetics	μ A748		Signetics	μ A748		Ti	TMS3129
	Silicon G	SG340-24		Silicon G	SG748		Silicon G	SG748		Ti	TMS3130
	Ti	SN72924		Teledyne S	709		Teledyne S	748		Ti	TMS3131
LM343	Motorola	MC1439		Ti	SN52709		Ti	SN52748		Ti	TMS3132
LM350	National	DS350	LM710	Fairchild	μ A710	LM75107A	National	DS75107	MM423	AMI	S8773
LM351	National	DS75453		Motorola	MC1710	LM75108A	National	DS75108	MM4232	Mostek	MK2500
LM354	NPC	SFC2524		NPC	SFC2710	LM7520	National	DS7520	MM4240	AMI	S8614
	NPC	SFC2525		Raytheon	RC710	LM75207	National	DS75207	MM452	Siliconix	S1452
LM358	Raytheon	LM358		Raytheon	RM710	LM75208	National	DS75208	MM455	Siliconix	S1455
	Raytheon	RC4139		RCA	CA710	LM7521	National	DS7521	MM5013	AMI	S2512A
LM360	Fairchild	760		Signetics	μ A710	LM7522	National	DS7522		Signetics	2512
LM3611	National	DS3611		Silicon G	SG710	LM7523	National	DS7523		Signetics	2525
LM3612	National	DS3612		Teledyne S	710	LM7524	National	DS7524	MM5016	AMI	S1865
LM3613	National	DS3613		Ti	SN52710	LM7524	National	DS7524	MM5020	Intersil	IM7780
LM3614	National	DS3614	LM711	Fairchild	μ A711	LM7525	National	DS7525	MM5025	Synertek	SY5025
LM3625	National	DS3625		Motorola	MC1711	LM7528	National	DS7528	MM5026	Synertek	SY5026
LM363	National	DS3603		NPC	SFC2711	LM7529	National	DS7529	MM5027	Synertek	SY5027
LM363A	National	DS3604		Raytheon	RC711	LM75324	National	DS75324	MM5054	AMI	S2181
LM370	Lithic Sys	LS370		Raytheon	RM711	LM75325	National	DS75325	MM5055	AMD	5055
LM371	Lithic Sys	LS371		RCA	CA711	LM7534	National	DS7534	MM5056	AMD	5056
LM376	Fairchild	μ A376		Signetics	μ A711	LM7535	National	DS7535	MM5057	AMD	5057
	NPC	SFC2376		Silicon G	SG711	LM7538	National	DS7538	MM5058	Ti	TMS3133
	Teledyne S	LM376		Teledyne S	711	LM7539	National	DS7539	MM506	Signetics	2506
	Ti	SN72376		Ti	SN52711	LM7540	National	DS7540	MM5060	AMI	S2181
LM377	Sprague	ULN-2278	LM723	AMD	723	LM75451	National	DS75451	MM5230	Motorola	MCM1112
LM380	Sprague	ULN-2280		Fairchild	μ A723	LM75452	National	DS75452		Nitron	NCM1112
LM3900	Motorola	MC3401		Intersil	723	LM75454	National	DS75454	MM5231	AMI	S5232
	Raytheon	RC3302		Motorola	MC1723	LM7805	Signetics	7805	see page 706	Nitron	NCM1110
LM3901	Motorola	MC3302		NPC	SFC2723		see page 668	Signetics	7806	Mostek	MK2500
	Raytheon	MC3302		Raytheon	RC723	LM7806	see page 668	see page 668	7806	Mostek	MK2600
LM4250	Fairchild	μ A776		Raytheon	RM723			MM5233	AMI	S3514	
	Harris	HA-2720		RCA	CA723			see page 706	see page 706		
	Intersil	LM4250		Signetics	μ A723			MM5232	Mostek	MK2500	
	Silicon G	SG4250		Silicon G	SG723			MM5233	Mostek	MK2600	
LM55107A	National	DS55107		Teledyne S	723						
LM55108A	National	DS55108		Ti	SN52723						
LM55109	National	DS55109	LM725	AMD	725						
LM5520	National	DS5520		Fairchild	μ A725						
LM55207	National	DS55207		Intersil	SSS725						
LM55208	National	DS55208		PMI	SSS725						
LM5521	National	DS5521		Raytheon	RC725						
LM5522	National	DS5522		Raytheon	RM725						
LM5523	National	DS5523									
LM5524	National	DS5524		AMD	733						
	NPC	SFC2524		Fairchild	μ A733						
LM5525	National	DS5525		Motorola	MC1733						
	NPC	SFC2525		Raytheon	RC733						
LM5528	National	DS5528		Raytheon	RM733						
				Signetics	μ A733						
				Ti	SN52733						
			LM741	AMD	741						
						MH0013	Intersil	IM5013			
						MH0025	National	DS0025			
						MH0026	National	DS0026			

1 Discontinued

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Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
National Semiconductor (cont)			MM74C08	Harris	HD74C08	MM74C10	Harris	HD74C10	NH00016	Fairchild	SH2200
MM54C107	Harris	HD54C107	MM74C10	Teledyne S	MM74C10	MM74C107	Harris	HD74C107	NH00017	Fairchild	SH2200
MM54C151	Harris	HD54C151	MM74C107	Teledyne S	MM74C107	MM74C151	Harris	HD74C151	NH00018	Fairchild	SH2200
MM54C154	Harris	HD54C154	MM74C151	Teledyne S	MM74C151	MM74C154	Harris	HD74C154	Nitron		
MM54C157	Harris	HD54C157	MM74C154	Teledyne S	MM74C154	MM74C157	Harris	HD74C157	NCM1110	Motorola	MCM1110
MM54C160	Harris	HD54C160	MM74C157	Teledyne S	MM74C157	MM74C160	Harris	HD74C160	National	MM5231	MCM1111
MM54C161	Harris	HD54C161	MM74C160	Teledyne S	MM74C160	MM74C161	Harris	HD74C161	TI	2430	2461
MM54C162	Harris	HD54C162	MM74C161	Teledyne S	MM74C161	MM74C162	Harris	HD74C162	Motorola	MCM1112	MCM1112
MM54C163	Harris	HD54C163	MM74C162	Teledyne S	MM74C162	MM74C163	Harris	HD74C163	National	MM5230	MCM1120
MM54C164	Harris	HD54C164	MM74C163	Teledyne S	MM74C163	MM74C164	Harris	HD74C164	TI	TMS2400	MCM1121
MM54C165	Harris	HD54C165	MM74C164	Teledyne S	MM74C164	MM74C165	Harris	HD74C165	Motorola	MCM1122	MCM1122
MM54C173	Harris	HD54C173	MM74C165	Teledyne S	MM74C165	MM74C173	Harris	HD74C173	Motorola	MCM1130	MCM1130
MM54C174	Harris	HD54C174	MM74C173	Teledyne S	MM74C173	MM74C174	Fairchild	F40174	TI	TMS4100	MCM1131
MM54C175	Harris	HD54C175	MM74C174	Teledyne S	MM74C174	MM74C175	Harris	HD74C175	Motorola	MCM1140	MCM1140
MM54C192	Harris	HD54C192	MM74C175	Teledyne S	MM74C175	MM74C192	Harris	HD74C192	TI	TMS4300	MCM1131
MM54C193	Harris	HD54C193	MM74C192	Teledyne S	MM74C192	MM74C193	Harris	HD74C193	Motorola	MCM6560	MCM6561
MM54C195	Harris	HD54C195	MM74C193	Teledyne S	MM74C193	MM74C195	Harris	HD74C195	Motorola	MCM6570	MCM6571
MM54C20	Harris	HD54C20	MM74C195	Teledyne S	MM74C195	MM74C20	Harris	HD74C20	Motorola	MCM6572	MCM6572
MM54C200	Harris	HD54C200	MM74C20	Teledyne S	MM74C20	MM74C200	Harris	HD74C200	Motorola	MCM6580	MCM6581
MM54C221	Harris	HD54C221	MM74C200	Teledyne S	MM74C200	MM74C221	Harris	HD74C221	Motorola	MCM6581	MCM6581
MM54C30	Harris	HD54C30	MM74C221	Teledyne S	MM74C221	MM74C30	Harris	HD74C30	Motorola	MCM6583	MCM6583
MM54C32	Harris	HD54C32	MM74C30	Teledyne S	MM74C30	MM74C32	Harris	HD74C32	Motorola	MCM6590	MCM6590
MM54C42	Harris	HD54C42	MM74C32	Teledyne S	MM74C32	MM74C42	Harris	HD74C42	Motorola	MCM6832	MCM6832
MM54C48	Harris	HD54C48	MM74C42	Teledyne S	MM74C42	MM74C48	Harris	HD74C48	Motorola	S2567	S2567
MM54C73	Harris	HD54C73	MM74C48	Teledyne S	MM74C48	MM74C73	Harris	HD74C73	Motorola	AMI	S2566
MM54C74	Harris	HD54C74	MM74C73	Teledyne S	MM74C73	MM74C74	Harris	HD74C74	Motorola	AMI	S2555
MM54C76	Harris	HD54C76	MM74C74	Teledyne S	MM74C74	MM74C76	Harris	HD74C76	National	MM5555	MM5555
MM54C83	Harris	HD54C83	MM74C76	Teledyne S	MM74C76	MM74C83	Harris	HD74C83	Motorola	MC2257	MC2257
MM54C85	Harris	HD54C85	MM74C83	Teledyne S	MM74C83	MM74C85	Fairchild	F40085	Motorola	MC2259	MC2259
MM54C86	Harris	HD54C86	MM74C85	Teledyne S	MM74C85	MM74C86	Harris	HD74C86	Motorola	MC2260	MC2260
MM54C901	Harris	HD54C901	MM74C86	Teledyne S	MM74C86	MM74C88	Harris	HD74C88	Nortec Electronics		
MM54C902	Harris	HD54C902	MM74C88	Teledyne S	MM74C88	MM74C89	Harris	HD74C89	2222	AMI	S2222
MM54C903	Harris	HD54C903	MM74C89	Teledyne S	MM74C89	MM74C901	Harris	HD74C901	6002	TI	TMS4062
MM54C906	Harris	HD54C906	MM74C901	Teledyne S	MM74C901	MM74C902	Harris	HD74C902	6003	TI	TMS6002
MM54C907	Harris	HD54C907	MM74C902	Teledyne S	MM74C902	MM74C903	Harris	HD74C903	Plessey Semiconductors		
MM54C95	Harris	HD54C95	MM74C903	Teledyne S	MM74C903	MM74C904	Harris	HD74C904	SL3045	RCA	CA3045
MM551	AMI	MX52D	MM74C904	Teledyne S	MM74C904	MM74C95	Harris	HD74C95	SL3046	RCA	CA3046
MM552	Siliconix	S1552	MM74C95	Teledyne S	MM74C95	MM80C95	Harris	HD80C95	SL3086	RCA	CA3086
MM555	Siliconix	S1555	MM80C95	Teledyne S	MM80C95	MM80C97	Fairchild	F40097	SP1001	Motorola	MC1001
MM5555	Nitron	NCM1183	MM80C97	Teledyne S	MM80C97	MM80C98	Harris	HD80C98	SP1002	Motorola	MC1002
MM5556	Nitron	NC1184	MM80C98	Teledyne S	MM80C98	MM80C99	Fairchild	F40098	SP1003	Motorola	MC1003
MM601	Motorola	MC14001	MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	SP1004	Motorola	MC1004
MM602	Motorola	MC14002	MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	SP1005	Motorola	MC1005
MM70C95	Harris	HD70C95	MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	SP1006	Motorola	MC1006
MM70C97	Harris	HD70C97	MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	SP1007	Motorola	MC1007
MM74C00	Harris	HD74C00	MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	SP1008	Motorola	MC1008
MM74C02	Harris	HD74C02	MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	SP1009	Motorola	MC1009
MM74C04	Harris	HD74C04	MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	SP1010	Motorola	MC1010
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	SP1011	Motorola	MC1011
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	SP1012	Motorola	MC1012
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	SP1013	Motorola	MC1013
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	SP1014	Motorola	MC1014
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	SP1015	Motorola	MC1015
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	Precision Monolithics		
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	† SSS108	RCA	CA108
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	SSS1408	Motorola	MC1408
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	SSS1508	Motorola	MC1508
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	† SSS208	RCA	CA208
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	† SSS308	RCA	CA308
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	SSS747	AMD	SSS747
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	Raytheon Semiconductor		
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	LM101	AMD	LM101
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	Intersil	LM101	LM101
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	National	LM101	LM101
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	RCA	CA101	CA101
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	see page 661		
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	Signetics	LM101	LM101
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	Silicon G	SG101	SG101
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	Teledyne S	LM101	LM101
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	TI	SN52101	SN52101
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	LM105	AMD	LM105
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	Intersil	LM105	LM105
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	National	LM105	LM105
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	Silicon G	SG105	SG105
			MM80C99	Teledyne S	MM80C99	MM80C99	Harris	HD80C99	Teledyne S	LM105	LM105

† Discontinued

ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
Raytheon Semiconductor (cont)			LM308	AMD	LM308	RC747	Signetics	μA747	RC944	TI	SN15844
LM106	AMD	LM106	Intersil	LM308	RC748	Teledyne S	747	RC945	Motorola	MC845	MC845
	TI	SN52106	RCA	CA308		AMD	748		TI	SN15845	SN15845
LM107	AMD	LM107	Signetics	LM308		Intersil	748	RC946	Motorola	MC846	MC846
	Intersil	LM107	Silicon G	SG308		RCA	CA748		TI	SN15846	SN15846
	National	LM107	Teledyne S	LM308		Signetics	μA748	RC948	Motorola	MC848	MC848
	RCA	CA107				Teledyne S	748		TI	SN15848	SN15848
	see page 661		LM309	Silicon G	SG309	RC7489	Intersil	IM5501	RC949	Motorola	MC849
	Signetics	LM107	LM311	AMD	LM311	† RC7520	Signetics	7520		TI	SN15849
	SG107	LM107	Harris	HA-2311			Silicon G	SG7520	RC950	Motorola	MC850
	Teledyne S	LM107	Intersil	LM311		† RC7521	Signetics	7521		TI	SN15850
	TI	SN52107	National	LM311			Silicon G	SG7521	RC951	Motorola	MC851
LM108	AMD	LM108	RCA	CA311		† RC7522	Signetics	7522		TI	SN15851
	Intersil	LM108	see page 661				Silicon G	SG7522	RC957	Motorola	MC857
	National	LM108	Signetics	LM311		RC7523	Signetics	7523		TI	SN15857
	RCA	CA108	Teledyne S	LM311			Silicon G	SG7523	RC958	Motorola	MC858
	Signetics	LM108	TI	SN52111		† RC7524	Signetics	7524		TI	SN15858
	SG108	LM108	LM324	Teledyne S	LM324		Silicon G	SG7524	RC961	Motorola	MC861
	TI	SN52108	LM339	RCA	CA339	† RC7525	Signetics	7525		TI	SN15861
LM109	Silicon G	SG109	see page 661				Silicon G	SG7525	RC962	Motorola	MC862
LM111	AMD	LM111	RC10144	Fairchild	F10410	RC8T09	Signetics	8T09	RC963	Motorola	MC863
	Harris	HA-2111	Signetics	10144		RC8T10	Signetics	8T10		TI	SN15862
	Intersil	LM111	TI	SN10144		RC8T13	Signetics	8T13	RC993	Motorola	MC853
	National	LM111	RC1437	Motorola	MC1437	RC8T14	Signetics	8T14		TI	SN15863
	RCA	CA111	RC1458	Harris	HA-2655	RC8T23	Signetics	8T23	RC994	Motorola	MC853
	see page 661			PMI	SSS1458	RC8T24	Signetics	8T24		TI	SN158093
	Signetics	LM111		RCA	CA1458	RC8200	Signetics	N8200	RC997	Motorola	MC856
	Teledyne S	LM111		Signetics	MC1458	RC8201	Signetics	N8201		TI	SN158094
	TI	SN52111		Silicon G	SG1458	RC8202	Signetics	N8202	RC999	Motorola	MC852
LM124	Teledyne S	LM124		Teledyne S	1458	RC8203	Signetics	N8203		TI	SN158092
LM139	Teledyne S	LM139	RC1488	Exar	XR1488	RC8225	Intersil	IM5501	RM1514	TI	SN52514
LM201	AMD	LM201	Silicon G	SG1488			Signetics	N8225	RM1537	Motorola	MC1537
	Intersil	LM201	TI	SN75188		RC8230	Signetics	N8230	RM1556	Signetics	MC1556
	National	LM201	RC1489	Exar	XR1489A	RC8231	Signetics	N8231	RM1558	Harris	HA-2650
	RCA	CA201	Silicon G	SG1489		RC8233	Signetics	N8233		PMI	SSS1558
	see page 661			TI	SN75189	RC8234	Signetics	N8234		RCA	CA1558
LM204	Teledyne S	LM204	RC1556	Signetics	MC1456	RC8241	Signetics	N8241		Silicon G	SG1558
LM205	AMD	LM205	RC1558	RCA	CA1558	RC8242	Signetics	N8242	RM4531	Signetics	SE531
	Intersil	LM205	RC3403	see page 649		RC8243	Signetics	N8243	† RM4741	PMI	SSS4741
	National	LM205		Exar	XR3403	RC8250	Signetics	N8250		Silicon G	SG747
	Teledyne S	LM205		Fairchild	μA3403	RC8251	Signetics	N8251		Teledyne S	747
LM207	AMD	LM207		Motorola	MC3403	RC8252	Signetics	N8252	RM555	AMD	SE555
	Intersil	LM207	RC4136	see page 647		RC8260	Signetics	N8260		Intersil	SE555
	National	LM207		Exar	XR4136	RC8261	Signetics	N8261		Lithic Sys	LS555
	RCA	CA207		see page 640	XR4212	RC8263	Signetics	N8263		Signetics	SE555
	see page 661			see page 639	RC4136	RC8264	Signetics	N8264		Teledyne S	1558
	Teledyne S	LM207		TI	RC4136	RC8266	Signetics	N8266	RM4194	see page 655	SN52558
LM208	AMD	LM208	RC4194	see page 655	XR4194	RC8267	Signetics	N8267		Exar	XR4194
	Intersil	LM208		Exar	XR4194	RC8270	Signetics	N8270		TI	RM4136
	RCA	CA208	RC4531	Signetics	NE531	RC8271	Signetics	N8271	RM4531	Signetics	SE531
LM211	AMD	LM211	RC4558	see page 651		RC8273	Signetics	N8273		Signetics	SE531
	Harris	HA-2211		Exar	XR4558	RC8274	Signetics	N8274		Intersil	SE555
	Intersil	LM211		TI	RC4558	RC8280	Signetics	N8280		Lithic Sys	LS555
	National	LM211	RC5332	Fairchild	93411		TI	SN74176		Signetics	SE555
	RCA	CA211	RC5342	Fairchild	93411	RC8281	Signetics	N8281	RM702	TI	SN52702
	see page 661		RC555	Exar	XR555	RC8290	Signetics	N8290		Signetics	μA709
	Signetics	LM211		Intersil	NE555		TI	SN74196	RM709	Teledyne S	709
	Teledyne S	LM211		Lithic Sys	LS555	RC8291	Signetics	N8291		TI	SN52709
LM224	Teledyne S	LM224		RCA	CA555		TI	SN74176	RM710	Signetics	μA710
LM239	Teledyne S	LM239		see page 661		RC930	Motorola	MC830		Silicon G	SG710
LM2900	National	LM2900		Signetics	NE555		TI	SN15830		Teledyne S	710
LM2902	National	LM2902		Teledyne S	555	RC932	Motorola	MC832		TI	SN52710
LM301	AMD	LM301	RC556	Exar	XR-556		TI	SN15832	RM711	Signetics	μA711
	Intersil	LM301		Signetics	NE556	RC933	Motorola	MC933		Silicon G	SG711
	National	LM301		Teledyne S	556		TI	SN15833		Teledyne S	711
	Signetics	LM301	RC709	Signetics	μA709	RC934	Motorola	MC934	RM723	AMD	723
	Silicon G	SG301		Teledyne S	709		TI	SN15834		Intersil	723
	Teledyne S	LM301				RC935	Motorola	MC935		RCA	CA723
LM304	Teledyne S	LM304	RC710	Signetics	μA710		TI	SN15835		Signetics	μA723
LM305	AMD	LM305		Teledyne S	710	RC936	Motorola	MC836		Silicon G	SG723
	Intersil	LM305	RC711	Signetics	μA711		TI	SN15837		Teledyne S	723
	National	LM305		Teledyne S	711	RC937	Motorola	MC837	RM733	AMD	733
	Teledyne S	LM305					TI	SN15837		Signetics	μA733
LM307	AMD	LM307	RC723	Intersil	723	RC940	Motorola	MC840		Silicon G	SG733
	Intersil	LM307		Signetics	μA723		TI	SN15837			
	National	LM307	RC733	Signetics	μA733	RC941	Motorola	MC841			
	Teledyne S	LM307		Teledyne S	723		TI	SN15837			
	RCA	CA307	RC741	Intersil	741	RC944	Motorola	MC844			
	see page 661			PMI	SSS741						
	Signetics	LM307		RCA	CA741						
	Silicon G	SG307		see page 661							
	Teledyne S	LM307		Signetics	μA741						
				Teledyne S	741						

† Discontinued

The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

IC UPDATE MASTER

Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
Raytheon Semiconductor (cont)			54LS04	see page 282 Signetics S54LS04		54LS193	see page 282 Signetics S54LS193		54LS73	see page 282 Signetics S54LS73	
RM733	TI	SN52733					see page 384			see page 384	
RM741	AMD	741	54LS05	see page 282 Signetics S54LS05		54LS194A	see page 282 Signetics S54LS194A		54LS74	see page 282 Signetics S54LS74	
	Intersil	741		see page 384			see page 384			see page 384	
	PMI	SSS741	54LS08	see page 282 Signetics S54LS08		54LS195A	see page 282 Signetics S54LS195A		54LS76	see page 282 Signetics S54LS76	
	RCA	CA741		see page 384			see page 384			see page 384	
	see page 661		54LS09	see page 282 Signetics S54LS09		54LS196	see page 282 Signetics S54LS196		54LS78	see page 282 Signetics S54LS78	
	Signetics	μA741		see page 384			see page 384			see page 384	
	Silicon G	SG741	54LS10	see page 282 Signetics S54LS10		54LS197	see page 282 Signetics S54LS197		54LS83A	see page 282 Signetics S54LS83A	
	Teledyne S	741		see page 384			see page 384			see page 384	
	TI	SN52741	54LS109	see page 282 Signetics S54LS109		54LS20	see page 282 Signetics S54LS20		54LS86	see page 282 Signetics S54LS86	
RM747	AMD	747		see page 384			see page 384			see page 384	
	PMI	SSS747	54LS11	see page 282 Signetics S54LS11		54LS21	Signetics S54LS21		54LS95B	see page 282 Signetics S54LS95B	
	Signetics	μA747		see page 384			see page 384			see page 384	
	Teledyne S	747	54LS112	see page 282 Signetics S54LS112		54LS22	see page 282 Signetics S54LS22		54170	Fairchild TI	54170 54170
	TI	SN52747		see page 384			see page 384		RCA Solid State Division		
RM748	AMD	748	54LS113	see page 282 Signetics S54LS113		54LS251	see page 282 Signetics S54LS251		CA101	see page 661	
	Intersil	748		see page 384			see page 384		AMD	LM101	
	RCA	CA748	54LS114	see page 282 Signetics S54LS114		54LS253	see page 282 Signetics S54LS253		AD	AD101	
	Signetics	μA748		see page 384			see page 384		see page 625		
	Silicon G	SG748	54LS12	see page 282 Signetics S54LS12		54LS257	see page 282 Signetics S54LS257		Fairchild	μA101	
	Teledyne S	748		see page 384			see page 384		Intersil	LM101	
	TI	SN52748	54LS136	see page 282 Signetics S54LS136		54LS258	see page 282 Signetics S54LS258		Motorola	MLM101	
RM930	Motorola	MC930		see page 384			see page 384		National	LM101	
	TI	SN15930	54LS138	see page 282 Signetics S54LS138		54LS26	see page 282 Signetics S54LS26		NPC	SFC2121	
RM932	Motorola	MC932		see page 384			see page 384		Raytheon	LM101	
	TI	SN15932	54LS139	see page 282 Signetics S54LS139		54LS27	see page 282 Signetics S54LS27		Signetics	LM101	
RM933	Motorola	MC933		see page 384			see page 384		Silicon G	SG101	
	TI	SN15933	54LS15	see page 282 Signetics S54LS15		54LS28	see page 282 Signetics S54LS28		Siliconix	LM101	
RM934	Motorola	MC934		see page 384			see page 384		Teledyne S	LM101	
	TI	SN15934	54LS151	see page 282 Signetics S54LS151		54LS283	see page 282 Signetics S54LS283		TI	SN52101	
RM935	Motorola	MC935		see page 384			see page 384		CA107	see page 661	
	TI	SN15935	54LS157	see page 282 Signetics S54LS157		54LS295A	see page 282 Signetics S54LS295A		AMD	LM107	
RM936	Motorola	MC936		see page 384			see page 384		Intersil	LM107	
	TI	SN15936	54LS158	see page 282 Signetics S54LS158		54LS30	see page 282 Signetics S54LS30		Motorola	MLM107	
RM937	Motorola	MC937		see page 384			see page 384		National	LM107	
	TI	SN15937	54LS160	see page 282 Signetics S54LS160		54LS32	see page 282 Signetics S54LS32		Raytheon	LM107	
RM940	Motorola	MC940		see page 384			see page 384		Signetics	LM107	
RM941	Motorola	MC941	54LS162	see page 282 Signetics S54LS162		54LS33	see page 282 Signetics S54LS33		Silicon G	SG107	
	TI	SN15944		see page 384			see page 384		Teledyne S	LM107	
RM944	Motorola	MC944	54LS163	see page 282 Signetics S54LS163		54LS37	see page 282 Signetics S54LS37		TI	LM107	
	TI	SN15944		see page 384			see page 384		CA108	AMD	LM108
RM945	Motorola	MC945	54LS174	see page 282 Signetics S54LS174		54LS38	see page 282 Signetics S54LS38		Fairchild	μA108	
	TI	SN15945		see page 384			see page 384		National	LM108	
RM946	Motorola	MC946	54LS175	Signetics S54LS175		54LS386	see page 282 Signetics S54LS386		Raytheon	LM108	
	TI	SN15946		see page 384			see page 384		Signetics	LM108	
RM947	TI	SN15947	54LS181	see page 282 Signetics S54LS181		54LS40	see page 282 Signetics S54LS40		Silicon G	SG108	
RM948	Motorola	MC948		see page 384			see page 384		CA111	see page 661	
	TI	SN15948	54LS181	see page 282 Signetics S54LS181		54LS458	Harris HA-2655		AMD	LM111	
RM949	Motorola	MC949		see page 384			see page 384		Harris	HA2111	
	TI	SN15949	54LS190	see page 282 Signetics S54LS190		54LS54	see page 282 Signetics S54LS54		Intersil	LM111	
RM950	Motorola	MC950		see page 384			see page 384		Motorola	MLM111	
	TI	SN15950	54LS191	see page 282 Signetics S54LS191		54LS55	see page 282 Signetics S54LS55		National	LM111	
RM951	Motorola	MC951		see page 384			see page 384		NPC	SFC2111	
	TI	SN15951	54LS192	see page 282 Signetics S54LS192		54LS670	Signetics S54LS670		Raytheon	LM111	
RM957	Motorola	MC957		see page 384			see page 384		Signetics	LM111	
	TI	SN15957	54LS193	see page 282 Signetics S54LS193			see page 384		Silicon G	SG111	
RM958	Motorola	MC958		see page 384			see page 384		Teledyne S	LM111	
	TI	SN15958	54LS194	see page 282 Signetics S54LS194		CA1310	Signetics MC1310		TI	SN52111	
RM961	Motorola	MC961		see page 384		CA1458	Harris HA-2655				
	TI	SN15961	54LS195	see page 282 Signetics S54LS195			see page 384		National	LM1458	
RM962	Motorola	MC962		see page 384			see page 384		PMI	SSS1458	
	TI	SN15962	54LS196	see page 282 Signetics S54LS196			see page 384		Raytheon	RC1458	
RM963	Motorola	MC963		see page 384			see page 384		Signetics	MC1458	
	TI	SN15963	54LS197	see page 282 Signetics S54LS197			see page 384		Silicon G	SG1458	
RM993	Motorola	MC953		see page 384			see page 384		Teledyne S	1458	
	TI	SN159093	54LS198	see page 282 Signetics S54LS198			see page 384		TI	SN72558	
RM994	Motorola	MC956		see page 384			see page 384		CA1558	Fairchild μA1558	
	TI	SN159094	54LS199	see page 282 Signetics S54LS199			see page 384		Harris	HA-2650	
RM997	Motorola	MC955		see page 384			see page 384				
	TI	SN159097	54LS200	see page 282 Signetics S54LS200			see page 384				
RM999	Motorola	MC952		see page 384			see page 384				
	TI	SN159099	54LS201	see page 282 Signetics S54LS201			see page 384				

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ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device
RCA Solid State Division (cont)							
CA1558	National LM1558 PMI SSS1558 Raytheon RM1558 Signetics MC1558 Silicon G SG1558 Teledyne S 1558 TI SN52558	CA3036	Fairchild μ A3036 NPC SFC2036	CA311	Harris HA-2311 Intersil LM311 Motorola MLM311 National LM311 NPC SFC3111 Raytheon LM311 Signetics LM311 Silicon G SG311 Teledyne S LM311 TI SN72311	CA747	National LM747 PMI SSS747 Raytheon HC747 Raytheon RM741 Raytheon RM747 Signetics UA747 Silicon G SG747 Teledyne S 747
CA201	see page 661 AMD LM201 AD AD201 see page 625 Fairchild μ A201 Intersil LM201 Motorola MLM201 National LM201 Raytheon LM201 Signetics LM201 Silicon G SG201 Siliconix LM201 Teledyne S LM201	CA3038	Motorola MC1709	CA3120	Sprague ULN-2125	CA748	AMD 748 Fairchild μ A748 Intersil 748 Motorola MC1748 National LM748 Raytheon RC748 Raytheon RM748 Signetics UA748 Silicon G SG748 Teledyne S 748 TI SN52748
CA207	see page 661 AMD LM207 Fairchild LM207 Intersil LM207 Motorola MLM207 National LM207 Raytheon LM207 Signetics LM207 Teledyne S LM207	CA3039	Fairchild μ A3039	CA3121	Sprague ULN-2269		
CA208	AMD LM208 AD AD208 see page 625 Fairchild LM208 Intersil LM208 National LM208 NPC SFC2208 Raytheon LM208 Signetics LM208 Silicon G SG208	CA3045	Fairchild μ A3045 Lithic Sys LA3045 National LM3045 Plessey SL3045 Silicon G SG3821 Sprague ULS2045	CA3123	Sprague ULN-2137		
CA211	see page 661 AMD LM211 Harris HA-2211 Intersil LM211 Motorola MLM211 National LM211 NPC SFC2211 Raytheon LM211 Signetics LM211 Teledyne S LM211	CA3049	Lithic Sys LA3049 Silicon G SG3822	CA324	see page 661 National LM324 Signetics LM324 Silicon G SG324 Teledyne S LM324		
CA2111	Sprague ULN-2111	CA3053	Lithic Sys LS3053	CA339	see page 661 National LM339 Raytheon LM339 Signetics LM339 Silicon G SG339 Teledyne S LM339	CD4000	see page 375 Harris HD4000 Motorola MC14000 SSS SCL4000 Solitron CM4000 TI TF4000 TI TP4000
CA239	see page 661 Teledyne S LM239	CA3054	Fairchild μ A3054 National LM3054 NPC SFC2054	CA3458	RCA CA1458	CD4001	see page 375 Fairchild F4001 Fairchild 34001 GI MEM4001 Harris HD4001 Motorola MC14001 National CD4001 SGS HBF4001 SSS SCL4001 Solitron CM4001 SW SW4001 TI TF4001 TI TP4001 Toshiba TC4001
CA301	see page 661 AD AD301 see page 625 AD LM301 Fairchild μ A301 Intersil LM301 Motorola MLM301 National LM301 NPC SFC2301 Raytheon LM301 Signetics LM301 Teledyne S LM301 TI SN72301	CA3055	Silicon G SG300	CA3741	RCA CA741 see page 661		
CA3011	Motorola MC1590	CA3064	Fairchild μ A3064 Motorola MC1364 Sprague ULN-2264	CA3747	RCA CA747 see page 661		
CA3012	Motorola MC1590	CA3065	Fairchild μ A3065 Motorola MC1358 Sprague ULN-2165	CA3748	RCA CA748		
CA3013	Motorola MC1355	CA3066	Fairchild μ A3066	CA555	see page 661 AMD NE555 AMD SE555 Exar XR555 Intersil NE555 Lithic Sys LS555 Motorola MC1455 Motorola MC1555 National LM555 Raytheon RC555 Raytheon RM555 Signetics NE555 Teledyne S 555 TI SN72555	CD4002	see page 375 Fairchild F4002 Fairchild 34002 Harris HD4002 Motorola MC14002 National CD4002 SGS HBF4002 SSS SCL4002 Solitron CM4002 SW SW4002 TI TF4002 TI TP4002 Toshiba TC4002
CA3014	Motorola MC1357	CA3067	Fairchild μ A3067 Sprague ULN-2267	CA723	AMD 723 Fairchild μ A723 Intersil 723 ITT ITT723 Motorola MC1723 National LM723 NPC SFC2723 Raytheon RC723 Signetics UA723 Silicon G SG723 Teledyne S 723 TI SN52723	CD4006	see page 375 Fairchild F4006 Harris HD4006 Motorola MC14006 National CD4006 SSS SCL4006 Solitron CM4006
CA3018	Fairchild μ A3018 Lithic Sys LA3018 NPC SFC2018 Silicon G SG3818	CA3070	Fairchild μ A780 Motorola MC1370 Sprague ULN-2124	CA741	see page 661 AMD SSS741 AMD 741 AD AD741 see page 625 Fairchild μ A741 Intersil LM741 Intersil SSS741 Intersil 741 Motorola MC1741 National LM741 NPC SFC2741 PMI SSS741 Raytheon RC741 Raytheon RM741 Signetics UA741 Silicon G SG741 Teledyne S 741 TI SN52741	CD4007	see page 375 Fairchild F4007 GI MEM4007 Harris HD4007 Motorola MC14007 National CD4007 SGS HBF4007 SSS SCL4007 Solitron CM4007 TI TF4007 TI TP4007 Toshiba TC4007
CA3018A	Lithic Sys LA3018A	CA3071	Fairchild μ A781 Motorola MC1371 Sprague ULN-2127	CA747	see page 661 AMD SSS747 AMD 747 Fairchild μ A747 Intersil SSS747 Motorola MC1747	CD4008	see page 375 Fairchild F4008 Harris HD4008 Motorola MC14008 National CD4008 SGS HBF4008 SSS SCL4008 Solitron CM4008 TI TF4008
CA3019	Fairchild μ A3019	CA3072	Fairchild 746 Motorola MC1328 Sprague ULN-2114	CA748	AMD SSS748 AMD 748 Fairchild μ A748 Intersil SSS748 Motorola MC1748		
CA3026	Fairchild μ A3026 Lithic Sys LA3026 Silicon G SG3822	CA3075	Fairchild μ A3075 Motorola MC1375 Sprague ULN-2129				
CA3028	Lithic Sys LS3028	CA3076	Fairchild μ A3076				
CA3031	Motorola MC1712	CA308	AMD LM308 AD AD308 see page 625 Fairchild LM308 Intersil LM308 Motorola MLM308 National LM308 NPC SFC2308 Raytheon LM308 Signetics LM308 Silicon G SG308 Teledyne S LM308 TI SN72308				
CA3032	Motorola MC1712	CA3081	Silicon G SG3081				
		CA3082	Silicon G SG3082				
		CA3086	Fairchild μ A3086 Lithic Sys LA3086 National LM3086 Plessey SL3086 Silicon G SG3086				
		CA3089	SGS TDA1200 Sprague ULN-2289				
		CA311	see page 661 AMD LM311 Fairchild μ A311				

1 Discontinued

The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device			Replacement Source Device			Manufacturer Device			Replacement Source Device			Manufacturer Device			Replacement Source Device																																																																									
RCA Solid State Division (cont)																																																																																								
CD4008	TI	TP4008 Toshiba TC4008	CD4016	see page 375 AD AD7516 see page 546 Motorola MC14016 National CD4016 SSS SCL4016 Solitron CM4016	CD4023	see page 375 Fairchild F4023 Harris HD4023 Motorola MC14023 National CD4023 SGS HBF4023 SSS SCL4023 Solitron CM4023 SW SW4023 TI TF4023 TI TP4023 Toshiba TC4023	CD4030	Motorola MC14030 National CD4030 SGS HBF4030 SSS SCL4030 Solitron CM4030 SW SW4030 TI TF4030 TI TP4030 Toshiba TC4030	CD4009	see page 375 Motorola MC14009 National CD4009 SGS HBF4009 SSS SCL4009 Solitron CM4009 TI TF4009 TI TP4009 Toshiba TC4009	CD4017	see page 375 Fairchild F4017 Harris HD4017 Motorola MC14017 National CD4017 SGS HBF4017 SSS SCL4017 Solitron CM4017 SW SW4017 TI TF4017 TI TP4017 Toshiba TC4017	CD4031	see page 375 Fairchild F4031 National CD4031	CD4010	see page 375 Motorola MC14010 National CD4010 SGS HBF4010 SSS SCL4010 Solitron CM4010 TI TF4010 TI TP4010 Toshiba TC4010	CD4018	see page 375 Fairchild F4018 Harris HD4018 see page 266 National CD4018 SGS HBF4018 SSS SCL4018 Solitron CM4018 TI TF4018 TI TP4018 Toshiba TC4018	CD4024	see page 375 Fairchild F4024 Harris HD4024 Motorola MC14024 National CD4024 SGS HBF4024 SSS SCL4024 Solitron CM4024 SW SW4024 TI TF4024 TI TP4024 Toshiba TC4024	CD4032	see page 375 Motorola MC14032 Solitron CM4032 Toshiba TC4032	CD4011	see page 375 Fairchild F4011 GI MEM4011 Harris HD4011 Motorola MC14011 National CD4011 SGS HBF4011 SSS SCL4011 Solitron CM4011 SW SW4011 TI TF4011 TI TP4011 Toshiba TC4011	CD4019	see page 375 Fairchild F4019 Harris HD4019 see page 266 Motorola MC14519 National CD4019 SGS HBF4019 SSS SCL4019 Solitron CM4019 SW SW4019 TI TF4019 TI TP4019 Toshiba TC4019	CD4025	see page 375 Fairchild F4025 Harris HD4025 Motorola MC14025 National CD4025 SGS HBF4025 SSS SCL4025 Solitron CM4025 SW SW4025 TI TF4025 TI TP4025 Toshiba TC4025	CD4033	see page 375 SGS HBF4033 SSS SCL4033 Solitron CM4033	CD4012	see page 375 Harris HD4012 Motorola MC14012 National CD4012 National MM4612 SGS HBF4012 SSS SCL4012 Solitron CM4012 SW SW4012 TI TF4012 TI TP4012 Toshiba TC4012	CD4026	see page 375 SSS SCL4026 Solitron CM4026	CD4034	see page 375 Fairchild F4034 Motorola MC14034 SSS SCL4034 Solitron CM4034 Toshiba TC4034	CD4013	see page 375 Fairchild F4013 GI MEM4013 Harris HD4013 Motorola MC14013 SGS HBF4013 SSS SCL4013 Solitron CM4013 SW SW4013 TI TF4013 TI TP4013 Toshiba TC4013	CD4027	see page 375 Fairchild F4027 Harris HD4027 Motorola MC14027 National CD4027 SGS HBF4027 SSS SCL4027 Solitron CM4027 SW SW4027 TI TF4027 TI TP4027 Toshiba TC4027	CD4035	see page 375 Fairchild F4035 Harris HD4035 see page 266 Motorola MC14035 National CD4035 SGS HBF4035 SSS SCL4035 Solitron CM4035 TI TF4035 TI TP4035 Toshiba TC4035	CD4014	see page 375 Fairchild F4014 Harris HD4014 see page 266 Motorola MC14014 National CD4014 SGS HBF4014 SSS SCL4014 Solitron CM4014 TI TF4014 TI TP4014 Toshiba TC4014	CD4028	see page 375 Fairchild F4028 Harris HD4028 see page 266 Motorola MC14028 National CD4028 SGS HBF4028 SSS SCL4028 Solitron CM4028 SW SW4028 TI TF4028 TI TP4028 Toshiba TC4028	CD4036	see page 375 Solitron CM4036	CD4015	see page 375 Fairchild F4015 Harris HD4015 see page 266 Motorola MC14015 National CD4015 SGS HBF4015 SSS SCL4015 Solitron CM4015 SW SW4015 TI TF4015 TI TP4015	CD4029	see page 375 Fairchild F4029 Harris HD4029 see page 266 Motorola MC14029 National CD4029 SGS HBF4029 SSS SCL4029 Solitron CM4029 SW SW4029 TI TF4029 TI TP4029 Toshiba TC4029	CD4037	see page 375 Fairchild F4037 Solitron CM4037	CD4016	see page 375 Fairchild F4016 Harris HD4016 see page 266 Motorola MC14016 National CD4016 SSS SCL4016 Solitron CM4016 TI TF4016 TI TP4016 Toshiba TC4016	CD4020	see page 375 Fairchild F4020 Harris HD4020 see page 266 Motorola MC14020 National CD4020 SGS HBF4020 SSS SCL4020 Solitron CM4020 SW SW4020 TI TF4020 TI TP4020 Toshiba TC4020	CD4038	see page 375 Motorola MC14038 Solitron CM4038 Toshiba TC4038	CD4017	see page 375 Fairchild F4017 Harris HD4017 Motorola MC14017 National CD4017 SGS HBF4017 SSS SCL4017 Solitron CM4017 SW SW4017 TI TF4017 TI TP4017 Toshiba TC4017	CD4021	see page 375 Fairchild F4021 Harris HD4021 see page 266 Motorola MC14021 National CD4021 SSS SCL4021 Solitron CM4021 SW SW4021 TI TF4021 TI TP4021 Toshiba TC4021	CD4039	see page 375 Solitron CM4039	CD4018	see page 375 Fairchild F4018 Harris HD4018 see page 266 Motorola MC14018 National CD4018 SGS HBF4018 SSS SCL4018 Solitron CM4018 SW SW4018 TI TF4018 TI TP4018 Toshiba TC4018	CD4022	see page 375 Fairchild F4022 Harris HD4022 see page 266 Motorola MC14022 National CD4022 SGS HBF4022 SSS SCL4022 Solitron CM4022 TI TF4022 TI TP4022 Toshiba TC4022	CD4040	see page 375 Fairchild F4040 Harris HD4040 Motorola MC14040 National CD4040 SSS SCL4040 Solitron CM4040 TI TF4040 TI TP4040 Toshiba TC4040	CD4019	see page 375 Fairchild F4019 Harris HD4019 see page 266 Motorola MC14019 National CD4019 SSS SCL4019 Solitron CM4019 SW SW4019 TI TF4019 TI TP4019 Toshiba TC4019	CD4024	see page 375 Fairchild F4024 Harris HD4024 Motorola MC14024 National CD4024 SGS HBF4024 SSS SCL4024 Solitron CM4024 SW SW4024 TI TF4024 TI TP4024 Toshiba TC4024	CD4041	see page 375 Fairchild F4041 SSS SCL4041 Solitron CM4041	CD4010	see page 375 Fairchild F4010 Harris HD4010 see page 266 Motorola MC14010 National CD4010 SGS HBF4010 SSS SCL4010 Solitron CM4010 TI TF4010 TI TP4010 Toshiba TC4010	CD4025	see page 375 Fairchild F4025 Harris HD4025 Motorola MC14025 National CD4025 SGS HBF4025 SSS SCL4025 Solitron CM4025 SW SW4025 TI TF4025 TI TP4025 Toshiba TC4025	CD4042	see page 375 Fairchild F4042 Harris HD4042 Motorola MC14042 National CD4042 SGS HBF4042 SSS SCL4042 Solitron CM4042 TI TF4042 TI TP4042 Toshiba TC4042	CD4020	see page 375 Fairchild F4020 Harris HD4020 see page 266 Motorola MC14020 National CD4020 SGS HBF4020 SSS SCL4020 Solitron CM4020 SW SW4020 TI TF4020 TI TP4020 Toshiba TC4020	CD4043	see page 375 Fairchild F4043 Harris HD4043 Motorola MC14043 National CD4043 SSS SCL4043 Solitron CM4043 TI TF4043

ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device		
RCA Solid State Division (cont)									
CD4043	TI TP4043 Toshiba TC4043	CD4066	see page 375 Fairchild F4066 Harris HD4066 National CD4066 SGS HBF4066 SSS SCL4066 Solitron CM4066 Teledyne S CD4066	CD4508	Solitron CM4508 Toshiba TC4508	HBF4010	SSS SCL4010		
CD4044	see page 375 Fairchild F4044 Harris HD4044 Motorola MC14044 National CD4044 SSS SCL4044 Solitron CM4044 TI TF4044 TI TP4044 Toshiba TC4044	CD4067	see page 375 Fairchild F4067	CD4510	see page 375 National MM14510	HBF4011	RCA CD4011 see page 375 SSS SCL4011		
CD4045	see page 375 SGS HBF4045 SSS SCL4445 Solitron CM4045	CD4068	see page 375 Fairchild F4068 Motorola MC14068 Toshiba TC4068	CD4511	see page 375 Fairchild F4511 Motorola MC14511 National MM14511 SSS SCL4511 Solitron CM4511	HBF4012	RCA CD4012 see page 375 SSS SCL4012		
CD4046	see page 375 Fairchild F4046 Motorola MC14046 Solitron CM4046	CD4069	see page 375 Fairchild F4069 Harris MM54C04 Harris MM74C04 Motorola MC14069 National CD4069 National MM54C04 National MM74C04 Teledyne S MM54C04 Teledyne S MM74C04 Toshiba TC4069	CD4514	see page 375 Fairchild F4514 Motorola MC14514 SSS SCL4514 Solitron CM4514 Toshiba TC4514	HBF4016	RCA CD4016 see page 375 SSS SCL4016		
CD4047	see page 375 Fairchild F4047 Solitron CM4047 Toshiba TC4047	CD4070	see page 375 Fairchild F4070 National CD4070 National MM74C86 Solitron CM4030	CD4515	see page 375 Fairchild F4515 Motorola MC14515 Solitron CM4515 Toshiba TC4515	HBF4020	RCA CD4020 see page 375 SSS SCL4020		
CD4048	see page 375 National CD4048 Solitron CM4048	CD4071	see page 375 Fairchild F4071 Motorola MC14071 SSS SCL4071 TI TF4071 TI TP4071 Toshiba TC4071	CD4516	see page 375 Fairchild F4516 Harris HD4516 Motorola MC14516 National CD4516	HBF4022	SSS SCL4022		
CD4049	see page 375 Fairchild F4049 GI MEM4049 Harris HD4049 Motorola MC14049 National CD4049 SGS HBF4049 SSS SCL4049 Solitron CM4049 SW SW4049 Teledyne S CD4049 TI TF4049 TI TP4049 Toshiba TC4049	CD4072	see page 375 Fairchild F4072 Toshiba TC4072	CD4518	see page 375 Fairchild F4518 Harris HD4518 Motorola MC14518 National CD4518 SSS SCL4518 TI TF4518 TI TP4518 Toshiba TC4518	HBF4023	RCA CD4023 see page 375 SSS SCL4023		
CD4050	see page 375 Fairchild F4050 GI MEM4050 Harris HD4050 Motorola MC14050 National CD4050 SGS HBF4050 SSS SCL4050 Solitron CM4050 SW SW4050 Teledyne S CD4050 TI TF4050 TI TP4050 Toshiba TC4050	CD4073	see page 375 Fairchild F4073 Motorola MC14073 Toshiba TC4073	CD4520	see page 375 Fairchild F4520 Harris HD4520 Motorola MC14520 National CD4520 SSS SCL4520 TI TF4520 TI TP4520 Toshiba TC4520	HBF4024	RCA CD4024 see page 375 SSS SCL4024		
CD4051	see page 375 Fairchild F4051 National CD4051 SSS SCL4051 Solitron CM4051 TI TF4051 TI TP4051	CD4075	see page 375 Fairchild F4075 Motorola MC14075 Toshiba TC4075	CD4527	see page 375 Motorola MC14527	HBF4025	RCA CD4025 see page 375 SSS SCL4025		
CD4052	see page 375 Fairchild F4052 National CD4052 SSS SCL4052 Solitron CM4052 TI TF4052 TI TP4052	CD4076	see page 375 Fairchild F4076 Harris MM54C173 Harris MM74C173 Motorola MC14076 National CD4076 National MM54C173 National MM74C173 Teledyne S MM54C173 Teledyne S MM74C173	CD4532	see page 375 Fairchild F4532 Motorola MC14532 Toshiba TC4532	HBF4027	RCA CD4027 see page 375 SSS SCL4027		
CD4053	see page 375 Fairchild F4053 GI MEM4053 National CD4053 SSS SCL4053 Solitron CM4053 TI TF4053 TI TP4053	CD4077	see page 375 Fairchild F4077 Solitron CM4077	CD4552	see page 375 Fairchild F4552 Motorola MC14552	HBF4029	RCA CD4029 see page 375 SSS SCL4029		
CD4060	see page 375 SSS SCL4060	CD4078	see page 375 Fairchild F4078 Motorola MC14078 Toshiba TC4078	CD4555	see page 375 Fairchild F4555 Motorola MC14555	HBF4035	RCA CD4035 see page 375 SSS SCL4035		
CD4061	see page 375 Toshiba TC4061	CD4081	see page 375 Fairchild F4081 Motorola MC14081 SSS SCL4081 TI TF4081 TI TP4081 Toshiba TC4081	CD4556	see page 375 Fairchild F4556 Motorola MC14556	HBF4040	RCA CD4040 see page 375 SSS SCL4040		
		CD4082	see page 375 Fairchild F4082 Toshiba TC4082	Rockwell Microelectronic Div.					
		CD4085	see page 375 Fairchild F4085	1103	AMI S1103A see page 712	μA709	Fairchild μA709 Fairchild 709 Motorola MC1709 National LM709 Raytheon RM709 Teledyne S 709 TI SN52709		
		CD4086	see page 375 Fairchild F4086	1604	AMI 4096 EA EA4096 Mostek 4096	μA710	Fairchild μA710 Motorola MC1710 National LM710 Raytheon RM710 Silicon G SG710 Teledyne S 710 TI SN52710		
		CD4508	see page 375 Motorola MC14508	SGS-ATES Semiconductor				μA711	Fairchild μA711 Motorola MC1711 National LM711 Raytheon RM711 Silicon G SG711 Teledyne S 711 TI SN52711
				HBF4001	RCA CD4001 see page 375 SSS SCL4001	μA723	Fairchild μA723 Intersil 723 Motorola MC1723 National LM723 Raytheon RM723 RCA CA723 Silicon G SG723 Teledyne S 723 TI SN52723		
				HBF4002	RCA CD4002 see page 375 SSS SCL4002	μA733	AMD 733 National LM733 Raytheon RM733 Silicon G SG733 TI SN52733		
				HBF4008	RCA CD4002 see page 375 SSS SCL4008	μA740	Fairchild μA740 Intersil 740 National LH740		
				HBF4009	RCA CD4009 see page 375 SSS SCL4009	μA741	AMD 741 AD AD741 see page 625 Fairchild μA741		
				HBF4010	RCA CD4010 see page 375				

† Discontinued

The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device			Replacement Source Device			Manufacturer Device			Replacement Source Device			Manufacturer Device			Replacement Source Device																																																																																																																																																																																
Signetics (cont)																																																																																																																																																																																															
μA741	Intersil Motorola National PMI Raytheon RCA	741 MC1741 LM741 SSS741 RM741 CA741	LM301	Raytheon RCA	LM301 CA301	N5558	Fairchild Motorola National Raytheon RCA Silicon G Teledyne S	MC1458 MC1458 LM1458 RC1458 CA1458 SG1458 1458	N74151	Raytheon	74151	LM307	AMD Fairchild Intersil National Raytheon RCA	LM307 μA307 LM307 LM307 LM307 CA307	N5595	Motorola	MC1495	N74152	Raytheon	74152	N74153	Raytheon	74153	N74154	Raytheon	74154	N74155	Raytheon	74155	N74156	Raytheon	74156	N74157	Raytheon	74157	N74158	Raytheon	74158	N74159	Raytheon	74159	N74160	Raytheon	74160	N74161	Raytheon	74161	N74162	Raytheon	74162	N74163	Raytheon	74163	N74164	Raytheon	74164	N74165	Raytheon	74165	N74166	Raytheon	74166	N74170	Raytheon	74170	N74174	Raytheon	74174	N74175	Raytheon	74175	N74181	Raytheon	74181	N74182	Raytheon	74182	N74190	Raytheon	74190	N74191	Raytheon	74191	N74192	Raytheon	74192	N74193	Raytheon	74193	N74194	Raytheon	74194	N74195	Raytheon	74195	N74198	Raytheon	74198	N74199	Raytheon	74199	N7420	Hitachi	HD2504 SN7420	N7421	Raytheon	7421	N7422	Raytheon	7422	N74283	Raytheon	74283	N7430	Hitachi	HD2508 TI SN7430	N7440	Hitachi	HD2501 TI SN7440	N7441	Hitachi	HD2518 SN74141	N7442	Raytheon	7442	N7443	Raytheon	7443	N7444	Raytheon	7444	N7445	Raytheon	7445	N7451	Hitachi	HD2505 TI SN7451	N7453	Hitachi	HD2512 TI SN7453	N7454	Hitachi	HD2514 TI SN7454	N7460	Hitachi	HD2502 TI SN7460	N7470	Hitachi	HD2539 TI SN7470	N7472	Hitachi	HD2529 TI SN7472	N7473	Hitachi	HD2515 SN7473	N7474	Hitachi	HD2510 Raytheon TI SN7474	N7475	Hitachi	HD2517 TI SN7475	N7476	Hitachi	HD2516 TI SN7476	N7481	Raytheon	7481	N7483	Raytheon	7483	N7486	Raytheon	7486	N7488	Intersil	IM5600 TI SN7488A	N7489	Hitachi	HD2502 Intersil Raytheon TI SN7489	N7490	Hitachi	HD2519 TI SN7490A	N7491	Hitachi	HD2524 TI SN7491A	N7492	Hitachi	HD2521 TI SN7492A	N7493	Hitachi	HD2520
μA747	AMD Fairchild Motorola National PMI Raytheon RCA	747 μA747 MC1747 LM747 SSS747 RM747 CA747	LM308	AMD Fairchild National Raytheon RCA Silicon G Teledyne S	LM308 μA308 LM308 LM308 CA308 SG308 LM308	N74H00	Fairchild Fairchild Raytheon TI	74H00 9H00 74H00 SN74H00	N74H01	Raytheon TI	74H01 SN74H01	N74H04	Raytheon TI	74H04 SN74H04	N74H05	Raytheon TI	74H05 SN74H05	N74H10	Raytheon TI	74H10 SN74H10	N74H11	Raytheon TI	74H11 SN74H11	N74H20	Raytheon TI	74H20 SN74H20	N74H22	Raytheon TI	74H22 SN74H22	N74H40	Raytheon TI	74H40 SN74H40	N74H74	Raytheon	74H74	N74LS138	see page 304 Raytheon	74LS138	N74LS139	see page 304 Raytheon	74LS139	N74LS253	see page 304 Raytheon	74LS253	N74S00	Fairchild Fairchild TI	74S00 9S00 SN74S00	N74S200	National	DM74S200	N74S201	see page 804, 806, 815, MMI	6531 SN74S201	N7400	Fairchild Fairchild Hitachi Raytheon TI	7400 9N00 HD2503 7400 SN7400	N7401	Hitachi- Raytheon TI	HD2509 7401 SN7401	N7402	Hitachi TI	HD2511 SN7402	N7403	Hitachi Raytheon TI	HD2528 7403 SN7403	N7404	Hitachi Raytheon TI	HD2522 7404 SN7404	N7405	Hitachi Raytheon TI	HD2523 7405 SN7405	N7408	Hitachi Raytheon TI	HD2550 7408 SN7408	N7409	Raytheon	7409	N7410	Hitachi Raytheon TI	HD2507 7410 SN7410	N74107	Hitachi TI	HD2530 SN74107	N7411	Raytheon	7411	N7412	Raytheon	7412	N74123	Raytheon	74123	N74136	Raytheon	74136	N74145	Raytheon	74145	N7415	Raytheon	7415	N74150	Raytheon	74150																																																																																							
μA748	AMD Fairchild Intersil Motorola National Raytheon RCA Silicon G Teledyne S TI	748 μA748 748 MC1748 LM748 RM748 CA748 SG748 748 SN52748	LM309	Fairchild Raytheon TI	μA309 LM309 SN72309	LM311	AMD Harris Raytheon Teledyne S TI	LM311 HA-2311 LM311 LM311 SN72311	LM324	Teledyne S	LM324	NE529	National	LM361	NE536	Intersil	NE536	NE555	AMD Exar Intersil Lithic Sys Raytheon RCA	NE555 XR555C NE555 LS555 RC555 CA555	NE556	AMD Exar Raytheon Teledyne S	NE556 XR556 RC556 556	NE567	Exar	XR567	† N1004	Motorola	MC1004	† N1005	Motorola	MC1005	† N1006	Motorola	MC1006	† N1010	Motorola	MC1010	† N1011	Motorola	MC1011	† N1012	Motorola	MC1012	† N1013	Motorola	MC1013	† N1014	Motorola	MC1014	† N1015	Motorola	MC1015	† N1016	Motorola	MC1016	† N1017	Motorola	MC1017	† N1024	Motorola	MC1024	† N1025	Motorola	MC1025	† N1027	Motorola	MC1027	† N1033	Motorola	MC1033	† N1039	Motorola	MC1039	† N2010	Motorola	MC1160/236	N2430	Nitron	NCM1110	N2461	Nitron	NCM1111	N3002	see page 1006 Intel	3002	N5065	Sprague	ULN-2165	N5070	Motorola Sprague	MC1370 ULN-2124	N5071	Motorola Sprague	MC1371 ULN-2127	N5072	Motorola Sprague	MC1328 ULN-2114	N5111	Motorola Sprague	MC1358 ULN-2111	N5556	Motorola Raytheon Silicon G	MC1456 RC1556 SG1456																																																																																							
DM8880	National	DS8880	LM101	AMD Fairchild Intersil Raytheon RCA	LM101 μA101 LM101 LM101 CA101	LM107	AMD Fairchild Intersil Raytheon RCA	LM107 μA107 LM107 LM107 CA107	LM108	AMD Fairchild Raytheon RCA Silicon G	LM108 μA108 LM108 CA108 SG108	LM109	Fairchild TI	μA109 SN52109	LM124	Teledyne S	LM124	LM201	AMD Fairchild Intersil Raytheon RCA	LM201 μA201 LM201 LM201 CA201	LM207	AMD Fairchild Intersil Raytheon RCA	LM207 μA207 LM207 LM207 CA207	LM209	Fairchild Raytheon	LM209 LM209	LM211	Teledyne S	LM211	LM224	Teledyne S	LM224	LM301	AMD Fairchild Intersil National	LM301 μA301 LM301 LM301																																																																																																																																																												

Discontinued

Bold face device number indicates additional data is provided in Catalog section

ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device
Signetics (cont)				N82S29	MMI 6301	N8280	Motorola MC7280
N7493	TI SN7493A	N82S110	TI SN74S309	National DM8574	National DM8280	National RC8280	National RC8280
N7494	Hitachi HD2533 TI SN7494	N82S111	TI SN74S209	TI SN54S287	TI SN74S287	TI SN74176	
N7495	Hitachi HD2534 TI SN7495A	N82S116	see page 804, 806, 815, MMI 6531 TI SN74S201	N8200	Raytheon RC8200	N8281	Motorola MC7281
N7496	Hitachi HD2546 TI SN7496			N8201	Raytheon RC8201	National DM8281	National RC8281
N7520	ITT ITT7520 Motorola MC7520 National DS7520 Silicon G SG7520	N82S123	see page 804, 826, 828, Harris HM7603 see page 746 Intersil IM5610 MMI 6331 National DM8598 TI SN74S288 TI 54S288	N8202	Raytheon RC8202	TI SN54177	
N7521	ITT ITT7521 Motorola MC7521 National DS7521 Silicon G SG7521			N8206	TI SN74S201	N8284	Motorola MC7284
N7522	ITT ITT7522 Motorola MC7522 National DS7522 Silicon G SG7522	N82S124	Intersil IM5610 TI SN74S387	N8207	TI SN74S301	Raytheon RC8284	
N7523	ITT ITT7523 Motorola MC7523 National DS7523 Silicon G SG7523	N82S126	see page 804, 826, 835, Harris HPROM-1024A Intel 3601 see page 772, 773 MMI 5300 MMI 6300 National DM7573 National DM8573 TI SN54S387 TI SN74S387	N8223	Harris HPROM-8256 Intersil IM5600 MMI 6330 National DM8577 TI SN74S188	N8285	Motorola MC7285
N7524	ITT ITT7524 Motorola MC7524 National DS7524 Silicon G SG7524			N8224	Fairchild 93434 Intersil IM5600 ITT ITT7488A National DM7488 TI SN7488	N8288	Motorola MC7288
N7525	ITT ITT7525 Motorola MC7525 National DS7525 Silicon G SG7525	N82S129	Harris HPROM-1024 Intel 3621-1 see page 772, 773 Intersil IM5603 MMI 5301 MMI 6301 National DM7574 National DM8574 TI SN54S287 TI SN74S287	N8225	AMD 3101 Intersil IM5501 MMI 6560 Motorola MCM4064 Raytheon RC8225 TI SN74S289	N8290	National DM8290
N7550	Hitachi HD2506			N8230	Hitachi HD2549 ITT ITT9312 Motorola MC7230 Raytheon RC8230 TI SN29312	Raytheon RC8290	National DM8290
N8H70	ITT ITT74H11 TI SN74H11	N82S130	see page 804, 826, 838, Fairchild 93436	N8231	Motorola MC7230 Raytheon RC8231 TI SN74S289	Raytheon RC8291	National DM8291
N8H80	ITT ITT74H00 TI SN74H00	N82S131	see page 804, 826, 838, Fairchild 93446	N8232	Motorola MC7230 Raytheon RC8232 TI SN74S289	TI SN74196	National DM8291
N8H90	ITT ITT74H04 TI SN74H04	N82S16	see page 804, 806, 815, Fairchild 93421 Intersil IM5523 MMI 6531 TI SN54S201 TI SN74S201	N8233	Motorola MC8233 Raytheon RC8233 TI SN7488	TI SN74197	TI SN74197
N8T09	Raytheon RC8T09			N8234	Motorola MC8234 Raytheon RC8234 TI SN7488	N8292	TI SN74LS196
N8T10	National DM8551 Raytheon RC8T10 TI SN74173	N82S17	see page 804, 806, 815, Fairchild 93411 Intersil IM5533 MMI 6530 TI SN54S301 TI SN74S301	N8241	Hitachi HD2526 Motorola MC7241/42 Raytheon RC8241	N8293	TI SN74LS197
N8T13	Fairchild 8T13 National DS75121 Raytheon RC8T13			N8242	Motorola MC7241/42 Raytheon RC8242 TI SN74LS266	N8455	Motorola MC7440
N8T14	Fairchild 8T14 National DS75122 Raytheon RC8T14	N82S226	Fairchild 93416 Intersil IM5603 MMI 6300 National DM8573 TI SN54187 TI SN74187	N8250	Motorola MC7250/51 Raytheon RC8250	TI SN7440	ITT ITT7410
N8T22	ITT ITT74122 Raytheon RC8T22 Raytheon RF8601 TI SN74122			N82506	Raytheon RC5340	N8470	ITT ITT7410
N8T23	Fairchild 8T23 National DS75123 Raytheon RC8T23 TI SN75123	N82S230	TI SN54S270 TI SN74S270	N82507	Raytheon RC5330	Motorola MC7440	ITT ITT7410
N8T24	Fairchild 8T24 National DS75124 Raytheon RC8T24 TI SN75124			N8251	Hitachi HD2536 Motorola MC7250/51 Raytheon RC8251	TI SN7400	ITT ITT7403
N8T25	National DS3625	N82S231	TI SN54S370 TI SN74S370	N82516	Raytheon RC5340	N8480	ITT ITT400
N8T380	National DS8836			N82517	Raytheon RC5330	TI SN7400	ITT ITT403
N8T74	Fairchild 9374 National DS8674	N82S232	see page 804, 826, 828, AMD AM27S09 Harris HM7602 see page 746 MMI 6330 TI SN54S188 TI SN74S188	N8252	Motorola MC7250/51 Raytheon RC8252 TI SN29301	N8481	ITT ITT7403
N82S06	Intersil IM5523 MMI 6531 TI SN74S201 TI SN74S301			N8260	Motorola MC7260 Raytheon RC8260	Motorola MC7403	ITT ITT7403
N82S07	Fairchild 93411 Intersil IM5533 MMI 6530 TI SN74S301	N82S236	Fairchild 93416 Intersil IM5603 MMI 6300 National DM8573 TI SN54S387	N8261	Hitachi HD2562 Motorola MC7261 Raytheon RC8261	N8488	ITT ITT7404
N82S08	Fairchild 93415 Fairchild 93421			N8262	Raytheon RC8262	Motorola MC7404	ITT ITT7404
N82S09	see page 804, 806, 817, MMI 6555	N82S26	Fairchild 93416 Intersil IM5603 MMI 6300 National DM8573 TI SN74S387	N8263	Raytheon RC8263	TI SN7404	ITT ITT7404
N82S10	see page 804, 806, 818, Fairchild 93415 TI SN74S309	N82S27	see page 804, 826, 832, Intel 3611	N8264	Raytheon RC8264	N8808	ITT ITT7430
N82S11	see page 804, 806, 818, Fairchild 93425			N8266	Motorola MC7266/67 Raytheon RC8266	Motorola MC7430	ITT ITT7430
		N82S29	Fairchild 93426 Intersil IM5623	N8267	Motorola MC7266/67 Raytheon RC8267	TI SN7430	ITT ITT7430
				N8268	ITT ITT7480 Motorola MC7268 TI SN7480	N8815	TI SN7425
				N8269	National DM8200	N8824	Motorola MC7474
				N8270	Motorola MC7270/71 Raytheon RC8270 TI SN74178	TI SN7474	Motorola MC7470
				N8271	Motorola MC7270/71 Raytheon RC8271 TI SN74179	N8825	Motorola MC7470
				N8277	Motorola MC7277 Raytheon RC8277	TI SN7474	ITT ITT7474
						N8828	ITT ITT7474
						Motorola MC7479	ITT ITT7474
						TI SN7474	TI SN7474
						N8829	Motorola MC7472
						N8840	ITT ITT7450
						Motorola MC7450	ITT ITT7450
						TI SN7450	TI SN7450
						N8848	ITT ITT74H74
						Motorola MC7453	ITT ITT74H74
						TI SN74H53	TI SN74H53
						N8875	Motorola MC7427
						TI SN7427	TI SN7427
						N8881	ITT ITT7401
						Motorola MC7401	ITT ITT7401
						TI SN7401	TI SN7401
						N8890	ITT ITT7404
						TI SN7404	ITT ITT7404
						N8891	ITT ITT7405
						TI SN7405	ITT ITT7405
						SE529	National LM161
						SE531	Raytheon RM4531
						SE550	National LM550
						SE555	AMD SE555
							Exar XR555M
							Intersil SE555
							Lithic Sys LS555
							National LM555
							Raytheon RM555
							Silicon G SG555
							Teledyne S 555
							TI SN52555

† Discontinued

The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
Signetics (cont)			S8T22	Raytheon TI	RM8T22 SN29601	S8280	Raytheon TI	RM8280 SN54176	2462	AMI	S8773
SE556	Raytheon	RM556	S8T23	Raytheon	RM8T23	S8281	Fairchild Raytheon TI	93177 RM8281 SN54177	25101	Intersil Mostek	IM7512 MK4007
SE565	National	LM565	S8T24	Raytheon	RM8T24	S8288	National	DM7288	2501	AMI see page 706	S4006 IM7501
SE566	National	LM566	S82S06	TI	SN54S201	S8290	Fairchild Raytheon TI	93196 RM8290 SN54196	2502	AMI	S2503A
SE567	National	LM567	S82S07	TI	SN54S301	S8291	Fairchild Raytheon TI	93197 RM8291 SN54197	2503	Synertek	SY1402
SN75107	AMD	SN75107B DS75107 RC75107A SN75107	S82S123	see page 804, 826, 828, Harris	HM7603 see page 746	S8292	TI	SN54LS196	2504	AMI	SY1403
SN75108	AMD	SN75108B DS75108 RC75108A SN75108	S82S126	see page 804, 826, 835, Harris	HPROM-1024A TI SN54S385 SN54S387	S8293	TI	SN54LS197	2505	AMI	AM2805 S2505A
SN7520	National	DS7520 SN7520	S82S129	see page 804, 826, 835, Harris	HPROM-1024 TI SN54S287	S8455	TI	SN5440	2512	AMD	AM2806 S2512A
SN7521	National	DS7521 SN7521	S82S17	TI	SN54S301	S8470	TI	SN5410	2513	Intersil	IM7712
SN7522	National	DS7522 SN7522	S82S23	see page 804, 826, 828, Harris	HM7602 see page 746	S8471	TI	SN5412	2518	Nortec	2512
SN7523	National	DS7523 SN7523	S82S25	TI	SN54S188	S8480	TI	SN5400	2519	GI	RO3-2513
SN7524	Fairchild National TI	7524 DS7524 SN7524	S82S26	AMD	82S26	S8481	TI	SN5403	2521	TI	TMS3122
SN7525	Fairchild National TI	7525 DS7525 SN7525	S82S29	National	DM7574 SN54S287	S8488	TI	SN5403	2522	AMD	AM2521
SN75450	Fairchild National Raytheon TI	75450 DS75450 RC75450 SN75450	S82S30	Fairchild	93S12	S8875	TI	SN5404	2523	AMI	S2181
SN75451	Fairchild National Raytheon TI	75451 DS75451 RC75451 SN75451	S82S62	Fairchild	93S62	S8881	TI	SN5401	2524	TI	TMS3128
SU536	Intersil	SU536	S8200	Raytheon	RM8200	S8890	TI	SN5404	2527	AMI	S2181
S54H00	Fairchild Fairchild TI	54H00 9H00 SN54H00	S8201	Raytheon	RM8201	S8891	TI	SN5405	2532	TI	TMS3129
S54LS138	see page 384 Raytheon	54LS138 see page 282	S8202	Raytheon	RM8202	S93410	Fairchild TI	93410 SN54S301 SN74S301	2524	AMD	AM2807 S1685
S54LS139	see page 384 Raytheon	54LS139 see page 282	S8203	Raytheon	RM8203	10101	Motorola	MC10101	2525	AMI	AM2808
S54LS253	see page 384 Raytheon	54LS253 see page 282	S8207	TI	SN54S301	10102	Motorola	MC10102	2526	Intersil	IM7722
S54S00	Fairchild Fairchild TI	54S00 9500 SN54S00	S8223	Harris Intersil MMI	HPROM-8256 IM5600 5330	10105	Motorola	MC10105	2527	AMI	S8564
S5400	Fairchild Fairchild TI	5400 9N00 SN5400	S8224	National	DM7577 SN54S188	10106	Motorola	MC10106	2548	Synertek	SY2527
S5556	Motorola Raytheon Raytheon Silicon G TI	MC1556 RM1556 RM1556A SG1556 SN52771	S8225	Fairchild TI	93434 IM5600 DM5488 SN5488A	10107	Motorola	MC10107	2532	AMI	S2181
S5558	Motorola Raytheon RCA Silicon G TI	MC1558 RM1558 CA1558 SG1558 SN52558	S8230	Fairchild Raytheon TI	93403 SN54S289	10109	Motorola	MC10109	2536	Intersil	IM7780
S5596	Lithic Sys Motorola Silicon G	LS1596 MC1596 SG1596	S8231	Fairchild Raytheon TI	9312 RM8230 SN39312	10110	Motorola	MC10110	2537	TI	TMS3120
S7280	National	DM7280	S8241	Fairchild Raytheon	9313 RM8231	10111	Motorola	MC10111	2538	AMI	AM2833
S7281	National	DM7281	S8242	Fairchild Raytheon TI	9386 RM8242 SN54LS266	10115	Motorola	MC10115	2548	Synertek	SY2533
S7290	National	DM7290	S8250	Raytheon	RM8250	10116	Motorola	MC10116	2548	TI	TMS3133
S7291	National	DM7291	S82506	Raytheon	RM5340	10117	Motorola	MC10117	2548	GI	AY5-1013
S8H70	TI	SN54H11	S82507	Raytheon	RM5330	10118	Motorola	MC10118	2602	TI	TMS6011
S8H80	TI	SN54H00	S8251	Raytheon	RM8251	10119	Motorola	MC10119	see page 790	Intersil	IM7752
S8H90	TI	SN54H04	S8252	Fairchild Raytheon TI	9301 RM8252 SN39301	10121	Motorola	MC10121	see page 790	Mostek	MK4102
S8T09	Raytheon	RM8T09	S8260	Raytheon	RM8260	10122	Motorola	MC10122	see page 790	TI	TMS4033
S8T10	Raytheon	RM8T10 SN54173	S8261	Raytheon	RM8261	10125	Motorola	MC10125	see page 790	TI	TMS4035
S8T13	Raytheon	RM8T13 SN55121	S8262	Raytheon	RM8262	10130	Motorola	MC10130	3207	ITT	IT75361
S8T14	Raytheon	RM8T14 SN55122	S8263	Raytheon	RM8263	10131	Motorola	MC10131	54LS00	Raytheon	54LS00
S8T22	Fairchild	9601	S8264	Raytheon	RM8264	10132	Motorola	MC10132	see page 282	Raytheon	54LS01
			S8266	Raytheon	RM8266	10133	Motorola	MC10133	see page 282	Raytheon	54LS02
			S8267	Raytheon	RM8267	10134	Motorola	MC10134	see page 282	Raytheon	54LS03
			S8268	TI	SN5480	10136	Motorola	MC10136	see page 282	Raytheon	54LS04
			S8269	National	DM7200	10137	Motorola	MC10137	see page 282	Raytheon	54LS05
			S8270	Fairchild Raytheon TI	93178 RM8270 SN54178	10140	Motorola	MC10140	see page 282	Raytheon	54LS10
			S8271	Fairchild Raytheon TI	93179 RM8271 SN54179	10141	Motorola	MC10141	see page 282	Raytheon	54LS109
			S8277	Fairchild Raytheon	9328 RM8277	10144	Fairchild	F10410	see page 282	Raytheon	54LS109
			S8280	Fairchild	93176	10145	Motorola	MCM10145	see page 282	Raytheon	54LS112
						10149	Motorola	MC10149	see page 282	Raytheon	54LS112
						10160	Motorola	MC10160	see page 282	Raytheon	54LS113
						10161	Motorola	MC10161	see page 282	Raytheon	54LS114
						10162	Motorola	MC10162	see page 282	Raytheon	54LS114
						10164	Motorola	MC10164	see page 282	Raytheon	54LS12
						10171	Motorola	MC10171	see page 282	Raytheon	54LS12
						10172	Motorola	MC10172	see page 282	Raytheon	54LS12
						10173	Motorola	MC10173	see page 282	Raytheon	54LS136
						10174	Motorola	MC10174	see page 282	Raytheon	54LS136
						10175	Motorola	MC10175	see page 282	Raytheon	54LS138
						10176	Motorola	MC10176	see page 282	Raytheon	54LS138
						10181	Motorola	MC10181	see page 282	Raytheon	54LS139
						10210	Motorola	MC10210	see page 282	Raytheon	54LS139
						10211	Motorola	MC10211	see page 282	Raytheon	54LS151
						10212	Motorola	MC10212	see page 282	Raytheon	54LS151
						1103	AMI	S1103	see page 282	Raytheon	54LS153
						2400	AMI	S8773	see page 282	Raytheon	54LS158
						2441	AMI	S8773	see page 282	Raytheon	54LS158
						2451	AMI	S8773	see page 282	Raytheon	54LS160
						2461	AMI	S8773	see page 282	Raytheon	54LS160

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ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device
Signetics (cont)							
54LS161	Raytheon 54LS161 see page 282	SG105	National LM105 Raytheon LM105 Teledyne S LM105	SG208	Teledyne S LM208	SG723	Teledyne S 723
54LS162	Raytheon 54LS162 see page 282	SG107	AMD LM107 Intersil LM107 National LM107 Raytheon LM107 RCA CA107 see page 661	SG209	National LM209	SG733	AMD 733 Raytheon RC733 Raytheon RM733 Signetics μ A733
54LS163	Raytheon 54LS163 see page 282			SG210	AMD LM210 Intersil LM210 National LM210	SG741	AMD 741 National LM741 PMI SSS741 Raytheon RC741 Raytheon RM741 RCA CA741 see page 661
54LS174	Raytheon 54LS174 see page 282			SG211	AMD LM211 Harris HA-2211 Intersil LM211 National LM211 Raytheon LM211 RCA CA211 see page 661	SG747	AMD 747 National LM747 PMI SSS747 Raytheon RC747 Raytheon RM747 RCA CA747 see page 661
54LS175	Raytheon 54LS175	SG108	AMD LM108 Intersil LM108 National LM108 Raytheon LM108 RCA CA108	SG301	AMD LM301 National LM301 Raytheon LM301 RCA CA301 see page 661		
54LS181	Raytheon 54LS181 see page 282				Signetics LM301 Teledyne S LM301		Signetics μ A741 Teledyne S 741
54LS190	Raytheon 54LS190 see page 282	SG109	National LM109 Raytheon LM109	SG3018	Lithic Sys LA3018		
54LS191	Raytheon 54LS191 see page 282	SG110	AMD LM110 Intersil LM110 National LM110	SG3026	Lithic Sys LA3026	SG748	AMD 748 Raytheon RC748 Raytheon RM748 RCA CA748 Signetics μ A748 Teledyne S 748
54LS192	Raytheon 54LS192 see page 282	SG111	AMD LM111 Harris HA-2111 Intersil LM111 National LM111 Raytheon LM111 RCA CA111 see page 661	SG304	Raytheon LM304 Teledyne S LM304		
54LS193	Raytheon 54LS193 see page 282			SG3045	Lithic Sys LA3045		
54LS194A	Raytheon 54LS194A see page 282	SG1458	Harris HA-2655 PMI SSS1458 Raytheon RC1458 RCA CA1458 Teledyne S 1458	SG305	AMD LM305 National LM305 Raytheon LM305 Teledyne S LM305	SG748C	Raytheon RC748
54LS195A	Raytheon 54LS195A see page 282	SG1488	AMD MC1488 Exar XR1488 National DS1488 Raytheon RC1488	SG307	AMD LM307 National LM307 Raytheon LM307 RCA CA307 see page 661	SG7520	National DS7520 Raytheon RC7520 Signetics SN7520
54LS196	Raytheon 54LS196 see page 282			SG308	AMD LM308 National LM308 Raytheon LM308 RCA CA308 Teledyne S LM308	SG7521	National DS7521 Signetics SN7521
54LS197	Raytheon 54LS197 see page 282	SG1489	AMD MC1489 Exar XR1489 National DS1489 Raytheon RC1489	SG3086	Lithic Sys LA3086	SG7522	National DS7522 Signetics SN7522
54LS20	Raytheon 54LS20 see page 282	SG1489A	Exar XR1489A	SG309	National LM309 Raytheon LM309	SG7523	National DS7523 Signetics SN7523
54LS251	Raytheon 54LS251 see page 282	SG1495	Lithic Sys LS1495	SG310	National LM310	SG7524	National DS7524 Signetics SN7524
54LS253	Raytheon 54LS253 see page 282	SG1496	Lithic Sys LS1496 Signetics MC1496	SG311	AMD LM311 Harris HA-2311 National LM311 Raytheon LM311 RCA CA311 see page 661	SG7525	National DS7525 Signetics SN7525
54LS257	Raytheon 54LS257 see page 282	SG1558	Harris HA-2650 PMI SSS1558 Raytheon RM1558 RCA CA1558 Teledyne S 1558	SG3821	Lithic Sys LA3045		
54LS26	Raytheon 54LS26 see page 282			SG3822	Lithic Sys LA3026		
54LS28	Raytheon 54LS28 see page 282	SG1595	Lithic Sys LS1595	SG3886	Lithic Sys LA3086		
54LS283	Raytheon 54LS283 see page 282	SG1596	Lithic Sys LS1596 Signetics MC1496	SG555	Lithic Sys LS555 Raytheon RC555 Raytheon RM555 RCA CA555 see page 661		
54LS295A	Raytheon 54LS295A see page 282	SG201	AMD LM201 Harris HI201 Intersil LM201 National LM201 Raytheon LM201 RCA CA748	SG709	National LM709 Raytheon RM709 Signetics μ A709 Teledyne S 709		
54LS33	Raytheon 54LS33 see page 282			SG710	National LM710 Raytheon RC710 Raytheon RM710 Signetics μ A710 Teledyne S 710		
54LS37	Raytheon 54LS37 see page 282	SG205	AMD LM205 Intersil LM205 National LM205 Raytheon LM205 Teledyne S LM205	SG711	National LM711 Raytheon RC711 Raytheon RM711 Signetics μ A711 Teledyne S 711		
54LS38	Raytheon 54LS38 see page 282	SG207	AMD LM207 Intersil LM207 National LM207 Raytheon LM207 RCA CA207 see page 661	SG723	AMD 723 Intersil 723 National LM723 Raytheon RC723 Raytheon RM723 RCA CA723 Signetics μ A723		
54LS40	Raytheon 54LS40 see page 282						
54LS54	Raytheon 54LS54 see page 282	SG208	AMD LM208 Intersil LM208 National LM208 Raytheon LM208 RCA CA208				
54LS55	Raytheon 54LS55 see page 282						
54LS73	Raytheon 54LS73 see page 282						
54LS75	Raytheon 54LS75						
54LS76	Raytheon 54LS76 see page 282						
54LS78	Raytheon 54LS78 see page 282						
54LS83	Raytheon 54LS83A see page 282						
54LS86	Raytheon 54LS86 see page 282						
54LS95B	Raytheon 54LS95B see page 282						
Silicon General							
SG101	AMD LM101 Intersil LM101 National LM101 Raytheon LM101 RCA CA748 Signetics LM101 Teledyne S LM101						
SG105	AMD LM105 Intersil LM105						
Siliconix							
						DG126	see page 551 Intersil DG126 National AH0126
						DG129	see page 551 Intersil DG129 National AH0129
						DG133	see page 551 Intersil DG133 National AH0133
						DG134	see page 551 Intersil DG134 National AH0134
						DG139	see page 551 Intersil DG139 National AH0139
						DG140	see page 551 Intersil DG140 National AH0140
						DG142	see page 551 Intersil DG142 National AH0142
						DG143	see page 551 Intersil DG143 National AH0143
						DG144	see page 551 Intersil DG144 National AH0144
						DG145	see page 551 Intersil DG145 National AH0145
						DG146	see page 551 Intersil DG146 National AH0146
						DG151	see page 551 Intersil DF151

1 Discontinued

The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
Siliconix (cont)			SCL4012	Motorola National RCA	MC14012 CD4012 CD4012	SCL4028	National RCA	CD4028 CD4028	SCL4518	National RCA	CD4518 CD4518
DG151	National	AH0151									
DG153	see page 551		SCL4013	Harris Motorola	HD4013 MC14013	SCL4029	Harris National RCA	HD4029 CD4029 CD4029	SCL4520	Harris National RCA	HD4520 CD4520 CD4520
DG154	see page 551			National RCA	CD4013 CD4013						
DG163	see page 551		SCL4014	Harris Intersil National	HD4014 DG163 AM0163	SCL4030	Harris National RCA	HD4030 CD4030 CD4030	SCL5437	Mostek	MK50040
DG164	see page 551			Motorola RCA	MC14014 CD4014				Solitron Devices		
DG200	see page 559, 560		SCL4015	Harris Motorola National RCA	HD4015 MC14015 CD4015 CD4015	SCL4033	RCA	CD4033	CM4000	Harris Motorola RCA	HD4000 MC14000 CD4000
DG506	see page 561, 563, 564, AD	AD7513								SSS	SCL4000
	see page 546		SCL4016	Motorola National RCA	MC14016 CD4016 CD4016	SCL4034	RCA	CD4034	CM4001	Harris Motorola National RCA	HD4001 MC14001 CD4001 CD4001
DG507	see page 561, 563, 564, AD	AD7507								SSS	SCL4001
	see page 548		SCL4017	Harris Motorola National RCA	HD4017 MC14017 CD4017 CD4017	SCL4035	Harris RCA	HD4035 CD4035	CM4002	Harris Motorola National RCA	HD4002 MC14002 CD4002 CD4002
DG509	see page 561, 563, 564, Harris	H1509								SSS	SCL4001
LM101	RCA	CA101	SCL4018	Harris National RCA	HD4018 CD4018 CD4018	SCL4042	Harris National RCA	HD4042 CD4042 CD4042	CM4006	Harris Motorola RCA	HD4006 MC14006 CD4006
	see page 661									SSS	SCL4006
	Teledyne S	LM101	SCL4019	Harris Motorola National RCA	HD4019 MC14019 CD4019 CD4019	SCL4043	Harris National RCA	HD4043 CD4043 CD4043	CM4007	Harris Motorola National RCA	HD4007 MC14007 CD4007 CD4007
SMC Microsystems Corp.										SSS	SCL4007
COM2017	AMI	S1883	SCL4020	Harris Motorola National RCA	HD4020 MC14020 CD4020 CD4020	SCL4044	Harris National National RCA	HD4044 CD4044 MM4644 CD4044	CM4008	Harris Motorola RCA	HD4008 MC14008 CD4008
COM2505	GI	AY5-1013								SSS	SCL4008
KR2376	GI	AY5-2376	SCL4021	Harris Motorola National RCA	HD4021 MC14021 CD4021 CD4021	SCL4049	Harris National RCA	HD4049 CD4049 CD4049	CM4009	Motorola RCA	MC14009 CD4009
KR3600	GI	AY5-KR3600								SSS	SCL4009
SMC2376	GI	AY5-2376	SCL4022	Harris Motorola National RCA	HD4022 MC14022 CD4022 CD4022	SCL4051	RCA	CD4051	CM4010	Motorola National RCA	MC14010 CD4010 CD4010
Solid State Scientific										SSS	SCL4010
SCL4000	Harris Motorola RCA	HD4000 MC14000 CD4000	SCL4023	Harris Motorola National RCA	HD4023 MC14023 CD4023 CD4023	SCL4052	RCA	CD4052	CM4011	Harris Motorola National RCA	HD4011 MC14011 CD4011 CD4011
SCL4001	Harris Motorola National RCA	HD4001 MC14001 CD4001 CD4001								SSS	SCL4011
SCL4002	Harris Motorola National RCA	HD4002 MC14002 CD4002 CD4002	SCL4024	Harris Motorola National RCA	HD4024 MC14024 CD4024 CD4024	SCL4053	RCA	CD4053	CM4012	Harris Motorola RCA	HD4012 MC14012 CD4012
SCL4006	Harris Motorola RCA	HD4006 MC14006 CD4006								SSS	SCL4012
SCL4007	Harris Motorola National RCA	HD4007 MC14007 CD4007 CD4007	SCL4025	Harris Motorola National RCA	HD4025 MC14025 CD4025 CD4025	SCL4054	RCA	CD4054	CM4013	Harris Motorola National RCA	HD4013 MC14013 CD4013 CD4013
SCL4008	Harris RCA	HD4008 CD4008								SSS	SCL4013
SCL4009	Motorola National RCA	MC14009 CD4009 CD4009	SCL4026	RCA	CD4026	SCL4055	RCA	CD4055	CM4014	Harris Motorola RCA	HD4014 MC14014 CD4014
SCL4010	Motorola National RCA	MC14010 CD4010 CD4010								SSS	SCL4014
SCL4011	Harris National RCA	HD4011 CD4011 CD4011	SCL4027	Harris Motorola National RCA	HD4027 MC14027 CD4027 CD4027	SCL4056	Harris National RCA	HD4056 CD4056 CD4056	CM4015	Harris Motorola National RCA	HD4015 MC14015 CD4015 CD4015
SCL4012	Harris	HD4012	SCL4028	Harris	HD4028	SCL4518	Harris	HD4518		SSS	SCL4015

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ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device
Solitron Devices (cont)							
CM4016	Motorola MC14015 National CD4016 RCA CD4016 see page 375 SSS SCL4016	CM4029	RCA CD4029 see page 375 SSS SCL4029	CM4053	RCA CD4053 see page 375 SSS SCL4053	SW1808	TI SN151808
CM4017	Harris HD4017 Motorola MC14017 National CD4017 RCA CD4017 see page 375 SSS SCL4017	CM4030	Harris HD4030 see page 266 National CD4030 RCA CD4030 see page 375 SSS SCL4030	CM4066	Harris HD4066 RCA CD4066 see page 375 SSS SCL4066	SW1810	Motorola MC1810 TI SN151810
CM4018	Harris HD4018 see page 266 National CD4018 RCA CD4018 see page 375 SSS SCL4018	CM4032	Motorola MC14032 RCA CD4032 see page 375	CM4510	National CD4510	SW1812	Motorola MC1812 TI SN151812
CM4019	Harris HD4019 see page 266 Motorola MC14519 National CD4019 RCA CD4019 see page 375 SSS SCL4019	CM4033	RCA CD4033 see page 375 SSS SCL4033	CM4511	National CD4511 RCA CD4511 see page 375	SW1814	Motorola MC1814
CM4020	Harris HD4020 see page 266 Motorola MC14020 National CD4020 RCA CD4020 see page 375 SSS SCL4020	CM4034	RCA CD4034 see page 375 SSS SCL4034	CM4514	RCA CD4514 see page 375	SW1900	Motorola MC1900 TI SN151900
CM4021	Harris HD4021 see page 266 Motorola MC14021 National CD4021 RCA CD4021 see page 375 SSS SCL4021	CM4035	Harris HD4035 see page 266 RCA CD4035 see page 375 SSS SCL4035	CM4515	RCA CD4515 see page 375	SW1901	Motorola MC1901 TI SN151901
CM4022	Harris HD4022 see page 266 Motorola MC14022 National CD4022 RCA CD4022 see page 375 SSS SCL4022	CM4036	RCA CD4036 see page 375	CM4518	National CD4518 Harris HD4518 National CD4518 RCA CD4518 see page 375 SSS SCL4518	SW1902	Motorola MC1902 TI SN151902
CM4023	Harris HD4023 Motorola MC14023 National CD4023 RCA CD4023 see page 375 SSS SCL4023	CM4037	RCA CD4037 see page 375	CM4520	Harris HD4520 National CD4520 RCA CD4520 see page 375	SW1905	Motorola MC1905 TI SN151905
CM4024	Harris HD4024 Motorola MC14024 National CD4024 RCA CD4024 see page 375 SSS SCL4024	CM4038	Motorola MC14038 RCA CD4038 see page 375	MA2556	Mostek MK4007	SW1906	Motorola MC1906 TI SN151906
CM4025	Harris HD4025 Motorola MC14025 National CD4025 RCA CD4025 see page 375 SSS SCL4025	CM4039	RCA CD4039 see page 375	MA2656	Mostek MK4007	SW1907	Motorola MC1907 TI SN151907
CM4026	RCA CD4026 see page 375 SSS SCL4026	CM4040	Harris HD4040 Motorola MC14040 National CD4040 RCA CD4040 see page 375 SSS SCL4040	MA3556	Mostek MK4007	SW1908	Motorola MC1908 TI SN151908
CM4027	Harris HD4027 Motorola MC14027 National CD4027 RCA CD4027 see page 375 SSS SCL4027	CM4041	RCA CD4041 see page 375 SSS SCL4041	UC4250	Silicon G SG4250	SW1910	Motorola MC1910 TI SN151910
CM4028	Harris HD4028 see page 266 Motorola MC14028 National CD4028 RCA CD4028 see page 375	CM4042	Harris HD4042 Motorola MC14042 National CD4042 RCA CD4042 see page 375 SSS SCL4042	UC4741	PMI SSS741 RCA CA741 see page 661 Teledyne S 741	SW1912	Motorola MC1912 TI SN151912
CM4029	Harris HD4029 see page 266 National CD4029	CM4043	Harris HD4043 National CD4043 RCA CD4043 see page 375 SSS SCL4043	Sprague Electric Co.		SW1914	Motorola MC1914
		CM4044	Harris HD4044 National CD4044 RCA CD4044 see page 375 SSS SCL4044	ULN-2111	National LM2111 RCA CA2111	SW301	Motorola MC301
		CM4045	RCA CD4045 see page 375	ULN-2114	Fairchild μ A746 RCA CA3072	SW302	Motorola MC302
		CM4046	RCA CD4046 see page 375	ULN-2120	Fairchild μ A732	SW303	Motorola MC303
		CM4047	RCA CD4047 see page 375	ULN-2124	Fairchild μ A780 RCA CA3070	SW304	Motorola MC304
		CM4048	RCA CD4048 see page 375	ULN-2126	Fairchild μ A739 Fairchild 739	SW305	Motorola MC305
		CM4049	Harris HD4049 National CD4049 RCA CD4049 see page 375 SSS SCL4049	ULN-2127	Fairchild μ A781 RCA CA3071	SW306	Motorola MC306
		CM4050	Harris HD4050 National CD4050 RCA CD4050 see page 375 SSS SCL4050	ULN-2128	Fairchild μ A767	SW307	Motorola MC307
		CM4051	RCA CD4051 see page 375 SSS SCL4051	ULN-2131	Fairchild μ A753	SW308	Motorola MC308
		CM4052	RCA CD4052 see page 375 SSS SCL4052	ULN-2136	Fairchild 2136	SW309	Motorola MC309
				ULN-2165	Fairchild μ A3065	SW310	Motorola MC310
				ULN-2210	RCA CA1310	SW311	Motorola MC311
				ULN-2262	RCA CA3126	SW351	Motorola MC351
				ULN-2266	RCA CA3066	SW352	Motorola MC352
				ULN-2298	RCA CA1398	SW353	Motorola MC353
				ULN-2741	National LM741 RCA CA741 see page 661 Teledyne S 741	SW354	Motorola MC354
				ULN-2747	RCA CA747 see page 661 Teledyne S 747	SW355	Motorola MC355
				ULN-2778	Fairchild μ A705	SW356	Motorola MC356
				Stewart-Warner Microcircuits		SW357	Motorola MC357
				SW1800	Motorola MC1800 TI SN151800	SW358	Motorola MC358
				SW1801	Motorola MC1801 TI SN151801	SW359	Motorola MC359
				SW1802	Motorola MC1802 TI SN151802	SW360	Motorola MC360
				SW1805	Motorola MC1805 TI SN15805	SW361	Motorola MC361
				SW1806	Motorola MC1806 TI SN151806	SW705-1	Motorola MC953 TI SN159093
				SW1807	Motorola MC1807 TI SN151807	SW705-2	Motorola MC853 TI SN158093
				SW1808	Motorola MC1808	SW706-1	Motorola MC952 TI SN15952
						SW706-2	Motorola MC852 TI SN15852
						SW708-1	Motorola MC956 TI SN15956
						SW708-2	Motorola MC856 TI SN15856
						SW709-1	Motorola MC955 TI SN15955
						SW709-2	Motorola MC855 TI SN15855
						SW930-1	Motorola MC930 TI SN15930
						SW930-2	Motorola MC830 TI SN15830
						SW932-1	Motorola MC932 TI SN15932
						SW932-2	Motorola MC832 TI SN15832
						SW933-1	Motorola MC933 TI SN15933
						SW933-2	Motorola MC833 TI SN15833
						SW935-1	Motorola MC940 TI SN15935
						SW935-2	Motorola MC840 TI SN15835
						SW936-1	Motorola MC936 TI SN15936

† Discontinued

The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device			Replacement Source Device			Manufacturer Device			Replacement Source Device			Manufacturer Device			Replacement Source Device			Manufacturer Device			Replacement Source Device																																																																																																																										
Stewart-Warner Microcircuits (cont)																																																																																																																																															
SW936-2	Motorola	MC836	TI	SN15836		† 1001	Motorola	MC1001				† 1002	Motorola	MC1002				† 1003	Motorola	MC1003				† 1004	Motorola	MC1004				† 1005	Motorola	MC1005				† 1006	Motorola	MC1006				† 1007	Motorola	MC1007				† 1008	Motorola	MC1008				† 1009	Motorola	MC1009				† 1010	Motorola	MC1010				† 1011	Motorola	MC1011				† 1013	Motorola	MC1013				† 1014	Motorola	MC1014				† 1015	Motorola	MC1015				† 1016	Motorola	MC1016				† 1017	Motorola	MC1017				† 1018	Motorola	MC1018				† 1019	Motorola	MC1019				† 1020	Motorola	MC1020				† 1021	Motorola	MC1021				† 1024	Motorola	MC1024				† 1025	Motorola	MC1025				† 1029	Motorola	MC1029			

† Discontinued

Bold face device number indicates additional data is provided in Catalog section

ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
Teledyne Semiconductor (cont)			1458	Harris	HA-2655				Texas Instruments		
MM54C74	National	MM54C74		National	LM1458				SN151912	Motorola	MC1912
MM54C76	Harris	HD54C76		Raytheon	RC1458				SN158093	Motorola	MC853
	National	MM54C76		RCA	CA1458					SW	SW705
MM54C86	Harris	HD54C86		Signetics	MC1458	RC4136	Exar	XR4136		SW	SW8093
	National	MM54C86		Silicon G	SG1458			see page 640	SN158094	Motorola	MC856
MM54C89	Harris	HD54C89	1558	Fairchild	μA1558			Raytheon		SW	SW708
	National	MM54C89		Harris	HA-2650			RC4136	SN158097	Motorola	MC855
MM54C95	Harris	HD54C95		Motorola	MC1558	RC4558	Exar	XR4558		SW	SW709
	National	MM54C95		National	LM1558			Raytheon		SW	SW8097
MM74C00	Harris	HD74C00		RCA	CA1458			RC4558	SN158099	Motorola	MC852
	National	MM74C00		Signetics	MC1558	RM4136	Exar	XR4136		SW	SW706
MM74C02	Harris	HD74C02	555	Silicon G	SG1558			see page 640		SW	SW9099
	National	MM74C02		Exar	XR555			Raytheon	SN15830	Hitachi	HD2204
MM74C04	Harris	HD74C04		Lithic Sys	LS555	SN10101	Motorola	MC10101		Motorola	MC830
	National	MM74C04		National	CA555	SN10102	Motorola	MC10102	SN15831	Motorola	SW930
MM74C10	Harris	HD74C10	709	Exar	XR556	SN10104	Motorola	MC10104		SW	SW931
	National	MM74C10		Fairchild	μA709	SN10105	Motorola	MC10105	SN15832	Hitachi	HD2201
MM74C107	Harris	HD74C107		Raytheon	RC709	SN10106	Motorola	MC10106		Motorola	MC832
	National	MM74C107		Signetics	MA709	SN10107	Motorola	MC10107		SW	SW932
MM74C14	National	MM74C14	710	Fairchild	μA710	SN10109	Motorola	MC10109	SN15833	Hitachi	HD2202
MM74C151	Harris	HD74C151		National	LM710	SN10110	Motorola	MC10110		Motorola	MC833
	National	MM74C151		Raytheon	RC710	SN10111	Motorola	MC10111		SW	SW933
		see page 266		RCA	CA710	SN10115	Motorola	MC10115	SN15834	Motorola	MC834
MM74C154	Harris	HD74C154		Signetics	MA710	SN10116	Motorola	MC10116		SW	MC840
	National	MM74C154		Silicon G	SG710	SN10117	Motorola	MC10117	SN15835	Motorola	SW935
		see page 266		Fairchild	μA711	SN10118	Motorola	MC10118	SN15836	Hitachi	HD2206
MM74C157	Harris	HD74C157	711	National	LM711	SN10119	Motorola	MC10119		Motorola	MC836
	National	MM74C157		Raytheon	RC711	SN10121	Motorola	MC10121		SW	SW936
MM74C160	Harris	HD74C160		RCA	CA711	SN10130	Motorola	MC10130	SN15837	Motorola	MC837
	National	MM74C160		Signetics	MA723	SN10131	Motorola	MC10131		SW	SW937
		see page 266		Silicon G	SG711	SN10133	Motorola	MC10133	SN15838	Motorola	MC835
MM74C161	Harris	HD74C161	723	AMD	723	SN10147	Fairchild	F10405		SW	SW938
	National	MM74C161		Fairchild	μA723	SN10160	Motorola	MC10160	SN15844	Hitachi	HD2209
		see page 266		Intersil	LM723	SN10161	Motorola	MC10161		Motorola	MC844
MM74C162	Harris	HD74C162		Intersil	MA723	SN10175	Motorola	MC10175		SW	SW944
	National	MM74C162		National	CA723	SN10179	Motorola	MC10179	SN15845	Hitachi	HD2205
MM74C163	Harris	HD74C163		Raytheon	RC723	SN10181	Motorola	MC10181		Motorola	MC845
	National	MM74C163		Silicon G	SG723	SN151800	Motorola	MC1800	SN15846	Hitachi	HD2203
MM74C164	Harris	HD74C164	741	AMD	741		SW	SW1800		Motorola	MC846
	National	MM74C164		AD	AD741	SN151801	Motorola	MC1801		SW	SW946
		see page 625		Fairchild	μA741	SN151802	Motorola	MC1802	SN15848	Motorola	MC848
MM74C173	Harris	HD74C173		Intersil	LM741		SW	SW1802		SW	SW948
	National	MM74C173		Intersil	MA741	SN151803	Motorola	MC1803	SN15849	Motorola	MC849
MM74C192	Harris	HD74C192		National	LM741	SN151804	Motorola	MC1804		SW	SW949
	National	MM74C192		Raytheon	RC741		SW	SW1804	SN15850	Motorola	MC850
		see page 266		RCA	CA741	SN151805	Motorola	MC1805		SW	SW950
MM74C193	Harris	HD74C193		Signetics	MA741	SN151806	Motorola	MC1806	SN15851	Motorola	MC851
	National	MM74C193		Silicon G	SG741		SW	SW1806		SW	SW951
MM74C195	Harris	HD74C195	747	AMD	747	SN151807	Motorola	MC1807	SN15857	Motorola	MC857
	National	MM74C195		National	LM747	SN151808	Motorola	MC1808		SW	SW957
MM74C20	Harris	HD74C20		Raytheon	RC747		SW	SW1808	SN15858	Motorola	MC858
	National	MM74C20		RCA	CA747	SN151809	Motorola	MC1809		SW	SW958
MM74C200	Harris	HD74C200		Signetics	MA747	SN151810	Motorola	MC1810	SN15861	Motorola	MC861
	National	MM74C200		Silicon G	SG747		SW	SW1810		SW	SW961
		see page 661		Intersil	LM748	SN151811	Motorola	MC1811	SN15862	Hitachi	HD2207
MM74C42	Harris	HD74C42	748	Intersil	MA748	SN151812	Motorola	MC1812		Motorola	MC862
	National	MM74C42		National	LM748		SW	SW1812		SW	SW962
MM74C48	Harris	HD74C48		Raytheon	RC748	SN151900	Motorola	MC1900	SN15863	Motorola	MC863
	National	MM74C48		RCA	CA748		SW	SW1900		SW	SW963
MM74C73	Harris	HD74C73	75450	Signetics	MA748	SN151901	Motorola	MC1901	SN15903	Motorola	MC953
	National	MM74C73		Fairchild	75450		SW	SW1901		Raytheon	RM993
MM74C74	Harris	HD74C74		Fairchild	75451	SN151902	Motorola	MC1902		SW	SW705
	National	MM74C74		Fairchild	75452		SW	SW1902	SN15904	Motorola	MC956
MM74C76	Harris	HD74C76		Fairchild	75452	SN151903	Motorola	MC1903		Raytheon	RM994
	National	MM74C76		Fairchild	75453		SW	SW1903		SW	SW708
MM74C86	Harris	HD74C86		Fairchild	75453	SN151904	Motorola	MC1904	SN15907	Motorola	MC955
	National	MM74C86		Fairchild	75454		SW	SW1904		Raytheon	RM997
MM74C89	Harris	HD74C89		Fairchild	75454	SN151905	Motorola	MC1905		SW	SW709
	National	MM74C89		Fairchild	75460	SN151906	Motorola	MC1906	SN15909	Motorola	MC952
MM74C95	Harris	HD74C95		Fairchild	75461		SW	SW1906		Raytheon	RM999
	National	MM74C95		Fairchild	75462	SN151907	Motorola	MC1907		SW	SW706
TP1301	AD	AD509		Fairchild	75463	SN151908	Motorola	MC1908	SN15930	Motorola	MC930
		see page 624		Fairchild	75464		SW	SW1908		Raytheon	RM930
TP1322	AD	AD509		Fairchild	75464	SN151909	Motorola	MC1909		SW	SW930
		see page 624		Fairchild	75464	SN151910	Motorola	MC1910	SN15931	Motorola	MC931
TP301	AD	AD507		Fairchild	75464		SW	SW1910		Raytheon	RM931
		see page 624		Lithic Sys	LS171	SN151911	Motorola	MC1911		SW	SW931
TP321	AD	AD507	911A	Lithic Sys	LS271						
		see page 624		Lithic Sys	LS371						
1458	Fairchild	μA1458	911C	Lithic Sys	LS371						

† Discontinued

The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device			Replacement Source Device			Manufacturer Device			Replacement Source Device			Manufacturer Device			Replacement Source Device		
Texas Instruments (cont)						SN29308	Raytheon	RM9308	SN52558	National	LM1558	SN54H01	National	DM54H01			
SN15932	Motorola	MC932	SN29309	AMD	9309	SN52558	PMI	SSS1558	SN54H01	Raytheon	54H01	SN54H01	Raytheon	54H01			
	Raytheon	RM932		Fairchild	9309		Raytheon	RM1558	SN54H04	Fairchild	54H04	SN54H04	Fairchild	54H04			
	SW	SW932		National	DM9309		RCA	CA1558	SN54H04	Fairchild	9H04	SN54H04	National	DM54H04			
SN15933	Motorola	MC933	SN29310	AMD	9310	SN52702	Fairchild	μA702	SN54H05	Fairchild	54H05	SN54H05	Fairchild	54H05			
	Raytheon	RM933		Raytheon	RM9310		Motorola	MC1712	SN54H05	National	DM54H05	SN54H05	Raytheon	54H05			
	SW	SW933	SN29311	AMD	9311		Raytheon	RM702	SN54H05	Signetics	54H05	SN54H05	Signetics	54H05			
SN15934	Motorola	MC934	SN29312	AMD	9312	SN52709	Motorola	MC1709	SN54H10	Fairchild	54H10	SN54H10	Fairchild	54H10			
	Raytheon	RM934		ITT	ITT9312		National	LM709	SN54H10	Fairchild	9H10	SN54H10	National	DM54H10			
SN15935	Motorola	MC940		National	DM9312		Raytheon	RM709	SN54H10	National	DM54H10	SN54H10	Raytheon	54H10			
	Raytheon	RM935		Raytheon	RC9312		Signetics	μA709	SN54H10	Signetics	54H10	SN54H10	Signetics	54H10			
	SW	SW935		Raytheon	RM9312		Teledyne S	709	SN54H10	Signetics	54H10	SN54H10	Teledyne S	709			
SN15936	Motorola	MC936	SN29316	AMD	9316	SN52710	Fairchild	μA710	SN54H10	Fairchild	9H10	SN54H10	Fairchild	54H10			
	Raytheon	RM936		Raytheon	RM9316		Motorola	MC1710	SN54H10	National	DM54H10	SN54H10	National	DM54H10			
	SW	SW936	SN29318	AMD	9318		National	LM710	SN54H10	Raytheon	54H10	SN54H10	Raytheon	54H10			
SN15937	Motorola	MC937	SN29322	AMD	9322		Raytheon	RM710	SN54H10	Signetics	54H10	SN54H10	Signetics	54H10			
	Raytheon	RM937		Raytheon	RM9322		Signetics	μA710	SN54H10	Silicon G	SG710	SN54H10	Silicon G	SG710			
	SW	SW937	SN29601	AMD	9601		Teledyne S	710	SN54H10	Teledyne S	710	SN54H10	Teledyne S	710			
SN15938	Motorola	MC935		ITT	ITT93601	SN52711	Fairchild	μA711	SN54H10	Fairchild	54H10	SN54H10	Fairchild	54H10			
SN15941	SW	SW941		Motorola	MC9601		Motorola	MC1711	SN54H10	Fairchild	9H10	SN54H10	Fairchild	9H10			
SN15944	Motorola	MC944		National	DM9601		National	LM711	SN54H10	Signetics	54H10	SN54H10	Signetics	54H10			
	Raytheon	RM944		Raytheon	RF9601	SN39000	Raytheon	RM711	SN54H10	National	DM54H10	SN54H10	National	DM54H10			
	SW	SW944	SN39001	Fairchild	9000		Signetics	μA711	SN54H10	Fairchild	54H10	SN54H10	Fairchild	54H10			
SN15945	Motorola	MC945	SN39001	Fairchild	9001		Silicon G	SG711	SN54H10	National	DM54H10	SN54H10	National	DM54H10			
	Raytheon	RM945	SN39301	Fairchild	9301		Teledyne S	711	SN54H10	Teledyne S	711	SN54H10	Teledyne S	711			
	SW	SW945	SN39308	Fairchild	9308	SN52723	AMD	723	SN54H10	Fairchild	54H10	SN54H10	Fairchild	54H10			
SN15946	Motorola	MC946	SN39309	Fairchild	9309		Intersil	723	SN54H10	National	DM54H10	SN54H10	National	DM54H10			
	Raytheon	RM946	SN39312	Fairchild	9312		National	LM723	SN54H10	Raytheon	54H10	SN54H10	Raytheon	54H10			
	SW	SW946	SN39322	Fairchild	9322		Raytheon	RM923	SN54H10	Signetics	54H10	SN54H10	Signetics	54H10			
SN15948	Motorola	MC948	SN52101	AMD	LM101		Signetics	μA723	SN54H10	Teledyne S	723	SN54H10	Teledyne S	723			
	Raytheon	RM948		Fairchild	μA101	SN52733	AMD	733	SN54H10	Fairchild	54H10	SN54H10	Fairchild	54H10			
	SW	SW948		Intersil	LM101		Fairchild	μA733	SN54H10	Motorola	MC1733	SN54H11	National	DM54H11			
SN15949	Motorola	MC949		Motorola	MLM101		National	LM733	SN54H11	National	DM54H11	SN54H11	Raytheon	54H11			
	Raytheon	RM949		National	LM101		Raytheon	RM733	SN54H11	Signetics	54H11	SN54H11	Signetics	54H11			
	SW	SW949		Raytheon	LM101		Signetics	μA733	SN54H11	Silicon G	SG733	SN54H11	Silicon G	SG733			
SN15950	Motorola	MC950		Teledyne S	LM101		Silicon G	SG733	SN54H11	Teledyne S	733	SN54H11	Teledyne S	733			
	Raytheon	RM950				SN52741	AMD	741	SN54H11	Fairchild	54H11	SN54H11	Fairchild	54H11			
	SW	SW950					Fairchild	μA741	SN54H11	Motorola	MC1741	SN54H11	Motorola	MC1741			
SN15951	Motorola	MC951					Intersil	741	SN54H11	National	LM741	SN54H11	National	LM741			
	Raytheon	RM951					Motorola	MC1741	SN54H11	PMI	SSS741	SN54H11	PMI	SSS741			
	SW	SW951					Raytheon	RM741	SN54H11	Raytheon	54H11	SN54H11	Raytheon	54H11			
SN15957	Motorola	MC957					RCA	CA741	SN54H11	RCA	CA741	SN54H11	RCA	CA741			
	SW	SW957					see page 661		SN54H11	see page 661		SN54H11	see page 661				
SN15958	Motorola	MC958					Signetics	μA741	SN54H11	Signetics	54H11	SN54H11	Signetics	54H11			
	SW	SW958					Silicon G	SG741	SN54H11	Silicon G	SG741	SN54H11	Silicon G	SG741			
SN15961	Motorola	MC961					Teledyne S	741	SN54H11	Teledyne S	741	SN54H11	Teledyne S	741			
	Raytheon	RM961							SN54H11			SN54H11					
	SW	SW961							SN54H11			SN54H11					
SN15962	Motorola	MC962							SN54H11			SN54H11					
	Raytheon	RM962							SN54H11			SN54H11					
	SW	SW962							SN54H11			SN54H11					
SN15963	Motorola	MC963							SN54H11			SN54H11					
	Raytheon	RM963							SN54H11			SN54H11					
	SW	SW963							SN54H11			SN54H11					
SN29000	Fairchild	9000							SN54H11			SN54H11					
	ITT	ITT74104							SN54H11			SN54H11					
	ITT	ITT9000							SN54H11			SN54H11					
SN29001	Fairchild	9001							SN54H11			SN54H11					
	ITT	ITT74105							SN54H11			SN54H11					
	ITT	ITT9001							SN54H11			SN54H11					
SN29002	ITT	ITT9002							SN54H11			SN54H11					
	National	DM9002							SN54H11			SN54H11					
SN29003	ITT	ITT9003							SN54H11			SN54H11					
	National	DM9003							SN54H11			SN54H11					
SN29004	National	DM9004							SN54H11			SN54H11					
SN29005	ITT	ITT9005							SN54H11			SN54H11					
	National	DM9005							SN54H11			SN54H11					
SN29008	ITT	ITT9008							SN54H11			SN54H11					
	National	DM9008							SN54H11			SN54H11					
SN29009	ITT	ITT9009							SN54H11			SN54H11					
	National	DM9009							SN54H11			SN54H11					
SN29012	ITT	ITT9012							SN54H11			SN54H11					
SN29016	ITT	ITT9016							SN54H11			SN54H11					
	National	DM9016							SN54H11			SN54H11					
SN29300	AMD	9300							SN54H11			SN54H11					
	Raytheon	RM9300							SN54H11			SN54H11					
SN29301	AMD	9301							SN54H11			SN54H11					
	Fairchild	9301							SN54H11			SN54H11					
	National	DM9301							SN54H11			SN54H11					
SN29308	AMD	9308							SN54H11			SN54H11					
	Fairchild	9308							SN54H11			SN54H11					
	Raytheon	RC9308							SN54H11			SN54H11					

† Discontinued

ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device
Texas Instruments (cont)							
SN54H54	National Signetics	DM54H54 S54H54		SN54LS151	Signetics see page 384	S54LS151	SN54LS190 Signetics see page 384
SN54H55	Fairchild Fairchild National Signetics	54H55 9H55 DM54H55 S54H55		SN54LS152	Fairchild Raytheon see page 282	54LS152 54LS152	SN54LS191 AMD Fairchild Raytheon see page 282 Signetics
SN54H60	Fairchild Fairchild National Signetics	54H60 9H60 DM54H60 S54H60		SN54LS153	AMD Fairchild Raytheon see page 282 Signetics	SN54LS153 54LS153 54LS153	SN54LS192 Fairchild
SN54H61	Fairchild Fairchild National Signetics	54H61 9H61 DM54H61 S54H61		SN54LS155	Fairchild Raytheon see page 282	54LS155 54LS155	SN54LS193 AMD Fairchild Raytheon see page 282 Signetics
SN54H62	Fairchild Fairchild National Signetics	54H62 9H62 DM54H62 S54H62		SN54LS156	Fairchild Raytheon see page 282	54LS156 54LS156	SN54LS194A AMD Fairchild Raytheon see page 282 Signetics
SN54H71	Fairchild Fairchild National Signetics	54H71 9H71 DM54H71 S54H71		SN54LS157	AMD Fairchild Raytheon see page 282 Signetics	SN54LS157 54LS157 54LS157	SN54LS195A AMD Fairchild Raytheon see page 282 Signetics
SN54H72	Fairchild Fairchild National Signetics	54H72 9H72 DM54H72 S54H72		SN54LS158	AMD Fairchild Raytheon see page 282 Signetics	SN54LS158 54LS158 54LS158	SN54LS196 Fairchild Raytheon see page 282 Signetics
SN54H73	Fairchild Fairchild National Signetics	54H73 9H73 DM54H73 S54H73		SN54LS160	AMD Fairchild Raytheon see page 282 Signetics	SN54LS160 54LS160 54LS160	SN54LS197 Fairchild Raytheon see page 282 Signetics
SN54H74	Fairchild Fairchild National Signetics	54H74 9H74 DM54H74 S54H74		SN54LS161	AMD Fairchild Raytheon see page 282 Signetics	SN54LS161 54LS161 54LS161	SN54LS20 Fairchild National Raytheon see page 282 Signetics
SN54H76	Fairchild Fairchild National Signetics	54H76 9H76 DM54H76 S54H76		SN54LS162	AMD AMD Fairchild Raytheon see page 282 Signetics	SN54LSX62 SN54LS162 54LS162 54LS162	SN54LS21 Fairchild Raytheon Signetics
SN54H78	Fairchild Fairchild National	54H78 9H78 DM54H78		SN54LS163	AMD Fairchild Raytheon see page 282 Signetics	SN54LS163 54LS163 54LS163	SN54LS22 Fairchild National National Raytheon see page 282 Signetics
SN54H87	Fairchild Fairchild	54H87 93H87		SN54LS164	AMD Fairchild Signetics	AM54LS164 54LS164 S54LS164	SN54LS221 Signetics
SN54LS160	Fairchild Signetics	54LS260 S54LS260A see page 384		SN54LS170	Fairchild Signetics	54LS170 S54LS170 see page 384	SN54LS251 AMD Fairchild Raytheon see page 282 Signetics
SN54LS00	Fairchild National Raytheon see page 282 Signetics	54LS00 DM54LS00 54LS00 see page 282 S54LS00 see page 384		SN54LS174	AMD Fairchild Raytheon see page 282 Signetics	SN54LS174 54LS174 54LS174	SN54LS253 AMD Fairchild Raytheon see page 282 Signetics
SN54LS01	National Raytheon see page 282 Signetics	DM54LS01 54LS01 see page 282 S54LS01 see page 384		SN54LS175	AMD Fairchild Raytheon Raytheon Signetics	SN54LS175 54LS175 54LSX75 54LS175 S54LS175	SN54LS257 AMD Fairchild Raytheon see page 282 Signetics
SN54LS02	Fairchild Raytheon see page 282 Signetics	54LS02 54LS02 see page 282 S54LS02 see page 384		SN54LS181	AMD Fairchild Raytheon see page 282	SN54LS181 54LS181 54LS181	SN54LS258 AMD Fairchild Raytheon see page 282 Signetics
SN54LS03	Fairchild National Raytheon see page 282 Signetics	54LS03 DM54LS03 54LS03 see page 282 S54LS03 see page 384		SN54LS190	AMD Fairchild Raytheon see page 282	SN54LS190 54LS190 54LS190	SN54LS259 Fairchild
SN54LS04	Fairchild National Raytheon see page 282 Signetics	54LS04 DM54LS04 54LS04 see page 282 S54LS04 see page 384		SN54LS190	AMD Fairchild Raytheon see page 282	SN54LS190 54LS190 54LS190	SN54LS26 Fairchild
SN54LS05	Fairchild Raytheon see page 282 Signetics	54LS05 54LS05 see page 282 S54LS05 see page 384					
SN54LS08	Fairchild	54LS08					
SN54LS08	Raytheon see page 282 Signetics	54LS08 see page 282 S54LS08 see page 384		SN54LS10	Fairchild National Raytheon see page 282 Signetics	54LS10 DM54LS10 54LS10 see page 282 S54LS10 see page 384	SN54LS107 Raytheon see page 282 Signetics
SN54LS10	Fairchild National Raytheon see page 282 Signetics	54LS10 DM54LS10 54LS10 see page 282 S54LS10 see page 384		SN54LS107	Raytheon see page 282 Signetics	54LS107 see page 282 S54LS107 see page 384	SN54LS109 Fairchild Raytheon see page 282 Signetics
SN54LS107	Raytheon see page 282 Signetics	54LS107 see page 282 S54LS107 see page 384		SN54LS109	Fairchild Raytheon see page 282 Signetics	54LS109 54LS109 see page 282 S54LS109 see page 384	SN54LS112 Fairchild Raytheon see page 282 Signetics
SN54LS109	Fairchild Raytheon see page 282 Signetics	54LS109 54LS109 see page 282 S54LS109 see page 384		SN54LS112	Fairchild Raytheon see page 282 Signetics	54LS112 54LS112 see page 282 S54LS112 see page 384	SN54LS113 Fairchild Raytheon see page 282 Signetics
SN54LS112	Fairchild Raytheon see page 282 Signetics	54LS112 54LS112 see page 282 S54LS112 see page 384		SN54LS113	Fairchild Raytheon see page 282 Signetics	54LS113 54LS113 see page 282 S54LS113 see page 384	SN54LS114 Fairchild Raytheon see page 282 Signetics
SN54LS113	Fairchild Raytheon see page 282 Signetics	54LS113 54LS113 see page 282 S54LS113 see page 384		SN54LS114	Fairchild Raytheon see page 282 Signetics	54LS114 54LS114 see page 282 S54LS114 see page 384	SN54LS12 National Raytheon see page 282 Signetics
SN54LS114	Fairchild Raytheon see page 282 Signetics	54LS114 54LS114 see page 282 S54LS114 see page 384		SN54LS12	National Raytheon see page 282 Signetics	DM54LS12 54LS12 see page 282 S54LS12 see page 384	SN54LS123 AMD
SN54LS12	National Raytheon see page 282 Signetics	DM54LS12 54LS12 see page 282 S54LS12 see page 384		SN54LS123	AMD	SN54LS123	SN54LS125 Fairchild
SN54LS123	AMD	SN54LS123		SN54LS125	Fairchild	54LS125	SN54LS126 Fairchild
SN54LS125	Fairchild	54LS125		SN54LS126	Fairchild	54LS126	SN54LS132 Fairchild Signetics
SN54LS126	Fairchild	54LS126		SN54LS132	Fairchild Signetics	54LS132 S54LS132 see page 384	SN54LS136 Fairchild Raytheon see page 282 Signetics
SN54LS132	Fairchild Signetics	54LS132 S54LS132 see page 384		SN54LS136	Fairchild Raytheon see page 282 Signetics	54LS136 54LS136 see page 282 S54LS136 see page 384	SN54LS138 AMD Fairchild Raytheon see page 282 Signetics
SN54LS136	Fairchild Raytheon see page 282 Signetics	54LS136 54LS136 see page 282 S54LS136 see page 384		SN54LS138	AMD Fairchild Raytheon see page 282 Signetics	SN54LS138 54LS138 54LS138 see page 282 S54LS138 see page 384	SN54LS139 AMD Fairchild Raytheon see page 282 Signetics
SN54LS138	AMD Fairchild Raytheon see page 282 Signetics	SN54LS138 54LS138 54LS138 see page 282 S54LS138 see page 384		SN54LS139	AMD Fairchild Raytheon see page 282 Signetics	SN54LS139 54LS139 54LS139 see page 282 S54LS139 see page 384	SN54LS14 Fairchild Signetics
SN54LS139	AMD Fairchild Raytheon see page 282 Signetics	SN54LS139 54LS139 54LS139 see page 282 S54LS139 see page 384		SN54LS14	Fairchild Signetics	54LS14 S54LS14 see page 384	SN54LS145 Signetics
SN54LS14	Fairchild Signetics	54LS14 S54LS14 see page 384		SN54LS145	Signetics	54LS145 S54LS145 see page 384	SN54LS15 Fairchild Raytheon see page 282 Signetics
SN54LS145	Signetics	54LS145 S54LS145 see page 384		SN54LS15	Fairchild Raytheon see page 282 Signetics	54LS15 54LS15 see page 282 S54LS15 see page 384	SN54LS151 AMD Fairchild Raytheon see page 282
SN54LS15	Fairchild Raytheon see page 282 Signetics	54LS15 54LS15 see page 282 S54LS15 see page 384		SN54LS151	AMD Fairchild Raytheon see page 282	SN54LSU51 54LS151 54LS151 see page 282	
SN54LS151	AMD Fairchild Raytheon see page 282	SN54LSU51 54LS151 54LS151 see page 282					

1 Discontinued

The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device			Replacement Source Device			Manufacturer Device			Replacement Source Device			Manufacturer Device			Replacement Source Device		
Texas Instruments (cont)																	
			SN54LS54	Fairchild	54LS54			SN54L73	National	DM54L73			SN54S22	Fairchild	9S22		
				Raytheon	54LS54			SN54L74	National	DM54L74				National	DM54S22		
SN54LS26	Raytheon	54LS26		Signetics	54LS54			SN54L75	National	DM54L75			SN54S251	AMD	SN54S251		
	see page 282			see page 384				SN54L78	National	DM54L78			SN54S257	AMD	SN54S257		
			SN54LS261	Signetics	54LS261			SN54L85	National	DM54L85			SN54S258	AMD	SN54S258		
	see page 384			see page 384				SN54L86	National	DM54L86			SN54S270	MMI	5205		
			SN54LS266	Fairchild	54LS266			SN54L90	National	DM54L90			SN54S287	MMI	5301		
				Raytheon	54LS266			SN54L91	National	DM54L91				National	DM7574		
	see page 282			Signetics	54LS266			SN54L93	National	DM54L93				National	DM8574		
	see page 384			see page 384				SN54L95	National	DM54L95			SN54S288	MMI	5331		
			SN54LS27	Fairchild	54LS27			SN54L98	National	DM54L98			SN54S289	AMD	AM27S02		
				Raytheon	54LS27			SN54S00	Fairchild	54S00				AMD	SN54S289		
	see page 282			Signetics	54LS27				Fairchild	9S00			SN54S370	MMI	5206		
	see page 384			see page 384				SN54S03	National	DM54S00			SN54S387	Intel	3601		
			SN54LS279	Fairchild	54LS279				Fairchild	54S03				see page 772, 773			
									National	DM54S03				MMI	5300		
			SN54LS28	Raytheon	54LS28			SN54S04	Fairchild	54S04				MMI	6300		
	see page 282			Signetics	54LS28				Fairchild	9S04				National	DM54S387		
	see page 384			see page 384					National	DM54S04				National	DM7573		
			SN54LS283	Fairchild	54LS283			SN54S05	Fairchild	54S05				Signetics	N82S126		
				Raytheon	54LS283				Fairchild	9S05				see page 804, 826, 835,			
				Signetics	54LS283				National	DM54S05			SN54S40	Fairchild	54S40		
	see page 282			see page 384					National	DM54S10				Fairchild	9S40		
	see page 384			see page 384						DM54S11				National	DM54S40		
			SN54LS290	Fairchild	54LS290			SN54S11	National	DM54S11			SN54S64	Fairchild	54S64		
				Signetics	54LS290				Fairchild	54S112				Fairchild	9S64		
	see page 384			see page 384					Fairchild	9S112				National	DM54S64		
			SN54LS293	Fairchild	54LS293			SN54S112	National	DM54S112			SN54S65	Fairchild	54S65		
				Signetics	54LS293				Fairchild	54S113				Fairchild	9S65		
	see page 384			see page 384					National	DM54S113				National	DM54S65		
			SN54LS295A	Fairchild	54LS295			SN54S114	Fairchild	54S114			SN54S74	Fairchild	54S74		
				Raytheon	54LS295A				Fairchild	9S114				Fairchild	9S74		
	see page 282			Signetics	54LS295A				National	DM54S114				National	DM54S74		
	see page 384			see page 384					Fairchild	9S133			SN54S86	National	DM54S86		
				see page 384					Fairchild	9S134			SN5400	Fairchild	5400		
			SN54LS298	Fairchild	54LS298				AMD	SN54S138				Fairchild	9N00		
									AMD	SN54S139				National	DM5400		
			SN54LS30	Fairchild	54LS30			SN54S138	National	DM54S138				Raytheon	5400		
				National	DM54LS30				Fairchild	54S140				Signetics	55400		
				Raytheon	54LS30				Fairchild	9S140				Signetics	8889		
	see page 282			see page 282					National	DM54S140							
	see page 384			see page 384						DM54S15			SN5401	Fairchild	5401		
				Signetics	54LS30				AMD	SN54S151				Fairchild	9N01		
				see page 384					National	DM54S151				National	DM5401		
			SN54LS32	Fairchild	54LS32				AMD	SN54S153				Raytheon	5401		
				Raytheon	54LS32				National	DM54S153				Signetics	55401		
	see page 282			see page 282					AMD	SN54S157				Signetics	8881		
	see page 384			see page 384					National	DM54S157			SN5402	Fairchild	5402		
				Signetics	54LS32				AMD	SN54S158				Fairchild	9N02		
				see page 384					AMD	SN54S174				National	DM5402		
			SN54LS33	Raytheon	54LS33				AMD	SN54S175				Signetics	55402		
	see page 282			see page 282					AMD	SN54S174							
	see page 384			see page 384					AMD	SN54S175			SN5403	Fairchild	5403		
				Signetics	54LS33				AMD	SN54S181				Fairchild	9N03		
				see page 384					Fairchild	54S181				National	DM5403		
			SN54LS368	Fairchild	54LS368				Fairchild	93S41				Raytheon	5403		
									Fairchild	93S42				Signetics	55403		
			SN54LS37	Fairchild	54LS37					54S182							
				Raytheon	54LS37					DM54S182				SN5404	Fairchild	5404	
	see page 282			see page 282						93S42				Fairchild	9N04		
	see page 384			see page 384						AM27S09				Fairchild	DM5404		
				Signetics	54LS37					HM7602				Raytheon	5404		
				see page 384						see page 746				Signetics	55404		
			SN54LS378	AMD	SN54LS378									Signetics	8890		
			SN54LS38	Fairchild	54LS38			SN54S188A	MMI	5330							
				Raytheon	54LS38				AMD	AM27S/O				SN5405	Fairchild	5405	
	see page 282			see page 282					AMD	SN54S189				Fairchild	9N05		
	see page 384			see page 384						SN54S194				National	DM5405		
				Signetics	54LS38					SN54S195				National	5405		
				see page 384						Fairchild	93S00			Raytheon	5405		
				see page 384						Fairchild	54S20			Signetics	55405		
			SN54LS386	Raytheon	54LS386					National	DM54S20			Signetics	8891		
	see page 282			see page 282													
	see page 384			see page 384									SN5406	Fairchild	5406		
				see page 384										Fairchild	9N06		
				Signetics	54LS386									National	DM5406		
				see page 384										Signetics	55406		
			SN54LS40	Fairchild	54LS40			SN54S200	Intersil	IM5523							
				Raytheon	54LS40				MMI	5531							
	see page 282			see page 282						DM54S200				SN5407	Fairchild	5407	
	see page 384			see page 384						RM5340				Fairchild	9N07		
				Signetics	54LS40					554S200				National	DM5407		
				see page 384						see page 804, 806, 815,				National	55407		
				see page 384						TI	SN54S201			Signetics	55407		
			SN54LS42	Fairchild	54LS42												
				Signetics	54LS42									SN5408	Fairchild	5408	
	see page 384			see page 384										Fairchild	9N08		
				see page 384										National	DM5408		
				Signetics	54LS42									Raytheon	5408		
				see page 384										Signetics	55408		
			SN54LS51	Fairchild	54LS51												
				Raytheon	54LS51												
	see page 282			see page 282													
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				Signetics	54LS51												
				see page 384													
				see page 384													
				see page 384													

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Manufacturer Device			Replacement Source Device			Manufacturer Device			Replacement Source Device			Manufacturer Device			Replacement Source Device		
Texas Instruments (cont)																	
			SN54156	Raytheon Signetics	54156 S54156	SN54181	AMD AMD Fairchild Fairchild National Raytheon Signetics	SN54181 9341 54181 9341 DM54181 54181 S54181	SN54206	TI	SN545301	SN5422	Raytheon	5422	SN54221	AMD	SN54221
SN5409	Fairchild National Raytheon Signetics	9N09 DM5409 5409 S5409	SN54157	AMD Fairchild National Raytheon Signetics	SN54157 9322 DM9322 54157 S54157	SN54182	AMD AMD Fairchild Fairchild National Raytheon Signetics	SN54182 9342 54182 9342 DM54182 54182 S54182	SN5425	Fairchild Fairchild National	5425 9N25 DM5425	SN54251	National	DM7121	SN5426	Fairchild Fairchild National	5426 9N26 DM5426
SN5410	Fairchild Fairchild National Raytheon Signetics Signetics	5410 9N10 DM5410 5410 S5410 8879	SN54159	Raytheon	54159	SN54184	National	DM54184	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5428	Raytheon	5428
SN54107	AMD Fairchild Fairchild National Signetics	SN54107 54107 9N107 DM54107 S54107	SN54160	AMD Fairchild National Raytheon Signetics	SN54160 9310 DM54160 54160 S54160	SN54185A	Fairchild National	93434 DM54185A	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5428	Raytheon	5428
SN54109	National Signetics	DM54109 S54109	SN54161	AMD Fairchild National Raytheon Signetics	SN54161 9316 DM54161 54161 S54161	SN54186	Harris	HPROM-0512	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5428	Raytheon	5428
SN5412	Fairchild Fairchild Raytheon	5412 9N12 5412	SN54162	AMD National Raytheon Signetics	SN54162 DM54162 54162 S54162	SN54188	Harris	MM7602	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5428	Raytheon	5428
SN54121	Fairchild Motorola National Signetics	54121 9603 MC9603 DM54121 S54121	SN54163	AMD National Raytheon Signetics	SN54163 DM54163 54163 S54163	SN54188A	MMI National	5330 DM7577	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5428	Raytheon	5428
SN54123	AMD AMD National Raytheon Signetics	AM26123 SN54123 DM54123 54123 S54123	SN54164	AMD Fairchild Fairchild National Raytheon Signetics	SN54164 54164 93164 DM7570 54164 S54164	SN54190	Fairchild Fairchild National Raytheon	54190 93190 DM54190 54190	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5428	Raytheon	5428
SN54125	National	DM7093	SN54164	AMD Fairchild Fairchild National Raytheon Signetics	SN54164 54164 93164 DM7570 54164 S54164	SN54191	Fairchild Fairchild National Raytheon	54191 93191 DM54191 54191	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5428	Raytheon	5428
SN54126	National	DM7094	SN54165	Fairchild Fairchild National Raytheon Signetics	54165 93165 DM7590 54165 S54165	SN54192	AMD AMD Fairchild Fairchild National Raytheon Signetics	SN54192 9360 54192 9360 DM7560 54192 S54192	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5428	Raytheon	5428
SN5413	Fairchild Fairchild National Signetics	5413 9N13 DM5413 S5413	SN54166	Fairchild Fairchild National Raytheon Signetics	54166 93166 DM54166 54166 S54166	SN54193	AMD AMD Fairchild Fairchild National Raytheon	SN54193 9366 54193 9366 DM7563 54193 S54193	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5428	Raytheon	5428
SN54132	National Signetics	DM54132 S54132	SN54170	Fairchild Raytheon	54170 54170	SN54194	AMD National National Raytheon	SN54194 DM54194 DM8300 54194	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5428	Raytheon	5428
SN54136	Raytheon	54136	SN54173	National	DM7551	SN54195	AMD Fairchild National Raytheon Signetics	SN54195 9300 DM9300 54195 S54195	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5428	Raytheon	5428
SN5414	National Signetics	DM5414 S5414	SN54174	AMD Fairchild National Raytheon Signetics	SN54174 93174 DM54174 54174 S54174	SN54196	Fairchild Fairchild National National Raytheon	54196 93196 DM54196 S8290	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5428	Raytheon	5428
SN54141	National Signetics	DM54141 S54141	SN54175	AMD Fairchild National Raytheon Signetics	SN54175 93175 DM54175 54175 S54175	SN54197	Fairchild Fairchild National	54197 93197 DM54197	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5428	Raytheon	5428
SN54145	Fairchild Fairchild National Raytheon Signetics	54145 93145 DM54145 54145 S54145	SN54176	Fairchild Fairchild National Signetics	54176 93176 DM7280 S8280	SN54198	Fairchild Fairchild National National Raytheon Signetics	54198 93198 DM54198 54198 S54198	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5428	Raytheon	5428
SN54150	Fairchild Fairchild National Raytheon Signetics	54150 93150 DM54150 54150 S54150	SN54177	Fairchild Fairchild National Signetics	54177 93177 DM7281 S8281	SN54199	National Raytheon Signetics	DM54199 54199 S54199	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5428	Raytheon	5428
SN54151	Fairchild Fairchild National Raytheon Signetics TI	54151 93151 DM54151 54151 S54151 SN54151A	SN54178	Fairchild Fairchild National Signetics	54178 93178 S8270	SN54200	MMI National TI	5531 DM54200 SN54S201	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5427	Fairchild Fairchild National	5427 9N27 DM5427	SN5428	Raytheon	5428
SN54152	Fairchild Fairchild Raytheon Signetics TI	54152 93152 54152 S54152 SN54152A	SN54179	Fairchild Fairchild National Signetics	54179 93179	SN54206	MMI	5530	SN5427	Fairchild	5427	SN5427	Fairchild	5427	SN5428	Raytheon	5428
SN54153	AMD Fairchild Fairchild National Raytheon Signetics	SN54153 54153 93153 DM54153 54153 S54153	SN54180	Fairchild Fairchild National Signetics	54180 93180 DM54180 54180 S54180				SN5427	Fairchild	5427	SN5427	Fairchild	5427	SN5428	Raytheon	5428
SN54154	AMD Fairchild National Raytheon Signetics	SN54154 9311 DM54154 54154 S54154							SN5427	Fairchild	5427	SN5427	Fairchild	5427	SN5428	Raytheon	5428
SN54155	Fairchild National Raytheon Signetics	93155 DM54155 54155 S54155							SN5427	Fairchild	5427	SN5427	Fairchild	5427	SN5428	Raytheon	5428
SN54156	Fairchild National	93156 DM54156							SN5427	Fairchild	5427	SN5427	Fairchild	5427	SN5428	Raytheon	5428

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The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

IC UPDATE MASTER

Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	
Texas Instruments (cont)			† SN5488	National TI	DM5488 SN5488A	SN55452	Raytheon	RM55452	SN72709	Signetics Teledyne S	μA709 709	
† SN5447	Fairchild National TI	9357 DM5447 SN5447A	† SN5489	AMD Fairchild MMI	SN5489 93403 5560	SN55453	National Raytheon	DS55453 RM55453	SN72710	Fairchild Motorola National Raytheon	710 MC1710 LM710 RC710	
SN5448	Fairchild Fairchild National Signetics	5448 9358 DM5448 S5448		National Raytheon Signetics TI	DM5489 5489 S8225 SN54S189	SN55454	National Raytheon	DS55454 RM55454	SN55460	ITT National Silicon G	ITT55460 DS55460 SG55460	
SN5449	Fairchild Fairchild	5449 9359	† SN5490	Fairchild Fairchild National Signetics TI	5490 9390 DM5490 S5490 SN5490A	SN555	RCA	CA555	SN72711	Fairchild Motorola National Raytheon Signetics Silicon G	711 MC1711 LM711 RC711 μA711 SG711 Teledyne S 711	
SN5450	Fairchild Fairchild National Signetics	5450 9N50 DM5450 S5450 8859	† SN5491	Fairchild Fairchild National Signetics TI	5491 9391 DM5491 S5491 SN5491A	SN55702	Motorola	MC1712	SN5830	SW	SW930	
SN5451	Fairchild Fairchild National Signetics	5451 9N51 DM5451 S5451	† SN5492	Fairchild Fairchild National Signetics TI	5492 9392 DM5492 S5492 SN5492A	SN72301	AMD Fairchild Intersil Motorola National Raytheon RCA	LM301 LM301 LM301 MLM301 LM301 LM301 CA301	SN72301	AMD Fairchild Intersil Motorola National Raytheon RCA	LM301 LM301 LM301 MLM301 LM301 LM301 CA301	
SN5453	Fairchild Fairchild National Signetics	5453 9N53 DM5453 S5453	† SN5493	Fairchild Fairchild National Signetics TI	5493 9393 DM5493 S5493 SN5493A		Signetics Silicon G Teledyne S	LM301 SG301 LM301	SN72720	National	LM1414	
SN5454	Fairchild Fairchild National Signetics	5454 9N54 DM5454 S5454		Fairchild Fairchild National Signetics TI	5494 9394 DM5494 S5494	SN72305	AMD Intersil Raytheon Teledyne S	LM305 LM305 LM305 LM305	SN72723	AMD Intersil Raytheon Signetics Teledyne S	723 723 RC723 μA723 723	
SN5460	Fairchild Fairchild National Signetics	5460 9N60 DM5460 S5460	SN5494	Fairchild Fairchild Signetics	5494 9394 S5494	SN72307	Fairchild Intersil Motorola National Raytheon RCA	LM307 LM307 MLM307 LM307 LM307 CA307	SN72723	AMD Fairchild Motorola Raytheon Signetics Silicon G	733 733 MC1733 RC733 μA733 SG733	
SN5470	Fairchild Fairchild National Signetics	5470 9N70 DM5470 S5470	† SN5495	Fairchild Fairchild National Signetics TI	5495 9395 DM5495 S5495 SN5495A		Signetics Silicon G Teledyne S	LM307 SG307 LM307	SN72741	AMD Fairchild Intersil Motorola National PMI Raytheon RCA	741 741 741 MC1741 LM741 SSS741 RC741 CA741	
SN5472	Fairchild National Signetics	9N72 DM5472 S5472	SN5496	Fairchild Fairchild National Signetics	5496 9396 DM5496 S5496	SN72308	AMD Intersil Raytheon Silicon G Teledyne S	LM308 LM308 LM308 SG308 LM308		Signetics Silicon G Teledyne S	μA741 SG741 741	
SN5473	Fairchild Fairchild National Signetics	5473 9N73 DM5473 S5473	SN5510	Motorola	MC1510	SN72308	AMD Intersil Raytheon Silicon G Teledyne S	LM308 LM308 LM308 SG308 LM308	SN72747	AMD Fairchild Motorola PMI Raytheon RCA	747 747 MC1747 SSS747 RC747 CA747	
SN5474	Fairchild Fairchild National Raytheon Signetics	5474 9N74 DM5474 5474 S5474	SN55107	AMD Fairchild Motorola National Raytheon	SN55107B 55107 MC55107 DS55107 RM55107 55107	SN72310	AMD Intersil	LM310 LM310		see page 661 Signetics Silicon G Teledyne S	SG747 747	
SN5475	Fairchild Fairchild National Signetics	5475 9375 DM5475 S5475	SN55108	AMD Fairchild Motorola National Raytheon	SN55108B 55108 MC55108 DS55108 RM55108 55108	SN72311	AMD Harris Intersil Raytheon RCA	LM311 HA-2311 LM311 LM311 LM311 CA311	SN72748	AMD Fairchild Intersil Motorola RCA Signetics Silicon G Teledyne S	748 748 748 MC1748 RC748 CA748 μA748 SG748 748	
SN5476	Fairchild Fairchild Motorola National Signetics	5476 9N76 MC5476 DM5476 S5476	SN55109	AMD Fairchild National Raytheon	SN55109 55109 DS55109 RM55109		see page 661 Signetics Teledyne S	LM311 LM311		SN72777	Intersil	777
SN5477	Fairchild Fairchild Signetics	5477 9377 S5477	SN55110	AMD Fairchild National Raytheon	SN55110 55110 DS55110 RM55110	SN72514	Raytheon	RC1414		SN74H00	Fairchild Fairchild ITT Motorola National Raytheon Signetics	74H00 9H00 ITT74H00 MC74H00 DM74H00 74H00 N74H00
SN5480	Fairchild Fairchild Signetics	5480 9380 S5480	SN55114	ITT	ITT9614	SN72555	AMD Intersil Lithic Sys Raytheon RCA	NE555 NE555 LS555 RC555 CA555				
† SN5481	Fairchild Raytheon TI	93407 5481 SN5481A	SN55115	ITT	ITT9615		see page 661 Teledyne S	555				
SN5482	Fairchild Fairchild	5482 9382	SN55182	National	DS7820	SN72558	Fairchild Harris Motorola National PMI Raytheon RCA	1458 HA-2655 MC1458 LM1458 SSS1458 RC1458 RC4558	SN74H01	Fairchild Fairchild ITT Motorola National Raytheon Signetics	74H01 9H01 ITT74H01 MC74H01 DM74H01 74H01 N74H01	
† SN5483	Fairchild Fairchild National Raytheon Signetics TI	5483 9383 DM5483 5483 S5483 SN5483A	SN5520	ITT National	ITT5520 DS5520		Signetics Teledyne S	CA1458 MC1458 1458				
SN5485	National	DM5485	SN5521	National	DS5521	SN72702	Fairchild Motorola Raytheon Raytheon	702 MC1712 RC1458 RC4558	SN74H04	Fairchild Fairchild ITT Motorola National Raytheon Signetics	74H04 9H04 ITT74H04 MC74H04 DM74H04 74H04 N74H04	
SN5486	Fairchild Fairchild National Raytheon Signetics	5486 9N86 DM5486 5486 S5486	SN5522	National	DS5522		see page 651 Signetics Teledyne S	CA1458 MC1458 1458				
† SN5488	Fairchild Intersil MMI	93434 IM5600 5230	SN5524	National	DS5524	SN72709	Fairchild Motorola Raytheon	709 MC1709 RC709	SN74H05	Fairchild	74H05	
			SN5525	National	DS5525							
			SN55325	Raytheon	RM55325							
			SN55450	National Raytheon Silicon G	DS55450 RM55450 SG55450							
			SN55451	National Raytheon	DS55451 RM55451							
			SN55452	National	DS55452							

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Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
Texas Instruments (cont)			SN74H51	Signetics	N74H51	SN74LS02	Fairchild Signetics see page 304	74LS02 N74LS02	SN74LS156	Fairchild	74LS156
SN74H05	Fairchild ITT Motorola National Raytheon Signetics	9H05 ITT74H05 MC74H05 DM74H05 74H05 N74H05	SN74H52	Fairchild Fairchild Motorola National Signetics	74H52 9H52 MC74H52 DM74H52 N74H52	SN74LS03	Fairchild National Signetics see page 304	74LS03 DM74LS03 N74LS03	SN74LS157	AMD Fairchild Signetics see page 304	SN74LS157 74LS157 N74LS157
SN74H10	Fairchild Fairchild ITT Motorola National Raytheon Signetics	74H10 9H10 ITT74H10 MC74H10 DM74H10 74H10 N74H10	SN74H53	Fairchild Fairchild ITT Motorola National Signetics	74H53 9H53 ITT74H53 MC74H53 DM74H53 N74H53	SN74LS04	Fairchild National Signetics see page 304	74LS04 DM74LS04 N74LS04	SN74LS158	AMD Fairchild Signetics see page 304	SN74LS158 74LS158 N74LS158
SN74H101	Motorola Signetics	MC74H101 N74H101	SN74H54	Fairchild Fairchild ITT Motorola National Signetics	74H54 9H54 ITT74H54 MC74H54 DM74H54 N74H54	SN74LS05	Fairchild Signetics see page 304	54LS05 N74LS05	SN74LS160	AMD Fairchild Signetics see page 304	SN74LS160 74LS160 N74LS160
SN74H102	Motorola Signetics	MC74H102 N74H102	SN74H55	Fairchild Fairchild Motorola National Signetics	74H55 9H55 MC74H55 DM74H55 N74H55	SN74LS08	Fairchild Signetics see page 304	74LS08 N74LS08	SN74LS161	AMD Fairchild Signetics see page 304	SN74LS161 74LS161 N74LS161
SN74H103	National Signetics	DM74H103 N74H103	SN74H60	Fairchild Fairchild ITT Motorola National Signetics	74H60 9H60 ITT74H60 MC74H60 DM74H60 N74H60	SN74LS09	Fairchild Signetics see page 304	74LS09 N74LS09	SN74LS162	AMD Fairchild Signetics see page 304	SN74LS162 74LS162 N74LS162
SN74H106	Fairchild Fairchild National Signetics	74H106 9H106 DM74H106 N74H106	SN74H61	Fairchild Fairchild Motorola National Signetics	74H61 9H61 MC74H61 DM74H61 N74H61	SN74LS10	Fairchild National Signetics see page 304	74LS10 DM74LS10 N74LS10	SN74LS163	AMD Fairchild Signetics see page 304	SN74LS163 74LS163 N74LS163
SN74H108	Fairchild Fairchild Motorola National Signetics	74H108 9H108 MC74H108 DM74H108 N74H108	SN74H62	Fairchild Fairchild ITT Motorola National Signetics	74H62 9H62 ITT74H62 MC74H62 DM74H62 N74H62	SN74LS107	Signetics see page 304	N74LS107	SN74LS164	AMD Fairchild Signetics see page 304	SN74LS164 74LS164 N74LS164
SN74H11	Fairchild Fairchild ITT Motorola National Raytheon Signetics	74H11 9H11 ITT74H11 MC74H11 DM74H11 74H11 N74H11	SN74H71	Fairchild Fairchild Motorola National Signetics	74H71 9H71 MC74H71 DM74H71 N74H71	SN74LS109	Fairchild Signetics see page 304	74LS109 N74LS109	SN74LS170	Fairchild Signetics see page 304	74LS170 N74LS170
SN74H183	Fairchild Fairchild Hitachi	74H183 93H183 HD2563	SN74H72	Fairchild Fairchild ITT Motorola National Signetics	74H72 9H72 ITT74H72 MC74H72 DM74H72 N74H72	SN74LS11	Fairchild Signetics see page 304	74LS11 N74LS11	SN74LS174	AMD Fairchild Signetics see page 304	SN74LS174 74LS174 N74LS174
SN74H20	Fairchild Fairchild ITT Motorola National Raytheon Signetics	74H20 9H20 ITT74H20 MC74H20 DM74H20 74H20 N74H20	SN74H73	Fairchild Fairchild ITT Motorola National Signetics	74H73 9H73 ITT74H73 MC74H73 DM74H73 N74H73	SN74LS112	Fairchild Signetics see page 304	74LS112 N74LS112	SN74LS175	AMD Fairchild Signetics see page 304	SN74LS175 74LS175 N74LS175
SN74H21	Fairchild Fairchild ITT Motorola National Signetics	74H21 9H21 ITT74H21 MC74H21 DM74H21 N74H21	SN74H74	Fairchild Fairchild ITT Motorola National Signetics	74H74 9H74 ITT74H74 MC74H74 DM74H74 N74H74	SN74LS113	Fairchild Signetics see page 304	74LS113 N74LS113	SN74LS181	AMD Fairchild Signetics see page 304	SN74LS181 74LS181 N74LS181
SN74H22	Fairchild Fairchild Motorola National Raytheon Signetics	74H22 9H22 MC74H22 DM74H22 74H22 N74H22	SN74H76	Fairchild Fairchild ITT Motorola National Signetics	74H76 9H76 ITT74H76 MC74H76 DM74H76 N74H76	SN74LS114	Fairchild Signetics see page 304	74LS114 N74LS114	SN74LS190	AMD Fairchild Signetics see page 304	SN74LS190 74LS190 N74LS190
SN74H30	Fairchild Fairchild ITT Motorola National Signetics	74H30 9H30 ITT74H30 MC74H30 DM74H30 N74H30	SN74H77	Fairchild Fairchild ITT Motorola National Signetics	74H77 9H77 ITT74H77 MC74H77 DM74H77 N74H77	SN74LS115	Fairchild Signetics see page 304	74LS115 N74LS115	SN74LS191	AMD Fairchild Signetics see page 304	SN74LS191 74LS191 N74LS191
SN74H40	Fairchild Fairchild ITT Motorola National Raytheon Signetics	74H40 9H40 ITT74H40 MC74H40 DM74H40 74H40 N74H40	SN74H78	Fairchild Fairchild National	74H78 9H78 DM74H78	SN74LS12	National Signetics see page 304	DM74LS12 N74LS12	SN74LS192	AMD Fairchild Signetics see page 304	SN74LS192 74LS192 N74LS192
SN74H50	Fairchild Fairchild ITT Motorola National Signetics	74H50 9H50 ITT74H50 MC74H50 DM74H50 N74H50	SN74H87	Fairchild Fairchild Motorola	74H87 9H87 MC74H87	SN74LS123	AMD	SN74LS123	SN74LS193	AMD Fairchild Signetics see page 304	SN74LS193 74LS193 N74LS193
SN74H51	Fairchild Fairchild ITT Motorola National	74H51 9H51 ITT74H51 MC74H51 DM74H51	SN74LS00	Fairchild National Signetics see page 304	74LS00 DM74LS00 N74LS00	SN74LS125	Fairchild	74LS125	SN74LS194	AMD Fairchild Signetics see page 304	SN74LS194 74LS194 N74LS194
			SN74LS01	National Signetics see page 304	DM74LS01 N74LS01	SN74LS126	Fairchild	74LS126	SN74LS195	AMD Fairchild Signetics see page 304	SN74LS195 74LS195 N74LS195
						SN74LS127	AMD	SN74LS127	SN74LS196	Fairchild Signetics see page 304	74LS196 N74LS196
						SN74LS128	Fairchild	74LS128	SN74LS197	Fairchild Signetics see page 304	74LS197 N74LS197
						SN74LS129	Fairchild	74LS129	SN74LS200	Fairchild National Signetics see page 304	74LS200 DM74LS200 N74LS200
						SN74LS130	Fairchild	74LS130	SN74LS21	Fairchild Signetics see page 304	74LS21 N74LS21
						SN74LS131	Signetics	N74LS131	SN74LS155	Fairchild	74LS155

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The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device
Texas Instruments (cont)		SN74LS73	Fairchild Signetics see page 384	74LS73 N74LS73	SN74S11	Signetics	N74S11
SN74LS22	Fairchild National Signetics see page 384	SN74LS74	Fairchild Signetics see page 384	74LS74 N74LS74	SN74S112	Fairchild Fairchild National	74S112 9S112 DM74S112
SN74LS221	Signetics see page 384	SN74LS76	Signetics see page 384	74LS76 N74LS76	SN74S113	Fairchild Fairchild National	74S113 9S113 DM74S113
SN74LS251	AMD Fairchild Signetics see page 384	SN74LS78	Signetics see page 384	74LS78 N74LS78	SN74S114	Fairchild Fairchild National	74S114 9S114 DM74S114
SN74LS253	AMD Fairchild Signetics see page 384	SN74LS83A	Signetics see page 384	74LS83A N74LS83A	SN74S133	Fairchild	9S133
SN74LS257	AMD Fairchild	SN74LS86	Fairchild Signetics see page 384	74LS86 N74LS86	SN74S134	Fairchild	9S134
SN74LS258	AMD Fairchild Signetics see page 384	SN74LS90	Fairchild Signetics see page 384	74LS90 N74LS90	SN74S138	AMD	SN54S138
SN74LS259	Fairchild	SN74LS92	Fairchild Signetics see page 384	74LS92 N74LS92	SN74S139	AMD	SN74S139
SN74LS26	Fairchild Signetics see page 384	SN74LS93	Fairchild Signetics see page 384	74LS93 N74LS93	SN74S140	Fairchild Fairchild National	74S140 9S140 DM74S140
SN74LS260	Fairchild Signetics see page 384	SN74LS95B	Fairchild Signetics see page 384	74LS95 N74LS95B	SN74S15	National Signetics	DM74S15 N74S15
SN74LS261	Signetics see page 384	SN74LS96	Signetics see page 384	74LS96 N74LS96	SN74S151	AMD National Signetics	SN74S151 DM74S151 N74S151
SN74LS266	Fairchild Signetics see page 384	SN74L00	National	DM74L00	SN74S153	AMD Fairchild National Signetics	SN74S153 93S153 DM74S153 N74S153
SN74LS27	Fairchild Signetics	SN74L01	National	DM74L01	SN74S157	AMD Fairchild National Signetics	SN74S157 93S157 DM74S157 N74S157
SN74LS279	Fairchild	SN74L02	National	DM74L02	SN74S158	AMD Fairchild Signetics	SN74S158 93S158 N74S158
SN74LS28	Signetics see page 384	SN74L03	National	DM74L03	SN74S174	AMD Signetics	SN74S174 N74S174
SN74LS283	Fairchild Signetics see page 384	SN74L04	National	DM74L04	SN74S175	AMD Fairchild Signetics	SN74S175 93S175 N74S175
SN74LS290	Fairchild Signetics see page 384	SN74L10	National	DM74L10	SN74S181	AMD Fairchild Fairchild Signetics	SN74S181 74S181 93S41 N74S181
SN74LS293	Fairchild Signetics see page 384	SN74L123	National	DM74L123	SN74S188	AMD Harris see page 746	AM27S09 HM7602
SN74LS295A	Fairchild Signetics see page 384	SN74L154	National	DM74L154A	SN74S189	AMD AMD Fairchild	6330 N82S23 see page 804, 826, 828,
SN74LS298	Fairchild	SN74L157	National	DM74L157A	SN74S194	AMD AMD Fairchild Signetics	AM27S03 SN74S189 93405
SN74LS30	Fairchild National Signetics see page 384	SN74L164	National	DM74L164	SN74S194	AMD Fairchild Signetics	SN74S194 93S194 N74S194
SN74LS32	Fairchild Signetics see page 384	SN74L192	National	DM74L192	SN74S195	AMD Fairchild	SN74S195 93S00
SN74LS33	Signetics see page 384	SN74L193	National	DM74L193	SN74S196	Fairchild	82S90
SN74LS368	Fairchild Signetics	SN74L20	National	DM74L20	SN74S197	Fairchild	82S91
SN74LS37	Fairchild Signetics see page 384	SN74L30	National	DM74L30	SN74S20	Fairchild Fairchild National Signetics	74S20 9S20 DM74S20 N74S20
SN74LS38	Fairchild Signetics see page 384	SN74L42	National	DM74L42A	SN74S200	Fairchild Intersil MMI National Raytheon Signetics TI	93421 IM5523 6531 DM74S200 RC5340 N74S200 SN74S201
SN74LS40	Fairchild Signetics see page 384	SN74L51	National	DM74L51	SN74S201	MMI Signetics see page 804, 806, 815,	7401 9N01 HD2509 ITT ITT7401 Motorola MC7401 National DM7401 Raytheon 7401 Signetics N7401 SW SW7401 7401
SN74LS42	Fairchild Signetics see page 384	SN74L54	National	DM74L54	SN74S206	Fairchild Intersil MMI Raytheon Signetics	93411 IM5533 6205 RC5330 N82S17 see page 804, 806, 815, TI SN74S301
SN74LS54	Fairchild Signetics see page 384	SN74L55	National	DM74L55	SN74S22	Fairchild Fairchild	74S22 9S22
SN74LS54	Fairchild Signetics see page 384	SN74L71	National	DM74L71			
SN74LS670	Fairchild Signetics see page 384	SN74L72	National	DM74L72			
		SN74L73	National	DM74L73			
		SN74L74	National	DM74L74			
		SN74L75	National	DM74L75			
		SN74L78	National	DM74L78			
		SN74L85	National	DM74L85			
		SN74L86	National	DM74L86			
		SN74L90	National	DM74L90			
		SN74L91	National	DM74L91			
		SN74L93	National	DM74L93			
		SN74L95	National	DM74L95			
		SN74L98	National	DM74L98			
		SN74S00	Fairchild Fairchild National Signetics	74S00 9S00 DM74S00 N74S00			
		SN74S03	Fairchild Fairchild National Signetics	74S03 9S03 DM74S03 N74S03			
		SN74S04	Fairchild Fairchild National Signetics	74S04 9S04 DM74S04 N74S04			
		SN74S05	Fairchild Fairchild National Signetics	74S05 9S05 DM74S05 N74S05			
		SN74S10	National Signetics	DM74S10 N74S10			
		SN74S109	Fairchild	9S109			
		SN74S11	Fairchild National	9S11 DM74S11			
		SN74S22	Fairchild Fairchild	74S22 9S22			
		SN74S22	National Signetics	DM74S22 N74S22			
		SN74S251	AMD Signetics	SN74S25 N74S251			
		SN74S257	AMD Signetics	SN74S257 N74S257			
		SN74S258	AMD Fairchild Signetics	SN74S258 93S258 N74S258			
		SN74S270	Intersil MMI	IM5604 6205			
		SN74S287	Intel Intersil MMI National National Signetics	3621-1 see page 772, 773 IM5603 6301 DM74S287 7574 N82S129			
		SN74S288	MMI Signetics see page 804, 826, 828,	6331 N82S123			
		SN74S289	AMD Fairchild Signetics see page 804, 806, 814,	SN74S289 93404 N82S25			
		SN74S301	Signetics see page 804, 806, 815,	N74S301			
		SN74S370	MMI	6206			
		SN74S371	MMI	HE6236			
		SN74S387	Intel MMI National National Signetics	3601-1 see page 772, 773 6300 DM74S387 DM8573 N82S126 see page 804, 826, 835,			
		SN74S40	Fairchild Fairchild National Signetics	74S40 9S40 DM74S40 N74S40			
		SN74S64	Fairchild Fairchild National Signetics	74S64 9S64 DM74S64 N74S64			
		SN74S65	Fairchild Fairchild National Signetics	74S65 9S65 DM74S65 N74S65			
		SN74S74	Fairchild Fairchild National Signetics	74S74 9S74 DM74S74 N74S74			
		SN74S86	National	DM74S86			
		SN7400	Fairchild Fairchild Hitachi ITT Motorola National Raytheon Signetics Signetics SW TRW	7400 9N00 HD2503 ITT7400 MC7400 DM7400 7400 N7400 8889 SW7400 7400			
		SN7401	Fairchild Fairchild Hitachi ITT Motorola National Raytheon Signetics SW TRW	7401 9N01 HD2509 ITT7401 MC7401 DM7401 7401 Signetics N7401 SW SW7401 7401			
		SN7402	Fairchild Fairchild Hitachi ITT Motorola National Signetics	7402 9N02 HD2511 ITT7402 MCT402 DM7402 N7402			

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ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
Texas Instruments (cont)			SN74100	Signetics SW	N74100 SW74100	SN74145	Fairchild Hitachi ITT	93145 HD2555 ITT74145	SN74157	SW	SW74157
SN7402	SW TRW	SW7402 7402	1 SN74104	ITT SW	ITT74104 SW74104	TI	SN29000		SN74159	Raytheon	74159
SN7403	Fairchild Fairchild Hitachi ITT Motorola National Raytheon Signetics SW TRW	7403 9N03 HD2528 ITT7403 MC7403 DM7403 7403 N7403 SW7403 7403	1 SN74105	ITT SW TI	ITT74105 SW74105 SN29001	SN74107	AMD Fairchild Fairchild Hitachi ITT Motorola National Signetics SW	SN74107 74107 9N107 HD2530 ITT74107 MC74107 DM74107 N74107 SW74107	SN74150	Fairchild Fairchild Hitachi ITT Motorola National Raytheon Signetics SW TRW	74150 93150 HD2548 ITT74150 MC74150 DM74150 74150 N74150 SW74150 74150
SN7404	Fairchild Fairchild Hitachi ITT Motorola National Raytheon Signetics SW TRW	7404 9N04 HD2522 ITT7404 MC7404 DM7404 7404 N7404 SW7404 7404	SN74109	ITT ITT National Signetics	ITT74109 ITT9024 DM74109 N74109	SN74111	TRW	74111	SN74160	AMD Fairchild ITT Motorola National Raytheon Signetics TRW	SN74160 9310 ITT74160 MC74160 DM74160 74160 N74160 74160
SN7405	Fairchild Fairchild Hitachi ITT Motorola National Raytheon Signetics SW TRW	7405 9N05 HD2523 ITT7405 MC7405 DM7405 7405 N7405 8891 SW7405 7405	SN74112	Fairchild Fairchild ITT Motorola TRW	7412 9N12 ITT7412 MC7412 7412 7412	SN74121	Fairchild Fairchild Hitachi ITT Motorola National Signetics SW TRW	74121 9603 HD2543 ITT74121 MC74121 DM74121 N74121 SW74121 74121	1 SN74151	Fairchild Fairchild Hitachi ITT Motorola National Raytheon Signetics SW TI TRW	74151 93151 HD2549 ITT74151 MC74151 DM74151 74151 N74151 SW74151 SN74151A 74151
SN7406	Fairchild Fairchild ITT Motorola National Signetics SW TRW	7406 9N06 ITT7406 MC7406 DM7406 N7406 SW7406 7406	SN74122	ITT Motorola National Signetics Signetics SW	ITT74122 MC74122 DM74122 N74122 8T22 SW74122	SN74123	AMD AMD Hitachi ITT Motorola National Raytheon Signetics SW TRW	AM26123 SN74123 HD2561 ITT74123 MC74123 DM74123 74123 N74123 SW74123 74123	SN74152	Fairchild Fairchild Motorola Raytheon TRW	74152 93152 MC74152 74152 74152
SN7407	Fairchild Fairchild ITT Motorola National Signetics SW TRW	7407 9N07 ITT7407 MC7407 DM7407 N7407 SW7407 7407	SN74125	National National Signetics	DM8093 DM8094 N74125	SN74126	Signetics	N74126	SN74153	AMD Fairchild Fairchild Hitachi ITT Motorola National Raytheon Signetics SW TRW	SN74153 74153 93153 HD2564 ITT74153 MC74153 DM74153 74153 N74153 SW74153 74153
SN7408	Fairchild Fairchild Hitachi ITT Motorola National Raytheon Signetics SW TRW	7408 9N08 HD2550 ITT7408 MC7408 DM7408 7408 N7408 SW7408 7408	SN74129	National	DM74193	SN7413	Fairchild Fairchild Hitachi ITT National Signetics SW TRW	7413 9N13 HD2545 ITT7413 DM7413 N7413 SW7413 7413	SN74154	AMD Fairchild Hitachi ITT Motorola National Raytheon Signetics SW TRW	SN74154 9311 HD2580 ITT74154 MC74154 DM74154 74154 N74154 SW74154 74154
SN7409	Fairchild Fairchild Hitachi ITT Motorola National Raytheon Signetics SW TRW	7409 9N09 HD2551 ITT7409 MC7409 DM7409 7409 N7409 SW7409 7409	SN74132	National	DM74132	SN74136	Motorola Raytheon TRW	MC74136 74136 74136	SN74155	Fairchild ITT Motorola National Raytheon Signetics SW TRW	93155 ITT74155 MC74155 DM74155 74155 N74155 SW74155 74155
SN7410	Fairchild Fairchild Hitachi ITT Motorola National Raytheon Signetics SW TRW	7410 9N10 HD2507 ITT7410 MC7410 DM7410 7410 N7410 8879 SW7410 7410	SN74141	Fairchild Fairchild Hitachi ITT National National Signetics Signetics SW	74141 93141 HD2558 ITT74141 DM74141 DM7441 N74141 N7441 SW74141	SN74145	Fairchild	74145	SN74170	Fairchild Hitachi National Raytheon Signetics	74170 HD2540 DM74170 74170 N74170
SN74100	Motorola	MC74100							SN74172	Signetics	N74172
									SN74173	National	DM8551
									SN74174	AMD Fairchild ITT National	SN74174 93174 ITT74174 DM74174

1 Discontinued

The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device	Manufacturer Device	Replacement Source	Device
Texas Instruments (cont)			SN74190	ITT	ITT74190	SN74200	Fairchild	93421	SN7438	ITT	ITT7438
SN74174	Raytheon	74174	Motorola	MC74190	National	DM74190	Intersil	IM5523	Motorola	MC7438	Motorola
	Signetics	N74174	National	DM74190	Raytheon	74190	MMI	6531	National	DM7438	National
SN74175	AMD	SN74175	Raytheon	74190	Signetics	N74190	National	DM74200	Signetics	N7438	Signetics
	Fairchild	93175	Signetics	N74190			Raytheon	RC5340	SW	SN7438	SW
	ITT	ITT74175					Signetics	N82506	TRW	7438	TRW
	National	DM74175	SN74191	Fairchild	74191	SN74206	Intersil	IM5533	SN74387	Fairchild	93416
	Raytheon	74175	Fairchild	93191	ITT	ITT74191	MMI	6530	SN7440	Fairchild	7440
	Signetics	N74175	ITT	ITT74191	Motorola	MC74191	Raytheon	RC5330	Fairchild	9N40	Hitachi
SN74176	Fairchild	74176	Motorola	MC74191	National	DM74191	TI	SN74S301	Hitachi	HD2501	ITT
	Fairchild	82S90	Raytheon	74191	Signetics	N74191			ITT	ITT7440	Motorola
	Fairchild	93176					SN7422	Raytheon	7422	SN74400	National
	Motorola	MC74176	SN74192	AMD	SN74192	SN7423	Fairchild	7423	Fairchild	7423	SN74400
	National	DM74176	AMD	9360	AMD	9360	Fairchild	9N23	Hitachi	HD2501	National
	National	DM8280	Fairchild	74192	Fairchild	9360	Motorola	MC7423	Motorola	MC7440	Signetics
	Signetics	N8280	Fairchild	9360	ITT	ITT74192	National	DM7423	National	N7440	Signetics
SN74177	Fairchild	74177	ITT	ITT74192	Motorola	MC74192	SW	SW7423	SW	SW7440	TRW
	Fairchild	82S91	Motorola	MC74192	National	DM74192			† SN7441A	National	DM7441A
	Fairchild	93177	National	DM74192	National	DM8560	Fairchild	7425	TI	SN74141	
	Motorola	MC74177	National	DM8560	Raytheon	74192	Motorola	MC7425	† SN7442	Fairchild	7442
	National	DM74177	Raytheon	74192	Signetics	N74192	National	DM7425	Fairchild	9352	Hitachi
	National	DM8281	SW	SN74192	SW	SN74192	SW	SW7425	Hitachi	HD2536	ITT
	Signetics	N8281							ITT	ITT7442	Motorola
SN74178	Fairchild	74178	SN74193	AMD	SN74193	SN74251	National	DM8121	Motorola	MC7442	National
	Fairchild	82S70	AMD	9366	AMD	9366	Fairchild	7426	Fairchild	9N40	Raytheon
	Fairchild	93178	Fairchild	74193	Fairchild	9366	Fairchild	9N26	National	DM7442	Raytheon
	Motorola	MC74178	Fairchild	9366	ITT	ITT74193	Hitachi	HD2560	Raytheon	7442	Signetics
	Signetics	N8270	ITT	ITT74193	Motorola	MC74193	ITT	ITT7426	Signetics	N7442	SW
SN74179	Fairchild	74179	Motorola	MC74193	National	DM8563	Motorola	MC7426	TI	SN7442A	
	Fairchild	82S72	National	DM8563	Raytheon	74193	Signetics	N7426	SN74425	National	DM8083
	Fairchild	93179	Raytheon	74193	Signetics	N74193	SW	SW7426	SN74426	National	DM8094
	Motorola	MC74179	SW	SN74193	SW	SN74193	TRW	7426			
	Signetics	N8271							† SN7443	Fairchild	7443
SN74180	Fairchild	74180	SN74194	AMD	SN74194	SN7427	Fairchild	7427	Fairchild	9353	Hitachi
	Fairchild	93180	ITT	ITT74194	ITT	ITT74194	Fairchild	9N27	Hitachi	HD2537	ITT
	Hitachi	HD2525	Motorola	MC74194	Motorola	MC74194	Motorola	MC7427	ITT	ITT7443	Motorola
	ITT	ITT74180	National	DM74194	National	DM74194	National	DM7427	Motorola	MC7443	Raytheon
	Motorola	MC74180	Raytheon	74194	Raytheon	74194	SW	SW7427	Raytheon	7443	Signetics
	National	DM74180	Signetics	N74194	Signetics	N74194			Signetics	N7443	SW
	Raytheon	74180					SN74270	MMI	6205	SN7443A	TI
	Signetics	N74180	SN74195	AMD	SN74195	SN7428	ITT	ITT7428	SN7428	Raytheon	74283
	SW	SN74180	Fairchild	9300	Fairchild	9300	Raytheon	74283	SN74283	Raytheon	74283
	TRW	74180	ITT	ITT74195	ITT	ITT9300	National	DM8875A	† SN7444	Fairchild	7444
SN74181	AMD	SN74181	ITT	ITT9300	ITT	ITT9300	National	DM8875B	Fairchild	9354	Hitachi
	AMD	9341	Motorola	MC74195	Motorola	MC74195	National	DM8875B	Hitachi	HD2538	ITT
	Fairchild	74181	National	DM8300	National	DM8300	Fairchild	93426	ITT	ITT7444	Motorola
	Fairchild	9341	Raytheon	74195	Raytheon	74195	TRW	74290	Motorola	MC7444	Raytheon
	Hitachi	HD2547	Signetics	N74195	Signetics	N74195	SN74290	74290	Raytheon	7444	Signetics
	ITT	ITT74181					SN74293	74293	Signetics	N7444	SW
	Motorola	MC74181	SN74196	Fairchild	74196	SN7429301	ITT	ITT9301	SW	SN7444A	TI
	National	DM74181	Fairchild	82S90	Fairchild	82S90	Fairchild	7430	TI	SN7444A	
	Raytheon	74181	Fairchild	93196	Fairchild	93196	Fairchild	9N30	SN7445	Fairchild	7445
	Signetics	N74181	Motorola	MC74196	Motorola	MC74196	Hitachi	HD2508	Fairchild	9345	Hitachi
	SW	SN74181	National	DM74196	National	DM74196	ITT	ITT7430	Hitachi	HD2531	ITT
SN74182	AMD	SN74182	Signetics	N8290	Signetics	N8290	Motorola	MC7430	ITT	ITT7445	Motorola
	AMD	9342					National	DM7430	National	DM7445	National
	Fairchild	74182	SN74197	Fairchild	74197	SN74285	Signetics	N7430	National	DM7445	Raytheon
	Fairchild	9342	Fairchild	82S91	Fairchild	93197	SW	SW7430	Raytheon	7445	Signetics
	Hitachi	HD2562	Fairchild	93197	Motorola	MC74197	TRW	7430	Signetics	N7445	SW
	ITT	ITT74182	Motorola	MC74197	National	DM74197	SN7432	Fairchild	7432	SN7445	TRW
	Motorola	MC74182	Signetics	N8291	Signetics	N8291	Fairchild	9N32	7445		
	National	DM74182					ITT	ITT7432	† SN7446	Fairchild	7446
	Raytheon	74182	SN74198	Fairchild	74198	SN7433	National	DM7432	Fairchild	9357	Hitachi
	Signetics	N74182	Fairchild	93198	Fairchild	93198	Signetics	N7432	Hitachi	HD2553	ITT
	SW	SN74182	Motorola	MC74198	National	DM74198	SW	SW7432	ITT	ITT7446	Motorola
SN74184	National	DM74184	National	DM74198	Raytheon	74198	ITT	ITT7433	Motorola	MC7446	National
SN74185A	National	DM74185A	Raytheon	74198	Signetics	N74198	SN74365	National	National	DM7446	Signetics
SN74186	Harris	HPROM-0512	SN74199	Fairchild	93199	SN74367	National	DM8097	Signetics	N7446	SW
SN74187	Fairchild	93406	Motorola	MC74199	National	DM74199	SN74368	National	TI	SN7446A	
	Intersil	IM5603	Raytheon	74199	Raytheon	74199	SN7437	Fairchild	7437	† SN7447	Fairchild
	MMI	6200	Signetics	N74199	Signetics	N74199	Fairchild	9N37	Hitachi	HD2532	ITT
	National	DM74187					Hitachi	HD2552	ITT	ITT7447	Motorola
	Signetics	N82S226	SN7420	Fairchild	7420	SN74370	ITT	ITT7437	National	DM7447	National
SN74188	Harris	HPROM-8256	Fairchild	9N20	Fairchild	9N20	Motorola	MC7437	Signetics	N7447	Signetics
	Intersil	IM5600	Hitachi	HD2504	Hitachi	HD2504	National	DM7437	SW	SN7447A	TI
	Signetics	N82S23	ITT	ITT7420	ITT	ITT7420	Signetics	N7437	TI	SN7447A	
	see page 804, 826, 828,		Motorola	MC7420	Motorola	MC7420	SW	SW7437			
	TI	SN74188A	National	DM7420	National	DM7420	TRW	7437	SN7448	Fairchild	7448
SN74188A	MMI	6330	Raytheon	7420	Signetics	N7420	SN74370	MMI	Fairchild	9358	ITT
	National	DM8577	Signetics	N8819	Signetics	N8819	SN7438	Fairchild	ITT	ITT7448	Motorola
SN74190	Fairchild	74190	SW	SN7420	SW	SN7420	Fairchild	9N38	Motorola	MC7448	National
	Fairchild	93190	TRW	7420	TRW	7420	Hitachi	HD2544	National	DM7448	Signetics
									Signetics	N7448	

† Discontinued

ALTERNATE SOURCE DIRECTORY

Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device	Manufacturer Device	Replacement Source Device
Texas Instruments (cont)							
SN7448	Signetics N8T04 Signetics N8T05 SW SW7448	SN7474	Raytheon 7474 Signetics N7474 SW SW7474 TRW N7474	SN7489	Hitachi HM2502 Intersil IM5501 National DM7489 Raytheon 7489 Signetics N02S25 see page 804, 806, 814, TRW 7489	SN75108	ITT ITT75108 Motorola MC75108 National DS75108 Raytheon RC75108
SN7449	Fairchild 7449 Fairchild 9359 Motorola MC7449	SN7475	Fairchild 7475 Fairchild 9375 Hitachi HD2517 ITT ITT7475 Motorola MC7475 National DM7475 Signetics N7475 SW SW7475 TRW 7475	† SN7490	Fairchild 7490 Fairchild 9390 Hitachi HD2519 ITT ITT7490 Motorola MCM4023 Motorola MC7490 National DM7490 Signetics N7490 SW SW7490 TI SN7490A TRW 7490	SN75109	AMD SN75109 Fairchild 75109 ITT ITT75109 Motorola MC75109 National DS75109 Raytheon RC75109
SN7450	Fairchild 7450 Fairchild 9N50 Hitachi HD2506 ITT ITT7450 Motorola MC7450 National DM7450 Signetics N7450 Signetics N8859 SW SW7450 TRW 7450	SN7476	Fairchild 7476 Fairchild 9N76 Hitachi HD2516 ITT ITT7476 Motorola MC7476 National DM7476 Signetics N7476 SW SW7476 TRW 7476	† SN7491	Fairchild 7491 Fairchild 9391 Hitachi HD2524 ITT ITT7491 Motorola MC7491 National DM7491 Signetics N7491 SW SW7491 TI SN7491A	SN75110	AMD SN75110 Fairchild 75110 ITT ITT75110 Motorola MC75110 National DS75110 Raytheon RC75110
SN7451	Fairchild 7451 Fairchild 9N51 Hitachi HD2505 ITT ITT7451 Motorola MC7451 National DM7451 Signetics N7451 SW SW7451 TRW 7451	† SN7477	Fairchild 7477 Fairchild 9377 Motorola MC7477	† SN7492	Fairchild 7492 Fairchild 9392 Hitachi HD2521 ITT ITT7492 Motorola MC7492 National DM7492 Signetics N7492 SW SW7492A TRW 7492	SN75114	Fairchild 9614
SN7453	Fairchild 7453 Fairchild 9N53 Hitachi HD2512 ITT ITT7453 Motorola MC7453 National DM7453 Signetics N7453 SW SW7453 TRW 7453	† SN7480	Fairchild 7480 Fairchild 9380 ITT ITT7480 Motorola MC7480 Signetics N7480 SW SW7480	† SN7493	Fairchild 7493 Fairchild 9392 Hitachi HD2520 ITT ITT7493 Motorola MC7493 National DM7493 Signetics N7493 SW SW7493A TI SN7493A TRW 7493	SN75115	Fairchild 9615
SN7454	Fairchild 7454 Fairchild 9N54 Hitachi HD2514 ITT ITT7454 Motorola MC7454 National DM7454 Signetics N7454 SW SW7454 TRW 7454	† SN7481	Fairchild 93407 Hitachi HM2501 ITT ITT7481 Motorola MC4004 Raytheon 7481 TI SN7481A TRW 7481	† SN7494	Fairchild 7494 Fairchild 9394 Hitachi HD2533 ITT ITT7494 Motorola MC7494 Signetics N7494 SW SW7494	SN75121	National DS75121
SN7460	Fairchild 7460 Fairchild 9N60 Hitachi HD2502 ITT ITT7460 Motorola MC7460 National DM7460 Signetics N7460 SW SW7460 TRW 7460	† SN7483	Fairchild 7483 Fairchild 9383 Hitachi HD2535 ITT ITT7483 Motorola MC7483 National DM7483 Raytheon 7483 Signetics N7483 TI SN7483A	† SN7495	Fairchild 7495 Fairchild 9395 Hitachi HD2534 ITT ITT7495 Motorola MC7495 National DM7495 Signetics N7495 SW SW7495 TI SN7495A	SN75122	National DS75122
SN7470	Fairchild 7470 Fairchild 9N70 Hitachi HD2539 ITT ITT7470 Motorola MC7470 National DM7470 Signetics N7470	† SN7484	ITT ITT7484 Motorola MC7484 TI SN7484A	SN75107	AMD SN75107B Fairchild 75107 ITT ITT75107 Motorola MC75107 National DS75107 Raytheon RC75107	SN75123	National DS75123
SN7472	Fairchild 7472 Fairchild 9N72 Hitachi HD2529 ITT ITT7472 Motorola MC7472 National DM7472 Signetics N7472 SW SW7472 TRW 7472	SN7485	Motorola MC7485 National DM7485 Signetics N7485 SW SW7485 TRW 7485	SN75108	AMD SN75108B Fairchild 75108	SN75124	Fairchild 9616
SN7473	Fairchild 7473 Fairchild 9N73 Hitachi HD2515 ITT ITT7473 National DM7473 Signetics N7473 SW SW7473	SN7486	Fairchild 7486 Fairchild 9N86 Hitachi HD2526 ITT ITT7486 Motorola MC7486 National DM7486 Raytheon 7486 Signetics N7486 SW SW7486 TRW 7486	SN75111	Fairchild 75111 ITT ITT75111 Motorola MC75111 National DS75111 Raytheon RC75111	SN75125	Fairchild 9617
SN7474	Fairchild 7474 Fairchild 9N74 Hitachi HD2510 ITT ITT7474 Motorola MC7474 National DM7474	† SN7488	Fairchild 93434 Intersil IM5600 ITT ITT7488 MMI 6230 Motorola MCM4002 National DM7488 TI SN7488A	SN75112	Fairchild 75112 ITT ITT75112 Motorola MC75112 National DS75112 Raytheon RC75112	SN75126	ITT ITT9311 National DS75154 Raytheon RC75154
		SN7489	AMD SN7489 Fairchild 7489	SN75113	Fairchild 75113 ITT ITT75113 Motorola MC75113 National DS75113 Raytheon RC75113	SN75127	AMD 8820 National DS8820 Signetics DM8820
				SN75114	Fairchild 9614	SN75128	AMD 8830 National DS8830 Signetics DM8830
				SN75115	Fairchild 9615	SN75188	ITT ITT1448 Signetics MC1488
				SN75116	Fairchild 9616	SN75189	ITT ITT1449 Signetics MC1489
				SN75117	Fairchild 9617	SN7520	ITT ITT7520 Motorola MC7520 National DS7520 Signetics 7520 Silicon G SG7520
				SN75118	Fairchild 9618	SN75207	National DS75207
				SN75119	Fairchild 9619	SN7521	ITT ITT7521 Motorola MC7521 National DS7521 Signetics 7521 Silicon G SG7521
				SN75120	Fairchild 9620	SN7522	ITT ITT7522 Motorola MC7522 National DS7522 Signetics 7522 Silicon G SG7522
				SN75121	Fairchild 9621	SN7523	ITT ITT7523 Motorola MC7523 National DS7523 Signetics 7523 Silicon G SG7523
				SN75122	Fairchild 9622	SN75234	Fairchild 75234 ITT ITT75234 Motorola MC75234
				SN75123	Fairchild 9623	SN75235	Fairchild 75235 ITT ITT75235 Motorola MC75235
				SN75124	Fairchild 9624	SN75236	ITT ITT75236
				SN75125	Fairchild 9625	SN75238	Motorola MC75238
				SN75126	Fairchild 9626	SN75239	Motorola MC75239
				SN75127	Fairchild 9627	SN7524	Fairchild 7524 ITT ITT7524 Motorola MC7524 National DS7524 Signetics 7524 Silicon G SG7524
				SN75128	Fairchild 9628	SN7525	Fairchild 7525 ITT ITT7525 Motorola MC7525 National DS7525 Silicon G SG7525
				SN75129	Fairchild 9629	SN7528	ITT ITT7528

† Discontinued

The manufacturers report their devices can be used as direct replacements. Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Replacement Device	Manufacturer Device	Replacement Source	Replacement Device	Manufacturer Device	Replacement Source	Replacement Device	Manufacturer Device	Replacement Source	Replacement Device
Texas Instruments (cont)			SN75463	ITT National Teledyne S	ITT75463 DS75463 75463	TF4010	Motorola	MC14010	TMS8080	Intel	8080 see page 958
SN7528	Motorola National Silicon G	MC7528 DS7528 SG7528	SN75464	Fairchild ITT National Teledyne S	75464 ITT75464 DS75464 75464	TF4011	Motorola	MC14011	TM54060	Intel	2107B see page 760, 765
SN7529	ITT Motorola National Silicon G	ITT7529 MC7529 DS7529 SG7529	SN75491	Motorola National	MC75491 DS75491	TF4012	Motorola	MC14012	TP4000	Motorola	MC14000
SN75324	National Raytheon	DS75324 RC75324	SN75492	Motorola National	MC75492 DS75492	TF4013	Motorola	MC14013	TP4001	Motorola	MC14001
SN75325	ITT Motorola National Raytheon	ITT75325 MC75325 DS75325 RC75325	SN75493	National	DS75493	TF4023	Motorola	MC14023	TP4002	Motorola	MC14002
SN75326	ITT	ITT75326	SN75494	National	DS75494	TF4025	Motorola	MC14025	TP4007	Motorola	MC14007
SN75327	ITT	ITT75327	SN76104	Fairchild Motorola Sprague	732 MC1304 ULN-2120	TF4027	Motorola	MC14027	TP4009	Motorola	MC14009
SN7534	ITT National Silicon G	ITT7534 DS7534 SG7534	SN76105	Motorola Sprague	MC1305 ULN-2122	TMS1101	Intersil Signetics	IM7501 1101	TP4010	Motorola	MC14010
SN7535	ITT National Silicon G	ITT7535 DS7535 SG7535	SN76107	Fairchild Motorola	767 MC1370	TMS1103	Signetics	1103	TP4011	Motorola	MC14011
SN75361	ITT National	ITT75361 DS75361	SN76111	Sprague	ULN-2121	† TMS2102	Intersil	IM7552	TP4012	Motorola	MC14012
SN75365	ITT National	ITT75365 DS75365	SN76113	Sprague	ULN-2128	† TMS2300	AMI	S8773	TP4013	Motorola	MC14013
SN75370	ITT	ITT75370	SN76115	RCA Sprague	CA1310 ULN-2210	† TMS2500	AMI	S8773	TP4023	Motorola	MC14023
SN7538	Silicon G	SG7538	SN76131	Fairchild	739	† TMS2600	AMI National Nitron	S8773 MM4230 MM5230 NCM1110	TP4025	Motorola	MC14025
SN7539	Silicon G	SG7539	SN76149	Fairchild	749	† TMS2800	National	MM4210	TP4027	Motorola	MC14027
SN75450	Hitachi ITT Motorola National Raytheon Signetics Silicon G Teledyne S	HD2574 ITT75450 MC75450 DS75450 RC75450 75450 SG75450 75450	SN76177	Fairchild Sprague	705 ULN-2277	† TMS2900	AMI	S8773	RM1701	Intel	2107 TMS4030 TMS4060
SN75451	Hitachi ITT Motorola National Raytheon Signetics Teledyne S	HD2575 ITT75451 MC75451 DS75451 RC75451 75451 75451	SN76242	Fairchild Motorola RCA Sprague	780 MC1370 CA3070 ULN-2124	TMS3112	Fairchild	3348	TR1402A	GI	AY5-1013
SN75452	Fairchild Hitachi ITT Motorola National Raytheon Signetics Teledyne S	75452 HD2577 ITT75452 MC75452 DS75452 RC75452 75452 75452	SN76243	Fairchild Motorola Sprague	781 MC1371 ULN-2127	TMS3113	AMI	S2181A	TR1602	AMI	S1883 see page 533
SN75453	Fairchild Hitachi ITT Motorola National Raytheon Signetics Teledyne S	75453 HD2578 ITT75453 MC75453 DS75453 RC75453 75453 75453	SN76246	Fairchild Motorola Sprague	746 MC1328 CA3071 ULN-2114	TMS3114	AMD AMI	3114 S2181A			
SN75454	Fairchild Hitachi ITT Motorola National Raytheon Signetics Teledyne S	75454 HD2579 ITT75454 MC75454 DS75454 RC75454 75454 75454	SN76266	Fairchild RCA	3066 CA3066	TMS3120	Signetics	2532			
SN75460	Fairchild ITT National Silicon G Teledyne S	75460 ITT75460 DS75460 SG75460 75460	SN76267	Fairchild RCA Sprague	3067 CA3067 ULN-2267	TMS3121	Fairchild	3342			
SN75461	Fairchild ITT National Teledyne S	75461 ITT75461 DS75461 75461	SN76530	Motorola	MC1330	TMS3122	Signetics	2518			
SN75462	Fairchild ITT National Teledyne S	75462 ITT75462 LM75462 75462	SN76564	Fairchild Motorola RCA Sprague	3064 MC1364 CA3064 ULN-2264	TMS3126	National	MM4060			
SN75463	Fairchild	75463	SN76600	Motorola	MC1350	TMS3127	National	MM4060			
			SN76603	Fairchild	703	TMS3128	National	MM4060			
			SN76630	Fairchild	786	TMS3129	National	MM4060			
			SN76642	Motorola Sprague	MC1357 ULN-2113	TMS3130	National	MM4060			
			SN76643	Fairchild Signetics Sprague	2136 ULN2111 ULN-2111	TMS3131	National	MM4060			
			SN76650	Motorola RCA	MC1352 CA1352	TMS3132	National	MM4060			
			SN76651	Motorola	MC1351	TMS3133	Fairchild	3355			
			SN76653	Motorola	MC1353	† TMS3304	Motorola	MC1141			
			SN76665	Fairchild Motorola RCA Sprague	3065 MC1353 CA3065 ULN-2165	TMS3409	Intersil	IM7780			
			SN76666	Fairchild	3066	TMS3412	AMI Signetics Signetics	S1685 S2502 S2532			
			SN76675	Fairchild Motorola Sprague	3075 MC1375 ULN-2129	TMS3414	AMI	S1685			
			SN76676	Fairchild	3076	TMS3417	Fairchild	3342			
			S54LS192	AMD Fairchild Raytheon	SN54LS192 54LS192 54LS192 see page 282	TMS4000	GI	RO5-8192			
			TF4000	Motorola	MC14000	TMS4024	Signetics	2535			
			TF4001	Motorola	MC14001	TMS4030	Intel Western	2107A RM1701			
			TF4002	Motorola	MC14002	TMS4033	Signetics	2602-1 see page 790			
			TF4007	Motorola	MC14007	TMS4034	Signetics	2602-2 see page 790			
			TF4009	Motorola	MC14009	TMS4050	MMI	2150			
						TMS4060	AMI	S4021 see page 722			
							EA	EA4060			
							Intel	2107			
							Signetics	2604 see page 793			
							Western	RM1701			
							Nortec	6002			
							Western	RM1701			
							Motorola	MCM1130			
							Nitron	NCM1130			
							Motorola	MCM1131/32			
							Motorola	MCM1132			
							Nitron	NCM1140			
							Fairchild	MCM1140			
							Motorola	MCM1141			
							EA	EA4800			
							EA	EA4900			
							GI	AY5-3600			
							AMI	S1757 see page 532			
							GI	AY5-1013			
							AMI	S1883 see page 533			
							AMS	AMS7001			
							Motorola	MCM7001			
							Nitron	7001			
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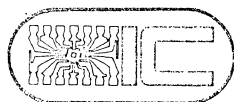
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Burr-Brown International S.A., Tel: 954 3558

Intl Germany
Leinfelden Bei Stuttgart
Burr-Brown International GMBH, Tel: (711) 75 10 21

Intl Greece, Athens
Hellenici Scientific Representations Ltd., Tel: 7705 960

Intl Holland, Breda
Datron B.V., Tel: 076-141152

Intl India, Bombay
Vibronics Private Limited, Tel: 551973

Intl Israel, Tel-Aviv
Racom Electronics Co., Ltd., Tel: 443126

Intl Italy, Milano
Metroelectronica, Tel: 546 26 41

Intl Japan
Chiyoda-ku, Tokyo
Kyokuto Boeki Kaisha Ltd., Tel: 03 244 3784 8

Intl New Zealand, Auckland
W. & K. McLean Ltd., Tel: 587 037

Intl Norway, Oslo
Bugø Riso A/S, Tel: 23 2580

Intl Pakistan, Karachi
I & S Corporation, Tel: 223322

Intl Portugal, Lisbon
Tleectra, Tel: 686072

Intl So. Africa
Johannesburg
David Pollock (Pty.) Ltd., Tel: 724 8274

Intl Spain, Madrid
Distesa, Tel: 457 28 00

Intl Sweden, Vallingby
Teletinstrument AB, Tel: 08 38 03 70

Intl Switzerland, Zurich
Telemeter Electronic AG, Tel: 01 25 78 72

Intl Turkey, Istanbul
Telekom, Tel: 49 40 40

Cermetek, Inc.

Cermetek, Inc.
660 National Avenue
Mountain View, Ca. 94043
(415) 969-9433

Sales Offices and Representatives

Ariz Phoenix
Chaparral-Dorton, (602) 263-0414

Cal Marina del Rey
Relcom, (213) 822-1187

Col Boulder
R.G. Enterprises, (303) 447-9211

Fla Ft. Lauderdale
Reynolds & Associates, (305) 581-6611, (305) 565-2369
Hollywood
Reynolds & Associates, (305) 987-6720
Satellite Beach
Reynolds & Associates, (305) 773-4700
St. Petersburg
Reynolds & Associates, (813) 360-1484

Ga Atlanta
Reynolds & Associates, (404) 252-5360, (205) 536-1941

Ill Chicago
Reynolds & Associates, (312) 647-7755

Mass Burlington
Contact Sales, Inc., (617) 273-1520

Md Florissant
Mid West Marketing, (301) 922-2092
Randallstown
C.L. Malinow & Co., (301) 922-2092

NJ Cherry Hill
J.M. Barrett Associates, Inc., (609) 429-1551
Clifton
Compar New York, Inc., (201) 546-3660

NM Albuquerque
Tritronix/Albuquerque, (505) 265-5400

Oh Dayton
Compass Associates, (513) 252-9939

Tx Houston
Data Aid Associates, (713) 862-6685

Can Richmond Hill, Ontario
Ferritronics Ltd., (416) 889-7313

Intl Israel, Tel Aviv
STG International, (03) 534598 523648 523658 53115

Collins Radio

Collins Radio Group
4311 Jamboree Road
Newport Beach, California 92663
(714) 833-4661
TWX: (910) 959-1705

Specific product information:

Don Gibson ext. 4637

Application engineering:

Don Gibson ext. 4637
Charlene Root ext. 4630
Mike Kilgore ext. 4590
Mike Kilgore ext. 4590
Charlene Root ext. 4630

Sales Offices & Representatives

Ala Huntsville
Gentry Associates, Inc., (205) 534-9771

Ariz Scottsdale
Williams Associates, (602) 947-4297

Cal Burlingame
Jack Logan Associates, (415) 697-6377
Garden Grove
Impact Electronics, Inc., (714) 893-8551

Collins Radio (cont)

Colo Denver
Williams Associates, (303) 373-4730

Fla Orlando
Gentry Associates, Inc., (305) 894-4401

Ga Atlanta
Gentry Associates, Inc., (404) 448-2365

Ind Ft. Wayne
Walter W. Bierberich, Inc., (219) 432-2537

New Albany
Walter W. Bierberich, Inc., (812) 945-3187

Iowa Cedar Rapids
Engineering Services Co., (913) 649-4000

Mass Lexington
Circuit Sales, Inc., (617) 861-0567

Mich Grosse Pointe Park
Greiner Associates, Inc., (313) 499-0188

Mo St. Louis
Engineering Services Co., (314) 977-1515

NC Burlington
Gentry Associates, Inc.98 (919) 227-3639

NM Albuquerque
Williams Associates, (602) 947-4297

NY Pittsford
T² Electronics Co., (716) 381-2551

Plainview
E.R.A., (516) 822-9890

Syracuse
T² Electronics Co., (315) 463-8592

Ohio Cleveland
Arthur H. BAIER Co., (216) 461-6161

Dayton
Arthur H. Bair CO., (513) 276-4128

Tex Dallas
J Clay Company, (214) 350-1281

Wash Redmond
Desco Northwest, (206) 455-9325

Wisc Milwaukee
J M Sales Company, (414) 546-0040

Can Toronto, Ontario
Norgay Enterprises, LTD., (416) 233-2930

Consumer Microcircuits of America

Consumer Microcircuits of America
114 E Simmons St.
Galesburg, Illinois 61401
(309) 342-5311

Datel Systems

Datel Systems
1020 Turnpike St.
Canton, Massachusetts 02021
(617) 828-8000
TWX: (710) 348-0135
Telex: 924461

Regional Offices
Santa Ana, Calif. (714) 835-2751
Sunnyvale, Calif. (408) 733-2424
Canton, Mass (617) 828-8000
Home office, Canton, Mass. (617) 828-8000

Ala Huntsville
Int'l Scientific Instruments, (205) 533-6880

Ariz Phoenix
Cleveland Enterprises, (602) 996-6130

Cal Los Angeles-Santa Ana
Western Regional Office (213) 933-72568 (714) 835-2751

Sunnyvale
NO. Calif Sales Office, (408) 733-2424

Fla Lighthouse Point
Saber Assoc., (305) 943-3076

Longwood
Saber Assoc., (305) 422-3686

St. Petersburg
Saber Assoc., (813) 441-1301

Haw Honolulu
Hawaii Data Systems, (808) 946-1533

Ill Chicago
Carter Electronics, Inc., (312) 585-5486

Ind Indianapolis
Carter Electronics, (317) 293-0696

Iowa Cedar Rapids
Technical Representatives, Inc., (319) 363-2489

Kan Olathe
Technical Representatives, (913) 782-1177

Mich Troy
George R. Peters, Assoc., (313) 362-1220

Minn Minneapolis
Carter Electronics, Inc., (612) 544-9393

Mo Hazelwood
Technical Representatives, Inc., (314) 731-5200

NC Raleigh
Saber Associates, (919) 834-3961

NJ Fort Lee
Technical Marketing Assoc., (201) 224-6911

NM Albuquerque
Cleveland Enterprises, (505) 345-2481

NY Liverpool
R. & D. Associates, Inc., (315) 622-2350

Ohio Cleveland
Instrumentation Systems, Inc., (216) 486-0782

Dayton
Instrumentation Systems, Inc., (513) 294-2838

Penn King of Prussia
Rivco, (215) 265-5211

Pittsburgh
Instrumentation Systems, Inc., (412) 243-1111

Tex Dallas
Evans-McDowell, (214) 238-7157

Houston
Evans-McDowell, (713) 783-2900

Va Arlington
J.H. Heffernan Co., (703)522-6666

Wash Seattle
Jon B. Jolly Inc, (206) 938-4166

Wisc Milwaukee
Carter Electronics, Inc., (414) 464-5555

Can Montreal, Quebec
Preco Electronics, Ltd. (514) 389-8051

Ottawa, Ontario
Preco Electronics, Ltd., (613) 237-6150

Rexdale, Ontario
Preco Electronics, Ltd., (416) 678-0401

Intl Australia, Artarmon, NSW
Digital Electronics (Marketing) Pty. Ltd. Tel: 43 6668

Intl Austria, Vienna
Bacher Elektronische Gerate Tel: 83 63 96 0

Intl Belgium, Brussels
Sotronic A.A. Tel: 736.10.07

Intl Denmark, Valby
Paratron A/S Tel: (01) 74 44 66

Intl Finland, Helsinki
Havulinna Oy Tel: (90) 661451

Intl France, Paris
Datel Systems Snael Tel: 603-06-74

Intl India, Bombay
Smita Electronics Tel: 40 542 564

Intl Israel, Tel Aviv
MTI Engineering Ltd. Tel: 244090, 236334

Intl Italy, Milano
3G Electronics s.r.l. Tel: 5442918 543096

Intl Japan, Tokyo
Datel KK Tel: 499-0631

Intl Netherlands, Amsterdam
Techmaton Tel: 020-456995

Intl New Zealand, Auckland
David J. Reid (N.Z.) Ltd. Tel: 492-189

Intl Norway, Oslo
Morgensierne & Co., A/S Tel: 37 29 40

Intl So. Africa, Johannesburg
Peter Jones Electronic Equipment PTY, Ltd., Tel: 22-3658

Intl Spain, Madrid
Aupoca Electronica Y Sistemas Tel: 457 53 12

Intl Sweden, Stockholm
AB Nordqvist & Berg Tel: 08-69 04 001

Intl Switzerland, Zurich
Traco Electronic Co., Ltd. Tel: 01/3607 11

Intl U.K.
Basingstoke, Hampshire
Datel (UK) Ltd. Tel: Basingstoke (0256) 66721

Intl W. Germany, Munich
Datelek Systems GmbH Tel: 089/78 4045

Data Device

Data Device Corporation
Airport Industrial Plaza
Bohemia, New York 11716
(516) 567-5600
TWX: (510) 221-1874

Electronic Arrays

Electronic Arrays, Inc.
550 East Middlefield Road
Mountain View, California 94043
(415) 964-4321
TWX: (910) 379-6985

Advanced Products Dick Eiler
Memory Products Bob Cushman
Consumer Products Dick Eiler
Literature:
Marketing Services Ed Meagher

Price and delivery:
Local Field Sales Offices (preferred), or Customer Service

Follow-up an order:
Customer Service
All other information:
Marketing Service Ed Meagher

Sales Offices & Representatives

Ariz Phoenix
Dorton Enterprises, Inc., (602) 263-0414

Cal Huntington beach
Electronic Arrays, Regional Office, (714) 968-3775

Los Angeles
Black, Ekizian & Strong, Inc., (213) 870-9191

Mountain View
Caltron/Pyle, Inc., (415) 964-3244
Electronic Arrays Regional Office, (415) 964-4321

San Diego
Bestronics, (714) 278-2150

Colo Denver
The Thorson Co., (303) 759-0809

Conn Wallingford
Com-Sale, Inc., (203) 269-7964

Fla Largo
Col-Ins-Co., (813) 343-0978

Orlando
Col-Ins-Co., Inc., (305) 423-7615

Ill Westchester
Gassner & Clark Company, (312) 345-4245

Ind Indianapolis
Ihrg Associates, (317) 783-7630

Iowa Cedar Rapids
Engineering Services Co., (319) 362-0503

Kan Prairie Village
Engineering Services Co., (913) 649-4000

Mass Waltham
Com-Sale, Inc., (617) 890-0011

Minn Minneapolis
Electronic Innovators, Inc., (612) 884-7471

Mo. St. Louis
Electronic Arrays, Regional Office, (314) 878-6446
Engineering Services Co., (314) 997-1515

NH Manchester
Com-Sale, Inc., (603)688-8500

N J Cherry Hill
Electronic Arrays, Inc., (609) 795-5066

NM Albuquerque
The Thorson Company, (505) 265-5655

NY Elmont
Crane & Egert Corp., (516) 488-2100

Ohio Cleveland
K.W. Electronic Sales, Inc., (216) 831-8292

Dayton
K.W. Electronic Sales, Inc., (513)890-2150

Electronic Arrays (cont)

- Ore** **Beaverton**
N. R. Schultz Co., (503) 643-1644
- Pa** **Allison Park**
K. W. Electronic Sales, Inc., (412) 487-3636
- Willow Grove**
Harry Nash Associates, (215) 657-2213
- Tex** **Dallas**
The Thorson Company, (214) 233-5744
- Houston**
The Thorson Company, (713) 771-3504
- Va** **Reston**
Boyle Associates (703) 620-9558
- Wash** **Bellevue**
N. R. Schultz Co., (206) 454-0300
- Intl** **Netherlands, Amsterdam**
Electronic Arrays, European Sales, (020) 712560
- Intl** **Far East, MT View Ca**
Electronic Arrays, Far East Sales, (415) 964-4321
- Intl** **Germany, Munich**
Electronic Arrays, GmbH, (089) 7853168
- Intl** **Japan, Tokyo**
Electronic Arrays Sales Office, 03-403-9061

Distributors

- Intl** **Australia, Prospect, SA**
A. J. Ferguson, 269-1244
- Intl** **Belgium, Bruxelles**
Beta Sprl., 02 49-80-85
- Intl** **France, Paris**
Technology Resources S.A., 747-4717
- Intl** **Holland, Breda**
Famatra Benelux, 01600-33457
- Intl** **India, Bombay**
Hinditron Services Pvt. Ltd., 36-5-3-44
- Intl** **Israel, Tel-Aviv**
Israel Radio Company, 50156
- Intl** **Italy, Milan**
Memos Italiana, 02-871353 or 867589
Philips Sezione Elcoma, 02-6994
- Intl** **Norway, Lillestrom**
Kjell Bakke & Co., 711-872
- Intl** **So. Amer. MT View Ca**
intetra, (415) 967-8818
- Intl** **Sweden, Vallingby**
Svensk Teleindustri, 08/89 04 35
- Intl** **Switzerland, Zurich**
Dimos AG, 08/89 04 35
- Intl** **U.K., East Molesey, Eng**
Analog Devices, Ltd., 941-0466

EMM/Semi

For data on selected products see page 734.

EMM/SEMI
Subsidiary of Electronic Memories
and Magnetics Corporation
3883 North 28th Avenue
Phoenix, Arizona 85017
(602) 263-0202
TWX: (910) 951-1383

Sales Offices & Representatives

- Ala** **Huntsville**
Gentry Associates, (205) 543-9771
- Ariz** **Tempe**
EMM, (602) 968-2492
- Cal** **Hawthorne**
EMM, (213) 644-9881
- Orange**
EMM, (714) 639-5811
- Santa Clara**
EMM, (408) 247-9711
- Fla** **Orlando**
Gentry Associates, (305) 894-9180

- Ga** **Atlanta**
Gentry Associates, (404) 448-2365
- Ill** **Des Plaines**
EMM, (312) 297-7090
- Mass** **Lexington**
EMM, (617) 861-9650
- NY** **Melville**
EMM, (516) 423-5800
- NC** **Burlington**
EMM, (919) 227-3639
- Ohio** **Akron**
EMM, (216) 867-5435
- Wash** **Bellevue**
Thorson Company, (206) 455-9180
- Can** **Montreal**
Cantec, (514) 620-3121
- Ottawa**
Cantec, (613) 225-0363
- Toronto**
Cantec, (416) 457-4455

Distributors

- Cal** **Newport Beach**
Semicomp Corporation, (213) 971-5253
- Minn** **Bloomington**
Arrow Electronics, (612) 888-5521
- NM** **Albuquerque**
Century Electronics, (505) 292-2700

Exar Integrated Systems

For data on selected products see page 630.

Exar Integrated Systems, Inc.
750 Palomar Ave.
Sunnyvale, California 94086
(408) 733-7700
TWX: (910) 339-9233

Specific product information:
Product Marketing

Application engineering:
Applications Engineering

Literature:
Local Representative or Distributor

Price and delivery:
Local Representative or Distributor

Place an order:
Less than 1000 pcs Local Distributor
Larger Orders Local Representative

Follow-up an order:
Local Representative or Exar Customer Service, (408) 733-7700

Sales Offices & Representatives

- Ariz** **Scottsdale**
Summit Sales, (602) 994-4587
- Cal** **Culver City**
DeAngelo, Rothman & Co., Inc., (213) 398-6239
- Redwood City**
Logan Sales, (415) 369-6726
- San Diego**
DeAngelo, Rothman & Co., Inc. (714) 560-5707
- Conn** **Wallingford**
Com-Sale, (203) 269-7964
- Fla** **Miami**
Reprtronics, Inc., (305) 251-5478
- St. Petersburg**
Reprtronics, Inc., (813) 522-8220
- Ga** **Atlanta**
Electro-Mech, (404) 449-6337
- Ill** **Chicago**
M & S Sales, (312) 992-1053
- Kan** **Wichita**
Dy-Tronix, Inc., (316) 943-6221
- Md** **Baltimore**
Component Sales, Inc., (301) 484-3647
- Mass** **Waltham**
Com-Sale, (617) 890-0011
- Mich** **Warren**
DEM Electronic Sales, (313) 755-6660
- Minn** **Minneapolis**
Electronic Innovators, (612) 884-7471
- Mo** **Hazelwood**
Dy-Tronix, Inc., (314) 731-5799

- Mo** **Kansas City**
Dy-Tronix, Inc., (816) 761-6543
- NM** **Albuquerque**
Tri-Tronix, (505) 265-8409
- NY** **Buffalo**
Quality Components, Inc., (716) 839-2044
- Manlius**
Quality Components, Inc., (315) 682-8885
- Rochester**
Quality Components, Inc., (716) 889-1919
- Williston Park, N.Y.C.**
ABC Electronic Sales, (516) 747-6610
- NC** **Raleigh**
Component Sales, Inc., (919) 782-8433
- Ohio** **Columbus**
McFadden Sales, (614) 221-3363
- Penn** **Erie**
ECCO Electronic Sales, (814) 452-3762
- Huntingdon Valley**
ABC Electronic Sales, (215) 947-6960
- Tenn** **Nashville**
Electro-Mech, (615) 883-1490
- Tex** **Dallas**
Technical Marketing, Inc., (214) 387-3601
- Houston**
Technical Marketing, Inc., (713) 777-9228
- Wash** **Bellevue**
SE-R² Products & Sales, (206) 747-9424
- Can** **Mississauga Ont.**
R.F.Q. Limited, (416) 625-8874
- Quebec, PQ**
R.F.Q. Limited, (514) 626-8324

Distributors

- Ala** **Huntsville**
Hall-Mark Electronics Corp., (205) 837-8700
- Ariz** **Phoenix**
MIRCO Electronic Dist., (602) 944-2281
- Cal** **Newport Beach**
Semicomp Corp., (714) 833-3070 (213) 971-5253
- San Diego**
Intermark Electronics, (714) 279-5200
- Santa Ana**
Intermark Electronics, (714) 540-1322
- Sunnyvale**
Intermark Electronics, (408) 738-1111
Semicomp Corp, (408) 736-2330
- Woodland Hills**
Semiconductor Concepts, Inc., (213) 884-4560
- Fla** **Ft. Lauderdale**
Hall-Mark Electronics Corp, (305) 971-9280
- Orlando**
Hall-Mark Electronics Corp, (305) 855-4020
- Ga** **Lawrenceville**
Hall-Mark Electronics Corp, (404) 963-9728
- Ill** **Elk Grove Village**
Hall-Mark Electronics Corp, (312) 437-8800
- Westmont**
Bodelle Co. Inc., (312) 323-9670
- Ind** **Ft. Wayne**
Graham Electronics, (219) 423-3422
- Indianapolis**
Graham Electronics, (317) 634-8486
- Lafayette**
Graham Electronics, (317) 742-4006
- Iowa** **Cedar Rapids**
Hall-Mark Electronics Corp., (319) 393-3556
- Kan** **Lenexa**
Hall-Mark Electronics, (913) 888-4747
- Wichita**
Hall-Mark Electronics Corp., (316) 682-2073
Radio Supply, (316) 267-5214
- Md** **Baltimore**
Hall-Mark Electronics Corp., (301) 265-8500
- Gaithersburg**
Pioneer, (301) 948-0710
- Mass** **Dedham**
Gerber Electronics, (617) 329-2400
- Mich** **Ann Arbor**
Wedemeyer Electronics, Inc., (313) 665-8611
- Minn** **Bloomington**
Hall-Mark Electronics, (612) 884-9056
- Minneapolis**
Cassidy Electronics, (612) 835-7744
- MO** **Earth City**
Hall-Mark Electronic, (314) 291-5350

Exar Integrated Systems (cont)

MO	St. Louis Olive Industrial Elec., (314) 863-7800
NH	Londonderry Yankee Electronics Supply, (603) 625-9746
NY	Hauppauge Hall-Mark Electronics, (516) 273-0030 Semiconductor Concepts, Inc., (516) 273-1234
NC	Raleigh Hall-Mark Electronics, (919) 832-4465
Ohio	Cincinnati Graham Electronics, (513) 733-1661 Dayton Hall-Mark Electronics, (513) 294-0437
Okla	Tulsa Component Specialties, Inc., (918) 664-2820 Hall-Mark Electronics, (918) 835-8458
Penn	Horsham Pioneer, (215) 674-5710 Huntingdon Valley Hall-Mark Electronics, (215) 355-7300
Tex	Austin Component Specialties, Inc., (512) 459-3307 Hall-Mark Electronics, (512) 837-2814 Dallas Component Specialties Inc., (214) 357-4576 Hall-Mark Electronics, (214) 231-6111 El Paso Hall-Mark Electronics, (915) 545-1763 Houston Component Specialties Inc., (713) 771-7237 Hall-Mark Electronics, (713) 781-6100
Utah	Salt Lake City Intermark Electronics, (801) 426-5600
Wash	Seattle Intermark Electronics, (206) 767-3160
Wisc	Mequon Taylor Electric Co., (414) 241-4321 West Allis Hall-Mark Electronics, (414) 476-1270
Can	Montreal, Quebec Future Electronics, (514) 735-5775 Vancouver, B.C. R-A-E Industrial Electronics, (604) 687-2621
Intl	Australia, Prospect A.J. Ferguson (Adelaide) Pty. Ltd., 269-1244
Intl	India, Bombay Zenith Electronics Jaikishan Nivas 36-7717
Intl	New Zealand, Auckland Professional Electronics Ltd., 469-450

Hobbyist Distributor

Cal Belmont
James Electronics, (415) 592-8097

Fairchild Semiconductor

For data on selected products see page 923.

Fairchild Camera and Instrument Corp.
Integrated Circuits Group
464 Ellis Street
Mountain View, California 94042
(415) 962-5011
TWX: (910) 379-6435

Specific product information:

Local field sales office or franchised distributor, or specific product marketing department at 464 Ellis Street, Mountain View, Ca.
Request through main switchboard:
Linear Integrated Circuit Product Mktg.
Bipolar Memory Product Mktg.
Digital Product Mktg. (Bipolar and CMOS)
Diode Product Marketing
MOS Product Marketing
Optoelectronic Product Marketing
Transistor Product Marketing

Application engineering:
See Product Information

Literature:
Local field office or specific product marketing group in Mountain View.

Price and delivery:
Local field sales office or franchised distributor.

Place an order:
Local field sales office or franchised distributor.

Follow-up an order:
Customer Service Center, 401 Ellis Street, Mountain View, Calif.
94042 (415) 962-3424
All other information:
Fairchild Information Line, (415) 962-4401

Sales Offices & Representatives

Ala	Huntsville Field Sales Office, (205) 883-7020 Cartwright & Bean, Inc., (205) 533-3509
Ariz	Phoenix Field Sales Office, (602) 264-4948
Cal	Irvine Cellec Company, (714) 752-6111 Los Angeles Field Sales Office, (213) 466-8393 Cellec Company, (213) 874-6002 San Diego Field Sales Office, (714) 279-6021 Cellec Company, (714) 279-7961 Santa Ana Field Sales Office, (714) 558-1881 Santa Clara Field Sales Office, (408) 244-1400 Magna Sales, Inc., (408) 985-1750
Colo	Denver Field Sales Office, (303) 234-9292 Littleton Simpson Associates, Inc., (303) 794-8381
Conn	Stamford Field Sales Office, (203) 348-7701 Lorac Sales, Inc., (203) 327-6238
Fla	Altamonte Springs WMM Associates, Inc., (305) 862-4700 Clearwater WMM Associates, Inc., (813) 447-2533 Orlando Field Sales Office, (305) 834-7000 Pompano Beach WMM Associates, Inc., (305) 943-3091 Tampa Field Sales Office, (813) 585-3892
Ga	Atlanta Cartwright & Bean, Inc., (404) 255-5262
Ill	Schiller Park Field Sales Office, (312) 671-4660
Ind	Fort Wayne Field Sales Office, (219) 483-6453 Indianapolis Field Sales Office, (317) 849-5412 Leslie M. Devoe Company, (317) 257-1227
Kan	Olathe B.C. Electronic Sales, Inc., (913) 782-6696 Wichita B.C. Electronic Sales, Inc., (316) 686-3394
Md	Bladensburg Field Sales Office, (301) 779-0954 L. D. Lowery, (301) 277-6555
Mass	Wellesley Hills Field Sales Office, (617) 237-3400 Spectrum Associates, Inc., (617) 237-2796
Mich	Detroit Rathsburg Associates, (313) 882-1717 Westland Field Sales Office, (313) 425-3250
Minn	Edina Field Sales Office, (612) 835-3322 Minneapolis PSI Company, (612) 835-1777
Miss	Jackson Cartwright & Bean, Inc., (601) 981-1368
Mo	Hazelwood B.C. Electronic Sales, Inc., (314) 731-1255
NJ	Wayne Field Sales Office, (201) 696-7070 Lorac Sales Inc., (201) 696-8815
NM	Albuquerque Field Sales Office, (505) 265-5601
NY	Endwell Field Sales Office, (607) 754-1094 Fairport Field Sales Office, (716) 223-7700 Melville Field Sales Office, (516) 293-2900
293-29 Lorac Sales, Inc., (516) 696-8815	
North Syracuse Advanced Components, Inc., (315) 699-2671	
Poughkeepsie Field Sales Office, (914) 452-4200	
293-29 Tuckahoe Spectrum Sales, Inc., (914) 793-1660	
NC	Charlotte Cartwright & Bean, Inc., (704) 333-6457 Raleigh Cartwright & Bean, Inc., (919) 834-1186
Ohio	Cleveland Components, Inc., (216) 243-9200 Dayton Field Sales Office, (513) 278-8278 Highland Heights Field Sales Office, (216) 461-8288 West Carrollton Components, Inc., (513) 866-0661
Okla	Tulsa Field Sales Office, (918) 663-7131
Pa	Broomall L.D. Lowery, (215) 356-5300 or 528-5170 Fort Washington Field Sales Office, (215) 886-6623 BGR Associates, (215) 643-4111
SC	Seneca Field Sales Office, (803) 882-1760
Tenn	Knoxville Cartwright & Bean, Inc., (615) 693-7450 Memphis Cartwright & Bean, Inc., (901) 276-4442
Tex	Dallas Field Sales Office, (214) 234-3391 Technical Marketing, 7214) 387-3601 Houston Field Sales Office, (713) 771-3547 Technical Marketing, (713) 777-9228
Wash	Bellevue Quadra Corporation, (206) 454-4946
Wisc	Greenfield Field Sales Office, (414) 282-5260 Wauwatosa Larsen Associates, (414) 258-0529
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Specific product information:

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Consumer ext. 247
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Application engineering:

Contact appropriate Product Marketing Department

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Semiconductor Specialist, (513) 278-9455

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Semiconductor Specialist, (412) 781-8120

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Cramer Electronics, (801) 487-4131

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Cramer Electronics, (206) 763-1550
Kierulff Electronics, (206) 763-1550
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Prelec Electronics, (514) 389-8051

Motorola Semiconductor

Motorola Semiconductor Products
5005 East McDowell Road
Phoenix, Arizona 85008

Specific product information:

Contact nearest district sales office or franchised distributor

Application engineering:

See Product Information

Literature:

See above

Price and delivery:

Direct contact with the proper people in the factory, if required, can be made through one of the sales offices or distributors.

Place an order:

See Price & Delivery

Follow-up an order:

See above

Sales Offices and Representatives

Ala Huntsville
Field Sales Office, (205) 533-1650

Ariz Phoenix
Field Sales Office, (602) 244-6900

Ariz Scottsdale
Field Sales Office, (602) 244-6364

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Motorola Semicondutores do Brasil, Ltd., 71-3185

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Motorola Semiconductors (01) 88.44.55

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Hamburg
RTG E SPRINGORUM KG, (040) 29 29 66

Hannover
SASCO Vertrieb von elektronischen Bauelementen GmbH,
(0511) 86 25 86

Karlsruhe
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Munich
EBV Elektronik Vertriebs GmbH (089) 64 40 55

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(0911) 20 41 52

Putzbrunn b Munich
SASCO Vertrieb von elektronischen Bauelementen GmbH, (089)
46 40 61

Schwalbach/Ts
Technoprojekt, (06196) 8 11 54

Stuttgart
EBV Elektronik Vertriebs GmbH (0711) 24 74 81/82/83

Saasfeld
SASCO Vertrieb von elektroni GmbH, (711) 24 45 21

Bachthop project.
(0711) 56 17 12

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Wuerges u Idstein
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Macedonian Electronics Ltd., 23 65 63

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Holland, Utrecht
N V Diode (030) 88 42 14

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Milcom Ltd., 68 12 14/15

Intl
Israel, Tel Aviv
Motorola Israel Ltd., 3 69 41/2/3

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Celdis Italiana SpA, (051) 31 08 43
Cramer Italia SpA, (051) 42 28 90

Milano
Celdis Italiana SpA, (02) 68 06 81/688 77 49
Cramer Italia SpA, (02) 376 40 39, 376 40 95

Roma
Celdis Italiana SpA, (06) 42 38 55/427 15 50
Cramer Italia SpA, (06) 513 93 87/90

Torino
Celdis Italiana SpA, (11) 35 93 128 36 74 48

Norway, Oslo
Ola Tandberg Elektro A/A, (02) 19 70 30

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Motorola S.A. NPty., Ltd., (002711) 636 90 57

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(513) 866-7471
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All Information: Marketing Dept.

National Semiconductor

For data on selected products see page 970.

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MOS LSI Dept Head	ext. 6595
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Literature:

Jean Hodges, Marketing Services ext. 6128

Price and delivery:

See listing of sales offices and representatives.

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Follow-up an order:

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All other information:

Chuck Signor, Public Relations ext. 6106.

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Astralronics, (213) 990-5903
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Pioneer/Washington Electronics, (301) 948-0710

Hanover
Hamilton/Avnet Electronics, (301) 796-5000

Mass Billerica
Kierulff Electronics, (617) 667-8331, 935-5134
Burlington
Hamilton/Avnet Electronics, (617) 273-2120
Wilshire Electronics, (617) 272-8200
Lexington
Harvey Electronics, (617) 861-9200

Mich Farmington
Advent Electronics, (313) 477-1650
Kentwood
Harvey Michigan Inc.
R-M Electronic Company, (616) 531-9300
Livonia
Hamilton/Avnet Electronics, (313) 522-4700
Pioneer/Michigan, (313) 525-1800

Minn Bloomington
Hall-Mark Electronics Corp., (612) 884-9056
Edina
Hamilton/Avnet Electronics, (612) 941-3801

Mo Earth City
Hall-Mark Electronics Corp., (314) 291-5350
Hazelwood
Hamilton/Avnet Electronics, (314) 731-1144

NJ Cedar Grove
Hamilton/Avnet Electronics, (201) 239-0800
Cinnaminson
Wilshire Electronics, (609) 786-8990 (215) 627-1920
Fairfield
Harvey Electronics, (201) 227-1262
Mount Laurel
Hamilton/Avnet Electronics, (609) 234-2133
Rutherford
Kierulff Electronics, (201) 935-2120

NM Albuquerque
Century Electronics, Inc., (505) 292-2700
Hamilton/Avnet Electronics, (505) 765-1500

NY Binghamton
Harvey Electronics, (607) 748-8211
Buffalo
Summit Distributors, (716) 884-3450
East Syracuse
Hamilton/Avnet Electronics, (315) 437-2642
Hauppauge, L.I.
Components Plus, (516) 231-9200
Semiconductor Concepts, (516) 273-1234
Rochester
Hamilton/Avnet Electronics, (716) 442-7820
Summit Electronics of Rochester Inc., (716) 334-8110
Westbury, L.I.
Hamilton/Avnet Electronics, (516) 333-5800
Woodbury
Harvey Electronics, (516) 921-8700

NC Greensboro
Hammond Electronics, (919) 275-6391
Pioneer/Carolina Electronics, (919) 273-4441
Raleigh
Hall-Mark Electronics (919) 832-4465

Ohio Cleveland
Hamilton/Avnet Electronics, (216) 461-1400
Pioneer Standard, (216) 587-3600
Dayton
Hamilton/Avnet Electronics, (513) 433-0610
Pioneer Standard, (513) 236-9900

Okla Oklahoma City
Radio, Inc., (405) ce5-1551
Tulsa
Hall-Mark Electronics Corp., (918) 835-8458
Radio Inc., Industrial Electronics, (918) 587-9124

Ore Portland
Almac/Stroum Electronics, (503) 292-3534

Pa Erie
Mace Electronics, (814) 838-3511
Huntington Valley
Hall-Mark Electronics Corp., (215) 355-7300
Pittsburgh
Cameradio, (412) 288-2600
Pioneer/Pittsburgh, (412) 782-2300

SC Greenville
Hammond Electronics of Carolina, Inc., (803) 233-4121

Tex Austin
Hall-Mark Electronics Corp., (512) 837-2814
Dallas
Hall-Mark Electronics Corp., (214) 231-6111
Hamilton/Avnet Electronics, (214) 661-8661
Sterling Electronics, (214) 357-9131
El Paso
Hall-Mark ELECTRONICS Corp., (915) 545-1763
Houston
Hall-Mark Electronics Corp., (713) 781-6100
Hamilton/Avnet Electronics, (713) 526-4661

Utah Salt Lake City
Century Electronics Inc., (801) 487-8551
Hamilton/Avnet Electronics, (801) 262-8451

Wash Bellevue
Hamilton/Avnet Electronics, (206) 746-8750
Seattle
Almac/Stroum Electronics, (206) 763-2300
Liberty Electronics Northwest, (206) 763-8200

Wisc Milwaukee
Taylor Electric Company, (414) 241-4321

Can Dorval, Quebec
Semad Electronics, Ltd.,
Downsview, Ont.
Semad Electronics, Ltd., (416) 635-9880
Mississauga
Hamilton/Avnet Electronics, Ltd., (416) 677-7432
Montreal, Quebec
Prelco Electronics, Ltd., (514) 389-8051
Ottawa
Hamilton/Avnet Electronics, (613) 725-3071

National Semiconductor (cont)

Can St. Laurent, Quebec
Hamilton/Avnet Electronics, (514) 331-6443
Willowdale, Ontario
Electro SONIC, Inc., (416) 494-1666

NEC Microcomputers

NEC Microcomputers
5 Militia Drive
Lexington, Mass 02173
TWX: 92-3434
(617) 862-6410

Sales Offices and Representatives

Ariz Scottsdale
Summit Sales, (602) 994-4587

Cal El Toro
Electronic Component Marketing, (714) 830-3939
Mountain View
Trident Associates, (415) 967-7031
San Diego
Electronic Component Marketing, (714) 295-6122
Woodland Hills
Electronic Component Marketing, (213) 340-1745

Fla Clearwater
Perrott Associates, Inc., (813) 726-1549
Orlando
Perrott Associates, Inc., (305) 275-1132

Ill Park Ridge
R.F. Specialists, (7312) 698-2044

Mass Lexington
Circuit Sales Company, (617) 861-0567

Minn Minneapolis
Bitronics Sales Company, (612) 835-7744

NM Albuquerque
Tri-Tronix, (505) 265-8400

NY Great Neck
TRIONIC Associates, Inc., (516) 466-2300

Ohio Columbus
McFadden Sales, Inc., (614) 221-3363

Penn Hershey
C.A. Newson & Associates, (717) 233-8576, (301) 825-0001
Philadelphia
C.H. Newson & Associates, (215) 248-3377

Tex Dallas
Merino Sales Company, (214) 233-6002

Wash Bellevue
Tri-tronix N.E., (7206) 454-0940

Can Mississauga, Ontario
R.F.Q. Ltd., (514) 626-8324
Dollard Des Ormeaux, Que
R.F.Q. Ltd., (416) 625-8874

Nippon Electric Co.

NEC America
Nippon Electric Ltd.
277 Park Avenue
New York, N.Y. 10017
(212) 758-1666

Nitron

Nitron
A Division of McDonnell Douglas
Corporation
10420 Bubb Road
Cupertino, California 95014
(408) 255-7550
TWX: (910) 338-0222

Specific product information:

ROMS ext. 208
MNOS ext. 203

Application engineering:

..... ext. 217

Literature:

..... ext. 218

Price and delivery:

..... ext. 218

Place an order:

..... ext. 218

Follow-up an order:

..... ext. 218

Sales Offices & Representatives

Ala Huntsville
Technology Marketing Assoc., (205) 883-7893
Scottsdale
Carter Associates, Inc., (602) 947-4355

Cal Glendale
Orion Sales, Inc., (213) 240-3151
Palo Alto
R. W. Thompson Assoc., Inc., (415) 494-7516
Tustin
Orion Sales, Inc., (714) 832-9687

Colo Denver
Omega Ltd., (303) 758-1508

Conn Guilford
R. H. Sturdy Company, Inc., (203) 453-5424

Fla Ormond Beach
Technology Marketing Assoc., (904) 672-2314
Pompano Beach
Technology Marketing Assoc., (305) 942-0774

Ill Chicago
Carlson Electronic Sales Co., (312) 774-9022, (312) 774-4812

Md Glen Burnie
New Era Sales, Inc., (301) 768-6666

Mass Wellesley Hills
R. H. Sturdy Co., Inc., (617) 235-2330

Mich Warren
Dem Electronic Sales, (313) 755-6660

Minn Minneapolis
S & R Component Sales, Inc., (612) 544-3022

NY Jericho
Electro Rep Inc., (516) 938-0540

Ore Portland
C.K. Shanks & Associates, Inc., (503) 292-5656

Penn Birchrunville
Jadelectronic Associates, Inc., (215) 647-5151

Tex Addison
Robert R. Thomas Co., (214) 233-8235

Utah Salt Lake City
Omega Ltd., (801) 266-9617

Wash Seattle
C.K. Shanks & Associates, Inc., (206) 632-4290

Wisc Milwaukee
Carlson Electronic Sales Co., (414) 476-2790

Can Mississauga, Ont.
Munro Electronic Components Ltd., (416) 676-1042
Ottawa, Ont.
Munro Electronic Components Ltd., (613) 749-0740
Dollard des Ormeaux, PQ
Munro Electronic Components Ltd., (514) 626-6723

Intl Denmark, lyngby
Knud Kamuk A/S, (01) 88 38 33

Intl England, Oxfordshire
Peter Gray Electronics Ltd., (Henley 6543)

Intl France, Sevres
Tekelec Airtronic, 626 02 35

Intl Germany
Hamburg
Infratron Ing., 040-81 75 78

Intl Munich
Infratron Ing., 089-52 41 81

Intl Holland, Breda
Klaasing Electronics B.V. 01600-48457

Intl Italy, Milan
Silverstar, Ltd., 4996

Intl Japan, Tokyo
Kyokuto Boeki Kaisha, Ltd., 244-3511

Intl Sweden, SoIna
Johan Lagercrantz KB 08-83 07 90

Intl Switzerland, Mutschellen
W. Stolz AG, 057-5 46 55

Nortec Electronics

Nortec Electronics Corporation
3697 Tahoe Way
Santa Clara, California 95051
(408) 732-2204
Telex: 348359

Specific product information:

Joel Scheinberg ext. 201

Application engineering:

Joel Scheinberg ext. 201
Candi Harrell

Price and delivery:

Joel Scheinberg ext. 201

Place an order:

Joel Scheinberg ext. 201
Judy Rowan ext. 209

Follow-up an order:

Joel Scheinberg ext. 201

All other information:

Dick Kors ext. 207

Sales Offices and Representatives

Ariz Scottsdale
Summit Sales, (602) 994-4587

Cal Pasadena
Micronics, (216) 449-0075

Colo Denver
James S. Heaton Co., Inc., (303) 758-5130

Ill Park Ridge
R. R. Specialists, (312) 698-2044

Ind Ft. Wayne
R.R. Specialists, (219) 485-8982

Md Towson
Newson & Associates, (301) 825-0001

Mass Lexington
Circuit Sales Company, Inc., (617) 861-0567

Mich New Baltimore
Tek-Tron Engineering, (313) 725-4600

NJ Ft. Lee
Tech Sales, (201) 944-3642

Pa Philadelphia
Newson & Associates, Inc., (215) 248-3377

Tex Richardson
Semiconducto Sales, (214) 231-6181

Wash Bellevue
Tri-Tronix, (7206) 454-0940

Can Mississauga, Ont.
Semicon Electronics Limited, (416) 678-9225
Point Claire, Quebec
Semicon Electronics Limited, (514) 697-9970

Nucleonic Products Co.

Nucleonic Products Co.
6660 Variel Avenue
Canoga Park, California 91303
(213) 887-1010
TWX: (910) 494-1954

Sales Offices and Representatives

Ariz Phoenix
Chaparral-Dorton, (602) 263-0414

Cal Los Angeles
NPC, (213) 887-1010
Newbury Park
Astralonics, (805) 498-2183
Redwood City
Logan Sales, (415) 367-6726
San Diego
Earle Associates, (714) 278-5441

Colo Denver
Egeman Assoc., (303) 423-3707

Conn Fairfield
Hingston-Walsh, (914) 834-4423

Fla Miami
Component Engr. Sales Co., (305) 922-5230

Ill Chicago
R.H. Dutton & Assoc., (312) 297-3365
Franklin Park
Dekotech, Inc., (312) 455-5100

Ind Indianapolis
Technical Reprs., (317) 849-6454

Iowa Cedar Rapids
J.R. Sales, (319) 377-8211

Kan Kansas City
CenTech Sales, (816) 358-8100

Md Baltimore
Component Sales, (301) 484-3647

Mass Waltham
Ranteck, Inc., (617) 890-5110

Mich Farmington
Davis & Martensen, (313) 474-8300

Minn Minneapolis
Quantum Sales, (612) 831-8583

Mo St. Louis
CenTech Sales, (314) 731-4220

NY New York City
Kahgan Sales, (516) 538-2300
De Ruyter
R.P. Kennedy Co., (315) 662-3996
Red Hook
R.P. Kennedy Co., (914) 876-2700
Rochester
R.P. Kennedy Co., (716) 271-6322

NC Raleigh
Component Sales, (919) 782-8433

Ohio Cincinnati
GH Sales Co., (513) 771-8231
Cleveland
GH Sales Co., (216) 248-8490

Ore Portland
Freed Assoc., (503) 223-3374

Penn Willow Grove
Harry Nash Assoc., (215) 657-2213

Tex Dallas
Bonser-Philhower Sales, (214) 234-8438
Houston
Bonser-Philhower Sales, (713) 467-4373

Wash Seattle
Freed Assoc., (206) 822-8223

OKI Electronics of America

OKI Electronics of America
4031 N.E. 12th Terrace
P. O. Box 24260
Fort Lauderdale, Florida 33307
(305) 563-6234
TWX: (510) 955-9837

Panasonic

Panasonic
Matsushita Electric Corporation Industrial
Division
1 Panasonic Way
Secaucus, New Jersey 07094
(201) 348-7267

Specific product information:
IC's and Solid State Products Product Manager, Bob Zolkowski

Application engineering:
Chicago, Arthur Suyamaext. (312) 455-3105
New Jersey, M. Toyoscu
(201) 348-7275

Price and delivery:
See Local Representatives

Place an order:
See Local Representatives

Follow-up an order:
See Local Representatives

Sales Offices & Representatives

Ala Huntsville
Rep, Inc., (205) 881-9270

Ariz Phoenix
Arrowhead Sales Corporation, (602) 277-7148

Cal Los Angeles
West Inc., (213) 625-1868, (714) 540-9040
San Jose
Allgood-North, (408) 288-6731

Col Arvada
Arrowhead Sales Corporation, (303) 423-5556

Conn Bridgeport
Vector Sales, (203) 366-2506

Fla Casselberry
EIR, Incorporated, (305) 830-9600
Palm Beach
EIR, Incorporated, (305) 585-6689
Plantation
EIR, Incorporated, (305) 791-6390

Ga Tucker
Rep, Inc., (404) 938-4358

Ill Chicago
Brock & Cushman, (312) 622-4110

Iowa Des Moines
B.E.A.M.S., Inc., (515) 282-0292

Kans Overland Park
B.E.A.M.S., Inc., (913) 341-7744

Mass Allston
Vector Sales, Inc., (617) 787-2790

Mich Detroit
NICON Associates, (313) 341-7688

Minn St. Paul
SKOR, (614) 645-6461

Mo St. Louis
B.E.A.M.S., Inc., (314) 781-6855

NJ Plainfield
Meg Electronic Sales, (201) 757-4332, (212) 233-9059

NY Ontario Center
Kehoe Elec., (315) 524-2491

NC Charlotte
Anthom Inc., (704) 527-1515

Ohio Columbus
Tom Mulligan & Associates, (614) 457-2242

Ore Portland
Almac/Stroum Electronics, (503) 292-3534

Pa King of Prussia
Monteiro Associates, Inc., (215) 265-0634

Tex Addison
Dunbar Associates, Inc., (214) 239-7151

Va Alexandria
Dyna Rep. Co., (703) 354-1222

Wash Seattle
Almac/Stroum Electronics, (206) 763-2300, (206) 243-2301

Can Quebec
R F Q Ltd., (514) 626-8324
Ontario
R F Q Ltd., (416) 625-8874

Intl Japan, Kyoto
Matsushita Electronics, Tel: (075) 921-8151

Plessey Semiconductors

Plessey Semiconductors
1674 McGaw Avenue
Santa Ana, California 92705
(714) 540-9979 or 540-9945
TWX: (910) 595-1930

Application engineering:
Walt Boris ext. 49

Literature:
Donna Clark ext. 35

Price and delivery:
Donna Clark ext. 35

Follow-up an order:
Donna Clark ext. 35

Sales Offices & Representatives

Ariz Phoenix
The Thorson Company, (602) 956-5300

Cal Los Altos
Cain-White, (415) 948-6533
Los Angeles
The Thorson Company, (213) 476-1241
Tustin
The Thorson Company, (714) 544-5121

Colo Denver
West Mark Associates, (303) 433-7181

Ill Park Ridge
R. F. Specialists, (219) 485-8982

Ind Fort Wayne
R. F. Specialists, (219) 485-8982

Iowa Cedar Rapids
Glassner & Clark Co., (319) 393-5763

Kan Prairie Village
Engineering Services, (913) 649-4000

Mass Natick
Wayland Engineering Sales, (617) 655-6080

Mo Saint Louis
Engineering Services, (314) 997-1515

NM Albuquerque
The Thorson Company, (505) 265-5655

NY Plainview
Erde Associates, Inc., (516) 822-5357
Syracuse
Syracuse Technical Reprs. (315) 488-0222

Ohio Cincinnati
Luebbe Sales, (513) 871-4211

Pa Easton
Megargel/Himmelstein, (609) 622-3081

Tenn Bristol
Remco, (615) 968-4195

Tex Dallas
W. Pat Frau Co., (817) 738-2394

Wash Olympia
Bergford and Associates, (206) 866-2001

Power Monolithics

Power Monolithics
121 International Drive
Corpus Christi, Texas 78401
(512) 883-6251

Precision Monolithics

Precision Monolithics, Inc.
1500 Space Park Drive
Santa Clara, California 95050
(408) 246-9222
TWX: (910) 338-0528

Specific product information:
Local Field Sales Office

Literature:

Local Field Sales Office

Follow-up an order:

Customer Service ext. 171

Sales Offices & Representatives

Ala Huntsville
W. A. Brown Components, (205) 539-4411

Ariz Tempe
Argus Sales Inc., (602) 967-8709

Cal El Toro
ECM, (714) 830-3939
Mt. View
Thresum Assoc., (408) 965-9180
Newport Beach
PMI, (714) 752-1760
San Diego
ECM, (714) 295-6122
Woodland Hills
ECM, (213) 340-1745

Colo Denver
Thorson Company, (303) 759-0809

Conn Wallingford
Com-Sale, (203) 269-7964

Fla Clearwater
DYNE-A-MARK, (813) 441-4702
Ft. Lauderdale
DYNE-A-MARK, (305) 771-6501, (305) 944-5031 (Miami)

Ga Atlanta
W. A. Brown Components, (404) 455-0405

Ill Arlington Heights
PMI, (312) 437-6697
Rolling Meadows
Sumer Inc., (312) 394-4900

Ind Indianapolis
Jerry Ihrig Assoc. Inc., (317) 783-7630

Iowa Cedar Rapids
Comstrand, Inc., (319) 363-7495

Kan Olathe
Technical Representatives, Inc., (913) 782-1177

Md Baltimore
Stemler Assoc. Inc, (301) 944-8262

Mass Waltham
COM-SALE, (617) 890-0011

Mich Detroit
A. Blumenberg Assoc., (313) 557-1934

Minn Minneapolis
Comstrand, Inc., (612) 571-0000

Mo Hazelwood
Technical Representatives, (314) 731-5200

NJ Cherry Hill
Stemler Assoc., (609) 966-4070
Laurel Springs
Stemler Assoc. Inc., (215) 644-3477

NM Albuquerque
Thorson Company, (505) 265-5655

NY Jericho
J-Square Marketing, Inc., (516) 433-5330
Rochester
Ontec Associates, (716) 464-8636
Wantagh
PMI, (516) 785-3331

NC Raleigh
W. A. Brown Components, (919) 876-9601
Winston-Salem
W.A. Brown Components, (919) 725-5384

Ohio Cleveland
Del Steffen & Associates, (216) 461-8333
Dayton
Del Steffen & Associates, (513) 293-3145
Lexington
Del Steffen & Assoc., (419) 884-2313

Ore Portland
SJI, (206) 224-0344

Tex Houston
Oeler & Menelaides, Inc., (713) 772-0730
Richardson
Oeler & Menelaides, Inc., (214) 234-6334

Va Alexandria
Stemler Associates, Inc., (703) 548-7818

Wash Seattle
SJI, (206) 624-9020

Can Mississauga, Ontario
RFQ Limited, (416) 625-8874

Distributors

Ariz Phoenix
Sterling Electronics, (602) 258-4531

Cal Chatsworth
Westates Electronics Corp., (213) 341-4411

Cal San Diego
Intermark Electronics, (714) 279-5200
Santa Ana
Intermark Electronics, (714) 540-1322
Sunnyvale
Intermark Electronics, (408) 738-1111
Westates Electronics Corp., (408) 733-8383

Colo Denver
Intermark Electronics, (303) 936-8284

Ill Elk Grove Village
Hallmark Electronics, (312) 437-8800

Ind Indianapolis
Pioneer Electronics, (317) 849-7300

Md Baltimore
Whitney Distributors, (301) 944-8080

Mass Dedham
Gerber Electronics, (617) 329-2400
Woburn
Newark Electronics, (617) 935-8350

Mich Detroit
R.S. Electronics, (313) 491-1000

Minn Bloomington
Hallmark Electronics, (612) 884-9056

Mo Garth City
Hallmark Electronics, (314) 291-5350

NM Albuquerque
Sterling Electronics, (505) 345-6601

NY Binghamton
Harvey Electronics
Vestal
Shipping Address, (607) 748-8211
Woodbury
Harvey Electronics, (516) 921-8700

NC Winston-Salem
Kirkman Electronics, (919) 724-0541

Ohio Cleveland
Pioneer Electronics, (216) 587-3600
Columbus
Pioneer Electronics, (800) 362-2274
Dayton
Pioneer Electronics, (513) 236-9900

Ore Portland
Almac/Stroum Electronics, (503) 292-3534

Pa Huntington Valley
Hallmark Electronics, (215) 355-7300
Pittsburgh
Pioneer Electronics, (412) 391-4846

Tex Dallas
Sterling Electronics, (214) 357-9131
Houston
Sterling Electronics, (713) 627-9800

Wash Seattle

Can Vancouver, B. C.
Intek Electronics, Ltd., (604) 736-7677
Almac/Stroum Electronics, (206) 763-2300

Ragen Semiconductor

Ragen Semiconductor
53 South Jefferson Road
Whippany, New Jersey 07981
(201) 887-4141

Information:
F. Jack Hartley
Joseph Larkin

Raytheon Semiconductor

For data on selected products see page:

Digital 282
Linear 647

Raytheon Semiconductor
350 Ellis St.
Mt. View, California 94042
(415) 968-9211
TWX: (910) 379-6481

Specific product information:

Linear Al Borken, Nik Raines
Digital Steve Fry
Discrete John Norton, Larry Collins
Microprocessors Paul Sullivan

Price and delivery:
Local Field Sales Office

Place an order:
Local Field Sales Office

Follow-up an order:
Customer Service

Sales Offices & Representatives

Ariz Scottsdale
Gleason Sales, (602) 946-3992

Cal Irvine
Raytheon Semiconductor, (714) 833-9042
Los Altos
P. M. Sales, (415) 941-4444
Mountain View
Raytheon Semiconductor, (415) 964-4754

Colo Denver
Straube Associates, (303) 426-0890

Fla Clearwater
Perrott Associates, (813) 726-1549
Fort Lauderdale
Raytheon Semiconductor, (305) 792-8400

Orlando
Perrott Associates, (305) 275-1132

Ill Chicago
Carlson Electronic Sales, (312) 774-9022
Des Plaines
Raytheon Semiconductor, (312) 297-5540

Kan Overland Park
Electri-Rep, (913) 649-2168

Mass Burlington
Raytheon Semiconductor, (617) 272-8500

Mich Birmingham
J.C. Hofstetter Co., (313) 643-7203
Grand Rapids
J.C. Hofstetter Co., (616) 942-0650

Minn New Brighton
Raytheon Semiconductor, (612) 636-7696

Mo St. Louis
Kebco, (314) 569-2660

NJ Pennsauken
Raytheon Semiconductor, (609) 663-4066

NY Baldwin (NY Metro Area)
R.O.M.E. Inc., (516) 623-3344
Melville
Raytheon Semiconductor, (516) 420-0700
North Syracuse
Precision Sales, (315) 458-2223
Orchard Park
Precision Sales, (716) 648-5450

Raytheon Semiconductor (cont)

NY Oswego
Precision Sales, (607) 687-2893

Ohio Dayton
J.C. Hofstetter Co., (513) 296-1010
Medina
J.C. Hofstetter Co., (216) 241-4880

Ore Beaverton
E.S. Chase Co., (503) 649-6177

Tex Dallas
Kruvand Associates, (214) 691-4592
Mark Kruvand Co., Inc., (214) 827-8043
Houston
Kruvand Associates, (713) 661-3007
Mark Kruvand Co., Inc., (713) 661-3007

Wash Seattle
E.S. Chase Co., Inc., (206) 762-4324

Wisc Milwaukee
Carlson Electronic Sales, (414) 476-2790

Can Massachusetts Office

Intl Germany, Munich
Raytheon Halbleiter GmbH, 089/539 693

Intl Japan, Tokyo
New Japan Radio Co., Ltd., (591) 3451

Intl Switzerland, Zurich
Transistor AG-Raytheon 01 625611

Intl All other Overseas Areas
Lexington, Mass
Raytheon Co., International (617) 862-6600

Distributors

Ala Huntsville
Hallmark Electronics, (205) 837-8700

Ariz Phoenix
Cramer Electronics, (602) 267-7321
Kierulff Electronics, (602) 273-7331

Ark Fort Smith
Carlton Bates, (501) 646-8201, (800) 362-9009

Cal Culver City
Avnet Electronics, (213) 559-4111
Irvine
Cramer/Los Angeles, (213) 771-8300, (714) 979-3000
Los Angeles
Kierulff Electronics, (213) 685-5511
Newport Beach
Semicomp, (714) 833-3070 (213) 581-7201
Palo Alto
Kierulff Electronics, (415) 968-6292
San Diego
Cramer/San Diego, (714) 565-1881
Intermark Electronics, (714) 279-5200
Kierulff Electronics, (714) 278-2112
Santa Ana
Intermark Electronics, (714) 540-1322, (213) 436-5275
Sunnyvale
Bell Industries, (408) 734-8570
Cramer/San Francisco, (408) 739-3011
Intermark Electronics, (408) 738-1111

Colo Denver
Cramer/Denver, (303) 758-2100
Wheatridge
Century Electronics, (303) 424-1985

Conn North Haven
Cramer/Connecticut, (203) 239-5641

Fla Clearwater
Diplomat/Southland, (813) 443-4514
Hollywood
Cramer/EW Hollywood, (305) 923-8181
Orlando
Cramer/EW Orlando, (305) 894-1511

Ga Atlanta
Cramer/EW Atlanta, (404) 448-9050
Lykes Electronics, (404) 355-2223

Ill Elk Grove Village
Hallmark Electronics, (312) 437-8800
Diplomat/Lakeland, (312) 595-1000
Mt. Prospect
Cramer/Chicago, (312) 593-8230

Ind Indianapolis
Graham Electronics Supply, Inc., (317) 635-5453

Md Baltimore
Radio Electric Service Co., (301) 823-0070
Technico, (301) 828-6416
Gaithersburg
Cramer/Washington, (301) 948-0110
Pioneer Washington Elect., (301) 948-0710
Hanover
Cramer/Baltimore, (301) 796-5790

Mass Billerica
Kierulff Electronics, (617) 667-8331.
Framingham
Future Electronics, (617) 879-0860, (800) 225-0380-Toll Free
Newton
Cramer Electronics, (617)

Mich Farmington
Diplomat/Northland, (313) 477-3200

Minn Minneapolis
Diplomat/Electro Com., (612) 788-8601
Hallmark Electronics, (612) 884-9056
Stark Electronic Supply, (612) 332-1325

Mo Earth City
Hallmark Electronics, (314) 291-5350
St. Louis
Diplomat/St. Louis, (314) 645-8550

NJ Cherry Hill
Cramer/Pennsylvania, (609) 424-5993
Hackensack
Components Plus, (201) 487-0565
Moonachie
Cramer Electronics, (201) 935-5600
Moorestown
Arrow/Angus, (609) 235-1900

NM Albuquerque
Centruy Electronics, (505) 292-2700
Cramer/New Mexico, (505) 265-5767
Kierulff Electronics, (505) 247-1055

NY East Syracuse
Cramer/Syracuse, (315) 437-6671
Elmsford
Zeus Components, Inc., (914) 592-4120
Hauppauge
Components Plus, (516) 231-9200
Cramer/Long Island, (516) 231-5600
Semiconductor Concepts, (516) 273-1234
New Hyde Park
Lafayette Industrial Elect., (516) 488-6600
Plainview
ACI Electronics Corp., (513) 293-6630
Rochester
Cramer/Rochester, (716) 275-0300

NC Winston-Salem
Cramer/EW Winston-Salem, (919) 725-8711

Ohio Cleveland
Cramer/Cleveland, (216) 248-8400
Dayton
Diplomat/Ohio, (513) 228-1080

Okla Tulsa
Component Specialties, (918) 664-2820

Pa Braddock
Leff Radio Parts, (412) 271-7100

Tex Austin
Component Specialties, (512) 459-3307
Dallas
Component Specialties, (214) 357-4576
Cramer/Texas, (214) 661-9300
Houston
Component Specialties, (713) 771-7237

Utah Salt Lake City
Diplomat/Altalad, (801) 486-7227
Cramer/Utah, (801) 487-4131

Wash Bellevue
Bell Industries, (206) 747-1515
Seattle
Cramer/Seattle, (206) 762-5755
Intermark Electronics, (206) 767-3160

Wisc West Allis
Hallmark Electronics, (414) 476-1270

Can Calgary, Alberta
PAAR Industrial Electronics (408) 287-2840
Downsview, Ont.
Cramer/Canada, (416) 661-9222
Ottawa, Ont.
Wackid Radio & Television Labs, (613) 728-1821
Montreal, P.Q.
Future Electronics, (514) 735-5775
Prelco Electronics, Ltd., (514) 389-8051
Rexdale, Ont.
Future Electronics, (416) 677-7820
Vancouver, B.C.
RAE Industrial Electronics, Ltd., (604) 687-2621

RCA Solid State Division

For data on selected products see page:

Digital 375
Linear 661
Memory 784
Microprocessor 993

RCA Solid State Division
Rte. 202
Somerville, N.J. 08876
(201) 685-6000
TWX: 710-480-9333

Sales Offices and Representatives

Ala Huntsville
Field Sales Office, (205) 881-4100

Ariz Scottsdale
Field Sales Office, (602) 947-7235

Cal Hollywood
Field Sales Office, (213) 461-9171
Los Altos
Field Sales Office, (415) 948-8996
San Diego
Field Sales Office, (714) 279-0420
Tustin
Field Sales Office, (714) 832-5302

Colo Denver
Field Sales Office, (303) 433-8841

Conn Stamford
Field Sales Office, (203) 329-2041

Fla Riviera Beach
Field Sales Office, (305) 842-1577

Ga Atlanta
Field Sales Office, (404) 634-6131

Ill Des Plaines
Field Sales Office, (312) 827-0033

Ind Fort Wayne
Field Sales Office, (219) 432-9461
Indianapolis
Field Sales Office, (317) 546-4001

Kans Overland Park
Field Sales Office, (913) 642-7656

Mass Needham Heights
Field Sales Office, (617) 444-7200

Mich Birmingham
Field Sales Office, (313) 644-1151

Minn Minneapolis
Field Sales Office, (612) 929-0676

NJ Cherry Hill
Field Sales Office, (609) 424-3650
Edison
Field Sales Office, (201) 485-3900

NY Long Island
Field Sales Office, (516) 293-0180
Fairport
Field Sales Office, (716) 223-5240
Syracuse
Field Sales Office, (315) 474-8221

Ohio Dayton
Field Sales Office, (513) 253-1133
Pepper Pike
Field Sales Office, (216) 831-0030

Tex Dallas
Field Sales Office, (214) 638-6200

Va Arlington
Field Sales Office, (703) 558-4161

Wash Bellevue
Field Sales Office, (206) 747-8534

Can Rexdale (Toronto), Ont.
Field Sales Office, (416) 247-5491
St. Anne de Bellevue
Field Sales Office, (514) 457-9000

Intl Eng., Sunbury-on-Thames
RCA Ltd. for Europe, Middle East, Africa & U.K., SUN 85511

Intl Latin America
Somerville, NJ
International Sales, (201) 722-3200

Intl Japan, Tokyo
RCA Purchasing Co., 581-2311

Intl Taiwan, Taipei
RCA 579171

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RCA Solid State Division (cont)

Distributors

Ala **Huntsville**
Hamilton/Avnet Electronics, (205) 533-1170

Ariz **Phoenix**
Hamilton/Avnet Electronics, (602) 275-7851
Kierulff Electronics, (602) 272-7331
Liberty Electronics/Arizona, (602) 257-1272

Cal **Culver City**
Hamilton Electro Sales, (213) 558-2020

El Monte
G.S. Marshall Co., (213) 686-0141

El Segundo
Liberty Electronics, (213) 322-8100

Irvine
Cramer/Los Angeles, (213) 771-8300

Los Angeles
Kierulff Electronics, (213) 685-5511
RPS Electronics, Inc., (213) 748-1271

Mt. View
Elmar Electronics, Inc., (415) 961-3611
Hamilton-Avnet Elect., (415) 961-7000

Palo Alto
Kierulff Electronics, (415) 968-6292

Riverside
Electronic Supply Corp., (714) 683-7300

San Diego
Hamilton/Avnet Electronics, (714) 279-2421
Kierulff Electronics, (714) 278-2112
Liberty/San Diego, (714) 565-9171

Sunnyvale
Cramer/San Francisco, (408) 739-3011

Colo **Commerce City**
Elmar Electronics/Denver, (303) 287-9611

Denver
Kierulff Electronics, (303) 343-7090

Conn **Danbury**
Schweber Electronics Corp., (203) 792-3500

North Haven
Cramer Electronics, Inc., (203) 239-5641

Fla **Hollywood**
Cramer/EW, Hollywood, (305) 945-4176
Hamilton/Avnet Electronics, (305) 927-0511
Schweber Electronics, (305) 927-0511

Orlando
Cramer/EW, Orlando, (305) 894-1511

Ga **Atlanta**
Schweber Electronics Corp., (404) 449-9170

Doraville
Cramer/EW, Atlanta, (404) 451-5241

Norcross
Hamilton/Avnet Electronics, (404) 448-0800

Ill **Chicago**
Newark Electronics, (312) 638-4411

Elmhurst
Semiconductor Specialist, (312) 279-1000

Mt. Prospect
Cramer/Chicago, (312) 593-8230

Ind **Indianapolis**
Graham Electronics Supply, Inc., (317) 634-8202

Iowa **Cedar Rapids**
Deeco Inc., (319) 365-7551
Schweber Electronics Corp., (319) 393-9125

Kans **Lenexa**
Hamilton/Avnet Electronics, (913) 888-8900

Wichita
Radio Supply Co., (316) 267-5214

Md **Gaithersburg**
Cramer/EW Washington, (301) 948-0110

Hanover
Hamilton/Avnet Electronics, (301) 796-7000

Rockville
Schweber Electronics, (301) 881-3300

Savage
Pytronix Industries, (301) 792-7000

Mass **Burlington**
Wilshire Electronics/New England, (617) 272-8200

Newton
Cramer Electronics, (617) 969-7700

Waltham
Schweber Electronics, (617) 890-8484

Watertown
Sterling Electronics, (617) 926-9720

West Newton
A.W. Mayer Co., Inc., (617) 965-1111

Mich **Troy**
Schweber Electronics Corp., (313) 583-9242

Mich **Detroit**
RS Electronics, Inc., (313) 491-1000

Oak Park
Newark Electronics, (313) 548-0250

Minn **Edina**
Cramer/Minnesota, (612) 941-4860

Minneapolis
Newark Electronics, (612) 331-6350
Semiconductor Specialists, Inc., (612) 854-8841

Mo **Hazelwood**
Hamilton/Avnet Electronics, (314) 731-1144
Semiconductor Specialists, Inc., (314) 731-2400

Kansas City
Semiconductor Specialists, Inc., (816) 452-3900

NJ **Clifton**
Wilshire Electronics/N.J., (201) 365-2600

Mount Laurel
Hamilton-Avnet Elect., (609) 234-2133

Pennsauken
Resco Electronics, Div. of Astrex, (609) 662-4000

Perth Amboy
Sterling Electronics, (201) 442-8000

Rutherford
Kierulff Electronics, (201) 935-2120

Somerset
Schweber/NJ Electronics, (201) 469-6008

NM **Albuquerque**
Cramer/New Mexico, (505) 265-5767
Hamilton/Avnet Electronics, (505) 765-1500

NY **Buffalo**
Summit Distributors, (716) 884-3450

Farmingdale
Arrow Electronics, Inc., (516) 694-6800

Freeport
Milgray Electronics, Inc., (516) 546-6000

Hauppauge
Cramer/Long Island, (516) 231-5600

Rochester
Cramer/Rochester, (716) 275-0300
Rochester Radio Supply, (716) 454-7800
Schweber Electronics Corp., (716) 328-4180

Rome
Rome Electronics, Inc., (315) 337-5400

Westbury
Schweber Electronics, (516) 334-7474

NC **Greenboro**
Hammond Electronics of Carolina, Inc., (919) 275-6391

Winston Salem
Cramer/EW, Winston Salem, (919) 725-8711

Ohio **Beachwood**
Schweber Electronics, (216) 464-2970

Solon
Cramer Electronics, Inc., (216) 248-8400

Columbus
Hughes-Peters, Inc., (614) 294-5351

Dayton
Hamilton/Avnet Electronics, (513) 433-0610
The Stotts Friedman Co., (513) 224-1111

Okla **Tulsa**
Radio, Inc., (918) 587-9127

Pa **Philadelphia**
Herbach & Rademan, Inc., (215) 426-1700

Pittsburgh
Semiconductor Specialists, Inc., (412) 781-8120

Tenn **Memphis**
Bluff City Distributing, (901) 725-9500

Tex **Austin**
Schweber Electronics Corp., (512) 837-2890

Dallas
Hamilton-Avnet Elect., (214) 661-8661
Schweber Electronics Corp., (214) 661-5010
Sterling Electronics, (214) 357-9131

Houston
Hamilton-Avnet Elect., (713) 526-4661
Schweber Electronics Corp., (713) 784-3600
Sterling Electronics, (713) 623-6600

Utah **Salt Lake City**
Cramer/Utah, (801) 487-3681

Wash **Seattle**
Liberty Electronics/Northwest, (206) 763-8200
Robert E. Priebe Co., (206) 682-8242

Wisc **Mequon**
Taylor Electric Co., (414) 241-4321

Reticon

Reticon Corp.
910 Benicia Avenue
Sunnyvale, California 94086
(408) 738-4266
TWX: (910) 339-9343

Sales Offices & Representatives

Colo **Wheatridge**
Waugaman Associates, Inc., (303) 423-1020

Conn **Stratford**
Gerald Rosen Company, Inc., (203) 375-5456

Ill **Schaumburg**
Carvel Engineering Company, (312) 885-8800

Kans **Prairie Village**
Engineering Services, Inc., (913) 649-4000

Md **Baltimore**
Component Sales, Inc., (301) 484-3647

Mass **Framingham**
Gerald Rosen Company, Inc., (617) 879-5505

Mich **Birmingham**
J. C. Hofstetter Company, (313) 643-7203

Minn **Minneapolis**
Arjay Sales, Inc., (612) 854-4972

Mo **St. Louis**
Engineering Services, Inc., (314) 997-1515

NJ **Pennsauken**
Megargel/Himmelstein Assoc, Inc., (609) 662-3081

NY **Buffalo**
Ossman Component Sales Corp., (716) 832-4271

Huntington
CBD Enterprises, Inc., (516) 692-5200

Kingston
Ossman Component Sales Corp., (914) 338-5505

Rochester
Ossman Component Sales Corp., (716) 442-3290

Syracuse
Ossman Component Sales Corp., (315) 454-4477

Vestal
Ossman Component Sales Corp., (607) 785-9949

NC **Raleigh**
Component Sales, Inc., (919) 782-8433

Ohio **Dayton**
J. C. Hofstetter Company, (513) 296-1010

Medina
J. C. Hofstetter Company, (216) 725-4477

Tex **Dallas**
Evans & McDowell Assoc., Inc., (214) 238-7157

Houston
Evans & McDowell, (713) 783-2900

Intl **Australia, prospect**
A.J. Ferguson (Adelaide) Pty., Ltd., 269 1244

Intl **Austria, Wein**
Bacher Elektronische, Gerate G.m.b.H (0222) 83 63 96

Intl **Belgium, Bruxelles**
Inelco, (02) 660 00 12

Intl **Denmark, Copenhagen**
Scandinavian Semiconductor Supply A/S, (01) 93/Aegir 5090

Intl **England, Letchworth**
Herbert Control & Instruments Ltd., 3841 (Std Code 04626)

London
Rapid Recall, (01) 379674

Intl **Finland, Helsinki**
Havulinna Oy, (090) 661 451

Intl **France, Sevres**
Tekelec Airtronic, (01) 626 02 35

Intl **Germany, Frankfurt**
Ing Erich Sommer Elektronik G.m.b.H., (0611) 55 02 89

Munich
Opteltec, Div. Neumuller G.m.b.H., (089) 59911

Wolfratshausen
Ing Erich Sommer G.m.b.H., (08171) 15 15

Intl **Israel, Ramat-Gan**
Telsys Ltd., Electronic Engineering, 739865

Intl **Italy, Milan**
Eledra 3S SPA, (02) 34 93 041

Intl **Japan, Yokohama**
Pan Electron, Inc., 045-471-8811

Reticon (cont)

Int'l	Netherlands, Amsterdam Inelco, (020) 93 4824
Int'l	Norway, Oslo Nordisk Elektronik (Norge) A/S, (02) 55 38 93
Int'l	South Africa, Transvaal Electronic Building Elements Pty. Ltd., 78-9221/6
Int'l	Sweden, Stockholm Nordisk Elektronik AB, (08) 24 83 40
Int'l	Switzerland, Zurich Industrade AG, (01) 60 22 30

Rockwell Microelectronic Div.

Rockwell International
Microelectronic Device Division
P. O. Box 3669
3430 Miraloma Avenue
Anaheim, California 92803
(714) 632-3729

Sales Offices & Representatives

Cal	Anaheim Field Sales office, (714) 632-3729
Ga	Atlanta Field Sales Office, (404) 469-7571
Ill	Elk Grove Village Field Sales Office, (312) 439-1713
Mich	Troy Field Sales Office, (313) 576-5116
NY	Smithtown Field Sales Office (516) 979-0183

Sanken Electric Co.

Sanken Electric Company
1-22-8 Nishi-Ikebukuro
Toshima-ku, Tokyo, Japan
Cable: SANKELE TOKYO
U. S. Agent:
American Data Corp
PO Box 5228
401 Wynn Drive, N.W.
Huntsville, Alabama 35805
(205) 837-5180

SGS-ATES Semiconductor

SGS-ATES Semiconductor Corporation
435 Newtonville Avenue
Newtonville, Massachusetts 02160
(617) 969-1610
Telex: 92-2482

Specific product information:	Product Marketing Umberto Broggi
Application engineering:	Product Marketing Umberto Broggi
Literature:	Sales Department Marilyn Schribman
Place an order:	Sales Department Anne Girolamo
Follow-up an order:	Customer Service Anne Girolamo

Sales Offices & Representatives

Ala	Huntsville Rep. Inc. (205) 881-9270
Ariz	Tempe J. F. Hurlbut Co., (602) 968-5962

Cal	Santa Ana Rical Associates, (714) 557-6543 Mountain View Caltron/Pyle, (415) 964-3244
Colo	Golden J. F. Hurlbut (303) 279-7138
Fla	Clearwater Dyne-A-Mark, (813) 441-4702 Ft. Lauderdale Dyne-A-Mark, (305) 771-6501
Ga	Tucker Rep. Inc., (404) 938-4358
Ill	Bellwood Fiat Engineering, (312) 547-6200
Ind	Indianapolis Latronics, (317) 846-5788
Mass	Waltham Conti-Younger, (617) 890-4582
Mich	Grosse Pointe Park Greiner Associates, (313) 499-0188
Minn	Minneapolis Loren F. Green Associates, (612) 781-1611
Mo	Grandview Beneke & McCaul, Inc., (816) 765-2998 St. Louis Beneke & McCaul, Inc., (314) 434-6242
NJ	Ridgefield Rical Associates, (201) 945-5250
NY	Pompey S. F. Foster Co., (315) 677-3333 Webster S. F. Foster Co., (716) 265-2072
Ohio	Cleveland Imtech Inc., (216) 826-3400 Englewood Imtech Inc., (513) 836-0600
Pa	Philadelphia C.H. Newson & Associates Inc., (215) 248-3377
Tex	Dallas Blackburn Associates, (214) 692-8885
Va	Reston Boyle Associates, (703) 620-9558
Wash	Seattle Ray Johnston Co., Inc., (206) 524-5170
Can	Ottawa Multitek Inc., (613) 825-4695 Toronto Multitek Inc., (416) 429-1269
Int'l	Mexico, Mexico City Mexel (905) 575-7868

Distributors

Cal	Los Angeles Energy Electronic Products, (213) 670-7880 Santa Clara Re-Coil Electronics, Inc., (408) 984-0400
Fla	Pompano Beach Zeus Components Inc., (305) 942-4312
Ill	Des Plaines Edmar Electronics Co., 7312) 298-8580
Mass	Burlington Wilshire Electronics, (617) 272-8200 Zeus Components Inc., (617) 273-0750
NY	Bayshore Rosyl Electronics, (516) 586-1800 Elmsford Zeus Components Inc., (914) 592-4120
Ohio	Dayton Esco Inc., (513) 226-1133
Tex	Dallas KA Electronic Sales, (214) 634-7870
Wash	Seattle Radar Electric Co., (206) 282-2511
Can	Montreal Preico Electronics Ltd., (514) 389-8051
Int'l	Mexico, Mexico City Mexel (905) 575-7868

Signetics

For data on selected products see page:

Digital	384
Linear	668
Memory	787
Microprocessor	997

Signetics Corporation
811 East Arques Avenue
Sunnyvale, California 94086
(408) 739-7700
TWX: (910) 339-9283

Specific product information:

Digital	
Memory	ext. 2430
CMOS	ext. 2353
TTL	ext. 2968
ECL	ext. 2968
Analog	ext. 2460
DMOS	ext. 2748
MOS	ext. 2580
CMOS	ext. 2968

Application engineering:

DMOS	
Rus Hansen	ext. 2746
Digital	
Clement Lee	ext. 2511
MOS	
Hal Hall	ext. 3047
Chuck Merritz	ext. 2731
Dave Umari	ext. 2439
Analog	
Ted Veeches	ext. 2746

Literature:

Information Services	ext. 2982
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Price and delivery:

Sales Service	
Commercial	ext. 2236
Distributor	ext. 2667
Military	ext. 2156

Place an order:

Sales Service	
Commercial	ext. 2236
Distributor	ext. 2667
Military	ext. 2156

Follow-up an order:

Customer Sales Service	ext. 2236
NY Metropolitan Region	ext. 2623
Northeast Region	
Jim Gremmell	ext. 2623
South Atlantic	
Midwest Region	
George Schweizer	ext. 2538
Southwest Region	
Northwest Region	
Dave Young	ext. 2612

All other information:

Customer Service	ext. 2236
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Sales Offices and Representatives

Ala	Huntsville 20th Century Marketing Inc., (205) 772-9237
Ariz	Phoenix Signetics, (602) 971-2517
Cal	Encino Signetics, (213) 990-2610 Irvine Signetics, (714) 833-8980 San Diego Mesa Engineering, (714) 278-8021 Signetics, (714) 560-0242 Sunnyvale Signetics, (408) 736-7565
Colo	Denver Parker/Webster Co., (303) 770-1972
Conn	Washington Depot Kanan Associates, (203) 868-0513
Fla	Altamonte Springs Semtronic Associates, (305) 831-8233 Ft. Lauderdale Semtronic Associates, (305) 771-0010 Largo Semtronic Associates, (813) 586-1404 Pompano Beach Signetics, (305) 782-8225
Ga	Douglasville 20th Century Marketing Inc., (404) 942-6483
Ill	Rolling Meadows Signetics, (312) 259-8300

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Signetics (cont)

Ind Indianapolis
Signetics, (317) 293-4777

Kans Shawnee
Signetics, (913) 384-1711
Shawnee Mission
Buckman & Associates, (913) 722-5210
Wichita
Buckman & Associates, (316) 267-3655

Md Glen Burnie
Microcomp, Inc., (301) 761-4600
Rockville
Signetics, (301) 881-5710

Mass Lexington
Signetics, (617) 861-0840
Reading
Kanan Associates, (617) 944-8484

Mich Southfield
Signetics, (313) 559-9166 - (313) 559-9167

Minn Minneapolis
Signetics, (612) 884-7451

Mo St. Charles
Buckman & Associates, (314) 724-6690

NH Portsmouth
J.J. Theobald, Inc., (603) 731-8450

NJ Bayonne
J.J. Theobald, Inc., (201) 823-2866
Cherry Hill
Signetics, (609) 665-5071
Piscataway
Signetics, (201) 981-0123

NM Albuquerque
The Staley Co., Inc., (505) 294-2660

NY DeWitt
Tri-Tech Electronics, Inc., (315) 446-2881
East Rochester
Tri-Tech Electronics, Inc., (716) 381-2722
Great Neck
Pacent/DiBlasi - c/o J.J. Theobald, Inc. (516) 482-4040
Larchmont
Tri-Tech Electronics, Inc., (914) 834-4423
Wappingers Falls
Signetics, (914) 297-4074
Woodbury, L.I.
Signetics, (516) 364-9100

Ohio Fairview Park
Norm Case Associates, (216) 333-4120
Centerville
Norm Case Associates, (513) 443-0966

Ore Portland
Western Technical Sales, (503) 297-1711

Tex Dallas
Signetics, (214) 661-1296

Utah Salt Lake City
Parker/Webster Co., (801) 486-3737

Wash Bellevue
Western Technical Sales, (206) 641-3900

Can Downsview, Ont.
Kaytronics Ltd., (416) 638-5511
Montreal, P.Q.
Kaytronics Ltd., (514) 487-3434

Int'l Argentina/Chile,
Buenos Aires
Electronica del Atlantico SRL, 35-2624

Int'l AUSTRALIA
Melbourne
Technico Electronics, 489-9322
Sydney
Technico Electronics, 550 411

Int'l Brazil, Sao Paulo
Teleimport Eletronica Ltd., 221-3296/221-3943

Int'l Finland, Helsinki
AB Kuno Kallman Oy, 575231/575362

Int'l France, Boulogne
Signetics S A R L, 604-8127

Int'l Germany
Dusseldorf
Signetics GmbH, (0211) 244238
Hamburg
Signetics GmbH, (040) 60-35-242
Munchen
Signetics GmbH, (089) 15-20-20/15-20-29
Stuttgart
Signetics GmbH, (0711) 73-50-61

Int'l Hong Kong, Aberdeen
Enterprise Systems (Hong Kong) Ltd., 5-530141/5-531845

Int'l India/Ceylon
(Sri-Lanka)/Bangladesh
Bombay
Semiconductors Limited, 293 667

Int'l Iran, Tehran
Berkeh Company Ltd., 831564/828294

Int'l Israel, Tel Aviv
RAPAC Electronics Ltd., 477 115/116/117

Int'l Japan, Tokyo
Asahi Glass Co. Ltd., 218-5536

Int'l Korea, Seoul
Kumho & Co., Inc., 28-5271/24-3241/22-0404

Int'l Philippines, Manila
Edgeworth Marketing Corp., 406227/406569/406663

Int'l Scandinavia, Stockholm
Signetics AB, (08) 29-31-00/29-95-95

Int'l Singapore/Malaysia
Singapore
General Engineers Corp. Pte. Ltd., 333641/333651/321791

Int'l Sweden
Gothenburg
AB Kuno Kallman, 80-30-20
Stockholm
AB Kuno Kallman, (08) 67-17-11/67-15-95

Int'l Switzerland, Zurich
Omni Ray AG, (01) 34-07-66

Int'l Taiwan R.O.C., Taipei
Dynatek Corporation, 713-362

Int'l Thailand/Laos,
Bangkok
Saeng Thong Radio L.P., 527195/519763

Int'l United Kingdom, London
Signetics International Corp., 01-659 2111

Int'l Venezuela/Panama
Caracas
Instrulab C.A., 614138/614558

Distributors

Ala Huntsville
Hamilton/Avnet Electronics, (205) 533-1170

Ariz Phoenix
Hamilton/Avnet Electronics, (602) 275-7851
Kierulff Electronics, (602) 273-7331

Cal Culver City
Hamilton Electro Sales, (213) 558-2131
El Segundo
Liberty Electronics, (213) 322-8100
Los Angeles
Kierulff Electronics, (213) 685-5511
Mt. View
Hamilton/Avnet Electronics, (415) 961-7000
Palo Alto
Kierulff Electronics, (415) 968-6292
San Diego
Hamilton/Avnet Electronics, (714) 279-2421
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Ossman Component Sales, (914) 338-5505
Rochester
Ossman Component Sales, (716) 442-3290
Syracuse
Ossman Component Sales, (315) 454-4477
Vestal
Ossman Component Sales, (607) 785-9949

NC Winston Salem
Burgin-Kreh Assoc., (919) 768-4174

Ohio Cincinnati
Sheridan Assoc., (513) 761-5432

Penn Pittsburgh
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Tex Dallas
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Houston
Mark Kruvand Co. Inc.,
Lynchburg
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SDR², (206) 747-9424

Can Mississauga, Ontario
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Dollrd Os Ormeaux, Que
R.F.Q. Ltd., (514) 626-8324

Intl Australia, Adelaide SA
A.J. Ferguson Pty. Ltd., 516895

Intl France, Sevres
Tekelec-airtronic

Intl Israel, Jerusalem
Carmira, 02-281-051

Intl Japan, Tokyo
Tejin-Tapco, (506) 4670-3

Intl W. Germany, Frankfurt
EEP, 0611-550289

Distributors

Cal Culver City
Nesco, (213) 389-6239

Ill Skokie
Mar-Con Sales, (312) 675-6450

Md Baltimore
Tully Electronics, (301) 788-4200

Mass Stoneham
Nasco, (617) 438-7133

Mich Farmington
Sheridan Sales, (800) 582-7027
Florissant Mo
Sheridan Sales, (314) 837-5200

NY Buffalo
Ossman Component Sales, (607) 785-9949
Forest Hills
Nasco, (212) 793-6500
Kingston
Ossman Component, (914) 338-5505
Rochester
Ossman Component Sales, (716) 442-3290
Syracuse
Ossman Component Sales, (315) 454-4477
Vestal
Ossman Component Sales, (607) 785-9949

Ohio Cincinnati
Sheridan Sales, (800) 582-7027

Penn Pittsburgh
Sheridan Sales, (412) 294-1640
Toronto, Ont. Can
Westburne, (416) 789-4181
Montreal, P Q
Future Electronics, (514) 735-5775

Intl Australia, Adelaide SA
A.J. Ferguson Pty Ltd., 516895

Intl France, Sevres
Tekelec-Airtronic

Intl Japan, Tokyo
Teijin Tapco, (506) 4670-3

Intl W. Germany, Frankfurt
EEP, 0611-550289

Solid State Scientific

Solid State Scientific, Inc.
Montgomeryville Industrial Center
Montgomeryville, Pennsylvania 18936
(215) 855-8400
TWX: (510) 661-7267

All other information:
All inquiries: Sales Department

Sales Offices & Representatives

Cal El Segundo
Varigon Assoc. (213) 679-0621
Mountain View
Thresum Assoc., (415) 965-9180
San Diego
Littlefield & Smith Assoc., (714) 277-8044

Colo Denver
Lindberg, Co., (303) 758-9033

Fla Casselberry
EIR Inc., (305) 830-9600
Maitland
Delmac Sales, (305) 644-2526

Ill Rolling Meadows
Solid State Scientific, (312) 253-2390
Sumer Inc., (312) 394-4900

Ind Indianapolis
Delesa, (317) 894-3778

Kan Lenexa
Palatine Sales, Inc., (913) 492-7020

NY Pittsford
T-Squared Electronics, (716) 381-2551
Syracuse
T-Squared Electronics, (315) 463-8592

Tex Richardson
Semiconductor Sales Inc., (214) 231-6181

Utah Salt Lake City
Lindberg Co., (801) 534-1500

Can Montreal, Quebec
Penryn Electronics, (514) 735-2107

Distributors

Ariz Phoenix
Sterling Electronics, (602) 258-4531

Cal Fullerton
Zeus Components, (714) 871-0391
San Carlos
Sterling Electronics, (415) 592-2353
San Diego
Sterling Electronics, (714) 565-2441
Santa Clara
Re-Coil, (408) 984-0400
Sun Valley
Sterling Electronics, (213) 767-5030
Woodland Hills
Semiconductor Concepts, (213) 884-4560

Colo Wheatridge
Century Electronics, (303) 424-1985

Ind Indianapolis
Advent Electronics, (317) 297-4910
Pioneer/Indiana, (317) 849-7300

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Hallmark Electronics, (301) 365-8500
Gaithersburg
Pioneer/Washington, (301) 948-0710

Mass Burlington
Zeus/New England, (617) 273-0750
Holliston
Diplomat/New England, (617) 429-4120

Minn Bloomington
Hallmark Electronics, (612) 884-9056

NM Albuquerque
Sterling Electronics, (505) 345-6601

Pa Erie
Advacom Inc., (814) 455-8110
Horsham
Pioneer/Philadelphia, (215) 674-7510

Utah Salt Lake City
Century Electronics, (801) 487-8551

Wash Seattle
Sterling Electronics, (206) 762-9100

Solitron Devices

Solitron Devices, Inc.
Semiconductor Division
8808 Balboa Avenue
San Diego, California 92123
(714) 278-8780
TWX: (910) 335-1221

Sprague Electric Co.

Sprague Electric Company
Semiconductor Division
115 Northeast Cutoff
Worcester, Massachusetts 01606
(617) 853-5000
Telex: 920467

Specific product information:

(413) 664-4411 ext. 2424
Automotive B. Marshall
Consumer R. Milewski
Camera B. Marshall
Digital G. Tully
Transistor Arrays G. Tully
Operational Amplifiers G. Tully
Display Drivers P. Emerald
Mos G. Tully

Application engineering:
Same as Above

Literature:
647 Marshall Street, North Adams, Massachusetts 01247, (413) 664-4411 ext. 2572

Price and delivery:
Same as Product Information

Place an order:
Same as Above

Follow-up an order:
Same as Above

Sales Offices & Representatives

Contact these offices for names of distributors

Ala Decatur
Southeastern Distributors Supply Co., (205) 353-3615
Huntsville
Sprague Electric Co., (205) 883-0520

Ariz Phoenix
Zeus/KCE, (602) 951-1362
Tempe
Sprague Electric Co., (602) 279-5435

Cal Burlingame
William J. Purdy Co., (415) 347-7701
Encino
KCE Corporation, (213) 990-0511
Inglewood
Sprague Electric Co., (213) 649-2600
Los Angeles
KCE Corporation, (213) 649-2622
Sacramento
William J. Purdy Company, (916) 422-0128
San Diego
KCE Corporation, (714) 278-7640

Colo Denver
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Conn Trumbull
Sprague Electric Co., (203) 261-2551

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Sprague Electric Co., (Gov't sales only) (202) 244-6006

Fla Ft. Lauderdale
UniRep, Inc., (305) 527-1556
Longwood
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Hi Honolulu
Hawaii Electronics Sales, (808) 845-8207

Ill Chicago
D. Dolin Sales Co., (312) 286-6200
Schiller Park
Sprague Electric Co., (312) 678-2262

Ind Indianapolis
Sprague Electric Co., (317) 253-4247
Mulberry
Maish Sales, (317) 638-8484 (For Indianapolis)
Maish Sales, (317) 296-2322 (For Mulberry Area)

Mass North Adams
Sprague Electric Co., (413) 664-4411
Waltham
Sprague Electric Co., (617) 899-9840

Mich Jackson
Sprague Electric Co., (517) 787-3934

Minn Minneapolis
HMR, Inc., (612) 920-8200

Mo Kansas City
Nevco, Inc., (816) 421-1751
St. Louis
Nevco, Inc., (314) 843-7406

NJ Cherry Hill
Sprague Electric Co., (609) 795-2299
Trinkle Sales Inc., (609) 795-4200
Cranford
G. G. Burnett, (914) 698-8600
Wayne
Sprague Electric Co., (201) 696-8200

NM Albuquerque
William J. Purdy Co., (505) 266-7959

NY Mamaroneck
William Rutt, Inc., (914) 698-8600
Melville
Sprague Electric Co., (516) 549-4141
Syracuse
Mar-Com Associates, (315) 437-2843
Paston-Hunter Co., Inc., (315) 437-2992
Sprague Electric Co., (315) 437-7311

NC Winston-Salem
Electronic Marketing Asso., (919) 722-5151

Ohio Beachwood
Electronic Salesmasters, Inc., (216) 831-9555
Sprague Electric Co., (216) 464-7540
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Sprague Electric Co., (513) 278-0781

SC Greenville
Electronic Marketing Assoc. Inc., (803) 268-1125

Tex Arlington
EMC, Inc., (817) 261-8424
Dallas
Lund & Company, Inc., (214) 387-4634
Richardson
Sprague Electric Co., (214) 235-1256

Va Lexington
Sprague Electric Co., (703) 463-9161

Wash Seattle
Fleehart & Sullivan, Inc., (206) 522-1533
Sprague Electric Co., (206) 632-7761

Can Montreal, P.Q.
Sprague Electric of Canada, (514) 747-7811
Toronto, Ont.
Sprague Electric of Canada, (416) 766-6123

Intl Belgium, Ronsse (Renaix)
Sprague-Benelux, 215.351 (055)

Intl England, Yiewsley
Sprague Electric (U.K.) Ltd., 44627

Intl France, Bagneux
Sprague France S.A.R.L., 1-655 19 19

Intl Germany, Frankfurt
Sprague G.m.b.H., 0611-439407

Intl Hong Kong,
Sprague World Trade Corp., 5-626231-4

Intl Italy
Milan
Sprague-Italiana, S.p.A., 02-47 91 21
Rome
Sprague-Italiana S.p.A., 06-83 33 69

Intl Switzerland, Geneva
Sprague World Trade Corp., 98-4021

Intl Taiwan, Taipei
Sprague Taiwan Corp., 7310748

Stewart-Warner Microcircuits

Stewart-Warner Microcircuits
730 East Evelyn Avenue
Sunnyvale, California 94086
(408) 245-9200
TWX: (910) 339-9210

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- Ariz** Scottsdale
De Angelo, Rothman & Cheever, Inc., (602) 948-2240
- Cal** El Segundo
Varigon Associates, (213) 679-0621
Los Altos
PM Sales, (415) 941-4444
San Diego
Varigon Associates, (714) 299-5413
- Colo** Wheatridge
Waugaman Associates, Inc., (303) 432-1020
- Conn** Meriden
Com-Sale, (203) 634-0179
- Ill** Chicago
LGS Electronics, (312) 456-9616
- Ind** Fort Wayne
G&D Electronic Sales, Inc., (219) 432-5585
- Mass** Waltham
Com-Sale, (617) 890-0011
- Mich** Farmington
Carter McCormic & Peirce, Inc., (313) 477-7700
- Minn** Minneapolis
S&R Component Sales, (612) 544-3022
- Mo** Hazelwood
Dy-Tronix, Inc., (314) 731-5799
- NY** Jamaica
SJ Sales Associates, (212) 291-3232
- Ohio** Chagrin Falls
Crest Component Sales, (216) 543-9808
- Pa** King of Prussia
Monteiro Associates, Inc., (215) 265-0634
- Tex** Dallas
Evans McDowell Associates, (214) 238-7157
Houston
Evans McDowell Associates (713) 783-2900
- Wash** Bellevue
SD-R², (206) 747-9424

Distributors

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Powell Electronics, (205) 539-2731
- Ariz** Phoenix
Intermark Electronics, (602) 263-9500
- Cal** Mountain View
Powell Electronics, (415) 964-0820
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Intermark, (714) 279-5200
Santa Ana
Intermark, (714) 540-1322, (213) 436-5275
Sunnyvale
Intermark, (408) 738-1111
Woodland Hills
Semiconductor Concepts, (213) 884-4560
- Colo** Denver
Intermark, (303) 936-8284
- Conn** Fairfield
U-Tronics, (203) 255-4521
Hamden
Wilshire Electronics, (203) 281-1166
- Fla** Miami
Lykes Electronics, (305) 633-8535
Miami Springs
Powell Electronics, (305) 592-3260
Orlando
Powell Electronics, (305) 859-1450
Tampa
Lykes Electronics, (813) 886-6646
- Ga** Atlanta
Lykes Electronics, (404) 355-2223
- Ill** Skokie
Bell Electronics, (312) 965-7500

- Ill** Westmont
Bodelle Co., Inc., (312) 323-9670
- La** New Orleans
Lykes Electronics, (504) 486-7441
- Md** Beltsville
Powell Electronics, (301) 937-4030
- Mass** Burlington
Wilshire Electronics, (617) 272-8200
Dedham
Gerber Electronics, (617) 329-2400
West Newton
A. W. Mayer, (617) 965-1111
- Mich** Ann Arbor
Wedemeyer Electronic Supply, (313) 665-8611
Farmington
Diplomat/Northland Electronics, (313) 477-3200
- Minn** Minneapolis
Electro-Com Corporation, (612) 788-8601
Industrial Components, Inc., (612) 831-2666
- NJ** Cinnaminson
Wilshire Electronics, (609) 786-8990
- NY** Elmsford
Zeus Components, (914) 592-4120
Farmingdale
Harrison Electronics Corporation, (516) 293-7990
Johnson City
Wilshire Electronics, (607) 797-1236
- NC** Winston Salem
Kirkman Electronics, (919) 724-0541
- Ohio** Dayton
Stotts Freidman, (513) 224-1111
- Pa** Philadelphia
Powell Electronics, (215) 365-1900
Pittsburgh
RPC, (412) 782-3770
- Tex** Dallas
KA Electronic Sales, (214) 634-7870
Houston
Lenert Company, (713) 225-1465
- Utah** Salt Lake City
Alta-Land Electronics, (801) 486-7227
- Wash** Seattle
Intermark, (206) 767-3160
Zepher Electronics, (206) 242-2517, (206) 243-0224

Synertek

Synertek
3050 Coranado Drive
Santa Clara, California 95051
(408) 241-4300

All other information:
All Information: Jack Balletto

Sales Offices & Representatives

- Ariz** Phoenix
R.R. Sales, (602) 959-5150
- Cal** Los Angeles
Relcom, (213) 822-1187
Mountain View
Thresum Associates, (415) 965-9180
- Conn** Danbury
C.P.S. Corporation, (203) 795-3515
- Fla** Hollywood
R.C. Simon, (305) 941-2757
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- Mass** Waltham
Synasel Assoc., (617) 890-6777
- Mich** Detroit
Kent & Associates, (313) 651-1006
- Minn** Bloomington
Electronic Innovators, (612) 884-7471
- NJ** Camden
Sunday O'Brien, (609) 429-4013
- NY** Garden City
Comtron Assoc., (516) 741-8966
Syracuse
Honsinger Assoc., (315) 463-5718

- Tex** Dallas
Mark Kruvad Co., (214) 691-4592
Houston
Mark Kruvad Co., (713) 661-3007

Teledyne Crystalonics

Teledyne Crystalonics
147 Sherman Street
Cambridge, Mass. 02140
(617) 491-1670

Teledyne Philbrick

Teledyne Philbrick
Allied Drive at Route 128
Dedham, Massachusetts 02026
(617) 329-1600
TWX: (710) 348-6726

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Zeus, Inc., (602) 258-7519
- Cal** Del Mar
T. Louis Snitzer Co., (714) 454-2191
Los Angeles
T. Louis Snitzer Co., (213) 836-6170
Redwood City
James S. Heaton Co., (415) 369-4671
- Colo** Denver
PLS Associates, Inc., (303) 773-1218
- Fla** Largo
Col-Ins-Co., (813) 581-8233
Orlando
Col-Ins-Co., (305) 423-7615
- Hawaii** Kailua
Lanikai Electronics, (808) 262-6286
- Ill** Chicago
Data Electronics Co. (312) 283-0300,
- Kans** Mission
Mid-West Marketing, (913) 384-3737
- Md** Kensington
Electronic Marketing Associates, (301) 881-5300
- Mass** Burlington
Tekdata Manufacturer's Rep., (617) 273-0198
- Mich** Farmington
Carter, McCormic & Peirce, Inc., (313) 477-7700
- Minn** Minneapolis
Electronic Innovators, Inc., (612) 884-7471
- Mo** Florissant
Mid-West Marketing, (314) 831-0342
- NM** Albuquerque
Zeus, Inc., (505) 256-9831
- NY** Elmont
Crane & Egert Corp., (516) 488-2100
N. Syracuse
KLM Associates, (315) 458-6214
Rochester
KLM Associates, (716) 442-0820
Utica
KLM Associates, (315) 735-8525
- NC** Raleigh
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- Ohio** Cleveland
Carter, McCormic & Peirce, Inc., (216) 333-5650
Dayton
Carter, McCormic & Peirce, Inc., (513) 278-5873
- Okla** Norman
Data Marketing Associates, (405) 364-8320
- Pa** King of Prussia
Electronic Marketing Associates, (215) 265-1600, (215) 248-5050

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Carter, McCormick & Peirce, Inc., (412) 824-3760

SC Myrtle Beach
The Candor Company, Inc., (803) 448-8361

Tenn Chattanooga
The Candor Company, Inc., (615) 894-7454

Tex Dallas
Data Marketing Associates, (214) 661-0300
Houston
Data Marketing Associates, (713) 686-9627
San Antonio
Data Marketing Associates, (512) 828-0937

Utah Salt Lake City
Zeus, Inc., (801) 486-2317

Wash Seattle
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Cesco Electronics Ltd., (416) 661-0220
Montreal, P.Q.
Cesco Electronics, Ltd., (514) 735-5511
Ottawa, Ont.
Cesco Electronics, Ltd., (613) 729-5118
Quebec, P.Q.
Cesco Electronics, Ltd., (418) 524-4641
Vancouver, B.C.
Intek Electronics, Ltd., (604) 324-6831

Int'l Argentina, Buenos Aires
Sirex 42-1927, 44-5781

Int'l Australia
Brookvale, N.S.W.
Elmeasco Instruments Pty. Ltd., 939 7944
Victoria
Elmeasco Instruments Pty. Ltd., 266 658

Int'l Austria, Vienna
Kontron GmbH & Co. KG, 94 56 46

Int'l Belgium, Brussels
Simac Electronics SPRL, (6) 72.45.56
Teledyne Philbrick, 673 99 88

Int'l Brazil, Sao Paulo
Setpoint S/A Comercio E Importacao, 288-3834

Int'l Chile, Santiago
Sirex, 39-5752, 3-4455

Int'l Denmark, Lyngby
Knud Kamuk A/S, (01) 88 38 33

Int'l Finland, Kauniainen
Findip A.B., 90-502255

Int'l France, Paris
Teledyne Philbrick France, (1) 577 95 69

Int'l Germany, Wiesbaden
Teledyne GmbH, (06121)-39171

Int'l Greece, Athens
Demetrius C. Tzitzinias, 287783, 281049, 283311

Int'l Hong Kong, Hong Kong
Schmidt & Co., Ltd., 240168, 232735

Int'l India, Bombay
Electronic Enterprises, 353069, 375376

Int'l Ireland
Belfast
Neltronic Ltd., 36521/2
Dublin
Neltronic Ltd., 501845

Int'l Israel, Gamat Gan
Elina Ltd., (03) 734129

Int'l Italy, Milan
Eledra 3S SPA, 34.93.041

Int'l Japan
Osaka
Teledyne Philbrick Japan, (06) 364-8712,2,3,4
Tokyo
Teledyne Philbrick Japan, 403-8921

Int'l Korea, Seoul
Korea Un Trading Corp., 76-2502, 76-2501

Int'l Netherlands, Steensel
Simac Electronics b.v., (04970)-2011

Int'l New Zealand, Auckland
Professional Electronics, Ltd., 491-609

Int'l Nigeria, Lagos
DeeMTee Electronics, Ltd.,

Int'l Iran, Tehran
Berkeh Company, Ltd., 828294, 831564

Int'l Norway, Oslo
Scancopter a.s., 69-44-90, 55-11-96

Int'l Pakistan, Karachi
Syed Traders, 45363

Int'l Portugal, Lisbon
Ditram Components e Electronica, Lda., 45313

Int'l South Africa, Transvaal
K. Baker Associates Pty. Ltd., 42-1939, 42-2043

Int'l Spain, Madrid
Hispano Electronica S.A., 233 1601 T

Int'l Sweden, Jarfalla
Scancopter AB, 0758-37440

Int'l Switzerland, Zurich
Kontron Electronic Ltd., 01/62 82 82

Int'l Taiwan, Taipei
Industrial Electronics, 774 257

Int'l U.K., Cranford
Teledyne Philbrick U.K., (01) 897-2501

Int'l West Indies,
Miami, Fla
West Indies Sales Co., Ltd., (305) 592-8188

Teledyne Semiconductor

Teledyne Semiconductor
1300 Terra Bella Avenue
Mountain View, California 94043
(415) 968-9241
TWX: (910) 379-6494

Specific product information:

Digital Marketing
Linear Marketing

Application engineering:

See Product Information

Literature:

Literature Center

Price and delivery:

See Product Information

Place an order:

Local Field Sales Office or Order Entry

Follow-up an order:

Customer Service for (Product)

All other information:

Marketing Services

Sales Offices and Representatives

Ala Huntsville
EMA, (205) 837-6061

Ariz Tempe
Sedco Sales, Inc., (602) 968-7791

Cal Escondido
Cirolia Electronic Sales, (714) 743-3015
Los Angeles
Teledyne Semiconductor, (213) 826-6639
Mountain View
Teledyne Semiconductor, (415) 965-1455
Redwood City
James S. Heaton Co., Inc., (415) 369-4671
Santa Ana
Rical Associates, (714) 557-6543

Colo Wheat Ridge
Waugaman Associates, (303) 423-1020

Fla Maitland
Hutto Hawkins Peregoy, Inc., (305) 831-2474
Pompano Beach
Hutto Hawkins Peregoy, Inc., (305) 943-9593

Ill Des Plaines
Teledyne Semiconductor, (312) 299-6196
Westchester
Gassner & Clark Co., (312) 345-4245

Ind Fort Wayne
The Given Corporation, G & D Electronic Sales, (219) 432-5585

Iowa Cedar Rapids
Penzner-Mankus Corp., (319) 362-9177

Kan Overland Park
Penzner-Mankus Corp., (913) 381-0004
Wichita
Penzner-Mankus Corp., (316) 264-2662

Md Baltimore
Burgin-Kreh Associates, Inc., (301) 788-5200
Towson
Teledyne Semiconductor, (301) 825-1920

Mass Waltham
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Mich Ann Arbor
A.P. Associates, (312) 971-8870

Minn Minneapolis
Teledyne Semiconductor, (612) 888-0540

Mo Hazelwood
Penzner-Mankus Corp., (314) 731-4334

NH Salem
Teledyne Semiconductor, (603) 893-9551

NJ Haddonfield
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NM Albuquerque
The Thorson Co., (505) 265-5655

NY Buffalo
Bowser & Sapecky Associates, (716) 839-4170
Manlius
Bowser & Sapecky Associates, (315) 682-8885
Mount Vernon
Friedman-Smith Electronic Sales, Inc., (914) 664-4866
Stony Brook
Teledyne Semiconductor, (516) 751-5640

NC Winston-Salem
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Ohio Dayton
Neal Bear Corp. - Bear Marketing, (513) 299-3566
Richfield
Neal Bear Corp. - Bear Marketing, (216) 659-3131

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Evans-McDowell Associates, (214) 238-7157
Houston
Evans-McDowell Associates, (713) 783-2900

Utah Salt Lake City
Waugaman Associates, Inc., (801) 277-8911

Va Lynchburg
Burgin-Kreh Associates, (804) 845-5600

Wash Bellevue
SD.R², (206) 747-9424

PR Santurce
E. Franceschini Associates, (809) 726-0225

Can Ottawa, Ont.
Cantec Representatives, (613) 225-0363

Int'l England,
Hounslow, Middlesex
Teledyne Semiconductor (44) 01-897-2503

Int'l Hong Kong, Kowloon
Teledyne Semiconductor, 3-240122

Int'l Japan, Tokyo
Teledyne Semiconductor, 03-405-5738

Int'l Singapore
Kallang Bahru Ind. Est
Teledyne Semiconductor, 2582811

Int'l West Germany
Tiengen
Teledyne Semiconductor, 7741-5066
Wiesbaden
Teledyne Semiconductor, 06121-39171

Distributors

Ala Huntsville
Powell Electronics, (205) 539-2731

Cal Chatsworth
Westates Electronics Corp., (213) 341-4411
Los Angeles
Kierulff Electronics Co., Inc., (213) 685-5511
Newport Beach
SemiComp Corporation, (714) 833-3070
Riverside
Electronic Supply, (714) 683-8110
San Diego
Intermark Electronics, (714) 279-5200
Kierulff Electronics Co., Inc., (714) 278-2122
Santa Ana
Intermark Electronics, (714) 540-1322
Sunnyvale
Intermark Electronics, (408) 738-1111
Woodland Hills
Semiconductor Concepts, (213) 884-4560

Colo Wheat Ridge
Century Electronics, (303) 424-1985

Conn Norwalk
Harvey Electronics, (203) 853-1515

Fla Clearwater
Diplomat/Southland Electronics, Inc., (813) 443-4514
Ft. Lauderdale
Newark Electronics, (305) 587-2372
Orlando
Hammond Electronics, (305) 849-6060
Pompano Beach
Zeus Components, Inc., (305) 942-4312

Ill Rosemont
Advent Electronics, (312) 298-4210

Teledyne Semiconductor (cont)

Ill Skokie
Bell Industries, (312) 965-7500

Md Baltimore
Technico, Inc., (301) 828-6416
Gaithersburg
Kierulff Electronics Co., Inc., (301) 948-0250
Savage
Pyttronic Industries, Inc., (301) 792-7000

Mass Burlington
Milgray Electronics, (617) 272-6800
Dedham
Gerber Electronics, (617) 329-2400
Frammingham
Future Electronics, (617) 879-0860

Mich Ann Arbor
Cadence Electronics, (617) 879-3000
Advent Electronics, (313) 769-8650
Farmington
Diplomat/Northland, (313) 477-3200

Mich Livonia
Rep-tron, Inc., (313) 525-2700

Minn Minneapolis
Electro-Com Corp., (612) 788-8601

NJ Clifton
Wilshire Electronics, (201) 365-2600
Moorestown
Arrow/Angus, (609) 235-1900

NM Albuquerque
Century Electronics, (505) 292-2700

NY Buffalo
Summit Distributors, Inc., (716) 884-3450
Elmsford
Zeus Components, Inc., (914) 592-4120
Hauppauge, L.I.
Semiconductor Concepts, (516) 273-1234
Johnson City
Wilshire Electronics, (607) 797-1236
New Hyde Park, L.I.
Lafayette Industrial Elec., (516) 488-6600
Rochester
Summit Electronics of Rochester, Inc., (716) 334-8110

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Pioneer/Cleveland, (216) 587-3600
Columbus
Electronics Marketing Corp., (614) 299-4161
Dayton
Pioneer/Dayton, (513) 236-9900

Pa Montgomeryville
Pyttronic Industries, Inc., (215) 643-2850
Philadelphia
Almo Electronics, (215) 698-4021

Tex Dallas
Component Specialties, (214) 357-4576
Solid State Electronics, (214) 352-2601
Houston
Component Specialties, (713) 771-7237
Solid State Electronics, (713) 785-5205

Utah Salt Lake City
Diplomat/Alta Electronics, (801) 486-7227

Wash Seattle
Intermark Electronics, (206) 767-3160

Can Montreal, P.Q.
Future Electronics, (514) 735-5775
Rexdale, Ont.
Future Electronics, (416) 677-7820
Scarborough, Ont.
Carsten Electronics, (416) 751-5095
Vancouver, B. C.
Bowtek Electric Co. Ltd., (604) 736-1141
R-A-E, (604) 687-2621

Intl Australia
Victoria
Austronic Engineering Labs, Pty. Ltd., 387-1477
Prospect
A.J. Ferguson (Adelaide) Pty. Ltd., 269-1244

Intl Belgium, Brussels
Sobelab Electronics S.A., 673-9055

Intl Denmark, Herlev
A/S Nordisk Elektronik (45) (1) 969596

Intl Finland, Helsinki
Yleiselektronikka Oy, 578922

Intl France, Sevres
Tekelec Airtronic, (8) 626-0235

Intl Germany
Bremen
Arthur Behren VDI, (49) (410) 343022

Intl Hannover
Theo Henskes,
(49) (511) 440213
Nettetal
Omni Ray GmbH, (49) (2153) 4548
Ottoeburn
Hot Electronic
Vertreibe GmbH & Co. KG,
Unterhaching
Metronik GmbH, (49) (811) 615560

Intl Holland, Barneveld
Ritro Electronics N.V. 03420 5041

Intl India, New Delhi
Continental Device India, Ltd., 392784

Intl Israel, Tel Aviv
STG International Ltd., (10) 53459

Intl Italy
Milan
Mesa, S.P.A., (39) (2) 3491040
Tekelec Airtronic S.P.A., (39) (2) 738.56.74

Intl Japan
Tokyo
KH Electronics Corporation, 584-6395, 584-7111
O.S. Seidi Company, Ltd., 255-6051
Takachiho Koheki Company, 263-3211
Teijin Advance Products Corporation, (506) 4670-3
Towa Denshi Company, Ltd., 0422-31-3211

Intl Norway, Oslo
Nordisk Elektronik, (47) (2)55.38.93

Intl Singapore, Singapore
Techco (Private) Ltd., 2588663, 2587390

Intl So. Africa, Johannesburg
Impectron Pty. Ltd., 22-1386, 28-7856

Intl Spain, Madrid
Payma S.A., (34) (1) 215.39.41

Intl Sweden, Stockholm
Nordisk Elektronik AB (46) (8) 24.83.40

Intl Switzerland
Zurich
Omni Ray AG, (41) (57) 54665
Mutshellen
W. Stolz A.G.

Intl Taiwan, Taipei
Mardel 563155-6

Intl United Kingdom
Hitchin
Double R. Electronics
Slough
G.D.S. Sales, Ltd., Slough
Macro-Marketing Ltd., (44) (753) 35444

Texas Instruments

Texas Instruments Incorporated
Semiconductor Group
P.O. Box 5012
Dallas, Texas 75222
(214) 238-2011
TWX: (910) 867-4702

Specific product information:
Digital Circuits
Houston, Texas (713) 494-5115 ext. 2734
MOS
Houston, Texas (713) 494-5115 ext. 2821
Special Products
Dallas, Texas
Low Power
Low Power Schottky
CMOS (214) 238-2011 ext. 4841
Consumer Circuits
Lubbock, Texas (806) 762-8831 ext. 51
Linear Circuits
Dallas, Texas (214) 238-2011 ext. 3865
Advanced Circuits
ECL
Sherman, Texas (214) 893-5166 ext. 303

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Ariz Phoenix
Field Sales Office, (602) 248-8028

Cal San Diego
Field Sales Office, (714) 279-2622
Santa Ana
Field Sales Office, (714) 835-9031
Sunnyvale
Field Sales Office, (408) 732-1840

Colo Denver
Field Sales Office, (303) 750-4100

Conn Hamden
Field Sales Office, (203) 281-0074

Fla Ft. Lauderdale
Field Sales Office, (305) 566-3294

Ga Atlanta
Field Sales Office, (404) 458-7791

Ill Glenview
Field Sales Office, (312) 729-5710

Ind Ft. Wayne
Field Sales Office, (219) 484-0606
Indianapolis
Field Sales Office, (317) 248-8555

Mass Waltham
Field Sales Office, (617) 890-7400

Mich Southfield
Field Sales Office, (313) 353-0830

Minn Edina
Field Sales Office, (612) 835-2900

NJ Clark
Field Sales Office, (201) 574-9800

NM Albuquerque
Field Sales Office, (505) 265-8491

NY East Syracuse
Field Sales Office, (315) 463-9291
Endicott
Field Sales Office, (607) 785-9987
Fishkill
Field Sales Office, (914) 896-6793
Rochester
Field Sales Office, (716) 461-1800

NC High Point
Field Sales Office, (919) 869-3651

Ohio Dayton
Field Sales Office, (513) 253-6128

Ore Beaverton
Field Sales Office, (503) 643-6750

Pa Ft. Washington
Field Sales Office, (215) 643-6450

Tex Dallas
Field Sales Office, (214) 238-6805
Houston
Field Sales Office, (713) 785-6906

Va Arlington
Field Sales Office, (703) 527-2800
Richmond
Field Sales Office, (804) 320-3830

Wash Bellevue
Field Sales Office, (206) 455-3480

Can Montreal, P.Q.
Field Sales Office, (518) 561-1900
Toronto, Ont.
Field Sales Office, (716) 856-4453

Distributors

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Cramer Huntsville, (205) 539-5722, Ext. 475
Hall-Mark Electronics, (205) 539-0691

Ariz Phoenix
Cramer Phoenix, (602) 263-1112
R. V. Weatherford Co., (602) 272-7144

Cal Anaheim
R. V. Weatherford Co., (714) 633-9633
Glendale
R. V. Weatherford Co., (213) 849-3451
Goleta
Radio Product Sales, (805) 964-6823
Irvine
Cramer Los Angeles, (714) 979-3000
Los Angeles
Kierulff Electronics, (213) 685-5511
Radio Product Sales, (213) 748-1271
Mountain View
Time Electronics, (415) 965-8000
Palo Alto
Kierulff Electronics, (415) 968-6292
R. V. Weatherford Co., (415) 493-5373
Pomona
R. V. Weatherford Co., (714) 623-1261

Texas Instruments (cont)

Cal **San Diego**
Cramer San Diego, (714) 565-1881
Radio Product Sales, (714) 292-5611
R. V. Weatherford Co., (714) 278-7400

Sunnyvale
Cramer San Francisco, (408) 739-3011
TI Supply Company, (408) 732-5555

Colo **Denver**
Cramer/Denver, (303) 758-2100
TI Supply Company, (303) 757-7671

Englewood
R. V. Weatherford Co., (303) 761-5432

Conn **Hamden**
Arrow Electronics, (203) 248-3801

North Haven
Cramer Connecticut, (203) 239-5641

Fla **Hollywood**
Cramer Hollywood, (305) 923-8181

Orlando
Cramer Orlando, (305) 894-1511, Ext. 563
Hall-Mark Electronics, (305) 855-4020

Ga **Atlanta**
Cramer Atlanta, (404) 448-9050, Ext. 497

Ill **Arlington Heights**
TI Supply Company, (312) 593-7660

Chicago
Newark Electronics Corp., (312) 638-4411
Semiconductor Specialists, (312) 279-1000

Elk Grove Village
Hall-Mark Electronics, (312) 437-8800

Mt. Prospect
Cramer Chicago, (312) 593-0230, Ext. 376

Ind **Indianapolis**
Esco Electronics, (317) 888-5373
Graham Electronics, (317) 634-8202

Iowa **Cedar Rapids**
Deeco Incorporated, (319) 365-7551

Md **Baltimore**
Arrow Electronics, (202) 737-1700
Technico Incorporated, (301) 828-6416

Gaithersburg
Cramer Washington, (301) 948-0110, Ext. 485

Hyattsville
Milgray/Washington, (301) 864-1111

Mass **Billerica**
Kierulff Electronics, (617) 667-8331

Boston
DeMambo Electronics, (617) 787-1200

Burlington
Arrow Electronics, (617) 273-0100

Newton
Cramer Newton, (617) 969-7700

Waltham
TI Supply Company, (617) 890-0510

Mich **Detroit**
Newark Electronics Corp., (313) 548-0250

Livonia
Cramer Detroit, (313) 425-7000

Wyoming
Newark Electronics Corp., (616) 241-6681

Minn **Edina**
Cramer Bonn Minnesota, (612) 835-7811
TI Supply Company, (612) 835-5353

Minneapolis
Newark Electronics Corp., (612) 331-6350
Semiconductor Specialists, (612) 845-8841

Mo **Kansas City**
Semiconductor Specialists, (816) 452-3900

N. Kansas City
Lcomp-Kansas City, (816) 221-2400

St. Louis
Lcomp-St. Louis, (314) 647-5505
Semiconductor Specialists, (314) 428-6100

NJ **Camden**
General Radio Supply Co., (609) 964-8560

Cherry Hill
Cramer Pennsylvania, (215) 923-5950 (609) 424-5993
Milgray/Delaware Valley, (609) 424-1300 (Phila.) (215) 228-2000

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TI Supply Company, (201) 382-6400

Moonachie
Cramer New Jersey, (201) 935-5600

Moorestown
Arrow Electronics/Angus, (215) 928-1800

Saddlebrook
Arrow Electronics, (201) 797-5800

NM **Albuquerque**
Cramer Albuquerque, (505) 265-5767
R. V. Weatherford Co., (505) 265-5671

NY **E. Syracuse**
Cramer Syracuse, (315) 437-6671

Endwell
Cramer Binghamton, (607) 754-6661, Ext. 389

Farmingdale
Arrow Electronics, (516) 694-6800

Freeport
Milgray Electronics, (516) 546-6000; (N.J.) (201) 432-4300

NY **Hauppauge**
Cramer Electronics, (516) 231-5600

Huntington Station
TI Supply Company, (516) 293-2660

Rochester
Cramer Rochester, (716) 275-0300
Rochester Radio Supply Co., (716) 454-7800

NC **Raleigh**
Hall-Mark Electronics, (919) 832-4465

Winston/Salem
Cramer Winston/Salem, (919) 725-8711, Ext. 550

Ohio **Cincinnati**
Cramer Tri-States, (513) 771-6441, Ext. 574

Cleveland
Arrow Electronics, (216) 464-2000
Cramer Cleveland, (216) 248-8400, Ext. 565

Dayton
Esco Electronics, (513) 226-1133

Kettering
Arrow Electronics, (513) 253-9176

Okla **Tulsa**
TI Supply Company, (918) 437-4555

Ore **Portland**
Almac/Stroum Electronics, (503) 292-3534

Tex **Austin**
TI Supply Company, (512) 258-1636

Dallas
TI Supply Company, (214) 238-6823

Houston
Harrison Equipment Co., (713) 224-9131
TI Supply Company, (713) 785-4800

Utah **Salt Lake City**
Cramer Utah, (801) 487-4131
Standard Supply Company, (801) 355-2971

Va **Arlington**
TI Supply Company (Wash.)(703) 524-5885

Wash **Seattle**
ALMAC/Stroum Electronics, (206) 763-2300
Kierulff Electronics, (206) 763-1550

Wis **Milwaukee**
Hall-Mark Electronics, (414) 476-1270

Oak Creek
Cramer Wisconsin, (414) 764-1700

Wauwatosa
Semiconductor Specialists, (414) 778-0606

Can **Downsview, Ont.**
Cesco Electronics, Ltd., (416) 661-0220

Ottawa
Cesco Electronics, Ltd., (613) 729-5118
Future Electronics, (613) 232-7757

Rexdale (Toronto)
Future Electronics, (416) 677-7820

Montreal, P.Q.
Cesco Electronics, Ltd., (514) 735-5511
Future Electronics, (514) 735-5775

Quebec City
Cesco Electronics, Ltd., (418) 524-4641

Calgary, Alberta
Canadian Electronics, Ltd., (403) 287-1800

Edmonton
Canadian Electronics, Ltd., (403) 452-9393

Vancouver, B.C.
Canadian Electronics, Ltd., (604) 685-9311

Winnipeg, Man.
Canadian Electronics, Ltd., (204) 943-0763

TMX, Inc.

TMX Incorporated
250 Park Avenue
New York, New York 10017
(212) 661-9400

Sales Offices and Representatives

Cal **Woodland Hills**
Interstate Marketing Assoc., (213) 883-7670

Mass **Burlington**
Tritek, (617) 272-4550

Ohio **Centerville**
Micro Sales Corporation, (513) 433-8171

Toshiba

Toshiba America
Chicago Office
5235 N. Elston Ave.
Chicago, Illinois 60630
(312) 545-5123

New York Office
280 Park Avenue
New York, New York 10017
(212) 557-0407

Main Office
Toshiba Semiconductor Division
1 Komukai-Toshiba-cho, Saiwai-ku'
Kawasaki City, Kanagawa 210, Japan

Transitron Electronic

Transitron Electronics Corp.
168 Albion Street
Wakefield, Mass. 01880
(617) 245-4500
TWX: (710) 643-6708

TRW

trw Semiconductors
14520 Aviation Blvd.
Lawndale, California 90260
(213) 679-4561
TWX: (910) 325-6206
Telex: 67-7148

Western Digital

Western Digital Corporation
3128 Red Hill Avenue
P. O. Box 2180
Newport Beach, California 92663
(714) 557-3550
TWX: (910) 595-1139

Specific product information:

- Product Marketing ext. 243, 250
- Application engineering: ext. 292
- Literature:
 - Marketing Services ext. 241
- Price and delivery:
 - MOS/LSI Circuits - Marketing Department ext. 250
 - Spartan Test Systems - SPARTAN Sales ext. 208
- Place an order:
 - MOS/LSI Circuits -Local Sales Rep., Marketing Department ext. 250
 - Customer Service ext. 243
- Follow-up an order:
 - Customer Service ext. 243
- All other information:
 - Public Relations ext. 262

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Murcota Corp., (205) 539-8476
- Ariz** Scottsdale
Winter & Associates, (602) 948-1499
- Cal** Burlingame
Wm J. Purdy Co., (415) 347-7701
Long Beach
Walst, Inc., (213) 429-0772
Newport Beach
Regional Sales Office, (714) 557-3550
- Colo** Denver
W.J. Purdy Co., (303) 777-1411
- Conn** Trumbull
Blake Assoc., (203) 268-2560
- Fla** Clearwater
G.F. Bohman Assoc., Inc., (813) 422-5606
Ft. Lauderdale
G.F. Bohman Assoc., Inc., (305) 564-3081
Orlando
G.F. Bohman Assoc., Inc., (305) 855-0274
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Dolin Sales Co., (312) 286-6200
- Iowa** Cedar Rapids
S & O Sales, (319) 393-1845
- Md** Rockville
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Timonium
Marktron, Inc., (301) 252-7111
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Blake Associates, (617) 391-7890
- Mich** Detroit
A. Blumberg Associates, (313) 557-1934
St. Joseph
A. Blumenberg Assoc. Inc., (616) 983-0481
- Minn** Edina
Wagner Consultants Corp., (612) 941-6310
- Mo** Crestwood
Nevco, Inc., (314) 843-7406
Kansas City
Nevco, Incorporated, (816) 421-1751

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Wm. J. Purdy Co., (505) 266-7959
- NC** Winston Salem
Murcota Corp. (919) 722-9445
- NY** Camilus
Ontec, (315) 487-0596
Grand Island
Ontec, (716) 733-9319
Fayetteville
Ontec, (315) 466-2580
Rochester
Ontec, (716) 464-8636
Valley Cottage
LRC Associates, Inc., (914) 634-7973
- Ohio** Aurora
Engineering Marketing Assoc. (216) 562-6104
Centerville
Engineering Marketing Assoc., (513) 433-2800
- Ore** Portland
SJI Corp, (503) 224-0344
- Penn** Havertown
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Knowles Associates, (215) 947-5641
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Bonser-Philhower Sales, (214) 234-8438
Houston
Bonser-Philhower Sales, (713) 467-4373
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SJI Corp., (206) 624-9020
- Wisc** Milwaukee
D. Dolin Sales Co., (414) 355-9100
- Can** Montreal, Quebec
ITT Cannon Electric/Canada, (514) 336-7660
Whitby, Ontario
ITT Cannon Electric/Canada, (416) 668-8881
- Intl** England, Hounslow
Sims-Worms International Ltd., 01-572-0393
- Intl** France
Neuilly-Sur-Seine
Technology Resources, 747-4717
- Intl** Hong Kong, Hong Kong
Power Corporation, 3-637656
- Intl** Japan, Yokohama
Pan Electron, Inc., 045-471-8811
- Intl** Latin America, Africa,
India
Los Altos Cal
Row International Inc., (415) 941-6730
- Intl** Sweden, Vallingby
Svensk Teleindustri VX08-89 04 35
- Intl** Taiwan, Taipei
Sinoca Enterprises Co., Tlx 22-112
- Intl** West Germany, Munich
Spezial-Electronic KG, 0811/7600031

- Tex** Houston
Component Specialties, Inc., (713) 771-7237
- Utah** Salt Lake City
Diplomat/Salt Lake City, (801) 486-7227
- Can** Whitby, Ontario
ITT Cannon Electric/Canada, (416) 668-8881

Distributors

- Cal** Chatsworth
Westates Electronics, (213) 341-4411
Costa Mesa
Westates Electronics Corp., (714) 549-8401
Sunnyvale
Bell Industries, (408) 734-8570
Diplomat/Westland, (408) 734-1900
- Fla** Clearwater
Diplomat Southland, (813) 443-4514
- Ill** Elk Grove Village
Diplomat/Lakeland, (312) 595-1000
- Mass** Woburn
Time Electronics/New England, (617) 935-8080
- Mich** Farmington
Diplomat/Northland, (313) 477-3200
- Minn** Minneapolis
Diplomat/Electro-Com Corp., (612) 788-8601
- NY** Woodbury
Diplomat/Long Island, (516) 921-9373
- Ohio** Dayton
Diplomat/Ohio, (513) 228-1080
- Okla** Tulsa
Component Specialties, Inc., (918) 664-2820
- Pa** Clifton Heights
Time Mid Atlantic, (215) 622-2500
- Tex** Dallas
Component Specialties, Inc., (214) 357-4576

PRODUCT INDEX

This index shows the page and the line on that page of every device in the Master Selection Guide and the Application Note Directory. It is organized alphabetically by manufacturer and for each manufacturer, alpha-numerically by device. Bold face listings lead to data on important products which has been supplied for you by the manufacturers. If you want to determine which products are in the book from a given manufacturer, simply check the Product Index.

how to use the product index

The Product Index contains the same references as the Part Number Index, but in this case the listings are sorted by manufacturer.

As in the Part Number Index, the model numbers are sorted alpha-numerically from **left to right**. Here the manufacturer's prefixes are included so that devices with alphabetic prefixes appear before those without them (i.e., LM101 would be before

1101). Application note pages are indicated by a ¶ sign and data by a ★ sign. The numbers preceding the dash are the page numbers, while those following the dash indicate the location on the device on the page.

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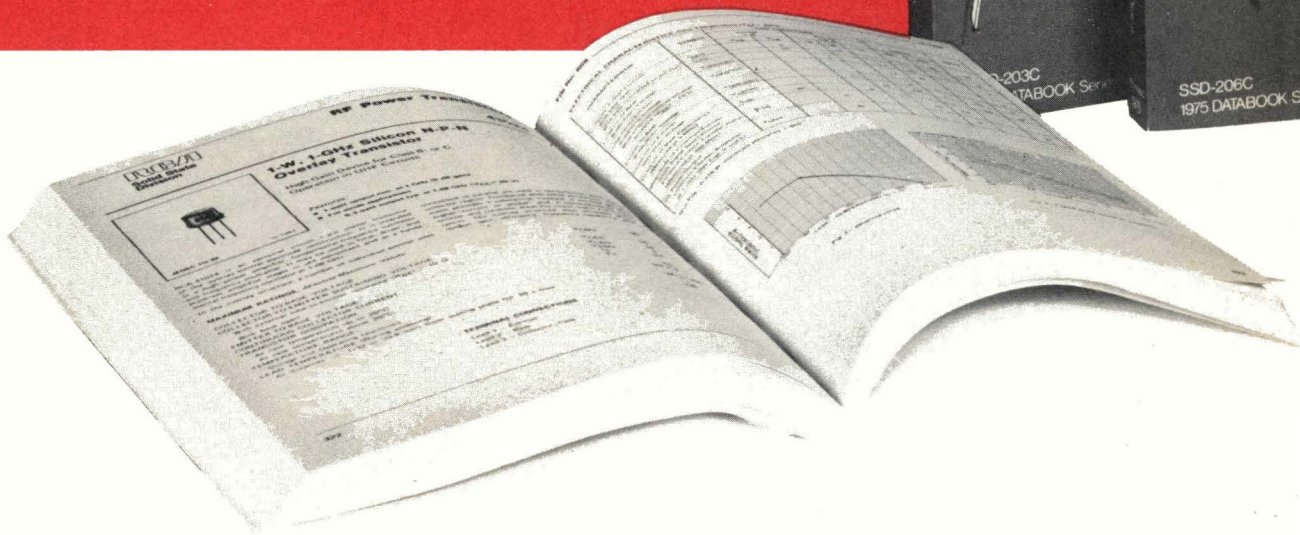
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