PRELIMINARY

MOSTEK®

MD SERIES MICROCOMPUTER MODULE

Operations Manual

MDX-CPU2 Z80-BASED CENTRAL PROCESSOR MODULE

MOSTEK MDX-CPU2 OPERATIONS MANUAL

MK77853

MK77853-4

Publication No. MK79711

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SECTION 1.0

GENERAL INFORMATION

1.1 INTRODUCTION

The Mostek MDX-CPU2 is a Z80 based microcomputer board. It features six 24-pin memory sockets capable of accepting any combination of pin compatible RAM, ROM or EPROM. Additionally, it provides a 4-channel counter/timer which is accessable both internally through software and externally for zero-count output and trigger control.

1.2 MD SERIES GENERAL DESCRIPTION

The MD Series and the STD-Z80 BUS were designed to satisfy the need for low cost OEM microcomputer modules. The STD-Z80 BUS uses a motherboard interconnect system concept and is designed to handle any MD Series card type in any slot. The modules for the STD-Z80 BUS are a compact 4.5 x 6.5 inches which provides for system partitioning by function, e.g. CPU, Memory, I/O, etc. This smaller module size makes system packaging easier while increasing MOS-LSI densities provide high functionally per module.

1.3 MDX-CPU2 FEATURES

.Utilizes the powerful Z80 microprocessor.

.Provides six 24-pin sockets which may be strapped to accept any combination of the following 24-pin industry-standard memory devices:

EPROM	STATIC RAM	ROM
2758(1kx8) 2716(2kx8) 2732(4kx8)	MK4118(1kx8) MK4801(1kx8) MK4802(2kx8)	MK34000(2kx8)

.Flexible memory decoding on any 1k boundary.

.Bidirectional address, data and control busses to permit external DMA.

.Four cascadable counter/timer channels, both hardware and software accessable.

.Fully buffered signals for system expandability.

.Selectable reset address to either 0000H or E000H.

.Selectable wait state generator, decoded on a per socket basis for slow memory devices.

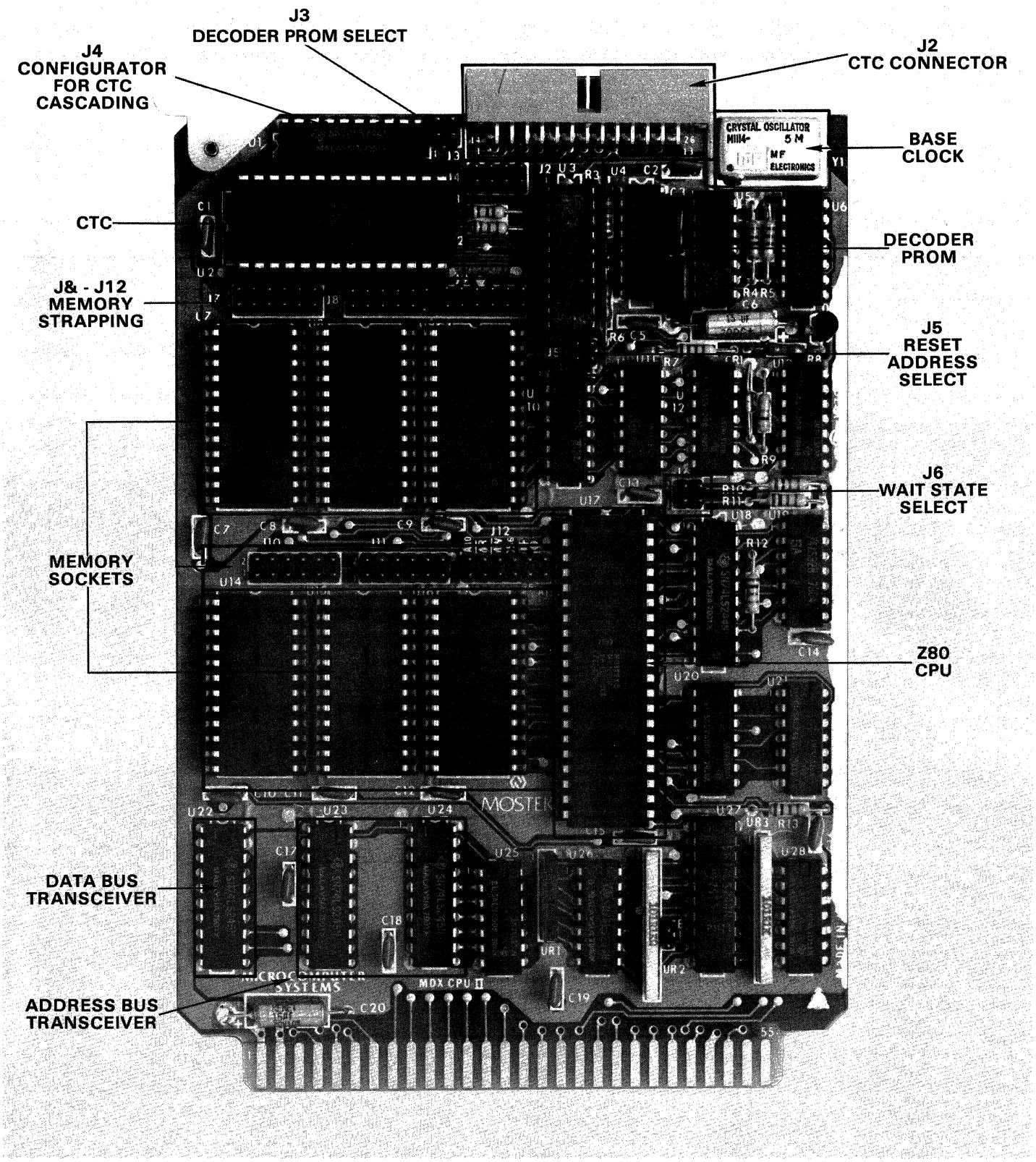
.Compatible with MDX-SST for single step operation during debugging.

.4 MHZ version available.

.Single +5 volt supply.

.STD-Z80 BUS compatible.

FIGURE 1-1 MDX-CPU2 BOARD PHOTO



SECTION 2.0

FUNCTIONAL HARDWARE DESCRIPTION

2.1 INTRODUCTION

The MDX-CPU2 utilizes the MK3880 (Z80) microprocessor as the system controller. It features six 24-pin memory sockets which enable the user to populate the module with any combination of designated ROM, RAM and EPROM. Flexible address decoding allows the user to configure each memory device within any 1k boundary of the 64k memory map. A PROM decoder is supplied which will allow the user to choose one of four popular memory configurations, or, if desired, the user may implement any possible mixture of memory devices simply by programming a decoder PROM accordingly. A programming example is shown in Appendix E.

Address, data and control busses have been made bidirectional to allow external DMA Controllers to directly access on-board memory.

A 4-channel counter/timer circuit (MK 3882) is included on-board for software controlled counting and timing functions. The CTC Trigger inputs and Zero Count outputs are buffered and brought out to a connector for external access. In addition, an on-board strapping option makes it possible to cascade the four CTC channels for long count sequences.

Another strapping option allows the user to select a reset address of either 0000H or E000H. The E000 option is required for use of standard MOSTEK software and hardware products including DDT-80, ASMB-80, FLP-80DOS/MDX, MDX-SST, and MDX-DEBUG. These products also require strapping on-board RAM to reside at Location FC00 through FFFF so that it will act as the operating system RAM for DDT-80.

A 4 MHZ version of MDX-CPU2 is also available (MDX-CPU2-4). In this version a jumper option enables automatic insertion of one WAIT state during on-board memory cycles for those memory devices having access times greater than 250 ns.

The decoder PROM supplied is programmed to identify MK2716 EPROMs as "slow" and MK4118 STATIC RAMs as "fast"; i.e., wait states will not be generated for MK4118 devices.

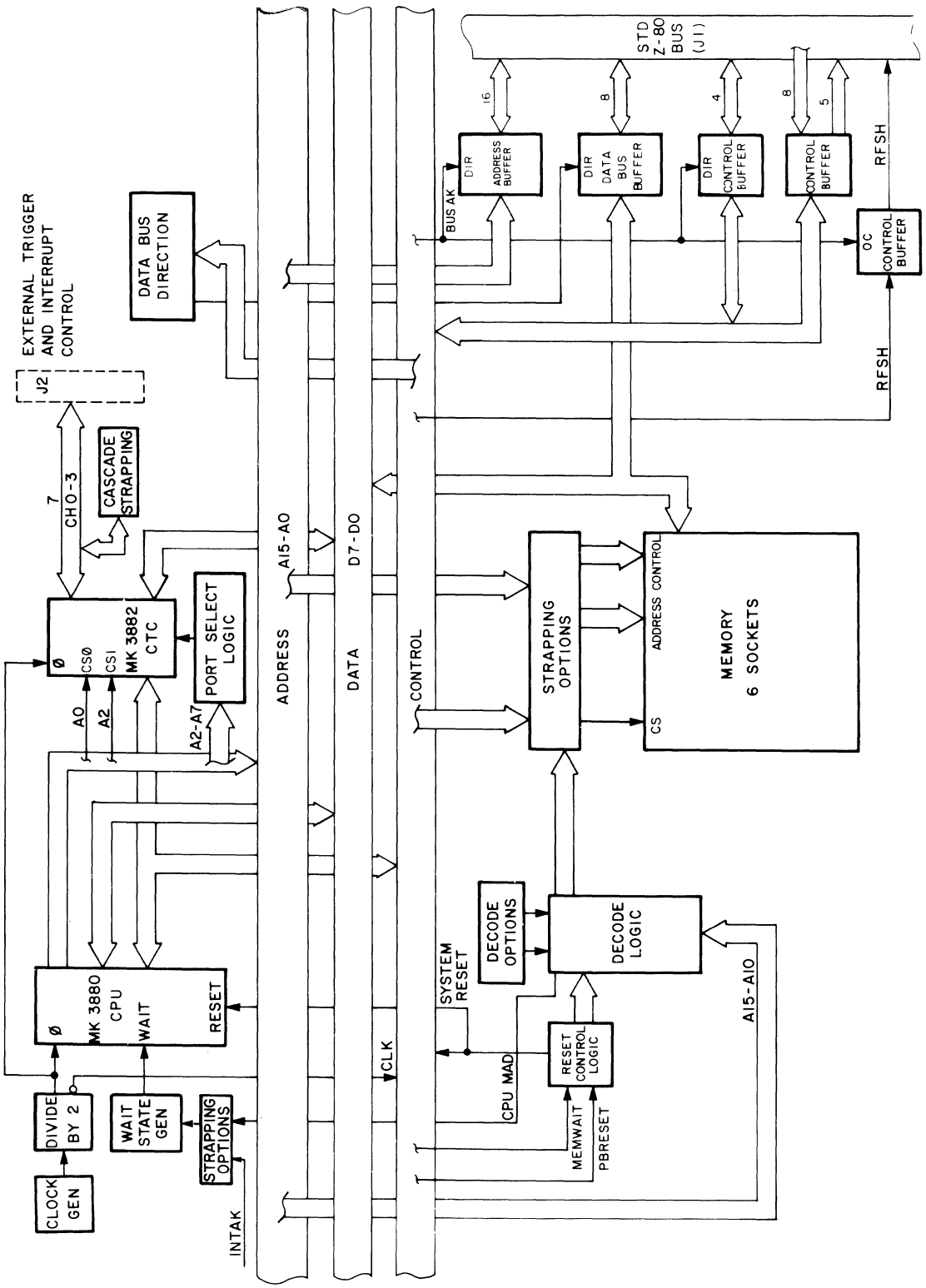
2.2 BLOCK DIAGRAM DESCRIPTION

Fiqure 2-1 is a block diagram illustrating the flow of system address, data and control signals on MDX-CPU2. The following paragraphs describe the function of each of the major blocks.

2.2.1 CPU.

The MK3880 (Z80) CPU is the system controller. It fetches, decodes and executes instructions from memory and generates the necessary address and control signals to coordinate data flow between the CPU and memory, or between the CPU and system I/O devices. Refer to the MK3880 Technical Manual for a complete description of the MK3880 CPU.

FIGURE 2-1 MDX-CPU2 BLOCK DIAGRAM



2.2.2 CLOCK GENERATOR

A hybrid, crystal-controlled oscillator generates the basic clock signals necessary for sequencing and synchronizing all CPU operations. The divide-by-2 block ensures a 50% duty cycle. The system clock frequency is 2.5 MHZ for MDX-CPU2 and 4.0 MHZ for MDX-CPU2-4. An inverted clock is applied to the system bus for use by other modules.

2.2.3 CTC (COUNTER/TIMER CIRCUIT)

The MK3882 Counter/Timer Circuit provides four independent, programmable channels for either software or hardware controlled counting and timing functions. Each channel can be configured by the CPU for various modes of operation and the built-in daisy chain priority interrupt logic provides for automatic, independent interrupt vectoring. The I/O port addresses for the CTC are hard-wired as follows:

I/O PORT ADDRESS	CTC CHANNEL
7C	0
7D	1
7E	2
7F	3

The Trigger inputs and Zero Count outputs are buffered and brought out to a connector for external hadware control. A strapping option has also been included to permit any or all of the four CTC channels to be cascaded for long count sequences.

Section 3 provides the necessary information for utilizing this option. For a complete description of CTC operation, refer to the MK3882 Technical Manual.

2.2.4 MEMORY

The MDX-CPU2 has been designed to accommodate any combination of the above

mentioned RAM, ROM and EPROM devices. Six 24-pin sockets have been provided, each of which may be strapped for any of the allowable memory types and for any 1k address boundary within the 64K Z80 memory map. These user-selectable options are fully described in Section 3.

2.2.5 DECODE LOGIC

This section primarily consists of a 256x8 PROM which decodes the high order six bits of memory address and generates the applicable chip select if on-board memory is to be selected. The 256 byte PROM provides for four separate memory configurations and is supplied programmed as defined in Section 3 and Appendix E. A strapping option must be hard-wired to the desired configuration as explained in Section 3.

2.2.6 RESET CONTROL LOGIC

This is a strapping option that causes a hardware-forced memory starting address upon system reset. A reset address of either 0000H or E000H may be selected.

This logic is required for use of standard MOSTEK hardware and software products including DDT-80, FLP-80DOS/MDX, MDX-SST, and MDX-DEBUG.

2.2.7 WAIT STATE GENERATOR

This function, if selected, causes on-board memory read and write cycles to be lengthened by one clock period in order to allow sufficient access time when slower memory devices are used. Each socket is selected independently for wait state generation as determined by the decoder PROM firmware. The decoder PROM supplied is programmed to cause a wait state to be inserted whenever on-board 2716 EPROMs are addressed. No wait states are generated during 4118 RAM access. This option should only be necessary for 4 MHZ CPU operation. The wait state generator for on-board memory may be disabled by disconnecting J6 pins 1 and 2.

The wait state generator may also be strapped to insert an additional wait cycle during interrupt acknowledge. The use of this option is dependent on the CPU clock frequency and the number of interrupting devices in the daisy chain. It is enabled by connecting J6 pins 3 and 4.

SECTION 3.0

USER SELECTABLE OPTIONS

3.1 INTRODUCTION

The MDX-CPU2 incorporates many strapping options to provide the user with a high degree of flexibility in system configuration. This section describes the use of the available jumper options.

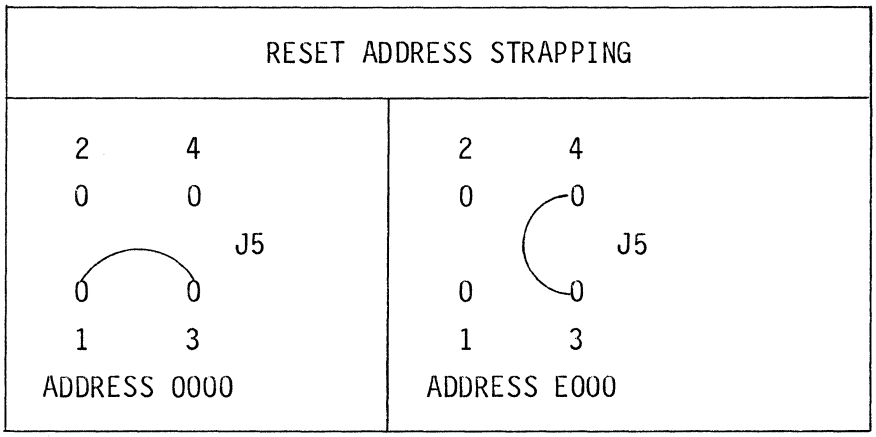
3.2 EXPLANATION OF STRAPPING OPTIONS

3.2.1 RESET ADDRESS STRAPPING

The MDX-CPU2 is capable of starting execution at either 0000H or E000H after reset.

Figure 3-1 illustrates the required jumper connections for selecting the desired reset address.

FIGURE 3-1



Reset address E000 is implemented in hardware. Since the program counter (internal to the Z80 microprocessor) always resets to 0000H, it must be updated to the correct address (E000) immediately following the reset. The hardware latch forcing the address must then be cleared. This is accomplished automatically during an I/O port read or write instruction. If no port access is normally made

then a "dummy" I/O read or write to an unused port address must be inserted. Otherwise, memory access will be constrained to address E000 through FFFF. To ensure proper operation after reset, the following code sequence should be placed in memory at the appropiate reset address:

ADDRESS	INSTRUCTION	
E000	C3 03 E0	("jump" instruction to update program counter)
E003	DB nn	(read unused I/O port nn to clear reset address latch)
E005		(first instruction of user program)

If any standard Mostek software (including DDT-80, FLP-80 DOS/MDX, or MDX-DEBUG) is used, address E000H must be strapped as the reset address to be compatible with the DDT-80 firmware package. The program counter and address latch modification instructions previously described are already contained within the DDT-80 ROM.

Pins 1 and 2 of header EI must be connected when the MDX-SST module is used.

3.2.2 MEMORY CONFIGURATION

The MDX-CPU2 incorporates six 24-pin sockets which can be independently configured to accept a variety of pin-compatible memory devices. Table 3-1 lists each socket and its corresponding jumper, and Table 3-2 illustrates the necessary jumper connections for configuring a socket to accept a particular memory device. Figure 3-2 shows the pin numbering for each jumper.

TABLE 3-1

MEMORY SOCKETS AND THEIR ASSOCIATED JUMPERS

SOCKET	JUMPER BLOCK
U7 (CS1)	J7
U8 (CS2)	J8
U9 (CS3)	J9
U14 (CS4)	J10
U15 (CS5)	J11
U16 (CS6)	J12

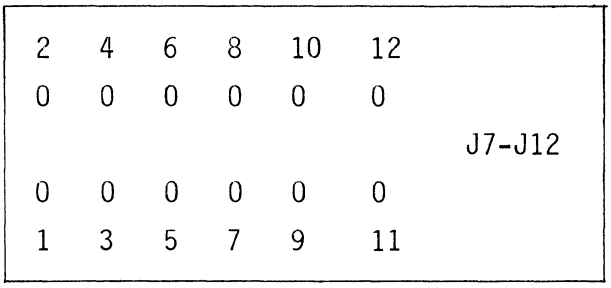
TABLE 3-2

JUMPER CONNECTIONS FOR VARIOUS MEMORY TYPES

FOR MEMORY TYPE:	CONNECT JUMPER PINS:
2758 EPROM	1 to 8 3 to 10 5 to 4 7 to 9
2716 EPROM	1 to 8 3 to 2 5 to 4 7 to 9
2732 EPROM	1 to 8 3 to 2 5 to 4 7 to 11
MK4801 SRAM	1 to 8 3 to 9 5 to 4 7 to 6
MK4118 SRAM	1 to 8 3 to 9 5 to 4 7 to 6
MK4802 SRAM	1 to 8 3 to 2 5 to 4 7 to 6
MK34000 ROM	1 to 8 3 to 2 5 to 4 7 to 9

FIGURE 3-2

JUMPER PIN NUMBERING FOR MEMORY STRAPPING



3.2.3 MEMORY ADDRESS DECODING

Each on-board memory device is enabled via a PROM decoder. This decoder provides for four separate memory configurations which are user selectable with a simple strapping option. The PROM is supplied preprogrammed for four options listed in Table 3-3. Figure 3-3 shows the J3 connections for selecting the desired option.

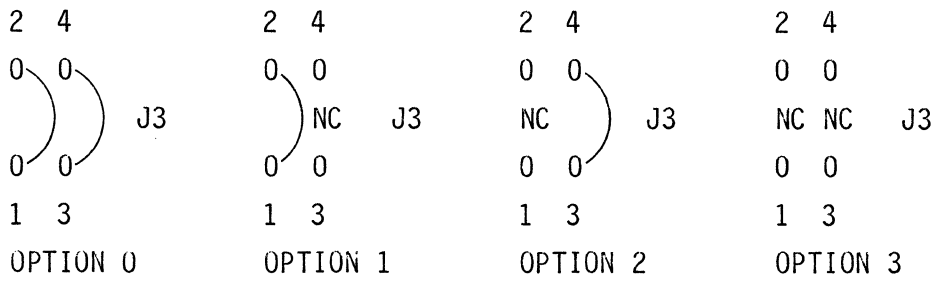
TABLE 3-3

MDX-CPU2 ON-BOARD MEMORY OPTIONS

OPTION	MEMORY TYPE	BOARD LOCATION	MEMORY ADDRESS	MEMORY TYPE	BOARD LOCATION	MEMORY ADDRESS
0	MK2716	U7,8	0000-0FFF	MK4118	U9,14,15,16	F000-FFFF
1	MK2716	U7,8,9,14	0000-1FFF	MK4118	U15,16	F800-FFFF
2	MK2716	U7,8	E000-EFFF	MK4118	U9,14,15,16	F000-FFFF
3	MK2716	U7,8,9,14,15	0000-27FF	MK4118	U16	FC00-FFFF

FIGURE 3-3

JUMPER CONNECTIONS FOR SELECTING THE DESIRED MEMORY OPTION



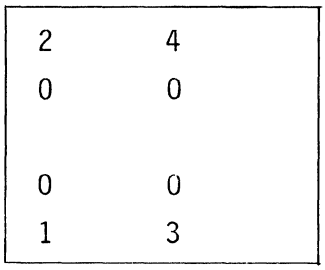
3.2.4 WAIT STATE GENERATOR

MDX-CPU2 provides an option to insert a wait state during on-board memory cycles to allow sufficient access time for EPROM memories and

during interrupt acknowledge cycles to allow sufficient response time for I/O devices. One wait cycle will be automatically inserted at the correct times when the J6 jumper connections are made as illustrated in Figure 3-4.

FIGURE 3-4

JUMPER CONNECTIONS FOR WAIT STATE GENERATOR



J6

Pins 1 and 2 of J6 must be connected to generate a wait state during on-board memory access.
Pins 3 and 4 of J6 must be connected to generate a wait state during interrupt acknowledge.

3.2.5 CTC CASCADING

The four Counter/Timer channels may be cascaded for extended counting and timing functions. Table 3-4 is a jumper pin reference list for cascading the CTC channels. Figure 3-5 is an example showing the necessary connections for cascading channels 0 and 1. Several combinations are possible.

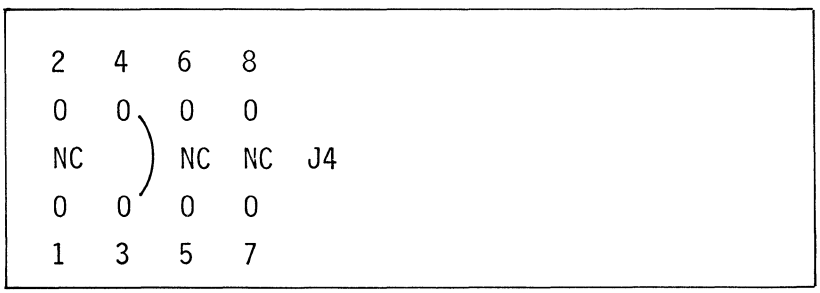
TABLE 3-4

JUMPER PIN REFERENCE LIST FOR CTC CASCADING

CTC CH	CNT ZERO OUT	CLK/TRIG IN
0	J4 PIN 3	J4 PIN 2
1	J4 PIN 5	J4 PIN 4
2	J4 PIN 7	J4 PIN 6
3	N/A	J4 PIN 8

FIGURE 3-5

EXAMPLE FOR CASCADING CTC CHANNELS 0 AND 1



Refer to the MK3882 Technical Manual for a complete description of CTC operation.

The CTC Clock/Trigger inputs and Zero Count outputs are brought out to a connector for external access. Table 3-5 lists the pin correspondence for the connector.

TABLE 3-5

CTC CONNECTOR PIN LIST (J2)

J2 PIN NO.	FUNCTION
1	C/T 0
2	ZC 0
3	C/T 1
4	ZC 1
5	C/T 2
6	ZC 2
7	C/T 3
8	NC
9	NMI*
10-13	NC
14-26	GND

* The CPU will respond to an externally generated non-maskable interrupt. This signal is logically OR'ed with NMIRQ (pin 46) on the STD-BUS.

Note that if two or more CTC channels are cascaded via J4, the corresponding J2 pins must be left open to prevent contention at the driver outputs.

SECTION 4

SPECIFICATIONS

4.1 FUNCTIONAL SPECIFICATIONS

4.1.1 WORD SIZE

Instruction:	8, 16, 24, or 32 bits
Data:	8 bits

4.1.2 CYCLE TIME

Clock period (T state):	400 ns for MDX-CPU2 250 ns for MDX-CPU2-4
Instruction Cycle:	Min. 4 T states Max. 23 T states

4.1.3 MEMORY CAPACITY

Six 24-pin sockets are provided which may be populated with any mixture of the following devices:

2758 (1K x 8 EPROM)
2716 (2K x 8 EPROM)
2732 (4K x 8 EPROM)
MK 34000 (2K x 8 ROM)
MK 4118 (1K x 8 Static RAM)
MK 4801 (1K x 8 Static RAM)
MK 4802 (2K x 8 Static RAM)

4.1.4 MEMORY ACCESS TIME

The time required to access on-board CPU2 memory by external DMA controllers is 106 ns plus the access time of the memory device. This is defined as the time interval between the time that the memory address is valid on the

STD-BUS and the time that the output data is valid on the STD-BUS.

4.1.5 MEMORY ADDRESSING

On-board PROM decoding allows any on-board memory to be configured on any 1K boundary of the Z80 CPU memory map.

Off-board memory expansion to a total of 65,536 bytes is possible with the use of the MDX-DRAM and MDX-UMC modules.

4.1.6 I/O ADDRESSING

The on-board 4-channel programmable timer is hard-wired to the following port addresses:

MK 3882 Channel	Port Address
0	7C
1	7D
2	7E
3	7F

4.1.7 I/O CAPACITY

The Z80 CPU utilizes the lower 8 bits of its address bus for I/O addressing to yeild a total of 256 possible port addresses, including the four CTC channel addresses on the CPU2 module.

4.1.8 INTERRUPTS

The CPU may be programmed to process interrupts in any of three different modes (mode 0, 1 or 2 as described in the MK3880 Technical Manua). Mode 2 operation (vectored interrupts) is by far the most powerful and is compatible with MOSTEK MDX Series cards.

Multi-level interrupt processing is also possible with the Z80 CPU. The level of stacking is limited only by available memory space.

The MDX-CPU2 will also accept non-maskable interrupts which force a restart at location 0066H.

4.1.9 SYSTEM CLOCK

MDX-CPU2	2.5 MHz ± 0.05%
MDX-CPU2-4	4.0 MHz ± 0.05%

4.2 ELECTRICAL SPECIFICATIONS

4.2.1 STD BUS INTERFACE

Bus Inputs:	One 74LS load max.
Bus outputs:	IOL = 24 mA min. @ VOL = 0.5 Volts
	IOL =-15 mA min. @ VOL = 2.4 Volts

4.2.2 OPERATING TEMPERATURE

0°C to 60°C

4.2.3 POWER SUPPLY REQUIREMENTS

5V ± 5% @ 1.2A (excluding memory power requirements)

4.3 MECHANICAL SPECIFICATIONS

4.3.1 CARD DIMENSIONS

4.50 in. (11.43 cm.) wide by 6.50 in. (16.51 cm.) long
0.48 in. (1.22 cm.) maximum height
0.062 in. (0.16 cm.) printed circuit board thickness

4.3.2 STD BUS EDGE CONNECTOR

56 Pin Dual Readout; 0.125 in. centers

4.3.3 MATING CONNECTOR

VIKING 3VH28/1CE5 (printed circuit)
VIKING 3VH28/1CND5 (wire wrap)
VIKING 3VH28/1CN5 (solder lug)

APPENDIX A

FACTORY NOTICES

FACTORY REPAIR SERVICE

In the event that difficulty is encountered with this unit, it may be returned directly to MOSTEK for repair. This service will be provided free of charge if the unit is returned within the warranty period. However, units which have been modified or abused in any way will not be accepted for service, or will be repaired at the owner's expense. When returning a circuit board, place it inside the conductive plastic bag in which it was delivered to protect the MOS devices from electrostatic discharge. THE CIRCUIT BOARD MUST NEVER BE PLACED IN CONTACT WITH SYTROFOAM MATERIAL. Enclose a letter containing the following information with the returned circuit board.

Name, address, and phone number of purchaser
Date and place of purchase
Brief description of the difficulty

Mail a copy of this letter SEPARATELY to:

In USA:

MOSTEK Corporation
Microcomputer Service Manager
1215 West Crosby Road
Carrollton TX, 75006

OUTSIDE USA:

Please address the letter and board to the Mostek office or representtive in your country.

Securely package and mail the circuit board, prepaid and insured, to the same address.

LIMITED WARRANTY

MOSTEK warrants this product against defective materials and workmanship for a period of 90 days. This warranty does not apply to any product that has been subjected to misuse, accident, improper installation, improper application, or improper operation, nor does it apply to any product that has been repaired or altered by other than an authorized factory representative.

There are no warranties which extend beyond those herein specifically given.

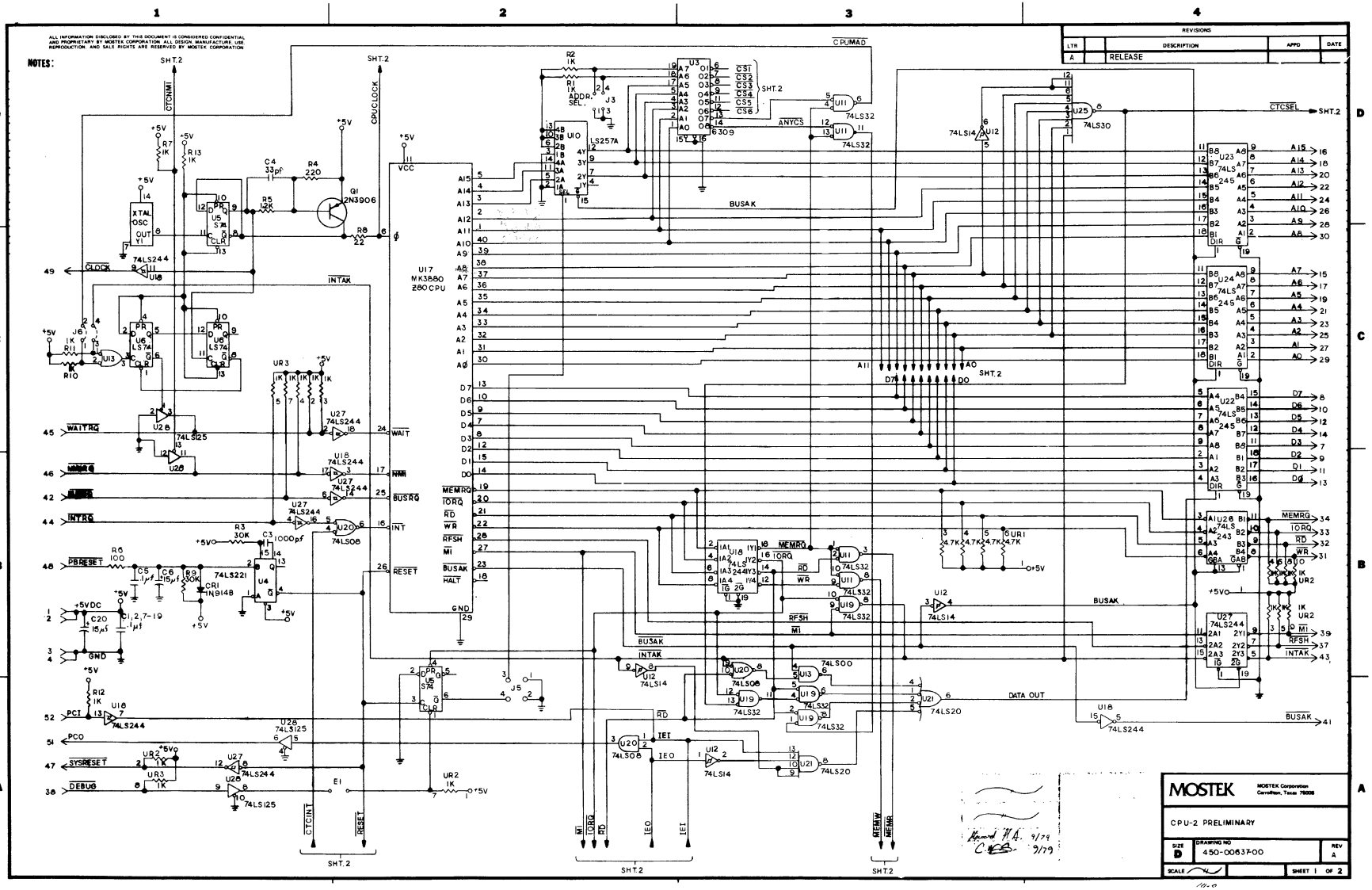
NOTICE

This antistatic bag is provided for shipment of the Mostek PC boards to prevent damage to the components due to electrostatic discharge.

Failure to use this bag in shipment will **VOID** the warranty.

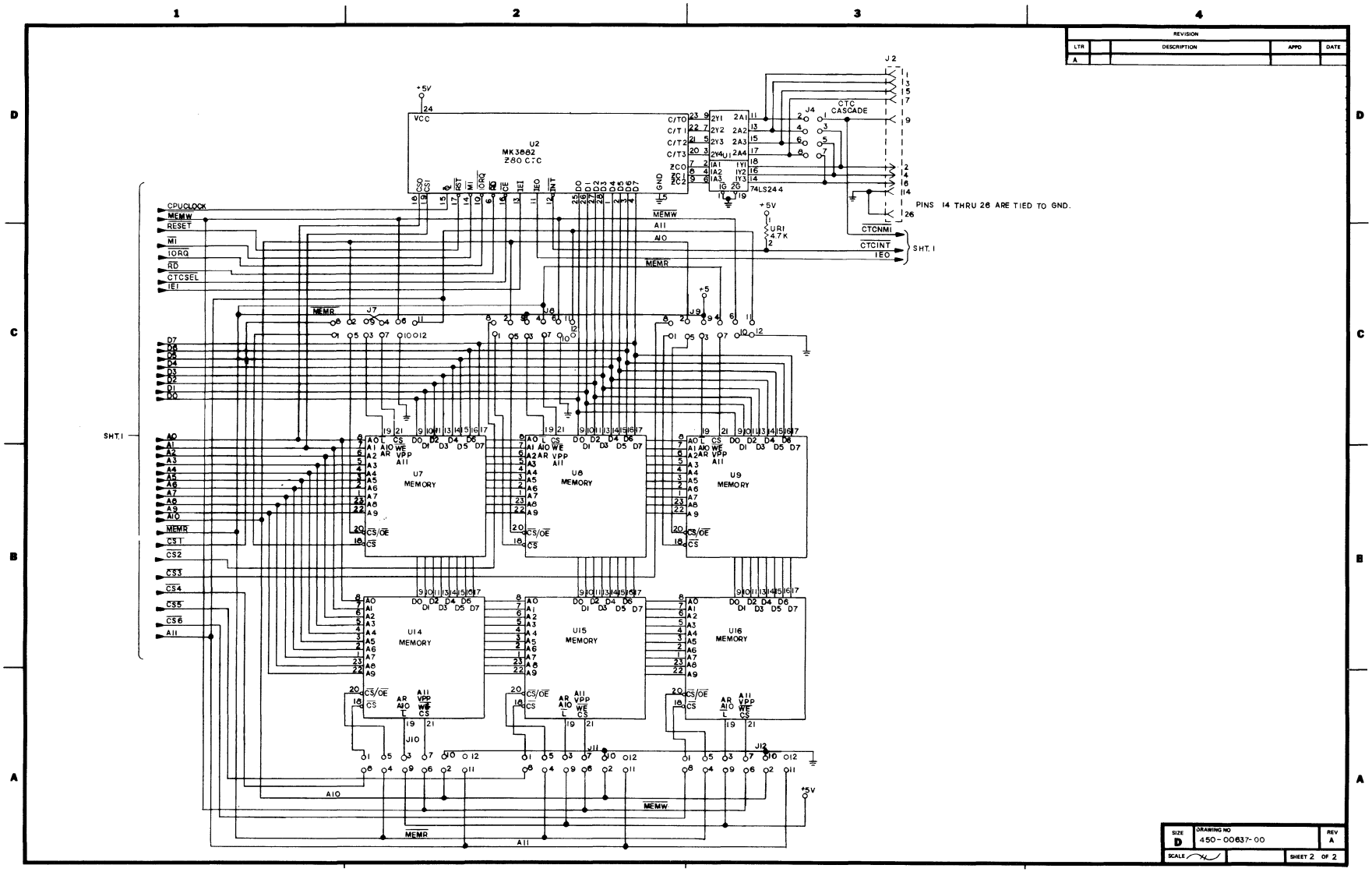
APPENDIX B

SCHEMATIC



B.1 SCHEMATIC

SCHEMATIC (CON'T)

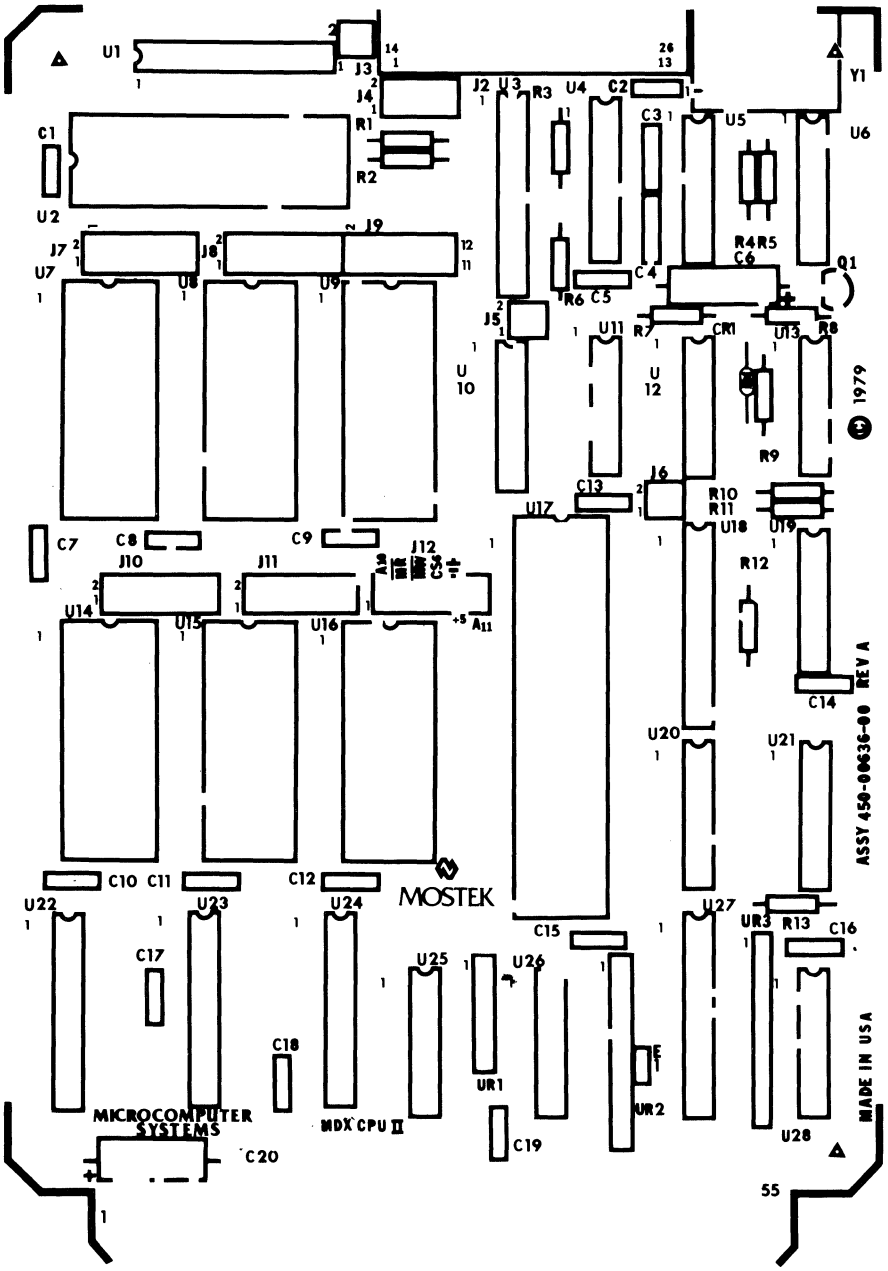


APPENDIX C

ASSEMBLY DRAWING

PARTS LIST

ASSEMBLY DRAWING



PARTS LIST OF MDX-CPU2

000000		AA:NOTE FOLLOWING PARTS USED
000000		AB:WITH 2.5 MHZ MDX-CPU2
4610214	FAB 450-00635-REV A	AC:
0000000	ASSY 450-00636-00 REV A	AD:
0000000	SCH 450-00637-00 REV A	AE:
4150111 16	CAPACITOR .1 UF	C1,2,5,7-19
4150101 1	CAPACITOR 1000 PF MICA	C3
4150086 1	CAPACITOR 33 PF MICA	C4
4150140 2	CAPACITOR 15 UF TANT.	C6,20
4480067 1	DIODE 1N914B	CR1
4210087 1	HEADER 2 PIN	E1
4210295 1	CONNECTOR 26 PIN	J2
4210238 3	HEADER 4 PIN	J3,5,6
4210239 1	HEADER 8 PIN	J4
4210285 6	HEADER 12 PIN	J7,8,9,10,11,12
4480011 1	TRANSISTOR 2N3906	Q1
4470073 7	RESISTOR 1K	R1,2,7,10-13
4470108 2	RESISTOR 30K	R3,9
4470057 1	RESISTOR 220 OHM	R4
4470075 1	RESISTOR 1.2 K	R5
4470049 1	RESISTOR 100 OHM	R6
4470033 1	RESISTOR 22 OHM	R8
4313507 3	IC 74LS244	U1,18,27
4313785 1	IC 74LS257A	U10
4313411 2	IC 74LS32	U11,19
4313291 1	IC 74LS14	U12
4313287 1	IC 74LS00	U13
4313271 1	IC MK3880 Z-80 CPU	U17
4313269 1	IC MK3882 CTC	U2
4313289 1	IC 74LS08	U20
4313292 1	IC 74LS20	U21
4313508 3	IC 74LS245	U22,23,24
4313410 1	IC 74LS30	U25

4313562	1	IC 74LS243	U26
4313641	1	IC 74LS125	U28
4314005	1	IC MK6289 (MMI 6309-1)	U3
4313638	1	IC 74LS221	U4
4313266	1	IC 74S74	U5
4313413	1	IC 74LS74	U6
4470202	1	RESISTOR SIP 4.7K 6 PIN	UR1
4470174	2	RESISTOR SIP 1K 10 PIN	UR2,3
4620019	1	SOCKET 40 PIN	X17
4620038	1	SOCKET 28 PIN	X2
4620070	1	SOCKET 20 PIN	X3
4620018	6	SOCKET 24 PIN	X7,8,9,14,15,16
4230019	1	OSCILLATOR MOD. 5 MHZ	Y1
4280155	1	EJECTOR	Z
MK79815	1	FACTORY NOTICES	Z:SHIPPED NOT ASSEMBLED
MK79728	1	WARRANTY REGISTRATION	Z:SHIPPED NOT ASSEMBLED
5013004	2	ANTI-STATIC BAG	Z:SHIPPED NOT ASSEMBLED
5013204	1	BOX	Z:SHIPPED NOT ASSEMBLED
MK79711	1	MDX-CPU2 OPS. MANUAL	Z:SHIPPED NOT ASSEMBLED

C.2 PARTS LIST FOR MDX-CPU2-4

000000		AA:NOTE FOLLOWING PARTS USED
000000		AB:WITH 4 MHZ MDX-CPU2
4610214	FAB 450-00635-00 REV A	AC:
0000000	ASSY 450-00636-00 REV A	AD:
0000000	SCH 450-00637-00 REV A	AE:
4150111 16	CAPACITOR .1 UF	C1,2,5,7-19
4150101 1	CAPACITOR 1000 PF MICA	C3
4150086 1	CAPACITOR 33 PF MICA	C4
4150140 2	CAPACITOR 15 UF TANT.	C6,20
4480067 1	DIODE 1N914B	CR1
4210087 1	HEADER 2 PIN	E1
4210295 1	CONNECTOR 26 PIN	J2
4210238 3	HEADER 4 PIN	J3,5,6
4210239 1	HEADER 8 PIN	J4
4210285 6	HEADER 12 PIN	J7,8,9,10,11,12
4480011 1	TRANSISTOR 2N3906	Q1
4470073 7	RESISTOR 1K	R1,2,7,10-13
4470108 2	RESISTOR 30K	R3,9
4470057 1	RESISTOR 220 OHM	R4
4470075 1	RESISTOR 1.2 K	R5
4470049 1	RESISTOR 100 OHM	R6
4470033 1	RESISTOR 22 OHM	R8
4313507 3	IC 74LS244	U1,18,27
4313785 1	IC 74LS257A	U10
4313411 2	IC 74LS32	U11,19
4313291 1	IC 74LS14	U12
4313287 1	IC 74LS00	U13
4313532 1	IC MK3880-4 CPU	U17
4313674 1	IC MK3882-4 CTC	U2
4313289 1	IC 74LS08	U20
4313292 1	IC 74LS20	U21
4313508 3	IC 74LS245	U22,23,24
4313410 1	IC 74LS30	U25
4313562 1	IC 74LS243	U26

4313641	1	IC 74LS125	U28
4314005	1	IC MK6289 (MMI 6309-1)	U3
4313638	1	IC 74LS221	U4
4313266	1	IC 74S74	U5
4313413	1	IC 74LS74	U6
4470202	1	RESISTOR SIP 4.7K 6 PIN	UR1
4470174	2	RESISTOR SIP 1K 10 PIN	UR2,3
4620019	1	SOCKET 40 PIN	X17
4620038	1	SOCKET 28 PIN	X2
4620070	1	SOCKET 20 PIN	X3
4620018	6	SOCKET 24 PIN	X7,8,9,14,15,16
4230020	1	OSCILLATOR MOD. 8 MHZ	Y1
4280155	1	EJECTOR	Z
MK79815	1	FACTORY NOTICES	Z:SHIPPED NOT ASSEMBLED
MK79728	1	WARRANTY REGISTRATION	Z:SHIPPED NOT ASSEMBLED
MK79711	1	MDX-CPU2 OPS. MANUAL	Z:SHIPPED NOT ASSEMBLED
5013004	2	ANTI-STATIC BAG	Z:SHIPPED NOT ASSEMBLED
5013204	1	BOX	Z:SHIPPED NOT ASSEMBLED

APPENDIX D

PROGRAMMING THE DECODER PROM

FOR CUSTOM APPLICATIONS

D.1 PROGRAMMING THE DECODER PROM FOR CUSTOM APPLICATIONS

The 256 x 8 decoder PROM (U3) supplied with MDX-CPU2 is preprogrammed as described in Appendix E. The primary function of the PROM is to decode the upper six bits of the memory address and select one of six on-board memory devices to be accessed. The PROM assigns the address boundaries to each memory device in increments of 1024 (1K) bytes. If address assignments other than those (4) provided are required, then a new decoder PROM must be programmed accordingly.

The function of the decoder may be visualized as illustrated in Figure D.1. The 256 x 8 PROM is divided into four 64-byte sections via strapping header J3 and address bits A7 and A6. The six remaining address bits, A5 through A0, are connected to A15-A10 of the address bus. These high-order six bits of the 16-bit address will partition the memory into blocks of 1K bytes. Figure D.2 illustrates address partitioning.

The PROM outputs O1 through O6 drive the low-active chip enables of the six on-board memory devices. Output O7 drives the wait state generator. Output O8 is defined to be a logical "OR" of outputs O1 through O6, which is necessary to control bus direction. Table D.1 summarizes the PROM output functions.

After determining the memory device type and associated address space for each socket location, simply program a logic "0" in the PROM data bit corresponding to the device (socket) to be enabled. The relationship between the PROM address and memory address space is shown in Figure D.3. Each 1024 increments of memory address cause the PROM address to increment by 1, thereby "decoding" the memory address on 1K boundaries.

Bit O7 must be programmed (low) simultaneously with the chip select function for those devices requiring a wait state during 4 MHz operation.

Bit O8 must be programmed to be active (low) whenever any chip select is active

for bus direction control.

Each socket is customized for a particular device type via hardware strapping options while the decoder PROM firmware determines the memory address space in which each device resides.

The information given in Section 3 and Appendix E concerning the memory configuration options supplied with MDX-CPU2 will serve as an example to aid the user in developing custom decoder firmware.

FIGURE D.1
PROM DECODER-FUNCTIONAL DIAGRAM

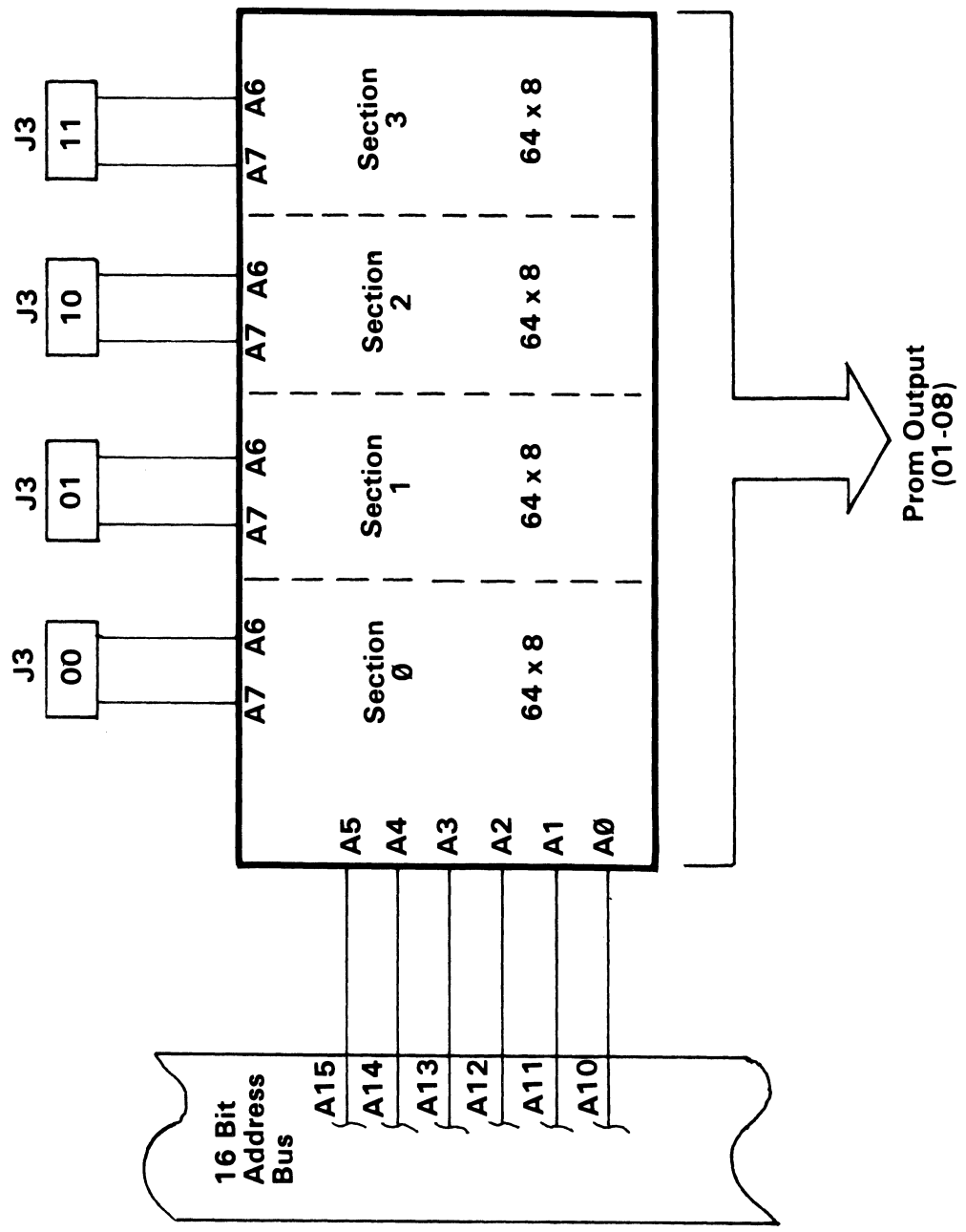


FIGURE D.2
MEMORY ADDRESS PARTITIONING

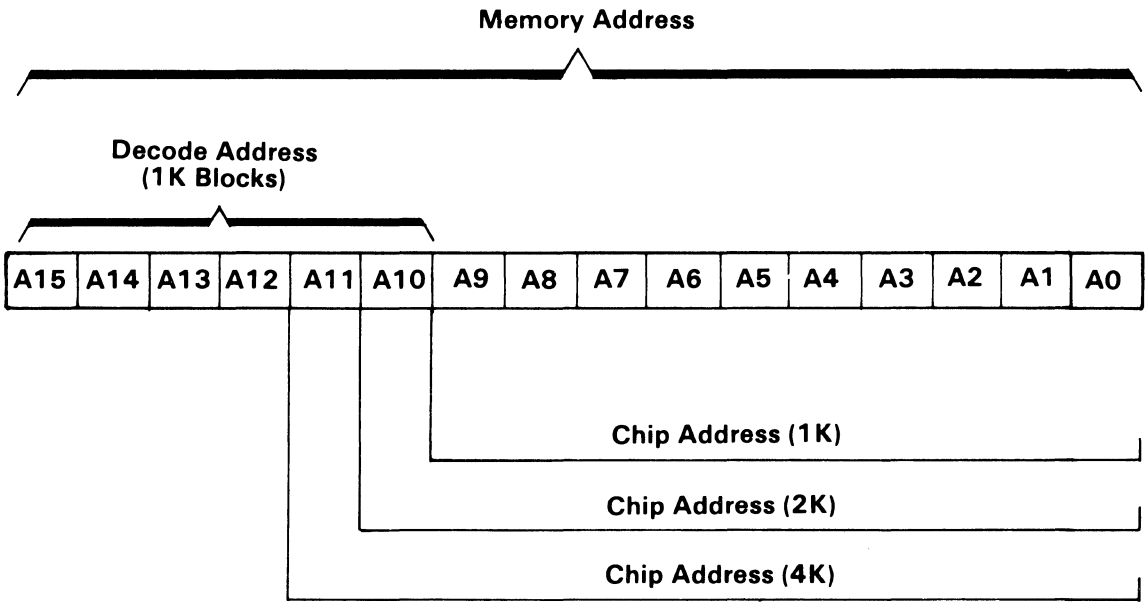


TABLE D.1

OUTPUT BIT	01	02	03	04	05	06	07	08
PIN NUMBER	6	7	8	9	11	12	13	14
FUNCTION	$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	$\overline{CS5}$	$\overline{CS6}$	$\overline{WAIT}$	$\overline{ANY\ CS}$
LOCATION	U7	U8	U9	U14	U15	U16	----	----

FIGURE D.3

MEMORY ADDRESS SPACE VS. DECODER PROM ADDRESS

MEMORY ADDRESS HEX	DECODER ADDRESS BINARY	OCTAL	ENABLES SECTION OF:
0000-03FF	XX000000	X00	1st 1K Block
0400-07FF	XX000001	X01	2nd 1K Block
0800-0BFF	XX000010	X02	3rd 1K Block
.	.		.
.	.		.
.	.		.
F800-FBFF	XX111110	X76	63rd 1K Block
FC00-FFFF	XX111111	X77	64th 1K Block

"XX" is determined by the optional wiring of J3.

APPENDIX E

PROM DECODER FIRMWARE

E.1 PROM DECODER FIRMWARE

The 256x8 PROM is divided into four 64-byte sections, one section for each memory option, as follows:

OPTION 0 (00-3F)		OPTION 2 (80-BF)	
ADDRESS	DATA	ADDRESS	DATA
00	3E	80-B7	FF
01	3E	B8	3E
02	3D	B9	3E
03	3D	BA	3D
04-3B	FF	BB	3D
3C	7B	BC	7B
3D	77	BD	77
3E	6F	BE	6F
3F	5F	BF	5F

OPTION 1 (40-7F)		OPTION 3 (C0-FF)	
ADDRESS	DATA	ADDRESS	DATA
40	3E	C0	3E
41	3E	C1	3E
42	3D	C2	3D
43	3D	C3	3D
44	3B	C4	3B
45	3B	C5	3B
46	37	C6	37
47	37	C7	37
48-7D	FF	C8	2F
7E	6F	C9	2F
7F	5F	CA-FE	FF

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