

MEX6816-1HR  
MEX6832-1HR  
MEX6848-1HR  
MEX6864-1HR

16K/64K HIDDEN REFRESH MEMORY MODULE

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## GENERAL INFORMATION .

## 1.1 INTRODUCTION

This manual provides general information, installation instructions, programming considerations, hardware preparation, and theory of operation for the MEX6816-1HR (16K), MEX6832-1HR (32K), MEX6848-1HR (48K), and MEX6864-1HR (64K) Hidden Refresh Memory Module. A typical module is shown in Figure 1-1. All address references within this manual are shown in hexadecimal unless otherwise indicated.

## 1.2 FEATURES

The features of the Hidden Refresh Memory Module include:

- . 16384 x 9 bits, 32768 x 9 bits, 49152 x 9 bits, or 65536 x 9 bits of RAM organized in four independently addressed rows of 16K bytes each.
- . Refresh during  $\phi 1$  of the MPU cycle, eliminating the need to stop MPU operation during refresh.
- . Jumper selectable memory address enable.
- . Series II DSB (Dynamic System Bus) provides Page Enable, Parity Error, and extended memory control.
- . Parity error circuitry with jumper selectable connector outputs.
- . TTL voltage compatible high impedance inputs.

## 1.3 SPECIFICATIONS

The Hidden Refresh Memory Module specifications are identified in Table 1-1.

## 1.4 GENERAL INFORMATION

The Hidden Refresh Memory Module is populated with 16K x 1 bit dynamic RAM devices. The devices are connected in rows of nine devices each. A 16K module has nine devices, a 32K module has 18 devices, a 48K module has 27 devices, and a 64K module has 36 devices. Each row is addressed and refreshed independently.

Memory refresh is accomplished during phase 1 of the MPU clock. The MC6800 MPU is designed to operate on a two-phase clock. Phase 1 is dedicated to internal MPU operations. Phase 2 is used to access external memory and I/O. This leaves all external RAM idle during phase 1 of the MPU cycle. The Hidden Refresh Memory Module takes advantage of the idle memory time to refresh the dynamic memory.

The module circuitry generates and detects even parity. The module outputs a PARITY ERROR signal to the system whenever a parity error is detected. The output is jumper selectable to the system bus as PARITY ERROR, NMI, or a custom interface through the Dynamic System Bus (P2).

In the upper left-hand portion of the module is a 20-pin wire-wrap header, P2 (Dynamic System Bus). Parity error, parity control, and page enable lines are connected to the DSB.

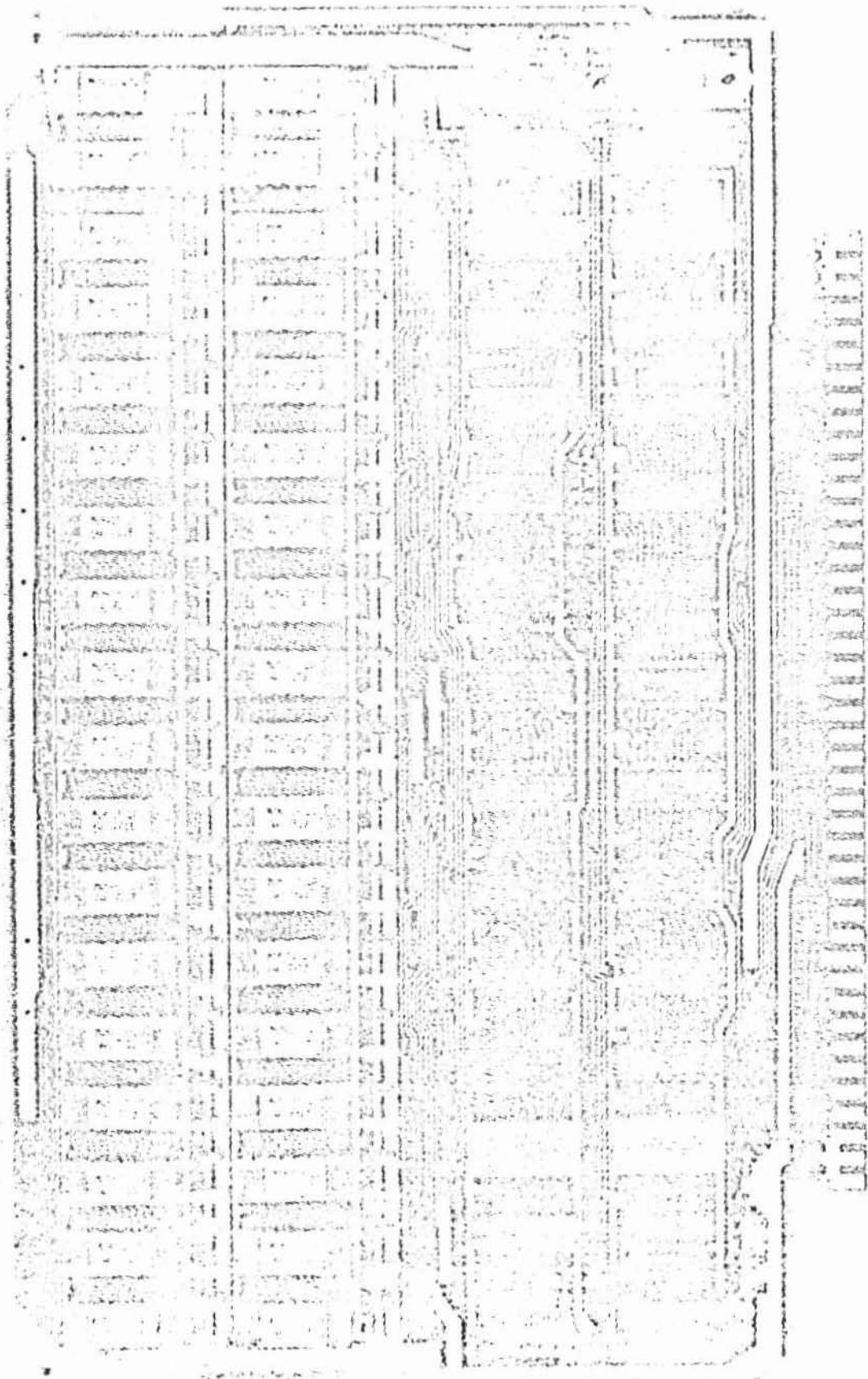


FIGURE 1-1. Typical Hidden Refresh Memory Module

TABLE 1-1. Hidden Refresh Memory Module Specifications

CHARACTERISTIC	SPECIFICATION
Memory Type	N-channel MOS Dynamic RAM
Memory Organization	64K x 9 bits organized in four 16K x 9 bit rows
Read Access Time	350 ns from memory clock
Parity	Even parity
Hidden Refresh	Row refresh during $\phi 1$ of each MPU cycle
Input Signals	
Commands	TTL voltage compatible
Address	TTL voltage compatible
Data Bus	Three-state TTL voltage compatible
Operating Temperature	0° to 70°C
Power Requirements	+5 Vdc - Peak = 1.00 Amp Typ. Average = 980 mA Typ.
	+12 Vdc - Peak = 160 mA Typ. Average = 130 mA Typ.
	-12 Vdc - Peak = 8 mA Typ. Average = 4 mA Typ.
Dimensions	
Width and Height	9.75 inches x 6.00 inches
Board Thickness	0.062 inches

## CHAPTER 2

### INSTALLATION INSTRUCTIONS, HARDWARE PREPARATION, AND INTERCONNECTION CONSIDERATIONS

#### 2.1 INTRODUCTION

This chapter provides the unpacking, inspection, installation, and preparation for use instructions for the Hidden Refresh Memory Module. Also included in this chapter are the module interconnection signals.

#### 2.2 UNPACKING INSTRUCTIONS

##### NOTE

IF THE SHIPPING CARTON IS DAMAGED UPON RECEIPT, REQUEST THAT THE CARRIER'S AGENT BE PRESENT DURING UNPACKING AND INSPECTION OF THE MODULE.

Unpack the Hidden Refresh memory module from the shipping carton. Refer to the packing list and verify that all of the items are present. Save the packing material for storing and reshipping the module.

#### 2.3 INSPECTION

The Hidden Refresh Memory Module should be inspected upon receipt for broken, damaged, or missing parts, and physical damage to the printed circuit board.

#### 2.4 HARDWARE PREPARATION

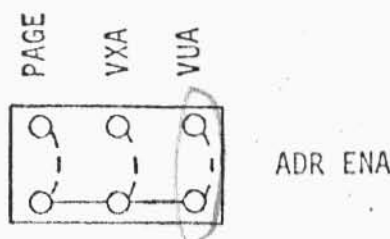
Prior to installing the module in the system, the user must ensure that the module is set up to perform the functions required. Various user options are provided on the module through the use of jumpers and wire-wrap headers. Figure 2-1 shows the locations of the headers which are referred to in the following paragraphs.

##### 2.4.1 Memory Map Assignment

The user has the option of three map modes to enable the address decoding.

VUA - Valid User Address  
VXA - Valid Executive Address  
PAGE ENABLE - For multiple "pages" of 64K bytes

A jumper at ADR ENA is provided for the purpose, as illustrated below:





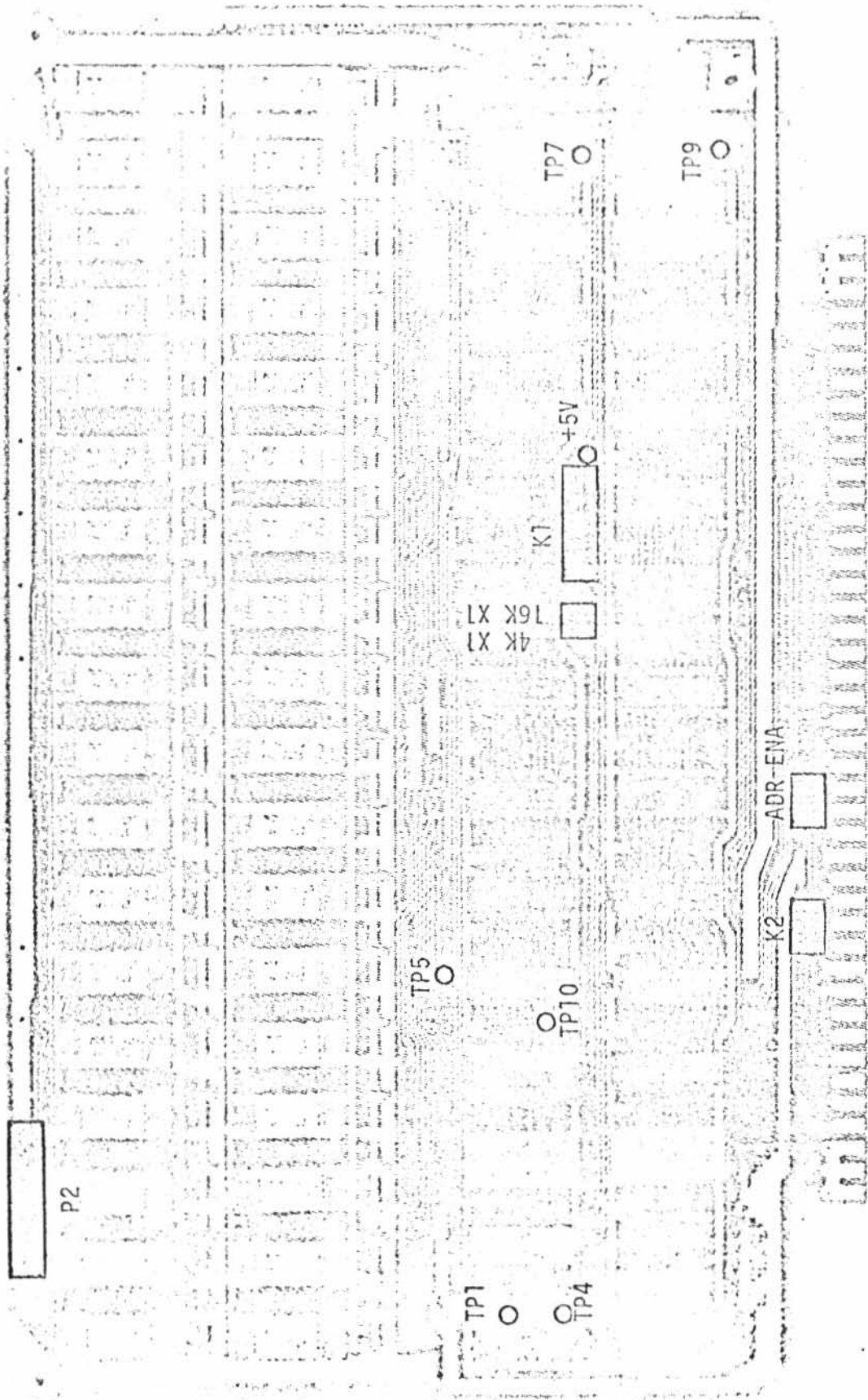


FIGURE 2-1. User Option and Test Point Locations

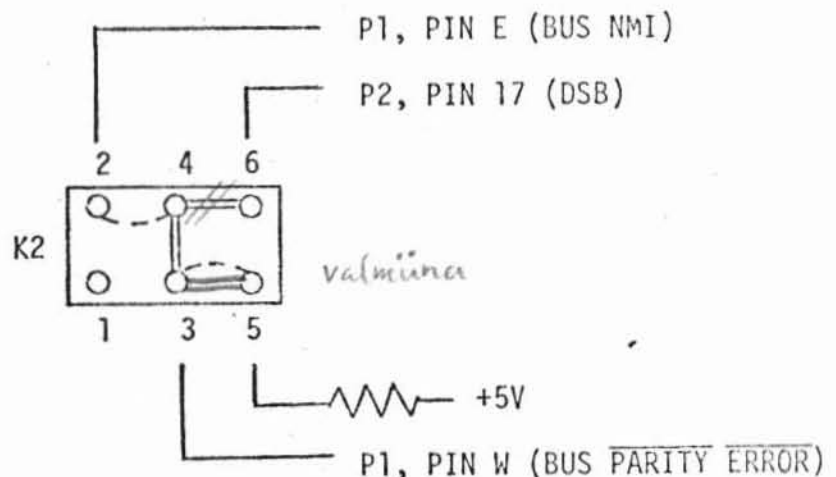
## 2.4.2 Parity Option

If the user is monitoring parity, he has the choice of three options for connecting the parity error detect signal to the system. Wire-wrap header K2 is provided for this purpose. The header is factory wired with  $\overline{\text{PARITY ERROR}}$  connected to P1, pin W and to P2, pin 17 (DSB).

- Option 1 - As factory wired,  $\overline{\text{PARITY ERROR}}$  output on P1, pin W.
- Option 2 - To output  $\overline{\text{PARITY ERROR}}$  on P1, pin E,  $\overline{\text{NMI}}$ . On back of module, cut track between header pins 3 and 4. On front of module, install jumper between header pins 2 and 4. In this configuration, the parity error will generate a non-maskable interrupt (NMI) for one clock cycle.
- Option 3 - As factory wired,  $\overline{\text{PARITY ERROR}}$  output on P2, pin 17 (DSB). The usefulness of this configuration depends upon the user's implementation of the Dynamic System Bus.

When the Hidden Refresh Module is used in a system without a DEbug II module, the  $\overline{\text{PARITY ERROR}}$  line must be held high by a user module or by a jumper between header K2, pin 3 and 5.

Header K2 is illustrated below:



## 2.4.3 Address Select Header

Header K1 is a 16 pin wire-wrap device providing the user with the capability of selecting the 16K block (row) addressing. The wire-wrap jumpers may be installed to enable from one to four of the 16K blocks. Each of the blocks may be independently located at any 16K boundary in the 64K memory map. The selection of blocks is limited by the number of memory devices on the module. The 16K module has one row of memory, the 32K module has two rows of memory, the 48K module has three rows of memory, and the 64K module has four rows of memory. Capability is also provided to allow "masking off" the upper or lower half of any 16K block.

Each 16K block is enabled by a row address select ( $\overline{\text{RAS}}$ ) signal driven from gate U45. Both inputs to the gate must be low to enable the block of memory. The two input signals are driven by the outputs of the address decoder U59 (See schematic, Figure 3-3).

Figure 2-2 shows the K1 header pin configuration, memory devices, and bit storage.



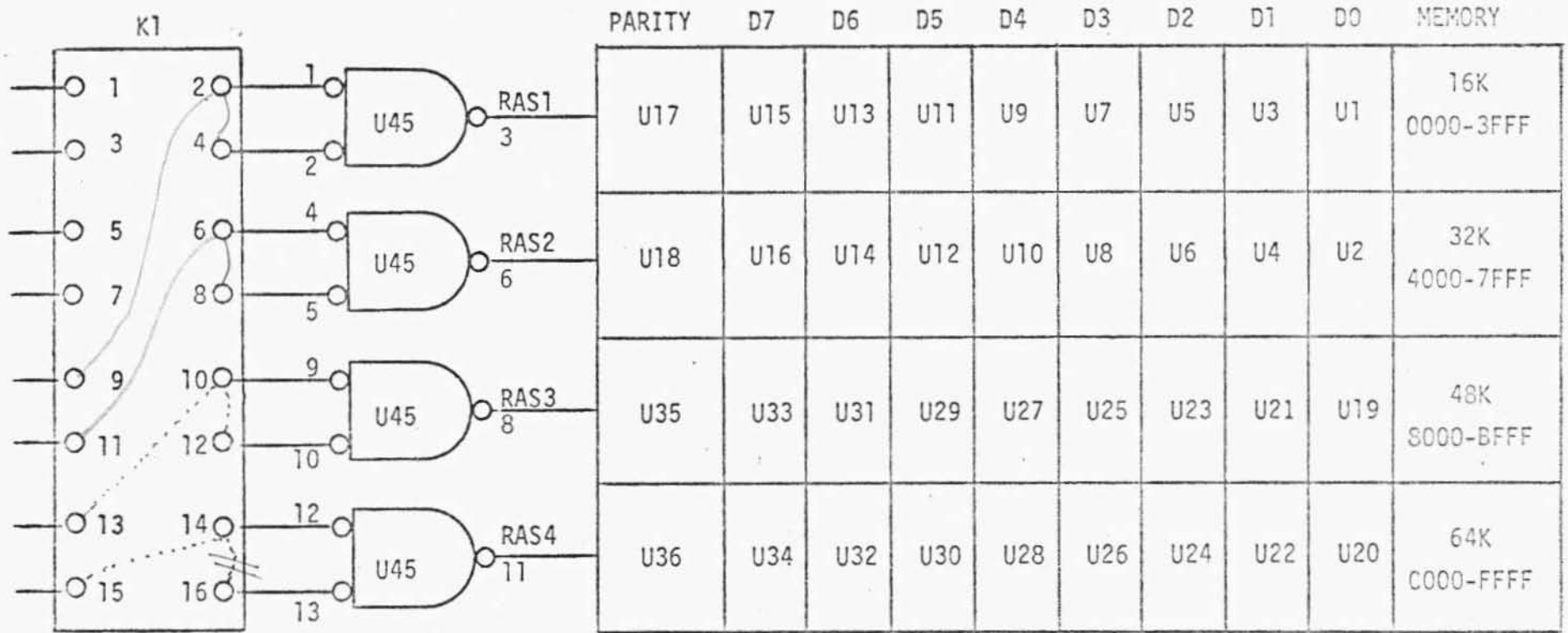


FIGURE 2-2. Header K1, Memory and Bit Storage.

### 2.4.3.1 Addressing Considerations

The user must install jumpers on K1 to address the memory blocks. Table 2-1 lists the jumper connections to enable memory. Refer to Figure 2-2 in conjunction with Table 2-1.

TABLE 2-1. Memory Enable Jumpers

MODULE MEMORY SIZE	JUMPERS			
	FROM	TO	FROM	TO
16K	K1-9	K1-2	K1-2	K1-4
32K	K1-9 K1-11	K1-2 K1-6	K1-2 K1-6	K1-4 K1-8
48K	K1-9 K1-11 K1-13	K1-2 K1-6 K1-10	K1-2 K1-6 K1-10	K1-4 K1-8 K1-12
64K	K1-9 K1-11 K1-13 K1-15	K1-2 K1-6 K1-10 K1-14	K1-2 K1-6 K1-10 K1-14	K1-4 K1-8 K1-12 K1-16

An entire 16K block (row) of memory may be disabled by tying the inputs of the desired block enable gate to +5Vdc. A wire-wrap pin, labeled +5V, is located to the right of K1 for this purpose. Table 2-2 lists the jumper arrangement to disable the upper two 16K blocks of memory.

TABLE 2-2. Memory Block Disable

JUMPERS			
FROM	TO	FROM	TO
K1-9	K1-2	K1-2	K1-4
K1-11	K1-6	K1-6	K1-8
+5V	K1-10	K1-10	K1-12
+5V	K1-14	K1-14	K1-16

The above tables listed jumper arrangements for typical user implementation. Other addressing configurations can be made by the user.

### 2.4.3.2 Configuration Requirements for 56K Memory

To prevent conflict with system firmware (EXbug) which uses memory locations F000-FFFF, the user may wish to disable the upper 8K (E000-FFFF) of the 64K block (64K module only). Table 2-3 lists the jumper arrangements for this purpose.

Cut circuit track on front of module at arrow located between U58 and U59. This is the circuit track for the A12 line to U59, pin 2.

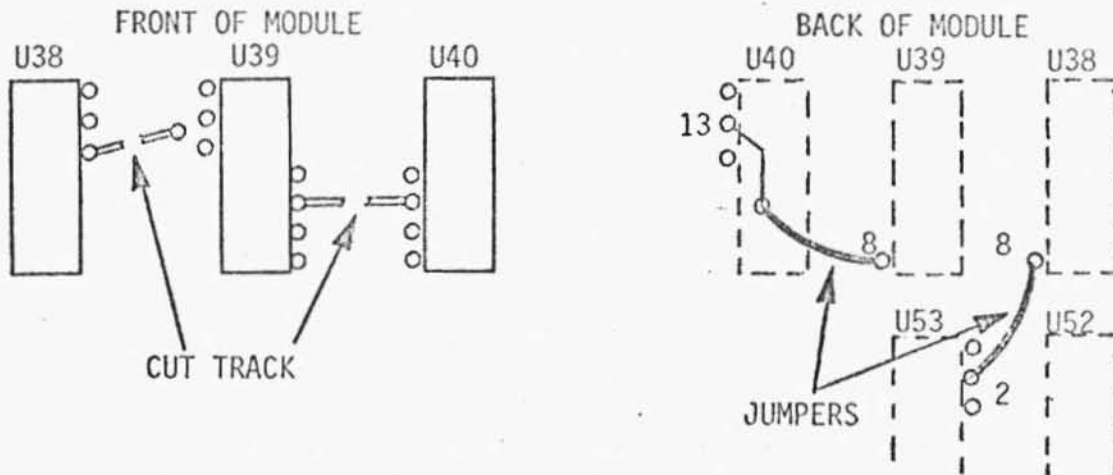
TABLE 2-3. Upper 8K Disable Option

JUMPERS			
FROM	TO	FROM	TO
K1-9	K1-2	K1-2	K1-4
K1-11	K1-6	K1-6	K1-8
K1-13	K1-12	K1-12	K1-10
K1-15	K1-16	<del>K1-14</del>	<del>K1-7</del>

Note: Remove jumper between K1-14 and K1-16, if installed.

#### 2.4.4 Configuration for Lower Clock Speeds

The Hidden Refresh Module can be operated at clock speeds between 625 KHz and .919 MHz. Circuit track must be cut and jumpers installed. The track must be cut between U38 pin 12 and U53 pin 2, and between U39 pin 10 and U40 pin 13. Jumpers must be installed between U38 pin 8 and U53 pin 2, and U39 pin 8 and U40 pin 13. The illustration below indicates the most convenient areas to accomplish this.



#### 2.5 INSTALLATION INSTRUCTIONS

Install the Hidden Refresh Memory Module as follows:

- (a) Turn power OFF on equipment module is being installed in.

**CAUTION:** INSERTING MODULE WHILE POWER IS APPLIED MAY RESULT IN DAMAGE TO COMPONENTS ON MODULE.

- (b) Install module in the selected card slot.
- (c) Turn power on.

#### 2.6 MODULE INTERCONNECTIONS

The Hidden Refresh Memory module interconnects directly with the system bus. Table 2-4 lists each pin connection, signal mnemonic, and signal characteristic. Table 2-5 identifies the Dynamic System Bus interface signals on connector P2.

TABLE 2-4. Connector P1 Bus Interface Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A,B,C	+5VDC	+5Vdc Power - Used by the module logic circuits.
D		Not Used
E	$\overline{\text{NMI}}$	NON-MASKABLE INTERRUPT - A low-going, <u>edge-sensitive</u> output to the MPU. Jumper selectable <u>PARITY ERROR</u> output. The MPU will wait until it completes the instruction being executed before it recognizes the request. At that time, regardless of the logic state of the Interrupt Mask bit in the MPU Condition Code Register, the MPU will begin executing the non-maskable interrupt (parity error).
F,H		Not Used
J	$\phi 2$	Phase 2 - One of the bi-phase clock signals generated by the clock circuit on the MPU Module.
K		Not Used
L	MEM CLK	MEMORY CLOCK - The basic clock signal generated by the MPU Module and used to control timing and refresh.
M	-12VDC	-12 Vdc Power - Used to develop the -5 Vdc used by the module logic circuits.
N-S		Not Used
T	+12VDC	+12 Vdc Power - Used by the module logic circuits.
U,V		Not Used
W	PARITY ERROR	PARITY ERROR - When used in a system with a DEbug II Module, this signal line is normally held high by that module. When used in a system without a DEbug II Module, this line should be held high by a user module or a jumper at K2 (See paragraph 2.4.2). Whenever a parity error is detected, this signal is forced low for one clock cycle.
X,Y,Z		Not Used
$\overline{\text{H}}$	$\overline{\text{D3}}$	DATA bus (bit 3) - One of 8 bi-directional data lines used to provide a two-way transfer between the MPU Module and all other plug-in modules within the system. The data bus drivers on the other modules are in their off or high impedance state except when selected during a memory read or write operation.
$\overline{\text{J}}$	$\overline{\text{D7}}$	DATA bus (bit 7) - Same as $\overline{\text{D3}}$ on Pin $\overline{\text{H}}$ .
$\overline{\text{K}}$	$\overline{\text{D2}}$	DATA bus (bit 2) - Same as $\overline{\text{D3}}$ on Pin $\overline{\text{H}}$ .
$\overline{\text{L}}$	$\overline{\text{D6}}$	DATA bus (bit 6) - Same as $\overline{\text{D3}}$ on Pin $\overline{\text{H}}$ .
$\overline{\text{M}}$	A14	ADDRESS bus (bit 14) - One of 16 address lines from the MPU Module that permits the MPU to select any addressable memory location within the system.
$\overline{\text{N}}$	A13	ADDRESS bus (bit 13) - Same as A14 on Pin $\overline{\text{M}}$ .

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
$\bar{P}$	A10	ADDRESS bus (bit 10) - Same as A14 on Pin $\bar{M}$ .
$\bar{R}$	A9	ADDRESS bus (bit 9) - Same as A14 on Pin $\bar{M}$ .
$\bar{S}$	A6	ADDRESS bus (bit 6) - Same as A14 on Pin $\bar{M}$ .
$\bar{T}$	A5	ADDRESS bus (bit 5) - Same as A14 on Pin $\bar{M}$ .
$\bar{U}$	A2	ADDRESS bus (bit 2) - Same as A14 on Pin $\bar{M}$ .
$\bar{V}$	A1	ADDRESS bus (bit 1) - Same as A14 on Pin $\bar{M}$ .
$\bar{W}, \bar{X}, \bar{Y}$	GND	GROUND
1,2,3	+5 VDC	+5 Vdc Power - Used by the module logic circuits
4		Not Used
5	RESET	RESET - This signal is used to reset the parity error flip-flop. The reset will occur when power is initially applied to the system.
6	R/W	READ/WRITE - This signal is generated by the MPU Module and indicates to the other modules contained within the system that the MPU is performing a memory read (high) or write (low) operation. The normal standby state of this signal is read (high). Additionally, when the MPU is halted, this signal will be in the read state.
7-9		Not Used
10	VUA	VALID USER'S ADDRESS - When high, this signal indicates that the address on the address bus is valid.
11	-12 VDC	-12 Vdc Power - Used to develop the -5 Vdc used by the module logic circuits.
12-15		Not Used
16	+12 VDC	+12 Vdc Power - Used by the module logic circuits.
17-18		Not Used
19	VXA	VALID EXECUTIVE ADDRESS - A high-level signal generated by the DEbug II Module in place of the VUA signal when the EXORciser II is operating in the Dual Map Mode and the EXbug program is addressing the Executive portion of the memory map. When the Hidden Refresh memory Module is used with the EXORciser, the upper 8K of memory must be disabled (see paragraph 2.4.3.1). Failure to set the appropriate switches on the DEbug II Module will make it impossible to access the memory on the Hidden Refresh Memory Module.
20-28		Not Used
29	$\bar{D1}$	DATA bus (bit 1) - Same as $\bar{D3}$ on Pin $\bar{H}$ .
30	$\bar{D5}$	DATA bus (bit 5) - Same as $\bar{D3}$ on Pin $\bar{H}$ .
31	$\bar{D0}$	DATA bus (bit 0) - Same as $\bar{D3}$ on Pin $\bar{H}$ .
32	$\bar{D4}$	DATA bus (bit 4) - Same as $\bar{D3}$ on Pin $\bar{H}$ .

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
33	A15	ADDRESS bus (bit 15) - Same as A14 on Pin $\bar{M}$ .
34	A12	ADDRESS bus (bit 12) - Same as A14 on Pin $\bar{M}$ .
35	A11	ADDRESS bus (bit 11) - Same as A14 on Pin $\bar{M}$ .
36	A8	ADDRESS bus (bit 8) - Same as A14 on Pin $\bar{M}$ .
37	A7	ADDRESS bus (bit 7) - Same as A14 on Pin $\bar{M}$ .
38	A4	ADDRESS bus (bit 4) - Same as A14 on Pin $\bar{M}$ .
39	A3	ADDRESS bus (bit 3) - Same as A14 on Pin $\bar{M}$ .
40	A $\emptyset$	ADDRESS bus (bit $\emptyset$ ) - Same as A14 on Pin $\bar{M}$ .
41,42,43	GND	GROUND

TABLE 2-5. Connector P2 Dynamic System Bus

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
17	PARITY ERROR	PARITY ERROR - Same as PARITY ERROR on P1-W.
18	GND	GROUND
19	PAGE ENA	PAGE ENABLE - If a user builds a controller that can convert the VMA signal from the MPU into one of several "pages," an unlimited number of "pages" of 64K bytes can be realized.



### 3.1 INTRODUCTION

This chapter provides a block diagram description of the Hidden Refresh Memory Module. A block diagram of the module is illustrated in Figure 3-1 and the schematic diagram is presented in Figure 3-3.

### 3.2 BLOCK DIAGRAM DESCRIPTION

The Hidden Refresh Memory Module receives the 16 address lines A0-A15, a MEM CLK (memory clock) timing signal, VUA (Valid User's Address), VXA (Valid Executive Address), R/W (Read/Write), and  $\phi 2$  clock signal during each memory operation. In addition, in a memory read operation, this module also receives the eight data bits  $\overline{D0-D7}$  from the MPU.

The MC6800 MPU is designed to operate on a two-phase clock. Phase 1 ( $\phi 1$ ) is dedicated to internal MPU operations. Phase 2 ( $\phi 2$ ) is used to access external memory and I/O. This leaves all external RAM idle during  $\phi 1$  of the MPU cycle.

The Hidden Refresh Module utilizes this idle memory time to refresh the dynamic memory. The memory cycle can then be broken down into two parts:

- $\phi 1$  - REFRESH
- $\phi 2$  - ACCESS

Refer to Figure 3-1, block diagram, for the following discussion.

#### 3.2.1 $\phi 1$ REFRESH

During  $\phi 1$  of the cycle a row address is applied to the memory array by the refresh counter. Then one of the four  $\overline{RAS1-RAS4}$  (Row Address Strobe) is generated. This causes one of the four memory blocks (rows) to refresh an internal row of its storage cells. During refresh all memory outputs remain in the tri-state mode. During the following  $\phi 2$  half cycle, the row address counter is incremented in preparation for the next refresh half cycle.

#### 3.2.2 $\phi 2$ ACCESS

When the MEM CLK (memory clock) signal is received, a 7 bit (A6-11, A13) row address is routed from the system bus to the Memory Array by the Address Bus Latches. Two additional address bits (A14, A15) are decoded by Address Select Logic to direct a  $\overline{RAS}$  signal to the appropriate block of memory. Then a 7 bit (A0-A5, A12) column address is routed to the Memory Array and  $\overline{CAS}$  (Column Address Strobe) is applied to all blocks of memory. The  $\overline{CAS}$  signal causes all memory outputs to be tri-stated except the block which previously received the  $\overline{RAS}$  signal.

Read Operation - When a memory read is executed, the contents of the selected location is routed to the system bus via the data bus buffers. The Parity Check circuit monitors these data lines. If a parity error is detected, a  $\overline{PARITY ERROR}$  signal is generated which is maintained for the remainder of the cycle.

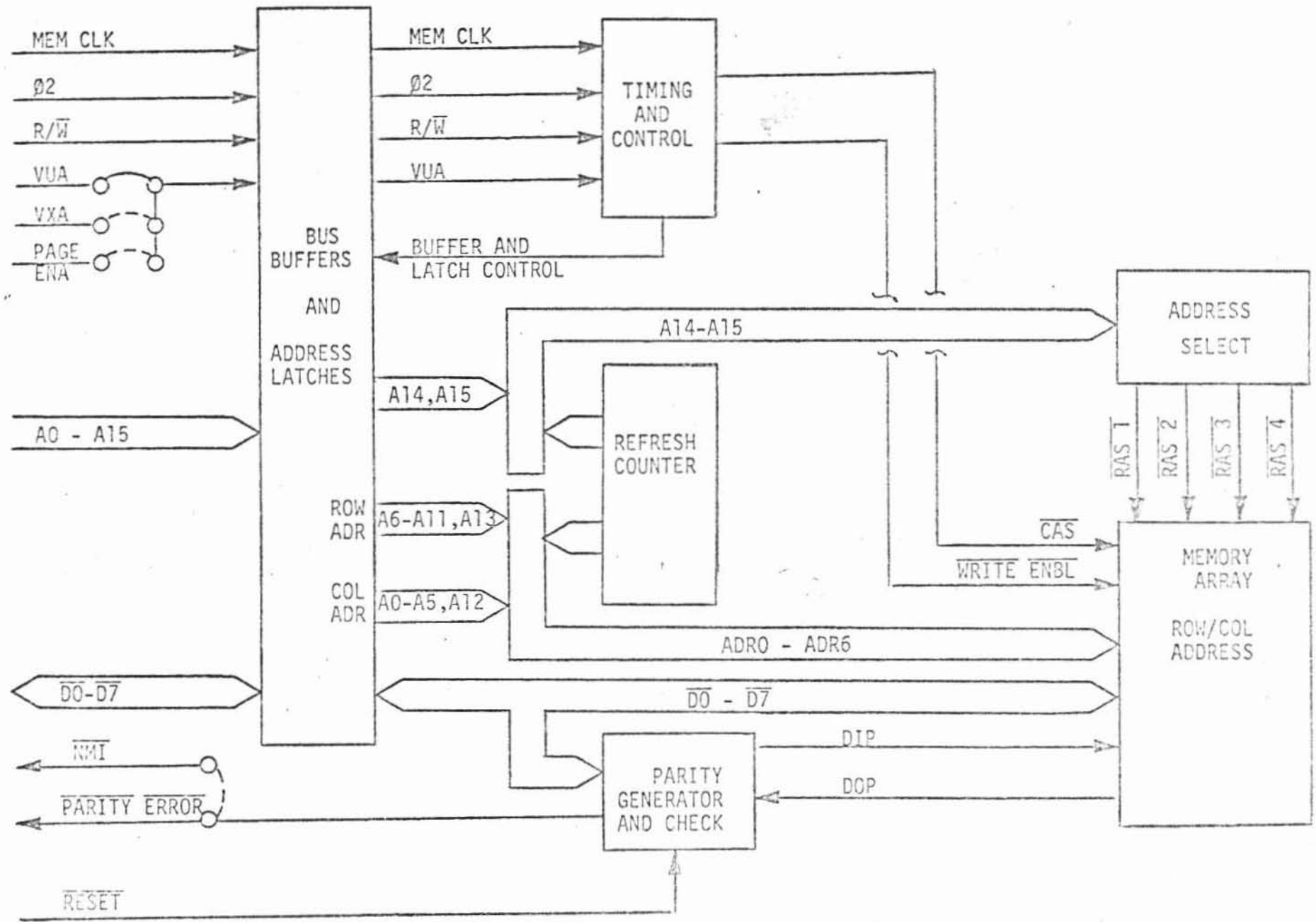


FIGURE 3-1. Hidden Refresh Memory Module Block Diagram

Write Operation - When a memory write is executed, a  $\overline{WE}$  (Write Enable) signal is applied to the Memory Array. The data bus buffers are enabled to route the 8 bits of data to the Memory Array and the Parity Generator. This writes the data into memory together with the parity bit from the parity generator.

### 3.3 TIMING SEQUENCE GENERATION

The rising edge of the MEM CLK signal clocks flip-flop U49 which outputs a transition to delay line 1 (U52). This transition then propagates through all three delay lines (U52, U39, U33) generating the various timing pulses on the outputs of X-OR gates U40 and U53. These timing pulses are shown in Figure 3-2. Once the timing sequence begins, the flip-flop will not generate any further transitions until at least 900 nsec later when the last delay line output is fed back to the flip-flop D input.

#### 3.3.1 Access Half-cycle Timing

The falling edge of the signal generated at TP7 causes the following:

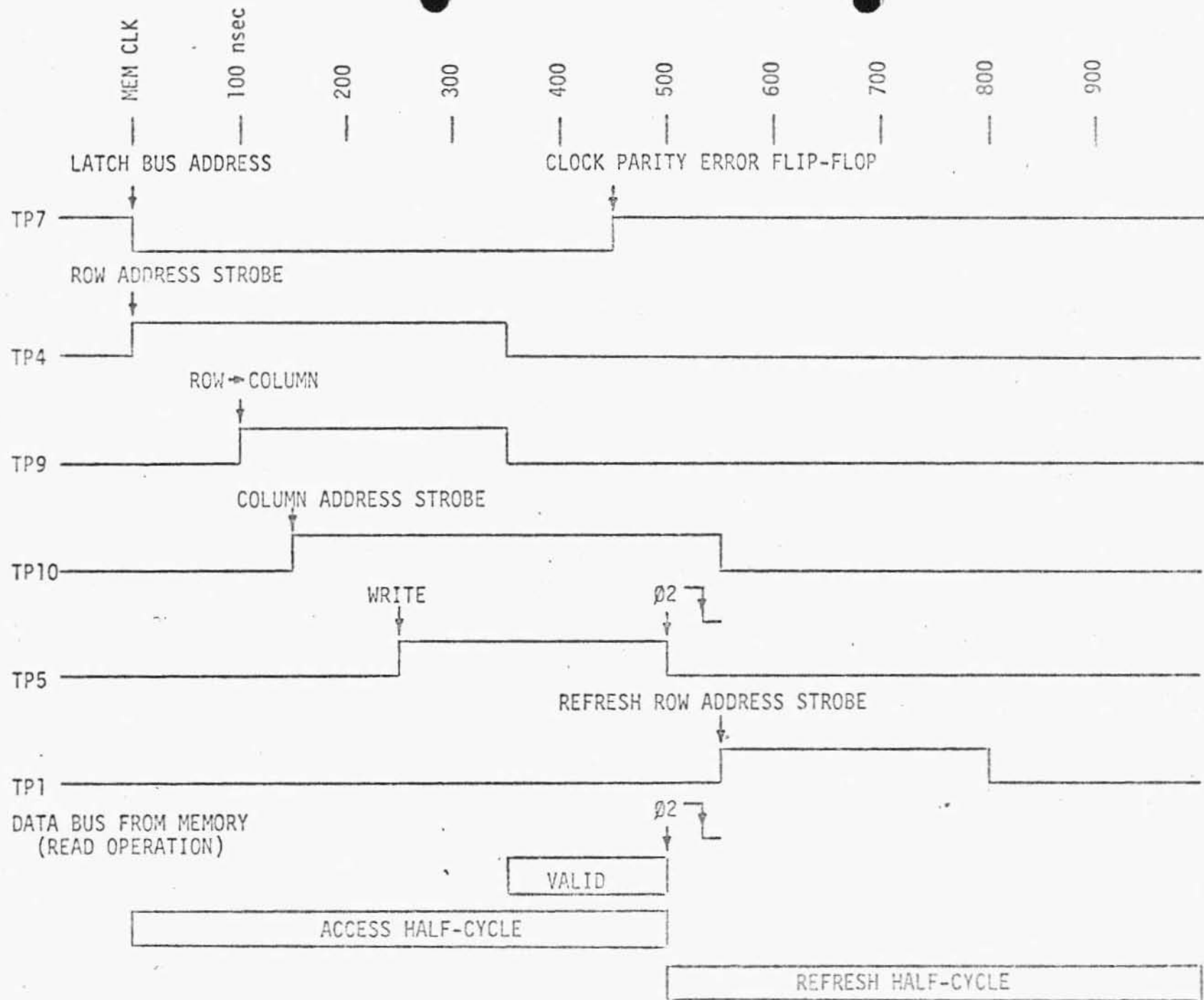
1. Latches the bus address levels (U60, U61, U62).
2. Tri-states the Refresh Counter output lines (U46, U47, U48).
3. Routes the row address levels to the Memory Array by enabling U61, U58 tri-state drivers.

At the same time, a rising edge on TP4 (in conjunction with a high VUA signal) enables decoder U59. The address latched on the A12-A15 lines generates a  $\overline{RAS}$  (Row Address Strobe) which latches the row address into one of 16K memory blocks (rows). The same rising edge clocks flip-flop U41 generating a BOARD SELECTED signal which enables data bus drivers U56 and U57 if the board is being read. After the row address has been held for about 100 nsec, the rising edge of the signal on TP9 tri-states the row drivers of U61 and U58 and turns on the column drivers of U62 and U58. This column address is then allowed to stabilize for about 50 nsec prior to the rising edge of the signal on TP10 which strobes it into memory. This column address strobe, unlike the row address strobe, is applied to all memory devices in the array. This causes all memories which did not receive a row address strobe to tri-state their outputs.

If the R/W line is in the write mode, the rising edge of the signal on TP5 causes the data entering through the data buffers (U56, U57) to be strobed into memory along with the parity bit generated by U42.

If the R/W line is in the read mode, this strobe is inhibited and valid data appears on the DOX lines 200 nsec after the column address strobe. U43 then generates an odd/even parity signal which is latched into flip-flop U41 on the rising edge of the signal on TP7. The resulting parity error, if a parity error has been detected, will be maintained on the system bus until the flip-flop is clocked again on the following cycle.

The falling edge of the  $\phi 2$  signal tri-states the data bus drivers, at the end of the access half cycle by presetting flip-flop U41.



3-4

FIGURE 3-2. Timing Diagram

### 3.3.2 Refresh Half-cycle Timing

The rising edge of the signal at TP7 approximately 450 nsec into the cycle tri-states all of the address bus latch outputs (U60, U61, U62, U58) and enables the output drivers of the three refresh counters (U46, U47, U48). These address lines are allowed to stabilize for about 100 nsec before the rising edge of the signal on TP1 strobes them into the memory array. This causes an entire row of storage cells in the memory devices to be refreshed (no column address is required).

The refresh row address is maintained on the outputs of the refresh counters until the beginning of the next memory cycle. At that time the falling edge of the signal on TP7 simultaneously tri-states the refresh counter outputs and increments the counter.







CHAPTER 4

PARTS

4.1 INTRODUCTION

This chapter provides the parts list (Table 4-1) and the parts location (Figure 4-1) for the Hidden Refresh Memory Module. The parts list reflects the latest issue of hardware at the time of printing.

TABLE 4-1. Hidden Refresh Memory Module Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFECTIVITY
	84DW6737X01	Printed Wiring Board, Hidden Refresh Memory Module	K
	55NW9403A05	Ejector, Circuit Card with Roll Pin Attachment, 2 required	K
C1-C4, C6, C10, C14, C18, C22, C26, C30, C34, C38, C78-C90, C92, C93, C95-C105, C107, C108	21NW9702A09	Capacitor, Fixed, Ceramic, 0.1 MFD at 50 VDC (41 required - 16K module only)	K
C1-C4, C6, C8, C10, C12, C14, C16, C18, C20, C22, C24, C26, C28, C30, C32, C34, C36, C38, C40, C78-C90, C92, C93, C95-C105, C107, C108	21NW9702A09	Capacitor, Fixed, Ceramic, 0.1 MFD at 50 VDC (50 required - 32K module only)	K
C1-C4, C6, C8, C10, C12, C14, C16, C18, C20, C22, C24, C26, C28, C30, C32, C34, C36, C38, C40, C42, C46, C50, C54, C58, C62, C66, C70, C74, C76, C78-C90, C92, C93, C95-C105, C107, C108	21NW9702A09	Capacitor, Fixed, Ceramic, 0.1 MFD at 50 VDC (60 required - 48K module only)	K

TABLE 4-1. Hidden Refresh Memory Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFECTIVITY
C1-4,C6,C8, C10,C12,C14, C16,C18,C20, C22,C24,C26, C28,C30,C32, C34,C36,C38, C40,C42,C44, C46,C48,C50, C52,C54,C56, C58,C60,C62, C64,C66,C68, C70,C72,C74, C76,C78-C90, C92,C93,C95- C105,C107, C108	21NW9702A09	Capacitor, Fixed, Ceramic, 0.1 MFD at 50 VDC (68 required - 64K module only)	K
C5,C9,C13, C17,C21,C25, C29,C33,C37, C106	21NW9604A08	Capacitor, Fixed, Ceramic, 1.0 MFD at 50 VDC (10 required - 16K module only)	K
C5,C7,C9,C11, C13,C15,C17, C19,C21,C23, C25,C27,C29, C31,C33,C35, C37,C39,C106	21NW9604A08	Capacitor, Fixed, Ceramic, 1.0 MFD at 50 VDC (19 required - 32K module only)	K
C5-C39,C41, C45,C49,C53, C57,C61,C65, C69,C73,C106	21NW9604A08	Capacitor, Fixed, Ceramic, 1.0 MFD at 50 VDC (28 required - 48K module only)	K
C5,C7,C9,C11, C13,C15,C17, C19,C21,C23, C25,C27,C29, C31,C33,C35, C37,C39,C41, C43,C45,C47, C49,C51,C53, C55,C57,C59, C61,C63,C65, C67,C69,C71, C73,C75,C106	21NW9604A08	Capacitor, Fixed, Ceramic, 1.0 MFD at 50 VDC (37 required - 64K module only)	K
C77,C91,C94	23NW9618A33	Capacitor, Electrolytic, 25 MFD at 16 VDC, -10 +50 Pct.	K
K1	28NW9802B34	Header, Double Row Post, 16 pin	K
P2	28NW9802C12	Header, Double Row Post, 20 pin	K
RP1,RP2	51NW9626A40	Resistor Network,5/1K ohm, 6 pin	K
RP3,RP4,RP8	51NW9626A36	Resistor Network, 3/100 ohm, 6 pin	K
RP5,RP7	51NW9626A44	Resistor Network, 3/33 ohm, 6 pin	K

TABLE 4-1. Hidden Refresh Memory Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFECTIVITY
R1,R7	06SW-124C49	Resistor, Fixed, Carbon, 1K ohm, 10%, 1/4 W	K
R2	06SW-124A25	Resistor, Fixed, Carbon, 100 ohm, 5%, 1/4 W	K
R3-R6	06SW-124A21	Resistor, Fixed, Carbon, 68 ohm, 5%, 1/4 W	K
R8	06SW124A13	Resistor, Fixed, Carbon, 33 ohm, 5%, 1/4 W	K
TP1-TP10	29NW9805A46	Terminal, Feed-thru, wire-wrap	K
U1,U3,U5,U7, U9,U11,U13, U15,U17	51NW9615E37	I.C. MCM4116C20 (9 required - 16K module only)	K
U1-U18	51NW9615E37	I.C. MCM4116C20 (18 required - 32K module only)	K
U1-U18,U19, U21,U23,U25, U27,U29,U31, U33,U35	51NW9615E37	I.C. MCM4116C20 (27 required - 48K module only)	K
U1-U36	51NW9615E37	I.C. MCM4116C20 (36 required - 64K module only)	K
U37	51NW9615D32	I.C. SN74S02N	K
U38,U52	01NW9804B62	Delay Line, Digital, 250 nsec	K
U39	01NW9804B63	Delay Line, Digital, 515 nsec	K
U40,U53	51NW9615C58	I.C. SN74S86N	K
U41,U49	51NW9615C95	I.C. SN74S74N	K
U42,U43	51NW9615F12	I.C. SN74LS280N	K
U44	51NW9615F35	I.C. DM74LS21N	K
U45	51NW9615A79	I.C. SN7432N	K
U46,U47,U48	51NW9615F36	I.C. DM8556N	K
U50	51NW9615C96	I.C. SN74S04N	K
U54	51NW9615C36	I.C. 8T98	K
U55,U63	51NW9615C94	I.C. SN74S00N	K
U56,U57	51NW9615F19	I.C. 8T26A	K
U58	51NW9615F34	I.C. DM74125N	K
U59	51NW9615D91	I.C. SN74S139N	K
U60,U61,U62	51NW9615E32	I.C. DS3645N	K
Y1	51NW9615C39	I.C. MC7905CP	K
	28NW9802B88	Header, Double Row Post, 6 pin, 2 required (Use at ADR ENA and K2)	K
	28NW9802C29	Header, Double Row Post, 4 pin	K
	28NW9802B07	Socket, DIL, 16 pin (9 required - 16K module; 18 required - 32K module) (27 required - 48K module; 36 required - 64K module)	K

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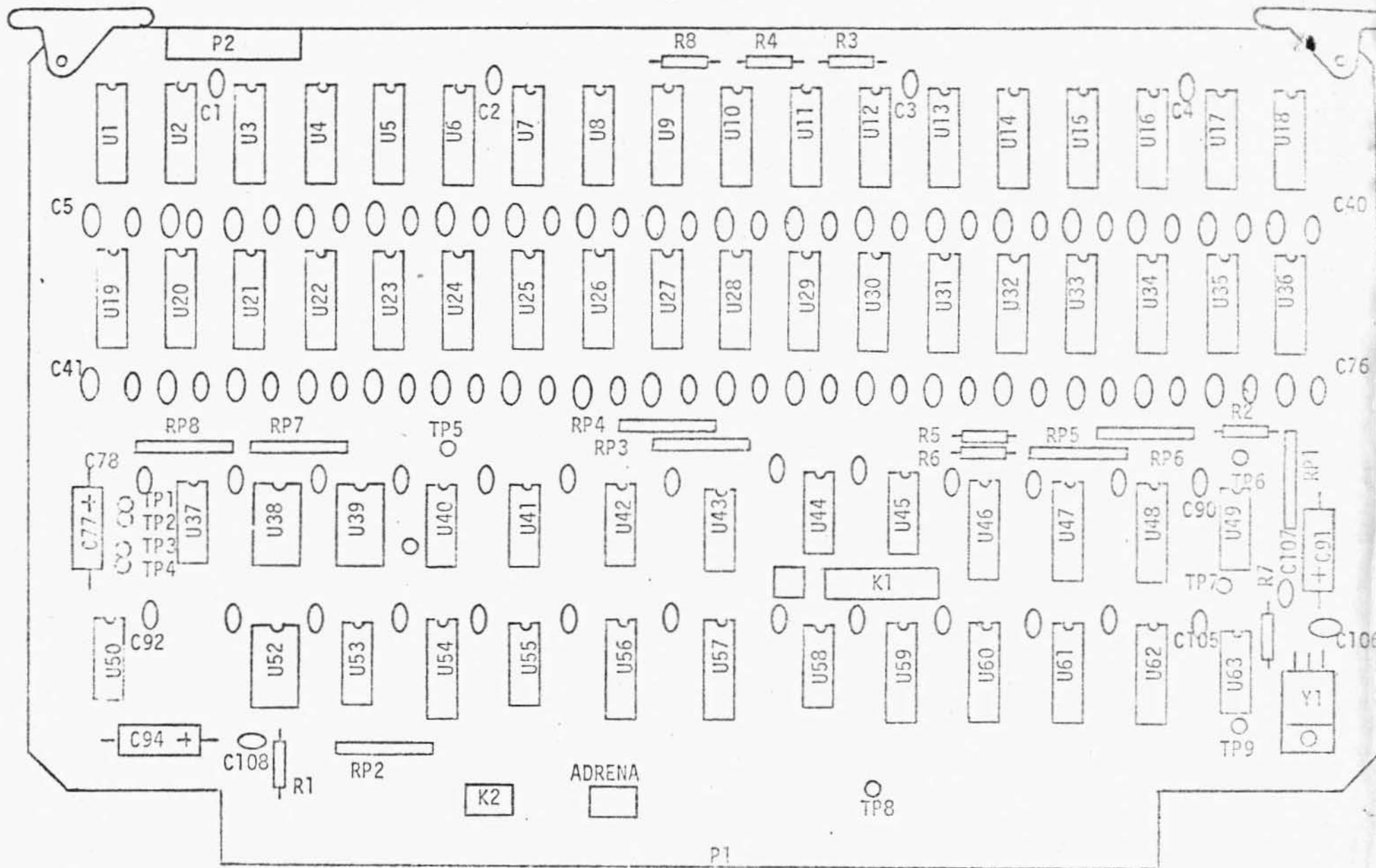


FIGURE 5-1. Typical Hidden Refresh Memory Module Parts Location