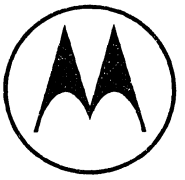
POWER

DEVICE DATA

MOTOROLA

POWER TRANSISTORS & THYRISTORS



MOTOROLA

POWER DEVICE DATA

Prepared by
Technical Information Center

This book presents technical data for Motorola's broad line of silicon power transistors, thyristors, and triggers. Complete specifications for preferred devices are provided in the form of data sheets. In addition, selection guides provide a quick comparison of characteristics to simplify the task of choosing the best device for a circuit.

The information in this book has been carefully checked and is believed to be reliable; however, no responsibility is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of semiconductor devices any license under the patent rights of any manufacturer.

First Edition

Printed in U.S.A.

MOTOROLA POWER DEVICES IN BRIEF

SILICON POWER TRANSISTORS

Wide Range of Transistor Specifications

Motorola offers more than 600 standard (off the shelf) power transistors to cover the widest range of applications at the lowest cost.

Current Range — 0.5 to 70 Amperes
Voltage Range — 25 to 1500 Volts
Power Dissipation Range — 1 to 300 Watts

Darlingtons, Too

Darlington transistors represent the integrated circuits of the power field. Consisting of two transistors, two resistors, and (up to) two diodes, they achieve gain figures up to 20,000 in a single package. Rapid line expansion, and the resulting widespread implementation make Motorola Darlingtons highly cost effective in a fast-growing number of applications.

Complete Selection of Popular Packages

In metal and plastic, Motorola offers a wide range of packages to match thermal, electrical and cost requirements.

Chips, Chips, Chips!

Designing a hybrid? Motorola's wide range of power transistors is available. . . UNENCAPSULATED: Check with your Motorola sales representative for price and delivery quotations.

Specials Unlimited

Need a unique transistor with specifications not available off-the-shelf? Chances are Motorola can produce it quickly and inexpensively. Routine use of four major power processes* and more than two decades of experience in the pioneering of new structures and geometries provide the insight and capability to meet any required specification within the limits of state-of-the-art technology.

**Routinely Used Processes and Their Specific Attributes*

Process	Feature
Planar Double and Triple Diffused	Good frequency response (f_T 25 MHz) combined with BV_{CEO} of 200 V, which can be extended to 450 V by use of a "field plate" diffusion. Available in both NPN and PNP types, for fast switches or high-frequency amplifiers where dc SOA is of little concern.
Mesa Double and Triple Diffused	A high-voltage process capable of attaining 2000 V breakdowns, with low to medium gain, medium speed and ruggedness, at low cost. NPN process only. Used in auto ignition, Switchmode regulators and TV horizontal outputs.
EpiBase	A predictable epitaxial base grown on thick collector silicon produces a workhorse transistor with 4-10 MHz f_T, 40-150 V BV_{CEO}, and 70 A current capability in both PNP and NPN. Applications for the economical standards include audio amplifiers, inductive power switches and low-frequency voltage regulators and converters.
PowerBase	Using a thick epitaxial base region, with mask-oriented voltage profile control, PowerBase combines the advantages of EpiBase with the superior SOA characteristics of the single-diffused process. Moreover, it extends these SOA characteristics to PNP devices as well as to the NPN structures obtainable with single-diffused technology.

THYRISTORS

Characteristics and Ratings for Your Triggered Power Switching Applications

The wide variety of Thyristor and Trigger devices offered by Motorola is intended to serve a diversified market, in which each application demands particular voltage, current, trigger and package characteristics. Thyristors are divided into these classes:

Silicon Controlled Rectifiers (SCRs)—
For dc and half-wave ac applications
Current Range — 0.5 to 50 Amperes, rms (Radar pulse modulators to 1000 Amperes, peak)
Voltage Range — 25 to 800 Volts

Triacs — For full-wave ac applications
Current Range — 0.8 to 40 Amperes rms
Voltage Range — 25 to 800 Volts

— And Triggers

To meet the wide variety of input requirements, the following Trigger Devices are supplied by Motorola:

Unijunction Transistors (UJT) — For unidirectional, fixed threshold SCR triggering.

Programmable Unijunction Transistors (PUT) — For externally preset SCR triggering.

Bilateral Triggers (DIAC) — For bidirectional Triac Triggering

Silicon Bilateral Switches (SBS) — For bidirectional, externally synchronized triggering.

Optically Coupled Triac Drivers — For driving isolated loads from sensitive logic sources.

Just the Package You've Been Looking For!

More than 20 packages, both metal and plastic, with a variety of plastic package leadform options. Such variety allows flexibility of mounting in sockets, printed circuit boards, and on heat sinks, for higher dissipation applications. High power metal thyristors are available in press-fit, stud, isolated stud or isolated flange, for ease of mounting.

Radar Pulse Modulators Handle 1000 Amperes Peak

A line of high speed, high pulse current SCRs can provide the massive, short duration pulses, with minimum variations in rise time, needed by today's radar systems. JAN specification is available for military applications.

Experience, Flexibility and Mass-Production Expertise

Recognizing that Thyristor users often have technical requirements that no available standard type can meet, Motorola's engineers can quickly evaluate new applications and produce specially specified Thyristors with the confidence of having done it, in volume, many times before.

Ruggedness and Reliability

Motorola Thyristors are designed into thousands of high-stress power switching applications worldwide . . . and have proven themselves in the real world.

For example, the Plastic Thyristor Reliability Guide shows samples with no failure after 1000 hours of High Temperature Reverse Blocking, 10,000 Power Cycles, 50 cycles of Method 1051 Temperature Cycle, 4000 hours of High Temperature Storage, and much more. Motorola Thyristors can take it!

Alphanumeric Index

1

Alphanumeric Index

1

Alphanumeric Index (Continued)

Alphanumeric Index (Continued)

Alphanumeric Index (Continued)

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Alphanumeric Index (Continued)

Power Transistor Selector Guide

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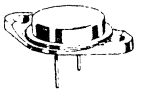
Motorola Standard Silicon Power Transistors Arranged by Package

TO-3



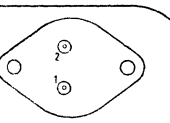
CASE 11-01 – 40-mil pins

MODIFIED TO-3

CASE 197-01 – 60-mil pins

For single side mounting in power range of 87.5 to 300 watts, at 25°C.

Devices shown have 40-mil pins unless otherwise noted.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

I_C Cont Amps	$V_{CEO(sus)}$ Volts	Device Type		h_{FE} @ I_C		Resistive Switching t_s μs	Resistive Switching t_f μs @ I_C		f_T MHz	P_D (Case) Watts
Max	Min	NPN	PNP	Min/Max	Amp	Max	Max	Amp	Min	@ 25°C
2.5	1300*	BU204		2	2		0.75 typ	2	4 typ	36
	1500*	BU205		2	2		0.75 typ	2	4 typ	36
		MJ12002		1.11	2		1	2	4 typ	75
3	250	2N5838		8/40	3	1 typ	0.4 typ	3	5	100
	275	2N5839		10/50	2	1 typ	0.4 typ	3	5	100
	350	2N5840		10/50	2	1 typ	0.4 typ	3	5	100
3.5	325	2N3902		30/90	1	1.2 typ	0.1 typ	1	2.8	100
5	120	2N4347		15/60	2					100
	200	MJ410		30/90	1				2.5	100
	250	MJ3029		30 min	0.4		1	3		125
	300	MJ411		30/90	1				2.5	100
		2N6542		7/35	3	4	0.8	3	6	100
	325	MJ3030		3.75 min	3		1	3		125
	400	2N6543		7/35	3	4	0.8	3	6	100
	1300*	BU207		2.25 min	4.5		1	4.5	7.5	125
	1500*	BU208		2.25 min	4.5		1	4.5	7.5	125
		MJ12004		2.5 min	4.5		1	4.5	4	100
6	100	2N5758	2N6226	25/100	3	0.7 typ	0.5 typ	3	1	150
	120	2N5759	2N6227	20/80	3	0.7 typ	0.5 typ	3	1	150
	140	2N5760	2N6228	15/60	3	0.7 typ	0.5 typ	3	1	150
	250	MJ15011	MJ15012	20/100	2					200
7	300	MJ3041		250 min	2.5					100
	350	MJ3042		250 min	2.5					100
7.5	60	2N3447		40/120	5	2	0.35	5	10	115
	80	2N3448		40/120	5	2	0.35	5	10	115
8	60	MJ1000	MJ900	1k min	3					90
		2N6055	2N6053	750/18k	4	1.5 typ	1.5 typ	4	4#	100
	80	MJ1001	MJ901	1k min	3					90
		2N6056	2N6054	750/18k	4	1.5 typ	1.5 typ	4	4#	100
	250	2N6306		15/75	3	1.6	0.4	3	5	125
	300	2N6307		15/75	3	1.6	0.4	3	5	125
		2N6544		7/35	5	4	1	5	6	125
	350	2N6308		12/60	3	1.6	0.4	5	5	125
	400	2N6545		7/35	5	4	1	5	6	125
	1400*	MJ10011		20 min	4		1	4		80
	1500*	MJ12005		5 min	5		1	5		100
10	40	2N6383		1k/20k	5				20#	100
	60	2N3713	2N3789	15 min	3	0.3 typ	0.4 typ	5	4	150
		2N3715	2N3791	30 min	3	0.3 typ	0.4 typ	5	4	150
		2N5877	2N5875	20/100	4	1	0.8	4	4	150
		MJ3000	MJ2500	1k min	5					150
		2N6384		1k/20k	5				20#	100
	80	2N3714	2N3790	15 min	3	0.3 typ	0.4 typ	5	4	150
		2N3716	2N3792	30 min	3	0.3 typ	0.4 typ	5	4	150
		2N5878	2N5876	20/100	4	1	0.8	4	4	150
		MJ3001	MJ2501	1k min	5					150
		2N6385		1k/20k	5				20#	100
	100	2N5632	2N6229	25/100	5	0.9 typ	0.9 typ	5	1	150
	120	2N5633	2N6230	20/80	5	0.9 typ	0.9 typ	5	1	150
	140	2N5634	2N6231	15/60	5	0.9 typ	0.9 typ	5	1	150
		2N3442		20/70	4					117
	150	MJ11018	MJ11017	100 min	10					200
	200	MJ11020	MJ11019	100 min	10					200

*BV_{CEX}

$|h_{fe}|$ @ 1 MHz

(continued)

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I_C Cont Amps	$V_{CEO(sus)}$ Volts	Device Type		h_{FE} @ I_C		Resistive Switching τ_s μs	Resistive Switching τ_f μs	Resistive Switching @ I_C	f_T MHz	P_D (Case) Watts
Max	Min	NPN	PNP	Min/Max	Amp	Max	Max	Amp	Min	@ 25°C
10 (cont'd)	250	MJ11022	MJ11021	100 min	10					200
		MJ15011	MJ15012	20/100	2					200
	325	MJ413		20/80	0.5				2.5	125
		MJ423		30/90	1				2.5	125
		MJ431		15/35	2.5				2.5	125
	350	MJ13014		8/20	5	2	0.5	5		150
		MJ10002		30/300	5	2.5	1	5	10#	150
		MJ10006		30/300	5	1.5	0.5	5	10#	150
	400	MJ10003		30/300	5	2.5	1	5	10#	150
		MJ10007		30/300	5	1.5	0.5	5	10#	150
		MJ10012		100/2k	6	15	15	6		175
		MJ13015		8/20	5	2	0.5	5		150
	450	SDT13304		10/40	5	1.6 typ	0.35 typ	5	15 typ	125*
	500	SDT13305		10/40	5	1.6 typ	0.35 typ	5	15 typ	125*
12	40	2N6569	2N6594	15/200	4	5	1.5	2	1.5 to 15	100
	60	2N6057	2N6050	750/18k	6	1.6 typ	1.5 typ	6	4#	150
	80	2N6058	2N6051	750/18k	6	1.6 typ	1.5 typ	6	4#	150
	100	2N6059	2N6052	750/18k	6	1.6 typ	1.5 typ	6	4#	150
15	60	2N3055	MJ2955	20/70	4	0.7 typ	0.3 typ	4	2.5	115
		2N3055A	MJ2955A	20/70	4				0.8	115
		2N6576		2k/20k	4	2	7	10	10 to 200#	120
		2N5881	2N5879	20/100	6	1	0.8	6	4	160
	80	2N5882	2N5880	20/100	6	1	0.8	6	4	160
	90	2N6577		2k/20k	4	2	7	10	10 to 200#	120
	120	MJ15015	MJ15016	20/70	4				1	180
		2N6578		2k/20k	4	2	7	10	10 to 200#	120
	140	MJ15001	MJ15002	25/150	4				2	200
	200	2N6249		10/50	10	3.5	1	10	2.5	175
	275	2N6250		8/50	10	3.5	1	10	2.5	175
	300	2N6546		6/30	10	4	0.7	10	6 to 24	175
	350	2N6251		6/50	10	3.5	1	10	2.5	175
	400	2N6547		6/30	10	4	0.7	10	6 to 24	175
	550	MJ10013		10/250	10	2.5	0.8	10		175
	600	MJ10014		10/250	10	2.5	0.8	10		175
16	60	MJ4033	MJ4030	1k min	10					150
	80	MJ4034	MJ4031	1k min	10					150
	100	2N5629	2N6029	25/100	8	1.2 typ	1.2 typ	8	1	200
		MJ4035	MJ4032	1k min	10					150
	120	2N5630	2N6030	20/80	8	1.2 typ	1.2 typ	8	1	200
	140	2N3773	2N6609	15/60	8	1.1 typ	1.5 typ	8	4	150
		2N5631	2N6031	15/60	8	1.2 typ	1.2 typ	8	1	200
20	40	2N6257		15/75	8				2	150
	60	2N3772		15/60	10				2	150
		2N6282	2N6285	750/18k	10	2.5 typ	2.5 typ	10	4#	160
	75	2N5039		20/100	10	1.5	0.5	10	60	140
	80	2N5303	2N5745	15/60	10	2	1	10	2	200
		2N6283	2N6286	750/18k	10	2.5 typ	2.5 typ	10	4#	160
	90	2N5038		20/100	12	1.5	0.5	12	60	140
	100	2N6284	2N6287	750/18k	10	2.5 typ	2.5 typ	10	4#	160
	140	MJ15003	MJ15004	25/150	5				2	250
	200	MJ13330		8/40	10	3.5	0.7	10	5 to 40	175
	250	MJ13331		8/40	10	3.5	0.7	10	5 to 40	175
	350	MJ10000		40/400	10	3	1.8	10	10#	175
		MJ10004		40/400	10	1.5	0.5	10	10#	175
		MJ13332		10/60	5	4	0.7	10		175
	400	MJ10001		40/400	10	3	1.8	10	10#	175
		MJ10005		40/400	10	1.5	0.5	10	10#	175
		MJ13333		10/60	5	4	0.7	10		175
	450	MJ10008		30/300	10	2	0.6	10	8#	175
		MJ13334		10/60	5	4	.07	10		175
	500	MJ10009		30/300	10	2	0.6	10	8#	175
		MJ13335		10/60	5	4	0.7	10		175
25	60	2N5885	2N5883	20/100	10	1	0.8	10	4	200
	80	2N5886	2N5884	20/100	10	1	0.8	10	4	200
			2N6436	20/80	10	1	0.25	10	40	200
	100	2N6338		30/120	10	1	0.25	10	40	200
			2N6437	20/80	10	1	0.25	10	40	200
	120	2N6339		30/120	10	1	0.25	10	40	200
			2N6438	20/80	10	1	0.25	10	40	200

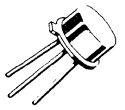
$|h_{fe}|$ @ 1 MHz * @ 100° C

(continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} @ I_C Min/Max	I_C Amp	Resistive Switching t_s μs Max	t_f μs @ I_C Max	I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
25 (cont'd)	140	2N6340		30/120	10	1	0.25	10	40	200
	150	2N6341		30/120	10	1	0.25	10	40	200
	200	MJ15022	MJ15023	15/60	8				5	250
	250	MJ15024	MJ15025	15/60	8				5	250
30	40	2N3771		15/60	15				2	150
		2N5301	2N4398	15/60	15	2	1	10	2	200
	60	2N5302	2N4399	15/60	15	2	1	10	2	200
		MJ11012	MJ11011	1k min	20				4#	200
	90	MJ11014	MJ11013	1k min	20				4#	200
	100	MJ802	MJ4502	25/100	7.5				2	200
	120	MJ11016	MJ11015	1k min	20				4#	200
50	60	2N5685●	2N5683●	15/60	25	0.5 typ	0.3 typ	25	2	300
		MJ11028●	MJ11029●	400 min	50					300
	80	2N5686●	2N5684●	15/60	25	0.5 typ	0.3 typ	25	2	300
			2N6377●	30/120	20	0.8	0.25	20	30	250
	90	MJ11030	MJ11031	400 min	50					300
	100	2N6274●	2N6378●	30/120	20	0.8	0.25	20	30	250
	120	2N6275●	2N6379●	30/120	20	0.8	0.25	20	30	250
		MJ11032●	MJ11033●	400 min	50					300
	140	2N6276●		30/120	20	0.8	0.25	20	30	250
	150	2N6277●		30/120	20	0.8	0.25	20	30	250
	400	MJ10015●		10 min	40	2.5	1.0	20		250
	500	MJ10016●		10 min	40	2.5	1.0	20		250
70	60	MJ14000●	MJ14001●	15/100	50					300
	80	MJ14002●	MJ14003●	15/100	50					300

●Modified TO-3

#| h_{fe} | @ 1 MHz

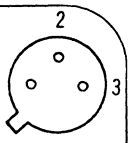


TO-39

CASE 79-02

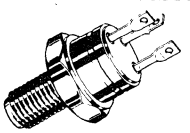
Lead mounted devices; power dissipation of 5 to 10 watts at 25°C ambient.

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR



I_C Cont Amps	$V_{CEO(sus)}$ Volts	Device Type		h_{FE} @ I_C		Resistive Switching t_s μs	Resistive Switching t_f μs @ I_C		f_T MHz	P_D (Case) Watts
Max	Min	NPN	PNP	Min/Max	Amp	Max	Max	Amp	Min	@ 25°C
0.5	150		2N4929	20 min	0.05				100	5
	200		2N4930	20 min	0.05				20	5
			MJ4645	20 min	0.5	0.72*		0.05	40	5
	250		2N4931	20 min	0.03				20	5
	300		MJ4646	20 min	0.5	0.72*		0.05	40	5
	400		MJ4647	20 min	0.5	0.72*		0.05	30	5
1	40	2N3110		25/70	0.5	0.6*		0.15	60	5
			2N3244	50/150	0.5	0.14	0.045	0.5	175	5
			2N3467	40/120	0.5	0.06	0.03	0.5	175	5
	50		2N3245	30/90	0.5	0.12	0.045	0.5	150	5
			2N3468	40/120	0.5	0.06	0.03	0.5	175	5
	60		MM4030	25/40	0.5	0.35			100/400	7
			MM4032	70/100	0.5	0.35			150/500	7
	65		MM4036	20/40	0.5	0.175*			60	7
	80	2N3019		50 min	0.5				100	5
		2N3020		30/100	0.5				100	5
			MM4031	25/40	0.5	0.35			100/400	7
			MM4033	70/100	0.5	0.35			150/500	7
	100	2N5681	2N5679	40/150	0.25				30	10
	120	2N5682	2N5680	40/150	0.25				30	10
	200		2N5415	30 min	0.05				15	5
	250	2N3440		40/160	0.02				15	5
	300		2N5416	30 min	0.05				15	5
	350	2N3439		40/160	0.02				15	5
1.5	40		2N3762	30/120	1	0.08	0.035	1	180	4
	50	2N3734		30/120	1	0.03	0.03	1	250	4
	60		2N3763	20/80	1	0.08	0.035	1	150	4
	75	2N3735		20/80	1	0.03	0.03	1	250	4
2	40	2N5859		30/120	0.5	0.035	0.035	0.1	250	5
	60	2N5861		25/120	0.5	0.035	0.035	0.5	200	5
	100	MM3007	MM5007	50/250	0.25				30	8
3	40	2N4237	2N4234	30/150	0.25				3	6
	60	2N4238	2N4235	30/150	0.25				3	6
		2N3506		40/200	1.5	0.055	0.035	1.5	60	5
	80	2N4239	2N4236	30/150	0.25				3	6
		2N3507		40/200	1.5	0.055	0.035	1.5	60	5
4	60	2N4877		20/100	4	1.5	0.5	4	30	10
5	60		MJ8100	25/180	2	1	0.15	2	30	10
	80	2N5337	2N6191	60/240	2	2	0.2	2	30	10
	100	2N5339	2N6193	60/240	2	2	0.2	2	30	10

*t_{off}

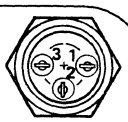


TO-59

CASE 160-03

Stud mounted devices; power dissipation 60 watts at 25°C case.

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR



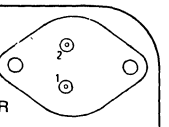
I_C Cont Amps	$V_{CEO(sus)}$ Volts	Device Type		h_{FE} @ I_C		Resistive Switching t_s μs	Resistive Switching t_f μs @ I_C		f_T MHz	P_D (Case) Watts
Max	Min	NPN	PNP	Min/Max	Amp	Max	Max	Amp	Min	@ 25°C
7	80	2N5347		60/240	2	2	0.2	2	30	60
	100	2N5349		60/240	2	2	0.2	2	30	60
10	60		MJ6700	25/180	2	1	0.15	2	30	60
	80		2N6187	60/240	2	2	0.2	2	30	60
	100		2N6189	60/240	2	2	0.2	2	30	60

TO-66

CASE 80-02

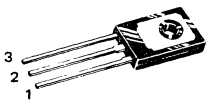
For single side mounting; power dissipation of 20 to 90 watts at 25°C case.

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR



I_C Cont Amps	$V_{CEO(sus)}$ Volts	Device Type		h_{FE} @ I_C		Resistive Switching t_s μs	Resistive Switching t_f μs @ I_C		f_T MHz	P_D (Case) Watts
Max	Min	NPN	PNP	Min/Max	Amp	Max	Max	Amp	Min	@ 25°C
1	40		2N4898	20/100	0.5	0.6 typ	0.3 typ	0.5	3	25
	60		2N4899	20/100	0.5	0.6 typ	0.3 typ	0.5	3	25
	80	2N4912	2N4900	20/100	0.5	0.6 typ	0.3 typ	0.5	3	25
	175	2N3583	2N6420	40/200	0.5	2 typ	0.23 typ	0.5	10	35
	225	2N3738	2N6424	40/200	0.1	3 typ	0.3 typ	0.1	10	20
	250		2N5344	25/100	0.5	0.6	0.1	0.5	60	40
	300	2N3739	2N6425	40/200	0.1	3 typ	0.3 typ	0.1	10	20
			2N5345	25/100	0.5	0.6	0.1	0.5	60	40
2	120	2N5050		25/100	0.75	3.5	1.2	0.75	10	40
	150	2N5051		25/100	0.75	3.5	1.2	0.75	10	40
	200	2N5052		25/100	0.75	3.5	1.2	0.75	10	40
	225		2N6211	10/100	1	2.5	0.6	1	20	35
	250	2N3584	2N6421	25/100	1	4	3	1	10	35
	300		2N6212	10/100	1	2.5	0.6	1	20	35
		2N3585	2N6422	25/100	1	4	3	1	10	35
	350		2N6213	10/100	1	2.5	0.6	1	20	35
3	140	2N3441		25/100	0.5				0.2	25
4	60		2N3740	30/100	0.25	1.3 typ	0.27 typ	0.25	4	25
		2N3054,A	2N6049	25/100	0.5	1 typ	0.3 typ	0.5	3	75
		2N3766		40/160	0.5	0.9 typ	0.09 typ	0.5	10	20
		2N6294	2N6296	750/18k	2	0.9 typ	0.7 typ	2	4#	50
	80		2N3741	30/100	0.25	1.3 typ	0.27 typ	0.25	4	25
		2N3767		40/160	0.5	0.9 typ	0.09 typ	0.5	10	20
		2N6295	2N6297	750/18k	2	0.9 typ	0.7 typ	2	4	50
5	40	2N4231A	2N6312	25/100	1.5	0.5 typ	0.2 typ	1.5	4	75
	60	2N4232A	2N6313	25/100	1.5	0.5 typ	0.2 typ	1.5	4	75
	80	2N4233A	2N6314	25/100	1.5	0.5 typ	0.2 typ	1.5	4	75
	225	2N6233		25/125	1	3.5	0.5	1	20	50
	275	2N6234		25/125	1	3.5	0.5	1	20	50
	325	2N6235		25/125	1	3.5	0.5	1	20	50
7	60	2N6315	2N6317	20/100	2.5	1	0.8	2.5	4	90
	80	2N5428		60/240	2	2	0.2	2	30	40
		2N6316	2N6318	20/100	2.5	1	0.8	2.5	4	90
	100	2N5430		60/240	2	2	0.2	2	30	40
	150	MJ15014	MJ15013	40 min	1				10	50
	250	2N6078		12/70	1.2	2.8	0.3	1.2	1	45
	275	2N6077		12/70	1.2	2.8	0.3	1.2	1	45
8	60	2N6300	2N6298	750/18k	4	1.5 typ	1.5 typ	4	4#	75
	80	2N6301	2N6299	750/18k	4	1.5 typ	1.5 typ	4	4#	75
10	80	2N6495		10/60	10	0.15 typ	0.05 typ	10	25	70

| h_{fe} | @ 1 MHz



TO-126

CASE 77-03

PLASTIC

For lead mounted applications or use with heat sinks; power dissipation of 15 to 40 watts at 25°C case.

STYLE 1
(Case 77 on Tables):
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 3
(Case 77R on Tables)
PIN 1. BASE
2. COLLECTOR
3. EMITTER

I_C Cont Amps	$V_{CEO(sus)}$ Volts	Device Type		h_{FE} @ I_C		Resistive Switching t_s μs	Resistive Switching t_f μs @ I_C		f_T MHz	P_D (Case) Watts
Max	Min	NPN	PNP	Min/Max	Amp	Max	Max	Amp	Min	@ 25°C
0.3	250	MJE3440		40/160	0.02				15	15
	350	MJE3439		40/160	0.02				15	15
0.5	150	MJE341		25/200	0.05				15	20.8
	200	MJE344		30/300	0.05				15	20.8

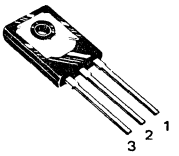
(continued)

TO-126 (continued)

I_C Cont Amps	$V_{CEO(sus)}$ Volts	Device Type		h_{FE} @ I_C		Resistive Switching t_s μs	Resistive Switching t_f μs @ I_C		f_T MHz	P_D (Case) Watts
Max	Min	NPN	PNP	Min/Max	Amp	Max	Max	Amp	Min	@ 25°C
0.5 (cont'd)	250	2N5655		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20
	300	MJE340	MJE350	30/240	0.05					20.8
		2N5656		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20
	350	2N5657		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20
1	40	2N4921	2N4918	20/100	0.5	0.6 typ	0.3 typ	0.5	3	30
	60	2N4922	2N4919	20/100	0.5	0.6 typ	0.3 typ	0.5	3	30
	80	2N4923	2N4920	20/100	0.5	0.6 typ	0.3 typ	0.5	3	30
1.5	300	MJE13002●		5/25	1	4	0.7	1	5	40
	400	MJE13003●		5/25	1	4	0.7	1	5	40
3	30	MJE520	MJE370	25 min	1					25
	40	MJE180	MJE170	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5
	60	MJE181	MJE171	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5
	80	MJE182	MJE172	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5
4	40	MJE3300●	MJE3310●	1k min	1				20	15
		2N5190	2N5193	25/100	1.5	0.4 typ	0.4 typ	1.5	2	40
		MJE521	MJE371	40 min	1					40
		2N6037	2N6034	750/18k	2	1.7 typ	1.2 typ	2	25	40
	60	MJE3301●	MJE3311●	1k min	1				20#	15
		2N5191	2N5194	25/100	1.5	0.4 typ	0.4 typ	1.5	2	40
		MJE800	MJE700	750 min	1.5				1#	40
		2N6038	2N6035	750/18k	2	1.7 typ	1.2 typ	2	25	40
	80	MJE3302●	MJE3312●	1k min	1				20#	15
		2N5192	2N5195	25/100	1.5	0.4 typ	0.4 typ	1.5	2	40
		2N6039	2N6036	750/18k	2	1.7 typ	1.2 typ	2	25	40
	100	MJE243	MJE253	40/120	0.2	0.7 typ	0.08 typ	0.2	40	15
5	25	MJE200	MJE210	45/180	2	0.13 typ	0.035 typ	2	65	15

●Case 77R (Style 3)

| h_{fe} | @ 1 MHz



TO-127

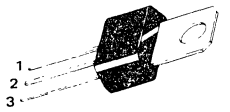
CASE 90-05
PLASTIC

For lead mounted applications or use with heat sinks; power dissipation of 40 to 100 watts at 25°C case.

STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

I_C Cont Amps	$V_{CEO(sus)}$ Volts	Device Type		h_{FE} @ I_C		Resistive Switching t_s μs	Resistive Switching t_f μs @ I_C		f_T MHz	P_D (Case) Watts
Max	Min	NPN	PNP	Min/Max	Amp	Max	Max	Amp	Min	@ 25°C
5	40	2N5977	2N5974	20/120	2.5	0.45 typ	0.18 typ	2.5	2	75
	50	MJE205	MJE105	25/100	2					65
	60	2N5978	2N5975	25/100	2.5	0.45 typ	0.18 typ	2.5	2	75
	80	2N5979	2N5976	20/120	2.5	0.45 typ	0.18 typ	2.5	2	75
8	60	MJE6043	MJE6040	1k/20k	4	1.5 typ	1.5 typ	4	4#	75
	80	MJE6044	MJE6041	1k/20k	4	1.5 typ	1.5 typ	4	4#	75
	100	MJE6045	MJE6042	1k/20k	4	1.5 typ	1.5 typ	4	4#	75
10	60	MJE3055	MJE2955	20/70	4				2	90
12	40	2N5989	2N5986	20/120	6	0.5 typ	0.25 typ	6	2	100
	60	2N5990	2N5987	20/120	6	0.5 typ	0.25 typ	6	2	100
	80	2N5991	2N5988	20/120	6	0.5 typ	0.25 typ	6	2	100
15	40	MJE1660	MJE1290	20/100	5				3	90
	60	MJE1661	MJE1291	20/100	5				3	90

| h_{fe} | @ 1 MHz

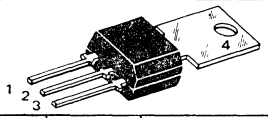


CASE 152

For lead or chassis mounted application or use with heat sink; power dissipation of 1 to 10 watts.

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

I_C Cont Amps	$V_{CEO(sus)}$ Volts	Device Type		h_{FE} @ I_C		Resistive Switching t_s μs	t_f μs @ I_C		f_T MHz	P_D (Case) Watts
Max	Min	NPN	PNP	Min/Max	Amp	Max	Max	Amp	Min	@ 25°C
0.5	65	MPS-U31		10 min	0.1					10
	300	MPS-U10	MPS-U60	30 min	0.030				60	10
0.8	40	MPS-U02	MPS-U52	30 min	0.5				150	10
1	120	MPS-U03		40 min	0.010				100	10
	180	MPS-U04		40 min	0.010				100	10
2	30	MPS-U01	MPS-U51	50 min	1				50	10
	40	MPS-U01A	MPS-U51A	50 min	1				50	10
		MPS-U45	MPS-U95	4k min	1				100	10
	60	MPS-U05	MPS-U55	60 min	0.25				50	10
	80	MPS-U06	MPS-U56	60 min	0.25				50	10
	100	MPS-U07	MPS-U57	30 min	0.25				50	10



TO-202

CASE 306

For lead or chassis mounted applications or use with heat sink; power dissipation of 2 to 10 watts.

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

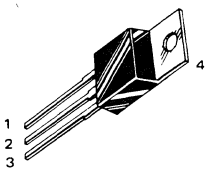
I_C Cont Amps	$V_{CEO(sus)}$ Volts	Device Type		h_{FE} @ I_C		Resistive Switching t_s μs	t_f μs @ I_C		f_T MHz	P_D (Case) Watts
Max	Min	NPN	PNP	Min/Max	Amp	Max	Max	Amp	Min	@ 25°C
0.1	250	D40N1		30/90	0.02				50	6.25
		D40N2		60/180	0.02				50	6.25
	300	D40N3		30/90	0.02				50	6.25
		D40N4		60/180	0.02				50	6.25
0.5	30	D40C1		10k/60k	0.2	0.35 typ	0.8 typ	1	100	6.25
		D40C2		40k min	0.2	0.35 typ	0.8 typ	1	100	6.25
	40	D40C4		10k/60k	0.2	0.35 typ	0.8 typ	1	100	6.25
		D40C5		40k min	0.2	0.35 typ	0.8 typ	1	100	6.25
	120	D40P1		40 min	0.08	2.5		0.08	50	6.25
	150	2N6591		40/200	0.1				35	10
	180	D40P3		40 min	0.08	2.5		0.08	50	6.25
	200	2N6592		30/200	0.1				35	10
	225	D40P5		40 min	0.08	2.5		0.08	50	6.25
	250	2N6557		40/180	0.03				45	10
		MDS20		40/250	0.03				60	10
		2N6593		30/200	0.1				35	10
	300	2N6558		40/180	0.03				45	10
			MDS60	30 min	0.03				45	10
		MDS21		40/250	0.03				60	10
	350	2N6559		40/180	0.03				45	10

(continued)

I_C Cont Amps	$V_{CEO(sus)}$ Volts	Device Type		h_{FE} @ I_C		Resistive Switching t_s	t_f	@ I_C	f_T	P_D (Case) Watts
Max	Min	NPN	PNP	Min/Max	Amp	μs Max	μs Max	Amp	MHz Min	@ 25°C
1	30	D40D1	D41D1	10 min	1	0.2 typ	0.05 typ	1	200 typ	10
		D40D2	D41D2	20 min	1	0.2 typ	0.05 typ	1	200 typ	10
	45	D40D4	D41D4	10 min	1	0.2 typ	0.05 typ	1	200 typ	10
		D40D5	D41D5	10 min	1	0.2 typ	0.05 typ	1	200 typ	10
	60	2N6551	2N6554	25 min	0.5				75	10
		D40D7	D41D7	10 min	1	0.2 typ	0.05 typ	1	200 typ	10
		D40D8	D41D8	10 min	1	0.2 typ	0.05 typ	1	200 typ	10
	75	D40D10	D41D10	10 min	1	0.2 typ	0.05 typ	1	200 typ	10
		D40D11	D41D11	10 min	1	0.2 typ	0.05 typ	1	200 typ	10
		D40D13	D41D13	50/150	0.1	0.2 typ	0.05 typ	1	200 typ	10
		D40D14	D41D14	50/150	0.1	0.2 typ	0.05 typ	1	200 typ	10
	80	2N6552	2N6555	25 min	0.5				75	10
	100	2N6553	2N6556	25 min	0.5				75	10
2	30	D40E1	D41E1	10 min	1	0.4 typ	0.17 typ	1	230 typ	8
		D40K1	D41K1	1k min	1.5				100	10
		D40K3	D41K3	1k min	1.0				100	10
	40	2N6548		5k min	1				100	10
		2N6549		3k min	1				100	10
	50	D40K2	D41K2	1k min	1.5				100	10
		D40K4	D41K4	1k min	1.0				100	10
	60	D40E5	D41E5	10 min	1	0.4 typ	0.17 typ	1	230 typ	8
	80	D40E7	D41E7	10 min	1	0.4 typ	0.17 typ	1	220 typ	8
3	40	MDS26†	MDS76†	30 min	1.0				50	10
	60	MDS23	MDS73	50/250	0.1				50	10
		MDS27†	MDS77†	30 min	1.0				50	10
	65*	MDS1678		10 min	1.5				100	10
	80	MDS24	MDS74	50/250	0.1				50	10
	100	MDS25	MDS75	50/250	0.1				50	10

*V_{CBO}

† Pin out is: Pin1-Base, Pin2-Collector, Pin3-Emitter, Pin4-Collector



TO-220

CASE 221A-02
PLASTIC

For lead mounted applications or use with heat sinks; power dissipation of 40 to 100 watts at 25°C case.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

I_C Cont Amps	$V_{CEO(sus)}$ Volts	Device Type		h_{FE} @ I_C		Resistive Switching t_s	t_f	@ I_C	f_T	P_D (Case) Watts
Max	Min	NPN	PNP	Min/Max	Amp	μs Max	μs Max	Amp	MHz Min	@ 25°C
0.5	350	MJE2360T		15 min	0.1				10 typ	30
		MJE2361T		40 min	0.1				10 typ	30
1	40	TIP29	TIP30	15/75	1	0.6 typ	0.3 typ	1	3	30
	60	TIP29A	TIP30A	15/75	1	0.6 typ	0.3 typ	1	3	30
	80	TIP29B	TIP30B	15/75	1	0.6 typ	0.3 typ	1	3	30
	100	TIP29C	TIP30C	15/75	1	0.6 typ	0.3 typ	1	3	30
	250	TIP47		30/150	0.3	2 typ	0.18 typ	0.3	10	40
	300	TIP48		30/150	0.3	2 typ	0.18 typ	0.3	10	40
	350	TIP49		30/150	0.3	2 typ	0.18 typ	0.3	10	40
	400	TIP50		30/150	0.3	2 typ	0.18 typ	0.3	10	40
2	60	TIP110	TIP115	500 min	2	1.7 typ	1.3 typ	2	25#	50
	80	TIP111	TIP116	500 min	2	1.7 typ	1.3 typ	2	25#	50
	100	TIP112	TIP117	500 min	2	1.7 typ	1.3 typ	2	25#	50
3	40	TIP31	TIP32	25 min	1	0.6 typ	0.3 typ	1	3	40
	60	TIP31A	TIP32A	25 min	1	0.6 typ	0.3 typ	1	3	40
	75	MJE1909		20/150	0.5				100	10
	80	TIP31B	TIP32B	25 min	1	0.6 typ	0.3 typ	1	3	40
	100	TIP31C	TIP32C	25 min	1	0.6 typ	0.3 typ	1	3	40

$|h_{fe}|$ @ 1 MHz

(continued)

I_C Cont Amps	$V_{CEO(sus)}$ Volts	Device Type		h_{FE} @ I_C		Resistive Switching t_s μs	Resistive Switching t_f μs	Resistive Switching @ I_C	f_T MHz	P_D (Case) Watts
Max	Min	NPN	PNP	Min/Max	Amp	Max	Max	Amp	Min	@ 25°C
4	45	2N6121	2N6124	25/100	1.5	0.4 typ	0.3 typ	1.5	2.5	40
	60	2N6122	2N6125	25/100	1.5	0.4 typ	0.3 typ	1.5	2.5	40
	80	2N6123	2N6126	20/80	1.5	0.4 typ	0.3 typ	1.5	2.5	40
	300	MJE13004		6/30	3	3	0.7	3	4	60
	400	MJE13005		6/30	3	3	0.7	3	4	60
5	60	TIP120	TIP125	1k min	3	1.5 typ	1.5 typ	3	4#	65
	80	TIP121	TIP126	1k min	3	1.5 typ	1.5 typ	3	4#	65
	100	TIP122	TIP127	1k min	3	1.5 typ	1.5 typ	4	4#	75
	250	MJE51T		5 min	5	2 typ*		2.5	2.5	80
		2N6497		10/75	2.5	1.8	0.8	2.5	5	80
	300	MJE52T		5 min	5	2 typ*		2.5	2.5	80
		2N6498		10/75	2.5	1.8	0.8	2.5	5	80
	350	MJE53T		5 min	5	2 typ*		2.5	2.5	80
		2N6499		10/75	2.5	1.8	0.8	2.5	5	80
6	40	TIP41	TIP42	15/75	3	0.4 typ	0.15 typ	3	3	65
	60	TIP41A	TIP42A	15/75	3	0.4 typ	0.15 typ	3	3	65
	80	TIP41B	TIP42B	15/75	3	0.4 typ	0.15 typ	3	3	65
	100	TIP41C	TIP42C	15/75	3	0.4 typ	0.15 typ	3	3	65
7	30	2N6288	2N6111	30/150	3	0.4 typ	0.15 typ	3	4	40
	50	2N6290	2N6109	30/150	2.5	0.4 typ	0.15 typ	3	4	40
	70	2N6292	2N6107	30/150	3	0.4 typ	0.15 typ	3	4	40
8	40	2N6386		1k/20k	3				20#	65
	60	2N6043	2N6040	1k/10k	4	1.5 typ	1.5 typ	3	4#	75
		TIP100	TIP105	1k/20k	3	1.5 typ	1.5 typ	3	4#	80
	80	2N6044	2N6041	1k/10k	4	1.5 typ	1.5 typ	3	4#	75
		TIP101	TIP106	1k/20k	3	1.5 typ	1.5 typ	3	4#	80
	100	2N6045	2N6042	1k/10k	3	1.5 typ	1.5 typ	3	4#	75
		TIP102	TIP107	1k/20k	3	1.5 typ	1.5 typ	3	4#	80
	120	MJE15028	MJE15029	40 min	3				30	50
	150	MJE15030	MJE15031	40 min	3				30	50
	300	MJE13006		6/30	5	3	0.7	5	4	80
	400	MJE13007		6/30	5	3	0.7	5	4	80
10	60	MJE2801T	MJE2901T	25/100	3					75
		MJE3055T	MJE2955T	20/70	4					75
		2N6387		1k/20k	5				20#	65
	80	2N6388		1k/20k	5				20#	65
		D44H10	D45H10	20 min	4				50 typ	50
		D44H11	D45H11	40 min	4				50 typ	50
12	300	MJE13008		6/30	8	3	0.7	8	4	100
	400	MJE13009		6/30	8	3	0.7	8	4	100
15	40	2N6486	2N6489	20/150	5	0.6 typ	0.3 typ	5	5	75
	60	2N6487	2N6490	20/150	5	0.6 typ	0.3 typ	5	5	75
	80	2N6488	2N6491	20/150	5	0.6 typ	0.3 typ	5	5	75

*t_{off}

$|h_{fe}|$ @ 1 MHz

Motorola Power Darlingtons

Power Darlingtons provide high gain, high input impedance and reduced component count, with subsequent space savings. Devices are listed in ascending order of maximum continuous collector current, I_C Cont, and open base sustaining voltage, $V_{CEO\ (sus)}$.
Complementary types are grouped together.

I_C Cont Amps	$V_{CEO(sus)}$ Volts	Device Type		h_{FE}	@ I_C	Resistive Switching t_s	t_f	@ I_C	$\lvert h_{fe} \rvert$	P_D (Case) Watts	Case
Max	Min	NPN	PNP	Min/Max	Amp	μs Max	μs Max	Amp	@ 1 MHz Min	@ 25°C	JEDEC/MOT
0.5	30	D40C1		10k/60k	0.2	0.35 typ	0.8 typ	1	75 typ	10	TO-202/306
		D40C2		40k min	0.2	0.35 typ	0.8 typ	1	75 typ	6.25	
	40	D40C4		10k/60k	0.2	0.35 typ	0.8 typ	1	75 typ	10	TO-202/306
		D40C5		40k min	0.2	0.35 typ	0.8 typ	1	75 typ	6.25	
2	30	D40K1	D41K1	1k min	1.5				75 typ	10	TO-202/306
		D40K3	D41K3	1k min	1.0				75 typ	10	
	40	2N6548		5k min	1				100	10	TO-202/306
		2N6549		3k min	1				100	10	TO-202/306
		MPS-U45	MPS-U95	4k min	.1				100	10	/152
	50	D40K2	D41K2	1k min	1.5				75 typ	10	TO-202/306
		D40K4	D41K4	1k min	1.0				75 typ	10	
	60	TIP110	TIP115	1k min	1	2 typ	1 typ	1	25	50	TO-220/221A
	80	TIP111	TIP116	1k min	1	2 typ	1 typ	1	25	50	TO-220/221A
	100	TIP112	TIP117	1k min	1	2 typ	1 typ	1	25	50	TO-220/221A
4	40	MJE3300	MJE3310	1k min	1				20	15	TO-126/77R
		2N6037	2N6034	750/1k	2	1.7 typ	1.2 typ	2	25	40	TO-126/77
	60	MJE3301	MJE3311	1k min	1				20	15	TO-126/77R
		MJE800	MJE700	750 min	1.5				1	40	TO-126/77
		2N6038	2N6035	750/18k	2	1.7 typ	1.2 typ	2	25	40	TO-126/77
		2N6294	2N6296	750/18k	2	0.9 typ	0.7 typ	2	4	50	TO-66/80
	80	MJE3302	MJE3312	1k min	1				20	15	TO-126/77R
		2N6039	2N6036	750/18k	2	1.7 typ	1.2 typ	2	25	40	TO-126/77
		2N6295	2N6297	750/18k	2	0.9 typ	0.7 typ	2	4	50	TO-66/80
5	60	TIP120	TIP125	1k min	3	1.5 typ	1.5 typ	3	4	65	TO-220/221A
	80	TIP121	TIP126	1k min	3	1.5 typ	1.5 typ	3	4	65	TO-220/221A
	100	TIP122	TIP127	1k min	3	1.5 typ	1.5 typ	3	4	65	TO-220/221A
7	300	MJ3041		250 min	2.5					100	TO-3/11
	350	MJ3042		250 min	2.5					100	TO-3/11
8	40	2N6386		1k/20k	3				20	65	TO-220/221A
	60	MJ1000	MJ900	1k min	3					90	TO-3/11
		TIP100	TIP105	1k/20k	3	1.5 typ	1.5 typ	3	4	80	TO-220/221A
		2N6043	2N6040	1k/10k	4	1.5 typ	1.5 typ	3	4	75	TO-220/221A
		2N6300	2N6298	750/18k	4	1.5 typ	1.5 typ	4	4	75	TO-66/80
		2N6055	2N6053	750/18k	4	1.5 typ	1.5 typ	4	4	100	TO-3/11
		MJE6043	MJE6040	1k/20k	4	1.5 typ	1.5 typ	4	2	75	TO-127/90
	80	MJ1001	MJ901	1k min	3					90	TO-3/11
		TIP101	TIP106	1k/20k	3	1.5 typ	1.5 typ	3	4	80	TO-220/221A
		2N6044	2N6041	1k/10k	4	1.5 typ	1.5 typ	3	4	75	TO-220/221A
		2N6301	2N6299	750/18k	4	1.5 typ	1.5 typ	4	4	75	TO-66/80
		2N6056	2N6054	750/18k	4	1.5 typ	1.5 typ	4	4	100	TO-3/11
		MJE6044	MJE6041	1k/20k	4	1.5 typ	1.5 typ	4	2	75	TO-127/90
	100	MJE6045	MJE6042	1k/20k	4	1.5 typ	1.5 typ	4	2	75	TO-127/90
		TIP102	TIP107	1k/20k	3	1.5 typ	1.5 typ	3	4	80	TO-220/221A
		2N6045	2N6042	1k/10k	4	1.5 typ	1.5 typ	3	4	75	TO-220/221A
	1400*	MJ10011		20 min	4		1	4		80	TO-3/11
10	40	2N6383		1k/20k	5				20	100	TO-3/11
	60	MJ3000	MJ2500	1k min	5					150	TO-3/11
		2N6387		1k/20k	5				20	65	TO-220/221A
		2N6384		1k/20k	5				20	100	TO-3/11
	80	MJ3001	MJ2501	1k min	5					150	TO-3/11
		2N6388		1k/20k	5				20	65	TO-220/221A
		2N6385		1k/20k	5				20	100	TO-3/11
	150	MJ11018	MJ11017	100 min	10					200	TO-3/11
	200	MJ11020	MJ11019	100 min	10					200	TO-3/11
	250	MJ11022	MJ11021	100 min	10					200	TO-3/11

*V_{CEX}

(continued)

I_CCont Amps	$V_{CEO(sus)}$ Volts	Device Type		h_{FE} @ I_C		Resistive Switching t_s μs	Resistive Switching t_f μs @ I_C		$\lvert h_{fe} \rvert$ @ 1 MHz	P_D (Case) Watts	Case
Max	Min	NPN	PNP	Min/Max	Amp	Max	Max	Amp	Min	@ 25°C	JEDEC/MOT
10 (cont'd)	350	MJ10002		30/300	5	2.5	1	5	10	150	TO-3/11
		MJ10006		30/300	5	1.5	0.5	5	10	150	TO-3/11
	400	MJ10003		30/300	5	2.5	1	5	10	150	TO-3/11
		MJ10007		30/300	5	1.5	0.5	5	10	150	TO-3/11
		MJ10012		100/2k	6	15	15	6		175	TO-3/11
12	60	2N6057	2N6050	750/18k	6	1.6 typ	1.5 typ	6	4	150	TO-3/11
	80	2N6058	2N6051	750/18k	6	1.6 typ	1.5 typ	6	4	150	TO-3/11
	100	2N6059	2N6052	750/18k	6	1.6 typ	1.5 typ	6	4	150	TO-3/11
15	60	2N6576		2k/20k	4	2	7	10	10/200	120	TO-3/11
	90	2N6577		2k/20k	4	2	7	10	10/200	120	TO-3/11
	120	2N6578		2k/20k	4	2	7	10	10/200	120	TO-3/11
	550	MJ10013		10/250	10	2.5	0.8	10		175	TO-3/11
	600	MJ10014		10/250	10	2.5	0.8	10		175	TO-3/11
16	60	MJ4033	MJ4030	1k min	10					150	TO-3/11
	80	MJ4034	MJ4031	1k min	10					150	TO-3/11
	100	MJ4035	MJ4032	1k min	10					150	TO-3/11
20	60	2N6282	2N6285	750/18k	10	2.5 typ	2.5 typ	10	4	160	TO-3/11
	80	2N6283	2N6286	750/18k	10	2.5 typ	2.5 typ	10	4	160	TO-3/11
	100	2N6284	2N6287	750/18k	10	2.5 typ	2.5 typ	10	4	160	TO-3/11
	350	MJ10000		40/400	10	3	1.8	10	10	175	TO-3/11
		MJ10004		40/400	10	1.5	0.5		10	175	TO-3/11
	400	MJ10001		40/400	10	3	1.8	10	10	175	TO-3/11
		MJ10005		40/400	10	1.5	0.5		10	175	TO-3/11
	450	MJ10008		30/300	10	2	0.6	10	8	175	TO-3/11
	500	MJ10009		30/300	10	2	0.6	10	8	175	TO-3/11
30	60	MJ11012	MJ11011	1k min	20				4	200	TO-3/11
	90	MJ11014	MJ11013	1k min	20				4	200	TO-3/11
	120	MJ11016	MJ11015	1k min	20				4	200	TO-3/11
50	60	MJ11028	MJ11029	400 min	50					300	TO-3 Mod/197
	90	MJ11030	MJ11031	400 min	50					300	TO-3 Mod/197
	120	MJ11032	MJ11033	400 min	50					300	TO-3 Mod/197
	400	MJ10015		10 min	40	2.5	0.5	20	1 0	250	TO-3 Mod/197
	500	MJ10016		10 min	40	2.5	0.5	20	1 0	250	TO-3 Mod/197

Power Switching Transistors

BV_{CEO} <200 V

(See next page for 200 Volts and greater.)

I_CCont Amps	$V_{CEO(sus)}$ Volts	Device Type		h_{FE} @ I_C		Resistive Switching t_s μs	Resistive Switching t_f μs @ I_C		f_T MHz	P_D (Case) Watts	Case
Max	Min	NPN	PNP	Min/Max	Amp	Max	Max	Amp	Min	@ 25°C	JEDEC/MOT
1	40		2N3244	50/150	0.5	0.14	0.045	0.5	175	5	TO-39/79
			2N3467	40/120	0.5	0.06	0.03	0.5	175	5	TO-39/79
	50		2N3245	30/90	0.5	0.12	0.045	0.5	150	5	TO-39/79
			2N3468	40/120	0.5	0.06	0.03	0.5	175	5	TO-39/79
	65		MM4036	20/40	0.5	0.175*		0.15	60	7	TO-39/79
1.5	40		2N3762	30/120	1	0.08	0.035	1	180	4	TO-39/79
	50	2N3734		30/120	1	0.03	0.03	1	250	4	TO-39/79
	60		2N3763	20/80	1	0.08	0.035	1	150	4	TO-39/79
	75	2N3735		20/80	1	0.03	0.03	1	250	4	TO-39/79
2	40	2N5859		30/120	0.5	0.035	0.035	0.1	250	5	TO-39/79
	60	2N5861		25/100	0.5	0.035	0.035	0.1	200	5	TO-39/79
	120	2N5050		25/100	0.75	3.5	1.2	0.75	10	40	TO-66/80
	150	2N5051		25/100	0.75	3.5	1.2	0.75	10	40	TO-66/80
3	40		2N3719	25/180	2	0.4*		1	60	6	TO-5/31
			2N3867	40/200	2	0.4*		1	60	6	TO-5/31
	60		2N3720	25/180	2	0.4*		1	60	6	TO-5/31
		2N3506		40/200	1.5	0.055	0.035	1 5	60	5	TO-39/79
			2N3868	30/150	2	0.4*		1	60	6	TO-5/31
	80		2N6303	30/150	2	0.4*		1	60	6	TO-5/31
		2N3507		30/150	1.5	0.055	0.035	1.5	60	5	TO-39/79

*t_{off}

(continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type NPN	Device Type PNP	h_{FE} @ I_C Min/Max	Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C	Case JEDEC/MOT
4	60	2N4877		20/100	4	1.5	0.5	4	30	10	TO-39/79
5	60		MJ8100	25/180	2	1	0.15	2	30	10	TO-39/79
	80	2N5337	2N6191	60/240	2	2	0.2	2	30	10	TO-39/79
	100	2N5339	2N6193	60/240	2	2	0.2	2	30	10	TO-39/79
7	60	2N6315	2N6317	20/100	2.5	1	0.8	2.5	4	90	TO-66/80
	80	2N5428		60/240	2	2	0.2	2	30	60	TO-66/80
		2N5347	2N6187	60/240	2	2	0.2	2	30	60	TO-59/160
		2N6316	2N6318	20/100	2.5	1	0.8	2.5	4	90	TO-66/80
	100	2N5430		60/240	2	2	0.2	2	30	60	TO-66/80
		2N5349	2N6189	60/240	2	2	0.2	2	30	60	TO-59/160
7.5	60	2N3447		40/120	5	2	0.35	5	10	115	TO-3/11
	80	2N3448		40/120	5	2	0.35	5	10	115	TO-3/11
10	60		MJ6700	25/180	2	1	0.15	2	30	60	TO-59/160
		2N5877	2N5875	20/100	4	1	0.8	4	4	150	TO-3/11
	80	2N5878	2N5876	20/100	4	1	0.8	4	4	15	TO-3/11
15	60	2N5881	2N5879	20/100	6	1	0.8	6	4	160	TO-3/11
	80	2N5882	2N5880	20/100	6	1	0.8	6	4	160	TO-3/11
20	75	2N5039		20/100	10	1.5	0.5	10	60	140	TO-3/11
	80	2N5303	2N5745	15/60	10	2	1	10	2	200	TO-3/11
	90	2N5038		20/100	12	1.5	0.5	12	60	140	TO-3/11
25	60	2N5885	2N5883	20/100	10	1	0.8	10	4	200	TO-3/11
	80	2N5886	2N5884	20/100	10	1	0.8	10	4	200	TO-3/11
			2N6436	20/80	10	1	0.25	10	40	200	TO-3/11
	100	2N6338		30/120	10	1	0.25	10	40	200	TO-3/11
			2N6437	20/80	10	1	0.25	10	40	200	TO-3/11
	120	2N6339		30/120	10	1	0.25	10	40	200	TO-3/11
			2N6438	20/80	10	1	0.25	10	40	200	TO-3/11
	140	2N6340		30/120	10	1	0.25	10	40	200	TO-3/11
	150	2N6341		30/120	10	1	0.25	10	40	200	TO-3/11
30	40	2N5301	2N4398	15/60	15	2	1	10	2	200	TO-3/11
	60	2N5302	2N4399	15/60	15	2	1	10	2	200	TO-3/11
50	80		2N6377	30/120	20	0.8					TO-3 Mod/197
	100	2N6274	2N6378	30/120	20	0.8	0.25	20	30	250	TO-3 Mod/197
	120	2N6275	2N6379	30/120	20	0.8	0.25	20	30	250	TO-3 Mod/197
	140	2N6276		30/120	20	0.8	0.25	20	30	250	TO-3 Mod/197
	150	2N6277		30/120	20	0.8	0.25	20	30	250	TO-3 Mod/197

Motorola SWITCHMODE Power Transistors

$BV_{CEO} \geq 200$ V

SWITCHMODE power transistors are useful for "off line" converters, switching regulators, deflection circuits, solenoid drivers, and motor control. SWITCHMODE devices, both regular transistor structures and Darlingtons with and without "speed-up" diodes, are completely characterized in a Designers Data Sheet format. This format includes switching information at 25°C and 100°C for both resistive and inductive loads, as well as clamped inductive reverse-bias SOA.

Other power switching devices with $BV_{CEO} \geq 200$ V, but without the SWITCHMODE label or Designers Data Sheet, are included in this table.

Devices are listed in descending order of $V_{CEO(sus)}$, I_C Cont, and V_{CEX}.

$V_{CEO(sus)}$ Volts Min	I_C Cont Amps Max	V_{CEX} Volts Min	Device Type NPN unless otherwise noted	h_{FE} @ I_C Min/Max	Amp	Resistive Switching t_s µs Max	t_f µs Max	@ I_C Amp	f_T MHz Min	Case JEDEC/MOT
750	8	1500	MJ12005	5 min	5		1	5	4 typ	TO-3/11
	5	1500	MJ12004	2.5 min	4.5		1	4.5	4 typ	TO-3/11
	2.5	1500	MJ12002	1.11	2		1	2	4 typ	TO-3/11
700	8	1400	MJ10011#	20 min	4		1	4		TO-3/11
600	15	700	MJ10014##	10/250	10	2.5	0.8	10		TO-3/11

Designers Data Sheet characterization #Darlington ##Darlington with speed-up diode

(continued)

V_{CEO} (sus) Volts Min	I_C Cont Amps Max	V_{CEX} Volts Min	Device Type NPN unless otherwise noted	h_{FE} @ I_C Min/Max	Amp	Resistive Switching t_S µs Max	t_F µs Max @ I_C Amp		f_T MHz Min	Case JEDEC/MOT
550	15	650	MJ10013##	10/250	10	2.5	0.8	10		TO-3/11
500	50	750	MJ10016##	10 min	40	2.5	1.0	20		TO-3 Mod/197
	20	750	MJ10009##	30/300	10	2	0.6	10	8**	TO-3/11
		600	MJ13335	10/60	5	4	0.7	10		TO-3/11
450	20	650	MJ10008##	30/300	10	2	0.6	10	8**	TO-3/11
		550	MJ13334	10/60	5	4	0.7	10		TO-3/11
400	50	650	MJ10015##	10 min	40	2.5	1.0	20		TO-3 Mod/197
	20	500	MJ10001#	40/400	10	3	1.8	10	10**	TO-3/11
			MJ10005##	40/400	10	1.5	0.5	10	10**	TO-3/11
			MJ13333	10/60	5	4	0.7	10		TO-3/11
	15	850	2N6547	6/30	10	4	0.7	10	6 to 24	TO-3/11
	12	700	MJE13009	6/30	8	3	0.7	8	4**	TO-220/221A
	10	550	MJ10012#	100/2k	6	6	15	15	6	TO-3/11
	10	500	MJ10003#	30/300	5	2.5	1	5	10**	TO-3/11
			MJ10007##	30/300	5	1.1	0.25	5	10**	TO-3/11
	10	450	MJ13015	8/20	5	2	0.5	5		TO-3/11
	8	850	2N6545	7/35	5	4	1	5	6	TO-3/11
		700	MJE13007	6/30	5	3	0 7	5	4	TO-220/221A
	5	850	2N6543	7/35	3	4	0.8	3	6	TO-3/11
	4	700	MJE13005	6/30	3	3	0.7	3	4	TO-220/221A
	1.5	700	MJE13003	5/25	1	4	0.7	1	5	TO-126/77R
	0.5	400	MJ4647 - PNP	20 min	0.5	0.72*		0.05	40	TO-39/79
350	20	450	MJ10000#	40/400	10	3	1 8	10	10**	TO-3/11
			MJ10004##	40/400	10	1.5	0.5	10	10**	TO-3/11
			MJ13332	10/60	5	4	0.7	10		TO-3/11
	15	375	2N6251	6/50	10	3.5	1	10	2.5	TO-3/11
	10	450	MJ10002#	30/300	5	2.5	1	5	10**	TO-3/11
			MJ10006##	30/300	5	1.5	0.5	5	10**	TO-3/11
	10	400	MJ13014	8/20	5	2	0.5	5		TO-3/11
	8	700	2N6308	12/60	3	1.6	0.4	5	5	TO-3/11
	5	450	2N6499	10/75	2.5	1.8	0.8	2.5	5	TO-220/221A
	3	375	2N5840	10/50	2	3	1.5	2	5	TO-3/11
	2	400	2N6213-PNP	10/100	1	2.5	0.6	1	4	TO-66/80
325	5	700	MJ3030	3.75 min	3		1	3		TO-3/11
		350	2N6235	25/125	1	3.5	0.5	1	20	TO-66/80
300	15	650	2N6546	6/30	10	4	0.7	10	6 to 24	TO-3/11
	12	600	MJE13008	6/30	8	3	0.7	8	4**	TO-220/221A
	8	650	2N6544	7/35	5	4	1	5	6	TO-3/11
		600	2N6307	15/75	3	1.6	0.4	3	5	TO-3/11
			MJE13006	6/30	5	3	0.7	5	4	TO-220/221A
	5	650	2N6542	7/35	3	4	0.8	3	6	TO-3/11
		400	2N6498	10/75	2.5	1 8	0.8	2.5	5	TO-220/221A
	4	600	MJE13004	6/30	3	3	0.7	3	4	TO-220/221A
	2	500	2N3585	25/100	1	4	3	1	10	TO-66/80
			2N6422-PNP	25/100	1	4	3	1	10	TO-66/80
		350	2N6212-PNP	10/100	1	2.5	0.6	1	4	TO-66/80
	1.5	600	MJE13002	5/25	1	4	0 7	1	5	TO-126/77R
	1	300	2N5345 - PNP	25/100	0.5	0.6	0.1	0.5	60	TO-66/80
	0.5	300	MJ4646 - PNP	20 min	0.5	0.72*		0.05	40	TO-39/79
275	15	300	2N6250	8/50	10	3 5	1	10	2.5	TO-3/11
	7	300	2N6077	12/70	1.2	2.8	0.3	1.2	7	TO-66/80
	5	275	2N6234	25/125	1	3.5	0.5	1	20	TO-66/80
	3	300	2N5839	10/50	2	3.75	1.5	2	5	TO-3/11
250	20	350	MJ13331	8/40	10	3.5	0.7	10	5/40	TO-3/11
	8	500	2N6306	15/75	3	1.6	0.4	3	5	TO-3/11
	7	275	2N6078	12/70	1.2	2.8	0.3	1.2	7	TO-66/80
	5	500	MJ3029	30 min	0.4		1	3		TO-3/11
		350	2N6497	10/75	2.5	1.8	0.8	2 5	5	TO-220/221A
	3	275	2N5838	10/50	2	3	1.5	3	5	TO-3/11
	2	375	2N3584	25/100	1	4	3	1	10	TO-66/80
		375	2N6421-PNP	25/100	1	4	3	1	10	TO-66/80
	1	250	2N5344-PNP	25/100	0.5	0.6	0.1	0.5	60	TO-66/80
225	2	275	2N6211	10/100	1	2.5	0.6	1	20	TO-66/80
200	20	300	MJ13330	8/40	10	3.5	0 7	10	5/40	TO-3/11
	15	225	2N6249	10/50	10	3.5	1	10	2 5	TO-3/11
	2	200	2N5052	25/100	0.75	3 5	1 2	0.75	10	TO-66/80
	0.5	200	MJ4645-PNP	20 min	0.5	0.72*		0.05	40	TO-39/79

Designers Data Sheet characterization
#Darlington
##Darlington with speed-up diode

*t_{off}

**$|h_{fe}|$ @ 1 MHz

Military Specified Power Transistors

Devices listed are active per QPL-19500 (Qualified Product List) as of June 1, 1978, with the exception of those devices marked *** which should be active by September, 1978. Check your local Motorola sales office or franchised distributor for current qualification status and availability of these devices or additions.

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I_C Cont Amps	$V_{CEO(sus)}$ Volts	Device Type		h_{FE} @ I_C		Resistive Switching t_s μs @ I_C	Resistive Switching t_f μs @ I_C		f_T MHz	P_D (Case) Watts	Case
Max	Min	NPN / #	PNP / #	Min/Max	Amp	Max	Max	Amp	Min	@ 25°C	JEDEC/MOT
0.5	200		2N4930J,/397 TX,TXV	20 min	0.05				20	5	TO-39/79
	250		2N4931J,/397 TX,TXV	20 min	0.03				20	5	TO-39/79
1	40		2N3467J,/348 TX,TXV	40/120	0.5	0.06	0.03	0.5	175	5	TO-39/79
	50		2N3468J,/348 TX,TXV	40/120	0.5	0.06	0.03	0.5	175	5	TO-39/79
	80	2N3019J,/391 TX		50 min	0.5				100	5	TO-39/79
	300	2N3739J,/402A TX		40/200	0.1	3 typ	0.3 typ	0.1	10	20	TO-66/80
1.5	40		2N3762J,/396 TX,TXV	30/120	1	0.08	0.035	1	180	4	TO-39/79
	60		2N3763J,/396 TX,TXV	20/80	1	0.08	0.035	1	150	4	TO-39/79
	75	2N3735J,/395 TX,TXV		20/80	1	0.03	0.03	1	250	4	TO-39/79
3	40	2N3506J,/349 TX,TXV	2N3867J,/350A TX,TXV	40/200	2	0.4*		1	60	6	TO-5/31**
	60	2N3507J,/349 TX,TXV	2N3868J,/350A TX,TXV	30/150	2	0.4*		1	60	6	TO-5/31**
4	60		2N3740J,/441A TX,TXV	30/100	0.25	1.3 typ	0.27 typ	0.25	4	25	TO-66/80
		2N3766J,/518 TX, TXV***		40/160	0.5	0.9 typ	0.09 typ	0.5	10	20	TO-66/80
	80		2N3741J,/441A TX,TXV	30/100	0.25	1.3 typ	0.27 typ	0.25	4	25	TO-66/80
		2N3776J/518 TX, TXV***		40/160	0.5	0.9 typ	0.09 typ	0.5	10	20	TO-66/80
10	60	2N3715J,/408B TX,TXV	2N3791J,/379B TX,TXV	30 min	3	0.3 typ	0.4 typ	5	4	150	TO-3/11
	80	2N3716J,/408B TX,TXV	2N3792J,/379B TX,TXV	30 min	3	0.3 typ	0.4 typ	5	4	150	TO-3/11
12	80	2N6058J,/502 TX, TXV	2N6051J,/501 TX, TXV	750/18k	6	1.6 typ	1.5 typ	6	4##	150	TO-3/11
	100	2N6059J,/502 TX, TXV	2N6052J,/501 TX, TXV***	750/18k	6	1.6 typ	1.5 typ	6	4##	150	TO-3/11
15	300	2N6546J,/525 TX, TXV***		6/30	10	4	0.7	10	6-24	175	TO-3/11
	400	2N6547J,/525 TX, TXV***		6/30	10	4	0.7	10	6-24	175	TO-3/11
20	80	2N5303J,/456A TX	2N5745J,/433 TX,TXV	15/60	10	2	1	10	2	200	TO-3 Mod/12
		2N6283J/504 TX, TXV	2N6286J/505 TX, TXV	750/18k	10	2.5 typ	2.5 typ	10	4##	160	TO-3
	100	2N6284J,/504 TX, TXV***	2N6287J,/505 TX, TXV***	750/18k	10	2.5 typ	2.5 typ	10	4##	160	TO-3 Mod/12
25	100	2N6338J/509 TX, TXV***		30/120	10	1	0.25	10	40	200	TO-3 Mod/12
			2N6437J,/508 TX, TXV***	20/80	10	1	0.25	10	40	200	TO-3 Mod/12
	120		2N6438J,/508 TX, TXV***	20/80	10	1	0.25	10	40	200	TO-3 Mod/12
	150	2N6341J,/509 TX, TXV***		30/120	10	1	0.25	10	40	200	TO-3 Mod/12

MIL-S-19500 Detailed Spec. shown by Device Type

$|h_{fe}|$ @ 1 MHz

* t_{off}

** 2N3506 and 2N3507 are TO-39

*** Should be active by September 1978.

I_C Cont Amps	$V_{CEO(sus)}$ Volts	Device Type		h_{FE} @ I_C		Resistive Switching t_s μs	Resistive Switching t_f μs @ I_C		f_T MHz	P_D (Case) Watts	Case
Max	Min	NPN / #	PNP / #	Min/Max	Amp	Max	Max	Amp	Min	@ 25°C	JEDEC/MOT
30	60	2N5302J,/456A TX	2N4399J,/433 TX,TXV	15/60	15	2	1	10	2	200	TO-3 Mod/12
50	60	2N5685J,/464 TX,TXV	2N5683J,/466 TX,TXV	15/60	25	0.5 typ	0.3 typ	25	2	300	TO-3Mod/197
	80	2N5686J,/464 TX,TXV	2N5684J,/466 TX,TXV	15/60	25	0.5 typ	0.3 typ	25	2	300	TO-3 Mod/197
	100	2N6274J,/514 TX, TXV***	2N6378J,/515 TX, TXV***	30/120	20	0.8	0.25	20	30	250	TO-3 Mod/197
	120		2N6379J/515 TX, TXV***	30/120	20	0.8	0.25	20	30	250	TO-3 Mod/197
	150	2N6277J,/514 TX, TXV***		30/120	20	0.8	0.25	20	30	250	TO-3 Mod/197

Mil S 19500 Detailed Spec. shown by Device Type

*** Should be active by September 1978.

Secondary Motorola Power Transistors

(These are available from Motorola but may not be performance/cost effective for new designs)

Device Type	Polarity	$V_{CEO(sus)}$ Volts	I_C Amps	h_{FE}	I_C	f_T MHz	Case	Suggested Replacement for New Designs			
								Metal		Plastic	
			Max	Min/Max	@Amp	Min		Device	Case	Device	Case
2N3445	NPN	60	7.5	20/60	3	10	TO-3	2N3447	TO-3		
2N3446	NPN	80	7.5	20/60	3	10	TO-3	2N3448	TO-3		
2N3740A	PNP	60	4	30/100	0.25	4	TO-66	2N3740	TO-66	TIP30A	TO-220
2N3741A	PNP	80	4	30/100	0.25	4	TO-66	2N3741	TO-66	TIP30B	TO-220
2N4240	NPN	300	2	30/150	1	30	TO-66	2N3585	TO-66		
2N4901	PNP	40	5	20/80	1	4	TO-3	2N6312	TO-66	TIP32	TO-220
2N4902	PNP	60	5	20/80	1	4	TO-3	2N6313	TO-66	TIP32A	TO-220
2N4903	PNP	80	5	20/80	1	4	TO-3	2N6314	TO-66	TIP32B	TO-220
2N4904	PNP	40	5	25/100	2.5	4	TO-3	2N6317	TO-66	2N6109	TO-220
2N4905	PNP	60	5	25/100	2.5	4	TO-3	2N6317	TO-66	2N6107	TO-220
2N4906	PNP	80	5	25/100	2.5	4	TO-3	2N6318	TO-66	TIP42B	TO-220
2N4913	NPN	40	5	25/100	2.5	4	TO-3	2N6315	TO-66	2N6290	TO-220
2N4914	NPN	60	5	25/100	2.5	4	TO-3	2N6315	TO-66	2N6292	TO-220
2N4915	NPN	80	5	25/100	2.5	4	TO-3	2N6316	TO-66	TIP41B	TO-220
2N5067	NPN	40	5	20/80	1	4	TO-3	2N4231A	TO-66	TIP31	TO-220
2N5068	NPN	60	5	20/80	1	4	TO-3	2N4232A	TO-66	TIP31A	TO-220
2N5069	NPN	80	5	20/80	1	4	TO-3	2N4233A	TO-66	TIP31B	TO-220
2N5241	NPN	325	5	15/35	2.5	2.5	TO-3	2N3902	TO-3	MJE13004	TO-220
2N5336	NPN	80	5	30/120	2	30	TO-39	2N5337	TO-39		
2N5338	NPN	100	5	30/120	2	30	TO-39	2N5339	TO-39		
2N5346	NPN	80	7	30/120	2	30	TO-59	2N5347	TO-59		
2N5348	NPN	100	7	30/120	2	30	TO-59	2N5349	TO-59		
2N5427	NPN	80	7	30/120	2	30	TO-66	2N5428	TO-3		
2N5429	NPN	100	7	30/120	2	30	TO-66	2N5430	TO-3		
2N6186	PNP	80	10	30/120	2	30	TO-59	2N6187	TO-59		
2N6188	PNP	100	10	30/120	2	30	TO-59	2N6189	TO-59		
2N6190	PNP	80	5	30/120	2	30	TO-39	2N6191	TO-39		
2N6192	PNP	100	5	30/120	2	30	TO-39	2N6193	TO-39		
2N6423	PNP	300	2	30/150	0.75	15	TO-3	2N6422	TO-3		
BU108	NPN	1500*	5	2.25 min	4.5		TO-3	BU208	TO-3		
MJ205	NPN	1400*	2.5	2 min	2.5		TO-3	BU205	TO-3		
MJ804	NPN	1400*	5	2.2 min	3.5		TO-3	MJ12004	TO-3		
MJ1800	NPN	250	5	40/120	0.4		TO-3	MJ3029	TO-3		
MJ2252	NPN	300	0.5	25/200	0.05		TO-39	2N3739	TO-39	MJE340	TO-126
MJ3040	NPN	300	7	100 min	2.5		TO-3	MJ3041	TO-3		
MJ3771	NPN	40	30	15/60	15	2	TO-3	2N3771	TO-3		
MJ3772	NPN	60	20	15/60	10	2	TO-3	2N3772	TO-3		
MJ3773	NPN	140	16	15/60	8	1	TO-3	2N3773	TO-3		
MJ7160	NPN	350	8	25/125	3	30	TO-3	2N6544	TO-3	MJE13006	TO-220
MJ7161	NPN	400	8	25/125	3	30	TO-3	2N6545	TO-3	MJE13007	TO-220

*BV_{CEX}

(continued)

Device Type	Polarity	$V_{CEO(sus)}$ Volts	I_C Amps	h_{FE}	I_C	f_T MHz	Case	Suggested Replacement for New Designs			
								Metal		Plastic	
			Max	Min/Max	@Amp	Min		Device	Case	Device	Case
MJ9000	NPN	700*	10	3.75 min	6		TO-3	MJ3030	TO-3		
MJE31	NPN	40	3	25 min	1	3	TO-126R			TIP31	TO-220
MJE31A	NPN	60	3	25 min	1	3	TO-126R			TIP31A	TO-220
MJE31B	NPN	80	3	25 min	1	3	TO-126R			TIP31B	TO-220
MJE31C	NPN	100	3	25 min	1	3	TO-126R			TIP31C	TO-220
MJE32	PNP	40	3	25 min	1	3	TO-126R			TIP32	TO-220
MJE32A	PNP	60	3	25 min	1	3	TO-126R			TIP32A	TO-220
MJE32B	PNP	80	3	25 min	1	3	TO-126R			TIP32B	TO-220
MJE32C	PNP	100	3	25 min	1	3	TO-126R			TIP32C	TO-220
MJE220	NPN	60	4	40/200	0.2	50	TO-126			MJE181	TO-126
MJE221	NPN	60	4	40/150	0.2	50	TO-126			MJE181	TO-126
MJE222	NPN	60	4	25 min	0.2	50	TO-126			MJE181	TO-126
MJE223	NPN	80	4	40/200	0.2	50	TO-126			MJE182	TO-126
MJE224	NPN	80	4	40/150	0.2	50	TO-126			MJE182	TO-126
MJE225	NPN	80	4	25 min	0.2	50	TO-126			MJE182	TO-126
MJE230	PNP	60	4	40/200	0.2	50	TO-126			MJE171	TO-126
MJE231	PNP	60	4	40/150	0.2	50	TO-126			MJE171	TO-126
MJE232	PNP	60	4	25 min	0.2	50	TO-126			MJE171	TO-126
MJE233	PNP	80	4	40/200	0.2	50	TO-126			MJE172	TO-126
MJE234	PNP	80	4	40/150	0.2	50	TO-126			MJE172	TO-126
MJE235	PNP	80	4	25 min	0.2	50	TO-126			MJE172	TO-126
MJE240	NPN	80	4	40/200	0.2	40	TO-126			MJE182	TO-126
MJE241	NPN	80	4	40/120	0.2	40	TO-126			MJE182	TO-126
MJE242	NPN	80	4	25 min	0.2	40	TO-126			MJE182	TO-126
MJE244	NPN	100	4	25 min	0.2	40	TO-126			MJE243	TO-126
MJE250	PNP	80	4	40/200	0.2	40	TO-126			MJE172	TO-126
MJE251	PNP	80	4	40/120	0.2	40	TO-126			MJE172	TO-126
MJE252	PNP	80	1	25 min	0.2	40	TO-126			MJE172	TO-126
MJE254	PNP	100	4	25 min	0.2	40	TO-126			MJE253	TO-126
MJE371	PNP	40	4	40 min	1		TO-126			2N5193	TO-126
MJE521	NPN	40	4	40 min	1		TO-126			2N5190	TO-126
MJE701	NPN	60	4	750 min	2	1#	TO-126			2N6035	TO-126
MJE702	NPN	80	4	750 min	1.5	1#	TO-126			2N6036	TO-126
MJE703	NPN	80	4	750 min	2	1#	TO-126			2N6036	TO-126
MJE710	NPN	40	1.5	20 min	0.5		TO-126	2N4898	TO-66	2N4918	TO-126
MJE711	NPN	60	1.5	20 min	0.5		TO-126	2N4899	TO-66	2N4919	TO-126
MJE712	NPN	80	1.5	20 min	0.5		TO-126	2N4900	TO-66	2N4920	TO-126
MJE720	NPN	40	1.5	20 min	0.5		TO-126	2N3054	TO-66	2N4921	TO-126
MJE721	NPN	60	1.5	20 min	0.5		TO-126	2N3054	TO-66	2N4922	TO-126
MJE722	NPN	80	1.5	20 min	0.5		TO-126	2N4912	TO-66	2N4923	TO-126
MJE801	NPN	60	4	750 min	2	1#	TO-126			2N6038	TO-126
MJE802	NPN	80	4	750 min	1.5	1#	TO-126			2N6039	TO-126
MJE803	NPN	80	4	750 min	2	1#	TO-126			2N6039	TO-126
MJE1090	PNP	60	5	750 min	3	1#	TO-127	2N6298	TO-66	MJE6040	TO-127
MJE1091	PNP	60	5	750 min	4	1#	TO-127	2N6298	TO-66	MJE6040	TO-127
MJE1092	PNP	80	5	750 min	3	1#	TO-127	2N6299	TO-66	MJE6041	TO-127
MJE1093	PNP	80	5	750 min	4	1#	TO-127	2N6299	TO-66	MJE6041	TO-127
MJE1100	NPN	60	5	750 min	3	1#	TO-127	2N6300	TO-66	MJE6043	TO-127
MJE1101	NPN	60	5	750 min	4	1#	TO-127	2N6300	TO-66	MJE6043	TO-127
MJE1102	NPN	80	5	750 min	3	1#	TO-127	2N6301	TO-66	MJE6044	TO-127
MJE1103	NPN	80	5	750 min	4	1#	TO-127	2N6301	TO-66	MJE6044	TO-127
MJE2801	NPN	60	10	25/100	3		TO-127	2N3055	TO-3	MJE3055	TO-127
MJE2901	PNP	60	10	25/100	3		TO-127	MJ2955	TO-3	MJE2955	TO-127
SE9300	NPN	60	10	100 min	7.5	1#	TO-220			2N6043	TO-220
SE9301	NPN	80	10	100 min	7.5	1#	TO-220			2N6044	TO-220
SE9302	NPN	100	10	100 min	7.5	1#	TO-220			2N6045	TO-220
SE9400	PNP	60	10	100 min	7.5	1#	TO-220			2N6040	TO-220
SE9401	PNP	80	10	100 min	7.5	1#	TO-220			2N6041	TO-220
SE9402	PNP	100	10	100 min	7.5	1#	TO-220			2N6042	TO-220

#$|h_{fe}|$ @ 1 MHz

Power Transistor Cross Reference

3

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POWER TRANSISTOR CROSS REFERENCE

Devices are not shown in the following list if the Motorola number is identical. Refer to Chapter 1, the Alphanumeric Index, for the location of specifications.

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
2N1483		TIP41
2N1484		TIP41A
2N1485		TIP41
2N1486		TIP41A
2N1487	2N5877	
2N1488	2N5878	
2N1489	2N5877	
2N1490	2N5878	
2N2987	2N5681	
2N2988	2N5681	
2N2989	2N5681	
2N2990	2N5681	
2N3016	2N5337	
2N3021	2N3789	
2N3022	2N3789	
2N3023	2N3789	
2N3024	2N3791	
2N3025	2N3791	
2N3026	2N3791	
2N3055H	2N3055A	
2N3055SD	2N3055A	
2N3055UB	2N3055A	
2N3076		2N6249
2N3079		2N5838
2N3080		2N6542
2N3171	2N3789	
2N3172	2N3789	
2N3173	2N3790	
2N3174	2N6226	
2N3183	2N3789	
2N3184	2N3789	
2N3185	2N3790	
2N3186	2N6226	
2N3195	2N3789	
2N3196	2N3789	
2N3197	2N3790	
2N3202	2N3719	
2N3198	2N6226	
2N3203	2N3720	
2N3204	2N6303	
2N3232	2N5877	
2N3233	2N5632	
2N3234	2N5760	
2N3235	2N3055	
2N3236	2N5632	
2N3237	2N5302	
2N3238	2N5882	
2N3239	2N5882	
2N3240	2N5882	
2N3418	2N4877	
2N3419	2N5336	
2N3420	2N4877	
2N3421	2N5336	
2N3660	2N4234	
2N3661	2N4235	
2N3667	2N5881	
2N3788	MJ3030	
2N3863	2N3715	
2N3864	2N5632	
2N3865	2N5634	
2N3878	2N5427	
2N3879	2N5429	
2N3996		2N5347
2N3997		2N5347
2N4000	2N5336	
2N4001	2N5339	
2N4002	2N6274	
2N4003	2N6274	
2N4063		MJE3439
2N4064		MJE3440
2N4070	2N6306	
2N4071	2N6306	
2N4111	2N3715	
2N4113	2N3716	
2N4115		2N5347
2N4116		2N5347
2N4231	2N4231A	
2N4232	2N4232A	
2N4233	2N4233A	
2N4296	2N3738	
2N4297	2N3738	
2N4298	2N6235	
2N4299	2N6235	
2N4300	2N5336	
2N4301	2N5337	
2N4305	2N5337	
2N4307	2N5337	
2N4309	2N5339	
2N4311	2N5337	
2N4314	2N3868	
2N4347	2N5759	
2N4348	2N5630	
2N4387	2N4898	
2N4388	2N4898	
2N4907	2N3791	
2N4908	2N3791	
2N4909	2N3792	
2N4910	2N3054	
2N4911	2N3054	
2N4998	2N5347	
2N4999	2N6187	
2N5000	2N5347	
2N5001	2N6187	
2N5002	2N5347	
2N5003	2N6187	
2N5004	2N5347	
2N5005	2N6187	
2N5034		2N3055
2N5035		2N3055
2N5036		2N3055
2N5037		2N3055
2N5038	2N6338	
2N5039	2N6338	
2N5083	2N5347	
2N5084	2N5347	
2N5085	2N5347	
2N5147	2N6190	
2N5148	2N5336	
2N5149	2N6190	
2N5150	2N5336	
2N5151	2N6190	
2N5152	2N5336	
2N5153	2N6191	
2N5154	2N5337	
2N5157		2N6545
2N5202	2N5427	
2N5239	2N6306	
2N5240	2N6544	
2N5264	2N6249	
2N5284	2N5346	
2N5285	2N5347	
2N5286	2N6188	
2N5287	2N6189	
2N5293	2N6123	
2N5294	2N6123	
2N5295	2N6121	
2N5296	2N6121	
2N5297	2N6122	
2N5298	2N6122	
2N5326		2N5347
2N5333	2N6303	
2N5334	2N4877	
2N5335	2N5336	
2N5384		2N6187
2N5404	2N6190	
2N5405	2N6192	
2N5406	2N6191	
2N5407	2N6193	
2N5408		2N6187
2N5409		2N6188
2N5410		2N6187
2N5411		2N6189
2N5466	2N6545	
2N5467	2N6545	
2N5477		2N5347
2N5478		2N5347
2N5479		2N5349
2N5480		2N5349
2N5490	2N6290	
2N5491	2N6290	
2N5492	2N6292	
2N5493	2N6292	
2N5494	2N6290	
2N5495	2N6290	
2N5496	2N6292	
2N5497	2N6292	
2N5508	2N5428	
2N5539		2N6379
2N5559	2N5633	
2N5575	2N5685	
2N5578	2N5685	

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
2N5598	2N5428	
2N5600	2N5427	
2N5602	2N5428	
2N5604	2N5429	
2N5606	2N5428	
2N5610	2N5428	
2N5612	2N5430	
2N5614	2N3448	
2N5616	2N3448	
2N5618	2N3448	
2N5651	2N6235	
2N5660	2N6233	
2N5664	2N6233	
2N5665	2N6235	
2N5671	2N6338	
2N5672	2N6339	
2N5678		2N6381
2N5729	2N5336	
2N5730	2N5347	
2N5733		2N6274
2N5734	2N6338	
2N5737	2N5878	
2N5738	2N6229	
2N5739	2N5878	
2N5740	2N6229	
2N5741	2N5883	
2N5742	2N6029	
2N5743	2N5883	
2N5744	MJ4502	
2N5804	2N6306	
2N5805	2N6542	
2N5867	2N3789	
2N5868	2N3790	
2N5869	2N3713	
2N5870	2N3714	
2N5871	2N3789	
2N5872	2N3790	
2N5873	2N3713	
2N5874	2N3714	
2N5929	2N6338	
2N5930	2N6338	
2N5931	2N6341	
2N5932	2N6338	
2N5933	2N6338	
2N5935	2N6341	
2N5936	2N6338	
2N5937	2N6341	
2N5954	2N6318	
2N5955	2N6317	
2N5956	2N6317	
2N5970	2N5882	
2N5971	2N5882	
2N5972	MJ15003	
2N5980	2N6489	
2N5981	MJE2955	
2N5982		2N6491
2N5983	MJE3055	
2N5984	MJE3055	
2N5985		2N6488
2N6021	2N6126	
2N6022	2N6126	
2N6023	2N6124	
2N6024	2N6124	
2N6025	2N6125	
2N6026	2N6125	
2N6032	2N6275	
2N6033	2N6277	
2N6079	2N6235	
2N6098	2N6487	
2N6099	2N6487	
2N6100	2N6488	
2N6101	2N6488	
2N6102	2N6486	
2N6103	2N6486	
2N6106	2N6107	
2N6108	2N6109	
2N6110	2N6111	
2N6129	2N6290	
2N6130	2N6292	
2N6131	TIP31B	
2N6132	2N6109	
2N6133	2N6107	
2N6134	TIP32B	
2N6175		2N5656
2N6176		2N5656
2N6177		2N5657
2N6178		MJE182
2N6179		MJE181
2N6180		MJE172
2N6181		MJE171
2N6242		MJ13015
2N6243		MJ13334
2N6244		MJ13333
2N6245		MJ13334
2N6246	2N5879	
2N6247	2N5880	
2N6253	2N5877	
2N6253		2N3055H
2N6254	2N5878	
2N6258	2N5686	
2N6259	2N5631	
2N6260	2N4231A	
2N6261	2N4233A	
2N6262	2N5760	
2N6263	2N5050	
2N6264	2N5051	
2N6270	2N6338	
2N6271	2N6338	
2N6278		2N6274
2N6279		2N6275
2N6280		2N6276
2N6281		2N6277
2N6289	2N6288	
2N6291	2N6290	
2N6293	2N6292	
2N6302	2N5630	
2N6326	2N5302	
2N6327	2N5886	
2N6328		2N6338
2N6329	2N4399	
2N6330	2N5884	
2N6331		2N6436
2N6355	2N6057	
2N6356	2N6057	
2N6357	2N6058	
2N6358	2N6058	
2N6359	2N5885	
2N6360	2N5629	
2N6371	2N6569	
2N6372	2N6316	
2N6373	2N6315	
2N6374	2N6315	
2N6380	2N6377	
2N6381	2N6378	
2N6382	2N6379	
2N6406	MJE171	
2N6407	MJE172	
2N6408	MJE181	
2N6409	MJE182	
2N6410	MJE200	
2N6411	MJE210	
2N6412	MJE180	
2N6413	MJE181	
2N6414	MJE170	
2N6415	MJE171	
2N6416	MJE241	
2N6417	MJE243	
2N6418	MJE251	
2N6419	MJE253	
2N6465		TIP41C
2N6467	2N6420	
2N6468	2N6420	
2N6469	2N5879	
2N6470	2N5881	
2N6471	2N5881	
2N6472	2N5882	
2N6473	TIP31C	
2N6475	TIP32C	
2N6492	2N6055	
2N6493	2N6056	
2N6494	2N6056	
2N6496	2N6339	
2N6500	2N5429	
2N6510	2N6306	
2N6511	2N6306	
2N6512	2N6544	
2N6513	2N6545	
2N6514	2N6544	
2N6530	TIP101	
2N6531	TIP102	
2N6532	TIP103	
2N6534	2N6577	
2N6535	2N6578	
2N6536	2N6578	
2N6537	2N6578	
2N6573	2N6546	
2N6574	2N6546	
2N6575	2N6547	
2N6579		MJ13014
2N6580		MJ13015
2N6581		MJ13334
2N6582	2N6308	
2N6583	2N6545	
2N6584		MJ13334
2N6648	MJ2500	
2N6649	MJ2500	
2N6650	MJ2501	
2N6653		MJ13332
2N6654		MJ13332
2N6655		MJ13333
2N6671		2N6544
2N6672		2N6545
2N6673		2N6545
2N6674		MJ13014
2N6675		MJ13015
2N6676		MJ13332
2N6677		MJ13332
2N6678		MJ13333
2SC1306		MJE1909
2SC1678		MJE1909
2SC1816		MJE1909

DEVICES NOT SHOWN IF MOTOROLA NUMBER IS IDENTICAL, REFER TO CHAPTER 1

POWER TRANSISTOR CROSS REFERENCE (continued)

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
2SC1909	MJE1909	
2SC2078		MJE1909
2SC2092		MJE1909
2SC2166		MJE1909
BU105	BU205	
BU126		MJ3030
BUX80		2N6547
BUX81		MJ13335
BUX82		2N6545
BUX83		2N6545
BUX84	MJE13005	
BUX85		MJE13005
BUX86	MJE13003	
BUX87		MJE13003
D40D3	D40D2	
D42C1		MDS26
D42C2		MDS26
D42C3		MDS26
D42C4		MDS27
D42C5		MDS27
D42C6		MDS27
D42C7		MDS27
D42C8		MDS27
D42C9		MDS27
D43C1		MDS76
D43C2		MDS76
D43C3		MDS76
D43C4		MDS77
D43C5		MDS77
D43C6		MDS77
D43C7		MDS77
D43C8		MDS77
D43C9		MDS77
D44C1		MJE180
D44C2		MJE180
D44C3		MJE180
D44C4		MJE181
D44C5		MJE181
D44C6		MJE181
D44C7		MJE181
D44C8		MJE181
D44C9		MJE181
D44C10		MJE182
D44C11		MJE182
D44C12		MJE182
D44E1		2N6386
D44E2		2N6387
D44E3		2N6388
D44H1	D44H10	
D44H2	D44H11	
D44H4	D44H10	
D44H5	D44H11	
D44H7	D44H10	
D44H8	D44H11	
D44R1		2N3584
D44R2		2N3584
D44R3		2N3585
D44R4		2N3585
D44R5		2N3584
D44R6		2N3585
D45C1		MJE170
D45C2		MJE170
D45C3		MJE170
D45C4		MJE171
D45C5		MJE171
D45C6		MJE171
D45C7		MJE171
D45C8		MJE171
D45C9		MJE171
D45C10		MJE172
D45C11		MJE172
D45C12		MJE172
D45E1		TIP125
D45E2		TIP125
D45E3		TIP126
D45H1	D45H10	
D45H2	D45H11	
D45H4	D45H10	
D45H5	D45H11	
D45H7	D45H10	
D45H8	D45H11	
D45H9	D45H11	
D45H12	D45H11	
D56W1	BU208	
D56W2	BU208	
D56W3	BU207	
D56W4	BU207	
DTS310	2N6306	
DTS311	2N6306	
DTS401	2N3902	
DTS402	2N3902	
DTS403	2N6308	
DTS409	2N6308	
DTS410	MJ410	
DTS411	MJ411	
DTS413	MJ413	
DTS423	MJ423	
DTS424	2N6308	
DTS425	2N6545	
DTS430	2N6307	
DTS431	MJ431	
DTS515	2N6306	
DTS516	2N6306	
DTS517	2N6306	
DTS518	2N6307	
DTS519	2N6308	
DTS660	2N6233	
DTS663	2N6235	
DTS665	2N6235	
DTS701	BU204	
DTS702	BU205	
DTS712	BU207	
DTS714	BU208	
DTS801	BU205	
DTS802	BU207	
DTS804	BU208	
DTS812	BU207	
DTS814	BU208	
DTS1010	2N6056	
DTS1020	MJ3001	
DTS4010	MJ3041	
DTS4025	MJ3041	
DTS4026	MJ10012	
DTS4039	MJ10000	
DTS4040	MJ10000	
DTS4041	MJ10000	
DTS4045	MJ10000	
DTS4059	MJ10000	
DTS4060	MJ10001	
DTS4061	MJ10000	
DTS4065	MJ10001	
DTS4066		MJ10000
DTS4067		MJ10000
DTS4074		MJ10004
DTS4075		MJ10004
FT47	TIP47	
FT48	TIP48	
FT49	TIP49	
FT50	TIP50	
FT317	MJE15028	
FT317A	MJE15028	
FT317B	MJE15030	
FT359	MJ10012	
FT401	MJ411	
FT402	MJ413	
FT410	MJ410	
FT411	MJ411	
FT413	MJ413	
FT417	MJE15029	
FT417A	MJE15029	
FT417B	MJE15031	
FT423	MJ423	
FT423		MJ423
FT430	2N6307	
FT431	MJ431	
FT2955	MJE2955T	
FT3055	MJE3055T	
GE5060	MJ10000	
GE5061	MJ10000	
GE5062	MJ10001	
GE6060	MJ10004	
GE6061	MJ10004	
GE6062	MJ10005	
IR401	2N3902	
IR402	2N3902	
IR403	2N6308	
IR409	2N6308	
IR410	MJ410	
IR411	MJ411	
IR413	MJ413	
IR423	MJ423	
IR424	2N6308	
IR425	2N6545	
IR430	2N6307	
IR431	MJ431	
IR515	2N6250	
IR516	2N6250	
IR517	2N6251	
IR518	2N6546	
IR519	2N6547	
IR640	MJ3000	
IR641	MJ3001	
IR642	2N6578	
IR645	MJ2500	
IR646	MJ2501	
IR647	2N6052	
IR660	MJ410	
IR663	MJ423	
IR665	2N5157	
IR701	BU204	
IR801	BU205	
IR802	MJ802	
IR900	MJ900	
IR901	MJ901	
IR1000	MJ1000	
IR1001	MJ1001	
IR1010	2N6056	
IR1020	MJ3001	
IR2500	MJ2500	
IR2501	MJ2501	
IR3000	MJ3000	

DEVICES NOT SHOWN IF MOTOROLA NUMBER IS IDENTICAL,
REFER TO CHAPTER 1

POWER TRANSISTOR CROSS REFERENCE (continued)

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
IR3001	MJ3001	
IR3771	MJ3771	
IR3772	MJ3772	
IR3773	MJ3773	
IR4039	MJ10000	
IR4040	MJ10000	
IR4041	MJ10000	
IR4045	MJ10000	
IR4050	MJ10000	
IR4055	MJ10000	
IR4059	MJ10000	
IR4060	MJ10001	
IR4061	MJ10000	
IR4065	MJ10001	
IR4502	MJ4502	
IR5000	MJ10000	
IR5001	MJ10000	
IR5002	MJ10001	
IR5060	MJ10000	
IR5061	MJ10000	
IR5062	MJ10001	
IR5252	MJ10003	
IR5261	MJ10002	
IR6000	MJ10004	
IR6001	MJ10004	
IR6002	MJ10005	
IR6060	MJ10004	
IR6061	MJ10004	
IR6062	MJ10005	
IR6251	MJ10006	
IR6252	MJ10007	
IR6302	2N5630	
KDT410	MJ410	
KDT411	MJ411	
KDT413	MJ413	
KDT423	MJ423	
KDT430	2N6307	
KDT431	MJ431	
KDT515	2N6306	
KDT516	2N6306	
KDT517	2N6306	
KDT518	2N6307	
KDT519	2N6308	
KP3946	2N6274	
KP3948	2N6274	
MJ105	MJ205	
MJ400	2N3739	
MJ420	MM420	
MJ421	MM421	
MJ424	2N6308	
MJ425	2N6545	
MJ430		2N4234
MJ440		2N4237
MJ450	2N4398	
MJ480	2N3713	
MJ481	2N3713	
MJ490	2N3789	
MJ491	2N3789	
MJ701	MJ12002	
MJ702	MJ12002	
MJ704	MJ12002	
MJ721	MJ12002	
MJ723	MJ12002	
MJ920		(2)2N6298
MJ921		(2)2N6299
MJ1200		(2)2N6300
MJ1201		(2)2N6301
MJ2249	2N3766	
MJ2250	2N3767	
MJ2251	2N3738	
MJ2252	2N3739	
MJ2253	2N3740	
MJ2254	2N3741	
MJ2267	2N6594	
MJ2268	MJ2955	
MJ2801	2N6569	
MJ2802	2N5881	
MJ2840	2N5877	
MJ2841	2N5878	
MJ2901	2N6594	
MJ2940	2N5875	
MJ2941	2N5876	
MJ3010	2N6542	
MJ3011	2N6542	
MJ3012	2N6542	
MJ3026	MJ3029	
MJ3027	MJ3029	
MJ3028	MJ3029	
MJ3055	2N3055	
MJ3101	2N3766	
MJ3201	2N3738	
MJ3202	2N3739	
MJ3260	2N5838	
MJ3430	2N6307	
MJ3480	BU208	
MJ3520	MJ3000	
MJ3521	MJ3001	
MJ3583	2N6420	
MJ3584	2N6421	
MJ3585	2N6422	
MJ3701	2N4898	
MJ3702	2N4898	
MJ3703	2N4899	
MJ3704	2N4900	
MJ3738	2N6424	
MJ3739	2N6425	
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MJ3761	MJ9000	
MJ3801	MJ3001	
MJ3802	MJ3001	
MJ4000	2N6055	
MJ4001	2N6056	
MJ4010	2N6053	
MJ4011	2N6054	
MJ4200		(2)2N6294
MJ4201		(2)2N6295
MJ4210		(2)2N6296
MJ4211		(2)2N6297
MJ4240	2N6423	
MJ4648	MJ4647	
MJ5038	2N5038	
MJ5039	2N5039	
MJ5415	MM5415	
MJ5416	MM5416	
MJ6257	2N6257	
MJ6302	2N5630	
MJ6701	2N6186	
MJ7000		2N6338
MJ7260		2N6546
MJ7261		2N6547
MJ8020	MJ12004	
MJ8101	2N6190	
MJ13010	2N6547	
MJE29		TIP29
MJE29A		TIP29A
MJE29B		TIP29B
MJE29C		TIP29C
MJE30		TIP30
MJE30A		TIP30A
MJE30B		TIP30B
MJE30C		TIP30C
MJE33	TIP41	
MJE33A	TIP41A	
MJE33B	TIP41B	
MJE33C	TIP41C	
MJE34	TIP42	
MJE34A	TIP42A	
MJE34B	TIP42B	
MJE34C	TIP42C	
MJE41	TIP41	
MJE41A	TIP41A	
MJE41B	TIP41B	
MJE41C	TIP41C	
MJE42	TIP42	
MJE42A	TIP42A	
MJE42B	TIP42B	
MJE42C	TIP42C	
MJE47	TIP47	
MJE48	TIP48	
MJE49	TIP49	
MJE51	MJE51T	
MJE52	MJE52T	
MJE53	MJE53T	
MJE101	2N5974	
MJE102	2N5975	
MJE103	2N5976	
MJE104	2N5976	
MJE105K	TIP42A	
MJE201	2N5977	
MJE202	2N5978	
MJE203	2N5978	
MJE204	2N5979	
MJE205K	TIP41A	
MJE340K	TIP48	
MJE341K	TIP47	
MJE344K	TIP47	
MJE345	MJE3439	
MJE370K	TIP32	
MJE371K	TIP32	
MJE482	2N5190	
MJE483	2N5191	
MJE484	2N5192	
MJE492	2N5193	
MJE493	2N5194	
MJE494	2N5195	
MJE520K	TIP31	
MJE521K	TIP31	
MJE2010	TIP42	
MJE2011	TIP42A	
MJE2020	TIP41	
MJE2021	TIP41A	
MJE2050	MJE200	
MJE2055	MJE3055	
MJE2090	TIP125	
MJE2091	TIP125	
MJE2092	TIP126	
MJE2093	TIP126	
MJE2100	TIP120	
MJE2101	TIP120	
MJE2102	TIP121	
MJE2103	TIP121	

DEVICES NOT SHOWN IF MOTOROLA NUMBER IS IDENTICAL, REFER TO CHAPTER 1.

POWER TRANSISTOR CROSS REFERENCE (continued)

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
MJE2150	MJE210	
MJE2160	TIP48	
MJE2360	MJE2360T	
MJE2361	MJE2361T	
MJE2370	TIP32	
MJE2371	TIP32A	
MJE2480	TIP31	
MJE2481	TIP31A	
MJE2482	TIP41	
MJE2483	TIP41A	
MJE2490	TIP32	
MJE2491	TIP32A	
MJE2520	TIP31	
MJE2801K	MJE2801T	
MJE2901K	MJE2901T	
MJE2955K	MJE2955T	
MJE3055K	MJE3055T	
MJE3370		MJE370
MJE3371		2N5193
MJE3520		MJE520
MJE3521		2N5190
MJE3738	TIP47	
MJE3739	TIP48	
MJE4918	TIP30	
MJE4919	TIP30A	
MJE4920	TIP30B	
MJE4921	TIP29	
MJE4922	TIP29A	
MJE4923	TIP29B	
MJE5190	2N6121	
MJE5191	2N6122	
MJE5192	2N6123	
MJE5193	2N6124	
MJE5194	2N6125	
MJE5195	2N6126	
MJE5655	TIP47	
MJE5656	TIP48	
MJE5657	TIP49	
MJE5960	2N6489	
MJE5974	TIP42	
MJE5975	TIP42A	
MJE5976	TIP42B	
MJE5977	TIP41	
MJE5978	TIP41A	
MJE5979	TIP41B	
MJE5981	2N6490	
MJE5982	2N6491	
MJE5983	2N6486	
MJE5984	2N6487	
MJE5985	2N6488	
MPC900		MC1563 AND 2N6050
MPC1000		MC1726 AND 2N6077
MPSU11	MPSU10	
MPSU12	MPSU45	
MPSU47	MPSU31	
NSD102	MDS23	
NSD103	MDS23	
NSD104	2N6552	
NSD105	2N6552	
NSD106	2N6553	
NSD123	2N6591	
NSD127	2N6591	
NSD128	2N6592	
NSD129	2N6593	
NSD130	2N6557	
NSD132	2N6557	
NSD133	2N6558	
NSD134	2N6558	
NSD135	2N6559	
NSD151	2N6549	
NSD152	2N6548	
NSD202	MDS73	
NSD203	MDS73	
NSD204	2N6555	
NSD205	2N6555	
NSD206	2N6556	
NSD457	2N6591	
NSD458	2N6593	
NSD459	2N6558	
NSP41	TIP41	
NSP41A	TIP41A	
NSP41B	TIP41B	
NSP41C	TIP41C	
NSP42	TIP42	
NSP42A	TIP42A	
NSP42B	TIP42B	
NSP42C	TIP42C	
NSP105	TIP42A	
NSP205	TIP41A	
NSP370	TIP32	
NSP371	TIP32	
NSP520	TIP31	
NSP521	TIP31	
NSP575	TIP29A	
NSP576	TIP30A	
NSP577	TIP29A	
NSP578	TIP30A	
NSP579	TIP29B	
NSP580	TIP30B	
NSP581	TIP29C	
NSP582	TIP30C	
NSP585	TIP29A	
NSP586	TIP30A	
NSP587	TIP29A	
NSP588	TIP30A	
NSP589	TIP29B	
NSP590	TIP30B	
NSP595	TIP31A	
NSP596	TIP32A	
NSP597	TIP31A	
NSP598	TIP32A	
NSP599	TIP31B	
NSP600	TIP32B	
NSP695	TIP120	
NSP695A	TIP100	
NSP696	TIP125	
NSP696A	TIP105	
NSP697	TIP120	
NSP697A	TIP100	
NSP698	TIP125	
NSP698A	TIP105	
NSP699	TIP121	
NSP699A	TIP101	
NSP700	TIP126	
NSP700A	TIP106	
NSP701	TIP122	
NSP702	TIP127	
NSP2010	TIP42	
NSP2011	TIP42A	
NSP2021	TIP41A	
NSP2090	TIP125	
NSP2091	TIP125	
NSP2092	TIP126	
NSP2093	TIP126	
NSP2100	TIP120	
NSP2101	TIP120	
NSP2102	TIP121	
NSP2103	TIP121	
NSP2370	TIP32	
NSP2480	TIP31	
NSP2481	TIP31A	
NSP2490	TIP32	
NSP2491	TIP32A	
NSP2520	TIP31	
NSP2955	MJE2955T	
NSP3054	TIP31A	
NSP3055	MJE3055T	
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NSP4919	TIP30A	
NSP4920	TIP30B	
NSP4921	TIP29	
NSP4922	TIP29A	
NSP4923	TIP29B	
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NSP5191	2N6122	
NSP5192	2N6123	
NSP5193	2N6124	
NSP5194	2N6125	
NSP5195	2N6126	
NSP5974	TIP42	
NSP5975	TIP42A	
NSP5976	TIP42B	
NSP5977	TIP41	
NSP5978	TIP41A	
NSP5979	TIP41B	
NSP5980	2N6489	
NSP5981	2N6490	
NSP5982	2N6491	
NSP5983	2N6486	
NSP5984	2N6487	
NSP5985	2N6488	
PM26K380		MJ13015
PM27K380		2N6543
PMD10K-40	2N6057	
PMD10K-60	2N6057	
PMD10K-80	2N6058	
PMD10K-100	2N6059	
PMD11K-40	2N6050	
PMD11K-60	2N6050	
PMD11K-80	2N6051	
PMD11K-100	2N6052	
PMD12K-40	MJ1000	
PMD12K-60	MJ1000	
PMD12K-80	MJ1001	
PMD12K-100	2N6059	
PMD13K-40	MJ900	
PMD13K-60	MJ900	
PMD13K-80	MJ901	
PMD13K-100	2N6052	
PMD16K-40	2N6282	
PMD16K-60	2N6282	
PMD16K-80	2N6283	
PMD16K-100	2N6284	
PMD17K-40	2N6285	
PMD17K-60	2N6285	
PMD17K-80	2N6286	
PMD17K-100	2N6287	
PMD20K-120	2N6578	
PMD25K-120	2N6578	

DEVICES NOT SHOWN IF MOTOROLA NUMBER IS IDENTICAL, REFER TO CHAPTER 1

POWER TRANSISTOR CROSS REFERENCE (continued)

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
PMD1600K	2N6282	
PMD1601K	2N6282	
PMD1602K	2N6283	
PMD1603K	2N6284	
PMD1700K	2N6285	
PMD1701K	2N6285	
PMD1702K	2N6286	
PMD1703K	2N6287	
RCA1B01	2N5878	
RCA1C03	TIP31C	
RCA1C04	TIP32C	
RCA1C05	2N6315	
RCA1C06	2N6317	
RCA1C07		2N6488
RCA1C08		2N6491
RCA1C09		2N6488
RCA1C10	TIP41	
RCA1C11	TIP42	
RCA1C14	2N6315	
RCA29	TIP29	
RCA29A	TIP29A	
RCA29B	TIP29B	
RCA29C	TIP29C	
RCA30	TIP30	
RCA30A	TIP30A	
RCA30B	TIP30B	
RCA30C	TIP30C	
RCA31	TIP31	
RCA31A	TIP31A	
RCA31B	TIP31B	
RCA31C	TIP31C	
RCA32	TIP32	
RCA32A	TIP32A	
RCA32B	TIP32B	
RCA32C	TIP32C	
RCA41	TIP41	
RCA41A	TIP41A	
RCA41B	TIP41B	
RCA41C	TIP41C	
RCA42	TIP42	
RCA42A	TIP42A	
RCA42B	TIP42B	
RCA42C	TIP42C	
RCA120	TIP120	
RCA121	TIP121	
RCA122	TIP122	
RCA125	TIP125	
RCA126	TIP126	
RCA410	MJ410	
RCA411	MJ411	
RCA413	MJ413	
RCA423	MJ423	
RCA431	MJ431	
RCA1000	MJ1000	
RCA1001	MJ1001	
RCA3054	TIP31A	
RCA3055	MJE3055	
RCA8203	TIP125	
RCA8203A	TIP126	
RCA8203B	TIP127	
RCA8350	2N6050	
RCA8350A	2N6050	
RCA8350B	2N6051	
RCA8766		MJ10002
RCA8766A		MJ10002
RCA8766B		MJ10003
RCA8766C		MJ10003
RCA8766D		MJ10003
RCA8766E		MJ10003
RCA8767		2N6546
RCA8767A		2N6547
RCA8767B		2N6547
RCA9113		2N6546
RCA9113A		2N6547
RCA9113B		2N6547
RCP111A	2N6557	
RCP111B	2N6557	
RCP111C	2N6558	
RCP111D	2N6559	
RCP113A	2N6557	
RCP113B	2N6557	
RCP113C	2N6558	
RCP113D	2N6559	
RCP115	2N6591	
RCP115B	2N6557	
RCP117	2N6591	
RCP117B	2N6557	
RCP700A	2N6554	
RCP700B	2N6554	
RCP700C	2N6555	
RCP700D	2N6556	
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RCP701B	2N6551	
RCP701C	2N6552	
RCP701D	2N6553	
RCP702A	2N6554	
RCP702B	2N6554	
RCP702C	2N6555	
RCP702D	2N6556	
RCP703A	2N6551	
RCP703B	2N6551	
RCP703C	2N6552	
RCP703D	2N6553	
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RCP704B	2N6554	
RCP705	2N6551	
RCP705B	2N6551	
RCP706	2N6554	
RCP706B	2N6554	
RCP707	2N6551	
RCP707B	2N6551	
RCS29	2N4231A	
RCS29A	2N4232A	
RCS29B	2N4233A	
RCS30	2N6312	
RCS30A	2N6313	
RCS30B	2N6314	
RCS30C	2N6420	
RCS31	2N4231A	
RCS31A	2N4232A	
RCS31B	2N4233A	
RCS32	2N6312	
RCS32A	2N6313	
RCS32B	2N6314	
RCS32C	2N6421	
RCS242		2N3055H
RCS258		2N3772
RCS258	2N5885	
RCS559		2N6211
RCS560		2N6211
RCS564		2N6249
RCS579		2N6306
RCS579	2N6306	
SDM6000	MJ10012	
SDM6001	MJ10012	
SDM6002	MJ10012	
SDM6003	MJ10012	
SDM20301	MJ4033	
SDM20302	MJ4033	
SDM20303	MJ4034	
SDM20304	MJ4035	
SDM20311	MJ4033	
SDM20312	MJ4033	
SDM20313	MJ4034	
SDM20314	MJ4035	
SDM20321	MJ4033	
SDM20322	MJ4033	
SDM20323	MJ4034	
SDM20324	MJ4035	
SDM21301	MJ4030	
SDM21302	MJ4030	
SDM21303	MJ4031	
SDM21304	MJ4032	
SDM21311	MJ4030	
SDM21312	MJ4030	
SDM21313	MJ4031	
SDM21314	MJ4032	
SDN1010	2N6056	
SDN1020	MJ3001	
SDN4040	MJ10000	
SDN4045	MJ10000	
SDN6000	MJ10000	
SDN6001	MJ10000	
SDN6002	MJ10001	
SDN6060	MJ10000	
SDN6061	MJ10000	
SDN6062	MJ10000	
SDN6251	MJ10002	
SDN6252	MJ10002	
SDN6253	MJ10003	
SDT7A01	2N5428	
SDT7A02	2N5428	
SDT7A03	2N5428	
SDT7A07	2N5427	
SDT7A08	2N5427	
SDT7A09	2N5427	
SDT401	2N6543	
SDT402	2N6543	
SDT410	MJ410	
SDT411	MJ411	
SDT413	MJ413	
SDT423	MJ423	
SDT424	2N6308	
SDT425	2N6545	
SDT430	2N6307	
SDT431	MJ431	
SDT520	2N6306	
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SDT525	2N6306	
SDT526	2N6306	
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SDT530	2N6306	
SDT531	2N6306	
SDT532	2N6306	
SDT535	2N6306	
SDT536	2N6307	
SDT537	2N6307	
SDT540	2N6307	
SDT541	2N6307	
SDT542	2N6307	

DEVICES NOT SHOWN IF MOTOROLA NUMBER IS IDENTICAL, REFER TO CHAPTER 1

POWER TRANSISTOR CROSS REFERENCE (continued)

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SDT545	2N6308	
SDT546	2N6308	
SDT547	2N6308	
SDT550	2N6308	
SDT551	2N6308	
SDT552	2N6308	
SDT1050	2N5838	
SDT1051	2N5840	
SDT1052	2N6543	
SDT1053	2N6543	
SDT1054	2N6543	
SDT1055	2N5838	
SDT1056	2N3902	
SDT1057		2N6545
SDT1058		2N6545
SDT1059		2N6545
SDT1060	2N5838	
SDT1061	2N3902	
SDT1062		2N6545
SDT1063		2N6545
SDT1064		2N6545
SDT1301	2N6235	
SDT1302	2N6235	
SDT1303	2N6235	
SDT1304	2N6235	
SDT3125	MJ6701	
SDT3126	MJ6701	
SDT3321	MJ8100	
SDT3322	MJ8100	
SDT3323	2N6190	
SDT3324	2N6192	
SDT3325	MJ8100	
SDT3326	MJ8100	
SDT3327	2N6190	
SDT3328	2N6192	
SDT3401		2N5347
SDT3402		2N5347
SDT3403		2N5347
SDT3404		2N5349
SDT3405		2N5347
SDT3406		2N5347
SDT3407		2N5347
SDT3408		2N5349
SDT3421	2N4877	
SDT3422	2N4877	
SDT3423	2N5336	
SDT3424	2N5338	
SDT3425	2N4877	
SDT3426	2N4877	
SDT3427	2N5336	
SDT3428	2N5338	
SDT3501	2N3719	
SDT3502	2N3720	
SDT3503	2N6303	
SDT3504	2N6192	
SDT3505	2N3867	
SDT3506	2N3868	
SDT3507	2N6303	
SDT3508	2N6193	
SDT3775	2N6867	
SDT3776	2N3868	
SDT3777	2N6303	
SDT3778	2N3867	
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SDT4454	2N5336	
SDT4455	2N5337	
SDT4456	2N5337	
SDT4483	2N4877	
SDT4901	2N3583	
SDT4902	2N6233	
SDT4903	2N6234	
SDT4904	2N3585	
SDT4905	2N3585	
SDT5101	TIP41A	
SDT5102	TIP41A	
SDT5103	TIP41A	
SDT5111	TIP42A	
SDT5112	TIP42A	
SDT5113	TIP42A	
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SDT6413		2N5347
SDT6414		2N5347
SDT6415		2N5347
SDT6416		2N5347
SDT6901	2N5050	
SDT6902	2N5051	
SDT6903	2N5052	
SDT6904	2N5052	
SDT7201	2N6306	
SDT7202	2N6306	
SDT7203	2N6306	
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SDT7206	2N6341	
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SDT7604	2N6339	
SDT7605	2N6341	
SDT7609	2N6338	
SDT7610	2N6339	
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SDT7612	2N6249	
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SDT7733	2N5882	
SDT7734	2N5629	
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SDT7736	2N5631	
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SDT9202	2N5878	
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SDT9207	2N5878	
SDT9208	2N5632	
SDT9209	2N5633	
SDT9210	2N6569	
SDT9301	2N5067	
SDT9302	2N5068	
SDT9303	2N5069	
SDT9304	2N5067	
SDT9305	2N5068	
SDT9306	2N5069	
SDT9307	2N3713	
SDT9308	2N3715	
SDT9309	2N3716	
SDT9701	2N5303	
SDT9702	2N5629	
SDT9703	2N5630	
SDT9704	2N5882	
SDT9705	2N5629	
SDT9706	2N5330	
SDT9707	2N3055	
SDT12301	MJ5039	
SDT12301	2N5039	
SDT12302	MJ7260	
SDT12302		2N5347
SDT12303	MJ7260	
SDT12303		2N5347
SDT12305		2N5347
SDT12306		2N5347
SDT12307		2N5347
SDT13301	2N6546	
SDT13302	2N6547	
SDT13303	2N6547	
SDT13304		MJ13334
SDT13305		MJ13335
SDTB01		2N5346
SDTB02		2N5346
SDTB03		2N5348
SDTB05		2N5346

DEVICES NOT SHOWN IF MOTOROLA NUMBER IS IDENTICAL, REFER TO CHAPTER 1

POWER TRANSISTOR CROSS REFERENCE (continued)

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
SDTB06		2N5346
SDTB07		2N5346
SE9303	MJ3000	
SE9304	MJ3001	
SE9305	2N6059	
SE9306	MJ4033	
SE9307	MJ4034	
SE9308	MJ4035	
SE9331	2N3739	
SE9403	MJ2500	
SE9404	MJ2501	
SE9405	2N6052	
SE9406	MJ4030	
SE9407	MJ4031	
SE9408	MJ4032	
SV7056	2N6558	
SVT200-10	2N6306	
SVT250-5	2N5838	
SVT250-10	2N6306	
SVT300-5	2N6542	
SVT300-10	2N6307	
SVT350-3		2N6545
SVT350-5	2N5840	
SVT400-3	2N5157	
SVT400-5	2N6543	
SVT450-3		2N6545
SVT450-5	2N6543	
SVT6000	MJ10004	
SVT6001	MJ10004	
SVT6002	MJ10005	
SVT6060	MJ10004	
SVT6061	MJ10004	
SVT6062	MJ10005	
SVT6251	MJ10006	
SVT6252	MJ10006	
SVT6253	MJ10007	
TIP33		TIP41
TIP33A		TIP41A
TIP33B		TIP41B
TIP33C		TIP41C
TIP34		TIP42
TIP34A		TIP42A
TIP34B		TIP42B
TIP34C		TIP42C
TIP35		2N5301
TIP35A		2N5885
TIP35B		2N5886
TIP35C		MJ802
TIP36		2N4398
TIP36A		2N5883
TIP36B		2N5884
TIP36C		MJ4502
TIP51		2N6306
TIP52		2N6307
TIP53		2N6308
TIP54		2N6545
TIP55A		2N6546
TIP56A		2N6307
TIP57A		2N6308
TIP58A		2N6544
TIP61		TIP29
TIP61A		TIP29A
TIP61B		TIP29B
TIP61C		TIP29C
TIP62		TIP30
TIP62A		TIP30A
TIP62B		TIP30B
TIP62C		TIP30C
TIP69		BU205
TIP70		BU205
TIP71		BU205
TIP72		BU205
TIP75		MJE13005
TIP140		2N6057
TIP141		2N6058
TIP142		2N6059
TIP145		2N6050
TIP146		2N6051
TIP147		2N6052
TIP150		MJE13006
TIP151		MJE13007
TIP152		MJE13007
TIP160		MJ10002
TIP161		MJ10002
TIP162		MJ10012
TIP303		2N6544
TIP304		2N6544
TIP305		2N6545
TIP306		2N6545
TIP309		BU208
TIP310		BU208
TIP501	2N4877	
TIP502	2N4877	
TIP503	2N5050	
TIP504	2N5051	
TIP515	2N6339	
TIP516	2N6341	
TIP530	2N6235	
TIP531		2N6546
TIP532		2N6547
TIP535	2N6544	
TIP536	2N6544	
TIP537	2N6545	
TIP538	2N6249	
TIP539	2N6546	
TIP540	2N6547	
TIP544	2N6226	
TIP545	2N6227	
TIP546	2N6228	
TIP550		BU205
TIP551		BU205
TIP552		BU207
TIP553		BU208
TIP554		2N6306
TIP555	2N6307	
TIP556	2N6545	
TIP558	2N6544	
TIP559	2N6544	
TIP560	2N6545	
TIP561	2N6545	
TIP562		2N6546
TIP563		2N6547
TIP620	2N6055	
TIP621	2N6056	
TIP622	2N6578	
TIP625	2N6053	
TIP626	2N6054	
TIP627	2N6052	
TIP640	MJ3000	
TIP641	MJ3001	
TIP642	2N6578	
TIP645	MJ2500	
TIP646	MJ2501	
TIP647	2N6052	
TIP660	MJ10002	
TIP661	MJ10002	
TIP662	MJ10012	
TIP2955		MJE2955
TIP3055		MJE3055
UMT1008	MJ13014	
UMT1009	MJ13015	
UMT1203	MJE13004	
UMT1204	MJE13005	
WT5100		MJ13015
WT5200		2N6547
40250	2N4231A	
40251	2N6569	
40310	2N4231A	
40312	2N4232A	
40313	2N4240	
40316	2N4231A	
40318	2N4240	
40322	2N4240	
40324	2N4231A	
40325	2N6569	
40328	2N4240	
40363	2N5877	
40364	2N4233A	
40513		2N5984
40514		2N5984
40542		2N5978
40543		2N5978
40613	TIP31	
40618	TIP31	
40621	TIP31	
40622	TIP31	
40624	TIP41A	
40627	TIP41A	
40629	TIP31	
40630	TIP31	
40631	TIP31A	
40632	TIP41A	
40636	2N5878	
40829	2N6316	
40830	2N6315	
40831	2N6315	
40850	2N4240	
40852	2N6543	
40853	2N6546	
40854	2N6546	
40871	TIP41C	
40872	TIP42C	
40873	TIP41B	
40874	TIP41B	
40875	TIP41C	
40876	TIP41A	
40885		2N5655
40886		2N5656
40887		2N5657
41500	TIP29	
41501	TIP30	
41504	TIP31	
41505		2N5655
41506	2N6543	
43104	2N5631	

DEVICES NOT SHOWN IF MOTOROLA NUMBER IS IDENTICAL, REFER TO CHAPTER 1.

Power Transistor Data Sheets

4

2N3054
2N3054A (SILICON)

MEDIUM-POWER NPN SILICON TRANSISTORS

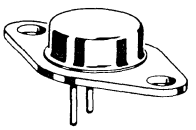
. . . designed for general purpose switching and amplifier applications.

- Excellent Safe Operating Area
- DC Current Gain Specified to 3.0 Amperes
- Complement to PNP Type 2N6049 or 2N4912

4 AMPERE

POWER TRANSISTORS NPN SILICON

55 VOLTS
25 WATTS – 2N3054
75 WATTS – 2N3054A



4

*MAXIMUM RATINGS

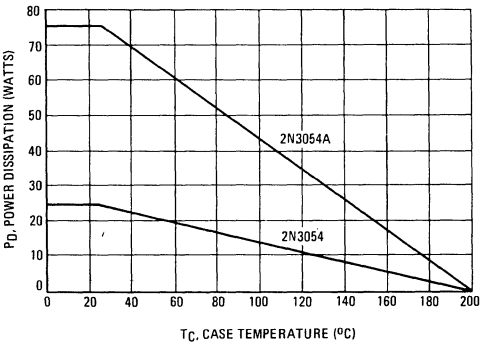
Rating	Symbol	2N3054A	2N3054	Unit
Collector-Emitter Voltage	V_{CEO}	55		Vdc
Collector-Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	60		Vdc
Collector-Base Voltage	V_{CB}	90		Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current – Continuous Peak	I_C	4.0 10**		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.43	25 0.143	Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	−65 to +200		°C

*Indicates JEDEC Registered Data
**Addition to JEDEC Registered Data

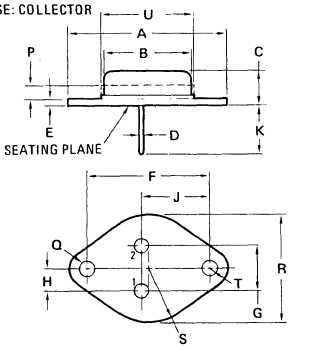
THERMAL CHARACTERISTICS

Characteristic	Symbol	2N3054A	2N3054	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.33	7.0	°C/W

FIGURE 1 – POWER-TEMPERATURE DERATING



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	55	—	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, R_{BE} = 100 Ω)	$V_{CER(sus)}$	60	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	—	500	μAdc
Collector Cutoff Current (V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	— —	1.0 6.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
***ON CHARACTERISTICS** (1)				
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	25 5.0	150 —	—
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc) (I_C =3.0 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$	— —	1.0 6.0	Vdc
Base-Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	1.7	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10 Vdc)	f_T	3.0	—	MHz
*Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	25	180	—
*Common-Emitter Cutoff Frequency (I_C = 100 mAdc, V_{CE} = 4.0 Vdc)	f_{hfe}	30	—	kHz

*Indicates JEDEC Registered Data

(1) Pulse test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%

FIGURE 2 – SWITCHING TIME EQUIVALENT TEST CIRCUIT

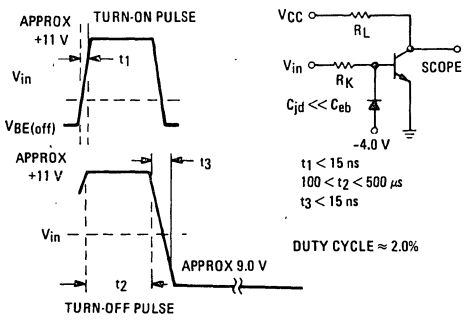


FIGURE 3 – TURN-ON TIME

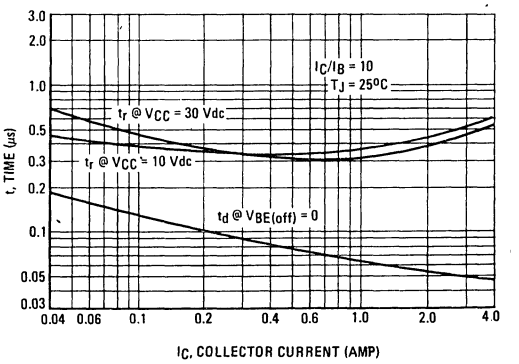


FIGURE 4 – THERMAL RESPONSE

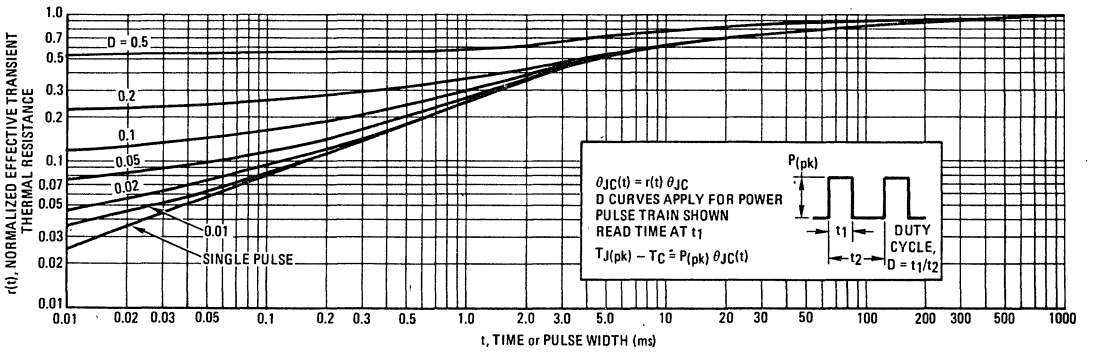
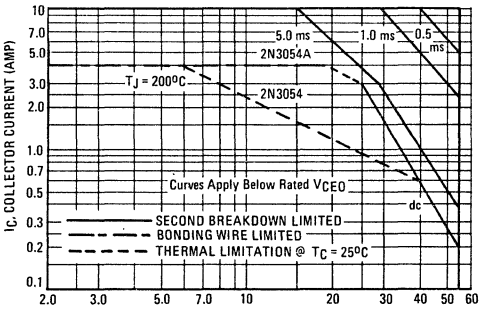


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

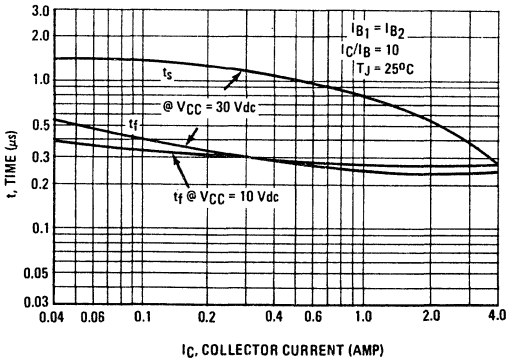


FIGURE 7 – CAPACITANCE

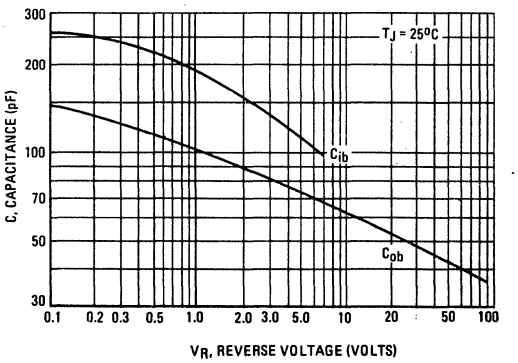


FIGURE 8 – DC CURRENT GAIN

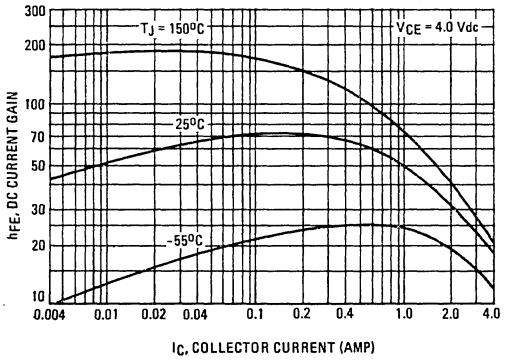
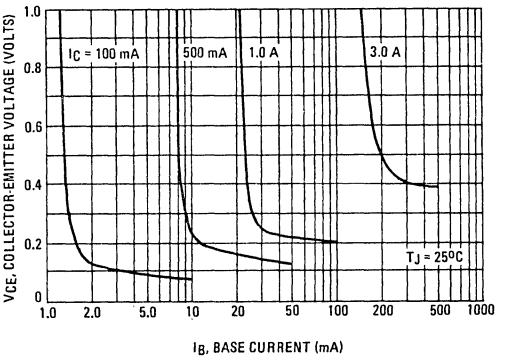


FIGURE 9 – COLLECTOR SATURATION REGION



4

FIGURE 10 – TEMPERATURE COEFFICIENTS

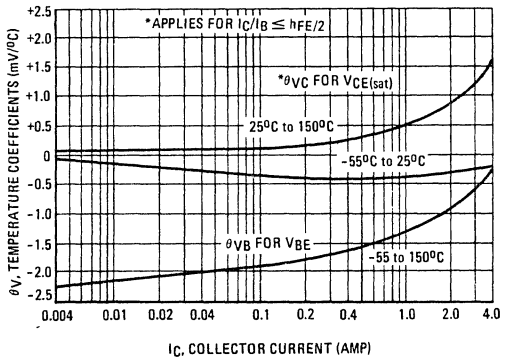


FIGURE 11 – "ON" VOLTAGES

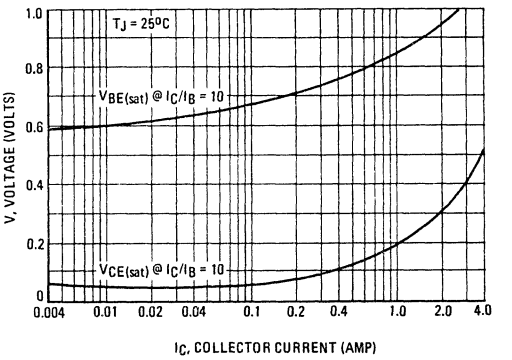


FIGURE 12 – COLLECTOR CUT-OFF REGION

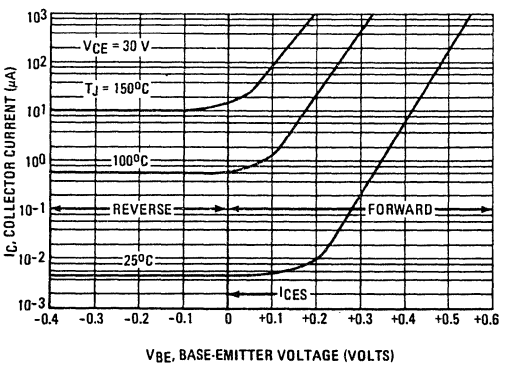
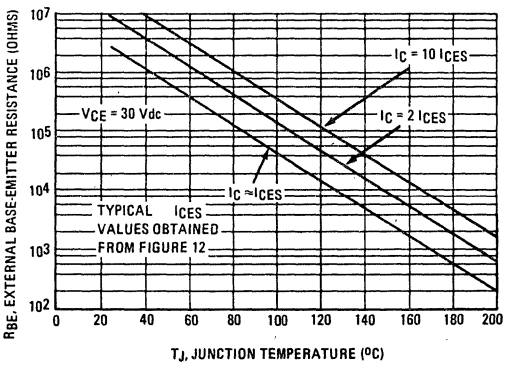


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



NPN 2N3055 PNP MJ2955

COMPLEMENTARY SILICON POWER TRANSISTORS

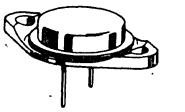
. . . designed for general-purpose switching and amplifier applications.

- DC Current Gain – h_{FE} = 20-70 @ I_C = 4 Adc
- Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 1.1 Vdc (Max) @ I_C = 4 Adc
- Excellent Safe Operating Area

15 AMPERE
POWER TRANSISTORS

COMPLEMENTARY SILICON

60 VOLTS
115 WATTS



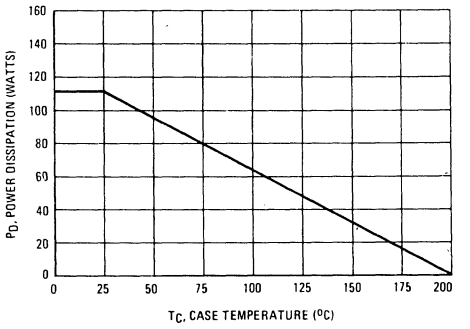
MAXIMUM RATINGS

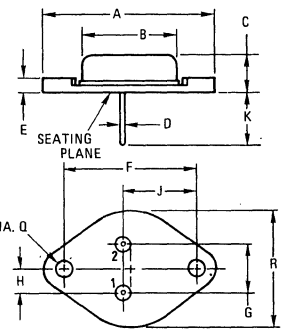
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Emitter Voltage	V_{CER}	70	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	7	Vdc
Collector Current – Continuous	I_C	15	Adc
Base Current	I_B	7	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.657	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	°C/W

FIGURE 1 – POWER DERATING





NOTE:
1. DIM "Q" IS DIA.

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

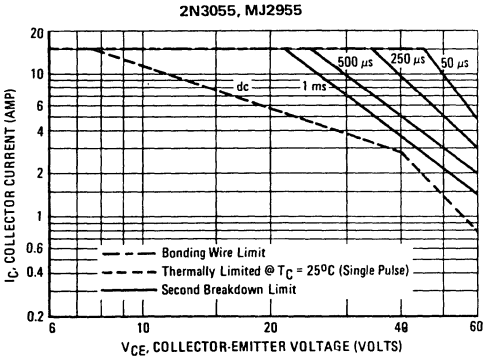
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, R_{BE} = 100 Ohms)	$V_{CER(sus)}$	70	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	0.7	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	1.0 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
***ON CHARACTERISTICS (1)**				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 5.0	70 –	–
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	–	1.1 3.0	Vdc
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.5	Vdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1.0 s; Nonrepetitive)	$I_{s/b}$	2.87	–	Adc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.5	–	MHz
*Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	15	120	–
*Small-Signal Current Gain Cutoff Frequency (V_{CE} = 4.0 Vdc, I_C = 1.0 Adc, f = 1.0 kHz)	f_{hfe}	10	–	kHz

* Indicates Within JEDEC Registration. (2N3055)

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

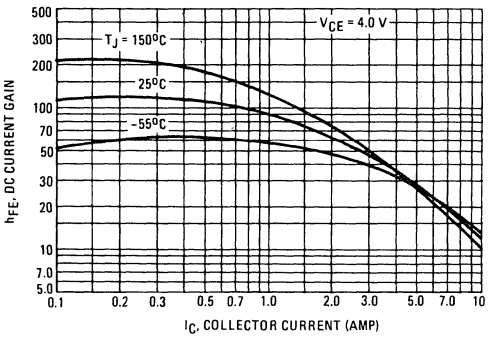
The data of Figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

4

NPN
2N3055

PNP
MJ2955

FIGURE 3 – DC CURRENT GAIN



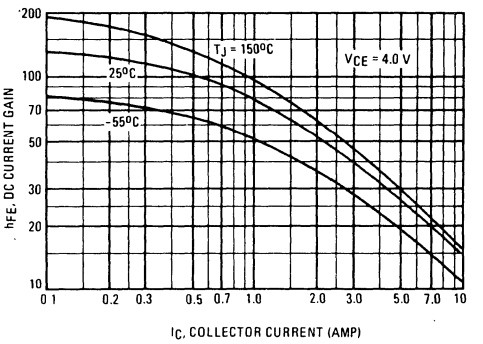
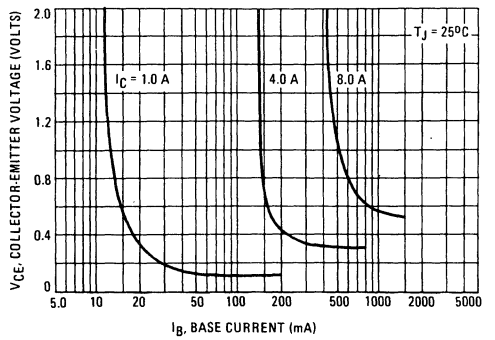


FIGURE 4 – COLLECTOR SATURATION REGION



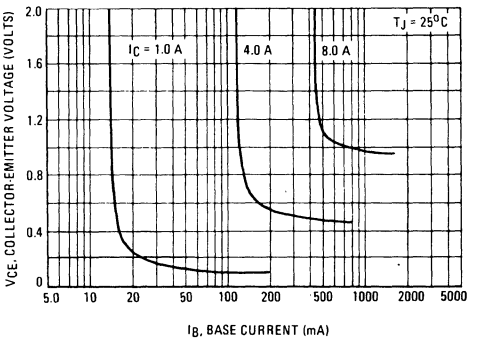
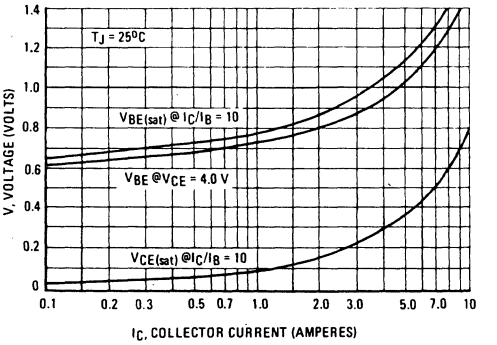


FIGURE 5 – "ON" VOLTAGES



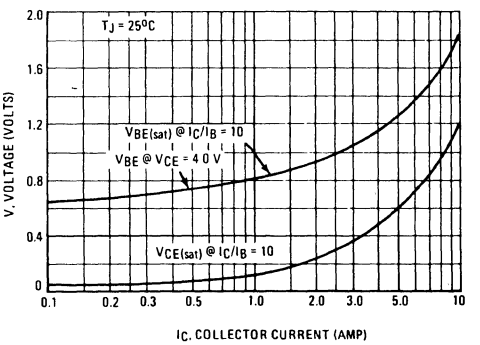
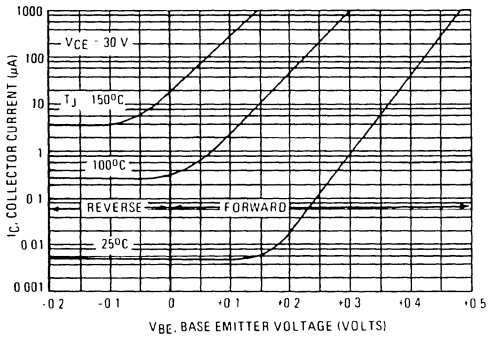


FIGURE 6 – COLLECTOR CUTOFF REGION

NPN – 2N3055



PNP – MJ2955

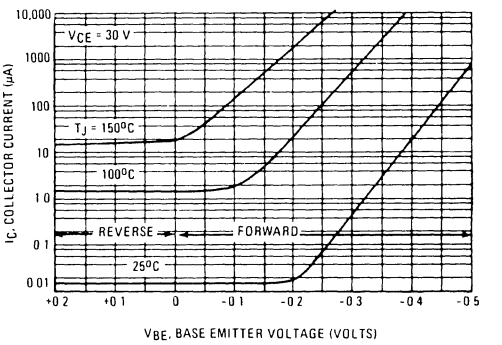
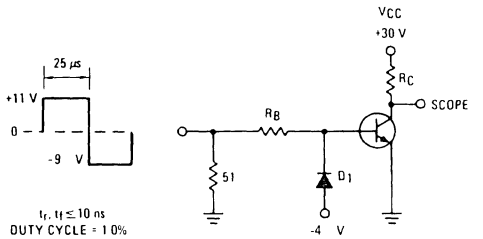


FIGURE 7 – SWITCHING TIMES TEST CIRCUIT



tr, tf ≤ 10 ns
DUTY CYCLE = 1 0%

RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg
M8D5300 USED ABOVE IB = 100 mA
MSD6100 USED BELOW IB = 100 mA

For PNP Test Circuit,
Reverse All Polarities.

FIGURE 8 – TURN-ON TIME

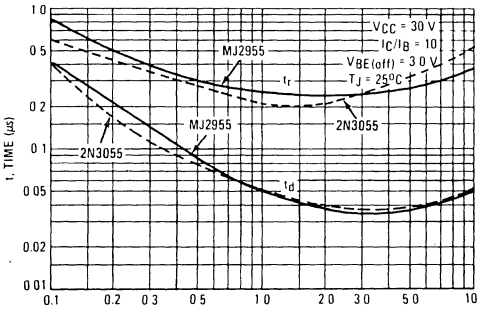


FIGURE 9 – TURN-OFF TIME

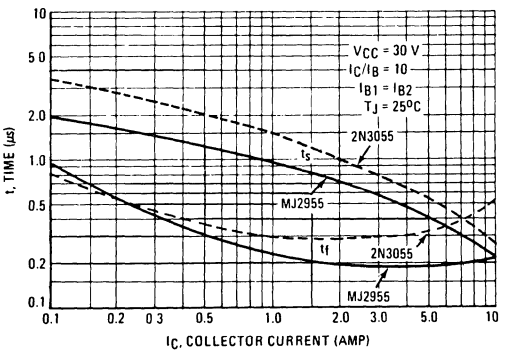
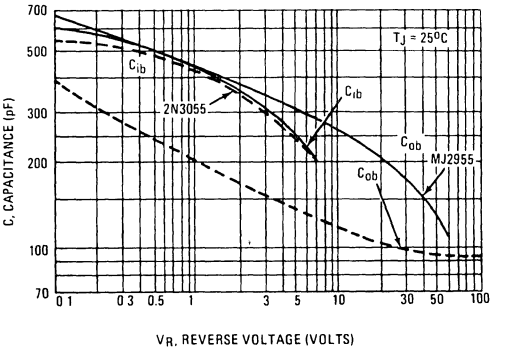


FIGURE 10 – CAPACITANCE



4

NPN
2N3055A · MJ15015
PNP
MJ2955A · MJ15016

COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

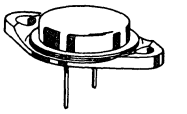
. . . PowerBase complementary transistors designed for high power audio, stepping motor and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc-to-dc converters, inverters, or for inductive loads requiring higher safe operating area than the 2N3055 and MJ2955.

- Current-Gain – Bandwidth-Product @ I_C = 1 Adc
  f_T = 0.8 MHz (Min) – NPN
  = 2.2 MHz (Min) – PNP
- Safe Operating Area – Rated to 60 V and 120 V, Respectively

15 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

60, 120 VOLTS
115, 180 WATTS



***MAXIMUM RATINGS**

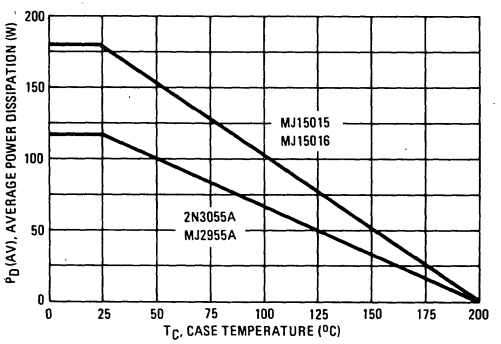
Rating	Symbol	2N3055A MJ2955A	MJ15015 MJ15016	Unit
Collector-Emitter Voltage	V_{CEO}	60	120	Vdc
Collector-Base Voltage	V_{CBO}	100	200	Vdc
Collector-Emitter Voltage Base Reversed Biased	V_{CEV}	100	200	Vdc
Emitter-Base Voltage	V_{EBO}	7.0		Vdc
Collector Current – Continuous	I_C	15		Adc
Base Current	I_B	7.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.65	180 1.03	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

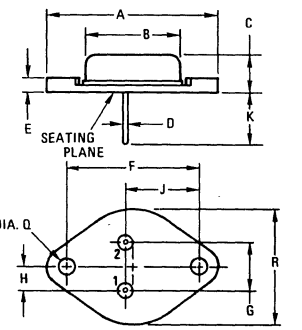
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.52	0.98	°C/W

*Indicates JEDEC Registered Data (2N3055A)

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)					
*Collector-Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0)	2N3055A, MJ2955A MJ15015, MJ15016	$V_{CEO(sus)}$	60 120	– –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, $V_{BE(off)}$ = 0 Vdc) (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 0 Vdc)	 2N3055A, MJ2955A MJ15015, MJ15016	I_{CEO}	 – –	 0.7 0.1	mAdc
*Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	2N3055A, MJ2955A MJ15015, MJ15016	I_{CEV}	– –	5.0 1.0	mAdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3055A, MJ2955A MJ15015, MJ15016	I_{CEV}	– –	30 6.0	mAdc
*Emitter Cutoff Current (V_{EB} = 7 Vdc, I_C = 0)	2N3055A, MJ2955A MJ15015, MJ15016	I_{EBO}	– –	5.0 0.2	mAdc
***SECOND BREAKDOWN**					
Second Breakdown Collector Current with Base Forward Biased (t = 0.5 s non-repetitive) (V_{CE} = 60 Vdc)	 2N3055A, MJ2955A MJ15015, MJ15016	$I_{S/b}$	 1.95 3.0	 – –	Adc
***ON CHARACTERISTICS (1)**					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	 10 20 5.0	 70 70 –	–
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 3.3 Adc) (I_C = 15 Adc, I_B = 7.0 Adc)		$V_{CE(sat)}$	 – – –	 1.1 3.0 5.0	Vdc
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	0.7	1.8	Vdc
***DYNAMIC CHARACTERISTICS**					
Current-Gain–Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)	2N3055A, MJ15015 MJ2955A, MJ15016	f_T	0.8 2.2	6.0 18	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	60	600	pF

***SWITCHING CHARACTERISTICS (2N3055A only)**

RESISTIVE LOAD					
Delay Time	(V_{CC} = 30 Vdc, I_C = 4.0 Adc, I_{B1} = I_{B2} = 0.4 Adc, t_p = 25 μs Duty Cycle ≤ 2%)	t_d	–	0.5	μs
Rise Time		t_r	–	4.0	μs
Storage Time		t_s	–	3.0	μs
Fall Time		t_f	–	6.0	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.
*Indicates JEDEC Registered Data (2N3055A)

4

FIGURE 2 – DC CURRENT GAIN

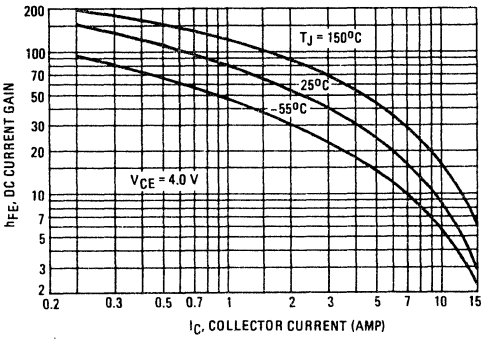


FIGURE 3 – COLLECTOR SATURATION REGION

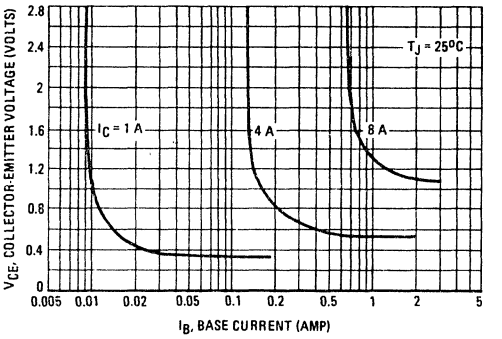


FIGURE 4 – "ON" VOLTAGES

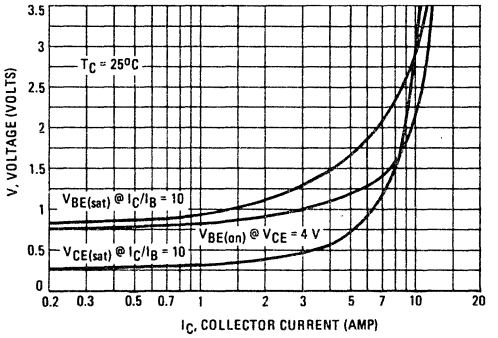


FIGURE 5 – CURRENT-GAIN–BANDWIDTH PRODUCT

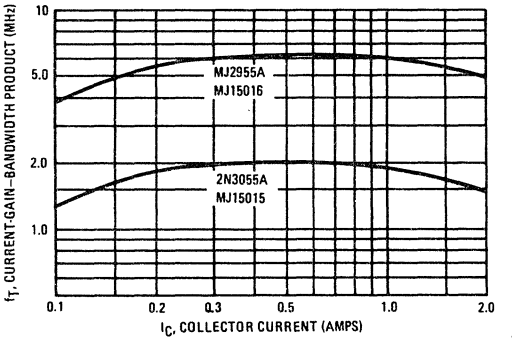


FIGURE 6 – SWITCHING TIMES TEST CIRCUIT
(Circuit shown is for NPN)

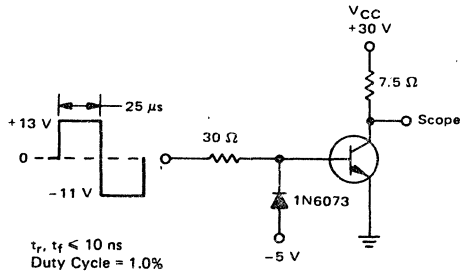


FIGURE 7 – TURN-ON TIME

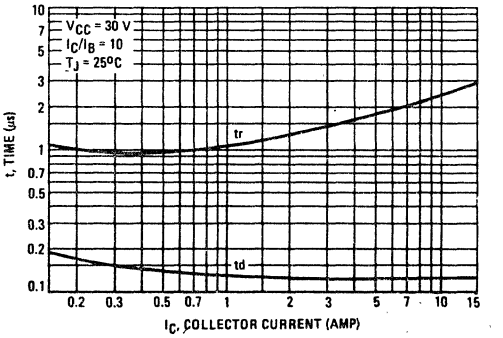


FIGURE 8 – TURN-OFF TIMES

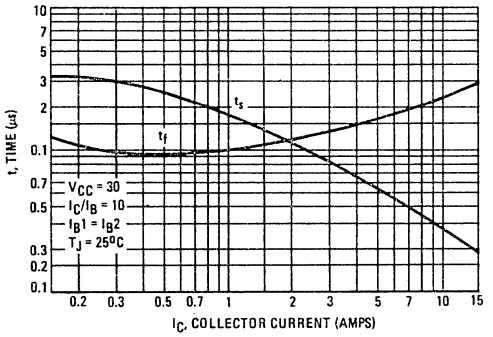
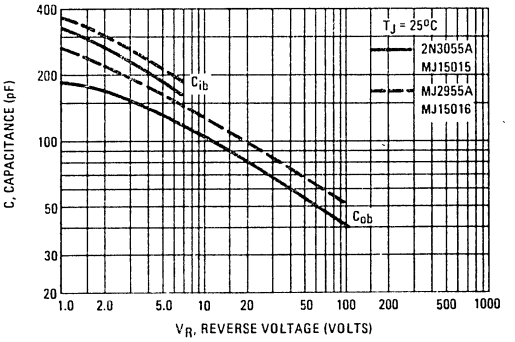


FIGURE 9 – CAPACITANCES

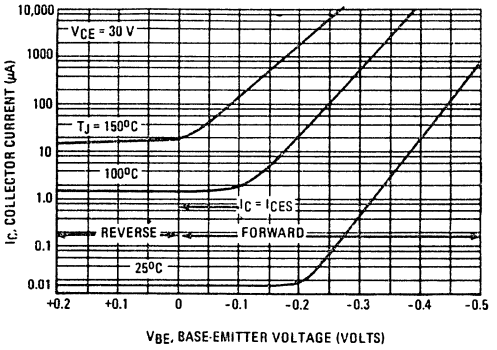


4

COLLECTOR CUT-OFF REGION

NPN

FIGURE 10 – 2N3055A, MJ15015



PNP

FIGURE 11 – MJ2955A, MJ15016

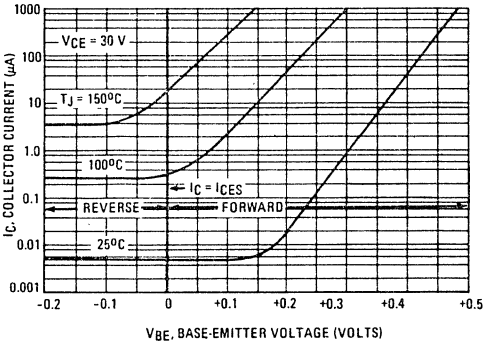


FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA
2N3055A, MJ2955A

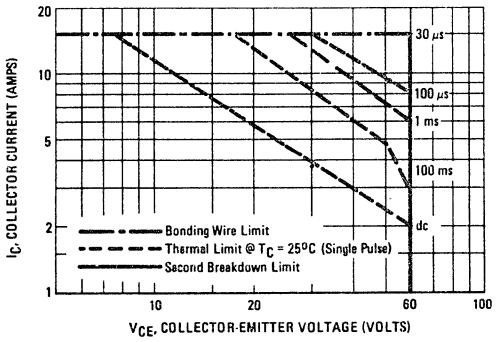
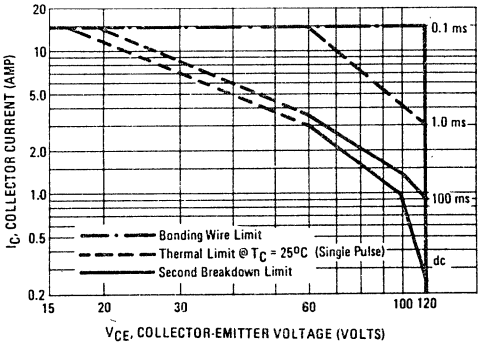


FIGURE 13 – FORWARD BIAS SAFE OPERATING AREA
MJ15015, MJ15016



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe Operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 12 and 13 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

2N3441

NPN SILICON POWER TRANSISTOR

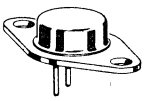
. . . 2N3441 transistor is designed for use in general-purpose switching and linear amplifier applications requiring high breakdown voltages. It is characterized for use as:

- Driver for High Power Outputs
- Series and Shunt Regulators
- Audio and Servo Amplifiers
- Solenoid and Relay Drivers
- Power Switching Circuits

3 AMPERES

NPN SILICON POWER TRANSISTOR

140 VOLTS
25 WATTS

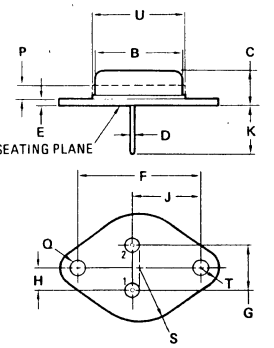


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	140	Vdc
Collector-Base Voltage	V_{CBO}	160	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector Current — Continuous	I_C	3	Adc
Base Current — Continuous	I_B	2	Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	25 0.142	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	7	$^oC/W$



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

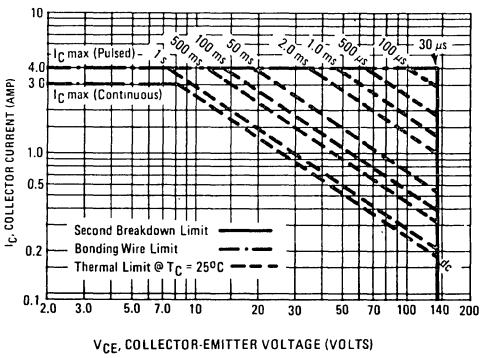
All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	–	Vdc
Collector Cutoff Current (V_{CE} = 140 Adc, I_B = 0)	I_{CEO}	–	100	mA
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 V) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 V @ 150°C)	I_{CEX}	– –	5.0 6.0	mA
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mA
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 0.5 Adc, V_{CE} = 4.0 V) (I_C = 2.7 Adc, V_{CE} = 4.0 V)	h_{FE}	25 5.0	100 –	–
Collector-Emitter Saturation Voltage (1) (I_C = 2.7 Adc, I_B = 0.9 Adc)	$V_{CE(sat)}$	–	6.0	Vdc
Base-Emitter On Voltage (1) (I_C = 2.7 Adc, I_B = 4.0 Vdc)	$V_{BE(on)}$	–	6.0	Vdc
DYNAMIC CHARACTERISTICS				
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1 kHz)	h_{fe}	15	75	–
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f_{test} = 0.4 MHz)	$\|h_{fe}\|$	5.0	–	–

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power-handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

2N3442
2N4347

4

HIGH-POWER INDUSTRIAL TRANSISTORS

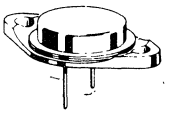
NPN silicon power transistors designed for applications in industrial and commercial equipment including high fidelity audio amplifiers, series and shunt regulators and power switches.

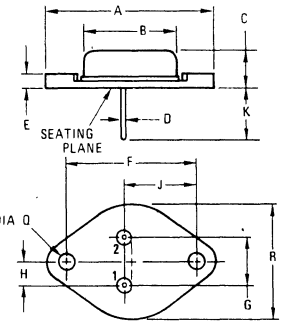
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 2.0 Adc – 2N4347
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 120 Vdc (Min) – 2N4347
  140 Vdc (Min) – 2N3442
- Excellent Second-Breakdown Capability

5.0 AND 10 AMPERE

POWER TRANSISTORS
NPN SILICON

120, 140 VOLTS
100, 117 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case
CASE 11-01
(TO-3)

*MAXIMUM RATINGS

Rating	Symbol	2N4347	2N3442	Unit
Collector-Emitter Voltage	V_{CEO}	120	140	Vdc
Collector-Base Voltage	V_{CB}	140	160	Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current – Continuous Peak	I_C	5.0 10	10 15**	Adc
Base Current – Continuous Peak	I_B	3.0 8.0	7.0 –	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.57	117 0.67	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	2N4347	2N3442	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	1.5	°C/W

*Indicates JEDEC Registered Data.
**This data guranteed in addition to JEDEC registered data.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

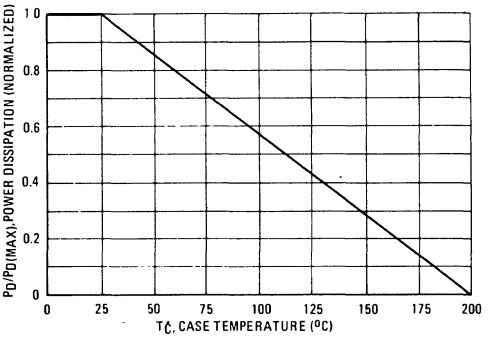
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N4347		120	–	
	2N3442		140	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 100 Vdc, I_B = 0	2N4327		–	200	
(V_{CE} = 140 Vdc, I_B = 0)	2N3422		–	200	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 125 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N4347		–	2.0	
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N3442		–	5.0	
(V_{CE} = 120 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N4347		–	10	
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3442		–	30	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 7.0 Vdc, I_C = 0)	2N4347, 2N3442		–	5.0	
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)	2N4347		15	60	
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)	2N4347		10	–	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	2N3442		20	70	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)	2N3442		7.5	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 200 mAdc)	2N4347		–	1.0	
(I_C = 5.0 Adc, I_B = 0.63 Adc)	2N4347		–	2.0	
(I_C = 10 Adc, I_B = 2.0 Adc)	2N3442		–	5.0	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 2.0 Adc; V_{CE} = 4.0 Vdc)	2N4347		–	2.0	
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)	2N4347		–	3.0	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)	2N3442		–	5.7	
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (2)		f_T			kHz
(I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f_{test} = 50 kHz)	2N4347		200	–	
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 40 kHz)	2N3442		80	–	
Small-Signal Current Gain		h_{fe}			–
(I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	2N4347		40	–	
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	2N3442		12	72	

*Indicates JEDEC Registered Data

NOTES: 1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

2. $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 1 – POWER DERATING



ACTIVE REGION SAFE OPERATING AREA INFORMATION

FIGURE 2 – 2N3442

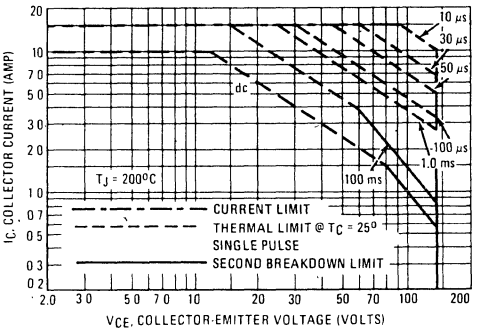
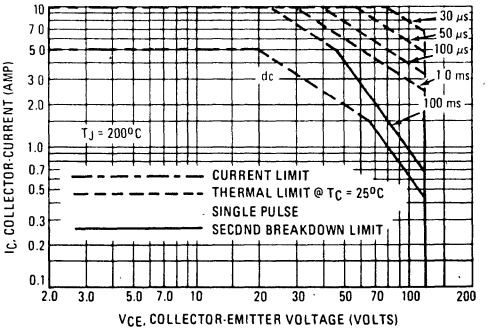


FIGURE 3 – 2N4347



There are two limitations on the power-handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 2 and 3 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 4 – DC CURRENT GAIN

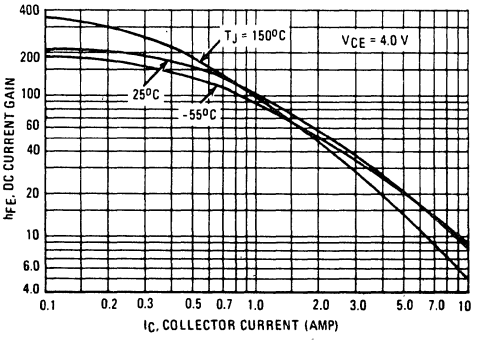


FIGURE 5 – COLLECTOR-SATURATION REGION

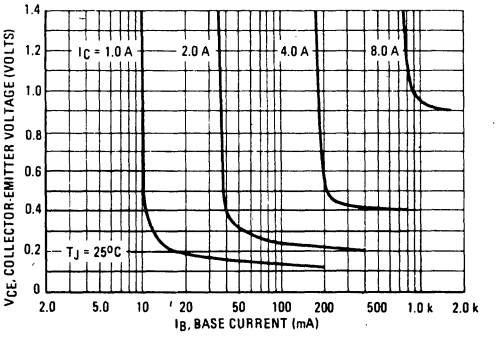


FIGURE 6 – "ON" VOLTAGE

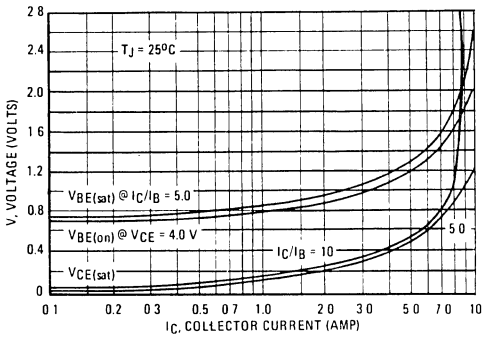


FIGURE 7 – COLLECTOR CUTOFF REGION

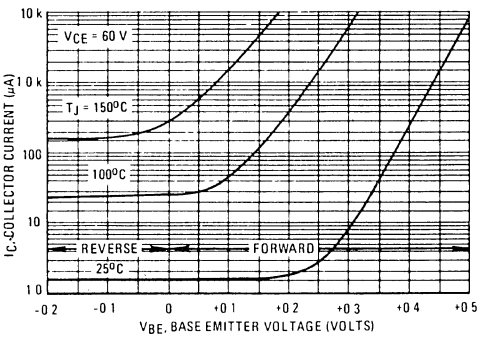
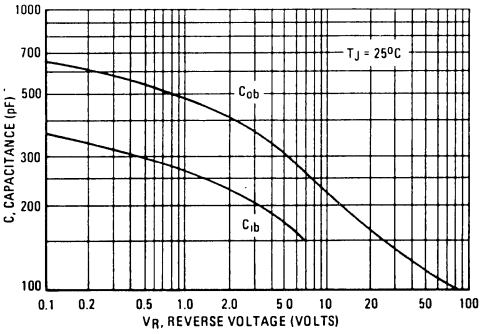


FIGURE 8 – CAPACITANCE



2N3445 thru 2N3448

HIGH-SPEED SILICON ANNULAR* NPN POWER TRANSISTORS

. . . for switching and amplifier applications

FEATURES

- Fast Switching: Total Switching Time = 1.2 μs (Typ) @ 5.0 A
- High Gain: H_{FE} = 40 to 120 @ 5.0 Amps (2N3447-48)
- Guaranteed DC Safe Area: 1.5 Amps (Min) @ V_{CE} = 40 Vdc
- Low $V_{CE(sat)}$: 1.0 Volt (Typ), 1.5 Volts (Max) @ 5.0 Amps
- Excellent Beta Linearity

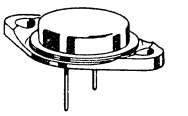
APPLICATIONS

- Specified safe area of this series allows reliable design for inverters, converters, hammer, and servo drivers.
- Fast response makes it ideal for series regulators; high switching speeds enhance its use in switching regulators.
- Wide bandwidth and flat beta hold-up result in exceptional amplifier characteristics.

7.5 AMPERE

POWER TRANSISTORS SILICON NPN

60-80 VOLTS
115 WATTS

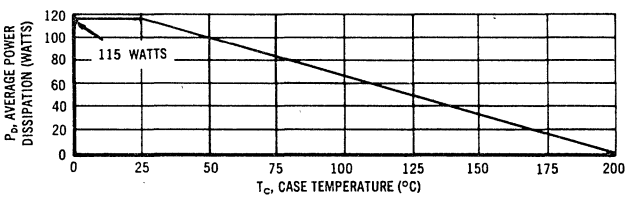


4

MAXIMUM RATING

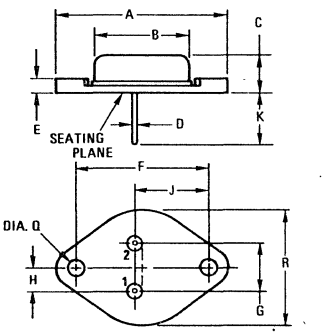
Rating	Symbol	2N3445 2N3447	2N3446 2N3448	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0	10	Vdc
Collector Current-Continuous	I_C	7.5		Adc
Base Current - Continuous	I_B	4.0		Adc
Total Device Dissipation	P_D	Figure 1, 2	Figure 1, 3	Watts
Operating Junction Temperature Range	T_J	−65 to +200		°C

FIGURE 1 – POWER DERATING CURVE



These transistors are also subject to safe area curves as indicated by Figures 2, 3. Both limits are applicable and must be observed.

*Annular Semiconductors Patented by Motorola Inc.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Emitter-Base Cutoff Current		I_{EBO}				mAdc
(V_{EB} = 6 Vdc)	2N3445, 2N3447		–	–	0.25	
(V_{EB} = 10 Vdc)	2N3446, 2N3448		–	–	0.25	
Collector-Emitter Cutoff Current		I_{CEX}				mAdc
(V_{CE} = 60 Vdc, V_{BE} = –1 Vdc)	2N3445, 2N3447		–	–	0.1	
(V_{CE} = 60 Vdc, V_{BE} = –1 Vdc, T_C = 150°C)	2N3445, 2N3447		–	–	1.0	
(V_{CE} = 80 Vdc, V_{BE} = –1 Vdc)	2N3446, 2N3448		–	–	0.1	
(V_{CE} = 80 Vdc, V_{BE} = –1 Vdc, T_C = 150°C)	2N3446, 2N3448		–	–	1.0	
Collector-Emitter Cutoff Current		I_{CEO}				mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N3445, 2N3447		–	–	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N3446, 2N3448		–	–	1.0	
Collector-Base Breakdown Voltage		BV_{CBO}				Vdc
(I_C = 1 mAdc, I_E = 0)	2N3445, 2N3447		80	–	–	
	2N3446, 2N3448		100	–	–	
Collector-Emitter Sustaining Voltage		$V_{CEO(sus)}$				Vdc
(I_C = 100 mAdc, I_B = 0)	2N3445, 2N3447		60	–	–	
	2N3446, 2N3448		80	–	–	
DC Current Gain		h_{FE}				–
(I_C = 0.5 Adc, V_{CE} = 5 Vdc)	2N3445, 2N3446		20	45	–	
	2N3447, 2N3448		40	85	–	
(I_C = 3 Adc, V_{CE} = 5 Vdc)	2N3445, 2N3446		20	40	60	
(I_C = 5 Adc, V_{CE} = 5 Vdc)	2N3447, 2N3448		40	75	120	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 3 Adc, I_B = 0.3 Adc)	2N3445, 2N3446		–	0.6	1.5	
(I_C = 5 Adc, I_B = 0.5 Adc)	2N3447, 2N3348		–	0.8	1.5	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 3 Adc, I_B = 0.3 Adc)	2N3445, 2N3446		–	1.0	1.5	
(I_C = 5 Adc, I_B = 0.5 Adc)	2N3447, 2N3338		–	1.0	1.5	
Base-Emitter Voltage		V_{BE}				Vdc
(I_C = 3 Adc, V_{CE} = 5 Vdc)	2N3445, 2N3446		–	1.0	1.5	
(I_C = 5 Adc, V_{CE} = 5 Vdc)	2N3447, 2N3448		–	1.0	1.4	
Small Signal Current Gain		h_{fe}				–
(V_{CE} = 10 Vdc, I_C = 0.5 Adc, f = 1 KHz)	2N3445, 2N3446		20	–	100	
	2N3447, 2N3448		40	–	200	
(V_{CE} = 10 Vdc, I_C = 0.5 Adc, f = 10 MHz)	All Types		1.0	1.6	–	
Common Base Output Capacitance		C_{ob}				pf
(V_{CB} = 10 Vdc, f = 0.1 MHz)	All Types		–	260	400	
Switching Times						μs
(V_{CC} = 25 Vdc, R_L = 5 ohms, I_C = 5 A, I_{B1} = I_{B2} = 0.5 A)						
Delay Time plus Rise Time		$t_d + t_r$	–	0.15	0.35	
Storage Time		t_s	–	0.9	2.0	
Fall Time		t_f	–	0.15	0.35	

SAFE OPERATING AREAS

FIGURE 2 – 2N3445, 2N3447

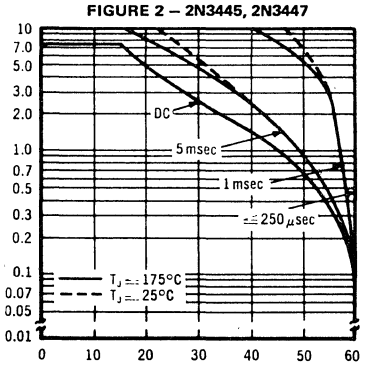
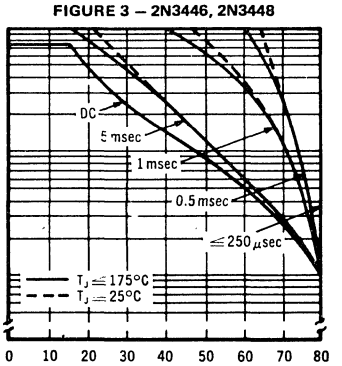


FIGURE 3 – 2N3446, 2N3448



V_{ce}, COLLECTOR-EMITTER VOLTAGE (VOLTS)

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector-emitter short. (Duty cycle of the excursions make no significant change in these safe areas.) To insure operation below the maximum T_J, the power-temperature derating curve must be observed for both steady state and pulse power conditions.

FIGURE 4 – BASE CURRENT-VOLTAGE VARIATIONS

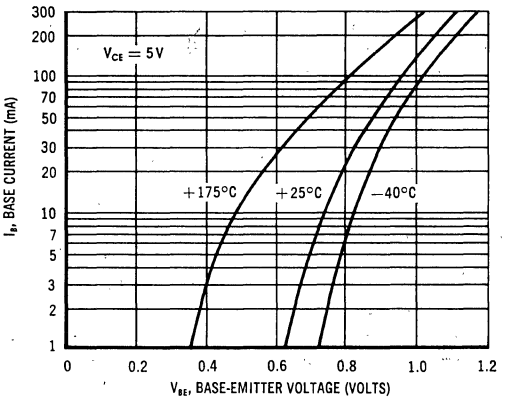
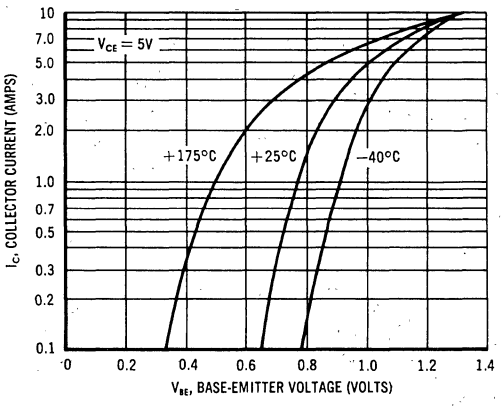


FIGURE 5 – COLLECTOR CURRENT-VOLTAGE VARIATIONS



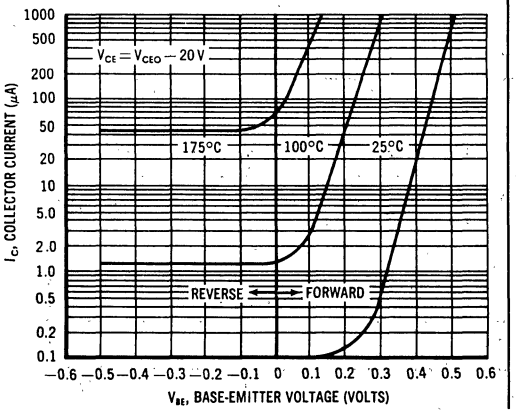
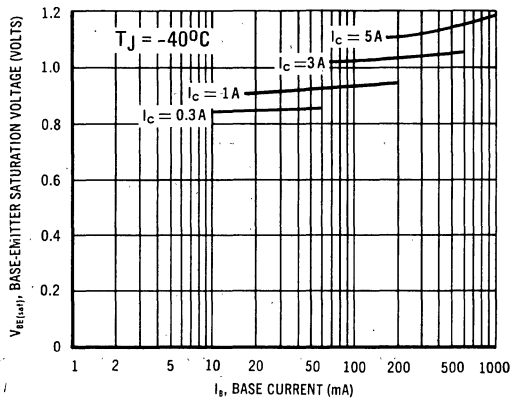
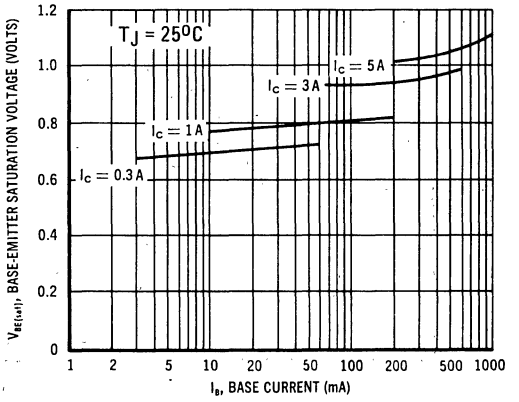


FIGURE 6 – BASE-EMITTER SATURATION VOLTAGE VARIATIONS





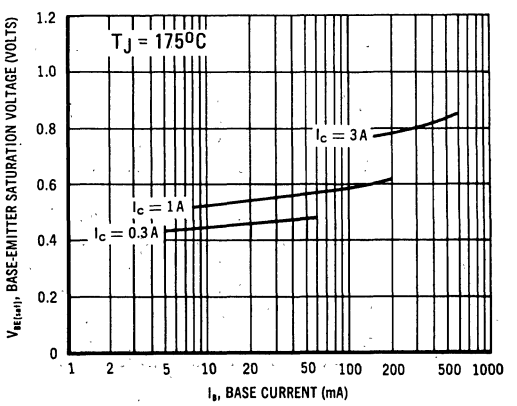
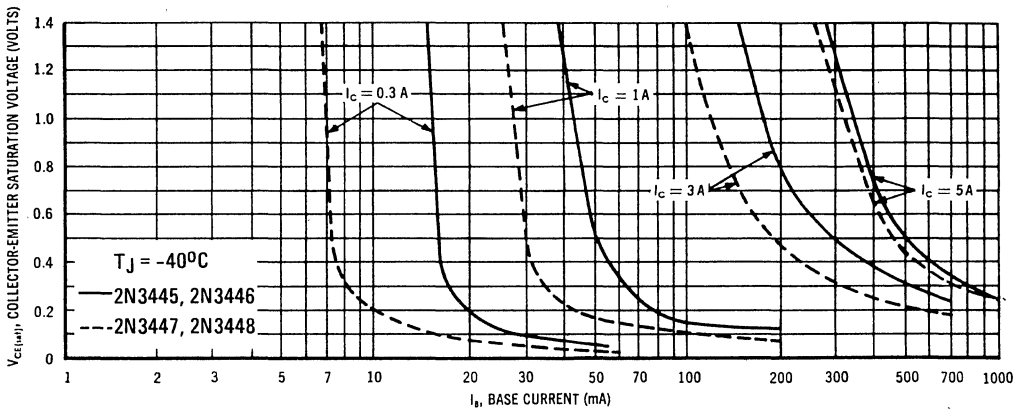
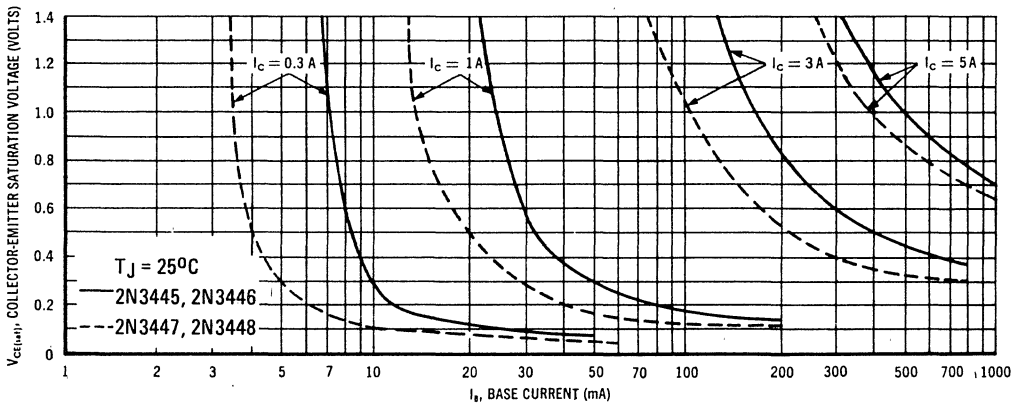


FIGURE 7 – COLLECTOR-EMITTER SATURATION VOLTAGE VARIATIONS





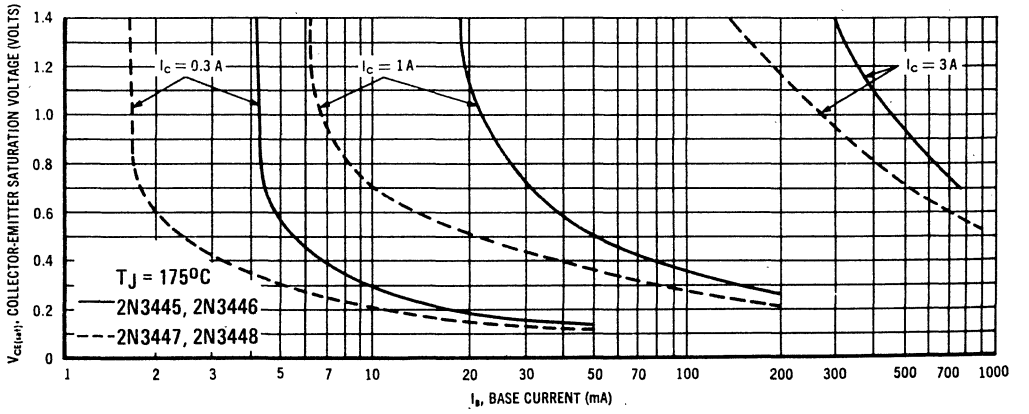


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FIGURE 8 – COLLECTOR CURRENT versus BASE CURRENT

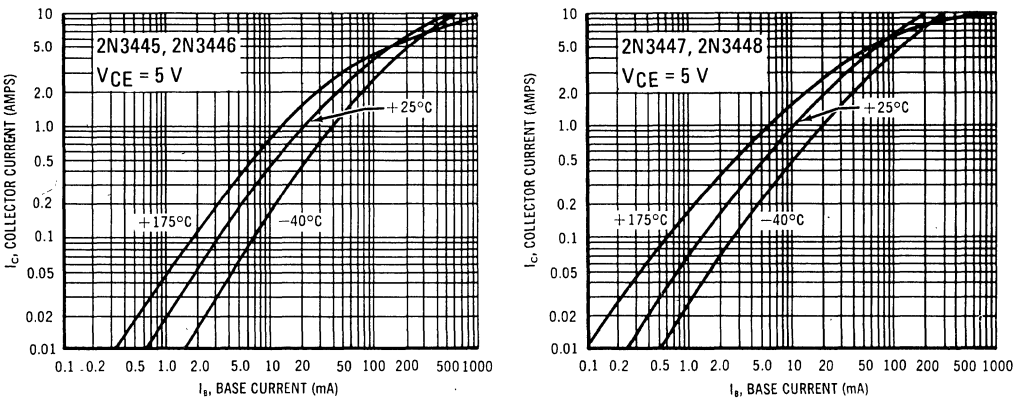


FIGURE 9 – CURRENT GAIN VARIATIONS

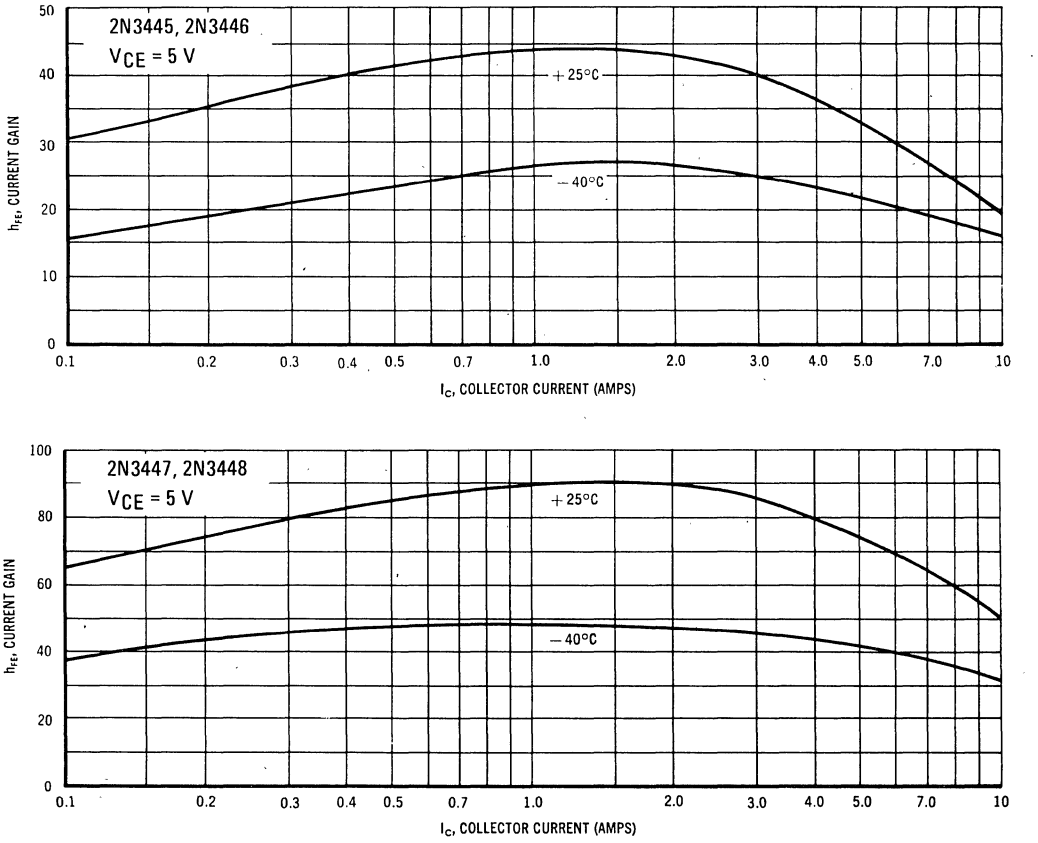
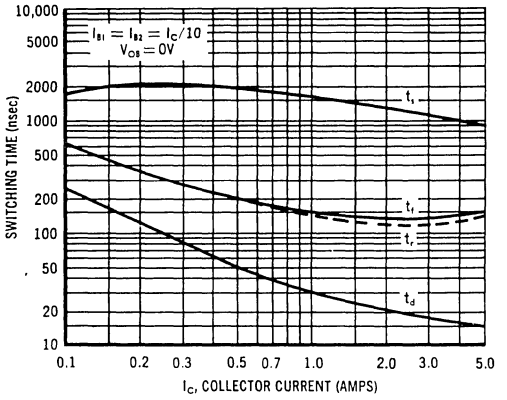


FIGURE 10 – TYPICAL SWITCHING TIMES



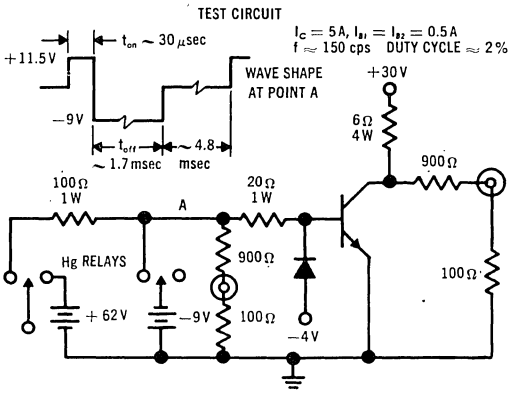


FIGURE 11 – ACTIVE REGION TIME CONSTANT

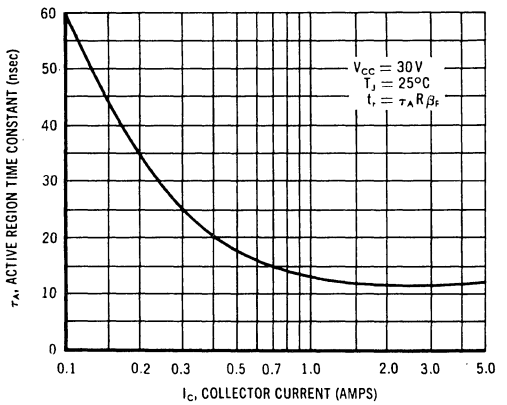


FIGURE 12 – RISE TIME FACTOR

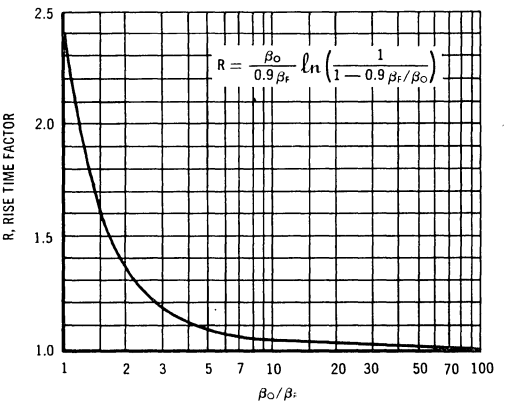


FIGURE 13 – COLLECTOR-EMITTER LEAKAGE CURRENT versus BASE-EMITTER RESISTANCE

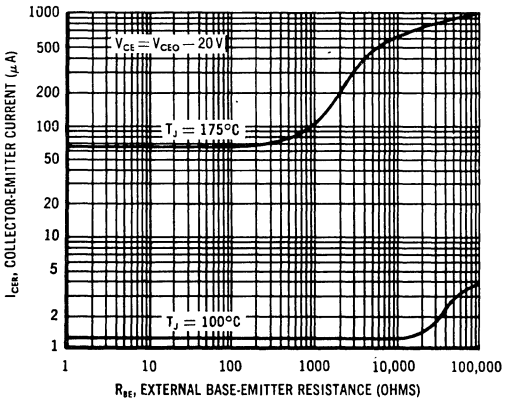
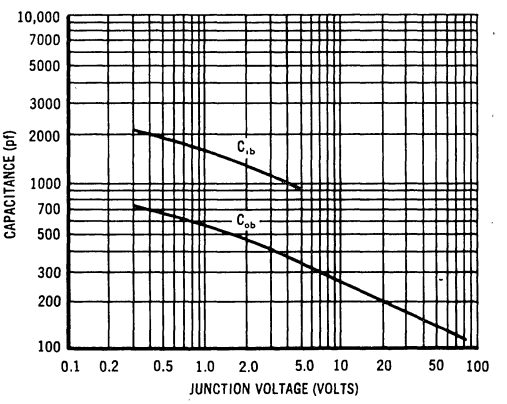


FIGURE 14 – JUNCTION CAPACITANCE versus REVERSE JUNCTION VOLTAGE



4

2N3583 thru 2N3585, 2N4240 NPN
2N6420 thru 2N6423 PNP

4

COMPLEMENTARY MEDIUM-POWER HIGH VOLTAGE POWER TRANSISTORS

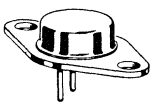
. . . designed for high-speed switching and linear amplifier applications for high-voltage operational amplifiers, switching regulators, converters, inverters, deflection stages and high fidelity amplifiers.

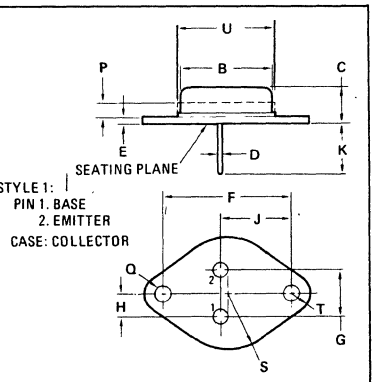
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 175 to 300 Vdc @ I_C = 200 mAdc
- Second Breakdown Collector Current –
  $I_{s/b}$ = 350 mAdc @ V_{CE} = 100 Vdc – NPN
  = 150 mAdc @ V_{CE} = 100 Vdc – PNP
- Usable DC Current Gain to 2.0 Adc

1.0 AND 2.0 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

250-500 VOLTS
35 WATTS





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

*MAXIMUM RATINGS

Rating	Symbol	2N3583 2N6420	2N3584 2N6421	2N3585 2N6422	2N4240 2N6423	Unit
Collector-Emitter Voltage	V_{CEO}	175	250	300	300	Vdc
Collector-Base Voltage	V_{CB}	250	375	500	500	Vdc
Emitter-Base Voltage	V_{EB}	6.0				Vdc
Collector Current—Continuous	I_C	1.0	2.0			Adc
—Peak (1)		5.0	5.0			
Base Current	I_B	1.0				Adc
Total Power Dissipation @ T_C = 25°C	P_D	35				Watts
Derate above 25°C		0.2				W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	5.0	°C/W

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	NPN	PNP	Symbol	NPN Min	NPN Max	PNP Min	PNP Max	Unit
***OFF CHARACTERISTICS (1)**								
Collector-Emitter Sustaining Voltage	2N3583	2N6420	$V_{CEO(sus)}$	175	–	175	–	Vdc
(I_C = 200 mAdc, I_B = 0) NPN	2N3584	2N6421		250	–	250	–	
	2N3585	2N6422		300	–	300	–	
(I_C = 50 mAdc, I_B = 0) PNP	2N4240	2N6423		300	–	300	–	
Collector Cutoff Current			I_{CEO}					mAdc
(V_{CE} = 150 Vdc, I_B = 0)	2N3583	2N6420		–	10	–	10	
	2N3584	2N6421		–	5.0	–	5.0	
	2N3585	2N6422		–	5.0	–	5.0	
	2N4240	2N6423		–	5.0	–	5.0	
Collector Cutoff Current			I_{CEX}					mAdc
(V_{CE} = 225 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N3583	2N6420		–	1.0	–	1.0	
(V_{CE} = 340 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N3584	2N6421		–	1.0	–	1.0	
(V_{CE} = 450 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N3585	2N6422		–	1.0	–	1.0	
	2N4240	2N6423		–	2.0	–	2.0	
(V_{CE} = 225 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3583	2N6420		–	3.0	–	3.0	
(V_{CE} = 300 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3584	2N6421		–	3.0	–	3.0	
	2N3585	2N6422		–	3.0	–	3.0	
	2N4240	2N6423		–	5.0	–	5.0	
Emitter Cutoff Current			I_{EBO}					mAdc
(V_{BE} = 6.0 Vdc, I_C = 0)	2N3583	2N6420		–	5.0	–	5.0	
	2N3584	2N6421		–	0.5	–	0.5	
	2N3585	2N6422		–	0.5	–	0.5	
	2N4240	2N6423		–	0.5	–	0.5	
ON CHARACTERISTICS (1)								
DC Current Gain	All	All	h_{FE}					–
(I_C = 0.1 Adc, V_{CE} = 10 Vdc)				40	–	40	–	
*(I_C = 0.5 Adc, V_{CE} = 10 Vdc)	2N3583	2N6420		40	200	40	200	
*(I_C = 0.75 Adc, V_{CE} = 2.0 Vdc)	2N4240	2N6423		10	100	10	100	
(I_C = 0.75 Adc, V_{CE} = 10 Vdc)	2N4240	2N6423		30	150	30	150	
*(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	2N3584	2N6421		8.0	80	8.0	80	
	2N3585	2N6422		8.0	80	8.0	80	
(I_C = 1.0 Adc, V_{CE} = 10 Vdc)	2N3583*	2N6420		10	–	10	–	
	2N3584	2N6421		25	100	25	100	
	2N3585	2N6422		25	100	25	100	
*Collector-Emitter Saturation Voltage			$V_{CE(sat)}$					Vdc
(I_C = 0.75 Adc, I_B = 75 mAdc)	2N4240	2N6423		–	1.0	–	1.0	
(I_C = 1.0 Adc, I_B = 125 mAdc)	2N3583	2N6420		–	5.0	–	5.0	
	2N3584	2N6421		–	0.75	–	0.75	
	2N3585	2N6422		–	0.75	–	0.75	
*Base-Emitter Saturation Voltage			$V_{BE(sat)}$					Vdc
(I_C = 0.75 Adc, I_B = 75 mAdc)	2N4240	2N6423		–	1.8	–	1.8	
(I_C = 1.0 Adc, I_B = 100 mAdc)	2N3584	2N6421		–	1.4	–	1.4	
	2N3585	2N6422		–	1.4	–	1.4	
Base-Emitter On Voltage	All	All	$V_{BE(on)}$					Vdc
(I_C = 1.0 Adc, V_{CE} = 10 Vdc)				–	1.4	–	1.4	

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

4

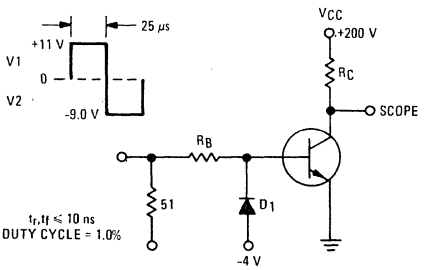
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	NPN	PNP	Symbol	NPN Min	NPN Max	PNP Min	PNP Max	Unit
DYNAMIC CHARACTERISTICS								
*Current Gain – Bandwidth Product[1] (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 5.0 MHz)	2N3583 2N3584 2N3585 2N4240	2N6420 2N6421 2N6422 2N6423	f_T	10 15	– –	10 15	– –	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	All		C_{ob}	–	120	–	120	pF
*Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 30 Vdc, f = 1.0 kHz)	2N3583	2N6420	h_{fe}	25	350	25	350	–
***SWITCHING CHARACTERISTICS**								
Rise Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, R_L = 200 Ohms, I_{B1} = 100 mAdc) (V_{CC} = 200 Vdc, I_C = 0.75 Adc, R_L = 267 Ohms, I_{B1} = 75 mAdc)	2N3584 2N3585 2N4240	2N6421 2N6422 2N6423	t_r	– –	3.0 0.5	– –	3.0 0.5	µs
Storage Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 100 mAdc) (V_{CC} = 200 Vdc, I_C = 0.75 Adc, I_{B1} = I_{B2} = 75 mAdc)	2N3584 2N3585 2N4240	2N6421 2N6422 2N6423	t_s	– –	4.0 6.0	– –	4.0 6.0	µs
Fall Time (V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 100 mAdc) (V_{CC} = 200 Vdc, I_C = 0.75 Adc, I_{B1} = I_{B2} = 75 mAdc)	2N3584 2N3585 2N4240	2N6421 2N6422 2N6423	t_f	– –	3.0 3.0	– –	3.0 3.0	µs
Second Breakdown Collector Current (V_{CE} = 100 Vdc)	All	All	$I_{s/b}$	350	–	150	–	mAdc

*Indicates JEDEC Registered Data

[1] $f_T = |h_{fe}| \bullet f_{test}$.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA
FOR t_d and t_r, D1 IS DISCONNECTED AND V_2 = 0.
FOR PNP TEST CIRCUIT, REVERSE DIODE AND VOLTAGE POLARITIES

NPN
2N3583 thru 2N3585,2N4240

PNP
2N6420 thru 2N6423

FIGURE 2 – TURN-ON TIME

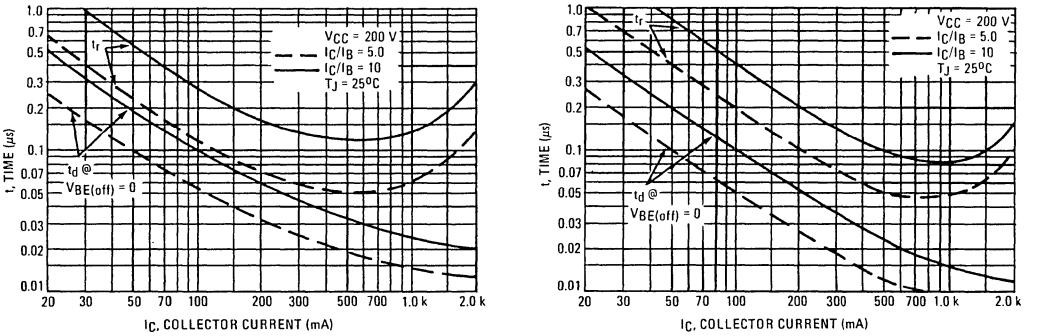


FIGURE 3 – TURN-OFF TIME

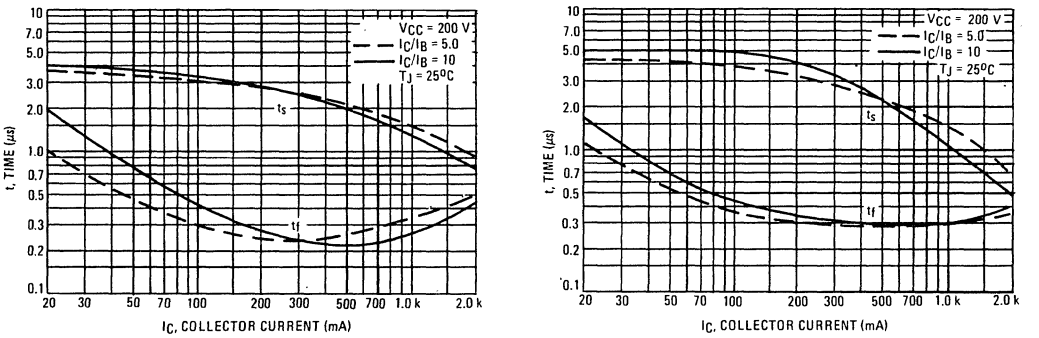


FIGURE 4 – CURRENT-GAIN – BANDWIDTH PRODUCT

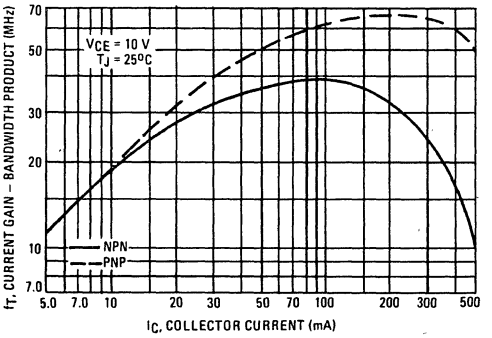


FIGURE 5 – CAPACITANCE

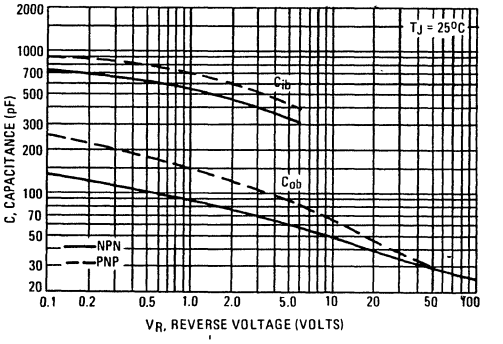
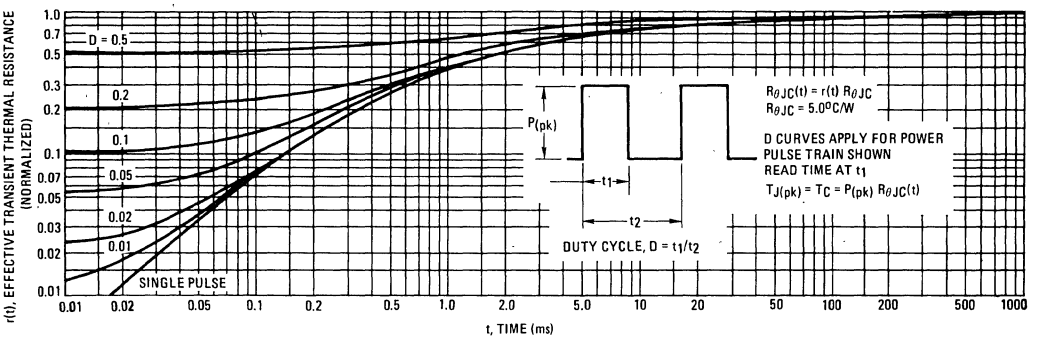


FIGURE 6 – THERMAL RESPONSE



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ACTIVE-REGION SAFE OPERATING AREA

FIGURE 7 – 2N3583 thru 2N3585, 2N4240

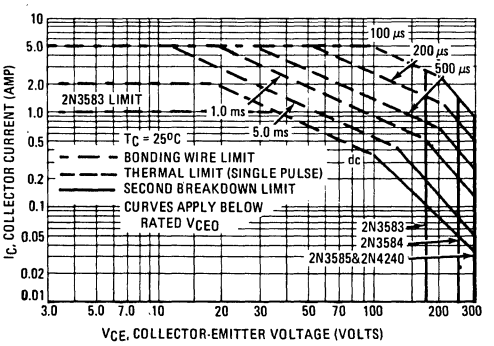


FIGURE 8 – 2N6420 thru 2N6423

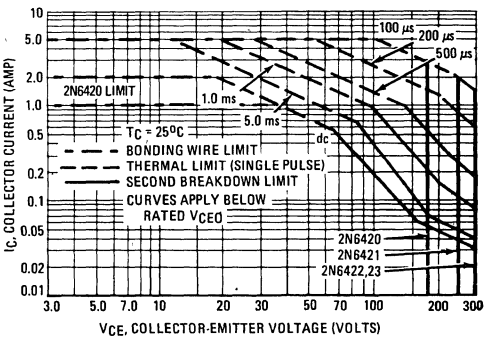
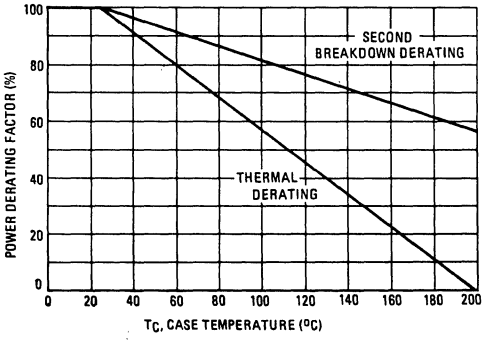


FIGURE 9 – POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 7 and 8 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 9.

$T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 7 and 8 may be found at any case temperature by using the appropriate curve on Figure 9.

NPN
2N3583 thru 2N3585,2N4240

PNP
2N6420 thru 2N6423

FIGURE 10 – DC CURRENT GAIN

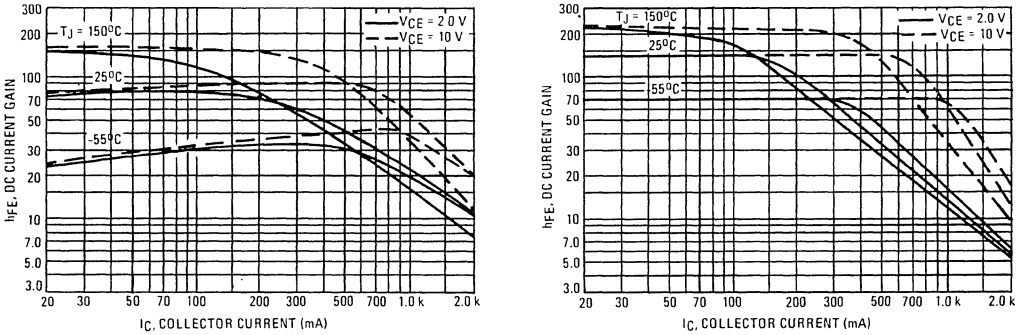


FIGURE 11 – COLLECTOR SATURATION REGION

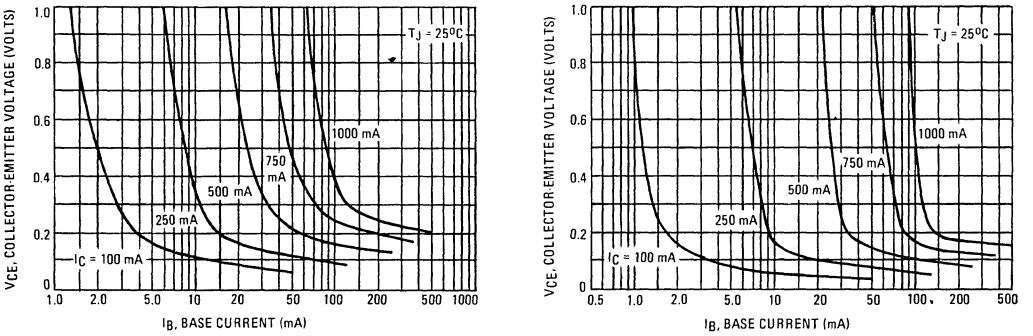
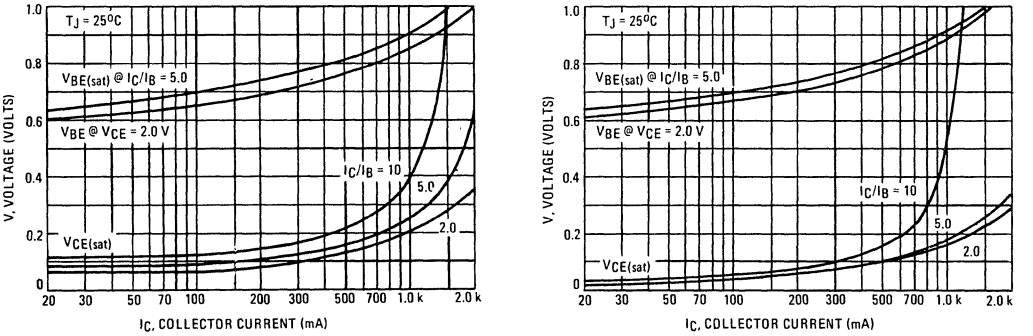


FIGURE 12 – "ON" VOLTAGES



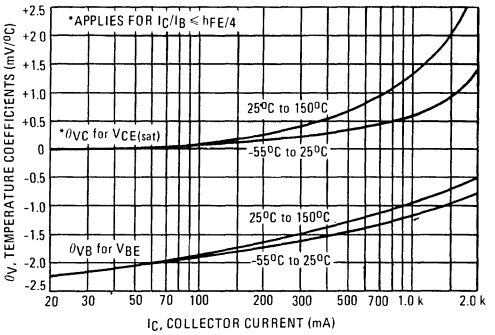
NOTE: DC CURRENT LIMIT FOR 2N3583, 2N6420 is 1.0 Amp.

4

NPN
2N3583 thru 2N3585,2N4240

PNP
2N6420 thru 2N6423

FIGURE 13 – TEMPERATURE COEFFICIENTS



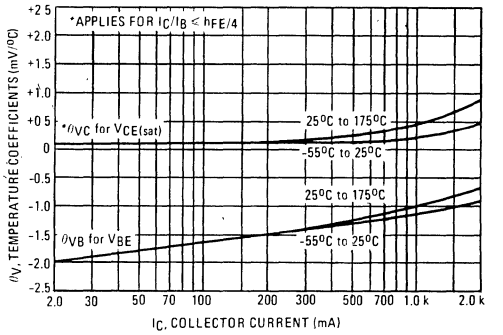
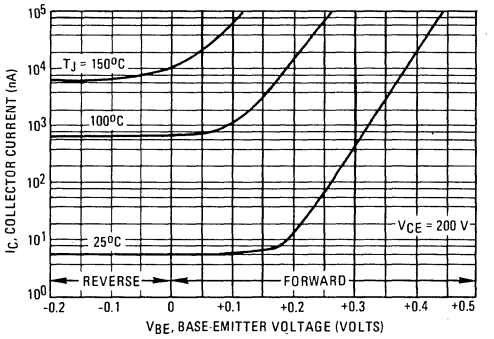


FIGURE 14 – COLLECTOR CUTOFF REGION



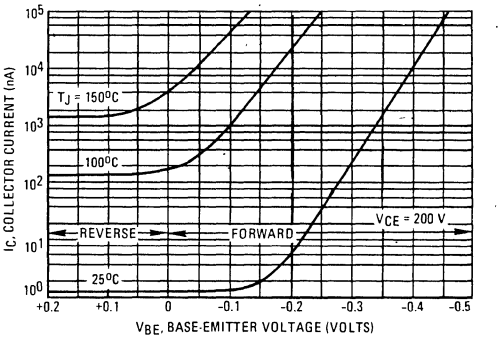
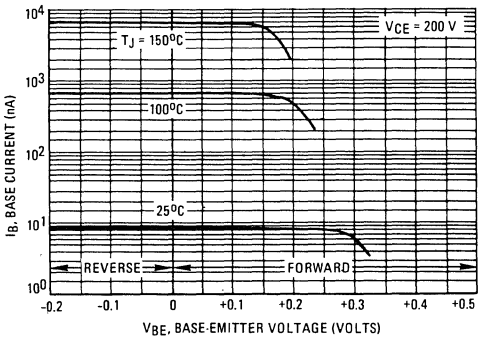
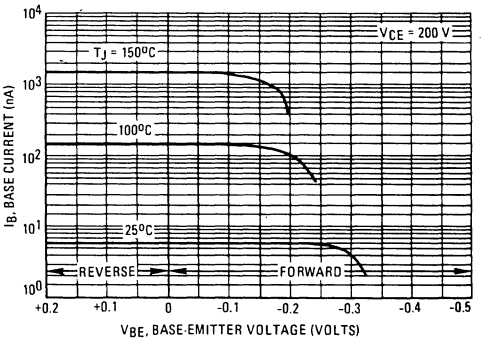


FIGURE 15 – BASE CUTOFF REGION





SILICON NPN POWER TRANSISTORS

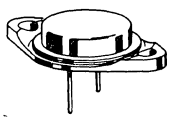
. . . designed for medium-speed switching and amplifier applications. These devices feature:

- Total Switching Time at 3 A typically 1.15 μs
- Gain Ranged Specified at 1 A and 3 A
- Low $V_{CE(sat)}$: typically 0.5V at I_C = 5A and I_B = 0.5A
- Excellent Safe Operating Areas
- Complement to 2N3789-92

10 AMPERE

POWER TRANSISTORS SILICON NPN

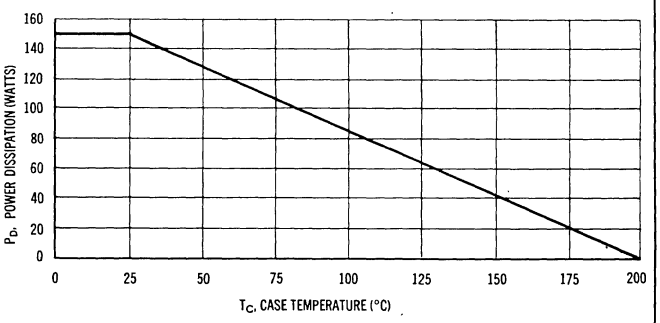
60-80 VOLTS
150 WATTS



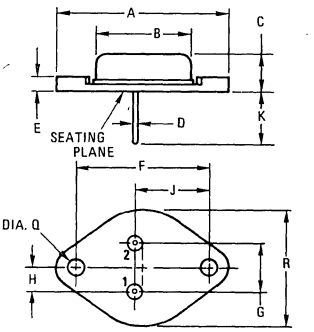
MAXIMUM RATINGS

Rating	Symbol	2N3713 2N3715	2N3714 2N3716	Unit
Collector-Base Voltage	V_{CB}	80	100	Volts
Collector-Emitter Voltage	V_{CEO}	60	80	Volts
Emitter-Base Voltage	V_{EB}	7.0	7.0	Volts
Collector Current (Continuous)	I_C	10	10	Amps
Base Current (Continuous)	I_B	4.0	4.0	Amps
Power Dissipation	P_D	150	150	Watts
Thermal Resistance	θ_{JC}	1.17	1.17	°C/W
Operating Junction and Storage Temperature Range	T_J and T_{stg}	-65 to +200		°C

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Limits are indicated by Figures 12, 13. Both limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

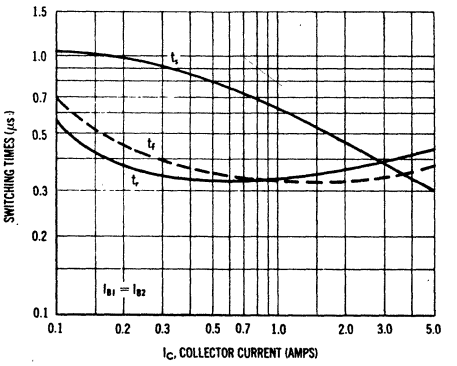
Collector connected to case.
CASE 11-01
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Emitter-Base Cutoff Current (V_{EB} = 7 Vdc)	All Types	I_{EBO}	—	5	mAdc
Collector-Emitter Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 80 Vdc, V_{BE} = -1.5 Vdc)	2N3713, 2N3715		—	1	
(V_{CE} = 100 Vdc, V_{BE} = -1.5 Vdc)	2N3714, 2N3716		—	1	
(V_{CE} = 60 Vdc, V_{BE} = -1.5 Vdc, T_C = 150°C)	2N3713, 2N3715		—	10	
(V_{CE} = 80 Vdc, V_{BE} = -1.5 Vdc, T_C = 150°C)	2N3714, 2N3716		—	10	
Collector-Emitter Sustaining Voltage*		$V_{CEO(sus)}$*			Vdc
(I_C = 200 mAdc, I_B = 0)	2N3713, 2N3715		60	—	
	2N3714, 2N3716		80	—	
DC Current Gain*		h_{FE}*			—
(I_C = 1 Adc, V_{CE} = 2 Vdc)	2N3713, 2N3714		25	90	
	2N3715, 2N3716		50	150	
(I_C = 3 Adc, V_{CE} = 2 Vdc)	2N3713, 2N3714		15	—	
	2N3715, 2N3716		30	—	
Collector-Emitter Saturation Voltage*		$V_{CE(sat)}$*			Vdc
(I_C = 5 Adc, I_B = 0.5 Adc)	2N3713, 2N3714		—	1.0	
	2N3715, 2N3716		—	0.8	
Base-Emitter Saturation Voltage*		$V_{BE(sat)}$*			Vdc
(I_C = 5 Adc, I_B = 0.5 Adc)	2N3713, 2N3714		—	2.0	
	2N3715, 2N3716		—	1.5	
Base-Emitter Voltage*		V_{BE}*			Vdc
(I_C = 3 Adc, V_{CE} = 2 Vdc)	All Types		—	1.5	
Small Signal Current Gain		h_{fe}			—
(V_{CE} = 10 Vdc, I_C = 0.5 Adc, f = 1 MHz)	All Types		4	—	
Switching Times (Figure 2)			Typ		μs
(I_C = 5A, I_{B1} = I_{B2} = 0.5 Adc)					
Rise Time		t_r	0.45		
Storage Time		t_s	0.3		
Fall Time		t_f	0.4		

*Use sweep test to prevent overheating

FIGURE 2 – TYPICAL SWITCHING TIMES



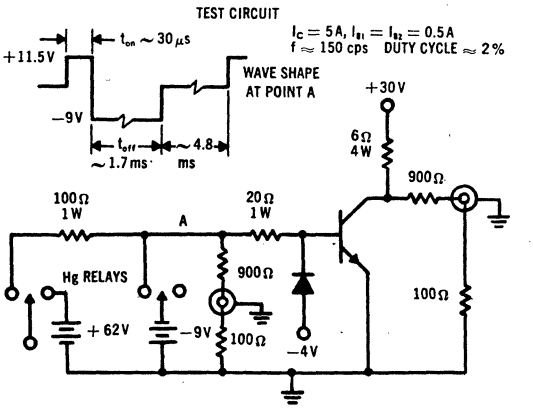


FIGURE 3 – COLLECTOR CURRENT versus BASE CURRENT

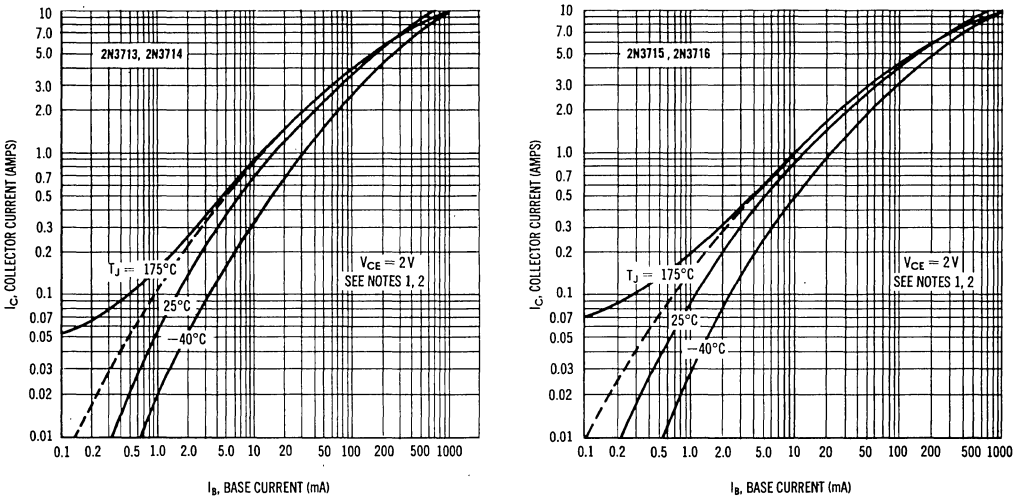


FIGURE 4 – BASE CURRENT-VOLTAGE VARIATIONS

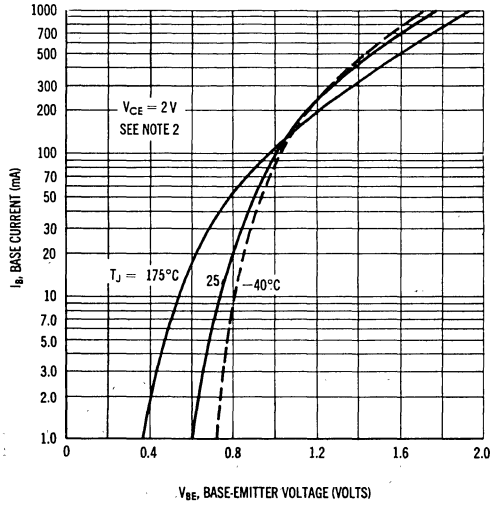
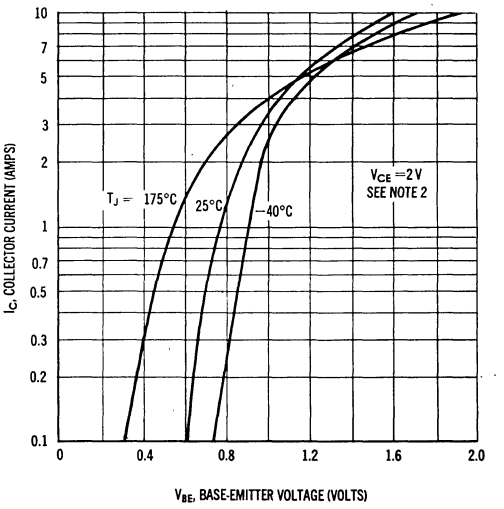


FIGURE 5 – COLLECTOR CURRENT-VOLTAGE VARIATIONS



NOTE 1. Dotted line indicates metered base current plus the I_{CBO} of the transistor at 175°C.

NOTE 2. Pulse test: pulse width ≈ 200 μsec, duty cycle ≈ 1.5%

FIGURE 6 – COLLECTOR-EMITTER SATURATION VOLTAGE VARIATIONS

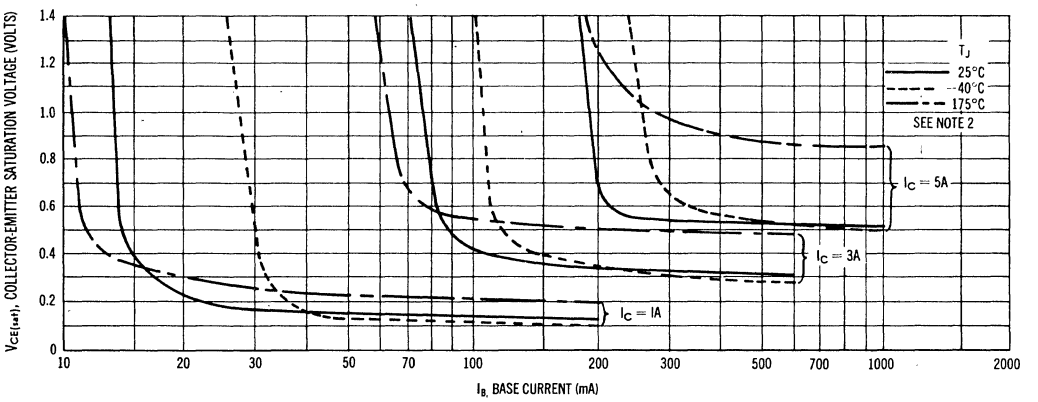


FIGURE 7 – BASE-EMITTER SATURATION VOLTAGE VARIATIONS

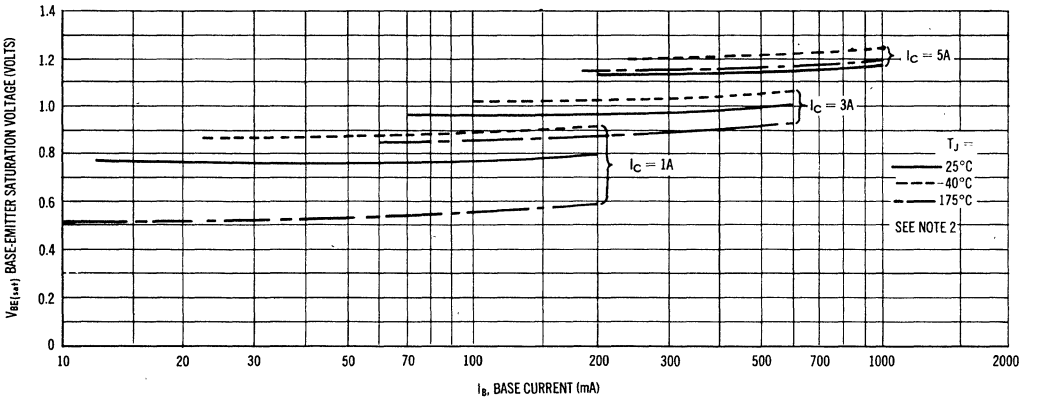


FIGURE 8 – COLLECTOR CURRENT versus BASE-EMITTER VOLTAGE

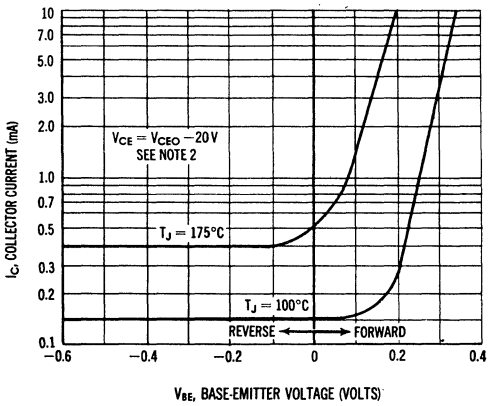


FIGURE 9 – COLLECTOR CURRENT versus BASE-EMITTER RESISTANCE

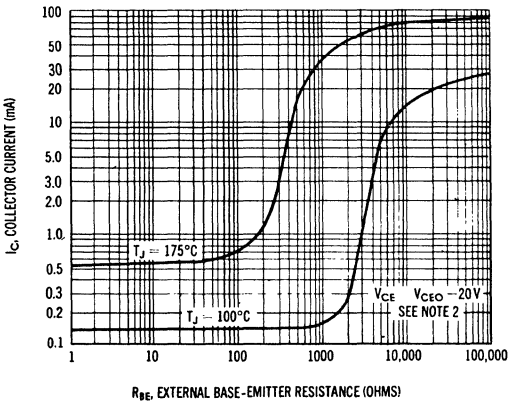
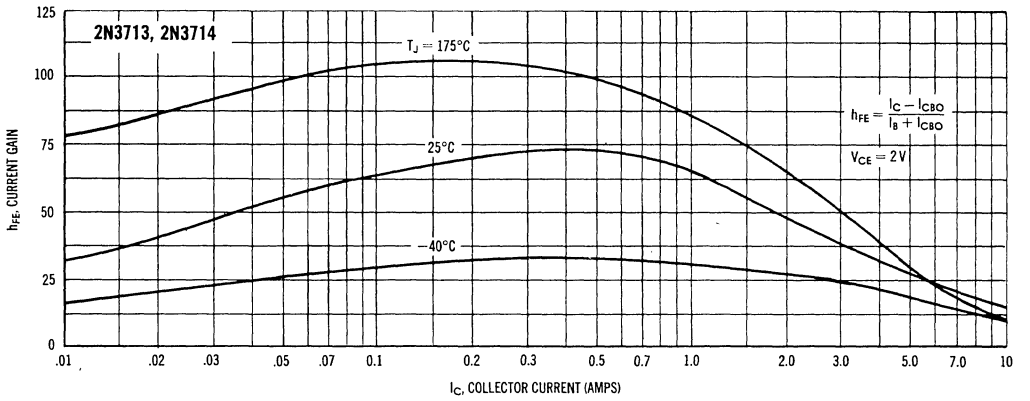


FIGURE 10 – CURRENT GAIN VARIATIONS



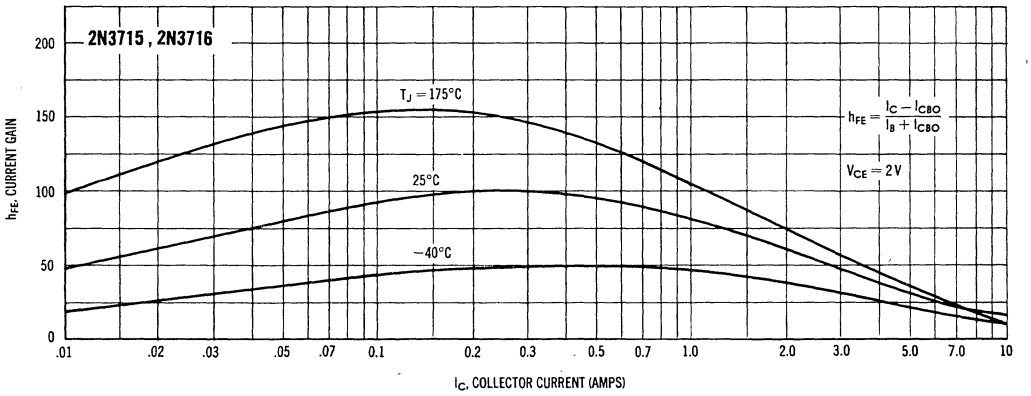
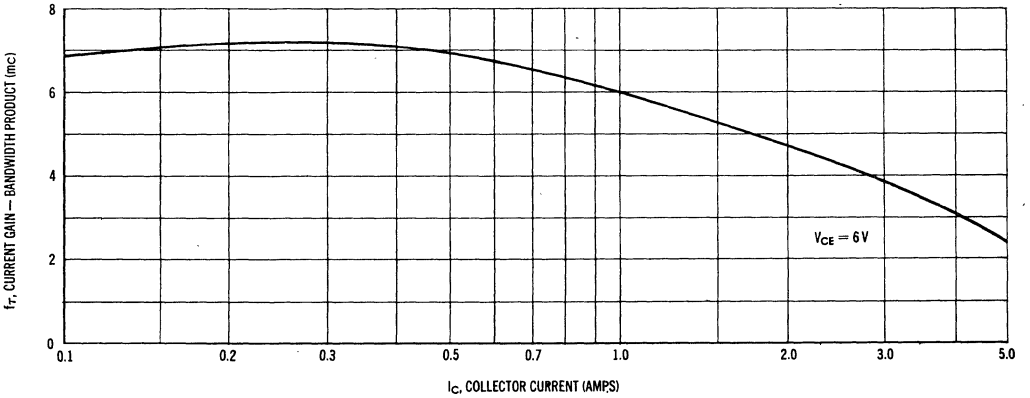


FIGURE 11 – CURRENT GAIN – BANDWIDTH PRODUCT versus COLLECTOR CURRENT



SAFE OPERATING AREAS

FIGURE 12 – 2N3713, 2N3715

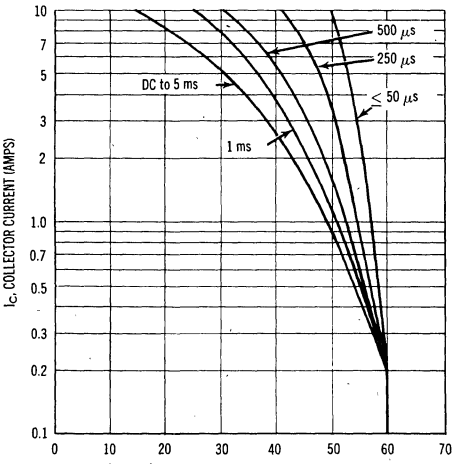
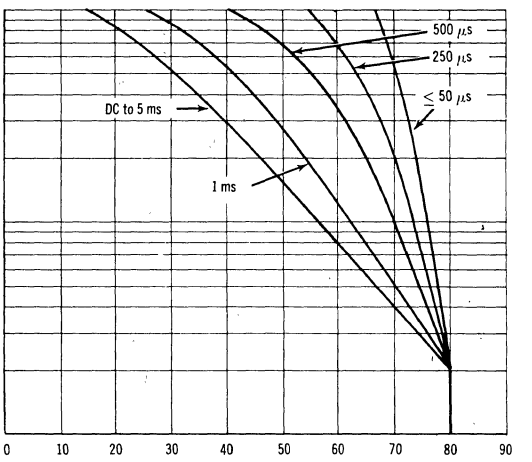


FIGURE 13 – 2N3714, 2N3716



VCE, COLLECTOR-EMITTER VOLTAGE (VOLTS)

The Safe Operating Area Curves indicate I_C — V_{CE} limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector-emitter short. (Duty cycle of the excursions make no significant change in these safe areas.) To insure operation below the maximum T_J, the power-temperature derating curve must be observed for both steady state and pulse power conditions.

2N3719, 2N3720 (SILICON)
2N3867, 2N3868
2N6303

SILICON PNP POWER TRANSISTORS

. . . designed for high-speed, medium-current switching and high-frequency amplifier applications.

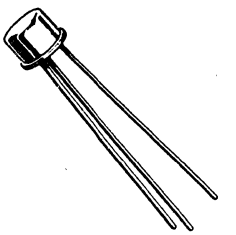
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 40 Vdc (Min) – 2N3719,2N3867
  = 60 Vdc (Min) – 2N3720,2N3868
  = 80 Vdc (Min) – 2N6303
- DC Current Gain –
  h_{FE} = 25-180 @ I_C = 1.0 Adc – 2N3719,2N3720
  = 40-200 @ I_C = 1.5 Adc – 2N3867
  = 30-150 @ I_C = 1.5 Adc – 2N3868,2N6303
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.75 Vdc @ I_C = 1.0 Adc – 2N3719,2N3720
  = 0.75 Vdc @ I_C = 1.5 Adc – 2N3867,2N3868, 2N6303
- High Current-Gain – Bandwidth Product –
  f_T = 90 MHz (Typ)
- 2N3867 JAN and 2N3868 JAN also Available

3 AMPERE

POWER TRANSISTORS PNP SILICON

40,60,80 VOLTS
6 WATTS

4



***MAXIMUM RATINGS**

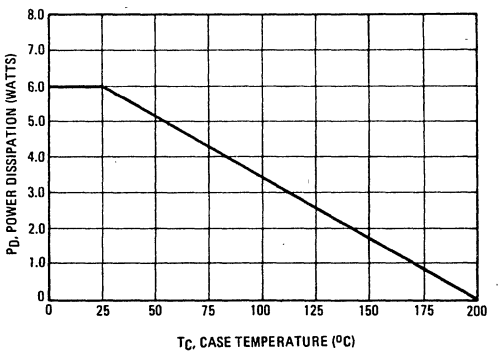
Rating	Symbol	2N3719 2N3867	2N3720 2N3868	2N6303	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4.0			Vdc
Collector Current – Continuous	I_C	3.0			Adc
Peak		10			
Base Current	I_B	0.5			Adc
Total Device Dissipation @ T_C = 25°C	P_D	6.0			Watts
Derate above 25°C		34.3			mW/°C
Total Device Dissipation @ T_A = 25°C	P_D	1.0			Watt
Derate above 25°C		5.71			mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			°C

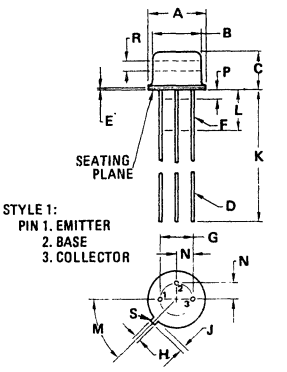
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	29	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	175	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING





DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.711	0.864	0.028	0.034
J	0.734	1.14	0.029	0.045
K	38.10	–	1.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	2.54 BSC		0.100 BSC	
P	–	1.27	–	0.050
R	2.54	–	0.100	–
S	–	0.179	–	0.007

All JEDEC dimensions and notes apply.

CASE 31-03
TO-5

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 20 mAdc, I_B = 0)	2N3867		40	–	
	2N3868		60	–	
	2N6303		80	–	
Collector-Base Breakdown Voltage		BV_{CBO}			Vdc
(I_C = 100 μAdc, I_E = 0)	2N3867		40	–	
	2N3868		60	–	
	2N6303		80	–	
Emitter-Base Breakdown Voltage		BV_{EBO}			Vdc
(I_E = 100 μAdc, I_C = 0)			4.0	–	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 2.0 Vdc)			–	1.0	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = Rated V_{CB}, I_E = 0, T_C = 150°C)			–	150	
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)	2N3867		50	–	
	2N3868, 2N6303		35	–	
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	2N3867		40	200	
	2N3868, 2N6303		30	150	
(I_C = 2.5 Adc, V_{CE} = 3.0 Vdc)	2N3867		25	–	
	2N3868, 2N6303		20	–	
(I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)	2N3867		20	–	
	2N3868, 2N6303				
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			–	0.5	
(I_C = 1.5 Adc, I_B = 150 mAdc)			–	0.75	
(I_C = 2.5 Adc, I_B = 250 mAdc)			–	1.3	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			–	1.0	
(I_C = 1.5 Adc, I_B = 150 mAdc)			0.9	1.4	
(I_C = 2.5 Adc, I_B = 250 mAdc)			–	2.0	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (2)		f_T			MHz
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc, f_{test} = 20 MHz)			60	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)			–	120	
Input Capacitance		C_{ib}			pF
(V_{EB} = 3.0 Vdc, I_C = 0, f = 0.1 MHz)			–	1000	
SWITCHING CHARACTERISTICS					
Delay Time	(V_{CC} = 30 Vdc, $V_{BE(off)}$ = 0,	t_d	–	35	ns
Rise Time	I_C = 1.5 Adc, I_{B1} = 150 mAdc)	t_r	–	65	ns
Storage Time	(V_{CC} = 30 Vdc, I_C = 1.5 Adc,	t_s	–	325	ns
Fall Time	I_{B1} = I_{B2} = 150 mAdc)	t_f	–	75	ns

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$

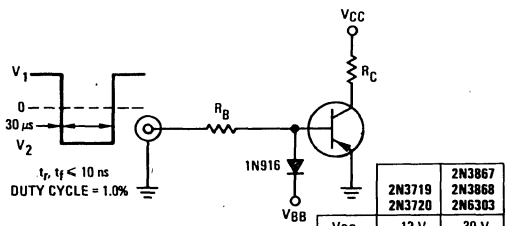
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 20 mAdc, I_B = 0)	2N3719		40	–	
	2N3720		60	–	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 2.0 Vdc)	2N3719		–	10	μAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 2.0 Vdc)	2N3720		–	10	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_C = 150°C)	2N3719		–	1.0	mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 2.0 Vdc, T_C = 150°C)	2N3720		–	1.0	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N3719		–	10	
(V_{CB} = 60 Vdc, I_E = 0)	2N3720		–	10	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 4.0 Vdc, I_C = 0)			–	1.0	
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 500 mAdc, V_{CE} = 1.5 Vdc)			20	–	
(I_C = 1.0 Adc, V_{CE} = 1.5 Vdc)			25	180	
(I_C = 1.0 Adc, V_{CE} = 1.5 Vdc, T_C = -40°C)			15	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 100 mAdc, T_C = -40°C to +100°C)			–	0.75	
(I_C = 3.0 Adc, I_B = 300 mAdc, T_C = -40°C to +100°C)			–	1.5	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 100 mAdc, T_C = -40°C to +100°C)			–	1.5	
(I_C = 3.0 Adc, I_B = 300 mAdc, T_C = -40°C to +100°C)			–	2.3	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (2)		f_T			MHz
(I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 30 MHz)			60	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)			–	120	
Input Capacitance		C_{ib}			pF
(V_{EB} = 0.5 Vdc, I_C = 0, f = 0.1 MHz)			–	1000	
SWITCHING CHARACTERISTICS					
Turn-On Time		t_{on}			ns
(V_{CC} = 12 Vdc, $V_{BE(off)}$ = 0, I_C = 1.0 Adc, I_{B1} = 0.1 Adc)			–	100	
Turn-Off Time		t_{off}			ns
(V_{CC} = 12 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 100 mAdc)			–	400	

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2.0%. (2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



	2N3719 2N3720	2N3867 2N3868 2N6303
V_{CC}	-12 V	-30 V
R_C	12 Ω	19 Ω
R_B	100 Ω	100 Ω
V_1	+8.0 V	13.6 V
V_2	-11 V	-16.4 V
V_{BB}	≈ 3.0 V	≈ 3.0 V

NOTE:
For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.
For t_d and t_r specifications, remove diode and set V_1 = 0.

FIGURE 3 – TURN-ON TIME

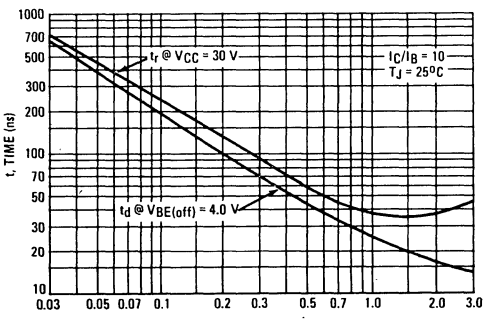
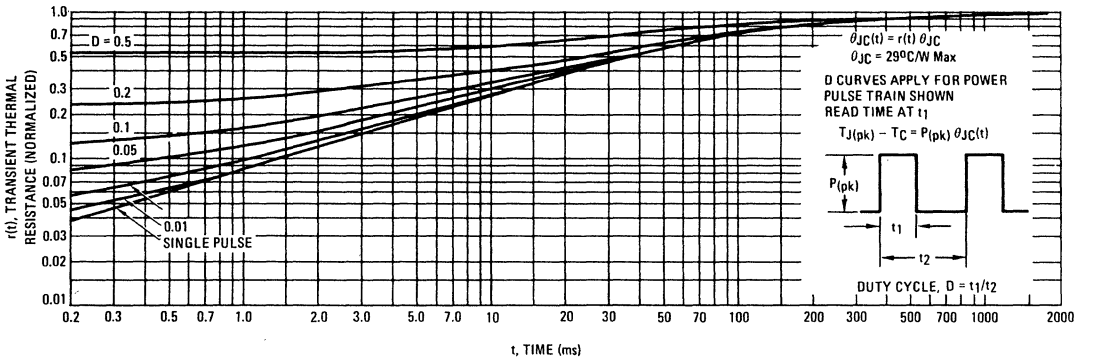
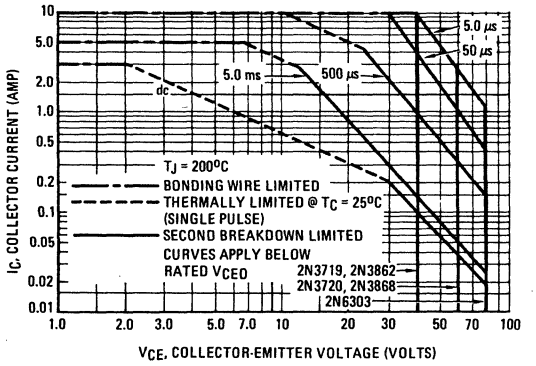


FIGURE 4 – THERMAL RESISTANCE



4

FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

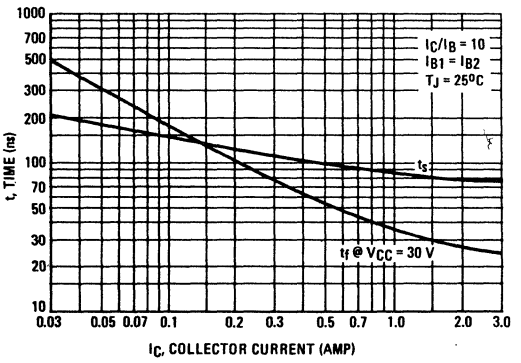


FIGURE 7 – CAPACITANCE

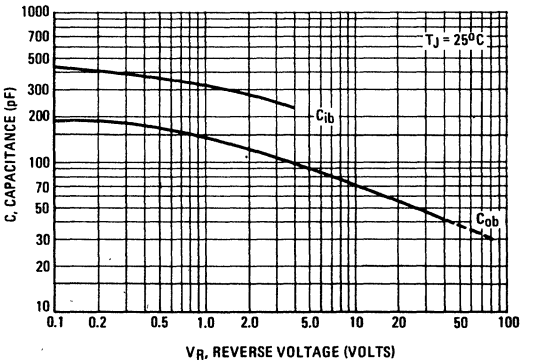


FIGURE 8 – DC CURRENT GAIN

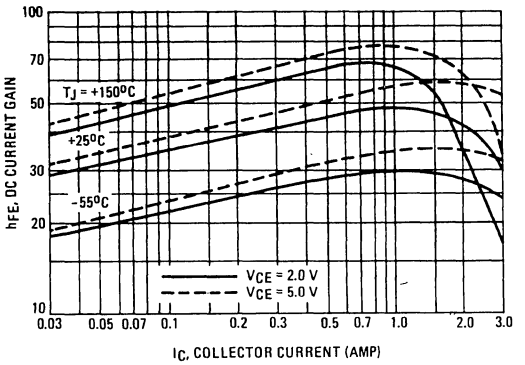


FIGURE 9 – COLLECTOR SATURATION REGION

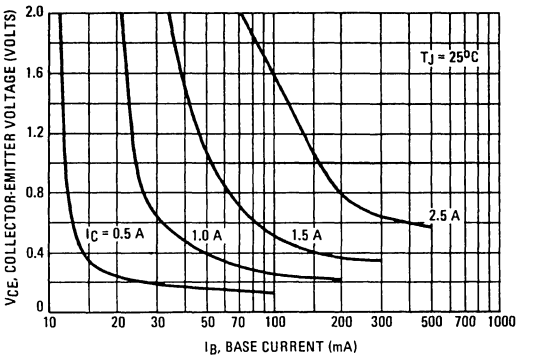


FIGURE 10 – "ON" VOLTAGES

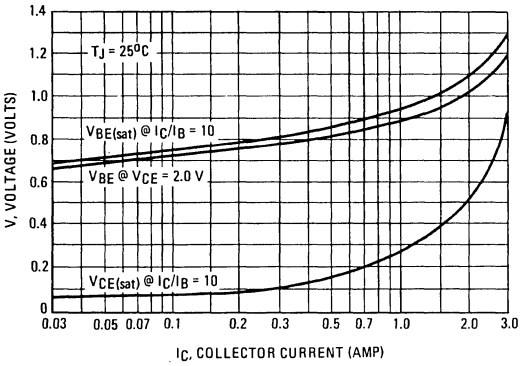


FIGURE 11 – TEMPERATURE COEFFICIENTS

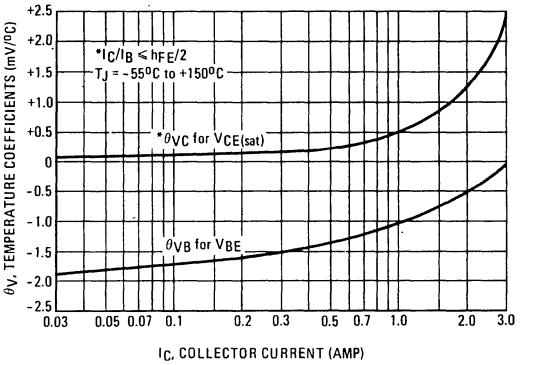


FIGURE 12 – COLLECTOR CUT-OFF REGION

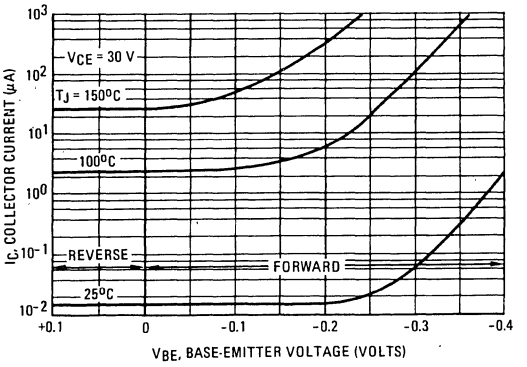
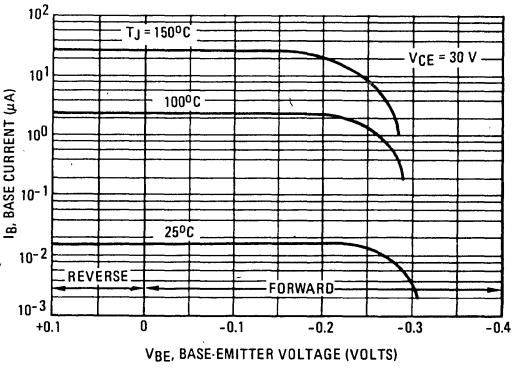


FIGURE 13 – BASE CUT-OFF REGION



2N3738, 2N3739 NPN (SILICON)
2N6424, 2N6425 PNP

HIGH VOLTAGE COMPLEMENTARY SILICON POWER TRANSISTORS

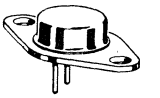
. . . designed for high-speed switching, linear amplifier applications, high-voltage operational amplifiers, switching regulators, converters, inverters, deflection stages and high fidelity amplifiers.

- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 225 Vdc @ I_C = 5.0 mAdc (2N3738, 2N6424)
  = 300 Vdc @ I_C = 5.0 mAdc (2N3739, 2N6425)
- DC Current Gain –
  h_{FE} = 40-200 @ I_C = 100 mAdc
- Current-Gain – Bandwidth Product –
  f_T = 10 MHz (Min) @ I_C = 100 mAdc
- $I_{S/b}$ Rated to 2.0 Amperes

1.0 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

225, 300 VOLTS
20 WATTS



*MAXIMUM RATINGS

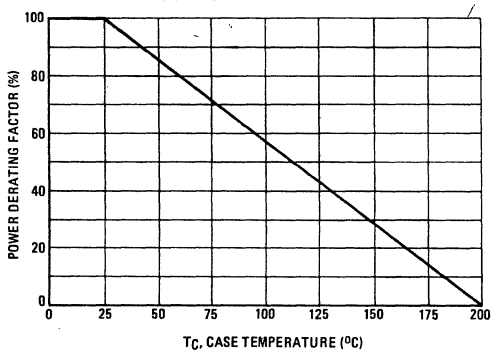
Rating	Symbol	2N3738 2N6424	2N3739 2N6425	Unit
Collector-Emitter Voltage	V_{CEO}	225	300	Vdc
Collector-Base Voltage	V_{CB}	250	325	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current – Continuous – Peak	I_C	1.0 2.0		Adc
Base Current – Continuous – Peak	I_B	0.50 1.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.133		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

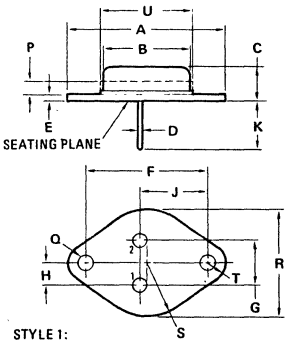
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	7.5	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

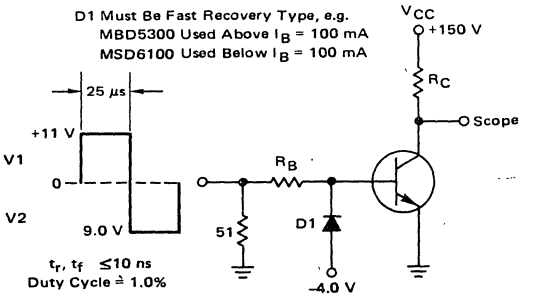
Characteristic		Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 5.0 mAdc, I_B = 0)	2N3738, 2N6424		225	–	
	2N3739, 2N6425		300	–	
Collector-Emitter Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 125 Vdc, I_B = 0)	2N3738, 2N6424		–	0.25	
(V_{CE} = 200 Vdc, I_B = 0)	2N3739, 2N6425		–	0.25	
Collector-Base Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 250 Vdc, I_E = 0)	2N3738, 2N6424		–	0.1	
(V_{CB} = 325 Vdc, I_E = 0)	2N3739, 2N6425		–	0.1	
Collector Cutoff Current		I_{CEV}			mAdc
(V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N3738, 2N6424		–	0.5	
(V_{CE} = 300 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N3739, 2N6425		–	0.5	
(V_{CE} = 125 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N3738, 2N6424		–	1.0	
(V_{CE} = 200 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N3739, 2N6425		–	1.0	
Emitter-Base Cutoff Current		I_{EBO}			mAdc
(V_{EB} = 6.0 Vdc)			–	0.1	
***ON CHARACTERISTICS**					
DC Current Gain (1)		h_{FE}			–
(I_C = 50 mAdc, V_{CE} = 10 Vdc)			30	–	
(I_C = 100 mAdc, V_{CE} = 10 Vdc)			40	200	
(I_C = 250 mAdc, V_{CE} = 10 Vdc)			25	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 250 mAdc, I_B = 25 mAdc)			–	2.5	
Base-Emitter "ON" Voltage (1)		$V_{BE(on)}$			Vdc
(I_C = 100 mAdc, V_{CE} = 10 Vdc)			–	1.0	
SMALL SIGNAL CHARACTERISTICS					
Current-Gain – Bandwidth Product (2)		f_T			MHz
(I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)			10	–	
*Output Capacitance		C_{ob}			pF
(V_{CB} = 100 Vdc, I_E = 0, f = 100 kHz)			–	20	
*Small-Signal Current Gain		h_{fe}			–
(I_C = 100 mAdc, V_{CE} = 20 Vdc, f = 1.0 kHz)			35	–	

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

(2) $f_T = |h_{fe}| \bullet$ frequency

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



R_B and R_C Varied to Obtain Desired Current Levels

For t_d and t_r, D1 is disconnected and V2 = 0
For PNP test circuit, reverse diode and voltage polarities.

NPN
2N3738, 2N3739

PNP
2N6424, 2N6425

FIGURE 3 – TURN-ON TIME

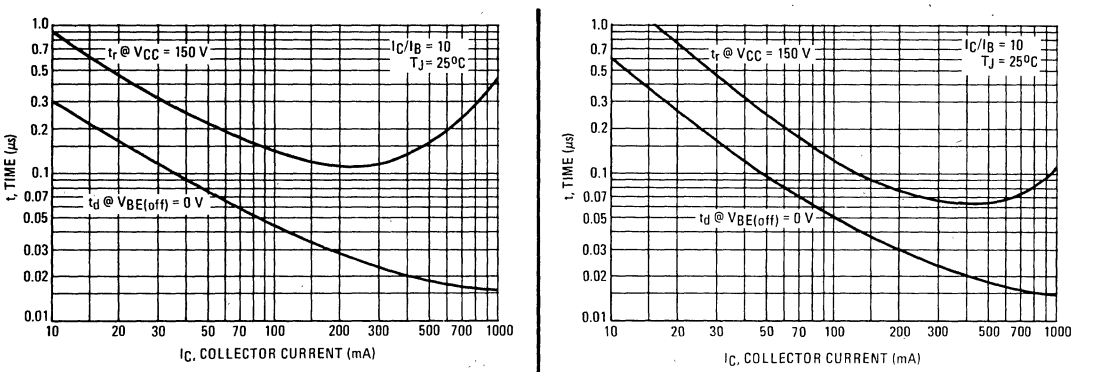


FIGURE 4 – TURN-OFF TIME

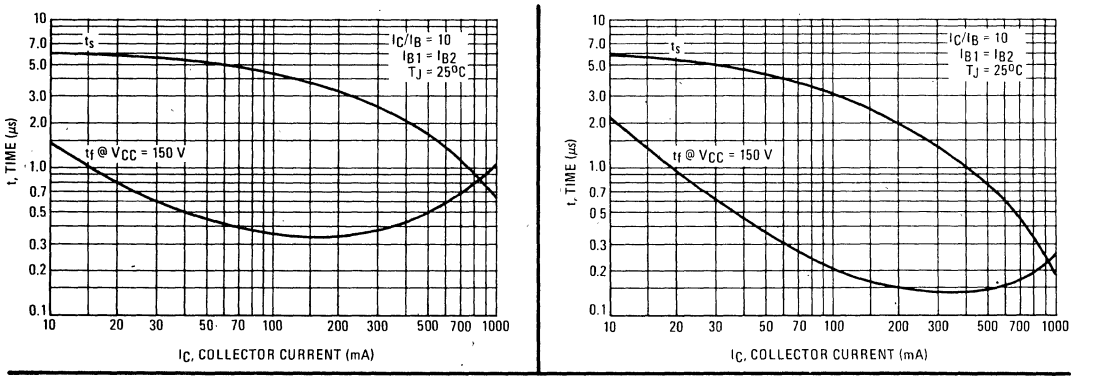


FIGURE 5 – CURRENT-GAIN – BANDWIDTH PRODUCT

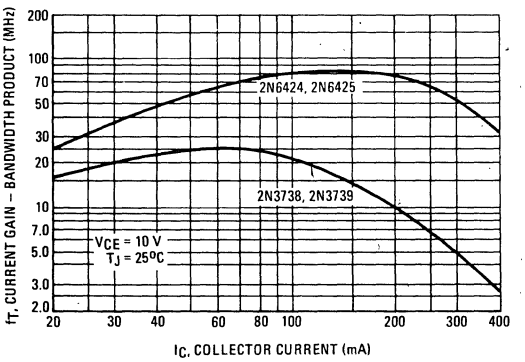


FIGURE 6 – CAPACITANCE

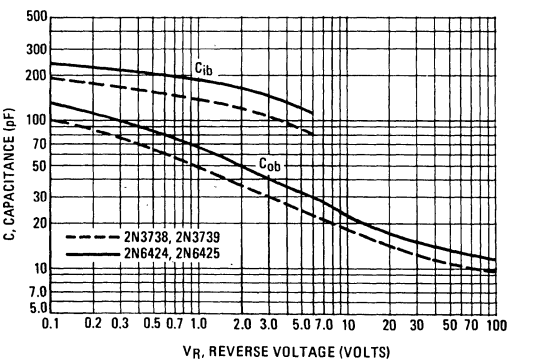
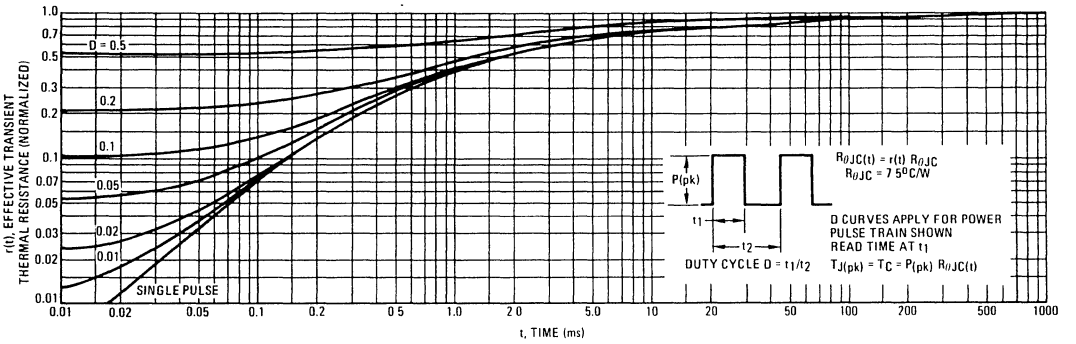


FIGURE 7 – THERMAL RESPONSE



4

ACTIVE-REGION SAFE OPERATING AREA

FIGURE 8 – 2N3738, 2N3739

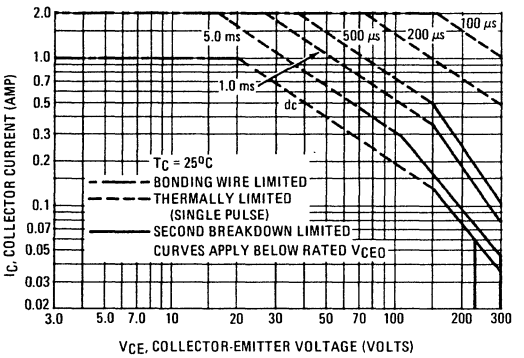
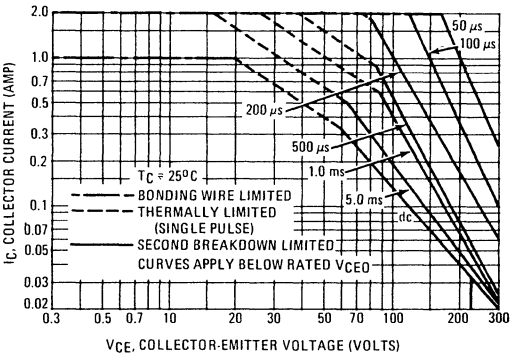


FIGURE 9 – 2N6424, 2N6425



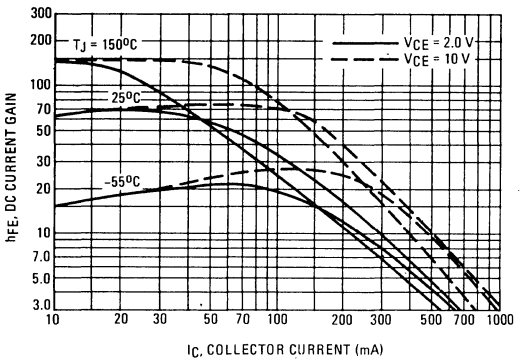
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 8 and 9 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 175^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 7. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 8 and 9 may be found at any case temperature by using the appropriate curve on Figure 1.

NPN
2N3738, 2N3739

PNP
2N6424, 2N6425

FIGURE 10 – DC CURRENT GAIN



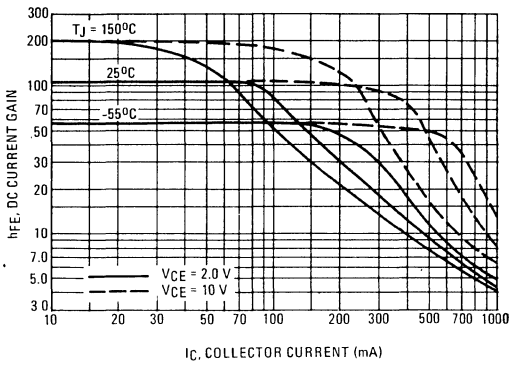
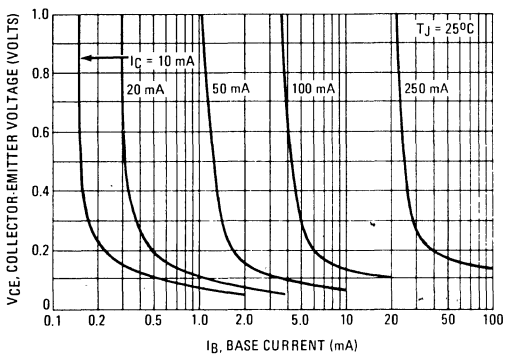


FIGURE 11 – COLLECTOR SATURATION REGION



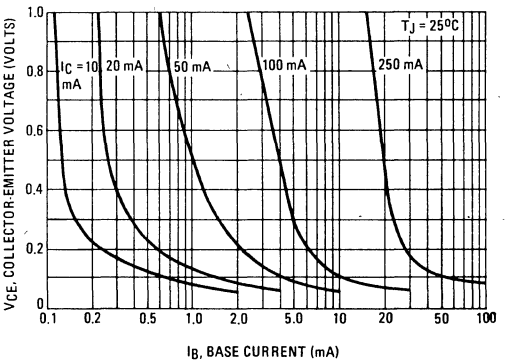
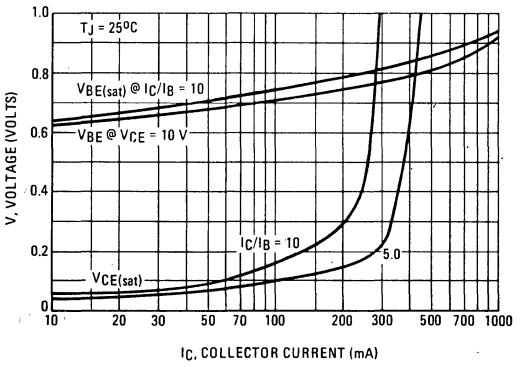
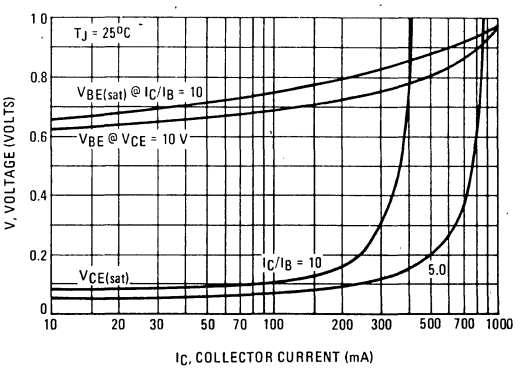


FIGURE 12 – "ON" VOLTAGE

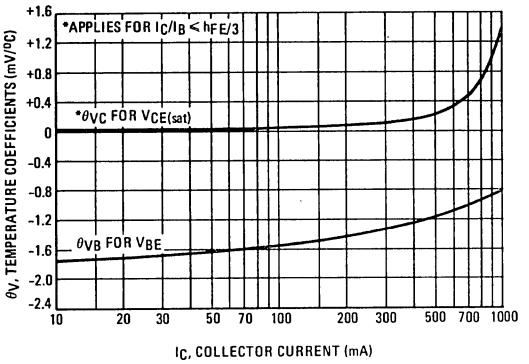




NPN
2N3738, 2N3739

PNP
2N6424, 2N6425

FIGURE 13 – TEMPERATURE COEFFICIENTS



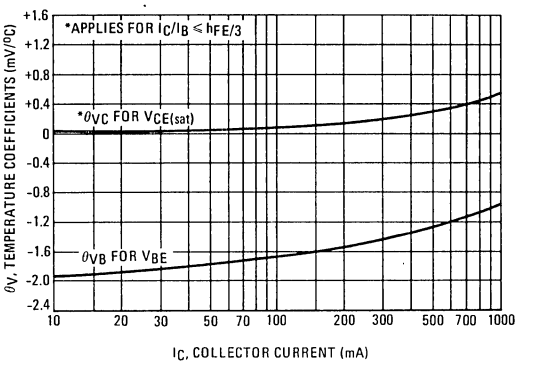
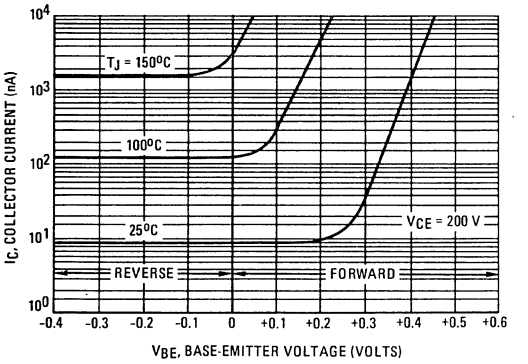


FIGURE 14 – COLLECTOR CUTOFF REGION



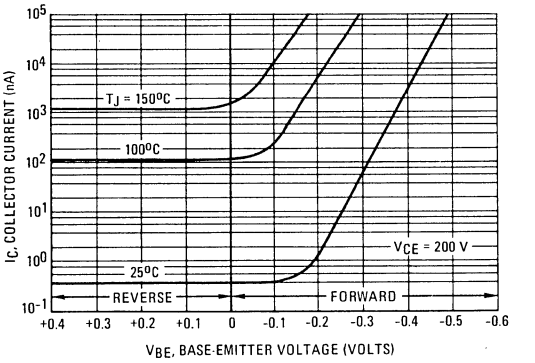
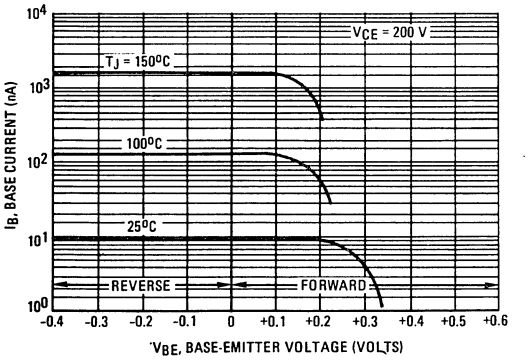
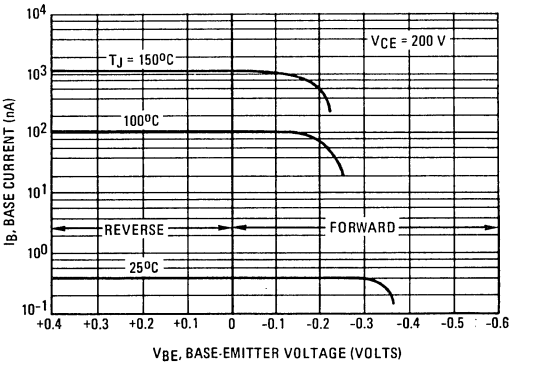


FIGURE 15 – BASE CUTOFF REGION





2N3740,A
2N3741,A

4

MEDIUM-POWER PNP TRANSISTORS

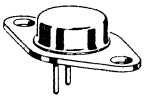
. . . ideal for use as drivers, switches and medium-power amplifier applications. These devices feature:

- Low Saturation Voltage – 0.6 $V_{CE(sat)}$ @ I_C = 1.0 Amp
- High Gain Characteristics – h_{FE}@ I_C = 250 mA: 30–100
- Excellent Safe Area Limits (See Figure 2)
- Low Collector Cutoff Current – 100 nA (Max) 2N3740A, 2N3741A
- Complementary to NPN 2N3766 (2N3740) and 2N3767 (2N3741)

POWER TRANSISTORS

PNP SILICON

60–80 VOLTS
25 WATTS

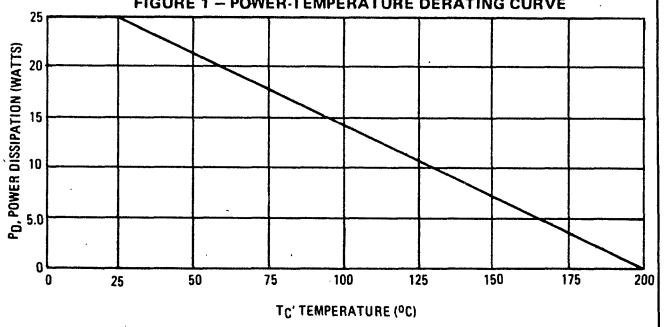


*MAXIMUM RATINGS

Rating	Symbol	2N3740 2N3740A	2N3741 2N3741A	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	7.0	7.0	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Collector Current – Continuous – Peak (Note 1)	I_C	4.0 10		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	25 0.143		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

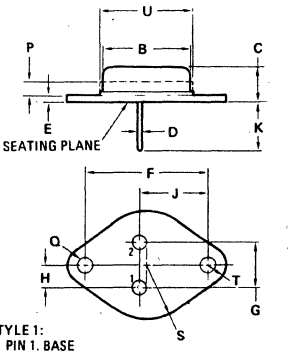
Note 1: See Figure 2

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 2.
Both limits are applicable and must be observed.

*Indicates JEDEC Registered Data.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
(TO-66)

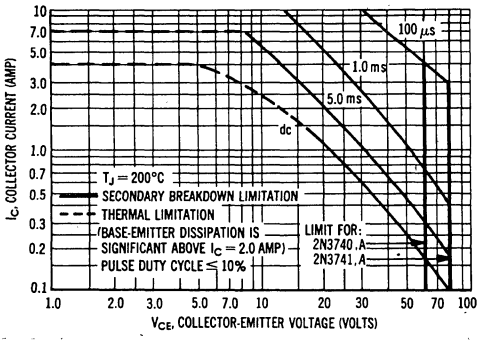
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Figure No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage ① (I_C = 100 mAdc, I_B = 0)	2N3740, 2N3740A	2	$V_{CEO(sus)}$ ①	60	–	Vdc
	2N3741, 2N3741A			80	–	
Emitter Base Cutoff Current (V_{EB} = 7.0 Vdc)	2N3740, 2N3741	–	I_{EBO}	–	0.5	mAdc
	2N3740A, 2N3741A			–	100	nAdc
Collector Cutoff Current		5, 6②	I_{CEX}			
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc	2N3740			–	100	μAdc
	2N3740A			–	100	nAdc
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N3741			–	100	μAdc
	2N3741A			–	100	nAdc
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3740			–	1.0	mAdc
	2N3740A			–	0.5	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C	2N3741			–	1.0	mAdc
	2N3741A			–	0.5	
Collector-Emitter Cutoff Current		5, 6②	I_{CEO}			
(V_{CE} = 40 Vdc, I_B = 0)	2N3740			–	1.0	mAdc
	2N3740A			–	1.0	μAdc
(V_{CE} = 60 Vdc, I_B = 0)	2N3741			–	1.0	mAdc
	2N3741A			–	1.0	μAdc
Collector Base Cutoff Current		–	I_{CBO}			
(V_{CB} = 60 Vdc, I_E = 0)	2N3740			–	100	μAdc
	2N3740A			–	100	nAdc
(V_{CB} = 80 Vdc, I_E = 0)	2N3741			–	100	μAdc
	2N3741A			–	100	nAdc
ON CHARACTERISTICS						
DC Current Gain		7	h_{FE}①			–
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)				40	–	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)				30	100	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)				20	–	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)				10	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 125 mAdc)		8, 9, 10	$V_{CE(sat)}$①	–	0.6	Vdc
Base-Emitter Voltage (I_C = 250 mAdc, V_{CE} = 1.0 Vdc)		3, 4, 9, 10	V_{BE}①	–	1.0	Vdc
TRANSIENT CHARACTERISTICS						
Current-Gain–Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		–	f_T	3.0 4.0†	– –	MHz
Common Base Output Capacitance (V_{CB} = 10 Vdc, I_C = 0, f = 100 kHz)		14	C_{ob}	–	100	pF
Small-Signal Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		–	h_{fe}	25	–	–

*Indicates JEDEC Registered Data.
†Motorola guarantees this value in addition to the JEDEC registered data shown.

① Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
② Figures 5 and 6 apply to 2N3740 and 2N3741 only.

FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

4

LARGE SIGNAL CHARACTERISTICS

FIGURE 3 – TRANSCONDUCTANCE

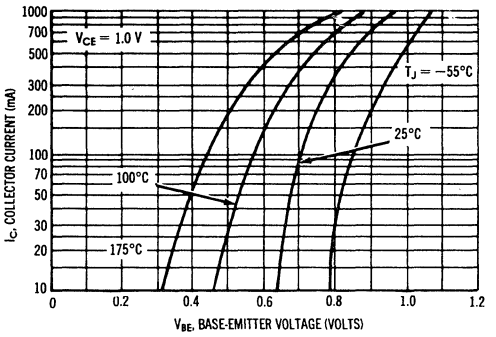
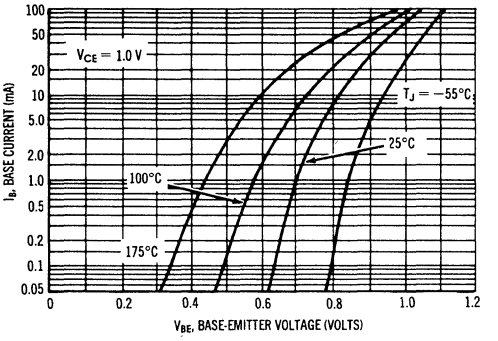


FIGURE 4 – INPUT ADMITTANCE



"OFF" REGION CHARACTERISTICS

FIGURE 5 – TRANSCONDUCTANCE

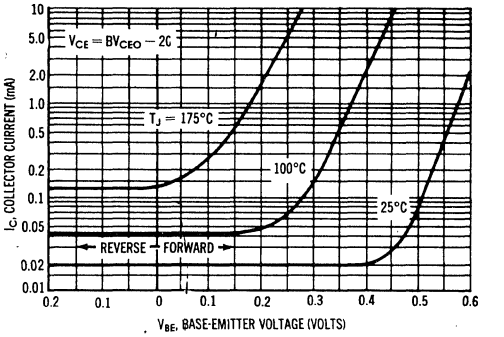
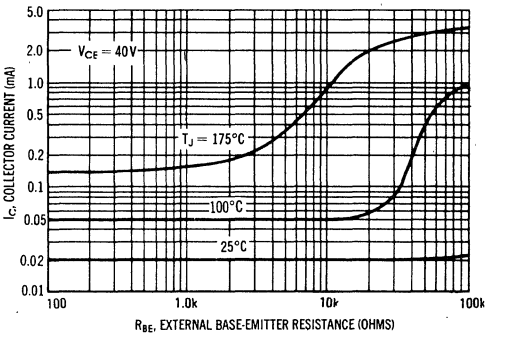


FIGURE 6 – EFFECTS OF BASE-EMITTER RESISTANCE



② Figures 5 and 6 apply to 2N3740 and 2N3741.

FIGURE 7 – THERMAL RESPONSE

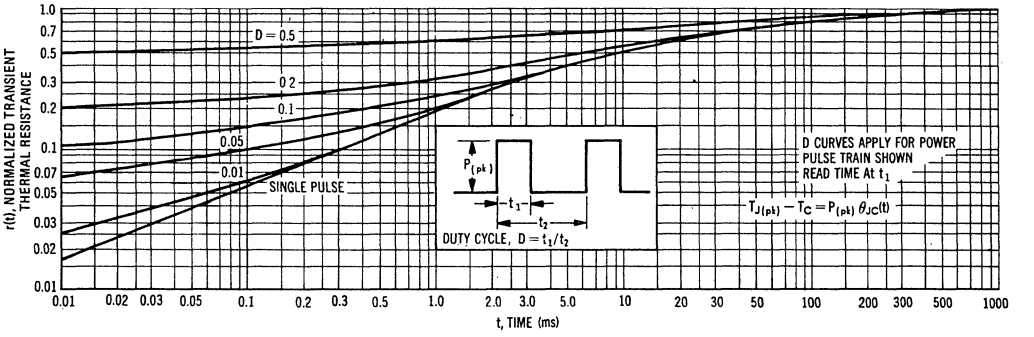
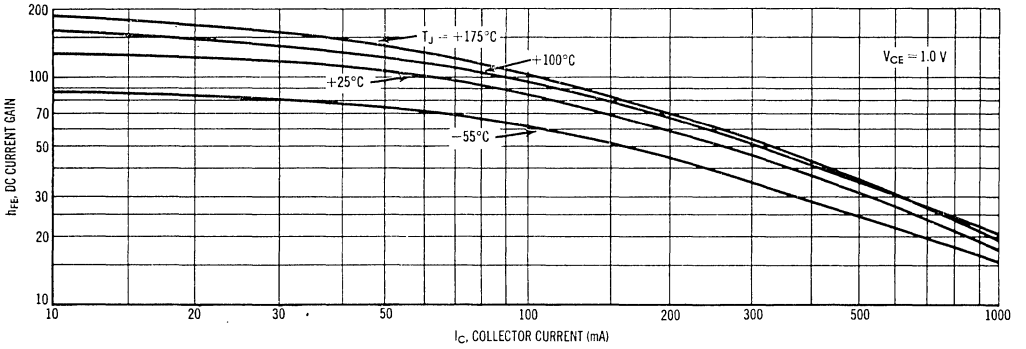


FIGURE 8 – CURRENT GAIN



4

SATURATION REGION CHARACTERISTICS

FIGURE 9 – COLLECTOR SATURATION REGION

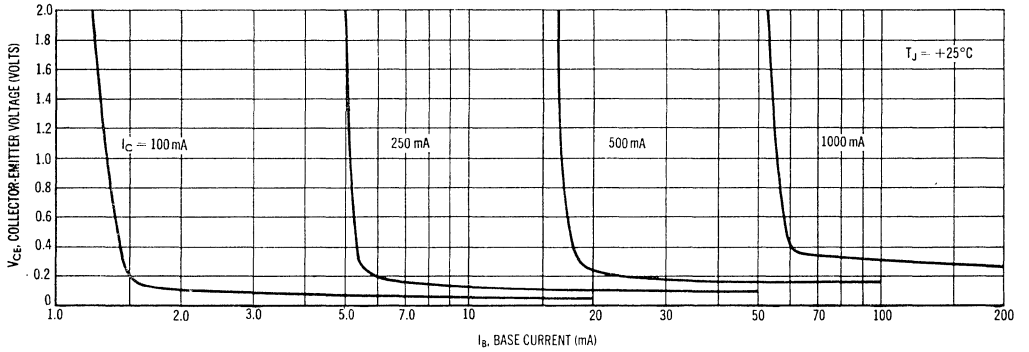


FIGURE 10 – "ON" VOLTAGES

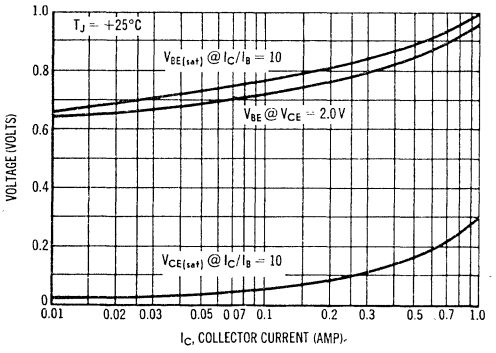


FIGURE 11 – TEMPERATURE COEFFICIENTS

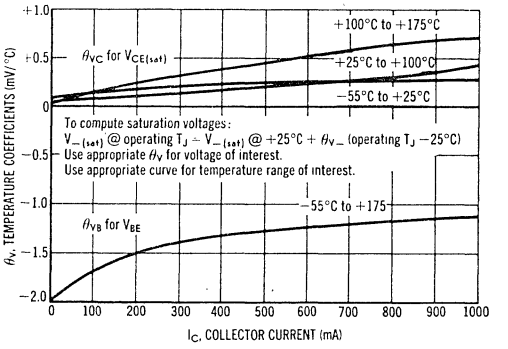


FIGURE 12 – TURN-ON TIME

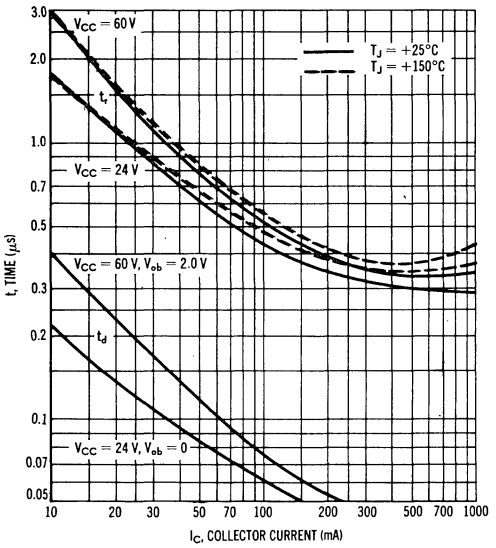


FIGURE 13 – CAPACITANCE

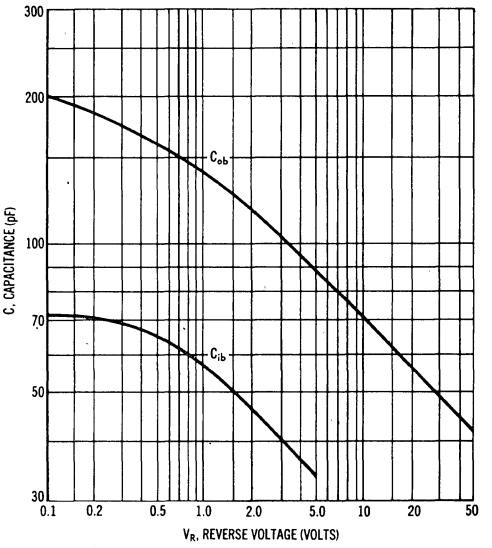


FIGURE 14 – STORAGE TIME

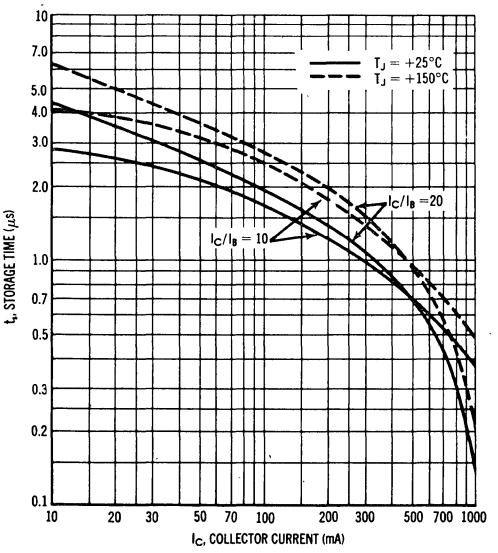
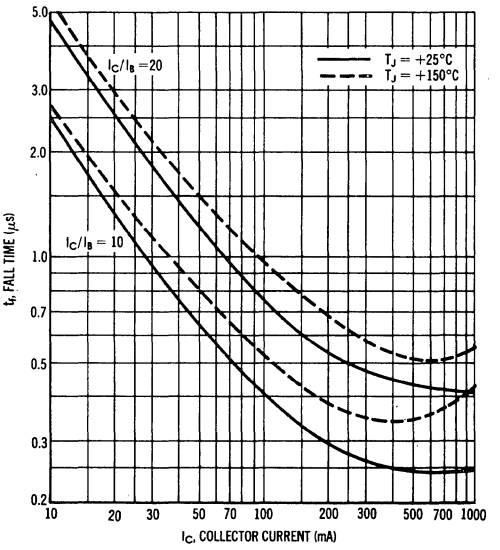


FIGURE 15 – FALL TIME



2N3766 (SILICON)
2N3767

MEDIUM-POWER NPN SILICON TRANSISTORS

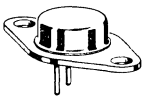
. . . for use in driver circuits, switching, and medium-power-amplifiers applications. These high performance devices feature:

- Low Saturation Voltage — 1.0 $V_{CE(sat)}$ @ I_C = 500 mA
- High Gain Characteristics — h_{FE} = 40-160 @ I_C = 500 mA
- Packaged in the Compact, High-Efficiency TO-66 Case
- Complementary to PNP 2N3740 (2N3766) and 2N3741 (2N3767)

4 AMPERE POWER TRANSISTORS

NPN SILICON
60-80 VOLTS
20 WATTS

4



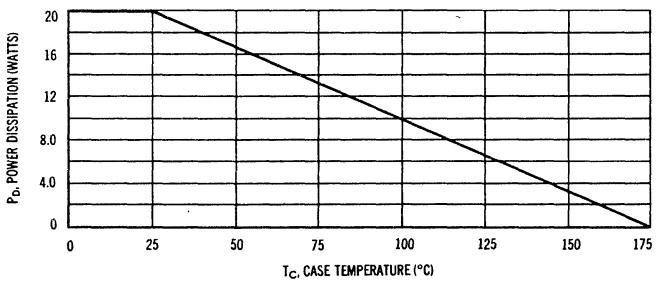
MAXIMUM RATINGS

Rating	Symbol	2N3766	2N3767	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current	I_C	4.0		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.133		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200		°C

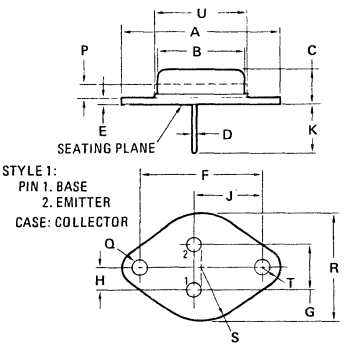
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	7.5	°C/W

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 2. Both limits are applicable and must be observed.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

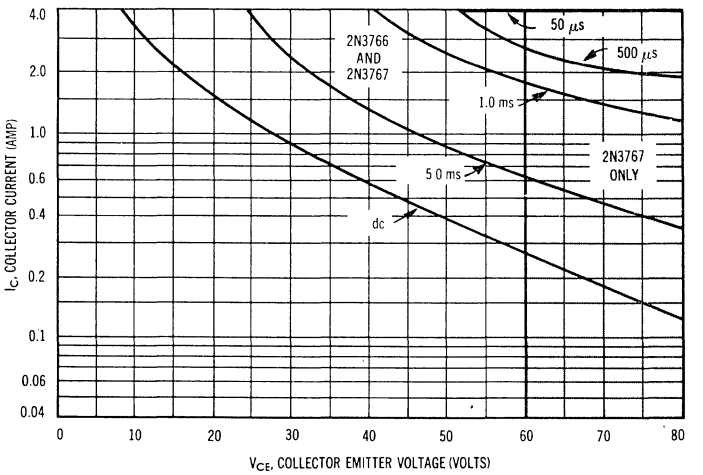
CASE 80-02
TO-66

ELECTRICAL CHARACTERISTICS (Tc = 25°C unless otherwise noted)

Characteristic		Figure No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Voltage (1) (I_C = 100 mAdc, I_B = 0)	2N3766	2	BV_{CEO}	60	—	Vdc
	2N3767			80	—	
Emitter-Base Cutoff Current (V_{EB} = 6.0 Vdc)		—	I_{EBO}	—	0.75	mAdc
Collector Cutoff Current		4, 6	I_{CEX}			mAdc
(V_{CE} = 80 Vdc, V_{BE} = 1.5 Vdc)	2N3766			—	0.1	
(V_{CE} = 100 Vdc, V_{BE} = 1.5 Vdc)	2N3767			—	0.1	
(V_{CE} = 50 Vdc, V_{BE} = 1.5 Vdc, T_C = 150°C)	2N3766			—	1.0	
(V_{CE} = 70 Vdc, V_{BE} = 1.5 Vdc, T_C = 150°C)	2N3767			—	1.0	
Collector-Emitter Cutoff Current		6	I_{CEO}			mAdc
(V_{CE} = 60 Vdc, I_B = 0)	2N3766			—	0.7	
(V_{CE} = 80 Vdc, I_B = 0)	2N3767			—	0.7	
Collector-Base Cutoff Current		4	I_{CBO}			mAdc
(V_{CB} = 80 Vdc, I_E = 0)	2N3766			—	0.1	
(V_{CB} = 100 Vdc, I_E = 0)	2N3767			—	0.1	
ON CHARACTERISTICS						
DC Current Gain		7	h_{FE}			—
(I_C = 50 mAdc, V_{CE} = 5.0 Vdc)				30	—	
(I_C = 500 mAdc, V_{CE} = 5.0 Vdc)				40	160	
(I_C = 1.0 Adc, V_{CE} = 10 Vdc)				20	—	
Collector-Emitter Saturation Voltage		8,9	$V_{CE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)				—	2.5	
(I_C = 500 mAdc, I_B = 50 mAdc)				—	1.0	
Base-Emitter Voltage (I_C = 1.0 Adc, V_{CE} = 10 Vdc)		3, 5, 9	V_{BE}	—	1.5	Vdc
TRANSIENT CHARACTERISTICS						
Current-Gain - Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		—	f_T	10	—	MHz
Common-Base Output Capacitance (V_{CB} = 10 Vdc, I_C = 0 Adc, f = 100 kHz)		13	C_{ob}	—	50	pF
Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		—	h_{fe}	40	—	—

(1) Pulse Test: Pulse Width ≤300μs, Duty Cycle ≤2.0%.

FIGURE 2 – ACTIVE REGION SAFE AREAS



The Safe Operating Area Curves indicate I_C-V_{CE} limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector-emitter short. (Case temperature and duty cycle of the excursions make no significant change in these safe areas.) The load line may exceed the BV_{CEO} voltage limit only if the collector current has been reduced to 20 mA or less before or at the BV_{CES} limit; then and only then may the load line be extended to the absolute maximum voltage rating of BV_{CBO}. To insure operation below the maximum T_J, the power-temperature derating curve must be observed for both steady state and pulse power conditions.

LARGE SIGNAL CHARACTERISTICS

FIGURE 3 – TRANSCONDUCTANCE

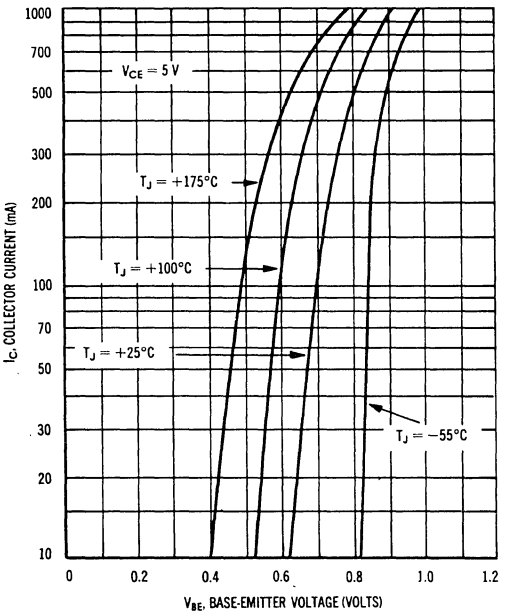
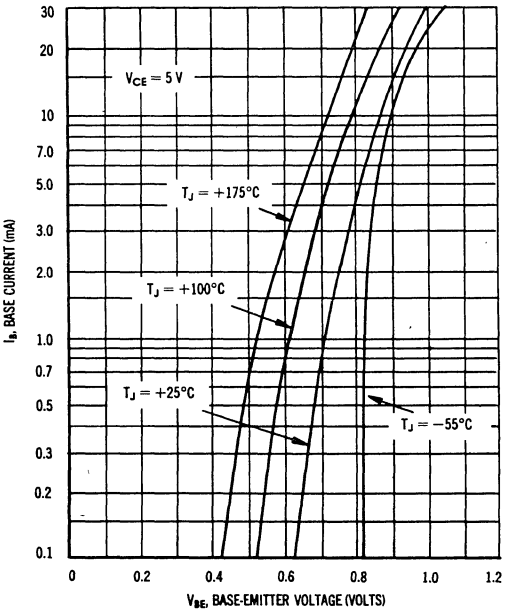


FIGURE 5 – INPUT ADMITTANCE



CUT-OFF CHARACTERISTICS

FIGURE 4 – TRANSCONDUCTANCE

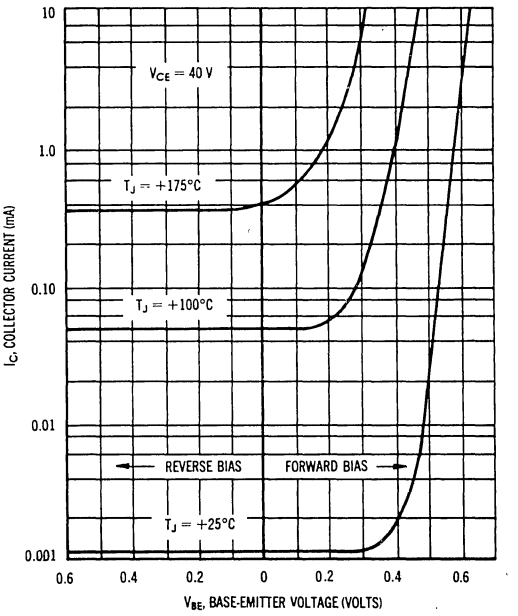


FIGURE 6 – EFFECT OF BASE-EMITTER RESISTANCE

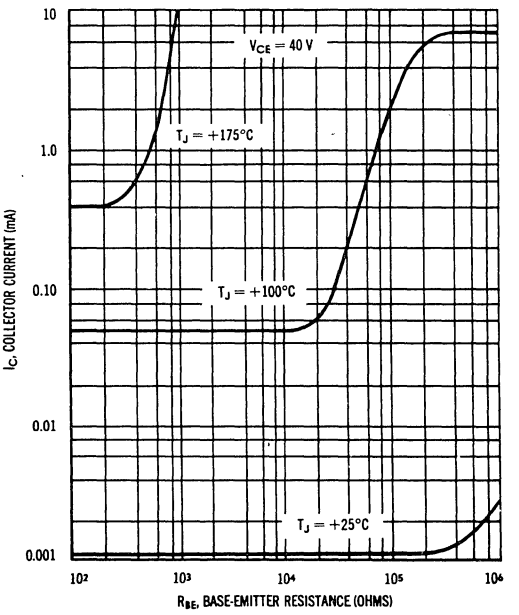


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FIGURE 7 – CURRENT GAIN

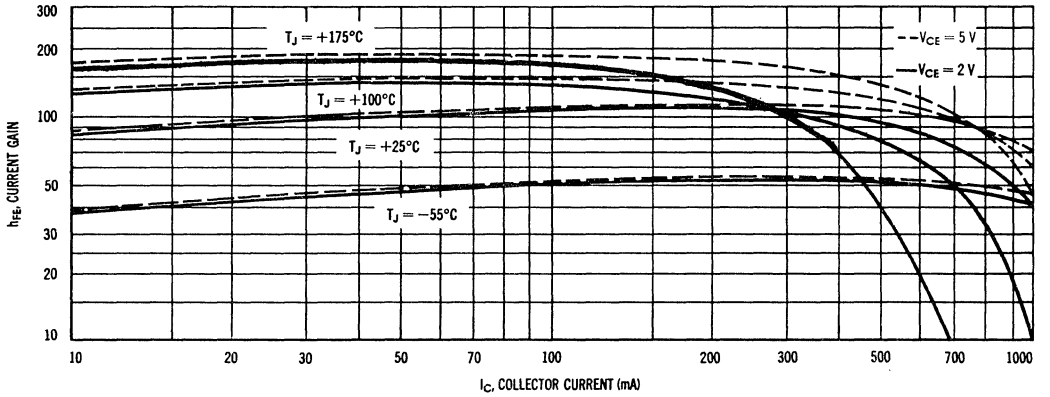

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FIGURE 8 – COLLECTOR SATURATION REGION

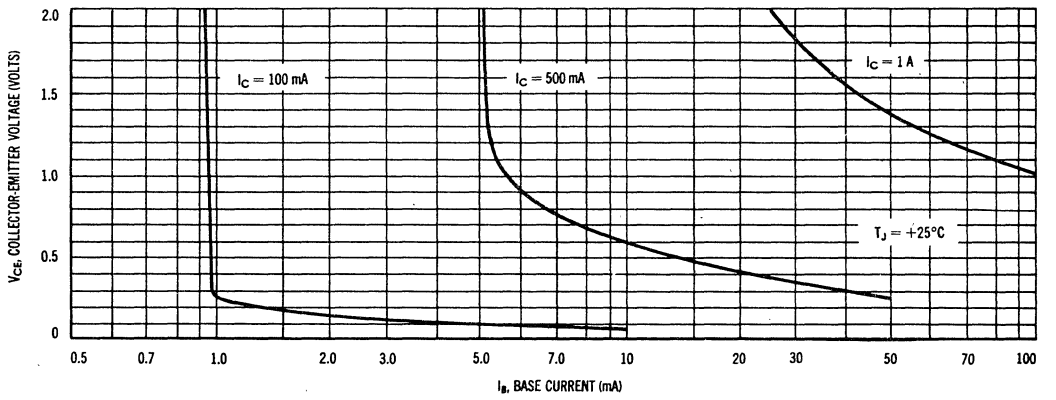


FIGURE 9 – "ON" VOLTAGES

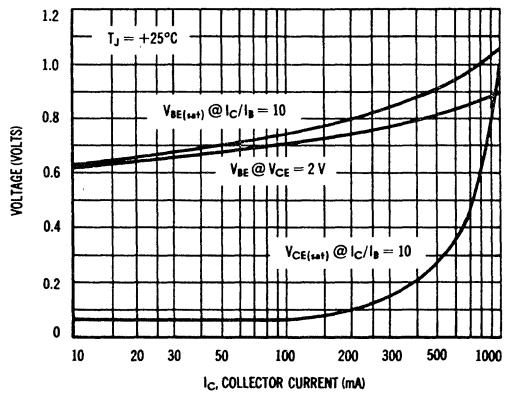
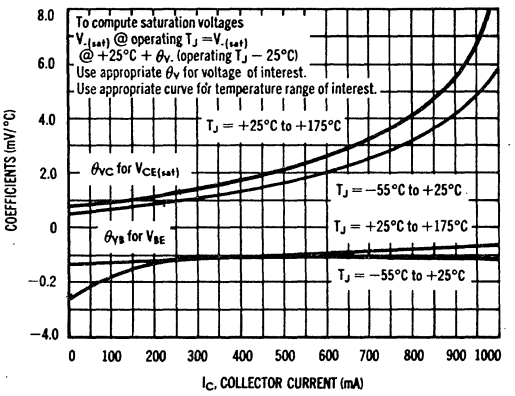


FIGURE 10 – TEMPERATURE COEFFICIENTS



TRANSIENT CHARACTERISTICS

(T_J = 25°C)

FIGURE 11 – TURN-ON TIME

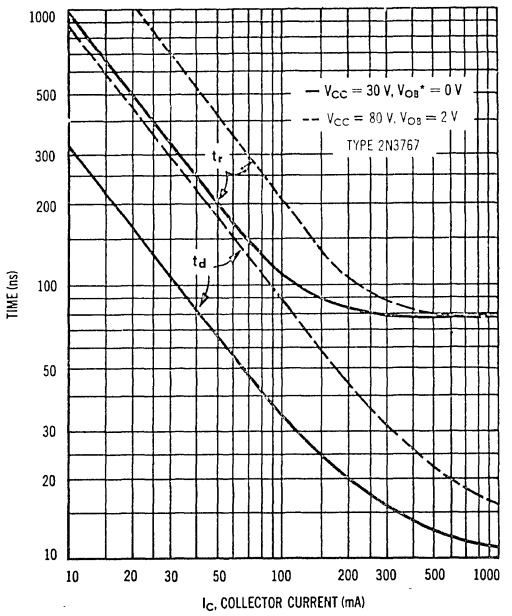


FIGURE 12 – TURN-OFF TIME

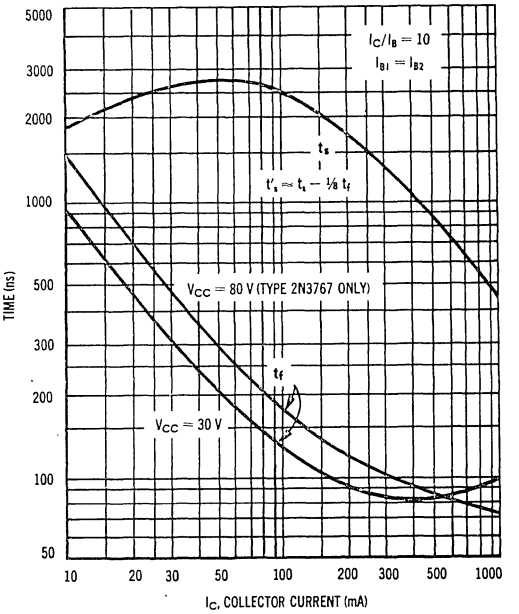


FIGURE 13 – CAPACITANCE

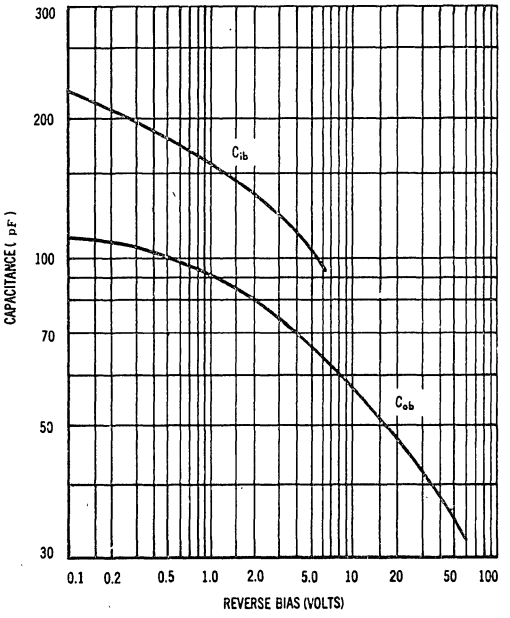
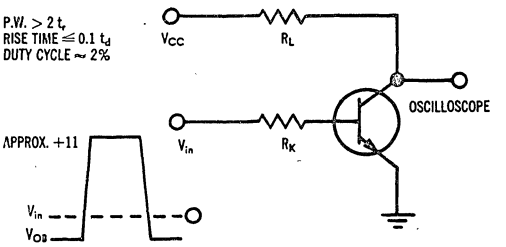
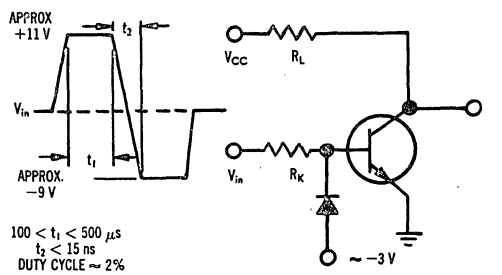


FIGURE 14 – EQUIVALENT CIRCUIT FOR MEASURING DELAY AND RISE TIME



*V_{OB} = BASE-EMITTER "OFF" BIAS VOLTAGE

FIGURE 15 – EQUIVALENT CIRCUIT FOR MEASURING STORAGE AND FALL TIMES



2N3771 2N3772
2N6257

HIGH POWER NPN SILICON POWER TRANSISTORS

. . . designed for linear amplifiers, series pass regulators, and inductive switching applications.

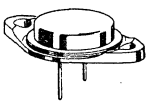
- Forward Biased Second Breakdown Current Capability

  $I_{S/b}$ = 3.75 Adc @ V_{CE} = 40 Vdc – 2N3771
  = 2.5 Adc @ V_{CE} = 60 Vdc – 2N3772
  = 3.75 Adc @ V_{CE} = 40 Vdc – 2N6257

20 and 30 AMPERE

POWER TRANSISTORS
NPN SILICON

40 and 60 VOLTS
150 WATTS



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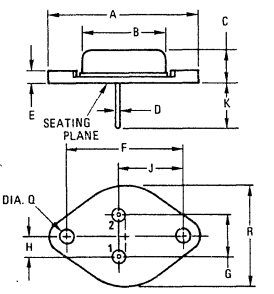
*MAXIMUM RATINGS

Rating	Symbol	2N3771	2N3772	2N6257	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	40	Vdc
Collector-Emitter Voltage	V_{CEX}	50	80	50	Vdc
Collector-Base Voltage	V_{CB}	50	100	50	Vdc
Emitter-Base Voltage	V_{EB}	5.0	7.0	5.0	Vdc
Collector Current – Continuous Peak	I_C	15 30	10 30	20 30	Adc
Base Current – Continuous Peak	I_B	7.5 15	5.0 15	5.0 15	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.855			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	2N3771, 2N3772, 2N6257	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

*Indicates JEDEC Registered Data



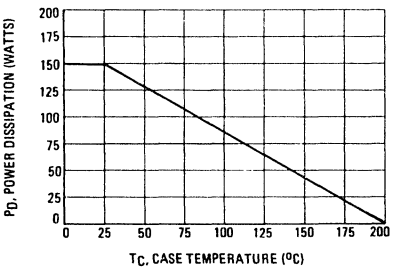
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.

CASE 11-01

FIGURE 1 – POWER DERATING



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
*Collector-Emitter Sustaining Voltage (1)	2N3771	$V_{CEO(sus)}$	40	–	Vdc
(I_C = 0.2 Adc, I_B = 0)	2N3772		60	–	
	2N6257		40	–	
Collector-Emitter Sustaining Voltage	2N3771	$V_{CEX(sus)}$	50	–	Vdc
(I_C = 0.2 Adc, $V_{EB(off)}$ = 1.5 Vdc, R_{BE} = 100 Ohms)	2N3772		80	–	
	2N6257		50	–	
Collector-Emitter Sustaining Voltage	2N3771	$V_{CER(sus)}$	45	–	Vdc
(I_C = 0.2 Adc, R_{BE} = 100 Ohms)	2N3772		70	–	
	2N6257		45	–	
*Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N3771		–	10	
(V_{CE} = 50 Vdc, I_B = 0)	2N3772		–	10	
(V_{CE} = 25 Vdc, I_B = 0)	2N6527		–	10	
*Collector Cutoff Current		I_{CEV}			mAdc
(V_{CE} = 50 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N3771		–	2.0	
(V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N3772		–	5.0	
(V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6257		–	4.0	
(V_{CE} = 30 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3771		–	10	
	2N3772		–	10	
(V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6527		–	20	
*Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 50 Vdc, I_E = 0)	2N3771		–	2.0	
	2N6257		–	4.0	
(V_{CB} = 100 Vdc, I_E = 0)	2N3772		–	5.0	
*Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)	2N3771		–	5.0	
	2N6257		–	10	
(V_{BE} = 7.0 Vdc, I_C = 0)	2N3772		–	5.0	
***ON CHARACTERISTICS**					
DC Current Gain (1)		h_{FE}			–
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)	2N3771		15	60	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)	2N3772		15	60	
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)	2N6257		5.0	–	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N3771		5.0	–	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)	2N3772		5.0	–	
	2N6257		5.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 15 Adc, I_B = 1.5 Adc)	2N3771		–	2.0	
(I_C = 10 Adc, I_B = 1.0 Adc)	2N3772		–	1.4	
(I_C = 8.0 Adc, I_B = 0.8 Adc)	2N6257		–	1.5	
(I_C = 30 Adc, I_B = 6.0 Adc)	2N3771		–	4.0	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N3772		–	4.0	
	2N6257		–	4.0	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)	2N3771		–	2.7	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)	2N3772		–	2.2	
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)	2N6257		–	2.2	
***DYNAMIC CHARACTERISTICS**					
Current-Gain–Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 50 kHz)		f_T	0.2	–	MHz
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	40	–	–
SECOND BREAKDOWN					
Second Breakdown Energy with Base Forward Biased, t = 1.0 s (non-repetitive)		$I_{S/b}$			Adc
(V_{CE} = 40 Vdc)	2N3771		3.75	–	
	2N6257		3.75	–	
(V_{CE} = 60 Vdc)	2N3772		2.5	–	

*Indicates JEDEC Registered Data

(1) Pulse Test: 300 μs, Rep. Rate 60 cps.

FIGURE 2 – THERMAL RESPONSE – 2N3771, 2N3772, 2N6257

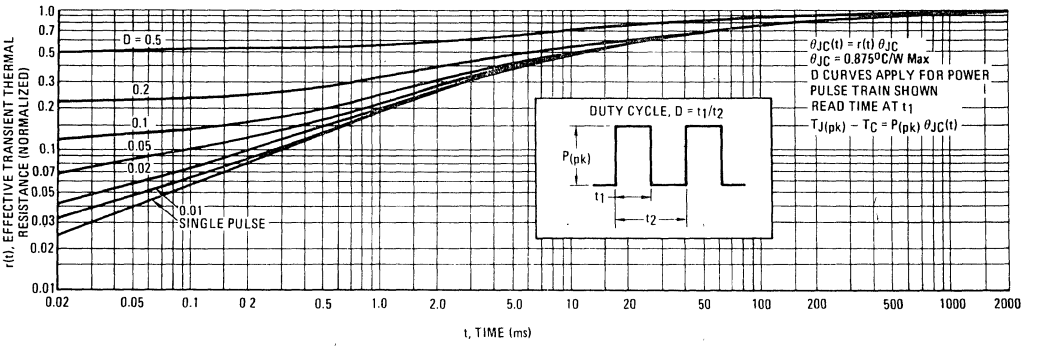


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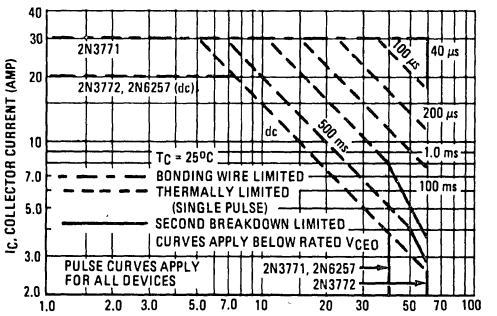
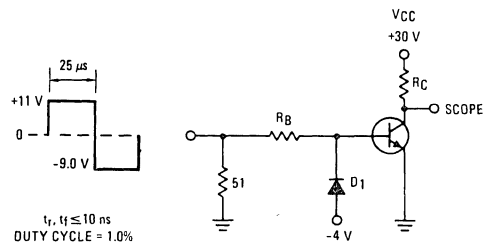
FIGURE 3 – ACTIVE-REGION SAFE OPERATING AREA – 2N3771, 2N3772, 2N6257



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Figure 3 is based upon JEDEC registered Data. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data of Figure 2. Using data of Figure 2 and the pulse power limits of Figure 3, $T_{J(pk)}$ will be found to be less than $T_{J(max)}$ for pulse widths of 1 ms and less. When using Motorola transistors, it is permissible to increase the pulse power limits until limited by $T_{J(max)}$.

FIGURE 4 – SWITCHING TIME TEST CIRCUIT



RB AND RC ARE VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE IB ≈100 mA
MSD6100 USED BELOW IB ≈100 mA

FIGURE 5 – TURN-ON TIME

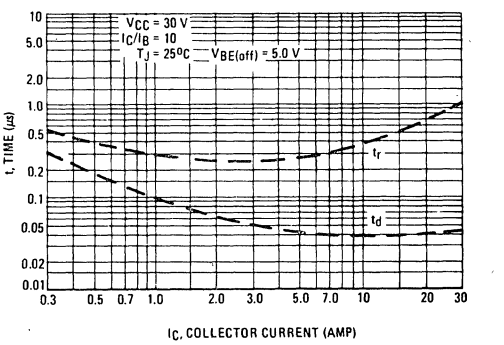


FIGURE 6 – TURN-OFF TIME

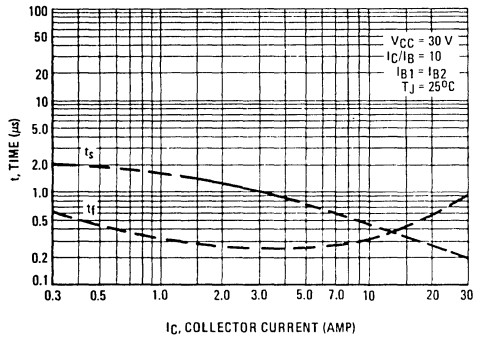


FIGURE 7 – CAPACITANCE

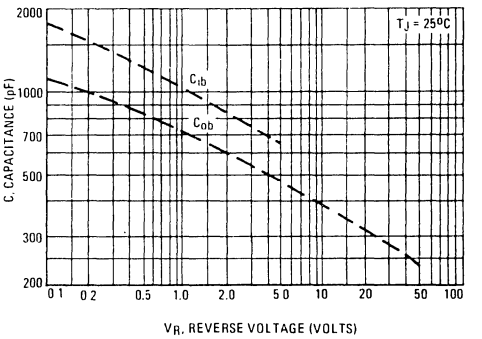


FIGURE 8 – DC CURRENT GAIN

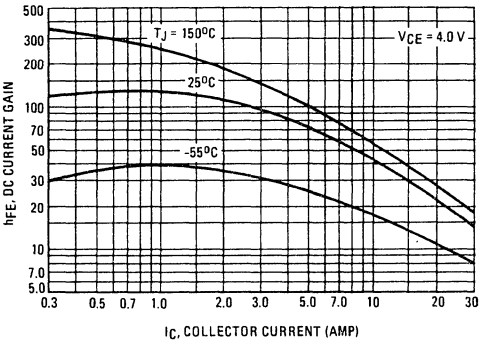
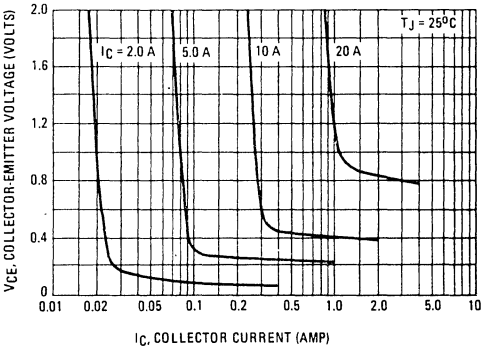


FIGURE 9 – COLLECTOR SATURATION REGION



4

FIGURE 10 – "ON" VOLTAGES

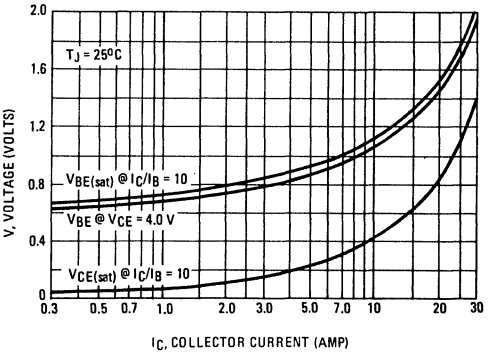


FIGURE 11 – TEMPERATURE COEFFICIENTS

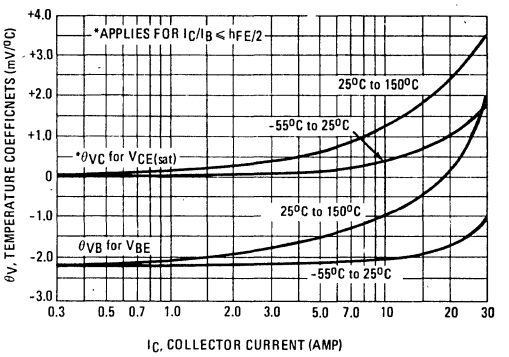
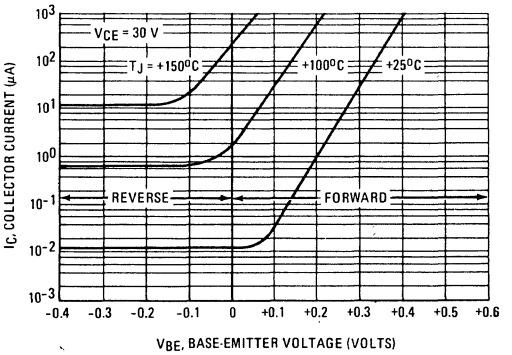


FIGURE 12 – COLLECTOR CUTOFF REGION



NPN PNP

2N3773 2N6609

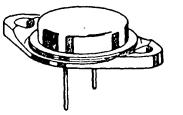
COMPLEMENTARY SILICON POWER TRANSISTORS

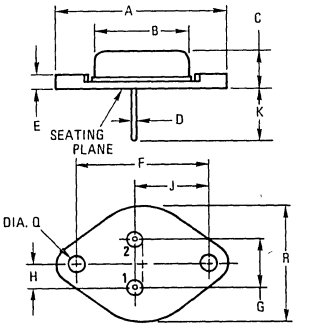
The 2N3773 and 2N6609 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc to dc converters or inverters.

- High Safe Operating Area (100% Tested)
  150 W @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage
  h_{fe} = 15 (Min) @ 8 A, 4 V
  $V_{CE(sat)}$ = 1.4 V (Max) @ I_C = 8 A, I_B = 0.8 A
- For Low Distortion Complementary Designs

16 AMPERE COMPLEMENTARY POWER TRANSISTORS

140 VOLTS
150 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector Emitter Voltage	V_{CEO}	140	Vdc
Collector-Emitter Voltage	V_{CEX}	160	Vdc
Collector-Base Voltage	V_{CBO}	160	Vdc
Emitter-Base Voltage	V_{EBO}	7	Vdc
Collector Current – Continuous – Peak (1)	I_C	16 30	Adc
Base Current – Continuous – Peak (1)	I_B	4 15	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.855	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5ms, Duty Cycle ≤ 10%.

PowerBase is a trademark of Motorola.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

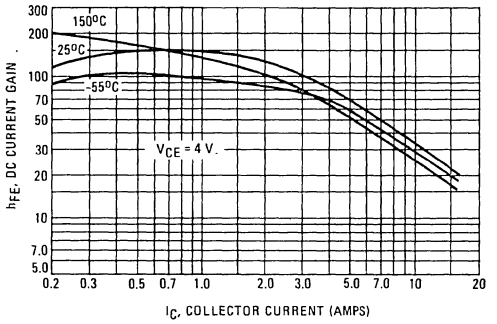
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)				
*Collector-Emitter Breakdown Voltage (I_C = 0.2 Adc, I_B = 0)	$V_{CEO(sus)}$	140	–	Vdc
*Collector-Emitter Sustaining Voltage (I_C = 0.1 Adc, $V_{BE(off)}$ = 1.5 Vdc, R_{BE} = 100 Ohms)	$V_{CEX(sus)}$	160	–	Vdc
Collector-Emitter Sustaining Voltage (I_C = 0.2 Adc, R_{BE} = 100 Ohms)	$V_{CER(sus)}$	150	–	Vdc
*Collector Cutoff Current (V_{CE} = 120 Vdc, I_B = 0)	I_{CEO}	–	10	mAdc
*Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	2 10	mAdc
Collector Cutoff Current (V_{CB} = 140 Vdc, I_E = 0)	I_{CBO}	–	2	mAdc
*Emitter Cutoff Current (V_{BE} = 7 Vdc, I_C = 0)	I_{EBO}	–	5	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain *(I_C = 8 Adc, V_{CE} = 4 Vdc) (I_C = 16 Adc, V_{CE} = 4 Vdc)	h_{FE}	 15 5	 60	–
Collector-Emitter Saturation Voltage *(I_C = 8 Adc, I_B = 800 mAdc) (I_C = 16 Adc, I_B = 3.2 Adc)	$V_{CE(sat)}$	 – –	 1.4 4	Vdc
*Base-Emitter On Voltage (I_C = 8 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	–	2.2	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common-Emitter Small-Signal, Short-Circuit, Forward Current Transfer Ratio (I_C = 1 A, f = 50 kHz)	$\|h_{fe}\|$	4	–	–
*Small-Signal Current Gain (I_C = 1 Adc, V_{CE} = 4 Vdc, f = 1 kHz)	h_{fe}	40	–	–
SECOND BREAKDOWN CHARACTERISTICS				
Second Breakdown Collector Current with Base Forward Biased t = 1 s (non-repetitive), V_{CE} = 100 V, See Figure 12	$I_{S/b}$	1.5	–	Adc

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

*Indicates JEDEC Registered Data

NPN

FIGURE 1 – DC CURRENT GAIN



PNP

FIGURE 2 – DC CURRENT GAIN

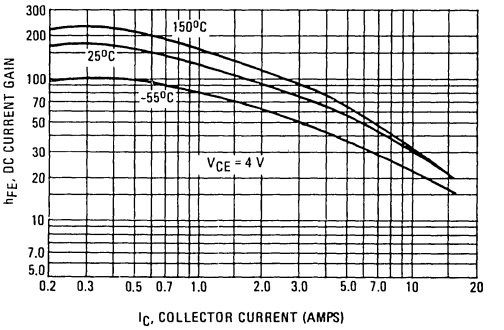


FIGURE 3 – COLLECTOR SATURATION REGION

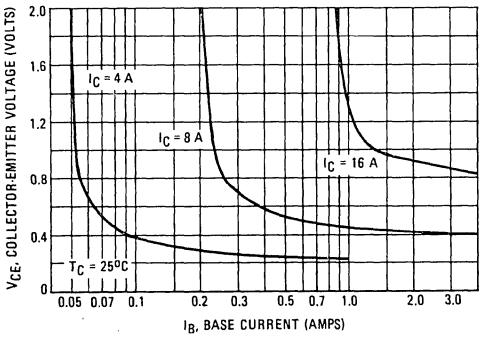


FIGURE 4 – COLLECTOR SATURATION REGION

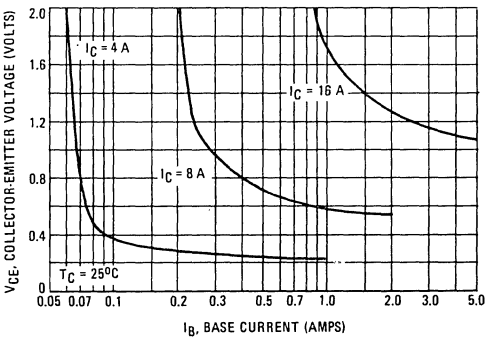


FIGURE 5 – "ON" VOLTAGE

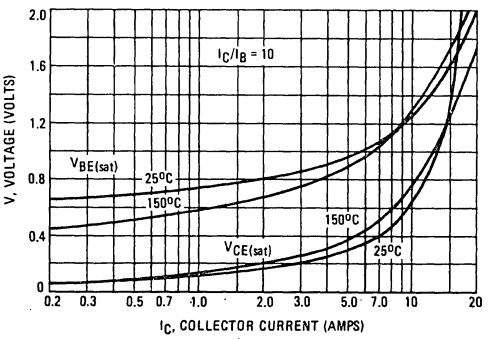


FIGURE 6 – "ON" VOLTAGE

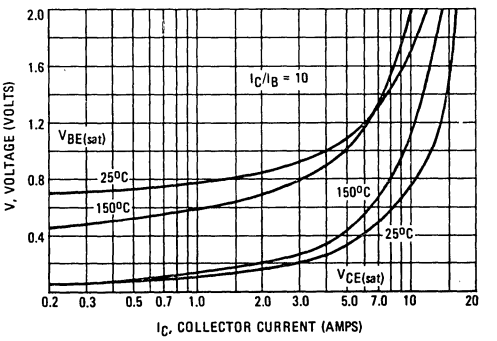


FIGURE 7 – TURN-ON SWITCHING TIMES – 2N3773, 2N6609

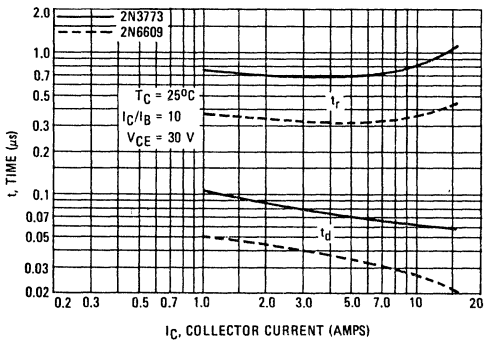


FIGURE 8 – TURN-OFF SWITCHING TIMES – 2N3773, 2N6609

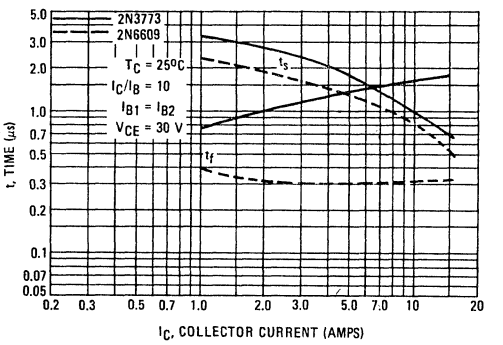


FIGURE 9 – CURRENT-GAIN – BANDWIDTH PRODUCT – 2N3773, 2N6609

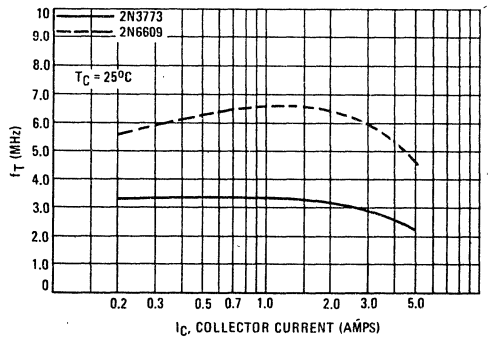


FIGURE 10 – CAPACITANCES – 2N3773, 2N6609

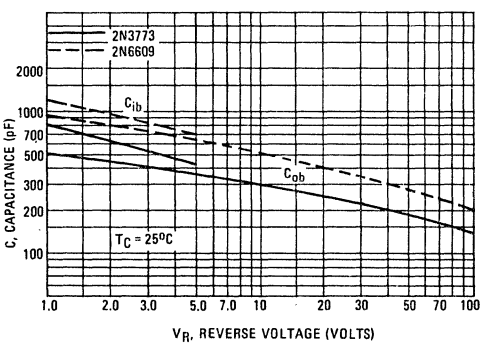


FIGURE 11 – THERMAL RESPONSE – 2N3773, 2N6609

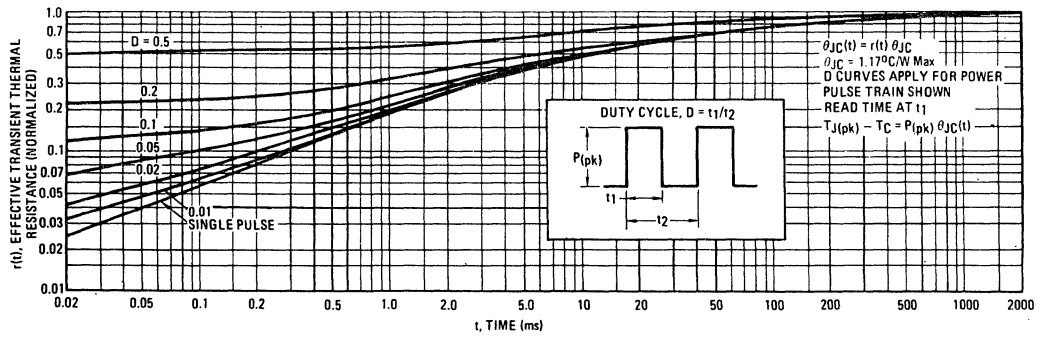
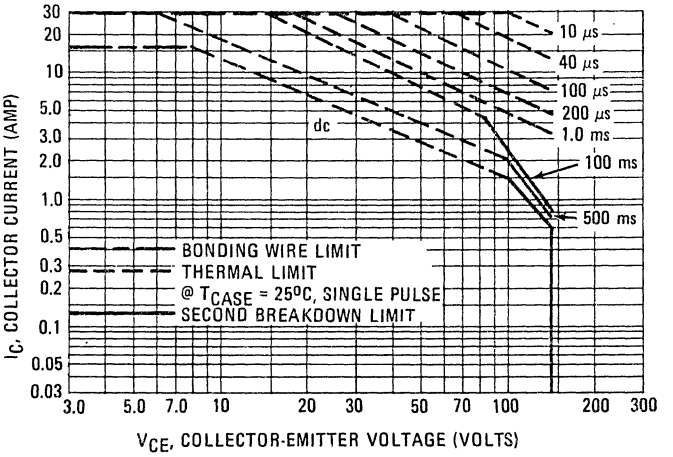


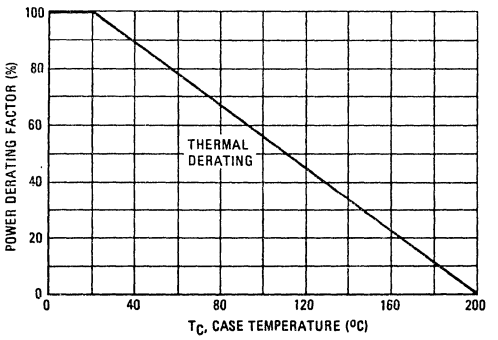
FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^oC$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 13 – POWER DERATING



4

SILICON PNP POWER TRANSISTORS

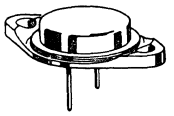
. . . designed for medium-speed switching and amplifier applications. These devices feature:

- Total Switching Time @ 3 A ≈ 1 μs (typ)
- Two Gain Ranges:
  h_{FE} (min) = 15 and 30 @ 3 A (2N3789, 2N3790)
  25 and 50 @ 1 A (2N3791, 2N3792)
- Low $V_{CE(sat)}$ = 0.5 V (typ) @ I_C = 4.0 A, I_B = 0.4 A
- Excellent Safe Area Limits
- Complementary NPN types available — 2N3713 thru 2N3716

10 AMPERE

POWER TRANSISTORS PNP SILICON

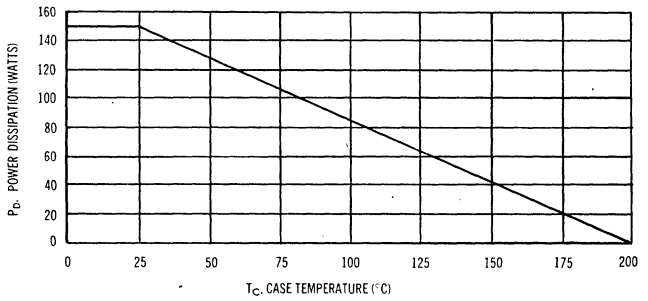
60-80 VOLTS
150 WATTS



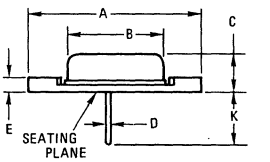
MAXIMUM RATINGS

Characteristic	Symbol	2N3789 2N3791	2N3790 2N3792	Unit
Collector-Base Voltage	V_{CB}	60	80	Volts
Collector-Emitter Voltage	V_{CEO}	60	80	Volts
Emitter-Base Voltage	V_{EB}	7.0	7.0	Volts
Collector Current (Continuous)	I_C	10	10	Amps
Base Current (Continuous)	I_B	4.0	4.0	Amps
Power Dissipation	P_D	150	150	Watts
Thermal Resitance	θ_{JC}	1.17	1.17	°C/W
Junction Operating and Storage Temperature Range	T_J, T_{stg}	-65 to +200		°C

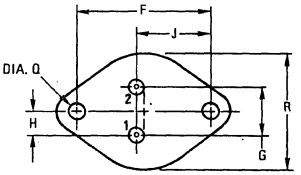
FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Limits are indicated by Figures 15, 16. Both limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

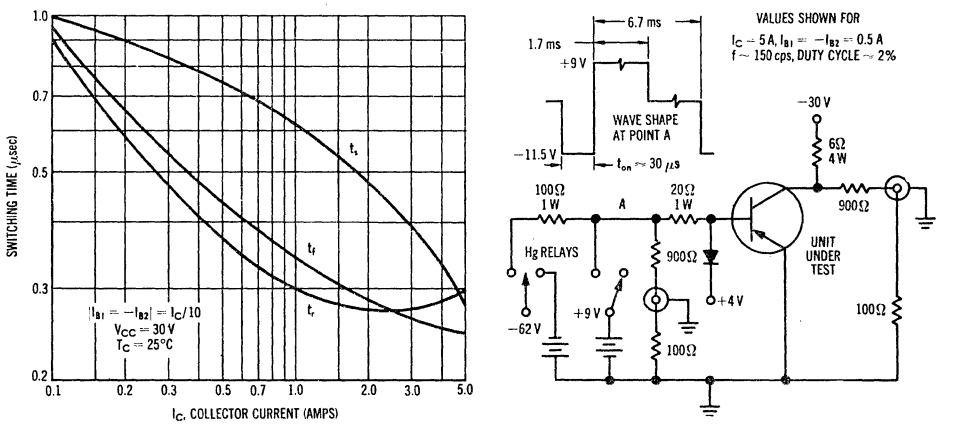
Collector connected to case.
CASE 11-01
(TO-3)

ELECTRICAL CHARACTERISTICS (Tc = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Collector-Emitter Sustaining Voltage* (I_C = 200 mAdc, I_B = 0)	2N3789, 2N3791 2N3790, 2N3792	$V_{CEO(sus)}$*	60 80	— —	Vdc
Collector-Emitter Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, V_{BE} = -1.5 Vdc)	2N3789, 2N3791		—	1	
(V_{CE} = 80 Vdc, V_{BE} = -1.5 Vdc)	2N3790, 2N3792		—	1	
(V_{CE} = 60 Vdc, V_{BE} = -1.5 Vdc, T_C = 150°C)	2N3789, 2N3791		—	5	
(V_{CE} = 80 Vdc, V_{BE} = -1 5 Vdc, T_C = 150°C)	2N3790, 2N3792		—	5	
Emitter-Base Cutoff Current (V_{EB} = 7 Vdc)	All Types	I_{EBO}	—	5	mAdc
DC Current Gain*		h_{FE}*			—
(I_C = 1 Adc, V_{CE} = 2 Vdc)	2N3789, 2N3790 2N3791, 2N3792		25 50	90 150	
(I_C = 3 Adc, V_{CE} = 2 Vdc)	2N3789, 2N3790 2N3791, 2N3792		15 30	— —	
Collector-Emitter Saturation Voltage*		$V_{CE(sat)}$*			Vdc
(I_C = 4 Adc, I_B = 0.4 Adc)	2N3789, 2N3790		—	1.0	
(I_C = 5 Adc, I_B = 0.5 Adc)	2N3791, 2N3792		—	1.0	
Base-Emitter Saturation Voltage*		$V_{BE(sat)}$*			Vdc
(I_C = 4 Adc, I_B = 0.4 Adc)	2N3789, 2N3790		—	2.0	
(I_C = 5 Adc, I_B = 0.5 Adc)	2N3791, 2N3792		—	1.5	
Current Gain — Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.5 Adc, f = 1 mc)	All Types	f_T	4	—	mc

*Sweep Test: 1/2 sine wave cycle @ 60 cps.

FIGURE 2 – TYPICAL SWITCHING TIMES AND TEST CIRCUIT



4

LARGE SIGNAL CHARACTERISTICS – TYPE 2N3789, 2N3790

(PULSE TEST: pulse width ≈ 200 μsec, duty cycle ≈ 1%)

FIGURE 3 – TRANSCONDUCTANCE

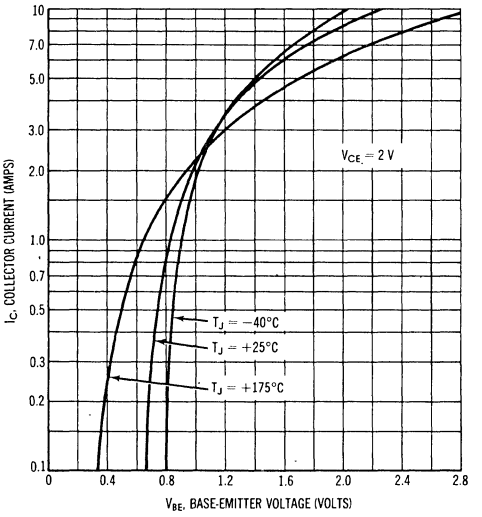


FIGURE 5 – CURRENT GAIN

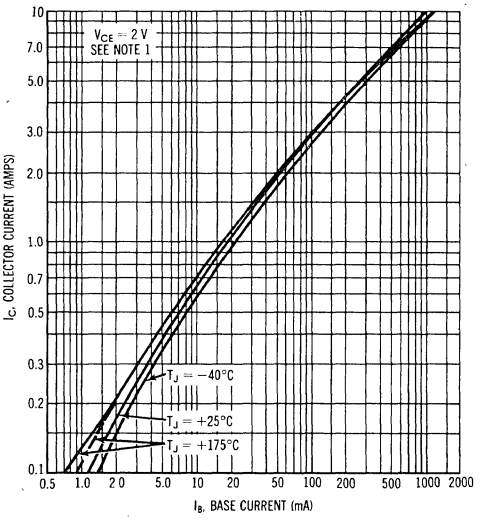


FIGURE 4 – INPUT ADMITTANCE

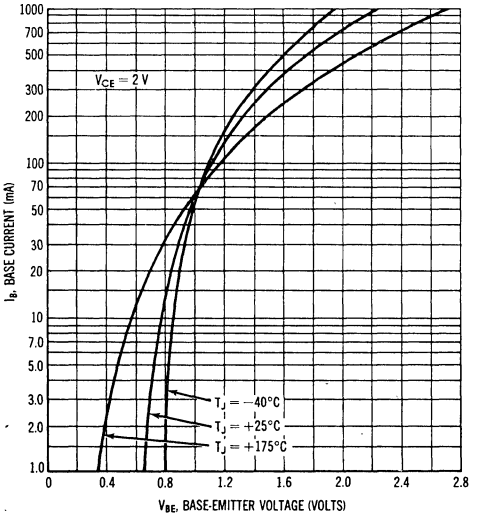
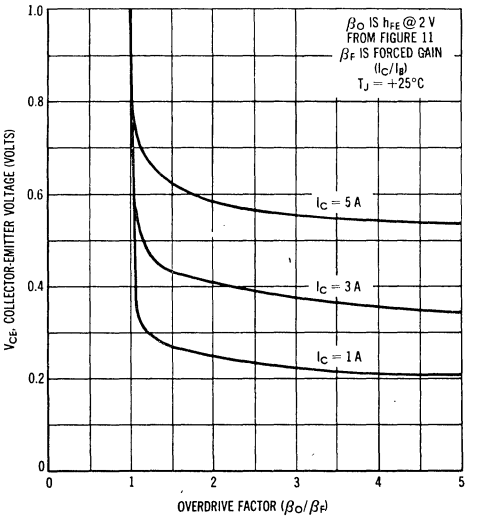


FIGURE 6 – SATURATION REGION



NOTE 1. Dashed line indicates metered base current minus I_{CBO} of the transistor at 175°C.

LARGE SIGNAL CHARACTERISTICS – TYPE 2N3791, 2N3792

(PULSE TEST: pulse width ≈ 200 μsec, dutv cycle ≈ 1%)

FIGURE 7 – TRANSCONDUCTANCE

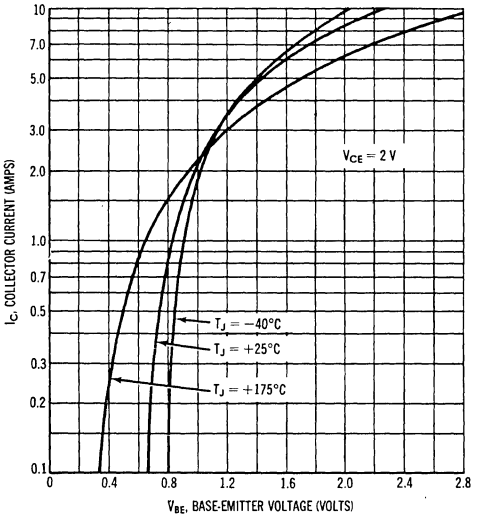


FIGURE 9 – CURRENT GAIN

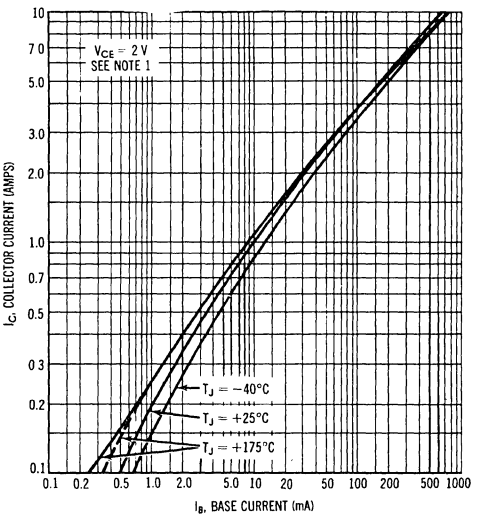


FIGURE 8 – INPUT ADMITTANCE

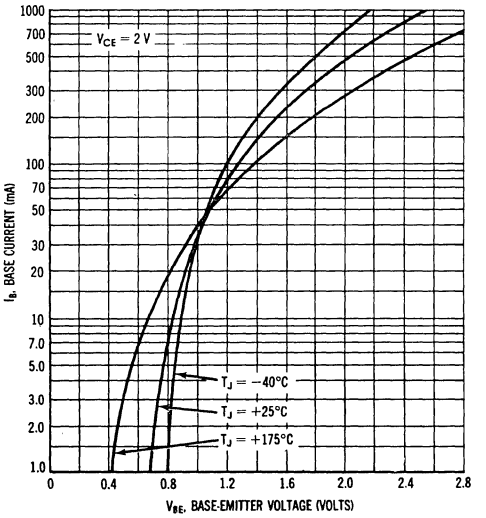
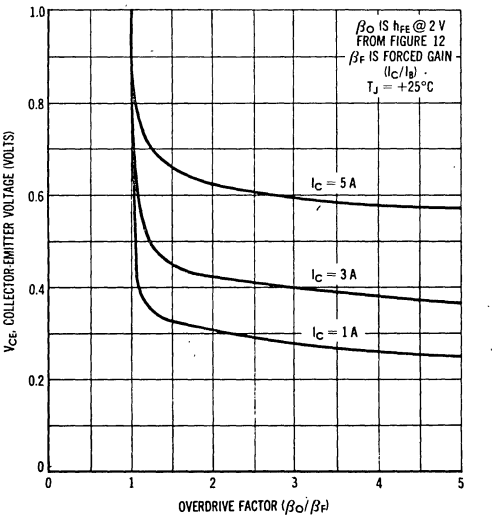


FIGURE 10 – SATURATION REGION



NOTE 1. Dashed line indicates metered base current minus I_{CBO} of the transistor at 175°C.

FIGURE 11 – CURRENT GAIN VARIATIONS

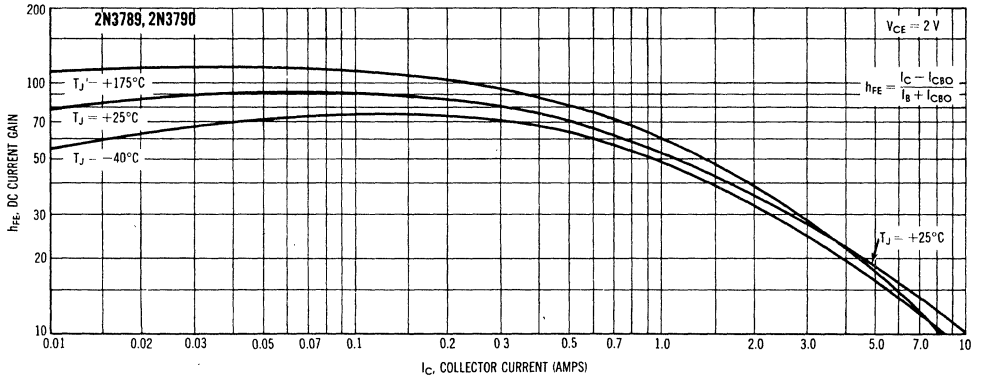


FIGURE 12 – CURRENT GAIN VARIATIONS

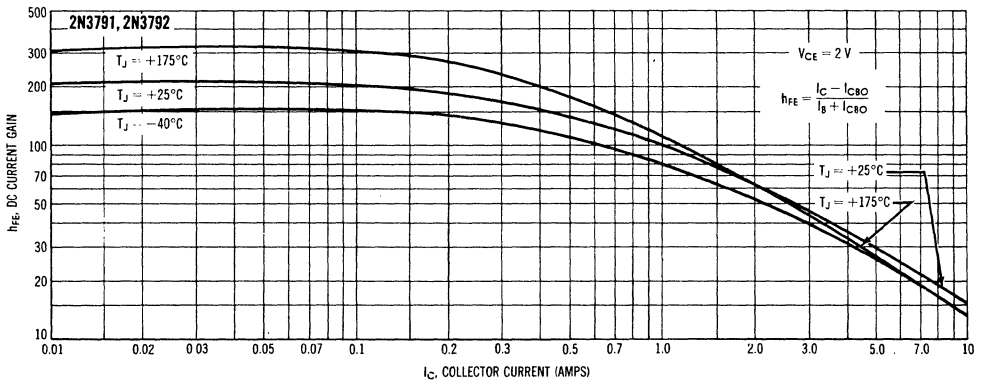


FIGURE 13 – SATURATION VOLTAGES

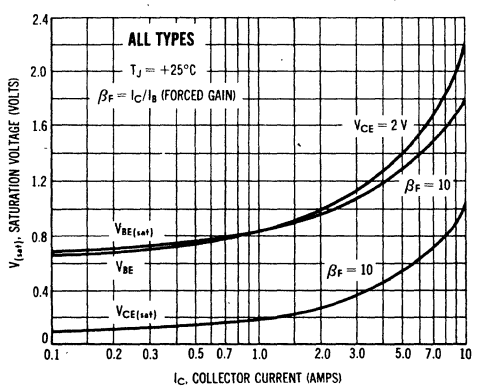
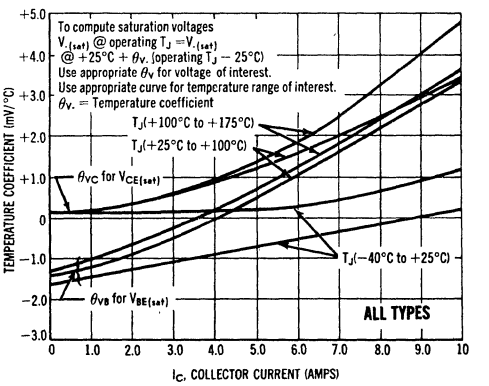


FIGURE 14 – TEMPERATURE COEFFICIENTS



SAFE OPERATING AREAS

FIGURE 15 – 2N3789, 2N3791

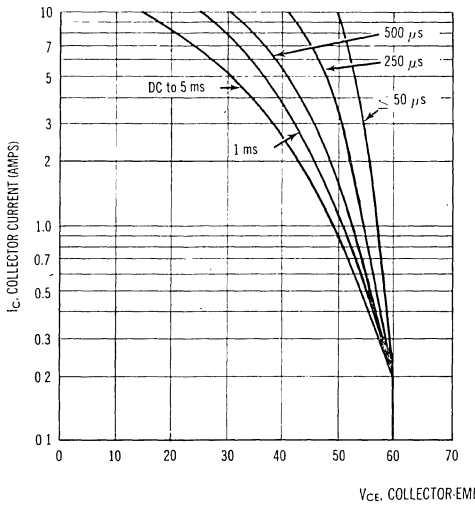
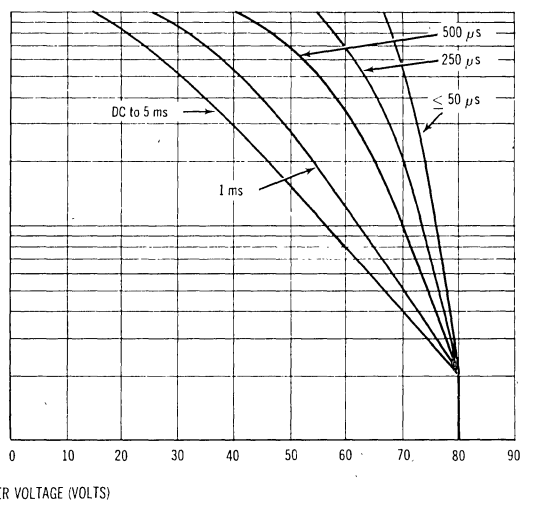


FIGURE 16 – 2N3790, 2N3792



V_{CE}, COLLECTOR-EMITTER VOLTAGE (VOLTS)

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector-emitter short. (Duty cycle of the excursions make no significant change in these safe areas.) To insure operation below the maximum T_J, the power-temperature derating curve must be observed for both steady state and pulse power conditions.

FIGURE 17 – CUT-OFF REGION TRANSCONDUCTANCE

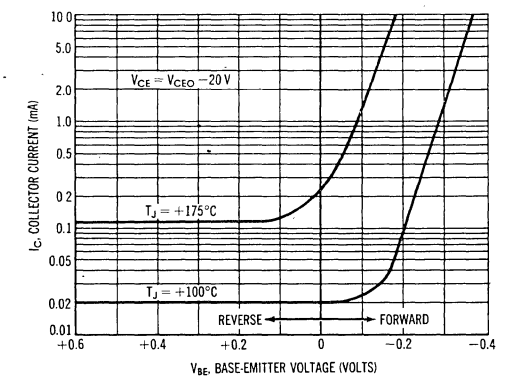
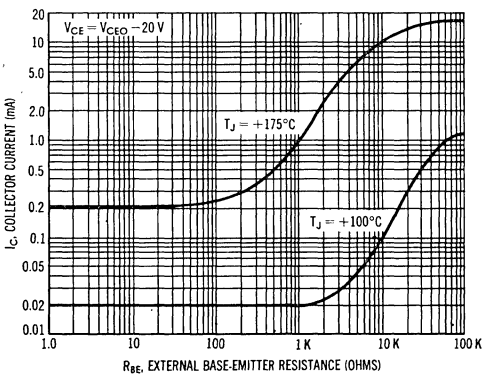


FIGURE 18 – COLLECTOR CUT-OFF CURRENT versus BASE-EMITTER RESISTANCE



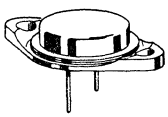
2N3902 NPN (SILICON)

HIGH VOLTAGE NPN SILICON TRANSISTORS

. . . designed for use in high-voltage inverters, converters, switching regulators and line operated amplifiers.

- High Collector-Emitter Voltage – V_{CEX} = 700 Vdc
- Excellent DC Current Gain – h_{FE} = 10 (Min) @ I_C = 2.5 Adc
- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 0.8 Vdc (Max) @ I_C = 1.0 Adc

3.5 AMPERE
POWER TRANSISTORS NPN SILICON
400 VOLTS
100 WATTS



4

*MAXIMUM RATINGS

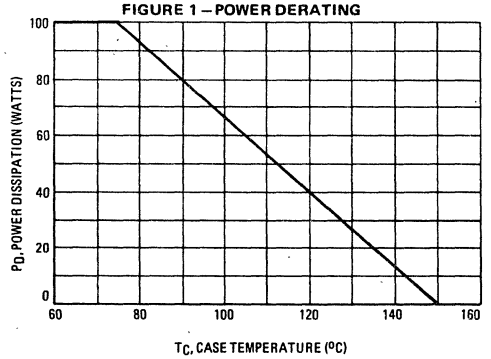
Rating	Symbol	2N3902	Unit
Collector-Emitter Voltage	V_{CEO}	400	Vdc
Collector-Emitter Voltage	V_{CEX}	700	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	3.5	Adc
Base Current	I_B	2.0	Adc
Total Device Dissipation @ T_C = 75°C Derate above 75°C	P_D	100 1.33	Watts W/°C
Operating Junction Temperature Range	T_J	-65 to +150	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

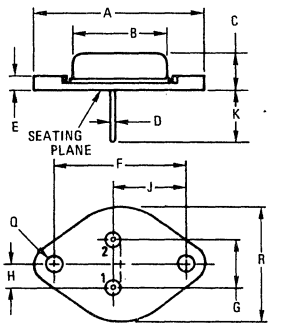
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.75	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.

CASE 11-01
TO-3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0) (See Figure 12)	$V_{CEO(sus)}$	325	–	Vdc
Collector Cutoff Current (V_{CE} = 400 Vdc, I_B = 0)	I_{CEO}	0.25	–	mAdc
Collector Cutoff Current (V_{CE} = 700 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	I_{CEX}	–	2.5	mAdc
(V_{CE} = 400 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)		–	0.5	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	30	90	–
(I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)		10	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	–	0.8	Vdc
(I_C = 2.5 Adc, I_B - 0.5 Adc)		–	2.5	
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B - 0.1 Adc)	$V_{BE(sat)}$	–	1.5	Vdc
(I_C 2.5 Adc, I_B 0.5 Adc)		–	2.0	
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 10 Vdc)	f_T	2.8	–	MHz

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

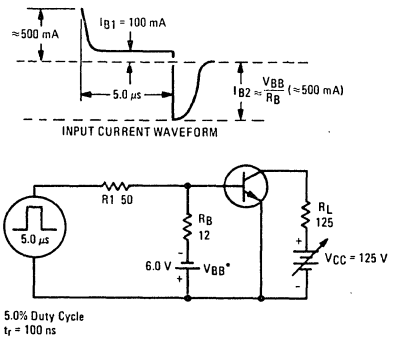


FIGURE 3 – TURN-ON TIME

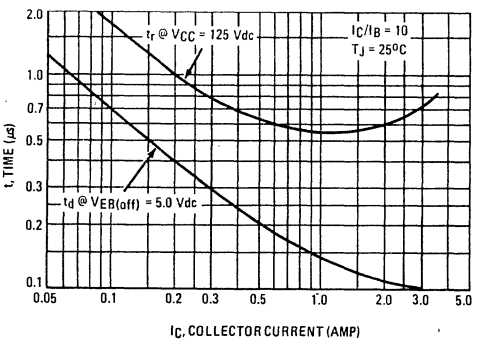
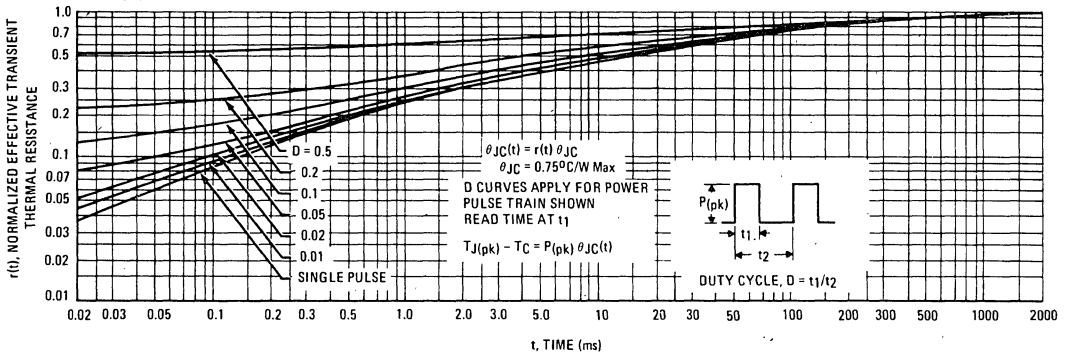
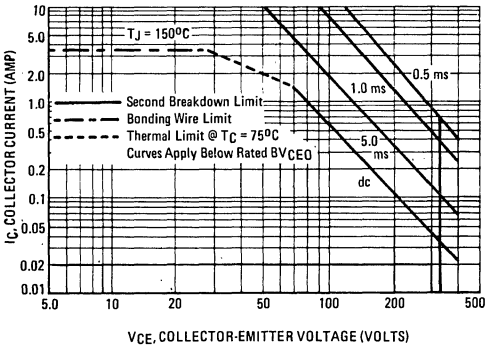


FIGURE 4 – THERMAL RESPONSE



4

FIGURE 5 – ACTIVE-REGION SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 – TURN-OFF TIME

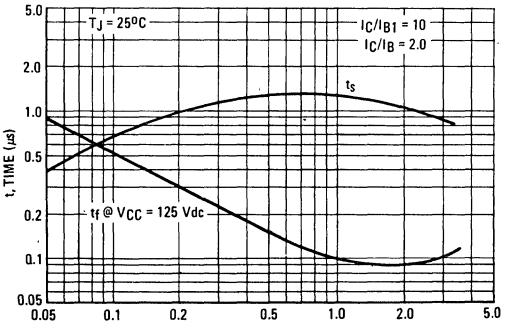


FIGURE 7 – CAPACITANCE

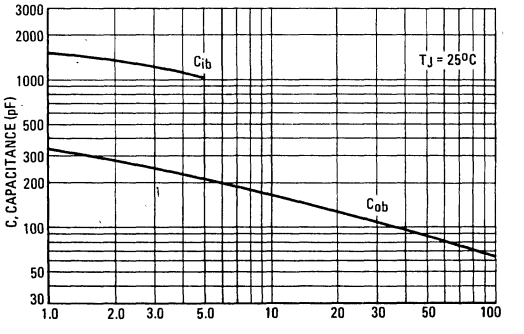


FIGURE 8 – DC CURRENT GAIN

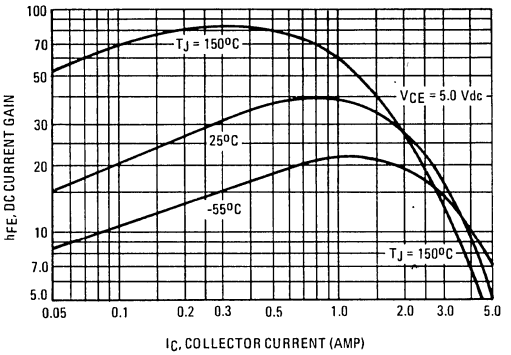
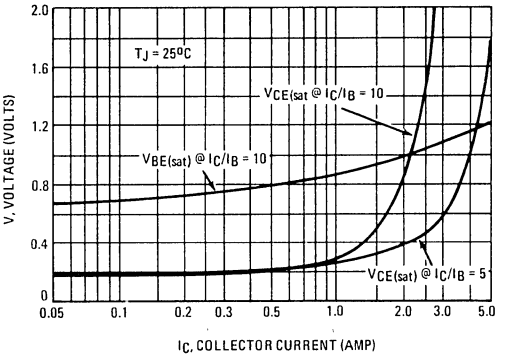


FIGURE 9 – "ON" VOLTAGES



4

FIGURE 10 – COLLECTOR CUT-OFF REGION

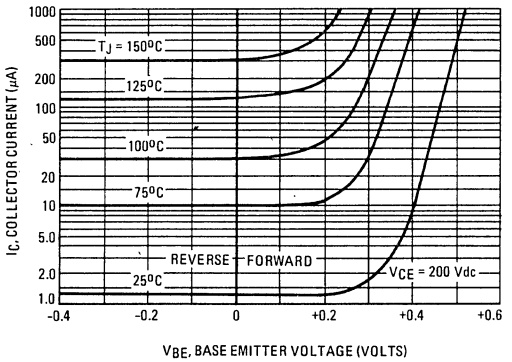


FIGURE 11 – TEMPERATURE COEFFICIENTS

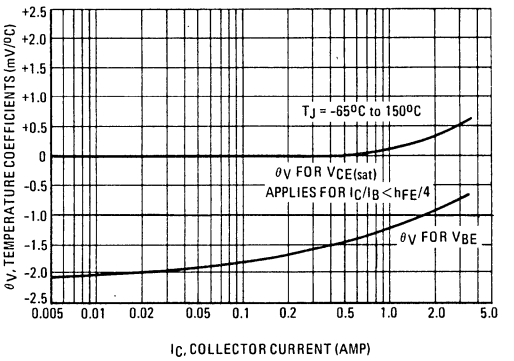
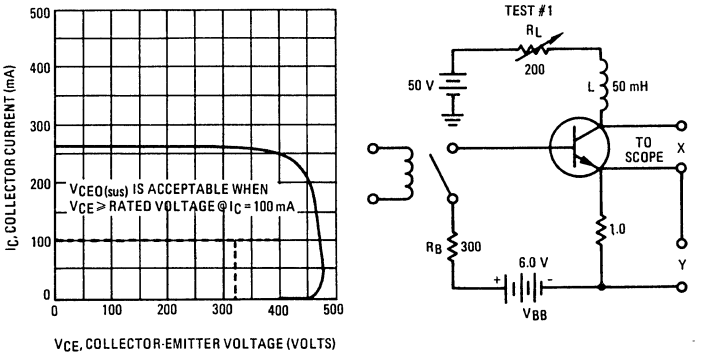


FIGURE 12 – COLLECTOR-EMITTER SUSTAINING VOLTAGE TEST CIRCUITS AND LOAD LINES



2N4231A thru 2N4233A NPN (SILICON)
2N6312 thru 2N6314 PNP

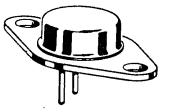
4

COMPLEMENTARY SILICON MEDIUM-POWER TRANSISTORS

. . . designed for general-purpose power amplifier and switching applications.

- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 0.7 Vdc (Max) @ I_C = 1.5 Adc
- Low Leakage Current – I_{CEX} = 0.1 mAdc (Max)
- Excellent DC Current Gain – h_{FE} = 25-100 @ I_C = 1.5 Adc
- High Current Gain – Bandwidth Product – f_T = 4.0 MHz @ I_C = 0.25 Adc

5.0 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
40-60-80 VOLTS
75 WATTS



*MAXIMUM RATINGS

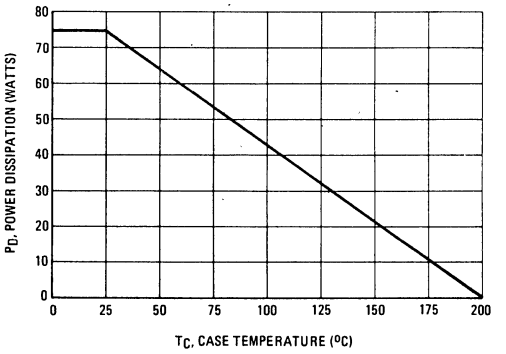
Rating	Symbol	2N4231A 2N6312	2N4232A 2N6313	2N4233A 2N6314	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current – Continuous Peak	I_C	← 5.0 → ← 10 →			Adc
Base Current	I_B	← 2.0 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 75 → ← 0.43 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	← -65 to +200 →			°C

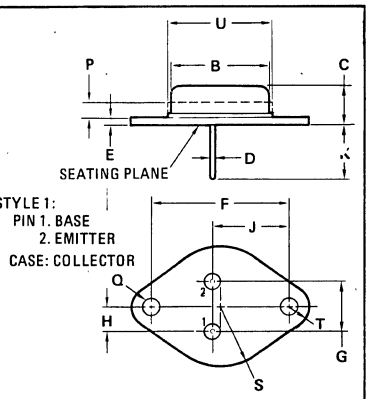
*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.32	°C/W

*Indicates JEDEC registered data. (All values meet or exceed JEDEC registered data).

FIGURE 1 – POWER DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.
CASE 80-02
TO-66

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

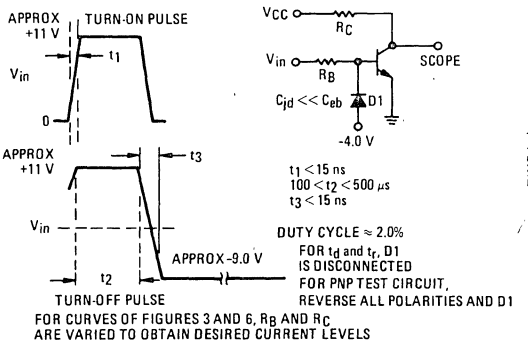
Characteristic		Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N4231A, 2N6312		40	–	
	2N4232A, 2N6313		60	–	
	2N4233A, 2N6314		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N4231A, 2N6312		–	1.0	
(V_{CE} = 50 Vdc, I_B = 0)	2N4232A, 2N6313		–	1.0	
(V_{CE} = 70 Vdc, I_B = 0)	2N4233A, 2N6314		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N4231A, 2N6312		–	0.1	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N4232A, 2N6313		–	0.1	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N4233A, 2N6314		–	0.1	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N4231A, 2N6312		–	1.0	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N4232A, 2N6313		–	1.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N4233A, 2N6314		–	1.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N4231A, 2N6312		–	0.05	
(V_{CB} = 60 Vdc, I_E = 0)	2N4232A, 2N6313		–	0.05	
(V_{CB} = 80 Vdc, I_E = 0)	2N4233A, 2N6314		–	0.05	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)			–	0.5	
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
*(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)			40	–	
*(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)			25	100	
*(I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)			10	–	
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)			4.0	–	
*Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 0.15 Adc)			–	0.7	
(I_C = 3.0 Adc, I_B = 0.3 Adc)			–	2.0	
(I_C = 5.0 Adc, I_B = 1.25 Adc)			–	4.0	
*Base-Emitter On Voltage (1)		$V_{BE(on)}$			Vdc
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)			–	1.4	
***DYNAMIC CHARACTERISTICS**					
Current-Gain – Bandwidth Product		f_T			MHz
(I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)			4.0	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)			–	300	
Small-Signal Current Gain		h_{fe}			–
(I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)			20	–	

*Indicates JEDEC registered data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

4

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



t_1 < 15 ns
100 < t_2 < 500 μs
t_3 < 15 ns

DUTY CYCLE ≈ 2.0%
FOR t_d and t_r, D1 IS DISCONNECTED
FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES AND D1

FOR CURVES OF FIGURES 3 AND 6, R_B AND R_C ARE VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE I_B ≈ 100 mA
MSD6100 USED BELOW I_B ≈ 100 mA

FIGURE 3 – TURN "ON" TIME

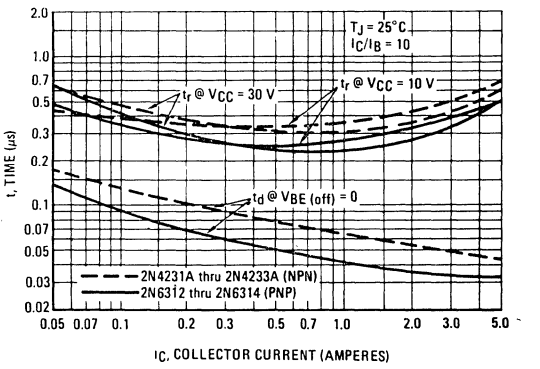
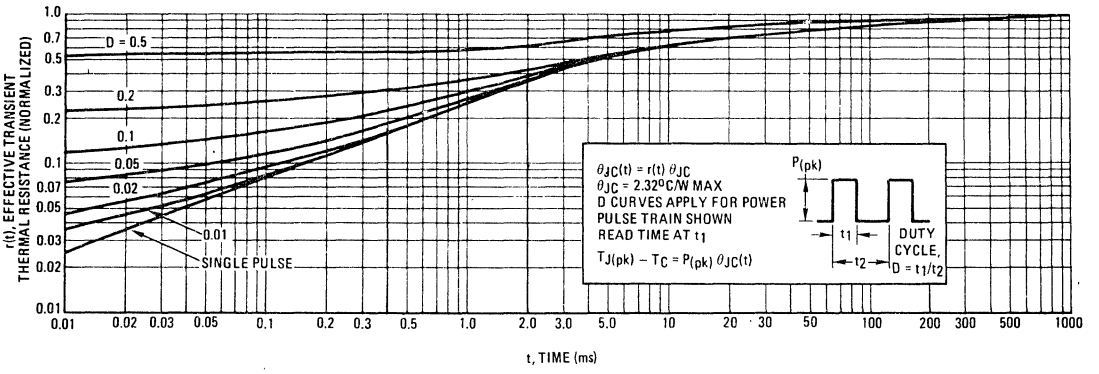
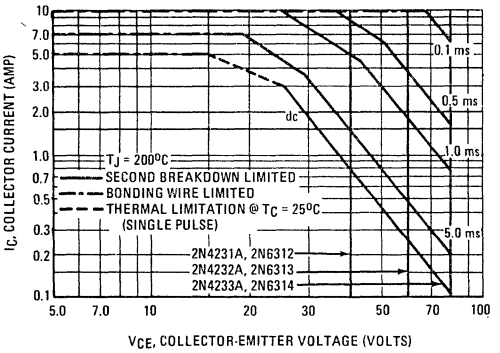


FIGURE 4 – THERMAL RESPONSE



4

FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN "OFF" TIME

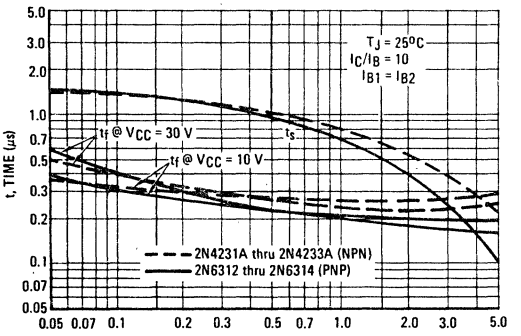
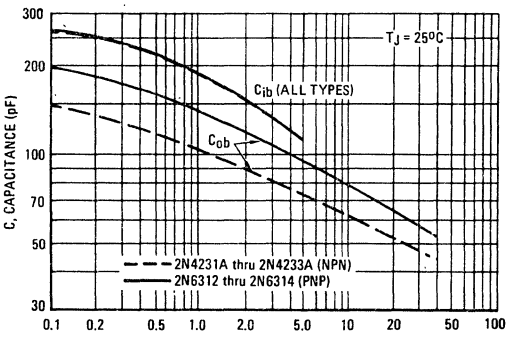


FIGURE 7 – CAPACITANCE



NPN
2N4231A thru 2N4233A

PNP
2N6312 thru 2N6314

FIGURE 8 – DC CURRENT GAIN

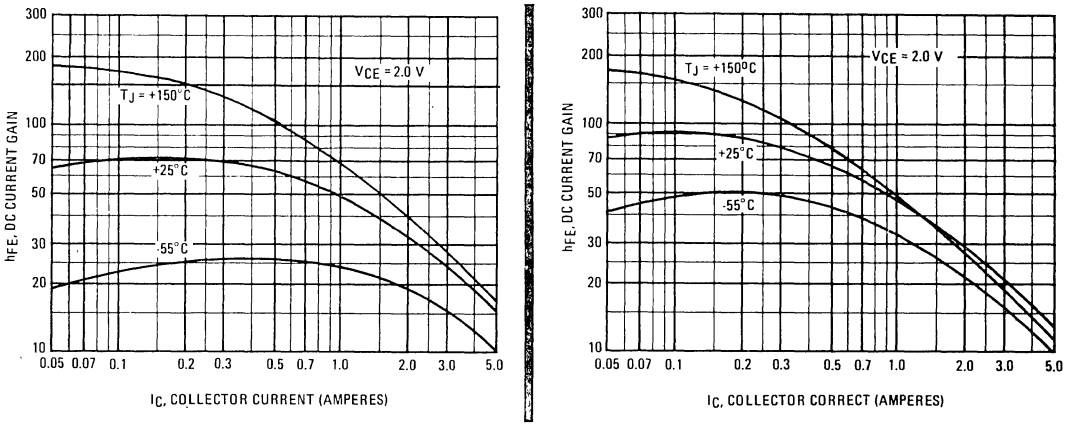


FIGURE 9 – COLLECTOR SATURATION REGION

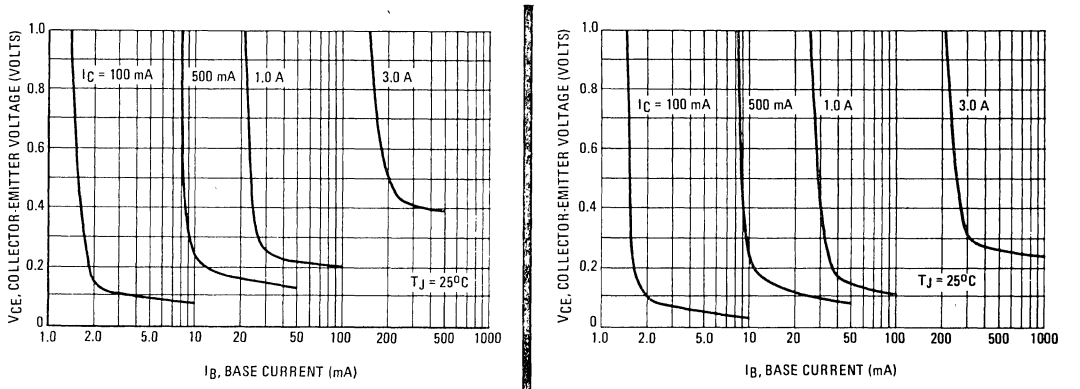
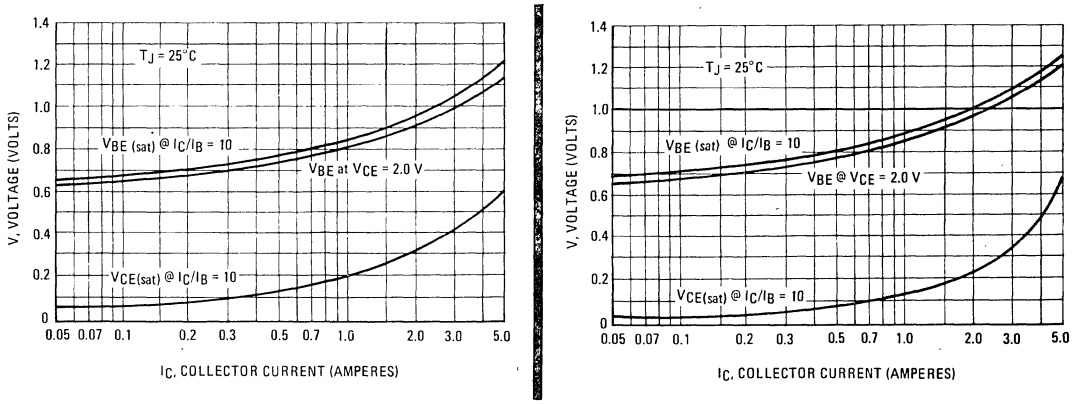


FIGURE 10 – "ON" VOLTAGES

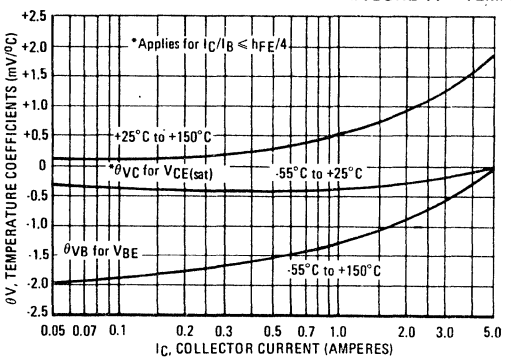


4

NPN
2N4231A thru 2N4233A

PNP
2N6312 thru 2N6314

FIGURE 11 – TEMPERATURE COEFFICIENTS



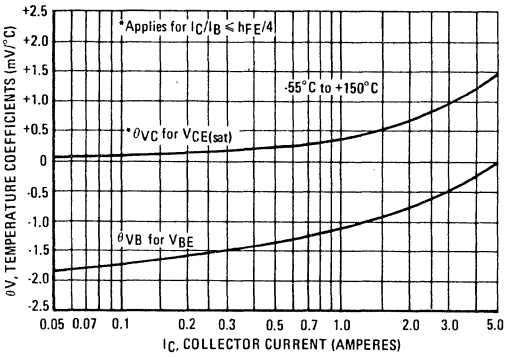


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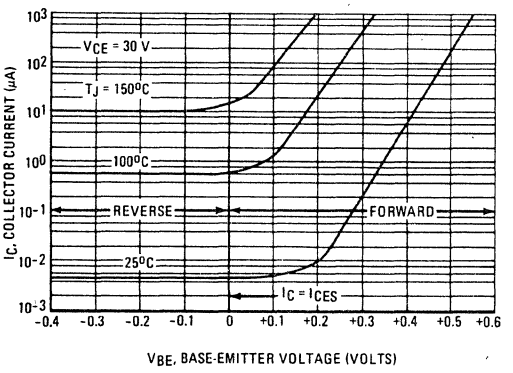
FIGURE 12 – COLLECTOR CUT-OFF REGION



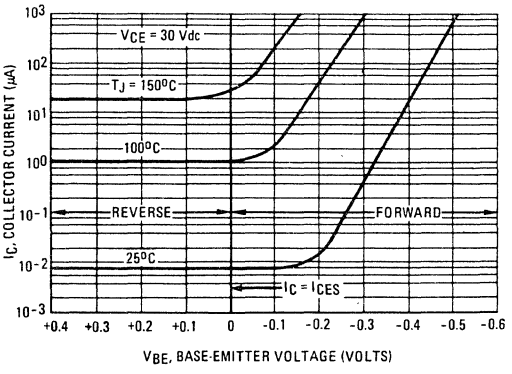
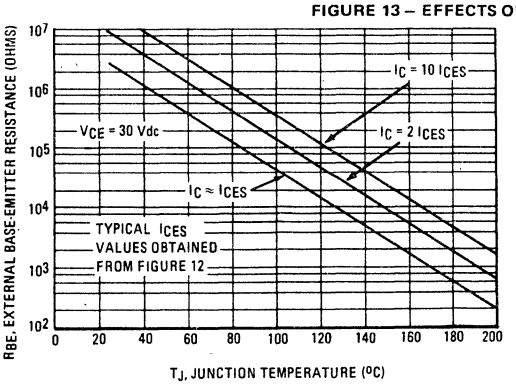
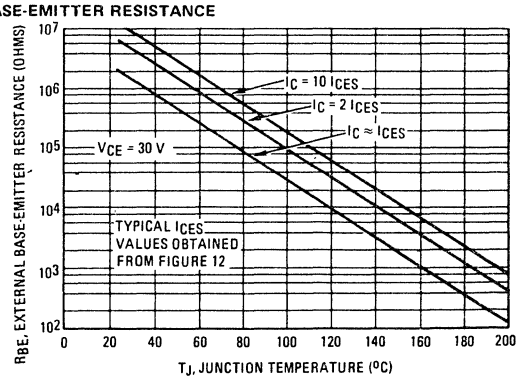


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE





2N4398
2N4399
2N5745

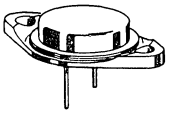
PNP SILICON HIGH-POWER TRANSISTORS

. . . designed for use in power amplifier and switching circuits.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 15 Adc (2N4398, 2N4399)
- DC Current Gain Specified — 1.0 to 30 Adc
- Complements to NPN 2N5301, 2N5302, 2N5303

20, 30 AMPERE POWER TRANSISTORS PNP SILICON

40–60–180 VOLTS
200 WATTS



*MAXIMUM RATINGS

Rating	Symbol	2N4398	2N4399	2N5745	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	30 50	30 50	20 50	Adc
Base Current — Continuous Peak	I_B	7.5 15			Adc
Total Device Dissipation @ $T_A = 25^oC$** Derate above 25^oC	P_D	5.0 28.6			Watts mW/^oC
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	200 1.15			Watts W/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			^oC

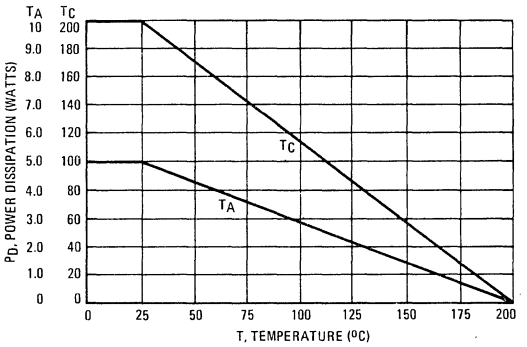
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	$^oC/W$
Thermal Resistance, Junction to Ambient	θ_{JA}	35	$^oC/W$

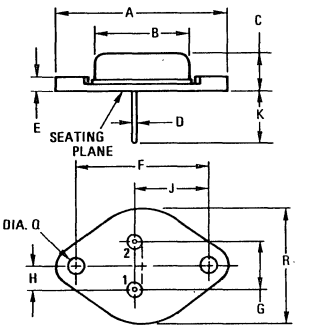
*Indicates JEDEC Registered Data

**Motorola guarantees this data in addition to JEDEC Registered Data.

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 13. All limits are applicable and must be observed.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11–01
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage(1) (I_C = 200 mAdc, I_B = 0)	2N4398	$V_{CEO(sus)}$	40	–	Vdc
	2N4399		60	–	
	2N5745		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N4398		–	5.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N4399		–	5.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N5745		–	5.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N4398		–	5.0	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N4399		–	5.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5745		–	5.0	
(V_{CE} = 30 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N4398, 2N4399		–	10	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5745		–	10	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N4398		–	1.0	
(V_{CB} = 60 Vdc, I_E = 0)	2N4399		–	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	2N5745		–	1.0	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain(1)		h_{FE}			
(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	All Types		40	–	
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5745		15	60	
(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N4398, 2N4399		15	60	
(I_C = 20 Adc, V_{CE} = 2.0 Vdc)	2N5745		5.0	–	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N4398, 2N4399		5.0	–	
Collector-Emitter Saturation Voltage(1)		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)	2N4398, 2N4399		–	0.75	
	2N5745		–	1.0	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N4398, 2N4399		–	1.0	
	2N5745		–	1.5	
(I_C = 20 Adc, I_B = 2.0 Adc)	2N4398, 2N4399		–	2.0	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5745		–	2.0	
(I_C = 30 Adc, I_B = 6.0 Adc)	2N4398, 2N4399		–	4.0	
Base-Emitter Saturation Voltage(1)		$V_{BE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)**	2N4398, 2N4399		–	1.6	
	2N5745		–	1.7	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N4398, 2N4399		–	1.85	
	2N5745		–	2.0	
(I_C = 20 Adc, I_B = 2.0 Adc)**	2N4398, 2N4399		–	2.5	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5745		–	2.5	
Base-Emitter On Voltage(1)		$V_{BE(on)}$			Vdc
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5745		–	1.5	
(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N4398, 2N4399		–	1.7	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)	2N5745		–	2.5	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N4398, 2N4399		–	3.0	
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product(2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	2N4398, 2N4399	f_T	4.0	–	MHz
	2N5745		2.0	–	
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	40	–	–
SWITCHING CHARACTERISTICS (See Figures 2 and 3)					
Rise Time	2N4398, 2N4399	t_r	–	0.4	μs
	2N5745		–	1.0	
Storage Time (V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	2N4398, 2N4399	t_s	–	1.5	μs
	2N5745		–	2.0	
Fall Time	2N4398, 2N4399	t_f	–	0.6	μs
	2N5745		–	1.0	

*Indicates JEDEC Registered Data.

**Motorola Guarantees this Data in Addition to JEDEC Registered Data.

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2)f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

SWITCHING TIME EQUIVALENT TEST CIRCUITS

FIGURE 2 – TURN-ON TIME

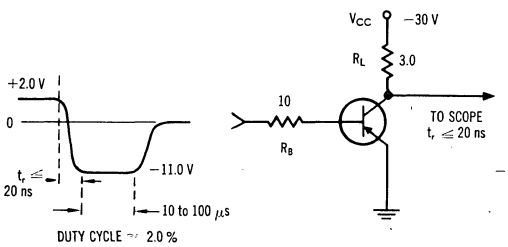
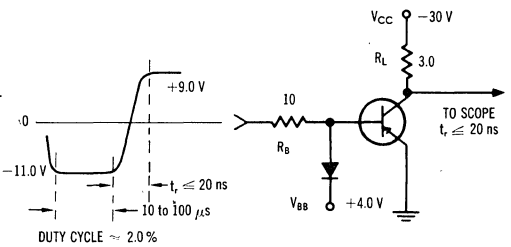


FIGURE 3 – TURN-OFF TIME



FOR CURVES OF FIGURES 5 & 6, R_B, R_L, & V_{CC} ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.

TYPICAL TRANSIENT CHARACTERISTICS

FIGURE 4 – CAPACITANCES

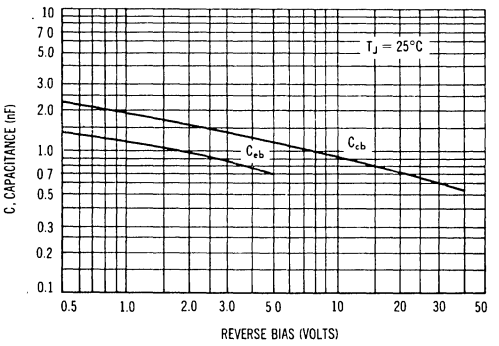


FIGURE 5 – TURN-ON TIME

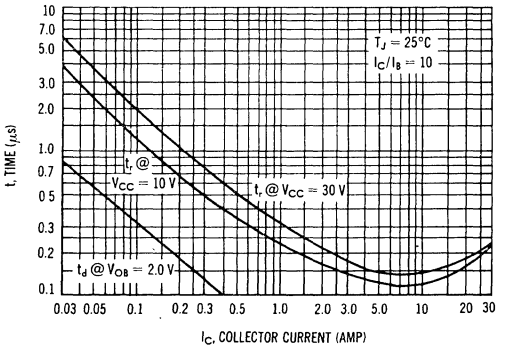
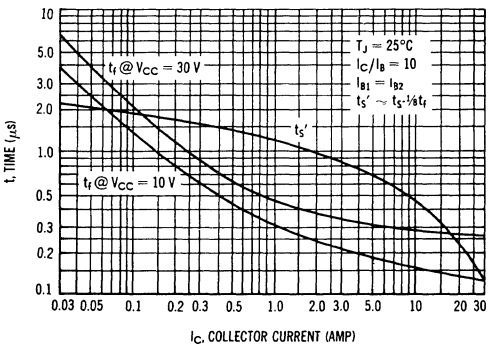


FIGURE 6 – TURN-OFF TIME



TYPICAL "OFF" REGION CHARACTERISTICS

FIGURE 7 – TRANSCONDUCTANCE

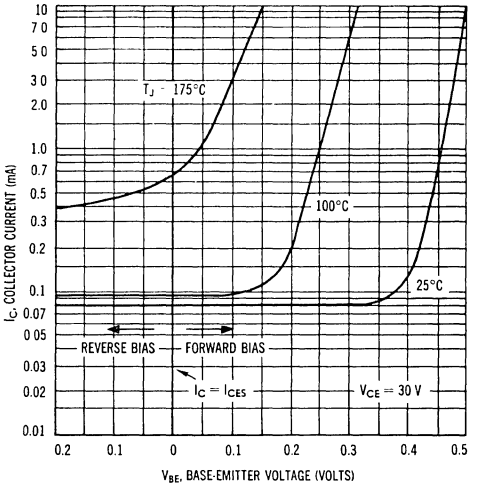
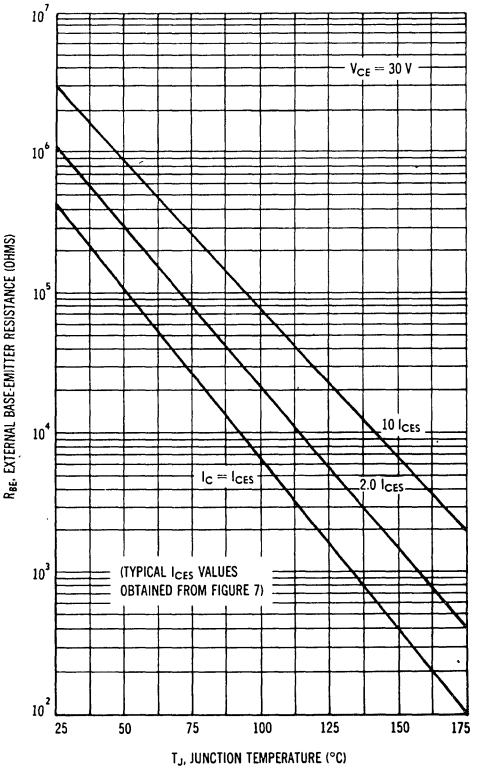


FIGURE 8 – EFFECT OF BASE-EMITTER RESISTANCE



TYPICAL "ON" REGION CHARACTERISTICS

FIGURE 9 – DC CURRENT GAIN

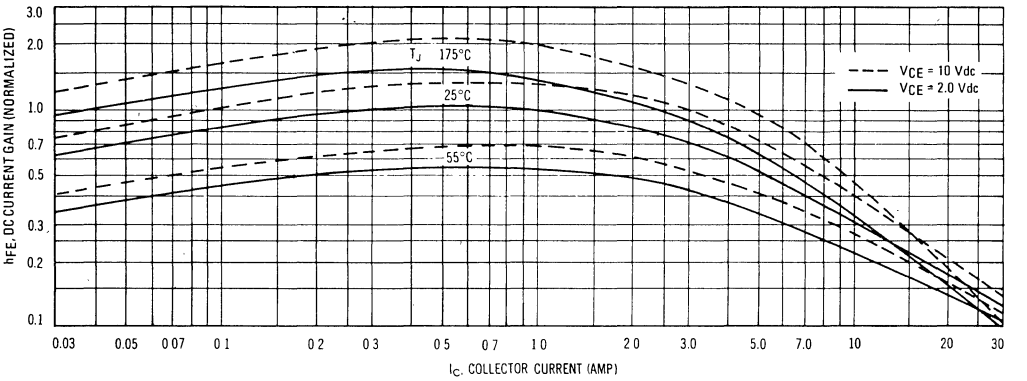


FIGURE 10 – COLLECTOR SATURATION REGION

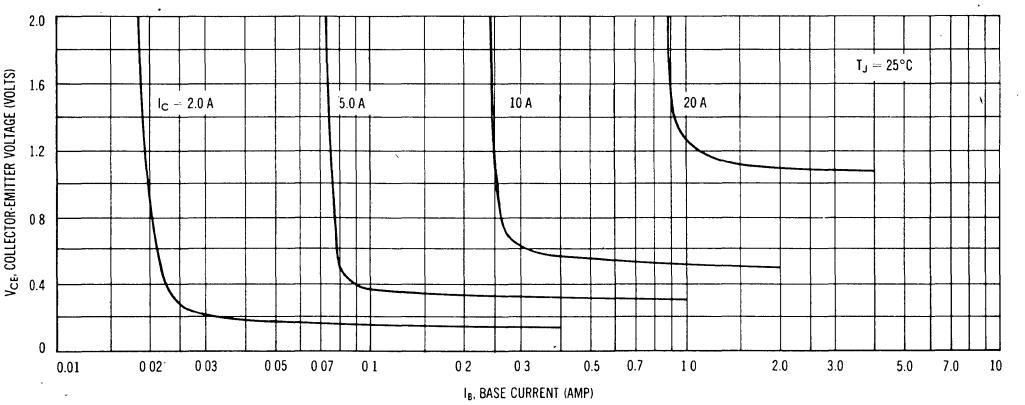


FIGURE 11 – "ON" VOLTAGES

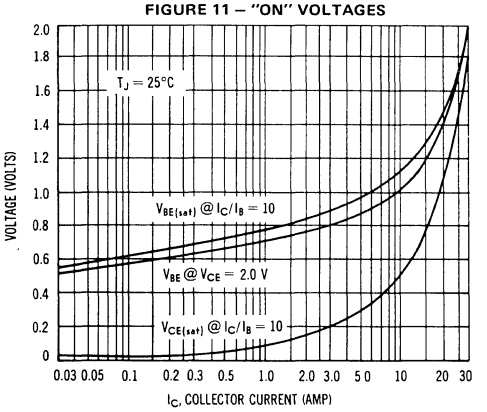
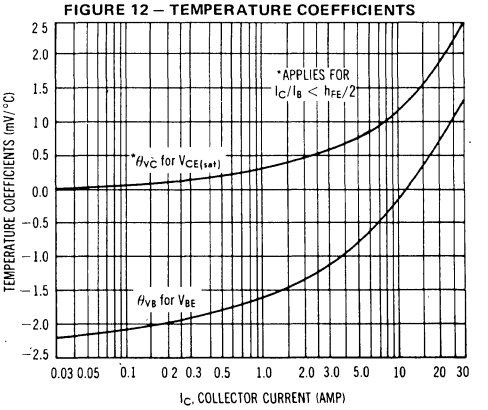
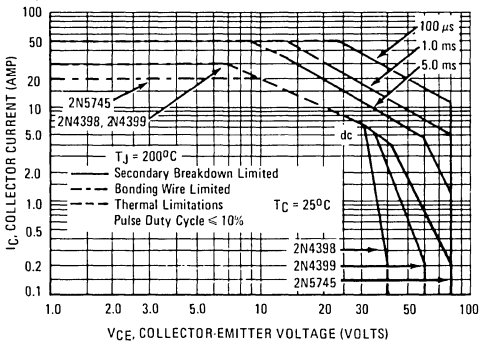


FIGURE 12 – TEMPERATURE COEFFICIENTS



RATINGS AND THERMAL DATA

FIGURE 13 – ACTIVE-REGION SAFE OPERATING AREA

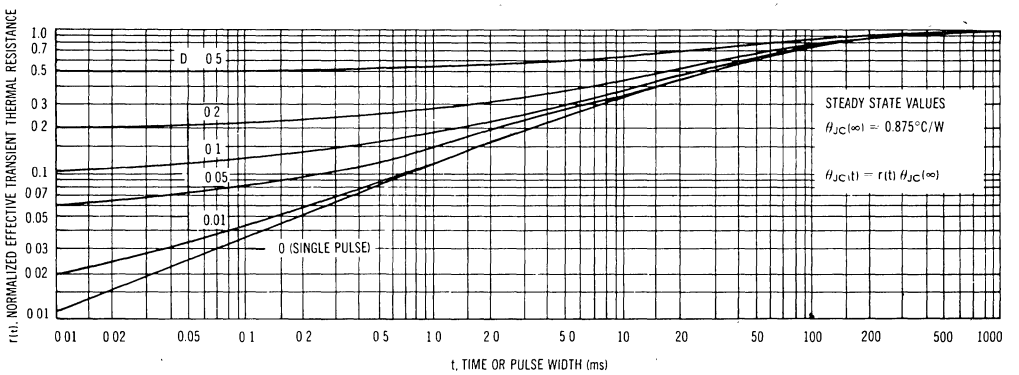


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

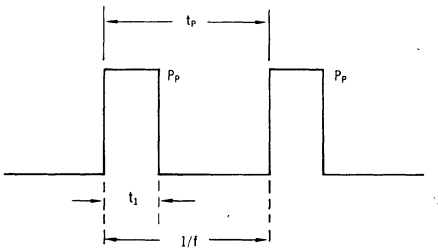
The data of Figure 13 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 14. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

4

FIGURE 14 – THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA



DUTY CYCLE D $t_1 f = \frac{t_1}{t_P}$

PEAK PULSE POWER P_P

A train of periodical power pulses can be represented by the model as shown in Figure A. Using the model and the device thermal reponse, the normalized effective transient thermal resistance of Figure 14 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 14 by the steady state value $\theta_{JC}(\infty)$.

Example:

The 2N4398 is dissipating 100 watts under the following conditions: $t_1 = 1.0$ ms, $t_P = 5.0$ ms. (D = 0.2)

Using Figure 14, at a pulse width of 1.0 ms and D = 0.2, the reading of r (t) is 0.28.

The peak rise in junction temperature is therefore

$$\triangle T = r(t) \times P_P \times \theta_{JC}(\infty) = 0.28 \times 100 \times 0.875 = 24.5°C$$

2N4877 (SILICON)

MEDIUM-POWER NPN SILICON TRANSISTOR

. . . designed for switching and wide band amplifier applications.

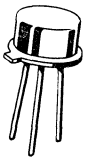
- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 4.0 Amp
- DC Current Gain Specified to 4 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact TO-39 Case for Critical Space-Limited Applications.

4 AMPERE POWER TRANSISTOR

NPN SILICON

60 VOLTS

10 WATTS



4

* MAXIMUM RATINGS

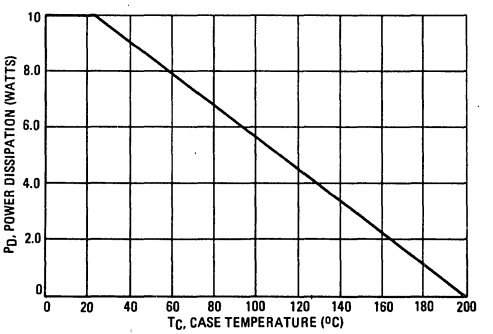
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	70	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	4.0	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 57.2	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data

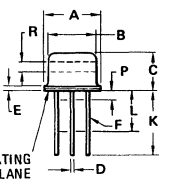
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	17.5	°C/W

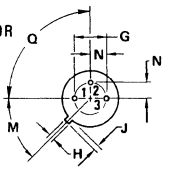
FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 2. All limits are applicable and must be observed.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

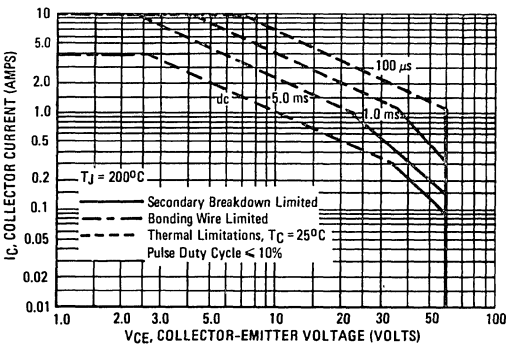
CASE 79-02
TO-39

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector Cutoff Current (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	I_{CEX}	–	100	μAdc
(V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)		–	1.0	mAdc
Collector Cutoff Current (V_{CB} = 70 Vdc, I_E = 0)	I_{CBO}	–	100	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS(1)				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	30	–	–
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)		20	100	
Collector-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	–	1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 0.4 Adc)	$V_{BE(sat)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 0.25 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	4.0	–	MHz
(I_C = 0.25 Adc, V_{CE} = 10 Vdc, f = 10 MHz)**		30	–	
SWITCHING CHARACTERISTICS				
Rise Time (V_{CC} = 25 Vdc, I_C = 4.0 Adc, I_{B1} = 0.4 Adc)	t_r	–	100	ns
Storage Time (V_{CC} = 25 Vdc, I_C = 4.0 Adc,	t_s	–	1.5	μs
Fall Time I_{B1} = I_{B2} = 0.4 Adc)	t_f	–	500	ns

*Indicates JEDEC Registered Data.
**Motorola guarantees this value in addition to JEDEC Registered Data.
Note 1: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

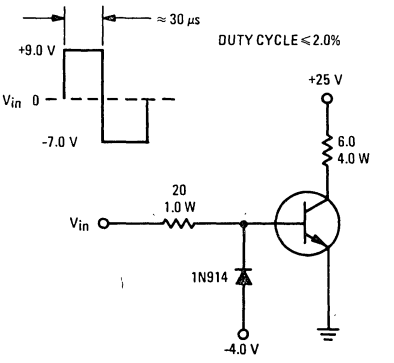
FIGURE 2 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 200°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 3 – SWITCHING TIME TEST CIRCUIT



2N4898 thru 2N4900

4

MEDIUM-POWER PNP SILICON TRANSISTORS

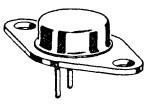
. . . designed for driver circuits, switching, and amplifier applications. These high-performance devices feature:

- Low Saturation Voltage – $V_{CE(sat)}$ = 0.6 V max @ I_C = 1.0 Amp
- Excellent Safe Operating Area
- Gain Specified to I_C = 1.0 Ampere
- 2N4900 Complementary to NPN 2N4912

4 AMPERE

GENERAL PURPOSE POWER TRANSISTORS

40-80 VOLTS
25 WATTS



MAXIMUM RATINGS

Rating	Symbol	2N4898	2N4899	2N4900	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current – Continuous*	I_C*	← 1.0 →			Adc
		← 4.0 →			
Base Current	I_B	← 1.0 →			Adc
Total Device Dissipation T_C = 25°C	P_D	← 25 →			Watts
Derate above 25°C		← 0.143 →			W/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	← −65 to +200 →			°C

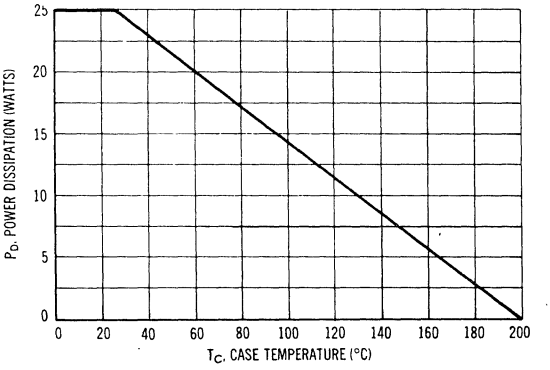
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Reistance, Junction to Case	θ_{JC}	7.0	°C/W

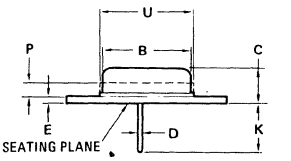
*The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements.

The 4.0 Amp maximum value is based upon actual current-handling capability of the device (see Figure 5).

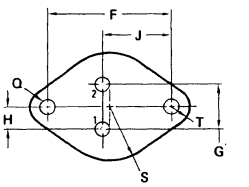
FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0) 2N4898	-	$BV_{CEO(sus)}$*	40	-	Vdc
2N4899			60	-	
2N4900			80	-	
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) 2N4898		I_{CEO}	-	0.5	mAdc
(V_{CE} = 30 Vdc, I_B = 0) 2N4899			-	0.5	
(V_{CE} = 40 Vdc, I_B = 0) 2N4900			-	0.5	
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc)	12	I_{CEX}	-	0.1	mAdc
(V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			-	1.0	
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	-	I_{CBO}	-	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	-	I_{EBO}	-	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain* (I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	8	h_{FE}*	40	-	-
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			20	100	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)			10	-	
Collector-Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)	9, 11, 13	$V_{CE(sat)}$*	-	0.6	Vdc
Base-Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)	11, 13	$V_{BE(sat)}$*	-	1.3	Vdc
Base-Emitter On Voltage* (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	11, 13	$V_{BE(on)}$*	-	1.3	Vdc
SMALL SIGNAL CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C - 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	-	f_T	3.0	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	-	C_{ob}	-	100	pF
Small-Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	-	h_{fe}	25	-	-

* Pulse Test: PW ≈300 μs, Duty Cycle ≈ 2.0%

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

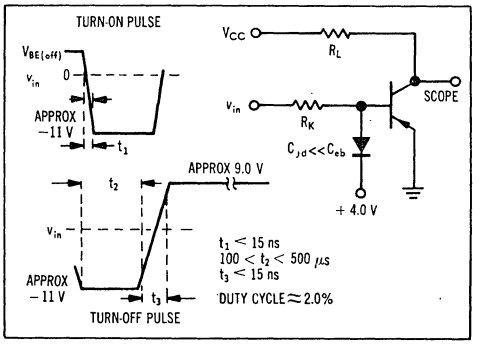


FIGURE 3 – TURN-ON TIME

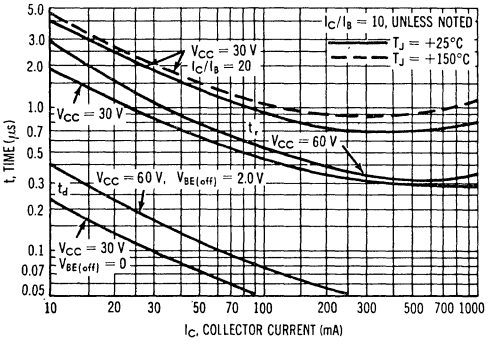
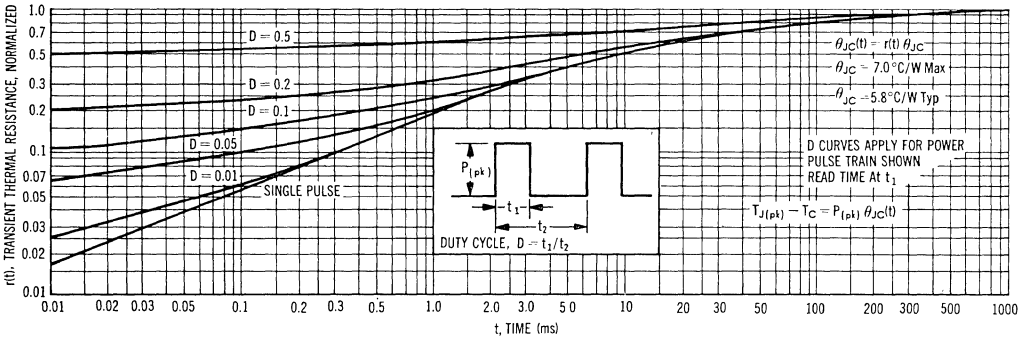
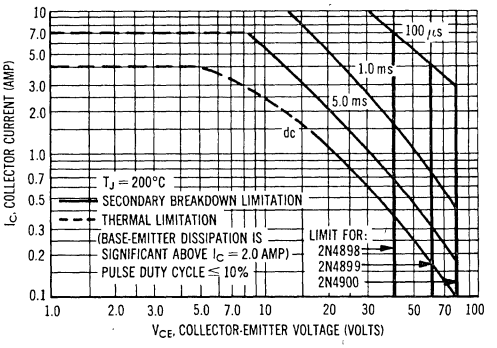


FIGURE 4 – THERMAL RESPONSE



4

FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



The safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor which must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 5 is based upon $T_{J(pk)} = 200°C$; T_C is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power which can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 – STORAGE TIME

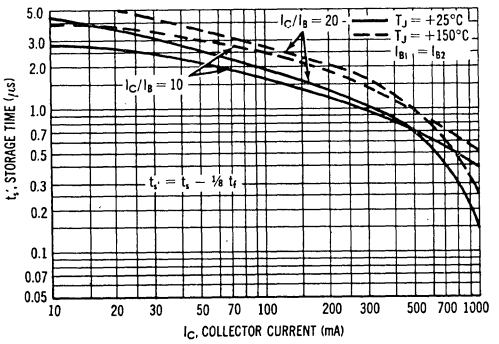


FIGURE 7 – FALL TIME

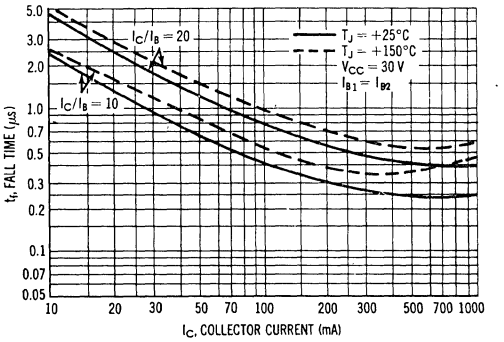


FIGURE 8 – CURRENT GAIN

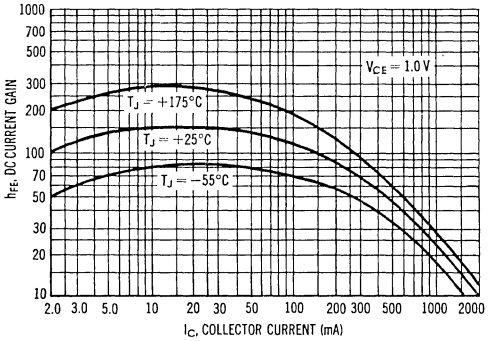
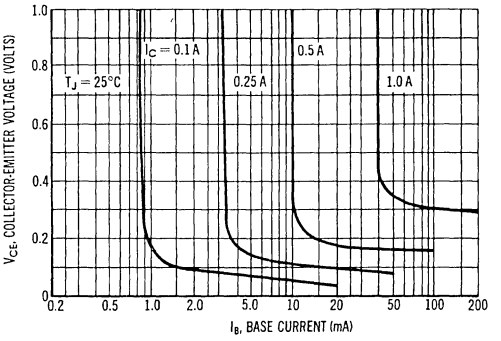


FIGURE 9 – COLLECTOR SATURATION REGION



4

FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

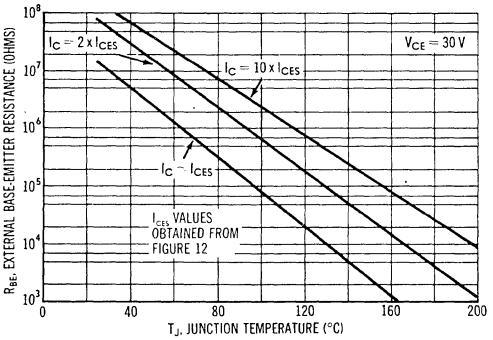


FIGURE 11 – "ON" VOLTAGE

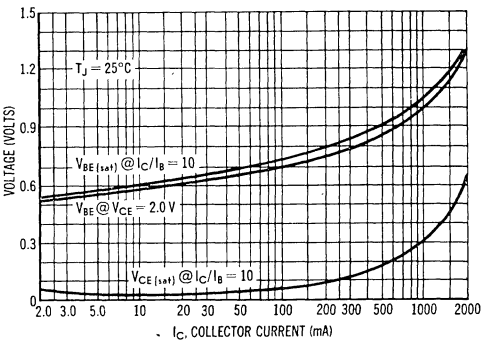


FIGURE 12 – COLLECTOR CUTOFF REGION

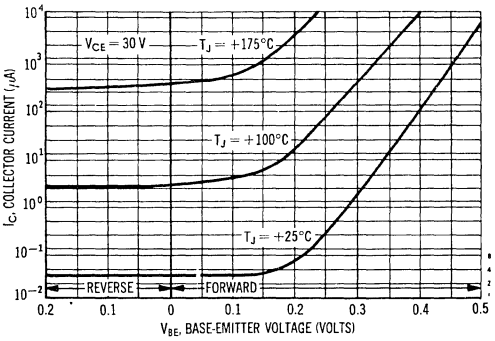
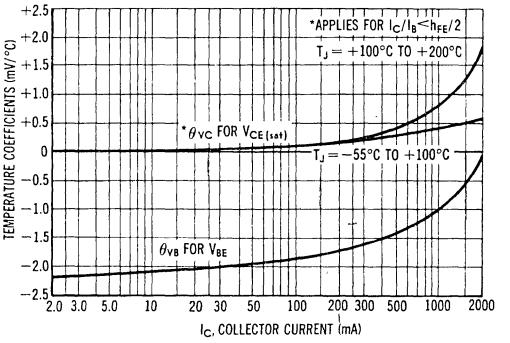


FIGURE 13 – TEMPERATURE COEFFICIENTS



NPN SILICON TRANSISTOR

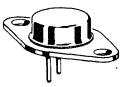
. . . designed for driver circuits, switching, and amplifier applications. This high-performance device features:

- Low Saturation Voltage – $V_{CE(sat)}$ = 0.6 V max @ I_C = 1.0 Amp
- Excellent Safe Operating Area
- Gain Specified to I_C = 1.0 Amp
- Complement to PNP 2N4900

1 AMPERE

NPN SILICON POWER TRANSISTOR

80 VOLTS
25 WATTS



MAXIMUM RATINGS

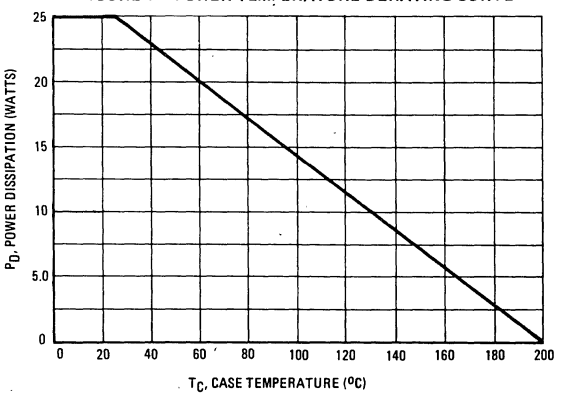
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	80	Vdc
Collector-Base Voltage	V_{CB}	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous*	I_C*	1.0	Adc
Base Current – Continuous	I_B	1.0	Adc
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	25 0.143	Watts mW/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

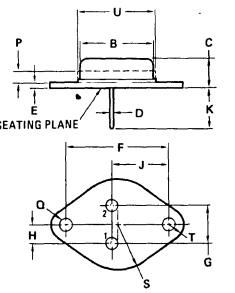
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	7.0	°C/W

*The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements.

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0)	$BV_{CEO(sus)}$	80	–	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0)	I_{CEO}	–	0.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 – –	 0.1 1.0	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	I_{CBO}	–	0.1	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	 40 20 10	 – 100 –	–
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	–	0.6	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{BE(sat)}$	–	1.3	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} - 1.0 Vdc)	$V_{BE(on)}$	–	1.3	Vdc
SMALL SIGNAL CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	3.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	100	pF
Small-Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	25	–	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

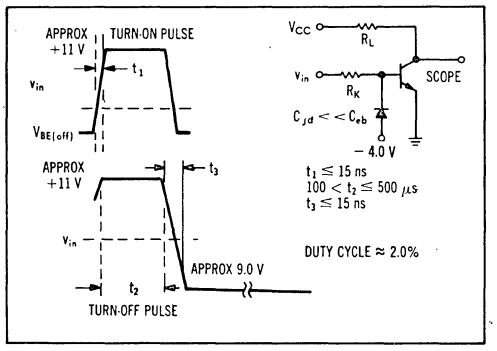


FIGURE 3 – TURN-ON TIME

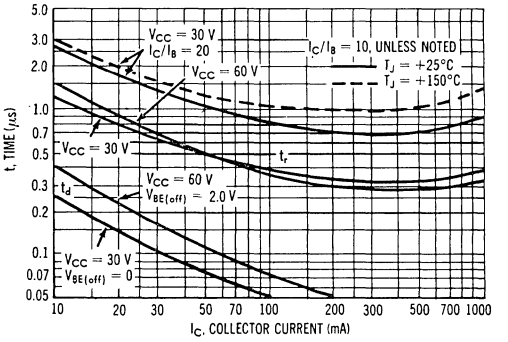
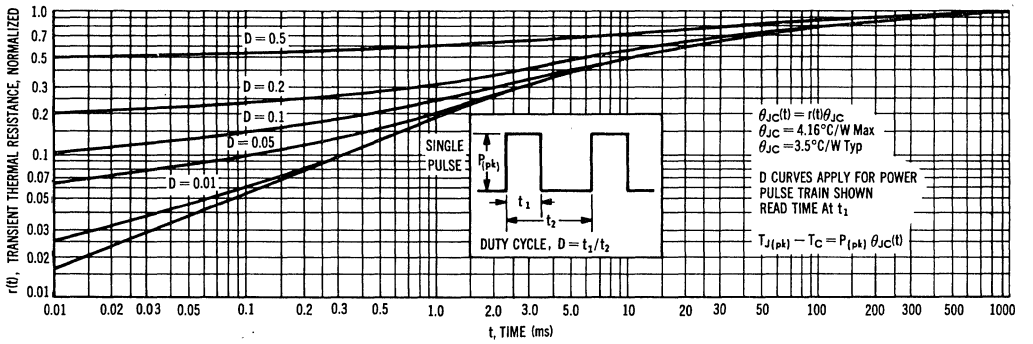
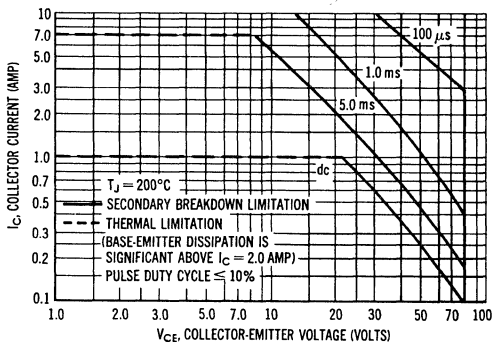


FIGURE 4 – THERMAL RESPONSE



4

FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 – STORAGE TIME

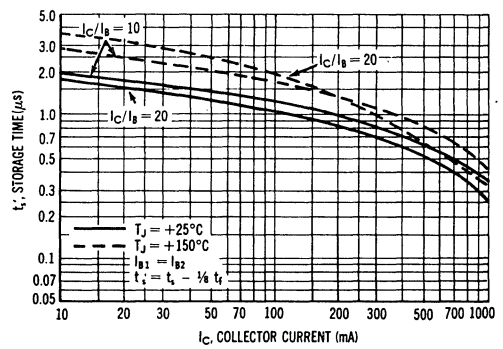
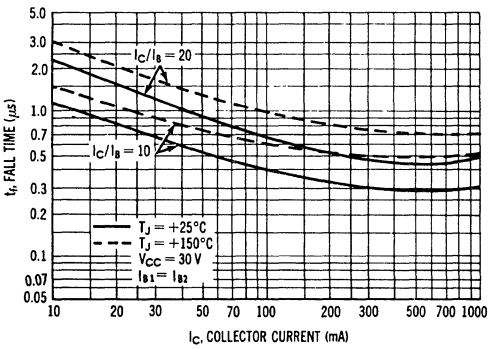


FIGURE 7 – FALL TIME



TYPICAL DC CHARACTERISTICS

FIGURE 8 – CURRENT GAIN

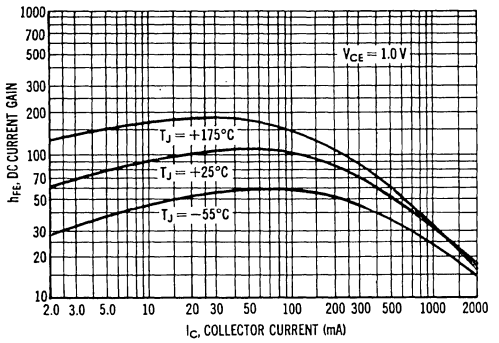


FIGURE 9 – COLLECTOR SATURATION REGION

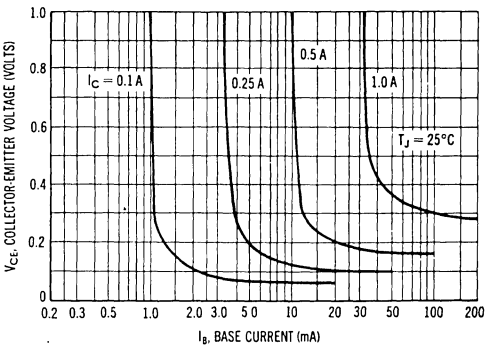


FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

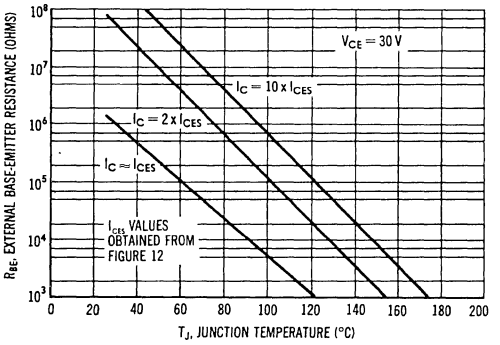


FIGURE 11 – "ON" VOLTAGE

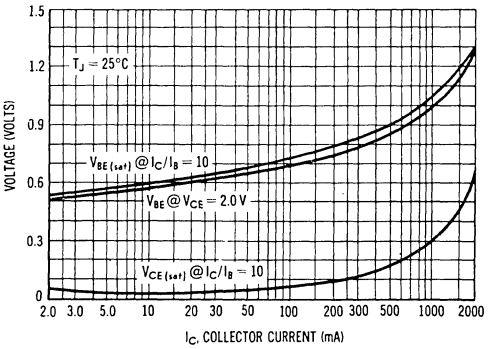


FIGURE 12 – COLLECTOR CUTOFF REGION

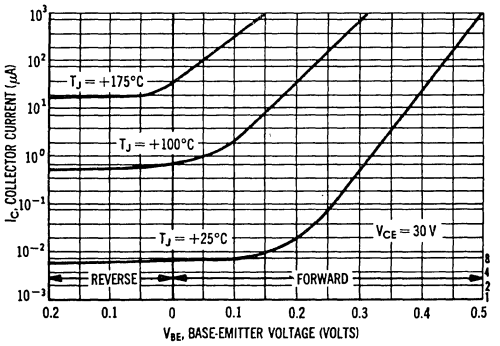
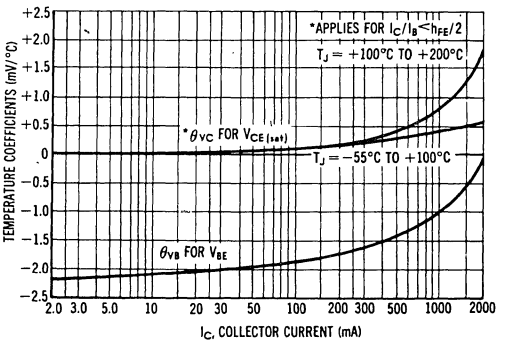


FIGURE 13 – TEMPERATURE COEFFICIENTS



2N4918 thru 2N4920 (SILICON)

4

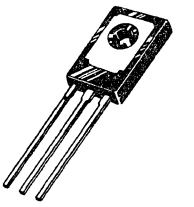
MEDIUM-POWER PLASTIC PNP SILICON TRANSISTORS

. . . designed for driver circuits, switching, and amplifier applications. These high-performance plastic devices feature:

- Low Saturation Voltage – $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 1.0 Amp
- Excellent Power Dissipation Due to Thermopad Construction – P_D = 30 @ T_C = 25°C
- Excellent Safe Operating Area
- Gain Specified to I_C = 1.0 Amp
- Complement to NPN 2N4921, 2N4922, 2N4923

3 AMPERE GENERAL-PURPOSE POWER TRANSISTORS

40-80 VOLTS
30 WATTS



*MAXIMUM RATINGS

Ratings	Symbol	2N4918	2N4919	2N4920	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous (1)	I_C*	1.0 3.0			Adc
Base Current	I_B	1.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 0.24			Watts W/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			°C

THERMAL CHARACTERISTICS (2)

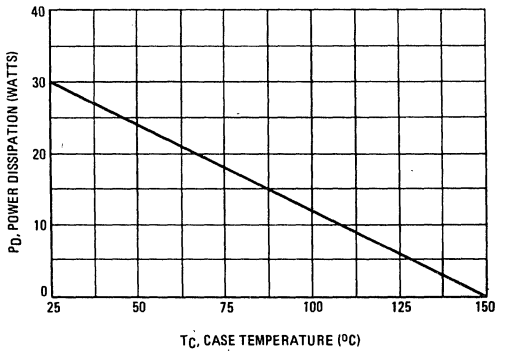
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

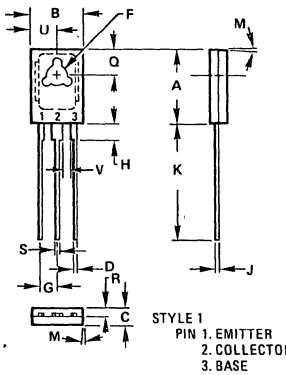
*Indicates JEDEC Registered Data for 2N4918 Series

(1) The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements. The 3.0 Amp maximum value is based upon actual current-handling capability of the device (See Figure 5).

(2) Recommend use of thermal compound for lowest thermal resistance.

FIGURE 1 – POWER DERATING





STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)	–	$V_{CEO(sus)}$			Vdc
(I_C = 0.1 Adc, I_B = 0) 2N4918			40	–	
2N4919			60	–	
2N4920			80	–	
Collector Cutoff Current	–	I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0) 2N4918			–	0.5	
(V_{CE} = 30 Vdc, I_B = 0) 2N4919			–	0.5	
(V_{CE} = 40 Vdc, I_B = 0) 2N4920			–	0.5	
Collector Cutoff Current	13	I_{CEX}			mAdc
(V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc)			–	0.1	
(V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)			–	0.5	
Collector Cutoff Current	–	I_{CBO}			mAdc
(V_{CB} = Rated V_{CB}, I_E = 0)			–	0.1	
Emitter Cutoff Current	–	I_{EBO}	–	1.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS					
DC Current Gain (1)	9	h_{FE}			–
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)			40	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			20	100	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)			10	–	
Collector-Emitter Saturation Voltage (1)	10	$V_{CE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)	12		–	0.6	
	14				
Base-Emitter Saturation Voltage (1)	12	$V_{BE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)	14		–	1.3	
Base-Emitter On Voltage (1)	12	$V_{BE(on)}$			Vdc
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	14		–	1.3	
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain – Bandwidth Product	–	f_T			MHz
(I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)			3.0	–	
Output Capacitance	–	C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)			–	100	
Small-Signal Current Gain	–	h_{fe}			–
(I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)			25	–	

*Indicates JEDEC Registered Data

(1) Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

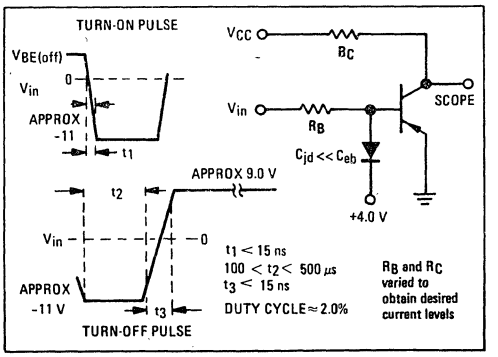


FIGURE 3 – TURN-ON TIME

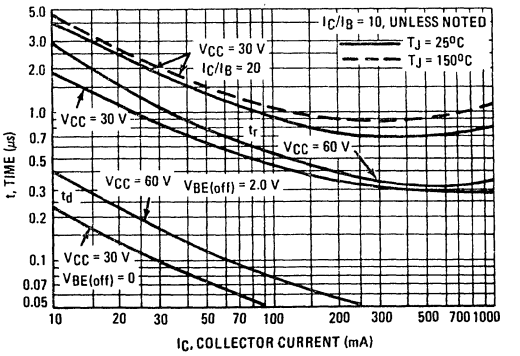
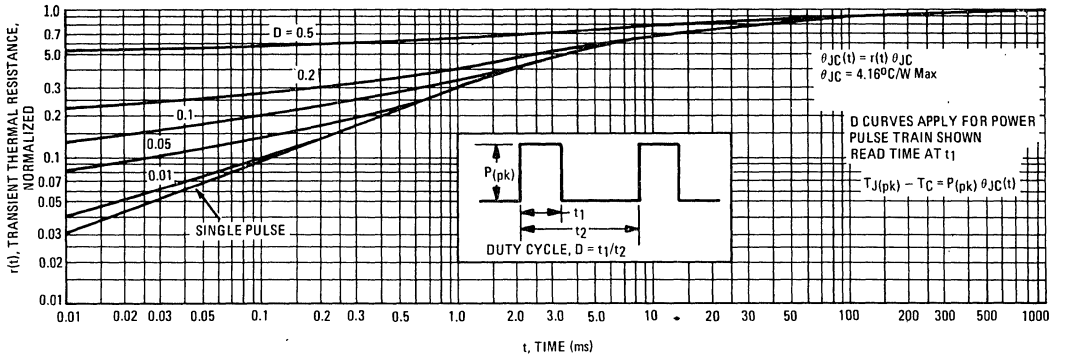
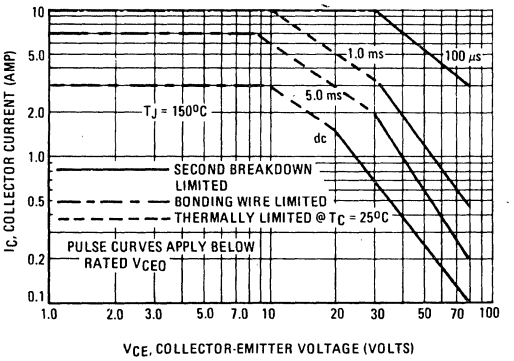


FIGURE 4 – THERMAL RESPONSE



4

FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – STORAGE TIME

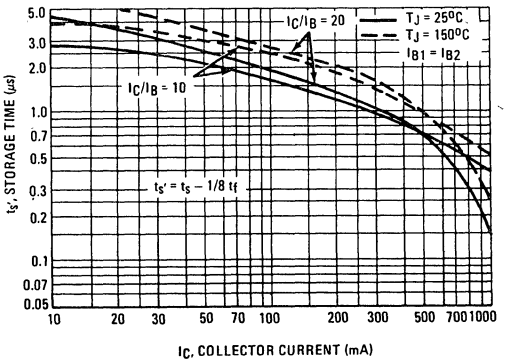
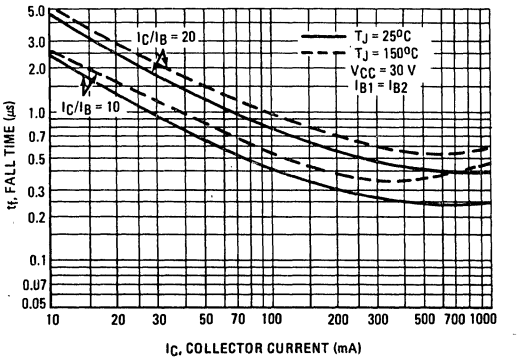


FIGURE 7 – FALL TIME



TYPICAL DC CHARACTERISTICS

FIGURE 8 – CURRENT GAIN

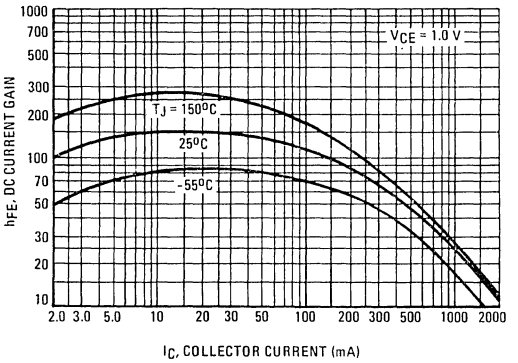


FIGURE 9 – COLLECTOR SATURATION REGION

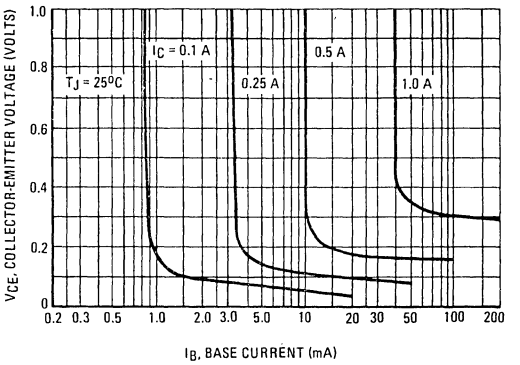


FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

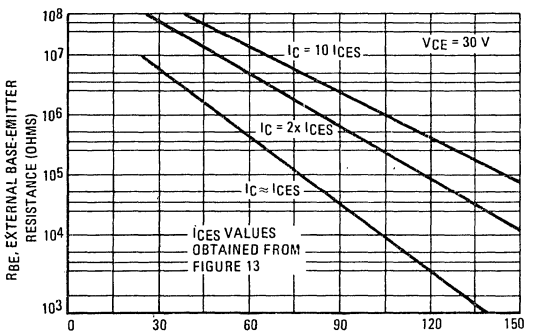


FIGURE 11 – "ON" VOLTAGE

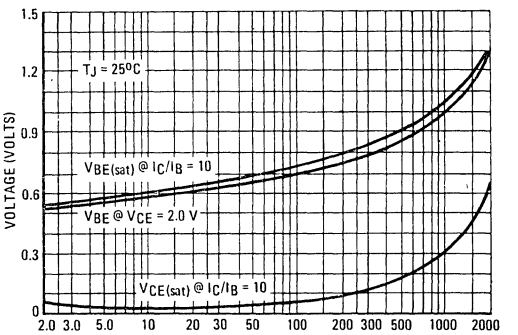


FIGURE 12 – COLLECTOR CUTOFF REGION

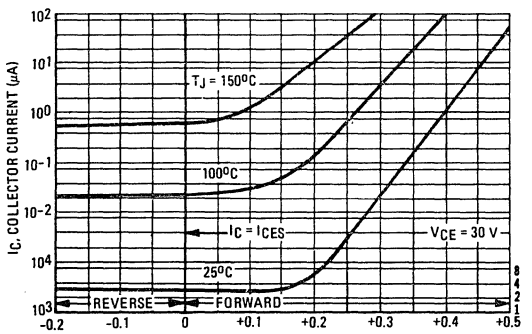
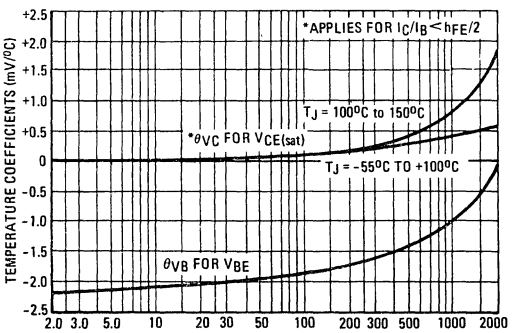


FIGURE 13 – TEMPERATURE COEFFICIENTS



2N4921 thru 2N4923 (SILICON)

4

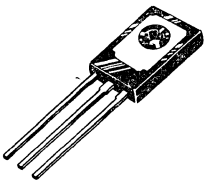
MEDIUM-POWER PLASTIC NPN SILICON TRANSISTORS

. . . designed for driver circuits, switching, and amplifier applications. These high-performance plastic devices feature:

- Low Saturation Voltage — $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 1.0 Amp
- Excellent Power Dissipation Due to Thermopad Construction — P_D = 30 W @ T_C = 25°C
- Excellent Safe Operating Area
- Gain Specified to I_C = 1.0 Amp
- Complement to PNP 2N4918, 2N4919, 2N4920

3 AMPERE GENERAL-PURPOSE POWER TRANSISTORS

40-80 VOLTS
30 WATTS



*MAXIMUM RATINGS

Rating	Symbol	2N4921	2N4922	2N4923	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous (1)	I_C	1.0 3.0			Adc
Base Current — Continuous	I_B	1.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 0.24			Watts W/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150			°C

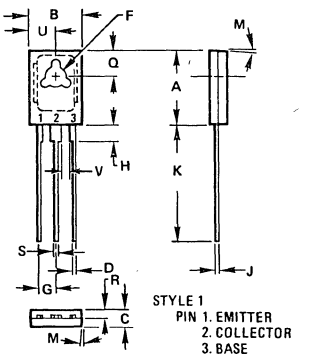
THERMAL CHARACTERISTICS (2)

Characteristic	Symbol		Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

(1) The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements. The 3.0 Amp maximum value is based upon actual current-handling capability of the device (see Figures 5 and 6).

(2) Recommend use of thermal compound for lowest thermal resistance.

*Indicates JEDEC Registered Data.

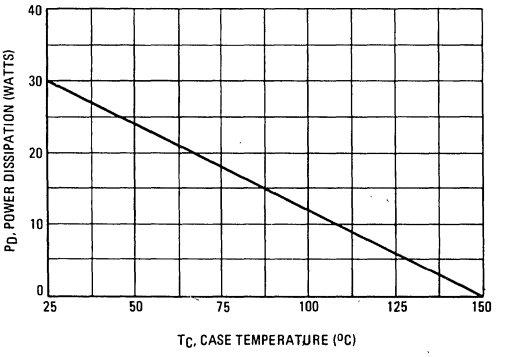


STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	—	0.040	—

CASE 77-04
TO-126

FIGURE 1 — POWER DERATING



Safe Area Curves are indicated by Figure 5 All limits are applicable and must be observed

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Figure No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1)		–	$V_{CEO(sus)}$			Vdc
(I_C = 0.1 Adc, I_B = 0)	2N4921			40	–	
	2N4922			60	–	
	2N4923			80	–	
Collector Cutoff Current		–	I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N4921			–	0.5	
(V_{CE} = 30 Vdc, I_B = 0)	2N4922			–	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	2N4923			–	0.5	
Collector Cutoff Current		13	I_{CEX}			mAdc
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc)				–	0.1	
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)				–	0.5	
Collector Cutoff Current		–	I_{CBO}			mAdc
(V_{CB} = Rated V_{CB}, I_E = 0)				–	0.1	
Emitter Cutoff Current		–	I_{EBO}			mAdc
(V_{EB} = 5.0 Vdc, I_C = 0)				–	1.0	
ON CHARACTERISTICS						
DC Current Gain (1)		9	h_{FE}			–
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)				40	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)				20	100	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)				10	–	
Collector-Emitter Saturation Voltage (1)		10	$V_{CE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)		12		–	0.6	
		14				
Base-Emitter Saturation Voltage (1)		12	$V_{BE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)		14		–	1.3	
Base-Emitter On Voltage (1)		12	$V_{BE(on)}$			Vdc
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		14		–	1.3	
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain – Bandwidth Product		–	f_T			MHz
(I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)				3.0	–	
Output Capacitance		–	C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)				–	100	
Small-Signal Current Gain		–	h_{fe}			–
(I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)				25	–	

(1) Pulse Test: PW≈300 μs, Duty Cycle≈2.0%.
*Indicates JEDEC Registered Data

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

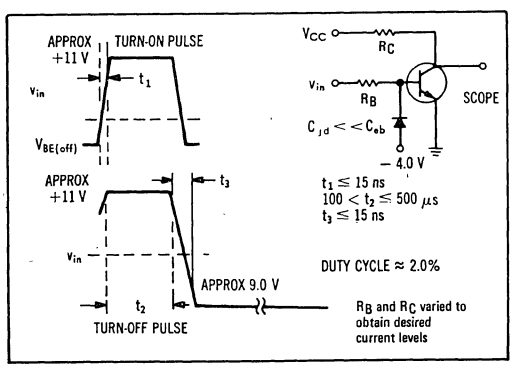


FIGURE 3 – TURN-ON TIME

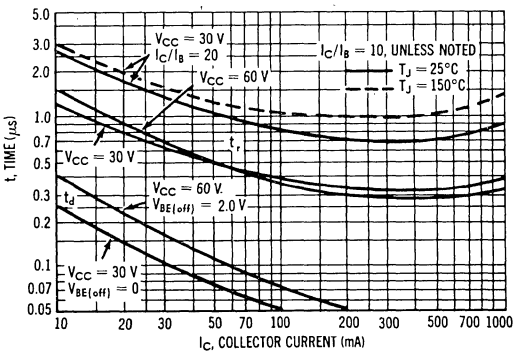


FIGURE 4 – THERMAL RESPONSE

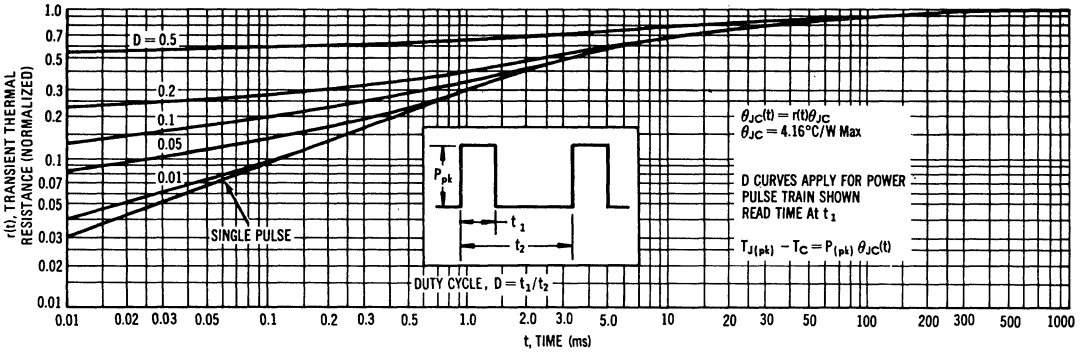


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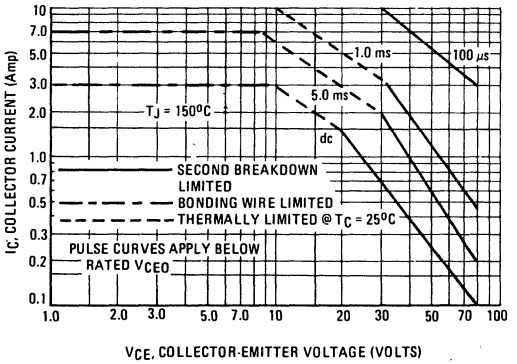
FIGURE 5 – ACTIVE – REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – STORAGE TIME

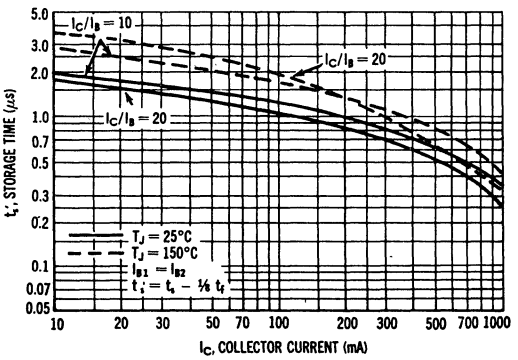


FIGURE 7 – FALL TIME

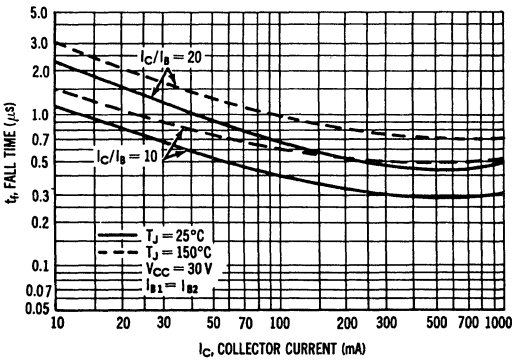


FIGURE 8 – CURRENT GAIN

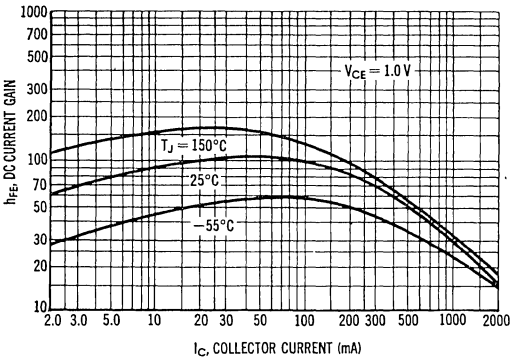


FIGURE 9 – COLLECTOR SATURATION REGION

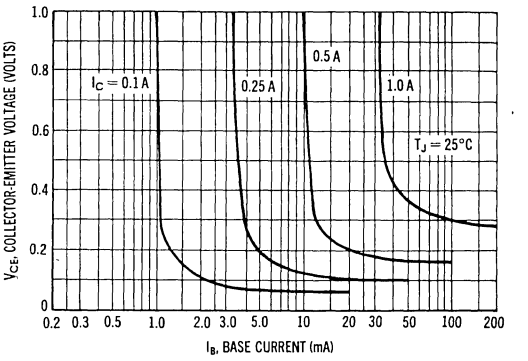


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FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

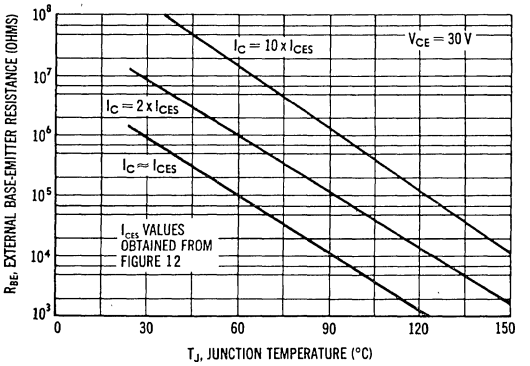


FIGURE 11 – "ON" VOLTAGE

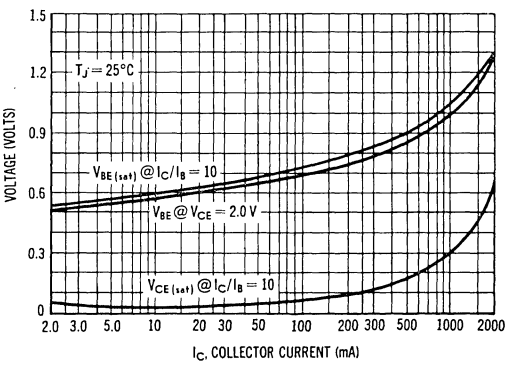


FIGURE 12 – COLLECTOR CUTOFF REGION

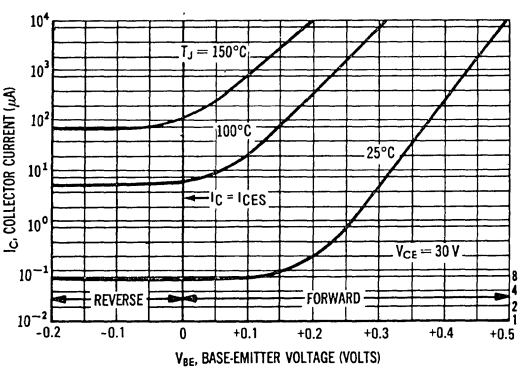
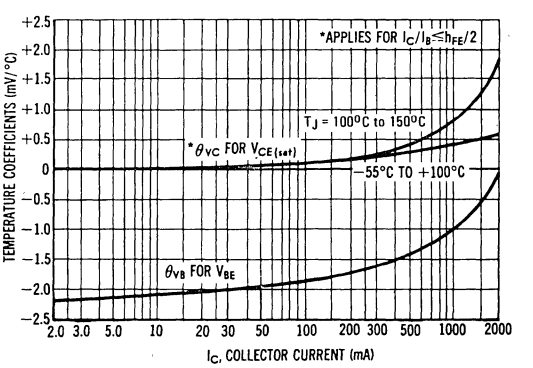


FIGURE 13 – TEMPERATURE COEFFICIENTS



2N5038
2N5039

4

NPN SILICON TRANSISTORS

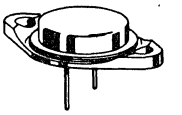
. . . fast switching speeds and high current capacity ideally suit these parts for use in switching regulators, inverters, wide-band amplifiers and power oscillators in industrial and commercial applications.

- High Speed – t_f = 0.5 μs (Max)
- High Current – $I_{C(max)}$ = 30 Amps
- Low Saturation – $V_{CE(sat)}$ = 2.5 V (Max) @ I_C = 20 Amps

20 AMPERE

NPN SILICON POWER TRANSISTORS

120 and 150 VOLTS
140 WATTS



*MAXIMUM RATINGS

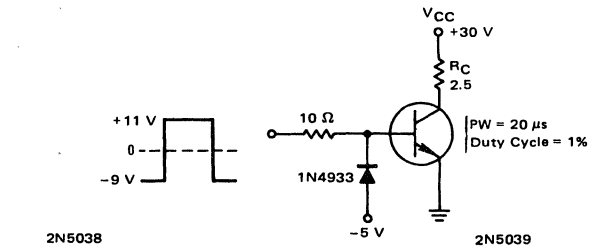
Rating	Symbol	2N5038	2N5039	Unit
Collector-Base Voltage	V_{CBO}	150	120	Vdc
Collector-Emitter Voltage	V_{CEV}	150	120	Vdc
Emitter-Base Voltage	V_{EBO}	7		Vdc
Collector Current – Continuous Peak (1)	I_C I_{CM}	20 30		Adc
Base Current – Continuous	I_B	5		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	140 0.8		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W

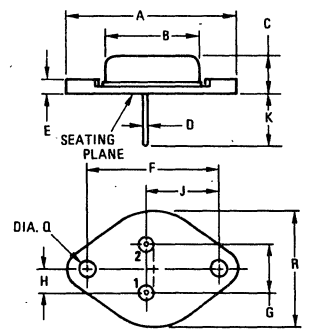
*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 10 ms, Duty Cycle ≤ 50%.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



2N5038
I_C = 12 Amps
I_{B1} = I_{B2} = 1.2 Amps

2N5039
I_C = 10 Amps
I_{B1} = I_{B2} = 1.0 Amps



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

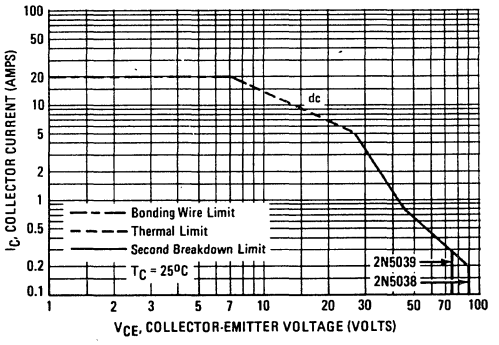
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C *unless otherwise noted*).

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N5038		90	–	
	2N5039		75	–	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 V)	2N5038		–	50	
(V_{CE} = 110 Vdc, $V_{BE(off)}$ = 1.5 V)	2N5039		–	50	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5038		–	10	
(V_{CE} = 85 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5039		–	10	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{EB} = 5 Vdc, I_C = 0)	2N5038		–	5	
	2N5039		–	15	
(V_{EB} = 7 Vdc, I_C = 0)	Both		–	50	
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 12 Adc, V_{CE} = 5 Vdc)	2N5038		20	100	
(I_C = 10 Adc, V_{CE} = 5 Vdc)	2N5039		20	100	
Collector-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 5 Adc)		$V_{CE(sat)}$	–	2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 5 Adc)		$V_{BE(sat)}$	–	3.3	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common-Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio (I_C = 2 Adc, V_{CE} = 10 Vdc, f = 5 MHz)		$\lvert h_{fe} \rvert$	12	–	–
SWITCHING CHARACTERISTICS					
RESISTIVE LOAD					
Rise Time	(V_{CC} = 30 Vdc)	t_r	–	0.5	μs
Storage Time	(I_C = 12 Adc, I_{B1} = I_{B2} = 1.2 Adc) 2N5038	t_s	–	1.5	μs
Fall Time	(I_C = 10 Adc, I_{B1} = I_{B2} = 1 Adc) 2N5039	t_f	–	0.5	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

FIGURE 2 – FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Second breakdown pulse limits are valid for duty cycles to 10%. At high case temperatures, thermal limitations may reduce the power that can be handled to values less than the limitations imposed by second breakdown.

2N5050 (SILICON)
2N5051
2N5052

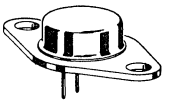
MEDIUM-POWER NPN SILICON TRANSISTORS

. . . designed for untuned amplifier and switching applications.

- High Voltage Ratings –
  V_{CEO} = 125, 150 and 200 Vdc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 0.75 Adc
- Packaged in the Compact, High Efficiency TO-66 Case

2 AMPERE
POWER TRANSISTORS
NPN SILICON

125-200 VOLTS
40 WATTS



*MAXIMUM RATINGS

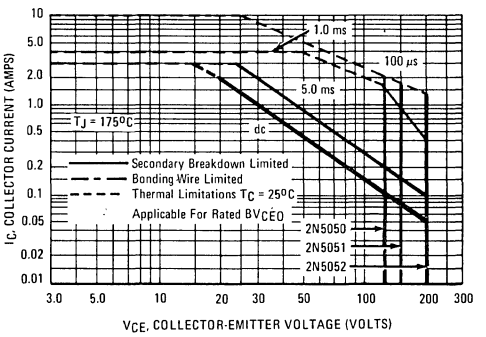
Rating	Symbol	2N5050	2N5051	2N5052	Unit
Collector-Emitter Voltage	V_{CEO}	125	150	200	Vdc
Collector-Base Voltage	V_{CB}	125	150	200	Vdc
Emitter-Base Voltage	V_{EB}		6.0		Vdc
Collector Current – Continuous	I_C		2.0		Adc
Base Current	I_B		1.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		40 0.266		Watts W/°C
Operating Junction Temperature Range	T_J		-65 to +175		°C
Storage Temperature Range	T_{stg}		-65 to +200		°C

*THERMAL CHARACTERISTICS

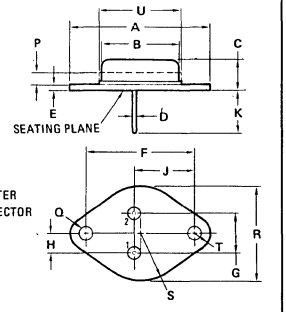
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.76	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

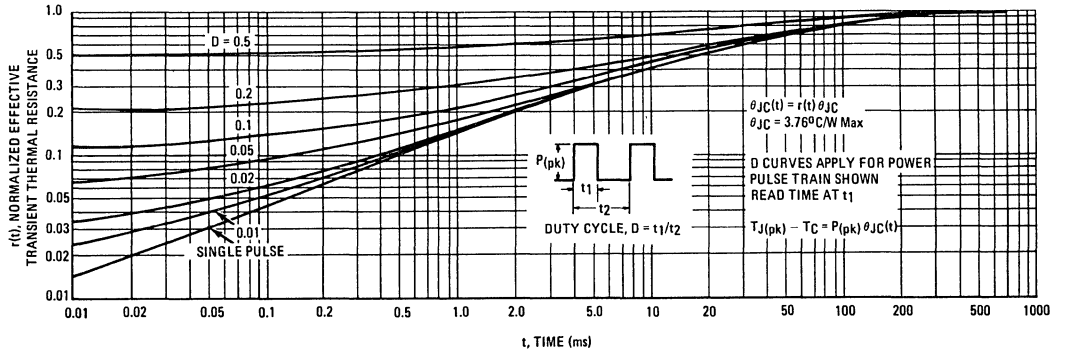
CASE 80-02
TO-66

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (Note 1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N5050		125	–	
	2N5051		150	–	
	2N5052		200	–	
Collector-Emitter Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 62.5 Vdc, I_B = 0)	2N5050		–	0.1	
(V_{CE} = 75 Vdc, I_B = 0)	2N5051		–	0.1	
(V_{CE} = 100 Vdc, I_B = 0)	2N5052		–	0.1	
Collector-Emitter Cutoff Current		I_{CEX}			mAdc
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc)			–	0.5	
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)			–	5.0	
Emitter-Base Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	mAdc
***ON CHARACTERISTICS**					
DC Current Gain (Note 1)		h_{FE}			–
(I_C = 0.75 Adc, V_{CE} = 5.0 Vdc)			25	100	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)			25	–	
(I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)			5.0	–	
Collector-Emitter Saturation Voltage (Note 1)		$V_{CE(sat)}$			Vdc
(I_C = 0.75 Adc, I_B = 0.1 Adc)			–	1.0	
(I_C = 2.0 Adc, I_B = 0.4 Adc)			–	5.0	
Base-Emitter On Voltage (Note 1) (I_C = 0.75 Adc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	1.2	Vdc
***DYNAMIC CHARACTERISTICS**					
Current-Gain–Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 5.0 MHz)		f_T	10	–	MHz
Small-Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–
Common Base Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	250	pF
***SWITCHING CHARACTERISTICS**					
Rise Time	(V_{CC} = 120 Vdc, I_C = 750 mAdc, R_L = 150 Ohms, I_{B1} = I_{B2} = 100 mAdc)	t_r	–	300	ns
Storage Time		t_s	–	3.5	μs
Fall Time		t_f	–	1.2	μs

*Indicates JEDEC Registered Data. Note 1: Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

FIGURE 2 – THERMAL RESPONSE



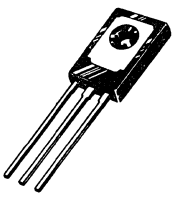
2N5190 thru 2N5192 (SILICON)

SILICON NPN POWER TRANSISTORS

. . . for use in power amplifier and switching circuits, – excellent safe area limits. Complement to PNP 2N5193, 2N5194, 2N5195

4 AMPERE
POWER TRANSISTORS
SILICON NPN

40-80 VOLTS
40 WATTS



*MAXIMUM RATINGS

Rating	Symbol	2N5190	2N5191	2N5192	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current	I_C	← 4.0 →			Adc
Base Current	I_B	← 1.0 →			Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	40 320			Watts mW/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			^oC

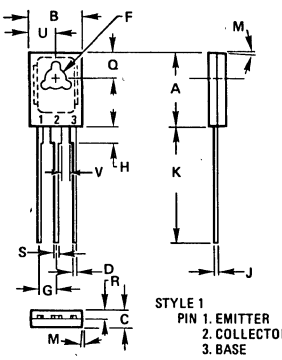
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	$^oC/W$

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 0.1 Adc, I_B = 0)	2N5190		40	–	
	2N5191		60	–	
	2N5192		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N5190		–	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N5191		–	1.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N5192		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5190		–	0.1	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5191		–	0.1	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5192		–	0.1	
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5190		–	2.0	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5191		–	2.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5192		–	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N5190		–	0.1	
(V_{CB} = 60 Vdc, I_E = 0)	2N5191		–	0.1	
(V_{CB} = 80 Vdc, I_E = 0)	2N5192		–	0.1	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)			–	1.0	
ON CHARACTERISTICS					
DC Current Gain(1)		h_{FE}			–
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	2N5190		25	100	
	2N5191		25	100	
	2N5192		20	80	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	2N5190		10	–	
	2N5191		10		
	2N5192		7.0	–	
Collector-Emitter Saturation Voltage(1)		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 0.15 Adc)			–	0.6	
(I_C = 4.0 Adc, I_B = 1.0 Adc)			–	1.4	
Base-Emitter On Voltage (1)		$V_{BE(on)}$			Vdc
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)			–	1.2	
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product		f_T			MHz
(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)			2.0	–	

(1)Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.
*Indicates JEDEC Registered Data



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

FIGURE 1 – DC CURRENT GAIN

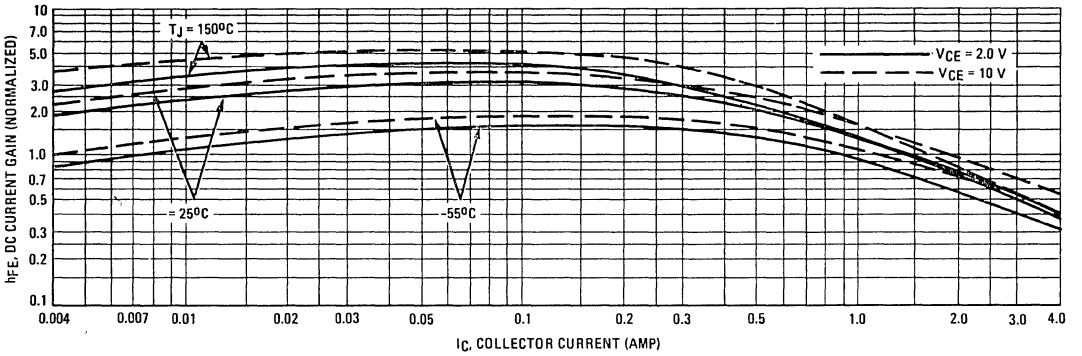


FIGURE 2 – COLLECTOR SATURATION REGION

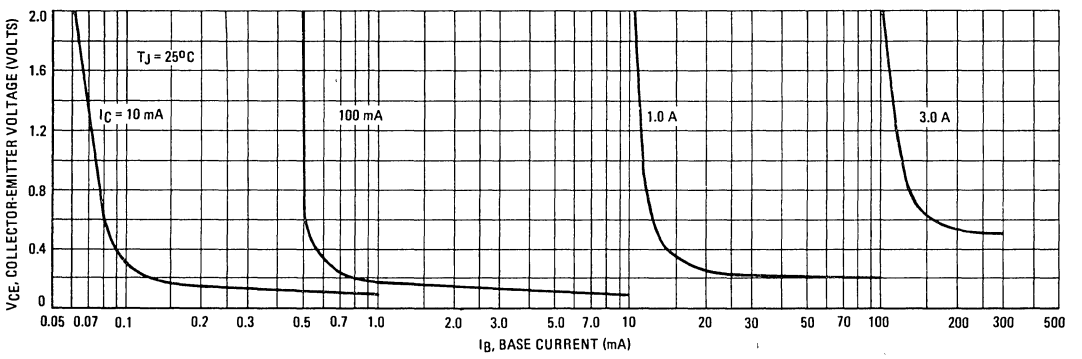


FIGURE 3 – "ON" VOLTAGES

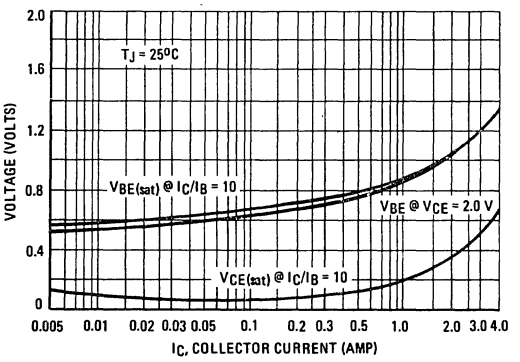


FIGURE 4 – TEMPERATURE COEFFICIENTS

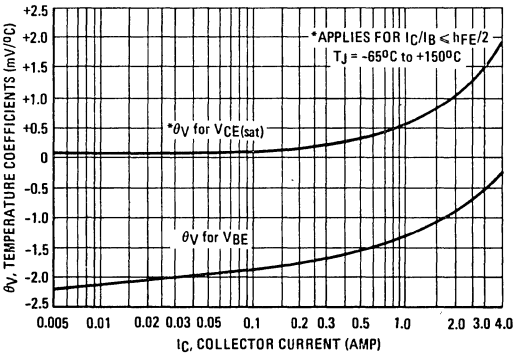


FIGURE 5 – COLLECTOR CUT-OFF REGION

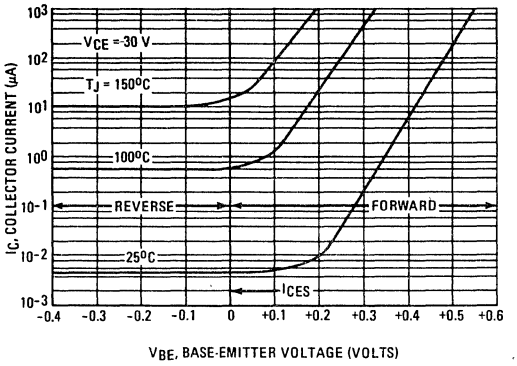


FIGURE 6 – EFFECTS OF BASE-EMITTER RESISTANCE

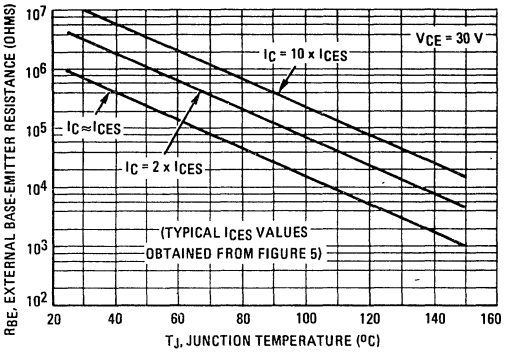


FIGURE 7 – SWITCHING TIME EQUIVALENT CIRCUIT

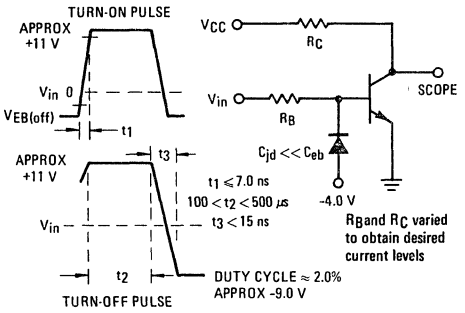


FIGURE 8 – CAPACITANCE

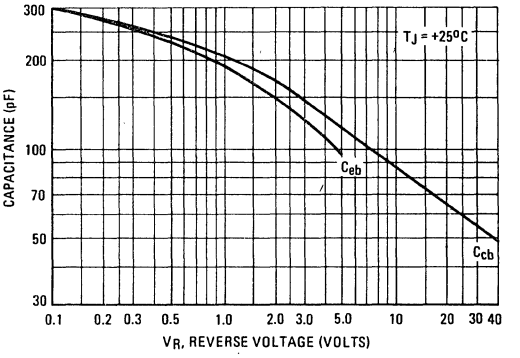


FIGURE 9 – TURN-ON TIME

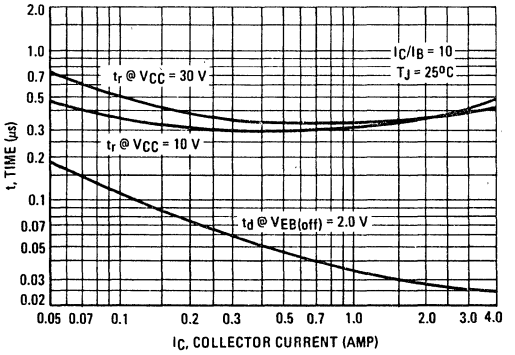


FIGURE 10 – TURN-OFF TIME

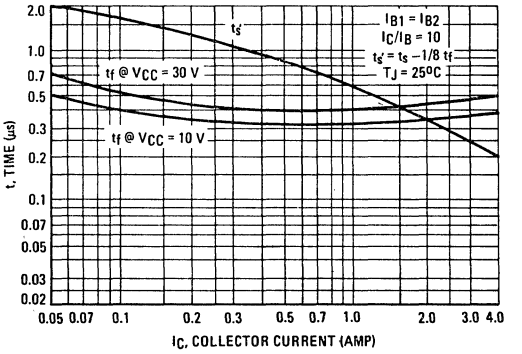
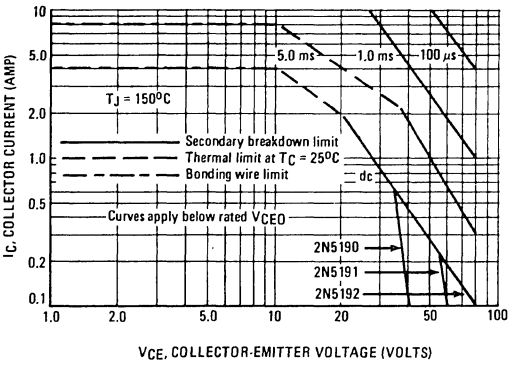


FIGURE 11 RATING AND THERMAL DATA
ACTIVE-REGION SAFE OPERATING AREA

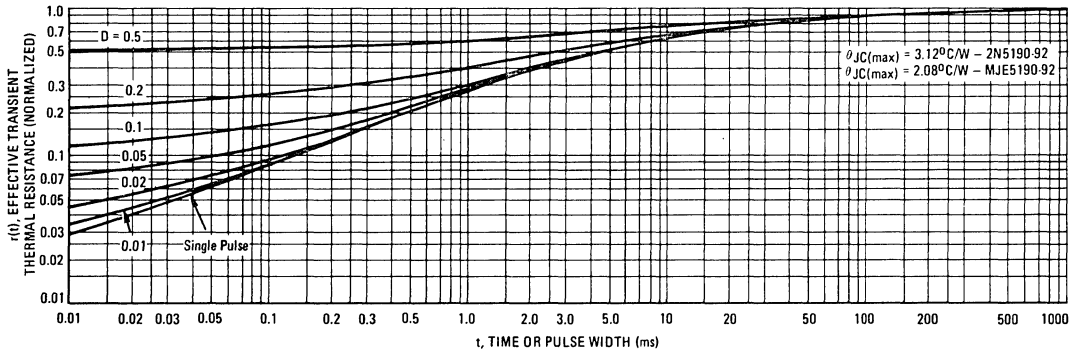


There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

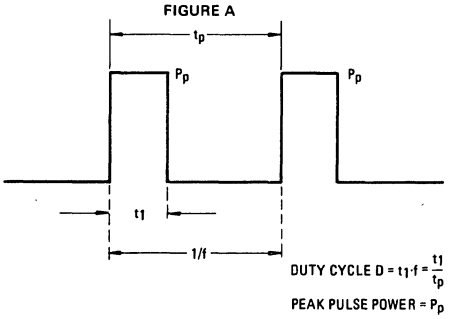
4

FIGURE 12 – THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

FIGURE A



A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC}.

Example:

The 2N5190 is dissipating 50 watts under the following conditions: t_1 = 0.1 ms, t_p = 0.5 ms. (D = 0.2).

Using Figure 12, at a pulse width of 0.1 ms and D = 0.2, the reading of r(t_1, D) is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_P \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2°C$$

2N5193 thru 2N5195 (SILICON)

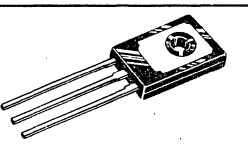
4

SILICON PNP POWER TRANSISTORS

. . . for use in power amplifier and switching circuits, – excellent safe area limits. Complement to NPN 2N5190, 2N5191, 2N5192

4 AMPERE
POWER TRANSISTORS
SILICON PNP

40-80 VOLTS
40 WATTS



*MAXIMUM RATINGS

Rating	Symbol	2N5193	2N5194	2N5195	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	◄——— 5.0 ———		———►	Vdc
Collector Current	I_C	◄——— 4.0 ———		———►	Adc
Base Current	I_B	◄——— 1.0 ———		———►	Adc
Total Power Dissipation @ $T_C = 25^oC$	P_D	◄——— 40 ———		———►	Watts
Derate above 25^oC		◄——— 320 ———		———►	$mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	◄——— -65 to +150 ———		———►	$^oC/W$

THERMAL CHARACTERISTICS

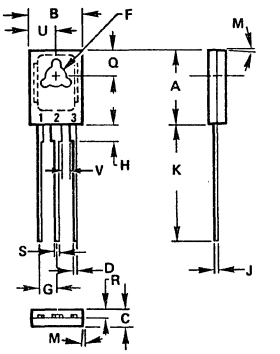
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	$^oC/W$

*ELECTRICAL CHARACTERISTICS ($T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 0.1 Adc, I_B = 0)	2N5193		40	–	
	2N5194		60	–	
	2N5195		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N5193		–	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N5194		–	1.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N5195		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5193		–	0.1	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5194		–	0.1	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5195		–	0.1	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 125^oC$)	2N5193		–	2.0	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 125^oC$)	2N5194		–	2.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, $T_C = 125^oC$)	2N5195		–	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N5193		–	0.1	
(V_{CB} = 60 Vdc, I_E = 0)	2N5194		–	0.1	
(V_{CB} = 80 Vdc, I_E = 0)	2N5195		–	0.1	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)			–	1.0	
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	2N5193		25	100	
	2N5194		25	100	
	2N5195		20	80	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	2N5193		10	–	
	2N5194		10	–	
	2N5195		7.0	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 0.15 Adc)			–	0.6	
(I_C = 4.0 Adc, I_B = 1.0 Adc)			–	1.4	
Base-Emitter On Voltage (1)		$V_{BE(on)}$			Vdc
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)			–	1.2	
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product		f_T			MHz
(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)			2.0	–	

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

FIGURE 1 – DC CURRENT GAIN

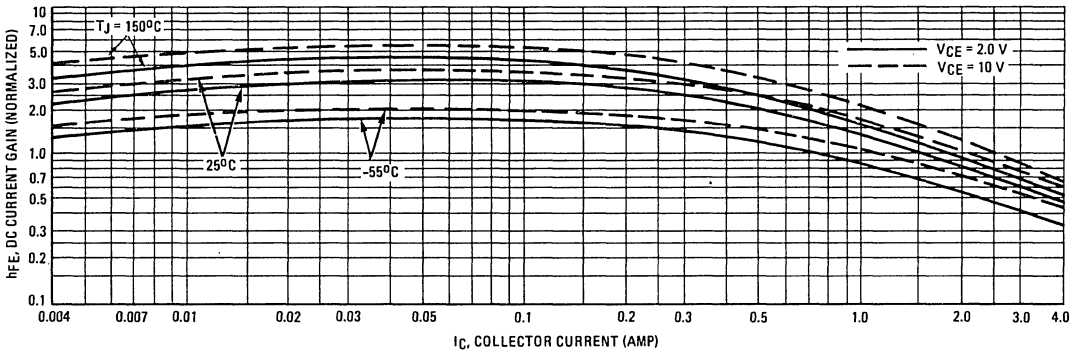


FIGURE 2 – COLLECTOR SATURATION REGION

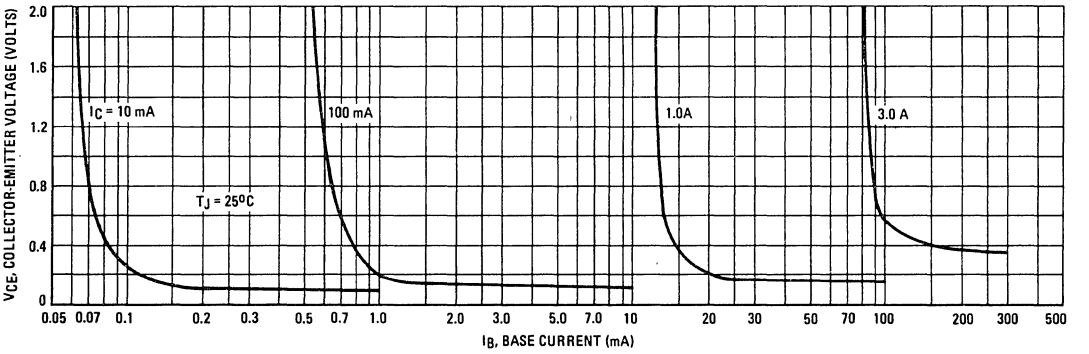


FIGURE 3 – "ON" VOLTAGE

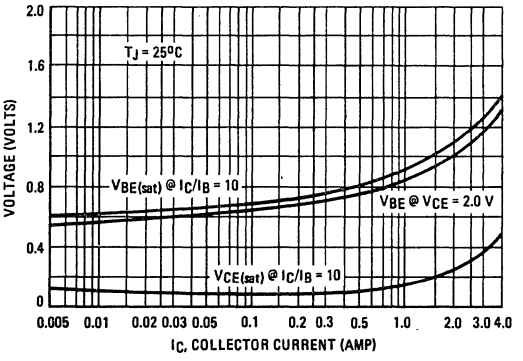


FIGURE 4 – TEMPERATURE COEFFICIENTS

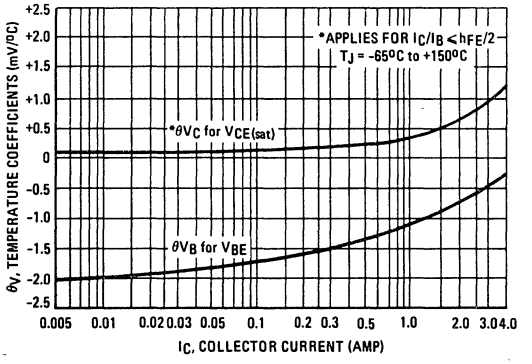


FIGURE 5 – COLLECTOR CUT-OFF REGION

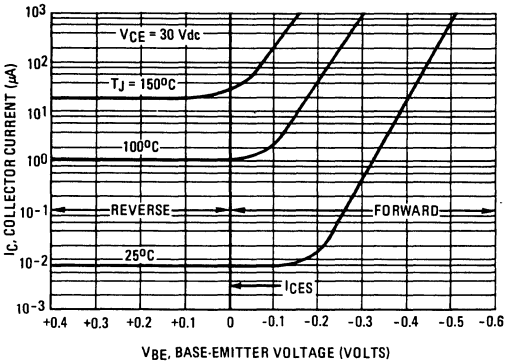


FIGURE 6 – EFFECTS OF BASE-EMITTER RESISTANCE

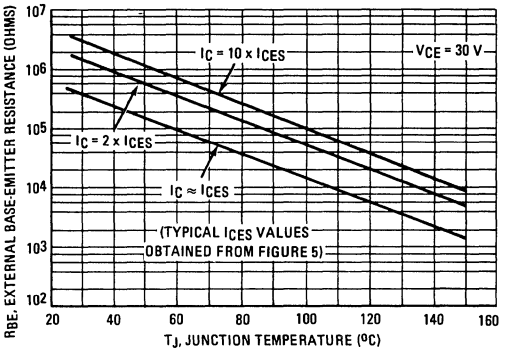


FIGURE 7 – SWITCHING TIME EQUIVALENT CIRCUIT

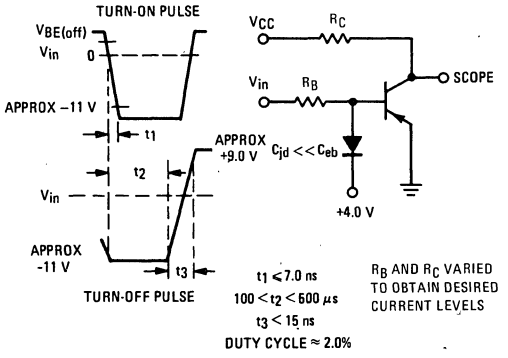


FIGURE 8 – CAPACITANCE

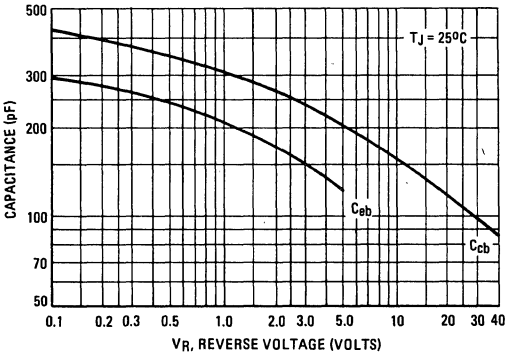


FIGURE 9 – TURN-ON TIME

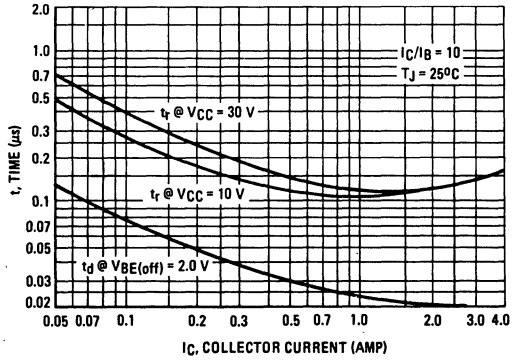


FIGURE 10 – TURN-OFF TIME

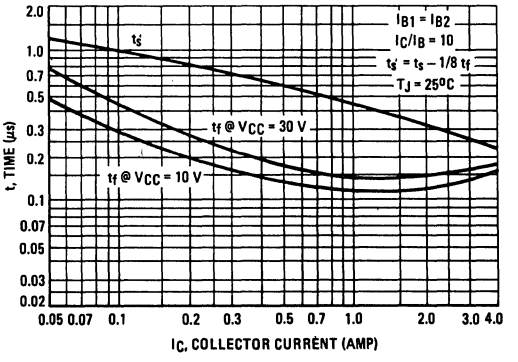
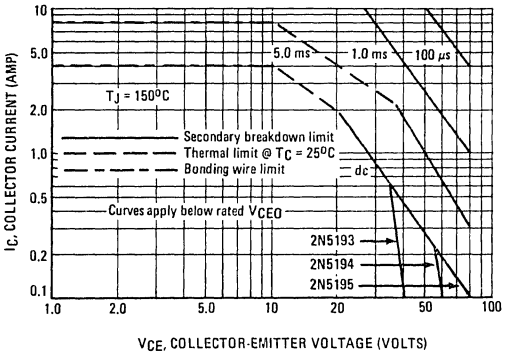


FIGURE 11

RATING AND THERMAL DATA
ACTIVE-REGION SAFE OPERATING AREA



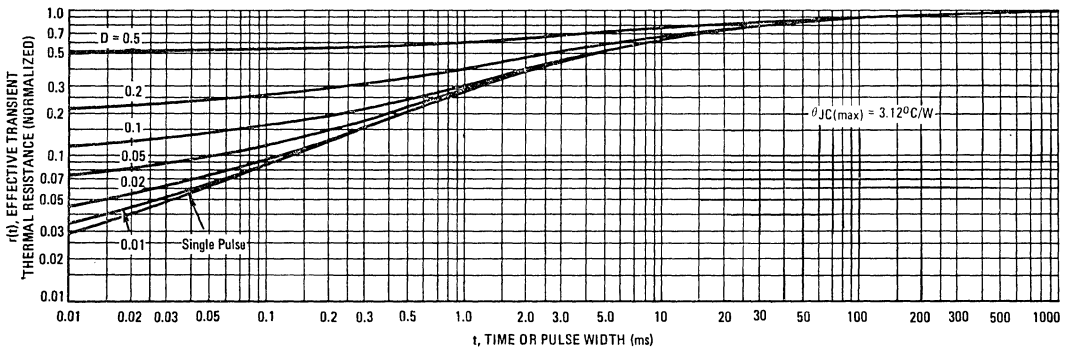
Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_{J(pk)}$ = 150°C. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high-case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

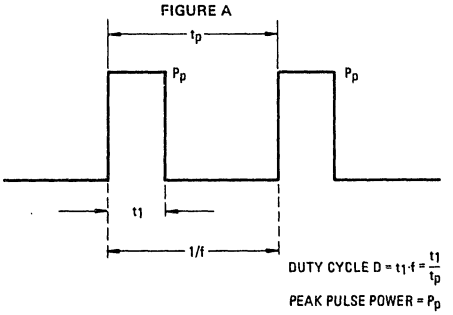
4

FIGURE 12 — THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

FIGURE A



A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC}.

Example:

The 2N5193 is dissipating 50 watts under the following conditions: t_1 = 0.1 ms, tp = 0.5 ms. (D = 0.2).

Using Figure 12, at a pulse width of 0.1 ms and D = 0.2, the reading of $r(t_1, D)$ is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_P \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2°C$$

2N5301
2N5302
2N5303

HIGH-POWER NPN SILICON TRANSISTORS

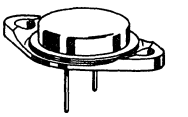
. . . for use in power amplifier and switching circuits applications.

- High Collector-Emitter Sustaining Voltage –
  $BV_{CEO(sus)}$ = 80 Vdc (Min) @ I_C = 200 mAdc (2N5303)
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.75 Vdc (Max) @ I_C = 10 Adc (2N5301, 2N5302)
  1.0 Vdc (Max) @ I_C = 10 Adc (2N5303)
- Excellent Safe Operating Area –
  200 Watt dc Power Rating to 30 Vdc (2N5303)
- Complements to PNP 2N4398, 2N4399 and 2N5745

20 AND 30 AMPERE POWER TRANSISTORS

NPN SILICON

40-60-80 VOLTS
200 WATTS



*MAXIMUM RATINGS

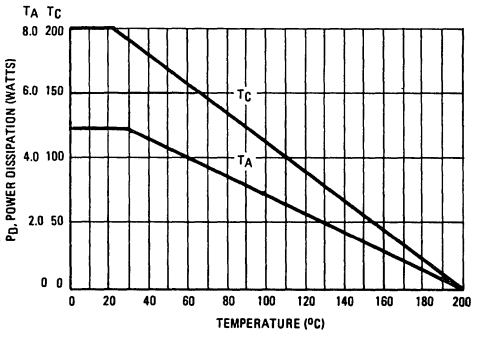
Rating	Symbol	2N5301	2N5302	2N5303	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Collector Current – Continuous	I_C	30	30	20	Adc
Base Current	I_B	← 7.5 →			Adc
Total Device Dissipation @ T_C=25°C Derate above 25°C	P_D	← 200 → ← 1.14 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	← -65 to +200 →			°C

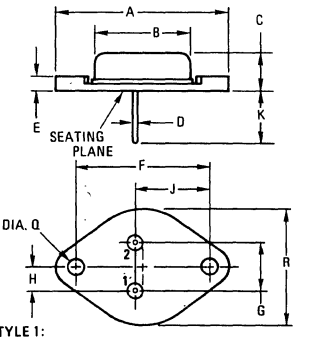
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W
Thermal Resistance, Case to Ambient	θ_{CA}	34	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER TEMPERATURE DERATING CURVE





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (Note 1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N5301		40	–	
	2N5302		60	–	
	2N5303		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N5301		–	5.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N5302		–	5.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N5303		–	5.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5301		–	1.0	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5302		–	1.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5303		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5301		–	10	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5302		–	10	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5303		–	10	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N5301		–	1.0	
(V_{CB} = 60 Vdc, I_E = 0)	2N5302		–	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	2N5303		–	1.0	
Emitter Cutoff Current		I_{EBO}	–	5.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS					
DC Current Gain (Note 1)		h_{FE}			–
*(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	ALL TYPES		40	–	
*(I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5303		15	60	
*(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N5301,2N5302		15	60	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)	2N5303		5.0	–	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N5301,2N5302		5.0	–	
*Collector-Emitter Saturation Voltage (Note 1)		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)	2N5301,2N5302		–	0.75	
(I_C = 10 Adc, I_B = 1.0 Adc)	2N5303		–	1.0	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N5303		–	1.5	
(I_C = 20 Adc, I_B = 2.0 Adc)	2N5301,2N5302		–	2.0	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5303		–	2.0	
(I_C = 30 Adc, I_B = 6.0 Adc)	2N5301,2N5302		–	3.0	
*Base-Emitter Saturation Voltage (Note 1)		$V_{BE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)	ALL TYPES		–	1.7	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N5301,2N5302		–	1.8	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N5303		–	2.0	
(I_C = 20 Adc, I_B = 2.0 Adc)	2N5301,2N5302		–	2.5	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5303		–	2.5	
*Base-Emitter On Voltage (Note 1)		$V_{BE(on)}$			Vdc
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5303		–	1.5	
(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N5301,2N5302		–	1.7	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)	2N5303		–	2.5	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N5301,2N5302		–	3.0	
***DYNAMIC CHARACTERISTICS**					
Current-Gain–Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	2.0	–	MHz
Small-Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	40	–	–
***SWITCHING CHARACTERISTICS**					
Rise Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	t_r	–	1.0	μs
Storage Time		t_s	–	2.0	μs
Fall Time		t_f	–	1.0	μs

*Indicates JEDEC Registered Data.
Note 1: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

SWITCHING TIME EQUIVALENT TEST CIRCUITS

FIGURE 2 – TURN-ON TIME

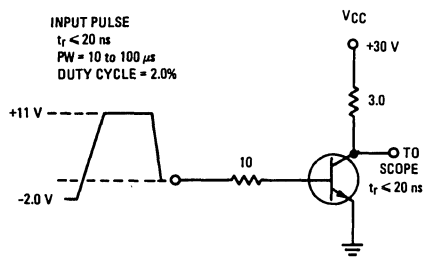
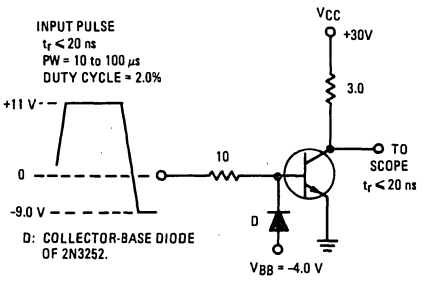


FIGURE 3 – TURN-OFF TIME



D: COLLECTOR-BASE DIODE OF 2N3252.

FIGURE 4 – THERMAL RESPONSE

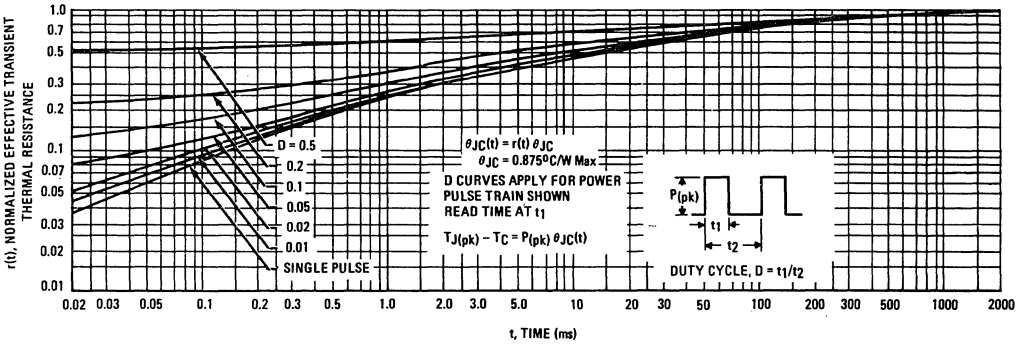


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA

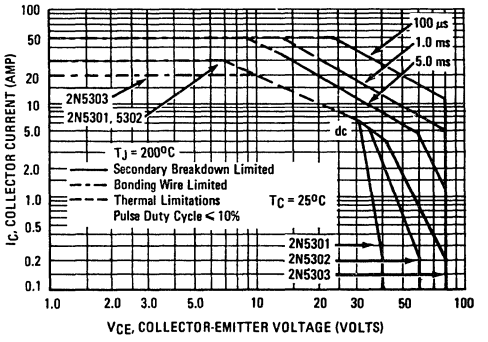


FIGURE 6 – CAPACITANCE versus VOLTAGE

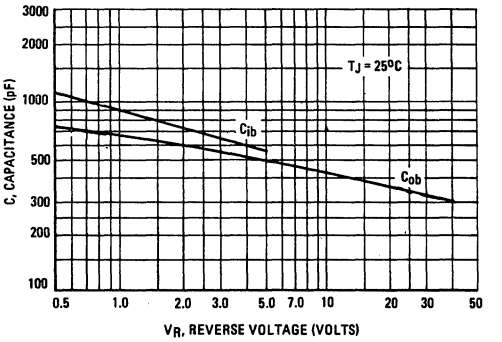


FIGURE 7 – TURN-ON TIME

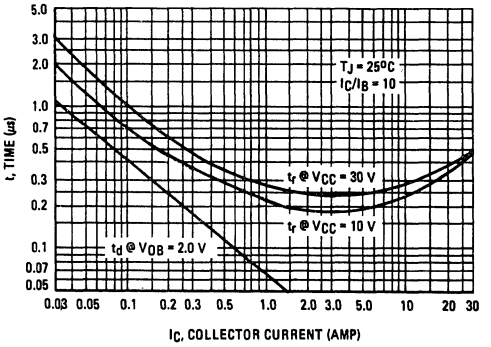


FIGURE 8 – TURN-OFF TIME

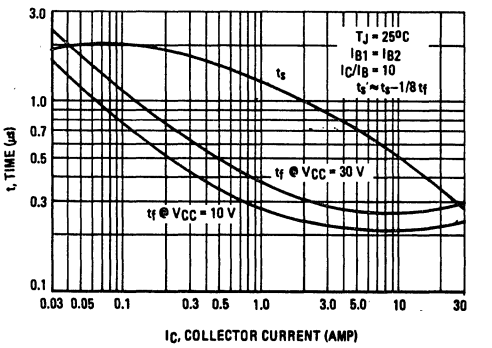


FIGURE 9 – DC CURRENT GAIN

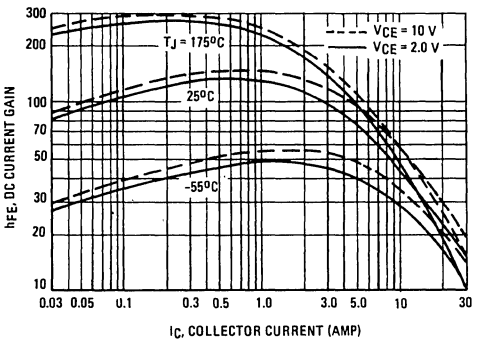


FIGURE 10 – COLLECTOR SATURATION REGION

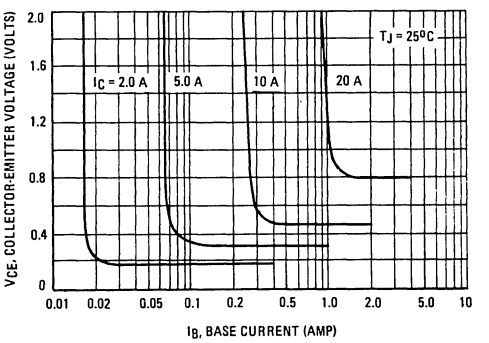


FIGURE 11 – EFFECTS OF BASE-EMITTER RESISTANCE

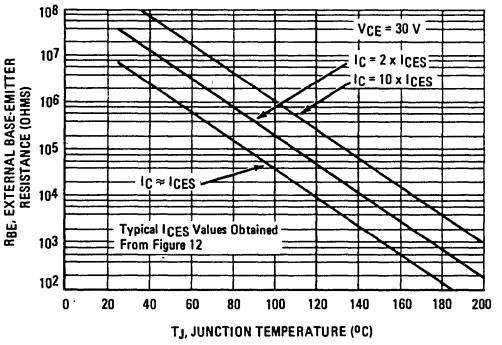


FIGURE 12 – "ON" VOLTAGES

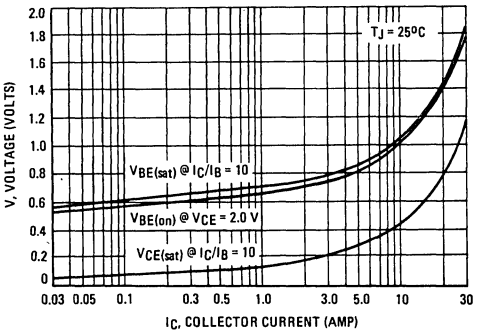


FIGURE 13 – COLLECTOR CUT-OFF REGION

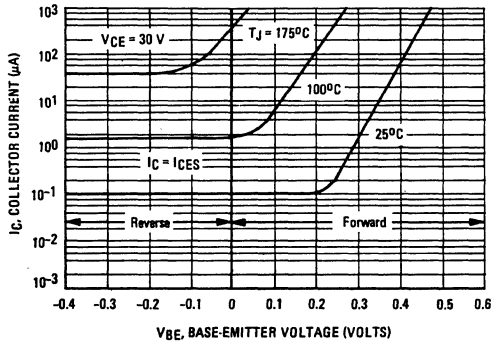
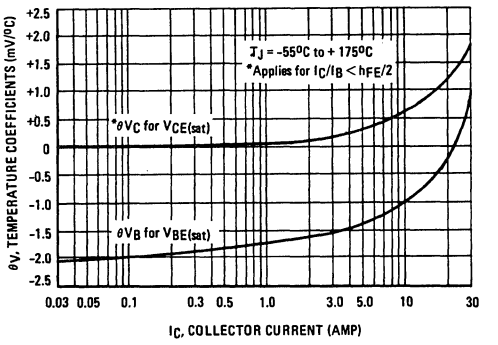


FIGURE 14 – TEMPERATURE COEFFICIENTS



2N5336 thru 2N5339

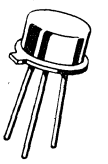
MEDIUM-POWER NPN SILICON TRANSISTORS

. . . designed for switching and wide band amplifier applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 5.0 Amp
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact TO-39 Case for Critical Space-Limited Applications
- Complement to 2N6190 thru 2N6193

5 AMPERE
POWER TRANSISTORS
NPN SILICON

80–100 VOLTS
6 WATTS



4

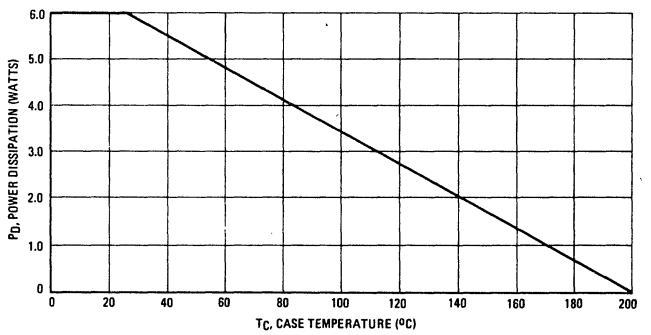
MAXIMUM RATINGS

Rating	Symbol	2N5336 2N5337	2N5338 2N5339	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	5.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	6.0 34.3		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

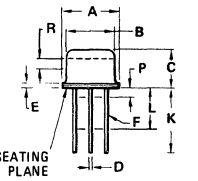
THERMAL CHARACTERISTICS

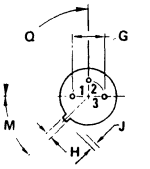
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	29.2	°C/W

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
(TO-39)

ELECTRICAL CHARACTERISTICS (T_C = 25°C, unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage*		–	$BV_{CEO(sus)}$*			Vdc
(I_C = 50 mAdc, I_B = 0)	2N5336, 2N5337			80	–	
	2N5338, 2N5339			100	–	
Collector Cutoff Current		–	I_{CEO}			μAdc
(V_{CE} = 75 Vdc, I_B = 0)	2N5336, 2N5337			–	100	
(V_{CE} = 90 Vdc, I_B = 0)	2N5338, 2N5339			–	100	
Collector Cutoff Current		12	I_{CEX}			μAdc
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5336, 2N5337			–	10	
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5338, 2N5339			–	10	
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5336, 2N5337			–	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5338, 2N5339			–	1.0	
Collector Cutoff Current		–	I_{CBO}			μAdc
(V_{CB} = 80 Vdc, I_E = 0)	2N5336, 2N5337			–	10	
(V_{CB} = 100 Vdc, I_E = 0)	2N5338, 2N5339			–	10	
Emitter Cutoff Current		–	I_{EBO}			μAdc
(V_{BE} = 6.0 Vdc, I_C = 0)				–	100	
ON CHARACTERISTICS						
DC Current Gain*		8	h_{FE}*			–
(I_C = 500 mAdc, V_{CE} = 2.0 Vdc)	2N5336, 2N5338			30	–	
	2N5337, 2N5339			60	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	2N5336, 2N5338			30	120	
	2N5337, 2N5339			60	240	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N5336, 2N5338			20	–	
	2N5337, 2N5339			40	–	
Collector-Emitter Saturation Voltage*		9, 11, 13	$V_{CE(sat)}$*			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	0.7	
(I_C = 5.0 Adc, I_B = 0.5 Adc)				–	1.2	
Base-Emitter Saturation Voltage*		11, 13	$V_{BE(sat)}$*			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	1.2	
(I_C = 5.0 Adc, I_B = 0.5 Adc)				–	1.8	
DYNAMIC CHARACTERISTICS						
Current-Gain–Bandwidth Product		–	f_T			MHz
(I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 10 MHz)				30	–	
Output Capacitance		7	C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)				–	250	
Input Capacitance		7	C_{ib}			pF
(V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)				–	1,000	
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 40 Vdc, $V_{EB(off)}$ = 3.0 Vdc,	2, 3	t_d	–	100	ns
Rise Time	(I_C = 2.0 Adc, I_{B1} = 0.2 Adc)		t_r	–	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc,	2, 6	t_s	–	2.0	μs
Fall Time	I_{B1} = I_{B2} = 0.2 Adc)		t_f	–	200	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

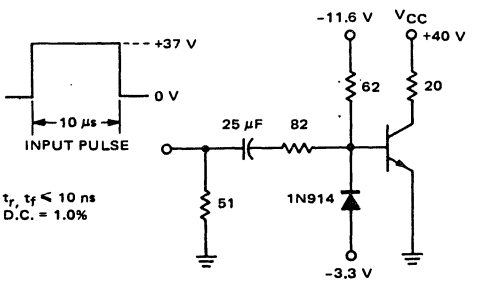


FIGURE 3 – TURN-ON TIME

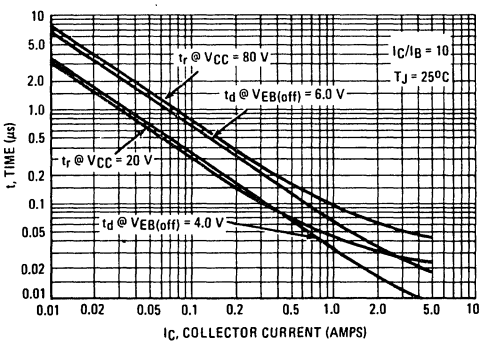
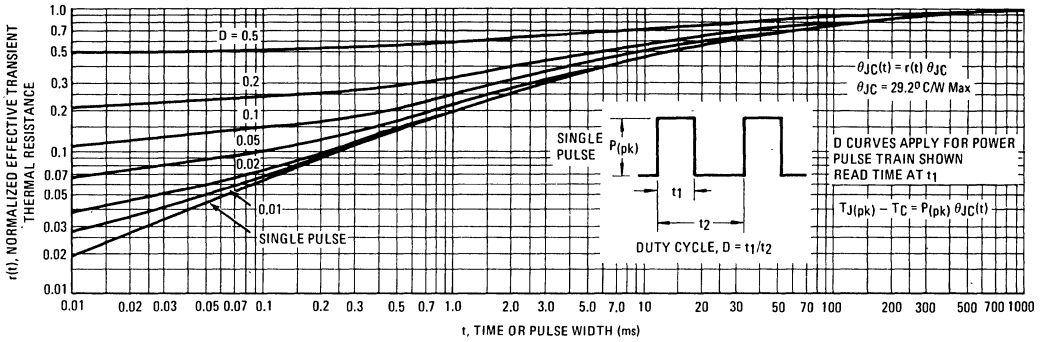
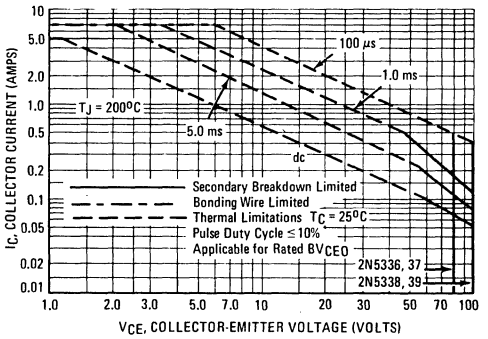


FIGURE 4 – THERMAL RESPONSE



4

FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 – TURN-OFF TIME

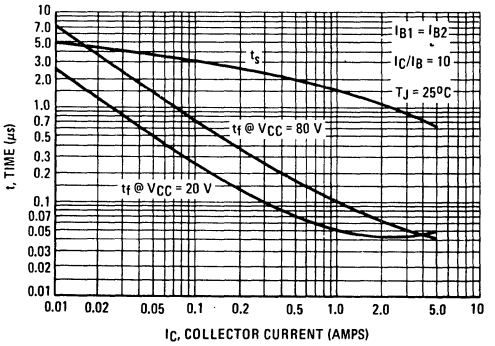


FIGURE 7 – CAPACITANCE versus VOLTAGE

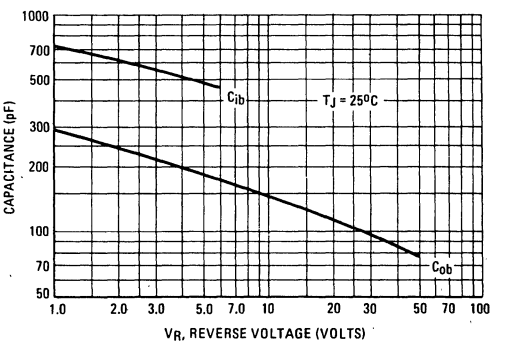


FIGURE 8 – DC CURRENT GAIN

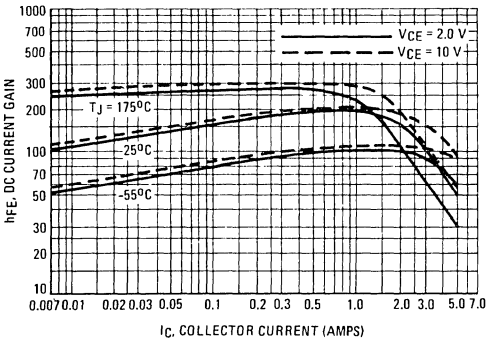
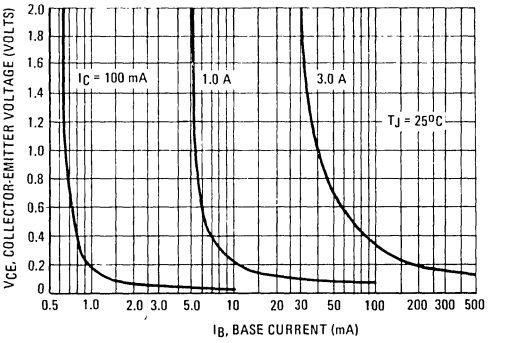


FIGURE 9 – COLLECTOR SATURATION REGION



4

FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

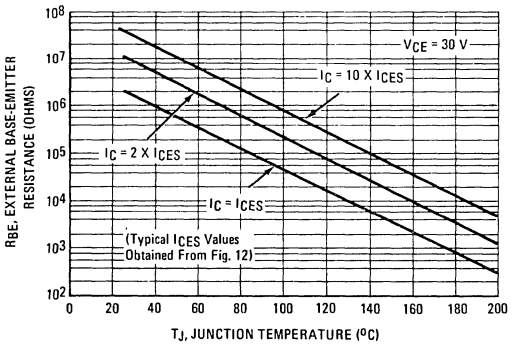


FIGURE 11 – ON VOLTAGES

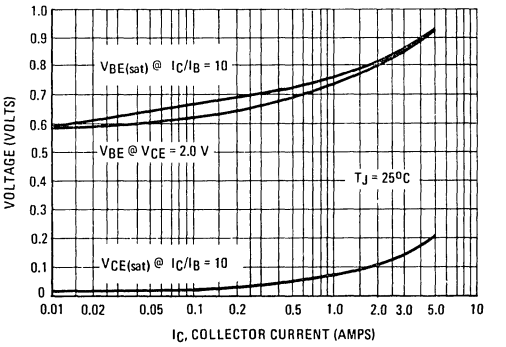


FIGURE 12 – COLLECTOR CUT-OFF REGION

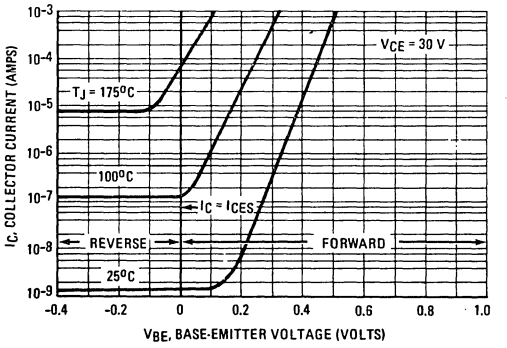
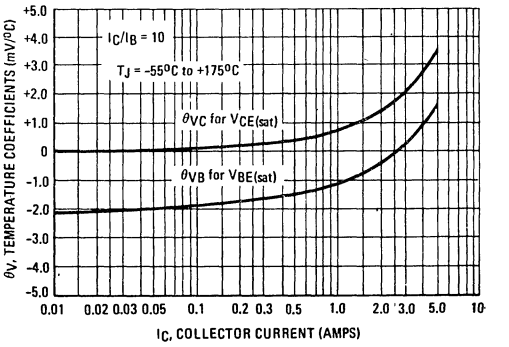


FIGURE 13 – TEMPERATURE COEFFICIENTS



2N5344 (SILICON)
2N5345

4

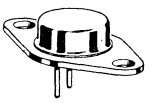
HIGH VOLTAGE POWER PNP SILICON TRANSISTORS

. . . designed for high-voltage switching and amplifier applications.

- High Voltage Ratings — V_{CEO} = 250 and 300 Vdc
- Fast Switching Times — Typically Less Than 550 ns Total @ V_{CC} = 100 Vdc
- High Current-Gain-Bandwidth Product — f_T = 60 MHz (Min) @ I_C = 100 mAdc
- Packaged in the Compact, High-Efficiency TO-66 Case

1 AMPERE
HIGH-VOLTAGE
PNP
POWER TRANSISTORS

250-300 VOLTS
40 WATTS



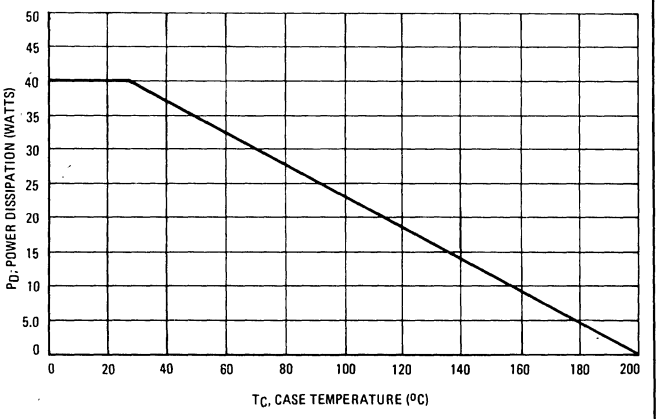
MAXIMUM RATINGS

Rating	Symbol	2N5344	2N5345	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	Vdc
Collector-Base Voltage	V_{CB}	250	300	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	1.0		Adc
Base Current — Continuous	I_B	0.5		Adc
Total Device Dissipation @ T_C = 25°C	P_D	40		Watts
Derate above 25°C		228		mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

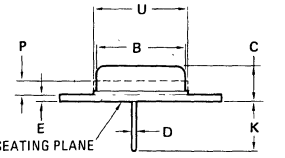
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.38	°C/W

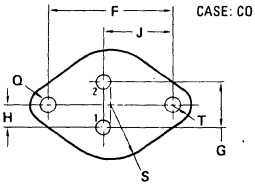
FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



Safe Area Curves Are Indicated By Figure 5.
All Limits Are Applicable And Must Be Observed



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0) 2N5344	5	$V_{CEO(sus)}$	250	-	Vdc
2N5345			300	-	
Collector Cutoff Current (V_{CE} = 225 Vdc, $V_{BE(off)}$ = 1.5 Vdc) 2N5344	10, 12	I_{CEX}	-	100	μAdc
(V_{CE} = 270 Vdc, $V_{BE(off)}$ = 1.5 Vdc) 2N5345			-	100	
(V_{CE} = 225 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C) 2N5344			-	1.0	mAdc
(V_{CE} = 270 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C) 2N5345			-	1.0	
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	-	I_{CBO}	-	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	-	I_{EBO}	-	0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	8	h_{FE}	25	100	-
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)			7.0	-	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)	9, 11, 13	$V_{CE(sat)}$	-	3.0	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)	11, 13	$V_{BE(sat)}$	-	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 100 mAdc, V_{CE} = 20 Vdc, f = 10 MHz)	-	f_T	60	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0)	7	C_{ob}	-	200	pF
SWITCHING CHARACTERISTICS					
Delay Time (V_{CC} = 100 Vdc, $V_{BE(off)}$ = 0.85 Vdc, I_C = 500 mAdc, I_{B1} = 50 mAdc)	2, 3	t_d	-	100	ns
Rise Time	2, 3	t_r	-	100	ns
Storage Time (V_{CC} = 100 Vdc, I_C = 500 mAdc, I_{B1} = I_{B2} = 50 mAdc)	2, 6	t_s	-	600	ns
Fall Time	2, 6	t_f	-	100	ns

(1) Pulse Test: Pulse Width ≈ 300 μs, Duty Cycle ≈ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

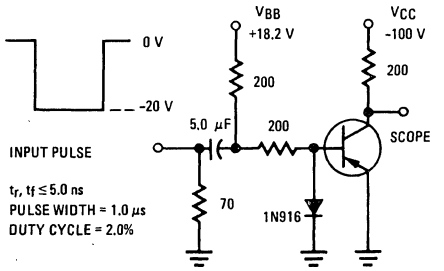


FIGURE 3 – TURN-ON TIME

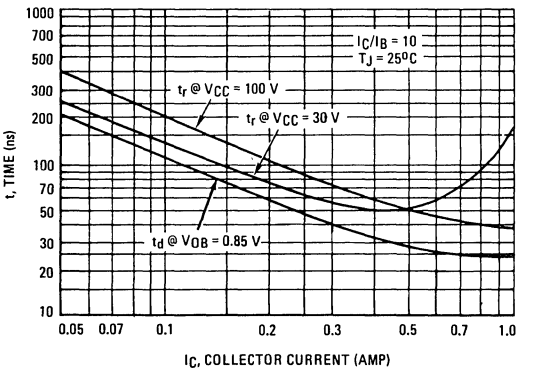


FIGURE 4 – THERMAL RESPONSE

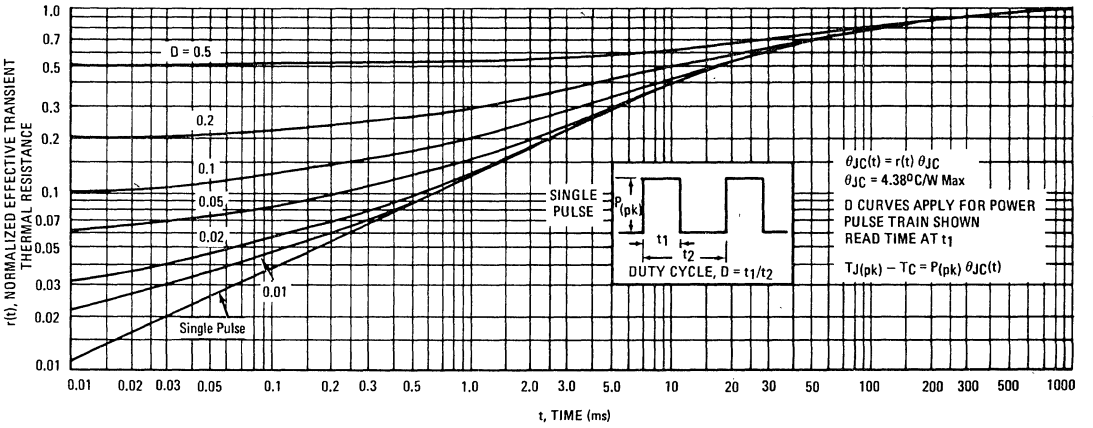


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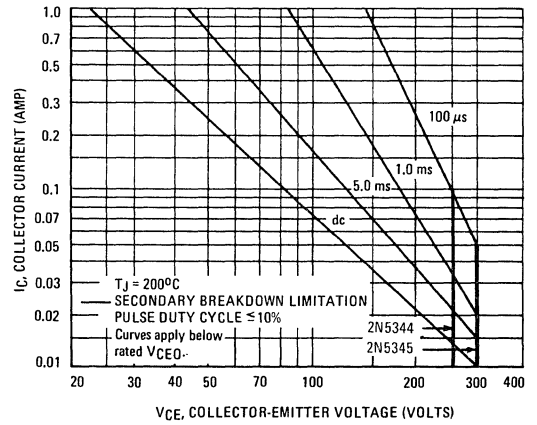
FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 – TURN-OFF TIME

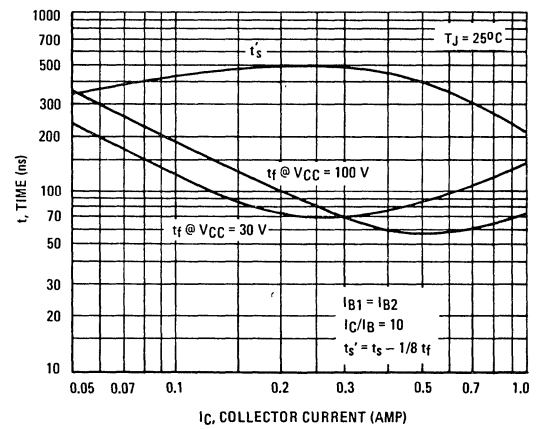
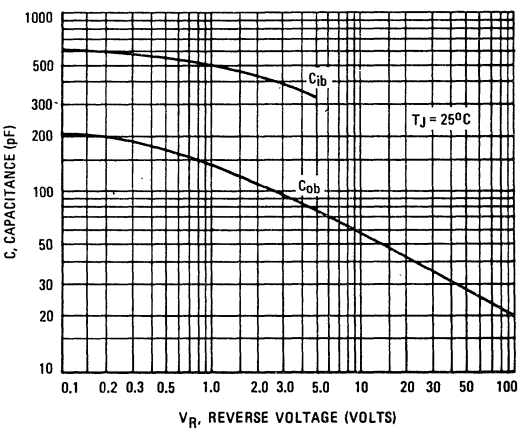


FIGURE 7 – CAPACITANCES



TYPICAL DC CHARACTERISTICS

FIGURE 8 – DC CURRENT GAIN

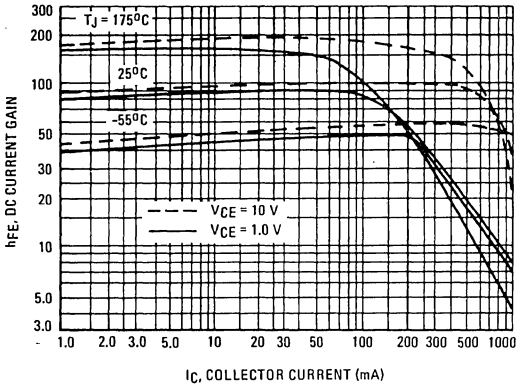


FIGURE 9 – COLLECTOR SATURATION REGION

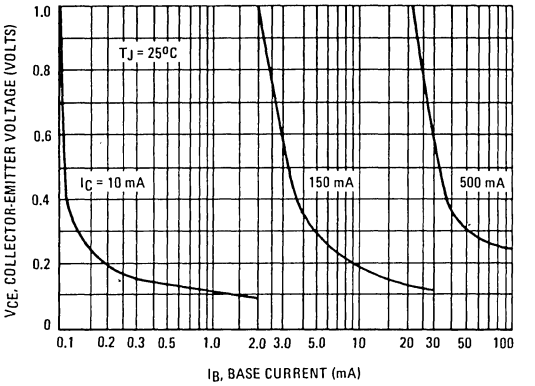


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FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

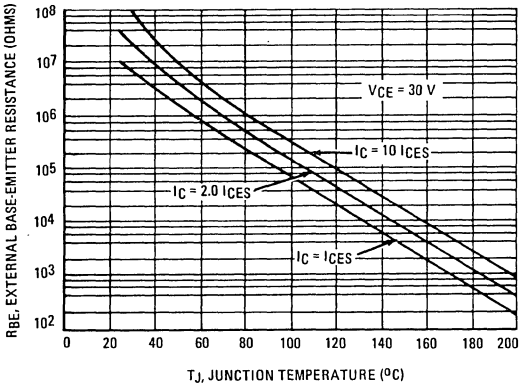


FIGURE 11 – "ON" VOLTAGES

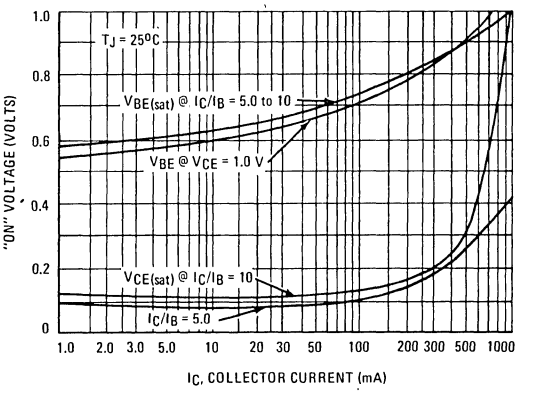


FIGURE 12 – COLLECTOR CUT-OFF REGION

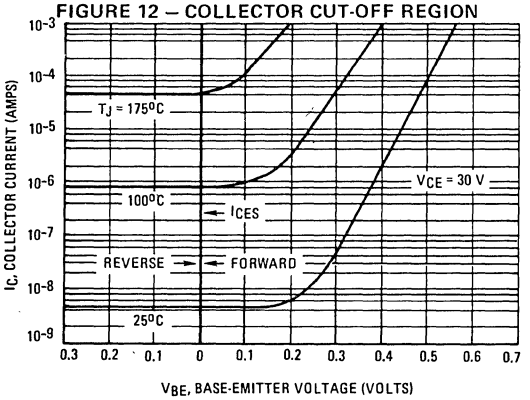
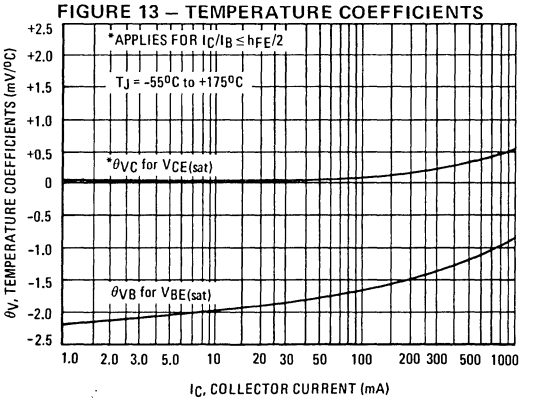


FIGURE 13 – TEMPERATURE COEFFICIENTS



2N5346 thru 2N5349

MEDIUM-POWER NPN SILICON TRANSISTORS

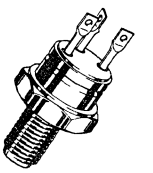
. . . designed for switching and wide-band amplifier applications.

- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 7.0 Adc
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact, High Dissipation TO-59 Case
- Isolated Collector Configuration
- Complementary to 2N6186 thru 2N6189

7 AMPERE

POWER TRANSISTORS NPN SILICON

80–100 VOLTS
60 WATTS



4

***MAXIMUM RATINGS**

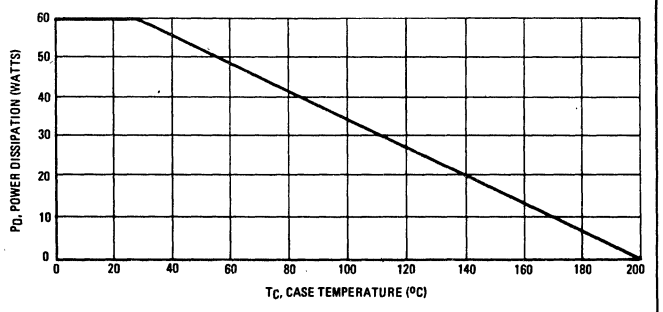
Rating	Symbol	2N5346 2N5347	2N5348 2N5349	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current – Continuous	I_C	7.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	60 343		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

THERMAL CHARACTERISTICS

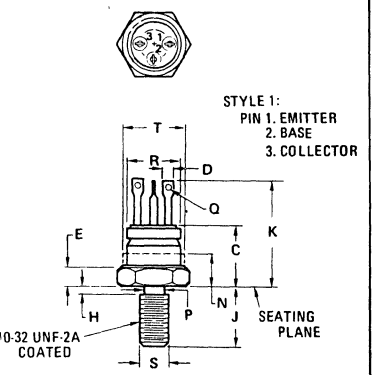
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.91	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	10.77	11.10	0.424	0.437
C	8.13	11.89	0.320	0.468
E	2.29	3.81	0.090	0.150
G	4.70	5.46	0.185	0.215
H	–	1.98	–	0.078
J	10.16	11.56	0.400	0.455
K	14.48	19.38	0.570	0.763
L	2.29	2.79	0.090	0.110
N	–	6.35	–	0.250
P	4.14	4.80	0.163	0.189
Q	1.02	1.65	0.040	0.065
R	8.08	9.65	0.318	0.380
S	4.212	4.310	0.1658	0.1697
T	9.65	11.10	0.380	0.437

All JEDEC dimensions and notes apply
Collector isolated from case.

CASE 160-03
TO-59

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C, unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1)		–	$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N5346, 2N5347			80	–	
	2N5348, 2N5349			100	–	
Collector Cutoff Current		–	I_{CEO}			μAdc
(V_{CE} = 75 Vdc, I_B = 0)	2N5346, 2N5347			–	100	
(V_{CE} = 90 Vdc, I_B = 0)	2N5348, 2N5349			–	100	
Collector Cutoff Current		12	I_{CEX}			μAdc
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5346, 2N5347			–	10	
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5348, 2N5349			–	10	
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5346, 2N5347			–	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5348, 2N5349			–	1.0	
Collector Cutoff Current		–	I_{CBO}			μAdc
(V_{CB} = Rated V_{CB}, I_E = 0)				–	10	
Emitter Cutoff Current		–	I_{EBO}			μAdc
(V_{EB} = 6.0 Vdc, I_C = 0)				–	100	
ON CHARACTERISTICS (1)						
DC Current Gain		8	h_{FE}			–
(I_C = 500 mAdc, V_{CE} = 2.0 Vdc)	2N5346, 2N5348			30	–	
	2N5347, 2N5349			60	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	2N5346, 2N5348			30	120	
	2N5347, 2N5349			60	240	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N5346, 2N5348			20	–	
	2N5347, 2N5349			40	–	
Collector-Emitter Saturation Voltage		9, 11, 13	$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	0.7	
(I_C = 7.0 Adc, I_B = 0.7 Adc)				–	1.2	
Base-Emitter Saturation Voltage		11, 13	$V_{BE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	1.2	
(I_C = 7.0 Adc, I_B = 0.7 Adc)				–	2.0	
DYNAMIC CHARACTERISTICS						
Current-Gain–Bandwidth Product		–	f_T			MHz
(I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)				30	–	
Output Capacitance		7	C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)				–	250	
Input Capacitance		7	C_{ib}			pF
(V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)				–	1,000	
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 40 Vdc, $V_{EB(off)}$ = 3.0 Vdc,	2, 3	t_d	–	100	ns
Rise Time	(I_C = 2.0 Adc, I_{B1} = 200 mAdc)		t_r	–	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc,	2, 6	t_s	–	2.0	μs
Fall Time	I_{B1} = I_{B2} = 200 mAdc)		t_f	–	200	ns

*Indicates JEDEC Registered Data. (1) Pulse Test: Pulse Width ≈ 300 μs, Duty Cycle ≈ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

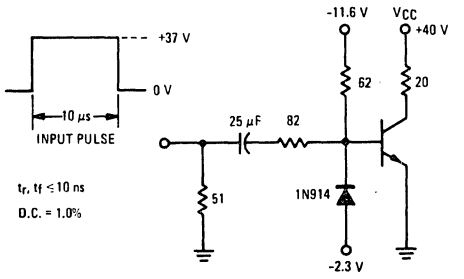


FIGURE 3 – TURN-ON TIME

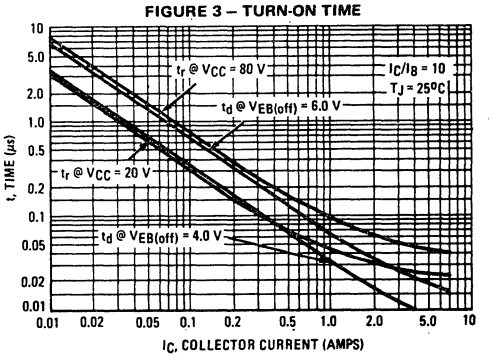


FIGURE 4 – THERMAL RESPONSE

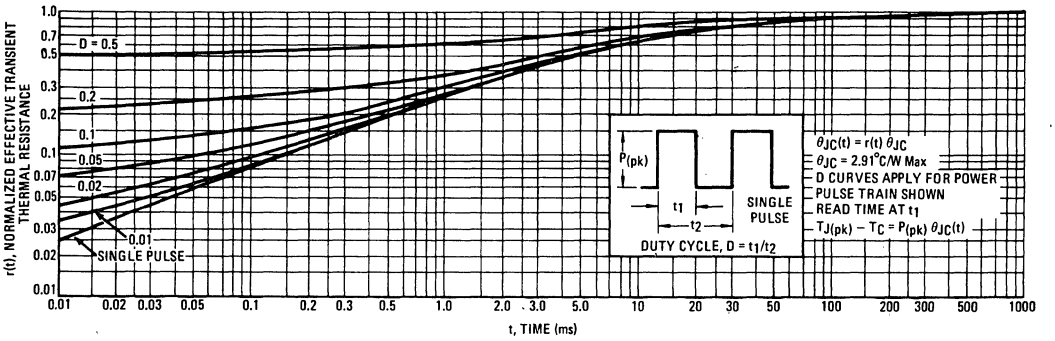


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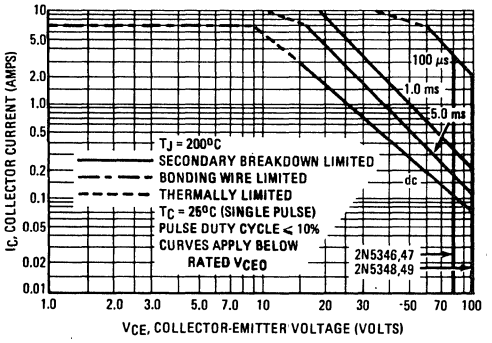
FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 – TURN-OFF TIME

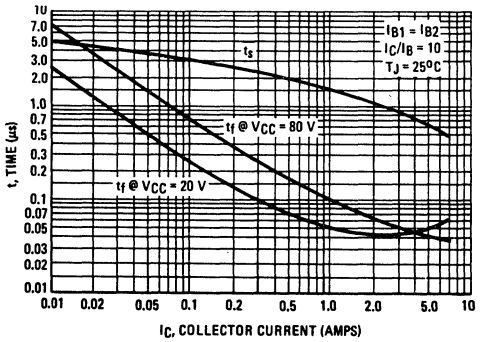


FIGURE 7 – CAPACITANCE versus VOLTAGE

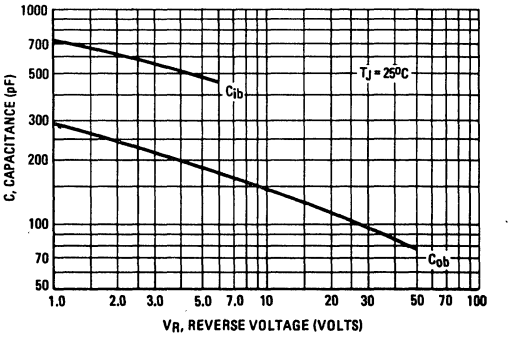


FIGURE 8 – DC CURRENT GAIN

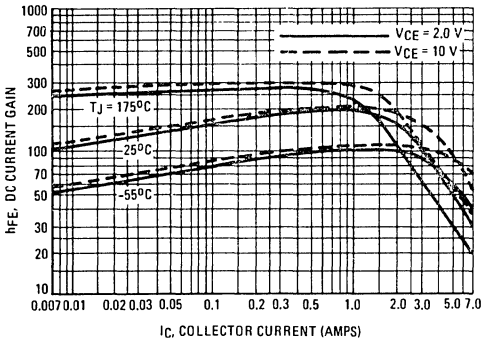


FIGURE 9 – COLLECTOR SATURATION REGION

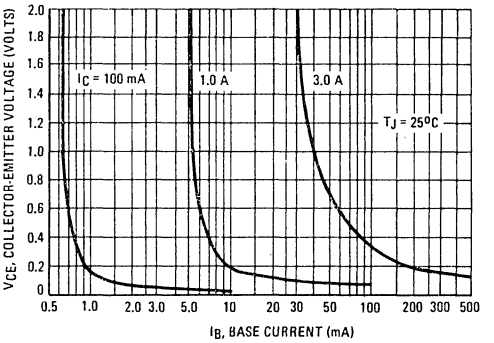


FIGURE 10 – EFFECTS OF BASE EMITTER RESISTANCE

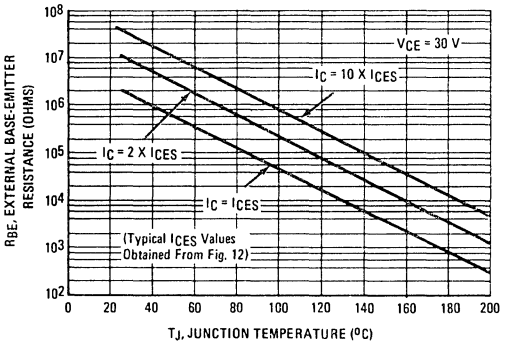


FIGURE 11 – "ON" VOLTAGES

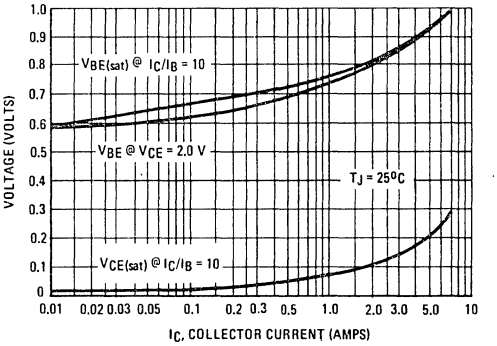


FIGURE 12 – COLLECTOR CUT-OFF REGION

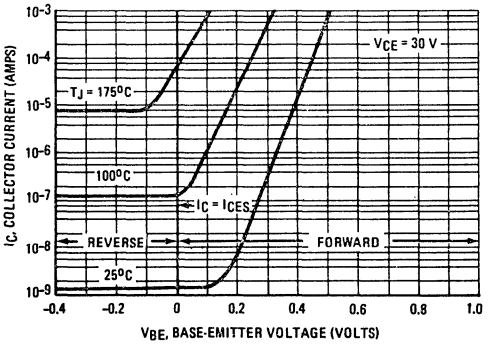
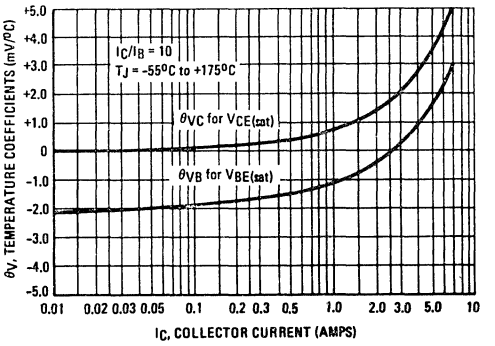


FIGURE 13 – TEMPERATURE COEFFICIENTS



2N5427 thru 2N5430

MEDIUM-POWER NPN SILICON TRANSISTORS

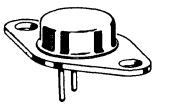
. . . designed for switching and wide-band amplifier applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 7.0 Adc
- DC Current Gain Specified to 7 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact TO-66 Case

7 AMPERE

POWER TRANSISTORS NPN SILICON

80–100 VOLTS
40 WATTS



4

***MAXIMUM RATINGS**

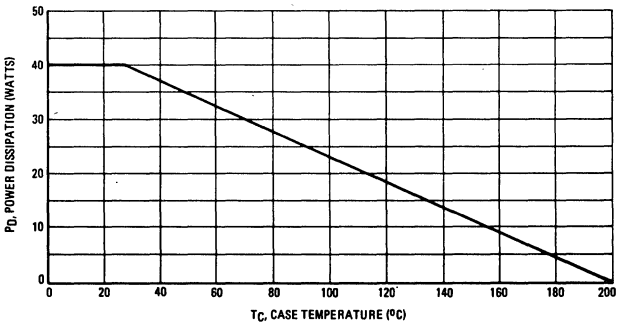
Rating	Symbol	2N5427 2N5428	2N5429 2N5430	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	7.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 228		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

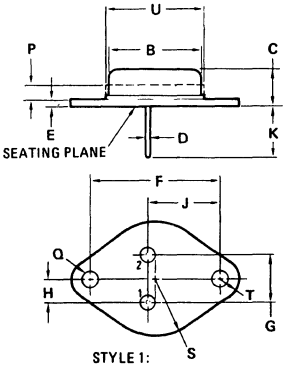
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.37	°C/W

* Indicates JEDEC Registered Data

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C, unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1)		–	$BV_{CEO(sus)}$*			Vdc
(I_C = 50 mAdc, I_B = 0)	2N5427, 2N5428			80	–	
	2N5429, 2N5430			100	–	
Collector Cutoff Current		–	I_{CEO}			μAdc
(V_{CE} = 75 Vdc, I_B = 0)	2N5427, 2N5428			–	100	
(V_{CE} = 90 Vdc, I_B = 0)	2N5429, 2N5430			–	100	
Collector Cutoff Current		12	I_{CEX}			μAdc
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5427, 2N5428			–	10	
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5429, 2N5430			–	10	
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5427, 2N5428			–	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5429, 2N5430			–	1.0	
Collector Cutoff Current		–	I_{CBO}			μAdc
(V_{CB} = Rated V_{CB}, I_E = 0)				–	10	
Emitter Cutoff Current		–	I_{EBO}			μAdc
(V_{BE} = 6.0 Vdc, I_C = 0)				–	100	
ON CHARACTERISTICS (1)						
DC Current Gain		8	h_{FE}*			–
(I_C = 500 mAdc, V_{CE} = 2.0 Vdc)	2N5427, 2N5429			30	–	
	2N5428, 2N5430			60	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	2N5427, 2N5429			30	120	
	2N5428, 2N5430			60	240	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N5427, 2N5429			20	–	
	2N5428, 2N5430			40	–	
Collector-Emitter Saturation Voltage		9, 11, 13	$V_{CE(sat)}$*			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	0.7	
(I_C = 7.0 Adc, I_B = 0.7 Adc)				–	1.2	
Base-Emitter Saturation Voltage		11, 13	$V_{BE(sat)}$*			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	1.2	
(I_C = 7.0 Adc, I_B = 0.7 Adc)				–	2.0	
DYNAMIC CHARACTERISTICS						
Current-Gain—Bandwidth Product		–	f_T			MHz
(I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)				30	–	
Output Capacitance		7	C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)				–	250	
Input Capacitance		7	C_{ib}			pF
(V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)				–	1,000	
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 40 Vdc, $V_{EB(off)}$ = 3.0 Vdc,	2, 3	t_d	–	100	ns
Rise Time	(I_C = 2.0 Adc, I_{B1} = 200 mAdc)		t_r	–	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc,	2, 6	t_s	–	2.0	μs
Fall Time	I_{B1} = I_{B2} = 200 mAdc)		t_f	–	200	ns

*Indicates JEDEC Registered Data. (1)Pulse Test: Pulse Width ≈ 300 μs, Duty Cycle ≈ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

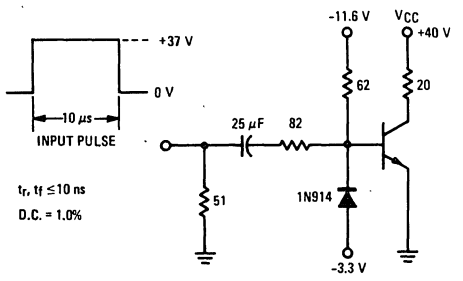


FIGURE 3 – TURN-ON TIME

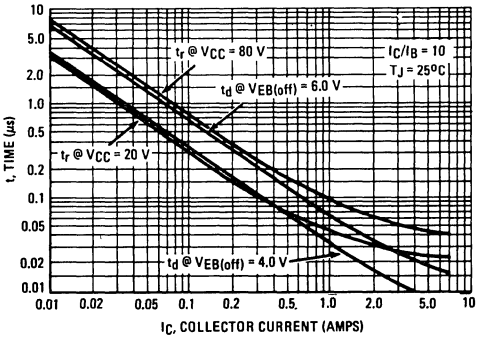


FIGURE 4 – THERMAL RESPONSE

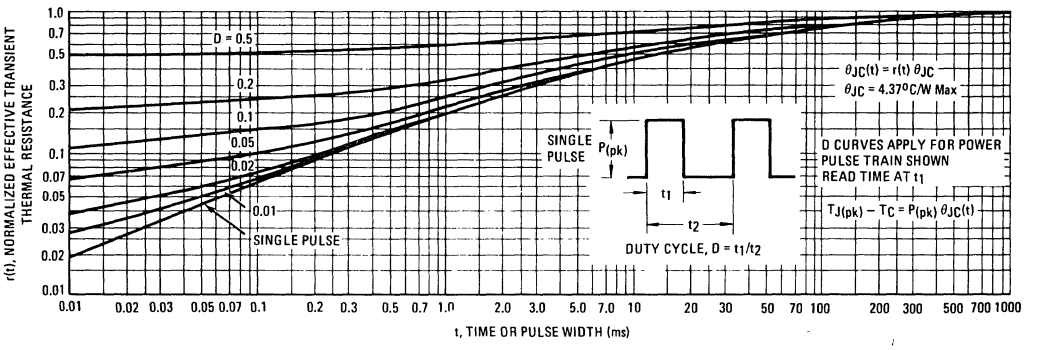
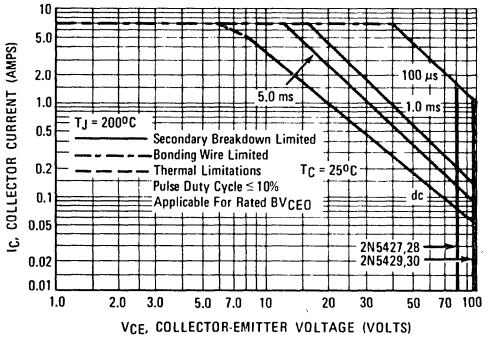


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 6 – TURN-OFF TIME

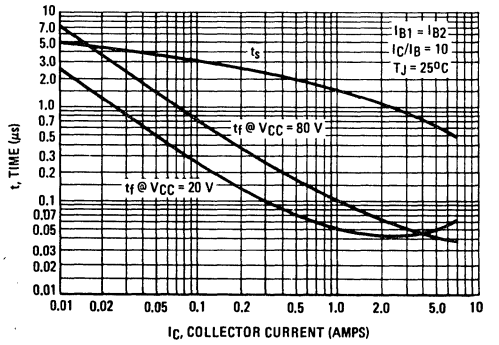


FIGURE 7 – CAPACITANCE versus VOLTAGE

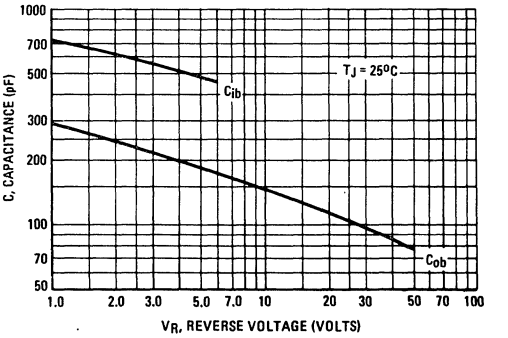


FIGURE 8 – DC CURRENT GAIN

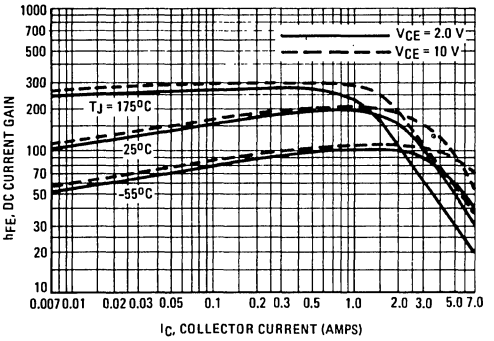


FIGURE 9 – COLLECTOR SATURATION REGION

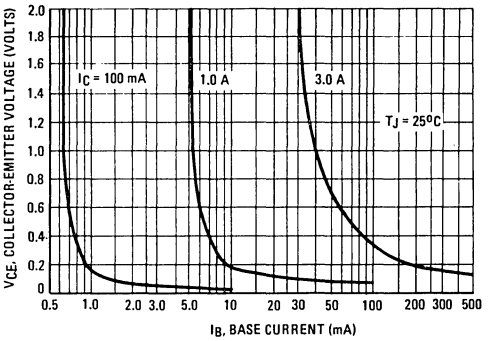


FIGURE 10 – EFFECTS OF BASE-EMITTER RESISTANCE

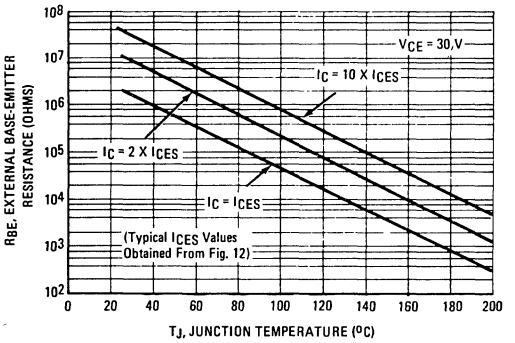


FIGURE 11 – "ON" VOLTAGES

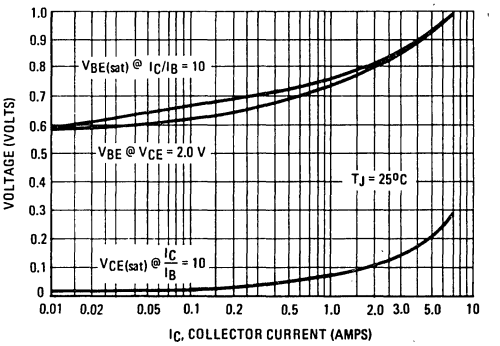


FIGURE 12 – COLLECTOR CUT-OFF REGION

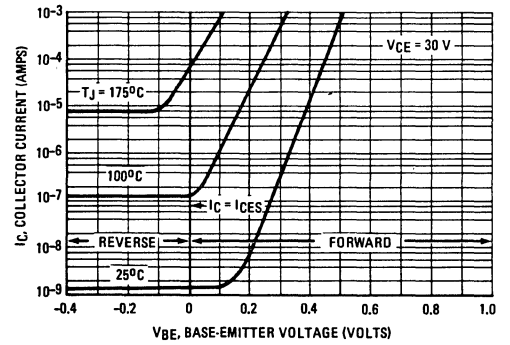
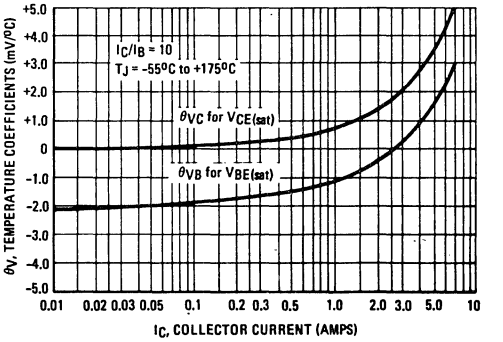


FIGURE 13 – TEMPERATURE COEFFICIENTS



4

2N5629, 2N5630, 2N5631 NPN
2N6029, 2N6030, 2N6031 PNP

4

HIGH-VOLTAGE – HIGH POWER TRANSISTORS

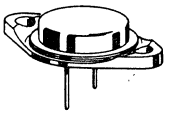
. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc – 2N5629, 2N6029
  = 120 Vdc – 2N5630, 2N6030
  = 140 Vdc – 2N5631, 2N6031
- High DC Current Gain – @ I_C = 8.0 Adc
  h_{FE} = 25 (Min) – 2N5629, 2N6029
  = 20 (Min) – 2N5630, 2N6030
  = 15 (Min) – 2N5631, 2N6031
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc

16 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

100-120-140 VOLTS
200 WATTS



*MAXIMUM RATINGS

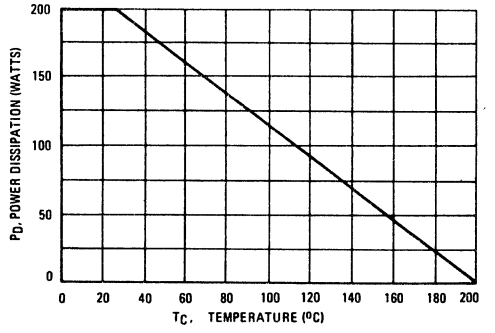
Rating	Symbol	2N5629 2N6029	2N5630 2N6030	2N5631 2N6031	Unit
Collector-Emitter Voltage	V_{CEO}	100	120	140	Vdc
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Emitter-Base Voltage	V_{EB}	← 7.0 →			Vdc
Collector Current – Continuous Peak	I_C	← 16 → ← 20 →			Adc
Base Current – Continuous	I_B	← 5.0 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 200 → ← 1.14 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			°C

*THERMAL CHARACTERISTICS

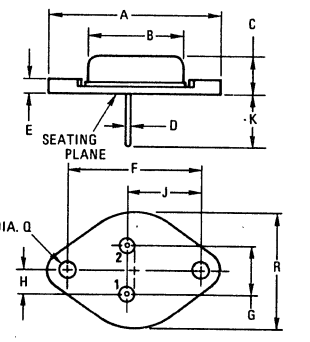
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING



Safe Area Curves are indicated by Figure 5. All Limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

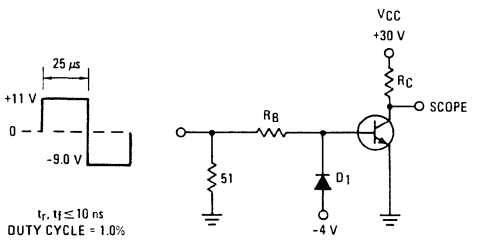
Collector connected to case.
CASE 11-01
(TO-3)

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N5629, 2N6029 2N5630, 2N6030 2N5631, 2N6031	$V_{CEO(sus)}$	 100 120 140	 — — —	Vdc
Collector-Emitter Cutoff Current (V_{CE} = 50 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 70 Vdc, I_B = 0)	 2N5629, 2N6029 2N5630, 2N6030 2N5631, 2N6031	I_{CEO}	 — — —	 1.0 1.0 1.0	mAdc
Collector-Emitter Cutoff Current (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	 — —	 1.0 5.0	mAdc
Collector-Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	—	1.0	mAdc
Emitter-Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 16 Adc, V_{CE} = 2.0 Vdc)	2N5629, 2N6029 2N5630, 2N6030 2N5631, 2N6031 All Types	h_{FE}	 25 20 15 4.0	 100 80 60 —	—
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 16 Adc, I_B = 4.0 Adc)	All Types	$V_{CE(sat)}$	 — —	 1.0 2.0	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	—	1.8	Vdc
Base-Emitter On Voltage (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N5629, 30, 31 2N6029, 30, 31	C_{ob}	—	 500 1000	pF
Small-Signal Current Gain (I_C = 4.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	15	—	—

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≥ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE I_B ~100 mA
MSD6100 USED BELOW I_B ~100 mA

For PNP test circuit, reverse all polarities and D1.

FIGURE 3 – TURN-ON TIME

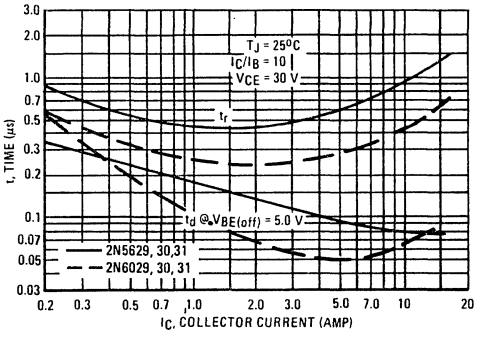


FIGURE 4 – THERMAL RESPONSE

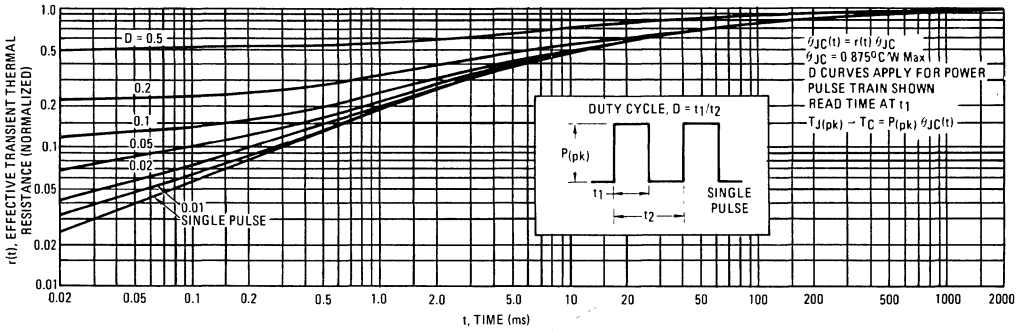
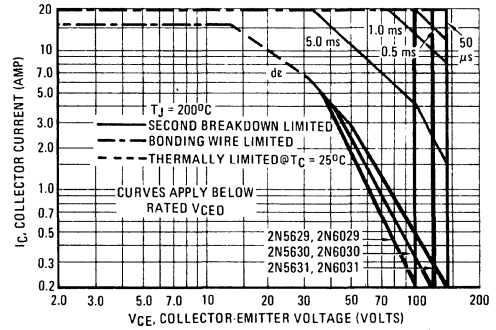


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



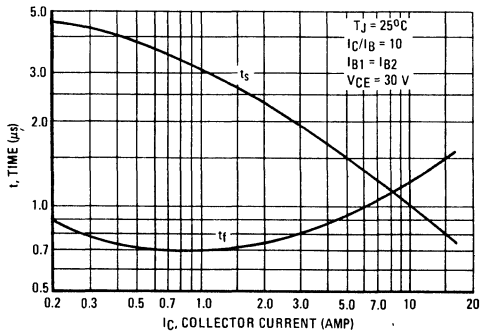
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

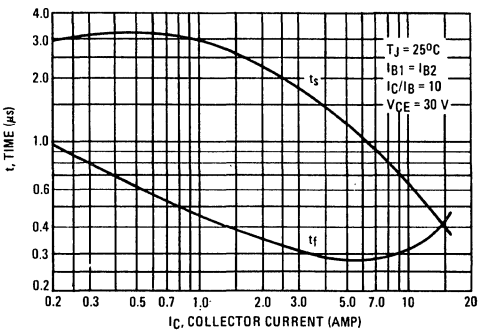
The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN
2N5629, 2N5630, 2N5631

PNP
2N6029, 2N6030, 2N6031

FIGURE 6 – TURN-OFF TIME

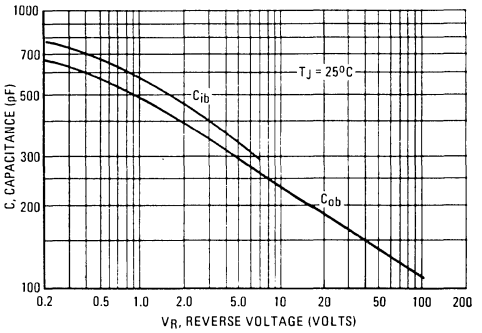


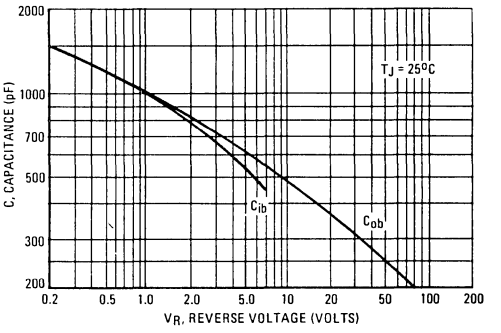


NPN
2N5629, 2N5630, 2N5631

PNP
2N6029, 2N6030, 2N6031

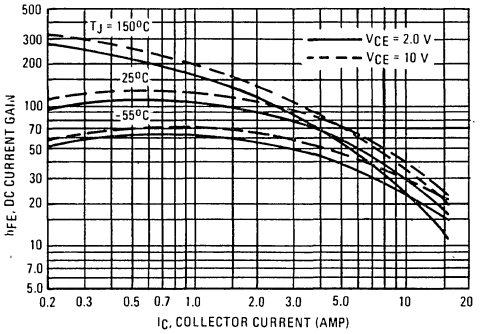
FIGURE 7 – CAPACITANCE





4

FIGURE 8 – DC CURRENT GAIN



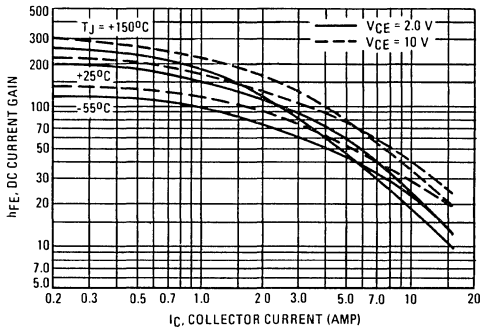
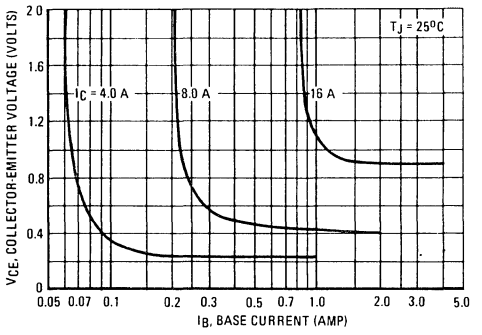
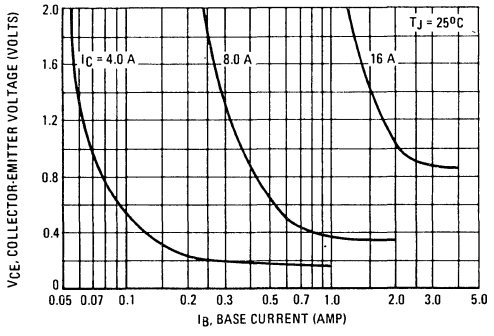


FIGURE 9 – COLLECTOR SATURATION REGION



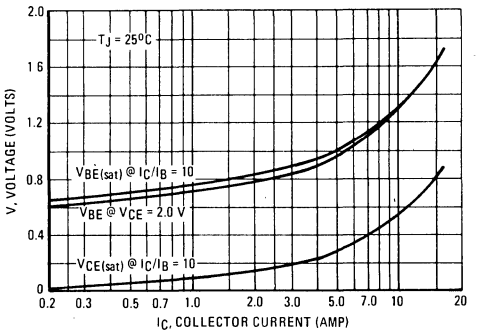


4

NPN
2N5629, 2N5630, 2N5631

PNP
2N6029, 2N6030, 2N6031

FIGURE 10 – ON VOLTAGES



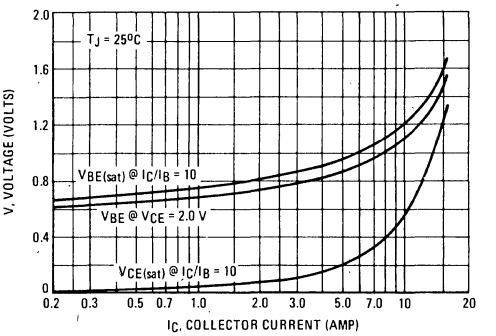
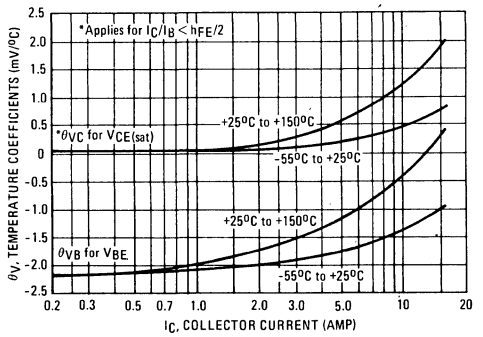


FIGURE 11 – TEMPERATURE COEFFICIENTS



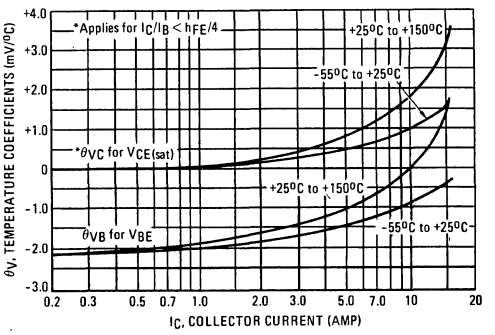
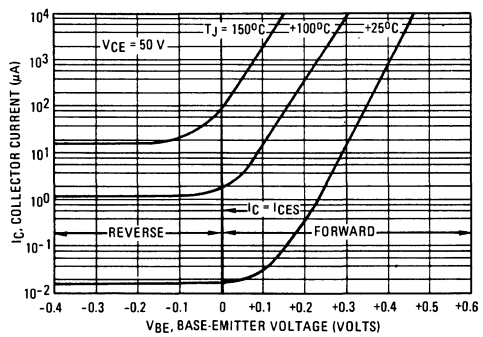
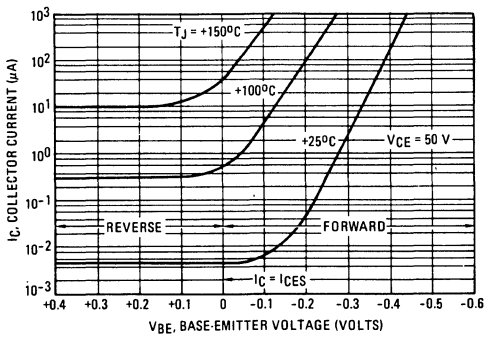


FIGURE 12 – COLLECTOR CUTOFF REGION

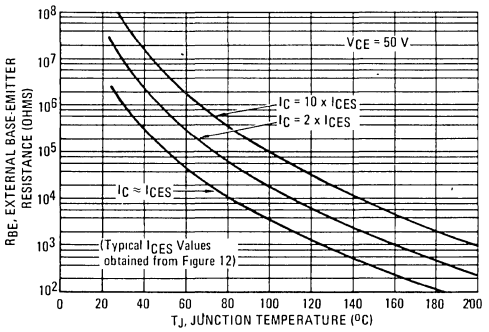


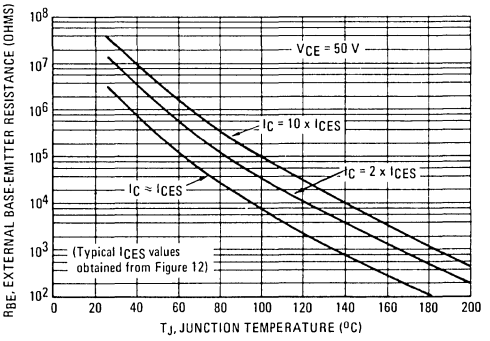


NPN
2N5629, 2N5630, 2N5631

PNP
2N6029, 2N6030, 2N6031

FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE





4

2N5632, 2N5633, 2N5634 NPN
2N6229, 2N6230, 2N6231 PNP

4

HIGH VOLTAGE-HIGH-POWER SILICON TRANSISTORS

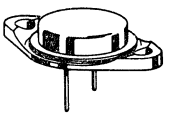
. . . designed for use in high power audio amplifier applications and high-voltage switching regulator circuits.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc (Min) – 2N5632, 2N6229
  = 120 Vdc (Min) – 2N5633, 2N6230
  = 140 Vdc (Min) – 2N5634, 2N6231
- High DC Current Gain @ I_C = 5.0 Adc –
  h_{FE} = 25 (Min) – 2N5632, 2N6229
  = 20 (Min) – 2N5633, 2N6230
  = 15 (Min) – 2N5634, 2N6231
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 7.5 Adc

10 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

100-120-140 VOLTS
150 WATTS



*MAXIMUM RATINGS

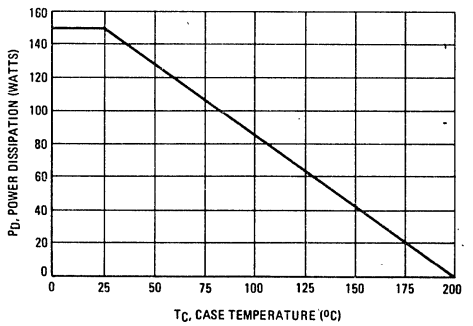
Rating	Symbol	2N5632 2N6229	2N5633 2N6230	2N5634 2N6231	Unit
Collector-Emitter Voltage	V_{CEO}	100	120	140	Vdc
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Emitter-Base Voltage	V_{EB}	← 7.0 →			Vdc
Collector Current – Continuous – Peak	I_C	← 10 → ← 15 →			Adc
Base Current – Continuous	I_B	← 5.0 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 150 0.857 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

*Indicates JEDEC Registered Data.

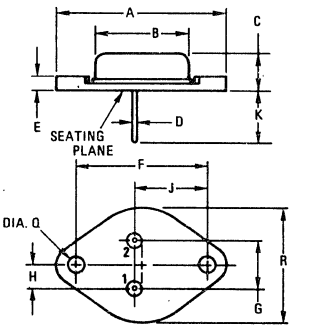
FIGURE 1 – POWER DERATING



Safe area limits are indicated by Figure 5.
Both limits are applicable and must be observed.

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

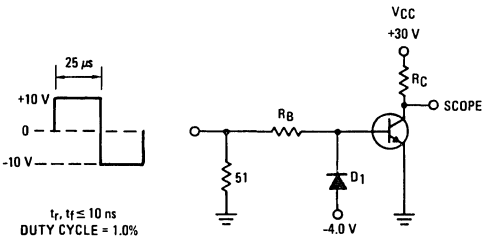
Collector connected to case.
CASE 11-01
TO-3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage(1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N5632, 2N6229		100	–	
	2N5633, 2N6230		120	–	
	2N5634, 2N6231		140	–	
Collector-Emitter Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 50 Vdc, I_B = 0)	2N5632, 2N6229		–	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N5633, 2N6230		–	1.0	
(V_{CE} = 70 Vdc, I_B = 0)	2N5634, 2N6231		–	1.0	
Collector-Emitter Cutoff Current		I_{CEX}			mAdc
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc)			–	1.0	
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)			–	5.0	
Collector Base Cutoff Current		I_{CBO}	–	1.0	mAdc
(V_{CB} = Rated V_{CB}, I_E = 0)					
Emitter-Base Cutoff Current		I_{EBO}	–	1.0	mAdc
(V_{BE} = 7.0 Vdc, I_C = 0)					
ON CHARACTERISTICS					
DC Current Gain(1)		h_{FE}			–
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N5632, 2N6229		25	100	
	2N5633, 2N6230		20	80	
	2N5634, 2N6231		15	60	
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)	All Types		5.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 7.5 Adc, I_B = 0.75 Adc)			–	1.0	
(I_C = 10 Adc, I_B = 2.0 Adc)			–	2.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$	–	2.0	Vdc
(I_C = 7.5 Adc, I_B = 0.75 Adc)					
Base-Emitter On Voltage		$V_{BE(on)}$	–	1.5	Vdc
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (2)		f_T	1.0	–	MHz
(I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)					
Output Capacitance	2N5632, 2N5633, 2N5634	C_{ob}	–	300	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6229, 2N6230, 2N6231		–	600	
Small Signal Current Gain		h_{fe}	15	–	–
(V_{CE} = 10 Vdc, I_C = 2.0 Adc, f = 1.0 kHz)					

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE I_B ≈100 mA
MSD6100 USED BELOW I_B ≈100 mA

For PNP test, reverse all polarities and D1.

4

NPN
2N5632, 2N5633, 2N5634

PNP
2N6229, 2N6230, 2N6231

FIGURE 3 – TURN-ON TIME

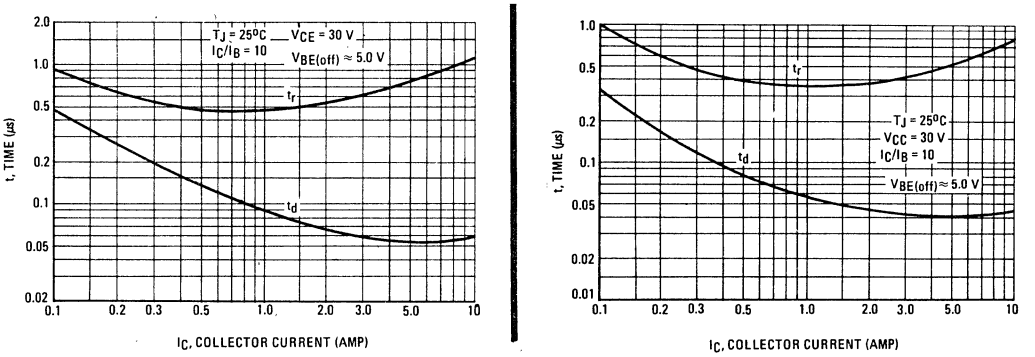


FIGURE 4 – THERMAL RESPONSE

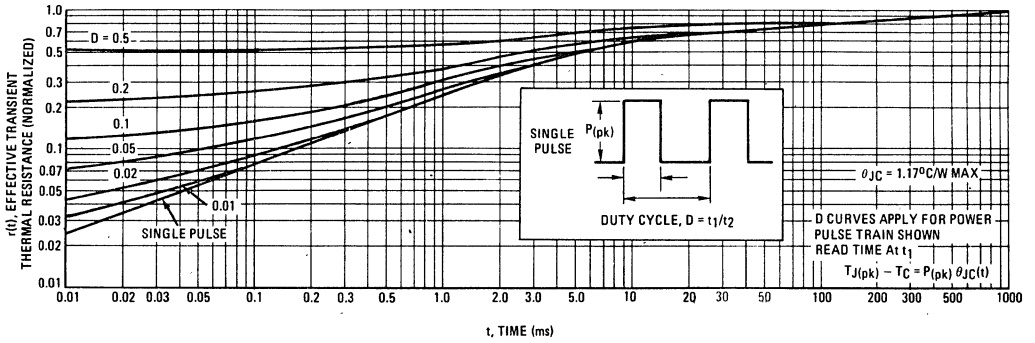
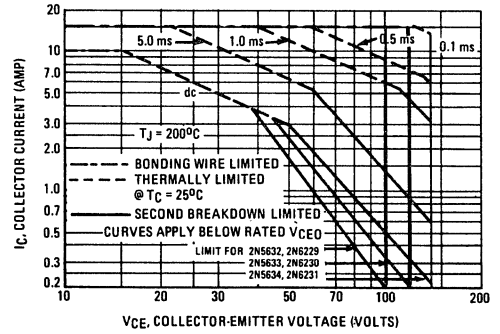


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN
2N5632, 2N5633, 2N5634

PNP
2N6229, 2N6230, 2N6231

FIGURE 6 – TURN-OFF TIME

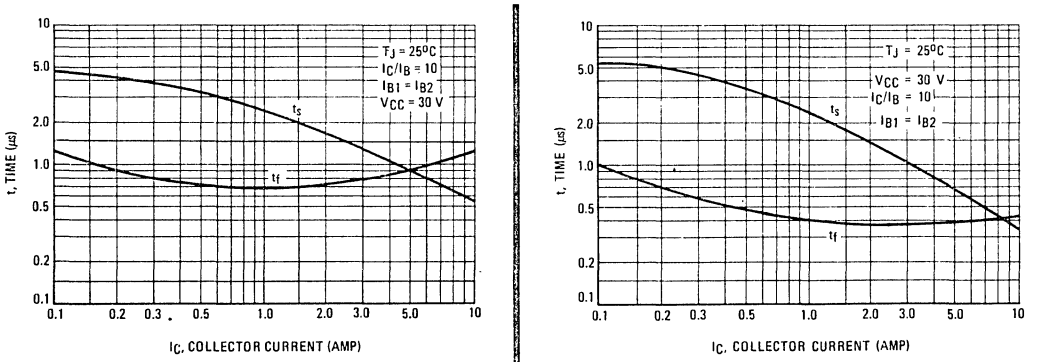


FIGURE 7 – CAPACITANCE

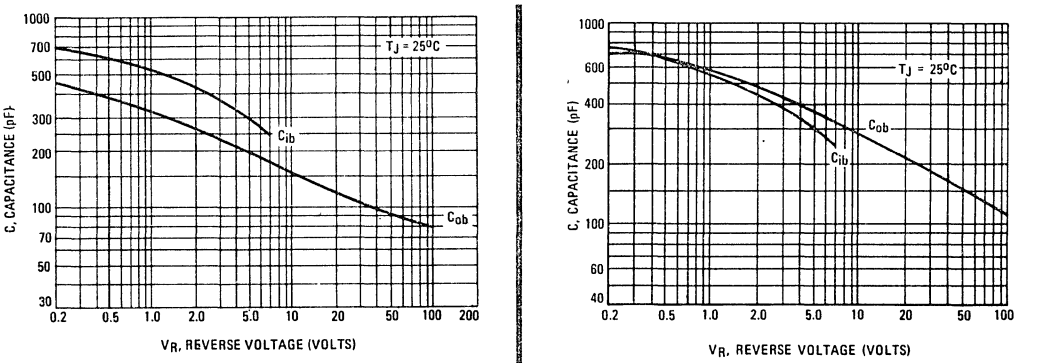
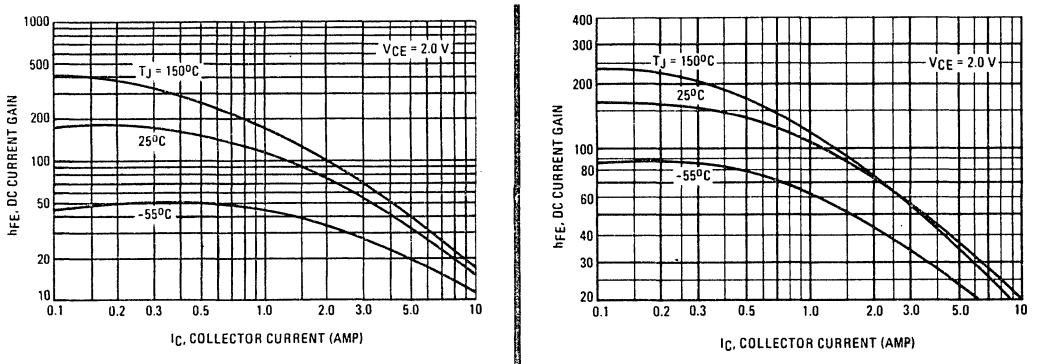


FIGURE 8 – DC CURRENT GAIN

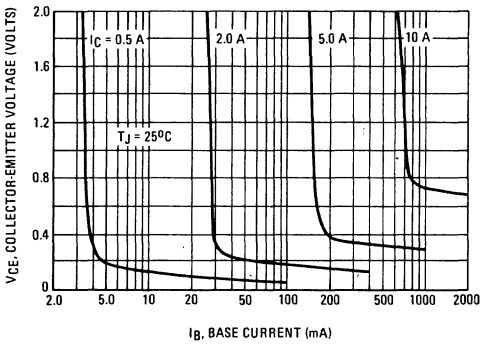


4

NPN
2N5632, 2N5633, 2N5634

PNP
2N6229, 2N6230, 2N6231

FIGURE 9 – COLLECTOR SATURATION REGION



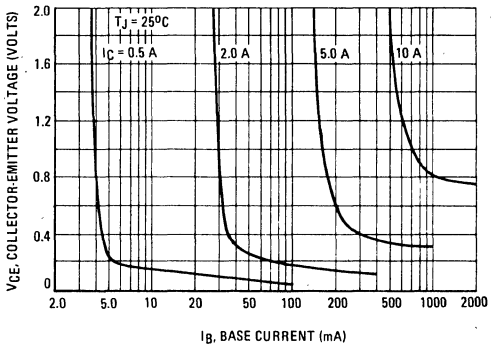
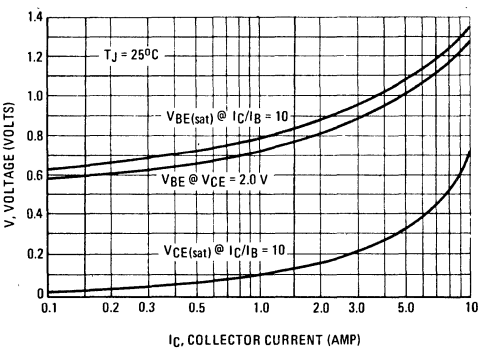


FIGURE 10 – "ON" VOLTAGES



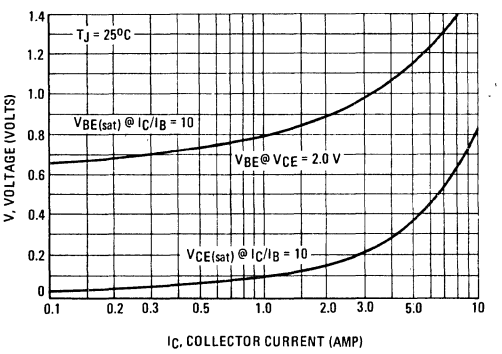
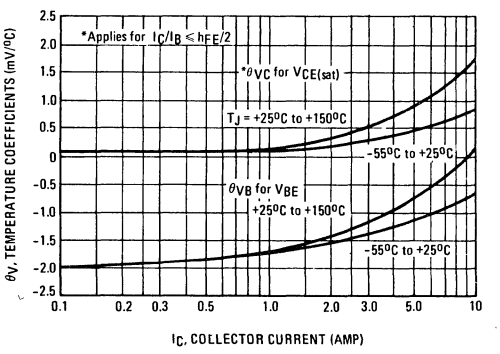
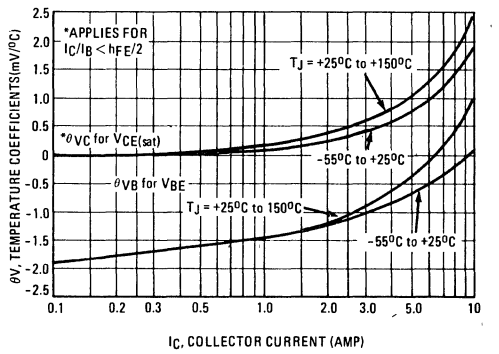


FIGURE 11 – TEMPERATURE COEFFICIENTS





NPN
2N5632, 2N5633, 2N5634

PNP
2N6229, 2N6230, 2N6231

FIGURE 12 – COLLECTOR CUTOFF REGION

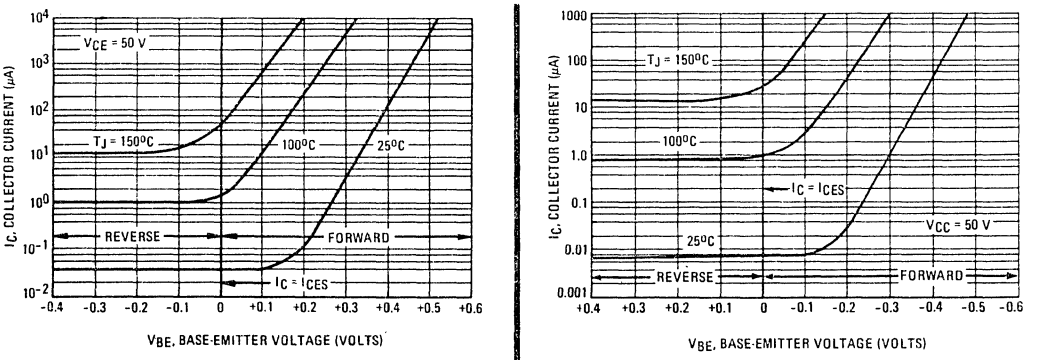
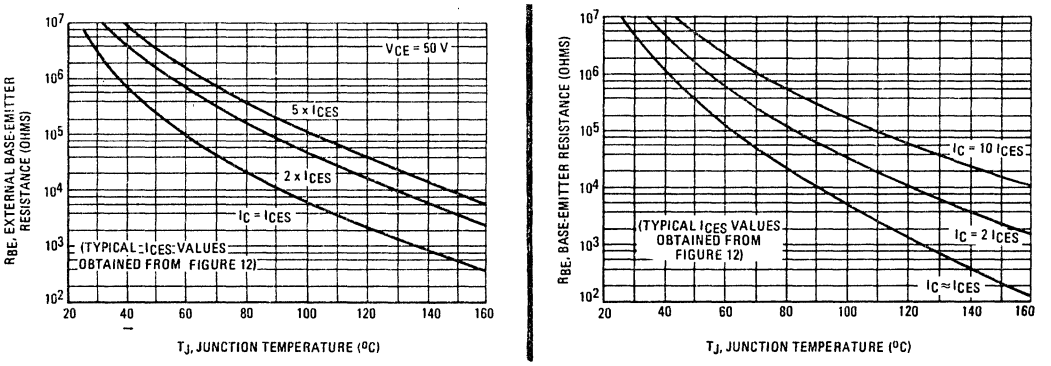


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



2N5655, 2N5656, 2N5657 (SILICON)

4

PLASTIC NPN SILICON HIGH-VOLTAGE POWER TRANSISTOR

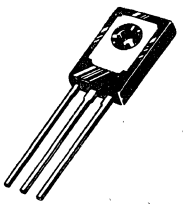
. . . designed for use in line-operated equipment such as audio output amplifiers; low-current, high-voltage converters; and AC line relays

- Excellent DC Current Gain – h_{FE} = 30-250 @ I_C = 100 mAdc
- Current-Gain – Bandwidth Product – f_T = 10 MHz (Min) @ I_C = 50 mAdc
- Packaged in Thermopad Case for Low Cost

0.5 AMPERE

POWER TRANSISTORS NPN SILICON

250-300-350 VOLTS 20 WATTS



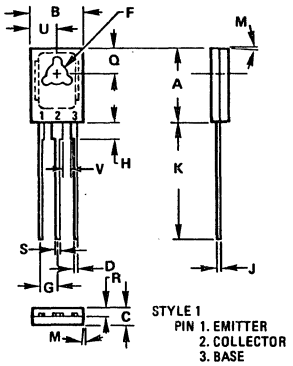
*MAXIMUM RATINGS

Rating	Symbol	2N5655	2N5656	2N5657	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
Collector-Base Voltage	V_{CB}	275	325	375	Vdc
Emitter-Base Voltage	V_{EB}	6.0			Vdc
Collector Current – Continuous Peak	I_C	0.5 1.0			Adc
Base Current	I_B	0.25			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

*Indicates JEDEC Registered Data



STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

FIGURE 1 – POWER DERATING

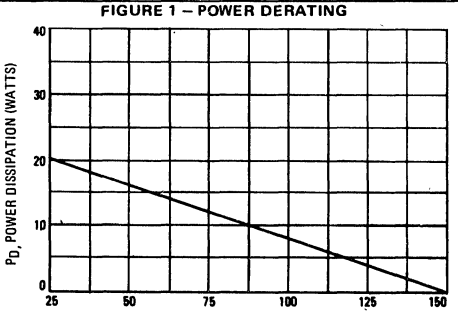
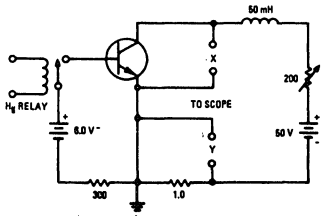


FIGURE 2 – SUSTAINING VOLTAGE TEST CIRCUIT



Safe Area Limits are indicated by Figures 3 and 4. Both limits are applicable and must be observed.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

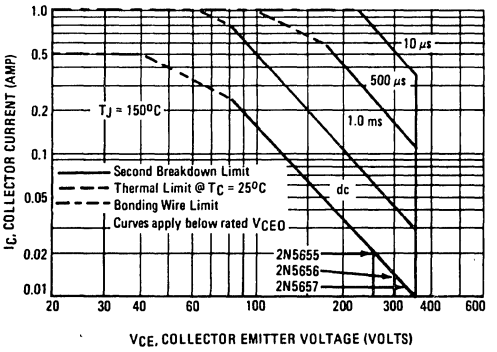
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc (inductive), L = 50 mH)	2N5655	$V_{CEO(sus)}$	250	–	Vdc
	2N5656		300	–	
	2N5657		350	–	
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	2N5655	BV_{CEO}	250	–	Vdc
	2N5656		300	–	
	2N5657		350	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 150 Vdc, I_B = 0)	2N5655		–	0.1	
(V_{CE} = 200 Vdc, I_B = 0)	2N5656		–	0.1	
(V_{CE} = 250 Vdc, I_B = 0)	2N5657		–	0.1	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5655		–	0.1	
(V_{CE} = 300 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5656		–	0.1	
(V_{CE} = 350 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5657		–	0.1	
(V_{CE} = 150 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N5655		–	1.0	
(V_{CE} = 200 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N5656		–	1.0	
(V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N5657		–	1.0	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 275 Vdc, I_E = 0)	2N5655		–	10	
(V_{CB} = 325 Vdc, I_E = 0)	2N5656		–	10	
(V_{CB} = 375 Vdc, I_E = 0)	2N5657		–	10	
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}		10	μAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 50 mAdc, V_{CE} = 10 Vdc)			25	–	
(I_C = 100 mAdc, V_{CE} = 10 Vdc)			30	250	
(I_C = 250 mAdc, V_{CE} = 10 Vdc)			15	–	
(I_C = 500 mAdc, V_{CE} = 10 Vdc)			5.0	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 100 mAdc, I_B = 10 mAdc)			–	1.0	
(I_C = 250 mAdc, I_B = 25 mAdc)			–	2.5	
(I_C = 500 mAdc, I_B = 100 mAdc)			–	10	
Base-Emitter Voltage (1) (I_C = 100 mAdc, V_{CE} = 10 Vdc)		V_{BE}	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (2) (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		f_T	10	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	25	pF
Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–

*Indicates JEDEC Registered Data for 2N5655 Series

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

FIGURE 3 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values loss than the limitations imposed by second breakdown.

4

LARGE SIGNAL CHARACTERISTICS

FIGURE 4 – TRANSCONDUCTANCE

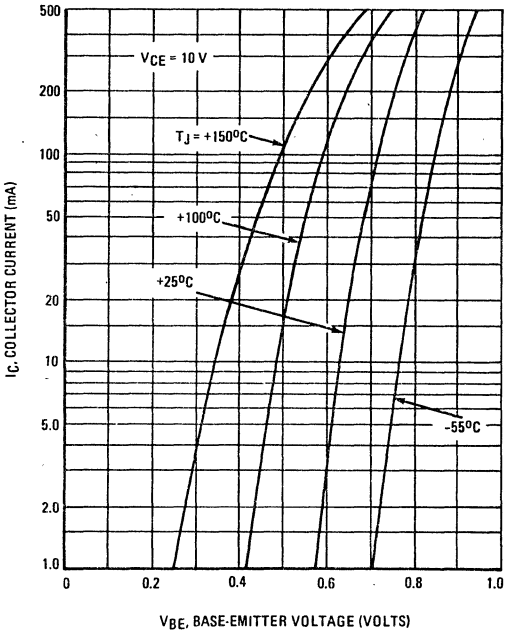
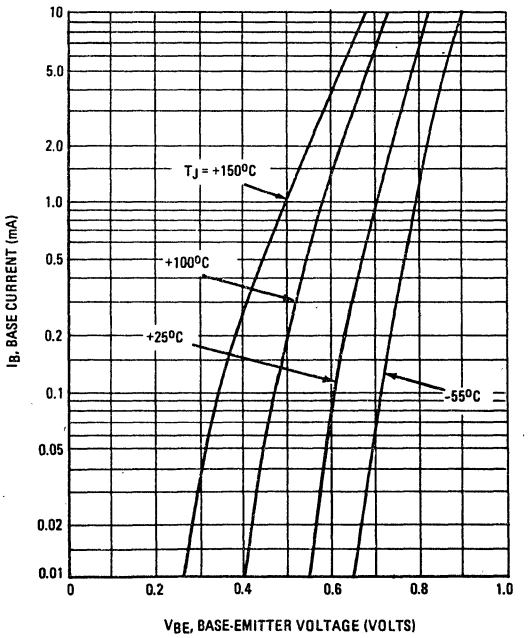


FIGURE 6 – INPUT ADMITTANCE



CUT-OFF CHARACTERISTICS

FIGURE 5 – TRANSCONDUCTANCE

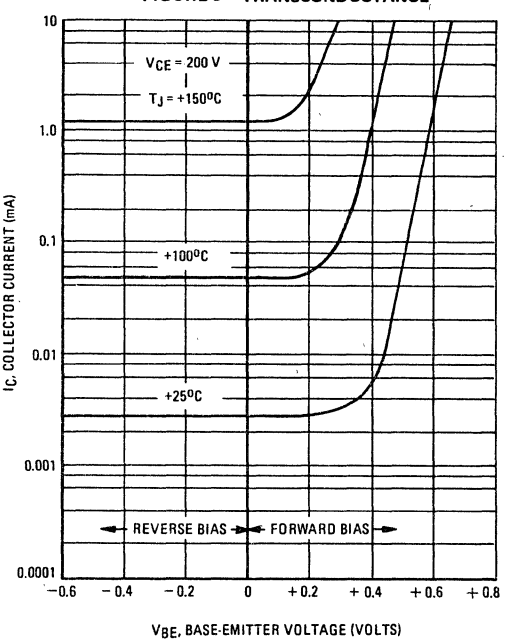


FIGURE 7 – EFFECT OF BASE-EMITTER RESISTANCE

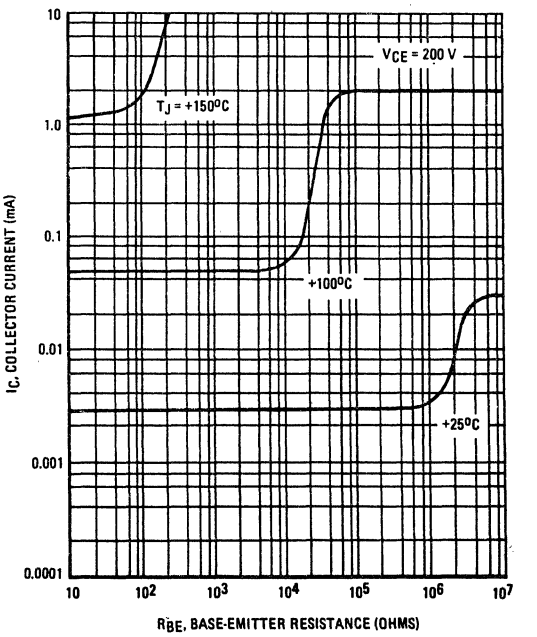


FIGURE 8 – CURRENT GAIN

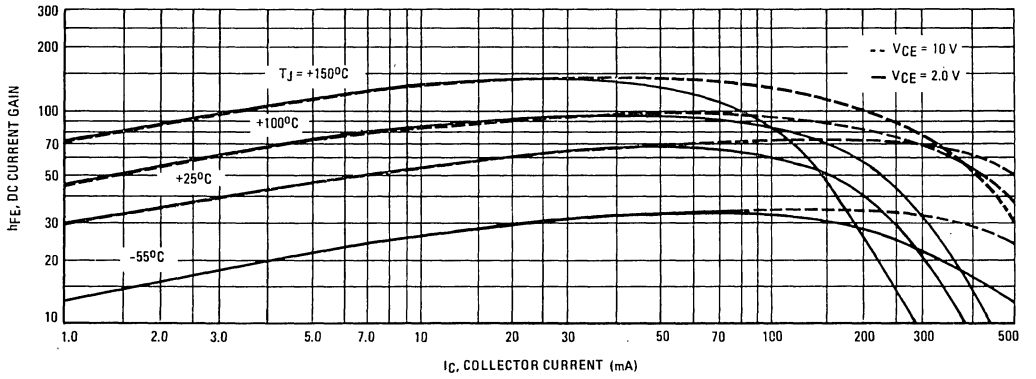


FIGURE 9 – "ON" VOLTAGES

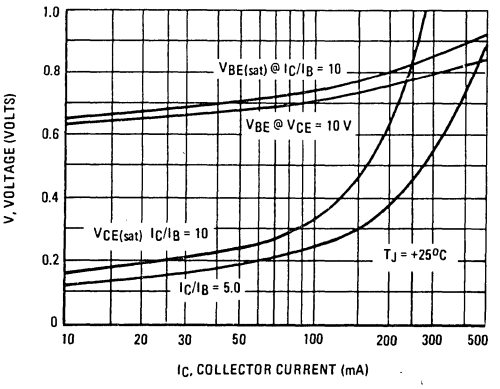


FIGURE 10 – CAPACITANCE

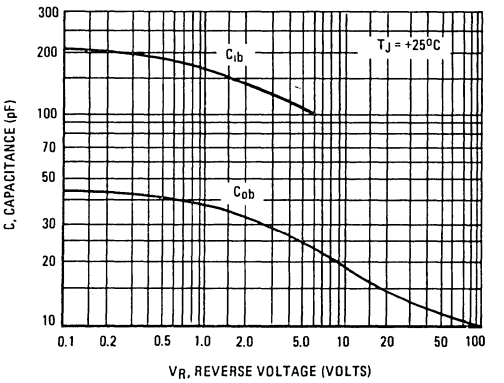


FIGURE 11 – TURN-ON TIME

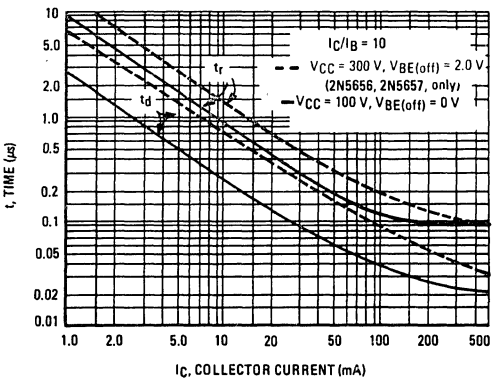
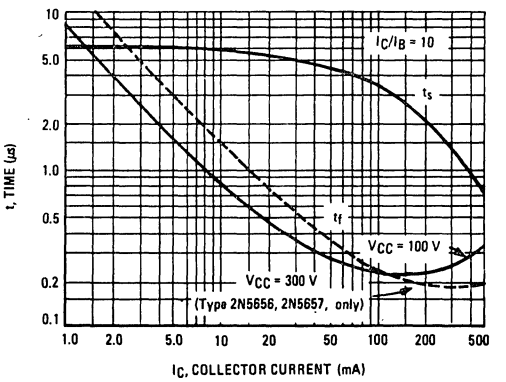


FIGURE 12 – TURN-OFF TIME



2N5683, 2N5684 PNP (SILICON)
2N5685, 2N5686 NPN

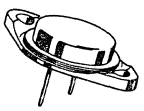
HIGH-CURRENT COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for use in high-power amplifier and switching circuit applications.

- High Current Capability – I_C Continuous = 50 Amperes.
- DC Current Gain – h_{FE} = 15 - 60 @ I_C = 25 Adc
- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 25 Adc

50 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60–80 VOLTS
300 WATTS



4

***MAXIMUM RATINGS**

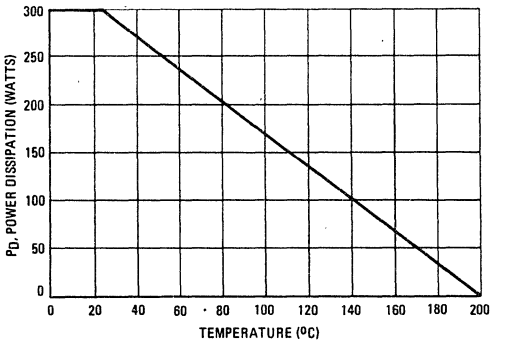
Rating	Symbol	2N5683 2N5685	2N5684 2N5686	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous	I_C	50		Adc
Base Current	I_B	15		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.715		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

***THERMAL CHARACTERISTICS**

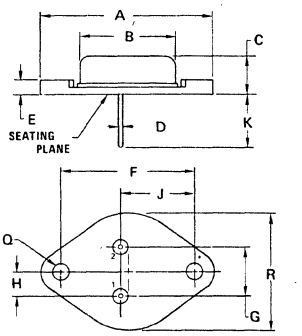
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.584	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
TO-3 Except Pin Diameter

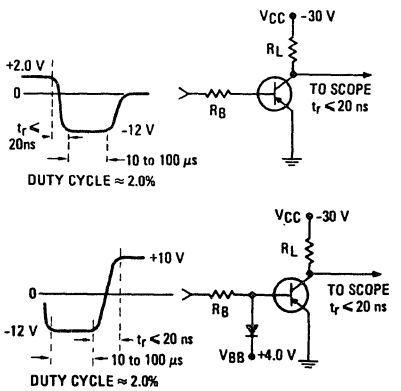
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Note 1)		$V_{CEO(sus)}$			Vdc
(I_C = 0.2 Adc, I_B = 0)	2N5683, 2N5685		60	–	
	2N5684, 2N5686		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N5683, 2N5685		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5684, 2N5686		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5683, 2N5685		–	2.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5684, 2N5686		–	2.0	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5683, 2N5685		–	10	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5684, 2N5686		–	10	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N5683, 2N5685		–	2.0	
(V_{CB} = 80 Vdc, I_E = 0)	2N5684, 2N5686		–	2.0	
Emitter Cutoff Current		I_{EBO}	–	5.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS					
DC Current Gain (Note 1)		h_{FE}			–
(I_C = 25 Adc, V_{CE} = 2.0 Vdc)			15	60	
(I_C = 50 Adc, V_{CE} = 5.0 Vdc)			5.0	–	
Collector-Emitter Saturation Voltage (Note 1)		$V_{CE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 2.5 Adc)			–	1.0	
(I_C = 50 Adc, I_B = 10 Adc)			–	5.0	
Base-Emitter Saturation Voltage (Note 1)		$V_{BE(sat)}$	–	2.0	Vdc
(I_C = 25 Adc, I_B = 2.5 Adc)					
Base-Emitter On Voltage (Note 1)		$V_{BE(on)}$	–	2.0	Vdc
(I_C = 25 Adc, V_{CE} = 2.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product		f_T	2.0	–	MHz
(I_C = 5.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)					
Output Capacitance	2N5683, 2N5684	C_{ob}	–	2000	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N5685, 2N5686		–	1200	
Small-Signal Current Gain		h_{fe}	15	–	
(I_C = 10 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)					

*Indicates JEDEC Registered Data

Note 1: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

FIGURE 3 – TURN-ON TIME

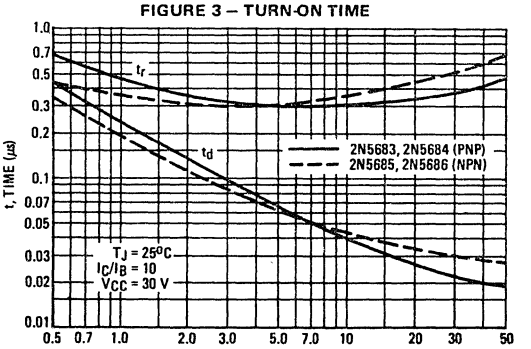


FIGURE 4 – THERMAL RESPONSE

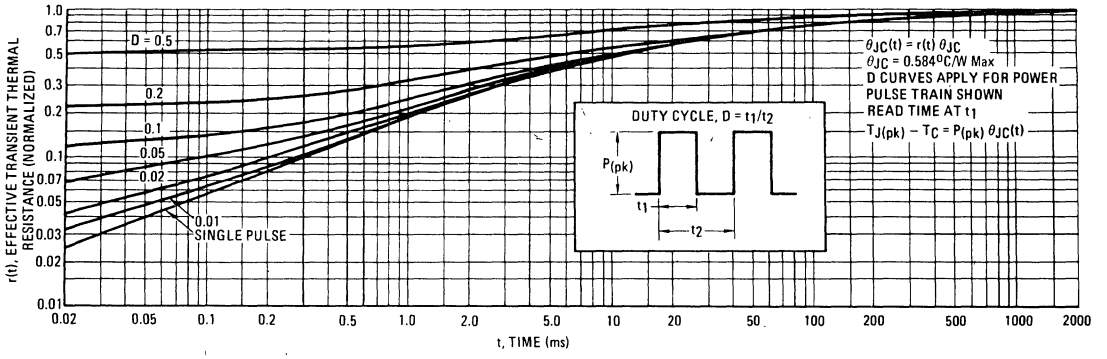
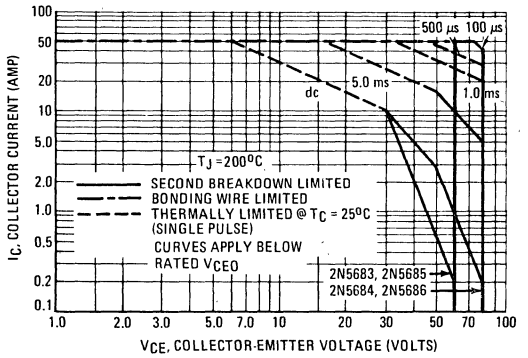


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

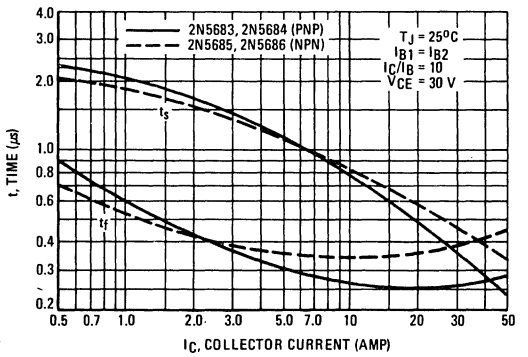
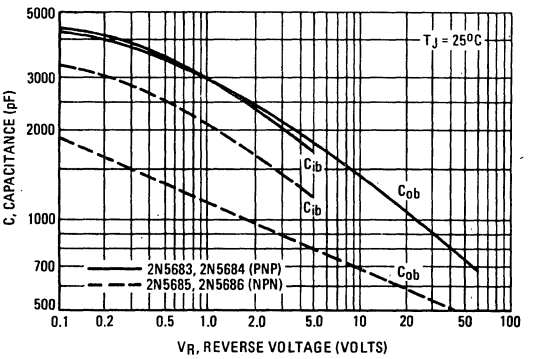


FIGURE 7 – CAPACITANCE



PNP
2N5683, 2N5684

NPN
2N5685, 2N5686

FIGURE 8 – DC CURRENT GAIN

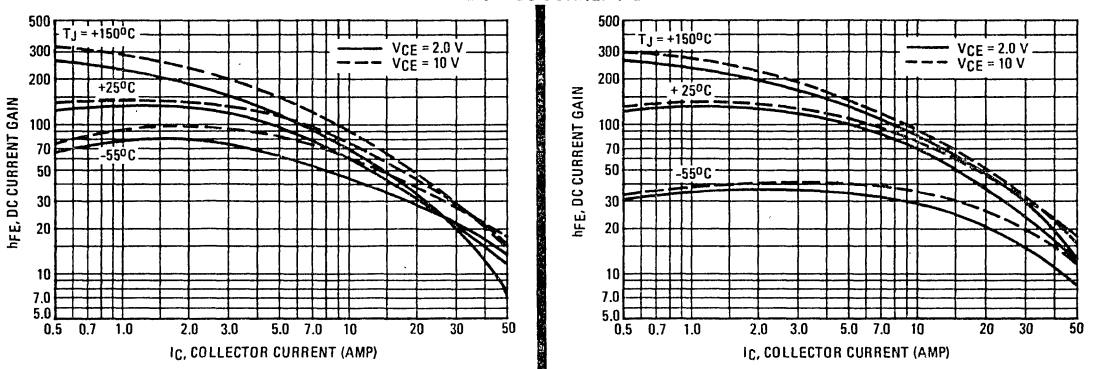


FIGURE 9 – COLLECTOR SATURATION REGION

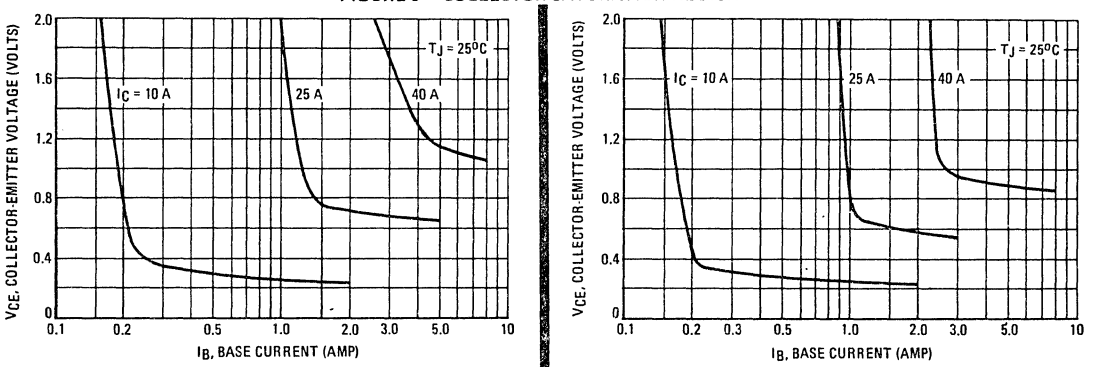
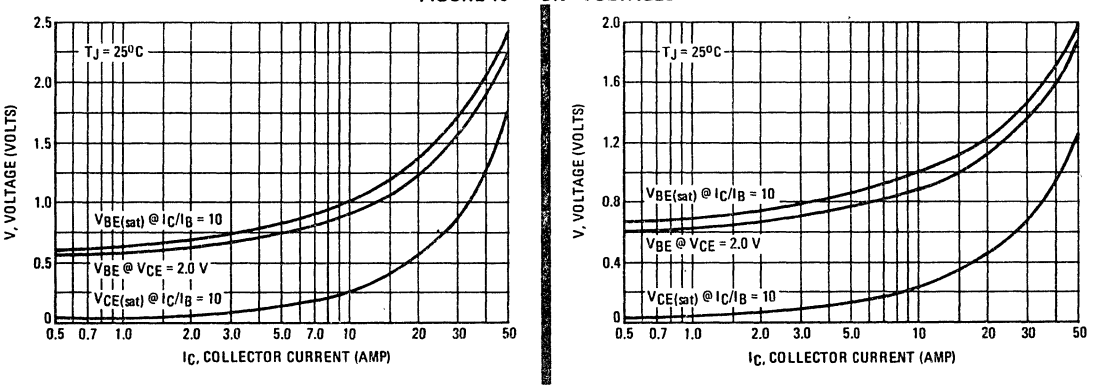


FIGURE 10 – "ON" VOLTAGES



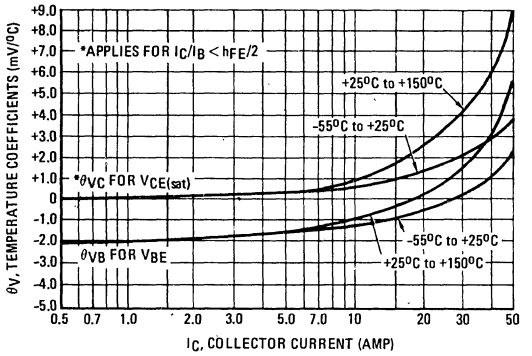
4

4

PNP
2N5683, 2N5684

NPN
2N5685, 2N5686

FIGURE 11 – TEMPERATURE COEFFICIENTS



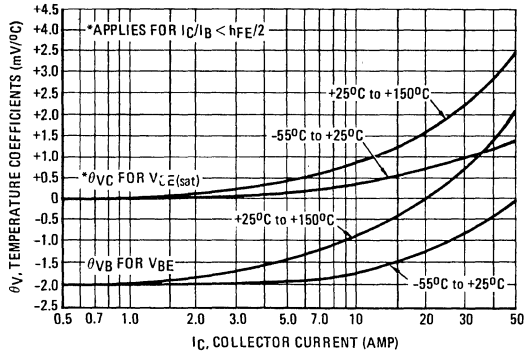
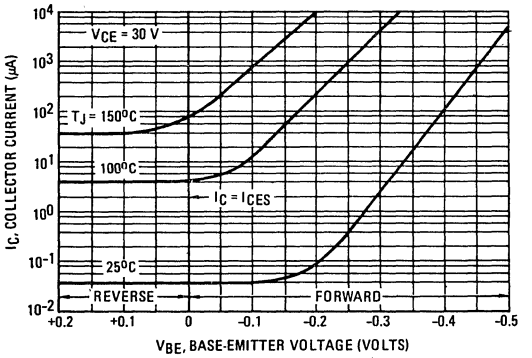


FIGURE 12 – COLLECTOR CUTOFF REGION



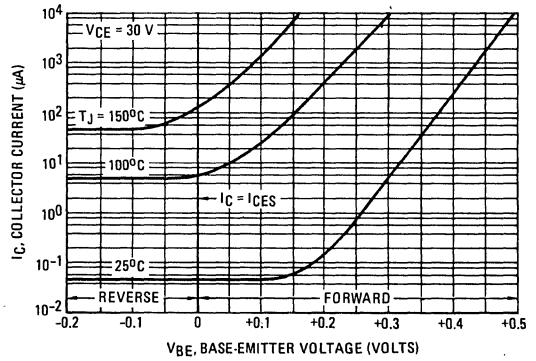
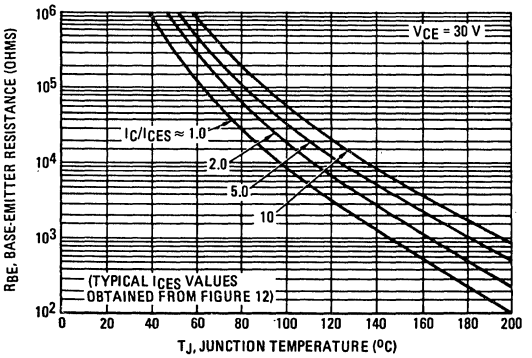
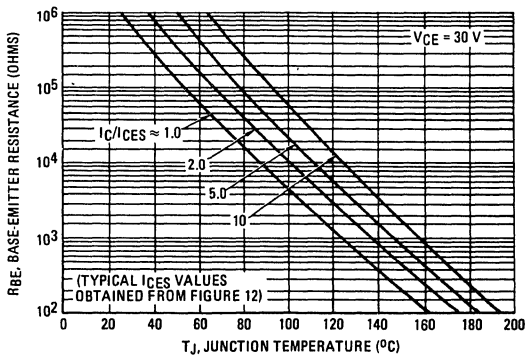


FIGURE 13 – EFFECT OF EXTERNAL BASE-EMITTER RESISTANCE





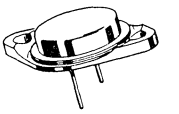
2N5758, 2N5759, 2N5760 NPN
2N6226, 2N6227, 2N6228 PNP

HIGH-VOLTAGE HIGH-POWER SILICON TRANSISTORS

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc (Min) – **2N5758, 2N6226**
  = 120 Vdc (Min) – **2N5759, 2N6227**
  = 140 Vdc (Min) – **2N5760, 2N6228**
- DC Current Gain @ I_C = 3.0 Adc –
  h_{FE} = 25 (Min) – **2N5758, 2N6226**
  = 20 (Min) – **2N5759, 2N6227**
  = 15 (Min) – **2N5760, 2N6228**
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 3.0 Adc

6 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON
100-120-140 VOLTS
150 WATTS



*MAXIMUM RATINGS

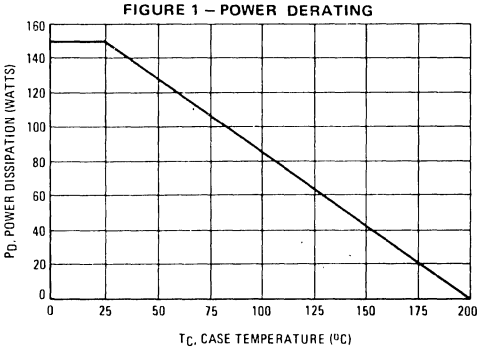
Rating	Symbol	2N5758 2N6226	2N5759 2N6227	2N5760 2N6228	Unit
Collector-Emitter Voltage	V_{CEO}	100	120	140	Vdc
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Emitter-Base Voltage	V_{EB}	← 7.0 →			Vdc
Collector Current - Continuous Peak	I_C	← 6.0 → ← 10 →			Adc
Base Current	I_B	← 4.0 →			Adc
Total Device Dissipation@T_C = 25°C Derate above 25°C	P_D	← 150 → ← 0.857 →			Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

THERMAL CHARACTERISTICS

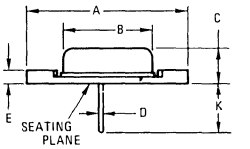
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING

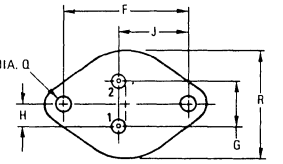


Safe area limits are indicated by Figure 5.
Both limits are applicable and must be observed.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

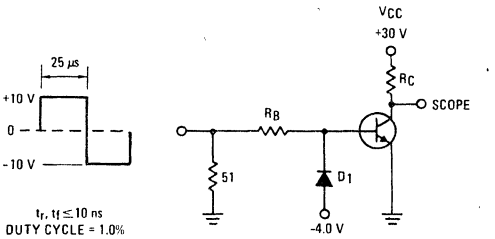
Collector connected to case.
CASE 11-01
TO-3

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0	2N5758, 2N6226		100	–	
	2N5759, 2N6227		120	–	
	2N5760, 2N6228		140	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 50 Vdc, I_B = 0)	2N5758, 2N6226		–	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N5759, 2N6227		–	1.0	
(V_{CE} = 70 Vdc, I_B = 0)	2N5760, 2N6228		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)			–	1.0	
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	5.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = Rated V_{CB}, I_E = 0)			–	1.0	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 7.0 Vdc, I_C = 0)			–	1.0	
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)	2N5758, 2N6226		25	100	
	2N5759, 2N6227		20	80	
	2N5760, 2N6228		15	60	
(I_C = 6.0 Adc, V_{CE} = 2.0 Vdc)	All Types		5.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 0.3 Adc)			–	1.0	
(I_C = 6.0 Adc, I_B = 1.2 Adc)			–	2.0	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)			–	1.5	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T			MHz
(I_C = 0.5 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)			1.0	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)			–	300	
Small-Signal Current Gain		h_{fe}			–
(I_C = 2.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)			15	–	

*Indicates JEDEC Registered Data
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE I_B ≈ 100 mA
MSD6100 USED BELOW I_B ≈ 100 mA

***For PNP test circuit, reverse all polarities and D1.**

NPN
2N5758, 2N5759, 2N5760

PNP
2N6226, 2N6227, 2N6228

FIGURE 3 – TURN-ON TIME

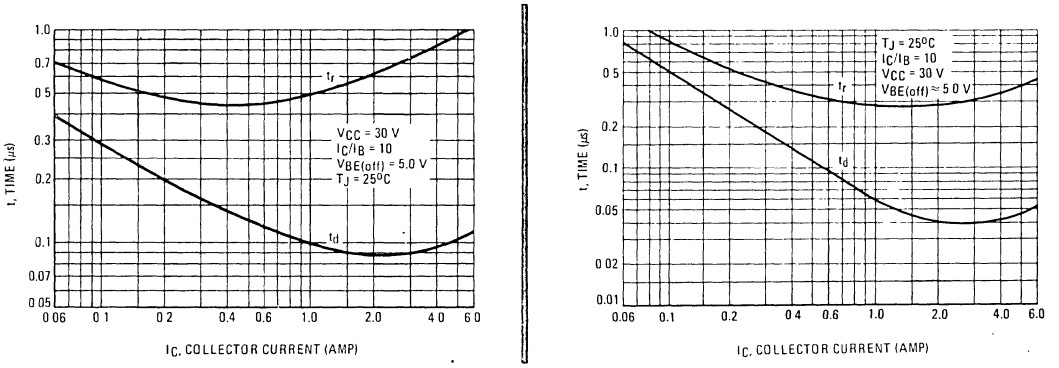


FIGURE 4 – THERMAL RESPONSE

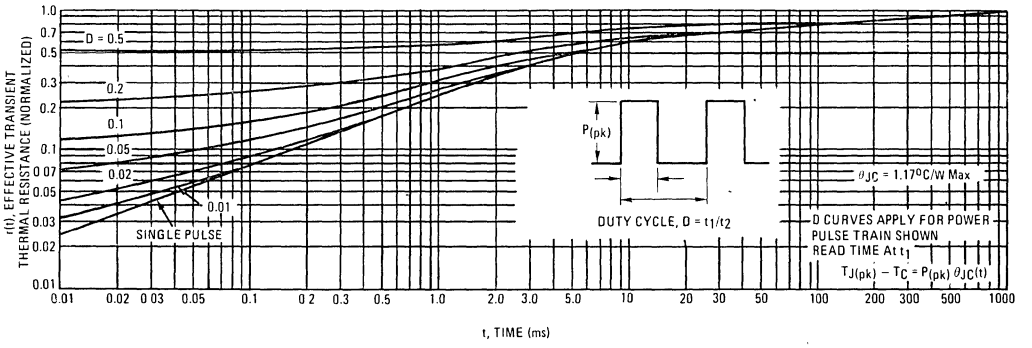
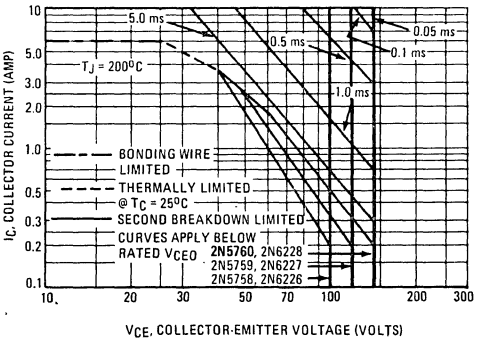


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



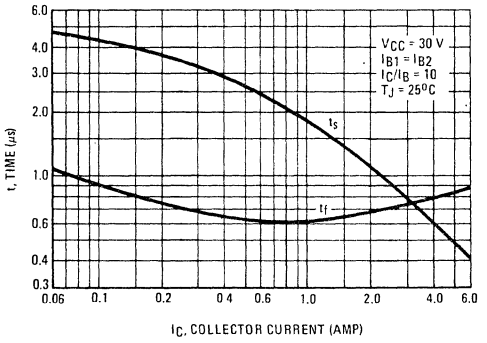
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN
2N5758, 2N5759, 2N5760

PNP
2N6226, 2N6227, 2N6228

FIGURE 6 – TURN-OFF TIME



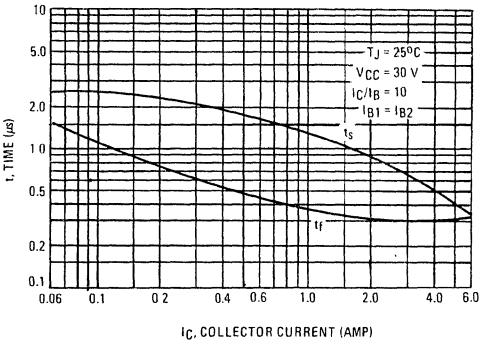
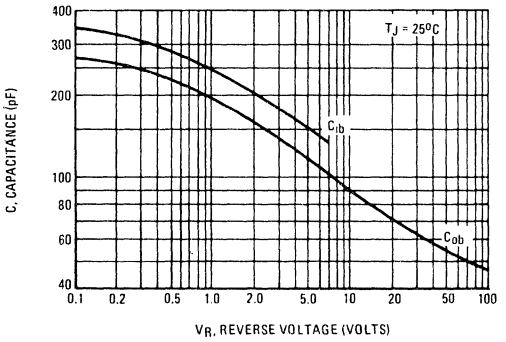


FIGURE 7 – CAPACITANCE



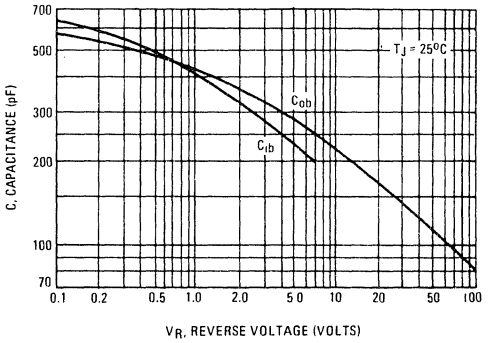
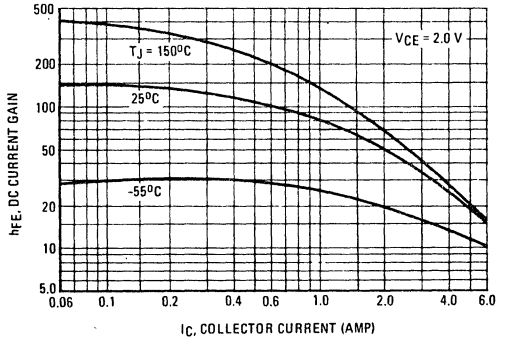
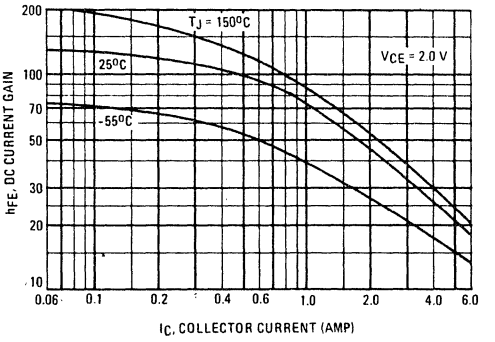


FIGURE 8 – DC CURRENT GAIN





NPN
2N5758, 2N5759, 2N5760

PNP
2N6226, 2N6227, 2N6228

FIGURE 9 – COLLECTOR SATURATION REGION

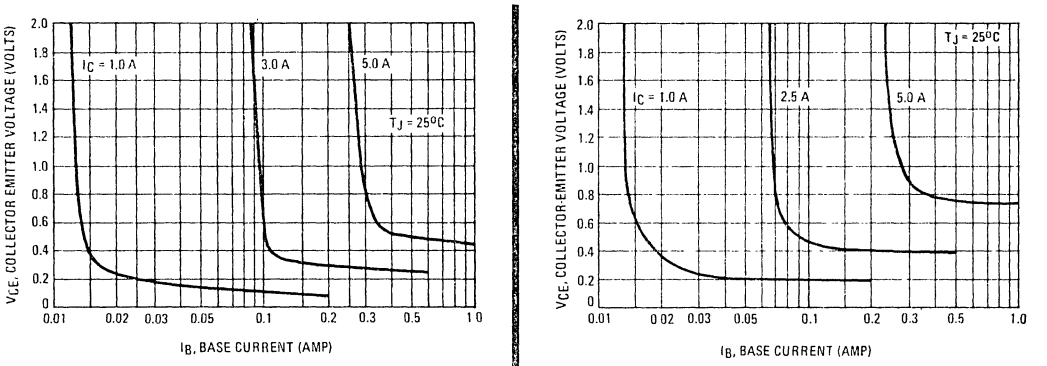


FIGURE 10 – "ON" VOLTAGES

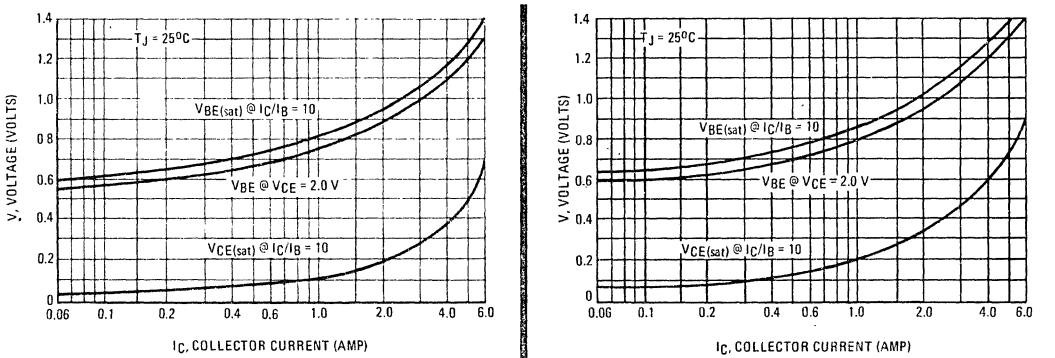
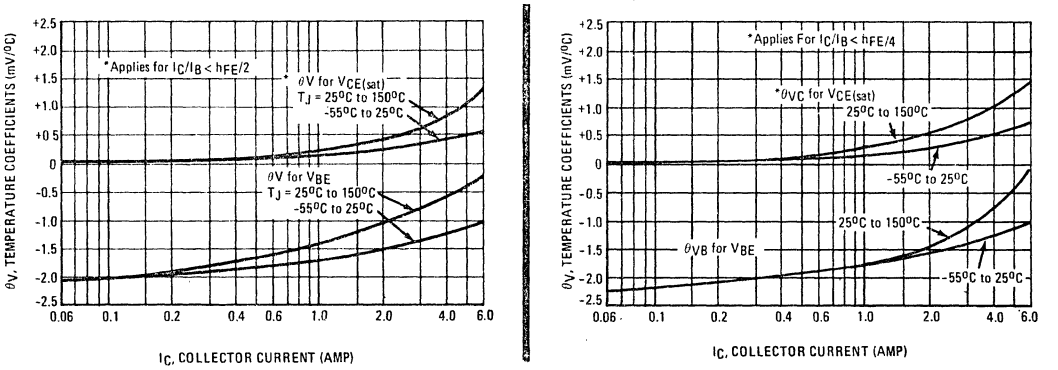


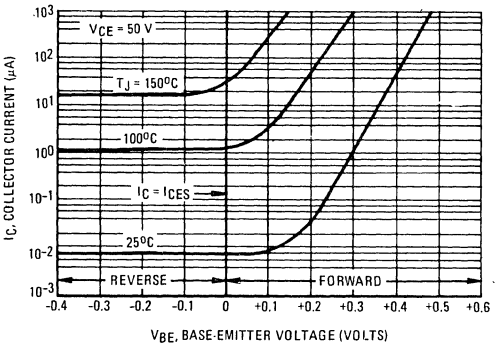
FIGURE 11 – TEMPERATURE COEFFICIENTS



NPN
2N5758, 2N5759, 2N5760

PNP
2N6226, 2N6227, 2N6228

FIGURE 12 – COLLECTOR CUT-OFF REGION



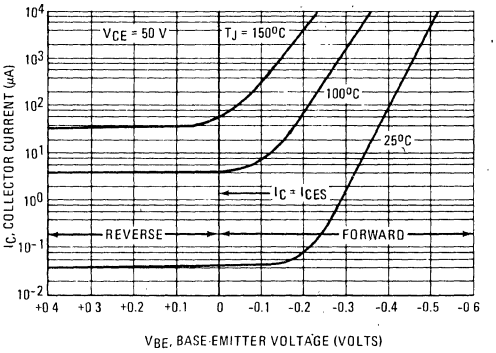
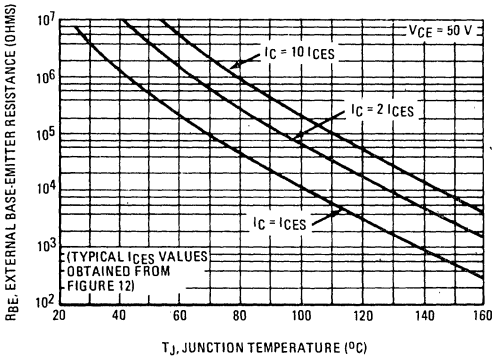
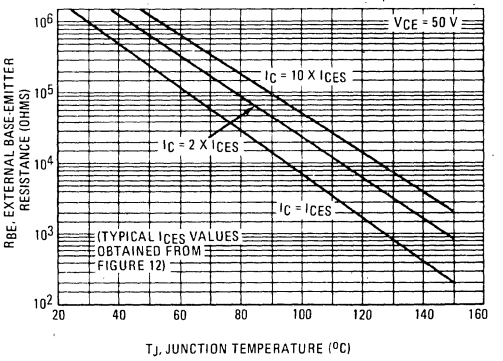


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE





2N5875, 2N5876 PNP (SILICON)
2N5877, 2N5878 NPN

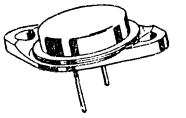
COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

. . . designed for general-purpose power amplifier and switching applications.

- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 5.0 Adc
- Low Leakage Current –
  I_{CEX} = 0.5 mAdc (Max) @ Rated Voltage
- Excellent DC Current Gain –
  h_{FE} = 20 (Min) @ I_C = 4.0 Adc
- High Current Gain – Bandwidth Product –
  f_T = 4.0 MHz (Min) @ I_C = 0.5 A

10 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS
150 WATTS



4

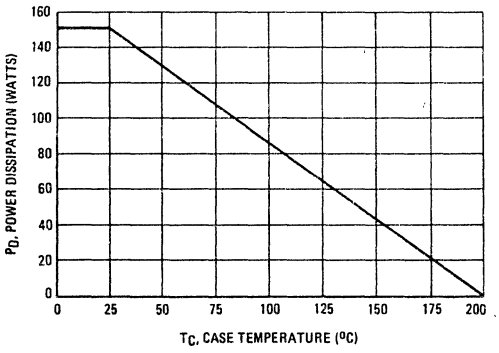
*MAXIMUM RATINGS

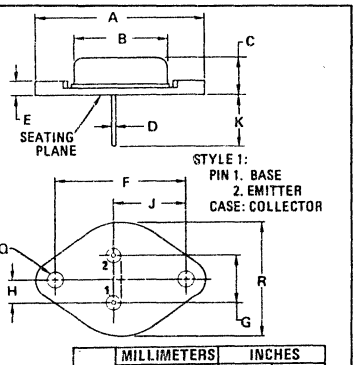
Rating	Symbol	2N5875 2N5877	2N5876 2N5878	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous Peak	I_C	10 20		Adc
Base Current	I_B	4.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.857		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

FIGURE 1 – POWER DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-01
TO-3

NOTE:
1. DIM "Q" IS DIA.

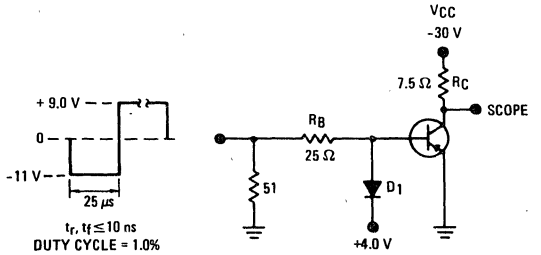
Collector connected to case.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N5875, 2N5877		60	–	
	2N5876, 2N5878		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N5875, 2N5877		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5876, 2N5878		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5875, 2N5877		–	0.5	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5876, 2N5878		–	0.5	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5875, 2N5877		–	5.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5876, 2N5878		–	5.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N5875, 2N5877		–	0.5	
(V_{CB} = 80 Vdc, I_E = 0)	2N5876, 2N5878		–	0.5	
Emitter Cutoff Current		I_{EBO}	–	1.0	mAdc
(V_{EB} = 5.0 Vdc, I_E = 0)					
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			35	–	
(I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)			20	100	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)			4.0	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 0.5 Adc)			–	1.0	
(I_C = 10 Adc, I_B = 2.5 Adc)			–	3.0	
Base-Emitter Saturation Voltage (1)		$V_{BE(sat)}$	–	2.5	Vdc
(I_C = 10 Adc, I_B = 2.5 Adc)					
Base-Emitter On Voltage (1)		$V_{BE(on)}$	–	1.5	Vdc
(I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (2)		f_T	4.0	–	MHz
(I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)					
Output Capacitance		C_{ob}	–		pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N5875, 2N5876		–	500	
	2N5877, 2N5878		–	300	
Small-Signal Current Gain		h_{fe}	20	–	–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)					
SWITCHING CHARACTERISTICS					
Rise Time	(V_{CC} = 30 Vdc, I_C = 4.0 Adc, I_{B1} = I_{B2} = 0.4 Adc, See Figure 2)	t_r	–	0.7	μs
Storage Time		t_s	–	1.0	μs
Fall Time		t_f	–	0.8	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



t_r, $t_f \leq 10$ ns
DUTY CYCLE = 1.0%

FOR CURVES OF FIGURES 3 and 6, R_B and R_C ARE VARIED TO OBTAIN DESIRED CURRENT LEVELS

For NPN test circuit, reverse all polarities.

D_1 MUST BE FAST RECOVERY TYPE, e.g.
MBD5300 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

FIGURE 3 – TURN-ON TIME

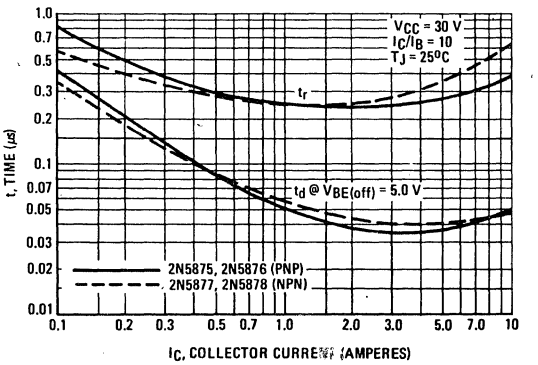


FIGURE 4 – THERMAL RESPONSE

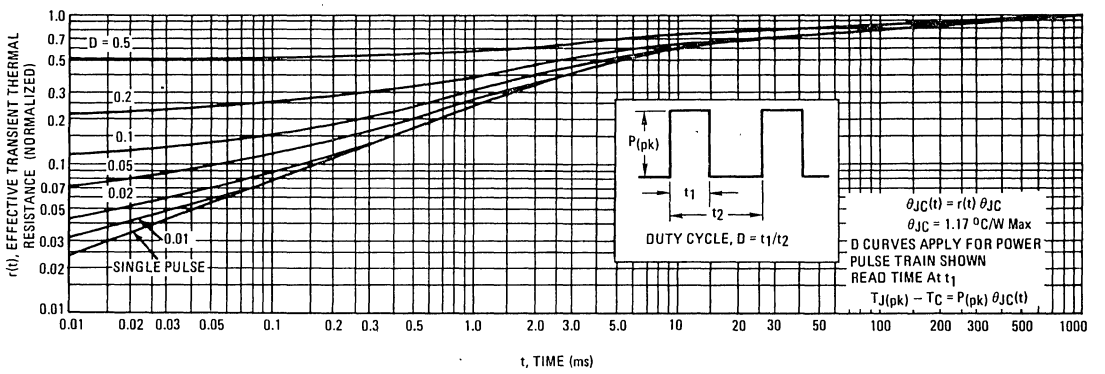


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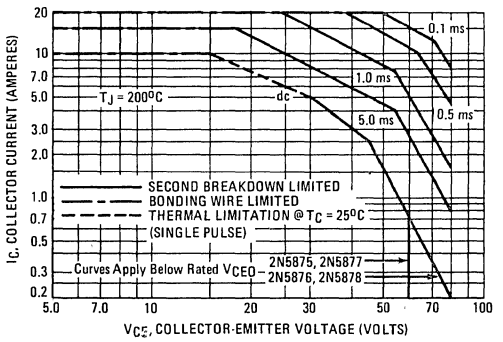
FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

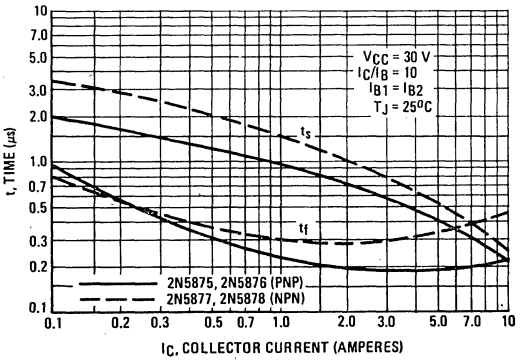
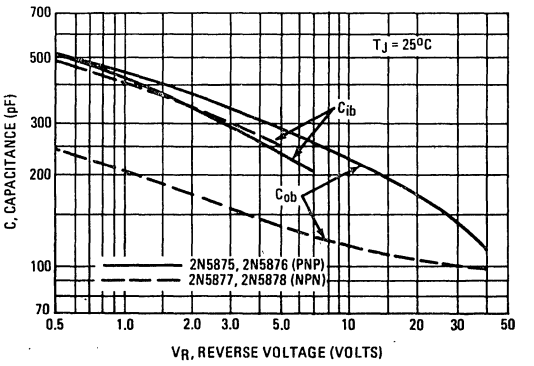


FIGURE 7 – CAPACITANCE



PNP DEVICES
2N5875 and 2N5876

NPN DEVICES
2N5877 and 2N5878

FIGURE 8 – DC CURRENT GAIN

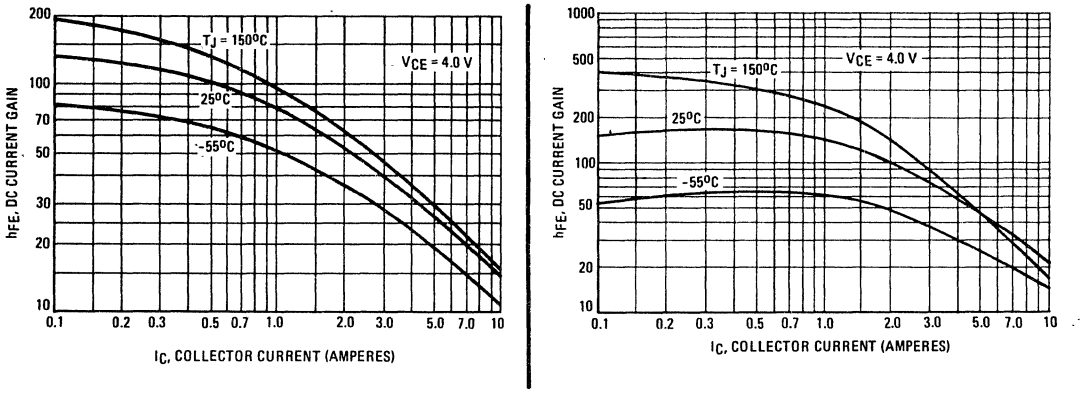


FIGURE 9 – COLLECTOR SATURATION REGION

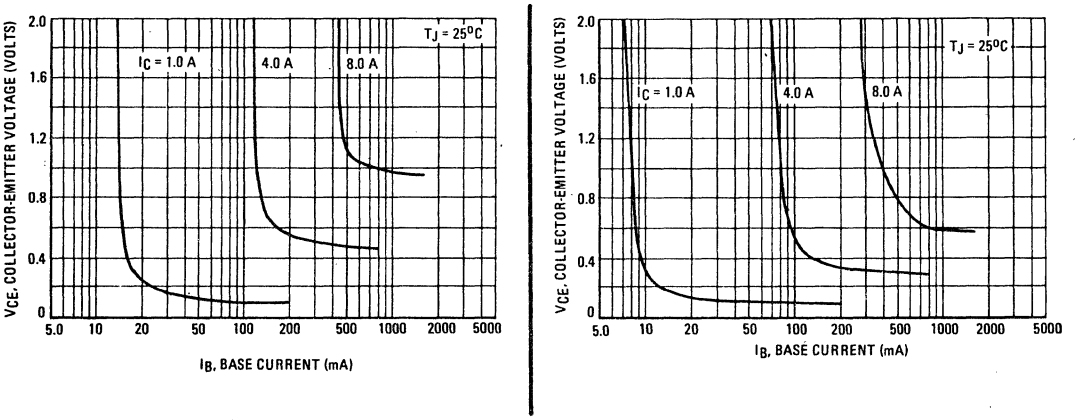
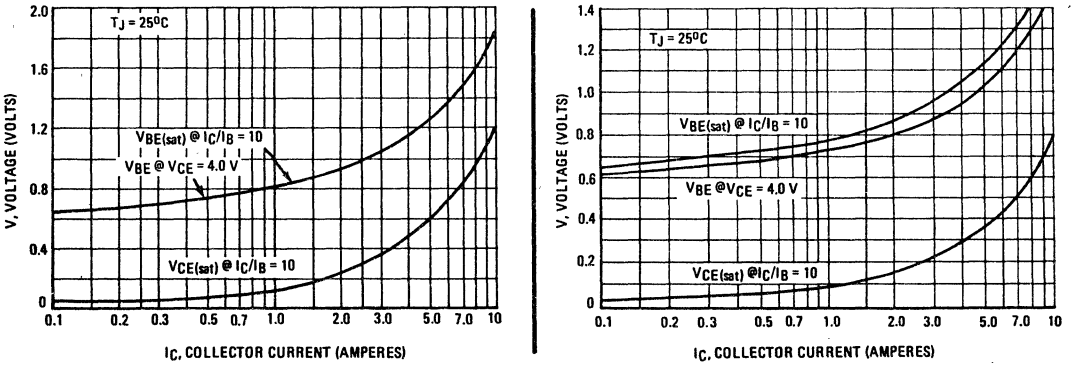


FIGURE 10 – "ON" VOLTAGES



PNP DEVICES
2N5875 and 2N5876

NPN DEVICES
2N5877 and 2N5878

FIGURE 11 – TEMPERATURE COEFFICIENTS

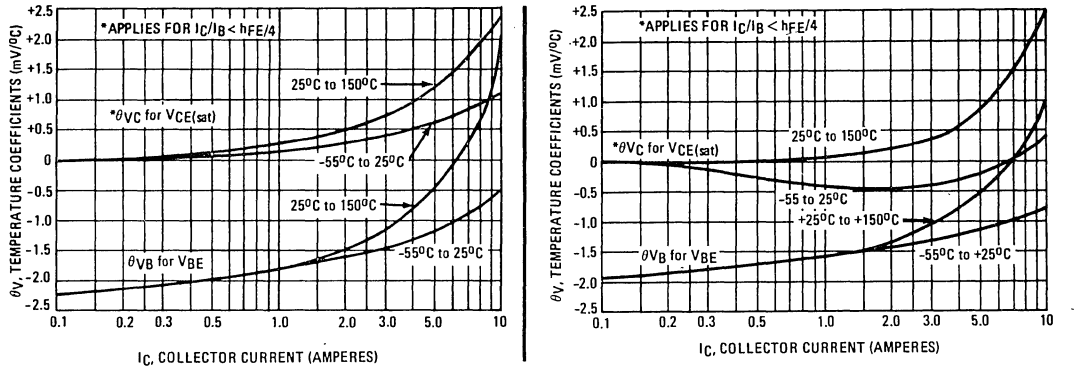


FIGURE 12 – COLLECTOR CUT-OFF REGION

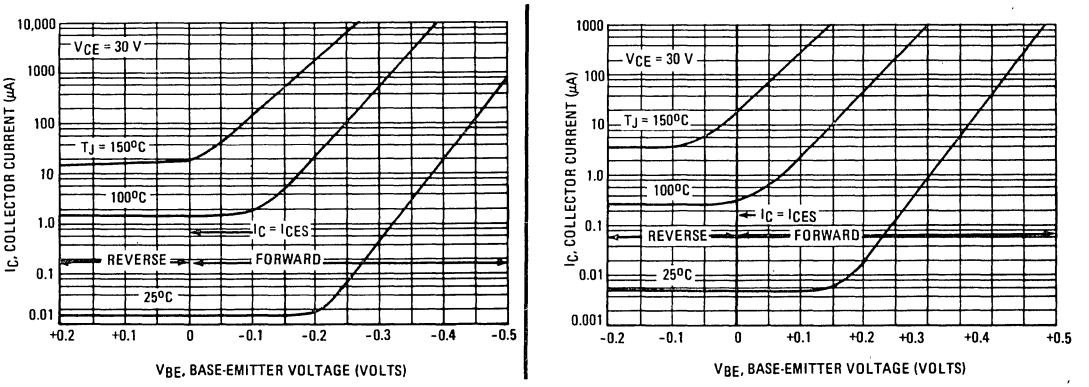
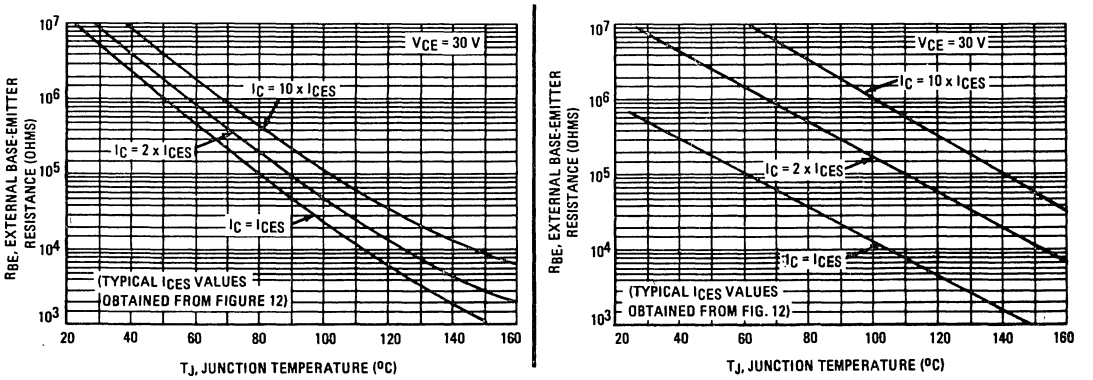


FIGURE 13 – EFFECTS OF EXTERNAL BASE-EMITTER RESISTANCE



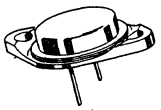
2N5879, 2N5880, PNP (SILICON)
2N5881, 2N5882 NPN

COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

. . . designed for general-purpose power amplifier and switching applications.

- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N5879, 2N5881
  = 80 Vdc (Min) — 2N5880, 2N5882
- DC Current Gain —
  h_{FE} = 20 (Min) @ I_C = 6.0 Adc
- Low Collector — Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 7.0 Adc
- High Current — Gain-Bandwidth Product —
  f_T = 4.0 MHz (Min) @ I_C = 1.0 Adc
- Recommended for New Circuit Designs

15 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60-80 VOLTS
160 WATTS



4

*MAXIMUM RATINGS

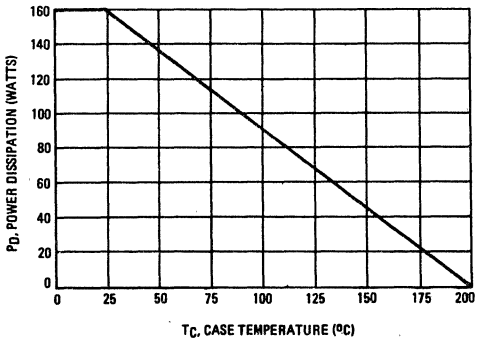
Rating	Symbol	2N5879 2N5881	2N5880 2N5882	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	15 30		Adc
Base Current	I_B	5.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	160 0.915		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200		°C

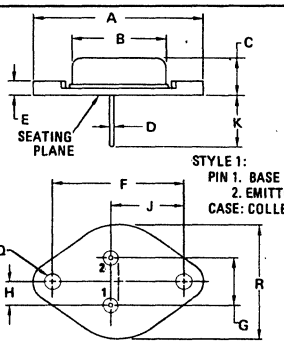
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.1	°C/W

*Indicates JEDEC registered data. Limits and conditions differ on some parameters and re-registration reflecting these changes has been requested. All above values meet or exceed present JEDEC registered data.

FIGURE 1 — POWER DERATING





CASE 11-01
TO-3

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

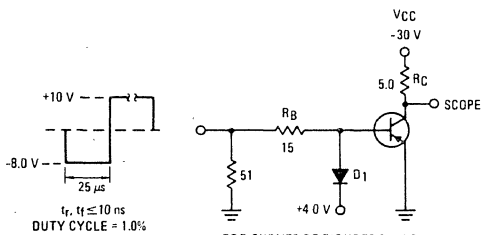
NOTE:
1. DIM "Q" IS DIA.
Collector connected to case.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N5879, 2N5881		60	–	
	2N5880, 2N5882		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N5879, 2N5881		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5880, 2N5882		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5879, 2N5881		–	0.5	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5880, 2N5882		–	0.5	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5879, 2N5881		–	5.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5880, 2N5882		–	5.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N5879, 2N5881		–	0.5	
(V_{CB} = 80 Vdc, I_E = 0)	2N5880, 2N5882		–	0.5	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)			35	–	
(I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)			20	100	
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)			4.0	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 7.0 Adc, I_B = 0.7 Adc)			–	1.0	
(I_C = 15 Adc, I_B = 3.75 Adc)			–	4.0	
Base-Emitter Saturation Voltage (1) (I_C = 15 Adc, I_B = 3.75 Adc)		$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (1) (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	4.0	–	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	2N5879, 2N5880		–	600	
	2N5881, 2N5882		–	400	
Small-Signal Current Gain (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–
SWITCHING CHARACTERISTICS					
Rise Time	(V_{CC} = 30 Vdc, I_C = 6.0 Adc, I_{B1} = I_{B2} = 0.6 Adc *See Figure 2*)	t_r	–	0.7	μs
Storage Time		t_s	–	1.0	μs
Fall Time		t_f	–	0.8	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



For NPN test circuit, reverse all polarities.

FOR CURVES OF FIGURES 3 and 6, R_B and R_C ARE VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE I_B ≈ 100 mA
MSD6100 USED BELOW I_B ≈ 100 mA

FIGURE 3 – TURN-ON TIME

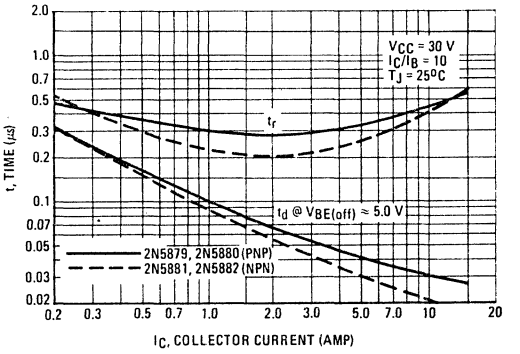
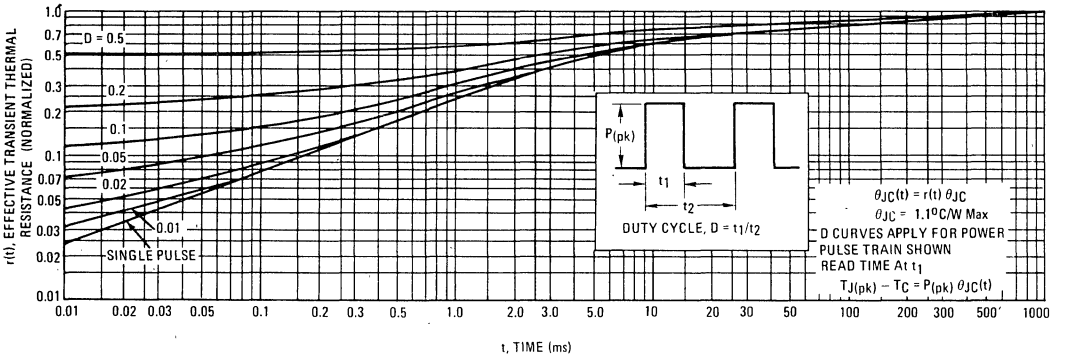
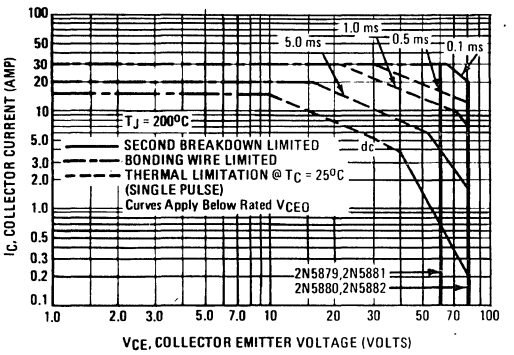


FIGURE 4 – THERMAL RESPONSE



4

FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

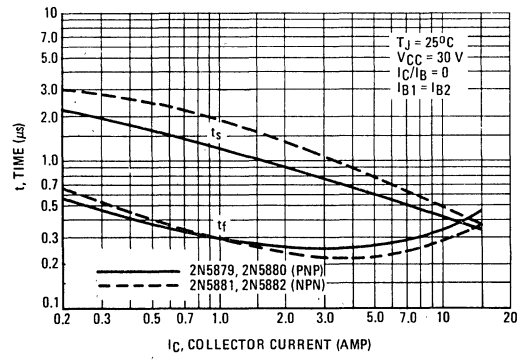
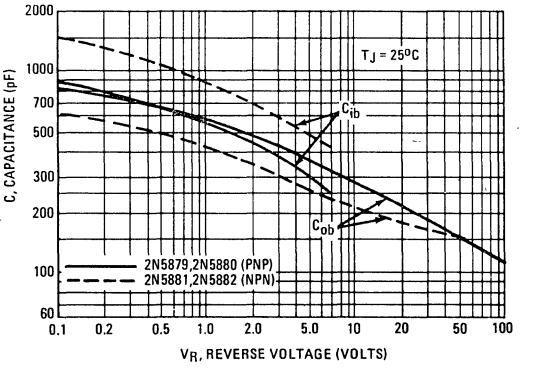


FIGURE 7 – CAPACITANCE



PNP
2N5879, 2N5880

NPN
2N5881, 2N5882

FIGURE 8 – DC CURRENT GAIN

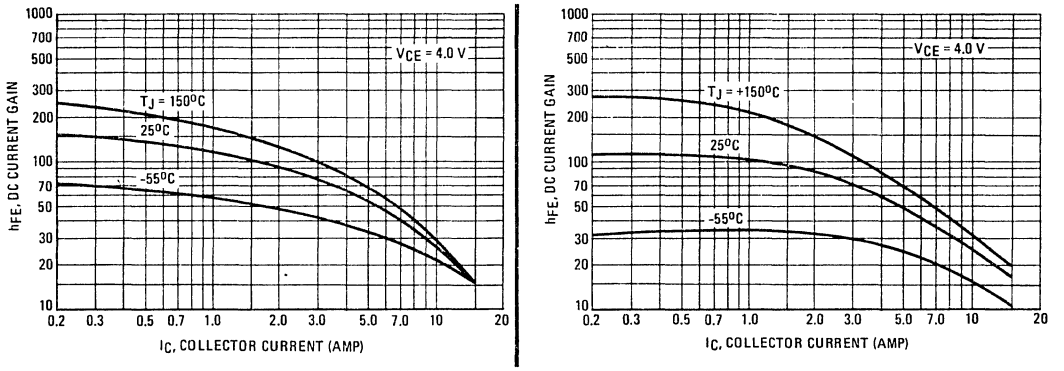


FIGURE 9 – COLLECTOR SATURATION REGION

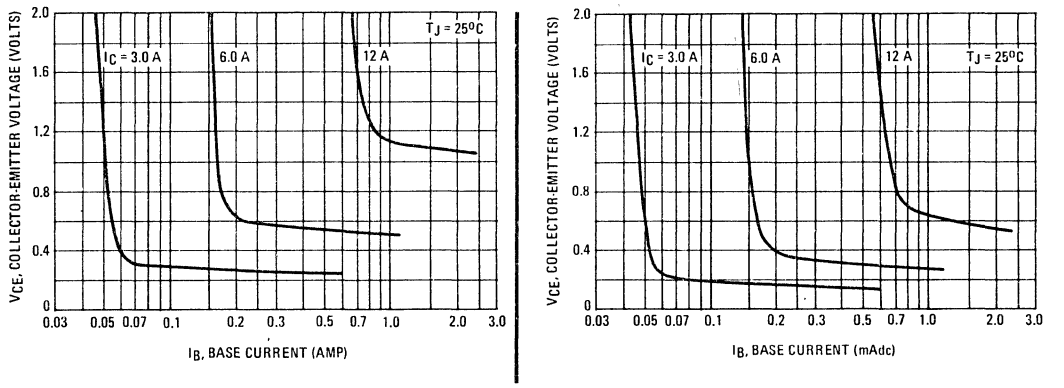
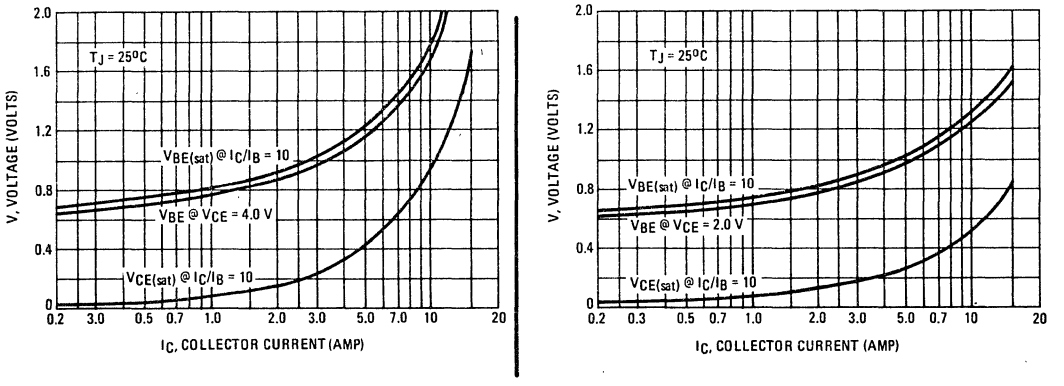


FIGURE 10 – "ON" VOLTAGES



PNP
2N5879, 2N5880

NPN
2N5881, 2N5882

FIGURE 11 – TEMPERATURE COEFFICIENTS

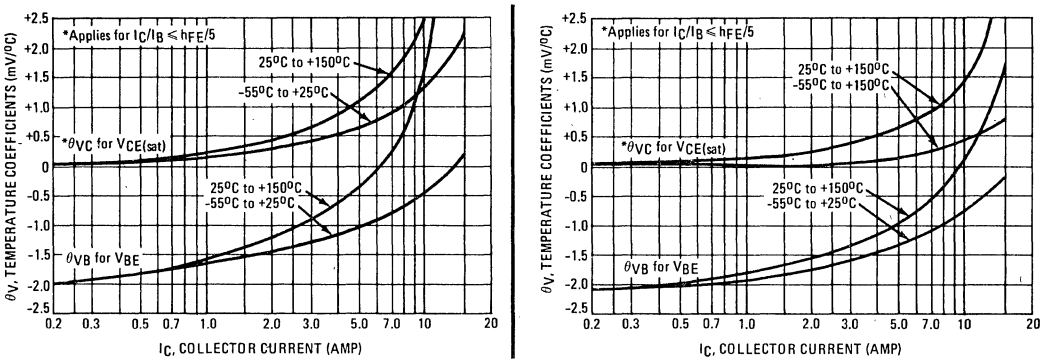


FIGURE 12 – COLLECTOR CUTOFF REGION

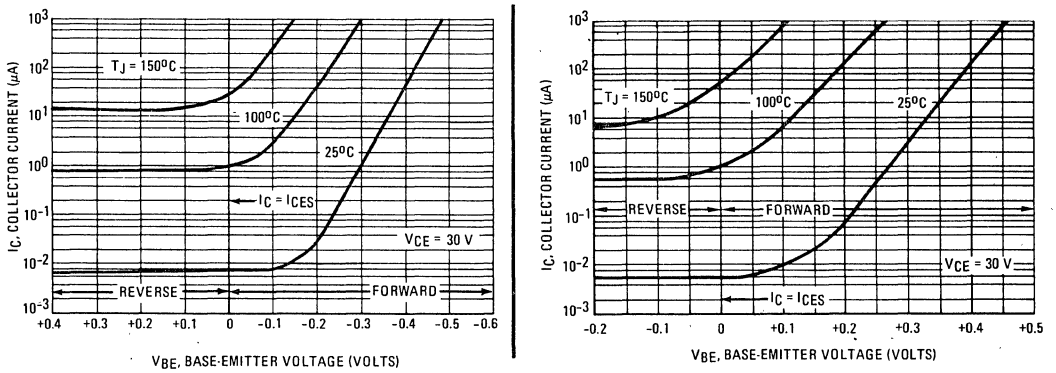
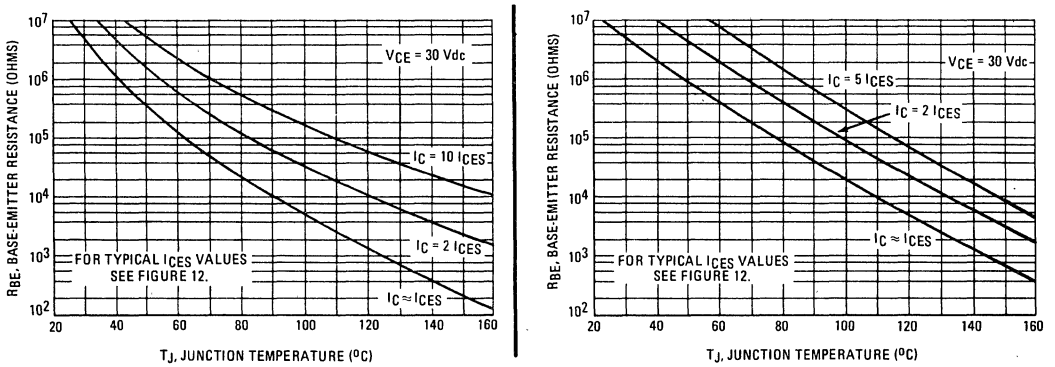


FIGURE 13 – EFFECTS OF EXTERNAL BASE-EMITTER RESISTANCE



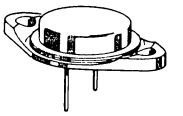
2N5883, 2N5884 PNP (SILICON)
2N5885, 2N5886 NPN

COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

. . . designed for general-purpose power amplifier and switching applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 Vdc, (max) at I_C = 15 Adc
- Low Leakage Current I_{CEX} = 1.0 mAdc (max) at Rated Voltage
- Excellent DC Current Gain — h_{FE} = 20 (min) at I_C = 10 Adc
- High Current Gain Bandwidth Product — f_T = 4.0 MHz (min) at I_C = 1.0 Adc

25 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60-80 VOLTS
200 WATTS



4

*MAXIMUM RATINGS

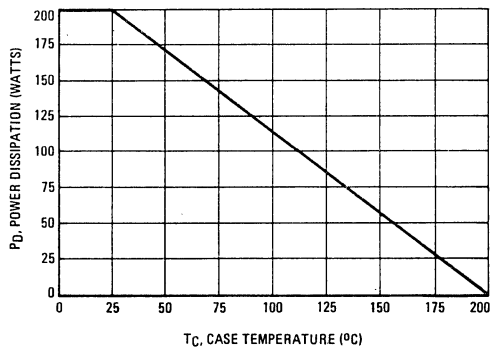
Rating	Symbol	2N5883 2N5885	2N5884 2N5886	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	25 50		Adc
Base Current	I_B	7.5		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.15		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200		°C

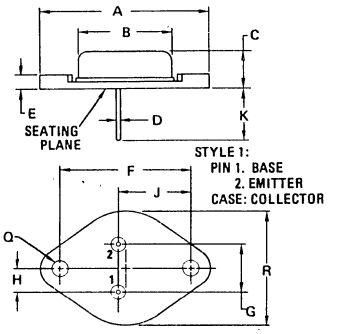
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

*Indicates JEDEC registered data. Limits and conditions differ on some parameters and re-registration reflecting these changes has been requested. All above values meet or exceed present JEDEC registered data.

FIGURE 1 — POWER DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

NOTE: Collector connected to case.
1. DIM "Q" IS DIA. CASE 11-01
TO-3

2N5883, 2N5884 PNP, 2N5885, 2N5886 NPN

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

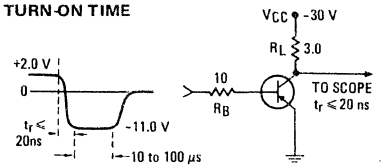
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N5883, 2N5885		60	–	
	2N5884, 2N5886		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N5883, 2N5885		–	2.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5884, 2N5886		–	2.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5883, 2N5885		–	1.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5884, 2N5886		–	1.0	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5883, 2N5885		–	10	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5884, 2N5886		–	10	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N5883, 2N5885		–	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	2N5884, 2N5886		–	1.0	
Emitter Cutoff Current		I_{EBO}	–	1.0	mAdc
(V_{EB} = 5.0 Vdc, I_C = 0					
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			35	–	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)			20	100	
(I_C = 25 Adc, V_{CE} = 4.0 Vdc)			4.0	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 15 Adc, I_B = 1.5 Adc)			–	1.0	
(I_C = 25 Adc, I_B = 6.25 Adc)			–	4.0	
Base-Emitter Saturation Voltage (1)		$V_{BE(sat)}$	–	2.5	Vdc
(I_C = 25 Adc, I_B = 6.25 Adc)					
Base-Emitter On Voltage (1)		$V_{BE(on)}$	–	1.5	Vdc
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (2)		f_T	4.0	–	MHz
(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)					
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N5883, 2N5884		–	1000	
	2N5885, 2N5886		–	500	
Small-Signal Current Gain		h_{fe}	20	–	–
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 kHz)					
SWITCHING CHARACTERISTICS					
Rise Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	t_r	–	0.7	μs
Storage Time		t_s	–	1.0	μs
Fall Time		t_f	–	0.8	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%. (2) $f_T = |h_{fe}| \cdot f_{test}$

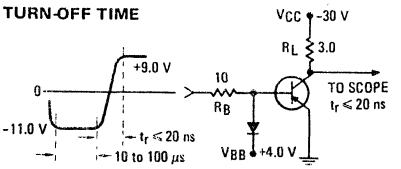
FIGURE 2 – SWITCHING TIME EQUIVALENT TEST CIRCUITS

TURN-ON TIME



DUTY CYCLE ≈ 2.0%

TURN-OFF TIME



DUTY CYCLE ≈ 2.0%

FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN, REVERSE ALL POLARITIES

FIGURE 3 – TURN-ON TIME

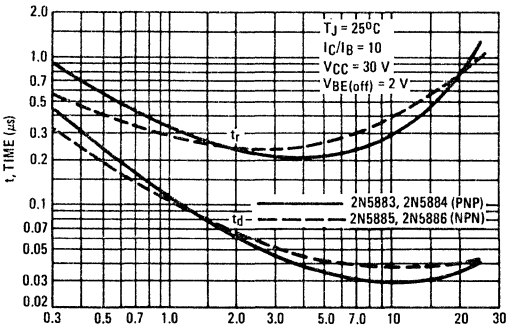


FIGURE 4 – THERMAL RESPONSE

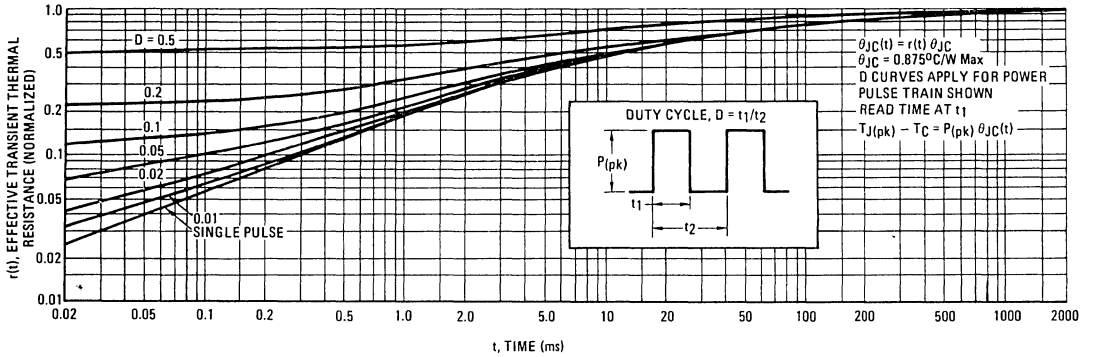
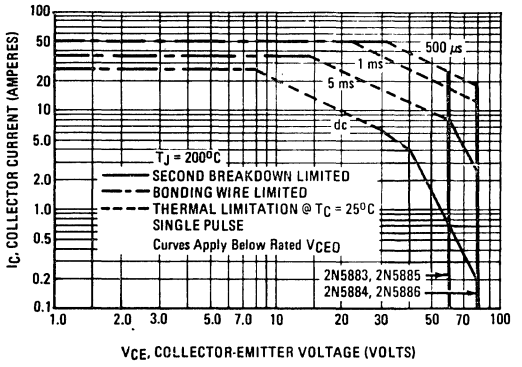


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

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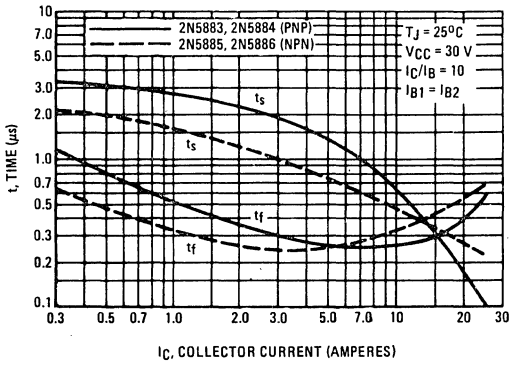
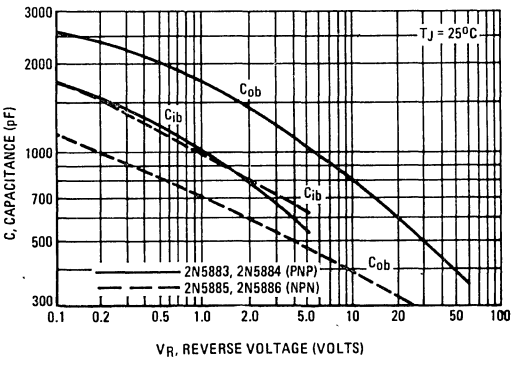


FIGURE 7 – CAPACITANCE



PNP DEVICES
2N5883 and 2N5884

NPN DEVICES
2N5885 and 2N5886

FIGURE 8 – DC CURRENT GAIN

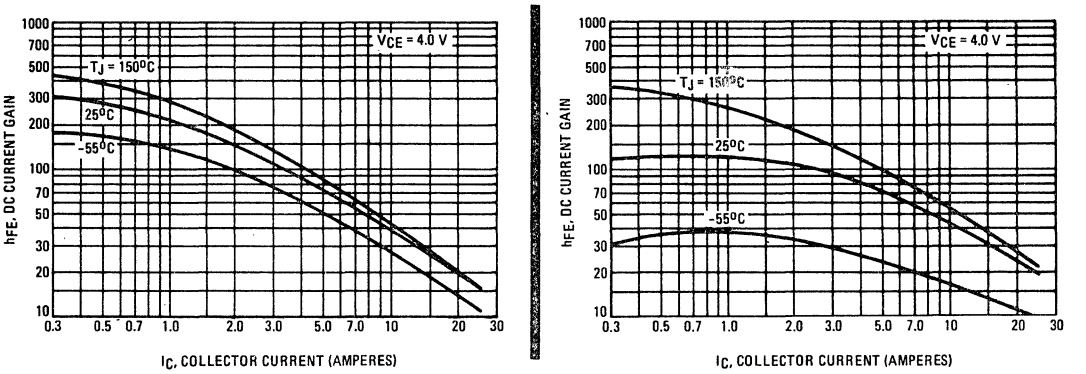


FIGURE 9 – COLLECTOR SATURATION REGION

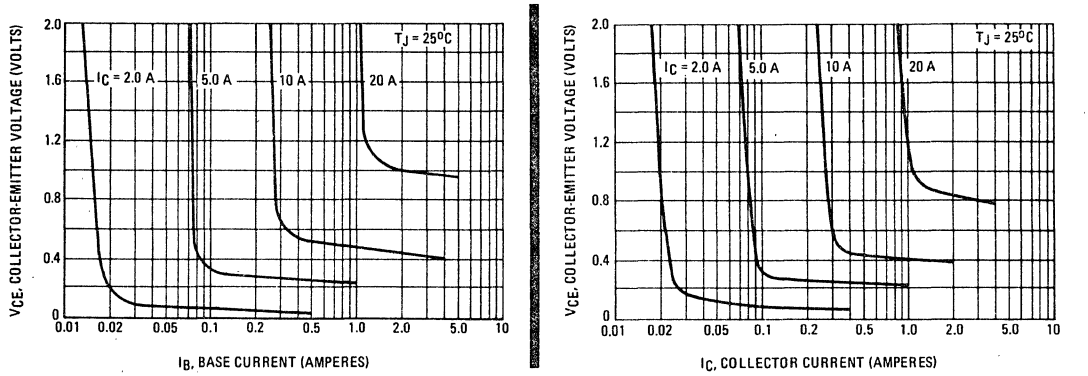
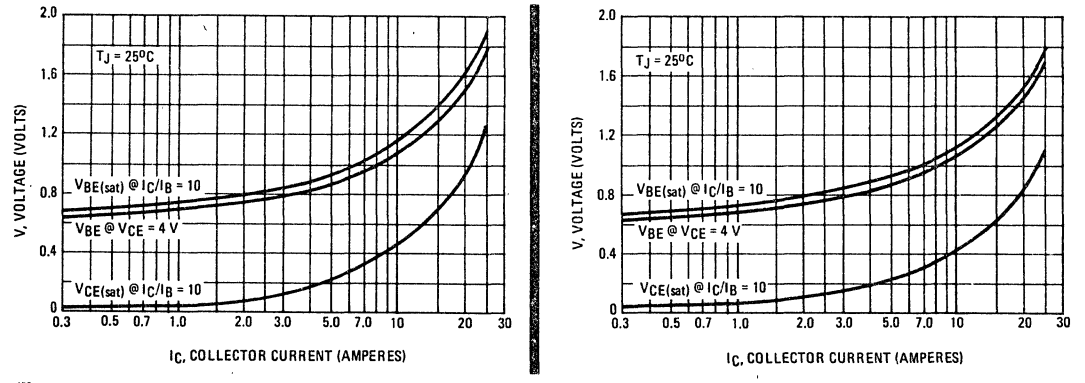


FIGURE 10 – "ON" VOLTAGES



PNP DEVICES
2N5883 and 2N5884

NPN DEVICES
2N5885 and 2N5886

FIGURE 11 – TEMPERATURE COEFFICIENTS

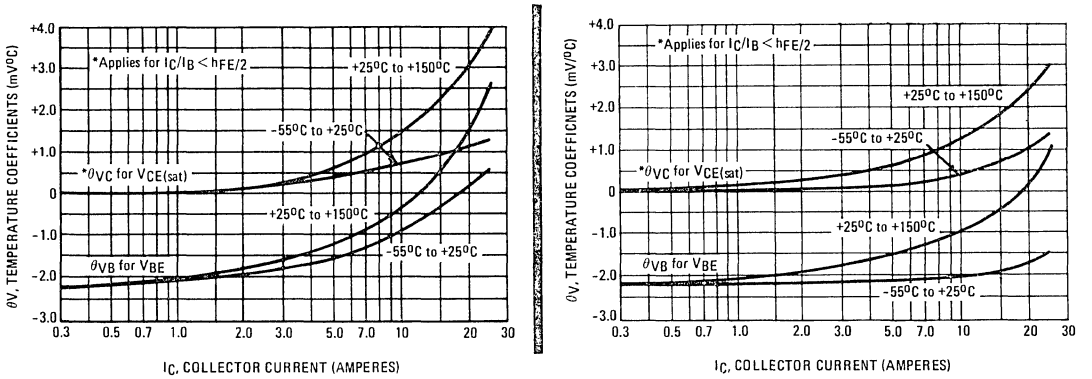


FIGURE 12 – COLLECTOR CUT-OFF REGION

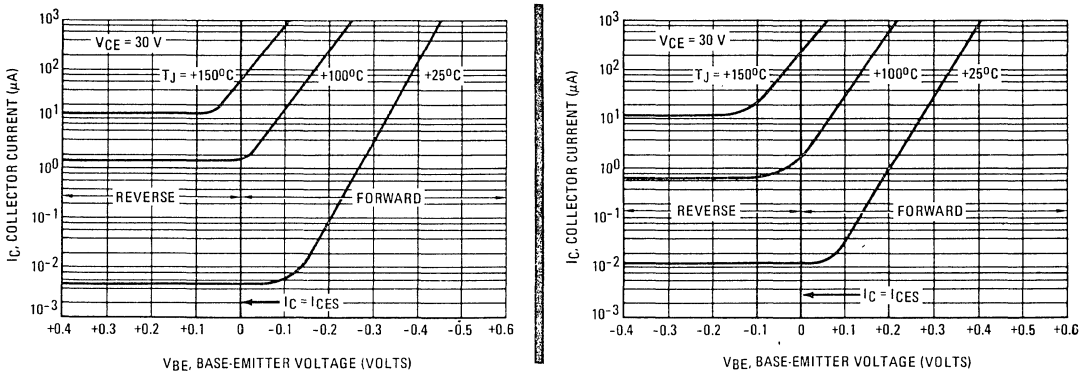
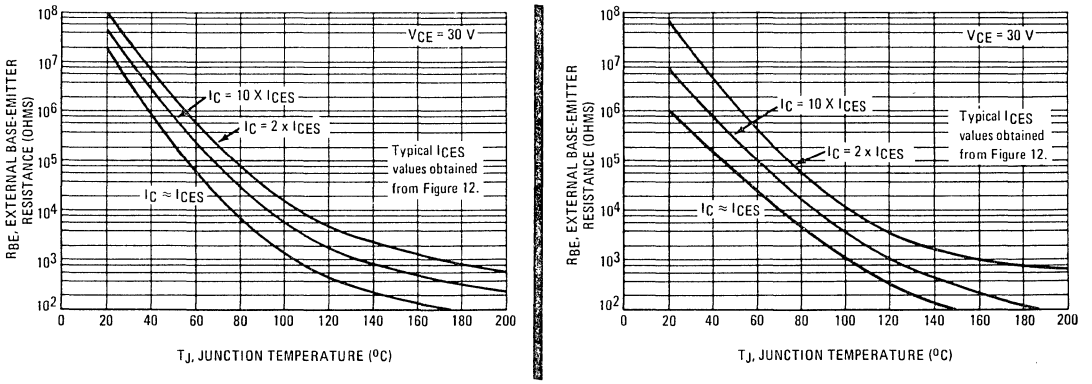


FIGURE 13 – EFFECTS OF EXTERNAL BASE-EMITTER RESISTANCE



2N5974, 2N5975, 2N5976 (SILICON)

4

PNP SILICON PLASTIC POWER TRANSISTORS

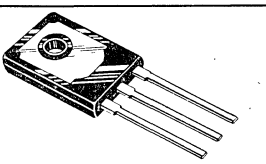
. . . designed for use in general purpose amplifier and switching applications.

- DC Current Gain Specified to 5 Amperes
  h_{FE} = 20-120 @ I_C = 2.5 Adc
  = 7.0 (Min) @ I_C = 5.0 Adc
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 40 Vdc (Min) – 2N5974
  = 60 Vdc (Min) – 2N5975
  = 80 Vdc (Min) – 2N5976
- High Current Gain – Bandwidth Product –
  f_T = 2.0 MHz (Min) @ I_C = 500 mAdc
- Complements to NPN Transistors 2N5977, 2N5978, 2N5979

5 AMPERE POWER TRANSISTORS

PNP SILICON

40-60-80 VOLTS
75 WATTS



*MAXIMUM RATINGS

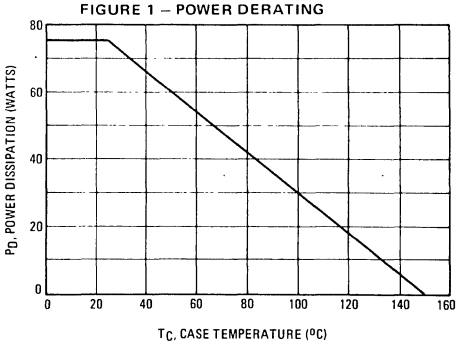
Rating	Symbol	2N5974	2N5975	2N5976	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current - Continuous Peak	I_C	5.0 10			Adc
Base Current	I_B	2.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.60			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			°C

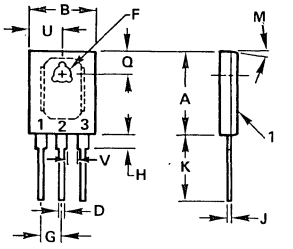
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W

*Indicates JEDEC Registered Data for 2N5974 Series.

FIGURE 1 – POWER DERATING





STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. DIM "D" UNCONTROLLED IN ZONE "H"
2. DIM "F" DIA THRU
3. HEAT SINK CONTACT AREA (BOTTOM)
4. LEADS WITHIN 0.005" RAD OF TRUE POSITION (TP) AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05
TO-127

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

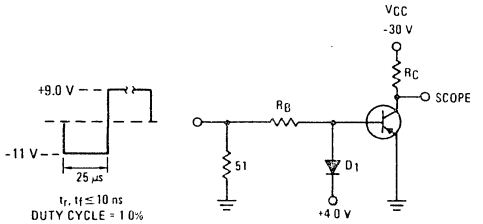
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N5974		40	–	
	2N5975		60	–	
	2N5976		80		
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N5974		–	1.0	
(V_{CE} = 30 Vdc, I_B = 0)	2N5975		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5976		–	1.0	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5974		–	100	μAdc
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5975		–	100	
(V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5976		–	100	
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5974		–	1.0	mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5975		–	1.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5976		–	1.0	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)			–	1.0	
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)			40	–	
(I_C = 2.5 Adc, V_{CE} = 2.0 Vdc)			20	120	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)			7.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 2.5 Adc, I_B = 250 mAdc			–	0.6	
(I_C = 5.0 Adc, I_B = 750 mAdc			–	1.7	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 750 mAdc)			–	2.5	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 2.5 Adc, V_{CE} = 2.0 Vdc)			–	1.4	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (2)		f_T			MHz
(I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)			2.0	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)			–	300	
Small-Signal Current Gain		h_{fe}			–
(I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)			20	–	

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

FIGURE 3 – TURN-ON TIME

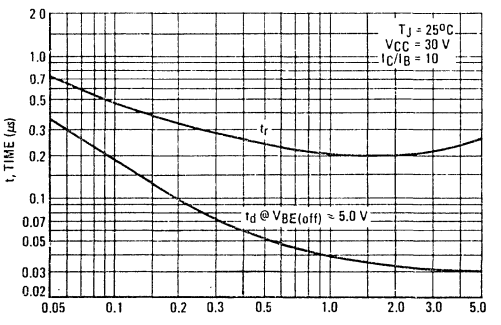


FIGURE 4 – THERMAL RESPONSE

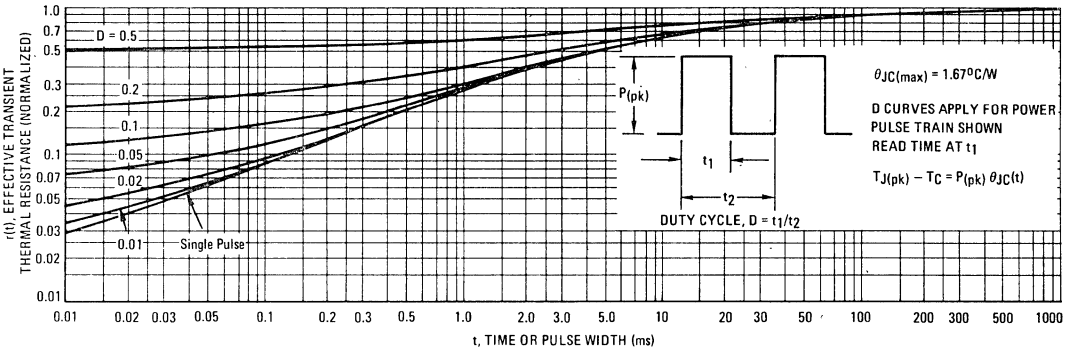
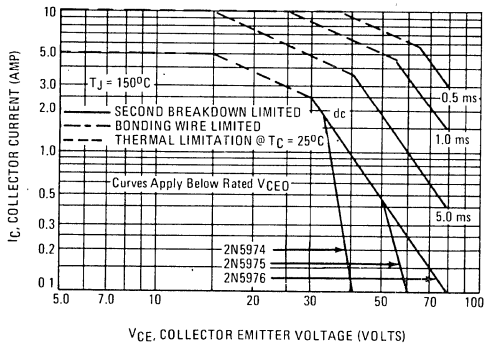


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

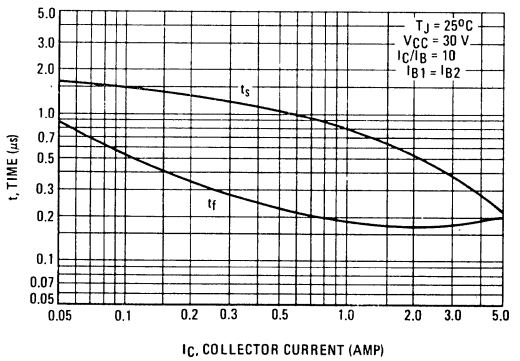


FIGURE 7 – CAPACITANCE

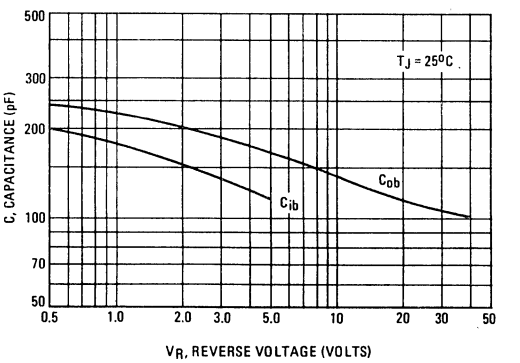


FIGURE 8 – DC CURRENT GAIN

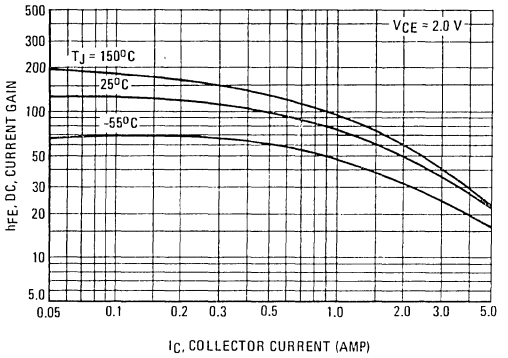


FIGURE 9 – COLLECTOR SATURATION REGION

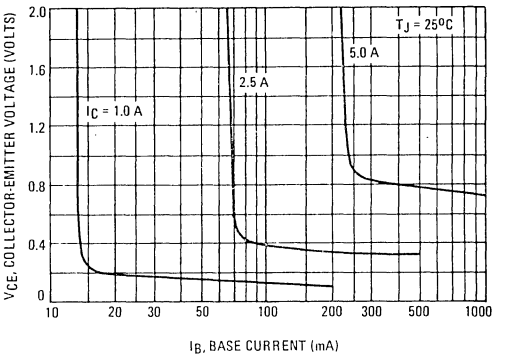


FIGURE 10 – "ON" VOLTAGES

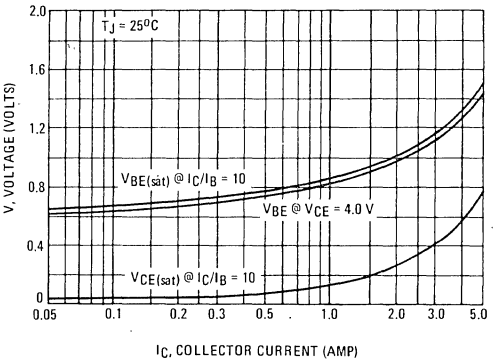


FIGURE 11 – TEMPERATURE COEFFICIENTS

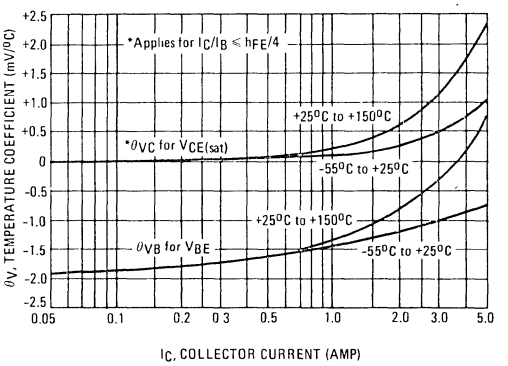


FIGURE 12 – COLLECTOR CUT-OFF REGION

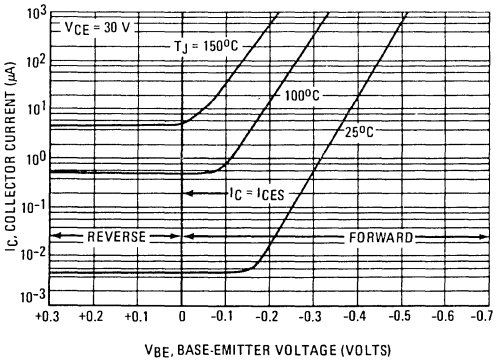
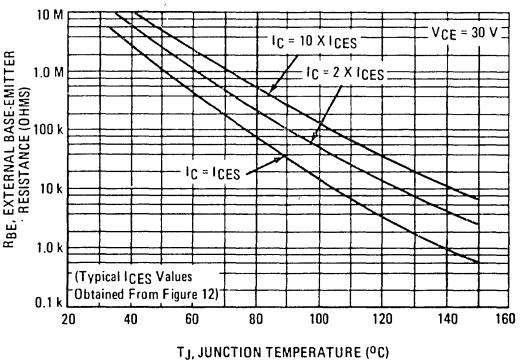


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



2N5977, 2N5978, 2N5979 (SILICON)

4

NPN SILICON PLASTIC POWER TRANSISTORS

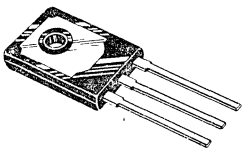
. . . designed for use in general purpose amplifier and switching applications.

- DC Current Gain Specified to 5 Amperes
  h_{FE} = 20-120 @ I_C = 2.5 Adc
  = 7.0 (Min) @ I_C = 5.0 Adc
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 40 Vdc (Min) – 2N5977
  = 60 Vdc (Min) – 2N5978
  = 80 Vdc (Min) – 2N5979
- High Current Gain – Bandwidth Product
  f_T = 2.0 MHz (Min) @ I_C = 500 mAdc
- Complement to PNP Transistors –
  2N5974, 2N5975, 2N5976

5 AMPERE POWER TRANSISTORS

NPN SILICON

40-60-80 VOLTS
75 WATTS



*MAXIMUM RATINGS

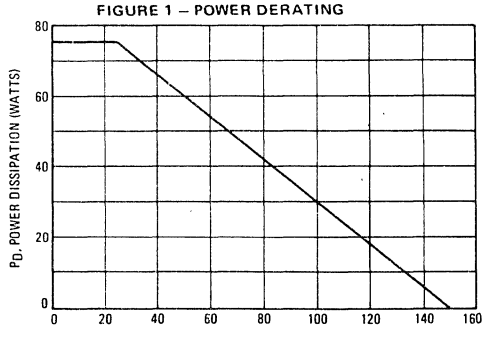
Rating	Symbol	2N5977	2N5978	2N5979	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current - Continuous	I_C	5.0			Adc
Peak		10			
Base Current	I_B	2.0			Adc
Total Power Dissipation @ T_C = 25°C	P_D	75			Watts
Derate above 25°C		0.60			W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150			°C

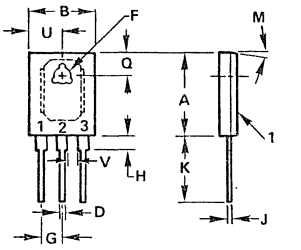
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING





STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. DIM "D" UNCONTROLLED IN ZONE "H"
2. DIM "F" DIA THRU
3. HEAT SINK CONTACT AREA (BOTTOM)
4. LEADS WITHIN 0.005" RAD OF TRUE POSITION (TP) AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
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B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
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J	0.813	0.864	0.032	0.034
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Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05
TO-127

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

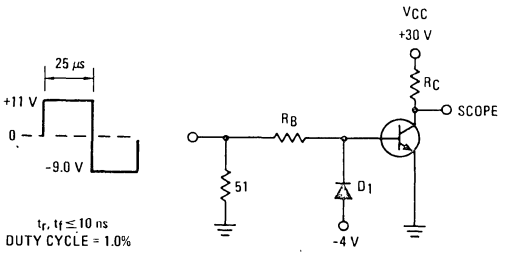
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N5977		40	–	
	2N5978		60	–	
	2N5979		80		
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N5977		–	1.0	
(V_{CE} = 30 Vdc, I_B = 0)	2N5978		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5979		–	1.0	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5977		–	100	μAdc
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5978		–	100	
(V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5979		–	100	
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5977		–	1.0	mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5978		–	1.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5979		–	1.0	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)			–	1.0	
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)			40	–	
(I_C = 2.5 Adc, V_{CE} = 2.0 Vdc)			20	120	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)			7.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 2.5 Adc, I_B = 250 mAdc)			–	0.6	
(I_C = 5.0 Adc, I_B = 750 mAdc)			–	1.7	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 750 mAdc)			–	2.5	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 2.5 Adc, V_{CE} = 2.0 Vdc)			–	1.4	
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2)		f_T			MHz
(I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)			2.0	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)			–	200	
Small-Signal Current Gain		h_{fe}			–
(I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)			20	–	

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE I_B ≈ 100 mA
MSD6100 USED BELOW I_B ≈ 100 mA

FIGURE 3 – TURN-ON TIME

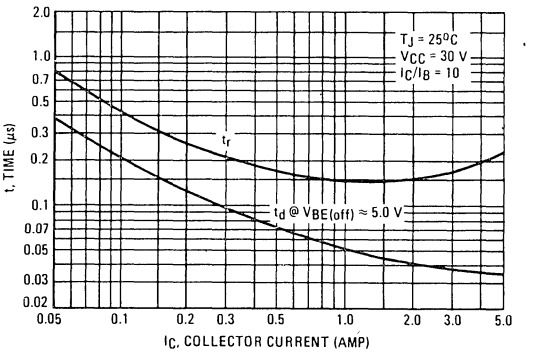


FIGURE 4 – THERMAL RESPONSE

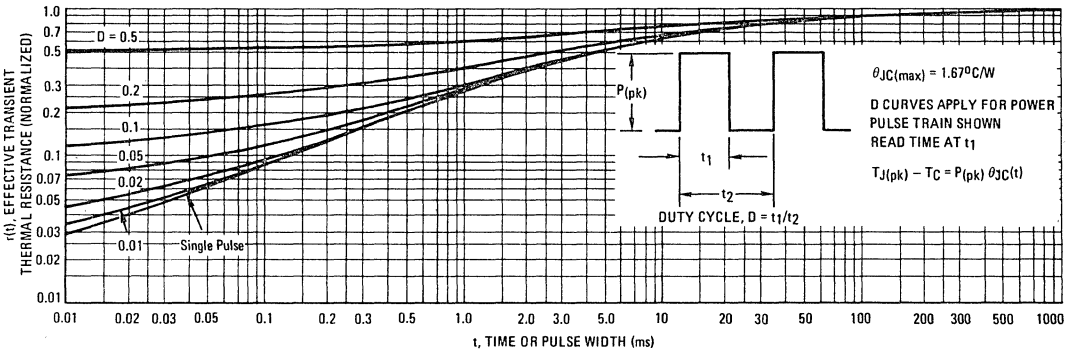
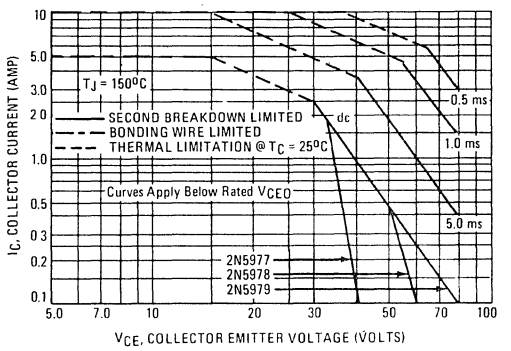


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

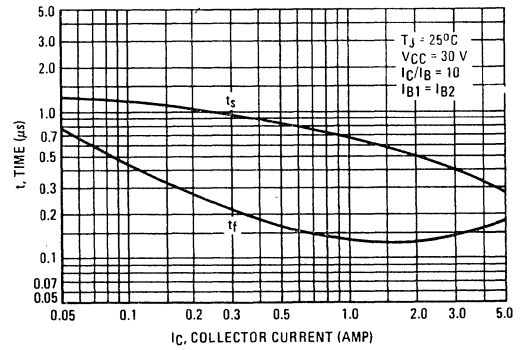


FIGURE 7 – CAPACITANCE

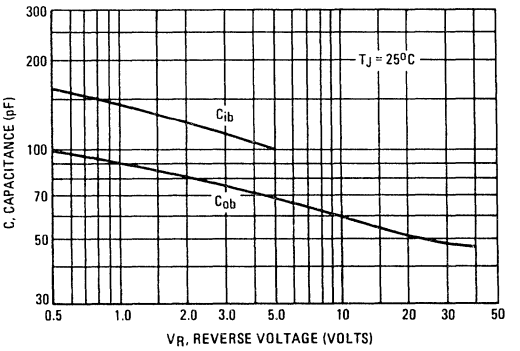


FIGURE 8 – DC CURRENT GAIN

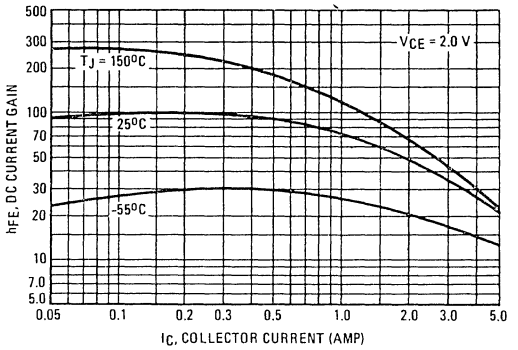


FIGURE 9 – COLLECTOR SATURATION REGION

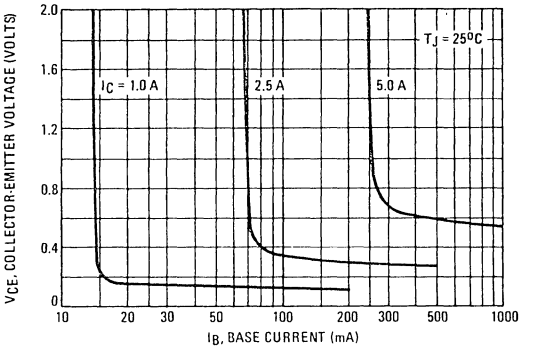


FIGURE 10 – "ON" VOLTAGES

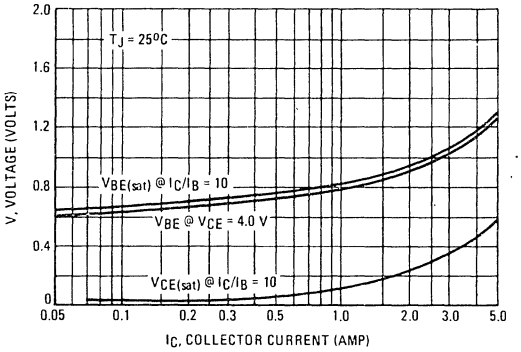


FIGURE 11 – TEMPERATURE COEFFICIENTS

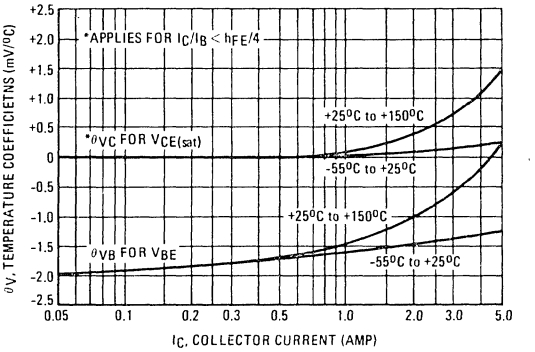


FIGURE 12 – COLLECTOR CUT-OFF REGION

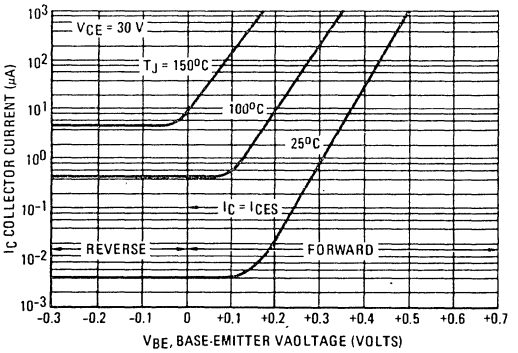
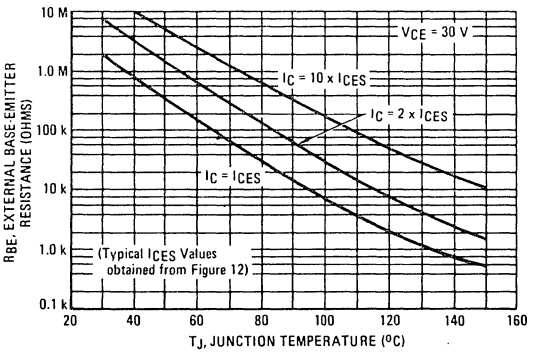


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



2N5986,2N5987,2N5988 PNP (SILICON)
2N5989,2N5990,2N5991 NPN

4

HIGH POWER PLASTIC COMPLEMENTARY SILICON POWER TRANSISTORS

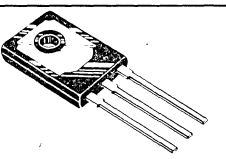
. . . designed for use in general-purpose amplifier and switching circuits.

- Collector-Base Voltage – V_{CBO} = 60 Vdc – 2N5986, 2N5989
  = 80 Vdc – 2N5987, 2N5990
  = 100 Vdc – 2N5988, 2N5991
- Collector-Emitter Voltage – V_{CEO} = 40 Vdc – 2N5986, 2N5989
  = 60 Vdc – 2N5987, 2N5990
  = 80 Vdc – 2N5988, 2N5991
- DC Current Gain –
  h_{FE} = 20-120 @ I_C = 6.0 Adc
  = 7.0 (Min) @ I_C = 12 Adc
- Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.7 Vdc (Max) @ I_C = 6.0 Adc

12 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

40, 60, 80 VOLTS
100 WATTS



*MAXIMUM RATINGS

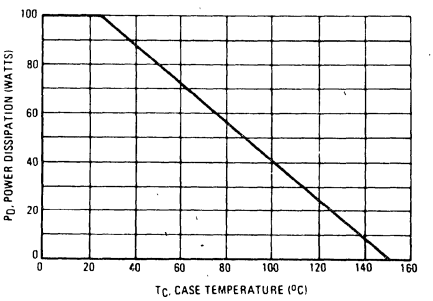
Rating	Symbol	2N5986 2N5989	2N5987 2N5990	2N5988 2N5991	Unit
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous Peak	I_C	12 20			Adc
Base Current	I_B	4.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.8			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			°C

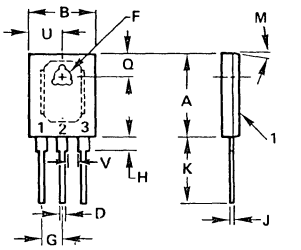
THERMAL CHARACTERISTICS

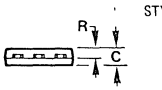
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.25	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING







STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. DIM "D" UNCONTROLLED IN ZONE "H"
2. DIM "F" DIA THRU
3. HEAT SINK CONTACT AREA (BOTTOM)
4. LEADS WITHIN 0.005" RAD OF TRUE POSITION (TP) AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05
TO-127

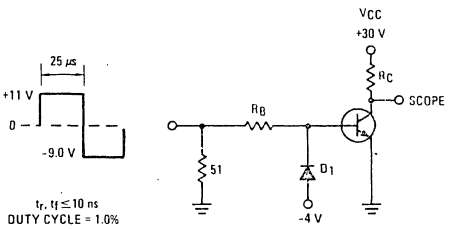
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 0.2 Adc, I_B = 0)	2N5986, 2N5989	$BV_{CEO(sus)}$	40	–	Vdc
	2N5987, 2N5990		60	–	
	2N5988, 2N5991		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N5986, 2N5989		–	2.0	
(V_{CE} = 30 Vdc, I_B = 0)	2N5987, 2N5990		–	2.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5988, 2N5991		–	2.0	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5986, 2N5989		–	200	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5987, 2N5990		–	200	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5988, 2N5991		–	200	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5986, 2N5989		–	2.0	mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5987, 2N5990		–	2.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N5988, 2N5991		–	2.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)			40	–	
(I_C = 6.0 Adc, V_{CE} = 2.0 Vdc)			20	120	
(I_C = 12 Adc, V_{CE} = 2.0 Vdc)			7.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 6.0 Adc, I_B = 0.6 Adc)			–	0.7	
(I_C = 12 Adc, I_B = 1.8 Adc)			–	1.7	
Base-Emitter Saturation Voltage (I_C = 12 Adc, I_B = 1.8 Adc)		$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.4	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	2.0	–	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N5986 thru 2N5988		–	500	
	2N5989 thru 2N5991		–	300	
Small-Signal Current Gain (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–

*Indicates JEDEC Registered Data.

(1) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE I_B ≈100 mA
MSD6100 USED BELOW I_B ≈100 mA

For PNP test circuit reverse diode and voltage polarities.

FIGURE 3 – TURN-ON TIME

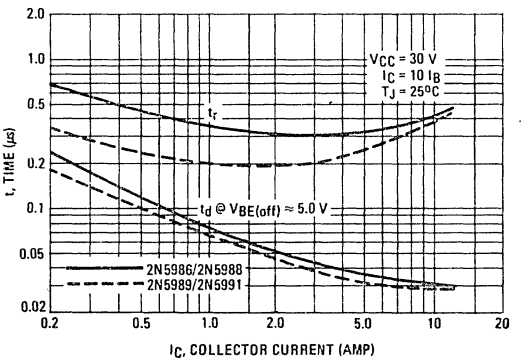


FIGURE 4 – THERMAL RESPONSE

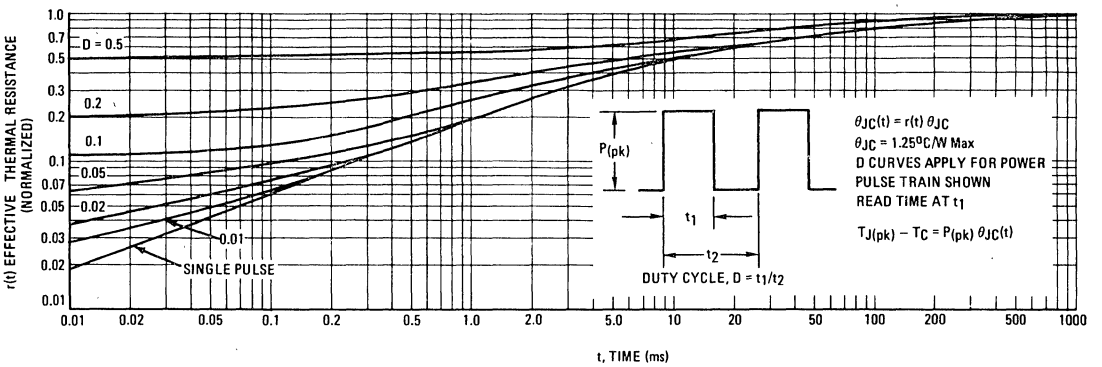
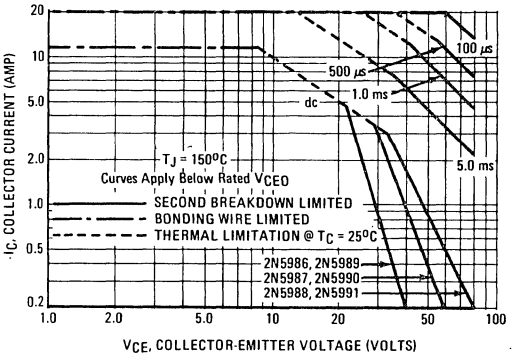


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^oC$ $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

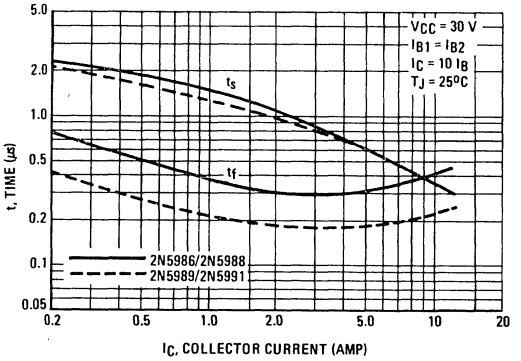
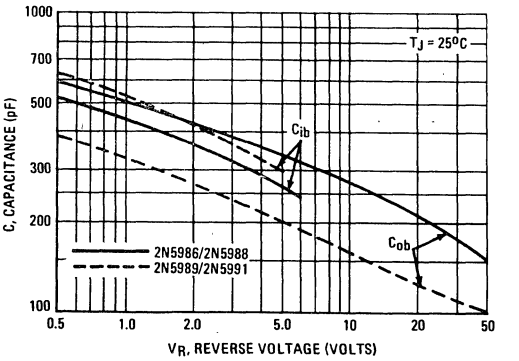


FIGURE 7 – CAPACITANCE



PNP
2N5986 thru 2N5988

NPN
2N5989 thru 2N5991

FIGURE 8 – DC CURRENT GAIN

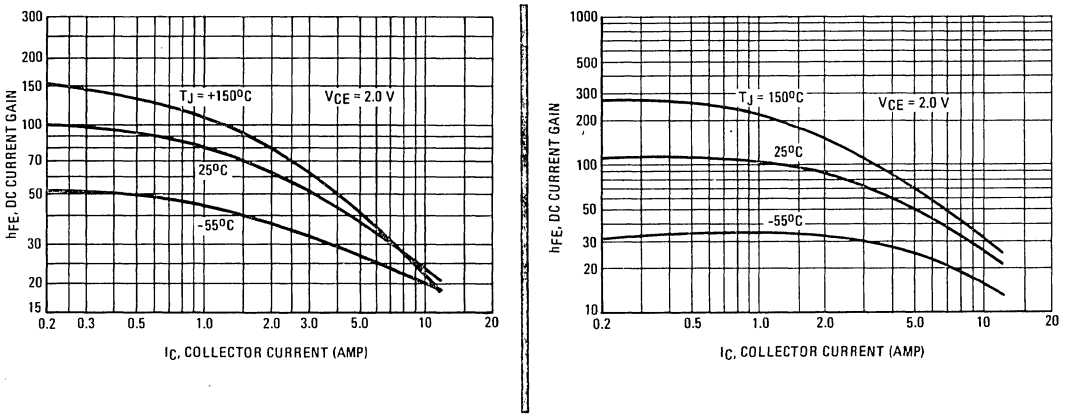


FIGURE 9 – COLLECTOR SATURATION REGION

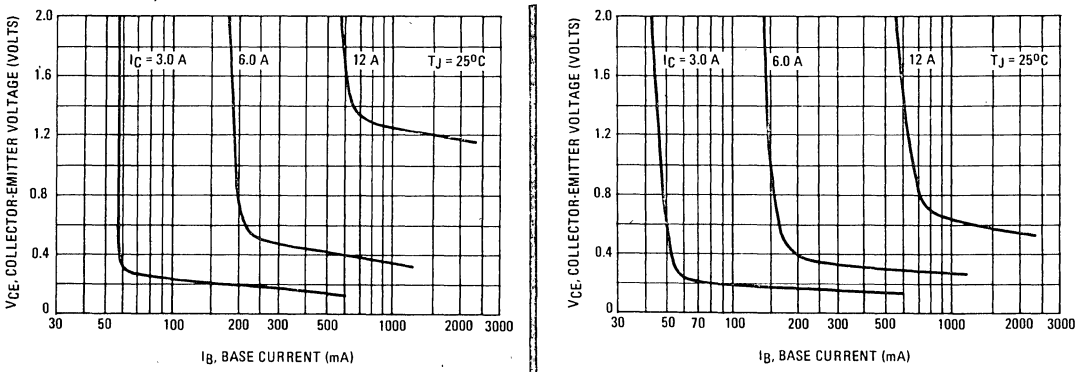
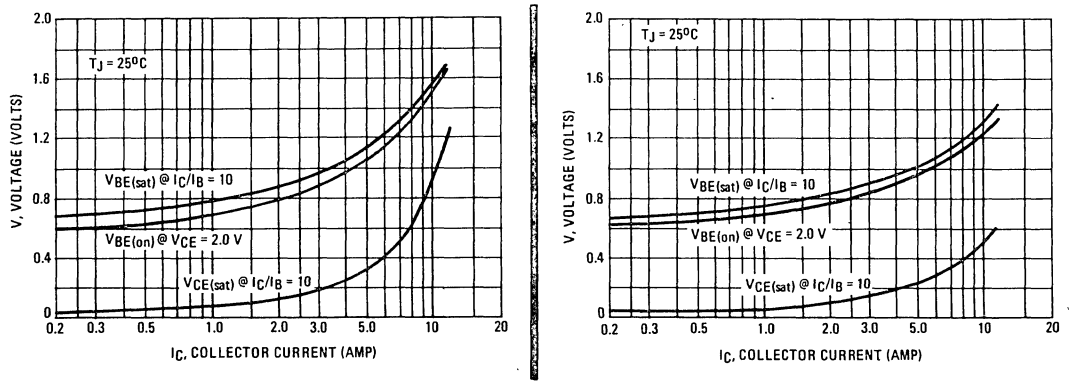


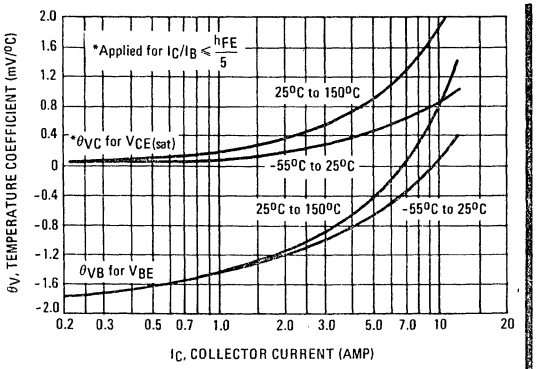
FIGURE 10 – "ON" VOLTAGES



PNP
2N5986 thru 2N5988

NPN
2N5989 thru 2N5991

FIGURE 11 – TEMPERATURE COEFFICIENTS



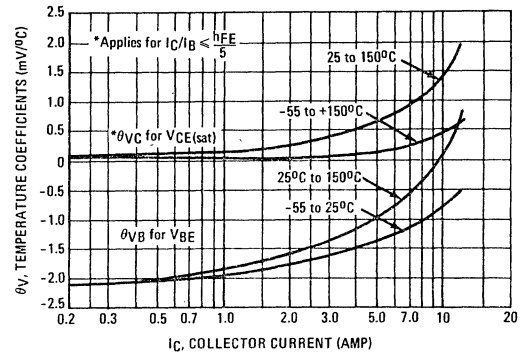
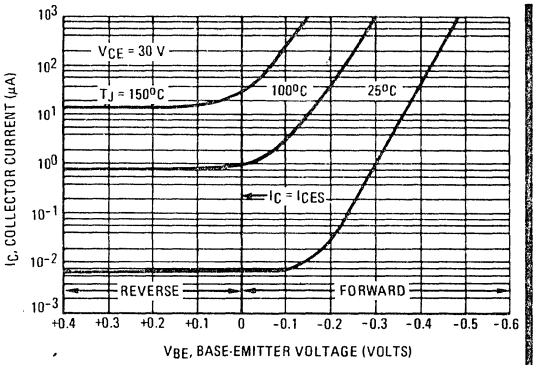


FIGURE 12 – COLLECTOR CUTOFF REGION



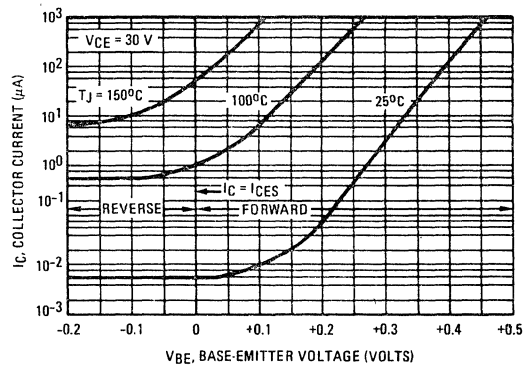
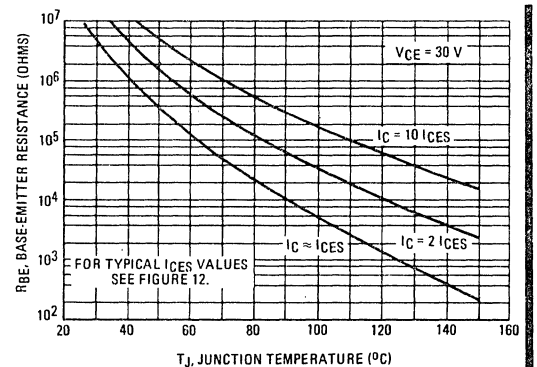
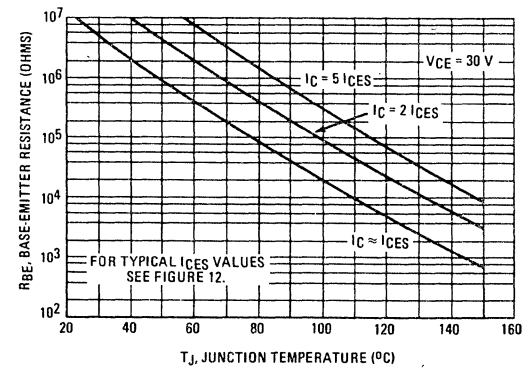


FIGURE 13 – EFFECTS OF EXTERNAL BASE-EMITTER RESISTANCE





2N6034, 2N6035, 2N6036 PNP (SILICON)
2N6037, 2N6038, 2N6039 NPN

PLASTIC DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

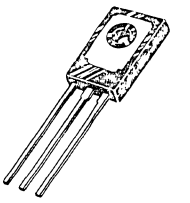
. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain –
  h_{FE} = 2000 (Typ) @ I_C = 2.0 Adc
- Collector-Emitter Sustaining Voltage – @ 100 mAdc
  $V_{CEO(sus)}$ = 40 Vdc (Min) – 2N6034, 2N6037
  = 60 Vdc (Min) – 2N6035, 2N6038
  = 80 Vdc (Min) – 2N6036, 2N6039
- Forward Biased Second Breakdown Current Capability
  $I_{S/b}$ = 1.5 Adc @ 25 Vdc
- Monolithic Construction with Built-In Base-Emitter Resistors to Limit Leakage Multiplication
- Space-Saving High Performance-to-Cost Ratio
  TO-126 Plastic Package

DARLINGTON 4-AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

40, 60, 80 VOLTS
40 WATTS



*MAXIMUM RATINGS

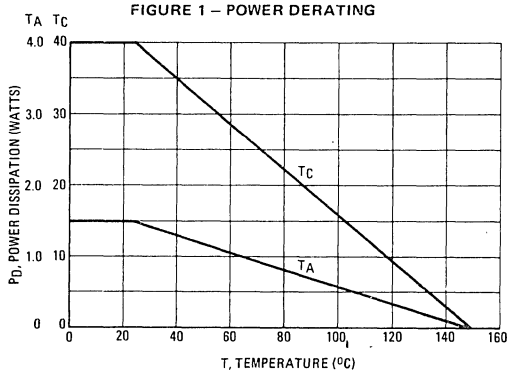
Rating	Symbol	2N6034 2N6037	2N6035 2N6038	2N6036 2N6039	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous	I_C	4.0			Adc
Peak		8.0			
Base Current	I_B	100			mAdc
Total Power Dissipation @ T_C = 25°C	P_D	40			Watts
Derate above 25°C		0.32			W/°C
Total Power Dissipation @ T_A = 25°C	P_D	1.5			Watts
Derate above 25°C		0.012			W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	−65 to +150			°C

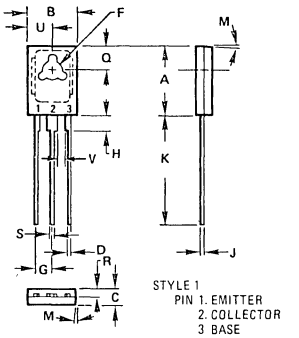
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.3	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING





STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3 BASE

NOTES
1. MT = MAIN TERMINAL
2. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. TO DIM. "A" & "B" AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

4

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	2N6034, 2N6037	$V_{CEO(sus)}$	40	–	Vdc
	2N6035, 2N6038		60	–	
	2N6036, 2N6039		80	–	
Collector-Cutoff Current		I_{CEO}			μA
(V_{CE} = 40 Vdc, I_B = 0)	2N6034, 2N6037		–	100	
(V_{CE} = 60 Vdc, I_B = 0)	2N6035, 2N6038		–	100	
(V_{CE} = 80 Vdc, I_B = 0)	2N6036, 2N6039		–	100	
Collector Cutoff Current		I_{CEX}			μA
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6034, 2N6037		–	100	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6035, 2N6038		–	100	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6036, 2N6039		–	100	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc T_C = 125°C)	2N6034, 2N6037		–	500	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc T_C = 125°C)	2N6035, 2N6038		–	500	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc T_C = 125°C)	2N6036, 2N6039		–	500	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N6034, 2N6037		–	0.5	
(V_{CB} = 60 Vdc, I_E = 0)	2N6035, 2N6038		–	0.5	
(V_{CB} = 80 Vdc, I_E = 0)	2N6036, 2N6039		–	0.5	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 3.0 Vdc)			500	–	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)			750	15,000	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			100	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 8.0 mAdc)			–	2.0	
(I_C = 4.0 Adc, I_B = 40 mAdc)			–	3.0	
Base-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 40 mAdc)		$V_{BE(sat)}$	–	4.0	Vdc
Base-Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current-Gain (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	1.0	–	–
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E =0, f = 0.1 MHz)	2N6034, 2N6035, 2N6036		–	200	
	2N6037, 2N6038, 2N6039		–	100	

*Indicates JEDEC Registered Data.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

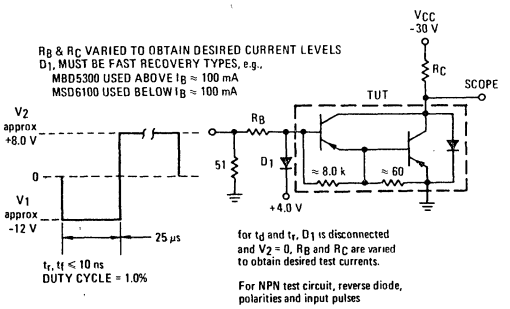


FIGURE 3 – SWITCHING TIMES

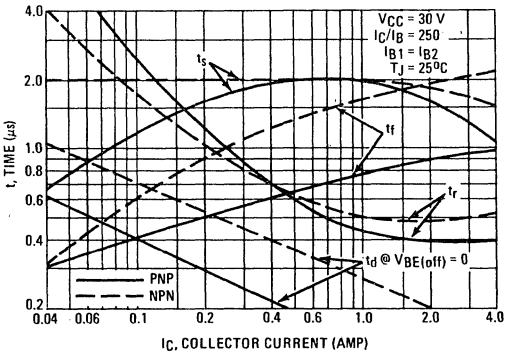
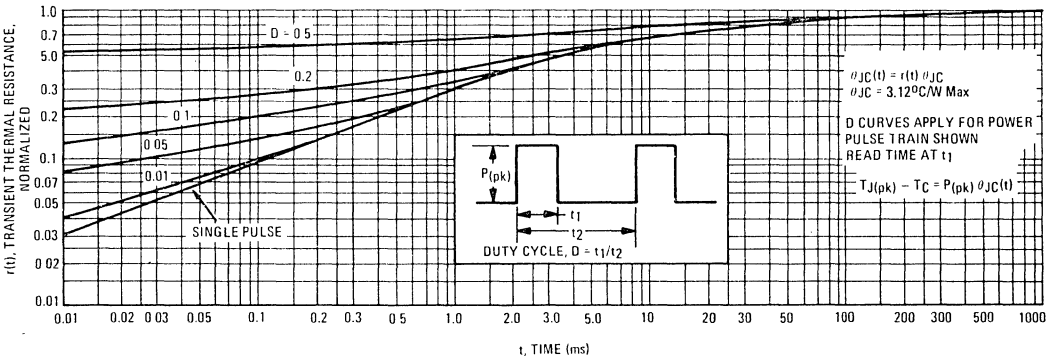


FIGURE 4 – THERMAL RESPONSE



ACTIVE-REGION SAFE-OPERATING AREA

FIGURE 5 – 2N6034, 2N6035, 2N6036

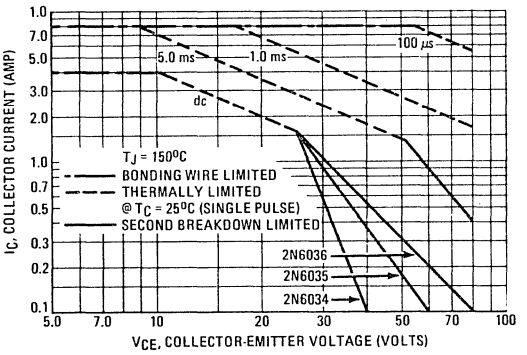
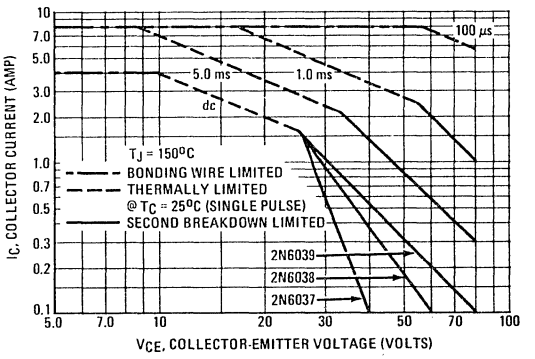


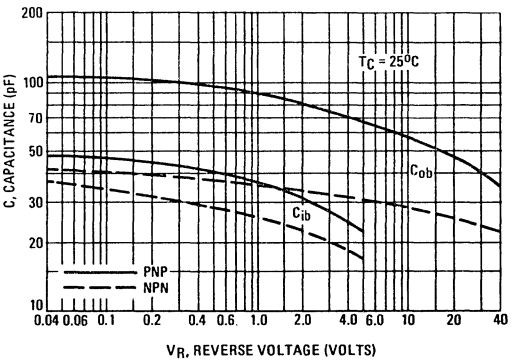
FIGURE 6 – 2N6037 2N6038, 2N6039



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 7 – CAPACITANCE



4

PNP
2N6034, 2N6035, 2N6036

NPN
2N6037, 2N6038, 2N6039

FIGURE 8 – DC CURRENT GAIN

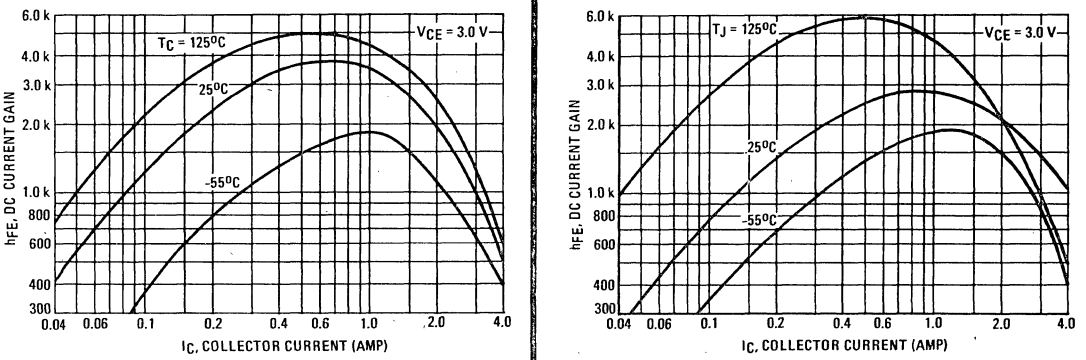


FIGURE 9 – COLLECTOR SATURATION REGION

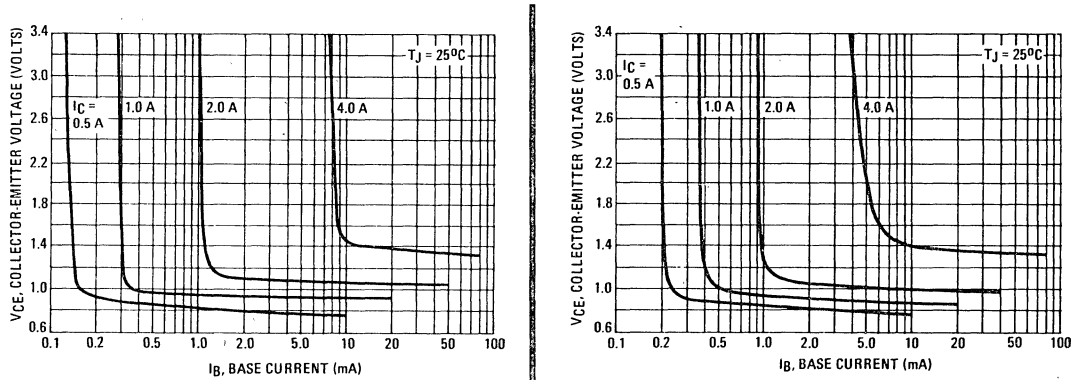
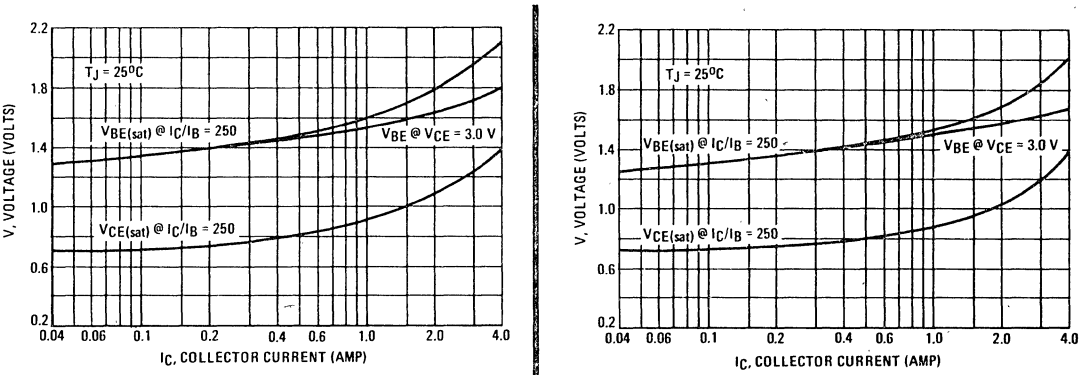


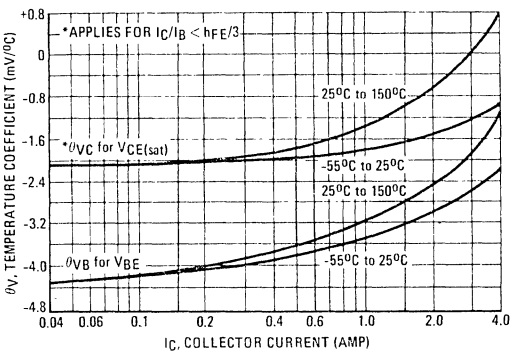
FIGURE 10 – "ON" VOLTAGES



PNP
2N6034, 2N6035, 2N6036

NPN
2N6037, 2N6038, 2N6039

FIGURE 11 -- TEMPERATURE COEFFICIENCTS



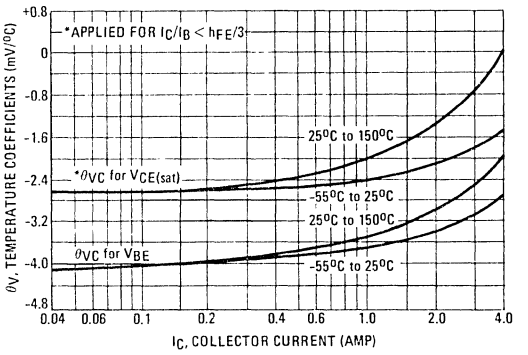
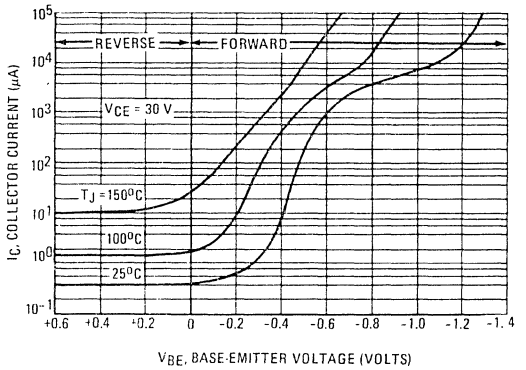


FIGURE 12 – COLLECTOR CUT-OFF REGION



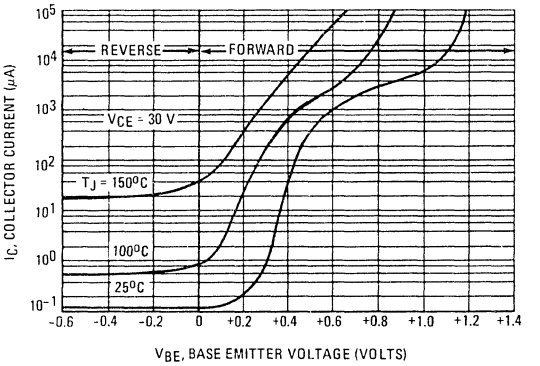
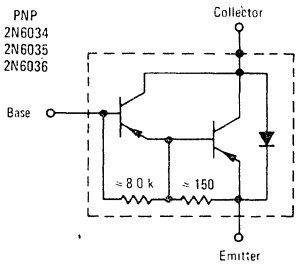
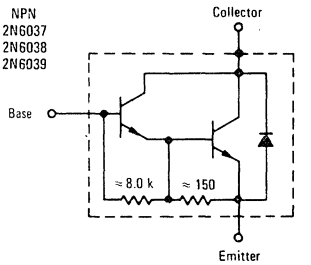


FIGURE 13 – DARLINGTON SCHEMATIC





2N6040 thru 2N6042 PNP (SILICON)
2N6043 thru 2N6045 NPN
MJE6040 thru MJE6042 PNP
MJE6043 thru MJE6045 NPN

PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

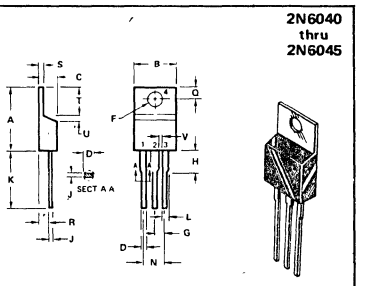
. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain – h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage – @ 100 mAdc (1)
  $V_{CEO(sus)}$ = 60 Vdc (Min) – 2N6040, 2N6043
  = 80 Vdc (Min) – 2N6041, 2N6044
  = 100 Vdc (Min) – 2N6042, 2N6045
- Low Collector-Emitter Saturation Voltage – (1)
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 4.0 Adc – 2N6040,41,2N6043,44
  = 2.0 Vdc (Max) @ I_C = 3.0 Adc – 2N6042, 2N6045
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

(1) Applies to corresponding in-house part numbers also.

DARLINGTON 8 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60-80-100 VOLTS
75 WATTS

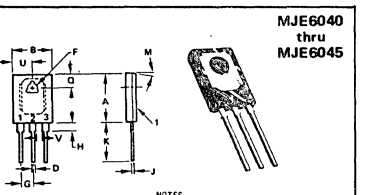


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	

STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

NOTE
1 DIM L & H APPLIES TO ALL LEADS

CASE 221A-02
TO-220AB



NOTES
1 DIM "D" UNCONTROLLED IN ZONE "H"
2 DIM "F" DIA THRU
3 HEAT SINK CONTACT AREA (BOTTOM)
4 LEADS WITHIN 0.005" RAD OF TRUE POSITION (TP) AT MAXIMUM MATERIAL CONDITION

STYLE 2
PIN 1 EMITTER
2 COLLECTOR
3 BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.32 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	90° TYP		90° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05
TO-127

*MAXIMUM RATINGS

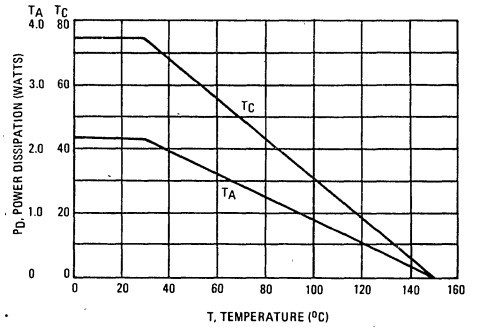
Rating	Symbol	2N6040 2N6043 MJE6040 MJE6043	2N6041 2N6044 MJE6041 MJE6044	2N6042 2N6045 MJE6042 MJE6045	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous	I_C	8.0			Adc
Peak		16			
Base Current	I_B	120			mAdc
Total Power Dissipation @ T_C = 25°C	P_D	75			Watts
Derate above 25°C		0.60			W/°C
Total Power Dissipation @ T_A = 25°C	P_D	2.2			Watts
Derate above 25°C		0.0175			W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	57	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING



2N6040 thru 2N6042 PNP
2N6043 thru 2N6045 NPN
MJE6040 thru MJE6042 PNP
MJE6043 thru MJE6045 NPN

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	2N6040, 2N6043, MJE6040, MJE6043	$V_{CEO(sus)}$	60	–	Vdc
	2N6041, 2N6044, MJE6041, MJE6044		80	–	
	2N6042, 2N6045, MJE6042, MJE6045		100	–	
Collector Cutoff Current		I_{CEO}			μA
(V_{CE} = 60 Vdc, I_B = 0)	2N6040, 2N6043, MJE6040, MJE6043		–	20	
(V_{CE} = 80 Vdc, I_B = 0)	2N6041, 2N6044, MJE6041, MJE6044		–	20	
(V_{CE} = 100 Vdc, I_B = 0)	2N6042, 2N6045, MJE6042, MJE6045		–	20	
Collector Cutoff Current		I_{CEX}			μA
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6040, 2N6043, MJE6040, MJE6043		–	20	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6041, 2N6044, MJE6041, MJE6044		–	20	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6042, 2N6045, MJE6042, MJE6045		–	20	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6040, 2N6043, MJE6040, MJE6043		–	200	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6041, 2N6044, MJE6041, MJE6044		–	200	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6042, 2N6045, MJE6042, MJE6045		–	200	
Collector Cutoff Current		I_{CBO}			μA
(V_{CB} = 60 Vdc, I_E = 0)	2N6040, 2N6043, MJE6040, MJE6043		–	20	
(V_{CB} = 80 Vdc, I_E = 0)	2N6041, 2N6044, MJE6041, MJE6044		–	20	
(V_{CB} = 100 Vdc, I_E = 0)	2N6042, 2N6045, MJE6042, MJE6045		–	20	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	2N6040,41, 2N6043,44, MJE6040,41, MJE6043,44		1000	10,000	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	2N6042, 2N6045, MJE6042, MJE6045		1000	10,000	
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)	All Types		100	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 4.0 Adc, I_B = 16 mAdc)	2N6040,41,2N6043,44,MJE6040,41,MJE6043,44		–	2.0	
(I_C = 3.0 Adc, I_B = 12 mAdc)	2N6042,2N6045,MJE6042,MJE6045		–	2.0	
(I_C = 8.0 Adc, I_B = 80 mAdc)	All Types		–	4.0	
Base-Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 80 mAdc)		$V_{BE(sat)}$	–	4.5	Vdc
Base-Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6040/2N6042, MJE6040/MJE6042	C_{ob}	–	300	pF
	2N6043/2N6045, MJE6043/MJE6045		–	200	
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	300	–	–

*Indicates JEDEC Registered Data

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

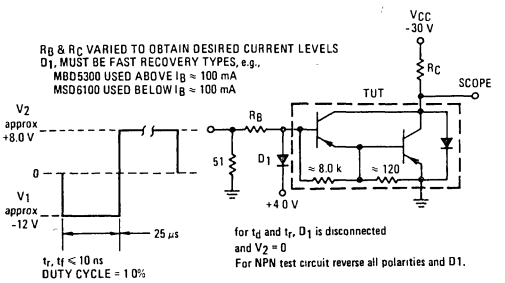


FIGURE 3 – SWITCHING TIMES

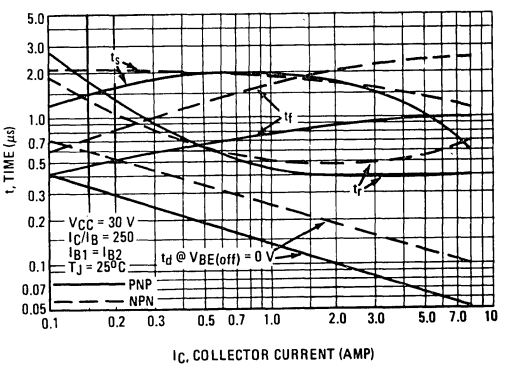


FIGURE 4 – THERMAL RESPONSE

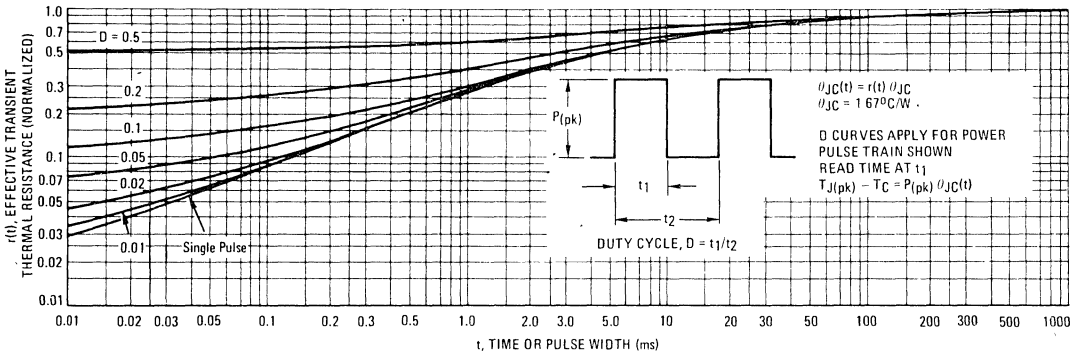
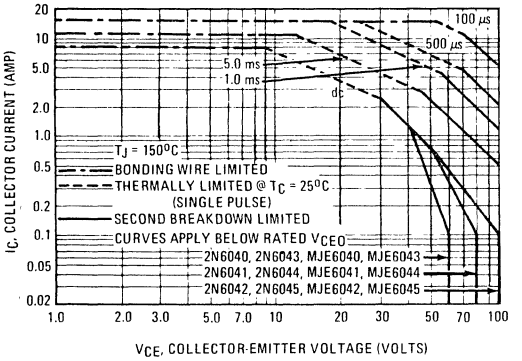


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

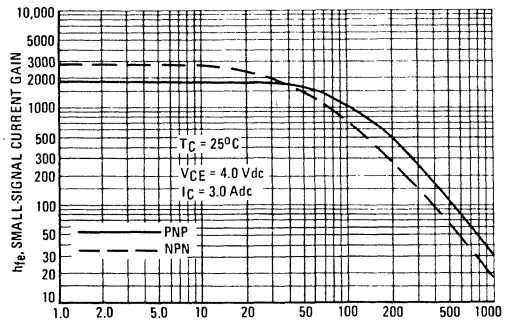
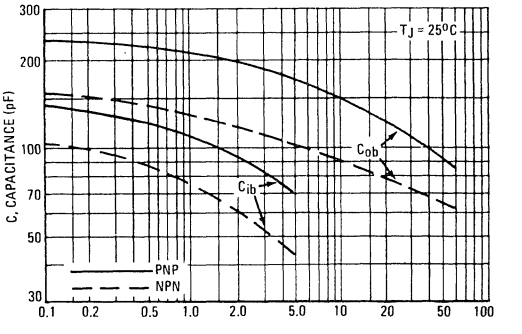


FIGURE 7 – CAPACITANCE



PNP
2N6040, 2N6041, 2N6042
MJE6040, MJE6041, MJE6042

NPN
2N6043, 2N6044, 2N6045
MJE6043, MJE6044, MJE6045

FIGURE 8 – DC CURRENT GAIN

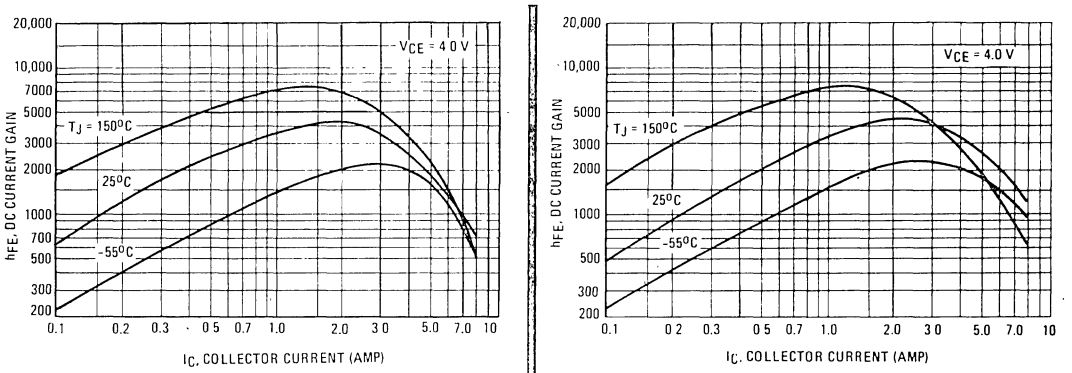


FIGURE 9 – COLLECTOR SATURATION REGION

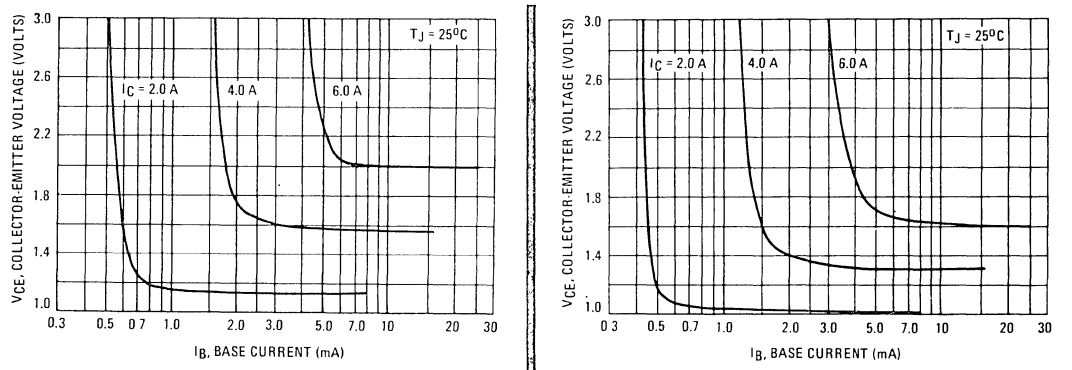
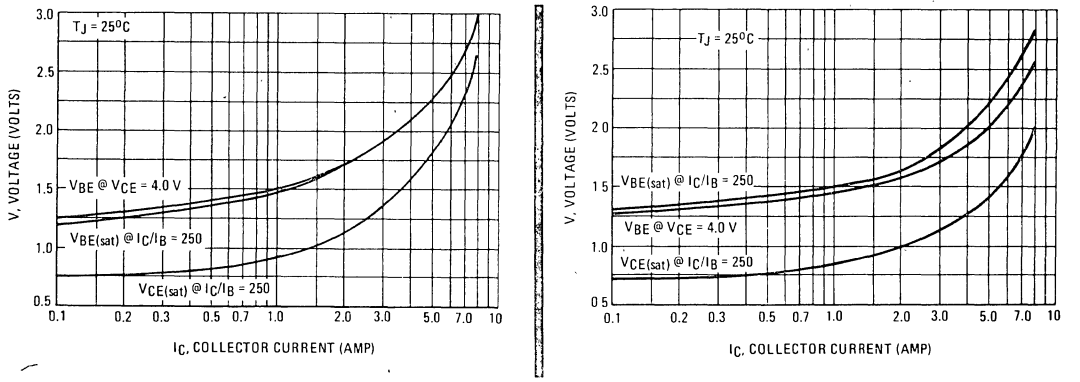


FIGURE 10 – "ON" VOLTAGES

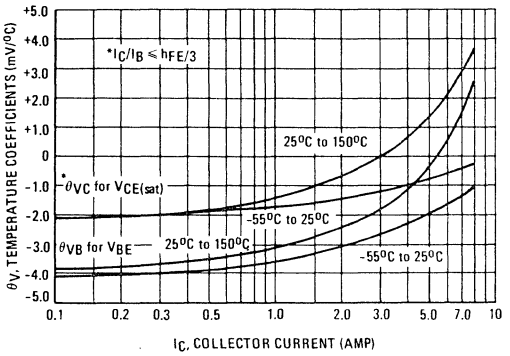


4

PNP
2N6040, 2N6041, 2N6042
MJE6040, MJE6041, MJE6042

NPN
2N6043, 2N6044, 2N6045
MJE6043, MJE6044, MJE6045

FIGURE 11 – TEMPERATURE COEFFICIENTS



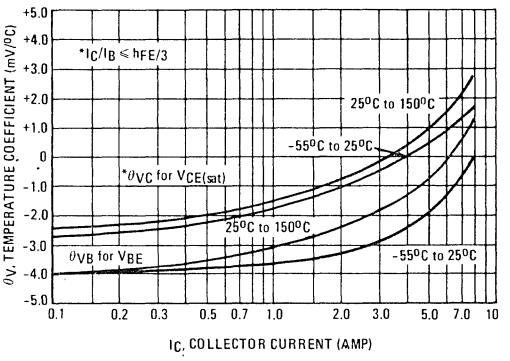
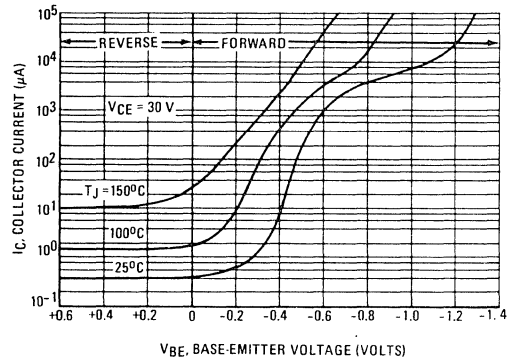


FIGURE 12 – COLLECTOR CUT-OFF REGION



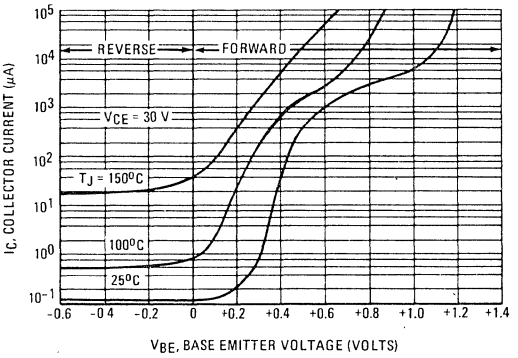
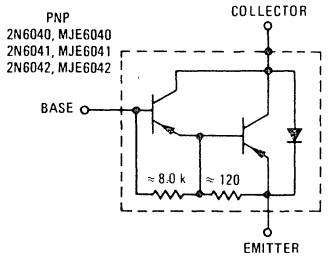
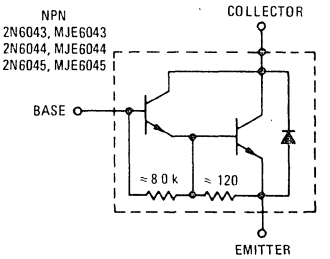


FIGURE 13 – DARLINGTON SCHEMATIC



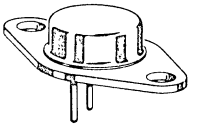


MEDIUM-POWER PNP SILICON TRANSISTOR

. . . designed for general-purpose switching and amplifier applications

- Excellent Safe Operating Area
- DC Current Gain Specified to 4.0 Amperes
- Complement to NPN Type 2N3054A

4 AMPERE
POWER TRANSISTOR
PNP SILICON
55 VOLTS
75 WATTS



*MAXIMUM RATINGS

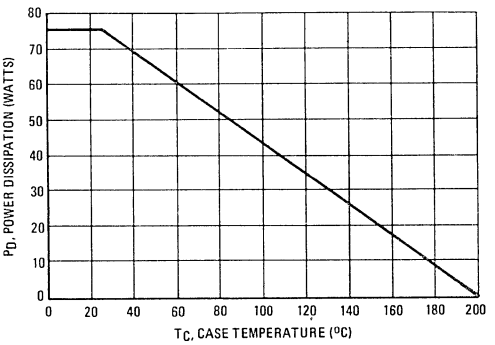
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	55	Vdc
Collector-Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	60	Vdc
Collector-Base Voltage	V_{CB}	90	Vdc
Emitter-Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous Peak	I_C	4.0 10	Adc
Base Current	I_B	2.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°	P_D	75 0.43	Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +200	°C

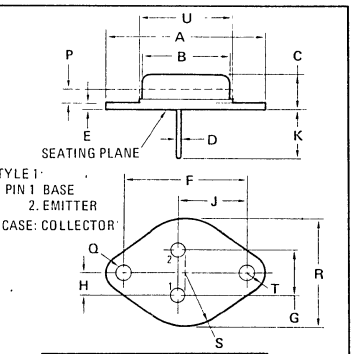
*Indicates JEDEC Registered Data

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.33	°C/W

FIGURE 1 — POWER-TEMPERATURE DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

4

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	55	–	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, R_{BE} = 100 Ω	$V_{CER(sus)}$	60	–	Vdc
Collector Cuttoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	500	μAdc
Collector Cutoff Current (V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	1.0 6.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 500 mAdc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	25 6.0	100	– –
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 4.0 Adc, I_B = 800 mAdc)	$V_{CE(sat)}$	– –	0.5 2.0	Vdc
Base-Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10 Vdc)	f_T	3.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	200	pF
Small-Signal Current Gain (I_C = 100 mAdc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	25	180	

*Indicates JEDEC Registered Data

(1) Pulse test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

FIGURE 2 – SWITCHING TIME EQUIVALENT TEST CIRCUIT

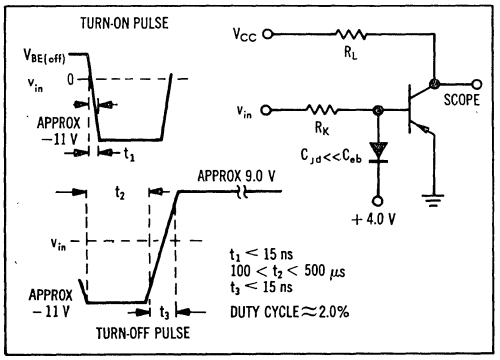


FIGURE 3 – TURN-ON TIME

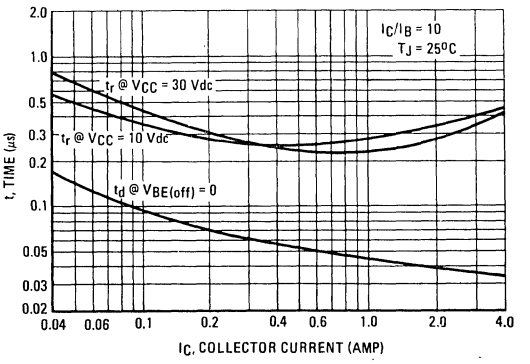


FIGURE 4 – THERMAL RESPONSE

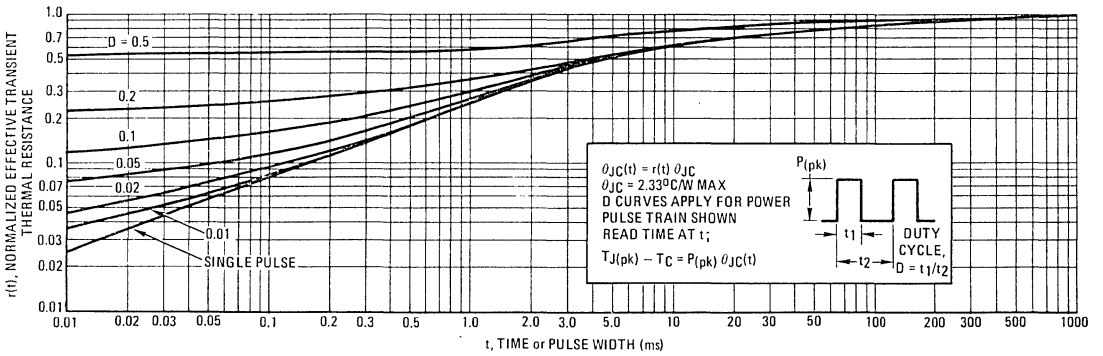
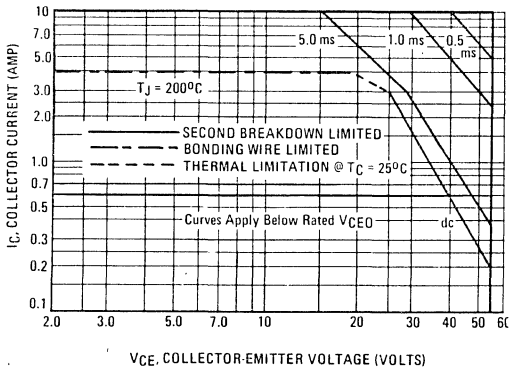


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

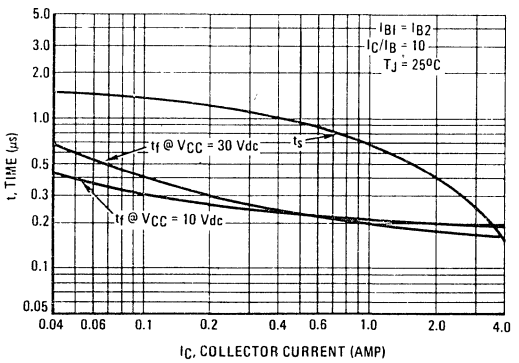


FIGURE 7 – CAPACITANCE

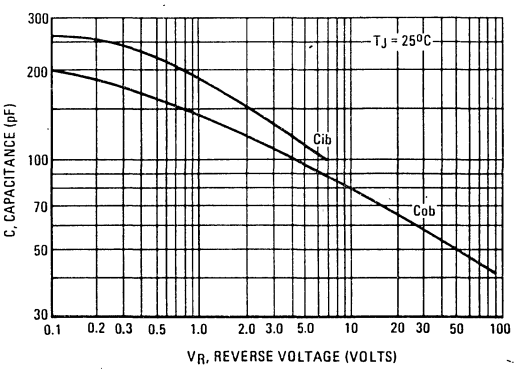


FIGURE 8 – DC CURRENT GAIN

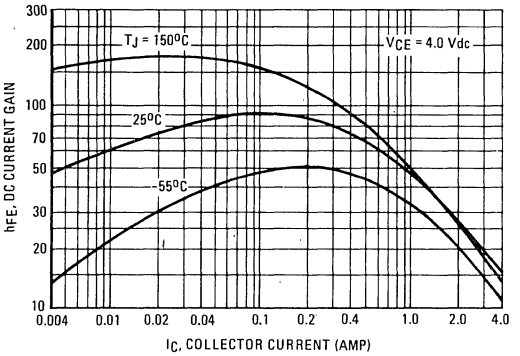


FIGURE 9 – COLLECTOR SATURATION REGION

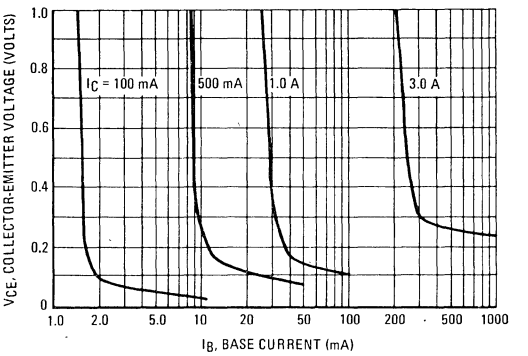


FIGURE 10 – TEMPERATURE COEFFICIENT

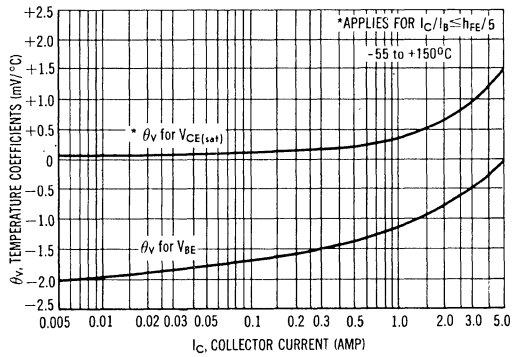


FIGURE 11 – "ON" VOLTAGES

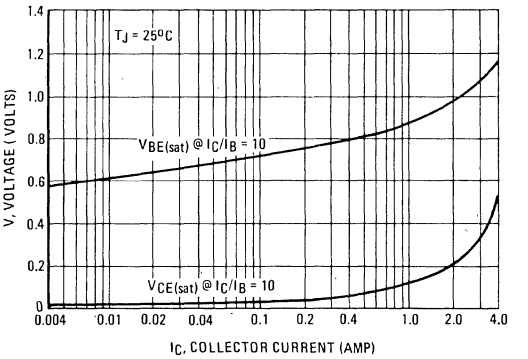


FIGURE 12 – COLLECTOR CUT-OFF REGION

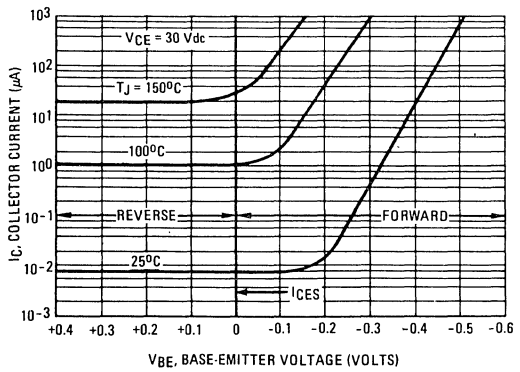
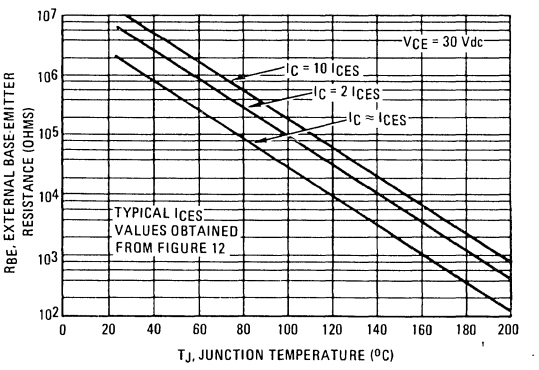


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



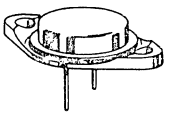
2N6050 thru 2N6052 PNP (SILICON)
2N6057 thru 2N6059 NPN

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier and low frequency switching applications.

- High DC Current Gain — h_{FE} = 3500 (Typ) @ I_C = 5.0 Adc
- Collector-Emitter Sustaining Voltage — @ 100 mA
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6050, 2N6057
  80 Vdc (Min) — 2N6051, 2N6058
  100 Vdc (Min) — 2N6052, 2N6059
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

DARLINGTON 12 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60-80-100 VOLTS 150 WATTS



4

*MAXIMUM RATINGS

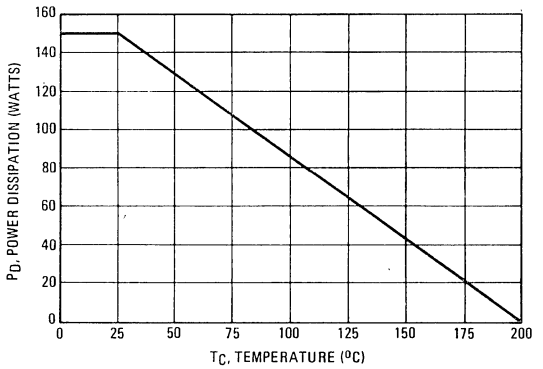
Rating	Symbol	2N6050 2N6057	2N6051 2N6058	2N6052 2N6059	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	12 20			Adc
Base Current	I_B	0.2			Adc
Total Device Dissipation @T_C = 25°C Derate above 25°C	P_D	150 0.857			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200°C			°C

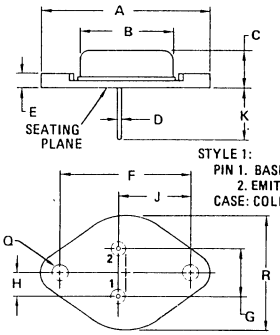
THERMAL CHARACTERISTICS

Characteristic	Symbol	Rating	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 — POWER DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.

CASE 11-01
TO-3

NOTE:
1. DIM "Q" IS DIA.

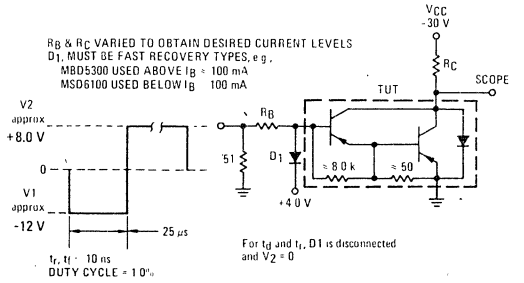
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N6050, 2N6057		60	–	
	2N6051, 2N6058		80	–	
	2N6052, 2N6059		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N6050, 2N6057		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N6051, 2N6058		–	1.0	
(V_{CE} = 50 Vdc, I_B = 0)	2N6052, 2N6059		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc)			–	0.5	
(V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)				5.0	
Emitter Cutoff Current		I_{EBO}	–	2.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 6.0 Adc, V_{CE} = 3.0 Vdc)			750	18,000	
(I_C = 12 Adc, V_{CE} = 3.0 Vdc)			100	–	
Collector-Emitter Saturation Volatage		$V_{CE(sat)}$			Vdc
(I_C = 6.0 Adc, I_B = 24 mAdc)			–	2.0	
(I_C = 12 Adc, I_B = 120 mAdc)			–	3.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$	–	4.0	Vdc
(I_C = 12 Adc, I_B = 120 mAdc)					
Base-Emitter On Voltage		$V_{BE(on)}$	–	2.8	Vdc
(I_C = 6.0 Adc, V_{CE} = 3.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small-Signal Short Circuit Forward Current Transfer Ratio		$\lvert h_{fe} \rvert$	4.0	–	MHz
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)					
Output Capacitance	2N6050/2N6052	C_{ob}	–	500	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6057/2N6059		–	300	
Small-Signal Current Gain		h_{fe}	300	–	–
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)					

*Indicates JEDEC Registered Data

(1) Pulse test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode and voltage polarities.

FIGURE 3 – SWITCHING TIMES

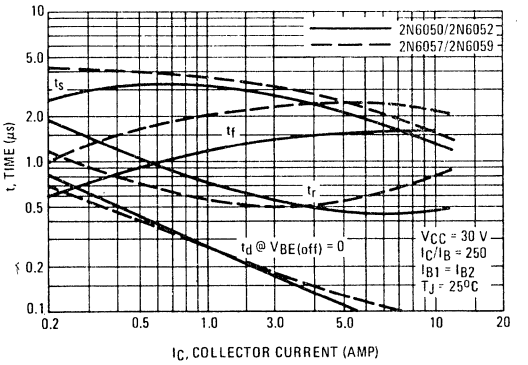
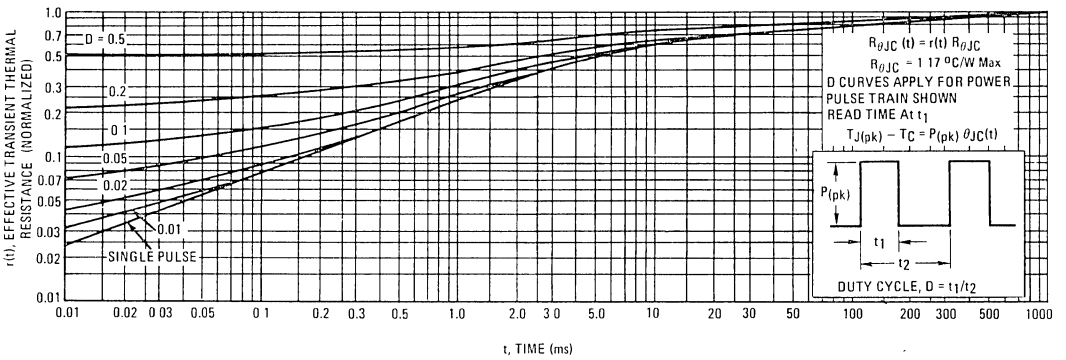


FIGURE 4 – THERMAL RESPONSE



4

ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – 2N6050, 2N6057

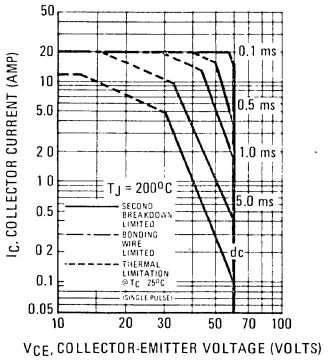


FIGURE 6 – 2N6051, 2N6058

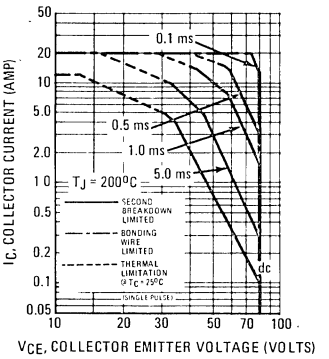
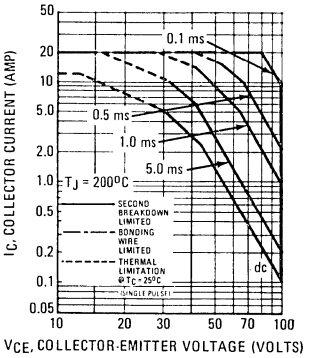


FIGURE 7 – 2N6052, 2N6059



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, 6 and 7 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^oC$ $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 8 – SMALL-SIGNAL CURRENT GAIN

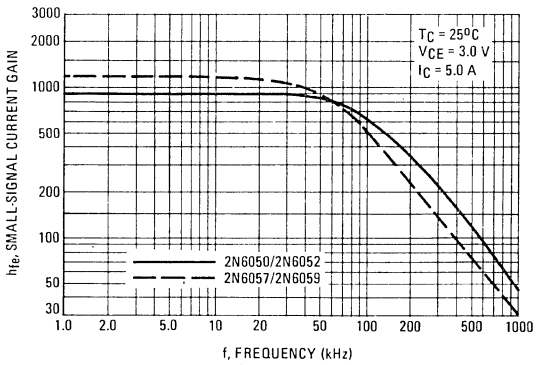
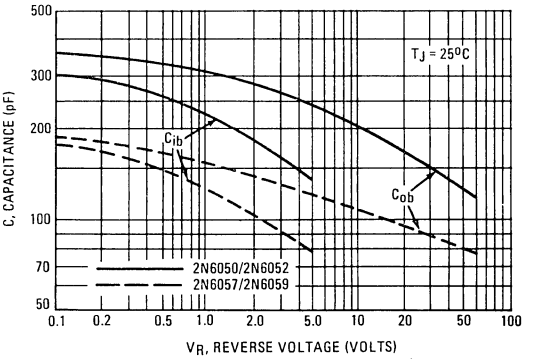


FIGURE 9 – CAPACITANCE

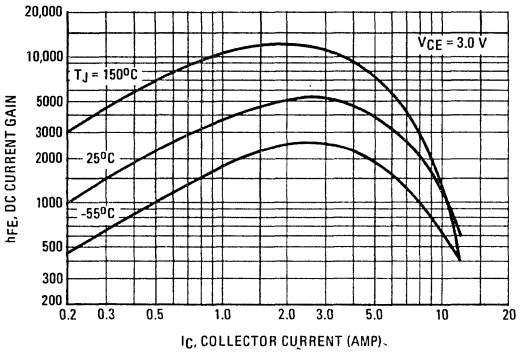


4

PNP
2N6050, 2N6051, 2N6052

NPN
2N6057, 2N6058, 2N6059

FIGURE 10 – DC CURRENT GAIN



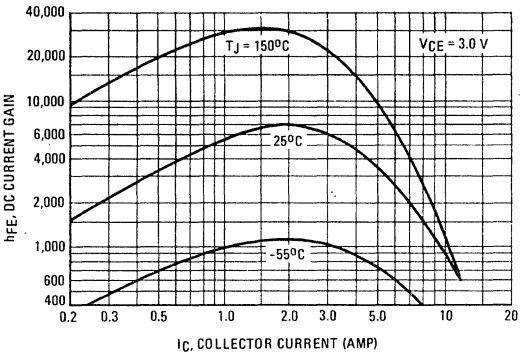
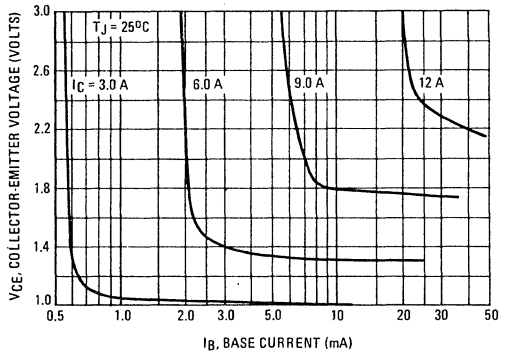


FIGURE 11 – COLLECTOR SATURATION REGION



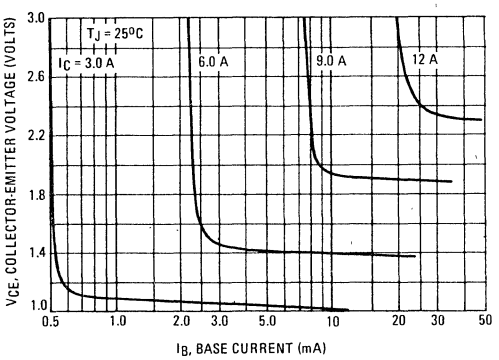
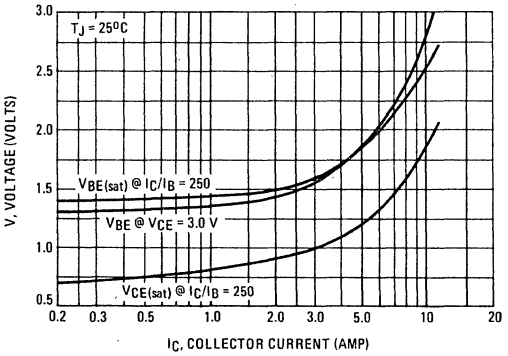
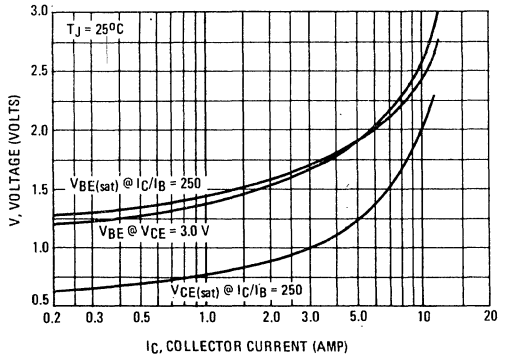


FIGURE 12 – "ON" VOLTAGES





PNP
2N6050, 2N6051, 2N6052

NPN
2N6057, 2N6058, 2N6059

FIGURE 13 – TEMPERATURE COEFFICIENTS

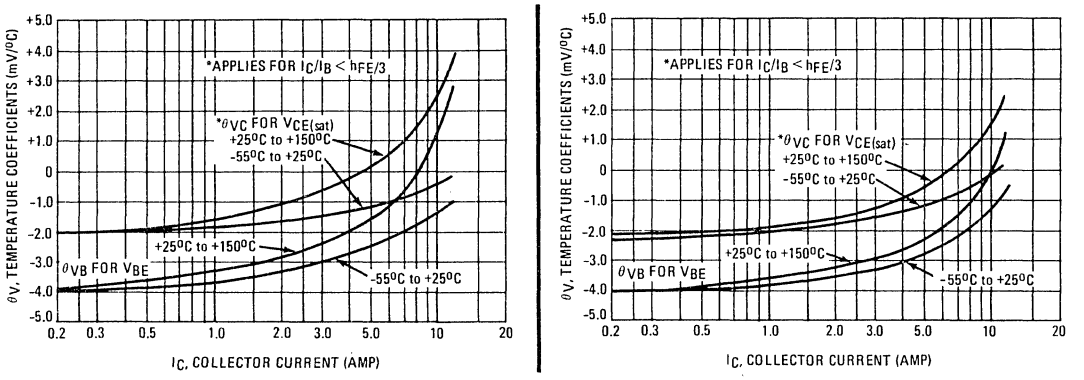


FIGURE 14 – COLLECTOR CUT-OFF REGION

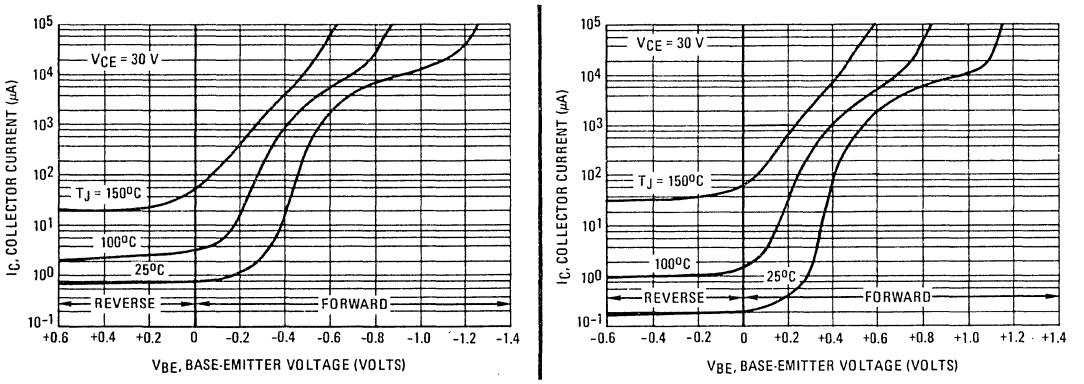
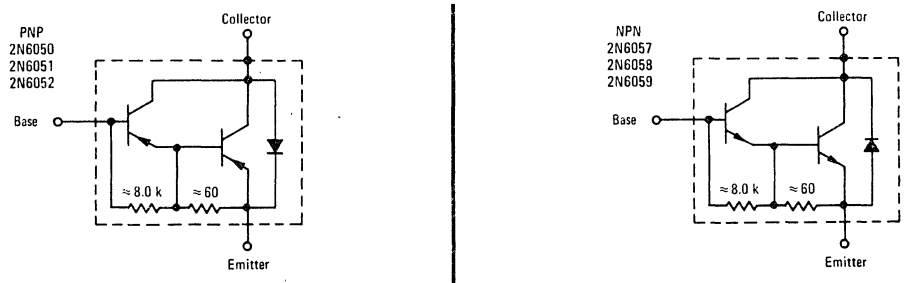


FIGURE 15 – DARLINGTON SCHEMATICS



2N6053, 2N6054, 2N6298, 2N6299 PNP (SILICON)
2N6055, 2N6056, 2N6300, 2N6301 NPN

4

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier and low frequency switching applications.

- High DC Current Gain –
  h_{FE} = 3000 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage – @ 100 mA
  $V_{CEO(sus)}$ = 60 Vdc (Min) – 2N6053, 2N6055, 2N6298, 2N6300
  = 80 Vdc (Min) – 2N6054, 2N6056, 2N6299, 2N6301
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 4.0 Adc
  = 3.0 Vdc (Max) @ I_C = 8.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

DARLINGTON 8 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60-80 VOLTS 75,100 WATTS

*MAXIMUM RATINGS

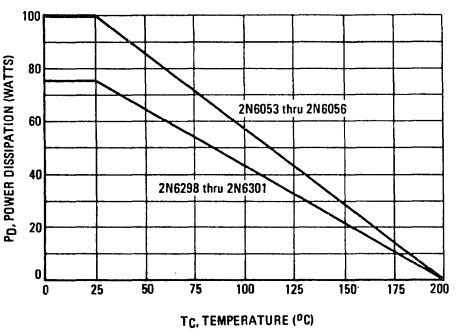
Rating	Symbol	2N6053 2N6055 2N6298 2N6300	2N6054 2N6056 2N6299 2N6301	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous	I_C	8.0		Adc
Peak		16		
Base Current	I_B	120		mAdc
		2N6053 2N6054 2N6055 2N6056	2N6298 2N6299 2N6300 2N6301	
Total Device Dissipation @ T_C = 25°C	P_D	100	75	Watts
Derate above 25°C		0.571	0.428	W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

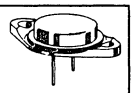
Characteristic	Symbol	2N6053 2N6054 2N6055 2N6056	2N6298 2N6299 2N6300 2N6301	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	2.33	°C/W

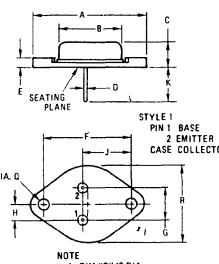
*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING



2N6053
2N6054
2N6055
2N6056



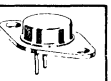


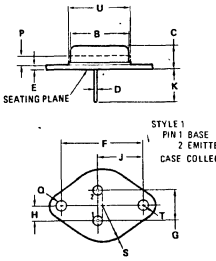
NOTE
1 DIM "Q" IS DIA

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case
CASE 11-01
(TO-3)

2N6298
2N6299
2N6300
2N6301





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	8.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply

CASE 80-02
TO-66

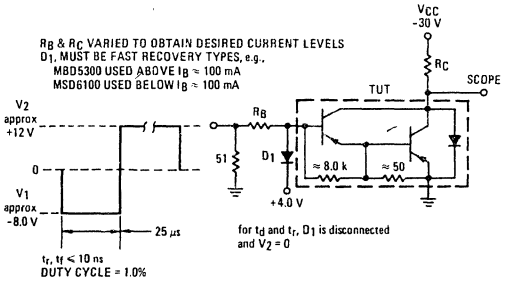
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N6053, 2N6055, 2N6298, 2N6300		60	–	
	2N6054, 2N6056, 2N6299, 2N6301		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N6053, 2N6055, 2N6298, 2N6300		–	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	2N6054, 2N6056, 2N6299, 2N6301		–	0.5	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)			–	0.5	
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C			–	5.0	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)			–	2.0	
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			750	18000	
(I_C = 8.0 Adc, V_{CE} = 3.0 Vdc)			100	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 4.0 Adc, I_B = 16 mAdc)			–	2.0	
(I_C = 8.0 Adc, I_B = 80 mAdc)			–	3.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 8.0 Adc, I_B = 80 mAdc)			–	4.0	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			–	2.8	
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small-Signal Short Circuit Current Transfer Ratio		$\lvert h_{fe} \rvert$			–
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)			4.0	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6053, 2N6054, 2N6298, 2N6299		–	300	
	2N6055, 2N6056, 2N6300, 2N6301		–	200	
Small-Signal Current Gain		h_{fe}			–
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)			300	–	

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0 %.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode, polarities and input pulses.

FIGURE 3 – SWITCHING TIMES

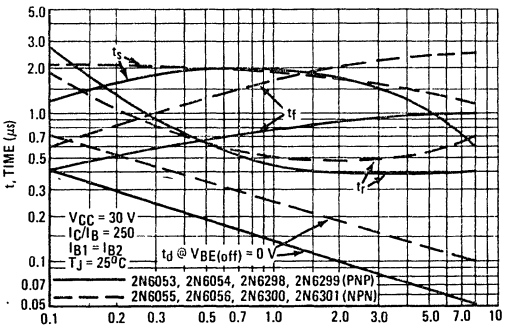
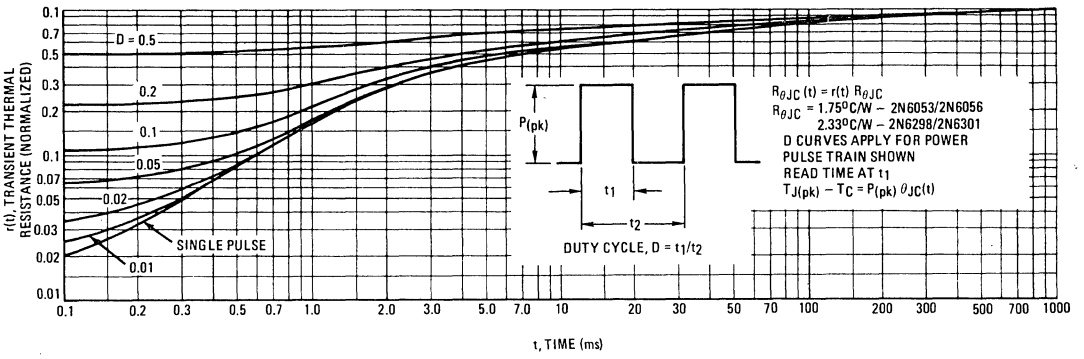


FIGURE 4 – THERMAL RESPONSE



4

ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – 2N6053 thru 2N6056

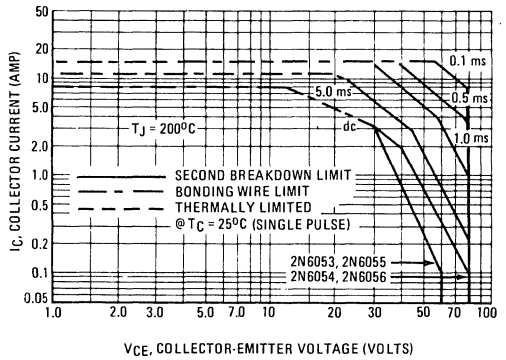
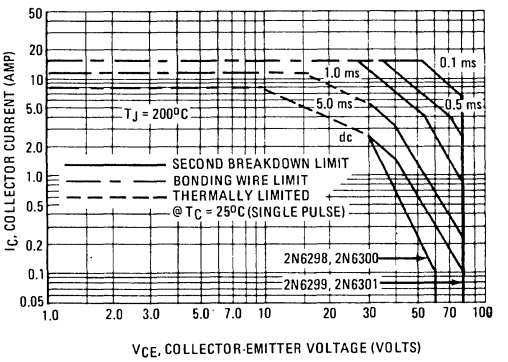


FIGURE 6 – 2N6298 thru 2N6301



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figures 5 and 6 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 7 – SMALL-SIGNAL CURRENT GAIN

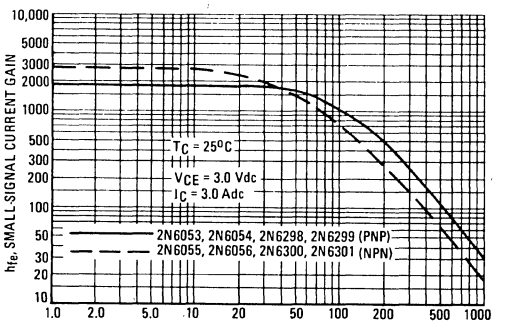
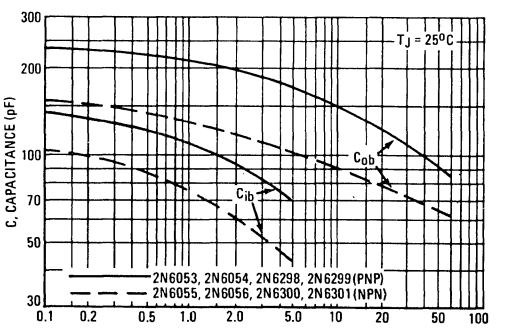


FIGURE 8 – CAPACITANCE



PNP

2N6053, 2N6054, 2N6298, 2N6299

NPN

2N6055, 2N6056, 2N6300, 2N6301

FIGURE 9 – DC CURRENT GAIN

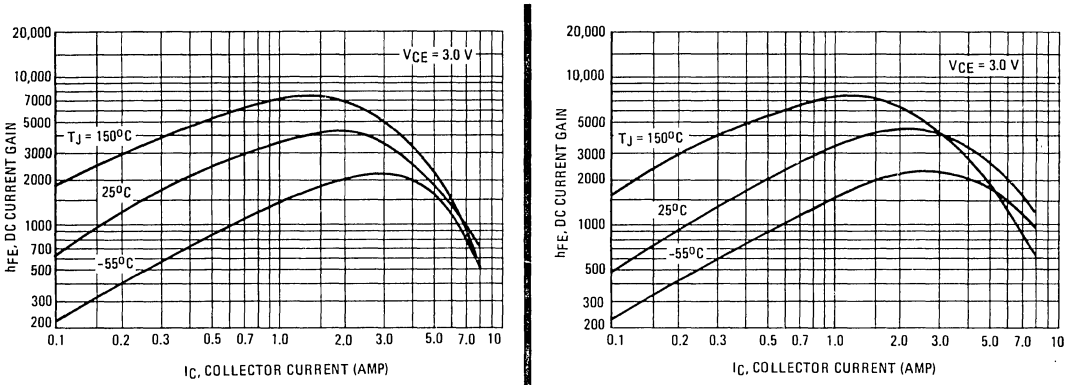


FIGURE 10 – COLLECTOR SATURATION REGION

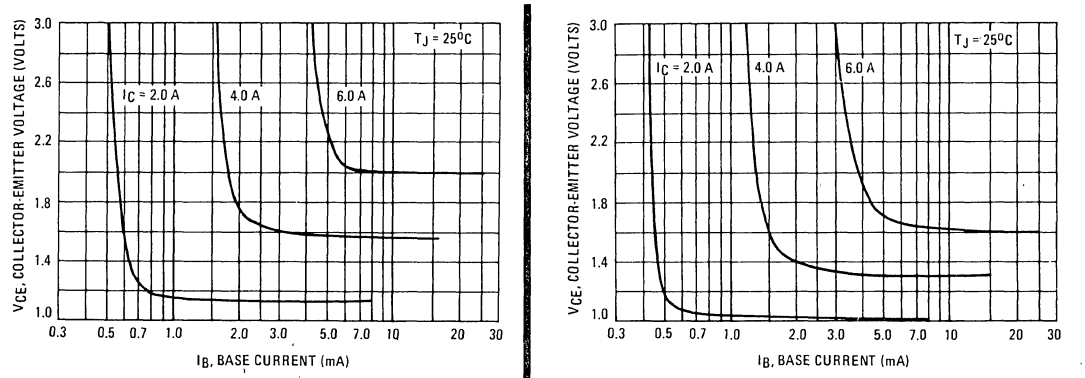
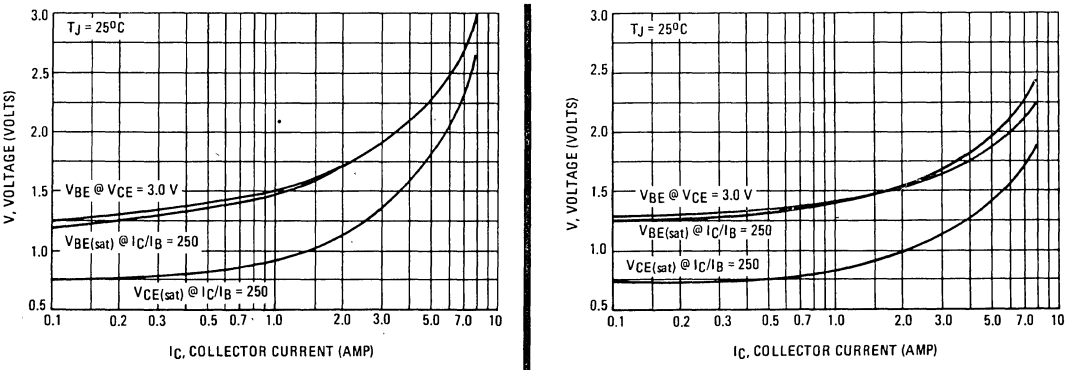


FIGURE 11 – "ON" VOLTAGES



PNP

2N6053, 2N6054, 2N6298, 2N6299

NPN

2N6055, 2N6056, 2N6300, 2N6301

FIGURE 12 – TEMPERATURE COEFFICIENTS

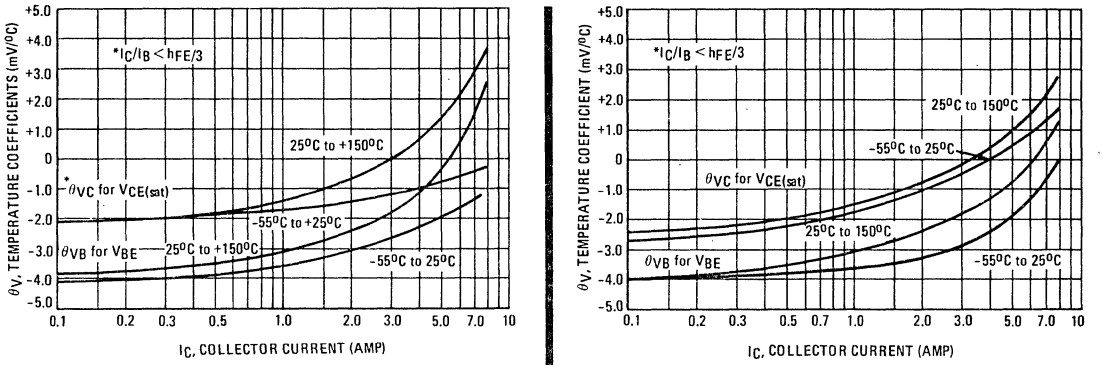


FIGURE 13 – COLLECTOR CUT-OFF REGION

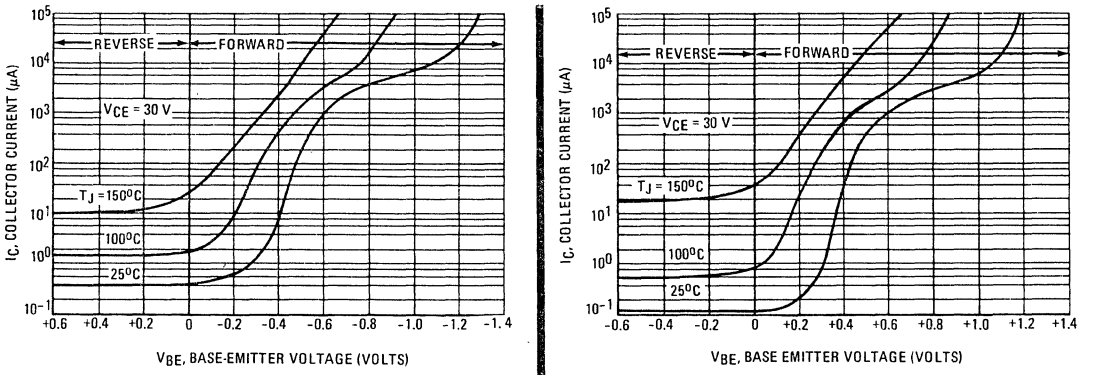
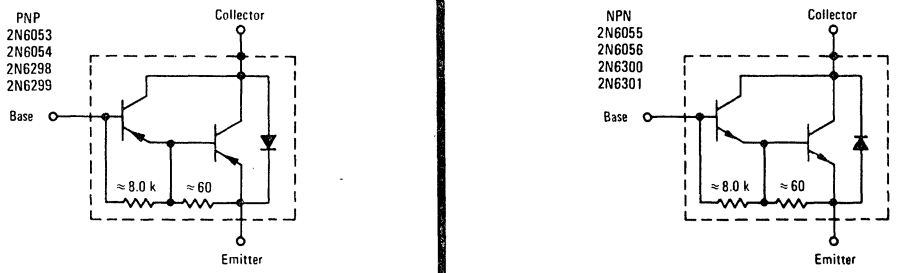


FIGURE 14 – DARLINGTON SCHEMATIC



2N6077
2N6078

HIGH VOLTAGE NPN SILICON TRANSISTORS

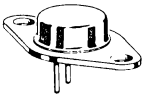
. . . the 2N6077 and 2N6078 transistors are designed for high-voltage, high-speed switching applications. They are characterized for operating directly off the rectified 110 Volt power lines in circuits such as:

- Switching Regulators
- Solenoid and Relay Drivers
- Motor Controls
- Inverters

7 AMPERES

NPN SILICON POWER TRANSISTORS

275–300 VOLTS
45 WATTS



4

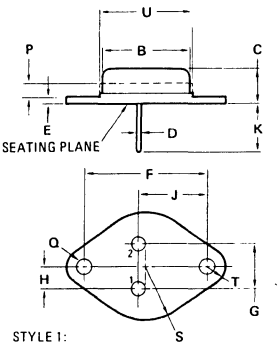
*MAXIMUM RATINGS

Rating	Symbol	2N6077	2N6078	Unit
Collector-Emitter Voltage	V_{CEX}	300	275	Vdc
Collector-Base Voltage	V_{CBO}	300	275	Vdc
Emitter-Base Voltage	V_{EBO}	6		Vdc
Collector Current — Continuous — Peak	I_C I_{CM}	7 10		Adc
Base Current — Continuous	I_B	4		Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	45 0.257		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.9	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	^oC

*Indicates JEDEC Registered Data



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

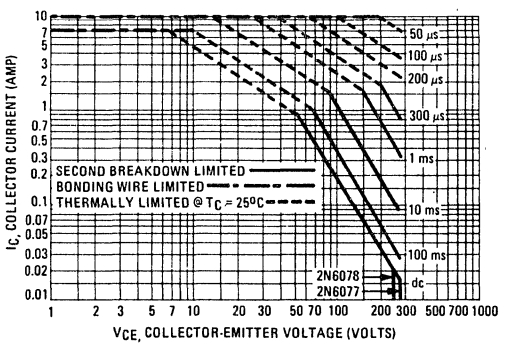
CASE 80-02
TO-66

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mA, I_B = 0)	2N6077		275	–	
	2N6078		250	–	
Emitter Cutoff Current		I_{EBO}	–	1.0	mAdc
(V_{BE} = 6 Vdc, I_C = 0)					
Collector Cutoff Current		I_{CEV}			mAdc
(V_{CEV} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6077		–	5.0	
	2N6078		–	0.05	
(V_{CEV} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6077		–	8.0	
	2N6078		–	0.2	
Collector Cutoff Current		I_{CEO}			mA
(V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6077		–	2.0	
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 1.2 Adc, V_{CE} = 1 Vdc)			12	70	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 1.2 Adc, I_B = 0.2 Adc)	2N6077		–	0.5	
	2N6078				
(I_C = 3 Adc, I_B = 0.6 Adc)	2N6077		–	1.0	
(I_C = 5 Adc, I_B = 1 Adc)	2N6078		–	3.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 1.2 Adc, I_B = 0.2 Adc)	2N6077		–	1.6	
	2N6078				
(I_C = 3 Adc, I_B = 0.6 Adc)	2N6077		–	1.9	
(I_C = 5 Adc, I_B = 1 Adc)	2N6078		–	2.0	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		$\|h_{fe}\|$	1.0	–	MHz
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Rise Time	(V_{CC} = 250 Vdc, I_C = 1.2 Adc,	t_r	–	0.75	μs
Storage Time	I_{B1} = I_{B2} = 200 mAdc = 100 μs,	t_s	–	5.0	μs
Fall Time	Duty Cycle ≤ 2.0%)	t_f	–	0.75	μs

* Indicates JEDEC Registered Data

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe Operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 12 and 13 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

PNP NPN

2N6107 2N6288
2N6109 2N6290
2N6111 2N6292

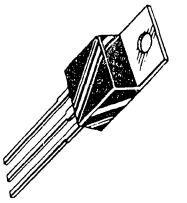
COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 7.0 Amperes
  h_{FE} = 30–150 @ I_C = 3.0 Adc – 2N6111, 2N6288
  = 2.3 (Min) @ I_C = 7.0 Adc – All Devices
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 30 Vdc (Min) – 2N6111, 2N6288
  = 50 Vdc (Min) – 2N6109, 2N6290
  = 70 Vdc (Min) – 2N6107, 2N6292
- High Current Gain – Bandwidth Product
  f_T = 4.0 MHz (Min) @ I_C = 500 mAdc – 2N6288, 90, 92
  = 10 MHz (Min) @ I_C = 500 mAdc – 2N6107, 09, 11
- TO-220AB Compact Package
- TO-66 Leadform Also Available

7 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON

30–50–70 VOLTS
40 WATTS



4

*MAXIMUM RATINGS

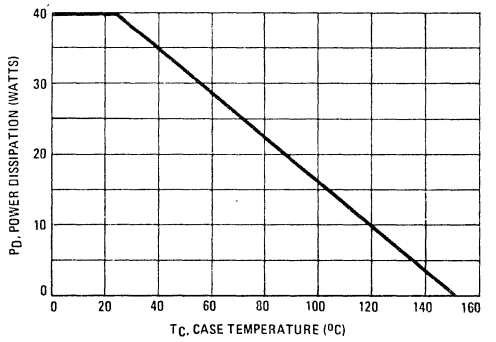
Rating	Symbol	2N6111 2N6288	2N6109 2N6290	2N6107 2N6292	Unit
Collector-Emitter Voltage	V_{CEO}	30	50	70	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous Peak	I_C	7.0 10			Adc
Base Current	I_B	3.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			°C

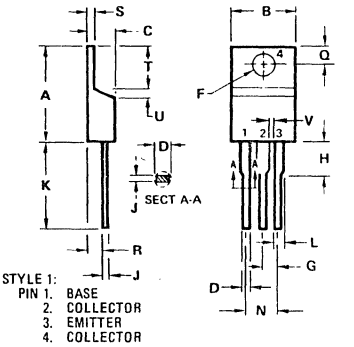
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING





DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02
TO-220AB

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

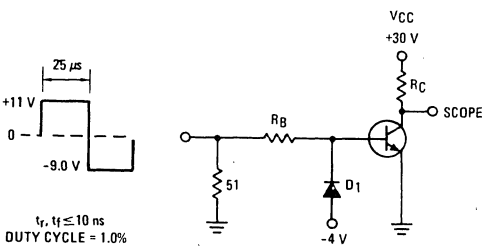
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N6111, 2N6288		30	–	
	2N6109, 2N6290		50	–	
	2N6107, 2N6292		70	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N6111, 2N6288		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N6109, 2N6290		–	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N6107, 2N6292		–	1.0	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6111, 2N6288		–	100	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6109, 2N6290		–	100	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6107, 2N6292		–	100	
(V_{CE} = 30 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6111, 2N6288		–	2.0	mAdc
(V_{CE} = 50 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6109, 2N6290		–	2.0	
(V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6107, 2N6292		–	2.0	
Emitter Cutoff Current		I_{EBO}	–	1.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)	2N6107, 2N6292		30	150	
(I_C = 2.5 Adc, V_{CE} = 4.0 Vdc)	2N6109, 2N6290		30	150	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	2N6111, 2N6288		30	150	
(I_C = 7.0 Adc, V_{CE} = 4.0 Vdc)	All Devices		2.3	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	–	3.5	Vdc
(I_C = 7.0 Adc, I_B = 3.0 Adc)					
Base-Emitter On Voltage		$V_{BE(on)}$	–	3.0	Vdc
(I_C = 7.0 Adc, V_{CE} = 4.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2)		f_T			MHz
(I_C = 500 mAdc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 MHz)					
	2N6288, 90, 92		4.0	–	
	2N6107, 09, 11		10	–	
Output Capacitance		C_{ob}	–	250	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)					
Small-Signal Current Gain		h_{fe}	20	–	–
(I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 50 kHz)					

*Indicates JEDEC Registered Data.

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2)$f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx$100 mA
MSD6100 USED BELOW $I_B \approx$100 mA

FIGURE 3 – TURN-ON TIME

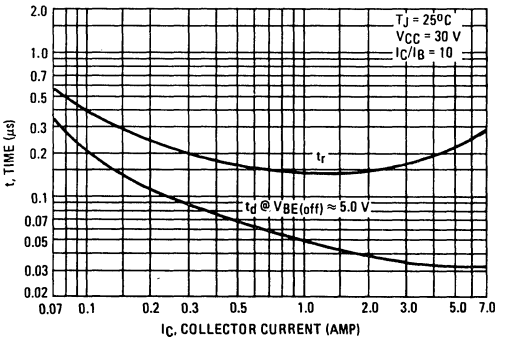


FIGURE 4 – THERMAL RESPONSE

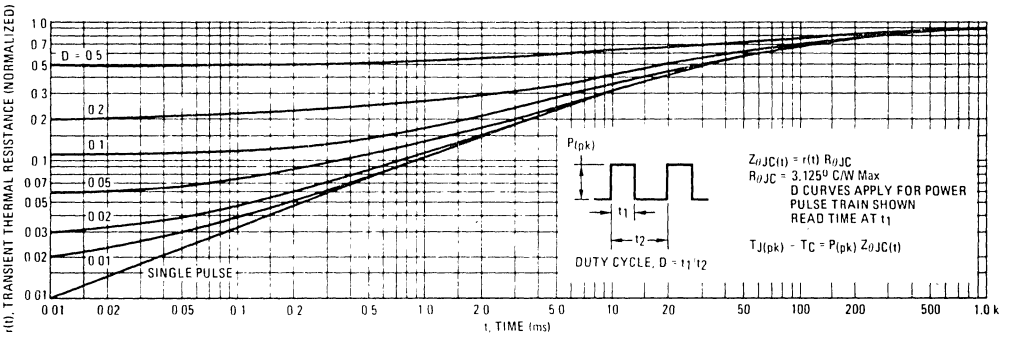


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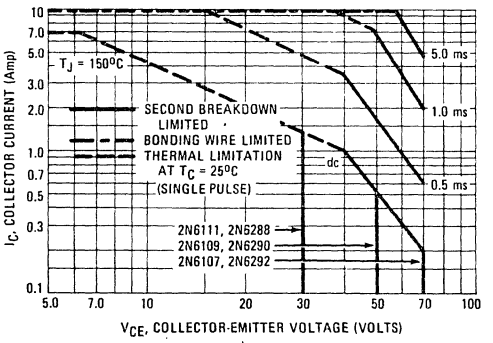
FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

FIGURE 6 – TURN-OFF TIME

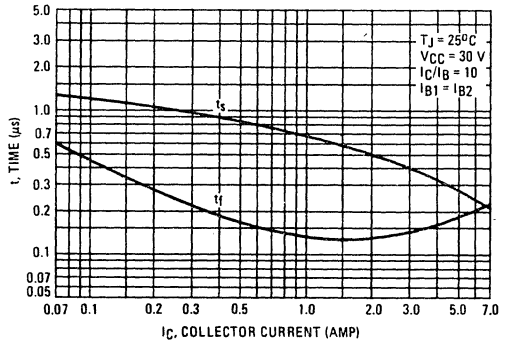


FIGURE 7 – CAPACITANCE

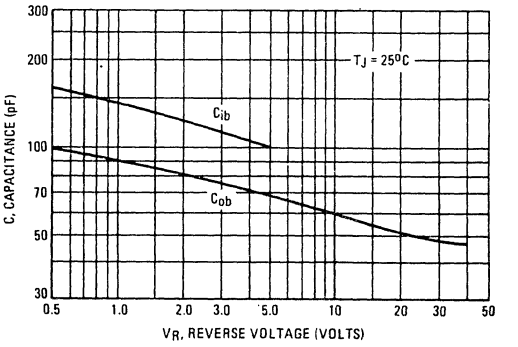


FIGURE 8 – DC CURRENT GAIN

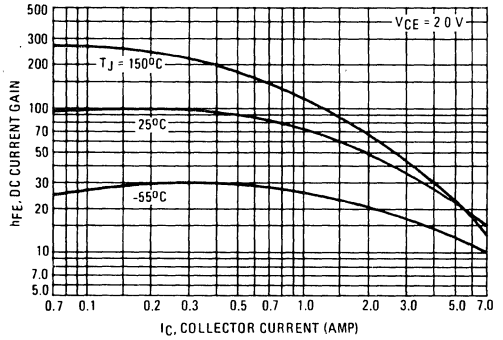


FIGURE 9 – COLLECTOR SATURATION REGION

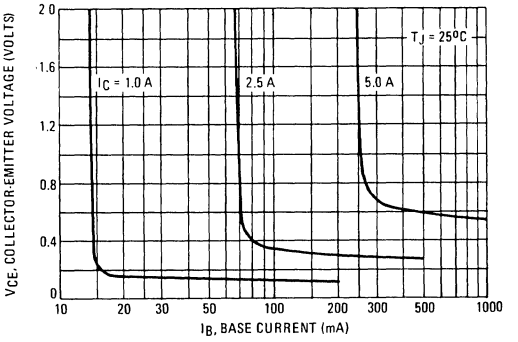


FIGURE 10 – "ON" VOLTAGES

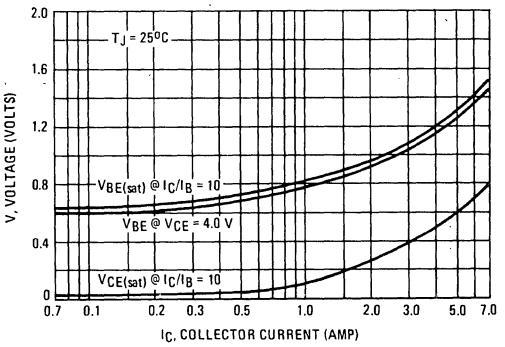


FIGURE 11 – TEMPERATURE COEFFICIENTS

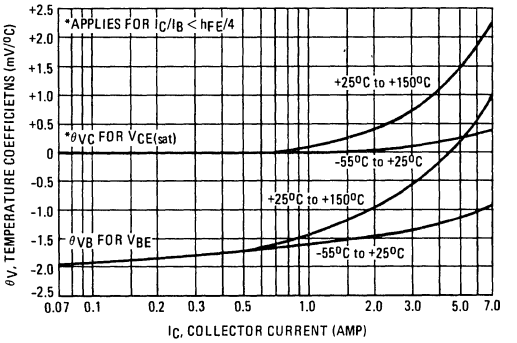


FIGURE 12 – COLLECTOR CUT-OFF REGION

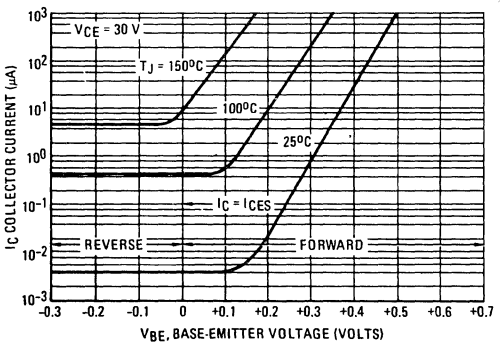
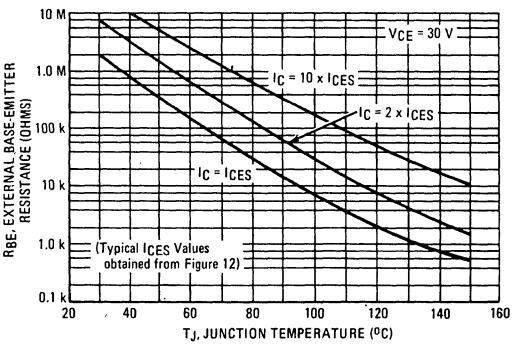


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



NPN 2N6121 2N6122 2N6123

PNP 2N6124 2N6125 2N6126

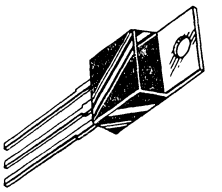
COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in power amplifier and switching circuits, – packaged in the compact TO-220AB outline. TO-66 leadform also available.

4 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

45-80 VOLTS
40 WATTS



4

*MAXIMUM RATINGS

Rating	Symbol	2N6121 2N6124	2N6122 2N6125	2N6123 2N6126	Unit
Collector-Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector-Base Voltage	V_{CB}	45	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current	I_C	← 4.0 →			Adc
Base Current	I_B	← 1.0 →			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 40 →			Watts mW/°C
		← 320 →			
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← −65 to +150 →			°C

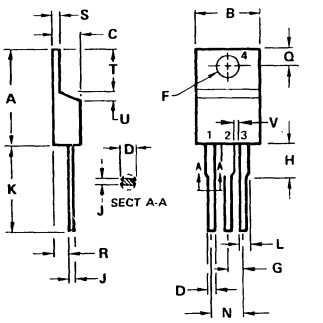
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	3.12	°C/W

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 0.1 Adc, I_B = 0)	2N6121, 2N6124		45	–	
	2N6122, 2N6125		60	–	
	2N6123, 2N6126		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 45 Vdc, I_B = 0)	2N6121, 2N6124		–	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N6122, 2N6125		–	1.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N6123, 2N6126		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6121, 2N6124		–	0.1	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6122, 2N6125		–	0.1	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6123, 2N6126		–	0.1	
(V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6121, 2N6124		–	2.0	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6122, 2N6125		–	2.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6123, 2N6126		–	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 45 Vdc, I_E = 0)	2N6121, 2N6124		–	0.1	
(V_{CB} = 60 Vdc, I_E = 0)	2N6122, 2N6125		–	0.1	
(V_{CB} = 80 Vdc, I_E = 0)	2N6123, 2N6126		–	0.1	
Emitter Cutoff Current		I_{EBO}	–	1.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	2N6126, 2N6124		25	100	
	2N6122, 2N6125		25	100	
	2N6123, 2N6126		20	80	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	2N6121, 2N6124		10	–	
	2N6122, 2N6125		10		
	2N6123, 2N6126		7.0	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 0.15 Adc)			–	0.6	
(I_C = 4.0 Adc, I_B = 1.0 Adc)			–	1.4	
Base-Emitter On Voltage (1)		$V_{BE(on)}$	–	1.2	Vdc
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain		h_{fe}	25	–	–
(I_C = 0.1 Adc, V_{CE} = 2.0 Vdc, f = 1.0 kHz)					
Current-Gain-Bandwidth Product		f_T	2.5	–	MHz
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)					

(1) Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.
*Indicates JEDEC Registered Data.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–

CASE 221A-02
TO-220AB

FIGURE 1 – DC CURRENT GAIN

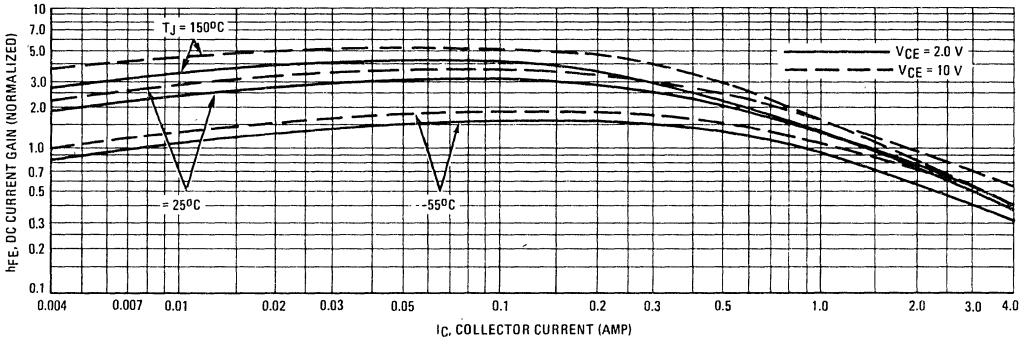


FIGURE 2 – COLLECTOR SATURATION REGION

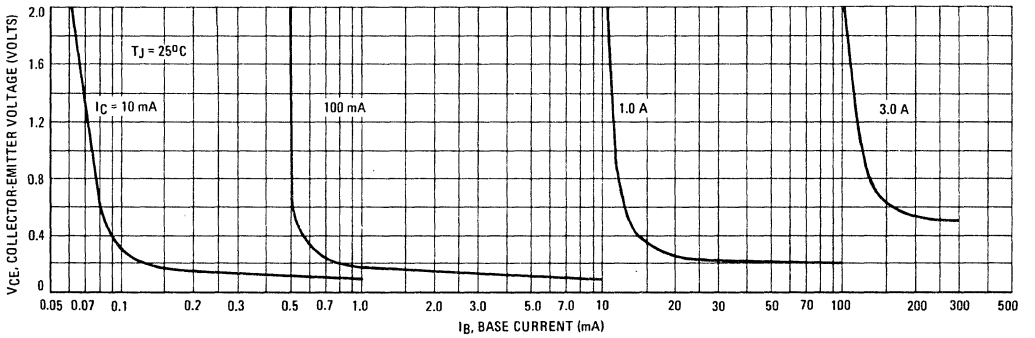


FIGURE 3 – "ON" VOLTAGES

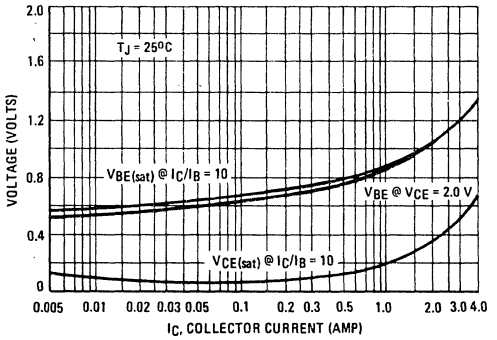


FIGURE 4 – TEMPERATURE COEFFICIENTS

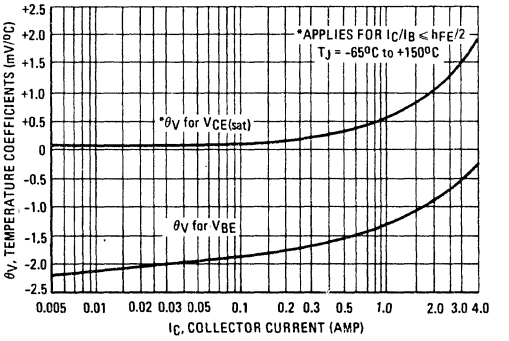


FIGURE 5 – COLLECTOR CUT-OFF REGION

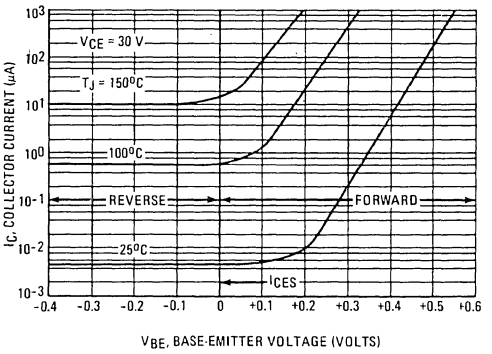


FIGURE 6 – EFFECTS OF BASE-EMITTER RESISTANCE

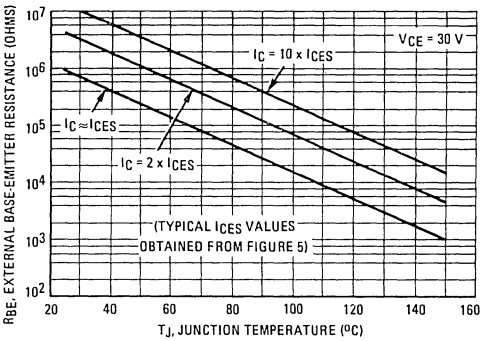
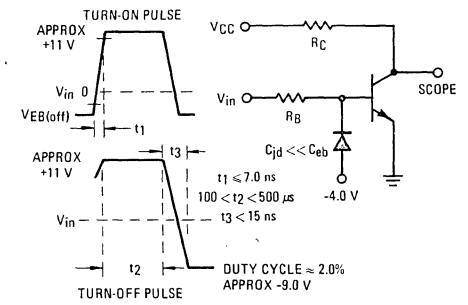


FIGURE 7 – SWITCHING TIME EQUIVALENT CIRCUIT



R_B AND R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

FIGURE 8 – CAPACITANCE

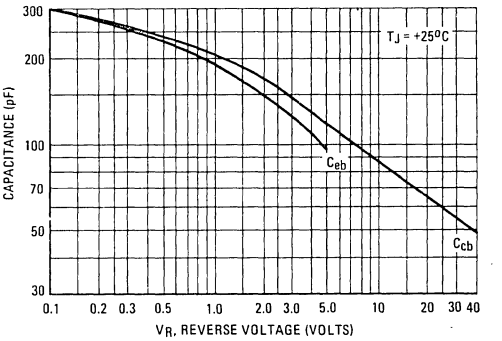


FIGURE 9 – TURN-ON TIME

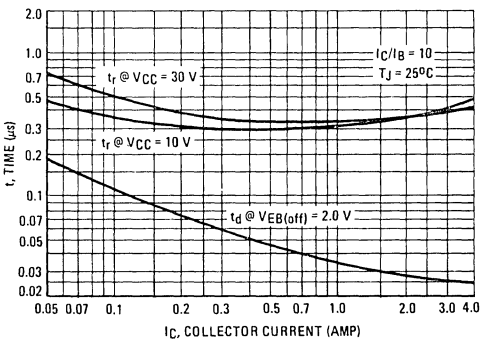
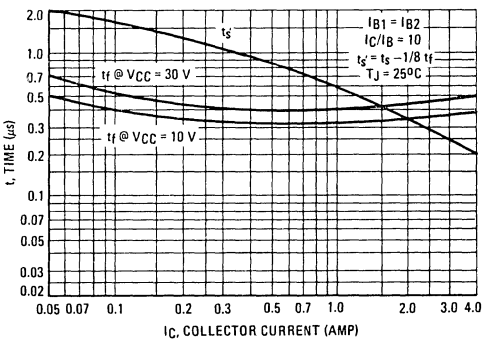
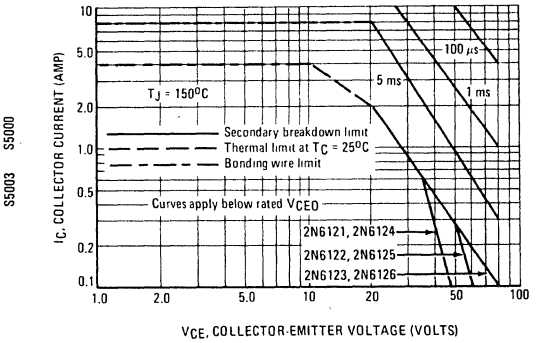


FIGURE 10 – TURN-OFF TIME



RATING AND THERMAL DATA

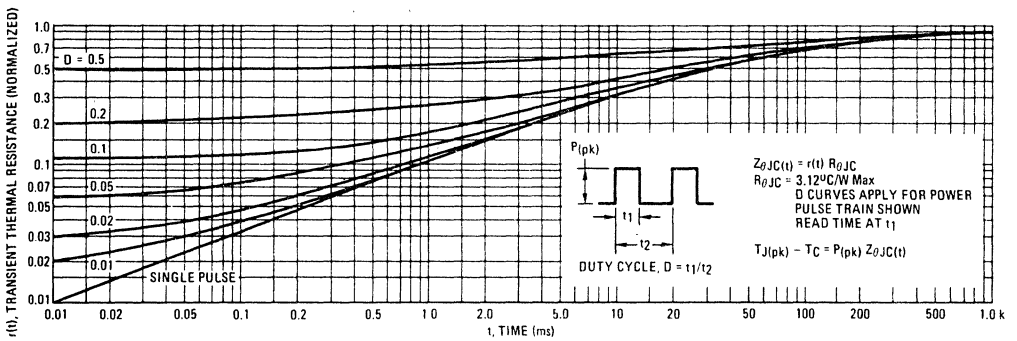
FIGURE 11 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: peak junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

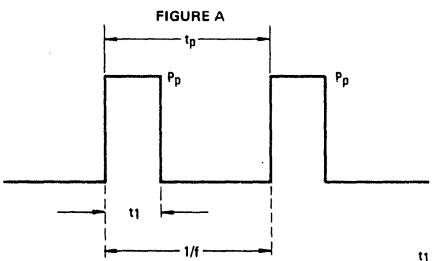
The data of Figure 11 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 12 – THERMAL RESPONSE



DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

FIGURE A



A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC}.

Example:

The 2N6121 is dissipating 50 watts under the following conditions: t_1 = 0.1 ms, t_p = 0.5 ms. (D = 0.2).

Using Figure 12, at a pulse width of 0.1 ms and D = 0.2, the reading of r(t_1, D) is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_P \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2°C$$

2N6186 thru 2N6189

MEDIUM-POWER PNP SILICON TRANSISTORS

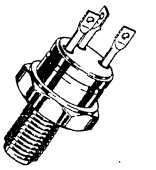
. . . designed for switching and wide-band amplifier applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 10 Adc
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact, High Dissipation TO-59 Case
- Isolated Collector Configuration
- Complement to NPN 2N5346 thru 2N5349

10 AMPERE

POWER TRANSISTORS PNP SILICON

80–100 VOLTS
60 WATTS



***MAXIMUM RATINGS**

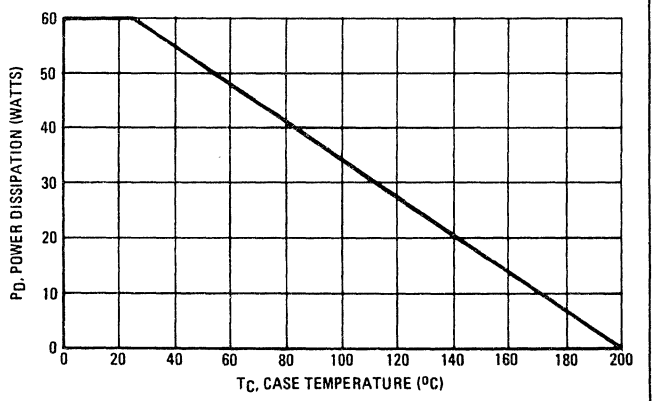
Rating	Symbol	2N6186 2N6187	2N6188 2N6189	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	10		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	60 343		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200		°C

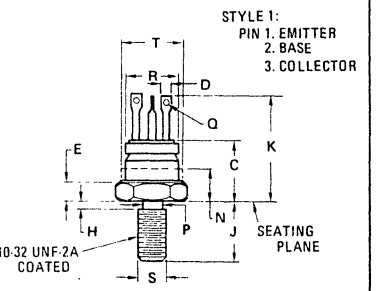
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.91	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	10.77	11.10	0.424	0.437
C	8.13	11.89	0.320	0.468
E	2.29	3.81	0.090	0.150
G	4.70	5.46	0.185	0.215
H	–	1.98	–	0.078
J	10.16	11.56	0.400	0.455
K	14.48	19.38	0.570	0.763
L	2.29	2.79	0.090	0.110
N	–	6.35	–	0.250
P	4.14	4.80	0.163	0.189
Q	1.02	1.65	0.040	0.065
R	8.08	9.65	0.318	0.380
S	4.212	4.310	0.1658	0.1697
T	9.65	11.10	0.380	0.437

All JEDEC dimensions and notes apply
Collector isolated from case.

CASE 160-03
TO-59

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C, unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1)		–	$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N6186, 87			80	–	
	2N6188, 89			100	–	
Collector Cutoff Current		–	I_{CEO}			μAdc
(V_{CE} = 75 Vdc, I_B = 0)	2N6186, 87			–	100	
(V_{CE} = 90 Vdc, I_B = 0)	2N6188, 89			–	100	
Collector Cutoff Current		12	I_{CEX}			μAdc
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6186, 87			–	10	
(V_{CE} = 90 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6188, 89			–	10	
(V_{CE} = 75 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6186, 87			–	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6188, 89			–	1.0	
Collector Cutoff Current		–	I_{CBO}			μAdc
(V_{CB} = Rated V_{CB}, I_E = 0)				–	10	
Emitter Cutoff Current		–	I_{EBO}			μAdc
(V_{BE} = 6.0 Vdc, I_C = 0)				–	100	
ON CHARACTERISTICS (1)						
DC Current Gain		8	h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	2N6186, 88			30	–	
	2N6187, 89			60	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	2N6186, 88			30	120	
	2N6187, 89			60	240	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N6186, 88			20	–	
	2N6187, 89			40	–	
Collector-Emitter Saturation Voltage		9, 10, 11	$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	0.7	
(I_C = 7.0 Adc, I_B = 0.7 Adc)				–	1.2	
Base-Emitter Saturation Voltage		10, 11	$V_{BE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	1.2	
(I_C = 10 Adc, I_B = 1.0 Adc)				–	2.0	
DYNAMIC CHARACTERISTICS						
Current-Gain–Bandwidth Product (2)		–	f_T			MHz
(I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{Test} = 10 MHz)				30	–	
Output Capacitance		7	C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)				–	300	
Input Capacitance		7	C_{ib}			pF
(V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)				–	1250	
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 40 Vdc, $V_{EB(off)}$ = 3.0 Vdc,	2.3	t_d	–	100	ns
Rise Time	(I_C = 2.0 Adc, I_{B1} = 200 mAdc)		t_r	–	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc,	2.6	t_s	–	2.0	μs
Fall Time	I_{B1} = I_{B2} = 200 mAdc)		t_f	–	200	ns

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≈ 300 μs, Duty Cycle ≈ 2.0%.
(2) $f_T = |h_{fe}| \cdot f_{Test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

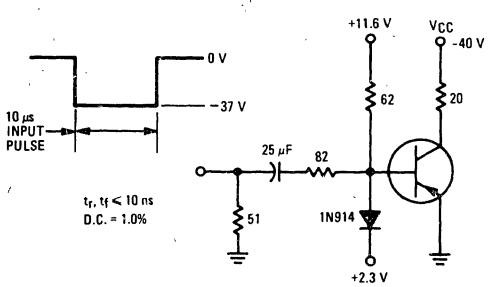


FIGURE 3 – TURN-ON TIME

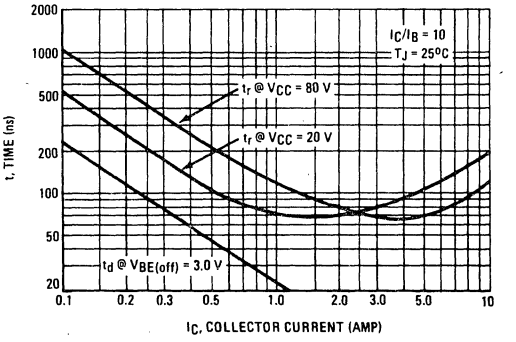


FIGURE 4 – THERMAL RESPONSE

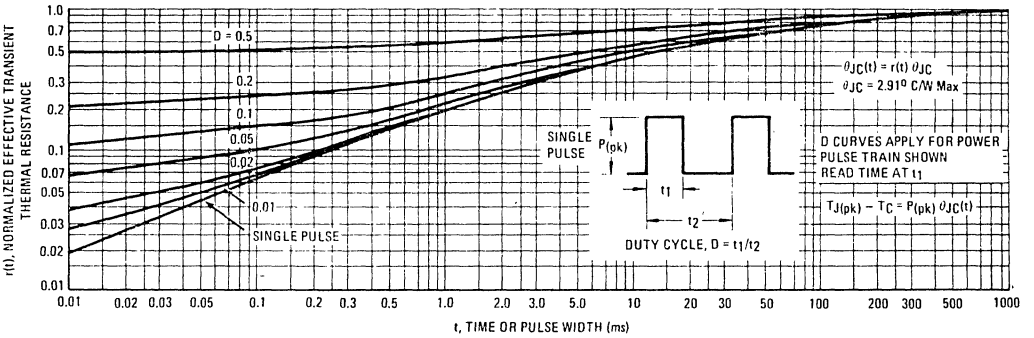
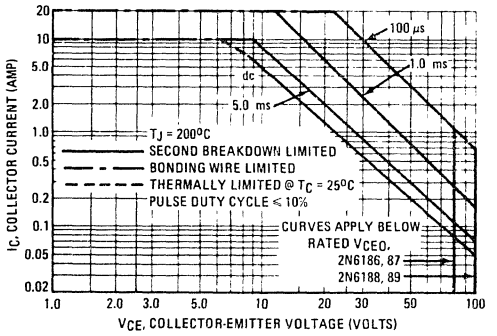


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

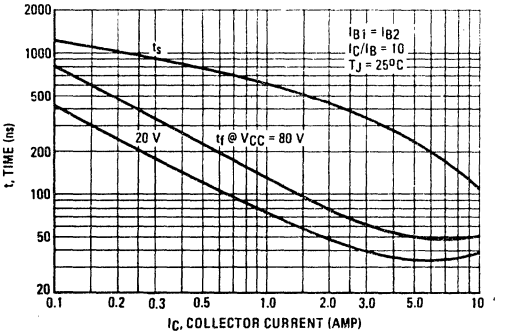


FIGURE 7 – CAPACITANCE versus VOLTAGE

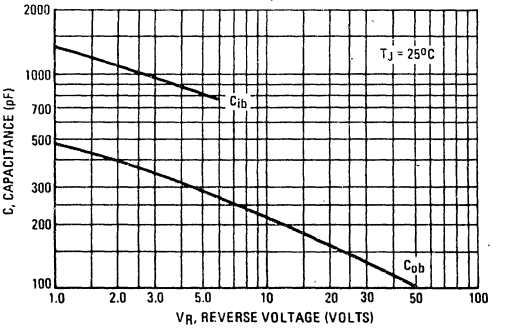


FIGURE 8 – DC CURRENT GAIN

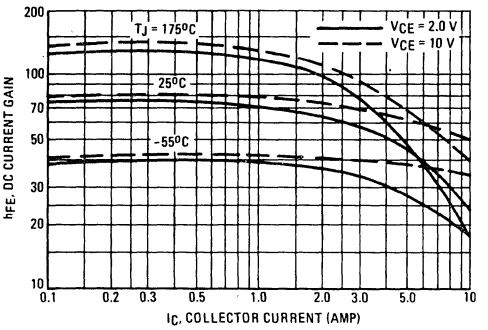


FIGURE 9 – COLLECTOR SATURATION REGION

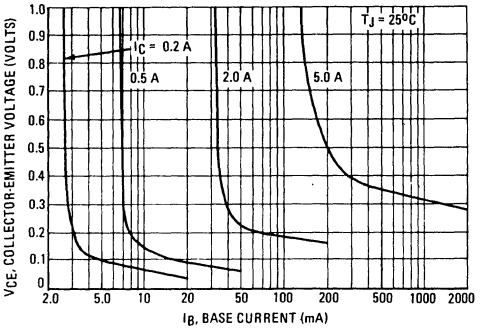


FIGURE 10 – "ON" VOLTAGES

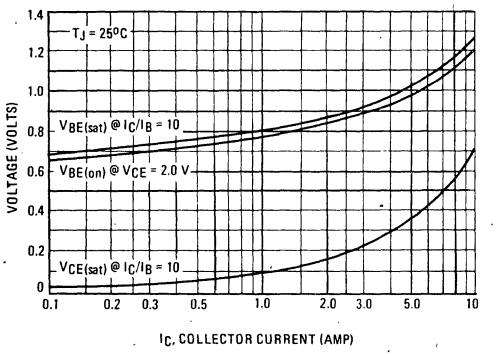


FIGURE 11 – TEMPERATURE COEFFICIENTS

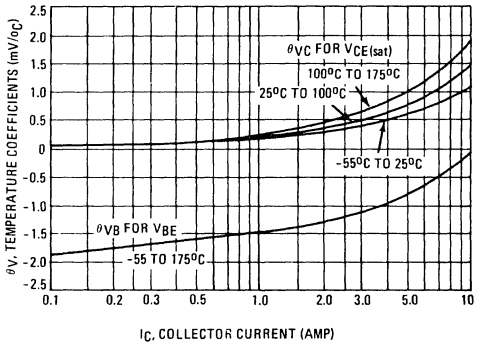


FIGURE 12 – COLLECTOR CUT-OFF REGION

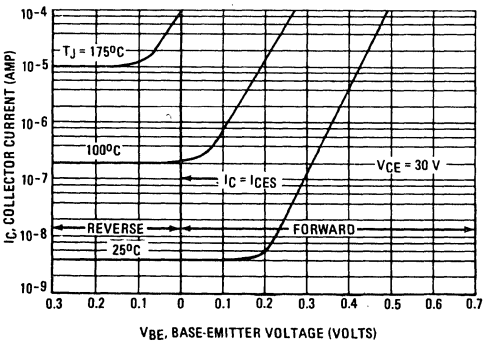
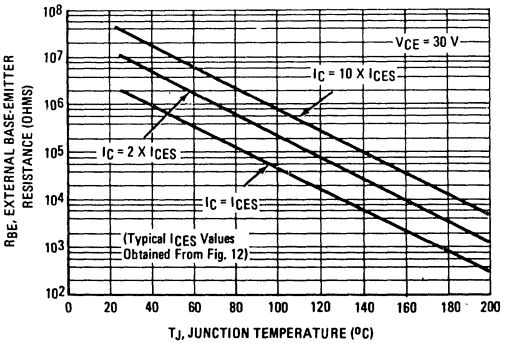


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



2N6190 thru 2N6193

MEDIUM-POWER PNP SILICON TRANSISTORS

. . . designed for switching and wide band amplifier applications.

- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 5.0 Amp
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact TO-39 Case for Critical Space Limited Applications
- Complement to NPN 2N5336 thru 2N5339

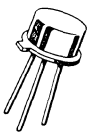
5 AMPERE POWER TRANSISTORS

PNP SILICON

80-100 VOLTS
10 WATTS

*MAXIMUM RATINGS

Rating	Symbol	2N6190 2N6191	2N6192 2N6193	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous	I_C	5.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ T_C = 25°C	P_D	10		Watts
Derate above 25°C		57.1		mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

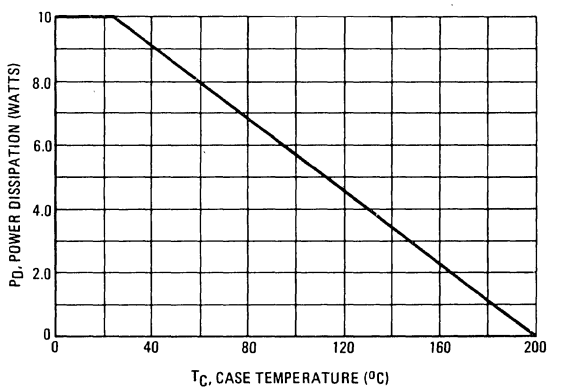


THERMAL CHARACTERISTICS

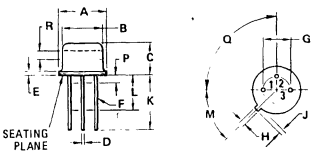
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	17.5	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER-TEMPERATURE DERATING



Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.



STYLE 1:
PIN 1 EMITTER
2. BASE
3 COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

4

* ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1)		–	$V_{CEO(sus)}$			V_{dc}
(I_C = 50 mAdc, I_B = 0)	2N6190, 2N6191			80	–	
	2N6192, 2N6193			100	–	
Collector Cutoff Current		–	I_{CEO}			μAdc
(V_{CE} = 75 Vdc, I_B = 0)	2N6190, 2N6191			–	100	
(V_{CE} = 90 Vdc, I_B = 0)	2N6192, 2N6193			–	100	
Collector Cutoff Current		12	I_{CEX}			μAdc
(V_{CE} = 75 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6190, 2N6191			–	10	
(V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6192, 2N6193			–	10	
(V_{CE} = 75 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6190, 2N6191			–	1.0	mAdc
(V_{CE} = 90 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6192, 2N6193			–	1.0	
Collector Cutoff Current		–	I_{CBO}			μAdc
(V_{CB} = 80 Vdc, I_E = 0)	2N6190, 2N6191			–	10	
(V_{CB} = 100 Vdc, I_E = 0)	2N6192, 2N6193			–	10	
Emitter Cutoff Current		–	I_{EBO}			μAdc
(V_{BE} = 6.0 Vdc, I_C = 0)				–	100	
ON CHARACTERISTICS (1)						
DC Current Gain		8	h_{FE}			–
(I_C = 500 mAdc, V_{CE} = 2.0 Vdc)	2N6190, 2N6192			30	–	
	2N6191, 2N6193			60	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	2N6190, 2N6192			30	120	
	2N6191, 2N6193			60	240	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	2N6190, 2N6192			20	–	
	2N6191, 2N6193			40	–	
Collector-Emitter Saturation Voltage		9,10,11	$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	0.7	
(I_C = 5.0 Adc, I_B = 0.5 Adc)				–	1.2	
Base-Emitter Saturation Voltage		10,11	$V_{BE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)				–	1.2	
(I_C = 5.0 Adc, I_B = 0.5 Adc)				–	1.8	
DYNAMIC CHARACTERISTICS						
Current-Gain-Bandwidth Product (2) (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{Test} = 10 MHz)		–	f_T	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		7	C_{ob}	–	300	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)		7	C_{ib}	–	1250	pF
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 40 Vdc, $V_{BE(off)}$ = 3.0 Vdc, I_C = 2.0 Adc, I_{B1} = 0.2 Adc)	2,3	t_d	–	100	ns
Rise Time			t_r	–	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc, I_{B1} = I_{B2} = 0.2 Adc)	2,6	t_s	–	2.0	μs
Fall Time			t_f	–	200	ns

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
(2) $f_T = |h_{fe}| \cdot f_{Test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

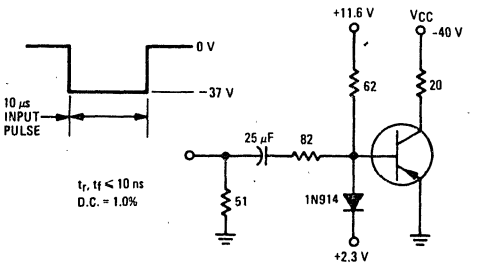


FIGURE 3 – TURN ON TIME

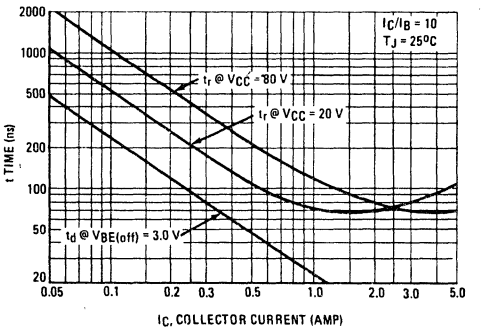
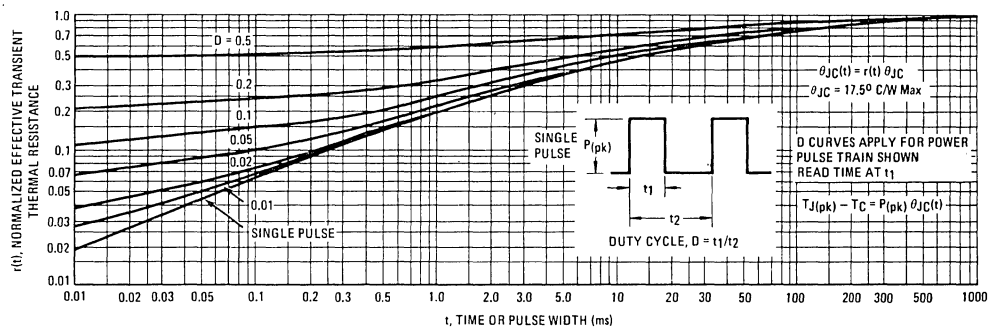


FIGURE 4 – THERMAL RESPONSE



4

FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA

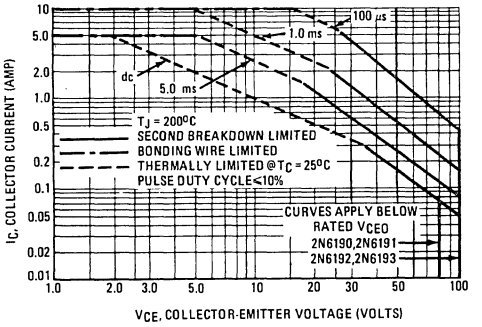


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FIGURE 6 – TURN-OFF TIME

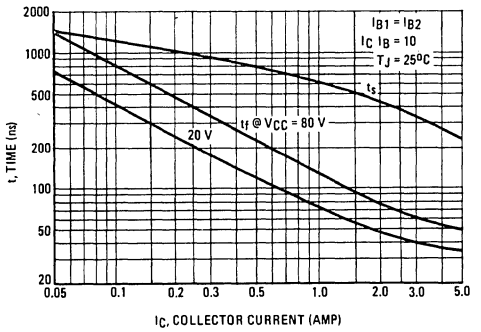


FIGURE 7 – CAPACITANCE versus VOLTAGE

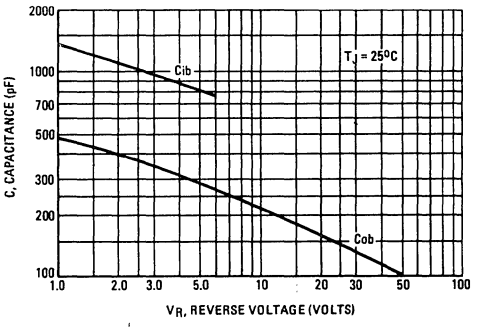


FIGURE 8 – DC CURRENT GAIN

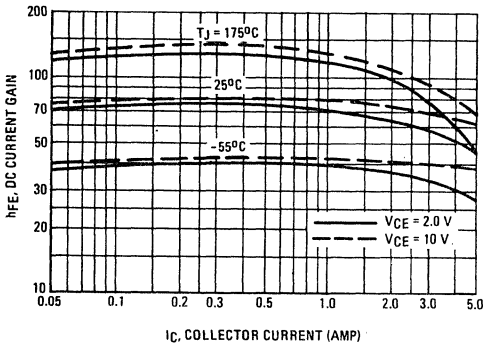


FIGURE 9 – COLLECTOR SATURATION REGION

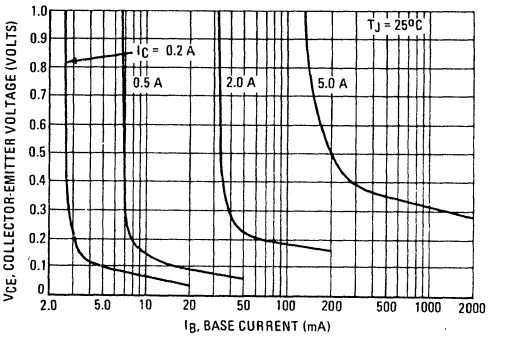


FIGURE 10 – ON VOLTAGES

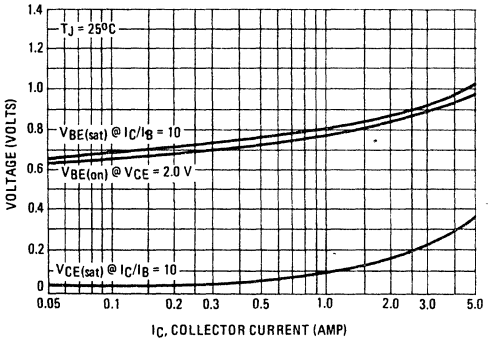


FIGURE 11 – TEMPERATURE COEFFICIENTS

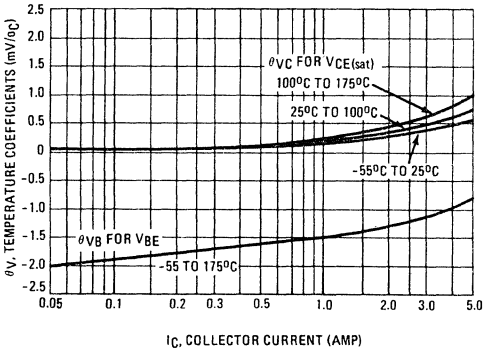


FIGURE 12 – COLLECTOR CUT-OFF REGION

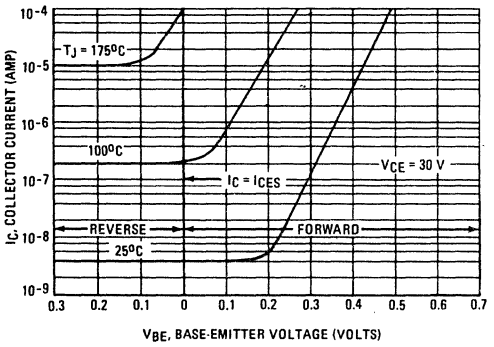
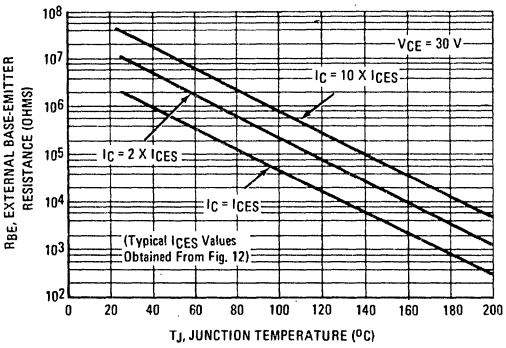


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



2N6211
2N6212
2N6213

MEDIUM-POWER HIGH-VOLTAGE PNP POWER TRANSISTORS

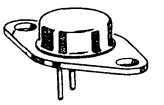
. . . designed for high-speed switching and linear amplifier applications for high-voltage operational amplifiers, switching regulators, converters, inverters, deflection stages and high fidelity amplifiers.

- Collector-Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 225 to 350 Vdc @ I_C = 200 mAdc
- Second Breakdown Collector Current — $I_{s/b}$ = 875 mAdc @ V_{CE} = 40 Vdc
- t_f = 0.6 μs Resistive Fall Time
- Usable DC Current Gain to 2.0 Adc

2 AMPERE POWER TRANSISTORS

PNP SILICON

225–350 VOLTS
35 WATTS



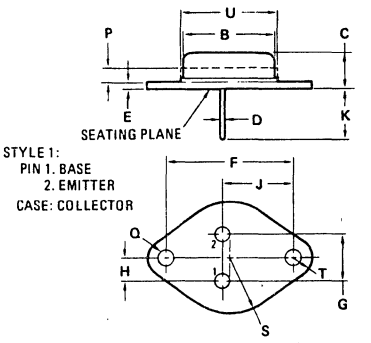
***MAXIMUM RATINGS**

Rating	Symbol	2N6211	2N6212	2N6213	Unit
Collector-Emitter Voltage	V_{CEO}	225	300	350	Vdc
Collector-Base Voltage	V_{CB}	275	350	400	Vdc
Emitter-Base Voltage	V_{EB}	6			Vdc
Collector Current — Continuous Peak	I_C	2 5			Adc
Base Current	I_B	1			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	35 0.2			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W

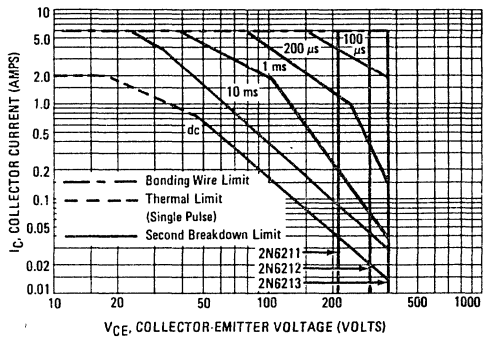
*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.
CASE 80-02
TO-66

FIGURE 1 — FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See Figure 8).

4

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
*Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N6211		225	–	
	2N6212		300	–	
	2N6213		350	–	
*Collector-Emitter Sustaining Voltage		$V_{CEX(sus)}$			Vdc
(I_C = 200 mA, V_{BE} = −1.5 V, L = 10 mH)	2N6211		275	–	
	2N6212		350	–	
	2N6213		400	–	
*Collector-Emitter Sustaining Voltage (1)		$V_{CER(sus)}$			Vdc
(I_C = 200 mA, I_B = 0, R_{BE} = 50 Ω	2N6211		250	–	
	2N6212		325	–	
	2N6213		375	–	
*Emitter-Base Breakdown Voltage (1)		V_{EBO}			Vdc
(I_E = 0.5 mAdc, I_C = 0)	2N6212/13		6.0	–	
(I_E = 1.0 mAdc, I_C = 0)	2N6211		6.0	–	
*Collector Cutoff Current		I_{CEV}			mAdc
(V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 25°C)			–	0.5	
(T_C = 100°C)			–	5.0	
(V_{CE} = 315 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 25°C)			–	0.5	
(T_C = 100°C)			–	5.0	
(V_{CE} = 360 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 25°C)			–	0.5	
(T_C = 100°C)			–	5.0	
Collector Cutoff Current	All Types	I_{CEO}	–	5.0	mAdc
(V_{CE} = 150 Vdc, I_B = 0)					
*Emitter Cutoff Current		I_{EBO}			mAdc
(V_{EB} = 6.0 Vdc, I_C = 0)	2N6211		–	1.0	
	2N6212		–	0.5	
	2N6213		–	0.5	
***ON CHARACTERISTICS (1)**					
DC Current Gain		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 2.8 Vdc)	2N6211		10	100	
(I_C = 1.0 Adc, V_{CE} = 3.2 Vdc)	2N6212		10	100	
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)	2N6213		10	100	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 125 mAdc)	2N6211		–	1.4	
	2N6212		–	1.6	
	2N6213		–	2.0	
Base-Emitter Saturation Voltage	All Types	$V_{BE(sat)}$	–	1.4	Vdc
(I_C = 1.0 Adc, I_B = 125 mAdc)					
DYNAMIC CHARACTERISTICS					
*Current Gain—Bandwidth Product (2) (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 5.0 MHz)		f_T	20	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	220	pF
***SECOND BREAKDOWN**					
*Second Breakdown Collector Current with Base Forward Biased t = 1.0 s (non-repetitive) (V_{CE} = 40 Vdc)		$I_{S/b}$	0.875	–	Adc
***SWITCHING CHARACTERISTICS**					
Rise Time	(V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.125 Adc)	t_r	–	0.6	μs
Storage Time		t_s	–	2.5	μs
Fall Time		t_f	–	0.6	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

FIGURE 2 – SWITCHING TIME TEST CIRCUIT

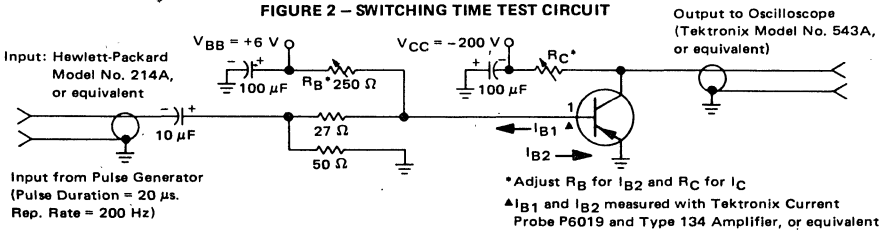


FIGURE 3 – DC CURRENT GAIN

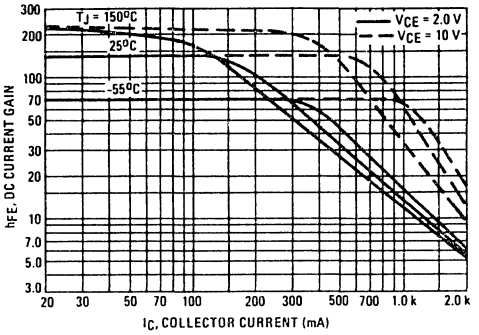


FIGURE 4 – COLLECTOR SATURATION REGION

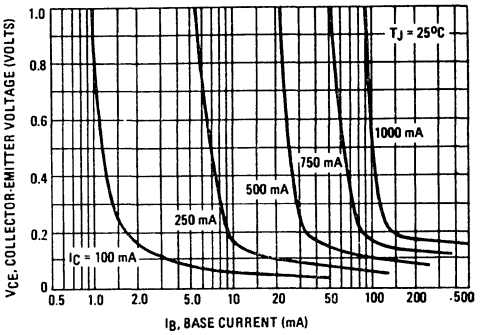


FIGURE 5 – COLLECTOR CUTOFF REGION

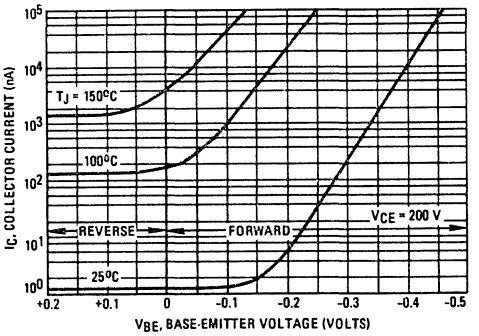


FIGURE 6 – TEMPERATURE COEFFICIENTS

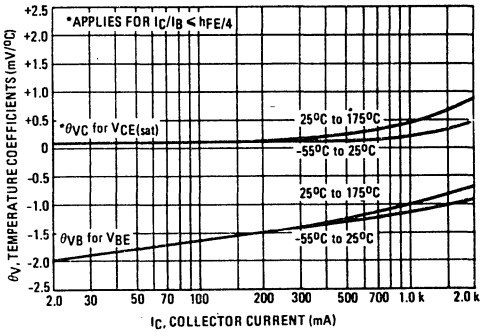


FIGURE 7 – BASE CUTOFF REGION

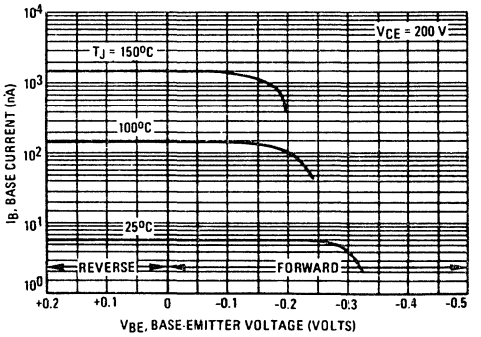


FIGURE 8 – POWER DERATING

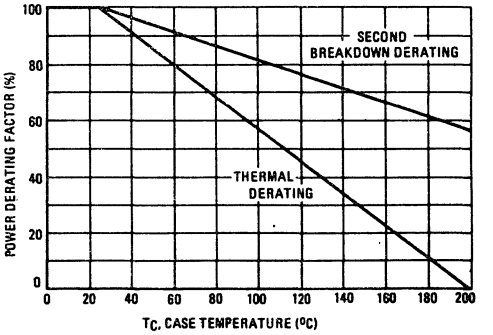


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FIGURE 9 – CURRENT-GAIN–BANDWIDTH PRODUCT

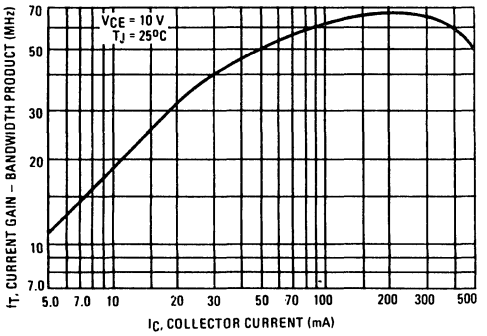


FIGURE 10 – TURN-ON TIME

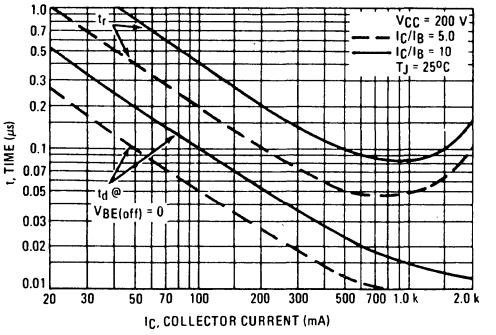


FIGURE 11 – TURN-OFF TIME

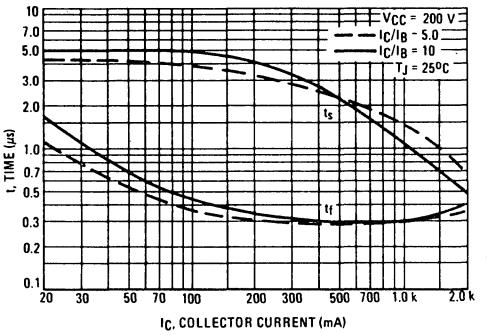


FIGURE 12 – CAPACITANCE

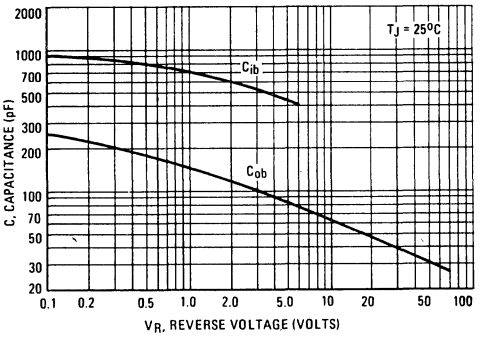
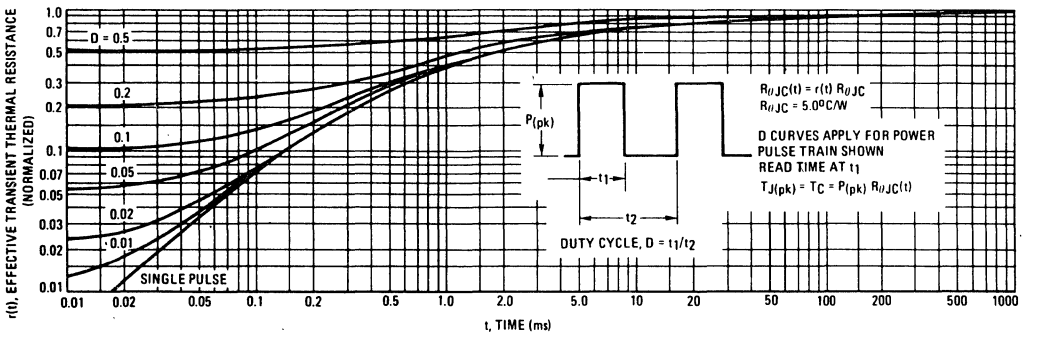


FIGURE 13 – THERMAL RESPONSE



2N6233 (SILICON)
2N6234
2N6235

HIGH VOLTAGE NPN SILICON TRANSISTORS

. . . useful for high-voltage medium power applications such as switching regulators.

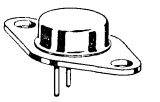
- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 225 Vdc – 2N6233
  275 Vdc – 2N6234
  325 Vdc – 2N6235
- DC Current Gain – h_{FE} = 25 to 125 – I_C = 1.0 Adc
- Low Collector-Emitter Saturation Voltage
  $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 1.0 Adc
- High Frequency Response – f_T = 20 MHz (Min)
- Fast Switching Times @ 1.0 Adc –
  t_r = 0.5 μs (Max)
  t_s = 3.5 μs (Max)
  t_f = 0.5 μs (Max)

5 AMPERE POWER TRANSISTORS

NPN SILICON

225,275,325 VOLTS
50 WATTS

4



*MAXIMUM RATINGS

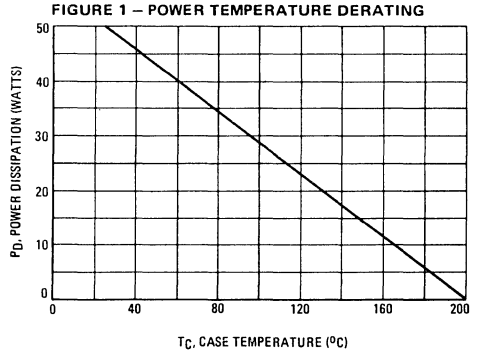
Rating	Symbol	2N6233	2N6234	2N6235	Unit
Collector-Emitter Voltage	V_{CEO}	225	275	325	Vdc
Collector-Base Voltage	V_{CB}	250	300	350	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current – Continuous	I_C	← 5.0 →			Adc
Peak		← 10 →			
Base Current	I_B	← 2.0 →			Adc
Total Device Dissipation @ T_C = 25°C	P_D	← 50 →			Watts
Derate above 25°C		← 0.286 →			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200			°C

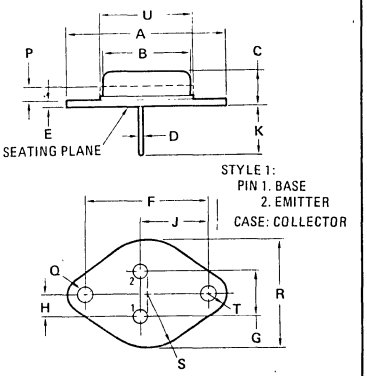
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.5	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER TEMPERATURE DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

4

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

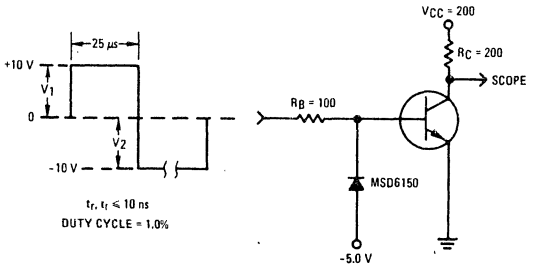
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 20 mAdc, I_B = 0)	2N6233		225	–	
	2N6234		275	–	
	2N6235		325	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 225, I_B = 0)	2N6233		–	1.0	
(V_{CE} = 275, I_B = 0)	2N6234		–	1.0	
(V_{CE} = 325, I_B = 0)	2N6235		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6233		–	1.0	
(V_{CE} = 300 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6234		–	1.0	
(V_{CE} = 350 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6235		–	1.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 250 Vdc, I_E = 0)	2N6233		–	0.1	
(V_{CB} = 300 Vdc, I_E = 0)	2N6234		–	0.1	
(V_{CB} = 350 Vdc, I_E = 0)	2N6235		–	0.1	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 6.0 Vdc, I_C = 0)			–	0.1	
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.1 Adc, V_{CE} = 5.0 Vdc)			25	–	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)			25	125	
(I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)			10	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)			–	0.5	
(I_C = 5.0 Adc, I_B = 1.0 Adc)			–	2.5	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)			–	1.0	
(I_C = 5.0 Adc, I_B = 1.0 Adc)			–	2.0	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)			–	1.0	
DYNAMIC CHARACTERISTICS					
Current-Gain Bandwidth Product (2)		f_T			MHz
(I_C = 0.25 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)			20	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)			–	250	
SWITCHING CHARACTERISTICS					
Rise Time		t_r			μs
(V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_B = 0.1 Adc)			–	0.5	
Storage Time		t_s			μs
(V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc)			–	3.5	
Fall Time		t_f			μs
(V_{CC} = 200 Vdc, I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc)			–	0.5	

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



FOR INFORMATION ON FIGURES 3 and 6 R_B AND R_C ARE VARIED TO OBTAIN DESIRED CURRENT LEVELS; D_1 DISCONNECTED AND V_2 REDUCED TO 5 VOLTS FOR t_d MEASUREMENT.

FIGURE 3 – TURN-ON TIME

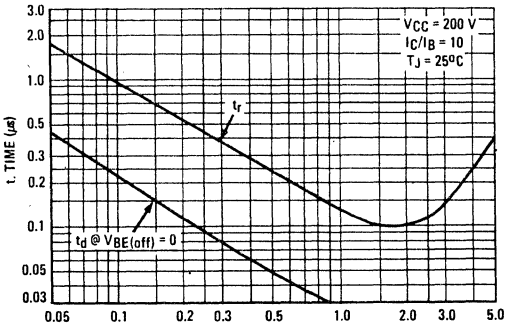


FIGURE 4 – THERMAL RESPONSE

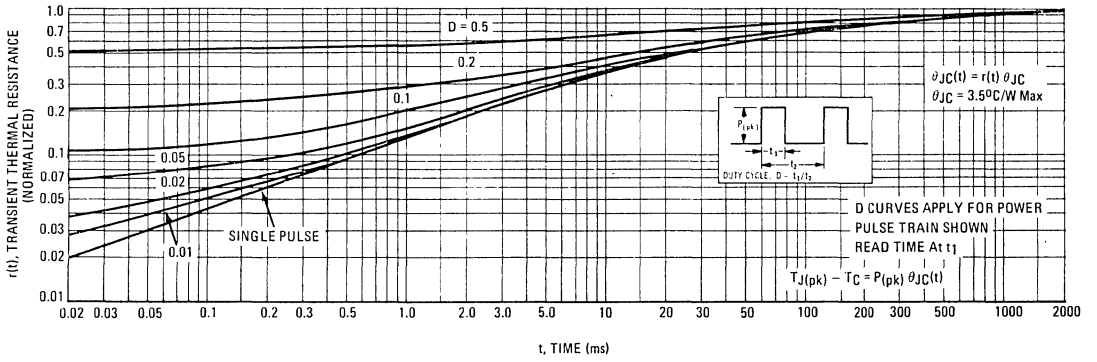


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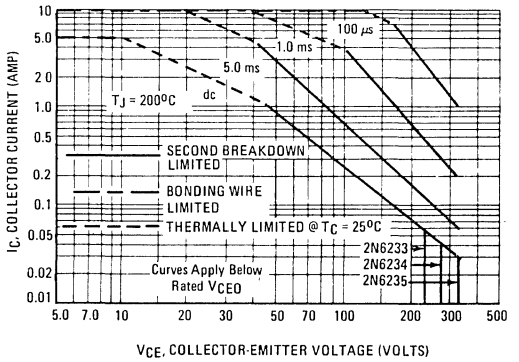
FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

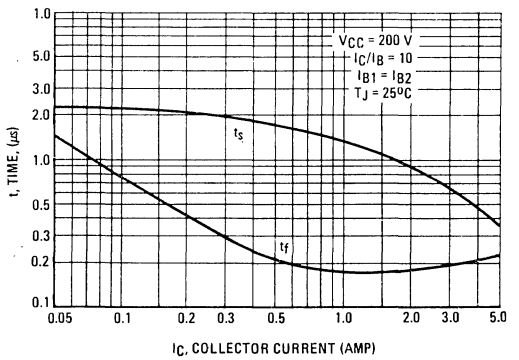


FIGURE 7 – CAPACITANCES

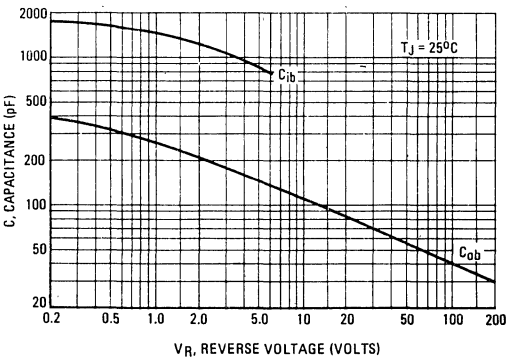


FIGURE 8 – DC CURRENT GAIN

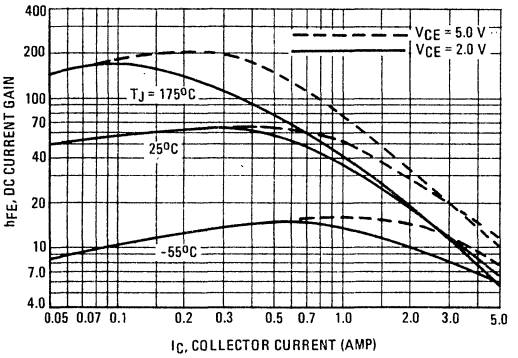


FIGURE 9 – COLLECTOR SATURATION REGION

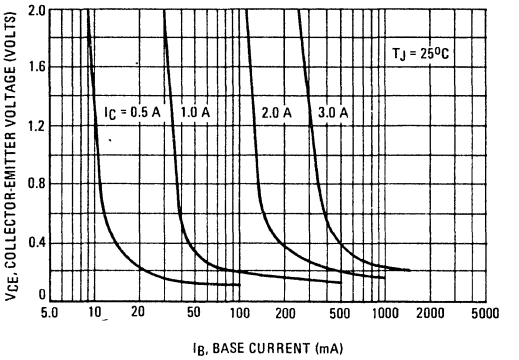


FIGURE 10 – "ON" VOLTAGES

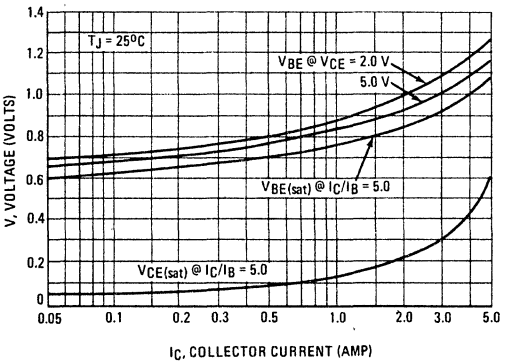


FIGURE 11 – TEMPERATURE COEFFICIENTS

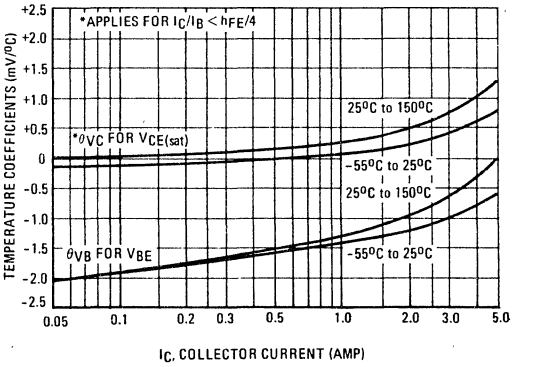


FIGURE 12 – COLLECTOR CUT-OFF REGION

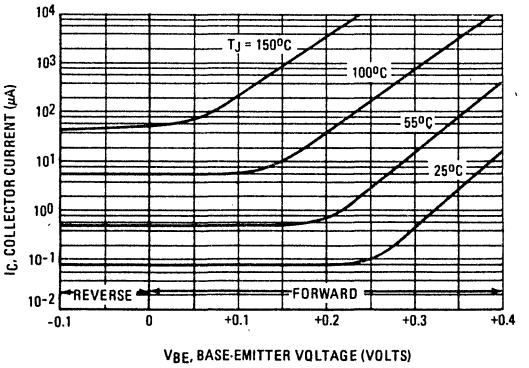
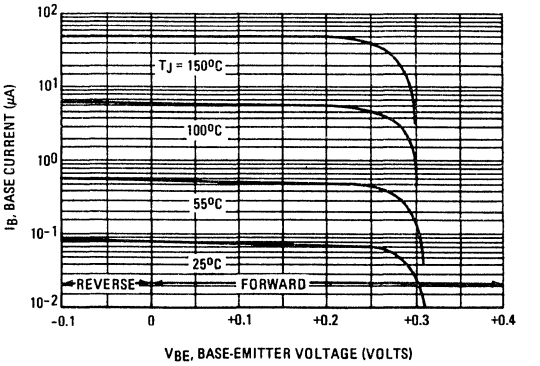


FIGURE 13 – BASE CUT-OFF REGION



2N6249
2N6250
2N6251

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

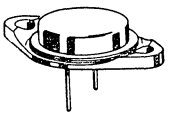
. . . designed for high voltage inverters, switching regulators and line operated amplifier applications. Especially well suited for switching power supply applications.

- High Voltage Breakdown Rating
- Low Saturation Voltages
- Fast Switching Capability
- High $E_{S/b}$ Energy Handling Capability

15 AMPERE POWER TRANSISTORS

NPN SILICON

200, 275, 350 VOLTS
175 WATTS



MAXIMUM RATINGS

Rating	Symbol	2N6249	2N6250	2N6251	Unit
*Collector-Emitter Voltage	$V_{CEO(sus)}$	200	275	350	Vdc
*Collector-Emitter Voltage	$V_{CER(sus)}$	225	300	375	Vdc
*Collector-Base Voltage	V_{CB}	300	375	450	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current — Continuous**	I_C	← 15 →			Adc
— Peak	I_{CM}	← 30 →			
Base Current — Continuous*	I_B	← 10 →			Adc
— Peak	I_{BM}	← 20 →			
Emitter Current — Continuous	I_E	← 25 →			Adc
— Peak	I_{EM}	← 50 →			
Total Power Dissipation @ $T_C = 25^oC$	P_D	← 175 →			Watts
@ $T_C = 100^oC$		← 100 →			
Derate above 25^oC*		← 1.0 →			$W/^oC$
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			^oC

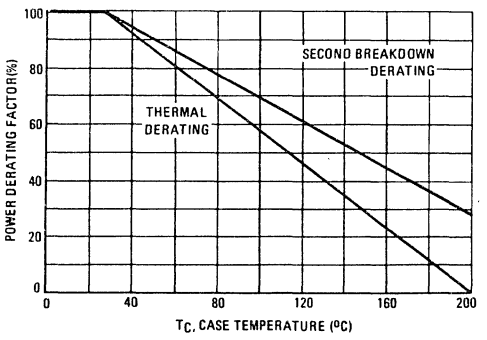
THERMAL CHARACTERISTICS

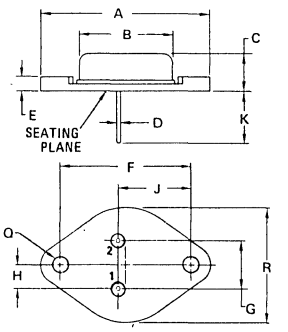
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	^oC

*Indicates JEDEC Registered Data.

**JEDEC Registered Value is 10 A, Motorola Guaranteed Value is 15 A.

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-03
TO-3

4

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mA, I_B = 0)	2N6249		200	–	
	2N6250		275	–	
	2N6251		350	–	
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CER(sus)}$			Vdc
(I_C = 200 mA,	2N6249		225	–	
	2N6250		300	–	
	2N6251		375	–	
Collector Cutoff Current		I_{CEV}			mAdc
(V_{CE} = Rated V_{CER}, $V_{BE(off)}$ = 1.5 Vdc)			–	5.0	
(V_{CE} = Rated V_{CER}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)			–	10	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 150 Vdc, I_B = 0)	2N6249		–	5.0	
(V_{CE} = 225 Vdc, I_B = 0)	2N6250		–	5.0	
(V_{CE} = 300 Vdc, I_B = 0)	2N6251		–	5.0	
Emitter Cutoff Current		I_{EBO}	–	1.0	mAdc
(V_{EB} = 6.0 Vdc, I_C = 0)					
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased t = 1.0 s (non-repetitive)	(V_{CE} = 30 V)	$I_{S/b}$	5.8	–	Vdc
	(V_{CE} = 100 V)		0.3	–	
Second Breakdown Energy with base reverse biased (Table 1)		$E_{S/b}$	2.5	–	mJ
(I_C = 10 A, $V_{BE(off)}$ = 4.0 Vdc, L = 50 μH)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)	2N6249		10	50	
	2N6250		8.0	50	
	2N6251		6.0	50	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)	2N6249		–	1.5	
(I_C = 10 Adc, I_B = 1.25 Adc	2N6250		–	1.5	
(I_C = 10 Adc, I_B = 1.67 Adc)	2N6251		–	1.5	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc	2N6249		–	2.5	
(I_C = 10 Adc, I_B = 1.25 Adc)	2N6250		–	2.5	
(I_C = 10 Adc, I_B = 1.67 Adc)	2N6251		–	2.5	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	2.5	–	MHz
(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)					
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Rise Time	(V_{CC} = 200 Vdc, I_C = 10 A, Duty Cycle ≤ 2.0%, t_p = 100 μs)	t_r	–	2.0	μs
Storage Time	(I_{B1} = I_{B2} = 1.0 Adc) 2N6249 (I_{B1} = I_{B2} = 1.25 Adc) 2N6250 (I_{B1} = I_{B2} = 1.67 Adc) 2N6251	t_s	–	3.5	μs
Fall Time		t_f	–	1.0	μs

* Indicates JEDEC Registered Data.
(1) Measured on a curve tracer (60 Hz full-wave rectified sine wave).

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	$V_{CER(sus)}$	$E_{S/b}$	RESISTIVE SWITCHING
INPUT CONDITIONS	+6.0 V, 39, 0, 1, 2	+6.0 V, 39, 51, 0, 1, 2	I_{B1} = 2.0 A, 50, +10 V, 0, 4 V, 1, 2	+15 V, 50 µF, 2N4231, 51, 51, 4.7, 0.02 µF, 1, 2
CIRCUIT VALUES	L_{coil} = 42 mH R_{coil} = 0.7 Ω, f_o = 60 Hz V_{CC} = 0 to 50 V	L_{coil} = 14 mH R_{coil} = 0.05 Ω V_{CC} = 0 to 50 V f_o = 60 Hz	L_{coil} = 50 µH V_{CC} = 11.5 V R_{coil} = 0.2 Ω	V_{CC} = 200 V R_L = 20 Ω
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT: TUT, 1N4937, R_{Coil}, L_{Coil}, V_{CL}, V_{CC}, R_S 0.1, 1, 2 OUTPUT WAVEFORMS: I_C, $I_{C(pk)}$, t_1, t_f, V_{CE}, t t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$			RESISTIVE TEST CIRCUIT: +200 V, 20, DC Current Probe, TUT, 1, 3, 2, 25, -6.0 V

NOTE Set $I_{C(pk)}$ to Obtain I_C = 200 mA at $V_{CEO(sus)}$ Equal to Rated Value
Adjust V_{Clamp} Voltage for $V_{CEO(sus)}$ Rated Value.

FIGURE 2 – THERMAL RESPONSE

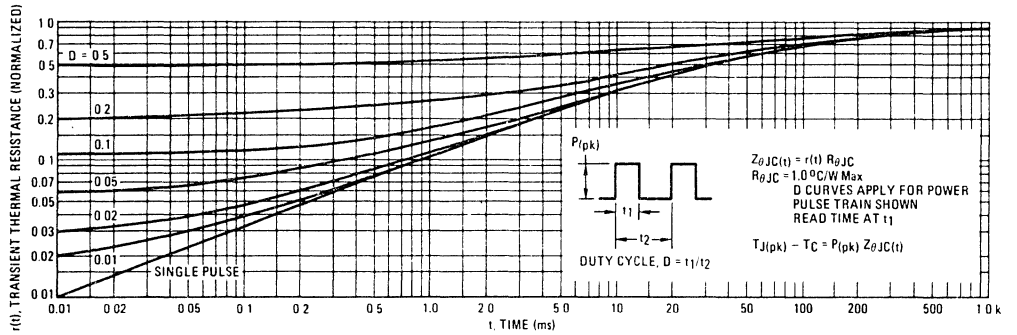
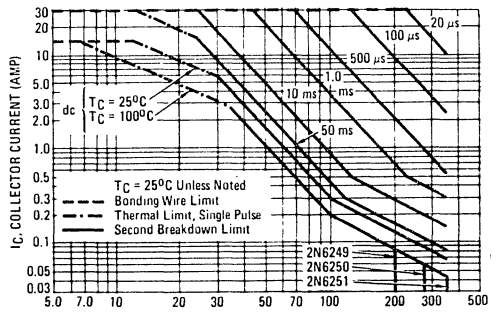


FIGURE 3 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on T_C = 25°C, $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 3 may be found at any case temperature by using the appropriate curve on Figure 1.

$T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

DC CHARACTERISTICS

FIGURE 4 – DC CURRENT GAIN

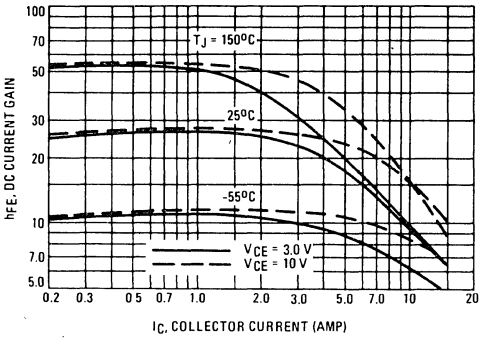


FIGURE 5 – COLLECTOR SATURATION REGION

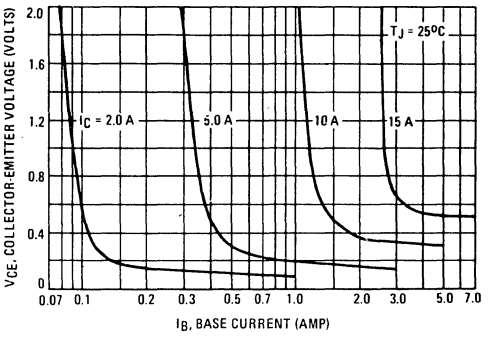


FIGURE 6 – "ON" VOLTAGE

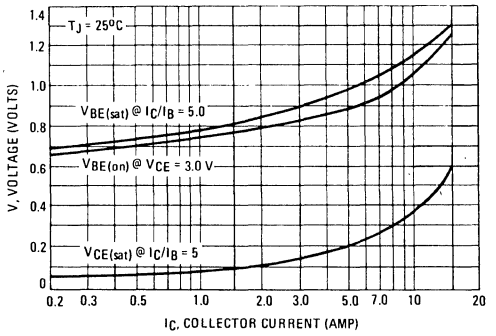
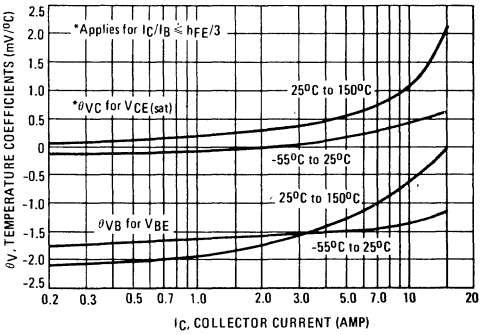


FIGURE 7 – TEMPERATURE COEFFICIENTS



RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

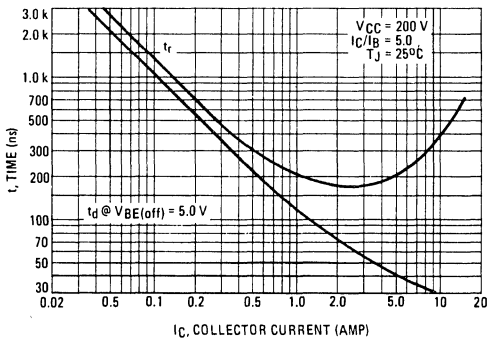
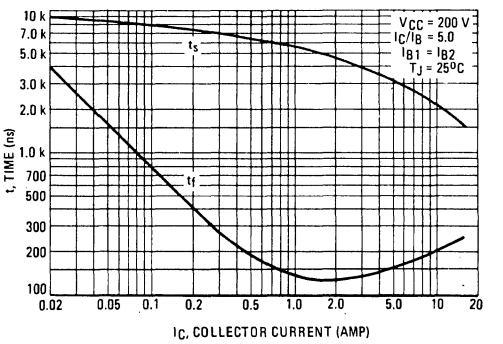


FIGURE 9 – TURN-OFF TIME



2N6274 (SILICON) thru 2N6277

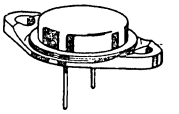
HIGH-POWER NPN SILICON TRANSISTORS

. . . designed for use in industrial-military power amplifer and switching circuit applications.

- High Collector Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc (Min) – 2N6274
  = 120 Vdc (Min) – 2N6275
  = 140 Vdc (Min) – 2N6276
  = 150 Vdc (Min) – 2N6277
- High DC Current Gain –
  h_{FE} = 30-120 @ I_C = 20 Adc
  = 10 (Min) @ I_C = 50 Adc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 20 Adc
- Fast Switching Times @ I_C = 20 Adc
  t_r = 0.35 μs (Max)
  t_s = 0.8 μs (Max
  t_f = 0.25 μs (Max)
- Complement to 2N6377-79

50 AMPERE
POWER TRANSISTORS
NPN SILICON

100, 120, 140, 150 VOLTS
250 WATTS



4

*MAXIMUM RATINGS

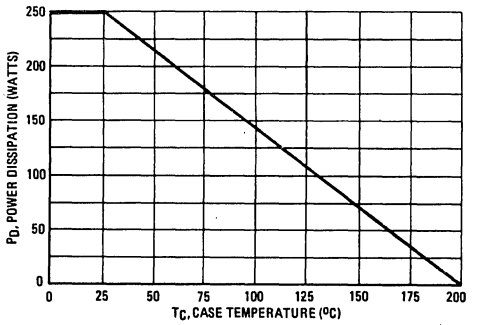
Rating	Symbol	2N6274	2N6275	2N6276	2N6277	Unit
Collector-Base Voltage	V_{CB}	120	140	160	180	Vdc
Collector-Emitter Voltage	V_{CEO}	100	120	140	150	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →				Vdc
Collector Current – Continuous Peak	I_C	← 50 → ← 100 →				Adc
Base Current	I_B	← 20 →				Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 250 → ← 1.43 →				Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	← -65 to +200 →				°C

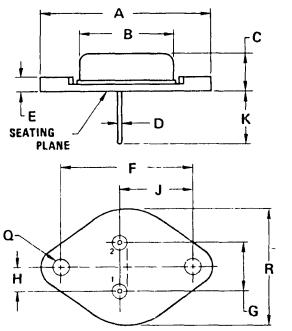
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

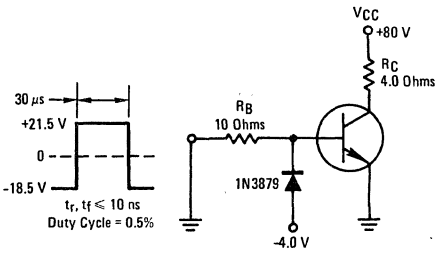
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N6274		100	–	
	2N6275		120	–	
	2N6276		140	–	
	2N6277		150	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 50 Vdc, I_B = 0)	2N6274		–	50	
(V_{CE} = 60 Vdc, I_B = 0)	2N6275		–	50	
(V_{CE} = 70 Vdc, I_B = 0)	2N6276		–	50	
(V_{CE} = 75 Vdc, I_B = 0)	2N6277		–	50	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc)			--	10	μAdc
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)			–	1.0	mAdc
Emitter Cutoff Current		I_{EBO}	–	100	μAdc
(V_{BE} = 6.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			50	–	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)			30	120	
(I_C = 50 Adc, V_{CE} = 4.0 Vdc)			10	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)			–	1.0	
(I_C = 50 Adc, I_B = 10 Adc)			–	3.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)			–	1.8	
(I_C = 50 Adc, I_B = 10 Adc)			–	3.5	
Base-Emitter On Voltage		$V_{BE(on)}$	–	1.8	Vdc
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (2)		f_T	30	–	MHz
(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)					
Output Capacitance		C_{ob}	–	600	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)					
SWITCHING CHARACTERISTICS					
Rise Time		t_r	–	0.35	μs
(V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = 2.0 Adc, $V_{BE(off)}$ = 5.0 Vdc)					
Storage Time		t_s	–	0.80	μs
(V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)					
Fall Time		t_f	–	0.25	μs
(V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)					

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \cdot f_{test}$.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



Note: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 – TURN-ON TIME

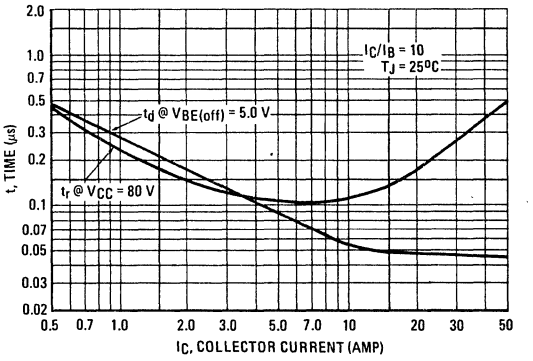
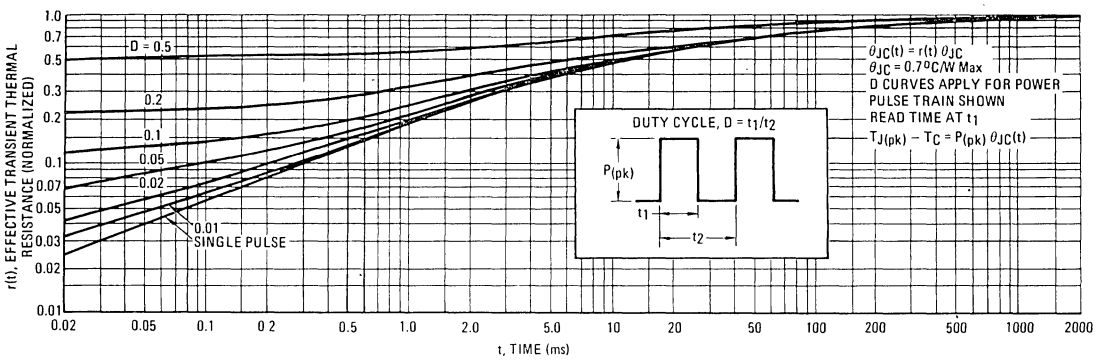
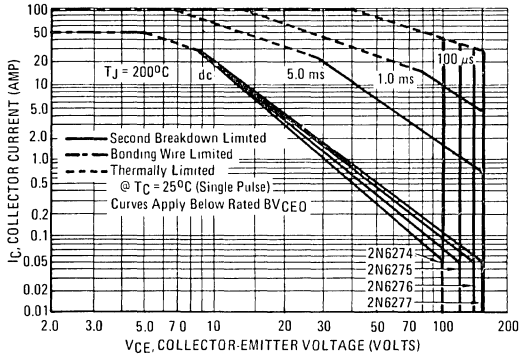


FIGURE 4 – THERMAL RESPONSE



4

FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; *i.e.*, the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

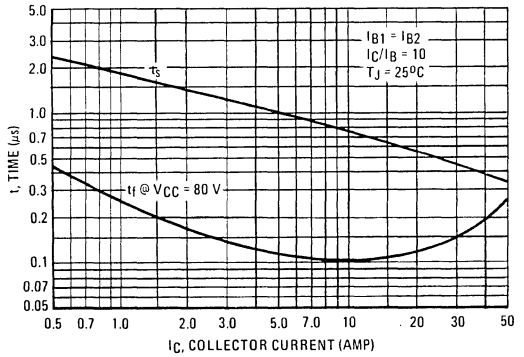


FIGURE 7 – CAPACITANCE

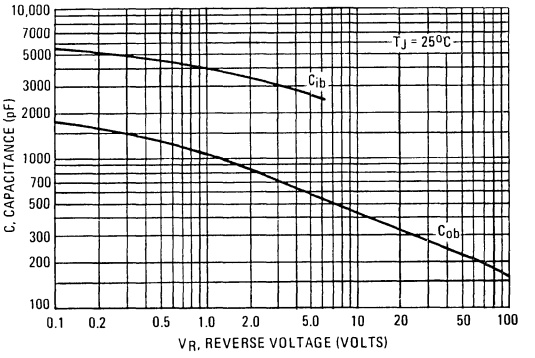


FIGURE 8 – DC CURRENT GAIN

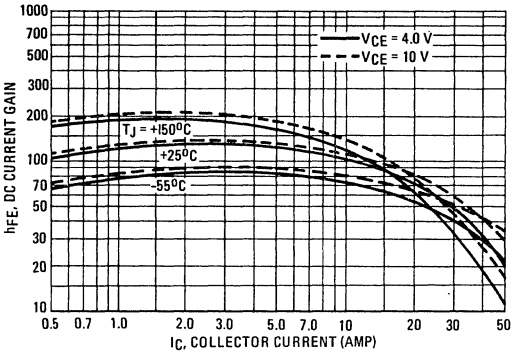


FIGURE 9 – COLLECTOR SATURATION REGION

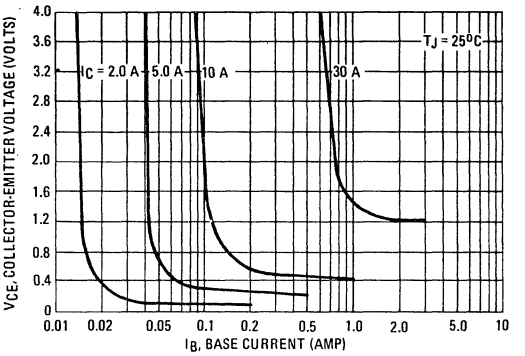


FIGURE 10 – "ON" VOLTAGES

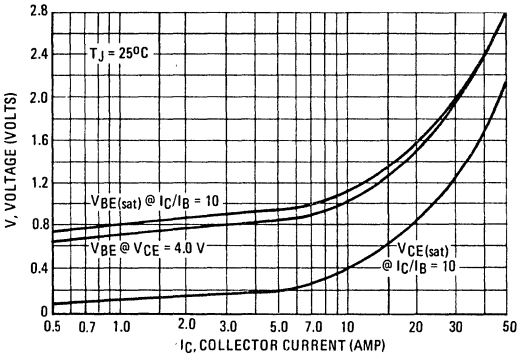


FIGURE 11 – TEMPERATURE COEFFICIENTS

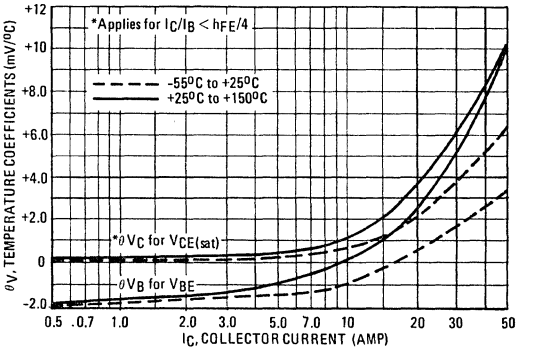


FIGURE 12 – COLLECTOR CUT-OFF REGION

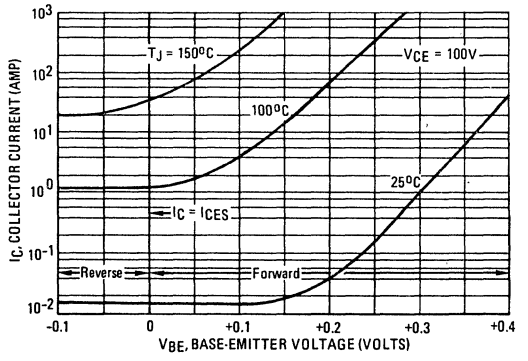
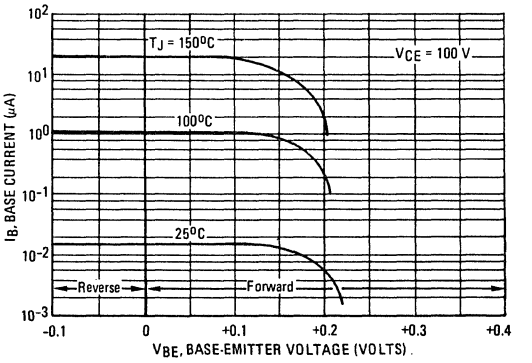


FIGURE 13 – BASE CUT-OFF REGION



2N6282 thru 2N6284 NPN (SILICON)
2N6285 thru 2N6287 PNP

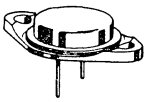
DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier and low-frequency switching applications.

- High DC Current Gain @ I_C = 10 Adc –
  h_{FE} = 2400 (Typ) – 2N6282, 2N6283, 2N6284
  = 4000 (Typ) – 2N6285, 2N6286, 2N6287
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 60 Vdc (Min) – 2N6282, 2N6285
  = 80 Vdc (Min) – 2N6283, 2N6286
  = 100 Vdc (Min) – 2N6284, 2N6287
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

DARLINGTON 20 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60, 80, 100 VOLTS
160 WATTS



*MAXIMUM RATINGS

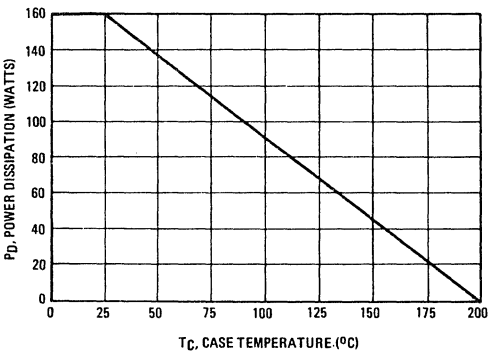
Rating	Symbol	2N6282 2N6285	2N6283 2N6286	2N6284 2N6287	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous Peak	I_C	20 40			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	160 0.915			Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200			°C

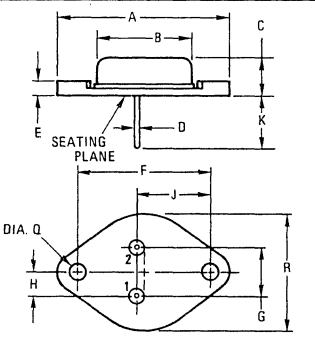
*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.09	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

4

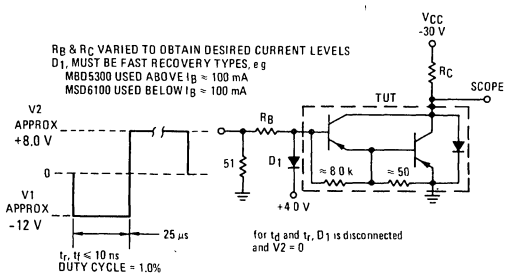
*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage		$V_{CEO(sus)}$			Vdc
(I_C = 0.1 Adc, I_B = 0)	2N6282, 2N6285		60	–	
	2N6283, 2N6286		80	–	
	2N6284, 2N6287		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N6282, 2N6285		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N6283, 2N6286		–	1.0	
(V_{CE} = 50 Vdc, I_B = 0)	2N6284, 2N6287		–	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)			–	0.5	
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	5.0	
Emitter Cutoff Current		I_{EBO}	–	2.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)			750	18,000	
(I_C = 20 Adc, V_{CE} = 3.0 Vdc)			100	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 40 mAdc)			–	2.0	
(I_C = 20 Adc, I_B = 200 mAdc)			–	3.0	
Base-Emitter On Voltage		$V_{BE(on)}$	–	2.8	Vdc
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)					
Base-Emitter Saturation Voltage		$V_{BE(sat)}$	–	4.0	Vdc
(I_C = 20 Adc, I_B = 200 mAdc)					
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio		$\lvert h_{fe} \rvert$	4.0	–	MHz
(I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)					
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6282, 83, 84		–	400	
	2N6285, 86, 87		–	600	
Small-Signal Current Gain		h_{fe}	300	–	–
(I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)					

*Indicates JEDEC Registered Data.

(1) Pulse test: Pulse Width = 300 μs, Duty Cycle = 2%

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



For NPN test circuit reverse diode and voltage polarities.

FIGURE 3 – SWITCHING TIMES

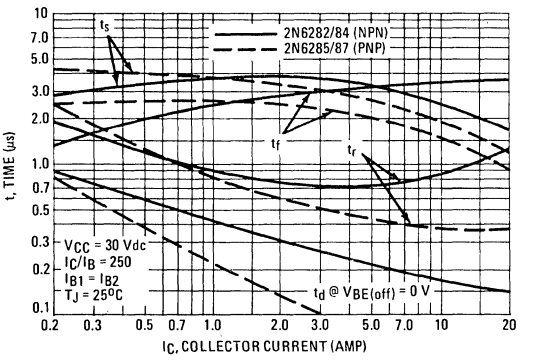
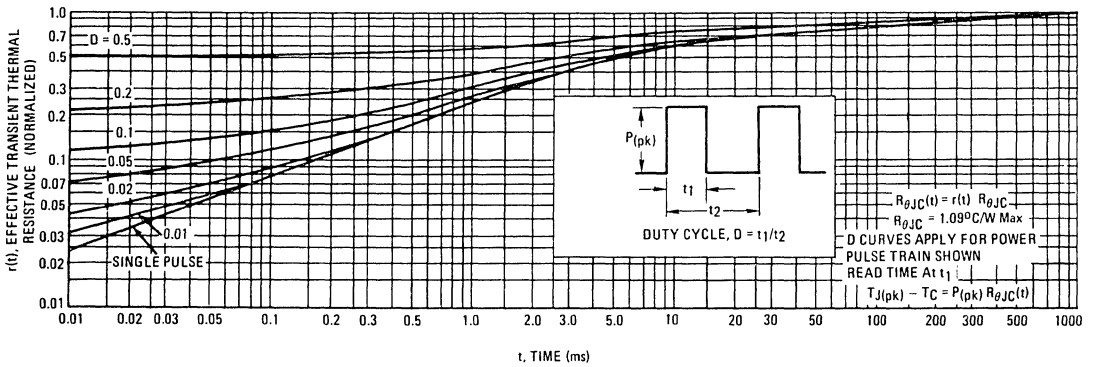


FIGURE 4 – THERMAL RESPONSE



4

ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – 2N6282, 2N6285

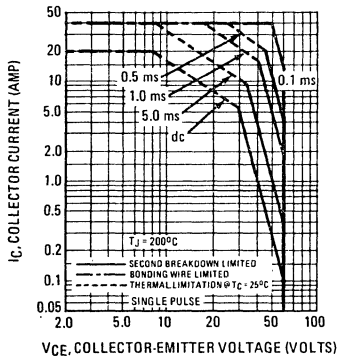


FIGURE 6 – 2N6283, 2N6286

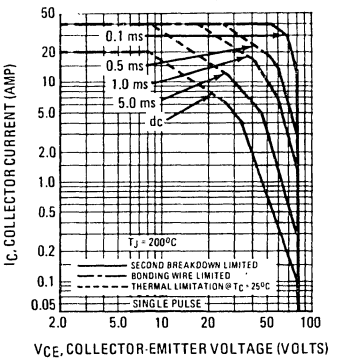
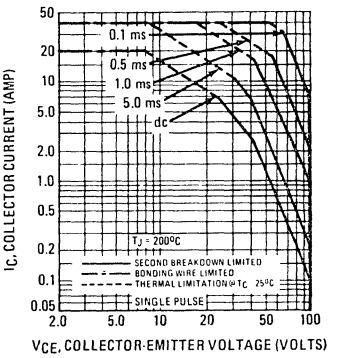


FIGURE 7 – 2N6284, 2N6287



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e. the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, 6 and 7 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 8 – SMALL-SIGNAL CURRENT GAIN

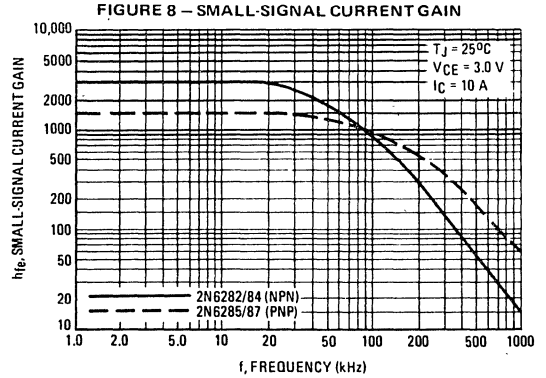
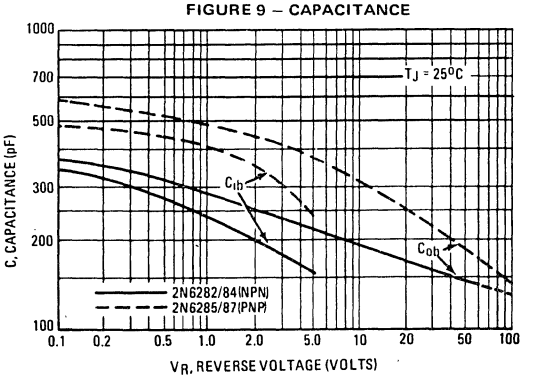


FIGURE 9 – CAPACITANCE



4

NPN
2N6282, 2N6283, 2N6284

PNP
2N6285, 2N6286, 2N6287

FIGURE 10 – DC CURRENT GAIN

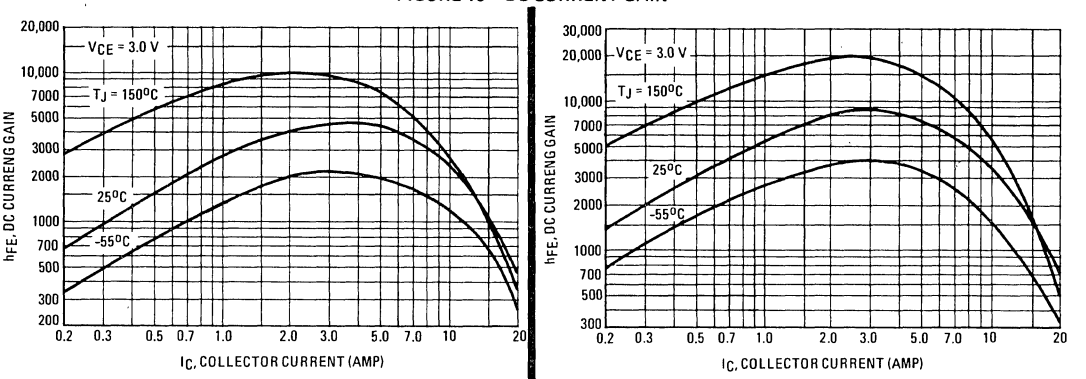


FIGURE 11 – COLLECTOR SATURATION REGION

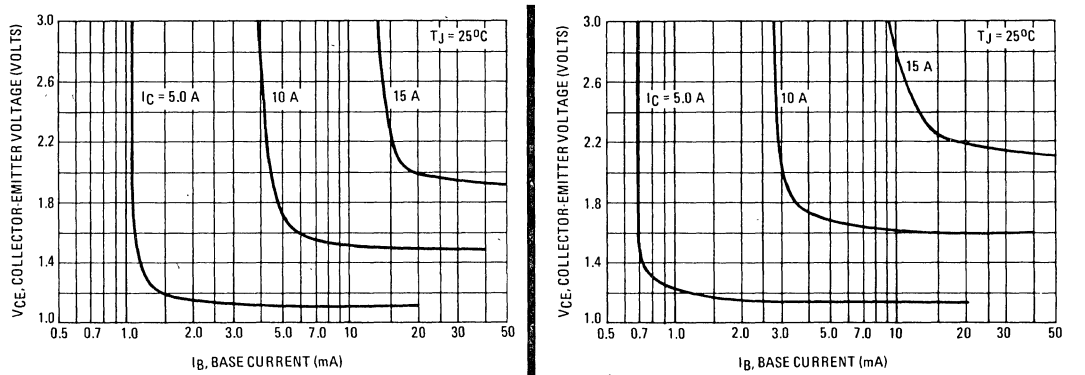
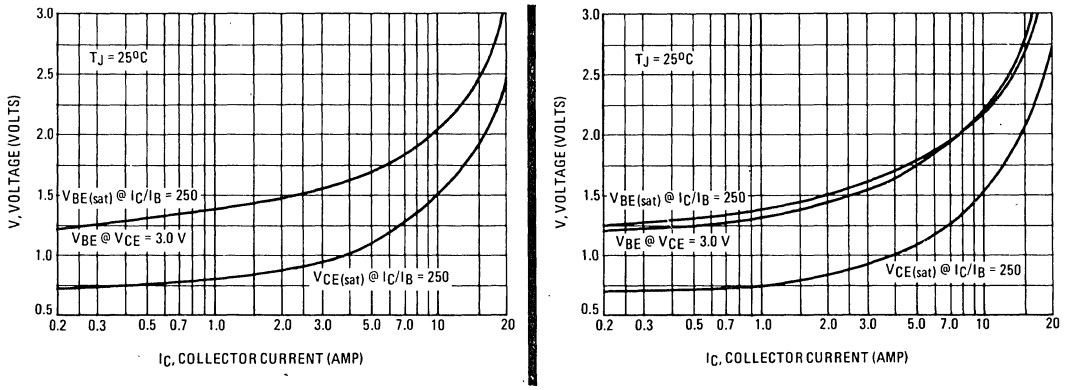


FIGURE 12 – "ON" VOLTAGES



NPN 2N6282, 2N6283, 2N6284	PNP 2N6285, 2N6286, 2N6287

FIGURE 13 – TEMPERATURE COEFFICIENTS

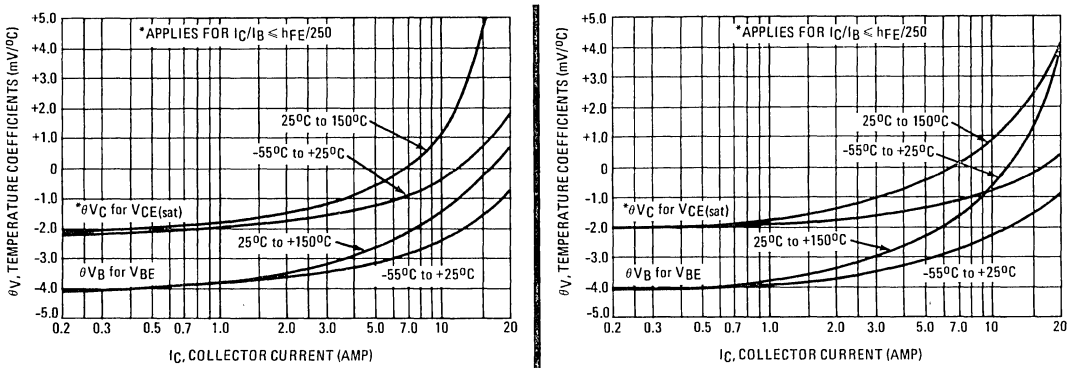


FIGURE 14 – COLLECTOR CUTOFF REGION

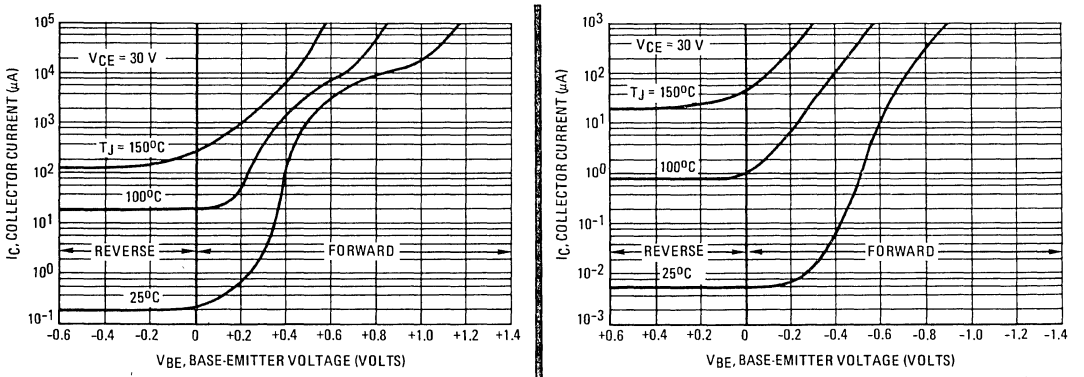
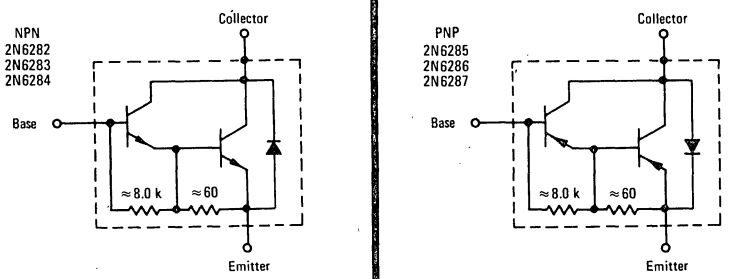


FIGURE 15 – DARLINGTON SCHEMATIC



2N6294, 2N6295 NPN (SILICON)
2N6296, 2N6297 PNP

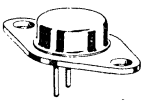
4

DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed for general-purpose amplifier, low-frequency switching and hammer driver applications.

- High DC Current Gain – h_{FE} = 3000 (Typ) @ I_C = 2.0 Adc
- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 2.0 Adc
- Collector-Emitter Sustaining Voltage $V_{CEO(sus)}$ = 60 Vdc (Min) – 2N6294, 2N6296 = 80 Vdc (Min) – 2N6295, 2N6297
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

4 AMPERES
DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS
60, 80 VOLTS
50 WATTS



*MAXIMUM RATINGS

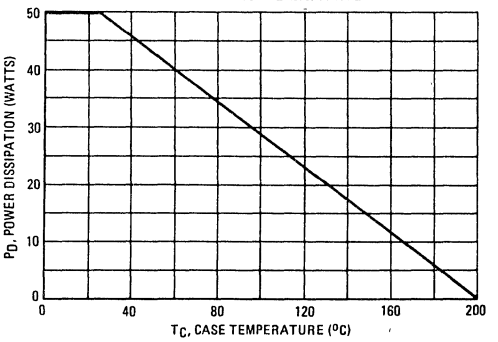
Rating	Symbol	2N6294 2N6296	2N6295 2N6297	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous Peak	I_C	4.0 8.0		Adc
Base Current	I_B	80		mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.286		Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +200		°C

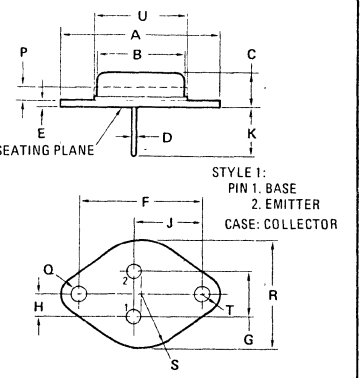
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

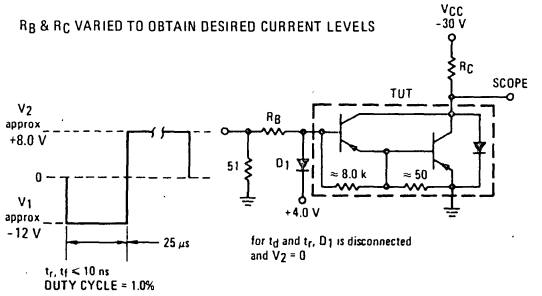
CASE 80-02
TO-66

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 50 mAdc, I_B = 0)	2N6294, 2N6296	$V_{CEO(sus)}$	60	–	Vdc
	2N6295, 2N6297		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N6294, 2N6296		–	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	2N6295, 2N6297		–	0.5	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc)	2N6294, 2N6295		–	0.5	
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)	2N6296, 2N6297		–	0.5	
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6294, 2N6295		–	5.0	
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6296, 2N6297		–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)			750	18000	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			100	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 8.0 mAdc)			–	2.0	
(I_C = 4.0 Adc, I_B = 40 mAdc)			–	3.0	
Base-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 40 mAdc)		$V_{BE(sat)}$	–	4.0	Vdc
Base-Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6294, 2N6295	C_{ob}	–	120	pF
	2N6296, 2N6297		–	200	
Small-Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	–	–

*Indicates JEDEC Registered Data

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



For NPN test circuit, reverse all polarities.

FIGURE 3 – SWITCHING TIMES

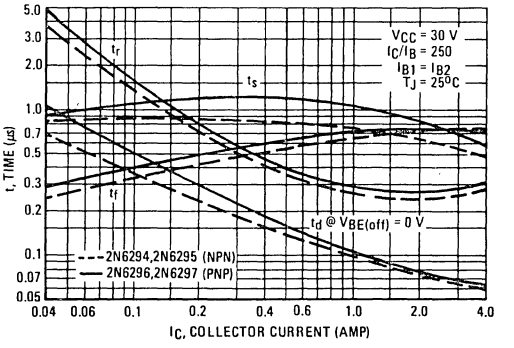


FIGURE 4 – THERMAL RESPONSE

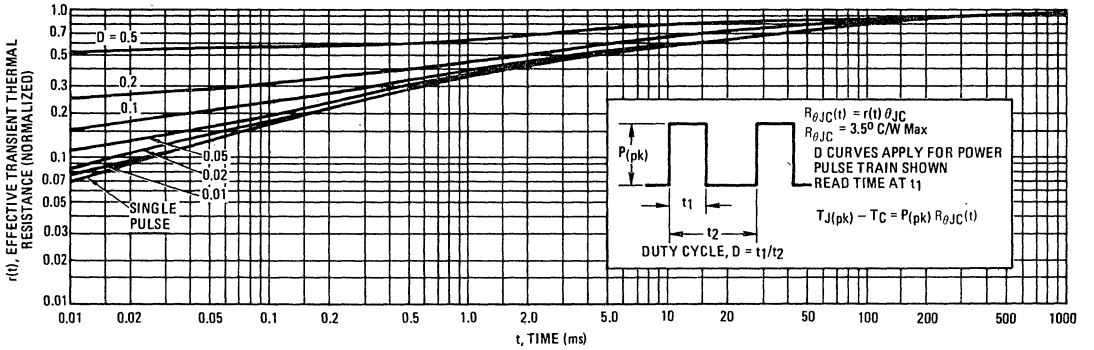
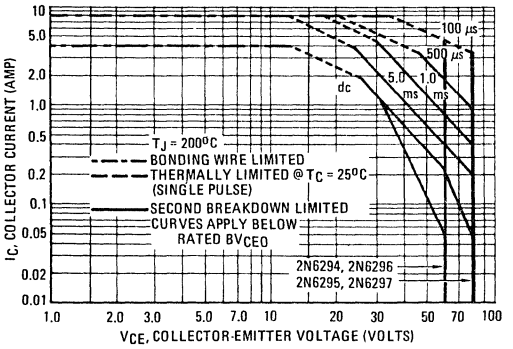


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

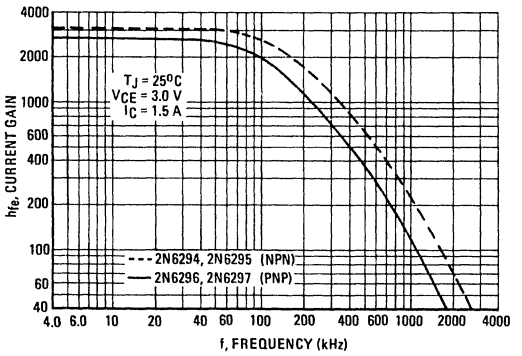
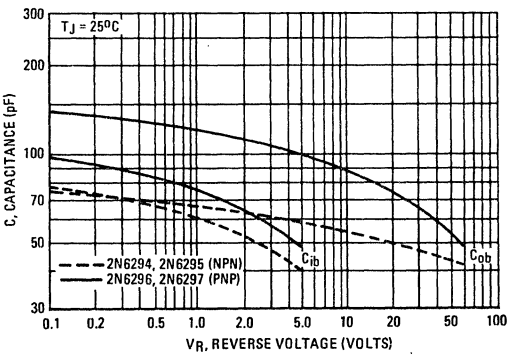


FIGURE 7 – CAPACITANCE



NPN
2N6294, 2N6295

PNP
2N6296, 2N6297

FIGURE 8 – DC CURRENT GAIN

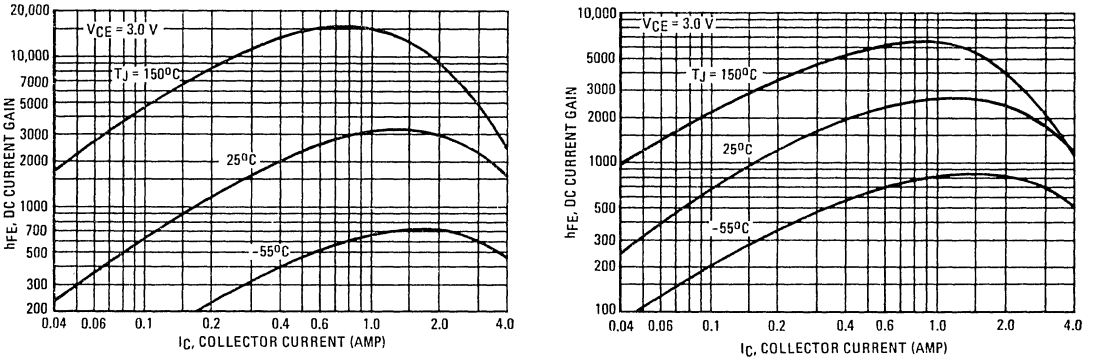


FIGURE 9 – COLLECTOR SATURATION REGION

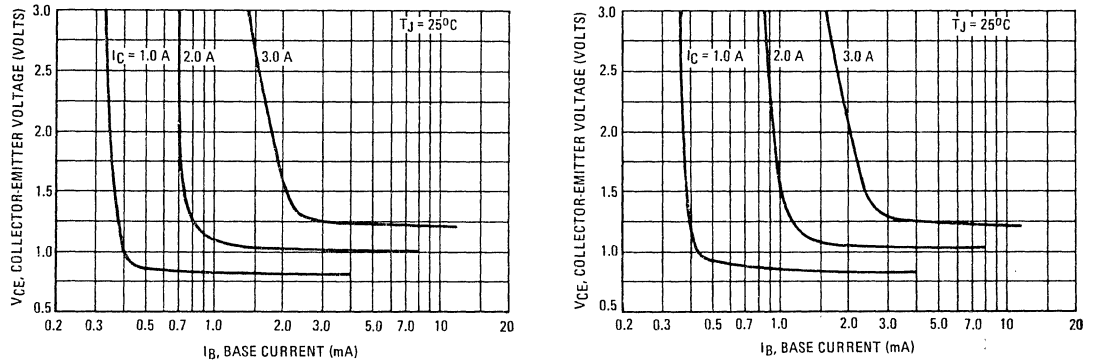
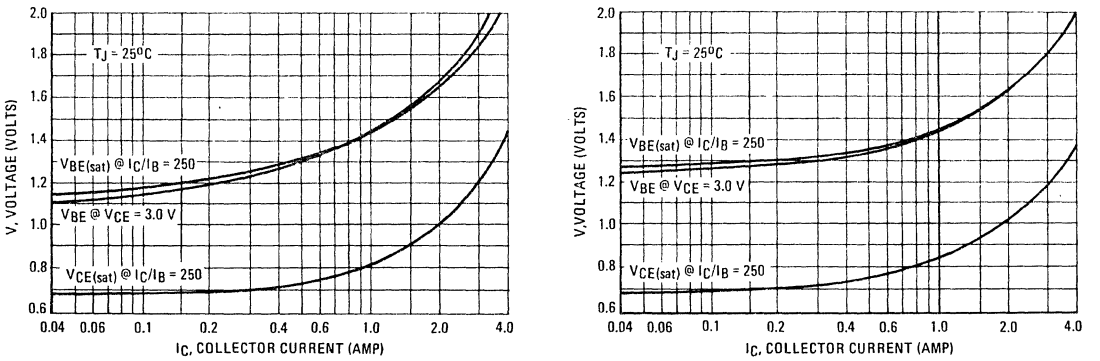


FIGURE 10 – "ON" VOLTAGES



NPN
2N6294, 2N6295

PNP
2N6296, 2N6297

FIGURE 11 – TEMPERATURE COEFFICIENTS

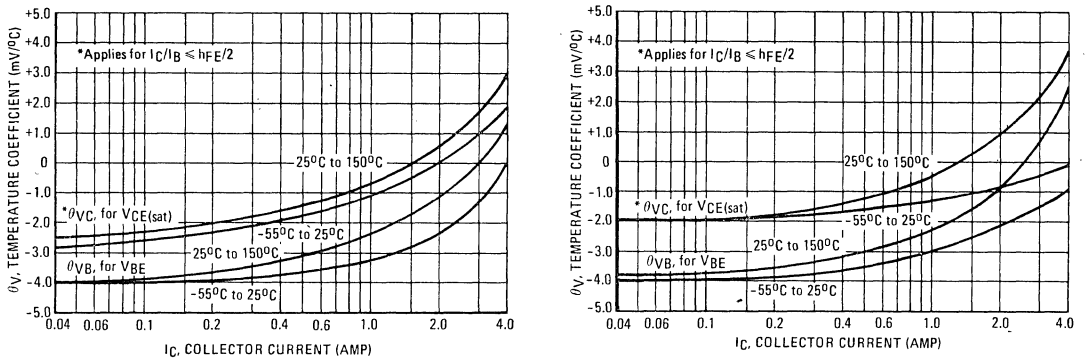


FIGURE 12 – COLLECTOR CUTOFF REGION

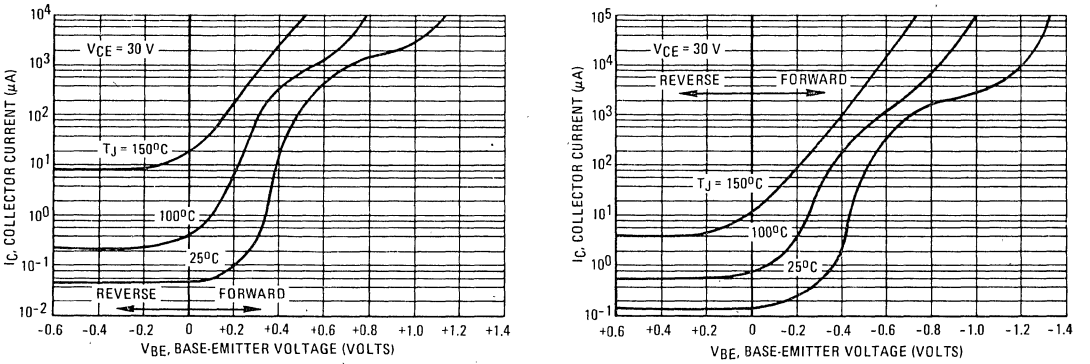
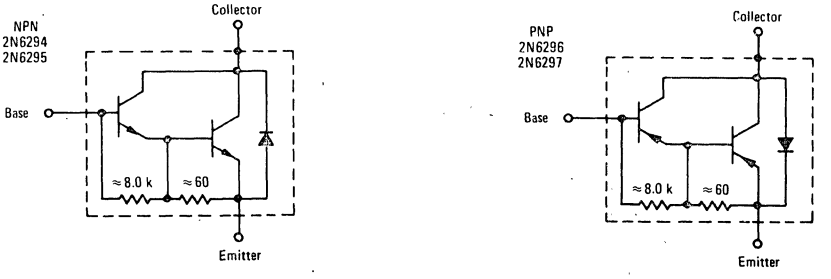


FIGURE 13 – DARLINGTON SCHEMATICS



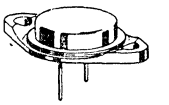
HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

. . . designed for high voltage inverters, switching regulators and line-operated amplifier applications. Especially well suited for switching power supply applications in associated consumer products.

- High Collector-Base Voltage –
  V_{CB} = 500 Vdc – 2N6306
  = 600 Vdc – 2N6307
  = 700 Vdc – 2N6308
- Excellent DC Current Gain @ I_C = 3.0 Adc
  h_{FE} = 15 - 75 – 2N6306, 2N6307
  = 12 - 60 – 2N6308
- Low Collector-Emitter Saturation Voltage @ I_C = 3.0 Adc
  $V_{CE(sat)}$ = 0.8 Vdc (Max) – 2N6306
  = 1.0 Vdc (Max) – 2N6307
  = 1.5 Vdc (Max) – 2N6308
- Current Gain Bandwidth Product –
  f_T = 5.0 MHz (Min) @ I_C = 0.3 Adc

8 AMPERE POWER TRANSISTORS NPN SILICON

250-300-350 VOLTS
125 WATTS



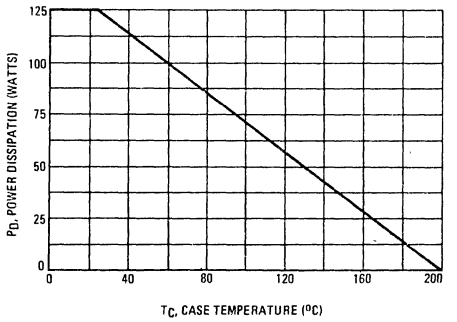
*MAXIMUM RATINGS

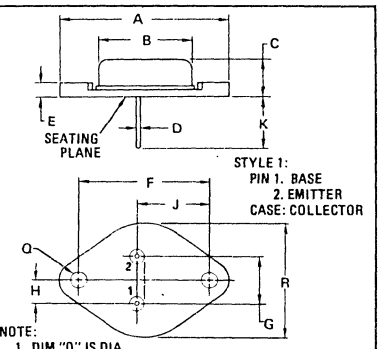
Rating	Symbol	2N6306	2N6307	2N6308	Unit
Collector-Base Voltage	V_{CB}	500	600	700	Vdc
Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
Emitter-Base Voltage	V_{EB}	8.0			Vdc
Collector Current – Continuous Peak	I_C	8.0 16			Adc
Base Current	I_B	4.0			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 0.714			Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200			°C

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.4	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING





NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-03
TO-3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N6306		250	–	
	2N6307		300	–	
	2N6308		350	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = Rated V_{CEO}, I_B = 0)			–	0.5	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 500 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6306		–	0.5	
(V_{CE} = 600 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6307		–	0.5	
(V_{CE} = 700 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6308		–	0.5	
(V_{CE} = 450 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6306		–	2.5	
(V_{CE} = 550 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6307		–	2.5	
(V_{CE} = 650 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6308		–	2.5	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 8.0 Vdc, I_C = 0)			–	1.0	
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)	2N6306, 2N6307		15	75	
	2N6308		12	60	
(I_C = 8.0 Adc, V_{CE} = 5.0 Vdc)	2N6306, 2N6307		4.0	–	
	2N6308		3.0	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 0.6 Adc)	2N6306		–	0.8	
	2N6307		–	1.0	
	2N6308		–	1.5	
(I_C = 8.0 Adc, I_B = 2.0 Adc)	2N6306, 2N6307		–	5.0	
(I_C = 8.0 Adc, I_B = 2.67 Adc)	2N6308		–	5.0	
Base-Emitter Saturation Voltage (1)		$V_{BE(sat)}$			Vdc
(I_C = 8.0 Adc, I_B = 2.0 Adc)	2N6306, 2N6307		–	2.3	
(I_C = 8.0 Adc, I_B = 2.67 Adc)	2N6308		–	2.5	
Base-Emitter On Voltage (1)		$V_{BE(on)}$			Vdc
(I_C = 3.0 Adc, V_{CE} = 5.0 Vdc)	2N6306, 2N6307		–	1.3	
	2N6308		–	1.5	
Second Breakdown Energy (Figure 2)		$E_{s/b}$			mJ
($I_{C(PK)}$ = 3.0 Adc, L = 40 mH, R_{BE} = 3 kΩ, V_{BB2} = 1.5 Vdc)			–	180	
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2)		f_T			MHz
(I_C = 0.3 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)			5.0	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)			–	250	
SWITCHING CHARACTERISTICS					
Rise Time		t_r			μs
(V_{CC} = 125 Vdc, I_C = 3.0 Adc, I_B = 0.6 Adc)			–	0.6	
Storage Time (3)		t_s			μs
(V_{CC} = 125 Vdc, I_C = 3.0 Adc, I_{B1} = 0.6 Adc, I_{B2} = 1.5 Adc)					
Pulse Width = 25 μs			–	1.6	
Pulse Width = 5.0 μs			–	0.8	
Fall Time		t_f			μs
(V_{CC} = 125 Vdc, I_C = 3.0 Adc, I_{B1} = 0.6 Adc, I_{B2} = 1.5 Adc)			–	0.4	

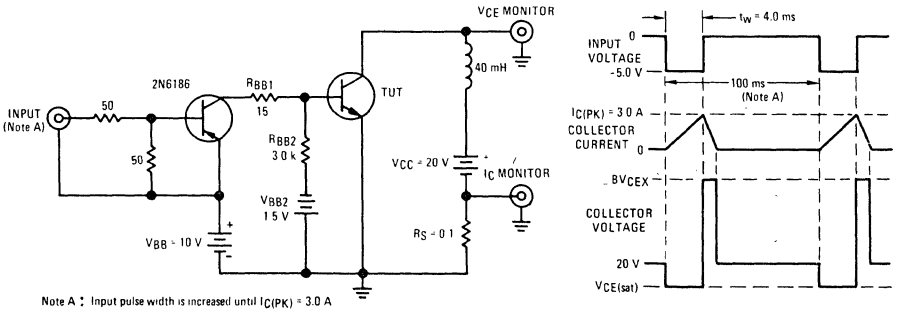
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2.0%

(2) $f_T = |h_{fe}| \cdot f_{test}$

(3) "On" time is 25 μs. t_s decreases with shorter pulse widths, being approximately 50% of the values shown at a 5.0 μs pulse width

*Indicates JEDEC Registered Data

FIGURE 2 – SECOND BREAKDOWN ENERGY TEST CIRCUIT AND WAVEFORMS



Note A: Input pulse width is increased until $I_{C(PK)}$ = 3.0 A

FIGURE 3 – THERMAL RESPONSE

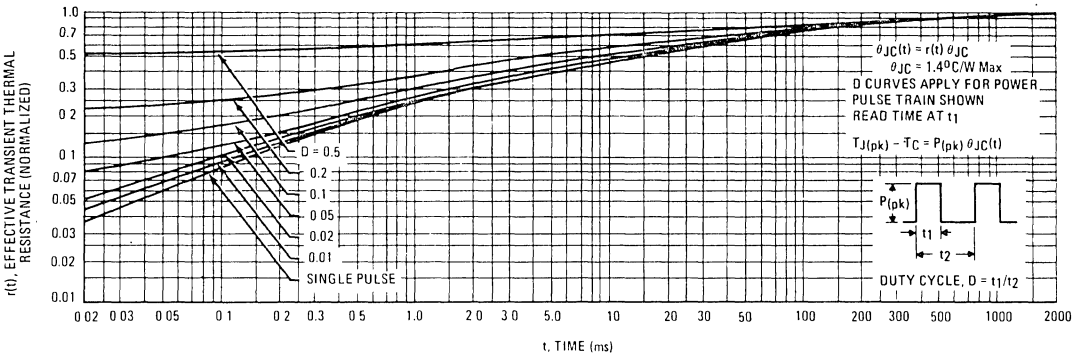
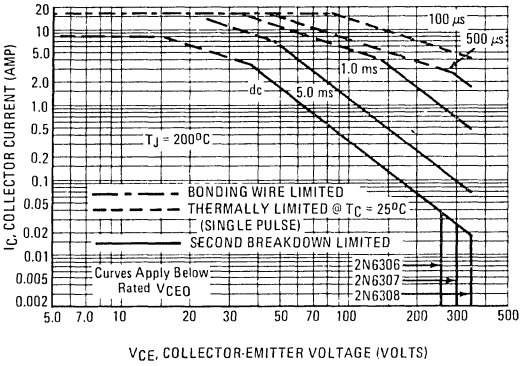


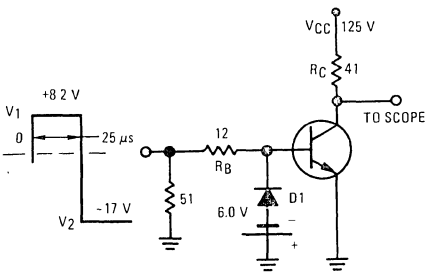
FIGURE 4 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor. average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)} = 200^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 5 – SWITCHING TIMES TEST CIRCUIT



DUTY CYCLE 1%
t_r, $t_f \leqslant 10$ ns
D_1 – 1N3879
COLLECTOR-BASE JUNCTION

FOR DATA IN FIGURE 6, R_B & R_C ARE VARIED TO OBTAIN DESIRED TEST CONDITIONS. D_1 OMITTED AND V_2 REDUCED TO 5.0 V FOR t_d and t_r MEASUREMENTS

FIGURE 6 – TURN-ON AND TURN-OFF TIMES

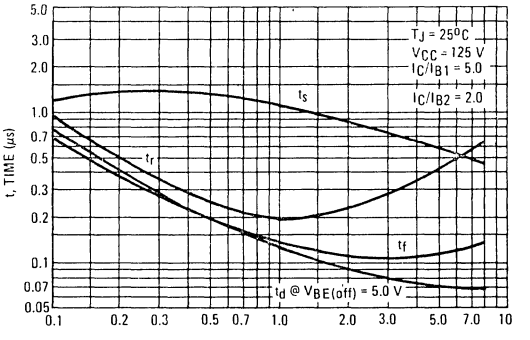


FIGURE 7 – DC CURRENT GAIN

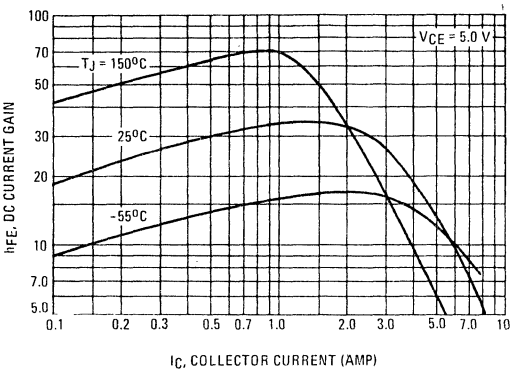


FIGURE 8 – COLLECTOR SATURATION REGION

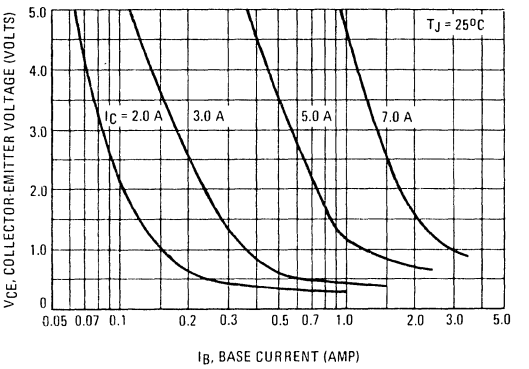


FIGURE 9 – "ON" VOLTAGES

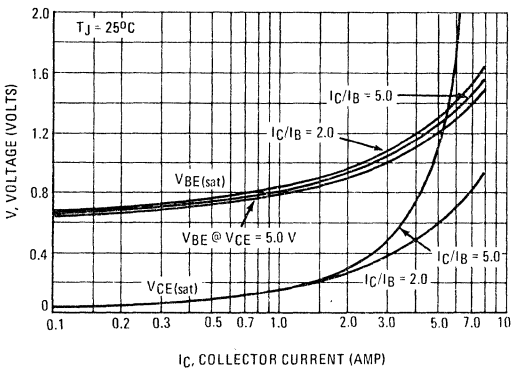


FIGURE 10 – TEMPERATURE COEFFICIENTS

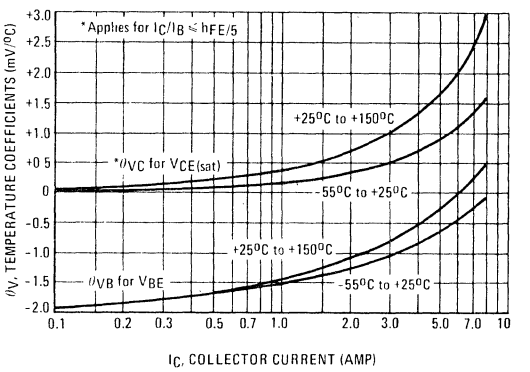


FIGURE 11 – COLLECTOR-CUTOFF REGION

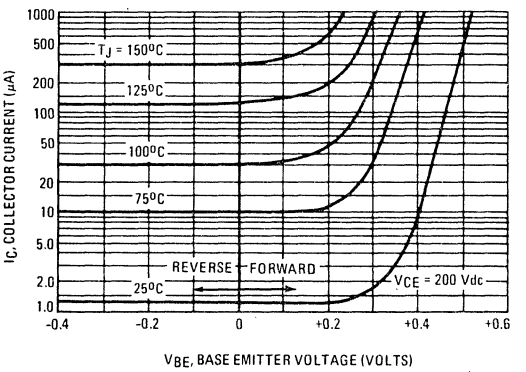
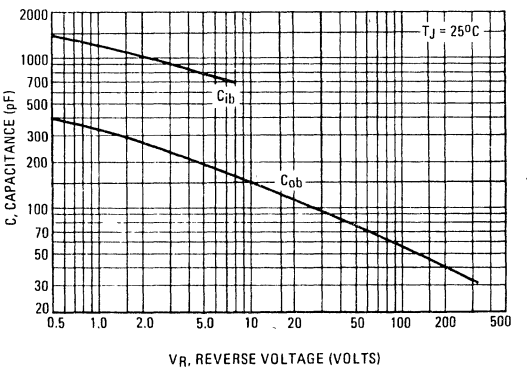


FIGURE 12 – CAPACITANCE



NPN
2N6315 2N6316
PNP
2N6317 2N6318

COMPLEMENTARY SILICON MEDIUM-POWER TRANSISTORS

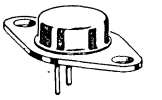
. . . designed for general-purpose power amplifier and switching applications.

- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 4.0 Adc
- Low Leakage Current – I_{CEX} = 0.25 mAdc (Max)
- Excellent DC Current Gain – h_{FE} = 20 (Min) @ I_C = 2.5 Adc
- High Current Gain – Bandwidth Product – f_T = 4.0 MHz @ I_C = 0.25 Adc

7.0 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS
90 WATTS



4

*MAXIMUM RATINGS

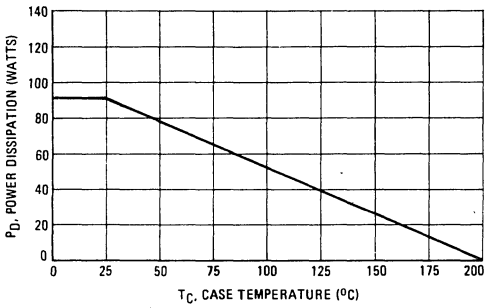
Rating	Symbol	2N6315 2N6317	2N6316 2N6318	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous Peak	I_C	7.0 15		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation – T_C = 25°C Derate above 25°C	P_D	90 0.515		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

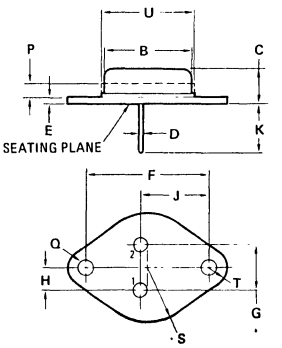
Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.94	°C/W

*Indicates JEDEC registered data. Limits and conditions differ on some parameters and re-registration reflecting these changes has been requested. All above values meet or exceed present JEDEC registered data.

FIGURE 1 – POWER DERATING



Safe Area Limits are indicated by Figure 13.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

4

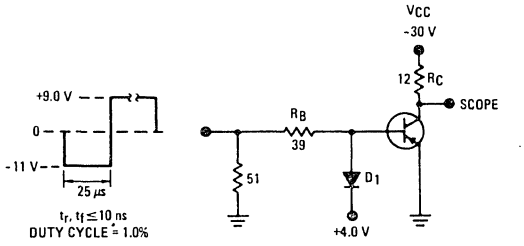
*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	2N6315,2N6317	$V_{CEO(sus)}$	60	–	Vdc
	2N6316,2N6318		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N6315,2N6317		–	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	2N6316,2N6318		–	0.5	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6315,2N6317		–	0.25	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6316,2N6318		–	0.25	
(V_{CE} = 60 Vdc $V_{BE(off)}$ =1.5 Vdc,T_C =150°C)	2N6315,2N6317		–	2.0	
(V_{CE} = 80 Vdc,$V_{BE(off)}$ =1.5 Vdc,T_C =150°C)	2N6316,2N6318		–	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N6315,2N6317		–	0.25	
(V_{CB} = 80 Vdc, I_E = 0)	2N6316,2N6318		–	0.25	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 4.0 Vdc)			35	–	
(I_C = 2.5 Adc, V_{CE} = 4.0 Vdc)			20	100	
(I_C = 7.0 Adc, V_{CE} = 4.0 Vdc)			4.0	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 4.0 Adc, I_B = 0.4 Adc)			–	1.0	
(I_C = 7.0 Adc, I_B = 1.75 Adc)			–	2.0	
Base-Emitter Saturation Voltage (1) (I_C = 7.0 Adc, I_B = 1.75 Adc)		$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (1) (I_C = 2.5 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (2) (I_C = 0.25 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	4.0	–	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N6317,2N6318		–	300	
	2N6315,2N6316		–	200	
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	20	–	–
SWITCHING CHARACTERISTICS					
Rise Time	(V_{CC} = 30 Vdc, I_C = 2.5 Adc, I_{B1} = I_{B2} = 0.25 Adc)	t_r	–	0.7	μs
Storage Time		t_s	–	1.0	μs
Fall Time		t_f	–	0.8	μs

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2 0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

TYPICAL CHARACTERISTICS

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



FOR CURVES OF FIGURES 3 AND 5, R_B AND R_C ARE VARIED TO OBTAIN DESIRED CURRENT LEVELS.
D_1 MUST BE FAST RECOVERY TYPE, e.g.
MBD5300 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA
FOR NPN TEST CIRCUIT, REVERSE ALL POLARITIES.

FIGURE 3 – TURN "ON" TIME

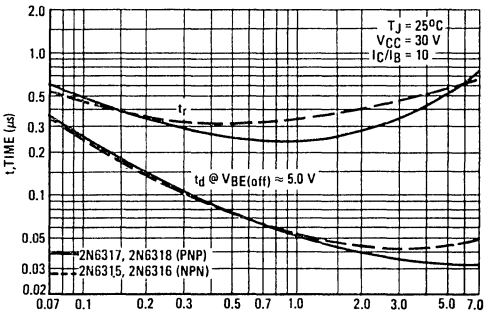


FIGURE 4 – THERMAL RESPONSE

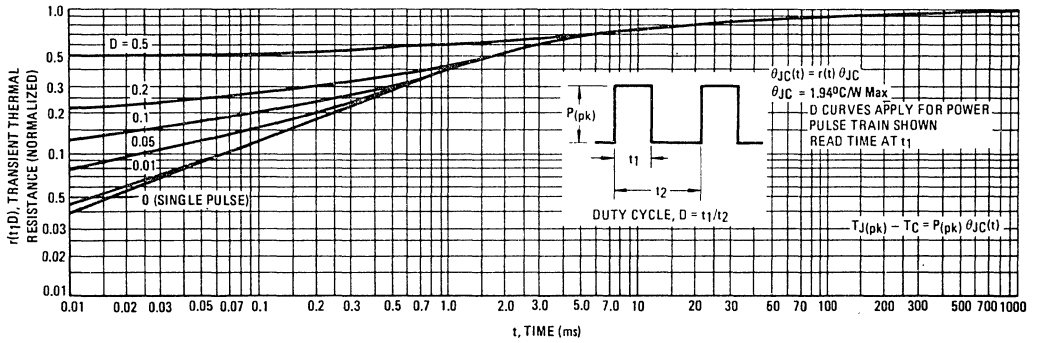


FIGURE 5 – TURN "OFF" TIME

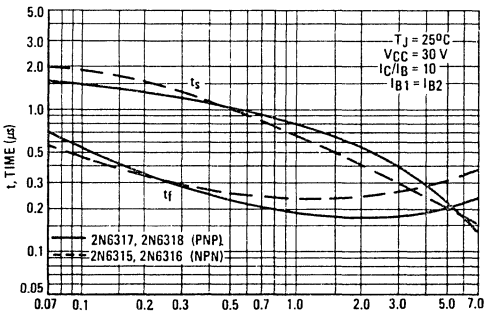
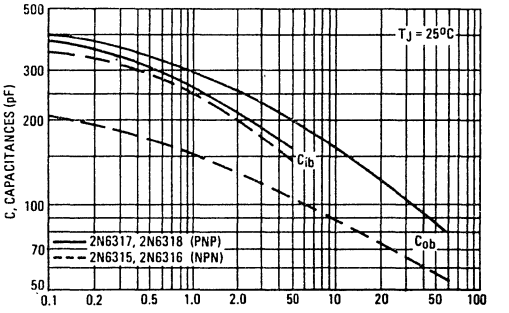


FIGURE 6 – CAPACITANCE

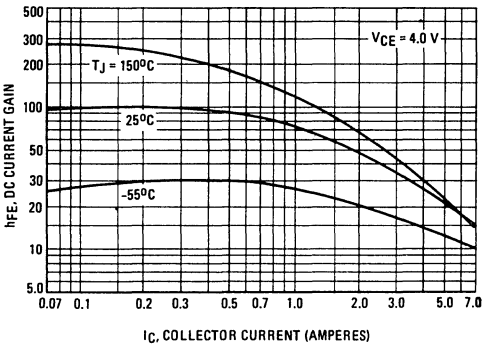


4

NPN
2N6315 and 2N6316

PNP
2N6317 and 2N6318

FIGURE 7 – DC CURRENT GAIN



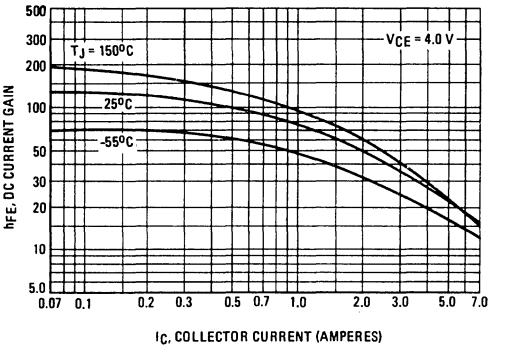
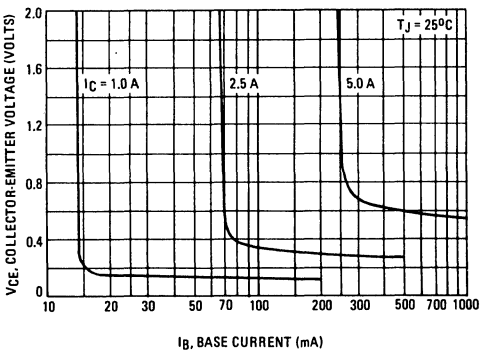


FIGURE 8 – COLLECTOR SATURATION REGION



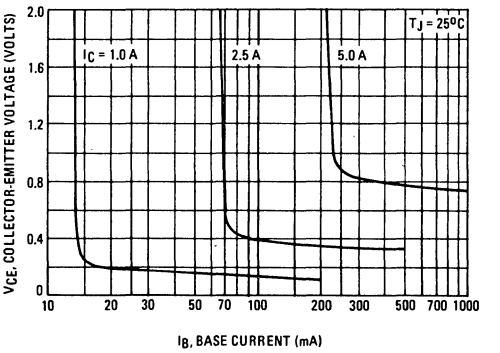
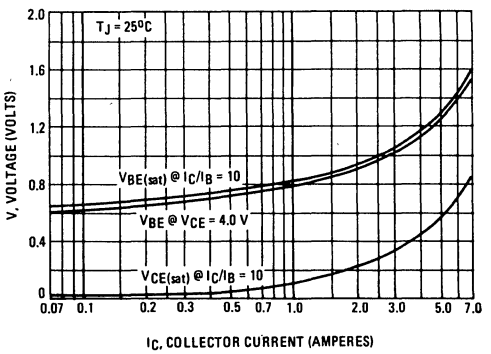
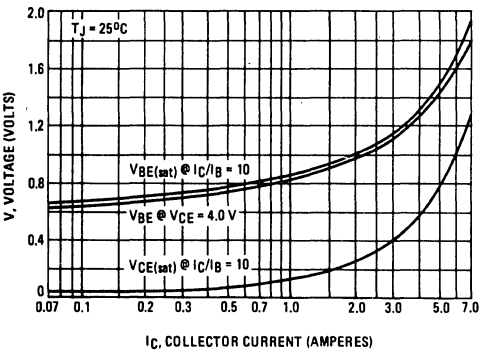


FIGURE 9 – "ON" VOLTAGES





NPN
2N6315 and 2N6316

PNP
2N6317 and 2N6318

FIGURE 10 – TEMPERATURE COEFFICIENTS

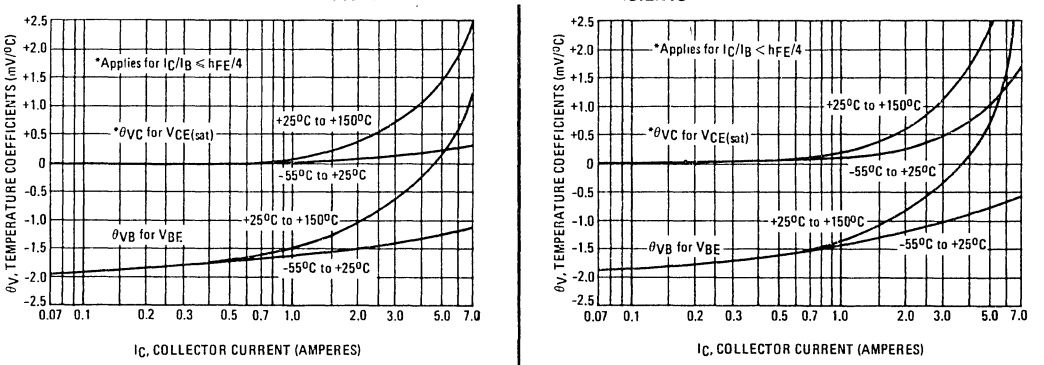


FIGURE 11 – COLLECTOR CUT-OFF REGION

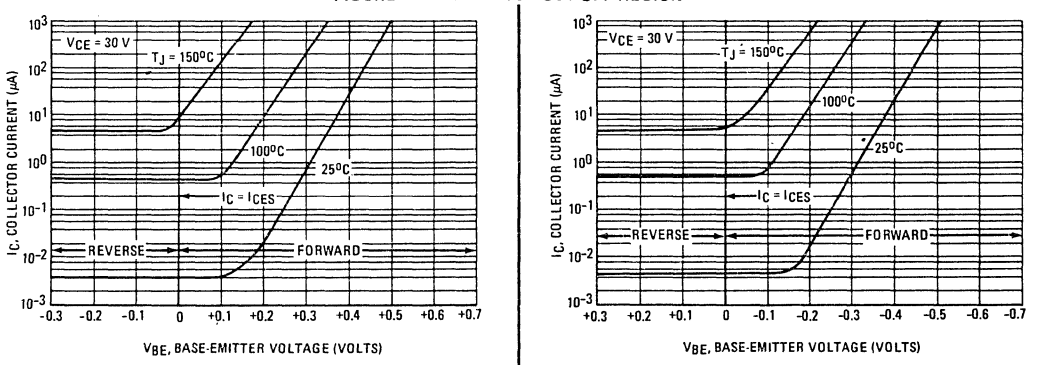


FIGURE 12 – EFFECTS OF EXTERNAL BASE-EMITTER RESISTANCE

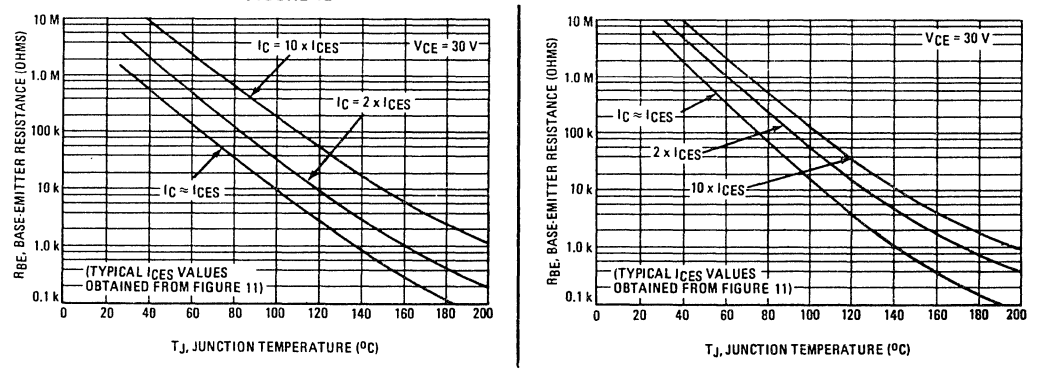


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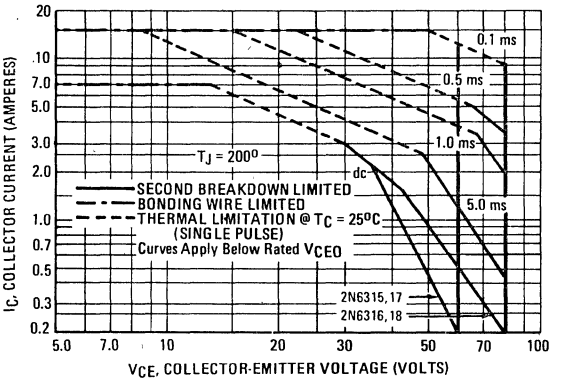
FIGURE 13 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 200°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

2N6338 (SILICON) thru 2N6341

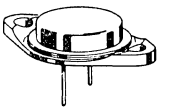
HIGH-POWER NPN SILICON TRANSISTORS

. . . designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 100 Vdc (Min) – 2N6338
  = 120 Vdc (Min) – 2N6339
  = 140 Vdc (Min) – 2N6340
  = 150 Vdc (Min) – 2N6341
- High DC Current Gain –
  h_{FE} = 30-120 @ I_C = 10 Adc
  = 12 (Min) @ I_C = 25 Adc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc
- Fast Switching Times @ I_C = 10 Adc
  t_r = 0.3 μs (Max)
  t_s = 1.0 μs (Max)
  t_f = 0.25 μs (Max)
- Complement to 2N6436–38

25 AMPERE
POWER TRANSISTORS
NPN SILICON

100, 120, 140, 150 VOLTS
200 WATTS



*MAXIMUM RATINGS

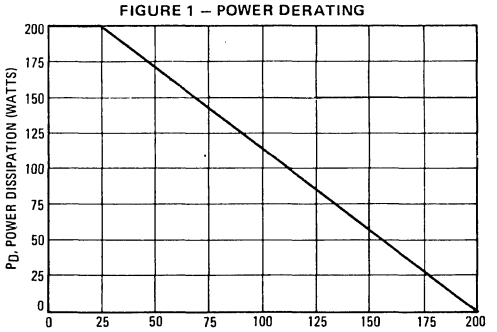
Rating	Symbol	2N6338	2N6339	2N6340	2N6341	Unit
Collector-Base Voltage	V_{CB}	120	140	160	180	Vdc
Collector-Emitter Voltage	V_{CEO}	100	120	140	150	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →				Vdc
Collector Current – Continuous	I_C	← 25 →				Adc
Peak		← 50 →				
Base Current	I_B	← 10 →				Adc
Total Device Dissipation @ T_C = 25°C	P_D	← 200 →				Watts
Derate above 25°C		← 1.14 →				W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	← -65 to +200 →				°C

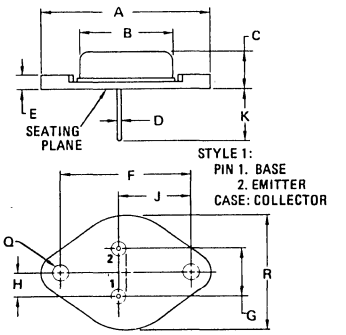
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING





NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

4

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

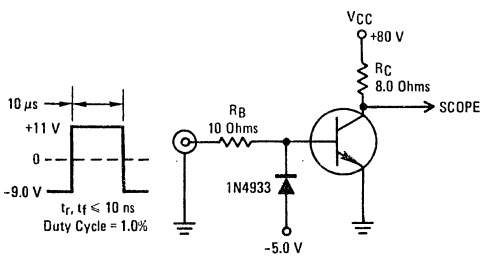
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N6338		100	–	
	2N6339		120	–	
	2N6340		140	–	
	2N6341		150	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 50 Vdc, I_B = 0)	2N6338		–	50	
(V_{CE} = 60 Vdc, I_B = 0)	2N6339		–	50	
(V_{CE} = 70 Vdc, I_B = 0)	2N6340		–	50	
(V_{CE} = 75 Vdc, I_B = 0)	2N6341		–	50	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc)			–	10	μAdc
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)			–	1.0	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	–	10	μAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	100	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)			50	–	
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)			30	120	
(I_C = 25 Adc, V_{CE} = 2.0 Vdc)			12	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)			–	1.0	
(I_C = 25 Adc, I_B = 2.5 Adc)			–	1.8	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)			–	1.8	
(I_C = 25 Adc, I_B = 2.5 Adc)			–	2.5	
Base-Emitter On Voltage (I_C = 10 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	40	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	300	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 6.0 Vdc)		t_r	–	0.3	μs
Storage Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)		t_s	–	1.0	μs
Fall Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)		t_f	–	0.25	μs

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



Note: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 – TURN-ON TIME

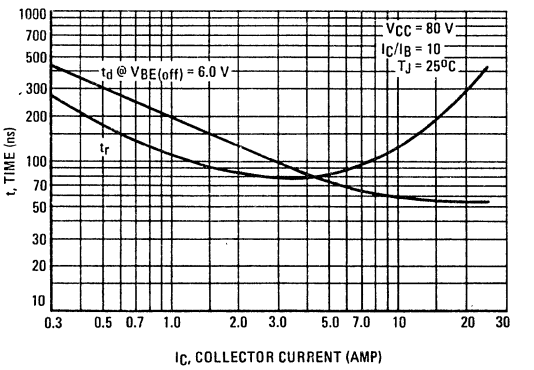


FIGURE 4 – THERMAL RESPONSE

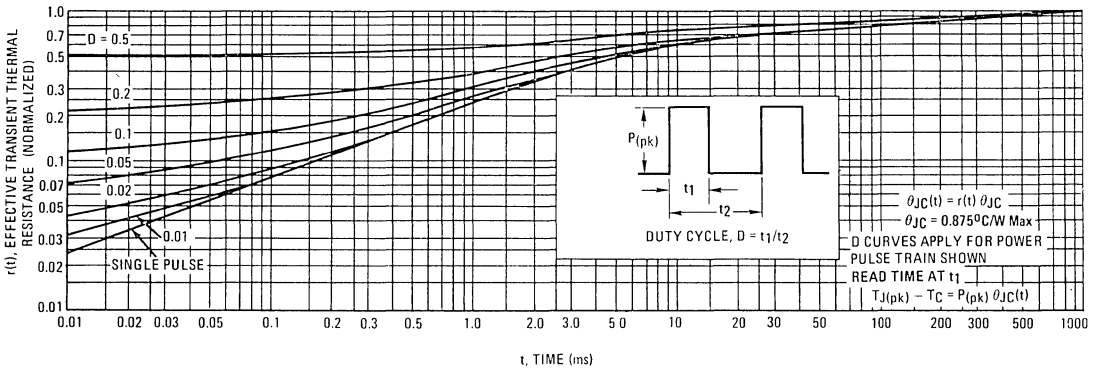
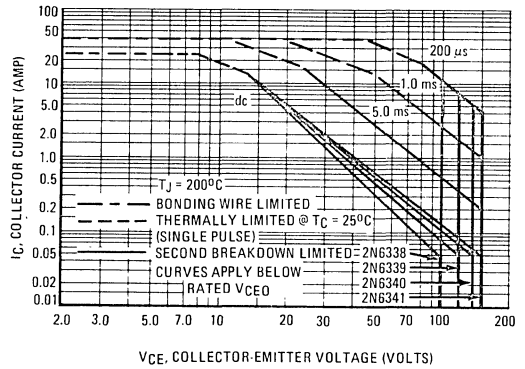


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

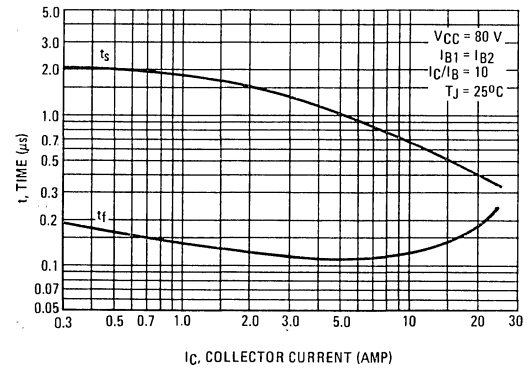


FIGURE 7 – CAPACITANCE

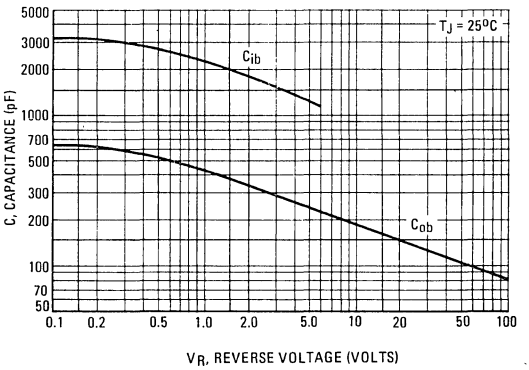


FIGURE 8 – DC CURRENT GAIN

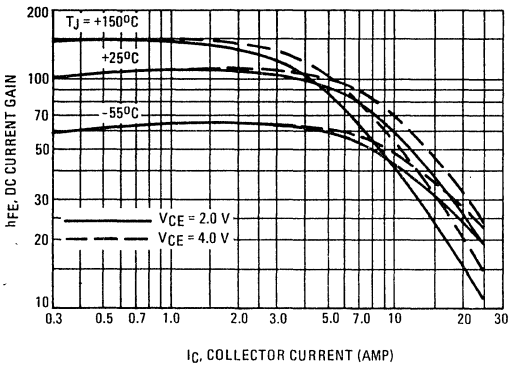


FIGURE 9 – COLLECTOR SATURATION REGION

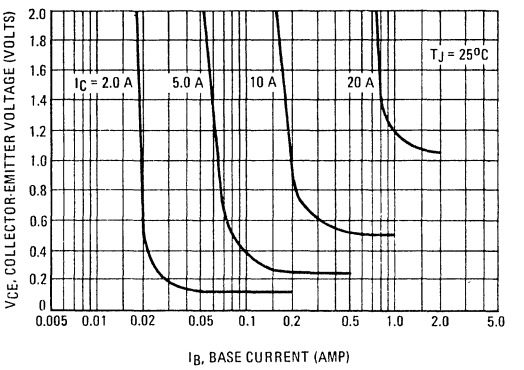


FIGURE 10 – "ON" VOLTAGES

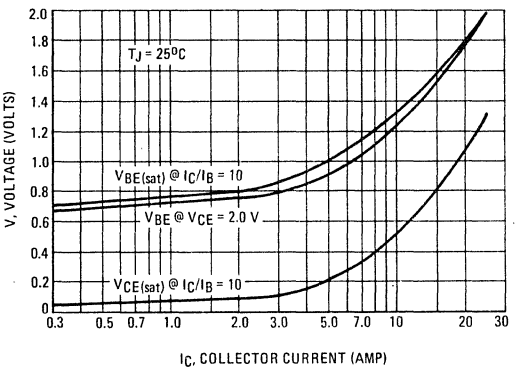


FIGURE 11 – TEMPERATURE COEFFICIENTS

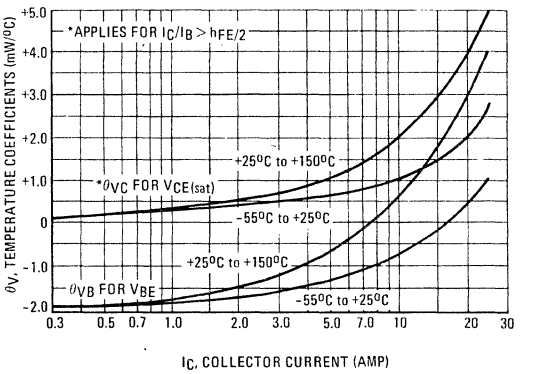


FIGURE 12 – COLLECTOR CUT-OFF REGION

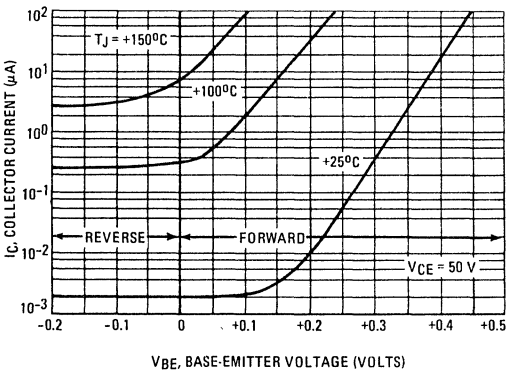
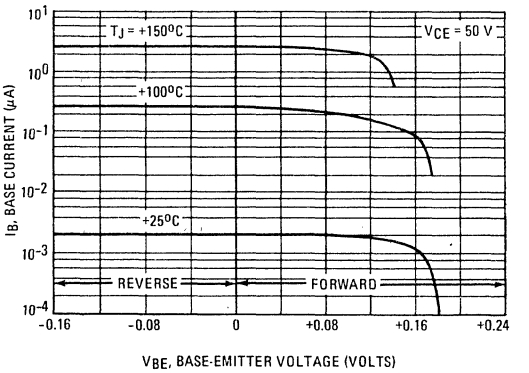


FIGURE 13 – BASE CUT-OFF REGION



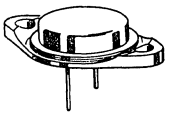
2N6377 (SILICON) thru 2N6379

HIGH-POWER PNP SILICON TRANSISTORS

. . . designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector Emitter Sustaining Voltage –
  $V_{CEO\ (sus)}$ = 80 Vdc (Min) – 2N6377
  = 100 Vdc (Min) – 2N6378
  = 120 Vdc (Min) – 2N6379
- High DC Current Gain –
  h_{FE} = 30-120 @ I_C = 20 Adc
  = 10 (Min) @ I_C = 50 Adc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 20 Adc
- Fast Switching Times @ I_C = 20 Adc
  t_r = 0.35 μs (Max)
  t_s = 0.8 μs (Max)
  t_f = 0.25 μs (Max)
- Complement to 2N6274–77

50 AMPERE
POWER TRANSISTORS
PNP SILICON
80, 100, 120 VOLTS
250 WATTS



* MAXIMUM RATINGS

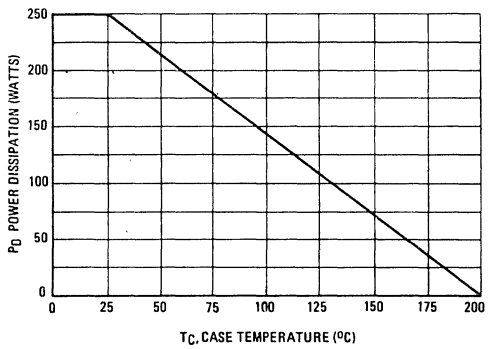
Rating	Symbol	2N6377	2N6378	2N6379	Unit
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Collector-Emitter Voltage	V_{CEO}	80	100	120	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current – Continuous Peak	I_C	← 50 → ← 100 →			Adc
Base Current	I_B	← 20 →			Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	← 250 → ← 1.43 →			Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			^oC

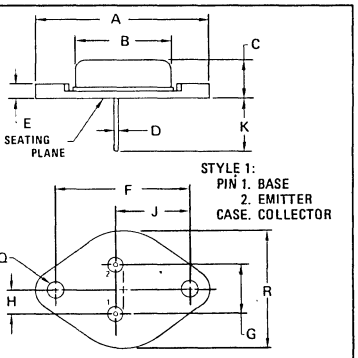
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	$^oC/W$

*Indicates JEDEC Registered Data.

FIGURE 1 – POWER DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01

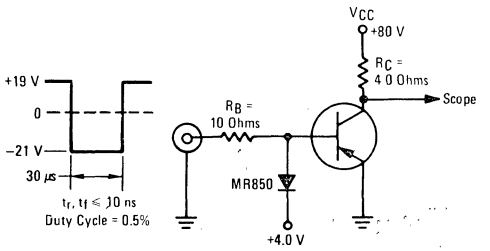
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N6380		80	–	
	2N6381		100	–	
	2N6382		120	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 50 Vdc, I_B = 0)	2N6380		–	50	
(V_{CE} = 60 Vdc, I_B = 0)	2N6381		–	50	
(V_{CE} = 70 Vdc, I_B = 0)	2N6382		–	50	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 90% Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)			–	10	μAdc
(V_{CE} = 90% Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	1.0	mAdc
Emitter Cutoff Current		I_{EBO}	–	100	μAdc
(V_{EB} = 6.0 Vdc, I_C = 0)					
***ON CHARACTERISTICS** (1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			50	–	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)			30	120	
(I_C = 50 Adc, V_{CE} = 4.0 Vdc)			10	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	–		Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)			–	1.2	
(I_C = 50 Adc, I_B = 10 Adc)			–	3.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)			–	1.8	
(I_C = 50 Adc, I_B = 10 Adc)			–	3.5	
DYNAMIC CHARACTERISTICS					
*Current-Gain — Bandwidth Product (2)		f_T	30	–	MHz
(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)					
Input Capacitance		C_{ib}			pF
(V_{EB} = 2.0 Vdc, I_C = 0, f = 0.1 MHz)			–	7000	
*Output Capacitance		C_{ob}	–	1500	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)					
***SWITCHING CHARACTERISTICS** (Figure 2)					
Rise Time	(V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)	t_r	–	0.35	μs
Storage Time		t_s	–	0.80	μs
Fall Time		t_f	–	0.25	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%. (2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



Note: For information on Figures 3 & 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 – TURN ON TIME

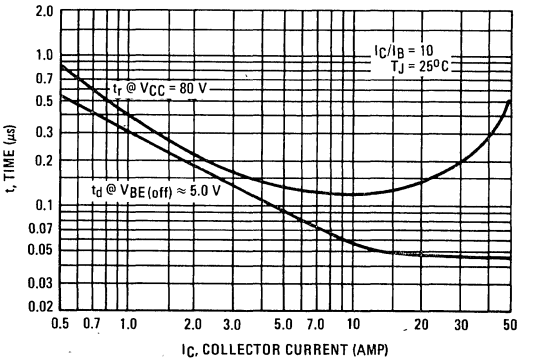


FIGURE 4 – THERMAL RESPONSE

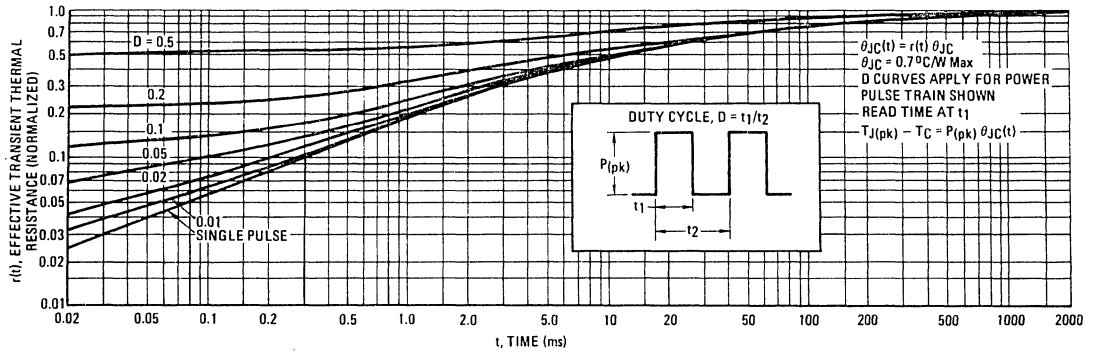
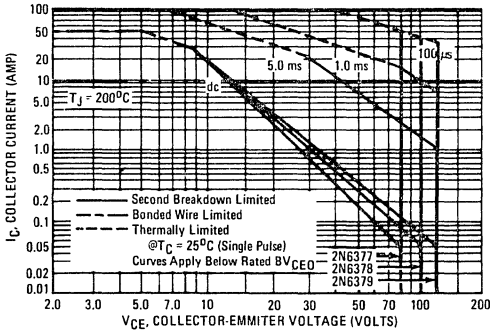


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor. average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

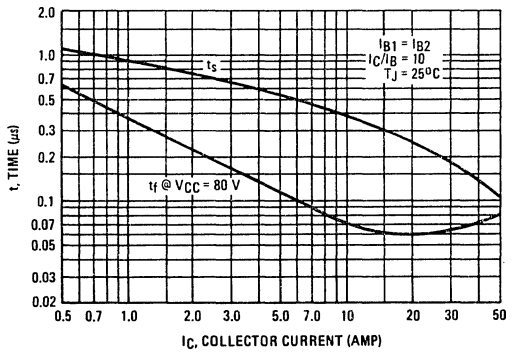


FIGURE 7 – CAPACITANCE

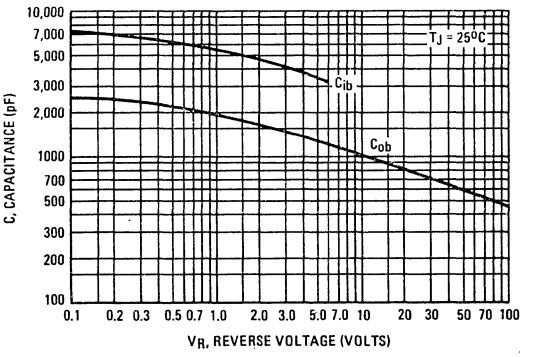


FIGURE 8 – DC CURRENT GAIN

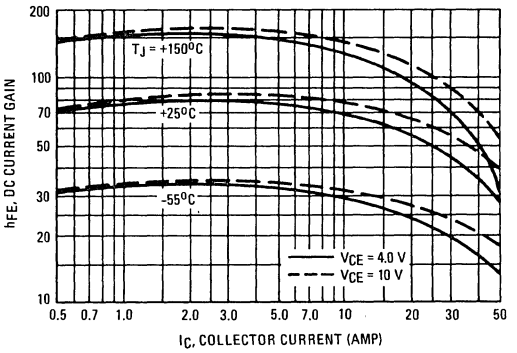


FIGURE 9 – COLLECTOR SATURATION REGION

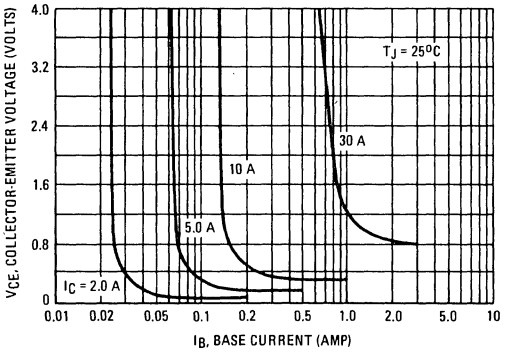


FIGURE 10 – "ON" VOLTAGES

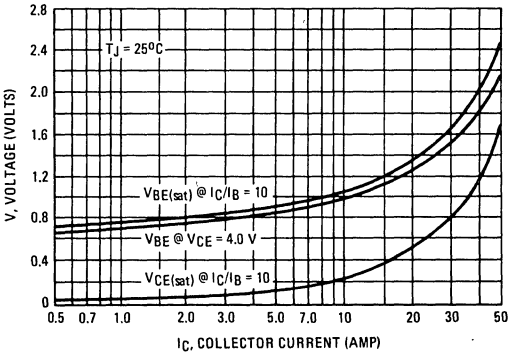


FIGURE 11 – TEMPERATURE COEFFICIENTS

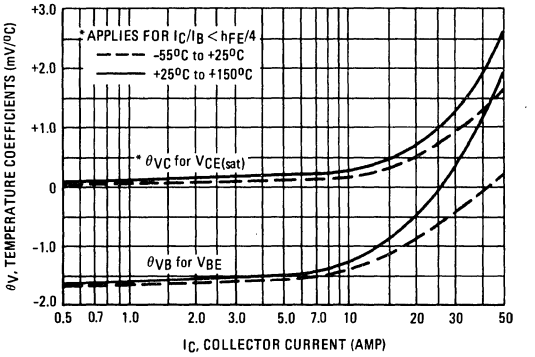


FIGURE 12 – COLLECTOR CUT-OFF REGION

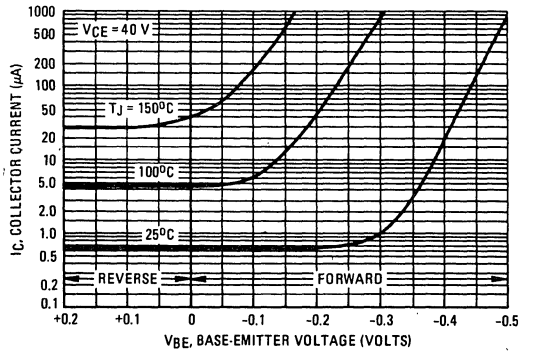
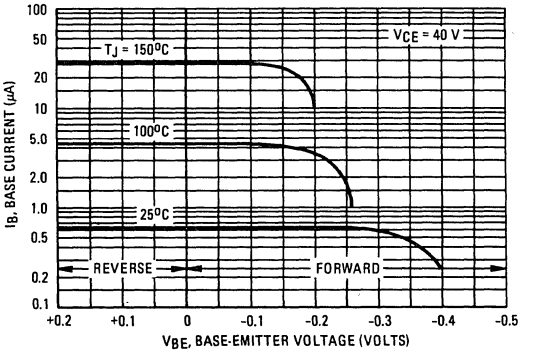


FIGURE 13 – BASE CUTOFF REGION



NPN 2N6383 2N6384 2N6385
PNP 2N6648 2N6649 2N6650

COMPLEMENTARY SILICON POWER DARLINGTON TRANSISTORS

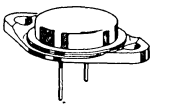
. . . monolithic complementary silicon Darlington transistors designed for low and medium frequency power applications such as power switching, audio amplifiers, hammer drivers, and shunt and series regulators.

- High Gain Darlington Performance
- True Complementary Specifications

15 AMPERE PEAK

COMPLEMENTARY SILICON POWER DARLINGTON TRANSISTORS

40–60–80 VOLTS
100 WATTS



4

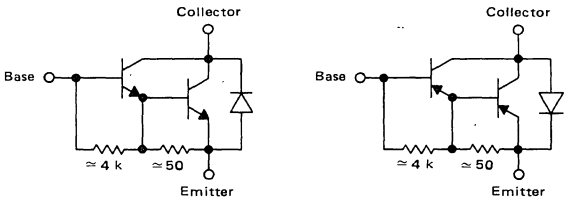
*MAXIMUM RATINGS

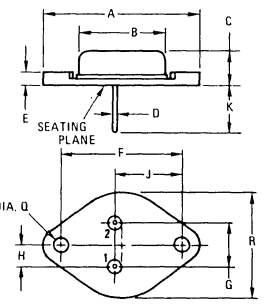
Rating	Symbol	2N6383 2N6648	2N6384 2N6649	2N6385 2N6650	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	40	60	80	Vdc
Collector-Emitter Voltage	V_{CEX}	40	60	80	Vdc
Collector-Emitter Voltage	V_{CBO}	40	60	80	Vdc
Emitter Base Voltage	V_{EBO}	5.0			Vdc
Collector Current — Continuous	I_C	10			Adc
Peak (1)**	I_{CM}	15			
Base Current — Continuous	I_B	0.25			Adc
Total Power Dissipation @ $T_C = 25^oC$ (2)	P_D	100			Watts
Derate above 25^oC		0.571			$W/^oC$
Operating and Storage Junction Temperature Range (2)	T_J, T_{stg}	−65 to +200			^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	$^oC/W$
Maximum Lead Temperature for Soldering Purposes, 1/32" from Case for 5 Seconds	T_L	235	^oC

*Indicates JEDEC Registered Data.
**Not JEDEC Registered.
(1) Pulse Width = 50 ms, Duty Cycle ≤ 10%.
(2) Exceeds JEDEC Registration for 2N6648, 2N6649, 2N6650.
JEDEC Registration gives P_D = 70 W, T_J = 150°C.





STYLE 1.
PIN 1 BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.560
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case
CASE 11-01
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
*Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0	2N6383, 2N6648		40	–	
	2N6384, 2N6649		60	–	
	2N6385, 2N6650		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = Rated Value)			–	1.0	
*Collector Cutoff Current		I_{CEV}			mAdc
(V_{CE} = Rated $V_{CEO(sus)}$ Value, $V_{BE(off)}$ = 1.5 Vdc)			–	0.3	
(V_{CE} = Rated $V_{CEO(sus)}$ Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	3.0	
*Emitter Cutoff Current		I_{EBO}	–	10	mAdc
(V_{EB} = 5.0 Vdc, I_C = 0)					
Collector-Emitter Sustaining Voltage (1)		$V_{CER(sus)}$			Vdc
(R_{BE} = 100 Ω, I_C = 200 mA)	2N6383, 2N6648		40	–	
	2N6384, 2N6649		60	–	
	2N6385, 2N6650		80	–	
Collector-Emitter Sustaining Voltage (1)		$V_{CEV(sus)}$			Vdc
($V_{BE(off)}$ = 1.5 V, I_C = 200 mA)	2N6383, 2N6648		40	–	
	2N6384, 2N6649		60	–	
	2N6385, 2N6650		80	–	
ON CHARACTERISTICS (1)					
*DC Current Gain		h_{FE}			–
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)			1000	20,000	
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)			100	–	
*Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 0.01 Adc)			–	2.0	
(I_C = 10 Adc, I_B = 0.1 Adc)			–	3.0	
*Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)			–	2.8	
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)			–	4.5	
Diode Forward Voltage		V_F	–	4.0	Vdc
(I_F = 10 Adc)					
***DYNAMIC CHARACTERISTICS**					
Output Capacitance		C_{ob}	–	200	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)					
*Magnitude of Common-Emitter Small-Signal Short-Circuit Current Transfer Ratio		$\|h_{fe}\|$	20	–	–
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 MHz)					
Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio		h_{fe}	1000	–	–
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)					
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base-Forward Biased		$I_{S/B}$	See Figures 8 and 9		
Second Breakdown Energy with Base Reverse-Biased		$E_{s/b}$	120	–	mJ
(L = 12 mH, R_{BE} = 100 Ω, $V_{BE(off)}$ = 1.5 Vdc, I_C = 4.5 Adc)					

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

* Indicates JEDEC Registered Data.

FIGURE 1 – DC CURRENT GAIN

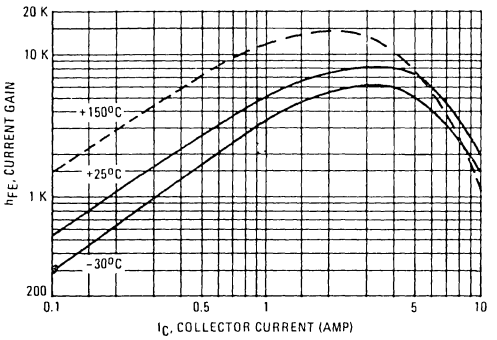
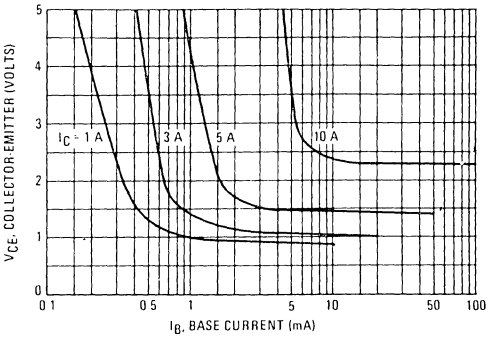


FIGURE 2 – COLLECTOR SATURATION REGION



4.

FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

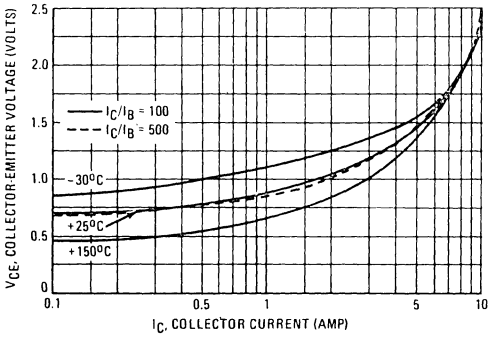


FIGURE 4 – BASE-EMITTER VOLTAGE

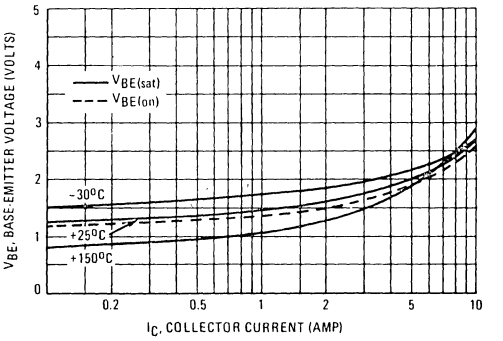


FIGURE 5 – SWITCHING TIME TEST CIRCUIT
(Shown for NPN)

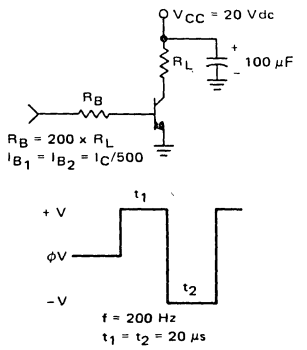


FIGURE 6 – SWITCHING TIMES

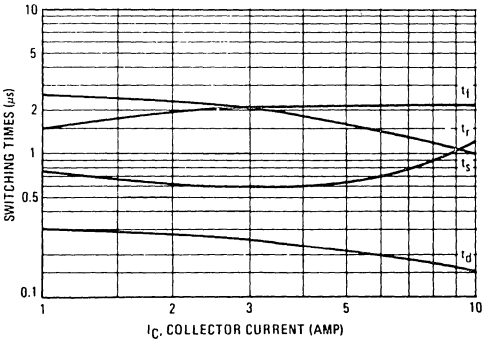
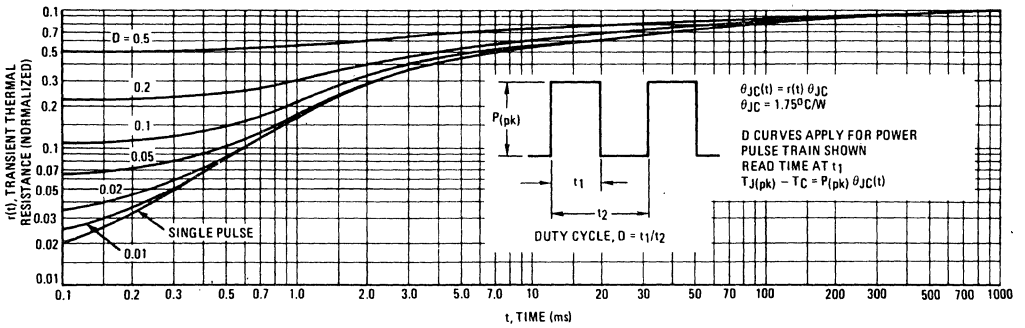


FIGURE 7 – THERMAL RESPONSE



4

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 8 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature.

$T_{J(pk)}$ may be calculated from the data in Figure 7. At high case temperatures, see Figure 9, thermal limitations will reduce the current that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do derate the same as thermal limitations. Allowable current at the voltages shown on Figure 8 may be found at any case temperature by derating linearly to 200°C.

FORWARD BIASED SAFE OPERATING AREA

FIGURE 8 – $T_C = 25^oC$

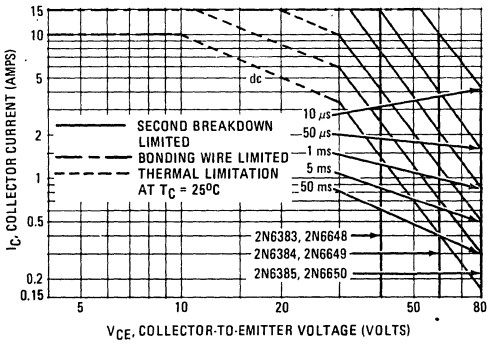


FIGURE 9 – $T_C = 100^oC$

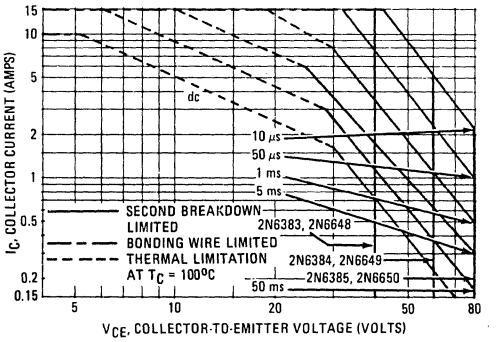
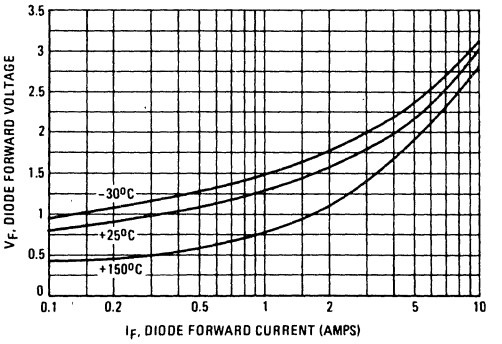


FIGURE 10 – CE DIODE CHARACTERISTICS



2N6386 2N6387 2N6388

PLASTIC MEDIUM-POWER SILICON TRANSISTORS

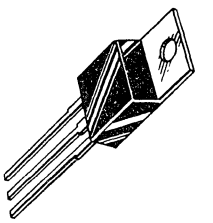
. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain –
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage – @ 100 mAdc
  $V_{CEO(sus)}$ = 40 Vdc (Min) – 2N6386
  = 60 Vdc (Min) – 2N6387
  = 80 Vdc (Min) – 2N6388
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc – 2N6386
  = 2.0 Vdc (Max) @ I_C = 5.0 Adc – 2N6387, 2N6388
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- TO-66 Leadform Also Available

DARLINGTON
8 AND 10 AMPERE

NPN SILICON POWER TRANSISTORS

40-60-80 VOLTS
65 WATTS



4

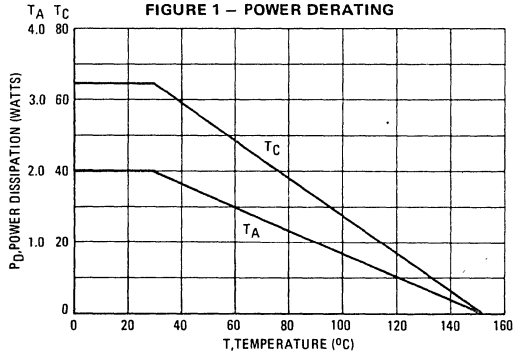
***MAXIMUM RATINGS**

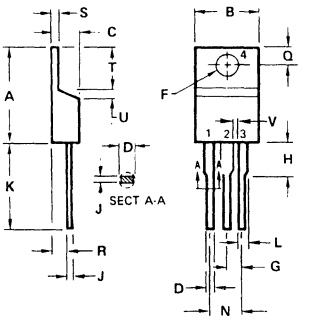
Rating	Symbol	2N6386	2N6387	2N6388	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current – Continuous Peak	I_C	8.0 15	10 15	10 15	Adc
Base Current	I_B	← 250 →			mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 65 → ← 0.52 →			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 2.0 → ← 0.016 →			Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	← −65 to +150 →			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE.
1. DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–

CASE 221A-02
TO-220AB

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N6386		40	–	
	2N6387		60	–	
	2N6388		80	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N6386		–	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N6387		–	1.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N6388		–	1.0	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6386		–	300	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6387		–	300	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6388		–	300	
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6386		–	3.0	mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6387		–	3.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6388		–	3.0	
Emitter Cutoff Current		I_{EBO}	–	5.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	2N6386		1000	20000	
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		1000	20000	
(I_C = 8.0 Adc, V_{CE} = 3.0 Vdc)	2N6386		100	–	
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		100	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 0.006 Adc)	2N6386		–	2.0	
(I_C = 5.0 Adc, I_B = 0.01 Adc)	2N6387, 2N6388		–	2.0	
(I_C = 8.0 Adc, I_B = 0.08 Adc)	2N6386		–	3.0	
(I_C = 10 Adc, I_B = 0.1 Adc)	2N6387, 2N6388		–	3.0	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	2N6386		–	2.8	
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		–	2.8	
(I_C = 8.0 Adc, V_{CE} = 3.0 Vdc)	2N6386		–	4.5	
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		–	4.5	
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain		$\|h_{fe}\|$	20	–	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)					
Output Capacitance		C_{ob}	–	200	pF
(V_{CB = 10 Vdc, I_E = 0, f = 1.0 MHz)					
Small-Signal Current Gain		h_{fe}	1000	–	–
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)					

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

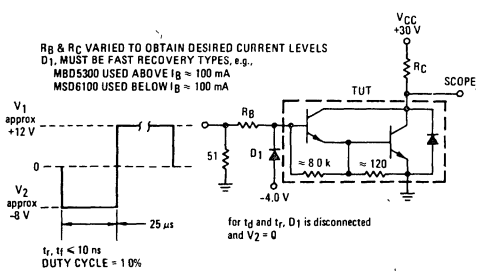


FIGURE 3 – SWITCHING TIMES

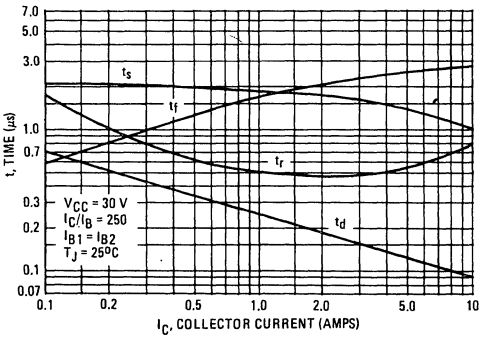


FIGURE 4 – THERMAL RESPONSE

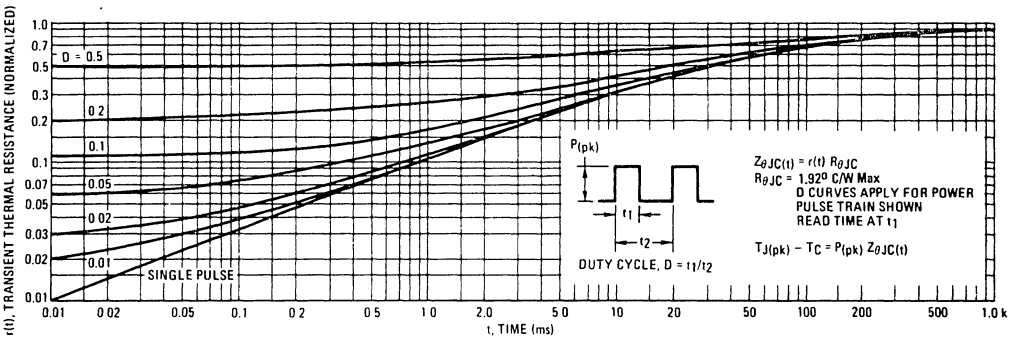
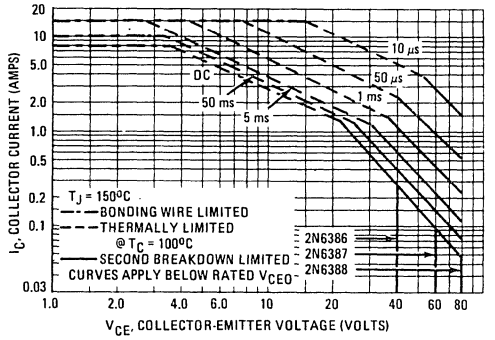


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

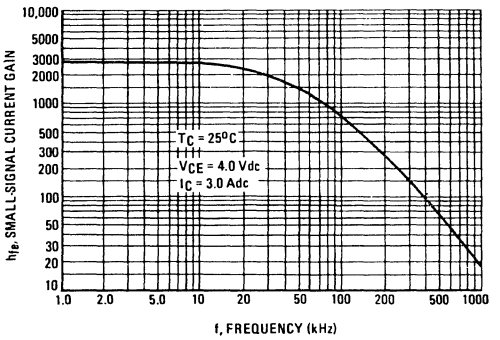


FIGURE 7 – CAPACITANCE

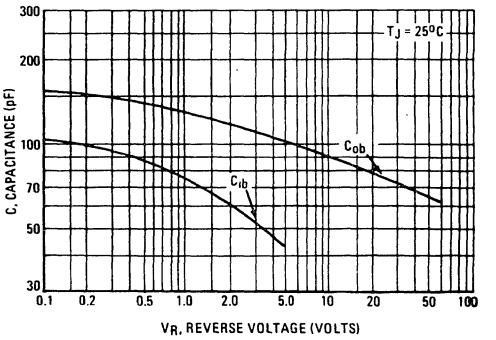


FIGURE 8 – DC CURRENT GAIN

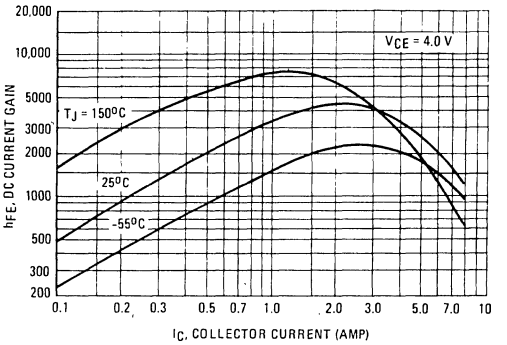


FIGURE 9 – COLLECTOR SATURATION REGION

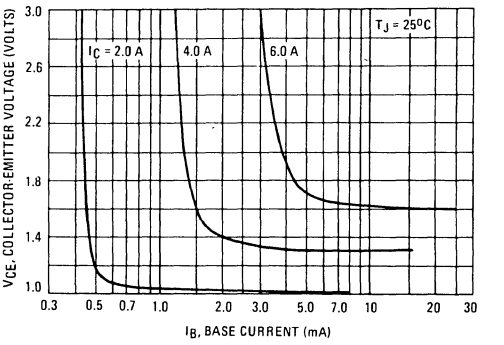


FIGURE 10 – "ON" VOLTAGES

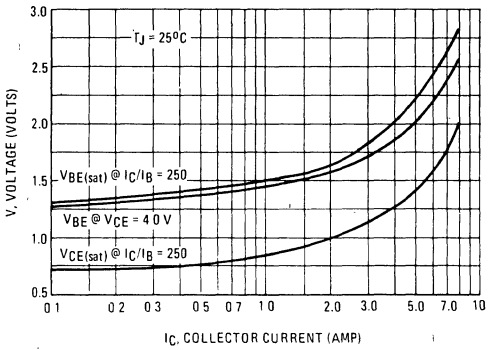


FIGURE 11 – TEMPERATURE COEFFICIENTS

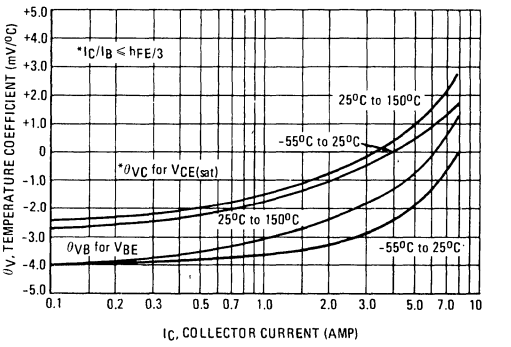


FIGURE 12 – COLLECTOR CUT-OFF REGION

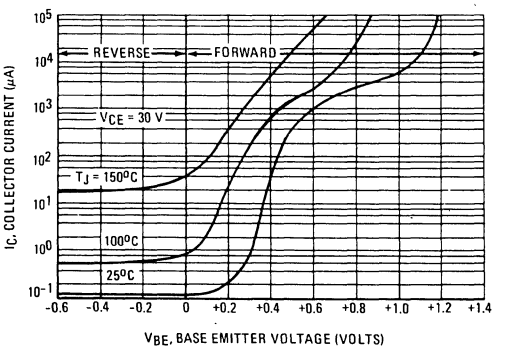
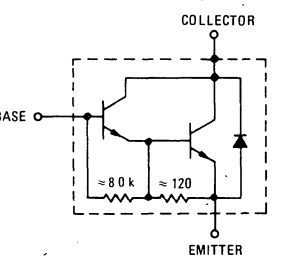


FIGURE 13 – DARLINGTON SCHEMATIC



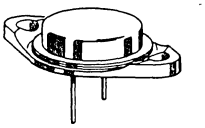
2N6436 (SILICON)
2N6437
2N6438

HIGH-POWER PNP SILICON TRANSISTORS

. . . designed for use in industrial-military power amplifier and switching circuit applications.

- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 80 Vdc (Min) — 2N6436
  = 100 Vdc (Min) — 2N6437
  = 120 Vdc (Min) — 2N6438
- High DC Current Gain —
  h_{FE} = 20-80 @ I_C = 10 Adc
  = 12 (Min) @ I_C = 25 Adc
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc
- Fast Switching Times @ I_C = 10 Adc
  t_r = 0.3 μs (Max)
  t_s = 1.0 μs (Max)
  t_f = 0.25 μs (Max)
- Complement to NPN 2N6338 thru 2N6341

25 AMPERE
POWER TRANSISTORS
PNP SILICON
80, 100, 120 VOLTS
200 WATTS



4

*MAXIMUM RATINGS

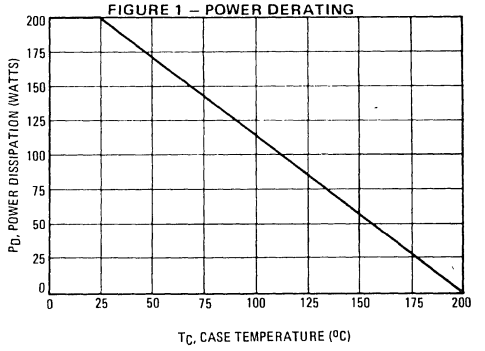
Rating	Symbol	2N6436	2N6437	2N6438	Unit
Collector-Base Voltage	V_{CB}	100	120	140	Vdc
Collector-Emitter Voltage	V_{CEO}	80	100	120	Vdc
Emitter-Base Voltage	V_{EB}	6.0			Vdc
Collector Current — Continuous Peak	I_C	25 50			Adc
Base Current	I_B	10			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14			Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200			°C

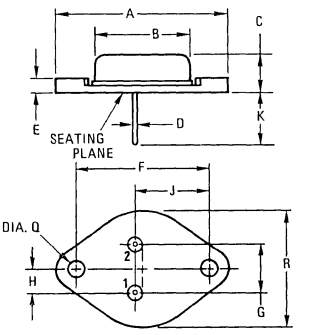
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	°C/W

*Indicates JEDEC Registered Data.

FIGURE 1 — POWER DERATING





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050

Collector connected to case.
CASE 11-01
(TO-3)

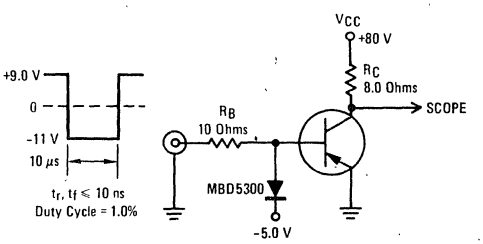
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 50 mAdc, I_B = 0)	2N6436		80	–	
	2N6437		100	–	
	2N6438		120	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N6436		–	50	
(V_{CE} = 50 Vdc, I_B = 0)	2N6437		–	50	
(V_{CE} = 60 Vdc, I_B = 0)	2N6438		–	50	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 90 Vdc, $V_{BE(off)}$ = -1.5 Vdc)	2N6436		–	10	
(V_{CE} = 110 Vdc, $V_{BE(off)}$ = -1.5 Vdc)	2N6437		–	10	
(V_{CE} = 130 Vdc, $V_{BE(off)}$ = -1.5 Vdc)	2N6438		–	10	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = -1.5 Vdc, T_C = 150°C)	2N6436		–	1.0	mAdc
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = -1.5 Vdc, T_C = 150°C)	2N6437		–	1.0	
(V_{CE} = 120 Vdc, $V_{BE(off)}$ = -1.5 Vdc, T_C = 150°C	2N6438		–	1.0	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 100 Vdc, I_E = 0)	2N6436		–	10	
(V_{CB} = 120 Vdc, I_E = 0)	2N6437		–	10	
(V_{CB} = 140 Vdc, I_E = 0)	2N6438		–	10	
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	–	100	μAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)			30	–	
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)			20	80	
(I_C = 25 Adc, V_{CE} = 2.0 Vdc)			12	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)			–	1.0	
(I_C = 25 Adc, I_B = 2.5 Adc)			–	1.8	
Base-Emitter Saturation Voltage (1)		$V_{BE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)			–	1.8	
(I_C = 25 Adc, I_B = 2.5 Adc)			–	2.5	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	40	–	MHz
Output Capacitance (V_{CE} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	700	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} = 80 Vdc, I_C = 10 A, $V_{BE(off)}$ = 6.0 Vdc, I_{B1} = 1.0 Adc)		t_r	–	0.3	μs
Storage (V_{CC} = 80 Vdc, I_C = 10 A, $V_{BE(off)}$ = 6.0 Vdc, I_{B1} = I_{B2} = 1.0 Adc)		t_s	–	1.0	μs
Fall Time (V_{CC} = 80 Vdc, I_C = 10 A, $V_{BE(off)}$ = 6.0 Vdc, I_{B1} = I_{B2} = 1.0 Adc)		t_f	–	0.25	μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



Note: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

FIGURE 3 – TURN-ON TIME

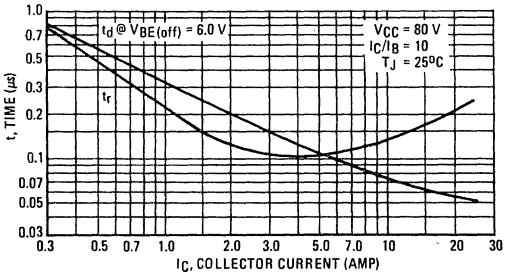
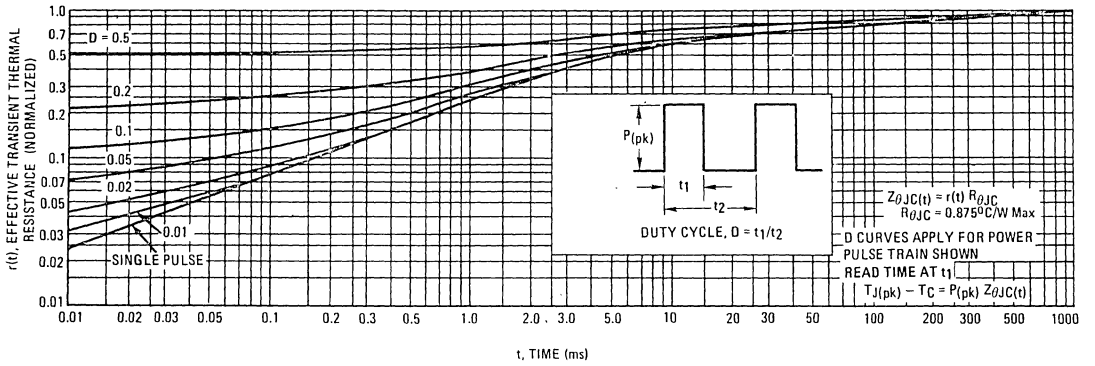
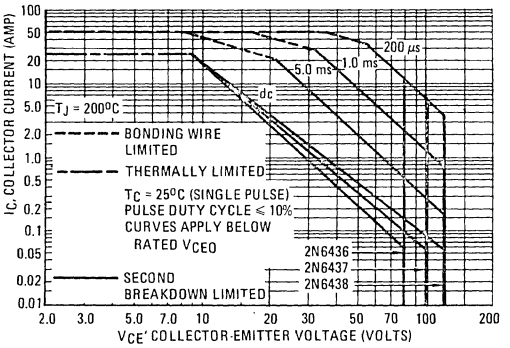


FIGURE 4 – THERMAL RESPONSE



4

FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

FIGURE 6 – TURN-OFF TIME

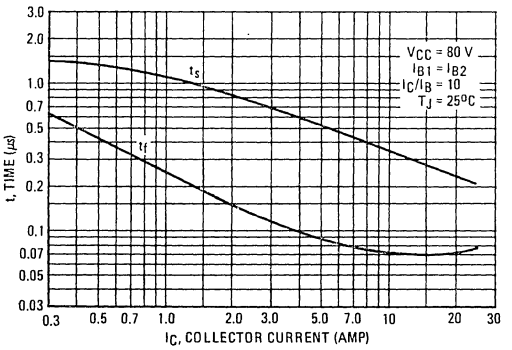


FIGURE 7 – CAPACITANCE

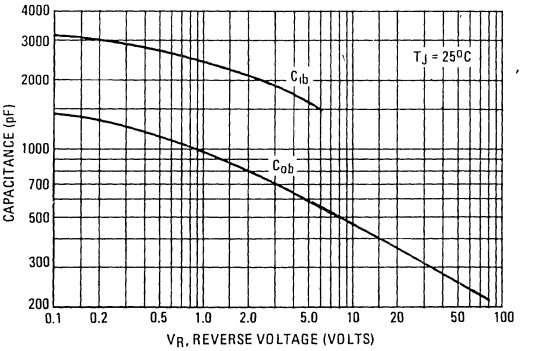


FIGURE 8 – DC CURRENT GAIN

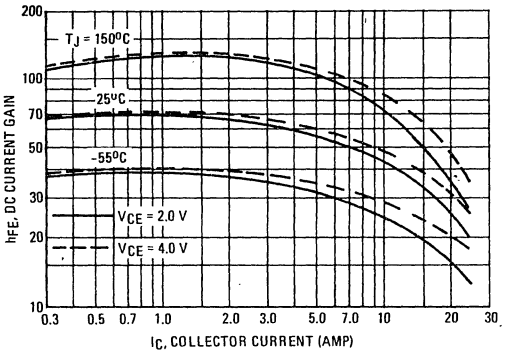


FIGURE 9 – COLLECTOR SATURATION REGION

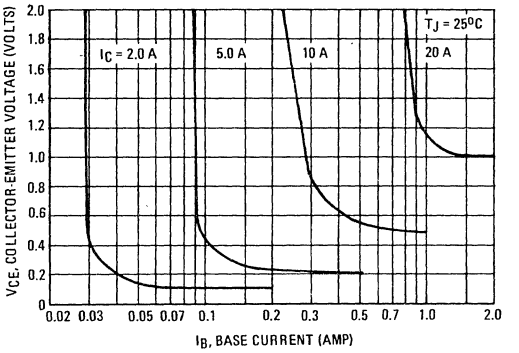


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FIGURE 10 – "ON" VOLTAGE

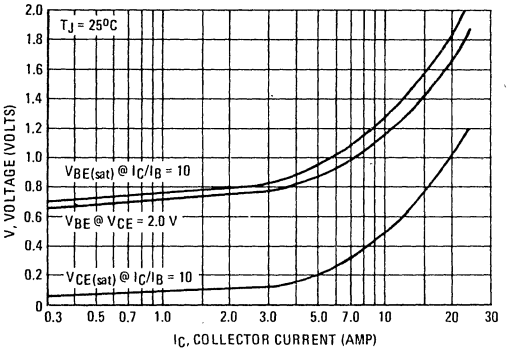


FIGURE 11 – TEMPERATURE COEFFICIENTS

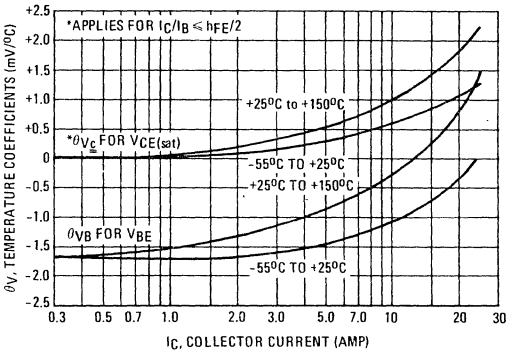


FIGURE 12 – COLLECTOR CUT-OFF REGION

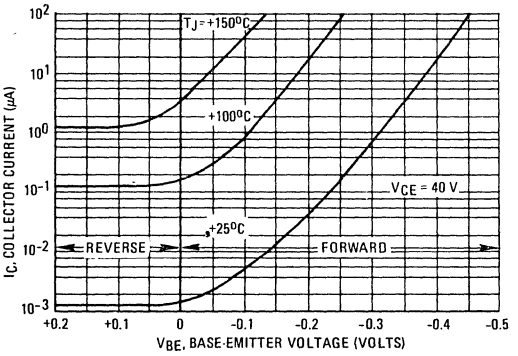
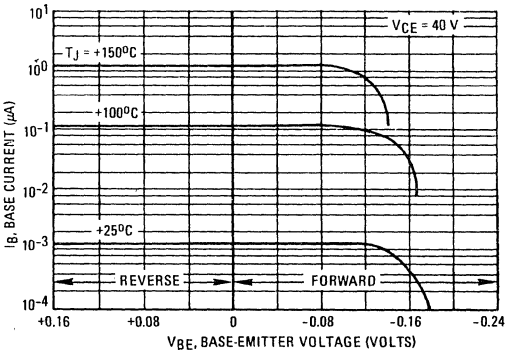


FIGURE 13 – BASE CUT-OFF REGION



2N6486 2N6487 2N6488 NPN
2N6489 2N6490 2N6491 PNP

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

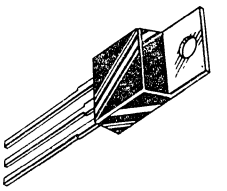
. . . designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 15 Amperes
  h_{FE} = 20–150 @ I_C = 5.0 Adc
  = 5.0 (Min) @ I_C = 15 Adc
- Collector-Emitter Sustaining Voltage –
  $V_{CEO\ (sus)}$ = 40 Vdc (Min) – 2N6486, 2N6489
  = 60 Vdc (Min) – 2N6487, 2N6490
  = 80 Vdc (Min) – 2N6488, 2N6491
- High Current Gain – Bandwidth Product
  f_T = 5.0 MHz (Min) @ I_C = 1.0 Adc
- TO-220AB Compact Package
- TO-66 Leadform Also Available

15 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

40-60-80 VOLTS
75 WATTS



4

***MAXIMUM RATINGS**

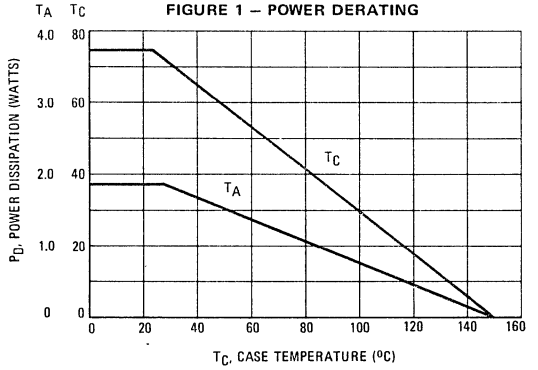
Rating	Symbol	2N6486 2N6489	2N6487 2N6490	2N6488 2N6491	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	50	70	90	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous	I_C	15			Adc
Base Current	I_B	5.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.8 0.014			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			°C

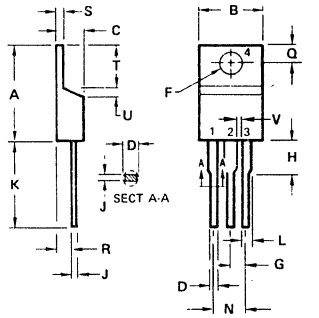
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W

*Indicates JEDEC Registered Data

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–

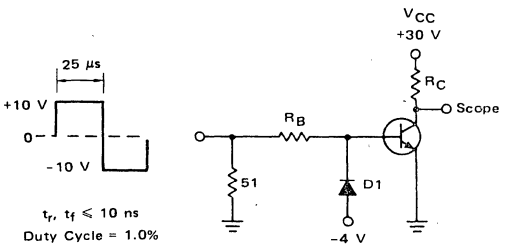
CASE 221A-02
TO-220AB

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N6486, 2N6489		40	–	
	2N6487, 2N6490		60	–	
	2N6588, 2N6491		80	–	
Collector-Emitter Sustaining Voltage (1)		V_{CEX}			Vdc
(I_C = 200 mAdc, V_{BE} = 1.5 Vdc)	2N6486, 2N6489		50	–	
	2N6487, 2N6490		70	–	
	2N6488, 2N6491		90	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N6486, 2N6489		–	1.0	
(V_{CE} = 30 Vdc, I_B = 0)	2N6487, 2N6490		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N6488, 2N6491		–	1.0	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6486, 2N6489		–	500	
(V_{CE} = 65 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6487, 2N6490		–	500	
(V_{CE} = 85 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6488, 2N6491		–	500	
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6486, 2N6489		–	5.0	mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6487, 2N6490		–	5.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6488, 2N6491		–	5.0	
Emitter Cutoff Current		I_{EBO}	–	1.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)			20	150	
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)			5.0	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 0.5 Adc)			–	1.3	
(I_C = 15 Adc, I_B = 5.0 Adc)			–	3.5	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)			–	1.3	
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)			–	3.5	
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2)		f_T	5.0	–	MHz
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 MHz)					
Small-Signal Current Gain		h_{fe}	25	–	–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)					

*Indicates JEDEC Registered Data.
(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2)$f_T = |h_{fe}| \cdot f_{test}$.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C varied to obtain desired current levels.
For PNP reverse all polarities.

D1 must be fast recovery type, e.g.;
MBD5300 used above $I_B \approx 100$ mA
MSD6100 used below $I_B \approx 100$ mA

FIGURE 3 – TURN-ON TIME

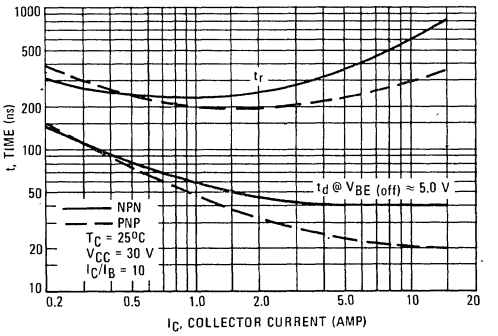
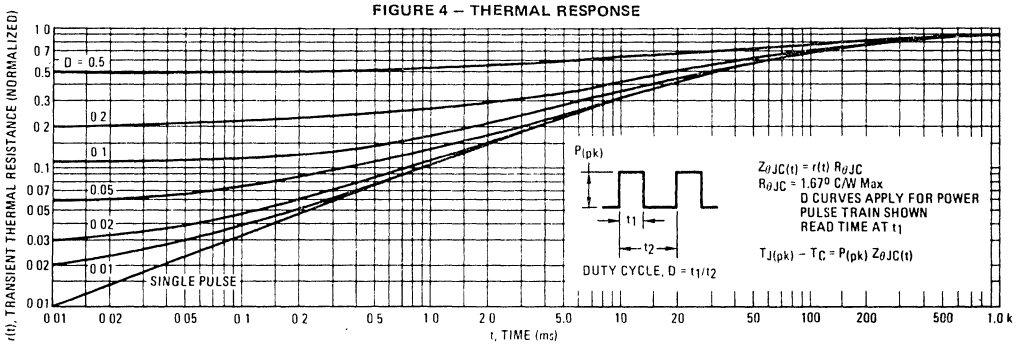
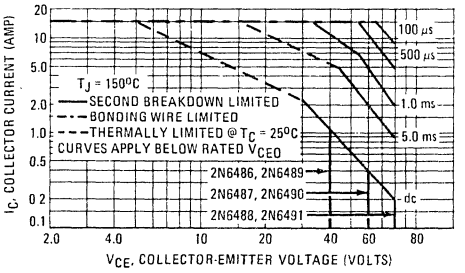


FIGURE 4 – THERMAL RESPONSE



4

FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

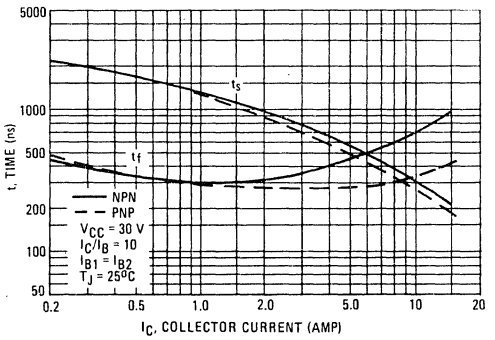
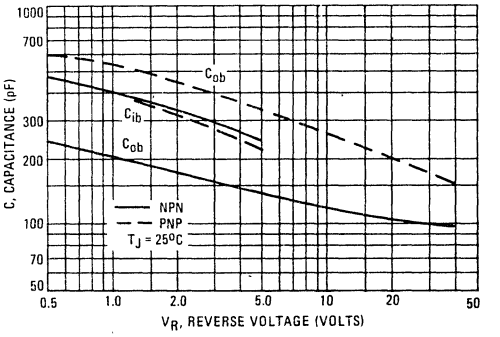


FIGURE 7 – CAPACITANCES

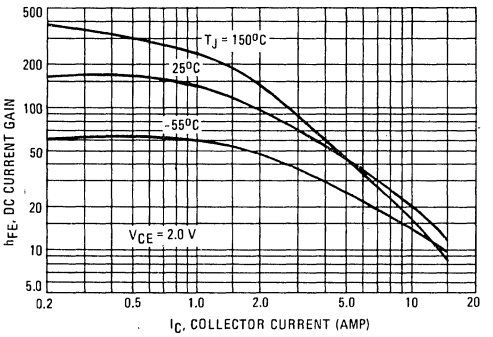


4

NPN
2N6486, 2N6487, 2N6488

PNP
2N6489, 2N6490, 2N6491

FIGURE 8 – DC CURRENT GAIN



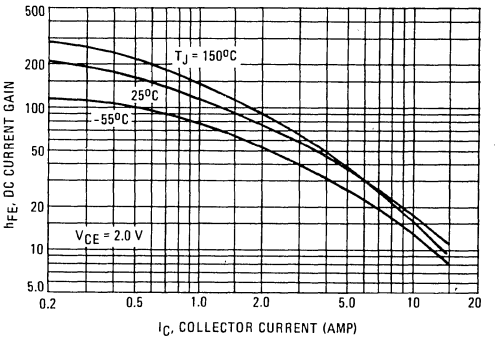
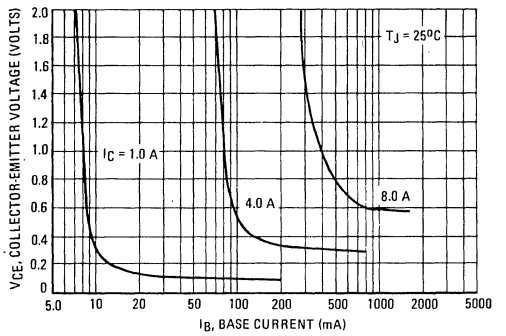


FIGURE 9 – COLLECTOR SATURATION REGION



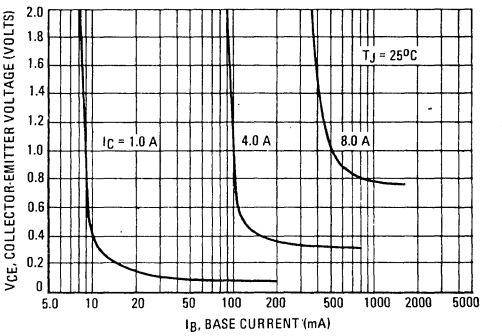
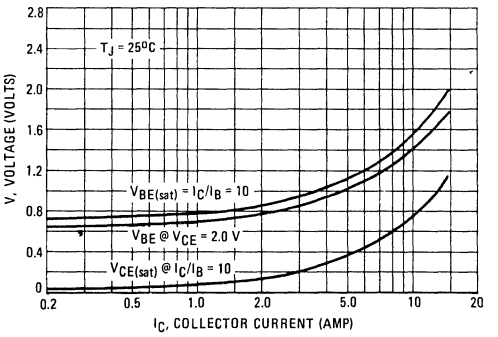
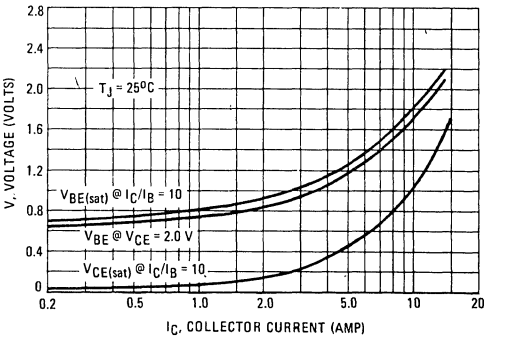


FIGURE 10 – "ON" VOLTAGES

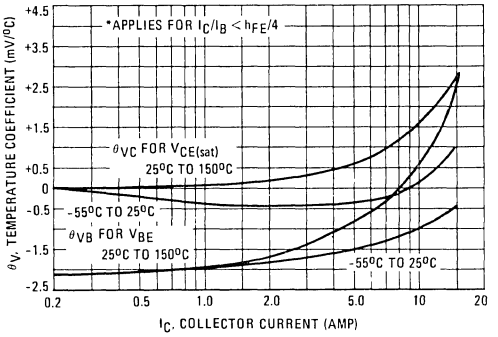




NPN
2N6486, 2N6487, 2N6488

PNP
2N6489, 2N6490, 2N6491

FIGURE 11 – TEMPERATURE COEFFICIENTS



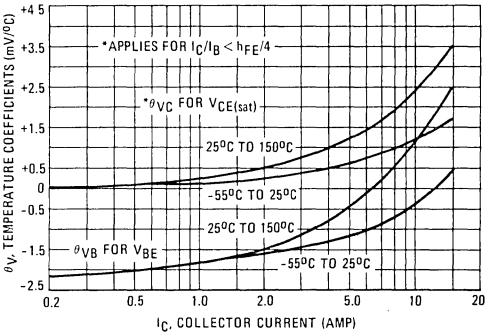
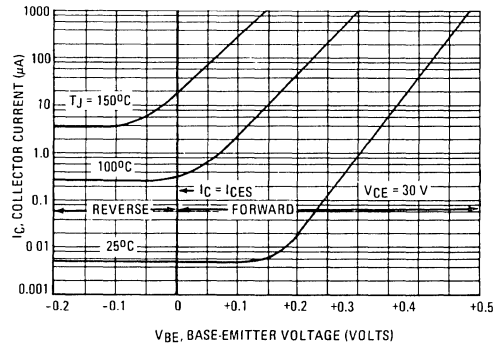


FIGURE 12 – COLLECTOR CUTOFF REGION



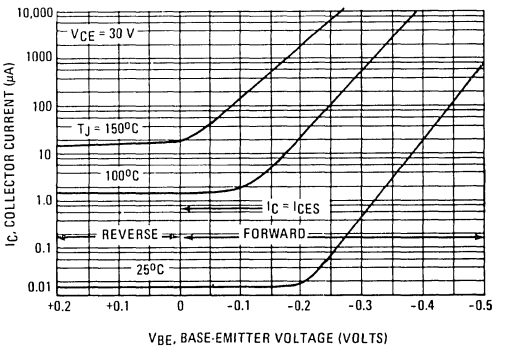
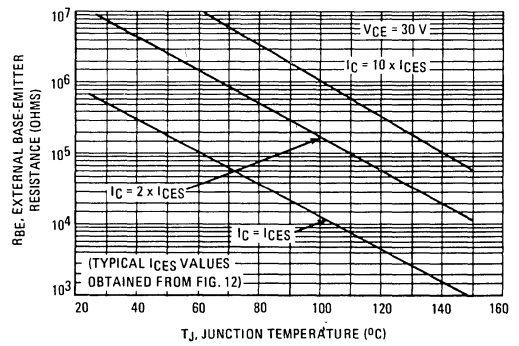
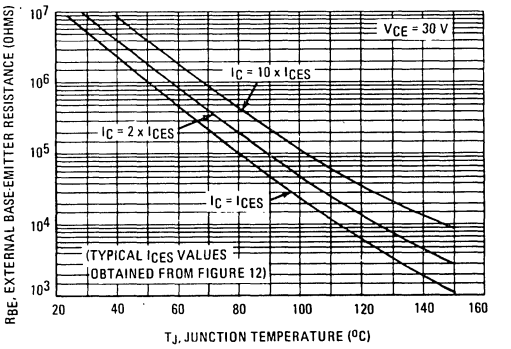


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE





2N6495 NPN

NPN SILICON POWER SWITCHING TRANSISTOR

Double Diffused epitaxial mesa technology combining high-speed switching with rugged power handling capability.

- High-Speed Switching Times –
  t_{on} = 350 ns (Max)
  t_{off} = 350 ns (Max)
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.75 Vdc (Max) @ I_C = 5.0 Adc
  = 1.5 Vdc (Max) @ I_C = 10 Adc
- Current-Gain–Bandwidth Product –
  f_T = 15 MHz (Typ) @ I_C = 5.0 Adc (See Figure 1)
- High Safe Operating Area – Full Power Rated to V_{CE} = 20 Vdc

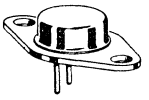
Designed for Use in:

- Switching Control Amplifiers
- Switching Regulators
- Converters
- Inverters
- Power Oscillators

10 AMPERE
POWER TRANSISTOR

NPN SILICON

80 VOLTS
70 WATTS



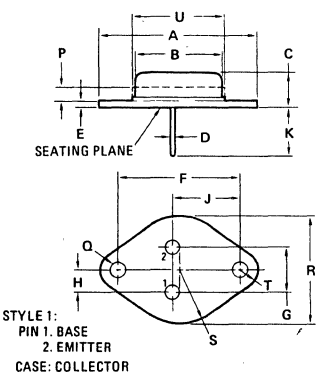
*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	80	Vdc
Collector-Base Voltage	V_{CB}	150	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current – Continuous – Peak	I_C	10 20	Adc
Base Current	I_B	5.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	70 0.4	Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W

*Indicates JEDEC Registered Data.

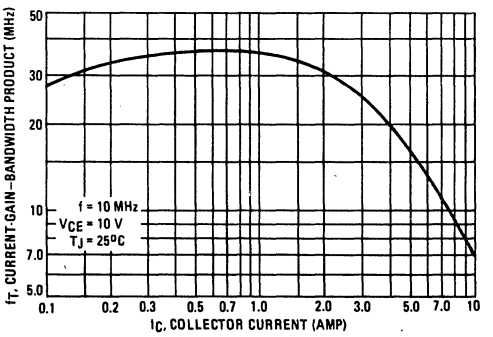


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

All JEDEC Dimensions and and Notes Apply.

CASE 80-02
TO-66

FIGURE 1 – CURRENT-GAIN–BANDWIDTH PRODUCT

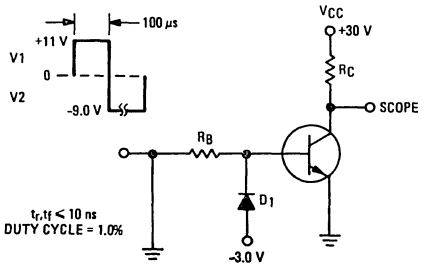


***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	80	–	Vdc
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	–	100	μAdc
(V_{CE} = 70 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 200°C)		–	5.0	mAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	100	nAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc)	h_{FE}	10	60	–
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$	–	1.5	Vdc
(I_C = 5.0 Adc, I_B = 1.0 Adc)		–	0.75	
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)	$V_{BE(sat)}$	–	2.2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 10 MHz)	f_T	25	–	MHz
SWITCHING CHARACTERISTICS				
Turn-On Time (V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = 1.0 Adc)	t_{on}	–	350	ns
Turn-Off Time (V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	t_{off}	–	350	ns

*Indicates JEDEC Registered Data.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA
FOR t_d and t_r, D1 IS DISCONNECTED AND V_2 = 0.

FIGURE 3 – TURN-ON TIME

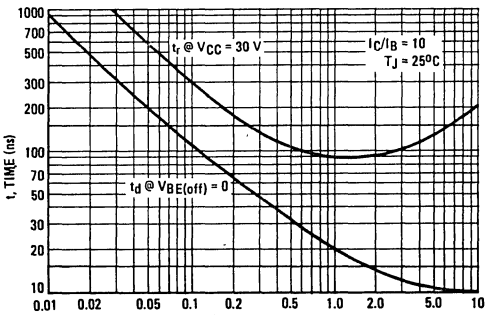
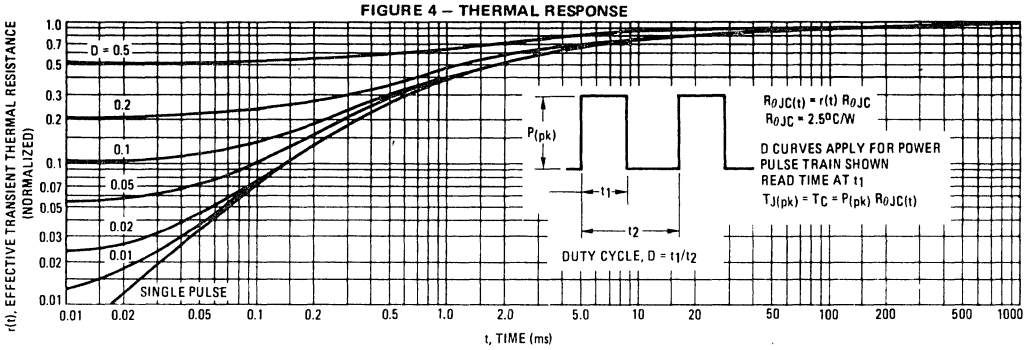


FIGURE 4 – THERMAL RESPONSE



4

FIGURE 5 – ACTIVE-REGION SAFE-OPERATING AREA

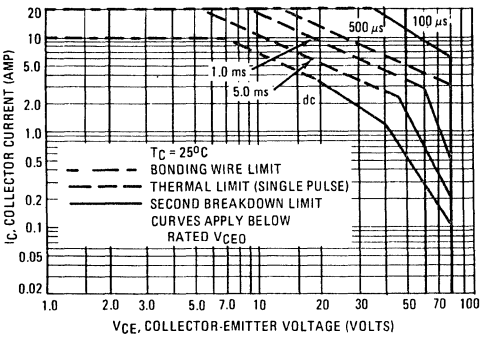
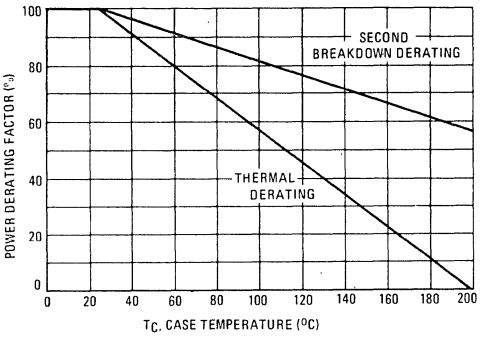


FIGURE 6 – POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 6.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 5 may be found at any case temperature by using the appropriate curve on Figure 6.

FIGURE 7 – TURN-OFF TIME

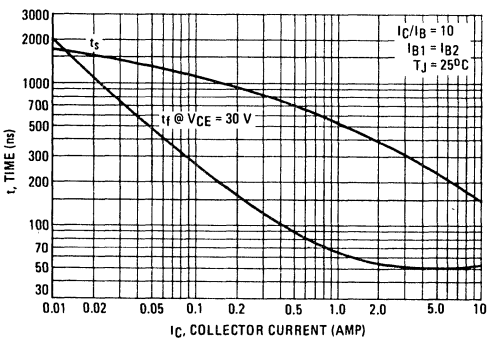


FIGURE 8 – CAPACITANCE

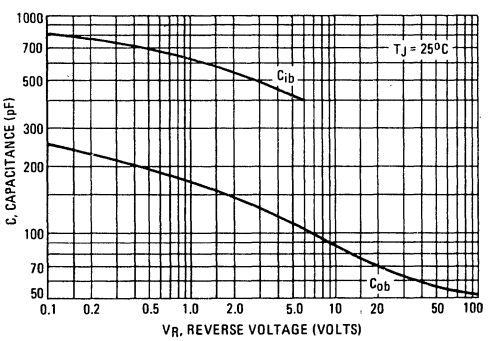


FIGURE 9 – DC CURRENT GAIN

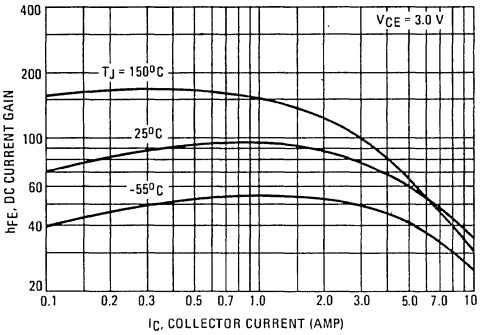


FIGURE 10 – COLLECTOR SATURATION REGION

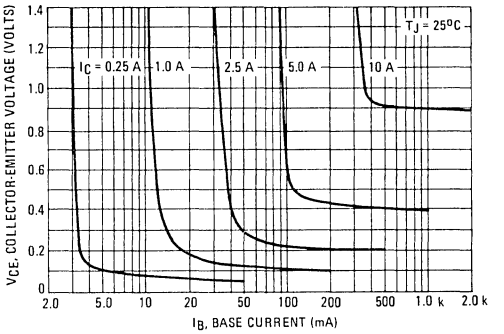


FIGURE 11 "ON" VOLTAGE

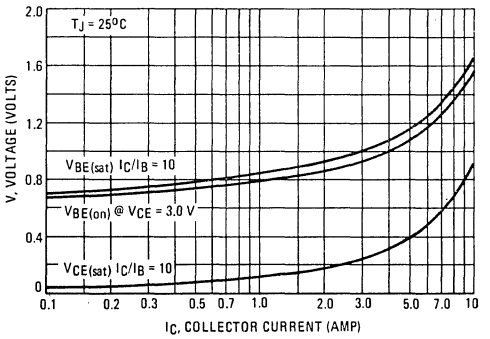


FIGURE 12 – TEMPERATURE COEFFICIENT

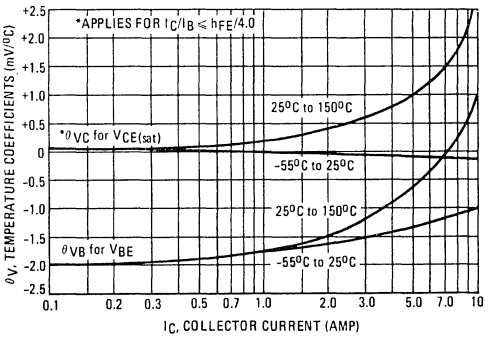


FIGURE 13 – COLLECTOR CUTOFF REGION

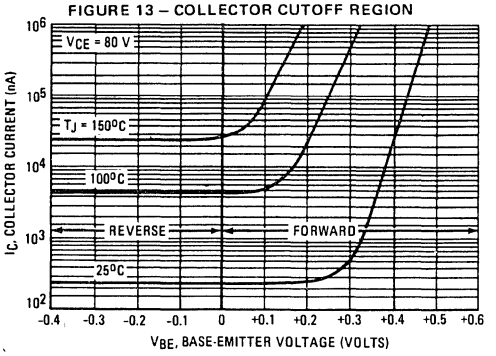
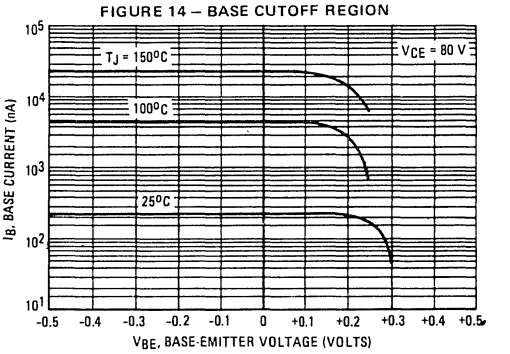


FIGURE 14 – BASE CUTOFF REGION



2N6497
2N6498
2N6499

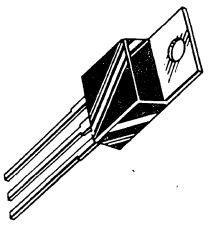
HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

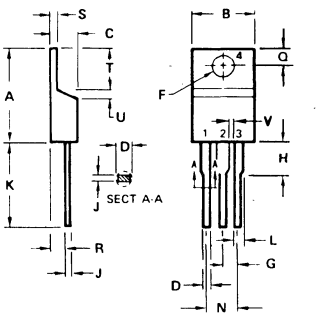
· · · designed for high voltage inverters, switching regulators and line-operated amplifier applications. Especially well suited for switching power supply applications.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 250 Vdc (Min) – 2N6497
  = 300 Vdc (Min) – 2N6498
  = 350 Vdc (Min) – 2N6499
- Excellent DC Current Gain –
  h_{FE} = 10 – 75 @ I_C = 2.5 Adc
- Low Collector-Emitter Saturation Voltage @ I_C = 2.5 Adc –
  $V_{CE(sat)}$ = 1.0 Vdc (Max) – 2N6497
  = 1.25 Vdc (Max) – 2N6498
  = 1.5 Vdc (Max) – 2N6499

5 AMPERE
POWER TRANSISTORS
NPN SILICON

250, 300, 350 VOLTS
80 WATTS





STYLE 1
PIN 1 BASE
2 COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–

CASE 221A-02
TO-220AB

*MAXIMUM RATINGS

Rating	Symbol	2N6497	2N6498	2N6499	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
Collector-Base Voltage	V_{CB}	350	400	450	Vdc
Emitter-Base Voltage	V_{EB}	← 6.0 →			Vdc
Collector Current – Continuous – Peak	I_C	← 5.0 → ← 10 →			Adc
Base Current	I_B	← 2.0 →			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 80 → ← 0.64 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	← -65 to +150 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W

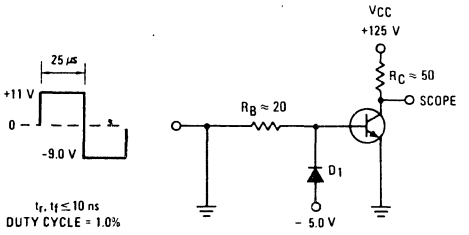
*Indicates JEDEC Registered Data.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$				Vdc
(I_C = 25 mAdc, I_B = 0)	2N6497		250	–	–	
	2N6498		300	–	–	
	2N6499		350	–	–	
Collector Cutoff Current		I_{CEX}				mAdc
(V_{CE} = 350 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6497		–	–	1.0	
(V_{CE} = 400 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6498		–	–	1.0	
(V_{CE} = 450 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6499		–	–	1.0	
(V_{CE} = 175 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	2N6497		–	–	10	
(V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	2N6498		–	–	10	
(V_{CE} = 225 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	2N6499		–	–	10	
Emitter Cutoff Current		I_{EBO}	–	–	1.0	mAdc
(V_{BE} = 6.0 Vdc, I_C = 0)						
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}				–
(I_C = 2.5 Adc, V_{CE} = 10 Vdc)			10	–	75	
(I_C = 5.0 Adc, V_{CE} = 10 Vdc)			3.0	–	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 2.5 Adc, I_B = 500 mAdc)	2N6497		–	–	1.0	
	2N6498		–	–	1.25	
	2N6499		–	–	1.5	
(I_C = 5.0 Adc, I_B = 2.0 Adc)	All Devices		–	–	5.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 2.5 Adc, I_B = 500 mAdc)			–	–	1.5	
(I_C = 5.0 Adc, I_B = 2.0 Adc)			–	–	2.5	
DYNAMIC CHARACTERISTICS						
Current-Gain–Bandwidth Product		f_T	5.0	–	–	MHz
(I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)						
Output Capacitance		C_{ob}	–	–	150	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)						
SWITCHING CHARACTERISTICS						
Rise Time		t_r	–	0.4	0.8	μs
(V_{CC} = 125 Vdc, I_C = 2.5 Adc, I_{B1} = 0.5 Adc)						
Storage Time		t_s	–	1.4	1.8	μs
(V_{CC} = 125 Vdc, I_C = 2.5 Adc, V_{BE} = 5.0 Vdc, I_{B1} = I_{B2} = 0.5 Adc)						
Fall Time		t_f	–	0.45	0.8	μs
(V_{CC} = 125 Vdc, I_C = 2.5 Adc, I_{B1} = I_{B2} = 0.5 Adc)						

*Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE I_B ≈ 100 mA
MSD6100 USED BELOW I_B ≈ 100 mA

FIGURE 2 – TURN-ON TIME

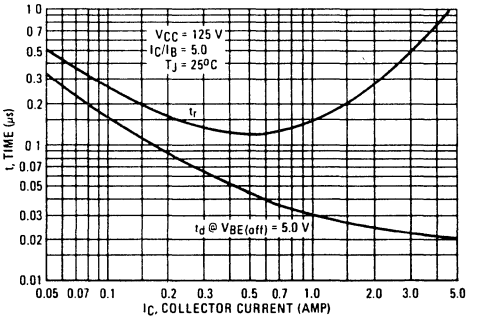


FIGURE 3 – THERMAL RESPONSE

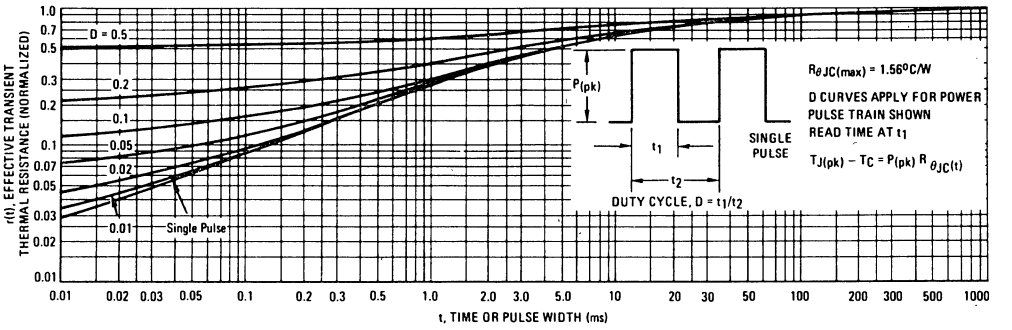
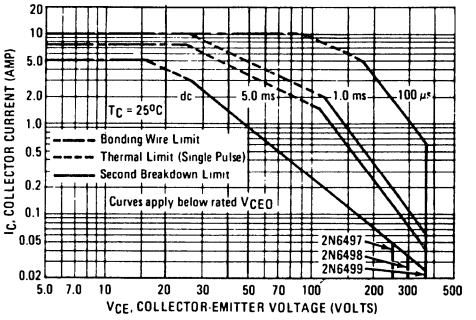


FIGURE 4 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 4 may be found at any case temperature by using the appropriate curve on Figure 6.

FIGURE 5 – TURN-OFF TIME

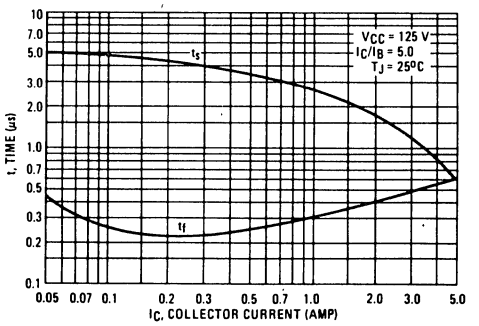


FIGURE 6 – POWER DERATING

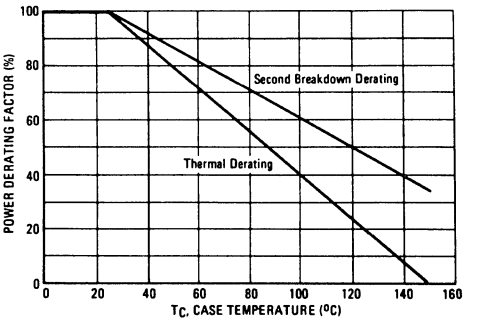


FIGURE 7 – DC CURRENT GAIN

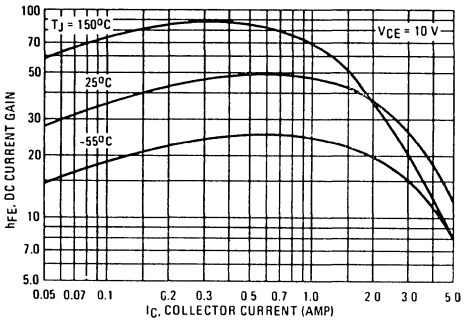


FIGURE 8 – COLLECTOR SATURATION REGION

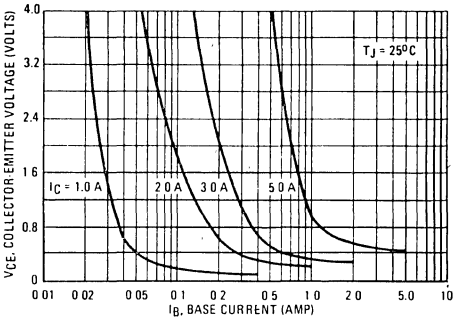


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FIGURE 9 – "ON" VOLTAGES

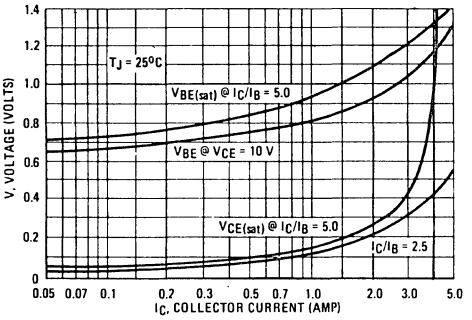


FIGURE 10 – TEMPERATURE COEFFICIENTS

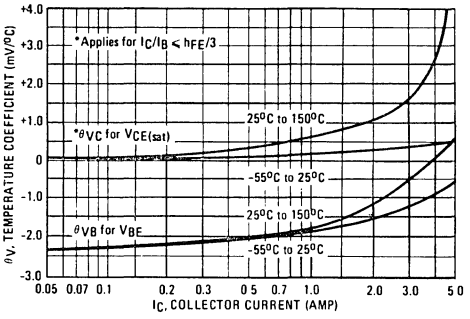


FIGURE 11 – COLLECTOR CUTOFF REGION

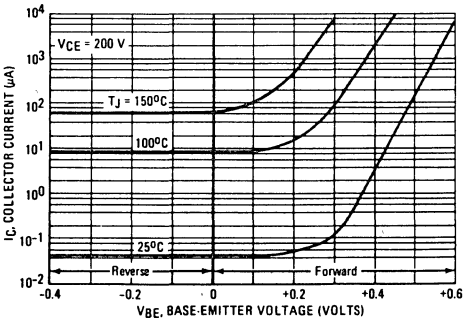
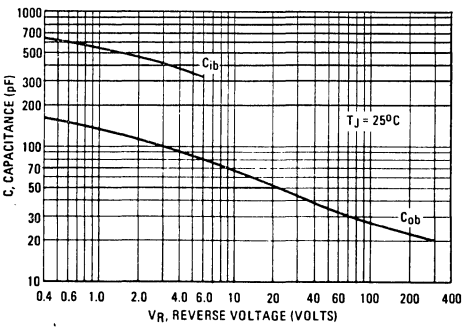


FIGURE 12 – CAPACITANCE



2N6542
2N6543

Designers Data Sheet

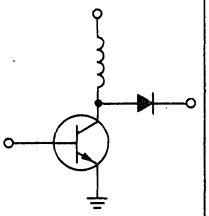
SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The 2N6542 and 2N6543 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for 115 and 220 volt line operated switch-mode applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

Specification Features –

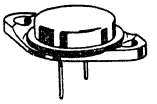
High Temperature Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents

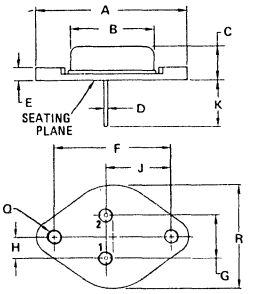


5 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
100 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-03
TO-3

***MAXIMUM RATINGS**

Rating	Symbol	2N6542	2N6543	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	350	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	850	Vdc
Emitter Base Voltage	V_{EB}	9.0		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	5.0 10		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	5.0 10		Adc
Emitter Current – Continuous – Peak (1)	I_E I_{EM}	10 20		Adc
Total Power Dissipation @ $T_C = 25^oC$ @ $T_C = 100^oC$ Derate above 25^oC	P_D	100 57.2 0.57		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	^oC

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mA, I_B = 0)	2N6542		300	–	
	2N6543		400	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 13)		$V_{CEX(sus)}$			Vdc
(I_C = 2.6 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	2N6542		350	–	
	2N6543		450	–	
(I_C = 5.0 Adc, V_{clamp} = Rated V_{CEO} -100 V,	2N6542		200	–	
T_C = 100°C)	2N6543		300	–	
Collector Cutoff Current		I_{CEV}			mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	0.5	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C			–	3.0	
Collector Cutoff Current		I_{CER}	–	3.0	mAdc
(V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)					
Emitter Cutoff Current		I_{EBO}	–	1.0	mAdc
(V_{EB} = 9.0 Vdc, I_C = 0)					
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	0.2	–	Adc
t = 1.0 s (non-repetitive) (V_{CE} = 100 Vdc)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)			12	60	
(I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)			7.0	35	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 0.6 Adc)			–	1.0	
(I_C = 5.0 Adc, I_B = 1.0 Adc)			–	5.0	
(I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)			–	2.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 0.6 Adc)			–	1.4	
(I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C			–	1.4	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	6.0	28	MHz
(I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)					
Output Capacitance		C_{ob}	50	200	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)					
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	(V_{CC} = 250 Vdc, I_C = 3.0 A, I_{B1} = I_{B2} = 0.6 A, t_p = 100 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.05	μs
Rise Time		t_r	–	0.7	μs
Storage Time		t_s	–	4.0	μs
Fall Time		t_f	–	0.8	μs
Inductive Load, Clamped (Table 1)					
Storage Time	(I_C = 3.0 A(pk), V_{clamp} = Rated V_{CEX},	t_s	–	4.0	μs
Fall Time	I_{B1} = 0.6 A, $V_{BE(off)}$ = 5.0 Vdc , T_C = 100°C)	t_f	–	0.8	μs
			Typical		
Storage Time	(I_C = 3.0 A(pk), V_{clamp} = Rated V_{CEX},	t_s	1.1		μs
Fall Time	I_{B1} = 0.6 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_f	0.12		μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

4

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

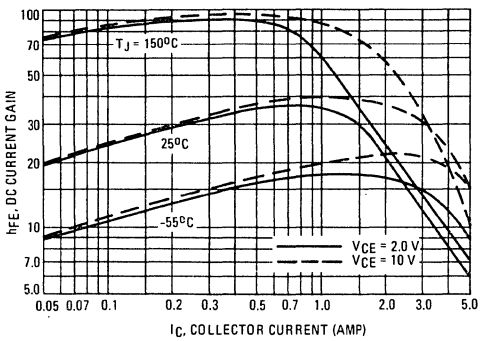


FIGURE 2 – COLLECTOR SATURATION REGION

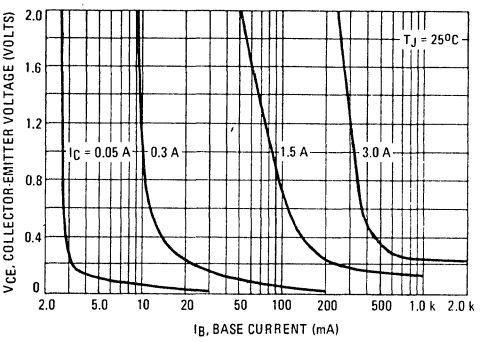


FIGURE 3 – "ON" VOLTAGE

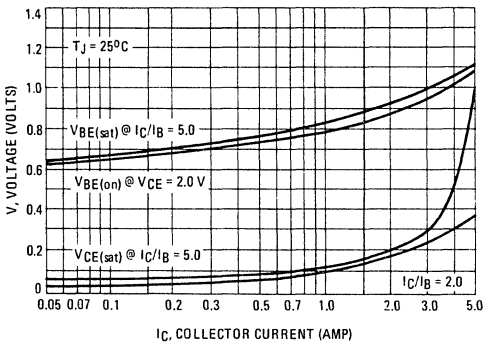


FIGURE 4 – TEMPERATURE COEFFICIENTS

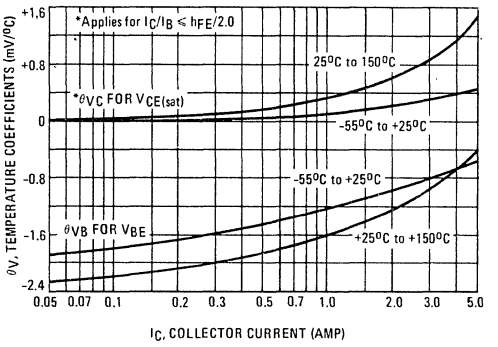


FIGURE 5 – COLLECTOR CUTOFF REGION

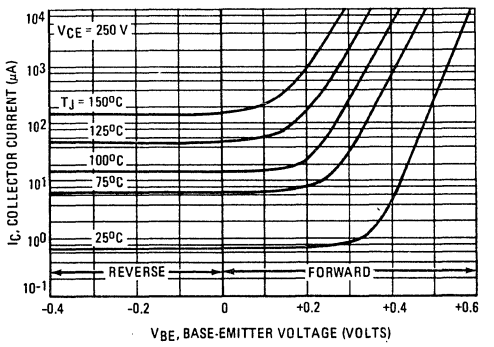


FIGURE 6 – CAPACITANCE

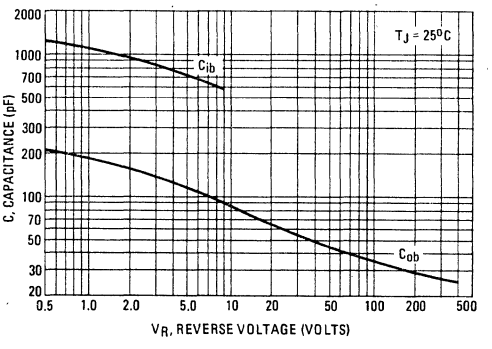
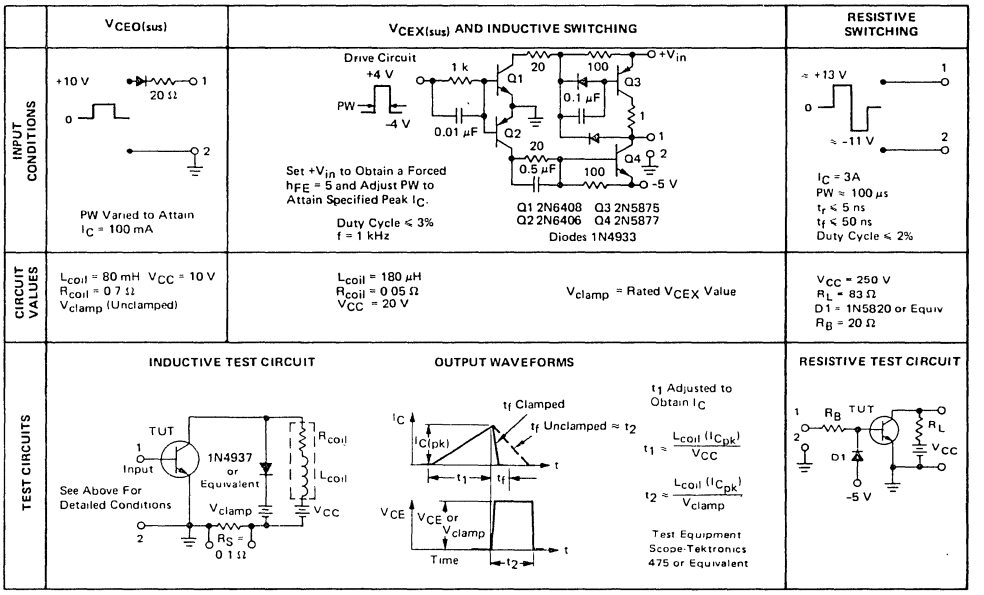


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE



DESIGNERS INFORMATION FOR APPLICATIONS AND SWITCHMODE SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for switch-mode applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in switch-mode applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 12) are the proper design limits.

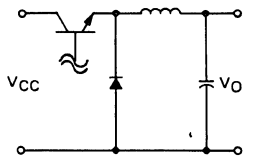
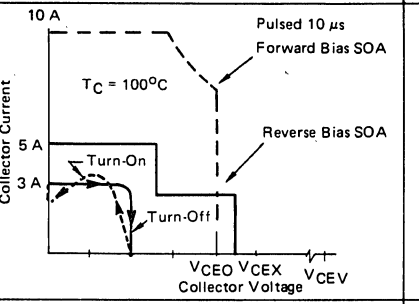
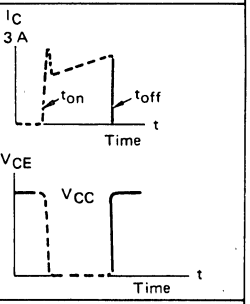
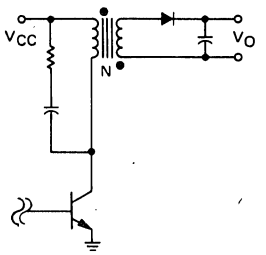
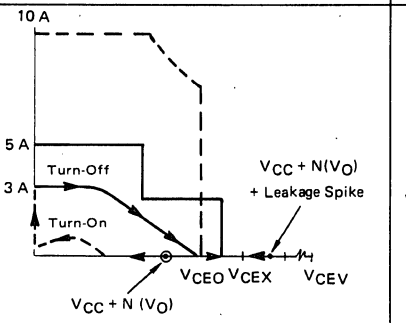
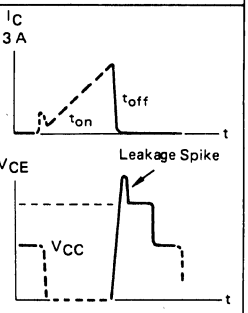
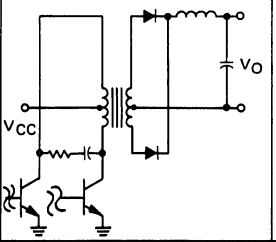
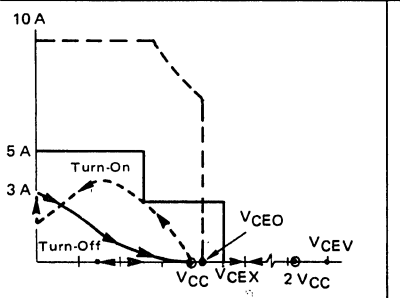
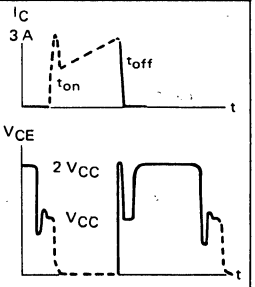
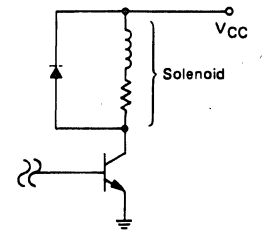
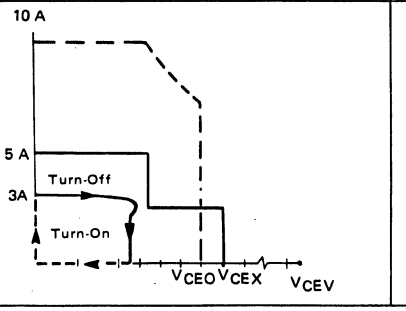
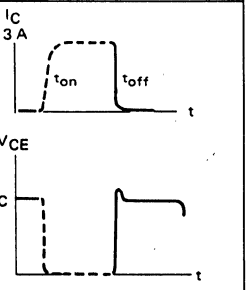
For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given high collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

As shown on the reverse bias SOA curve in Figure 13, two voltage levels are specified, one at the maximum continuous current level and one near the recommended operating level so that both normal and fault/transient

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-588, AN-719, AN-737, AN-752, AN-767

4

TABLE 2 – APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	SERIES SWITCHING REGULATOR 		
B	RINGING CHOKE INVERTER 		
C	PUSH-PULL INVERTER/CONVERTER 		
D	SOLENOID DRIVER 		

conditions can be taken into consideration. In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves. Note that the boundary along the $I_C = 0$ axis extends to V_{CEV}.

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output reactifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to limit the leakage spike to $< V_{CEX(sus)}$ during turn-off and $< V_{CEV}$ after turn-off (i.e. @ $I_C \leqslant I_{CEV}$).

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.

(2) The turn-on time or pulse width does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 12).

(3) The base drive conditions are similar to those specified on the data sheet (See Table 1), i.e., $V_{BE(off)} \leqslant 5$ V.

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 3 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_f). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 8 and Table 3 and resistive loads in Figures 9 and 10. Usually the inductive load component will be the dominant factor in switch-mode applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

SECONDARY BREAKDOWN REQUIRMENTS

Secondary breakdown capability is important in switching applications because of the turn-on and turn-off conditions that can exist during the switching cycle. Typically, forward biased secondary breakdown ($I_{S/b}$) is not a problem in switching applications because of the relatively higher current capability in the forward biased mode. The forward biased SOA curves provide adequate information for these conditions.

Reverse biased secondary breakdown ($E_{S/b}$) is quite different and a more complex situation from both design and specification standpoint. The $E_{S/b}$ rating is intended to define the amount of energy that the device can absorb while it is in a reverse biased avalanche mode (unclamped). The major problems in specifying $E_{S/b}$ are:

(1) Individual device capability can vary by more than an order of magnitude within the same production lot.

(2) Energy handling capability is not constant within the same device family when the test conditions are changed.

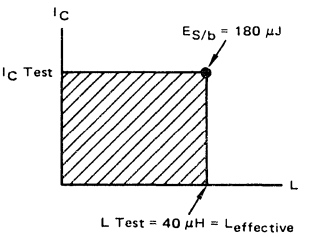
(3) $E_{S/b}$ testing is often destructive when a device actually goes into secondary breakdown.

(4) Some device families exhibit very limited capability in the avalanche condition.

(5) Depending on the device and test conditions, some devices may not reach the avalanche condition during the test.

For these reasons, the most reliable design approach is to avoid this mode of operation by clamping or snubbing the main inductive load component and minimizing leakage inductance whenever possible. The $E_{S/b}$ specification does provide a boundary condition represented in Figure 7.

FIGURE 7 – COLLECTOR CURRENT versus UNCLAMPED LOAD INDUCTANCE



Operation with an unclamped inductance is safe within the shaded area provided the base drive conditions are similar to or less severe than the specified conditions shown in Table 1, i.e., $V_{BE(off)} \leqslant 4$ V, $R_{BE} \geqslant 50\ \Omega$ and

$$L_{effective} = \frac{L_L(V_{CEX})}{V_{CEX}-V_{CC}}$$

where L_L = Circuit Leakage Reactance

TEMPERATURE REQUIREMENTS

The important parameters on this data sheet have been specified at a case temperature of 100°C to represent a recommended worst case design condition.

FIGURE 8 – TURN-OFF WAVEFORM

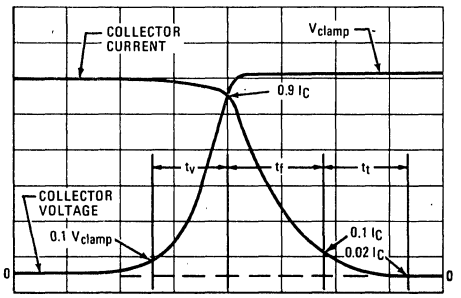


TABLE 3 – INDUCTIVE SWITCHING PERFORMANCE

I_C (A)	T_C °C	t_s µs	t_v µs	t_f µs	t_t µs	$t_v+t_f+t_t$ µs
1.0	25	0.70	0.22	0.21	0.23	0.66
	100	1.20	0.37	0.19	0.39	0.95
3.0	25	1.10	0.09	0.12	0.08	0.29
	100	1.60	0.42	0.19	0.40	1.01
5.0	25	1.10	0.16	0.19	0.11	0.46
	100	1.70	0.45	0.37	0.26	1.08

Note: All Data Recorded in the Inductive Switching Circuit Shown in Table 1.

To facilitate volume production testing, maximum inductive switching limits for these transistors are specified using conventional measurement techniques, e.g. t_s(max) is measured from the point where I_{B1} has decreased 10% to the point where I_C has decreased 10%, and t_f(max) is measured between the 90% and 10% points on the I_C waveform. In most applications, a large percentage of the total device power dissipation occurs during the fall time and t_f is normally used as a figure of merit when choosing a device for a switch-mode application. However, there are two portions of the turn-off waveform that can add losses and in some cases these losses can become a significant portion of the total device dissipation.

Figure 8 shows an enlarged portion of the inductive switching waveform during turn-off. The interval labeled t_v is part of the storage time interval (t_s) and is defined as voltage switching time. During this interval the transistor collector to emitter voltage changes from a saturation level to a level equal to or approaching the clamp voltage while the collector current has only changed by 10%. Typical values for this time interval at various current levels are shown in Table 3 at 25°C and 100°C case temperature.

The time interval labeled t_t occurs after the fall time and appears as a "tail" on the trailing edge of the collector current waveform. It is measured, for this discussion, from the 10% point to the 2% point; and during this interval the collector to emitter voltage is equal to the clamp voltage. Typical values for these time intervals are also shown in Table 3.

Since power dissipation occurs during the total time period $t_v + t_f + t_t$ and each interval can be affected by external conditions, some applications may require a specific analysis in order to accurately predict total device dissipation.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON TIME

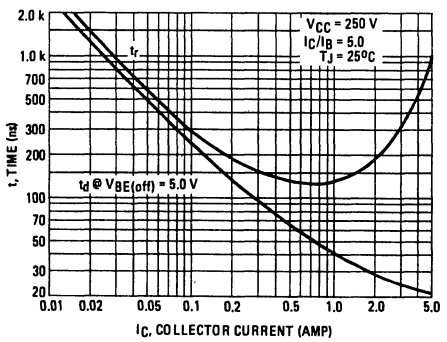


FIGURE 10 – TURN-OFF TIME

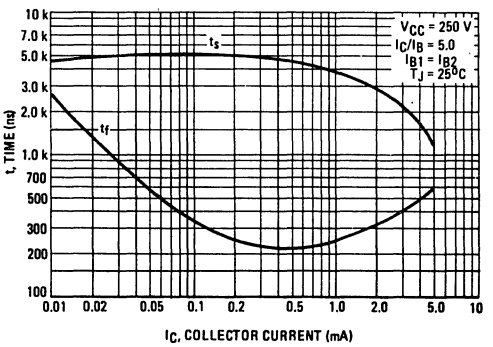


FIGURE 11 – THERMAL RESPONSE

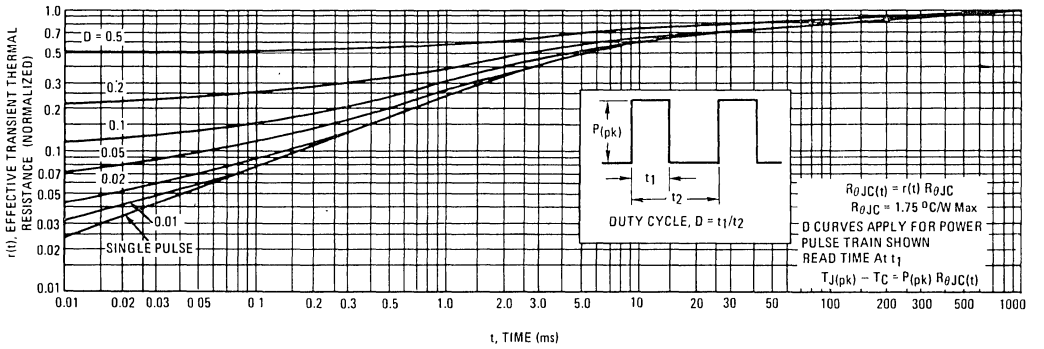


FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

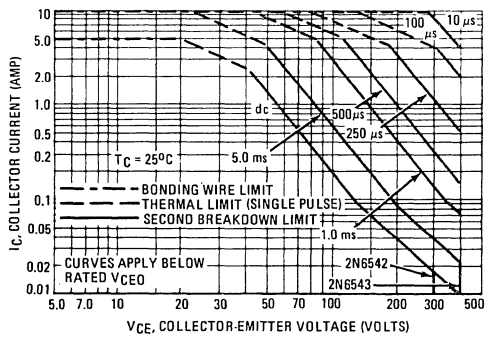


FIGURE 13 – REVERSE BIAS SAFE OPERATING AREA

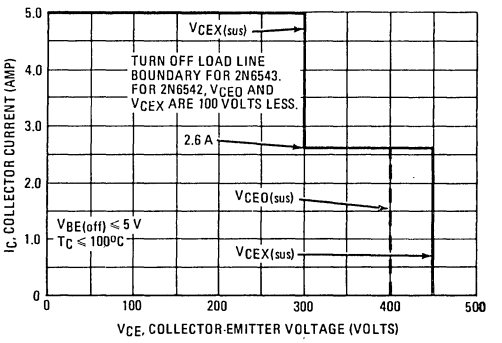
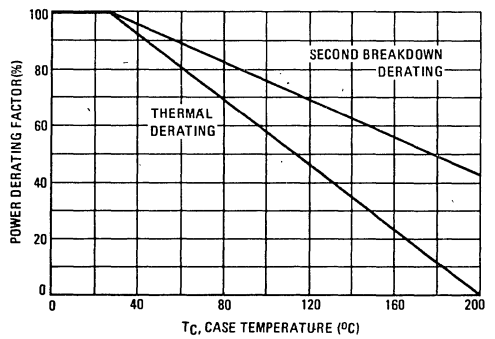


FIGURE 14 – POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Use of reverse biased safe operating area data (Figure 13) is discussed in the designer's application section.

2N6544
2N6545

Designers Data Sheet

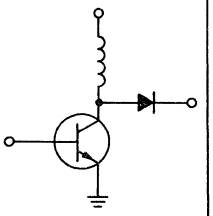
SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The 2N6544 and 2N6545 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for 115 and 220 volt line operated switch-mode applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

Specification Features –

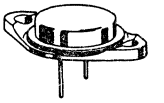
High Temperature Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents

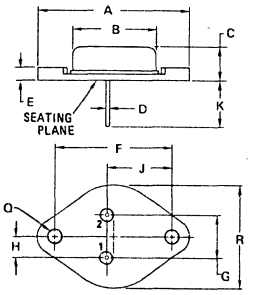


8 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
125 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-03
TO-3

*MAXIMUM RATINGS

Rating	Symbol	2N6544	2N6545	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	350	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	850	Vdc
Emitter Base Voltage	V_{EB}	9.0		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	8.0 16		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	8.0 16		Adc
Emitter Current – Continuous – Peak (1)	I_E I_{EM}	16 32		Adc
Total Power Dissipation @ $T_C = 25^oC$ @ $T_C = 100^oC$ Derate above 25^oC	P_D	125 71.5 0.714		Watts W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^{o}C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	^{o}C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	^{o}C

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mA, I_B = 0)	2N6544		300	–	
	2N6545		400	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 13)		$V_{CEX(sus)}$			Vdc
(I_C = 4.5 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	2N6544		350	–	
	2N6545		450	–	
(I_C = 8.0 A, V_{clamp} = Rated V_{CEO} -100 V,	2N6544		200	–	
T_C = 100°C)	2N6545		300	–	
Collector Cutoff Current		I_{CEV}			mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	0.5	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C			–	2.5	
Collector Cutoff Current		I_{CER}	–	3.0	mAdc
(V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)					
Emitter Cutoff Current		I_{EBO}	–	1.0	mAdc
(V_{EB} = 9.0 Vdc, I_C = 0)					
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	0.2	–	Adc
t = 1.0 s (non-repetitive) (V_{CE} = 100 Vdc)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 2.5 Adc, V_{CE} = 3.0 Vdc)			12	60	
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)			7.0	35	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 1.0 Adc)			–	1.5	
(I_C = 8.0 Adc, I_B = 2.0 Adc)			–	5.0	
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)			–	2.5	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 1.0 Adc)			–	1.6	
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C			–	1.6	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	6.0	28	MHz
(I_C = 300 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)					
Output Capacitance		C_{ob}	75	300	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)					
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	(V_{CC} = 250 Vdc, I_C = 5.0 A, I_{B1} = I_{B2} = 1.0 A, t_p = 100 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.05	μs
Rise Time		t_r	–	1.0	μs
Storage Time		t_s	–	4.0	μs
Fall Time		t_f	–	1.0	μs
Inductive Load, Clamped (Table 1)					
Storage Time	(I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_s	–	4.0	μs
Fall Time		t_f	–	0.9	μs
			Typical		
Storage Time	(I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_s	1.2		μs
Fall Time		t_f	0.18		μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

4

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

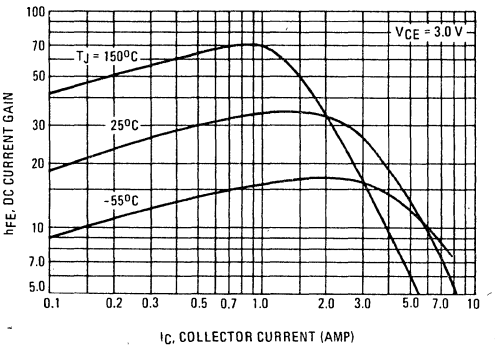


FIGURE 2 – COLLECTOR SATURATION REGION

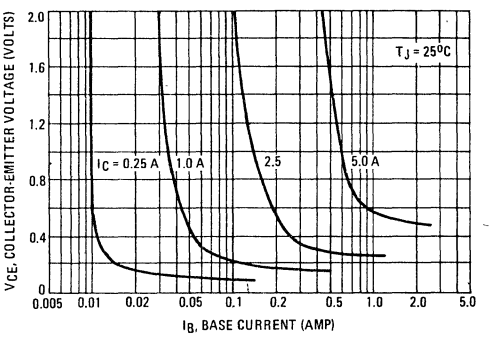


FIGURE 3 – "ON" VOLTAGE

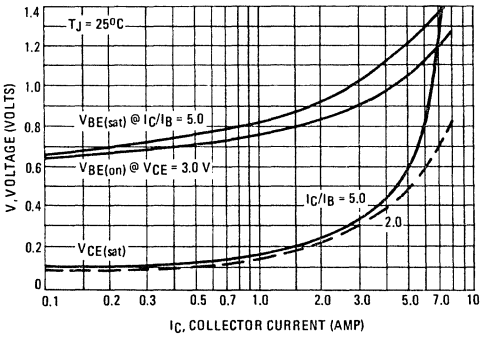


FIGURE 4 – TEMPERATURE COEFFICIENTS

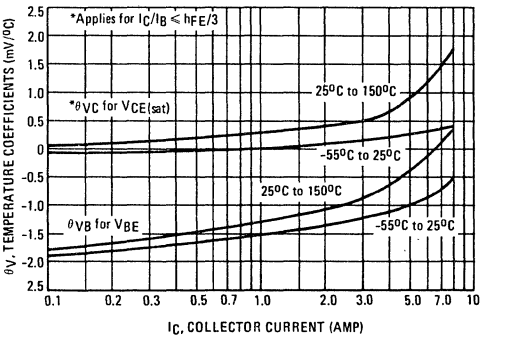


FIGURE 5 – COLLECTOR CUTOFF REGION

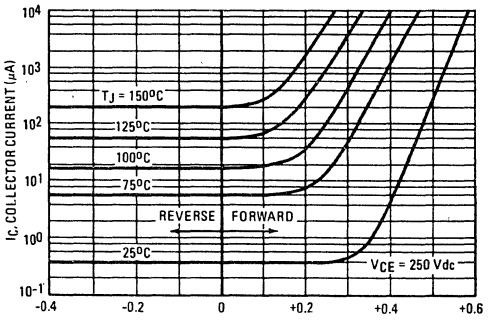


FIGURE 6 – CAPACITANCE

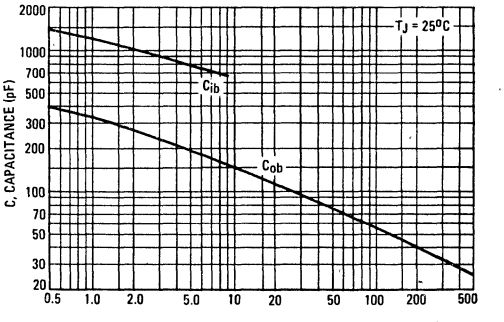
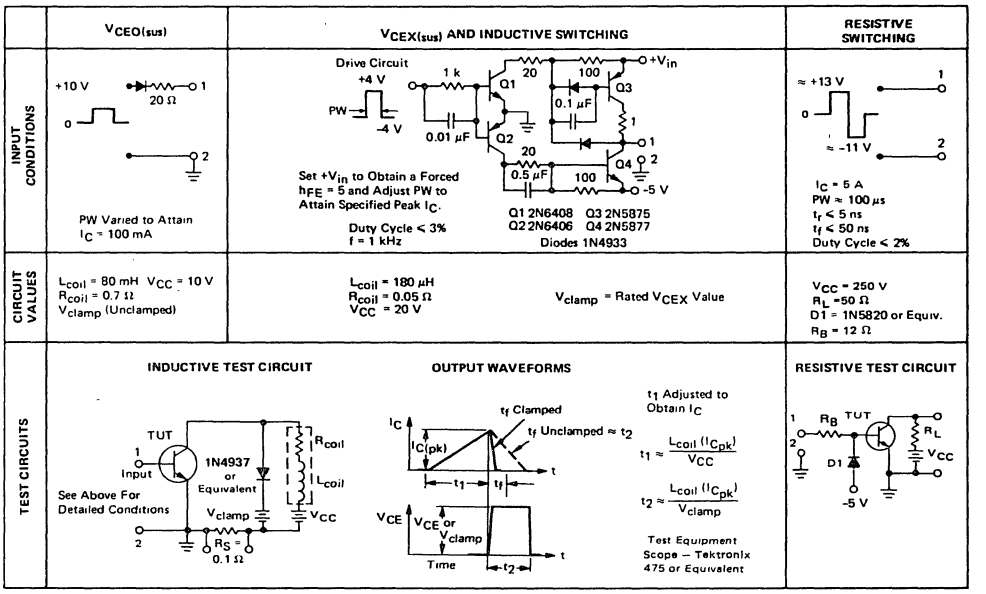


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE



DESIGNERS INFORMATION FOR APPLICATIONS AND SWITCHMODE SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for switch-mode applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in switch-mode applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

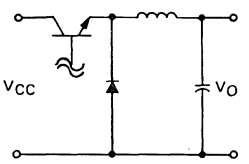
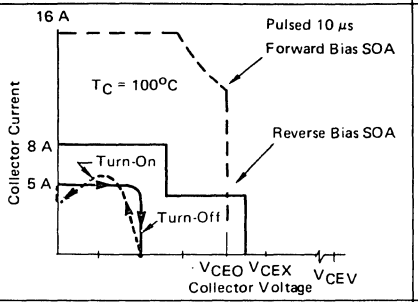
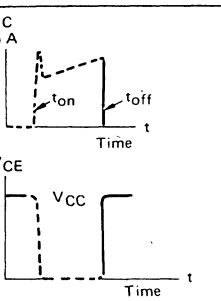
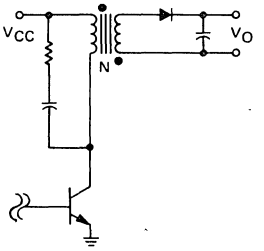
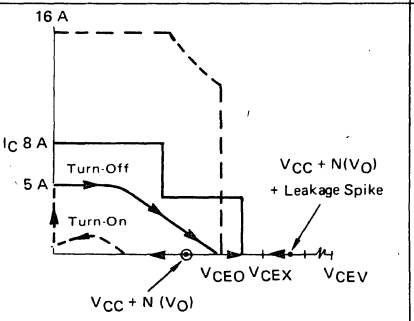
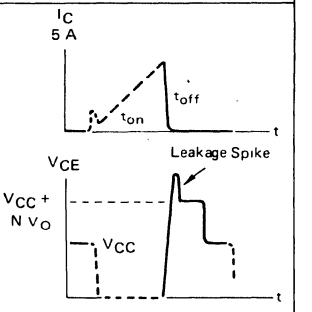
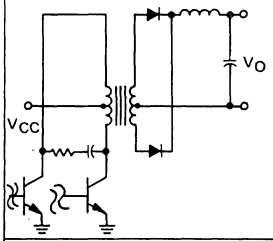
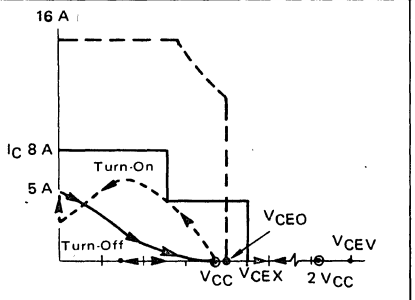
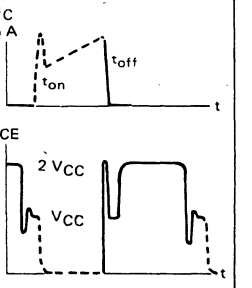
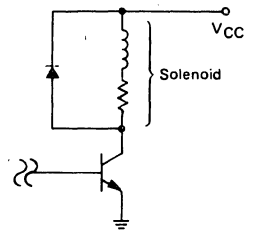
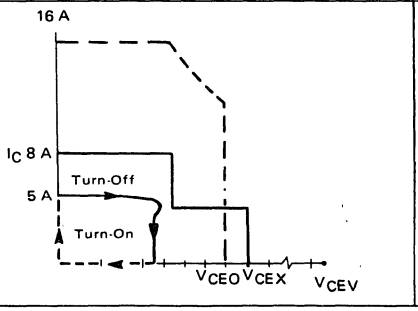
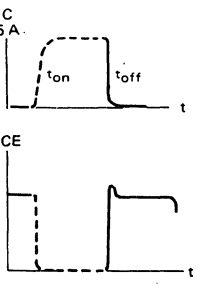
The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 12) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given high collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

As shown on the reverse bias SOA curve in Figure 13, two voltage levels are specified, one at the maximum continuous current level and one near the recommended operating level so that both normal and fault/transient

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-588, AN-719, AN-737, AN-752, AN-767 and Engineering Bulletin EB-39.

TABLE 2 – APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	SERIES SWITCHING REGULATOR 		
B	RINGING CHOKE INVERTER 		
C	PUSH-PULL INVERTER/CONVERTER 		
D	SOLENOID DRIVER 		

conditions can be taken into consideration. In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves. Note that the boundary along the $I_C = 0$ axis extends to V_{CEV}.

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output reactifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to limit the leakage spike to $< V_{CEX(sus)}$ during turn-off and $< V_{CEV}$ after turn-off (i.e. @ $I_C \leqslant I_{CEV}$).

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.

(2) The turn-on time or pulse width does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 12).

(3) The base drive conditions are similar to those specified on the data sheet (See Table 1), i.e., $V_{BE(off)} \leqslant 5$ V.

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 5 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_f). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 8 and Table 3 and resistive loads in Figures 9 and 10. Usually the inductive load component will be the dominant factor in switch-mode applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

SECONDARY BREAKDOWN REQUIRMENTS

Secondary breakdown capability is important in switching applications because of the turn-on and turn-off conditions that can exist during the switching cycle. Typically, forward biased secondary breakdown ($I_{S/b}$) is not a problem in switching applications because of the relatively higher current capability in the forward biased mode. The forward biased SOA curves provide adequate information for these conditions.

Reverse biased secondary breakdown ($E_{S/b}$) is quite different and a more complex situation from both design and specification standpoint. The $E_{S/b}$ rating is intended to define the amount of energy that the device can absorb while it is in a reverse biased avalanche mode (unclamped). The major problems in specifying $E_{S/b}$ are:

(1) Individual device capability can vary by more than an order of magnitude within the same production lot.

(2) Energy handling capability is not constant within the same device family when the test conditions are changed.

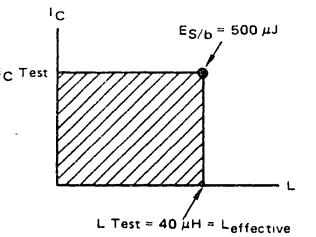
(3) $E_{S/b}$ testing is often destructive when a device actually goes into secondary breakdown.

(4) Some device families exhibit very limited capability in the avalanche condition.

(5) Depending on the device and test conditions, some devices may not reach the avalanche condition during the test.

For these reasons, the most reliable design approach is to avoid this mode of operation by clamping or snubbing the main inductive load component and minimizing leakage inductance whenever possible. The $E_{S/b}$ specification does provide a boundary condition represented in Figure 7.

FIGURE 7 – COLLECTOR CURRENT versus UNCLAMPED LOAD INDUCTANCE



Operation with an unclamped inductance is safe within the shaded area provided the base drive conditions are similar to or less severe than the specified conditions shown in Table 1, i.e., $V_{BE(off)} \leqslant 4$ V, $R_{BE} \geqslant 50\,\Omega$ and

$$L_{effective} = \frac{L_L(V_{CEX})}{V_{CEX}-V_{CC}}$$

where L_L = Circuit Leakage Reactance

TEMPERATURE REQUIREMENTS

The important parameters on this data sheet have been specified at a case temperature of 100°C to represent a recommended worst case design condition.

FIGURE 8 – TURN-OFF WAVEFORM

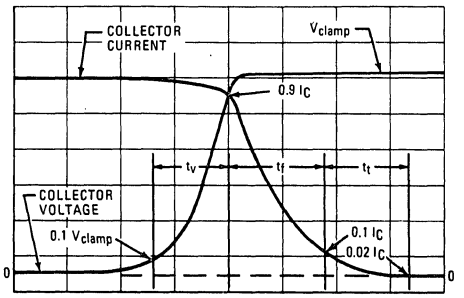


TABLE 3–INDUCTIVE SWITCHING PERFORMANCE

I_C Amps	T_C °C	t_s µs	t_v µs	t_f µs	t_t µs	$t_v+t_f+t_t$ µs
3.0	25	0.94	0.09	0.14	0.10	0.33
	100	1.40	0.30	0.44	0.06	0.80
5.0	25	1.20	0.17	0.18	0.10	0.45
	100	1.90	0.50	0.45	0.05	1.00
8.0	25	1.60	0.27	0.12	0.09	0.48
	100	1.80	0.57	0.17	0.30	1.04

Note: All Data Recorded in the Inductive Switching Circuit Shown in Table 1.

To facilitate volume production testing, maximum inductive switching limits for these transistors are specified using conventional measurement techniques, e.g. t_s(max) is measured from the point where I_{B1} has decreased 10% to the point where I_C has decreased 10%, and t_f(max) is measured between the 90% and 10% points on the I_C waveform. In most applications, a large percentage of the total device power dissipation occurs during the fall time and t_f is normally used as a figure of merit when choosing a device for a switch-mode application. However, there are two portions of the turn-off waveform that can add losses and in some cases these losses can become a significant portion of the total device dissipation.

Figure 8 shows an enlarged portion of the inductive switching waveform during turn-off. The interval labeled t_v is part of the storage time interval (t_s) and is defined as voltage switching time. During this interval the transistor collector to emitter voltage changes from a saturation level to a level equal to or approaching the clamp voltage while the collector current has only changed by 10%. Typical values for this time interval at various current levels are shown in Table 3 at 25°C and 100°C case temperature.

The time interval labeled t_t occurs after the fall time and appears as a "tail" on the trailing edge of the collector current waveform. It is measured, for this discussion, from the 10% point to the 2% point; and during this interval the collector to emitter voltage is equal to the clamp voltage. Typical values for these time intervals are also shown in Table 3.

Since power dissipation occurs during the total time period $t_v + t_f + t_t$ and each interval can be affected by external conditions, some applications may require a specific analysis in order to accurately predict total device dissipation.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON TIME

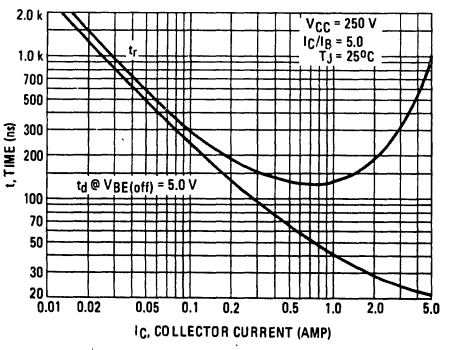


FIGURE 10 – TURN-OFF TIME

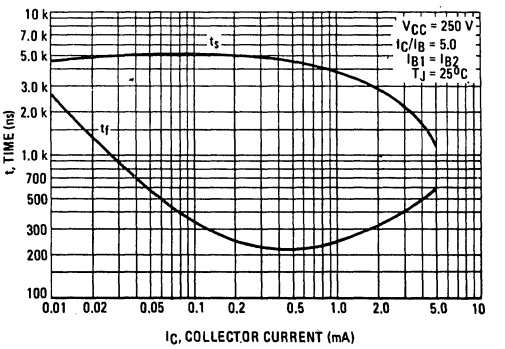


FIGURE 11 – THERMAL RESPONSE

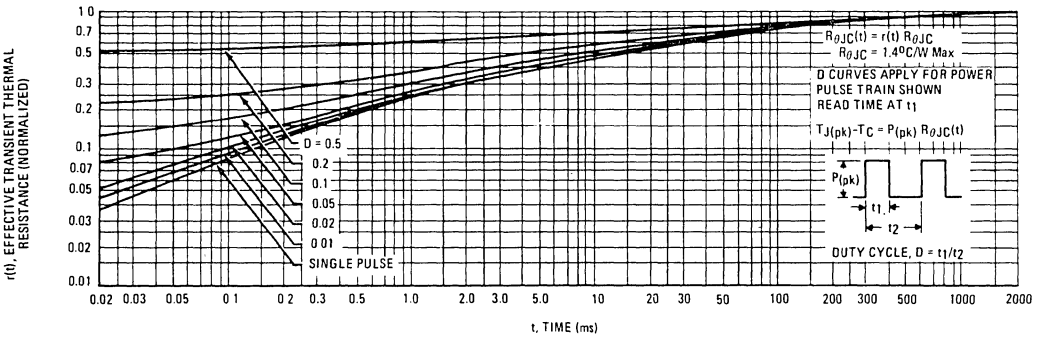


FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

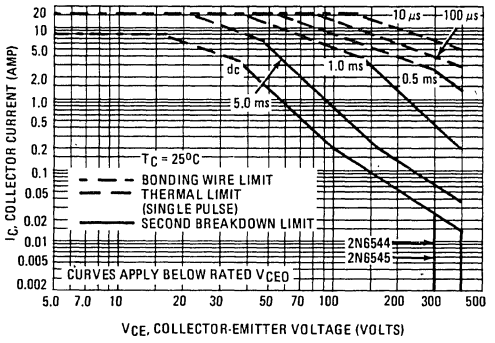


FIGURE 13 – REVERSE BIAS SAFE OPERATING AREA

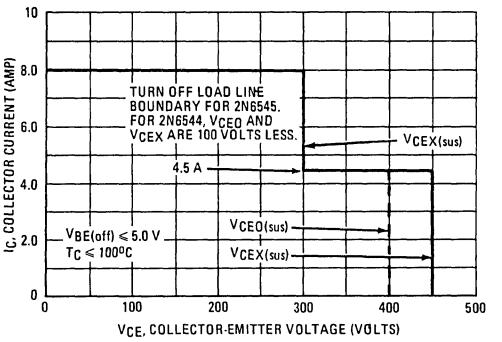
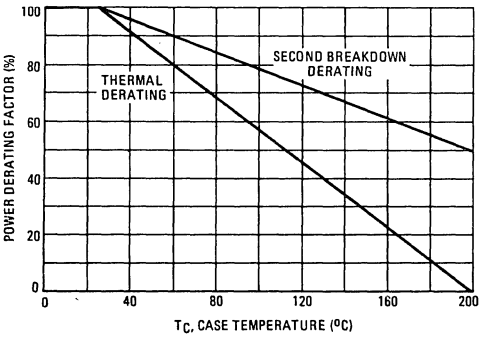


FIGURE 14 – POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^{o}C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^{o}C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Use of reverse biased safe operating area data (Figure 13) is discussed in the designer's application section.

2N6546
2N6547

Designers Data Sheet

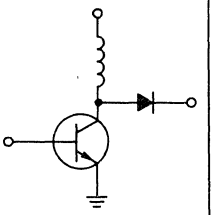
SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The 2N6546 and 2N6547 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for 115 and 220 volt line operated switch-mode applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

Specification Features –

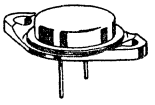
High Temperature Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents

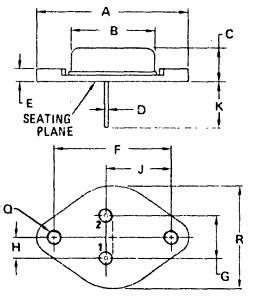


15 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-03
TO-3

***MAXIMUM RATINGS**

Rating	Symbol	2N6546	2N6547	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	350	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	850	Vdc
Emitter Base Voltage	V_{EB}	9.0		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	15 30		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	10 20		Adc
Emitter Current – Continuous – Peak (1)	I_E I_{EM}	25 50		Adc
Total Power Dissipation @ $T_C = 25^oC$ @ $T_C = 100^oC$ Derate above 25^oC	P_D	175 100 1.0		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	^oC

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mA, I_B = 0)	2N6546		300	–	
	2N6547		400	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 13)		$V_{CEX(sus)}$			Vdc
(I_C = 8.0 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	2N6546		350	–	
	2N6547		450	–	
(I_C = 15 A, V_{clamp} = Rated V_{CEO} – 100 V,	2N6546		200	–	
T_C = 100°C)	2N6547		300	–	
Collector Cutoff Current		I_{CEV}			mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	1.0	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			–	4.0	
Collector Cutoff Current		I_{CER}	–	5.0	mAdc
(V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)					
Emitter Cutoff Current		I_{EBO}	–	1.0	mAdc
(V_{EB} = 9.0 Vdc, I_C = 0)					
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	0.2	–	Adc
t = 1.0 s (non-repetitive) (V_{CE} = 100 Vdc)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)			12	60	
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)			6.0	30	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 2.0 Adc)			–	1.5	
(I_C = 15 Adc, I_B = 3.0 Adc)			–	5.0	
(I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)			–	2.5	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 2.0 Adc)			–	1.6	
(I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C			–	1.6	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	6.0	28	MHz
(I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)					
Output Capacitance		C_{ob}	125	500	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)					
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	(V_{CC} = 250 V, I_C = 10 A,	t_d	–	0.05	μs
Rise Time	I_{B1} = I_{B2} = 2.0 A, t_p = 100 μs,	t_r	–	1.0	μs
Storage Time	Duty Cycle ≤ 2.0%)	t_s	–	4.0	μs
Fall Time		t_f	–	0.7	μs
Inductive Load, Clamped (Table 1)					
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 2.0 A,	t_s	–	5.0	μs
Fall Time	$V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_f	–	1.5	μs
			Typical		
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 2.0 A,	t_s	2.0		μs
Fall Time	$V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_f	0.09		μs

*Indicates JEDEC Registered Data.

(1) Puse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

4

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

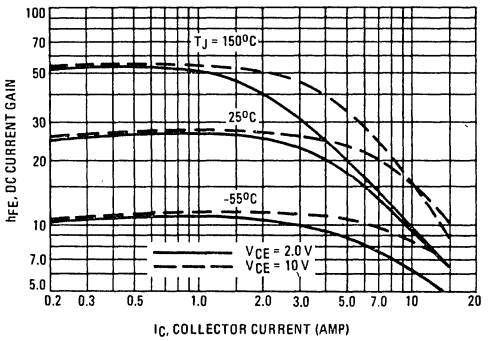


FIGURE 2 – COLLECTOR SATURATION REGION

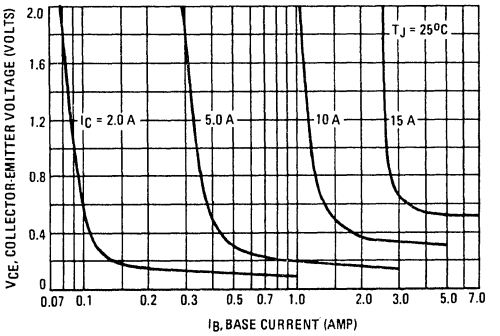


FIGURE 3 – "ON" VOLTAGE

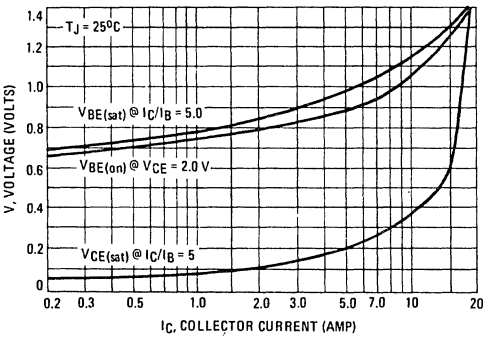


FIGURE 4 – TEMPERATURE COEFFICIENTS

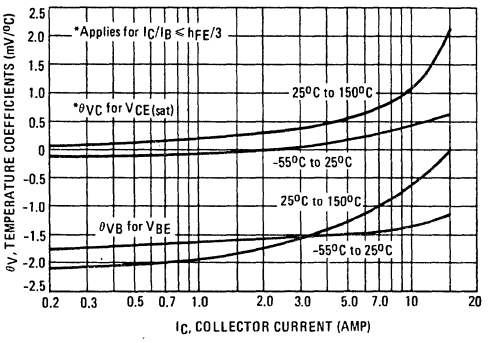


FIGURE 5 – COLLECTOR CUTOFF REGION

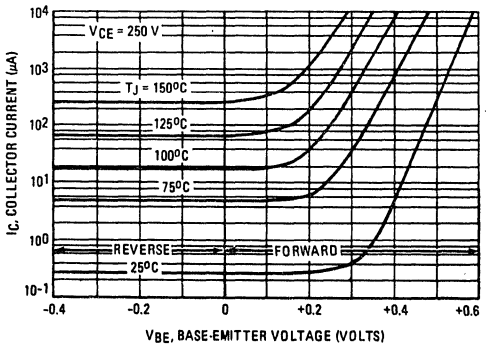


FIGURE 6 – CAPACITANCE

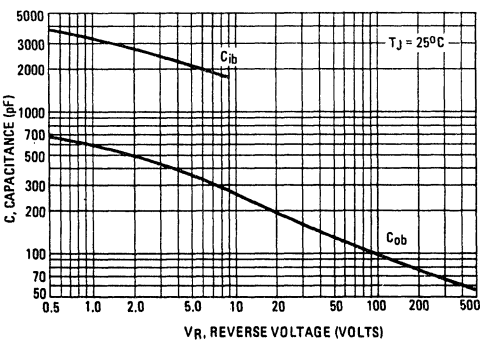


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V, 20 Ω, 0, 1, 2 PW Varied to Attain I_C = 100 mA	Drive Circuit +4 V, -4 V, PW, 1 k, 0.01 µF, 0.5 µF, 0.1 µF, 20, 100, Q1, Q2, Q3, Q4, $+V_{in}$, -5 V Set $+V_{in}$ to Obtain a Forced h_{FE} = 5 and Adjust PW to Attain Specified Peak I_C. Duty Cycle ≤ 3% f = 1 kHz Q1 2N6408 Q3 2N5875 Q2 2N6406 Q4 2N5877 Diodes 1N4933	≈ +13 V, 0, ≈ -11 V, 1, 2 I_C = 10 A PW ≈ 100 µs t_r ≤ 5 ns t_f ≤ 50 ns Duty Cycle ≤ 2%
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} (Unclamped)	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 25 Ω D1 = 1N5820 or Equiv. R_B = 6 Ω
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT TUT, 1, Input, 2, 1N4937 or Equivalent, See Above For Detailed Conditions, R_{coil}, L_{coil}, V_{clamp}, V_{CC}, R_S 0.1 Ω OUTPUT WAVEFORMS t_f Clamped, t_f Unclamped ≈ t_2, t_1 Adjusted to Obtain I_C, I_C, $I_{C(pk)}$, V_{CE}, V_{CE} or V_{clamp}, Time, t_1, t_f, t_2 $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 1, R_B, TUT, 2, D1, R_L, V_{CC}, -5 V

DESIGNERS INFORMATION FOR APPLICATIONS AND SWITCHMODE SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for switch-mode applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in switch-mode applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

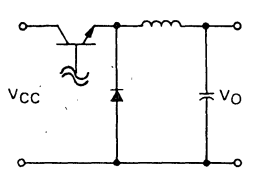
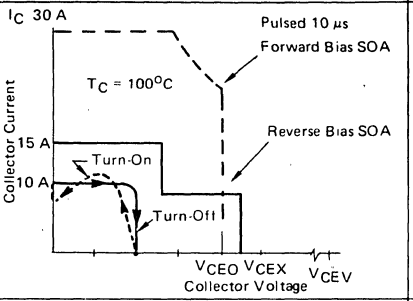
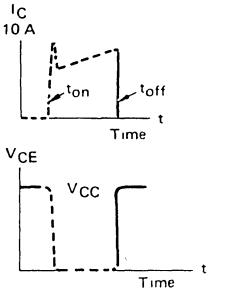
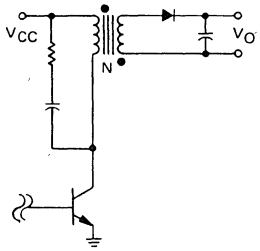
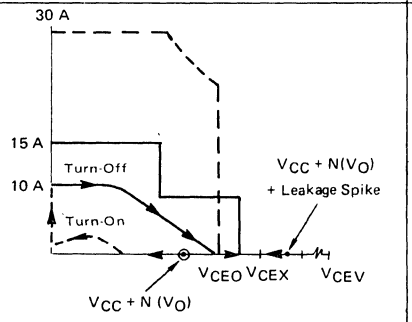
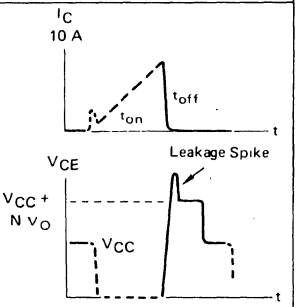
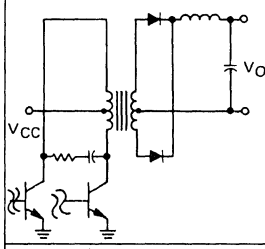
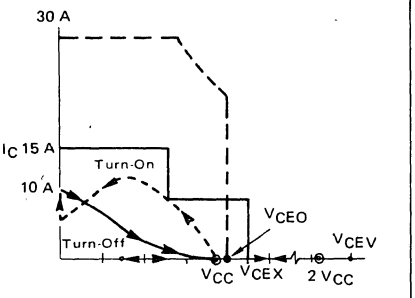
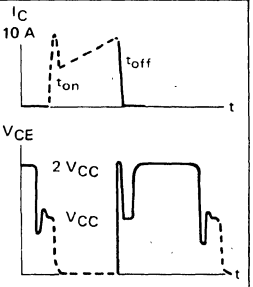
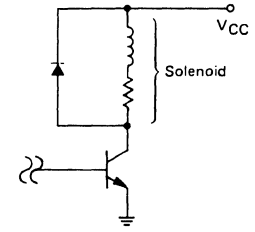
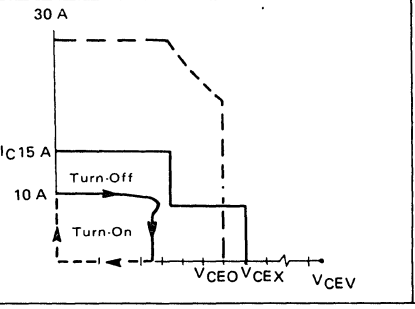
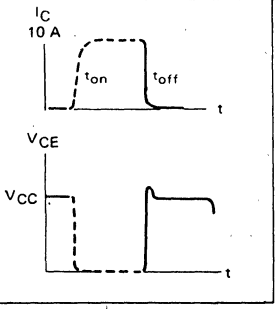
The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 12) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given high collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

As shown on the reverse bias SOA curve in Figure 13, two voltage levels are specified, one at the maximum continuous current level and one near the recommended operating level so that both normal and fault/transient

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-588, AN-719, AN-737, AN-752, AN-767

TABLE 2 – APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 		
B	**RINGING CHOKE INVERTER** 		
C	**PUSH-PULL INVERTER/CONVERTER** 		
D	**SOLENOID DRIVER** 		

conditions can be taken into consideration. In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves. Note that the boundary along the $I_C = 0$ axis extends to V_{CEV}.

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output reactifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to limit the leakage spike to $< V_{CEX(sus)}$ during turn-off and $< V_{CEV}$ after turn-off (i.e. @ $I_C \leq I_{CEV}$).

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.

(2) The turn-on time or pulse width does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 12).

(3) The base drive conditions are similar to those specified on the data sheet (See Table 1), i.e., $V_{BE(off)} \leq 5$ V.

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 10 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_f). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 8 and Table 3 and resistive loads in Figures 9 and 10. Usually the inductive load component will be the dominant factor in switch-mode applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

SECONDARY BREAKDOWN REQUIRMENTS

Secondary breakdown capability is important in switching applications because of the turn-on and turn-off conditions that can exist during the switching cycle. Typically, forward biased secondary breakdown ($I_{S/b}$) is not a problem in switching applications because of the relatively higher current capability in the forward biased mode. The forward biased SOA curves provide adequate information for these conditions.

Reverse biased secondary breakdown ($E_{S/b}$) is quite different and a more complex situation from both design and specification standpoint. The $E_{S/b}$ rating is intended to define the amount of energy that the device can absorb while it is in a reverse biased avalanche mode (unclamped). The major problems in specifying $E_{S/b}$ are:

(1) Individual device capability can vary by more than an order of magnitude within the same production lot.

(2) Energy handling capability is not constant within the same device family when the test conditions are changed.

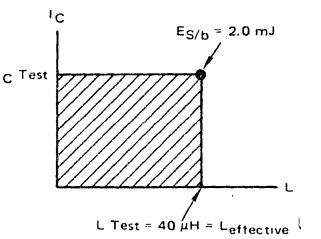
(3) $E_{S/b}$ testing is often destructive when a device actually goes into secondary breakdown.

(4) Some device families exhibit very limited capability in the avalanche condition.

(5) Depending on the device and test conditions, some devices may not reach the avalanche condition during the test.

For these reasons, the most reliable design approach is to avoid this mode of operation by clamping or snubbing the main inductive load component and minimizing leakage inductance whenever possible. The $E_{S/b}$ specification does provide a boundary condition represented in Figure 7.

FIGURE 7 – COLLECTOR CURRENT versus UNCLAMPED LOAD INDUCTANCE



Operation with an unclamped inductance is safe within the shaded area provided the base drive conditions are similar to or less severe than the specified conditions shown in Table 1, i.e., $V_{BE(off)} \leq 4$ V, $R_{BE} \geq 50\ \Omega$ and

$$L_{effective} = \frac{L_L(V_{CEX})}{V_{CEX}-V_{CC}}$$

where L_L = Circuit Leakage Reactance

TEMPERATURE REQUIREMENTS

The important parameters on this data sheet have been specified at a case temperature of 100°C to represent a recommended worst case design condition.

4

FIGURE 8 – TURN-OFF WAVEFORM

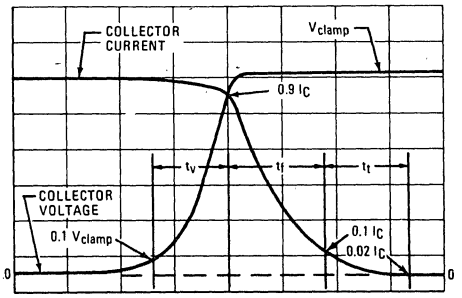


TABLE 3 – INDUCTIVE SWITCHING PERFORMANCE

I_C Amps	T_C °C	t_s µs	t_v µs	t_f µs	t_t µs	$t_v+t_f+t_t$ µs
3.0	25	1.30	0.17	0.05	0.20	0.42
	100	2.10	0.25	0.08	0.25	0.58
5.0	25	1.60	0.08	0.04	0.08	0.20
	100	2.40	0.16	0.08	0.23	0.48
10	25	2.00	0.09	0.09	0.20	0.38
	100	2.50	0.16	0.20	0.13	0.49

Note: All Data Recorded in the Inductive Switching Circuit Shown in Table 1.

To facilitate volume production testing, maximum inductive switching limits for these transistors are specified using conventional measurement techniques, e.g. t_s(max) is measured from the point where I_{B1} has decreased 10% to the point where I_C has decreased 10%, and t_f(max) is measured between the 90% and 10% points on the I_C waveform. In most applications, a large percentage of the total device power dissipation occurs during the fall time and t_f is normally used as a figure of merit when choosing a device for a switch-mode application. However, there are two portions of the turn-off waveform that can add losses and in some cases these losses can become a significant portion of the total device dissipation.

Figure 8 shows an enlarged portion of the inductive switching waveform during turn-off. The interval labeled t_v is part of the storage time interval (t_s) and is defined as voltage switching time. During this interval the transistor collector to emitter voltage changes from a saturation level to a level equal to or approaching the clamp voltage while the collector current has only changed by 10%. Typical values for this time interval at various current levels are shown in Table 3 at 25°C and 100°C case temperature.

The time interval labeled t_t occurs after the fall time and appears as a "tail" on the trailing edge of the collector current waveform. It is measured, for this discussion, from the 10% point to the 2% point; and during this interval the collector to emitter voltage is equal to the clamp voltage. Typical values for these time intervals are also shown in Table 3.

Since power dissipation occurs during the total time period $t_v + t_f + t_t$ and each interval can be affected by external conditions, some applications may require a specific analysis in order to accurately predict total device dissipation.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON TIME

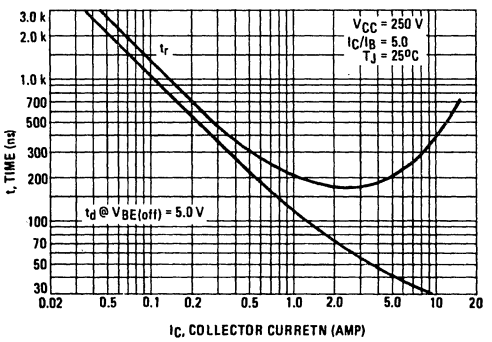


FIGURE 10 – TURN-OFF TIME

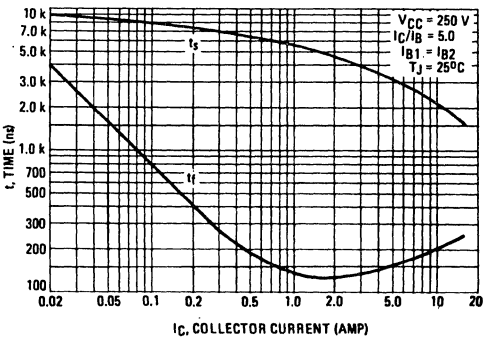
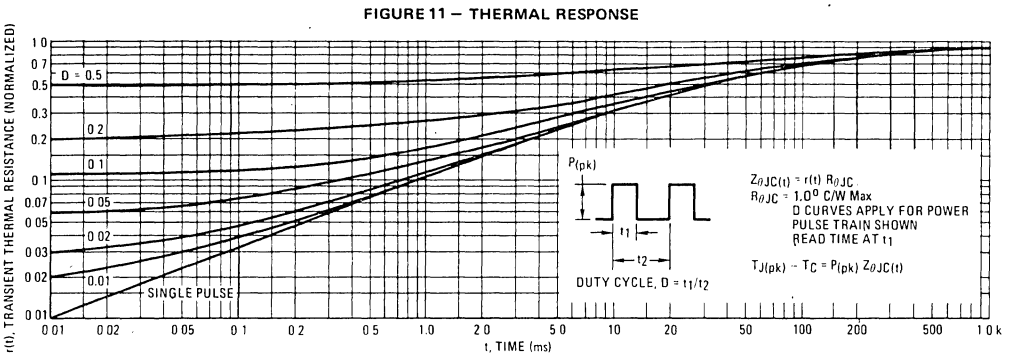


FIGURE 11 – THERMAL RESPONSE



4

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

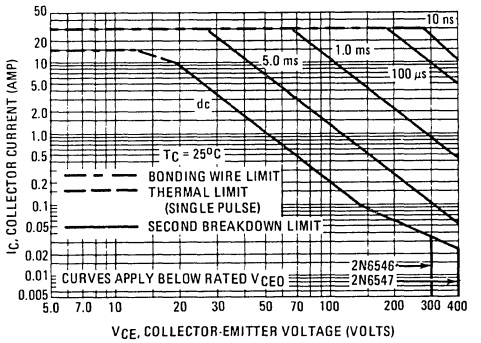


FIGURE 13 – REVERSE BIAS SAFE OPERATING AREA

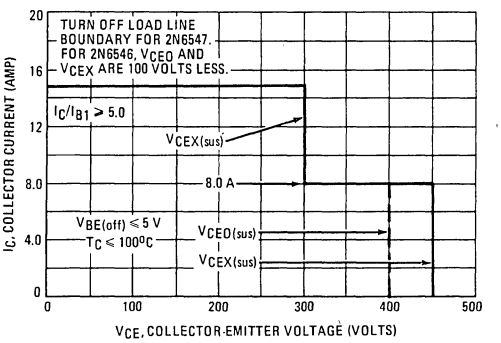
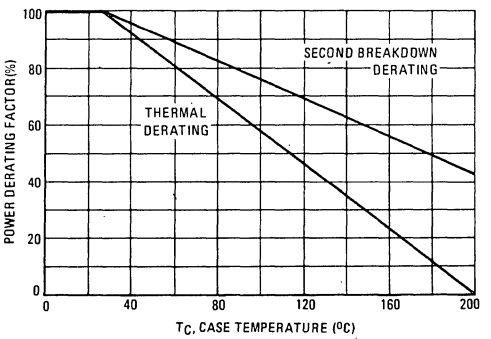


FIGURE 14 – POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Use of reverse biased safe operating area data (Figure 13) is discussed in the designer's application section.

2N6548
2N6549

4

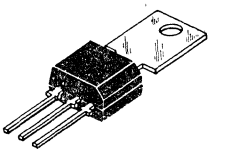
NPN SILICON DARLINGTON AMPLIFIER TRANSISTORS

. . . designed for amplifier and driver applications where high gain is an essential requirement, low power lamp and relay drivers and power drivers for high-current applications such as voltage regulators.

- High DC Current Gain –
  h_{FE} = 25,000 (Min) @ I_C = 200 mAdc – 2N6548
  = 15,000 (Min) @ I_C = 500 mAdc – 2N6548
- Collector-Emitter Breakdown Voltage –
  BV_{CES} = 40 Vdc (Min) @ I_C = 100 μAdc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 1.0 Adc
- Duowatt Package –
  2 Watts Free Air Dissipation @ T_A = 25°C

DUOWATT

NPN SILICON DARLINGTON AMPLIFIER TRANSISTORS



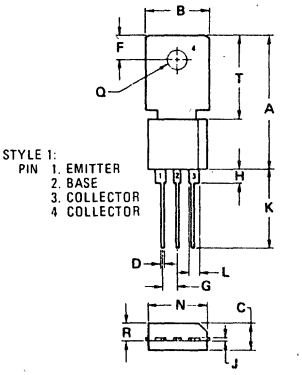
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
*Collector-Base Voltage	V_{CBO}	50	Vdc
*Emitter-Base Voltage	V_{EBO}	12	Vdc
*Collector Current – Continuous	I_C	2.0	Adc
*Base Current – Continuous	I_B	100	mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 16	Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150	°C
*Solder Temperature, 1/16" from Case for 10 Seconds	–	260	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.19	4.44	0.165	0.175
D	0.61	0.71	0.024	0.028
F	3.68	3.94	0.145	0.155
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.70	–	0.500	–
L	1.78	2.03	0.070	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	2.41	2.67	0.095	0.105
T	13.21	13.97	0.520	0.550

CASE 306-04
TO-202AC

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

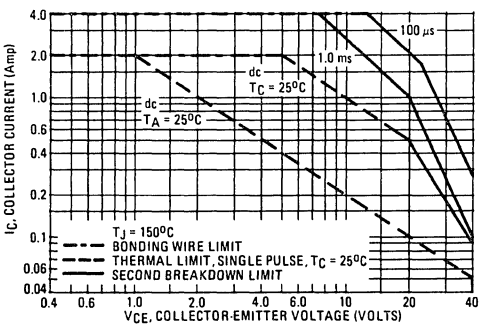
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 100 μAdc, V_{BE} = 0)		BV_{CES}	40	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)		BV_{CBO}	50	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		BV_{EBO}	12	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)		I_{CBO}	–	100	nAdc
Emitter Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}	–	100	nAdc
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			–
(I_C = 200 mAdc, V_{CE} = 5.0 Vdc)	2N6548		25,000	150,000	
	2N6549		15,000	150,000	
(I_C = 500 mAdc, V_{CE} = 5.0 Vdc)	2N6548		15,000	–	
	2N6549		10,000	–	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	2N6548		5,000	–	
	2N6549		3,000	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 1.0 Adc, I_B = 2.0 mAdc)			–	1.5	
(I_C = 2.0 Adc, I_B = 4.0 mAdc)			–	2.0	
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 2.0 mAdc)		$V_{BE(sat)}$	–	2.0	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS					
High Frequency Current Gain (I_C = 200 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		$\|h_{fe}\|$	1.0	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	7.0	pF
Small-Signal Current Gain		h_{fe}			–
(I_C = 50 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	2N6548		20,000	–	
	2N6549		15,000	–	

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TYPICAL CHARACTERISTICS

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS (continued)

FIGURE 2 – DC CURRENT GAIN

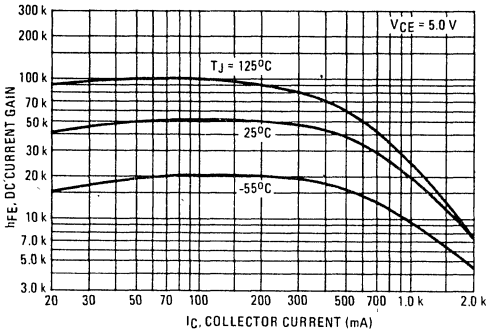


FIGURE 3 – "ON" VOLTAGES

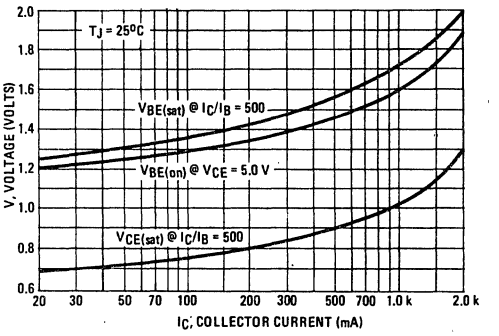


FIGURE 4 – COLLECTOR SATURATION REGION

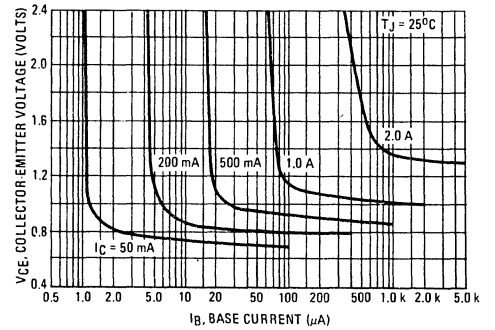


FIGURE 5 – TEMPERATURE COEFFICIENT

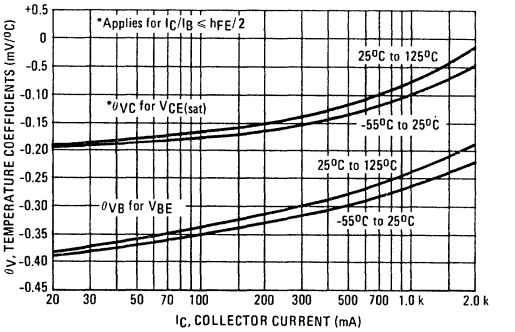
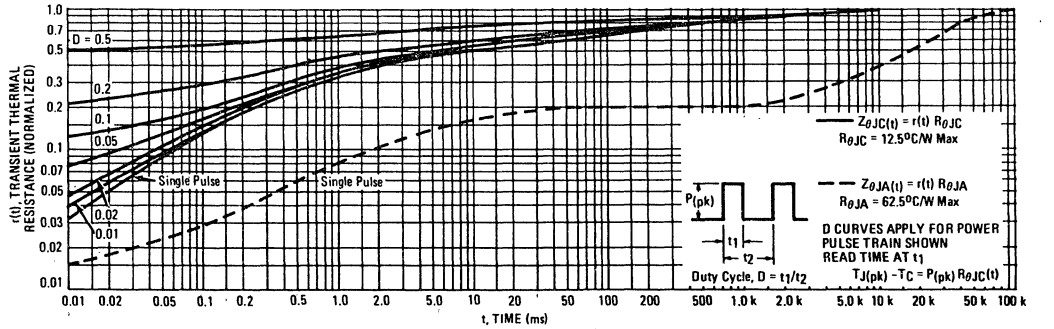


FIGURE 6 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – CAPACITANCE

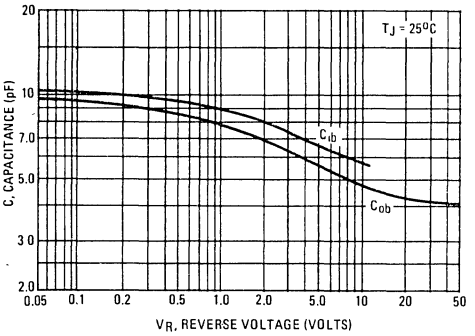
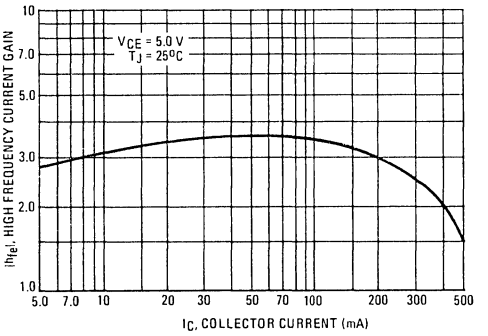


FIGURE 8 – HIGH-FREQUENCY CURRENT GAIN



4

2N6551
2N6552
2N6553

4

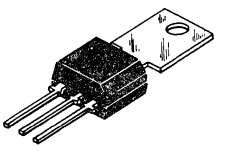
NPN SILICON ANNULAR AMPLIFIER TRANSISTORS

. . . designed for general-purpose, medium-voltage, medium power amplifier and driver applications; series, shunt and switching regulators, and low and high frequency inverters and converters.

- High Collector-Emitter Breakdown Voltage – BV_{CEO} = 100 Vdc (Min) @ I_C = 1.0 mAdc – 2N6553
- Duowatt Package – 2 Watts Free Air Dissipation @ $T_A = 25^oC$
- Complements to PNP 2N6554/5/6

DUOWATT

NPN SILICON AMPLIFIER TRANSISTORS



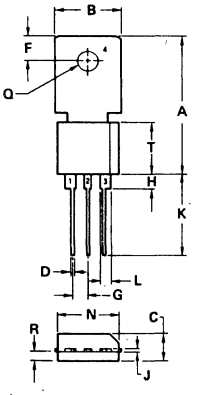
MAXIMUM RATINGS

Rating	Symbol	2N6551	2N6552	2N6553	Unit
*Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
*Collector-Base Voltage	V_{CBO}	60	80	100	Vdc
*Emitter-Base Voltage	V_{EBO}	5.0			Vdc
*Collector Current – Continuous	I_C	1.0			Adc
– Peak (1)		2.0			
*Base Current	I_B	100			mAdc
*Total Power Dissipation @ $T_A = 25^oC$	P_D	2.0			Watts
Derate above 25^oC		16			mW/^{o}C
Total Power Dissipation @ $T_C = 25^oC$	P_D	10			Watts
Derate above 25^oC		80			mW/^{o}C
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150			^{o}C
*Solder Temperature, 1/16" from Case for 10 Seconds	–	260			^{o}C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R\theta_{JA}$	62.5	^{o}C/W
Thermal Resistance, Junction to Case	$R\theta_{JC}$	12.5	^{o}C/W

*Indicates JEDEC Registered Data.
(1) ≤10 ms, ≤ 50% Duty Cycle



STYLE 1.
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04
TO-202AC

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage		BV_{CEO}			Vdc
(I_C = 1.0 mAdc, I_B = 0)	2N6551		60	–	
	2N6552		80	–	
	2N6553		100	–	
Collector-Base Breakdown Voltage		BV_{CBO}			Vdc
(I_C = 100 μAdc, I_E = 0)	2N6551		60	–	
	2N6552		80	–	
	2N6553		100	–	
Emitter-Base Breakdown Voltage		BV_{EBO}	5.0	–	Vdc
(I_E = 100 μAdc, I_C = 0)					
Collector Cutoff Current		I_{CBO}			nAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N6551		–	100	
(V_{CB} = 60 Vdc, I_E = 0)	2N6552		–	100	
(V_{CB} = 80 Vdc, I_E = 0)	2N6553		–	100	
Emitter Cutoff Current		I_{EBO}	–	100	nAdc
(V_{EB} = 4.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)			80	300	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			25	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 250 mAdc, I_B = 10 mAdc)			–	0.5	
(I_C = 1.0 Adc, I_B = 100 mAdc)			–	1.0	
Base-Emitter On Voltage		$V_{BE(on)}$	–	1.2	Vdc
(I_C = 250 mAdc, V_{CE} = 5.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	75	375	MHz
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)					
Collector-Base Capacitance		C_{cb}	–	18	pF
(V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)					

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TYPICAL CHARACTERISTICS

FIGURE 1 – CURRENT-GAIN – BANDWIDTH PRODUCT

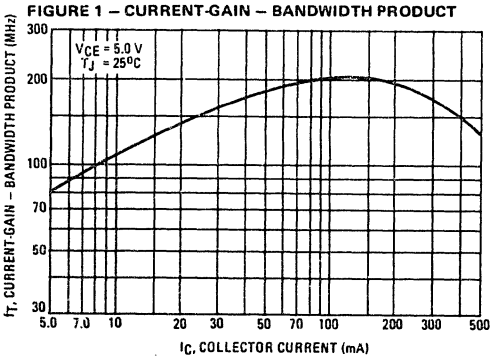
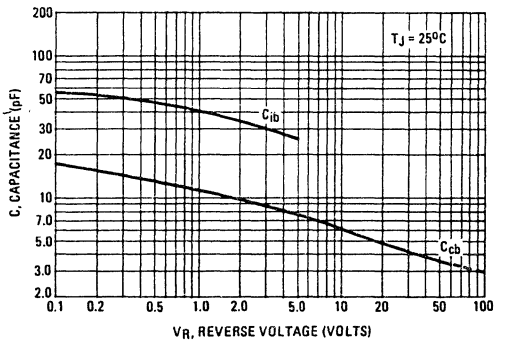


FIGURE 2 – CAPACITANCES



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TYPICAL CHARACTERISTICS (continued)

FIGURE 3 – DC CURRENT GAIN

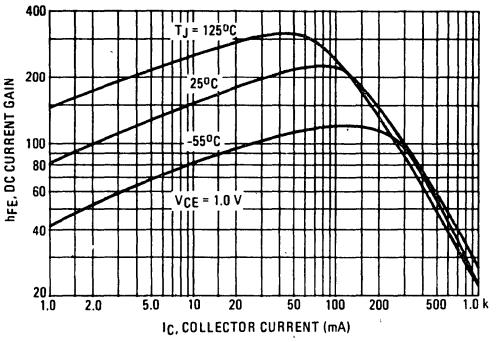


FIGURE 4 – "ON" VOLTAGE

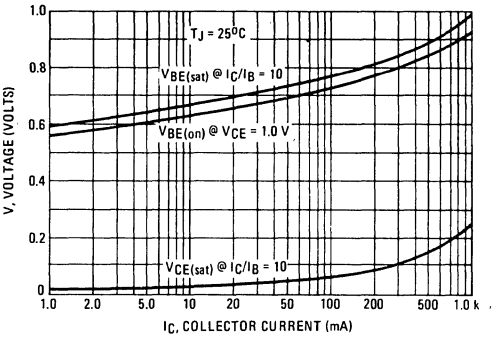


FIGURE 5 – COLLECTOR SATURATION REGION

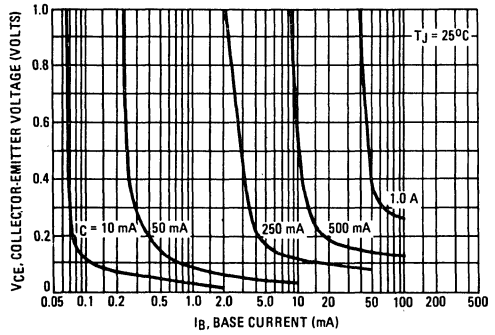


FIGURE 6 – TEMPERATURE COEFFICIENTS

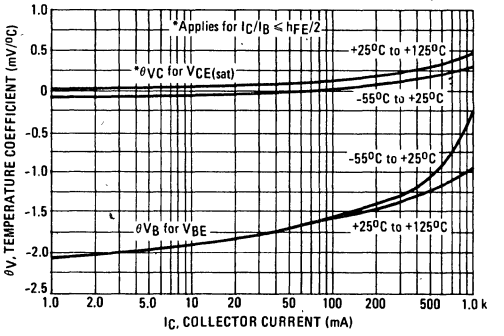


FIGURE 7 – COLLECTOR CHARACTERISTICS

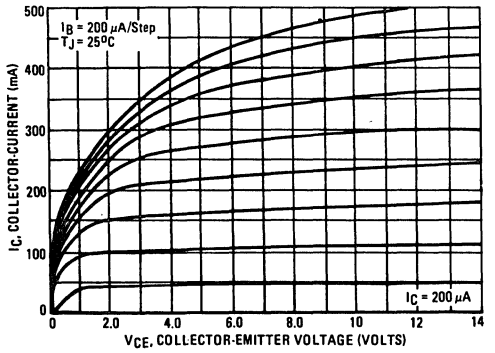
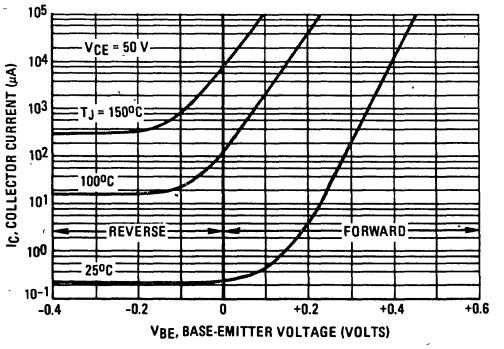


FIGURE 8 – COLLECTOR CUTOFF REGION



TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – THERMAL RESPONSE

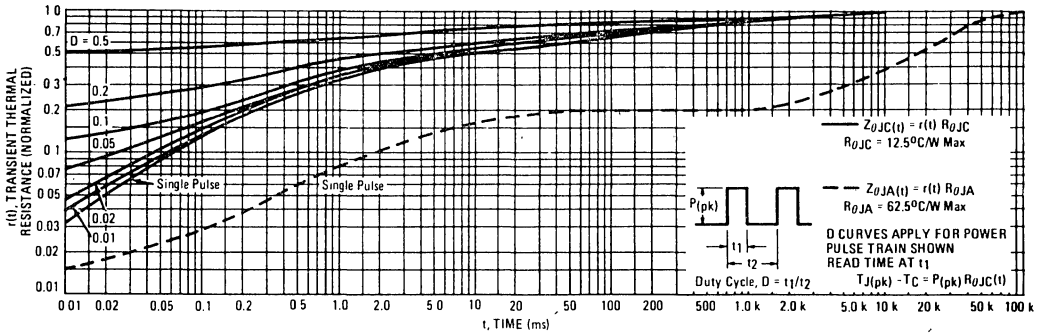
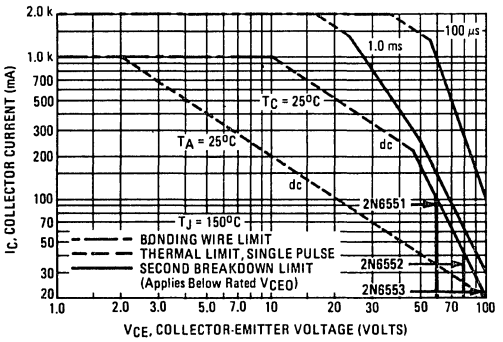


FIGURE 10 – ACTIVE-REGION SAFE-OPERATING AREA

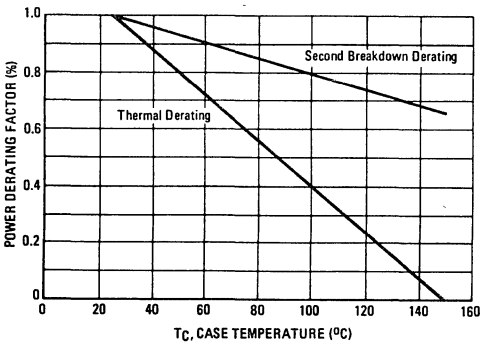


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 – POWER DERATING



2N6554
2N6555
2N6556

4

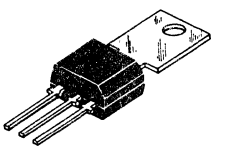
PNP SILICON ANNULAR AMPLIFIER TRANSISTORS

. . . designed for general-purpose, medium-voltage, medium power amplifier and driver applications; series, shunt and switching regulators, and low and high frequency inverters and converters.

- High Collector-Emitter Breakdown Voltage — BV_{CEO} = 100 Vdc (Min) @ I_C = 1.0 mAdc — 2N6556
- Duowatt Package — 2 Watts Free Air Dissipation @ $T_A = 25^oC$
- Complements to NPN 2N6551/2/3

DUOWATT

PNP SILICON AMPLIFIER TRANSISTORS



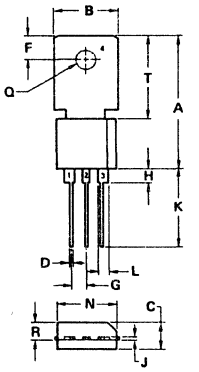
MAXIMUM RATINGS

Rating	Symbol	2N6554	2N6555	2N6556	Unit
*Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
*Collector-Base Voltage	V_{CBO}	60	80	100	Vdc
*Emitter-Base Voltage	V_{EBO}	← 5.0 →			Vdc
*Collector Current — Continuous Peak	I_C	← 1.0 → ← 2.0 →			Adc
*Base Current	I_B	← 100 →			mAdc
*Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	← 2.0 → ← 16 →			Watts $mW/^oC$
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	← 10 → ← 80 →			Watts $mW/^oC$
*Operating and Storage Junction Temperature Range	T_J, T_{stg}	← −55 to +150 →			^oC
*Solder Temperature, 1/16" from Case for 10 Seconds	—	← 260 →			^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	$^oC/W$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	$^oC/W$

*Indicates JEDEC Registered Data.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.19	4.44	0.165	0.175
D	0.61	0.71	0.024	0.028
F	3.68	3.94	0.145	0.155
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.70	–	0.500	–
L	1.78	2.03	0.070	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	2.41	2.67	0.095	0.105
T	13.21	13.97	0.520	0.550

CASE 306-04
TO-202AC

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

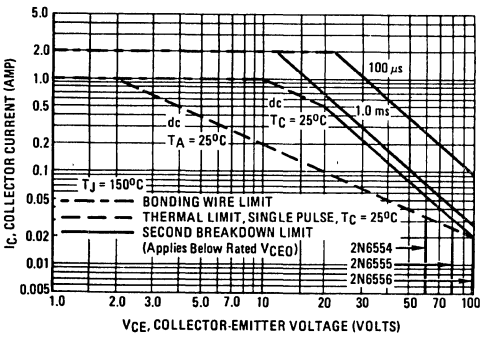
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage		BV_{CEO}			Vdc
(I_C = 1.0 mAdc, I_B = 0)	2N6554		60	–	
	2N6555		80	–	
	2N6556		100	–	
Collector-Base Breakdown Voltage		BV_{CBO}			Vdc
(I_C = 100 μAdc, I_E = 0)	2N6554		60	–	
	2N6555		80	–	
	2N6556		100	–	
Emitter-Base Breakdown Voltage		BV_{EBO}	5.0	–	Vdc
(I_E = 100 μAdc, I_C = 0)					
Collector Cutoff Current		I_{CBO}			nAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N6554		–	100	
(V_{CB} = 60 Vdc, I_E = 0)	2N6555		–	100	
(V_{CB} = 80 Vdc, I_E = 0)	2N6556		–	100	
Emitter Cutoff Current		I_{EBO}	–	100	nAdc
(V_{EB} = 4.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)			80	300	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			25	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 250 mAdc, I_B = 10 mAdc)			–	0.5	
(I_C = 1.0 Adc, I_B = 100 mAdc)			–	1.0	
Base-Emitter On Voltage		$V_{BE(on)}$	–	1.2	Vdc
(I_C = 250 mAdc, V_{CE} = 5.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	75	375	MHz
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)					
Collector-Base Capacitance		C_{cb}	–	18	pF
(V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)					

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

4

TYPICAL CHARACTERISTICS (continued)

FIGURE 2 – DC CURRENT GAIN

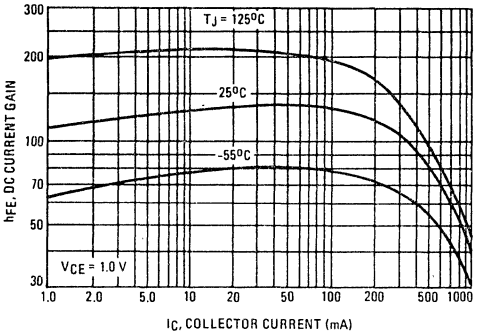


FIGURE 3 – "ON" VOLTAGE

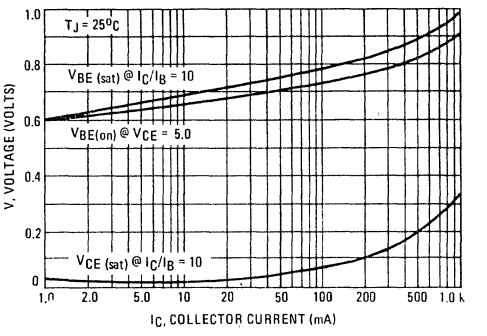


FIGURE 4 – COLLECTOR SATURATION REGION

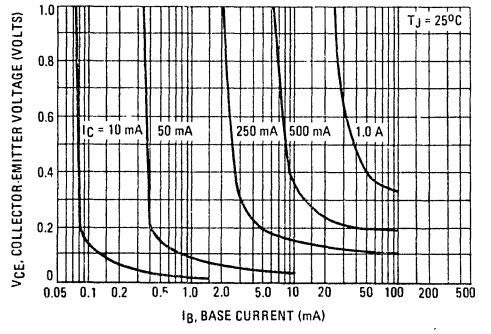


FIGURE 5 – TEMPERATURE COEFFICIENT

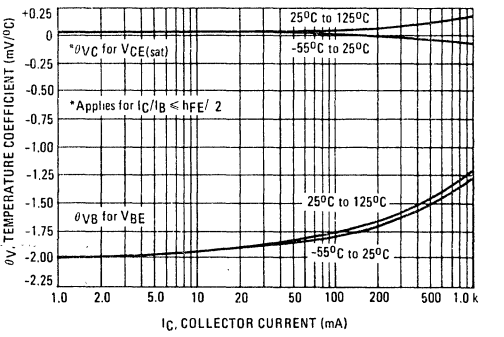
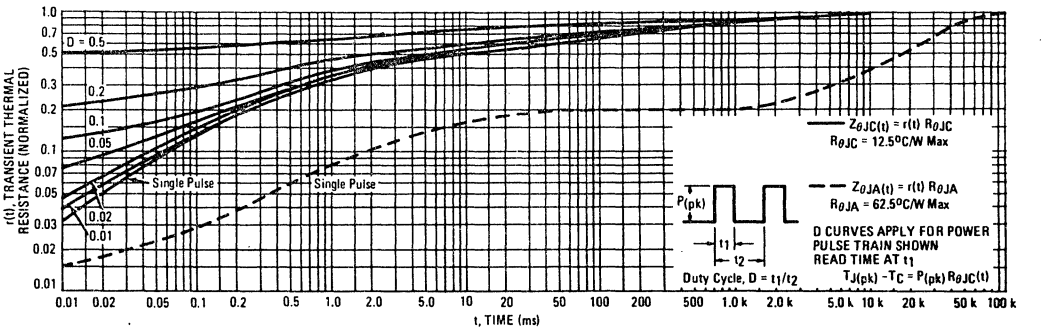


FIGURE 6 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – CAPACITANCE

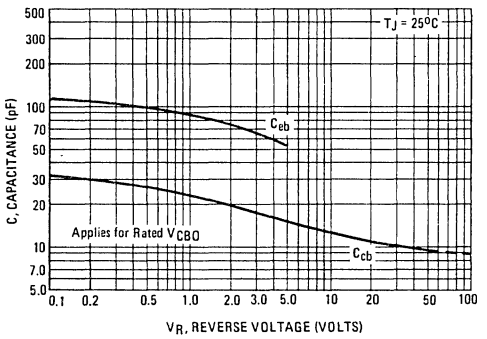
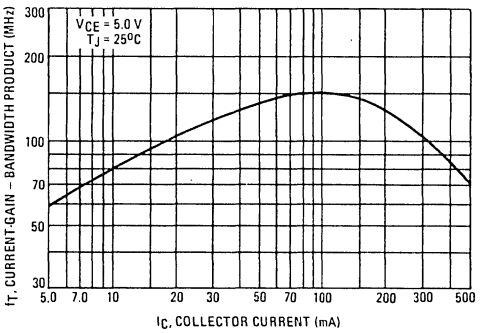


FIGURE 8 – CURRENT-GAIN – BANDWIDTH PRODUCT



4

2N6557
2N6558
2N6559

4

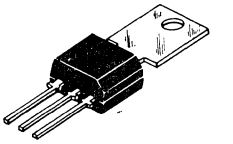
NPN SILICON ANNULAR HIGH VOLTAGE AMPLIFIER TRANSISTORS

. . . designed for high-voltage TV video and chroma output circuits, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage –
  BV_{CEO} = 350 Vdc (Min) @ I_C = 1.0 mAdc – 2N6559
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 30 mAdc
- Low Collector-Base Capacitance –
  C_{cb} = 3.0 pF (Max) @ V_{CB} = 20 Vdc
- Duowatt Package –
  2 Watts Free Air Dissipation @ T_A = 25°C

DUOWATT

NPN SILICON AMPLIFIER TRANSISTORS



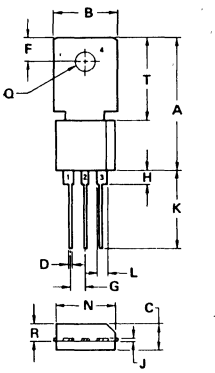
MAXIMUM RATINGS

Rating	Symbol	2N6557	2N6558	2N6559	Unit
*Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
*Collector-Base Voltage	V_{CBO}	250	300	350	Vdc
*Emitter-Base Voltage	V_{EBO}	← 6.0 →			Vdc
*Collector Current – Continuous Peak	I_C	← 0.5 → ← 0.7 →			Adc
*Base Current	I_B	← 250 →			mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 2.0 → ← 16 →			Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 10 → ← 80 →			Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J,T_{stg}	← -55 to +150 →			°C
*Solder Temperature, 1/16" from Case for 10 Seconds	–	← 260 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

*Indicates JEDEC Registered Data.



STYLE 1
PIN 1 EMITTER
2 BASE
3 COLLECTOR
4 COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.19	4.44	0.165	0.175
D	0.61	0.71	0.024	0.028
F	3.68	3.94	0.145	0.155
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.70	–	0.500	–
L	1.78	2.03	0.070	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	2.41	2.67	0.095	0.105
T	13.21	13.97	0.520	0.550

CASE 306-04
TO-202AC

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

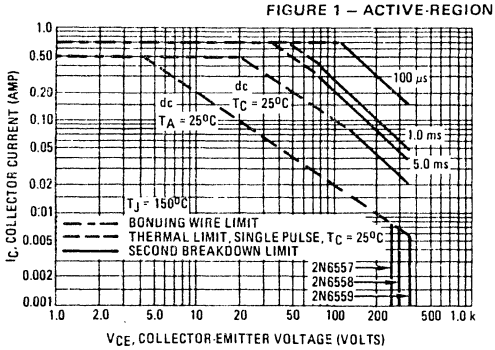
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage		BV_{CEO}			Vdc
(I_C = 1.0 mAdc, I_B = 0)	2N6557		250	–	
	2N6558		300	–	
	2N6559		350	–	
Collector-Base Breakdown Voltage		BV_{CBO}			Vdc
(I_C = 100 μAdc, I_E = 0)	2N6557		250	–	
	2N6558		300	–	
	2N6559		350	–	
Emitter-Base Breakdown Voltage		BV_{EBO}	6.0	–	Vdc
(I_E = 100 μAdc, I_C = 0)					
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 150 Vdc, I_E = 0)	2N6557		–	0.2	
(V_{CB} = 200 Vdc, I_E = 0)	2N6558		–	0.2	
(V_{CB} = 250 Vdc, I_E = 0)	2N6559		–	0.2	
Emitter Cutoff Current		I_{EBO}	–	0.1	μAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)			25	–	
(I_C = 30 mAdc, V_{CE} = 10 Vdc)			40	180	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 30 mAdc, I_B = 3.0 mAdc)			–	0.6	
(I_C = 50 mAdc, I_B = 5.0 mAdc)			–	1.5	
Base-Emitter On Voltage		$V_{BE(on)}$	–	0.85	Vdc
(I_C = 30 mAdc, V_{CE} = 10 Vdc)					
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	45	200	MHz
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)					
Collector-Base Capacitance		C_{cb}	–	3.0	pF
(V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)					

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

4

TYPICAL CHARACTERISTICS (continued)

FIGURE 2 – DC CURRENT GAIN

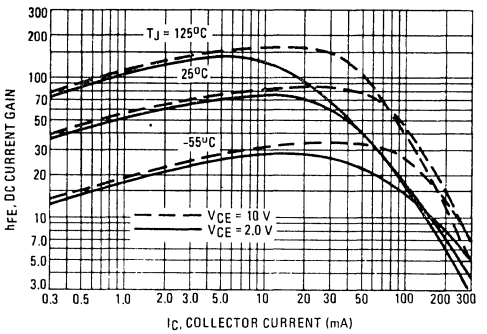


FIGURE 3 – "ON" VOLTAGES

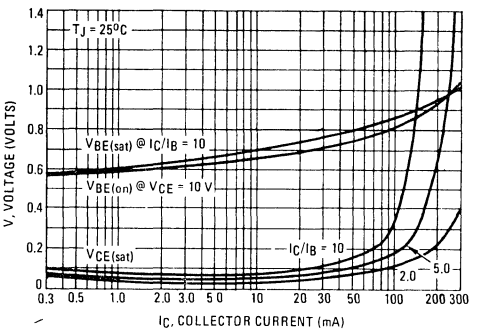


FIGURE 4 – COLLECTOR SATURATION REGION

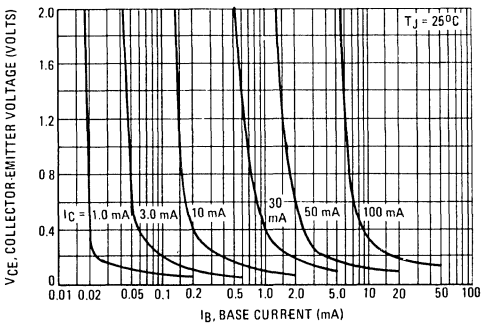


FIGURE 5 – TEMPERATURE COEFFICIENTS

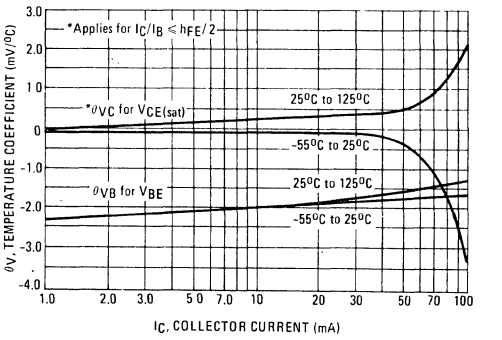
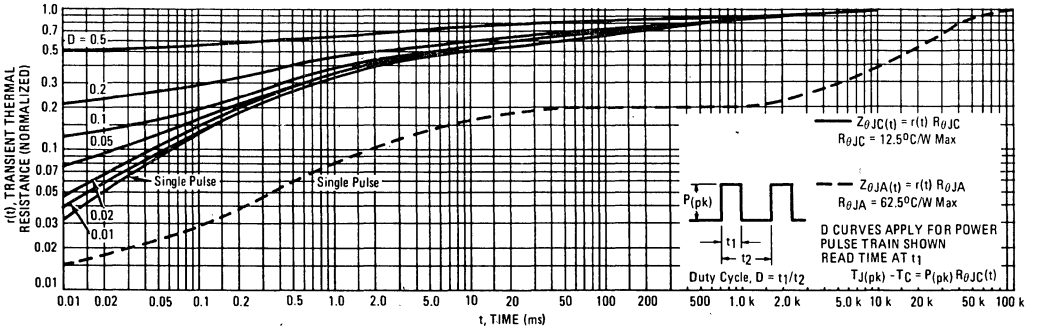


FIGURE 6 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – CAPACITANCE

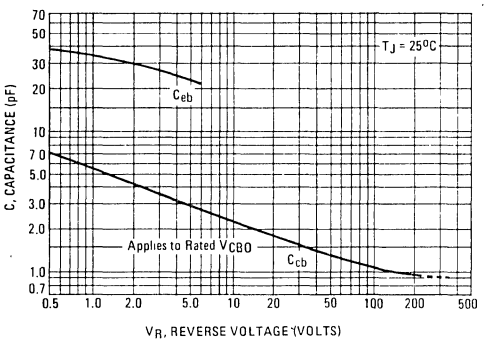
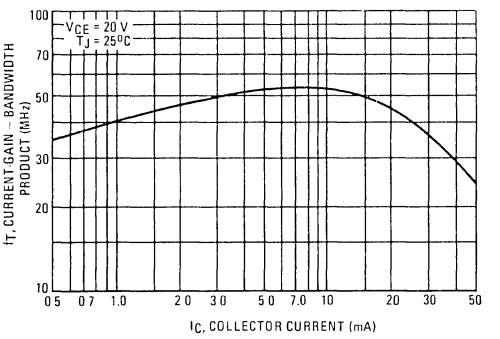


FIGURE 8 – CURRENT-GAIN – BANDWIDTH PRODUCT



4

APPLICATIONS INFORMATION

The 2N6558 is primarily designed for use in the R, G, and B output stages of color television receivers and with a high BV_{CEO}, it can supply the video amplitude requirements of any known system. The low feedback capacitance provides good video bandwidth with modest drive current requirements. Typical drive is from an emitter-follower with a 4.7 k emitter-resistor operated from a 20-Volt supply. It will, therefore, be operable directly from a number of available chroma demodulators. The low output capacitance of this device adds little to the total load capacitance, allowing improved bandwidth for a given collector load resistor. Two typical applications for the 2N6558 are shown in Figures 9 and 10.

Device dissipation will reach approximately 1.6 Watts under worst-case signal conditions and some heat sinking is required at ambient temperature above 50°C.

Used as a color difference output, where drive and bandwidth requirements are less severe, the 2N6558 can be operated with 27 k ohm load resistors (worst-case dissipation would then be only 0.6 Watts). The device can, therefore, be operated as a color-difference output without any heat radiator in ambient temperatures to 150 -(0.6) (62.5) = 112.5°C.

In addition the safe operating area of the 2N6558 will fill the requirements of the luminance output function with a total equivalent load of 5.0 kilohms. Worst-case dissipation can reach 3 Watts, this requires a total $R_{\theta JA}$ of (150-65)/3 = 28.4°C/W. To achieve this a 2" x 3" aluminum plate will be required.

FIGURE 9 – 2N6558 AS RGB OUTPUT WITH RGB INPUT

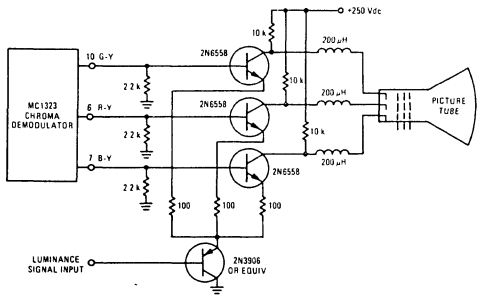
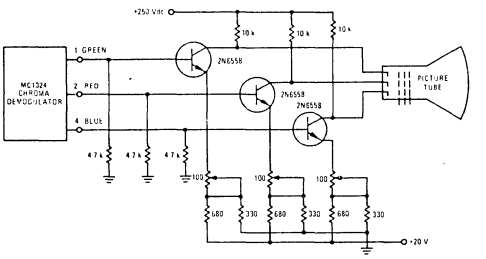


FIGURE 10 – 2N6558 AS RGB OUTPUT, MATRIXING COLOR DIFFERENCE AND LUMINANCE INPUTS



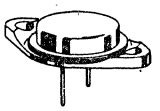
2N6569

NPN SILICON POWER TRANSISTOR

The 2N6569 is a general-purpose, EPIBASE power transistor designed for low voltage amplifier and power switching applications.

- Low Cost
- Safe Operating Area – Full Power Rating to 40 V
- EPIBASE Performance in Gain and Speed
- Metal Can Reliability – TO-3 Package
- All-Purpose Replacement for Industry Standard 2N3055

12 AMPERE
POWER TRANSISTOR
NPN SILICON
40 VOLTS
100 WATTS

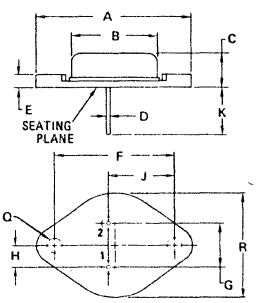


*MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	40	Vdc
Collector-Base Voltage	V_{CBO}	45	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current – Continuous – Peak	I_C	12 24	Adc
Base Current – Continuous – Peak	I_B	5.0 10	Adc
Emitter Current – Continuous – Peak	I_E	17 34	Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	100 0.572	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/16" from Case fo 10s.	T_L	265	^oC



NOTE:
1. DIM "Q" IS DIA.

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

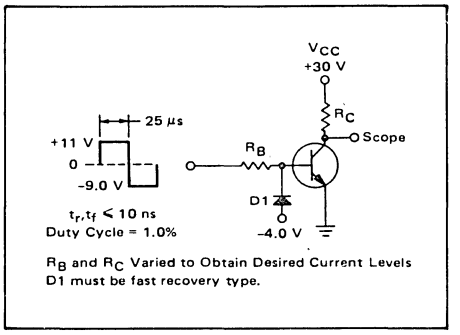
Collector connected to case.
CASE 11-01
(TO-3)

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	40	–	Vdc
Collector Cutoff Current	I_{CEV}			mAdc
(V_{CEV} = 45 Vdc, $V_{BE(off)}$ = 1.5 Vdc)		–	1.0	
(V_{CEV} = 45 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	10	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1.0 s (non-repetitive))	$I_{S/b}$	2.5	–	Adc
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			–
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)		15	200	
(I_C = 12 Adc, V_{CE} = 4.0 Vdc)		5.0	100	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 4.0 Adc, I_B = 0.4 Adc)		–	1.5	
(I_C = 12 Adc, I_B = 2.4 Adc)		–	4.0	
Base-Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 0.4 Adc)	$V_{BE(sat)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 0.5 MHz)	f_T	1.5	15	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)	C_{ob}	75	750	pF
SWITCHING CHARACTERISTICS				
RESISTIVE LOAD				
Delay Time	(V_{CC} = 30 Vdc, I_C = 2.0 Adc, I_{B1} = 0.2 Adc, t_p = 25 μs, Duty Cycle ≤ 1.0%)	t_d	–	0.4	μs
Rise Time		t_r	–	1.5	μs
Storage Time	(V_{CC} = 30 Vdc, I_C = 2.0 Adc, I_{B1} = I_{B2} = 0.2 Adc, t_p = 25 μs, Duty Cycle ≤ 1.0%)	t_s	–	5.0	μs
Fall Time		t_f	–	1.5	μs

*Indicates JEDEC Registered Data.

FIGURE 1 – SWITCHING TIMES TEST CIRCUIT



R_B and R_C Varied to Obtain Desired Current Levels
D1 must be fast recovery type.

FIGURE 2 – THERMAL RESPONSE

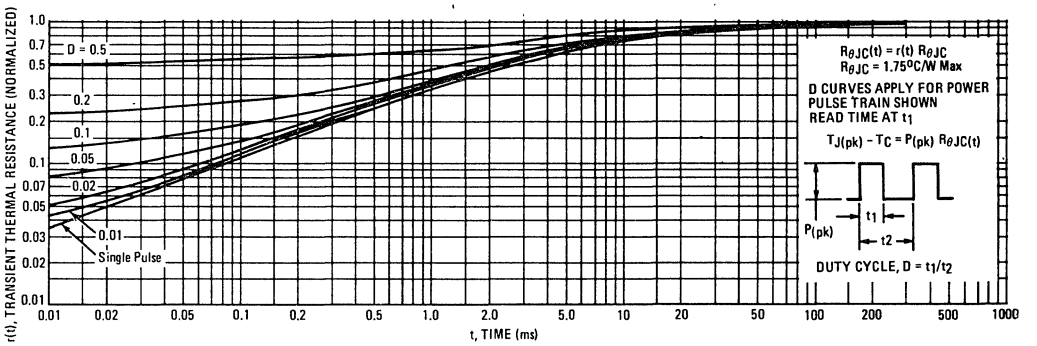
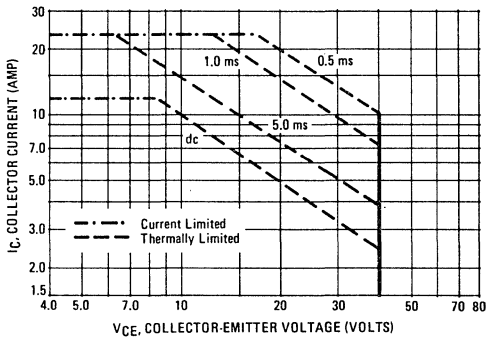


FIGURE 3 – SAFE OPERATING AREA



Safe operating area curves indicate I_C-V_{CE} limits of the transistor being observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. This transistor is thermally limited over its entire operation area. Figure 4 may be used to derate the curves shown or an effective $R_{\theta JC(t)}$ may be computed from Figure 2 for pulsed operation.

FIGURE 4 – POWER DERATING

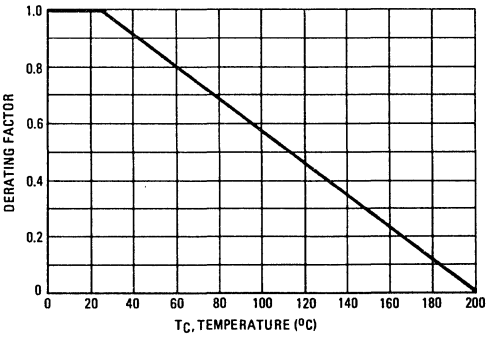


FIGURE 5 – DC CURRENT GAIN

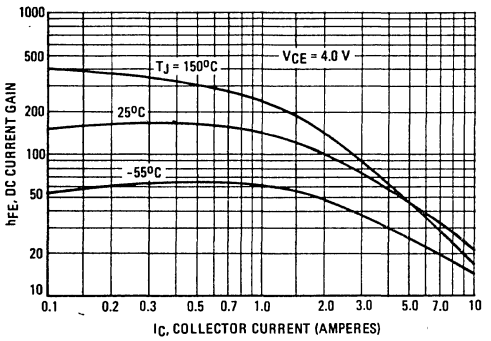


FIGURE 6 – COLLECTOR SATURATION REGION

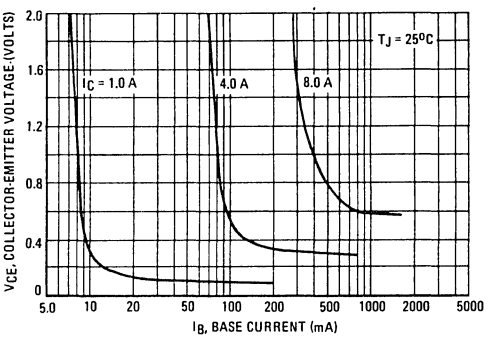


FIGURE 7 – "ON" VOLTAGES

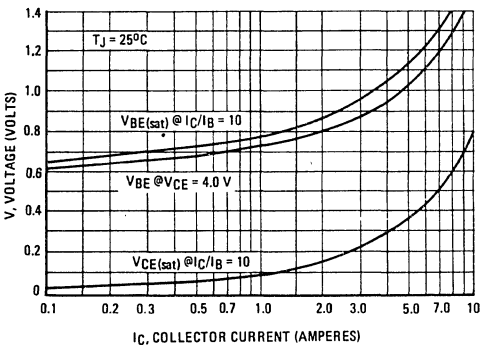
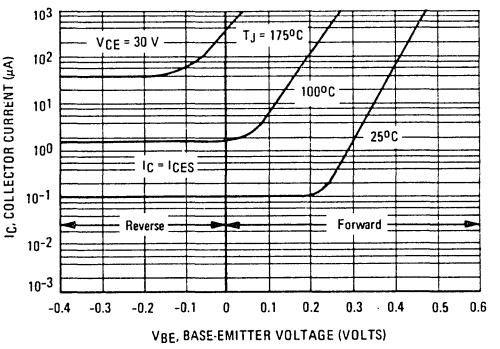


FIGURE 8 – COLLECTOR CUT-OFF REGION



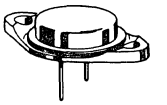
2N6576
2N6577
2N6578

NPN SILICON POWER DARLINGTON TRANSISTORS

General-purpose EpiBase power darlington transistors, suitable for linear and switching applications.

- Replacement for 2N3055 and Driver
- High Gain Darlington Performance
- Built-In Diode Protection for Reverse Polarity Protection
- Can Be Driven from Low-Level Logic
- Popular Voltage Range
- Operating Range – –65 to +200°C

15 AMPERE
POWER TRANSISTORS
NPN SILICON
DARLINGTON
60, 90, 120 VOLTS
120 WATTS



*MAXIMUM RATINGS

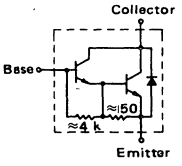
Rating	Symbol	2N6576	2N6577	2N6578	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	60	90	120	Vdc
Collector-Base Voltage	V_{CB}	60	90	120	Vdc
Emitter-Base Voltage	V_{EB}	◄—— 7.0 ——►			Vdc
Collector Current – Continuous – Peak	I_C	◄—— 15 ——► ◄—— 30 ——►			Adc
Base Current – Continuous – Peak	I_B	◄—— 0.25 ——► ◄—— 0.50 ——►			Adc
Emitter Current – Continuous – Peak	I_E	◄—— 15.25 ——► ◄—— 30.5 ——►			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	◄—— 120 ——► ◄—— 0.685 ——►			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	◄—— -65 to +200 ——►			°C

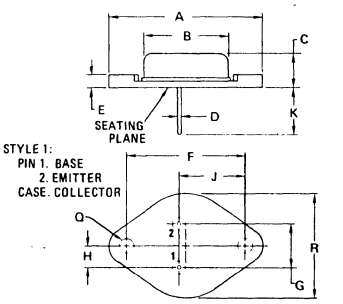
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.46	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/16" from Case for 10s.	T_L	265	°C

*Indicates JEDEC Registered Data

DARLINGTON SCHEMATIC





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-03
TO-3

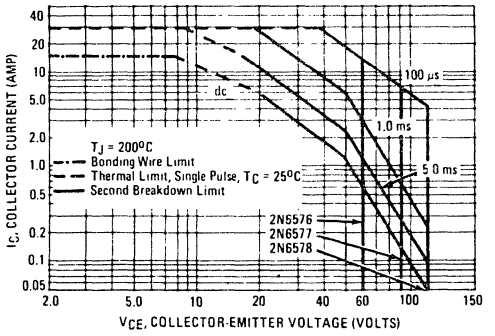
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage(1) (I_C = 200 mAdc, I_B = 0) 2N6576	$V_{CEO(sus)}$	60	–	Vdc
2N6577		90	–	
2N6578		120	–	
Collector Cutoff Current (V_{CE} = Rated Value)	I_{CEO}	–	1.0	mAdc
Collector Cutoff Current (V_{CER} = Rated $V_{CEO(sus)}$ Value, R_{BE} = 10 kΩ, T_C = 150°C)	I_{CER}	–	5.0	mAdc
Collector Cutoff Current V_{CEX} = Rated $V_{CEO(sus)}$ Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	5.0	mAdc
Collector Cutoff Current (V_{CB} = Rated Value)	I_{CBO}	–	0.5	mAdc
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			–
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)		100	–	
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)		500	5,000	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)		2000	20,000	
(I_C = 0.4 Adc, V_{CE} = 3.0 Vdc)		200	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 15 Adc, I_B = 0.15 Adc)		–	4.0	
(I_C = 10 Adc, I_B = 0.1 Adc)		–	2.8	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 15 Adc, I_B = 0.15 Adc)		–	4.5	
(I_C = 10 Adc, I_B = 0.1 Adc)		–	3.5	
Collector-Emitter Diode Voltage Drop (I_{EC} = 15 Adc)	V_F	–	4.5	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common-Emitter Small-Signal Short-Circuit Current Transfer Ratio (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)	$\lvert h_{fe} \rvert$	10	200	–
SWITCHING CHARACTERISTICS				
RESISTIVE LOAD (Figure 2)				
Delay Time (V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = 0.1 Adc, t_p = 300 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.15	μs
Rise Time	t_r	–	1.0	μs
Storage Time (V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 0.1 Adc, t_p = 300 μs, Duty Cycle ≤ 2.0%)	t_s	–	2.0	μs
Fall Time	t_f	–	7.0	μs

*Indicates JEDEC Registered Data

(1) Pulse test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 – RATED FORWARD BIASED SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10%.

$T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 – DC CURRENT GAIN

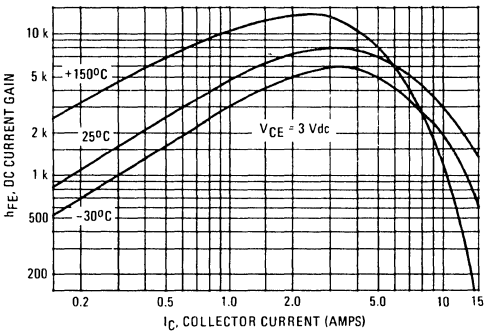


FIGURE 3 – COLLECTOR-SATURATION REGION

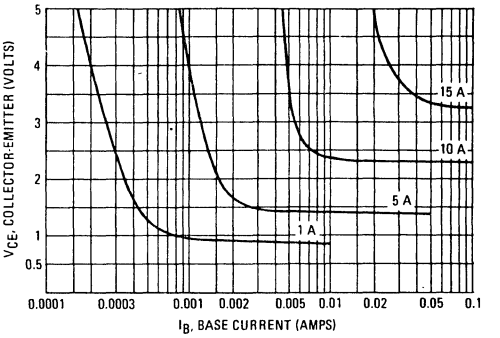


FIGURE 4 – COLLECTOR SATURATION VOLTAGE

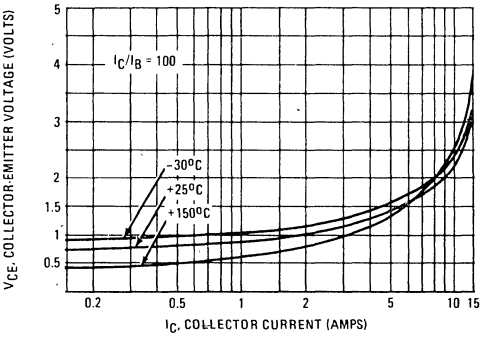


FIGURE 5 – BASE-EMITTER VOLTAGE

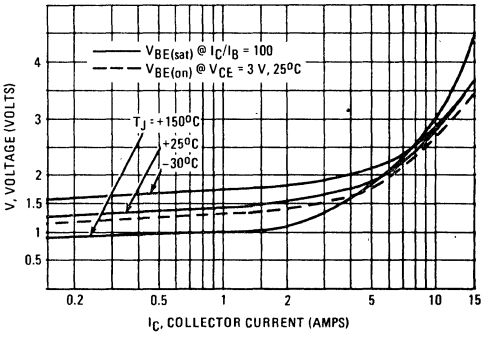


FIGURE 6 – THERMAL RESPONSE

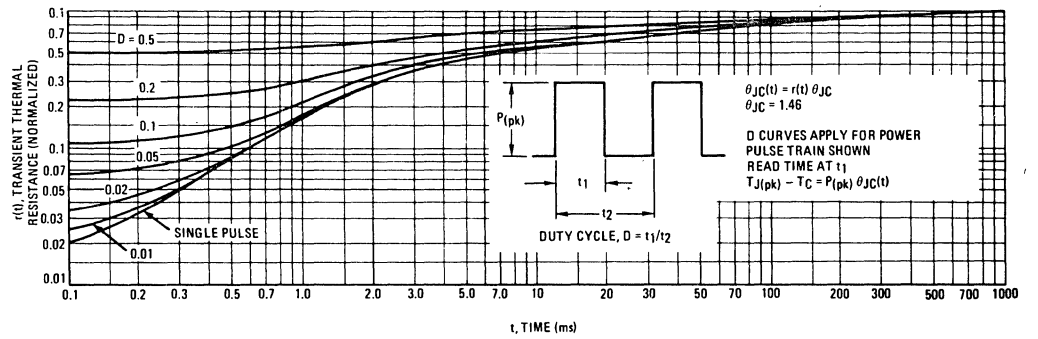
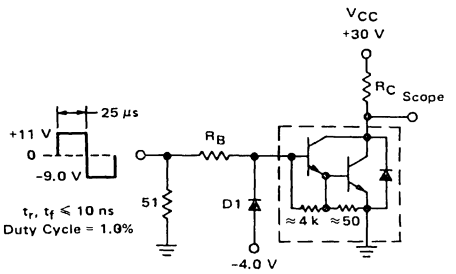


FIGURE 7 – SWITCHING TIMES TEST CIRCUIT



R_B and R_C Varied to Obtain Desired Current Levels
D1 Must be Fast Recovery Type, eg:

FIGURE 8 – SWITCHING TIMES

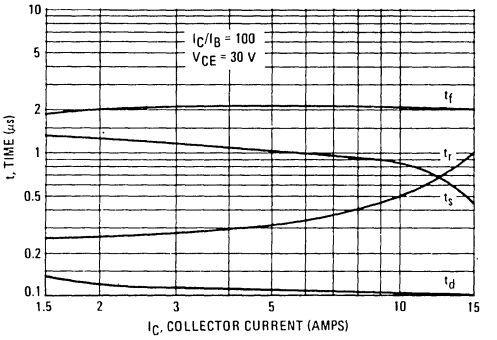


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FIGURE 9 – COLLECTOR CUT-OFF REGION

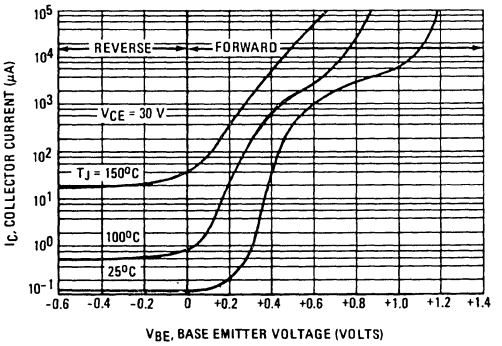


FIGURE 10 – CAPACITANCE

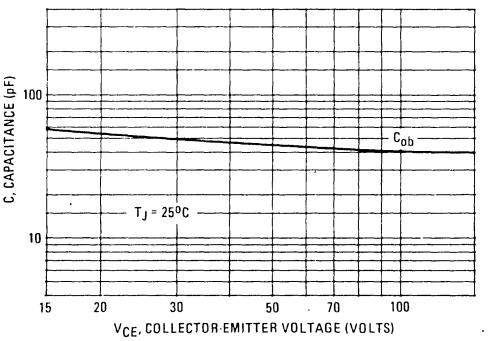
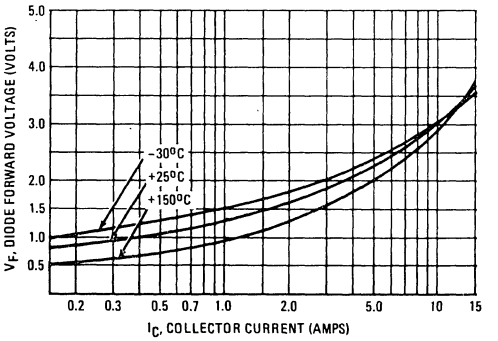


FIGURE 11 – COLLECTOR-EMITTER VOLTAGE



2N6591
2N6592
2N6593

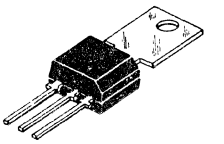
NPN SILICON ANNULAR HIGH VOLTAGE AMPLIFIER TRANSISTORS

. . . designed for horizontal drive applications, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage –
  BV_{CEO} = 250 Vdc (Min) @ I_C = 1.0 mAdc – 2N6593
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 200 mAdc
- Duowatt Package –
  2 Watts Free Air Dissipation @ T_A = 25°C

DUOWATT

NPN SILICON AMPLIFIER TRANSISTORS



MAXIMUM RATINGS

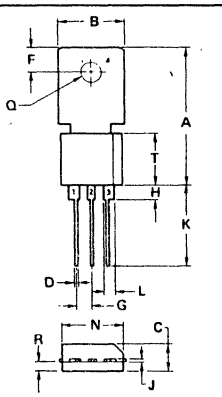
Rating	Symbol	2N6591	2N6592	2N6593	Unit
*Collector-Emitter Voltage	V_{CEO}	150	200	250	Vdc
*Collector-Base Voltage	V_{CBO}	150	200	250	Vdc
*Emitter-Base Voltage	V_{EBO}	← 5.0 →			Vdc
*Collector Current – Continuous Peak (1)	I_C	← 0.5 → ← 1.0 →			Adc
*Base Current	I_B	← 100 →			mAdc
*Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	← 2.0 → ← 16 →			Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 10 → ← 80 →			Watts mW/°C
*Operating and Storage Junction Temperature Range	T_J,T_{stg}	← -55 to +150 →			°C
*Solder Temperature, 1/16" from Case for 10 Seconds	–	← 260 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 1.0 ms, Duty Cycle ≤ 50%.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04
TO-202AC

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage		BV_{CEO}			Vdc
(I_C = 1.0 mAdc, I_B = 0)	2N6591		150	–	
	2N6592		200	–	
	2N6593		250	–	
Collector-Base Breakdown Voltage		BV_{CBO}			Vdc
(I_C = 100 μAdc, I_E = 0)	2N6591		150	–	
	2N6592		200	–	
	2N6593		250	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 100 Vdc, I_E = 0)	2N6591		–	0.2	
(V_{CB} = 150 Vdc, I_E = 0)	2N6592		–	0.2	
(V_{CB} = 200 Vdc, I_E = 0)	2N6593		–	0.2	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			
(I_C = 10 mAdc, V_{CE} = 10 Vdc)	2N6591		40	250	
	2N6592		30	250	
	2N6593		30	250	
(I_C = 100 mAdc, V_{CE} = 10 Vdc)	2N6591		40	200	
	2N6592		40	200	
	2N6593		30	200	
Collector-Emitter Saturation Voltage (I_C = 200 mAdc, I_B = 20 mAdc)		$V_{CE(sat)}$	–	0.8	Vdc
Base-Emitter On Voltage (I_C = 100 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 50 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)		f_T	35	300	MHz
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	–	12	pF

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 – CURRENT-GAIN – BANDWIDTH PRODUCT

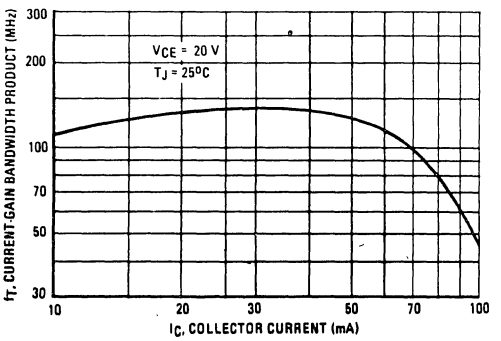
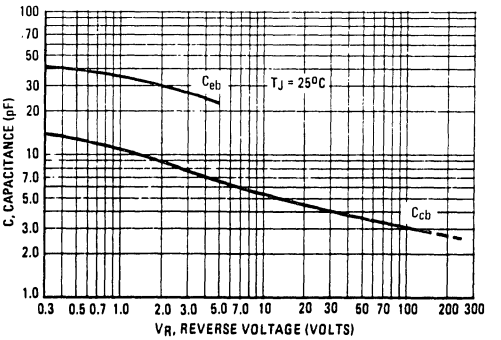


FIGURE 2 – CAPACITANCE



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TYPICAL CHARACTERISTICS (Continued)

FIGURE 3 – DC CURRENT GAIN

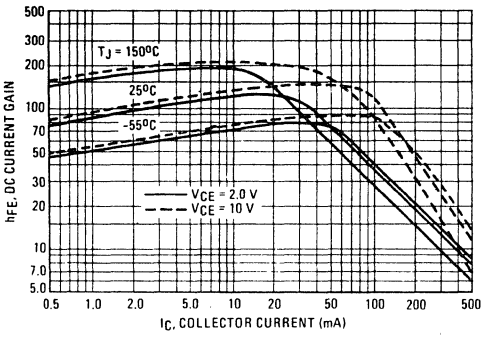


FIGURE 4 – "ON" VOLTAGE

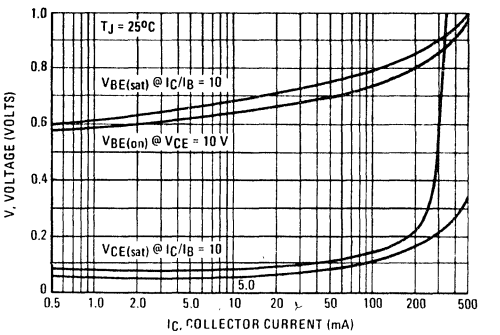


FIGURE 5 – COLLECTOR SATURATION REGION

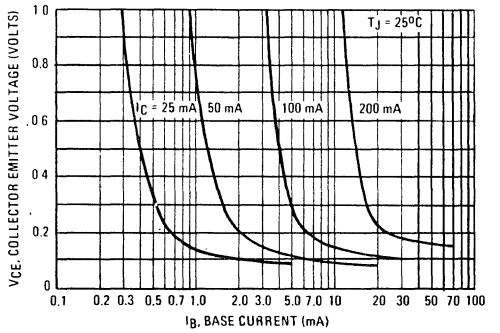


FIGURE 6 – TEMPERATURE COEFFICIENTS

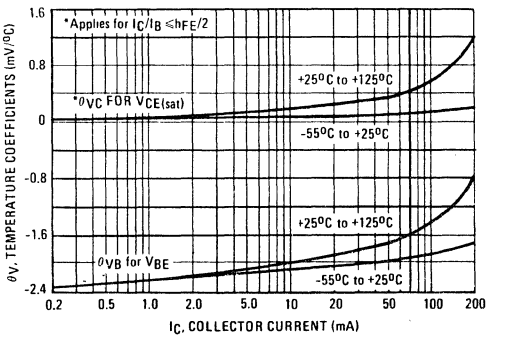


FIGURE 7 – COLLECTOR CHARACTERISTICS

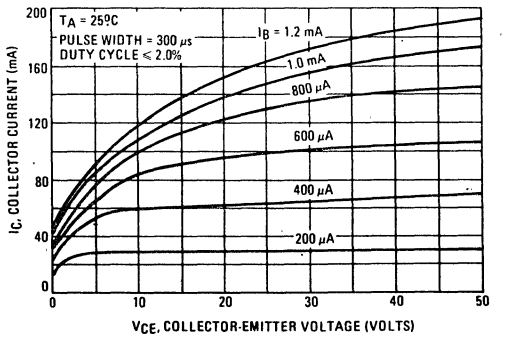
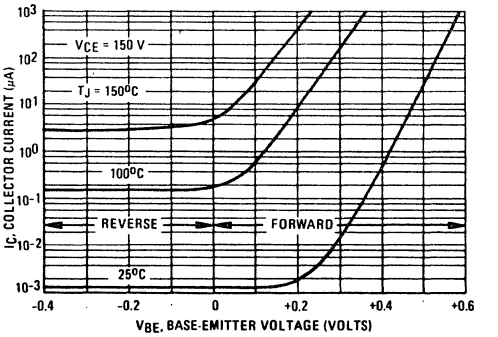


FIGURE 8 – COLLECTOR CUTOFF REGION



TYPICAL CHARACTERISTICS (Continued)

FIGURE 9 – THERMAL RESPONSE

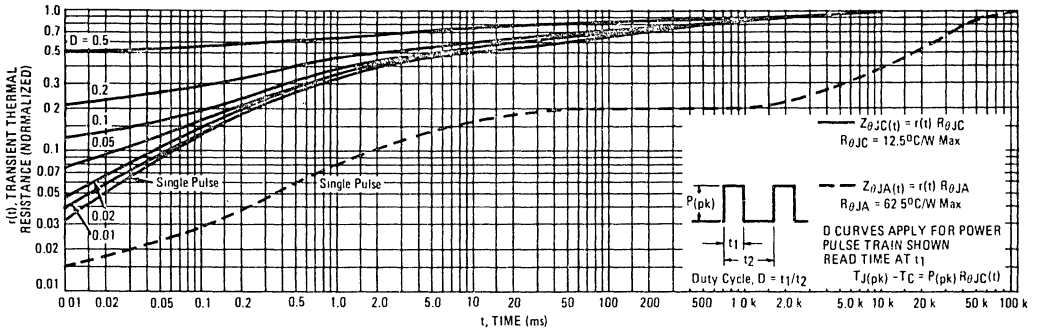


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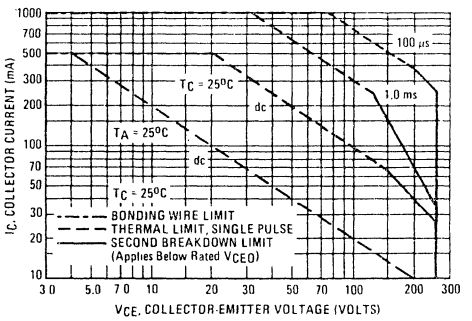
FIGURE 10 – ACTIVE REGION SAFE-OPERATING AREA

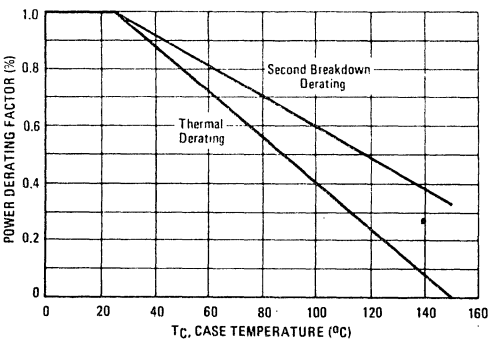


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25^{\circ}C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^{\circ}C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 – POWER DERATING



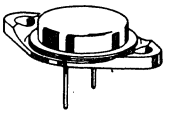
2N6594

PNP SILICON POWER TRANSISTOR

The 2N6594 is a general-purpose, EPI-BASE▲ power transistor designed for low voltage amplifier and power switching applications. It is a complement to the NPN 2N6569.

- Safe Operating Area – Full Power Rating to 40 V
- EPI-BASE Performance in Gain and Speed
- Lower Voltage, Economical Complement to the 2N3055

12 AMPERE
POWER TRANSISTOR
PNP SILICON
40 VOLTS
100 WATTS

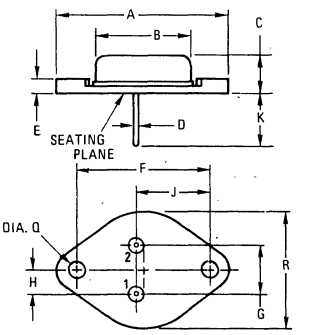


***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	40	Vdc
Collector-Base Voltage	V_{CBO}	45	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector Current – Continuous – Peak	I_C	12 24	Adc
Base Current – Continuous – Peak	I_B	5 10	Adc
Emitter Current – Continuous – Peak	I_E	17 34	Adc
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	100 0.572	Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/16" from Case for 10 seconds	T_L	265	^oC



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	40	–	Vdc
Collector Cutoff Current (V_{CEV} = 45 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	1	mAdc
(V_{CEV} = 45 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	10	
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	–	5	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1 s (non-repetitive))	$I_{S/b}$	2.5	–	Adc
ON CHARACTERISTICS				
DC Current Gain (I_C = 4 Adc, V_{CE} = 3 Vdc)	h_{FE}	15	200	–
(I_C = 12 Adc, V_{CE} = 4 Vdc)		5	100	
Collector-Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	–	1.5	Vdc
(I_C = 12 Adc, I_B = 2.4 Adc)		–	4	
Base-Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{BE(sat)}$	–	2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_C = 1 Adc, V_{CE} = 4 Vdc, f_{test} = 0.5 MHz)	f_T	2.5	25	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	100	1000	pF
SWITCHING CHARACTERISTICS				
RESISTIVE LOAD				
Delay Time	(V_{CC} = 30 Vdc, I_C = 2 Adc, I_{B1} = 0.2 Adc, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	–	0.4 μs
Rise Time		t_r	–	1.5 μs
Storage Time	(V_{CC} = 30 Vdc, I_C = 2 Adc, I_{B1} = I_{B2} = 0.2 Adc, t_p = 25 μs, Duty Cycle ≤ 1%)	t_s	–	5 μs
Fall Time		t_f	–	1.5 μs

*Indicates JEDEC Registered Data.

(1) Pulse Test, PW = 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 – SWITCHING TIMES TEST CIRCUIT

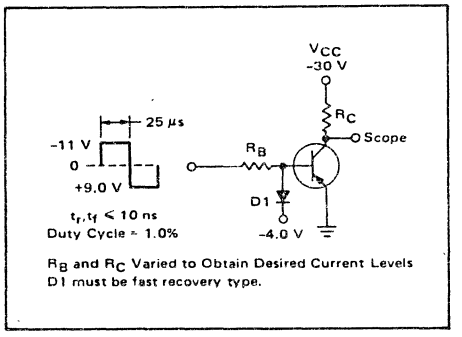


FIGURE 2 – THERMAL RESPONSE

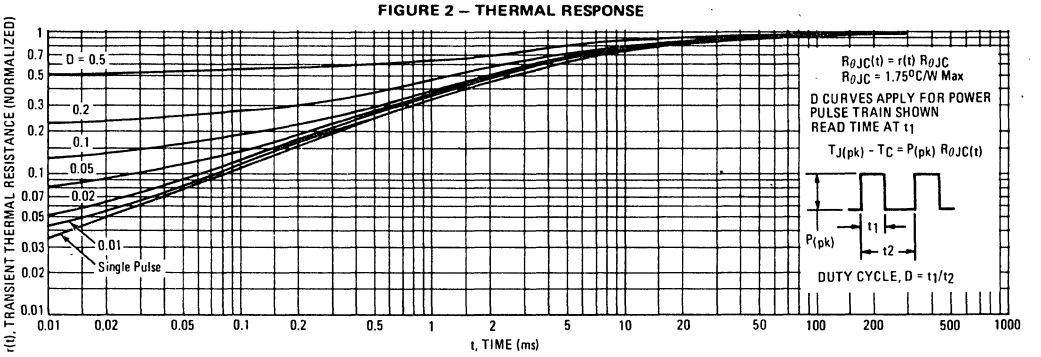
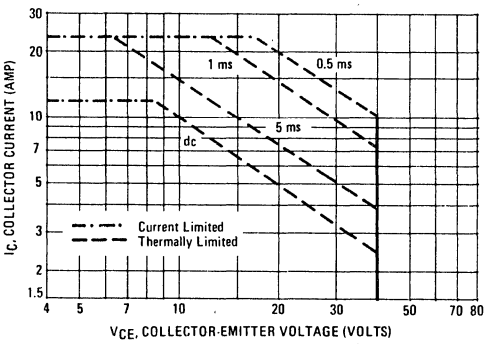


FIGURE 3 – SAFE OPERATING AREA



Safe operating area curves indicate I_C-V_{CE} limits of the transistor being observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. Figure 4 may be used to derate the curves shown or an effective $R_{\theta JC(t)}$ may be computed from Figure 2 for pulsed operation.

FIGURE 4 – POWER DERATING

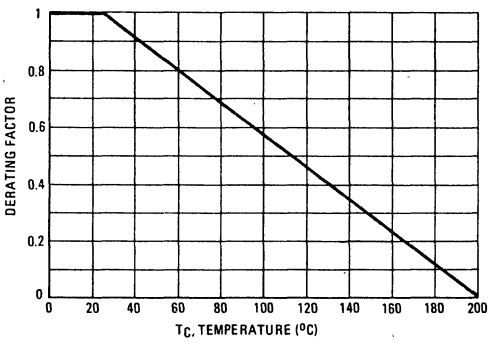


FIGURE 5 – DC CURRENT GAIN

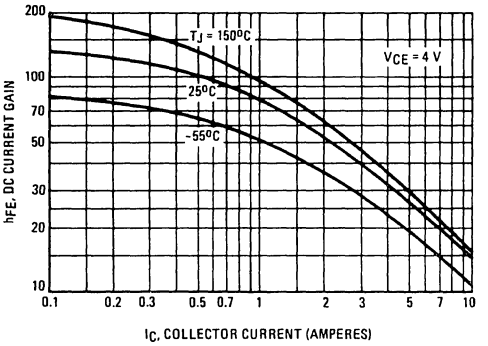
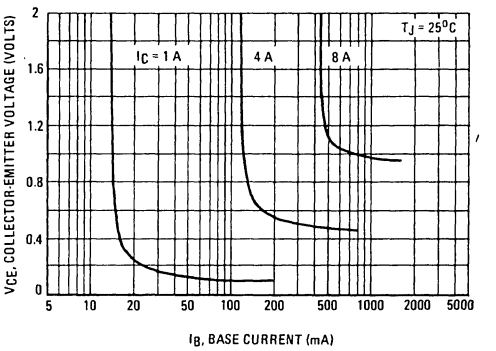


FIGURE 6 – COLLECTOR SATURATION REGION



4

FIGURE 7 – "ON" VOLTAGES

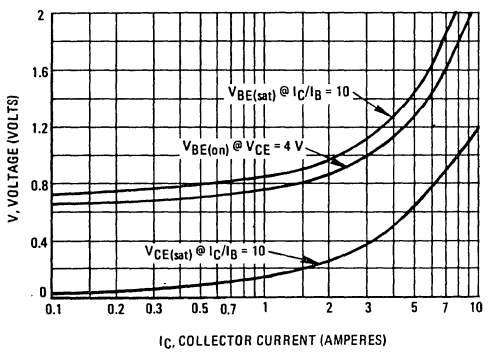
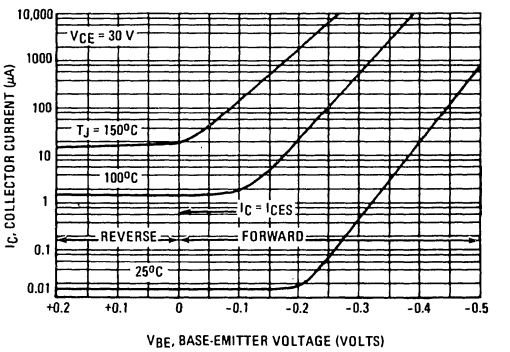


FIGURE 8 – COLLECTOR CUT-OFF REGION



BU204
BU205

Designers Data Sheet

HORIZONTAL DEFLECTION TRANSISTOR

. . . specifically designed for use in large screen color deflection circuits.

- Collector-Emitter Voltage – V_{CEX} = 1300 Vdc – BU204
  1500 Vdc – BU205
- Glassivated Base-Collector Junction
- Switching Times with Inductive Loads –
  t_f = 0.65 μs (Typ) @ I_C = 2A

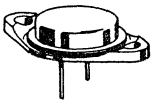
2.5 AMPERE

NPN SILICON POWER TRANSISTORS

1300 AND 1500 VOLTS
36 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



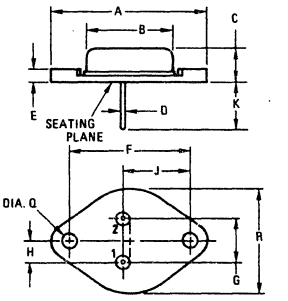
MAXIMUM RATINGS

Rating	Symbol	BU204	BU205	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	600	700	Vdc
Collector-Emitter Voltage	V_{CEX}	1300	1500	Vdc
Emitter Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	2.5 3		Adc
Base Current – Peak (1)	I_{BM}	2.5		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 90°C Derate above 25°C	P_D	36 10 0.4		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +115		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

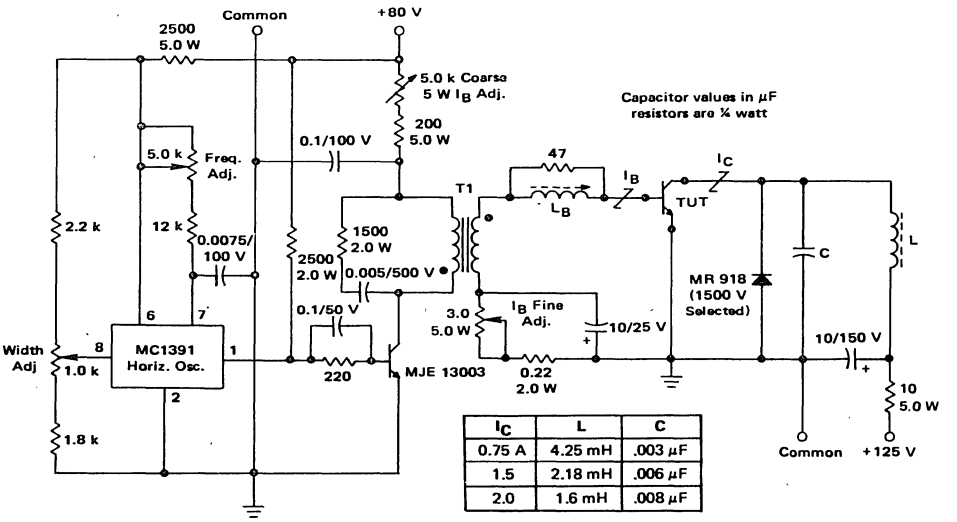
CASE 11-01
TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	BU204 BU205	$V_{CEO(sus)}$	600 700	– –	– –	Vdc
Collector Cutoff Current (V_{CE} = 1300 Vdc, V_{BE} = 0) (V_{CE} = 1500 Vdc, V_{BE} = 0)	 BU204 BU205	I_{CES}	 – –	 – –	 1.0 1.0	mAdc
Emitter Base Voltage (I_E = 10 mA, I_C = 0)		V_{EBO}	5.0	–	–	Vdc
ON CHARACTERISTICS (1)						
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 1.0 Adc)		$V_{CE(sat)}$	–	–	5.0	Vdc
Base Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	–	–	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased		$I_{S/B}$	See Figure 14			
DYNAMIC CHARACTERISTICS						
Current-Gain – Bandwidth Product (1) (I_C =0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)		f_T	–	4.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	50	–	pF
SWITCHING CHARACTERISTICS						
Fall Time (I_C = 2.0 Adc, I_{B1} = 1.0 Adc, L_B = 25 μH) (See Figure 1)		t_f	–	0.65	–	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

FIGURE 1 – TEST CIRCUIT



I_C	L	C
0.75 A	4.25 mH	.003 μF
1.5	2.18 mH	.006 μF
2.0	1.6 mH	.008 μF

DRIVER TRANSFORMER (T1)

Motorola part number 25D68782A-05-1/4" laminate "E" iron core. Primary Inductance – 39 mH. Secondary Inductance – 22 mH, Leakage Inductance with primary shorted – 2.0 μH, Primary 260 turns #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.

BASE DRIVE: The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B as shown in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1}, and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when $I_{B1}\ h_{FE} = I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the $I_{B1}\ h_{FE} = I_{CM}$ point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor initiation of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left or right according to the relation $I_{B1}\ h_{FE}$ = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM}. These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

TEST CIRCUIT WAVEFORMS

FIGURE 2

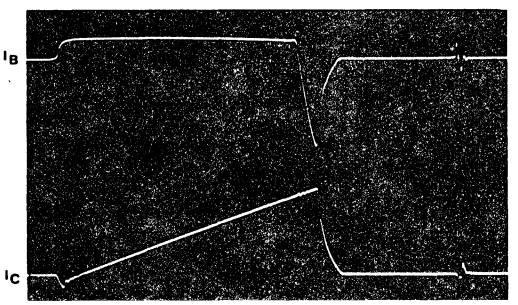
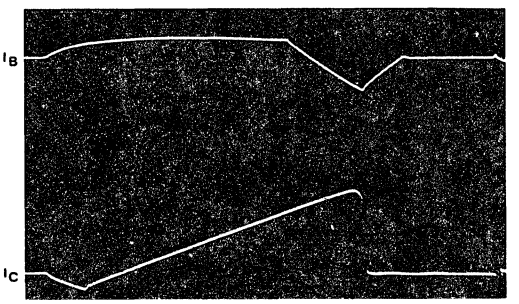


FIGURE 3



TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance.

Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

FIGURE 4 – OPTIMIZING DRIVE @ I_C = 0.75 A

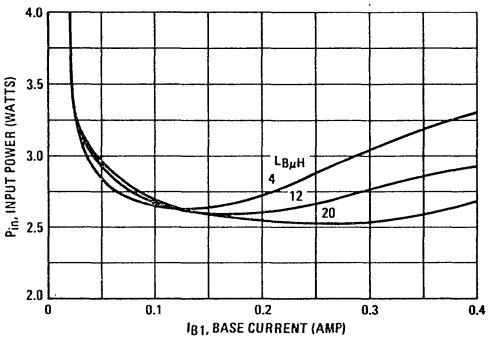


FIGURE 5 – OPTIMIZING DRIVE @ I_C 1.5 A

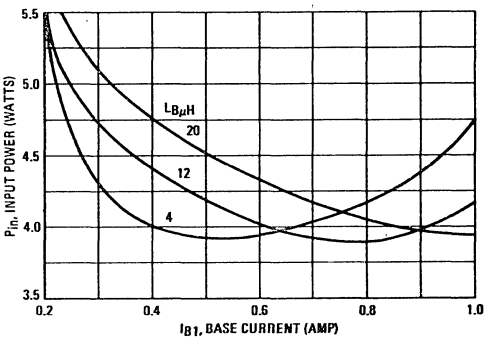


FIGURE 6 – OPTIMIZING DRIVE @ I_C = 2.0 A

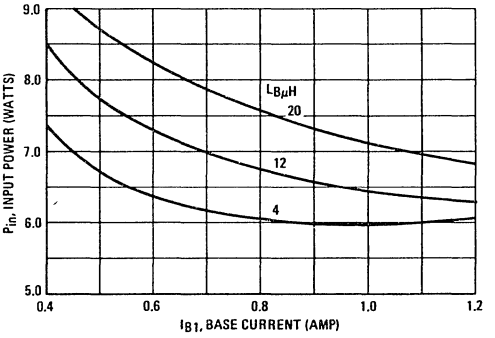


FIGURE 7 – SWITCHING BEHAVIOR versus TEMPERATURE

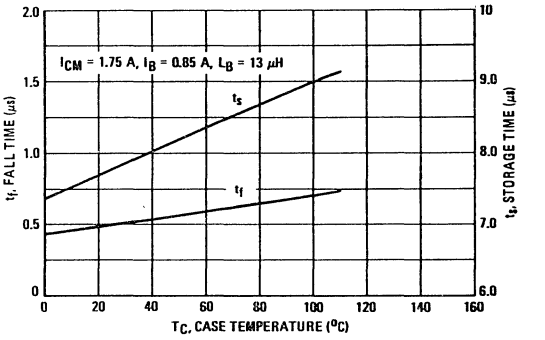


FIGURE 8 – OPTIMUM DRIVE CONDITIONS

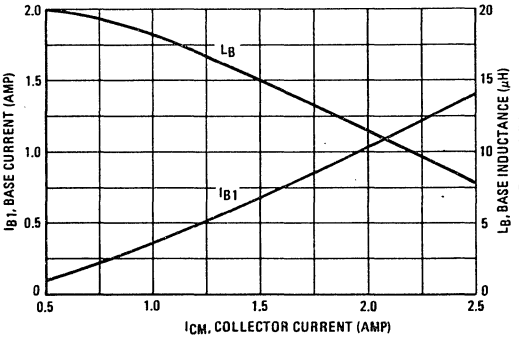


FIGURE 9 – SWITCHING BEHAVIOR versus I_{CM}

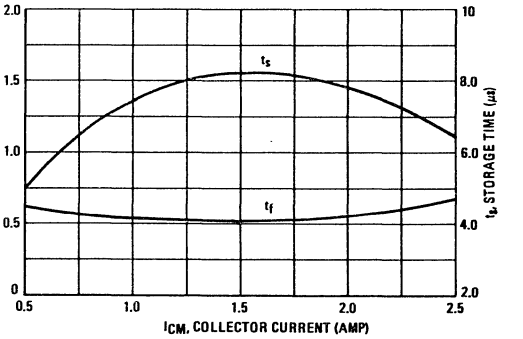


FIGURE 10 – THERMAL RESPONSE

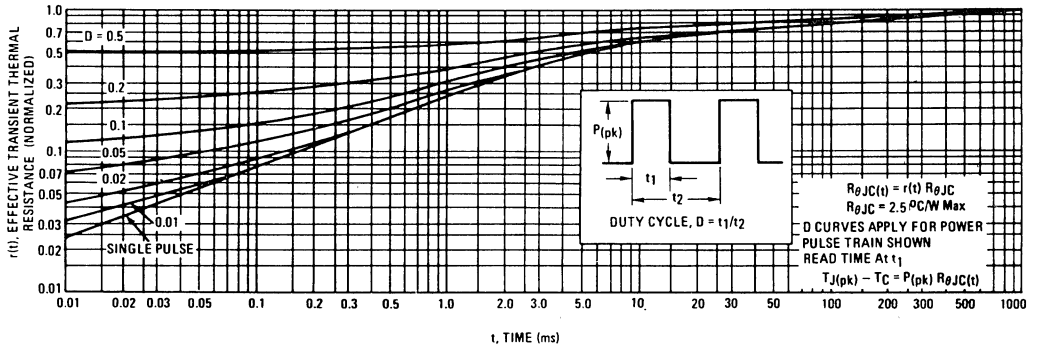


FIGURE 11 – COLLECTOR SATURATION REGION

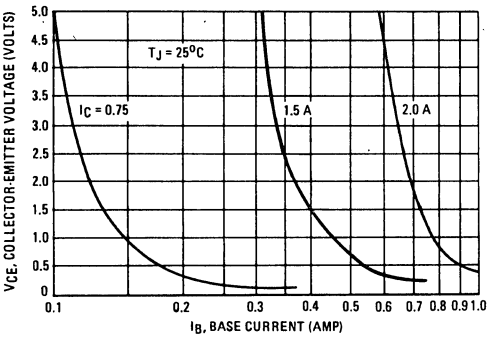


FIGURE 12 – DC CURRENT GAIN

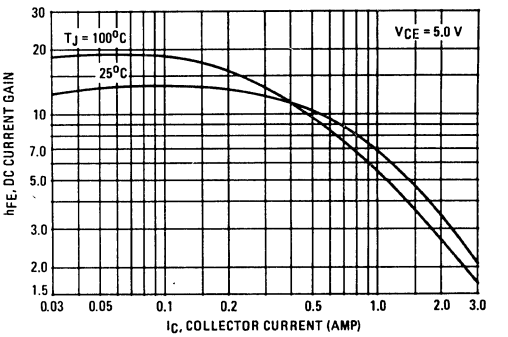


FIGURE 13 – "ON" VOLTAGES

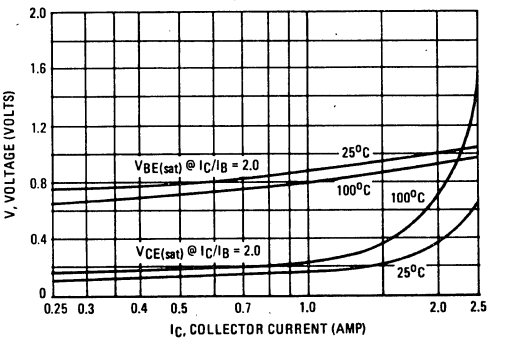
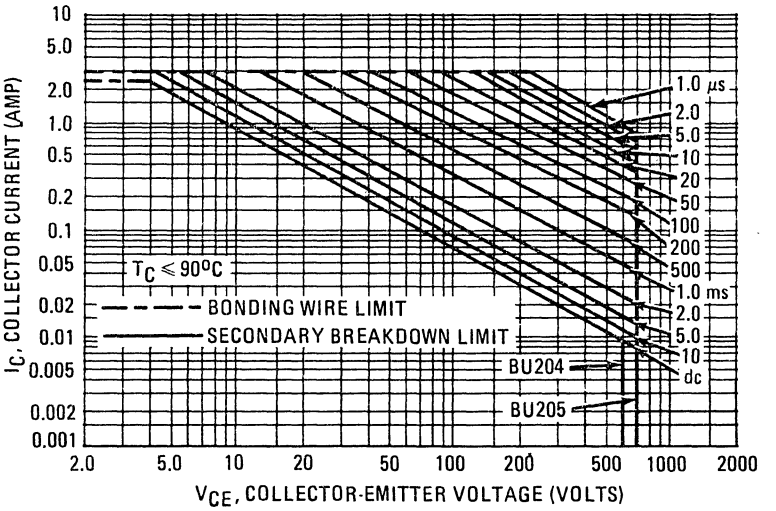


FIGURE 14 – MAXIMUM FORWARD BIAS
SAFE OPERATING AREA



4

BU207
BU208

Designers Data Sheet

HORIZONTAL DEFLECTION TRANSISTOR

. . . specifically designed for use in large screen color deflection circuits.

- Collector-Emitter Voltage —
  V_{CEX} = 1300 Vdc — BU207
  1500 Vdc — BU208
- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 600 Vdc — BU207
  700 Vdc — BU208
- Switching Times with Inductive Loads, t_f = 0.4 μs (Typ) @ I_C = 4.5 A
- Optimum Drive Condition Curves
- Glass Base-Collector Junction

5 AMPERE NPN SILICON POWER TRANSISTORS

1300 AND 1500 VOLTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

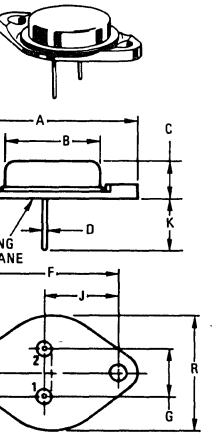
***MAXIMUM RATINGS**

Rating	Symbol	BU207	BU208	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	600	700	Vdc
Collector-Emitter Voltage	V_{CEX}	1300	1500	Vdc
Emitter Base Voltage	V_{EB}	5		Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	5 7.5		Adc
Base Current — Peak (1)	I_{BM}	4		Adc
Total Power Dissipation @ T_C = 95°C Derate above 95°C	P_D	12.5 0.625		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +115		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	1.6	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050

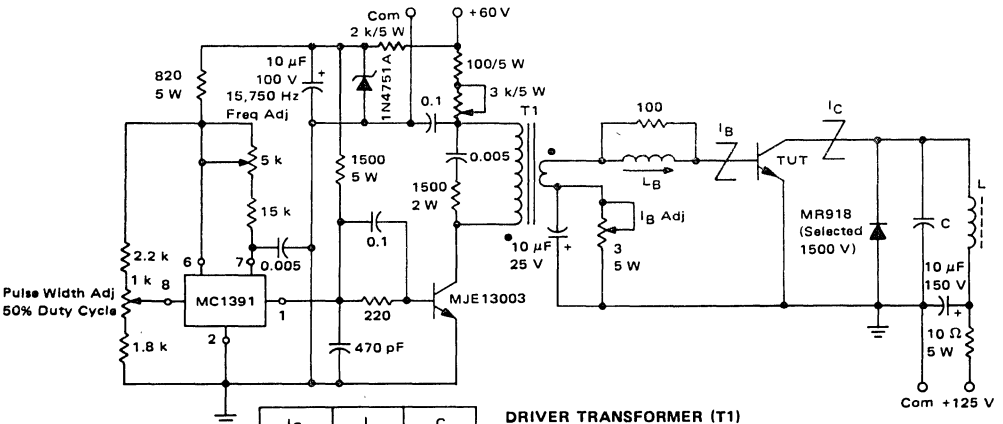
Collector connected to case.
CASE 11-01

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	BU208	$V_{CEO(sus)}$	600	–	–	Vdc
	BU207		700	–	–	
Collector Cutoff Current		I_{CES}				Vdc
(V_{CE} = 1500 Vdc, V_{BE} = 0)	BU208		–	–	1.0	
(V_{CE} = 1300 Vdc, V_{BE} = 0)	BU207		–	–	1.0	
Emitter Base Voltage (I_E = 10 mA, I_C = 0)		V_{EBO}	5.0	–	–	Vdc
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 4.5 Adc, V_{CE} = 5 Vdc)		h_{FE}	2.25	–	–	–
Collector-Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2 Adc)		$V_{CE(sat)}$	–	–	5	Vdc
Base Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2 Adc)		$V_{BE(sat)}$	–	–	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$		See Figure 14		
DYNAMIC CHARACTERISTICS						
Current-Gain – Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1 MHz)		f_T	–	4.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	125	–	pF
SWITCHING CHARACTERISTICS						
Fall Time	(I_C = 4.5 Adc, I_B = 1.8 Adc, L_B = 10 μH, see Figure 1)	t_f	–	0.6	–	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 – SWITCHING TIMES TEST CIRCUIT



I_C A	L mH	C μF
3.5	0.87	0.013
4.5	0.67	0.017

DRIVER TRANSFORMER (T1)

Motorola part number 25D68782A-05-1/4" laminate "E" iron core. Primary Inductance – 39 mH, Secondary Inductance – 0.22 mH, Leakage Inductance with primary shorted – 2.0 μH. Primary 260 turns, #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.

4

BASE DRIVE: The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst-case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B as shown in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1}, and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when $I_{B1}\ h_{FE} = I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the $I_{B1}\ h_{FE} = I_{CM}$ point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor *initiation* of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left or right according to the relation $I_{B1}\ h_{FE}$ = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM}. These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

TEST CIRCUIT WAVEFORMS

FIGURE 2

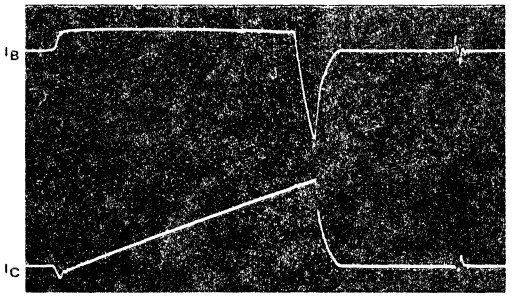
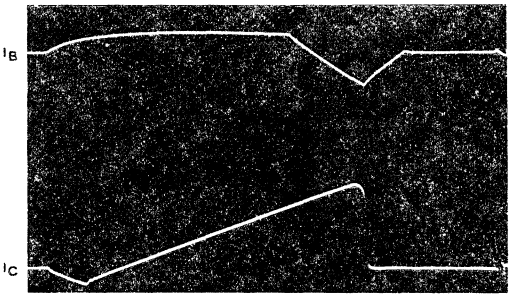


FIGURE 3



TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance.

Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

FIGURE 4 – OPTIMIZING DRIVE @ I_C = 3.5 A

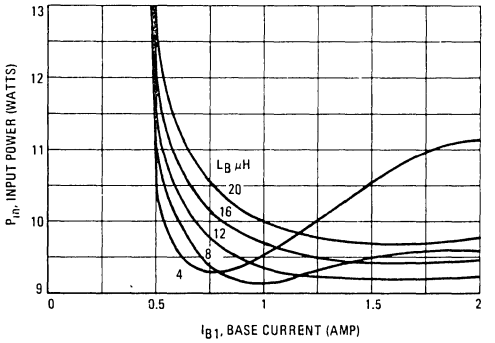
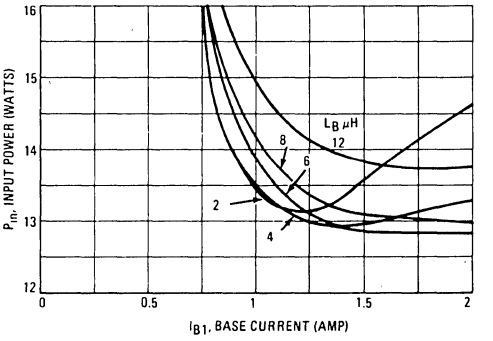


FIGURE 5 – OPTIMIZING DRIVE @ I_C = 4.5 A



4

FIGURE 6 – SWITCHING BEHAVIOR versus TEMPERATURE
I_{CM} = 3.5 A, I_B = 1.5 A, L_B = 14 μH

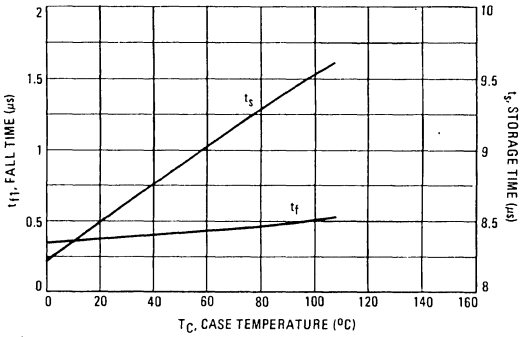


FIGURE 7 – SWITCHING BEHAVIOR versus TEMPERATURE
I_{CM} = 4.5 A, I_B = 1.75 A, L_B = 8 μH

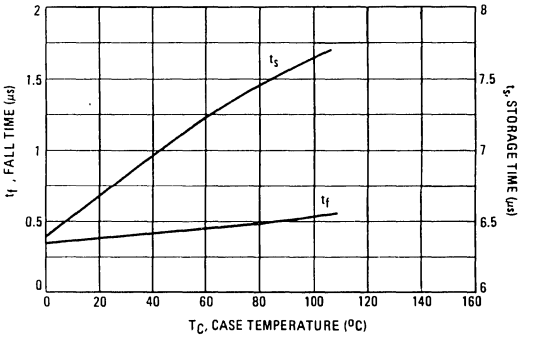


FIGURE 8 – OPTIMUM DRIVE CONDITIONS

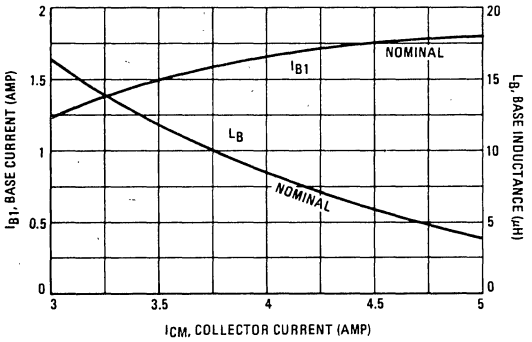


FIGURE 9 – SWITCHING BEHAVIOR versus I_{CM}

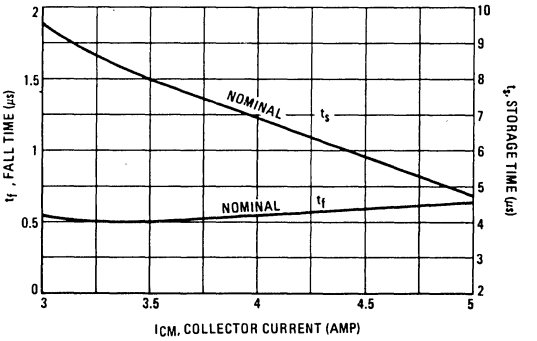
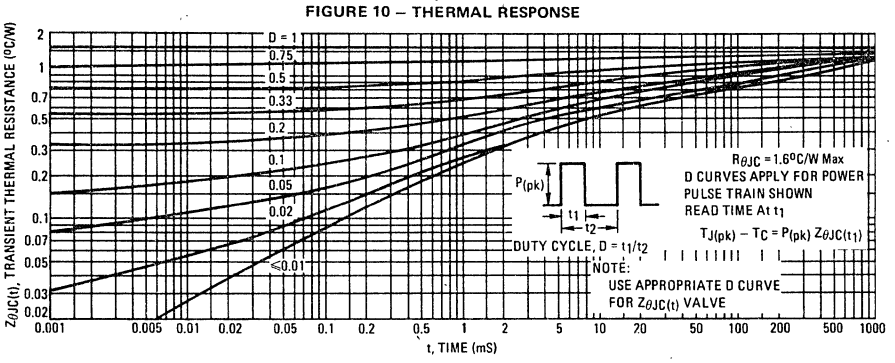


FIGURE 10 – THERMAL RESPONSE



4

FIGURE 11 – COLLECTOR SATURATION REGION

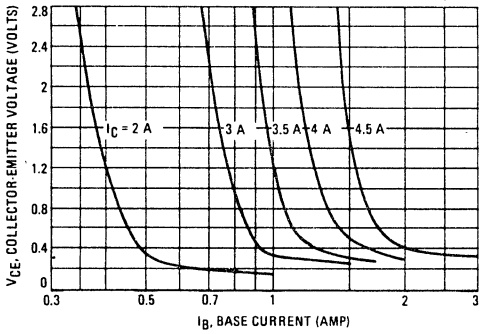


FIGURE 12 – DC CURRENT GAIN

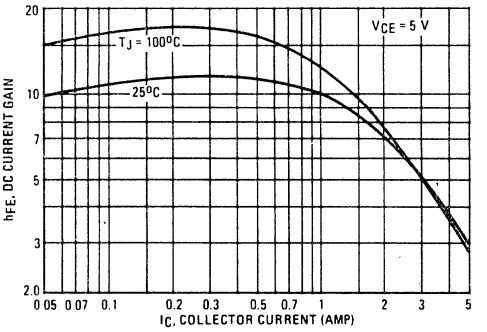


FIGURE 13 – "ON" VOLTAGES

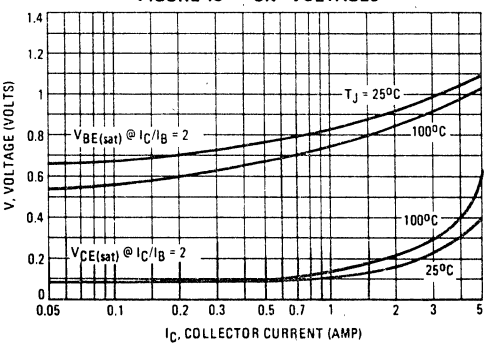
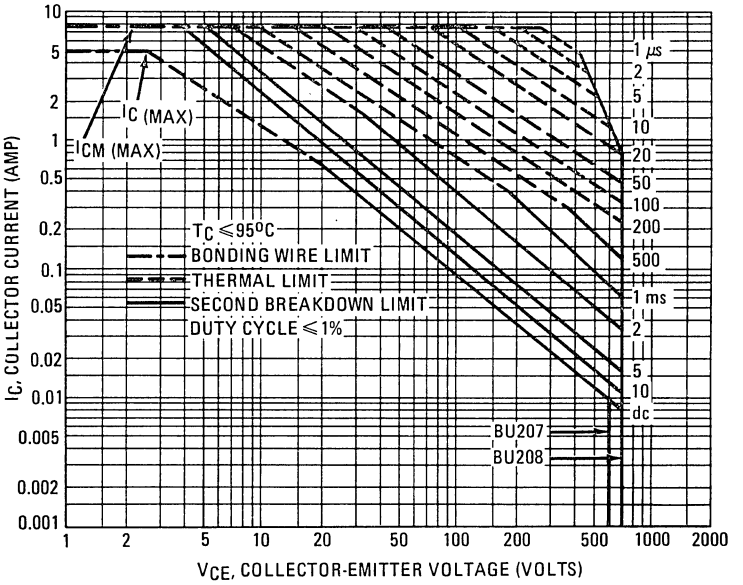


FIGURE 14 – MAXIMUM FORWARD BIAS
SAFE OPERATING AREA



4

D40C1
D40C2
D40C4
D40C5

4

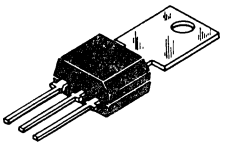
NPN SILICON DARLINGTON AMPLIFIER TRANSISTORS

. . . designed for amplifier and driver applications where high gain is an essential requirement, low power lamp and relay drivers and power drivers for high-current applications such as voltage regulators.

- High DC Current Gain —
  h_{FE} = 40,000 (Min) @ I_C = 200 mAdc — D40C2, 5
- Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 40 Vdc (Min) @ I_C = 10 mAdc — D40C4, 5
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 500 mAdc
- Duowatt Package —
  2 Watts Free Air Dissipation @ T_A = 25°C

DUOWATT

NPN SILICON DARLINGTON AMPLIFIER TRANSISTORS



Tab forming and TO-5 lead forming available on special request.

MAXIMUM RATINGS

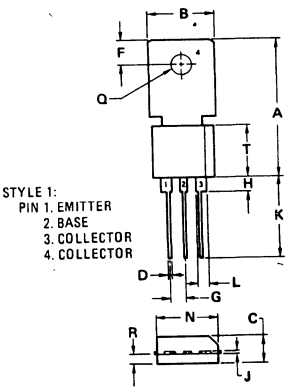
Rating	Symbol	D40C1,2	D40C4,5	Unit
Collector-Emitter Voltage	V_{CEO}	30	40	Vdc
Collector-Emitter Voltage	V_{CES}	30	40	Vdc
Emitter-Base Voltage	V_{EBO}	13		Vdc
Collector Current — Continuous Peak (1)	I_C	0.5 1.0		Adc
Base Current — Continuous	I_B	100		mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C (2)	P_D	1.67 13.3		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	6.25 50		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C
Solder Temperature, 1/16" from Case for 10 Seconds	—	260		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	20	°C/W

(1) Pulse Width ≤ 25 ms, Duty Cycle ≤ 50%.

(2) The actual power dissipation capability of Duowatt transistors are 2 W @ T_A = 25°C.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

TO-202AC
CASE 306-04

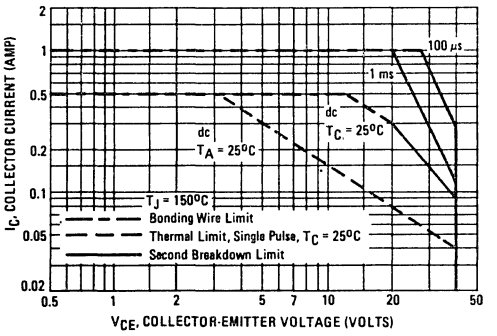
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, V_{BE} = 0)	D40C1, 2 D40C4, 5	BV_{CEO}	 30 40	 – –	Vdc
Collector Cutoff Current (V_{CB} = Rated V_{CES}, I_E = 0, T_J = 150°C)		I_{CBO}	–	20	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{BE} = 0)		I_{CES}	–	0.5	μAdc
Emitter Cutoff Current (V_{EB} = 13 Vdc, I_C = 0)		I_{EBO}	–	100	nAdc
ON CHARACTERISTICS (1)					
Current Gain (I_C = 200 mAdc, V_{CE} = 5.0 Vdc)	D40C1, 4 D40C2, 5	h_{FE}	 10,000 40,000	 60,000 –	–
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 0.5 mAdc)		$V_{CE(sat)}$	–	1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 0.5 mAdc)		$V_{BE(sat)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Collector Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{cb}	–	10	pF
High Frequency Current Gain (I_C = 20 mA, V_{CE} = 5 Vdc, f = 100 MHz)		h_{fe}	1.0	–	–
Input Impedance (I_C = 20 mA, V_{CE} = 5 Vdc, f = 1 kHz)		h_{ie}	50	–	Ohms

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 – ACTIVE-REGION SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS (continued)

FIGURE 2 – DC CURRENT GAIN

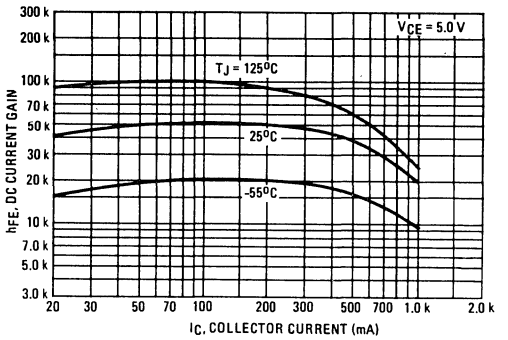


FIGURE 3 – "ON" VOLTAGES

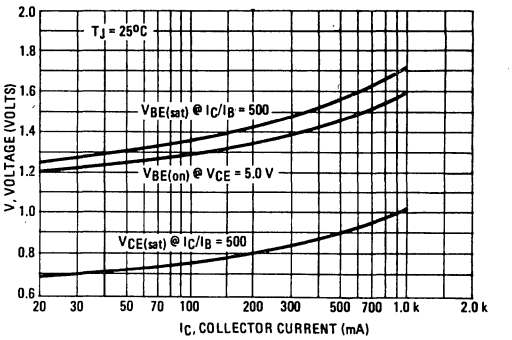


FIGURE 4 – COLLECTOR SATURATION REGION

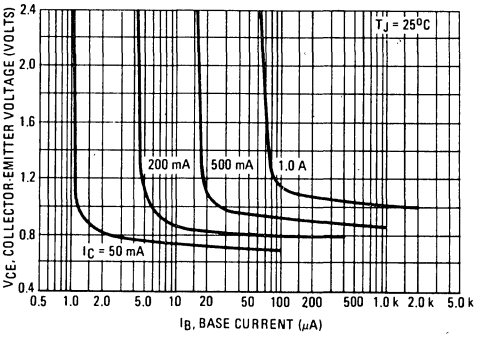


FIGURE 5 – TEMPERATURE COEFFICIENT

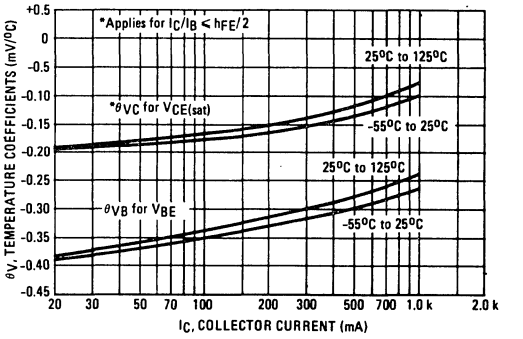
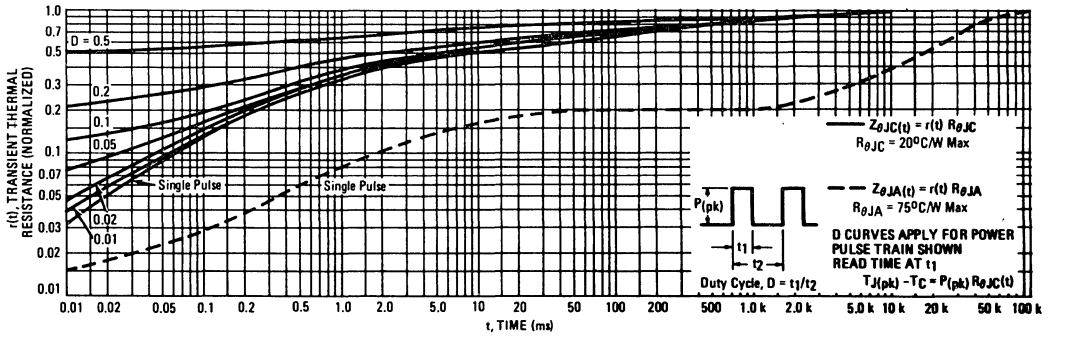


FIGURE 6 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – CAPACITANCE

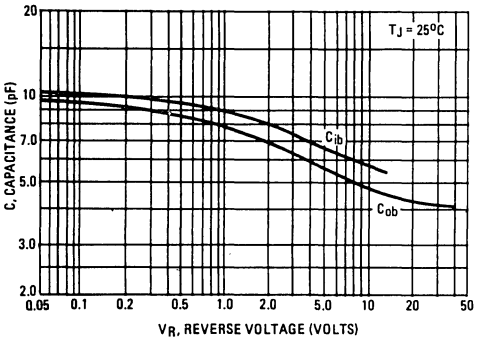
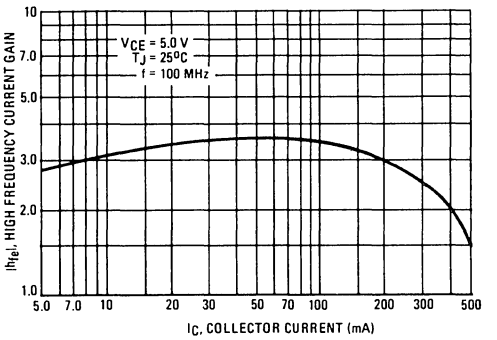


FIGURE 8 – HIGH-FREQUENCY CURRENT GAIN



NPN

D40D

PNP

D41D

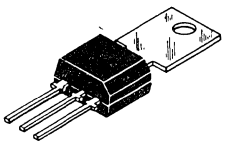
COMPLEMENTARY SILICON ANNULAR◆ AMPLIFIER TRANSISTORS

. . . designed for general-purpose, medium-voltage, medium power amplifier and driver applications; series, shunt and switching regulators, and low and high frequency inverters and converters.

- Duowatt Package — 2 Watts Free Air Dissipation @ $T_A = 25^oC$

DUOWATT

COMPLEMENTARY SILICON AMPLIFIER TRANSISTORS



Tab forming and TO-5 lead forming available on special request.

4

MAXIMUM RATINGS

Rating	Symbol	D40/41D 1,2	D40/41D 4,5	D40/41D 7,8	D40/41D 10,11,13,14	Unit
Collector-Emitter Voltage	V_{CEO}	30	45	60	75	Vdc
Collector-Emitter Voltage	V_{CES}	45	60	75	90	Vdc
Emitter-Base Voltage	V_{EBO}	5.0				Vdc
Collector Current — Continuous	I_C	1.0				Adc
Peak (1)		2.0				
Base Current	I_B	100				mAdc
Total Power Dissipation @ $T_A = 25^oC$	P_D	1.67				Watts
Derate above 25^oC (2)		13.3				$mW/^oC$
Total Power Dissipation @ $T_C = 25^oC$	P_D	6.25				Watts
Derate above 25^oC		50				$mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150				^oC
Solder Temperature, 1/16" from Case for 10 Seconds	—	260				^oC

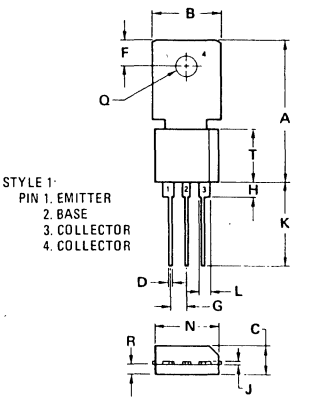
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	$^oC/W$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	20	$^oC/W$

(1) Pulse Test: Pulse Width ≤ 300 μs.

(2) The actual power dissipation capability of Duowatt transistors are 2 W @ $T_A = 25^oC$.

◆Annular Semiconductors Patented by Motorola Inc.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
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C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

TO-202AC
CASE 306-04

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	D40D1,2/D41D1,2	BV_{CEO}	30	–	Vdc
	D40D/D41D–4,5		45	–	
	D40D/D41D–7,8		60	–	
	D40D/D41D–10,11,13,14		75	–	
Collector Cutoff Current (V_{CE} = Rated V_{CES})		I_{CES}	–	100	nAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc)		I_{EBO}	–	100	nAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 2.0 Vdc)	D40D/D41D–1,4,7,10,13	h_{FE}	50	150	–
	D40D/D41D–2,5,8,11,14		120	360	
(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	D40D1,4,5,7,8,10,11		10	–	
	D41D1,4,5,7,8,10,11		10	–	
	D40D/D41D–2		20	–	
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)	D40D/D41D–1,2,4,5	$V_{CE(sat)}$	–	0.5	Vdc
	D40D,7,8,10,11,13,14		–	1.0	
	D41D7,8,10,11,13,14		–	1.0	
Base-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)		$V_{BE(sat)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (I_C = 20 mA, V_{CE}= 10 Vdc, f = 20 MHz)		f_T	75	375	MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1 MHz)	D40D series	C_{cb}	–	12	pF
	D41D series		–	18	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 – CURRENT-GAIN–BANDWIDTH PRODUCT

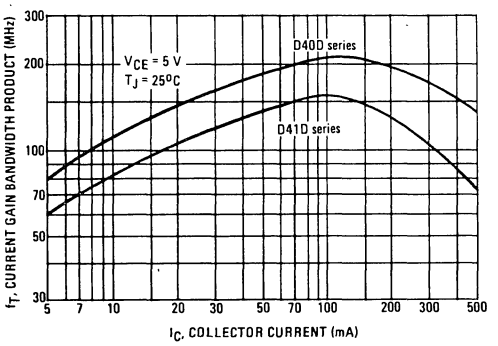
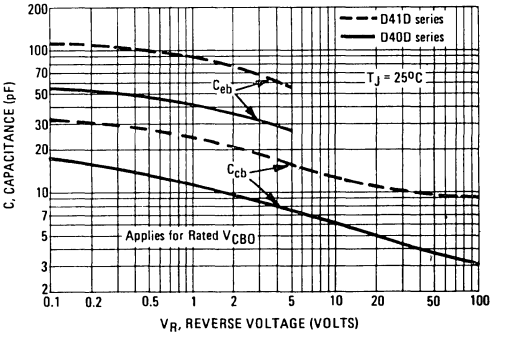
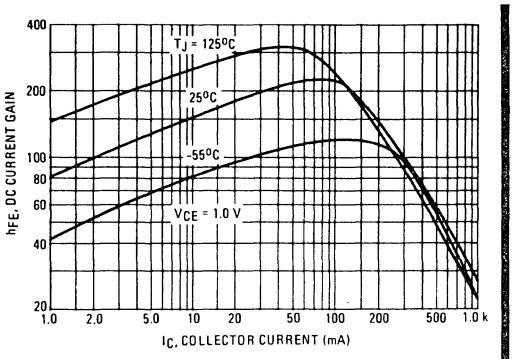


FIGURE 2 – CAPACITANCES



TYPICAL CHARACTERISTICS (continued)

D40D series — FIGURE 3 – DC CURRENT GAIN — D41D series



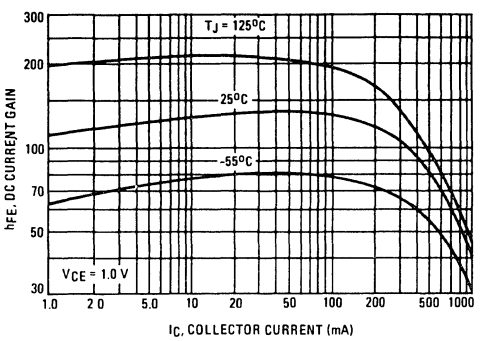
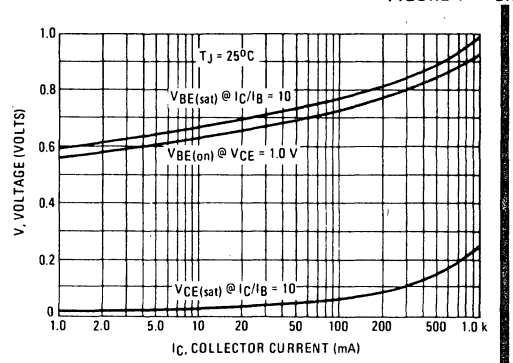


FIGURE 4 – "ON" VOLTAGE



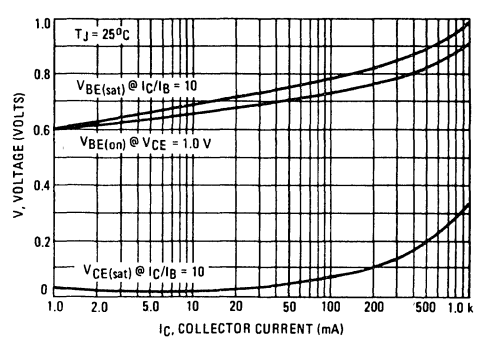
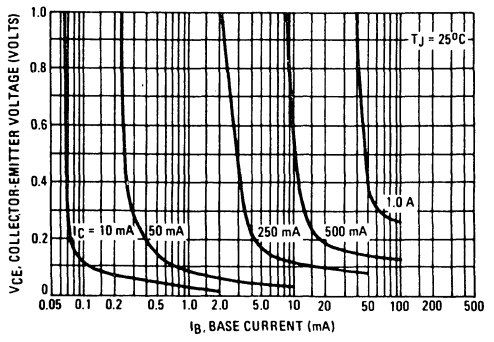
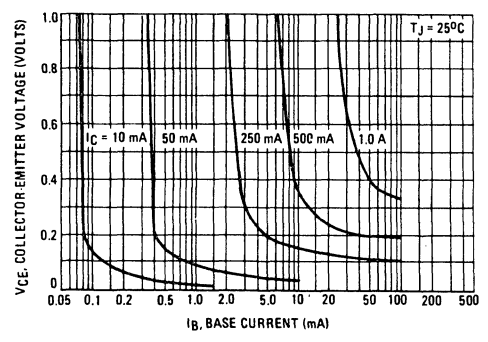


FIGURE 5 – COLLECTOR SATURATION REGION





TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – THERMAL RESPONSE

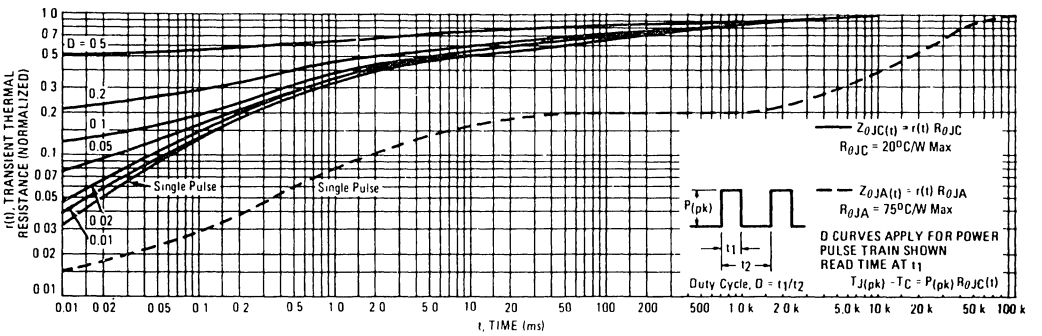
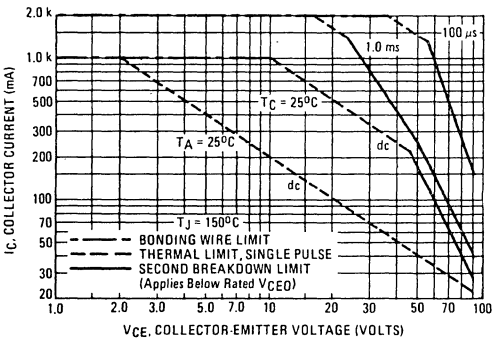
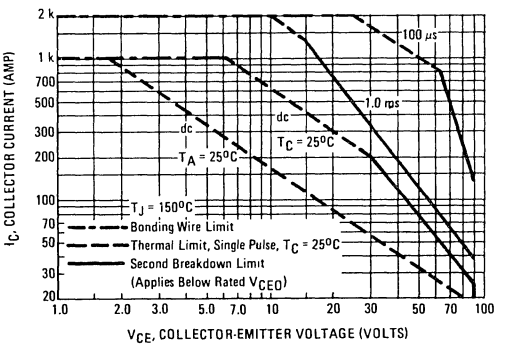


FIGURE 7 – ACTIVE-REGION SAFE-OPERATING AREA

D40D series



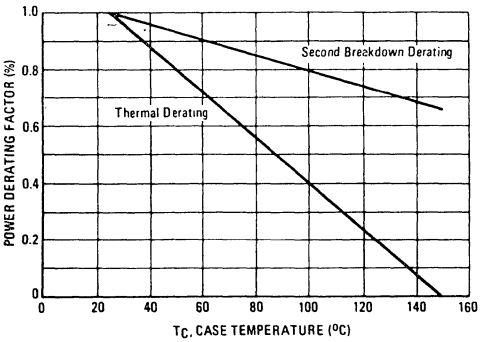
D41D series



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 8 – POWER DERATING



NPN PNP

D40E1 D41E1
D40E5 D41E5
D40E7 D41E7

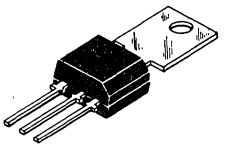
COMPLEMENTARY SILICON ANNULAR♦ AMPLIFIER TRANSISTORS

. . . designed for general-purpose, medium-voltage, medium power amplifier and driver applications; series, shunt and switching regulators, and low and high frequency inverters and converters.

- Duowatt Package — 2 Watts Free Air Dissipation @ $T_A = 25^oC$

DUOWATT

COMPLEMENTARY SILICON AMPLIFIER TRANSISTORS



Tab forming and TO-5 lead forming available on special request.

MAXIMUM RATINGS

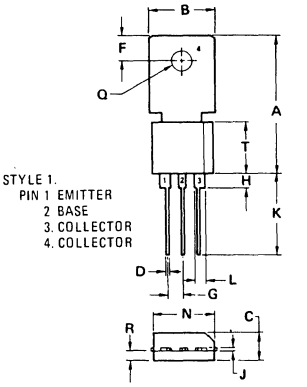
Rating	Symbol	D40/41E1	D40/41E5	D40/41E7	Unit
Collector-Emitter Voltage	V_{CEO}	30	60	80	Vdc
Collector-Emitter Voltage	V_{CES}	40	70	90	Vdc
Emitter-Base Voltage	V_{EBO}	5.0			Vdc
Collector Current — Continuous Peak (1)	I_C	2 3			Adc
Base Current	I_B	0.5			mAdc
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC (2)	P_D	1.67 13.3			Watts $mW/^oC$
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	8 64			Watts $mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150			^oC
Solder Temperature, 1/16" from Case for 10 Seconds	—	260			^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R\theta_{JA}$	75	$^oC/W$
Thermal Resistance, Junction to Case	$R\theta_{JC}$	15.6	$^oC/W$

NOTES 1. Pulse Test: Pulse Width ≤ 300 μs.

2. The actual power dissipation capability of Duowatt transistors are 2 W @ $T_A = 25^oC$.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

TO-202AC
CASE 306-04

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	D40E1/D41E1	BV_{CEO}	30	–	Vdc
	D40E5/D41E5		60	–	
	D40E7/D41E7		80	–	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	100	nAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES})		I_{CES}	–	100	nAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 2.0 Vdc)		h_{FE}	50	–	–
(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)			10	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 100 mAdc)		$V_{CE(sat)}$	–	1.0	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 100 mAdc)		$V_{BE(sat)}$	–	1.3	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain –Bandwidth Product (I_C = 20 mA, V_{CE} = 10 Vdc, f = 20 MHz)		f_T	75	375	MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1 MHz)	D40E series	C_{cb}	–	12	pF
	D41E series		–	18	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 – CURRENT GAIN-BANDWIDTH PRODUCT

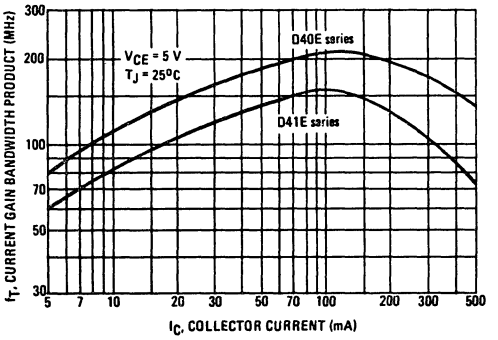
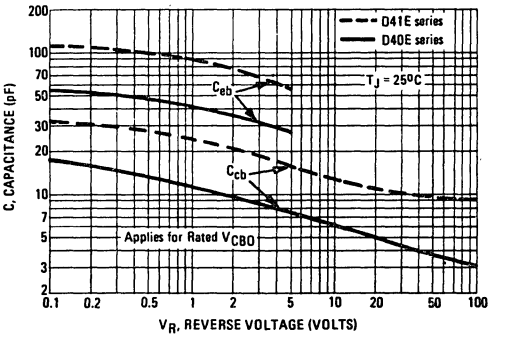


FIGURE 2 – CAPACITANCES



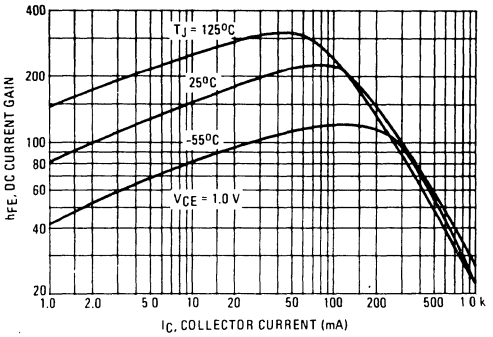
4

TYPICAL CHARACTERISTICS (continued)

D40E series

D41E series

FIGURE 3 – DC CURRENT GAIN



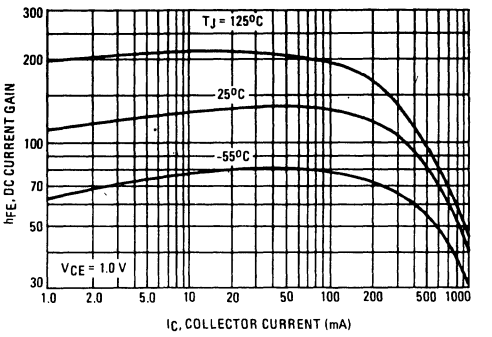
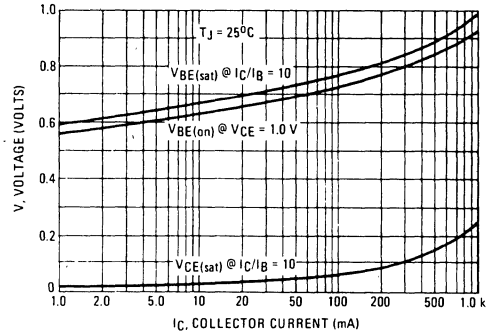


FIGURE 4 – "ON" VOLTAGE



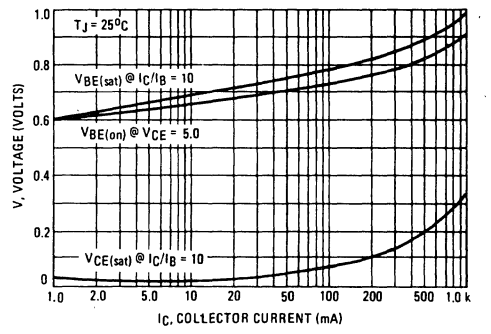
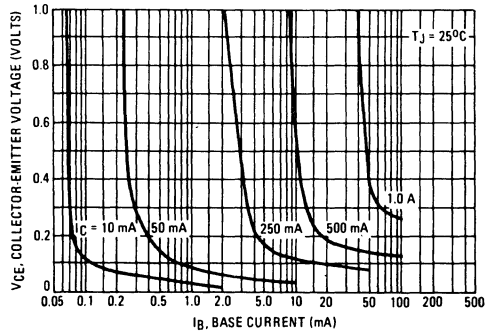
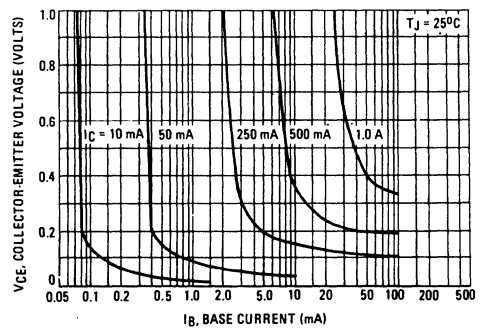


FIGURE 5 – COLLECTOR SATURATION REGION





TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – THERMAL RESPONSE

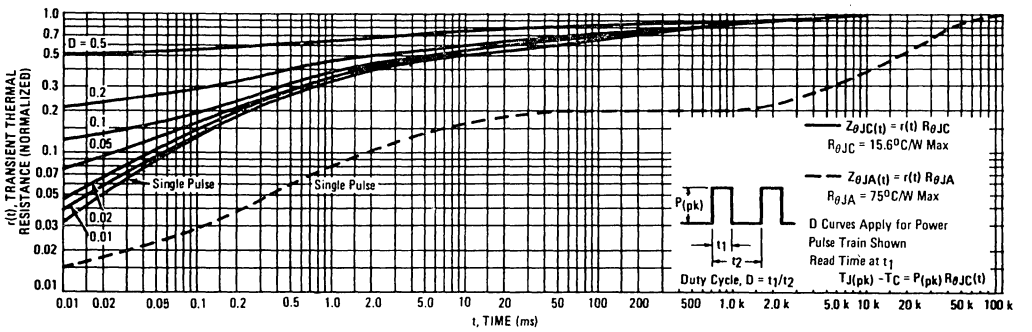
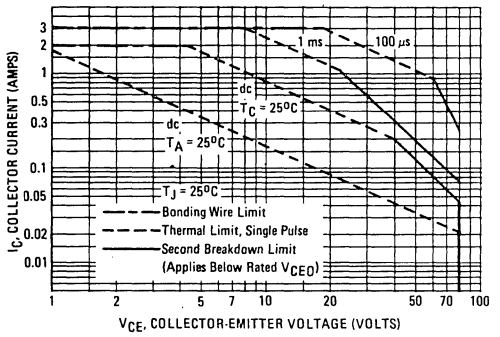


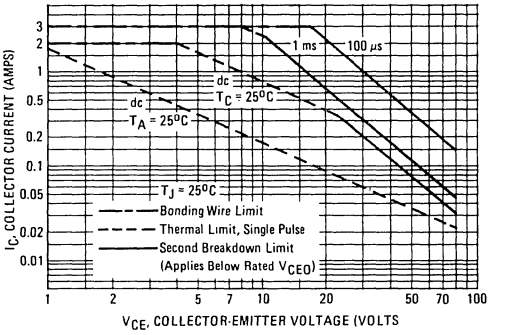
FIGURE 7 – ACTIVE-REGION SAFE-OPERATING AREA

D40E series



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

D41E series



The data of Figure 7 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

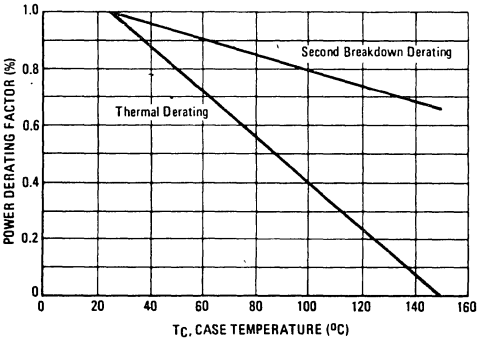


FIGURE 8 – POWER DERATING

NPN

D40K

PNP

D41K

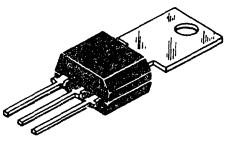
COMPLEMENTARY SILICON DARLINGTON AMPLIFIER TRANSISTORS

. . . designed for amplifier and driver applications where high gain is an essential requirement, low power lamp and relay drivers and power drivers for high-current applications such as voltage regulators.

- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 1.5 Adc for D40,41K1,2
- Duowatt Package –
  2 Watts Free Air Dissipation @ T_A = 25°C

DUOWATT

COMPLEMENTARY SILICON DARLINGTON AMPLIFIER TRANSISTORS



Tab forming and TO-5 lead forming available on special request.

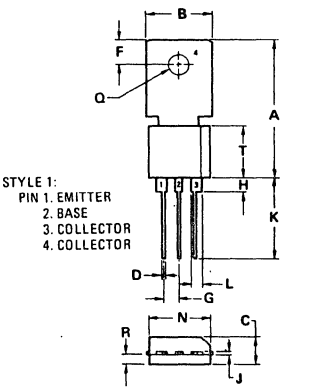
MAXIMUM RATINGS

Rating	Symbol	D40/41K 1,3	D40/41K 2,4	Unit
Collector-Emitter Voltage	V_{CEO}	30	50	Vdc
Collector-Emitter Voltage	V_{CES}	30	50	Vdc
Emitter-Base Voltage	V_{EBO}	13		Vdc
Collector Current – Continuous Peak (1)	I_C	2.0 3.0		Adc
Base Current – Continuous	I_B	100		mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C (2)	P_D	1.67 13.3		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C
Solder Temperature, 1/16" from Case for 10 Seconds	–	260		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

1. Pulse Width ≤ 25 ms, Duty Cycle ≤ 50%.
2. The actual power dissipation capability of Duowatt transistors are 2 W @ T_A = 25°C.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

TO-202AC
CASE 306-04

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc)	D40,41K1,3 D40,41K2,4	BV_{CEO}	30 50	– –	Vdc
Collector Cutoff Current (V_{CB} = Rated V_{CES}, I_E = 0, T_J = 150°C)		I_{CBO}	–	20	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{BE} = 0)		I_{CES}	–	0.5	μAdc
Emitter Cutoff Current (V_{EB} = 13 Vdc, I_C = 0)		I_{EBO}	–	100	nAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 200 mAdc, V_{CE} = 5.0 Vdc)	All Devices		10,000	–	
(I_C = 1.5 Adc, V_{CE} = 5.0 Vdc)	D40,41K1,2		1,000	–	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	D40,41K3,4		1,000	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 3.0 mAdc)	D40,41K1,2		–	1.5	
(I_C = 1.0 Adc, I_B = 2.0 mA)	D40,41K3,4		–	1.5	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 3.0 mAdc)	D40,41K1,2		–	2.5	
(I_C = 1.0 Adc, I_B = 2.0 mAdc)	D40,41K3,4		–	2.5	
DYNAMIC CHARACTERISTICS					
Collector Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	D40K series D41K series	C_{cb}	– –	10 25	pF
High Frequency Current Gain (I_C = 20 mA, V_{CE} = 5 Vdc, f = 100 MHz)		$\|h_{fe}\|$	1.0	–	–

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 – DC SAFE OPERATING AREA

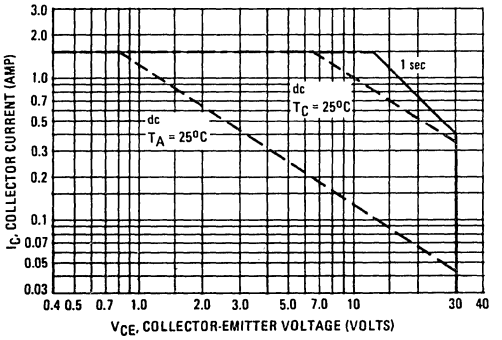
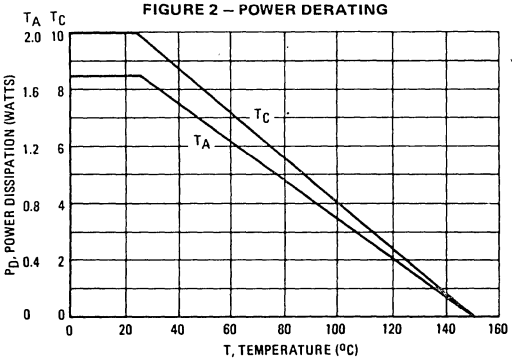


FIGURE 2 – POWER DERATING



TYPICAL CHARACTERISTICS (continued)

DC CURRENT GAIN

FIGURE 3 – (D40K series)

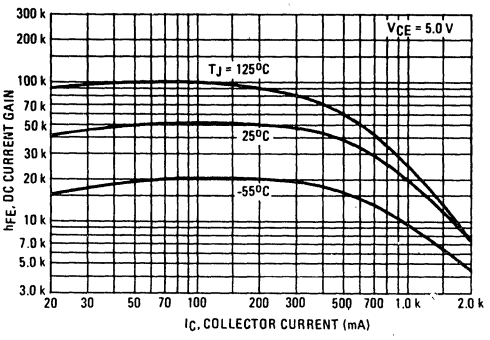
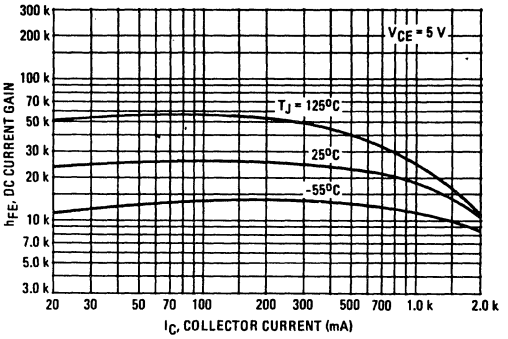


FIGURE 4 – (D41K series)



"ON" VOLTAGES

FIGURE 5 – (D40K series)

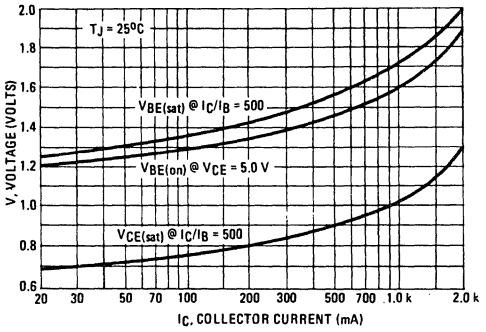


FIGURE 6 – (D41K series)

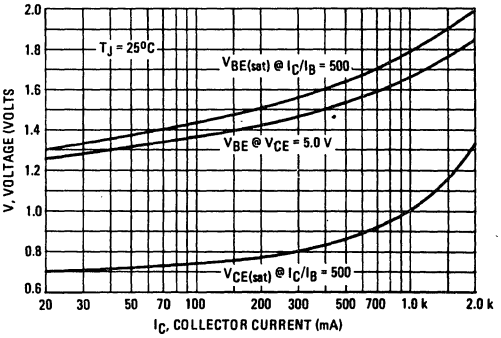
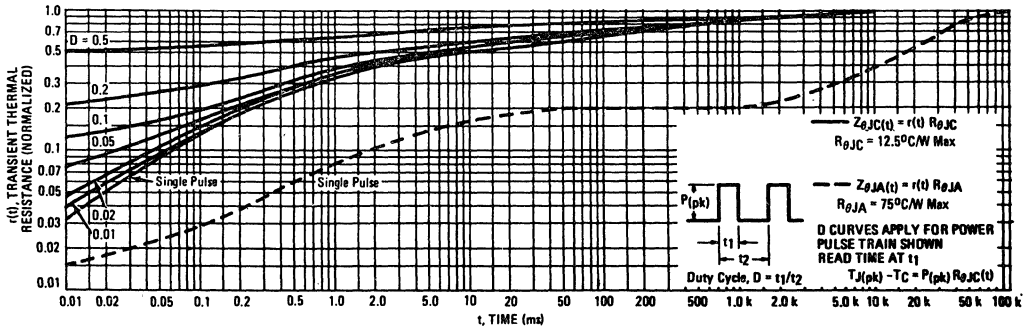


FIGURE 7 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS (continued)

CAPACITANCE

FIGURE 8 – (D40K series)

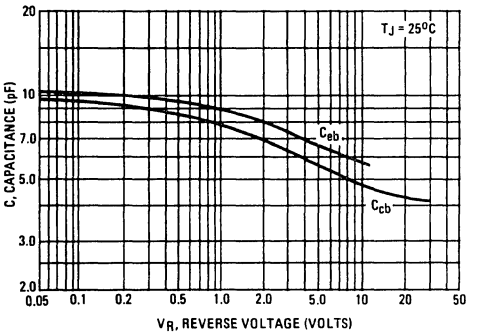
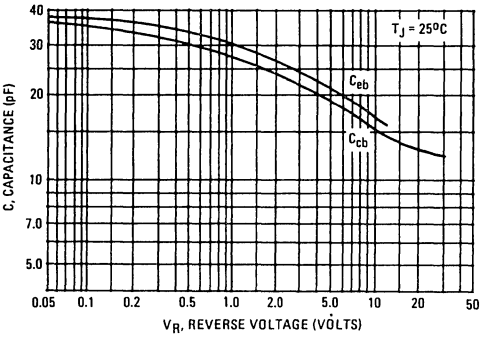


FIGURE 9 – (D41K series)



HIGH FREQUENCY CURRENT GAIN

FIGURE 10 – (D40K series)

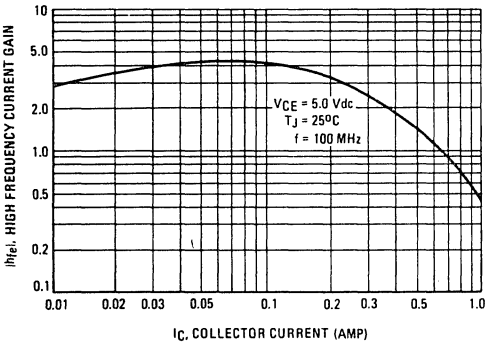
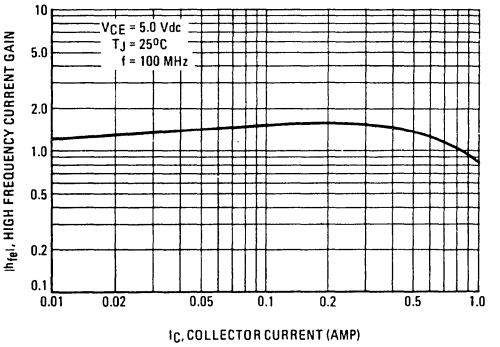


FIGURE 11 – (D41K series)



D40N1 D40N3
D40N2 D40N4

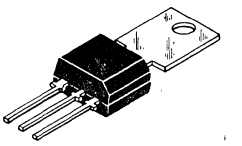
NPN SILICON ANNULAR HIGH VOLTAGE AMPLIFIER TRANSISTORS

. . . designed for high-voltage TV video and chroma output circuits, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage –
  BV_{CER} = 300 Vdc (Min) @ I_C = 1.0 mAdc – D40N3, 4
- Low Collector-Base Capacitance –
  C_{cb} = 3.0 pF (Max) @ V_{CB} = 20 Vdc
- Duowatt Package –
  2 Watts Free Air Dissipation @ T_A = 25°C

DUOWATT

NPN SILICON AMPLIFIER TRANSISTORS



Tab forming and TO-5 lead forming available on special request.

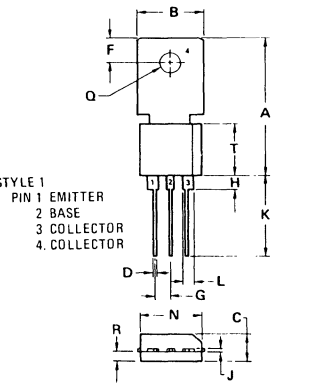
MAXIMUM RATINGS

Rating	Symbol	D40N1, 2	D40N3, 4	Unit
Collector-Emitter Voltage (1, 2)	V_{CER}	250	300	Vdc
Collector-Base Voltage	V_{CBO}	250	300	Vdc
Emitter-Base Voltage	V_{EBO}	5.0		Vdc
Collector Current – Continuous – Peak	I_C	0.1 0.7		Adc
Base Current	I_B	250		mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.67 (3) 13.3		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	6.25 50		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C
Solder Temperature, 1/16" from Case for 10 Seconds	–	260		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	20	°C/W

(1) I_C = 1.0 mAdc, R_{BE} = 10 kΩ.
(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(3) The actual power dissipation capability of Duowatt transistors are 2 W @ T_A = 25°C.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

TO-202AC
CASE 306-04

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

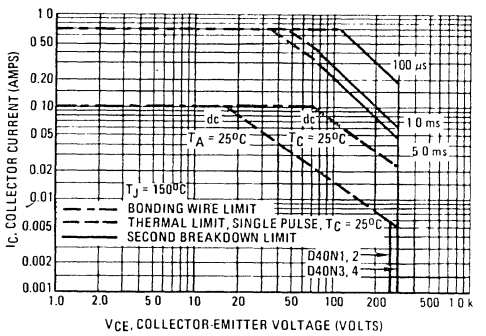
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1)		BV_{CER}			Vdc
(I_C = 1.0 mAdc, I_B = 0, R_{BE} = 10 kΩ)	D40N1, 2		250	–	
	D40N3, 4		300	–	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 250 Vdc, I_E = 0)	D40N1, 2		–	10	
(V_{CB} = 300 Vdc, I_E = 0)	D40N3, 4		–	10	
Emitter Cutoff Current		I_{EBO}	–	10	μAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 4.0 mAdc, V_{CE} = 10 Vdc)	D40N1, 3		20	–	
	D40N2, 4		30	–	
(I_C = 20 mAdc, V_{CE} = 10 Vdc)	D40N1, 3		30	90	
	D40N2, 4		60	180	
(I_C = 40 mAdc, V_{CE} = 10 Vdc)	D40N1, 3		20	–	
	D40N2, 4		30	–	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	50	–	MHz
(I_C = 20 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)					
Collector-Base Capacitance		C_{cb}	–	3.0	pF
(V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)					

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

4

TYPICAL CHARACTERISTICS

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS (continued)

FIGURE 2 – DC CURRENT GAIN

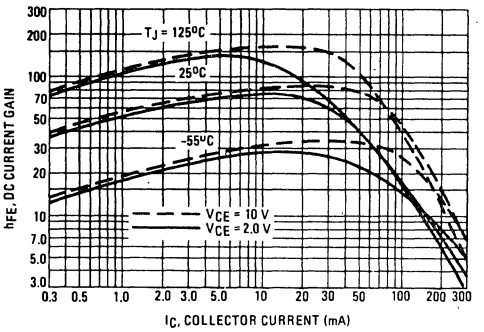


FIGURE 3 – "ON" VOLTAGES

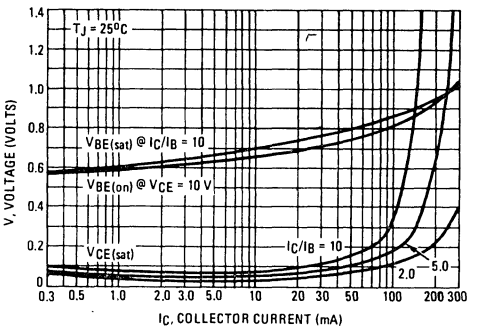


FIGURE 4 – COLLECTOR SATURATION REGION

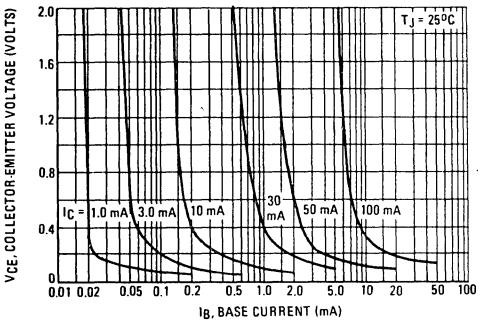


FIGURE 5 – TEMPERATURE COEFFICIENTS

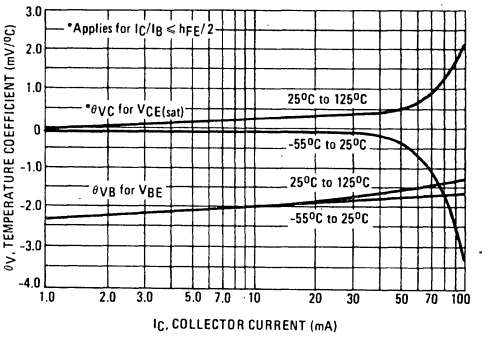
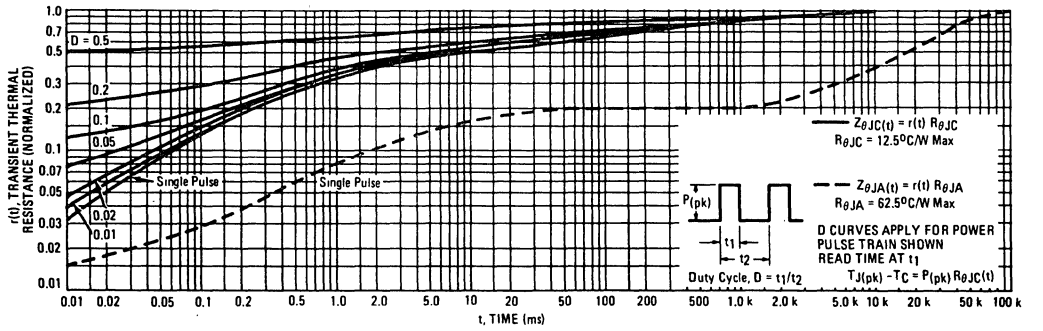


FIGURE 6 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – CAPACITANCE

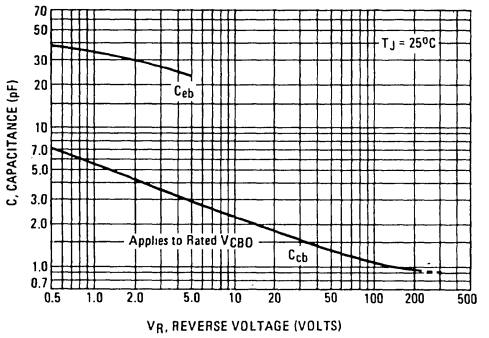
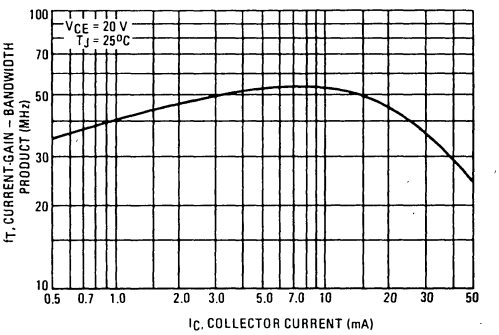


FIGURE 8 – CURRENT-GAIN – BANDWIDTH PRODUCT



4

APPLICATIONS INFORMATION

The D40N4 is primarily designed for use in the R, G, and B output stages of color television receivers and with a high BV_{CEO}, it can supply the video amplitude requirements of any known system. The low feedback capacitance provides good video bandwidth with modest drive current requirements. Typical drive is from an emitter-follower with a 4.7 k emitter-resistor operated from a 20-Volt supply. It will, therefore, be operable directly from a number of available chroma demodulators. The low output capacitance of this device adds little to the total load capacitance, allowing improved bandwidth for a given collector load resistor. Two typical applications for the D40N4 are shown in Figures 9 and 10.

Device dissipation will reach approximately 1.6 Watts under worst-case signal conditions and some heat-sinking is required at ambient temperatures above 50°C.

Used as a color difference output, where drive and bandwidth requirements are less severe, the D40N4 can be operated with 27 k ohm load resistors (worst-case dissipation would then be only 0.6 Watts). The device can, therefore, be operated as a color-difference output without any heat radiator in ambient temperatures to 150 – (0.6)(75) = 105°C.

In addition, the safe operating area of the D40N4 will fill the requirements of the luminance output function with a total equivalent load of 5.0 kilohms. Worse-case dissipation can reach 3 Watts, this requires a total $R_{\theta JA}$ of (150–65)/3 = 28.4°C/W. To achieve this a 2" X 3" aluminum plate will be required.

FIGURE 9 – RGB OUTPUT WITH RGB INPUT

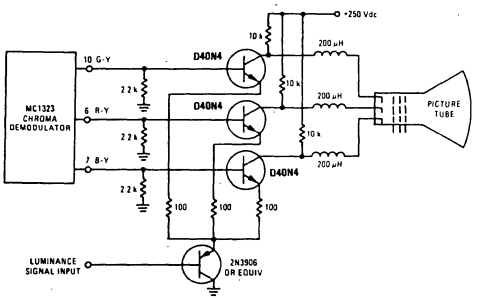
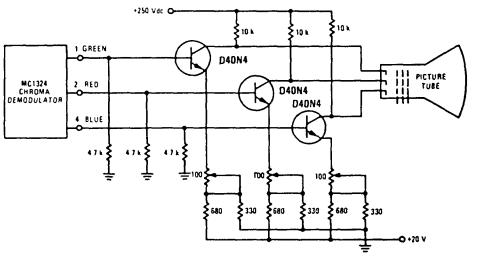


FIGURE 10 – RGB OUTPUT, MATRIXING COLOR DIFFERENCE AND LUMINANCE INPUTS



D40P1
D40P3
D40P5

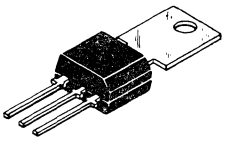
NPN SILICON ANNULAR HIGH VOLTAGE AMPLIFIER TRANSISTORS

. . . designed for horizontal drive applications, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage — BV_{CEO} = 225 Vdc (Min) @ I_C = 1.0 mAdc — D40P5
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 100 mAdc
- Duowatt Package — 2 Watts Free Air Dissipation @ $T_A = 25^oC$

DUOWATT

NPN SILICON AMPLIFIER TRANSISTORS



Tab forming and TO-5 lead forming available on special request.

MAXIMUM RATINGS

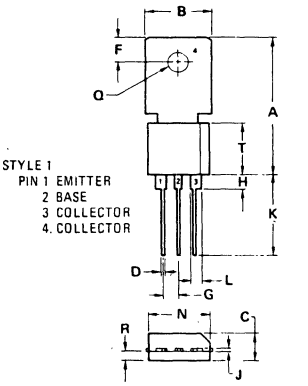
Rating	Symbol	D40P1	D40P3	D40P5	Unit
Collector-Emitter Voltage	V_{CEO}	120	180	225	Vdc
Collector-Base Voltage	V_{CBO}	200	250	300	Vdc
Emitter-Base Voltage	V_{EBO}	7.0			Vdc
Collector Current — Continuous Peak (1)	I_C	0.5 1.0			Adc
Base Current	I_B	100			mAdc
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	1.67 (2) 13.3			Watts mW/^oC
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	6.25 50			Watts mW/^oC
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150			^oC
Solder Temperature, 1/16" from Case for 10 Seconds	—	260			^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	$^oC/W$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	20	$^oC/W$

(1) Pulse Test: Pulse Width ≤ 1.0 ms, Duty Cycle ≤ 50%.

(2) The actual power dissipation capability of Duowatt transistors are 2 W @ $T_A = 25^oC$.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

TO-202AC
CASE 306-04

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Character		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1)		BV_{CEO}			Vdc
(I_C = 1.0 mAdc, I_B = 0)	D40P1		120	–	
	D40P3		180	–	
	D40P5		225	–	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 200 Vdc, I_E = 0)	D40P1		–	10	
(V_{CB} = 250 Vdc, I_E = 0)	D40P3		–	10	
(V_{CB} = 300 Vdc, I_E = 0)	D40P5		–	10	
Emitter Cutoff Current		I_{EBO}	–	10	μAdc
(V_{EB} = 7.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 80 mAdc, V_{CE} = 10 Vdc)			40	–	
(I_C = 2.0 mAdc, V_{CE} = 10 Vdc)			20	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	–	1.0	Vdc
(I_C = 100 mAdc, I_B = 10 mAdc)					
Base-Emitter Saturation Voltage		$V_{BE(sat)}$	–	1.5	Vdc
(I_C = 100 mAdc, I_B = 10 mA)					
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	50	–	MHz
(I_C = 80 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)					
Collector-Base Capacitance		C_{cb}	–	6.0	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)					
SWITCHING CHARACTERISTICS					
Storage Time		t_s	–	2.5	μs
($I_{C(on)}$ = 80 mA, $I_{B(on)}$ = 8.0 mA, $I_{B(off)}$ = 8.0 mA)					

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 – CURRENT-GAIN – BANDWIDTH PRODUCT

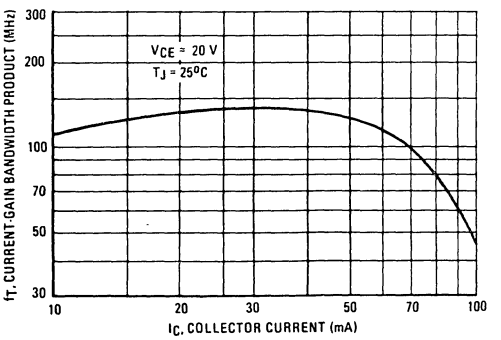
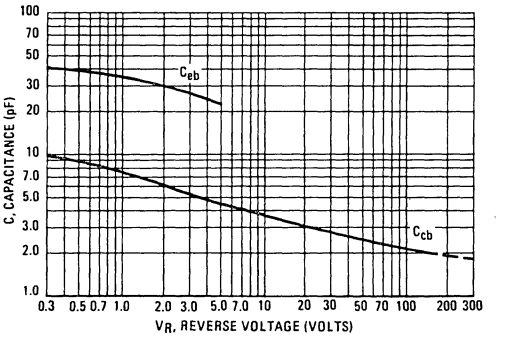


FIGURE 2 – CAPACITANCE



4

TYPICAL CHARACTERISTICS (Continued)

FIGURE 3 – DC CURRENT GAIN

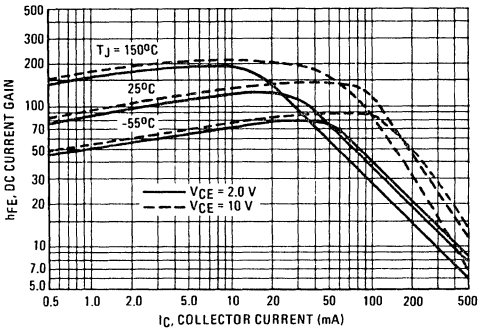


FIGURE 4 – "ON" VOLTAGE

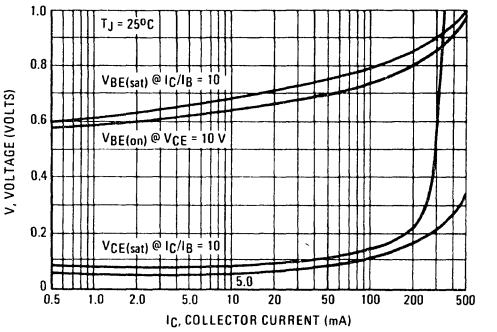


FIGURE 5 – COLLECTOR SATURATION REGION

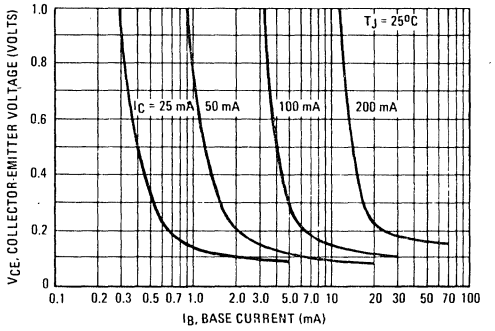


FIGURE 6 – TEMPERATURE COEFFICIENTS

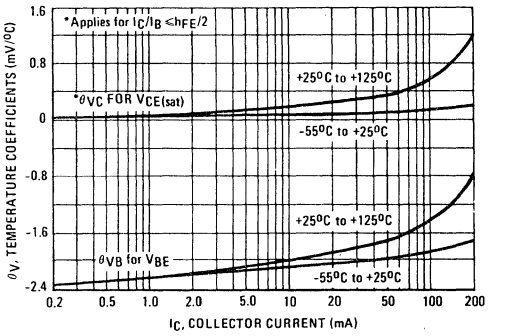


FIGURE 7 – COLLECTOR CHARACTERISTICS

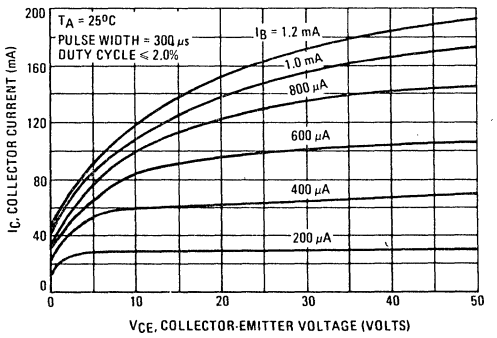
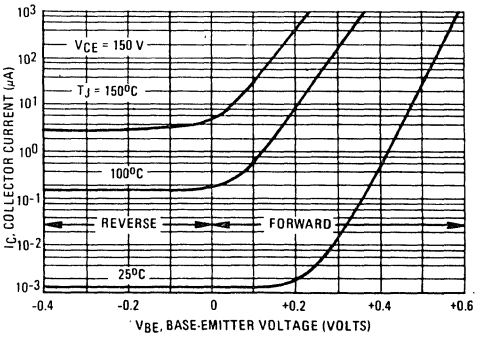


FIGURE 8 – COLLECTOR CUTOFF REGION



TYPICAL CHARACTERISTICS (Continued)

FIGURE 9 – THERMAL RESPONSE

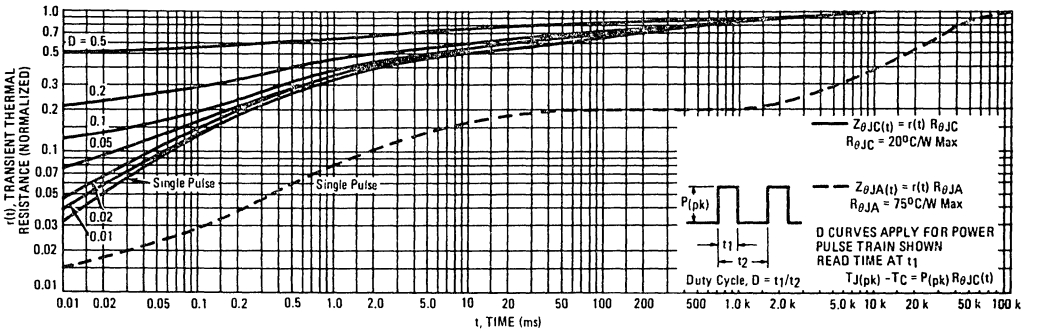


FIGURE 10 – ACTIVE REGION SAFE-OPERATING AREA

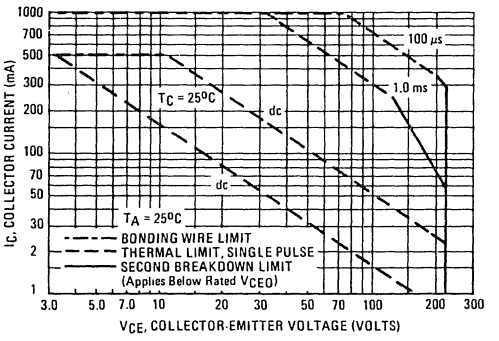
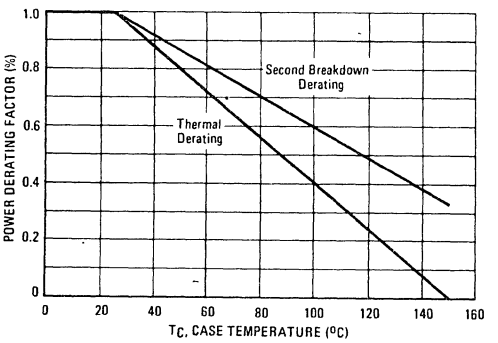


FIGURE 11 – POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25^{o}C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^{o}C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MDS20
MDS21

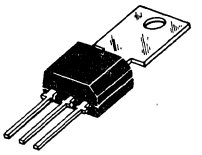
NPN SILICON ANNULAR HIGH VOLTAGE AMPLIFIER TRANSISTORS

. . . designed for high-voltage TV video and chroma output circuits, high-voltage linear amplifiers, high-voltage drivers and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage —
  BV_{CEO} = 300 Vdc (Min) @ I_C = 1.0 mAdc — MDS21
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 30 mAdc
- Low Collector-Base Capacitance —
  C_{cb} = 3.0 pF (Max) @ V_{CB} = 20 Vdc
- Duowatt Package —
  2 Watts Free Air Dissipation @ T_A = 25°C

DUOWATT

NPN SILICON AMPLIFIER TRANSISTORS



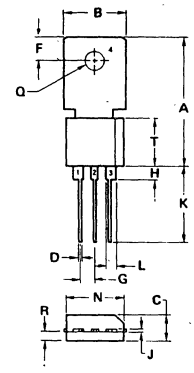
4

MAXIMUM RATINGS

Rating	Symbol	MDS20	MDS21	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	Vdc
Collector-Base Voltage	V_{CBO}	250	300	Vdc
Emitter-Base Voltage	V_{EBO}	8.0		Vdc
Collector Current — Continuous	I_C	0.5		Adc
Base Current	I_B	0.25		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 16		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		°C
Solder Temperature, 1/16" from Case for 10 Seconds	—	260		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04
TO-202AC

DS 3364

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

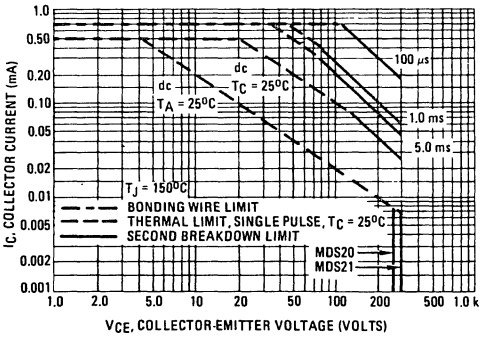
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1)		BV_{CEO}			Vdc
(I_C = 1.0 mAdc, I_B = 0)	MDS20		250	–	
	MDS21		300	–	
Collector-Base Breakdown Voltage	MDS20	BV_{CBO}	250	–	Vdc
(I_C = 100 μAdc, I_E = 0)	MDS21		300	–	
Emitter-Base Breakdown Voltage		BV_{EBO}	8.0	–	Vdc
(I_E = 100 μAdc, I_C = 0)					
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 150 Vdc, I_B = 0)	MDS20		–	0.5	
(V_{CE} = 200 Vdc, I_B = 0)	MDS21		–	0.5	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 200 Vdc, I_E = 0)	MDS20		–	0.1	
(V_{CB} = 250 Vdc, I_E = 0)	MDS21		–	0.1	
Emitter Cutoff Current		I_{EBO}	–	0.1	μAdc
(V_{BE} = 6.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}	40	250	–
(I_C = 30 mAdc, V_{CE} = 10 Vdc)					
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	–	0.6	Vdc
(I_C = 30 mAdc, I_B = 3.0 mAdc)					
Base-Emitter On Voltage		$V_{BE(on)}$	–	0.85	Vdc
(I_C = 30 mAdc, V_{CE} = 10 Vdc)					
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Prdouct		f_T	60	–	MHz
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)					
Collector-Base Capacitance		C_{cb}	–	3.0	pF
(V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)					

Note 1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

4

TYPICAL CHARACTERISTICS

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS (continued)

FIGURE 2 – DC CURRENT GAIN

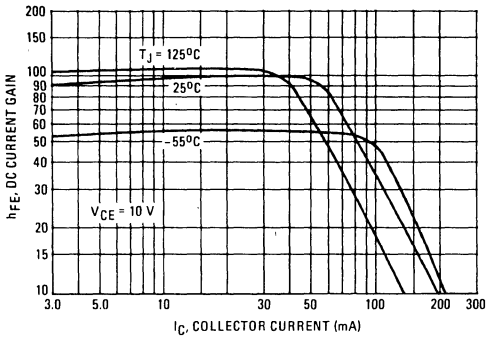


FIGURE 3 – "ON" VOLTAGES

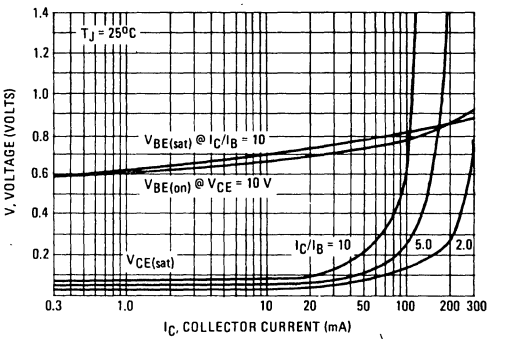


FIGURE 4 – COLLECTOR SATURATION REGION

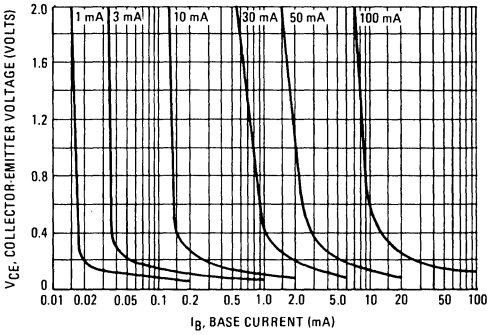


FIGURE 5 – TEMPERATURE COEFFICIENTS

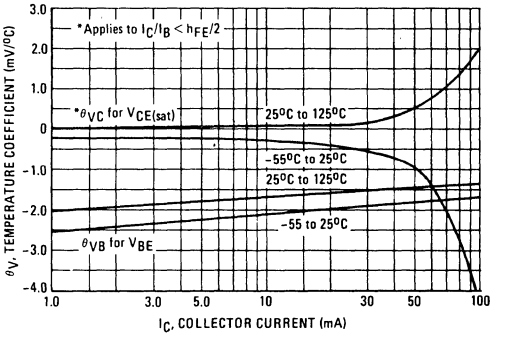
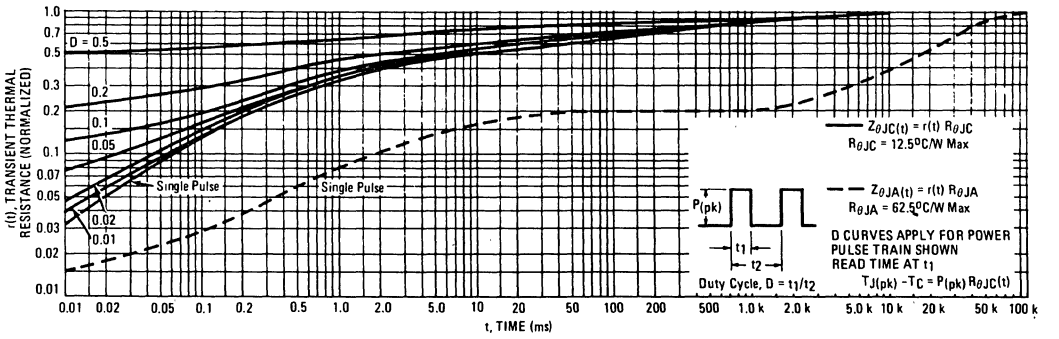


FIGURE 6 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – CAPACITANCE

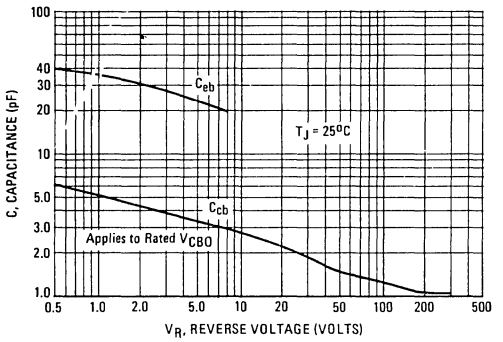
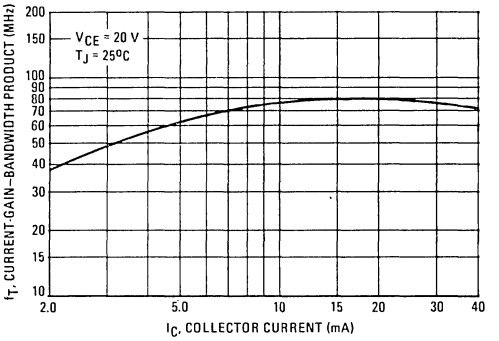


FIGURE 8 – CURRENT-GAIN–BANDWIDTH PRODUCT



4

APPLICATIONS INFORMATION

The MDS21 is primarily designed for use in the R, G, and B output stages of color television receivers, and with a high BV_{CEO} it can supply the video amplitude requirements of any known system. The low feedback capacitance provides good video bandwidth with modest drive current requirements. Typical drive is from an emitter-follower with a 4.7 k emitter-resistor operated from a 20-Volt supply. It will, therefore, be operable directly from a number of available chroma demodulators. The low output capacitance of this device adds little to the total load capacitance, allowing improved bandwidth for a given collector load resistor. Two typical applications for the MDS21 are shown in Figures 9 and 10.

Device dissipation will reach approximately 1.6 Watts under worst-case signal conditions and some heat sinking is required at ambient temperature above 50°C.

Used as a color difference output, where drive and bandwidth requirements are less severe, the MDS21 can be operated with 27 k ohm load resistors (worst-case dissipation would then be only 0.6 Watts). The device can, therefore, be operated as a color-difference output without any heat radiator in ambient temperatures to 150 – (0.6)(62.5) = 112.5°C.

In addition, the safe operating area of the MDS21 will fill the requirements of the luminance output function with a total equivalent load of 5.0 kilohms. Worst-case dissipation can reach 3 Watts; this requires a total $R_{\theta JA}$ of (150 – 65)/3 = 28.4°C/W. To achieve this a 2" x 3" aluminum plate will be required.

FIGURE 9 – MDS21 AS RGB OUTPUT WITH RGB INPUT

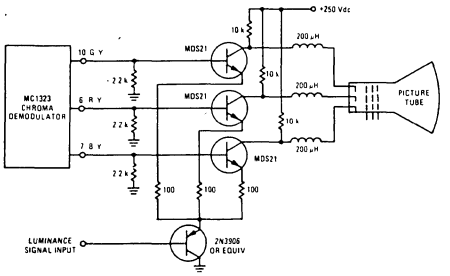
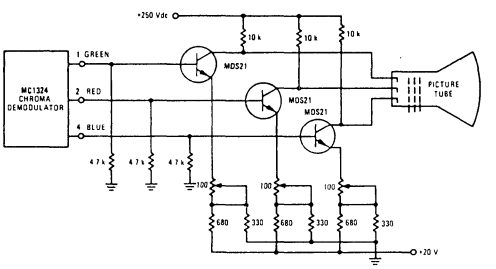


FIGURE 10 – MDS21 AS RGB OUTPUT, MATRIXING COLOR DIFFERENCE AND LUMINANCE INPUTS



NPN PNP

MDS26 MDS76
MDS27 MDS77

Advance Information

COMPLEMENTARY PLASTIC SILICON POWER TRANSISTORS

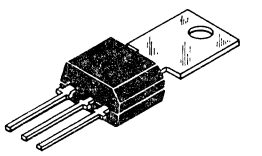
. . . designed for low power audio amplifier and low current, high speed switching applications.

- Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 40 Vdc — MDS26, MDS76
  = 60 Vdc — MDS27, MDS77
- DC Current Gain —
  h_{FE} = 40 (Min) @ I_C = 0.2 Adc
  = 30 (Min) @ I_C = 1.0 Adc
- Current-Gain — Bandwidth Product —
  f_T = 50 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakages —
  I_{CBO} = 100 nA (Max) @ Rated V_{CB}

DUOWATT
3.0 AMPERE

COMPLEMENTARY SILICON POWER TRANSISTORS

40, 60 VOLTS
10 WATTS



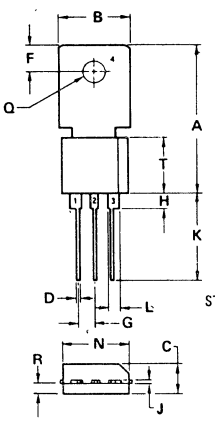
Tab forming and TO-5 lead forming available on special request.

MAXIMUM RATINGS

Rating	Symbol	MDS26 MDS76	MDS27 MDS77	Unit
Collector-Base Voltage	V_{CB}	60	80	Vdc
Collector-Emitter Voltage	V_{CEO}	40	60	Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current — Continuous Peak	I_C	3.0 5.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016		Watts W/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	62.5	°C/W



STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04
TO-202 AC

This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	MDS26,MDS76 MDS27,MDS77	$V_{CEO(sus)}$	 40 60	 – –	Vdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0, T_C = 125°C) (V_{CB} = 80 Vdc, I_E = 0, T_C = 125°C)	 MDS26,MDS76 MDS27,MDS77 MDS26,MDS76 MDS27,MDS77	I_{CBO}	 – – – –	 0.1 0.1 0.1 0.1	μAdc mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 200 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		h_{FE}	 40 30	 200 –	–
Collector-Emitter Saturation Voltage (I_C = 200 mAdc, I_B = 20 mAdc) (I_C = 1.0 Adc, I_B = 100 mAdc) (I_C = 3.0 Adc, I_B = 600 mAdc)		$V_{CE(sat)}$	 – – –	 0.3 0.6 1.7	Vdc
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	 –	 1.8	Vdc
Base-Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	 –	 1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (2) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	 50	 –	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MDS26, MDS27 MDS76, MDS77	C_{ob}	 – –	 50 70	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

(2) $f_T = |h_{fe}| \bullet f_{test}$

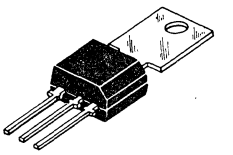
MDS60

PNP SILICON ANNULAR TRANSISTOR

. . . designed for general-purpose applications requiring high breakdown voltages, low saturation voltages and low capacitance.

- Complement to NPN Type 2N6558

DUOWATT
PNP SILICON
HIGH VOLTAGE
TRANSISTOR



4

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Collector-Base Voltage	V_{CB}	300	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	500	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 16	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150	°C

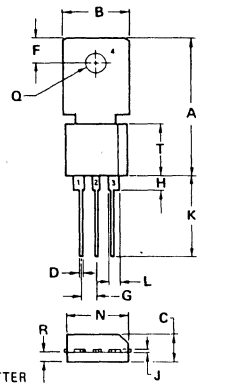
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	12.5	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector Emitter Breakdown Voltage(1) (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	300	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	300	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 200 Vdc, I_E = 0)	I_{CBO}	–	0.2	μAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 30 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 25 30 30	 – – –	–
Collector-Emitter Saturation Voltage (I_C = 30 mAdc, I_B = 3.0 mAdc)	$V_{CE(sat)}$	–	0.75	Vdc
Base-Emitter Saturation Voltage (I_C = 30 mAdc, I_B = 3.0 mAdc)	$V_{BE(sat)}$	–	0.9	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain–Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 10 MHz)	f_T	45	–	MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	8.0	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04
TO-202 AC

FIGURE 1 – DC CURRENT GAIN

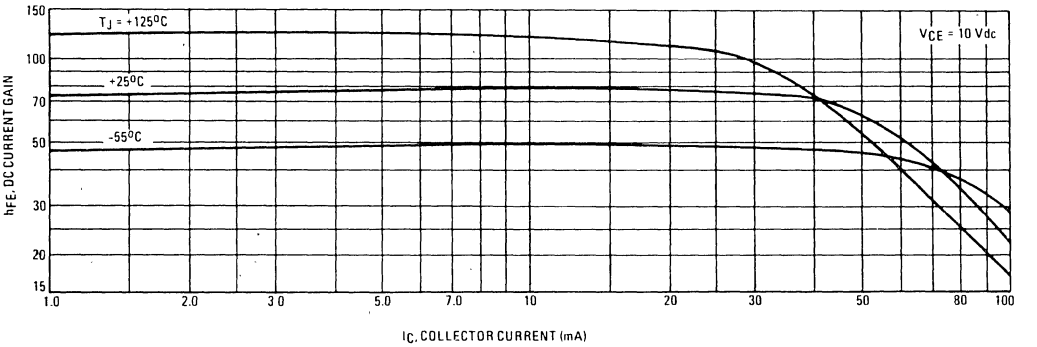


FIGURE 2 – CAPACITANCES

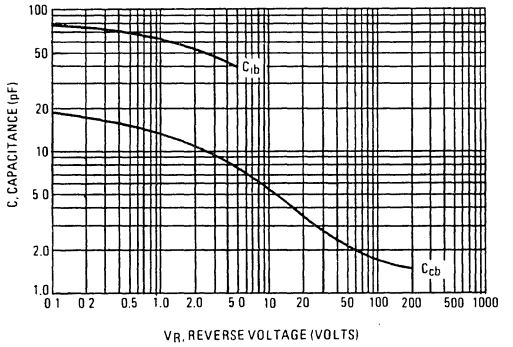


FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

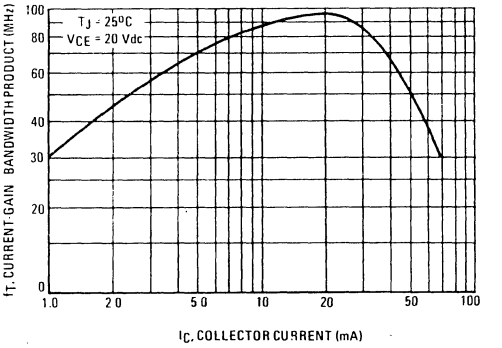


FIGURE 4 – "ON" VOLTAGES

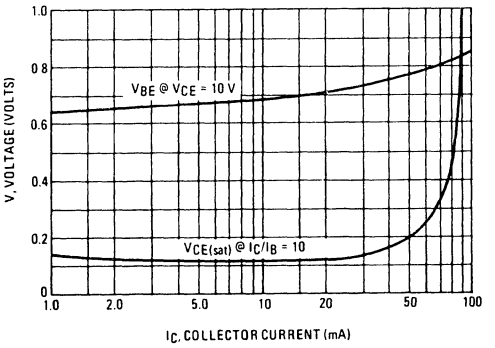
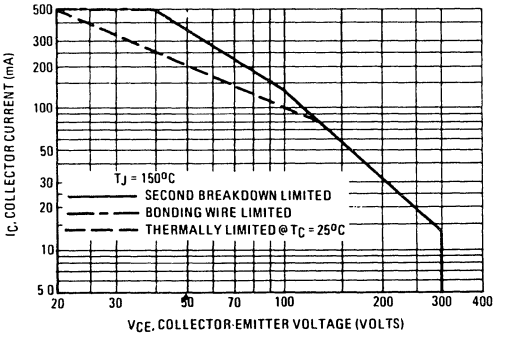


FIGURE 5 – DC SAFE OPERATING AREA



MDS1678

NPN SILICON ANNULAR◆ RF TRANSISTOR

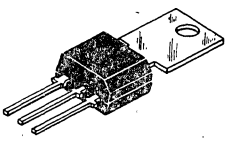
. . . designed for use in Citizen-band and other high-frequency communications equipment operating to 30 MHz. Higher breakdown voltages allow a high percentage of up-modulation in AM circuits.

- Output Power = 4 W (Min) @ V_{CC} = 12 Vdc
- Power Gain = 10 dB (Min)
- High Collector-Emitter Breakdown Voltage — $BV_{CER} \geq$ 65 Vdc

DUOWATT
4 W—27 MHz

RF POWER OUTPUT TRANSISTOR

NPN SILICON



Tab-forming and TO-5 lead-forming available on special request.

4

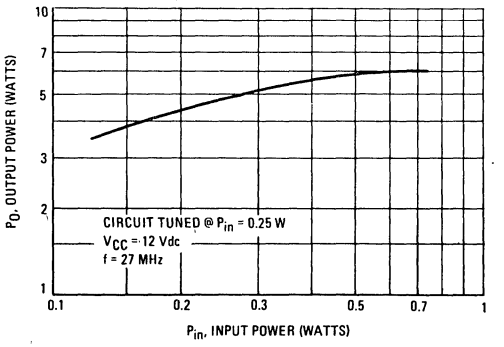
MAXIMUM RATINGS

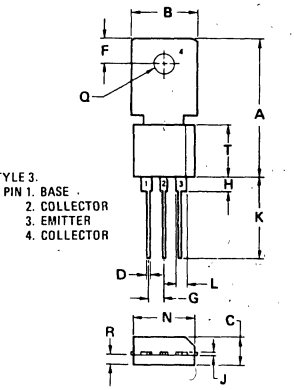
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	65	Vdc
Collector-Emitter Voltage	V_{CER}	65	Vdc
Emitter-Base Voltage	V_{EBO}	4	Vdc
Collector Current — Continuous	I_C	3	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 16	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Reistance, Junction to Case	θ_{JC}	12.5	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	62.5	°C/W

FIGURE 1 — POWER GAIN





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04
TO-202AC

◆ Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, R_{BE} = 10 Ω)	BV_{CER}	65	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1 mAdc, I_C = 0)	BV_{EBO}	4	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	0.01	mAdc
ON CHARACTERISTICS					
DC Current Gain (2) (I_C = 500 mAdc, V_{CE} = 5 Vdc) (I_C = 1.5 Adc, V_{CE} = 5 Vdc)	h_{FE}	15 10	– –	– –	–
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{CE(sat)}$	–	–	1	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	–	–	45	pF
Current-Gain—Bandwidth Product (I_C = 100 mAdc, V_{CE} = 5 Vdc, f = 20 MHz)	f_T	100	–	–	MHz
FUNCTIONAL TEST (Figure 1)					
Common-Emitter Amplifier Power Gain (P_{out} = 4 W, V_{CC} = 12 Vdc, f = 27 MHz)	G_{PE}	10	–	–	dB
Output Power (P_{in} = 400 mW, V_{CC} = 12 Vdc, f = 27 MHz)	P_{out}	4	–	–	Watts
Collector Efficiency (3) (P_{out} = 4 W, V_{CC} = 12 Vdc, f = 27 MHz)	η	–	70	–	%
Percentage Up-Modulation (4) (f = 27 MHz)	–	–	85	–	%

(1) Pulsed through a 25 mH Inductor.

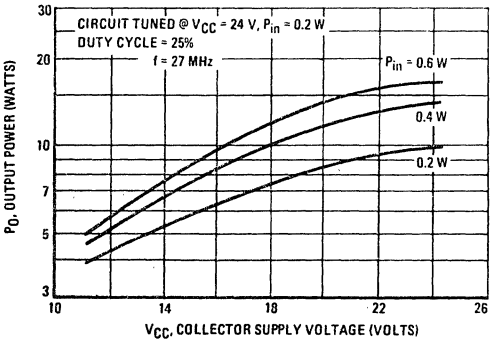
(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(3) $\eta = \frac{R_F P_{out}}{(V_{CC})(I_C)} \cdot 100$

(4) Percentage Up-Modulation is measured in the test circuit (Figure 3) by setting the Carrier Power (P_c) to 4 Watts with V_{CC} = 12 Vdc and noting the power input. Then the Peak Envelope Power (PEP) is noted after doubling the original power input to simulate driver modulation (at a 25% duty cycle for thermal considerations) and raising the V_{CC} to 24 Vdc (to simulate the modulating voltage). Percentage Up-Modulation is then determined by the relation:

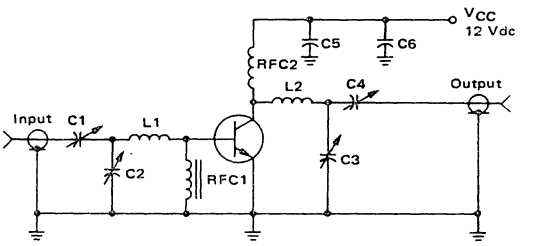
$$\text{Percentage Up-Modulation} = \left[\left(\frac{PEP}{P_c}\right)^{1/2} - 1\right] \circ 100$$

FIGURE 2 – OUTPUT POWER WITH V_{CC} VARIATIONS



C1, C2 – 9.0-180 pF ARCO 463 or equivalent
C3, C4 – 4.0-80 pF ARCO 462 or equivalent
C5 – 0.02 μF ceramic disc
C6 – 0.1 μF ceramic disc
RFC1 – 4 turns #30 enameled wire wound on ferroxcube bead type 56-590-65/3B
RFC2 – 26 Turns #22 enameled wire (2 layers—13 turns each layer) 1/4" inner diameter
L1 – 0.22 μH molded choke
L2 – 0.68 μH molded choke

FIGURE 3 – 27 MHz TEST CIRCUIT



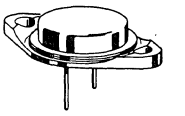
MJ410 (SILICON)
MJ411

HIGH VOLTAGE NPN SILICON TRANSISTORS

. . . designed for medium to high voltage inverters, converters, regulators and switching circuits.

- High Collector-Emitter Voltage –
  V_{CEO} = 200 Volts – MJ410
  300 Volts – MJ411
- DC Current Gain Specified @ 1.0 and 2.5 Adc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.8 Vdc @ I_C = 1.0 Adc

5 AMPERE
POWER TRANSISTORS
NPN SILICON
200-300 VOLTS
100 WATTS



4

MAXIMUM RATINGS

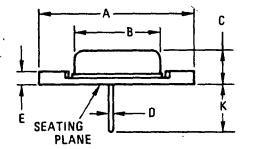
Rating	Symbol	MJ410	MJ411	Unit
Collector-Emitter Voltage	V_{CEO}	200	300	Vdc
Collector-Base Voltage	V_{CB}	200	300	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous Peak	I_C	5.0 10		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 75°C Derate above 75°C	P_D	100 1.33		Watts W/°C
Operating Junction Temperature Range	T_J	-65 to +150		°C
Storage Temperature Range	T_{stg}	-65 to +200		°C

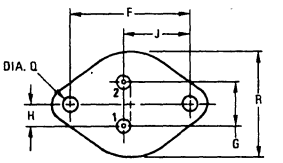
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.75	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	MJ410 MJ411	$V_{CEO(sus)}$	200 300	– –	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0) (V_{CE} = 300 Vdc, I_B = 0)	 MJ410 MJ411	I_{CEO}	 – –	 0.25 0.25	mAdc
Collector Cutoff Current (V_{CE} = 200 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 300 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	MJ410 MJ411	I_{CEX}	– –	0.5 0.5	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	30 10	90 –	–
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	–	0.8	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{BE(sat)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	2.5	–	MHz





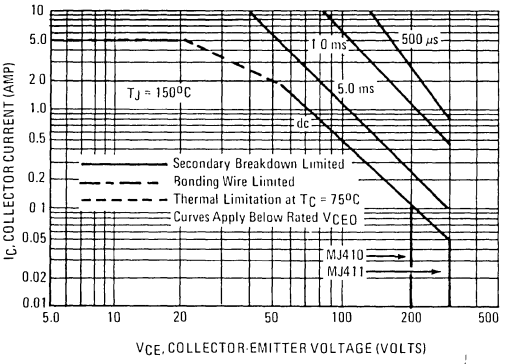
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-01
TO-3

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

4

FIGURE 2 – DC CURRENT GAIN

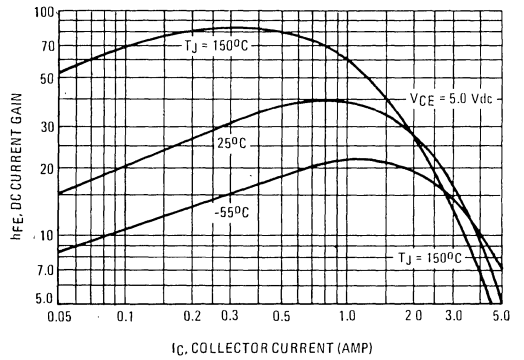


FIGURE 3 – "ON" VOLTAGES

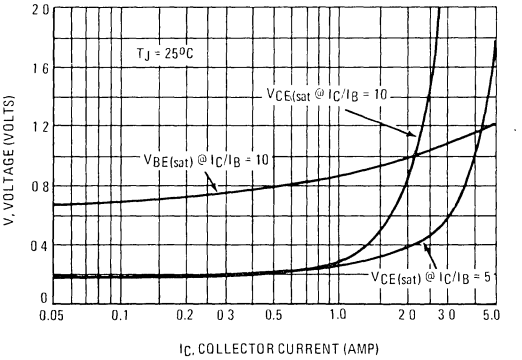


FIGURE 4 – SUSTAINING VOLTAGE TEST LOAD LINE

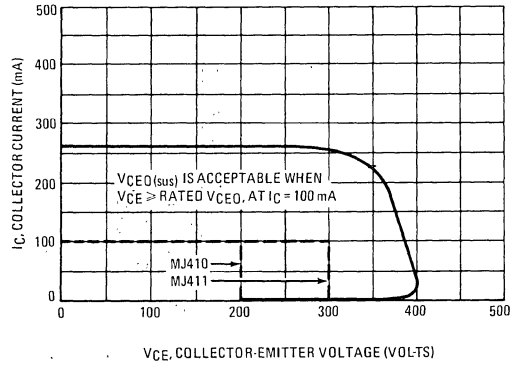
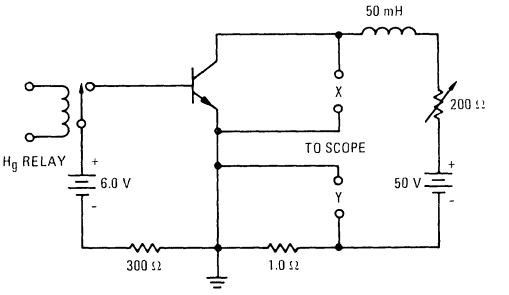


FIGURE 5 – SUSTAINING VOLTAGE TEST CIRCUIT



MJ413 (SILICON)
MJ423
MJ431

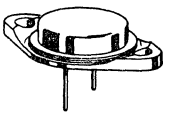
HIGH-VOLTAGE NPN SILICON TRANSISTORS

. . . designed for medium-to-high voltage inverters, converters, regulators and switching circuits.

- High Voltage — V_{CEX} = 400 Vdc
- Gain Specified to 3.5 Amp
- High Frequency Response to 2.5 MHz

10 AMPERE
POWER TRANSISTORS
NPN SILICON

400 VOLTS
125 WATTS



4

MAXIMUM RATINGS

Rating	Symbol	MJ413	MJ423	MJ431	Unit
Collector-Emitter Voltage	V_{CEX}	400	400	400	Vdc
Collector-Base Voltage	V_{CB}	400	400	400	Vdc
Emitter-Base Voltage	V_{EB}	5.0	5.0	5.0	Vdc
Collector Current — Continuous	I_C	10	10	10	Adc
Base Current	I_B	2.0	2.0	2.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1.0			Watts W/°C
Operation Junction Temperature Range	T_J	-65 to +150			°C
Storage Temperature Range	T_{stg}	-65 to +200			°C

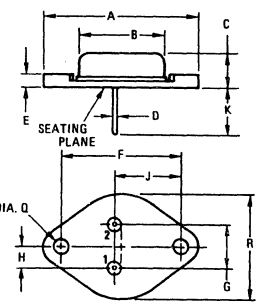
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage* (1) (I_C = 100 mAdc, I_B = 0)		$BV_{CEO(sus)}$	325	—	Vdc
Collector Cutoff Current (V_{CE} = 400 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	MJ413, MJ423 MJ431	I_{CEX}	— —	0.25 2.5	mAdc
(V_{CE} = 400 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	MJ413, MJ423 MJ431		— —	0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	MJ413, MJ423 MJ431	I_{EBO}	— —	5.0 2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)	MJ413	h_{FE}	20	80	—
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)			15	—	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	MJ423		30	90	
(I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)			10	—	
(I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)	MJ431		15	35	
(I_C = 3.5 Adc, V_{CE} = 5.0 Vdc)			10	—	
Collector-Emitter Saturation Voltage (1) (I_C = 0.5 Adc, I_B = 0.05 Adc)	MJ413	$V_{CE(sat)}$	—	0.8	Vdc
(I_C = 1.0 Adc, I_B = 0.10 Adc)	MJ423		—	0.8	
(I_C = 2.5 Adc, I_B = 0.5 Adc)	MJ431		—	0.7	
Base-Emitter Saturation Voltage (1) (I_C = 0.5 Adc, I_B = 0.05 Adc)	MJ413	$V_{BE(sat)}$	—	1.25	Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)	MJ423		—	1.25	
(I_C = 2.5 Adc, I_B = 0.5 Adc)	MJ431		—	1.5	
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10Vdc, f = 1.0 MHz)		f_T	2.5	—	MHz

(1) PW ≤ 300 μs, Duty Cycle ≤ 2.0%



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-01
TO-3

FIGURE 1 — ACTIVE-REGION SAFE-OPERATING AREA

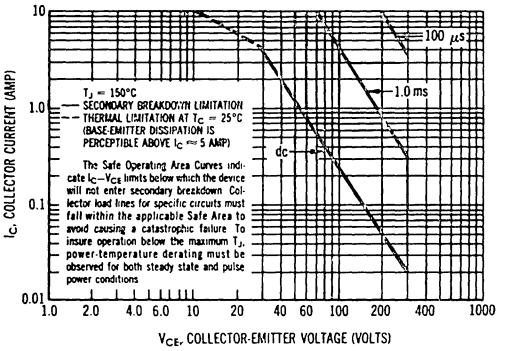


FIGURE 2 — POWER-TEMPERATURE DERATING CURVE

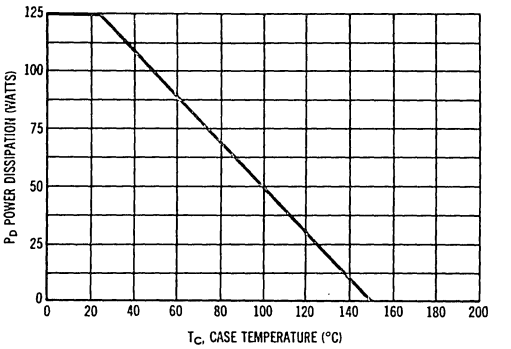


FIGURE 3 — SUSTAINING VOLTAGE TEST LOAD LINE

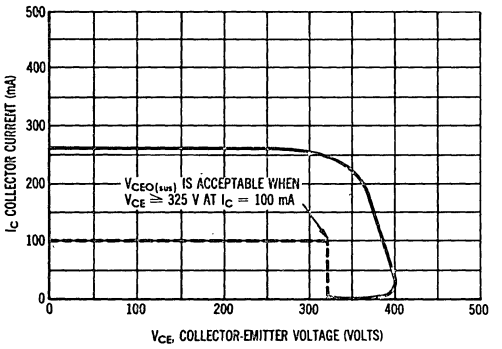


FIGURE 4 — SUSTAINING VOLTAGE TEST CIRCUIT

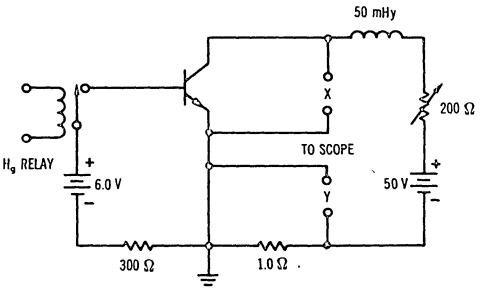


FIGURE 5 — CURRENT GAIN

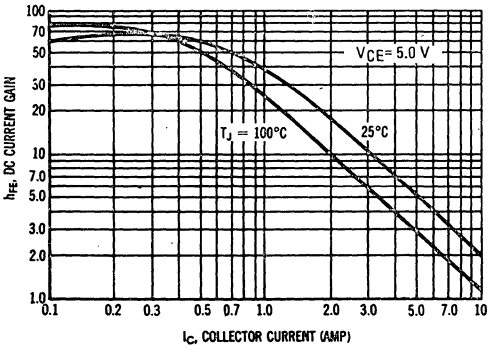
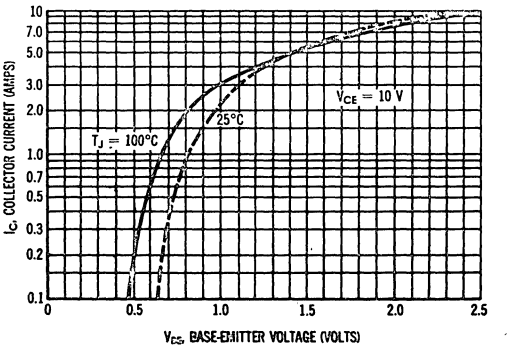


FIGURE 6 — TRANSCONDUCTANCE



MJ802 (SILICON)

HIGH-POWER NPN SILICON TRANSISTOR

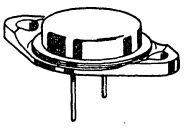
. . . for use as an output device in complementary audio amplifiers to 100-Watts music power per channel.

- High DC Current Gain – h_{FE} = 25–100 @ I_C = 7.5 A
- Excellent Safe Operating Area
- Complement to the PNP MJ4502

30 AMPERE
POWER TRANSISTOR

NPN SILICON

100 VOLTS
200 WATTS



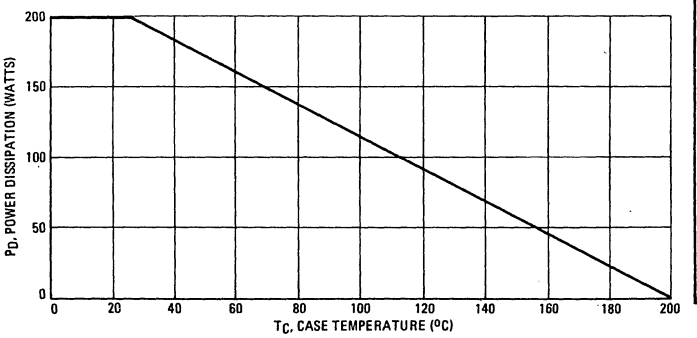
MAXIMUM RATINGS

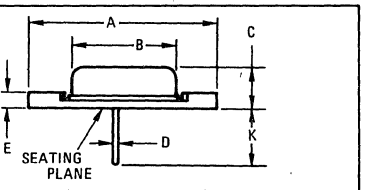
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CER}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Collector-Emitter Voltage	V_{CEO}	90	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	30	Adc
Base Current	I_B	7.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

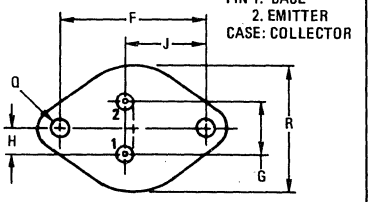
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

NOTE:
1. DIM "Q" IS DIA.

CASE 11-01
TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 200 mAdc, R_{BE} = 100 Ohms)	BV_{CER}	100	–	Vdc
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc)	$V_{CEO(sus)}$	90	–	Vdc
Collector-Base Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	–	1.0	mAdc
(V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)		–	5.0	
Emitter-Base Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (1) (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	–
Base-Emitter "On" Voltage (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	–	1.3	Vdc
Collector-Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{CE(sat)}$	–	0.8	Vdc
Base-Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{BE(sat)}$	–	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	–	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

4

FIGURE 2 – DC CURRENT GAIN

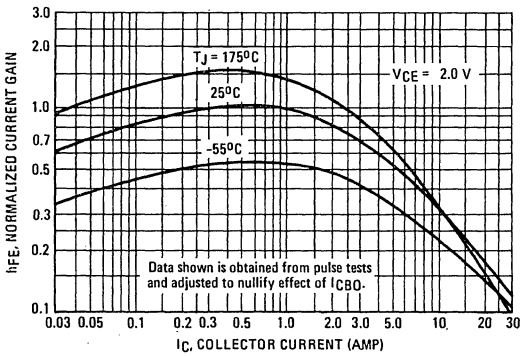


FIGURE 3 – "ON" VOLTAGES

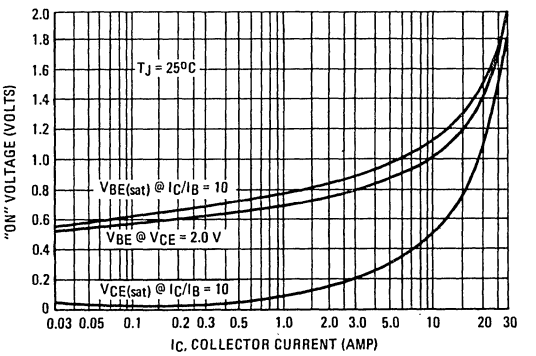
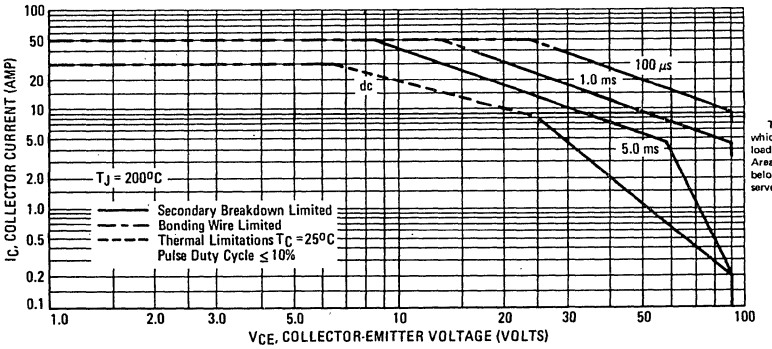


FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C – V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

MJ900, MJ901 PNP (SILICON)
MJ1000, MJ1001 NPN

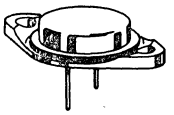
MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain – h_{FE} = 6000 (Typ) @ I_C = 3.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

8.0 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY SILICON

60-80 VOLTS
90 WATTS



4

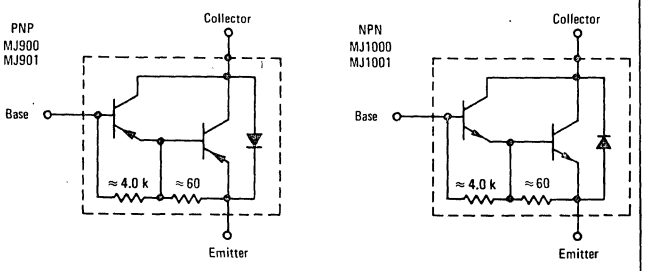
MAXIMUM RATINGS

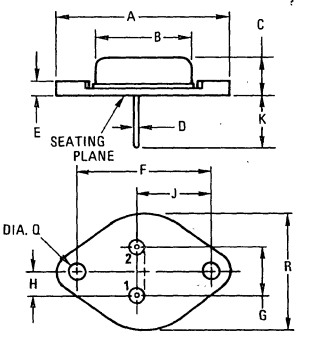
Rating	Symbol	MJ900 MJ1000	MJ901 MJ1001	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	8.0		Adc
Base Current	I_B	0.1		Adc
Total Device Dissipation @ $T_C = 25^oC$	P_D	90		Watts
Derate above 25^oC		0.515		$W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.94	$^oC/W$

FIGURE 1 – DARLINGTON CIRCUIT SCHEMATIC





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1)		BV_{CEO}			Vdc
(I_C = 100 mAdc, I_B = 0)	MJ900, MJ1000		60	–	
	MJ901, MJ1001		80	–	
Collector Emitter Leakage Current		I_{CER}			mAdc
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm)	MJ900, MJ1000		–	1.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm)	MJ901, MJ1001		–	1.0	
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ900, MJ1000		–	5.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ901, MJ1001		–	5.0	
Emitter Cutoff Current		I_{EBO}	–	2.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
Collector-Emitter Leakage Current		I_{CEO}			μAdc
(V_{CE} = 30 Vdc, I_B = 0)	MJ900, MJ1000		–	500	
(V_{CE} = 40 Vdc, I_B = 0)	MJ901, MJ1001		–	500	
ON CHARACTERISTICS					
DC Current Gain(1)		h_{FE}			–
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)			1000	–	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			750	–	
Collector-Emitter Saturation Voltage(1)		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 12 mAdc)			–	2.0	
(I_C = 8.0 Adc, I_B = 40 mAdc)			–	4.0	
Base-Emitter Voltage(1)		V_{BE}	–	2.5	Vdc
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)					

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

4

FIGURE 2 – DC CURRENT GAIN

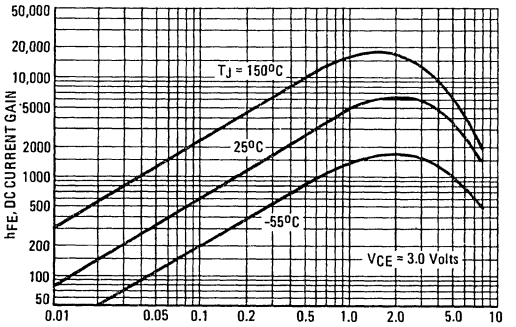


FIGURE 3 – SMALL-SIGNAL CURRENT GAIN

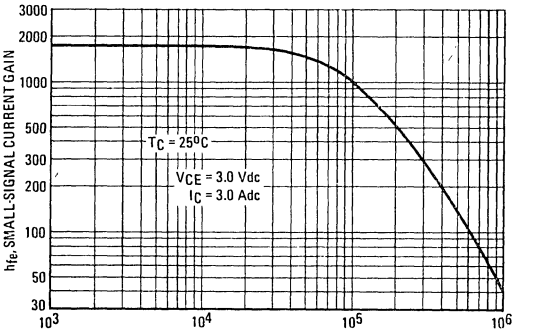


FIGURE 4 – "ON" VOLTAGES

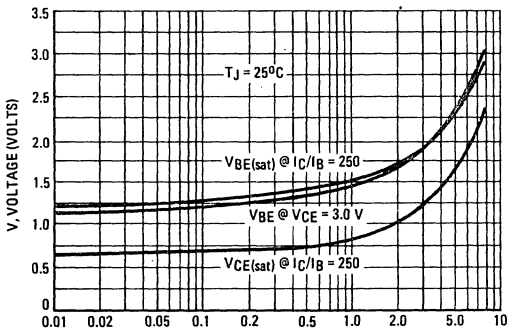
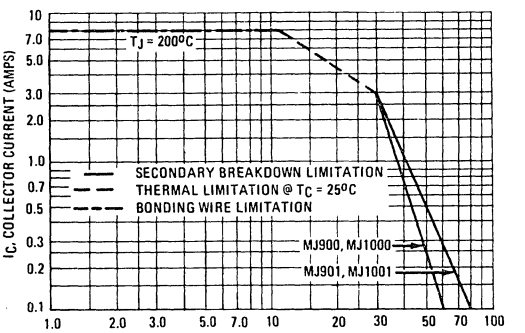


FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MJ2500, MJ2501 PNP (SILICON)
MJ3000, MJ3001 NPN

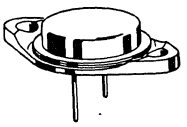
MEDIUM-POWER COMPLEMENTARY
SILICON TRANSISTORS

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain – h_{FE} = 4000 (Typ) @ I_C = 5.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

10 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY SILICON

60-80 VOLTS
150 WATTS



4

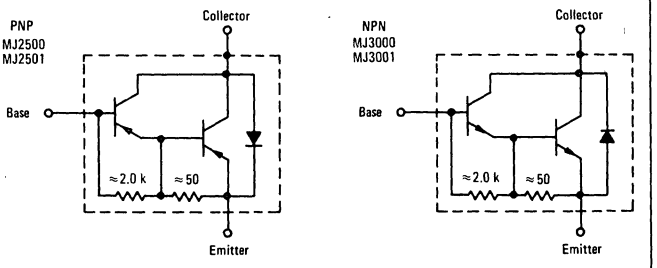
MAXIMUM RATINGS

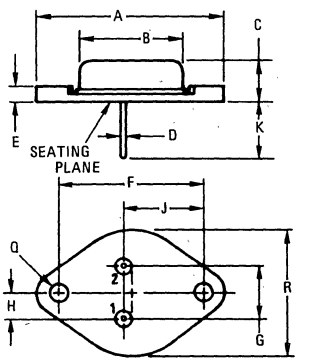
Rating	Symbol	MJ2500 MJ3000	MJ2501 MJ3001	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	10		Adc
Base Current	I_B	0.2		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.857		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

FIGURE 1 – DARLINGTON CIRCUIT SCHEMATIC





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-01
TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 100 mAdc, I_B = 0)	MJ2500, MJ3000 MJ2501, MJ3001	BV_{CEO}	60 80	– –	Vdc
Collector Emitter Leakage Current		I_{CER}			mAdc
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm)	MJ2500, MJ3000		–	1.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm)	MJ2501, MJ3001		–	1.0	
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ2500, MJ3000		–	5.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ2501, MJ3001		–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	2.0	mAdc
Collector-Emitter Leakage Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	MJ2500, MJ3000		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	MJ2501, MJ3001		–	1.0	
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	1000	–	–
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 20 mAdc)			–	2.0	
(I_C = 10 Adc, I_B = 50 mAdc)			–	4.0	
Base-Emitter Voltage (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)		V_{BE}	–	3.0	Vdc

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

4

FIGURE 2 – DC CURRENT GAIN

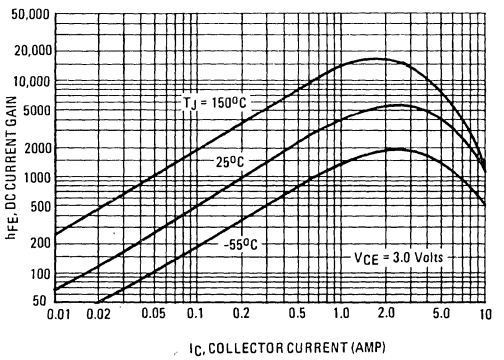


FIGURE 3 – SMALL-SIGNAL CURRENT GAIN

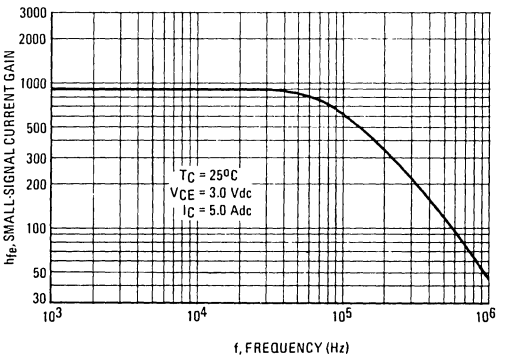


FIGURE 4 – "ON" VOLTAGES

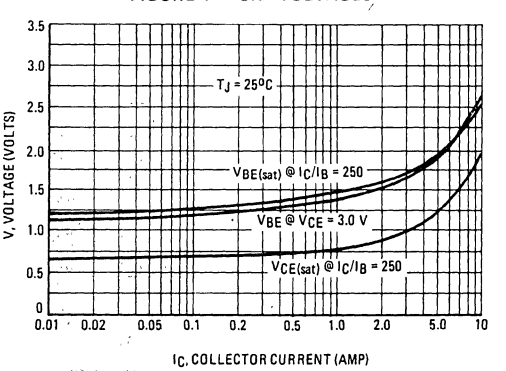
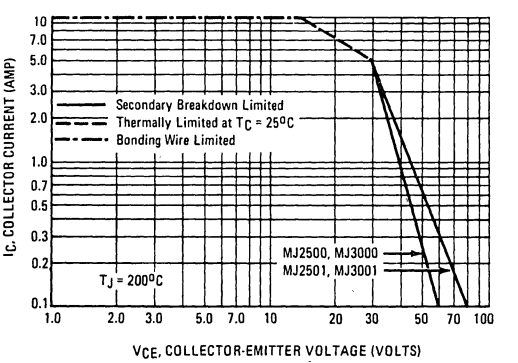


FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

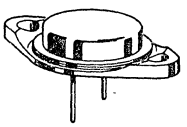
MJ3029 (SILICON)
MJ3030

NPN SILICON HIGH-VOLTAGE TRANSISTORS

. . . designed for TV horizontal and vertical deflection amplifier circuits.

- High Collector-Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 250 Vdc (Min) MJ3029
  325 Vdc (Min) MJ3030
- Fast Fall Time in Horizontal Deflection —
  t_f = 1.0 μs (Max) @ V_{CC} = 80 Vdc — MJ3030
- Excellent Gain Linearity for Vertical Deflection —
  h_{fe} @ 0.4 Adc, h_{fe} @ 0.3 Adc = 0.95 (Min) — MJ3029

5 AMPERE
POWER TRANSISTORS
NPN SILICON
250-325 VOLTS
125 WATTS



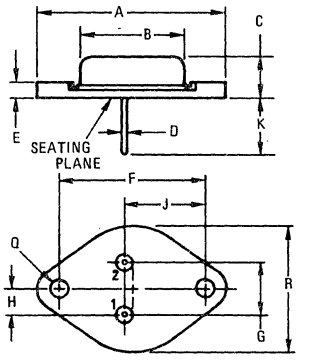
4

MAXIMUM RATINGS

Rating	Symbol	MJ3029	MJ3030	Unit
Collector-Emitter Voltage	V_{CEO}	250	325	Vdc
Collector-Emitter Voltage	V_{CER}	500	—	Vdc
Collector-Emitter Voltage	V_{CEX}	—	700	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	5.0		Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1.0		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.0	°C/W



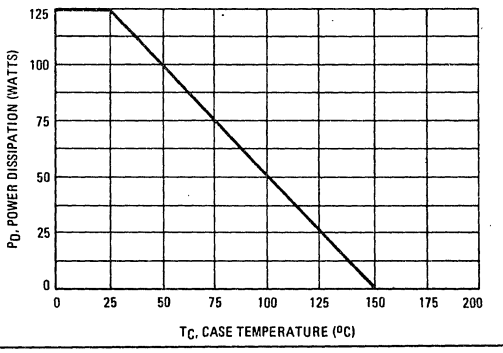
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050

CASE 11-01
TO-3

FIGURE 1 — POWER-TEMPERATURE DERATING CURVE



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage(1) (I_C = 0.1 Adc, I_B = 0)	MJ3029 MJ3030	$V_{CEO(sus)}$	250 325	– –	Vdc
Collector Cutoff Current (V_{CE} = 500 Vdc, R_{BE} = 1.5 k Ohms)	MJ3029	I_{CER}	–	1.0	mAdc
Collector Cutoff Current (V_{CE} = 700 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	MJ3030	I_{CEX}	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 5.0 Vdc)(1) (I_C = 0.4 Adc, V_{CE} = 5.0 Vdc)(1)	MJ3029 MJ3029	$\frac{h_{FE1}}{h_{FE2}}$	25 30	– –	–
Gain Linearity	MJ3029	$\frac{h_{FE2}}{h_{FE1}}$	0.95	–	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.8 Adc)	MJ3030	$V_{CE(sat)}$	–	2.0	Vdc
SWITCHING CHARACTERISTICS					
Fall Time (V_{CC} = 80 Vdc, I_C = 3.0 Adc, I_{B1} = 0.8 Adc) Figure 3	MJ3030	t_f	–	1.0	μs

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

4

FIGURE 2 – DC CURRENT GAIN

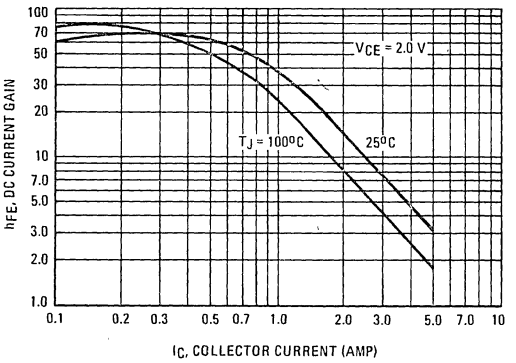
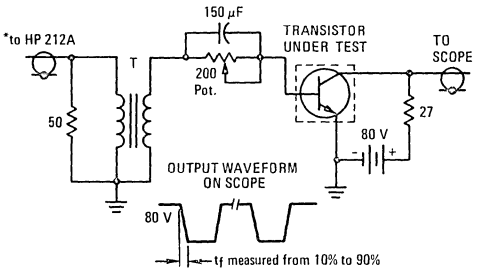
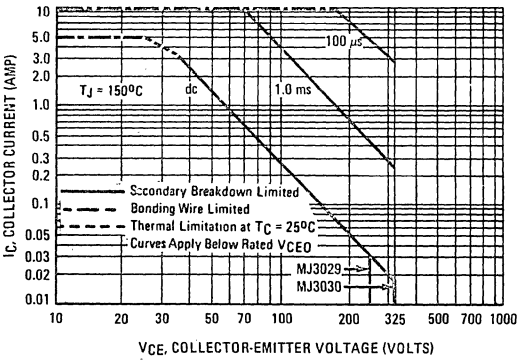


FIGURE 3 – TEST FOR FALL TIME



*HP 212A: Set for 10 μs wide pulses at 2000 pulses per sec. (500 μs intervals). Adjust for I_{B1} = 0.8 A.
Bias: Adjust to 1.5 V on a VTVM across the 200 Ω Pot.
T: Pulse Transformer: Motorola Part No. 25D68782A01.

FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MJ3040
MJ3041
MJ3042

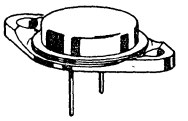
HIGH VOLTAGE SILICON POWER DARLINGTONS

. . . developed for line operated amplifier, series pass and switching regulator applications.

- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 300 Vdc (Min) – MJ3040, MJ3041
  = 350 Vdc (Min) – MJ3042
- High DC Current Gain –
  h_{FE} = 100 (Min) @ I_C = 2.5 Adc – MJ3040
  = 250 (Min) @ I_C = 2.5 Adc – MJ3041, MJ3042
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 2.2 Vdc (Max) @ I_C = 2.5 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors

DARLINGTON 10 AMPERE POWER TRANSISTORS NPN SILICON

300, 350 VOLTS
175 WATTS



MAXIMUM RATINGS

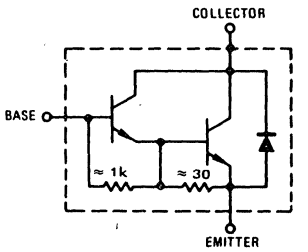
Rating	Symbol	MJ3040	MJ3041	MJ3042	Unit
Collector-Base Voltage	V_{CB}	400	400	500	Vdc
Collector-Emitter Voltage	V_{CEO}	300	300	350	Vdc
Emitter-Base Voltage	V_{EB}	← 8.0 →			Vdc
Collector Current – Continuous – Peak (1)	I_C	← 10 → ← 15 →			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	← 175 → ← 1.0 →			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +200 →			°C

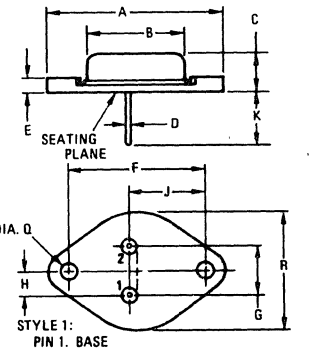
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

(1) Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

DARLINGTON SCHEMATIC





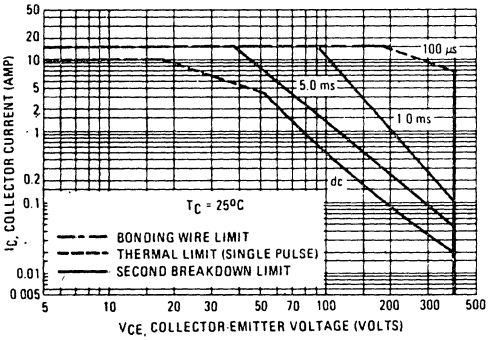
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	MJ3040, MJ3041	$V_{CEO(sus)}$	300	–	Vdc
	MJ3042		350	–	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 400 Vdc, I_E = 0)	MJ3040, MJ3041		–	1.0	
(V_{CB} = 500 Vdc, I_E = 0)	MJ3042		–	1.0	
(V_{CB} = 400 Vdc, I_E = 0, T_C = 100°C)	MJ3040, MJ3041		–	5.0	
(V_{CB} = 500 Vdc, I_E = 0, T_C = 100°C)	MJ3042		–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	40	mAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)	MJ3040		100	–	
	MJ3041, MJ3042		250	–	
(I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	MJ3040		25	–	
	MJ3041, MJ3042		50		
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 2.5 Adc, I_B = 50 mAdc)			–	2.2	
(I_C = 5.0 Adc, I_B = 400 mAdc)			–	2.5	
Base-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 400 mAdc)		$V_{BE(sat)}$	–	3.0	Vdc
Base-Emitter On Voltage (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	2.5	Vdc

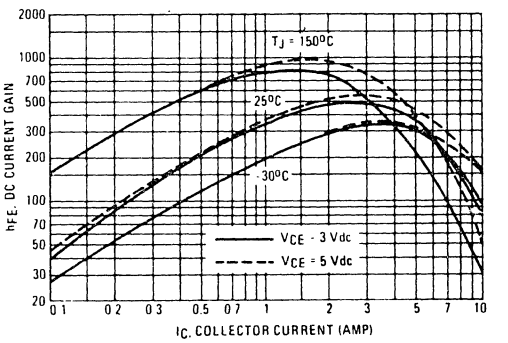
FIGURE 1 – FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor – average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 – DC CURRENT GAIN



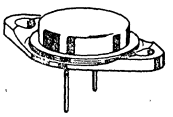
MJ4030, MJ4031, MJ4032 PNP (SILICON)
MJ4033, MJ4034, MJ4035 NPN

MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain – h_{FE} = 3500 (Typ) @ I_C = 10 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistor

16 AMPERE
DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON
60–100 VOLTS
150 WATTS



4

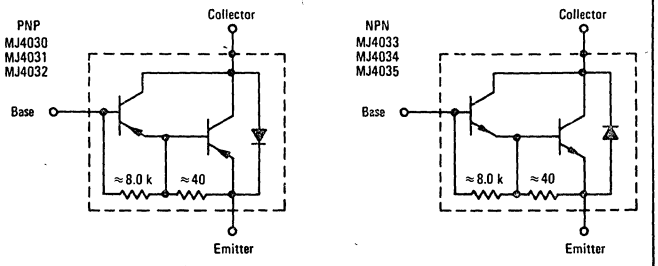
MAXIMUM RATINGS

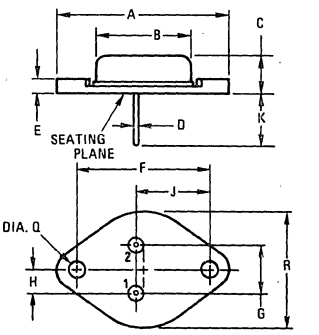
Rating	Symbol	MJ4030 MJ4033	MJ4031 MJ4034	MJ4032 MJ4035	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current	I_C	16			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.857			Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	−55 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

FIGURE 1 – DARLINGTON CIRCUIT SCHEMATIC





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 100 mAdc, I_B = 0)	MJ4030, MJ4033	BV_{CEO}	60	–	Vdc
	MJ4031, MJ4034		80	–	
	MJ4032, MJ4035		100	–	
Collector Emitter Leakage Current		I_{CER}			mAdc
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm)	MJ4030, MJ4033		–	1.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm)	MJ4031, MJ4034		–	1.0	
(V_{CB} = 100 Vdc, R_{BE} = 1.0 k ohm)	MJ4032, MJ4035		–	1.0	
(V_{CB} = 60 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ4030, MJ4033		–	5.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ4031, MJ4034		–	5.0	
(V_{CB} = 100 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ4032, MJ4035		–	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	5.0	mAdc
Collector-Emitter Leakage Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	MJ4030, MJ4033		–	3.0	
(V_{CE} = 40 Vdc, I_B = 0)	MJ4031, MJ4034		–	3.0	
(V_{CE} = 50 Vdc, I_B = 0)	MJ4032, MJ4035		–	3.0	
ON CHARACTERISTICS(1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	1000	–	–
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 40 mAdc)			–	2.5	
(I_C = 16 Adc, I_B = 80 mAdc)			–	4.0	
Base-Emitter Voltage (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		V_{BE}	–	3.0	Vdc

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

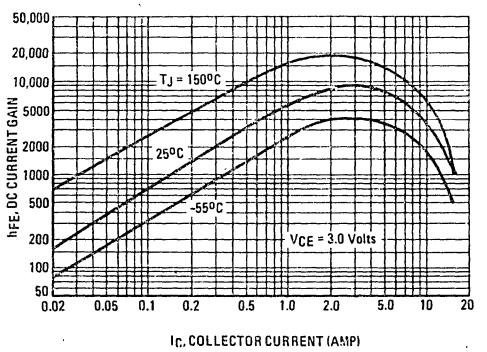


FIGURE 3 – SMALL-SIGNAL CURRENT GAIN

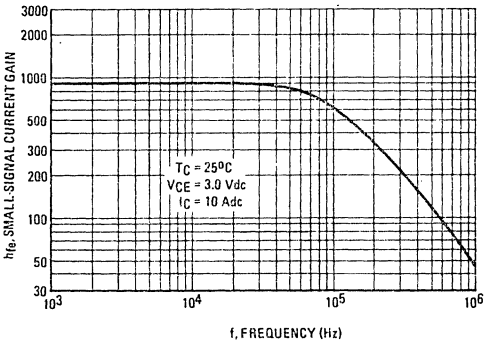


FIGURE 4 – "ON" VOLTAGES

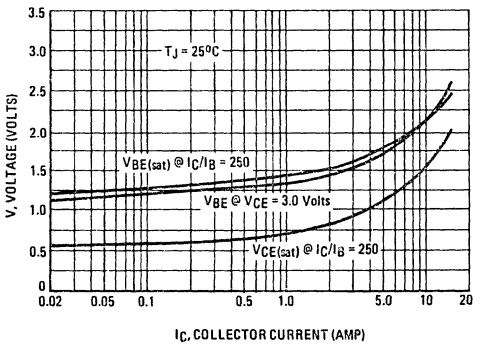
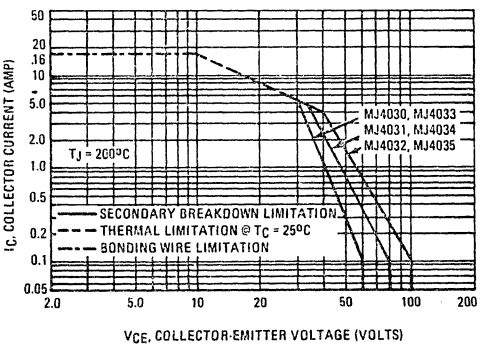


FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MJ4502 (SILICON)

HIGH-POWER PNP SILICON TRANSISTOR

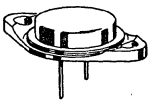
. . . for use as an output device in complementary audio amplifiers to 100-Watts music power per channel.

- High DC Current Gain – h_{FE} = 25-100 @ I_C = 7.5 A
- Excellent Safe Operating Area
- Complement to the NPN MJ802

30 AMPERE
POWER TRANSISTOR

PNP SILICON

100 VOLTS
200 WATTS



4

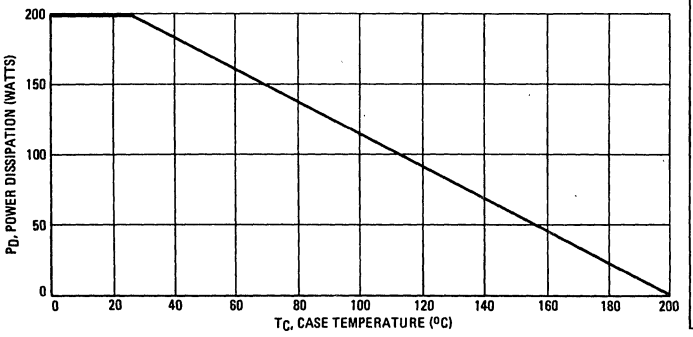
MAXIMUM RATINGS

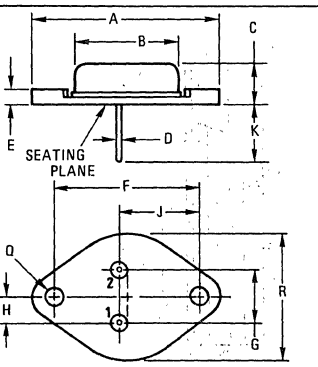
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CER}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Collector-Emitter Voltage	V_{CEO}	90	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	30	Adc
Base Current	I_B	7.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-01
TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage [1] (I_C = 200 mAdc, R_{BE} = 100 Ohms)	BV_{CER}	100	–	Vdc
Collector-Emitter Sustaining Voltage [1] (I_C = 200 mAdc)	$V_{CEO(sus)}$	90	–	Vdc
Collector-Base Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	–	1.0	mAdc
(V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)		–	5.0	
Emitter-Base Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS [1]				
DC Current Gain (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	–
Base-Emitter "On" Voltage (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	–	1.3	Vdc
Collector-Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{CE(sat)}$	–	0.8	Vdc
Base-Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{BE(sat)}$	–	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	–	MHz

[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

4

FIGURE 2 – DC CURRENT GAIN

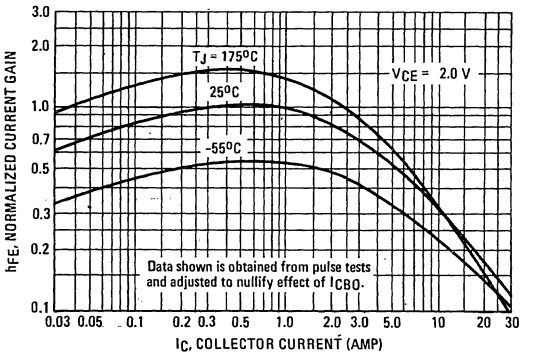


FIGURE 3 – "ON" VOLTAGES

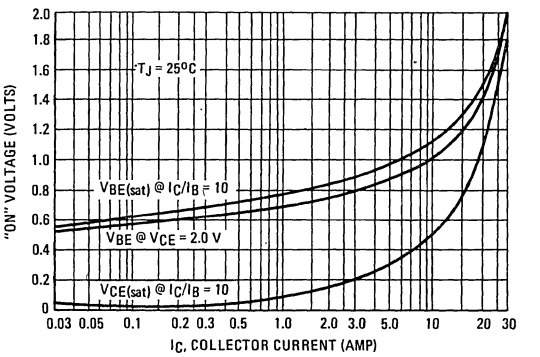
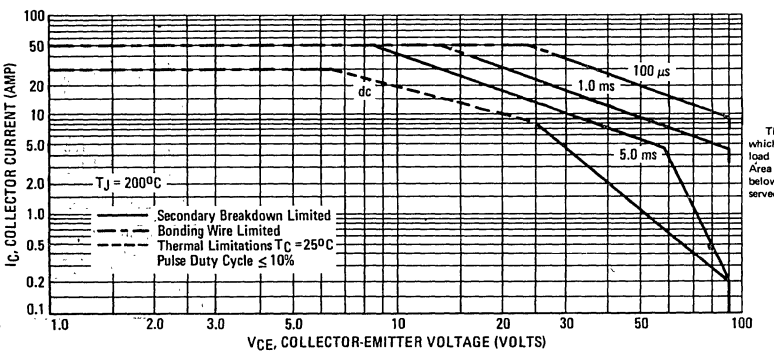


FIGURE 4 – ACTIVE REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

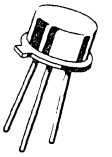
MJ4645 (SILICON) thru MJ4647

PNP SILICON POWER TRANSISTORS

. . . designed for high-voltage amplifier and saturated switching applications at collector currents to one Ampere. Ideally suited for applications of dc-to-dc converters, relay and hammer drivers, motor controls, and servo and pulse amplifiers. High-voltage ratings permit direct-line operation.

- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = < 1.5 Vdc (Max) @ I_C = 500 mAdc
- High Collector-Emitter Breakdown Voltage – BV_{CEO} = 200, 300, and 400 Vdc (Min)
- DC Current Gain Specified – 10 mAdc to 500 mAdc

1.0 AMPERE
POWER TRANSISTORS
PNP SILICON
200-300-400 VOLTS
5 WATTS



4

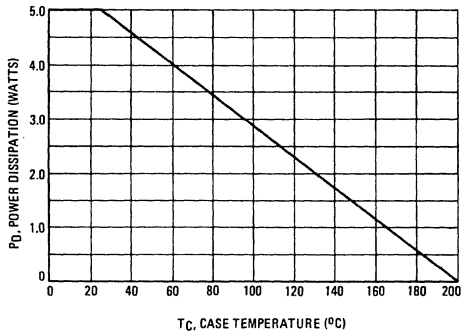
MAXIMUM RATINGS

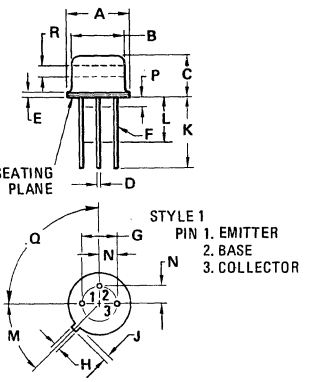
Rating	Symbol	MJ4645	MJ4646	MJ4647	Unit
Collector-Emitter Voltage	V_{CEO}	200	300	400	Vdc
Collector-Base Voltage	V_{CB}	200	300	400	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current – Continuous Peak	I_C	← 0.5 → ← 1.0 →			Adc
Total Device Dissipation @ T_C = 25°C	P_D	← 5.0 →			Watts
Derate above 25°C		← 28.6 →			mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	← -65 to +200 →			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	35	°C/W

FIGURE 1 – POWER DERATING





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

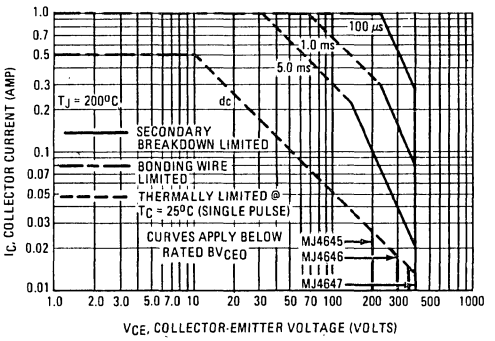
CASE 79-02
TO-39

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, I_B = 0)	MJ4645	BV_{CEO}	200	–	–	Vdc
	MJ4646		300	–	–	
	MJ4647		400	–	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	MJ4645	BV_{CBO}	200	–	–	Vdc
	MJ4646		300	–	–	
	MJ4647		400	–	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, $V_{BE(off)}$ = 0.5 Vdc)		I_{CEX}	–	–	10	μAdc
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				–
(I_C = 10 mAdc, V_{CE} = 10 Vdc)			20	–	–	
(I_C = 100 mAdc, V_{CE} = 10 Vdc) (1)			25	–	–	
(I_C = 500 mAdc, V_{CE} = 10 Vdc) (1)			20	–	–	
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 100 mAdc)	MJ4645	$V_{CE(sat)}$	–	0.5	1.0	Vdc
	MJ4646		–	0.6	1.2	
	MJ4647		–	0.75	1.5	
DYNAMIC CHARACTERISTICS						
Current-Gain–Bandwidth Product (I_C = 70 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)	MJ4645, MJ4646	f_T	40	–	–	MHz
	MJ4647,		30	–	–	
Output Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 100 kHz)	MJ4645	C_{ob}	–	–	80	pF
	MJ4646, MJ4647		–	–	60	
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 100 Vdc, I_C = 500 mAdc,	t_d	–	–	100	ns
Rise Time	I_{B1} = 50 mAdc, $V_{BE(off)}$ = 5.0 Vdc)	t_r	–	–	100	ns
Turn-Off Time	(V_{CC} = 100 Vdc, I_C = 500 mAdc, I_{B1} = I_{B2} = 50 mAdc, Pulse Width = 1.0 μs)	t_{off}	–	–	720	ns

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MJ6700 (SILICON)

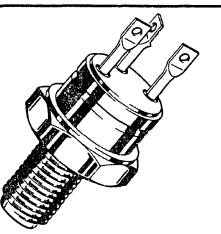
MEDIUM-POWER PNP SILICON TRANSISTORS

. . . designed for switching and wide-band amplifier applications.

- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 7.0 Adc
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact, High Dissipation TO-59 Case
- Isolated Collector Configuration – 700 V Breakdown

7 AMPERE
POWER TRANSISTORS
PNP SILICON

60 VOLTS
60 WATTS



4

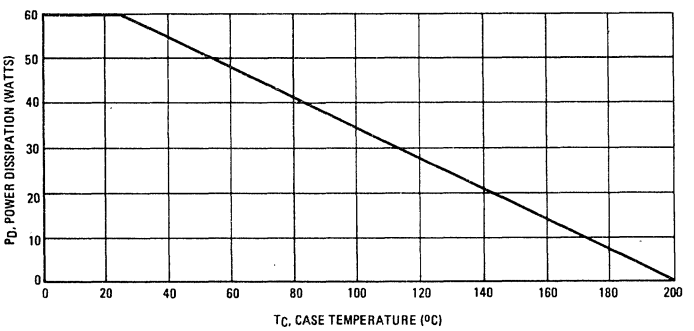
MAXIMUM RATINGS

Rating	Symbol	MJ6700	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	7.0	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	60 343	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

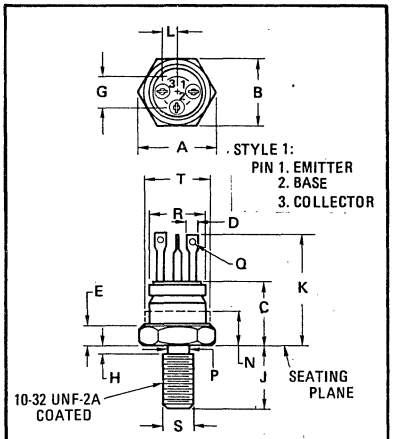
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2.91	°C/W

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 2. All limits are applicable and must be observed.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	10.77	11.10	0.424	0.437
C	8.13	11.89	0.320	0.468
E	2.29	3.81	0.090	0.150
G	4.70	5.46	0.185	0.215
H	–	1.98	–	0.078
J	10.16	11.56	0.400	0.455
K	14.48	19.38	0.570	0.763
L	2.29	2.79	0.090	0.110
N	–	6.35	–	0.250
P	4.14	4.80	0.163	0.189
Q	1.02	1.65	0.040	0.065
R	8.08	9.65	0.318	0.380
S	4.212	4.310	0.1658	0.1697
T	9.65	11.10	0.380	0.437

All JEDEC dimensions and notes apply
Collector isolated from case.

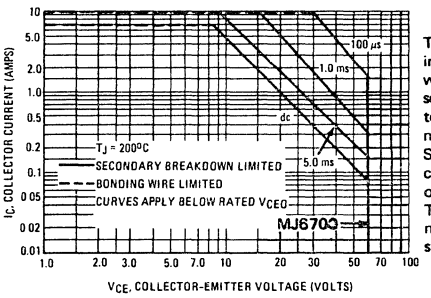
CASE 160-03
(TO-59)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage [1] (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector Cutoff Current (V_{CE} = 55 Vdc, I_B = 0)	I_{CEO}	–	100	μAdc
Collector Cutoff Current (V_{CE} = 55 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	–	10	μAdc
(V_{CE} = 55 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		–	1.0	mAdc
Collector Cutoff Current (V_{CB} = 60Vdc, I_E = 0)	I_{CBO}	–	10	μAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS [1]				
DC Current Gain (I_C = 500 mAdc, V_{CE} = 2.0 Vdc)	h_{FE}	25	–	–
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)		25	180	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)		15	–	
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc)	$V_{CE(sat)}$	–	0.7	Vdc
(I_C = 7.0 Adc, I_B = 0.7 Adc)		–	1.2	
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc)	$V_{BE(sat)}$	–	1.2	Vdc
(I_C = 7.0 Adc, I_B = 0.7 Adc)		–	2.0	
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)	f_T	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	300	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)	C_{ib}	–	1250	pF
SWITCHING CHARACTERISTICS				
Delay Time	(V_{CC} = 40 Vdc, $V_{BE(off)}$ = 4.0 Vdc,	t_d	–	100	ns
Rise Time	I_C = 2.0 Adc, I_{B1} = 200 mAdc)	t_r	–	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc,	t_s	–	1.0	μs
Fall Time	I_{B1} = I_{B2} = 200 mAdc)	t_f	–	150	ns

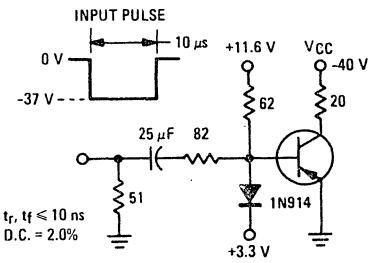
[1] Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%

FIGURE 2 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 3 – SWITCHING TIME TEST CIRCUIT



MJ8100 (SILICON)

4

MEDIUM-POWER PNP SILICON TRANSISTORS

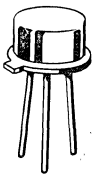
. . . designed for switching and wide band amplifier applications.

- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 5.0 Amp
- DC Current Gain Specified to 5 Amperes
- Excellent Safe Operating Area
- Packaged in the Compact TO-39 Case for Critical Space-Limited Applications.

5 AMPERE
POWER TRANSISTORS

PNP SILICON

60 VOLTS
10 WATTS



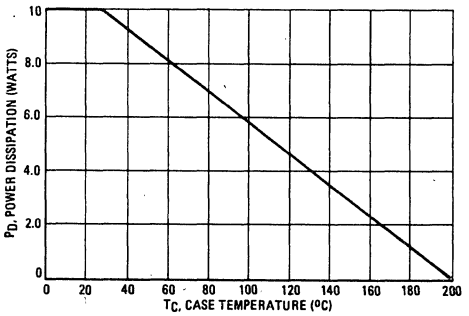
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	5.0	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 57.2	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

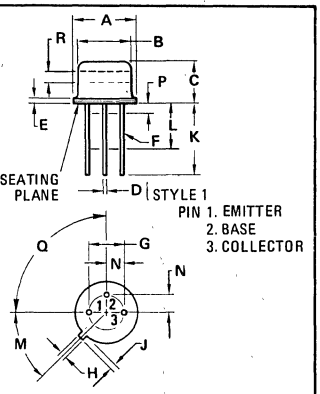
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	17.5	°C/W

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE



Safe Area Curves are indicated by Figure 2. All limits are applicable and must be observed.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

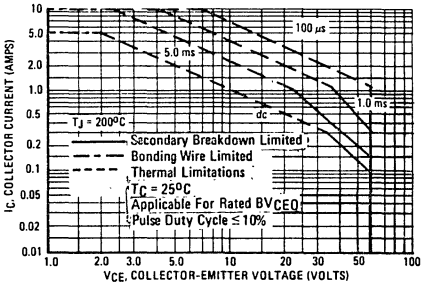
All JEDEC dimensions and notes apply.
CASE 79-02
TO-39

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage [1] (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector Cutoff Current (V_{CE} = 55 Vdc, I_B = 0)	I_{CEO}	–	100	μAdc
Collector Cutoff Current (V_{CE} = 55 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	–	10	μAdc
(V_{CE} = 55 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		–	1.0	mAdc
Collector Cutoff Current (V_{CB} = 60 V, I_E = 0)	I_{CBO}	–	10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 500 mAdc, V_{CE} = 2.0 Vdc)	h_{FE}	25	–	–
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)		25	180	
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)		15	–	
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc)	$V_{CE(sat)}$	–	0.7	Vdc
(I_C = 5.0 Adc, I_B = 0.5 Adc)		–	1.2	
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc)	$V_{BE(sat)}$	–	1.2	Vdc
(I_C = 5.0 Adc, I_B = 0.5 Adc)		–	1.8	
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 10 MHz)	f_T	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	300	pF
Input Capacitance (V_{BE} = 2.0 Vdc, I_C = 0, f = 100 kHz)	C_{ib}	–	1250	pF
SWITCHING CHARACTERISTICS				
Delay Time	(V_{CC} = 40 Vdc, $V_{BE(off)}$ = 4.0 Vdc,	t_d	–	100	ns
Rise Time	I_C = 2.0 Adc, I_{B1} = 0.2 Adc)	t_r	–	100	ns
Storage Time	(V_{CC} = 40 Vdc, I_C = 2.0 Adc,	t_s	–	1.0	μs
Fall Time	I_{B1} = I_{B2} = 0.2 Adc)	t_f	–	150	ns

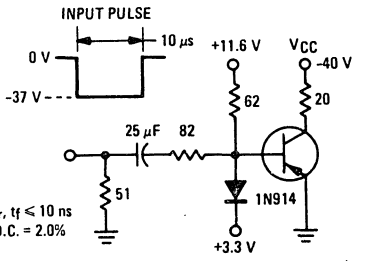
[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

FIGURE 2 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 3 – SWITCHING TIME TEST CIRCUIT



MJ10000
MJ10001

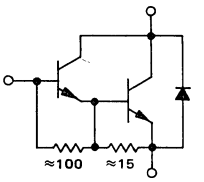
Designers Data Sheet

20 AMPERE
NPN SILICON
POWER DARLINGTON TRANSISTORS
350 and 400 VOLTS
175 WATTS

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS

The MJ10000 and MJ10001 darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



100°C Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times With Inductive Loads —
210 ns Inductive Fall Time (Typ)
Saturation Voltages
Leakage Currents

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

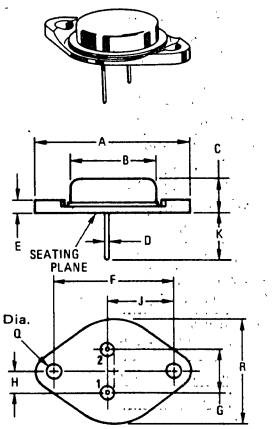
MAXIMUM RATINGS

Rating	Symbol	MJ10000	MJ10001	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	20 30		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.5 5		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (2)					
Collector-Emitter Sustaining Voltage (Table 1)	$V_{CEO(sus)}$				Vdc
(I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO}) MJ10000		350	–	–	
MJ10001		400	–	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12)	$V_{CEX(sus)}$				Vdc
I_C = 2 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C MJ10000		400	–	–	
MJ10001		450	–	–	
I_C = 10 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C MJ10000		275	–	–	
MJ10001		325	–	–	
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		–	–	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		–	–	5	
Collector Cutoff Current	I_{CER}	–	–	5	mAdc
(V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)					
Emitter Cutoff Current	I_{EBO}	–	–	150	mAdc
(V_{EB} = 8 Vdc, I_C = 0)					
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 11			Adc
ON CHARACTERISTICS (2)					
DC Current Gain	h_{FE}				–
(I_C = 5 Adc, V_{CE} = 5 Vdc)		50	–	600	
(I_C = 10 Adc, V_{CE} = 5 Vdc)		40	–	400	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 400 mAdc)		–	–	1.9	
(I_C = 20 Adc, I_B = 1 Adc)		–	–	3	
(I_C = 10 Adc, I_B = 400 mAdc, T_C = 100°C)		–	–	2	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 400 mAdc)		–	–	2.5	
(I_C = 10 Adc, I_B = 400 mAdc, T_C = 100°C)		–	–	2.5	
Diode Forward Voltage (1)	V_f	–	3	5	Vdc
(I_F = 10 Adc)					
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain	$\lvert h_{fe} \rvert$	10		–	–
(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)					
Output Capacitance	C_{ob}	100		325	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)					
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 250 Vdc, I_C = 10 A,	t_d	–	0.12	0.2	μs
Rise Time I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs,	t_r	–	0.20	0.6	μs
Storage Time Duty Cycle ≤ 2%).	t_s	–	1.5	3.5	μs
Fall Time	t_f	–	1.1	2.4	μs
Inductive Load, Clamped (Table 1)					
Storage Time (I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA,	t_{sv}	–	3.5	5.5	μs
Crossover Time $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_c	–	1.5	3.7	μs
Storage Time (I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA,	t_{sv}	–	1.0	–	μs
Crossover Time $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_c	–	0.7	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

4

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

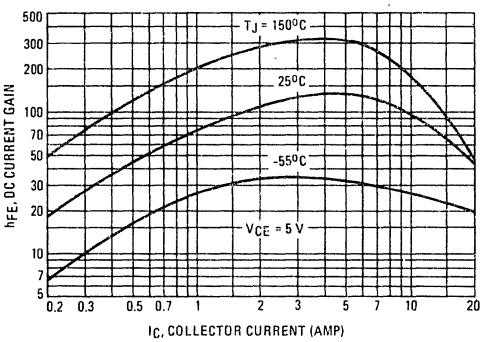


FIGURE 2 – COLLECTOR SATURATION REGION

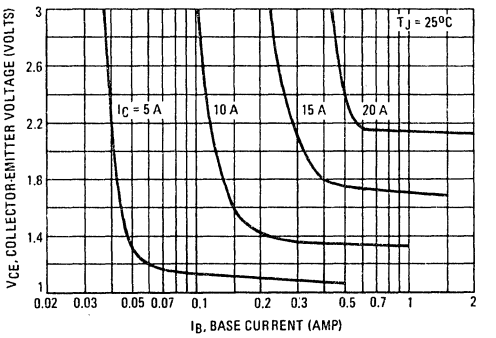


FIGURE 3 – COLLECTOR EMITTER SATURATION VOLTAGES

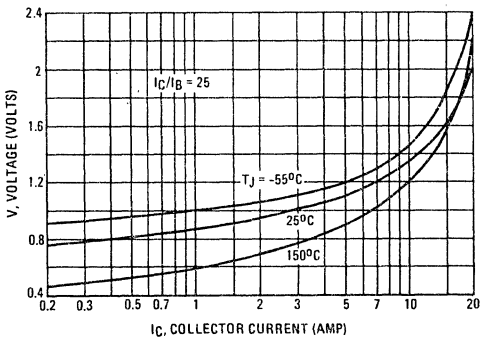


FIGURE 4 – BASE-EMITTER VOLTAGE

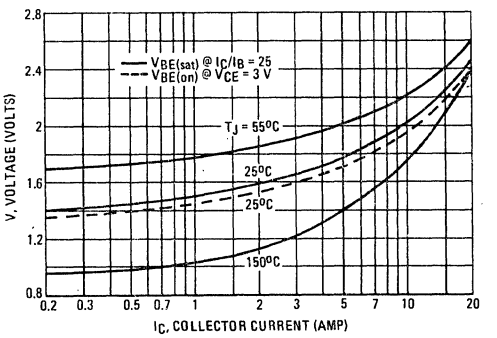


FIGURE 5 – COLLECTOR CUTOFF REGION

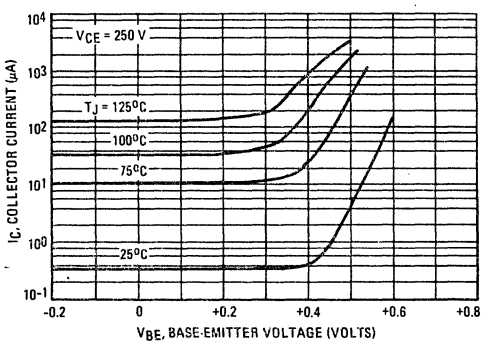


FIGURE 6 – OUTPUT CAPACITANCE

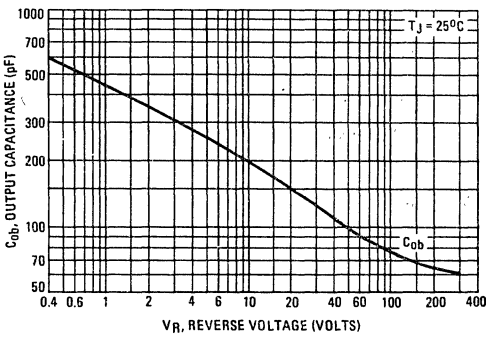


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

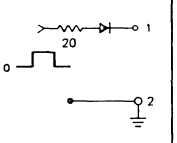
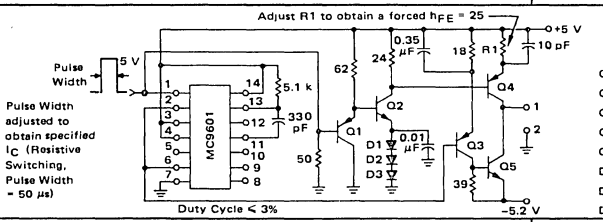
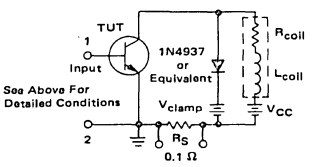
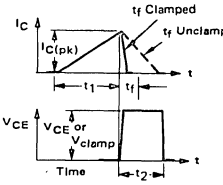
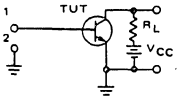
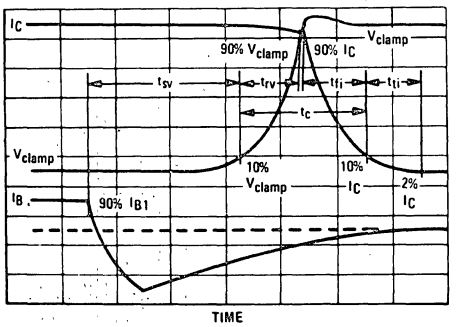
	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 250 mA		Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 25 Ω Pulse Width = 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope-Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

4

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C(t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

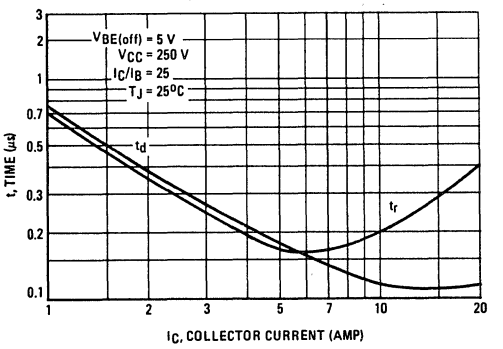


FIGURE 9 – TURN-OFF TIME

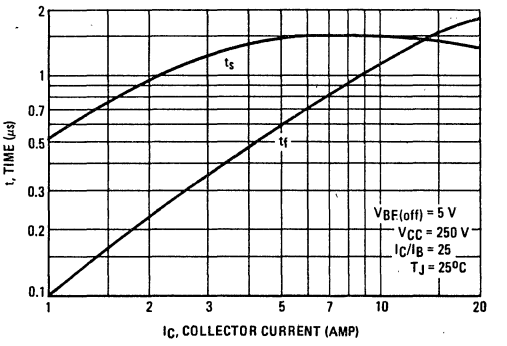
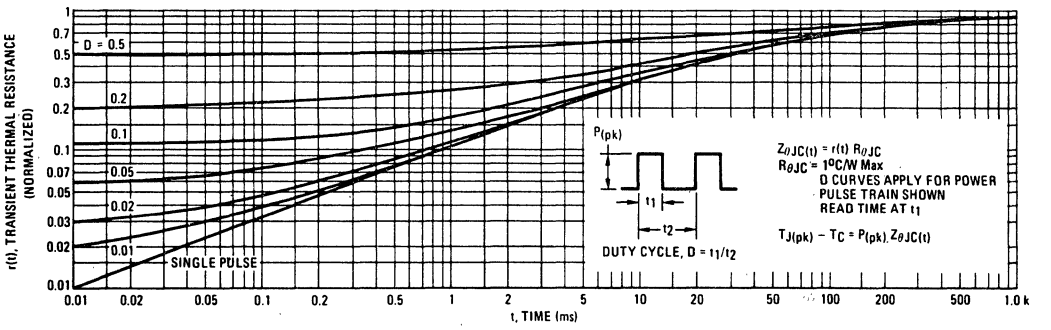


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

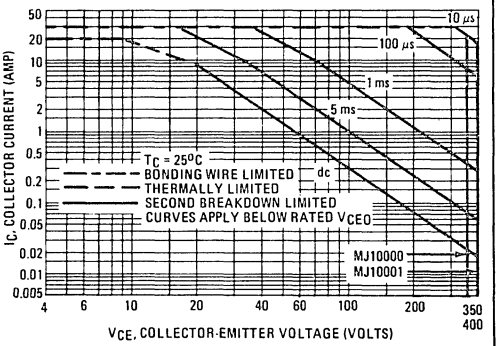
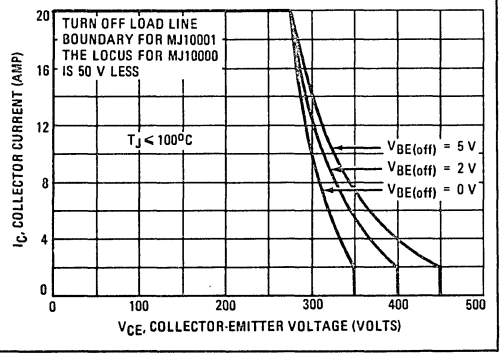


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

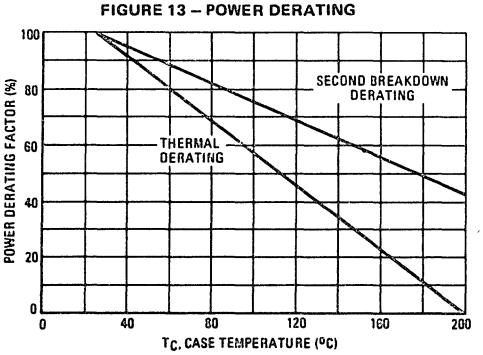
The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

FIGURE 13 – POWER DERATING



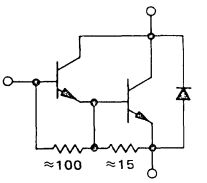
MJ10002
MJ10003

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS

The MJ10002 and MJ10003 darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



100°C Performance Specified for:

Reversed Biased SOA with Inductive Loads

Switching Times with Inductive Loads — 140 ns Inductive Fall Time (Typ)

Saturation Voltages

Leakage Currents

10 AMPERE
NPN SILICON
POWER DARLINGTON TRANSISTORS
350 and 400 VOLTS
150 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

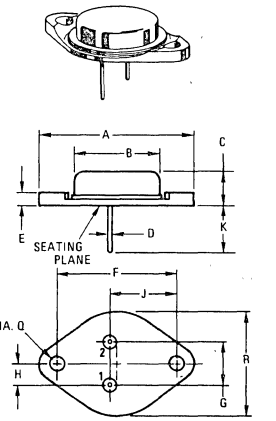
MAXIMUM RATINGS

Rating	Symbol	MJ10002	MJ10003	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 20		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.5 5		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	150 100 0.86		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (2)						
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$				Vdc
(I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO})	MJ10002		350	–	–	
	MJ10003		400	–	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12)		$V_{CEX(sus)}$				Vdc
(I_C = 1 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	MJ10002		400	–	–	
	MJ10003		450	–	–	
(I_C = 5 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	MJ10002		275	–	–	
	MJ10003		325	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	–	5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	5	mAdc
Emitter Cutoff Current (V_{EB} = 8 Vdc, I_C = 0)		I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 11			Adc
ON CHARACTERISTICS (2)						
DC Current Gain		h_{FE}				–
(I_C = 2.5 Adc, V_{CE} = 5 Vdc)			40	–	500	
(I_C = 5 Adc, V_{CE} = 5 Vdc)			30	–	300	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 250 mAdc)			–	–	1.9	
(I_C = 10 Adc, I_B = 1 Adc)			–	–	2.9	
(I_C = 5 Adc, I_B = 250 mAdc, T_C = 100°C)			–	–	2	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 250 mAdc)			–	–	2.5	
(I_C = 5 Adc, I_B = 250 mAdc, T_C = 100°C)			–	–	2.5	
Diode Forward Voltage (1) (I_F = 5.0 Adc)		V_f	–	3	5	Vdc
DYNAMIC CHARACTERISTICS						
Small-Signal Current Gain (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		$\lvert h_{fe} \rvert$	10	–	–	–
Output Capacitance (V_{CB} = 50 Vdc, I_E = 0, f_{test} = 100 kHz)		C_{ob}	60	–	275	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 5 A, I_{B1} = 250 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%).	t_d	–	0.05	0.2	μs
Rise Time		t_r	–	0.25	0.6	μs
Storage Time		t_s	–	1.2	3.0	μs
Fall Time		t_f	–	0.6	1.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 5 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	2.1	5	μs
Crossover Time		t_c	–	1.3	3.3	μs
Storage Time	(I_C = 5 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	–	0.92	–	μs
Crossover Time		t_c	–	0.5	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

4

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

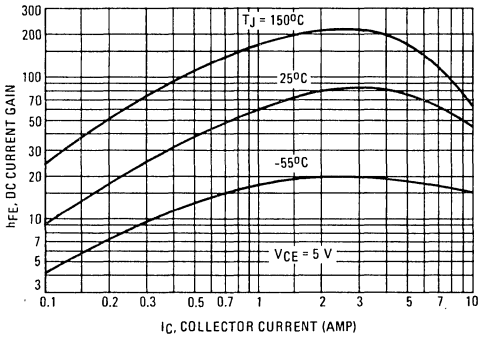


FIGURE 2 – COLLECTOR SATURATION REGION

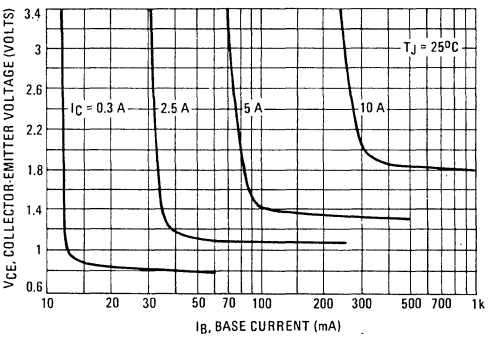


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

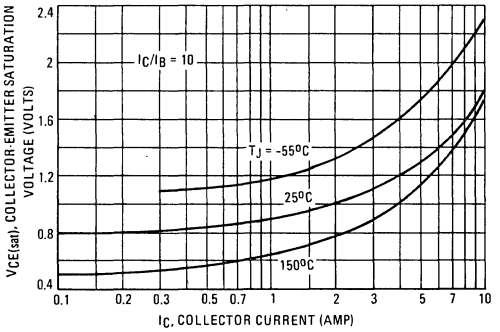


FIGURE 4 – BASE-EMITTER VOLTAGE

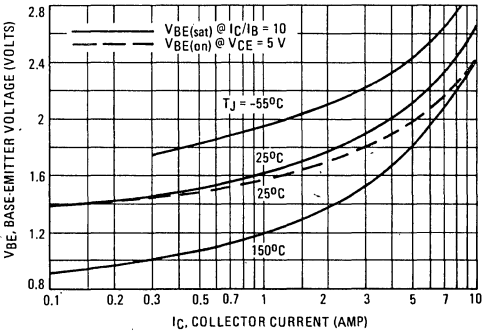


FIGURE 5 – COLLECTOR CUT-OFF REGION

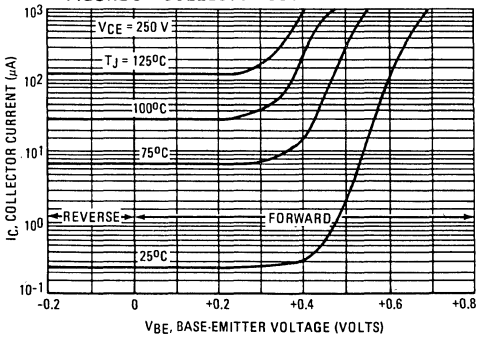


FIGURE 6 – OUTPUT CAPACITANCE

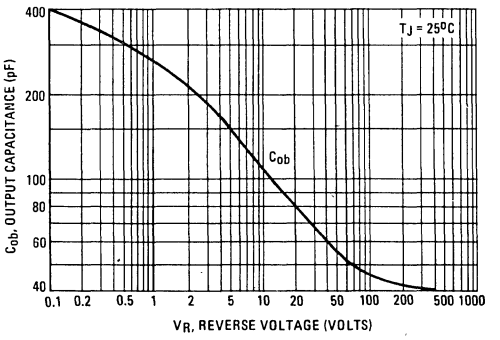


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	PW Varied to Attain I_C = 250 mA	Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 50 μs)	Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 50 Ω Pulse Width = 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT OUTPUT WAVEFORMS		RESISTIVE TEST CIRCUIT

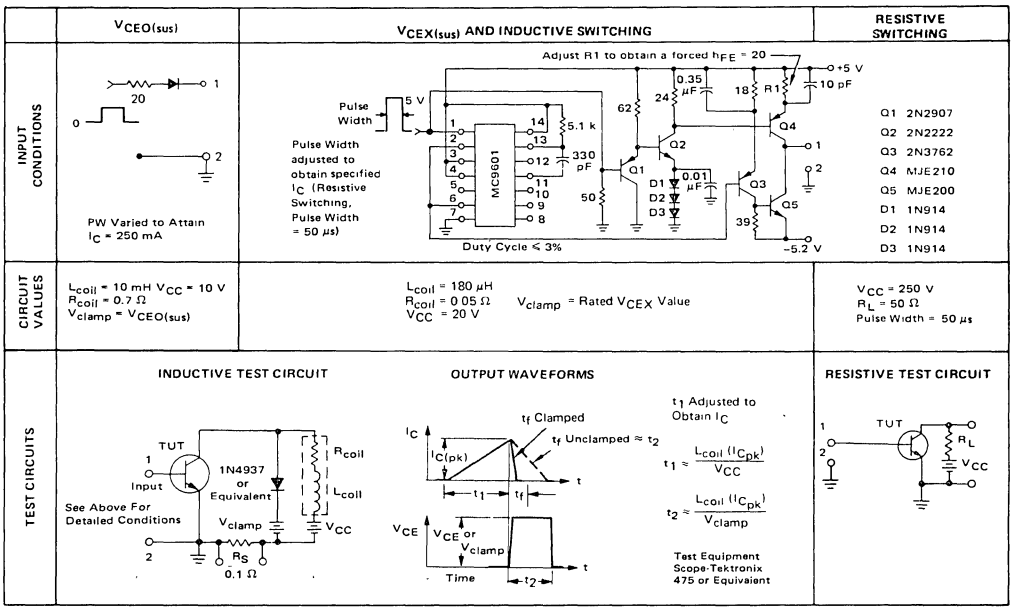
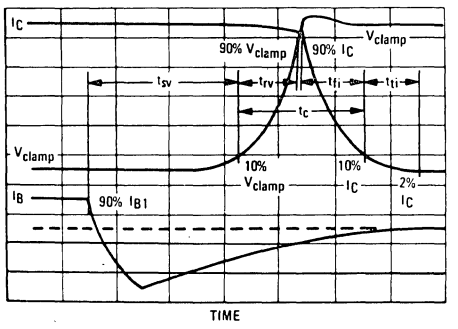


FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

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t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

4

SWITCHING TIME NOTES (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C(t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

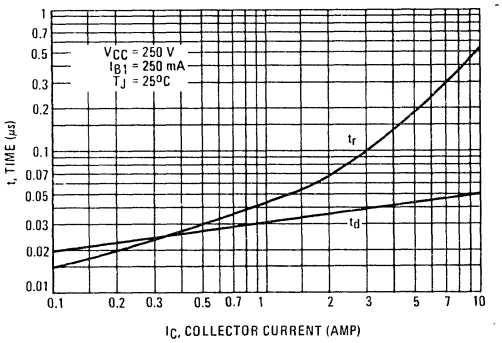


FIGURE 9 – TURN-OFF TIME

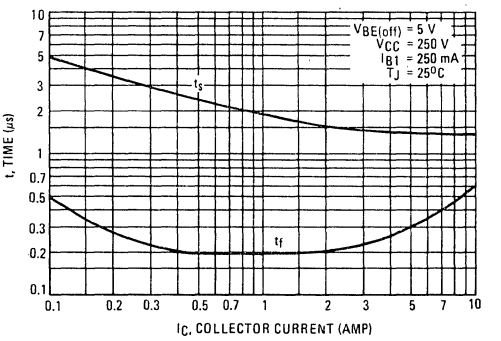
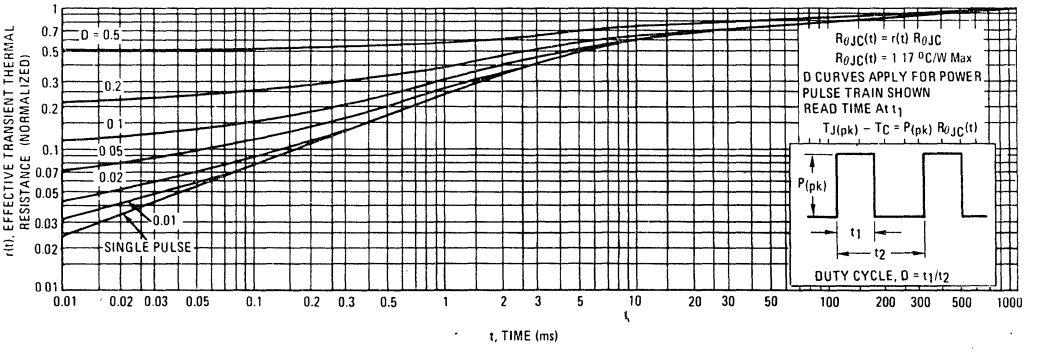


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – ACTIVE-REGION SAFE OPERATING AREA

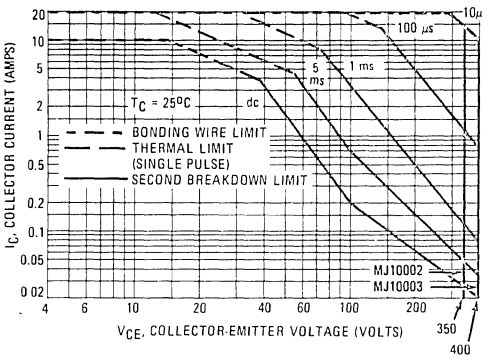
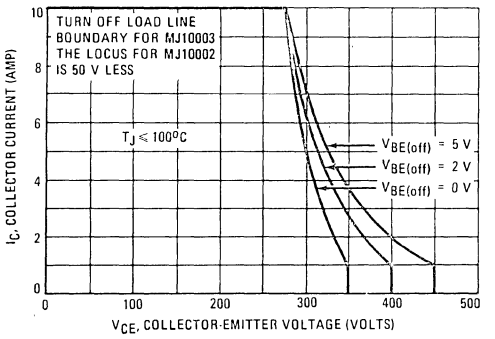


FIGURE 12 – REVERSE BIASED SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

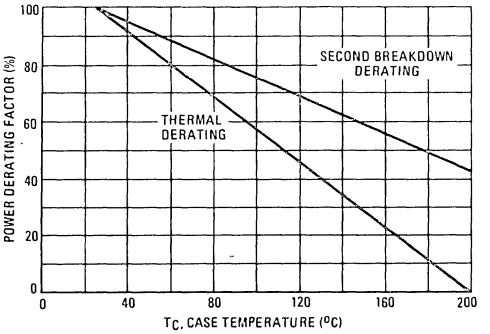
The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

FIGURE 13 – POWER DERATING



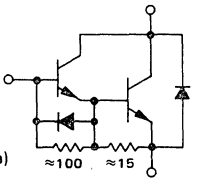
MJ10004
MJ10005

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The MJ10004 and MJ10005 darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
- 40 ns Inductive Fall Time – 25°C (Typ)
- 650 ns Inductive Storage Time – 25°C (Typ)

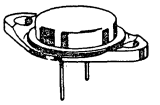
Operating Temperature Range -65 to +200°C

100°C Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

20 AMPERE
NPN SILICON
POWER DARLINGTON TRANSISTORS
350 and 400 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



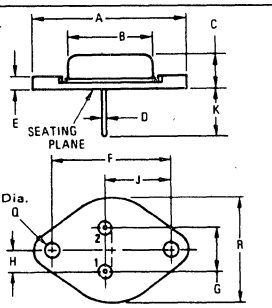
MAXIMUM RATINGS

Rating	Symbol	MJ10004	MJ10005	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	20 30		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	2.5 5		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%



PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$				Vdc
(I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO})	MJ10004		350	–	–	
	MJ10005		400	–	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12)		$V_{CEX(sus)}$				Vdc
(I_C = 2 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	MJ10004		400	–	–	
	MJ10005		450	–	–	
(I_C = 10 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	MJ10004		275	–	–	
	MJ10005		325	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	–	5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	5	mAdc
Emitter Cutoff Current (V_{EB} = 2 Vdc, I_C = 0)		I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 11			
ON CHARACTERISTICS (2)						
DC Current Gain		h_{FE}				–
(I_C = 5 Adc, V_{CE} = 5 Vdc)			50	–	600	
(I_C = 10 Adc, V_{CE} = 5 Vdc)			40	–	400	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 400 mAdc)			–	–	1.9	
(I_C = 20 Adc, I_B = 2 Adc)			–	–	3	
(I_C = 10 Adc, I_B = 400 mAdc, T_C = 100°C)			–	–	2	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 400 mAdc)			–	–	2.5	
(I_C = 10 Adc, I_B = 400 mAdc, T_C = 100°C)			–	–	2.5	
Diode Forward Voltage (1) (I_F = 10 Adc)		V_f	–	3	5	Vdc
DYNAMIC CHARACTERISTICS						
Small-Signal Current Gain (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		$\lvert h_{fe} \rvert$	10	–	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)		C_{ob}	100	–	325	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%).	t_d	–	0.12	0.2	μs
Rise Time		t_r	–	0.2	0.6	μs
Storage Time		t_s	–	0.6	1.5	μs
Fall Time		t_f	–	0.15	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	1.0	2.5	μs
Crossover Time		t_c	–	0.4	1.5	μs
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	–	0.65	–	μs
Crossover Time		t_c	–	0.2	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

4

TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

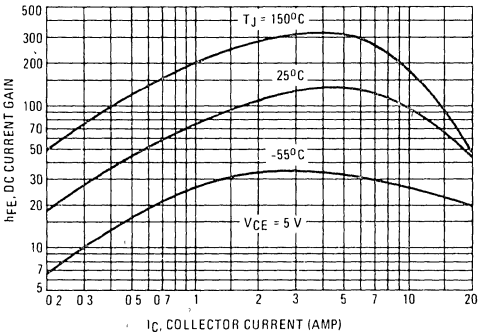


FIGURE 2 – COLLECTOR SATURATION REGION

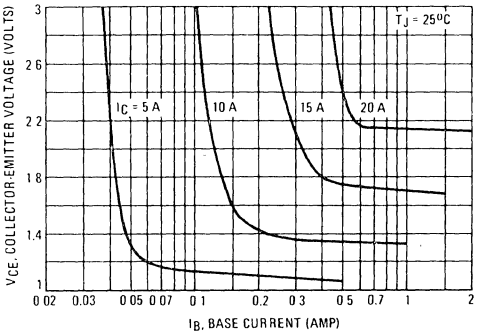


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

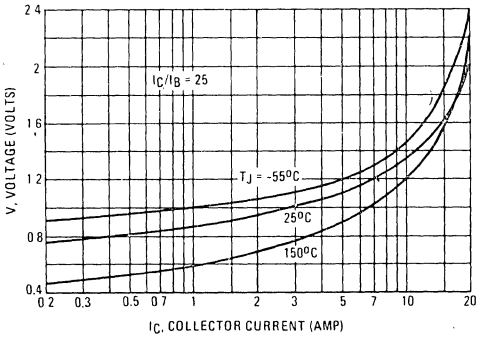


FIGURE 4 – BASE-EMITTER VOLTAGE

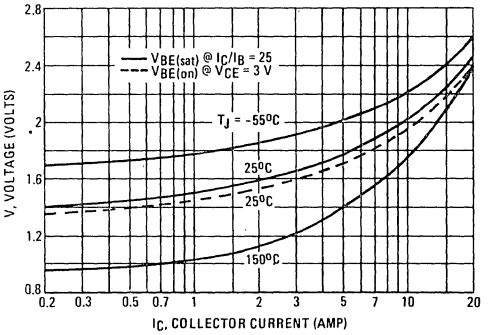


FIGURE 5 – COLLECTOR CUTOFF REGION

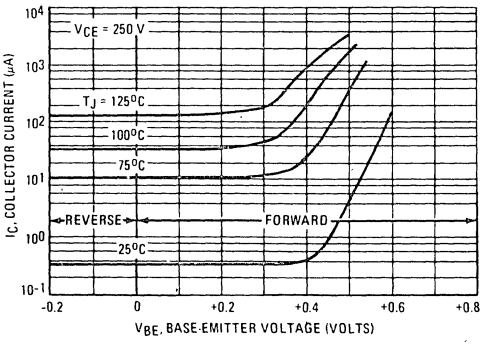


FIGURE 6 – OUTPUT CAPACITANCE

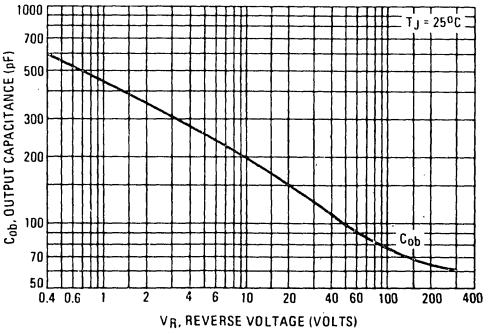
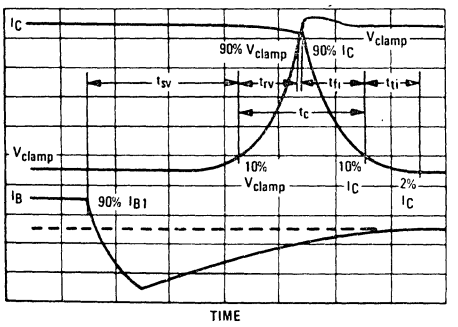


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	PW Varied to Attain I_C = 250 mA	Adjust R1 to obtain a forced h_{FE} = 25; Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 50 μs); Duty Cycle ≤ 3%	Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 25 Ω Pulse Width = 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT See Above For Detailed Conditions	OUTPUT WAVEFORMS t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

4

TYPICAL CHARACTERISTICS

SWITCHING TIME NOTES (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

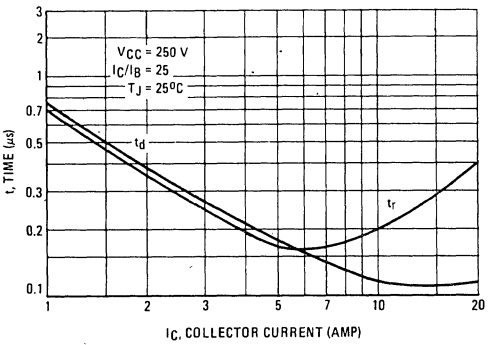


FIGURE 9 – TURN-OFF TIME

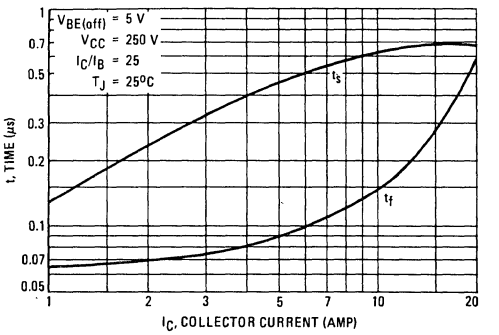
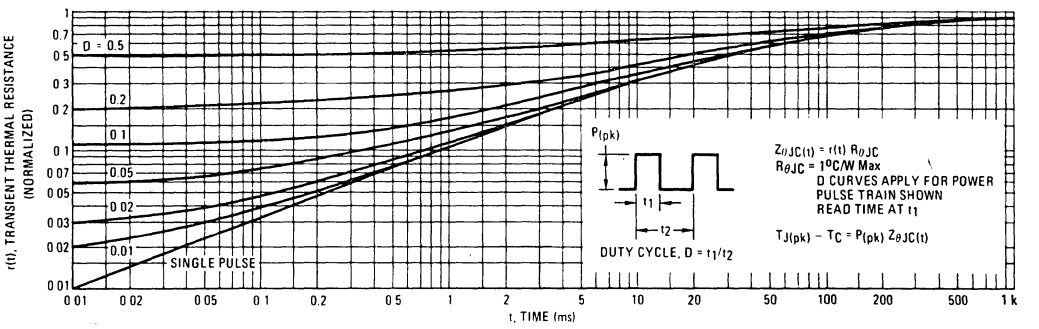


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

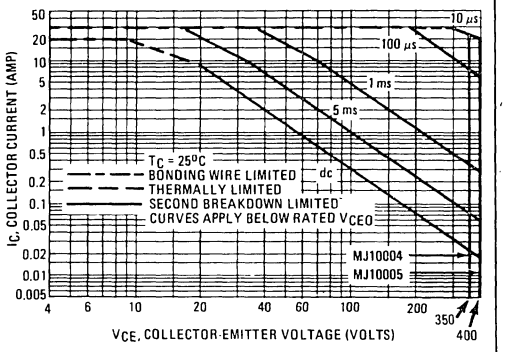
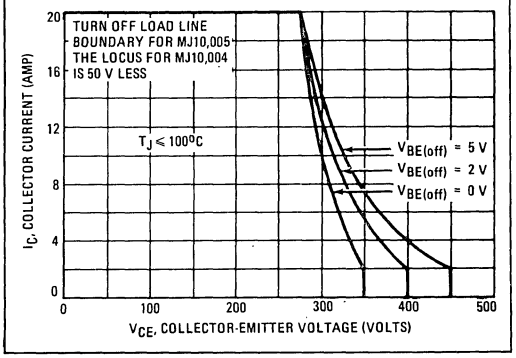


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

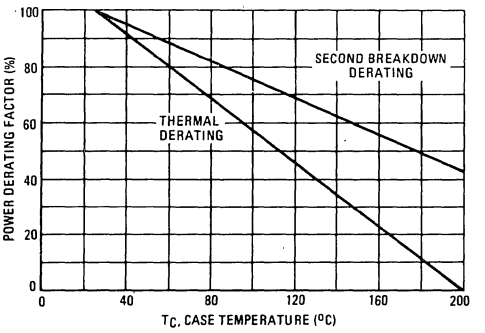
The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

FIGURE 13 – POWER DERATING



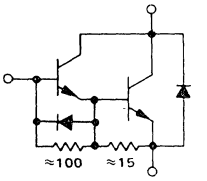
MJ10006
MJ10007

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The MJ10006 and MJ10007 darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
30 ns Inductive Fall Time – 25°C (Typ)
500 ns Inductive Storage Time – 25°C (Typ))
Operating Temperature Range -65 to +200°C
100°C Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents

10 AMPERE
NPN SILICON
POWER DARLINGTON TRANSISTORS
350 and 400 VOLTS
150 WATTS

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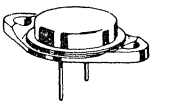


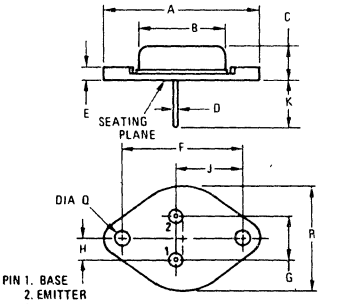
MAXIMUM RATINGS

Rating	Symbol	MJ10006	MJ10007	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	10 20		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	2.5 5		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	150 100 0.86		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1)	$V_{CEO(sus)}$				Vdc
(I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO}) MJ10006		350	–	–	
MJ10007		400	–	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12)	$V_{CEX(sus)}$				Vdc
(I_C = 1 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) MJ10006		400	–	–	
MJ10007		450	–	–	
(I_C = 5 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) MJ10006		275	–	–	
MJ10007		325	–	–	
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		–	–	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		–	–	5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	–	5	mAdc
Emitter Cutoff Current (V_{EB} = 2 Vdc, I_C = 0)	I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 11			
ON CHARACTERISTICS (2)					
DC Current Gain	h_{FE}				–
(I_C = 2.5 Adc, V_{CE} = 5 Vdc)		40	–	500	
(I_C = 5 Adc, V_{CE} = 5 Vdc)		30	–	300	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 250 mAdc)		–	–	1.9	
(I_C = 10 Adc, I_B = 1 Adc)		–	–	2.9	
(I_C = 5 Adc, I_B = 250 mAdc, T_C = 100°C)		–	–	2	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 250 mAdc)		–	–	2.5	
(I_C = 5 Adc, I_B = 250 mAdc, T_C = 100°C)		–	–	2.5	
Diode Forward Voltage (1) (I_F = 5 Adc)	V_f	–	3	5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	$\lvert h_{fe} \rvert$	10	–	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	60	–	275	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	t_d	–	0.05	0.2	μs
Rise Time	t_r	–	0.25	0.6	μs
Storage Time	t_s	–	0.5	1.5	μs
Fall Time	t_f	–	0.06	0.5	μs
Inductive Load, Clamped (Table 1)					
Storage Time	t_{sv}	–	0.8	2.0	μs
Crossover Time	t_c	–	0.6	1.5	μs
Storage Time	t_{sv}	–	0.5	–	μs
Crossover Time	t_c	–	0.3	–	μs

(V_{CC} = 250 Vdc, I_C = 5 A, I_{B1} = 250 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%).

(I_C = 5 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)

(I_C = 5 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

4

TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

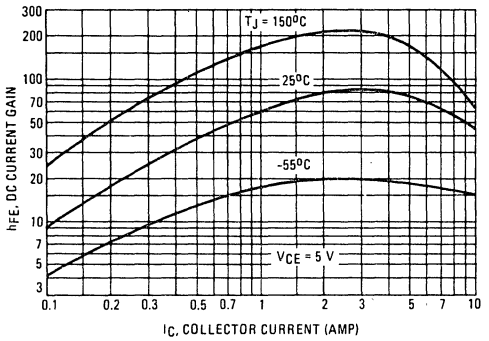


FIGURE 2 – COLLECTOR SATURATION REGION

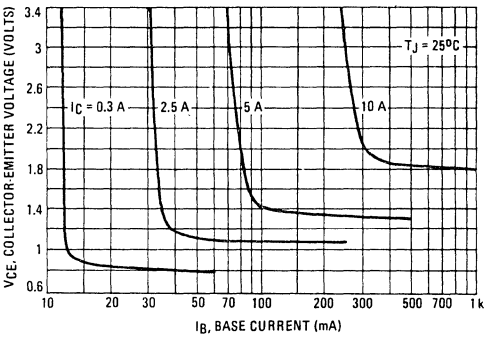


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

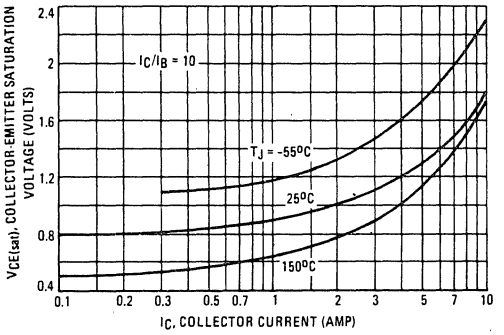


FIGURE 4 – BASE-EMITTER VOLTAGE

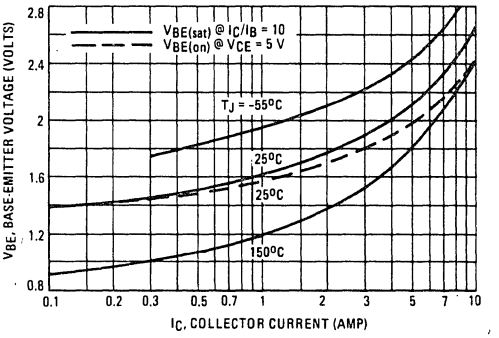


FIGURE 5 – COLLECTOR CUTOFF REGION

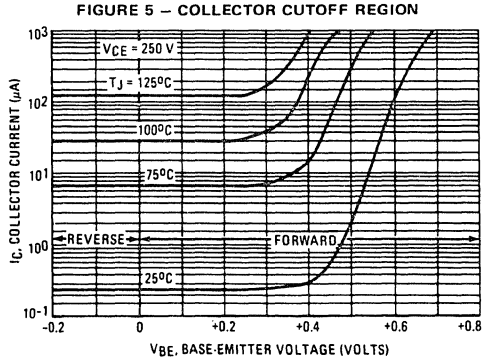


FIGURE 6 – OUTPUT CAPACITANCE

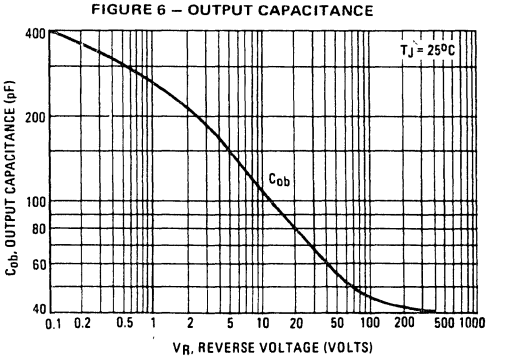


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

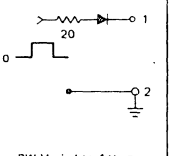
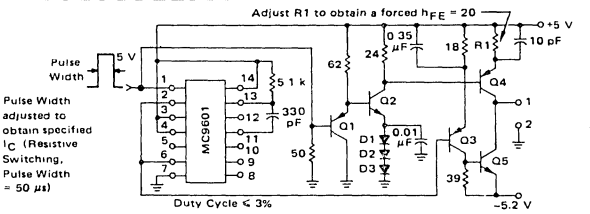
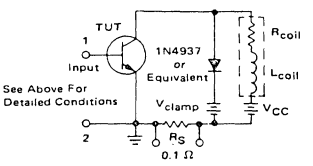
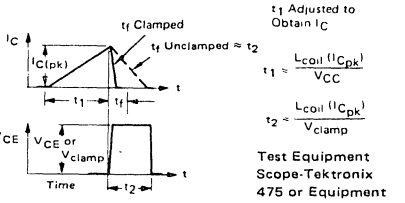
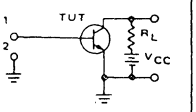
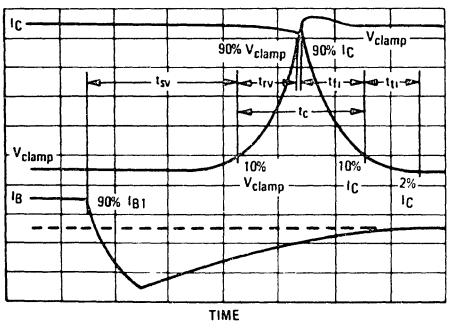
	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 250 mA		Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V f_o = 500 kHz V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 50 Ω Pulse Width = 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  See Above For Detailed Conditions	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope-Tektronix 475 or Equipment	RESISTIVE TEST CIRCUIT 

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

4

TYPICAL CHARACTERISTICS

SWITCHING TIME NOTES (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C(t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

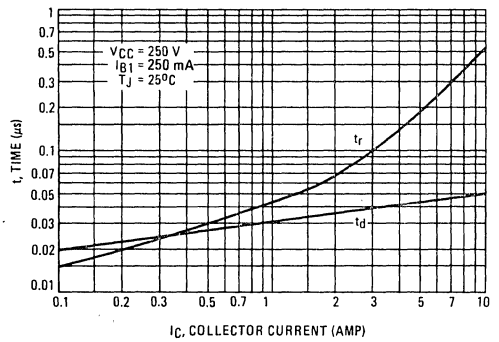


FIGURE 9 – TURN-OFF TIME

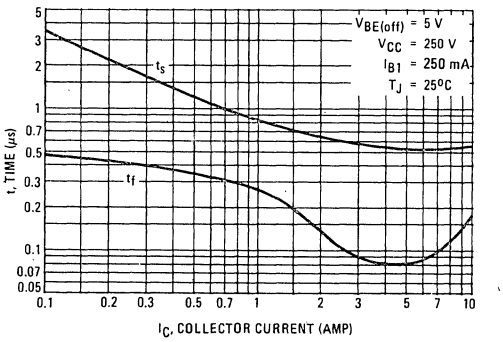
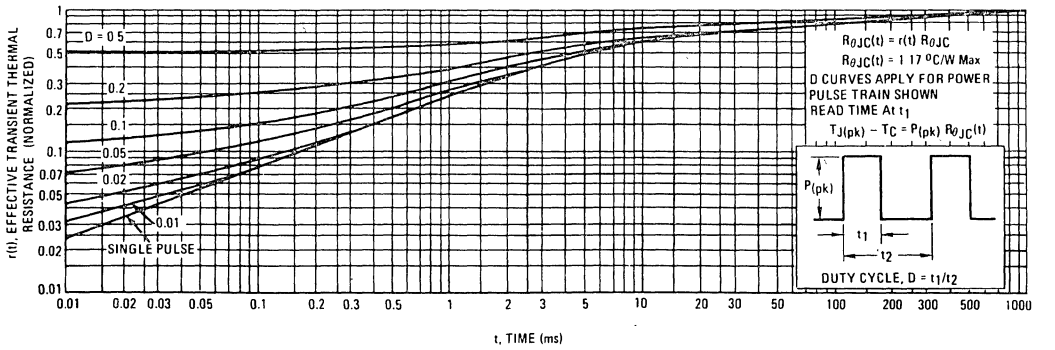


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

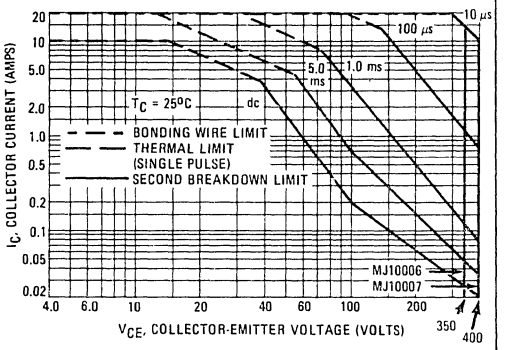
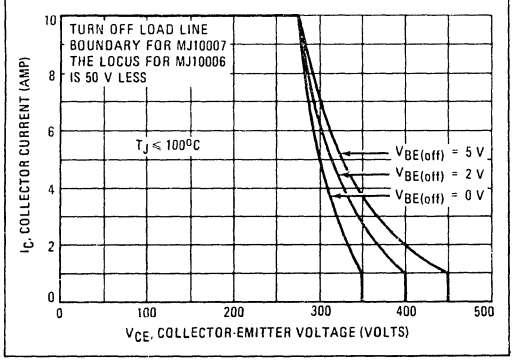


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

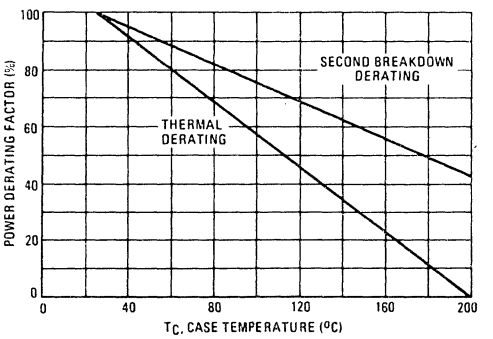
The data of Figure 11 is based on T_C = 25°C, $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

FIGURE 13 – POWER DERATING



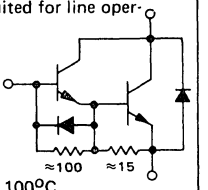
MJ10008
MJ10009

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The MJ10008 and MJ10009 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times

1.6 μs (max) Inductive Crossover Time – 10 A, 100°C

3.5 μs (max) Inductive Storage Time – 10 A, 100°C

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:

Reversed Biased SOA with Inductive Loads

Switching Times with Inductive Loads

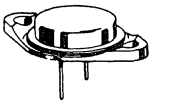
Saturation Voltages

Leakage Currents

20 AMPERE
NPN SILICON
POWER DARLINGTON TRANSISTORS
450 and 500 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



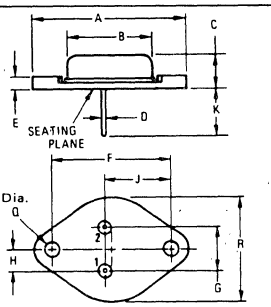
MAXIMUM RATINGS

Rating	Symbol	MJ10008	MJ10009	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	500	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	450	500	Vdc
Collector-Emitter Voltage	V_{CEV}	650	700	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	20 30		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	2.5 5		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



PIN 1 BASE
2 EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case
CASE 11-01
TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$				Vdc
(I_C = 100 mA, I_B = 0, V_{clamp} = Rated V_{CEO})	MJ10008		450	–	–	
	MJ10009		500	–	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12)		$V_{CEX(sus)}$				Vdc
(I_C = 2 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C,	MJ10008		450	–	–	
$V_{BE(off)}$ = 5 V)	MJ10009		500	–	–	
(I_C = 10 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C,	MJ10008		325	–	–	
$V_{BE(off)}$ = 5 V)	MJ10009		375	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	–	5	
Collector Cutoff Current		I_{CER}	–	–	5	mAdc
(V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)						
Emitter Cutoff Current		I_{EBO}	–	–	175	mAdc
(V_{EB} = 2 Vdc, I_C = 0)						
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 11			
ON CHARACTERISTICS (2)						
DC Current Gain		h_{FE}				–
(I_C = 5 Adc, V_{CE} = 5 Vdc)			40	–	400	
(I_C = 10 Adc, V_{CE} = 5 Vdc)			30	–	300	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 500 mAdc)			–	–	2	
(I_C = 20 Adc, I_B = 2 Adc)			–	–	3.5	
(I_C = 10 Adc, I_B = 500 mAdc, T_C = 100°C)			–	–	2.5	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 500 mAdc)			–	–	2.5	
(I_C = 10 Adc, I_B = 500 mAdc, T_C = 100°C)			–	–	2.5	
Diode Forward Voltage (1)		V_f	–	3	5	Vdc
(I_F = 10 Adc)						
DYNAMIC CHARACTERISTICS						
Small-Signal Current Gain		$\|h_{fe}\|$	8	–	–	–
(I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)						
Output Capacitance		C_{ob}	100	–	325	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)						
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 500 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 25 μs Duty Cycle ≤ 2%).	t_d	–	0.12	0.25	μs
Rise Time		t_r	–	0.5	1.5	μs
Storage Time		t_s	–	0.8	2.0	μs
Fall Time		t_f	–	0.2	0.6	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 10 A(pk), V_{clamp} = 250 V, I_{B1} = 500 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	1.5	3.5	μs
Crossover Time		t_c	–	0.36	1.6	μs
Storage Time	(I_C = 10 A(pk), V_{clamp} = 250 V, I_{B1} = 500 mA, $V_{BE(off)}$ = 5 Vdc)	t_{sv}	–	0.8	–	μs
Crossover Time		t_c	–	0.18	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

4

TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

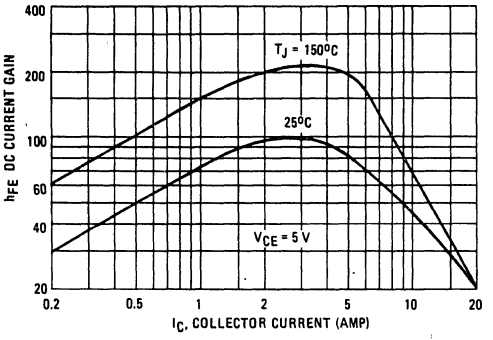


FIGURE 2 – COLLECTOR SATURATION REGION

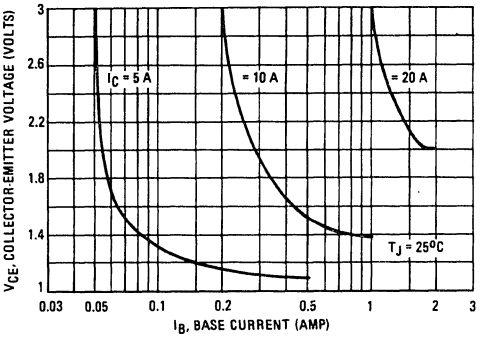


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

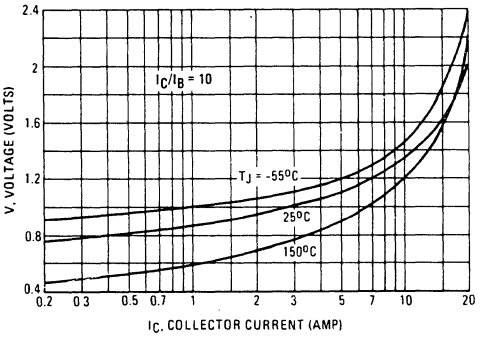


FIGURE 4 – BASE-EMITTER VOLTAGE

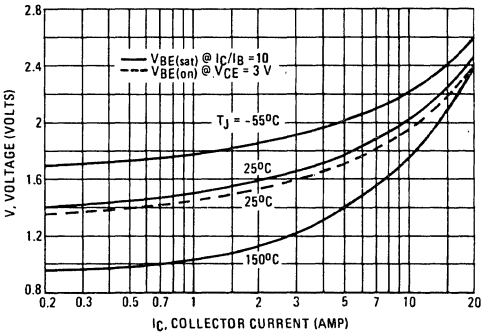


FIGURE 5 – COLLECTOR CUTOFF REGION

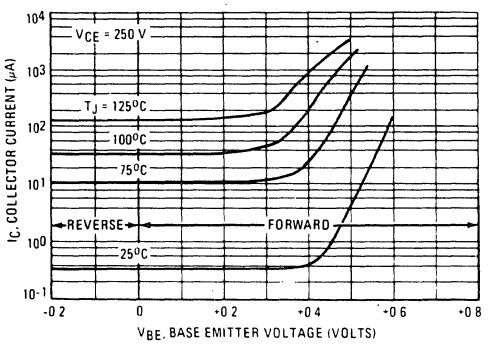


FIGURE 6 – OUTPUT CAPACITANCE

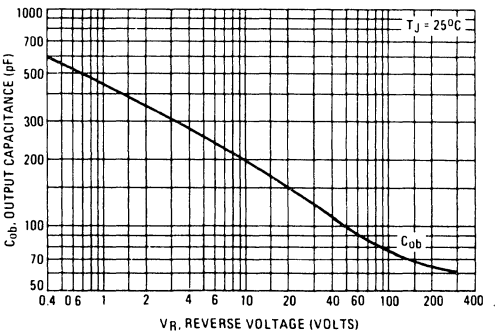
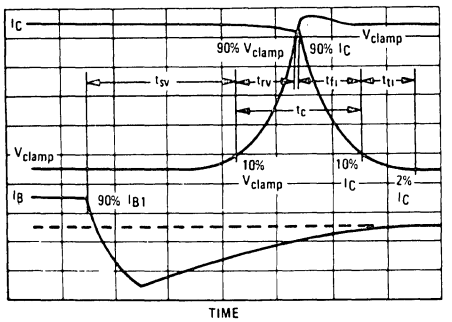


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	PW Varied to Attain I_C = 100 mA	Adjust R1 to obtain a forced h_{FE} = 20; Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 25 μs); Duty Cycle ≤ 3%	TURN-ON TIME: I_{B1} adjusted to obtain the forced h_{FE} desired. TURN-OFF TIME: Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V; R_{coil} = 0.7 Ω; V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH; R_{coil} = 0.05 Ω; V_{CC} = 20 V; V_{clamp} = 250V	V_{CC} = 250 V; R_L = 25 Ω; Pulse Width = 25 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT: TUT, 1N4937 or Equivalent, R_{coil}, L_{coil}, V_{clamp}, V_{CC}, R_S 0.1 Ω; See Above For Detailed Conditions	OUTPUT WAVEFORMS: t_f Clamped, t_f Unclamped ≈ t_2; t_1 Adjusted to Obtain I_C; $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$; $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$; Test Equipment: Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT: TUT, R_L, V_{CC}

*Adjust –V such that $V_{BE(off)}$ = 5 V except as required for RB SOA (Figure 12).

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

– continued –

4

TYPICAL CHARACTERISTICS

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 7. In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at $T_C = 25^oC$ and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at $T_C = 100^oC$.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

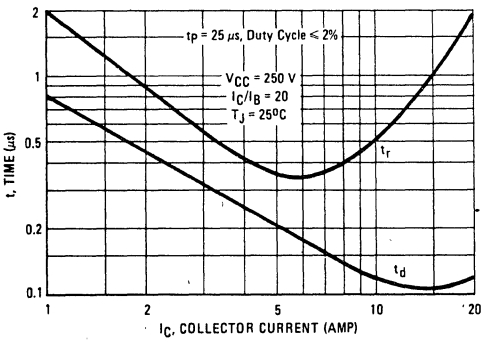


FIGURE 9 – TURN-OFF TIME

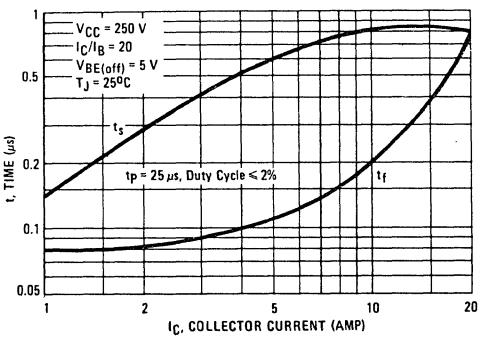
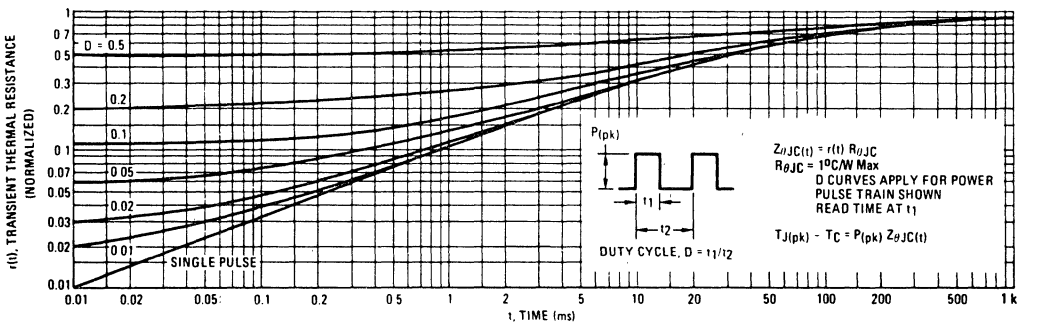


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

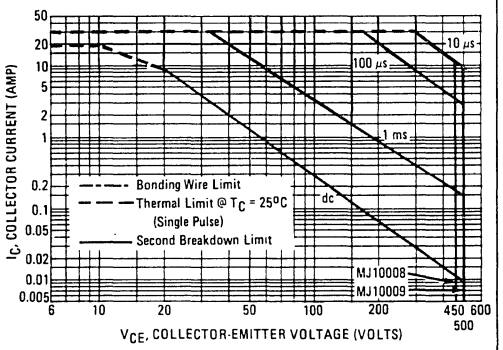
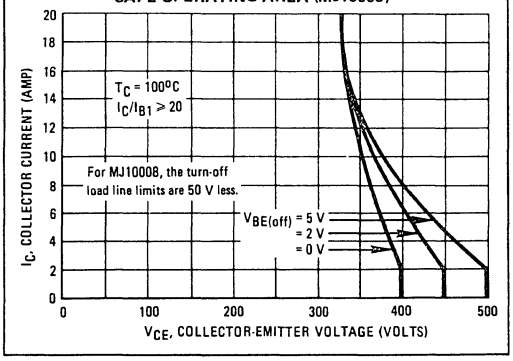


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA (MJ10009)



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics. See Table 1 for circuit conditions.

FIGURE 13 – POWER DERATING

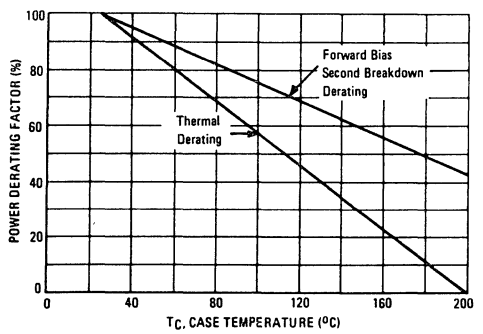
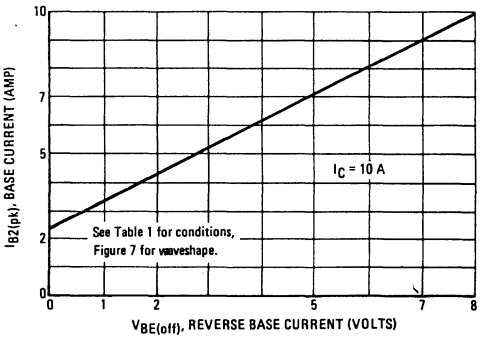


FIGURE 14 – REVERSE BASE CURRENT versus $V_{BE(off)}$ WITH NO EXTERNAL BASE RESISTANCE



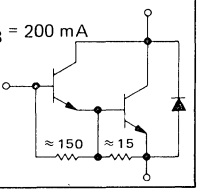
MJ10011

Advance Information

DARLINGTON HORIZONTAL DEFLECTION TRANSISTOR

. . . specifically designed for use in deflection circuits.

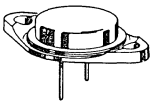
- $V_{CE(sat)}$ = 3.0 Volts (Max) @ I_C = 4.0 Amps, I_B = 200 mA
- Built-In Damper Diode
- V_{CEX} = 1400 Volts
- Glassivated Base-Collector Junction
- Safe Operating Area @ 50 μs = 25 A, 200 V



8 AMPERE

NPN SILICON DARLINGTON POWER TRANSISTOR

1400 VOLTS
80 WATTS



MAXIMUM RATINGS

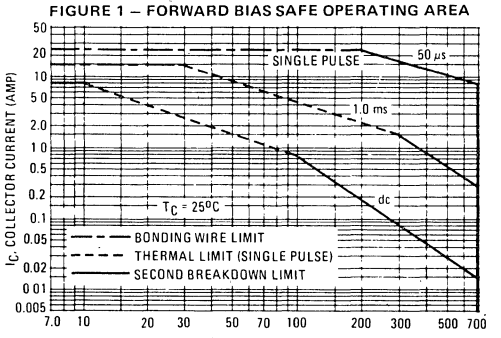
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEX}	1400	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	8.0 16	Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	2.0 4.0	Adc
Emitter Current — Continuous Peak (1)	I_E I_{EM}	10 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.6	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

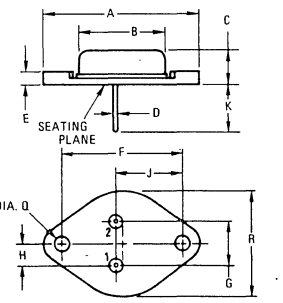
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Maximum Lead Temperature for Soldering Purposes: 1.8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 1 ms, Duty Cycle ≤ 10%.

FIGURE 1 — FORWARD BIAS SAFE OPERATING AREA





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

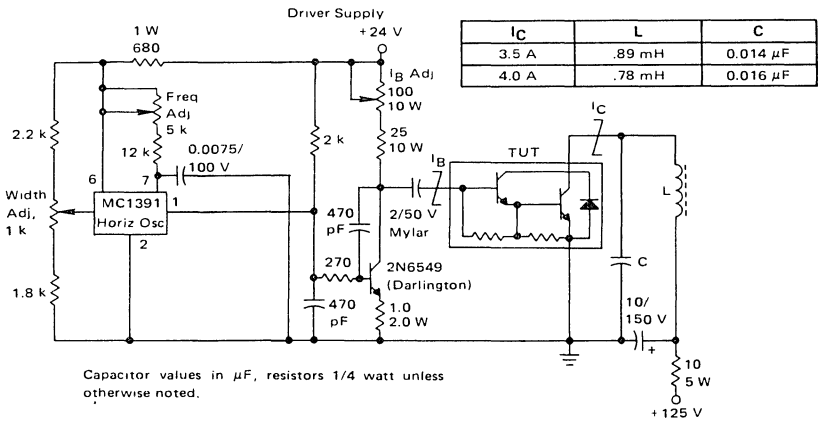
CASE 11-01
TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	700	–	–	Vdc
Collector Cutoff Current (V_{CE} = 1400 Vdc, V_{BE} = 0)	I_{CES}	–	–	0.25	mAdc
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	–	50	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 3.5 Adc, I_B = 0.15 Adc)		–	–	3.0	
(I_C = 4.0 Adc, I_B = 0.2 Adc)		–	–	3.0	
Base Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 3.5 Adc, I_B = 0.15 Adc)		–	–	2.0	
(I_C = 4.0 Adc, I_B = 0.2 Adc)		–	–	2.0	
Forward Diode Voltage (I_F = 4.0 Adc)	V_f	–	1.2	2.0	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 1			
SWITCHING CHARACTERISTICS					
Fall Time (See Figure 2) (I_C = 4.0 Adc, I_{B1} = 0.2 Adc)	t_f	–	0.65	1.0	μs

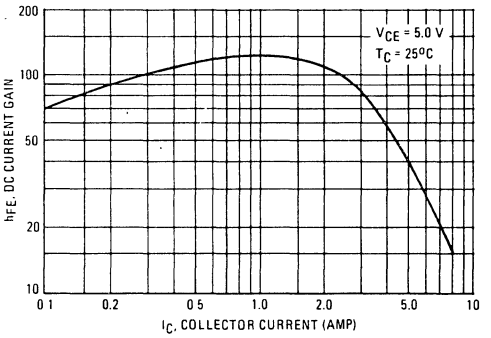
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

FIGURE 2 – FALL TIME TEST CIRCUIT



I_C	L	C
3.5 A	.89 mH	0.014 μF
4.0 A	.78 mH	0.016 μF

FIGURE 3 – DC CURRENT GAIN

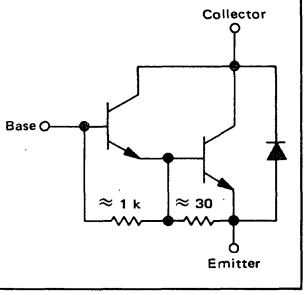


MJ10012

NPN SILICON POWER DARLINGTON TRANSISTOR

The MJ10012 is a high-voltage, high-current darlington transistor designed for automotive ignition, switching regulator and motor control applications.

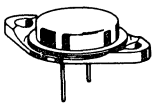
- Collector-Emitter Sustaining Voltage – $V_{CEO(sus)}$ = 400 Vdc (Min)
- 175 Watts Capability at 50 Volts
- Automotive Functional Tests



15 AMPERE PEAK

POWER TRANSISTOR DARLINGTON NPN SILICON

400 VOLTS
175 WATTS



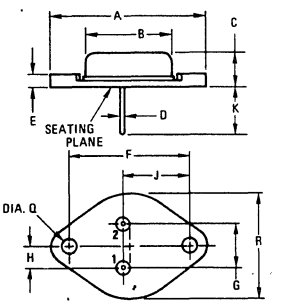
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Emitter Voltage (R_{BE} = 27 Ω)	V_{CER}	550	Vdc
Collector-Base Voltage	V_{CBO}	600	Vdc
Emitter-Base Voltage	V_{EBO}	8	Vdc
Collector Current – Continuous – Peak (1)	I_C	10 15	Adc
Base Current	I_B	2	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1	Watts Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-01
TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Figure 1) (I_C = 200 mAdc, I_B = 0, V_{clamp} = Rated V_{CEO})	$V_{CEO(sus)}$	400	–	–	Vdc
Collector-Emitter Sustaining Voltage (Figure 1) (I_C = 200 mAdc, R_{BE} = 27 Ohms, V_{clamp} = Rated V_{CER})	$V_{CER(sus)}$	425	–	–	Vdc
Collector Cutoff Current (Rated V_{CER}, R_{BE} = 27 Ohms)	I_{CER}	–	–	1	mAdc
Collector Cutoff Current (Rated V_{CBO}, I_E = 0)	I_{CBO}	–	–	1	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)	I_{EBO}	–	–	40	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 3 Adc, V_{CE} = 6 Vdc) (I_C = 6 Adc, V_{CE} = 6 Vdc) (I_C = 10 Adc, V_{CE} = 6 Vdc)	h_{FE}	 300 100 20	 550- 350 150	 – 4000 –	–
Collector-Emitter Saturation Voltage (I_C = 3 Adc, I_B = 0.3 Adc) (I_C = 6 Adc, I_B = 0.6 Adc) (I_C = 10 Adc, I_B = 2 Adc)	$V_{CE(sat)}$	 – – –	 – – –	 1.5 2 2.5	Vdc
Base-Emitter Saturation Voltage (I_C = 6 Adc, I_B = 0.6 Adc) (I_C = 10 Adc, I_B = 2 Adc)	$V_{BE(sat)}$	 – –	 – –	 2.5 3	Vdc
Base-Emitter On Voltage (I_C = 10 Adc, V_{CE} = 6 Vdc)	$V_{BE(on)}$	–	–	2.8	Vdc
Diode Forward Voltage (I_F = 10 Adc)	V_f	–	2	3.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	–	165	350	pF
SWITCHING CHARACTERISTICS					
Storage Time (V_{CC} = 12 Vdc, I_C = 6 Adc, I_{B1} = I_{B2} = 0.3 Adc) Figure 2	t_s	–	7.5	15	μs
Fall Time	t_f	–	5.2	15	μs
FUNCTIONAL TESTS					
Second Breakdown Collector Current with Base-Forward Biased	$I_{S/B}$	See Figure 10			–
Pulsed Energy Test (See Figure 12)	$\frac{I_C 2_L}{2}$	–	–	180	mJ

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 – SUSTAINING VOLTAGE TEST CIRCUIT

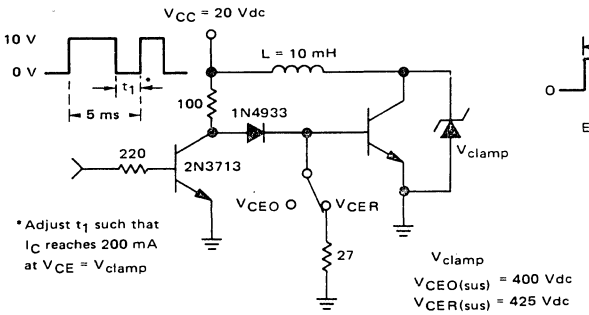


FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

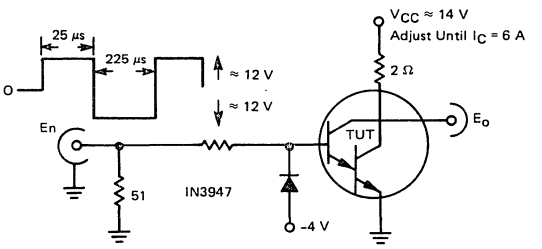


FIGURE 3 – DC CURRENT GAIN

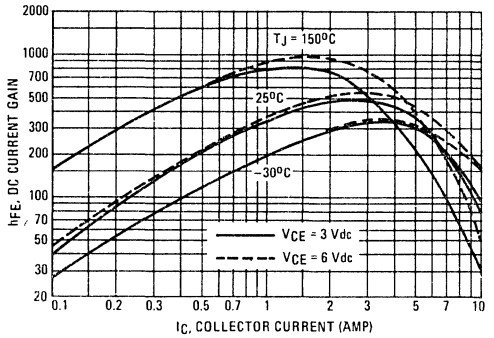


FIGURE 4 – COLLECTOR-SATURATION REGION

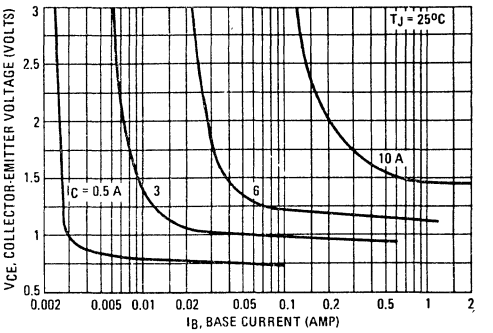


FIGURE 5 – COLLECTOR-EMITTER SATURATION VOLTAGE

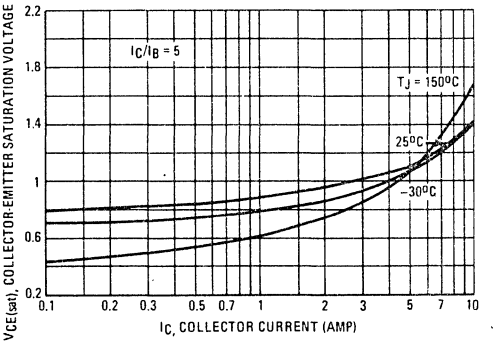


FIGURE 6 – BASE-EMITTER VOLTAGE

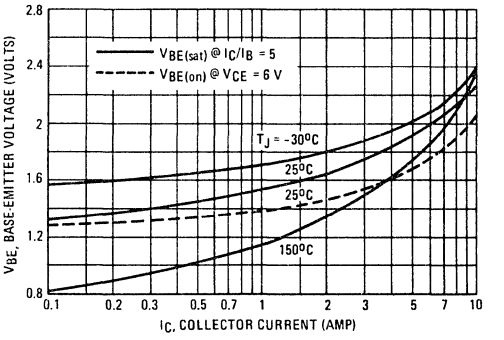


FIGURE 7 – TURN-OFF SWITCHING TIME

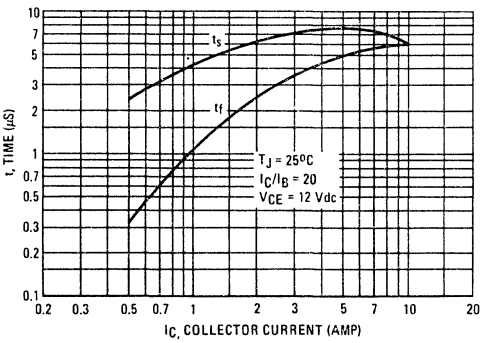


FIGURE 8 – COLLECTOR CUTOFF REGION

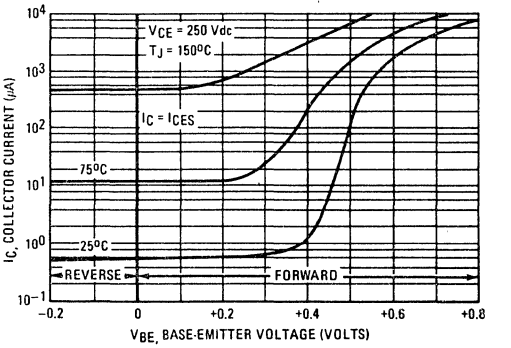


FIGURE 9 – THERMAL RESPONSE

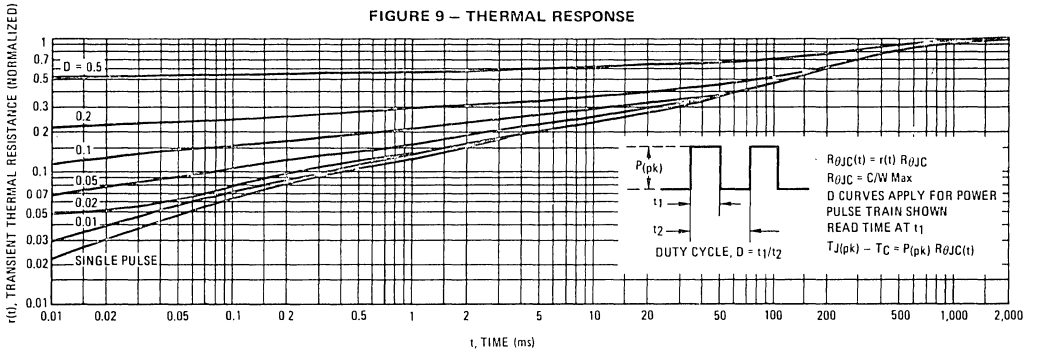
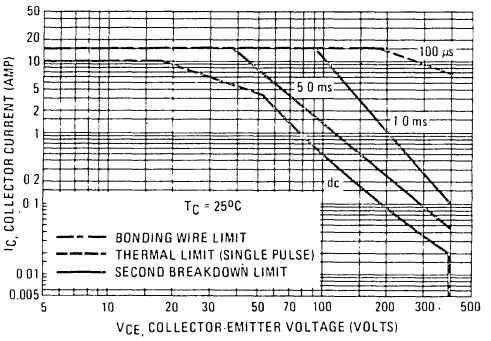


FIGURE 10 – FORWARD BIAS SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 – POWER DERATING

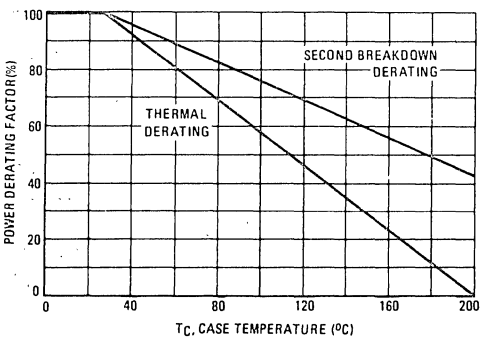
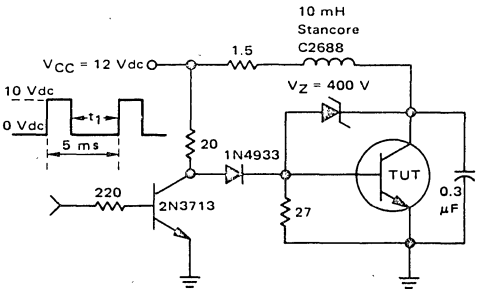


FIGURE 12 – USAGE TEST CIRCUIT



t_1 to be selected such that I_C reaches 6 Adc before switch-off.

NOTE:

"Usage Test," Figure 12 specifies energy handling capabilities in an automotive ignition circuit.

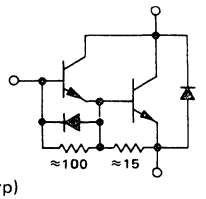
MJ10013
MJ10014

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS

The MJ10013 and MJ10014 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

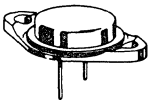


- Fast Turn-Off Times
  - 250 ns Inductive FAll Time–25°C (Typ)
  - 500 ns Inductive Crossover Time–25°C (Typ)
  - 1.4 μs Inductive Storage Time–25°C (Typ)
- Operating Temperature Range: -65 to +200°C
- 100°C Performance Specified for:
  - Reversed Biased SOA With Inductive Loads
  - Switching Times With Inductive Loads
  - Saturation Voltages
  - Leakage Currents

10 AMPERE
NPN SILICON
POWER DARLINGTON TRANSISTORS
550 AND 600 VOLTS
175 WATTS

Designers Data for "Worst-Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristic boundaries—are given to facilitate "worst-case" design.



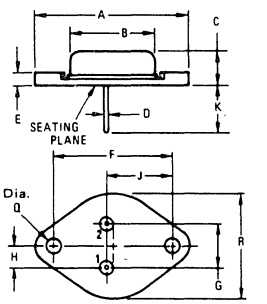
MAXIMUM RATINGS

Rating	Symbol	MJ10013	MJ10014	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	550	600	Vdc
Collector-Emitter Voltage	V_{CEV}	650	700	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	10 15		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	7 10		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%



PIN 1. BASE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case
CASE 11-01
TO-3

Designers and Switchmode are Trademarks of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1)	$V_{CEO(sus)}$				Vdc
(I_C = 100 mA, I_B = 0) MJ10013		550	–	–	
MJ10014		600	–	–	
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		–	–	0.3	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		–	–	5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	–	–	5	mAdc
Emitter Cutoff Current (V_{EB} = 2 Vdc, I_C = 0)	I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (2)					
DC Current Gain	h_{FE}				–
(I_C = 5 Adc, V_{CE} = 5 Vdc)		20	–	500	
(I_C = 10 Adc, V_{CE} = 5 Vdc)		10	–	250	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 2 Adc)		–	–	2.5	
(I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)		–	–	2.6	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 2 Adc)		–	–	3	
(I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)		–	–	3	
Diode Forward Voltage (1) (I_F = 10 Adc)	V_f	–	3	5	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	$\lvert h_{fe} \rvert$	10	–	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	100	–	350	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	t_d	–	0.02	0.2	μs
Rise Time	t_r	–	0.9	2	μs
Storage Time	t_s	–	0.95	4	μs
Fall Time	t_f	–	0.22	1	μs
Inductive Load, Clamped (Table 1)					
Storage Time (I_C = 10 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 1 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_s	–	2.3	6	μs
Crossover Time	t_c	–	1	3	μs
Storage Time (I_C = 10 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 1 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_s	–	1.4	–	μs
Crossover Time	t_c	–	0.5	–	μs
Fall Time	t_{fi}	–	0.25	–	μs

(V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%).

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

4

TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

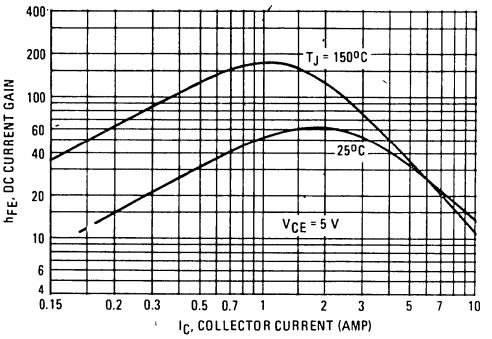


FIGURE 2 – COLLECTOR SATURATION REGION

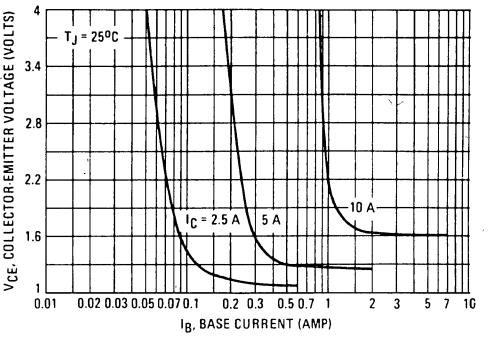


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

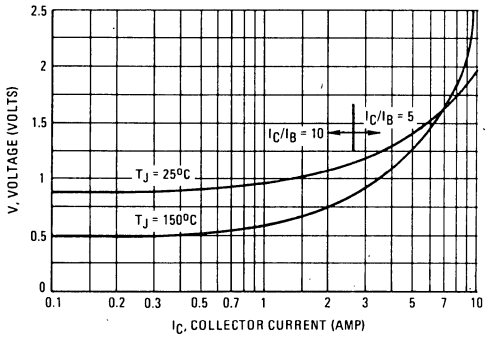


FIGURE 4 – BASE-EMITTER VOLTAGE

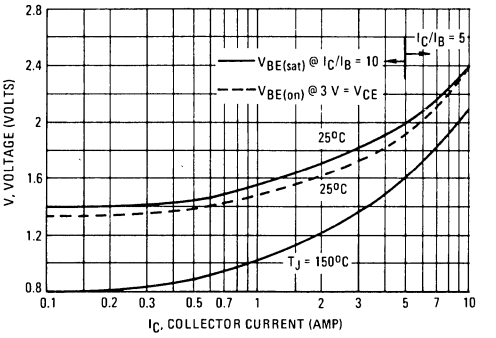


FIGURE 5 – COLLECTOR CUTOFF REGION

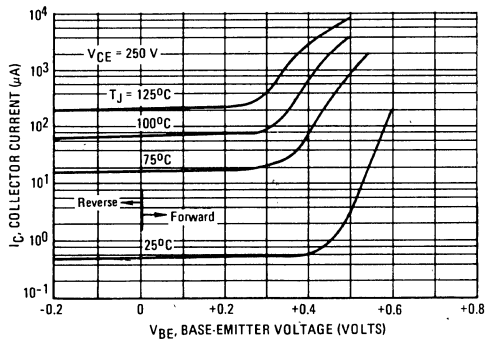


FIGURE 6 – OUTPUT CAPACITANCE

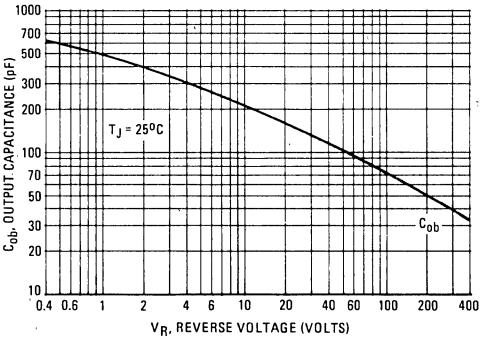


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	PW Varied to Attain I_C = 250 mA	Adjust R1 to obtain a forced h_{FE} = 10; Pulse Width; Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 50 μs); Duty Cycle < 3%; Q1 2N2907, Q2 2N2222, Q3 2N3762, Q4 MJE210, Q5 MJE200, D1 1N914, D2 1N914, D3 1N914	
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V, R_{coil} = 0.7 Ω, V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH, R_{coil} = 0.05 Ω, V_{CC} = 20 V	V_{CC} = 250 V, R_L = 25 Ω, Pulse Width = 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT: TUT, Input, See Above for Detailed Conditions, 1N4937 or Equivalent, R_{coil}, L_{coil}, V_{clamp}, V_{CC}, R_S = 0.1 Ω	OUTPUT WAVEFORMS: I_C, $I_{C(pk)}$, t_f Clamped, t_1, t_f, V_{CE}, V_{CE} or V_{clamp}, Time, t_2; t_1 Adjusted to Obtain I_C; $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$; $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$; Test Equipment: Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT: TUT, R_L, V_{CC}

SWITCHING TIME NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

– continued –

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

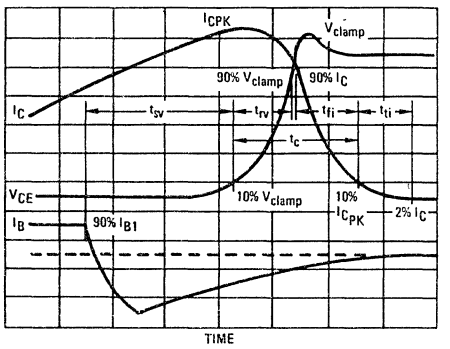
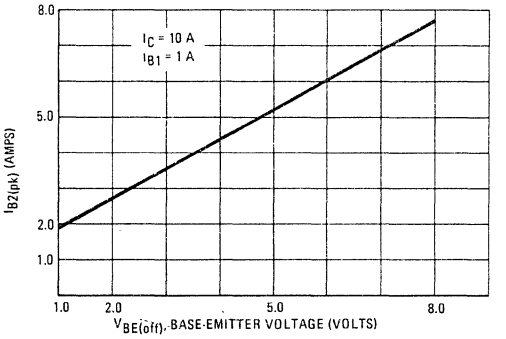


FIGURE 8 – PEAK REVERSE CURRENT



4

TYPICAL CHARACTERISTICS

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C(t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON TIME

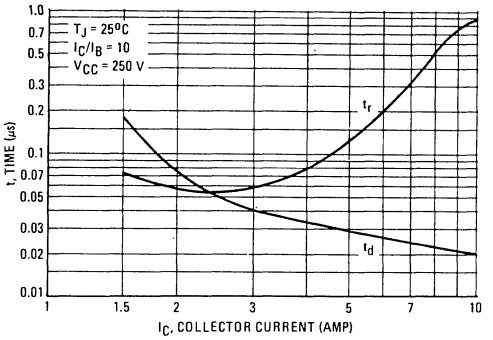


FIGURE 10 – TURN-OFF TIME

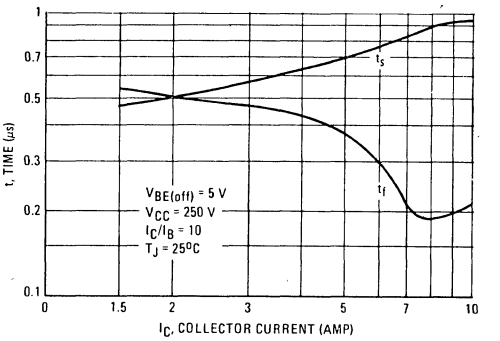
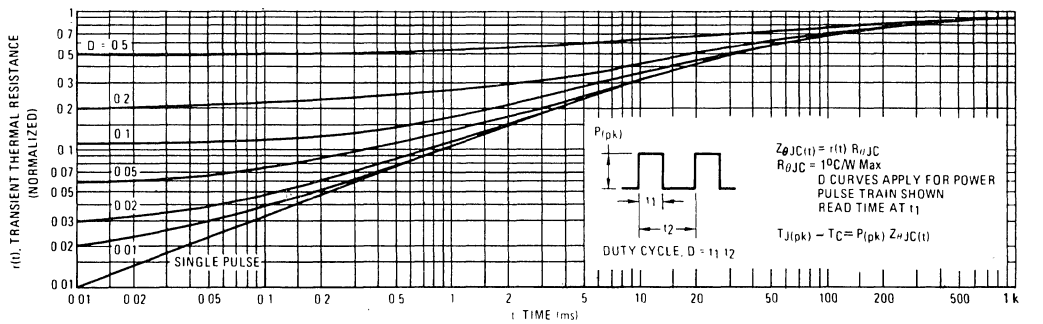


FIGURE 11 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

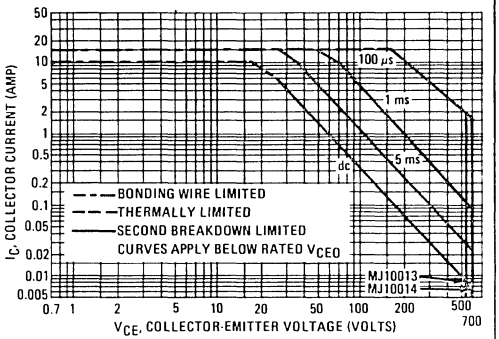
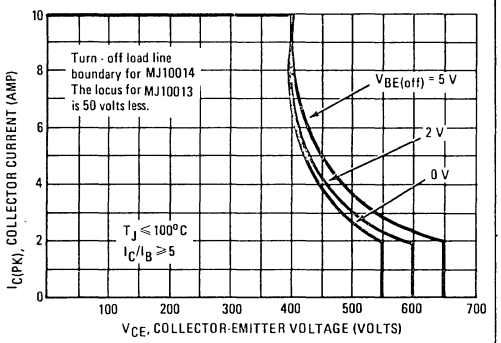


FIGURE 13 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

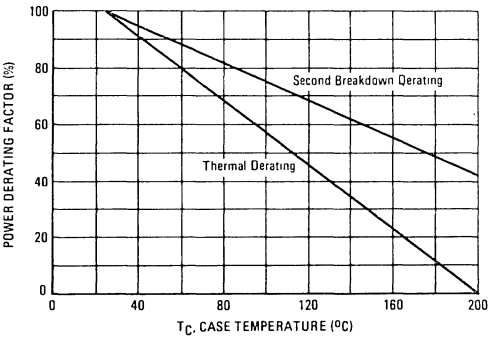
The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 – POWER DERATING



MJ10015
MJ10016

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

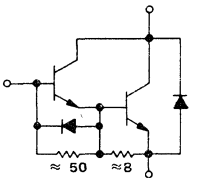
The MJ10015 and MJ10016 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

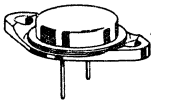
- Switching Regulators
- Motor Controls
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  - 1.0 μs (max) Inductive Crossover Time – 20 Amps
  - 2.5 μs (max) Inductive Storage Time – 20 Amps
- Operating Temperature Range –65 to +200°C
- Performance Specified for
  - Reversed Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents

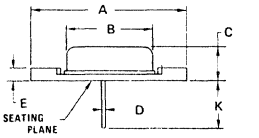
50 AMPERE

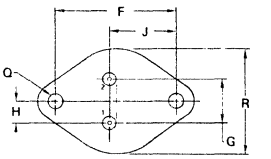
NPN SILICON POWER DARLINGTON TRANSISTORS

400 and 500 VOLTS
250 WATTS









STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO-3

MAXIMUM RATINGS

Rating	Symbol	MJ10015	MJ10016	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	500	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	50 75		Adc
Base Current – Continous – Peak (1)	I_B I_{BM}	10 15		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 143 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%

Switchmode is a trademark of Motorola, Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0, V_{clamp} = Rated V_{CEO})	MJ10015 MJ10016	$V_{CEO(sus)}$	 400 500	 – –	 – –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	–	–	0.25	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 Vdc, I_C = 0)		I_{EBO}	–	–	350	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 7			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 8			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 20 Adc, V_{CE} = 5.0 Vdc) (I_C = 40 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	 25 10	 – –	 – –	–
Collector-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.0 Adc) (I_C = 50 Adc, I_B = 10 Adc)		$V_{CE(sat)}$	 – –	 – –	 2.2 5.0	Vdc
Base-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	–	–	2.75	Vdc
Diode Forward Voltage (2) (I_F = 20 Adc)		V_f	–	2.5	5.0	Vdc
DYNAMIC CHARACTERISTIC						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)		C_{ob}	–	–	750	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 20 A, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 5 Vdc, t_p = 25 μs Duty Cycle ⩽ 2%).	t_d	–	0.14	0.3	μs
Rise Time		t_r	–	0.3	1.0	μs
Storage Time		t_s	–	0.8	2.5	μs
Fall Time		t_f	–	0.3	1.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 20 A(pk), V_{clamp} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc)	t_{sv}	–	1.0	2.5	μs
Crossover Time		t_c	–	0.36	1.0	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ⩽ 2%.

(2) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

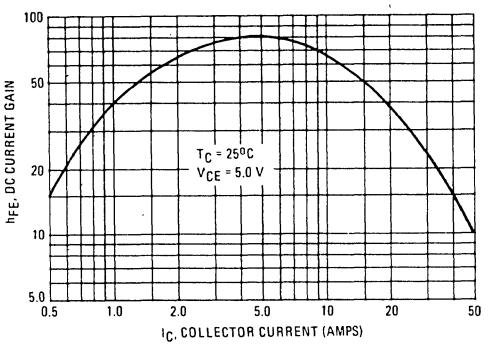


FIGURE 2 – COLLECTOR-EMITTER SATURATION VOLTAGE

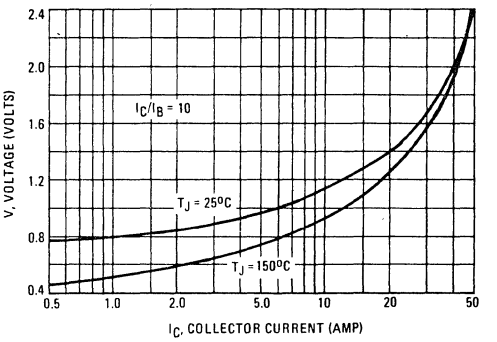


FIGURE 3 – BASE-EMITTER SATURATION VOLTAGE

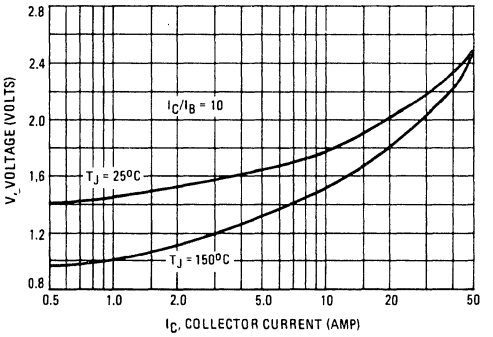


FIGURE 4 – COLLECTOR CUTOFF REGION

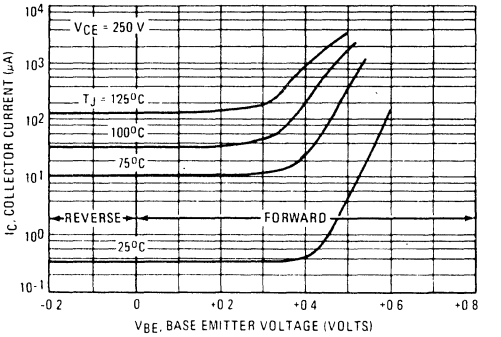


FIGURE 5 – OUTPUT CAPACITANCE

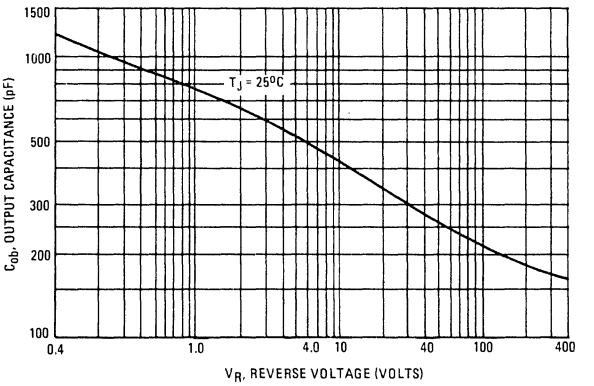
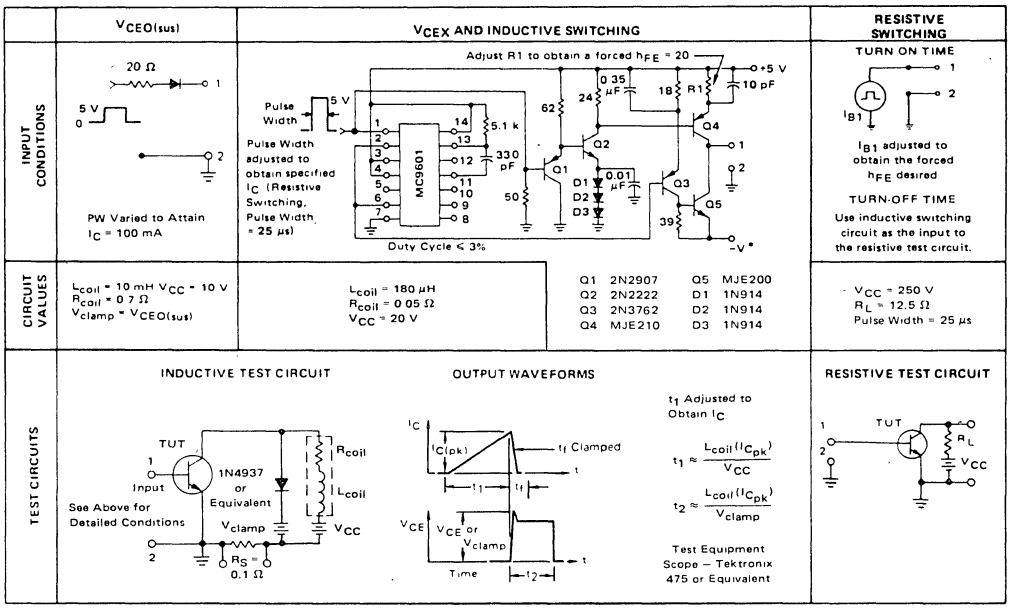
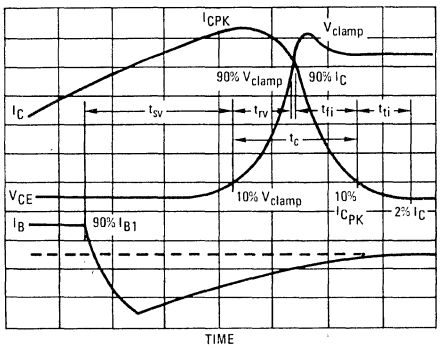


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE



*Adjust -V such that $V_{BE(off)}$ = 5 V except as required for RB SOA (Figure 12).

FIGURE 6 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10-90% V_{clamp}
t_{fi} = Current Fall Time, 90-10% I_C
t_{ti} = Current Tail, 10-2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed.

4

The Safe Operating Area figures shown in Figures 7 and 8 are specified ratings for these devices under the test conditions shown.

FIGURE 7 – FORWARD BIAS SAFE OPERATING AREA

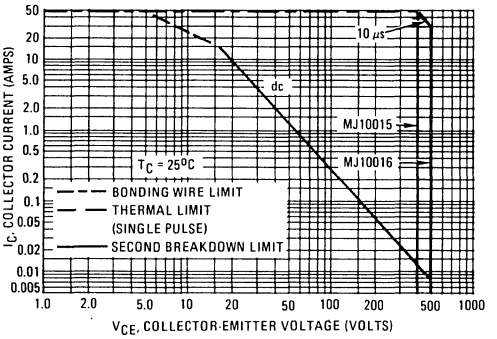
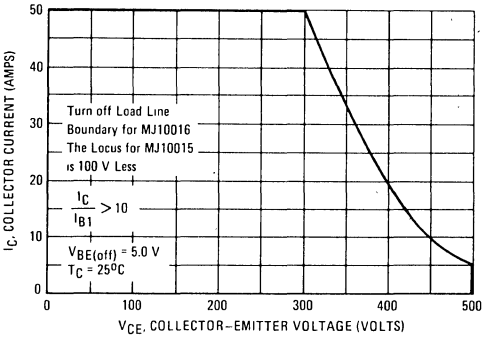


FIGURE 8 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 8 gives the complete RBSOA characteristics.

FIGURE 9 – POWER DERATING

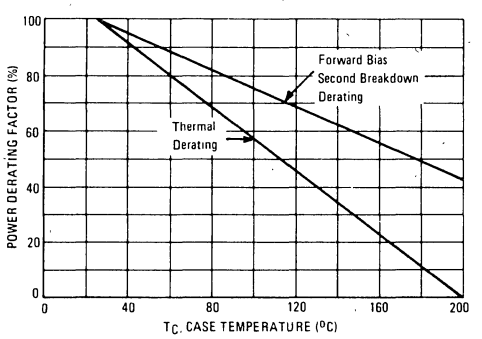
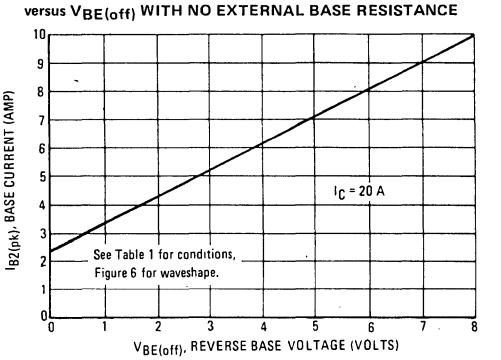


FIGURE 10 – TYPICAL REVERSE BASE CURRENT versus $V_{BE(off)}$ WITH NO EXTERNAL BASE RESISTANCE



PNP

MJ11011, MJ11013, MJ11015

NPN

MJ11012, MJ11014, MJ11016

HIGH-CURRENT COMPLEMENTARY SILICON TRANSISTORS

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain – h_{FE} = 1000 (Min) @ I_C = 20 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistor
- Junction Temperature to +200°C

30 AMPERE

DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON

60-120 VOLTS
200 WATTS

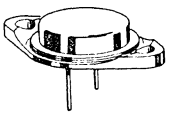
4

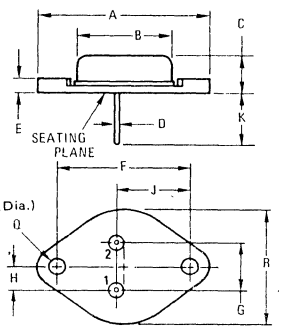
MAXIMUM RATINGS

Rating	Symbol	MJ11011 MJ11012	MJ11013 MJ11014	MJ11015 MJ11016	Unit
Collector-Emitter Voltage	V_{CEO}	60	90	120	Vdc
Collector-Base Voltage	V_{CB}	60	90	120	Vdc
Emitter-Base Voltage	V_{EB}	5			Vdc
Collector Current	I_C	30			Adc
Base Current	I_B	1			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C @ T_C = 100°C	P_D	200 115			Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.87	°C/W
Maximum Lead Temperature for Soldering Purposes for ≤ 10 Seconds.	T_L	275	°C



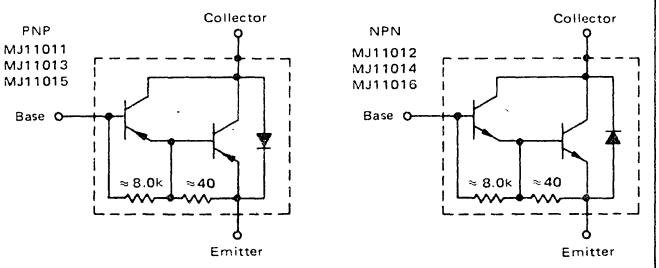


PIN 1 BASE
2 EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
TO-3

FIGURE 1 – DARLINGTON CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1)		BV_{CEO}			Vdc
(I_C = 100 mAdc, I_B = 0)	MJ11011,MJ11012		60	–	
	MJ11013,MJ11014		90	–	
	MJ11015,MJ11016		120	–	
Collector Emitter Leakage Current		I_{CER}			mAdc
(V_{CE} = 60 Vdc, R_{BE} = 1 k ohm)	MJ11011,MJ11012		–	1	
(V_{CE} = 90 Vdc, R_{BE} = 1 k ohm)	MJ11013,MJ11014		–	1	
(V_{CE} = 120 Vdc, R_{BE} = 1 k ohm)	MJ11015,MJ11016		–	1	
(V_{CE} = 60 Vdc, R_{BE} = 1 k ohm, T_C = 150°C)	MJ11011,MJ11012		–	5	
(V_{CE} = 90 Vdc, R_{BE} 1 k ohm, T_C = 150°C)	MJ11013,MJ11014		–	5	
(V_{CE} = 120 Vdc, R_{BE} 1 k ohm, T_C = 150°C)	MJ11015,MJ11016		–	5	
Emitter Cutoff Current		I_{EBO}	–	5	mAdc
(V_{BE} = 5 Vdc, I_C = 0)					
Collector-Emitter Leakage Current		I_{CEO}	–	1	mAdc
(V_{CE} = 50 Vdc, I_B = 0)					
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			–
(I_C = 20 Adc, V_{CE} = 5 Vdc)			1000	–	
(I_C = 30 Adc, V_{CE} = 5 Vdc)			200	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 20 Adc, I_B = 200 mAdc)			–	3	
(I_C = 30 Adc, I_B = 300 mAdc)			–	4	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
I_C = 20 Adc, I_B = 200 mAdc)			–	3.5	
I_C = 30 Adc, I_B = 300 mAdc)			–	5	
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio (I_C = 10 Adc, V_{CE} = 3 Vdc, f = 1 MHz)		$\|h_{fe}\|$	4	–	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

FIGURE 2 – DC CURRENT GAIN (1)

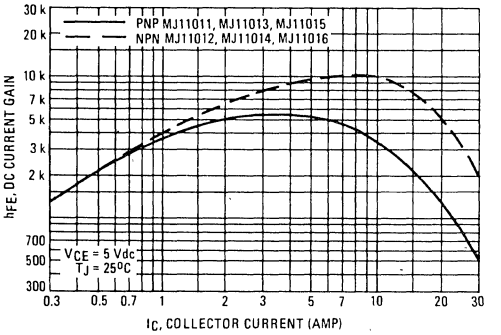


FIGURE 3 – SMALL-SIGNAL CURRENT GAIN

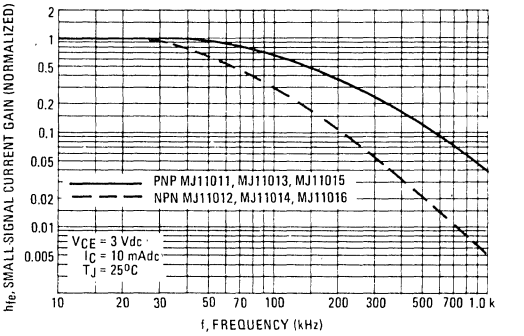


FIGURE 4 – "ON" VOLTAGES (1)

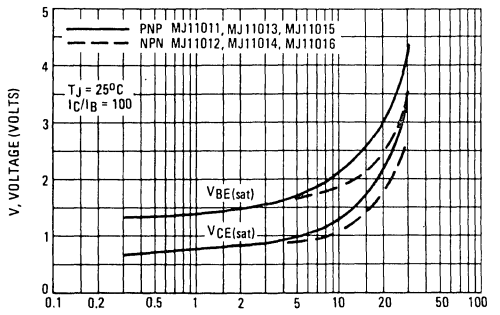
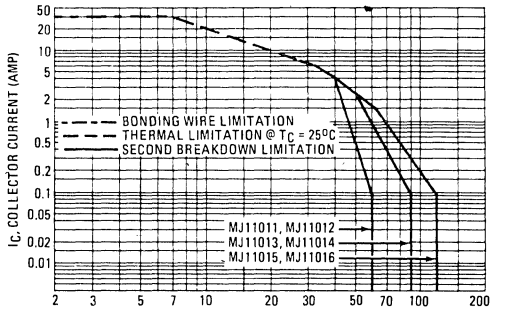


FIGURE 5 – ACTIVE REGION DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation, e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

NPN PNP

MJ11028 MJ11029
MJ11030 MJ11031
MJ11032 MJ11033

Advance Information

HIGH-CURRENT COMPLEMENTARY SILICON TRANSISTORS

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain – h_{FE} = 1000 (Min) @ I_C = 25 Adc
  h_{FE} = 400 (Min) @ I_C = 50 Adc
- Curves to 100 A (Pulsed)
- Diode Protection to Rated I_C
- Monolithic Construction with Built-In Base-Emitter Shunt Resistor
- Junction Temperature to +200°C

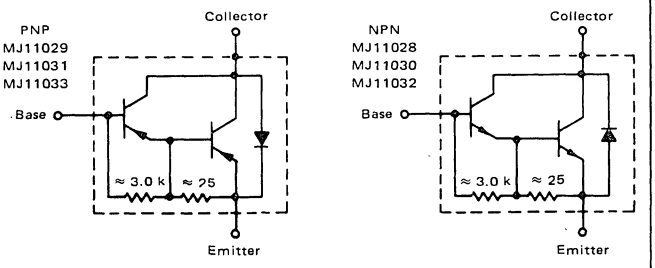
MAXIMUM RATINGS

Rating	Symbol	MJ11028 MJ11029	MJ11030 MJ11031	MJ11032 MJ11033	Unit
Collector-Emitter Voltage	V_{CEO}	60	90	120	Vdc
Collector-Base Voltage	V_{CB}	60	90	120	Vdc
Emitter-Base Voltage	V_{EB}	5			Vdc
Collector Current—Continuous Peak	I_C I_{CM}	50 100			Adc
Base Current—Continuous	I_B	2			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C @ T_C = 100°C	P_D	300 1.71			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Maximum Lead Temperature for Soldering Purposes for ≤ 10 seconds	T_L	275	°C
Thermal Resistance Junction to Case	$R_{\theta JC}$	0.584	°C

FIGURE 1 – DARLINGTON CIRCUIT SCHEMATIC

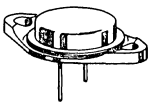


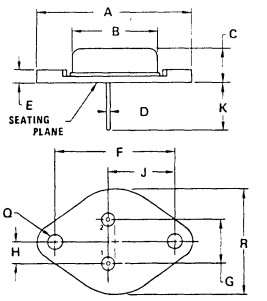
This is advance information and specifications are subject to change without notice.

50 AMPERE

COMPLEMENTARY SILICON DARLINGTON POWER TRANSISTOR

60–120 VOLTS
300 WATTS





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

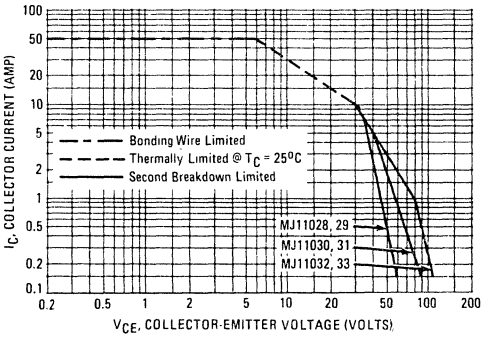
CASE 197-01
(TO-3 Except Pin Diameter)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1)		BV_{CEO}			Vdc
(I_C = 100 mAdc, I_B = 0)	MJ11028 MJ11029		60	–	
	MJ11030 MJ11031		90	–	
	MJ11032 MJ11033		120	–	
Collector-Emitter Leakage Current		I_{CER}			mAdc
(V_{CE} = 60 Vdc, R_{BE} = 1 k ohm)	MJ11028 MJ11029		–	2	
(V_{CE} = 90 Vdc, R_{BE} = 1 k ohm)	MJ11030 MJ11031		–	2	
(V_{CE} = 120 Vdc, R_{BE} = 1 k ohm)	MJ11032 MJ11033		–	2	
(V_{CE} = 60 Vdc, R_{BE} = 1 k ohm, T_C = 150°C)	MJ11028 MJ11029		–	10	
(V_{CE} = 90 Vdc, R_{BE} = 1 k ohm, T_C = 150°C)	MJ11030 MJ11031		–	10	
(V_{CE} = 120 Vdc, R_{BE} = 1 k ohm, T_C = 150°C)	MJ11032 MJ11033		–	10	
Emitter Cutoff Current		I_{EBO}	–	5	mAdc
(V_{BE} = 5 Vdc, I_C = 0)					
Collector-Emitter Leakage Current		I_{CEO}	–	2	mAdc
(V_{CE} = 50 Vdc, I_B = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 25 Adc, V_{CE} = 5 Vdc)			1 k	18 k	
(I_C = 50 Adc, V_{CE} = 5 Vdc)			400	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 250 mAdc)			–	2.5	
(I_C = 50 Adc, I_B = 500 mAdc)			–	3.5	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 200 mAdc)			–	3.0	
(I_C = 50 Adc, I_B = 300 mAdc)			–	4.5	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC SAFE OPERATING AREA



There are two limitations on the power-handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 3 – DC CURRENT GAIN

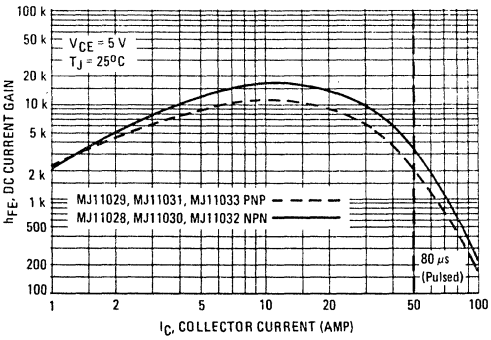
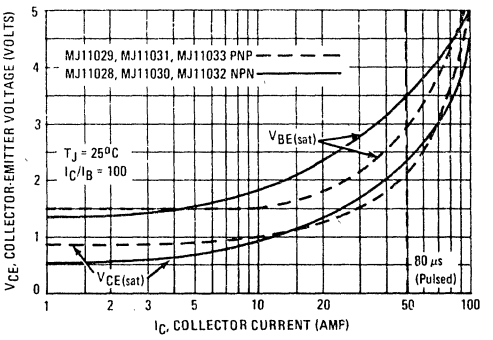


FIGURE 4 – "ON" VOLTAGE



Designer's Data Sheet

HORIZONTAL DEFLECTION TRANSISTOR

. . . specifically designed for use in large screen color deflection circuits.

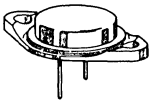
- Collector-Emitter Voltage — V_{CEX} = 1500 Volts
- Glassivated Base-Collector Junction
- Forward Bias Safe Operating Area @ 50 μs = 15 A, 300 V
- Switching Times with Inductive Loads — t_f = 0.65 μs (Typ) @ I_C = 2.0 A

2.5 AMPERE
NPN SILICON
POWER TRANSISTOR

1500 VOLTS
75 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

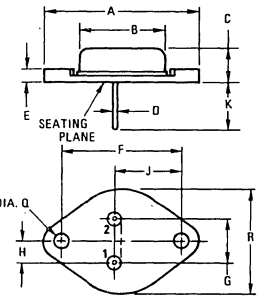


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	750	Vdc
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current — Continuous	I_C	2.5	Adc
Base Current — Continuous	I_B	2.0	Adc
Emitter Current — Continuous	I_E	4.5	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	75 30 0.6	Watts Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

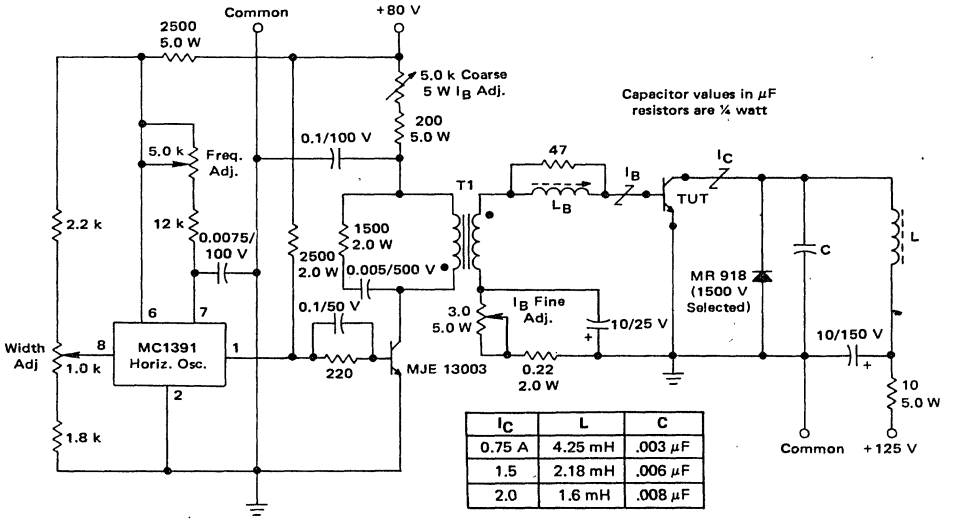
CASE 11-01
TO-3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	750	–	–	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)	I_{CES}	–	–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	–	0.1	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 1.8 Adc)	$V_{CE(sat)}$	–	–	5.0	Vdc
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 1.8 Adc)	$V_{BE(sat)}$	–	–	1.5	Vdc
Second Breakdown Collector Current with Base-Forward Biased	$I_{S/B}$		See Figure 14		–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	50	–	pF
Current Gain – Bandwidth Product (1) (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T	–	4.0	–	MHz
SWITCHING CHARACTERISTICS					
Fall Time (I_C = 2.0 Adc, I_{B1} = 1.0 Adc, L_B = 12 μH, See Figure 1)	t_f	–	0.65	1.0	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

FIGURE 1 – TEST CIRCUIT



I_C	L	C
0.75 A	4.25 mH	.003 μF
1.5	2.18 mH	.006 μF
2.0	1.6 mH	.008 μF

DRIVER TRANSFORMER (T1)

Motorola part number 25D68782A-05-1/4" laminate "E" iron core. Primary Inductance – 39 mH. Secondary Inductance – 22 mH, Leakage Inductance with primary shorted – 2.0 μH, Primary 260 turns #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.

BASE DRIVE: The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B as shown in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1}, and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when $I_{B1}\ h_{FE} = I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the $I_{B1}\ h_{FE} = I_{CM}$ point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor initiation of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left or right according to the relation $I_{B1}\ h_{FE}$ = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM}. These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

4

TEST CIRCUIT WAVEFORMS

FIGURE 2

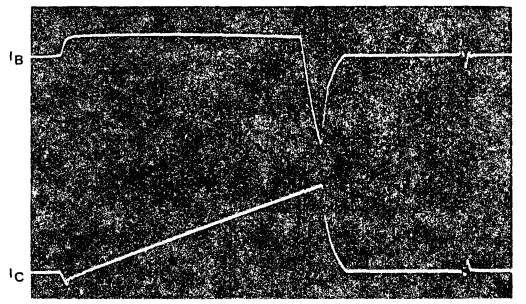
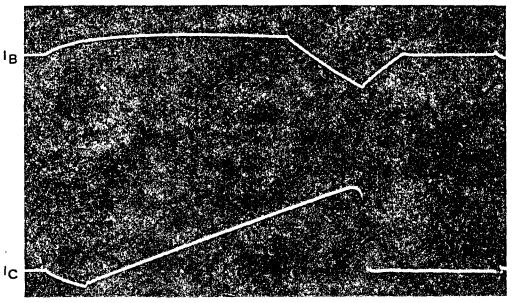


FIGURE 3



TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance.

Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

FIGURE 4 – OPTIMIZING DRIVE @ I_C = 0.75 A

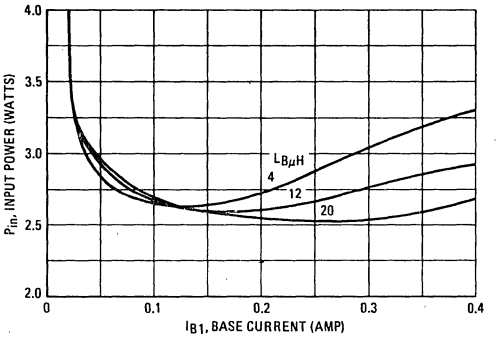


FIGURE 5 – OPTIMIZING DRIVE @ I_C = 1.5 A

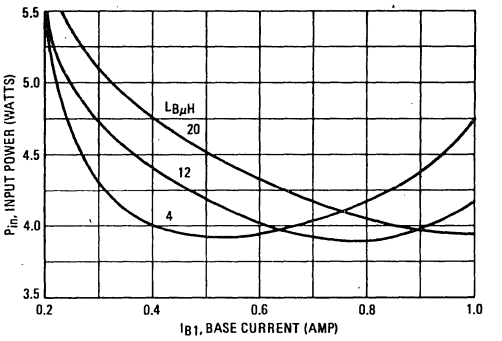


FIGURE 6 – OPTIMIZING DRIVE @ I_C = 2.0 A

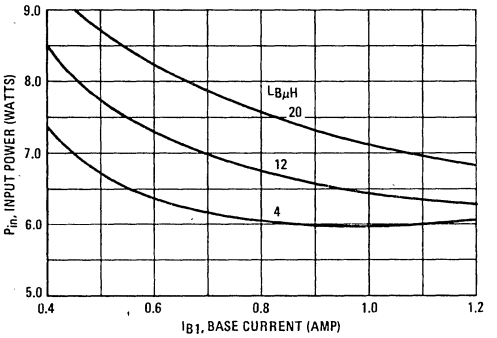


FIGURE 7 – SWITCHING BEHAVIOR versus TEMPERATURE

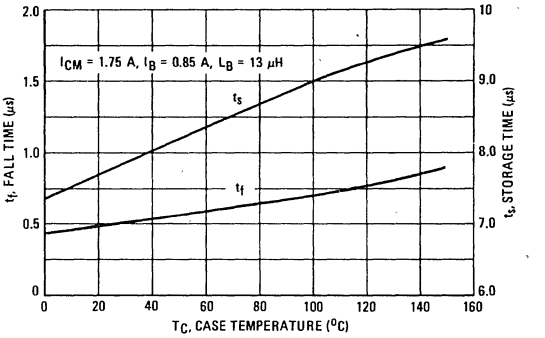


FIGURE 8 – OPTIMUM DRIVE CONDITIONS

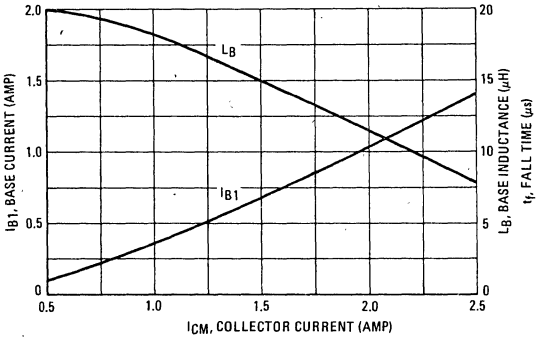


FIGURE 9 – SWITCHING BEHAVIOR versus I_{CM}

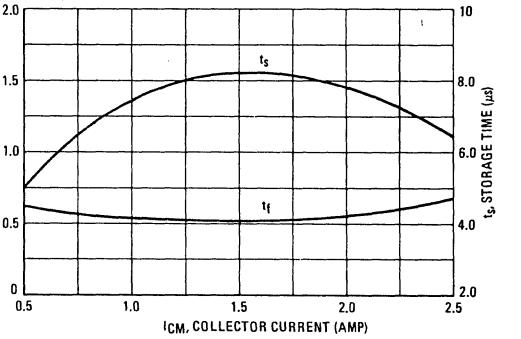


FIGURE 10 – THERMAL RESPONSE

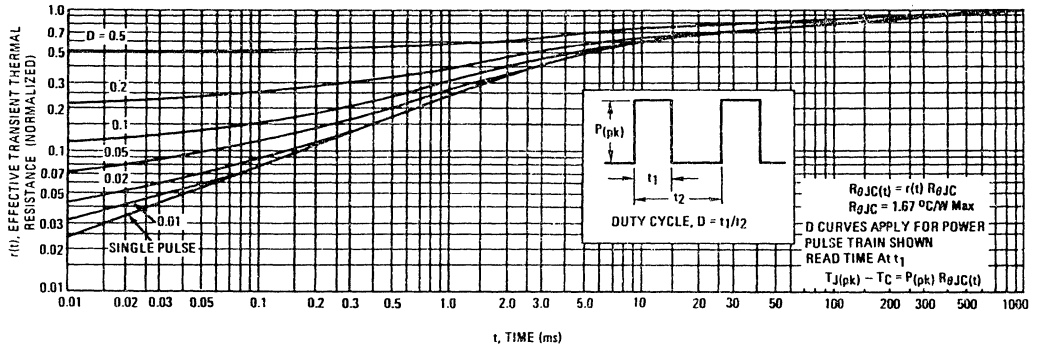


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FIGURE 11 – COLLECTOR SATURATION REGION

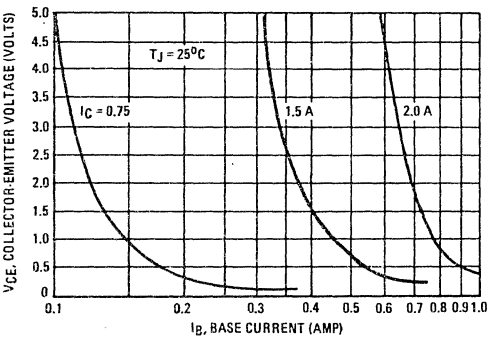


FIGURE 12 – DC CURRENT GAIN

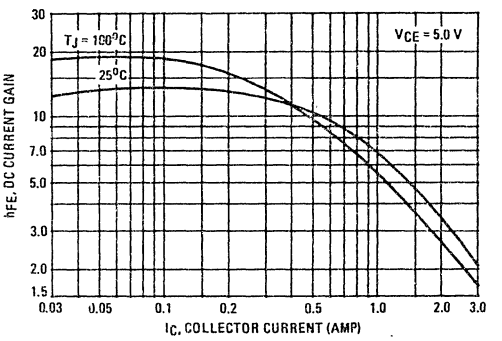


FIGURE 13 – "ON" VOLTAGES

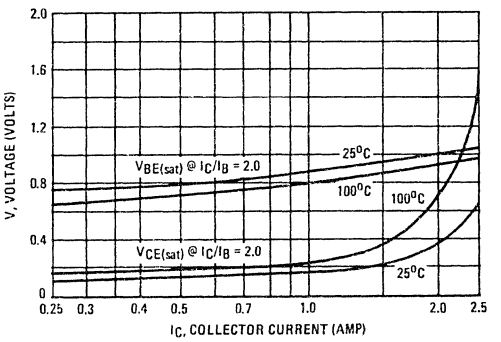
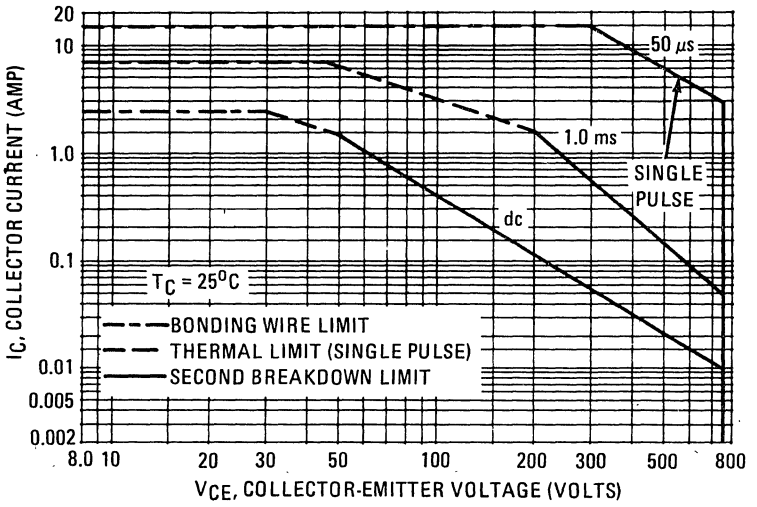


FIGURE 14 – MAXIMUM FORWARD BIAS
SAFE OPERATING AREA



NOTE:
There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The 50 μs SB curve is beyond the thermal limits of this part. However, the parts will survive a transient that remains within these SB limits without failing.

MJ12004

Designers Data Sheet

HORIZONTAL DEFLECTION TRANSISTOR

. . . specifically designed for use in large screen color deflection circuits.

- Collector-Emitter Voltage — V_{CEX} = 1500 Vdc
- Glassivated Base-Collector Junction
- Safe Operating Area @ 50 μs = 20 A, 400 V
- Switching Times with Inductive Loads — t_f = 0.4 μs (Typ) @ I_C = 4.5 A

5 AMPERE

NPN SILICON POWER TRANSISTORS

1500 VOLTS
100 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

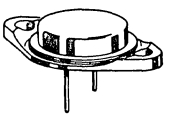
4

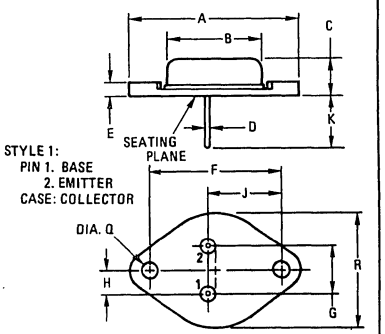
MAXIMUM RATINGS

Rating	Symbol	MJ12004	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	750	Vdc
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	5.0	Adc
Base Current — Continuous	I_B	4.0	Adc
Emitter Current — Continuous	I_E	9.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	100 40 0.8	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.

CASE 11-01
TO-3

4

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	750	–	–	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)	I_{CES}	–	–	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	–	1.0	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 4.5 Adc, I_B = 1.8 Adc)		–	–	5.0	
(I_C = 3.5 Adc, I_B = 1.5 Adc)		–	–	5.0	
Base Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 4.5 Adc, I_B = 1.8 Adc)		–	–	1.5	
(I_C = 3.5 Adc, I_B = 1.5 Adc)		–	–	1.5	
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 14			
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1 MHz)	f_T	–	4	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	125	–	pF
SWITCHING CHARACTERISTICS					
Fall Time	t_f				μs
(I_C = 4.5 Adc, I_{B1} = 1.8 Adc, T_C = 25°C		–	0.4	1.0	
L_B = 8.0 μH, See Figure 1) T_C = 100°C		–	0.6	–	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

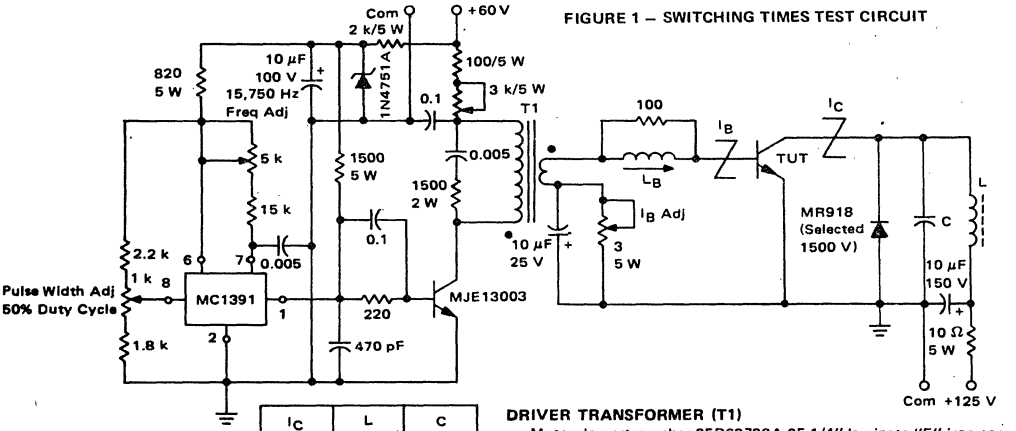


FIGURE 1 – SWITCHING TIMES TEST CIRCUIT

I_C A	L mH	C μF
3.5	0.87	0.013
4.5	0.67	0.017

DRIVER TRANSFORMER (T1)

Motorola part number 25D68782A-05-1/4" laminate "E" iron core. Primary Inductance – 39 mH, Secondary Inductance – 0.22 mH, Leakage Inductance with primary shorted – 2.0 μH. Primary 260 turns, #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.

BASE DRIVE: The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst-case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B as shown in Figures 4 and 5. This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1}, and low values of L_B is due to switching losses as described above. Note that for very low L_B a very narrow optimum is obtained. This occurs when $I_{B1}\ h_{FE} = I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the $I_{B1}\ h_{FE} = I_{CM}$ point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor *initiation* of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left or right according to the relation $I_{B1}\ h_{FE}$ = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Figure 8 gives values recommended for L_B and I_{B1} for this device over a wide range of I_{CM}. These values were chosen from a large number of curves like Figure 4 and Figure 5. Neither L_B nor I_{B1} are absolutely critical, as can be seen from the examples shown, and values of Figure 8 are provided for guidance only.

4

TEST CIRCUIT WAVEFORMS

FIGURE 2

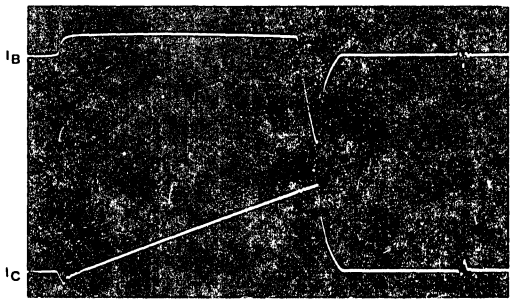
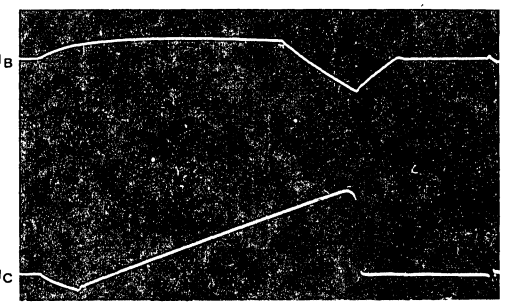


FIGURE 3



TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance.

Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

FIGURE 4 – OPTIMIZING DRIVE @ 3.5 A

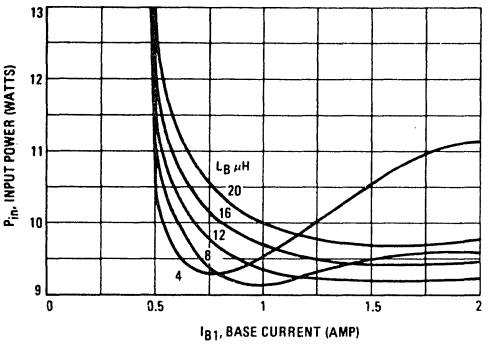


FIGURE 5 – OPTIMIZING DRIVE @ 4.5 A

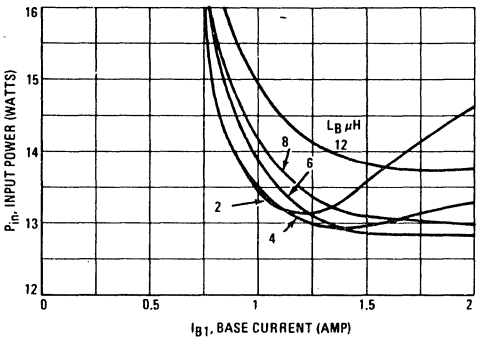


FIGURE 6 – SWITCHING BEHAVIOR versus TEMPERATURE
I_{CM} = 3.5 A, I_B = 1.5 A, L_B = 14 μH

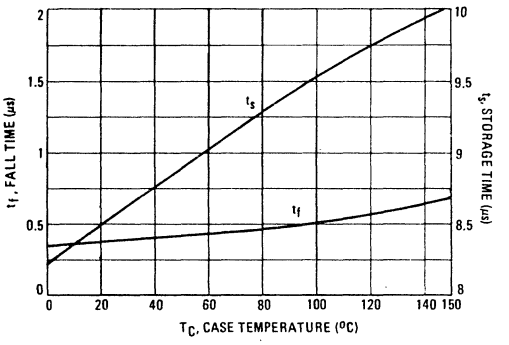


FIGURE 7 – SWITCHING BEHAVIOR versus TEMPERATURE
I_{CM} = 4.5 A, I_B = 1.75 A, L_B = 8 μH

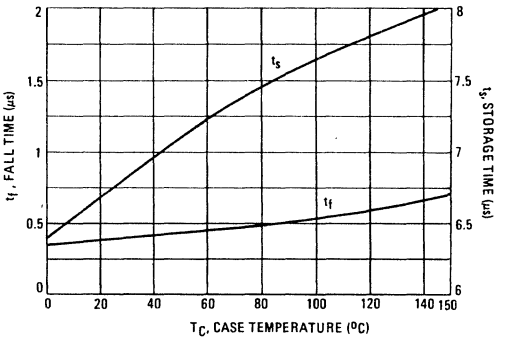


FIGURE 8 – OPTIMUM DRIVE CONDITIONS

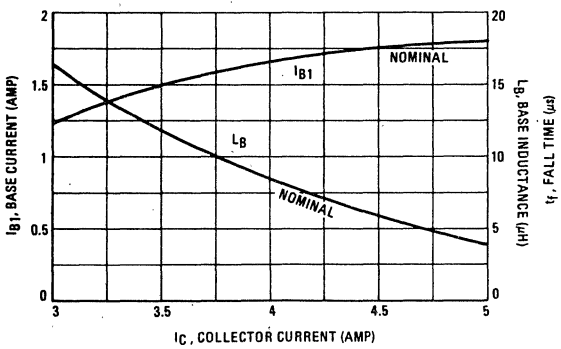


FIGURE 9 – SWITCHING BEHAVIOR versus I_{CM}

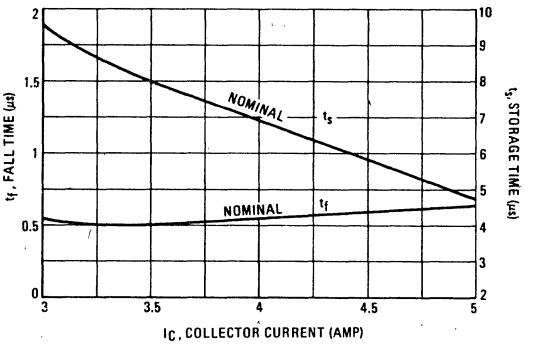


FIGURE 10 – THERMAL RESPONSE

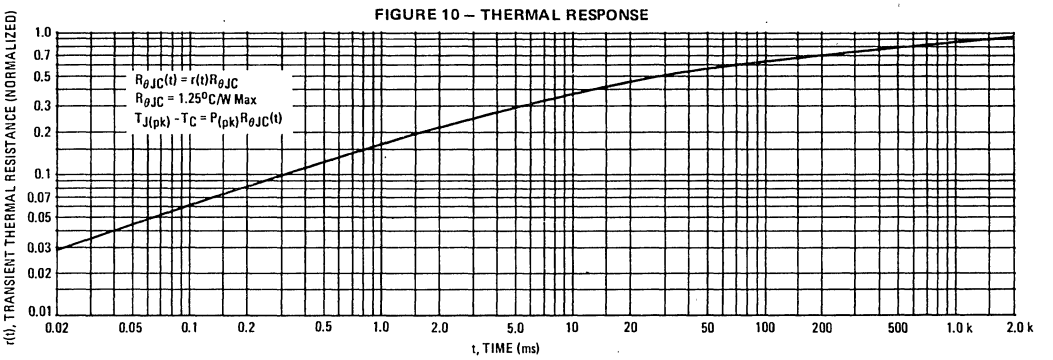


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FIGURE 11 – COLLECTOR SATURATION REGION

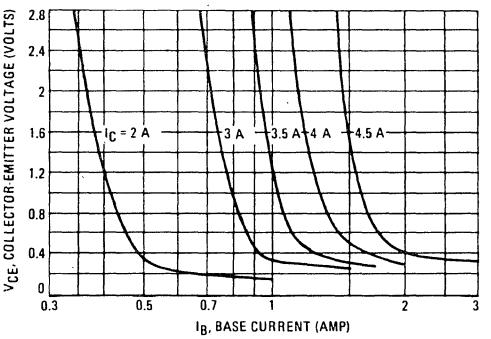


FIGURE 12 – DC CURRENT GAIN

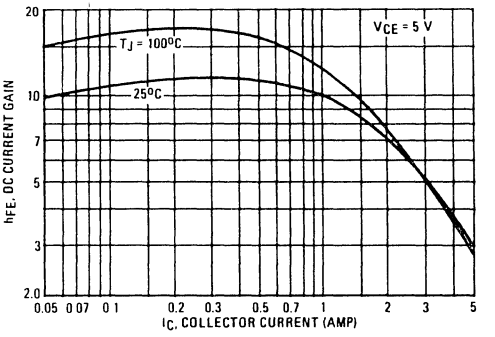


FIGURE 13 – "ON" VOLTAGES

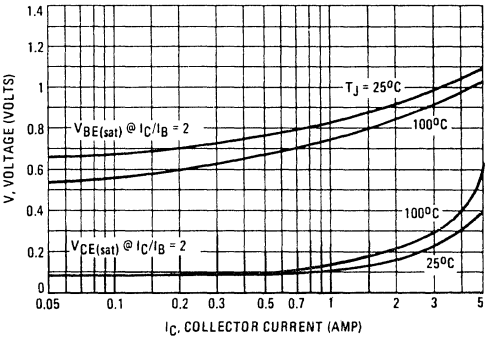
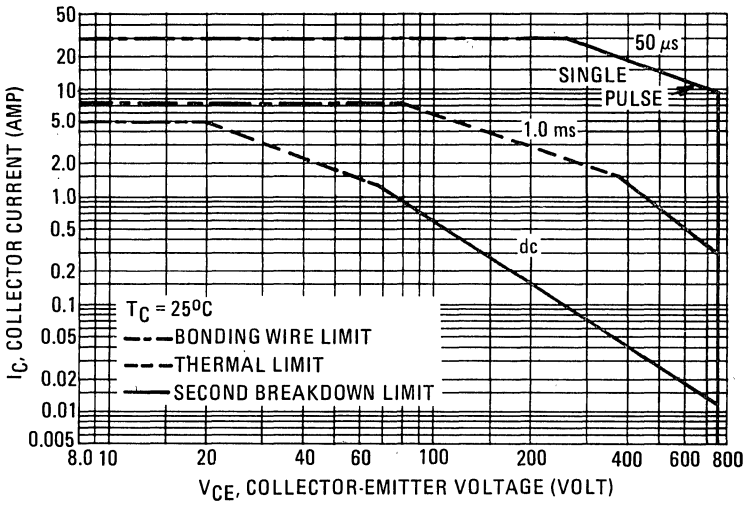


FIGURE 14 – MAXIMUM FORWARD BIAS
SAFE OPERATING AREA



NOTE:

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The 50 μs SB curve is beyond the thermal limits of this part. However, the parts will survive a transient that remains within these SB limits without failing.

Advance Information

HORIZONTAL DEFLECTION TRANSISTOR

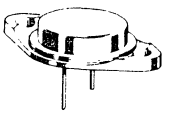
. . . specifically designed for use in deflection circuits.

- V_{CEX} = 1500 V
- Glassivated Base-Collector Junction
- Safe Operating Area @ 50 μs = 20 A, 400 V

8 AMPERE

NPN SILICON POWER TRANSISTOR

1500 VOLTS
100 WATTS



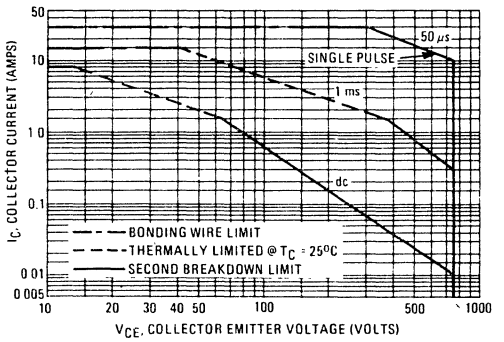
MAXIMUM RATINGS

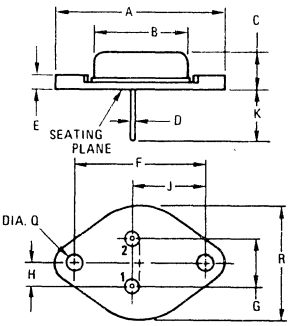
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEX}	1500	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	8.0	Adc
Base Current — Continuous	I_B	4.0	Adc
Emitter Current — Continuous	I_E	12	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.8	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to + 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

FIGURE 1 — MAXIMUM FORWARD BIAS SAFE OPERATING AREA





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
(TO-3)

This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (V_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	750	–	–	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0)	I_{CES}	–	–	0.25	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	–	0.1	mAdc
ON CHARACTERISTICS (1)					
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$	–	–	5.0	Vdc
Base Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{BE(sat)}$	–	–	1.5	Vdc
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	–	–	See Figure 1	
SWITCHING CHARACTERISTICS					
Fall Time (I_C = 5.0 Adc, I_{B1} = 1.0 Adc, L_B = 8.0 μH	t_f	–	0.4	1.0	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2%.

4

FIGURE 2 – DC CURRENT GAIN

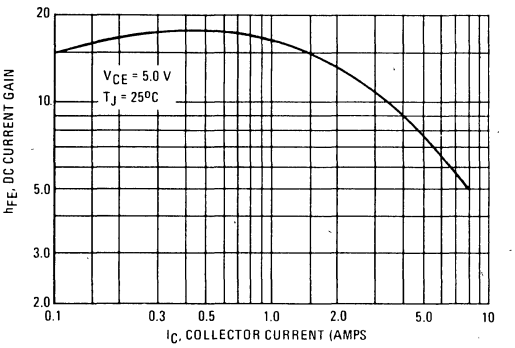
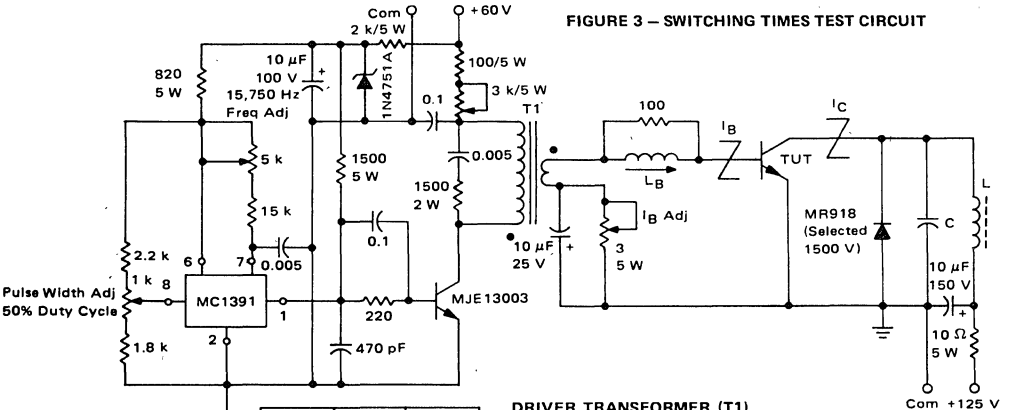


FIGURE 3 – SWITCHING TIMES TEST CIRCUIT



I_C A	L mH	C μF
5.0	0.575	0.018

DRIVER TRANSFORMER (T1)

Motorola part number 25D68782A-05-1/4" laminate "E" iron core. Primary Inductance – 39 mH, Secondary Inductance – 0.22 mH, Leakage Inductance with primary shorted – 2.0 μH. Primary 260 turns, #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.

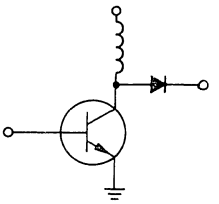
MJ13014
MJ13015

Designer's Data Sheet

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTORS

The MJ13014 and MJ13015 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn - Off Times:
60 ns Inductive Fall Time @ 25°C (Typ)
120 ns Inductive Crossover Time @ 25°C (Typ)
800 ns Inductive Storage Time @ 25°C (Typ)

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents

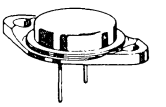
10 AMPERE

NPN SILICON POWER TRANSISTORS

350 AND 400 VOLTS
150 WATTS

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



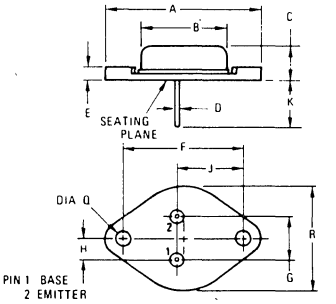
MAXIMUM RATINGS

Rating	Symbol	MJ13014	MJ13015	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Emitter Voltage	V_{CEV}	550	600	Vdc
Emitter Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 20		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	5.0 10		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	150 85.5 0.86		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



PIN 1 BASE
2 EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case
CASE 11-01
TO-3

▲ Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$				Vdc
(I_C = 100 mA, I_B = 0)	MJ13014		350	–	–	
	MJ13015		400	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	0.5	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	–	2.5	
Collector Cutoff Current		I_{CER}	–	–	3.0	mAdc
(V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)						
Emitter Cutoff Current		I_{EBO}	–	–	1.0	mAdc
(V_{EB} = 6.0 Vdc, I_C = 0)						
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}				–
(I_C = 2.5 Adc, V_{CE} = 5 Vdc)			12	–	40	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 1.0 Adc)			–	–	1.4	
(I_C = 10 Adc, I_B = 2.0 Adc)			–	–	5.0	
(I_C = 5 Adc, I_B = 1.0 Adc, T_C = 100°C)			–	–	2.4	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 1.0 Adc)			–	–	1.5	
(I_C = 5 Adc, I_B = 1.0 Adc, T_C = 100°C)			–	–	1.5	
DYNAMIC CHARACTERISTICS						
Output Capacitance		C_{ob}	50	–	350	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)						
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 5.0 A, I_{B1} = 1.0 A,	t_d	–	0.01	0.1	μs
Rise Time	t_p = 25 μs, Duty Cycle ≤ 2%)	t_r	–	0.085	0.5	μs
Storage Time	(V_{CC} = 250 Vdc, I_C = 5.0 A, I_{B1} = 1.0 A,	t_s	–	0.8	2.0	μs
Fall Time	$V_{BE(off)}$ = 5.0 Vdc, t_p = 25 μs, Duty Cycle ≤ 2%)	tf	–	0.095	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 5 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 1.0 A,	t_{sv}	–	1.5	3.5	μs
Crossover Time	$V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_c	–	0.25	1.0	μs
Fall Time		t_{fi}	–	0.12	–	μs
Storage Time	(I_C = 5 A (pk), V_{clamp} = 250 Vdc, I_{B1} = 1.0 A,	t_{sv}	–	0.8	–	μs
Crossover Time	$V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_c	–	0.12	–	μs
Fall Time		t_{fi}	–	0.06	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

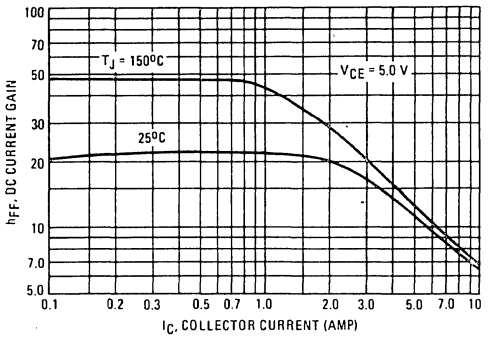


FIGURE 2 – COLLECTOR SATURATION REGION

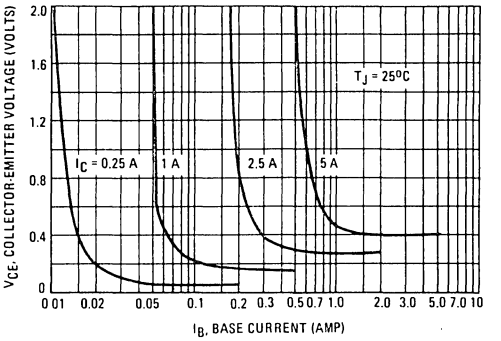


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

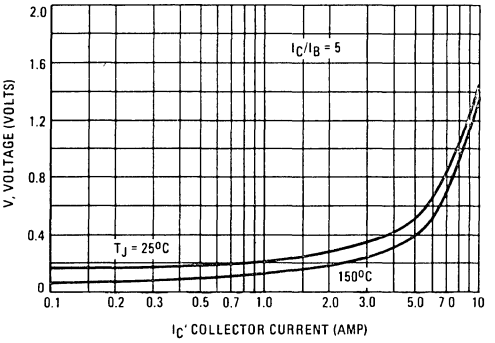


FIGURE 4 – BASE-EMITTER VOLTAGE

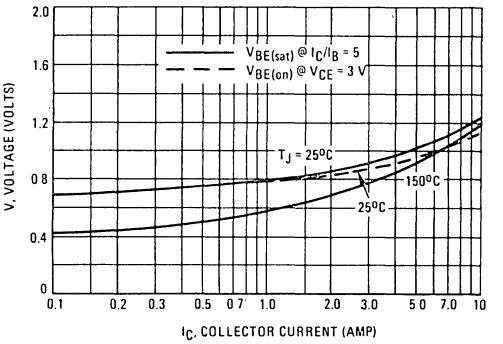


FIGURE 5 – COLLECTOR CUTOFF REGION

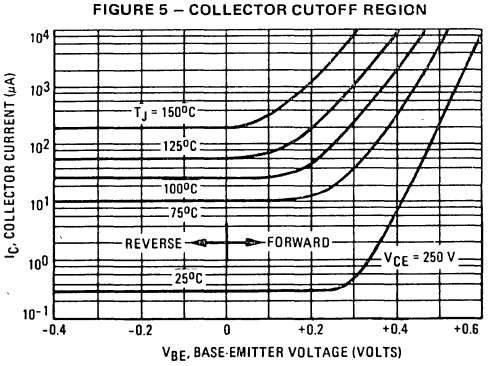
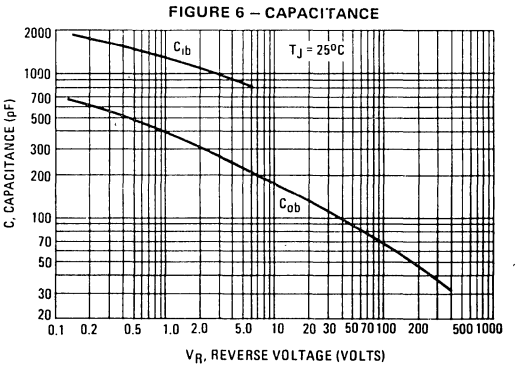


FIGURE 6 – CAPACITANCE



4

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V, 20, 0, 1, 2 PW Varied to Attain I_C = 100 mA	250 μF, 470 Ω 2 W, 47 Ω, R1, +15, 15 V, 0, 330 Ω, 5.1 Ω 5 W, R2, 50 Ω, 100 Ω, 430 Ω, 39 Ω, −5.2, 250 μF All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and RB_{SOA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞	TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 50 Ω Pulse Width = 10 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT TUT, 1, Input, 2, 1N4937 or Equivalent, R_{coil}, L_{coil}, V_{clamp}, V_{CC}, R_S = 0.1 Ω See Above for Detailed Conditions	OUTPUT WAVEFORMS I_C, $I_{C(pk)}$, t_f Clamped, t_1, t_f, t V_{CE}, V_{CE} or V_{clamp}, Time, t_2, t t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 1, 2, TUT, R_L, V_{CC}

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

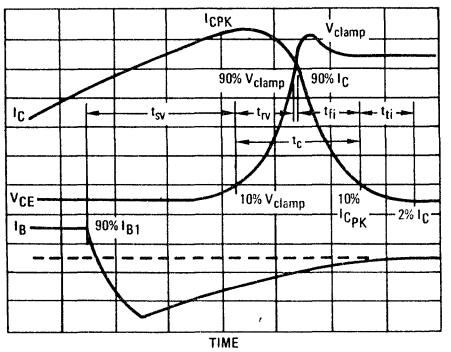
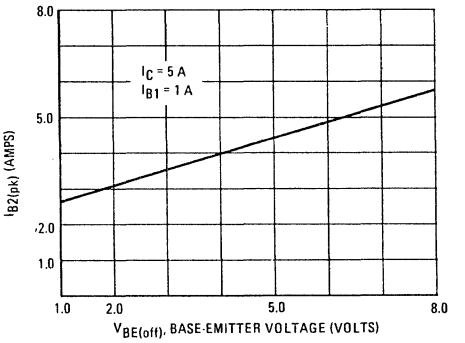


FIGURE 8 – PEAK REVERSE CURRENT



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C(t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

4

RESISTIVE SWITCHING

FIGURE 9 – TURN-ON SWITCHING TIMES

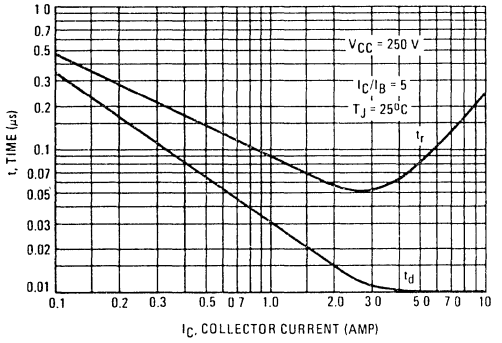


FIGURE 10 – TURN-OFF TIME

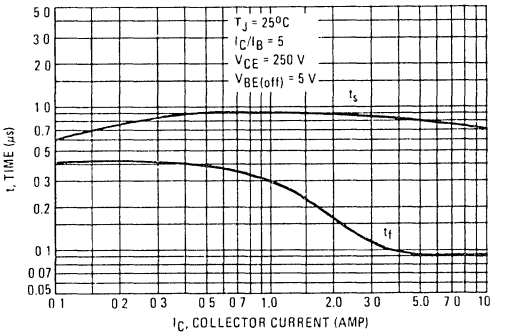
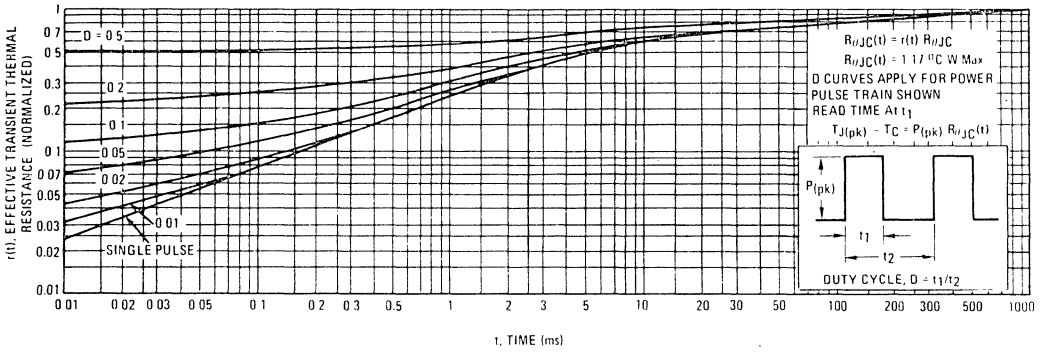


FIGURE 11 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

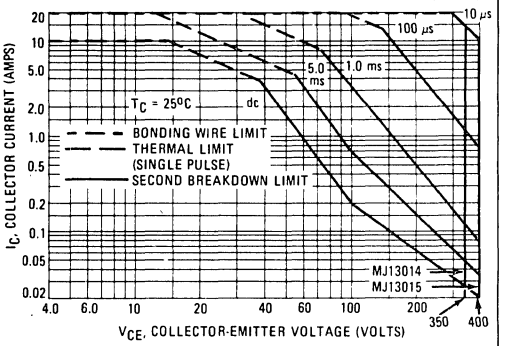
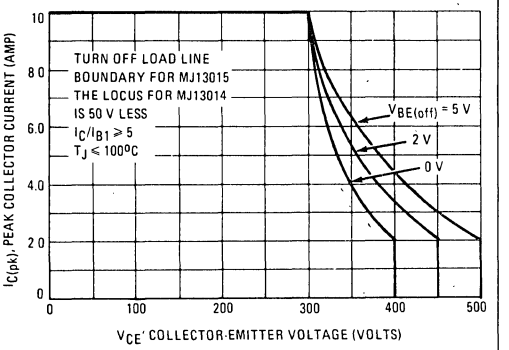


FIGURE 13 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

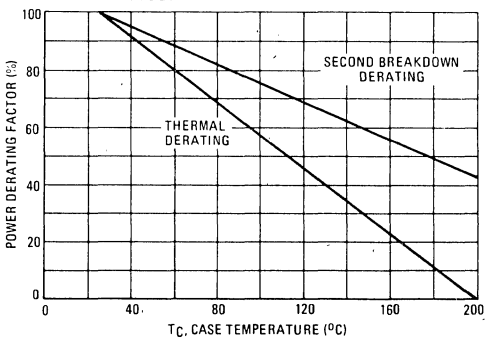
The data of Figure 12 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

FIGURE 14 – POWER DERATING



MJ13330
MJ13331

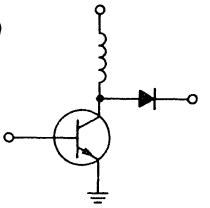
Designers▲ Data Sheet

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTORS

The MJ13330 and MJ13331 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Time
75 ns Inductive Fall Time–25°C (Typ)
150 ns Inductive Crossover Time–25°C (Typ)
900 ns Inductive Storage Time–25°C (Typ)
Operating Temperature Range -65 to +200°C
100°C Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents



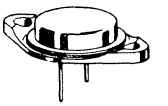
20 AMPERE

NPN SILICON POWER TRANSISTORS

200 and 250 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



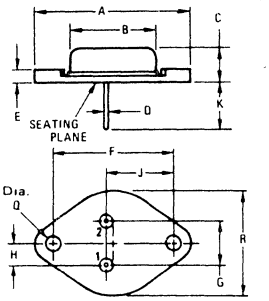
MAXIMUM RATINGS

Rating	Symbol	MJ13330	MJ13331	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	200	250	Vdc
Collector-Emitter Voltage	V_{CEV}	400	450	Vdc
Emitter Base Voltage	V_{EB}	6		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	20 30		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	10 20		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



PIN 1 BASE
2 EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case
CASE 11-01
TO-3

▲ Trademark of Motorola Inc.
Similar device types with higher V_{CEO} ratings are: MJ13332 (350 V) thru MJ13335 (500 V).

4

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage (R_{GK} = 1000 Ohms)	MCR1906-1	V_{DRM}	25	–	–	Volt
	MCR1906-2		50	–	–	
	MCR1906-3		100	–	–	
	MCR1906-4		200	–	–	
	MCR1906-5		300	–	–	
	MCR1906-6		400	–	–	
	MCR1906-7		500			
	MCR1906-8		600			
Peak Forward Blocking Current (Rated V_{DRM}, R_{GK} = 1000 Ohms, T_J = 110°C)		I_{DRM}	–	–	500	μA
Peak Reverse Blocking Current (Rated V_{RRM}, R_{GK} = 1000 Ohms, T_J = 110°C)		I_{RRM}	–	–	500	μA
Peak On-State Voltage (Pulsed, 1.0 ms max, Duty Cycle ≤ 1.0%) (I_F = 1.0 Adc peak)		V_{TM}	–	–	1.75	Volt
Gate Trigger Current (Continuous dc) (V_{AK} = 7.0 V, R_L = 100 ohms)		I_{GT}	–	–	1.0	mAdc
Gate Trigger Voltage (Continuous dc)		V_{GT}				Volt
(V_{AK} = 7.0 V, R_L = 100 ohms)			–	–	1.0	
(V_{AK} = Rated V_{DRM}, R_L = 100 ohms, R_{GK} = 1000 Ohms, T_J = 110°C)			0.1	–	–	
Holding Current (V_{AK} = 7.0 V, R_{GK} = 1000 ohms)		I_H	–	–	5.0	mA
Turn-On Time		t_{gt}				μs
(I_{GT} = 10 mA, I_F = 1.0 A)			–	0.8	–	
(I_{GT} = 20 mA, I_F = 1.0 A)			–	0.6	–	
Turn-Off Time (I_F = 1.0 A, I_R = 1.0 A, dv/dt = 20 V/μs, T_J = 110°C)		t_q	–	10	–	μs

CURRENT DERATING

FIGURE 1 – CASE TEMPERATURE REFERENCE

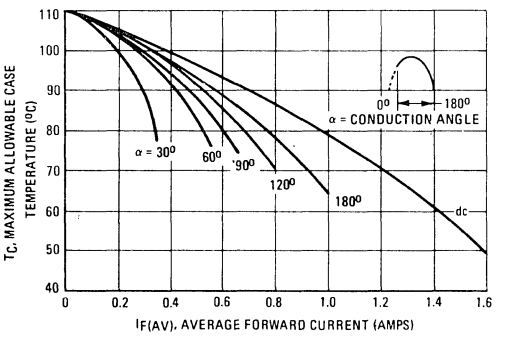


FIGURE 2 – AMBIENT TEMPERATURE REFERENCE

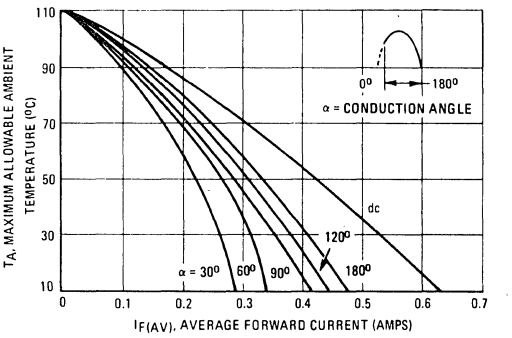


FIGURE 1 – DC CURRENT GAIN

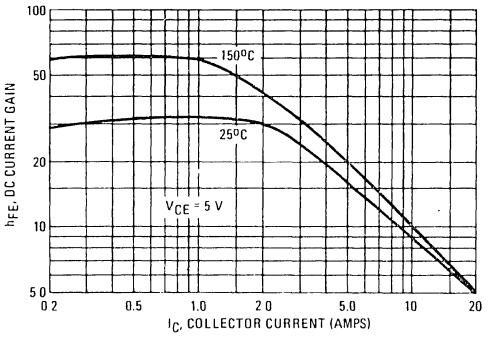


FIGURE 2 – COLLECTOR SATURATION REGION

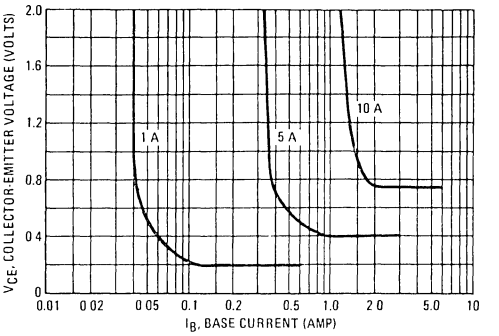


FIGURE 3 – COLLECTOR-EMITTER SATURATION REGION

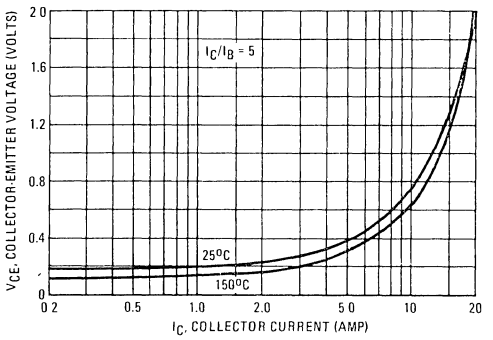


FIGURE 4 – BASE-EMITTER VOLTAGE

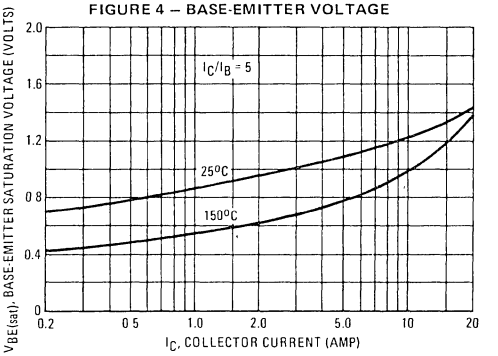


FIGURE 5 – COLLECTOR CUTOFF REGION

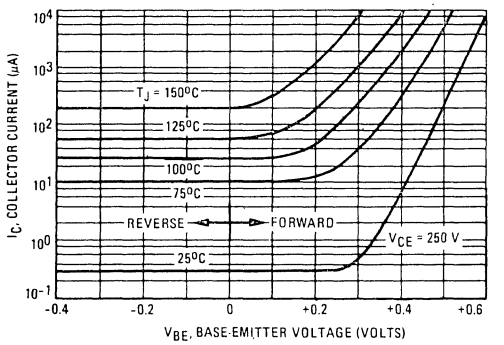
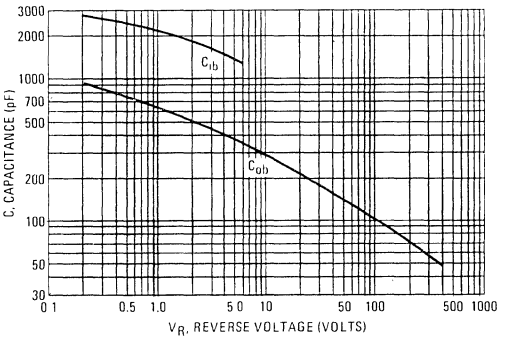


FIGURE 6 – CAPACITANCE



4

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

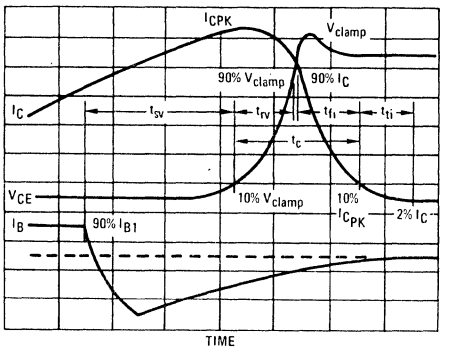
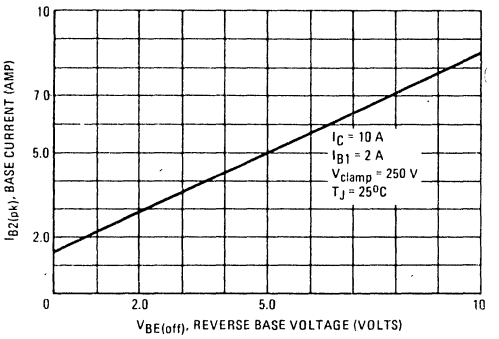


FIGURE 8 – REVERSE BASE CURRENT versus $V_{BE(off)}$ WITH NO EXTERNAL BASE RESISTANCE



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON SWITCHING TIMES

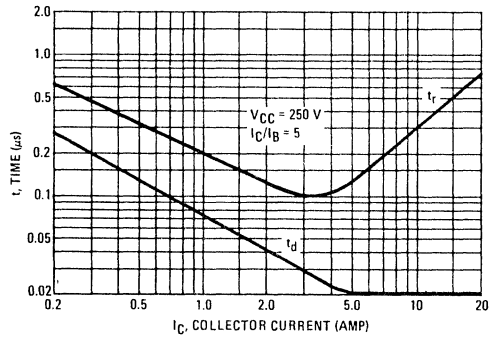


FIGURE 10 – TURN-OFF SWITCHING TIMES

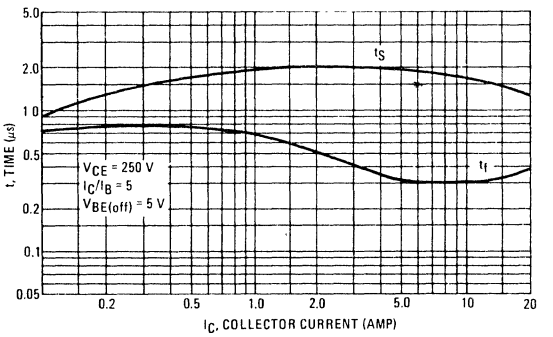


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V, 20, 0, 1, 2 PW Varied to Attain I_C = 100 mA	250 μF, 470 Ω 2 W, 47 Ω, R1, +15, 15 V, 0, 330 Ω, 5 1 Ω 5 W, R2, 50 Ω, 100 Ω, 430 Ω, 39 Ω, -5 2, 250 μF All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and RBSOA, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞	TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0 7 Ω	L_{coil} = 180 μH R_{coil} = 0 05 Ω V_{CC} = 20 V V_{clamp} = 200 V	V_{CC} = 175 V R_L = 17 5 Pulse Width = 25 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT TUT, 1, Input, 1N4937 or Equivalent, R_{coil}, L_{coil}, V_{clamp}, V_{CC}, 2, R_S = 0 1 Ω See Above for Detailed Conditions	OUTPUT WAVEFORMS I_C, $I_{C(pk)}$, t_f Clamped, t_1, t_f, t, V_{CE}, V_{CE} or V_{clamp}, Time, t_2 t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 1, 2, TUT, R_L, V_{CC}

FIGURE 11 – THERMAL RESPONSE

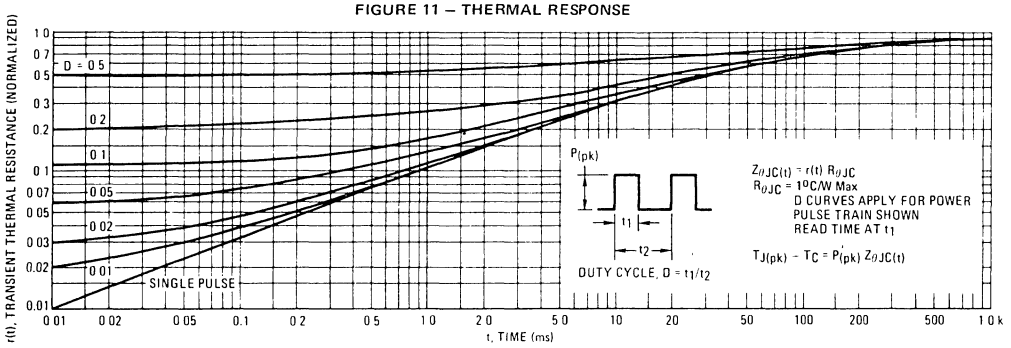


FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

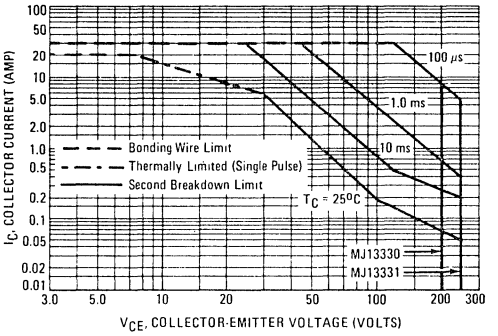
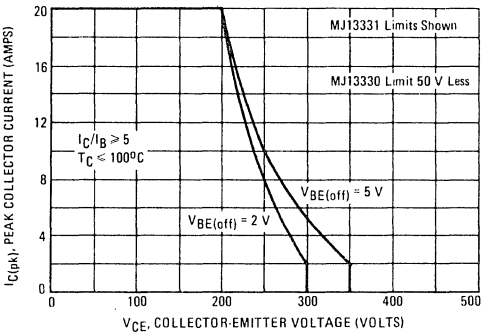


FIGURE 13 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

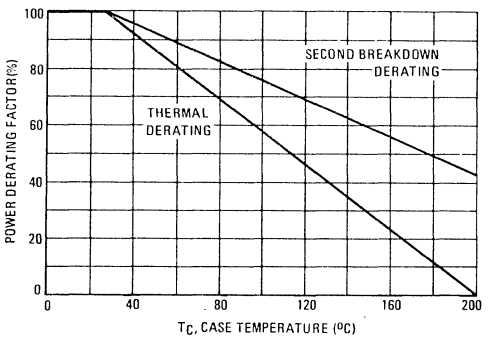
The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 – POWER DERATING



MJ13332 MJ13334
MJ13333 MJ13335

Designer's Data Sheet

SWITCHMODE△ SERIES
NPN SILICON POWER TRANSISTORS

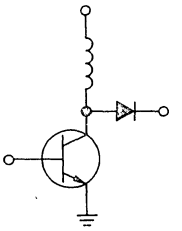
The MJ13332 through MJ13335 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn-Off Times
- 200 ns Inductive Fall Time—25°C (Typ)
- 1.8 μs Inductive Storage Time—25°C (Typ)

Operating Temperature Range −65 to +200°C

100°C Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



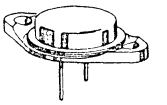
20 AMPERE

NPN SILICON POWER TRANSISTORS

350–500 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers△ Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



MAXIMUM RATINGS

Rating	Symbol	MJ13332	MJ13333	MJ13334	MJ13335	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	450	500	Vdc
Collector-Emitter Voltage	V_{CEV}	650	700	750	800	Vdc
Emitter Base Voltage	V_{EB}	6.0				Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	20 30				Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	10 15				Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1.0				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +200				°C

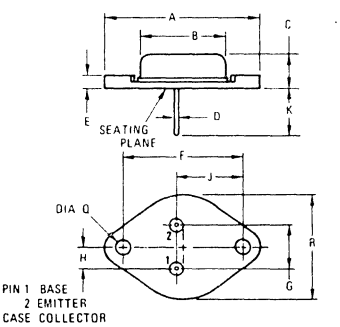
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Similar device types available with lower V_{CEO} ratings, see the MJ13330 (200 V) and MJ13331 (250 V).

△Trademark of Motorola Inc.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case
CASE 11-01
TO-3

4

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (Table 1)	$V_{CEO(sus)}$				Vdc
(I_C = 100 mA, I_B = 0) MJ13330		200	–	–	
MJ13331		250	–	–	
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		–	–	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		–	–	5	
Collector Cutoff Current	I_{CER}	–	–	5	mAdc
(V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)					
Emitter Cutoff Current	I_{EBO}	–	–	0.5	mAdc
(V_{EB} = 6 Vdc, I_C = 0)					
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with base reverse biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain	h_{FE}				–
(I_C = 5 Adc, V_{CE} = 5 Vdc)		15	–	75	
(I_C = 10 Adc, V_{CE} = 5 Vdc)		8.0	–	40	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 1.5 Adc)		–	–	1.5	
(I_C = 20 Adc, I_B = 5 Adc)		–	–	3.5	
(I_C = 10 Adc, I_B = 1.8 Adc, T_C = 100°C)		–	–	2.5	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 1.5 Adc)		–	–	1.8	
(I_C = 10 Adc, I_B = 1.8 Adc, T_C = 100°C)		–	–	1.8	
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 300 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	5	–	40	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	100	–	400	pF
SWITCHING CHARACTERSITICS					
Resistive Load (Table 1)					
Delay Time	t_d	–	0.08	0.20	μs
Rise Time (V_{CC} = 175 Vdc, I_C = 10 A, I_{B1} = 1.5 Adc,	t_r	–	0.55	1.0	μs
Storage Time $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%)	t_s	–	0.70	3.5	μs
Fall Time	t_f	–	0.11	0.7	μs
Inductive Load, Clamped (Table 1)					
Storage Time (I_C = 10 A(pk), V_{clamp} = 200 Vdc, I_{B1} = 1.8 Adc,	t_{sv}	–	1.35	4.5	μs
Crossover Time $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_c	–	0.45	1.8	μs
Storage Time (I_C = 10 A(pk), V_{clamp} = 200 Vdc, I_{B1} = 1.5 Adc,	t_{sv}	–	0.90	–	μs
Crossover Time $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_c	–	0.15	–	μs
Fall Time	t_{fi}	–	0.075	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

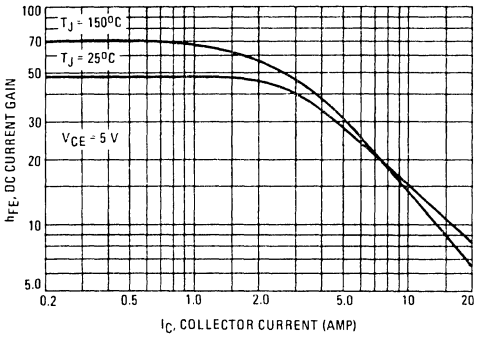


FIGURE 2 – COLLECTOR SATURATION REGION

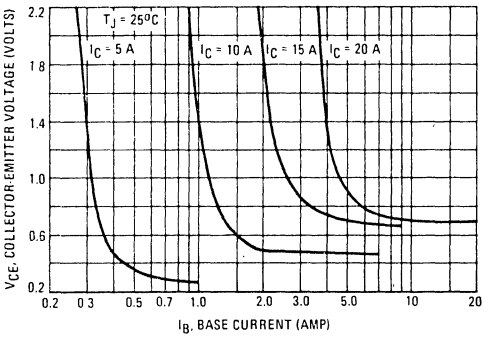


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

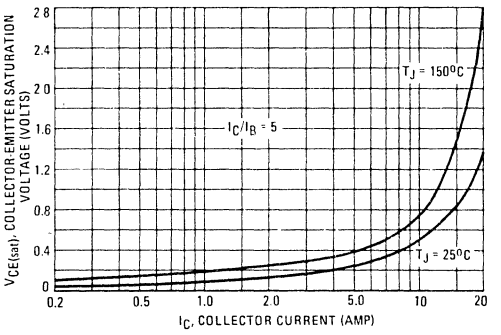


FIGURE 4 – BASE-EMITTER VOLTAGE

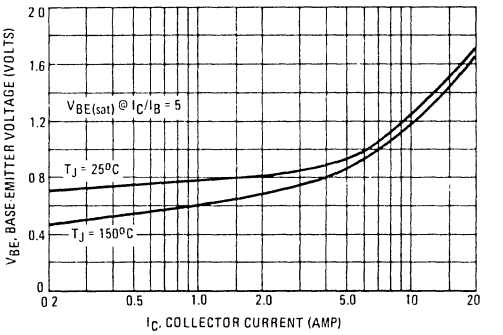


FIGURE 5 – COLLECTOR CUTOFF REGION

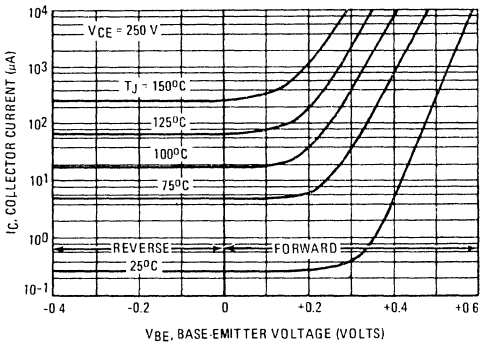
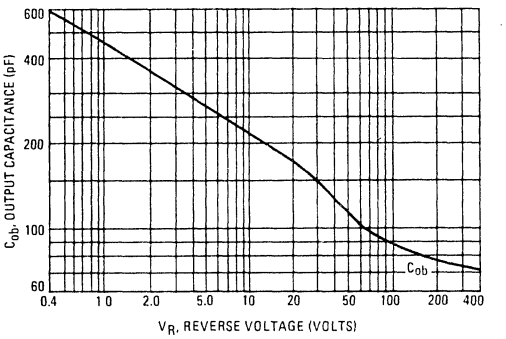


FIGURE 6 – OUTPUT CAPACITANCE



4

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

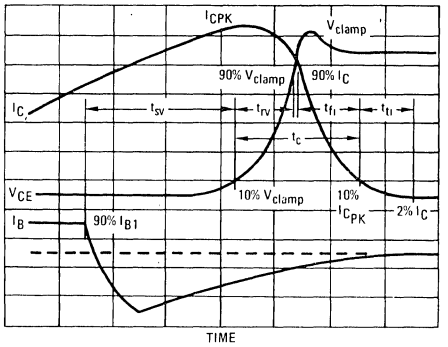
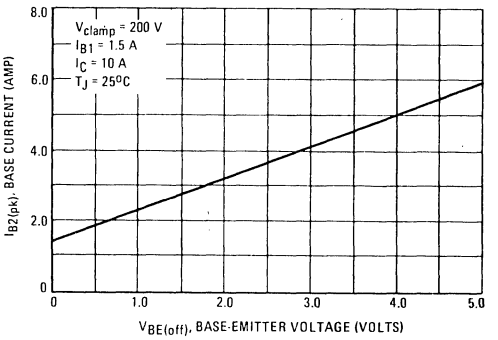


FIGURE 8 – REVERSE BASE CURRENT versus BASE EMITTER VOLTAGE



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING

FIGURE 9 – TURN-ON TIME

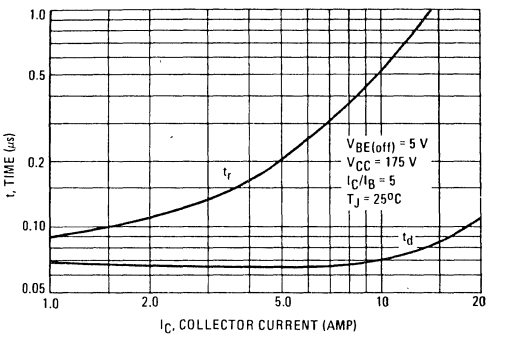


FIGURE 10 – TURN-OFF TIME

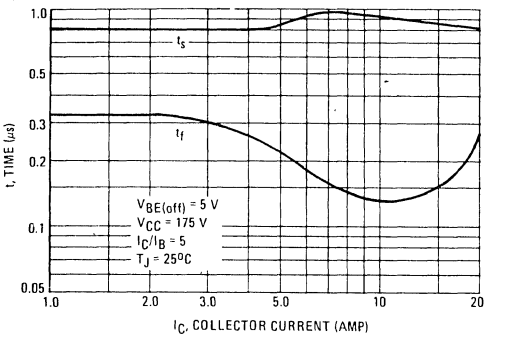


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V, 20, 0, 1, 2 PW Varied to Attain I_C = 100 mA	250 µF, 470 Ω 2 W, 47 Ω, R1, +15, 15 V, 0, 330 Ω, 5.1 Ω 5 W, R2, 50 Ω, 100 Ω, 430 Ω, 39 Ω, 250 µF, −5.2 All Diodes – 1N4934 All NPN – MJE200 All PNP – MJE210 Adjust R1 to obtain I_{B1} For switching and RBS_{OA}, R2 = 0 For $BV_{CEO(sus)}$, R2 = ∞	TURN ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN OFF TIME Use inductive switching driver as the input to the resistive test circuit
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} 250 V R_L = 50 Ω Pulse Width = 10 µs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT TUT, 1, Input, 1N4937 or Equivalent, See Above for Detailed Conditions, V_{clamp}, R_{coil}, L_{coil}, V_{CC}, 2, R_S = 0.1 Ω	OUTPUT WAVEFORMS I_C, $I_{C(pk)}$, t_f Clamped, t_1, t_f, t, V_{CE}, V_{CE} or V_{clamp}, Time, t_2 t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 1, 2, TUT, R_L, V_{CC}

FIGURE 11 – THERMAL RESPONSE

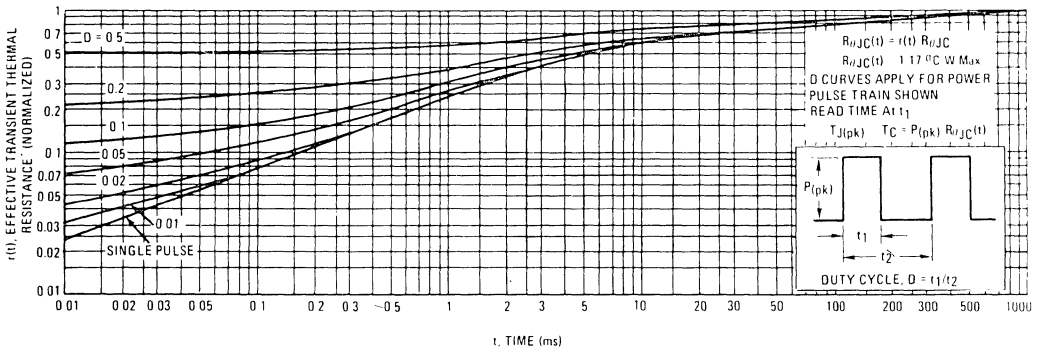


FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

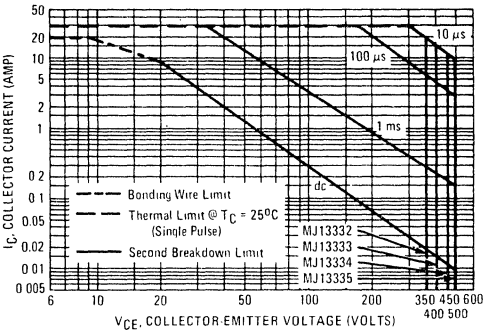
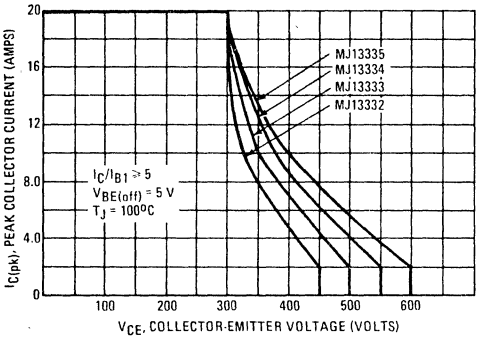


FIGURE 13 – RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

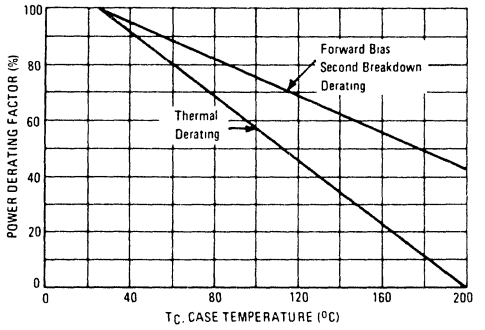
The data of Figure 12 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

FIGURE 14 – POWER DERATING



NPN PNP

MJ14000 MJ14001
MJ14002 MJ14003

Advance Information

HIGH-CURRENT COMPLEMENTARY SILICON POWER TRANSISTORS

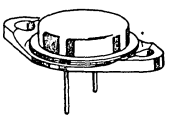
. . . designed for use in high-power amplifier and switching circuit applications.

- High Current Capability — I_C Continuous = 70 Amperes
- DC Current Gain — h_{FE} = 15-100 @ I_C = 50 Adc
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 2.5 Vdc (Max) @ I_C = 50 Adc

70 AMPERES

COMPLEMENTARY SILICON POWER TRANSISTORS

60-80 VOLTS
300 WATTS



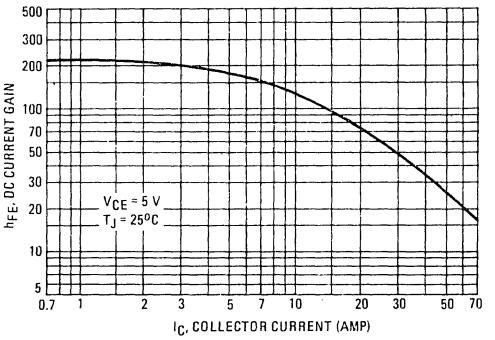
MAXIMUM RATINGS

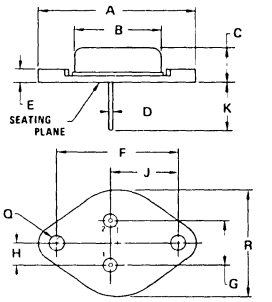
Rating	Symbol	MJ14000 MJ14001	MJ14002 MJ14003	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CBO}	60	80	Vdc
Emitter-Base Voltage	V_{EBO}	5		Vdc
Collector Current — Continuous	I_C	70		Adc
Base Current — Continuous	I_B	15		Adc
Emitter Current — Continuous	I_E	85		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.7		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.584	°C/W

FIGURE 1 — DC CURRENT GAIN





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO-3

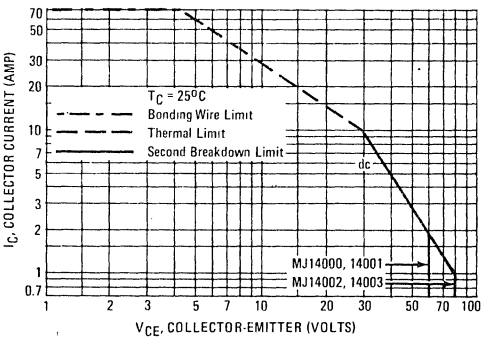
This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	MJ14000, MJ14001		60	–	
	MJ14002, MJ14003		80	–	
Collector Cutoff Current		I_{CEO}			mA
(V_{CE} = 30 Vdc, I_B = 0)	MJ14000, MJ14001		–	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	MJ14002, MJ14003		–	1.0	
Collector Cutoff Current		I_{CEX}			mA
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 V)	MJ14000, MJ14001		–	1.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 V)	MJ14002, MJ14003		–	1.0	
Collector Cutoff Current		I_{CBO}			mA
(V_{CB} = 60 Vdc, I_E = 0)	MJ14000, MJ14001		–	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	MJ14002, MJ14003		–	1.0	
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	–	1.0	mA
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 25 Adc, V_{CE} = 3 V)			30	–	
(I_C = 50 Adc, V_{CE} = 3 V)			15	100	
(I_C = 70 Adc, V_{CE} = 3 V)			5	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 2.5 Adc)			–	1	
(I_C = 50 Adc, I_B = 5 Adc)			–	2.5	
(I_C = 70 Adc, I_B = 14 Adc)			–	3	
Base-Emitter Saturation Voltage (1)		$V_{BE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 2.5 Adc)			–	2	
(I_C = 50 Adc, I_B = 5 Adc)			–	3	
(I_C = 70 Adc, I_B = 14 Adc)			–	4	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	2000	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

FIGURE 2 – DC SAFE OPERATING AREA



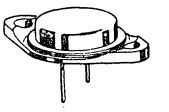
NPN
MJ15001
PNP
MJ15002

COMPLEMENTARY SILICON POWER TRANSISTORS

The MJ15001 and MJ15002 are EPIBASE▲ power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) –
  200 W @ 40 V
  50 W @ 100 V
- For Low Distortion Complementary Designs
- High DC Current Gain –
  h_{FE} = 25 (Min) @ I_C = 4 Adc

15 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
140 VOLTS
200 WATTS



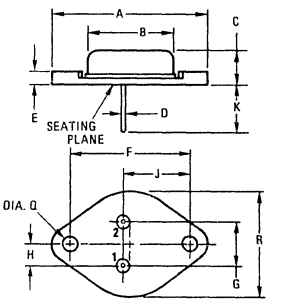
4

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	140	Vdc
Collector-Base Voltage	V_{CBO}	140	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector Current – Continuous	I_C	15	Adc
Base Current – Continuous	I_B	5	Adc
Emitter Current – Continuous	I_E	20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/16" from Case for ≤10s.	T_L	265	°C



PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
TO-3

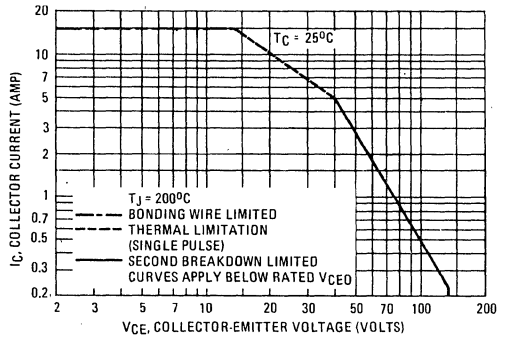
▲Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	–	Vdc
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	–	100	μAdc
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			2	mAdc
Collector Cutoff Current (V_{CE} = 140 Vdc, I_B = 0)	I_{CEO}	–	250	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1 s (non-repetitive))	$I_{S/b}$	5	–	Adc
(V_{CE} = 100 Vdc, t = 1 s (non-repetitive)		0.5	–	
ON CHARACTERISTICS				
DC Current Gain (I_C = 4 Adc, V_{CE} = 2 Vdc)	h_{FE}	25	150	–
Collector-Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	–	1	Vdc
Base-Emitter On Voltage (I_C = 4 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	–	2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 0.5 MHz)	f_T	2	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	–	1000	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

FIGURE 2 – CAPACITANCES

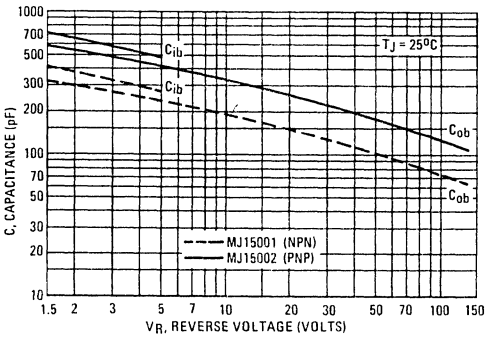
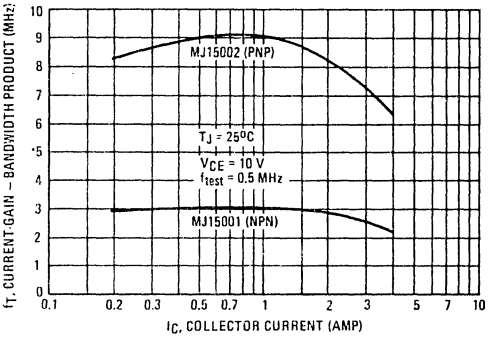


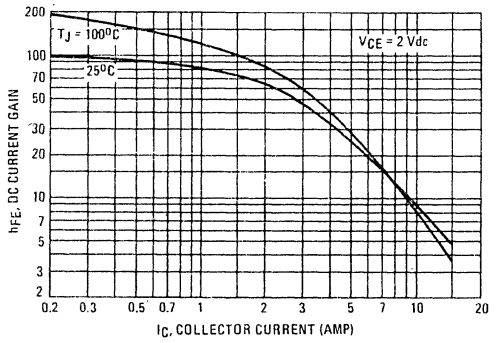
FIGURE 3 – CURRENT-GAIN – BANDWIDTH PRODUCT



4

FIGURE 4 – DC CURRENT GAIN

MJ15001



MJ15002

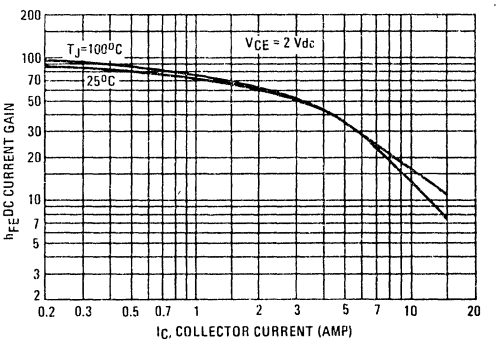
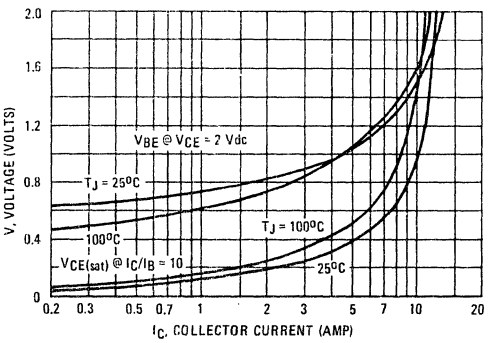


FIGURE 5 – "ON" VOLTAGE

MJ15001



MJ15002

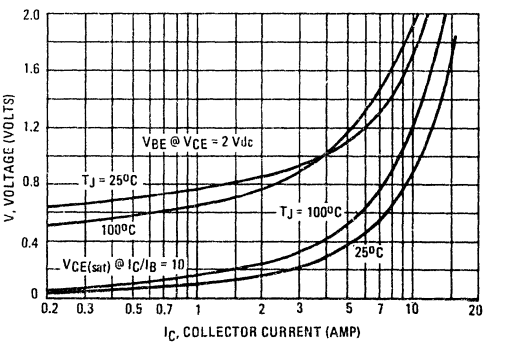
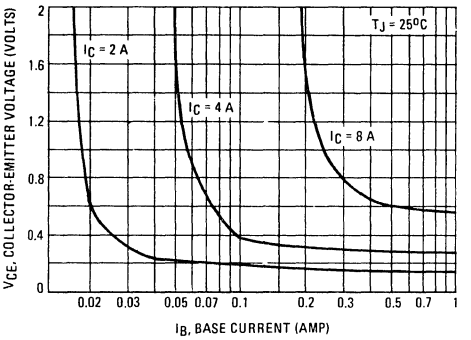
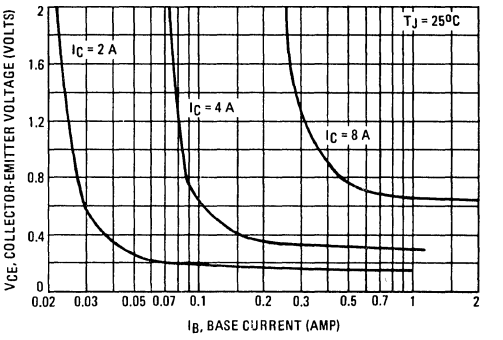


FIGURE 6 – COLLECTOR SATURATION REGION

MJ15001



MJ15002



4

MJ15003 NPN
MJ15004 PNP

COMPLEMENTARY SILICON POWER TRANSISTORS

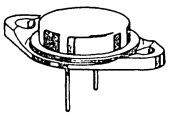
The MJ15003 and MJ15004 are EPIBASE power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) – 250 W @ 50 V
- For Low Distortion Complementary Designs
- High DC Current Gain – h_{FE} = 25 (Min) @ I_C = 5 Adc

20 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

140 VOLTS
250 WATTS

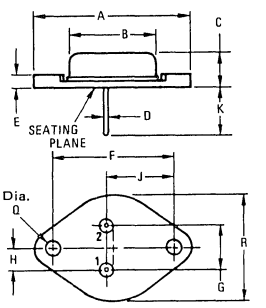


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	140	Vdc
Collector-Base Voltage	V_{CBO}	140	Vdc
Emitter-Base Voltage	V_{EBO}	5	Vdc
Collector Current – Continuous	I_C	20	Adc
Base Current – Continuous	I_B	5	Adc
Emitter Current – Continuous	I_E	25	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/16" from Case for ≤10s.	T_L	265	°C



PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

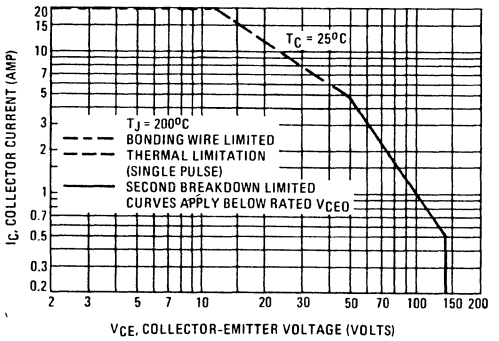
Collector connected to case.
CASE 11-01
TO-3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	–	Vdc
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	–	100	μAdc
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		–	2	mAdc
Collector Cutoff Current (V_{CE} = 140 Vdc, I_B = 0)	I_{CEO}	–	250	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 1 s (non-repetitive)	$I_{S/b}$	5	–	Adc
(V_{CE} = 100 Vdc, t = 1 s (non-repetitive)		1	–	
ON CHARACTERISTICS				
DC Current Gain (I_C = 5 Adc, V_{CE} = 2 Vdc)	h_{FE}	25	150	
Collector-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.5 Adc)	$V_{CE(sat)}$	–	1	Vdc
Base-Emitter On Voltage (I_C = 5 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	–	2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 0.5 MHz)	f_T	2	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	–	1000	pF

(1) Pulse Test. Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

FIGURE 2 – CAPACITANCES

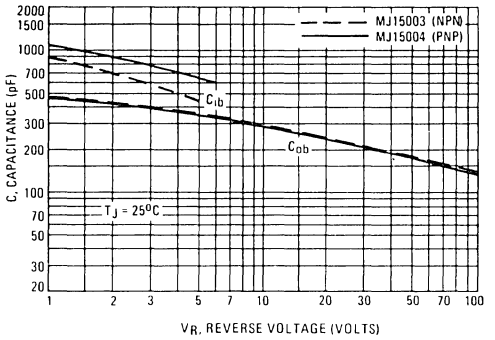


FIGURE 3 – CURRENT GAIN – BANDWIDTH PRODUCT

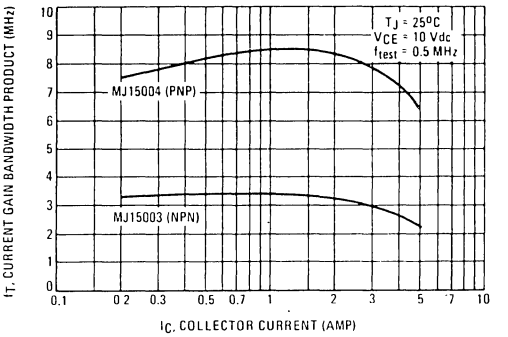
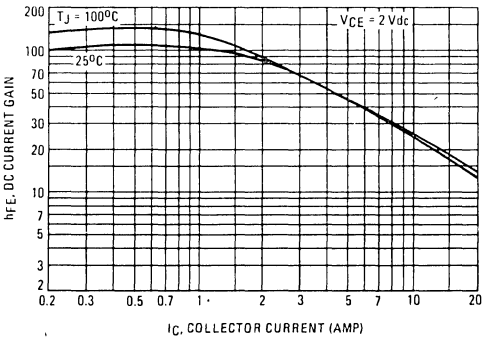


FIGURE 4 – DC CURRENT GAIN

MJ15003



MJ15004

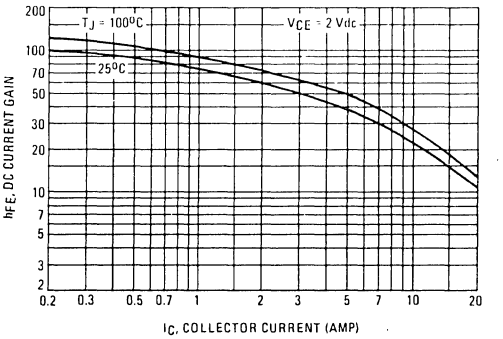
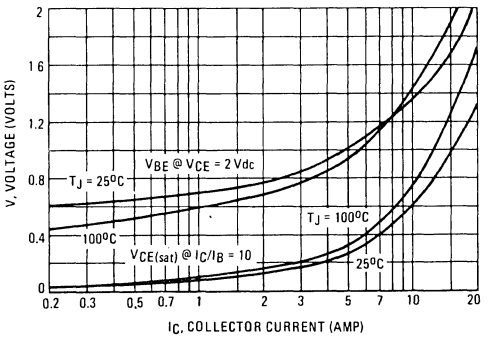


FIGURE 5 – "ON" VOLTAGE

MJ15003



MJ15004

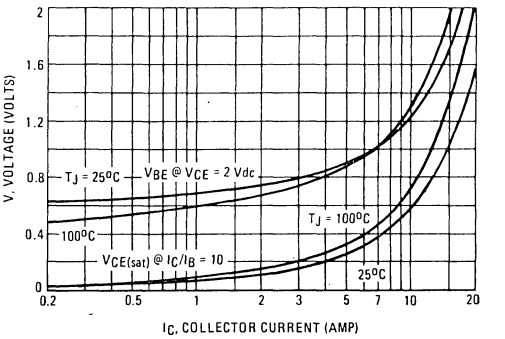
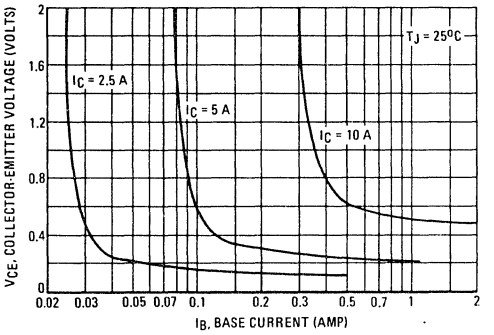
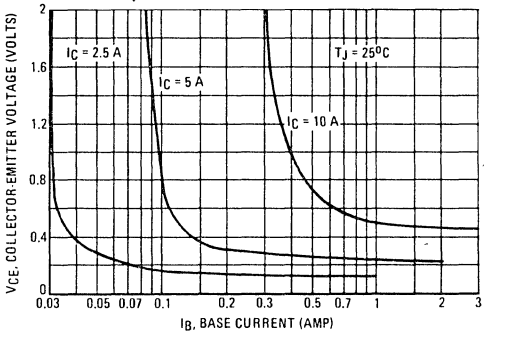


FIGURE 6 – COLLECTOR SATURATION VOLTAGE

MJ15003



MJ15004



4

NPN PNP

MJ15011 MJ15012

Advance Information

COMPLEMENTARY SILICON POWER TRANSISTORS

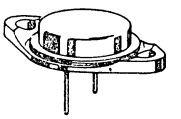
The MJ15011 and MJ15012 are Power Base power transistors designed for high-power audio, disk head positioners, and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc-to-dc converters or inverters.

- High Safe Operating Area (100% Tested)
  1.2 A @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage
  h_{FE} = 20 (Min) @ 2 A, 2 V
  $V_{CE(sat)}$ = 2.5 V (Max) @ I_C = 4 A, I_B = 0.4 A
- For Low Distortion Complementary Designs

10 AMPERE

COMPLEMENTARY POWER TRANSISTORS

250 VOLTS
200 WATTS



4

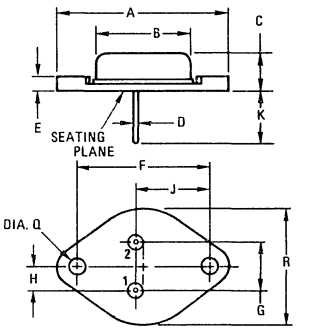
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	250	Vdc
Collector-Emitter Voltage	V_{CEX}	250	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 15	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 5	Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	12 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	°C/W
Maximum Lead Temperature for Soldering Purposes	T_L	265	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	—	3.43	—	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	—	26.67	—	1.050

Collector connected to case.
CASE 11-01
(TO-3)

This is advance information and specifications are subject to change without notice.
Power Base is a trademark of Motorola.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 100 mA)	$V_{CEO(sus)}$	250	–	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc)	I_{CEO}	–	1	mAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	–	500	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc)	I_{EBO}	–	500	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 2 Adc, V_{CE} = 2 Vdc) (I_C = 4 Adc, V_{CE} = 2 Vdc)	h_{FE}	 20 5	 100 –	–
Collector-Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.2 Adc) (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	 – –	 0.8 2.5	Vdc
Base-Emitter On Voltage (I_C = 4 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	–	2	Vdc
DYNAMIC CHARACTERISTICS				
Output Capacitance (V_{CB} = 10 Vdc, f = 1 MHz)	C_{ob}	–	250	pF
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 0.5 s) (V_{CE} = 100 Vdc, t = 0.5 s)	$I_{S/b}$	 4 1.2	 – –	Adc

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 – DC CURRENT GAIN

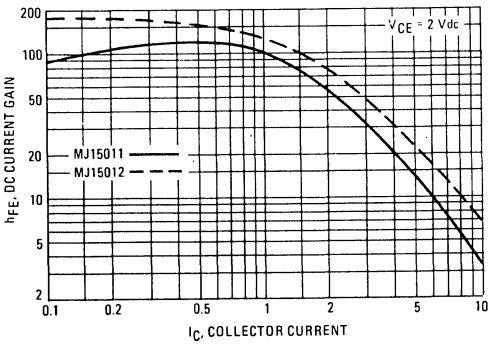
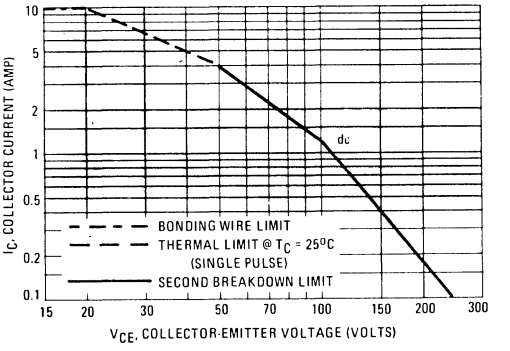


FIGURE 2 – ACTIVE REGION SAFE OPERATING AREA



NPN
MJ15022
MJ15024

SILICON POWER TRANSISTORS

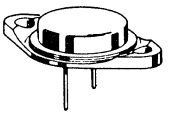
The MJ15022 and MJ15024 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) – 2 A @ 80 V
- High DC Current Gain – h_{FE} = 15 (Min) @ I_C = 8 Adc

16 AMPERE

SILICON POWER TRANSISTORS

200 and 250 VOLTS
250 WATTS



4

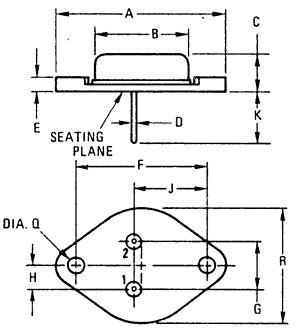
MAXIMUM RATINGS

Rating	Symbol	MJ15022	MJ15024	Unit
Collector-Emitter Voltage	V_{CEO}	200	250	Vdc
Collector-Base Voltage	V_{CBO}	350	400	Vdc
Emitter-Base Voltage	V_{EBO}	7		Vdc
Collector-Emitter Voltage	V_{CEX}	400		Vdc
Collector Current – Continuous Peak (1)	I_C	16 30		Adc
Base Current – Continuous	I_B	5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	°C/W

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTE:
1. DIM "Q" IS DIA.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

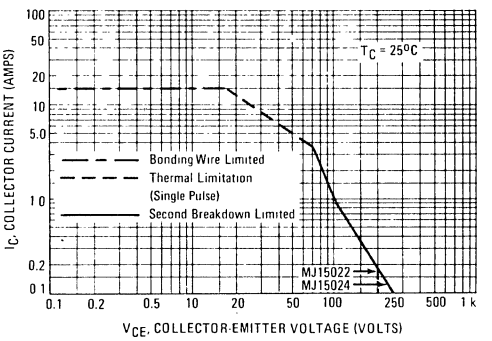
Collector connected to case.
CASE 11-01
(TO-3)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			
(I_C = 100 mAdc, I_B = 0)	MJ15022		200	–	
	MJ15024		250	–	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	MJ15022		–	250	μAdc
(V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	MJ15024		–	250	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 150 Vdc, I_B = 0)	MJ15022		–	500	
(V_{CE} = 200 Vdc, I_B = 0)	MJ15024		–	500	
Emitter Cutoff Current		I_{EBO}	–	500	μAdc
(V_{CE} = 7 Vdc, I_B = 0)	Both				
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$			Adc
(V_{CE} = 50 Vdc, t = 0.5 s (non-repetitive))			5	–	
(V_{CE} = 80 Vdc, t = 0.5 s (non-repetitive))			2	–	
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 8 Adc, V_{CE} = 4 Vdc)			15	60	
(I_C = 16 Adc, V_{CE} = 4 Vdc)			5	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 8 Adc, I_B = 0.8 Adc)			–	1.4	
(I_C = 16 Adc, I_B = 3.2 Adc)			–	4.0	
Base-Emitter On Voltage		$V_{BE(on)}$	–	2.2	Vdc
(I_C = 8 Adc, V_{CE} = 4 Vdc)					
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	4	–	MHz
(I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)					
Output Capacitance		C_{ob}	–	500	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)					

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

FIGURE 2 – CAPACITANCES

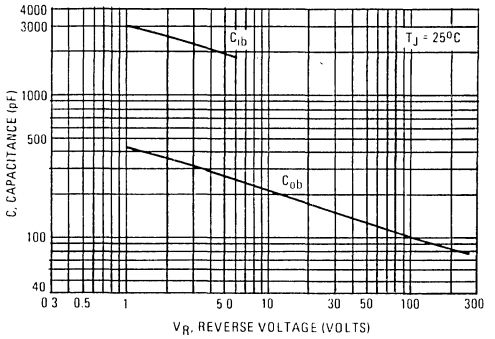


FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

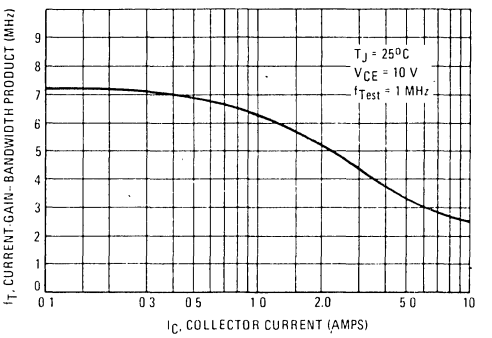


FIGURE 4 – DC CURRENT GAIN

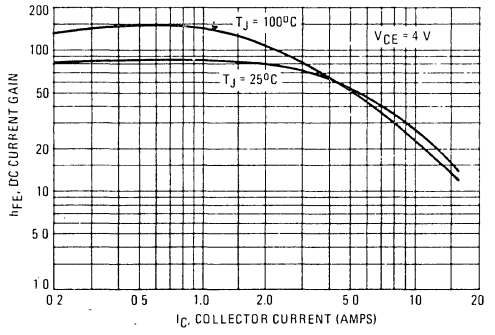


FIGURE 5 – "ON" VOLTAGE

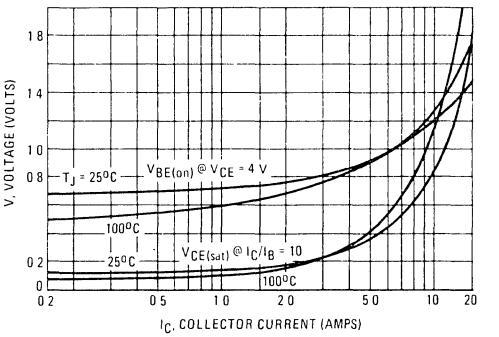
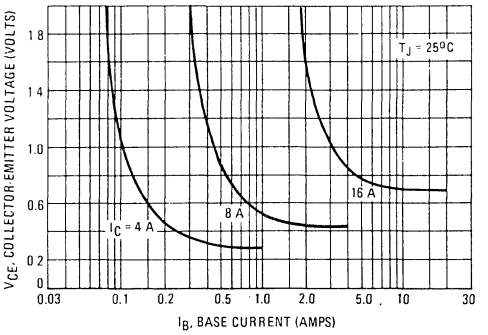


FIGURE 6 – COLLECTOR SATURATION REGION



MJE51T thru MJE53T

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

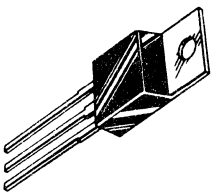
. . . designed for high voltage inverters, switching regulators and line-operated amplifier applications. Especially well suited for switching power supply applications.

- Intended as Economical Substitutes for the Electrically Similar TIP51 thru TIP53 Series
- High Collector-Emitter Sustaining Voltage @ 25 mAdc
  $V_{CEO(sus)}$ = 250 V(min) – MJE51T
  = 300 V(min) – MJE52T
  = 350 V(min) – MJE53T

5 AMPERE

POWER TRANSISTORS NPN SILICON

250, 300, 350 VOLTS 80 WATTS



4

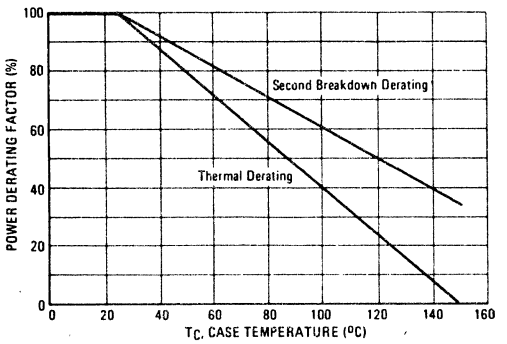
MAXIMUM RATINGS

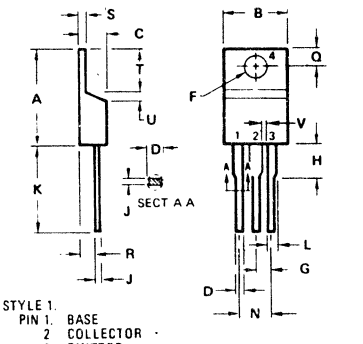
Rating	Symbol	MJE51T	MJE52T	MJE53T	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	350	Vdc
Collector-Base Voltage	V_{CB}	350	400	450	Vdc
Emitter-Base Voltage	V_{EB}	6.0			Vdc
Collector Current – Continuous – Peak	I_C	5.0 10			Adc
Base Current	I_B	2.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.64			Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W

FIGURE 1 – POWER DERATING





STYLE 1.
PIN 1. BASE
2 COLLECTOR
3 EMITTER
4. COLLECTOR

NOTE
1 DIM L & H APPLIES TO ALL LEADS

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0 014	0 022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0 050
V	1 14	–	0.045	–

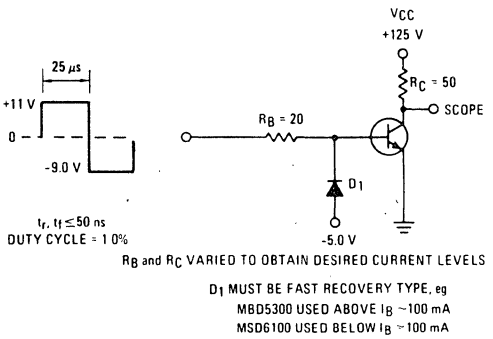
CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Charactoristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$				Vdc
(I_C = 25 mAdc, I_B = 0)	MJE51T		250	–	–	
	MJE52T		300	–	–	
	MJE53T		350	–	–	
Collector Cutoff Current		I_{CEO}				mAdc
(V_{CE} = 150 Vdc, I_B = 0)	MJE51T		–	–	1.0	
(V_{CE} = 200 Vdc, I_B = 0)	MJE52T		–	–	1.0	
(V_{CE} = 250 Vdc, I_B = 0)	MJE53T		–	–	1.0	
Collector Cutoff Current		I_{CES}				mAdc
(V_{CE} = 350 Vdc, V_{BE} = 0)	MJE51		–	–	1.0	
(V_{CE} = 400 Vdc, V_{BE} = 0)	MJE52		–	–	1.0	
(V_{CE} = 450 Vdc, V_{BE} = 0)	MJE53		–	–	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	–	1.0	mAdc
ON CHARACTERISTICS						
DC Current Gain(1)		h_{FE}				–
(I_C = 0.3 Adc, V_{CE} = 10 Vdc)			30	–	–	
(I_C = 5.0 Adc, V_{CE} = 10 Vdc)			5.0	–	–	
Collector-Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 2.0 Adc)		$V_{CE(sat)}$	–	–	2.0	Vdc
Base-Emitter On Voltage (I_C = 5.0 Adc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	–	2.0	Vdc
DYNAMIC CHARACTERISTICS						
Small-Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	2.5	–	–	–
Small-Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	30	–	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	–	150	pF
SWITCHING CHARACTERISTICS						
Turn-On Time (V_{CC} = 125 Vdc, $V_{BE(off)}$ = 5.0 Vdc, I_C = 2.5 Adc, I_{B1} = I_{B2} = 0.5 Adc)		t_{on}	–	0.5	–	μs
Turn-Off Time (V_{CC} = 125 Vdc, I_C = 2.5 Adc, $V_{BE(off)}$ = 5.0 Vdc, I_{B1} = I_{B2} = 0.5 Adc)		t_{off}	–	2.0	–	μs

(1)Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%

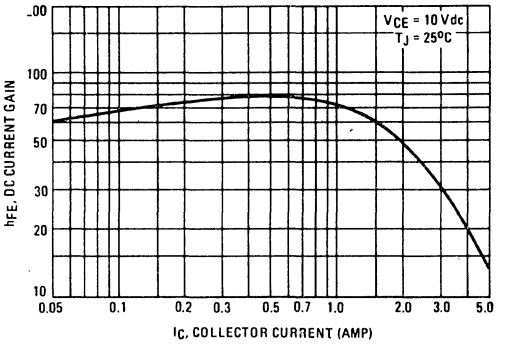
FIGURE 2 – SWITCHING TIME TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

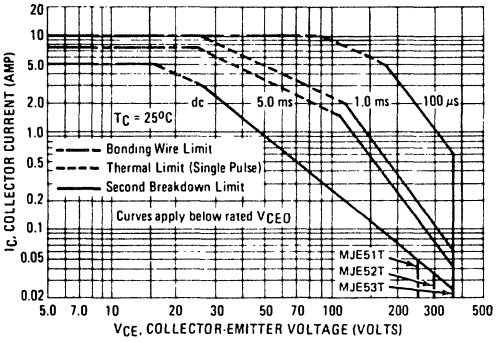
D1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE IB ~100 mA
MSD6100 USED BELOW IB ~100 mA

FIGURE 3 – DC CURRENT GAIN



4

FIGURE 4 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^oC$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 4 may be found at any case temperature by using the appropriate curve on Figure 1.

MJE105 (SILICON)

MEDIUM-POWER PNP SILICON TRANSISTOR

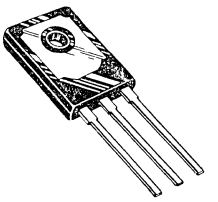
. . . for use as an output device in complementary audio amplifiers up to 20-Watts music power per channel.

- High DC Current Gain – h_{FE} = 25-100 @ I_C = 2.0 A
- Thermopad High-Efficiency Compact Package
- Complementary to NPN MJE205

5 AMPERE POWER TRANSISTOR

PNP SILICON

50 VOLTS
65 WATTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	5.0	Adc
Base Current	I_B	2.5	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D(1)	65 0.522	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

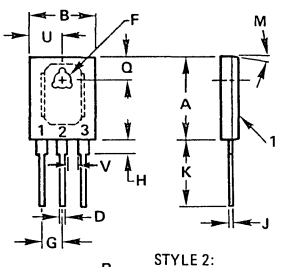
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.92	°C/W

(1) Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (2) (I_C = 100 mAdc, I_B = 0)	BV_{CEO}	50	–	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0) (V_{CB} = 50 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	– –	0.1 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	–
Base-Emitter Voltage (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	V_{BE}	–	1.2	Vdc

(2) Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

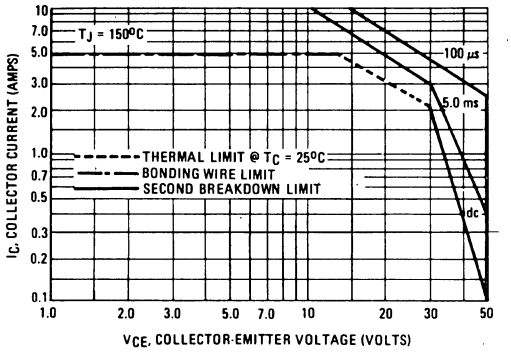


STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05
TO-127

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 – "ON" VOLTAGES

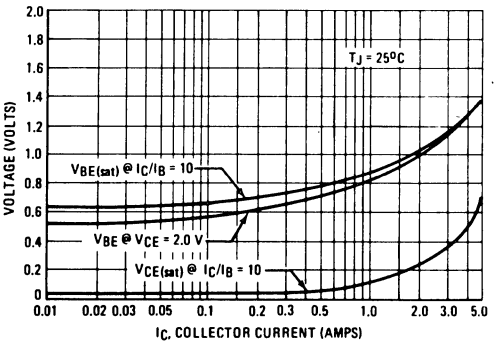


FIGURE 3 – DC CURRENT GAIN

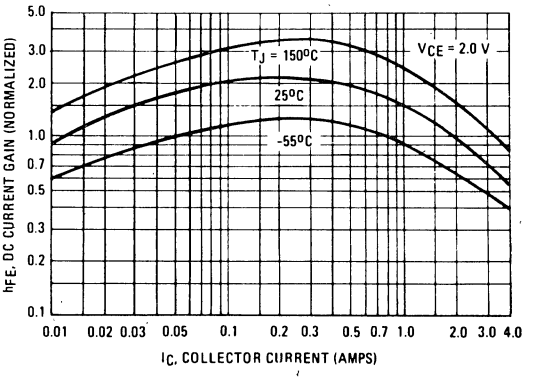
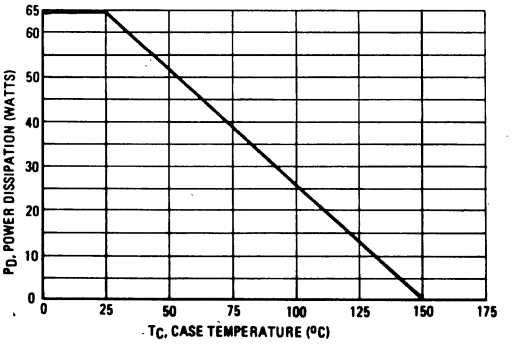


FIGURE 4 – POWER DERATING



MJE170 thru MJE172 PNP (SILICON)
MJE180 thru MJE182 NPN

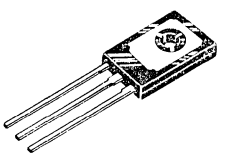
COMPLEMENTARY PLASTIC SILICON POWER TRANSISTORS

. . . designed for low power audio amplifier and low current, high speed switching applications.

- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 40 Vdc – MJE170, MJE180
  = 60 Vdc – MJE171, MJE181
  = 80 Vdc – MJE172, MJE182
- DC Current Gain –
  h_{FE} = 30 (Min) @ I_C = 0.5 Adc
  = 12 (Min) @ I_C = 1.5 Adc
- Current-Gain – Bandwidth Product –
  f_T = 50 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakages –
  I_{CBO} = 100 nA (Max) @ Rated V_{CB}

3 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON

40-60-80 VOLTS
12.5 WATTS



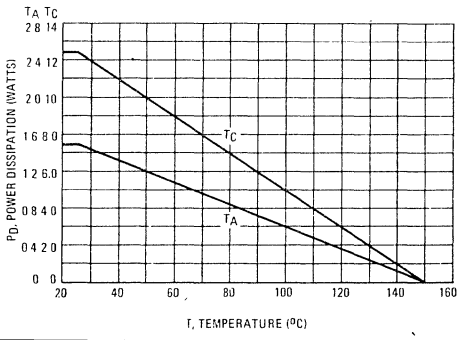
MAXIMUM RATINGS

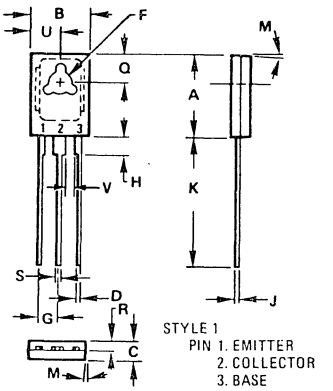
Rating	Symbol	MJE170 MJE180	MJE171 MJE181	MJE172 MJE182	Unit
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	7.0			Vdc
Collector Current Continuous	I_C	3.0			Adc
Peak		6.0			
Base Current	I_B	1.0			Adc
Total Power Dissipation @ T_A = 25°C	P_D	1.5			Watts
Derate above 25°C		0.012			W/°C
Total Power Dissipation @ T_C = 25°C	P_D	12.5			Watts
Derate above 25°C		0.1			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	°C/W

FIGURE 1 – POWER DERATING





STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	2.16	2.41	0.085	0.095
J	0.38	0.64	0.015	0.025
K	15.37	16.64	0.605	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-03
TO-126

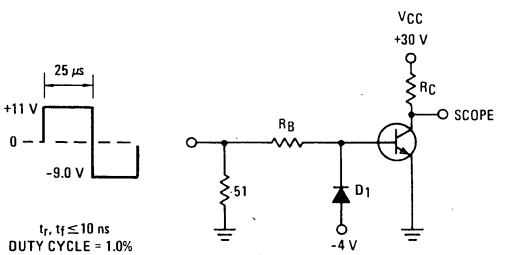
4

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0)	MJE170, MJE180	$V_{CEO(sus)}$	40	–	Vdc
	MJE171, MJE181		60	–	
	MJE172, MJE182		80	–	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 60 Vdc, I_E = 0)	MJE170, MJE180		–	0.1	
(V_{CB} = 80 Vdc, I_E = 0)	MJE171, MJE181		–	0.1	
(V_{CB} = 100 Vdc, I_E = 0)	MJE172, MJE182		–	0.1	
(V_{CB} = 60 Vdc, I_E = 0, T_C = 150°C)	MJE170, MJE180		–	0.1	mAdc
(V_{CB} = 80 Vdc, I_E = 0, T_C = 150°C)	MJE171, MJE181		–	0.1	
(V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)	MJE172, MJE182		–	0.1	
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)			50	250	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			30	–	
(I_C = 1.5 Adc, V_{CE} = 1.0 Vdc)			12	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			–	0.3	
(I_C = 1.5 Adc, I_B = 150 mAdc)			–	0.9	
(I_C = 3.0 Adc, I_B = 600 mAdc)			–	1.7	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 150 mAdc)			–	1.5	
(I_C = 3.0 Adc, I_B = 600 mAdc)			–	2.0	
Base-Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (1) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	50	–	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJE170/MJE172		–	50	
	MJE180/MJE182		–	30	

(1) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

For PNP test circuit, reverse all polarities.

FIGURE 3 – TURN-ON TIME

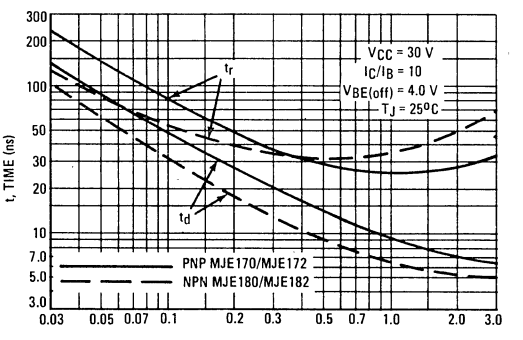
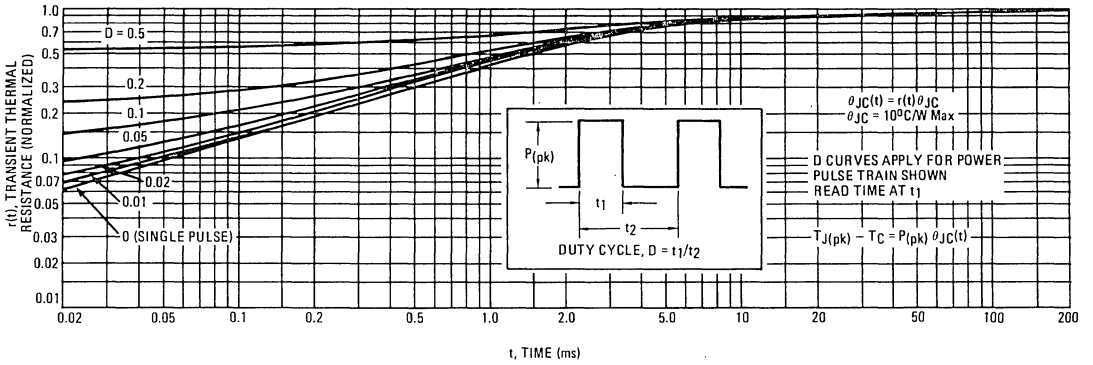


FIGURE 4 – THERMAL RESPONSE



4

ACTIVE-REGION SAFE OPERATING AREA

FIGURE 5 – MJE170, MJE171, MJE172

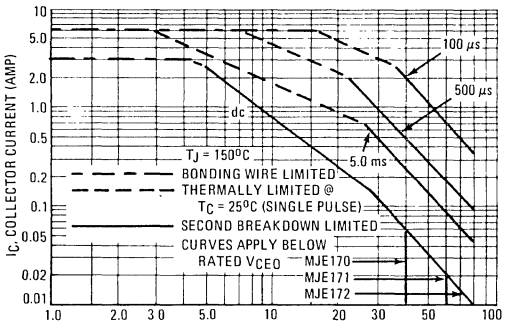
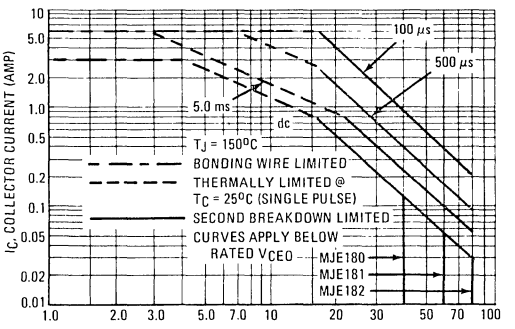


FIGURE 6 – MJE180, MJE181, MJE182



There are two limitations on the power handling ability of a transistor – average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperature, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 7 – TURN-OFF TIME

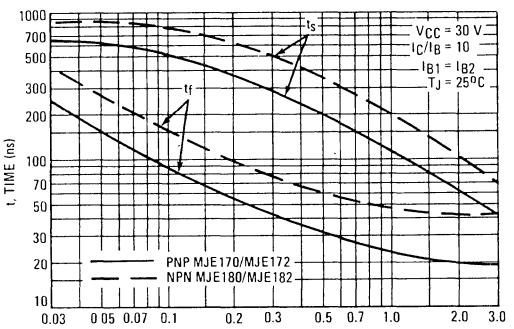
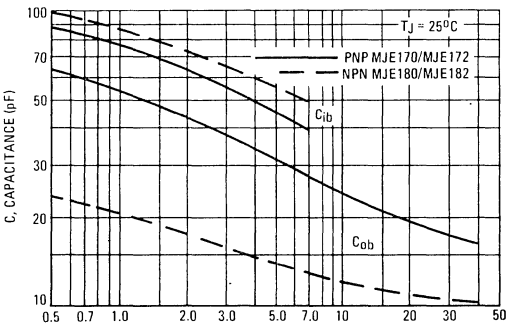


FIGURE 8 – CAPACITANCE

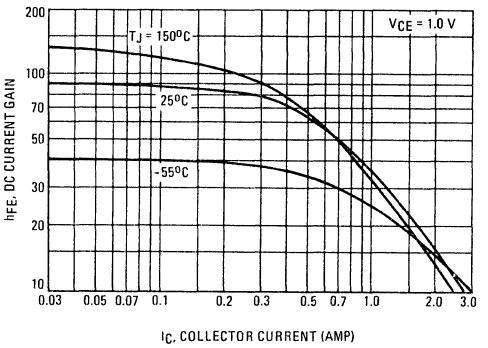


4

PNP
MJE170, MJE171, MJE172

NPN
MJE180, MJE181, MJE182

FIGURE 9 – DC CURRENT GAIN



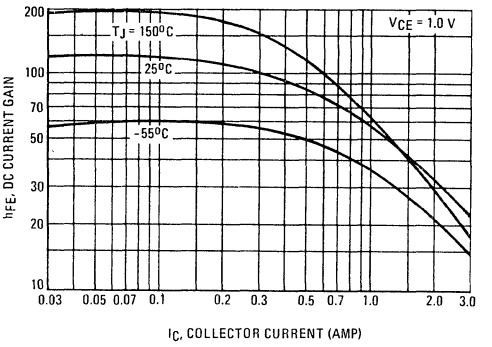
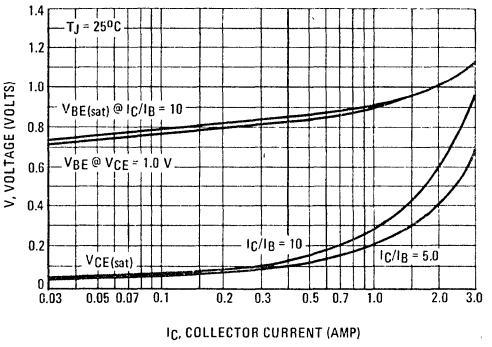


FIGURE 10 – "ON" VOLTAGES



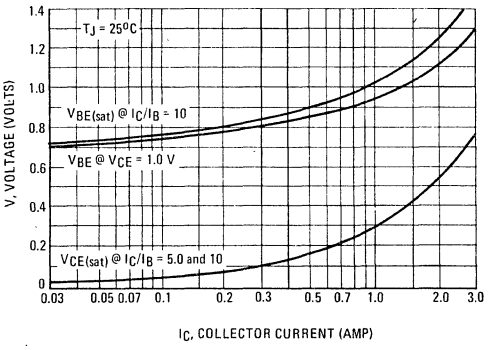
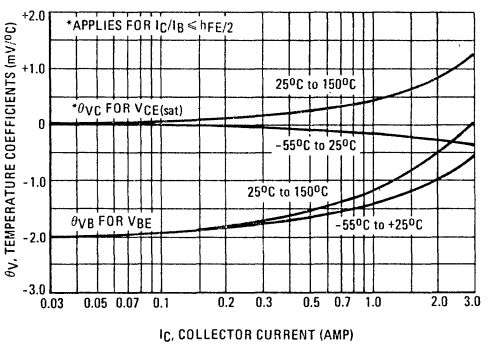
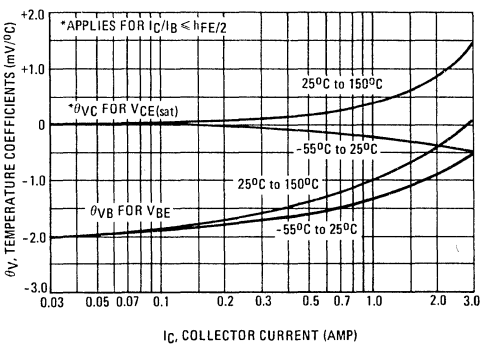


FIGURE 11 – TEMPERATURE COEFFICIENTS





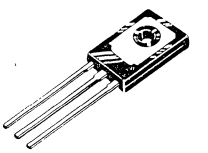
MJE200 NPN (SILICON)
MJE210 PNP

COMPLEMENTARY SILICON POWER PLASTIC TRANSISTORS

. . . designed for low voltage, low-power, high-gain audio amplifier applications.

- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 25 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain – h_{FE} = 70 (Min) @ I_C = 500 mAdc
  = 45 (Min) @ I_C = 2.0 Adc
  = 10 (Min) @ I_C = 5.0 Adc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
  = 0.75 Vdc (Max) @ I_C = 2.0 Adc
- High Current-Gain – Bandwidth Product –
  f_T = 65 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakage – I_{CBO} = 100 nAdc @ Rated V_{CB}

5 AMPERE
POWER TRANSISTORS COMPLEMENTARY SILICON
25 VOLTS
15 WATTS



4

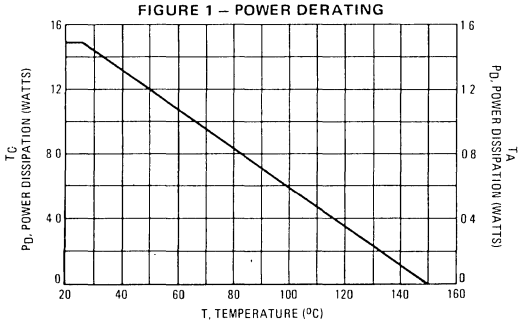
MAXIMUM RATINGS

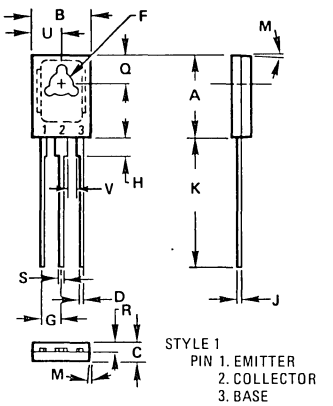
Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CB}	40	Vdc
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Emitter-Base Voltage	V_{EB}	8.0	Vdc
Collector Current – Continuous Peak	I_C	5.0 10	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.34	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	°C/W

FIGURE 1 – POWER DERATING





STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	2.16	2.41	0.085	0.095
J	0.38	0.64	0.015	0.025
K	15.37	16.64	0.605	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

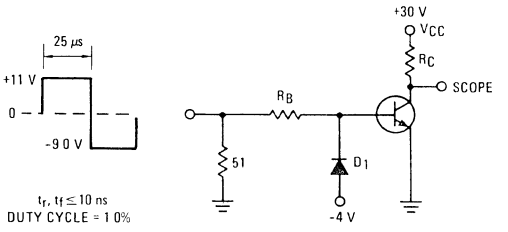
CASE 77-03
TO-126

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	25	–	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0, T_J = 125°C)	I_{CBO}	– –	100 100	nAdc μAdc
Emitter Cutoff Current (V_{BE} = 8.0 Vdc, I_C = 0)	I_{EBO}	–	100	nAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	 70 45 10	 – 180 –	–
Collector-Emitter Saturation Voltage (1) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 2.0 Adc, I_B = 200 mAdc) (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{CE(sat)}$	 – – –	 0.3 0.75 1.8	Vdc
Base-Emitter Saturation Voltage (1) (I_C = 5.0 Adc, I_B = 1.0 Adc)	$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (1) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc	$V_{BE(on)}$	–	1.6	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product (2) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	65	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJE200 MJE210	C_{ob}	 –	 80 120	pF

(1) Pulse test: Pulse Width = 300 μs, Duty Cycle ≈ 2.0%.
(2) $f_T = |h_{fe}| \cdot f_{test}$

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg
MBD5300 USED ABOVE IB ~100 mA
MSD6100 USED BELOW IB ~100 mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 – TURN-ON TIME

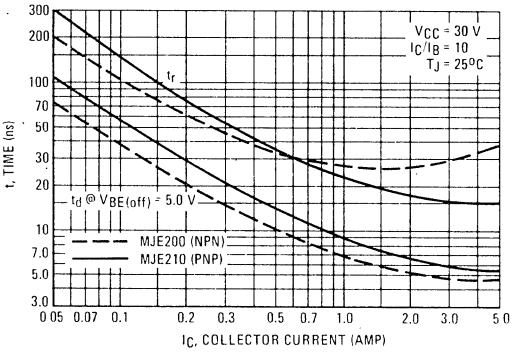
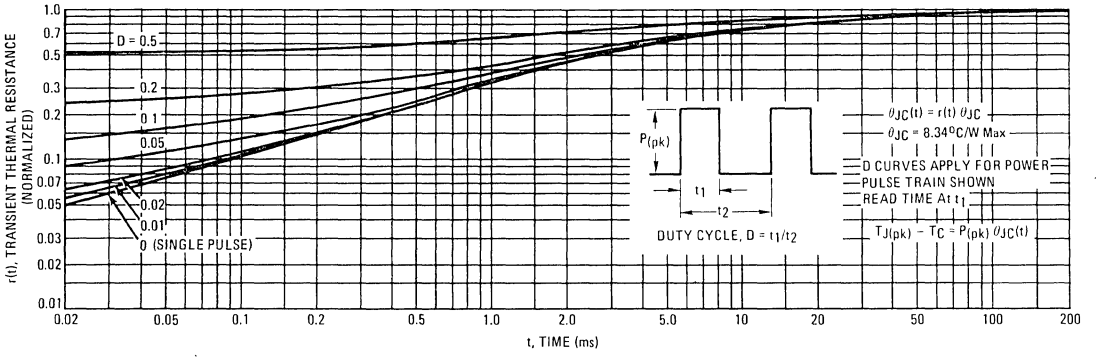
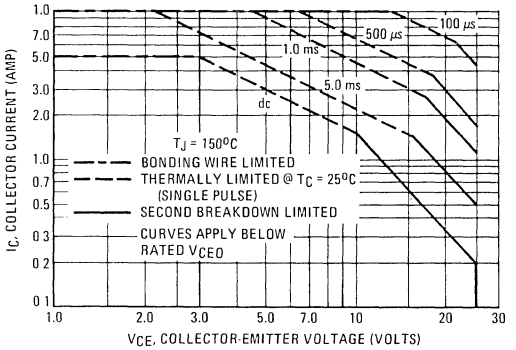


FIGURE 4 – THERMAL RESPONSE



4

FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

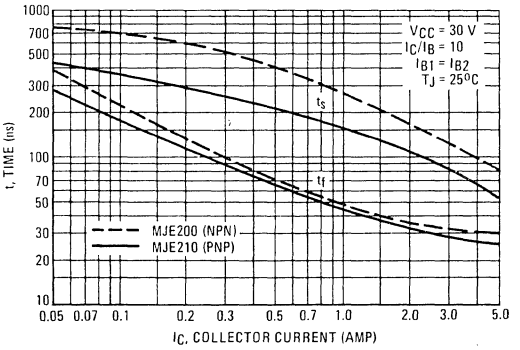
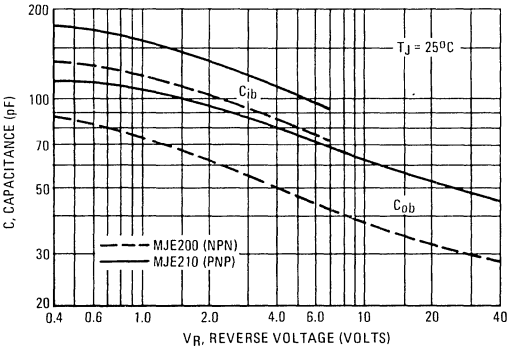


FIGURE 7 – CAPACITANCE

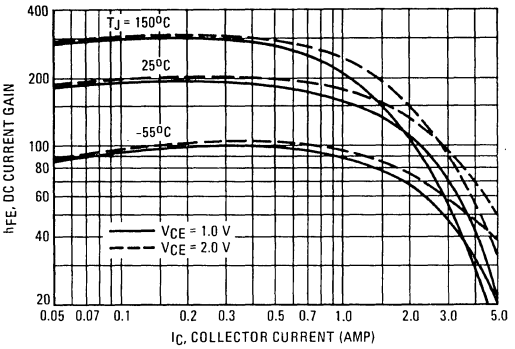


4

NPN
MJE200

PNP
MJE210

FIGURE 8 – DC CURRENT GAIN



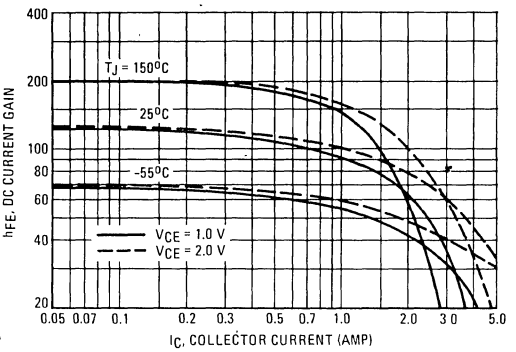
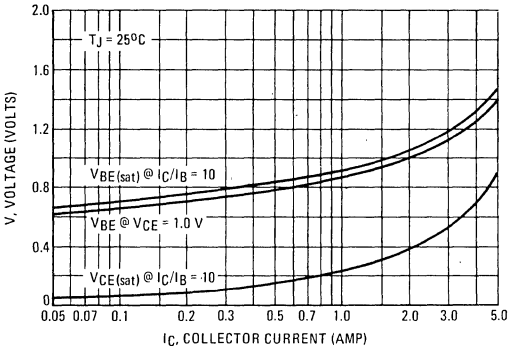


FIGURE 9 – "ON" VOLTAGE



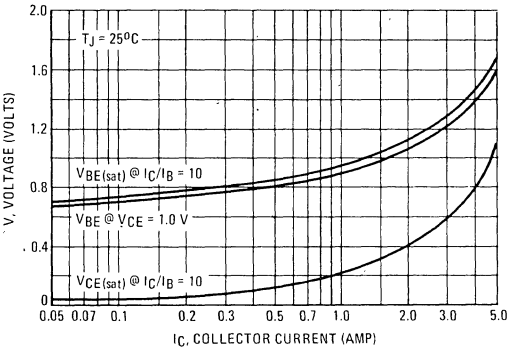
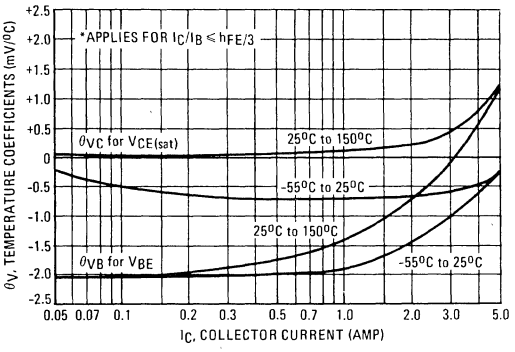
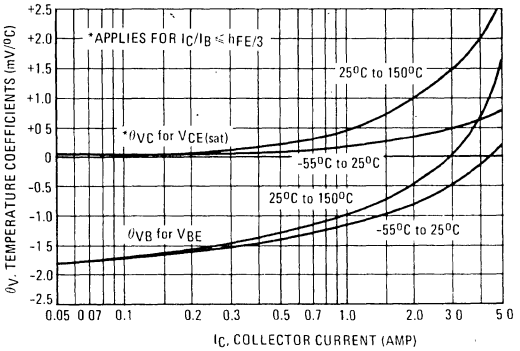


FIGURE 10 – TEMPERATURE COEFFICIENTS





MJE205 (SILICON)

MEDIUM-POWER NPN SILICON TRANSISTOR

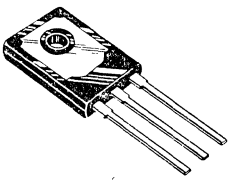
. . . for use as an output device in complementary audio amplifiers up to 20-Watts music power per channel.

- High DC Current Gain – h_{FE} = 25-100 @ I_C = 2.0 A
- Thermopad High-Efficiency Compact Package
- Complementary to PNP MJE 105

5 AMPERE POWER TRANSISTOR

NPN SILICON

50 VOLTS
65 WATTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	5.0	Adc
Base Current	I_B	2.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D†	65 0.522	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

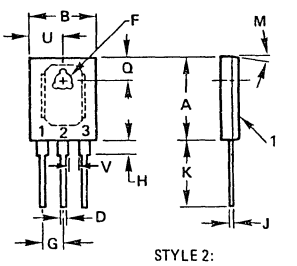
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.92	°C/W

†Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage‡ (I_C = 100 mAdc, I_B = 0)	BV_{CEO}‡	50	–	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0) (V_{CB} = 50 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	– –	0.1 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	–
Base-Emitter Voltage (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)	V_{BE}	–	1.2	Vdc

‡Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

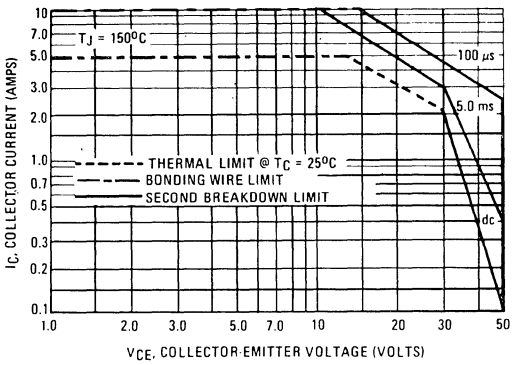


STYLE 2:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05
TO-127

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

4

FIGURE 2 – "ON" VOLTAGES

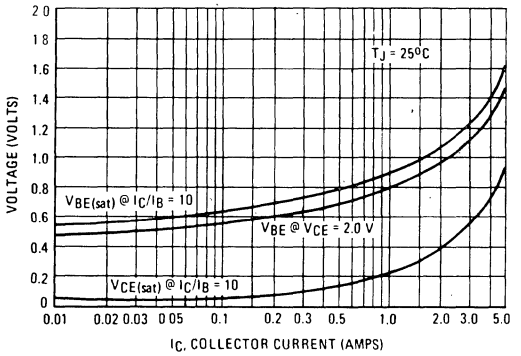


FIGURE 3 – DC CURRENT GAIN

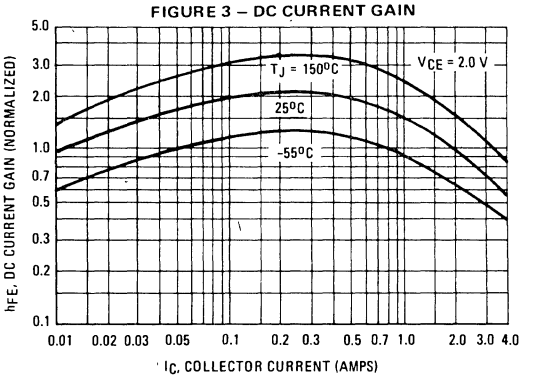
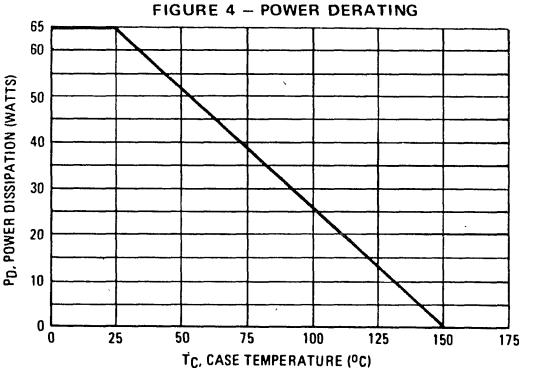


FIGURE 4 – POWER DERATING



NPN

MJE240 thru MJE244

PNP

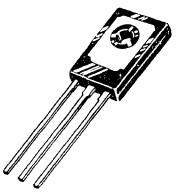
MJE250 thru MJE254

COMPLEMENTARY SILICON POWER PLASTIC TRANSISTORS

. . . designed for low power audio amplifier and low-current, high-speed switching applications.

- High Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 80 Vdc (Min) – MJE240/2, MJE250/2
  = 100 Vdc (Min) – MJE243/4, MJE253/4
- High DC Current Gain @ I_C = 200 mAdc
  h_{FE} = 40-200 – MJE240, MJE250
  = 40-120 – MJE241,243, MJE251,253
  = 25 (Min) – MJE242,44, MJE252,54
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
- High Current Gain Bandwidth Product –
  f_T = 40 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakages
  I_{CBO} = 100 nAdc (Max) @ Rated V_{CB}

4 AMPERE
POWER TRANSISTORS COMPLEMENTARY SILICON
80, 100 VOLTS
15 WATTS



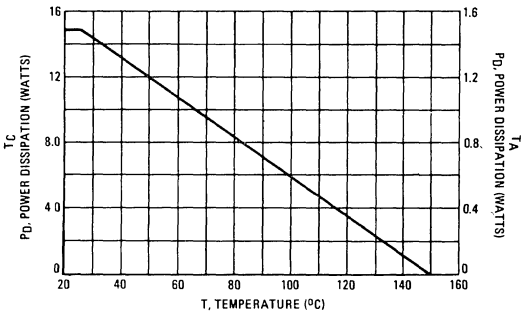
MAXIMUM RATINGS

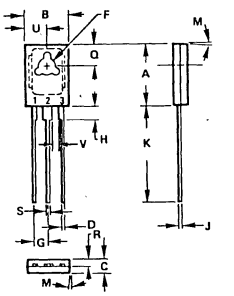
Rating	Symbol	MJE240 MJE241 MJE242 MJE250 MJE251 MJE252	MJE243 MJE244 MJE253 MJE254	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	Vdc
Collector-Base Voltage	V_{CB}	80	100	Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Collector Current – Continuous Peak	I_C	4.0 8.0		Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.34	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	°C/W

FIGURE 1 – POWER DERATING





STYLE 6
PIN 1 CATHODE
2. GATE
3. ANODE

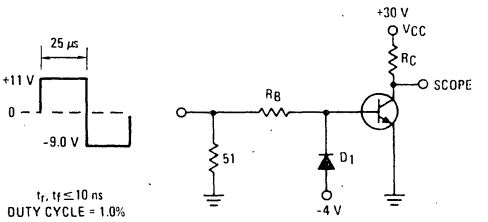
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0)	MJE240,MJE241,MJE242, MJE250,MJE251,MJE252	$V_{CEO(sus)}$	80	–	Vdc
	MJE243,MJE244 MJE253,MJE254		100	–	
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	MJE240,MJE241,MJE242, MJE250,MJE251,MJE252	I_{CBO}	–	0.1	μAdc
(V_{CB} = 100 Vdc, I_E = 0)	MJE243,MJE244, MJE253,MJE254		–	0.1	
(V_{CE} = 80 Vdc, I_E = 0, T_C = 125°C)	MJE240,MJE241,MJE242 MJE250,MJE251,MJE252,		–	0.1	mAdc
(V_{CE} = 100 Vdc, I_E = 0, T_C = 125°C)	MJE243,MJE244 MJE253,MJE254		–	0.1	
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 200 mAdc, V_{CE} = 1.0 Vdc)	MJE240,MJE250	h_{FE}	40	200	–
	MJE241,MJE251, MJE243,MJE253		40	120	
	MJE242,MJE252, MJE244,MJE254		25	–	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	MJE241,MJE251, MJE243,MJE253		20	–	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	MJE242,MJE252 MJE244,MJE254		10	–	
(I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)	MJE240,MJE250		15	–	
Collector-Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)	All Types	$V_{CE(sat)}$	–	0.3	Vdc
(I_C = 1.0 Adc, I_B = 100 mAdc)	MJE241,MJE251,		–	0.6	
(I_C = 2.0 Adc, I_B = 200 mAdc)	MJE243,MJE253 MJE240, MJE250		–	0.8	
Base-Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	–	1.8	Vdc
Base-Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	40	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJE240/MJE244	C_{ob}	–	50	pF
	MJE250/MJE254		–	70	

FIGURE 2 – SWITCHING TIME TEST CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg.
MBD5300 USED ABOVE I_B ≈100 mA
MSD6100 USED BELOW I_B ≈100 mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

FIGURE 3 – TURN-ON TIME

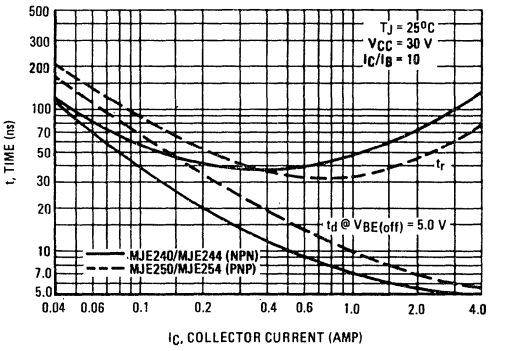


FIGURE 4 – THERMAL RESPONSE

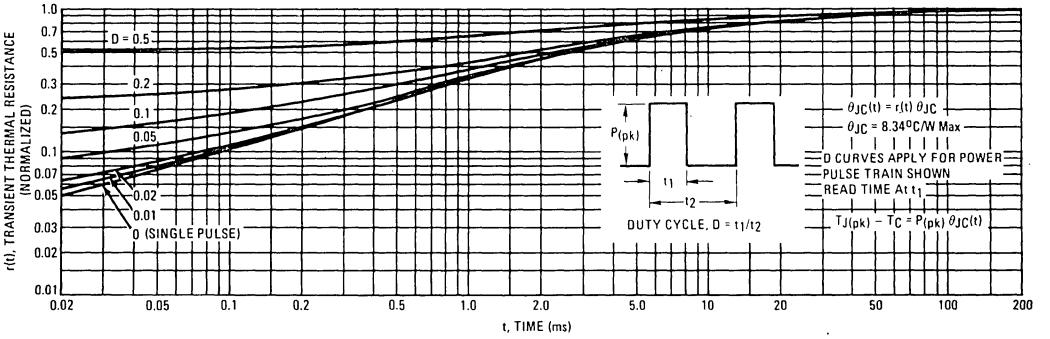
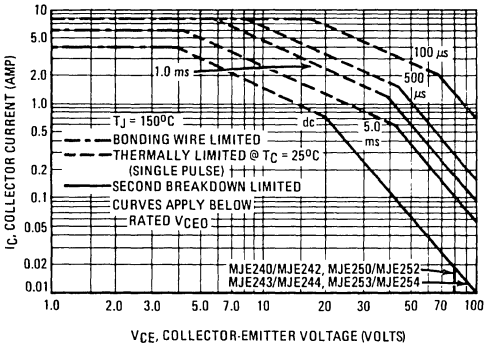


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

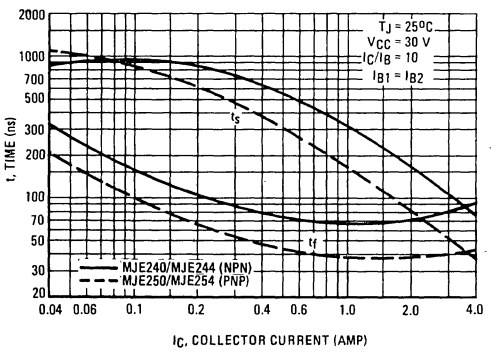
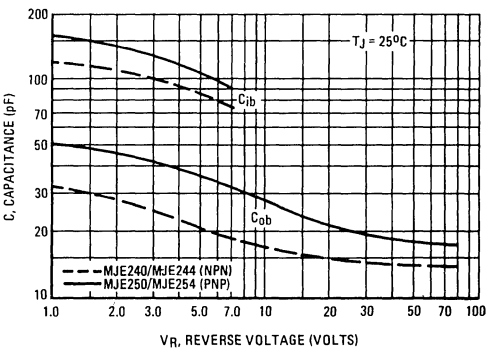


FIGURE 7 – CAPACITANCE

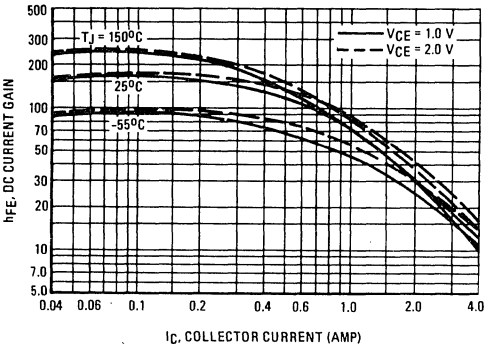


4

NPN
MJE240 thru MJE244

PNP
MJE250 thru MJE254

FIGURE 8 – DC CURRENT GAIN



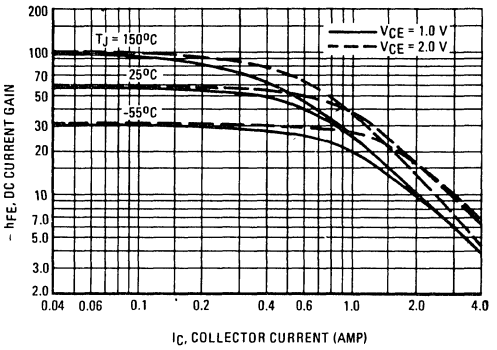
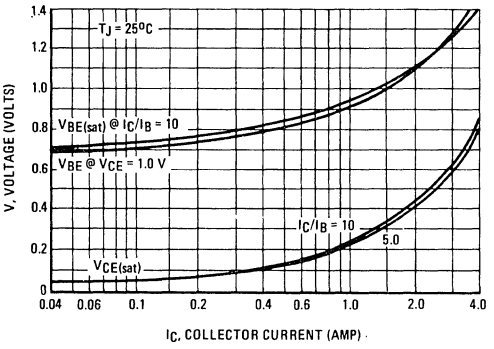


FIGURE 9 – "ON" VOLTAGES



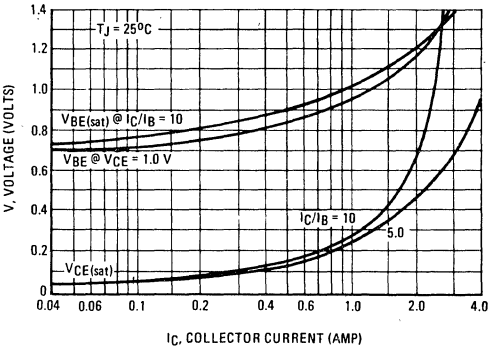
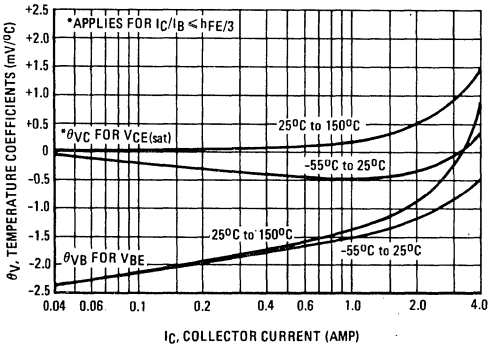
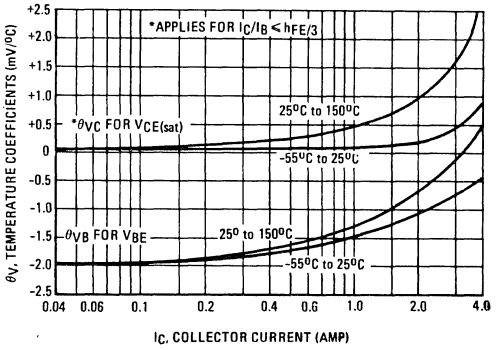


FIGURE 10 – TEMPERATURE COEFFICIENTS





MJE340 (SILICON)

PLASTIC MEDIUM POWER NPN
SILICON TRANSISTOR

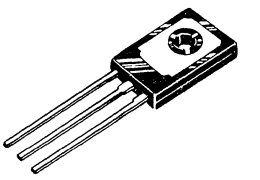
. . . useful for high-voltage general purpose applications.

- Suitable for Transformerless, Line-Operated Equipment
- Thermopad Construction Provides High Power Dissipation Rating for High Reliability

0.5 AMPERE
POWER TRANSISTOR

NPN SILICON

300 VOLTS
20 WATTS



4

MAXIMUM RATINGS

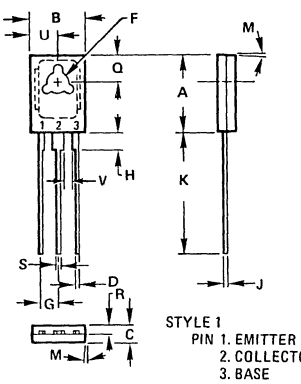
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current – Continuous	I_C	500	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	–	Vdc
Collector Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CBO}	–	100	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	–



STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

FIGURE 1 – POWER TEMPERATURE DERATING

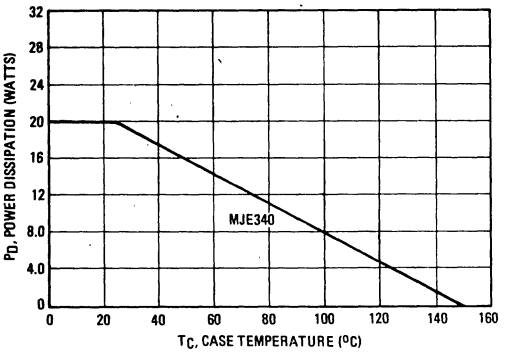
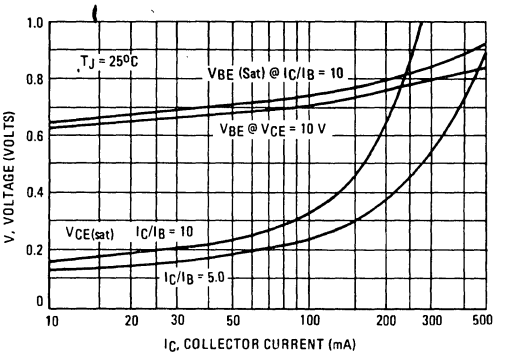
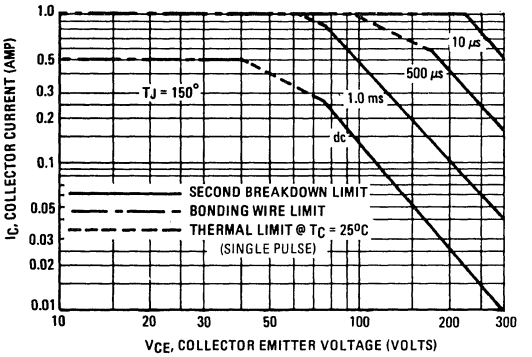


FIGURE 2 – "ON" VOLTAGES



ACTIVE-REGION SAFE OPERATING AREA

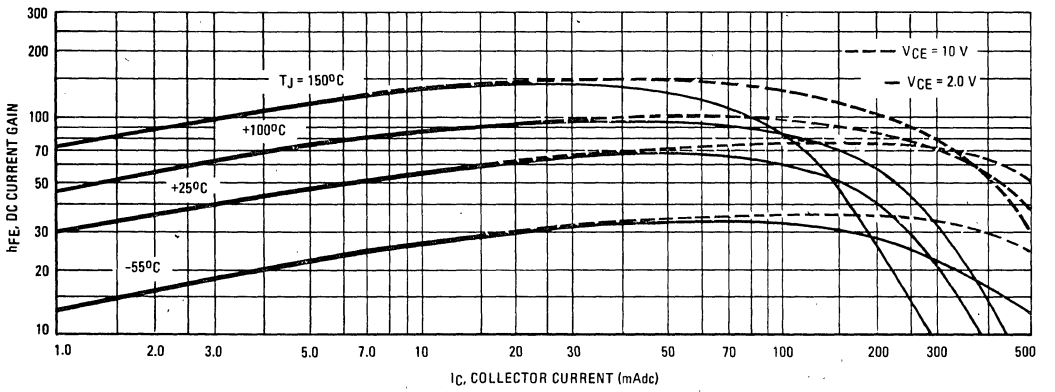
FIGURE 3 – MJE340



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 4 – DC CURRENT GAIN

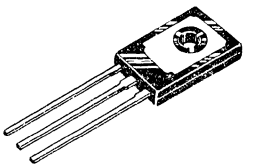


MJE341 (SILICON)
MJE344

PLASTIC NPN SILICON
MEDIUM-POWER TRANSISTORS

. . .useful for medium voltage applications requiring high f_T such as converters and extended range amplifiers.

0.5 AMPERE
POWER TRANSISTORS
NPN SILICON
150-200 VOLTS
20 WATTS



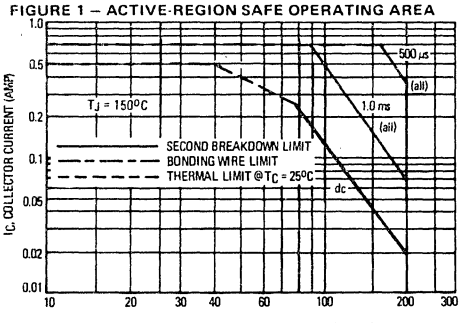
MAXIMUM RATINGS

Rating	Symbol	MJE341	MJE344	Unit
Collector-Emitter Voltage	V_{CEO}	150	200	Vdc
Collector-Base Voltage	V_{CB}	175	200	Vdc
Emitter-Base Voltage	V_{EB}	3.0	5.0	Vdc
Collector Current — Continuous	I_C	← 500 →		mAdc
Base Current	I_B	← 250 →		mAdc
Total Power Dissipation @ T_C=25°C Derate above 25°C	P_D	20 0.16		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	← −65 to +150 →		°C

THERMAL CHARACTERISTICS

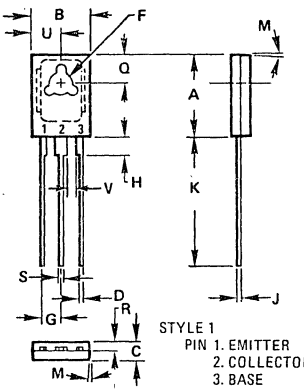
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

FIGURE 1 — ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	2.16	2.41	0.085	0.095
J	0.38	0.64	0.015	0.025
K	15.37	16.64	0.605	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-03
TO-126

4

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	MJE341 MJE344	$V_{CEO(sus)}$	 150 200	 – –	Vdc
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 150 Vdc, I_B = 0)	MJE341		–	1.0	
(V_{CE} = 200 Vdc, I_B = 0)	MJE344		–	1.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 175 Vdc, I_E = 0)	MJE341		–	0.3	
(V_{CB} = 200 Vdc, I_E = 0)	MJE344		–	0.1	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{EB} = 3.0 Vdc, I_C = 0)	MJE341		–	0.1	
(V_{EB} = 5.0 Vdc, I_C = 0)	MJE344		–	0.1	
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 10 mAdc, V_{CE} = 10 Vdc)	MJE341		20	–	
(I_C = 50 mAdc, V_{CE} = 10 Vdc)	MJE341		25	200	
	MJE344		30	300	
(I_C = 150 mAdc, V_{CE} = 10 Vdc)	MJE341		20	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 50 mAdc, I_B = 5.0 mAdc)	MJE344		–	1.0	
(I_C = 150 mAdc, I_B = 15 mAdc)	MJE341		–	2.3	
Base-Emitter On Voltage (I_C = 50 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 25 Vdc, f = 10 MHz)		f_T	15	–	MHz
Output Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	15	pF
Small-Signal Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–

FIGURE 2 – DC CURRENT GAIN

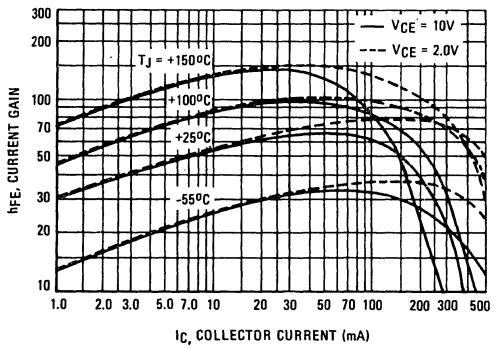
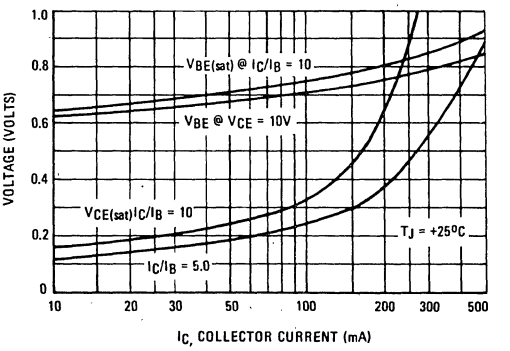


FIGURE 3 – "ON" VOLTAGES



MJE350 (SILICON)

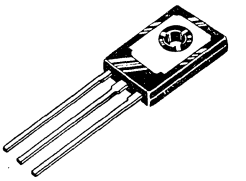
PLASTIC MEDIUM POWER PNP SILICON TRANSISTOR

. . . designed for use in line-operated applications such as low power, line-operated series pass and switching regulators requiring PNP capability.

- High Collector-Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 300 Vdc @ I_C = 1.0 mAdc
- Excellent DC Current Gain — h_{FE} = 30-240 @ I_C = 50 mAdc
- Plastic Thermopad Package

0.5 AMPERE POWER TRANSISTOR PNP SILICON

300 VOLTS
20 WATTS



MAXIMUM RATINGS

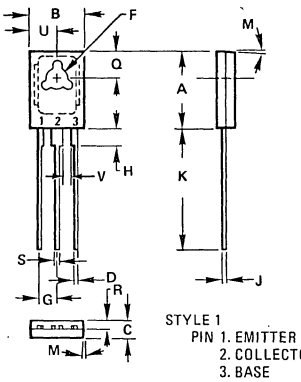
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	—	Vdc
Collector Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CBO}	—	100	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	—



STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	—	0.040	—

CASE 77-04
TO-126

FIGURE 1 – DC CURRENT GAIN

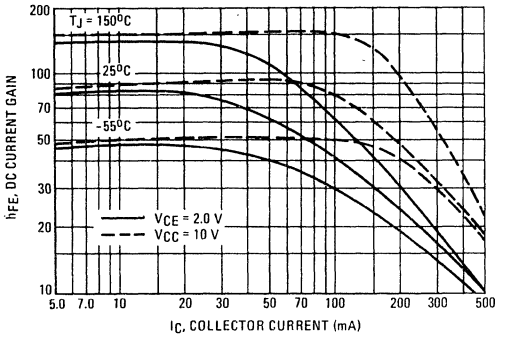


FIGURE 2 – "ON" VOLTAGES

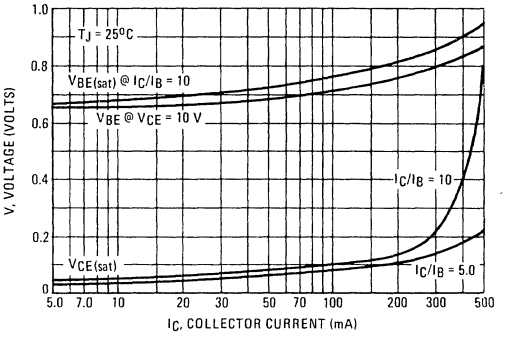


FIGURE 3 – ACTIVE-REGION SAFE OPERATING AREA

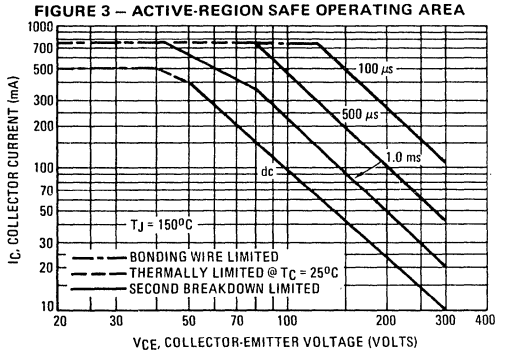
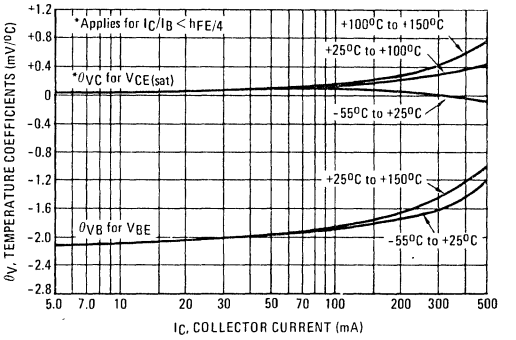


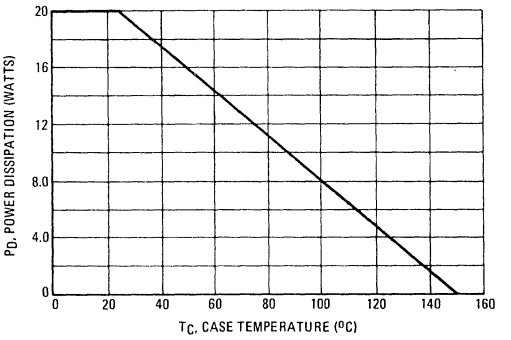
FIGURE 4 – TEMPERATURE COEFFICIENTS



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 5 – POWER DERATING



MJE370 (SILICON)

PLASTIC MEDIUM-POWER PNP
SILICON TRANSISTOR

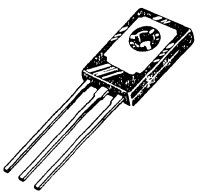
. . . designed for use in general-purpose amplifiers and switching circuits. Recommended for use in 5 to 10 Watt audio amplifiers utilizing complementary symmetry circuitry.

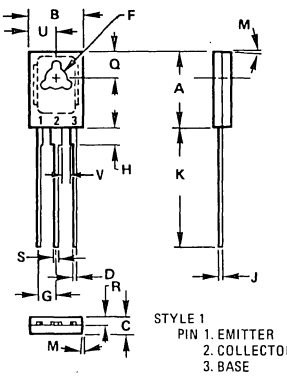
- DC Current Gain – h_{FE} = 25 (Min) @ I_C = 1.0 Adc
- Complementary to NPN MJE520

3 AMPERE
POWER TRANSISTOR

PNP SILICON

30 VOLTS
25 WATTS





STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous – Peak	I_C	3.0 7.0	Adc
Base Current – Continuous	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	25 0.2	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

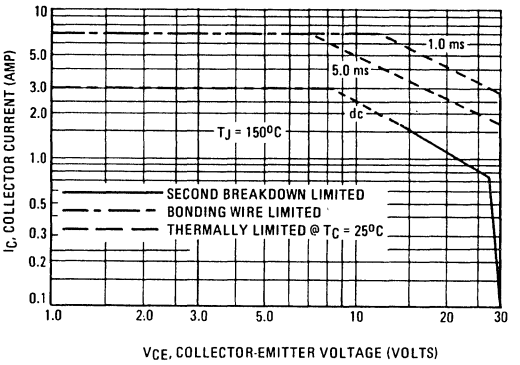
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	30	–	Vdc
Collector-Base Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	100	μAdc
Emitter-Base Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	25	–	–

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	2.16	2.41	0.085	0.095
J	0.38	0.64	0.015	0.025
K	15.37	16.64	0.605	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-03
TO-126

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J)pk)} \leqslant 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

4

FIGURE 2 – DC CURRENT GAIN

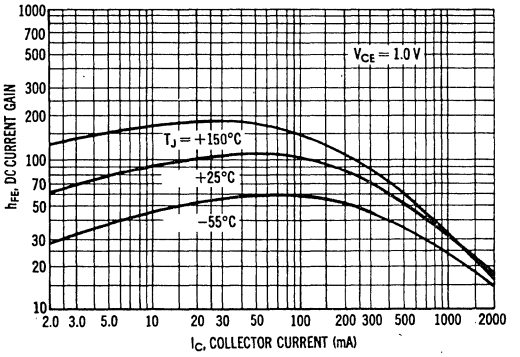


FIGURE 3 – "ON" VOLTAGE

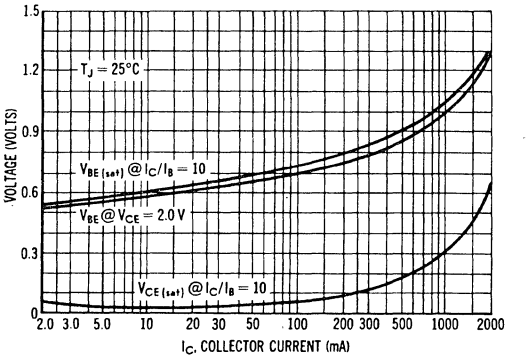
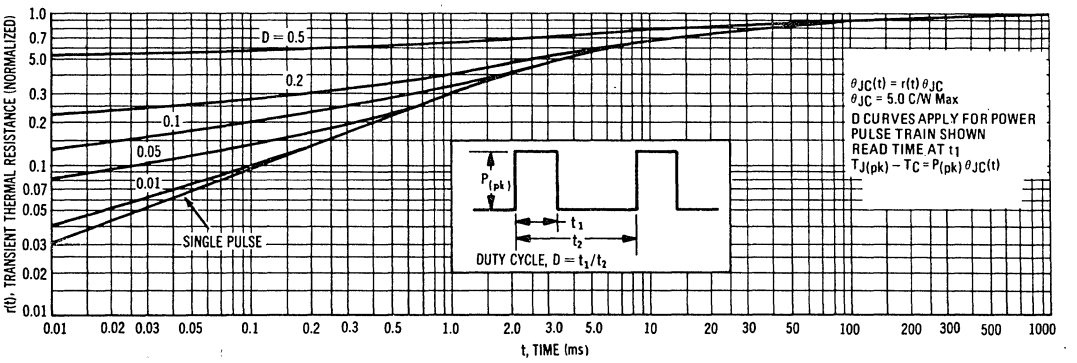


FIGURE 4 – THERMAL RESPONSE



MJE371

PLASTIC MEDIUM-POWER PNP SILICON TRANSISTORS

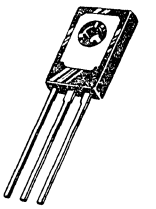
. . . designed for use in general-purpose amplifier and switching circuits. Recommended for use in 5 to 20 Watt audio amplifiers utilizing complementary symmetry circuitry.

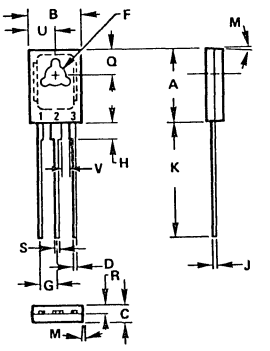
- DC Current Gain – h_{FE} = 40 (Min) @ I_C = 1.0 Adc
- MJE371 is Complementary to NPN MJE521

4 AMPERE

POWER TRANSISTORS PNP SILICON

40 VOLTS
40 WATTS





STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous – Peak	I_C	4.0 8.0	Adc
Base Current – Continuous	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 320	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

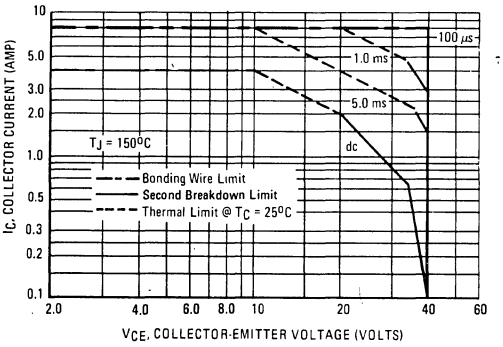
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	40	–	Vdc
Collector-Base Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	I_{CBO}	–	100	μAdc
Emitter-Base Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	40	–	–

(1) Pulse Test: Pulse Width ≤ 300 μs Duty Cycle ≤ 2.0%.

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 – DC CURRENT GAIN

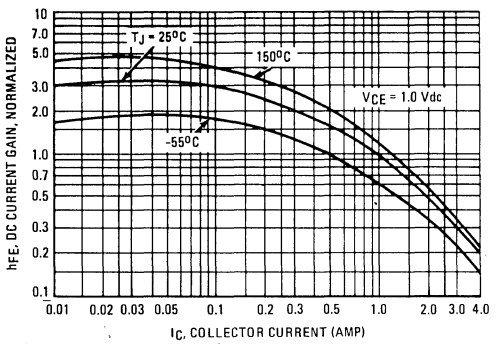


FIGURE 3 – "ON" VOLTAGE

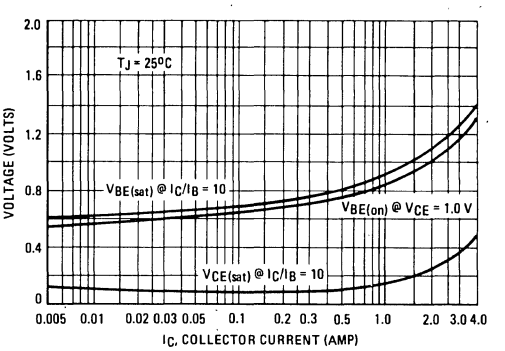
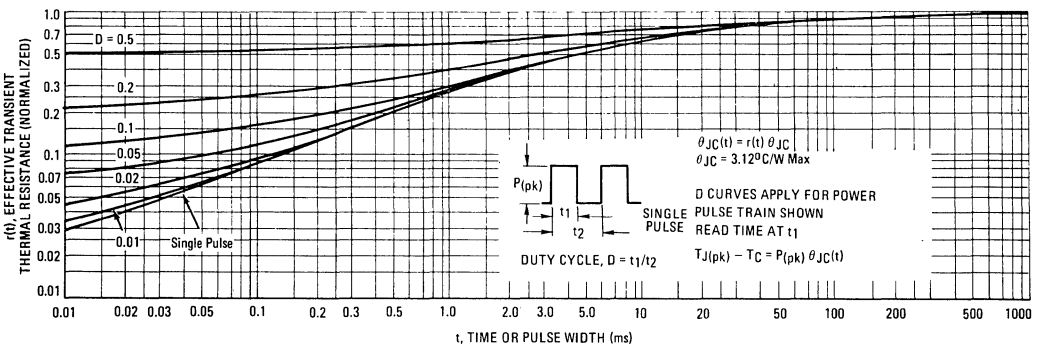


FIGURE 4 – THERMAL RESPONSE



MJE520 (SILICON)

PLASTIC MEDIUM-POWER NPN SILICON TRANSISTOR

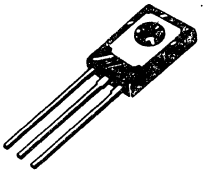
. . . designed for use in general-purpose amplifier and switching circuits. Recommended for use in 5 to 10 Watt audio amplifiers utilizing complementary symmetry circuitry.

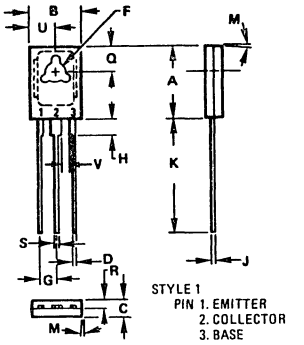
- DC Current Gain – h_{FE} = 25 (Min) @ I_C = 1.0 Adc
- Complementary to PNP MJE370

3 AMPERE POWER TRANSISTOR

NPN SILICON

30 VOLTS
25 WATTS





STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CB}	30	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current – Continuous – Peak	I_C	3.0 7.0	Adc
Base Current – Continuous	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	25 0.2	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

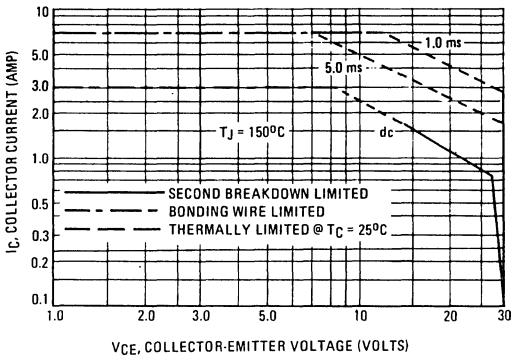
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	30	–	Vdc
Collector-Base Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	100	μAdc
Emitter-Base Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	25	–	–

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	2.16	2.41	0.085	0.095
J	0.38	0.64	0.015	0.025
K	15.37	16.64	0.605	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-03
TO-126

FIGURE 1 ACTIVE-REGION SAFE OPERATING AREA



The data of Figure 1 based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided (T_{Jpk}) ≤ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

FIGURE 2 – DC CURRENT GAIN

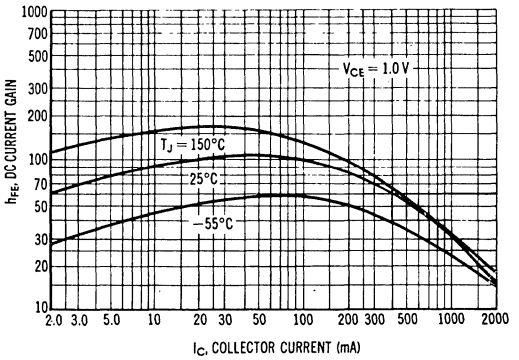


FIGURE 3 – "ON" VOLTAGE

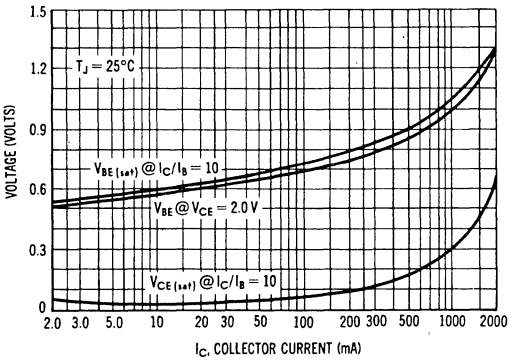
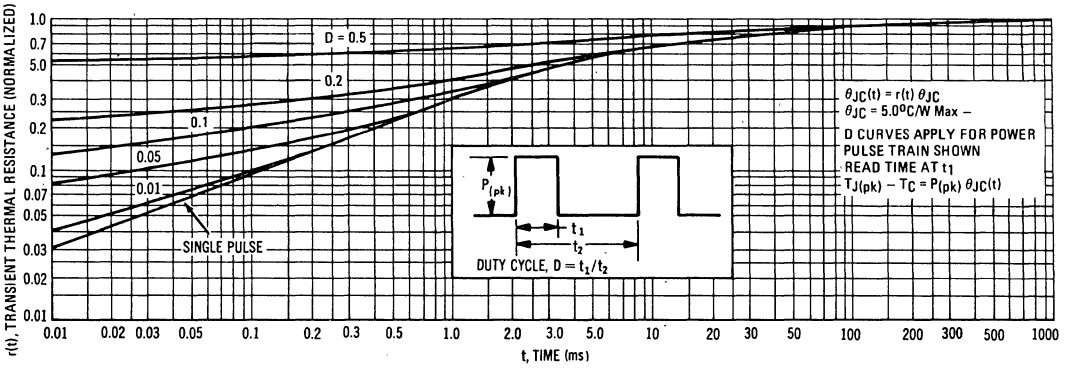


FIGURE 4 – THERMAL RESPONSE



PNP

MJE700 thru MJE703

NPN

MJE800 thru MJE803

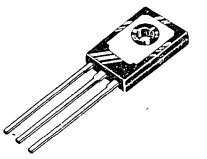
PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . designed to replace discrete driver and output stages in complementary audio amplifier applications.

- High DC Current Gain – h_{FE} = 750 (Min) @ I_C = 1.5 and 2.0 Adc
- Monolithic Construction
- Three Lead Design – Emitter-Base Resistors to Limit Leakage Multiplication are Built in.

4.0 AMPERE DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON

60-80 VOLTS
40 WATTS

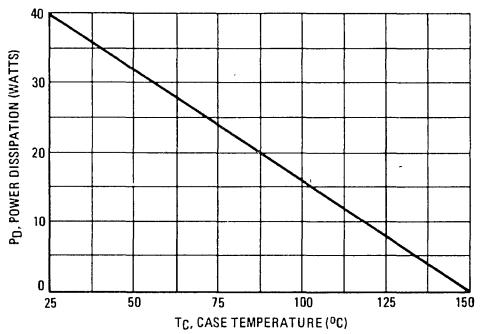


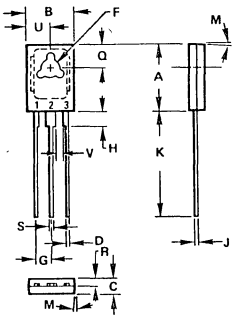
4

MAXIMUM RATINGS

Rating	Symbol	MJE700 MJE701 MJE800 MJE801	MJE702 MJE703 MJE802 MJE803	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	4.0		Adc
Base Current	I_B	0.1		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32		Watts W/°C
Operating and Storage Junction Temperating Range	T_J, T_{stg}	-55 to +150		°C
THERMAL CHARACTERISTICS				
Characteristic	**Symbol**	**Max**		**Unit**
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.13		°C/W

FIGURE 1 – POWER DERATING





STYLE 6
PIN 1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04

When mounting the device, torque not to exceed 6.0 in.-lb.

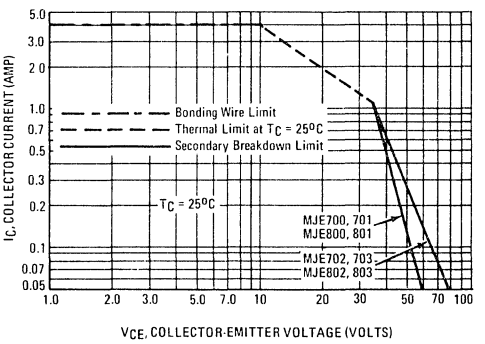
If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1)		BV_{CEO}			Vdc
(I_C = 50 mAdc, I_B = 0)	MJE700, MJE701, MJE800, MJE801		60	–	
	MJE702, MJE703, MJE802, MJE803		80	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 60 Vdc, I_B = 0)	MJE700, MJE701, MJE800, MJE801		–	100	
(V_{CE} = 80 Vdc, I_B = 0)	MJE702, MJE703, MJE802, MJE803		–	100	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = Rated BV_{CEO}, I_E = 0)			–	100	
(V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100°C)			–	500	
Emitter Cutoff Current		I_{EBO}	–	2.0	μA
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 1.5 Adc, V_{CE} = 3.0 Vdc)	MJE700, MJE702, MJE800, MJE802		750	–	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	MJE701, MJE703, MJE801, MJE803		750	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 30 mAdc)	MJE700, MJE702, MJE800, MJE802		–	2.5	
(I_C = 2.0 Adc, I_B = 40 mAdc)	MJE701, MJE703, MJE801, MJE803		–	2.8	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 1.5 Adc, V_{CE} = 3.0 Vdc)	MJE700, MJE702, MJE800, MJE802		–	2.5	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	MJE701, MJE703, MJE801, MJE803		–	2.5	
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain		$\lvert h_{fe} \rvert$	1.0	–	–
(I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)					

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

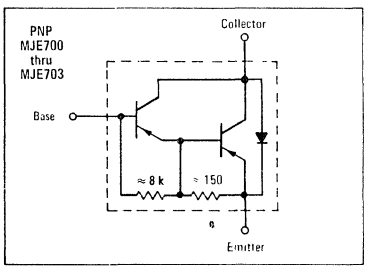
FIGURE 2 – DC SAFE OPERATING AREA

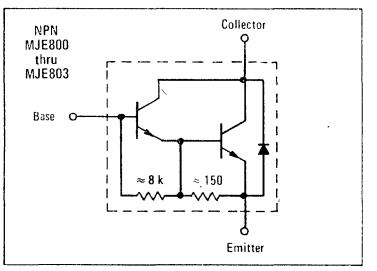


There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

FIGURE 3 – DARLINGTON CIRCUIT SCHEMATIC





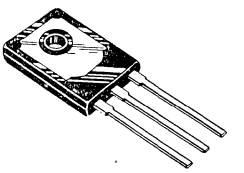
MJE1290 MJE1291 PNP (SILICON)
MJE1660 MJE1661 NPN

COMPLEMENTARY SILICON
MEDIUM-POWER TRANSISTORS

. . . designed for use in power amplifier and switching applications.

- High Collector Current – I_C = 15 Adc
- High DC Current Gain – h_{FE} = 10 (Min) @ I_C = 15 Adc

15 AMPERE
POWER TRANSISTORS
COMPLEMENTARY SILICON
40-60 VOLTS
90 WATTS



4

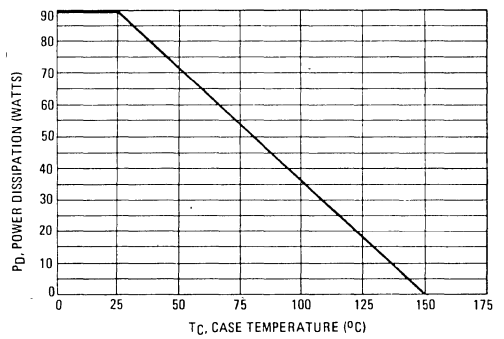
MAXIMUM RATINGS

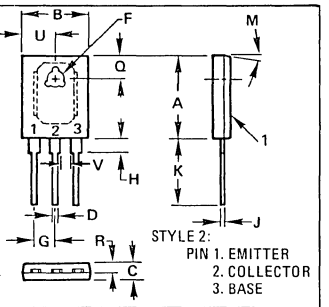
Rating	Symbol	MJE1290 MJE1660	MJE1291 MJE1661	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	Vdc
Collector-Base Voltage	V_{CB}	40	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current-Continuous	I_C	15		Adc
Base Current	I_B	5.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	90 0.72		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.39	°C/W

FIGURE 1 – POWER TEMPERATURE DERATING CURVE





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05
TO-127

When mounting the device, torque not to exceed 8.0 in.-lb.

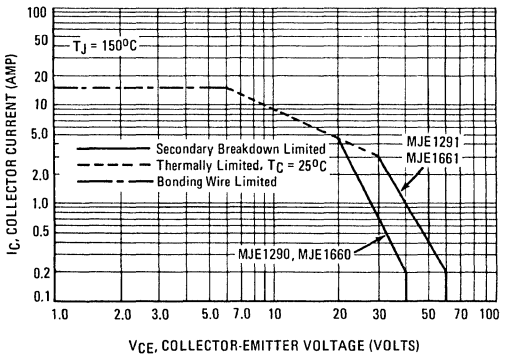
If lead bending is required, use suitable clamps or other supports between transistor case and point of bend.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	MJE1290, MJE1660		40	–	
	MJE1291, MJE1661		60	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)			–	1.0	
Collector Cutoff Current		I_{CES}			mAdc
(V_{CE} = 40 Vdc, V_{BE} = 0)	MJE1290, MJE1660		–	0.7	
(V_{CE} = 60 Vdc, V_{BE} = 0)	MJE1291, MJE1661		–	0.7	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	MJE1290, MJE1660		–	0.7	
(V_{CB} = 60 Vdc, I_E = 0)	MJE1291, MJE1661		–	0.7	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{BE} = 5.0 Vdc, I_E = 0)			–	1.0	
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			–
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)			20	100	
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)			10	–	
Collector-Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 15 Adc, I_B = 1.5 Adc)			–	1.8	
Base-Emitter on Voltage (1)		$V_{BE(on)}$			Vdc
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)			–	2.5	
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product		f_T			MHz
(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)			3.0	–	
Small-Signal Current Gain		h_{fe}			–
(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)			25	–	

(1) Pulse Test: Pulse Width ≤ 300 μs. Duty Cycle ≤ 2.0%.

FIGURE 2 – DC SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

MJE1909

NPN SILICON RF POWER TRANSISTOR

. . . this device is designed for use in large signal R.F. output amplifier stages in communications equipment operating to 50 MHz. This device is specifically tested for use at 27 MHz in Citizen Band equipment.

- Withstands Open and Short Circuit Load in AM Operation
- Specified 12 V, 27 MHz Characteristics
  Output Power = 4 W (CW)
  Minimum Efficiency = 60% (CW)

4 W (CW) –27 MHz

RF POWER TRANSISTOR

NPN SILICON

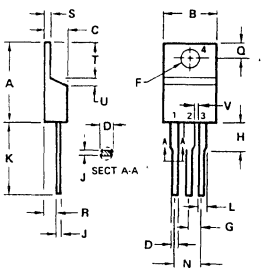
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage (R_{BE} = 150 Ω)	V_{CER}	75	Vdc
Collector-Base Voltage	V_{CBO}	75	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current – Peak (1)	I_C	3.0	Adc
Total Power Dissipation @ T_C = 50°C Derate Above 50°C	P_D	10 100	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W

(1) Pulse Width ≤ 20 ms, Duty Cycle ≤ 50%



STYLE 1.
PIN 1 BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.38	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	·	0.045	·

CASE 221A-02
TO-220 AB

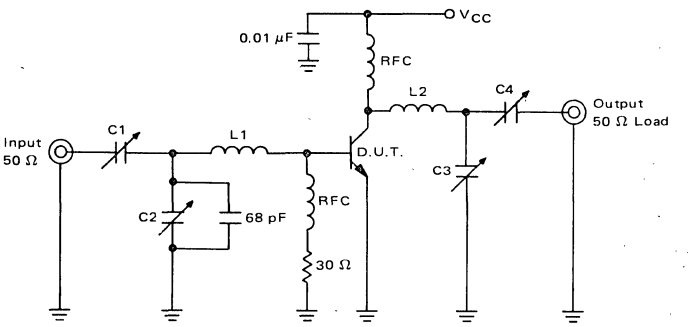
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	I_{CBO}	–	10	μA
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 0.5 Adc, V_{CE} = 10 V)	h_{FE}	20	150	–
Collector-Emitter Saturation Voltage (1) (I_C = 1 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	–	0.6	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 150 mA, V_{CE} = 10 V, f = 100 MHz)	f_T	100	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	70	pF
FUNCTIONAL TESTS (Figure 1)				
Output Power (V_{CC} = 12 V, f = 27 MHz, P_{in} = 0.2 W)	P_o	4.0	–	Watts
Collector Efficiency (V_{CC} = 12 V, f = 27 MHz, P_{in} = 0.2 W)	η	60	–	%

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%

4

FIGURE 1 – TEST CIRCUIT SCHEMATIC



C2, C3: ~ 110 pF Variable Capacitor
C1, C4: ~ 75 pF Variable Capacitor
L1: 0.15 to 0.22 μH, Q ≈ 5
L2: 0.46 μH, Q ≈ 5

MJE2360T
MJE2361T

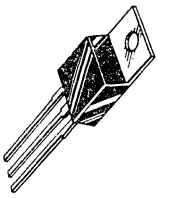
NPN SILICON HIGH-VOLTAGE TRANSISTOR

. . . useful for general-purpose, high voltage applications requiring high f_T.

- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 350 Vdc (Min) @ I_C = 2.5 mAdc
- DC Current Gain –
  h_{FE} = 40 (Min) @ I_C = 100 mAdc – MJE2361T
- Current-Gain–Bandwidth Product –
  f_T = 10 MHz (Typ) @ I_C = 50 mAdc

0.5 AMPERE POWER TRANSISTORS NPN SILICON

350 VOLTS
30 WATTS



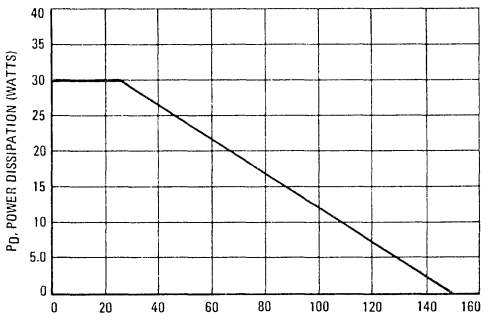
MAXIMUM RATINGS

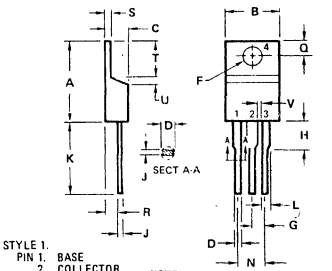
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	350	Vdc
Collector-Base Voltage	V_{CB}	375	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current – Continuous	I_C	0.5	Adc
Base Current	I_B	0.25	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 0.24	Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.167	°C/W

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE





STYLE 1.
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE.
1. DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

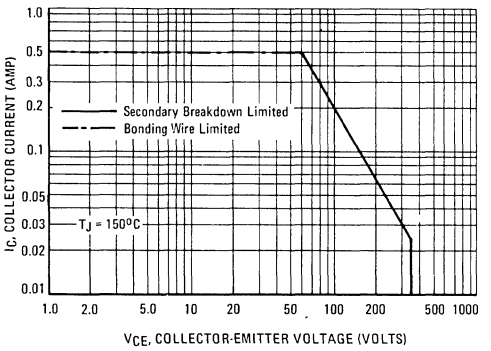
CASE 221A-02
(TO-220 AB)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage(1) (I_C = 2.5 mAdc, I_B = 0)		$V_{CEO(sus)}$	350	–	–	Vdc
Collector Cutoff Current (V_{CE} = 250 Vdc, I_B = 0)		I_{CEO}	–	–	0.25	mAdc
Collector Cutoff Current (V_{CE} = 375 Vdc, $V_{EB(off)}$ = 1.5 Vdc)		I_{CEX}	–	–	0.5	mAdc
Collector Cutoff Current (V_{CB} = 375 Vdc, I_E = 0)		I_{CBO}	–	–	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	–	0.1	mAdc
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}				–
(I_C = 50 mAdc, V_{CE} = 10 Vdc)	MJE2360T		25	–	200	
	MJE2361T		50	–	250	
(I_C = 100 mAdc, V_{CE} = 10 Vdc)	MJE2360T		15	–	–	
	MJE2361T		40	–	–	
Collector-Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)		$V_{CE(sat)}$		–	1.5	Vdc
Base-Emitter On Voltage (I_C = 100 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	–	1.0	Vdc
DYNAMIC CHARACTERISTICS						
Current-Gain - Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	–	10	–	MHz
Output Capacitance (V_{CB} = 100 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	20	–	pF

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

NPN

MJE2801, MJE2801T

PNP

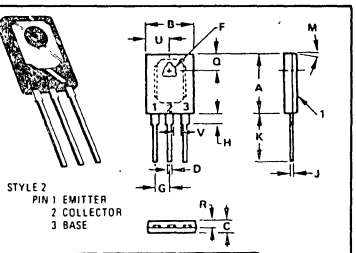
MJE2901, MJE2901T

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . for use as an output device in complementary audio amplifiers up to 35-Watts music power per channel.

- High DC Current Gain – h_{FE} = 25-100 @ I_C = 3.0 A
- Choice of Packages – MJE2801, 2901 – TO-225AB (TO-127)
  MJE2801T, 2901T – TO-220AB

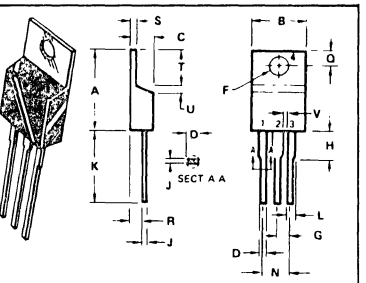
10 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60 VOLTS
75, 90 WATTS



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	5° TYP		5° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

MJE2801
MJE2901

CASE 90-05
TO-225AB
(TO-127)



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–

STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

NOTE
1 DIM. L & H APPLIES TO ALL LEADS

MJE2801T
MJE2901T

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	5.0	Adc
Total Power Dissipation @ T_C = 25°C MJE2801, 2901 MJE2801T, 2901T Derate above 25°C MJE2801, 2901 MJE2801T, 2901T	P_D†	 90 75 0.72 0.6	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case MJE2801, 2901 MJE2801T, 2901T	θ_{JC}	 1.39 1.67	°C/W

†Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

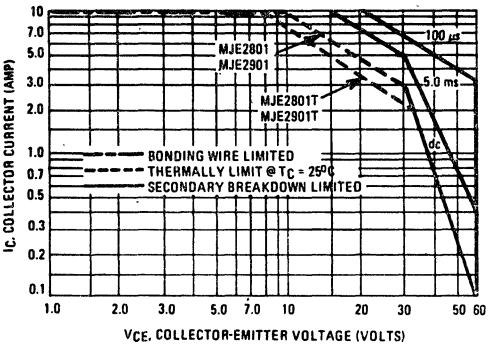
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 200 mAdc, I_B = 0)	BV_{CEO}	 60	 –	Vdc
Collector-Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	 – –	 0.1 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	–
Base-Emitter Voltage (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)	V_{BE}	–	1.4	Vdc

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

ΔTrademark of Motorola Inc.

FIGURE 1 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 2 – DC CURRENT GAIN

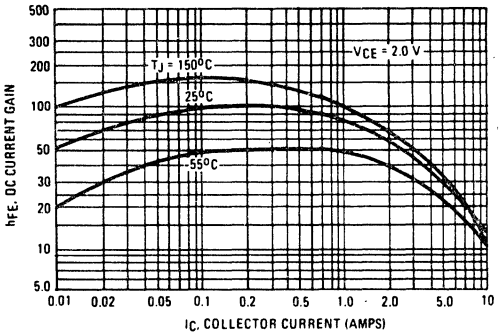


FIGURE 3 – POWER DERATING

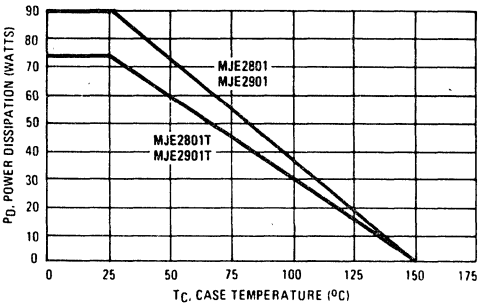
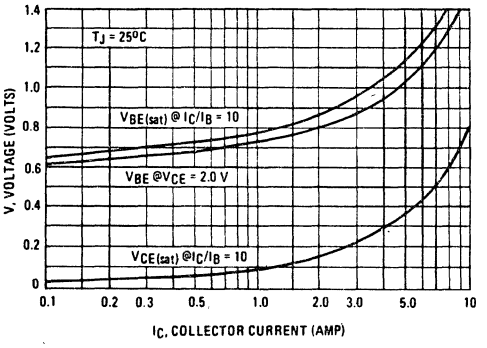
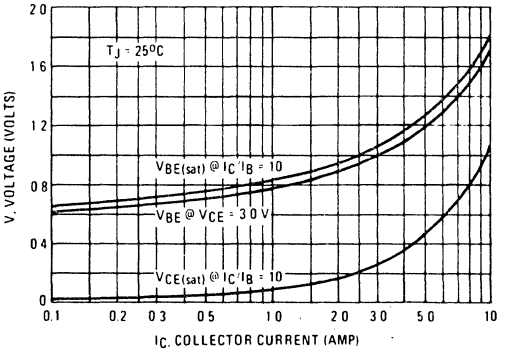


FIGURE 4 – "ON" VOLTAGES

MJE2801/MJE2801T



MJE2901/MJE2901T



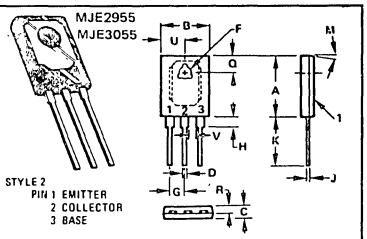
MJE2955, MJE2955T PNP (SILICON)
MJE3055, MJE3055T NPN

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general-purpose amplifier and switching applications.

- DC Current Gain Specified to 10 Amperes
- High Current Gain — Bandwidth Product — f_T = 2.0 MHz (Min) @ I_C = 500 mAdc
- Choice of Packages — MJE3055, MJE2955 — TO-225AB (TO-127)
  MJE3055T, MJE2955T — TO-220AB

10 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60 VOLTS
75, 90 WATTS



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
R	5° TYP		5° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05
TO-225AB
(TO-127)

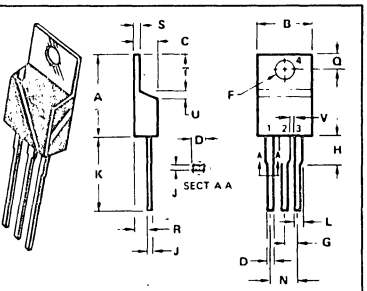
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CB}	70	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	6.0	Adc
Total Power Dissipation @ T_C = 25°C MJE3055, MJE2955 MJE3055T, MJE2955T Derate above 25°C MJE3055, MJE2955 MJE3055T, MJE2955T	P_D†	 90 75 0.72 0.6	Watts W/°C W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case MJE3055, MJE2955 MJE3055T, MJE2955T	θ_{JC}	 1.39 1.67	°C/W

†Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
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L	1.14	1.27	0.045	0.050
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Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–

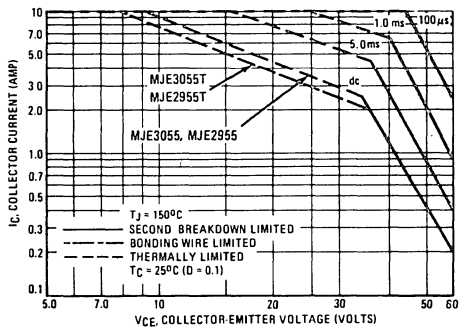
STYLE 1
PIN 1 BASE
2 COLLECTOR
3 EMITTER
4 COLLECTOR

NOTE
1 DIM L & H APPLIES TO ALL LEADS

MJE2955T
MJE3055T

CASE 221A-02
TO-220AB

FIGURE 1 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN 415A)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	700	μAdc
Collector Cutoff Current (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	1.0 5.0	mAdc
Collector Cutoff Current (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	– –	1.0 10	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 5.0	100 –	–
Collector-Emitter Saturation Voltage (1) (I_C = 4.0 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	– –	1.1 8.0	Vdc
Base-Emitter On Voltage (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 500 kHz)	f_T	2.0	–	MHz

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – DC CURRENT GAIN

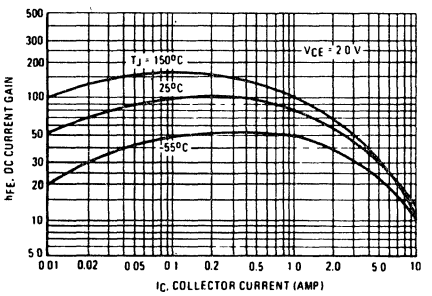


FIGURE 3 – POWER DERATING

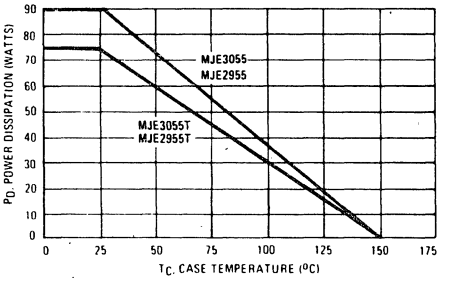
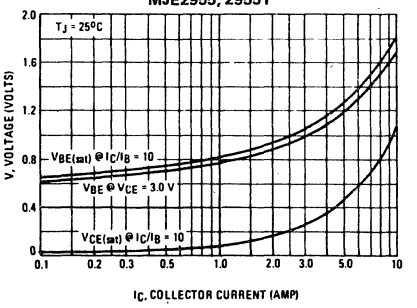
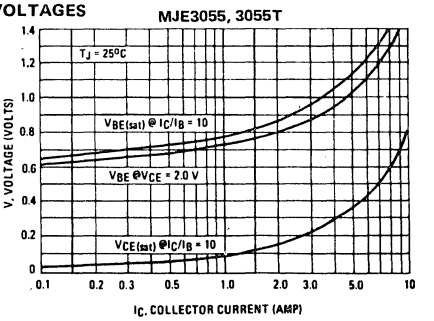


FIGURE 4 – "ON" VOLTAGES

MJE2955, 2955T



MJE3055, 3055T



MJE3300 MJE3301 MJE3302 NPN
MJE3310 MJE3311 MJE3312 PNP

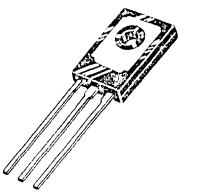
PLASTIC DARLINGTON COMPLEMENTARY SILICON ANNULAR POWER TRANSISTORS

. . . designed for general-purpose amplifier and high-speed switching applications.

- High DC Current Gain –
  h_{FE} = 2000 (Typ) @ I_C = 1.0 Adc
- Collector-Emitter Sustaining Voltage – @ 10 mAdc
  $V_{CEO(sus)}$ = 40 Vdc (Min) – MJE3310/MJE3300
  = 60 Vdc (Min) – MJE3311/MJE3301
  = 80 Vdc (Min) – MJE3312/MJE3302
- Reverse Voltage Protection Diode
- Pinout Compatible with TO-220 Package
- Monolithic Construction with Built-In Base-Emitter Output Resistor
- Thermopad II Construction With Hard Solder for High Reliability

DARLINGTON 4-AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

40, 60, 80 VOLTS
15 WATTS



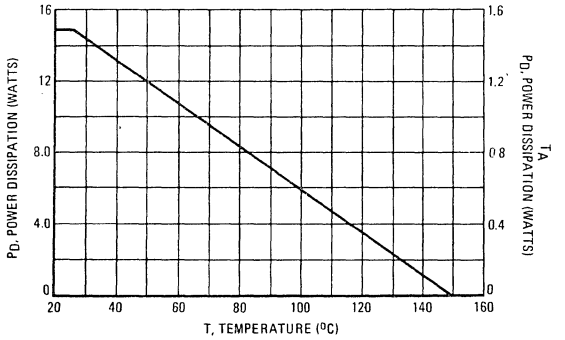
MAXIMUM RATINGS

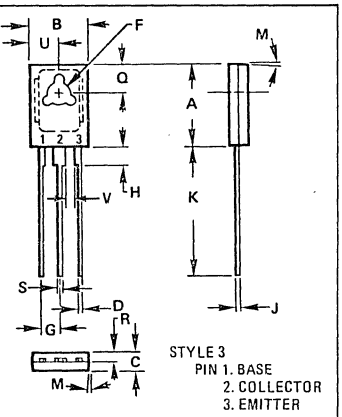
Rating	Symbol	MJE3310 MJE3300	MJE3311 MJE3301	MJE3312 MJE3302	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous Peak	I_C	4.0 6.0			Adc
Base Current	I_B	100			mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012			Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	83.3	°C/W

FIGURE 1 – POWER DERATING





DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	2.16	2.41	0.085	0.095
J	0.38	0.64	0.015	0.025
K	15.37	16.64	0.605	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-03
TO-126

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 10 mAdc, I_B = 0)	MJE3310,MJE3300		40	–	
	MJE3311,MJE3301		60	–	
	MJE3312,MJE3302		80	–	
Collector-Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 20 Vdc, I_B = 0)	MJE3310,MJE3300		–	100	
(V_{CE} = 30 Vdc, I_B = 0)	MJE3311,MJE3301		–	100	
(V_{CE} = 40 Vdc, I_B = 0)	MJE3312,MJE3302		–	100	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = Rated $V_{CEO(sus)}$, I_E = 0)			–	1.0	
(V_{CB} = Rated $V_{CEO(sus)}$, I_E = 0, T_C = 100°C)			–	100	
Emitter Cutoff Current		I_{EBO}	–	1.0	μAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)			1000	–	
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)			750	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	–	1.5	Vdc
(I_C = 1.5 Adc, I_B = 6.0 mAdc)					
Base-Emitter Saturation Voltage		$V_{BE(sat)}$	–	2.5	Vdc
(I_C = 1.5 Adc, I_B = 6.0 mAdc)					
Base-Emitter On Voltage		$V_{BE(on)}$	–	2.5	Vdc
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)					
Output Diode Voltage Drop		V_{EC}	–	2.0	Vdc
(I_{EC} = 2.0 Adc)					
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	20	–	MHz
(I_C= 1.0 Adc, V_{CE} = 2.0 Vdc)					

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – ACTIVE-REGION SAFE OPERATING AREA

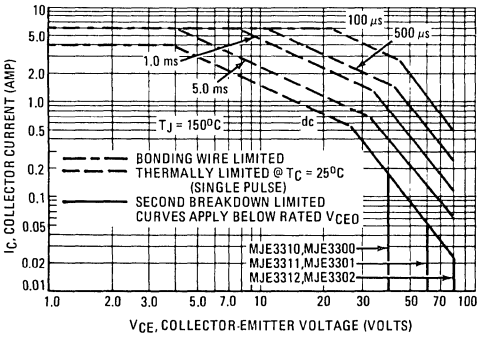


FIGURE 3 – TYPICAL DC CURRENT GAIN

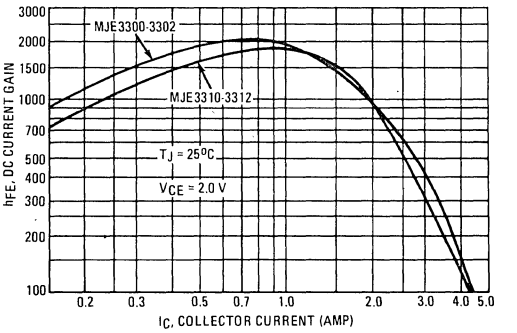
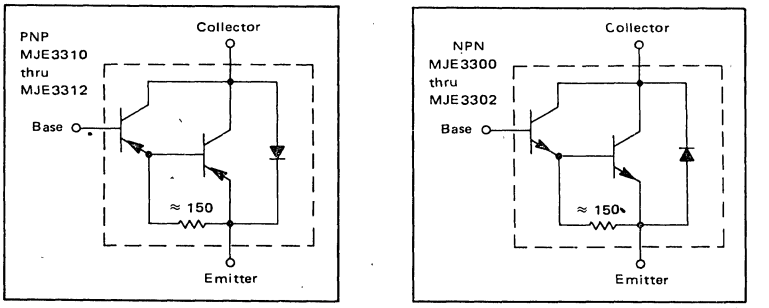


FIGURE 4 – DARLINGTON CIRCUIT SCHEMATIC



MJE3439 (SILICON)
MJE3440

NPN SILICON HIGH-VOLTAGE POWER TRANSISTORS

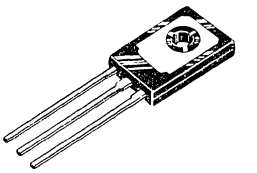
. . . designed for use in line-operated equipment requiring high f_T.

- High DC Current Gain –
  h_{FE} = 40-160 @ I_C = 20 mAdc
- Current-Gain–Bandwidth Product –
  f_T = 15 MHz (Min) @ I_C = 10 mAdc
- Low Output Capacitance –
  C_{ob} = 10 pF (Max) @ f = 1.0 MHz

0.3 AMPERE

NPN SILICON POWER TRANSISTORS

250-350 VOLTS
15 WATTS



4

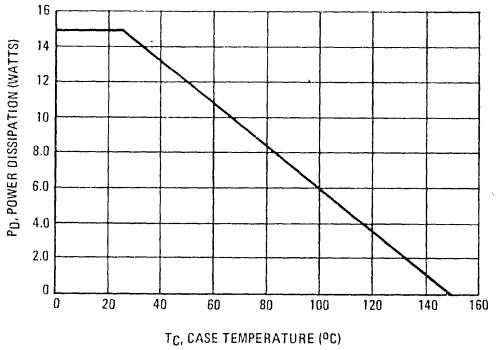
MAXIMUM RATINGS

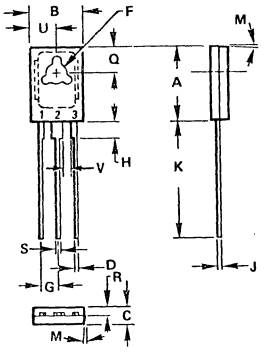
Rating	Symbol	MJE3439	MJE3440	Unit
Collector-Emitter Voltage	V_{CEO}	350	250	Vdc
Collector-Base Voltage	V_{CB}	450	350	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous	I_C	0.3		Adc
Base Current	I_B	150		mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.33	°C/W

FIGURE 1 – POWER-TEMPERATURE DERATING CURVE





STYLE 1
PIN 1. EMITTER
2. COLLECTOR
3. BASE

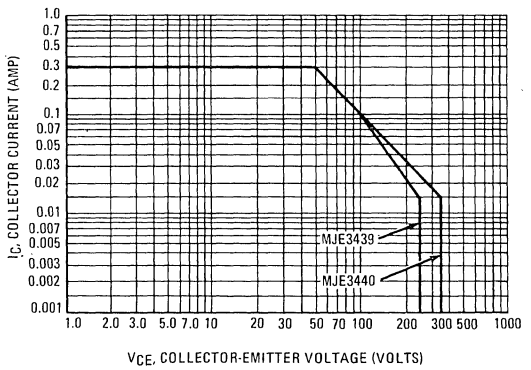
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage		$V_{CEO(sus)}$			Vdc
(I_C = 5.0 mAdc, I_B = 0)	MJE3439		350	–	
(I_C = 50 mAdc, I_B = 0)	MJE3440		250	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 300 Vdc, I_B = 0)	MJE3439		–	20	
(V_{CE} = 200 Vdc, I_B = 0)	MJE3440		–	50	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 450 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	MJE3439		–	500	
(V_{CE} = 300 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	MJE3440		–	500	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 350 Vdc, I_E = 0)	MJE3439		–	20	
(V_{CB} = 250 Vdc, I_E = 0)	MJE3440		–	20	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	20	μAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			–
(I_C = 2.0 mAdc, V_{CE} = 10 Vdc)			30	–	
(I_C = 20 mAdc, V_{CE} = 10 Vdc)			40	160	
Collector-Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 4.0 mAdc)		$V_{CE(sat)}$	–	0.5	Vdc
Base-Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 4.0 mAdc)		$V_{BE(sat)}$	–	1.3	Vdc
Base-Emitter On Voltage (I_C = 50 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	–	0.8	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 5.0 MHz)		f_T	15	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	10	pF
Small-Signal Current Gain (I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	–	–

FIGURE 2 – ACTIVE-REGION SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C-V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

MJE13002
MJE13003

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJE13002 and MJE13003 are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switch-mode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

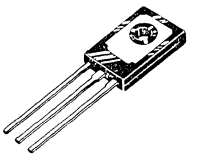
SPECIFICATION FEATURES:

- Reverse Biased SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 0.5 to 1.5 Amp, 25 and 100°C . . . t_c @ 1 A, 100°C is 290 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

1.5 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
40 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



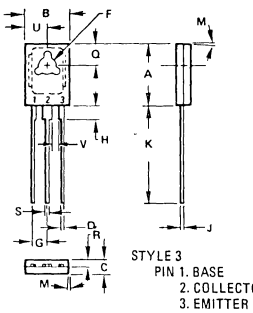
MAXIMUM RATINGS

Rating	Symbol	MJE13002	MJE13003	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	1.5 3		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	0.75 1.5		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	2.25 4.5		Adc
Total Power Dissipation@T_A = 25°C Derate above 25°C	P_D	1.4 11.2		Watts mW/°C
Total Power Dissipation@T_C = 25°C Derate above 25°C	P_D	40 320		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.12	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	89	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 3
PIN 1. BASE
2. COLLECTOR
3. EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	2.16	2.41	0.085	0.095
J	0.38	0.64	0.015	0.025
K	15.37	16.64	0.605	0.655
M	30° TYP		30° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-03
TO-126

4

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)	MJE13002	$V_{CEO(sus)}$	300	–	–	Vdc
	MJE13003		400	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	1	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			–	–	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 1			Adc
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}				–
(I_C = 0.5 Adc, V_{CE} = 2 Vdc)			8	–	40	
(I_C = 1 Adc, V_{CE} = 2 Vdc)			5	–	25	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 0.5 Adc, I_B = 0.1 Adc)			–	–	0.5	
(I_C = 1 Adc, I_B = 0.25 Adc)			–	–	1	
(I_C = 1.5 Adc, I_B = 0.5 Adc)			–	–	3	
(I_C = 1 Adc, I_B = 0.25 Adc, T_C = 100°C)			–	–	1	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 0.5 Adc, I_B = 0.1 Adc)			–	–	1	
(I_C = 1 Adc, I_B = 0.25 Adc)			–	–	1.2	
(I_C = 1 Adc, I_B = 0.25 Adc, T_C = 100°C)			–	–	1.1	
DYNAMIC CHARACTERISTICS						
Current-Gain – Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T	4	10	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	21	–	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 125 Vdc, I_C = 1 A,	t_d	–	0.05	0.1	μs
Rise Time	I_{B1} = I_{B2} = 0.2 A, t_p = 25 μs,	t_r	–	0.5	1	μs
Storage Time	Duty Cycle ≤ 1%)	t_s	–	2	4	μs
Fall Time		t_f	–	0.4	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Voltage Storage Time	(I_C = 1 A, V_{clamp} = 300 Vdc,	t_{sv}	–	1.7	4	μs
Crossover Time	I_{B1} = 0.2 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_c	–	0.29	0.75	μs

(1)Pulse Test: Pulse width = 300 μs, Duty Cycle = 2%.

FIGURE 1 – FORWARD BIAS SAFE OPERATION AREA

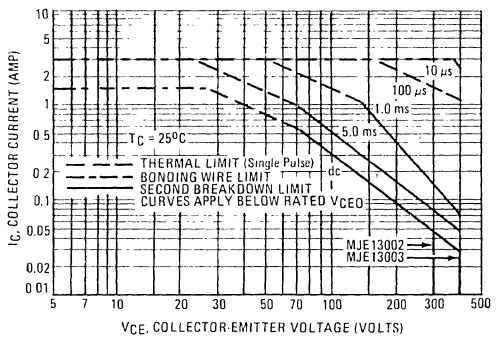
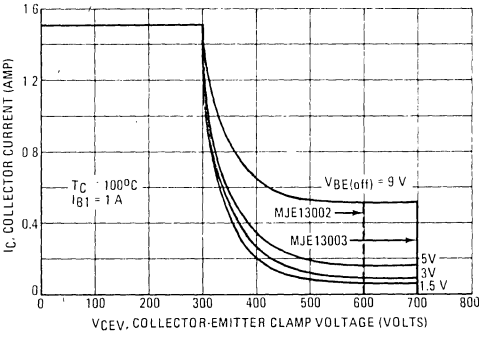
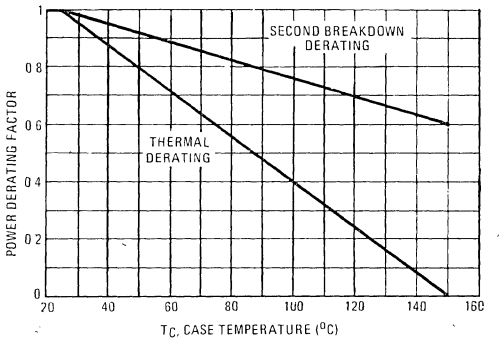


FIGURE 2 – REVERSE BIAS SAFE OPERATING AREA



The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

FIGURE 3 – FORWARD BIAS POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse bias safe operating area data (Figure 2) is discussed in the designer's application section.

FIGURE 4 – THERMAL RESPONSE

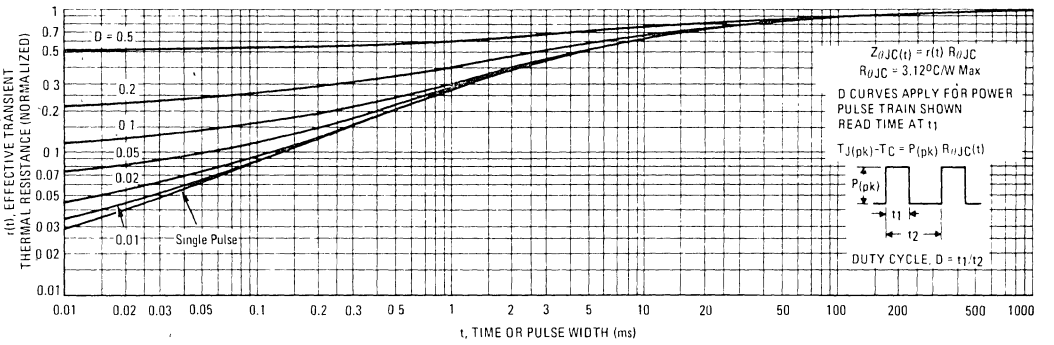


FIGURE 5 – DC CURRENT GAIN

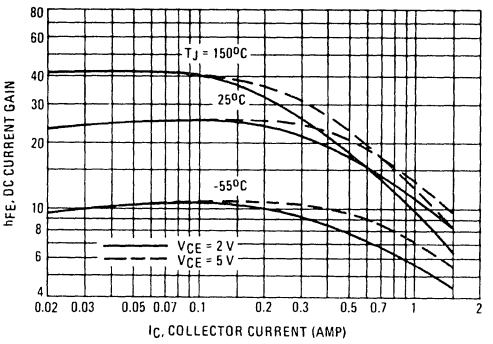


FIGURE 6 – COLLECTOR SATURATION REGION

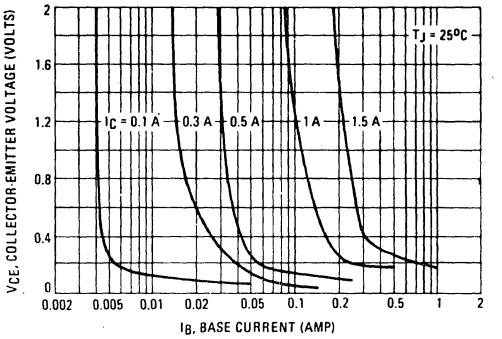


FIGURE 7 – BASE-EMITTER VOLTAGE

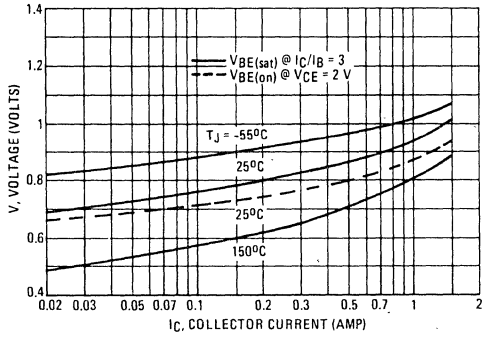


FIGURE 8 – COLLECTOR-EMITTER SATURATION REGION

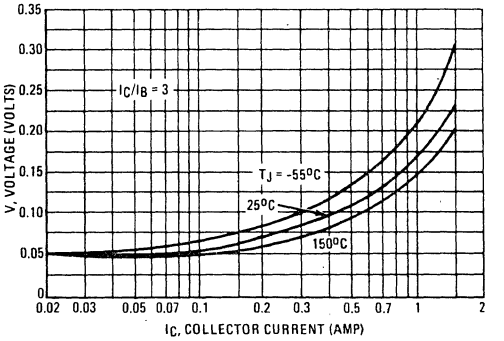


FIGURE 9 – COLLECTOR CUTOFF REGION

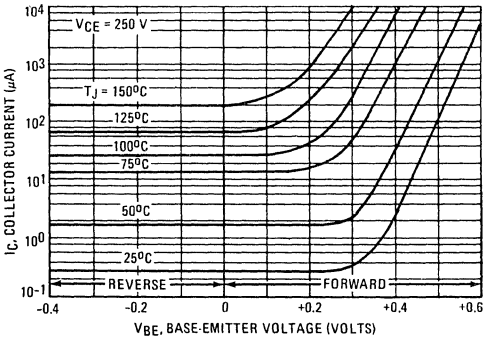


FIGURE 10 – CAPACITANCE

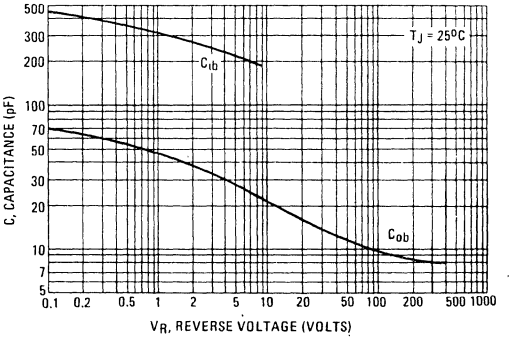
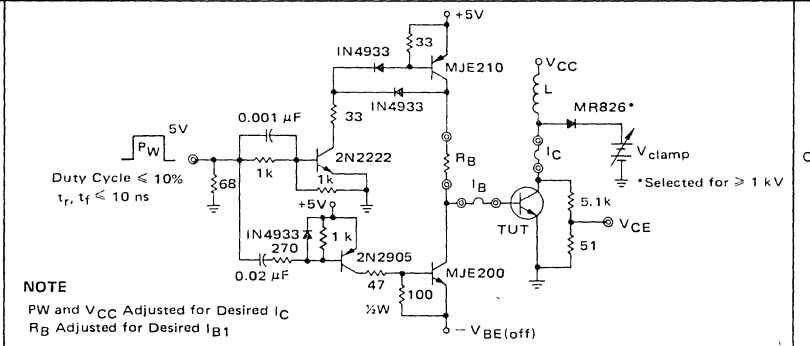
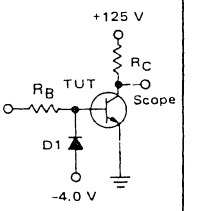
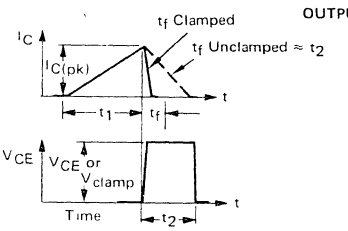
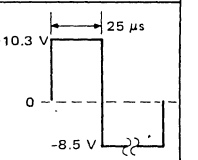


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS		
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~200 Turns) #20 GAP for 30 mH/2A L_{coil} = 50 mH V_{CC} = 20 V V_{clamp} = 300 Vdc	V_{CC} = 125 V R_C = 125 Ω D1 = 1N5820 or Equiv. R_B = 47 Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope-Tektronics 475 or Equivalent	 t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C

DESIGNERS INFORMATION FOR APPLICATIONS AND SWITCHMODE SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-588, AN-719, AN-737, AN-752, AN-767 and Engineering Bulletin EB-39.

VOLTAGE REQUIREMENTS (continued)

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.
(2) The turn-on time does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 1).
(3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 1 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 11 – TURN-ON TIME

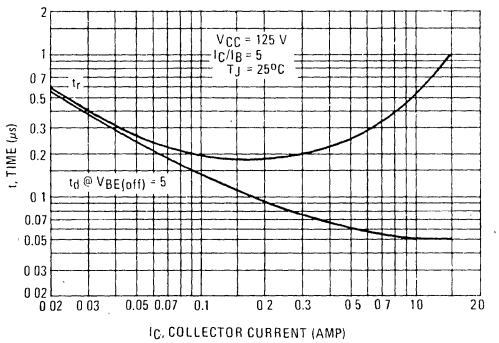


FIGURE 12 – TURN-OFF TIME

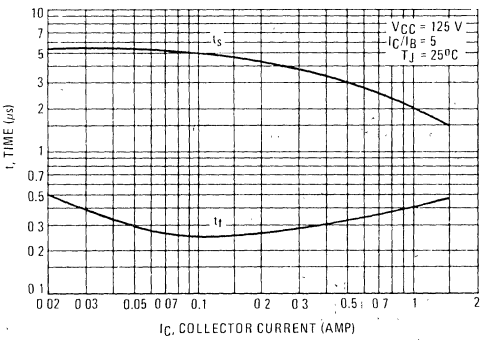


FIGURE 13 – INDUCTIVE SWITCHING MEASUREMENTS

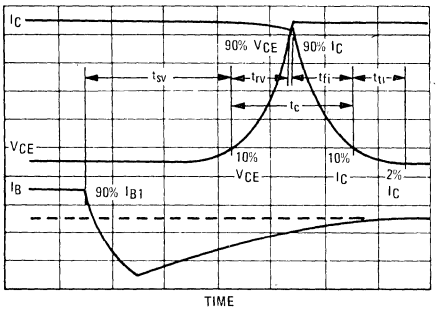


FIGURE 14 – TYPICAL INDUCTIVE SWITCHING WAVEFORMS
(at 300 V and 1 A with I_{B1} = 0.2 A and $V_{BE(off)}$ = 5.0 V)

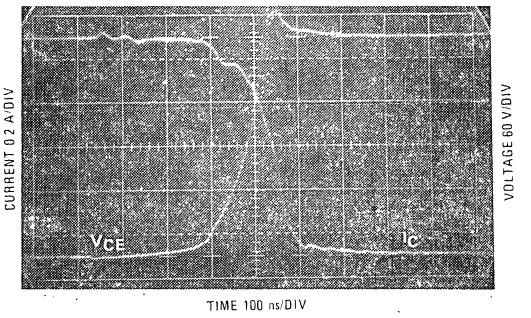


TABLE 2 – APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

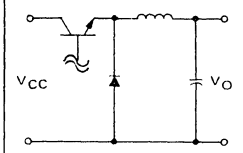
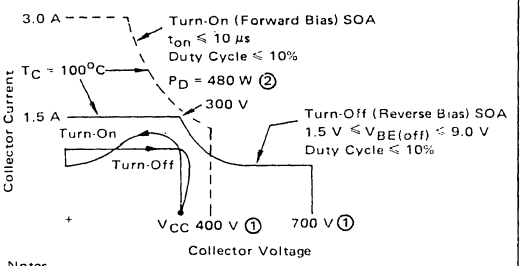
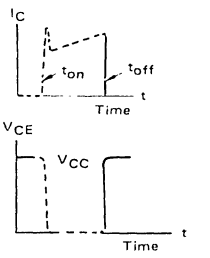
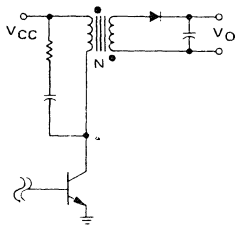
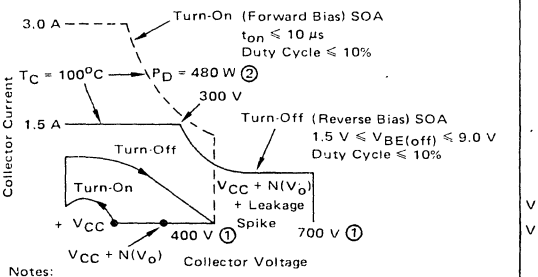
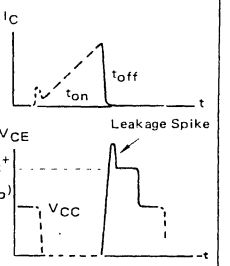
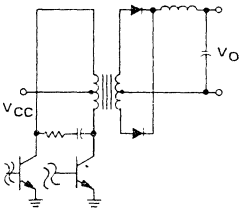
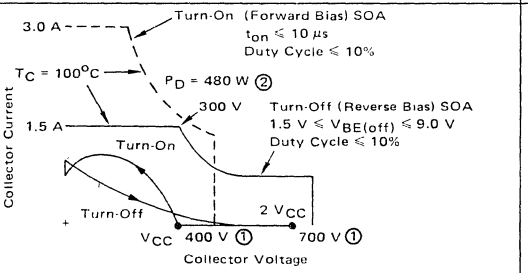
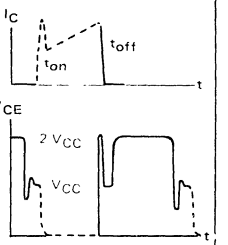
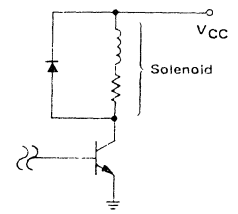
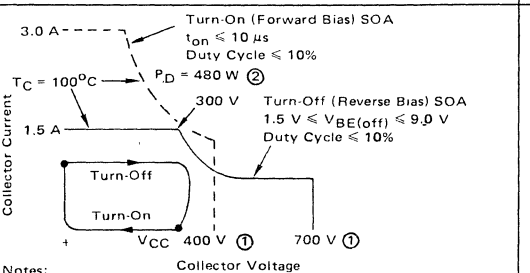
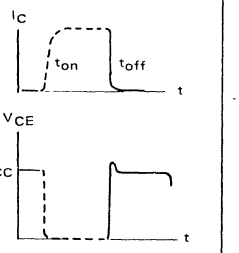
	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 	 Notes. ① MJE13003 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are Shown, MJE13002 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
B	**RINGING CHOKE INVERTER** 	 Notes: ① MJE13003 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13002 Ratings Are 100 V Lower. ② See AN-569 For Pulse Power Derating Procedure	
C	**PUSH-PULL INVERTER/CONVERTER** 	 Notes: ① MJE13003 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13002 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
D	**SOLENOID DRIVER** 	 Notes: ① MJE13003 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13002 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	

TABLE 3 – TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} μs	t_{rv} μs	t_{fi} μs	t_{ti} μs	t_c μs
0.5	25	1.3	0.23	0.30	0.35	0.30
	100	1.6	0.26	0.30	0.40	0.36
1	25	1.5	0.10	0.14	0.05	0.16
	100	1.7	0.13	0.26	0.06	0.29
1.5	25	1.8	0.07	0.10	0.05	0.16
	100	3	0.08	0.22	0.08	0.28

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

4

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CE}
t_{rv} = Voltage Rise Time, 10-90% V_{CE}
t_{fi} = Current Fall Time, 90-10% I_C
t_{ti} = Current Tail, 10-2% I_C
t_c = Crossover Time, 10% V_{CE} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

MJE13004
MJE13005

Designers Data Sheet

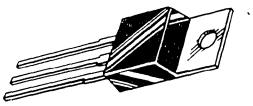
SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTORS

The MJE13004 and MJE13005 are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switchmode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 2 to 4 Amp, 25 and 100°C . . . t_c @ 3A, 100°C is 180 ns (Typ)
- 700 V Blocking Capability
- SOA and Switching Applications Information.

4 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
75 WATTS



Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.

4

MAXIMUM RATINGS

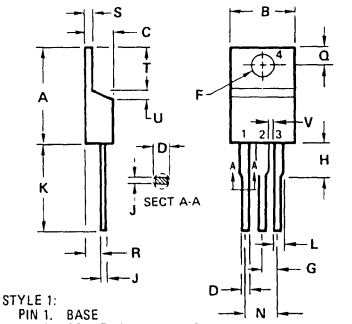
Rating	Symbol	MJE13004	MJE13005	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	4 8		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	2 4		Adc
Emitter Current – Continuous – Peak (1)	I_E I_{EM}	6 12		Adc
Total Power Dissipation@T_A = 25°C Derate above 25°C	P_D	2 16		Watts mW/°C
Total Power Dissipation@T_C = 25°C Derate above 25°C	P_D	75 600		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

▲Trademark of Motorola Inc.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE
1 DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0) MJE13004 / MJE13005	$V_{CEO(sus)}$	300 / 400	– / –	– / –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	–	1	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	–	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 1		
Clamped Inductive SOA with Base Reverse Biased	–		See Figure 2		
***ON CHARACTERISTICS**					
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc)	h_{FE}	10	–	60	–
(I_C = 2 Adc, V_{CE} = 5 Vdc)		8	–	40	
Collector-Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)	$V_{CE(sat)}$	–	–	0.5	Vdc
(I_C = 2 Adc, I_B = 0.5 Adc)		–	–	0.6	
(I_C = 4 Adc, I_B = 1 Adc)		–	–	1	
(I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)		–	–	1	
Base-Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)	$V_{BE(sat)}$	–	–	1.2	Vdc
(I_C = 2 Adc, I_B = 0.5 Adc)		–	–	1.6	
(I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)		–	–	1.5	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	4	–	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	65	–	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 125 Vdc, I_C = 2 A, I_{B1} = I_{B2} = 0.4 A, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	–	0.025	0.1	μs
Rise Time	t_r	–	0.3	0.7	μs
Storage Time	t_s	–	1.7	3.5	μs
Fall Time	t_f	–	0.4	0.9	μs
Inductive Load, Clamped (Table 1, Figure 13)					
Voltage Storage Time (I_C = 2 A, V_{clamp} = 300 Vdc, I_{B1} = 0.4 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	0.9	2.3	μs
Crossover Time	t_c	–	0.32	0.9	μs

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 – FORWARD BIAS SAFE OPERATING AREA

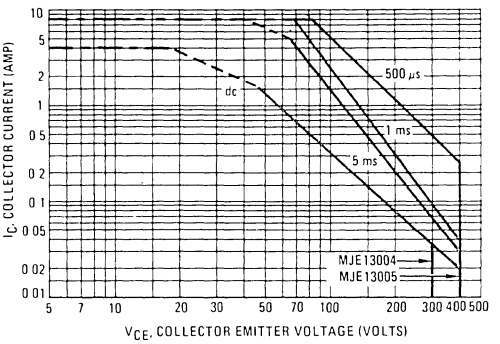
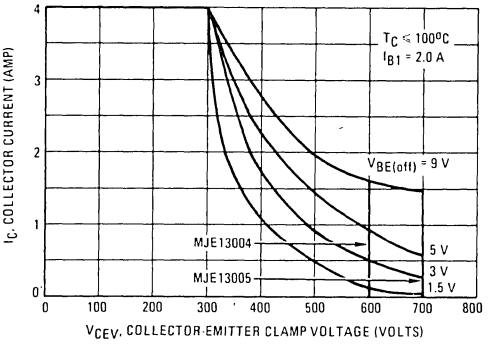


FIGURE 2 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown

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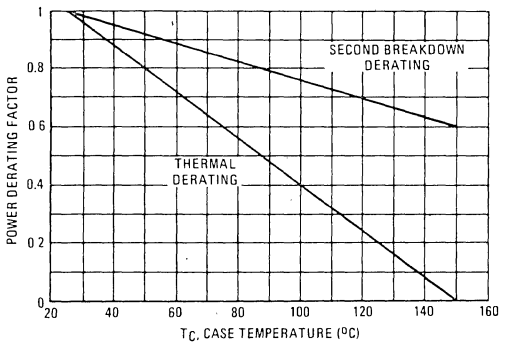
FIGURE 3 – FORWARD BIAS POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

FIGURE 4 – TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]

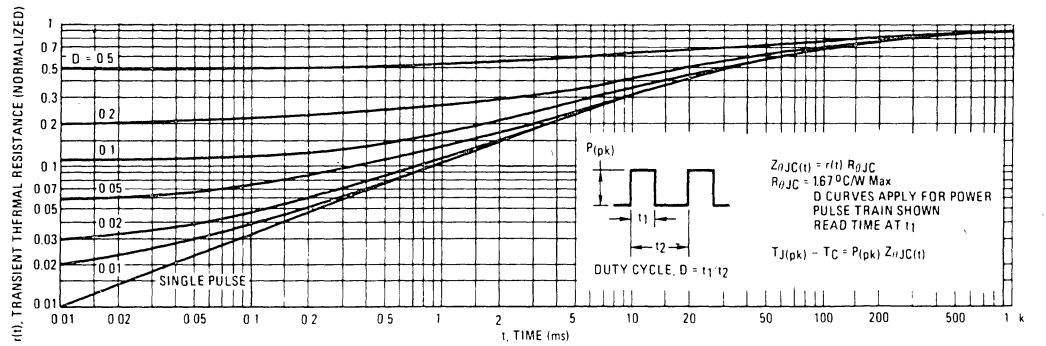


FIGURE 5 –DC CURRENT GAIN

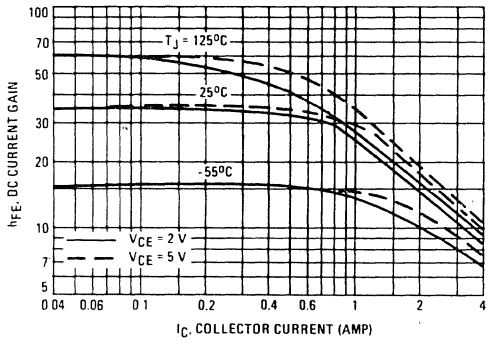


FIGURE 6 – COLLECTOR SATURATION REGION

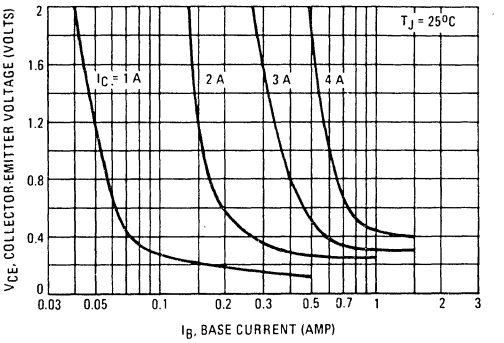


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FIGURE 7 – BASE-EMITTER VOLTAGE

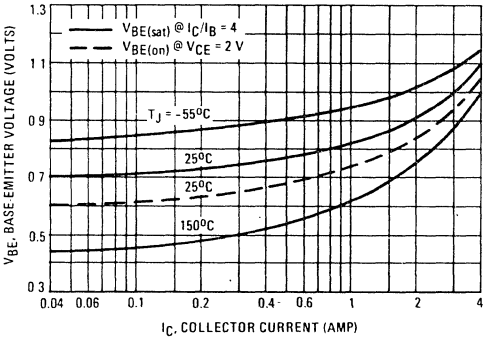


FIGURE 8 – COLLECTOR-EMITTER SATURATION VOLTAGE

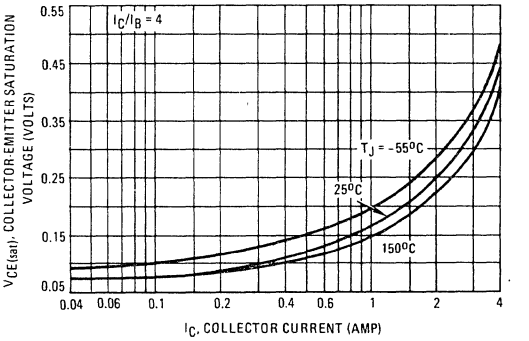


FIGURE 9 – COLLECTOR CUTOFF REGION

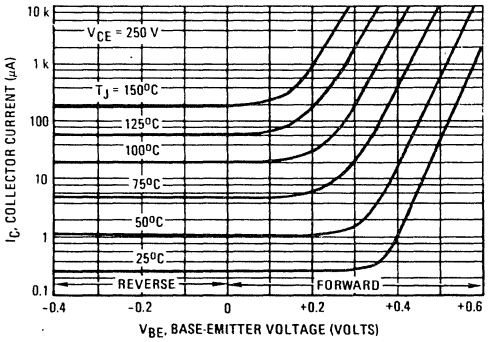


FIGURE 10 – CAPACITANCE

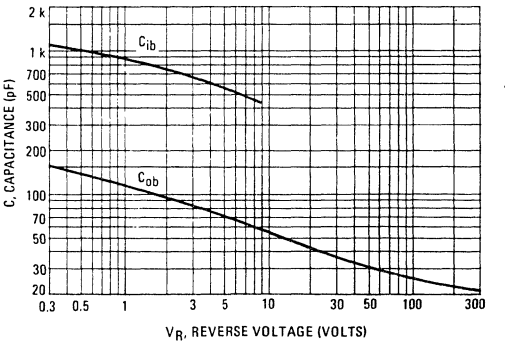
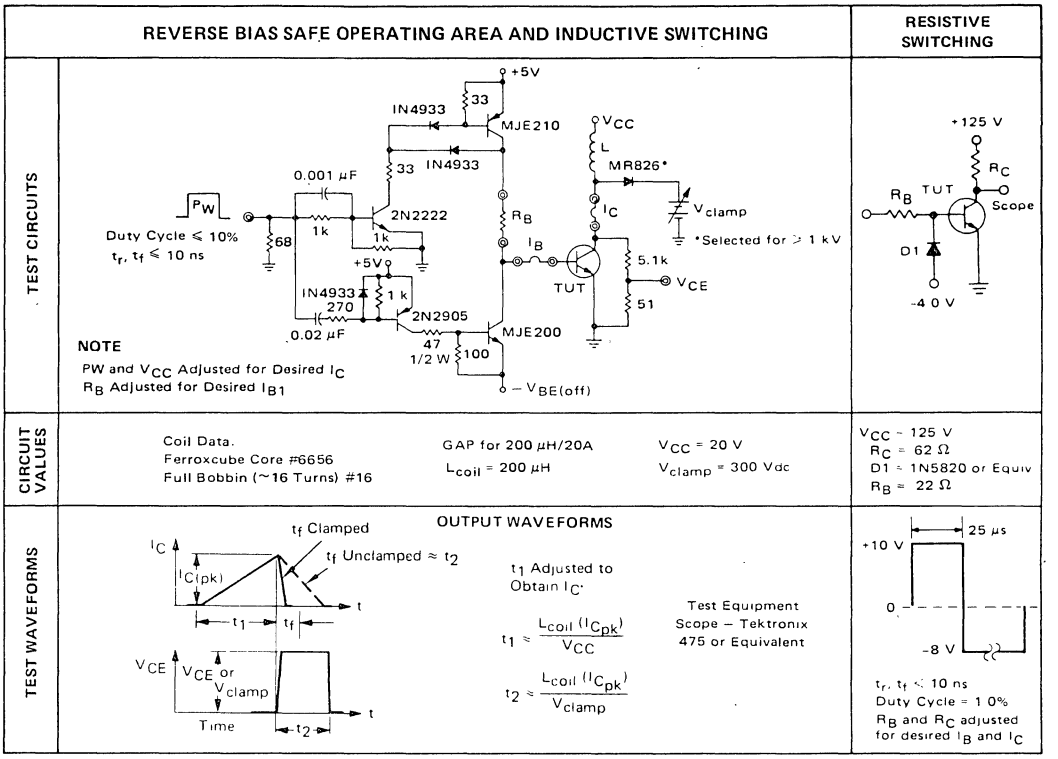


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE



APPLICATIONS INFORMATION FOR SWITCHMODE▲ SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-719, AN-737, AN-767, AN-752

VOLTAGE REQUIREMENTS (continued)

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.

(2) The turn-on time does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 1).

(3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 5 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 11 – TURN-ON TIME

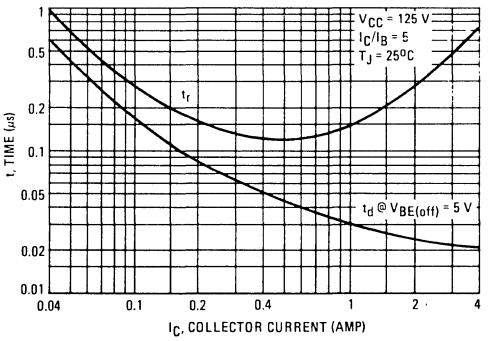


FIGURE 12 – TURN-OFF TIME

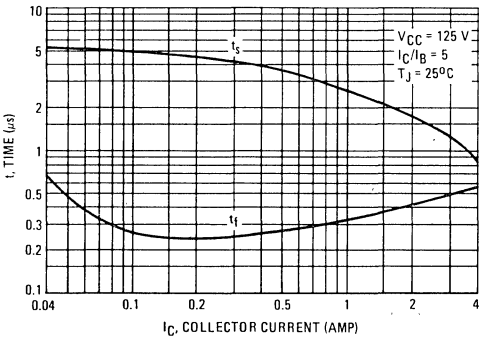


FIGURE 13 – INDUCTIVE SWITCHING MEASUREMENTS

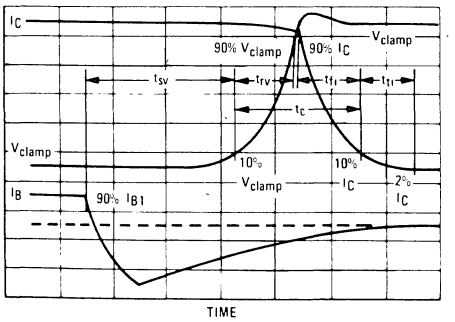


FIGURE 14 – TYPICAL INDUCTIVE SWITCHING WAVEFORMS
(at 300 V and 4 A with I_{B1} = 0.8 A and $V_{BE(off)}$ = 5.0 V)

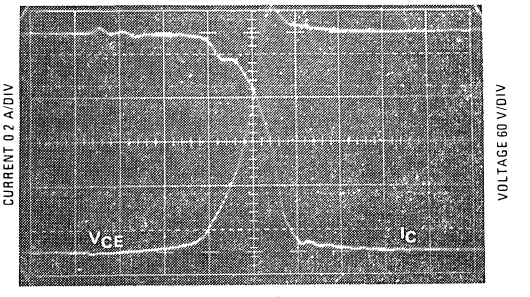


TABLE 2 – APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

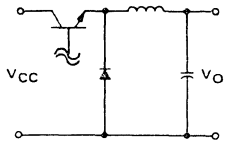
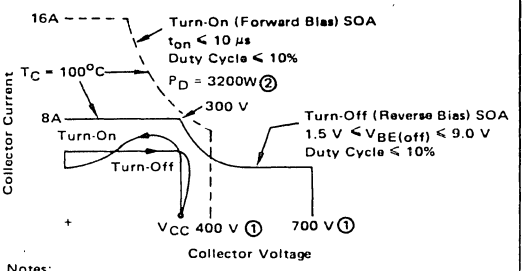
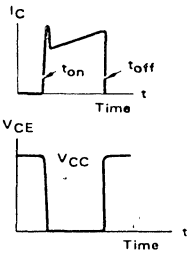
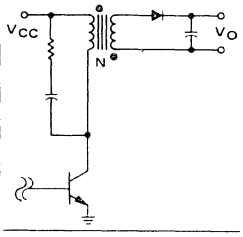
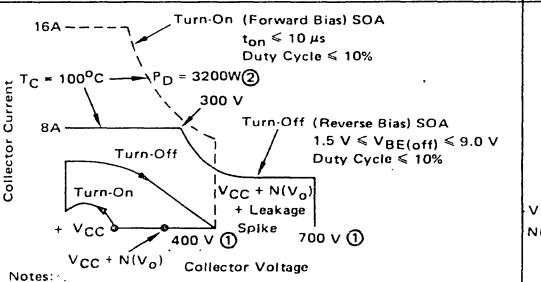
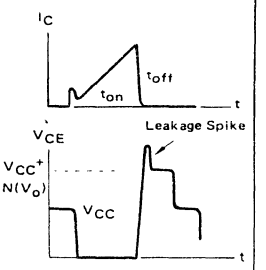
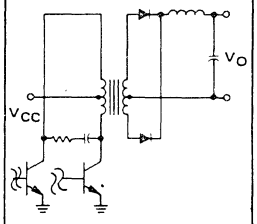
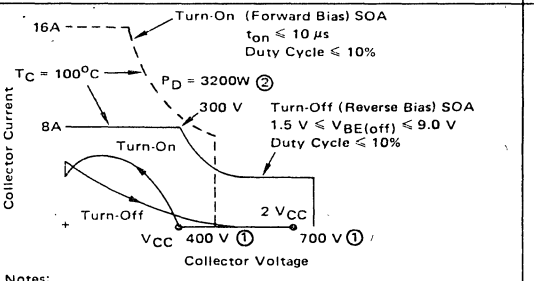
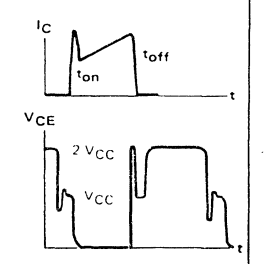
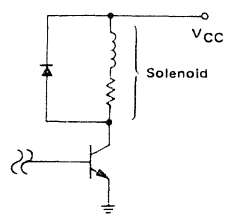
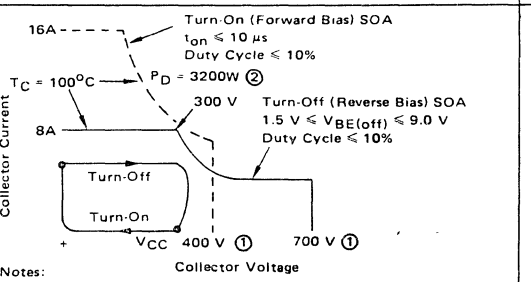
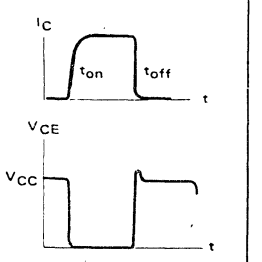
	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 	 Notes: ① MJE13005 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are Shown, MJE13004 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
B	**RINGING CHOKE INVERTER** 	 Notes: ① MJE13005 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13004 Ratings Are 100 V Lower. ② See AN-569 For Pulse Power Derating Procedure	
C	**PUSH-PULL INVERTER/CONVERTER** 	 Notes: ① MJE13005 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13004 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
D	**SOLENOID DRIVER** 	 Notes: ① MJE13005 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13004 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	

TABLE 3 – TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
2	25	600	70	100	80	180
	100	900	110	240	130	320
3	25	650	60	140	60	200
	100	950	100	330	100	350
4	25	550	70	160	100	220
	100	850	110	350	160	390

NOTE: All Data recorded in the inductive Switching Circuit in Table 1.

4

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C(t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

MJE13006
MJE13007

Designers Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJE13006 and MJE13007 are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switchmode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 3 to 8 Amp, 25 and 100°C . . . t_c @ 5A, 100°C is 136 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

MAXIMUM RATINGS

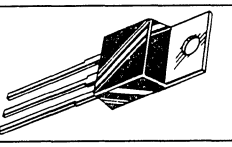
Rating	Symbol	MJE13006	MJE13007	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	8 16		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4 8		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	12 24		Adc
Total Power Dissipation@T_A = 25°C Derate above 25°C	P_D	2 16		Watts mW/°C
Total Power Dissipation@T_C = 25°C Derate above 25°C	P_D	80 640		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

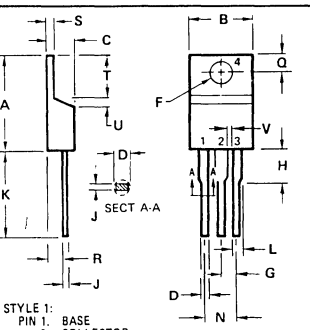
(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

8 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
80 WATTS



Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE
1. DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**						
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)	MJE13006	$V_{CEO(sus)}$	300	–	–	Vdc
	MJE13007		400	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	1	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			–	–	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 1			
Clamped Inductive SOA with Base Reverse Biased		–	See Figure 2			
***ON CHARACTERISTICS**						
DC Current Gain		h_{FE}				–
(I_C = 2 Adc, V_{CE} = 5 Vdc)			8	–	40	
(I_C = 5 Adc, V_{CE} = 5 Vdc)			6	–	30	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)			–	–	1	
(I_C = 5 Adc, I_B = 1 Adc)			–	–	1.5	
(I_C = 8 Adc, I_B = 2 Adc)			–	–	3	
(I_C = 5 Adc, I_B = 1 Adc, T_C = 100°C)			–	–	2	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)			–	–	1.2	
(I_C = 5 Adc, I_B = 1 Adc)			–	–	1.6	
(I_C = 5 Adc, I_B = 1 Adc, T_C = 100°C)			–	–	1.5	
DYNAMIC CHARACTERISTICS						
Current-Gain – Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T	4	–	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	110	–	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 125 Vdc, I_C = 5 A,	t_d	–	0.05	0.1	μs
Rise Time	I_{B1} = I_{B2} = 1 A, t_p = 25 μs,	t_r	–	0.5	1	μs
Storage Time	Duty Cycle ≤ 1%)	t_s	–	1	3	μs
Fall Time		t_f	–	0.15	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Voltage Storage Time	(I_C = 5 A, V_{clamp} = 300 Vdc,	t_{sv}	–	0.86	2.3	μs
Crossover Time	I_{B1} = 1 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_c	–	0.14	0.7	μs

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 – FORWARD BIAS SAFE OPERATING AREA

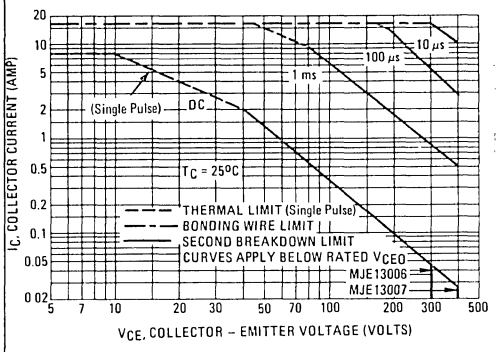
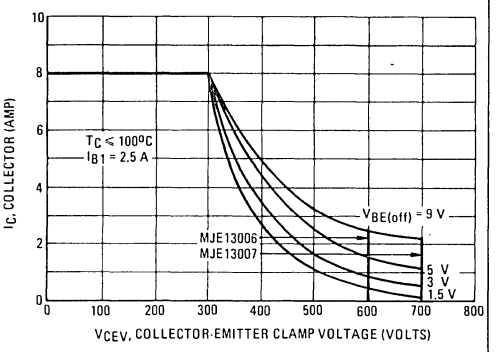
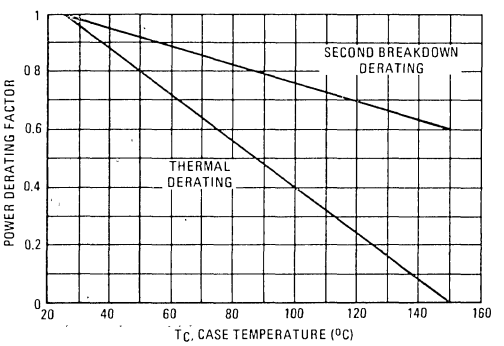


FIGURE 2 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

FIGURE 3 – FORWARD BIAS POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

FIGURE 4 – TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]

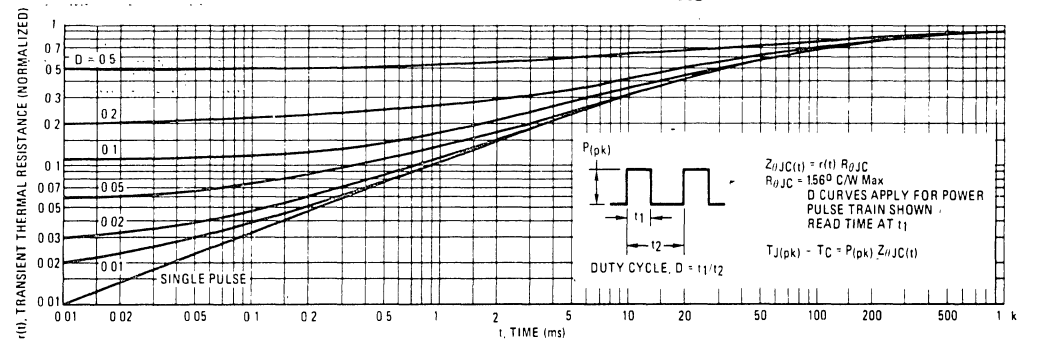


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FIGURE 5 –DC CURRENT GAIN

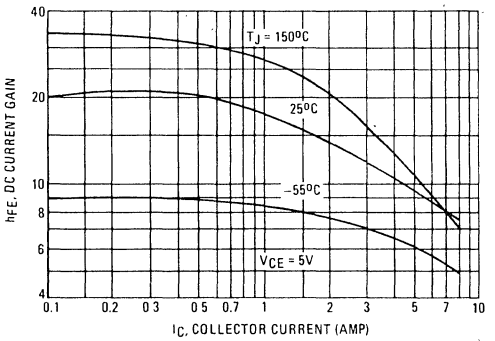


FIGURE 6 – COLLECTOR SATURATION REGION

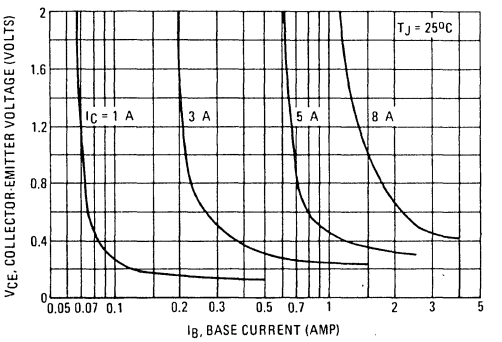


FIGURE 7 – BASE-EMITTER SATURATION VOLTAGE

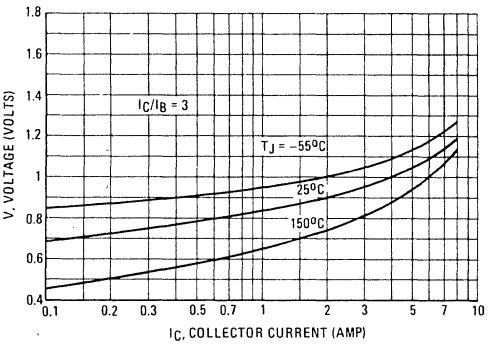


FIGURE 8 – COLLECTOR-EMITTER SATURATION VOLTAGE

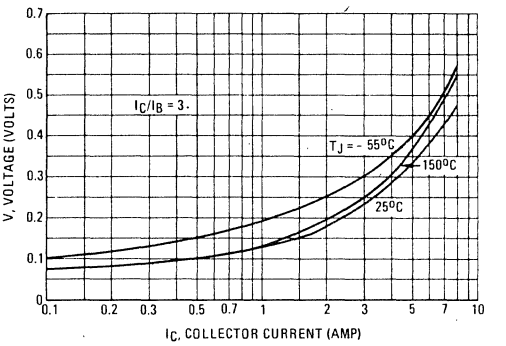


FIGURE 9 – COLLECTOR CUTOFF REGION

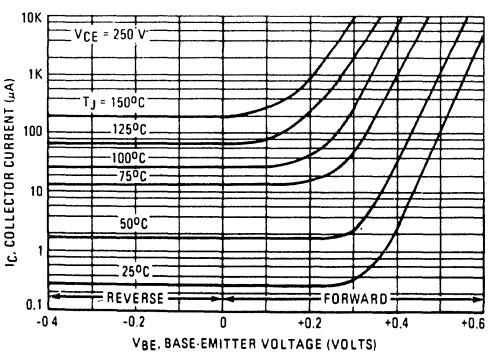


FIGURE 10 – CAPACITANCE

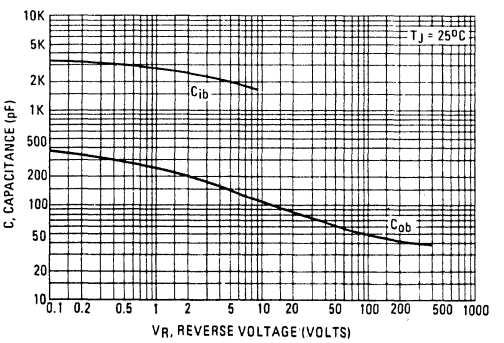


TABLE 2 – APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

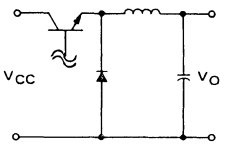
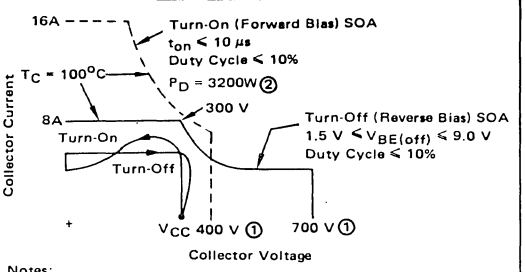
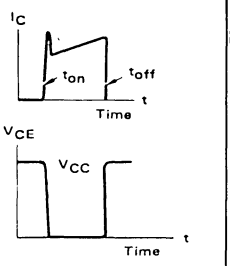
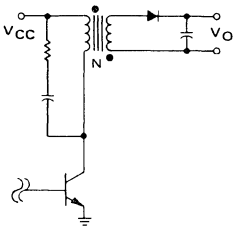
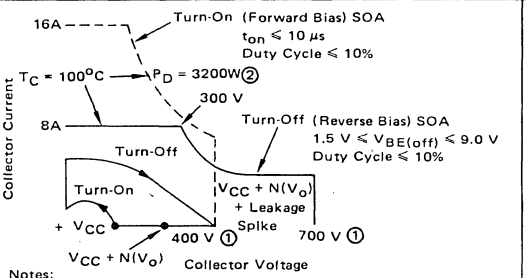
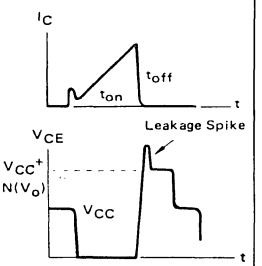
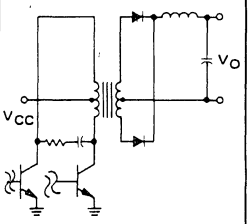
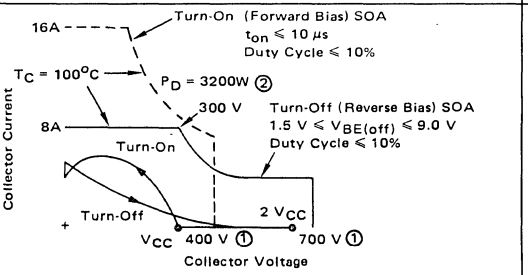
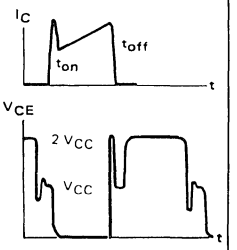
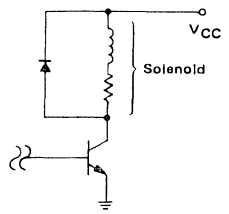
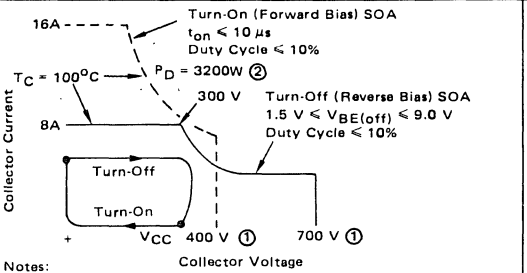
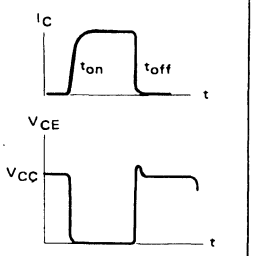
	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 	 Notes: ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are Shown, MJE13006 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
B	**RINGING CHOKE INVERTER** 	 Notes: ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown. MJE13006 Ratings Are 100 V Lower. ② See AN-569 For Pulse Power Derating Procedure	
C	**PUSH-PULL INVERTER/CONVERTER** 	 Notes: ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13006 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
D	**SOLENOID DRIVER** 	 Notes: ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13006 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	

TABLE 3 – TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
3	25	730	115	100	110	200
	100	1000	150	100	150	250
5	25	600	60	23	4	85
	100	860	84	50	10	136
8	25	650	25	26	4	42
	100	880	52	80	20	160

NOTE: All Data recorded in the inductive Switching Circuit in Table 1.

4

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

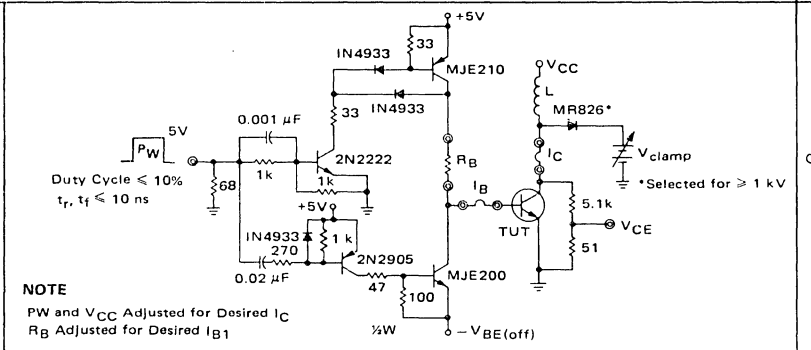
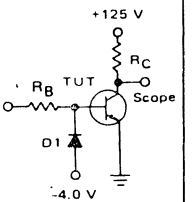
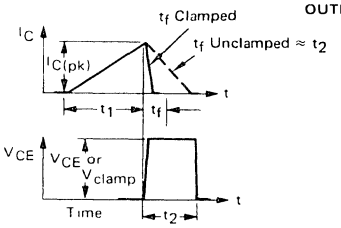
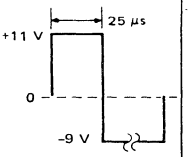
For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS	 NOTE PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}	
CIRCUIT VALUES	Coil Data Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 µH/20A L_{coil} = 200 µH V_{CC} = 20 V V_{clamp} = 300 Vdc	V_{CC} = 125 V R_C = 25 Ω D1 = 1N5820 or Equiv R_B = 10Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	 t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C

APPLICATIONS INFORMATION FOR SWITCHMODE SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-719, AN-737, AN-767, AN-752

VOLTAGE REQUIREMENTS (continued)

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.

(2) The turn-on time does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 1).

(3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 5 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 11 – TURN-ON TIME

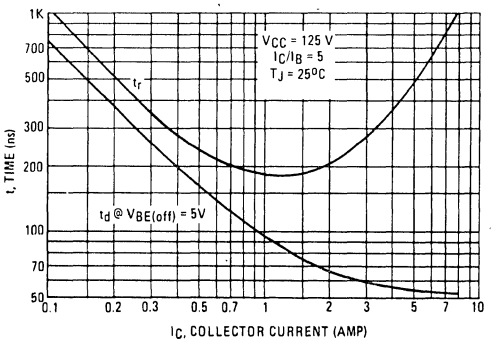


FIGURE 12 – TURN-OFF TIME

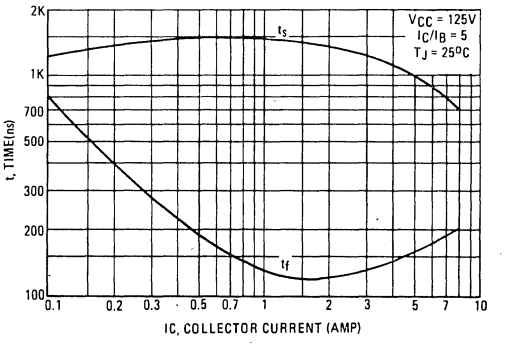


FIGURE 13 – INDUCTIVE SWITCHING MEASUREMENTS

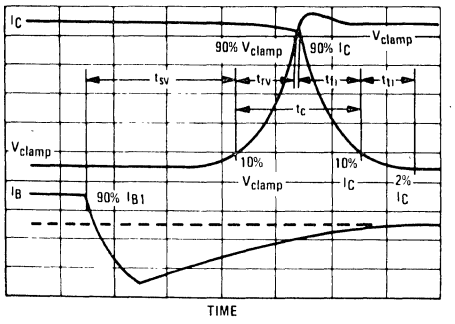
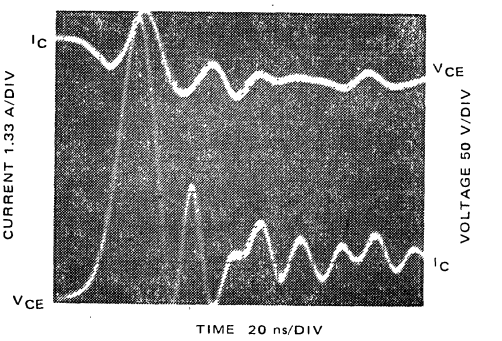


FIGURE 14 – TYPICAL INDUCTIVE SWITCHING WAVEFORMS
(at 300 V and 8A with I_{B1} = 1.6A and $V_{BE(off)}$ = 5 V)



MJE13008
MJE13009

Designer's Data Sheet

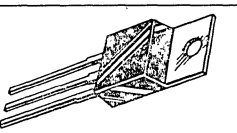
SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The MJE13008 and MJE13009 are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switch-mode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 3 to 12 Amp, 25 and 100°C ... t_c @ 8 A, 100°C is 120 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

12 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
100 WATTS



Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.

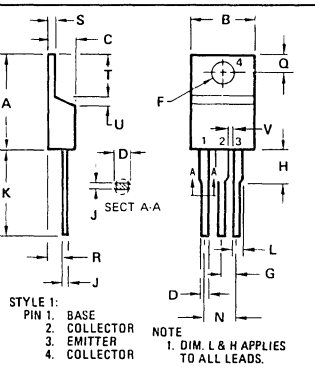
MAXIMUM RATINGS

Rating	Symbol	MJE13008	MJE13009	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	12 24		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	6 12		Adc
Emitter Current – Continuous – Peak (1)	I_E I_{EM}	18 36		Adc
Total Power Dissipation@T_A = 25°C Derate above 25°C	P_D	2 16		Watts mW/°C
Total Power Dissipation@T_C = 25°C Derate above 25°C	P_D	100 800		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE
1. DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	–	0.045	–

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0) MJE13008 / MJE13009	$V_{CEO(sus)}$	300 / 400	– / –	– / –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	–	–	1	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	–	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 1			
Clamped Inductive SOA with Base Reverse Biased	–	See Figure 2			
***ON CHARACTERISTICS**					
DC Current Gain (I_C = 5 Adc, V_{CE} = 5 Vdc)	h_{FE}	8	–	40	
(I_C = 8 Adc, V_{CE} = 5 Vdc)		6	–	30	
Collector-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1Adc)	$V_{CE(sat)}$	–	–	1	Vdc
(I_C = 8 Adc, I_B = 1.6 Adc)		–	–	1.5	
(I_C = 12 Adc, I_B = 3 Adc)		–	–	3	
(I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)		–	–	2	
Base-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1 Adc)	$V_{BE(sat)}$	–	–	1.2	Vdc
(I_C = 8 Adc, I_B = 1.6 Adc)		–	–	1.6	
(I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)		–	–	1.5	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	4	–	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	180	–	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 125 Vdc, I_C = 8 A,	t_d	–	0.06	0.1	μs
Rise Time I_{B1} = I_{B2} = 1.6 A, t_p = 25 μs,	t_r	–	0.45	1	μs
Storage Time Duty Cycle ≤ 1%)	t_s	–	1.3	3	μs
Fall Time	t_f	–	0.2	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)					
Voltage Storage Time (I_C = 8 A, V_{clamp} = 300 Vdc,	t_{sv}	–	0.92	2.3	μs
Crossover Time I_{B1} = 1.6 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_c	–	0.12	0.7	μs

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 – FORWARD BIAS SAFE OPERATING AREA

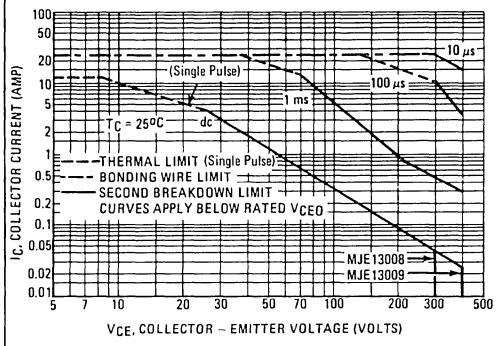
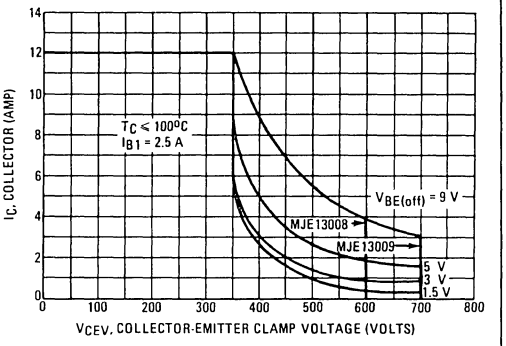
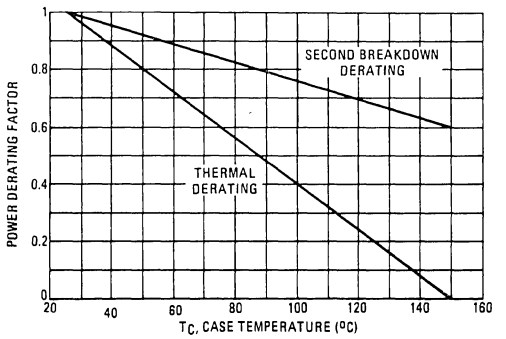


FIGURE 2 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

FIGURE 3 – FORWARD BIAS POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

FIGURE 4 – TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]

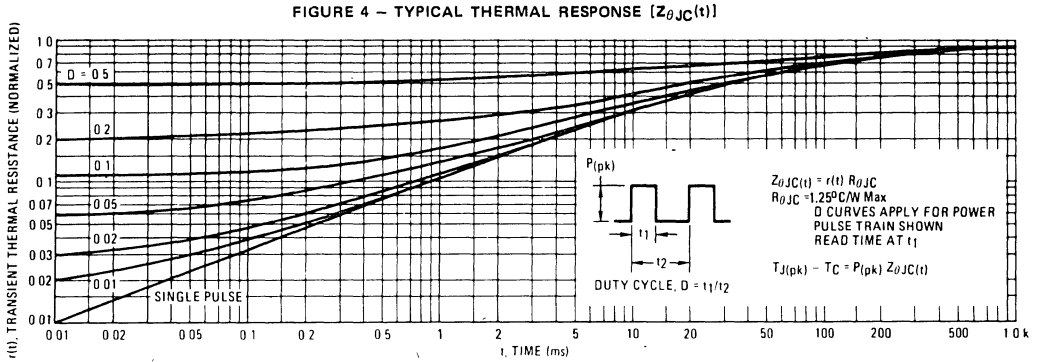


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FIGURE 5 – DC CURRENT GAIN

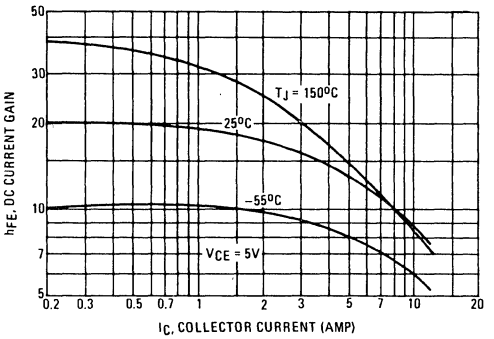


FIGURE 6 – COLLECTOR SATURATION REGION

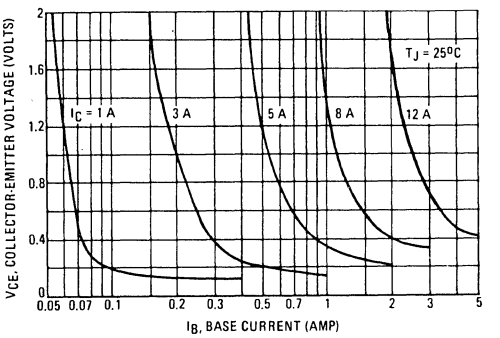


FIGURE 7 – BASE-EMITTER SATURATION VOLTAGE

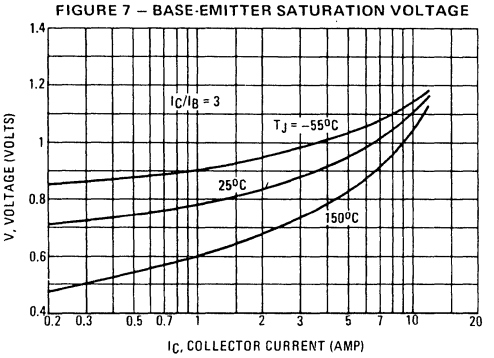


FIGURE 8 – COLLECTOR-EMITTER SATURATION VOLTAGE

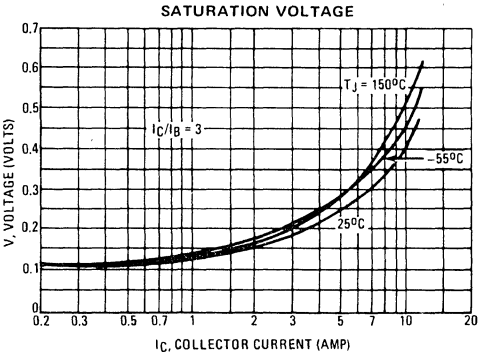


FIGURE 9 – COLLECTOR CUTOFF REGION

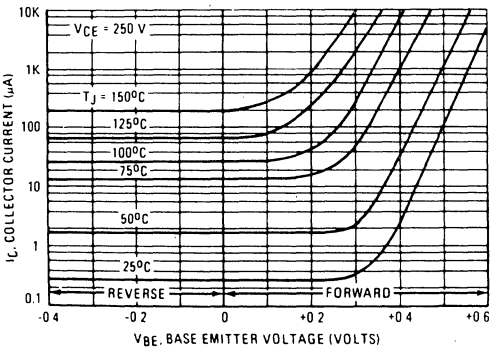


FIGURE 10 – CAPACITANCE

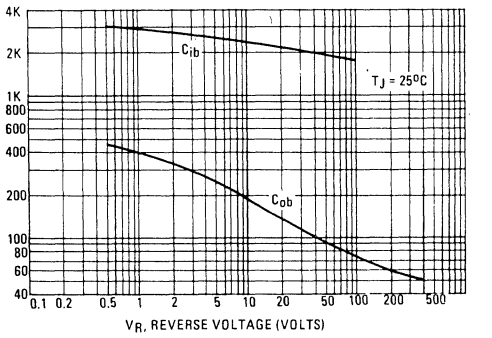


TABLE 2 – APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

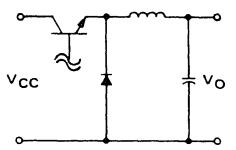
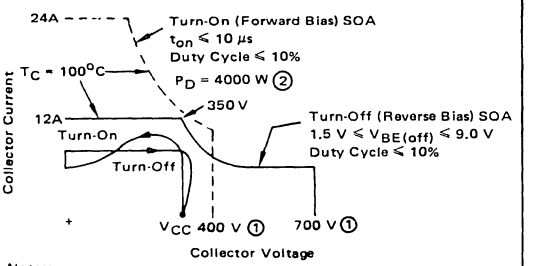
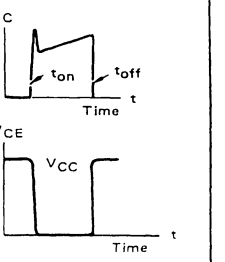
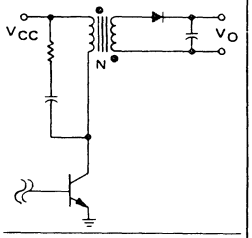
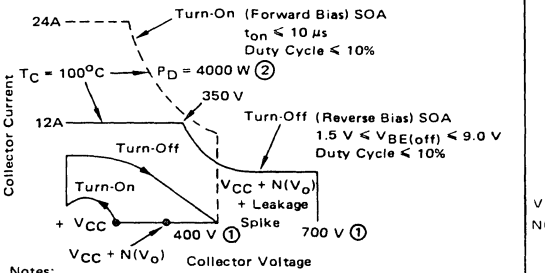
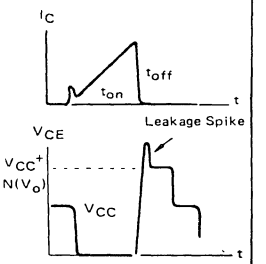
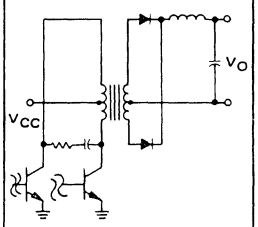
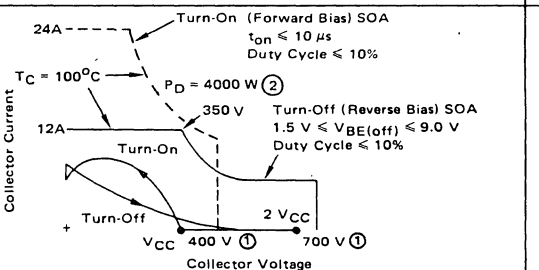
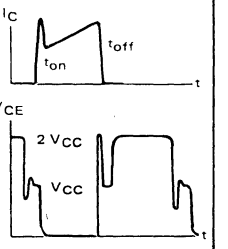
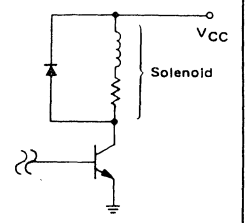
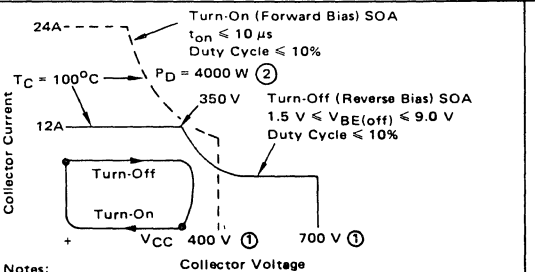
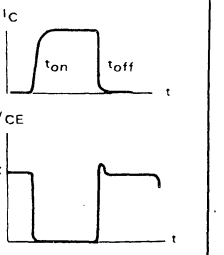
	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 	 Notes: ① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
B	**RINGING CHOKE INVERTER** 	 Notes: ① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower. ② See AN-569 For Pulse Power Derating Procedure	
C	**PUSH-PULL INVERTER/CONVERTER** 	 Notes: ① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
D	**SOLENOID DRIVER** 	 Notes: ① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	

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TABLE 3 – TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
3	25	770	100	150	200	240
	100	1000	230	160	200	320
5	25	630	72	26	10	100
	100	820	100	55	30	180
8	25	720	55	27	2	77
	100	920	70	50	8	120
12	25	640	20	17	2	41
	100	800	32	24	4	54

NOTE: All Data recorded in the Inductive Switching Circuit in Table 1.

4

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

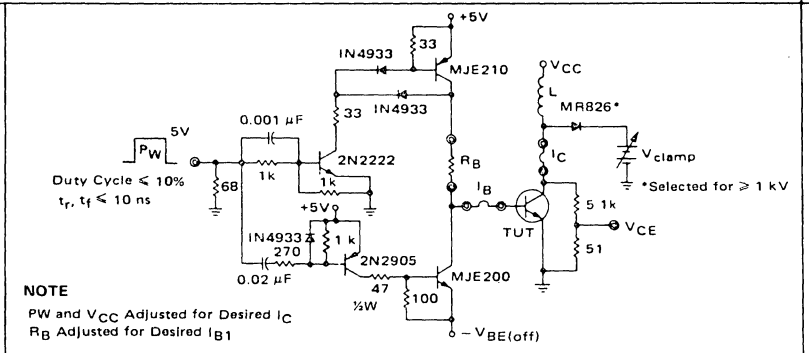
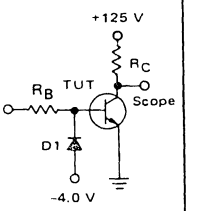
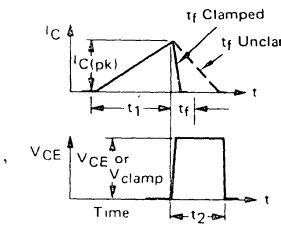
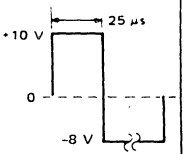
For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS		
CIRCUIT VALUES	Coil Data. Ferroxcube Core #G656 Full Bobbin (~16 Turns) #16 GAP for 200 µH/20A Lcoil = 200 µH VCC = 20 V Vclamp = 300 Vdc	VCC = 125 V RC = 15 Ω D1 = 1N5820 or Equiv RB = 5.6 Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t1 Adjusted to Obtain IC $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	 tr, tf < 10 ns Duty Cycle = 10% RB and RC adjusted for desired IB and IC

APPLICATIONS INFORMATION FOR SWITCHMODE SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-719, AN-737, AN-767, AN-752

VOLTAGE REQUIREMENTS (continued)

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.
(2) The turn-on time does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 1).
(3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 8 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 11 – TURN-ON TIME

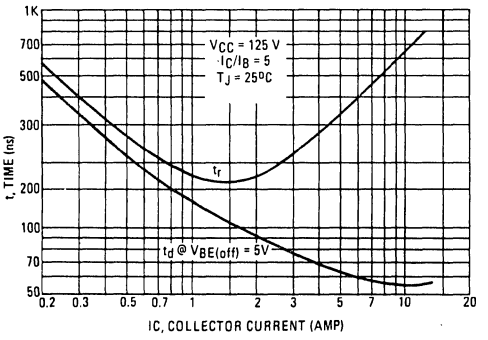


FIGURE 12 – TURN-OFF TIME

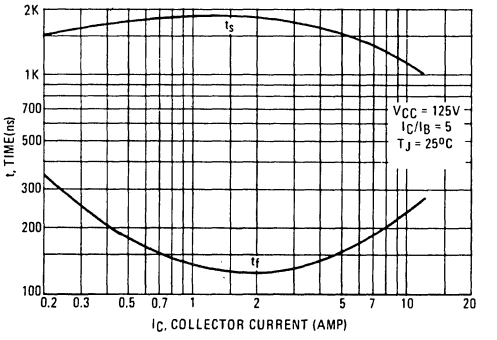


FIGURE 13 – INDUCTIVE SWITCHING MEASUREMENTS

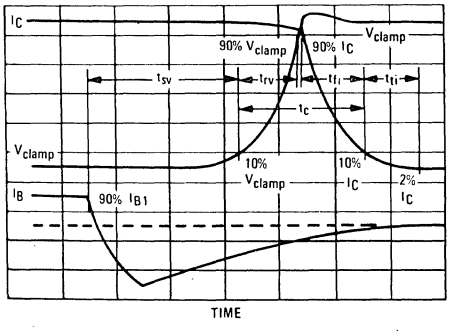
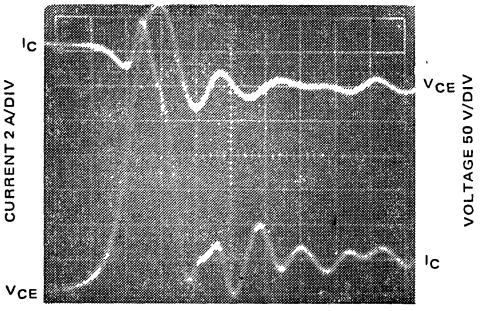


FIGURE 14 – TYPICAL INDUCTIVE SWITCHING WAVEFORMS
(at 300 V and 12 A with I_{B1} = 2.4 A and $V_{BE(off)}$ = 5 V)



NPN PNP

MJE15028 MJE15029
MJE15030 MJE15031

Advance Information

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

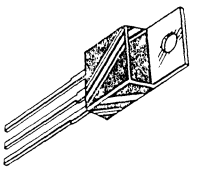
. . . designed for use as high-frequency drivers in audio amplifiers.

- DC Current Gain Specified to 4.0 Amperes
  h_{FE} = 40(Min) @ I_C = 3.0 Adc
  = 20(Min) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 120 Vdc (Min) – MJE15028, MJE15029
  = 150 Vdc (Min) – MJE15030, MJE15031
- High Current Gain – Bandwidth Product
  f_T = 30 MHz (Min) @ I_C = 500 mAdc
- TO-220AB Compact Package
- TO-66 Leadform Also Available

8 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

120–150 VOLTS
50 WATTS



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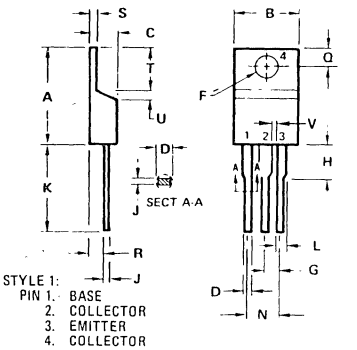
MAXIMUM RATINGS

Rating	Symbol	MJE15028 MJE15029	MJE15030 MJE15031	Unit
Collector-Emitter Voltage	V_{CEO}	120	150	Vdc
Collector-Base Voltage	V_{CB}	120	150	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current -- Continuous Peak	I_C	8.0 16		Adc
Base Current	I_B	2.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.40		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	

CASE 221A-02
TO-220AB

This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 10 mAdc, I_B = 0)	MJE15028, MJE15029		120	–	
	MJE15030, MJE15031		150	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 120 Vdc, I_B = 0)	MJE15028, MJE15029		–	0.1	
(V_{CE} = 150 Vdc, I_B = 0)	MJE15030, MJE15031		–	0.1	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 120 Vdc, I_E = 0)	MJE15028, MJE15029		–	10	
(V_{CB} = 150 Vdc, I_E = 0)	MJE15030, MJE15031		–	10	
Emitter Cutoff Current		I_{EBO}	–	10	μAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.1 Adc, V_{CE} = 2.0 Vdc)			40	–	
(I_C = 2.0 Adc, V_{CE} = 2.0 Vdc)			40	–	
(I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)			40	–	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)			20	–	
DC Current Gain Linearity		h_{FE}	Typ		
(V_{CE} From 2.0V to 20V, I_C From 0.1A to 3A)			2		
(NPN TO PNP)			3		
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	–	0.5	Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)					
Base-Emitter On Voltage		$V_{BE(on)}$	–	1.0	Vdc
(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2)		f_T	30	–	MHz
(I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)					

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2)$f_T = |h_{fe}| \cdot f_{test}$

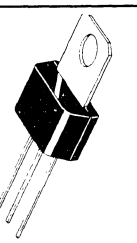
MPS-U01 (SILICON)
MPS-U01A

NPN SILICON ANNULAR TRANSISTORS

. . . designed for complementary symmetry audio circuits to 5 Watts output.

- Excellent Current Gain Linearity — 1.0 mAdc to 1.0 Adc
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 1.0 Adc
- Complements to PNP MPS-U51 and MPS-U51A
- Uniwatt Package for Excellent Thermal Properties — 1.0 Watt @ T_A = 25°C

NPN SILICON AUDIO TRANSISTORS



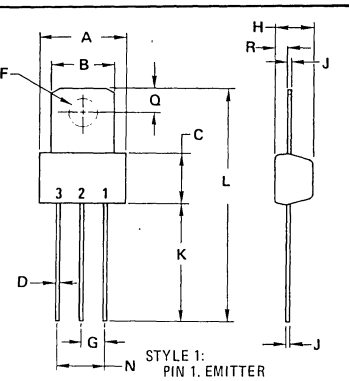
MAXIMUM RATINGS

Rating	Symbol	MPS-U01	MPS-U01A	Unit
Collector-Emitter Voltage	V_{CEO}	30	40	Vdc
Collector-Base Voltage	V_{CB}	40	50	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	2.0		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0		Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W

Uniwatt packages can be To-5 lead formed by adding -5 to the device title and tab formed for flush mounting by adding -1 to the device title.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 10 mAdc, I_B = 0)	MPS-U01	BV_{CEO}	30	–	Vdc
	MPS-U01A		40	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	MPS-U01	BV_{CBO}	40	–	Vdc
	MPS-U01A		50	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	MPS-U01	I_{CBO}	–	0.1	μAdc
(V_{CB} = 40 Vdc, I_E = 0)	MPS-U01A		–	0.1	
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 1.0 Vdc)		h_{FE}	55	–	–
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)			50	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	–	0.5	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)		f_T	50	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	–	20	pF

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 – DC CURRENT GAIN

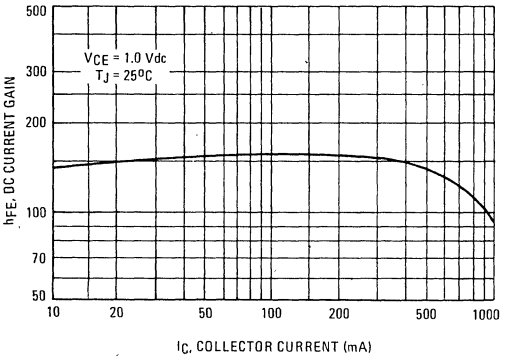


FIGURE 2 – "ON" VOLTAGES

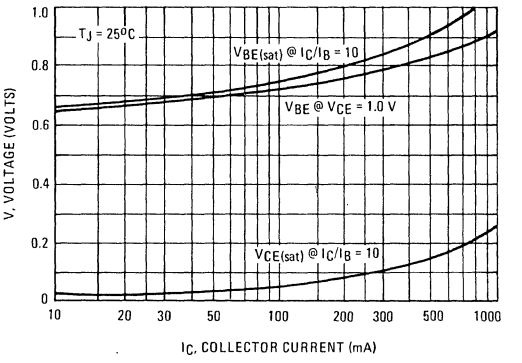
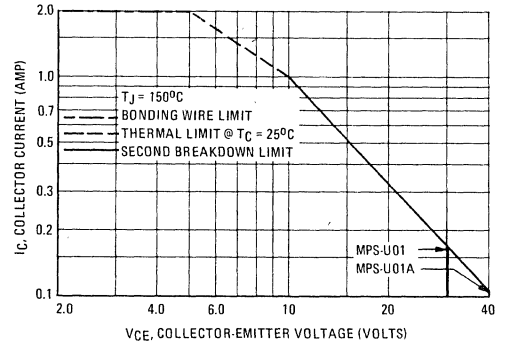


FIGURE 3 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

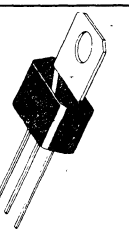
MPS - U02 (SILICON)

NPN SILICON ANNULAR AMPLIFIER TRANSISTOR

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Power Dissipation – P_D = 10 W @ T_C = 25°C
- Complement to PNP MPS-U52

NPN SILICON AMPLIFIER TRANSISTOR



MAXIMUM RATINGS

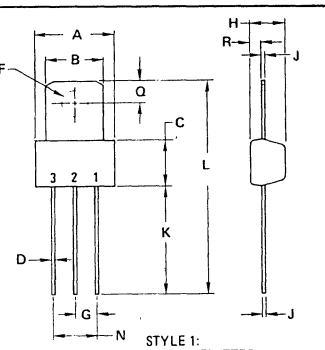
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	800	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R\theta_{JA}$	125	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	40	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	60	-	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	I_{CBO}	-	100	nAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 150 mAdc, V_{CE} = 10 Vdc) (I_C = 500 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 50 50 30	 - 300 -	-
Collector-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{CE(sat)}$	-	0.4	Vdc
Base-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{BE(sat)}$	-	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain–Bandwidth Product (I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	100	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	-	20	pF



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(COLLECTOR CONNECTED TO TAB)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

FIGURE 1 – NORMALIZED DC CURRENT GAIN

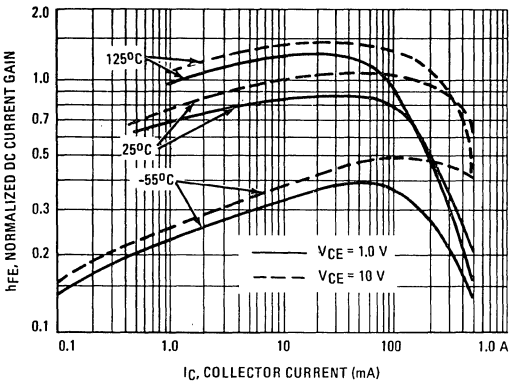


FIGURE 2 – COLLECTOR-EMITTER SATURATION VOLTAGE versus BASE CURRENT

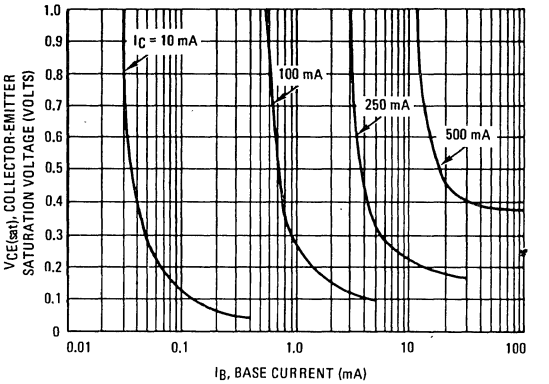


FIGURE 3 – BASE-EMITTER VOLTAGE versus COLLECTOR CURRENT

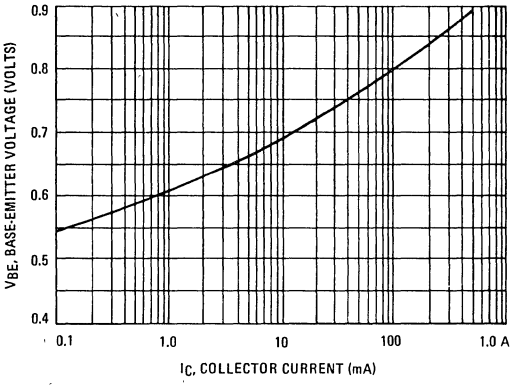


FIGURE 4 – CAPACITANCE versus VOLTAGE

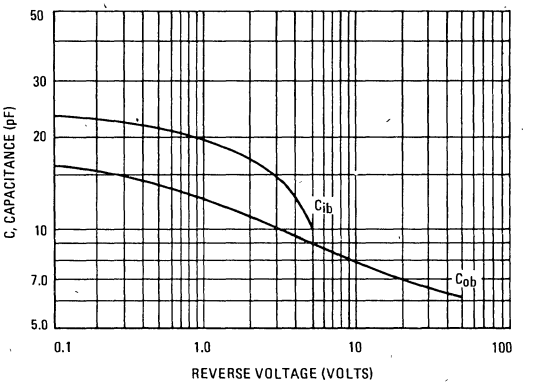


FIGURE 5 – CURRENT-GAIN-BANDWIDTH PRODUCT versus COLLECTOR CURRENT

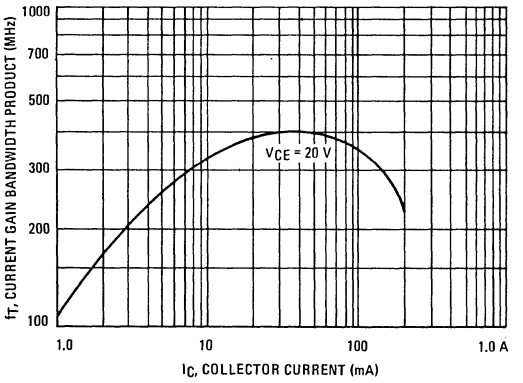
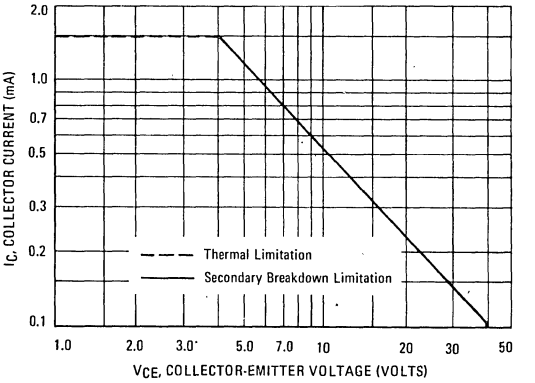


FIGURE 6 – ACTIVE REGION DC SAFE OPERATING AREA



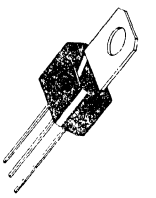
MPS-U03
MPS-U04

NPN SILICON ANNULAR HIGH VOLTAGE AMPLIFIER TRANSISTORS

. . . designed for horizontal drive applications, high-voltage linear amplifiers, and high-voltage transistor regulators.

- High Collector-Emitter Breakdown Voltage — BV_{CEO} = 180 Vdc (Min) @ I_C = 1 mAdc — MPS-U04
- Low Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 200 mAdc
- High Power Dissipation — P_D = 10 W @ T_C = 25°C

NPN SILICON AMPLIFIER TRANSISTORS



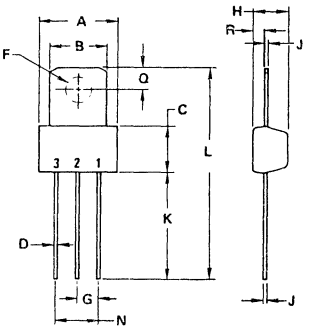
4

MAXIMUM RATINGS

Rating	Symbol	MPS-U03	MPS-U04	Unit
Collector-Emitter Voltage	V_{CEO}	120	180	Vdc
Collector-Base Voltage	V_{CB}	120	180	Vdc
Emitter-Base Voltage	V_{EB}	5		Vdc
Collector Current	I_C	1		Adc
Total Power Dissipation @ T_A = 25°C Derate Above 25°C	P_D	1 8		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		°C
Solder Temperature, 1/16" From Case for 10 Seconds	—	260		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(COLLECTOR CONNECTED TO TAB)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	MPS-U03	BV_{CEO}	120	–	Vdc
	MPS-U04		180	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	MPS-U03	BV_{CBO}	120	–	Vdc
	MPS-U04		180	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	MPS-U03	I_{CBO}	–	0.1	μAdc
(V_{CB} = 150 Vdc, I_E = 0)	MPS-U04		–	0.1	
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc)		h_{FE}	40	–	–
Collector-Emitter Saturation Voltage (I_C = 200 mAdc, I_B = 20 mAdc)		$V_{CE(sat)}$	–	0.5	Vdc
Base-Emitter On Voltage (I_C = 200 mAdc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 20 Vdc, f = 20 MHz)		f_T	35	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	12	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz)		C_{ib}	–	110	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

FIGURE 1 – CURRENT-GAIN – BANDWIDTH PRODUCT

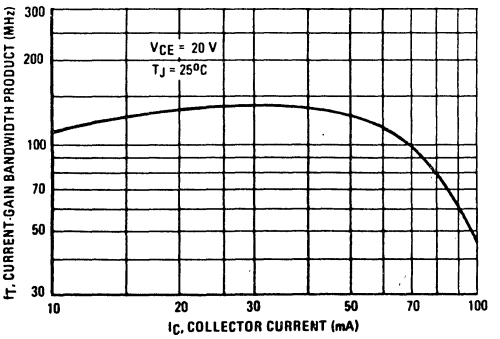
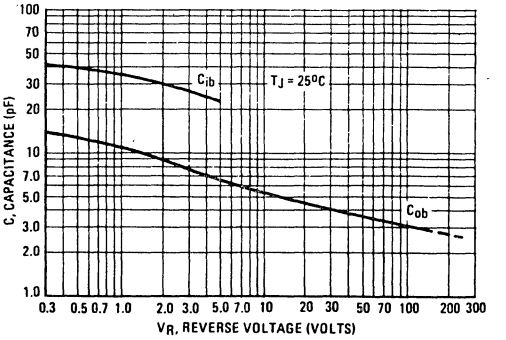


FIGURE 2 – CAPACITANCE



TYPICAL CHARACTERISTICS (Continued)

FIGURE 3 – DC CURRENT GAIN

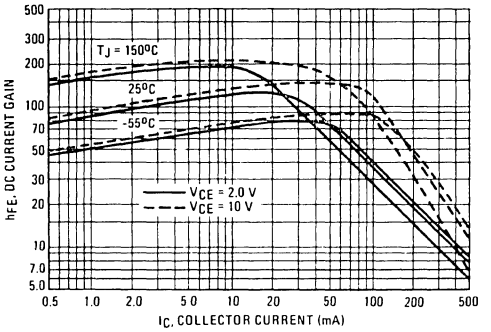


FIGURE 4 – "ON" VOLTAGE

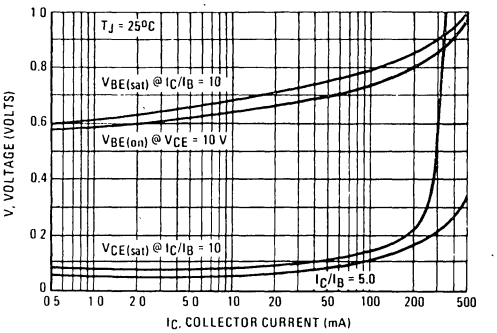


FIGURE 5 – COLLECTOR SATURATION REGION

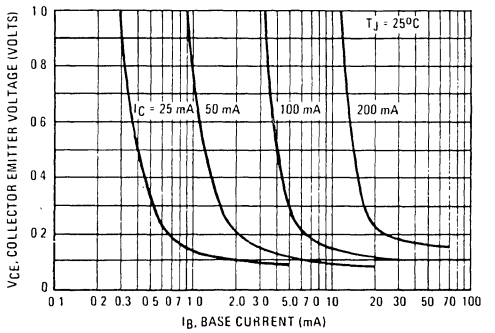


FIGURE 6 – TEMPERATURE COEFFICIENTS

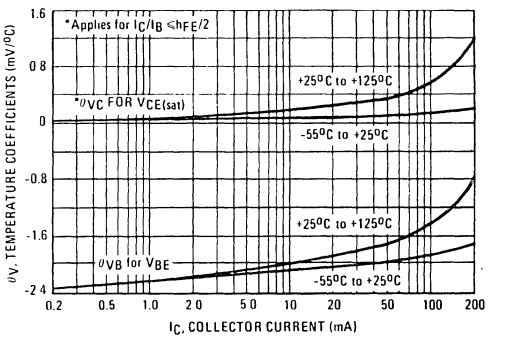


FIGURE 7 – COLLECTOR CHARACTERISTICS

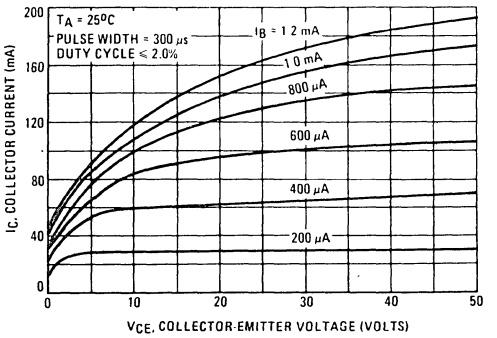
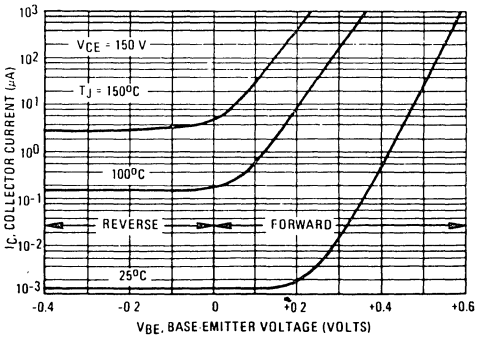


FIGURE 8 – COLLECTOR CUTOFF REGION



TYPICAL CHARACTERISTICS (Continued)

FIGURE 9 – THERMAL RESPONSE

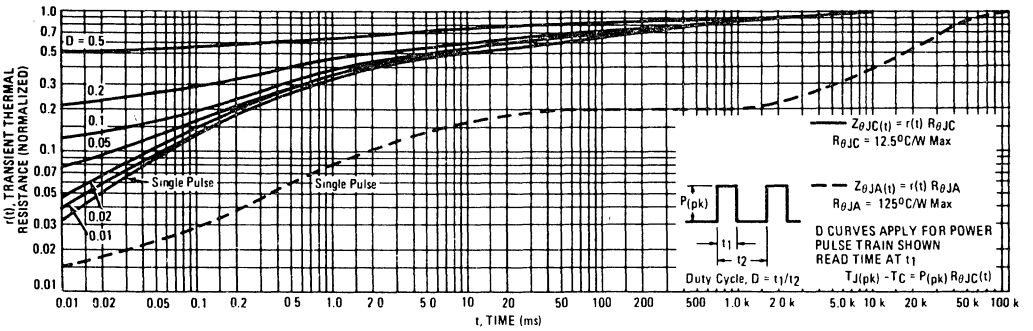
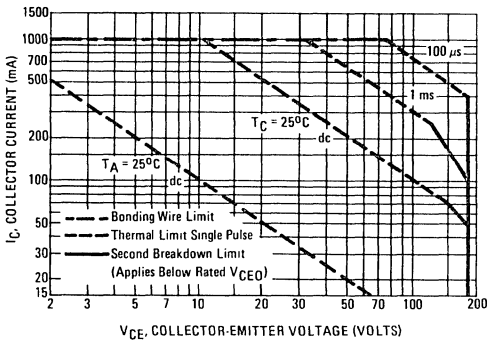


FIGURE 10 – ACTIVE REGION SAFE-OPERATING AREA

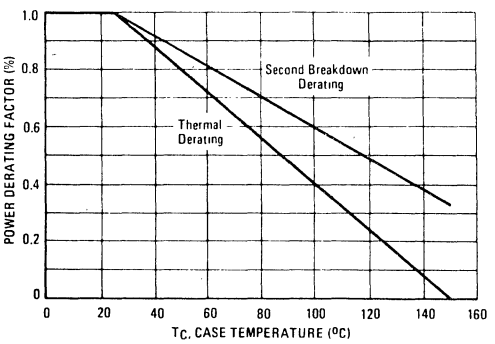


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 – POWER DERATING



MPS-U05 (SILICON)
MPS-U06

NPN SILICON ANNULAR
AMPLIFIER TRANSISTORS

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage –
  BV_{CEO} = 60 Vdc (Min) @ I_C = 1.0 mAdc – MPS-U05
  80 Vdc (Min) @ I_C = 1.0 mAdc – MPS-U06
- High Power Dissipation – P_D = 10 W @ T_C = 25°C
- Complements to PNP MPS-U55 and MPS-U56

NPN SILICON
AMPLIFIER TRANSISTORS

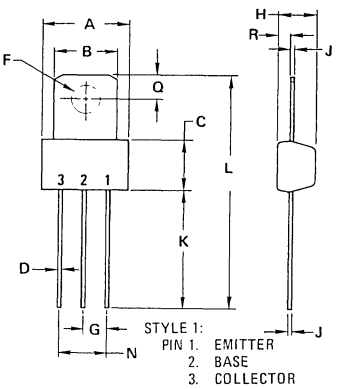
4

MAXIMUM RATINGS

Rating	Symbol	MPS-U05	MPS-U06	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current – Continuous	I_C	2.0		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0		Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	MPS-U05	BV_{CEO}	60	–	–	Vdc
	MPS-U06		80	–	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current		I_{CBO}				nAdc
(V_{CB} = 40 Vdc, I_E = 0)	MPS-U05		–	–	100	
(V_{CB} = 60 Vdc, I_E = 0)	MPS-U06		–	–	100	
ON CHARACTERISTICS						
DC Current Gain (1)		h_{FE}				–
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)			80	125	–	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)			60	100	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			–	55	–	
Collector-Emitter Saturation Voltage(1)		$V_{CE(sat)}$				Vdc
(I_C = 250 mAdc, I_B = 10 mAdc)			–	0.18	0.4	
(I_C = 250 mAdc, I_B = 25 mAdc)			–	0.1	–	
Base-Emitter On Voltage (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	0.74	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain—Bandwidth Product (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	50	150	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	6.0	12	pF

(1)Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

FIGURE 1 – DC CURRENT GAIN

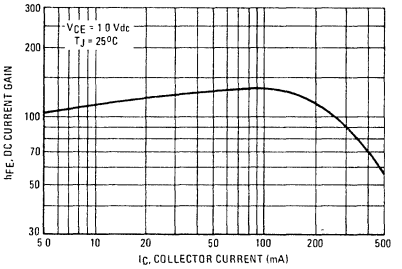


FIGURE 2 – "ON" VOLTAGES

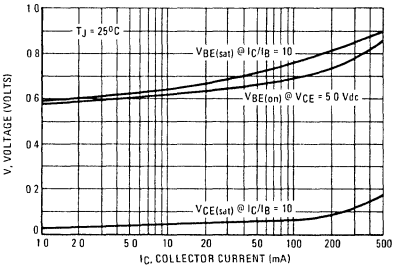


FIGURE 3 – DC SAFE OPERATING AREA

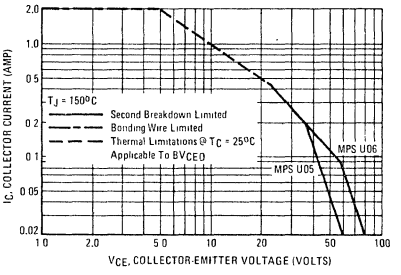
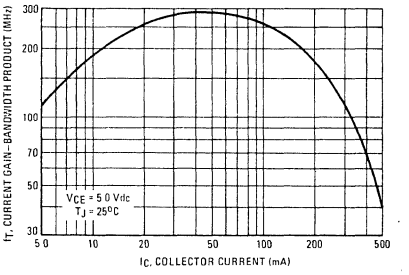


FIGURE 4 – CURRENT-GAIN–BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

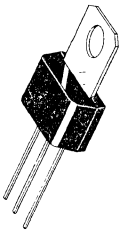
MPS - U07 (SILICON)

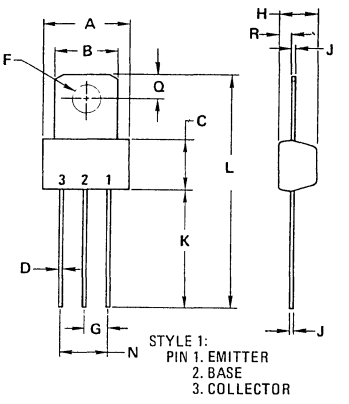
NPN SILICON ANNULAR AMPLIFIER TRANSISTOR

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage — BV_{CEO} = 100 Vdc (Min) @ I_C = 1.0 mAdc
- High Power Dissipation — P_D = 10 W @ T_C = 25°C
- Complement to PNP MPS-U57

NPN SILICON AMPLIFIER TRANSISTOR





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous	I_C	2.0	Adc
Total Power Dissipaton @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipaton @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	100	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	–	–	100	nAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (I_C = 250 mAdc, V_{CE} = 1.0 Vdc) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	 60 30 –	 110 65 33	 – – –	–
Collector-Emitter Saturation Voltage (1) (I_C = 250 mAdc, I_B = 10 mAdc) (I_C = 250 mAdc, I_B = 25 mAdc)	$V_{CE(sat)}$	 – –	 0.18 0.1	 0.4 –	Vdc
Base-Emitter On Voltage (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	–	0.76	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain–Bandwidth Product (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	50	150	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	6.0	12	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 – DC CURRENT GAIN

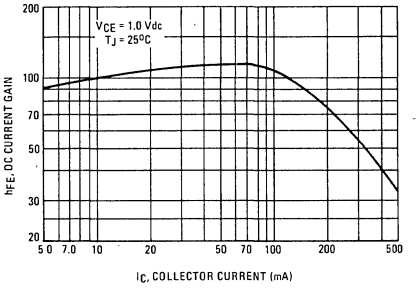


FIGURE 2 – "ON" VOLTAGES

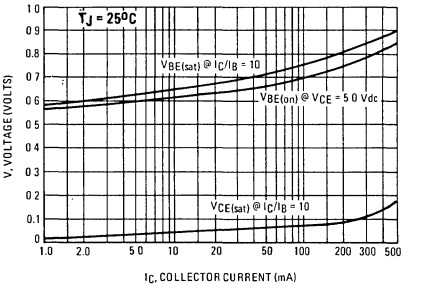


FIGURE 3 – DC SAFE OPERATING AREA

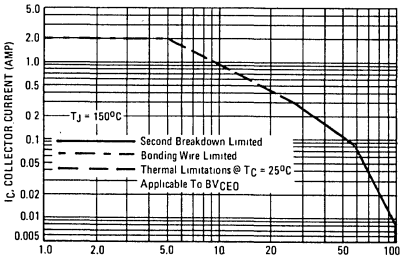
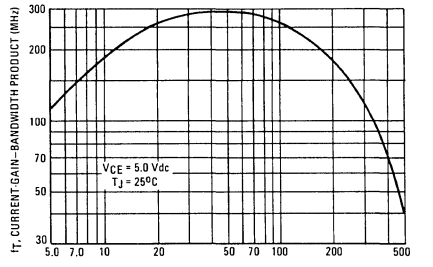


FIGURE 4 – CURRENT-GAIN–BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

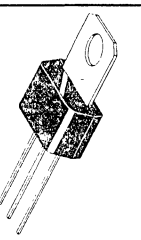
MPS - U10 (SILICON)

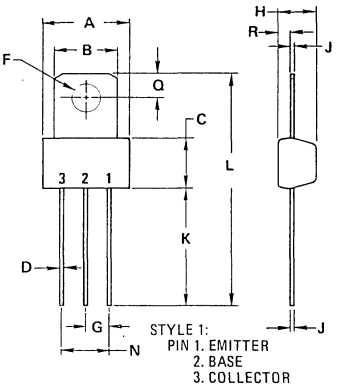
NPN SILICON ANNULAR TRANSISTOR

. . . designed for high-voltage video and luminance output stages in TV receivers.

- High Collector-Emitter Breakdown Voltage – BV_{CEO} = 300 Vdc (Min) @ I_C = 1.0 mAdc
- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 0.75 Vdc (Max) @ I_C = 30 mAdc
- Low Collector-Base Capacitance – C_{cb} = 3.0 pF (Max) @ V_{CB} = 20 Vdc

NPN SILICON
HIGH VOLTAGE
AMPLIFIER
TRANSISTOR





STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Collector-Base Voltage	V_{CB}	300	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Collector Current – Continuous	I_C	500	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

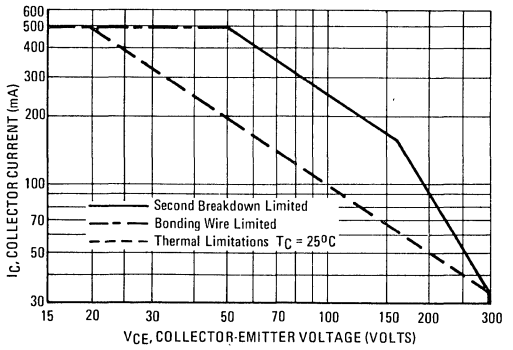
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	300	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	300	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)	BV_{EBO}	6.0	–	Vdc
Collector Cutoff Current (V_{CB} = 200 Vdc, I_E = 0)	I_{CBO}	–	0.2	μAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)	I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			–
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)		25	–	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)		40	–	
(I_C = 30 mAdc, V_{CE} = 10 Vdc)		40	–	
Collector-Emitter Saturation Voltage (I_C = 30 mAdc, I_B = 3.0 mAdc)	$V_{CE(sat)}$	–	0.75	Vdc
Base-Emitter On Voltage (I_C = 30 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	–	0.85	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain–Bandwidth Product (1) (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	45	–	MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	3.0	pF

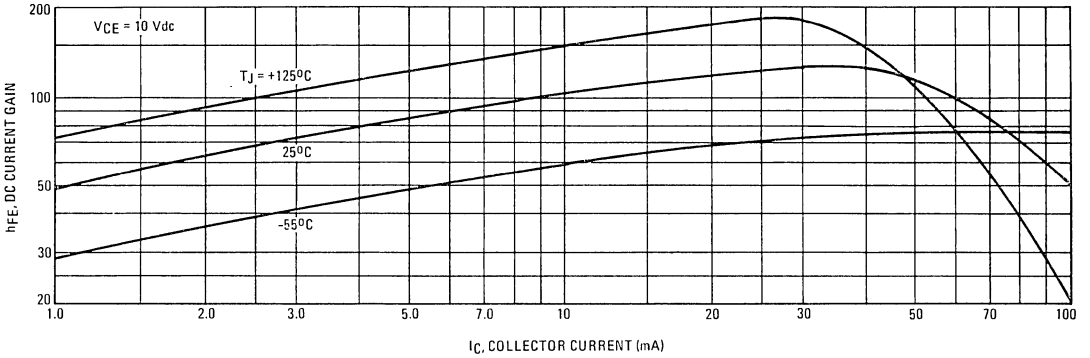
(1)Pulse Test: Pulse Width ≤300 μs, Duty Cycle≤ 2%.

FIGURE 1 – DC SAFE OPERATING AREA



The Safe Operating Area Curves indicate I_C–V_{CE} limits below which the device will not enter second breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power-temperature derating must be observed for both steady state and pulse power conditions.

FIGURE 2 – DC CURRENT GAIN



4

FIGURE 3 – CAPACITANCES

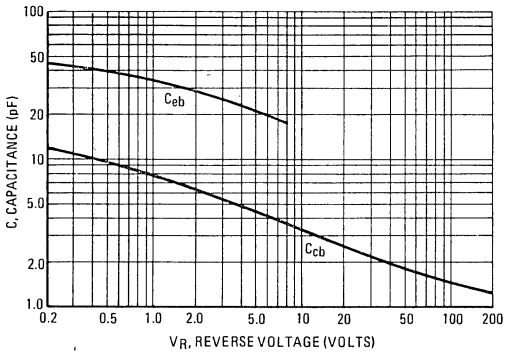


FIGURE 4 – CURRENT-GAIN–BANDWIDTH PRODUCT

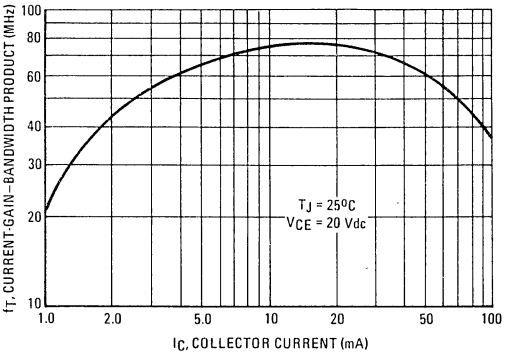
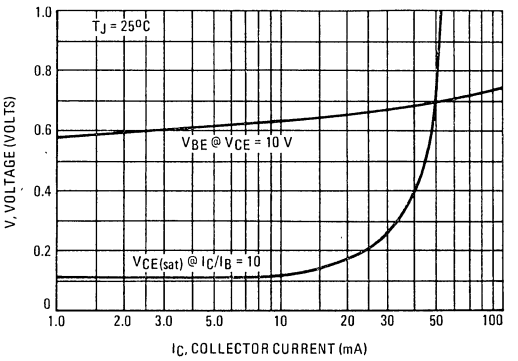


FIGURE 5 – "ON" VOLTAGES



APPLICATIONS INFORMATION

The MPS-U10 is primarily designed for use in the R, G, and B output stages of color television receivers and with a high BV_{CEO}, it can supply the video amplitude requirements of any known system. The low feedback capacitance provides good video bandwidth with modest drive current requirements. Typical drive is from an emitter-follower with a 4.7 k emitter-resistor operated from a 20-Volt supply. It will, therefore, be operable directly from a number of available chroma demodulators. The low output capacitance of this device adds little to the total load capacitance, allowing improved bandwidth for a given collector load resistor. Two typical applications for the MPS-U10 are shown in Figures 6 and 7.

Device dissipation will reach approximately 1.6 Watts under worst-case signal conditions and some heat sinking is required. At an operating ambient temperature of 65°C, a thermal resistance $R_{\theta JA}$ = 150-65/1.6 = 53°C/W will be required. The junction-to-case thermal resistance, $R_{\theta JC}$, of the device is 12.5°C/W, thus a heat dissipator of 40.5°C/W, or lower, will be required. A black anodized 0.020" thick aluminum plate measuring 1" x 2" can be folded into a channel shape and formed with "feet" to snap into a printed circuit panel for support. This will provide the safety factor.

Used as a color difference output, where drive and bandwidth requirements are less severe, the MPS-U10 can be operated with 27 k ohm load resistors (worst-case dissipation would then be only 0.6 Watts). The device can, therefore, be operated as a color-difference output without any heat radiator in ambient temperatures to 150-0.6 (125) = 75°C.

In addition the safe operating area of the MPS-U10 will fill the requirements of the luminance output function with a total equivalent load of 5.0 kilohms. Worst-case dissipation can reach 3 Watts, this requires a total $R_{\theta JA}$ of 150-65/3 = 28.4°C/W. This 28.4°C/W means a heat dissipator of 15.9°C/W, (approximately 2" x 3" aluminum plate) will be required.

4

FIGURE 6 – MPS-U10 AS RGB OUTPUT WITH RGB INPUT

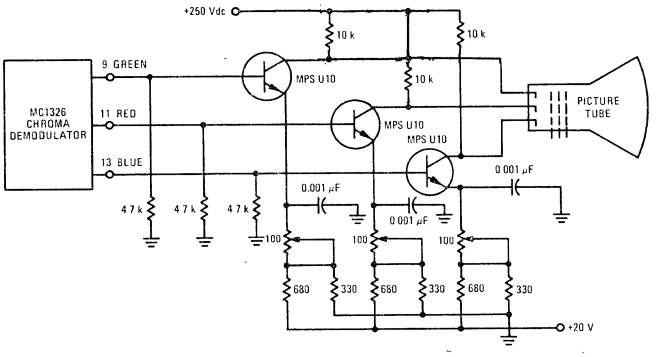
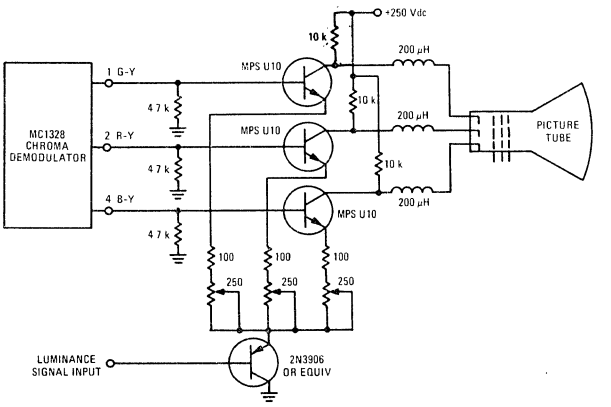


FIGURE 7 – MPS-U10 AS RGB OUTPUT, MATRIXING COLOR DIFFERENCE AND LUMINANCE INPUTS



MPS - U31 (SILICON)

NPN SILICON ANNULAR RF TRANSISTOR

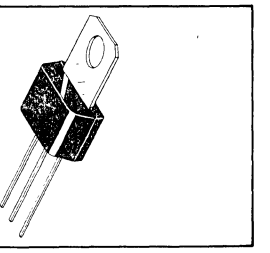
. . . designed for use in Citizen-Band and other high-frequency communications equipment operating to 30 MHz. Higher breakdown voltages allow a high percentage of up-modulation in AM circuits. This device is designed to be used with the MPS8000 driver and the MPS8001 RF oscillator.

- Output Power = 3.5 W (Min) @ V_{CC} = 13.6 Vdc
- Power Gain = 11.5 dB (Min)
- High Collector-Emitter Breakdown Voltage – $BV_{CES} \geq 65$ Vdc
- DC Current Gain – Linear to 500 mAdc

3.5 W – 27 MHz

RF POWER OUTPUT TRANSISTOR

NPN SILICON

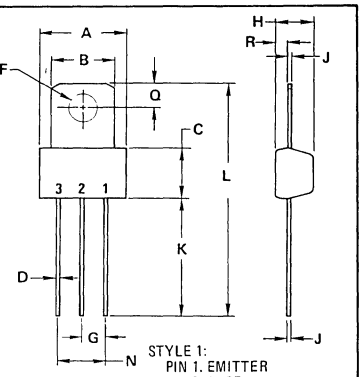


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CES}	65	Vdc
Emitter-Base Voltage	V_{EB}	3.0	Vdc
Collector Current – Continuous	I_C	500	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JA}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 150 mAdc, V_{BE} = 0)	BV_{CES}	65	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 1.0 mAdc, I_C = 0)	BV_{EBO}	3.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0)	I_{CBO}	–	–	0.01	mAdc
ON CHARACTERISTICS					
DC Current Gain (2) (I_C = 100 mAdc, V_{CE} = 10 Vdc)	h_{FE}	10	–	–	–
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	–	–	40	pF
FUNCTIONAL TEST (Figure 1)					
Common-Emitter Amplifier Power Gain (P_{out} = 3.5 W, V_{CC} = 13.6 Vdc, f = 27 MHz)	G_{PE}	11.5	–	–	dB
Output Power (P_{in} = 250 mW, V_{CC} = 13.6 Vdc, f = 27 MHz)	P_{out}	3.5	–	–	Watts
Collector Efficiency (3) (P_{out} = 3.5 W, V_{CC} = 13.6 Vdc, f = 27 MHz)	η	–	70	–	%
Percentage Up-Modulation (4) (f = 27 MHz)	–	–	85	–	%

(1) Pulsed thru a 25 mH Inductor

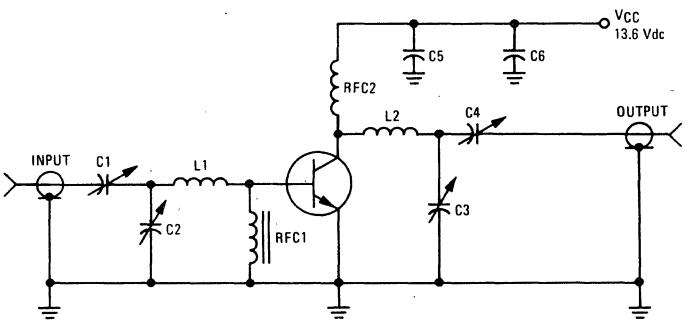
(2) Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

(3) $\eta = \dfrac{R_F\, P_{out}}{(V_{CC})\,(I_C)} \bullet 100$

(4) Percentage Up-Modulation is measured in the test circuit (Figure 1) by setting the Carrier Power (P_c) to 3.5 Watts with V_{CC} = 13.6 Vdc and noting the power input. Then the Peak Envelope Power (PEP) is noted after doubling the original power input to simulate driver modulation (at a 25% duty cycle for thermal considerations) and raising the V_{CC} to 25 Vdc (to simulate the modulating voltage). Percentage Up-Modulation is then determined by the relation:

$$\text{Percentage Up-Modulation} = \left[\left(\frac{PEP}{P_c}\right)^{1/2} - 1\right] \bullet 100$$

FIGURE 1 – 27 MHz TEST CIRCUIT



C1, C2 9.0-180 pF ARCO 463 or Equivalent
C3, C4 5.0-80 pF ARCO 462 or Equivalent
C5 0.02 μF Ceramic Disc
C6 0.1 μF Ceramic Disc
RFC1 4 Turns #30 Enameled Wire Wound on Ferroxcube Bead Type 56-590-65/3B
RFC2 26 Turns #22 Enameled Wire (2 Layers – 13 Turns Each Layer) ¼" Inner Diameter
L1 0.22 μH Molded Choke
L2 0.68 μH Molded Choke

POWER OUTPUT

FIGURE 2 – V_{CC} = 12.5 Vdc

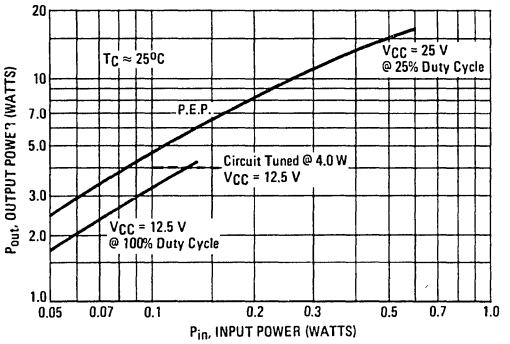


FIGURE 3 – V_{CC} = 13.6 Vdc

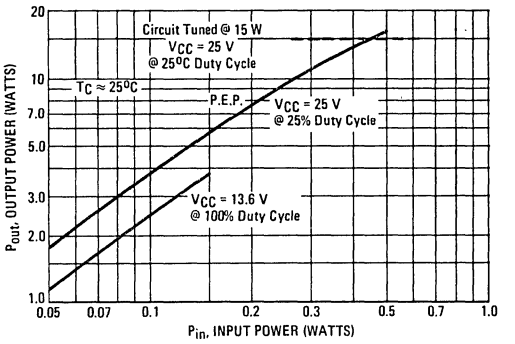


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FIGURE 4 – CURRENT-GAIN – BANDWIDTH PRODUCT

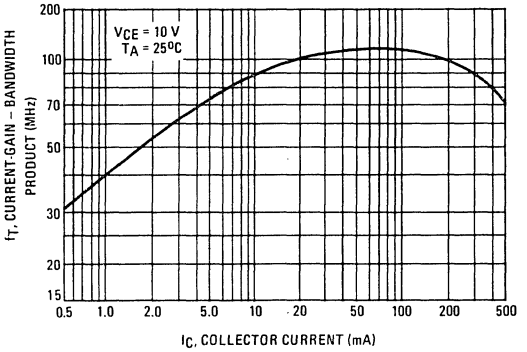


FIGURE 5 – CAPACITANCE

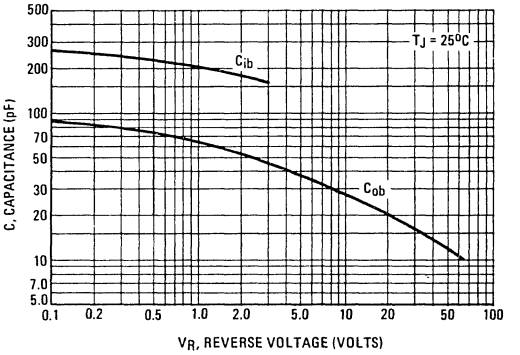


FIGURE 6 – DC CURRENT GAIN

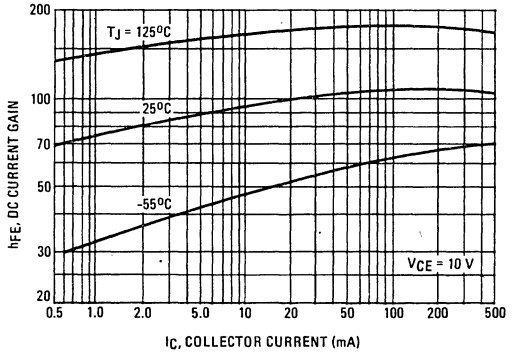


FIGURE 7 – ON VOLTAGES

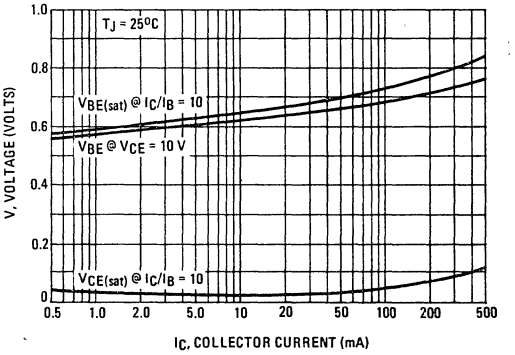
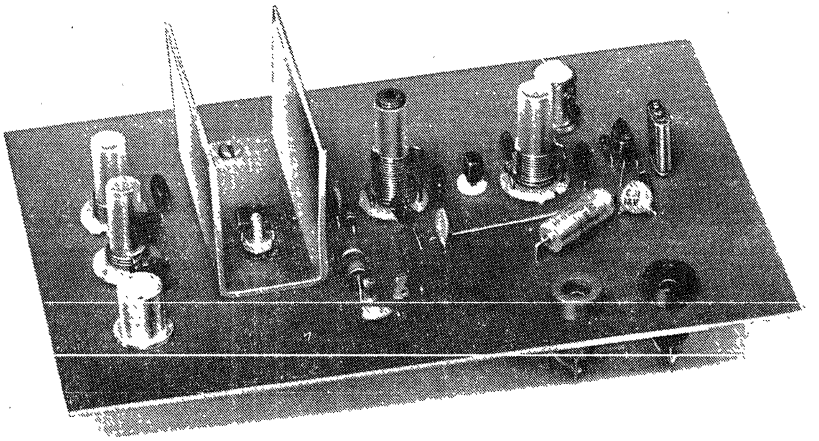
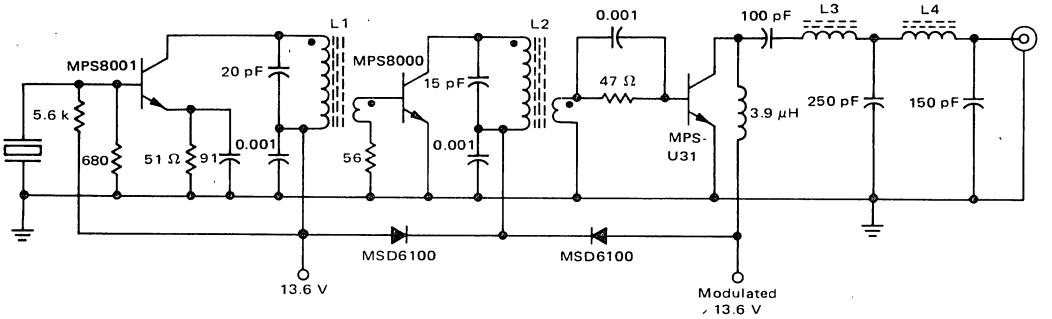


FIGURE 8 – TYPICAL APPLICATION – 27 MHz CITIZEN-BAND TRANSMITTER



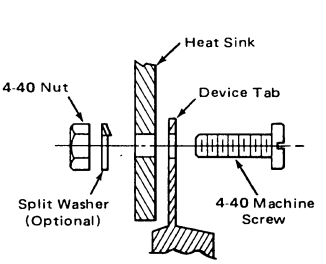


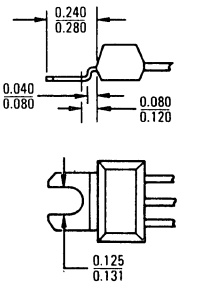
For complete information on this circuit, refer to Motorola Application Note, AN-596.

Case-(Tab)-to-Sink Thermal Resistances ($R_{\theta CS}$) for Common Mounting Methods

Condition	$R_{\theta CS}$ In °C/W	Mounting Screw Torque (in./lbs.)
No Grease	4.25	5
With Dow-340 Thermal Compound	2.1 1.7	2 5
With Dow-340 and 2 mil Mica Washer	4.7 4.3	2 5
With 0.1" Chassis Block and Dow-340	2.4	5
With 0.1" Block, Dow-340 and 2 mil Mica Washer	4.9	5
With 0.062" Block and Dow-340	2.2	5
With 0.062" Block, Dow-340 and 2 mil Mica Washer	4.7	5

LEAD FORM AND MOUNTING INFORMATION FOR UNIWATT PACKAGE





Tab formed for flush mounting order as MPS-U31-1

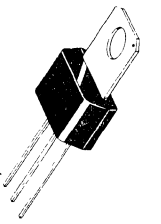
MPS - U45

NPN SILICON DARLINGTON AMPLIFIER TRANSISTOR

. . . designed for amplifier and driver applications.

- High DC Current Gain –
  h_{FE} = 25,000 (Min) @ I_C = 200 mAdc
  15,000 (Min) @ I_C = 500 mAdc
- Collector-Emitter Breakdown Voltage –
  BV_{CES} = 40 Vdc (Min) @ I_C = 100 μAdc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.5 Vdc @ I_C = 1.0 Adc
- Monolithic Construction for High Reliability
- Complement to PNP MPS-U95

NPN SILICON DARLINGTON TRANSISTOR



4

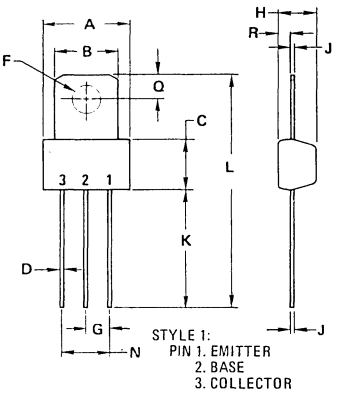
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}(1)	40	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	12	Vdc
Collector Current	I_C	2.0	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

(1) Due to the monolithic construction of this device, breakdown voltages of both transistor elements are identical. BV_{CES} is tested in lieu of BV_{CEO} in order to avoid errors caused by noise pickup. The voltage measured during the BV_{CES} test is the BV_{CEO} of the output transistor.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 μAdc, V_{BE} = 0)	BV_{CES}	40	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	50	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	12	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	100	nAdc
Emitter Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)	I_{EBO}	–	–	100	nAdc
ON CHARACTERISTICS(1)					
DC Current Gain	h_{FE}				–
(I_C = 200 mAdc, V_{CE} = 5.0 Vdc)		25,000	65,000	150,000	
(I_C = 500 mAdc, V_{CE} = 5.0 Vdc)		15,000	35,000	–	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		4,000	12,000	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 2.0 mAdc)	$V_{CE(sat)}$	–	1.2	1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 2.0 mAdc)	$V_{BE(sat)}$	–	1.85	2.0	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	–	1.7	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (1) (I_C = 200 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	$\|h_{fe}\|$	1.0	3.2	–	–
Collector Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	2.5	6.0	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Uniwatt darlington transistors can be used in any number of low power applications, such as relay drivers, motor control and as general purpose amplifiers. As an audio amplifier these devices, when used as a complementary pair, can drive 3.5 watts into a 3.2 ohm speaker using a 14 volt supply with less than one per cent distortion. Because of the high gain the base drive requirement is as low as 1 mA in this application. They are also useful as power drivers for high current application such as voltage regulators.

FIGURE 1 – DC CURRENT GAIN

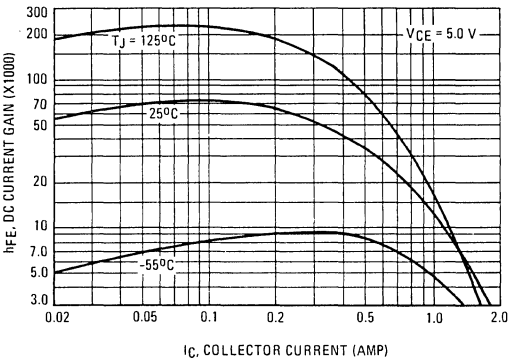


FIGURE 2 – SMALL-SIGNAL CURRENT GAIN

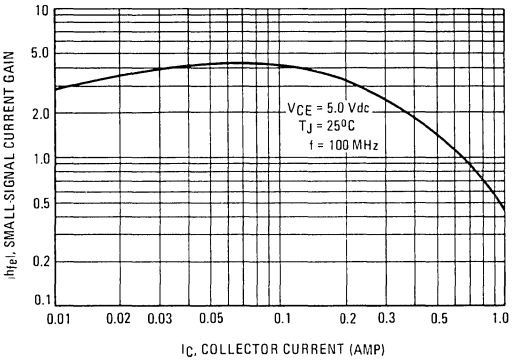


FIGURE 3 – "ON" VOLTAGES

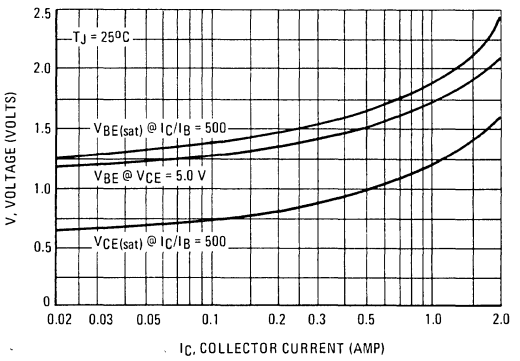


FIGURE 4 – TEMPERATURE COEFFICIENT

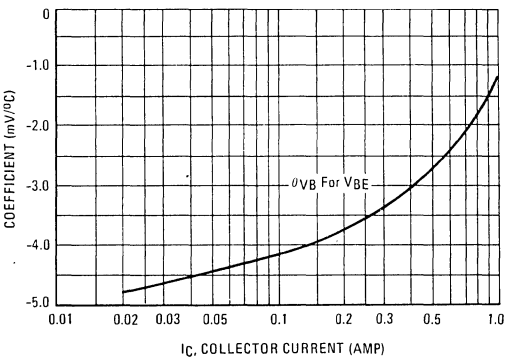
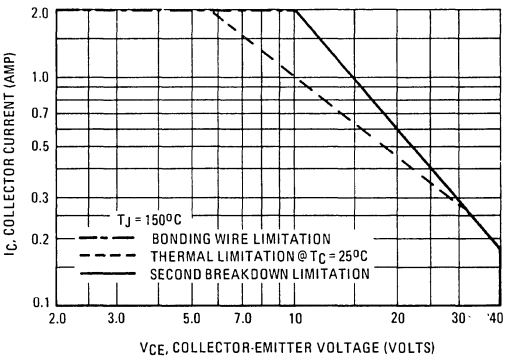


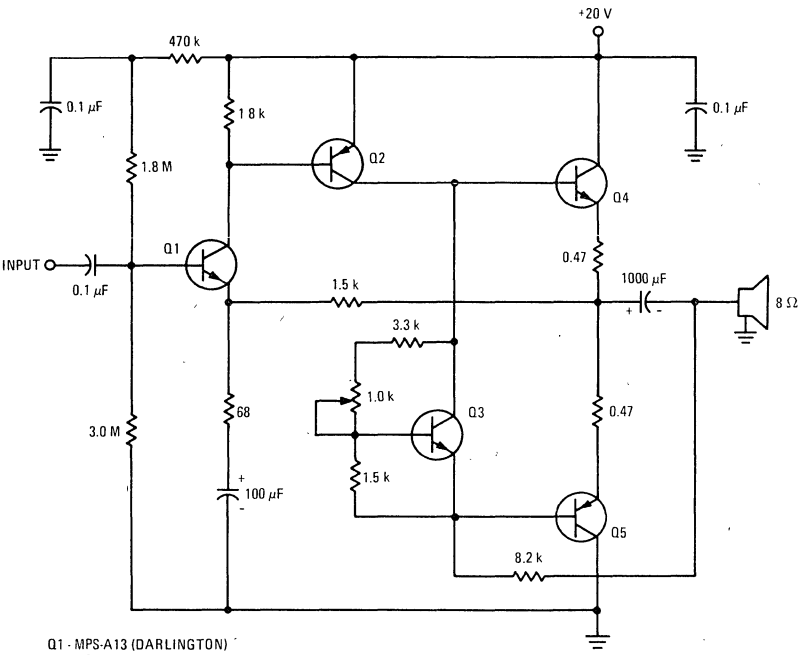
FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

5-WATT AUDIO AMPLIFIER



Q1 - MPS-A13 (DARLINGTON)
Q2 - MPS-A70
Q3 - MPS-A20
Q4 - MPS-U45 } COMPLEMENTARY
Q5 - MPS-U95 } DARLINGTONS

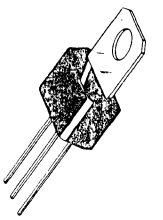
MPS - U51
MPS - U51A

PNP SILICON ANNULAR TRANSISTORS

. . . designed for complementary symmetry audio circuits to 5 Watts output.

- Excellent Current Gain Linearity – 1.0 mAdc to 1.0 Adc
- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 0.7 Vdc (Max) @ I_C = 1.0 Adc
- Complements to NPN MPS-U01 and MPS-U01A
- Uniwatt Package for Excellent Thermal Properties – 1.0 Watt @ T_A = 25°C

PNP SILICON AUDIO TRANSISTORS

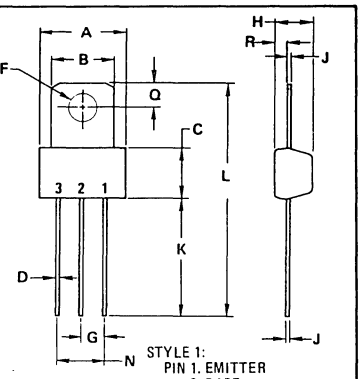


MAXIMUM RATINGS

Rating	Symbol	MPS-U51	MPS-U51A	Unit
Collector-Emitter Voltage	V_{CEO}	30	40	Vdc
Collector-Base Voltage	V_{CB}	40	50	Vdc
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous	I_C	2 0		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0		Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MPS-U51,MPS-U51A

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	MPS-U51	BV_{CEO}	30	–	Vdc
	MPS-U51A		40	–	
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	MPS-U51	BV_{CBO}	40	–	Vdc
	MPS-U51A		50	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	5.0	–	Vdc
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 30 Vdc, I_E = 0)	MPS-U51		–	0.1	
(V_{CB} = 40 Vdc, I_E = 0)	MPS-U51A		–	0.1	
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)		I_{EBO}	–	0.1	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			–
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)			55	–	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)			60	–	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)			50	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	–	0.7	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	–	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain–Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)		f_T	50	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	30	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 – DC CURRENT GAIN

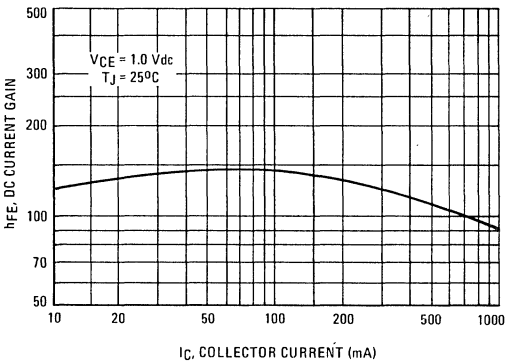


FIGURE 2 – "ON" VOLTAGES

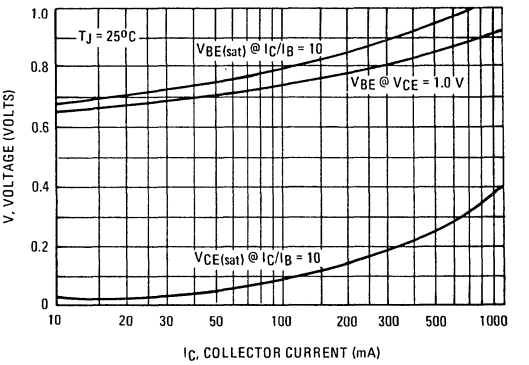
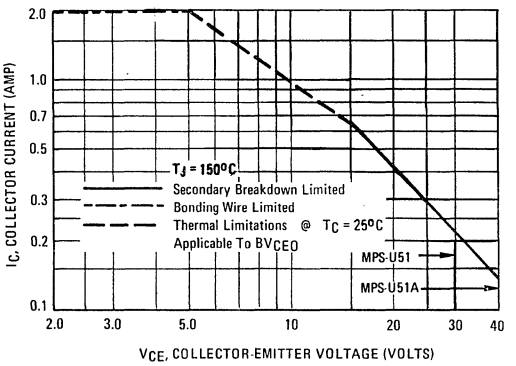


FIGURE 3 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

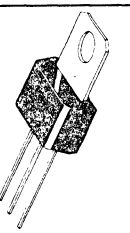
MPS - U52 (SILICON)

PNP SILICON ANNULAR TRANSISTOR

. . . designed for general-purpose amplifier and driver applications.

- Complement to NPN MPS-U02

PNP SILICON AMPLIFIER TRANSISTOR



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	60	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	1.5	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg} (1)	-55 to +150	°C

THERMAL CHARACTERISTICS

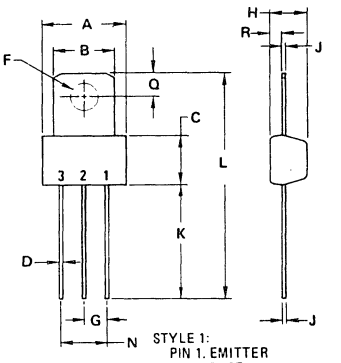
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	40	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	60	-	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	I_{CBO}	-	100	nAdc
ON CHARACTERISTICS (2)				
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 150 mAdc, V_{CE} = 10 Vdc) (I_C = 500 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 50 50 30	 - 300 -	-
Collector-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{CE(sat)}$	-	0.4	Vdc
Base-Emitter Saturation Voltage (I_C = 150 mAdc, I_B = 15 mAdc)	$V_{BE(sat)}$	-	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (2) (I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	100	-	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	-	24	pF

(1) $R_{\theta JA}$ is measured with device soldered into a typical printed circuit board

(2) Pulse Test: Pulse Width≤300 μs, Duty Cycle≤2.0%



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

FIGURE 1 – DC CURRENT GAIN

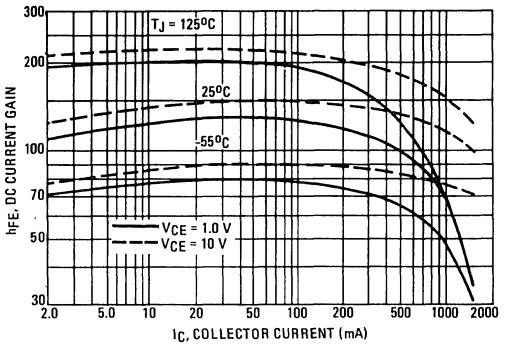


FIGURE 2 – "ON" VOLTAGES

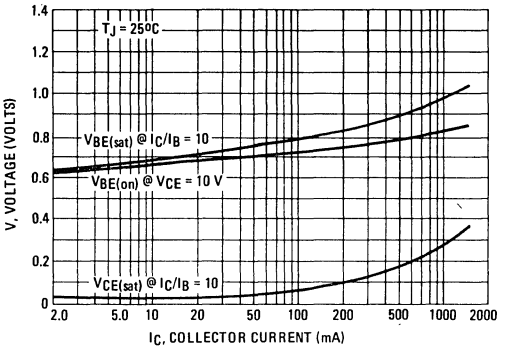


FIGURE 3 – COLLECTOR SATURATION REGION

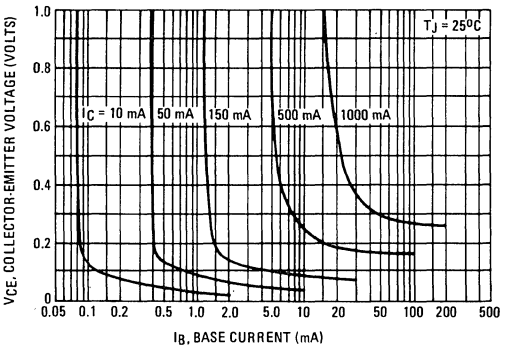


FIGURE 4 – DC SAFE OPERATING AREA

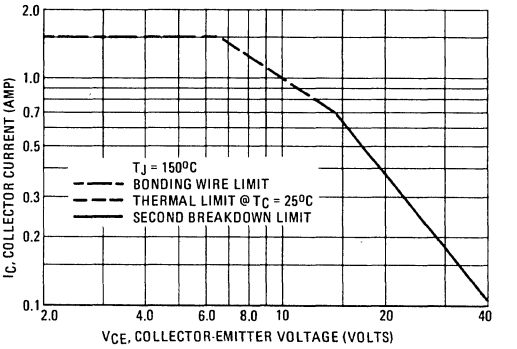


FIGURE 5 – CURRENT-GAIN BANDWIDTH PRODUCT

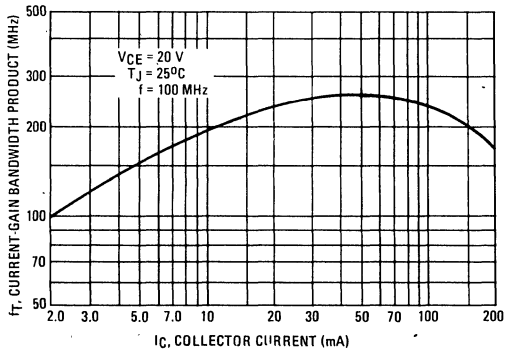
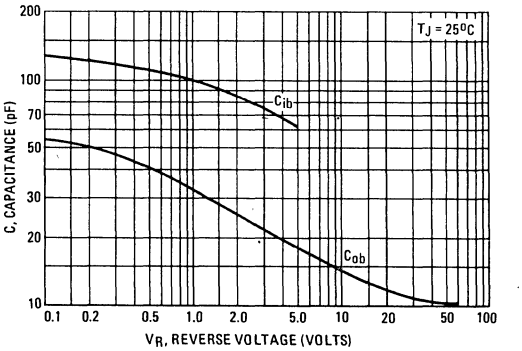


FIGURE 6 – CAPACITANCE



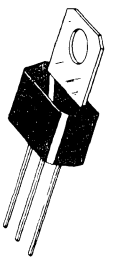
MPS - U55 (SILICON)
MPS - U56

PNP SILICON ANNULAR AMPLIFIER TRANSISTORS

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage –
  BV_{CEO} = 60 Vdc (Min) @ I_C = 1.0 mAdc – MPS-U55
  80 Vdc (Min) @ I_C = 1.0 mAdc – MPS-U56
- High Power Dissipation – P_D = 10 W @ T_C = 25°C
- Complements to NPN MPS-U05 and MPS-U06

PNP SILICON AMPLIFIER TRANSISTORS

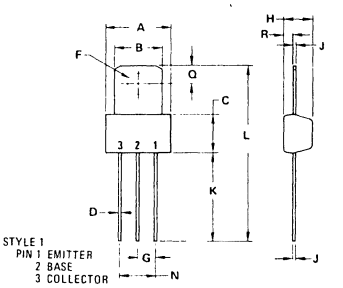


MAXIMUM RATINGS

Rating	Symbol	MPS-U55	MPS-U56	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	Vdc
Collector-Base Voltage	V_{CB}	60	80	Vdc
Emitter-Base Voltage	V_{EB}	4.0		Vdc
Collector Current – Continuous	I_C	2.0		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0		Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

Collector Connected to Tab
CASE 152-02

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_B = 0)	MPS-U55	BV_{CEO}	60	–	–	Vdc
	MPS-U56		80	–	–	
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current		I_{CBO}				nAdc
(V_{CB} = 40 Vdc, I_E = 0)	MPS-U55		–	–	100	
(V_{CB} = 60 Vdc, I_E = 0)	MPS-U56		–	–	100	
ON CHARACTERISTICS						
DC Current Gain (1)		h_{FE}				–
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)			80	160	–	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)			50	130	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			–	80	–	
Collector-Emitter Saturation Voltage(1)		$V_{CE(sat)}$				Vdc
(I_C = 250 mAdc, I_B = 10 mAdc)			–	0.22	0.5	
(I_C = 250 mAdc, I_B = 25 mAdc)			–	0.15	–	
Base-Emitter On Voltage (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	–	0.78	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain–Bandwidth Product (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	50	100	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	–	10	15	pF

(1)Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

FIGURE 1 – DC CURRENT GAIN

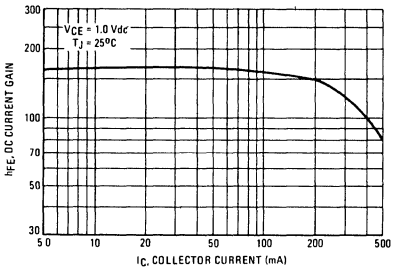


FIGURE 2 – "ON" VOLTAGES

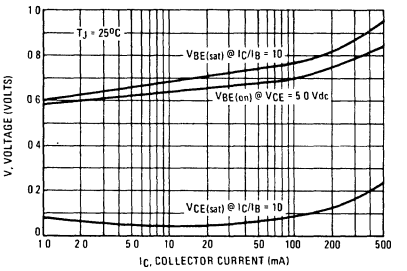


FIGURE 3 – ACTIVE-REGION SAFE OPERATING AREA

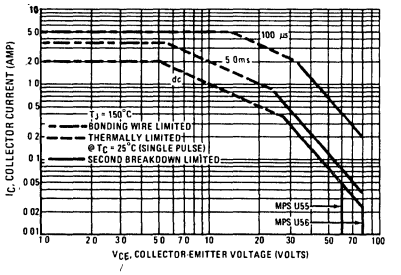
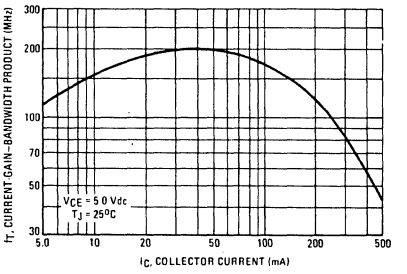


FIGURE 4 – CURRENT-GAIN–BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

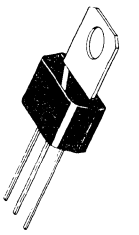
MPS - U57 (SILICON)

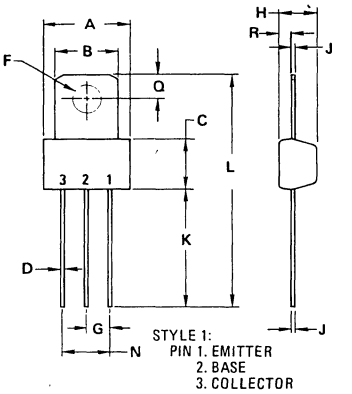
PNP SILICON ANNULAR
AMPLIFIER TRANSISTOR

. . . designed for general-purpose, high-voltage amplifier and driver applications.

- High Collector-Emitter Breakdown Voltage — BV_{CEO} = 100 Vdc (Min) @ I_C = 1.0 mAdc
- High Power Dissipation — P_D = 10 W @ T_C = 25°C
- Complement to NPN MPS-U07

AMPLIFIER TRANSISTOR
PNP SILICON





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous	I_C	2.0	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (1) (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	100	–	–	Vdc
Emitter-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{EBO}	4.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	I_{CBO}	–	–	100	nAdc
ON CHARACTERISTICS (1)					
DC Current Gain	h_{FE}				–
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)		60	140	–	
(I_C = 250 mAdc, V_{CE} = 1.0 Vdc)		30	65	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		–	30	–	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 250 mAdc, I_B = 10 mAdc)		–	0.24	0.5	
(I_C = 250 mAdc, I_B = 25 mAdc)		–	0.15	–	
Base-Emitter On Voltage (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	–	0.78	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain–Bandwidth Product (1) (I_C = 250 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	50	100	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	10	15	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

4

FIGURE 1 – DC CURRENT GAIN

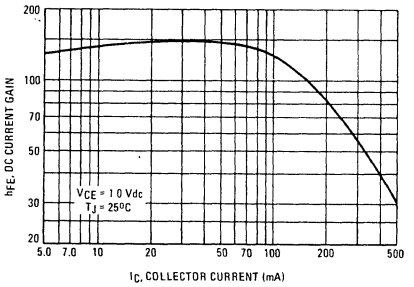


FIGURE 2 – "ON" VOLTAGES

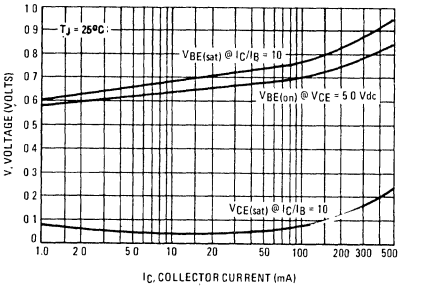


FIGURE 3 – DC SAFE OPERATING AREA

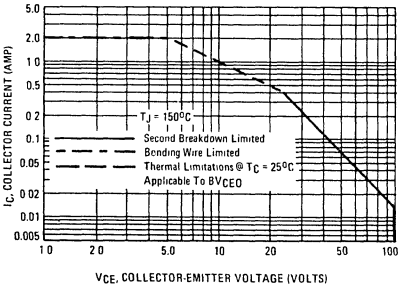
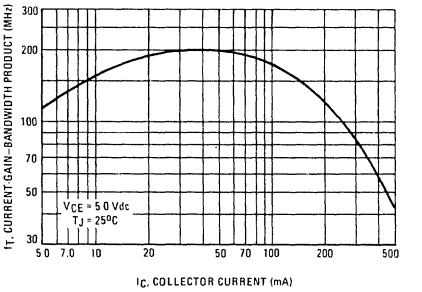


FIGURE 4 – CURRENT-GAIN–BANDWIDTH PRODUCT



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

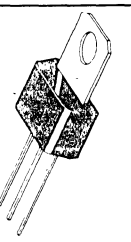
MPS - U60 (SILICON)

PNP SILICON ANNULAR TRANSISTOR

. . . designed for general-purpose applications requiring high breakdown voltages, low saturation voltages and low capacitance.

- Complement to NPN Type MPS-U10

PNP SILICON HIGH VOLTAGE TRANSISTOR



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	300	Vdc
Collector-Base Voltage	V_{CB}	300	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
Total Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	P_D	1.0 8.0	Watt $mW/^oC$
Total Power Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	10 80	Watts $mW/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	^oC

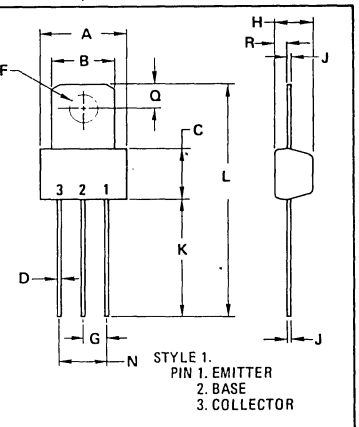
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	12.5	$^oC/W$
Thermal Resistance, Junction to Ambient	$R\theta_{JA}$	125	$^oC/W$

ELECTRICAL CHARACTERISTICS ($T_A = 25^oC$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector Emitter Breakdown Voltage(1) (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	300	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	300	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	5.0		Vdc
Collector Cutoff Current (V_{CB} = 200 Vdc, I_E = 0)	I_{CBO}		0.2	μAdc
Emitter Cutoff Current (V_{BE} = 3.0 Vdc, I_C = 0)	I_{EBO}		0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain (2) (I_C = 1.0 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 30 mAdc, V_{CE} = 10 Vdc)	h_{FE}	25 30 30		
Collector-Emitter Saturation Voltage (I_C = 20 mAdc, I_B = 2.0 mAdc)	$V_{CE(sat)}$		0.75	Vdc
Base-Emitter Saturation Voltage (I_C = 20 mAdc, I_B = 2.0 mAdc)	$V_{BE(sat)}$		0.9	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain—Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	60		MHz
Collector-Base Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	8.0	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

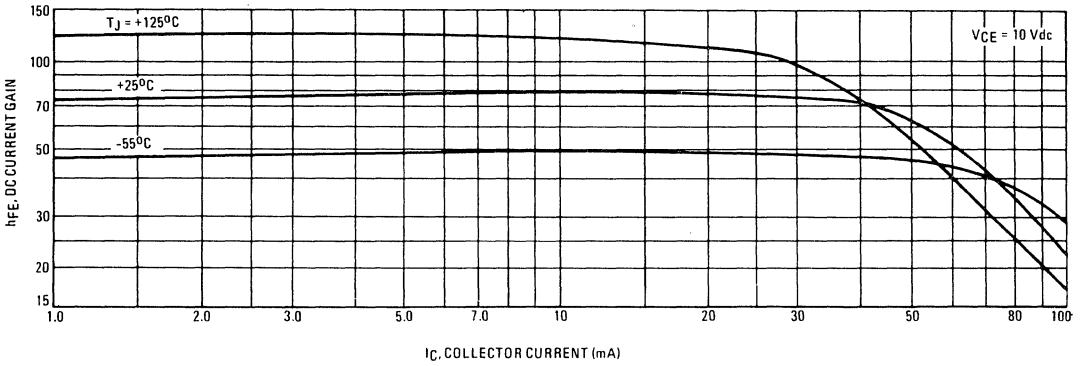


STYLE 1.
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

FIGURE 1 – DC CURRENT GAIN



4

FIGURE 2 – CAPACITANCES

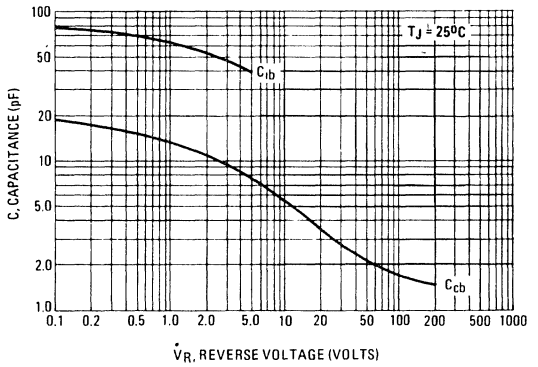


FIGURE 3 – CURRENT-GAIN–BANDWIDTH PRODUCT

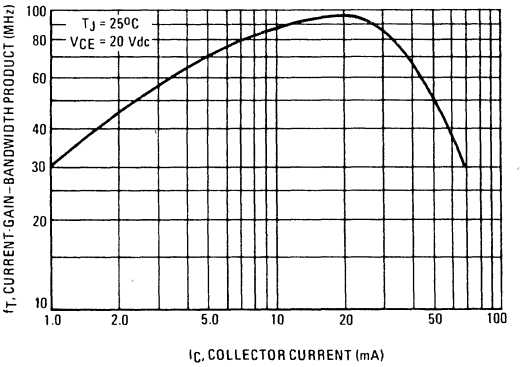


FIGURE 4 – "ON" VOLTAGES

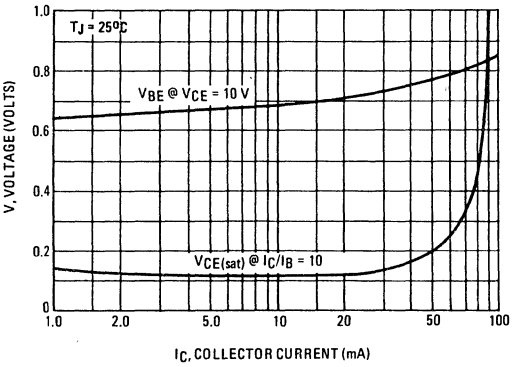
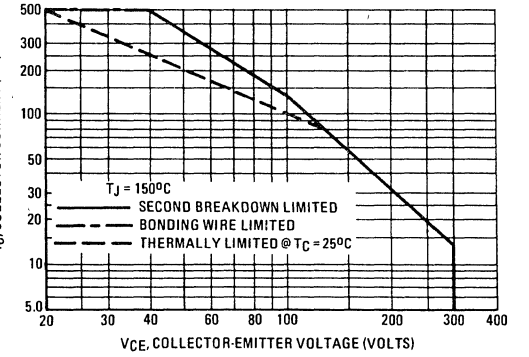


FIGURE 5 – DC SAFE OPERATING AREA



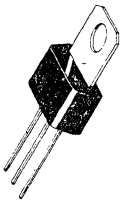
MPS - U95 (SILICON)

PNP SILICON DARLINGTON AMPLIFIER TRANSISTOR

. . . designed for amplifier and driver applications.

- High DC Current Gain –
  h_{FE} = 25,000 (Min) @ I_C = 200 mAdc
  15,000 (Min) @ I_C = 500 mAdc
- Collector-Emitter Breakdown Voltage –
  BV_{CES} = 40 Vdc (Min) @ I_C = 100 μAdc
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.5 Vdc @ I_C = 1.0 Adc
- Monolithic Construction for High Reliability
- Complement to NPN MPS-U45

PNP SILICON DARLINGTON TRANSISTOR



4

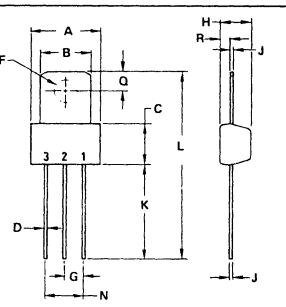
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}(1)	40	Vdc
Collector-Emitter Voltage	V_{CES}	40	Vdc
Collector-Base Voltage	V_{CB}	50	Vdc
Emitter-Base Voltage	V_{EB}	12	Vdc
Collector Current -Continuous	I_C	2.0	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	10 80	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	12.5	°C/W

(1) Due to the monolithic construction of this device, breakdown voltages of both transistor elements are identical. BV_{CES} is tested in lieu of BV_{CEO} in order to avoid errors caused by noise pickup. The voltage measured during the BV_{CES} test is the BV_{CEO} of the output transistor.



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	12.07	12.70	0.475	0.500
L	25.02	25.53	0.985	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (I_C = 100 μAdc, V_{BE} = 0)	BV_{CES}	40	–	–	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	BV_{CBO}	50	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	BV_{EBO}	10	–	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	–	100	nAdc
Emitter Cutoff Current (V_{EB} = 8.0 Vdc, I_C = 0)	I_{EBO}	–	–	100	nAdc
ON CHARACTERISTICS(1)					
DC Current Gain	h_{FE}				–
(I_C = 200 mAdc, V_{CE} = 5.0 Vdc)		25,000	65,000	150,000	
(I_C = 500 mAdc, V_{CE} = 5.0 Vdc)		15,000	35,000	–	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)		4,000	12,000	–	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 2.0 mAdc)	$V_{CE(sat)}$	–	1.2	1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 2.0 mAdc)	$V_{BE(sat)}$	–	1.85	2.0	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	–	1.7	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (1) (I_C = 200 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	$\|h_{fe}\|$	0.5	3.2	–	–
Collector Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	2.5	12	pF

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Uniwatt darlington transistors can be used in any number of low power applications, such as relay drivers, motor control and as general purpose amplifiers. As an audio amplifier these devices, when used as a complementary pair, can drive 3.5 watts into a 3.2 ohm speaker using a 14 volt supply with less than one per cent distortion. Because of the high gain the base drive requirement is as low as 1 mA in this application. They are also usefui as power drivers for high current application such as voltage regulators.

FIGURE 1 – DC CURRENT GAIN

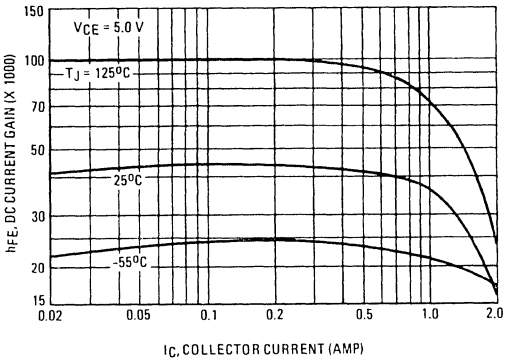


FIGURE 2 – SMALL-SIGNAL CURRENT GAIN

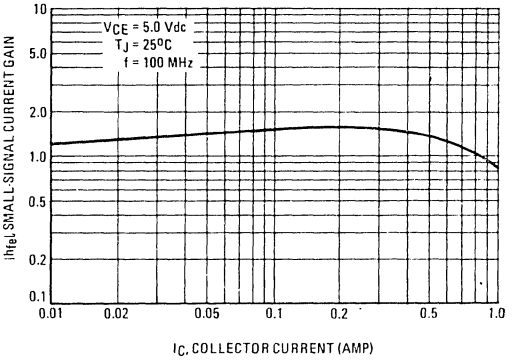


FIGURE 3 – "ON" VOLTAGES

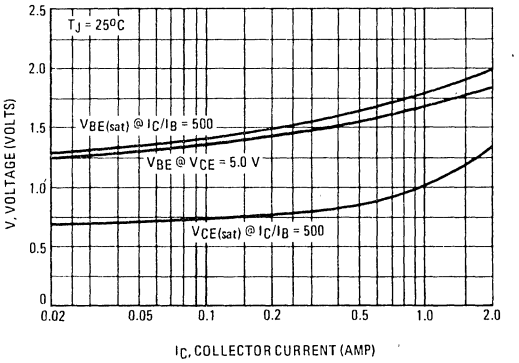


FIGURE 4 – TEMPERATURE COEFFICIENT

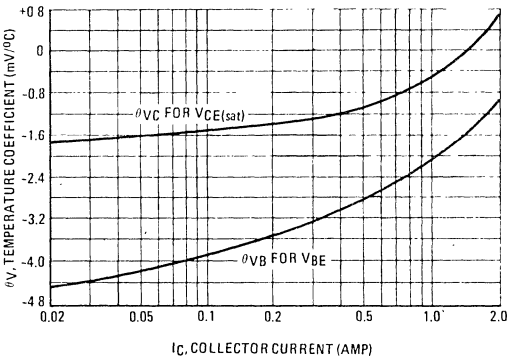
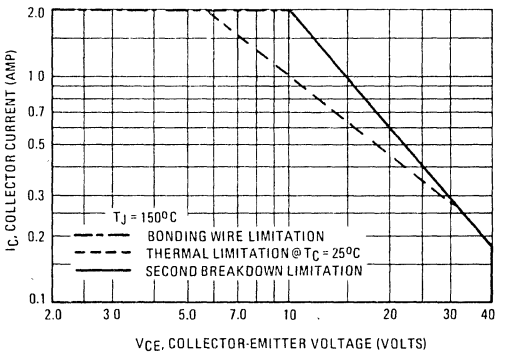


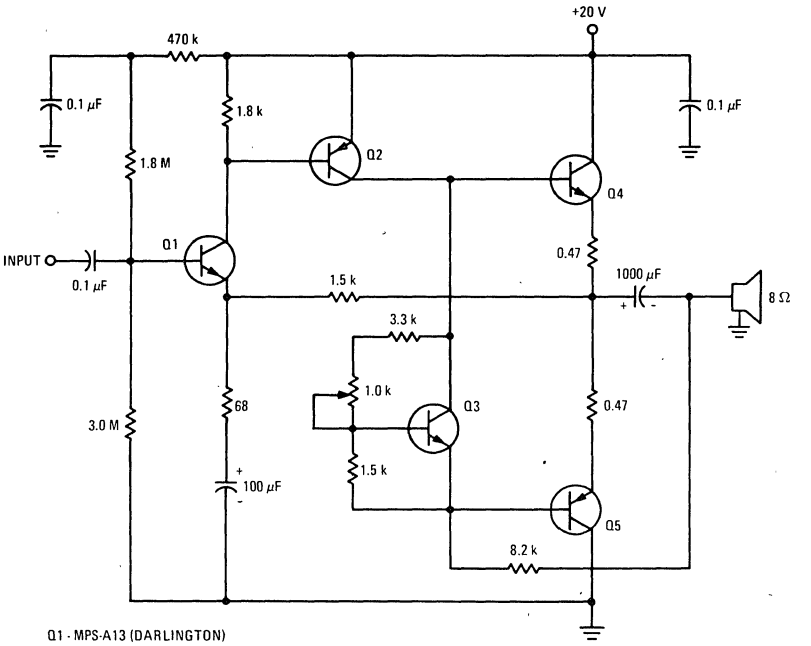
FIGURE 5 – DC SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

5-WATT AUDIO AMPLIFIER



Q1 - MPS-A13 (DARLINGTON)
Q2 - MPS-A70
Q3 - MPS-A20
Q4 - MPS-U45 } COMPLEMENTARY
Q5 - MPS-U95 } DARLINGTONS

NPN PNP

TIP29 TIP30
TIP29A TIP30A
TIP29B TIP30B
TIP29C TIP30C

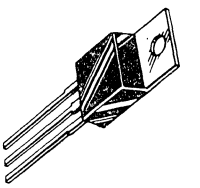
COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications. Compact TO-220 AB package. TO-66 leadform also available.

1 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

40-60-80-100 VOLTS
30 WATTS



4

MAXIMUM RATINGS

Rating	Symbol	TIP29 TIP30	TIP29A TIP30A	TIP29B TIP30B	TIP29C TIP30C	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current – Continuous / Peak	I_C	1.0 / 3.0				Adc
Base Current	I_B	0.4				Adc
Total Power Dissipation @ T_C = 25°C / Derate above 25°C	P_D	30 / 0.24				Watts / W/°C
Total Power Dissipation @ T_A = 25°C / Derate above 25°C	P_D	2.0 / 0.016				Watts / W/°C
Unclamped Inductive Load Energy (See Note 3)	E	32				mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150				°C

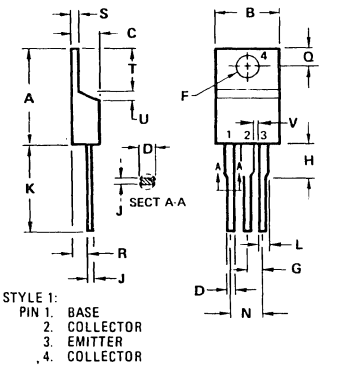
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.167	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP29, TIP30	$V_{CEO(sus)}$	40	–	Vdc
	TIP29A, TIP30A		60	–	
	TIP29B, TIP30B		80	–	
	TIP29C, TIP30C		100	–	
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	TIP29, TIP29A, TIP30, TIP30A	I_{CEO}	–	0.3	mAdc
(V_{CE} = 60 Vdc, I_B = 0)	TIP29B, TIP29C, TIP30B, TIP30C		–	0.3	
Collector Cutoff Current		I_{CES}			μAdc
(V_{CE} = 40 Vdc, V_{EB} = 0)	TIP29, TIP30		–	200	
(V_{CE} = 60 Vdc, V_{EB} = 0)	TIP29A, TIP30A		–	200	
(V_{CE} = 80 Vdc, V_{EB} = 0)	TIP29B, TIP30B		–	200	
(V_{CE} = 100 Vdc, V_{EB} = 0)	TIP29C, TIP30C		–	200	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.2 Adc, V_{CE} = 4.0 Vdc)			40	–	
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			15	75	
Collector-Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 125 mAdc)		$V_{CE(sat)}$	–	0.7	Vdc
Base-Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.3	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2) (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3.0	–	MHz
Small-Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		h_{fe}	20	–	–

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \cdot f_{test}$
(3) This rating based on testing with L_C = 20 mH, R_{BE} = 100 Ω, V_{CC} = 10 V, I_C = 1.8 A, P.R.F. = 10 Hz.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02
TO-220AB

FIGURE 1 – DC CURRENT GAIN

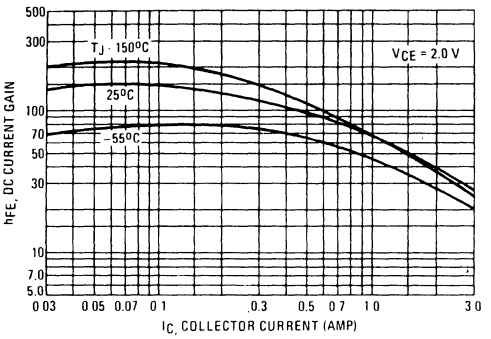


FIGURE 2 – TURN-OFF TIME

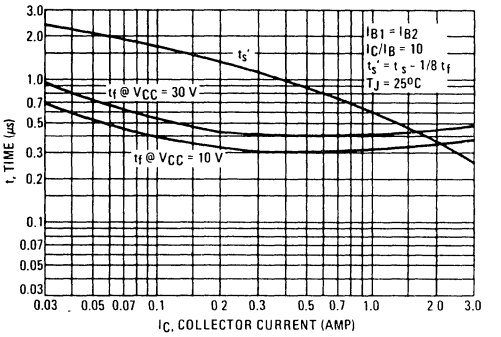
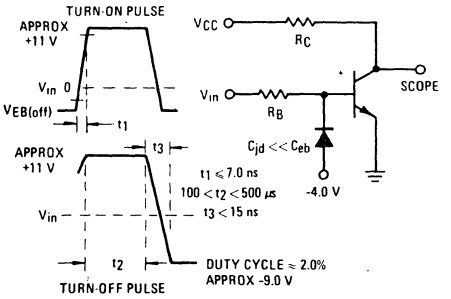


FIGURE 3 – SWITCHING TIME EQUIVALENT CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS.

FIGURE 4 – TURN-ON TIME

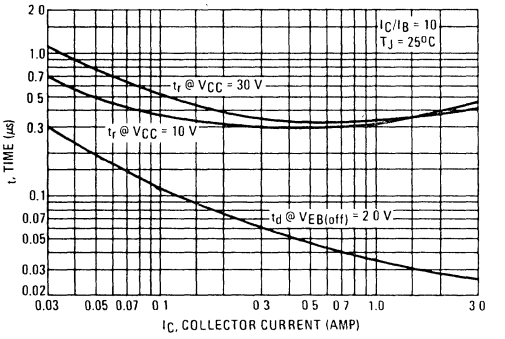
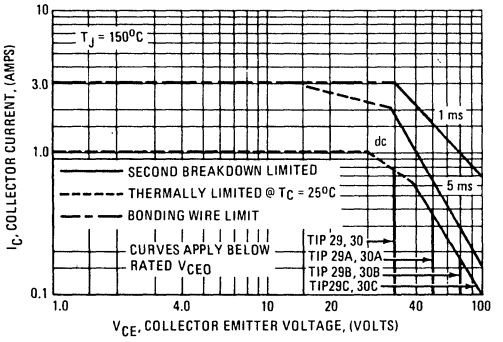


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN PNP

TIP31 TIP32
TIP31A TIP32A
TIP31B TIP32B
TIP31C TIP32C

COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

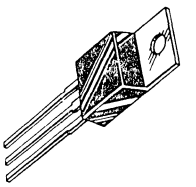
. . . designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 3.0 Adc
- Collector-Emitter Sustaining Voltage –
  $V_{CEO(sus)}$ = 40 Vdc (Min) – TIP31, TIP 32
  = 60 Vdc (Min) – TIP31A, TIP32A
  = 80 Vdc (Min) – TIP31B, TIP32B
  = 100 Vdc (Min) – TIP31C, TIP32C
- High Current Gain – Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO-220 AB Package
- TO-66 Leadform Also Available

3 AMPERE

POWER TRANSISTORS COMPLEMENTARY SILICON

40-60-80-100 VOLTS
40 WATTS



4

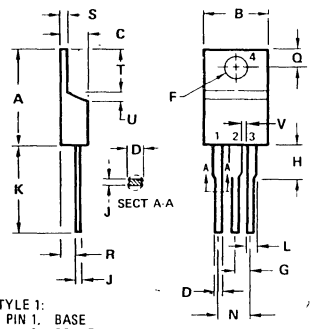
*MAXIMUM RATINGS

Rating	Symbol	TIP31 TIP32	TIP31A TIP32A	TIP31B TIP32B	TIP31C TIP32C	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current - Continuous Peak	I_C	3.0 5.0				Adc
Base Current	I_B	1.0				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 40 0.32				 Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	 2.0 0.016				 Watts W/°C
Unclamped Inductive Load Energy (1)	E	32				mJ
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) I_C = 1.8 A, L = 20 mH, P.R.F. = 10 Hz, V_{CC} = 10 V, R_{BE} = 100 Ω.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
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H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP31, TIP32	$V_{CEO(sus)}$	40	–	Vdc
	TIP31A, TIP32A		60	–	
	TIP31B, TIP32B		80	–	
	TIP31C, TIP32C		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP31, TIP31A, TIP32, TIP32A		–	0.3	
(V_{CE} = 60 Vdc, I_B = 0)	TIP31B, TIP31C, TIP32B, TIP32C		–	0.3	
Collector Cutoff Current		I_{CES}			μAdc
(V_{CE} = 40 Vdc, V_{EB} = 0)	TIP31, TIP32		–	200	
(V_{CE} = 60 Vdc, V_{EB} = 0)	TIP31A, TIP32A		–	200	
(V_{CE} = 80 Vdc, V_{EB} = 0)	TIP31B, TIP32B		–	200	
(V_{CE} = 100 Vdc, V_{EB} = 0)	TIP31C, TIP32C		–	200	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			25	–	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			10	50	
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 375 mAdc)		$V_{CE(sat)}$	–	1.2	Vdc
Base-Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3.0	–	MHz
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		$\|h_{fe}\|$	20	–	–

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 1 – POWER DERATING

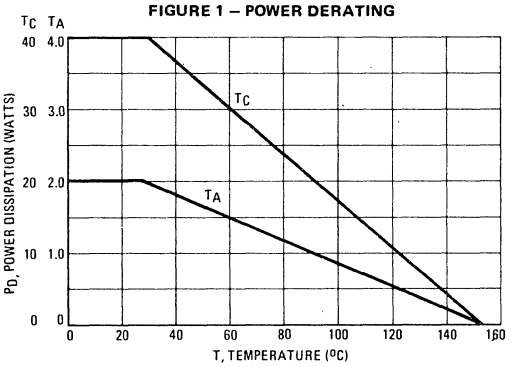
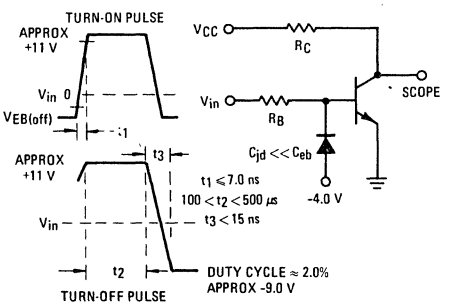


FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT



RB and RC VARIED TO OBTAIN|DESIRED CURRENT LEVELS.

FIGURE 3 – TURN-ON TIME

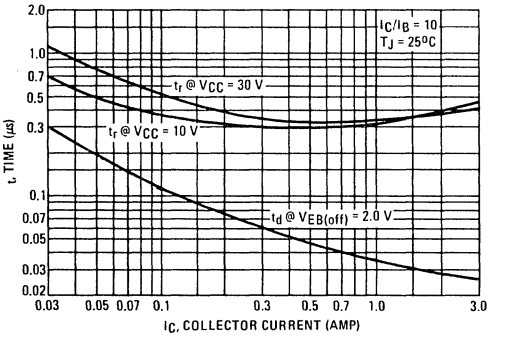


FIGURE 4 – THERMAL RESPONSE

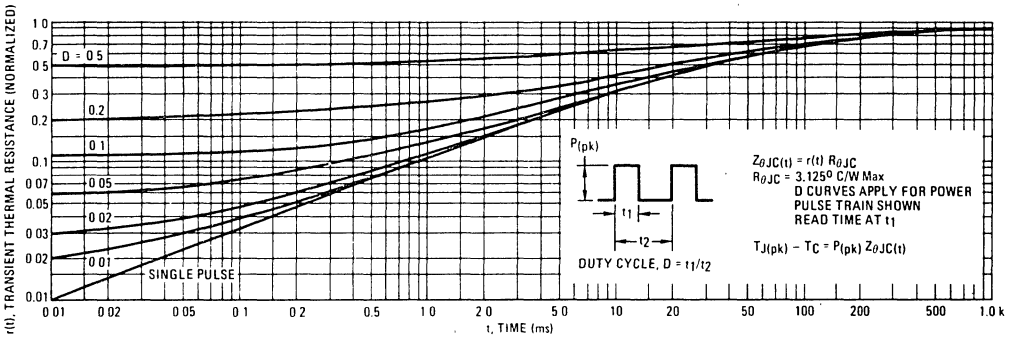


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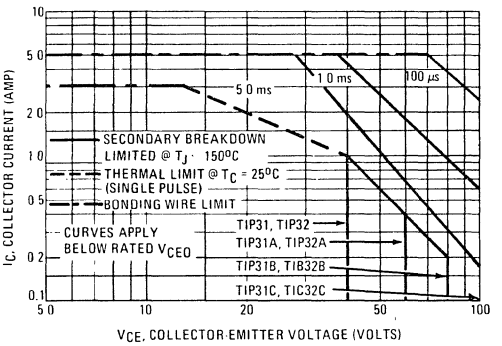
FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

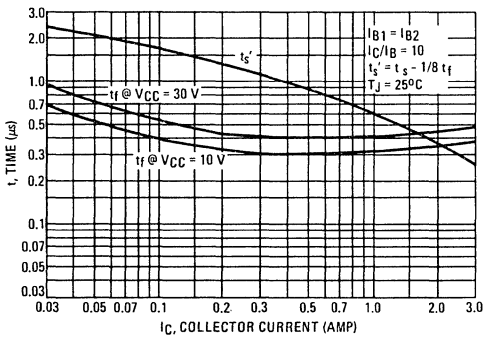


FIGURE 7 – CAPACITANCE

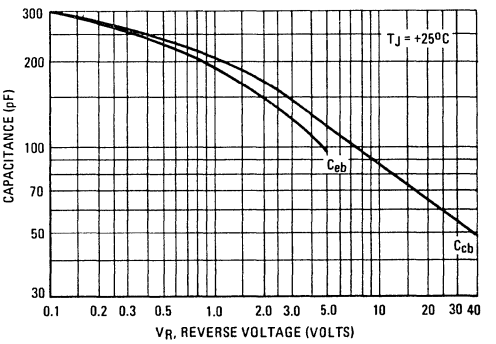


FIGURE 8 – DC CURRENT GAIN

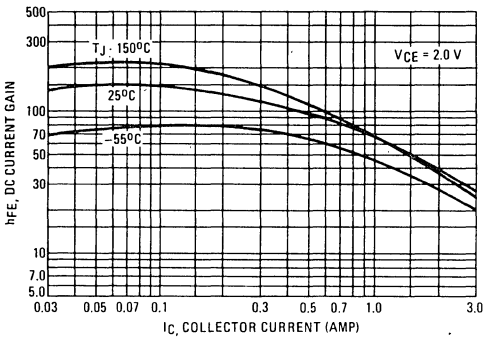


FIGURE 9 – COLLECTOR SATURATION REGION

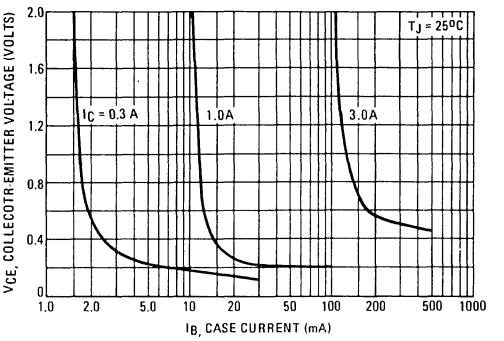


FIGURE 10 – "ON" VOLTAGES

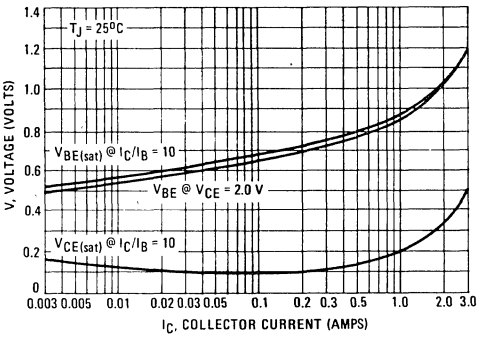


FIGURE 11 – TEMPERATURE COEFFICIENTS

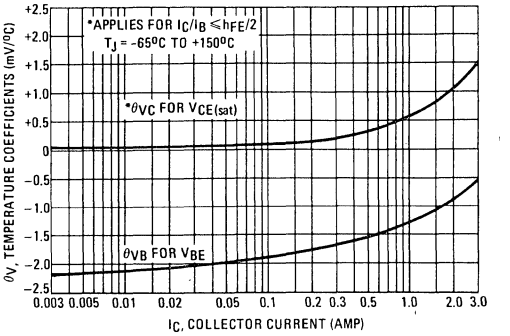


FIGURE 12 – COLLECTOR CUT-OFF REGION

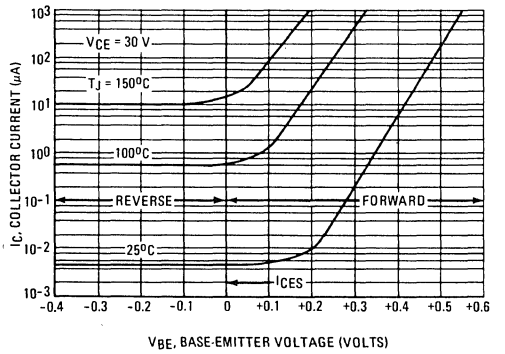
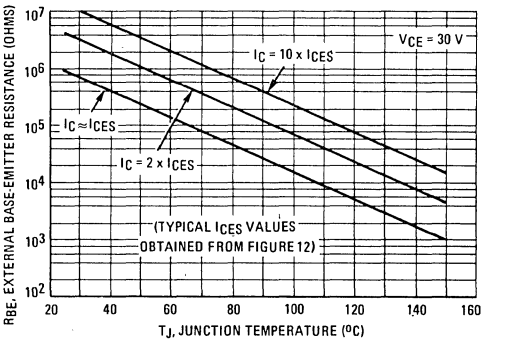


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



NPN PNP

TIP41 TIP42
TIP41A TIP42A
TIP41B TIP42B
TIP41C TIP42C

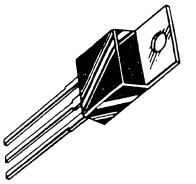
COMPLEMENTARY SILICON PLASTIC POWER TRANSISTORS

. . . designed for use in general purpose amplifier and switching applications.

- Collector-Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 6.0 Adc
- Collector-Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 40 Vdc (Min) — TIP41, TIP42
  = 60 Vdc (Min) — TIP41A, TIP42A
  = 80 Vdc (Min) — TIP41B, TIP42B
  = 100 Vdc (Min) — TIP41C, TIP42C
- High Current Gain — Bandwidth Product f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO-220AB Package
- TO-66 Leadform Also Available

6 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON

40-60-80-100 VOLTS
65 WATTS



4

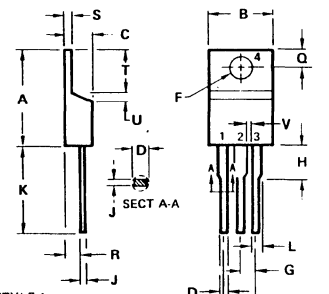
*MAXIMUM RATINGS

Rating	Symbol	TIP41 TIP42	TIP41A TIP42A	TIP41B TIP42B	TIP41C TIP42C	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current - Continuous	I_C	6				Adc
Peak		10				
Base Current	I_B	2.0				Adc
Total Power Dissipation @ T_C = 25°C	P_D	65				Watts
Derate above 25°C		0.52				W/°C
Total Power Dissipation @ T_A = 25°C	P_D	2.0				Watts
Derate above 25°C		0.016				W/°C
Unclamped Inductive Load Energy (1)	E	62.5				°C/W
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance , Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) I_C = 2.8 A, L = 50 mH, P.R.F. = 10 Hz, V_{CC} = 10 V, R_{BE} = 100 Ω.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP41, TIP42	$V_{CEO(sus)}$	40	–	Vdc
	TIP41A, TIP42A		60	–	
	TIP41B, TIP42B		80	–	
	TIP41C, TIP42C		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP41, TIP41A, TIP42, TIP42A		–	0.7	
(V_{CE} = 60 Vdc, I_B = 0)	TIP41B, TIP41C, TIP42B, TIP42C		–	0.7	
Collector Cutoff Current		I_{CES}			μAdc
(V_{CE} = 40 Vdc, V_{EB} = 0)	TIP41, TIP42		–	400	
(V_{CE} = 60 Vdc, V_{EB} = 0)	TIP41A, TIP42A		–	400	
(V_{CE} = 80 Vdc, V_{EB} = 0)	TIP41B, TIP42B		–	400	
(V_{CE} = 100 Vdc, V_{EB} = 0)	TIP41C, TIP42C		–	400	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.3 Adc, V_{CE} = 4.0 Vdc)			30	–	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			15	75	
Collector-Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 600 mAdc)		$V_{CE(sat)}$	–	1.5	Vdc
Base-Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3.0	–	MHz
Small-Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		$\|h_{fe}\|$	20	–	–

(1) Pulse Test: Pulsewidth ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 1 – POWER DERATING

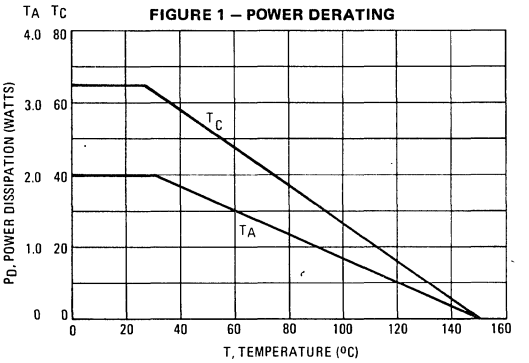
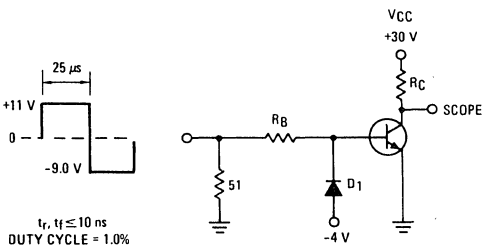


FIGURE 2 – SWITCHING TIME TEST CIRCUIT



RB and RC VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg:
MBD5300 USED ABOVE I_B ≈100 mA
MSD6100 USED BELOW I_B ≈100 mA

FIGURE 3 – TURN-ON TIME

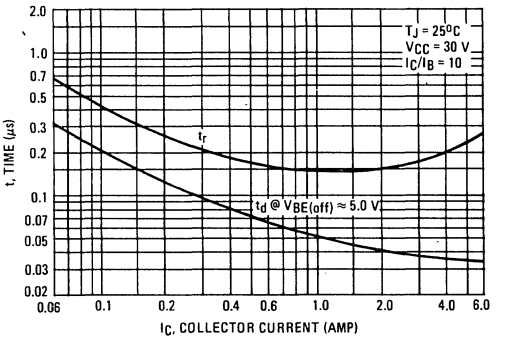


FIGURE 4 – THERMAL RESPONSE

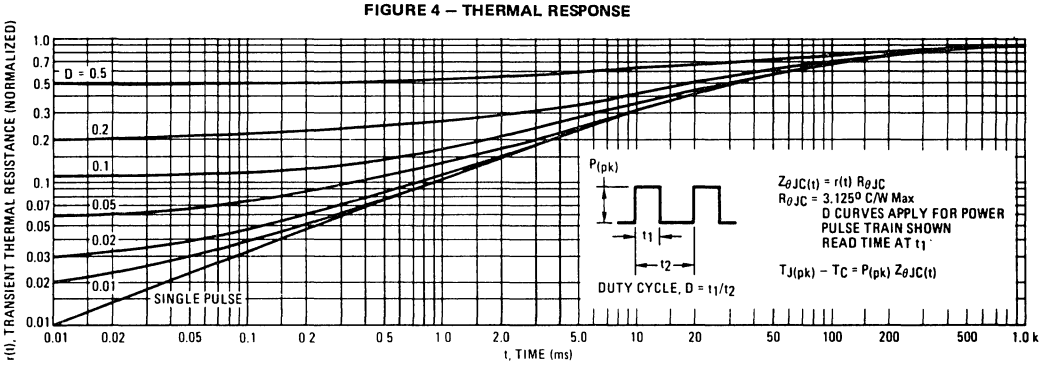


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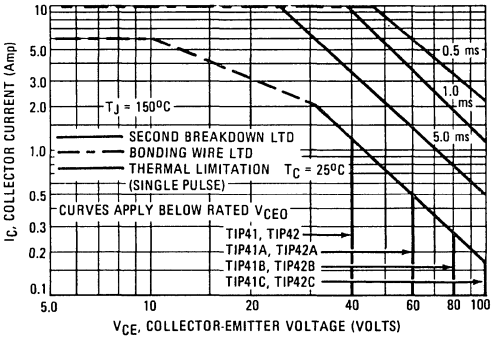
FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{o}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leqslant 150^{o}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

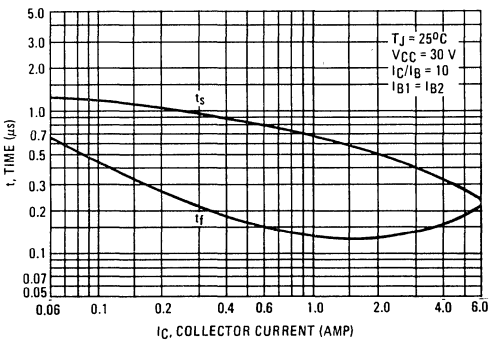


FIGURE 7 – CAPACITANCE

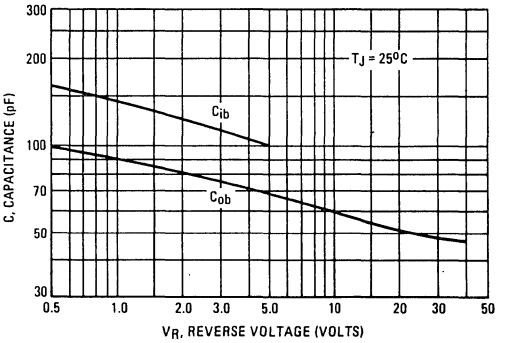


FIGURE 8 – DC CURRENT GAIN

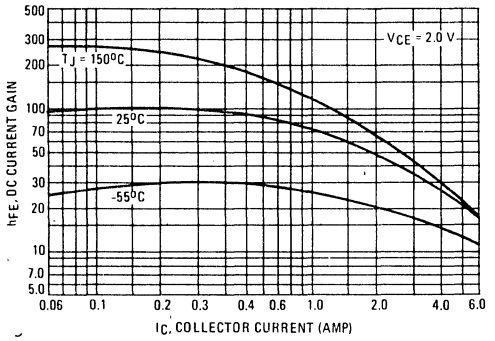


FIGURE 9 – COLLECTOR SATURATION REGION

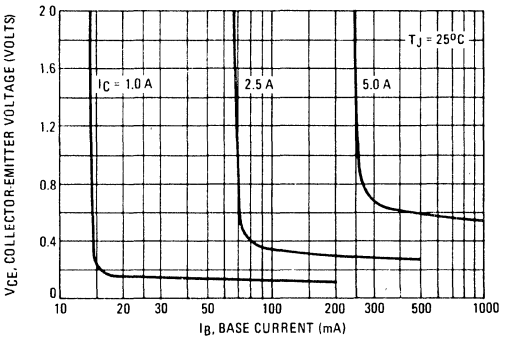


FIGURE 10 – "ON" VOLTAGES

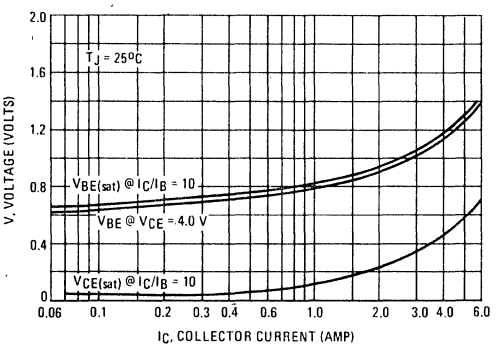


FIGURE 11 – TEMPERATURE COEFFICIENTS

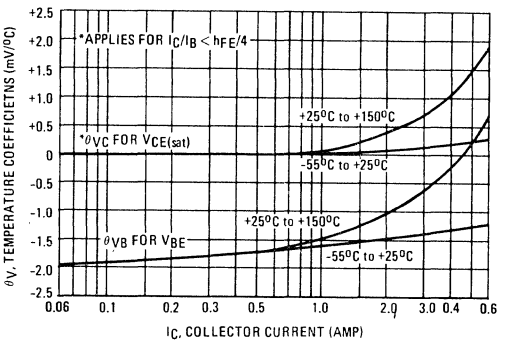


FIGURE 12 – COLLECTOR CUT-OFF REGION

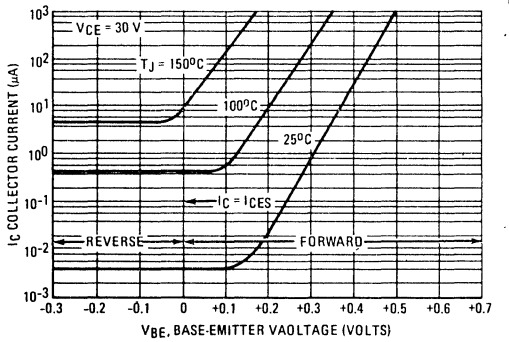
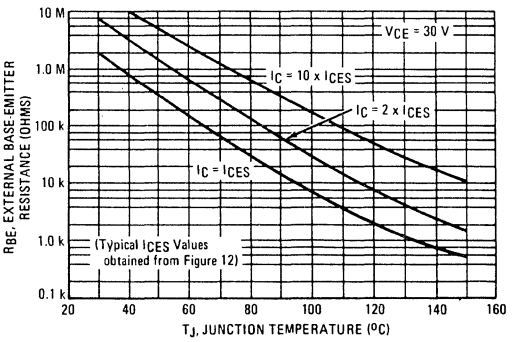


FIGURE 13 – EFFECTS OF BASE-EMITTER RESISTANCE



TIP47 TIP48
TIP49 TIP50

HIGH VOLTAGE NPN SILICON POWER TRANSISTORS

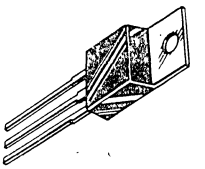
. . . designed for line operated audio output amplifier, Switchmode[1] power supply drivers and other switching applications.

- 250 V to 400 V (Min) – $V_{CEO(sus)}$
- 1 A Rated Collector Current
- Popular TO-220 Plastic Package
- TO-66 Leadform Available

1.0 AMPERE

POWER TRANSISTORS NPN SILICON

250-300-350-400 VOLTS
40 WATTS



4

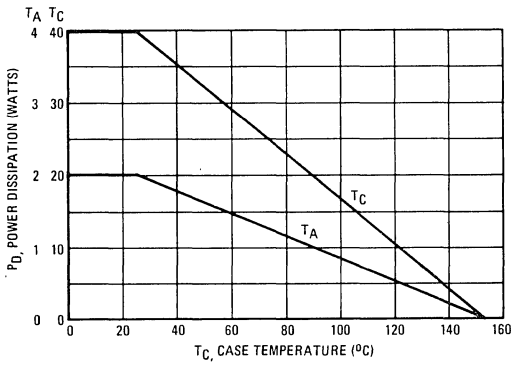
MAXIMUM RATINGS

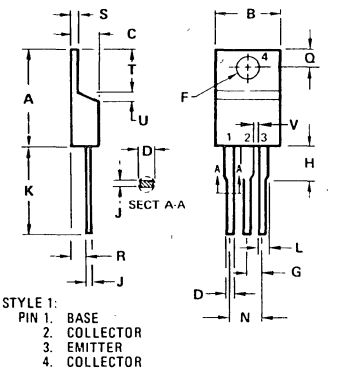
Rating	Symbol	TIP47	TIP48	TIP49	TIP50	Unit
Collector-Emitter Voltage	V_{CEO}	250	300	350	400	Vdc
Collector-Base Voltage	V_{CB}	350	400	450	500	Vdc
Emitter-Base Voltage	V_{EB}	5.0				Vdc
Collector Current—Continuous	I_C	1.0				Adc
Peak		2.0				
Base Current	I_B	0.6				Adc
Total Power Dissipation @ T_C = 25° C	P_D	40				Watts
Derate above 25° C		0.32				W/°C
Total Power Dissipation @ T_A = 25° C	P_D	2.0				Watts
Derate above 25° C		0.016				W/°C
Unclamped Inducting Load Energy (See Figure 8)	E	20				mJ
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02
TO-220AB

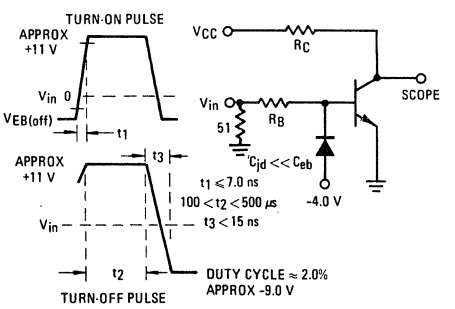
[1] Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)	TIP47	$V_{CEO(sus)}$	250	–	Vdc
(I_C = 30 mAdc, I_B = 0)	TIP48		300	–	
	TIP49		350	–	
	TIP50		400	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 150 Vdc, I_B = 0)	TIP47		–	1.0	
(V_{CE} = 200 Vdc, I_B = 0)	TIP48		–	1.0	
(V_{CE} = 250 Vdc, I_B = 0)	TIP49		–	1.0	
(V_{CE} = 300 Vdc, I_B = 0)	TIP50		–	1.0	
Collector Cutoff Current		I_{CES}			mAdc
(V_{CE} = 350 Vdc, V_{BE} = 0)	TIP47		–	1.0	
(V_{CE} = 400 Vdc, V_{BE} = 0)	TIP48		–	1.0	
(V_{CE} = 450 Vdc, V_{BE} = 0)	TIP49		–	1.0	
(V_{CE} = 500 Vdc, V_{BE} = 0)	TIP50		–	1.0	
Emitter Cutoff Current		I_{EBO}	–	1.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.3 Adc, V_{CE} = 10 Vdc)			30	150	
(I_C = 1.0 Adc, V_{CE} = 10 Vdc)			10	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	–	1.0	Vdc
(I_C = 1.0 Adc, I_B = 0.2 Adc)					
Base-Emitter On Voltage		$V_{BE(on)}$	–	1.5	Vdc
(I_C = 1.0 Adc, V_{CE} = 10 Vdc)					
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product		f_T	10	–	MHz
(I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 2.0 MHz)					
Small-Signal Current Gain		h_{fe}	25	–	–
(I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)					

(1) Pulse Test: Pulsewidth ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS.

FIGURE 3 – TURN-ON TIME

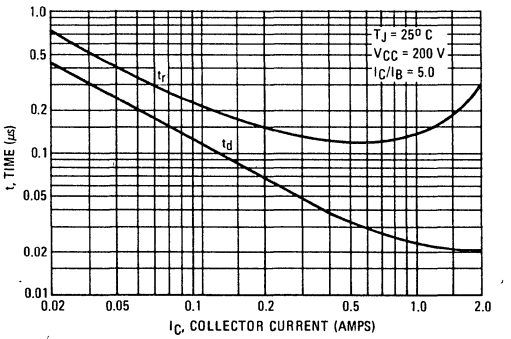


FIGURE 4 – THERMAL RESPONSE

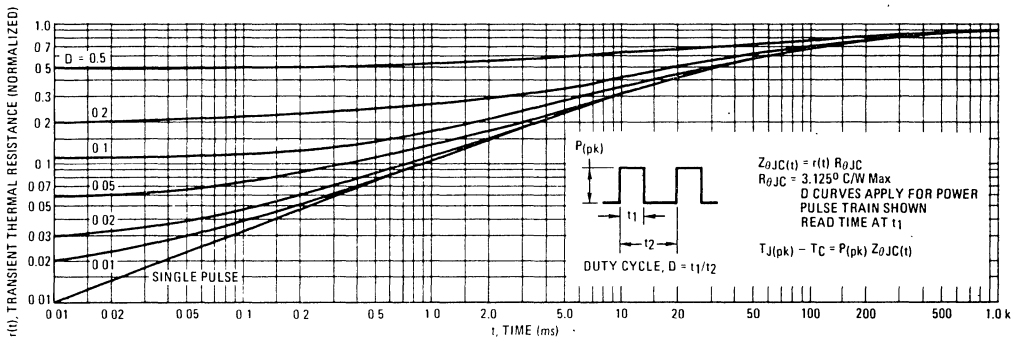
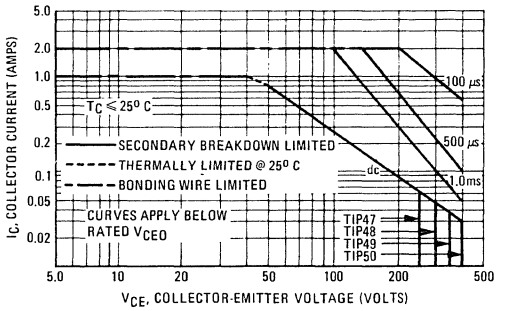


FIGURE 5 – ACTIVE REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 6 – TURN-OFF TIME

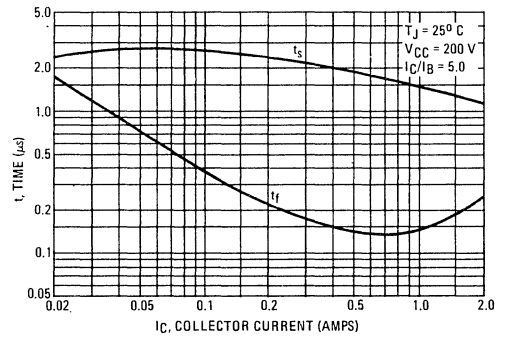


FIGURE 7 – TEMPERATURE COEFFICIENTS

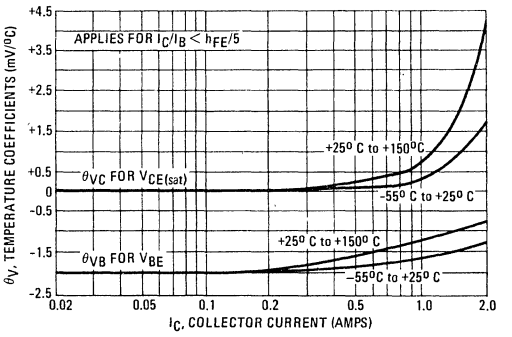
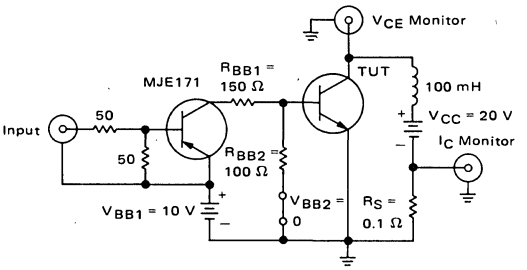


FIGURE 8 – INDUCTIVE LOAD SWITCHING

Test Circuit



Note A: Input pulse width is increased until I_{CM} = 0.63 A.

Voltage and Current Waveforms

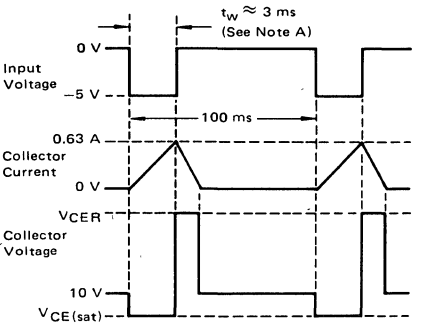


FIGURE 9 – DC CURRENT GAIN

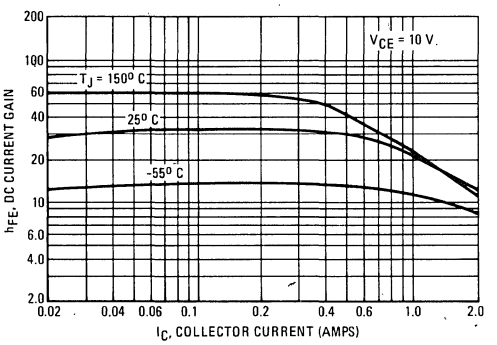
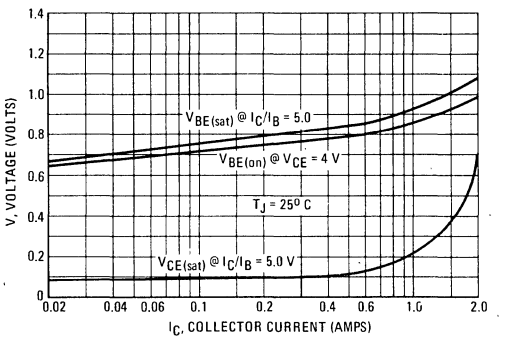


FIGURE 10 – "ON" VOLTAGES



NPN PNP

TIP100 TIP105
TIP101 TIP106
TIP102 TIP107

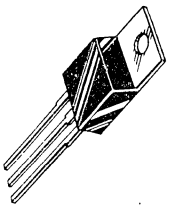
PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain – h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage – @ 30 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) – TIP100, TIP105
  = 80 Vdc (Min) – TIP101, TIP106
  = 100 Vdc (Min) – TIP102, TIP107
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 2.5 Vdc (Max) @ I_C = 8.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- TO-66 Leadform Also Available

DARLINGTON 8 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60-80-100 VOLTS
80 WATTS



*MAXIMUM RATINGS

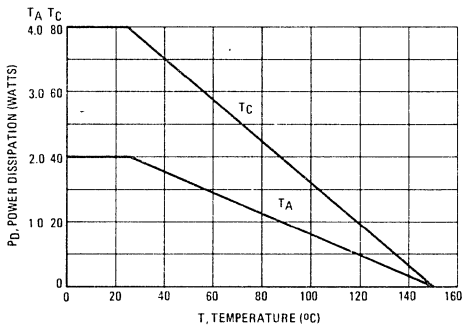
Rating	Symbol	TIP100, TIP105	TIP101, TIP106	TIP102, TIP107	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous	I_C	8.0			Adc
Peak		15			
Base Current	I_B	1.0			Adc
Total Power Dissipation @ T_C = 25°C	P_D	80			Watts
Derate above 25°C		0.64			W/°C
Unclamped Inductive Load Energy (1)	E	30			mJ
Total Power Dissipation @ T_A = 25°C	P_D	2.0			Watts
Derate above 25°C		0.016			W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150			°C

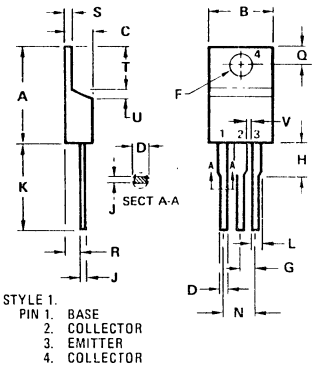
THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) I_C = 1.1 A, L = 50 mH, P.R.F. = 10 Hz, V_{CC} = 20 V, R_{BE} = 100 Ω.

FIGURE 1 – POWER DERATING





STYLE 1.
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	TIP100, TIP105		60	–	
	TIP101, TIP106		80	–	
	TIP102, TIP107		100	–	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP100, TIP105		–	50	
(V_{CE} = 40 Vdc, I_B = 0)	TIP101, TIP106		–	50	
(V_{CE} = 50 Vdc, I_B = 0)	TIP102, TIP107		–	50	
Collector Cuttoff Current		I_{CBO}			μAdc
(V_{CB} = 60 Vdc, I_E = 0)	TIP100, TIP105		–	50	
(V_{CB} = 80 Vdc, I_E = 0)	TIP101, TIP106		–	50	
(V_{CB} = 100 Vdc, I_E = 0)	TIP102, TIP107		–	50	
Emitter Cutoff Current		I_{EBO}	–	8.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON-CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			1000	20,000	
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)			200	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 6.0 mAdc)			–	2.0	
(I_C = 8.0 Adc, I_B = 80 mAdc)			–	2.5	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)			–	2.8	
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain		$\lvert h_{fe} \rvert$			
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)			4.0	–	–
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	TIP105, TIP106, TIP107		–	300	
	TIP100, TIP101, TIP102		–	200	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

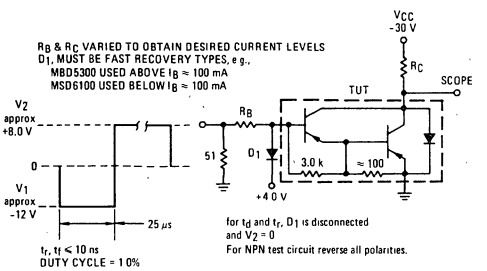


FIGURE 3 – SWITCHING TIMES

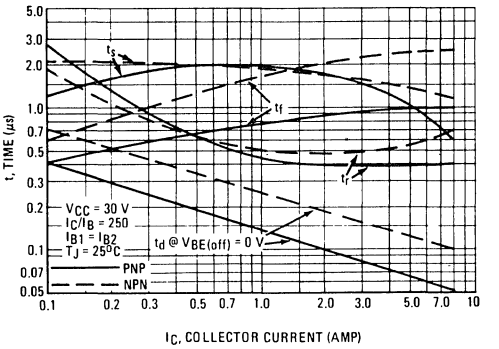


FIGURE 4 – THERMAL RESPONSE

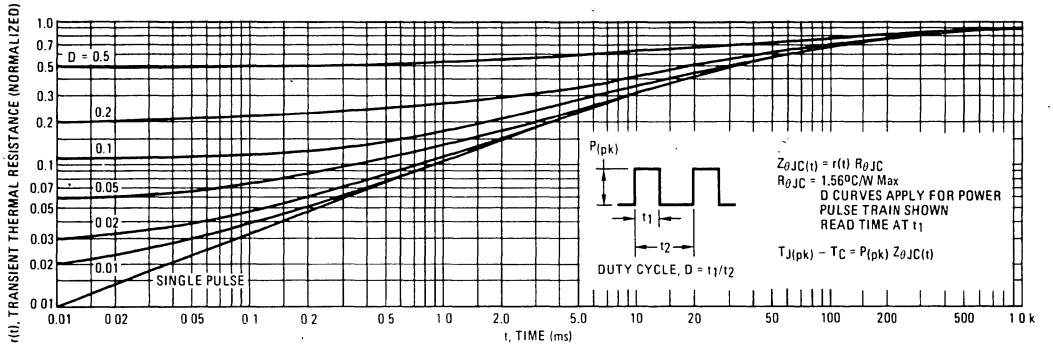
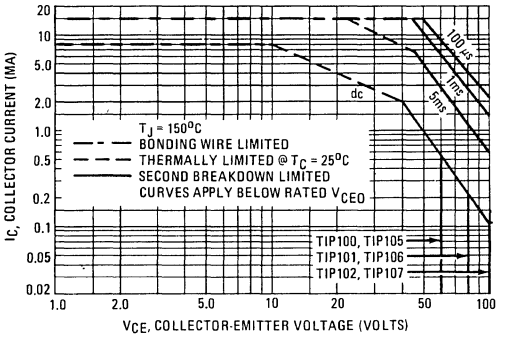


FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

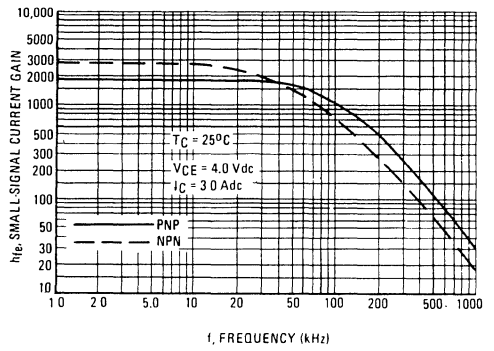
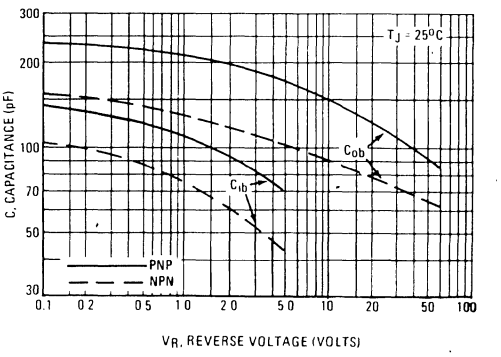


FIGURE 7 – CAPACITANCE

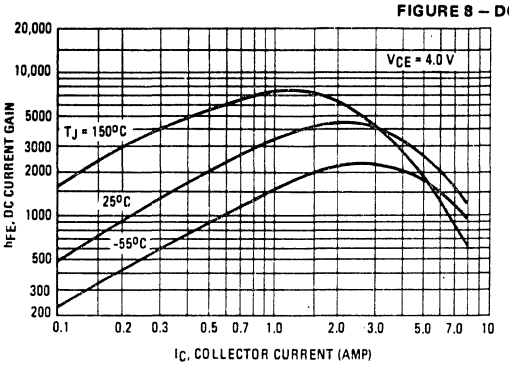


4

NPN
TIP100, TIP101, TIP102

PNP
TIP105, TIP106, TIP107

FIGURE 8 – DC CURRENT GAIN



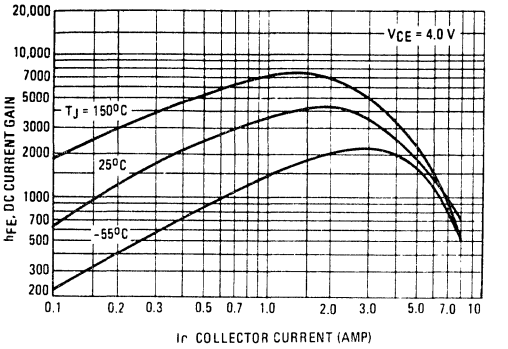
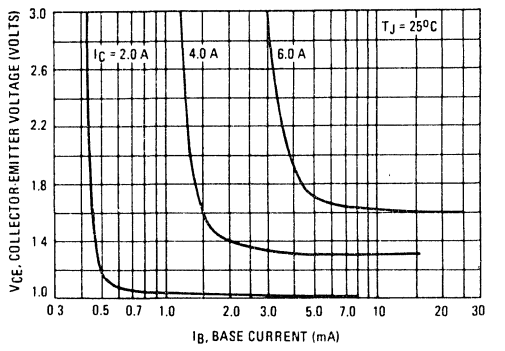


FIGURE 9 – COLLECTOR SATURATION REGION



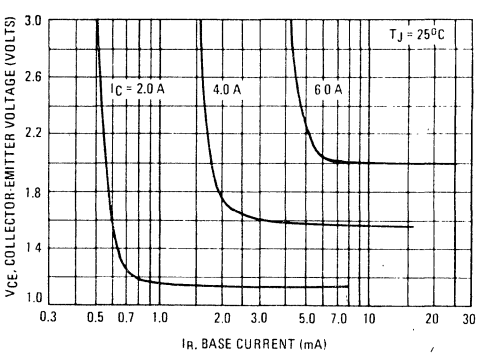
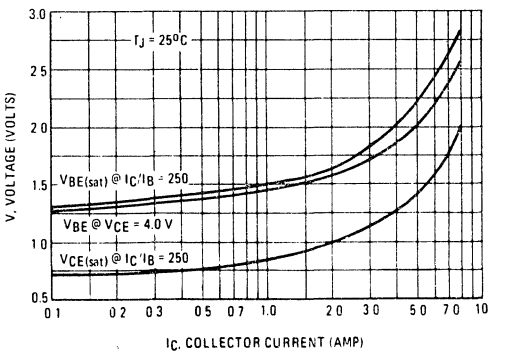
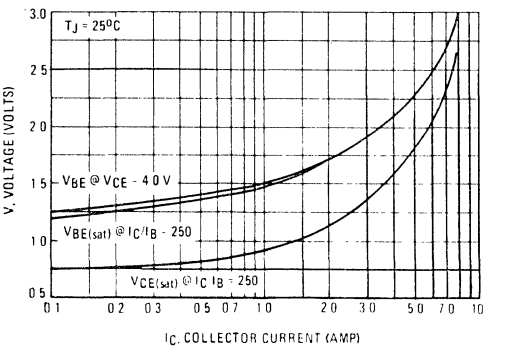


FIGURE 10 – "ON" VOLTAGES





NPN
TIP100, TIP101, TIP102

PNP
TIP105, TIP106, TIP107

FIGURE 11 – TEMPERATURE COEFFICIENTS

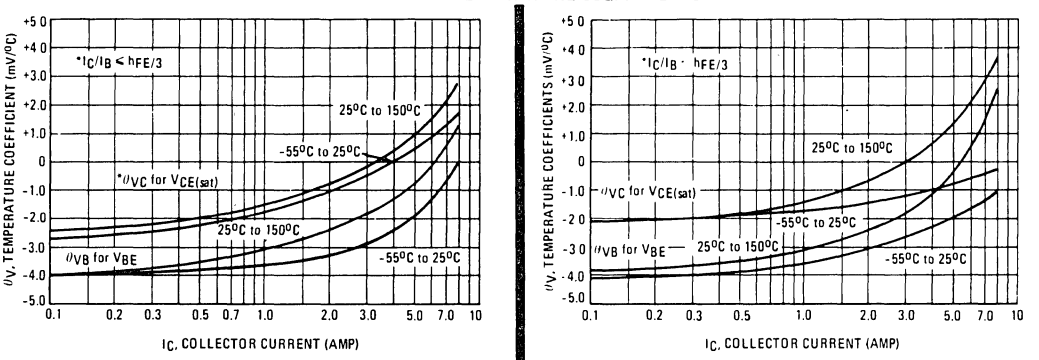


FIGURE 12 – COLLECTOR CUT-OFF REGION

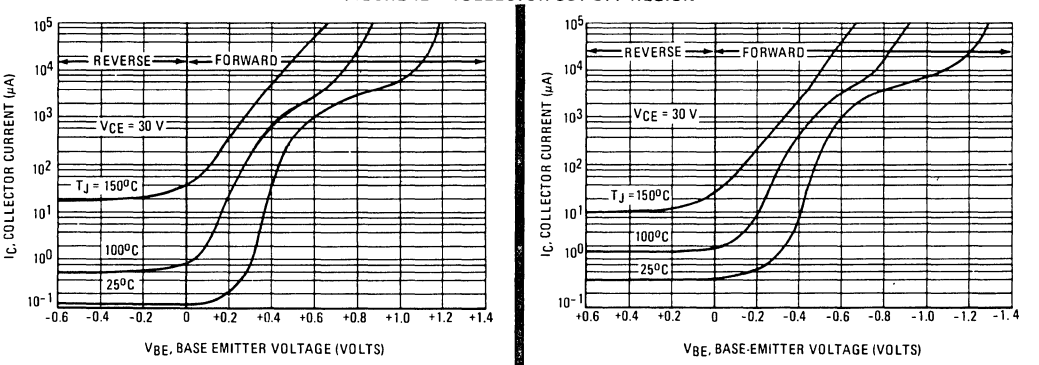
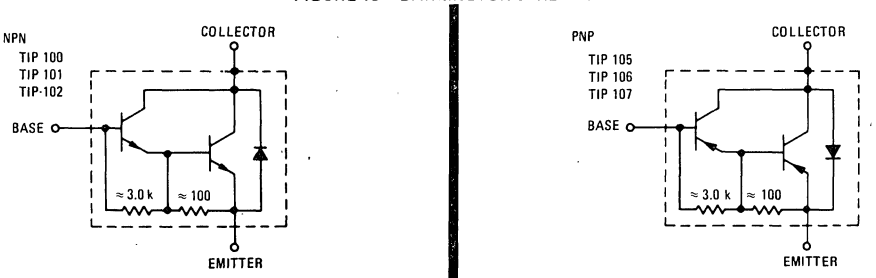


FIGURE 13 – DARLINGTON SCHEMATIC



NPN PNP

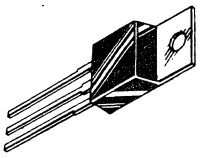
TIP110 TIP115
TIP111 TIP116
TIP112 TIP117

PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain – h_{FE} = 2500 (Typ) @ I_C = 1.0 Adc
- Collector-Emitter Sustaining Voltage – @ 30 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) – TIP110, TIP115
  = 80 Vdc (Min) – TIP111, TIP116
  = 100 Vdc (Min) – TIP112, TIP117
- Low Collector-Emitter Saturation Voltage – $V_{CE(sat)}$ = 2.5 Vdc (Max) @ I_C = 2.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- TO-66 Leadform Also Available

DARLINGTON
2 AMPERE
COMPLEMENTARY SILICON POWER TRANSISTORS
60-80-100 VOLTS
50 WATTS



4

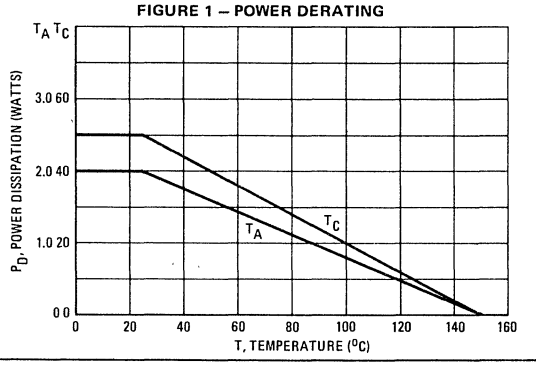
*MAXIMUM RATINGS

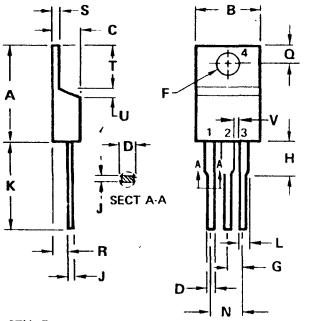
Rating	Symbol	TIP110, TIP115	TIP111, TIP116	TIP112, TIP117	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	◄ 5.0 ►			Vdc
Collector Current – Continuous Peak	I_C	◄ 2.0 ► ◄ 4.0 ►			Adc
Base Current	I_B	◄ 50 ►			mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	◄ 50 ► ◄ 0.4 ►			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	◄ 2.0 ► ◄ 0.016 ►			Watts W/°C
Unclamped Inductive Load Energy – Figure 13	E	◄ 25 ►			mJ
Operating and Storage Junction,	T_J, T_{stg}	◄ -65 to +150 ►			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
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S	1.14	1.39	0.045	0.055
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U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	TIP110, TIP115		60	–	
	TIP111, TIP116		80	–	
	TIP112, TIP117		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP110, TIP115		–	2.0	
(V_{CE} = 40 Vdc, I_B = 0)	TIP111, TIP116		–	2.0	
(V_{CE} = 50 Vdc, I_B = 0)	TIP112, TIP117		–	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	TIP110, TIP115		–	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	TIP111, TIP116		–	1.0	
(V_{CB} = 100 Vdc, I_E = 0)	TIP112, TIP117		–	1.0	
Emitter Cutoff Current		I_{BO}	–	2.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			1000	–	
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)			500	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 8.0 mAdc)			–	2.5	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)			–	2.8	
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain		$\|h_{fe}\|$			–
(I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)			25	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	TIP115, TIP116, TIP117		–	200	
	TIP110, TIP111, TIP112		–	100	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

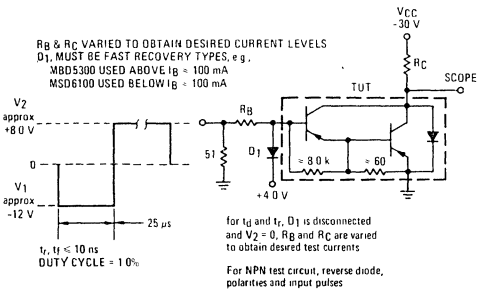


FIGURE 3 – SWITCHING TIMES

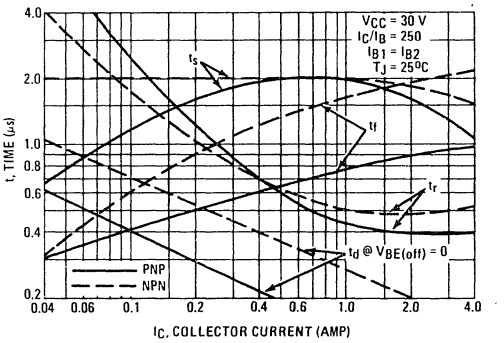
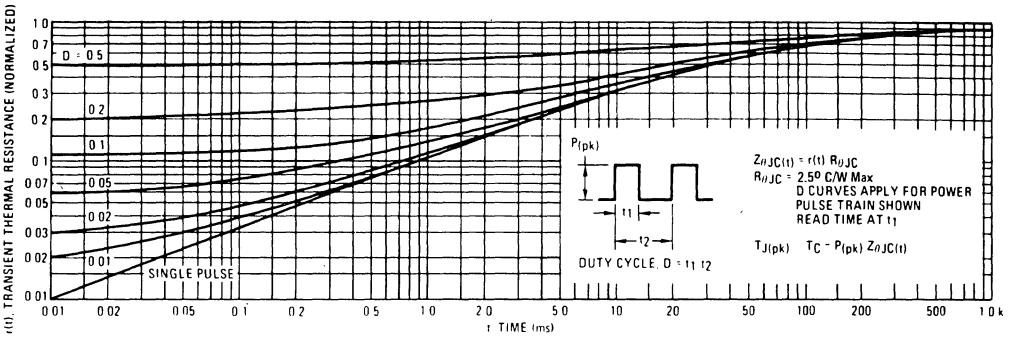


FIGURE 4 – THERMAL RESPONSE



4

ACTIVE-REGION SAFE-OPERATING AREA

FIGURE 5 – TIP115, 116, 117

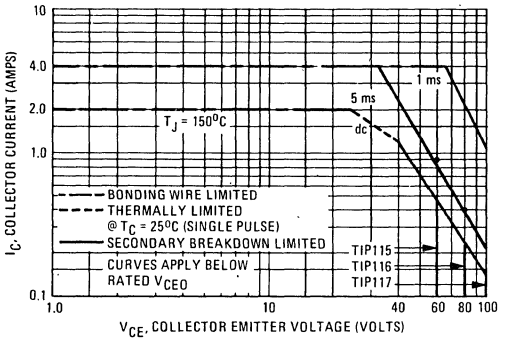
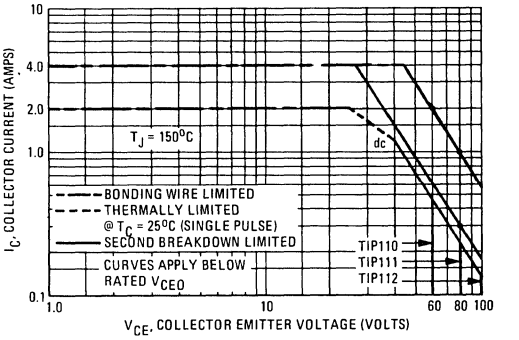


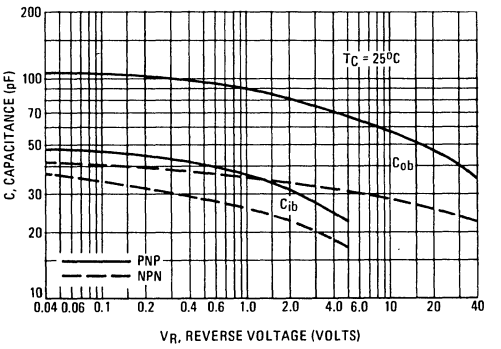
FIGURE 6 – TIP110, 111, 112



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^{\circ}C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 7 – CAPACITANCE



NPN
TIP110, 111, 112

PNP
TIP115, 116, 117

FIGURE 8 – DC CURRENT GAIN

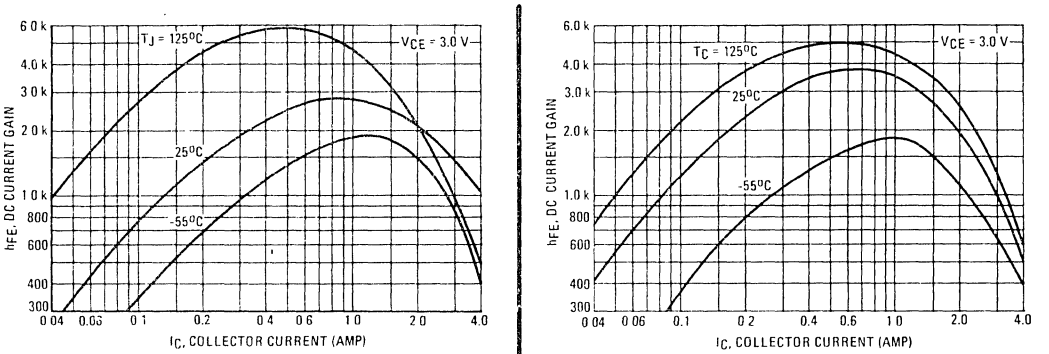


FIGURE 9 – COLLECTOR SATURATION REGION

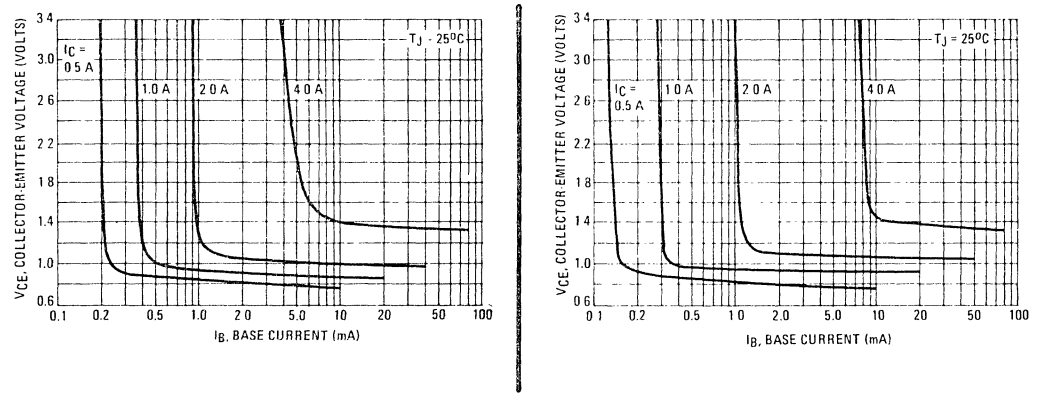
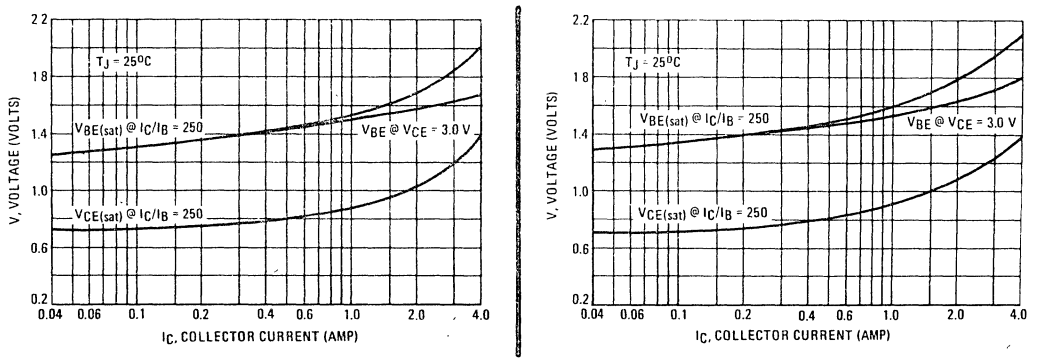


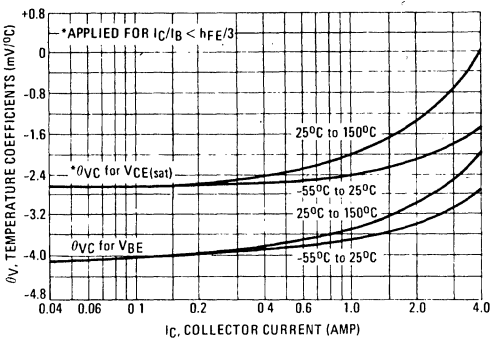
FIGURE 10 – "ON" VOLTAGES

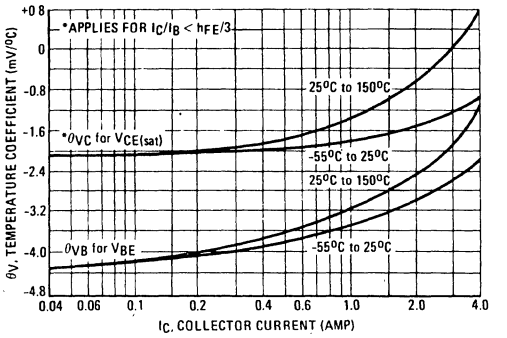


NPN
TIP110, 111, 112

PNP
TIP115, 116, 117

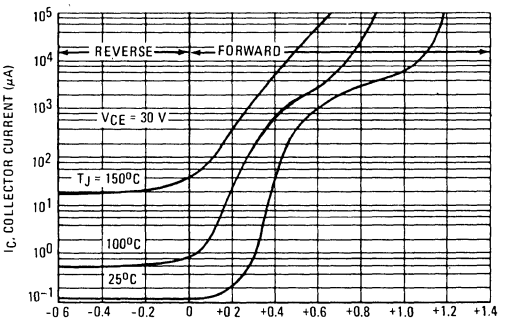
FIGURE 11 – TEMPERATURE COEFFICIENTS





4

FIGURE 12 – COLLECTOR CUT-OFF REGION



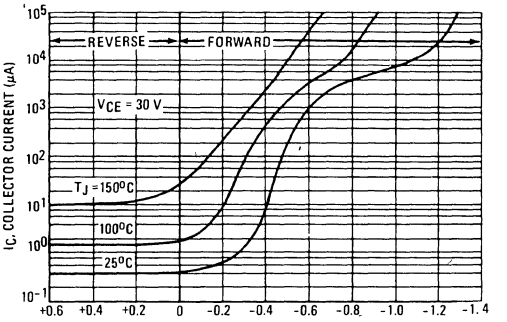
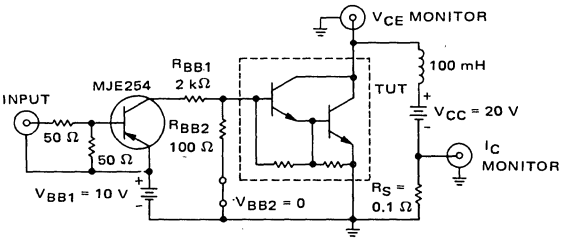


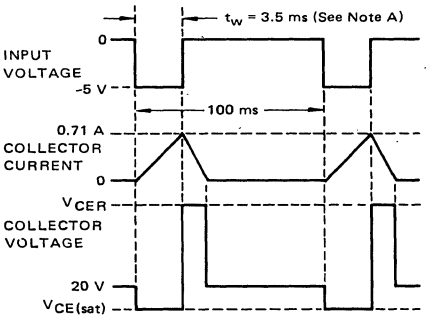
FIGURE 13 – INDUCTIVE LOAD SWITCHING

TEST CIRCUIT



NOTE A: Input pulse width is increased until I_{CM} = 0.71 A, NPN test shown; for PNP test reverse all polarity and use MJE224 driver.

VOLTAGE AND CURRENT WAVEFORMS



NPN PNP

TIP120 TIP125
TIP121 TIP126
TIP122 TIP127

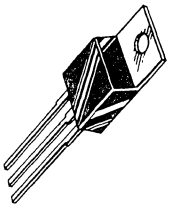
PLASTIC MEDIUM-POWER COMPLEMENTARY SILICON TRANSISTORS

. . . designed for general-purpose amplifier and low-speed switching applications.

- High DC Current Gain – h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector-Emitter Sustaining Voltage – @ 100 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) – TIP120, TIP125
  = 80 Vdc (Min) – TIP121, TIP126
  = 100 Vdc (Min) – TIP122, TIP127
- Low Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 4.0 Vdc (Max) @ I_C = 5.0 Adc
- Monolithic Construction with Built-In Base-Emitter Shunt Resistors
- TO-220AB Compact Package
- TO-66 Leadform Also Available

DARLINGTON 8 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS

60-80-100 VOLTS
65 WATTS



4

*MAXIMUM RATINGS

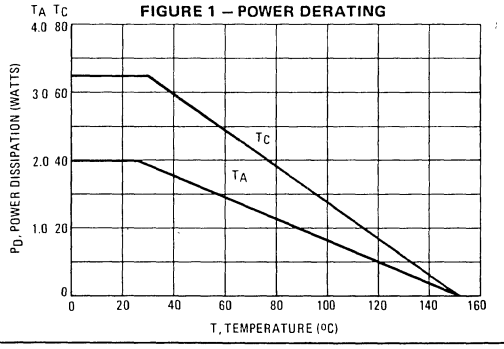
Rating	Symbol	TIP120, TIP125	TIP121, TIP126	TIP122, TIP127	Unit
Collector-Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector-Base Voltage	V_{CB}	60	80	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous	I_C	5.0			Adc
Peak		8.0			
Base Current	I_B	120			mAdc
Total Power Dissipation @ T_C = 25°C	P_D	65			Watts
Derate above 25°C		0.52			W/°C
Total Power Dissipation @ T_A = 25°C	P_D	2.0			Watts
Derate above 25°C		0.016			W/°C
Unclamped Inductive Load Energy (1)	E	50			mJ
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	-65 to +150			°C

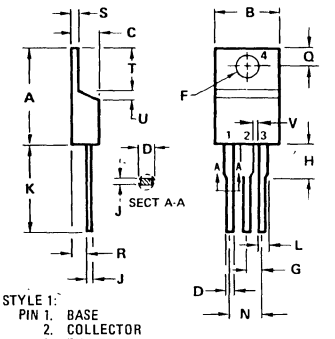
THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) I_C = 1 A, L = 100 mH, P.R.F. = 10 Hz, V_{CC} = 20 V, R_{BE} = 100 Ω.

FIGURE 1 – POWER DERATING





STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	TIP120, TIP125		60	–	
	TIP121, TIP126		80	–	
	TIP122, TIP127		100	–	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP120, TIP125		–	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	TIP121, TIP126		–	0.5	
(V_{CE} = 50 Vdc, I_B = 0)	TIP122, TIP127		–	0.5	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	TIP120, TIP125		–	0.2	
(V_{CB} = 80 Vdc, I_E = 0)	TIP121, TIP126		–	0.2	
(V_{CB} = 100 Vdc, I_E = 0)	TIP122, TIP127		–	0.2	
Emitter Cutoff Current		I_{EBO}	–	2.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 0.5 Adc, V_{CE} = 3.0 Vdc)			1000	–	
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)			1000	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 12 mAdc)			–	2.0	
(I_C = 5.0 Adc, I_B = 20 mAdc)			–	4.0	
Base-Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)			–	2.5	
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain		$\|h_{fe}\|$			–
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)			4.0	–	
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	TIP125, TIP126, TIP127		–	300	
	TIP120, TIP121, TIP122		–	200	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT

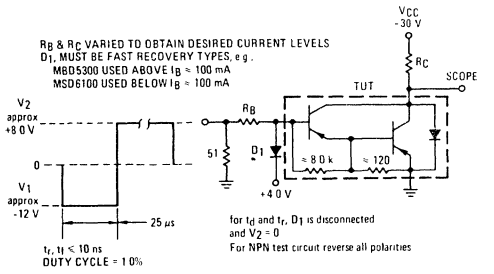


FIGURE 3 – SWITCHING TIMES

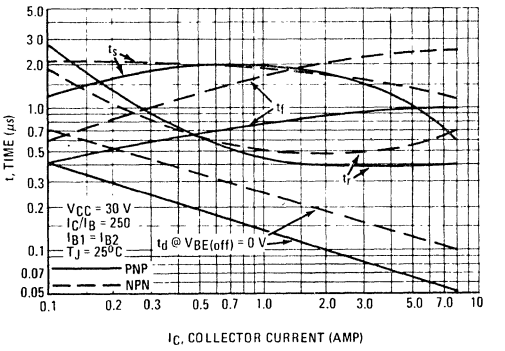
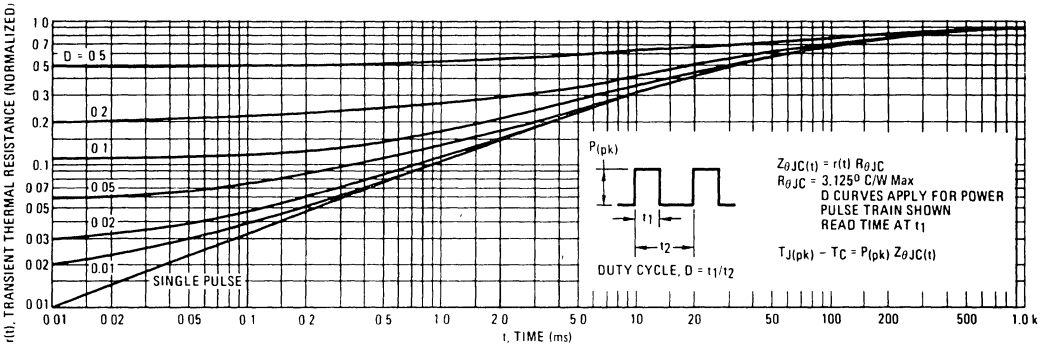
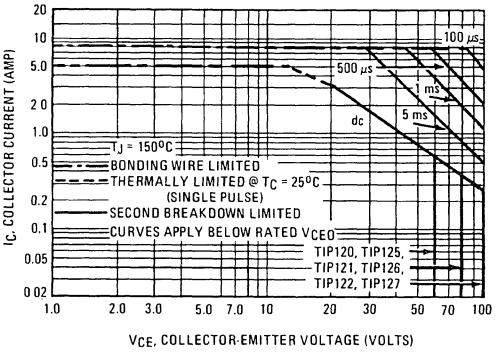


FIGURE 4 – THERMAL RESPONSE



4

FIGURE 5 – ACTIVE-REGION SAFE OPERATING AREA



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^oC$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^oC$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

FIGURE 6 – SMALL-SIGNAL CURRENT GAIN

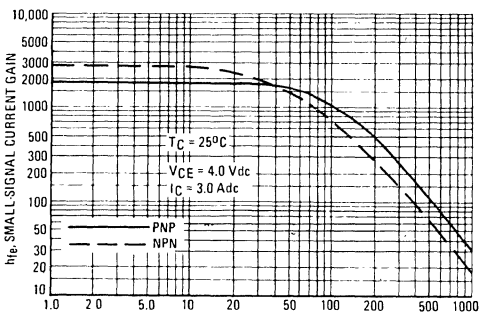
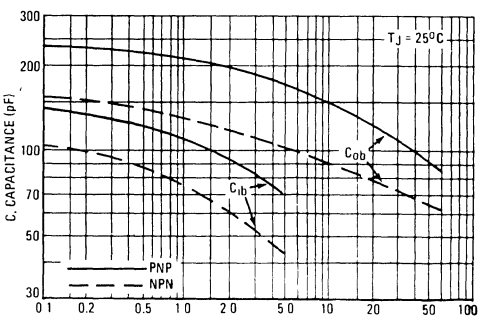


FIGURE 7 – CAPACITANCE

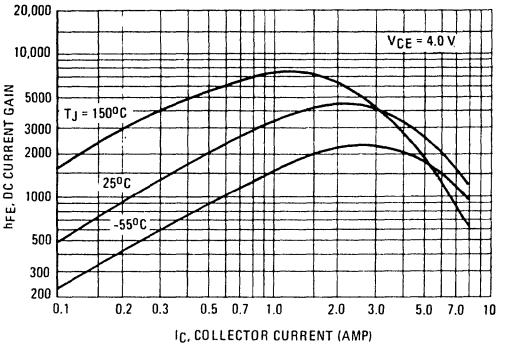


4

NPN
TIP120, TIP121, TIP122

PNP
TIP125, TIP126, TIP127

FIGURE 8 – DC CURRENT GAIN



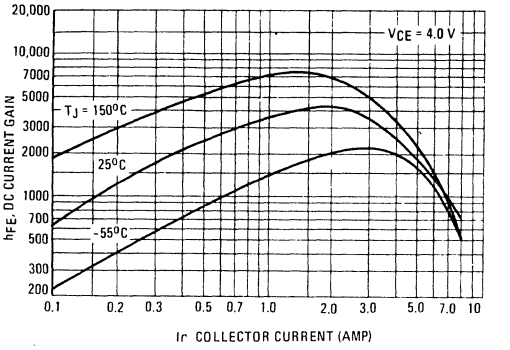
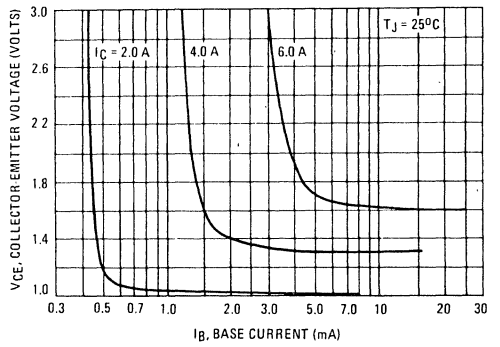


FIGURE 9 – COLLECTOR SATURATION REGION



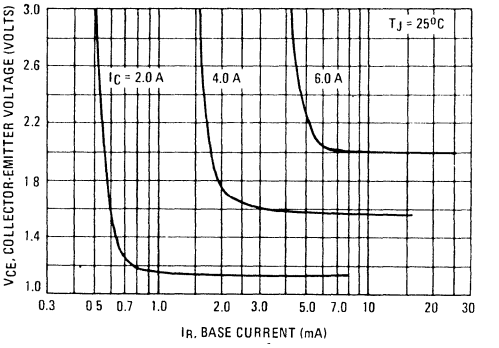
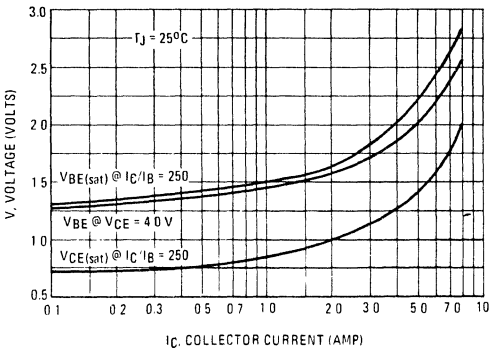
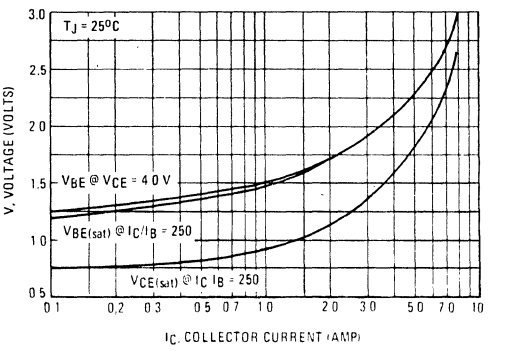


FIGURE 10 – "ON" VOLTAGES





NPN
TIP120, TIP121, TIP122

PNP
TIP125, TIP126, TIP127

FIGURE 11 – TEMPERATURE COEFFICIENTS

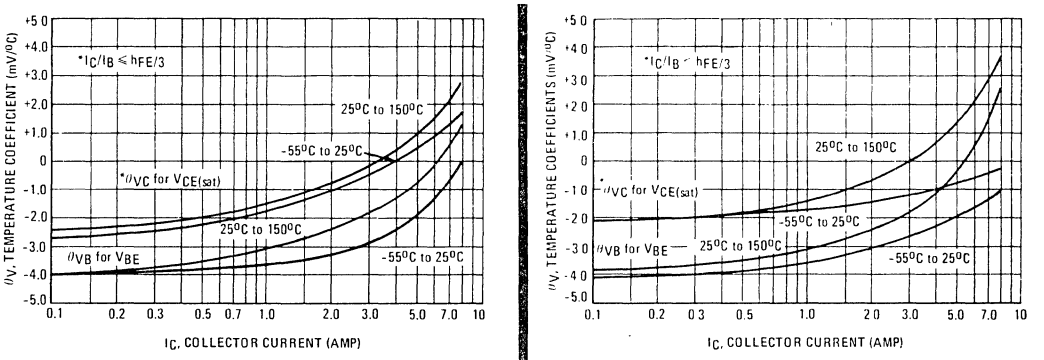


FIGURE 12 – COLLECTOR CUT-OFF REGION

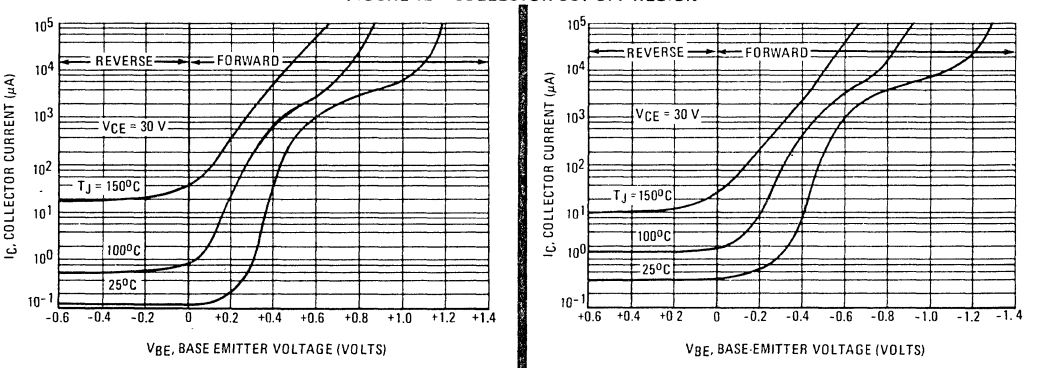
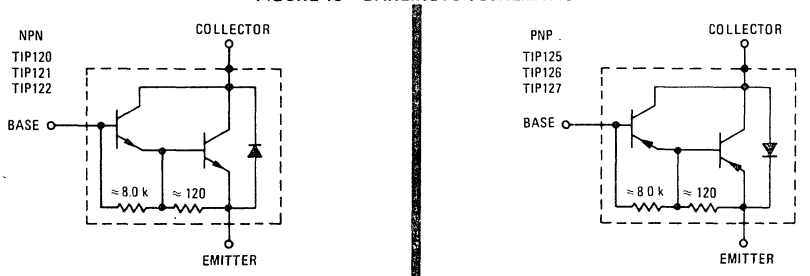


FIGURE 13 – DARLINGTON SCHEMATIC



Thyristor Selector Guide

5

Thyristors . . .

TRIGGERED SWITCHES FOR YOUR POWER HANDLING APPLICATION

Thyristors and their trigger devices can take numerous forms, but they share these characteristics:

- They are "open circuits," capable of withstanding rated voltage until triggered.
- They become low-impedance current paths when triggered, and remain so, even after the trigger source is removed, until current through that path stops, or is reduced below a minimum "holding" level.

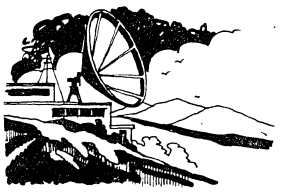
The regenerative action which "holds" a Thyristor in the "on" state is due to multiple layers of opposite P and N silicon, in which part of the load current through the Thyristor is injected to supplement the trigger current, and to sustain conduction when the trigger is removed. This characteristic, coupled with the Thyristor's low "on resistance," makes it possible to control a portion of each cycle of an AC power waveform into a load, in low-dissipation "dimming" or motor speed control applications, to precisely switch capacitive discharge currents in automotive ignition systems, or to efficiently modulate radar systems with high current, fast pulses.

5

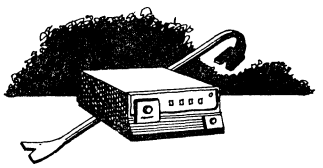
SCRs

Silicon-Controlled Rectifiers (SCRs) are Thyristors intended to switch load currents in one direction only, making them useful for DC and half-wave AC applications as well as full-wave applications, in which bidirectional current is routed in one direction through the SCR via a bridge rectifier.

For battery chargers, flashers and other applications where high humidity conditions might be encountered, the 20 Ampere, metal-packaged, pressfit SCR line is highly popular, due to low manufacturing cost.



High-current Radar pulse modulator SCRs.

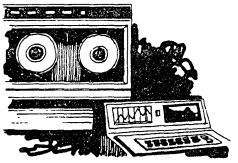


Types 2N6506, 2N3896 and 2N6396 are especially suited for use in Power Supply Crowbar Protection.

TRIACs

Triacs are bidirectional Thyristors, in which a single trigger source turns the device on for load current in either direction. Because they do not require a bridge rectifier in order to handle full-wave AC, Triacs are useful in AC power applications that require full source power control capability to be applied to the load.

For high-volume consumer use in power switches, lamp dimmers, and motor speed controls, consider the low-cost, medium-current, plastic packaged 2N6342.



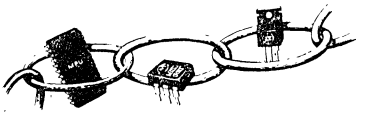
For high sensitivity and IC logic compatibility, investigate the MAC92 and 2N6068 series of Triacs.

In AC-operated appliances that use quick-disconnect terminals for assembly ease, such as Microwave Ovens, Motor Controls, and Space Heaters, check out the MAC20, MAC25, and MAC50 series.

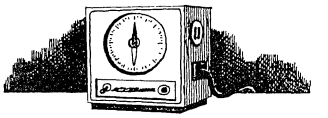
TRIGGER DEVICES

Motorola supplies a variety of trigger devices whose characteristics and modes of triggering are suited to different signal sources.

- Unijunction Transistors — UJT — A negative resistance, threshold sensitive device especially suited to unidirectional triggering of SCRs, pulse generators, oscillators, and timing circuits.
- Programmable Unijunction Transistors — PUT — Similar to the UJT, but capable of externally preset threshold characteristics via a voltage divider.
- Bilateral Triggers — DIAC — A low-cost bidirectional trigger which can drive a Triac in full-wave AC applications.
- Silicon Bidirectional Switch — SBS — Similar to a DIAC, the SBS has an added gate electrode for external synchronization.
- Optically Coupled Triac Driver — Allows bidirectional Triac triggering from low-level logic, such as Microprocessor outputs, while isolating these sensitive sources by as much as 1500V from AC line transients.



To isolate sensitive ICs, such as Microprocessors from damaging line voltages, the Power Triac may be driven by an Optically Coupled Triac Driver.



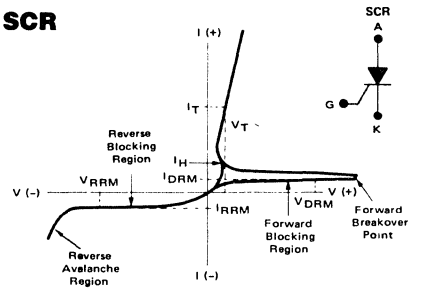
For applications in which an AC load is turned off after a fixed time interval, Motorola offers a selection of UJTs and PUTs.

Using Triacs for a dazzling Light Show? Low-cost DIACs or externally triggerable SBSs will turn you on!

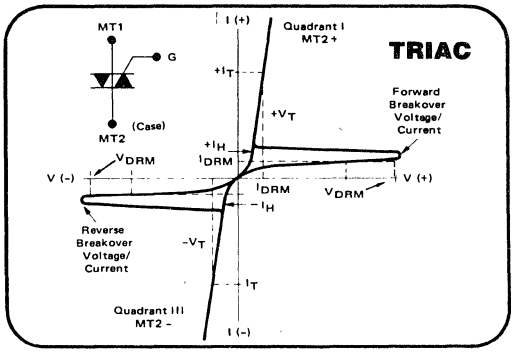
5

CHARACTERISTIC CURVES

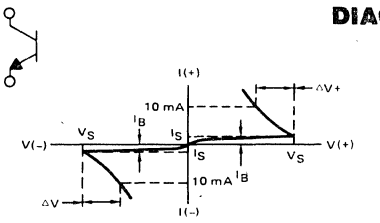
SCR



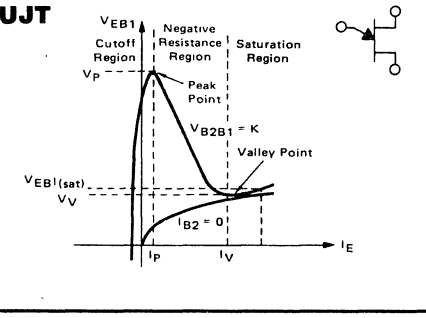
TRIAC



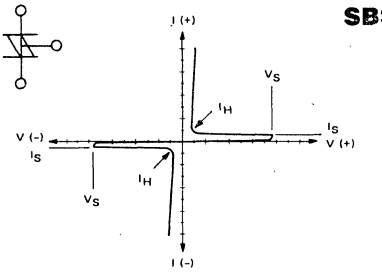
DIAC



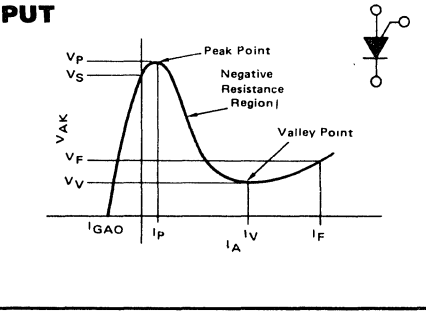
UJT



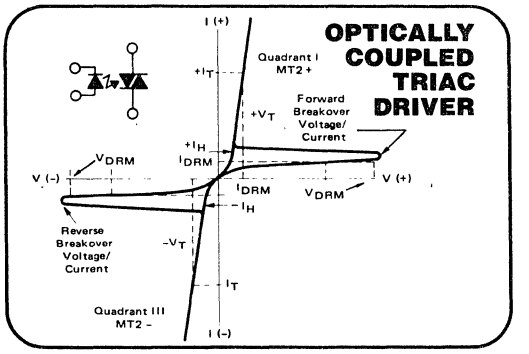
SBS



PUT



OPTICALLY COUPLED TRIAC DRIVER



NUMERIC INDEX

The following Motorola device types are recommended from the standpoint of cost, performance and delivery. If your specific requirement is not included in this listing (or the one below it), please ask your Motorola Sales Representative for special price and delivery information.

Device Type

MAC Devices (Triacs)
MAC15
MAC15A
MAC20
MAC20A
MAC25
MAC25A
MAC35
MAC36
MAC37
MAC38
MAC50
MAC50A
MAC92
MAC220
MAC221
MAC40688 Replaced by T6420B
MAC40689 Replaced by T6420D
MAC40690 Replaced by T6420M
MAC40795 Replaced by T4101M
MAC40796 Replaced by T4111M
MAC40799 Replaced by T4121B
MAC40800 Replaced by T4121D
MAC40801 Replaced by T4121M

MBS Devices (Bilateral Switch)
MBS4991
MBS4992

MCR Devices (SCRs)
MCR63
MCR64
MCR65
MCR100
MCR101
MCR102
MCR103
MCR104
MCR106
MCR120
MCR201
MCR202
MCR203
MCR204
MCR205
MCR206
MCR220
MCR221
MCR649AP
MCR729
MCR914
MCR1906
MCR1718
MCR2305 Replaced by 2N4167/74
MCR2604L Replaced by 2N4183/90
MCR3000
MCR3818
MCR3835
MCR3918
MCR3935

Device Type

MOC3010
MOC3011

MPU Devices (Programmable UJT)
MPU131
MPU132
MPU133
MPU6027
MPU6028

MU Devices (UJT)
MU10
MU20
MU2646
MU2647
MU4891
MU4892
MU4893
MU4894

1N Devices (Triggers)
1N5758 to 5762

2N Devices
2N681 to 692
2N1595 to 1599
2N1842 to 1850
2N2322 to 2329
2N2573 to 2579
2N2646
2N2647
2N3668 to 3670
2N3870 to 3873
2N3896 to 3899
2N3980
2N4103
2N4167 to 4174

Device Type

2N4183 to 4190
2N4199 to 4204
2N4212 to 4219
2N4441 to 4444
2N4851 to 4853
2N4870
2N4871
2N4948 to 4949
2N5060 to 5064
2N5164 to 5171
2N5431
2N5441 to 5446
2N5567 to 5570
2N5571 to 5574
2N6027
2N6028
2N6068 to 6075
2N6114
2N6116 to 6118
2N6145 to 6147
2N6151
2N6152
2N6153
2N6154
2N6155
2N6156
2N6157 to 6165
2N6167 to 6170
2N6171 to 6173
2N6174
2N6236 to 6241
2N6342 to 6349
2N6394 to 6399
2N6400 to 6405
2N6504 to 6509

5

The popular device types listed below, originally introduced by other manufacturers, are now produced in volume by Motorola.

Device Type

"C" Devices (SCRs)
C35
C106
C122
C228
C228( )3
C229
C230
C230( )3
C231
C231( )3
C232
C233

"S" Devices (SCRs)
S2800
S6200
S6210
S6220

"SC" Devices (Triacs)
SC136
SC141
SC146
SC245
SC245( )3
SC246

Device Type

SC250
SC250( )3
SC251
SC260
SC260( )3
SC261

"T" Devices (Triacs)
T2300P
T2301P
T2302P
T2500
T2800
T2801

Device Type

T2802
T4100
T4101
T4110
T4111
T4120
T4121
T6400
T6401
T6410
T6411
T6420
T6421

SCRs

. . . Metal or Plastic Packages
. . . 0.5 to 55 Amperes RMS
. . . 25 to 800 Volts
. . . Industry Standards, with a variety of Custom Specifications and Leadforms available.

5

		ON-STATE (RMS) CURRENT							
		0.5 AMP	0.8 AMP	1.6 AMPS				4.0 AMPS	
									
		Case 22-03 TO-18 Style 6	Case 29-02 TO-92 Style 10	Case 79-02 TO-39 Style 3				Case 77-03 TO-126 Style 2	
V_{DRM} V_{RRM}	25 V	MCR202	MCR102 2N5060		2N2322	2N4212	MCR1906-1	MCR106-1 2N6236	C106Y1
	50 V	MCR203	MCR103 2N5061	2N1595	2N2323	2N4213	MCR1906-2	MCR106-2 2N6237	C106F1
	100 V	MCR204	MCR104 2N5062	2N1596	2N2324	2N4214	MCR1906-3	MCR106-3 2N6238	C106A1
	200 V	MCR206	MCR120 2N5064	2N1597	2N2326	2N4216	MCR1906-4	MCR106-4 2N6239	C106B1
	300 V		MCR100-5	2N1598	2N2328	2N4218	MCR1906-5	MCR106-5	C106C1
	400 V		MCR100-6	2N1599	2N2329	2N4219	MCR1906-6	MCR106-6 2N6240	C106D1
	500 V		MCR100-7				MCR1906-7	MCR106-7	C106E1
	600 V		MCR100-8				MCR1906-8	MCR106-8 2N6241	C106M1
	700 V							MCR106-9	
	800 V								
MAXIMUM ELECTRICAL CHARACTERISTICS	I_{TSM} (Amps)	6.0	10	15	15	15	15	25	20
	I_{GT} (mA)	0.2	0.2	10	0.2	0.1	1.0	0.2	0.2
	V_{GT} (V)	0.8	0.8	3.0	0.8	0.8	1.0	1.0	0.8
	I_H (mA)	5.0	5.0	5.0 Typ	2.0	3.0	5.0	5.0	3.0

ON-STATE (RMS) CURRENT									
8.0 AMPS				12 AMPS	12.5 AMPS	16 AMPS			
									
Case 90-05 Style 1	Case 221-02 TO-220AB Style 1	Case 86 Style 1	Case 87L Style 1	Case 221-02 TO-220AB Style 1	Case 54 Style 2	Case 263-03 Style 1	Case 221-02 TO-220AB Style 1		
MCR3000-1		2N4167	2N4183			2N1842 2N1842A		25 V	
2N4441 MCR3000-2	C122F1 S2800F	2N4168	2N4184	2N6394		2N1843 2N1843A	2N6400	50 V	
MCR3000-3	C122A1 S2800A	2N4169	2N4185	2N6395	2N3668	2N1844 2N1844A	2N6401	100 V	
2N4442 MCR3000-4	C122B1 S2800B	2N4170	2N4186	2N6396	2N3669	2N1846 2N1846A	2N6402	200 V	
MCR3000-5	C122C1 S2800C	2N4171	2N4187	MCR220-5		2N1848 2N1848A	MCR221-5	300 V	V_{DRM}
2N4443 MCR3000-6	C122D1 S2800D	2N4172	2N4188	2N6397	2N3670	2N1849 2N1849A	2N6403	400 V	V_{RRM}
MCR3000-7	C122E1 S2800E	2N4173	2N4189	MCR220-7	2N4103	2N1850 2N1850A	MCR221-7	500 V	
2N4444 MCR3000-8	C122M1 S2800M	2N4174	2N4190	2N6398			2N6404	600 V	
MCR3000-9	C122S1 S2800S			MCR220-9			MCR221-9	700 V	
MCR3000-10	C122N1 S2800N			2N6399			2N6405	800 V	
80	C122/S2800 90/100	100		100	200	125	160	I_{TSM} (Amps)	MAXIMUM ELECTRICAL CHARACTERISTICS
30	C122/S2800 25/15	30		30	40	80	30	I_{GT} (mA)	
1.5	1.5	1.5		1.5	2.0	2.0	1.5	V_{GT} (V)	
40	C122/S2800 30/20	30		40	20 Typ	—	40	I_H (mA)	

SCRs (continued)

		ON-STATE (RMS) CURRENT								
		20 AMPS						25 AMPS		
				 Isolated						
		Case 310 Style 1	Case 283 Style 1	Case 311-01 Style 1	Case 54 Style 2	Case 174-03 Style 1	Case 175-02 Style 1	Case 221-02 TO-220AB Style 1	Case 61 TO-41 Style 1	Case 263-03 Style 1
V_{DRM} V_{RRM}	25 V				MCR649P1	MCR3818-1	MCR3918-1		2N2573	2N681
	50 V	2N5164	2N5168		MCR649P2	MCR3818-2	MCR3918-2	2N6504	2N2574	2N682
	100 V			2N6167	MCR649P3	MCR3818-3	MCR3918-3	2N6505	2N2575	2N683
	200 V	2N5165	2N5169	2N6168	MCR649P4	MCR3818-4	MCR3918-4	2N6506	2N2576	2N685
	300 V				MCR649P5	MCR3818-5	MCR3918-5		2N2577	2N687
	400 V	2N5166	2N5170	2N6169	MCR649P6	MCR3818-6	MCR3918-6	2N6507	2N2578	2N688
	500 V				MCR649P7	MCR3818-7	MCR3918-7		2N2579	2N689
	600 V	2N5167	2N5171	2N6170	MCR649P8	MCR3818-8	MCR3918-8	2N6508	MCR649A8	2N690
	700 V				MCR649P9	MCR3818-9	MCR3918-9		MCR649A9	2N691
	800 V				MCR649P10	MCR3818-10	MCR3918-10	2N6509	MCR649A10	2N692
MAXIMUM ELECTRICAL CHARACTERISTICS	I_{TSM} (Amps)	240			260	240	240	300	260	200
	@ 25°C I_{GT} (mA)	@ −40°C 75			80	40	40	40	40	25
	@ 25°C V_{GT} (V)	@ −40°C 2.5			3.5	1.5	1.5	1.5	3.5	3.0
	@ 25°C I_H (mA)	@ −40°C 90			20 Typ	50	50	40	20 Typ	20 Typ

RADAR MODULATORS

ON-STATE (RMS) CURRENT						ON-STATE PULSE CURRENT				
35 AMPS			55 AMPS			100 AMPS		1000 AMPS		
		 Isolated			 Isolated					
Case 174-03 Style 1	Case 175-02 Style 1	Case 311-01 Style 1	Case 310-01 Style 1	Case 263-03 Style 1	Case 311-01 Style 1	Case 63-03 TO-64 Style 1		Case 263-03 Style 1		
MCR3835-1	MCR3935-1		MCR63-1	MCR64-1	MCR65-1				25 V	V_{DRM}
MCR3835-2	MCR3935-2		MCR63-2	MCR64-2	MCR65-2				50 V	
2N3870	2N3896	2N6171	MCR63-3	MCR64-3	MCR65-3				100 V	
2N3871	2N3897	2N6172	MCR63-4	MCR64-4	MCR65-4				200 V	
MCR3835-5	MCR3935-5		MCR63-5	MCR64-5	MCR65-5	2N4199 2N4199 JAN	MCR729-5	MCR1718-5	300 V	
2N3872	2N3898	2N6173	MCR63-6	MCR64-6	MCR65-6	2N4200 2N4200 JAN	MCR729-6	MCR1718-6	400 V	
MCR3835-7	MCR3935-7		MCR63-7	MCR64-7	MCR65-7	2N4201 2N4201 JAN	MCR729-7	MCR1718-7	500 V	
2N3873 MCR3835-8	2N3899 MCR3935-8	2N6174	MCR63-8	MCR64-8	MCR65-8	2N4202 2N4202 JAN	MCR729-8	MCR1718-8	600 V	
MCR3835-9	MCR3935-9		MCR63-9	MCR64-9	MCR65-9	2N4203 2N4203 JAN	MCR729-9		700 V	
MCR3835-10	MCR3935-10		MCR63-10	MCR64-10	MCR65-10	2N4204 2N4204 JAN	MCR729-10		800 V	
350	350	350	550	550	550	100*	100*	1000*	I_{TSM} (Amps)	MAXIMUM ELECTRICAL CHARACTERISTICS
40	40	40	40	40	40	50	50	50	I_{GT} (mA)	
1.6	1.6	1.6	3.0	3.0	3.0	1.5	1.5	1.5	V_{GT} (V)	
50	50	50	60	60	60	@ 105°C 3.0 Min	3.0 Min	5.0 Min	I_H (mA)	

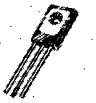
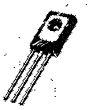
*Indicates pulse rating

5

TRIACs

. . . Metal or Plastic Packages
. . . 0.8 to 40 Amperes
. . . 25 to 800 Volts
. . . Industry Standards, with a variety of Custom Specifications and Leadforms available.

MAY MOTOROLA SUPPLY YOUR TRIAC?

		ON-STATE (RMS) CURRENT								
		0.6 AMP		2.5 AMPS			3.0 AMPS	4.0 AMPS		
				 Note Center Gate Pin Out						
		Case 29-02 TO-92 Style 12		Case 77-03 Style 7				Case 77-03 Style 5		
V_{DRM}	25 V	MAC92-1	MAC92A1					2N6068	2N6068A	2N6068B
	50 V	MAC92-2	MAC92A2	T2300PF	T2301PF	T2302PF		2N6069	2N6069A	2N6069B
	100 V	MAC92-3	MAC92A3	T2300PA	T2301PA	T2302PA	SC136A	2N6070	2N6070A	2N6070B
	200 V	MAC92-4	MAC92A4	T2300PB	T2301PB	T2302PB	SC136B	2N6071	2N6071A	2N6071B
	300 V	MAC92-5	MAC92A5	T2300PC	T2301PC	T2302PC	SC136C	2N6072	2N6072A	2N6072B
	400 V	MAC92-6	MAC92A6	T2300PD	T2301PD	T2302PD	SC136D	2N6073	2N6073A	2N6073B
	500 V	MAC92-7	MAC92A7	T2300PE	T2301PE	T2302PE	SC136E	2N6074	2N6074A	2N6074B
	600 V	MAC92-8	MAC92A8	T2300PM	T2301PM	T2302PM	SC136M	2N6075	2N6075A	2N6075B
	700 V									
	800 V									
MAXIMUM ELECTRICAL CHARACTERISTICS	I_{TSM} (Amps)	8	8	25	25	25	30	30	30	30
	I_{GT} @ 25°C (MA)									
	MT2(+)G(+)	5.0	3.0	3.0	4.0	10	25	30	5.0	3.0
	MT2(+)G(−)	5.0	3.0	3.0	4.0	10	25	—	5.0	3.0
	MT2(−)G(−)	5.0	3.0	3.0	4.0	10	25	30	5.0	3.0
	MT2(−)G(+)	—		3.0	4.0	10		—	10	5.0
	V_{GT} @ 25°C (V)							@ −40°C	@ −40°C	@ −40°C
	MT2(+)G(+)	2.0	2.0	2.2	2.2	2.2	2.0	2.5	2.5	2.5
	MT2(+)G(−)	2.0	2.0	2.2	2.2	2.2	2.0	—	2.5	2.5
	MT2(−)G(−)	2.0	2.0	2.2	2.2	2.2	2.0	2.5	2.5	2.5
	MT2(−)G(+)	—		2.2	2.2	2.2		—	2.5	2.5

ON-STATE (RMS) CURRENT

6.0 AMPS		8.0 AMPS	10 AMPS						12 AMPS			
												
Case 221-02 TO-220AB Style 2		Case 221-02 TO-220AB Style 2	Case 221-02 TO-220AB Style 2	Case 174-03 Style 3		Case 175-02 Style 3		Case 235-02 Style 2	Case 221-02 TO-220AB Style 2			
											25 V	V_{DRM}
		MAC220-2 MAC221-2									50 V	
T2500A	SC141A	MAC220-3 MAC221-3									100 V	
T2500B	SC141B	2N6342 2N6346	SC146B	2N5567	SC246B	2N5569	SC245B	T4121B	2N6342A	2N6346A	200 V	
T2500C	SC141C	MAC220-5 MAC221-5	SC146C		SC246C		SC245C	T4121C			300 V	
T2500D	SC141D	2N6343 2N6347	SC146D	2N5568	SC246D	2N5570	SC245D	T4121D	2N6343A	2N6347A	400 V	
T2500E	SC141E	MAC220-7 MAC221-7	SC146E		SC246E		SC245E	T4121E			500 V	
T2500M	SC141M	2N6344 2N6348	SC146M		SC246M		SC245M	T4121M	2N6344A	2N6348A	600 V	
T2500S	SC141S	MAC220-9 MAC221-9	SC146S		SC246S		SC245S	T4121S			700 V	
T2500N	SC141N	2N6345 2N6349	SC146N		SC246N		SC245N	T4121N	2N6345A	2N6349A	800 V	
60	80	100	120	100	100	100	100	100	120	120	I_{TSM} (Amps)	MAXIMUM ELECTRICAL CHARACTERISTICS
25	50	50	50	25	50	25	50	25	50	50	I_{GT} @25°C (MA) MT2(+)G(+)	
60	50	75#	50	40	50	40	50	40	—	75	MT2(+)G(−)	
25	50	50	50	25	50	25	50	25	50	50	MT2(−)G(−)	
60		75#		40	—	40	—	40	—	75	MT2(−)G(+)	
2.5	2.5	2.0	2.5	2.5	2.5	2.5	2.5	2.5	2.0	2.0	V_{GT} @ 25°C (V) MT2(+)G(+)	
2.5	2.5	2.5#	2.5	2.5	2.5	2.5	2.5	2.5	—	2.5	MT2(+)G(−)	
2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.0	2.0	MT2(−)G(−)	
2.5		2.5#		2.5	—	2.5	—	2.5	—	2.5	MT2(−)G(+)	

#Denotes 2N6346-49 and MAC221 Series only.

TRIACs (continued)

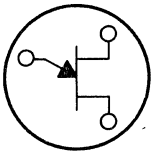
		ON-STATE (RMS) CURRENT											
		15 AMPS										25 AMPS	
													
		Case 174-03 Style 3		Case 175-02 Style 3		Case 311-01 Style 2		Case 221-02 TO-220AB Style 2		Case 326-01 Style 2		Case 326-01 Style 2	
V_{DRM}	25 V												
	50 V												
	100 V												
	200 V	2N5571	SC251B	2N5573	SC250B	2N6145	T4120B	MAC15-4	MAC15A4	MAC20-4	MAC20A4	MAC25-4	MAC25A4
	300 V		SC251C		SC250C		T4120C	MAC15-5	MAC15A5	MAC20-5	MAC20A5	MAC25-5	MAC25A5
	400 V	2N5572	SC251D	2N5574	SC250D	2N6146	T4120D	MAC15-6	MAC15A6	MAC20-6	MAC20A6	MAC25-6	MAC25A6
	500 V		SC251E		SC250E		T4120E	MAC15-7	MAC15A7	MAC20-7	MAC20A7	MAC25-7	MAC25A7
	600 V		SC251M		SC250M	2N6147	T4120M	MAC15-8	MAC15A8	MAC20-8	MAC20A8	MAC25-8	MAC25A8
	700 V		SC251S		SC250S		T4120S	MAC15-9	MAC15A9	MAC20-9	MAC20A9	MAC25-9	MAC25A9
	800 V		SC251N		SC250N		T4120N	MAC15-10	MAC15A10	MAC20-10	MAC20A10	MAC25-10	MAC25A10
MAXIMUM ELECTRICAL CHARACTERISTICS	I_{TSM} (Amps)	100	100	100	100	100	100	150	150	150	150	250	250
	I_{GT} @ 25°C (MA)												
	MT2(+)G(+)	50	50	50	50	50	50	50	50	50	50	70	70
	MT2(+)G(−)	80	50	80	50	80	80	—	75	50	50	70	70
	MT2(−)G(−)	50	50	50	50	50	50	50	50	50	50	70	70
	MT2(−)G(+)	80	—	80	—	80	80	—	75		75	—	100
	V_{GT} @ 25°C (V)												
	MT2(+)G(+)	2.5	2.5	2.5	2.5	2.5	2.5	2.0	2.0	2.0	2.0	2.0	2.0
	MT2(+)G(−)	2.5	2.5	2.5	2.5	2.5	2.5	—	2.5	2.0	2.0	2.0	2.0
	MT2(−)G(−)	2.5	2.5	2.5	2.5	2.5	2.5	2.0	2.0	2.0	2.0	2.0	2.0
	MT2(−)G(+)	2.5	—	2.5	—	2.5	2.5	—	2.5	—	2.5	—	2.5

ON-STATE (RMS) CURRENT

30 AMPS						40 AMPS								
														
Case 263-03 Style 2		Case 311-01 Style 2		Case 310-01 Style 2		Case 310-01 Style 2		Case 263-03 Style 2		Case 311-01 Style 2	Case 326-01 Style 2			
													25 V	V_{DRM}
													50 V	
					T6401A								100 V	
2N6160	T6411B	2N6163	T6421B	2N6157	T6401B	2N5441	T6400B	2N5444	T6410B	T6420B	MAC50-4	MAC50A4	200 V	
	T6411C		T6421C		T6401C		T6400C		T6410C	T6420C	MAC50-5	MAC50A5	300 V	
2N6161	T6411D	2N6164	T6421D	2N6158	T6401D	2N5442	T6400D	2N5445	T6410D	T6420D	MAC50-6	MAC50A6	400 V	
	T6411E		T6421E		T6401E		T6400E		T6410E	T6420E	MAC50-7	MAC50A7	500 V	
2N6162	T6411M	2N6165	T6421M	2N6159	T6401M	2N5443	T6400M	2N5446	T6410M	T6420M	MAC50-8	MAC50A8	600 V	
	T6411S		T6421S		T6401S		T6400S		T6410S	T6420S	MAC50-9	MAC50A9	700 V	
	T6411N		T6421N		T6401N		T6400N		T6410N	T6420N	MAC50-10	MAC50A10	800 V	
250	300	250	300	250	300	300	300	300	300	300	300	300	I_{TSM} (Amps)	MAXIMUM ELECTRICAL CHARACTERISTICS
@ −65°C		@ −65°C		@ −65°C		@ −65°C		@ −65°C					I_{GT} @25°C(MA)	
200	50	200	50	200	50	125	50	125	50	50	70	70	MT2(+)G(+)	
250	80	250	80	250	80	240	80	240	80	80	70	70	MT2(+)G(−)	
200	50	200	50	200	50	125	50	125	50	50	70	70	MT2(−)G(−)	
250	80	250	80	250	80	240	80	240	80	80	—	100	MT2(−)G(+)	
@ −65°C		@ −65°C		@ −65°C		@ −65°C		@ −65°C					V_{GT} @ 25°C (V)	
3.4	2.5	3.4	2.5	3.4	2.5	3.4	2.5	3.4	2.5	2.5	2.0	2.0	MT2(+)G(+)	
3.4	2.5	3.4	2.5	3.4	2.5	3.4	2.5	3.4	2.5	2.5	2.0	2.0	MT2(+)G(−)	
3.4	2.5	3.4	2.5	3.4	2.5	3.4	2.5	3.4	2.5	2.5	2.0	2.0	MT2(−)G(−)	
3.4	2.5	3.4	2.5	3.4	2.5	3.4	2.5	3.4	2.5	2.5	—	2.5	MT2(−)G(+)	

TRIGGER DEVICES

. . . Wide Range of Sensitivities
. . . Input Characteristics for Most Applications
. . . Industry Standards, with a variety of Custom Specifications available.



UJT

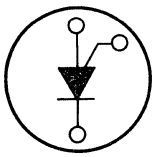
UNIJUNCTION TRANSISTORS — UJT

Highly stable devices for general-purpose trigger applications and as pulse generators (oscillators) and timing circuits. Useful at frequencies ranging (generally) from 1 Hz to 1 MHz. Available in low-cost plastic package (TO-92) and in hermetically sealed metal package (Case 22A).

UNIJUNCTION TRANSISTORS — (UJT)

Package	Device Type	η Min	η Max	I_P μA Max	I_{EB20} μA Max	I_V mA Min
	MU10	0.50	0.85	5.0	1.0	1.0
Plastic	2N4870	0.56	0.75	5.0	1.0	2.0
Case 29-02	2N4871	0.70	0.85	5.0	1.0	4.0
(TO-92)	MU2646	0.56	0.75	5.0	12	4.0
	MU4891	0.55	0.82	5.0	0.01	2.0
	MU4892	0.51	0.69	2.0	0.01	2.0
	MU4893	0.55	0.82	2.0	0.01	2.0
	MU4894	0.74	0.86	1.0	0.01	2.0
Metal	MU20	0.50	0.85	5.0	1.0	1.0
Case 22A-01	2N2646	0.56	0.75	5.0	12	4.0
	2N2647	0.68	0.82	2.0	0.2	8.0
	2N3980	0.68	0.82	2.0	0.01	1.0
	2N4851	0.56	0.75	2.0	0.1	2.0
	2N4852	0.70	0.85	2.0	0.1	4.0
	2N4853	0.70	0.85	0.4	0.05	6.0
	2N4948*	0.55	0.82	2.0	0.01	2.0
	2N4949*	0.74	0.86	1.0	0.01	2.0
	2N5431*	0.72	0.80	0.4	0.01	2.0

*Also available as JAN and JANTX devices.



PUT

PROGRAMMABLE UNIJUNCTION TRANSISTORS — PUT

Similar to UJTs, except that I_V, I_P and intrinsic standoff voltage are programmable (adjustable) by means of external voltage divider. This stabilizes circuit performance for variations in device parameters. General operating frequency range is from 0.01 Hz to 10 kHz, making them suitable for long-duration timer circuits. Two-package availability provides cost option.

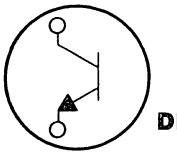
PROGRAMMABLE UNIJUNCTION TRANSISTORS — (PUT)

Package	Device Type	I_P R_G = 10 kΩ μA Max	I_P R_G = 1.0 MΩ μA Max	I_{GAO} @ 40V nA Max	I_V R_G = 10 kΩ μA Min	I_V R_G = 1.0 MΩ μA Max
Plastic	2N6027	5.0	2.0	10	70	50
Case 29-02	2N6028	1.0	0.15	10	25	25
TO-92	MPU6027	5.0	2.0	10	70	50
	MPU6028	1.0	0.15	10	25	25
	MPU131	5.0	2.0	5.0	70	50
	MPU132	2.0	0.3	5.0	50	50
	MPU133	1.0	0.15	5.0	50	25
Metal	2N6116*	5.0	2.0	5.0	70	50
Case 22-03	2N6117*	2.0	0.3	5.0	50	50
TO-18	2N6118*	1.0	0.15	5.0	50	25

*Also available as JAN and JANTX devices.

BILATERAL TRIGGERS — (DIACs)

Package	Device Type	Vs Volts	Is μA Max
Plastic Case 181-02 TO-92 	1N5758/MPT20	20 ± 4.0	100
	1N5759/MPT24	24 ± 4.0	100
	1N5760/MPT28	28 ± 4.0	100
	1N5761/MPT32	32 ± 4.0	100
	1N5762	36 ± 4.0	100
	1N5758A	20 ± 2.0	25
	1N5759A	24 ± 2.0	25
	1N5760A	28 ± 2.0	25
	1N5761A	32 ± 2.0	25
	1N5762A	36 ± 2.0	25



DIACs

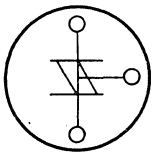
BILATERAL TRIGGERS — DIACs

Specifically designed as low-cost bidirectional triggers in line-operated Triac control circuits such as light dimmers, motor controls, and temperature controls.

5

SILICON BIDIRECTIONAL SWITCH — (SBS)

Package	Device Type	Vs Volts Min	Vs Volts Max	Is μA Max	IH mA Max
Plastic Case 29-02 TO-92 	MBS4991	6.0	10	500	1.5
	MBS4992	7.5	9.0	120	0.5



SBS

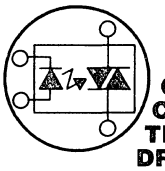
SILICON BIDIRECTIONAL SWITCH — SBS

Applications similar to DIAC, but has gate electrode that permits synchronization.

OPTICALLY COUPLED TRIAC DRIVER

Package	Device Type	Isolation Voltage Volts (Min)	Typ LED Trigger Current IFT (mA)	Peak Blocking Voltage (Volts)
8-Pin Plastic Dip 	MOC3010*	7500	8	250
	MOC3011*	7500	5	250

**Underwriters' Laboratories Recognition. File No. E54915.*



OPTICALLY COUPLED TRIAC DRIVER

OPTICALLY COUPLED TRIAC DRIVER

An infrared LED and a bidirectional photodetector in one 7500V isolated plastic DIP allows safe, economical triggering of Triacs and SCRs from logic sources as low as 3 Volts, 10 mA.

Thyristor Cross Reference 6

THYRISTOR CROSS REFERENCE

Devices are generally not shown in the following list if the Motorola number is identical. Refer to Chapter 1, the Alphanumeric Index, for the location of specifications.

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT	PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT	PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
2N876		MCR202	2N1878		MCR1906-3	2N3002		MCR203
2N877		MCR202	2N1878A		MCR1906-3	2N3003		MCR204
2N878		MCR203	2N1879		MCR1906-4	2N3004		MCR206
2N879		MCR204	2N1879A		MCR1906-4	2N3005		MCR202
2N880		MCR205	2N1880		MCR1906-4	2N3006		MCR203
2N881		MCR206	2N1880A		MCR1906-4	2N3007		MCR204
2N884		MCR202	2N1881		MCR1906-1	2N3008		MCR206
2N885		MCR202	2N1882		MCR1906-2	2N3027		MCR202
2N886		MCR203	2N1883		MCR1906-3	2N3028		MCR203
2N887		MCR204	2N1884		MCR1906-4	2N3029		MCR204
2N888		MCR205	2N1885		MCR1906-4	2N3030		MCR202
2N889		MCR206	2N2009		2N4212	2N3031		MCR203
2N948		MCR202	2N2010		2N4213	2N3032		MCR204
2N949		MCR203	2N2011		2N4214	2N3228		2N4170
2N950		MCR204	2N2012		2N4216	2N3254		MCR202
2N951		MCR206	2N2160		2N4853	2N3255		MCR202
2N1600		2N4168	2N2344		MCR1906-1	2N3256		MCR203
2N1601		2N4169	2N2345		MCR1906-2	2N3257		MCR202
2N1602		2N4170	2N2346		MCR1906-3	2N3258		MCR202
2N1603		2N4171	2N2347		MCR1906-4	2N3259		MCR203
2N1604		2N4172	2N2348		MCR1906-4	2N3269		2N4169
2N1671		2N4851	2N2417		2N4852	2N3270		2N4170
2N1671A		2N4851	2N2417A		2N4852	2N3271		2N4171
2N1671B		2N4851	2N2418		2N4852	2N3272		2N4172
2N1671C		2N4851	2N2418A		2N4852	2N3480		2N2646
2N1770		2N4167	2N2419		2N4846	2N3481		2N4852
2N1771		2N4168	2N2419A		2N4846	2N3483		2N2646
2N1772		2N4169	2N2419B		2N4846	2N3484		2N4852
2N1773		2N4170	2N2420		2N4846	2N3525		2N4171
2N1774		2N4170	2N2420A		2N4846	2N3528		2N4186
2N1775		2N4171	2N2420B		2N4846	2N3529		2N4188
2N1776		2N4171	2N2421		2N4846	2N3555		2N4212
2N1776B		2N4171	2N2421A		2N4846	2N3556		2N4213
2N1777		2N4172	2N2421B		2N4846	2N3557		2N4214
2N1778		2N4173	2N2422		2N4846	2N3558		2N4216
2N1869		2N4212	2N2422A		2N4846	2N3559		2N4212
2N1869A		MCR1906-1	2N2422B		2N4846	2N3560		2N4213
2N1870		2N4212	2N2619		2N4174	2N3561		2N4214
2N1870A		MCR1906-1	2N2653		2N4172	2N3562		2N4216
2N1871		2N4213	2N2679		MCR202	2N3568		MCR649P-3
2N1871A		MCR1906-2	2N2680		MCR203	2N3569		MCR649P-4
2N1872		2N4214	2N2681		MCR204	2N3570		MCR649P-6
2N1872A		MCR1906-3	2N2682		MCR206	2N3936		2N4169
2N1873		2N4215	2N2683		MCR202	2N3937		2N4170
2N1873A		MCR1906-4	2N2684		MCR203	2N3938		2N4171
2N1874		2N4216	2N2685		MCR204	2N3939		2N4172
2N1874A		MCR1906-4	2N2686		MCR206	2N3940		2N4173
2N1875		MCR1906-1	2N2687		MCR202	2N4096		MCR203
2N1875A		MCR1906-1	2N2688		MCR203	2N4097		MCR204
2N1876		MCR1906-1	2N2689		MCR204	2N4098		MCR206
2N1876A		MCR1906-1	2N2690		MCR206	2N4101		2N4174
2N1877		MCR1906-2	2N2840		2N5431	2N4102		2N4190
2N1877A		MCR1906-2	2N3001		MCR202	2N4108		MCR203

THYRISTOR CROSS REFERENCE (continued)

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
2N4109		MCR204
2N4110		MCR206
2N4144		MCR201
2N4145		MCR201
2N4146		MCR202
2N4147		MCR203
2N4148		MCR204
2N4149		MCR206
2N4316		MCR3918-3
2N4317		2N5169
2N4318		MCR3918-5
2N4319		2N5170
2N4332		MCR202
2N4333		MCR203
2N4334		MCR204
2N4335		MCR205
2N4336		MCR206
2N4891		MU4891
2N4892		MU4892
2N4893		MU4893
2N4894		MU4894
2N4897		2N4851
2N4898		2N4852
2N4899		2N4853
2N4991		MBS4991
2N4992		MBS4992
2N5204		2N3899
2N5273		2N6160
2N5274		2N6161
2N5719		MCR203
2N5720		MCR204
2N5721		MCR206
2N5724		MCR203
2N5725		MCR204
2N5726		MCR206
2N5754		2N6070
2N5755		2N6071
2N5756		2N6073
2N5757		2N6075
2N5787		2N5060
2N5788		2N5061
2N5789		2N5062
2N5790		2N5064
2N5806		2N6160
2N5807		2N6161
2N5808		2N6162
2N5809		2N6162
2N6119		2N6116
2N6120		2N6118
2N6137		2N6116
2N6138		2N6116
C5A	2N2324	
C5B	2N2326	
C5F	2N2323	
C5G	2N2325	
C5U	2N2322	
C6A		MCR1906-3
C6B		MCR1906-4
C6F		MCR1906-2
C6G		MCR1906-4
C6U		MCR1906-1
C7A		MCR1906-3
C7B		MCR1906-4
C7G		MCR1906-4
C7U		MCR1906-1
C11A		2N4169
C11B		2N4170
C11C		2N4171
C11D		2N4172
C11E		2N4173
C11F		2N4168
C11G		2N4170
C11H		2N4171
C11M		2N4174
C11U		2N4167
C15A		2N4169
C15B		2N4170
C15C		2N4171
C15D		2N4172
C15F		2N4168
C15G		2N4170
C15H		2N4171
C15M		2N4174
C20A		2N4169
C20B		2N4170
C20C		2N4171
C20D		2N4172
C20F		2N4168
C20U		2N4167
C30A		2N683
C30B		2N685
C30C		2N687
C30D		2N688
C30F		2N682
C30U		2N681
C31A		2N683
C31B		2N685
C31C		2N687
C31D		2N688
C31F		2N682
C31U		2N681
C32A		2N683
C32B		2N685
C32C		2N687
C32D		2N688
C32F		2N682
C32U		2N681
C33A		MCR3818-3
C33B		2N5165
C33C		MCR3818-5
C33D		2N5166
C33F		2N5164
C33U		MCR3818-1
C35 SERIES	NOTE 1	
C36A	2N1844	
C36B	2N1846	
C36C	2N1848	
C36D	2N1849	
C36E	2N1850	
C36F		2N1843
C36G	2N1845	
C36H	2N1847	
C36U		2N1842
C37A		MCR3918-3
C37B		2N5169
C37C		MCR3918-5
C37D		2N5170
C37E		MCR3918-7
C37F		2N5168
C37G		2N5169
C37H		MCR3918-5
C37M		2N5171
C37U		MCR3918-1
C38A		2N3896
C38B		2N3897
C38C		MCR3935-5
C38D		2N3898
C38E		MCR3935-7
C38F		MCR3935-2
C38G		2N3897
C38H		MCR3935-5
C38U		MCR3935-1
C103A		2N5062
C103B		2N5064
C103Y		2N5060
C103YY		2N5061
C106 SERIES	NOTE 1	
C107A	C106A	2N6238
C107B	C106B	2N6239
C107C	C106C	2N6240
C107D	C106D	2N6240
C107E	C106E	2N6241
C107F	C106F	2N6237
C107M	C106M	2N6241
C107Q	C106Q	2N6236
C107Y	C106Y	2N6236
C122A	C122A1	
C122A SERIES	NOTE 1	
C122B	C122B1	
C122B SERIES	NOTE 1	
C122C	C122C1	
C122C SERIES	NOTE 1	
C122D	C122D1	
C122D SERIES	NOTE 1	
C122E	C122E1	
C122E SERIES	NOTE 1	
C122F	C122F1	
C122F SERIES	NOTE 1	
C135A		2N3896
C135B		2N3897
C135C		MCR3935-5
C135D		2N3898
C135E		MCR3935-7
C135F		MCR3935-2
C135M		2N3899
C137E		MCR3935-7
C137M		2N3899
C228A SERIES	NOTE 1	
C229A SERIES	NOTE 1	
D5K1	2N6114	
D5K2	2N6115	
D13T1	MPU6027	
D13T2	MPU6028	
D13Q500		MBS4991
D30		1N5762
EC103A	MCR104	
EC103B	MCR120	
EC103Y	MCR102	
MAC10-4	2N6151	
MAC10-6	2N6152	
MAC10-8	2N6153	
MAC11-4	2N6154	
MAC11-6	2N6155	
MAC11-8	2N6156	
MAC35-1	2N6157	
MAC35-2	2N6157	
MAC35-3	2N6157	
MAC35-4	2N6157	
MAC35-5	2N6158	
MAC35-6	2N6158	
MAC35-7	2N6159	

DEVICES NOT SHOWN IF MOTOROLA NUMBER IS IDENTICAL, REFER TO CHAPTER 1.

NOTE 1 MOTOROLA DEVICE NUMBERS IDENTICAL

THYRISTOR CROSS REFERENCE (continued)

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
MAC35-8	2N6159	
MAC36-1	2N6160	
MAC36-2	2N6160	
MAC36-3	2N6160	
MAC36-4	2N6160	
MAC36-5	2N6161	
MAC36-6	2N6161	
MAC36-7	2N6162	
MAC36-8	2N6162	
MAC37-1		2N6157
MAC37-2		2N6157
MAC37-3		2N6157
MAC37-4		2N6157
MAC37-5		2N6158
MAC37-6		2N6158
MAC37-7		2N6159
MAC37-8		2N6159
MAC38-1		2N6160
MAC38-2		2N6160
MAC38-3		2N6160
MAC38-4		2N6160
MAC38-5		2N6161
MAC38-6		2N6161
MAC38-7		2N6162
MAC38-8		2N6162
MAC77-1	2N6068	
MAC77-2	2N6069	
MAC77-3	2N6070	
MAC77-4	2N6071	
MAC77-5	2N6072	
MAC77-6	2N6073	
MAC77-7	2N6074	
MAC77-8	2N6075	
MAC5571	2N5571	
MAC5572	2N5572	
MAC5573	2N5573	
MAC5574	2N5574	
MAC40802		2N6145
MAC40803		2N6146
MAC40804	2N6147	
MCR106-1	2N6236	
MCR106-2	2N6237	
MCR106-3	2N6238	
MCR106-4	2N6239	
MCR106-5	2N6240	
MCR106-6	2N6240	
MCR106-7	2N6241	
MCR106-8	2N6241	
MCR306-1	2N6236	
MCR306-2	2N6237	
MCR306-3	2N6238	
MCR306-4	2N6239	
MCR306-5	2N6240	
MCR306-6	2N6240	
MCR600-1		MCR102
MCR600-2		MCR103
MCR600-3		MCR104
MCR600-3.5		MCR115
MCR600-4		MCR120
MCR808-1		MCR3818-1
MCR808-2		2N5164
MCR808-3		MCR3818-3
MCR808-4		2N5165
MCR808-5		MCR3818-5
MCR808-6		2N5166
MCR808-7		MCR3818-7
MCR808-8		2N5167
MCR808-9		MCR3818-9
MCR808-10		2N2647-10
MCR808R2		2N5164
MCR808R4		2N5165
MCR808R6		2N5166
MCR808R8		2N5167
MCR1305R2		2N5168
MCR1305R4		2N5169
MCR1305R6		2N5170
MCR1305R8		2N5171
MCR1308-1	MCR3918-1	
MCR1308-2		2N5168
MCR1308-3	MCR3918-3	
MCR1308-4		2N5169
MCR1308-5	MCR3918-5	
MCR1308-6		2N5170
MCR1308-7	MCR3918-7	
MCR1308-8		2N5170
MCR1308-9	MCR3918-9	
MCR1308R2		2N5168
MCR1308R4		2N5169
MCR1308R6		2N5170
MCR1308R8		2N5171
MCR1604-1		2N4183
MCR1604-2		2N4184
MCR1604-3		2N4185
MCR1604-4		2N4186
MCR1604-5		2N4187
MCR1604-6		2N4188
MCR1604-7		2N4189
MCR1604-8		2N4190
MCR2305-1		2N4167
MCR2305-2		2N4168
MCR2305-3		2N4169
MCR2305-4		2N4170
MCR2305-5		2N4171
MCR2305-6		2N4172
MCR2305-7		2N4173
MCR2305-8		2N4174
MCR2315-1	2N4167	
MCR2315-2	2N4168	
MCR2315-3	2N4169	
MCR2315-4	2N4170	
MCR2315-5	2N4171	
MCR2315-6	2N4172	
MCR2315-7	2N4173	
MCR2315-8	2N4174	
MCR2604-1		2N4183
MCR2604-2		2N4184
MCR2604-3		2N4185
MCR2604-5		2N4187
MCR2604-6		2N4188
MCR2604-7		2N4189
MCR2604-8		2N4186
MCR2604-8		2N4190
MCR2604L1	2N4183	
MCR2604L2	2N4184	
MCR2604L3	2N4185	
MCR2604L4	2N4186	
MCR2604L5	2N4187	
MCR2604L6	2N4188	
MCR2604L7	2N4189	
MCR2604L8	2N4190	
MCR2818-1	MCR3818-1	
MCR2818-2		2N5164
MCR2818-3	MCR3818-3	
MCR2818-4		2N5165
MCR2818-5	MCR3818-5	
MCR2818-6		2N5166
MCR2818-7	MCR3818-7	
MCR2818-8		2N5167
MCR2818R2		2N5164
MCR2818R4		2N5165
MCR2818R6		2N5166
MCR2818R8		2N5167
MCR2835-1	MCR3835-1	
MCR2835-2	MCR3835-2	
MCR2835-3		2N3870
MCR2835-4		2N3871
MCR2835-5	MCR3835-5	
MCR2835-6		2N3872
MCR2835-7	MCR3835-7	
MCR2835-8		2N3873
MCR2918-1	MCR3918-1	
MCR2918-2		2N5168
MCR2918-3	MCR3918-3	
MCR2918-4		2N5169
MCR2918-5	MCR3918-5	
MCR2918-6		2N5170
MCR2918-7	MCR3918-7	
MCR2918-8		2N5171
MCR2918R2		2N5168
-4R2918R4		2N5169
MCR2918R6		2N5170
MCR2918R8		2N5171
MCR2935-1	MCR3935-1	
MCR2935-2	MCR3935-2	
MCR2935-3	2N3896	
MCR2935-4	2N3897	
MCR2935-5	MCR3935-5	
MCR2935-6	2N3898	
MCR2935-7	MCR3935-7	
MCR2935-8	2N3899	
MCR3000-1C	MCR3000-1	
MCR3000-2	2N4441	
MCR3000-3C	MCR3000-3	
MCR3000-4	2N4442	
MCR3000-5C	MCR3000-5	
MCR3000-6	2N4443	
MCR3000-7C	MCR3000-7	
MCR3000-8	2N4444	
MCR3000-9C	MCR3000-9	
MCR3000-10C	MCR3000-10	
MCR3818,R-2		2N5164
MCR3818,R-4		2N5165
MCR3818,R-6		2N5166
MCR3818,R-8		2N5167
MCR3835-3	2N3870	
MCR3835-4	2N3871	
MCR3835-6	2N3872	
MCR3835-8	2N3873	
MCR3918,R-2		2N5168
MCR3918,R-4		2N5169
MCR3918,R-6		2N5170
MCR3918,R-8		2N5171
MCR3935-3	2N3896	
MCR3935-4	2N3897	
MCR3935-6	2N3898	
MCR3935-8	2N3899	
MCR4018-3		2N6167
MCR4018-4		2N6168
MCR4018-5		2N6169
MCR4018-6		2N6169
MCR4018-7		2N6170

DEVICES NOT SHOWN IF MOTOROLA NUMBER IS IDENTICAL,
REFER TO CHAPTER 1

THYRISTOR CROSS REFERENCE (continued)

PART NO.	MOTOROLA DIRECT REPLACEMENT	MOTOROLA SIMILAR REPLACEMENT
MCR4018-8		2N6170
MCR4035-3		2N6171
MCR4035-4		2N6172
MCR4035-5		2N6173
MCR4035-6		2N6173
MCR4035-7		2N6174
MCR4035-8		2N6174
MPT20		1N5758
MPT24		1N5759
MPT28		1N5760
MPT32		1N5761
MPT36		1N5762
MPU231		2N6116
MPU232		2N6117
MPU233		2N6118
MU970		2N2646
MU971		2N2647
Q200E3		MAC92-4
Q2010L4		2N6346A
Q2025G	MAC37-4	
Q2025H	MAC38-4	
Q2040D		MAC40688
Q4010L4		2N6347A
Q4025G	MAC37-6	
Q4025H	MAC38-6	
Q4040D		MAC40689
Q5010L4		MAC10-7
Q5025G	MAC37-7	
Q5025H	MAC38-7	
Q6010L4		2N6348A
Q6015G		MAC40797
Q6015H		MAC40798
Q6040D		MAC40690
S0301MS3		MCR1906-1
S0303LS2		MCR106-1
S0303LS3		MCR106-1
S0308L		MCR3000-1
S0325C		MCR649-1
S0325G		MCR3835-1
S0325H		MCR3935-1
S0335G	MCR3835-1	
S0335H	MCR3935-1	
S0501MS3		MCR1906-2
S0503LS2		MCR106-2
S0503LS3		MCR106-2
S0525C		MCR649-2
S0525G		MCR3835-2
S0525H	MCR3935-2	
S0535G	MCR3835-2	
S1001MS3		MCR1906-3
S1003LS2		MCR106-3
S1003LS3		MCR106-3
S1008L		MCR3000-3
S1025C		MCR649-3
S1025G		MCR3818-3
S1025H	MCR3896	
S1035G	MCR3870	
S2001MS3		MCR1906-4
S2003LS2		MCR106-4
S2003LS3		MCR106-4
S2025C		MCR649-4
S2025G		MCR3818-4
S2025H	MCR3897	
S2035G	MCR3871	
S2035H	MCR3897	
S2800A SERIES	NOTE 1	
S4006B		MCR729-6
S4008L		MCR3000-6
S4025C		MCR649-6
S4025G		2N3872
S4025H		2N3898
S4035G	2N3872	
S4035H	2N3898	
S5006B		MCR729-7
S5008L		MCR3000-7
S5025C		MCR649-7
S5025G		MCR3835-7
S5025H		MCR3935-7
S5035G	MCR3835-7	
S5035H	MCR3935-7	
S6006B		MCR729-8
S6025G		MCR3835-8
S6025H		2N3899
S6035G	2N3873	
S6035H	2N3899	
S6200A SERIES	NOTE 1	
S6210 SERIES	NOTE 1	
S6220A SERIES	NOTE 1	
SC141	NOTE 1	
SC141A SERIES	NOTE 1	
SC141A1	SC141A	
SC141B	SC141B1	
SC141B SERIES	NOTE 1	
SC141C	SC141C1	
SC141C SERIES	NOTE 1	
SC141D	SC141D1	
SC141D SERIES	NOTE 1	
SC141E	SC141E1	
SC141E SERIES	NOTE 1	
SC141M	SC141M1	
SC141M SERIES	NOTE 1	
SC146A	SC146A1	
SC146A SERIES	NOTE 1	
SC146B	SC146B1	
SC146B SERIES	NOTE 1	
SC146C	SC146C1	
SC146C SERIES	NOTE 1	
SC146D	SC146D1	
SC146D SERIES	NOTE 1	
SC146E	SC146E1	
SC146E SERIES	NOTE 1	
SC146M	SC146M1	
SC146M SERIES	NOTE 1	
SC245 SERIES	NOTE 1	
SC246 SERIES	NOTE 1	
SC250 SERIES	NOTE 1	
SC251 SERIES	NOTE 1	
SC260 SERIES	NOTE 1	
SC261 SERIES	NOTE 1	
S0303LS2		MCR106-1
S0503LS2		MCR106-2
S1003LS2		MCR106-3
S2003LS2		MCR106-4
S4003LS2		MCR106-6
S6003LS2		MCR106-8
T2300A		T2300PA5
T2300B		T2300PB5
T2300C		T2300PC5
T2300D		T2300PD5
T2300E		T2300PE5
T2300F		T2300PF5
T2300M		T2300PM5
T2301A		T2301PA5
T2301B		T2301PA5
T2301C		T2301PC5
T2301D		T2301PD5
T2301E		T2301PE5
T2301F		T2301PF5
T2301M		T2301PM5
T2302A		T2302PA5
T2302B		T2302PB5
T2302C		T2302PC5
T2302D		T2302PD5
T2302E		T2302PE5
T2302F		T2302PF5
T2302M		T2302PM5
T2500 SERIES	NOTE 1	
T2800 SERIES	NOTE 1	
T2801 SERIES	NOTE 1	
T2802 SERIES	NOTE 1	
T2850A		2N6346A
T2850B		2N6346A
T2850D		2N6347A
T4120 SERIES	NOTE 1	
T4121 SERIES	NOTE 1	
T6400 SERIES	NOTE 1	
T6401 SERIES	NOTE 1	
T6410 SERIES	NOTE 1	
T6411 SERIES	NOTE 1	
T6420 SERIES	NOTE 1	
T6421 SERIES	NOTE 1	

DEVICES NOT SHOWN IF MOTOROLA NUMBER IS IDENTICAL; REFER TO CHAPTER 1

NOTE 1: MOTOROLA DEVICE NUMBERS IDENTICAL

Thyristor Data Sheets 7

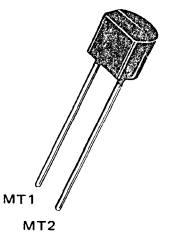
1N5758,A thru 1N5762,A

BIDIRECTIONAL DIODE THYRISTORS

. . . two-terminal 3-layer devices that exhibit bidirectional negative resistance switching characteristics. These economical, durable devices have been developed for use in thyristor triggering circuits for lamp drivers and universal motor speed controls.

- Switching Voltage Range — 20 to 36 Volts Nominal
- Symmetrical Characteristics
- Passivated Surface for Reliability and Uniformity

DIACS



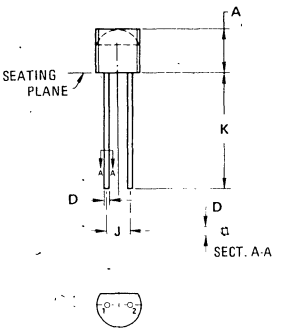
***MAXIMUM RATINGS** (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Pulse Current (30 μs duration, 120 Hz repetition rate)	I_{pulse}	2.0	Amp
Power Dissipation @ T_A = -40 to +25°C Derate above 25°C	P_D	300 4.0	mW mW/°C
Operating Junction Temperature Range	T_J	-40 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Switching Voltage (Both Directions)	1N5758	V_S	16	24	Volts
	1N5759		20	28	
	1N5760		24	32	
	1N5761		28	36	
	1N5762		32	40	
	1N5758A		18	22	
	1N5759A		22	26	
	1N5760A		26	30	
	1N5761A		30	34	
	1N5762A		34	38	
Switching Current (Both Directions)	1N5758/5762	I_S	–	100	μA
(T_A = -40 to +75°C)	1N5758A/5762A		–	25	
Switching Voltage Change (Both Directions)	1N5758,A,1N5759,A	ΔV	5.0	–	Volts
($\Delta I = I_S$ to I = 10 mA)	1N5760,A,61,A,62,A		7.0	–	
Leakage Current (Both Directions), (Applied Voltage = 14 Volts)		I_B	–	10	μA
Switching Voltage Symmetry	1N5758/5762	$(V_S+)-(V_S-)$	–	±4.0	Volts
	1N5758A/5762A		–	±2.0	
Peak Pulse Amplitude (Figure 1) (Both Polarities)	1N5758,A,1N5759,A		3.0	–	Volts
	1N5760,A,61,A,62,A		5.0	–	

*Indicates JEDEC Registered Data.



STYLE 3:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.45	4.70	0.175	0.185
D	0.41	0.48	0.016	0.019
J	2.29	2.79	0.090	0.110
K	12.70	–	0.500	–

CASE 182-03

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – PEAK PULSE AMPLITUDE TEST CIRCUIT

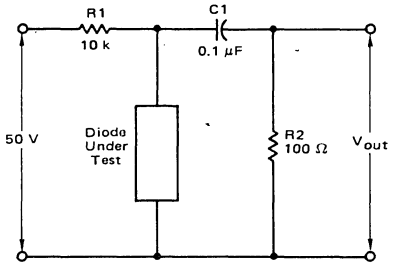


FIGURE 2 – VOLT-AMPERE CHARACTERISTICS

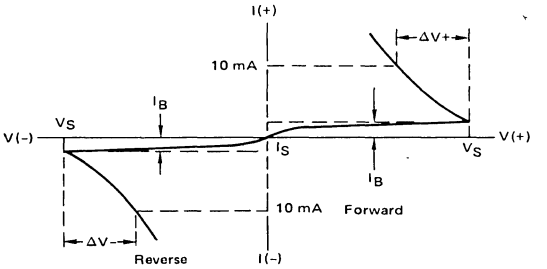


FIGURE 3 – BREAKOVER VOLTAGE BEHAVIOR

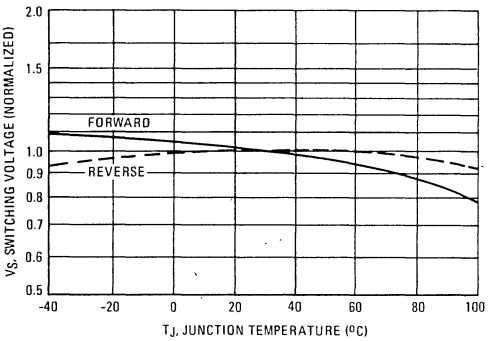


FIGURE 4 – NORMALIZED OUTPUT VOLTAGE BEHAVIOR

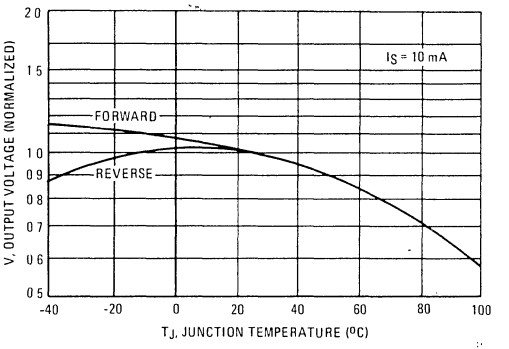


FIGURE 5 – SWITCHING TIMES

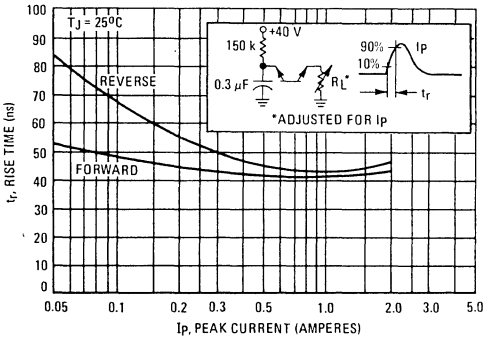
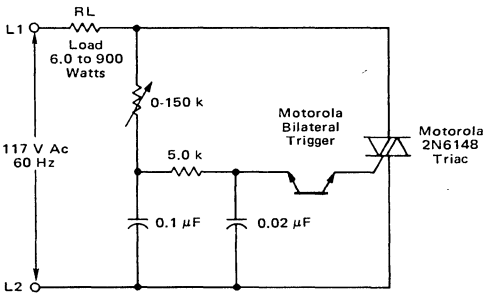


FIGURE 6 – CONTROL CIRCUIT



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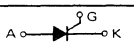
2N681 thru 2N692



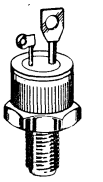
REVERSE BLOCKING TRIODE THYRISTORS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire for Greater Parameter Uniformity and Stability
- Blocking Voltage to 800 Volts

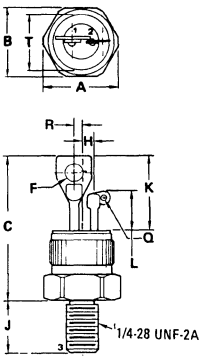
SILICON CONTROLLED RECTIFIER

25 AMPERES RMS
25-800 VOLTS



MAXIMUM RATINGS (T_J = 125°C unless otherwise noted.)

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Blocking Voltage (1)	V_{RRM} or V_{DRM}		Volts
2N681		25	
2N682		50	
2N683		100	
2N684		150	
2N685		200	
2N686		250	
2N687		300	
2N688		400	
2N689		500	
2N690		600	
2N691		700	
2N692		800	
*Peak Non-Repetitive Reverse Voltage	V_{RSM}		Volts
2N681		35	
2N682		75	
2N683		150	
2N684		225	
2N685		300	
2N686		350	
2N687		400	
2N688		500	
2N689		600	
2N690		720	
2N691		840	
2N692		960	
*RMS On-State Current (All Conduction Angles)	$I_{T(RMS)}$	25	Amp
*Average On-State Current (T_C = 65°C)	$I_{T(AV)}$	16	Amp
*Peak Non-Repetitive Surge Current (One cycle, 60 Hz, preceded and followed by rated current and voltage)	I_{TSM}	150	Amp
Circuit Fusing Considerations (T_J = -40 to +125°C, t = 1.0 to 8.3 ms)	I^2t	93	A^2s
*Peak Gate Power	P_{GM}	5.0	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current 2N681-2N689	I_{GM}	2.0	Amp
2N690-2N692		1.2	
*Peak Gate Voltage — Forward	V_{FGM}	10	Volts
Reverse	V_{RGM}	5.0	
*Operating Junction Temperature Range	T_J	-65 to +125	°C
*Storage Temperature Range	T_{stg}	-65 to +150	°C
Stud Torque	—	30	in.lb.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

STYLE 1:
PIN 1. CATHODE
2. GATE
3. ANODE

CASE 263-03

7

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Average Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open, T_J = 125°C)		$I_{D(AV)}$, $I_{R(AV)}$				mA
	2N681-2N684		–	–	6.5	
	2N685		–	–	6.0	
	2N686		–	–	5.5	
	2N687		–	–	5.0	
	2N688		–	–	4.0	
	2N689		–	–	3.0	
	2N690		–	–	2.5	
	2N691		–	–	2.25	
	2N692		–	–	2.0	
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM}, gate open, T_J = 125°C)		I_{DRM}, I_{RRM}	–	–	2.0	mA
*Peak On-State Voltage (I_{TM} = 50.3 A peak, Pulse Width ≤ 1.0 ms, Duty Cycle ≤ 2.0%)		V_{TM}	–	–	2.0	Volts
Gate Trigger Current, Continuous dc		I_{GT}				mA
(V_{AK} = 12 Vdc, R_L = 50 Ω)			–	–	40	
*(V_{AK} = 12 Vdc, R_L = 50 Ω, T_C = -65°C)			–	–	80	
Gate Trigger Voltage, Continuous dc		V_{GT}				Volts
(V_{AK} = 12 Vdc, R_L = 50 Ω)			–	0.65	2.0	
*(V_{AK} = 12 Vdc, R_L = 50 Ω, T_J = -65°C)			–	–	3.0	
*Gate Non-Trigger Voltage (Rated V_{DRM}, R_L = 50 Ω, T_J = 125°C)		V_{GD}	0.25	–	–	Volts
Holding Current (V_{AK} = 12 Vdc, Gate Open)		I_H	–	7.3	50	mA
Critical Rate of Rise of Off-State Voltage (Rated V_{DRM}, Exponential Waveform, T_J = 125°C, Gate Open)		dv/dt	–	30	–	V/μs

*Indicates JEDEC Registered Data.

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FIGURE 1 – AVERAGE CURRENT DERATING

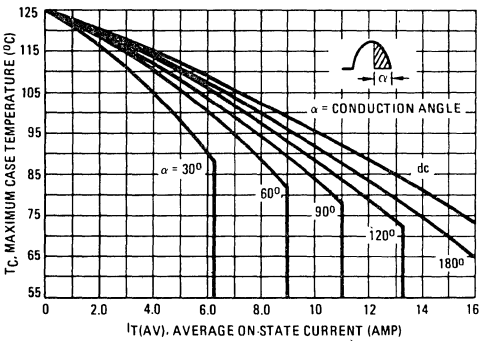

FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

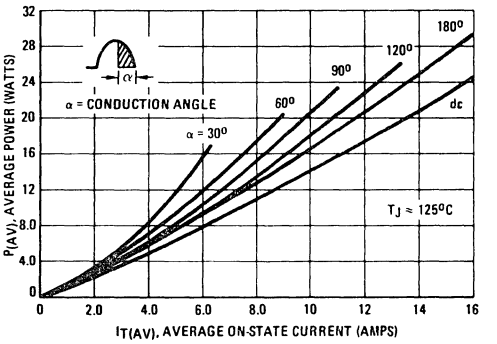

FIGURE 3 – ON-STATE CHARACTERISTICS

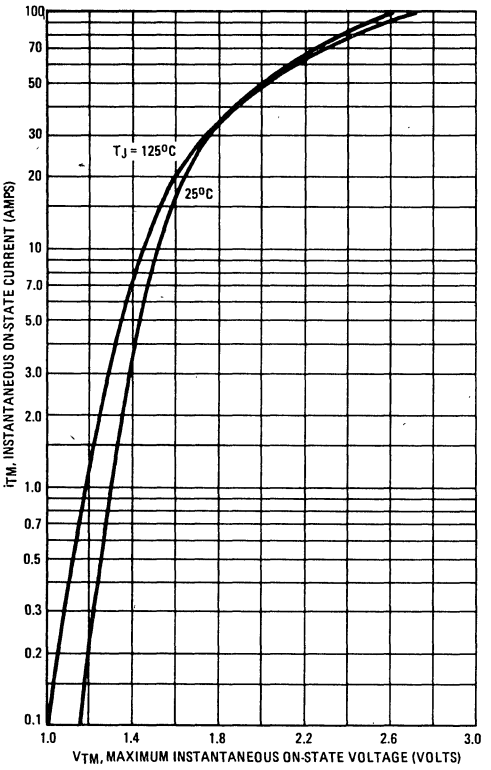

FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

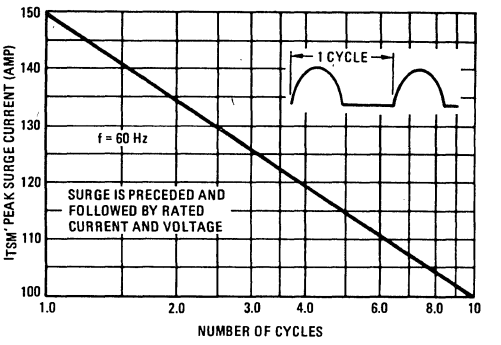

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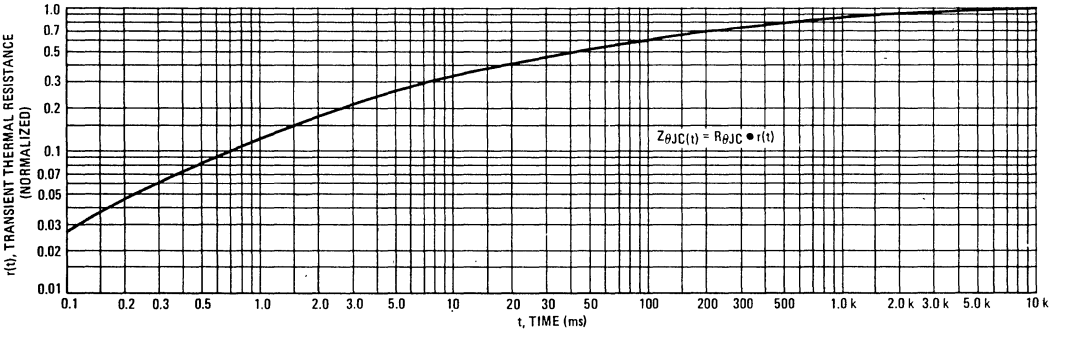
FIGURE 5 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS

FIGURE 6 – PULSE TRIGGER CURRENT

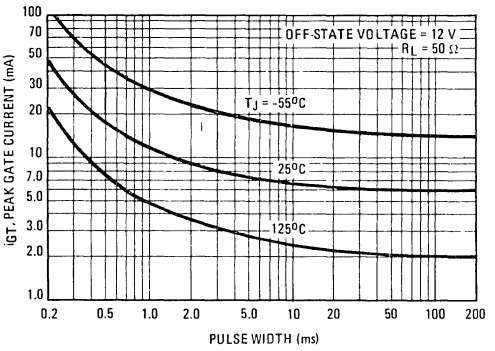


FIGURE 7 – GATE TRIGGER CURRENT

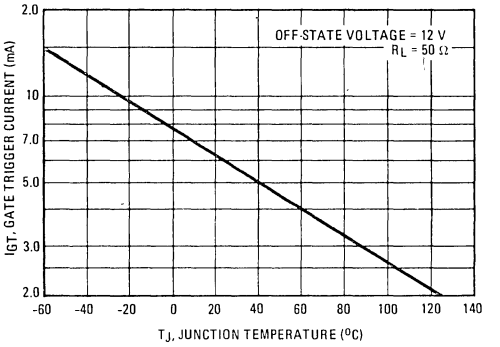


FIGURE 8 – GATE TRIGGER VOLTAGE

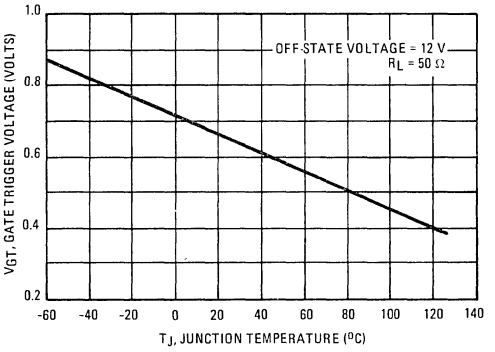
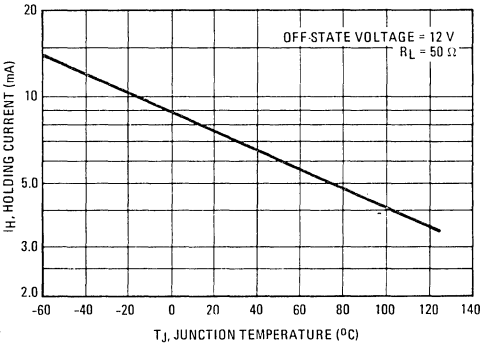
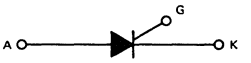


FIGURE 9 – HOLDING CURRENT



2N1595 thru 2N1599



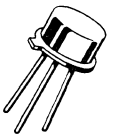
REVERSE BLOCKING TRIODE THYRISTORS

These devices are glassivated planar construction designed for gating operation in mA/μA signal or detection circuits.

- Low-Level Gate Characteristics – I_{GT} = 10 mA (Max) @ 25°C
- Low Holding Current – I_H = 5.0 mA (Typ) @ 25°C
- Glass-to-Metal Bond for Maximum Hermetic Seal

SILICON CONTROLLED RECTIFIERS

1.6 AMPERE RMS
50 thru 400 VOLTS

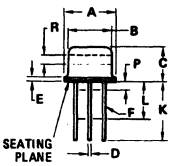


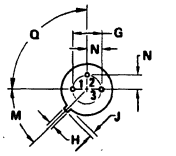
***MAXIMUM RATINGS** (T_J = 125°C unless otherwise noted, R_{GC} = 1 kΩ)

Rating	Symbol	Value	Unit
Repetitive Peak Reverse Blocking Voltage (1)	V_{RRM}		Volts
2N1595		50	
2N1596		100	
2N1597		200	
2N1598		300	
2N1599		400	
Repetitive Peak Forward Blocking Voltage (1)	V_{DRM}		Volts
2N1595		50	
2N1596		100	
2N1597		200	
2N1598		300	
2N1599		400	
RMS On-State Current (All Conduction Angles)	$I_{T(RMS)}$	1.6	Amps
Peak Non-Repetitive Surge Current (One Cycle, 60 Hz, T_J = -65 to +125°C)	I_{TSM}	15	Amps
Peak Gate Power	P_{GM}	0.1	Watt
Average Gate Power	$P_{G(AV)}$	0.01	Watt
Peak Gate Current	I_{GM}	0.1	Amp
Peak Gate Voltage – Forward	V_{GFM}	10	Volts
Reverse	V_{GRM}	10	
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

*Indicates JEDEC Registered Data.

(1) V_{DRM} or V_{RRM} for all types can be applied on a continuous DC basis without incurring damage.





STYLE 3:
PIN 1. CATHODE
2. GATE
3. ANODE (CONNECTED TO CASE)

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Reverse Blocking Current (V_R = Rated V_{RRM}, T_J = 125°C)	I_{RRM}	–	–	1.0	mA
*Peak Forward Blocking Current (V_D = Rated V_{DRM}, T_J = 125°C)	I_{DRM}	–	–	1.0	mA
*Peak On-State Voltage (I_F = 1.0 Adc, Pulsed, 1.0 ms (Max), Duty Cycle ≤ 1%)	V_{TM}	–	1.1	2.0	Volts
*Gate Trigger Current (V_D = 7 V, R_L = 12 Ohms)	I_{GT}	–	2.0	10	mA
*Gate Trigger Voltage (V_D = 7.0 V, R_L = 12 Ohms) (V_D = 7.0 V, R_L = 12 Ohms, T_J = 125°C)	V_{GT}	– 0.2	0.7 –	3.0 –	Volts
Reverse Gate Current (V_{GK} = 10 V)	I_{GR}	–	17	–	mA
Holding Current (V_D = 7.0 V)	I_H	–	5.0	–	mA
Turn-On Time (I_{GT} = 10 mA, I_F = 1.0 A) (I_{GT} = 20 mA, I_F = 1.0 A)	t_{gt}	– –	0.8 0.6	– –	μs
Turn-Off Time (I_F = 1.0 A, I_R = 1.0 A, dv/dt = 20 V/μs, T_J = 125°C)	t_q	–	10	–	μs

*Indicates JEDEC Registered Data.

CURRENT DERATING

FIGURE 1 – CASE TEMPERATURE REFERENCE

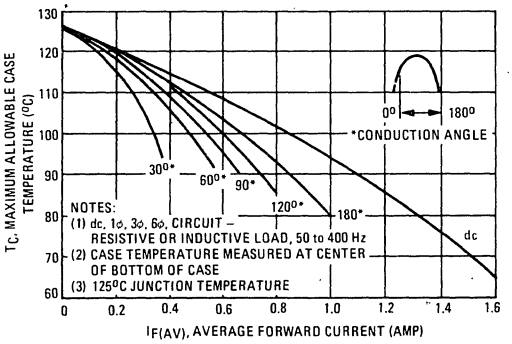
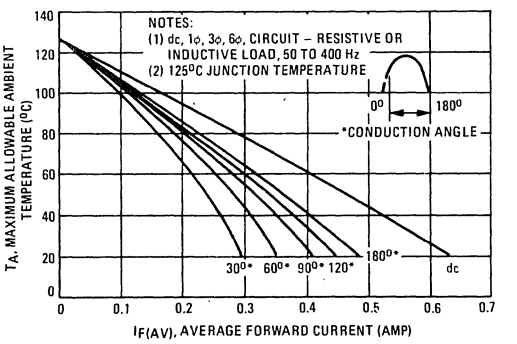
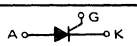


FIGURE 2 – AMBIENT TEMPERATURE REFERENCE



2N1842 thru 2N1850



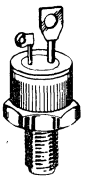
REVERSE BLOCKING TRIODE THYRISTOR

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions with Center Gate Geometry for Greater Parameter Uniformity and Stability
- Blocking Voltage to 500 Volts

SILICON CONTROLLED RECTIFIERS

16 AMPERE RMS
25–500 VOLTS



MAXIMUM RATINGS (T_J = 100°C unless otherwise noted.)

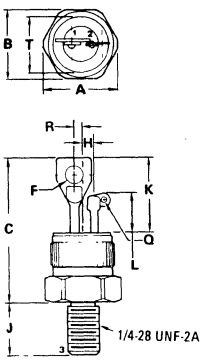
Rating	Symbol	Value	Unit
*Peak Repetitive Forward or Reverse Blocking Voltage (1) 2N1842	V_{DRM} or V_{RRM}	25	Volts
2N1843		50	
2N1844		100	
2N1845		150	
2N1846		200	
2N1847		250	
2N1848		300	
2N1849		400	
2N1850		500	
*Non-Repetitive Peak Reverse Voltage 2N1842	V_{RSM}	35	Volts
2N1843		75	
2N1844		150	
2N1845		225	
2N1846		300	
2N1847		350	
2N1848		400	
2N1849		500	
2N1850		600	
*Average On-State Current (T_C = 35°C)	$I_{T(AV)}$	10	Amp
*Peak Non-Repetitive Surge Current (One cycle, 60 Hz, preceded and followed by rated current and voltage)	I_{TSM}	125	Amp
Circuit Fusing (T_J = −40 to +100°C, t = 1.0 to 8.3 ms)	I^2t	60	A^2s
*Peak Gate Power	P_{GM}	5.0	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current	I_{GM}	2.0	Amp
*Peak Gate Voltage — Forward	V_{FGM}	10	Volts
Reverse	V_{RGM}	5.0	
*Operating Junction Temperature Range	T_J	-40 to +100	°C
*Storage Temperature Range	T_{stg}	-40 to +125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistanca, Junction to Case	$R_{\theta JC}$	2.0	°C/W

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

STYLE 1:
PIN 1. CATHODE
2. GATE
3. ANODE

CASE 263-03

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Average Forward or Reverse Blocking Current (V_D = Rated V_{DRM}, V_R = Rated V_{RRM}, T_C = 35°C)	$I_{D(AV)}$, $I_{R(AV)}$				mA
2N1842		–	–	22.5	
2N1843		–	–	19	
2N1844		–	–	12.5	
2N1845		–	–	6.5	
2N1846		–	–	6.0	
2N1847		–	–	5.5	
2N1848		–	–	5.0	
2N1849		–	–	4.0	
2N1850		–	–	3.0	
Peak Forward or Reverse Blocking Current (V_D Rated V_{DRM}, V_D = Rated V_{RRM}, gate open, T_C = 100°C)	I_{DRM}, I_{RRM}	–	–	6.0	mA
*Peak On-State Voltage (I_{TM} = 31.4 A peak, Pulse Width ≤ 1.0 ms, Duty Cycle ≤ 2.0%)	V_{TM}	–	–	2.5	Volts
Gate Trigger Current, Continuous dc	I_{GT}				mA
(V_D = 12 Vdc, R_L = 50 Ω)		–	6.0	80	
*(V_D = 12 Vdc, R_L = 50 Ω, T_C = -40°C)		–	–	150	
Gate Trigger Voltage, Continuous dc	V_{GT}				Volts
(V_D = 12 Vdc, R_L = 50 Ω)		–	0.65	–	
*(V_D = 12 Vdc, R_L = 50 Ω, T_C = -40°C)		–	–	3.5	
*(V_D Rated V_{DRM}, R_L = 50 Ω, T_C = 100°C)		0.3	–	–	
Holding Current (V_D = 12 Vdc, Gate Open)	I_H	–	7.0	–	mA
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_C = 100°C, Gate Open)	dv/dt	–	30	–	V/μS

*Indicates JEDEC Registered Data.

FIGURE 1 – AVERAGE CURRENT DERATING

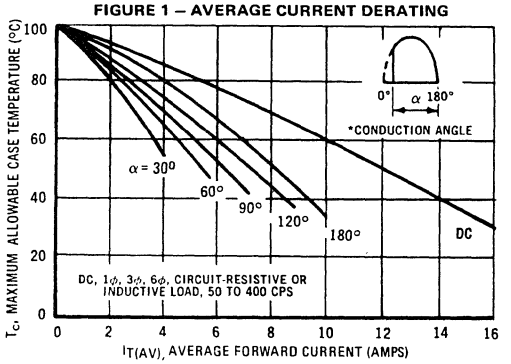


FIGURE 2 – GATE TRIGGER CURRENT

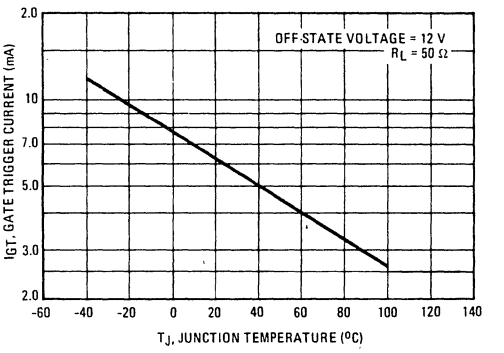


FIGURE 3 – GATE TRIGGER VOLTAGE

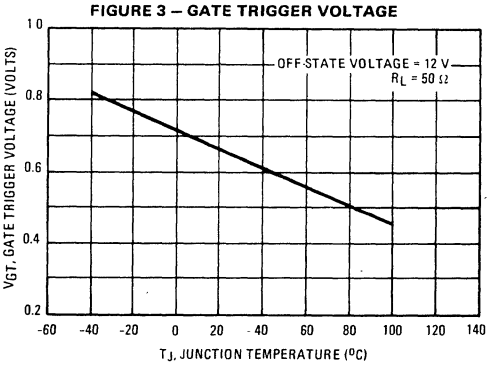
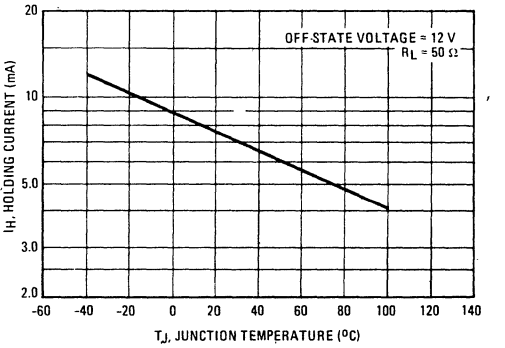
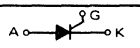


FIGURE 4 – HOLDING CURRENT



2N1842A thru 2N1850A



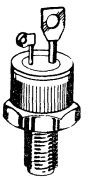
REVERSE BLOCKING TRIODE THYRISTOR

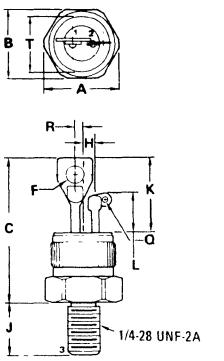
. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions with Center Gate Geometry for Greater Parameter Uniformity and Stability
- Blocking Voltage to 500 Volts
- Junction Temperature Rated @ 125°C

SILICON CONTROLLED RECTIFIERS

16 AMPERE RMS
25 – 500 VOLTS





MAXIMUM RATINGS (T_C = 125°C unless otherwise noted.)

Rating		Symbol	Value	Unit
*Peak Repetitive Forward or Reverse Blocking Voltage (1)	2N1842A	V_{DRM} or V_{RRM}	25	Volts
	2N1843A		50	
	2N1844A		100	
	2N1845A		150	
	2N1846A		200	
	2N1847A		250	
	2N1848A		300	
	2N1849A		400	
	2N1850A		500	
*Non-Repetitive Peak Reverse Voltage		V_{RSM}		Volts
	2N1842A		35	
	2N1843A		75	
	2N1844A		150	
	2N1845A		225	
	2N1846A		300	
	2N1847A		350	
	2N1848A		400	
	2N1849A		500	
	2N1850A		600	
*Average On-State Current (T_C = 80°C)		$I_{T(AV)}$	10	Amp
*Peak Non-Repetitive Surge Current (One cycle, 60 Hz, preceded and followed by rated current and voltage)		I_{TSM}	125	Amp
Circuit Fusing (T_J = -65 to +125°C, t = 1.0 to 8.3 ms)		I^2t	60	A^2s
*Peak Gate Power		P_{GM}	5.0	Watts
*Average Gate Power		$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current		I_{GM}	2.0	Amp
*Peak Gate Voltage – Forward		V_{FGM}	10	Volts
Reverse		V_{RGM}	5.0	
*Operating Junction Temperature Range		T_J	-65 to +125	°C
*Storage Temperature Range		T_{stg}	-65 to +125	°C

THERMAL CHARACTERISTIC

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

*Indicates JEDEC Registered Data.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

STYLE 1:
PIN 1. CATHODE
2. GATE
3. ANODE

CASE 263-03

ELECTRICAL CHARACTERISTICS (T_C = 125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Average Forward or Reverse Blocking Current (V_D = Rated V_{DRM} or V_R = Rated V_{RRM}, gate open, T_C = 125°C) 2N1842A	$I_{D(AV)}$,$I_{R(AV)}$				mA
2N1843A		–	–	22.5	
2N1844A		–	–	19	
2N1845A		–	–	12.5	
2N1846A		–	–	6.5	
2N1847A		–	–	6.0	
2N1848A		–	–	5.5	
2N1849A		–	–	5.0	
2N1850A		–	–	4.0	
		–	–	3.0	
Peak Forward or Reverse Blocking Current (V_D = Rated V_{DRM} or V_R = Rated V_{RRM}, gate open, T_C = 125°C)	I_{DRM},I_{RRM}	–	–	6.0	mA
*Peak On-State Voltage (I_{TM} = 31.4 A peak, Pulse Width ≤ 1.0 ms, Duty Cycle ≤ 2.0%)	V_{TM}	–	–	2.5	Volts
Gate Trigger Current, Continuous dc (V_D = 12 Vdc, R_L = 50 Ω)	I_{GT}	–	6.0	80	mA
*V_D = 12 Vdc, R_L = 50 Ω, T_C = -65°C)		–	–	150	
Gate Trigger Voltage, Continuous dc (V_D = 12 Vdc, R_L = 50 Ω)	V_{GT}	–	0.65	–	Volts
*(V_D = 12 Vdc, R_L = 50 Ω, T_C = -40°C)		–	–	3.5	
* (V_D = 12 Vdc, R_L = 50 Ω, T_C = -65°C)		–	–	3.7	
*(V_D = Rated V_{DRM}, R_L = 50 Ω, T_C = 125°C)		0.25	–	–	
Holding Current (V_D = 12 Vdc, Gate Open)	I_H	–	7.0	–	mA
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_C = 125°C, Gate Open)	dv/dt	–	30	–	V/μS

*Indicates JEDEC Registered Data.

FIGURE 1 – AVERAGE CURRENT DERATING

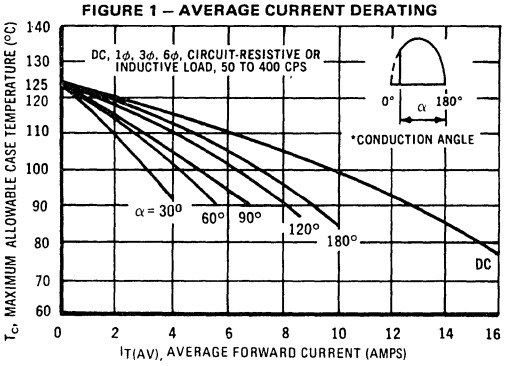


FIGURE 2 – GATE TRIGGER CURRENT

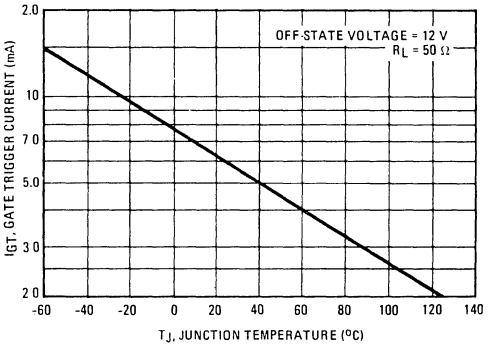


FIGURE 3 – GATE TRIGGER VOLTAGE

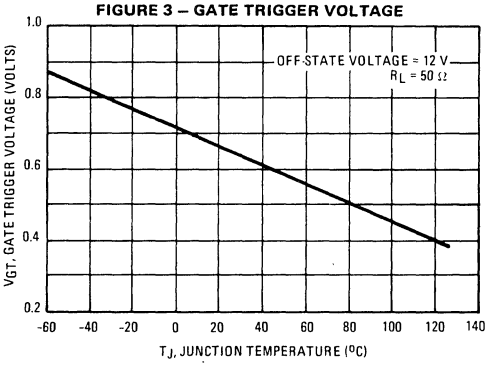
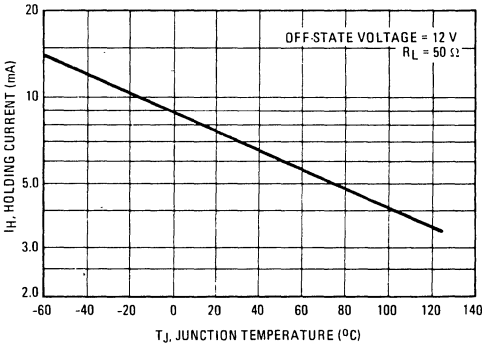
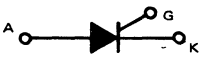


FIGURE 4 – HOLDING CURRENT



2N2322 thru 2N2329



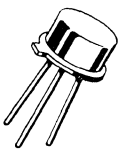
REVERSE BLOCKING TRIODE THYRISTOR

. . . all-diffused PNP devices designed for gating operation in mA/μA signal or detection circuits.

- Low-Level Gate Characteristics
  I_{GT} = 200 μA (Max) @ 25°C
- Low Holding Current – I_H = 2.0 mA (Max) @ 25°C
- Anode Common to Case
- Glass-to-Metal Bond for Maximum Hermetic Seal

SILICON CONTROLLED RECTIFIER

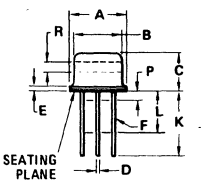
1.6 AMPERE RMS
25 thru 400 VOLTS

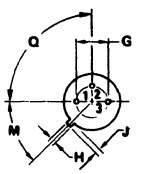


***MAXIMUM RATINGS** (T_C = 25°C unless otherwise noted, R_{GK} = 1000 ohms)

Rating		Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage (Notes 2 and 3)	2N2322	V_{DRM} or V_{RRM}	25	Volts
	2N2323		50	
	2N2324		100	
	2N2325		150	
	2N2326		200	
	2N2327		250	
	2N2328		300	
	2N2329		400	
Non- Repetitive Peak Reverse Blocking Voltage (t ≤ 5.0 ms, Notes 2 and 3)	2N2322	V_{RSM}	40	Volts
	2N2323		75	
	2N2324		150	
	2N2325		225	
	2N2326		300	
	2N2327		350	
	2N2328		400	
	2N2329		500	
RMS On-State Current (All Conduction Angles)		$I_{T(RMS)}$	1.6	Amp
Average On-State Current	T_C = 85°C	$I_{T(AV)}$	1.0	Amp
	T_A = 30°C		0.45	
Peak Non-Repetitive Surge Current (One Cycle, 60 Hz, T_C = 80°C) Preceded and followed by rated current and voltage		I_{TSM}	15	Amp
Peak Gate Power		P_{GM}	0.1	Watt
Average Gate Power		$P_{G(AV)}$	0.01	Watt
Peak Gate Current		I_{GM}	0.1	Amp
Peak Gate Voltage		V_{GM}	6.0	Volts
Operating Junction Temperature Range		T_J	-65 to +125	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C
Lead Solder Temperature (>1/16" from case, 10 s max)		–	+230	°C

*Indicates JEDEC Registered Data.





STYLE 3:
PIN 1. CATHODE
2. GATE
3. ANODE (CONNECTED TO CASE)

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO-39

7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted, R_{GK} = 1000 ohms)

Characteristic	Symbol	Min	Max	Unit
*Peak Reverse Blocking Current (Rated V_{RRM}, T_J = 125°C)	I_{RRM}	–	100	μA
*Peak Forward Blocking Current (Rated V_{DRM}, T_J = 125°C)	I_{DRM}	–	100	μA
Peak On-State Voltage	V_{TM}			Volts
(I_{TM} = 1.0 A Peak)		–	1.5	
(I_{TM} = 3.14 A Peak, T_C = 85°C)*		–	2.0	
Gate Trigger Current (Note 1)	I_{GT}			μA
(V_D = 6.0 Vdc, R_L = 100 ohms)		–	200	
(V_D = 6.0 Vdc, R_L = 100 ohms, T_C = -65°C)		–	350*	
Gate Trigger Voltage	V_{GT}			Volts
(V_D = 6.0 Vdc, R_L = 100 ohms)		–	0.8	
(V_D = 6.0 Vdc, R_L = 100 ohms, T_C = -65°C)*		–	1.0	
(V_D = Rated V_{DRM}, R_L = 100 ohms, T_J = 125°C)*		0.1	–	
Holding Current	I_H			mA
(V_D = 6.0 Vdc)		–	2.0	
(V_D = 6.0 Vdc, T_C = -65°C)*		–	3.0	
(V_D = 6.0 Vdc, T_C = 125°C)*		0.15	–	

*Indicates JEDEC Registered Data.

Notes: 1. R_{GK} current is not included in measurement.

2. Thyristor devices shall not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

3. Thyristor devices shall not have a positive bias applied to the gate concurrently with a negative potential applied to the anode.

CURRENT DERATING

FIGURE 1 – CASE TEMPERATURE

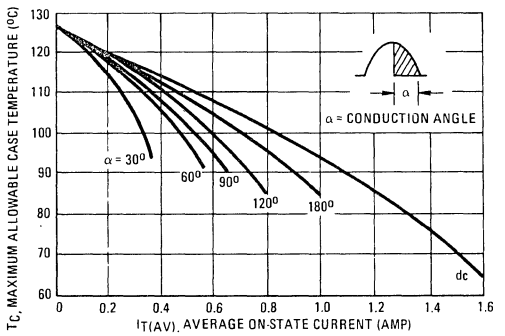
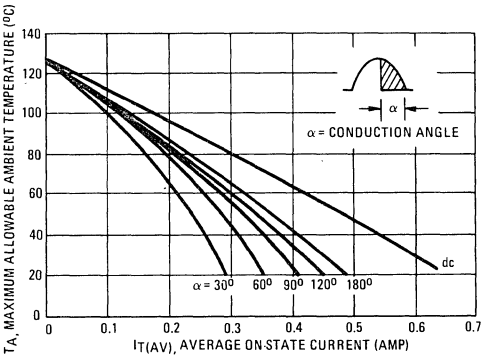


FIGURE 2 – AMBIENT TEMPERATURE



2N2573 thru 2N2579
MCR649AP-1 thru -10

REVERSE BLOCKING TRIODE THYRISTOR

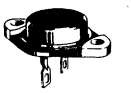
. . . designed for industrial applications such as motor controls, heater controls, and power supplies, wherever half-wave or dc silicon gate controlled devices are needed.

- Glass Passivated Junctions for Maximum Reliability
- Center Gate Geometry for Parameter Uniformity
- High Surge Current, I_{TSM} = 260 A, for Crowbar Service

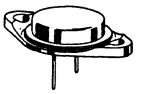
SILICON CONTROLLED RECTIFIER

25 AMPERES RMS

25-500 VOLTS



CASE 61-03



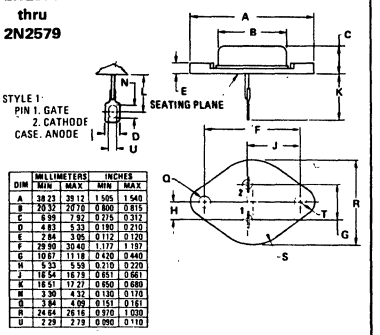
CASE 54-05

MAXIMUM RATINGS (T_J = 125°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage (1)	V_{DRM} or V_{RRM}		Volts
2N2573, MCR649AP-1		25	
2N2574, MCR649AP-2		50	
2N2575, MCR649AP-3		100	
2N2576, MCR649AP-4		200	
2N2577, MCR649AP-5		300	
2N2578, MCR649AP-6		400	
2N2579, MCR649AP-7		500	
On-State Current	$I_{T(RMS)}$	25	Amp
Circuit Fusing (T_J = -65°C to +125°C, t ≤ 8.3 ms)	I^2t	275	A^2sec.
Peak Surge Current (One Cycle, 60 Hz, T_J = -65° to +125°C)	I_{TSM}	260	Amp
Peak Gate Power — Forward	P_{GM}	5.0	Watts
Average Gate Power — Forward	$P_{G(AVG)}$	0.5	Watts
Peak Gate Current — Forward	I_{GM}	2.0	Amp
Peak Gate Voltage — Forward	V_{GFM}	10	Volts
Reverse	V_{GRM}	5.0	
Operating Junction Temperature	T_J	-65 to +125	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous basis without incurring damage. Ratings apply for zero or negative gate voltage.

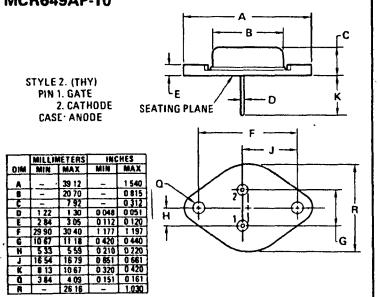
2N2573 thru 2N2579



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	38.23	39.12	1.505	1.540
B	20.32	20.70	0.800	0.815
C	6.99	7.92	0.275	0.312
D	4.83	5.33	0.190	0.210
E	2.84	3.05	0.112	0.120
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.54	16.79	0.651	0.661
K	16.51	17.27	0.650	0.680
M	3.30	4.32	0.130	0.170
Q	3.84	4.09	0.151	0.161
R	24.64	26.16	0.970	1.030
U	2.29	2.79	0.090	0.110

CASE 61-03

MCR649AP-1 thru MCR649AP-10



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	--	39.12	--	1.540
B	--	20.70	--	0.815
C	--	7.92	--	0.312
D	1.22	1.30	0.048	0.051
E	2.84	3.05	0.112	0.120
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.58	0.210	0.220
J	16.54	16.79	0.651	0.661
K	8.13	10.67	0.320	0.420
Q	3.84	4.09	0.151	0.161
R	--	26.16	--	1.030

CASE 54-05

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Units
Peak Forward Blocking Current (V_D = Rated V_{DRM} with gate open, T_J = 125°C)	I_{DRM}	–	0.6	5.0	mA
Peak Reverse Blocking Current (V_R = Rated V_{RRM}, T_J = 125°C)	I_{RRM}	–	0.6	5.0	mA
Gate Trigger Current (Continuous dc) (V_D = 7 Vdc, R_L = 100 Ω)	I_{GT}	–	–	40	mA
Gate Trigger Voltage (Continuous dc) (V_D = 7 Vdc, R_L = 100 Ω) (V_D = Rated V_{DRM}, R_L = 100 Ω, T_J = 125°C)	V_{GT}	– 0.3	0.7 –	3.5 –	Volts
Forward On Voltage (I_{TM} = 20 Adc)	V_{TM}	–	1.1	1.4	Volts
Holding Current (V_D = 7 Vdc, Gate Open)	I_H	–	10	–	mA
Turn-On Time (t_d + t_r) (I_{GT} = 50 mA, I_T = 10A, V_D = Rated V_{DRM})	t_{gt}	–	1.0	–	μs
Turn-Off Time (I_T = 10 A, I_R = 10 A, dv/dt = 20 V/μs, T_J = 125°C) (V_D = Rated Voltage V_{DRM})	t_q	–	30	–	μs
Forward Voltage Application Rate (Exponential) (Gate Open, T_J = 125°C, V_D = Rated V_{DRM})	dv/dt	–	30	–	V/μs

FIGURE 1 – CURRENT DERATING

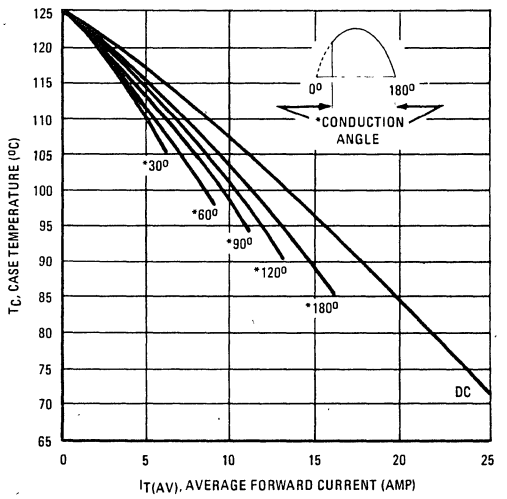


FIGURE 2 – GATE TRIGGER CHARACTERISTICS

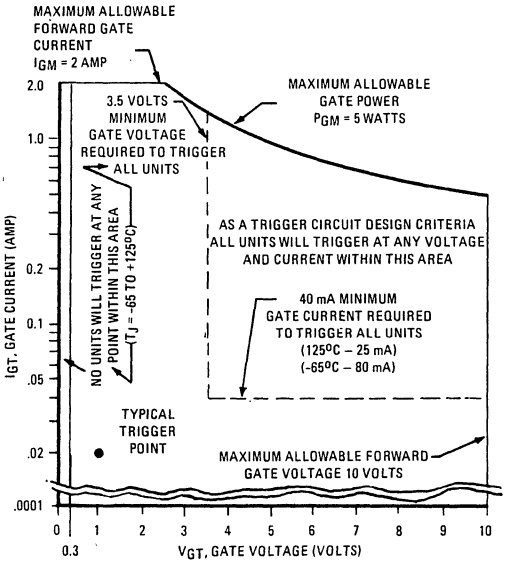


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FIGURE 3 – ON-STATE CHARACTERISTICS

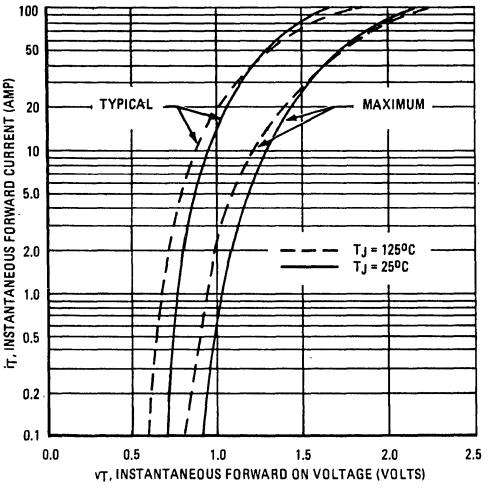


FIGURE 4 – MAXIMUM ALLOWABLE NON-RECURRENT SURGE CURRENT

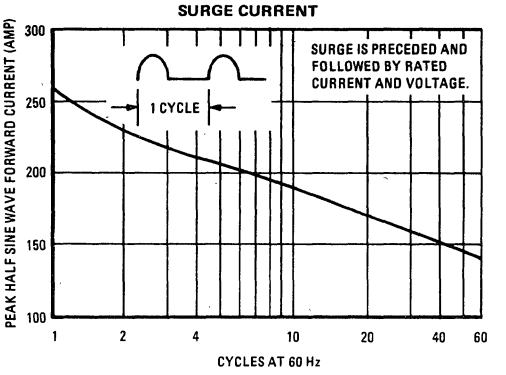


FIGURE 5 – EFFECT OF TEMPERATURE ON TYPICAL HOLDING CURRENT

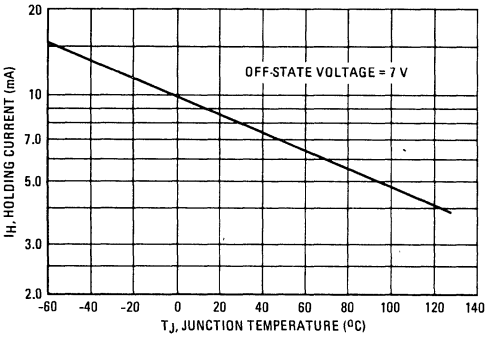


FIGURE 6 – EFFECT OF TEMPERATURE ON TYPICAL GATE CURRENT

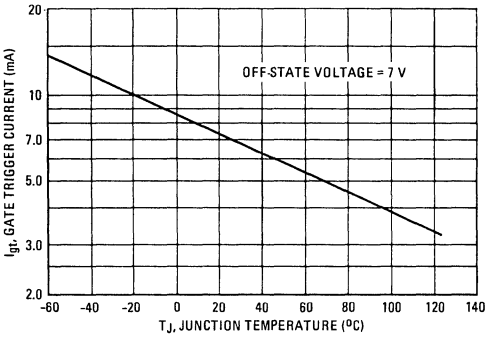


FIGURE 7 – EFFECT OF TEMPERATURE ON TYPICAL GATE VOLTAGE

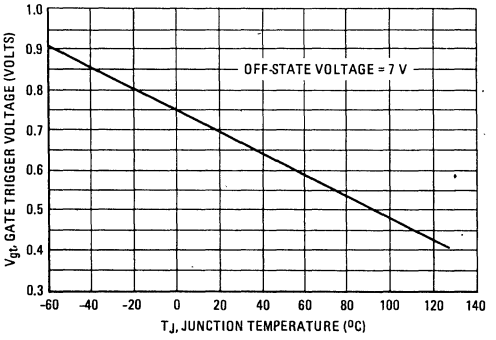
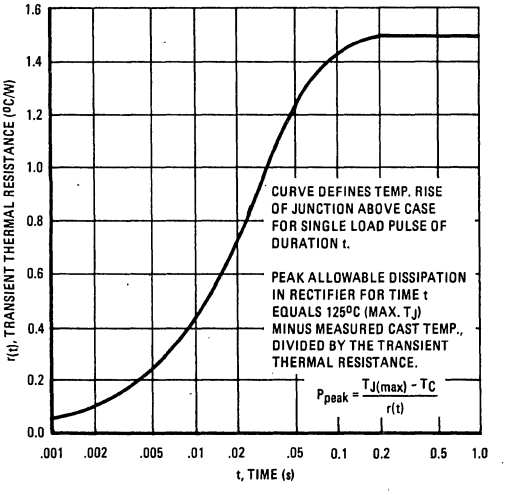


FIGURE 8 – MAXIMUM TRANSIENT THERMAL RESISTANCE JUNCTION TO CASE



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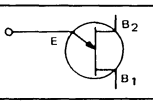
2N2646
2N2647



SILICON PN UNIJUNCTION TRANSISTORS

. . . designed for use in pulse and timing circuits, sensing circuits and thyristor trigger circuits. These devices feature:

- Low Peak Point Current – 2.0 μA (Max)
- Low Emitter Reverse Current – 200 nA (Max)
- Passivated Surface for Reliability and Uniformity

PN UNIJUNCTION TRANSISTORS

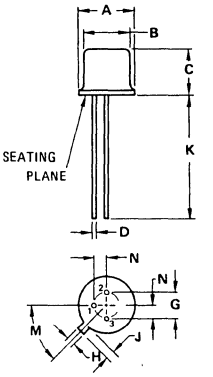
***MAXIMUM RATINGS** (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Dissipation (1)	P_D	300	mW
RMS Emitter Current	$I_{E(RMS)}$	50	mA
Peak Pulse Emitter Current (2)	i_E	2.0	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage	V_{B2B1}	35	Volts
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

*Indicates JEDEC Registered Data.

(1) Derate 3.0 mW/°C increase in ambient temperature. The total power dissipation (available power to Emitter and Base-Two) must be limited by the external circuitry.

(2) Capacitor discharge – 10 μF or less, 30 volts or less.



STYLE 1:
PIN 1. EMITTER
2. BASE 1
3. BASE 2

Pin 3 Connected to Case.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.48	0.016	0.019
G	2.54 TYP		0.100 TYP	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
M	45° TYP		45° TYP	
N	1.27 TYP		0.050 TYP	

CASE 22A-01

(TO-18 Except for Lead Position)

7

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio (V_{B2B1} = 10 V) (Note 1)	2N2646	η	0.56	–	0.75	–
	2N2647		0.68	–	0.82	
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)		r_{BB}	4.7	7.0	9.1	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = -55°C to +125°C)		$\alpha_{r_{BB}}$	0.1	–	0.9	%/°C
Emitter Saturation Voltage (V_{B2B1} = 10 V, I_E = 50 mA) (Note 2)		$V_{EB1(sat)}$	–	3.5	–	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)		$I_{B2(mod)}$	–	15	–	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)	2N2646	I_{EB2O}	–	0.005	12	μA
	2N2647		–	0.005	0.2	
Peak Point Emitter Current (V_{B2B1} = 25 V)	2N2646	I_P	–	1.0	5.0	μA
	2N2647		–	1.0	2.0	
Valley Point Current (V_{B2B1} = 20 V, R_{B2} = 100 ohms) (Note 2)	2N2646	I_V	4.0	6.0	–	mA
	2N2647		8.0	10	–	
Base-One Peak Pulse Voltage (Note 3, Figure 3)	2N2646	V_{OB1}	3.0	5.0	–	Volts
	2N2647		6.0	7.0	–	

*Indicates JEDEC Registered Data.

Notes:

(1) Intrinsic standoff ratio, η, is defined by equation:

$$\eta = \frac{V_P - V_F}{V_{B2B1}}$$

Where V_P = Peak Point Emitter Voltage
V_{B2B1} = Interbase Voltage
V_F = Emitter to Base-One Junction Diode Drop
(≈ 0.45 V @ 10 μA)

(2) Use pulse techniques: PW ≈ 300 μs, duty cycle ⩽ 2% to avoid internal heating due to interbase modulation which may result in erroneous readings.

(3) Base-One Peak Pulse Voltage is measured in circuit of Figure 3. This specification is used to ensure minimum pulse amplitude for applications in SCR firing circuits and other types of pulse circuits.

7

FIGURE 1
UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

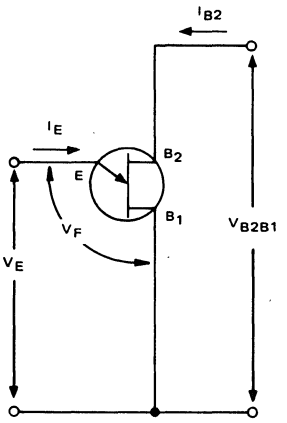


FIGURE 2
STATIC EMITTER CHARACTERISTIC CURVES
(Exaggerated to Show Details)

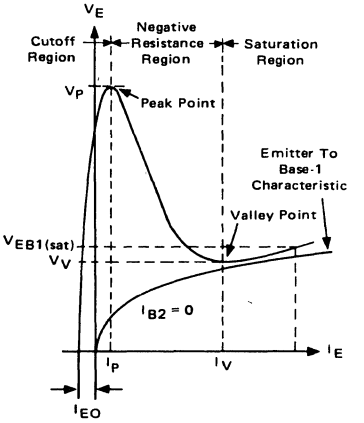
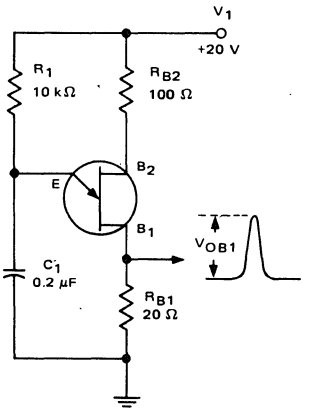
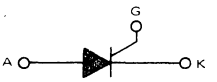


FIGURE 3 – V_{OB1} TEST CIRCUIT
(Typical Relaxation Oscillator)



2N3668 thru 2N3670
2N4103



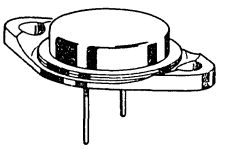
REVERSE BLOCKING TRIODE THYRISTOR

These devices are designed for 12.5 Ampere RMS, 100 through 600 Volt power supply and computer control applications to 100°C maximum Junction Temperature.

- Low Forward "On" Voltage –
  V_{TM} = 1.8 Volts (Max) @ T_J = 25°C
- All Diffused Junctions for Greater Parameter Uniformity
- Glass Passivated for Greater Stability

SILICON CONTROLLED RECTIFIER

12.5 AMPERES RMS
100–600 VOLTS

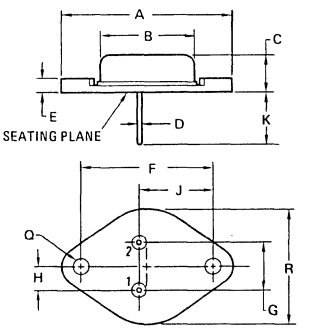


*MAXIMUM RATINGS Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage (1)	V_{DRM} or V_{RRM}		Volts
2N3668		100	
2N3669		200	
2N3670		400	
2N4103		600	
Forward Current RMS (T_C = 80°C) (All Conduction Angles)	$I_{T(RMS)}$	12.5	Amps
Peak Forward Surge Current (1/2 cycle, Sine Wave, 60 Hz, T_J = –40 to 100°C)	I_{TSM}	200	Amps
Circuit Fusing (T_J = –40 to +100°C, t = 1.0 to 8.3 ms)	I^2t	170	A^2s
Forward Peak Gate Power	P_{GM}	5.0	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2.0	Amps
Peak Forward Gate Voltage	V_{GF}	10	Volts
Peak Reverse Gate Voltage	V_{GR}	5.0	Volts
Operating Junction Temperature Range	T_J	–40 to +100	°C
Storage Temperature Range	T_{stg}	–40 to +125	°C

THERMAL CHARACTERISTICS Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.7	°C/W

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurrent damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

*Indicates JEDEC Registered Data.



STYLE 2: (THY)
PIN 1. GATE
2. CATHODE
CASE: ANODE

DIM*	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	39.12	–	1.540
B	–	20.70	–	0.815
C	–	7.92	–	0.312
D	1.22	1.30	0.048	0.051
E	2.84	3.05	0.112	0.120
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.54	16.79	0.651	0.661
K	8.13	10.67	0.320	0.420
Q	3.84	4.09	0.151	0.161
R	–	26.16	–	1.030

CASE 54-05

7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Current (V_D = Rated V_{DRM} @ T_J = 100°C)		I_{DRM}				mA
	2N3668		–	–	2.0	
	2N3669		–	–	2.5	
	2N3670		–	–	3.0	
	2N4103		–	–	4.0	
*Peak Reverse Blocking Current (V_R = Rated V_{RRM} @ T_J = 100°C)		I_{RRM}				mA
	2N3668		–	–	1.0	
	2N3669		–	–	1.25	
	2N3670		–	–	1.5	
	2N4103		–	–	2.0	
*Forward "On" Voltage (1) (I_{TM} = 25 A peak)		V_{TM}	–	1.1	1.8	Volts
*Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 24 Ohms)	(T_J = 25°C)	I_{GT}	–	7.0	40	mA
	(T_J = -40°C)*		–	–	80	
*Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, R_L = 24 Ohms)		V_{GT}				Volts
	(T_J = -40°C)*		–	1.0	3.0	
	(T_J = +25°C)		–	0.68	2.0	
	(T_J = +100°C)		0.3	–	–	
Holding Current (V_D = 12 Vdc, I_T = 0.5A)		I_H	–	20	50	mA
Turn-On Time (V_D = Rated V_{DRM}, I_{TM} = 8A, I_G = 0.2A, t_r = 100ns)		t_{gt}	–	0.5	–	μs
Turn-Off Time (V_D = Rated V_{DRM}, I_{TM} = 8A, I_G = 200 mA, Pulse Width ≤ 50μs, dv/dt = 20V/μs, di/dt = 30A/μs, T_C = 80°C)		t_q	–	20	–	μs
Forward Voltage Application Rate Exponential (V_D = Rated V_{DRM}, T_C = 100°C)		dv/dt	10	100	–	V/μs

* Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 1 ms, Duty Cycle ≤ 1%

7

FIGURE 1 – TYPICAL GATE TRIGGER CURRENT

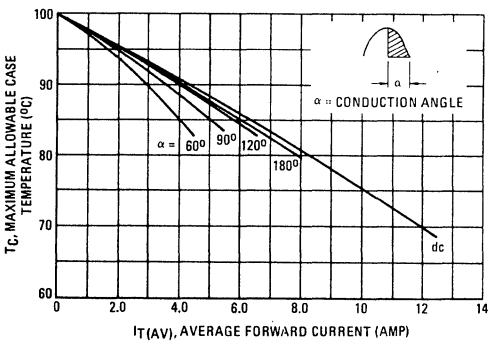


FIGURE 2 – TYPICAL GATE TRIGGER VOLTAGE

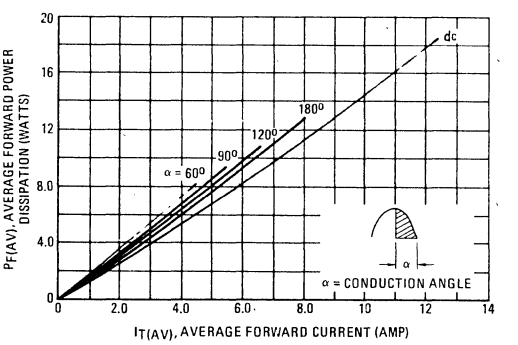


FIGURE 3 – TYPICAL GATE TRIGGER CURRENT

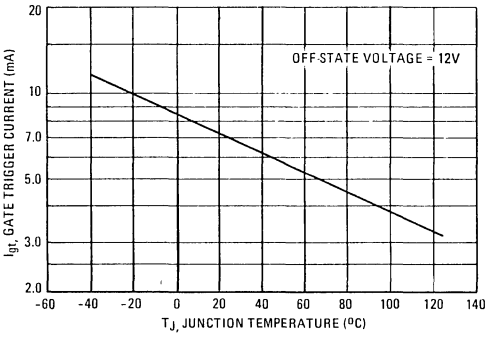
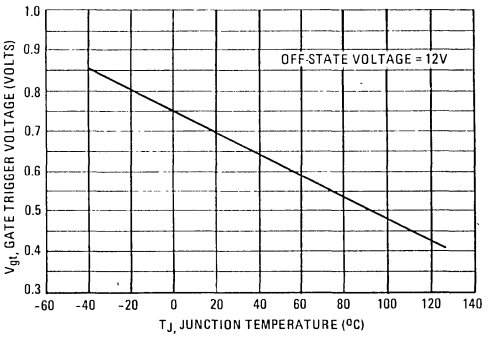
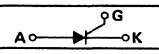


FIGURE 4 – TYPICAL GATE TRIGGER VOLTAGE



2N3870 thru 2N3873
2N3896 thru 2N3899
2N6171 thru 2N6174



REVERSE BLOCKING TRIODE THYRISTORS

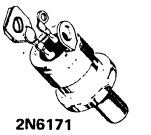
. . . designed for industrial and consumer applications such as power supplies; battery chargers; temperature, motor, light and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current – I_{TSM} = 350 Amp
- Practical Level Triggering and Holding Characteristics – 4.0 and 5.2 mA (Typ) @ T_C = 25°C
- Rugged Construction in Either Pressfit, Stud or Isolated Stud Package

SILICON CONTROLLED RECTIFIERS

35 AMPERES RMS
100-800 VOLTS

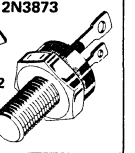
CASE 311-01
(Stud Isolated)



2N6171
thru
2N6174

CASE 174-03
TO-203
2N3870
thru
2N3873

CASE 175-02
2N3896
thru
2N3899



MAXIMUM RATINGS (T_C = 100°C unless otherwise noted)

Rating	Symbol	Value	Unit
*Peak Repetitive Forward or Reverse Blocking Voltage (1) (T_J = -40 to +100°C, 1/2 Sine Wave, 50 to 400 Hz, Gate Open)	V_{RRM} or V_{DRM}		Volts
2N3870, 2N3896, 2N6171		100	
2N3871, 2N3897, 2N6172		200	
2N3872, 2N3898, 2N6173		400	
2N3873, 2N3899, 2N6174		600	
*Peak Non-Repetitive Forward or Reverse Blocking Voltage (t ≤ 5.0 ms)	V_{RSM} or V_{DSM}		Volts
2N3870, 2N3896, 2N6171		150	
2N3871, 2N3897, 2N6172		330	
2N3872, 2N3898, 2N6173		660	
2N3873, 2N3899, 2N6174		700	
*Average On-State Current (2) (T_C = -40 to +65°C) (T_C = +85°C)	$I_{T(AV)}$	22 11	Amp
*Peak Non-Repetitive Surge Current (One cycle, 60 Hz) (T_C = +65°C)	I_{TSM}	350	Amp
Circuit Fusing (T_C = -40 to +100°C) (t = 1.0 to 8.3 ms)	I^2t	510	A^2s
*Peak Gate Power	P_{GM}	20	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current	I_{GM}	2.0	Amp
Peak Gate Voltage	V_{GM}	10	Volts
*Operating Junction Temperature Range	T_J	-40 to +100	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C
Stud Torque	–	30	in lb.

***THERMAL CHARACTERISTICS**

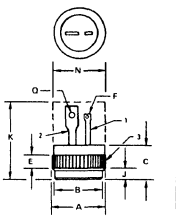
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
2N3870 thru 2N3873, 2N3896 thru 2N3899		0.9	
2N6171 thru 2N6174		1.0	

*Indicates JEDEC Registered Data.

(1) Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

(2) Isolated stud devices must be derated an additional 10 percent.

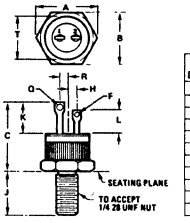
2N3870 thru 2N3873 — **CASE 174-03 TO-203**



STYLE 1:
TERM 1 GATE
2 CATHODE
3 ANODE

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	12.73	12.83	0.501	0.505
B	11.81	12.06	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54	–	0.100	
F	0.89	2.16	0.035	0.085
J	2.04	2.46	0.080	0.097
K	–	20.32	–	0.800
N	–	12.95	–	0.510
Q	1.65	4.06	0.065	0.160

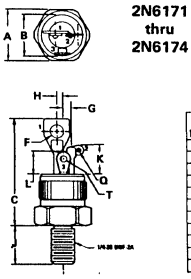
2N3896 thru 2N3899 — **CASE 175-02**



STYLE 1
TERM 1 CATHODE
2 GATE
STUD ANODE

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	0.89	2.16	0.035	0.085
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	1.65	4.06	0.065	0.160
R	1.65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505

2N6171 thru 2N6174 — **CASE 311-01 (Stud Isolated)**



STYLE 1
1 CATHODE
2 GATE
3 ANODE

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	32.51	–	1.280
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.60	2.01	0.063	0.079
J	10.67	11.56	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6.48	6.99	0.255	0.275
Q	1.40	2.16	0.055	0.085
T	3.43	3.81	0.135	0.150

7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Current (V_D = Rated V_{DRM}, with gate open, T_C = 100°C)	I_{DRM}				mA
2N3870, 2N3896, 2N6171		–	1.0	2.0	
2N3871, 2N3897, 2N6172		–	1.0	2.5	
2N3872, 2N3898, 2N6173		–	1.0	3.0	
2N3873, 2N3899, 2N6174		–	1.0	4.0	
*Peak Reverse Blocking Current (V_R = Rated V_{RRM}, with gate open, T_C = 100°C)	I_{RRM}				mA
2N3870, 2N3896, 2N6171		–	1.0	2.0	
2N3871, 2N3897, 2N6172		–	1.0	2.5	
2N3872, 2N3898, 2N6173		–	1.0	3.0	
2N3873, 2N3899, 2N6174		–	1.0	4.0	
*Peak On-State Voltage (I_{TM} = 69 A Peak)	V_{TM}	–	1.5	1.85	Volts
*Gate Trigger Current, Continuous dc (V_D = 12 V, R_L = 24 ohms) *T_C = -40°C	I_{GT}	–	9.0	80	mA
T_C = 25°C		–	4.0	40	
*Gate Trigger Voltage Continuous dc (V_D = 12 V, R_L = 24 ohms)	V_{GT}				Volts
*T_C = -40°C		–	0.9	3.0	
T_C = 25°C		–	0.69	1.6	
*Holding Current (Gate Open) (V_D = 12 V, I_{TM} = 200 mA) *T_C = -40°C	I_H	–	14	90	mA
T_C = 25°C		–	5.2	50	
*Gate Controlled Turn-On Time ($t_d + t_r$) (I_{TM} = 41 Adc, V_D = rated V_{DRM}, I_{GT} = 40 mAdc, Rise Time ≤ 0.05 μs, Pulse Width = 10 μs)	t_{gt}	–	–	1.5	μs
Circuit Commutated Turn-Off Time	t_q				μs
(I_{TM} = 10 A, I_R = 10 A)		–	25	–	
(I_{TM} = 10 A, I_R = 10 A, T_C = 100°C)		–	35	–	
Forward Voltage Application Rate (T_C = 100°C, V_D = Rated V_{DRM})	dv/dt	–	50	–	V/μs

*Indicates JEDEC Registered Data.

7

FIGURE 1 – AVERAGE CURRENT DERATING

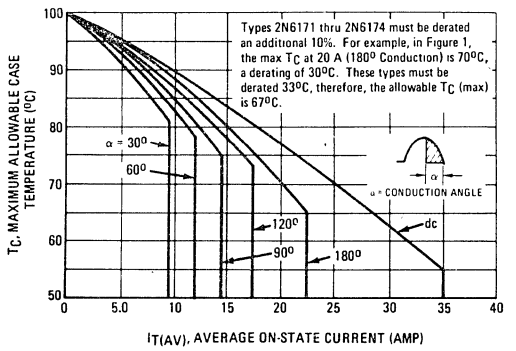


FIGURE 2 – ON-STATE POWER DISSIPATION

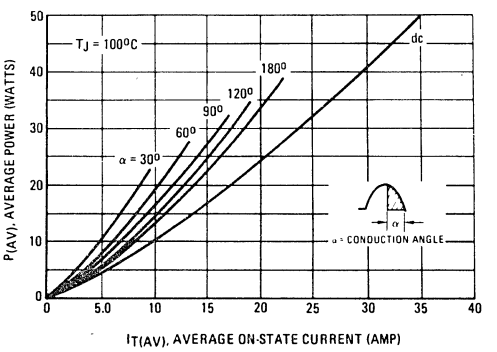


FIGURE 3 – ON-STATE CHARACTERISTICS

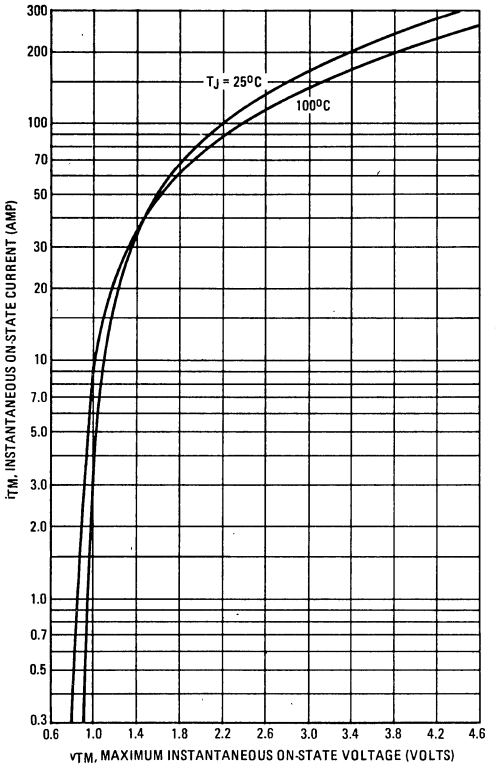


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

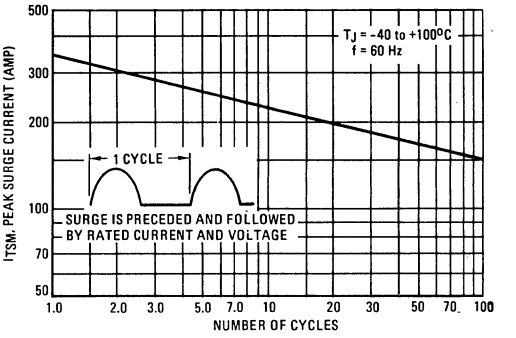


FIGURE 5 – TYPICAL THERMAL RESPONSE

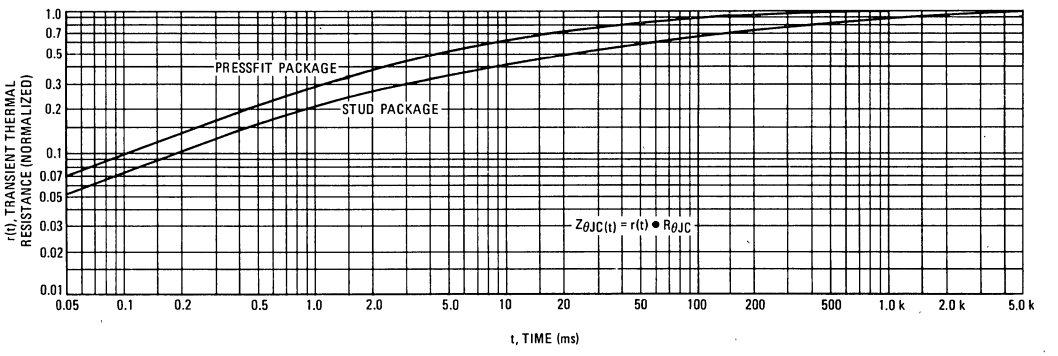


FIGURE 6 – PULSE TRIGGER CURRENT

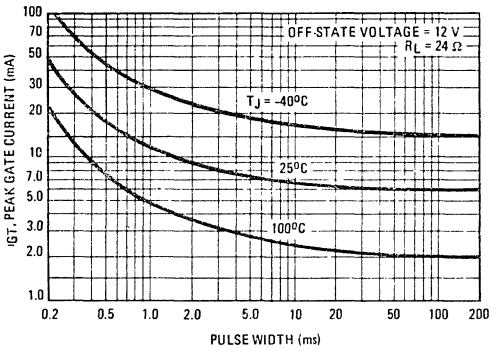


FIGURE 7 – GATE TRIGGER CURRENT

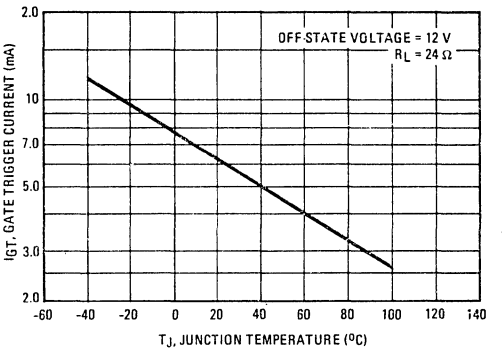


FIGURE 8 – GATE TRIGGER VOLTAGE

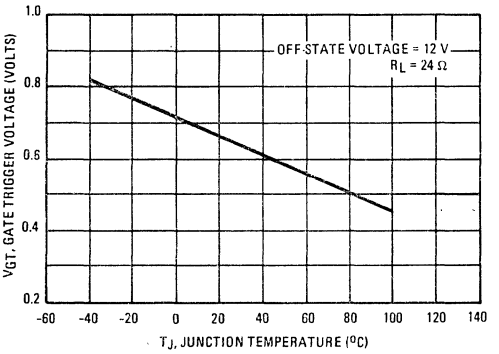
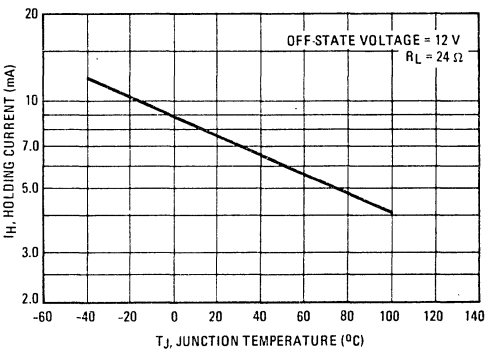


FIGURE 9 – HOLDING CURRENT



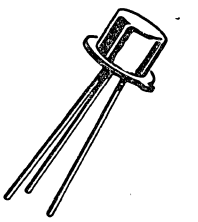
2N3980

SILICON ANNULAR† PN UNIJUNCTION TRANSISTOR

. . . designed for military and industrial use in pulse, timing, sensing, and oscillator circuits. These devices feature:

- Low Peak Point Current — 2.0 μA max
- Fast Switching — to 1.0 MHz
- Low Emitter Reverse Current — 10 nA max
- Passivated Surface for Reliability and Uniformity

PN UNIJUNCTION TRANSISTOR

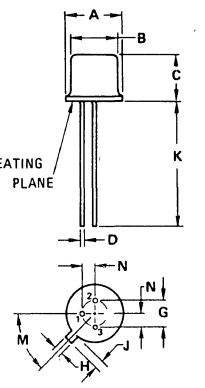


MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Rating	Unit
RMS Power Dissipation (1)	P_D	360	mW
RMS Emitter Current	I_e	50	mA
Peak Pulse Emitter Current (2)	i_e	1.0	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage	V_{B2B1}	35	Volts
Storage Temperature Range	T_{stg}	-65 to +200	°C

(1) Derate 2.4 mW/°C increase in ambient temperature. Total power dissipation (available power to Emitter and Base-Two) must be limited by external circuitry.

(2) Capacitance discharge current must fall to 0.37 Amp within 3.0 ms and PRR ≤ 10 PPS.



STYLE 1
PIN 1. EMITTER
2. BASE 1
3. BASE 2 CONNECTED TO CASE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.48	0.016	0.019
G	2.54 TYP		0.100 TYP	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	—	0.500	—
M	45° TYP		45° TYP	
N	1.27 TYP		0.050 TYP	

TO-18 except for lead position

CASE 22A-01
(TO-18 Type)

†Annular Semiconductors Patented by Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio (V_{B2B1} = 10 V) Note 1	η	0.68	–	0.82	–
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)	R_{BB}	4.0	6.0	8.0	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = -65°C to +100°C)	αR_{BB}	0.4	–	0.9	%/°C
Emitter Saturation Voltage (V_{B2B1} = 10 V, I_E = 50 mA) Note 2	$V_{EB1(sat)}$	–	2.5	3.0	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)	$I_{B2(mod)}$	12	15	–	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)	I_{EB20}	–	5.0	10	nA
(V_{B2E} = 30 V, I_{B1} = 0, T_A = 125°C)		–	–	1.0	μA
Peak Point Emitter Current (V_{B2B1} = 25V)	I_P	–	0.6	2.0	μA
Valley Point Current (V_{B2B1} = 20 V, R_{B2} = 100 ohms) Note 2	I_V	1.0	4.0	10	mA
Base-One Peak Pulse Voltage (Note 3, Figure 3)	V_{OB1}	6.0	8.0	–	Volts
Maximum Oscillation Frequency (Figure 4)	f(max)	1.0	1.25	–	MHz

NOTES

1. Intrinsic standoff ratio, η, is defined by equation:

$$\eta = \frac{V_P - V_{(EB1)}}{V_{B2B1}}$$

Where V_P = Peak Point Emitter Voltage
V_{B2B1} = Interbase Voltage
$V_{(EB1)}$ = Emitter to Base-One Junction Diode Drop (0.45V @ 10 μA)

2. Use pulse techniques: PW ≈ 300 μs duty cycle ≤2% to avoid internal heating due to interbase modulation which may result in erroneous readings.

3. Base-One Peak Pulse Voltage is measured in circuit of Figure 3. This specification is used to ensure minimum pulse amplitude for applications in ACR firing circuits and other types of pulse circuits.

FIGURE 1 – UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

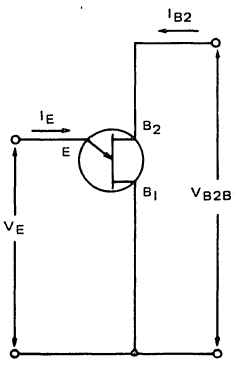


FIGURE 2 – STATIC EMITTER CHARACTERISTICS CURVES (Exaggerated to Show Details)

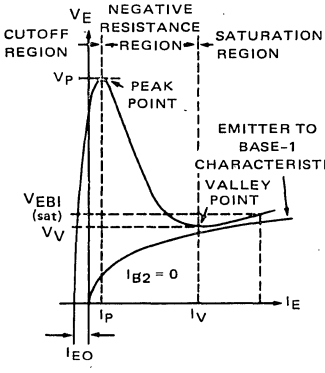


FIGURE 3 – V_{OB1} TEST CIRCUIT (Typical Relaxation Oscillator)

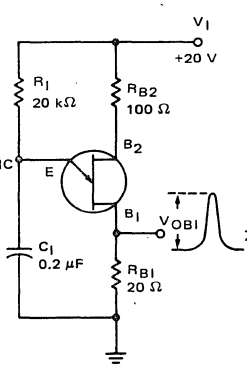
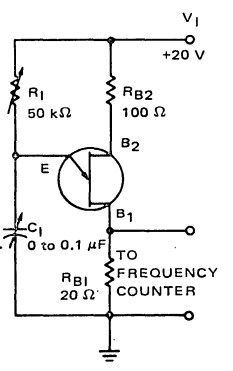


FIGURE 4 – f(max) MAXIMUM FREQUENCY TEST CIRCUIT



2N4167 thru 2N4174
2N4183 thru 2N4190

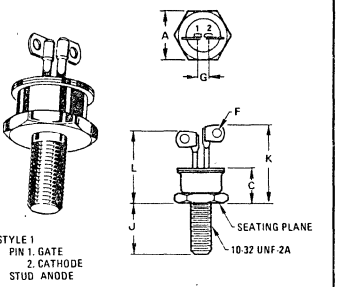
REVERSE BLOCKING TRIODE THYRISTOR

. . . multi-purpose PNPN silicon controlled rectifiers suited for industrial, consumer, and mulitary applications. Offered in a choice of space-saving, economical packages for mounting versatility.

- Uniform Low-Level Noise-Immune Gate Triggering – I_{GT} = 10 mA (Typ) @ T_C = 25°C
- Low Forward "On" Voltage – v_T = 1.0 V (Typ) @ 5.0 Amp @ 25°C
- High Surge-Current Capability – I_{TSM} = 100 Amp Peak
- Shorted Emitter Construction

SILICON CONTROLLED RECTIFIERS

8-AMPERE RMS
25 thru 600 VOLTS

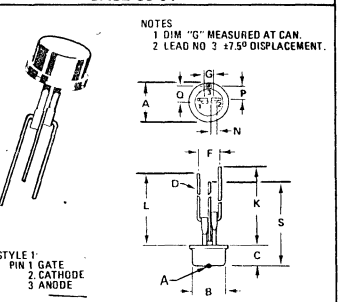


STYLE 1
PIN 1. GATE
2. CATHODE
STUD ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	11.10	–	0.437
C	–	7.87	–	0.310
F	1.78 TYP		0.070 TYP	
G	2.29	2.79	0.090	0.110
J	10.72	11.48	0.422	0.452
K	–	16.76	–	0.660
L	–	15.49	–	0.610

NOTE.
1 DIM "G" MEASURED AT CAN.

2N4167–74
CASE 86-01



NOTES
1 DIM "G" MEASURED AT CAN.
2 LEAD NO 3 ±7.5° DISPLACEMENT.

STYLE 1
PIN 1 GATE
2 CATHODE
3 ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	10.92	–	0.430
B	–	8.89	–	0.350
C	–	5.97	–	0.235
D	0.76	0.86	0.030	0.034
F	4.83	5.33	0.190	0.210
G	2.29	2.79	0.090	0.110
K	33.53	–	1.320	–
L	31.50 TYP		1.240 TYP	
N	1.65	1.91	0.065	0.075
P	3.43	3.68	0.135	0.145
Q	4.57	5.08	0.180	0.200
S	30.48	–	1.20	–

2N4183–90
CASE 87L-01

MAXIMUM RATINGS

(Apply over operating temperature range and for all case types unless otherwise noted)

Rating	Symbol	Value	Unit
*Peak Repetitive Forward and Reverse Blocking Voltage (1) 2N4167, 83,	V_{DRM} or V_{RRM}	25	Volts
2N4168, 84,		50	
2N4169, 85,		100	
2N4170, 86,		200	
2N4171, 87,		300	
2N4172, 88,		400	
2N4173, 89,		500	
2N4174, 90,		600	
Forward Current RMS	$I_{T(RMS)}$	8.0	Amp
*Peak Forward Surge Current (One cycle, 60 Hz, T_J = -40 to +100°C)	I_{TSM}	100	Amp
Circuit Fusing (T_J = -40 to +100°C; t ≤ 8.3 ms)	I^2t	40	A^2s
*Peak Gate Power	P_{GM}	5.0	Watt
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
Peak Gate Voltage (2)	V_{GM}	10	Volts
*Operating Temperature Range	T_J	-40 to +100	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C
Stud Torque		15	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	1.5	2.5*	°C/W
Thermal Resistance, Case to Ambient (See Fig. 11) 2N4183-98	$R\theta_{CA}$	50	–	°C/W

(1) Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage applied exceeds the rated blocking voltage.
(2) Devices should not be operated with a positive bias applied to the gate concurrently with a negative potential applied to the anode.
*Indicates JEDEC Registered Data

7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Current (V_D = Rated V_{DRM} @ T_J = 100°C, gate open)	I_{DRM}	–	–	2.0	mA
*Peak Reverse Blocking Current (V_R = Rated V_{RRM} @ T_J = 100°C, gate open)	I_{RRM}	–	–	2.0	mA
Gate Trigger Current (Continuous dc) (1)	I_{GT}				mA
(V_D = 7.0 Vdc, R_L = 100 Ω)		–	10	30	
*(V_D = 7.0 Vdc, R_L = 100 Ω, T_C = -40°C)		–	–	60	
Gate Trigger Voltage (Continuous dc)	V_{GT}				Volts
(V_D = 7.0 Vdc, R_L = 100 Ω)		–	0.75	1.5	
*(V_D = 7.0 Vdc, R_L = 100 Ω, T_C = -40°C)		–	–	2.5	
*(V_D = 7.0 Vdc, R_L = 100 Ω, T_J = 100°C)		0.2	–	–	
*Forward "On" Voltage (pulsed, 1.0 ms max, duty cycle ≤ 1%) (I_{TM} = 15.7 A)	V_{TM}	–	1.4	2.0	Volts
Holding Current	I_H				mA
(V_D = 7.0 Vdc, gate open)		–	10	30	
*(V_D = 7.0 Vdc, gate open, T_C = -40°C)		–	–	60	
Turn-On Time (t_d + t_r) (I_G = 20 mAdc, I_F = 5.0 Adc, V_D = Rated V_{DRM})	t_{on}	–	1.0	–	μs
Turn-Off Time	t_{off}				μs
(I_F = 5.0 Adc, I_R = 5.0 Adc)		–	15	–	
(I_F = 5.0 Adc, I_R = 5.0 Adc, T_J = 100°C, V_D = Rated V_{DRM}) (dv/dt = 30 V/μs)		–	25	–	
Forward Voltage Application Rate (Exponential) (Gate open, T_J = 100°C, V_D = Rated V_{DRM})	dv/dt	–	50	–	V/μs

(1) For optimum operation, i.e. faster turn-on, lower switching losses, best di/dt capability, recommended I_{GT} = 200 mA minimum.
*Indicates JEDEC Registered Data

7

TYPICAL TRIGGER CHARACTERISTICS

FIGURE 1 – PULSE CURRENT TRIGGERING

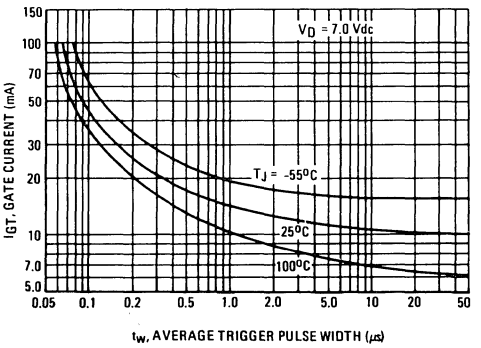
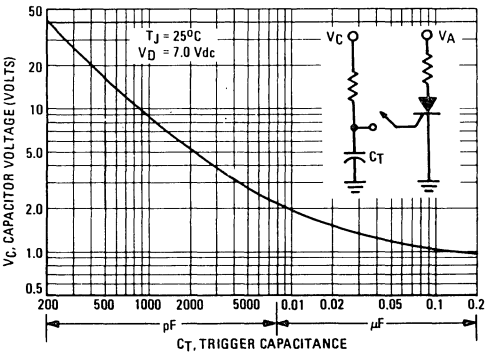


FIGURE 2 – CAPACITIVE DISCHARGE TRIGGERING



CURRENT DERATING

FIGURE 3 – MAXIMUM CASE TEMPERATURE

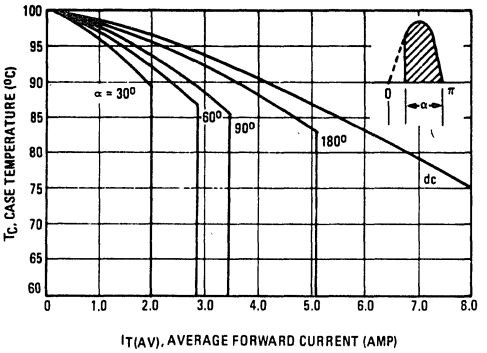


FIGURE 4 – MAXIMUM AMBIENT TEMPERATURE

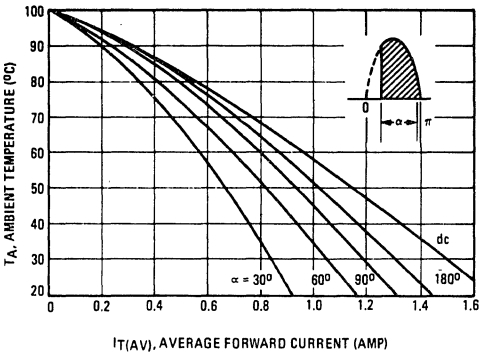


FIGURE 5 – POWER DISSIPATION

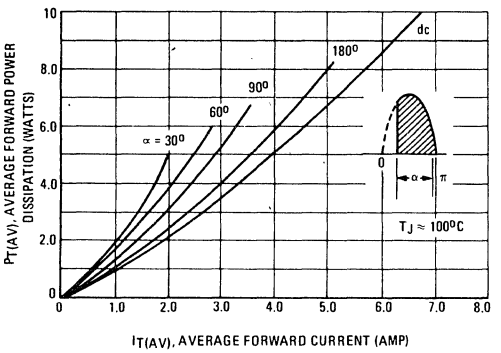


FIGURE 6 – MAXIMUM SURGE CAPABILITY

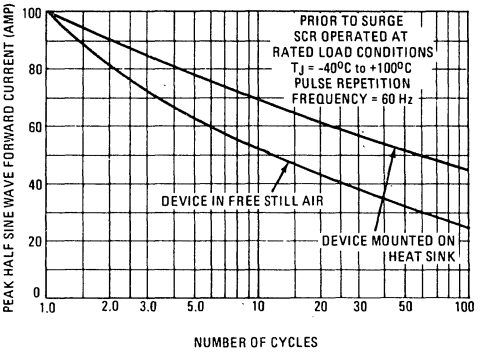


FIGURE 7 – THERMAL RESPONSE

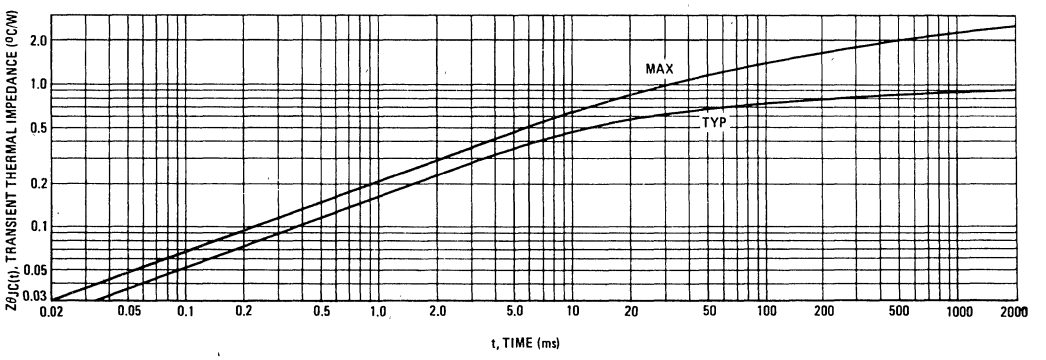


FIGURE 8 – FORWARD VOLTAGE

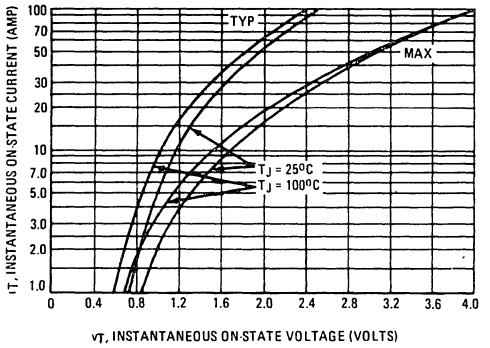


FIGURE 9 – HOLDING CURRENT

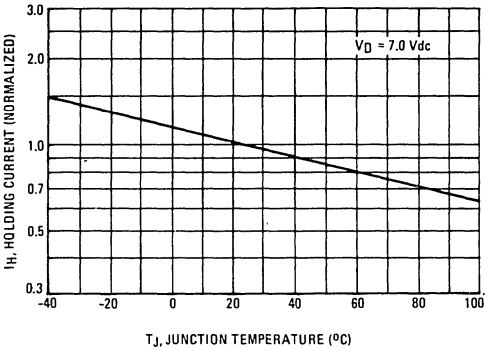


FIGURE 10 – TYPICAL THERMAL RESISTANCE OF PLATES

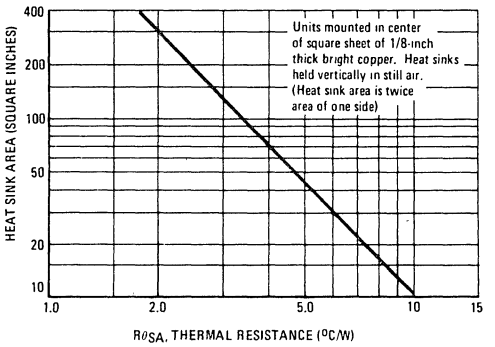
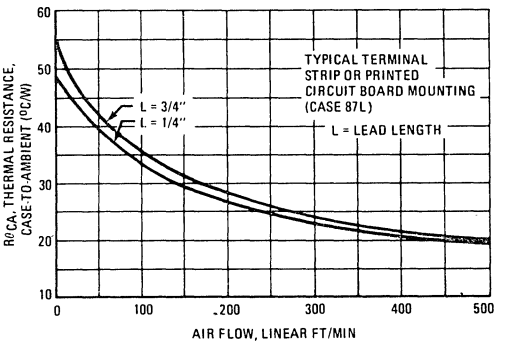


FIGURE 11 – CASE-TO-AMBIENT THERMAL RESISTANCE



2N4199 thru 2N4204

Designers Data Sheet

REVERSE BLOCKING TRIODE THYRISTOR

... fast switching, high-voltage Thyristors especially designed for pulse modulator applications in radar and other similar equipment.

- Guaranteed Limits on All Critical Parameters
- High-Voltage: V_{DRM} = 300 to 800 Volts
- Maximum Turn-On Times Specified – 300 to 400 ns
- Repetitive Pulse Current to 100 Amperes
- Stable Switching Characteristics Over an Operating Temperature Range From -65 to +105°C
- Pulse Repetition Rates as High as 20,000 pps
- Jan Versions Available

SILICON CONTROLLED RECTIFIERS

100 AMPERE PULSE
300 thru 800 VOLTS

Designers Data for "Worst Case" Conditions

The Designers▲ Data Sheets permit the design of most circuits entirely from the information presented. Limit curves – representing boundaries on device characteristics – are given to facilitate "worst case" design.

MAXIMUM RATINGS

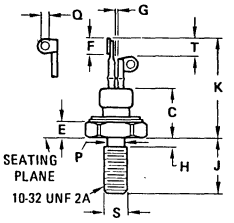
Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (1) (T_J = 105°C)	V_{RRM}	50	Volts
*Peak Forward Blocking Voltage (1) 2N4199 (T_C = 105°C)	V_{DRM}	300	Volts
2N4200		400	
2N4201		500	
2N4202		600	
2N4203		700	
2N4204		800	
Repetitive Peak On-State Current (PW = 3.0 μs, Duty Cycle = 0.6%, T_C = 85°C)	I_{TRM}	100	Amp
Continuous On-State Current (T_C = 65°C)	I_T	5.0	Amp
Current Application Rate (2)	di/dt	5000	A/μs
Peak Forward Gate Power	P_{GFM}	20	Watts
Average Forward Gate Power	$P_{GF(AV)}$	1	Watt
Peak Forward Gate Current	I_{GFM}	5.0	Amp
Peak Gate Voltage – Forward	V_{GFM}	10	Volts
Reverse (3)	V_{GRM}	10	
Operating Junction Temperature Range	T_J		°C
Blocking State		-65 to +105	
Conducting State		-65 to +200	
Storage Temperature Range	T_{stg}	-65 to +200	°C
Stud Torque	–	15	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.0	°C/W

(1) Characterized for unilateral applications where reverse blocking capability is not important. Higher voltage units available upon request. V_{DRM} and V_{RRM} may be applied as a continuous dc voltage for zero or negative gate voltage but positive gate voltage must not be applied concurrently with a negative potential on the anode. When checking blocking capability, do not permit the applied voltage to exceed the rated voltage.
(2) Minimum Gate Trigger Pulse: i_G = 200 mA, PW = 1 μs, t_r = 20 ns.
(3) Do not reverse bias gate during forward conduction if anode current exceeds 10 amperes.
▲Trademark of Motorola Inc.
*JEDEC Registered Data

STYLE 1.
PIN 1. CATHODE
2. GATE
STUD – ANODE



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	12.57	12.83	0.495	0.505
B	10.77	11.10	0.424	0.437
C	–	10.80	–	0.425
D	3.94	4.70	0.155	0.185
E	–	3.56	–	0.140
J	10.16	11.51	0.400	0.453
K	–	21.72	–	0.855
L	–	17.78	–	0.700
N	–	7.11	–	0.280
Q	1.02	1.91	0.040	0.075

CASE 63-03

7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Max	Unit
*Peak Forward and Reverse Blocking Current		17	I_{DRM}	–	2.0	mA
(Rated V_{DRM} and V_{RRM}, T_C = 105°C, gate open)			I_{RRM}	–	2.0	
Gate Trigger Current (Continuous dc)		14	I_{GT}			mA
(Anode Voltage = 7.0 Vdc, R_L = 100 ohms, T_C = 25°C)				–	50	
* (Anode Voltage = 7.0 Vdc, R_L = 100 ohms, T_C = -65°C)				–	100	
Gate Trigger Voltage (Continuous dc)		12	V_{GT}			Volts
* (Anode Voltage = rated V_{DRM}, R_L = 100 ohms, T_C = 105°C)				0.2	–	
(Anode Voltage = 7.0 Vdc, R_L = 100 ohms, T_C = 25°C)				–	1.5	
* (Anode Voltage = 7.0 Vdc, R_L = 100 ohms, T_C = -65°C)				–	2.0	
*Holding Current		18	I_H			mA
(Anode Voltage = 7.0 Vdc, gate open, T_C = 105°C)				3.0	–	
*Forward "On" Voltage		8	V_{TM}			Volts
(I_{TM} = 5 Adc, PW = 1.0 ms max, Duty cycle ≤ 1%)				–		
*Dynamic Forward "On" Voltage		7	V_{TM}			Volts
(0.5 μs after 50% decay point on dynamic forward voltage waveform.)						
Forward Current: 30 A pulse				–	25	
Gate Pulse: at 200 mA, PW = 1.0 μs, t_r = 20 ns						
*Turn-On Time (2) I_{TM} = 30A						ns
Delay Time	All types	1, 9	t_d	–	200	
Rise Time	2N4199 and 2N4200	1, 11	t_r	–	200	
	2N4201			–	150	
	2N4202			–	130	
	2N4203 and 2N4204			–	100	
*Pulse Turn-Off Time		2, 13	t_q			μs
Test Conditions: PFN discharge; Forward Current = 30 A pulse;				–	20	
Reverse Current = 5.0 A, T_C = 85°C, dv/dt = 250 V/μs to Rated V_{DRM};						
Reverse anode voltage during turn-off interval = 0 V;						
Reverse gate bias during turn-off interval = 6.0 V.						
*Forward Voltage Application Rate (Linear Rise of Voltage)		16	dv/dt			V/μs
(T_C = 105°C, gate open, V_D = Rated V_{DRM})				250	–	

*V_{DRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. When checking forward or reverse blocking capability, these devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage. Other voltage units available upon request.

7

TEST CIRCUITS

FIGURE 1 – TURN-ON TIME

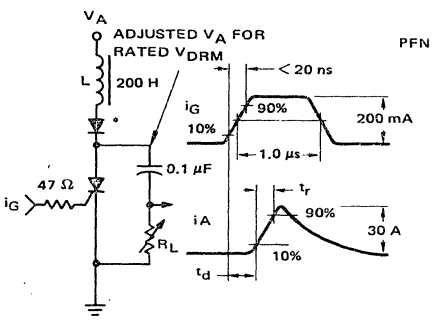
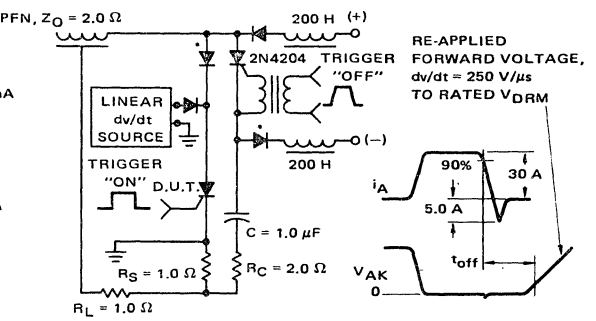


FIGURE 2 – TURN-OFF TIME



*Two 1N4937 fast-recovery diodes in series each shunted by a 180 kΩ resistor.

FIGURE 3 – MAXIMUM ALLOWABLE FORWARD PULSE CURRENT

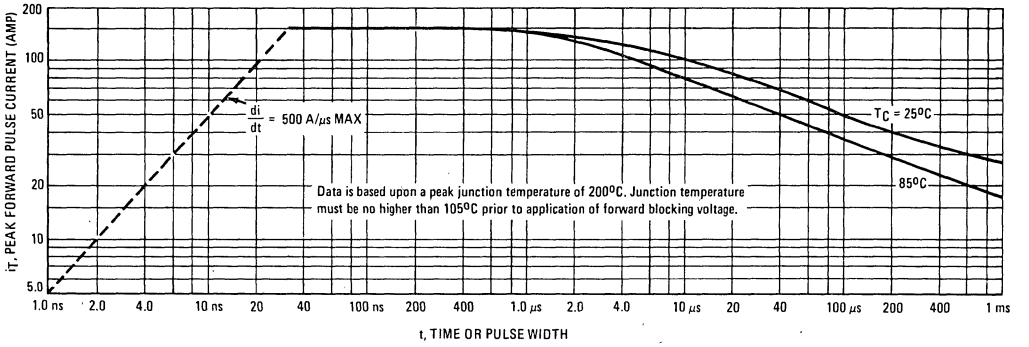


FIGURE 4 – DERATING USING NO SWITCHING LOSSES

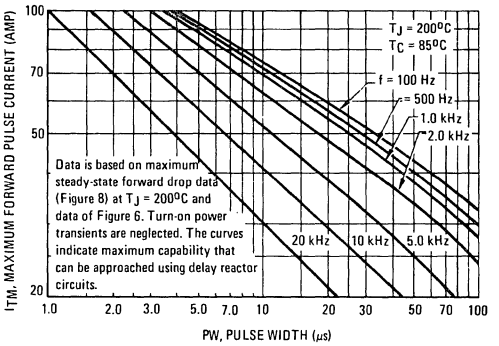
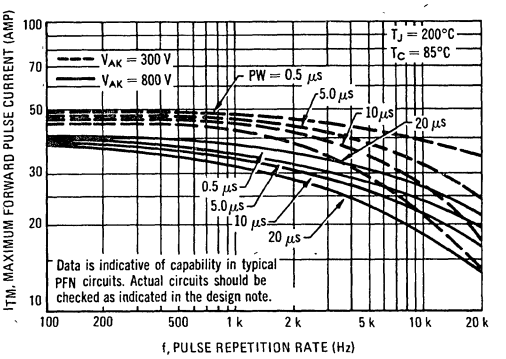


FIGURE 5 – DERATING USING TYPICAL SWITCHING LOSSES



7

DESIGN NOTE

Use of Transient Thermal Resistance Data

A train of periodical power pulses can be represented by the model shown in Fig. A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Fig. 6 was calculated for various duty cycles from:

$$r(t) = D + (1 - D) \cdot r(t_A + t_p) + r(t_A) - r(t_p)$$

To find $\theta_{JC}(t)$ multiply the value obtained from Fig. 6 by the steady-state value $\theta_{JC}(\infty)$. Use 3°C/W for worst-case results; use 2°C/W for typical information.

DESIGN EXAMPLE

A 2N4199 discharging a PFN, transient power pulse shown in Fig. C.

Conditions: V_{AK} = 150 V., I_{PK} = 44 A., f = 5000 Hz.

Determine: ΔT

Method 1: (See Fig. A) $P_A t_A$ is chosen to have the same energy as the actual power pulse, i.e.: the area under the curves are equal. P_A equals the peak of the actual power pulse. At a pulse repetition frequency of 5000 Hz and t_A = 2.14 μs (D = 0.0107); the reading on Fig. 6 is 0.039.

$\therefore \Delta T = r(t)\, R_{\theta JC}(\infty)\, P_A$ = (0.039) (3) (1000) = 120°C.

Method 2: For a power waveform where the time of the peak power is short compared to the total transient, the foregoing method results in an overly large safety factor. A pulse model closer to the real case is shown in Fig. B. Using the transient thermal resistance information for D = 0 in Fig. 6, $\Delta T(t_4)$ and $\Delta T(t_5)$ can be evaluated from

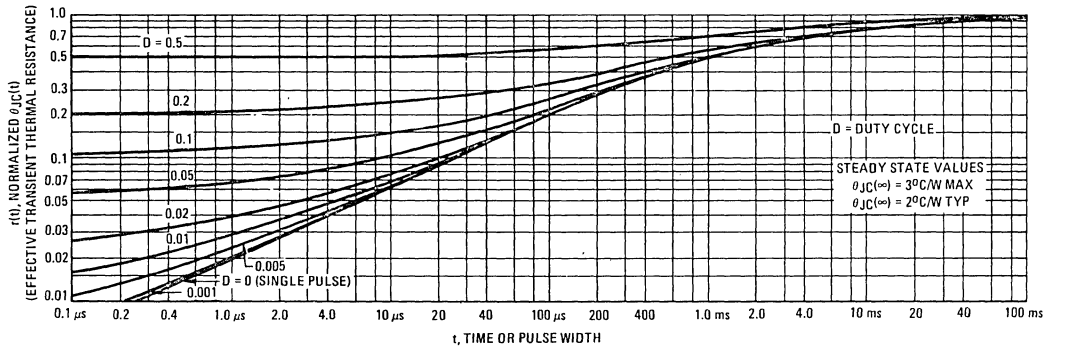
$$\Delta T(t_4) = [P_1\,[r(T_1) + (1 - D_1) \cdot r(T + T_1) + D - r(T)] + P_2[(1 - D_2) \cdot r(T) + D_2 - r(T - T_2)]\,]\, R_{\theta JC}(\infty)$$

$$\Delta T(t_5) = [P_1\,[r(T_1 + T_2) + (1 - D_1) \cdot r(T + T_1 + T_2) - r(T + T_2) - r(T_2)] + P_2\,[r(T_2) + (1 - D_2) \cdot r(T + T_2) + D_2 - r(T)]\,]\, R_{\theta JC}(\infty)$$

The two results are compared; the one with higher value is taken for worst-case design. For the problem, values for the equivalent pulses of Fig. B are P_1 = 1000 W, P_2 = 700 W, T_1 = 1.05 μs, T_2 = 1.55 μs, $D_1 = 5.25(10^{-3})$, $D_2 = 7.75(10^{-3})$.

(CONTINUED)

FIGURE 6 – NORMALIZED EFFECTIVE TRANSIENT THERMAL RESISTANCE



FORWARD "ON" VOLTAGE DATA

FIGURE 7 – TYPICAL DYNAMIC FORWARD "ON" VOLTAGE

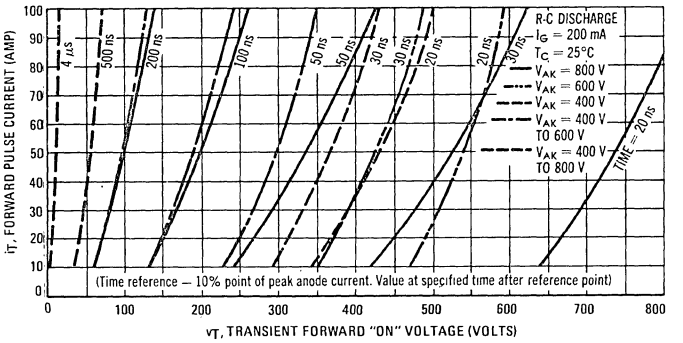
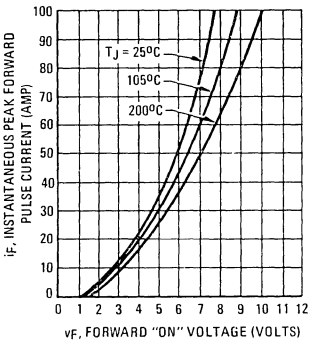


FIGURE 8 – MAXIMUM STEADY-STATE



DESIGN NOTE CONTINUED

$\Delta T(t_4) = [\ 1000\ [0.0205 + (1 - 5.25 \cdot 10^{-3})\ 0.27 + 5.25 \cdot 10^{-3} - 0.27]$
$+ 700\ [(1 - 7.75 \cdot 10^{-3})\ 0.27 + 7.75 \cdot 10^{-3} - 0.27]\ ]\ 3 = 93.51^{\circ}C$

$\Delta T(t_5) = [\ 1000\ [0.032 + (1 - 5.25 \cdot 10^{-3})\ 0.27 + 5.25 \cdot 10^{-3} - 0.27 - 0.0205]$
$+ 700\ [0.025 + (1 - 7.75 \cdot 10^{-3})\ 0.27 + 7.75 \cdot 10^{-3} - 0.27]\ ]\ 3 = 105.6^{\circ}C$

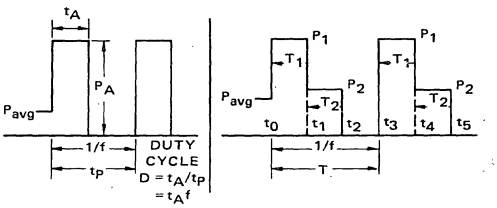


FIGURE A – SIMPLE MODEL FIGURE B – MORE ACCURATE MODEL

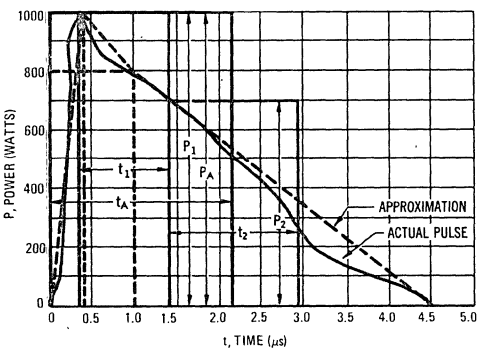


FIGURE C – AN ACTUAL TRANSIENT POWER PULSE

SWITCHING CHARACTERISTICS

FIGURE 9 – DELAY TIME

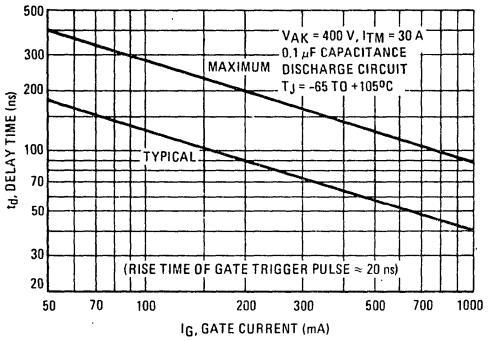


FIGURE 11 – CURRENT RISE TIME

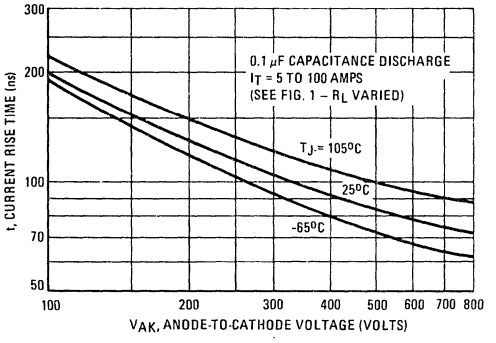
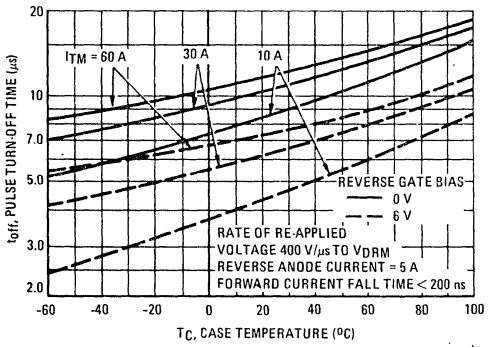


FIGURE 13 – TYPICAL TURN-OFF TIME



TRIGGERING CHARACTERISTICS

FIGURE 10 – TYPICAL PULSE TRIGGER CHARGE/CURRENT

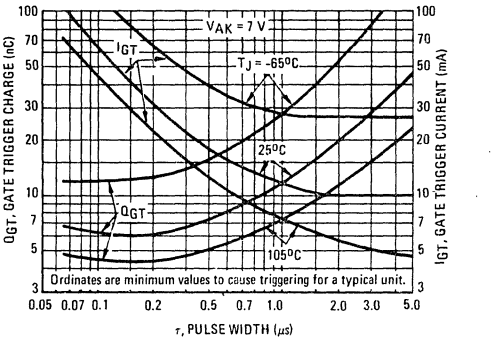


FIGURE 12 – DC GATE TRIGGER VOLTAGE

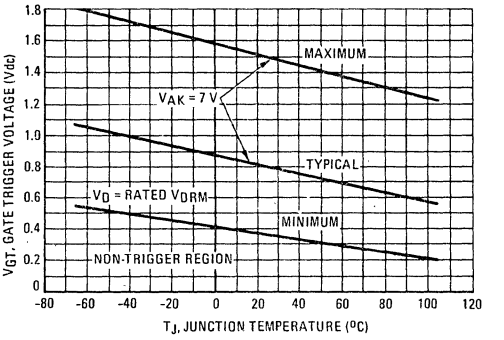


FIGURE 14 – DC GATE TRIGGER CURRENT

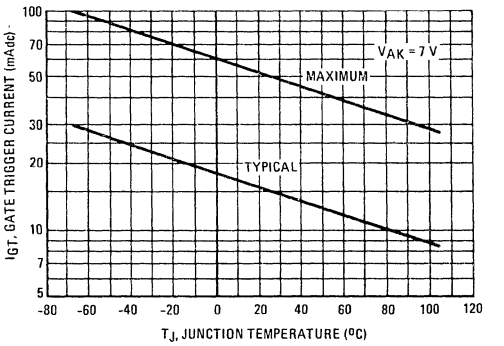


FIGURE 15 – TYPICAL BLOCKING VOLTAGE DERATING

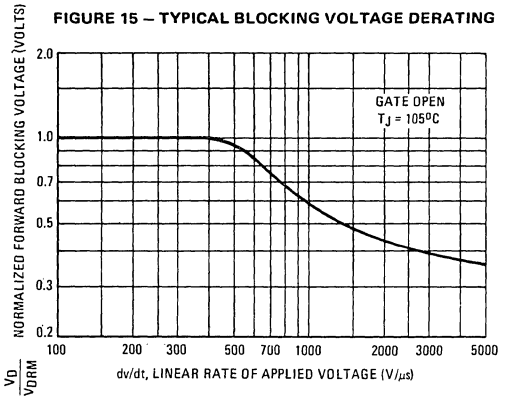


FIGURE 16 – TYPICAL LINEAR dv/dt CAPABILITY

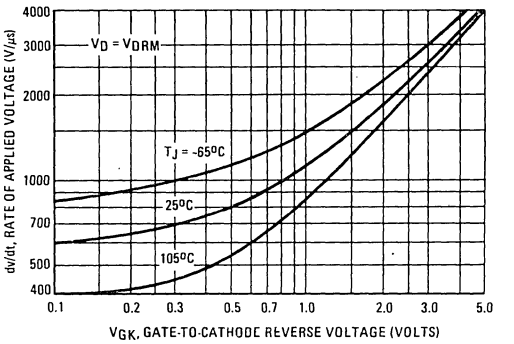


FIGURE 17 – FORWARD BLOCKING CURRENT

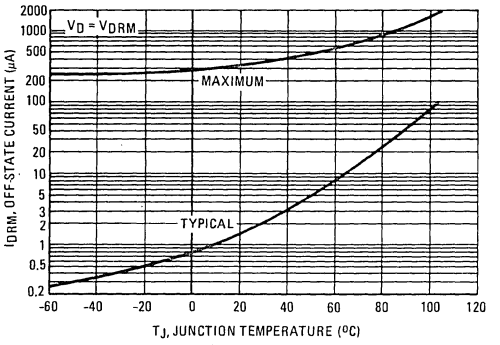


FIGURE 18 – HOLDING CURRENT

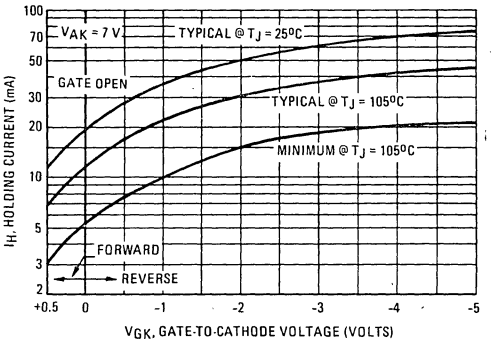


FIGURE 19 – TYPICAL ANODE-TO-CATHODE CAPACITANCE

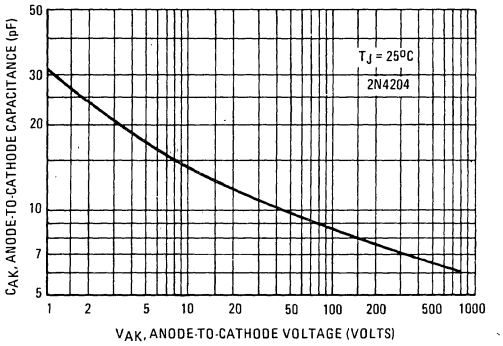
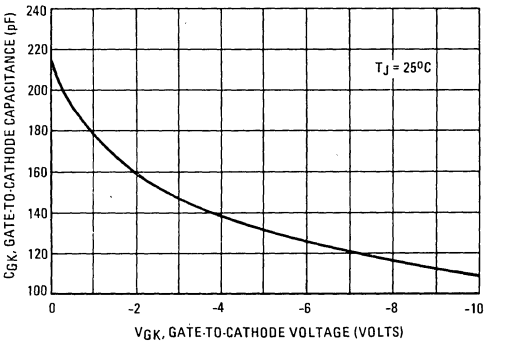


FIGURE 20 – TYPICAL GATE-TO-CATHODE CAPACITANCE



7

2N4212 thru 2N4216

REVERSE BLOCKING TRIODE THYRISTOR

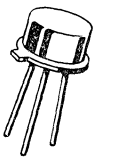
. . . all-diffused PNPN devices designed for operation in mA/μA signal or detection circuits.

- Low-Level Gate Characteristics – I_{GT} = 100 μA Max @ 25°C
- Low Holding Current – I_{HX} = 3.0 mA Max @ 25°C
- Anode Common To Case
- Glass-to-Metal Bond for Maximum Hermetic Seal

SILICON CONTROLLED RECTIFIERS

PNPN

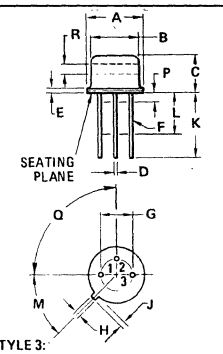
1.6 AMPERES RMS
25–200 VOLTS



***MAXIMUM RATINGS** (T_J = 125°C unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Peak Repetitive Forward and Reverse Blocking Voltage	V_{DRM} or		Volt
2N4212	V_{RRM}	25	
2N4213		50	
2N4214		100	
2N4215		150	
2N4216		200	
Forward Current RMS (All Conduction Angles)	$I_{T(RMS)}$	1.6	Amp
Peak Surge Current (One Cycle, 60 Hz) No Repetition until Thermal Equilibrium is Restored	I_{TSM}	15	Amp
Peak Gate Power – Forward	P_{GFM}	0.1	Watt
Average Gate Power – Forward	$P_{GF(AV)}$	0.01	Watt
Peak Gate Current – Forward	I_{GFM}	0.1	Amp
Peak Gate Voltage – Forward	V_{GFM}	6.0	Volt
Reverse	V_{GRM}	6.0	
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Solder Temperature (> 1/16.. from case, 10 sec. max)	–	+230	°C

*JEDEC Registered Values.



STYLE 3:
PIN 1. CATHODE
2. GATE
3. ANODE (CONNECTED TO CASE)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

All JEDEC dimensions and notes apply.

CASE 79-02
TO -39

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted, R_{GK} = 1000 ohms)

Characteristics	Symbol	Min	Max	Unit
*Peak Forward and Reverse Blocking Current (Rated V_{DRM} and V_{RRM}, T_J = 125°C)	I_{DRM} or I_{RRM}	–	200	μA
*Forward "On" Voltage (I_{TM} = 1.0 Adc peak)	V_{TM}	–	1.5	Volt
Gate Trigger Current (Note 2) (V_D = 7.0 V, R_L = 100 ohms)	I_{GT}			μAdc
(T_C = 25°C)		–	100	
(T_C = -65°C)		–	300	
Gate Trigger Voltage	V_{GT}			Volt
(V_D = 7.0 V, R_L = 100 ohms, T_C = 25°C)		–	0.8	
*(V_D = 7.0 V, R_L = 100 ohms, T_C = -65°C)		–	1.0	
*(V_D = Rated V_{DRM}, R_L = 100 ohms, T_J = 125°C)		0.1	–	
Holding Current (V_D = 7.0 V) T_C = 25°C	I_{HX}		3.0	mA
*T_C = -65°C			7.0	
Turn-On Time	t_{on}	Circuit dependent, consult manufacturer		
Turn-Off Time	t_{off}			

* JEDEC Registered Values

Notes: 1. V_{DRM} and V_{RRM} can be applied for all types on a continuous dc basis without incurring damage.

2. R_{GK} current is not included in measurement.

Thyristor devices shall not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

Thyristor devices shall not have a positive bias applied to the gate concurrently with a negative potential applied to the anode.

FIGURE 1 – CASE TEMPERATURE vs CURRENT

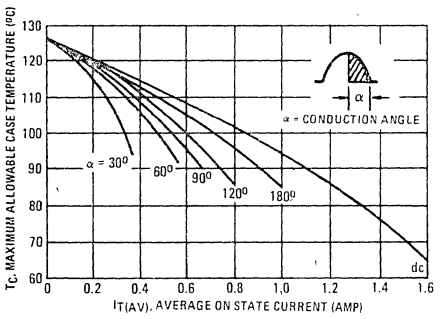
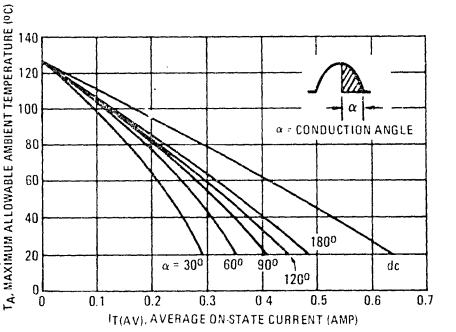
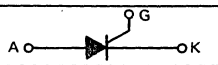


FIGURE 2 – AMBIENT TEMPERATURE vs CURRENT



2N4441 thru 2N4444



REVERSE BLOCKING TRIODE THYRISTORS

. . . designed for high-volume consumer phase-control applications such as motor speed, temperature, and light controls and for switching applications in ignition and starting systems, voltage regulators, vending machines, and lamp drivers requiring:

- Small, Rugged, Thermopad ▲ Construction – for Low Thermal Resistance, High Heat Dissipation, and Durability.
- Practical Level Triggering and Holding Characteristics @ 25°C
  I_{GT} = 7.0 mA (Typ)
  I_H = 6.0 mA (Typ)
- Low "On" Voltage – V_{TM} = 1.0 Volt (Typ) @ 5.0 Amp @ 25°C
- High Surge Current Rating – I_{TSM} = 80 Amp

SILICON CONTROLLED RECTIFIERS

8.0 AMPERES RMS
50 thru 600 VOLTS

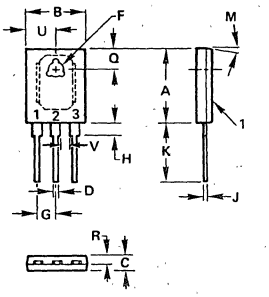
MAXIMUM RATING (T_J = 100°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage (Note1) 2N4441	V_{DRM} V_{RRM}	50	Volts
2N4442		200	
2N4443		400	
2N4444		600	
*Non-Repetitive Peak Reverse Blocking Voltage (t = 5.0 ms (max) duration)	V_{RSM}		Volts
2N4441		75	
2N4442		300	
2N4443		500	
2N4444		700	
*RMS On-State Current (All Conduction Angles)	$I_{T(RMS)}$	8.0	Amp
Average On-State Current, T_C = 73°C	$I_{T(AV)}$	5.1	Amp
*Peak Non-Repetitive Surge Current (1/2 cycle, 60 Hz preceded and followed by rated current and voltage)	I_{TSM}	80	Amp
Circuit Fusing (T_J = –40 to +100°C; t = 1.0 to 8.3 ms)	I^2t	25	A^2s
*Peak Gate Power	P_{GM}	5.0	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current	I_{GM}	2.0	Amp
*Peak Reverse Gate Voltage	V_{RGM}	10	Volts
*Operating Junction Temperature Range	T_J	-40 to +100	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C
Mounting Torque (6-32 screw) (Note 2)	–	8.0	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	–	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	40	–	°C/W

*Indicates JEDEC Registered Data.
▲Trademark of Motorola Inc.
Notes 1, 2, See page 2



STYLE 1:
PIN 1. CATHODE
2. ANODE
3. GATE

NOTES:
1. DIM "D" UNCONTROLLED IN ZONE "H"
2. DIM "F" DIA THRU
3. HEAT SINK CONTACT AREA (BOTTOM)
4. LEADS WITHIN 0.005" RAD OF TRUE POSITION (TP) AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	90° TYP		90° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255
V	2.03	–	0.080	–

CASE 90-05

7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (V_D = Rated V_{DRM}, T_J = 100°C, gate open)	I_{DRM}	–	–	2.0	mA
Peak Reverse Blocking Current (V_D = Rated V_{RRM}, T_J = 100°C, gate open)	I_{RRM}	–	–	2.0	mA
Gate Trigger Current (Continuous dc) (V_D = 7.0 Vdc, R_L = 100 Ohms)	I_{GT}				mA
T_C = 25°C		–	7.0	30	
* T_C = -40°C				60	
Gate Trigger Voltage (Continuous dc) (V_D = 7.0 Vdc, R_L = 100 Ohms)	V_{GT}				Volts
T_C = 25°C		–	0.75	1.5	
(V_D = 7.0 Vdc, R_L = 100 Ohms) T_C = -40°C		–	–	2.5	
(V_D = Rated V_{DRM}, R_L = 100 Ohms) T_J = 100°C		0.2	–	–	
Peak On-State Voltage (Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0%)	V_{TM}				Volts
(I_{TM} = 5.0 A peak)		–	1.0	1.5	
* (I_{TM} = 15.7 A peak)		–	–	2.0	
Holding Current (V_D = 7.0 Vdc, gate open)	I_H				mA
T_C = 25°C		–	6.0	40	
* T_C = -40°C		–	–	70	
Gate Controlled Turn-On Time (I_{TM} = 5.0 A, I_{GT} = 20 mA, V_D = Rated V_{DRM})	t_{gt}	–	1.0	–	μs
Circuit Commutated Turn-Off Time	t_q				μs
(I_{TM} = 5.0 A, I_R = 5.0 A)		–	15	–	
(I_{TM} = 5.0 A, I_R = 5.0 A, T_J = 100°C)		–	20	–	
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, T_J = 100°C, Gate Open)	dv/dt	–	50	–	V/μs

*Indicates JEDEC Registered Data

Note 1. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.

Note 2. Torque rating applies with use of torque washer (Shakeproof WD19522 #6 or equivalent). Mounting torque in excess of 8 in. lbs. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common.

For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +225°C.

FIGURE 1 – ON-STATE CHARACTERISTICS

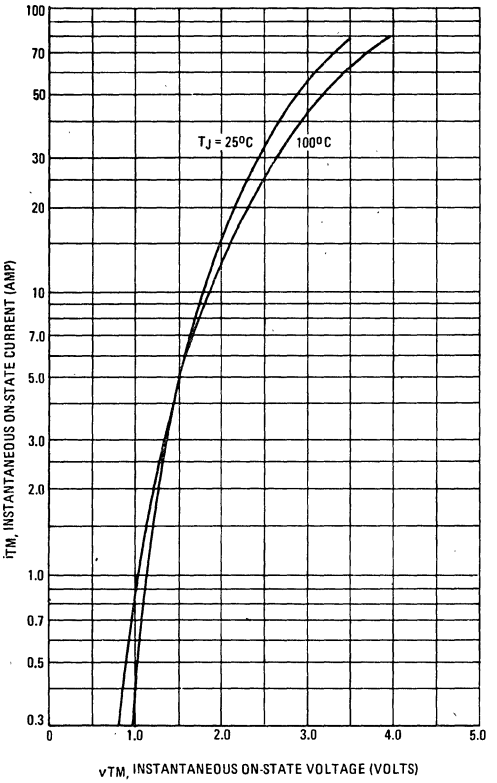


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

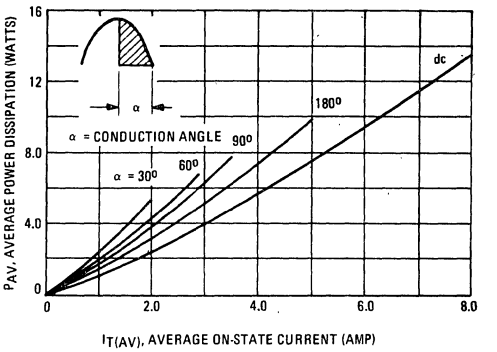
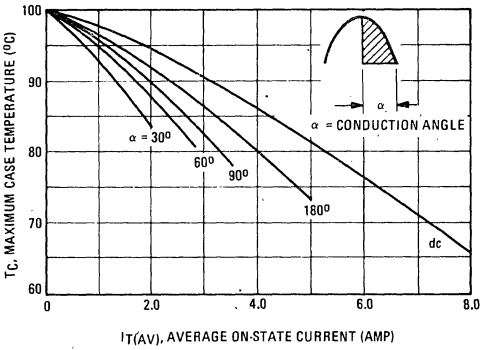


FIGURE 3 – AVERAGE CURRENT DERATING



7

FIGURE 4 – THERMAL RESPONSE

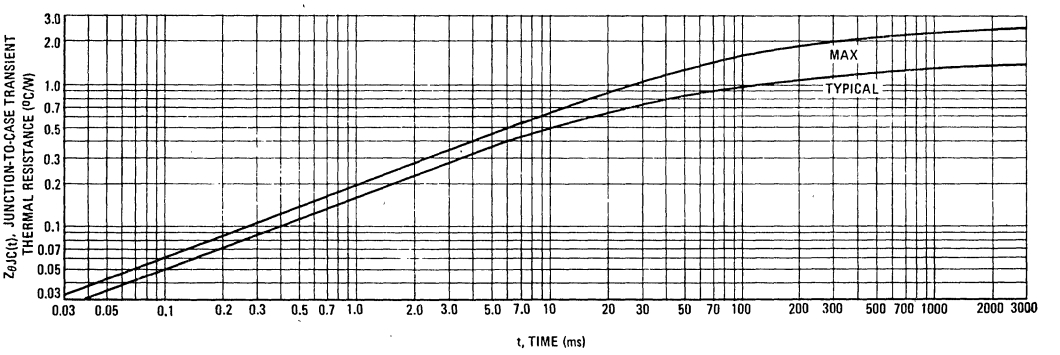


FIGURE 5 – MAXIMUM NON-REPETITIVE SURGE CURRENT

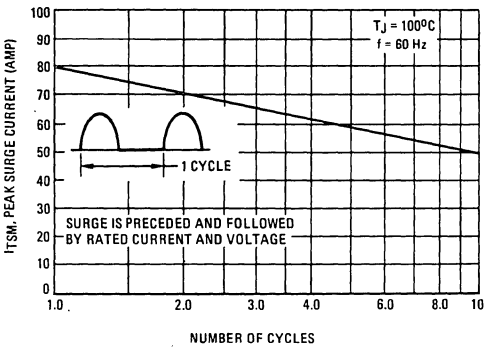


FIGURE 6 – TYPICAL HOLDING CURRENT

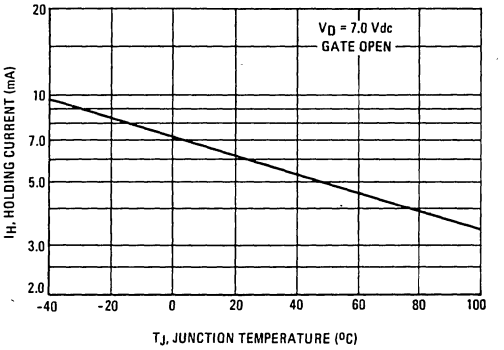


FIGURE 7 – TYPICAL GATE TRIGGER CURRENT

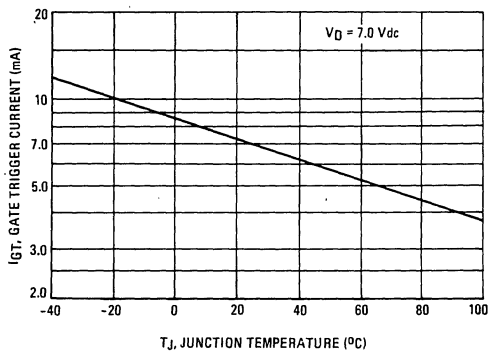
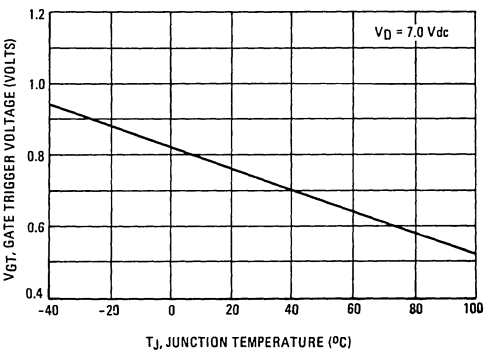
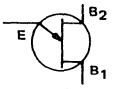


FIGURE 8 – TYPICAL GATE TRIGGER VOLTAGE



7

2N4851 thru 2N4853

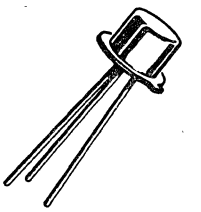


SILICON UNIJUNCTION TRANSISTOR

... designed for pulse and timing circuits, sensing circuits, and thyristor trigger circuits.

- Low Peak-Point Current – I_P = 0.4 μA Max
- Low Emitter Reverse Current – I_{EO} = 50 nA Max
- Fast Switching – 1.0 MHz Min

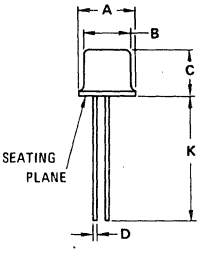
PN UNIJUNCTION TRANSISTORS



***MAXIMUM RATINGS** (T_A = 25°C unless otherwise noted)

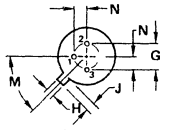
Rating	Symbol	Value	Unit
RMS Power Dissipation (1)	P_D	300	mW
RMS Emitter Current	I_e	50	mA
Peak-Pulse Emitter Current (2)	i_e	1.5	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage (3)	V_{B2B1}	35	Volts
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data
(1) Derate 3.0 mW/°C increase in ambient temperature
(2) Duty cycle ≤ 1%, PRR = (see figure 6)
(3) Based upon power dissipation at T_A = 25°C



NOTE:
1. PIN 3 CONNECTED TO CASE.

STYLE 1:
PIN 1. EMITTER
2. BASE 1
3. BASE 2



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.48	0.016	0.019
G	2.54 TYP		0.100 TYP	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
M	45° TYP		45° TYP	
N	1.27 TYP		0.050 TYP	

CASE 22A - 01
(TO-18 Except for Lead Position)

FIGURE 1 – UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

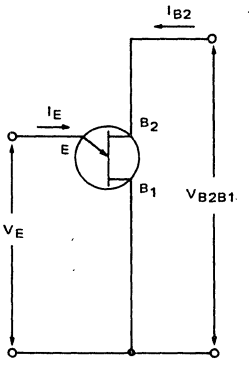
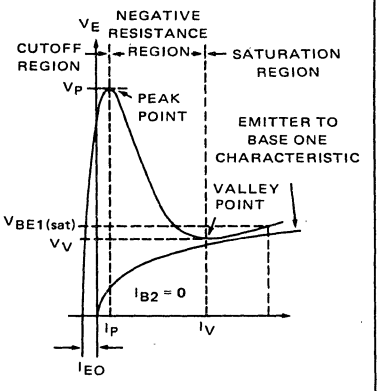


FIGURE 2 – STATIC EMITTER CHARACTERISTICS CURVES



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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Rating		Figure No.	Symbol	Min	Typ	Max	Unit
*Intrinsic Standoff Ratio (1)		4, 8	η				—
(V_{B2B1} = 10 V)	2N4851			0.56	–	0.75	
	2N4852, 2N4853			0.70	–	0.85	
*Interbase Resistance		11, 12	r_{BB}				k ohms
(V_{B2B1} = 3.0 V, I_E = 0)				4.7	–	9.1	
*Interbase Resistance Temperature Coefficient		12	α_{BB}				%/°C
(V_{B2B1} = 3.0 V, I_E = 0, T_A = -65 to +125°C)				0.2	–	0.8	
Emitter Saturation Voltage (2)			$V_{EB1(sat)}$				Volts
(V_{B2B1} = 10 V, I_E = 50 mA)				–	2.5	–	
Modulated Interbase Current			$I_{B2(mod)}$				mA
(V_{B2B1} = 10 V, I_E = 50 mA)				–	15	–	
*Emitter Reverse Current		7	I_{EB2O}				μA
(V_{B2E} = 30 V, I_{B1} = 0)	2N4851, 2N4852			–	–	0.1	
	2N4853			–	–	0.05	
*Peak-Point Emitter Current		9, 10	I_P				μA
(V_{B2B1} = 25 V)	2N4851, 2N4852			–	–	2.0	
	2N4853			–	–	0.4	
*Valley-Point Current (2)		13, 14	I_V				mA
(V_{B2B1} = 20 V, R_{B2} = 100 ohms)	2N4851			2.0	–	–	
	2N4852			4.0	–	–	
	2N4853			6.0	–	–	
*Base-One Peak Pulse Voltage	2N4851	3, 17	V_{OB1}	3.0	–	–	Volts
	2N4852			5.0	–	–	
	2N4853			6.0	–	–	
*Maximum Frequency of Oscillation		5	$f_{(max)}$	1.0	1.25	–	MHz

*Indicates JEDEC Registered Data.

(1) η, Intrinsic standoff ratio, is defined in terms of the peak-point voltage, V_P, by means of the equation: $V_P = \eta V_{B2B1} + V_F$, where V_F is about 0.49 volt at 25°C @ I_F = 10 μA and decreases with temperature at about 2.5 mV/°C. The test circuit is shown in Figure 4. Components R_1, C_1, and the UJT form a relaxation oscillator; the remaining circuitry serves as a peak-voltage detector. The forward drop of Diode D_1 compensates for V_F. To use, the "cal" button is pushed, and R_3 is adjusted to make the current meter, M_1, read full scale. When the "cal" button is released, the value of η is read directly from the meter, if full scale on the meter reads 1.0.

(2) Use pulse techniques: PW ≈ 300 μs, duty cycle ⩽ 2.0% to avoid internal heating, which may result in erroneous readings.

FIGURE 3 – V_{OB1} TEST CIRCUIT

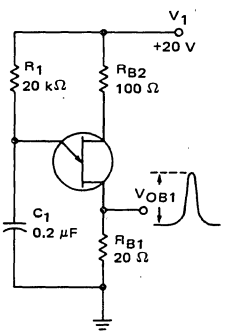
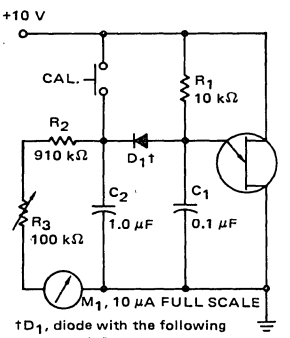


FIGURE 4 – η TEST CIRCUIT



†D_1, diode with the following characteristics:

V_F = 0.49 V @ I_F = 10 μA

I_R ⩽ 2.0 μA @ V_R = 20 V

FIGURE 5 – $f_{(max)}$ TEST CIRCUIT

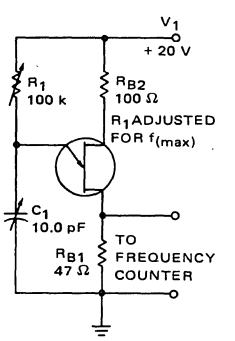
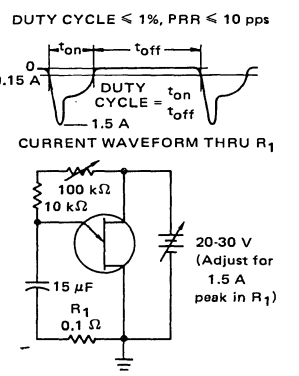


FIGURE 6 – PRR TEST CIRCUIT AND WAVEFORM



TYPICAL CHARACTERISTICS

FIGURE 7 – EMITTER REVERSE CURRENT

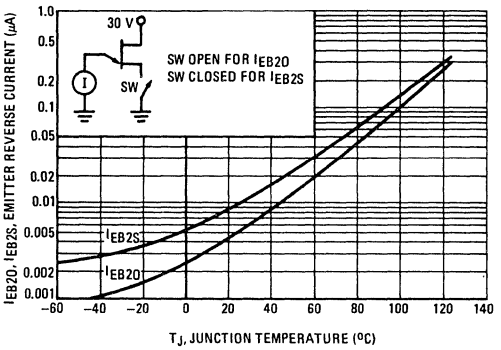
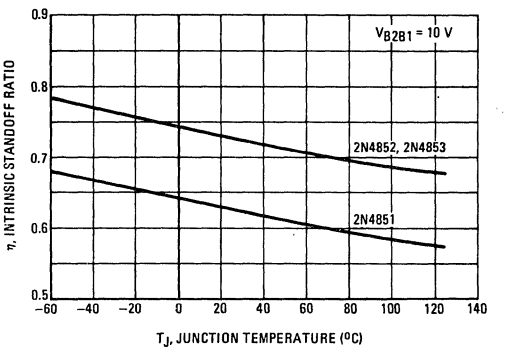


FIGURE 8 – INTRINSIC STANDOFF RATIO



PEAK POINT CURRENT

FIGURE 9 – EFFECT OF VOLTAGE

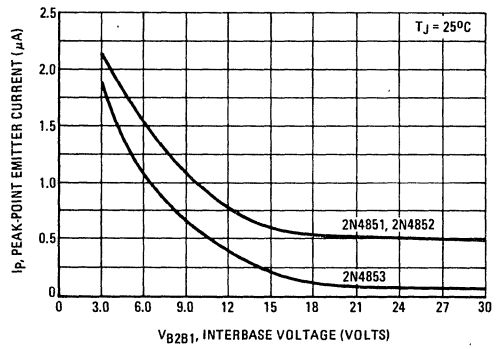
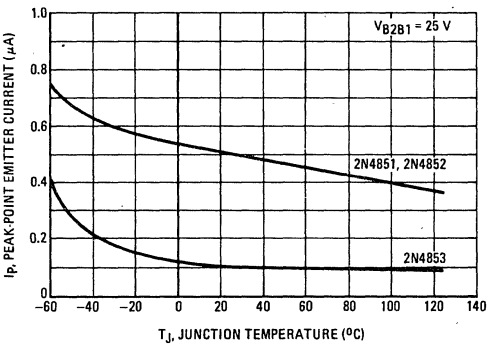


FIGURE 10 – EFFECT OF TEMPERATURE



INTERBASE RESISTANCE

FIGURE 11 – EFFECT OF VOLTAGE

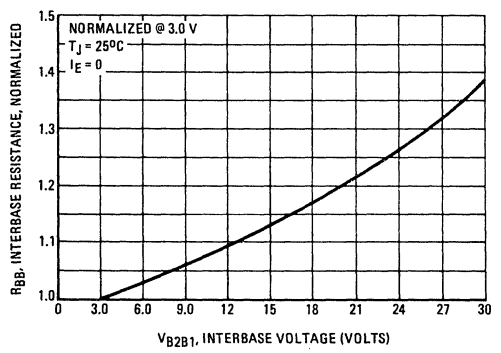
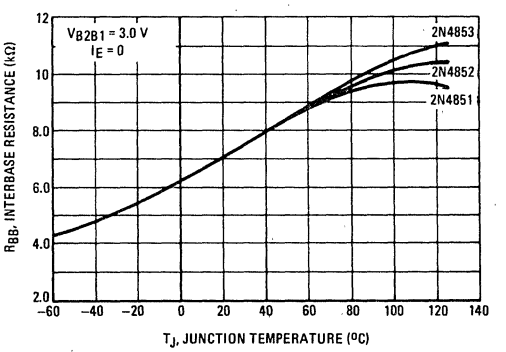


FIGURE 12 – EFFECT OF TEMPERATURE



7

TYPICAL CHARACTERISTICS

VALLEY CURRENT

FIGURE 13 – EFFECT OF VOLTAGE

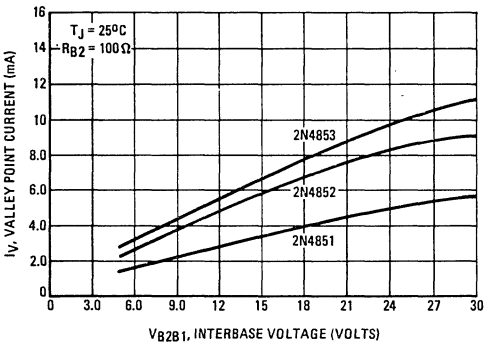
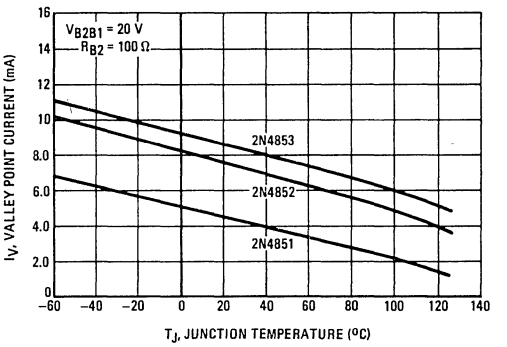


FIGURE 14 – EFFECT OF TEMPERATURE



VALLEY VOLTAGE

FIGURE 15 – EFFECT OF VOLTAGE

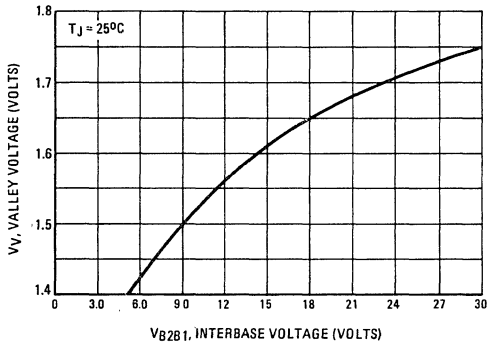


FIGURE 16 – EFFECT OF TEMPERATURE

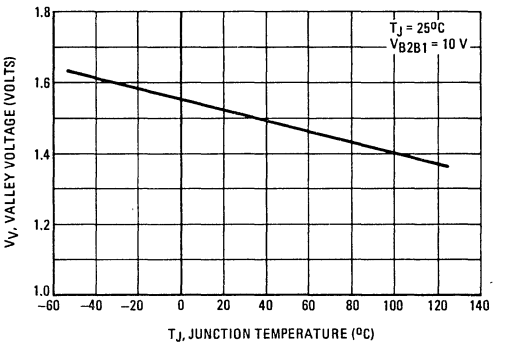
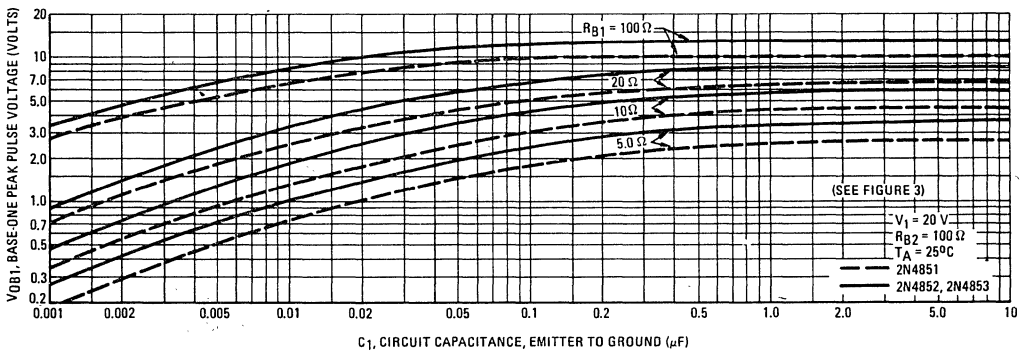
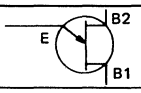


FIGURE 17 – OUTPUT VOLTAGE



2N4870
2N4871

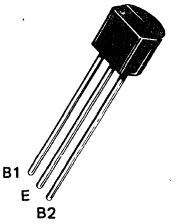


SILICON UNIJUNCTION TRANSISTORS

. . .designed for pulse and timing circuits, sensing circuits, and thyristor trigger circuits. These devices feature:

- Low Peak Point Current – 1.0 μA Typical
- Low Emitter Reverse Current – 5.0 nA Typical
- Passivated Surface for Reliability and Uniformity
- One-Piece Injection-Molded Unibloc‡ Plastic Package for Economy and Reliability

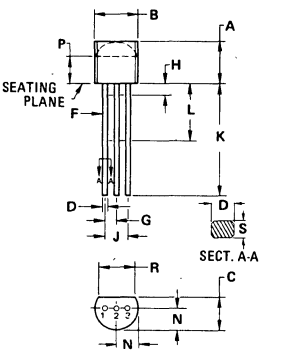
PN UNIJUNCTION TRANSISTORS



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
RMS Power Dissipation*	P_D*	300	mW
RMS Emitter Current	I_e	50	mA
Peak-Pulse Emitter Current**	i_e**	1.5	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage†	V_{B2B1}†	35	Volts
Operating Junction Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

*Derate 3.0 mW/°C increase in ambient temperature.
**Duty cycle ≤ 1%, PRR = 10 PPS (see Figure 5).
†Based upon power dissipation at T_A = 25°C.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02

FIGURE 1 – UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

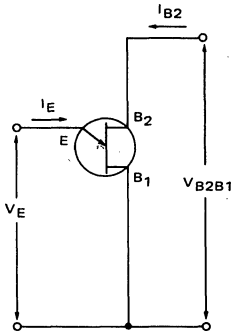
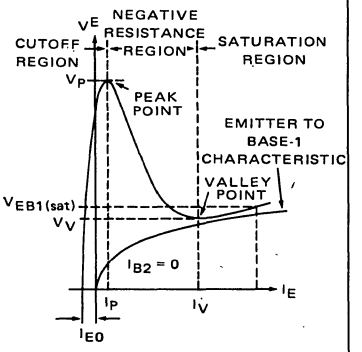


FIGURE 2 – STATIC EMITTER CHARACTERISTICS CURVES



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio* (V_{B2B1} = 10 V)	2N4870	4, 7	η*	0.56	–	0.75	–
	2N4871			0.70	–	0.85	
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)		10,11	R_{BB}	4.0	6.0	9.1	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = -65 to +125°C)		11	αR_{BB}	0.10	–	0.90	%/°C
Emitter Saturation Voltage** (V_{B2B1} = 10 V, I_E = 50 mA)			$V_{EB1(sat)}$**	–	2.5	–	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)			$I_{B2(mod)}$	–	15	–	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)		6	I_{EB2O}	–	0.005	1.0	μA
Peak-Point Emitter Current (V_{B2B1} = 25 V)		8, 9	I_P	–	1.0	5.0	μA
Valley-Point Current** (V_{B2B1} = 20 V, R_{B2} = 100 ohms)	2N4870	12, 13	I_V**	2.0	5.0	–	mA
	2N4871			4.0	7.0	–	
Base-One Peak Pulse Voltage	2N4870	3, 16	V_{OB1}	3.0	6.0	–	Volts
	2N4871			5.0	8.0	–	

* η, Intrinsic standoff ratio, is defined in terms of the peak-point voltage, V_P, by means of the equation: $V_p = \eta V_{B2B1} + V_F$, where V_F is about 0.49 volt at 25°C @ I_F = 10 μA and decreases with temperature at about 2.5 mV/°C. The test circuit is shown in Figure 4. Components R_1, C_1, and the UJT form a relaxation oscillator; the remaining circuitry serves as a peak-voltage detector. The forward drop of Diode D_1 compensates for V_R, To use, the "cal" button is pushed, and R_3 is adjusted to make the current meter, M_1, read full scale. When the "cal" button is released, the value of η is read directly from the meter, if full scale on the meter reads 1.0.

** Use pulse techniques: PW ≈ 300 μs, duty cycle ≤ 2.0% to avoid internal heating, which may result in erroneous readings.

FIGURE 3 – V_{OB1} TEST CIRCUIT

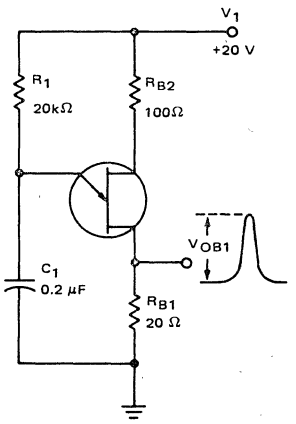
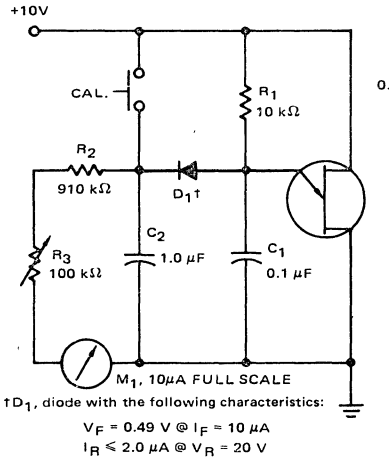
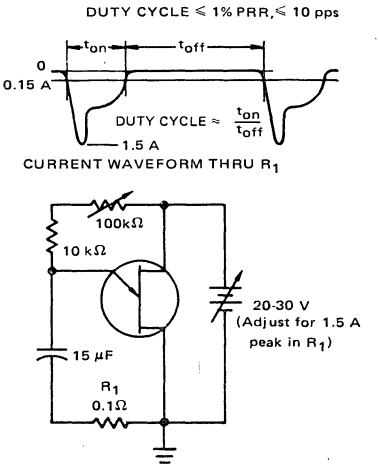


FIGURE 4 – η TEST CIRCUIT



†D_1, diode with the following characteristics:
V_F = 0.49 V @ I_F = 10 μA
$I_R \leq$ 2.0 μA @ V_R = 20 V

FIGURE 5 – PRR TEST CIRCUIT AND WAVEFORM



TYPICAL CHARACTERISTICS

FIGURE 6 – EMITTER REVERSE CURRENT

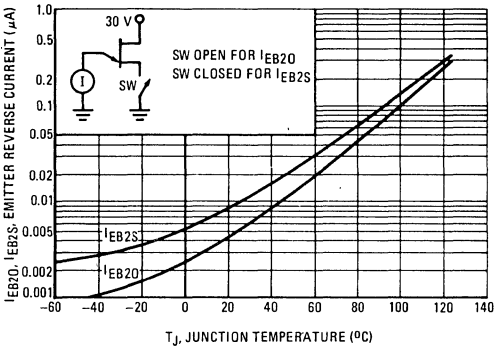
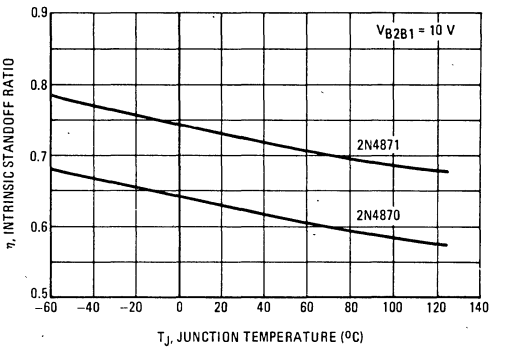


FIGURE 7 – INTRINSIC STANDOFF RATIO



PEAK POINT CURRENT

FIGURE 8 – EFFECT OF VOLTAGE

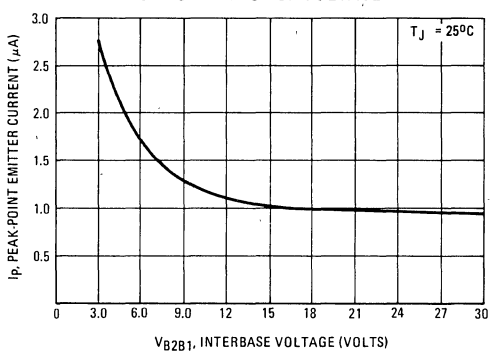
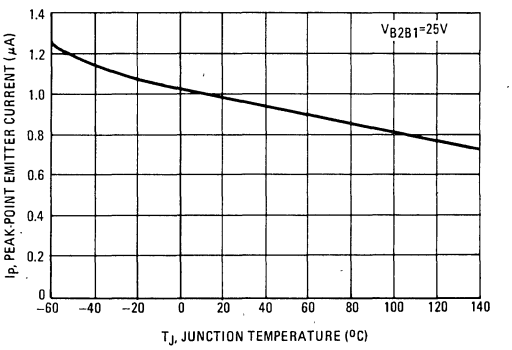


FIGURE 9 – EFFECT OF TEMPERATURE



INTERBASE RESISTANCE

FIGURE 10 – EFFECT OF VOLTAGE

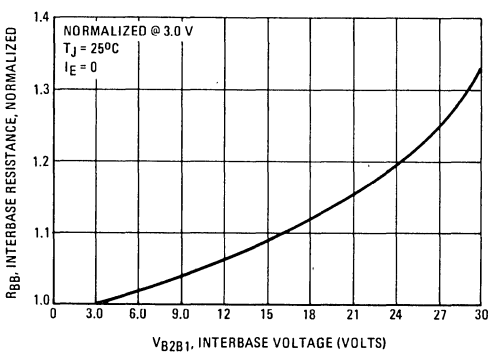
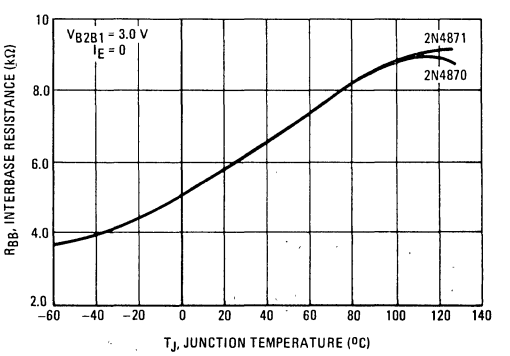


FIGURE 11 – EFFECT OF TEMPERATURE



7

TYPICAL CHARACTERISTICS

VALLEY CURRENT

FIGURE 12 – EFFECT OF VOLTAGE

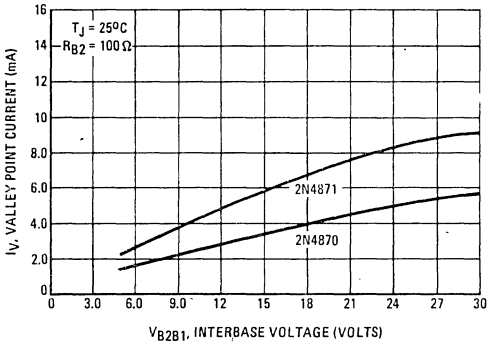
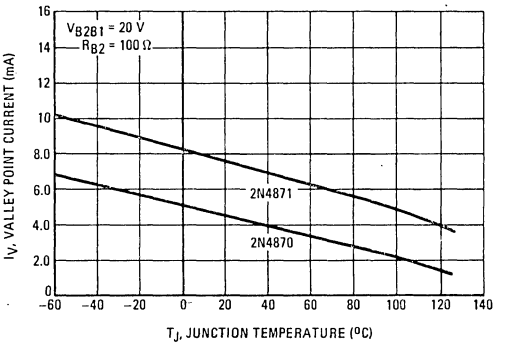


FIGURE 13 – EFFECT OF TEMPERATURE



VALLEY VOLTAGE

FIGURE 14 – EFFECT OF VOLTAGE

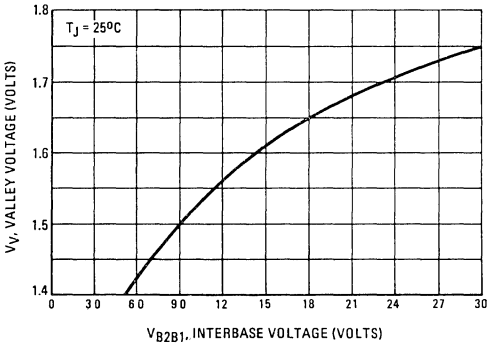


FIGURE 15 – EFFECT OF TEMPERATURE

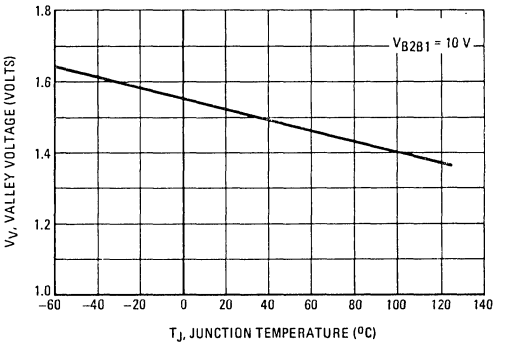
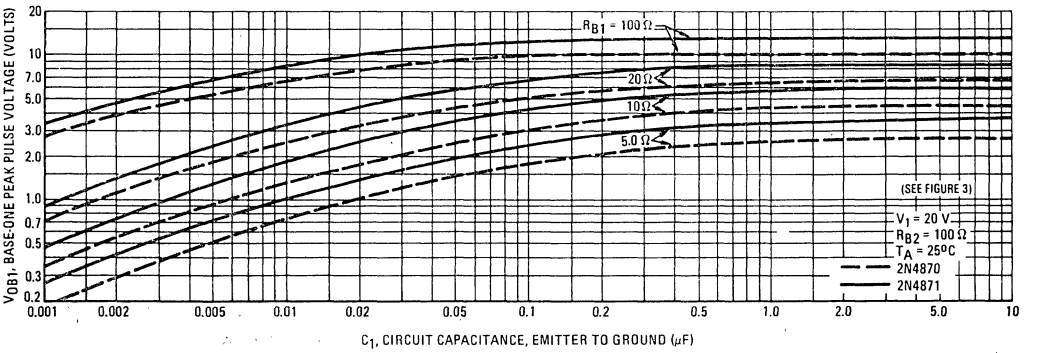
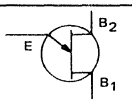


FIGURE 16 – OUTPUT VOLTAGE



2N4948
2N4949

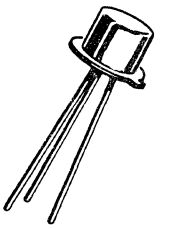


SILICON UNIJUNCTION TRANSISTORS

. . . designed for military and industrial use in pulse, timing, triggering, sensing, and oscillator circuits. The annular process provides low leakage current, fast switching and low peak-point currents as well as outstanding reliability and uniformity. Recommended usage includes:

- Silicon Controlled Rectifier Triggering Circuits – 2N4948
- Long-time Delay Circuits – 2N4949

PN UNIJUNCTION TRANSISTORS



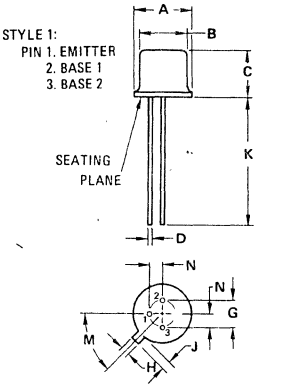
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
RMS Power Dissipation*	P_D	360*	mW
RMS Emitter Current	I_e	50	mA
Peak Pulse Emitter Current**	i_e	1.0**	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Storage Temperature Range	T_{stg}	-65 to +200	°C

* Derate 2.4 mW/°C increase in ambient temperature. Total power dissipation (available power to Emitter and Base-Two) must be limited by external circuitry. Interbase voltage (V_{B2B1}) limited by power dissipation, $V_{B2B1} = \sqrt{R_{BB} \cdot P_D}$.

** Capacitance discharge current must fall to 0.37 Amp within 3.0 ms and PRR ≤ 10 PPS.

NOTE:
1. PIN 3 CONNECTED TO CASE.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.48	0.016	0.019
G	2.54 TYP		0.100 TYP	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
M	45° TYP		45° TYP	
N	1.27 TYP		0.050 TYP	

CASE 22A-01

TO-18 PACKAGE
(Except for lead position)

7

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio		η				–
(V_{B2B1} = 10 V) Note 1	2N4948		0.55	–	0.82	
	2N4949		0.74	–	0.86	
Interbase Resistance		R_{BB}				k ohms
(V_{B2B1} = 3.0 V, I_E = 0)	2N4948, 2N4949		4.0	7.0	12.0	
Interbase Resistance Temperature Coefficient		αR_{BB}				%/°C
(V_{B2B1} = 3.0 V, I_E = 0, T_A = -65°C to +100°C)			0.1	–	0.9	
Emitter Saturation Voltage		$V_{EB1(sat)}$				Volts
(V_{B2B1} = 10 V, I_E = 50 mA) Note 2			–	2.5	3.0	
Modulated Interbase Current		$I_{B2(mod)}$				mA
(V_{B2B1} = 10 V, I_E = 50 mA)			12	15	–	
Emitter Reverse Current		I_{EB2O}				
(V_{B2E} = 30 V, I_{B1} = 0)			–	5.0	10	nA
(V_{B2E} = 30 V, I_{B1} = 0, T_A = 125°C)			–	–	1.0	μA
Peak Point Emitter Current		I_P				μA
(V_{B2B1} = 25 V)	2N4948		–	0.6	2.0	
	2N4949		–	0.6	1.0	
Valley Point Current		I_V				mA
(V_{B2B1} = 20 V, R_{B2} = 100 ohms) Note 2	2N4948, 2N4949		2.0	4.0	–	
Base-One Peak Pulse Voltage		V_{OB1}				Volts
(Note 3, Figure 3)	2N4949		3.0	5.0	–	
	2N4948		6.0	8.0	–	
Maximum Oscillation Frequency		$f_{(max)}$				MHz
(Figure 4)			–	1.25	–	

NOTES

1. Intrinsic standoff ratio.
   η, is defined by equation:

$$\eta = \frac{V_P - V_{(EB1)}}{V_{B2B1}}$$

Where V_P = Peak Point Emitter Voltage
V_{B2B1} = Interbase Voltage
$V_{(EB1)}$ = Emitter to Base-One Junction Diode Drop
(≈ 0.45 V @ 10 μA)

2. Use pulse techniques: PW ≈ 300 μs duty cycle ⩽ 2% to avoid internal heating due to interbase modulation which may result in erroneous readings.

3. Base-One Peak Pulse Voltage is measured in circuit of Figure 3. This specification is used to ensure minimum pulse amplitude for applications in SCR firing circuits and other types of pulse circuits.

FIGURE 1 – UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

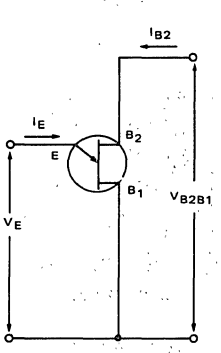


FIGURE 2 – STATIC EMITTER CHARACTERISTICS CURVES

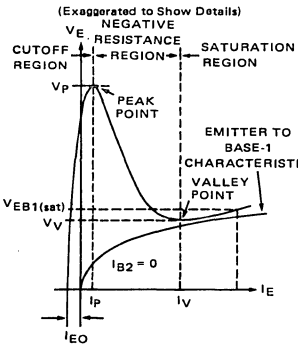


FIGURE 3 – V_{OB1} TEST CIRCUIT (Typical Relaxation Oscillator)

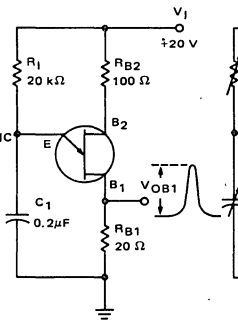
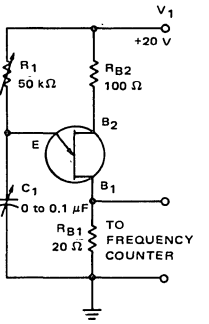
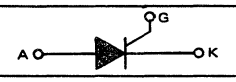


FIGURE 4 – F(max) MAXIMUM FREQUENCY TEST CIRCUIT



7

2N5060 thru 2N5064



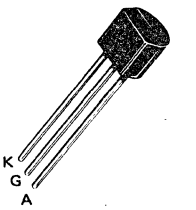
REVERSE BLOCKING TRIODE THYRISTORS

. . . Annular♦ PNPN devices designed for high volume consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-92 package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Trigger Current – 200 μA Maximum
- Low Reverse and Forward Blocking Current – 50 μA Maximum, T_C = 125°C
- Low Holding Current – 5.0 mA Maximum
- Passivated Surface for Reliability and Uniformity
- Also Available with TO-5 or TO-18 Lead Form

SILICON CONTROLLED RECTIFIERS

0.8 AMPERE RMS
30 thru 200 VOLTS



MAXIMUM RATINGS(1)

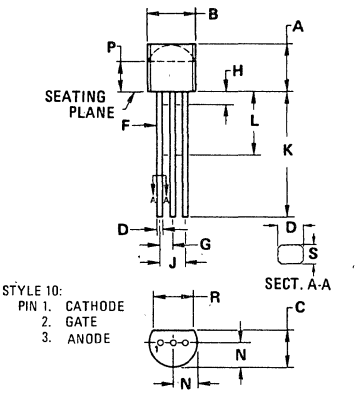
Rating	Symbol	Value	Unit
*Peak Repetitive Reverse Blocking Voltage (1) (R_{GK} = 1000 ohms, T_C = +125°C) 2N5060	V_{DRM} V_{RRM}	30	Volts
2N5061		60	
2N5062		100	
2N5063		150	
2N5064		200	
On-State Current RMS (All Conduction Angles)	$I_{T(RMS)}$	0.8	Amp
*Average On-State Current (T_C = 67°C)	$I_{T(AV)}$	0.51	Amp
(T_C = 102°C)		0.255	
*Peak Non-Repetitive Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	10	Amp
Circuit Fusing Considerations, T_A = 25°C (t = 1.0 to 8.3 ms)	I^2t	0.15	A^2s
*Peak Gate Power, T_A = 25°C	P_{GM}	0.1	Watt
*Average Gate Power, T_A = 25°C	$P_{G(AV)}$	0.01	Watt
*Peak Forward Gate Current, T_A = 25°C (300 μs, 120 PPS)	I_{FGM}	1.0	Amp
*Peak Reverse Gate Voltage	V_{RGM}	5.0	Volts
*Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	-65 to +125	°C
*Storage Temperature Range	T_{stg}	-65 to +150	°C
*Lead Solder Temperature (Lead Length ≥ 1/16" from case, 10 s Max)	–	+230*	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case (2)	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

(1) Ratings apply for zero or negative gate voltage. Device ratings exclude having a positive bias applied to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.
(2) This measurement is made with the case mounted "flat side down" on a heat sink and held in position by means of a metal clamp over the curved surface.

♦Annular Semiconductor Patented by Motorola Inc.
*Indicates JEDEC Registered Data.



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (4) (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Voltage (Note 1) (T_C = 125°C, R_{GK} = 1000 Ohms)	2N5060	V_{DRM}	30	–	–	Volts
	2N5061		60	–	–	
	2N5062		100	–	–	
	2N5063		150	–	–	
	2N5064		200	–	–	
*Peak Forward Blocking Current (Rated V_{DRM} @ T_C = 125°C, R_{GK} = 1000 Ohms)		I_{DRM}	–	–	50	μA
*Peak Reverse Blocking Current (Rated V_{RRM} @ T_C = 125°C, R_{GK} = 1000 Ohms)		I_{RRM}	–	–	50	μA
*Forward "On" Voltage (Note 2) (I_{TM} = 1.2 A peak @ T_A = 25°C)		V_{TM}	–	–	1.7	Volts
Gate Trigger Current (Continuous dc) (Note 3)	T_C = 25°C	I_{GT}	–	–	200	μA
*(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms, R_{GK} = 1000 Ohms)	T_C = -65°C		–	–	350	
Gate Trigger Voltage (Continuous dc)	T_C = 25°C	V_{GT}	–		0.8	Volts
*(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = -65°C		–		1.2	
(Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms)	T_C = 125°C	V_{GD}	0.1		–	
Holding Current	T_C = 25°C	I_H	–	–	5.0	mA
*(Anode Voltage = 7.0 Vdc, initiating current = 20 mA	T_C = -65°C		–	–	10	
Turn-On Time						μs
Delay Time		t_d	–	3.0	–	
Rise Time		t_r	–	0.2	–	
(I_{GT} = 1.0 mA, R_{GK} = 1.0 Ohm, V_D = Rated V_{DRM}, Forward Current = 1.0 A, di/dt = 6.0 A/μs)						
Turn-Off Time	2N5060,2N5061	tq	–	10	–	μs
(Forward Current = 1.0 A pulse, Pulse Width = 50 μs, 0.1% Duty Cycle, di/dt = 6.0 A/μs, dv/dt = 20 V/μs, I_{GT} = 1.0 mA, R_{GK} = 1.0 k Ohm)	2N5062,5063,5064		–	30	–	
Forward Voltage Application Rate (Rated V_{DRM}, R_{GK} = 1.0 k, Exponential)		dv/dt	–	300	–	V/μs

*Indicates JEDEC Registered Data.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.
2. Forward current applied for 1.0 ms maximum duration, duty cycle ≤ 1.0%.
3. R_{GK} current is not included in measurement.
4. For electrical characteristics for Gate-to-cathode resistance other than 1000 ohms see Motorola Bulletin EB-30.

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CURRENT DERATING

FIGURE 1 – MAXIMUM CASE TEMPERATURE

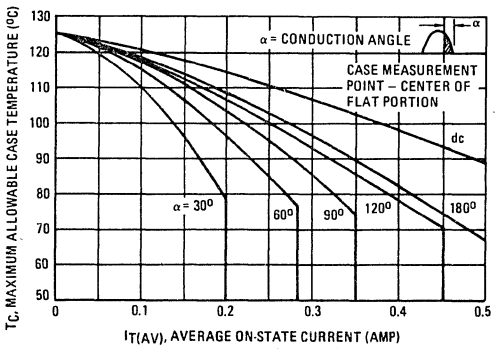

FIGURE 2 – MAXIMUM AMBIENT TEMPERATURE

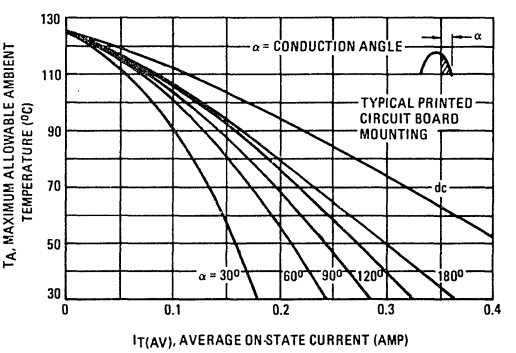

FIGURE 3 – TYPICAL FORWARD VOLTAGE

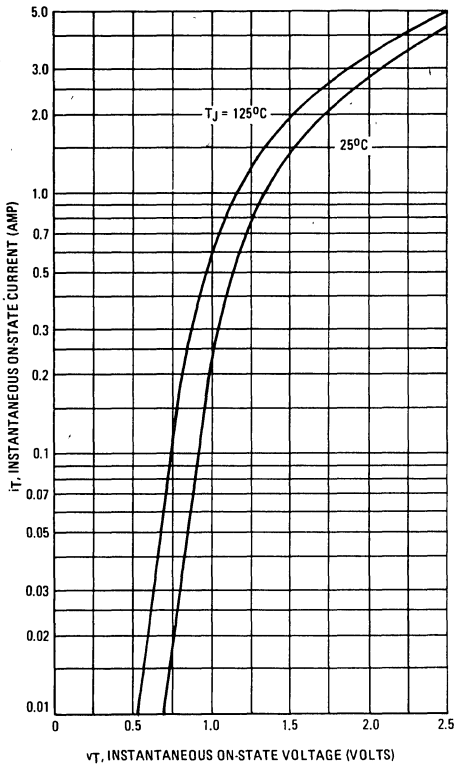

FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

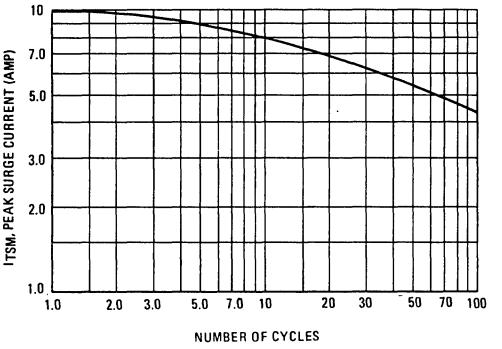

FIGURE 5 – POWER DISSIPATION

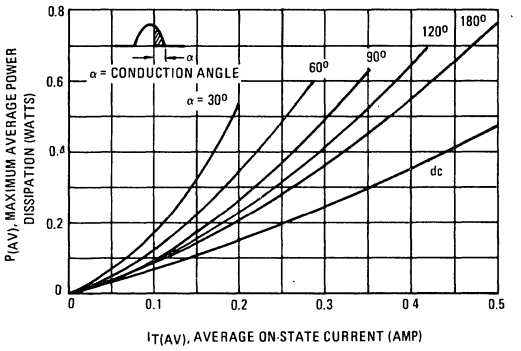

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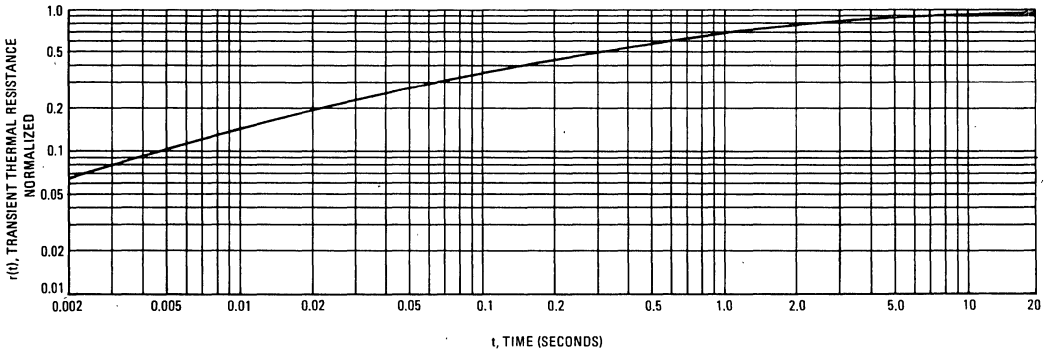
FIGURE 6 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS

FIGURE 7 – GATE TRIGGER VOLTAGE

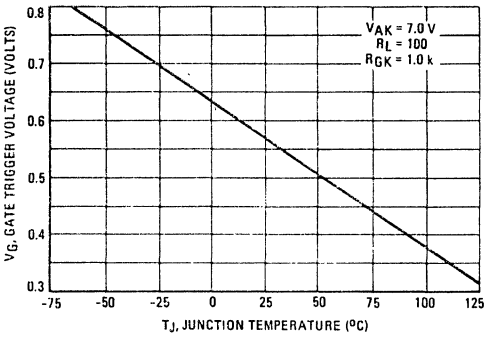


FIGURE 8 – GATE TRIGGER CURRENT

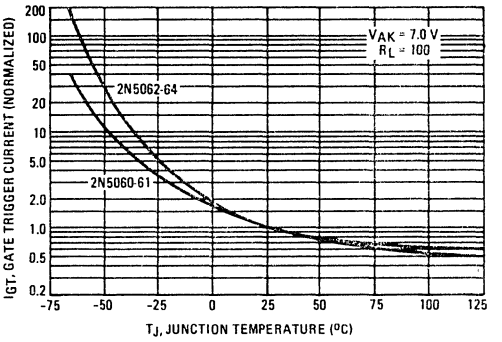


FIGURE 9 – HOLDING CURRENT

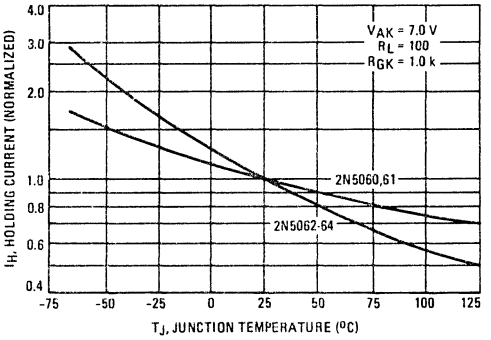
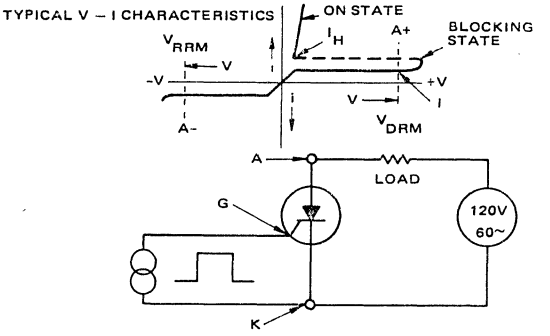


FIGURE 10 – CHARACTERISTICS AND SYMBOLS



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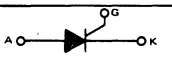
2N5164 thru 2N5171



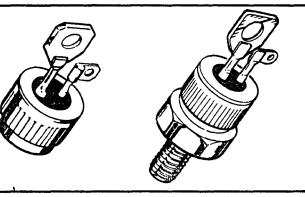
REVERSE BLOCKING TRIODE THYRISTOR

. . . designed for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls.

- Supplied in Either Pressfit or Stud Package
- High Surge Current Rating – I_{TSM} = 240 Amp
- Low On-State Voltage – 1.2 V (Typ) @ I_{TM} = 20 Amp
- Practical Level Triggering and Holding Characteristics – 40 mA (Max) and 50 mA (Max) @ $T_C = 25^oC$

SILICON CONTROLLED RECTIFIER

20 AMPERES RMS
50-600 VOLTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Forward and *Repetitive Reverse Blocking Voltage (1), (2) 2N5164, 2N5168	V_{DRM} or V_{RRM}	50	Volts
2N5165, 2N5169		200	
2N5166, 2N5170		400	
2N5167, 2N5171		600	
*Non-repetitive Peak Reverse Blocking Voltage 2N5164, 2N5168	V_{RSM}	75	Volts
2N5165, 2N5169		300	
2N5166, 2N5170		500	
2N5167, 2N5171		700	
On-State Current RMS	$I_{T(RMS)}$	20	Amp
Average On-State Current ($T_C = 67^oC$)	$I_{T(AV)}$	13	Amp
Circuit Fusing (T_J = -40 to +100°C, t ≤ 8.3 ms)	I^2t	235	A^2s
*Peak Non-Repetitive Surge Current (One cycle, 60 Hz, T_J = -40 to +100°C) Preceded and followed by rated current and voltage.	I_{TSM}	240	Amp
*Peak Gate Power (Maximum Pulse Width = 10 μs)	P_{GM}	5.0	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current (Maximum Pulse Width = 10 μs)	I_{GM}	2.0	Amp
Peak Gate Voltage	V_{GM}	10	Volts
*Operating Junction Temperature Range	T_J	-40 to +100	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C
Stud Torque 2N5168-2N5171		30	in. lb.

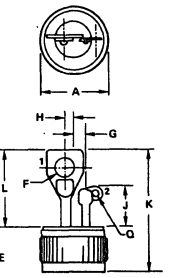
THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$			°C/W
2N5164, 65, 66, 67		1.0	1.5	
2N5168, 69, 70, 71		1.1	1.6	

(1) V_{DRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage applied exceeds the rated blocking voltage.

(2) Devices should not be operated with a positive bias applied to the gate concurrent with a negative potential applied to the anode.

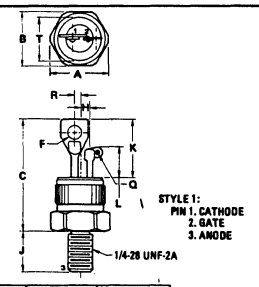
2N5164
2N5165
2N5166
2N5167



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	12.73	12.83	0.501	0.505
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.52	1.78	0.060	0.070
J	7.62	8.89	0.300	0.350
K	–	26.67	–	1.050
L	–	17.02	–	0.670
Q	1.40	2.16	0.055	0.085

CASE 310-01

2N5168
2N5169
2N5170
2N5171



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	29.87	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	16.75	17.02	0.820	0.670
L	7.67	8.89	0.300	0.350
Q	1.40	2.18	0.055	0.085
R	1.85 REF		0.085 REF	
T	12.73	12.83	0.501	0.505

CASE 263-03

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
*Peak Forward Blocking Current (V_D = Rated V_{DRM} @ T_J = 100°C, gate open)	I_{DRM}	–	5.0	mA
*Peak Reverse Blocking Current (V_R = Rated V_{RRM} @ T_J = 100°C, gate open)	I_{RRM}	–	5.0	mA
Gate Trigger Current (Continuous dc) (2)	I_{GT}			mA
(V_D = 7.0 Vdc, R_L = 100 Ω)		–	40	
*(V_D = 7.0 Vdc, R_L = 100 Ω, T_C = -40°C)		–	75	
Gate Trigger Voltage (Continuous dc)	V_{GT}			Volts
(V_D = 7.0 Vdc, gate open)		–	1.5	
*(V_D = 7.0 Vdc, R_L = 100 Ω, T_C = -40°C)		–	2.5	
*(V_D =Rated V_{DRM}, R_L = 100 Ω, T_J = 100°C)		0.2	–	
Peak On-State Voltage (Pulse Width = 1.0 ms max, duty cycle ≤1%)	V_{TM}			Volts
(I_{TM} = 20 A)		–	1.5	
*(I_{TM} = 41 A)		–	1.7	
Holding Current	I_H			mA
(V_D = 7.0 Vdc, gate open)		–	50	
*(V_D = 7.0 Vdc, gate open, T_C = -40°C)		–	90	
		Typical		
Gate Controlled Turn-On Time (t_d + t_r) (I_{TM} = 20 A, I_{GT} = 40 mAdc, V_D = Rated V_{DRM})	t_{gt}	1.0		μs
Circuit Commutated Turn-Off Time	t_q			μs
(I_{TM} = 10 A, I_R = 10 A)		20		
(I_{TM} = 10 A, I_R = 10 A, T_J = 100°C) (V_D = V_{DRM} = rated voltage) (dv/dt = 30 V/μs)		30		
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Wave Form, Gate open, T_J = 100°C)	dv/dt	50		V/μs

*Indicates JEDEC registered data.

7

EFFECT OF TEMPERATURE UPON TYPICAL TRIGGER CHARACTERISTICS

FIGURE 1 – GATE TRIGGER CURRENT

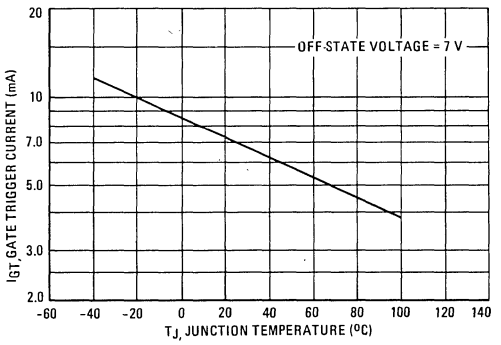
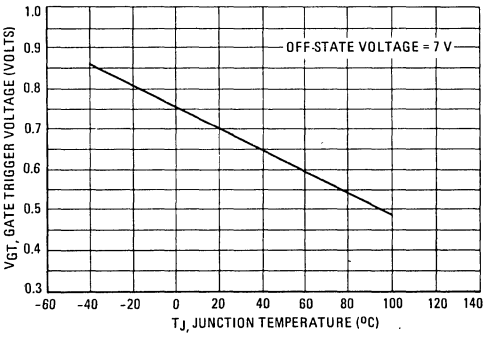


FIGURE 2 – GATE TRIGGER VOLTAGE



MAXIMUM ALLOWABLE NON-REPETITIVE SURGE CURRENT

FIGURE 3 – 60 Hz SURGES

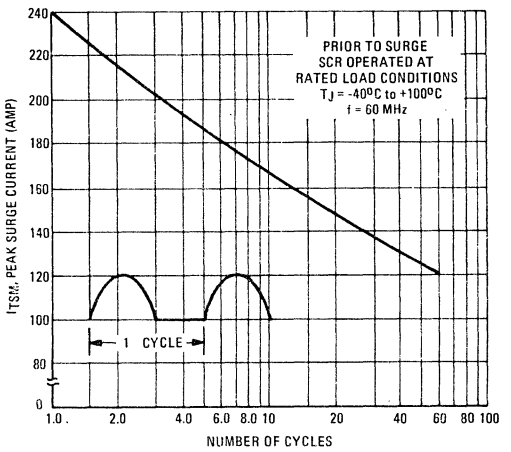


FIGURE 4 – SUB-CYCLE SURGES

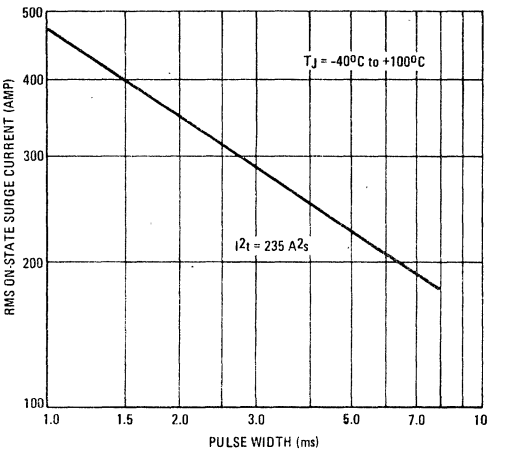


FIGURE 5 – GATE TRIGGER CHARACTERISTICS

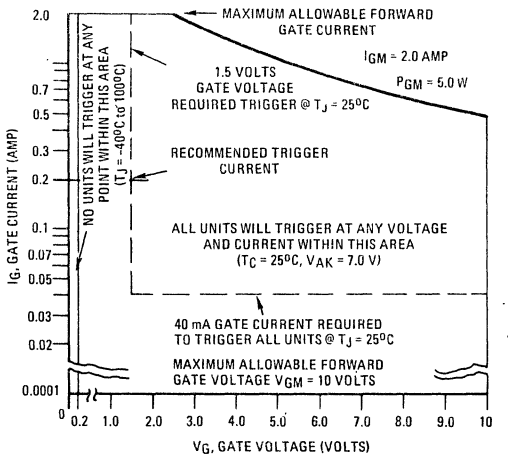
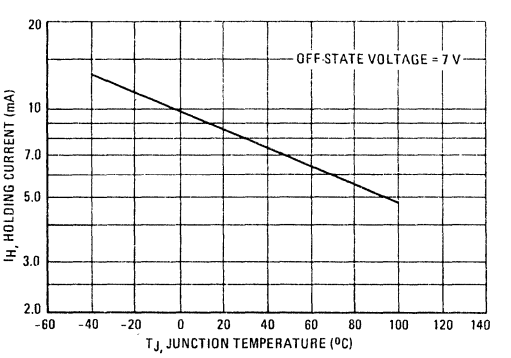


FIGURE 6 – EFFECT OF TEMPERATURE ON TYPICAL HOLDING CURRENT



DERATING AND DISSIPATION FOR RESISTIVE AND INDUCTIVE LOADS (f = 60 to 400 Hz, SINE WAVE)

FIGURE 7 – AVERAGE CURRENT DERATING

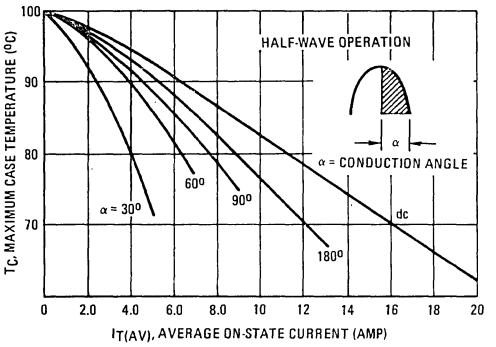


FIGURE 8 – ON-STATE POWER DISSIPATION

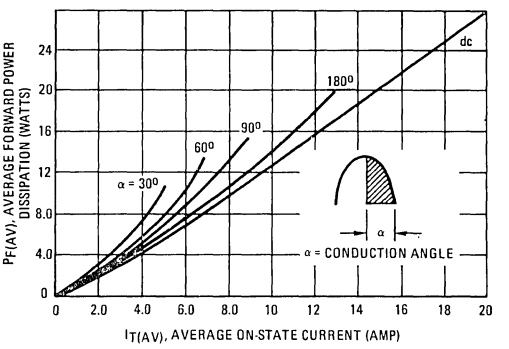


FIGURE 9 – ON-STATE CHARACTERISTICS

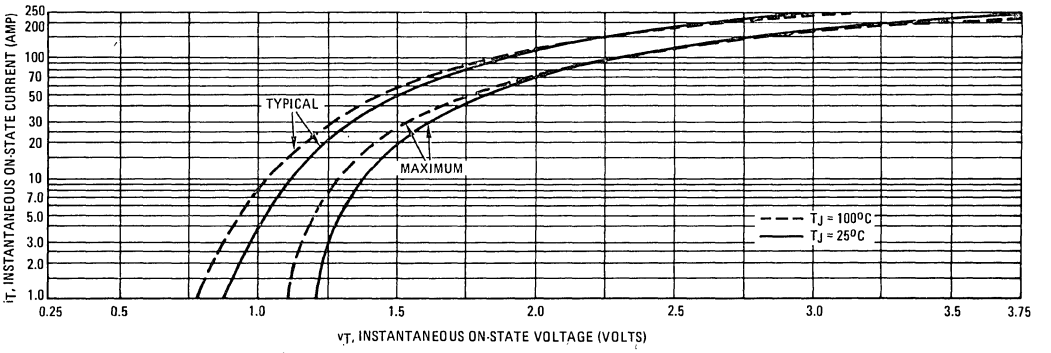


FIGURE 10 – TYPICAL THERMAL RESISTANCE OF PLATES

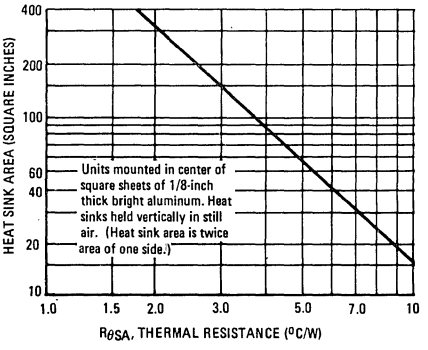
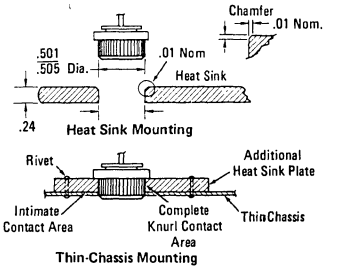


FIGURE 11 – MOUNTING DETAILS FOR PRESSFIT THYRISTORS



The hole edge must be chamfered as shown to prevent shearing off the knurled edge of the rectifier during press-in. The pressing force should be applied evenly on the shoulder ring to avoid tilting or canting of the rectifier case in the hole during the pressing operation. Also, the use of a thermal joint compound will be of considerable aid. The pressing force will vary from 250 to 1000 pounds, depending upon the heat sink material. Recommended hardnesses are: copper – less than 50 on the Rockwell F scale; aluminum – less than 65 on the Brinell scale. A heat sink as thin as 1/8" may be used, but the interface thermal resistance will increase in proportion to the reduction of contact area. A thin chassis requires the addition of a back-up plate.

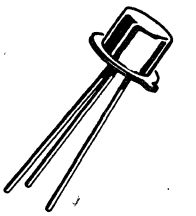
2N5431

SILICON ANNULAR† UNIJUNCTION TRANSISTORS

. . . characterized primarily for low interbase-voltage operation in sensing, pulse triggering, and timing circuits.

- Low R_{BB} Spread — 6.0 to 8.5 kΩ
- Low Peak-Point Current — Ip = 4.0 μA (Max) @ V_{B2B1} = 4.0 V
- Low Emitter Saturation Voltage — $V_{EB1(sat)}$ = 3.0 V (Max)
- Narrow Intrinsic Standoff Ratio — η = 0.72 to 0.80

PN UNIJUNCTION TRANSISTORS



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
RMS Power Dissipation*	P_D*	300	mW
RMS Emitter Current	I_e	50	mA
Peak-Pulse Emitter Current**	i_e**	1.5	A
Emitter Reverse Voltage	V_{B2E}	30	V
Interbase Voltage‡	V_{B2B1}‡	35	V
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

*Derate 3.0 mW/°C increase in ambient temperature.
**Duty Cycle ≤ 1.0%, PRR = 10 PPS (see figure 5).
‡Based upon power dissipation at T_A = 25°C.

FIGURE 1 — UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

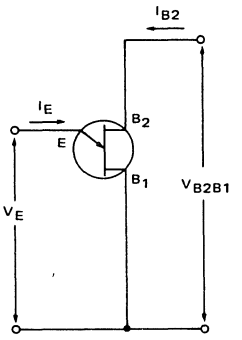
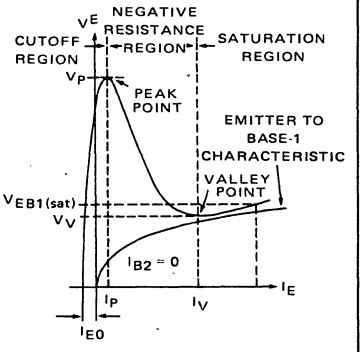
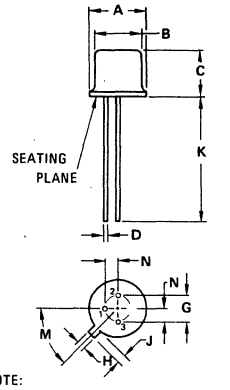


FIGURE 2 — STATIC EMITTER CHARACTERISTICS CURVES





NOTE:
1. PIN 3 CONNECTED TO CASE.

STYLE 1:
PIN 1. EMITTER
2. BASE 1
3. BASE 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.48	0.016	0.019
G	2.54 TYP		0.100 TYP	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	—	0.500	—
M	45° TYP		45° TYP	
N	1.27 TYP		0.050 TYP	

CASE 22A
(TO-18 Outline
Except for Lead Position)

7

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
Intrinsic Standoff Ratio [1] (V_{B2B1} = 10 V)	4	η	0.72	0.80	–
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)		R_{BB}	6.0	8.5	kΩ
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = 0 to 100°C)		αR_{BB}	0.4	0.8	%/°C
Emitter Saturation Voltage [2] (V_{B2B1} = 10 V, I_E = 50 mA)		$V_{EB1(sat)}$	–	3.0	V
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)		$I_{B2(mod)}$	5.0	30	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)		I_{EB2O}	–	10	nA
Peak-Point Emitter Current (V_{B2B1} = 25 V) (V_{B2B1} = 4.0 V)		I_P	– –	0.4 4.0	μA
Valley-Point Current [2] (V_{B2B1} = 20 V, R_{B2} = 100 ohms)		I_V	2.0	–	mA
Base-One Peak Pulse Voltage (V_{BB} = 4.0 volts)	3	V_{OB1}	1.0	–	V

[1] η, Intrinsic standoff ratio, is defined in terms of the peak-point voltage, V_P, by means of the equation: $V_P = \eta V_{B2B1} + V_F$, where V_F is about 0.45 volt at 25°C @ I_F = 10 μA and decreases with temperature at about 2.5 mV/°C. The test circuit is shown in Figure 4. Components R_1, C_1, and the UJT form a relaxation oscillator; the remaining circuitry serves as a peak-voltage detector. The forward drop of Diode D_1 compensates for V_F. To use, the "cal" button is pushed, and R_3 is adjusted to make the current meter, M_1, read full scale. When the "cal" button is released, the value of η is read directly from the meter, if full scale on the meter reads 1.0.

[2] Use pulse techniques: PW ≈ 300 μs, Duty Cycle ≤ 2.0% to avoid internal heating, which may result in erroneous readings.

FIGURE 3 – V_{OB1} TEST CIRCUIT

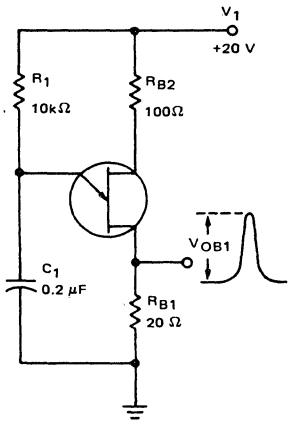
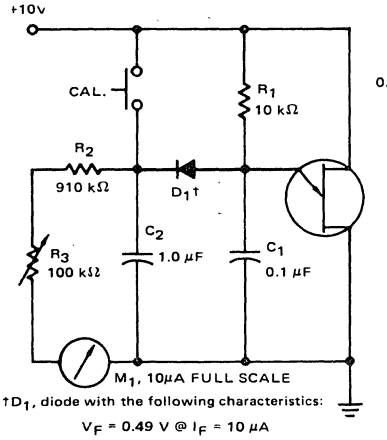
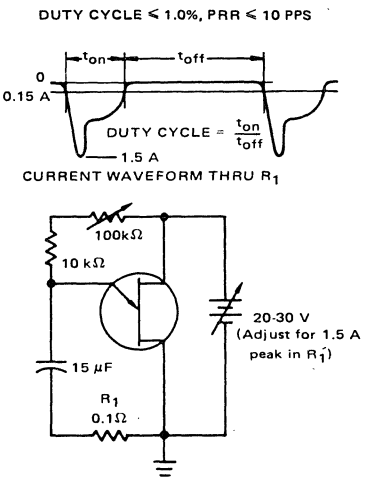


FIGURE 4 – η TEST CIRCUIT

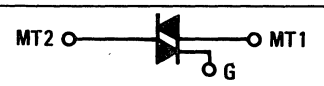


†D_1, diode with the following characteristics:
V_F = 0.49 V @ I_F = 10 μA
I_R ≤ 2.0 μA @ V_R = 20 V

FIGURE 5 – PRR TEST CIRCUIT AND WAVEFORM



2N5441 thru 2N5446
MAC40688 thru MAC40690



TRIACS

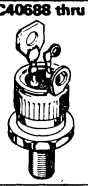
40 AMPERES RMS
200–600 VOLTS

SILICON BIDIRECTIONAL TRIODE THYRISTORS

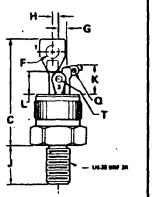
. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire
- Isolated Stud for Ease of Assembly
- Gate Triggering Guaranteed In All 4 Quadrants

MAC40688 thru MAC40690



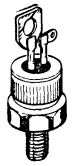
STYLE 2:
1. MT1
2. GATE
3. MT2



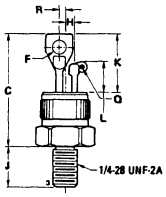
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	32.51	–	1.280
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.60	2.01	0.063	0.079
J	10.67	11.56	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6.48	6.99	0.255	0.275
Q	1.40	2.16	0.055	0.085
T	3.43	3.81	0.135	0.150

CASE 311-01

2N5444 thru 2N5446



STYLE 2:
PIN 1. MT1
2. GATE
3. MT2

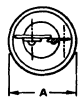


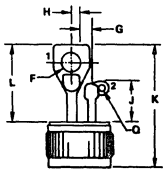
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.28 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.85 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

CASE 263-03

2N5441 thru 2N5443

STYLE 2:
1. MT1
2. GATE
CASE. MT2





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.52	1.78	0.060	0.070
J	7.62	8.89	0.300	0.350
K	–	26.67	–	1.050
L	–	17.02	–	0.670
Q	1.40	2.16	0.055	0.085

CASE 310-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (T_J = -65 to +110°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
*Peak Principal Voltage 2N5441, 2N5444, MAC40688 2N5442, 2N5445, MAC40689 2N5443, 2N5446, MAC40690		200 400 600	
*RMS On-State Current (T_C per Fig. 2) (T_C = +100°C) Full Sine Wave, 50 to 60 Hz	$I_{T(RMS)}$	40 20	Amp
*Peak Non-Repetitive Surge Current (One Full Cycle of surge current at 60 Hz, preceeded and followed by a 40 A RMS current, T_J = +110°C)	I_{TSM}	300	Amp
*Peak Gate Power (Pulse Width = 10 μs Max)	P_{GM}	40	Watts
*Average Gate Power	$P_{G(AV)}$	0.75	Watt
*Peak Gate Current (10 μs Max)	I_{GM}	4.0	Amp
*Peak Gate Voltage	V_{GM}	30	Volts
*Operating Junction Temperature Range	T_J	-65 to +110	°C
*Storage Temperature Range	T_{stg}	-65 to +150	°C
*Stud Torque	–	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case 2N5441, 2N5442, 2N5443 2N5444, 2N5445, 2N5446 MAC40688, MAC40689, MAC40690	$R_{\theta JC}$	0.8 0.9 1.0	°C/W

*Indicates JEDEC Registered Data for 2N5441 thru 2N5446.

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and either polarity of MT2 to MT1 voltage, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak On-State Voltage Rated V_{DRM} @ T_J = 110°C	I_{DRM}	–	0.5	4.0	mA
*Peak On-State Voltage I_{TM} = 56 A Peak, Pulse Width ≤ 1.0 ms, Duty Cycle ≤ 2.0%	V_{TM}	–	1.65	1.85	Volts
Gate Trigger Current (1) Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms	I_{GT}				mA
MT2 (+), G(+)		–	–	70	
MT2 (+), G(–)		–	–	70	
MT2 (–), G(–)		–	–	70	
MT2 (–), G(+)		–	–	100	
*MT2 (+), G(+); MT2 (–), G (–) T_C = –65°C		–	–	125	
*MT2 (+), G(–); MT2 (–), G(+) T_C = –65°C		–	–	240	
*Gate Trigger Voltage Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms	V_{GT}				Volts
MT2 (+), G(+)		–	–	2.0	
MT2 (+), G(–)		–	–	2.0	
MT2 (–), G(–)		–	–	2.0	
MT2 (–), G(+)		–	–	2.5	
*All Quadrants, T_C = –65°C)		–	–	3.4	
*Main Terminal Voltage = Rated V_{DRM} = R_L = 10 k ohms, T_J = +110°C		0.2	–	–	
*Holding Current Main Terminal Voltage = 12 Vdc, Gate Open Initiating Current = 150 mA	I_H				mA
T_C = 25°C		–	–	70	
*T_C = –65°C		–	–	100	
*Turn-On Time Main Terminal Voltage = Rated V_{DRM}, I_{TM} = 56 A, Gate Source Voltage = 12 V, R_S = 12 Ohms, Rise Time = 0.1 μs, Pulse Width = 2.0 μs	t_{gt}	–	1.0	2.0	μs
*Critical Rate-of -Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 40 A, Commutating di/dt = 22 A/ms, gate energized	dv/dt(c)				V/μs
T_C = 70°C 2N5441, 2N5442, 2N5443		5.0	30	–	
= 65°C 2N5444, 2N5445, 2N5446		5.0	30	–	
= 60°C MAC40688, MAC40689, MAC40690		5.0	30	–	
Critical Rate of Rise of Off State Voltage Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 110°C	dv/dt				V/μs
2N5441, 2N5444, MAC40688		50			
2N5442, 2N5445, MAC40689		30			
2N5443, 2N5446, MAC40690		20			

*Indicates JEDEC Registered Data for 2N5441 thru 2N5446.

FIGURE 1 – ON-STATE POWER DISSIPATION

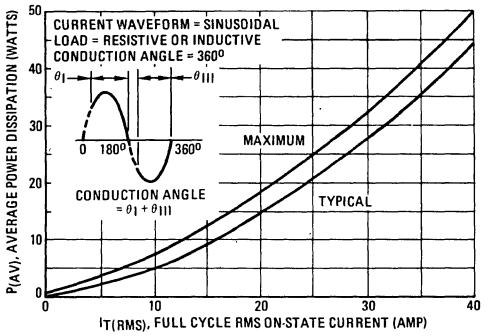


FIGURE 2 – RMS CURRENT DERATING

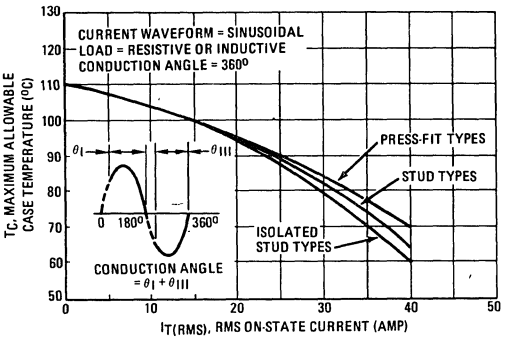


FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

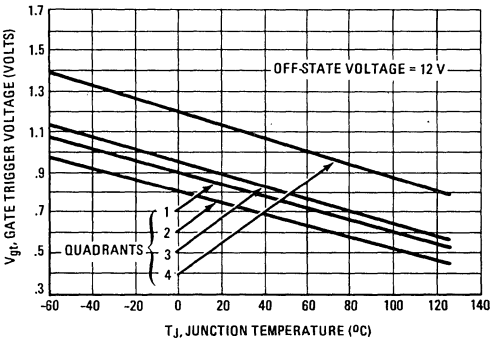


FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

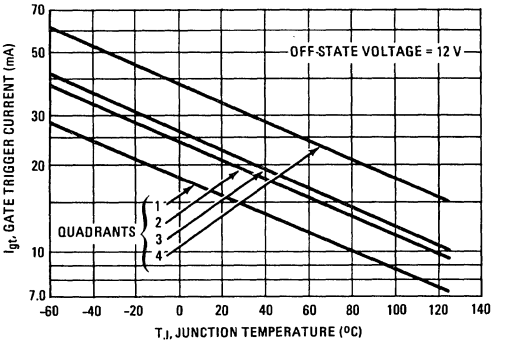


FIGURE 5 – TYPICAL THERMAL RESPONSE

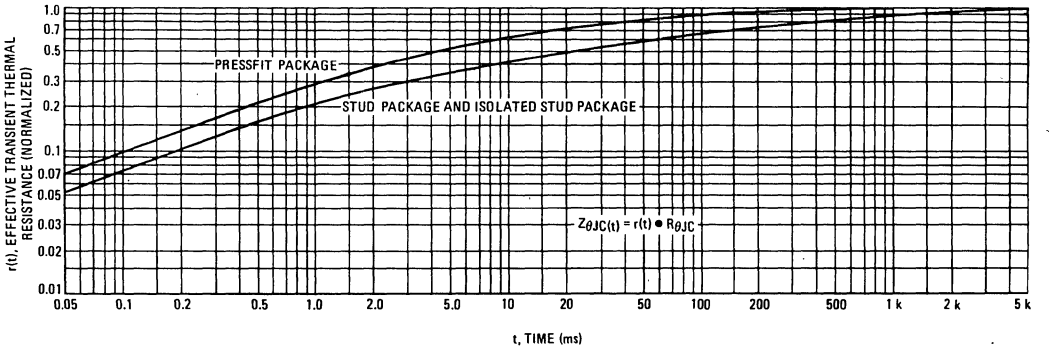


FIGURE 6 – ON-STATE CHARACTERISTICS

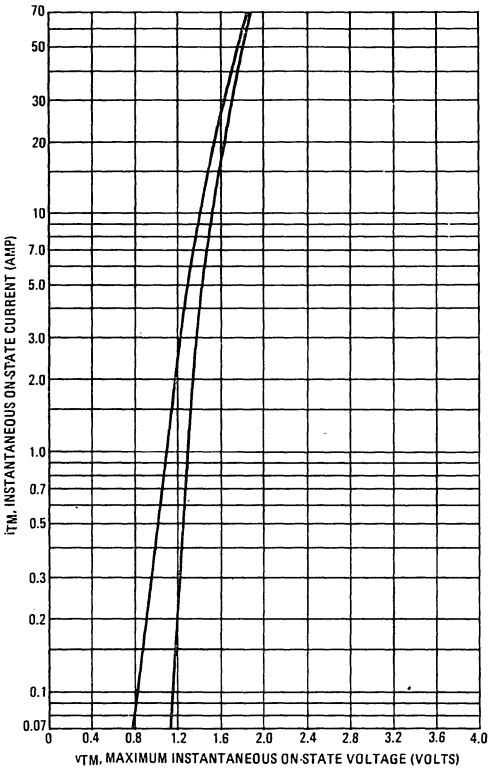


FIGURE 7 – TYPICAL HOLDING CURRENT

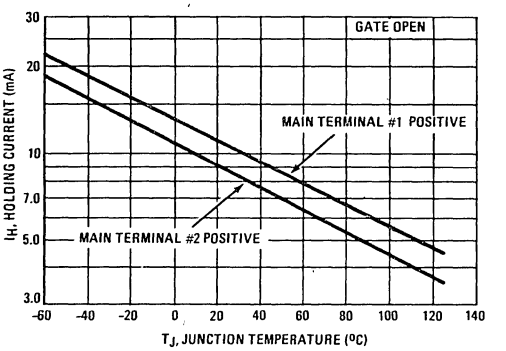
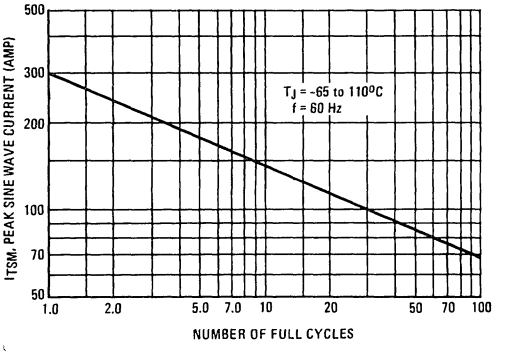


FIGURE 8 – MAXIMUM ALLOWABLE SURGE CURRENT



7

2N5567 thru 2N5570
T4101M, T4111M
T4121 series

BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for industrial and military applications for the fullwave control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems.

- All Diffused and Glass Passivated Junctions for Greater Stability
- Pressfit, Stud and Isolated Stud Packages
- Gate Triggering Guaranteed In All 4 Quadrants

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (T_J = -65 to +100°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open 2N5567, 2N5569, T4121B 2N5568, 2N5570, T4121D T4101M, T4111M, T4121M	V_{DRM}	 200 400 600	Volts
*Peak Gate Voltage	V_{GM}	20	Volts
*RMS On-State Current T_C = -65 to +85°C T_C = +90°C (Full cycle, Sine Wave, 50 to 60 Hz)	$I_{T(RMS)}$	 10 6.7	Amp
*Peak Non-Repetitive Surge Current (One Full cycle of surge current at 60 Hz, preceeded and followed by rated current, T_C = 85°C)	I_{TSM}	100	Amp
Circuit Fusing Considerations (T_C = -65 to +85°C, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
Peak Gate Power *(T_C = 85°C, Pulse Width = 1.0 μs)	P_{GM}	16	Watts
*Average Gate Power (T_C = 85°C, Pulse Width = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Operating Junction Temperature Range	T_J	-65 to +100	°C
*Storage Temperature Range	T_{stg}	-65 to +150	°C
Stud Torque	–	30	in. lb.

THERMAL CHARACTERISTICS

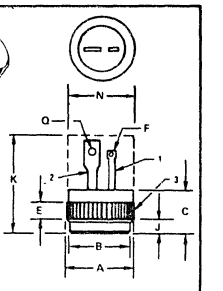
Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case Stud and Pressfit Isolated Stud	$R_{\theta JC}$	 1.0 1.1	°C/W

* Indicates JEDEC Registered Data.

TRIACS

10 AMPERES RMS
200–600 VOLTS

2N5567
2N5568
T4101M

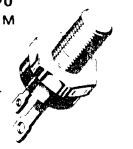


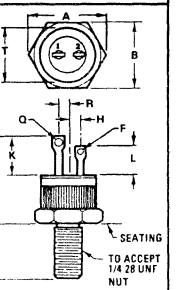
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	12.73	12.83	0.501	0.505
B	11.81	12.06	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54	–	0.100	–
F	0.89	2.16	0.035	0.085
J	2.04	2.46	0.080	0.097
K	–	20.32	–	0.800
N		12.95	–	0.510
Q	1.65	4.06	0.065	0.160

STYLE 3
TERM 1 GATE
2 MAIN TERMINAL 1
3 MAIN TERMINAL 2

CASE 174-03

2N5569
2N5570
T4111M



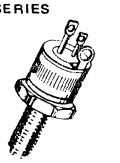


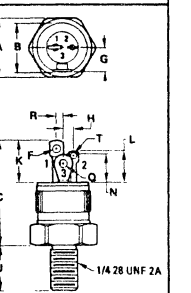
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	0.89	2.16	0.035	0.085
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	1.65	4.06	0.065	0.160
R	1.65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505

STYLE 3
TERM 1 MAIN TERMINAL 1
2 GATE
STUD MAIN TERMINAL 2

CASE 175-02

T4121 SERIES





DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	26.16	–	1.030
F	1.65	4.06	0.065	0.160
G	–	6.48	–	0.255
H	2.16	2.41	0.085	0.095
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
N	6.48	6.99	0.255	0.275
Q	3.43	3.81	0.135	0.150
R	1.52	1.78	0.060	0.070
T	0.89	2.16	0.035	0.085

STYLE 2
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2
STUD ISOLATED

CASE 235-02

7

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1 Voltage unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current V_D = Rated V_{DRM} @ T_C = 100°C	I_{DRM}	–	–	2.0	mA
*Peak On-State Voltage I_{TM} = 14.2 A Peak, Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0%	V_{TM}	–	1.3	1.65	Volts
Gate Trigger Current, Pulse Width ≥ 50 μs (1) V_D = 12 Vdc, R_L = 12 Ohms	I_{GT}				mA
MT2 (+), G (+); MT2 (–), G (–)		–	–	25	
MT2 (+), G (–); MT2 (–), G (+)		–	–	40	
*MT2 (+), G (+); MT2 (–), G (–), T_C = -65°C		–	–	100	
*MT2 (+), G (–); MT2 (–), G (+), T_C = -65°C		–	–	150	
Gate Trigger Voltage, Continuous dc (All Quadrants)	V_{GT}				Volts
V_D = 12 Vdc, R_L = 12 Ohms T_C = 25°C		–	–	2.5	
*T_C = -65°C		–	–	4.0	
V_D = Rated V_{DRM}, R_L = 125 Ω T_C = 100°C		0.2	–	–	
Holding Current V_D - 12 Vdc, Gate Open	I_H				mA
T_C = 25°C		–	–	30	
*T_C = -65°C		–	–	200	
Gate Controlled Turn-On Time V_D = Rated V_{DRM}, I_{TM} = 15 A Peak, I_{GT} = 160 mA, Rise Time = 0.1 μs, Pulse Width = 2.0 μs MT2 (+), G (+); MT2 (–), G (–)	t_{gt}	–	1.0	2.5	μs
*Critical Rate-of-Rise of Commutation Voltage V_D = Rated V_{DRM}, I_{TM} = 14.2 A Peak, Commutating di/dt = 5.4 A/ms, gate unenergized T_C = 85°C	dv/dt(c)	2.0	10	–	V/μs
Critical Rate-of-Rise of Off-State Voltage V_D = Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 100°C:	dv/dt				V/μs
*2N5567, *2N5569, T4121B		30	150	–	
*2N5568, *2N5570, T4121D		20	100	–	
T4101M, T4111M, T4121M		10	75	–	

*Indicates JEDEC Registered Data.
(1) All Voltage polarity reference to main terminal 1.

7

FIGURE 1 – RMS CURRENT DERATING
(Isolated Stud)

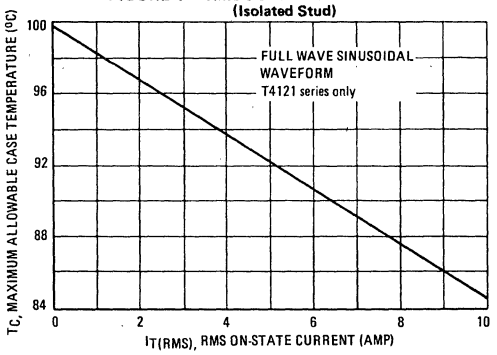


FIGURE 2 – RMS CURRENT DERATING
(Pressfit and Stud)

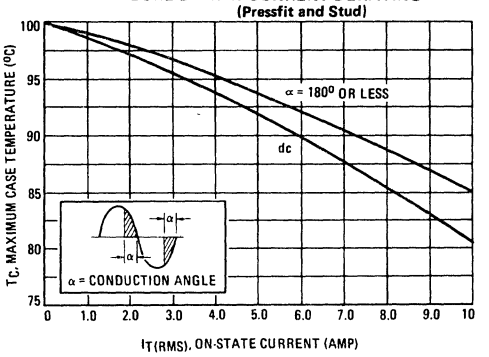


FIGURE 3 – POWER DISSIPATION
(Isolated Stud)

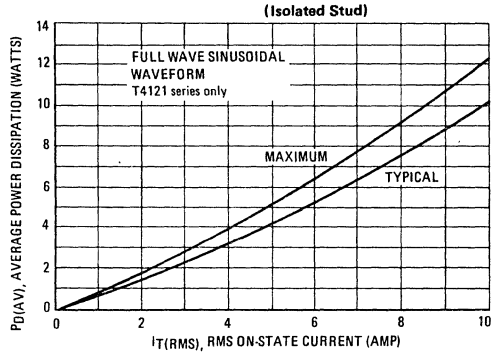


FIGURE 4 – POWER DISSIPATION
(Pressfit and Stud)

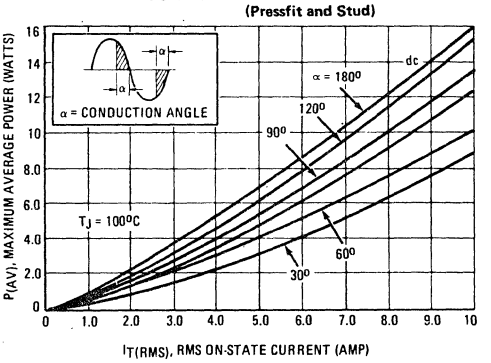


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FIGURE 5 – TYPICAL GATE TRIGGER VOLTAGE

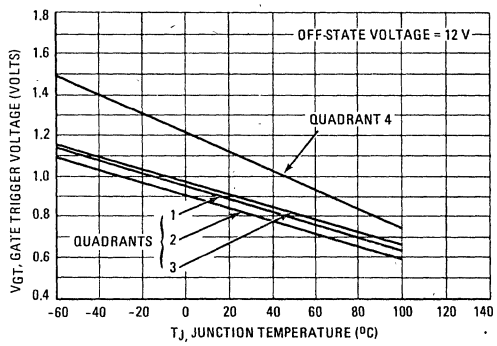


FIGURE 6 – TYPICAL GATE TRIGGER CURRENT

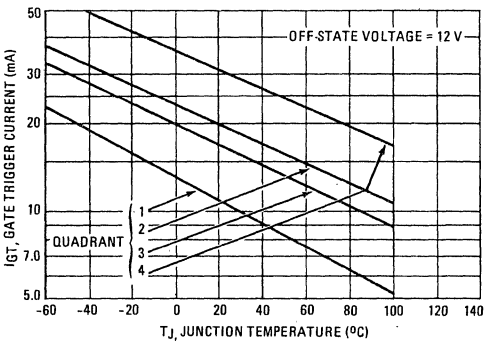


FIGURE 7 – ON-STATE CHARACTERISTICS

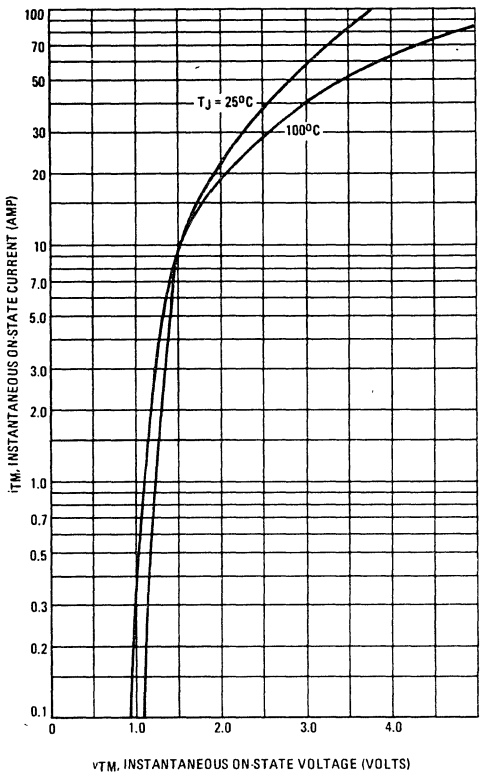


FIGURE 8 – TYPICAL HOLDING CURRENT

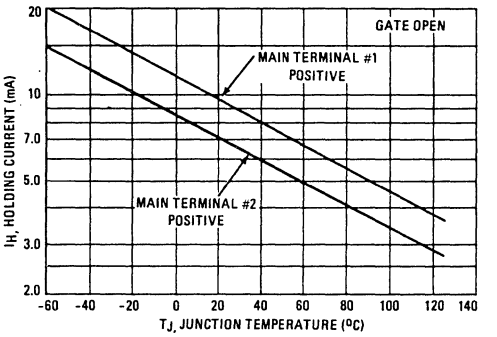


FIGURE 9 – MAXIMUM NON-REPETITIVE SURGE CURRENT

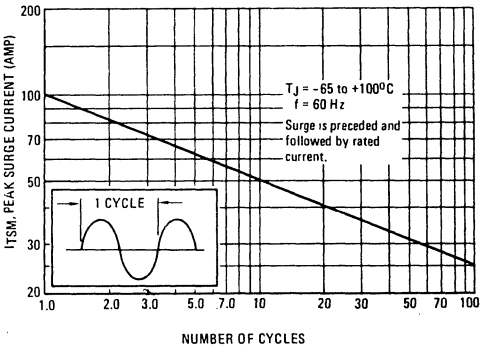
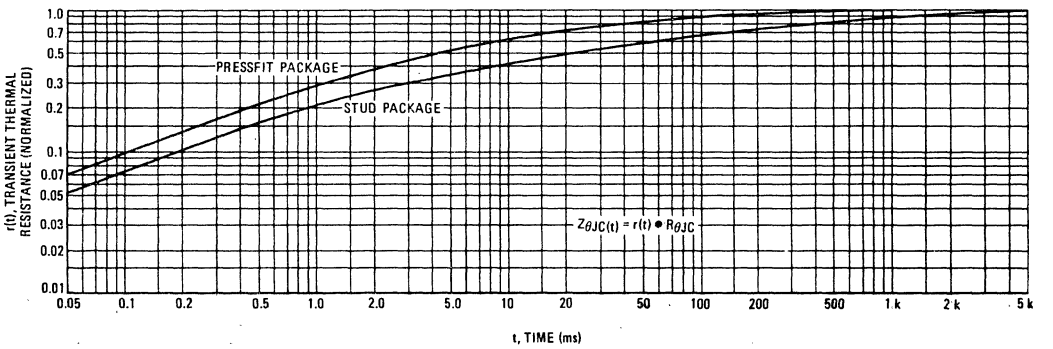


FIGURE 10 – TYPICAL THERMAL RESPONSE



2N5571 thru 2N5574
2N6145 thru 2N6147
T4100M, T4110M

SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- All Diffused and Glass Passivated Junctions for Greater Stability
- Pressfit, Stud and Isolated Stud Packages
- Gate Triggering Guaranteed In All 4 Quadrants

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (T_J = −65 to +100°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
2N5571, 2N5573, 2N6145		200	
2N5572, 2N5574, 2N6146		400	
T4100M, T4110M, 2N6147		600	
*Peak Gate Voltage	V_{GM}	20	Volts
*RMS On-State Current	$I_{T(RMS)}$		Amp
(T_C = −65 to +80°C)		15	
(T_C = +85°C)		10	
*Peak Non-Repetitive Surge Current (One Full cycle of surge current at 60 Hz, preceeded and followed by rated current, T_C = +80°C)	I_{TSM}	100	Amp
Circuit Fusing (T_C = −65 to +80°C, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
Peak Gate Power	P_{GM}		Watts
*(T_C = 80°C, Pulse Width = 1.0 μs) 2N5571 thru 2N5574		16	
T4100M, T4110M		16	
*(T_C = 80°C, Pulse Width = 2.0 μs) 2N6145 thru 2N6147		20	
*Average Gate Power (T_C = +80°C, Pulse Width = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Operating Junction Temperature Range	T_J	-65 to +100	°C
*Storage Temperature Range	T_{stg}	-65 to +150	°C
Stud Torque *2N5573, 2N5574, T4110M *2N6145, 2N6146, 2N6147	—	30	in. lb.

THERMAL CHARACTERISTICS

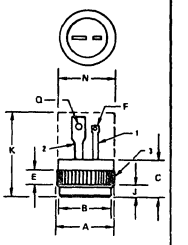
Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

*Indicates JEDEC Registered Data.

TRIACS

15 AMPERES RMS
200–600 VOLTS

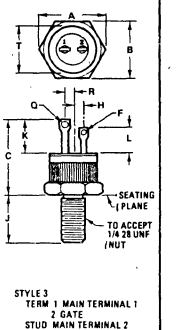
2N5571
2N5572
T4100M



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	12.73	12.83	0.501	0.505
B	11.81	12.06	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54	–	0.100	–
F	0.89	2.16	0.035	0.085
J	2.04	2.46	0.080	0.097
K	–	20.32	–	0.800
N	–	12.95	–	0.510
Q	1.65	4.06	0.065	0.160

CASE 174-03

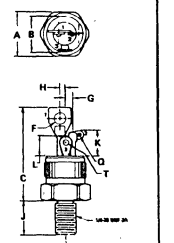
2N5573
2N5574
T4110M



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	0.89	2.16	0.035	0.085
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	1.65	4.06	0.065	0.160
R	1.65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505

CASE 175-02

2N6145
2N6146
2N6147



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	32.51	–	1.280
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.60	2.01	0.063	0.079
J	10.67	11.56	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6.48	6.99	0.255	0.275
Q	1.40	2.16	0.055	0.085
T	3.43	3.81	0.135	0.150

CASE 311-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and either polarity of MT2 to MT1 voltage unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current V_D = Rated V_{DRM} @ T_C = 100°C	I_{DRM}	–	–	2.0	mA
*Peak On-State Voltage I_{TM} = 21 A Peak, Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤2.0%	V_{TM}	–	1.3	1.8	Volts
Gate Trigger Current, Continuous dc (1) V_D = 12 Vdc, R_L = 30 ohms	I_{GT}				mA
MT2 (+), G(+); MT2(–), G(–)		–	–	50	
MT2 (+), G(–); MT2(–), G(+)		–	–	80	
*MT2 (+), G(+); MT2(–), G(–), T_C = -65°C		–	–	150	
*MT2 (+), G(–); MT2(–), G(+), T_C = -65°C		–	–	200	
Gate Trigger Voltage, Continuous dc (All Quadrants) V_D = 12 Vdc, R_L = 30 ohms	V_{GT}				Volts
T_C = 25°C		–	–	2.5	
*T_C = -65°C		–	–	4.0	
*V_D = Rated V_{DRM}, R_L = 10 k ohms, T_C = +100°C		0.2	–	–	
Holding Current V_D = 12 Vdc, Gate Open Initiating Current = 500 mA	I_H				mA
T_C = 25°C		–	–	75	
*T_C = -65°C		–	–	300	
Gate Controlled Turn-On Time Rated V_{DRM}, I_{TM} = 21 A Peak, I_{GT} = 160 mA, Rise Time ≤ 0.1 μs, Pulse Width = 2.0 μs	t_{gt}	–	1.0	2.0	μs
*Critical Rate-of-Rise of Commutation Voltage Rated V_{DRM}, I_{TM} = 21 A Peak, Commutating di/dt = 8.0 A/ms, gate unenergized	dv/dt(c)				V/μs
T_C = 80°C 2N5571 thru 2N5574, T4100M, T4110M		2.0	10	–	
T_C = 75°C 2N6145 thru 2N6147		2.0	10	–	
Critical Rate-of-Rise of Off-State Voltage Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 100°C:	dv/dt				V/μs
*2N5571, 2N5573, 2N6145		30	150	–	
*2N5572, 2N5574, 2N6146		20	100	–	
T4100M, T4110M, 2N6147		10	75	–	

*Indicates JEDEC Registered Data.

(1)All Voltage polarity reference to main terminal 1.

7

FIGURE 1 – RMS CURRENT DERATING

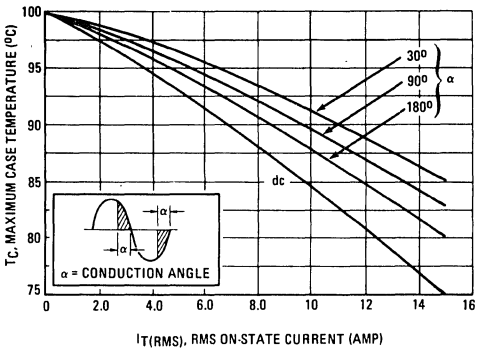


FIGURE 2 – ON-STATE POWER DISSIPATION

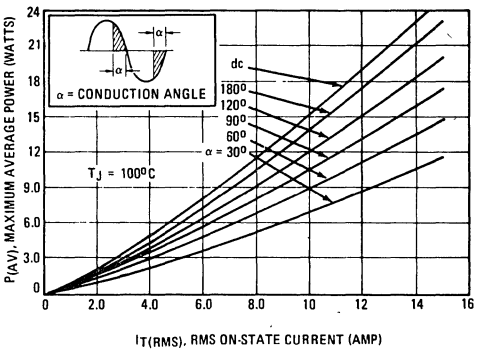


FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

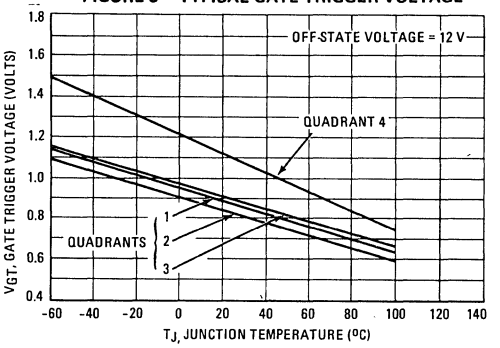


FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

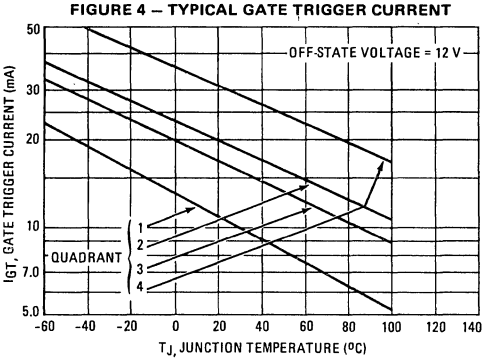


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FIGURE 5 – MAXIMUM ON-STATE CHARACTERISTICS

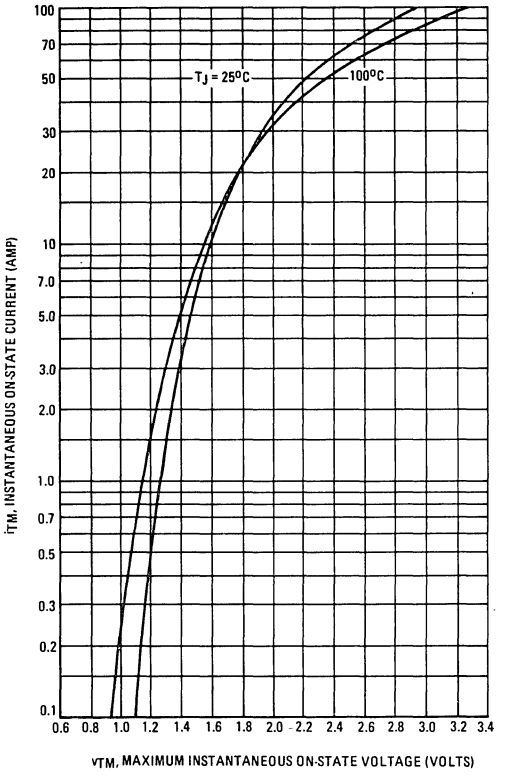


FIGURE 6 – TYPICAL HOLDING CURRENT

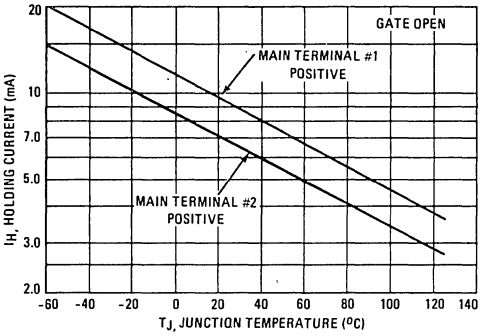


FIGURE 7 – MAXIMUM NON-REPETITIVE SURGE CURRENT

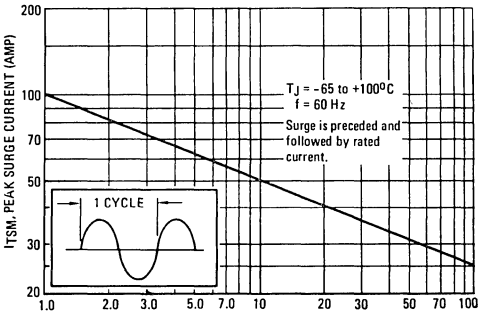
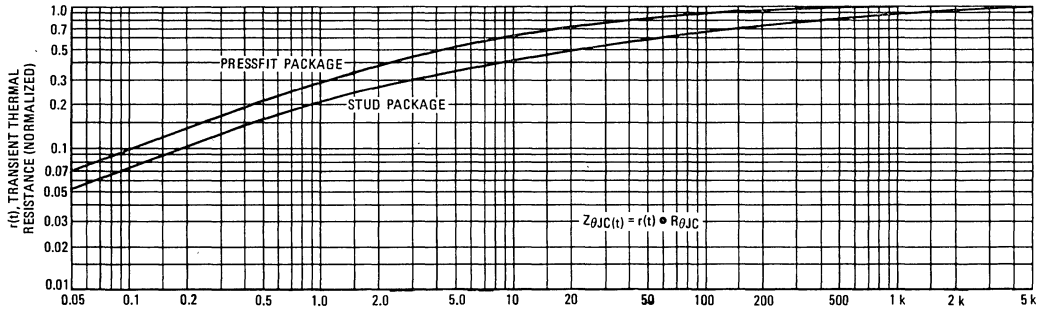
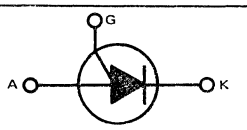


FIGURE 8 – TYPICAL THERMAL RESPONSE



2N6027
2N6028



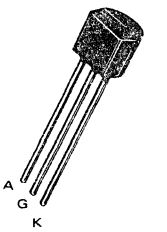
SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS

. . . designed to enable the engineer to "program" unijunction characteristics such as R_{BB}, η, I_V, and I_P by merely selecting two resistor values. Application includes thyristor-trigger, oscillator, pulse and timing circuits. These devices may also be used in special thyristor applications due to the availability of an anode gate. Supplied in an inexpensive TO-92 plastic package for high-volume requirements, this package is readily adaptable for use in automatic insertion equipment.

- Programmable – R_{BB}, η, I_V and I_P.
- Low On-State Voltage – 1.5 Volts Maximum @ I_F = 50 mA
- Low Gate to Anode Leakage Current – 10 nA Maximum
- High Peak Output Voltage – 11 Volts Typical
- Low Offset Voltage – 0.35 Volt Typical (R_G = 10 k ohms)

PROGRAMMABLE UNIJUNCTION TRANSISTORS

40 VOLTS
375 mW



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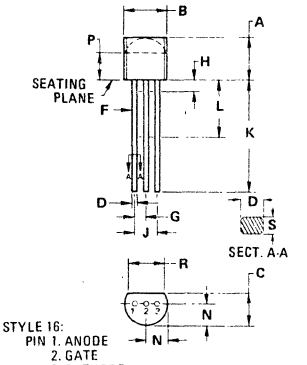
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Power Dissipation Derate Above 25°C	P_F $1/\theta_{JA}$	300 4.0	mW mW/°C
*DC Forward Anode Current Derate Above 25°C	I_T	150 2.67	mA mA/°C
*DC Gate Current	I_G	±50	mA
Repetitive Peak Forward Current 100 μs Pulse Width, 1.0% Duty Cycle *20 μs Pulse Width, 1.0% Duty Cycle	I_{TRM}	 1.0 2.0	 Amp Amp
Non-Repetitive Peak Forward Current 10 μs Pulse Width	I_{TSM}	5.0	Amp
*Gate to Cathode Forward Voltage	V_{GKF}	40	Volt
*Gate to Cathode Reverse Voltage	V_{GKR}	-5.0	Volt
*Gate to Anode Reverse Voltage	V_{GAR}	40	Volt
*Anode to Cathode Voltage (1)	V_{AK}	±40	Volt
Operating Junction Temperature Range	T_J	-50 to +100	°C
*Storage Temperature Range	T_{stg}	-55 to +150	°C

*Indicates JEDEC Registered Data
(1) Anode positive, R_{GK} = 1000 ohms
Anode negative, R_{GK} = open



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

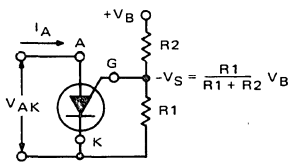
CASE 29-02
TO-92
PLASTIC

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

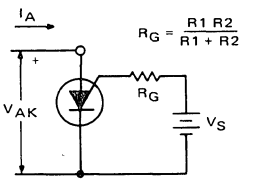
Characteristic		Figure	Symbol	Min	Typ	Max	Unit
*Peak Current		2,9,11	I_P				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6027			–	1.25	2.0	
	2N6028			–	0.08	0.15	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6027			–	4.0	5.0	
	2N6028			–	0.70	1.0	
*Offset Voltage		1	V_T				Volts
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6027			0.2	0.70	1.6	
	2N6028			0.2	0.50	0.6	
(V_S = 10 Vdc, R_G = 10 k ohms)	(Both Types)			0.2	0.35	0.6	
*Valley Current		1,4,5,	I_V				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6027			–	18	50	
	2N6028			–	18	25	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6027			70	270	–	
	2N6028			25	270	–	
(V_S = 10 Vdc, R_G = 200 Ohms)	2N6027			1.5	–	–	mA
	2N6028			1.0	–	–	
* Gate to Anode Leakage Current		–	I_{GAO}				nAdc
(V_S = 40 Vdc, T_A = 25°C, Cathode Open)				–	1.0	10	
(V_S = 40 Vdc, T_A = 75°C, Cathode Open)				–	3.0	–	
Gate to Cathode Leakage Current (V_S = 40 Vdc, Anode to Cathode Shorted)		–	I_{GKS}	–	5.0	50	nAdc
*Forward Voltage (I_F = 50 mA Peak)		1,6	V_F	–	0 8	1.5	Volts
*Peak Output Voltage (V_B = 20 Vdc, C_C = 0.2 μF)		3,7	V_o	6.0	11	–	Volts
Pulse Voltage Rise Time (V_B = 20 Vdc, C_C = 0.2 μF)		3	t_r	–	40	80	ns

*Indicates JEDEC Registered Data

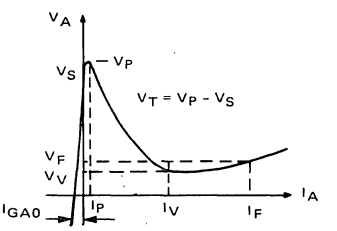
FIGURE 1 – ELECTRICAL CHARACTERIZATION



1A – Programmable Unijunction with "Program" Resistors R1 and R2



1B – Equivalent Test Circuit for Figure 1A used for electrical characteristics testing (also see Figure 2)



1C – Electrical Characteristics

FIGURE 2 – PEAK CURRENT (I_P) TEST CIRCUIT

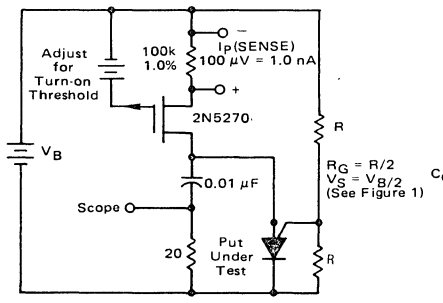
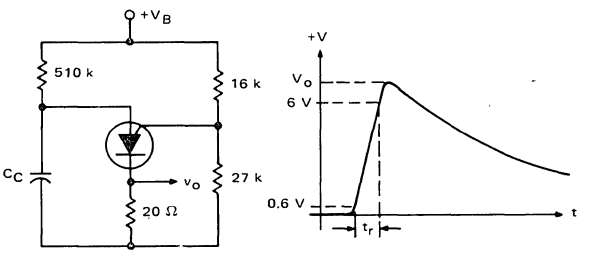


FIGURE 3 – V_o AND t_r TEST CIRCUIT



TYPICAL VALLEY CURRENT BEHAVIOR

FIGURE 4 – EFFECT OF SUPPLY VOLTAGE

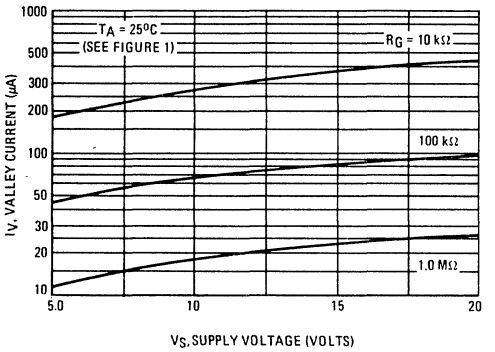


FIGURE 5 – EFFECT OF TEMPERATURE

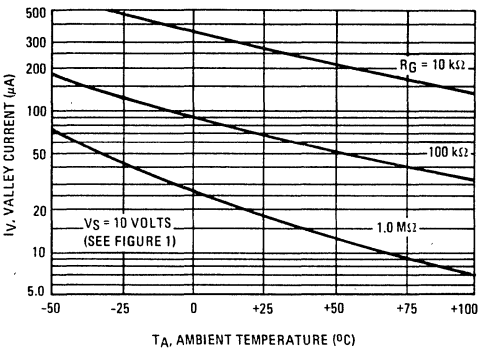


FIGURE 6 – FORWARD VOLTAGE

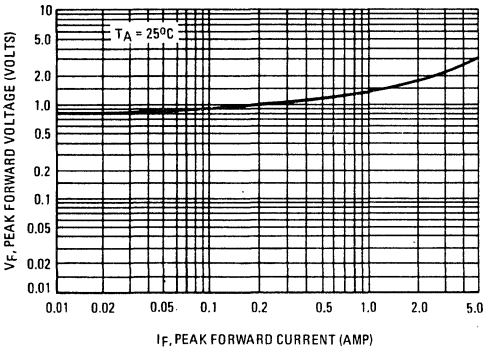


FIGURE 7 – PEAK OUTPUT VOLTAGE

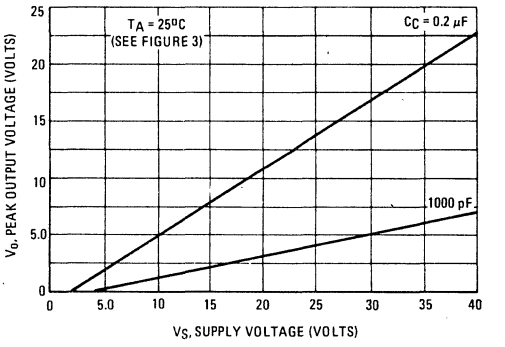
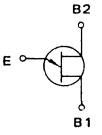
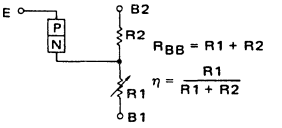


FIGURE 8 – STANDARD UNIJUNCTION
COMPARED TO PROGRAMMABLE UNIJUNCTION

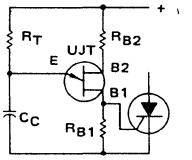
STANDARD UNIJUNCTION



Circuit Symbol

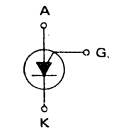


Equivalent Circuit

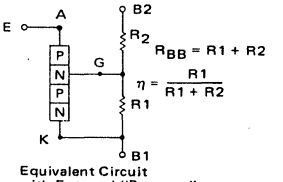


Typical Application

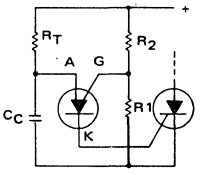
PROGRAMMABLE UNIJUNCTION



Circuit Symbol



Equivalent Circuit
with External "Program"
Resistors R1 and R2



Typical Application

TYPICAL PEAK CURRENT BEHAVIOR

2N6027

FIGURE 9 – EFFECT OF SUPPLY VOLTAGE AND R_G

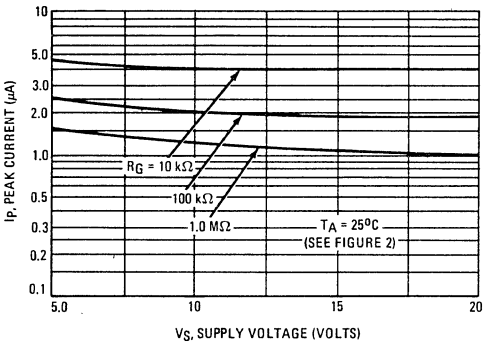
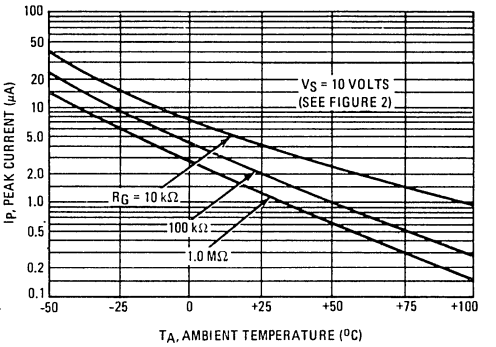


FIGURE 10 – EFFECT OF TEMPERATURE AND R_G



2N6028

FIGURE 11 – EFFECT OF SUPPLY VOLTAGE AND R_G

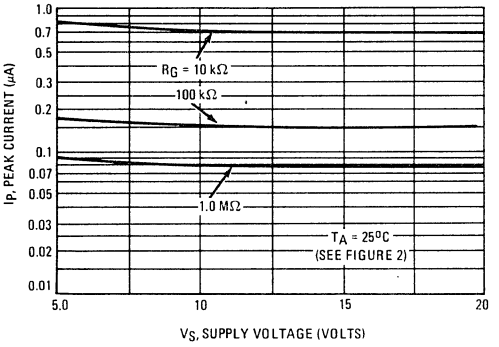
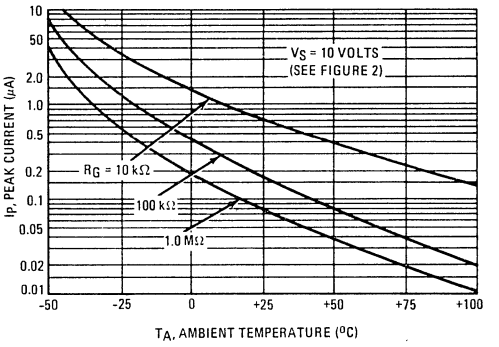
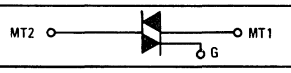


FIGURE 12 – EFFECT OF TEMPERATURE AND R_G



7

2N6068,A,B (SILICON)
thru
2N6075,A,B



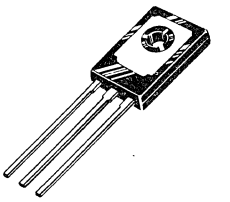
SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Sensitive Gate Triggering (A and B versions) Uniquely Compatible for Direct Coupling to TTL, HTL, CMOS and Operational Amplifier Integrated Circuit Logic Functions.
- Gate Triggering 2 Mode – 2N6068 thru 2N6075
  4 Mode – 2N6068A,B thru 2N6075A,B
- Blocking Voltages to 600 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability

SENSITIVE GATE

TRIACS
(THYRISTORS)
4 AMPERES RMS
25 THRU 600 VOLTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Repetitive Peak Off-State Voltage, Note 1 (T_J = 110°C) 2N6068,A,B	V_{DRM}	25	Volts
2N6069,A,B		50	
2N6070,A,B		100	
2N6071,A,B		200	
2N6072,A,B		300	
2N6073,A,B		400	
2N6074,A,B		500	
2N6075,A,B		600	
*On-State Current RMS (T_C = 85°C)	$I_{T(RMS)}$	4.0	Amp
*Peak Surge Current (One Full cycle, 60 Hz, T_J = -40 to +110°C)	I_{TSM}	30	Amp
Circuit Fusing Considerations (T_J = -40 to +110°C, t = 1.0 to 8.3 ms)	I^2t	3.6	A^2s
*Peak Gate Power	P_{GM}	10	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Gate Voltage	V_{GM}	5.0	Volts
*Operating Junction Temperature Range	T_J	-40 to +110	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C
Mounting Torque (6-32 Screw), Note 2	—	8.0	in. lb.

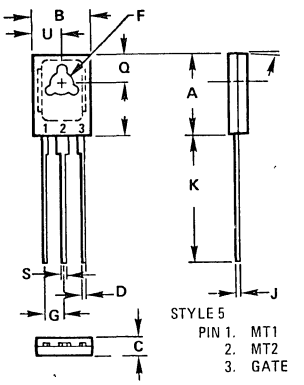
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R\theta_{JC}$	3.5	°C/W
Thermal Resistance, Case to Ambient	$R\theta_{CA}$	60	°C/W

*Indicates JEDEC Registered Data

NOTES:

1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. Torque rating applies with use of torque washer (Shakeproof WD19523 or equivalent). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Main terminal 2 and heatsink contact pad are common.
   For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +200°C, for 10 seconds. Consult factory for lead bending options.



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	9.91	11.43	0.390	0.450
B	6.86	8.38	0.270	0.330
C	1.78	3.30	0.070	0.130
D	0.51	0.66	0.020	0.026
F	2.92	3.00	0.115	0.118
G	2.29 BSC		0.090 BSC	
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
Q	3.30	4.45	0.130	0.175
S	0.64	0.89	0.025	0.035
U	3.81 NOM		0.150 NOM	

CASE 77-02

2N6068,A,B thru 2N6075,A,B (continued)

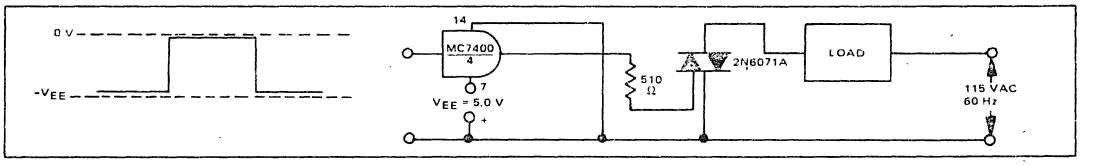
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

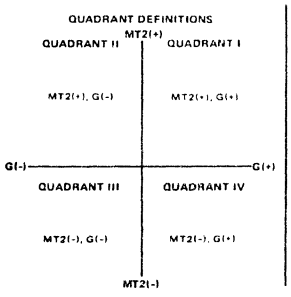
Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 110°C, Gate Open	I_{DRM}	–	–	2.0	mA
*On-State Voltage (Either Direction) I_{TM} = 6.0 A Peak	V_{TM}	–	–	2.0	Volts
*Peak Gate Trigger Voltage Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms, T_J = -40°C MT2 (+), G(+); MT2 (–), G(–) All Types MT2 (+), G(–); MT2 (–), G(+) 2N6068A,B thru 2N6075A,B Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = 110°C MT2 (+), G(+); MT2 (–), G(–) All Types MT2 (+), G(–); MT2 (–), G(+) 2N6068A,B thru 2N6075A,B	V_{GTM}	 – – 0.2 0.2	 1.4 1.4 – –	 2.5 2.5 – –	Volts
*Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, T_J = -40°C Initiating Current = 1.0 Adc 2N6068 thru 2N6075 2N6068A,B thru 2N6075A,B T_J = 25°C 2N6068 thru 2N6075 2N6068A,B thru 2N6075A,B	I_H	 – – – –	 – – – –	 70 30 30 15	mA
Turn-On Time (Either Direction) I_{TM} = 14 Adc, I_{GT} = 100 mAdc	t_{on}	–	1.5	–	μs
Blocking Voltage Application Rate at Commutation @ V_{DRM}, T_J = 85°C, Gate Open	dv/dt	–	5.0	–	V/μs

	Type	I_{GTM} @ T_J	QUADRANT (See Definition Below) I mA	II mA	III mA	IV mA
*Peak Gate Trigger Current Main Terminal Voltage = 12 Vdc, R_L = 100 ohms Maximum Value	2N6068 thru 2N6075	+25°C	30	–	30	–
		-40°C	60	–	60	–
	2N6068A thru 2N6075A	+25°C	5.0	5.0	5.0	10
		-40°C	20	20	20	30
	2N6068B thru 2N6075B	+25°C	3.0	3.0	3.0	5.0
		-40°C	15	15	15	20

*Indicates JEDEC Registered Data.

SAMPLE APPLICATION:
TTL-SENSITIVE GATE 4 AMPERE TRIAC TRIGGERS IN MODES II AND III





Trigger devices are recommended for gating on Triacs. They provide

1. Consistent predictable turn-on points
2. Simplified circuitry
3. Fast turn-on time for cooler, more efficient and reliable operation

For 2N6068 Thru 2N6075

ELECTRICAL CHARACTERISTICS of RECOMMENDED BIDIRECTIONAL SWITCHES

USAGE	General		Lamp Dimmer
PART NUMBER	MBS4991	MBS4992	MBS100
V_S	6.0 - 10 V	7.5 - 9.0 V	30 - 50 V
I_S	350 μA Max	120 μA Max	100 - 400 μA
$V_{S1} - V_{S2}$	0.5 V Max	0.2 V Max	0.35 V Max
Temperature Coefficient	0.02%/°C Typ		

See AN 526 for Theory and Characteristics of Silicon Bidirectional Switches

SENSITIVE GATE LOGIC REFERENCE

IC LOGIC FUNCTIONS	FIRING QUADRANT I	II	III	IV
TTL		2N6068A Series	2N6068A Series	
HTL		2N6068A Series	2N6068A Series	
McMOS (NAND)	2N6068B Series			2N6068B Series
McMOS (Buffer)		2N6068B Series	2N6068B Series	
Operational Amplifier	2N6068A Series			2N6068A Series
Zero Voltage Switch		2N6068A Series	2N6068A Series	

FIGURE 1 – AVERAGE CURRENT DERATING

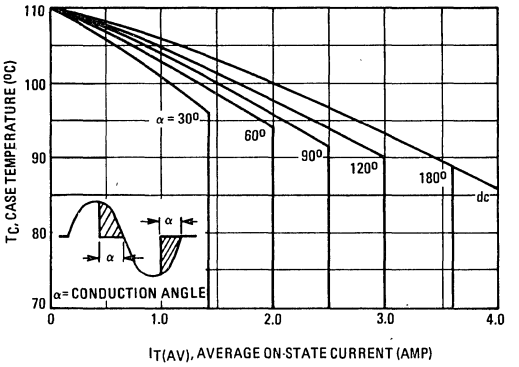


FIGURE 2 – RMS CURRENT DERATING

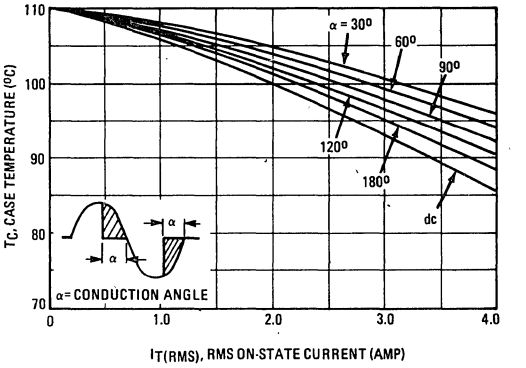


FIGURE 3 – POWER DISSIPATION

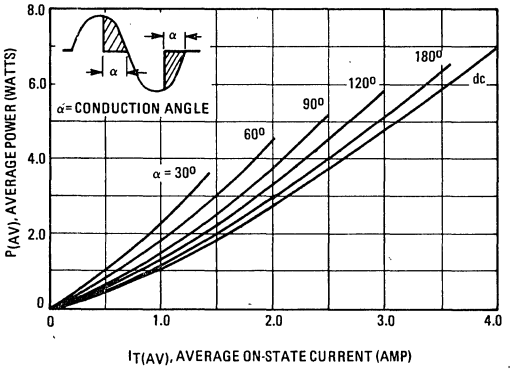


FIGURE 4 – POWER DISSIPATION

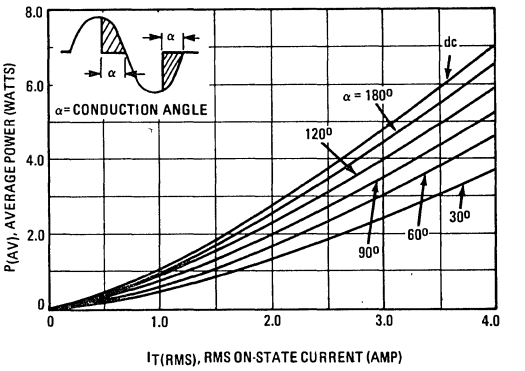


FIGURE 5 – TYPICAL GATE-TRIGGER VOLTAGE

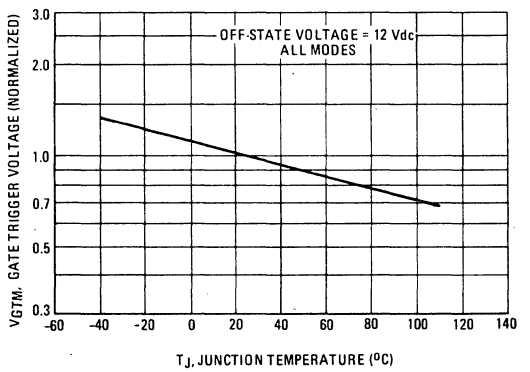


FIGURE 6 – TYPICAL GATE-TRIGGER CURRENT

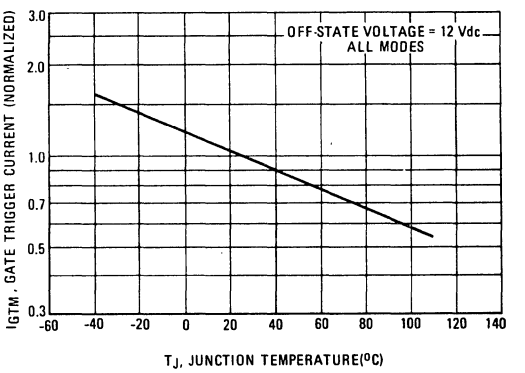


FIGURE 7 – MAXIMUM ON-STATE CHARACTERISTICS

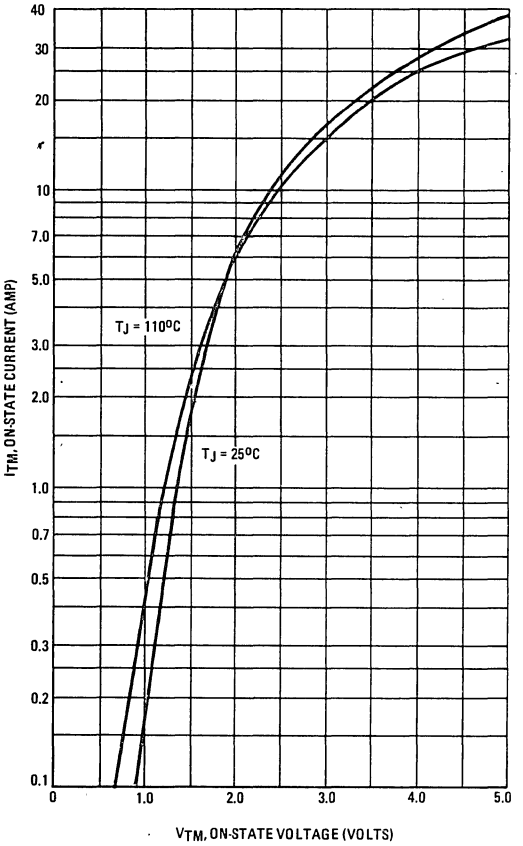


FIGURE 8 – TYPICAL HOLDING CURRENT

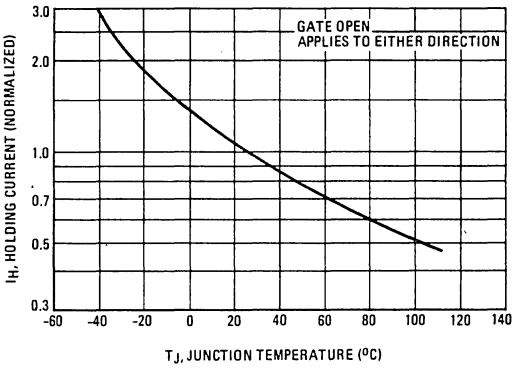


FIGURE 9 – MAXIMUM ALLOWABLE SURGE CURRENT

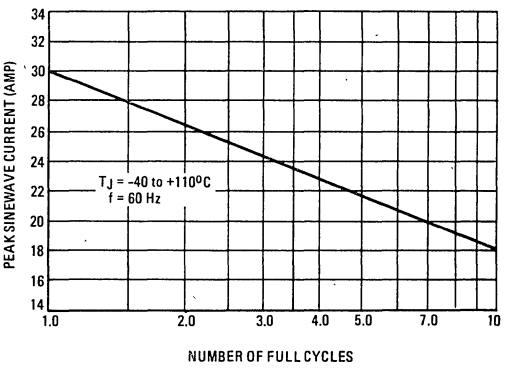
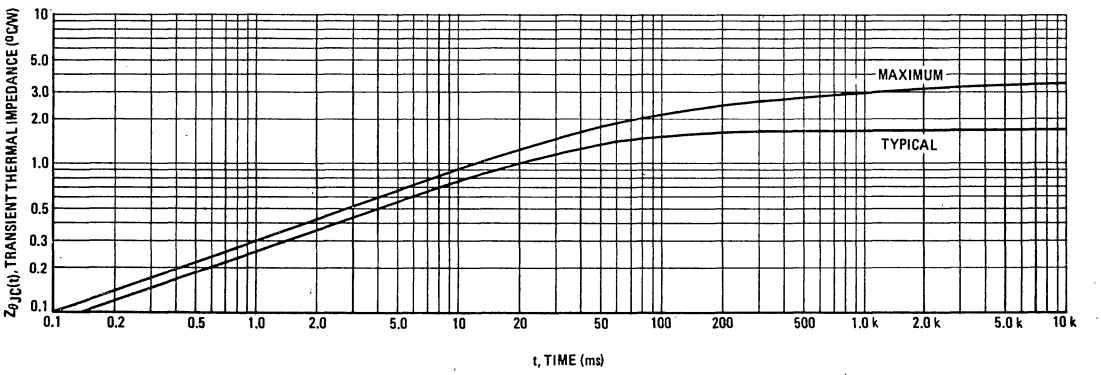
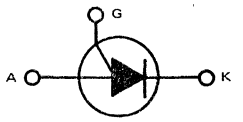


FIGURE 10 – THERMAL RESPONSE



2N6116 2N6117
2N6118

(FORMERLY MPU231, MPU232, MPU233)



SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS

. . . designed to enable the engineer to "program" unijunction characteristics such as R_{BB}, η, I_V, and Ip by merely selecting two resistor values. Application includes thyristor-triggor, oscillator, pulse and timing circuits. These devices may also be used in special thyristor applications due to the availability of an anode gate.

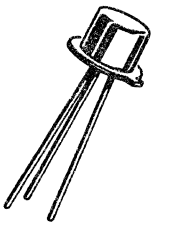
- Programmable – R_{BB}, η, I_V and I_P
- Hermetic TO-18 Package
- Low On-State Voltage – 1.5 Volts Maximum @ I_F = 50 mA
- Low Gate to Anode Leakage Current – 5.0 nA Maximum
- High Peak Output Voltage – 16 Volts Typical
- Low Offset Voltage – 0.35 Volt Typical (R_G = 10 k ohms)

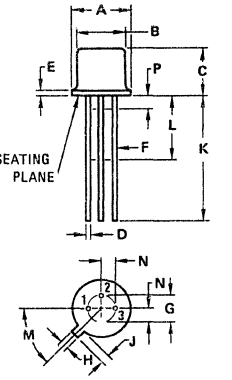
***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Repetitive Peak Forward Current 100 μs Pulse Width, 1.0% Duty Cycle 20 μs Pulse Width, 1.0% Duty Cycle	I_{TRM}	 1.0 2.0	 Amp Amp
Non-Repetitive Peak Forward Current 10 μs Pulse Width	I_{TSM}	5.0	Amp
DC Forward Anode Current Derate Above 25°C	I_T	200 2.0	mA mA/°C
DC Gate Current	I_G	±20	mA
Gate to Cathode Forward Voltage	V_{GKF}	40	Volt
Gate to Cathode Reverse Voltage	V_{GKR}	5.0	Volt
Gate to Anode Reverse Voltage	V_{GAR}	40	Volt
Anode to Cathode Voltage	V_{AK}	±40	Volt
Forward Power Dissipation @ T_A = 25°C Derate Above 25°C	P_F $1/\theta_{JA}$	250 2.5	mW mW/°C
Operating Junction Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data

SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS
40 VOLTS
250 mW





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.406	0.533	0.016	0.021
E	–	0.762	–	0.030
F	0.406	0.483	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

All JEDEC notes and dimensions apply.

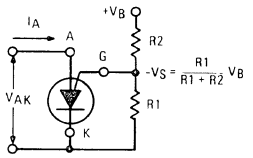
CASE 22-03
(TO-18)

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

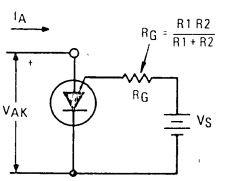
Characteristic		Figure	Symbol	Min	Typ	Max	Unit
Offset Voltage	2N6116	1	V_T	0.2	0.70	1.6	Volts
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6117			0.2	0.50	0.6	
	2N6118			0.2	0.40	0.6	
(V_S = 10 Vdc, R_G = 10 k ohms)	All Types			0.2	0.35	0.6	
Gate to Anode Leakage Current		–	I_{GAO}				nAdc
(V_S = 40 Vdc, T_A = 25°C, Cathode Open)				–	1.0	5.0	
(V_S = 40 Vdc, T_A = 75°C, Cathode Open)				–	30	75	
Gate to Cathode Leakage Current		–	I_{GKS}	–	5.0	50	nAdc
(V_S = 40 Vdc, Anode to Cathode Shorted)							
Peak Current	2N6116	2,9-14	I_P	–	1.25	2.0	μA
(V_S = 10 Vdc, R_G = 10 MΩ)	2N6117			–	0.19	0.3	
	2N6118			–	0.08	0.15	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6116			–	4.0	5.0	
	2N6117			–	1.20	2.0	
	2N6118			–	0.70	1.0	
Valley Current		1,4,5	I_V				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	2N6116, 2N6117			–	18	50	
	2N6118			–	18	25	
(V_S = 10 Vdc, R_G = 10 k ohms)	2N6116			70	270	–	
	2N6117, 2N6118			50	270	–	
Forward Voltage (I_F = 50 mA Peak)		1,6	V_T	–	0.8	1.5	Volts
Peak Output Voltage (V_B = 20 Vdc, C_C = 0.2 μF)		3,7	V_o	6.0	16	–	Volts
Pulse Voltage Rise Time (V_B = 20 Vdc, C_C = 0.2 μF)		3	t_r	–	40	80	ns

*Indicates JEDEC Registered Data

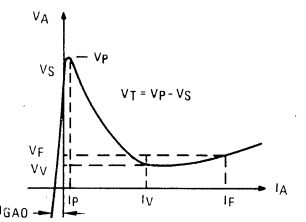
FIGURE 1 – ELECTRICAL CHARACTERIZATION



1A – PROGRAMMABLE UNIJUNCTION WITH "PROGRAM" RESISTORS R1 and R2



1B – EQUIVALENT TEST CIRCUIT FOR FIGURE 1A USED FOR ELECTRICAL CHARACTERISTICS TESTING (ALSO SEE FIGURE 2)



1C – ELECTRICAL CHARACTERISTICS

FIGURE 2 – PEAK CURRENT (I_P) TEST CIRCUIT

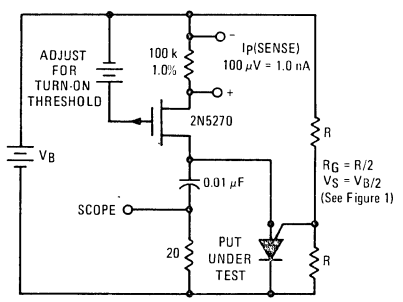
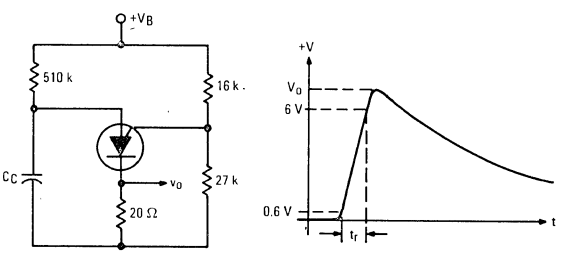


FIGURE 3 – V_o AND t_r TEST CIRCUIT



TYPICAL VALLEY CURRENT BEHAVIOR

FIGURE 4 – EFFECT OF SUPPLY VOLTAGE

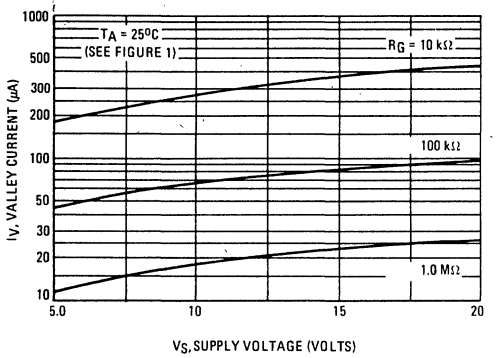


FIGURE 5 – EFFECT OF TEMPERATURE

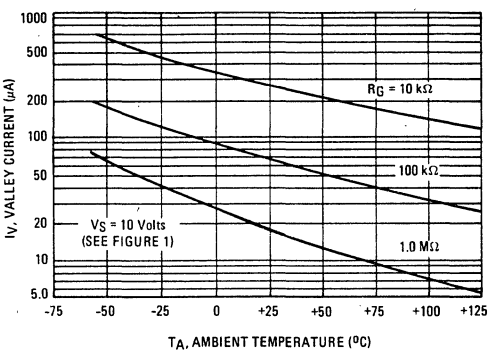


FIGURE 6 – FORWARD VOLTAGE

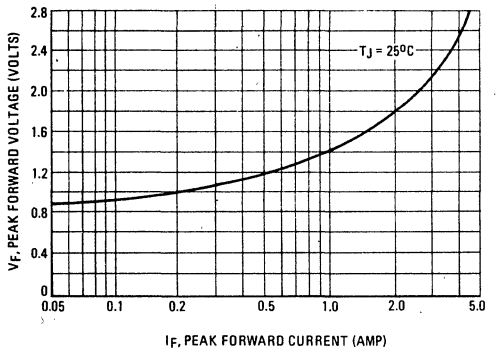


FIGURE 7 – PEAK OUTPUT VOLTAGE

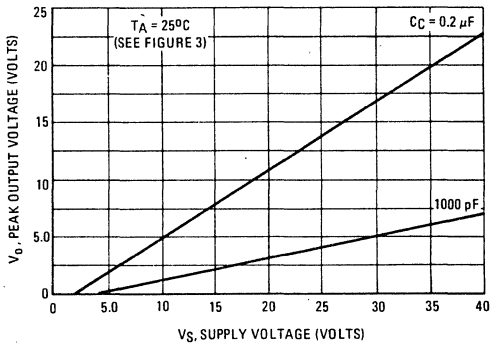
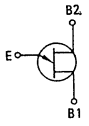
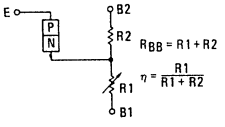


FIGURE 8 – STANDARD UNIJUNCTION
COMPARED TO PROGRAMMABLE UNIJUNCTION

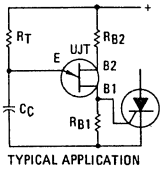
STANDARD UNIJUNCTION



CIRCUIT SYMBOL

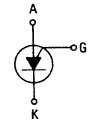


EQUIVALENT CIRCUIT

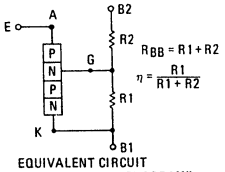


TYPICAL APPLICATION

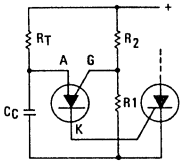
PROGRAMMABLE UNIJUNCTION



CIRCUIT SYMBOL



EQUIVALENT CIRCUIT
WITH EXTERNAL "PROGRAM"
RESISTORS R1 and R2



TYPICAL APPLICATION

TYPICAL PEAK CURRENT BEHAVIOR

2N6116

FIGURE 9 – EFFECT OF SUPPLY VOLTAGE AND R_G

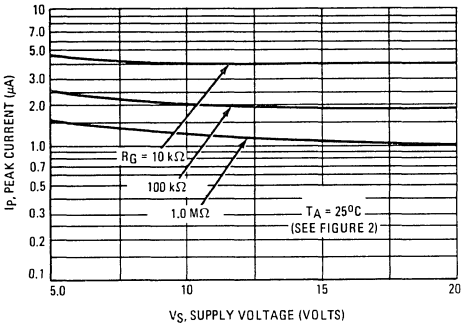
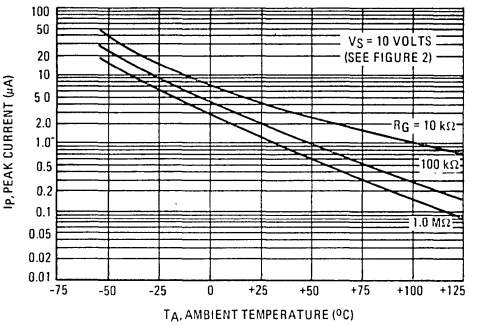


FIGURE 10 – EFFECT OF TEMPERATURE AND R_G



2N6117

FIGURE 11 – EFFECT OF SUPPLY VOLTAGE AND R_G

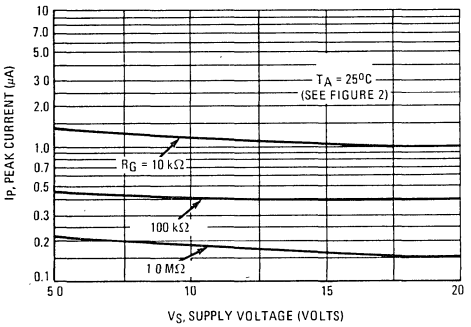
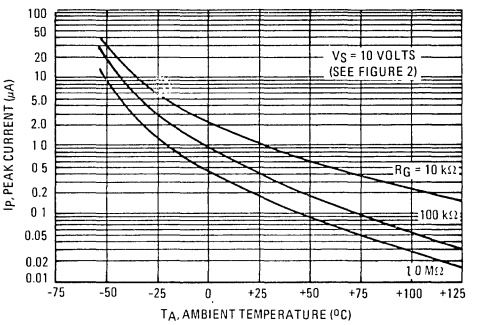


FIGURE 12 – EFFECT OF TEMPERATURE AND R_G



2N6118

FIGURE 13 – EFFECT OF SUPPLY VOLTAGE AND R_G

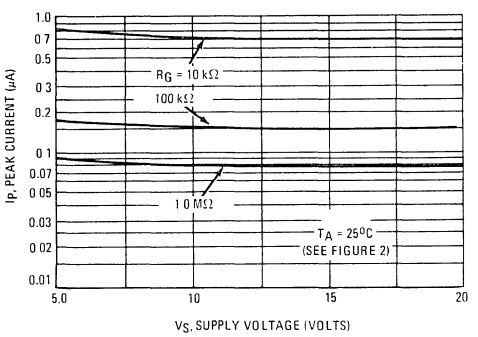
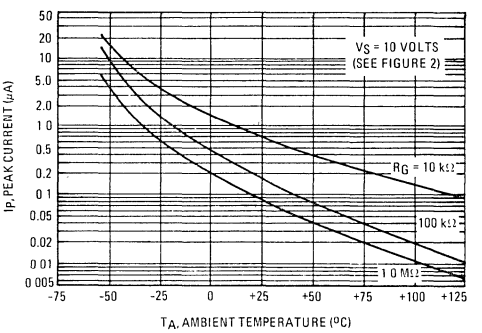


FIGURE 14 – EFFECT OF TEMPERATURE AND R_G



7

2N6151 (SILICON) thru 2N6156

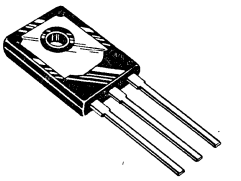
SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- All Diffused and Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two (2N6154, 2N6155, 2N6156) or Four Modes (2N6151, 2N6152, 2N6153)

TRIACS (THYRISTORS)

10 AMPERES RMS



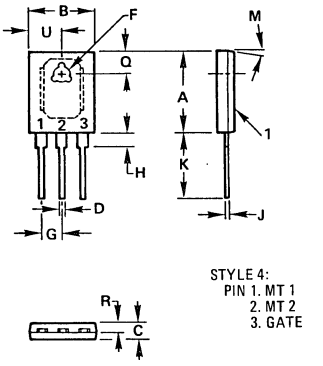
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
* Repetitive Peak Off-State Voltage, Note 1 (T_J = -40 to +100°C) ½ Sine Wave 50 to 60 Hz, Gate Open Peak Principle Voltage	V_{DRM}		Volts
2N6151, 2N6154		200	
2N6152, 2N6155		400	
2N6153, 2N6156		600	
*Peak Gate Voltage	V_{GM}	10	Volts
*On-State Current RMS (T_C = -40 to +75°C)	$I_{T(RMS)}$	10	Amp
Full Cycle Sine Wave 50 to 60 Hz (T_C = +90°C)		5.0	
*Peak Surge Current (One Full Cycle, 60 Hz, T_J = +75°C) preceded and followed by 10 A Current	I_{TSM}	100	Amp
Circuit Fusing Considerations (T_J = -40 to +100°C, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
*Peak Gate Power (T_J = +75°C, Pulse Width = 2.0 μs)	P_{GM}	20	Watts
*Average Gate Power (T_J = +75°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Operating Junction Temperature Range	T_J	-40 to +100	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C
*Mounting Torque (6-32 Screw), Note 2	—	8.0	in. lb

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
* Thermal Resistance, Junction to Case	$R\theta_{JC}$	2.0	°C/W
Thermal Resistance Case to Ambient	$R\theta_{CA}$	50	°C/W

*Indicates JEDEC Registered Data.



STYLE 4:
PIN 1. MT 1
2. MT 2
3. GATE

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255

CASE 90-05

7

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 100°C, Gate Open	I_{DRM}	–	–	2.0	mA
*On-State Voltage (Either Direction) I_{TM} = 14 A Peak; Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0 %	V_{TM}	–	1.3	1.8	Volts
Gate Trigger Current, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	I_{GT}				mA
MT2 (+), G(+) All Types		–	6.0	50	
MT2 (+), G(–) 2N6151 thru 2N6153		–	6.0	75	
MT2 (–), G(–) All Types		–	10	50	
MT2 (–), G(+) 2N6151 thru 2N6153		–	25	75	
*MT2 (+), G(+); MT2 (–), G(–) T_C = -40°C All Types		–	–	100	
*MT2 (+), G(–); MT2 (–), G(+) T_C = -40°C 2N6151 thru 2N6153		–	–	125	
Gate Trigger Voltage, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	V_{GT}				Volts
MT2 (+), G(+) All Types		–	0.9	2.0	
MT2 (+), G(–) 2N6151 thru 2N6153		–	0.9	2.5	
MT2 (–), G(–) All Types		–	1.1	2.0	
MT2 (–), G(+) 2N6151 thru 2N6153		–	1.4	2.5	
*MT2 (+), G(+); MT2 (–), G(–) T_C = -40°C All Types		–	–	2.5	
*MT2 (+), G(–); MT2 (–), G(+) T_C = -40°C 2N6151 thru 2N6153		–	–	3.0	
Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = 100°C					
*MT2 (+), G(+); MT2 (–), G(–) All Types		0.2	–	–	
*MT2 (+), G(–); MT2 (–), G(+) 2N6151 thru 2N6153		0.2	–	–	
Holding Current (Either Direction) Main Terminal Voltage = 12 Vdc, Gate Open, Initiating Current = 200 mA	I_H				mA
T_C = 25°C		–	6.0	40	
T_C = -40°C		–	–	75*	
*Turn-On Time Main Terminal Voltage = Rated V_{DRM}, I_{TM} = 14 A Gate Source Voltage = 12 V, R_S = 100 Ohms, Rise Time = 0.1 μs, Pulse Width = 2.0 μs	tgt	–	1.5	2.0	μs
Blocking Voltage Application Rate at Commutation, f = 60 Hz, T_C = 75°C On-State Conditions: I_{TM} = 14 A, Pulse Width = 4.0 ms, di/dt = 5.3 A/ms Off-State Conditions: Main Terminal Voltage = Rated V_{DRM} (200 μs min), Gate Source Voltage = 0 V, R_S = 100 Ω	dv/dt	–	5.0	–	V/μs

*Indicates JEDEC Registered Data

NOTES:

1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. Torque rating applies with use of torque washer (Shakeproof WD19522 #6 or equivalent). Mounting torque in excess of 8 in. lbs. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common.
   For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +230°C.

Trigger devices are recommended for gating on Triacs

Triggers Provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

Electrical Characteristics	For General Usage		For Lamp Dimmer
Symbol	MBS4991	MBS4992	MBS100
V_S =	6.0 –10 V	7.5–9.0 V	3.0–5.0 V
I_S =	350 μA Max	120 μA Max	100–400 μA
V_{S1}–V_{S2} =	0.5 V Max	0.2 V Max	0.35 V Max
Temperature Coefficient = 0.02%/°C Typ			

See AN-526 for Theory and Characteristics of Silicon Bidirectional Switches.

FIGURE 1 – AVERAGE CURRENT DERATING

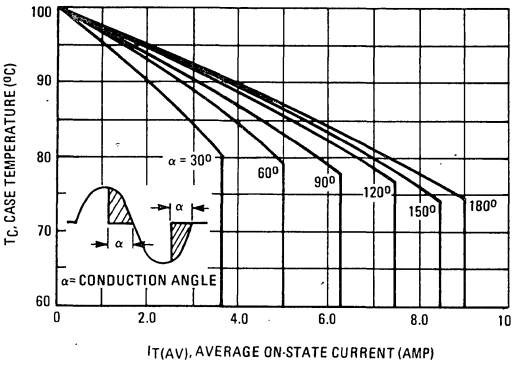


FIGURE 2 – RMS CURRENT DERATING

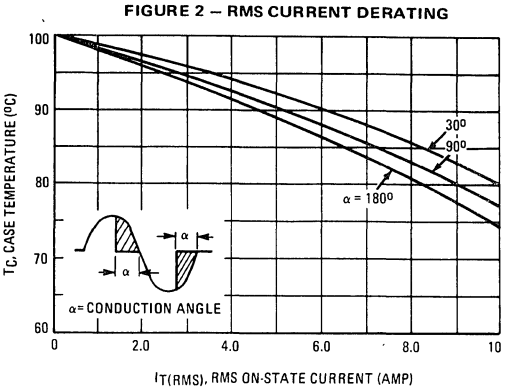


FIGURE 3 – POWER DISSIPATION

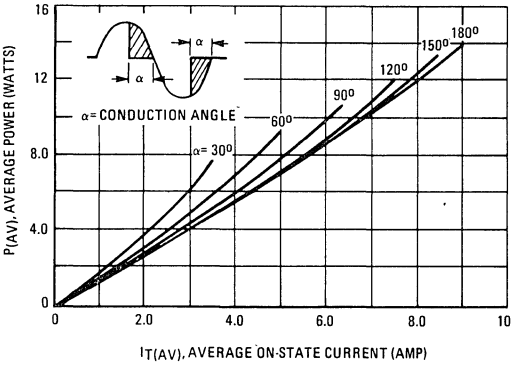


FIGURE 4 – POWER DISSIPATION

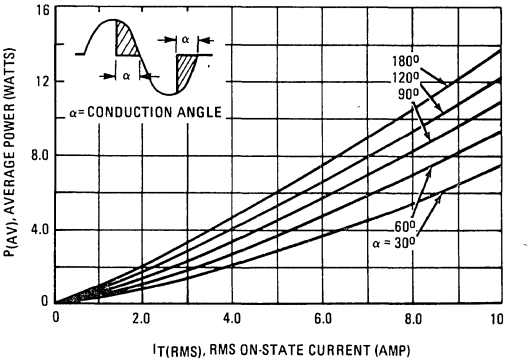


FIGURE 5 – TYPICAL GATE TRIGGER VOLTAGE

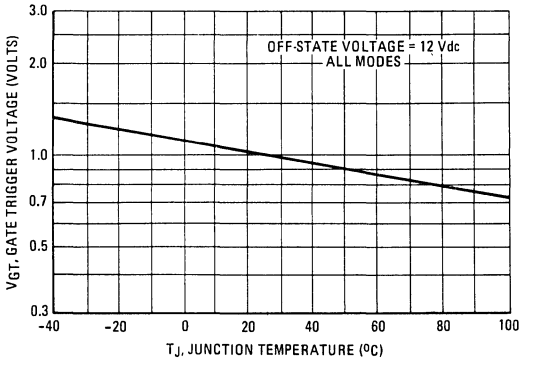


FIGURE 6 – TYPICAL GATE TRIGGER CURRENT

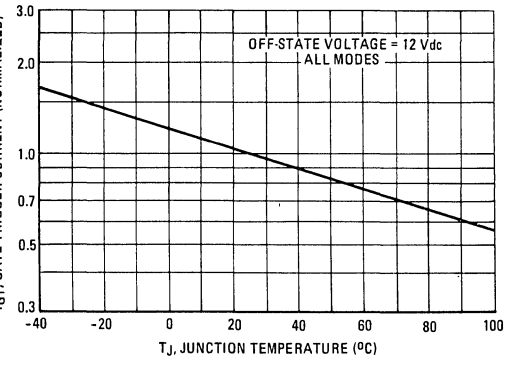


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FIGURE 7 – MAXIMUM ON-STATE CHARACTERISTICS

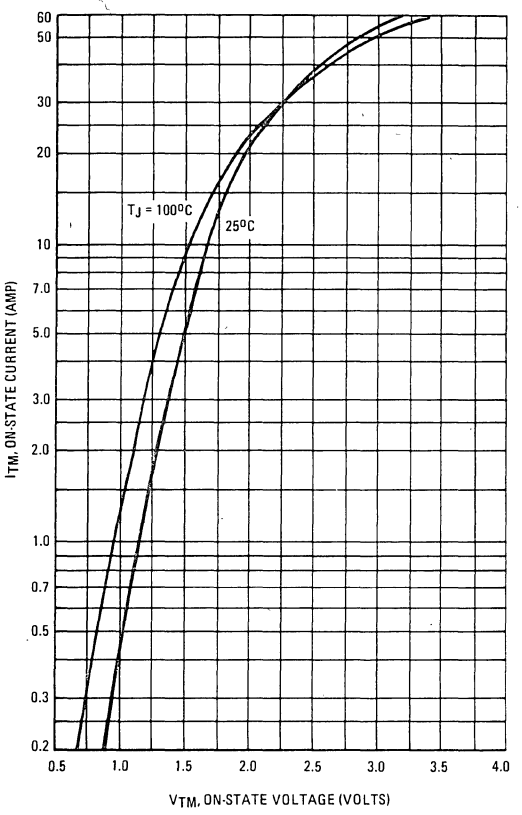

FIGURE 8 – TYPICAL HOLDING CURRENT

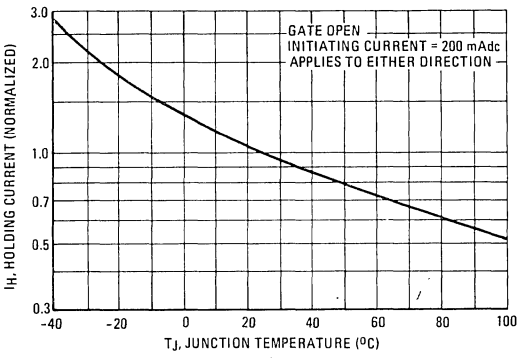

FIGURE 9 – MAXIMUM ALLOWABLE SURGE CURRENT

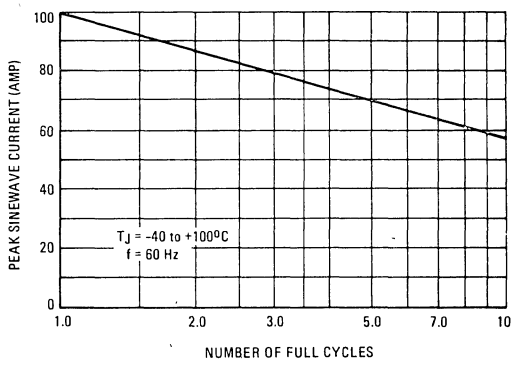

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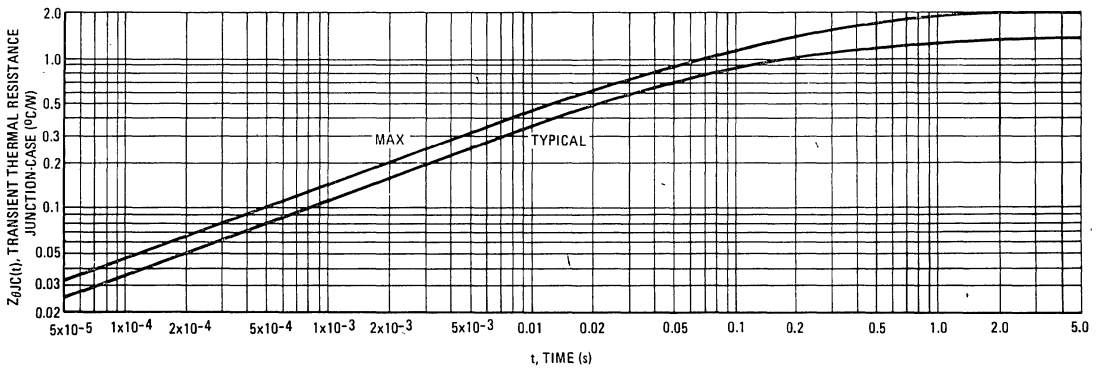
FIGURE 10 – THERMAL RESPONSE



2N6157 thru 2N6165

SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire
- Isolated Stud for Ease of Assembly
- Gate Triggering Guaranteed In All 4 Quadrants

TRIACS

30 AMPERES RMS
200–600 VOLTS

MAXIMUM RATINGS

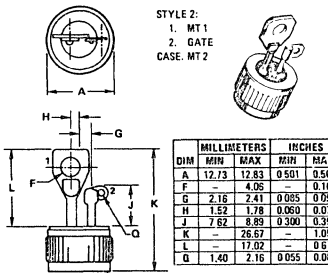
Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (T_J = -65 to +125°C) 1/2 Sine Wave 50 to 60 Hz, Gate Open *Peak Principal Voltage 2N6157, 2N6160, 2N6163 2N6158, 2N6161, 2N6164 2N6159, 2N6162, 2N6165	V_{DRM}	200 400 600	Volts
*Peak Gate Voltage	V_{GM}	10	Volts
*RMS On-State Current (T_C = -65 to +85°C) (T_C = +100°C) Full Sine Wave, 50 to 60 Hz	$I_{T(RMS)}$	30 20	Amp
*Peak Non-Repetitive Surge Current (One Full Cycle of surge current at 60 Hz, preceeded and followed by a 30 ARMS current, T_J = +125°C)	I_{TSM}	250	Amp
Circuit Fusing Considerations (T_J = -65 to +125°C, t = 1.0 to 8.3 ms)	I^2t	210	A^2s
*Peak Gate Power (T_J = +80°C, Pulse Width = 2.0 μs)	P_{GM}	20	Watts
*Average Gate Power (T_J = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Operating Junction Temperature Range	T_J	-65 to +125	°C
*Storage Temperature Range	T_{stg}	-65 to +150	°C
*Stud Torque 2N6160 thru 2N6165	–	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R\theta_{JC}$	1.0	°C/W

*Indicates JEDEC Registered Data.

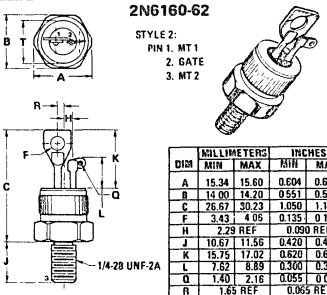
2N6157-59



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	12.73	12.83	0.501	0.505
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.52	1.78	0.060	0.070
J	7.62	8.89	0.300	0.350
K	–	26.67	–	1.050
L	–	17.02	–	0.670
Q	1.40	2.16	0.055	0.085

CASE 310-01

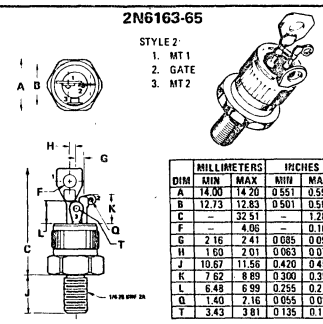
2N6160-62



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

CASE 263-03

2N6163-65



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	32.51	–	1.280
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.60	2.01	0.063	0.079
J	10.67	11.56	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6.48	6.99	0.255	0.275
Q	1.40	2.16	0.055	0.085
T	3.43	3.81	0.135	0.150

CASE 311-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
* Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 125°C	I_{DRM}	–	–	2.0	mA
*Peak On-State Voltage (Either Direction) I_{TM} = 42 A Peak, Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0 %	V_{TM}	–	1.5	2.0	Volts
Gate Trigger Current, Continuous dc (1) Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms	I_{GT}				mA
MT2 (+), G(+)		–	15	60	
MT2 (+), G(–)		–	20	70	
MT2 (–), G(–)		–	20	70	
MT2 (–), G(+)		–	30	100	
*MT2 (+), G(+); MT2 (–), G(–) T_C = -65°C		–	–	200	
*MT2 (+), G(–); MT2 (–), G(+) T_C = -65°C		–	–	250	
Gate Trigger Voltage, Continuous dc Main Terminal Voltage = 12 Vdc, R_L = 50 Ohms	V_{GT}				Volts
MT2 (+), G(+)		–	0.8	2.0	
MT2 (+), G(–)		–	0.7	2.1	
MT2 (–), G(–)		–	0.85	2.1	
MT2 (–), G(+)		–	1.1	2.5	
*All Quadrants, T_C = -65°C)		–	–	3.4	
*Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = +125°C		20	–	–	
Holding Current Main Terminal Voltage = 12 Vdc, Gate Open Initiating Current = 500 mA	I_H				mA
MT2 (+)		–	8	70	
MT2 (–)		–	10	80	
*Either Direction, T_C = -65°C		–	–	200	
*Turn-On Time Main Terminal Voltage = Rated V_{DRM}, I_{TM} = 42 A, Gate Source Voltage = 12 V, R_S = 50 Ohms, Rise Time = 0.1 μs, Pulse Width = 2.0 μs	t_{gt}	–	1.0	2.0	μs
Blocking Voltage Application Rate at Commutation, f = 60 Hz, T_C = 85°C On-State Conditions: I_{TM} = 42 A, Pulse Width = 4.0 ms, di/dt = 17.5 A/ms Off State Conditions: Main Terminal Voltage = Rated V_{DRM} (200 μs min), Gate Source Voltage = 0 V, R_S = 50 Ω	dv/dt(c)	–	5.0	–	V/μs

*Indicates JEDEC Registered Data.

(1) All voltage polarity reference to main terminal 1.

FIGURE 1 – RMS CURRENT DERATING

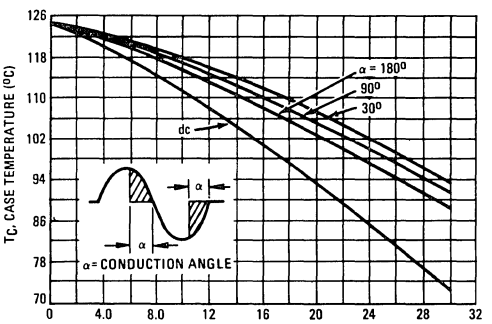


FIGURE 2 – POWER DISSIPATION

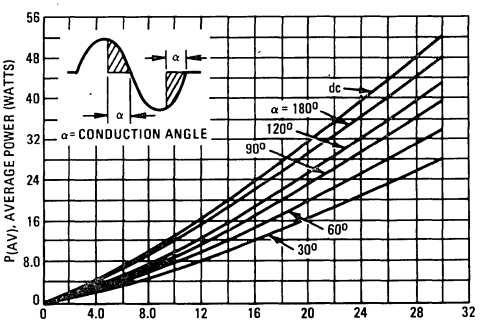


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FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

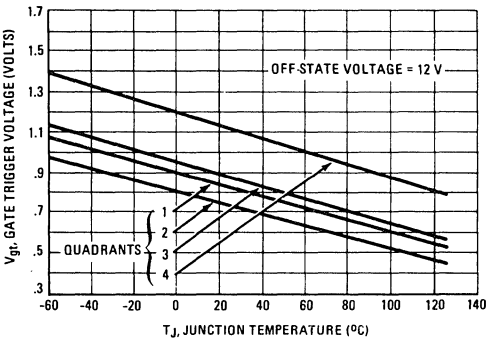

FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

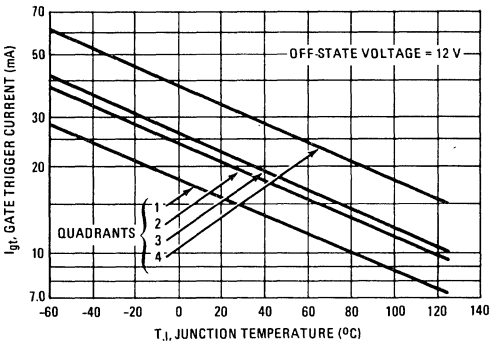

FIGURE 5 – MAXIMUM ON-STATE CHARACTERISTICS

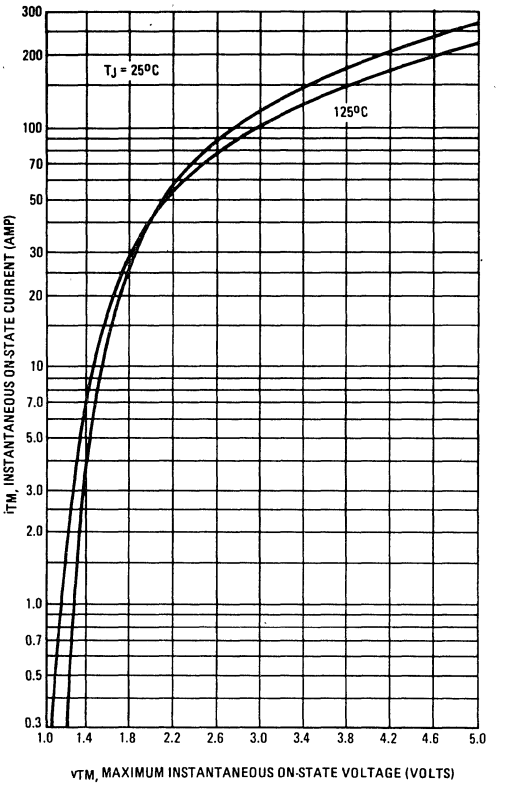

FIGURE 6 – TYPICAL HOLDING CURRENT

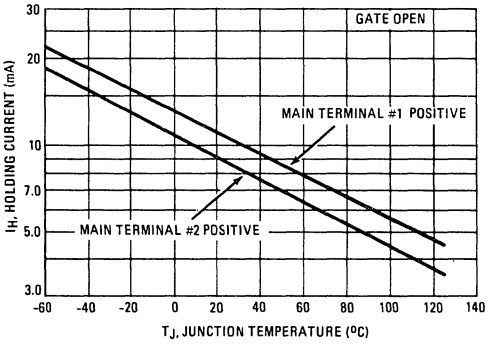

FIGURE 7 – MAXIMUM ALLOWABLE SURGE CURRENT

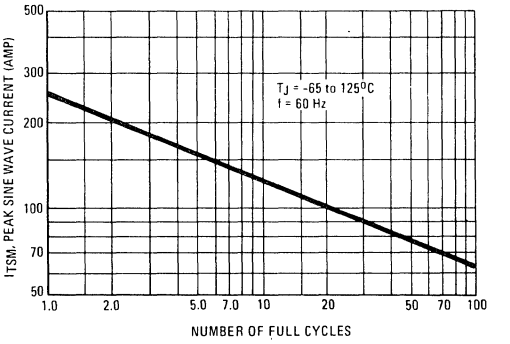

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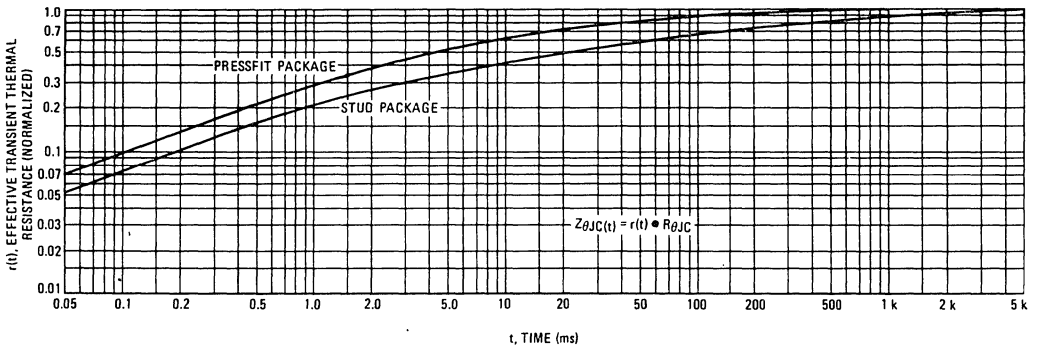
FIGURE 8 – TYPICAL THERMAL RESPONSE



2N6167 thru 2N6170

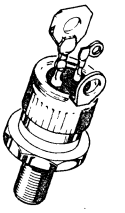
REVERSE-BLOCKING TRIODE THYRISTOR

. . . designed for industrial and consumer applications such as power supplies; battery chargers; temperature, motor, light and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current – I_{TSM} = 240 Amp
- Rugged Construction in Isolated Stud Package

SILICON CONTROLLED RECTIFIER

20 AMPERES RMS
100–600 VOLTS

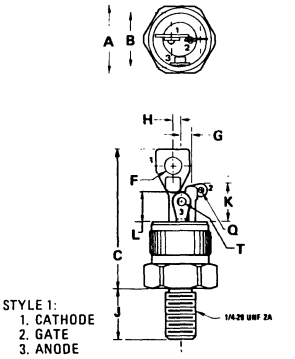


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Repetitive Forward and Reverse Blocking Voltage (1) (T_J = -40°C to +100°C)	V_{DRM} V_{RRM}		Volts
2N6167		100	
2N6168		200	
2N6169		400	
2N6170		600	
*Non-Repetitive Peak Reverse Blocking Voltage (t ≤ 5.0 ms)	V_{RSM}		Volts
2N6167		150	
2N6168		250	
2N6169		450	
2N6170		650	
*Average Forward Current (T_C = -40 to +65°C) (+85°C)	$I_{T(AV)}$	13 6.5	Amp
*Peak Surge Current (One cycle, 60 Hz) (T_C = +65°C) (1.5 ms pulse @ T_J = 100°C Preceded and followed by no current or Voltage	I_{TSM}	240 560	Amp
Circuit Fusing (T_J = -40 to +100°C) (t = 1.0 to 8.3 ms)	I^2t	235	A^2s
*Peak Gate Power	P_{GM}	5.0	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Forward Gate Current	I_{GFM}	2.0	Amp
*Operating Junction Temperature Range	T_J	-40 to +100	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C
*Stud Torque	–	30	in. lb.
***THERMAL CHARACTERISTICS**			
Characteristic	**Symbol**	**Max**	**Unit**
Thermal Resistance, Junction to Case	$R\theta_{JC}$	1.5	°C/W

*Indicates JEDEC Registered Data.

(1) Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.



STYLE 1:
1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	32.51	–	1.280
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.60	2.01	0.063	0.079
J	10.67	11.56	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6.48	6.99	0.255	0.275
Q	1.40	2.16	0.055	0.085
T	3.43	3.81	0.135	0.150

CASE 311-01

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Current (V_D = Rated V_{DRM}, gate open, T_J = 100°C)		I_{DRM}				mA
2N6167			–	1.0	2.0	
2N6168			–	1.0	2.5	
2N6169			–	1.0	3.0	
2N6170			–	1.0	4.0	
*Peak Reverse Blocking Current (V_R = Rated V_{RRM}, gate open, T_J = 100°C)		I_{RRM}				mA
2N6167			–	1.0	2.0	
2N6168			–	1.0	2.5	
2N6169			–	1.0	3.0	
2N6170			–	1.0	4.0	
*Peak Forward "On" Voltage (I_{TM} = 41 A Peak)		V_{TM}	–	1.5	1.7	Volts
Gate Trigger Current, Continuous dc (V_D = 12 V, R_L = 24 Ω)	*T_C = -40°C	I_{GT}	–	–	75	mA
	T_C = 25°C		–	2.1	40	
Gate Trigger Voltage, Continuous dc (V_D = 12 V, R_L = 24 Ω)		V_{GT}				Volts
	*T_C = -40°C		–	0.8	2.5	
	T_C = 25°C		–	0.63	1.6	
Holding Current (V_D = 12 V, gate open, I_T = 200 mA)	*T_C = -40°C	I_H	–	–	90	mA
	T_C = 25°C		–	3.5	50	
*Turn-On Time ($t_d + t_r$) (I_{TM} = 41 Adc, V_D = Rated V_{DRM}, I_{GT} = 200 mAdc, Rise Time ≤ 0.05 μs, Pulse Width = 10 μs)		t_{on}	–	–	1.0	μs
Turn-Off Time (I_{TM} = 10 A, I_R = 10 A)		t_{off}	–	25	–	μs
(I_{TM} = 10 A, I_R = 10 A, T_J = 100°C)			–	40	–	
Forward Voltage Application Rate (T_J = 100°C, V_D = Rated V_{DRM})		dv/dt	–	50	–	V/μs

*Indicates JEDEC Registered Data.

FIGURE 1 – AVERAGE CURRENT DERATING

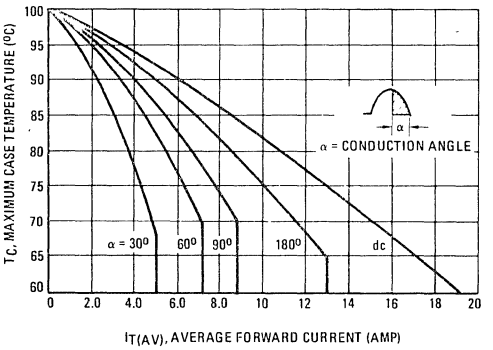


FIGURE 2 – POWER DISSIPATION

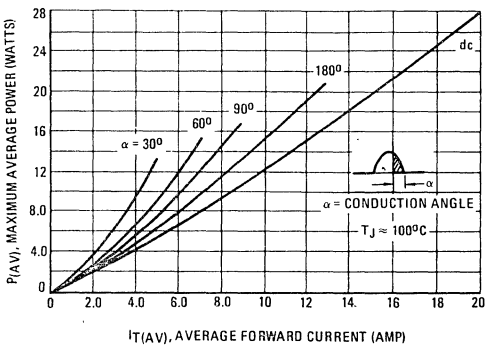


FIGURE 3 – MAXIMUM ON-STATE CHARACTERISTICS

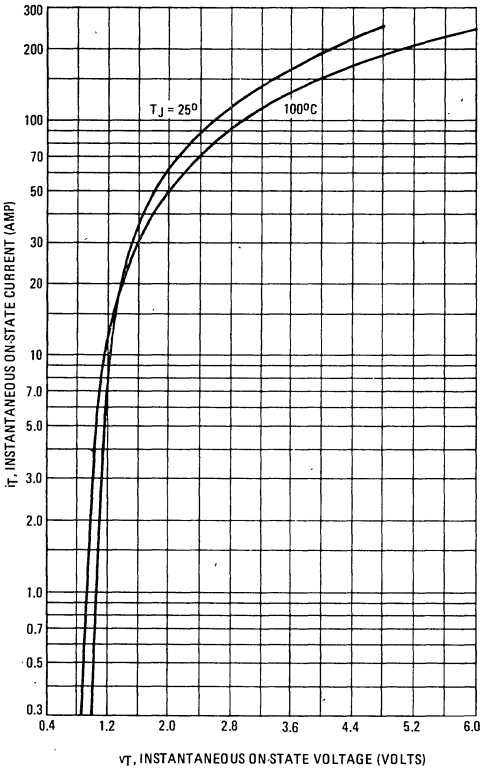


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

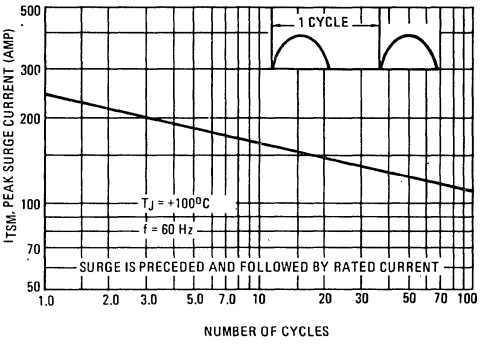


FIGURE 5 – CHARACTERISTICS AND SYMBOLS

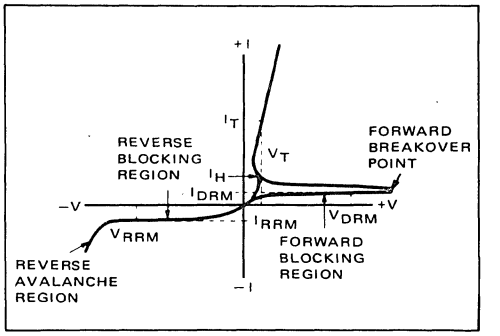


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FIGURE 6 – THERMAL RESPONSE

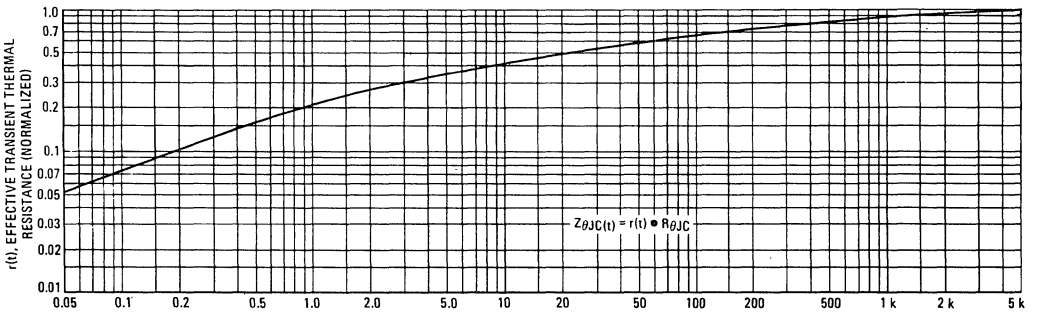


FIGURE 7 – TYPICAL GATE TRIGGER CURRENT

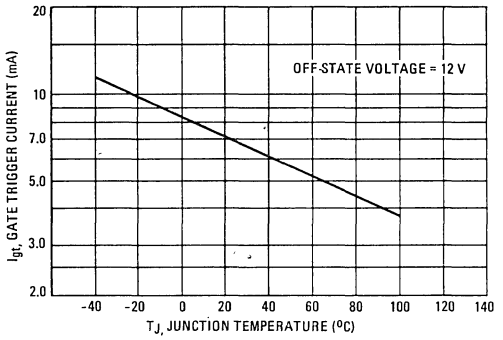


FIGURE 8 – TYPICAL GATE TRIGGER VOLTAGE

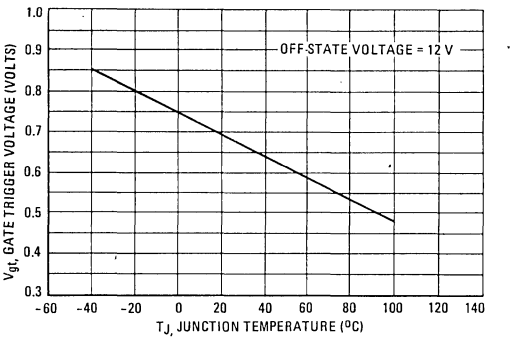
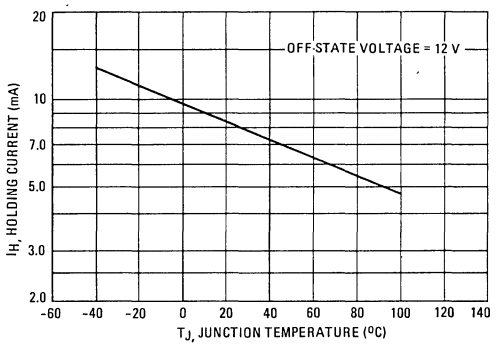


FIGURE 9 – TYPICAL HOLDING CURRENT



2N6236 thru 2N6241

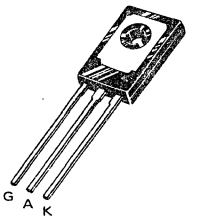
REVERSE BLOCKING TRIODE THYRISTORS

. . . PNPN devices designed for high volume consumer applications such as temperature, light, and speed control; process and remote control, and warning systems where reliability of operation is important.

- Passivated Surface for Reliability and Uniformity
- Power Rated at Economical Prices
- Practical Level Triggering and Holding Characteristics
- Flat, Rugged, Thermopad▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Recommended Electrical Replacement for C 106

SILICON CONTROLLED RECTIFIERS

4.0 AMPERES RMS
30 thru 600 VOLTS



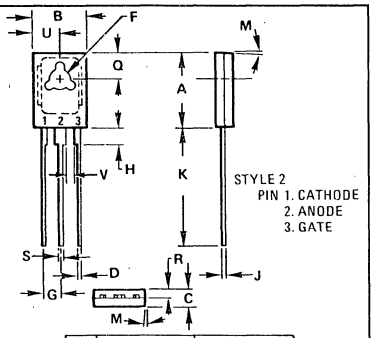
MAXIMUM RATINGS (T_C = 110°C unless otherwise noted.)

Rating		Symbol	Value	Unit
*Repetitive Peak Forward and Reverse Blocking Voltage (Note 1) (1/2 Sine Wave, (R_{GK} = 1000 ohms, T_C = -40 to +110°C)	2N6236	V_{DRM}, V_{RRM}	30	Volts
	2N6237		50	
	2N6238		100	
	2N6239		200	
	2N6240		400	
	2N6241		600	
*Non-Repetitive Peak Reverse Blocking Voltage (1/2 Sine Wave, R_{GK} = 1000 ohms, T_C = -40 to +110°C)	2N6236	V_{RSM}	50	Volts
	2N6237		100	
	2N6238		150	
	2N6239		250	
	2N6240		450	
	2N6241		650	
*Average On-State Current (T_C = -40 to +90°C) (T_C = +100°C)		$I_{T(AV)}$	2.6 1.6	Amp
*Surge On-State Current (1/2 Sine Wave, 60 Hz, T_C = +90°C) (1/2 Sine Wave, 1.5 ms, T_C = +90°C)		I_{TSM}	25 35	Amp
Circuit Fusing (T_C = -40 to 110°C, t = 1.0 to 8.3 ms)		i^2t	2.6	A^2s
*Peak Gate Power (Pulse Width = 10 μs, T_C = 90°C)		P_{GM}	0.5	Watts
*Average Gate Power (t = 8.3 ms, T_C = 90°C)		$P_{G(AV)}$	0.1	Watt
Peak Forward Gate Current		I_{GM}	0.2	Amp
Peak Reverse Gate Voltage		V_{RGM}	6.0	Volts
*Operating Junction Temperature Range		T_J	-40 to +110	°C
*Storage Temperature Range		T_{stg}	-40 to +150	°C
Mounting Torque (Note 2)		—	6.0	in.lb

THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	—	3.0	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	—	75	°C/W

*Indicates JEDEC Registered Data.
▲Trademark of Motorola Inc.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	—	0.040	—

CASE 77-04

ELECTRICAL CHARACTERISTICS (T_C = 25°C and R_{GK} = 1000 ohms unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Current (Note 1) (Rated V_{DRM}, T_C = 110°C)	I_{DRM}	–	–	200	μA
*Peak Reverse Blocking Current (Note 1) (Rated V_{RRM}, T_C = 110°C)	I_{RRM}	–	–	200	μA
*Peak Forward "On" Voltage (I_{TM} = 8.2 A Peak, Pulse Width = 1 to 2 ms, 2% Duty Cycle)	V_{TM}	–	–	2.2	Volts
Gate Trigger Current (Continuous dc) (Note 3) (V_{AK} = 12 Vdc, R_L = 24 Ohms) *(V_{AK} = 12 Vdc, R_L = 24 Ohms, T_C = -40°C)	I_{GT}	– –	– –	200 500	μA
Gate Trigger Voltage (Continuous dc) (Source Voltage = 12 V, R_S = 50 Ohms) *(V_{AK} = 12 Vdc, R_L = 24 Ohms, T_C = -40°C)	V_{GT}	–	–	1.0	Volts
Gate Non-Trigger Voltage (V_{AK} = Rated V_{DRM}, R_L = 100 Ohms, T_C = 110°C)	V_{GD}	0.2	–	–	Volts
Holding Current (V_{AK} = 12 Vdc, I_{GT} = 2.0 mA) T_C = 25°C *(Initiating On-State Current = 200 mA) T_C = -40°C	I_H	– –	– –	5.0 10	mA
*Total Turn-On Time (Source Voltage = 12 V, R_S = 6.0 k Ohms) (I_{TM} = 8.2 A, I_{GT} = 2.0 mA, Rated V_{DRM}) (Rise Time = 20 ns, Pulse Width = 10 μs)	t_{gt}	–	–	2.0	μs
Forward Voltage Application Rate (V_D = Rated V_{DRM}, T_C = 110°C)	dv/dt	–	10	–	V/μs

*Indicates JEDEC Registered Data

NOTES:

1. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. Torque rating applies with use of torque washer (Shakeproof WD19523 or equivalent). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common. (See AN-290 B)

   For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +225°C. For optimum results, an activated flux (oxide removing) is recommended.
3. Measurement does not include R_{GK} current.

CURRENT DERATING

FIGURE 1 – MAXIMUM CASE TEMPERATURE

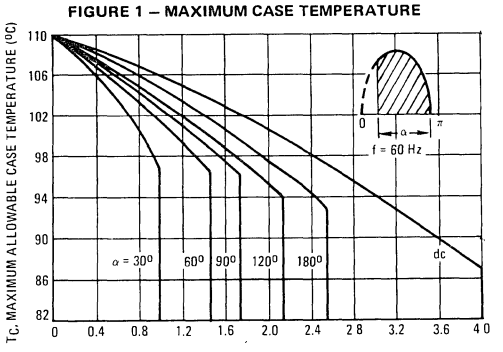
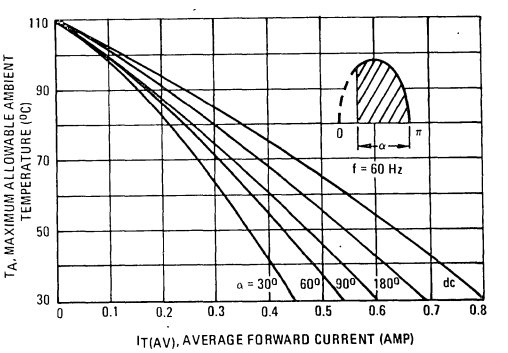
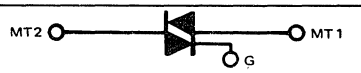


FIGURE 2 – MAXIMUM AMBIENT TEMPERATURE



2N6342 thru 2N6349
MAC 220 series
MAC 221 series



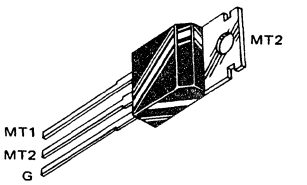
BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two Modes (2N6342, 2N6343, 2N6344, 2N6345, MAC220 Series) or Four Modes (2N6346, 2N6347, 2N6348,2N6349,MAC221 Series)
- For 400 Hz Operation, Consult Factory
- 12 Ampere Devices Available as 2N6342A thru 2N6349A

TRIACS

8 AMPERES RMS
50–800 VOLTS



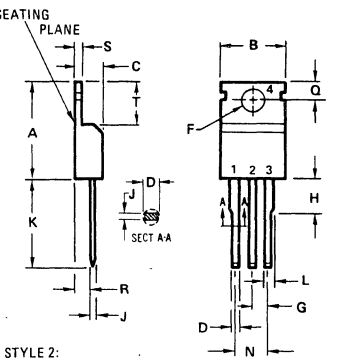
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (T_J = -40 to +100°C) ½ Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
MAC220-2,MAC221-2		50	
MAC220-3,MAC221-3		100	
2N6342,2N6346		200	
MAC220-5,MAC221-5		300	
2N6343,2N6347		400	
MAC220-7,MAC221-7		500	
2N6344,2N6348		600	
MAC220-9,MAC221-9		700	
2N6345,2N6349		800	
*RMS On-State Current (T_C = +80°C) Full Cycle Sine Wave 50 to 60 Hz (T_C = +90°C)	$I_{T(RMS)}$	8.0 4.0	Amp
*Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_J = +80°C) preceded and followed by 10 Rated Current	I_{TSM}	100	Amp
Circuit Fusing (T_J = -40 to +100°C, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
*Peak Gate Power (T_C = +80°C, Pulse Width = 2.0 μs)	P_{GM}	20	Watts
*Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Peak Gate Voltage	V_{GM}	10	Volts
*Operating Junction Temperature Range	T_J	-40 to +100	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
* Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W

*Indicates JEDEC Registered Data.
▲Trademark of Motorola Inc.



STYLE 2:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO-220 AB
All JEDEC dimensions and notes apply

7

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1 Voltage, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Off-State Current V_D = Rated V_{DRM} @ T_J = 100°C, Gate Open	I_{DRM}	–	–	2.0	mA
*Peak On-State Voltage I_{TM} = 11 A Peak; Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0 %	V_{TM}	–	1.3	1.55	Volts
Gate Trigger Current, Continuous dc V_D = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	I_{GT}				mA
MT2 (+), G(+) All Types		–	12	50	
MT2 (+), G(–) 2N6346 thru 49,MAC221		–	12	75	
MT2 (–), G(–) All Types		–	20	50	
MT2 (–), G(+) 2N6346 thru 49,MAC221		–	35	75	
*MT2 (+), G(+); MT2 (–), G(–) T_C = –40°C All Types		–	–	100	
*MT2 (+), G(–); MT2 (–), G(+) T_C = –40°C 2N6346 thru 49,MAC221		–	–	125	
Gate Trigger Voltage, Continuous dc V_D = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs	V_{GT}				Volts
MT2 (+), G(+) All Types		–	0.9	2.0	
MT2 (+), G(–) 2N6346 thru 49, MAC221		–	0.9	2.5	
MT2 (–), G(–) All Types		–	1.1	2.0	
MT2 (–), G(+) 2N6346 thru 49, MAC221		–	1.4	2.5	
*MT2 (+), G(+); MT2 (–), G(–) T_C = –40°C All Types		–	–	2.5	
*MT2 (+), G(–); MT2 (–), G(+) T_C = –40°C 2N6346 thru 49, MAC221		–	–	3.0	
V_D = Rated V_{DRM}, R_L = 10k Ohms, T_J = 100°C					
*MT2 (+), G(+); MT2 (–), G(–) All Types		0.2	–	–	
*MT2 (+), G(–); MT2 (–), G(–) 2N6346 thru 49, MAC221		0.2	–	–	
*Holding Current V_D = 12 Vdc, Gate Open; T_C = 25°C I_T = 200 mA; *T_C = –40°C	I_H	– –	6.0 –	40 75	mA
*Turn-On Time V_D = Rated V_{DRM}, I_{TM} = 11 A, I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2.0 μs	tgt	–	1.5	2.0	μs
Critical Rate of Rise of Commutation Voltage V_D = Rated V_{DRM}, I_{TM} = 11 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = 80°C	dv/dt(c)	–	5.0	–	V/μs

*Indicates JEDEC Registered Data

FIGURE 1 – RMS CURRENT DERATING

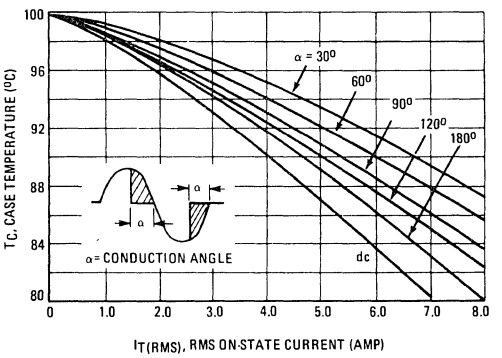


FIGURE 2 – ON-STATE POWER DISSIPATION

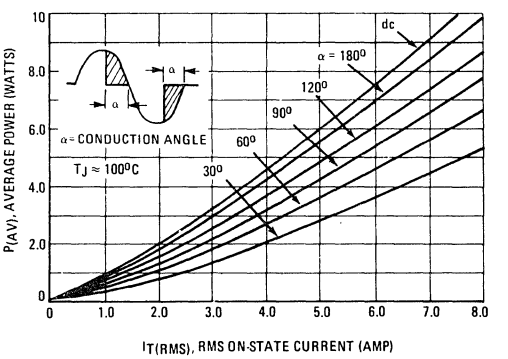


FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

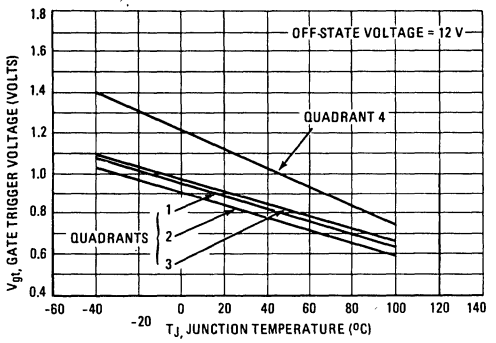


FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

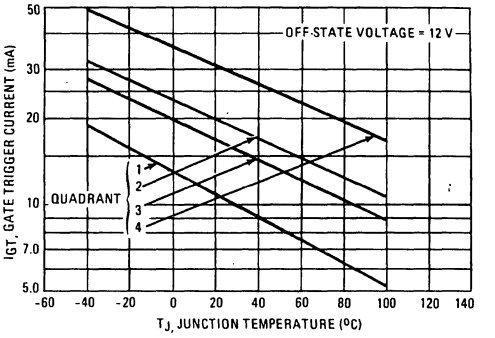


FIGURE 5 – ON-STATE CHARACTERISTICS

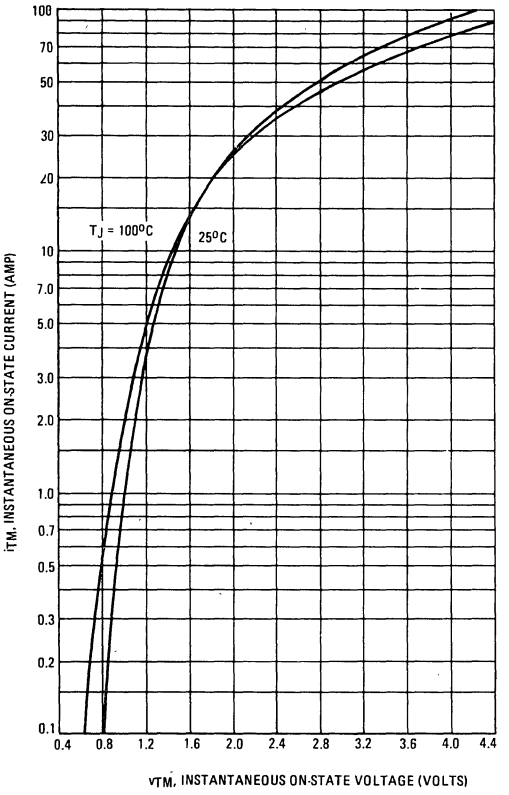


FIGURE 6 – TYPICAL HOLDING CURRENT

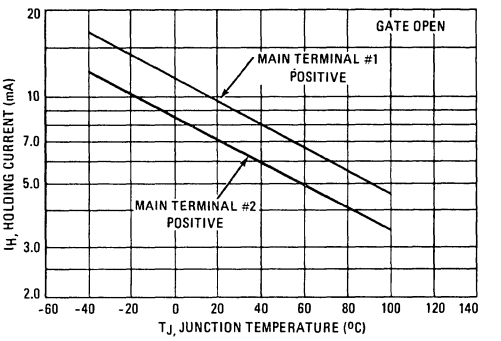


FIGURE 7 – MAXIMUM NON-REPETITIVE SURGE CURRENT

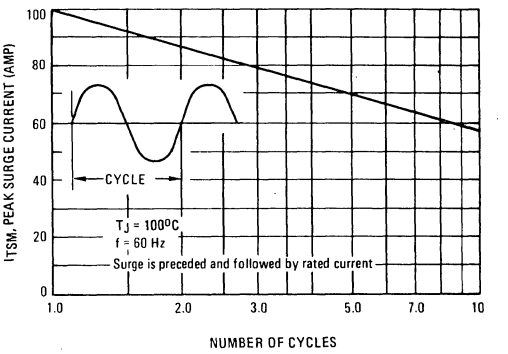
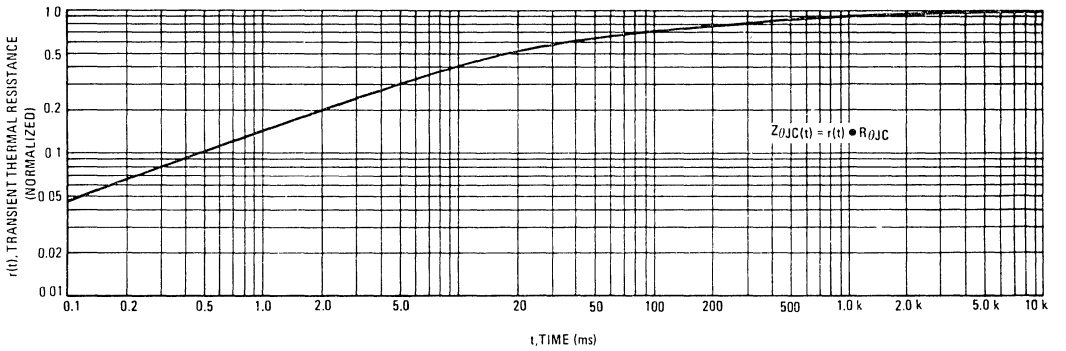
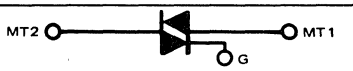


FIGURE 8 – TYPICAL THERMAL RESPONSE



2N6342A thru 2N6349A



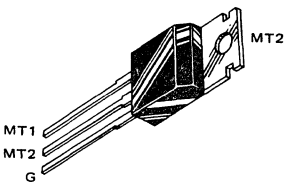
BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two Modes (2N6342A, 2N6343A, 2N6344A, 2N6345A) or Four Modes (2N6346A, 2N6347A, 2N6348A, 2N6349A)
- For 400 Hz Operation, Consult Factory
- 8 Ampere Devices Available as 2N6342 thru 2N6349

TRIACS

12 AMPERES RMS
200–800 VOLTS



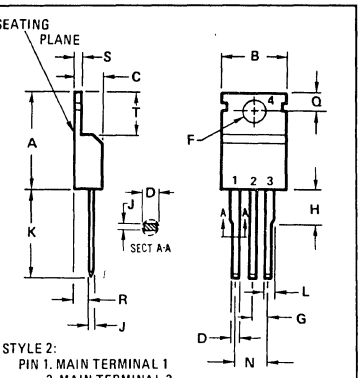
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage (T_J = -40 to +110°C) ½ Sine Wave 50 to 60 Hz, Gate Open 2N6342A, 2N6346A 2N6343A, 2N6347A 2N6344A, 2N6348A 2N6345A, 2N6349A	V_{DRM}	 200 400 600 800	Volts
*RMS On-State Current (Full cycle, Sine Wave, 50 to 60 Hz) T_C = +80°C T_C = +95°C	$I_{T(RMS)}$	 12 6.0	Amp
*Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_C = +80°C, Preceded and Followed by Rated Current)	I_{TSM}	120	Amps
Circuit Fusing (T_J = -40 to +110°C, t = 1.0 to 8.3 ms)	I^2t	59	A^2s
*Peak Gate Power (T_C = +80°C, Pulse Width = 2.0 μs	P_{GM}	20	Watts
*Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
*Peak Gate Current	I_{GM}	2.0	Amp
*Peak Gate Voltage	V_{GM}	±10	Volts
*Operating Junction Temperature Range	T_J	-40 to +110	°C
*Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTIC

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R\theta_{JC}$	2.0	°C/W

*Indicates JEDEC Registered Data.
▲Trademark of Motorola Inc.



STYLE 2:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO-220 AB
All JEDEC dimensions and notes apply

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ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Off-State Current V_D = Rated V_{DRM}, T_J = 110°C, Gate Open	I_{DRM}	–	–	2.0	mA
*Peak On-State Voltage (Either Direction) I_{TM} = 17 A Peak; Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0 %	V_{TM}	–	1.3	1.75	Volts
Gate Trigger Current, Continuous dc V_D = 12 Vdc, R_L = 100 ohms Minimum Gate Pulse Width = 2.0 μs	I_{GT}				mA
MT2 (+), G(+) All Types		–	6.0	50	
MT2 (+), G(–) 2N6346A thru 2N6349A		–	6.0	75	
MT2 (–), G(–) All Types		–	10	50	
MT2 (–), G(+) 2N6346A thru 2N6349A		–	25	75	
*MT2 (+), G(+); MT2 (–), G(–) T_C = –40°C All Types		–	–	100	
*MT2 (+), G(–); MT2 (–), G(+) T_C = –40°C 2N6346A thru 2N6349A		–	–	125	
*Peak Gate Trigger Voltage V_D = 12 Vdc, R_L = 100 ohms Minimum Gate Pulse Width = 2.0 μs	V_{GT}				Volts
MT2 (+), G(+) All Types		–	0.9	2.0	
MT2 (+), G(–) 2N6346A thru 2N6349A		–	0.9	2.5	
MT2 (–), G(–) All Types		–	1.1	2.0	
MT2 (–), G(+) 2N6346A thru 2N6349A		–	1.4	2.5	
*MT2 (+), G(+); MT2 (–), G(–) T_C = –40°C All Types		–	–	2.5	
*MT2 (+), G(–); MT2 (–), G(+) T_C = –40°C 2N6346A thru 2N6349A		–	–	3.0	
V_D = Rated V_{DRM}, R_L = 10k ohms, T_J = 100°C					
*MT2 (+), G(+); MT2 (–), G(–) All Types		0.2	–	–	
*MT2 (+), G(–); MT2 (–), G(+) 2N6346A thru 2N6349A		0.2	–	–	
Holding Current (Either Direction) V_D = 12 Vdc, Gate Open, T_C = 25°C I_T = 200 mA, *T_C = –40°C	I_H	– –	6.0 –	40 75	mA
*Turn-On Time V_D = Rated V_{DRM}, I_{TM} = 17A I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2.0 μs	tgt	–	1.5	2.0	μs
Critical Rate of Rise of Commutation Voltage V_D = Rated V_{DRM}, I_{TM} = 17A, Commutating di/dt = 6.5 A/ms, Gate Unenergized T_C = 80°C	dv/dt(c)	–	5.0	–	V/μs

*Indicates JEDEC Registered Data

FIGURE 1 – RMS CURRENT DERATING

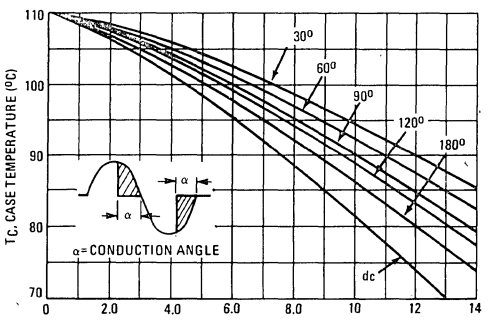

FIGURE 2 – ON-STATE POWER DISSIPATION

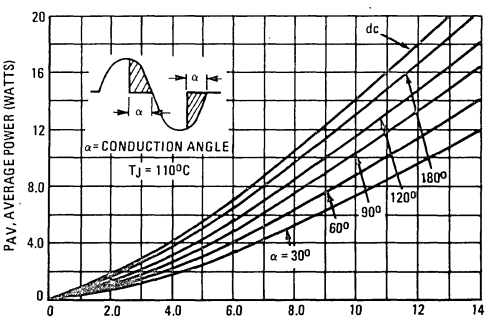

FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

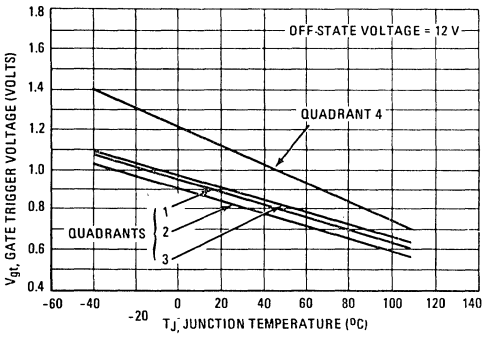

FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

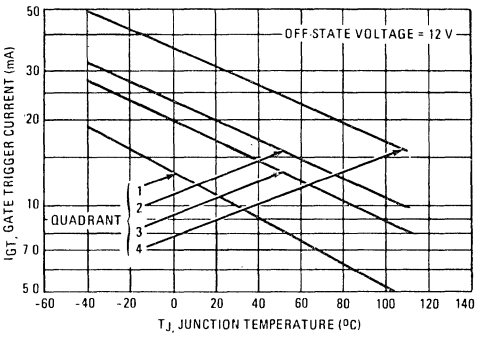

FIGURE 5 – ON-STATE CHARACTERISTICS

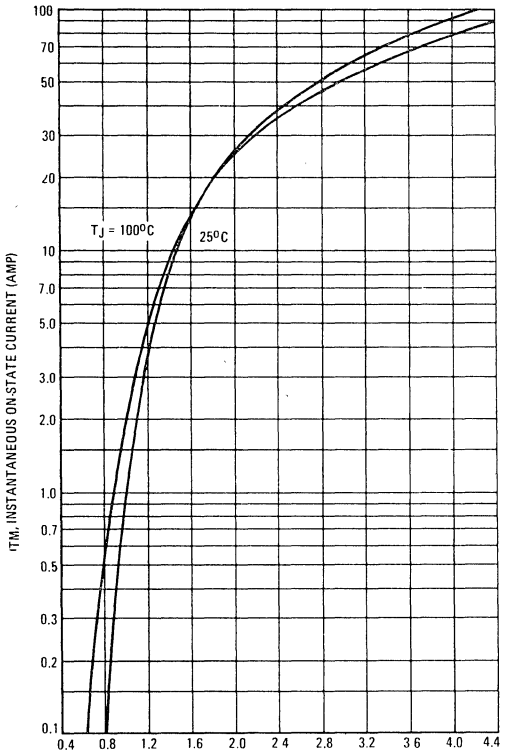

FIGURE 6 – TYPICAL HOLDING CURRENT

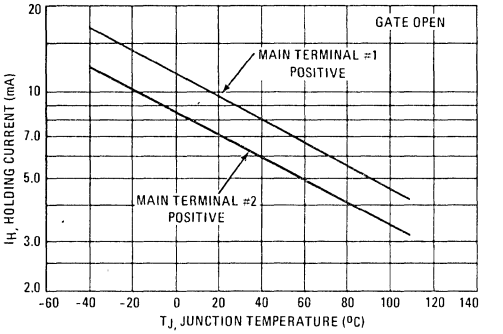

FIGURE 7 – MAXIMUM NON-REPETITIVE SURGE CURRENT

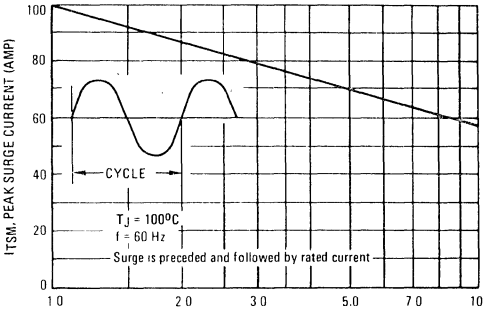

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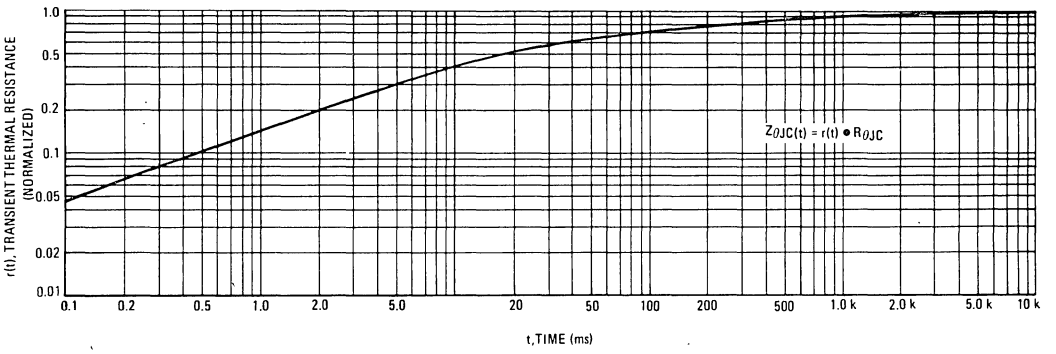
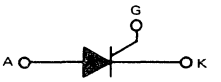
FIGURE 8 – TYPICAL THERMAL RESPONSE



2N6394 thru 2N6399 MCR220-5 MCR220-7 MCR220-9



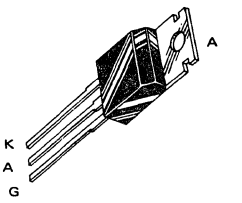
SILICON CONTROLLED RECTIFIERS

12 AMPERES RMS
50–800 VOLTS

REVERSE BLOCKING TRIODE THYRISTORS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies.

- Glass Passivated Junctions with Center Gate Geometry for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts



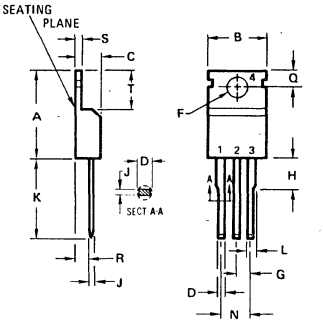
***MAXIMUM RATINGS**

Rating		Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage (T_J = -40 to 125°C)	2N6394	V_{RRM} V_{DRM}	50	Volts
	2N6395		100	
	2N6396		200	
	MCR220-5		300	
	2N6397		400	
	MCR220-7		500	
	2N6398		600	
	MCR220-9		700	
	2N6399		800	
RMS On-State Current (T_C = 90°C) (All Conduction Angles)		$I_{T(RMS)}$	12	Amps
Peak Non-Repetitive Surge Current (1/2 cycle, Sine Wave, 60 Hz, T_J = 125°C)		I_{TSM}	100	Amps
Circuit Fusing (T_J = -40 to +125°C, t = 1.0 to 8.3 ms)		I^2t	40	A^2s
Forward Peak Gate Power		P_{GM}	20	Watts
Forward Average Gate Power		$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current		I_{GM}	2.0	Amps
Operating Junction Temperature Range		T_J	-40 to +125	°C
Storage Temperature Range		T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

*Indicates JEDEC Registered Data.
▲Trademark of Motorola Inc.



STYLE 1:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

All JEDEC dimensions and notes apply

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	--	6.35	-	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO 220 AB

7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
* Peak Forward Blocking Current (V_D = Rated V_{DRM} @ T_J = 125°C)	I_{DRM}	–	–	2.0	mA
* Peak Reverse Blocking Current (V_R = Rated V_{RRM} @ T_J = 125°C)	I_{RRM}	–	–	2.0	mA
* Forward "On" Voltage (I_{TM} = 24 A Peak)	V_{TM}	–	1.7	2.2	Volts
* Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ohms)	I_{GT}	–	5.0	30	mA
* Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, R_L = 100 Ohms)	V_{GT}	–	0.7	1.5	Volts
(V_D = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)	V_{GD}	0.2	–	–	Volts
* Holding Current (V_D = 12 Vdc)	I_H	–	6.0	40	mA
Turn-On Time (I_{TM} = 12 A, I_{GT} = 40 mAdc, V_D = Rated V_{DRM}	t_{gt}	–	1.0	2.0	μs
Turn-Off Time (V_D = Rated V_{DRM}) (I_{TM} = 12 A, I_R = 12 A)	tq	–	15	–	μs
(I_{TM} = 12 A, I_R = 12 A, T_J = 125°C)		–	35	–	
Critical Rate-of-Rise of Off-State Voltage Exponential (V_D = Rated V_{DRM}, T_J = 125°C)	dv/dt	–	50	–	V/μs

*Indicates JEDEC Registered Data.

FIGURE 1 – CURRENT DERATING

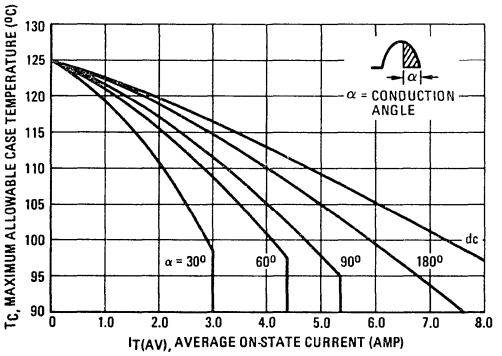


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

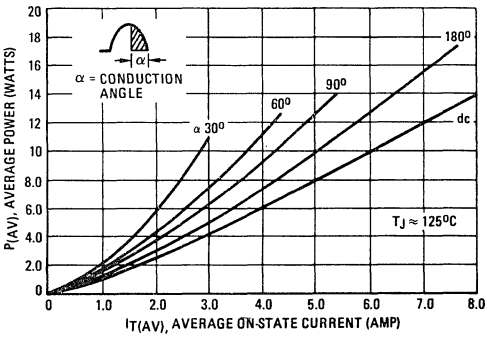


FIGURE 3 – ON-STATE CHARACTERISTICS

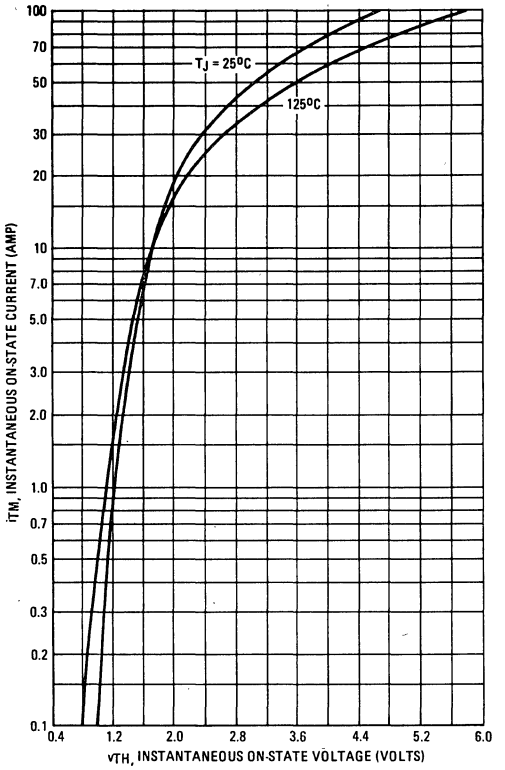


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

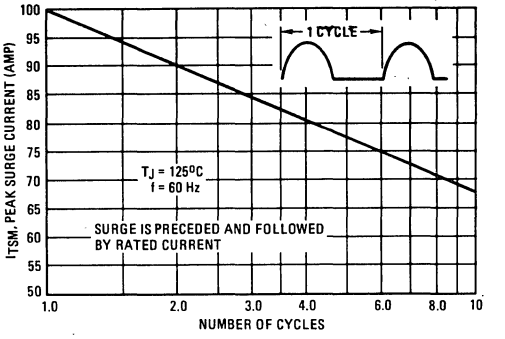
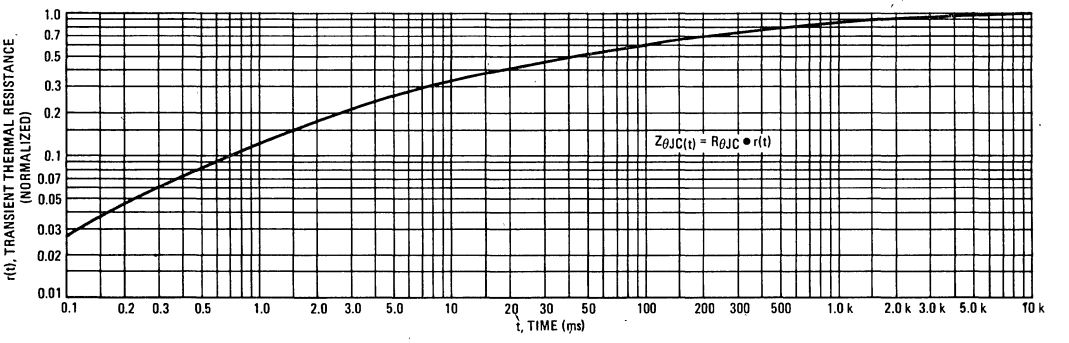


FIGURE 5 – THERMAL RESPONSE



TYPICAL CHARACTERISTICS

FIGURE 6 – PULSE TRIGGER CURRENT

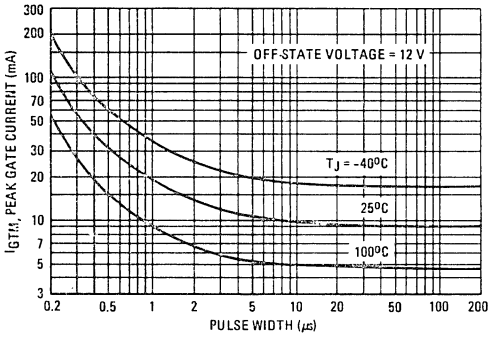


FIGURE 7 – GATE TRIGGER CURRENT

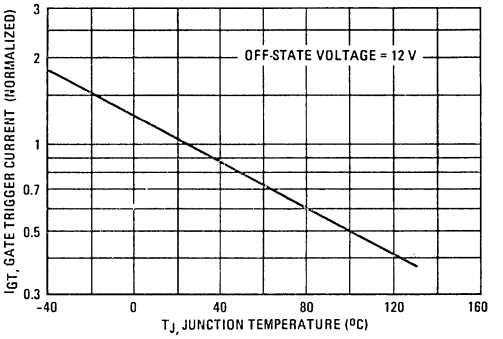


FIGURE 8 – GATE TRIGGER VOLTAGE

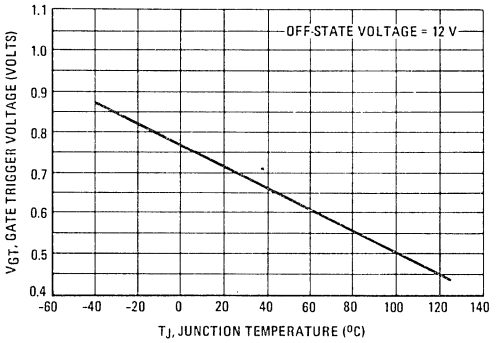
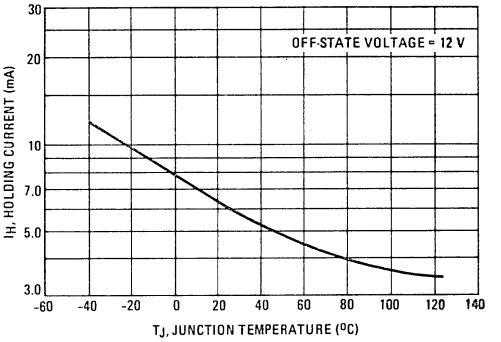
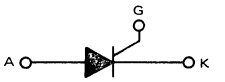


FIGURE 9 – HOLDING CURRENT



2N6400 MCR221-5 thru MCR221-7 2N6405 MCR221-9



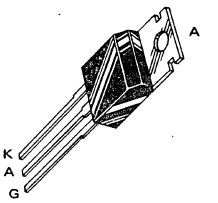
SILICON CONTROLLED RECTIFIER

16 AMPERES RMS
50–800 VOLTS

REVERSE BLOCKING TRIODE THYRISTORS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions with Center Gate Geometry for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts



***MAXIMUM RATINGS**

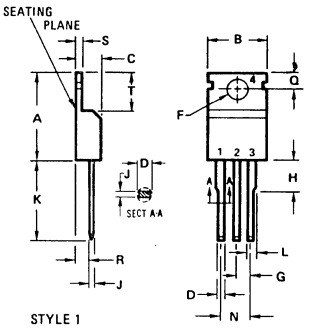
Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Voltage	V_{RRM}		Volts
2N6400	V_{DRM}	50	
2N6401		100	
2N6402		200	
MCR221-5		300	
2N6403		400	
MCR221-7		500	
2N6404		600	
MCR221-9		700	
2N6405		800	
RMS On-State Current, $T_C = 90^oC$	$I_{T(RMS)}$	16	Amps
Average On-State Current	$I_{T(AV)}$	10	Amps
Peak Non-Repetitive Forward Surge Current (1/2 cycle, Sine Wave, 60 Hz, $T_J = 125^oC$)	I_{TSM}	160	Amps
Circuit Fusing ($T_J = -40$ to $+125^oC$, t = 1.0 to 8.3 ms)	I^2t	100	A^2s
Forward Peak Gate Power	P_{GM}	20	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2.0	Amps
Operating Junction Temperature Range	T_J	-40 to +125	^oC
Storage Temperature Range	T_{stg}	-40 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	$^oC/W$

▲Trademark of Motorola Inc.

*Indicates JEDEC Registered Data.



STYLE 1
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

All JEDEC dimensions and notes apply

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO 220 AB

7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Current (V_D = Rated V_{DRM} @ T_J = 125°C)		I_{DRM}	–	–	2.0	mA
*Peak Reverse Blocking Current (V_R = Rated V_{RRM} @ T_J = 125°C)		I_{RRM}	–	–	2.0	mA
*Peak On-State Voltage (I_{TM} = 32 A Peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%)		V_{TM}	–	–	1.7	Volts
*Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 50 Ohms)		I_{GT}	–	5.0	30	mA
*Gate Trigger Voltage (Continuous dc)		V_{GT}				Volts
(V_D = 12 Vdc, R_L = 50 Ohms)	T_C = 25°C		–	0.7	1.5	
	T_C = -40°C		–	–	2.5	
(V_D = Rated V_{DRM}, R_L = 50 Ohms)	T_C = +125°C		0.2	–	–	
*Holding Current	T_C = 25°C	I_H	–	6.0	40	mA
(V_D = 12 Vdc)	*T_C = -40°C		–	–	60	
Turn-On Time (I_{TM} = 16 A, I_{GT} = 40 mAdc, V_D = Rated V_{DRM})		t_{gt}	–	1.0	–	μs
Turn-Off Time		t_q				μs
(I_{TM} = 16 A, I_R = 16 A, V_D = Rated V_{DRM})	T_C = 25°C		–	15	–	
	T_J = +125°C		–	35	–	
Critical Rate-of-Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform)	T_J = +125°C	dv/dt	–	50	–	V/μs

*Indicates JEDEC Registered Data.

FIGURE 1 – AVERAGE CURRENT DERATING

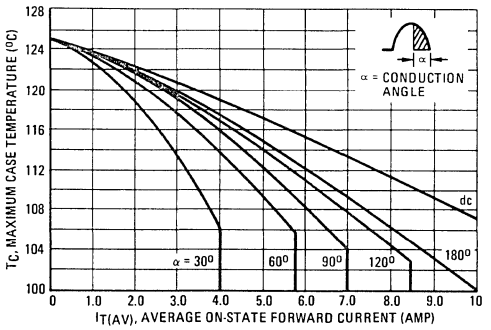


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

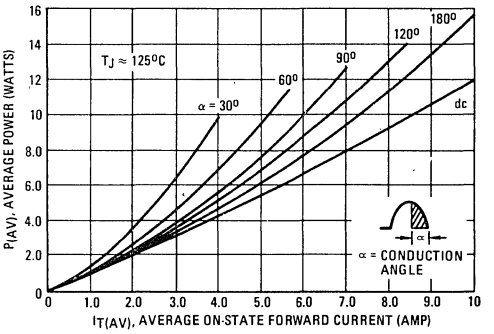


FIGURE 3 – ON-STATE CHARACTERISTICS

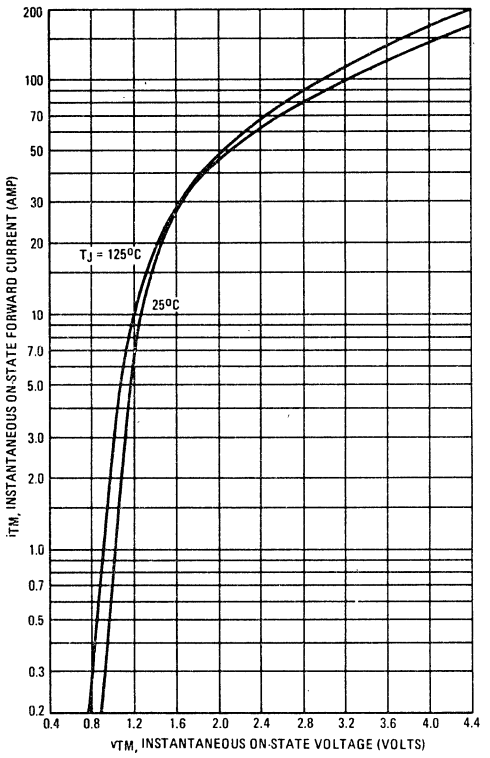


FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

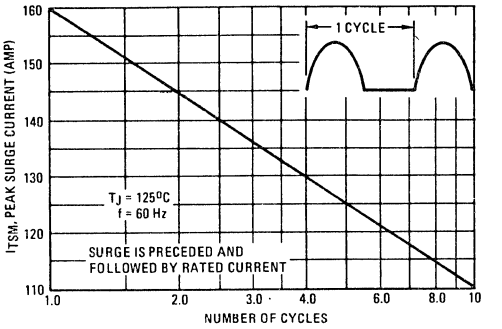


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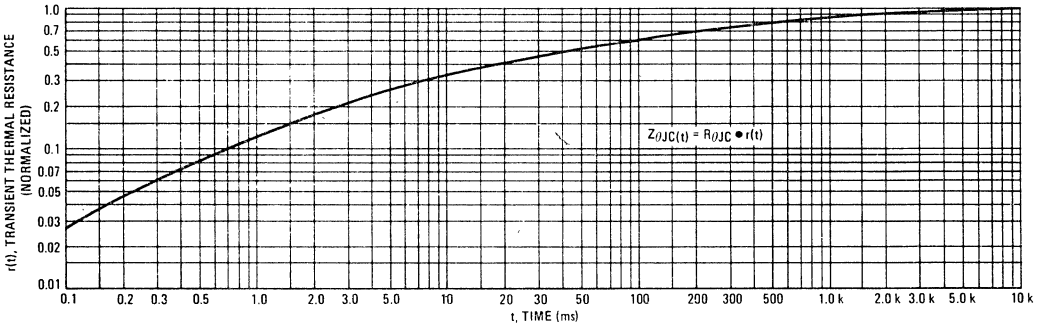
FIGURE 5 – THERMAL RESPONSE



TYPICAL TRIGGER CHARACTERISTICS

FIGURE 6 – PULSE TRIGGER CURRENT

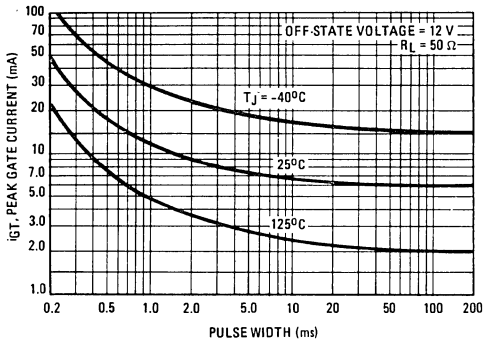


FIGURE 7 – GATE TRIGGER CURRENT

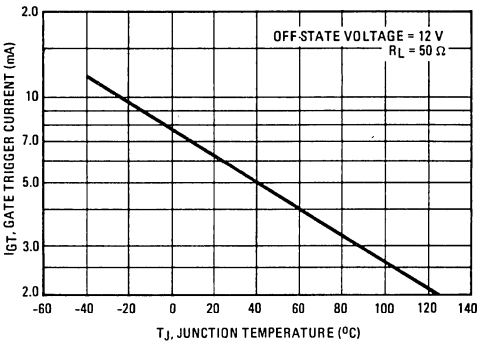


FIGURE 8 – GATE TRIGGER VOLTAGE

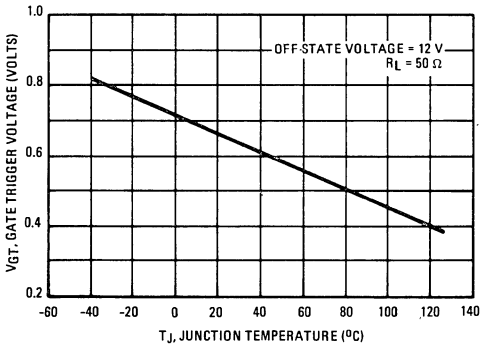
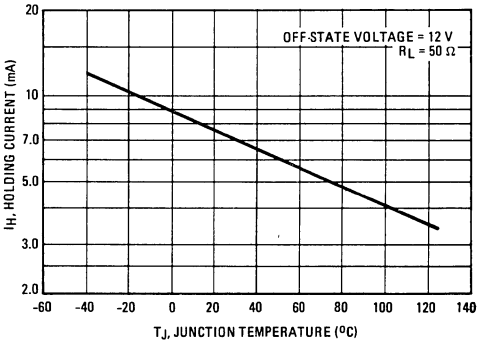


FIGURE 9 – HOLDING CURRENT



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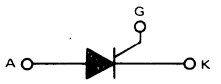
2N6504 thru 2N6509



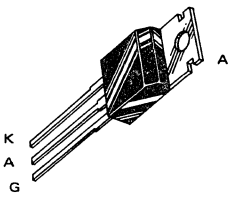
SILICON CONTROLLED RECTIFIER

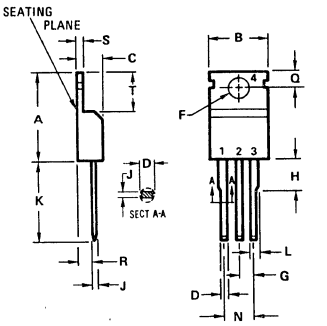
25 AMPERES RMS
50 – 800 VOLTS

REVERSE BLOCKING TRIODE THYRISTORS

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supply crowbar circuits.

- Glass Passivated Junctions with Center Gate Geometry for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Constructed for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 800 Volts
- 300 A Surge Current Capability





STYLE 1:
PIN 1. CATHODE
2. ANODE
3. GATE
4 ANODE

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO-220 AB
All JEDEC dimensions and notes apply

*MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Peak Repetitive Forward and Reverse Voltage (1)	2N6504	V_{RRM} V_{DRM}	50	Volts
	2N6505		100	
	2N6506		200	
	2N6507		400	
	2N6508		600	
	2N6509		800	
RMS On-State Current		$I_{T(RMS)}$	25	Amps
Average On-State Current (T_C = +85°C)		$I_{T(AV)}$	16	Amps
Peak Non-Repetitive Surge Current – 8.3 ms (1/2 Cycle, Sine Wave) 1.5 ms		I_{TSM}	300 350	Amps
Forward Peak Gate Power		P_{GM}	20	Watts
Forward Average Gate Power		$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current		I_{GM}	2	Amps
Operating Junction Temperature Range		T_J	-40 to +125	°C
Storage Temperature Range		T_{stg}	-40 to +150	°C

*THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

▲Trademark of Motorola Inc.
* Indicates JEDEC Registered Data.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward Blocking Current (V_D = Rated V_{DRM} @ T_J = 125°C)	I_{DRM}	–	–	2	mA
*Peak Reverse Blocking Current (V_R = Rated V_{RRM} @ T_J = 125°C)	I_{RRM}	–	–	2	mA
* Peak On-State Voltage (I_{TM} = 50 A, P.W. ≤ 300 μs, Duty Cycle ≤ 2%)	V_{TM}	–	–	1.8	Volts
*Gate Trigger Current (Continuous dc) T_C = 25°C (V_D = 12 Vdc, R_L = 100 Ohms) T_C = -40°C	I_{GT}	– –	– 25	40 75	mA
*Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc R_L = 100 Ohms, T_C = -40°C) (V_D = Rated V_{DRM}, R_L = 100 Ohms, T_J = 125°C)	V_{GT}	– 0.2	1 –	1.5 –	Volts
*Holding Current (V_D = 12 Vdc, T_C = 25°C)	I_H	–	35	40	mA
Turn-On Time (I_{TM} = 25 A, I_{GT} = 50 mAdc, V_D = Rated V_{DRM})	t_{gt}	–	1.5	2	μs
Turn-Off Time (V_D = Rated V_{DRM}) (I_{TM} = 25 A, I_R = 25 A) (I_{TM} = 25 A, I_R = 25 A, T_J = 125°C)	t_q	 – –	 15 35	 – –	μs
Critical Rate of Rise of Off-State Voltage (Gate Open, V_D = V_{DRM}, Exponential Waveform, T_J = 125°C)	dv/dt	–	50	–	V/μs

*Indicates JEDEC Registered Data.

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FIGURE 1 – AVERAGE CURRENT DERATING

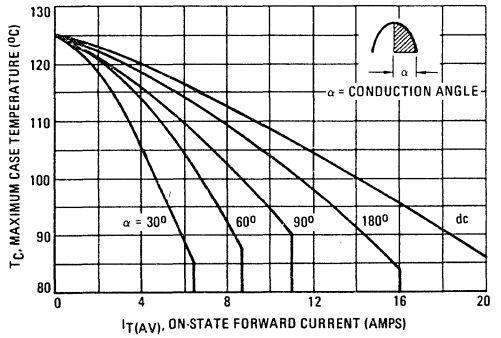

FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

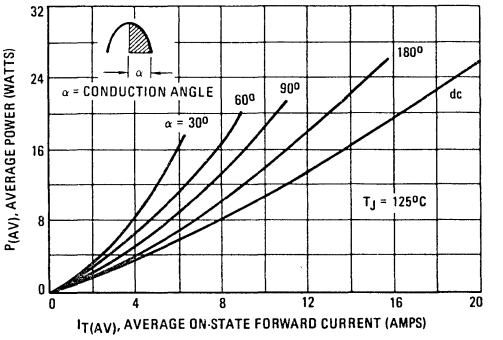

FIGURE 3 – ON-STATE CHARACTERISTICS

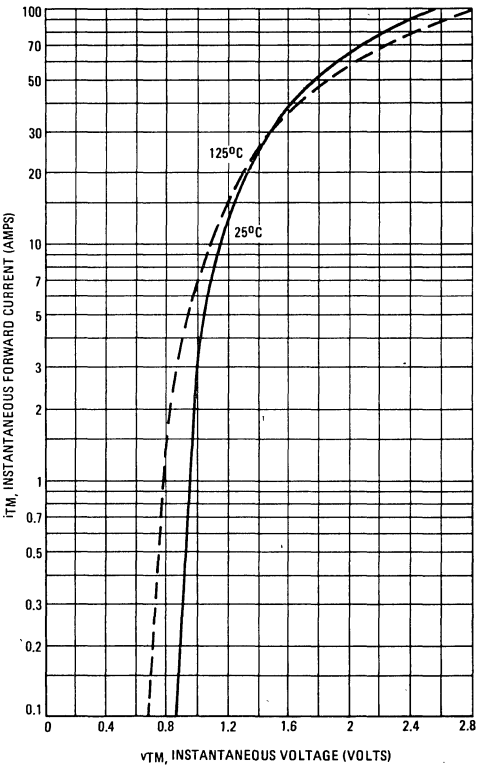

FIGURE 4 – MAXIMUM NON-REPETITIVE SURGE CURRENT

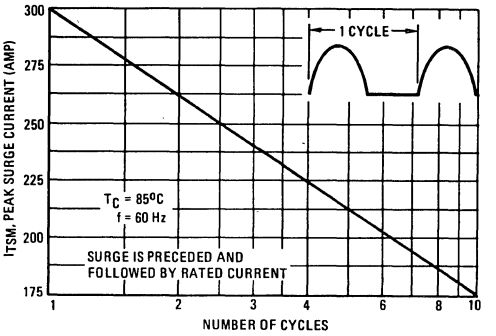

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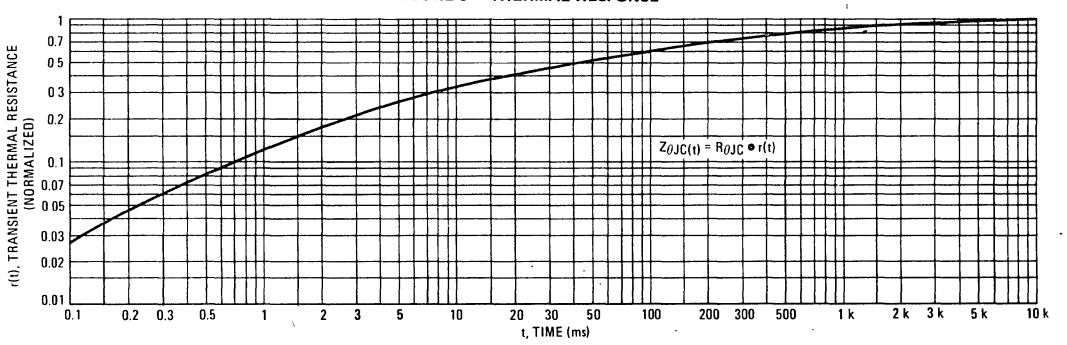
FIGURE 5 – THERMAL RESPONSE



TYPICAL TRIGGER CHARACTERISTICS

FIGURE 6 – PULSE TRIGGER CURRENT

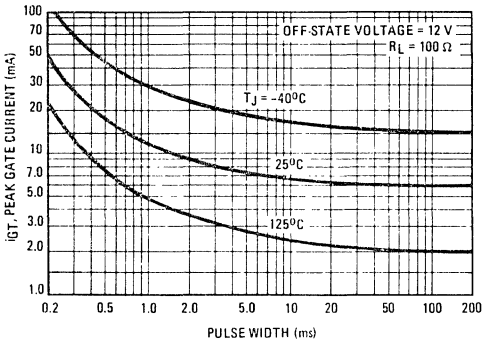


FIGURE 7 – GATE TRIGGER CURRENT

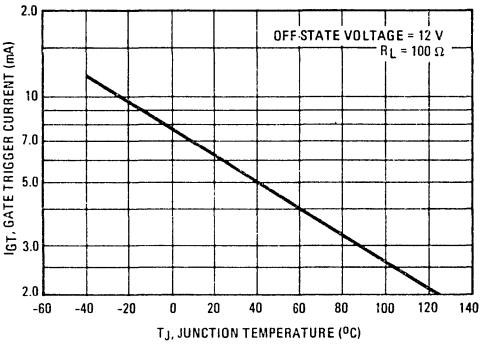


FIGURE 8 – GATE TRIGGER VOLTAGE

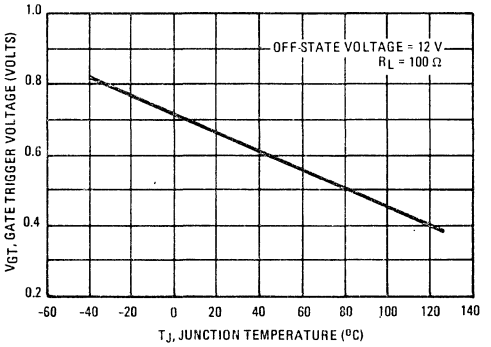
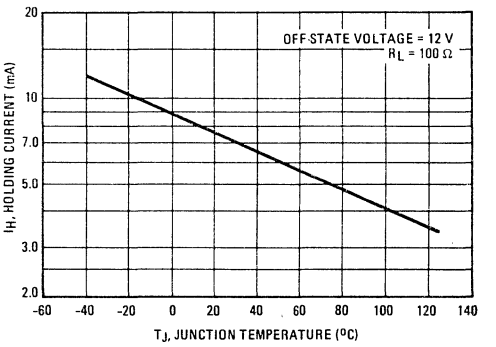


FIGURE 9 – HOLDING CURRENT



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C35 series

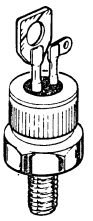
REVERSE BLOCKING TRIODE THYRISTOR

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire for Greater Parameter Uniformity and Stability
- Blocking Voltage to 800 Volts

SILICON CONTROLLED RECTIFIER

35 AMPERE RMS
25-800 VOLTS



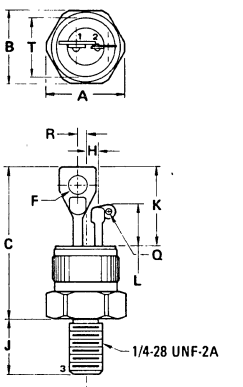
MAXIMUM RATINGS (T_J = 125°C unless otherwise noted.)

Rating		Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage (1) (T_C = -65 to +125°C)	C35U	V_{DRM} or V_{RRM}	25	Volts
	C35F		50	
	C35A		100	
	C35G		150	
	C35B		200	
	C35H		250	
	C35C		300	
	C35D		400	
	C35E		500	
	C35M		600	
	C35S		700	
	C35N		800	
Non-Repetitive Peak Reverse Voltage (T_C = -65 to +125°C, V < 5.0 ms)	C35U	V_{RSM}	35	Volts
	C35F		75	
	C35A		150	
	C35G		225	
	C35B		300	
	C35H		350	
	C35C		400	
	C35D		500	
	C35E		600	
	C35M		720	
	C35S		840	
	C35N		960	
RMS On-State Current (All Conduction Angles)		$I_{T(RMS)}$	35	Amp
Peak Non-Repetitive Surge Current (One cycle, 60 Hz)		I_{TSM}	225	Amp
Circuit Fusing (t = 1.0 to 8.3 ms)		I^2t	75	A^2s
Peak Gate Power		P_{GM}	5	Watts
Average Gate Power		$P_{G(AV)}$	0.5	Watt
Peak Reverse Gate Voltage		V_{GRM}	5	Volts
Operating Junction Temperature Range		T_J	-65 to +125	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

THERMAL CHARCTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.7	°C/W

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

STYLE 1:
PIN 1. CATHODE
2. GATE
3. ANODE

CASE 263-03
Similar to TO-48

7

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Reverse or Forward Blocking Current (V_D = Rated V_{DRM}, T_C = +125°C) (V_R = Rated V_{RRM}, T_C = 125°C)		I_{DRM} or I_{RRM}				mA
	C35U,F,A,G		–	–	13	
	C35B		–	–	12	
	C35H		–	–	11	
	C35C		–	–	10	
	C35D		–	–	8	
	C35E		–	–	6	
	C35M		–	–	5	
	C35S		–	–	4.5	
	C35N		–	–	4	
Average Forward or Reverse Blocking Current (V_D = Rated V_{DRM}, T_C = +125°C) (V_R = Rated V_{RRM}, T_C = 125°C)		I_{DRM} (AV) or I_{RRM} (AV)				mA
	C35U,F,A,G		–	–	6.5	
	C35B		–	–	6	
	C35H		–	–	5.5	
	C35C		–	–	5	
	C35D		–	–	4	
	C35E		–	–	3	
	C35M		–	–	2.5	
	C35S		–	–	2.25	
	C35N		–	–	2	
Peak On-State Voltage (I_{TM} = 50.3 A peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2.0%)		V_{TM}	–	–	2	Volts
Gate Trigger Current, Continuous dc (V_D = 12 Vdc, R_L = 50 Ω)		I_{GT}	–	6	40	mA
(V_D = 12 Vdc, R_L = 50 Ω, T_C = –65°C)			–	–	80	
Gate Trigger Voltage, Continuous dc (V_D = 12 Vdc, R_L = 50 Ω, T_C = –65°C to +125°C)		V_{GT}	–	–	3	Volts
(V_D = Rated V_{DRM}, R_L = 1000 Ω, T_C = 125°C)			.25			
Holding Current (V_D = 24 Vdc, Gate Supply = 10 V, 20 Ω, 45 μs minimum pulse width, I_T = 0.5A)		I_H	–	–	100	mA
Critical Rate of Rise of Forward Blocking Voltage V_D = Rated V_{DRM}, T_C = +125°C)	C35U,F,M,S,N	dv/dt	10	–	–	V/μs
	C35A,G,B,H		20	–	–	
	C35C,D,E		25	–	–	

FIGURE 1 – CURRENT DERATING (HALF-WAVE RECTIFIED SINE WAVE)

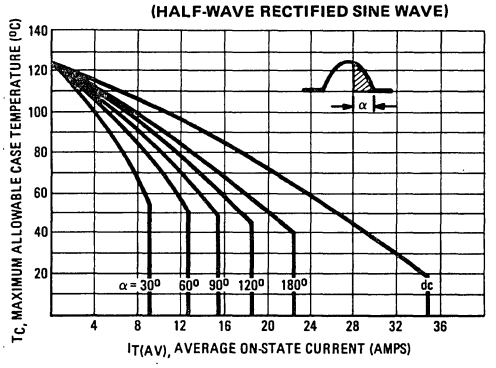
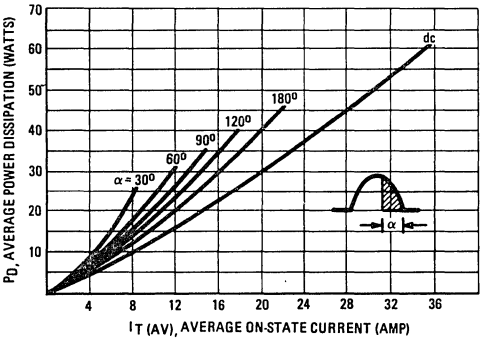


FIGURE 2 – POWER DISSIPATION (HALF-WAVE SINE WAVE)



C106 series

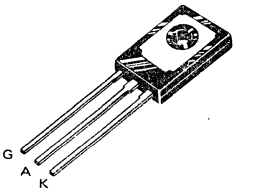
REVERSE BLOCKING TRIODE THYRISTORS

. . . Glassivated PNPN devices designed for high volume consumer applications such as temperature, light, and speed control; process and remote control, and warning systems where reliability of operation is important.

- Glassivated Surface for Reliability and Uniformity
- Power Rated at Economical Prices
- Practical Level Triggering and Holding Characteristics
- Flat, Rugged, Thermopad▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability

SILICON CONTROLLED RECTIFIER

4 AMPERES RMS
15 thru 600 VOLTS



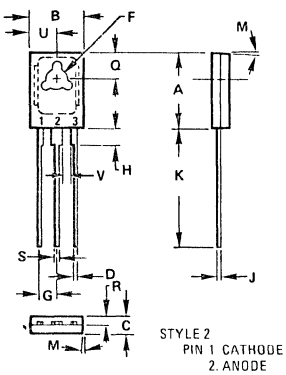
MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage R_{GK} = 1 kΩ T_C = -40° to 110°C	C106Q	V_{DRM} OR V_{RRM}	15	Volts
	C106Y		30	
	C106F		50	
	C106A		100	
	C106B		200	
	C106C		300	
	C106D		400	
	C106E		500	
	C106M		600	
RMS Forward Current (All Conduction Angles)		$I_{T(RMS)}$	4	Amp
Average Forward Current T_A = 30°C		$I_{T(AV)}$	2.55	Amp
Peak Non-Repetitive Surge Current (1/2 Cycle, 60 Hz, T_J = -40 to +110°C)		I_{TSM}	20	Amp
Circuit Fusing t > 1.5 ms		I^2t	0.5	A^2s
Peak Gate Power		P_{GM}	0.5	Watt
Average Gate Power		$P_{G(AV)}$	0.1	Watt
Peak Forward Gate Current		I_{GFM}	0.2	Amp
Peak Reverse Gate Voltage		V_{GRM}	6	Volts
Operating Junction Temperature Range		T_J	-40 to +110	°C
Storage Temperature Range		T_{stg}	-40 to +150	°C
Mounting Torque (Note 1)		–	6	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W

NOTE 1. Torque rating applies with use of torque washer (Shakeproof WD 19523 or equivalent). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common. (See AN-290 B)
For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +225°C. For optimum results, an activated flux (oxide removing) is recommended.



STYLE 2
PIN 1. CATHODE
2. ANODE
3. GATE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

▲Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current		I_{DRM}				μA
(Rated V_{DRM}, R_{GK} = 1000 Ohms, T_J = 25°C)			–	–	10	
(Rated V_{DRM}, R_{GK} = 1000 Ohms, T_J = 110°C)			–	–	100	
Peak Reverse Blocking Current		I_{RRM}				μA
(Rated V_{RRM}, R_{GK} = 1000 Ohms, T_J = 25°C)			–	–	10	
(Rated V_{RRM}, R_{GK} = 1000 Ohms, T_J = 110°C)			–	–	100	
Forward "On" Voltage (I_{FM} =4 A Peak)		V_{TM}	–	–	2.2	Volts
Gate Trigger Current (Continuous dc)		I_{GT}				μA
(V_{AK} = 6 Vdc, R_L = 100 Ohms)			–	30	200	
(V_{AK} = 6 Vdc, R_L = 100 Ohms, T_C = -40°C)			–	75	500	
Gate Trigger Voltage (Continuous dc)	T_J = 25°C	V_{GT}	0.4	–	0.8	Volts
(V_{AK} = 6 Vdc, R_L = 100 Ohms, R_{GK} = 1000 Ohms)	T_J = -40°C		0.5	–	1	
(V_{AK} = Rated V_{DRM}, R_L = 3000 Ohms, R_{GK} = 1000 Ohms, T_J = 110°C)			0.2	–	–	
Holding Current	T_J = 25°C	I_{HX}	0.3	–	3	mA
(V_D = 12 Vdc, R_{GK} = 1000 Ohms)	T_J = -40°C		0.4	–	6	
	T_J = +110°C		0.14	–	2	
Forward Voltage Application Rate (T_J = 110°C, R_{GK} = 1000 Ohms, V_D = Rated V_{DRM})		dv/dt	–	8	–	V/μs
Turn-On Time		t_{gt}	–	1.2	–	μs
Turn-Off Time		t_q	–	40	–	μs

FIGURE 1 – AVERAGE CURRENT DERATING

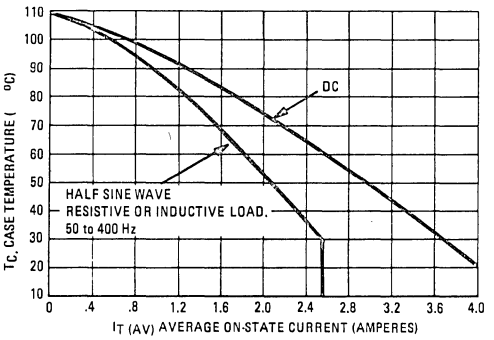
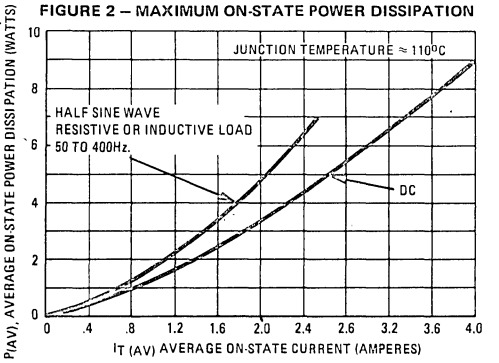
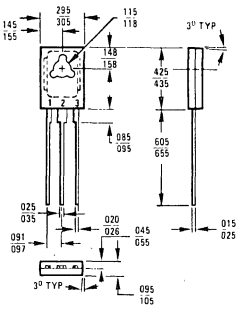


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION

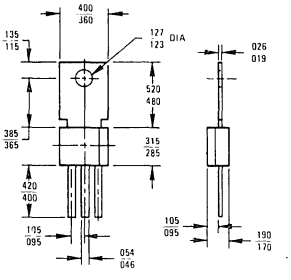


Package Interchangeability

The dimensional diagrams below compare the critical dimensions of the Motorola C-106 package with competitive devices. It has been demonstrated that the smaller dimensions of the Motorola package make it compatible in most lead-mount and chassis-mount applications. The user is advised to compare all critical dimensions for mounting compatibility.



Motorola C-106 Package



Competitive C-106 Package

C122 series

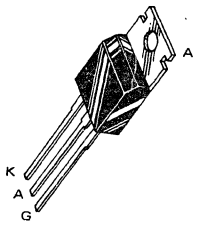
REVERSE BLOCKING TRIODE THYRISTOR

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 600 Volts
- Different Lead Form Configurations, Suffix (2) thru (6) available, see Thyristor Selection Guide for Information

SILICON CONTROLLED RECTIFIER

8 AMPERES RMS
50–600 VOLTS



MAXIMUM RATINGS

Rating (Note 2)	Symbol	Value	Unit
Repetitive Peak Off-State Voltage Repetitive Peak Reverse Voltage	V_{DRM} V_{RRM}		Volts
C122F		50	
C122A		100	
C122B		200	
C122C		300	
C122D		400	
C122E		500	
C122M		600	
Non-Repetitive Peak Reverse Voltage	V_{RSM}		Volts
C122F		75	
C122A		200	
C122B		300	
C122C		400	
C122D		500	
C122E		600	
C122M		700	
Forward Current RMS (All Conduction Angles) $T_C \leq 75^oC$	$I_{T(RMS)}$	8	Amps
Peak Forward Surge Current (1/2 Cycle, Sine Wave, 60 Hz,)	I_{TSM}	90	Amps
Circuit Fusing Considerations t = 8.3 ms	I^2t	34	A^2s
Forward Peak Gate Power (t = 10 μs)	P_{GM}	5	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current	I_{GM}	2	Amps
Operating Junction Temperature Range	T_J	-40 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +125	°C

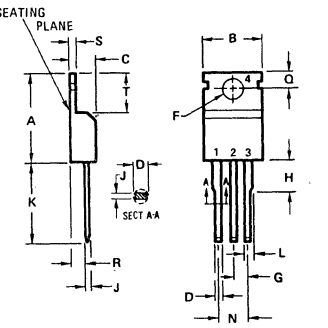
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.8	°C/W

(1) V_{DRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltage.

(2) Add lead form suffix designator "( )" to part number for lead configurations 2 thru 6. See Thyristor Selection Guide for information.

▲ Trademark of Motorola Inc.



PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO-220 AB

All JEDEC dimensions and notes apply

NOTE: SUFFIX (1) Lead Configuration Available as standard.

7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (V_D = Rated V_{DRM})	T_C = 25°C	I_{DRM}	–	–	0.1	mA
	T_C = 100°C		–	–	0.5	
Peak Reverse Blocking Current (V_R = Rated V_{RRM})	T_C = 25°C	I_{RRM}	–	–	0.1	mA
	T_C = 100°C		–	–	0.5	
Peak On-State Voltage (1) (I_{TM} = 16 A Peak, T_C = 25°C)		V_{TM}	–	–	1.83	Volts
Gate Trigger Current (Continuous dc)		I_{GT}				mA
(V_D = 6 V, R_L = 91 Ohms, T_C = 25°C)			–	–	25	
(V_D = 6 V, R_L = 45 Ohms, T_C = -40°C)			–	–	40	
Gate Trigger Voltage (Continuous dc)		V_{GT}				Volts
(V_D = 6 V, R_L = 91 Ohms, T_C = 25°C)			–	–	1.5	
(V_D = 6 V, R_L = 45 Ohms, T_C = -40°C)			–	–	2	
(V_D = Rated V_{DRM}, R_L = 1000 Ohms, T_C = 100°C)			0.2	–	–	
Holding Current (V_D = 24 Vdc, I_T = 0.5 A, 0.1 to 10 ms Pulse, Gate Trigger Source = 7 V, 20 Ohms)		I_H				mA
	T_C = 25°C		–	–	30	
	T_C = -40°C		–	–	60	
Turn-Off Time (V_D = Rated V_{DRM}) (I_{TM} = 8 A, I_R = 8A)		tq	–	50	–	μs
Critical Rate-of-Rise of Off-State Voltage (V_D = Rated V_{DRM}, Linear, T_C = 100°C)		dv/dt	–	50	–	V/μs

(1) Pulse Test: Pulse Width = 1 ms, Duty Cycle ≤ 2%.

FIGURE 1 – CURRENT DERATING (HALF-WAVE)

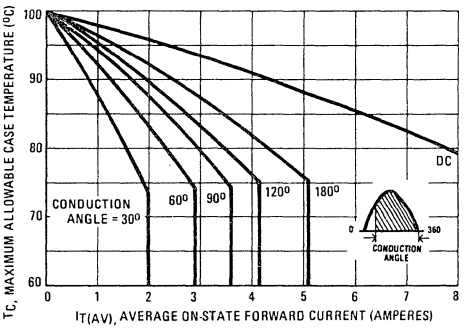


FIGURE 2 – CURRENT DERATING (FULL-WAVE)

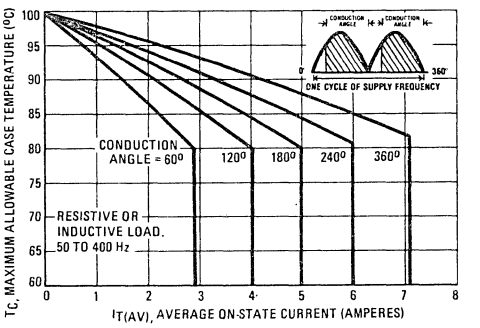


FIGURE 3 – MAXIMUM POWER DISSIPATION (HALF-WAVE)

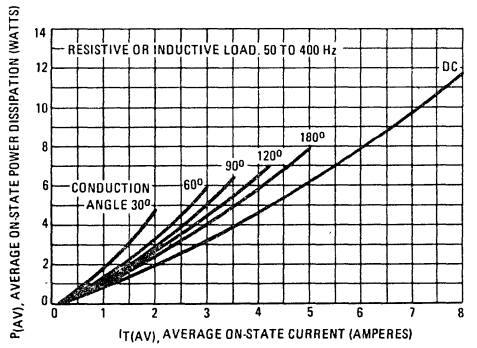
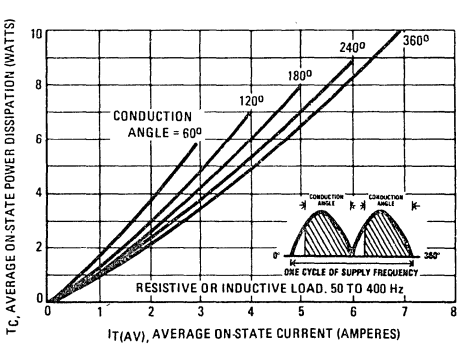


FIGURE 4 – MAXIMUM POWER DISSIPATION (FULL-WAVE)



C228
C228( )3
C229
series

REVERSE BLOCKING TRIODE THYRISTOR

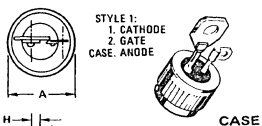
. . . designed for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current – I_{TSM} = 300 Amp
- Low Forward "On" Voltage – 1.2 V (Typ) @ I_{TM} = 35 Amp
- Practical Level Triggering and Holding Characteristics – 10 mA (Typ) @ T_C = 25°C
- Rugged Construction in Either Pressfit, Stud, or Isolated Stud Packages
- Glass Passivated Junctions for Maximum Reliability

SILICON CONTROLLED RECTIFIER

35 AMPERES RMS
50 thru 600 VOLTS

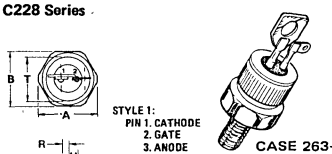
C229 Series



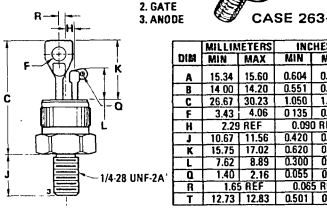
CASE 310-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.52	1.78	0.060	0.070
J	7.62	8.89	0.300	0.350
K	–	26.67	–	1.050
L	–	17.02	–	0.670
Q	1.40	2.16	0.055	0.085

C228 Series

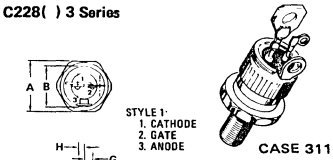


CASE 263-03

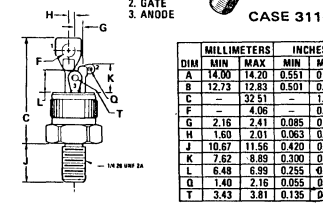


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

C228( ) 3 Series



CASE 311-01



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	32.51	–	1.280
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.60	2.01	0.063	0.079
J	10.67	11.56	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6.48	6.99	0.255	0.275
Q	1.40	2.16	0.055	0.085
T	3.43	3.81	0.135	0.150

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (1) (T_J = -40 to +125°C)	V_{DRM} and V_{RRM}		Volts
C229F, C228F, C228F3		50	
C229A, C228A, C228A3		100	
C229B, C228B, C228B3		200	
C229C, C228C, C228C3		300	
C229D, C228D, C228D3		400	
C229E, C228E, C228E3		500	
C229M, C228M, C228M3		600	
Non-Repetitive Reverse Voltage (T_J = -40 to +125°C)	V_{RSM}		Volts
C229F, C228F, C228F3		75	
C229A, C228A, C228A3		150	
C229B, C228B, C228B3		300	
C229C, C228C, C228C3		400	
C229D, C228D, C228D3		500	
C229E, C228E, C228E3		600	
C229M, C228M, C228M3		720	
Forward Current RMS	$I_{T(RMS)}$	35	Amp
Peak Surge Current (one cycle, 60 Hz) (T_C = -40 to +125°C)	I_{TSM}	300	Amp
Circuit Fusing Considerations (T_C = -40 to +125°C) (t = 1.0 to 8.3 ms)	I^2t	370	A^2s
Peak Gate Power	P_{GM}	5	Watts
Average Gate Power	$P_{G(AV)}$	0.5	Watt
Peak Forward Gate Current	I_{GM}	2	Amp
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C
Stud Torque	–	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
C228 and C229 Series		1.7	
C228( ) 3 Series		1.85	

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode.

7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (Rated V_{DRM}, with gate open)	T_C = 25°C T_C = 125°C	I_{DRM}	– –	– –	1 3	mA
Peak Reverse Blocking Current (Rated V_{RRM})	T_C = 25°C T_C = 125°C	I_{RRM}	– –	– –	1 3	mA
Forward "On" Voltage (I_{TM} = 100 A Peak)		V_{TM}	–	–	1.9	Volts
Gate Trigger Current (V_D = 12 Vdc, R_L = 80 Ohms, T_C = 25°C) (V_D = 6 Vdc, R_L = 50 Ohms, T_C = -40°C)		I_{GT}	 – –	 – –	 40 80	mA
Gate Trigger Voltage (V_D = 12 Vdc, R_L = 80 Ohms, T_C = 25°C) (V_D = 6 Vdc, R_L = 80 Ohms, T_C = -40°C)		V_{GT}	 – –	 – –	 2.5 3	Volts
Gate Trigger Voltage (Rated V_{DRM}, R_L = 1000 Ohms, T_C = +125°C)		V_{GT}	0.2	–	–	Volts
Holding Current (Anode Voltage = 24 V, gate open)	T_C = 25°C T_C = -40°C	I_H	– –	– –	75 150	mA
Turn-On Time (t_d + t_r) (I_{TM} = 35 Adc, I_{GT} = 40 mAdc)		t_{on}	–	1.0	–	μs
Turn-Off Time (I_{TM} = 10 A, I_R = 10 A) (I_{TM} = 10 A, I_R = 10 A, T_C = 100°C)		t_{off}	 – –	 20 35	 – –	μs
Forward Voltage Application Rate (T_C = 100°C)		dv/dt	–	50	–	V/μs

FIGURE 1 – CURRENT DERATING (HALF-WAVE RECTIFIED SINE WAVE)

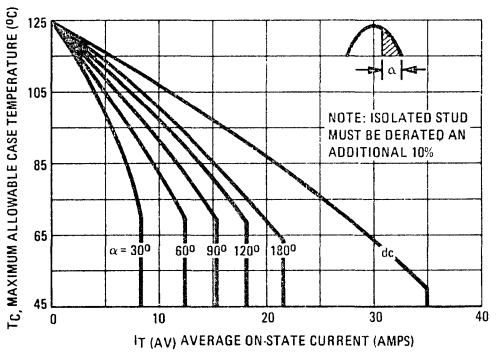
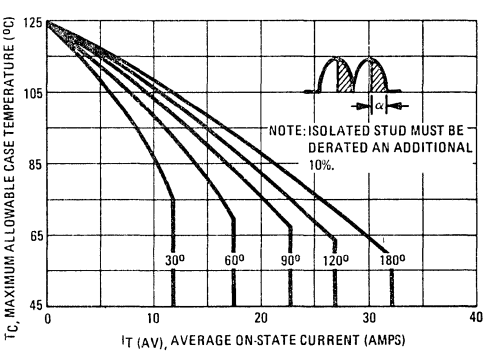


FIGURE 2 – CURRENT DERATING (FULL-WAVE RECTIFIED SINE WAVE)



7

C230, 231
C230( )3, 231( )3
C232, 233
series

REVERSE BLOCKING TRIODE-THYRISTOR

. . . designed for industrial and consumer applications such as power supplies; battery chargers; temperature, motor, light, and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current — I_{TSM} = 250 Amp
- Low Forward "On" Voltage — 1.2 V (Typ) @ I_{TM} = 25 Amp
- Practical Level Triggering and Holding Characteristics — 10 mA (Typ) @ T_C = 25°C
- Rugged Construction in Either Pressfit, Stud or Isolated Stud
- Glass Passivated Junctions for Maximum Reliability

SILICON CONTROLLED RECTIFIER

25 AMPERES RMS
50 thru 600 VOLTS

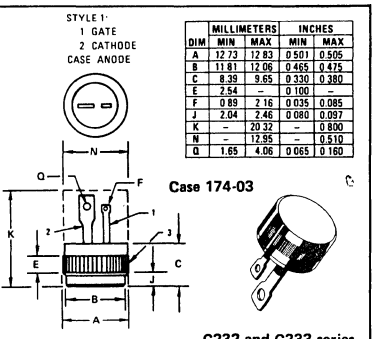
MAXIMUM RATINGS (T_C = 100°C unless otherwise noted)

Rating	Suffix	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (1) (T_C = −40 to +100°C) All Types	F A B C D E M	V_{DRM} and V_{RRM}	50 100 200 300 400 500 600	Volts
Non-Repetitive Reverse Voltage (T_C = −40 to 100°C) All Types	F A B C D E M	V_{RSM}	75 150 300 400 500 600 720	Volts
Forward Current RMS		$I_{T(RMS)}$	25	Amp
Peak Surge Current (One Cycle, 60 Hz)(T_C = −40 to 100°C)		I_{TSM}	250	Amp
Circuit Fusing (T_C = −40 to +100°C)(t = 1.0 to 8.3 ms)		I^2t	260	A^2s
Peak Gate Power		P_{GM}	5	Watts
Average Gate Power		$P_{G(AV)}$	0.5	Watt
Peak Forward Gate Current		I_{GM}	2	Amp
Operating Junction Temperature Range		T_J	−40 to +100	°C
Storage Temperature Range		T_{stg}	−40 to +125	°C
Stud Torque		—	30	in. lb.

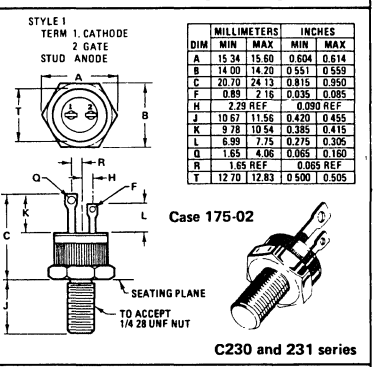
THERMAL CHARACTERISTICS

Characteristic		Symbol	Max	Unit
Thermal Resistance, Junction to Case Pressfit and Stud Isolated Stud		$R_{\theta JC}$	 1.00 1.15	°C/W

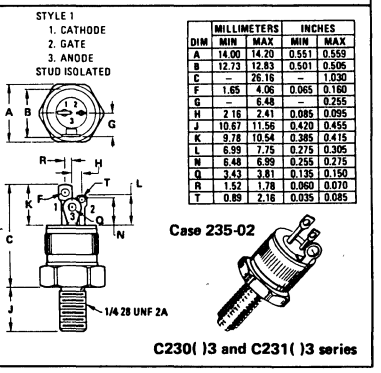
(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
B	11.81	12.06	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54	–	0.100	–
F	0.89	2.16	0.035	0.085
J	2.04	2.46	0.080	0.097
K	–	20.32	–	0.800
N	–	12.95	–	0.510
Q	1.65	4.06	0.065	0.160



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	0.89	2.16	0.035	0.085
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	1.65	4.06	0.065	0.160
R	1.65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505

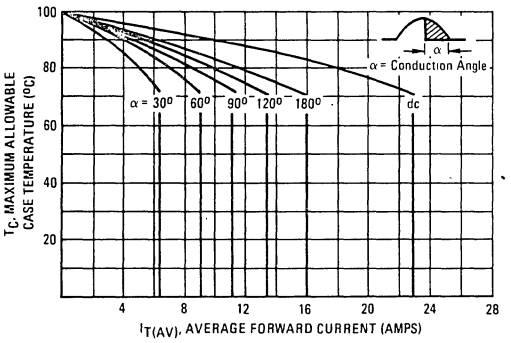


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	26.16	–	1.030
F	1.65	4.06	0.065	0.160
G	–	6.48	–	0.255
H	2.16	2.41	0.085	0.095
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
N	6.48	6.99	0.255	0.275
Q	3.43	3.81	0.135	0.150
R	1.52	1.78	0.060	0.070
T	0.89	2.16	0.035	0.085

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Currrent		I_{DRM}				mA
(V_D = Rated V_{DRM}, with gate open)	T_C = 25°C	or	–	–	0.5	
(V_R = Rated V_{RRM})	T_C = 100°C	I_{RRM}	–	–	1.0	
Forward "On" Voltage		V_{TM}	–	–	1.9	Volts
(I_{TM} = 100 A Peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%)						
Gate Trigger Current, C230, C230( )3, C232 series		I_{GT}				mA
(V_D = 12 Vdc, R_L = 120 Ohms)			–	–	25	
(V_D = 12 Vdc, R_L = 60 Ohms)	T_C = –40°C		–	–	40	
Gate Trigger Current, C231, C231( )3, C233		I_{GT}				mA
(V_D = 12 Vdc, R_L = 120 Ohms)			–	–	9.0	
(V_D = 12 Vdc, R_L = 60 Ohms)	T_C = –40°C		–	–	20	
Gate Trigger Voltage		V_{GT}				Volts
(V_D = 12 Vdc, R_L = 120 Ohms)			–	–	1.5	
(V_D = 12 Vdc, R_L = 60 Ohms)	T_C = –40°C		–	–	2.0	
(V_D = Rated V_{DRM}, R_L = 1000 Ohms)	T_C = +100°C		0.2	–	–	
Holding Current		I_H	–	–	50	mA
(V_D = 24 V, gate open, I_T = 0.5 A)	T_C = –40°C		–	–	100	
Turn-On Time (t_d + t_r)		t_{gt}	–	1.0	–	μs
(I_{TM} = 25 Adc, I_{GT} = 40 mAdc, V_D = Rated V_{DRM})						
Turn-Off Time		t_q				μs
(I_{TM} = 10 A, I_R = 10 A, Pulse Width = 50 μs,			–	25	–	
dv/dt = 20 V/μs, V_D = Rated V_{DRM})	T_C = 100°C		–	35	–	
Forward Voltage Application Rate		dv/dt	–	100	–	V/μs
(V_D = Rated V_{DRM})	T_C = 100°C					

FIGURE 1 – CURRENT DERATING FOR PRESSFIT AND NON-ISOLATED STUD



NOTE: Derating is for Pressift and Stud Devices. Isolated stud devices must be derated an additional 15%. For example, the max T_C @ 16 A (180° conduction angle) is 70°C, a derating of 30°C. Isolated stud devices must be derated 34.5°C; therefore, the maximum T_C is 65.5°C.

FIGURE 2 – ON-STATE POWER DISSIPATION versus ON-STATE CURRENT

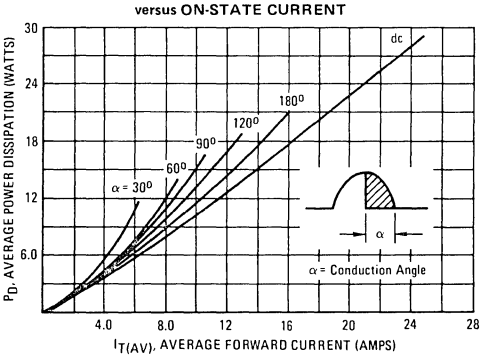


FIGURE 3 – GATE CURRENT VARIATION WITH TEMPERATURE

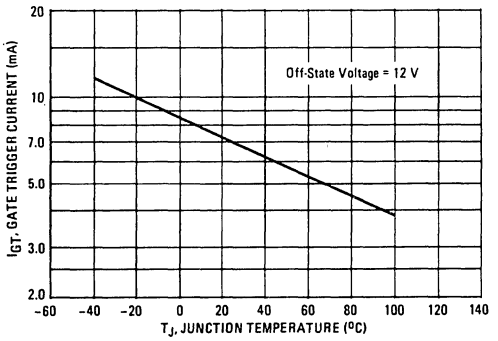
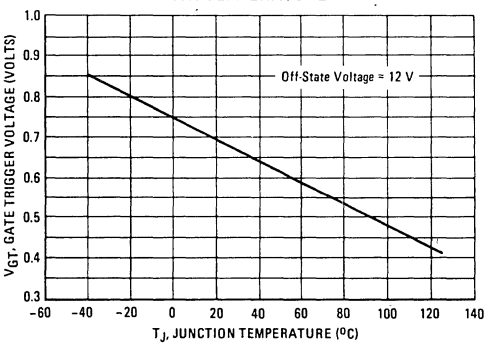


FIGURE 4 – GATE VOLTAGE VARIATION WITH TEMPERATURE



MAC15
MAC15A

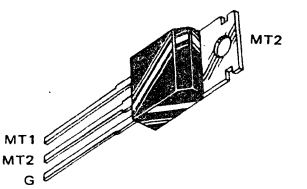
BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for full-wave ac control applications, such as solid-state relays, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in Two Modes (MAC15)
  Four Modes (MAC15A)

TRIACS

15 AMPERES RMS
200—800 VOLTS

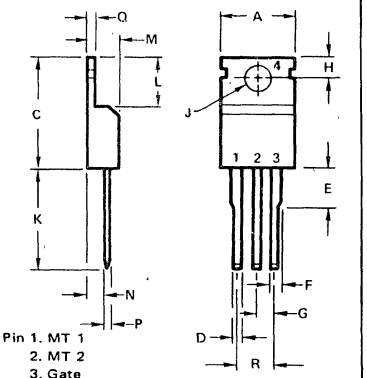


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (T_J = -40 to 125°C)	V_{DRM}		Volts
MAC15-4, MAC15A-4		200	
MAC15-6, MAC15A-6		400	
MAC15-8, MAC15A-8		600	
MAC15-10, MAC15A-10		800	
Peak Gate Voltage	V_{GM}	10	Volts
On-State Current RMS Full Cycle Sine Wave 50 to 60 Hz (T_C = +90°C)	$I_{T(RMS)}$	15	Amp
Circuit Fusing	I^2t	93	A^2sec
Peak Surge Current (One Full Cycle, 60 Hz, T_C = +80°C) preceded and followed by rated current	I_{TSM}	150	Amp
Peak Gate Power (T_C = +80°C, Pulse Width = 2 μs	P_{GM}	20	Watts
Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.5	Watt
Peak Gate Current	I_{GM}	2	Amp
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTIC

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W



All JEDEC dimensions and notes apply

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.380	0.420	9.660	10.66
C	0.560	0.625	14.23	15.87
D	0.020	0.045	0.510	1.140
E		0.250		6.350
F	0.045	0.070	1.140	1.770
G	0.090	0.110	2.290	2.790
H	0.100	0.120	2.540	3.040
J	0.139	0.147	3.531	3.733
K	0.500	0.562	12.70	14.27
L	0.230	0.270	5.850	6.820
M	0.140	0.190	3.560	4.820
N	0.080	0.115	2.040	2.920
P	0.012	0.045	0.310	1.140
Q	0.020	0.055	0.510	1.390
R	0.190	0.210	4.830	5.330

CASE 221-02
TO-220 AB

▲Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and either polarity of MT2 to MT1 Voltage unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current V_D = Rated V_{DRM} @ T_J = 125°C, Gate Open	I_{DRM}	–	–	2	mA
Peak On-State Voltage I_{TM} = 21 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%	V_{TM}	–	1.3	1.6	Volts
Peak Gate Trigger Current V_D = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2 μs	I_{GTM}				mA
MT2 (+), G(+) – MAC15, MAC15A		–	–	50	
MT2 (+), G(–) – MAC15A		–	–	75	
MT2 (–), G(–) – MAC15, MAC15A		–	–	50	
MT2 (–), G(+) – MAC15A		–	–	75	
Peak Gate Trigger Voltage V_D = 12 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2 μs	V_{GTM}				Volts
MT2 (+), G(+) – MAC15, MAC15A		–	0.9	2	
MT2 (+), G(–) – MAC15A		–	0.9	2.5	
MT2 (–), G(–) – MAC15, MAC15A		–	1.1	2	
MT2 (–), G(+) – MAC15A		–	1.4	2.5	
V_D = Rated V_{DRM}, R_L = 10k Ohms, T_J = 110°C					
MT2 (+), G(+); MT2 (–), G(–) – MAC15, MAC15A		0.2	–	–	
MT2 (+), G(–); MT2 (–), G(+) – MAC15A		0.2	–	–	
Holding Current (Either Direction) V_D = 12 Vdc, Gate Open I_T = 200 mA	I_H	–	6	40	mA
Turn-On Time V_D = Rated V_{DRM}, I_{TM} = 17 A I_{GT} = 120 mA, Rise Time = 0.1 μs, Pulse Width = 2 μs	tgt	–	1.5	2	μs
Critical Rate of Rise of Commutation Voltage V_D = Rated V_{DRM}, I_{TM} = 21 A, Commutating di/dt = 8 A/ms, Gate Unenergized, T_C = 80°C	dv/dt(c)	–	5	–	V/μs

FIGURE 1 – RMS CURRENT DERATING

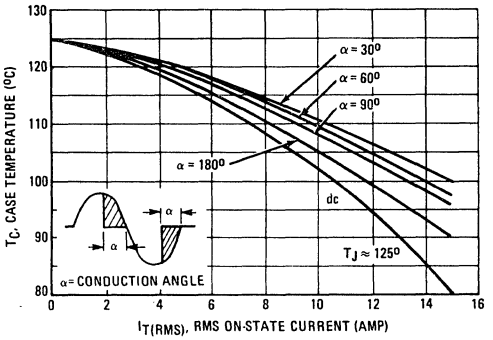


FIGURE 2 – ON-STATE POWER DISSIPATION

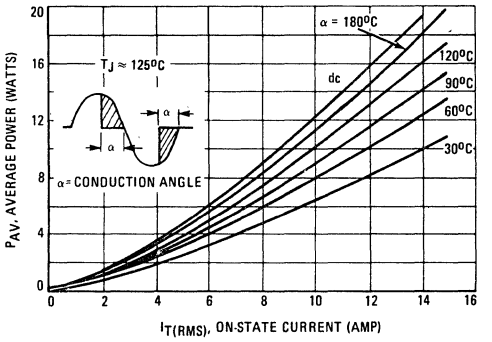


FIGURE 3 – TYPICAL GATE TRIGGER VOLTAGE

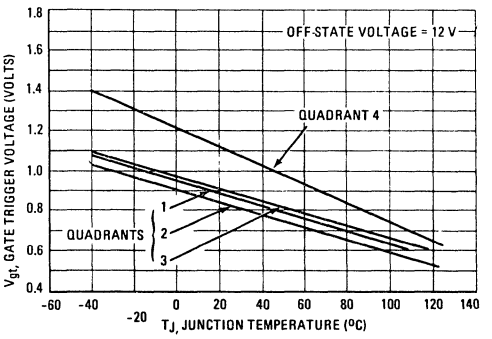


FIGURE 4 – TYPICAL GATE TRIGGER CURRENT

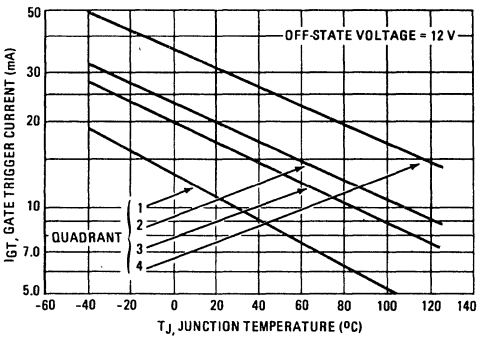


FIGURE 5 – ON-STATE CHARACTERISTICS

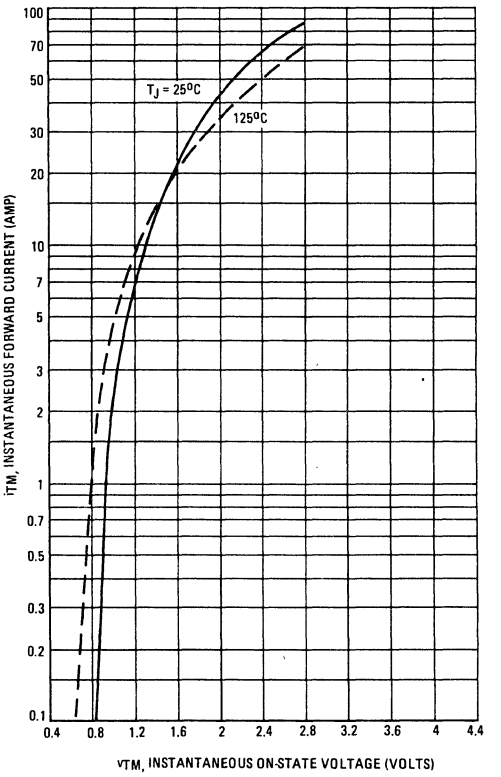


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FIGURE 6 – TYPICAL HOLDING CURRENT

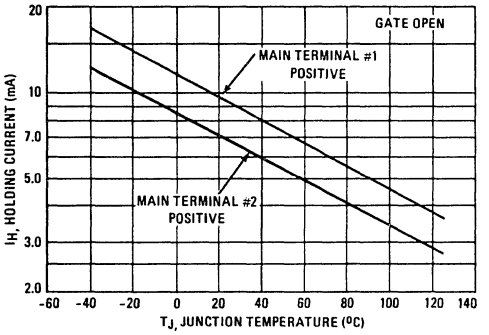


FIGURE 7 – MAXIMUM NON-REPETITIVE SURGE CURRENT

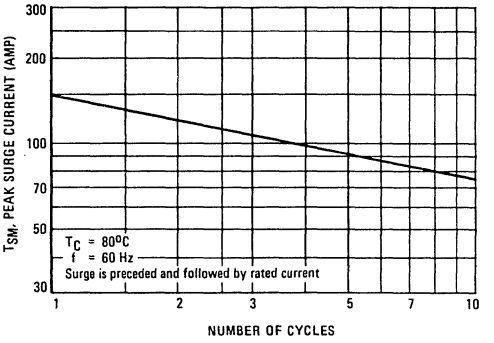
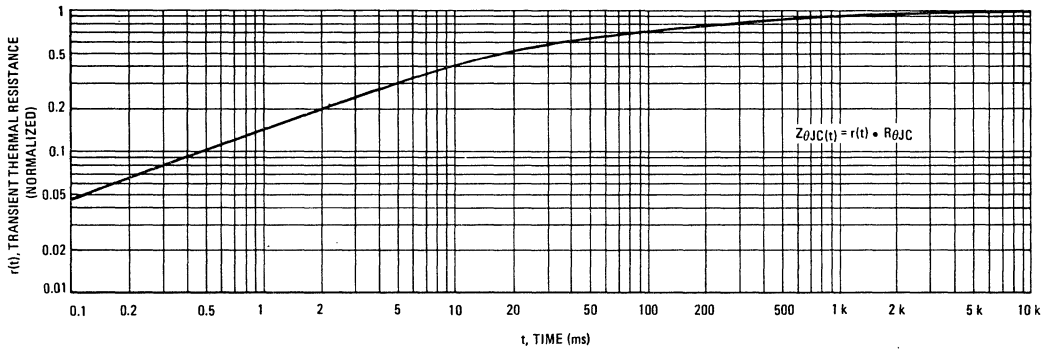


FIGURE 8 – THERMAL RESPONSE



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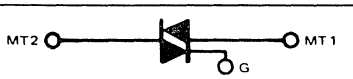
MAC20/MAC20A
15 AMPERES RMS

MAC25/MAC25A
25 AMPERES RMS

MAC50/MAC50A
40 AMPERES RMS



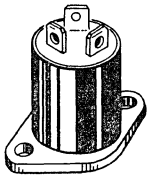
TRIACS

200-800 VOLTS

SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for industrial and consumer applications for full-wave control of ac loads such as appliance controls, power supplies, solid-state relays, heating controls, motor controls, welding equipment, and power switching systems.

- Electrically Isolated From Mounting Base
- Isolation Voltage of 2500 Volts RMS
- Quick Connect/Disconnect Terminals
- Glass-Passivated and Center Gate Geometry
- Gate Triggering Guaranteed in Three Modes (MAC20/25/50)
  Four Modes (MAC20A/25A/50A)



MAXIMUM RATINGS (T_J = -0 to +125°C unless otherwise noted)

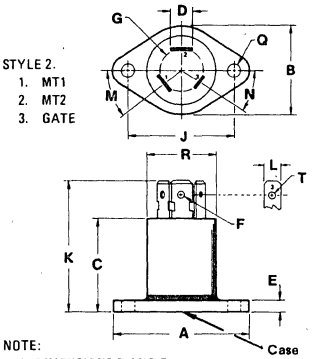
Rating	Symbol	MAC series 20	25	50	Unit
Repetitive Peak Off-State Voltage 1/2 Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}				Volts
MAC20/25/50-4, MAC20A/25A/50A-4		← 200 →			
MAC20/25/50-5, MAC20A/25A/50A-5		← 300 →			
MAC20/25/50-6, MAC20A/25A/50A-6		← 400 →			
MAC20/25/50-7, MAC20A/25A/50A-7		← 500 →			
MAC20/25/50-8, MAC20A/25A/50A-8		← 600 →			
MAC20/25/50-9, MAC20A/25A/50A-9		← 700 →			
MAC20/25/50-10, MAC20A/25A/50A-10		← 800 →			
RMS On-State Current. (T_C = 100°C for MAC20/A)	$I_{T(RMS)}$	15	–	–	Amps
T_C = 90°C for MAC25/A)		–	25	–	
(T_C = 70°C for MAC50/A)		–	–	40	
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	150	250	300	Amps
Circuit Fusing (t = 1 to 8.3 ms)	I^2t	90	260	375	A^2s
Average Gate Power	$P_{G(AV)}$	0.5	0.5	0.75	Watts
Peak Gate Current (10 μs)	I_{GM}	2	2	4	Amps
Operating Junction Temperature Range	T_J	-0 to +125			°C
Storage Temperature Range	T_{stg}	-40 to +125			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Maximum Value			Unit
Thermal Resistance, Junction to Case (DC)	$R_{\theta JC}$	1.6	1.5	1.4	°C/W
(Apparent)*		1.3	1.0	0.95	

*Defined as: $\frac{(125^{\circ}C - T_C)}{P_{AV}}$ for a 60 Hz full sine wave.

*Gate terminal thickness of .032" is available. Designate a device with .032" terminals by adding a T after the device type. For example, MAC20A4T.



NOTE:
1. DIMENSIONS D AND F APPLY TO TERM 1 AND 2.
2. MT1 AND MT2 THICKNESSES ARE A NOMINAL 0.032". GATE TERMINAL THICKNESS IS A NOMINAL 0.020".*

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	39.37	–	1.550
B	–	26.67	–	1.050
C	–	27.30	–	1.075
D	6.22	6.48	0.245	0.255
E	3.02	3.33	0.119	0.131
F	–	1.78	–	0.070
G	12.19	12.70	0.480	0.500
J	29.90	30.40	1.177	1.197
K	35.56	37.08	1.400	1.460
L	4.57	4.95	0.180	0.195
M	35°	40°	35°	40°
N	30°	35°	30°	35°
Q	3.81	4.09	0.150	0.161
R	19.81	22.35	0.780	0.880
T	–	1.52	–	0.060

CASE 326-01

ELECTRICAL CHARACTERISTICS

(All voltage polarity reference to MT1; applies to either polarity of MT2 to MT1, $T_C = 25^oC$ unless otherwise noted)

Characteristic		Symbol	MAC20/20A Min	MAC20/20A Typ	MAC20/20A Max	MAC25/25A Min	MAC25/25A Typ	MAC25/25A Max	MAC50/50A Min	MAC50/50A Typ	MAC50/50A Max	Unit
Peak Blocking Current	$T_C = 125^oC$	I_{DRM}	–	–	2	–	–	2	–	–	2	mA
V_D = Rated V_{DRM}, Gate Open	$T_C = 25^oC$		–	–	0.1	–	–	0.1	–	–	0.1	
Peak On-State Voltage		V_{TM}										Volts
Pulse Width = 1 ms, Duty Cycle 2%												
I_{TM} = 21 A Peak	MAC20/20A		–	1.3	1.6	–	–	–	–	–	–	
I_{TM} = 35 A Peak	MAC25/25A		–	–	–	–	1.4	1.7	–	–	–	
I_{TM} = 56 A Peak	MAC50/50A		–	–	–	–	–	–	–	1.65	1.75	
Peak Gate Trigger Current		I_{GTM}										mA
V_D = 12 Vdc, R_L = 50 Ohms, Pulse Width = 2 μs												
MT2 (+), G (+); MT2 (–), G (–); MT2 (+), G (–)			–	15	50	–	20	70	–	20	70	
MT2 (–), G (+)	A Suffix Only		–	30	75	–	35	100	–	35	100	
Peak Gate Trigger Voltage		V_{GTM}										Volts
V_D = 12 Vdc, R_L = 50 Ohms, Pulse Width = 2 μs												
MT2 (+), G (+); MT2 (–), G (–); MT2 (+), G (–)			–	0.9	2	–	1.1	2	–	1.1	2	
MT2 (–), G (+)	A Suffix Only		–	1.4	2.5	–	1.3	2.5	–	1.3	2.5	
V_D = Rated V_{DRM}, R_L = 10 kΩ, $T_C = 125^oC$			0.2	–	–	0.2	–	–	0.2	–	–	
Holding Current		I_H	–	6	40	–	10	75	–	10	75	mA
V_D = 12 Vdc, Gate Open, R_L = 40 Ohms												
Turn-On Time		tgt										μs
V_D = Rated V_{DRM},												
I_{TM} = 17 A, I_G = 120 mA	MAC20/20A		–	1.5	–	–	–	–	–	–	–	
I_{TM} = 25 Adc, I_G = 200 mA	MAC25/25A		–	–	–	–	1.5	–	–	–	–	
I_{TM} = 56 A, I_G = 200 mA	MAC50/50A		–	–	–	–	–	–	–	1.5	–	
Critical Rate-of-Rise of Commutation Voltage		dv/dt(c)										V/μs
V_D = Rated V_{DRM}, I_{TM} = 21 A, Commutating di/dt = 8 A/ms, $T_C = 100^oC$	MAC20/20A		5	30	–	–	–	–	–	–	–	
V_D = Rated V_{DRM}, I_{TM} = 35 A, Commutating di/dt = 16 A/ms, $T_C = 90^oC$	MAC25/25A		–	–	–	5	30	–	–	–	–	
V_D = Rated V_{DRM}, I_{TM} = 40 A, Commutating di/dt = 22 A/ms, $T_C = 70^oC$	MAC50/50A		–	–	–	–	–	–	5	30	–	
Critical Rate-of-Rise of Off-State Voltage (Exponential Rise)		dv/dt	–	100	–	–	100	–	–	75	–	V/μs
V_D = Rated V_{DRM}, Gate Open, $T_C = 125^oC$												

FIGURE 1 – CURRENT DERATING

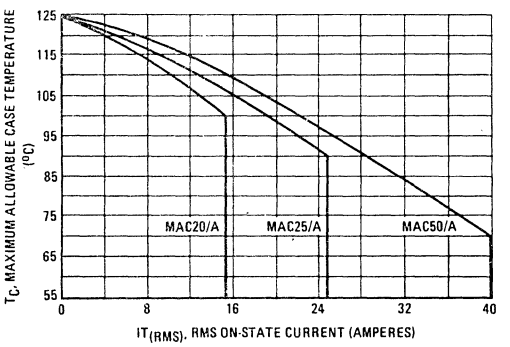
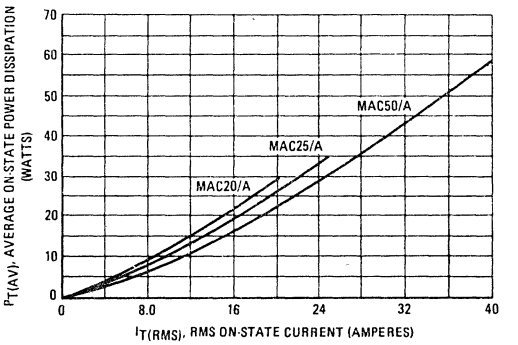


FIGURE 2 – MAXIMUM POWER DISSIPATION



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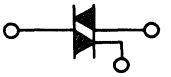
MAC35-1 thru MAC35-8, MAC35-10

MAC36-1 thru MAC36-8, MAC36-10



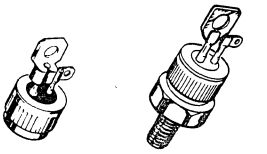
SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as solid-state relays, light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- 25 Amperes RMS @ T_C = 67°C
- Low On-State Voltage – 1.5 Volts Maximum
- Glass Passivated Junctions for Maximum Reliability

TRIAC
(THYRISTORS)

25 AMPERES RMS
25 thru 800 VOLTS



MAC 35
CASE 310-01

MAC 36
CASE 263-03

MAXIMUM RATINGS

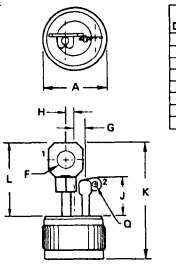
Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (1) (T_J = 110°C) MAC35 −1	V_{DRM}	25	Volts
MAC35 −2		50	
MAC35 −3		100	
MAC35 −4		200	
MAC36 −5		300	
MAC36 −6		400	
MAC36 −7		500	
MAC36 −8		600	
MAC36 −10		800	
On-State Current RMS	$I_{T(RMS)}$	25	Amp
Peak Surge Current (One Full cycle, 60 Hz, T_J = −40 to +110°C)	I_{TSM}	225	Amp
Circuit Fusing Considerations (T_J = −40 to +110°C, t = 1.0 to 8.3 ms)	I^2t	210	A^2s
Peak Gate Power (2)	P_{GM}	5.0	Watts
Average Gate Power	$P_{G(AV)}$	0.5	Watt
Peak Gate Current (2)	I_{GM}	2.0	Amp
Operating Junction Temperature Range	T_J	−40 to +110	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.0	°C/W
Stud Torque	–	30	in. lb.

(1) For either direction of blocking voltage. V_{DRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

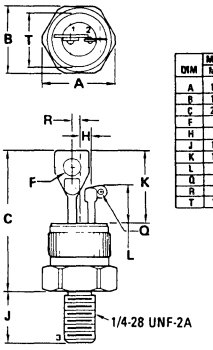
(2) T_J = 110°C, 1.0 second maximum duration; 5.0% duty cycle, I_{TM} = 10 Amps.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.60	2.01	0.063	0.079
J	7.62	8.89	0.300	0.350
K	–	26.67	–	1.050
L	–	17.02	–	0.670
Q	1.40	2.16	0.055	0.085

STYLE 1:
1. CATHODE
2. GATE
CASE. ANODE

CASE 310-01 MAC35



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

STYLE 1:
PIN 1. CATHODE
2. GATE
3. ANODE

CASE 263-03 MAC36

Metric "M6" thread denoted by addition of M following last digit of part number, i.e., MAC36-1M.

DS 8533 R1

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 110°C	I_{DRM}	–	–	4.0	mA
On-State Voltage (Either Direction) I_{TM} = 35 A Peak	V_{TM}	–	1.3	1.5	Volts
Gate Trigger Current, Continuous dc (1) Main Terminal Voltage = 7.0 Vdc, R_L = 47 ohms					
MT2(+)G(+); MT2(–)G(–)	I_{GT}	–	20	75	mA
MT2(+)G(–); MT2(–)G(+)	I_{GT}	–	30	100	mA
Gate Trigger Voltage, Continuous dc (1) Main Terminal Voltage = 7.0 Vdc, R_L = 47 ohms					
MT2(+)G(+); MT2(–)G(–)	V_{GT}	–	1.0	3.0	Volts
MT2(+) G(–); MT2(–)G(+)	V_{GT}	–	1.2	3.0	Volts
Gate Trigger Voltage, Continuous dc – All Modes Main Terminal Voltage = Rated V_{DRM}, R_L = 100 ohms, T_J = 110°C	V_{GD}	0.2	–	–	Volt
Holding Current (Either Direction) Main Terminal Voltage = 7.0 Vdc, Gate Open, Initiating Current = 150 mA	I_H	–	10	75	mA
Turn-On Time I_{TM} = 25 Adc, I_{GT} = 200 mA	t_{on}	–	1.0	–	μs
Critical Forward Voltage Application Rate (Exponential Rise of Voltage) @ V_{DRM}, T_J = 110°C, Gate Open	dv/dt	–	100	–	V/μs

FIGURE 1 – MAXIMUM THERMAL RESPONSE

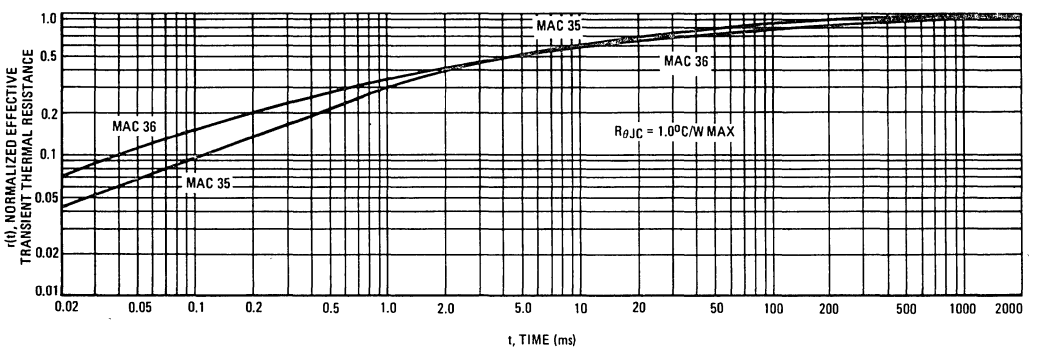

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FIGURE 2 – AVERAGE CURRENT DERATING

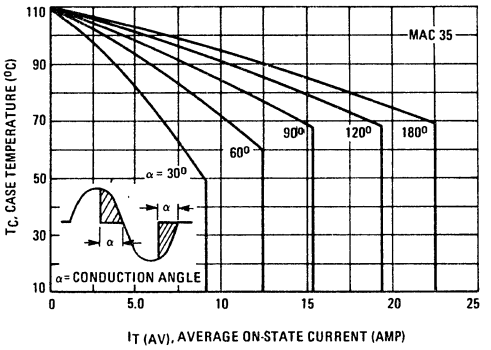

FIGURE 3 – RMS CURRENT DERATING

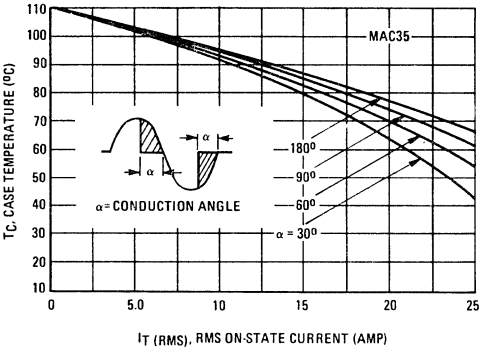

FIGURE 4 – AVERAGE CURRENT DERATING

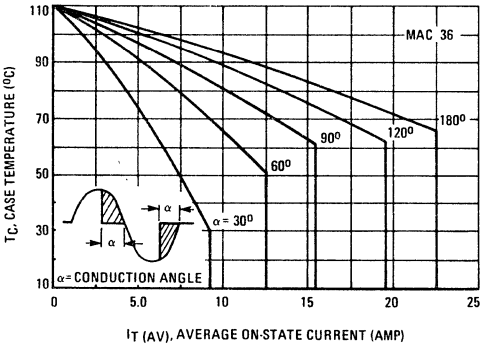

FIGURE 5 – RMS CURRENT DERATING

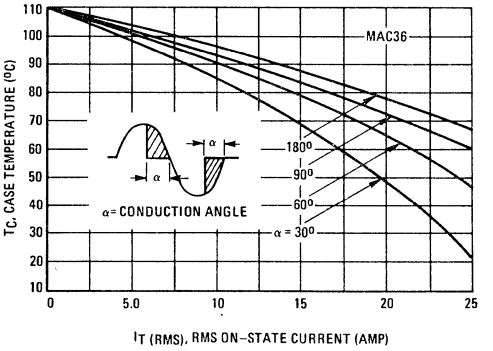

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FIGURE 6 – POWER DISSIPATION versus AVERAGE CURRENT

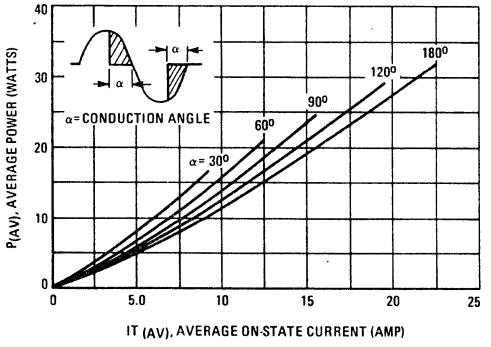


FIGURE 7 – POWER DISSIPATION versus RMS CURRENT

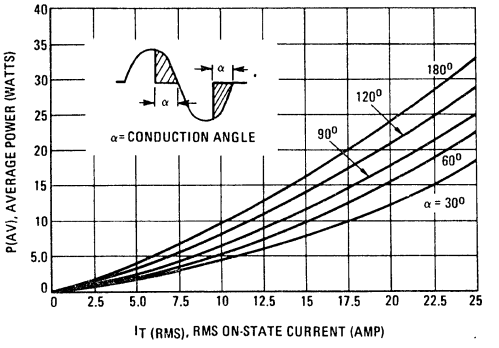


FIGURE 8 – MAXIMUM ON-STATE CHARACTERISTICS

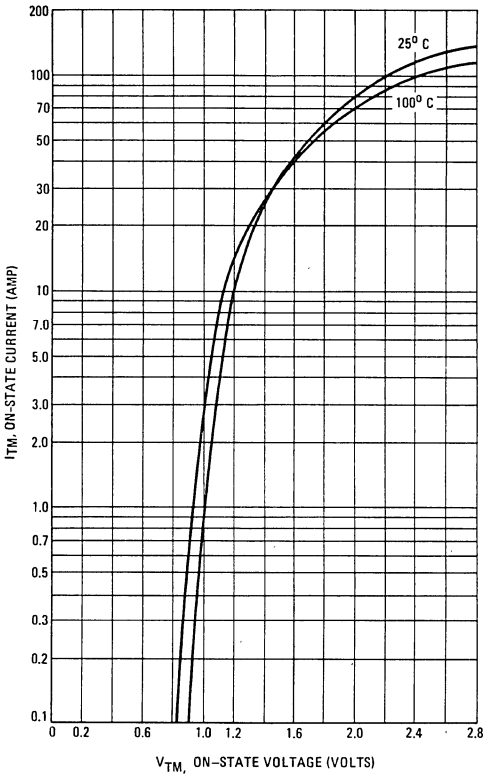


FIGURE 9 – MAXIMUM MULTI-CYCLE SURGE RATING

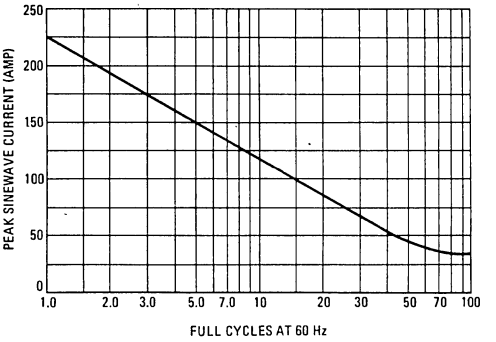


FIGURE 10 – TYPICAL HOLDING CURRENT

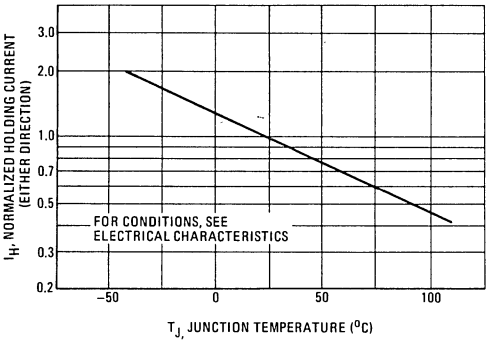


FIGURE 11 – TYPICAL GATE TRIGGER CURRENT

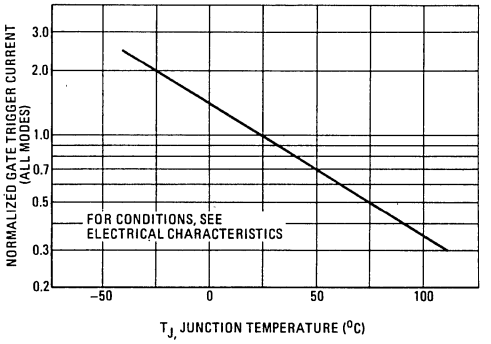
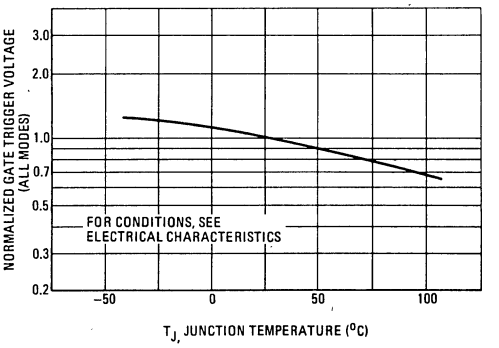


FIGURE 12 – TYPICAL GATE TRIGGER VOLTAGE



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MAC37-1 thru MAC37-7 (SILICON)
MAC38-1 thru MAC38-7

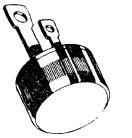
SILICON BIDIRECTIONAL THYRISTORS

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- Glass Passivated and Center Gate Fire
- 25 Amperes RMS @ T_C = 67°C
- Isolated Stud Available

TRIAC
(THYRISTORS)

25 AMPERES RMS
25 thru 500 VOLTS



MAC37

MAC38

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (1) (T_J = 110°C) MAC37 −1	V_{DRM}	25	Volts
MAC37 −2		50	
MAC37 −3		100	
MAC38 −4		200	
MAC38 −5		300	
MAC38 −6		400	
MAC38 −7		500	
On-State Current RMS	$I_{T(RMS)}$	25	Amp
Peak Surge Current (One Full cycle, 60 Hz, T_J = −40 to +110°C)	I_{TSM}	225	Amp
Circuit Fusing Considerations (T_J = −40 to +110°C, t = 1.0 to 8.3 ms)	I^2t	210	A^2s
Peak Gate Power (2)	P_{GM}	5.0	Watts
Average Gate Power	$P_{G(AV)}$	0.5	Watt
Peak Gate Current (2)	I_{GM}	2.0	Amp
Operating Junction Temperature Range	T_J	−40 to +110	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C
Stud Torque	—	30	in. lb.

(1) For either direction of blocking voltage. V_{DRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

(2) T_J = 110°C, 1.0 second maximum duration; 5.0% duty cycle, I_{TM} = 10 Amp.

THERMAL CHARACTERISTICS

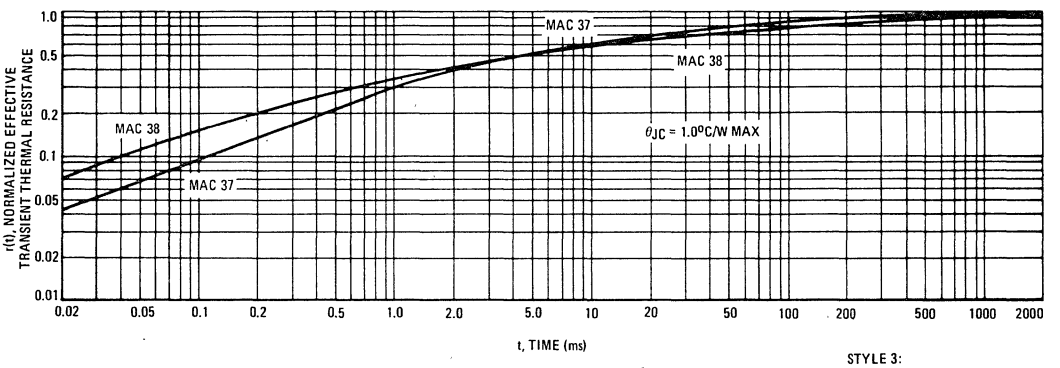
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.0	°C/W

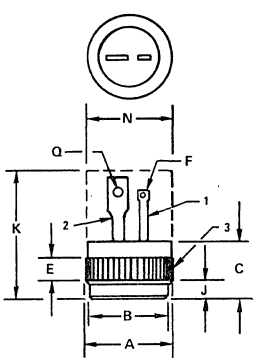
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Blocking Current (Either Direction) Rated V_{DRM} @ T_J = 110°C	I_{DRM}	–	–	2.0	mA
On-State Voltage (Either Direction) I_{TM} = 35 A Peak	V_{TM}	–	1.4	1.9	Volts
Gate Trigger Current, Continuous dc (1) Main Terminal Voltage = 7.0 Vdc, R_L = 47 ohms MT2(+)G(+); MT2(–)G(–)	I_{GT}	–	20	75	mA mA
Gate Trigger Voltage, Continuous dc (1) Main Terminal Voltage = 7.0 Vdc, R_L = 47 ohms MT2(+)G(+); MT2(–)G(–)	V_{GT}	–	1.0	3.0	Volts
Gate Trigger Voltage, Continuous dc – MT2(+) G(+); MT2(–) G(–) Main Terminal Voltage = Rated V_{DRM}, R_L = 100 ohms, T_J = 110°C	V_{GD}	0.2	–	–	Volt
Holding Current (Either Direction) Main Terminal Voltage = 7.0 Vdc, Gate Open, Initiating Current = 150 mA	I_H	–	10	75	mA
Turn-On Time I_{TM} = 25 Adc, I_{GT} = 200 mA	t_{on}	–	1.0	–	μs
Critical Forward Voltage Application Rate (Exponential Rise of Voltage) @ V_{DRM}, T_J = 110°C, Gate Open	dv/dt	–	100	–	V/μs

(1) All voltage polarity reference to main terminal 1.

FIGURE 1 – MAXIMUM THERMAL RESPONSE

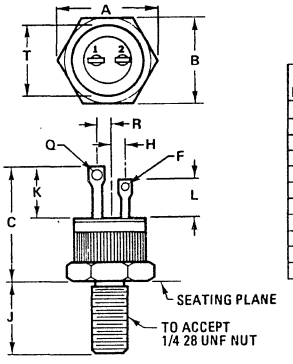




STYLE 3:
TERM. 1. GATE
2. MAIN TERMINAL 1
3. MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
B	11.81	12.06	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54	–	0.100	–
F	0.89	2.16	0.035	0.085
J	2.04	2.46	0.080	0.097
K	–	20.32	–	0.800
N	–	12.95	–	0.510
Q	1.65	4.06	0.065	0.160

CASE 174-03
MAC37



STYLE 3:
TERM. 1. MAIN TERMINAL 1
2. GATE
STUD: MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	0.89	2.16	0.035	0.085
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	1.65	4.06	0.065	0.160
R	1.65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505

CASE 175-02
MAC38

FIGURE 2 – AVERAGE CURRENT DERATING

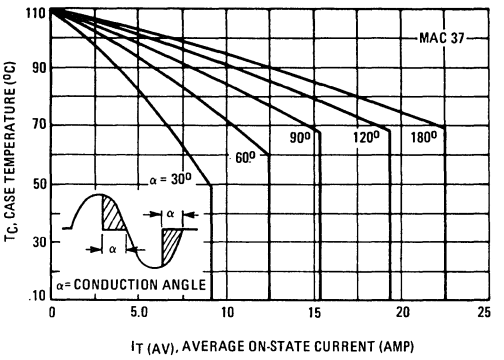


FIGURE 3 – RMS CURRENT DERATING

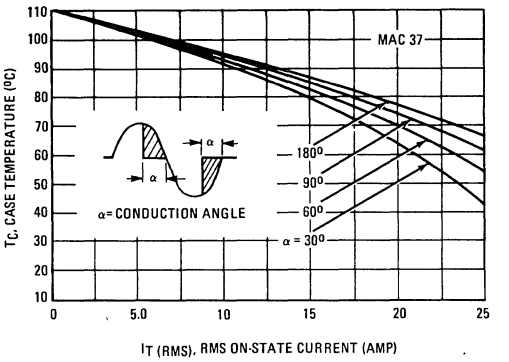


FIGURE 4 – AVERAGE CURRENT DERATING

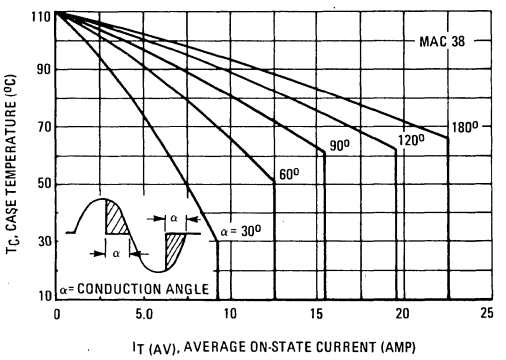


FIGURE 5 – RMS CURRENT DERATING

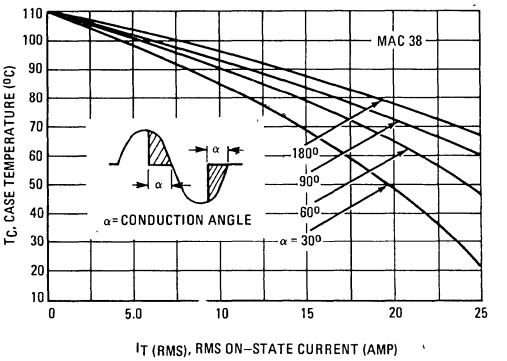


FIGURE 6 – POWER DISSIPATION versus AVERAGE CURRENT

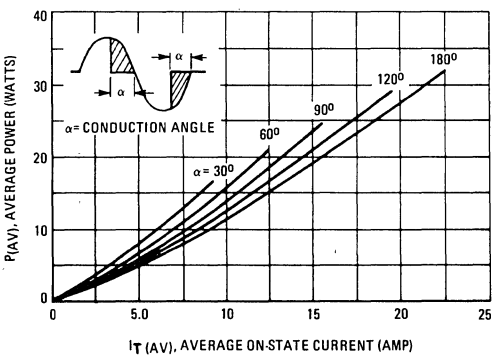


FIGURE 7 – POWER DISSIPATION versus RMS CURRENT

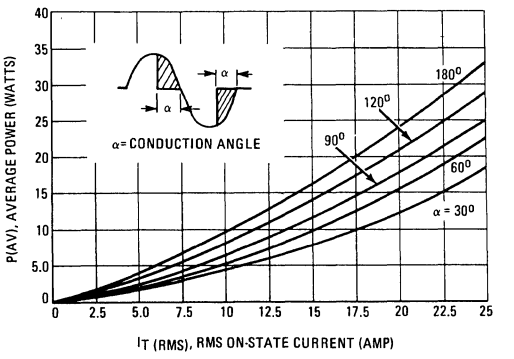


FIGURE 8 – MAXIMUM ON-STATE CHARACTERISTICS

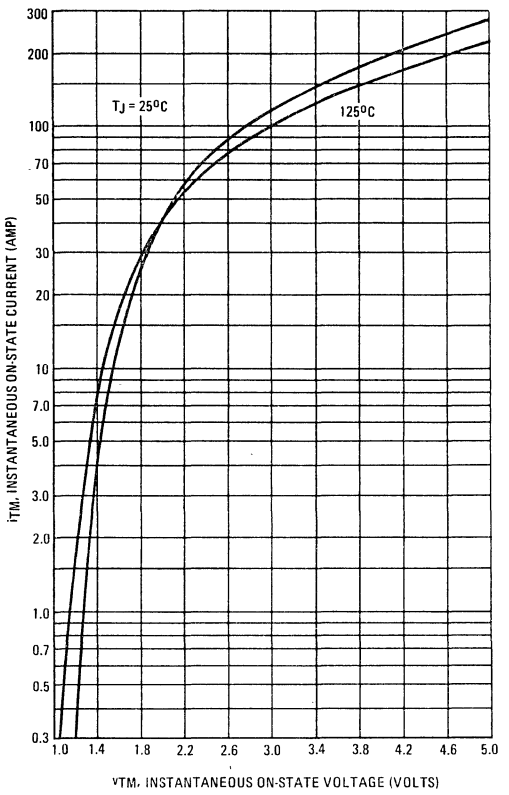


FIGURE 9 – MAXIMUM MULTI-CYCLE SURGE RATING

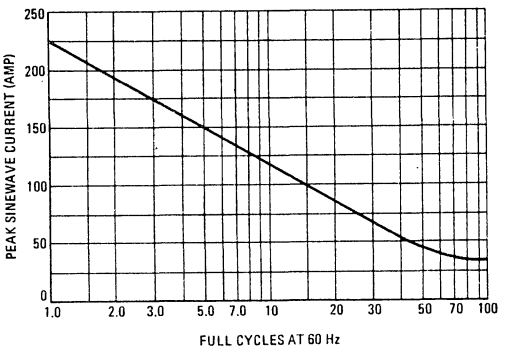


FIGURE 10 – TYPICAL HOLDING CURRENT

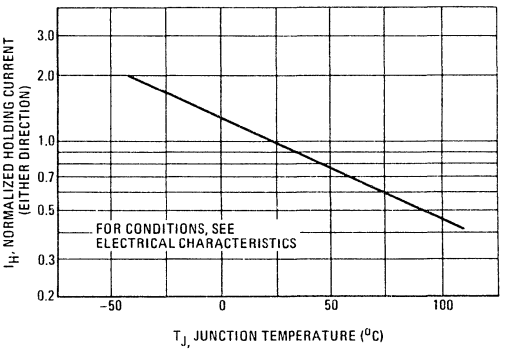


FIGURE 11 – TYPICAL GATE TRIGGER CURRENT

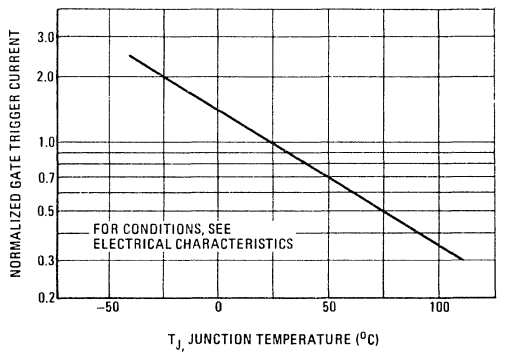
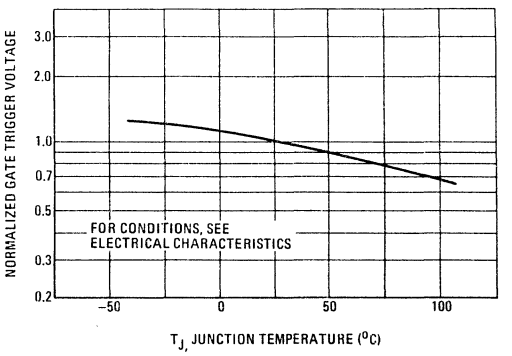


FIGURE 12 – TYPICAL GATE TRIGGER VOLTAGE



MAC92-1 thru MAC92-8

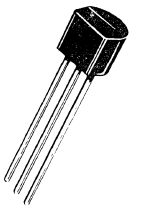
TRIACS

0.6 AMPERE RMS
30–600 VOLTS

SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed for use in solid state relays, TTL logic and light industrial applications. Supplied in an inexpensive plastic TO-92 package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Triggering Guaranteed in Three Modes
- One-Piece, Injection-Molded Unibloc ▲ Package



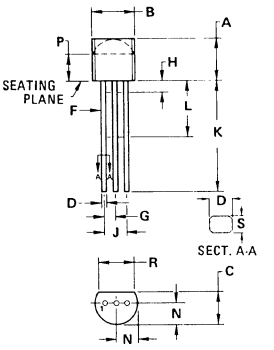
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (T_J = -40 to +110°C) ½ Sine Wave 50 to 60 Hz, Gate Open	V_{DRM}		Volts
MAC92 – 1		30	
– 2		60	
– 3		100	
– 4		200	
– 5		300	
– 6		400	
– 7		500	
– 8		600	
On-State RMS Current Full Cycle Sine Wave 50 to 60 Hz, (T_C = +50°C)	$I_{T(RMS)}$	0.8	Amp
Peak Non-Repetitive Surge Current (One Full Cycke, 60 Hz, T_C = +50°C) preceded and followed by rated current	I_{TSM}	8.0	Amp
Circuit Fusing Considerations (T_J = -40 to +110°C, t = 1.0 to 8.3 ms)	I^2t	0.26	A^2s
Average Gate Power	$P_{G(AV)}$	0.01	Watt
Peak Gate Current	I_{GM}	1.0	Amp
Operating Junction Temperature Range	T_J	-40 to +110	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

▲Trademark of Motorola Inc.



STYLE 12
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.
CASE 29-02
TO-92

7

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1 Voltage unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Peak Blocking Current V_D = Rated V_{DRM} @ T_J = 110°C, Gate Open	I_{DRM}	–	100	μA
Peak On-State Voltage I_{TM} = 1.0 A Peak; Pulse Width = 1.0 to 2.0 ms, Duty Cycle ≤ 2.0%	V_{TM}	–	1.9	Volts
Gate Trigger Current, Continuous dc V_D = 7.0 Vdc, R_L = 100 Ohms MT2(+), G(+); MT2(–), G(–), MT2(+), G(–)	I_{GT}	–	5.0	mA
Gate Trigger Voltage, Continuous dc V_D = 7.0 Vdc, R_L = 100 Ohms Minimum Gate Pulse Width = 2.0 μs MT2(+), G(+); MT2(–), G(–), MT2(+), G(–) MT2(+), G(+); MT2(–), G(–), MT2(+), G(–); T_C = –40°C V_D = Rated V_{DRM}, R_L = 10 k ohms, T_J = 110°C MT2(+), G(+); MT2(–), G(–)	V_{GT}	– – 0.1	2.5 3.5 –	Volts
Holding Current V_D = 7.0 Vdc, Gate Open; T_C = 25°C Initiating Current = 20 mA T_C = –40°C	I_H	– –	10 20	mA

FIGURE 1 – TYPICAL GATE TRIGGER VOLTAGE

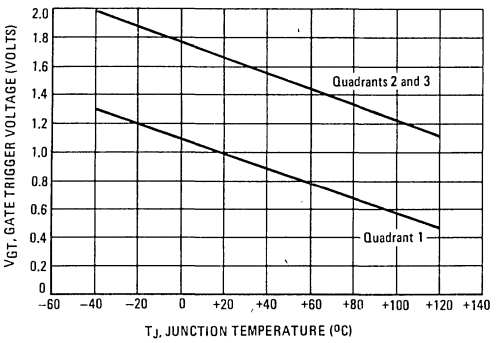


FIGURE 2 – TYPICAL GATE TRIGGER CURRENT

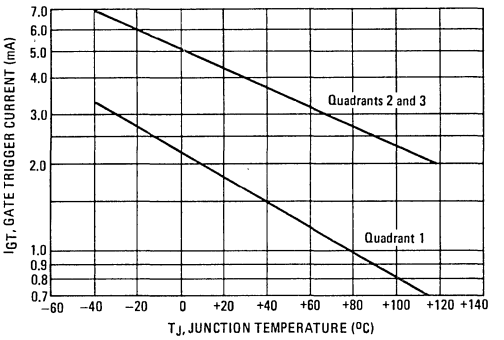


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FIGURE 3 – AVERAGE CURRENT DERATING
(REFERENCE: CASE TEMPERATURE)

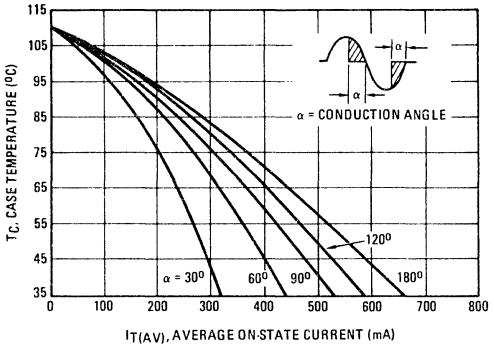

FIGURE 4 – RMS CURRENT DERATING
(REFERENCE: CASE TEMPERATURE)

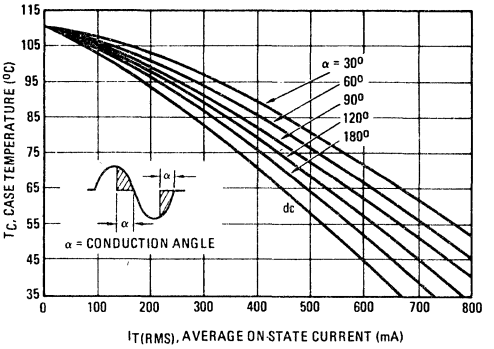

FIGURE 5 – AVERAGE CURRENT DERATING
(REFERENCE: AMBIENT TEMPERATURE)

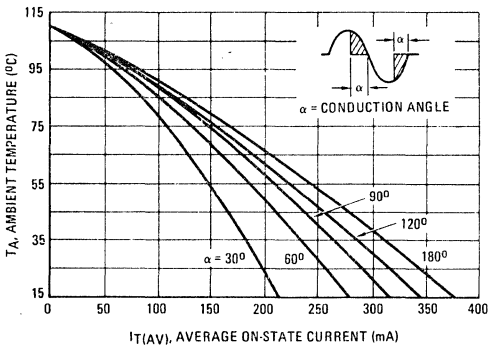

FIGURE 6 – RMS CURRENT DERATING
(REFERENCE: AMBIENT TEMPERATURE)

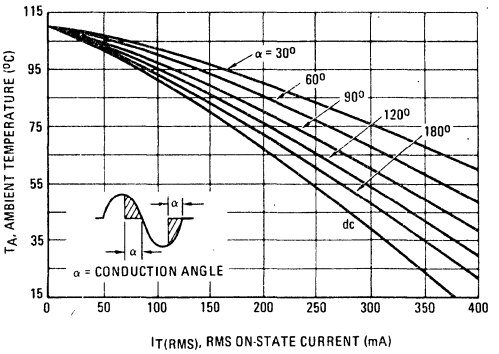

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FIGURE 7 – ON-STATE POWER DISSIPATION

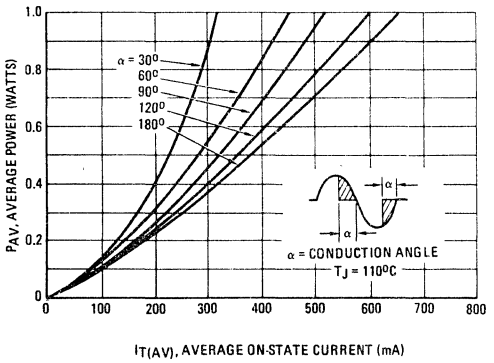


FIGURE 8 – ON-STATE POWER DISSIPATION

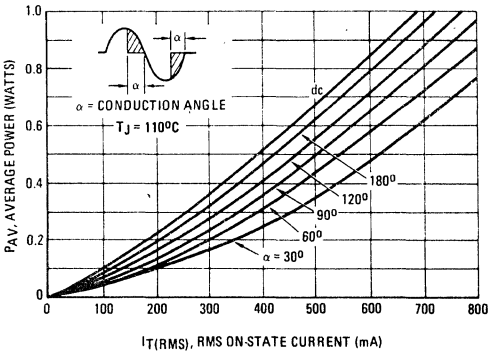


FIGURE 9 – ON-STATE CHARACTERISTICS

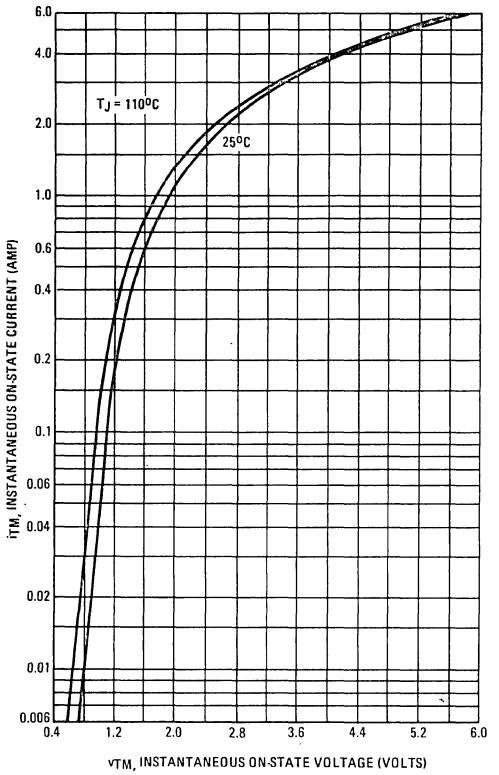


FIGURE 10 – TYPICAL HOLDING CURRENT

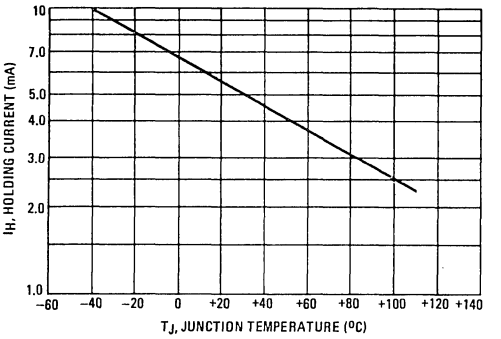


FIGURE 11 – MAXIMUM ALLOWABLE SURGE CURRENT

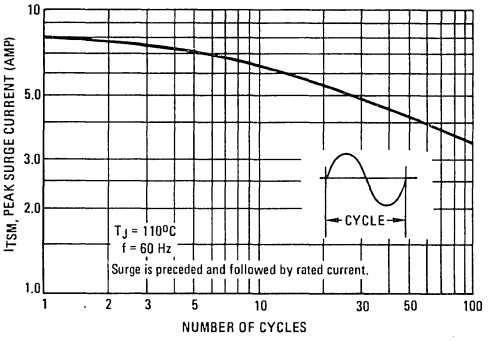
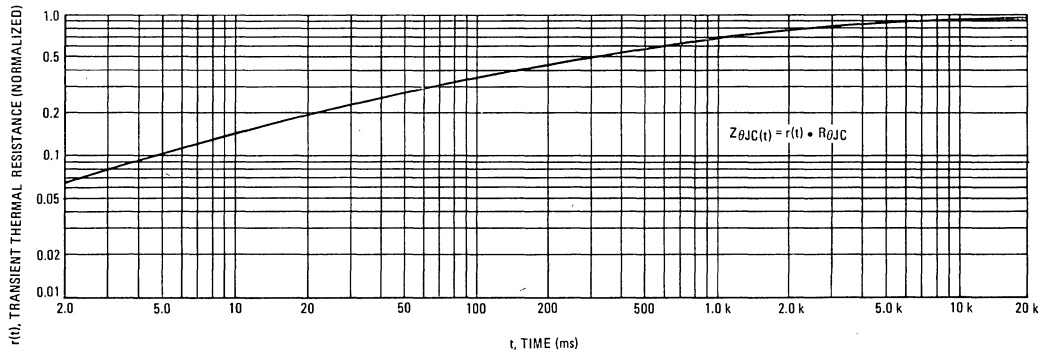


FIGURE 12 – THERMAL RESPONSE



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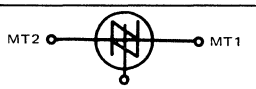
MBS4991
MBS4992

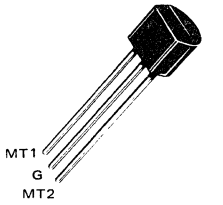


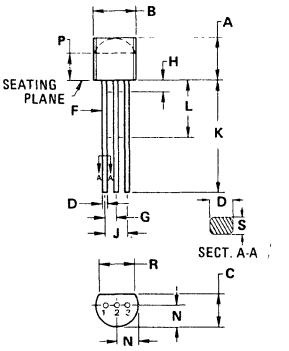
BIDIRECTIONAL DIODE THYRISTORS

. . . designed for full-wave triggering in Triac phase control circuits, half-wave SCR triggering application and as voltage level detectors. Supplied in an inexpensive plastic TO-92 package for high-volume requirements, this low-cost plastic package is readily adaptable for use in automatic insertion equipment.

- Low Switching Voltage – 8.0 Volts Typical
- Uniform Characteristics in Each Direction
- Low On-State Voltage – 1.7 Volts Maximum
- Low Off-State Current – 0.1 μA Maximum
- Low Temperature Coefficient – 0.02 %/°C Typical

SILICON BIDIRECTIONAL SWITCH (PLASTIC)





STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02
TO-92
PLASTIC

7

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Dissipation	P_D	500	mW
DC Forward Current	I_F	200	mA
DC Gate Current (off-state only)	$I_{G(off)}$	5.0	mA
Repetitive Peak Forward Current (1.0% Duty Cycle, 10 μs Pulse Width, T_A = 100°C)	$I_{FM(rep)}$	2.0	Amp
Non-Repetitive Forward Current 10 μs Pulse Width, T_A = 25°C	$I_{FM(nonrep)}$	6.0	Amp
Operating Junction Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Switching Voltage		V_S				Vdc
	MBS4991		6.0	8.0	10	
	MBS4992		7.5	8.0	9.0	
Switching Current		I_S				μAdc
	MBS4991		–	175	500	
	MBS4992		–	90	120	
Switching Voltage Differential		$\lvert V_{S1}-V_{S2}\rvert$				Vdc
	MBS4991		–	0.3	0.5	
	MBS4992		–	0.1	0.2	
Gate Trigger Current		I_{GF}				μAdc
(V_F = 5.0 Vdc R_L = 1.0 K ohm)	MBS4992		–	–	100	
Holding Current		I_H				mAdc
	MBS4991		–	0.7	1.5	
	MBS4992		–	0.2	0.5	
Off-State Blocking Current		I_B				μAdc
(V_F = 5.0 Vdc, T_A = 25°C)	MBS4991		–	0.08	1.0	
(V_F = 5.0 Vdc, T_A = 85°C)	MBS4991		–	2.0	10	
(V_F = 5.0 Vdc, T_A = 25°C)	MBS4992		–	0.08	0.1	
(V_F = 5.0 Vdc, T_A = 100°C)	MBS4992		–	6.0	10	
Forward On-State Voltage		V_F				Vdc
(I_F = 175 mAdc)	MBS4991		–	1.4	1.7	
(I_F = 200 mAdc)	MBS4992		–	1.5	1.7	
Peak Output Voltage (C_c = 0.1 μF, R_L = 20 ohms, (Figure 7)		V_o	3.5	4.8	–	Vdc
Turn-On Time (Figure 8)		t_{on}	–	1.0	–	μs
Turn-Off Time (Figure 9)		t_{off}	–	30	–	μs
Temperature Coefficient of Switching Voltage (-50 to +125°C)		T_C	–	+0.02	–	%/°C

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – SWITCHING VOLTAGE versus TEMPERATURE

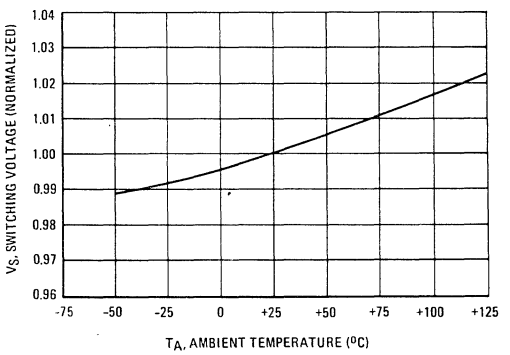


FIGURE 2 – SWITCHING CURRENT versus TEMPERATURE

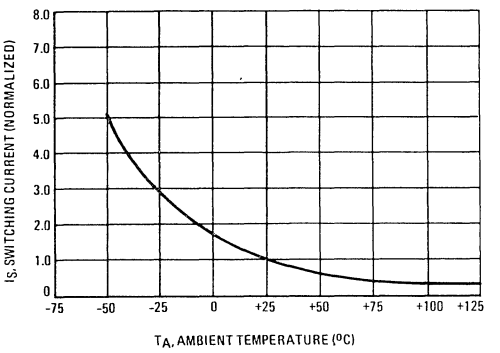


FIGURE 3 – HOLDING CURRENT versus TEMPERATURE

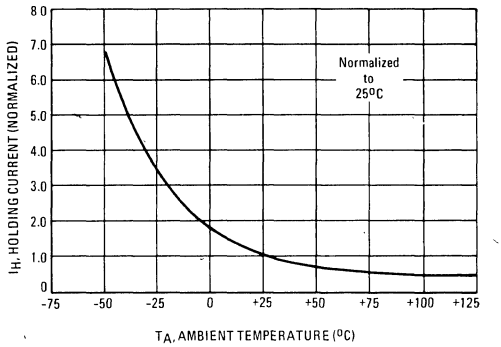


FIGURE 4 – OFF-STATE BLOCKING CURRENT versus TEMPERATURE

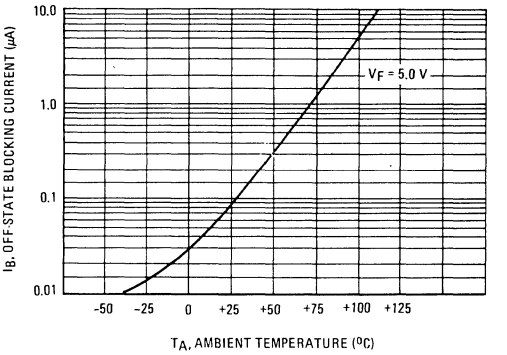


FIGURE 5 – ON-STATE VOLTAGE versus FORWARD CURRENT

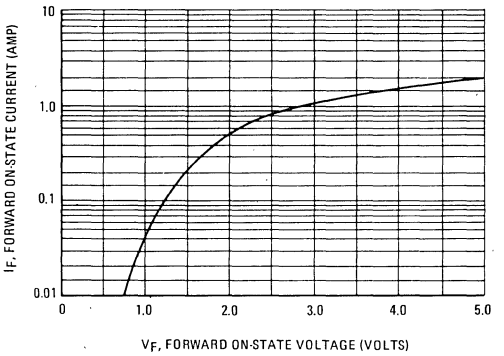


FIGURE 6 – PEAK OUTPUT VOLTAGE (FUNCTION OF R_L AND C_c)

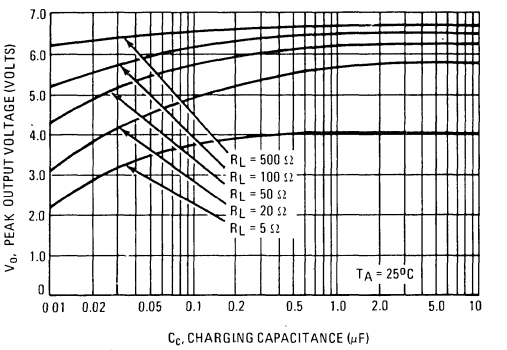


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FIGURE 7 – PEAK OUTPUT VOLTAGE TEST CIRCUIT

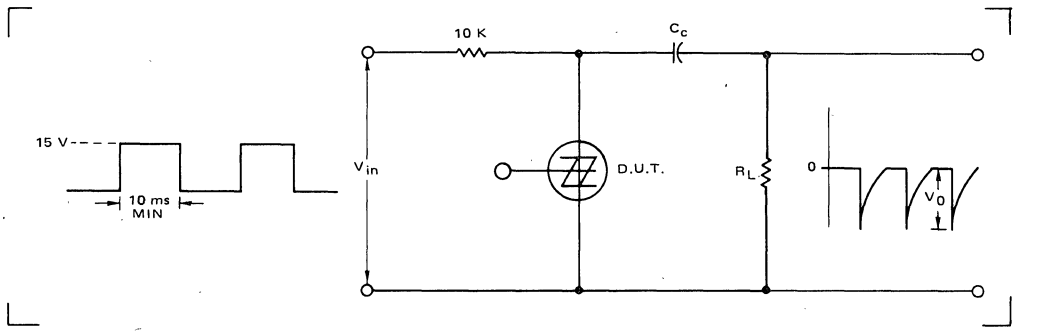
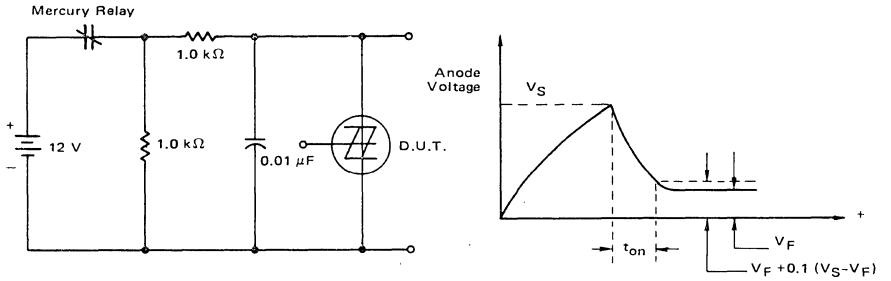
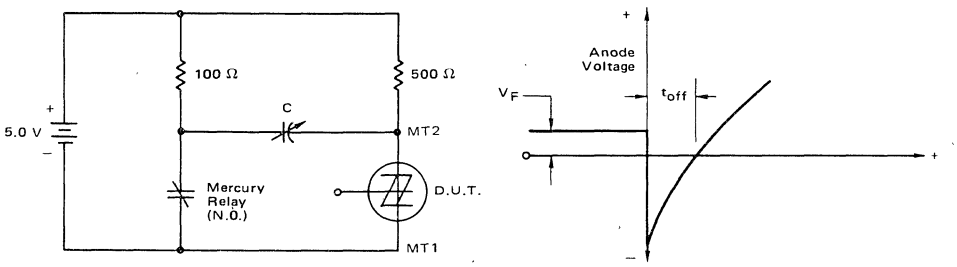


FIGURE 8 – TURN-ON TIME TEST CIRCUIT



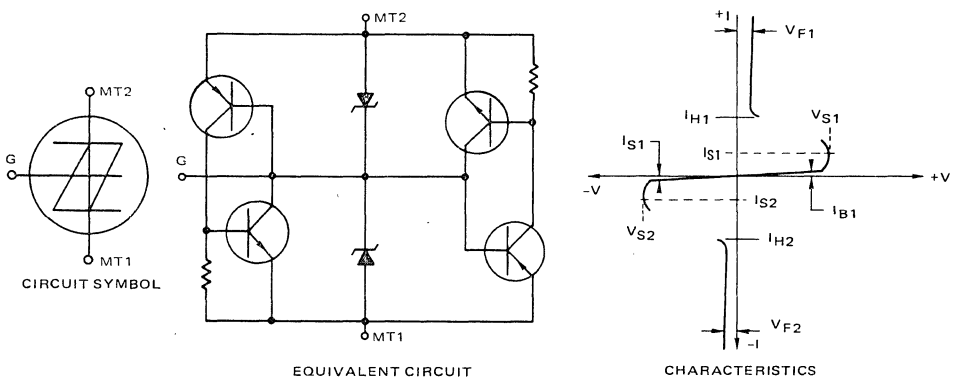
Turn-on time is measured from the time V_S is achieved to the time when the anode voltage drops to within 90% of the difference between V_S and V_F.

FIGURE 9 – TURN-OFF TIME TEST CIRCUIT



With the SBS in conduction and the relay contacts open, close the contacts to cause anode A2 to be driven negative. Decrease C until the SBS just remains off when anode A2 becomes positive. The turn-off time, t_{off}, is the time from initial contact closure and until anode A2 voltage reaches zero volts.

FIGURE 10 – DEVICE EQUIVALENT CIRCUIT, CHARACTERISTICS AND SYMBOLS



MCR63-1 thru 10
MCR64-1 thru 10
MCR65-1 thru 10

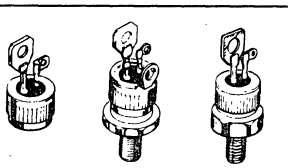
REVERSE BLOCKING TRIODE THYRISTOR

. . . designed for industrial and consumer applications such as power supplies; battery chargers; temperature, motor, light, and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current – I_{TSM} = 550 Amp
- Rugged Construction in Either Pressfit, Stud, or Isolated Stud
- Glass Passivated Junctions for Maximum Reliability

SILICON CONTROLLED RECTIFIER

55 AMPERES RMS
25–800 VOLTS



CASE 310-01 MCR63 series | **CASE 311-01** MCR65 series | **CASE 263-03** MCR64 series

MAXIMUM RATINGS

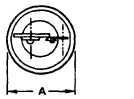
Rating		Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage		V_{DRM}(1) or V_{RRM}		Volts
MCR63, MCR64, MCR65	-1		25	
	-2		50	
	-3		100	
	-4		200	
	-5		300	
	-6		400	
	-7		500	
	-8		600	
	-9		700	
	-10		800	
Non-Repetitive Peak Reverse Blocking Voltage ($t \leq 5.0$ ms)		V_{RSM}		Volts
MCR63, MCR64, MCR65	-1		35	
	-2		75	
	-3		150	
	-4		300	
	-5		400	
	-6		500	
	-7		600	
	-8		700	
	-9		800	
	-10		900	
Forward Current RMS		$I_{T(RMS)}$	55	Amp
Peak Surge Current (One cycle, 60 Hz) (T_J = -40 to +125°C)		I_{TSM}	550	Amp
Circuit Fusing Considerations (T_J = -40 to +125°C)(t = 1.0 to 8.3 ms)		I^2t	1255	A^2s
Peak Gate Power		P_{GFM}	20	Watts
Average Gate Power (Pulse Width $\leq$ 2 μs)		$P_{GF(AV)}$	0.5	Watt
Peak Forward Gate Current		I_{GFM}	2.0	Amp
Peak Gate Voltage – Forward		V_{GFM}	10	Volts
Reverse		V_{GRM}	10	
Operating Junction Temperature Range		T_J	-40 to +125	°C
Storage Temperature Range		T_{stg}	-40 to +150	°C
Stud Torque		–	30	in. lb.

THERMAL CHARACTERISTICS

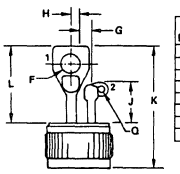
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
Pressfit and Stud		1.0	
Isolated Stud		1.1	

(1) V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode.

MCR63 series



STYLE 1
1. CATHODE
2. GATE
CASE. ANODE

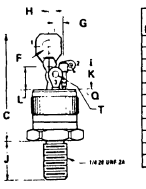


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.52	1.78	0.060	0.070
J	7.62	8.89	0.300	0.350
K	–	26.67	–	1.050
L	–	17.02	–	0.670
Q	1.40	2.16	0.055	0.085

CASE 310-01

MCR65 series

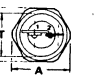
STYLE 1:
1. CATHODE
2. GATE
3. ANODE



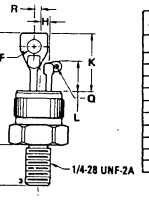
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	32.51	–	1.280
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.60	2.01	0.063	0.079
J	10.67	11.56	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6.48	6.99	0.255	0.275
Q	1.40	2.16	0.055	0.085
T	3.43	3.81	0.135	0.150

CASE 311-01

MCR64 series



STYLE 1:
PIN 1. CATHODE
2. GATE
3. ANODE



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

CASE 263-03

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Peak Forward Blocking Current (V_D = Rated V_{DRM}, with gate open, T_J = 125°C)		I_{DRM}	–	2.0	mA
Peak Reverse Blocking Current (V_R = Rated V_{RRM}, with gate open, T_J = 125°C)		I_{RRM}	–	2.0	mA
Forward "On" Voltage (I_{TM} = 175 A Peak)		V_{TM}	–	2.0	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 50 Ω)	T_C = 25°C T_C = -40°C	I_{GT}	 –	 40	mA
			–	75	
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 50 Ω)	T_C = 25°C T_C = -40°C	V_{GT}	 –	 3.0	Volts
			–	3.5	
(V_D = Rated V_{DRM}, R_L = 1.0 kΩ, T_J = 125°C)			0.2	–	
Holding Current (V_D = 12 V, R_L = 50 Ω, Gate Open)		I_H	–	60	mA
Forward Voltage Application Rate (T_J = 125°C, V_D = Rated V_{DRM})		dv/dt	50	–	V/μs

FIGURE 1 – AVERAGE CURRENT DERATING

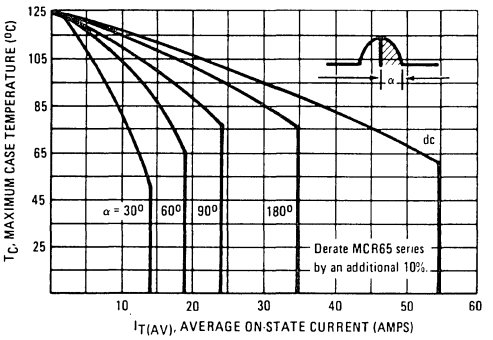
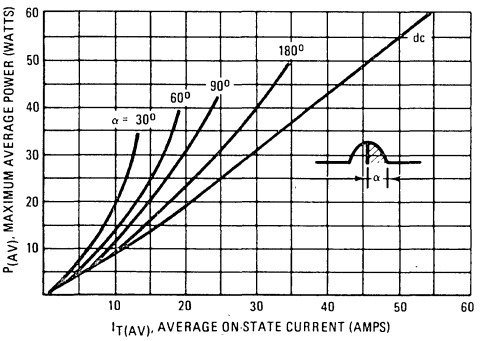
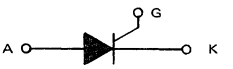


FIGURE 2 – POWER DISSIPATION



7

MCR100 series



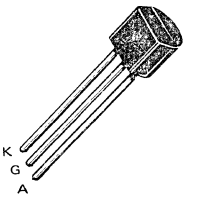
REVERSE BLOCKING TRIODE THYRISTORS

PNPN devices designed for high volume, line-powered consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-92 package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Trigger Current – 200 μA Maximum
- Low Reverse and Forward Blocking Current – 100 μA Maximum, T_C = 125°C
- Low Holding Current – 5.0 mA Maximum
- Glass-Passivated Surface for Reliability and Uniformity
- Also Available with TO-5 or TO-18 Lead Form

PLASTIC SILICON CONTROLLED RECTIFIERS

0.8 AMPERE RMS
100 to 600 VOLTS

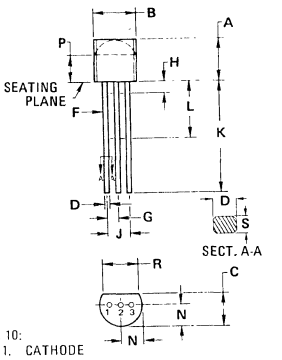


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage MCR100-3 MCR100-4 MCR100-5 MCR100-6 MCR100-7 MCR100-8	V_{RRM}	 100 200 300 400 500 600	Volts
Forward Current RMS (See Figures 1 & 2) (All Conduction Angles)	$I_{T(RMS)}$	0.8	Amp
Peak Forward Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	10	Amp
Circuit Fusing Considerations, T_A = 25°C (t = 1.0 to 8.3 ms)	I^2t	0.415	A^2s
Peak Gate Power – Forward, T_A = 25°C	P_{GM}	0.1	Watt
Average Gate Power – Forward, T_A = 25°C	$P_{GF(AV)}$	0.01	Watt
Peak Gate Current – Forward, T_A = 25°C (300 μs, 120 PPS)	I_{GFM}	1.0	Amp
Peak Gate Voltage – Reverse	V_{GRM}	5.0	Volts
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C
Lead Solder Temperature (<1/16" from case, 10 s max)	–	+230	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W



STYLE 10:
PIN 1. CATHODE
2 GATE
3. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.
CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (R_{GK} = 1000 Ohms)

Characteristic		Symbol	Min	Max	Unit
Peak Forward Blocking Voltage (T_C = 125°C)		V_{DRM}			Volts
	MCR100-3		100		
	MCR100-4		200		
	MCR100-5		300		
	MCR100-6		400		
	MCR100-7		500		
	MCR100-8		600		
Peak Forward Blocking Current (Rated V_{DRM} @ T_C = 125°C)		I_{DRM}	–	100	μA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_C = 125°C)		I_{RRM}	–	100	μA
Forward "On" Voltage (Note 1) (I_{TM} = 1.0 A peak @ T_A = 25°C)		V_{TM}	–	1.7	Volts
Gate Trigger Current (Continuous dc) (Note 2) (Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = 25°C	I_{GT}	–	200	μA
Gate Trigger Voltage (Continuous dc)	T_C = 25°C	V_{GT}	–	0.8	Volts
(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = -40°C		–	1.2	
(Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms)	T_C = 125°C		0.1	–	
Holding Current	T_C = 25°C	I_H	–	5.0	mA
(Anode Voltage = 7.0 Vdc, initiating current = 20 mA)	T_C = -40°C		–	10	

NOTE:
1. Forward current applied for 1.0 ms maximum duration, duty cycle ≤ 1.0%.
2. R_{GK} current is not included in measurement.

FIGURE 1 – CURRENT DERATING
(REFERENCE: CASE TEMPERATURE)

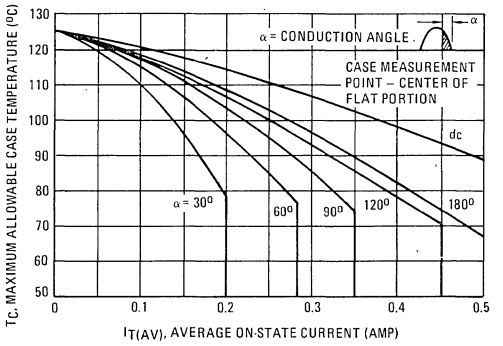
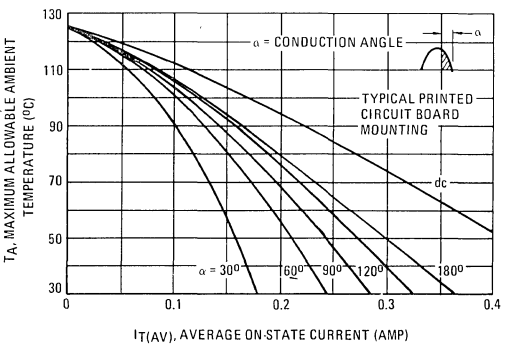
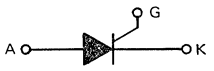


FIGURE 2 – CURRENT DERATING
(REFERENCE: AMBIENT TEMPERATURE)



MCR101 thru MCR104



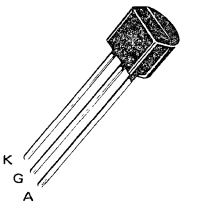
REVERSE BLOCKING TRIODE THYRISTOR

. . . Annular◆ PNPN devices designed for low cost, high volume consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-92 package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Trigger Current – 200 μA Maximum
- Low Reverse and Forward Blocking Current – 100 μA Maximum, T_C = 85°C
- Low Holding Current – 5.0 mA Maximum
- Passivated Surface for Reliability and Uniformity
- Also available with TO-5 or TO-18 Lead Form

SILICON CONTROLLED RECTIFIERS

0.8 AMPERE RMS
15 thru 100 VOLTS



MAXIMUM RATINGS(1)

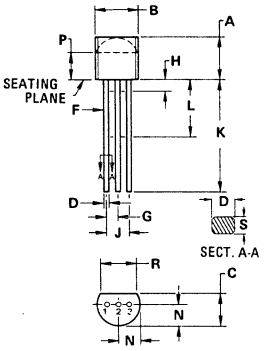
Rating		Symbol	Value	Unit
Peak Reverse Blocking Voltage (R_{GK} = 1000 ohms, T_C = +85°C)	MCR101	V_{RRM}	15	Volts
	MCR102		30	
	MCR103		60	
	MCR104		100	
Forward Current RMS (See Figures 1 & 2) (All Conduction Angles)		$I_{T(RMS)}$	0.8	Amp
Peak Forward Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)		I_{TSM}	10	Amp
Circuit Fusing Considerations, T_A = 25°C (t = 1.0 to 8.3 ms)		I^2t	0.415	A^2s
Peak Gate Power – Forward, T_A = 25°C		P_{GM}	0.1	Watt
Average Gate Power – Forward, T_A = 25°C		$P_{G(AV)}$	0.01	Watt
Peak Gate Current – Forward, T_A = 25°C (300 μs, 120 PPS)		I_{GM}	1.0	Amp
Peak Gate Voltage – Reverse		V_{GM}	4.0	Volts
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}		T_J	-65 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C
Lead Solder Temperature (<1/16" from case, 10 s max)		–	+230	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R\theta_{JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R\theta_{JA}$	200	°C/W

◆Annular Semiconductor Patented by Motorola Inc.

(1) Temperature reference point for all case temperature is center of flat portion of package. (T_C = +85°C unless otherwise noted.)



STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.
CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (R_{GK} = 1000 Ohms)

Characteristic		Symbol	Min	Max	Unit
Peak Forward Blocking Voltage (Note 1) (T_C = 85°C)	MCR101	V_{DRM}	15	–	Volts
	MCR102		30	–	
	MCR103		60	–	
	MCR104		100	–	
Peak Forward Blocking Current (Rated V_{DRM} @ T_C = 85°C)		I_{DRM}	–	100	μA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_C = 85°C)		I_{RRM}	–	100	μA
Forward "On" Voltage (Note 2) (I_{TM} = 1.0 A peak @ T_A = 25°C)		V_{TM}	–	1.7	Volts
Gate Trigger Current (Continuous dc) (Note 3) (Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = 25°C	I_{GT}	–	200	μA
Gate Trigger Voltage (Continuous dc) (Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = 25°C	V_{GT}	–	0.8	Volts
	T_C = -65°C		–	1.2	
	T_C = 85°C	V_{GD}	0.1	–	
Holding Current (Anode Voltage = 7.0 Vdc, initiating current = 20 mA)	T_C = 25°C	I_H	–	5.0	mA
	T_C = -65°C		–	10	

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.
2. Forward current applied for 1.0 ms maximum duration, duty cycle ≤ 1.0%.
3. R_{GK} current is not included in measurement.

7

FIGURE 1 – CURRENT DERATING
(REFERENCE: CASE TEMPERATURE)

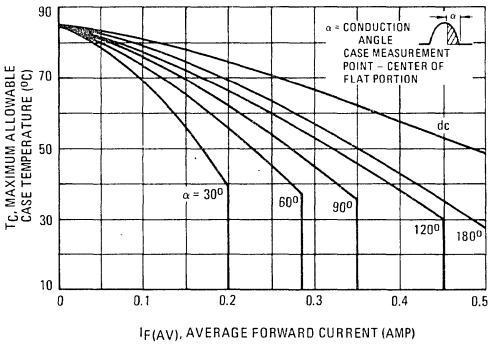
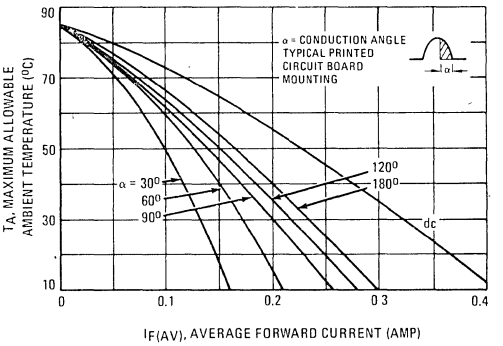


FIGURE 2 – CURRENT DERATING
(REFERENCE: AMBIENT TEMPERATURE)



MCR106-1 thru MCR106-8

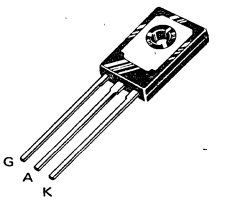
REVERSE BLOCKING TRIODE THYRISTORS

. . . PNPN devices designed for high volume consumer applications such as temperature, light, and speed control; process and remote control, and warning systems where reliability of operation is important.

- Glass-Passivated Surface for Reliability and Uniformity
- Power Rated at Economical Prices
- Practical Level Triggering and Holding Characteristics
- Flat, Rugged, Thermopad▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability.

SILICON CONTROLLED RECTIFIERS

4.0 AMPERES RMS
30 thru 600 VOLTS



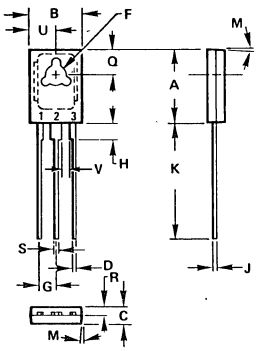
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage (Note 1) MCR106-1	V_{RRM}	30	Volts
-2		60	
-3		100	
-4		200	
-5		300	
-6		400	
-7		500	
-8		600	
RMS Forward Current (All Conduction Angles)	$I_{T(RMS)}$	4.0	Amp
Average Forward Current $T_C = 93^oC$	$I_{T(AV)}$	2.55	Amp
$T_A = 30^oC$		0.68	
Peak Non-Repetitive Surge Current (1/2 cycle, 60 Hz, $T_J = -40$ to $+110^oC$)	I_{TSM}	25	Amp
Circuit Fusing Considerations ($T_J = -40$ to $+110^oC$, t = 1.0 to 8.3 ms)	I^2t	2.6	A^2s
Peak Gate Power	P_{GM}	0.5	Watt
Average Gate Power	$P_{G(AV)}$	0.1	Watt
Peak Forward Gate Current	I_{GM}	0.2	Amp
Peak Reverse Gate Voltage	V_{RGM}	6.0	Volts
Operating Junction Temperature Range	T_J	-40 to +110	^oC
Storage Temperature Range	T_{stg}	-40 to +150	^oC
Mounting Torque (Note 2)	—	6.0	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.0	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	$^oC/W$

▲Trademark of Motorola Inc.



STYLE 2
PIN 1. CATHODE
2. ANODE
3. GATE

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	—	0.040	—

CASE 77-04

ELECTRICAL CHARACTERISTICS (T_C = 25°C and R_{GK} = 1000 ohms unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Voltage (T_J = 110°C, Note 1)	MCR106-1	V_{DRM}	30	–	–	Volts
	-2		60	–	–	
	-3		100	–	–	
	-4		200	–	–	
	-5		300	–	–	
	-6		400	–	–	
	-7		500			
	-8		600			
Peak Forward Blocking Current (Rated V_{DRM}, T_J = 110°C)		I_{DRM}	–	–	200	μA
Peak Reverse Blocking Current (Rated V_{RRM}, T_J = 110°C)		I_{RRM}	–	–	200	μA
Forward "On" Voltage (I_{TM} = 4.0 A Peak)		V_{TM}	–	–	2.0	Volts
Gate Trigger Current (Continuous dc) Note 3		I_{GT}				μA
(V_{AK} = 7.0 Vdc, R_L = 100 ohms)			–	–	200	
(V_{AK} = 7.0 Vdc, R_L = 100 ohms, T_C = -40°C)			–	–	500	
Gate Trigger Voltage (Continuous dc) (V_{AK} = 7.0 Vdc, R_L = 100 ohms, T_C = 25°C)		V_{GT}	–	–	1.0	Volts
Gate Non-Trigger Voltage (V_{AK} = Rated V_{DRM}, R_L = 100 ohms, T_J = 110°C)		V_{GD}	0.2	–	–	Volts
Holding Current (V_{AK} = 7.0 Vdc, T_C = 25°C)		I_H	–	–	5.0	mA
Forward Voltage Application Rate (T_J = 110°C)		dv/dt	–	10	–	V/μs

NOTES:

1. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.
2. Torque rating applies with use of torque washer (Shakeproof WD19523 or equivalent). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Anode lead and heatsink contact pad are common. (See AN-290 B)
   For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +225°C. For optimum results, an activated flux (oxide removing) is recommended.
3. R_{GK} current is not included in measurement.

CURRENT DERATING

FIGURE 1 – MAXIMUM CASE TEMPERATURE

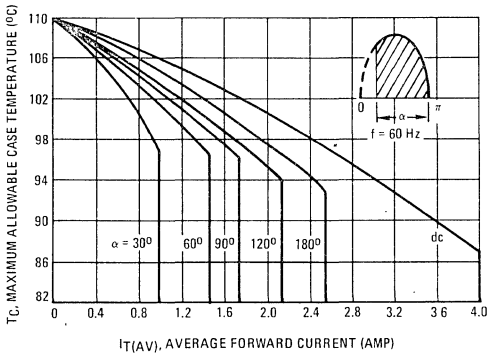
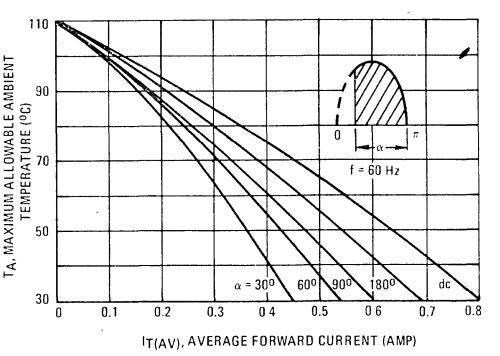
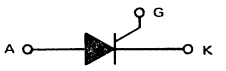


FIGURE 2 – MAXIMUM AMBIENT TEMPERATURE



MCR115
MCR120



REVERSE BLOCKING TRIODE THYRISTORS

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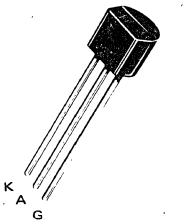
- Sensitive Gate Trigger Current – 200 μA Maximum
- Low Reverse and Forward Blocking Current – 100 μA Maximum, T_C = 110°C
- Low Holding Current – 5.0 mA Maximum
- Passivated Surface for Reliability and Uniformity
- Also Available with TO-5 or TO-18 Lead Form

PLASTIC SILICON CONTROLLED RECTIFIERS

0.8 AMPERE RMS
100 and 200 VOLTS

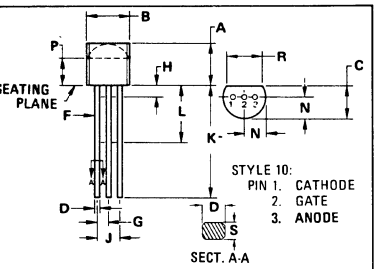


MAXIMUM RATINGS(1)

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage MCR115 MCR120	V_{RRM}	 150 200	Volts
Forward Current RMS (See Figures 1 & 2) (All Conduction Angles)	$I_{T(RMS)}$	0.8	Amp
Peak Forward Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	10	Amp
Circuit Fusing Considerations, T_A = 25°C (t = 1.0 to 8.3 ms)	I^2t	0.415	A^2s
Peak Gate Power – Forward, T_A = 25°C	P_{GM}	0.1	Watt
Average Gate Power – Forward, T_A = 25°C	$P_{GF(AV)}$	0.01	Watt
Peak Gate Current – Forward, T_A = 25°C (300 μs, 120 PPS)	I_{GFM}	1.0	Amp
Peak Gate Voltage – Reverse	V_{GRM}	5.0	Volts
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	-65 to +110	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Solder Temperature (<1/16" from case, 10 s max)	–	+230	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.
CASE 29-02
TO-92

♦Annular Semiconductor Patented by Motorola Inc.
(1) Temperature reference point for all case temperatures in center of flat portion of package. (T_C = +110°C unless otherwise noted.)

ELECTRICAL CHARACTERISTICS (R_{GK} = 1000 Ohms)

Characteristic		Symbol	Min	Max	Unit
Peak Forward Blocking Voltage (Note 1)		V_{DRM}			Volts
(T_C = 110°C)	MCR115		150	–	
	MCR120		200	–	
Peak Forward Blocking Current (Rated V_{DRM} @ T_C = 110°C)		I_{DRM}	–	100	μA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_C = 110°C)		I_{RRM}	–	100	μA
Forward "On" Voltage (Note 2) (I_{TM} = 1.0 A peak @ T_A = 25°C)		V_{TM}	–	1.7	Volts
Gate Trigger Current (Continuous dc) (Note 3) (Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = 25°C	I_{GT}	–	200	μA
Gate Trigger Voltage (Continuous dc)	T_C = 25°C	V_{GT}	–	0.8	Volts
(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = -65°C		–	1.2	
(Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms)	T_C = 110°C	V_{GD}	0.1	–	
Holding Current	T_C = 25°C	I_H	–	5.0	mA
(Anode Voltage = 7.0 Vdc, initiating current = 20 mA)	T_C = -65°C		–	10	

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.
2. Forward current applied for 1.0 ms maximum duration, duty cycle ≤ 1.0%.
3. R_{GK} current is not included in measurement.

7

FIGURE 1 – CURRENT DERATING
(REFERENCE: CASE TEMPERATURE)

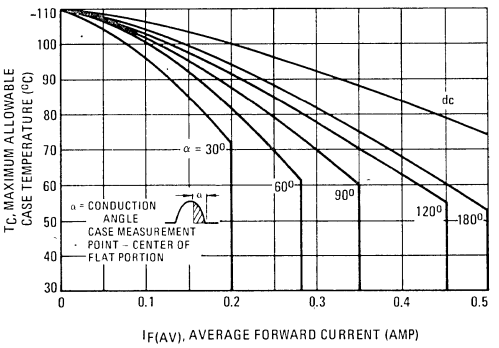
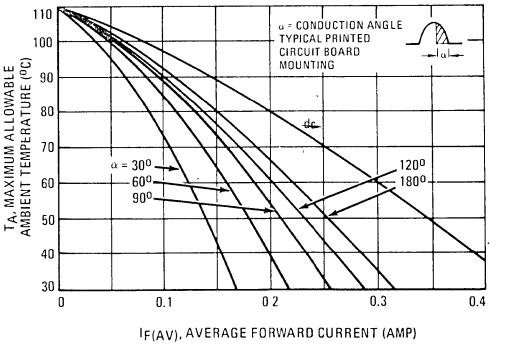
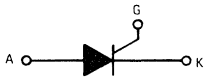


FIGURE 2 – CURRENT DERATING
(REFERENCE: AMBIENT TEMPERATURE)



MCR201 thru MCR206



SILICON CONTROLLED RECTIFIERS

0.5 AMPERE RMS
15–200 VOLTS

REVERSE BLOCKING TRIODE THYRISTORS

. . . Annular♦ PNPN devices designed for industrial/military applications such as relay and lamp drivers, small motor controllers and drivers for larger thyristors, and in sensing and detection circuits.

- Sensitive Gate Trigger Current – 200 μA Maximum
- Low Reverse and Forward Blocking Current – 100 μA Maximum, T_C = 125°C
- Low Holding Current – 5.0 mA Maximum
- Passivated Surface for Reliability and Uniformity
- TO-18 Hermetically Sealed Metal Package

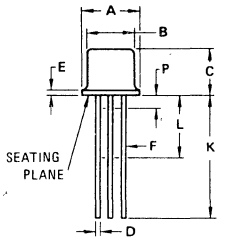
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Off-State and Reverse Voltage	V_{DRM}		Volts
MCR201	V_{RRM}	15	
MCR202		30	
MCR203		60	
MCR204		100	
MCR205		150	
MCR206		200	
RMS On-State Current (All Conduction Angles) (See Figs. 4 & 5)	$I_{T(RMS)}$	0.5	Amp
Peak Non-Repetitive Forward Surge Current (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	6.0	Amp
Circuit Fusing Considerations, (t = 1.0 to 8.3 ms)	I^2t	0.15	A^2s
Peak Forward Gate Power	P_{GM}	0.1	Watt
Average Forward Gate Power	$P_{GF(AV)}$	0.01	Watt
Peak Forward Gate Current (300 μs, 120 PPS)	I_{GFM}	1.0	Amp
Peak Reverse Gate Voltage	V_{GRM}	4.0	Volts
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	150	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	400	°C/W

♦Annular Semiconductor Patented by Motorola Inc.



STYLE 6:
PIN 1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.406	0.533	0.016	0.021
E	–	0.762	–	0.030
F	0.406	0.483	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

All JEDEC notes and dimensions apply.

CASE 22-03
(TO-18)

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ELECTRICAL CHARACTERISTICS (R_{GK} = 1000 Ohms)

Characteristic		Symbol	Min	Max	Unit
Peak Forward Blocking Current (Rated V_{DRM} @ T_C = 125°C)		I_{DRM}	–	100	μA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_C = 125°C)		I_{RRM}	–	100	μA
Peak On-State Voltage (I_{TM} = 1.2 A peak, ImS, Duty Cycle ≤ 1%)		V_{TM}	–	1.7	Volts
Gate Trigger Current (Continuous dc) (Note 1)	T_C = 25°C	I_{GT}	–	200	μA
(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = -65°C		–	350	
Gate Trigger Voltage (Continuous dc)	T_C = 25°C	V_{GT}	–	0.8	Volts
(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = -65°C		–	1.2	
	T_C = 125°C		0.1	–	
Holding Current	T_C = 25°C	I_H	–	5.0	mA
(Anode Voltage = 7.0 Vdc, initiating current = 20 mA)	T_C = -65°C		–	10	

1. R_{GK} current is not included in measurement.

FIGURE 1 – CURRENT DERATING
(REFERENCE: CASE TEMPERATURE)

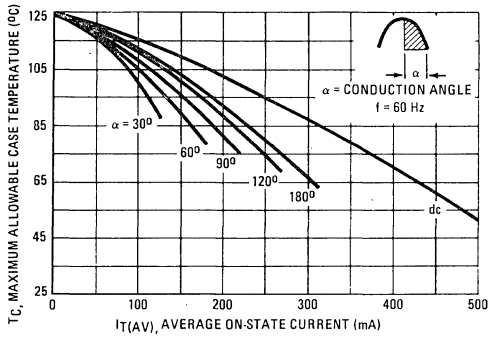

FIGURE 2 – POWER DISSIPATION

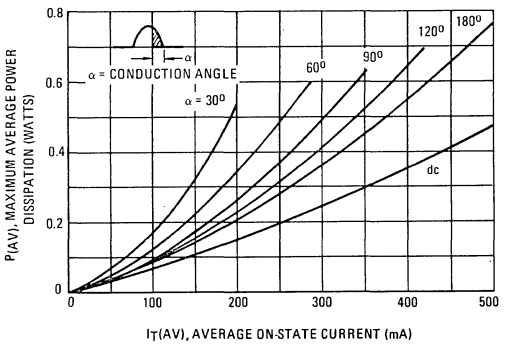

FIGURE 3 – FORWARD VOLTAGE

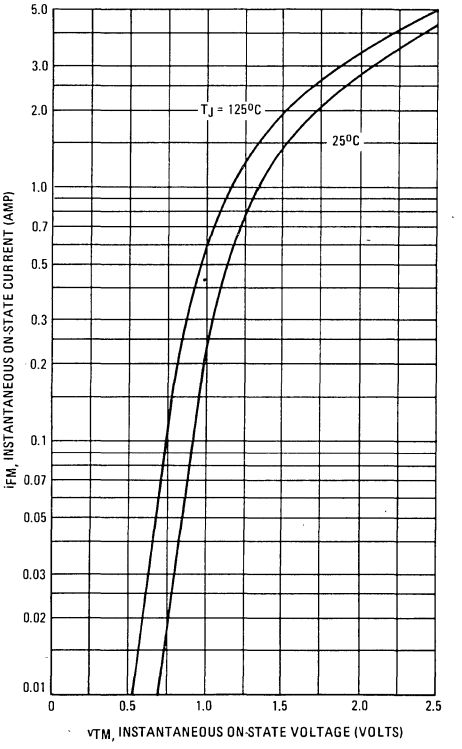

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FIGURE 4 – SURGE RATINGS

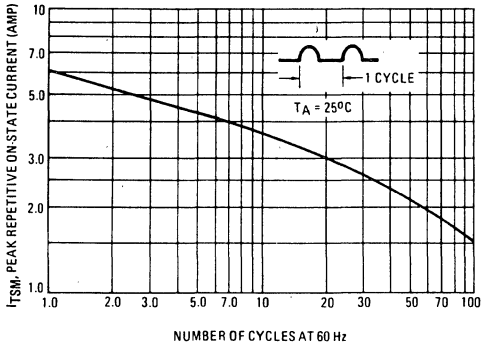


FIGURE 5 – CURRENT DERATING
(REFERENCE: AMBIENT TEMPERATURE)

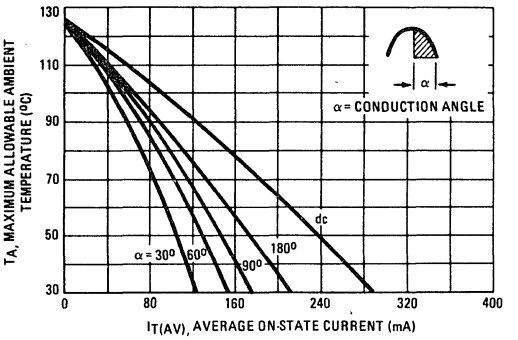
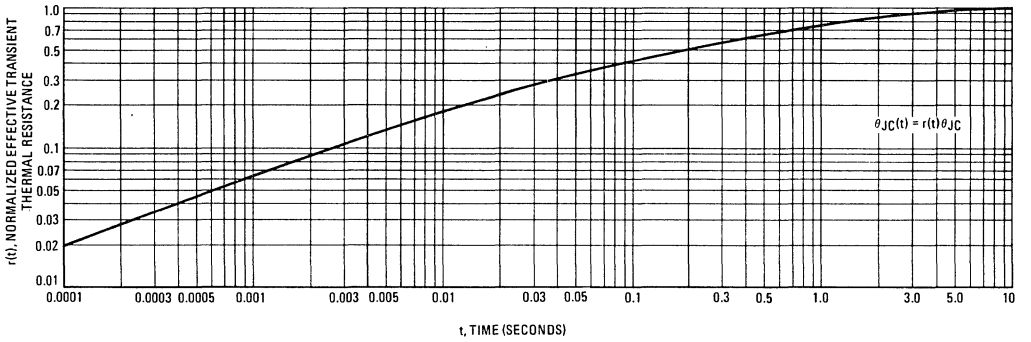


FIGURE 6 – THERMAL RESPONSE



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TYPICAL CHARACTERISTICS

FIGURE 7 – GATE TRIGGER VOLTAGE

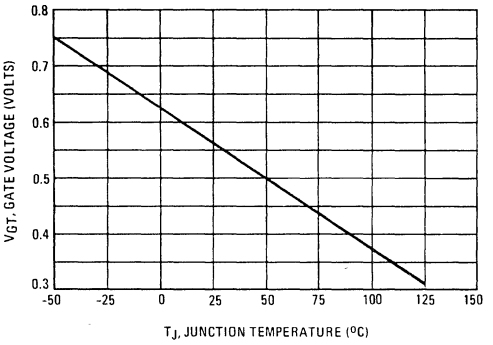


FIGURE 8 – GATE TRIGGER CURRENT

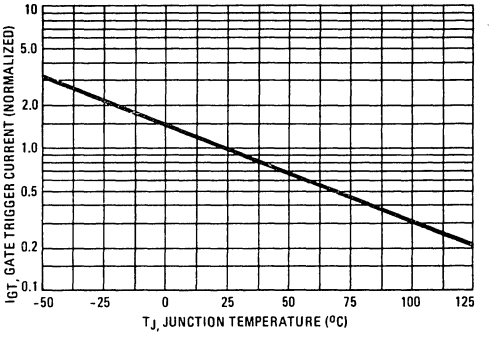
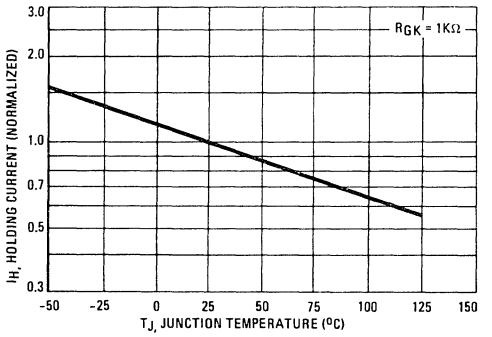
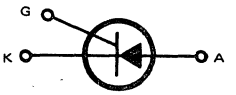


FIGURE 9 – HOLDING CURRENT



MCR729-5 thru MCR729-10



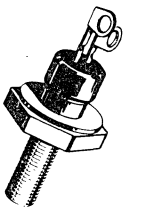
REVERSE BLOCKING TRIODE THYRISTOR

. . . fast switching, high-voltage Silicon Controlled Rectifiers especially designed for pulse modulator applications in radar and other similar equipment.

- High-Voltage: V_{DRM} = 300 to 800 Volts
- Turn-On Times: in Nanosecond Range
- Repetitive Pulse Current to 100 Amps
- Stable Switching Characteristics Over an Operating Temperature Range From -65 to +105°C
- Pulse Repetition Rates as High as 10,000 pps

SILICON CONTROLLED RECTIFIERS

5 AMPERES RMS
300–800 VOLTS

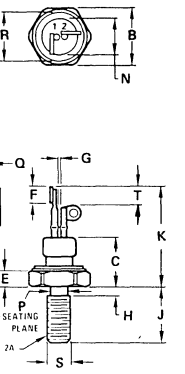


MAXIMUM RATINGS (T_J = 105°C unless otherwise noted)

Characteristic	Symbol	Value	Unit
Peak Repetitive Forward Blocking Voltage*(1)	V_{DRM}		Volts
MCR729-5		300	
-6		400	
-7		500	
-8		600	
-9		700	
-10		800	
Peak Repetitive Reverse Blocking Voltage (1)	V_{RRM}	50	Volts
Forward Current RMS	$I_{T(RMS)}$	5	Amps
Average Forward Power	$P_{F(AV)}$	5	Watts
Peak Repetitive On-State Control (PW = 10 μs)	I_{TRM}	100	Amps
Peak Forward Gate Power	P_{GFM}	20	Watts
Average Forward Gate Power	$P_{GF(AV)}$	1	Watt
Peak Forward Gate Current	I_{GFM}	5	Amps
Peak Forward Gate Voltage	V_{GFM}	10	Volts
Peak Reverse Gate Voltage	V_{GRM}	10	Volts
Operating Junction Temperature Range	T_J	-65 to +105	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Stud Torque		15	in/lb

*Characterized for unilateral applications where reverse blocking capability is not important. Higher V_{ROM} rated units available on request.

(1) Ratings apply for zero or negative gate voltages. Devices shall not have a positive bias to the gate concurrently with a negative potential on the anode. Devices should not be tested with a constant current source for forward and reverse blocking voltages such that the applied voltage exceeds the ratings.



STYLE 1.
PIN 1. CATHODE
2. GATE
STUD – ANODE

NOTE:
1. ALL RULES & NOTES ASSOCIATED WITH REFERENCED TO-64 OUTLINE SHALL APPLY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
B	10.77	11.10	0.424	0.437
C	7.62	10.16	0.300	0.400
E	1.52	4.45	0.060	0.175
F	2.03	3.45	0.080	0.136
G	0.33	–	0.013	–
H	–	1.98	–	0.078
J	10.16	11.51	0.400	0.453
K	17.78	21.72	0.700	0.855
N	–	10.77	–	0.424
P	4.14	4.80	0.163	0.189
Q	1.02	1.91	0.040	0.075
R	10.16	–	0.400	–
S	4.212	4.310	0.1658	0.1697
T	1.52	–	0.060	–

CASE 63-03

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (V_D = Rated V_{DRM}, T_C = 105°C, gate open)	I_{DRM}	–	0.2	2	mA
Gate Trigger Current (Continuous dc) (V_D = 7 Vdc, R_L = 100 ohms)	I_{GT}	–	10	50	mAdc
Gate Trigger Voltage (Continuous dc) (V_D = 7 Vdc, R_L = 100 ohms)	V_{GT}	–	0.8	1.5	Volts
Holding Current (V_D = 7 Vdc, gate open)	I_H	3	15	–	mA
Forward On Voltage (I_{TM} = 5A, PW ≤ 1mS, Duty Cycle ≤ 1%)	V_{TM}	–	–	2.6	Volts
Dynamic Forward On Voltage (0.5 μs after 50% pt, I_G = 200 mA, V_D = Rated V_{DRM}, $i_{F(pulse)}$ = 30 Amps)	V_{TM}	–	15	25	Volts
Turn-On Time ($t_d + t_r$) (I_G = 200 mA, V_D = Rated V_{DRM})	t_{on}				ns
(i_{TM} = 30 Amps peak)		–	200	–	
(i_{TM} = 100 Amps peak)		–	400	–	
Turn-On Time Variation (T_C = +25°C to +105°C and −65°C to +25°C, i_{TM} = 30 A)	t_{on}	–	±500	–	ns
Pulse Turn-Off Time ($i_{F(pulse)}$ = 30 Amps, $I_{reverse}$ = 0) (Inductive charging circuit)	t_{rec}	–	15	–	μs
Forward Voltage Application Rate (Linear Rate of Rise) (V_D = Rated V_{DRM}, gate open, T_C = 105°C)	dv/dt	50	–	–	V/μs
Thermal Resistance (Junction to Case)	θ_{JC}	–	–	4	°C/W

MCR1718-5 thru MCR1718-8

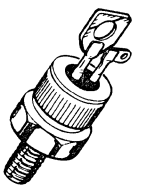
REVERSE BLOCKING TRIODE THYRISTOR

. . . fast switching, high-voltage thyristors especially designed for pulse modulator applications.

- High-Voltage Capability from 300 to 600 Volts
- Repetitive Pulse Current to 1000 Amp
- Pulse Repetition as High as 4000 pps
- Current Application Rate as High as 1000 A/μs

SILICON CONTROLLED RECTIFIER

25 AMPERES RMS
300 thru 600 VOLTS



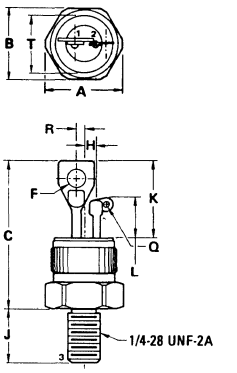
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Forward or Reverse Blocking Voltage * MCR1718-5	V_{DRM} V_{RRM}	300	Volts
-6		400	
-7		500	
-8		600	
Peak Reverse Blocking Voltage (Transient) (Non-Recurrent 5 ms (max) MCR1718-5	V_{RSM}	400	Volts
-6		500	
-7		600	
-8		700	
Forward Current RMS	$I_{T(RMS)}$	25	Amp
Peak Forward Surge Current (1-10 μs Pulse Width)	I_{TSM}	1000	Amp
Current Application Rate (up to 1000 A peak)	di/dt	1000	A/μs
Circuit Fusing (T_J = -65 to +125°C; t ≦ 1.0 ms	I^2t	250	A^2s
Dynamic Average Power (T_C = 65°C)	$P_{F(AV)}$	30	Watts
Peak Gate Power - Forward	P_{GM}	20	Watts
Average Gate Power - Forward	$P_{G(AV)}$	1.0	Watt
Peak Gate Current - Forward	I_{GM}	5.0	Amp
Peak Gate Voltage	V_{GM}	10	Volts
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Stud Torque	—	30	in.-lb

*V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage.
Ratings apply for zero or negative gate voltage.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W



STYLE 1:
PIN 1. CATHODE
2. GATE
3. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

CASE 263-03

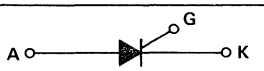
7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Units
Peak Forward Blocking Current (V_D = Rated V_{DRM} with gate open, T_J = 125°C)	I_{DRM}	–	–	8.0	mA
Peak Reverse Blocking Current (V_D = Rated V_{RRM} with gate open, T_J = 125°C)	I_{RRM}	–	–	8.0	mA
Forward "On" Voltage (I_{TM} = 25 Adc)	V_{TM}	–	1.1	1.3	Volts
Dynamic Forward On Voltage (I_{GT} = 500 mA, I_{pulse} = 500 Amps) (1.0 μs after start (10% pt.) of I_{pulse}) (5.0 μs after start (10% pt.) of I_{pulse})	v_{TM}	 – –	 30 5.0	 – –	
Gate Trigger Current (Continuous dc) (V_D = 7Vdc, R_L = 50Ohms)	I_{GT}	–	10	50	mA
Gate Trigger Voltage (Continuous dc) (V_D = 7 Vdc, R_L = 50 Ohms) (V_D = Rated V_{DRM}, R_L = 50 Ohms, T_J = 125°C)	V_{GT} V_{GD}	– 0.25	0.8 –	1.5 –	Volts
Holding Current (V_D = 7.0 Vdc, Gate Open) (V_D = 7.0 Vdc, Gate Open, T_J = 125°C)	I_H	5.0 –	15 6.0	– –	mA
Circuit Commutated Turn-Off Time (I_F = 500 A, I_R = 10 A, dv/dt = 20 V/μs V_D = Rated V_{DRM}, V_R = Rated V_{RRM}) (Conductive Charging Circuit – Circuit dependent)	t_q	–	20	–	μs
Critical Exponential Rate of Rise (Gate Open, T_J = 125°C, V_D = Rated V_{DRM})	dv/dt	–	100	–	V/μs

(1) V_{DRM} for all types can be supplied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage.

MCR1906-1 thru MCR1906-6



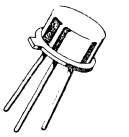
REVERSE BLOCKING TRIODE THYRISTORS

These devices are glassivated planar construction designed for applications in control systems and sensing circuits where low-level gating and holding characteristics are necessary.

- Low-Level Gate Characteristics – I_{GT} = 1.0 mA (Max) @ T_C = 25°C
- Low Holding Current – I_H = 5.0 mA (Max) @ T_C = 25°C
- Glass-to-Metal Bond for Maximum Hermetic Seal

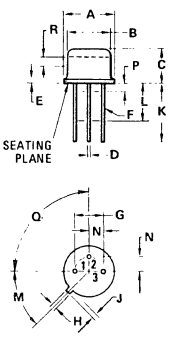
SILICON CONTROLLED RECTIFIERS

1.6 AMPERES RMS
25 thru 400 VOLTS



MAXIMUM RATINGS (T_J = 100°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Repetitive Peak Reverse Blocking Voltage MCR1906-1 MCR1906-2 MCR1906-3 MCR1906-4 MCR1906-5 MCR1906-6 MCR1906-7 MCR1906-8	V_{RRM}	 25 50 100 200 300 400 500 600	Volts
RMS On-State Current (All Conduction Angles)	$I_{T(RMS)}$	1.6	Amp
Peak Non-Repetitive Surge Current (One Cycle, 60 Hz, T_J = -40 to +110°C) Preceded and followed by rated current and voltage	I_{TSM}	15	Amp
Peak Gate Power	P_{GM}	0 1	Watt
Average Gate Power	$P_{GF(AV)}$	0.01	Watt
Peak Gate Current	I_{GM}	0.1	Amp
Peak Gate Voltage	V_{GM}	6.0	Volt
Operating Junction Temperature Range	T_J	-65 to +110	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Solder Temperature (>1/16" From Case, 10 s max.)	–	+230	°C



STYLE 3
PIN 1 CATHODE
2 GATE
3 ANODE (CONNECTED TO CASE)

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	8 89	9 40	0 350	0 370
B	8 00	8 51	0 315	0 335
C	6 10	6 60	0 240	0 260
D	0 406	0.533	0 016	0 021
E	0 229	3 18	0 009	0 125
F	0 406	0.483	0 016	0 019
G	4 83	5 33	0 190	0 210
H	0 711	0 864	0 028	0 034
J	0 737	1 02	0 029	0 040
K	12 70	–	0 500	–
L	6 35	–	0 250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0 050
Q	90° NOM		90° NOM	
R	2 54	–	0 100	–

All JEDEC dimensions and notes apply

CASE 79-02
TO-39

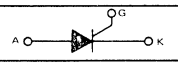
7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1)	MJ13335	$V_{CEO(sus)}$	500	–	–	Vdc
(I_C = 100 mA, I_B = 0)	MJ13334		450	–	–	
	MJ13333		400	–	–	
	MJ13332		350	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	–	5.0	
Collector Cutoff Current		I_{CER}	–	–	5.0	mAdc
(V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)						
Emitter Cutoff Current		I_{EBO}	–	–	1.0	mAdc
(V_{EB} = 6.0 Vdc, I_C = 0)						
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}	10	–	60	–
(I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)						
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 2.0 Adc)			–	–	1.8	
(I_C = 20 Adc, I_B = 6.7 Adc)			–	–	5.0	
(I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)			–	–	2.4	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 2.0 Adc)			–	–	1.8	
(I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)			–	–	1.8	
DYNAMIC CHARACTERISTICS						
Output Capacitance		C_{ob}	125	–	500	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)						
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 10 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.02	0.1	μs
Rise Time		t_r	–	0.3	0.7	μs
Storage Time		t_s	–	1.6	4.0	μs
Fall Time		t_f	–	0.3	0.7	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 10 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	2.5	5.0	μs
Crossover Time		t_c	–	0.8	2.0	μs
Storage Time	(I_C = 10 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	–	1.8	–	μs
Crossover Time		t_c	–	0.4	–	μs
Fall Time		t_{fi}	–	0.2	–	μs

(1) Pulse Test: PW - 300 μs, Duty Cycle ≤ 2%.

MCR3818-1 thru MCR3818-10
MCR3918-1 thru MCR3918-10



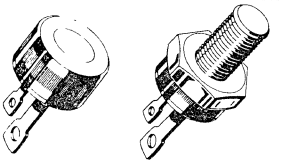
REVERSE BLOCKING TRIODE THYRISTOR

. . . designed for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls.

- Supplied in Either Pressfit or Stud Package
- High Surge Current Rating – I_{TSM} = 240 Amp
- Low On-State Voltage – 1.2 V (Typ) @ I_{TM} = 20 Amp
- Practical Level Triggering and Holding Characteristics – 40 mA (Max) and 50 mA (Max) @ $T_C = 25^oC$

SILICON CONTROLLED RECTIFIER

20 AMPERES RMS
25–800 VOLTS



MAXIMUM RATINGS

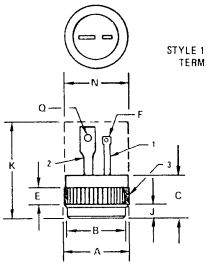
Rating	Symbol	Value	Unit
Peak Repetitive Forward and Reverse Voltage (1)			
MCR3818, MCR3918 - 1	V_{DRM}	25	Volts
- 2	- or	50	
- 3	V_{RRM}	100	
- 4		200	
- 5		300	
- 6		400	
- 7		500	
- 8		600	
- 9		700	
- 10		800	
Non-Repetitive Reverse Blocking Voltage	V_{RSM}		Volts
MCR3818, MCR3918 - 1		35	
-2		75	
-3		150	
- 4		300	
- 5		400	
- 6		500	
- 7		600	
- 8		700	
- 9		800	
- 10		900	
On-State Current RMS	$I_{T(RMS)}$	20	Amp
Average On-State Current ($T_C = 67^oC$)	$I_{T(AV)}$	13	Amp
Circuit Fusing (T_J = -40 to +100°C, t ⩽ 8.3 ms)	I^2t	235	A^2s
Peak Non-Repetitive Surge Current (One cycle, 60 Hz, T_J = -40 to +100°C)	I_{TSM}	240	Amp
Peak Gate Power (Maximum Pulse Width = 10 μs)	P_{GM}	5.0	Watts
Average Gate Power	$P_{G(AV)}$	0.5	Watt
Peak Forward Gate Current (Maximum Pulse Width = 10 μs)	I_{GM}	2.0	Amp
Peak Gate Voltage	V_{GM}	10	Volts
Operating Junction Temperature Range	T_J	-40 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C
Stud Torque		30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$			°C/W
Pressfit Package		1.0	1.5	
Stud Package		1.1	1.6	

(1)See note on page 2.

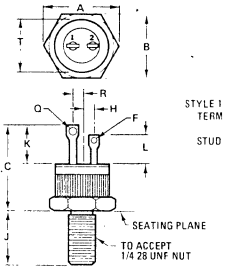
MCR3818 SERIES



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
B	11.81	12.06	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54		0.100	
F	0.89	2.16	0.035	0.085
J	2.04	2.46	0.080	0.097
K		20.32		0.800
N		12.95		0.510
Q	1.65	4.06	0.065	0.160

CASE 174-03

MCR3918 SERIES



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	0.89	2.16	0.035	0.085
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	1.65	4.06	0.065	0.160
R	1.65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505

CASE 175-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Peak Forward Blocking Current (V_D = Rated V_{DRM} @ T_J = 100°C, gate open)	I_{DRM}	–	5.0	mA
Peak Reverse Blocking Current (V_R = Rated V_{RRM} @ T_J = 100°C, gate open)	I_{RRM}	–	5.0	mA
Gate Trigger Current (Continuous dc) (2)	I_{GT}			mA
(V_D = 7.0 Vdc, R_L = 100 Ω)		–	40	
(V_D = 7.0 Vdc, R_L = 100 Ω, T_C = -40°C)		–	75	
Gate Trigger Voltage (Continuous dc)	V_{GT}			Volts
(V_D = 7.0 Vdc, gate open)		–	1.5	
(V_D = 7.0 Vdc, R_L = 100 Ω, T_C = -40°C)		–	2.5	
(V_D =Rated V_{DRM}, R_L = 100 Ω, T_J = 100°C)		0.2	–	
Peak On-State Voltage (Pulse Width = 1.0 ms max, duty cycle ≤ 1%)	V_{TM}			Volts
(I_{TM} = 20 A)		–	1.5	
(I_{TM} = 41 A)		–	1.7	
Holding Current	I_H			mA
(V_D = 7.0 Vdc, gate open)		–	50	
(V_D = 7.0 Vdc, gate open, T_C = -40°C)		–	90	
		Typical		
Gate Controlled Turn-On Time ($t_d + t_r$) (I_{TM} = 20 A, I_{GT} = 40 mAdc, V_D = Rated V_{DRM})	t_{gt}	1.0		μs
Circuit Commutated Turn-Off Time	t_q			μs
(I_{TM} = 10 A, I_R = 10 A)		20		
(I_{TM} = 10 A, I_R = 10 A, T_J = 100°C) (V_D = V_{DRM} = rated voltage) (dv/dt = 30 V/μs)		30		
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Wave Form, Gate open, T_J = 100°C)	dv/dt	50		V/μs

(1) V_{DRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. These devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

7

EFFECT OF TEMPERATURE UPON TYPICAL TRIGGER CHARACTERISTICS

FIGURE 1 – GATE TRIGGER CURRENT

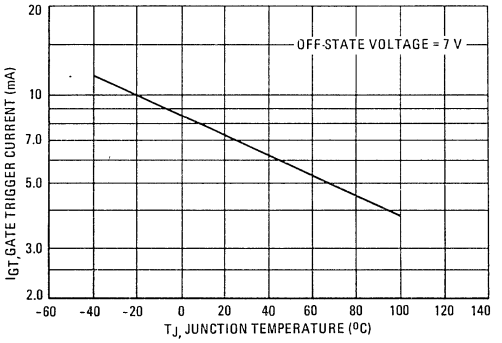
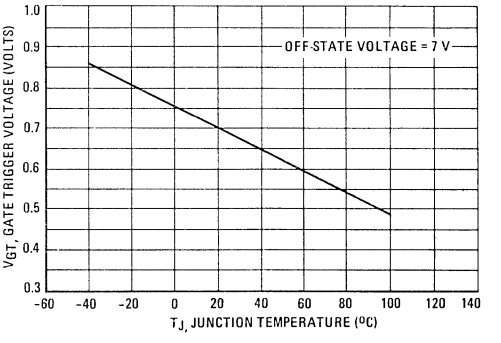


FIGURE 2 – GATE TRIGGER VOLTAGE



MAXIMUM ALLOWABLE NON-REPETITIVE SURGE CURRENT

FIGURE 3 – 60 Hz SURGES

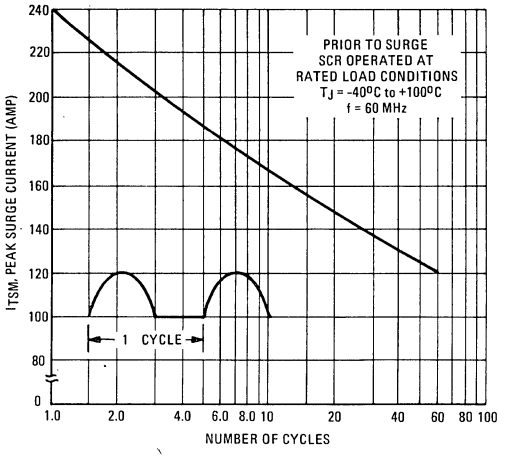


FIGURE 4 – SUB-CYCLE SURGES

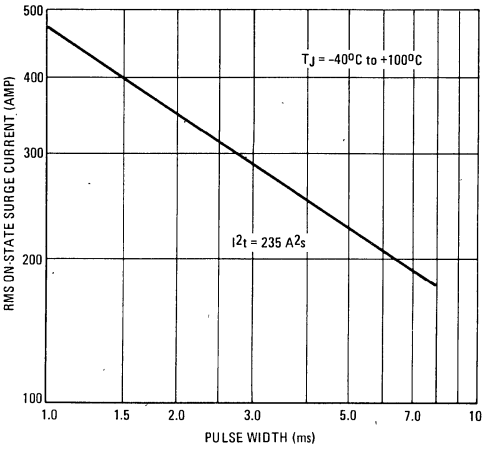


FIGURE 5 – GATE TRIGGER CHARACTERISTICS

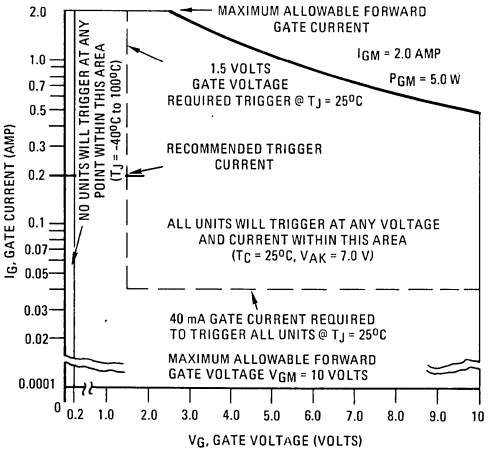
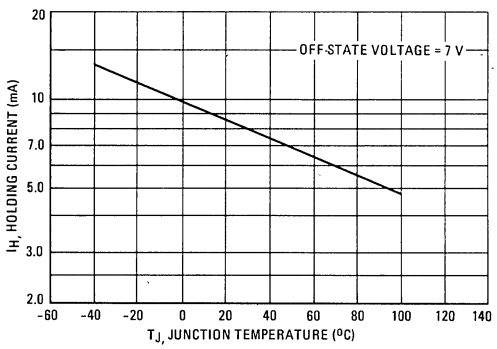


FIGURE 6 – EFFECT OF TEMPERATURE ON TYPICAL HOLDING CURRENT



DERATING AND DISSIPATION FOR RESISTIVE AND INDUCTIVE LOADS (f = 60 to 400 Hz, SINE WAVE)

FIGURE 7 – AVERAGE CURRENT DERATING

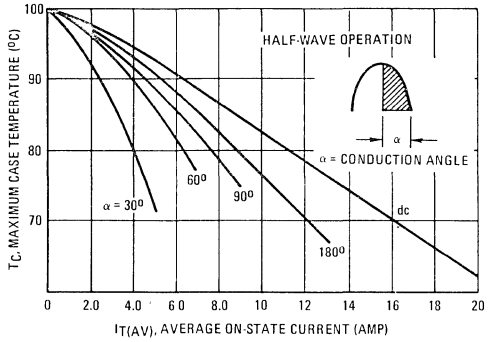


FIGURE 8 – ON-STATE POWER DISSIPATION

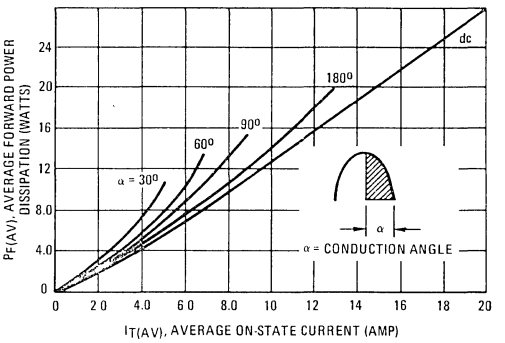


FIGURE 9 – ON-STATE CHARACTERISTICS

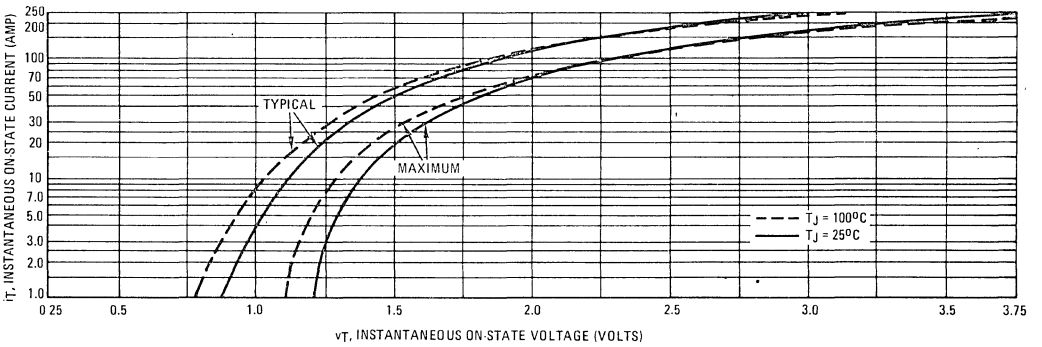


FIGURE 10 – TYPICAL THERMAL RESISTANCE OF PLATES

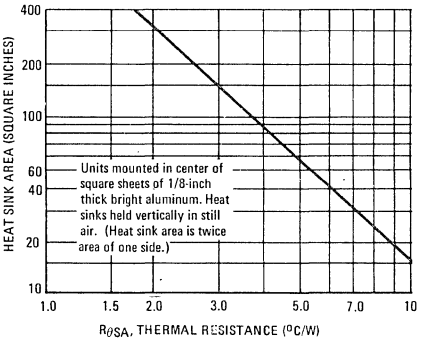
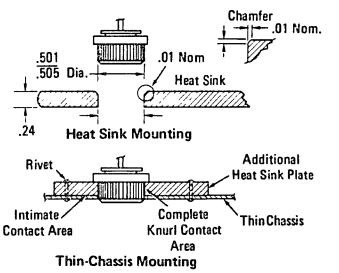


FIGURE 11 – MOUNTING DETAILS FOR PRESSFIT THYRISTORS



The hole edge must be chamfered as shown to prevent shearing off the knurled edge of the rectifier during press-in. The pressing force should be applied evenly on the shoulder ring to avoid tilting or canting of the rectifier case in the hole during the pressing operation. Also, the use of a thermal joint compound will be of considerable aid. The pressing force will vary from 250 to 1000 pounds, depending upon the heat sink material. Recommended hardnesses are: copper – less than 50 on the Rockwell F scale; aluminum – less than 65 on the Brinell scale. A heat sink as thin as 1/8" may be used, but the interface thermal resistance will increase in proportion to the reduction of contact area. A thin chassis requires the addition of a back-up plate.

MCR3835-1 thru MCR3835-10
MCR3935-1 thru MCR3935-10

REVERSE BLOCKING TRIODE THYRISTOR

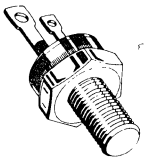
. . . designed for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current – I_{TSM} = 350 Amp
- Low Forward "On" Voltage – 1.2 V (Typ) @ I_{TM} = 35 Amp
- Practical Level Triggering and Holding Characteristics – 10 mA (Typ) @ T_C = 25°C
- Rugged Construction in Either Pressfit or Stud Package
- Glass Passivated Junctions for Maximum Reliability

SILICON CONTROLLED RECTIFIER

35 AMPERES RMS
25–800 VOLTS

CASE 174-03
MCR3835 Series



CASE 175-02
MCR3935 Series

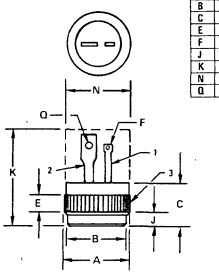
MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Peak Repetitive Forward and Reverse Blocking Voltage	-1	V_{DRM}(1) V_{RRM}	25	Volts
	-2		50	
	-3		100	
MCR3835	-4		200	
	-5		300	
	-6		400	
MCR3935	-7		500	
	-8		600	
	-9		700	
	-10		800	
Peak Non-Repetitive Reverse Blocking Voltage ($t \leq 5.0$ ms)	-1	V_{RSM}	35	Volts
	-2		75	
	-3		150	
MCR3835	-4		300	
	-5		400	
	-6		500	
MCR3935	-7		600	
	-8		700	
	-9		800	
	-10		900	
Forward Current RMS		$I_{T(RMS)}$	35	Amp
Peak Surge Current (One cycle, 60 Hz) (T_J = -40 to +100°C)		I_{TSM}	350	Amp
Circuit Fusing (T_J = -40 to +100°C) (t = 1.0 to 8.3 ms)		I^2t	510	A^2s
Peak Gate Power		P_{GFM}	5.0	Watts
Average Gate Power		$P_{GF(AV)}$	0.5	Watt
Peak Forward Gate Current		I_{GFM}	2.0	Amp
Peak Gate Voltage – Forward		V_{GFM}	10	Volts
Reverse		V_{GRM}	10	
Operating Junction Temperature Range		T_J	-40 to +100	°C
Storage Temperature Range		T_{stg}	-40 to +150	°C
Stud Torque		–	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
MCR3835		1.2	
MCR3935		1.3	

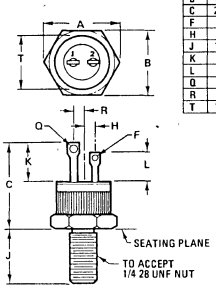
(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
B	11.81	12.06	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54	–	0.100	–
F	0.89	2.16	0.035	0.085
J	2.04	2.46	0.080	0.097
K	–	20.32	–	0.800
N	–	12.95	–	0.510
Q	1.65	4.06	0.065	0.160

STYLE 1
TERM. 1 GATE
2 CATHODE
3 ANODE

CASE 174-03



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	0.89	2.16	0.035	0.085
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	1.65	4.06	0.065	0.160
R	1.65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505

STYLE 1
TERM 1 CATHODE
2 GATE
STUD ANODE

CASE 175-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (V_D = Rated V_{DRM}, with gate open, T_J = 100°C)	I_{DRM}	–	1.0	5.0	mA
Peak Reverse Blocking Current (V_R = Rated V_{RRM}, with gate open, T_J = 100°C)	I_{RRM}	–	1.0	5.0	mA
Forward "On" Voltage (I_{TM} = 35 A Peak)	V_{TM}	–	1.2	1.5	Volts
Gate Trigger Current (Continuous dc) (V_D = 7.0 V, R_L = 100 Ω)	I_{GT}	–	10	40	mA
Gate Trigger Voltage (Continuous dc) (V_D = 7.0 V, R_L = 100 Ω)	V_{GT}	–	0.7	1.5	Volts
(V_D = Rated V_{DRM}, R_L = 100 Ω, T_J = 100°C)	V_{GD}	0.2	–	–	
Holding Current (V_D = 7.0 V, gate open)	I_H	–	10	50	mA
Turn-On Time ($t_d + t_r$) (I_{TM} = 35 Adc, I_{GT} = 40 mAdc)	t_{on}	–	1.0	–	μs
Turn-Off Time (I_{TM} = 10 A, I_R = 10 A)	t_q	–	20	–	μs
(I_{TM} = 10 A, I_R = 10 A, T_J = 100°C)		–	30	–	
Forward Voltage Application Rate (V_D = Rated V_{DRM}, T_J = 100°C)	dv/dt	–	50	–	V/μs

(1) V_{DRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested with a constant current source for forward or reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.

FIGURE 1 – CURRENT DERATING

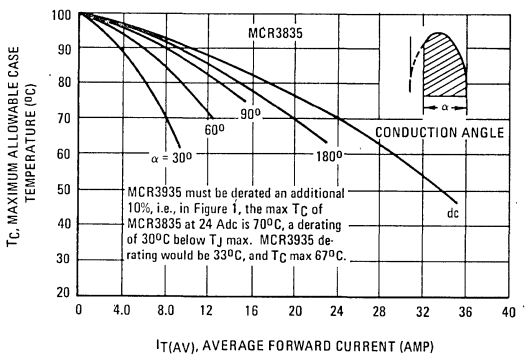


FIGURE 2 – TYPICAL POWER DISSIPATION

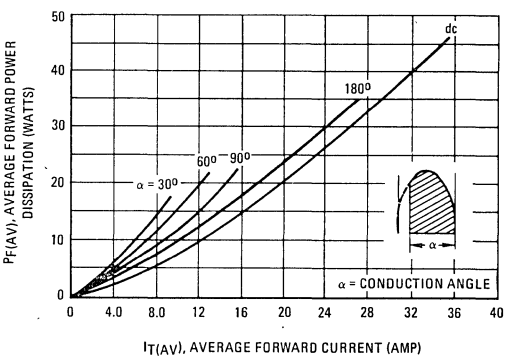


FIGURE 3 – TYPICAL GATE TRIGGER CURRENT

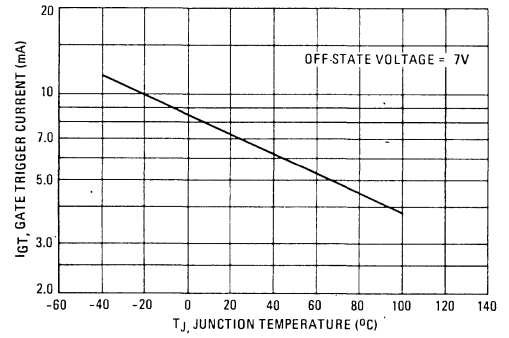
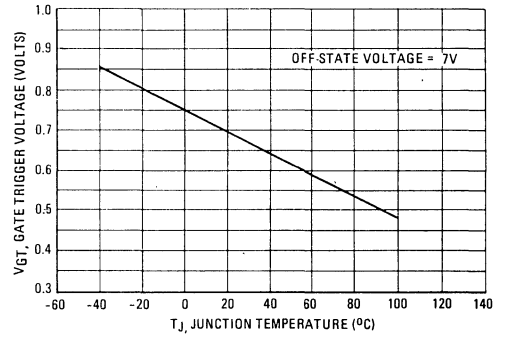


FIGURE 4 – TYPICAL GATE TRIGGER VOLTAGE



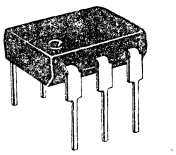
MOC3010
MOC3011

OPTICALLY ISOLATED TRIAC DRIVER

These devices consist of a gallium-arsenide infrared emitting diode, optically coupled to a silicon bilateral switch and are designed for applications requiring isolated triac triggering, low-current isolated ac switching, high electrical isolation (to 7500 V peak), high detector standoff voltage, small size, and low cost.

- UL Recognized File Number 54915

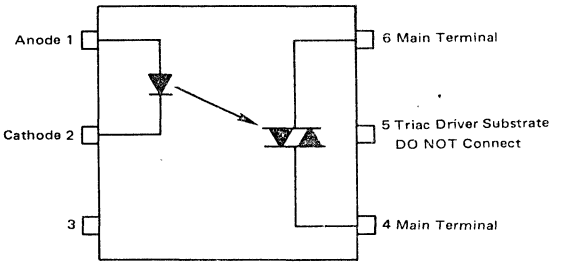
OPTICALLY ISOLATED TRIAC DRIVER

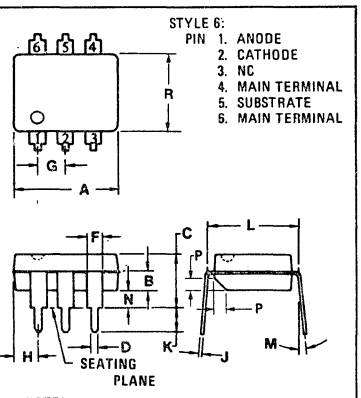


MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE MAXIMUM RATINGS			
Reverse Voltage	V_R	3.0	Volts
Forward Current — Continuous	I_F	50	mA
Total Power Dissipation @ T_A = 25°C Negligible Power in Transistor Derate above 25°C	P_D	100 1.33	mW mW/°C
OUTPUT DRIVER MAXIMUM RATINGS			
Off-State Output Terminal Voltage	V_{DRM}	250	Volts
On-State RMS Current T_A = 25°C (Full Cycle, 50 to 60 Hz) T_A = 70°C	$I_{T(RMS)}$	100 50	mA mA
Peak Nonrepetitive Surge Current (PW = 10 ms, DC = 10%)	I_{TSM}	1.2	A
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 4.0	mW mW/°C
TOTAL DEVICE MAXIMUM RATINGS			
Isolation Surge Voltage (1) (Peak ac Voltage, 60 Hz, 5 Second Duration)	V_{ISO}	7500	Vac
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	330 4.4	mW mW/°C
Junction Temperature Range	T_J	-40 to +100	°C
Ambient Operating Temperature Range	T_A	-40 to +70	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C
Soldering Temperature (10 s)	—	260	°C

(1) Isolation surge voltage, V_{ISO}, is an internal device dielectric breakdown rating.





NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIAMETER OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.13	8.89	0.320	0.350
B	1.27	2.03	0.050	0.080
C	2.92	5.08	0.115	0.200
D	0.41	0.51	0.016	0.020
F	1.02	1.78	0.040	0.070
G	2.54	BSC	0.100	BSC
H	1.02	2.16	0.040	0.085
J	0.20	0.30	0.008	0.012
K	2.54	3.81	0.100	0.150
L	7.62	BSC	0.300	BSC
M	0°	15°	0°	15°
N	0.38	2.54	0.015	0.100
P	0.61	0.97	0.032	0.038
R	6.10	6.60	0.240	0.260

CASE 730

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
LED CHARACTERISTICS						
Reverse Leakage Current (V_R = 3.0 V)		I_R	–	0.05	100	μA
Forward Voltage (I_F = 10 mA)		V_F	–	1.2	1.5	Volts
DETECTOR CHARACTERISTICS (I_F = 0 unless otherwise noted)						
Peak Blocking Current, Either Direction (Rated V_{DRM}, Note 1)		I_{DRM}	–	10	100	nA
Peak On-State Voltage, Either Direction (I_{TM} = 100 mA Peak)		V_{TM}	–	2.5	3.0	Volts
Critical Rate of Rise of Off-State Voltage, Figure 3		dv/dt	–	2.0	–	V/μs
Critical Rate of Rise of Commutation Voltage, Figure 3 (I_{load} = 15 mA)		dv/dt	–	0.15	–	V/μs
COUPLED CHARACTERISTICS						
LED Trigger Current, Current Required to Latch Output (Main Terminal Voltage = 3.0 V)	MOC3010	I_{FT}	–	8.0	15	mA
	MOC3011		–	5.0	10	
Holding Current, Either Direction		I_H	–	100	–	μA

Note 1. Test voltage must be applied within dv/dt rating.

2. Additional information on the use of the MOC3010/3011 is available in Application Note AN-780.

TYPICAL ELECTRICAL CHARACTERISTICS
T_A = 25°C

FIGURE 1 – ON-STATE CHARACTERISTICS

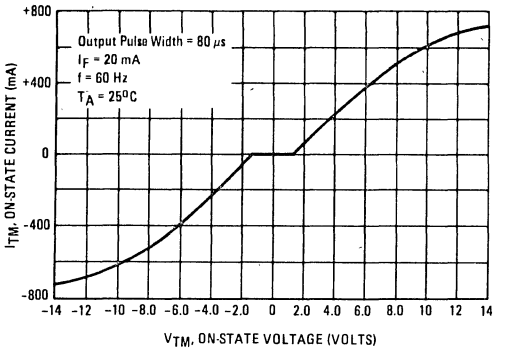

FIGURE 2 – TRIGGER CURRENT versus TEMPERATURE

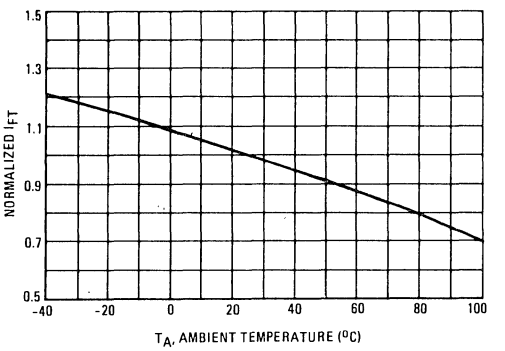

FIGURE 3 – dv/dt TEST CIRCUIT

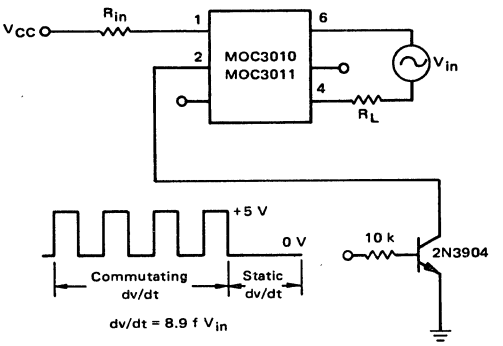

FIGURE 4 – dv/dt versus LOAD RESISTANCE

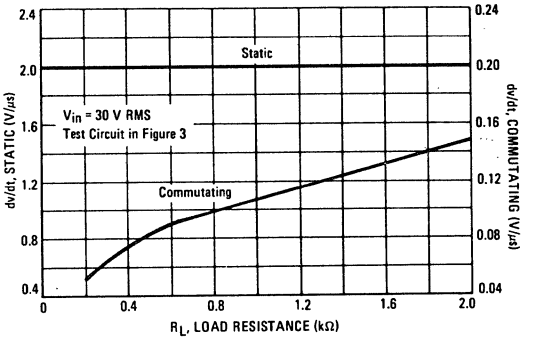

FIGURE 5 – dv/dt versus TEMPERATURE

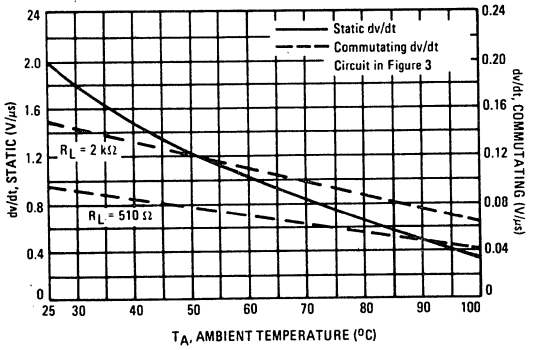

FIGURE 6 – COMMUTATING dv/dt versus FREQUENCY

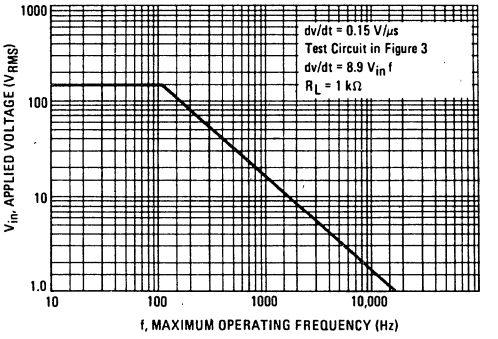

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FIGURE 7 – MAXIMUM NONREPETITIVE SURGE CURRENT

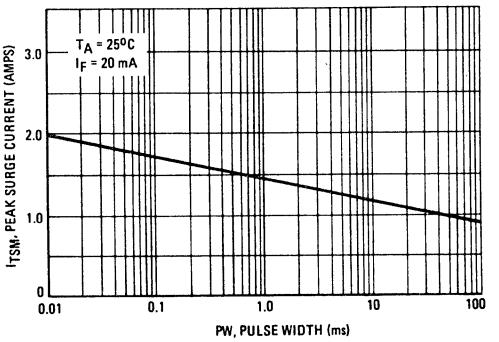


FIGURE 8 – LAMP DRIVER APPLICATION

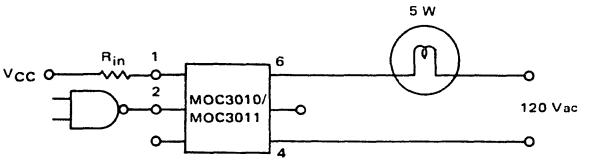


FIGURE 9 – RESISTIVE LOAD

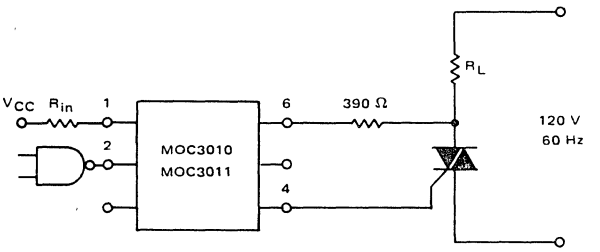
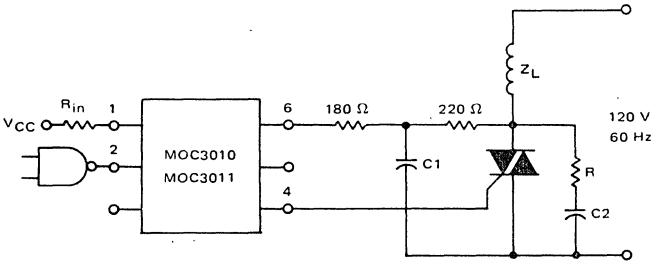
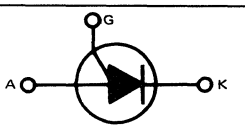


FIGURE 10 – INDUCTIVE LOAD



R, C1, C2 Values Depend upon Load Condition.

MPU131
MPU132
MPU133

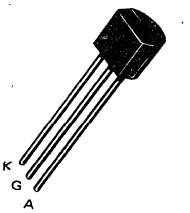


PROGRAMMABLE UNIJUNCTION TRANSISTORS

SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS

. . . designed to enable the engineer to "program" unijunction characteristics such as R_{BB}, η, I_V, and I_P by merely selecting two resistor values. Application includes thyristor-trigger, oscillator, pulse and timing circuits. The MPU131, MPU132 and MPU133 may also be used in special thyristor applications due to the availability of an anode gate. Supplied in an inexpensive TO-92 plastic package for high-volume requirements, this package is readily adaptable for use in automatic insertion equipment.

- Programmable — R_{BB}, η, I_V and I_P.
- Low On-State Voltage — 1.5 Volts Maximum @ I_F = 50 mA
- Low Gate to Anode Leakage Current — 5.0 nA Maximum
- High Peak Output Voltage — 11 Volts Typical
- Low Offset Voltage — 0.35 Volt Typical (R_G = 10 k ohms)

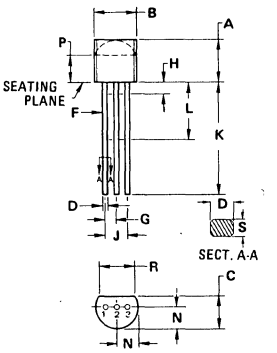


7

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Dissipation Derate Above 25°C	P_F $1/\theta_{JA}$	375 5.0	mW mW/°C
DC Forward Anode Current Derate Above 25°C	I_T	200 2.67	mA mA/°C
DC Gate Current	I_G	±20	mA
Repetitive Peak Forward Current 100 μs Pulse Width, 1.0% Duty Cycle 20 μs Pulse Width, 1.0% Duty Cycle	I_{TRM}	 1.0 2.0	 Amp Amp
Non-Repetitive Peak Forward Current 10 μs Pulse Width	I_{TSM}	5.0	Amp
Gate to Cathode Forward Voltage	V_{GKF}	40	Volt
Gate to Cathode Reverse Voltage	V_{GKR}	5.0	Volt
Gate to Anode Reverse Voltage	V_{GAR}	40	Volt
Anode to Cathode Voltage (1)	V_{AK}	±40	Volt
Operating Junction Temperature Range	T_J	-50 to +100	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

(1) Anode positive, R_{GK} = 1k ohm
Anode negative, R_{GK} = open



STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

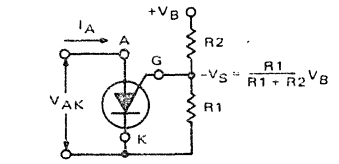
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.
CASE 29-02

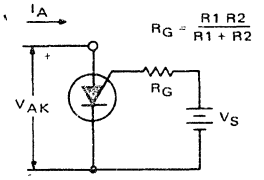
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Figure	Symbol	Min	Typ	Max	Unit
Peak Current	MPU131	2,9-14	I_P	–	1.25	2.0	μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	MPU132			–	0.19	0.30	
	MPU133			–	0.08	0.15	
(V_S = 10 Vdc, R_G = 10 k ohms)	MPU131			–	4.0	5.0	
	MPU132			–	1.20	2.0	
	MPU133				0.70	1.0	
Offset Voltage	MPU131	1	V_T	0.2	0.70	1.6	Volts
(V_S = 10 Vdc, R_G = 1.0 MΩ)	MPU132			0.2	0.50	0.6	
	MPU133			0.2	0.40	0.6	
(V_S = 10 Vdc, R_G = 10 k ohms) (All Types)				0.2	0.35	0.6	
Valley Current		1,4,5,	I_V				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	MPU131, 132			–	18	50	
	MPU133			–	18	25	
(V_S = 10 Vdc, R_G = 10 k ohms)	MPU131			70	270	–	
	MPU132, 133			50	270	–	
Gate to Anode Leakage Current		–	I_{GAO}				nAdc
(V_S = 40 Vdc, T_A = 25°C, Cathode Open)				–	1.0	5.0	
(V_S = 40 Vdc, T_A = 75°C, Cathode Open)				–	30	75	
Gate to Cathode Leakage Current (V_S = 40 Vdc, Anode to Cathode Shorted)		–	I_{GKS}	–	5.0	50	nAdc
Forward Voltage (I_F = 50 mA Peak)		1,6	V_F	–	0.8	1.5	Volts
Peak Output Voltage (V_B = 20 Vdc, C_C = 0.2 μF)		3,7	V_o	6.0	11	–	Volts
Pulse Voltage Rise Time (V_B = 20 Vdc, C_C = 0.2 μF)		3	t_r	–	40	80	ns

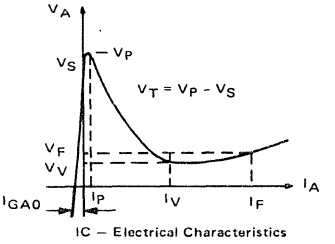
FIGURE 1 – ELECTRICAL CHARACTERIZATION



1A – Programmable Unijunction with "Program" Resistors R1 and R2



1B – Equivalent Test Circuit for Figure 1A used for electrical characteristics testing (also see Figure 2)



1C – Electrical Characteristics

FIGURE 2 – PEAK CURRENT (I_P) TEST CIRCUIT

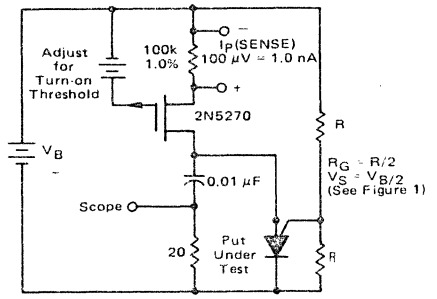
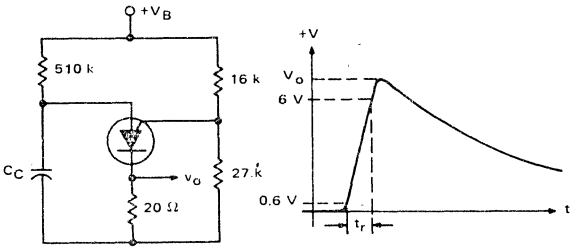


FIGURE 3 – V_o AND t_r TEST CIRCUIT



TYPICAL VALLEY CURRENT BEHAVIOR

FIGURE 4 – EFFECT OF SUPPLY VOLTAGE

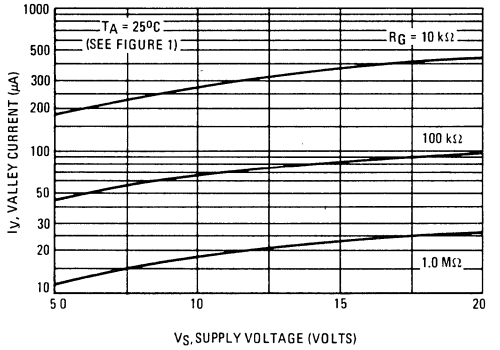


FIGURE 5 – EFFECT OF TEMPERATURE

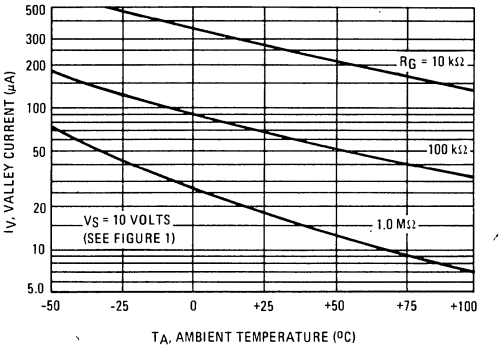


FIGURE 6 – FORWARD VOLTAGE

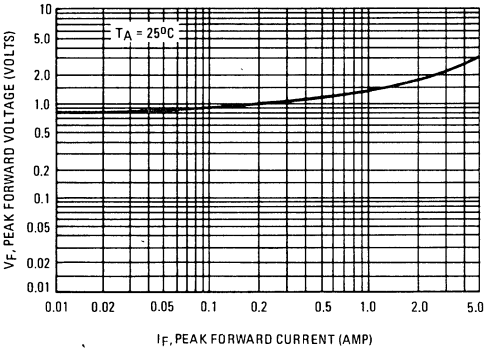


FIGURE 7 – PEAK OUTPUT VOLTAGE

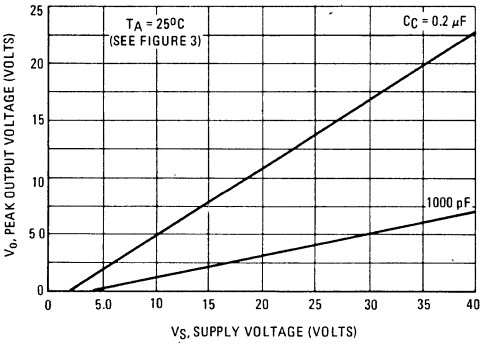
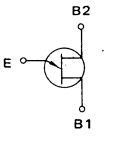
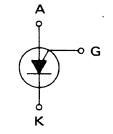


FIGURE 8 – STANDARD UNIJUNCTION COMPARED TO PROGRAMMABLE UNIJUNCTION

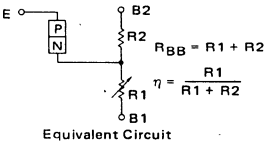


Circuit Symbol



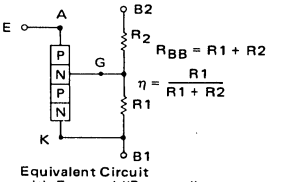
Circuit Symbol

STANDARD UNIJUNCTION

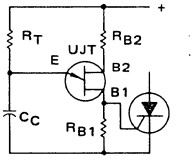


Equivalent Circuit

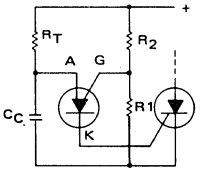
PROGRAMMABLE UNIJUNCTION



Equivalent Circuit
with External "Program"
Resistors R1 and R2



Typical Application



Typical Application

TYPICAL PEAK CURRENT BEHAVIOR

MPU131

FIGURE 9 – EFFECT OF SUPPLY VOLTAGE AND R_G

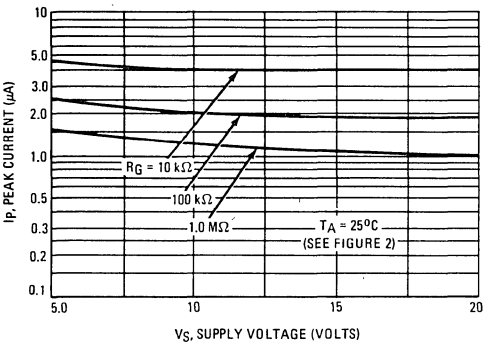
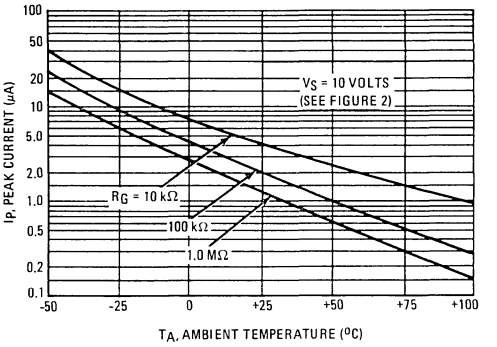


FIGURE 10 – EFFECT OF TEMPERATURE AND R_G



MPU132

FIGURE 11 – EFFECT OF SUPPLY VOLTAGE AND R_G

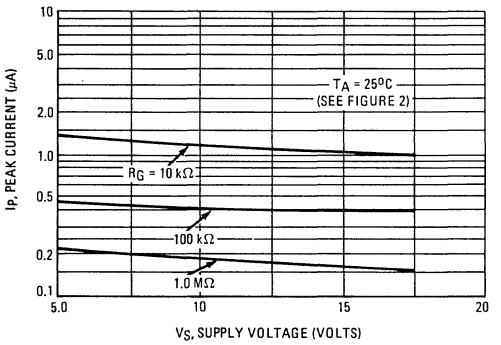
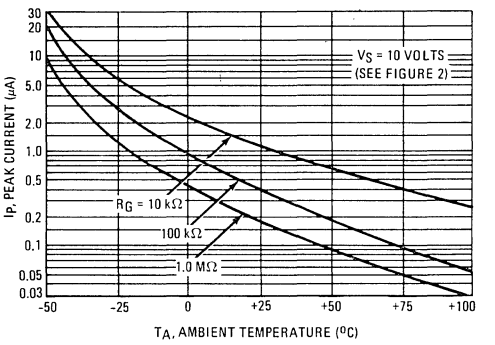


FIGURE 12 – EFFECT OF TEMPERATURE AND R_G



MPU133

FIGURE 13 – EFFECT OF SUPPLY VOLTAGE AND R_G

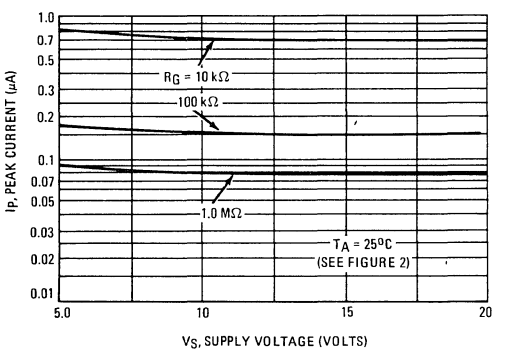
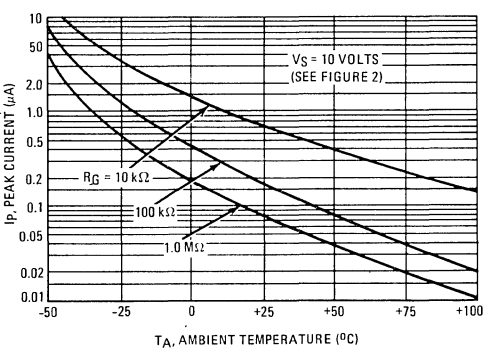
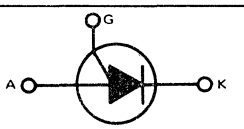


FIGURE 14 – EFFECT OF TEMPERATURE AND R_G



7

MPU6027
MPU6028

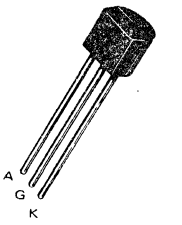


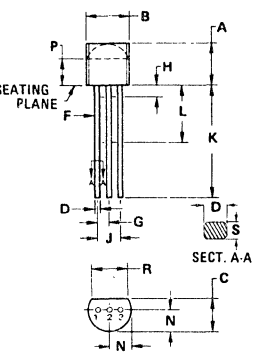
PROGRAMMABLE UNIJUNCTION TRANSISTORS

SILICON PROGRAMMABLE UNIJUNCTION TRANSISTORS

. . . designed to enable the engineer to "program" unijunction characteristics such as R_{BB}, η, I_V, and I_P by merely selecting two resistor values. Application includes thyristor-trigger, oscillator, pulse and timing circuits. These devices may also be used in special thyristor applications due to the availability of an anode gate. Supplied in an inexpensive TO-92 plastic package for high-volume requirements, this package is readily adaptable for use in automatic insertion equipment.

- Programmable – R_{BB}, η, I_V and I_P.
- Low On-State Voltage – 1.5 Volts Maximum @ I_F = 50 mA
- Low Gate to Anode Leakage Current – 10 nA Maximum
- High Peak Output Voltage – 11 Volts Typical
- Low Offset Voltage – 0.35 Volt Typical (R_G = 10 k ohms)





STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02
TO-92

7

MAXIMUM RATINGS

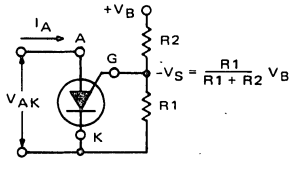
Rating	Symbol	Value	Unit
Power Dissipation (1) Derate Above 25°C	P_F $1/\theta_{JA}$	375 5.0	mW mW/°C
DC Forward Anode Current (2) Derate Above 25°C	I_T	200 2.67	mA mA/°C
DC Gate Current	I_G	±50	mA
Repetitive Peak Forward Current 100 μs Pulse Width, 1.0% Duty Cycle 20 μs Pulse Width, 1.0% Duty Cycle	I_{TRM}	 1.0 2.0	 Amp Amp
Non-Repetitive Peak Forward Current 10 μs Pulse Width	I_{TSM}	5.0	Amp
Gate to Cathode Forward Voltage	V_{GKF}	40	Volt
Gate to Cathode Reverse Voltage	V_{GKR}	-5.0	Volt
Gate to Anode Reverse Voltage (1)	V_{GAR}	40	Volt
Anode to Cathode Voltage	V_{AK}	±40	Volt.
Operating Junction Temperature Range	T_J	-50 to +100	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

(1) Anode positive, R_{GK} = 1k ohm
Anode negative, R_{GK} = open

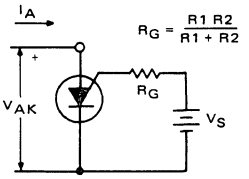
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Figure	Symbol	Min	Typ	Max	Unit
Peak Current		2,9,11	I_P				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	MPU6027			–	1.25	2.0	
	MPU6028			–	0.08	0.15	
(V_S = 10 Vdc, R_G = 10 k ohms)	MPU6027			–	4.0	5.0	
	MPU6028			–	0.70	1.0	
Offset Voltage		1	V_T				Volts
(V_S = 10 Vdc, R_G = 1.0 MΩ)	MPU6027			0.2	0.70	1.6	
	MPU6028			0.2	0.50	0.6	
(V_S = 10 Vdc, R_G = 10 k ohms)	(Both Types)			0.2	0.35	0.6	
Valley Current		1,4,5,	I_V				μA
(V_S = 10 Vdc, R_G = 1.0 MΩ)	MPU6027			–	18	50	
	MPU6028			–	18	25	
(V_S = 10 Vdc, R_G = 10 k ohms)	MPU6027			70	270	–	
	MPU6028			25	270	–	
Gate to Anode Leakage Current		–	I_{GAO}				nAdc
(V_S = 40 Vdc, T_A = 25°C, Cathode Open)				–	1.0	10	
(V_S = 40 Vdc, T_A = 75°C, Cathode Open)				–	3.0	–	
Gate to Cathode Leakage Current (V_S = 40 Vdc, Anode to Cathode Shorted)		–	I_{GKS}	–	5.0	50	nAdc
Forward Voltage (I_F = 50 mA Peak)		1,6	V_F	–	0.8	1.5	Volts
Peak Output Voltage (V_B = 20 Vdc, C_C = 0.2 μF)		3,7	V_o	6.0	11	–	Volts
Pulse Voltage Rise Time (V_B = 20 Vdc, C_C = 0.2 μF)		3	t_r	–	40	80	ns

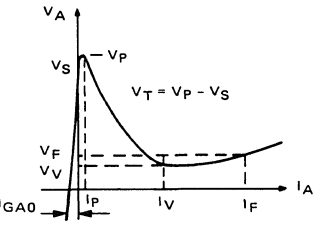
FIGURE 1 – ELECTRICAL CHARACTERIZATION



1A – Programmable Unijunction with "Program" Resistors R1 and R2



1B – Equivalent Test Circuit for Figure 1A used for electrical characteristics testing (also see Figure 2)



1C – Electrical Characteristics

FIGURE 2 – PEAK CURRENT (I_P) TEST CIRCUIT

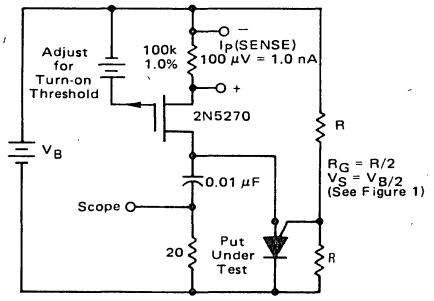
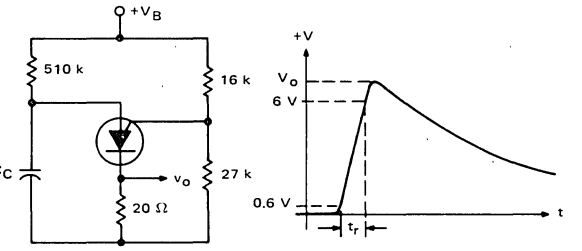


FIGURE 3 – V_o AND t_r TEST CIRCUIT



TYPICAL VALLEY CURRENT BEHAVIOR

FIGURE 4 – EFFECT OF SUPPLY VOLTAGE

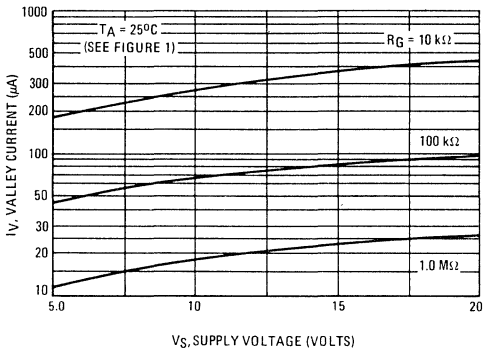


FIGURE 5 – EFFECT OF TEMPERATURE

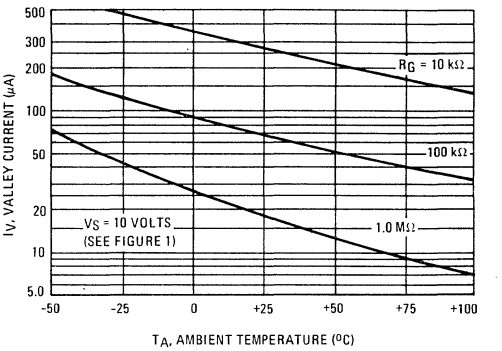


FIGURE 6 – FORWARD VOLTAGE

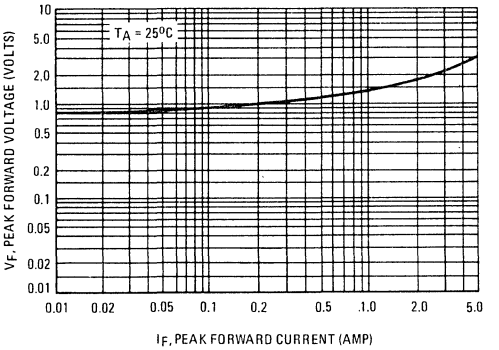
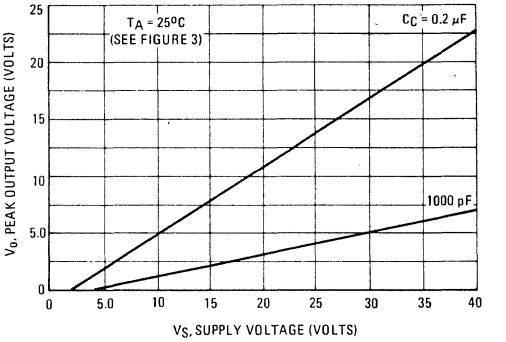


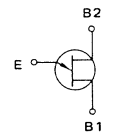
FIGURE 7 – PEAK OUTPUT VOLTAGE



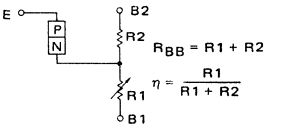
7

FIGURE 8 – STANDARD UNIJUNCTION
COMPARED TO PROGRAMMABLE UNIJUNCTION

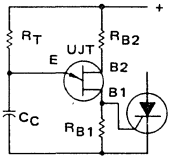
STANDARD UNIJUNCTION



Circuit Symbol

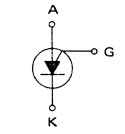


Equivalent Circuit

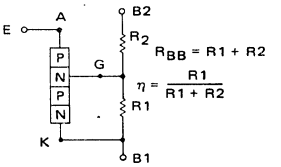


Typical Application

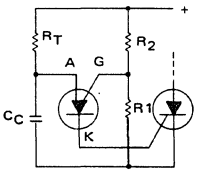
PROGRAMMABLE UNIJUNCTION



Circuit Symbol



Equivalent Circuit
with External "Program"
Resistors R1 and R2



Typical Application

TYPICAL PEAK CURRENT BEHAVIOR

MPU6027

FIGURE 9 – EFFECT OF SUPPLY VOLTAGE AND R_G

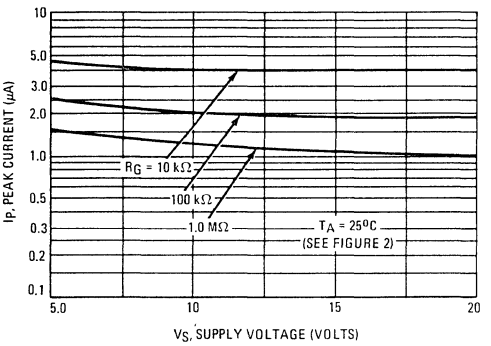
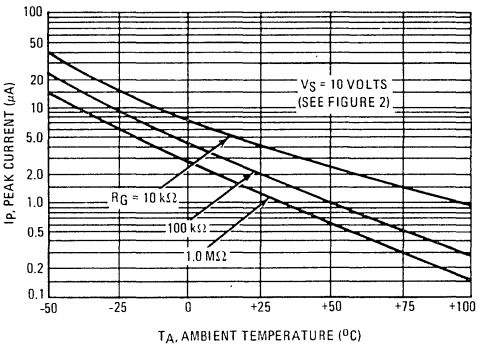


FIGURE 10 – EFFECT OF TEMPERATURE AND R_G



MPU6028

FIGURE 11 – EFFECT OF SUPPLY VOLTAGE AND R_G

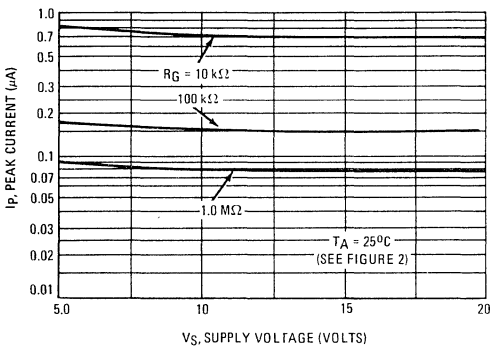
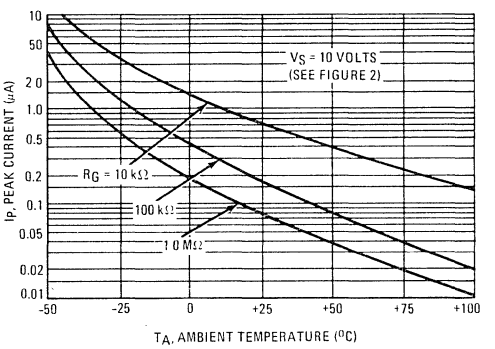
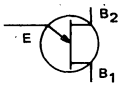


FIGURE 12 – EFFECT OF TEMPERATURE AND R_G



7

MU10
MU20



SILICON ANNULAR UNIJUNCTION TRANSISTORS

. . . designed for economical, general purpose use in pulse, timing, oscillator and thyristor trigger circuits.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
RMS Power Dissipation*	P_D	300	mW
RMS Emitter Current	I_e	50	mA
Peak-Pulse Emitter Current**	i_e	1.0	Amp
Emitter Reverse Voltage	V_{EB2}	30	Volts
Interbase Voltage Based upon Power Dissipation at T_A = 25°C	V_{B2B1}	35	Volts
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

*Derate 3.0 mW/°C increase in ambient temperature.

**Duty Cycle ≤ 1%, PRR = 10 PPS (See Figure 5).

FIGURE 1 – UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

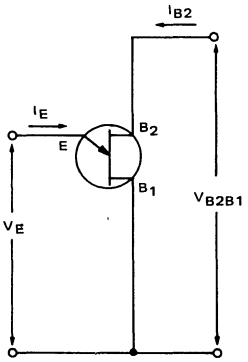
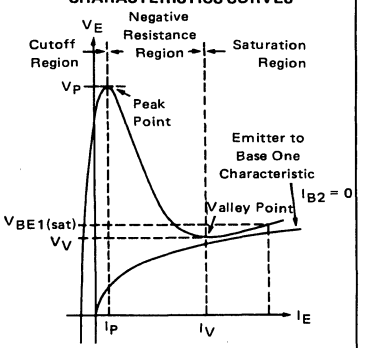


FIGURE 2 – STATIC EMITTER CHARACTERISTICS CURVES



Annular Semiconductors Patented by Motorola Inc.

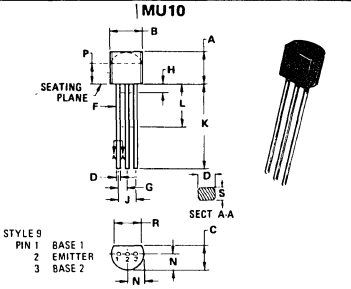
PN UNIJUNCTION TRANSISTORS

MU20

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.41	0.48	0.016	0.019
G	2.54 TYP		0.100 TYP	
H	0.91	1.17	0.036	0.046
J	0.71	1.22	0.028	0.048
K	12.70	–	0.500	–
M	45° TYP		45° TYP	
N	1.27 TYP		0.050 TYP	

CASE 22A-01
(TO-18 Outline
Except for Lead Position)

MU10



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

CASE 29-02
(TO-92)
Lead Forms 5 and 18
Shown on Next Page

7

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio* (Test Circuit Figure 4) (V_{B2B1} = 10 V)	η	0.50	–	0.85	–
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)	r_{BB}	4.0	–	10	kΩ
Emitter Saturation Voltage** (V_{B2B1} = 10 V, I_E = 50 mA)	$V_{EB1(sat)}$	–	2.0	–	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)	$I_{B2(mod)}$	–	–	50	mA
Emitter Reverse Current (V_{EB2} = 30 V, I_{B1} = 0)	I_{EB20}	–	–	1.0	μA
Peak-Point Emitter Current (V_{B2B1} = 25 V)	I_P	–	–	5.0	μA
Valley-Point Current** (V_{B2B1} = 20 V, R_{B2} = 100 Ohms)	I_V	1.0	–	–	mA
Base-One Peak Pulse Voltage (Test Circuit Figure 3)	V_{OB1}	3.0	–	–	Volts

* η, intrinsic standoff ratio, is defined in terms of the peak-point voltage, V_P, by means of the equation: $V_P = \eta V_{B2B1} + V_F$, where V_F is about 0.45 volt at 25°C @ I_F = 10 μA and decreases with temperature at about 2.5 mV/°C. The test circuit is shown in Figure 4. Components R_1, C_1, and the UJT form a relaxation oscillator; the remaining circuitry serves as a peak-voltage detector. The forward drop of Diode D_1 compensates for V_F. To use, the "cal" button is pushed, and R_3 is adjusted to make the current meter, M_1, read full scale. When the "cal" button is released, the value of η is read directly from the meter, if full scale on the meter reads 1.0.

** Pulse Test: Pulse Width ≈ 300 μs, Duty Cycle ≤ 2.0% to avoid internal heating, which may result in erroneous readings.

FIGURE 3 – V_{OB1} TEST CIRCUIT

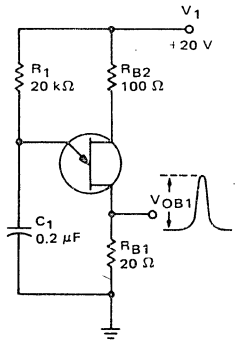
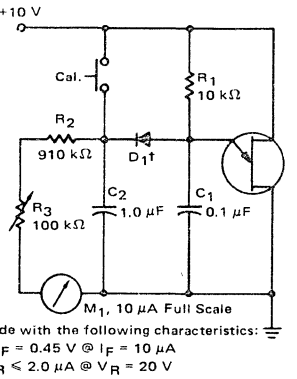
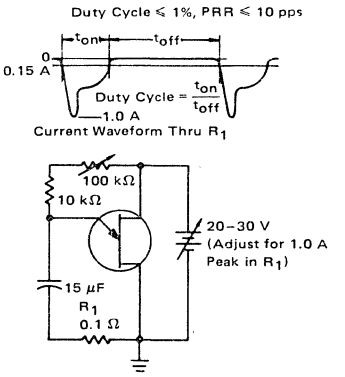


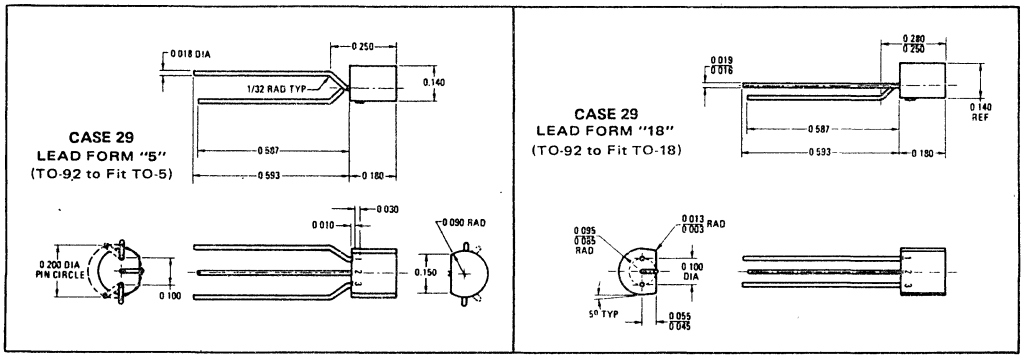
FIGURE 4 – η TEST CIRCUIT



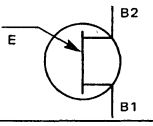
† D_1 diode with the following characteristics:
V_F = 0.45 V @ I_F = 10 μA
$I_R \leq$ 2.0 μA @ V_R = 20 V

FIGURE 5 – PRR TEST CIRCUIT AND WAVEFORM





MU2646

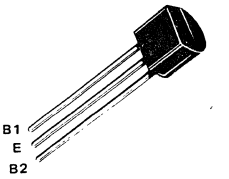


SILICON UNIJUNCTION TRANSISTOR

. . . designed for use in pulse and timing circuits, sensing circuits and thyristor trigger circuits.

- Low Peak Point Current – 5.0 μA (Max)
- Low Emitter Reverse Current – 12 μA (Max)
- Passivated Surface for Reliability and Uniformity
- TO-18 Lead Form Available Upon Request

PN UNIJUNCTION TRANSISTOR



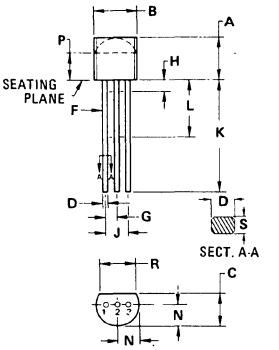
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
RMS Emitter Current	$I_{E(RMS)}$	50	mA
Peak Pulse Emitter Current (2)	i_e	2.0	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage	V_{B2B1}	35	Volts
RMS Power Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	300 3.0	mW mW/°C
Operating Junction Temperature Range	T_J	-65 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$(3)	333	°C/W

(1) The total power dissipation (available power to Emitter and Base-Two) must be limited by the external circuitry.
(2) Capacitor discharge – 10 μF or less, 30 volts or less.
(3) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.



STYLE 9:
PIN 1 BASE 1
2 EMITTER
3 BASE 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.
CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio (V_{B2B1} = 10 V) (Note 1)	η	0.56	–	0.75	–
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)	r_{BB}	4.7	7.0	9.1	kΩ
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = -55°C to +125°C)	$\alpha_{r_{BB}}$	0.1	–	0.9	%/°C
Emitter Saturation Voltage (V_{B2B1} = 10 V, I_E = 50 mA) (Note 2)	$V_{EB1(sat)}$	–	3.5	–	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)	$I_{B2(mod)}$	–	15	–	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)	I_{EB2O}	–	0.005	12	μA
Peak Point Emitter Current (V_{B2B1} = 25 V)	I_P	–	1.0	5.0	μA
Valley Point Current (V_{B2B1} = 20 V, R_{B2} = 100 ohms) (Note 2)	I_V	4.0	6.0	–	mA
Base-One Peak Pulse Voltage (Note 3, Figure 3)	V_{OB1}	3.0	5.0	–	Volts

Notes

(1) Intrinsic standoff ratio, η, is defined by equation

$$\eta = \frac{V_P - V_{(EB1)}}{V_{B2B1}}$$

Where V_P = Peak Point Emitter Voltage
V_{B2B1} = Interbase Voltage
$V_{(EB1)}$ = Emitter to Base-One Junction Diode Drop (≈0.5 V @ 10 μA)

(2) Use pulse techniques: PW ≈ 300 μs, duty cycle ≤ 2% to avoid internal heating due to interbase modulation which may result in erroneous readings.

(3) Base-One Peak Pulse Voltage is measured in circuit of Figure 3. This specification is used to ensure minimum pulse amplitude for applications in SCR firing circuits and other types of pulse circuits.

7

FIGURE 1
UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

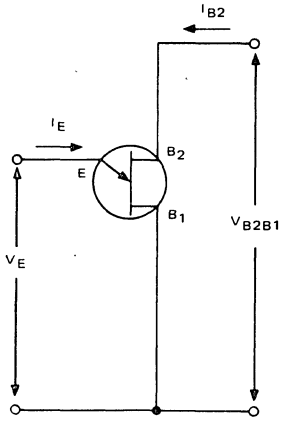


FIGURE 2
STATIC EMITTER CHARACTERISTIC CURVES
(Exaggerated to Show Details)

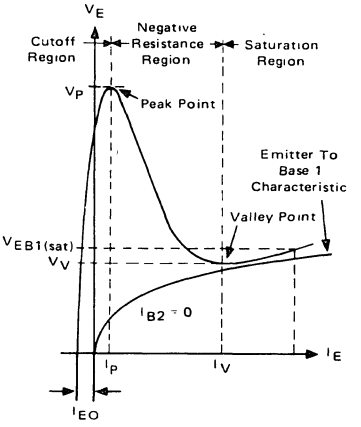
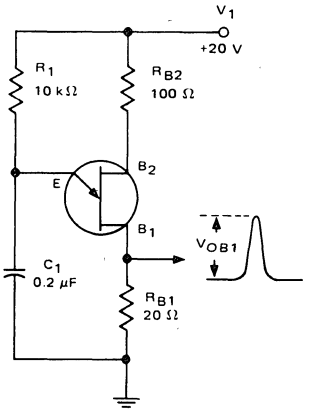
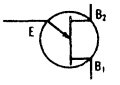


FIGURE 3 – V_{OB1} TEST CIRCUIT
(Typical Relaxation Oscillator)



MU4891 thru MU4894



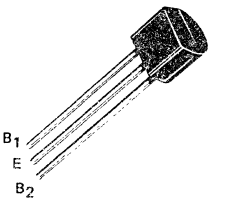
SILICON PLASTIC UNIJUNCTION TRANSISTORS

. . . designed for military and industrial use in pulse, timing, triggering, sensing, and oscillator circuits. The annular process provides low leakage current, fast switching and low peak-point currents as well as outstanding reliability and uniformity.

Recommended usage includes:

- Long-time Delay Circuits - MU4894
- Silicon Controlled Rectifier Triggering Circuits - MU4893
- High-frequency Relaxation-Oscillator Circuits - MU4892
- General-Purpose Unijunction Applications - MU4891

PN UNIJUNCTION TRANSISTORS



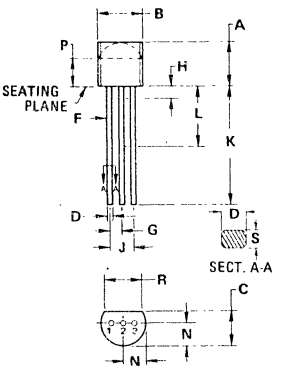
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
RMS Power Dissipation*	P_D	300	mW
RMS Emitter Current	I_e	50	mA
Peak Pulse Emitter Current**	i_e	1.0**	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Storage Temperature Range	T_{stg}	-65 to +150	°C

*Derate 3.0 mW/°C increase in ambient temperature. Total power dissipation (available power to Emitter and Base-Two) must be limited by external circuitry. Interbase voltage (V_{B2B1}) limited by power dissipation,

$$V_{B2B1} = \sqrt{R_{BB} \cdot P_D}$$

** Capacitance discharge current must fall to 0.37 Amp within 3.0 ms and PRR ≤ 10 PPS.



STYLE 9:
PIN 1 BASE 1
2 EMITTER
3 BASE 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.
CASE 29-02
TO-92

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio		η				–
(V_{B2B1} = 10 V) Note 1	MU4892		0.51	–	0.69	
	MU4891, MU4893		0.55	–	0.82	
	MU4894		0.74	–	0.86	
Interbase Resistance		R_{BB}				k ohms
(V_{B2B1} = 3.0 V, I_E = 0)	MU4891, MU4892		4.0	7.0	9.1	
	MU4893, MU4894		4.0	7.0	12.0	
Interbase Resistance Temperature Coefficient		αR_{BB}				%/°C
(V_{B2B1} = 3.0 V, I_E = 0, T_A = -65°C to +100°C)			0.1	–	0.9	
Emitter Saturation Voltage		$V_{EB1(sat)}$				Volts
(V_{B2B1} = 10 V, I_E = 50 mA) Note 2			–	2.5	4.0	
Modulated Interbase Current		$I_{B2(mod)}$				mA
(V_{B2B1} = 10 V, I_E = 50 mA)			10	15	–	
Emitter Reverse Current		I_{EB2O}				nA
(V_{B2E} = 30 V, I_{B1} = 0)			–	5.0	10	
Peak Point Emitter Current		I_P				μA
(V_{B2B1} = 25 V)	MU4891			0.6	5.0	
	MU4892, MU4893		–	0.6	2.0	
	MU4894		–	0.6	1.0	
Valley Point Current		I_V				mA
(V_{B2B1} = 20 V, R_{B2} = 100 Ohms) Note 2						
	MU4891, MU4893, MU4894		2.0	4.0	–	
	MU4892		2.0	3.0	–	
Base-One Peak Pulse Voltage		V_{OB1}				Volts
(Note 3, Figure 3)						
	MU4891, MU4892, MU4894		3.0	5.0	–	
	MU4893		6.0	8.0	–	

NOTES

1. Intrinsic standoff ratio.
   η is defined by equation:
   $$\eta = \frac{V_P - V_{(EB1)}}{V_{B2B1}}$$
   Where V_P = Peak Point Emitter Voltage
   V_{B2B1} = Interbase Voltage
   $V_{(EB1)}$ = Emitter to Base-One Junction Diode Drop (≈0.5 V @ 10 μA)

2. Use pulse techniques: PW ≈ 300 μs duty cycle ≤2% to avoid internal heating due to interbase modulation which may result in erroneous readings.

3. Base-One Peak Pulse Voltage is measured in circuit of Figure 3. This specification is used to ensure minimum pulse amplitude for applications in SCR firing circuits and other types of pulse circuits.

FIGURE 1 — UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

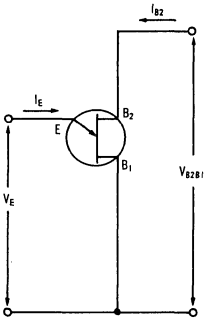


FIGURE 2 — STATIC EMITTER CHARACTERISTICS CURVES

(Exaggerated to Show Details)

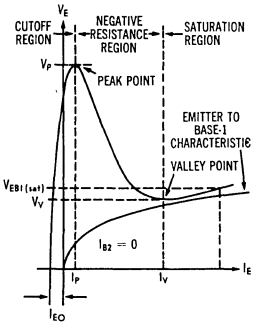
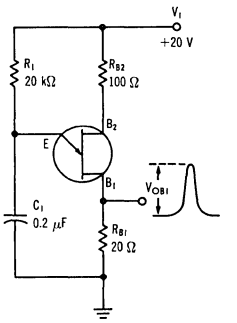


FIGURE 3 — V_{OB1} TEST CIRCUIT

(Typical Relaxation Oscillator)



7

S2800 series

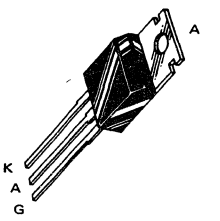
REVERSE BLOCKING TRIODE THYRISTORS

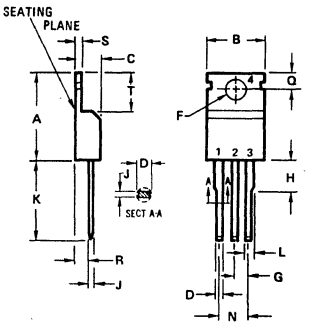
. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Blocking Voltage to 600 Volts

SILICON CONTROLLED RECTIFIERS

10 AMPERES RMS
100–600 VOLTS





PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO-220 AB
All JEDEC dimensions and notes apply

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Voltage (1) Peak Repetitive Off-State Voltage (1)	V_{RRM} V_{DRM}		Volts
S2800 A		100	
S2800 B		200	
S2800 D		400	
S2800 M		600	
Non-Repetitive Peak Reverse Voltage Non-Repetitive Off-State Voltage	V_{RSM} V_{DSM}		Volts
S2800 A		125	
S2800 B		250	
S2800 D		500	
S2800 M		700	
RMS Forward Current (All Conduction Angles) $T_C = 75^oC$	$I_{T(RMS)}$	10	Amps
Peak Forward Surge Current (1 Cycle, Sine Wave, 60 Hz, $T_C = 80^oC$)	I_{TSM}	100	Amps
Circuit Fusing Considerations ($T_J = -65$ to $+100^oC$, t = 1.0 to 8.3 ms)	I^2t	40	A^2s
Forward Peak Gate Power ($t \leq 10\ \mu s$)	P_{GM}	16	Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5	Watt
Operating Junction Temperature Range	T_J	-40 to +100	^oC
Storage Temperature Range	T_{stg}	-40 to +150	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	$^oC/W$

(1) V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode.

▲Trademark of Motorola Inc.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (V_D = Rated V_{DRM}, T_C = 100°C)	I_{DRM}	–	–	2	mA
Peak Reverse Blocking Current (V_R = Rated V_{RRM}, T_C = 100°C)	I_{RRM}	–	–	2	mA
Instantaneous On-State Voltage (I_{TM} = 30 A Peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%)	V_T	–	1.7	2	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 Vdc, R_L = 30 Ohms)	I_{GT}	–	8	15	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 Vdc, R_L = 30 Ohms)	V_{GT}	–	0.9	1.5	Volts
Holding Current (Gate Open, V_D = 12 Vdc, I_T = 150 mA)	I_H	–	10	20	mA
Gate Controlled Turn-on Time (V_D = Rated V_{DRM}, I_{TM} = 2 A, I_{GR} = 80 mA)	t_{gt}	–	1.6	–	μs
Circuit Commutated Turn-Off Time (V_D = V_{DRM}, I_{TM} = 2 A, Pulse Width = 50 μs, dv/dt = 200 V/μs, di/dt = 10 A/μs, T_C = 75°C)	tq	–	25	–	μs
Critical Rate-of-Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Rise, T_C = 100°C)	dv/dt	–	100	–	V/μs

FIGURE 1 – CURRENT DERATING

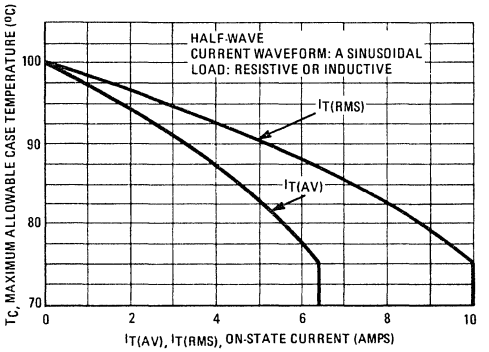
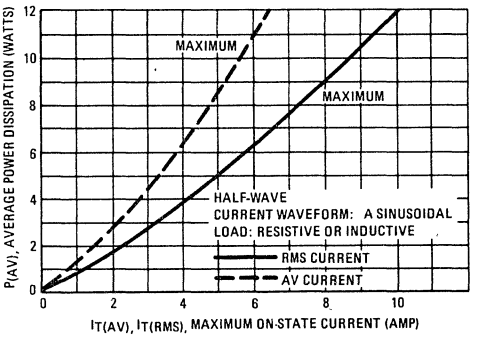


FIGURE 2 – POWER DISSIPATION



7

S6200
S6210
S6220
series

REVERSE BLOCKING TRIODE THYRISTOR

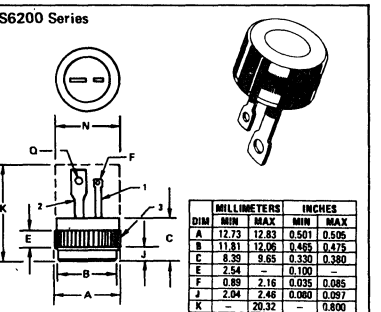
. . . designed for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current – I_{TSM} = 200 Amp
- Low Forward "On" Voltage – 1.2 V (Typ) @ I_{TM} = 20 Amp
- Practical Level Triggering and Holding Characteristics – 10 mA (Typ) @ T_C = 25°C
- Rugged Construction in Either Pressfit, Stud or Isolated Stud Package
- Glass Passivated Junctions for Maximum Reliability

SILICON CONTROLLED RECTIFIER

20 AMPERES RMS
100 thru 600 VOLTS

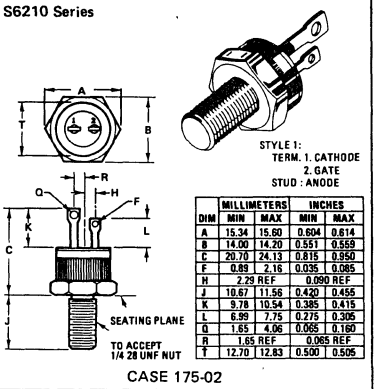
S6200 Series



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	12.73	12.83	0.501	0.505
B	11.81	12.06	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54	–	0.100	–
F	0.89	2.16	0.035	0.085
J	2.04	2.46	0.080	0.097
K	–	20.32	–	0.800
N	–	12.95	–	0.510
Q	1.65	4.06	0.065	0.160

CASE 174-03

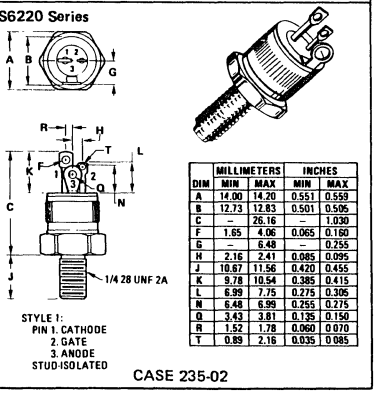
S6210 Series



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	0.89	2.16	0.035	0.085
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	1.65	4.06	0.065	0.160
R	1.65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505

CASE 175-02

S6220 Series



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	26.16	–	1.030
F	1.65	4.06	0.065	0.160
G	–	6.48	–	0.255
H	2.16	2.41	0.085	0.095
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
N	6.48	6.99	0.255	0.275
Q	3.43	3.81	0.135	0.150
R	1.52	1.78	0.060	0.070
T	0.89	2.16	0.035	0.085

CASE 235-02

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Peak Repetitive Forward and Reverse Voltage (1)		V_{DRM} or		Volts
S6200, S6210, S6220	A	V_{RRM}	100	
S6200, S6210, S6220	B		200	
S6200, S6210, S6220	D		400	
S6200, S6210, S6220	M		600	
Non-Repetitive Peak Forward and Reverse Voltage (1)		V_{DSM} or		Volts
S6200, S6210, S6220	A	V_{RSM}	150	
S6200, S6210, S6220	B		250	
S6200, S6210, S6220	D		500	
S6200, S6210, S6220	M		700	
RMS On-State Current (T_C = 75°C)		$I_{T(RMS)}$	20	Amp
Peak Non-Repetitive Surge Current (One Full cycle of surge current at 60 Hz, preceded and followed by rated current, T_C = 75°C)		I_{TSM}	200	Amp
Circuit Fusing (T_J = -65 to +100°C) (t = 1.0 to 8.3 ms)		I^2t	170	A^2s
Peak Gate Power (10 μs Max)		P_{GM}	40	Watts
Average Gate Power		$P_{G(AV)}$	0.5	Watt
Operating Junction Temperature Range		T_J	-65 to +100	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C
Stud Torque		–	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case S6200, S6210	$R_{\theta JC}$	1.2	°C/W
S6220		1.4	

(1) Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Instantaneous Forward Breakover Voltage (Gate Open, T_C = 100°C)		$V_{(BO)O}$				Volts
S6200, S6210, S6220	A		100	–	–	
S6200, S6210, S6220	B		200	–	–	
S6200, S6210, S6220	D		400	–	–	
S6200, S6210, S6220	M		600	–	–	
Peak Blocking Current (Rated V_{DRM} or V_{RRM}, T_C = 100°C)		I_{DRM} or I_{RRM}	–	–	2	mA
Peak On-State Voltage (I_{TM} = 100 A Peak)		V_T	–	–	2.4	Volts
Gate Trigger Current, Continuous dc (V_D = 12 Vdc, R_L = 30 Ohms)		I_{GT}	–	–	15	mA
Gate Trigger Voltage, Continuous dc (V_D = 12 Vdc, R_L = 30 Ohms)		V_{GT}	–	–	2	Volts
Holding Current (Initiating Current = 150mA, V_D = 12 V, Gate Open)		I_H	–	–	20	mA
Critical Rate-of-Rise of Off-State Voltage (V_D = V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 100°C)		dv/dt				V/μs
S6200, S6210, S6220	A,D		10	100	–	
S6200, S6210, S6220	B		10	100	–	
S6200, S6210, S6220	M		10	75	–	
Gate Controlled Turn-On Time (V_D = Rated V_{DRM}, I_T = 30 A Peak, I_{GT} = 200 mA, Rise Time = 0.1 μs		t_{gt}	–	2	–	μs
Circuit Commutated Turn-off Time (V_D = Rated V_{DM}, I_T = 18 A, t_p = 50 μs dv/dt = 10 V/μs, di/dt = 30 A/μs, T_C = 75°C)		t_q	–	30	–	μs

7

FIGURE 1 – CURRENT DERATING

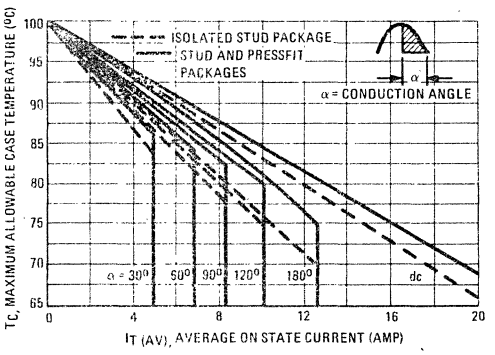
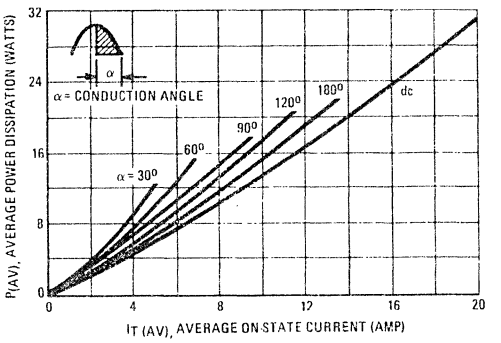


FIGURE 2 – POWER DISSIPATION



SC136 series

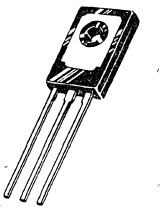
TRIACS

3 AMPERES RMS
200–600 VOLTS

BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies.

- Low Off-State Leakage Currents
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Rugged Industry Proven Thermopad△ Construction
- TO-5 Lead Form Available



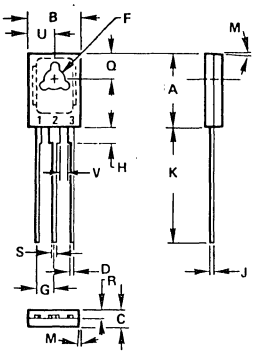
MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Peak Repetitive Off-State Voltage (T_C = 110°C)		V_{DRM}		Volts
	B		200	
	C		300	
SC136	D		400	
	E		500	
	M		600	
RMS On-State Current (T_C = 65°C)		$I_{T(RMS)}$	3.0	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)		I_{TSM}	30	Amp
Circuit Fusing (t = 1 to 8.3 ms)		I^2t	3.6	A^2s
Critical Rate of Rise of On-State Current		di/dt	5.0	A/μs
Peak Gate Power		P_{GM}	5.0	Watts
Average Gate Power		$P_{G(AV)}$	0.1	Watt
Peak Gate Voltage		V_{GM}	5.0	Volts
Operating Junction Temperature Range		T_J	-40 to +110	°C
Storage Temperature Range		T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	°C/W
Junction to Ambient	$R_{\theta JA}$	75	°C/W

△Trademark of Motorola Inc.



STYLE 7
PIN 1 MT1
2 GATE
3 MT2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

CASE 77-04
TO-126

7

***ELECTRICAL CHARACTERISTICS** (T_C = +25°C, either polarity of MT2 to MT1 voltage, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Off-State Current		I_{DRM}				μA
(V_D = Rated V_{DRM}, Gate Open)	T_C = +25°C		–	–	10	
	T_C = +110°C		–	–	500	
Peak On-State Voltage		V_{TM}	–	–	1.8	Volts
(I_{TM} = 5A, Pulse Width = 1 ms, Duty Cycle < 2%)						
DC Gate Trigger Current		I_{GT}				mAdc
(V_D = 6 Vdc, R_L = 50 Ohms)						
MT2 (+), G (+); MT2 (–), G (–); MT2 (+), G (–)	T_C = 25°C		–	–	25	
(V_D = 12 Vdc, R_L = 50 Ohms)						
MT2 (+), G (+); MT2 (–), G (–), MT2 (+) G (–)	T_C = –40°C		–	–	50	
DC Gate Trigger Voltage		V_{GT}				Vdc
(V_D = 12 Vdc, R_L = 50 Ohms)						
MT2 (+), G (+); MT2 (–), G (–); MT2 (+), G (–)	T_C = 25°C		–	–	2.0	
	T_C = –40°C		–	–	3.0	
(V_D = Rated V_{DRM}, All Modes)	T_C = 110°C		0.2	–	–	
Holding Current		I_H				mAdc
(V_D = 24 Vdc, R_L = 200 Ohms, Gate Open)						
	T_C = 25°C		–	–	50	
	T_C = –40°C		–	–	100	
Latching Current		I_L				mAdc
(V_D = 24 Vdc)						
Trigger Source: 5 V, 50 Ohms,	T_C = 25°C					
MT2 (+), G (+); MT2 (–), G (–);			–	–	50	
MT2 (+), G (–)			–	–	100	
Trigger Source: 10 V, 50 Ohms,	T_C = –40°C					
MT2 (+), G (+); MT2 (–), G (–);			–	–	100	
MT2 (+), G (–)			–	–	200	
Critical Rate-of-Rise of Off-State Voltage		dv/dt				Volts/μs
(V_D = Rated V_{DRM}, Gate Open)	T_C = 110°C		–	15	–	
Critical Rate-of-Rise of Commutating Voltage		dv/dt(c)				Volts/μs
(V_D = Rated V_{DRM}, $I_{T(RMS)}$ = 3 A,						
di/dt = 1.6 A/ms, Gate Open)	T_C = 65°C		–	5	–	

7

FIGURE 1 – RMS CURRENT DERATING

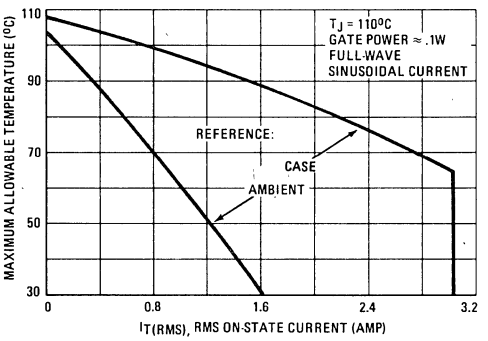
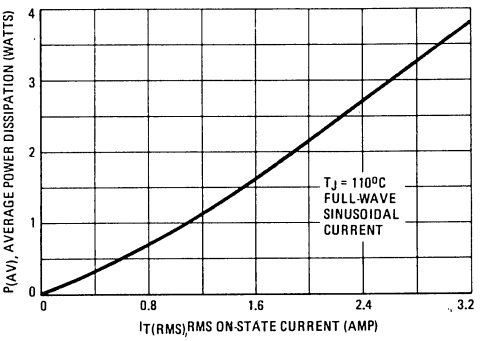


FIGURE 2 – MAXIMUM POWER DISSIPATION



SC141
SC146

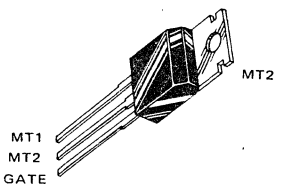
TRIACS

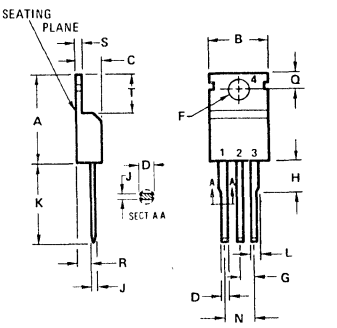
6 AND 10 AMPERES RMS
200–600 VOLTS

BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies.

- Triggering Specified in Three Quadrants
- Blocking Voltage to 600 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability





STYLE 2.
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO-220 AB
All JEDEC dimensions and notes apply

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Peak Repetitive Off-State Voltage, Gate Open,		V_{DRM}		Volts
	B		200	
SC141	D		400	
SC146	E		500	
	M		600	
RMS On-State Current		$I_{T(RMS)}$		Amp
$T_C = 80^oC$	SC141		6	
	SC146		10	
Peak Non-Repetitive Surge Current		I_{TSM}		Amp
One Full Cycle, 60 Hz	SC141		80	
	SC146		120	
Circuit Fusing Considerations		I^2t		A^2s
t = 8.3 ms	SC141		26.5	
	SC146		60	
Peak Gate Power (Pulse Width = 10 μs)		P_{GM}	10	Watts
Average Gate Power ($T_C = +80^oC$, t = 8.3 ms)		$P_{G(AV)}$	0.5	Watt
Peak Gate Current (Pulse Width = 10 μs)		I_{GM}	3.5	Amp
Peak Gate Voltage		V_{GM}	10	Volts
Operating Junction Temperature Range		T_J	-40 to +100	^oC
Storage Temperature Range		T_{stg}	-40 to +125	^oC

THERMAL CHARACTERISTICS

Characteristic		Symbol	Max	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$		$^oC/W$
	SC141		2.2	
	SC146		1.5	

This is advance information and specifications are subject to change without notice.

▲Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = +25°C, Either Polarity of MT2 - to - MT1 Voltage unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current	I_{DRM}				mA
V_D = Rated V_{DRM} |					
Gate Open-Circuited T_C = +25°C		–	–	0.1	
T_C = +100°C		–	–	0.5	
Peak On-State Voltage	V_{TM}				Volts
Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%.					
SC141 I_{TM} = 8.5 A Peak		–	–	1.83	
SC146 I_{TM} = 14 A Peak		–	–	1.65	
Critical Rate of Rise of Off-State Voltage	dv/dt	–	50	–	Volts/μs
V_D = Rated V_{DRM}, Gate Open-Circuited, Exponential Waveform T_C = +100°C					
Critical Rate-of-Rise of Commutating Off-State Voltage (1)	dv/dt(c)				Volts/μs
$I_{T(RMS)}$ = Rated $I_{T(RMS)}$, V_D = Rated V_{DRM}, T_C = +80°C					
Gate Open-Circuited					
SC141 Commutating di/dt = 3.2 A/ms		4	–	–	
SC146 Commutating di/dt = 5.4 A/ms		4	–	–	
DC Gate Trigger Current	I_{GT}				mAdc
V_D = 12 Vdc, Trigger Mode					
MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 100 Ohms		–	–	50	
MT2 (+), Gate (–); R_L = 50 Ohms		–	–	50	
MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 50 Ohms T_C = –40°C		–	–	80	
MT2 (+), Gate (–); R_L = 25 Ohms; T_C = –40°C		–	–	80	
DC Gate Trigger Voltage	V_{GT}				Vdc
V_D = 12 Vdc, Trigger Mode					
MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 100 Ohms		–	–	2.5	
MT2 (+), Gate (–); R_L = 50 Ohms		–	–	2.5	
MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 50 Ohms T_C = –40°C		–	–	3.5	
MT2 (+), Gate (–); R_L = 25 Ohms; T_C = –40°C		–	–	3.5	
V_D = Rated V_{DRM}; R_L = 1000 Ohms; All Polarities T_C = +100°C		0.2	–	–	
Holding Current	I_H				mAdc
V_D = 24 Vdc, I_T = 0.5A					
Pulse Width = 1 ms, Duty Cycle ≤ 2%.					
Gate Trigger Source = 7 V, 20 Ohms T_C = +25°C		–	–	50	
T_C = –40°C		–	–	100	
Latching Current	I_L				mAdc
V_D = 24 Vdc					
Gate Trigger Source = 15 V, 100 Ohms, Trigger Mode					
MT2 (+), Gate (+); MT2 (–), Gate (–)		–	–	100	
MT2 (+), Gate (–)		–	–	200	
MT2 (+), Gate (+); MT2 (–), Gate (–); T_C = –40°C		–	–	200	
MT2 (+), Gate (–); T_C = –40°C		–	–	400	

FIGURE 1 – RMS CURRENT DERATING

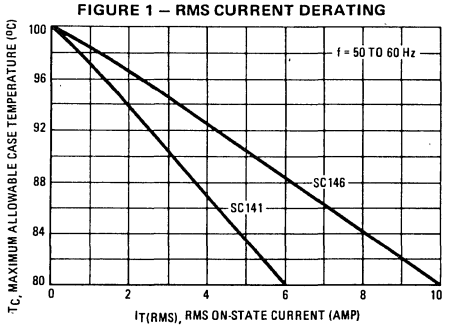
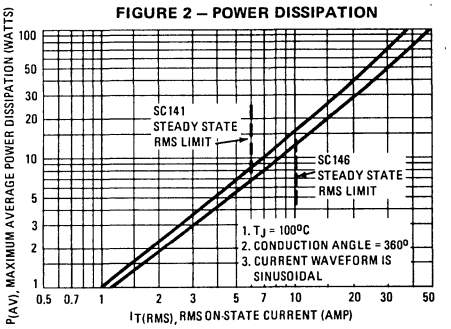


FIGURE 2 – POWER DISSIPATION



SC245
SC245( )3
SC246

TRIACS

10 AMPERES RMS
200-600 VOLTS

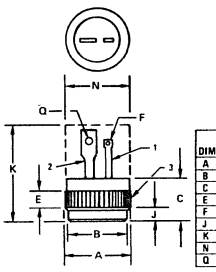
BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for industrial and military applications for the fullwave control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems.

- All Diffused and Glass Passivated Junctions for Greater Stability
- Gate Triggering Guaranteed In All 4 Quadrants
- Three Package Choices
  - Pressfit – SC245 Series
  - Stud – SC246 Series
  - Isolated Stud – SC245 ( ) 3 Series

SC246
PRESS FIT

STYLE 3:
TERM 1. GATE
2. MAIN TERMINAL 1
3. MAIN TERMINAL 2

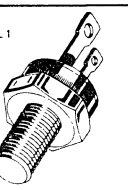


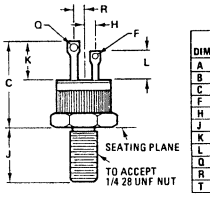
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
B	11.81	12.06	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54	–	0.100	–
F	0.89	2.16	0.035	0.085
J	2.04	2.46	0.080	0.097
K	–	20.32	–	0.800
N	–	12.95	–	0.510
Q	1.65	4.06	0.065	0.160

CASE 174-03

SC245
STUD

STYLE 3
TERM 1 MAIN TERMINAL 1
2 GATE
STUD MAIN TERMINAL 2



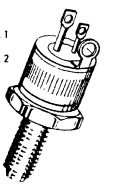


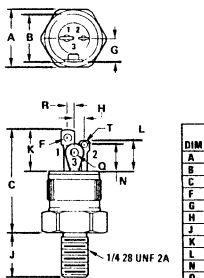
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	0.89	2.16	0.035	0.085
H	2.29 REF		0.09	REF
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	1.65	4.06	0.065	0.160
R	1.65 REF		0.065	REF
T	12.70	12.83	0.500	0.505

CASE 175-02

SC245( )3
ISOLATED
STUD

STYLE 2
PIN 1 MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2
STUD ISOLATED





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	26.16	–	1.030
F	1.65	4.06	0.065	0.160
G	–	6.48	–	0.255
H	2.16	2.41	0.085	0.095
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
N	6.48	6.99	0.255	0.275
Q	3.43	3.81	0.135	0.150
R	1.52	1.78	0.060	0.070
T	0.89	2.16	0.035	0.085

CASE 235-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (1) T_C = -40°C to +100°C	V_{DRM}		Volts
SC246B, SC245B, SC245B3		200	
SC246D, SC245D, SC245D3		400	
SC246E, SC245E, SC245E3		500	
SC246M, SC245M, SC245M3		600	
RMS On-State Current	$I_{T(RMS)}$	10	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	100	Amp
Circuit Fusing Considerations	I^2t		A^2s
t = 1 ms		20	
t = 8.3 ms		41.5	
Peak Gate Power	P_{GM}	10	Watts
Average Gate Power	$P_{G(AV)}$	0.5	Watt
Operating Junction Temperature Range	T_J	-40 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +125	°C
Stud Torque	–	30	in. lb.

THERMAL CHARACTERISTICS

Character	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R\Theta_{JC}$		°C/W
Pressfit and Stud		2.0	
Isolated Stud		2.15	

ELECTRICAL CHARACTERISTICS (T_C = +25°C, either polarity of MT2 to MT1 unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current Rated V_{DRM} = Peak Off-State Voltage, Gate Open-Circuited T_C = +25° T_C = +100°C	I_{DRM}	 – –	 – –	 0.1 0.5	mA
Peak On-State Voltage I_{TM} = 14 A Peak, Pulse Width = 1 ms, Duty Cycle ≤ 2%.	V_{TM}	–	–	1.65	Volts
Critical Rate of Rise of Off-State Voltage Rated V_{DRM}, Gate Open-Circuited, Exponential Waveform T_C = +100°C	dv/dt	–	50	–	Volts/μs
Critical Rate-of-Rise of Commutating Off-State Voltage $I_{T(RMS)}$ = Rated RMS On-State Current V_{DRM} = Rated Peak Off-State Voltage, Gate Open-Circuited, Commutating di/dt = 5.4 A/ms T_C = +78.5°C	dv/dt(c)	4	–	–	Volts/μs
DC Gate Trigger Current V_D = 12 Vdc MT2 (+),Gate (+); MT2 (–), Gate (–); RL = 100Ω MT2 (+), Gate (–); RL = 50Ω MT2 (+), Gate (+); MT2 (–), Gate (–) RL = 50Ω, T_C = –40°C MT2 (+), Gate (–) RL = 25Ω, T_C = –40°C	I_{GT}	 – – – –	 – – – –	 50 50 80 80	mAdc
DC Gate Trigger Voltage V_D = 12 Vdc MT2 (+), Gate (+); MT2 (–), Gate (–); RL = 100Ω MT2 (+), Gate (–) RL = 50Ω MT2 (+), Gate (+); MT2 (–), Gate (–) RL = 50Ω, T_C = –40°C MT2 (+), Gate (–) RL = 25Ω, T_C = –40°C V_D = Rated V_{DRM}, RL = 1 kΩ, T_C = 100°C All Trigger Modes	V_{GT}	 – – – – .2	 – – – – –	 2.5 2.5 3.5 3.5	Vdc
Holding Current Main Terminal Voltage = 24 Vdc, I_T = 0.5A Pulse Width = 0.1 to 10 ms Gate Trigger Source = 7 V, 20 Ohms T_C = +25°C T_C = –40°C	I_H	 – –	 – –	 50 100	mAdc
Latching Current Main Terminal Source Voltage = 24 Vdc, Gate Trigger Source = 15 V, 100 Ohms, Pulse Width = 50 μs, Rise and Fall Times maximum = 5 μs Trigger Mode MT2 (+), Gate (+); MT2 (–), Gate (–); T_C = 25°C MT2 (+), Gate (–) MT2 (+), Gate (+); MT2 (–), Gate (–); T_C = –40°C MT2 (+), Gate (–)	I_L	 – – – –	 – – – –	 100 200 200 400	mAdc

FIGURE 1 – CURRENT DERATING

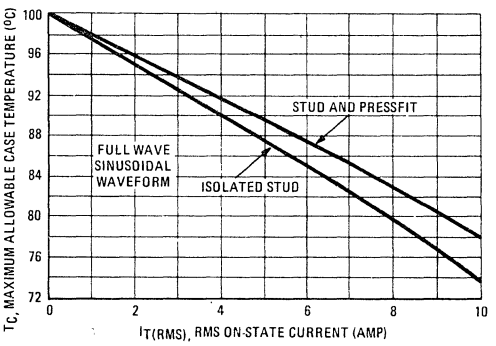
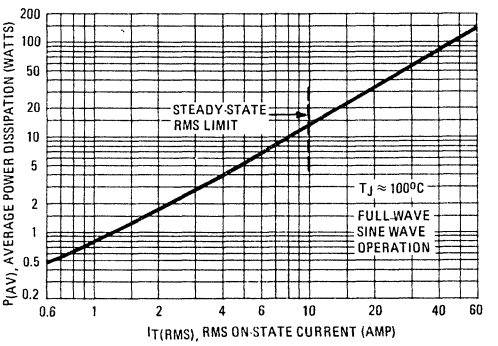


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION



SC250
SC250( )3
SC251

TRIACS

15 AMPERES RMS
200–600 VOLTS

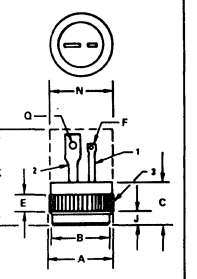
BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- All Diffused and Glass Passivated Junctions for Greater Stability
- Pressfit, Stud and Isolated Stud Packages
- Gate Triggering Guaranteed In All 3 Quadrants

SC251
PRESS FIT

STYLE 3:
TERM. 1. GATE
2. MAIN TERMINAL 1
3. MAIN TERMINAL 2

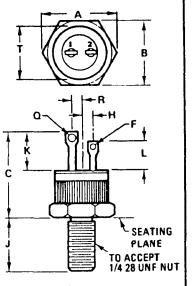


DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	12.73	12.83	0.501	0.505
B	11.81	12.06	0.465	0.475
C	8.39	9.65	0.330	0.380
E	2.54	–	0.100	–
F	0.89	2.16	0.035	0.085
J	2.04	2.46	0.080	0.097
K	–	20.32	–	0.800
N	–	12.95	–	0.510
Q	1.65	4.06	0.065	0.160

CASE 174-03

SC250
STUD

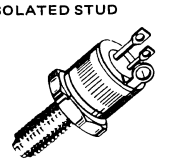
STYLE 3
TERM. 1. MAIN TERMINAL 1
2. GATE
STUD. MAIN TERMINAL 2



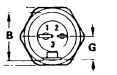
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	0.89	2.16	0.035	0.085
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	1.65	4.06	0.065	0.160
R	1.65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505

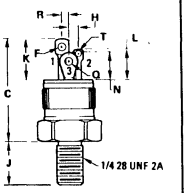
CASE 175-02

SC250( )3
ISOLATED STUD



STYLE 2.
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2
STUD ISOLATED





DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	26.16	–	1.030
F	1.65	4.06	0.065	0.160
G	–	6.48	–	0.255
H	2.16	2.41	0.085	0.095
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
N	6.48	6.99	0.255	0.275
Q	3.43	3.81	0.135	0.150
R	1.52	1.78	0.060	0.070
T	0.89	2.16	0.035	0.085

CASE 235-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage SC251B, SC250B, SC250B3 SC251D, SC250D, SC250D3 SC251E, SC250E, SC250E3 SC251M, SC250M, SC250M3	V_{DRM}	 200 400 500 600	Volts
RMS On-State Current	$I_{T(RMS)}$	15	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	100	Amp
Circuit Fusing Considerations t = 1 ms t = 8.3 ms	I^2t	 20 41.5	A^2s
Peak Gate Power	P_{GM}	10	Watts
Average Gate Power	$P_{G(AV)}$	0.5	Watt
Peak Gate Power (Pulse Width = 10 μs)	I_{GM}	2	Amp
Operating Junction Temperature Range	T_J	-40 to +115	°C
Storage Temperature Range	T_{stg}	-40 to +125	°C
Stud Torque	–	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case SC250, SC251 SC250 ( )3	$R_{\theta JC}$	 2 2.3	°C/W

This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS

(T_C = +25°C unless otherwise noted. Values apply for either polarity of Main Terminal 2 Characteristics referenced to Main Terminal 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current	I_{DRM}				mA
V_D = Rated V_{DRM}					
Gate Open-Circuited T_C = +25°C		–	–	0.1	
T_C = +115°C		–	–	0.5	
Peak On-State Voltage	V_{TM}	–	–	1.65	Volts
I_{TM} = 21 A, Pulse Width = 1 ms, Duty Cycle ≤ 2%.					
Critical Rate of Rise of Off-State Voltage	dv/dt	100	–	–	Volts/μs
Rated V_{DRM}, Gate Open-Circuited,					
Exponential Waveform, T_C = +115°C					
Critical Rate-of-Rise of Commutating Off-State Voltage (1)	dv/dt(C)				Volts/μs
$I_{T(RMS)}$ = Rated RMS On-State Current, V_D = V_{DRM}					
Gate Open-Circuited, Commutating di/dt = 8 A/ms					
SC250, SC251 T_C = +84°C		4	–	–	
SC250( )3 T_C = +78°C		4	–	–	
DC Gate Trigger Current	I_{GT}				mAdc
V_D = 12 Vdc					
MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 100 Ohms		–	–	50	
MT2 (+), Gate (–); R_L - 50 Ohms		–	–	50	
DC Gate Trigger Current	I_{GT}				mAdc
V_D = 12 Vdc, T_C = -40°C					
MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 50 Ohms		–	–	80	
MT2 (+), Gate (–); R_L = 25 Ohms		–	–	80	
DC Gate Trigger Voltage	V_{GT}				Vdc
V_D = 12 Vdc					
MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 100 Ohms		–	–	2.5	
MT2 (+), Gate (–); R_L = 50 Ohms		–	–	2.5	
DC Gate Trigger Voltage	V_{GT}				Vdc
V_D = 12 Vdc, T_C = -40°C					
MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 50 Ohms		–	–	3.5	
MT2 (+), Gate (–); R_L = 25 Ohms		–	–	3.5	
DC Gate Non-Trigger Voltage	V_{GD}				Vdc
V_D = Rated V_{DRM}, R_L - 1K Ohms, T_C = 115°C		0.20	–	–	
All Trigger Modes					
Holding Current	I_H				mAdc
V_D = 24 Vdc, Peak Initiating Current = 0.5 A,					
Pulse Width = 0.1 to 10 ms, Gate Trigger					
Source = 7 V, 20 Ohms					
T_C = +25°C		–	–	50	
T_C = -40°C		–	–	100	
Latching Current	I_L				mAdc
V_D = 24 Vdc, Gate Trigger Source = 15 V, 100 Ohms,					
Pulse Width = 50 μs, 5 μs Maximum Rise and Fall Times					
MT2 (+), Gate (+); MT2 (–), Gate (–);					
MT2 (+), Gate (–) T_C = 25°C		–	–	100	
MT2 (+), Gate (+); MT2 (–), Gate (–);					
MT2 (+), Gate (–) T_C = -40°C		–	–	200	

FIGURE 1 – CURRENT DERATING

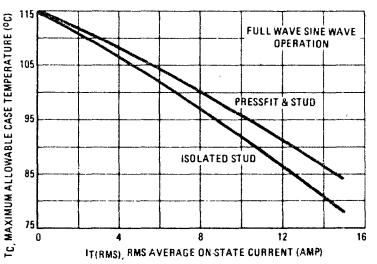
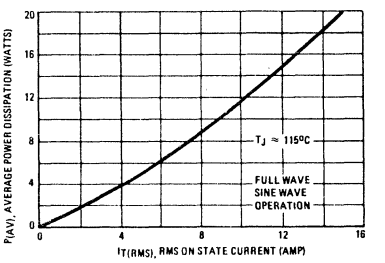


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION



SC260
SC260( )3
SC261

TRIACS

25 AMPERES RMS
200–600 VOLTS

BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- All Diffused and Glass Passivated Junctions for Greater Stability
- Pressfit, Stud and Isolated Stud Packages
- Gate Triggering Guaranteed In All 3 Quadrants

MAXIMUM RATINGS

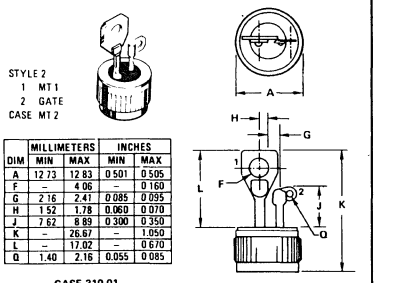
Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage T_C = -40°C to +115°C SC260B, SC260B3, SC261B SC260D, SC260D3, SC261D SC260E, SC260E3, SC261E SC260M, SC260M3, SC261M	V_{DRM}	 200 400 500 600	Volts
RMS On-State Current	$I_{T(RMS)}$	25	Amp
Peak Non-Repetitive Surge Current (One Cycle, 60 Hz)	I_{TSM}	250	Amp
Circuit Fusing Considerations t = 1.0 ms t = 8.3 ms	I^2t	 150 260	A^2s
Peak Gate Power (Pulse Width = 10 μs)	P_{GM}	10	Watts
Average Gate Power	$P_{G(AV)}$	0.5	Watt
Peak Gate Current	I_{GM}	2	Amp
Operating Junction Temperature Range	T_J	-40 to +115	°C
Storage Temperature Range	T_{stg}	-40 to +125	°C
Stud Torque	–	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case SC260, SC261 SC260( )3	$R_{\theta JC}$	 1.8 1.95	°C/W

This is advance information and specifications are subject to change without notice.

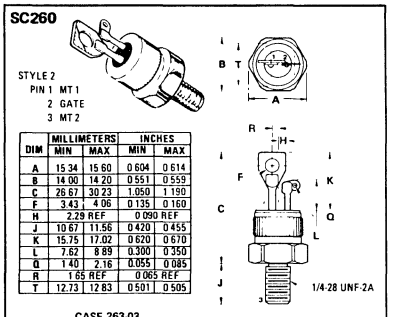
SC261



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	12.73	12.83	0.501	0.505
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.52	1.78	0.060	0.070
J	7.62	8.89	0.300	0.350
K	–	26.67	–	1.050
L	–	17.02	–	0.670
Q	1.40	2.16	0.055	0.085

CASE 310-01

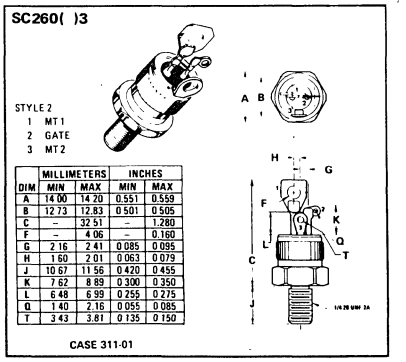
SC260



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

CASE 263-03

SC260( )3



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	32.51	–	1.280
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.60	2.01	0.063	0.079
J	10.67	11.56	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6.48	6.99	0.255	0.275
Q	1.40	2.16	0.055	0.085
T	3.43	3.81	0.135	0.150

CASE 311-01

7

ELECTRICAL CHARACTERISTICS

(T_C = +25°C unless otherwise noted. Values apply for either polarity of Main Terminal 2 characteristics referenced to Main Terminal 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current	I_{DRM}				mA
V_D = Rated V_{DRM} = Peak Off-State Voltage,					
Gate Open-Circuited T_C = +25°C		–	–	0.2	
T_C = +115°C		–	–	1	
Peak On-State Voltage	V_{TM}	–	–	1.58	Volts
I_{TM} = 35 A Peak, Pulse Width = 1 ms, Duty Cycle ≤ 2%.					
Critical Rate of Rise of Off-State Voltage	dv/dt	50	–	–	Volts/μs
Rated V_{DRM}, Gate Open-Circuited,					
Exponential Waveform T_C +115°C					
Critical Rate-of-Rise of Commutating Off-State Voltage	dv/dt(c)	5	–	–	Volts/μs
$I_{T(RMS)}$ = Rated RMS On-State Current					
V_{DRM} = Rated Peak Off-State Voltage,					
Gate Open-Circuited, Commutating di/dt - 13.5 A/ms,					
T_C = +80°C					
DC Gate Trigger Current	I_{GT}				mAdc
V_D = 12 Vdc					
MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 100 Ohms		–	–	50	
MT2 (+), Gate (–); R_L = 50 Ohms		–	–	50	
DC Gate Trigger Current	I_{GT}				
V_D = 12 Vdc, T_C = –40°C					
MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 50 Ohms		–	–	80	
MT2 (+), Gate (–); R_L = 25 Ohms		–	–	80	
DC Gate Trigger Voltage	V_{GT}				Vdc
V_D = 12 Vdc					
MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 100 Ohms		–	–	2.5	
MT2 (+), Gate (–); R_L = 50 Ohms		–	–	2.5	
DC Gate Trigger Voltage	V_{GT}				Vdc
V_D = 12 Vdc, T_C = –40°C					
MT2 (+), Gate (+); MT2 (–), Gate (–); R_L = 50 Ohms		–	–	3.5	
MT2 (+), Gate (–); R_L = 25 Ohms		–	–	3.5	
DC Gate Non-Trigger Voltage	V_{GD}	0.25	–	–	Vdc
V_D = Rated V_{DRM}, R_L = 1K Ohms, T_C = 115°C					
All Trigger Modes					
Holding Current	I_H				mAdc
V_D = 24 Vdc, Peak Initiating Current = 0.5A,					
Pulse Width = 0.1 to 10 ms, Gate Trigger Source = 7 V, 20 Ohms					
T_C = 25°C		–	–	75	
T_C = –40°C		–	–	100	
Latching Current	I_L				mAdc
V_D = 24 Vdc, Gate Trigger Source = 15 V, 100 Ohms,					
Pulse Width = 50 μs, 5 μs Maximum Rise and Fall Times					
MT2 (+), Gate (+); MT2 (–), Gate (–) T_C = 25°C		–	–	100	
MT2 (+), Gate (–) T_C = 25°C		–	–	200	
MT2 (+), Gate (+); MT2 (–), Gate (–); T_C = –40°C		–	–	200	
MT2 (+), Gate (–) T_C = –40°C		–	–	400	

FIGURE 1 – CURRENT DERATING

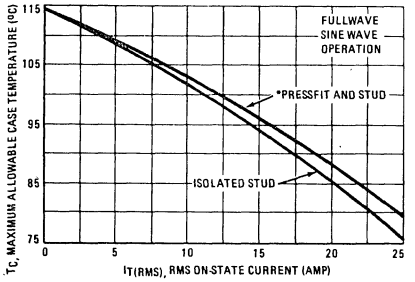
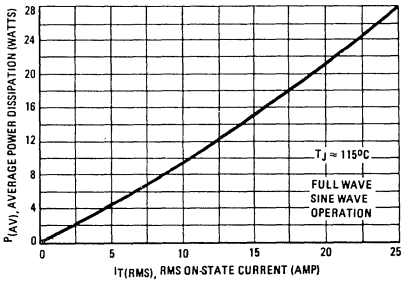


FIGURE 2 – MAXIMUM ON-STATE POWER DISSIPATION



T2300P
T2301P
T2302P
series

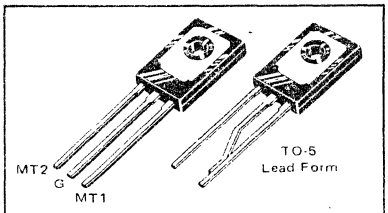
SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for full-wave ac control applications such as light dimmers, motor controls, heating controls and power supplies; or, wherever full-wave silicon-gate-controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Sensitive Gate Triggering Uniquely Compatible for Direct Coupling to TTL, HTL, CMOS and Operational Amplifier Integrated Circuit Logic Functions
- TO-5 Lead Form Available for Economical Replacement of T2300, T2301, and T2302 Series of Metal Triacs
- Blocking Voltages to 600 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small Rugged Thermopad▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability

SENSITIVE GATE TRIACS

2.5 AMPERES RMS
50–600 VOLTS



To order TO-5 lead form, add 5 to part number
For example, T2300PB5

MAXIMUM RATINGS (Apply for T_J = −40 to 100°C unless otherwise noted)

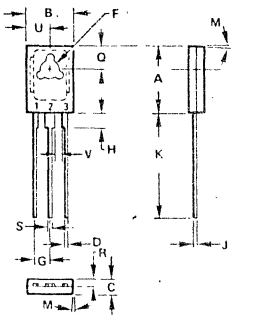
Rating	Suffix	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) T2300P, T2301P, T2302P	F	V_{DRM}	50	Volts
	A		100	
	B		200	
	C		300	
	D		400	
	E		500	
	M		600	
RMS On-State Current (T_C = 70°C)		$I_{T(RMS)}$	2.5	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)		I_{TSM}	25	Amp
Circuit Fusing (t = 8.3 ms)		I^2t	2.6	A^2s
Peak Gate Power (1 μs)		P_{GM}	10	Watts
Average Gate Power		$P_{G(AV)}$	0.15	Watt
Peak Gate Current (1 μs)		I_{GM}	0.5	Amp
Operating Junction Temperature Range		T_J	−40 to +100	°C
Storage Temperature Range		T_{stg}	−40 to +150	°C
Mounting Torque (6-32 Screw), Note 2		—	8.0	in.lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W

NOTES:
1. Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.
2. Torque rating applies with use of torque washer (Shakeproof WD19523 or equivalent). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Main terminal 2 and heat sink contact pad are common.
   For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +200°C. for 10 seconds. Consult factory for lead bending options.

▲Trademark of Motorola Inc.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	30° TYP		30° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.07	—	0.040	

CASE 77-04
TO-126

ELECTRICAL CHARACTERISTICS

(Voltage reference is to main terminal 1. Data applies for either polarity of MT2 to MT1 voltages and for $T_C = 25^oC$ unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Repetitive Off-State Current (V_D = Rated V_{DRM}, Gate Open, $T_C = 100^oC$)	All Types	I_{DRM}	–	–	0.75	mA
Peak On-State Voltage (I_{TM} = 3.5 A, Pulse Width ≈ 1 ms, Duty Cycle ≤ 2%)		V_{TM}	–	–	1.8	Volts
DC Gate Trigger Voltage (All Modes)	All Types	V_{GTM}				Volts
(V_D = 12 V, R_L = 30 Ω)			–	–	2.2	
(V_D = Rated V_{DRM}, R_L = 10 kΩ, $T_C = 100^oC$)			0.15	–	–	
DC Gate Trigger Current (All Modes)		I_{GTM}				mA
(V_D = 12 V, R_L = 30 Ω)	T2300P Series		–	–	3.0	
	T2301P Series		–	–	4.0	
	T2302P Series		–	–	10	
Holding Current		I_H				mA
(V_D = 12 V, I_{TM} = 150 mA, Gate Open)	T2300P, T2301P Series		–	–	5.0	
	T2302P Series		–	–	15	
($T_C = -40^oC$)	T2300P, T2301P Series		–	–	17	
	T2302P Series		–	–	35	
Gate-Controlled Turn-On Time (V_D = Rated V_{DRM}, I_G = 60 mA, I_{TM} = 3.5 A)	All Types	t_{gt}	–	–	2.5	μs
Critical Rate of Rise of Commutating Voltage (V_{DM} = Rated V_{DRM}, $I_{T(RMS)}$ = 2.5 A, di/dt = 0.95 A/ms, Gate Unenergized, $T_C = 70^oC$)	All Types	dv/dt(c)	–	2.0	–	V/μs
Critical Rate of Rise of Off-State Voltage (V_{DM} = Rated V_{DRM}, Exponential Rise, Gate Open)		dv/dt				V/μs
($T_C = 90^oC$)	T2300P, T2301P Series		–	5.0	–	
($T_C = 100^oC$)	T2302P Series		–	10	–	

FIGURE 1 – RMS CURRENT DERATING

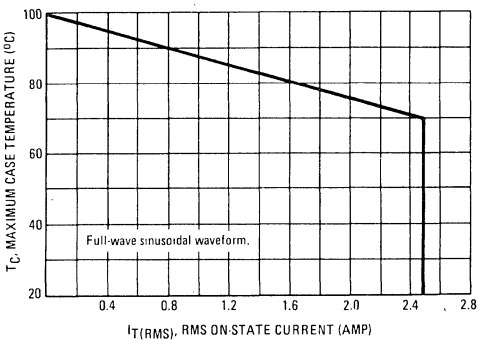


FIGURE 2 – RMS CURRENT DERATING FOR OPERATION WITHOUT HEAT SINK

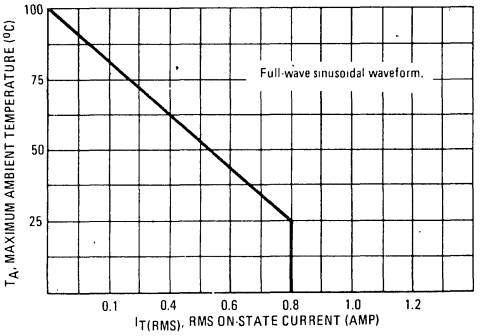
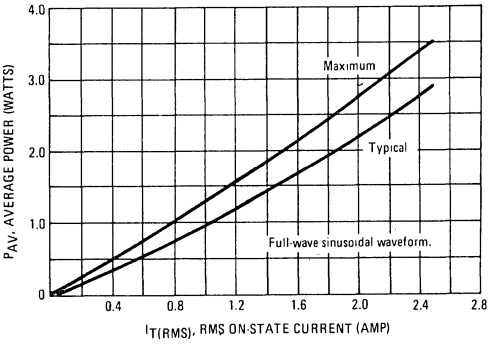


FIGURE 3 – ON-STATE POWER DISSIPATION



T2500

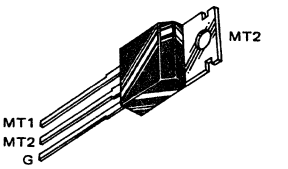
TRIACS

6 AMPERES RMS
200–400 VOLTS

BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies.

- Blocking Voltage to 400 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability

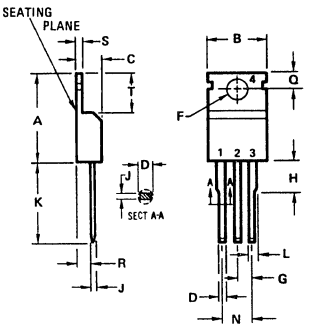


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (T_J = -40 to +100°C) Gate Open T2500 B / D	V_{DROM}	200 / 400	Volts
RMS On-State Current (T_C = +80°C) Full Cycle Sine Wave 50 to 60 Hz	$I_{T(RMS)}$	6	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_C = +80°C)	I_{TSM}	60	Amp
Peak Gate Power (T_C = +80°C, Pulse Width = 1 μs)	P_{GM}	16	Watts
Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.2	Watt
Peak Gate Trigger Current (Pulse Width = 10 μs)	I_{GTM}	4	Amp
Operating Junction Temperature Range	T_J	-40 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.7	°C/W



STYLE 2:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO-220 AB
All JEDEC dimensions and notes apply

▲Trademark of Motorola Inc.

7

ELECTRICAL CHARACTERISTICS (T_C = 25°C and Either Polarity of MT2-to-MT1 Voltage, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current V_D = Rated V_{DRM} @ T_J = 100°C, Gate Open	I_{DRM}	–	–	2	mA
Maximum On-State Voltage (Either Direction) I_{TM} = 30 A Peak	V_{TM}	–	–	2	Volts
Gate Trigger Current, Continuous dc V_D = 12 Vdc, R_L = 12 Ohms	I_{GT}				mA
V_{MT2} (+), V_{G}(+)		–	10	25	
V_{MT2} (+), V_{G}(–)		–	20	60	
V_{MT2} (–), V_{G}(–)		–	15	25	
V_{MT2} (–), V_{G}(+)		–	30	60	
Gate Trigger Voltage, Continuous dc (All Polarities) V_D = 12 Vdc, R_L = 12 Ohms	V_{GT}	–	1.25	2.5	Volts
V_D = V_{DRM}, R_L = 125 Ohms, T_C = 100°C		0.2	–	–	
Holding Current V_D = 12 Vdc, Gate Open Initiating Current = 150 mA, T_C = 25°C	I_{HO}	–	15	30	mA
Gate Controlled Turn-On Time V_D = Rated V_{DRM}, I_T = 10 A, I_{GT} = 160 mA, Rise Time = 0.1 μs	t_{gt}	–	1.6	2.5	μs
Critical Rate of Rise of Commutation Voltage V_D = Rated V_{DRM}, $I_{T(RMS)}$ = 6 A, Commutating di/dt = 3.2 A/ms, Gate Unenergized, T_C = 80°C	dv/dt(c)	–	10	–	V/μs
Critical Rate of Rise of Off-State Voltage V_D = Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 100°C T2500B	dv/dt	100	–	–	V/μs
T2500D		75	–	–	

FIGURE 1 – CURRENT DERATING

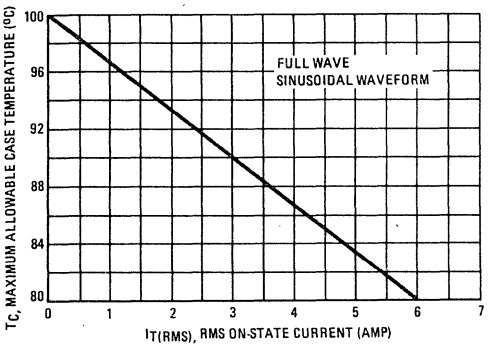
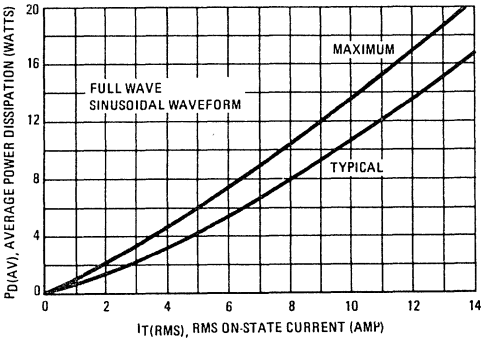


FIGURE 2 – POWER DISSIPATION



T2800
T2802

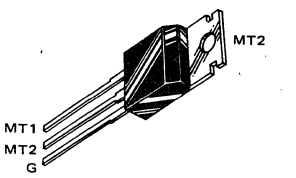
TRIACS

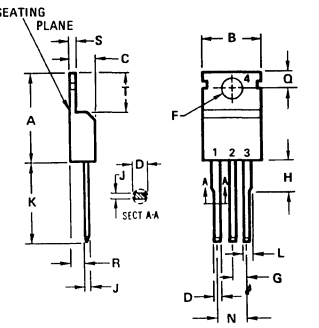
8 AMPERES RMS
200–600 VOLTS

BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies.

- Blocking Voltage to 600 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- T2800 — Four Quadrant Gating
  T2802 — Two Quadrant Gating





STYLE 2:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO-220 AB
All JEDEC dimensions and notes apply

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (1) (T_J = -40 to +100°C) Gate Open	V_{DRM}		Volts
T2800 B		200	
T2800 C		300	
T2802 D		400	
T2802 E		500	
T2802 M		600	
RMS On-State Current (T_C = +80°C) (Conduction Angle = 360°C)	$I_{T(RMS)}$	8	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz, T_J = +80°C)	I_{TSM}	100	Amp
Fusing Current (T_J = -40 to +100°C, t = 1.25 to 10 ms)	I^2t	50	A^2s
Peak Gate Power (Pulse Width = 1 μs)	P_{GM}	16	Watts
Average Gate Power	$P_{G(AV)}$	0.35	Watt
Peak Gate Trigger Current (Pulse Width = 1 μs)	I_{GTM}	4	Amp
Operating Junction Temperature Range	T_J	-40 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W

(1) Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

▲Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current (Either Direction) Rated V_{DRM} @ T_C = 100°C, Gate Open	I_{DRM}	–	–	2	mA
Peak On-State Voltage (Either Direction) I_T = 30 A Peak	V_{TM}	–	1.7	2	Volts
Gate Trigger Current, Continuous dc V_D = 12 Vdc, R_L = 12 Ohms	I_{GT}				mA
V_{MT2} (+), $V_{G(+)}$ T2800		–	10	25	
T2802		–	25	50	
V_{MT2} (+), $V_{G(-)}$ T2800 Only		–	20	60	
V_{MT2} (–), $V_{G(-)}$ T2800		–	15	25	
T2802		–	25	50	
V_{MT2} (–), $V_{G(+)}$ T2800 Only		–	30	60	
Gate Trigger Voltage, Continuous dc (All Polarities) V_D = 12 Vdc, R_L = 100 Ohms	V_{GT}	–	1.25	2.5	Volts
R_L = 125 Ohms, V_D = V_{DRM}, T_C = 100°C		0.2	–	–	
Holding Current (Either Direction) V_D = 12 Vdc, Gate Open, T2800 I_T = 125 mA T2802	I_{HO}	–	15	30	mA
		–	20	60	
Gate Controlled Turn-On Time Rated V_{DROM}, I_T = 10 A, I_{GT} = 80 mA, Rise Time = 0.1 μs	t_{gt}	–	1.6	–	μs
Critical Rate of Rise of Commutation Voltage Rated V_{DRM}, $I_{T(RMS)}$ = 8.0 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = 80°C	dv/dt(c)	–	10	–	V/μs
Critical Rate of Rise of Off-State Voltage Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 100°C	dv/dt				V/μs
T2800 B		100	–	–	
T2800 C		85	–	–	
T2802 D		75	–	–	
T2802 E		65	–	–	
T2802 M		60	–	–	

FIGURE 1 – CURRENT DERATING

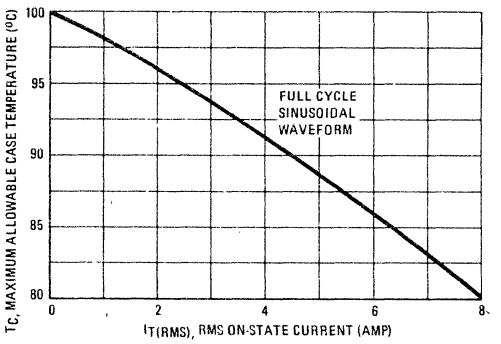
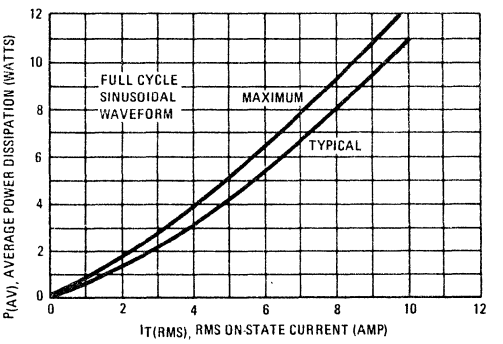


FIGURE 2 – POWER DISSIPATION



T2801

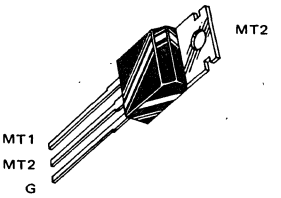
TRIACS

6 AMPERES RMS
200–600 VOLTS

BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies.

- Blocking Voltage to 600 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt▲ Construction for Low Thermal Resistance, High Heat Dissipation and Durability



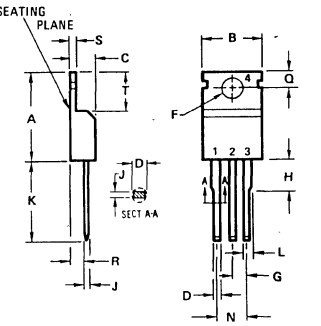
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (1) (T_J = -40 to +100°C) Gate Open	V_{DRM}		Volts
T2801 B		200	
T2801 C		300	
T2801 D		400	
T2801 E		500	
T2801 M		600	
RMS On-State Current (T_C = +80°C) (Conduction Angle = 360°C)	$I_{T(RMS)}$	6	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	80	Amp
Fusing Current (T_J = -40 to +100°C, t = 1 to 8.3 ms)	I^2t	35	A^2s
Peak Gate Power (T_C = +80°C, Pulse Width = 2 μs)	P_{GM}	16	Watts
Average Gate Power (T_C = +80°C, t = 8.3 ms)	$P_{G(AV)}$	0.35	Watt
Peak Gate Trigger Current (Pulse Width = 1 μs)	I_{GTM}	4	Amp
Operating Junction Temperature Range	T_J	-40 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.2	°C/W

(1) Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.



STYLE 2:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

CASE 221-02
TO-220 AB
All JEDEC dimensions and notes apply

This is advance information and specifications are subject to change without notice.

▲Trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C, Either Polarity of MT2-to-MT1 Voltage, unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current Rated V_{DRM}, Gate Open, T_J = 100°C	I_{DRM}	–	–	2	mA
Peak On-State Voltage I_{TM} = 30 A Peak; Pulse Width = 1 to 2 ms, Duty Cycle ≤ 2%	V_{TM}	–	2	3	Volts
Gate Trigger Current, Continuous dc (1) V_D = 12 Vdc, R_L = 12 Ohms	I_{GT}	–	25	80	mA
Gate Trigger Voltage, Continuous dc (1) V_D = 12 Vdc, R_L = 12 Ohms V_D = V_{DRM}, R_L = 125 Ohms, T_C = 100°C	V_{GT}	– 0.2	1.5 –	4 –	Volts
Holding Current (Either Direction) V_D = 12 Vdc, Gate Open, Initiating Current = 150 mA	I_H	–	100		mA
Turn-On Time (1) V_D = Rated V_{DRM}, I_T = 10 A, I_{GT} = 80 mA, Rise Time = 0.1 μs	t_{gt}	–	2.2	–	μs
Critical Rate of Rise of Commutation Voltage V_D = Rated V_{DRM}, $I_{T(RMS)}$ = 6.0 A, Commutating di/dt = 4.3 A/ms, Gate Unenergized, T_C = 80°C	dv/dt(c)	–	10	–	V/μs
Critical Rate of Rise of Off-State Voltage V_D = V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 100°C	dv/dt				V/μs
T2801 B		50	–	–	
T2801 C		40	–	–	
T2801 D		30	–	–	
T2801 E		20	–	–	

(1) Applies for MT2 (+), G (+), MT2 (–), G (–).

FIGURE 1 – CURRENT DERATING

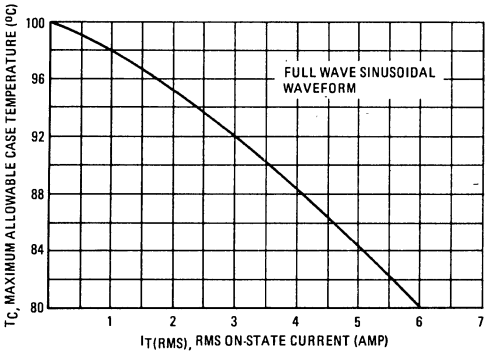
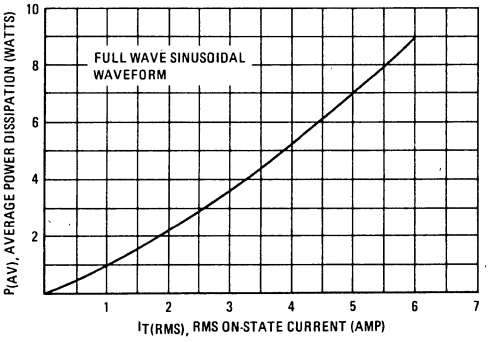


FIGURE 2 – POWER DISSIPATION



T4120

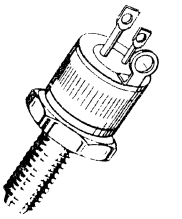
TRIACS

15 AMPERES RMS
200–600 VOLTS

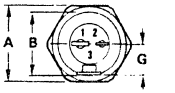
SILICON BIDIRECTIONAL TRIODE THYRISTORS

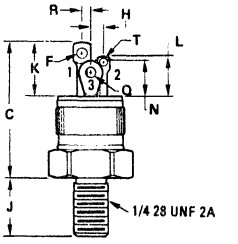
. . . designed primarily for industrial and military applications for full wave control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems.

- All Diffused and Glass Passivated Junctions for Greater Stability
- Isolated Stud Package
- Gate Triggering Guaranteed In All 4 Quadrants



STYLE 2:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2
STUD ISOLATED





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	26.16	–	1.030
F	1.65	4.06	0.065	0.160
G	–	6.48	–	0.255
H	2.16	2.41	0.085	0.095
J	10.67	11.58	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
N	6.48	6.99	0.255	0.275
Q	3.43	3.81	0.135	0.150
R	1.52	1.78	0.060	0.070
T	0.89	2.16	0.035	0.085

CASE 235-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (1) (T_J = -65 to +100°C) Gate Open T4120B D M	V_{DRM}	 200 400 600	Volts
RMS On-State Current (Conduction Angle = 360°C) T_C = +75°C	$I_{T(RMS)}$	15	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	100	Amp
Circuit Fusing (T_C = -65 to +100°C, t = 1.25 to 10 ms)	I^2t	50	A^2s
Peak Gate Power (Pulse Width = 1.0 μs)	P_{GM}	16	Watts
Average Gate Power	$P_{G(AV)}$	0.5	Watt
Peak Gate Trigger Current (Pulse Width = 1 μs)	I_{GTM}	4	Amp
Operating Case Temperature Range	T_C	-65 to +100	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Stud Torque	–	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.1	°C/W

(1) Ratings apply for open gate conditions. Thyristor devices shall not be tested with a constant current source for blocking capability such that the voltage applied exceeds the rated blocking voltage.

7

ELECTRICAL CHARACTERISTICS (T_C = 25°C, either polarity of MT2 to MT1 voltage, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current Gate Open Rated V_{DRM} @ T_C = 100°C	I_{DRM}	–	–	2	mA
Peak On-State Voltage I_T = 21 A Peak	V_{TM}	–	1.4	1.8	Volts
Gate Trigger Current, Continuous dc (1) V_D = 12 Vdc, R_L = 30 Ohms	I_{GT}				mA
V_{MT2} (+), V_G (+); V_{MT2} (–), V_G (–)		–	–	50	
V_{MT2} (+), V_G (–); V_{MT2} (–), V_G (+)		–	–	80	
V_{MT2} (+), V_G (+); V_{MT2} (–), V_G (–), T_C = -65°C		–	–	150	
V_{MT2} (+), V_G (–); V_{MT2} (–), V_G (+), T_C = -65°C		–	–	200	
Gate Trigger Voltage, Continuous dc (All Quadrants) V_D = 12 Vdc, R_L = 30 Ohms	V_{GT}				Volts
T_C = 25°C		–	–	2.5	
T_C = -65°C		–	–	4	
V_D = Rated V_{DROM}, R_L = 125 Ohms, T_C = 100°C		0.2	–	–	
Holding Current V_D = 12 Vdc, Gate Open I_T = 500 mA	I_H				mA
T_C = 25°C		–	–	75	
T_C = -65°C		–	–	300	
Gate Controlled Turn-On Time V_D = Rated V_{DRM}, I_{TM} = 25 A Peak, I_{GT} = 160 mA, Rise Time = 0.1 μs	t_{gt}	–	1.6	2.5	μs
Critical Rate-of-Rise of Commutation Voltage Rated V_{DRM}, $I_{T(RMS)}$ = 15 A, Commutating di/dt = 8 A/ms, Gate Unenergized, T_C = 75°C	dv/dt(c)	2	10	–	V/μs
Critical Rate-of-Rise of Off-State Voltage Rated V_{DRM}, Exponential Voltage Rise, Gate Open, T_C = 100°C	dv/dt				V/μs
T4120B		30	150	–	
D		20	100	–	
M		10	75	–	

(1) All Voltage polarity reference to main terminal 1.

7

FIGURE 1 – CURRENT DERATING

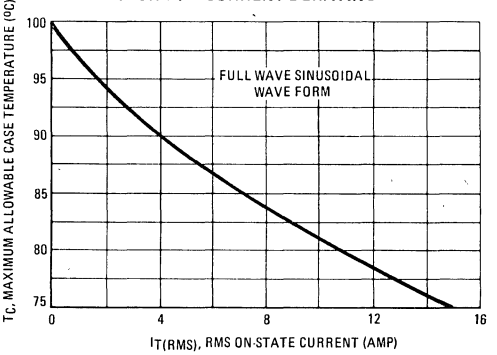
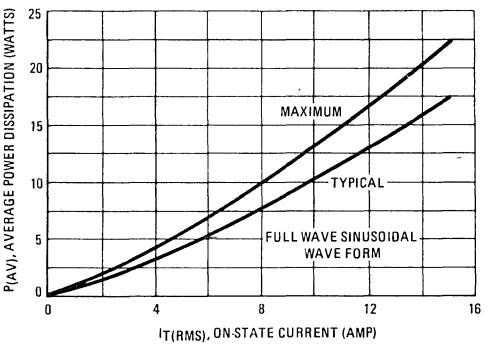


FIGURE 2 – POWER DISSIPATION



T6400
T6410
T6420

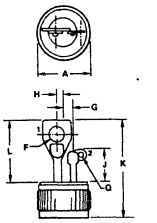
SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for industrial and military applications for the control of ac loads in applications such as power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire
- Press Fit Stud – T6400
  Stud – T6410
  Isolated Stud – T6420
- Gate Triggering Guaranteed in All 4 Quadrants

TRIACS

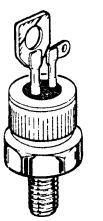
40 AMPERES RMS
200–800 VOLTS

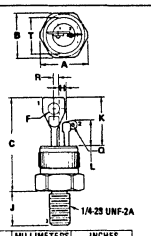


STYLE 2.
1. MT1
2. GATE
CASE. MT2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.73	12.83	0.501	0.505
F		4.06		0.160
G	2.16	2.41	0.085	0.095
H	1.52	1.78	0.060	0.070
J	7.62	8.89	0.300	0.350
K	–	26.67	–	1.050
L	–	17.02	–	0.670
Q	1.40	2.16	0.055	0.085

T6400
PRESS FIT
CASE 310-01

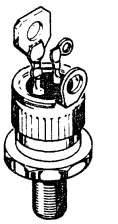


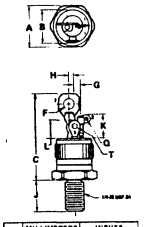


STYLE 2
PIN 1 MT1
2. GATE
3 MT2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.58	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.85 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

T6410
STUD
CASE 263-03





STYLE 2:
1. MT1
2. GATE
3. MT2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	32.51	–	1.280
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.80	2.01	0.083	0.079
J	10.67	11.58	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6.48	6.99	0.255	0.275
Q	1.40	2.18	0.055	0.085
T	3.43	3.81	0.135	0.150

T6420
ISOLATED STUD
CASE 311-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (T_J = -65 to +110°C) Gate Open T6400B, T6410B, T6420B T6400D, T6410D, T6420D T6400M, T6410M, T6420M T6400N, T6410N, T6420N	V_{DRM}	 200 400 600 800	Volts
On-State Current RMS T_C (Pressfit) = 70°C (Conduction Angle = 360°C) T_C (Stud) = 65°C	$I_{T(RMS)}$	40	Amp
Peak Surge Current (Non-Repetitive) (One Full Cycle, 60 Hz)	I_{TSM}	300	Amp
Circuit Fusing (T_J = -65 to +110°C, t = 1.25 to 10 ms)	I^2t	450	A^2s
Peak Gate Power (Pulse Width = 10 μs)	P_{GM}	40	Watts
Average Gate Power	$P_{G(AV)}$	0.75	Watt
Peak Gate Current (Pulse Width = 1 μs)	I_{GTM}	12	Amp
Operating Temperature Range	T_C	-65 to +110	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Stud Torque	–	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Pressfit Stud Isolated Stud	$R_{\theta JC}$	0.8 0.9 1.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current (Either Direction) Rated V_{DRM} @ T_J = 110°C, Gate Open	I_{DRM}	–	–	4	mA
Maximum On-State Voltage (Either Direction) I_T = 100 A Peak	V_{TM}	–	1.5	2	Volts
Gate Trigger Current, Continuous dc (1) V_D = 12 Vdc, R_L = 30 Ohms	I_{GT}				mA
V_{MT2} (+), $V_{G(+)}$		–	15	50	
V_{MT2} (+), $V_{G(-)}$		–	30	80	
V_{MT2} (–), $V_{G(-)}$		–	20	50	
V_{MT2} (–), $V_{G(+)}$		–	40	80	
V_{MT2} (+), $V_{G(+)}$; V_{MT2} (–), $V_{G(-)}$, T_C = -65°C		–	–	125	
V_{MT2} (+), $V_{G(-)}$; V_{MT2} (–), $V_{G(+)}$, T_C = -65°C		–	–	240	
Gate Trigger Voltage, Continuous dc	V_{GT}				Volts
V_D = 12 Vdc, R_L = 30 Ohms, T_C = 25°C		–	1.35	2.5	
T_C = -65°C		–	–	3.4	
V_D = Rated V_{DRM}, R_L = 125 Ohms, T_C = 110°C		0.2	–	–	
Holding Current (Either Direction) V_D = 12 Vdc, Gate Open	I_{HO}				mA
Initiating Current = 500 mA T_C = 25°C		–	25	60	
T_C = -65°C		–	–	100	
Gate Controlled Turn-On Time Rated V_{DRM}, I_T = 60 A, I_{GT} = 200 mA, Rise Time = 0.1 μs	t_{gt}	–	1.7	3	μs
Critical Rate of Rise of Commutation Voltage, On-State Conditions: di/dt = 22 A/ms, Gate Unenergized, V_D = Rated V_{DROM}, $I_{T(RMS)}$ = 40 A, T_C (Pressfit) = 70°C T_C (Stud) = 65°C	dv/dt(c)	–	5	–	V/μs

(1) All voltage polarity reference to main terminal 1.

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FIGURE 1 – ON-STATE POWER DISSIPATION

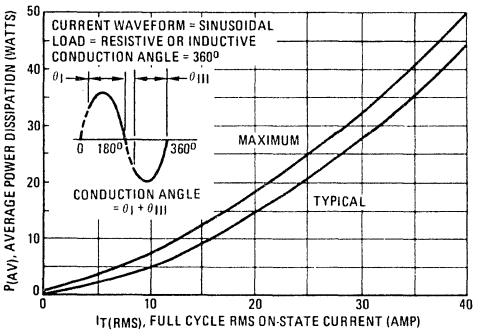
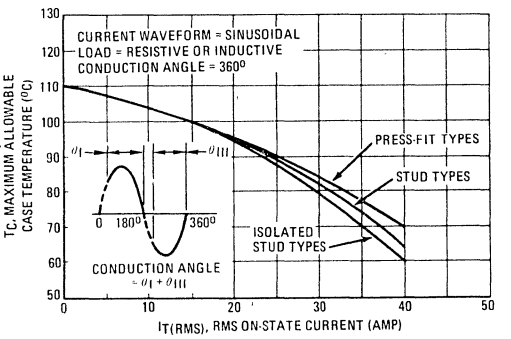


FIGURE 2 – RMS CURRENT DERATING



T6401
T6411
T6421

TRIACS

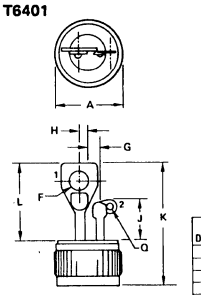
30 AMPERES RMS
200–600 VOLTS

SILICON BIDIRECTIONAL TRIODE THYRISTORS

. . . designed primarily for industrial and military applications for full wave control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems.

- Glass Passivated Junctions and Center Gate Geometry
- Isolated Stud Available for Ease of Assembly (T6421 Series)
- Gate Triggering Guaranteed In All 4 Modes

T6401

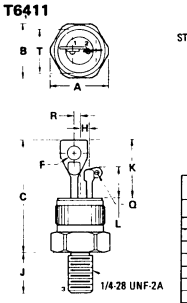


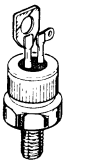
STYLE 2
1 MT1
2 GATE
CASE MT2

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	12 73	12 83	0 501	0 505
F	–	4 06	–	0 160
G	2 16	2.41	0 085	0 095
H	1.52	1.78	0.060	0.070
J	7 62	8 89	0 300	0 350
K	–	26 67	–	1 050
L	–	17 02	–	0 670
Q	1 40	2 16	0 055	0 085

PRESS FIT
CASE 310-01

T6411



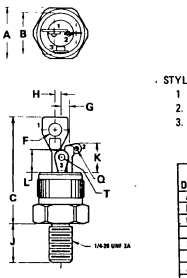


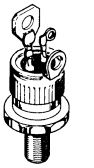
STYLE 2.
PIN 1 MT1
2. GATE
3 MT2

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.34	15.60	0.604	0.614
B	14 00	14.20	0.551	0.559
C	26.67	30.23	1 050	1 190
F	3 43	4 06	0.135	0.160
H	2.29 REF		0 090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12 73	12.83	0.501	0 505

STUD
CASE 263-03

T6421





STYLE 2:
1 MT1
2. GATE
3. MT2

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	14.00	14.20	0.551	0.559
B	12.73	12.83	0.501	0.505
C	–	32.51	–	1.280
F	–	4.06	–	0.160
G	2.16	2.41	0.085	0.095
H	1.60	2.01	0.063	0.079
J	10.67	11.56	0.420	0.455
K	7.62	8.89	0.300	0.350
L	6.48	6.99	0.255	0.275
Q	1.40	2.16	0.055	0.085
T	3.43	3.81	0.135	0.150

ISOLATED STUD
CASE 311-01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Repetitive Peak Off-State Voltage (T_J = -65 to +100°C) Gate Open T6401B, T6411B, T6421B T6401D, T6411D, T6421D T6401M, T6411M, T6421M	V_{DRM}	 200 400 600	Volts
On-State Current RMS (Conduction Angle = 360°C) $T_C \leq$ +65°C	$I_{T(RMS)}$	30	Amp
Peak Non-Repetitive Surge Current (One Full Cycle, 60 Hz)	I_{TSM}	300	Amp
Circuit Fusing (T_J = -65 to +100°C, t = 1.25 to 10 ms)	I^2t	450	A^2s
Peak Gate Power (Pulse Width = 1.0 μs)	P_{GM}	40	Watts
Average Gate Power	$P_{G(AV)}$	0.75	Watt
Peak Gate Current Pulse Width ≤ 1 μs)	I_{GM}	2	Amp
Operating Case Temperature Range	T_C	-65 to +100	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Stud Torque	–	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Pressfit Stud Isolated Stud	$R_{\theta JC}$	0.8 0.9 1.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and Either Polarity of MT2 to MT1, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Off-State Current V_D = Rated V_{DRM} @ T_J = 100°C, Gate Open	I_{DRM}	–	–	4	mA
Maximum On-State Voltage (Either Direction) I_{TM} = 100 A Peak	V_{TM}	–	2.1	2.5	Volts
Gate Trigger Current, Continuous dc (1) V_D = 12 Vdc, R_L = 30 Ohms V_{MT2} (+), $V_{G(+)}$; $V_{MT2(-)}$,$V_{G(-)}$ V_{MT2} (+), $V_{G(-)}$; $V_{MT2(-)}$,$V_{G(+)}$	I_{GT}	 – –	 20 35	 50 80	mA
Gate Trigger Voltage, Continuous dc, All Trigger Modes V_D = 12 Vdc, R_L = 30 Ohms V_D = Rated V_{DRM}, R_L = 125 Ohms, T_C = 100°C	V_{GT}	 – 0.2	 1.35 –	 2.5 –	Volts
Holding Current V_D = 12 Vdc, Gate Open I_T = 150 mA	I_{HO}	–	–	60	mA
Gate Controlled Turn-On Time V_D = Rated V_{DRM}, I_{TM} = 45 A, I_{GT} = 200 mA, Rise Time = 0.1 μs	t_{gt}	–	1.7	3	μs
Critical Rate of Rise of Commutation Voltage, On-State Conditions: di/dt = 16 A/ms, Gate Unenergized, V_D = Rated V_{DRM}, $I_{T(RMS)}$ = 30 A, T_C = Rated Value from Figure 1	dv/dt(c)	3	20	–	V/μs
Critical Rate of Rise of Off-State Voltage V_D = Rated V_{DRM}, Exponential Rise, T_C = 100°C T6401B, T6411B, T6421B T6401D, T6411D, T6421D T6401M, T6411M, T6421M	dv/dt	 40 25 20	 – – –	 – – –	V/μs

FIGURE 1 – CURRENT DERATING

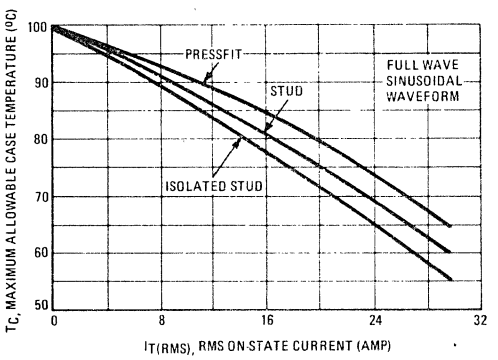
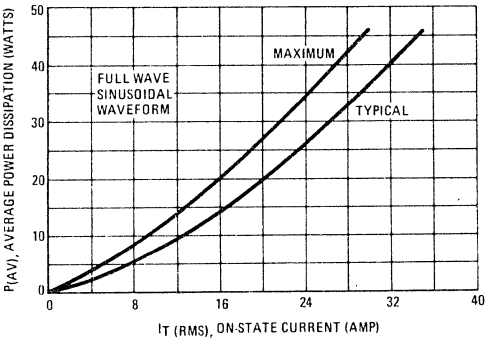


FIGURE 2 – POWER DISSIPATION



7

Leadforms, Hardware, and Mounting Techniques

8

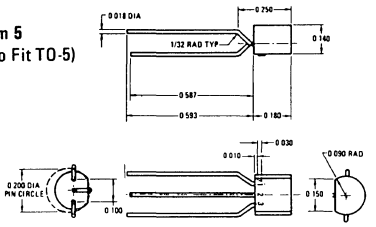
LEADFORM OPTIONS

Plastic packaged semiconductors may be leadformed to a variety of configurations for insertion into sockets and boards designed for metal can devices. The following are standard leadforms offered by Motorola.

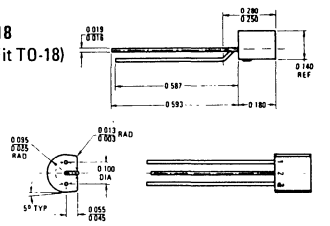
THYRISTOR AND TRIGGER LEADFORM OPTIONS

To order leadformed product, determine the form desired, and specify case number and applicable leadform number. A special device title will be assigned by the factory to process your order. Certain standard devices already incorporate a leadform, and may be purchased without consulting the factory.

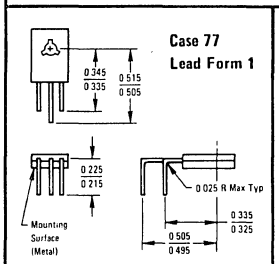
Case 29
Lead Form 5
(TO-92 To Fit TO-5)



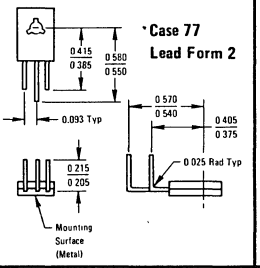
Case 29
Lead Form 18
(TO-92 To Fit TO-18)



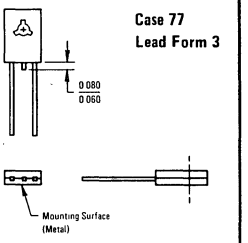
Case 77
Lead Form 1



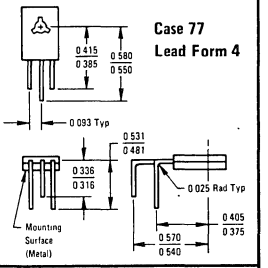
Case 77
Lead Form 2



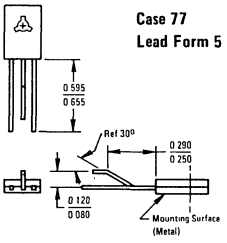
Case 77
Lead Form 3



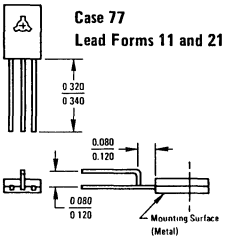
Case 77
Lead Form 4



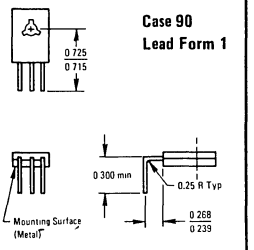
Case 77
Lead Form 5



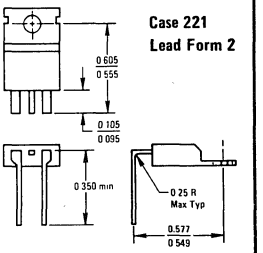
Case 77
Lead Forms 11 and 21



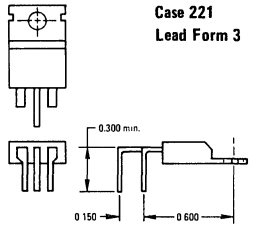
Case 90
Lead Form 1



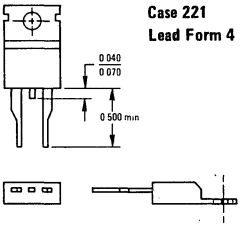
Case 221
Lead Form 2



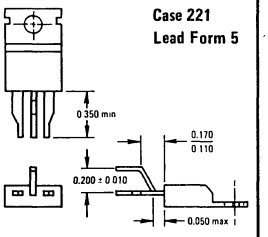
Case 221
Lead Form 3



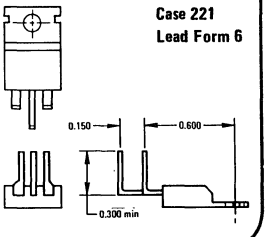
Case 221
Lead Form 4



Case 221
Lead Form 5



Case 221
Lead Form 6



8

PLASTIC POWER TRANSISTOR LEADFORM OPTIONS

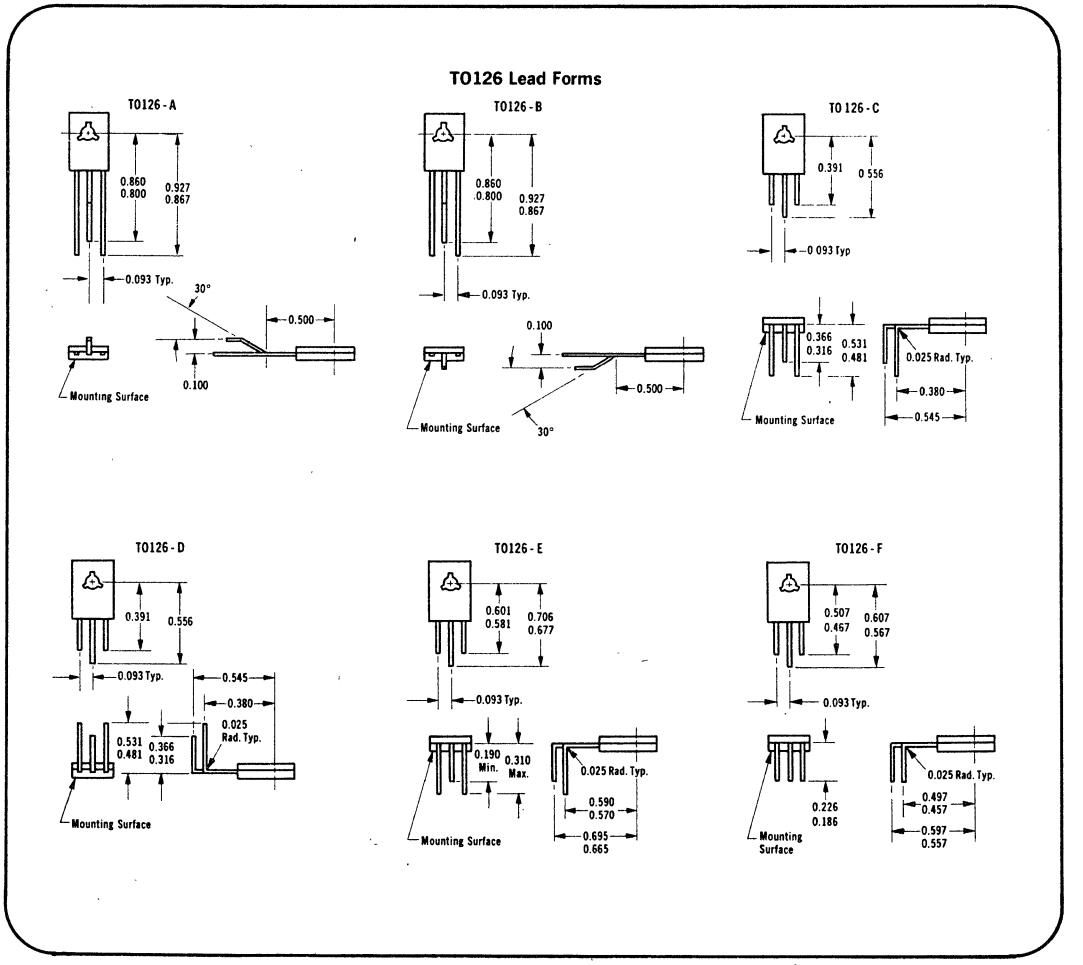
TO-126 (Case 77), TO-127 (Case 90), TO-220 (Case 221A)

Devices may be leadformed by first converting to a special "SJE" number. The factory must be given the designation of the package and the applicable leadform suffix letter. The factory must be consulted.

TO-202 (Duowatt) **Case 152 (Uniwatt)**

Any device in these packages may be leadformed by designating the proper suffix number after the device type called out.

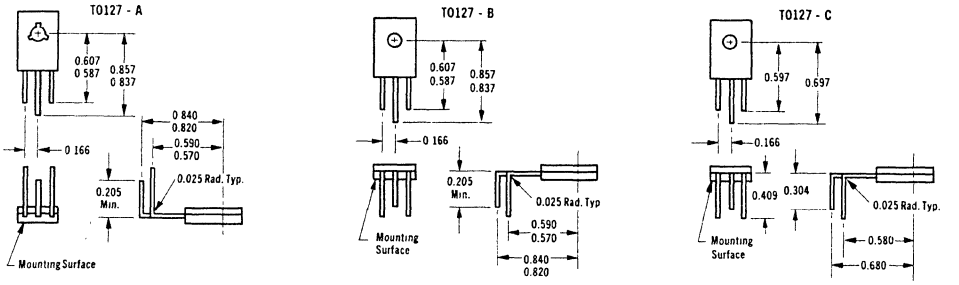
Example—To leadform an MPS-U01 into the TO-5 configuration, designate it as: MPS-U01-05.



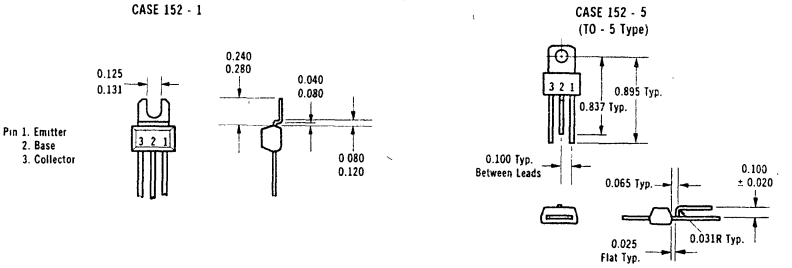
8

Plastic Power Transistor
Leadform Options (continued)

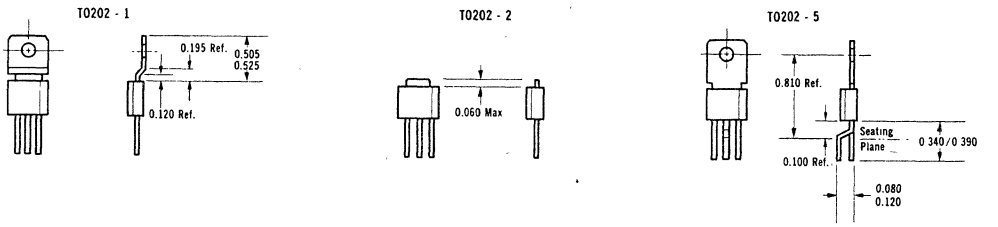
TO127 Lead Forms



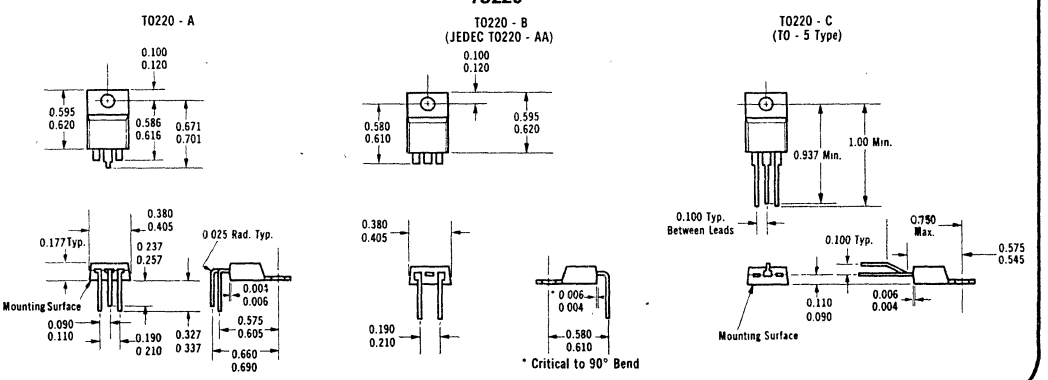
CASE 152 - UNIWATT



TO202 - DUOWATT

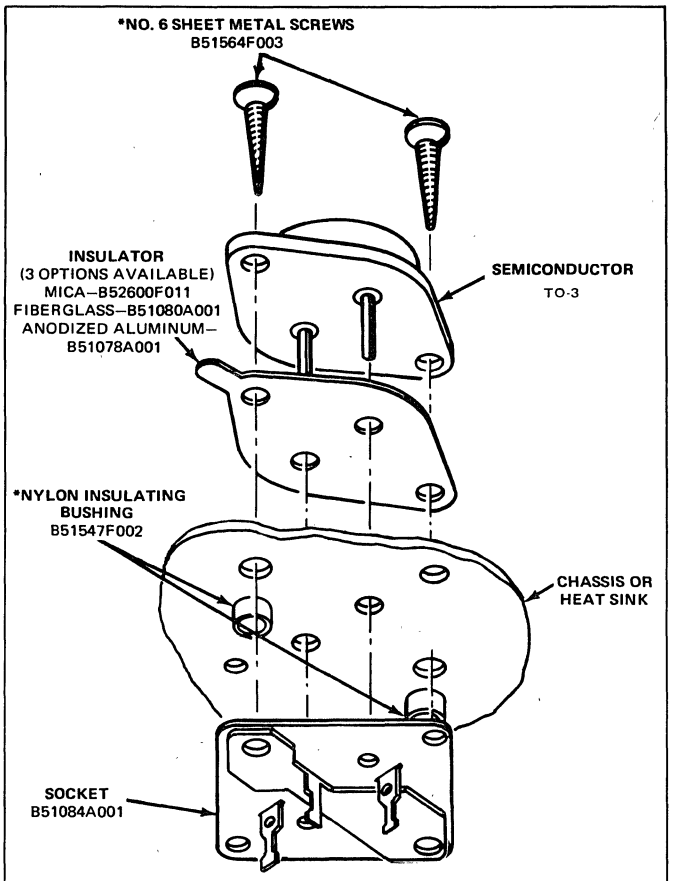


TO220



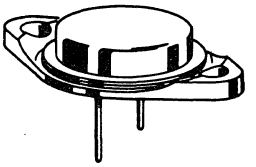
8

MOUNTING HARDWARE TO-3



*Longer screws (not available from Motorola) and multiple bushings may be required for thick chassis or heat sink.

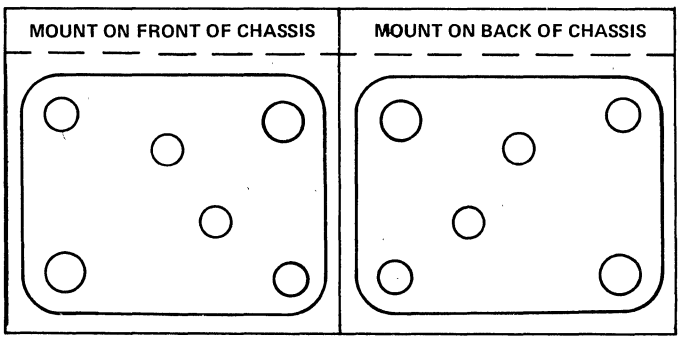
This hardware is applicable to the following packages.



CASE 1 (TO-3)
CASE 3
CASE 11A
CASE 11 (TO-3)
CASE 12
CASE 54
CASE 197

8

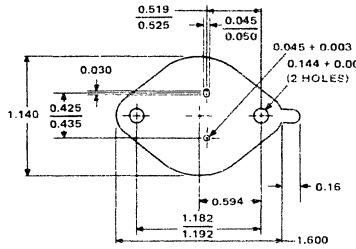
DRAWINGS NOT TO SCALE



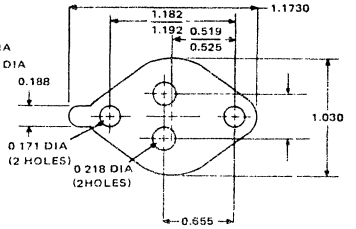
FRONT TEMPLATE
B51087A001

BACK TEMPLATE
B51087A002

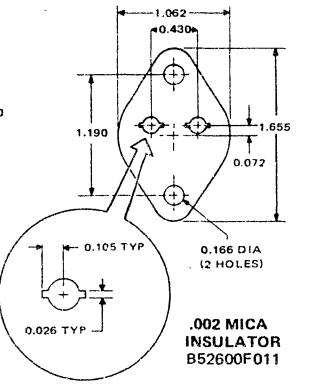
MOUNTING HARDWARE TO-3



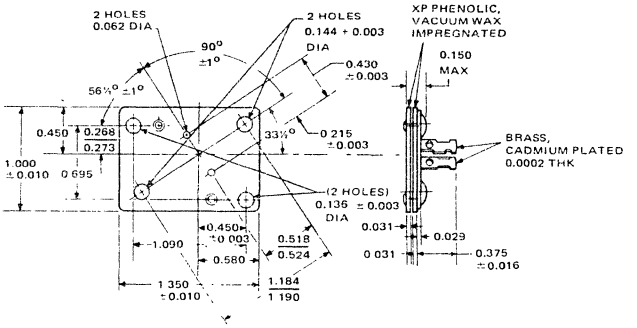
0.003 TEFLON-COATED FIBERGLASS INSULATOR
B51080A001



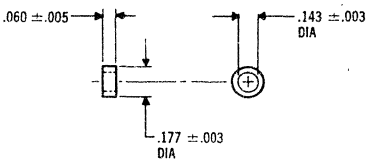
.020 ALUMINUM INSULATOR
B51078A001



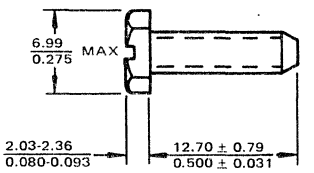
.002 MICA INSULATOR
B52600F011

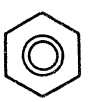


TRANSISTOR SOCKET
B51084A001

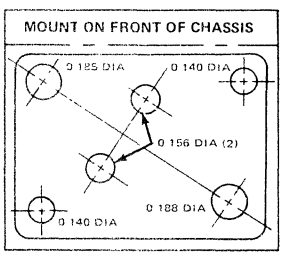


NYLON INSULATING BUSHING
B51547F002

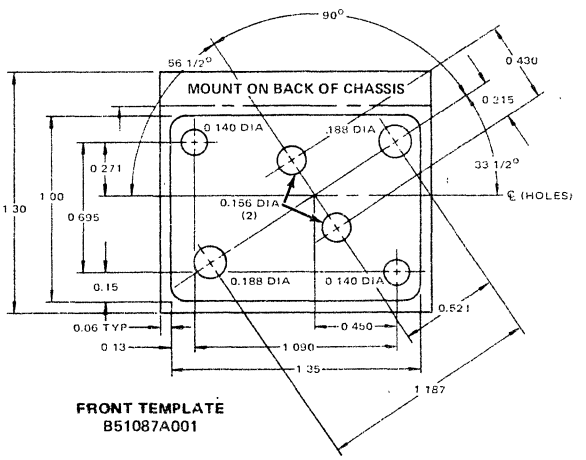




NO. 6 SHEET METAL SCREW
B51564F003

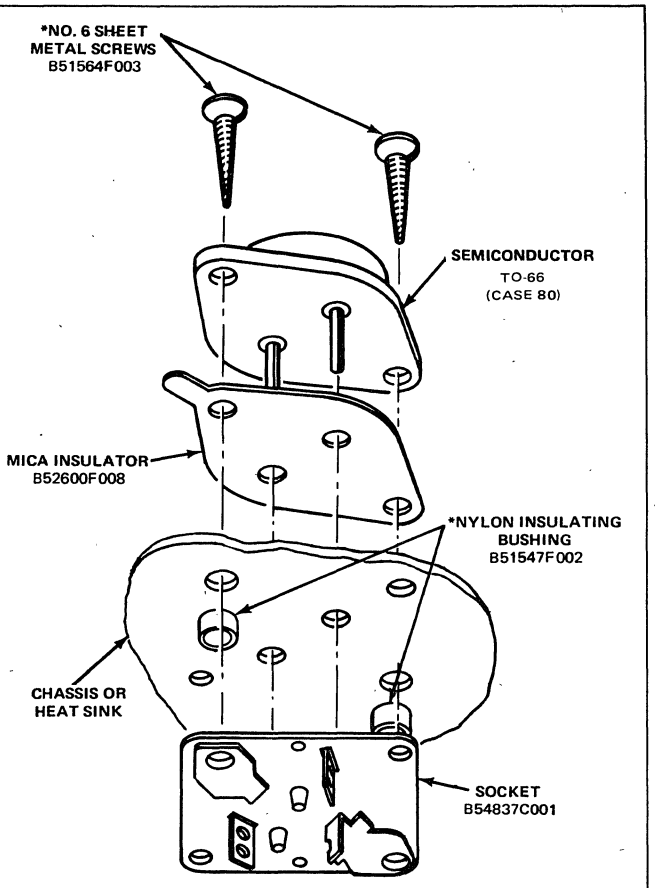


BACK TEMPLATE
B51087A002

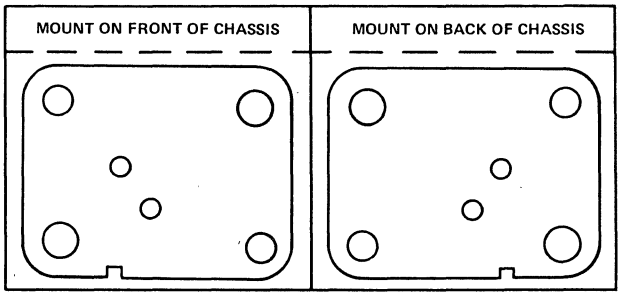


FRONT TEMPLATE
B51087A001

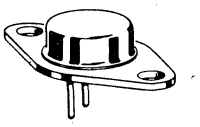
MOUNTING HARDWARE TO-66

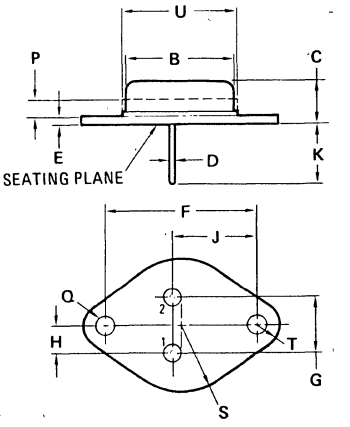


* Longer screws (not available from Motorola) and multiple bushings may be required for thick chassis or heat sink.



FRONT TEMPLATE B54879C001 (DRAWINGS NOT TO SCALE) BACK TEMPLATE B54879C002



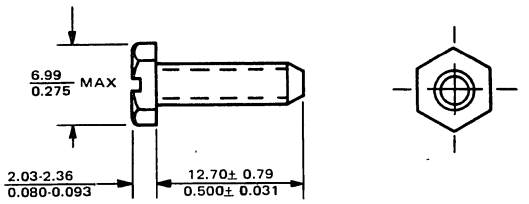


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.86	0.028	0.034
E	1.27	1.91	0.050	0.075
F	24.33	24.43	0.958	0.962
G	4.83	5.33	0.190	0.210
H	2.41	2.67	0.095	0.105
J	14.48	14.99	0.570	0.590
K	9.14	–	0.360	–
P	–	1.27	–	0.050
Q	3.61	3.86	0.142	0.152
S	–	8.89	–	0.350
T	–	3.68	–	0.145
U	–	15.75	–	0.620

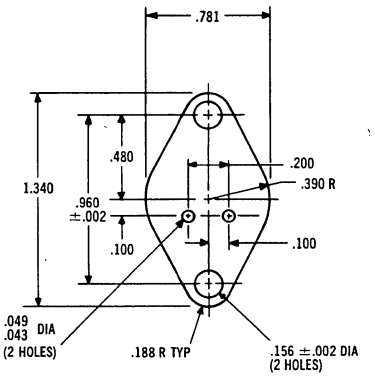
All JEDEC Dimensions and and Notes Apply.

CASE 80
(TO-66)

8

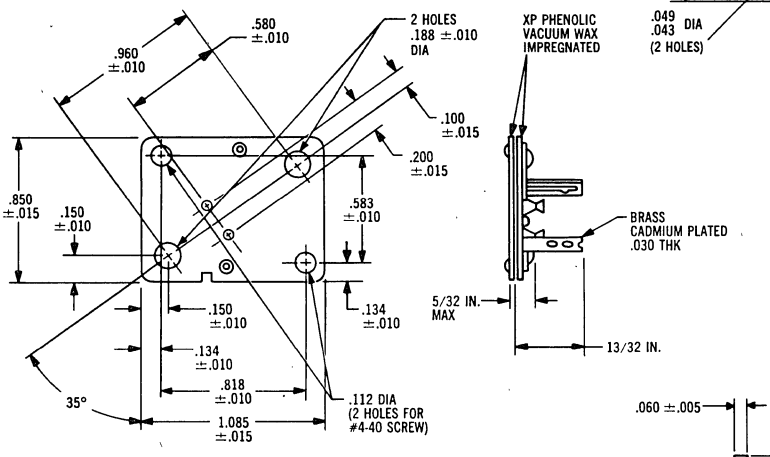


NO. 6 SHEET METAL SCREW
B51564F003

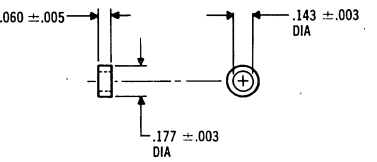


0.005 MICA INSULATOR
B52600F008

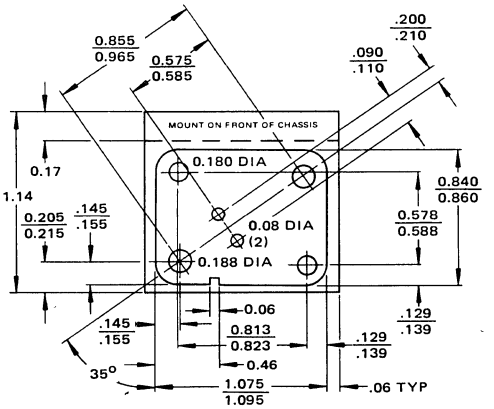
0.003 MICA INSULATOR
B52600F009



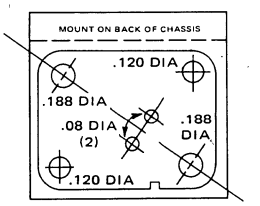
TRANSISTOR SOCKET
B54837C001



NYLON INSULATING BUSHING
B51547F002



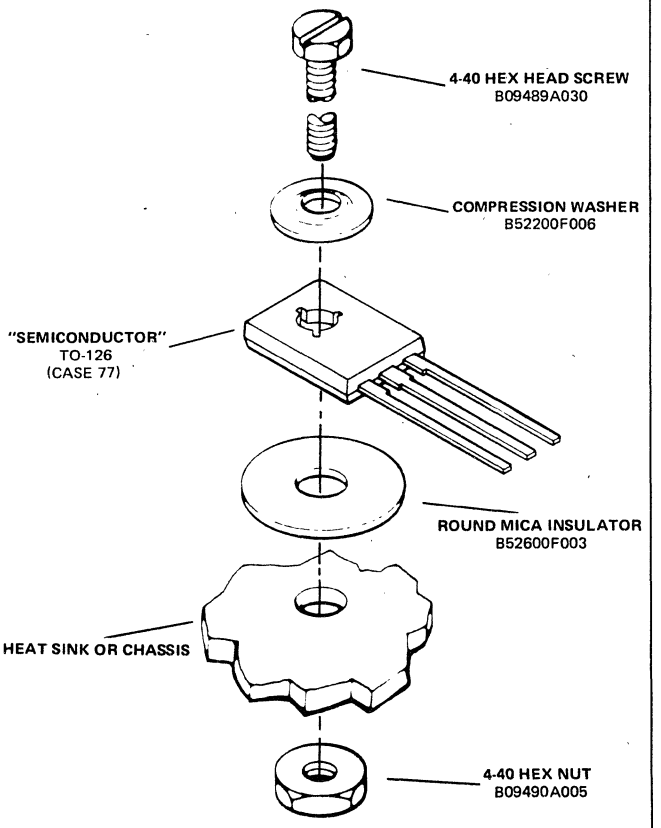
FRONT TEMPLATE
B54879C001



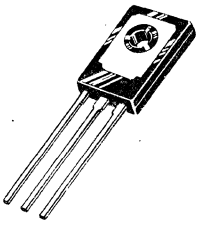
BACK TEMPLATE
B54879C002

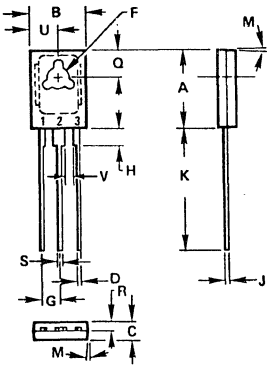
8

MOUNTING HARDWARE TO-126



TORQUE REQUIREMENTS
0.68N-m (6IN-LBS.) MAX.



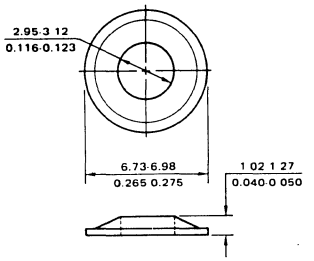


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.18	0.115	0.125
G	2.31	2.46	0.091	0.097
H	1.27	2.41	0.050	0.095
J	0.38	0.64	0.015	0.025
K	15.11	16.64	0.595	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155
V	1.02	–	0.040	–

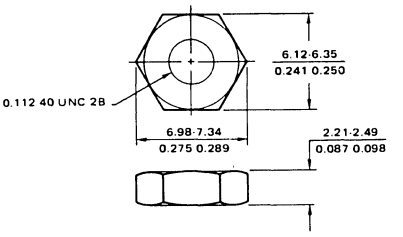
CASE 77-04
TO-126

8

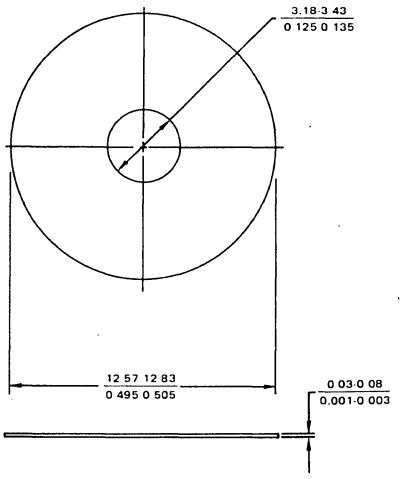
(DIMENSIONS – MILLIMETERS / INCH)



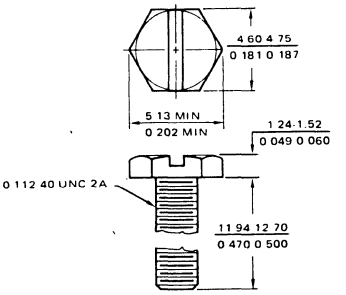
STEEL COMPRESSION WASHER
B52200F006



4-40 HEX NUT
CARBON STEEL,
CADMIUM PLATED
B09490A005



ROUND MICA INSULATOR
B52600F003



4-40 HEX HEAD SCREW
CARBON STEEL,
CADMIUM PLATED
B09489A003

8

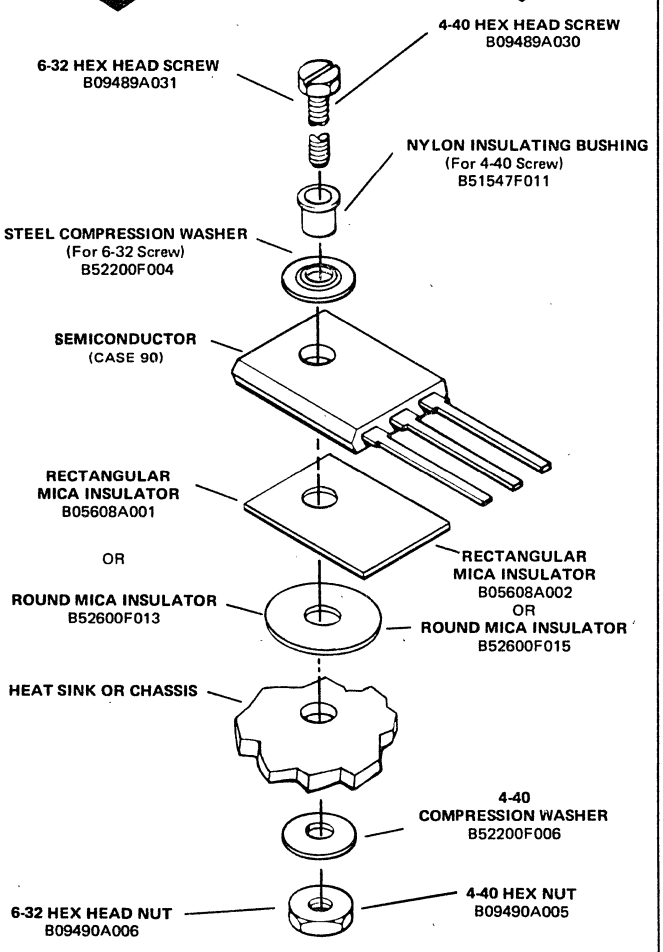
MOUNTING HARDWARE TO-127, CASE 90

Part numbers in this column for

INSULATED MOUNTING

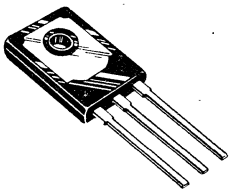
Part numbers in this column for

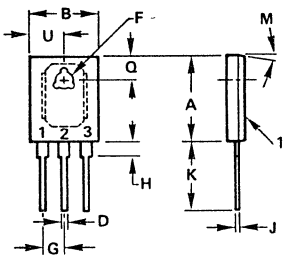
***HIGH VOLTAGE INSULATED MOUNTING**

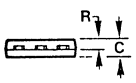


TORQUE REQUIREMENTS
Insulated 0.68 N-m (8 IN. LBS.) MAX
High Voltage Insulated 0.90 N-m (6 IN. LBS.) MAX

*High voltage mounting requirements depend on use environment. User is encouraged to make his own evaluation.







DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.13	16.38	0.635	0.645
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	1.09	1.24	0.043	0.049
F	3.51	3.76	0.138	0.148
G	4.22 BSC		0.166 BSC	
H	2.67	2.92	0.105	0.115
J	0.813	0.864	0.032	0.034
K	15.11	16.38	0.595	0.645
M	9° TYP		9° TYP	
Q	4.70	4.95	0.185	0.195
R	1.91	2.16	0.075	0.085
U	6.22	6.48	0.245	0.255

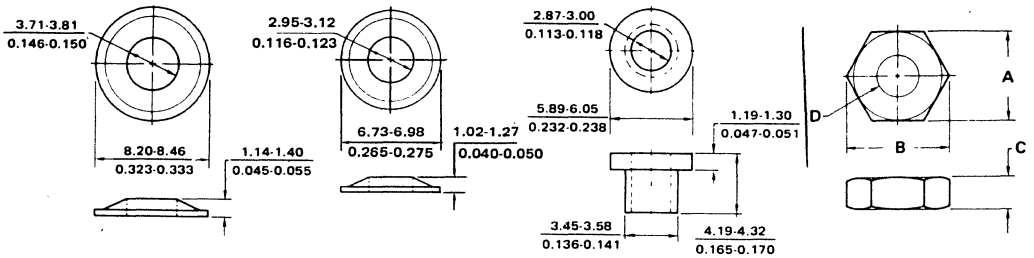
CASE 90
(TO-127)

8

MOUNTING HARDWARE TO-127, CASE 90

OUTLINE DIMENSIONS

DIMENSIONS – MILLIMETER / INCH

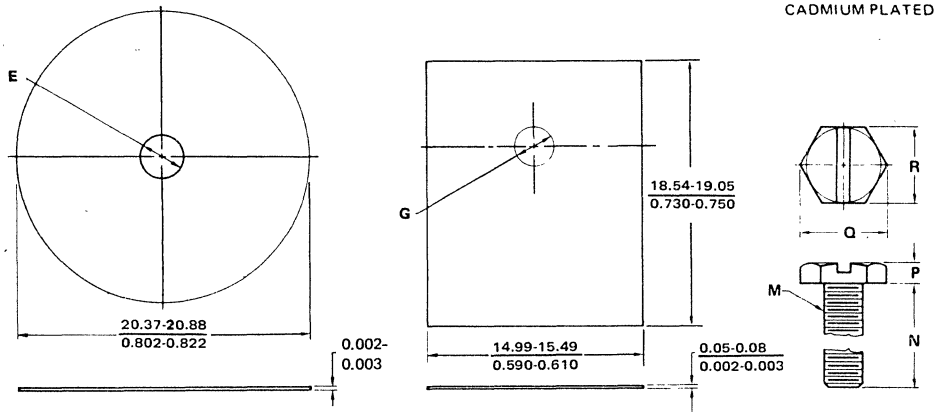


STEEL COMPRESSION WASHER
B52200F004

STEEL COMPRESSION WASHER
B52200F006

NYLON INSULATING BUSHING
B51547F011

HEX NUT
CARBON STEEL, CADMIUM PLATED



ROUND MICA INSULATOR
(See table below.)

RECTANGULAR MICA INSULATOR
(See table below.)

HEX HEAD SCREW
CARBON STEEL, CADMIUM PLATED

DIMENSIONS – MILLIMETER (INCH)

ROUND MICA INSULATOR

PART NO.	DIM E
B52600F013	3.56-3.81 (0.140-0.150)
B52600F015	2.87-2.97 (0.113-0.117)

RECTANGULAR MICA INSULATOR

PART NO.	DIM G
B05608A001	3.68-3.94 (0.145-0.155)
B05608A002	2.87-3.00 (0.113-0.118)

HEX NUT

TYPE	PART NO.	DIM A	DIM B	DIM C	DIM D
4-40	B09490A005	6.12-6.35 (0.241-0.250)	6.98-7.34 (0.275-0.289)	2.21-2.49 (0.087-0.098)	2.84 NOM (0.112 NOM)
6-32	B09490A006	7.67-7.92 (0.302-0.312)	8.74-9.17 (0.344-0.361)	2.59-2.90 (0.102-0.114)	3.50 NOM (0.138 NOM)

HEX HEAD SCREW

TYPE	PART NO.	DIM M	DIM N	DIM P	DIM Q	DIM R
4.40	B09489A030	2.84-40 (0.112-40)	11.94-12.70 (0.470-0.500)	1.24-1.52 (0.049-0.060)	5.13 MIN (0.202 MIN)	4.60-4.75 (0.181-0.187)
6.32	B09484A032	3.5-32 (0.138-32)	11.94-12.70 (0.470-0.500)	2.03-2.36 (0.080-0.093)	6.91 MIN (0.272 MIN)	6.20-6.35 (0.244-0.250)

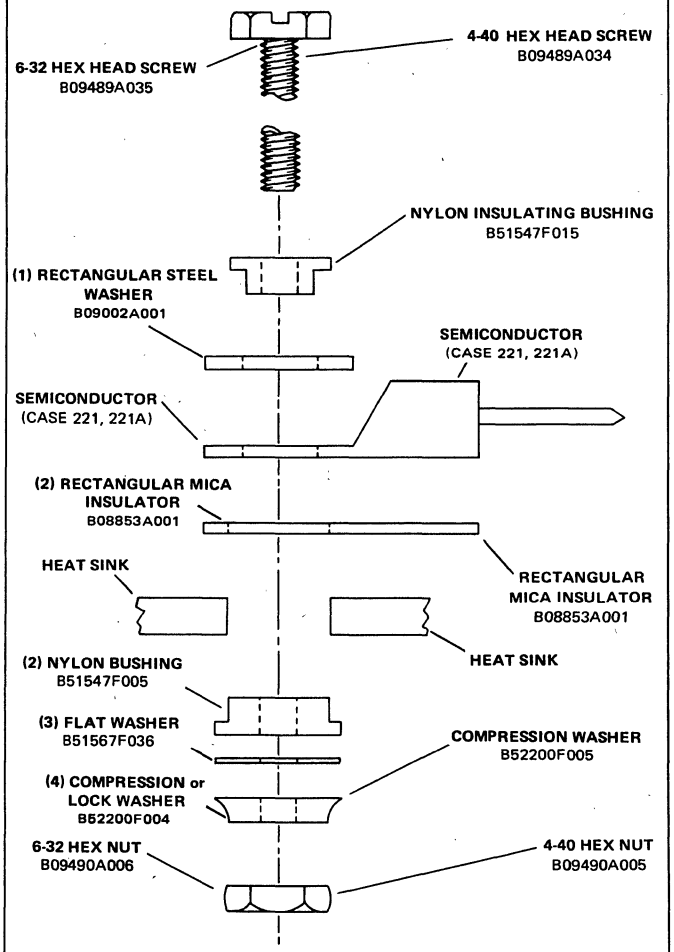
MOUNTING HARDWARE TO-220AB

PREFERRED ARRANGEMENT
for Isolated or Non-isolated Mounting. Screw is at Semiconductor Case Potential. 6-32 Hardware is Used.

Choose from Parts Listed Below.

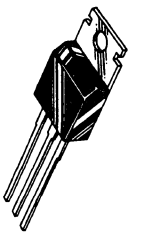
ALTERNATE ARRANGEMENT
for Isolated Mounting when Screw must be at Heat-Sink Potential. 4-40 Hardware is Used.

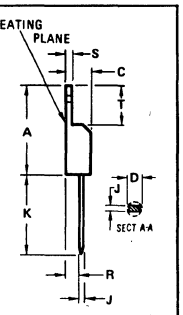
Use Parts Listed Below.



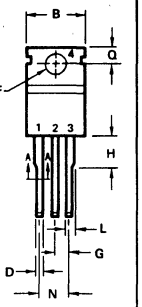
(1) Used with thin chassis and/or large hole.
(2) Used when isolation is required.
(3) Required when nylon bushing and lock washer are used.
(4) Compression washer preferred when plastic insulating material is used.

TORQUE REQUIREMENTS
Insulated 0.68 N-M (6 in-lbs) max
Noninsulated 0.9 N-M (8 in-lbs) max.

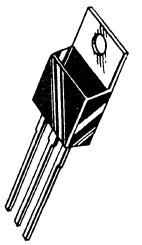


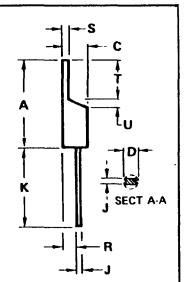


DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	14.23	15.87	0.560	0.625
B	9.66	10.66	0.380	0.420
C	3.56	4.82	0.140	0.190
D	0.51	1.14	0.020	0.045
F	3.531	3.733	0.139	0.147
G	2.29	2.79	0.090	0.110
H	–	6.35	–	0.250
J	0.31	1.14	0.012	0.045
K	12.70	14.27	0.500	0.562
L	1.14	1.77	0.045	0.070
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.92	0.080	0.115
S	0.51	1.39	0.020	0.055
T	5.85	6.85	0.230	0.270

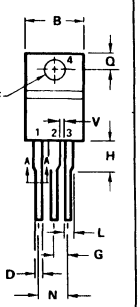


CASE 221-02
TO-220 AB
All JEDEC dimensions and notes apply





DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

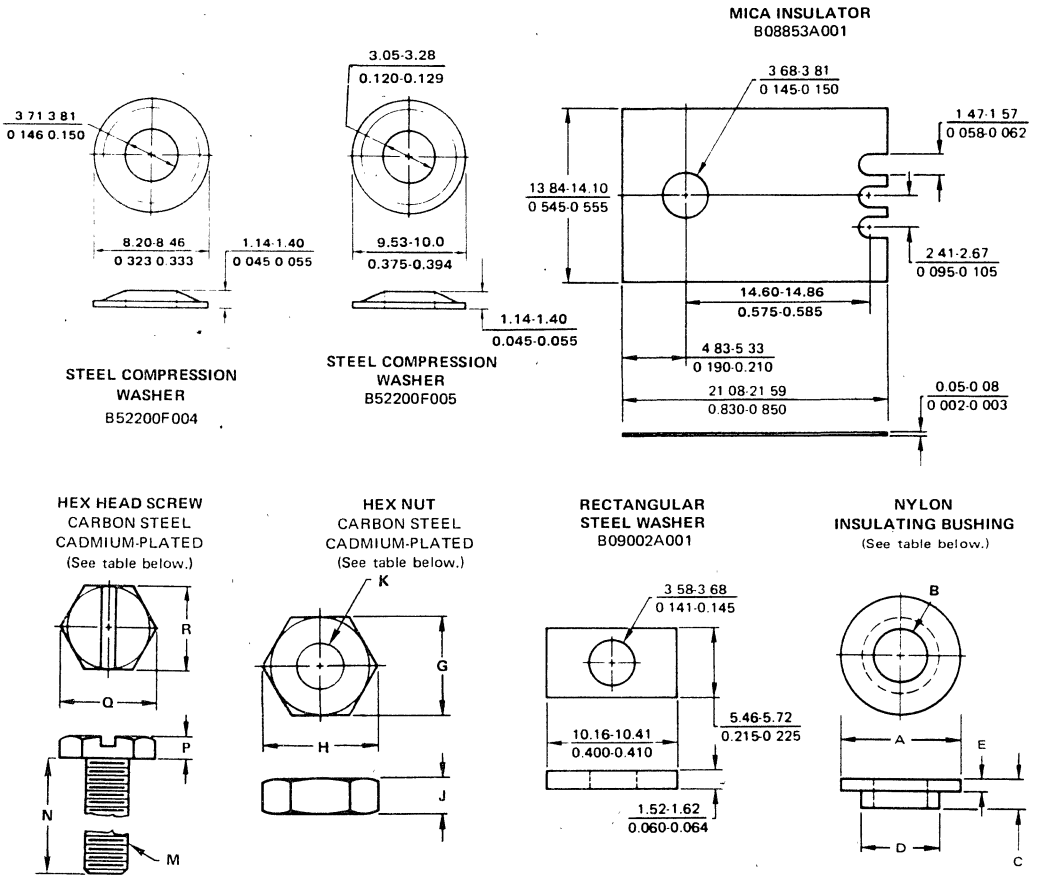


CASE 221A-02
TO-220AB

8

MOUNTING HARDWARE TO-220AB

(DIMENSION – MILLIMETER / INCH)



DIMENSIONS – MILLIMETER (INCH)

NYLON BUSHING

PART NO.	DIM A	DIM B	DIM C	DIM D	DIM E
B51547F005	9.40-9.65 (0.370-0.380)	3.84-4.09 (0.151-0.161)	2.16-2.41 (0.085-0.095	6.10-6.35 (0.240-0.250)	1.02-1.27 (0.040-0.050)
B51547F015	5.59-6.10 (0.220-0.240)	3.05-3.15 (0.120-0.124)	1.57-1.68 (0.062-0.066)	3.56-3.66 (0.140-0.144)	0.51-0.64 (0.020.0.025)

HEX NUT

TYPE	PART NO.	DIM G	DIM H	DIM J	DIM K
4-40	B09490A005	6.12-6.35 (0.241-0.250)	6.98-7.34 (0.275-0.289)	2.21-2.49 (0.087-0.098)	2.84 NOM (0.112 NOM)
6-32	B09490A006	7.67-7.92 (0.302-0.312)	8.74-9.17 (0.344-0.361)	2.59-2.90 (0.102-0.114)	3.50 NOM (0.138 NOM)

HEX HEAD SCREW

TYPE	PART NO.	DIM M	DIM N	DIM P	DIM Q	DIM R
4-40	B09489A034	0.112-40	1.57 (0.62)	1.24-1.52 (0.049-0.060)	5.13 MIN (0.202 MIN)	4.60-4.75 (0.181-0.187)
6-32	B09489A035	0.138-32	1.57 (0.62)	2.03-2.36 (0.080-0.093)	6.91 MIN (0.272 MIN)	6.20-6.35 (0.244-0.250)

MOUNTING TECHNIQUES FOR POWER SEMICONDUCTORS

INTRODUCTION

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead-mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, semiconductor-industry field history indicates that the failure rate of most silicon semiconductors decreases approximately by one half for a decrease in junction temperature from 160°C to 135°C.*

Many failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from mounting securely to a warped surface. With the widespread use of various plastic-packaged semiconductors, the dimension of mechanical damage becomes very significant.

Figure 1 shows an example of doing nearly everything wrong. In this instance, the device to be victimized is in the TO-220 package. The leads are bent to fit into a socket—an operation which, if not properly done, can crack the package, break the bonding wires, or crack the die. The package is fastened with a sheet-metal screw through a 1/4"-hole containing a fiber-insulating sleeve. The force used to tighten the screw pulls the package into the hole, causing enough distortion to crack the die. Even if the die were not cracked, the contact area is small because of the area consumed by the large hole and the bowing of the package; the result is a much higher junction temperature than expected. If a rough heat sink surface and some burrs around the hole are present, many—but unfortunately not all—poor mounting practices are covered.

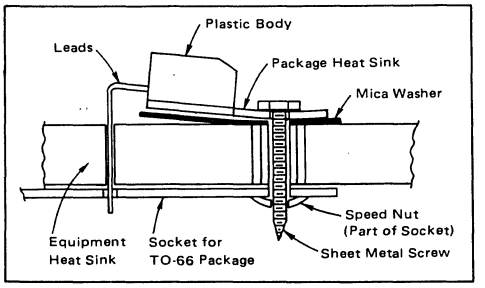


FIGURE 1 – Extreme Case of Improperly Mounting A Semiconductor (Distortion Exaggerated)

*See MIL–Handbook–217B, Section 2.2

In many situations the case of the semiconductor must be isolated electrically from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc-over problems is introduced if high voltages are being handled. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures necessitate attention to the following areas:

1. Mounting surface preparation,
2. Application of thermal compounds,
3. Installation of the insulator,
4. Fastening of the assembly, and
5. Lead bending and soldering.

In this note, the procedures are discussed in general terms. Specific details for each class of packages are given in the figures and in Table 1. Appendix A contains a brief review of thermal resistance concepts, and Appendix B lists sources of supply for accessories. Motorola supplies hardware for all power packages. It is detailed on separate data sheets for each package type.

MOUNTING SURFACE PREPARATION

In general, the heat-sink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heat-sink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high-power applications, a more detailed examination of the surface is required.

Surface Flatness

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 2. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness, i.e., $\Delta h/TIR$, is satisfactory in most cases if less than 4 mils per inch, which is normal for extruded aluminum—although disc type devices usually require 1 mil per inch.

Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 to 60 microinches is satisfactory;* a finer finish is costly to achieve and does not significantly lower contact resistance. Most commercially available cast or extruded

*Tests run by Thermalloy (Catalog #74-INS-3, page 14) using a copper TO-3 package with a typical 32-microinch finish, showed that finishes between 16 and 64 μ-in caused less than ±2.5% difference in interface thermal resistance.

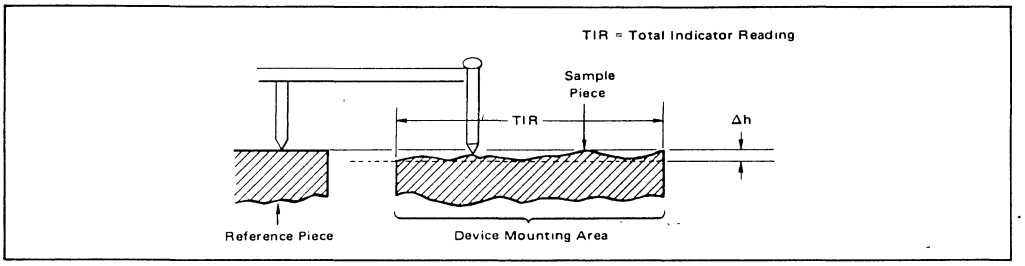


FIGURE 2 – Surface Flatness

heat sinks will require spotfacing when used in high-power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger packages having mounting holes removed from the semiconductor die location, such as a TO-3, may successfully be used with larger holes to accommodate an insulating bushing, but Thermopad plastic packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package..

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This "crater" in the heat sink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heat-sink indentation, or the device may only bridge the crater and leave a significant percentage of its heat-dissipating surface out of contact with the heat sink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early-life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heat sinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine-edge blanking or sheared-through holes when applied to sheet metal as commonly used for stamped heat sinks. The holes are pierced using Class A progressive dies mounted on four-post die sets equipped with proper pressure pads and holding fixtures.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. The edges should be broken to remove burrs which cause poor contact between device and heat sink and may puncture isolation material.

Many aluminum heat sinks are black-anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Another treated aluminum finish is iridite, or chromate-acid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heat sinks. For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of paint's high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heat sink, anodized or painted surfaces may be more effective than other insulating materials which tend to creep (i.e., they flow), thereby reducing contact pressure.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Unless used immediately after machining, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse. Thermal grease should be immediately applied thereafter and the semiconductor attached as the grease readily collects dust and metal particles.

THERMAL COMPOUNDS

To improve contacts, thermal joint compounds or greases are used to fill air voids between all mating surfaces. Values of thermal resistivity vary from 0.10 degrees Celsius-inches per watt for copper film to 1200°C-in/W for air, whereas satisfactory joint compounds will have a resistivity of approximately 60°C-in/W. Therefore, the voids, scratches, and imperfections which are filled with a joint compound, will have a thermal resistance of about 1/20th of the original value which makes a significant reduction in the overall interface thermal resistance.

Joint compounds are a formulation of fine zinc particles in a silicon oil which maintains a grease-like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Experience will indicate whether the quantity is sufficient, as excess will appear around the edges of the contact area. To prevent accumulation of airborne particulate matter, excess

compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic-encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the assembly.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table I. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator and is therefore highly desirable despite the handling problems created by its affinity for foreign matter. Some sources of supply for joint compounds are shown in Appendix B.

Some users and heat-sink manufacturers prefer not to use compounds. This necessitates use of a heat sink with lower thermal resistance which imposes additional cost, but which may be inconsequential when low power is being handled. Others design on the basis of not using grease, but apply it as an added safety factor, so that if improperly applied, operating temperatures will not exceed the design values.

TABLE 1
Approximate Values for Interface Thermal Resistance and Other Package Data
(See Table II for Case Number to JEDEC Outline Cross-Reference)

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heat sink. (See Note 4.)

Package Type and Data					Interface Thermal Resistance (°C/W)					
JEDEC Outline	Description	Recommended Mounting Hole and Drill Size	Machine Screw Size[2]	Torque In-Lb	Metal-to-Metal		With Insulator			See Note
					Dry	Lubed	Dry	Lubed	Type	
Case 152*	Uniwatt	0.113, #33	4-40	6	5.0	3.8	7.4	5.4	2 mil Mica	3
DO-4	10-32 Stud 7/16" Hex	0.188, #12	10-32	20	0.3	0.2	1.6	0.8	3 mil Mica	
DO-5	1/4-28 Stud 11/16" Hex	0.250, #1	1/4-28	25	0.2	0.1	0.8	0.6	5 mil Mica	
DO-21	Pressfit, 1/2"	See Figure 8	–	–	0.15	0.10	–	–	–	
TO-3	Diamond Flange	0.140, #28	6-32	6	0.5	0.1	1.3	0.36	3 mil Mica	1
TO-66	Diamond Flange	0.140, #28	6-32	6	1.5	0.5	2.3	0.9	2 mil Mica	
TO-83 TO-94	1/2" 20 Stud 1-1/16" Hex	0.5, 0.5 –	1/2-20	130	–	0.1	–	–	–	
TO-126	Thermopad 1/4" x 3/8"	0.113, #33	4-40	6	2.0	1.3	4.3	3.3	2 mil Mica	
TO-127	Thermopad 1/2" x 5/8"	0.140, #28	6-32	8	1.6	0.8	2.6	1.8	2 mil Mica	
TO-202AC	Duowatt	0.140, #28	6-32	8	1.3	0.9	4.8	2.0	2 mil Mica	3
TO-220AB	Thermowatt	0.140, #28	6-32	8	1.2	1.0	3.4	1.6	2 mil Mica	1, 2

*Motorola Case Number

NOTE 1. See Figures 3 and 4 for additional data on TO-3 and TO-220 packages.

NOTE 2. Screw not insulated.

NOTE 3. Case thermocouple soldered to top of tab.

NOTE 4. **Measurement of Interface Thermal Resistance.** Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the semi, a thermocouple on the heat sink, and a means of applying and measuring DC power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are in poor agreement.

Consider the TO-220 package shown in the accompanying figure. The mounting pressure at one end causes the other end—where the die is located— to lift off the mounting surface slightly. To improve contact, Motorola TO-220 packages are slightly concave and use of a spreader bar under the screw lessens the lifting, but some is inevitable with a single-ended package.

The thermocouple locations are shown:

a. The Motorola location is directly under the die reached through a hole in the heat sink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.

b. The EIA location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.

c. The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

Temperatures at the three locations are generally not the same. Consider the situation depicted in the figure. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the EIA location is hotter than at the Thermalloy location and the Motorola location is even hotter. Since junction-to-sink thermal resistance is constant for a given setup, junction-to-case values decrease and case-to-sink values increase as the case thermocouple readings become warmer.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semi package and the heat sink, tightening the screw will not bow the package;

Table 1, Note 5 (continued)

instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heat sink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location could be close to the temperature at the EIA location as the lateral heat flow is generally small.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The Motorola location is chosen to obtain the highest temperature of the case at a point where, hopefully, the semi is making contact to the heat sink, since heat sinks are measured from the point of semi contact to the ambient. Once the special heat sink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1°C/W for a TO-220 package mounted to a heat sink without thermal grease and no insulator. This error is small when compared to the heat dissipators often used with this package, since power dissipation is usually a few watts. When compared to the specified junction-to-case values of some of the higher power semiconductors becoming available, however, the difference becomes significant, and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heat sink. The washer is flat to within 1 mil/inch, has a finish better than 63 μ-inch, and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is therefore application-oriented. It is also easy to use and yields reproducible results. At this printing, however, sufficient data to compare results to other methods is not available.

The only way to get accurate measurements of the interface resistance is to also test for junction-to-case thermal resistance at the same time. If the junction-to-case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

JEDEC TO-220 Package mounted to heat sink showing various thermocouple locations and lifting caused by pressure at one end.

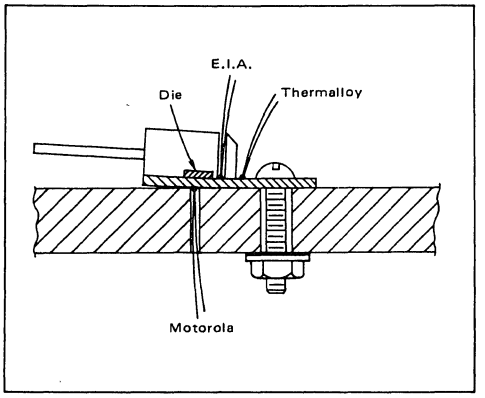


TABLE 2

Cross Reference Chart

Motorola Case Number to JEDEC Outline Number and Table 1 Reference

Motorola Number	JEDEC Number	Reference in Table 1
1	TO-3	TO-3
3	TO-3[2]	TO-3
9	TO-61	DO-5
11	TO-3	TO-3
11A	TO-3[2]	TO-3
12	TO-3[2]	TO-3
36	TO-60	DO-4
42A	DO-5	DO-5
44	DO-4	DO-4
54	TO-3[2]	TO-3
56	DO-4	DO-4
58	DO-5[2]	DO-5
77	TO-126	TO-126
80	TO-66	TO-66
86	TO-208[1]	DO-4
86L	TO-298[1]	DO-4
90	TO-127	TO-127
145C	TO-232[1]	DO-4
152	TO-202[1]	Case 152
160-03	TO-59	DO-4
167	DO-203[1] –1.25" hex	DO-4
157	DO-203[1]	DO-5
197	TO-3[2]	TO-3
199	TO-225[1]	TO-127
219	TO-94	TO-83
221	TO-220AB	TO-220AB
221A	TO-220AB	TO-220AB
235	TO-208[1]	DO-5
238	TO-208[1]	DO-5
239	TO-208	–
245	DO-4	DO-4
246	TO-83	TO-83
257-01	DO-5	DO-5
263	TO-208[1]	DO-5
283	DO-4	DO-4
285	TO-209[1]	TO-83
288	TO-208[1]	TO-83
289	TO-209[1]	DO-5
291	TO-94	TO-83
306	TO-202AC	TO-202AC

NOTE 1. Would fit within this family outline if registered with JEDEC.

NOTE 2. Not within all JEDEC outline dimensions. The data in Table 1 and suggested mounting hardware and procedures generally apply.

INSULATION CONSIDERATIONS

Since it is most expedient to manufacture power semiconductors with collectors or anodes electrically common to the case, the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, it is best to isolate the entire heat sink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heat sink. Where heat sink isolation is not possible, because of safety reasons or in instances where a chassis serves as a heat sink or where a heat sink is common to several devices, insulators are used to isolate the individual components from the heat sink.

When an insulator is used, thermal grease assumes greater importance than with a metal-to-metal contact, because two interfaces exist instead of one and some materials, such as mica, have a markedly uneven surface. Reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

Data obtained by Thermalloy, showing interface resistance for different insulators and torque applied to TO-3 and TO-220 packages, are shown in Figure 3 for bare surfaces and Figure 4 for greased surfaces. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction to case). When high power is handled, beryllium oxide is unquestionably the best choice. Thermafilm is Thermalloy's tradename for a polyimide material which is also commonly known as Kapton*; this material is fairly popular for low power applications because it is low cost, withstands high temperatures and is easily handled, in contrast to mica which chips and flakes easily.

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly so that having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the breakdown voltage of the insulation system. Because of these factors, which are not amenable to analysis, hi-pot testing should be done on prototypes and a large margin of safety employed. In some situations, it may be necessary to substitute "empty" packages for the semiconductors to avoid shorting them or to prevent the semiconductors from limiting the voltage applied during the hi-pot test.

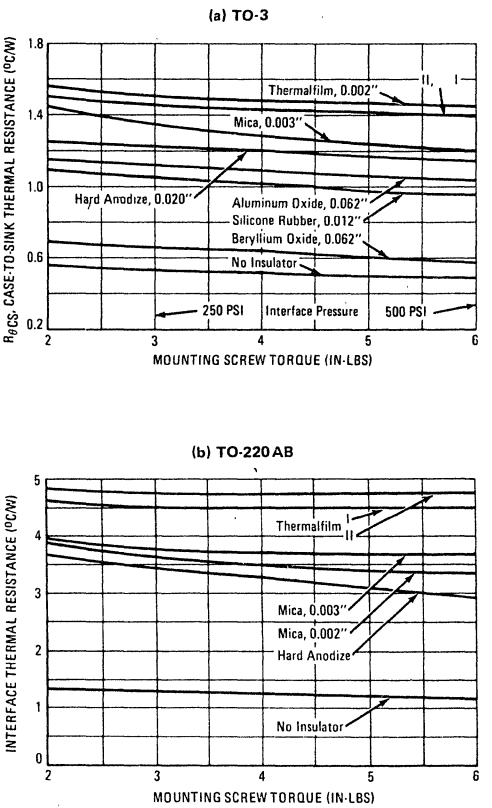


FIGURE 3 – Interface Thermal Resistance Without Thermal Grease as a Function of Mounting Screw Torque Using Various Insulating Materials

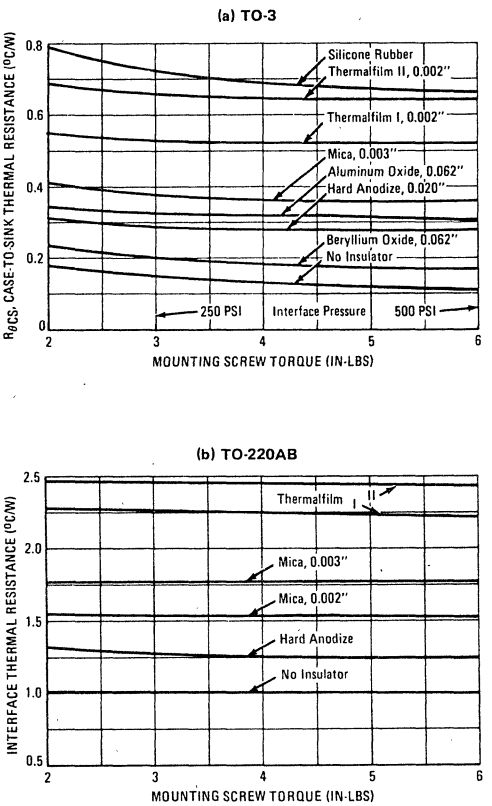


FIGURE 4 – Interface Thermal Resistance Using Thermal Grease as a Function of Mounting Screw Torque Using Various Insulating Materials

*®DuPont

FASTENER AND HARDWARE CHARACTERISTICS

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Washers

A very useful piece of hardware is the bell-type compression washer. As shown in Figure 5, it has the ability to maintain a fairly constant pressure over a wide range of physical deflection–generally 20% to 80%–thereby maintaining an optimum force on the package. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package or insulating washer caused by temperature changes. Bell type washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme.

Motorola washers designed for use with the Thermopad package maintain the proper force when properly secured. They are used with the large face contacting the packages.

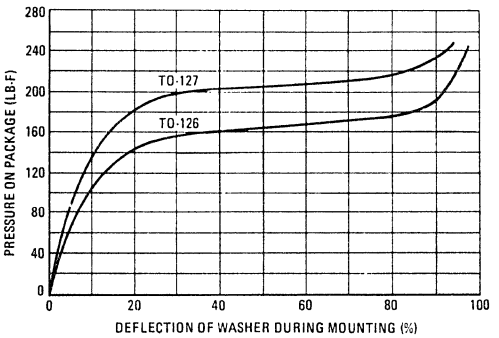


FIGURE 5 – Characteristics of the Bell Compression Washers Designed for Use with Thermopad Semiconductors

Machine Screws

Machine screws and nuts form a trouble-free fastener system for all types of packages which have mounting holes. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of any of the Thermopad plastic package types as the screw heads are not sufficiently flat to provide properly distributed force.

Self-Tapping Screws

Under some conditions, sheet-metal screws are acceptable. However, during the tapping process with a standard screw, a volcano-like protrusion will develop in the metal being threaded; a very unsatisfactory surface results. When used, a speed-nut must be used to secure a standard screw, or the type of screw must be used which roll-forms machine screw threads.

Eyelets

Successful mounting can also be accomplished with hollow eyelets provided an adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Rivets

When a metal flange-mount package is being mounted directly to a heat sink, rivets can be used. Rivets are not a recommended fastener for any of the plastic packages except for the tab-mount type. Aluminum rivets are preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

Insulators and Plastic Hardware

Because of its relatively low cost and low thermal resistance, mica is still widely used to insulate semiconductor packages from heat sinks despite its tendency to chip and flake. It has a further advantage in that it does not creep or flow so that the mounting pressure will not reduce with time in use. Plastic materials, particularly Teflon*, will flow. When plastic materials form parts of the fastening system, a compression washer is a valuable addition which assures that the assembly will not loosen with time.

FASTENING TECHNIQUES

Each of the various types of packages in use requires different fastening techniques. Details pertaining to each type are discussed in following sections. Some general considerations follow.

To prevent galvanic action from occurring when devices are used on aluminum heat sinks in a corrosive atmosphere, many devices are nickel- or gold-plated. Consequently, precautions must be taken not to mar the finish.

Manufacturers which provide heat sinks for general use and other associated hardware are listed in Appendix B. Manufacturer's catalogs should be consulted to obtain more detailed information. Motorola also has mounting hardware available for a number of different packages. Consult the Hardware Data Sheet for dimensions of the components and part numbers.

Specific fastening techniques are discussed in the remainder of this note for the following categories of semiconductor package.

1. Stud mount: DO-4, DO-5, DO-9, DO-30, TO-59, TO-60/63, TO-83, TO-93/94, etc.
2. Flange mount: DO-43, DO-44, TO-3, TO-37, TO-41, TO-53, TO-66, etc.
3. Pressfit: DO-21, DO-24, TO-203
4. Disc: DO-200 and TO-200 Families
5. Thermopad®: TO-126/7
6. Thermowatt®: TO-220 Family
7. Tab Mount (Duowatt® and Uniwatt®): TO-202 Family
8. RF Stripline: TO-119/121, TO-128/9, TO-216

*Trademark E. I. DuPont

Stud Mount

Mounting errors with stud-mounted parts are generally confined to application of excessive torque or tapping the stud into a threaded heat-sink hole. Both these practices may cause a warpage of the hex base which may crack the semiconductor die. The best fastening method is to use a nut and washer; the details are shown in Figure 6.

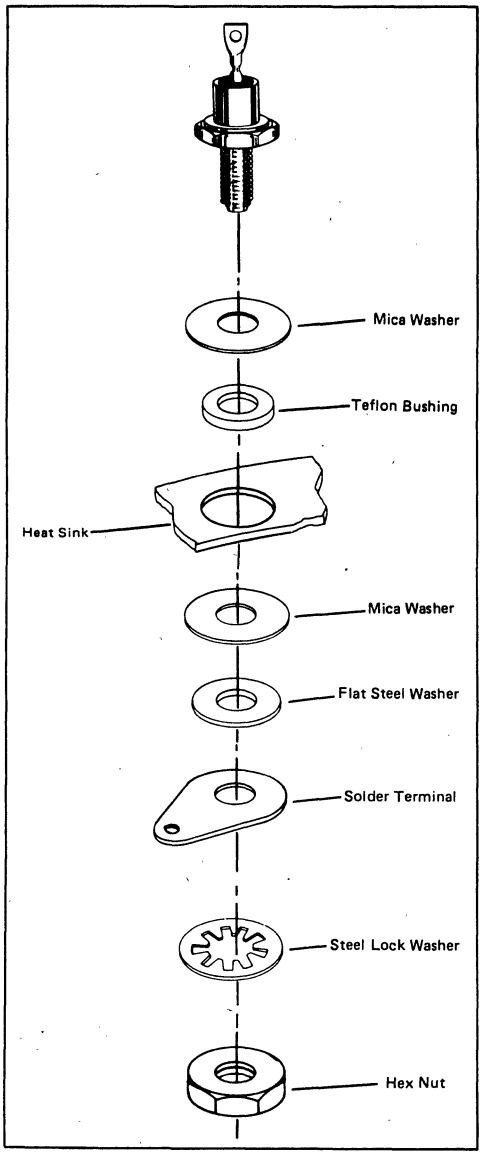


FIGURE 6 – Mounting Details For Stud-Mounted Semiconductors

Flange Mount

Few known mounting difficulties exist with this type of package. The rugged base and distance between die and mounting holes combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. A typical mounting installation is shown in Figure 7. Machine screws, self-tapping screws, eyelets, or rivets may be used to secure the package.

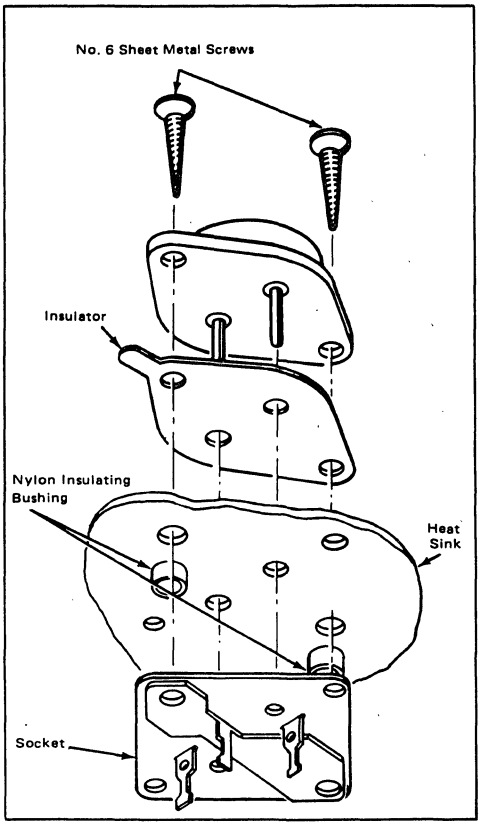


FIGURE 7 – Mounting Details for Flat-Base Mounted Semiconductors (TO-3 Shown).

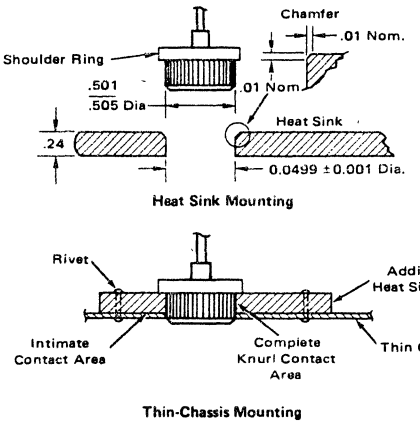
When not using a socket, machine screws tightened to their torque limits will produce lowest thermal resistance.

Press Fit

For most applications, the press-fit case should be mounted according to the instructions shown in Figure 8. A special fixture meeting the necessary requirements is a must.

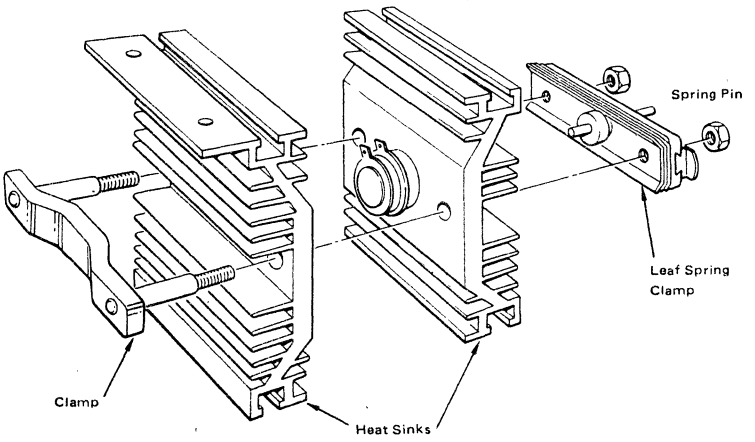
Disc

Disc type devices also require special handling. The details are shown in Figure 9.



The hole edge must be chamfered as shown to prevent shearing off the knurled edge of the case during press-in. The pressing force should be applied evenly on the shoulder ring to avoid tilting or canting of the case in the hole during the pressing operation. Also, the use of a thermal joint compound will be of considerable aid. The pressing force will vary from 250 to 1000 pounds, depending upon the heat-sink material. Recommended hardnesses are: copper—less than 50 on the Rockwell F scale; aluminum—less than 65 on the Brinell scale. A heat sink as thin as 1/8" may be used, but the interface thermal resistance will increase in direct proportion to the contact area. A thin chassis requires the addition of a backup plate.

FIGURE 8 – Mounting Details for Press-Fit Semiconductors



A self-leveling type mounting clamp is recommended to assure parallelism and even distribution of pressure on each contact area. A swivel type clamp or a narrow leaf spring in contact with the heat dissipator provides acceptable performance.

The clamping force should be applied smoothly, evenly, and perpendicularly to the semiconductor package to prevent deformation of the device or the heat-dissipator mounting surfaces during installation. The spring used should provide a mounting force within the range recommended by the semiconductor manufacturer; clamping forces usually range from 800 to 2000 pounds force depending upon the type number.

Installation of an assembly of disc-type semiconductors mounted between two heat dissipators should be done in a manner to permit one heat dissipator to move with respect to the other. Movement will avoid stresses being developed due to thermal expansion, which could damage the semiconductor.

Similarly, when two or more devices are to be operated electrically in parallel, one of the heat dissipators used may be common to all devices. Individual heat dissipators must be provided against the other mounting surfaces of the semiconductors so that the mounting force applied in each case will be independently adjustable.

FIGURE 9 – Mounting Details for Disc-Type Semiconductors

Thermopad

The Motorola Thermopad® plastic power packages have been designed to feature minimum size with no compromise in thermal resistance. This is accomplished by die-bonding the silicon chip on one side of a thin copper sheet; the opposite side is exposed as a mounting surface. The copper sheet has a hole for mounting, i.e., plastic is molded enveloping the chip but leaving the mounting hole open. The benefits of this construction are obtained at the expense of a requirement that strict attention be paid to the mounting procedure. Success in mounting Thermopad devices depends largely upon using a compression washer which provides a controllable pressure across a large bearing surface. Having a small hole with no chamfer and a flat, burr-free, well-finished heat sink are also important requirements.

Several types of fasteners may be used to secure the Thermopad package; machine screws, eyelets, or clips are preferred. With screws or eyelets, a bell compression washer should be used which applies the proper force to the package over a fairly wide range of deflection. Screws should not be tightened with any type of air-driven torque gun or equipment which may cause high impact. Characteristics of the recommended washers are shown in Figure 5.

Figure 10 shows details of mounting TO-126 or TO-127 devices. Use of the clip requires that caution be exercised to insure that adequate mounting force is applied. When electrical isolation is required, a bushing inside the mounting hole will insure that the screw threads do not contact the metal base.

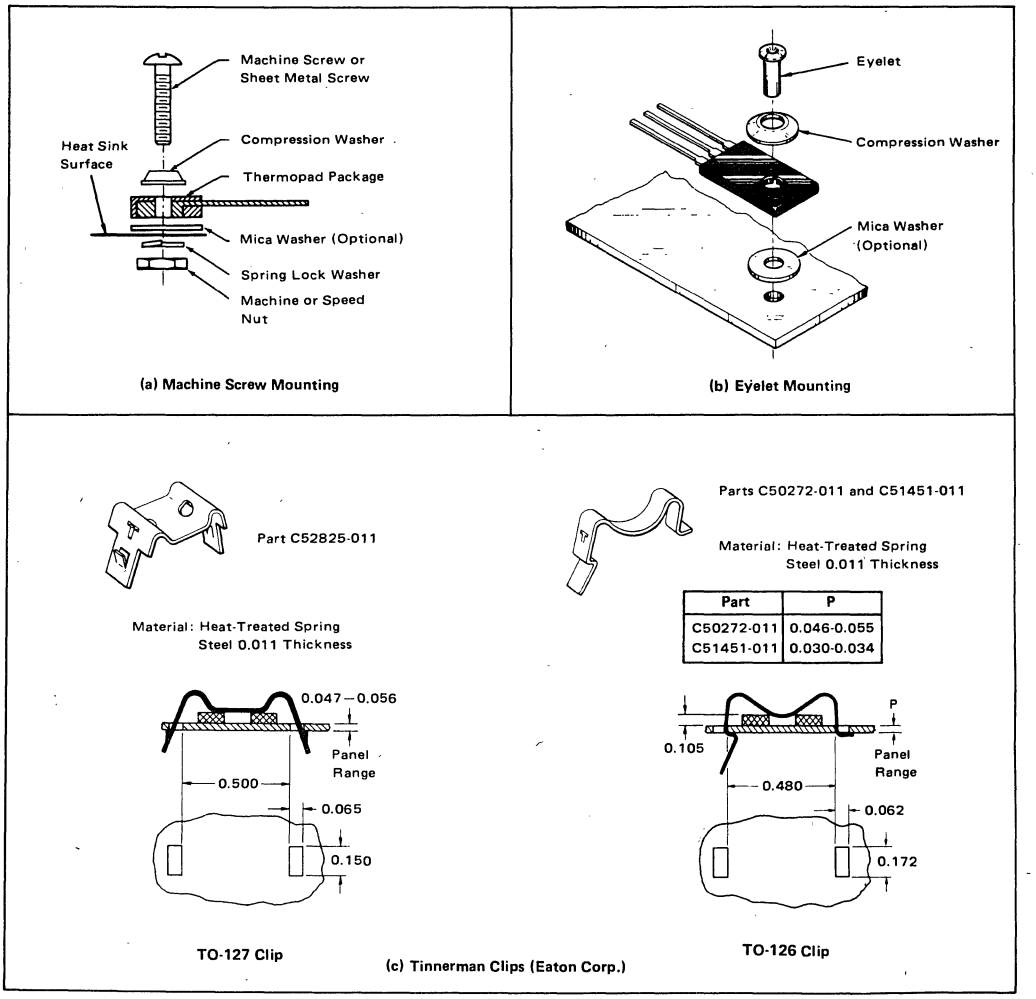


FIGURE 10 — Recommended Mounting Arrangements for TO-126 and TO-127 Thermopad Packages

The case 199 Thermopad is not more tolerant of mounting conditions than Case 77 or 90 parts even though the fastener does not bear on the plastic. The screw must not contact the semiconductor base plate as screw heads are not flat enough to apply pressure evenly and may cause warpage of the base plate resulting in die fracture. Procedures for mounting the Case 199 are shown in Figure 11.

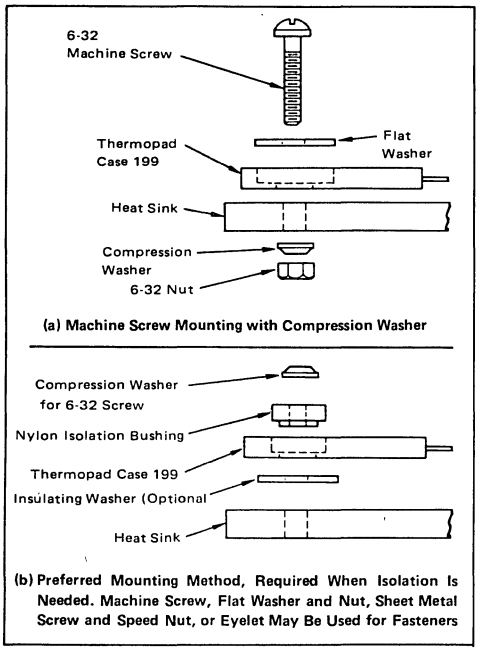


FIGURE 11 – Various Mounting Schemes For the Case 199 Thermopad

(a) shows direct contact with heat sink.
(b) shows technique when isolation is required.

Manual Assembly Should Be Used.

Thermowatt®

The popular TO-220 Thermowatt® package also requires attention to mounting details. Figure 12 shows suggested mounting arrangements and hardware. The rectangular washer shown in Figure 12a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate insulating bushings when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is suggested when using a 6-32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, Motorola TO-220 packages have a chamfer on one end. TO-220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

In situations where the Thermowatt package is making direct contact with the heat sink, an eyelet may be used, provided sharp blows or impact shock is avoided.

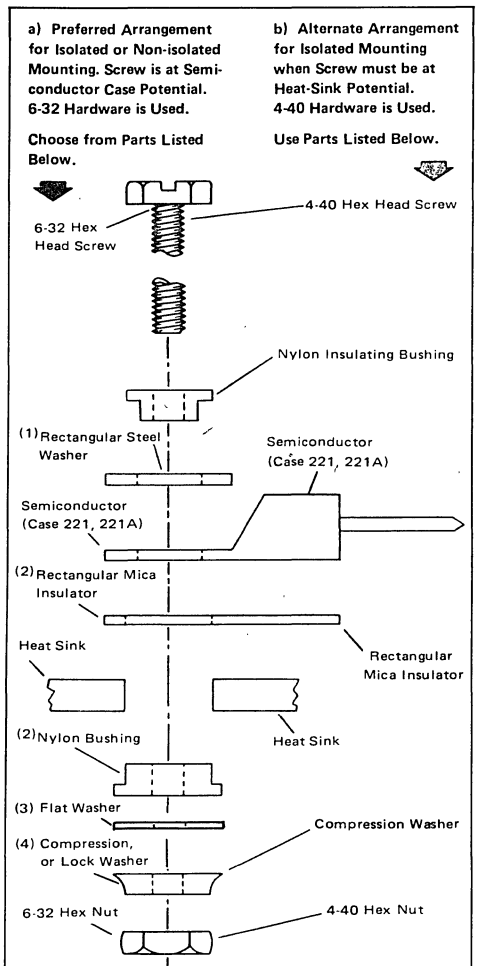


FIGURE 12 – Mounting Arrangements for Thermowatt Packages

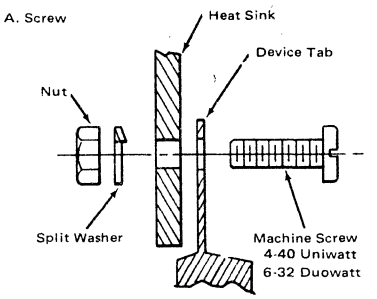
Tab Mount

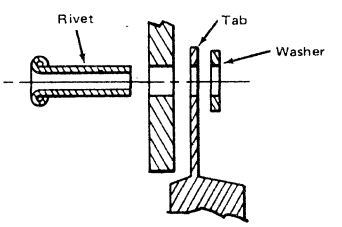
Although the Duowatt® and Uniwatt® packages are designed primarily for use in low-power applications where heat sinks are not required, they can be used to dissipate up to 10 watts if properly mounted to a heat sink. These packages are relatively rugged, since the mounting hole is not close to the die; mounting stresses, therefore, are not easily transmitted to the die.

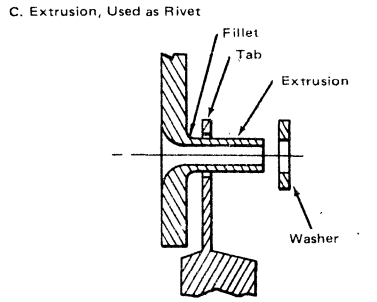
Figure 13 shows some possible mounting arrangements. An axial load of 300 lbs-force produces minimum contact thermal resistance. This is achieved at 6 in-lbs when a 4-40 machine screw is used. A sheet-metal screw and speed-nut can be substituted for the machine screw and nut, but torque readings are uncertain. The riveting technique should produce 300 lbs-force, using a gradually increasing pressure such as provided by an arbor press.

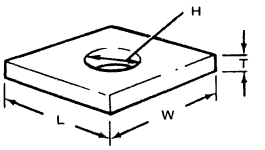
The extrusion requires a punch press to manufacture; however, it is potentially the least expensive technique. Note that the radius of the fillet must be small enough to allow the tab to lie flat on the heat sink. To utilize an existing chassis and board arrangement on heat sinking, it may be necessary to have the device lie flat on the chassis. In this case, the chassis mounting blocks shown in Figure 13d might be utilized. A possible application is shown in Figure 13e, where a complementary transistor pair is used. Insulated screws and mica insulating washers under the blocks must be used to prevent shorting of the collector circuits of the two transistors. Alternately, an insulated bushing and a #3 screw could be used to secure the packages.

To avoid the use of mounting blocks, a tab-forming option is available. Alternately, some equipment manufacturers have constructed heat sinks with a flat, raised island to permit the package to be flat. Users should not attempt to bend the tab as a cracked die is the probable result.



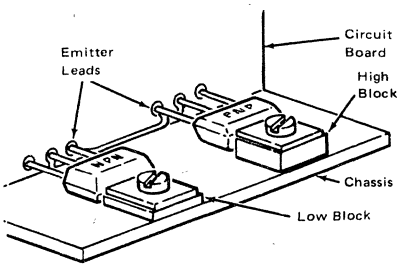






D. Chassis Mounting Block Details

	Block Dimensions				
	H	W	L	T	
				Low Block	High Block
Duowatt	0.140	0.4	0.5	0.07	0.12
Uniwatt	0.113	0.3	0.3	0.06	0.12



E. Chassis Mount Block, Mounting Details

Use Nylon Screws and Mica Insulating Washer to Prevent Shorting the Tabs to the Chassis, and Thus to Each Other.

FIGURE 13 – Methods of Mounting Duowatt and Uniwatt Transistors to a Heat Sink

R.F. Stripline

Besides the usual precautions regarding surface flatness and torque, the stripline package (see Figure 14a) requires attention to the following:

1. The device should never be mounted in such a manner as to place ceramic-to-metal joints in tension.
2. The device should never be mounted in such a manner as to apply force on the strip leads in a vertical direction towards the cap.
3. When the device is mounted in a printed circuit board with the copper stud or flange and BeO portion of the header passing through a hole in the circuit board, adequate clearance must be provided for the BeO to prevent shear forces from being applied to the leads.
4. Some clearance must be allowed between the leads and the circuit board when the device is properly secured to the heat sink.
5. The device should be properly secured into the heat sinks before the device leads are attached into the circuit.
6. The leads must not be used to prevent device rotation on stud type devices during stud torque application. A wrench flat is provided for this purpose.

Most of the considerations listed above are designed to prevent tension at the metal-ceramic interfaces on the SOE package. Improper mechanical design can lead to application of stresses to these joints resulting in device destruction. Three joints are considered: the cap to the BeO disc, the leads to the disc, and the stud or flange to the disc.

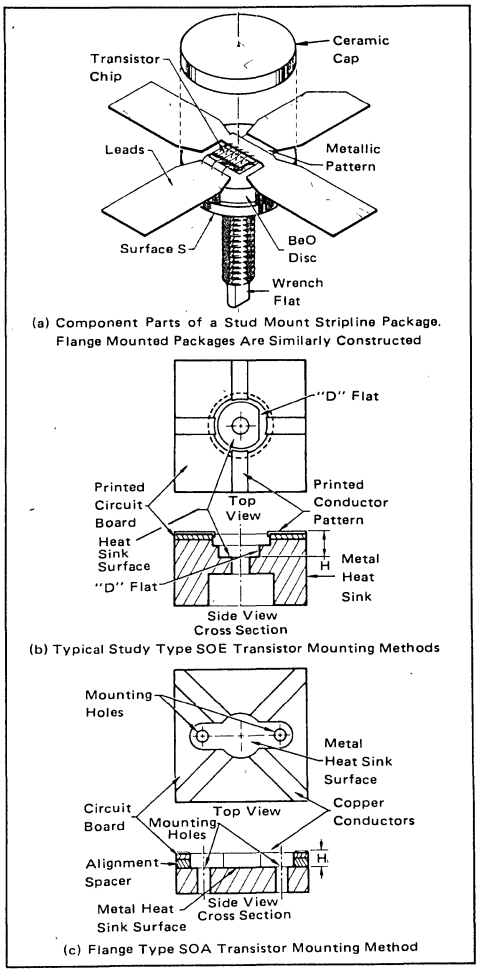
The joint between the ceramic cap and the BeO ceramic disc is composed of a material which loses strength above 175°C. While the strength of the material returns upon cooling, any force applied to the cap at high temperature may result in failure of the cap to ceramic joint.

Figure 14b shows a cross-section of a printed circuit board and heat-sink assembly for mounting a stud type stripline device. H is the distance from the top surface of the printed circuit board to the D-flat heat-sink surface. If H is less than the minimum distance from the bottom of the lead material to the mounting surface of the package, there is no possibility of tensile forces in the copper stud–BeO ceramic joint. If, however, H is greater than the package dimension, considerable force is applied to the cap to BeO joint and the BeO to stud joint. Two occurances are possible at this point. The first is a cap joint failure when the structure is heated, as might occur during the lead-soldering operation; while the second is BeO to stud failure if the force generated is high enough. Lack of contact between the device and the heat-sink surface will occur as the differences between H and the package dimension becomes larger, this may result in device failure as power is applied.

Figure 14c shows a typical mounting technique for flange-type stripline transistors. Again, H is defined as the distance from the top of the printed circuit board to the heat-sink surface. If distance H is less than the minimum distance from the bottom of transistor lead to the bottom surface of the flange, tensile forces at the various joints in the package are avoided. However, if distance H exceeds the package dimension, problems similar to those discussed for the stud type devices can occur. Because of the ability of the copper flange to bend under the types of loads encountered when the mounting screws are tightened, permanent deformation of the flange may result. Corrective action after the flange has been bent will not necessarily insure proper thermal contact with the heat sink.

The flange surface as supplied with Motorola transistors is either flat or slightly convex. It is important that the mating heat-sink surface also be flat or slightly convex to provide the best contact when the device is properly secured.

Since the flange may be permanently deformed during mounting, the device should not be dismounted and remounted in another position, without checking the flatness. The flange may be resurfaced using emery cloth mounted on a large, flat block. While this removes the gold- or nickel-plating, the thin layer of copper oxide which rapidly forms causes an insignificant increase in thermal resistance, although corrosion may occur.



(a) Component Parts of a Stud Mount Stripline Package. Flange Mounted Packages Are Similarly Constructed

(b) Typical Study Type SOE Transistor Mounting Methods

(c) Flange Type SOA Transistor Mounting Method

FIGURE 14 – Mounting Details for SOE Transistors

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FREE AIR AND SOCKET MOUNTING

In applications where average power dissipation is of the order of a watt or so, power semiconductors may be mounted with little or no heat-sinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked glass-to-metal seals around the leads. The plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heat sink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance.

In many situations, because its leads are fairly heavy, the TO-127 package has supported a small heat sink; however, no definitive data is available. When using a small heat sink, it is good practice to have the sink rigidly mounted such that the sink or the board is providing total support for the semiconductor. Two possible arrangements are shown in Figure 15. The arrangement of part (a) could be used with any plastic package, but the scheme of part (b) is more practical with Case 77 or Case 90 Thermopad devices. With the other package types, mounting the transistor on top of the heat sink is more practical.

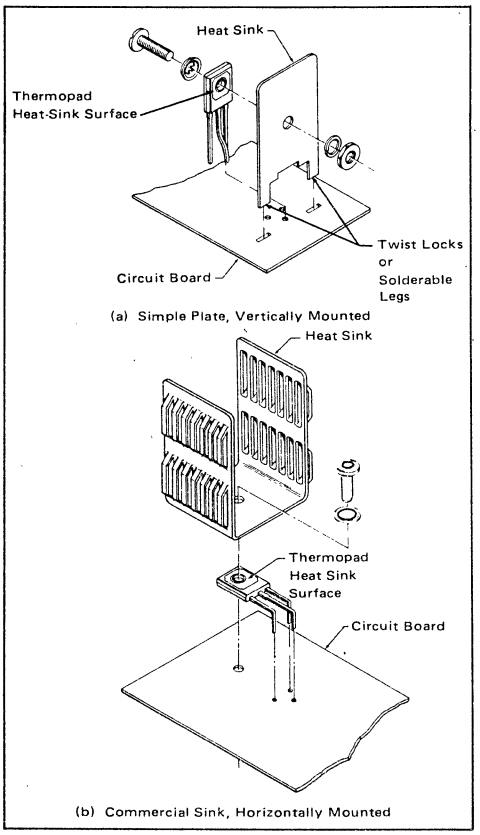

FIGURE 15 – Methods of Using Small Heat Sinks With Plastic Semiconductor Packages

In certain situations, in particular where semiconductor testing is required, sockets are desirable. Manufacturers have provided sockets for all the packages available from Motorola. The user is urged to consult manufacturers' catalogs for specific details.

HANDLING PINS, LEADS, AND TABS

The pins and lugs of metal-packaged devices are not designed for any bending or stress. If abused, the glass-to-metal seals could crack. Wires may be attached using sockets, crimp connectors, or solder, provided the data-sheet ratings are observed.

The leads and tabs of the plastic packages are more flexible and can be reshaped, although this is not a recommended procedure for users to do. In some cases, a heat sink can be chosen which makes lead-bending unnecessary. Numerous lead- and tab-forming options are available from Motorola. Preformed leads remove the risk of device damage caused by bending from the users.

If, however, lead-bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantitites of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

The following rules should be observed to avoid damage to the package.

1. A lead-bend radius greater than 1/16 inch is advisable for TO-126, 1/10 inch for TO-127 and Case 199, and 1/32 inch for TO-220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. An acceptable lead-forming method that provides this relief is to incorporate an S-bend into the lead. Wire-wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 275°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions.

CLEANING CIRCUIT BOARDS

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices.

Alcohol and unchlorinated Freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline may cause the encapsulant to swell, possibly damaging the

transistor die. Likewise, chlorinated Freon solvents are unsuitable, since they may cause the outer package to dissolve and swell.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if the packages are free-standing without support.

THERMAL SYSTEM EVALUATION

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see Motorola Application Note, AN-569.

Other applications, notably RF power amplifiers or switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area or thyristor di/dt limits, as applicable, must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A.) A fine wire thermocouple should be used, such as #32AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R_{\theta JC} \times P_D$$

where T_J = junction temperature (^oC)
T_C = case temperature (^oC)
$R_{\theta JC}$ = thermal resistance junction-to-case as specified on the data sheet ($^oC/W$)
P_D = power dissipiated in the device (W).

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

Graphical Integration

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instantaneous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation.

Substitution

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the "test" position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

APPENDIX A

THERMAL RESISTANCE CONCEPTS

The basic equation for heat transfer under steady-state conditions is generally written as:

$$q = hA\Delta T \quad (1)$$

where q = rate of heat transfer or power dissipation (P_D),
h = heat transfer cofficient,
A = area involved in heat transfer,
ΔT = temperature difference between regions of heat transfer.

However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance, R_θ, is

$$R_\theta = \Delta T/q = 1/hA \quad (2)$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm's Law is often made to form models of heat flow. Note that ΔT could be thought of as a voltage; thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure A1.

The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A \quad (3)$$

where T_J = junction temperature,
P_D = power dissipation,
$R_{\theta JC}$ = semiconductor thermal resistance (junction to case),
$R_{\theta CS}$ = interface thermal resistance (case to heat sink),
$R_{\theta SA}$ = heat sink thermal resistance (heat sink to ambient),
T_A = ambient temperature.

The thermal resistance junction to ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

The value for the interface thermal resistance, $R_{\theta CS}$, is affected by the mounting procedure and may be significant compared to the other thermal-resistance terms.

The thermal resistance of the heat sink is not constant; it decreases as ambient temperature increases and is affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. In some applications such as in RF power amplifiers and short-pulse applications, the concept may be invalid because of localized heating in the semiconductor chip.

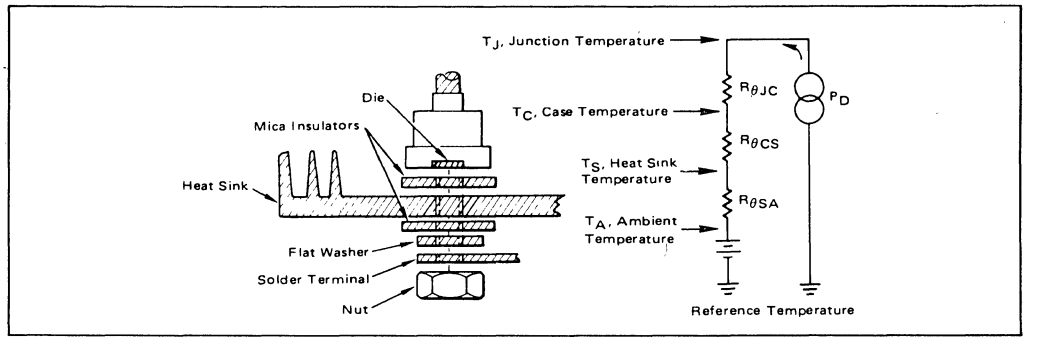

FIGURE A1 – Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor

APPENDIX B
SOURCES OF ACCESSORIES

		Insulators						Heat Sinks					
Manufacturer	Joint Compound	BeO	AlO_2	Anodize	Mica	Plastic Film	Silicone Rubber	Stud	Flange	Disc	Thermowatt	Uni/Duo Watt	RF Stripline
Aavid Eng.	Ther-o-link 1000	–	–	–	–	–	–	X	X	–	X	–	–
AHAM	–	–	–	–	–	–	–	X	X	–	X	–	–
Astrodyne	#829	–	–	–	–	–	–	X	X	X	X	X	–
Delbert Blinn	–	X	–	X	X	X	X	X	X	–	–	–	–
IERC	Thermate	–	–	–	–	–	–	X	X	–	X	X	X
Staver	–	–	–	–	–	–	–	X	X	–	X	X	X
Thermalloy	Thermacote	X	X	X	–	X	–	X	X	X	X	X	X
Tor	TJC	X	–	X	X	X	–	X	X	–	X	–	–
Tran-tec	XL500	X	–	–	–	X	X	X	X	X	X	X	X
Wakefield Eng.	Type 120	X	–	X	–	–	–	X	X	X	X	X	–
Wei Corp.	–	–	–	–	–	–	–	X	X	–	–	–	–

Other sources for Joint Compounds: Dow Corning, Type 340
Emerson & Cuming, Eccoshield – SO (Electrically Conducting)
Emerson & Cuming, Eccotherm – TC-4 (Electrically Insulating)

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APPENDIX B
SUPPLIERS ADDRESSES

Aavid Engineering, Inc., 30 Cook Court, Laconia, New Hampshire 03246 (603) 524-4443

AHAM Heat Sinks, 27901 Front Street, Rancho, California 92390 (714) 676-4151

Astrodyne, Inc., 353 Middlesex Avenue, Wilmington, Massachusetts 01887 (617) 272-3850

Delbert Blinn Company, P.O. Box 2007, Pomona, California 91766 (714) 623-1257

Dow Corning, Savage Road Building, Midland, Michigan 48640 (517) 636-8000

Eaton Corporation, Engineered Fasteners Division, Tinnerman Plant, P.O. Box 6688, Cleveland, Ohio 44101 (216) 523-5327

Emerson & Cuming, Inc., Dielectric Materials Division, 869 Washington Street, Canton, Massachusetts 02021 (617) 828-3300

International Electronics Research Corporation, 135 West Magnolia Boulevard, Burbank, California 91502 (213) 849-2481

The Staver Company, Inc., 41-51 North Saxon Avenue, Bay Shore, Long Island, New York 11706 (516) 666-8000

Thermalloy, Inc., P.O. Box 34829, 2021 West Valley View Lane, Dallas, Texas 75234 (214) 243-4321

Tor Corporation, 14715 Arminta Street, Van Nuys, California 91402 (213) 786-6524

Tran-tec Corporation, P.O. Box 1044, Columbus, Nebraska 68601 (402) 564-2748

Wakefield Engineering, Inc., Wakefield, Massachusetts 01880 (617) 245-5900

Wei Corporation, 1405 South Village Way, Santa Ana, California 92705 (614) 834-9333

Rectifier and Zener Diode Selector Guide

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These selector guides are included as a quick reference to Motorola product lines often used in conjunction with power devices.

RECTIFIERS

General-Purpose Rectifiers

Motorola offers a wide variety of low-cost devices, packaged to meet diverse mounting requirements. Of particular interest are plastic "buttons", such as the MR2500 series, designed for clip or recessed mounting, and the new plastic DO-4 stud-mounts, derived from these buttons, types MR2000S and MR2500S. All listed lines are available with anode-to-case connection by adding "R" suffix to the standard part number.

	I_O, AVERAGE RECTIFIED FORWARD CURRENT (Amperes)								
	1.0	1.5	30				6.0	12	
	59-01 (DO-41)	59-04 (DO-15) Plastic	60 Metal	70 Metal	267 Plastic		194 Plastic	245 (DO-4) Metal	283-01 (DO-4) Plastic
V_{RRM} Volts									
50	1N4001	1N5391	1N4719	1N4997	MR500	1N5400	MR750	MR1120 1N1199,A,B	1N1199C
100	1N4002	1N5392	1N4720	1N4998	MR501	1N5401	MR751	MR1121 1N1200,A,B	1N1200C
200	1N4003	1N5393	1N4721	1N4999	MR502	1N5402	MR752	MR1122 1N1202,A,B	1N1202C
400	1N4004	1N5395	1N4722	1N5000	MR504	1N5404	MR754	MR1124 1N1204,A,B	1N1204C
600	1N4005†	1N5397	1N4723	1N5001	MR506	1N5406	MR756	MR1126 1N1206,A,B	1N1206C
800	1N4006†	1N5398	1N4724	1N5002	MR508	1N5407	MR758	MR1128 1N3988	
1000	1N4007†	1N5399	1N4725	1N5003	MR510	1N5408	MR760	MR1130 1N3990	
I_{FSM} (Amps)	30	50	300	300	100	200	400	300	400
T_A @ Rated I_O (°C)	75	T_L = 70	75	75	95	T_L = 105°C	60		
T_C @ Rated I_O (°C)								150	150
T_J (Max) (°C)	175	175	175	175	175	175	175	190	200

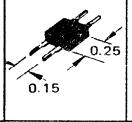
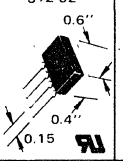
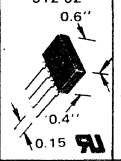
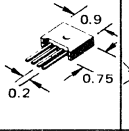
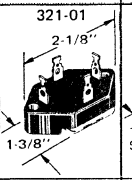
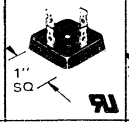
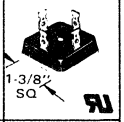
† Package Size: 0.120" Max Diameter by 0.260" Max Length

I_O, AVERAGE RECTIFIED FORWARD CURRENT (Amperes)									
15	20			25		30	35	40	50
42A (DO-5) Metal	42A (DO-5) Metal	283-01 (DO-4) Plastic	283-01 (DO-4) Plastic	193-03 Plastic	43 (DO-21) Metal	43 (DO-21) Metal	42A (DO-5) Metal	42A (DO-5) Metal	43-04 Metal
									
1N3208	1N248B 1N1191	MR2000S	MR2500S	MR2500	1N3491	1N3659	1N1183	1N1183A	MR5005
1N3209	1N249B 1N1192	MR2001S	MR2501S	MR2501	1N3492	1N3660	1N1184	1N1184A	MR5010
1N3210	1N250B 1N1194	MR2002S	MR2502S	MR2502	1N3493	1N3661	1N1186	1N1186A	MR5020
1N3212	1N1196 1N1196A	MR2004S	MR2504S	MR2504	1N3495	1N3663	1N1188	1N1188A	MR5040
1N3214	1N1198A 1N3214	MR2006S	MR2506S	MR2506	MR328	CF	1N1190	1N1190A	CF
CF	CF	MR2008S	MR2508S	MR2508	MR330	CF	1N3766	CF	CF
CF	CF	MR2010S	MR2510S	MR2510	MR331	CF	1N3768	CF	CF
250	350	400	600	400	300	400	400	800	600
150	150	150	150	150	130	100	140	150	150
175					175	175	190	190	195

▲ Request Data Sheet for Mounting Information
CF: Consult Factory

Rectifier Bridges

Motorola SUPERBRIDGES offer cost effectiveness and reliability in single phase applications. Chip/leadframe techniques are used for lower-current types, while the higher current assemblies combine pretested "button" rectifier cells for low assembly cost and high yields. Performance of four individual diodes is achieved at the cost of only two, with reliability of the whole assembly comparable to that of a single unit. The higher current assemblies feature versatile slip-on/solder/wire wrap terminals.

	I_O, DC OUTPUT CURRENT (Amperes)						
	1.5	1.0	2.0	4.0/8.0*	12	25	35
	109-03 	312-02 	312-02 	117 	321-01 	309A-03 	309A-02 
V_{RRM} Volts							
50	MDA920A2	3N246 MDA100A	3N253 MDA200	MDA970-1	MDA1200	MDA2500	MDA3500 BYW60
100	MDA920A3	3N247 MDA101A	3N254 MDA201	MDA970-2	MDA1201	MDA2501	MDA3501 BYW61
200	MDA920A4	3N248 MDA102A	3N255 MDA202	MDA970-3	MDA1202	MDA2502	MDA3502 BYW62
400	MDA920A6	3N249 MDA104A	3N256 MDA204	MDA970-5	MDA1204	MDA2504	MDA3504 BYW64
600	MDA920A7	3N250 MDA106A	3N257 MDA206	CF	MDA1206	MDA2506	MDA3506 BYW66
800	MDA920A8	3N251 MDA108A	3N258 MDA208				MDA3508 BYW68
1000	MDA920A9	3N252 MDA110A	3N259 MDA210				MDA3510
I_{FSM} (Amp)	32	45	60	100	400	400	400
T_A @ Rated I_O (°C)	50	75	55	*			
T_C @ Rated I_O (°C)				*	100	55	55
T_J (Max) (°C)	175	150	175	150	175	175	175

CF: Consult Factory

UL RECOGNIZED

*4.0 A @ T_A = 25°C
8.0 A @ T_C = 55°C

Dimensions given are nominal

SUPERBRIDGES is a trademark of Motorola Inc.

Fast Recovery Rectifiers

. . . available for designs requiring a power rectifier having maximum switching times ranging from 200 ns to 750 ns. These devices are offered in current ranges of 1.0 to 50 amperes and in voltages to 600 volts. Higher voltages are available upon request, but a necessary trade-off against switching speeds results. Reverse polarity (anode to case) obtained by adding an "R" suffix.

	I_O, AVERAGE RECTIFIED FORWARD CURRENT (Amperes)												
	1.0		3.0				5.0	6.0	12	20	30	40	50
	59-04 Plastic 		60 Metal 	70 Metal 	267-01 Plastic 		194 Plastic 	5C-02 (DO-4) Metal Note 1 		257 (DO-5) Metal Notes 2, 3 		42A (DO-5) Metal 	
V_{RRM} (Volts)													
50	1N4933†	MR810	MR830	MR800	MR850	MR910	MR820	1N3879	1N3889	1N3899	1N3909	MR860	MR870
100	1N4934†	MR811	MR831	MR801	MR851	MR911	MR821	1N3880	1N3890	1N3900	1N3910	MR861	MR871
200	1N4935†	MR812	MR832	MR802	MR852	MR912	MR822	1N3881	1N3891	1N3901	1N3911	MR862	MR872
400	1N4936†	MR814	MR834	MR804	MR854	MR914	MR824	1N3883	1N3893	1N3903	1N3913	MR864	MR874
600	1N4937†	MR816	MR836	MR806	MR856	MR916	MR826	MR1366	MR1376	MR1386	MR1396	MR866	MR876
800		MR817				MR917							
1000		MR818				MR918							
I_{FSM} (Amps)	30	30	100	100	100	100	300	150	200	250	300	350	400
T_A @ Rated I_O (°C)	75	75			90*	90*	55*						
T_C @ Rated I_O (°C)			100	100				100	100	100	100	100	100
T_J (Max) (°C)	150	150	150	150	175	175	175	150	150	150	150	160	160
t_{rr} (μs)	0.2	0.75	0.2	0.2	0.2	0.75	0.2	0.2	0.2	0.2	0.2	0.2	0.2

*Must be derated for reverse power dissipation. See Data Sheet.
†Package Size: 0.120" Max Diameter by 0.260" Max Length

JAN/JANTX(V) available

NOTES: 1. Also available in economical Case 245; add suffix –245 to part number. (Not applicable in JAN or JTX.)
2. Also available in economical Case 42A; add suffix –42A to part number. (Not applicable in JAN or JTX.)
3. Braided lead top terminal configuration available; consult your Sales Representative.

Schottky Rectifiers

Refinements in processing of SWITCHMODE Schottky Power Rectifiers are producing ruggedness and temperature performance comparable to silicon-junction rectifiers, with the high speed and low forward voltage drop characteristic of Schottky's metal/silicon junctions. Ideal for use in low voltage, high frequency power supplies and as very fast clamping diodes, these devices feature switching times less than 10 ns, and are offered in current ranges from 0.5 to 75 amperes, and reverse voltages to 45.

	I_O, AVERAGE RECTIFIED FORWARD CURRENT (Amperes)								
	0.5	1.0		3.0		3.0	5.0	15	
	51-02 (DO-7) Glass	59-04 Plastic		267 Plastic		60 Metal		245 (DO-4) Metal	
									
V_{RRM} (Volts)									
20	MBR020	1N5817	MBR120P	1N5820	MBR320P	MBR320M	1N5823	1N5826	MBR1520
30	††MBR030	1N5818	MBR130P	1N5821	MBR330P	MBR330M	1N5824	1N5827	MBR1530
35			MBR135P		MBR335P	MBR335M			MBR1535
40	MBR040	1N5819	MBR140P	1N5822	MBR340P	MBR340M	††1N5825	1N5828	MBR1540
45									
I_{FSM} (Amps)	5.0	100	50	250	200	500	500	500	500
†T_C @ Rated I_O (°C)								85	80
T_A @ Rated I_O PC Board Mount (°C)	50								
†T_L @ Rated I_O (°C)		90	80	95	85	90	80		
T_J(Max) (°C)	125	125	125	125	125	125	125	125	125
Max V_F @ $I_{FM} = I_O$	*0.55 T_L = 25°C	*0.60 T_L = 25°C	0.65 T_L = 25°C	*0.525 T_L = 25°C	0.60 T_L = 25°C	0.45 @ 5 A T_C = 25°C	*0.38 T_C = 25°C	*0.50 T_C = 25°C	0.55 T_C = 25°C

* Values are for the 40-Volt units. The lower voltage parts provide lower limits.
† Must be derated for reverse power dissipation. See Data Sheet.
†† Motorola TX versions available, consult factory.

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I_O, AVERAGE RECTIFIED FORWARD CURRENT (Amperes)									
25			35	40			50	60	75
245 (DO-4) Metal				257 (DO-5) Metal Note 1		430-2 (DO-21) Metal	257 (DO-5) Metal Note 1		
									
1N5829	MBR2520		MBR3520	1N5832	MBR4020	MBR4020PF		MBR6020	MBR7520
1N5830	MBR2530	1N6095	SD41	1N5833	MBR4030	MBR4030PF	1N6097	SD51	MBR7530
	MBR2535		MBR3535		MBR4035	MBR4035PF		MBR6035	MBR7535
†1N5831	MBR2540	1N6096		1N5834	MBR4040		1N6098		MBR7540
			†MBR3545					†MBR6045	MBR7545
800	800	400	600	800	800	800	800	800	1000
85	80	70	90	75	70	50	70	90	90
125	125	125	150	125	125	125	125	150	150
*0.48 T_C = 25°C	0.55 T_C = 25°C	0.86 @ 78.5 A T_C = 70°C	0.70 @ 78.5 A T_C = 125°C	*0.59 T_C = 25°C	0.63 T_C = 25°C	0.63 T_C = 25°C	0.86 @ 157 A T_C = 70°C	0.80 @ 157 A T_C = 125°C	0.90 @ 220 A T_C = 125°C

Capable of 150°C junction temperature operation.

(1) Braided lead top terminal configuration available; consult your Sales Representative.

†Motorola TX versions available, consult factory.

ZENER DIODES

Zener and Avalanche Regulator Diodes

Motorola's standard Zeners and Avalanche Regulator diodes comprise the largest inventoried line in the industry. Continuous development of improved manufacturing techniques have resulted in computerized diffusion and test, as well as critical process controls learned from surface-sensitive MOS fabrication. Resultant high yields lower factory costs. Check the following features for application to your specific requirements:

- Wide selection of package materials and styles:
  - Plastic (Surmetic) for low cost, mechanical ruggedness
  - Glass for highest reliability, lowest cost
  - Metal for highest power
- Power ratings from 0.25 to 50 Watts
- Breakdown voltages from 1.8 to 200 V in approximately 10% steps
- Available tolerances from 20% (low cost) to as tight as 1% (critical applications) with off-the-shelf delivery
- Special selection of electrical characteristics available at low cost due to high-volume lines (check your Motorola sales representative for special quotations)
- JAN/JANTX (V) availability (designated by tint)
- Special glass now used in DO-35 packages is compatible with low temperature alloy processes, yielding sharper breakdown and low leakage.

NOTES

1. The Zener Voltage is measured at approximately 1/4 the rated power, except for the MZ4614/1N4099 series. This series is measured with I_{ZT} = 250 μAdc. The 1N4370/1N746 series is measured with I_{ZT} = 20 mAdc.
2. Contact your Motorola representative for information on intermediate voltages and tighter tolerances.

Tolerances

3. No suffix = ±5%
4. No suffix = ±20%, A suffix = ±10% } with guaranteed limits on V_Z, V_F, and I_R only
   B suffix = ±5%
   C suffix = ±2%
   D suffix = ±1%
5. 1N4370/1N746 series: No suffix = ±10%, A suffix = ±5%
   1N957 series: No Suffix = ±20%, A suffix = ±10%, B suffix = ±5%
6. No suffix = ±10%, with guaranteed limits on V_Z, V_F, and I_R only
   A suffix = ±10%
   B suffix = ±5%

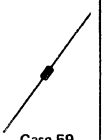
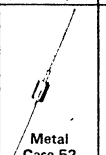
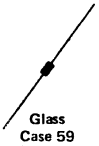
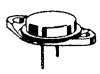
JAN/JANTX(V) available, ±5% only.

†Military parts in 1N4370/746/962 series at standard 1N985–1N992 supplied in DO-7.

#1N5271 – 1N5281 supplied in Surmetic DO-7.

Nominal Zener Voltage	250 MILLIWATT (400 mW Package) Low Noise Cathode = Polarity Mark	400 MILLIWATT Low Noise Low Leakage Cathode = Polarity Mark	500 MILLIWATT Cathode = Polarity Mark	
(Note 1)	(Notes 2, 3)	(Notes 2, 4)	(Notes 2,5)	(Notes 2,6)
	 Glass Case 51 (DO-7)		 Glass (DO-35)†	
1.8	MZ4614			
2.0	MZ4615			
2.2	MZ4616			
2.4	MZ4617		1N4370	1N5221
2.7	MZ4618		1N4371	1N5223
3.0	MZ4619		1N4372	1N5225
3.3	MZ4620	1N5518	1N746	1N5226
3.6	MZ4621	1N5519	1N747	1N5227
3.9	MZ4622	1N5520	1N748	1N5228
4.3	MZ4623	1N5521	1N749	1N5229
4.7	MZ4624	1N5522	1N750	1N5230
5.1	MZ4625	1N5523	1N751	1N5231
5.6	MZ4626	1N5524	1N752	1N5232
6.2	MZ4627	1N5525	1N753	1N5234
6.8	1N4099	1N5526	1N754, 1N957	1N5235
7.5	1N4100	1N5527	1N755, 1N958	1N5236
8.2	1N4101	1N5528	1N756, 1N959	1N5237
8.7	1N4102			1N5238
9.1	1N4103	1N5529	1N757, 1N960	1N5239
10	1N4104	1N5530	1N758, 1N961	1N5240
11	1N4105	1N5531	1N962	1N5241
12	1N4106	1N5532	1N759, 1N963	1N5242
13	1N4107	1N5533	1N964	1N5243
14	1N4108	1N5534		1N5244
15	1N4109	1N5535	1N965	1N5245
16	1N4110	1N5536	1N966	1N5246
17	1N4111	1N5537		1N5247
18	1N4112	1N5538	1N967	1N5248
19	1N4113	1N5539		1N5249
20	1N4114	1N5540	1N968	1N5250
22	1N4115	1N5541	1N969	1N5251
24	1N4116	1N5542	1N970	1N5252
25	1N4117	1N5543		1N5253
27	1N4118		1N971	1N5254
28	1N4119	1N5544		1N5255
30	1N4120	1N5545	1N972	1N5256
33	1N4121	1N5546	1N973	1N5257
36	1N4122		1N974	1N5258
39	1N4123		1N975	1N5259
43	1N4124		1N976	1N5260
47	1N4125		1N977	1N5261
51	1N4126		1N978	1N5262
56	1N4127		1N979	1N5263
60	1N4128			1N5264
62	1N4129		1N980	1N5265
68	1N4130		1N981	1N5266
75	1N4131		1N982	1N5267
82	1N4132		1N983	1N5268
87	1N4133			1N5269
91	1N4134		1N984	1N5270
100	1N4135		1N985	1N5271#
110			1N986	1N5272#
120			1N987	1N5273#
130			1N988	1N5274#
140				1N5275#
150			1N989	1N5276#
160			1N990	1N5277#
170				1N5278#
180			1N991	1N5279#
200			1N992	1N5281#

ZENER AND AVALANCHE REGULATOR DIODES (continued)

Nominal Zener Voltage	1 WATT Cathode = Polarity Mark	1 WATT Cathode to Case Metal Case 52 (DO-13)	1.5 WATT Cathode = Polarity Mark	1.5 WATT Cathode to Case	5 WATT Cathode = Polarity Mark	10 WATT Cathode to Case = 1N3993 Series Anode to Case = 1N2970 Series	50 WATT Anode to Case	
(Note 1)	(Notes 2, 7)	(Notes 2, 8)	(Notes 2, 9)	(Notes 2, 10)	(Notes 2, 11)	(Notes 2, 10)	(Notes 2, 10)	(Notes 2, 10)
	 Case 59 (DO-41)	 Metal Case 52 (DO-13	 Glass Case 59 (DO-41)	 Metal Case 55	 Surmetic 40 Case 17	 Metal Case 56 (DO-4)	 Metal Case 54 (TO-3)	 Metal Case 58 (DO-5)
3.3	1N4728	1N3821	1N5913		1N5333			
3.6	1N4729	1N3822	1N5914		1N5334			
3.9	1N4730	1N3823	1N5915		1N5335	1N3993&R	1N4557&R	1N4549&R
4.3	1N4731	1N3824	1N5916		1N5336	1N3994&R	1N4558&R	1N4550&R
4.7	1N4732	1N3825	1N5917		1N5337	1N3995&R	1N4559&R	1N4551&R
5.1	1N4733	1N3826	1N5918		1N5338	1N3996&R	1N4560&R	1N4552&R
5.6	1N4734	1N3827	1N5919		1N5339	1N3997&R	1N4561&R	1N4553&R
6.2	1N4735	1N3828	1N5920		1N5341	1N3998&R	1N4562&R	1N4554&R
6.8	1N4736	1N3829 1N3016	1N5921	1N3785	1N5342	1N3999&R 1N2970&R	1N4563&R 1N2804&R	1N4555&R 1N3305&R
7.5	1N4737	1N3830 1N3017	1N5922	1N3786	1N5343	1N4000&R 1N2971&R	1N4564&R 1N2805&R	1N4556&R 1N3306&R
8.2	1N4738	1N3018	1N5923	1N3787	1N5344	1N2972&R	1N2806&R	1N3307&R
8.7					1N5345			
9.1	1N4739	1N3019	1N5924	1N3788	1N5346	1N2973&R	1N2807&R	1N3308&R
10	1N4740	1N3020	1N5925	1N3789	1N5347	1N2974&R	1N2808&R	1N3309&R
11	1N4741	1N3021	1N5926	1N3790	1N5348	1N2975&R	1N2809&R	1N3310&R
12	1N4742	1N3022	1N5927	1N3791	1N5349	1N2976&R	1N2810&R	1N3311&R
13	1N4743	1N3023	1N5928	1N3792	1N5350	1N2977&R	1N2811&R	1N3312&R
14					1N5351	1N2978&R	1N2812&R	1N3313&R
15	1N4744	1N3024	1N5929	1N3793	1N5352	1N2979&R	1N2813&R	1N3314&R
16	1N4745	1N3025	1N5930	1N3794	1N5353	1N2980&R	1N2814&R	1N3315&R
17					1N5354		1N2815&R	1N3316&R
18	1N4746	1N3026	1N5931	1N3795	1N5355	1N2982&R	1N2816&R	1N3317&R
19					1N5356	1N2983&R	1N2817&R	1N3318&R
20	1N4747	1N3027	1N5932	1N3796	1N5357	1N2984&R	1N2818&R	1N3319&R
22	1N4748	1N3028	1N5933	1N3797	1N5358	1N2985&R	1N2819&R	1N3320&R
24	1N4749	1N3029	1N5934	1N3798	1N5359	1N2986&R	1N2820&R	1N3321&R
25					1N5360		1N2821&R	1N3322&R
27	1N4750	1N3030	1N5935	1N3799	1N5361	1N2988&R	1N2822&R	1N3323&R
28					1N5362			
30	1N4751	1N3031	1N5936	1N3800	1N5363	1N2989&R	1N2823&R	1N3324&R
33	1N4752	1N3032	1N5937	1N3801	1N5364	1N2990&R	1N2824&R	1N3325&R
36	1N4753	1N3033	1N5938	1N3802	1N5365	1N2991&R	1N2825&R	1N3326&R
39	1N4754	1N3034	1N5939	1N3803	1N5366	1N2992&R	1N2826&R	1N3327&R
43	1N4755	1N3035	1N5940	1N3804	1N5367	1N2993&R	1N2827&R	1N3328&R
47	1N4756	1N3036	1N5941	1N3805	1N5368	1N2996&R	1N2829&R	1N3330&R
51	1N4757	1N3037	1N5942	1N3806	1N5369	1N2997&R	1N2831&R	1N3332&R
56	1N4758	1N3038	1N5943	1N3807	1N5370	1N2998&R	1N2832&R	1N3334&R
60					1N5371			
62	1N4759	1N3039	1N5944	1N3808	1N5372	1N3000&R	1N2833&R	1N3335&R
68	1N4760	1N3040	1N5945	1N3809	1N5373	1N3001&R	1N2834&R	1N3336&R
75	1N4761	1N3041	1N5946	1N3810	1N5374	1N3002&R	1N2835&R	1N3337&R
82	1N4762	1N3042	1N5947	1N3811	1N5375	1N3003&R	1N2836&R	1N3338&R
87					1N5376			
91	1N4763	1N3043	1N5948	1N3812	1N5377	1N3004&R	1N2837&R	1N3339&R
100	1N4764	1N3044	1N5949	1N3813	1N5378	1N3005&R	1N2838&R	1N3340&R
110	1M110ZS10	1N3045	1N5950	1N3814	1N5379	1N3007&R	1N2840&R	1N3342&R
120	1M120ZS10	1N3046	1N5951	1N3815	1N5380	1N3008&R	1N2841&R	1N3343&R
130	1M130ZS10	1N3047	1N5952	1N3816	1N5381	1N3009&R	1N2842&R	1N3344&R
150	1M150ZS10	1N3048	1N5953	1N3817	1N5383	1N3011&R	1N2843&R	1N3346&R
160	1M160ZS10	1N3049	1N5954	1N3818	1N5384	1N3012&R	1N2844&R	1N3347&R
170	1M170ZS10				1N5385			
180	1M180ZS10	1N3050	1N5955	1N3819	1N5386	1N3014&R	1N2845&R	1N3349&R
200	1M200ZS10	1N3051	1N5956	1N3820	1N5388	1N3015&R	1N2846&R	1N3350&R

R, RA, and RB = Reverse Polarity Types Available.
JAN/JANTX(V) available, ±5% only.

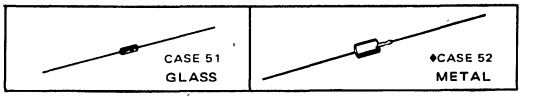
NOTES—Tolerances (continued)

7. No suffix = ±10%
   A suffix = ±5%
8. 1N3821 series: No suffix = ±10%
   A suffix = ±5%
   1N3016 series: No suffix = ±20%
   A suffix = ±10%
   B suffix = ±5%
9. No suffix = ±20%
   A suffix = ±10%
   B suffix = ±5%
   C suffix = ±2%
   D suffix = ±1%
10. No suffix = ±20%
    A suffix = ±10%
    B suffix = ±5%
11. No suffix = ±20% with guaranteed limits on V_Z, V_F, I_R, and i_R only
    A suffix = ±10%
    B suffix = ±5%

Zener Reference Devices

For applications where output voltage must remain within narrow limits during changes in input voltage, load resistance and temperature. Motorola guarantees all Reference Devices to fall within the specified maximum voltage variations, ΔV_Z, at the specifically indicated test temperatures and test current (JEDEC Standard #5). Temperature Coefficient is also specified but should be considered as a reference only — not a maximum rating.

Devices in this table are hermetically sealed structures. Includes JAN, JANTX and radiation hardened device types. These temperature compensated Zener Reference Diodes have low dynamic impedance and silicon-oxide-passivated junctions for long-term stability.



All devices Case 51 (DO-7) except as noted ♦

V_Z Volts	Test Current mAdc	Test Temp Points	AVERAGE TEMPERATURE COEFFICIENT OVER THE OPERATING RANGE									
			0.01 %/°C		0.005 %/°C		0.002 %/°C		0.001 %/°C		0.0005 %/°C	
			Device Type	ΔV_Z Max Volts	Device Type	ΔV_Z Max Volts	Device Type	ΔV_Z Max Volts	Device Type	ΔV_Z Max Volts	Device Type	ΔV_Z Max Volts
6.2⚠	7.5	A	1N821,	0.096	1N823,	0 048	1N825,	0.019	1N827,	0.009	1N829,	0.005
6.2⚠	7.5	A	1N821A	0.096	1N823A	0 048	1N825A	0.019	1N827A	0.009	1N829A	0.005
6.4	0.5	B	1N4565	0.018	1N4566	0.024	1N4567	0.010	1N4568	0.005	1N4569	0.002
	0.5	A	1N4565A	0.099	1N4566A	0.050	1N4567A	0.020	1N4568A	0.010	1N4569A	0.005
	1.0	B	1N4570	0.048	1N4571	0.024	1N4572	0.010	1N4573	0.005	1N4574	0.002
	1.0	A	1N4570A	0.099	1N4571A	0.050	1N4572A	0.020	1N4573A	0.010	1N4574A	0.005
	2.0	B	1N4575	0.048	1N4576	0.024	1N4577	0.010	1N4578	0.005	1N4579	0.002
	2.0	A	1N4575A	0.099	1N4576A	0.025	1N4577A	0.020	1N4578A	0.010	1N4579A	0.005
	4.0	B	1N4580	0.048	1N4581	0.024	1N4582	0.010	1N4583	0 005	1N4584	0.002
	4.0	A	1N4580A	0.099	1N4581A	0.050	1N4582A	0.020	1N4583A	0.010	1N4584A	0.005
8.4	10	A	1N3154,	0.130	1N3155,	0.065	1N3156,	0.026	1N3157,	0.013		
	10	C	1N3154A	0.072	1N3155A	0.085	1N3156A	0.034	1N3157A	0.017		
8.5	0.5	B	1N4775	0.064	1N4776	0.032	1N4777	0.013	1N4778	0.006	1N4779	0.003
	0.5	A	1N4775A	0.132	1N4776A	0.066	1N4777A	0.026	1N4778A	0 013	1N4779A	0.007
	1.0	B	1N4780	0.064	1N4781	0.032	1N4782	0.013	1N4783	0.006	1N4784	0.003
	1.0	A	1N4780A	0.132	1N4781A	0.066	1N4782A	0.026	1N4783A	0.013	1N4784A	0.007
9.0	7.5	B	1N935	0.067	1N936	0.033	1N937	0.013	1N938	0.006	1N939	0.003
	7.5	A	1N935A	0.139	1N936A	0.069	1N937A	0.027	1N938A	0.013	1N939A	0.007
	7.5	C	1N935B,	0.184	1N936B	0.092	1N937B,	0.037	1N938B,	0.018	1N939B,	0.009
9.4 ±0.4 (Suffix "A" +0.2 V)	10	D			♦1N2163,A	0.033			♦1N2166,A	0.007	♦1N2169,A	0.004
		E			♦1N2164,A	0.086			♦1N2167,A	0.017	♦1N2170,A	0.009
		F			♦1N2165,A	0.110			♦1N2168,A	0.023	♦1N2171,A	0.012
11.7	7.5	B	1N941	0.088	1N942	0.044	1N943	0.018	1N944	0.009	1N945	0.004
	7.5	A	1N941A	0.081	1N942A	0.090	1N943A	0.036	1N944A	0.018	1N945A	0.009
	7.5	C	1N941,B,	0.239	1N942B	0.120	1N943B,	0.047	1N944B	0.024	1N945B,	0.012

Test Temperature Points	
A	-55, 0, +25, +75, +100
B	0, +25, +75
C	-55, 0, +25, +75, +100, +150
D	0, +25, +70
E	-55, 0, +25, +75, +125
F	-55, 0, +75, +125, +185
G	+25, +75, +100

⚠ Non-suffix – Z_{ZT} = 15, "A" Suffix – Z_{ZT} = 10

JAN/JANTX(V) available, ±5% only

9

Precision Reference Diodes

Designed, manufactured and tested for ultra-high stability of voltage with time and temperature change. Use of special measurement equipment and voltage standards provide calibration directly traceable to the National Bureau of Standards.

CASE 51

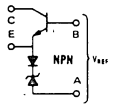
Reference Voltage Volts	Test Current mA	Temperature Stability ΔV_Z (mV)	Temperature Stability OP Temp Range °C	CERTIFIED VOLTAGE TIME STABILITY OVER 1000 HOURS OF OPERATION (Parts/Million Change) <5 PPM/1000 HR Device Type	<5 PPM/1000 HR Change µV Max	<10 PPM/1000 HR Device Type	<10 PPM/1000 HR Change µV Max	<20 PPM/1000 HR Device Type	<20 PPM/1000 HR Change µV Max	<40 PPM/1000 HR Device Type	<40 PPM/1000 HR Change µV Max
6.2 ± 5%	7.5	2.5	25,75,100	MZ605	30	MZ610	60	MZ620	120	MZ640	240

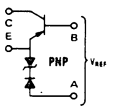
Amplifying Regulator Diodes

Designed for use in regulated power supplies as a combination voltage reference element and error voltage amplifier, providing temperature compensation for excellent reference voltage stability. Available with either PNP or NPN transistors by adding either P or N suffix to part number.

ELECTRICAL CHARACTERISTICS (I_{ZT} = 5.0 mA, V_{CEO} = 30 V)

CASE 212-01

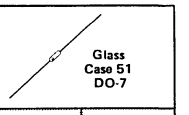




V_{REF} Volts	Tolerance ±%	Test Temperature °C	ΔV_{REF} Volts	Device Type
6.8	10	0, +25, +75	0.051	MCA1911
			0.025	MCA1912
			0.010	MCA1913
			0.005	MCA1914
6.8	5.0	-55, 0, +25, -55, +100	0.105	MCA1921
			0.052	MCA1922
			0.020	MCA1923
			0.010	MCA1924
6.8	5.0	-55, 0, +25 +75,+100,+150	0.139	MCA1931
			0.069	MCA1932
			0.026	MCA1933
			0.013	MCA1934
8.6	10	0, +25, +75	0.060	MCA2011
			0.030	MCA2012
			0.012	MCA2014
			0.006	MCA2014
8.6	5.0	-55, 0, +25 +75, +100	0.124	MCA2021
			0.062	MCA2022
			0.024	MCA2023
			0.012	MCA2024
8.6	5.0	-55, 0, +25 +75,+100,+150	0.164	MCA2031
			0.082	MCA2032
			0.032	MCA2033
			0.016	MCA2034
9.5	10	0, +25, +75	0.071	MCA2111
			0.035	MCA2112
			0.014	MCA2113
			0.007	MCA2114
9.5	5.0	-55, 0, +25 -75, +100	0.147	MCA2121
			0.073	MCA2122
			0.028	MCA2123
			0.014	MCA2124
9.5	5.0	-55, 0, +25 +75,-100,+150	0.194	MCA2131
			0.097	MCA2132
			0.038	MCA2133
			0.019	MCA2134
11	10	0, +25, +75	0.082	MCA2211
			0.041	MCA2212
			0.016	MCA2213
			0.008	MCA2214
11	5.0	-55, 0, +25 +75, +100	0.170	MCA2221
			0.085	MCA2222
			0.034	MCA2223
			0.017	MCA2224
11	5.0	-55, 0, +25 +75,+100,+150	0.225	MCA2231
			0.112	MCA2232
			0.044	MCA2233
			0.022	MCA2234

Field-Effect Current Regulator Diodes

High impedance diodes whose "constant current source" characteristic complements the "constant voltage" of the zener line. Currents are available from 0.22 to 4.7 mA, with usable voltage range from a minimum limit of 1.0 to 2.5 V, up to a voltage compliance of 100 V, for the 1N5283 series, or 70 V, for the MCL1300 series.



Glass Case 51 DO-7

Reg. Current I_P @V_T = 25 V mA Nom	Device Type	Knee Imp Z_K @V_K = 6.0 V MΩ Max	Limiting Voltage @I_L = 0.8 I_P Volts Max
0.22	1N5283	2.75	1.00
0.24	1N5284	2.35	1.00
0.27	1N5285	1.95	1.00
0.30	1N5286	1.60	1.00
0.33	1N5287	1.35	1.00
0.39	1N5288	1.00	1.05
0.43	1N5289	0.870	1.05
0.47	1N5290	0.750	1.05
0.56	1N5291	0.560	1.10
0.62	1N5292	0.470	1.13
0.68	1N5293	0.400	1.15
0.75	1N5294	0.335	1.20
0.82	1N5295	0.290	1.25
0.91	1N5296	0.240	1.29
1.00	1N5297	0.205	1.35
1.10	1N5298	0.180	1.40
1.20	1N5299	0.155	1.45
1.30	1N5300	0.135	1.50
1.40	1N5301	0.115	1.55
1.50	1N5302	0.105	1.60
1.60	1N5303	0.092	1.65
1.80	1N5304	0.074	1.75
2.00	1N5305	0.061	1.85
2.20	1N5306	0.052	1.95
2.40	1N5307	0.044	2.00
2.70	1N5308	0.035	2.15
3.00	1N5309	0.029	2.25
3.30	1N5310	0.024	3.35
3.60	1N5311	0.020	2.50
3.90	1N5312	0.017	2.60
4.30	1N5313	0.014	2.75
4.70	1N5314	0.012	2.90
0.5±0.3	MCL1300	0.500	1.00
1.0±0.6	MCL1301	0.200	1.50
2.0±0.6	MCL1302	0.100	2.00
3.0±0.6	MCL1303	0.050	2.00
4.0±0.6	MCL1304	0.025	2.50

▱ JAN/JANTX (V) availability

9

Low Voltage Regulators

High-conductance silicon diodes designed as stable forward-reference sources for transistor amplifier biasing and similar applications. Available in high reliability glass construction or economic plastic packaging.

CASE 51
(DO-7)

CASE 59

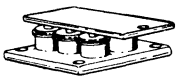
ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted).

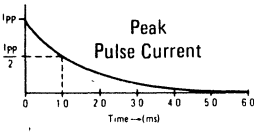
Forward Reference Voltage		Test Current	Leakage Current		Device Type	Case
Min	Max	I_F mA	I_R @ V_R µA Volts			
0.63	0.71	10	10	5.0	MZ2360	59 Surmetic
1.24	1.38	10	10	5.0	MZ2361	51 Surmetic
1.90	2.10	10	10	5.0	MZ2362	51
0.58	0.70	1.0	0.1	4.0	.4M.64FR10	Glass
1.29	1.43	10	↓	↓	.4M1.36FR5	↓
1.33	1.39	10			.4M1.36FR2	
1.94	2.14	10			.4M2.04FR5	
2.00	2.08	10			.4M2.04FR2	
0.58	0.70	1.0			1N816	

Transient Suppressors

Transient suppressors designed for applications requiring protection of voltage sensitive electronic devices in danger of destruction by high energy voltage transients. Select from standard factory available types or design the suppressor to meet specific needs by paralleling cells. For specific options, i.e., non-standard voltages, higher power capacity, and package configurations, consult factory.



CASE 119



V_R Operating Voltage		I_R Reverse Current	ΔV_Z Breakdown Voltage		V_C Clamping Voltage		V_F Forward Voltage		Device Type	Case
Nom Vdc	V(RMS)	µA	Min Volts	@ I_{ZT} mA	Max Volts	@ I_{pp} Amp	Volts	@ I_F Amp		
14	10	50	16	0.4	24	200	1.5	10	MPZ5-16A	119
14	10	↓	16	0.4	20	200	↓	↓	MPZ5-16B	↓
28	20		32	0.2	50	100			MPZ5-32A	
28	20		32	0.2	45	100			MPZ5-32B	
28	20		32	0.2	40	100			MPZ5-32C	
165	117		180	0.03	250	20			MPZ5-180A	
165	117		180	0.03	225	20			MPZ5-180B	
165	117		180	0.03	205	20			MPZ5-180C	

9

Supplementary Literature

10

SUPPLEMENTAL LITERATURE

The following documents may provide additional information for your circuit designs. Copies may be obtained from Motorola Semiconductor Products Inc., Literature Distribution Center, P.O. Box 20924, Phoenix, AZ 85036.

POWER SUPPLY CIRCUIT DESIGN

AN-719 A New Approach to Switching Regulators

This article describes a 24-Volt, 3-Ampere switching mode supply. It operates at 20 kHz from a 120 Vac line with an overall efficiency of 70%. New techniques are used to shape the load line. The control portion uses a quad comparator and an opto coupler and features short circuit protection.

AN-725 A Low-Cost 80 V-1.5 A Color TV Power Supply

A full-wave SCR power supply is proposed for application in line operated color television receivers. Economy of design is maintained while providing good regulation against line, load and temperature changes.

AN-737A Switched Mode Power Supplies—Highlighting a 5-V, 40-A Inverter Design

This application note identifies the features of various regulator circuits that are in use today in AC to DC power supplies. The note also illustrates how these circuits may be used as complementary building blocks in a system design. Primary emphasis is on switched mode regulators beause they fill the present need for energy and space savings.

A complete 5-V, 40-A line operated inverter supply is described in detail including design procedures for the magnetic components. The inverter itself is a "state-of-the-art" design which features CMOS logic, high voltage power transistors, Schottky rectifiers and an opto-electronic coupler. It operates with a full load efficiency of 80% at a frequency of 20kHz.

AN-752 An 80-Watt Switching Regulator for CATV and Industrial Applications

This application note describes a 24-Volt, 3-Ampere switching, regulated power supply that operates above 18 kHz from a 40-to 60-Volt, 60-Hz square wave source (CATV power line from a ferroresonant fransformer) or a dc standby source with input output isolation. The control circuit consists of a dual operational amplifier and a linear integrated circuit timer which are used to vary the on time of a new high-speed power transistor. The circuit provides good efficiency, good regulation, low output ripple and incorporates input and output voltage over shutdown protection.

AN-767 A Line Operated, Regulated 5V/50A Switching Power Supply

This application note describes a regulated 220V ac to 5 Vdc converter using high voltage switching transistors and Schottky barrier rectifiers. The control functions are all performed by integrated circuits.

AN-786 Power Darlington Load Line Considerations

Power Darlington load lines are discussed in the light of a typical application of a Switchmode Darlington power transistor. Darlington advantages are reviewed and the test circuit is introduced. Load line analysis revealed a reverse bias SOA problem and just enough snubbing was used to insure reliability without unduly sacrificing efficiency.

EB-52 Control Your Switching Regulator With The MC3380 Astable Multivibrator

Engineering Bulletin EB-52 describes the operation and characteristics of the MC3380 astable multivibrator and details the design of a 200 volt switching regulator circuit for gas discharge displays using this device as the control element.

EB-66 A Symmetry Correcting Circuit for Use with the MC3420

EB-66 shows a method of implementing an external symmetry-correction circuit with the MC3420 Switchmode Regulator Control IC to insure balanced operation of the power transformer in push-pull inverter configurations.

MC3420/3520 Switchmode Regulator Control Circuit

The MC3520/3420 is an inverter control unit which provides all the control circuitry for PWM push-pull, bridge and series type Switchmode power supplies.

TL494/495 Switchmode Pulse Width Modulation Control Circuits

The TL494 and TL495 combine the best features of existing PWM control circuits and add other on-chip functions. These devices provide, on a single monolithic chip, all the control circuitry for PWM push-pull, bridge and series type switchmode power supplies.

AN-240 SCR Power Control Fundamentals

Relationships of control angle to peak voltage, average voltage, RMS voltage and power are presented in chart form. Time constants for relaxation oscillators are discussed for both DC and AC supplies. These basic form the heart of SCR control.

AN-483B 20 and 30 Watt Power Amplifiers Using Darlington Output Transistors

Use of monolithic power Darlington output transistors can greatly simplify the design of highfidelity amplifiers. Described herein is a 20-Watt amplifier which uses only three transistors, and a 30-Watt amplifier which uses four.

AN-484A Medium-Power Audio Amplifiers

This note describes a basic circuit design approach for audio complementary power amplifiers. Procedures are detailed for the selection of input, driver and output transistors. Both simple and Darlington transistor systems are included. Biasing, thermal considerations, overload protection and power supply information is given extensive treatment.

Design examples, including all circuit values, performance data and and suggested P.C. board layouts, are given for simple tranasistor amplfiers at the 3, 5, 7, 10, 15, 20, 25, and 35 Watt levels. Also included are three amplfiers using Darlington output transistors at the 15, 20, and 25 Watt levels.

AN-485 High-Power Audio Amplifiers with Short-Circuit Protection

This application note describes a recommended circuit approach for high-performance audio amplifiers in the 35-Watt to 100-Watt RMS power range. Circuitry is included which enables the amplifier to operate safely continuously under any load condition including a short.

AN-705 Pulse Width Modulation for Small DC Motor Control

This application note explains the use of modern pulse width modulation techniques as an efficient and economical solution to small DC motor control. Several practical circuit design approaches using discrete, operational amplifier and integrated circuit devices are described and illustrated.

AN-712A Interface Techniques Between Industrial Logic and Power Devices

This application note presents worst case design approaches to illustrate the methods of interfacing McMOS and MHTL logic to various power load levels, both ac and dc. Interface devices vary from small-signal transistors to power transistors and thyristors, using direct coupling/level translation and optoelectronic coupling techniques.

AN-755 Solid-State Relays for AC Power Control

Solid-State Relays (SSRs) using both SCRs and Triacs are examined in detail. The advantages and disadvantages of SSRs compared with electromechanical relays are discussed. Inductive loads are reviewed and snubbing suggestions made. Parts lists are given for SSRs for voltages of 120 and 240 V rms and currents from 5 to 113 A rms. Also described are circuits to give ac and CMOS compatibility.

AN-766 A Variable Frequency Control for 3Ø Induction Motors

This application note describes a variable variable voltage drive system for three-phase induction motor controls. A survey of possible system configurations and a detailed description of a semi-converter/transistor inverter quasi-square wave drive system are included.

POWER TRANSISTORS

AN-569 Transient Thermal Resistance — General Data and Its Use

Data illustrating the thermal response of a number of semiconductor die and package combinations are given. Its use, employing the concepts of transient thermal resistance and superposition, permit the circuit designer to predict semiconductor junction temperature at any point in time during application of a complex power pulse train.

AN-778 Mounting Techniques for Power Semiconductors

For reliable operation, semiconductors must be properly mounted. Discussed are aspects of preparing the mounting surface, using thermal compounds, insulation techniques, fastening techniques, handling of leads and pins, and evaluation methods for the thermal system.

AN-785 Reverse Bias Safe Operating Area

The rating of high voltage, high speed switching transistors for safe turn-off operations is examined. Clamped inductive turn-off measurements are used to generate a switching RBSOA—reverse bias safe operating area—which can be used in conjunction with load line analysis to assure proper transistor operation. The effects of inductance, temperature, base turn-off conditions and forward base drive on RBSOA are included in the discussion.

EN-101 Verifying Collector Voltage Ratings

Methods of verifying the various voltage ratings given on transistor data sheets are described. Practical test circuits are given and testing problems are discussed. A detailed discussion of the avalanche breakdown mechanism and the significance of various voltage ratings is also included.

THYRISTORS

AN-466 Circuit Applications for the Triac

This note discusses the basic theory of operation of the triac with control methods and circuit applications. Among the applications included are basic switches, lamp dimmers, motor controls, a heater control, a flasher, a regulator, protective circuits and zero-point switching.

AN-568 A Fuse-Thyristor Coordination Primer

This report treats the considerations required for the use of fuses in protecting thyristors against short circuit fault currents. Basics of the mating philosophy are discussed and practical examples of coordination are given. Symbols, terms and their definitions are included.

ZENER DIODES

AN-784 Transient Power Capability of Zener Diodes

Because of the sensitivity of semiconductor components to voltage transients in excess of their ratings, circuits are often designed to inhibit voltage surges in order to protect equipment from catastrophic failure. This note discusses the power capability of zener diodes for transient suppression.

MOTOROLA *Semiconductor Products Inc.*

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