MOTOROLA

DL156/D
REV 1

Fast Static RAM

BiCMOS, CMOS, and Module Data

DATA CLASSIFICATION

Product Preview

This heading on a data sheet indicates that the device is in the formative stages or in design (under development). The disclaimer at the bottom of the first page reads: "This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice."

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MOTOROLA

Fast Static RAM

BiCMOS, CMOS, and Module Data

Motorola offers a broad range of fast SRAMs for virtually any digital data processing system application. This data book contains complete specifications for individual FSRAM circuits in data sheet form, as well as an explanation of Motorola's reliability and quality program and an applications section.

For information on Dynamic RAM devices, please refer to DL155/D. For information on Military Memory devices, please refer to DL144/D.

New Motorola memories are being introduced continually. For the latest releases, additional technical information, and pricing, please contact your nearest authorized Motorola distributor or Motorola Sales Office. A complete listing of distributors and sales offices is included at the back of this book.

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Selector Guide and Cross Reference

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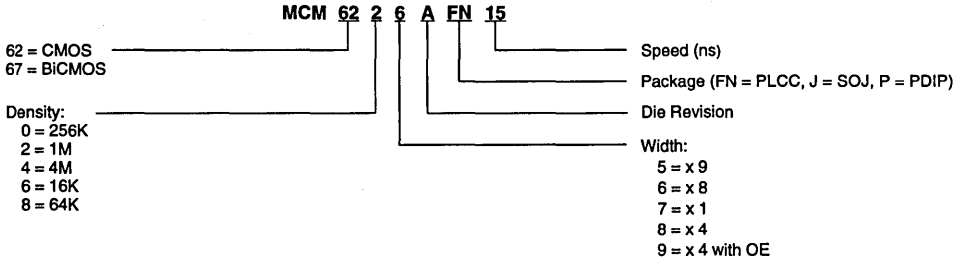
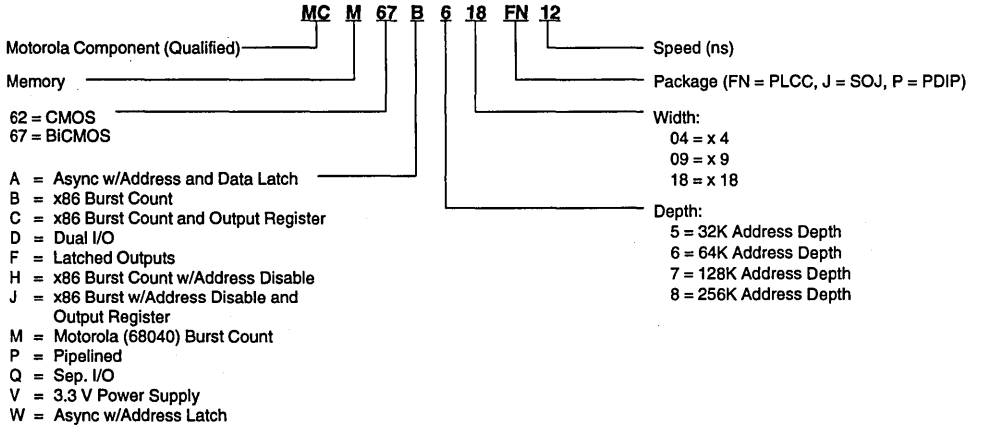
DEVICE/PART NUMBER DESIGNATORS





NOTE: There are some exceptions to these device numbering schemes, i.e., MCM62990A is a CMOS 16K x 16 and NOT a 512K x 90 device.

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
8M	256K x 36	12	—	**Motorola**	MCM44256	80		SIMM				◊	◊
		15	—	**Motorola**	MCM44256	80		SIMM				◊	◊
		17	—	**Motorola**	MCM44256	80		SIMM				◊	◊
	256K x 32	20	—	**Motorola**	MCM32257	64		ZIP				◊	
		20	—	AT&T	ATTM32257								
		20	—	Micron	MT8S25632								
		20	—	IDT	IDT7MP4045								
		25	—	**Motorola**	MCM32257	64		ZIP				◊	
		25	—	AT&T	ATTM32257								
		25	—	Micron	MT8S25632								
		25	—	IDT	IDT7MP4045								
		35	—	**Motorola**	MCM32257	64		ZIP				◊	
		35	—	AT&T	ATTM32257								
		35	—	Micron	MT8S25632								
4M	64K x 72	—	15	**Motorola**	MCM72BA64	136		SIMM		◊		◊	◊
		—	16.6	**Motorola**	MCM72BA64	136		SIMM		◊		◊	◊
	128K x 32	—	20	**Motorola**	MCM32AB128	112		SIMM			◊	◊	◊
		—	30	**Motorola**	MCM32AB128	112		SIMM			◊	◊	◊
		20	—	**Motorola**	MCM32128	64		ZIP, SIMM				◊	
		20	—	AT&T	ATTM32128								
		20	—	Micron	MT4S12832								
		25	—	**Motorola**	MCM32128	64		ZIP, SIMM				◊	
		25	—	AT&T	ATTM32128								
		25	—	Micron	MT4S12832								
		35	—	**Motorola**	MCM32128	64		ZIP, SIMM				◊	
		35	—	AT&T	ATTM32128								
		35	—	Micron	MT4S12832								
	512K x 8	25	—	**Motorola**	MCM6246	36	400	SOJ	◊				
		25	—	Micron	MT5C512K8A1	32	400	SOJ					
		25	—	Micron	MT5C512K8B2	36	400	SOJ, TSOP	◊				
		25	—	Micron	MT5LC512K8C3	32	400	SOJ					
		25	—	Micron	MT5LC512K8D4	36	400	SOJ, TSOP	◊				
		25	—	NEC	µPD434008	32/36	400	SOJ	◊				
		30	—	**Motorola**	MCM6246	36	400	SOJ	◊				
		30	—	Micron	MT5C512K8A1	32	400	SOJ					

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		30	—	Micron	MT5C512K8B2	36	400	SOJ, TSOP	◊				
		30	—	Micron	MT5LC512K8C3	32	400	SOJ					
		30	—	Micron	MT5LC512K8D4	36	400	SOJ, TSOP	◊				
		35	—	**Motorola**	MCM6246	36	400	SOJ	◊				
		35	—	Micron	MT5C512K8A1	32	400	SOJ					
		35	—	Micron	MT5C512K8B2	36	400	SOJ, TSOP	◊				
		35	—	Micron	MT5LC512K8C3	32	400	SOJ					
		35	—	Micron	MT5LC512K8D4	36	400	SOJ, TSOP	◊				
	2M x 2	10	—	**Motorola**	MCM101524	36	400	SOJ, SOP	◊				ECL
		12	—	**Motorola**	MCM101524	36	400	SOJ, SOP	◊				ECL
		15	—	Fujitsu	MBM100C524	32/36	*	SOJ, TSOP	◊				
		15	—	Fujitsu	MBM101C524	32/36	*	SOJ, TSOP	◊				
		15	—	Fujitsu	MBM10C524	32/36	*	SOJ, TSOP	◊				
		15	—	**Motorola**	MCM101524	36	400	SOJ, SOP	◊				ECL
	1M x 4	20	—	**Motorola**	MCM6249	32	400	SOJ	◊				
		20	—	Micron	MT5C1M4A1	32	400	SOJ					
		20	—	Micron	MT5C1M4B2	32	400	SOJ, TSOP	◊				
		20	—	Micron	MT5LC1M4C3	32	400	SOJ					
		20	—	Micron	MT5LC1M4D4	32	400	SOJ, TSOP	◊				
		20	—	NEC	µPD434004	32/36	400	SOJ	◊				
		25	—	Hitachi	HM624100	32	400	SOJ, TSOP II	◊				
		25	—	Fujitsu	MB82B206	36	400	SOJ	◊				
		25	—	**Motorola**	MCM6249	32	400	SOJ	◊				
		25	—	Micron	MT5C1M4A1	32	400	SOJ					
		25	—	Micron	MT5C1M4B2	32	400	SOJ, TSOP	◊				
		25	—	Micron	MT5LC1M4C3	32	400	SOJ					
		25	—	Micron	MT5LC1M4D4	32	400	SOJ, TSOP	◊				
		25	—	NEC	µPD434004	32/36	400	SOJ	◊				
		30	—	**Motorola**	MCM6249	32	400	SOJ	◊				
		30	—	Hitachi	HM624100	32	400	SOJ, TSOP II	◊				
		35	—	**Motorola**	MCM6249	32	400	SOJ	◊				
		35	—	Hitachi	HM624100	32	400		◊				
		35	—	Fujitsu	MB82B206	36	400	SOJ	◊				
		35	—	Micron	MT5C1M4A1	32	400	SOJ					
		35	—	Micron	MT5C1M4B2	32	400	SOJ, TSOP	◊				

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		35	—	Micron	MT5LC1M4C3	32	400	SOJ					
		35	—	Micron	MT5LC1M4D4	32	400	SOJ, TSOP	◊				
	4M x 1	10	—	**Motorola**	MCM101520	36	400	SOJ, SOP, TAB	◊				ECL
		12	—	**Motorola**	MCM101520	36	400	SOJ, SOP, TAB	◊				ECL
		15	—	**Motorola**	MCM101520	36	400	SOJ, SOP, TAB	◊				ECL
		15	—	Fujitsu	MBM100C520	32/36		SOJ, TSOP	◊				
		15	—	Fujitsu	MBM101C520	32/36		SOJ, TSOP	◊				
		15	—	Fujitsu	MBM10C520	32/36		SOJ, TSOP	◊				
2M	32K x 72	—	15	**Motorola**	MCM72BA32			SIMM		◊		◊	◊
		—	16.6	**Motorola**	MCM72BA32			SIMM		◊		◊	◊
	64K x 44	12	—	**Motorola**	MCM4464	80		SIMM				◊	
		15	—	**Motorola**	MCM4464	80		SIMM				◊	
		17	—	**Motorola**	MCM4464	80		SIMM				◊	
		17-5	—	**Motorola**	MCM4464SG	80		SIMM				◊	
2M	64K x 32	—	20	**Motorola**	MCM32AB64	112		SIMM			◊	◊	◊
		—	30	**Motorola**	MCM32AB64	112		SIMM			◊	◊	◊
		15	—	**Motorola**	MCM3264A	64		ZIP				◊	
		15	—	Micron	MT8S6432Z								
		15	—	IDT	IDT7MP4036B								
		20	—	**Motorola**	MCM3264A	64		ZIP				◊	
		20	—	AT&T	ATTM3264								
		20	—	Micron	MT8S6432Z								
		20	—	IDT	IDT7MP4036B								
		15	—	**Motorola**	MCM32A64	128		SIMM				◊	
		20	—	**Motorola**	MCM32A64	128		SIMM				◊	
1M	32K x 32	—	20	**Motorola**	MCM32AB32	112		SIMM			◊	◊	◊
		—	30	**Motorola**	MCM32AB32	112		SIMM			◊	◊	◊
	64K x 18	12	—	**Motorola**	MCM67A618	52		PLCC			◊	◊	
		15	—	**Motorola**	MCM67A618	52		PLCC			◊	◊	
		20	—	**Motorola**	MCM67A618	52		PLCC			◊	◊	
		9	15	**Motorola**	MCM67B618	52		PLCC		◊		◊	◊
		10	12.5	Cypress	CY7C1031								
		9	15	IC Works	ICW73B596								
		12	20	**Motorola**	MCM67B618	52		PLCC		◊		◊	◊
		12	15	Cypress	CY7C1031								

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		12	20	IC Works	ICW73B596								
		18	25	**Motorola**	MCM67B618	52		PLCC		◊		◊	◊
		14	20	Cypress	CY7C1031								
		7	12.5	**Motorola**	MCM67C618	52		PLCC		◊		◊	◊
		9	15	**Motorola**	MCM67C618	52		PLCC		◊		◊	◊
		9	15	**Motorola**	MCM67H618	52		PLCC		◊		◊	◊
		12	20	**Motorola**	MCM67H618	52		PLCC		◊		◊	◊
		18	25	**Motorola**	MCM67H618	52		PLCC		◊		◊	◊
		7	12.5	**Motorola**	MCM67J618	52		PLCC		◊		◊	◊
		9	15	**Motorola**	MCM67J618	52		PLCC		◊		◊	◊
		9	12.5	**Motorola**	MCM67M618	52		PLCC		◊		◊	◊
		11	15	**Motorola**	MCM67M618	52		PLCC		◊		◊	◊
		10	15	Cypress	CY7C1032								
		14	20	**Motorola**	MCM67M618	52		PLCC		◊		◊	◊
		19	25	**Motorola**	MCM67M618	52		PLCC		◊		◊	◊
		12	—	**Motorola**	MCM67W618	52		PLCC			◊		
		15	—	**Motorola**	MCM67W618	52		PLCC			◊		
		20	—	**Motorola**	MCM67W618	52		PLCC			◊		
		20	—	Sharp	LH521028	52							
	128K x 8	20	—	**Motorola**	MCM6226A	32	400	SOJ				◊	
		20	—	AT&T	ATT7C109J								
		20	—	IDT	IDT711024S								
		20	—	Micron	MT5C1008DJ								
		20	—	NEC	µPD431008								
		20	—	Sharp	LH521007K								
		20	—	Sony	CXK581120J								
		20	—	Samsung	KM681001								
		25	—	**Motorola**	MCM6226A	32	400	SOJ				◊	
		25	—	AT&T	ATT7C109J								
		25	—	Cypress	CY7C109								
		25	—	IDT	IDT711024S								
		25	—	Micron	MT5C1008DJ								
		25	—	Samsung	KM681001								
		25	—	Sharp	LH521007K								
		35	—	**Motorola**	MCM6226A	32	400	SOJ				◊	

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		35	—	Cypress	CY7C109								
		35	—	Micron	MT5C1008DJ								
		35	—	Samsung	KM681001								
		35	—	Sharp	LH521007K								
		35	—	Sony	CXK581020SJ								
		45	—	**Motorola**	MCM6226A	32	400	SOJ				◊	
		45	—	Cypress	CY7C109								
		45	—	Micron	MT5C1008DJ								
		45	—	Sony	CXK581020SJ								
		15	—	**Motorola**	MCM6226B	32	300/400	SOJ				◊	
		15	—	AT&T	ATT7CC108								
		15	—	Quality	QS812880								
		17	—	**Motorola**	MCM6226B	32	300/400	SOJ				◊	
		20	—	**Motorola**	MCM6226B	32	300/400	SOJ				◊	
		20	—	Quality	QS812880								
		25	—	**Motorola**	MCM6226B	32	300/400	SOJ				◊	
		25	—	Quality	QS812880								
		35	—	**Motorola**	MCM6226B	32	300/400	SOJ				◊	
		8	—	**Motorola**	MCM6726A	32	400	SOJ	◊			◊	
		10	—	**Motorola**	MCM6726	32	400	SOJ	◊			◊	
		10	—	**Motorola**	MCM6726A	32	400	SOJ	◊			◊	
		10	—	IDT	IDT71B124								
		10	—	Samsung	KM68B1002								
		12	—	**Motorola**	MCM6726	32	400	SOJ	◊			◊	
		12	—	**Motorola**	MCM6726A	32	400	SOJ	◊			◊	
		12	—	IDT	IDT71B124								
		15	—	**Motorola**	MCM6726	32	400	SOJ	◊			◊	
		15	—	**Motorola**	MCM6726A	32	400	SOJ	◊			◊	
		15	—	IDT	IDT71B124								
	128K x 9	16	—	**Motorola**	MCM67D709	52		PLCC	◊	◊		◊	
		20	—	**Motorola**	MCM67D709	52		PLCC	◊	◊		◊	
		5	10	**Motorola**	MCM67Q709				◊	◊			
		6	12	**Motorola**	MCM67Q709				◊	◊			
	256K x 4	20	—	**Motorola**	MCM6229A	28	400	SOJ				◊	
		20	—	AT&T	ATT7C106J								

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		20	—	Hitachi	HM624256AJ								
		20	—	IDT	IDT71028S								
		20	—	Micron	MT5C1008DJ								
		20	—	Samsung	KM641001								
		20	—	Sharp	LH521002								
		20	—	NEC	μ431004								
		25	—	**Motorola**	MCM6229A	28	400	SOJ				◊	
		25	—	AT&T	ATT7C106J								
		25	—	Cypress	CY7C106								
		25	—	Fujitsu	MB82B005								
		25	—	IDT	IDT71028S								
		25	—	Micron	MT5C1005DJ								
		25	—	Mitsubishi	M5M51004P								
		25	—	NEC	μ431004								
		25	—	Samsung	KM641001								
		25	—	Sharp	LH521002K								
		35	—	**Motorola**	MCM6229A	28	400	SOJ				◊	
		35	—	Cypress	CY7C106								
		35	—	Fujitsu	MB82B005								
		35	—	Micron	MT5C1005DJ								
		35	—	Mitsubishi	M5M51004P								
		35	—	NEC	μ431004								
		35	—	Samsung	KM641001								
		35	—	Sharp	LH521002K								
		45	—	**Motorola**	MCM6229A	28	400	SOJ				◊	
		45	—	Cypress	CY7C106								
		45	—	Micron	MT5C1005DJ								
		45	—	Mitsubishi	M5M51004P								
		15	—	**Motorola**	MCM6229B	28	300/400	SOJ				◊	
		17	—	**Motorola**	MCM6229B	28	300/400	SOJ				◊	
		20	—	**Motorola**	MCM6229B	28	300/400	SOJ				◊	
		25	—	**Motorola**	MCM6229B	28	300/400	SOJ				◊	
		35	—	**Motorola**	MCM6229B	28	300/400	SOJ				◊	
		8	—	**Motorola**	MCM6728A	28	400	SOJ	◊				
		10	—	**Motorola**	MCM6728	28	400	SOJ	◊				

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		10	—	**Motorola**	MCM6728A	28	400	SOJ	◊				
		10	—	Samsung	KM64B1002								
		12	—	**Motorola**	MCM6728	28	400	SOJ	◊				
		12	—	**Motorola**	MCM6728A	28	400	SOJ	◊				
		12	—	Samsung	KM64B1002								
		12	—	Toshiba	TC55B4256P								
		15	—	**Motorola**	MCM6728	28	400	SOJ	◊				
		15	—	**Motorola**	MCM6728A	28	400	SOJ	◊				
		15	—	IDT	IDT71BB028								
		15	—	Toshiba	TC55B4256P								
		8	—	**Motorola**	MCM6729A	32	400	SOJ	◊			◊	
		10	—	**Motorola**	MCM6729	32	400	SOJ	◊			◊	
		10	—	**Motorola**	MCM6729A	32	400	SOJ	◊			◊	
		10	—	Samsung	KM64B1003								
		12	—	**Motorola**	MCM6729	32	400	SOJ	◊			◊	
		12	—	**Motorola**	MCM6729A	32	400	SOJ	◊			◊	
		12	—	Samsung	KM64B1003								
		12	—	Toshiba	TC55B4257P								
		15	—	**Motorola**	MCM6729	32	400	SOJ	◊			◊	
		15	—	**Motorola**	MCM6729A	32	400	SOJ	◊			◊	
		15	—	IDT	IDT71B028								
		—	12	**Motorola**	MCM67F804	32	400	SOJ	◊	◊	◊	◊	
		—	15	**Motorola**	MCM67F804	32	400	SOJ	◊	◊	◊	◊	
		6	10	**Motorola**	MCM67P804	32	400	SOJ	◊	◊		◊	
		7	12	**Motorola**	MCM67P804	32	400	SOJ	◊	◊		◊	
		5	10	**Motorola**	MCM67Q804	36	400	SOJ	◊	◊		◊	
		6	12	**Motorola**	MCM67Q804	36	400	SOJ	◊	◊		◊	
	1M x 1	20	—	**Motorola**	MCM6227A	28	400	SOJ					
		20	—	AT&T	ATT7C107J								
		20	—	Hitachi	HM621100A								
		20	—	Micron	MT5C1001DJ								
		20	—	NEC	µ431001								
		20	—	Samsung	KM611001								
		25	—	**Motorola**	MCM6227A	28	400	SOJ					
		25	—	AT&T	ATT7C107J								

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		25	—	Cypress	CY7C107								
		25	—	Fujitsu	MB82B001								
		25	—	Hitachi	HM621100A								
		25	—	Micron	MT5C1001DJ								
		25	—	NEC	µ431001								
		25	—	Samsung	KM611001								
		35	—	**Motorola**	MCM6227A	28	400	SOJ					
		35	—	Cypress	CY7C107								
		35	—	Fujitsu	MB82B001								
		35	—	Hitachi	HM621100A								
		35	—	Micron	MT5C1001DJ								
		35	—	NEC	µ431001								
		35	—	Samsung	KM611001								
		45	—	**Motorola**	MCM6227A	28	400	SOJ					
		45	—	Cypress	CY7C107								
		45	—	Micron	MT5C1001DJ								
		15	—	**Motorola**	MCM6227B	28	300/400	SOJ					
		17	—	**Motorola**	MCM6227B	28	300/400	SOJ					
		20	—	**Motorola**	MCM6227B	28	300/400	SOJ					
		25	—	**Motorola**	MCM6227B	28	300/400	SOJ					
		35	—	**Motorola**	MCM6227B	28	300/400	SOJ					
512K	**32K x 18**	12	—	**Motorola**	MCM67A518	52		PLCC			◊	◊	
		15	—	**Motorola**	MCM67A518	52		PLCC			◊	◊	
		20	—	**Motorola**	MCM67A518	52		PLCC			◊	◊	
		9	15	**Motorola**	MCM67B518	52		PLCC		◊		◊	◊
		10	12.5	Cypress	CY7C175								
		9	15	IC Works	ICW73B586								
		12	20	**Motorola**	MCM67B518	52		PLCC		◊		◊	◊
		12	15	Cypress	CY7C175								
		12	20	IC Works	ICW73B586								
		18	25	**Motorola**	MCM67B518	52		PLCC		◊		◊	◊
		14	20	Cypress	CY7C175								
		7	12.5	**Motorola**	MCM67C518	52		PLCC		◊		◊	◊
		9	15	**Motorola**	MCM67C518	52		PLCC		◊		◊	◊
		9	15	**Motorola**	MCM67H518	52		PLCC		◊		◊	◊

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		12	20	**Motorola**	MCM67H518	52		PLCC		◊		◊	◊
		18	25	**Motorola**	MCM67H518	52		PLCC		◊		◊	◊
		7	12.5	**Motorola**	MCM67J518	52		PLCC		◊		◊	◊
		9	15	**Motorola**	MCM67J518	52		PLCC		◊		◊	◊
		9	12.5	**Motorola**	MCM67M518	52		PLCC		◊		◊	◊
		11	15	**Motorola**	MCM67M518	52		PLCC		◊		◊	◊
		14	20	**Motorola**	MCM67M518	52		PLCC		◊		◊	◊
		19	25	**Motorola**	MCM67M518	52		PLCC		◊		◊	◊
		12	—	**Motorola**	MCM67W518	52		PLCC			◊		
		15	—	**Motorola**	MCM67W518	52		PLCC			◊		
		20	—	**Motorola**	MCM67W518	52		PLCC			◊		
256K	**16K x 16**	15	—	**Motorola**	MCM62990A	52		PLCC		◊	◊	◊	◊
		15	—	Micron	MT58C1616EJ								
		20	—	**Motorola**	MCM62990A	52		PLCC		◊	◊	◊	◊
		20	—	Micron	MT58C1616EJ								
		25	—	**Motorola**	MCM62990A	52		PLCC		◊	◊	◊	◊
		25	—	Micron	MT58C1616EJ								
		15	—	**Motorola**	MCM62995A	52		PLCC			◊	◊	◊
		15	—	Micron	MT5C2516EJ								
		20	—	**Motorola**	MCM62995A	52		PLCC			◊	◊	◊
		20	—	Micron	MT5C2516EJ								
		25	—	**Motorola**	MCM62995A	52		PLCC			◊	◊	◊
		25	—	Micron	MT5C2516EJ								
		15	—	**Motorola**	MCM62996	52		PLCC				◊	
		20	—	**Motorola**	MCM62996	52		PLCC				◊	
		25	—	**Motorola**	MCM62996	52		PLCC				◊	
	32K x 9	15	—	**Motorola**	MCM6205C	32	300	SOJ				◊	
		15	—	**Motorola**	MCM6205D	32	300	SOJ				◊	
		15	—	Micron	MT5C2889								
		15	—	Mitsubishi	M5M5279								
		15	—	NEC	μ43259								
		15	—	Sony	CXK59288								
		17	—	**Motorola**	MCM6205C	32	300	SOJ				◊	
		17	—	**Motorola**	MCM6205D	32	300	SOJ				◊	
		17	—	Micron	MT5C2889								

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		17	—	Sony	CXK59288								
		17	—	Toshiba	TC55329								
		20	—	**Motorola**	MCM6205C	32	300	SOJ				◊	
		20	—	**Motorola**	MCM6205D	32	300	SOJ				◊	
		20	—	IDT	IDT71259								
		20	—	Micron	MT5C2889								
		20	—	Mitsubishi	M5M5279								
		20	—	NEC	µ43259								
		20	—	Sony	CXK59288								
		20	—	Toshiba	TC55329								
		25	—	**Motorola**	MCM6205C	32	300	SOJ				◊	
		25	—	**Motorola**	MCM6205D	32	300	SOJ				◊	
		25	—	Fujitsu	MB8299								
		25	—	IDT	IDT71259								
		25	—	Micron	MT5C2889								
		25	—	Mitsubishi	M5M5279								
		25	—	NEC	µ43259								
		25	—	Sony	CXK59288								
		25	—	Toshiba	TC55329								
		35	—	**Motorola**	MCM6205C	32	300	SOJ				◊	
		35	—	**Motorola**	MCM6205D	32	300	SOJ				◊	
		35	—	Fujitsu	MB8299								
		35	—	IDT	IDT71259								
		35	—	Mitsubishi	M5M5279								
		35	—	Toshiba	TC55329								
		10	—	**Motorola**	MCM6705A	32	300	SOJ					
		10	—	Mitsubishi	M5M52B79P								
		10	—	IDT	IDT71B259								
		10	—	Toshiba	TC55B329P								
		10	—	Samsung	KM69B257A								
		12	—	**Motorola**	MCM6705A	32	300	SOJ					
		12	—	Mitsubishi	M5M52B79P								
		12	—	IDT	IDT71B259								
		12	—	Toshiba	TC55B329P								
		12	—	Samsung	KM69B257A								

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		15	—	**Motorola**	MCM62110	52		PLCC		◊	◊	◊	◊
		17	—	**Motorola**	MCM62110	52		PLCC		◊	◊	◊	◊
		20	—	**Motorola**	MCM62110	52		PLCC		◊	◊	◊	◊
		11	15	**Motorola**	MCM62486A	44		PLCC		◊		◊	◊
		11	15	Cypress	CY7B173A								
		10	15	IC Works	ICW79B586								
		11	15	IDT	IDT71B590S								
		12	20	**Motorola**	MCM62486A	44		PLCC		◊		◊	◊
		12	20	Cypress	CY7B173A								
		12	20	IC Works	ICW79B586								
		14	20	**Motorola**	MCM62486A	44		PLCC		◊		◊	◊
		19	25	**Motorola**	MCM62486A	44		PLCC		◊		◊	◊
		19	25	SGS-Thomson	MK62486Q19								
		24	30	**Motorola**	MCM62486A	44		PLCC		◊		◊	◊
		25	30	SGS-Thomson	MK62486Q25								
		11	15	**Motorola**	MCM62486B	44		PLCC		◊		◊	◊
		11	15	Cypress	CY7B173A								
		10	15	IC Works	ICW79B586								
		11	15	IDT	IDT71B590S								
		12	20	**Motorola**	MCM62486B	44		PLCC		◊		◊	◊
		12	20	Cypress	CY7B173A								
		12	20	IC Works	ICW79B586								
		14	20	**Motorola**	MCM62486B	44		PLCC		◊		◊	◊
		19	25	**Motorola**	MCM62486B	44		PLCC		◊		◊	◊
		19	25	SGS-Thomson	MK62486Q19								
		24	30	**Motorola**	MCM62486B	44		PLCC		◊		◊	◊
		25	30	SGS-Thomson	MK62486Q25								
		11	15	**Motorola**	MCM62940A	44		PLCC		◊		◊	◊
		12	20	**Motorola**	MCM62940A	44		PLCC		◊		◊	◊
		14	20	**Motorola**	MCM62940A	44		PLCC		◊		◊	◊
		19	25	**Motorola**	MCM62940A	44		PLCC		◊		◊	◊
		19	25	SGS-Thomson	MK62940Q19								
		24	30	**Motorola**	MCM62940A	44		PLCC		◊		◊	◊
		25	30	SGS-Thomson	MK62940Q25								
		11	15	**Motorola**	MCM62940B	44		PLCC		◊		◊	◊

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		12	20	**Motorola**	MCM62940B	44		PLCC		◊		◊	◊
		14	2	**Motorola**	MCM62940B	44		PLCC		◊		◊	◊
		19	25	**Motorola**	MCM62940B	44		PLCC		◊		◊	◊
		19	25	SGS-Thomson	MK62940Q19								
		24	30	**Motorola**	MCM62940B	44		PLCC		◊		◊	◊
		25	30	SGS-Thomson	MK62940Q25								
	32K x 8	15	—	**Motorola**	MCM6206C	28	300	PDIP, SOJ				◊	
		15	—	**Motorola**	MCM6206D	28	300	PDIP, SOJ				◊	
		15	—	AT&T	ATT7C199								
		15	—	Hitachi	HM62832								
		15	—	IDT	IDT71256								
		15	—	Micron	MT5C2568								
		15	—	Mitsubishi	M5M5278								
		15	—	NEC	μ43258A								
		15	—	Paradigm	PDM51256								
		15	—	Quality	QS83280								
		15	—	Samsung	KM68257B								
		15	—	Sharp	LH52258A								
		15	—	Sony	CXK58258A								
		17	—	**Motorola**	MCM6206D	28	300	PDIP, SOJ				◊	
		17	—	IDT	IDT71256								
		17	—	Toshiba	TC55328P								
		20	—	**Motorola**	MCM6206C	28	300	PDIP, SOJ				◊	
		20	—	**Motorola**	MCM6206D	28	300	PDIP, SOJ				◊	
		20	—	AT&T	ATT7C199								
		20	—	Hitachi	HM62832								
		20	—	IDT	IDT71256								
		20	—	Micron	MT5C2568								
		20	—	Mitsubishi	M5M5278								
		20	—	NEC	μ43258A								
		20	—	Paradigm	PDM51256								
		20	—	Performance	P4C1256								
		20	—	Quality	QS83280								
		20	—	Samsung	KM68257B								
		20	—	Sharp	LH52258								

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		20	—	Sony	CXK58258								
		20	—	Toshiba	TC55328								
		25	—	**Motorola**	MCM6206C	28	300	PDIP, SOJ				◊	
		25	—	**Motorola**	MCM6206D	28	300	PDIP, SOJ				◊	
		25	—	AT&T	ATT7C199								
		25	—	Cypress	CY7C199								
		25	—	Fujitsu	MB8298								
		25	—	Hitachi	HM62832								
		25	—	IDT	IDT71256								
		25	—	Micron	MT5C2568								
		25	—	Mitsubishi	M5M5278								
		25	—	NEC	μ43258								
		25	—	Paradigm	PDM51256								
		25	—	Performance	P4C1256								
		25	—	Quality	QS83280								
		25	—	Samsung	KM68257								
		25	—	Sharp	LH52253								
		25	—	Sony	CXK58258								
		25	—	Toshiba	TC55328								
		35	—	**Motorola**	MCM6206C	28	300	PDIP, SOJ				◊	
		35	—	**Motorola**	MCM6206D	28	300	PDIP, SOJ				◊	
		35	—	Cypress	CY7C199								
		35	—	Fujitsu	MB8298								
		35	—	IDT	IDT71256								
		35	—	Micron	MT5C2568								
		35	—	Mitsubishi	M5M5278P								
		35	—	NEC	μ43258								
		35	—	Sharp	LH52258								
		35	—	Sony	CXK58258								
		35	—	Toshiba	TC55328								
		25	—	**Motorola**	MCM62V06D	28	300	PDIP, SOJ					
		25	—	Mitsubishi	M5M5278FP								
		35	—	**Motorola**	MCM62V06D	28	300	PDIP, SOJ					
		35	—	Mitsubishi	M5M5278FP								
		8	—	**Motorola**	MCM6706A	28	300	SOJ				◊	

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		8	—	Samsung	KM68B257A								
		10	—	**Motorola**	MCM6706A	28	300	SOJ				◊	
		10	—	Samsung	KM68B257A								
		10	—	Toshiba	TC55B328								
		10	—	Mitsubishi	M5M52B78								
		10	—	IDT	IDT71B256								
		10	—	Hitachi	HM67832								
		12	—	**Motorola**	MCM6706A	28	300	SOJ				◊	
		12	—	Samsung	KM68B257A								
		12	—	Toshiba	TC55B328								
		12	—	Mitsubishi	M5M52B78								
		12	—	IDT	IDT71B256								
		12	—	Hitachi	HM67832								
		12	—	Cypress	CY7B199								
		6	—	**Motorola**	MCM6706R	32	300	SOJ	◊			◊	
		7	—	**Motorola**	MCM6706R	32	300	SOJ	◊			◊	
		8	—	**Motorola**	MCM6706R	32	300	SOJ	◊			◊	
		8	—	Mitsubishi	M5M52B88								
	64K x 4	15	—	**Motorola**	MCM6208C	24	300	PDIP, SOJ					
		15	—	AT&T	ATT7C194								
		15	—	Micron	MT5C2564								
		15	—	Mitsubishi	M5M5258								
		15	—	NEC	µ43254B								
		15	—	Paradigm	PDM41258								
		15	—	Quality	QS86440								
		15	—	Sharp	LH52252								
		20	—	**Motorola**	MCM6208C	24	300	PDIP, SOJ					
		20	—	AT&T	ATT7C194								
		20	—	Micron	MT5C2564								
		20	—	Mitsubishi	M5M5258								
		20	—	NEC	µ43254B								
		20	—	Paradigm	PDM41258								
		20	—	Performance	P4C1258								
		20	—	Quality	QS86440								
		20	—	Sharp	LH52252								

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		20	—	Toshiba	TC55464								
		25	—	**Motorola**	MCM6208C	24	300	PDIP, SOJ					
		25	—	AT&T	ATT7C194								
		25	—	Cypress	CY7C194								
		25	—	Fujitsu	MB81C84A								
		25	—	Hitachi	HM6208								
		25	—	Micron	MT5C2564								
		25	—	SGS-Thompson	IMS1820D3								
		25	—	Mitsubishi	M5M5258								
		25	—	NEC	μ43254B								
		25	—	Paradigm	PDM41258								
		25	—	Performance	P4C1258								
		25	—	Samsung	KM64257A								
		25	—	Sharp	LH52252								
		25	—	Toshiba	TC55464								
		15	—	**Motorola**	MCM6209C	28	300	PDIP, SOJ				◊	
		15	—	AT&T	ATT7C196								
		15	—	IDT	IDT61298								
		15	—	Micron	MT5C2565								
		15	—	Mitsubishi	M5M5259								
		15	—	NEC	μ43253								
		15	—	Paradigm	PDM41259								
		15	—	Quality	QS86446								
		15	—	Sharp	LH52253								
		15	—	Samsung	KM64258B								
		20	—	**Motorola**	MCM6209C	28	300	PDIP, SOJ				◊	
		20	—	AT&T	ATT7C196								
		20	—	IDT	IDT61298								
		20	—	Micron	MT5C2565								
		20	—	Mitsubishi	M5M5259								
		20	—	NEC	μ43253B								
		20	—	Paradigm	PDM41259								
		20	—	Performance	P4C1298								
		20	—	Quality	QS86446								
		20	—	Samsung	KM64258B								

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		20	—	Sharp	LH52253								
		20	—	Toshiba	TC55465								
		25	—	**Motorola**	MCM6209C	28	300	PDIP, SOJ				◊	
		25	—	AT&T	ATT7C196								
		25	—	Cypress	CY7C195								
		25	—	IDT	IDT61298								
		25	—	Micron	MT5C2565								
		25	—	Mitsubishi	M5M5259								
		25	—	NEC	μ43253								
		25	—	Paradigm	PDM41259								
		25	—	Performance	P4C1298								
		25	—	Quality	QS86446								
		25	—	Samsung	KM64258B								
		25	—	Sharp	LH52253								
		25	—	Toshiba	TC55465								
		8	—	**Motorola**	MCM6708A	24	300	SOJ					
		10	—	**Motorola**	MCM6708A	24	300	SOJ					
		10	—	Toshiba	TC55B464								
		10	—	Hitachi	HM6708SH								
		12	—	**Motorola**	MCM6708A	24	300	SOJ					
		12	—	Cypress	CY7B194								
		12	—	Hitachi	HM6708SH								
		12	—	Toshiba	TC55B464								
		8	—	**Motorola**	MCM6709A	28	300	SOJ					
		8	—	Samsung	KM64B258A								
		10	—	**Motorola**	MCM6709A	28	300	SOJ					
		10	—	Samsung	KM64B258A								
		10	—	Toshiba	TC55B465								
		10	—	IDT	IDT61B298								
		10	—	Hitachi	HM6709SH								
		12	—	**Motorola**	MCM6709A	28	300	SOJ					
		12	—	Samsung	KM64B258A								
		12	—	Toshiba	TC55B465								
		12	—	IDT	IDT61B298								
		12	—	Hitachi	HM6709SH								

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		12	—	Cypress	CY7B194								
		6	—	**Motorola**	MCM6709R	28	300	SOJ	◊			◊	
		7	—	**Motorola**	MCM6709R	28	300	SOJ	◊			◊	
		8	—	**Motorola**	MCM6709R	28	300	SOJ	◊			◊	
		15	—	**Motorola**	MCM62980	28	300	SOJ		◊		◊	
		20	—	**Motorola**	MCM62980	28	300	SOJ		◊		◊	
		15	—	**Motorola**	MCM62981	32	300	SOJ					
		20	—	**Motorola**	MCM62981	32	300	SOJ					
192K	**8K x 24**	20	—	**Motorola**	MCM56824A	52		PLCC				◊	◊
		20	—	**Motorola**	MCM56824AZP	86		OMPAC				◊	◊
		25	—	**Motorola**	MCM56824A	52		PLCC				◊	◊
		25	—	**Motorola**	MCM56824AZP	86		OMPAC				◊	◊
		35	—	**Motorola**	MCM56824A	52		PLCC				◊	◊
		35	—	**Motorola**	MCM56824AZP	86		OMPAC				◊	◊
128K	**8K x 16**	12	20	**Motorola**	MCM62T316	44		PLCC		◊			◊
64K	**8K x 9**	12	—	**Motorola**	MCM6265C	28	300	PDIP, SOJ				◊	
		15	—	**Motorola**	MCM6265C	28	300	PDIP, SOJ				◊	
		15	—	IDT	IDT7169S								
		15	—	Mitsubishi	M5M5179								
		15	—	NEC	μ4369								
		15	—	SGS-Thompson	IMS1695								
		15	—	Sony	CXK5972								
		15	—	Toshiba	TC5589								
		20	—	**Motorola**	MCM6265C	28	300	PDIP, SOJ				◊	
		20	—	Mitsubishi	M5M5179								
		20	—	NEC	μ4369								
		20	—	Performance	P4C163								
		20	—	SGS-Thompson	IMS1695								
		20	—	Sony	CXK5972								
		20	—	Toshiba	TC5589								
		25	—	**Motorola**	MCM6265C	28	300	PDIP, SOJ				◊	
		25	—	IDT	IDT7169S								
		25	—	Mitsubishi	M5M5179								
		25	—	Sony	CXK5972								
		25	—	Toshiba	TC5589								

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		35	—	**Motorola**	MCM6265C	28	300	PDIP, SOJ				◊	
		35	—	Fujitsu	MB81C79								
		35	—	IDT	IDT7169S								
		35	—	Mitsubishi	M5M5179								
		35	—	Sony	CXK5972								
		35	—	Toshiba	TC5589								
	8K x 8	12	—	**Motorola**	MCM6264C	28	300	PDIP, SOJ				◊	
		12	—	AT&T	ATT7C185								
		12	—	Micron	MT5C6408								
		12	—	Samsung	KM6865								
		12	—	Toshiba	TC5588								
		15	—	**Motorola**	MCM6264C	28	300	PDIP, SOJ				◊	
		15	—	AT&T	ATT7C185								
		15	—	Cypress	CY7C185								
		15	—	IDT	IDT7164S								
		15	—	Micron	MT5C6408								
		15	—	Mitsubishi	M5M5178								
		15	—	NEC	µ4368								
		15	—	Performance	P4C164								
		15	—	Samsung	KM6865								
		15	—	SGS-Thompson	IMS1635								
		15	—	Toshiba	TC5588								
		20	—	**Motorola**	MCM6264C	28	300	PDIP, SOJ				◊	
		20	—	AT&T	ATT7C185								
		20	—	Cypress	CY7C185								
		20	—	IDT	IDT7164								
		20	—	Micron	MT5C6408								
		20	—	Mitsubishi	M5M5178								
		20	—	NEC	µ4368								
		20	—	Performance	P4C164								
		20	—	Samsung	KM6865								
		20	—	SGS-Thompson	IMS1635								
		20	—	Sony	CXK5863								
		20	—	Toshiba	TC5588								
		25	—	**Motorola**	MCM6264C	28	300	PDIP, SOJ				◊	

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		25	—	AT&T	ATT7C185								
		25	—	Cypress	CY7C185								
		25	—	IDT	IDT7164								
		25	—	Micron	MT5C6408								
		25	—	Mitsubishi	M5M5178								
		25	—	Performance	P4C164								
		25	—	Samsung	KM6865								
		25	—	SGS-Thompson	IMS1635								
		25	—	Sony	CXK5863								
		25	—	Toshiba	TC5588								
		35	—	**Motorola**	MCM6264C	28	300	PDIP, SOJ				◊	
		35	—	Fujitsu	MB81C78								
		35	—	IDT	IDT7164								
		35	—	Micron	MT5C6408								
		35	—	Mitsubishi	M5M5178								
		35	—	Sony	CXK5863								
		35	—	Toshiba	TC5588								
		—	—	**Motorola**	MCM62X308	28	300	SOJ		◊			◊
		—	—	**Motorola**	MCM62Y308	32	300	SOJ		◊			◊
	16K x 4	10	—	**Motorola**	MCM6288C	22	300	PDIP					
		10	—	AT&T	ATT7C164								
		10	—	Micron	MT5C6404								
		10	—	Quality	QS8888A								
		12	—	**Motorola**	MCM6288C	22	300	PDIP					
		12	—	AT&T	ATT7C164								
		12	—	Cypress	CY7C164								
		12	—	Micron	MT5C6404								
		12	—	NEC	μ4362B								
		12	—	Performance	P4C188								
		12	—	Quality	QS8888A								
		12	—	Samsung	KM6465B								
		15	—	**Motorola**	MCM6288C	22	300	PDIP					
		15	—	AT&T	ATT7C164								
		15	—	Cypress	CY7C164								
		15	—	Fujitsu	MB81C74								

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		15	—	IDT	IDT7188S								
		15	—	Micron	MT5C6404								
		15	—	Mitsubishi	M5M5188								
		15	—	NEC	μ4362B								
		15	—	Performance	P4C188								
		15	—	Quality	QS8888A								
		15	—	Samsung	KM6465B								
		15	—	SGS-Thompson	IMS1625								
		15	—	Sony	CXK5466								
		15	—	Toshiba	TC55416								
		20	—	**Motorola**	MCM6288C	22	300	PDIP					
		20	—	AT&T	ATT7C164								
		20	—	Cypress	CY7C164								
		20	—	Fujitsu	MB81C74								
		20	—	IDT	IDT7188S								
		20	—	Micron	MT5C6404								
		20	—	Mitsubishi	M5M5188								
		20	—	NEC	μ4362B								
		20	—	Performance	P4C188								
		20	—	Quality	QS8888								
		20	—	Samsung	KM6465								
		20	—	SGS-Thompson	IMS1625								
		20	—	Sony	CXK5466								
		20	—	Toshiba	TC55416								
		25	—	**Motorola**	MCM6288C	22	300	PDIP					
		25	—	AT&T	ATT7C164								
		25	—	Cypress	CY7C164								
		25	—	Fujitsu	MB81C74								
		25	—	Hitachi	HM6288H								
		25	—	IDT	IDT7188S								
		25	—	Micron	MT5C6404								
		25	—	Mitsubishi	M5M5188								
		25	—	Performance	P4C188								
		25	—	Quality	QS8888								
		25	—	Samsung	KM6465								

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		25	—	SGS-Thompson	IMS1625								
		25	—	Sony	CXK5464								
		25	—	Toshiba	TC55416								
		35	—	**Motorola**	MCM6288C	22	300	PDIP					
		35	—	Fujitsu	MB81C74								
		35	—	Hitachi	HM6288H								
		35	—	IDT	IDT7188S								
		35	—	Micron	MT5C6404								
		35	—	Mitsubishi	M5M5188								
		35	—	Quality	QS8888								
		35	—	Samsung	KM6465A								
		35	—	Sony	CXK5464								
		35	—	Toshiba	TC55416								
	64K x 1	12	—	**Motorola**	MCM6287B	22/24	300	PDIP, SOJ					
		12	—	AT&T	ATT7C187								
		12	—	Micron	MT5C6401								
		12	—	NEC	µ4361B								
		12	—	Performance	P4C187								
		15	—	**Motorola**	MCM6287B	22/24	300	PDIP, SOJ					
		15	—	AT&T	ATT7C187								
		15	—	IDT	IDT7187								
		15	—	Micron	MT5C6401								
		15	—	Mitsubishi	M5M5187								
		15	—	NEC	µ4361B								
		15	—	Performance	P4C187								
		15	—	SGS-Thompson	IMS1605								
		20	—	**Motorola**	MCM6287B	22/24	300	PDIP, SOJ					
		20	—	AT&T	ATT7C187								
		20	—	Cypress	CY7C187								
		20	—	IDT	IDT7187S								
		20	—	Micron	MT5C6401								
		20	—	Mitsubishi	M5M5187								
		20	—	NEC	µ4361B								
		20	—	Performance	P4C187								
		20	—	SGS-Thompson	IMS1605								

Density	Config-uration	Access (ns)	Cycle (ns)	Supplier	Part Number	No. Pins	Width (mils)	Package	Revol. Pinout	Syn-chronous	Latches	Output Enable	Special Function
		25	—	**Motorola**	MCM6287B	22/24	300	PDIP, SOJ					
		25	—	AT&T	ATT7C187								
		25	—	Cypress	CY7C187								
		25	—	Fujitsu	MB81C71A								
		25	—	IDT	IDT7187S								
		25	—	Micron	MT5C6401								
		25	—	Mitsubishi	M5M5187								
		25	—	Performance	P4C187								
		25	—	Samsung	KM6165								
		25	—	SGS-Thompson	IMS1605								
		25	—	Sony	CXK5164								
48K	**4K x 12**	18	—	**Motorola**	MCM62973A	44		PLCC		◊			◊
		20	—	**Motorola**	MCM62973A	44		PLCC		◊		◊	◊
	4K x 10	30	—	**Motorola**	MCM62963A	44		PLCC		◊			◊

BiCMOS Fast Static RAMs

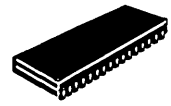
2

TTL I/O

ECL I/O

MCM6705A

32K x 9 Bit Static Random Access Memory



J PACKAGE
300 MIL SOJ
CASE 857

2

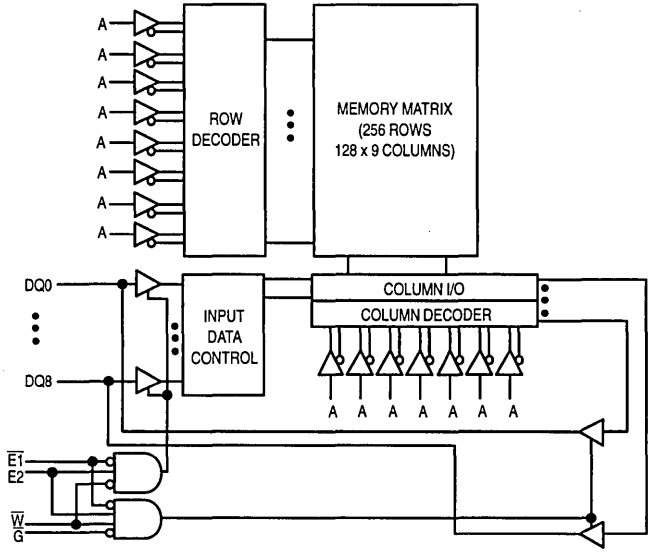
The MCM6705A is a 294,912 bit static random access memory organized as 32,768 words of 9 bits, fabricated using high performance silicon-gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

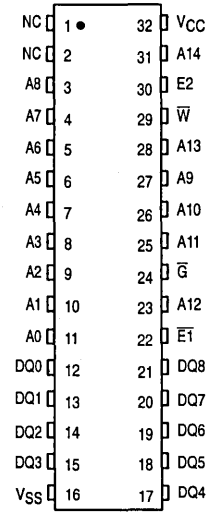
The MCM6705A is available in a 300 mil, 32 lead surface-mount SOJ package.

- Single 5.0 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM6705A-10 = 10 ns
  MCM6705A-12 = 12 ns

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A14	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ8	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

TRUTH TABLE (X = Don't Care)

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	H	Output Disabled	I_{CCA}	High-Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High-Z	Write Cycle

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

* V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
** V_{IL} (min) = –0.5 V dc @ 30.0 mA; V_{IL} (min) = –2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6705A-10	MCM6705A-12	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	195	185	mA
AC Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL}, V_{CC} = max, f = f_{max})	I_{SB1}	125	120	mA
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E1}$ ≥ V_{CC} – 0.2 V, or E2 ≤ V_{SS} + 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V)	I_{SB2}	55	55	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E1}$, E2, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE (See Notes 1, 2, and 3)

Parameter	Symbol		MCM6705A-10		MCM6705A-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	10	—	12	—	ns	4
Address Access Time	t_{AVQV}	t_{AA}	—	10	—	12	ns	
Chip Enable Access Time	t_{ELQV}	t_{ACS}	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	t_{LZ}	1	—	1	—	ns	5, 6, 7
Chip Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	6	0	7	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	t_{LZ}	0	—	0	—	ns	5, 6, 7
Output Enable High to Output High-Z	t_{GHQZ}	t_{HZ}	0	5	0	6	ns	5, 6, 7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ is represented by E in this table. E2 would require a transition opposite of $\overline{E1}$.
4. All read cycle timing is referenced from the last valid address to the first transitioning address.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, $\overline{G}$ = V_{IL}).
9. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

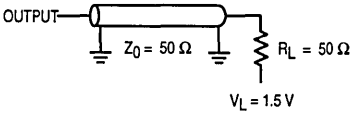


Figure 1A

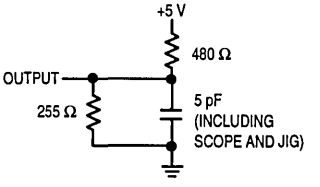


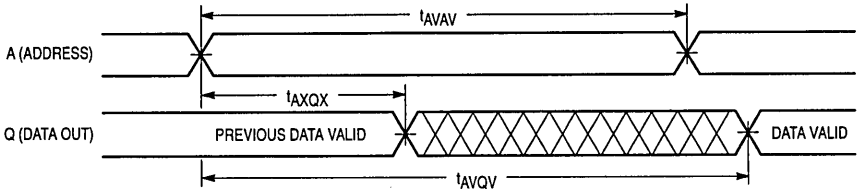
Figure 1B

TIMING LIMITS

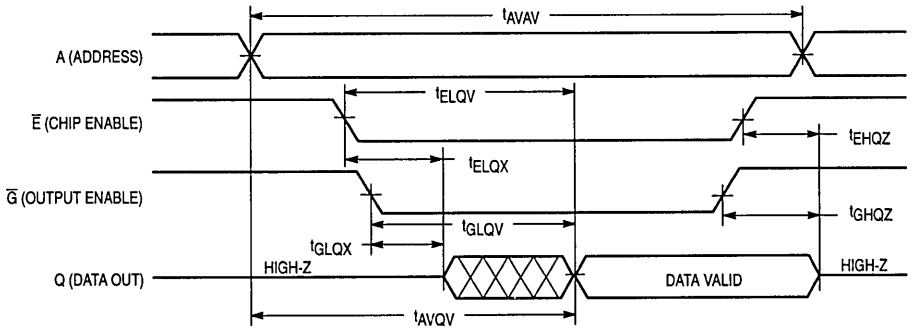
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note 9)

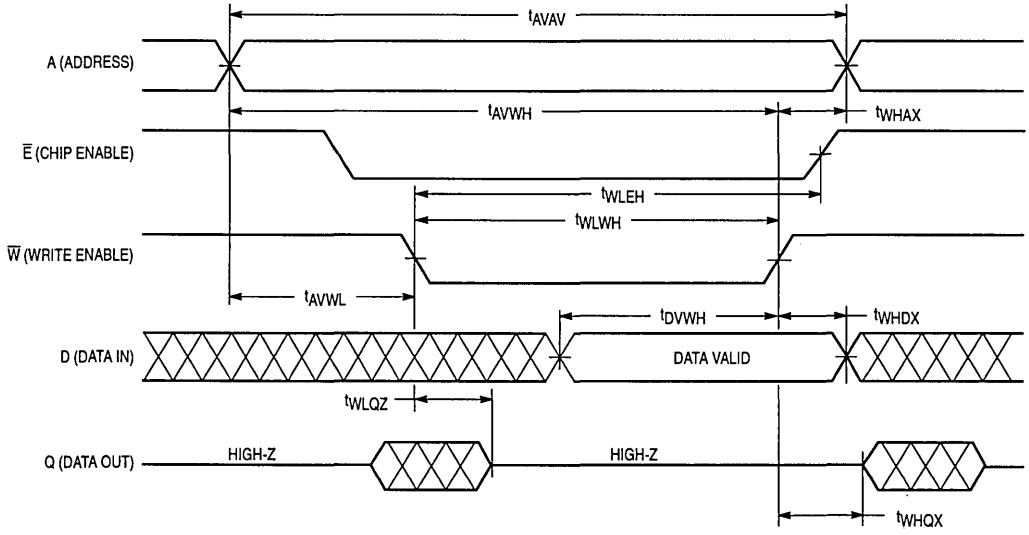


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		MCM6705A-10		MCM6705A-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	5	0	6	ns	5, 6, 7
Write High to Output Active	t_{WHQX}	t_{OW}	3	—	3	—	ns	5, 6, 7
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ is represented by E in this table. E2 would require a transition opposite of $\overline{E1}$.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
6. Parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max is < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

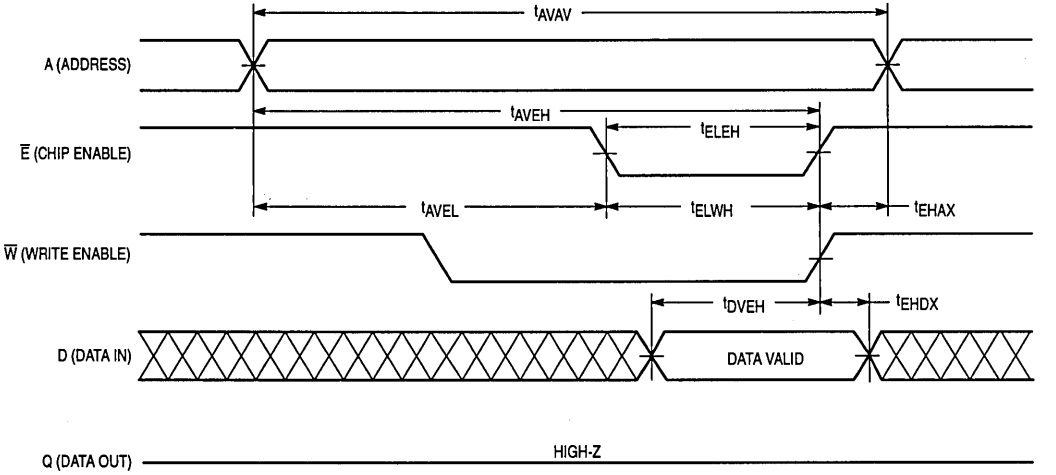


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		MCM6705A-10		MCM6705A-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	ns	4
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	9	—	10	—	ns	
Chip Enable to End of Write	t_{ELWH}, t_{ELEH}	t_{CW}	8	—	9	—	ns	5, 6
Data Valid to End of Write	t_{DVEH}	t_{DW}	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ is represented by E in this table. E2 would require a transition opposite of $\overline{E1}$.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6705A X XX XX

- MCM — Motorola Memory Prefix
- 6705A — Part Number
- X — Package (J = 300 mil SOJ)
- XX — Speed (10 = 10 ns, 12 = 12 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6705AJ10 MCM6705AJ10R2
MCM6705AJ12 MCM6705AJ12R2

MCM6706A

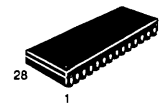
32K x 8 Bit Static Random Access Memory

The MCM6706A is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using high performance silicon-gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

The MCM6706A is available in a 300 mil, 28-lead surface-mount SOJ package.

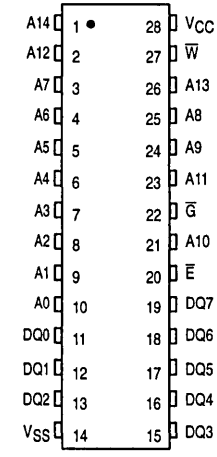
- Single 5.0 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM6706A-8 = 8 ns
  MCM6706A-10 = 10 ns
  MCM6706A-12 = 12 ns



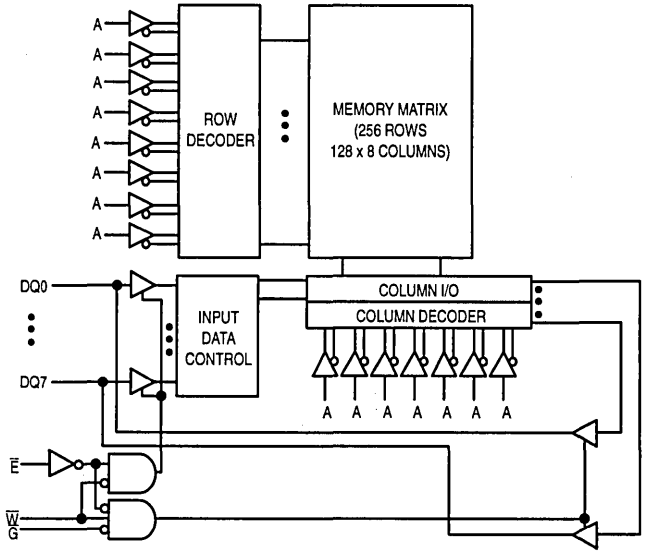
J PACKAGE
300 MIL SOJ
CASE 810B

2

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A14	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ7	Data Input/Output
V_{CC}	+5.0 V Power Supply
V_{SS}	Ground

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle
H	X	X	Not Selected	High-Z	—
L	H	H	Read	High-Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
** V_{IL} (min) = – 0.5 V dc @ 30.0 mA; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6706A-8	6706A-10	6706A-12	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	195	185	175	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	130	120	115	mA
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} – 0.2 V)	I_{SB2}	50	50	50	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	C_{out}	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol		MCM6706A-8		MCM6706A-10		MCM6706A-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	8	—	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	8	—	10	—	12	ns	
Chip Enable Access Time	t_{ELQV}	t_{ACS}	—	8	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	4	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	t_{LZ}	1	—	1	—	1	—	ns	4,5,6
Chip Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	4.5	0	5	0	6	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	t_{LZ}	0	—	0	—	0	—	ns	4,5,6
Output Enable High to Output High-Z	t_{GHQZ}	t_{HZ}	0	4	0	5	0	6	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

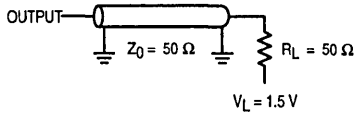


Figure 1A

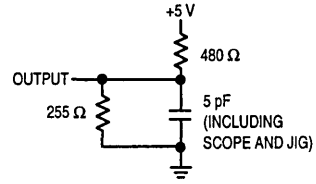


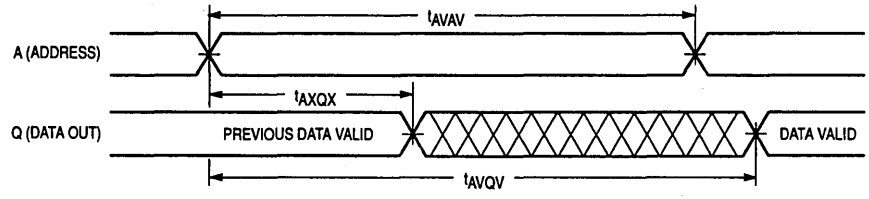
Figure 1B

TIMING LIMITS

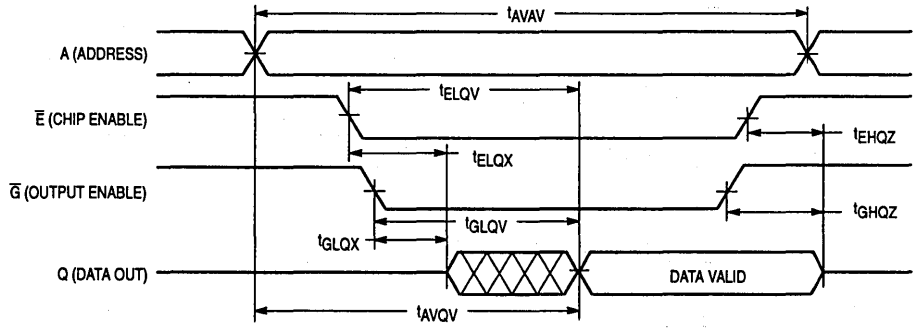
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

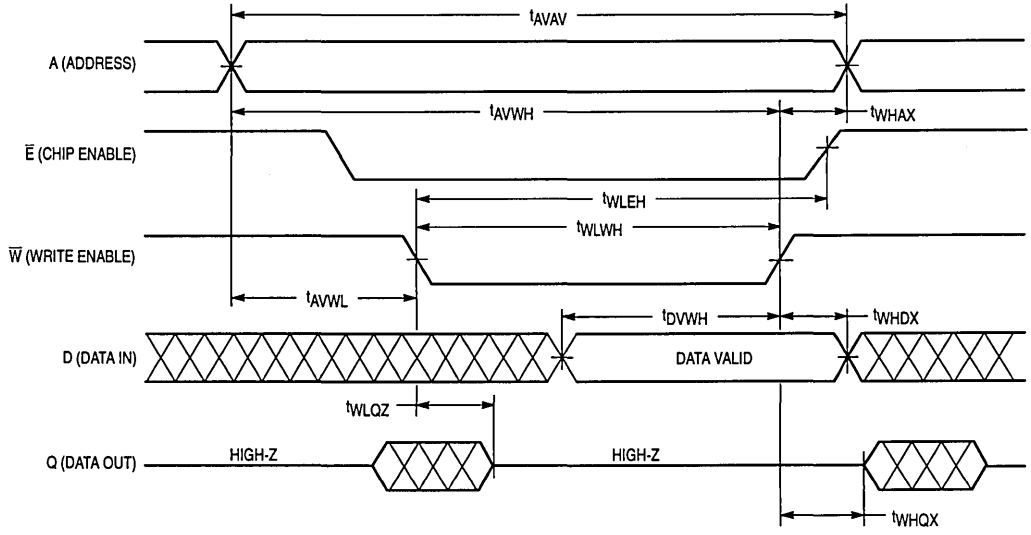


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6706A-8		MCM6706A-10		MCM6706A-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	4	0	5	0	6	ns	4, 5, 6
Wirte High to Output Active	t_{WHQX}	t_{OW}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
5. Parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

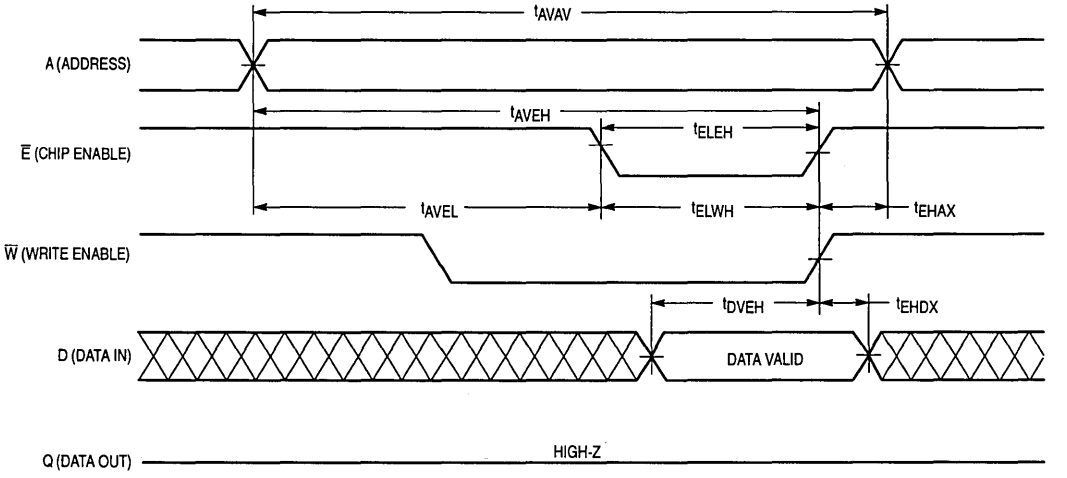


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6706A-8		MCM6706A-10		MCM6706A-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	8	—	9	—	10	—	ns	
Chip Enable to End of Write	t_{ELWH}, t_{ELEH}	t_{CW}	7	—	8	—	9	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	t_{DW}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6706A X XX XX

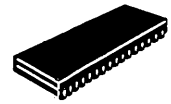
- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns)
- Package (J = 300 mil SOJ)

Full Part Numbers — MCM6706AJ8, MCM6706AJ10, MCM6706AJ12, MCM6706AJ8R2, MCM6706AJ10R2, MCM6706AJ12R2

MCM6706R

Product Preview

32K x 8 Bit Static Random Access Memory



J PACKAGE
300 MIL SOJ
CASE 857

2

The MCM6706R is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using high performance silicon-gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

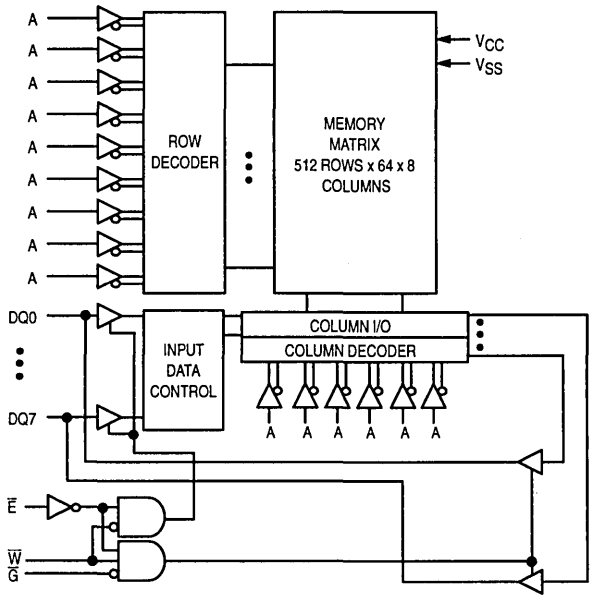
The MCM6706R meets JEDEC standards and is available in a revolutionary pinout 300 mil, 32-lead surface-mount SOJ package.

- Single 5.0 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM6706R-6 = 6 ns
  MCM6706R-7 = 7 ns
  MCM6706R-8 = 8 ns
- Center Power and I/O Pins for Reduced Noise

PIN ASSIGNMENT

A0	1	32	NC
A1	2	31	A14
A2	3	30	A13
A3	4	29	A12
$\overline{E}$	5	28	$\overline{G}$
DQ0	6	27	DQ7
DQ1	7	26	DQ6
V_{CC}	8	25	V_{SS}
V_{SS}	9	24	V_{CC}
DQ2	10	23	DQ5
DQ3	11	22	DQ4
$\overline{W}$	12	21	A11
A4	13	20	A10
A5	14	19	A9
A6	15	18	A8
A7	16	17	NC

BLOCK DIAGRAM



PIN NAMES

A0 – A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ7	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle
H	X	X	Not Selected	High-Z	—
L	H	H	Read	High-Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	− 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	− 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	− 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	− 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
** V_{IL} (min) = − 0.5 V dc @ 30.0 mA; V_{IL} (min) = − 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = − 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6706R-6	6706R-7	6706R-8	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	205	200	195	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	95	90	85	mA
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} − 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} − 0.2 V)	I_{SB2}	20	20	20	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	C_{out}	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol		MCM6706R-6		MCM6706R-7		MCM6706R-8		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	6	—	7	—	8	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	6	—	7	—	8	ns	
Chip Enable Access Time	t_{ELQV}	t_{ACS}	—	6	—	7	—	8	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	4	—	4	—	4	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	t_{LZ}	3	—	3	—	3	—	ns	4,5,6
Chip Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	3	0	3.5	0	4	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	t_{LZ}	0	—	0	—	0	—	ns	4, 5, 6
Output Enable High to Output High-Z	t_{GHQZ}	t_{HZ}	0	3	0	3.5	0	4	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ}max < t_{ELQX}min, and t_{GHQZ}max < t_{GLQX}min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

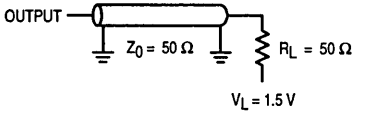


Figure 1A

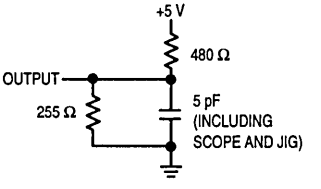
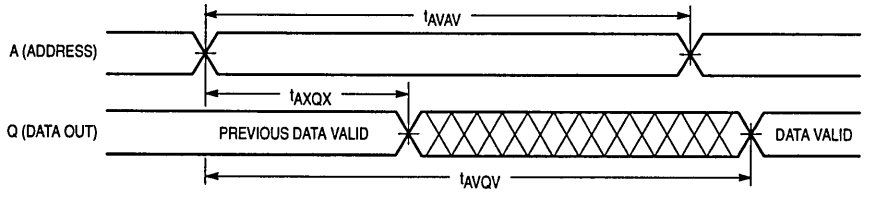


Figure 1B

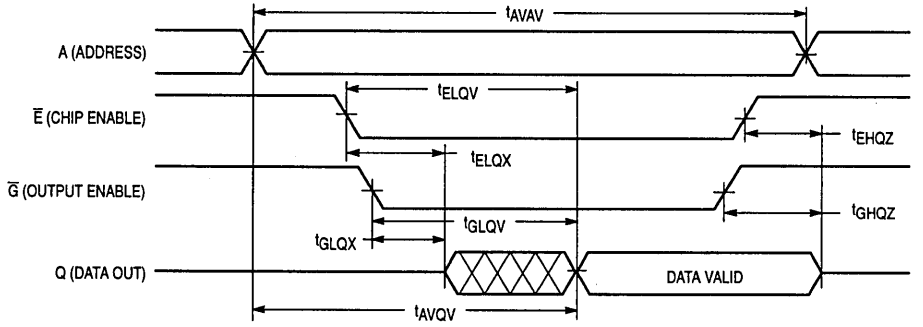
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

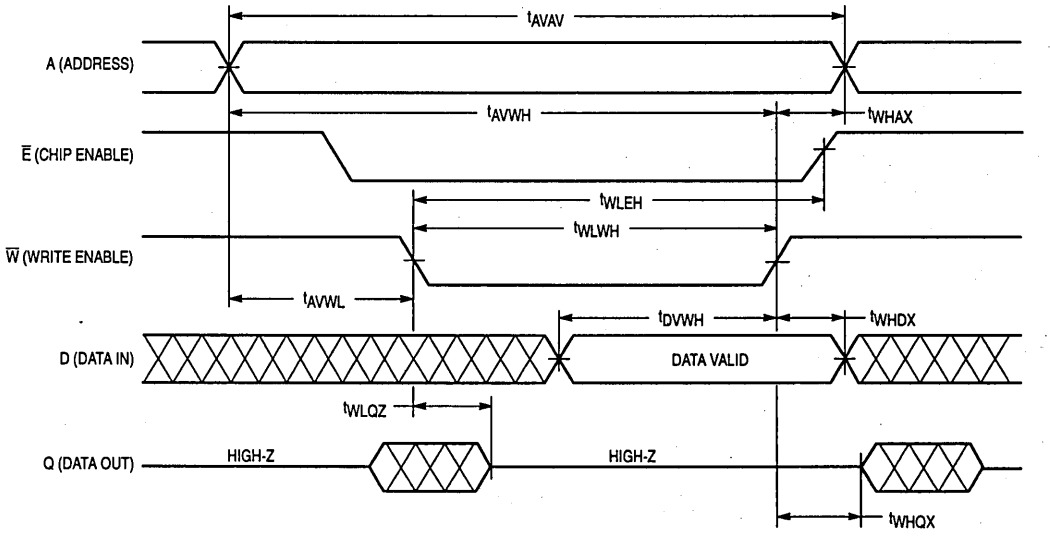


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6706R-6		MCM6706R-7		MCM6706R-8		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	6	—	7	—	8	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	6	—	7	—	8	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	3	—	3.5	—	4	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	3.5	0	3.5	0	4	ns	4, 5, 6
Wirte High to Output Active	t_{WHQX}	t_{OW}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
5. Parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

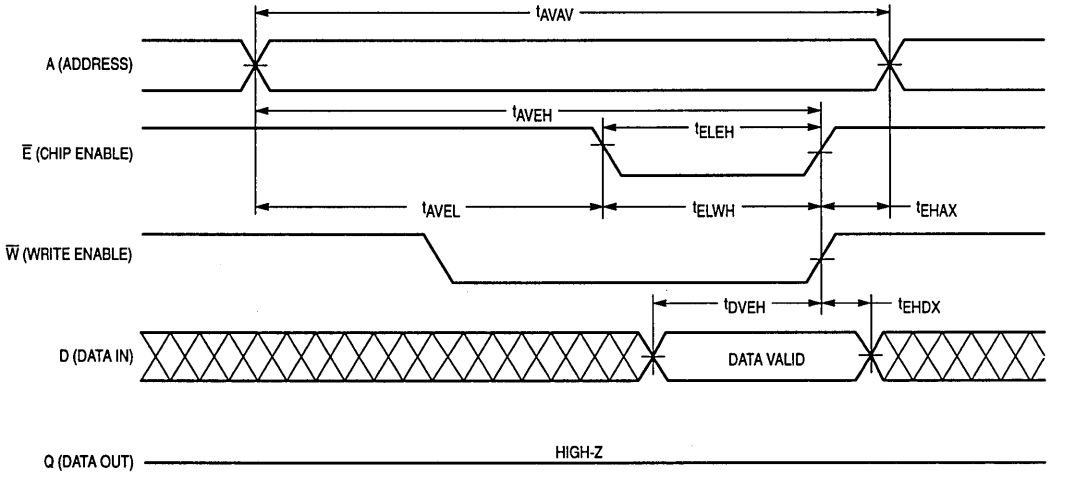


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6706R-6		MCM6706R-7		MCM6706R-8		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	6	—	7	—	8	—	ns	
Chip Enable to End of Write	t_{ELWH}, t_{ELEH}	t_{CW}	5	—	6	—	7	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	t_{DW}	3	—	3.5	—	4	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6706R X XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (6 = 6 ns, 7 = 7 ns, 8 = 8 ns)
- Package (J = 300 mil SOJ)

Full Part Numbers — MCM6706J6, MCM6706RJ7, MCM6706RJ8, MCM6706RJ6R2, MCM6706RJ7R2, MCM6706RJ8R2

64K x 4 Bit Static RAM

MCM6708A
MCM6709A

The MCM6708A and the MCM6709A are 262,144 bit static random access memories organized as 65,536 words of 4 bits, fabricated using high-performance silicon-gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$), a special control feature of the MCM6709A, provides increased system flexibility and eliminates bus contention problems.

The MCM6708A is available in a 300 mil, 24 lead plastic surface-mount SOJ package. The MCM6709A is available in a 300 mil, 28 lead plastic surface-mount SOJ package.

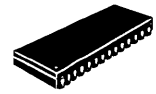
- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Access Times:

MCM6708A-8 = 8 ns	MCM6709A-8 = 8 ns
MCM6708A-10 = 10 ns	MCM6709A-10 = 10 ns
MCM6708A-12 = 12 ns	MCM6709A-12 = 12 ns

MCM6708A

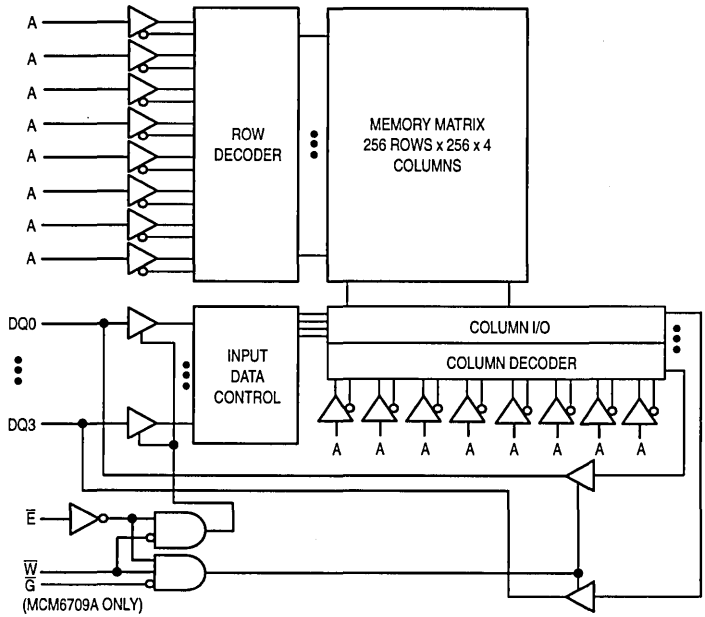
J PACKAGE
300 MIL SOJ
CASE 810A

MCM6709A



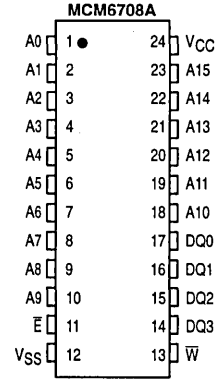
J PACKAGE
300 MIL SOJ
CASE 810B

BLOCK DIAGRAM

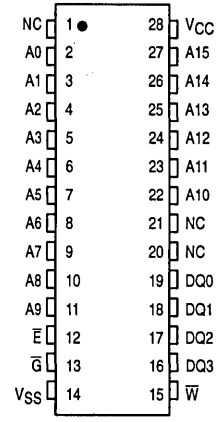


PIN ASSIGNMENT

MCM6708A



MCM6709A



PIN NAMES

A0 – A15 ..... Address Inputs	$\overline{W}$ ..... Write Enable
$\overline{G}$ ..... Output Enable	$\overline{E}$ ..... Chip Enable
DQ0 – DQ3 ..... Data Input/Output	V_{CC} ..... + 5 V Power Supply
V_{SS} ..... Ground	NC ..... No Connection

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Output	Cycle
H	X	X	Not Selected	High-Z	—
L	H	H	Read	High-Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	− 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	− 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	− 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	− 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
** V_{IL} (min) = − 0.5 V dc @ 30.0 mA; V_{IL} (min) = − 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = − 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6708A-8 MCM6709A-8	MCM6708A-10 MCM6709A-10	MCM6708A-12 MCM6709A-12	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	185	175	165	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	120	110	105	mA
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} − 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} − 0.2 V)	I_{SB2}	50	50	50	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	5	pF
Input/Output Capacitance	$C_{I/O}$	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLES 1 AND 2 (See Notes 1 and 2)

Parameter	Symbol		MCM6708A-8 MCM6709A-8		MCM6708A-10 MCM6709A-10		MCM6708A-12 MCM6709A-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	8	—	10	—	12	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	8	—	10	—	12	ns	
Chip Enable Access Time	t_{ELQV}	t_{ACS}	—	8	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	4	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	t_{LZ}	1	—	1	—	1	—	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	t_{LZ}	0	—	0	—	0	—	ns	4, 5, 6
Chip Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	4.5	0	5	0	6	ns	4, 5, 6
Output Enable High to Output High-Z	t_{GHQZ}	t_{HZ}	0	4	0	5	0	6	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.

AC TEST LOADS

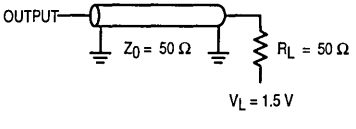


Figure 1A

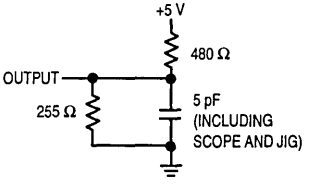


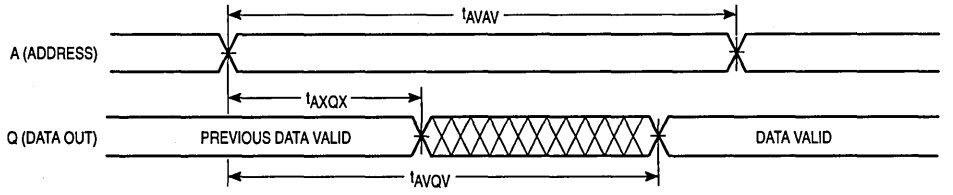
Figure 1B

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

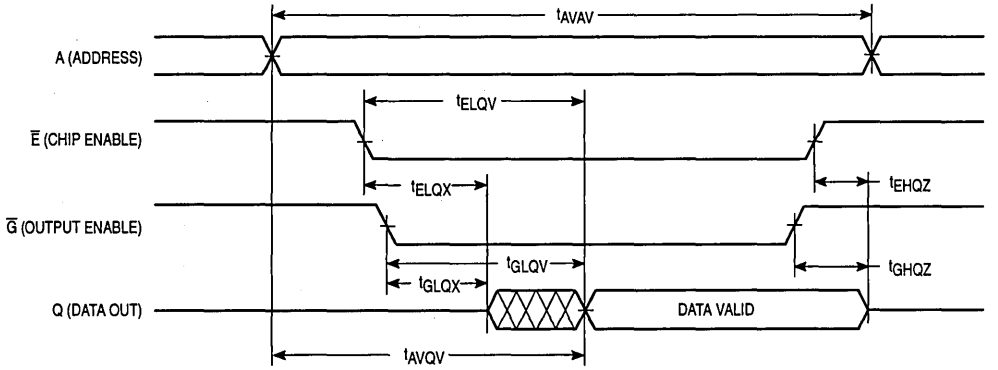
NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Note)



NOTE: Device is continuously selected ($\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$).

READ CYCLE 2 (See Note)



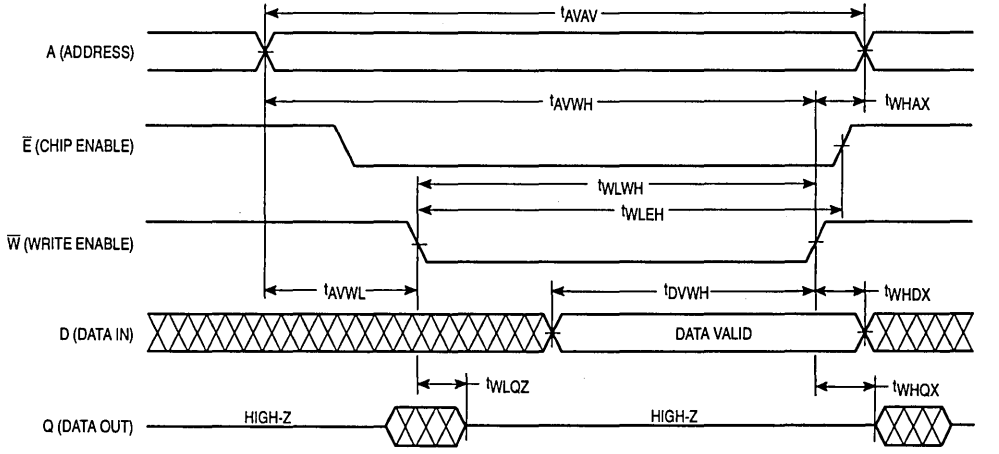
NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6708A-8 MCM6709A-8		MCM6708A-10 MCM6709A-10		MCM6708A-12 MCM6709A-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	t_{WP}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	4	0	5	0	6	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	t_{OW}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

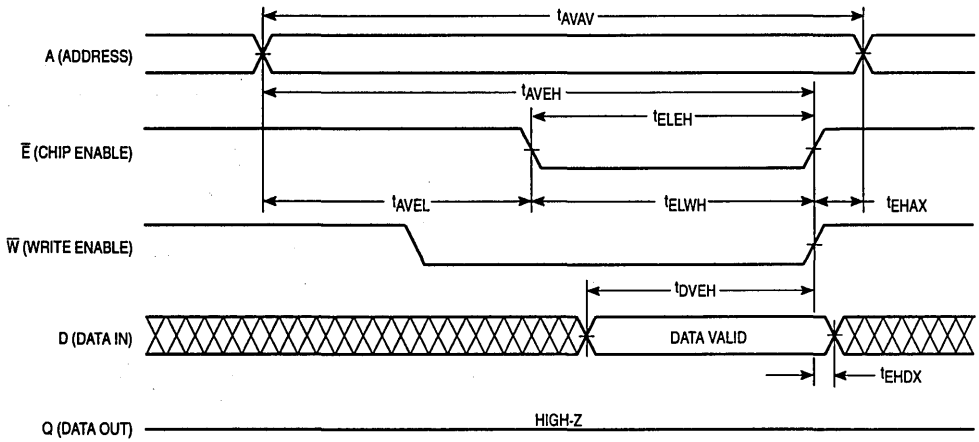


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

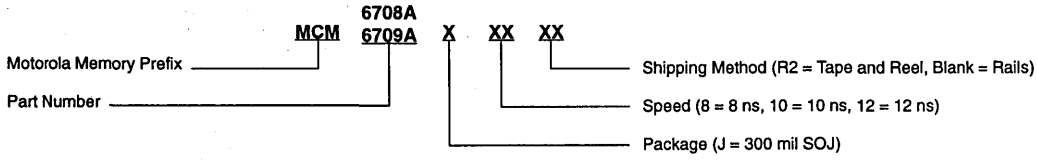
Parameter	Symbol		MCM6708A-8 MCM6709A-8		MCM6708A-10 MCM6709A-10		MCM6708A-12 MCM6709A-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	8	—	10	—	12	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	8	—	9	—	10	—	ns	
Chip Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	7	—	8	—	9	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	t_{DW}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

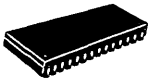


Full Part Numbers — MCM6708AJ8, MCM6708AJ8R2, MCM6708AJ10, MCM6708AJ10R2, MCM6708AJ12, MCM6708AJ12R2, MCM6709AJ8, MCM6709AJ8R2, MCM6709AJ10, MCM6709AJ10R2, MCM6709AJ12, MCM6709AJ12R2

MCM6709R

Product Preview

64K x 4 Bit Static RAM



J PACKAGE
300 MIL SOJ
CASE 810B

2

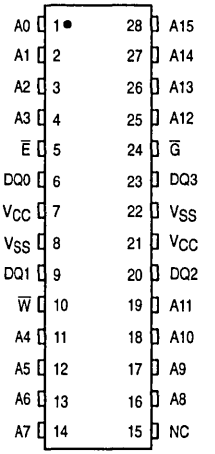
The MCM6709R is a 262,144 bit static random access memory organized as 65,536 words of 4 bits, fabricated using high-performance silicon-gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

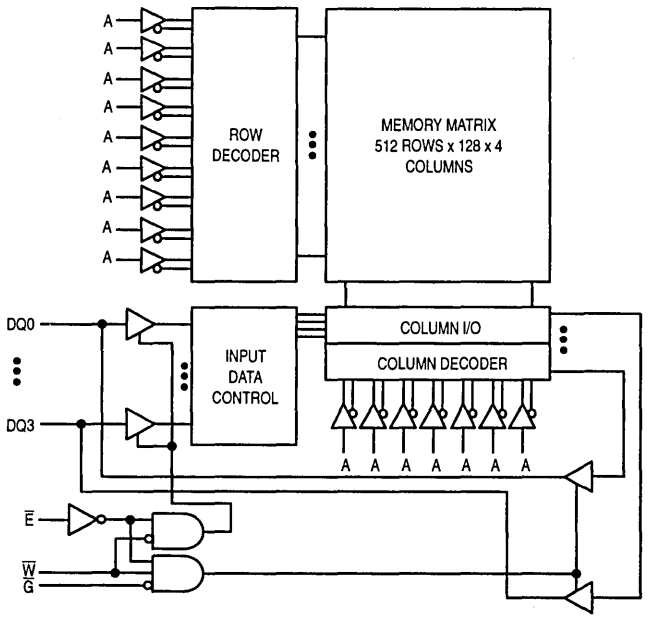
The MCM6709R meets JEDEC standards and is available in a revolutionary pinout 300 mil, 28 lead plastic surface-mount SOJ package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs are TTL Compatible
- Center Power and I/O Pins for Reduced Noise
- Three State Outputs
- Fast Access Times:
  MCM6709R-6 = 6 ns
  MCM6709R-7 = 7 ns
  MCM6709R-8 = 8 ns

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A15	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0 – DQ3	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Output	Cycle
H	X	X	Not Selected	High-Z	—
L	H	H	Read	High-Z	—
L	L	H	Read	D_{out}	Read Cycle
L	X	L	Write	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	− 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	− 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	− 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	− 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
** V_{IL} (min) = − 0.5 V dc @ 30.0 mA; V_{IL} (min) = − 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = − 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6709R-6	MCM6709R-7	MCM6709R-8	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	195	190	185	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	85	80	75	mA
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} − 0.2 V, V_{in} ≤ V_{SS}, or ≥ V_{CC} − 0.2 V)	I_{SB2}	20	20	20	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
Input/Output Capacitance	$C_{I/O}$	6	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLES 1 AND 2 (See Notes 1 and 2)

Parameter	Symbol		MCM6709R-6		MCM6709R-7		MCM6709R-8		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	6	—	7	—	8	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	6	—	7	—	8	ns	
Chip Enable Access Time	t_{ELQV}	t_{ACS}	—	6	—	7	—	8	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	4	—	4	—	4	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	t_{LZ}	3	—	3	—	3	—	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	t_{LZ}	0	—	0	—	0	—	ns	4, 5, 6
Chip Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	3	0	3.5	0	4	ns	4, 5, 6
Output Enable High to Output High-Z	t_{GHQZ}	t_{HZ}	0	3	0	3.5	0	4	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. .All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.

AC TEST LOADS

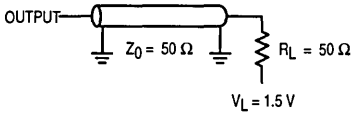


Figure 1A

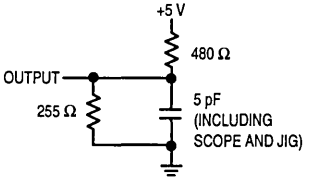
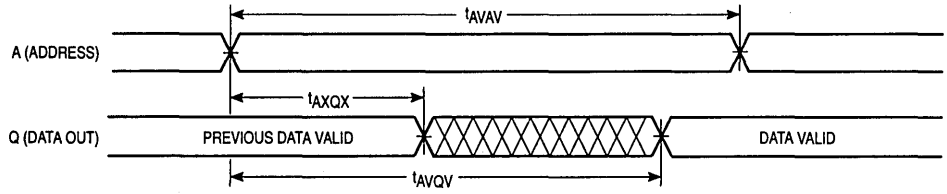


Figure 1B

TIMING LIMITS

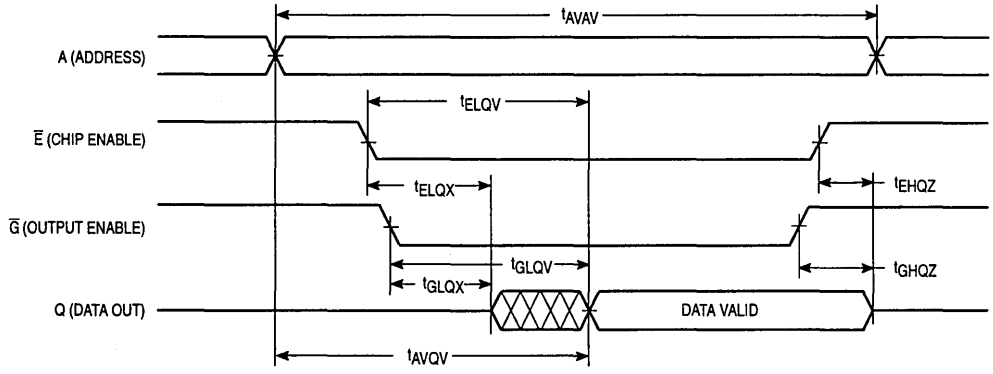
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note)



NOTE: Device is continuously selected ($\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$).

READ CYCLE 2 (See Note)



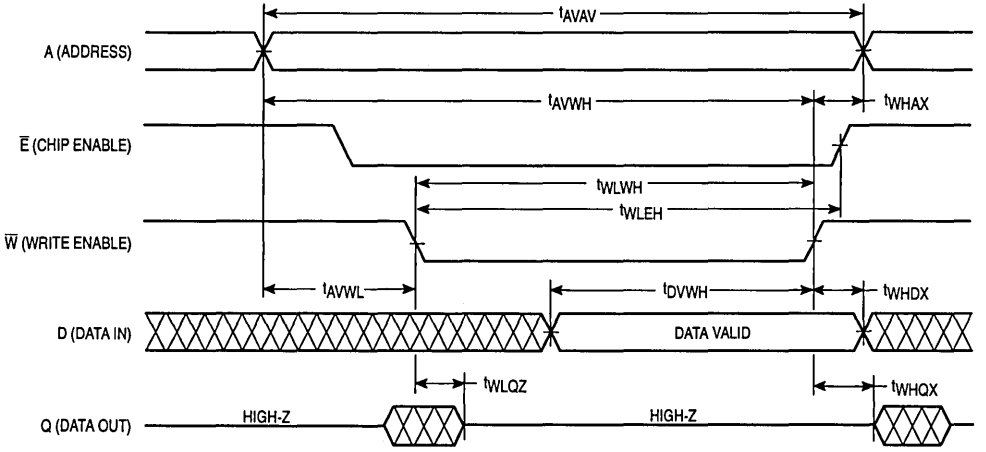
NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6709R-6		MCM6709R-7		MCM6709R-8		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	6	—	7	—	8	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	t_{WP}	6	—	7	—	8	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	3	—	3.5	—	4	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	3.5	0	3.5	0	4	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	t_{OW}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

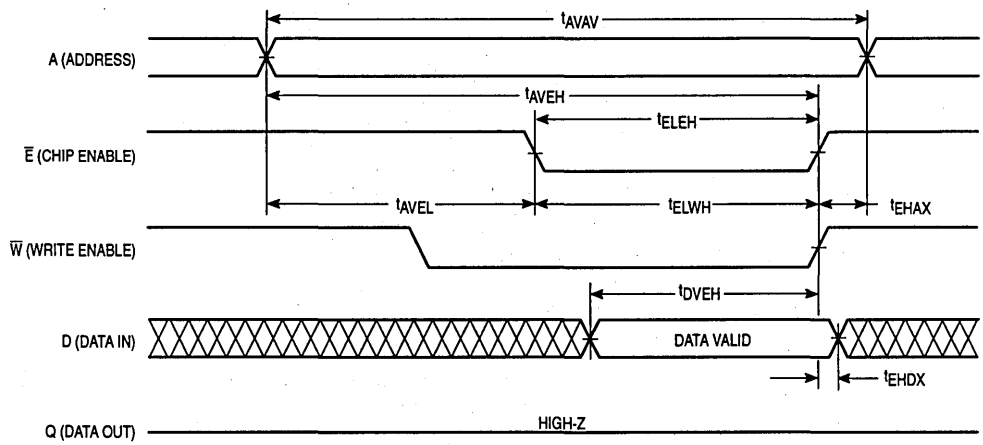


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6709R-6		MCM6709R-7		MCM6709R-8		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	6	—	7	—	8	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	6	—	7	—	8	—	ns	
Chip Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	5	—	6	—	7	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	t_{DW}	3	—	3.5	—	4	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6709R X XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (6 = 6 ns, 7 = 7 ns, 8 = 8 ns)
- Package (J = 300 mil SOJ)

Full Part Numbers — MCM6709RJ6, MCM6709RJ7, MCM6709RJ8, MCM6709RJ6R2, MCM6709RJ7R2, MCM6709RJ8R2

MCM6726

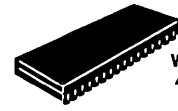
128K x 8 Bit Fast Static Random Access Memory

The MCM6726 is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. This device is fabricated using high performance silicon-gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small-outline J-leaded package.

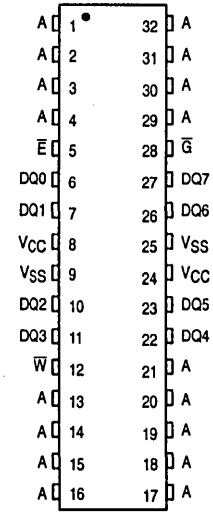
- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 10, 12, 15 ns
- Center Power and I/O Pins for Reduced Noise



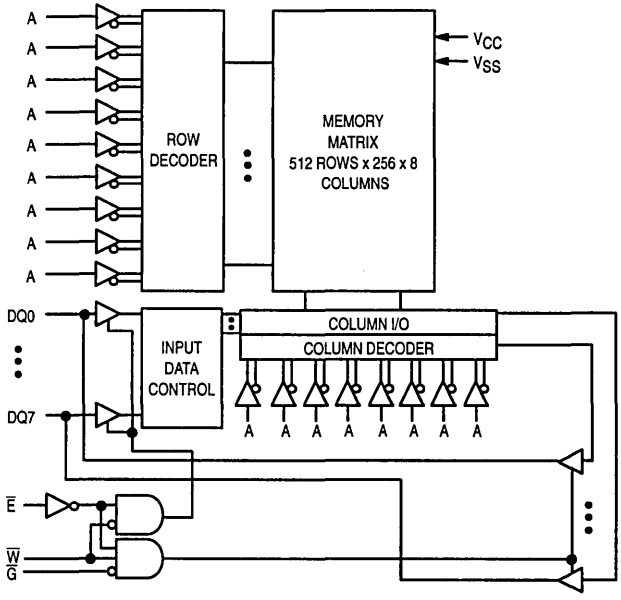
WJ PACKAGE
400 MIL SOJ
CASE 857A

2

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A16	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 – DQ7	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	Output Disabled	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	− 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias	T_{bias}	− 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	− 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	− 0.5*	—	0.8	V

* V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = − 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6726-10	MCM6726-12	MCM6726-15	Unit
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	175	165	155	mA
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	100	100	100	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	60	60	60	mA
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} − 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} − 0.2 V)	I_{SB2}	20	20	20	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		MCM6726-10		MCM6726-12		MCM6726-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	10	—	12	—	15	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	5	—	6	—	7	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	3	—	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	5	0	6	0	7	ns	4,5,6
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	5	0	6	0	7	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GHQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

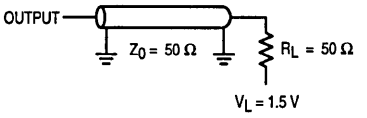


Figure 1A

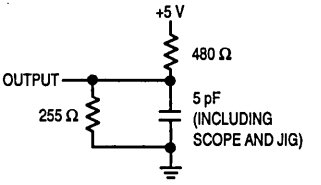
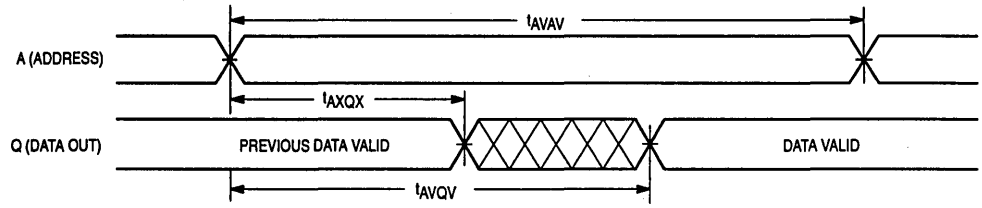


Figure 1B

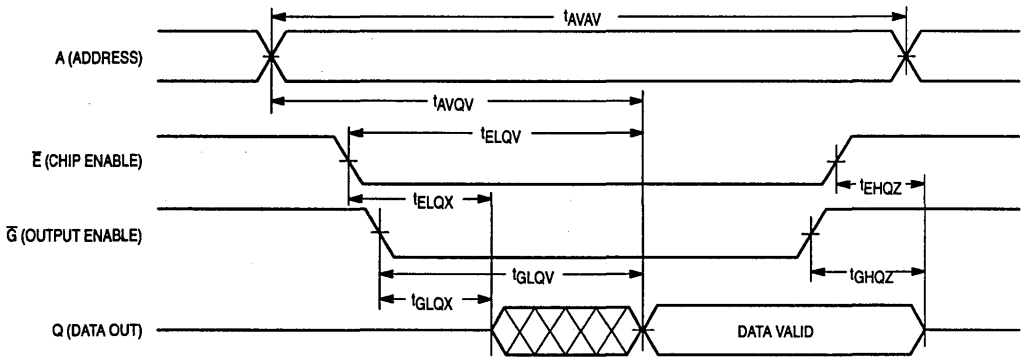
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)



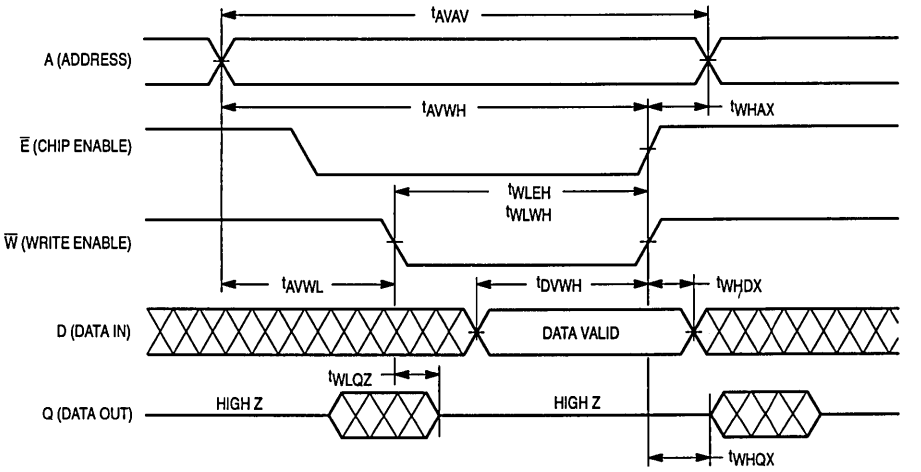
- Contention around Write access
- otherwise power issue.
- reads not a real issue.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6726-10		MCM6726-12		MCM6726-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	9	—	10	—	12	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	t_{AW}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	t_{WP} t_{WP}	9	—	10	—	12	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH} t_{WLEH}	t_{WP} t_{WP}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	5	0	6	0	7	ns	4,5,6
Write High to Output Active	t_{WHQX}	t_{OW}	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

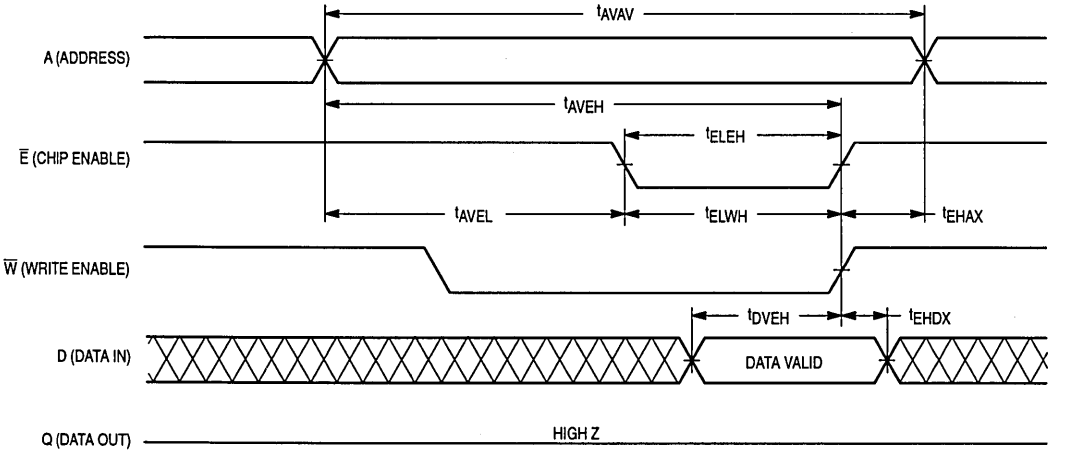


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

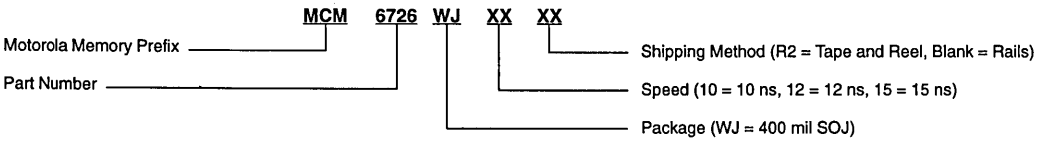
Parameter	Symbol		MCM6726-10		MCM6726-12		MCM6726-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	8	—	9	—	10	—	ns	
Enable to End of Write	t_{ELEH} t_{ELWH}	t_{CW} t_{CW}	8	—	9	—	10	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	t_{DW}	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

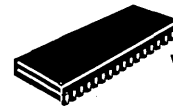


Full Part Numbers — MCM6726WJ10 MCM6726WJ12 MCM6726WJ15
MCM6726WJ10R2 MCM6726WJ12R2 MCM6726WJ15R2

MCM6726A

Product Preview

128K x 8 Bit Fast Static Random Access Memory



WJ PACKAGE
400 MIL SOJ
CASE 857A

The MCM6726A is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. This device is fabricated using high performance silicon-gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

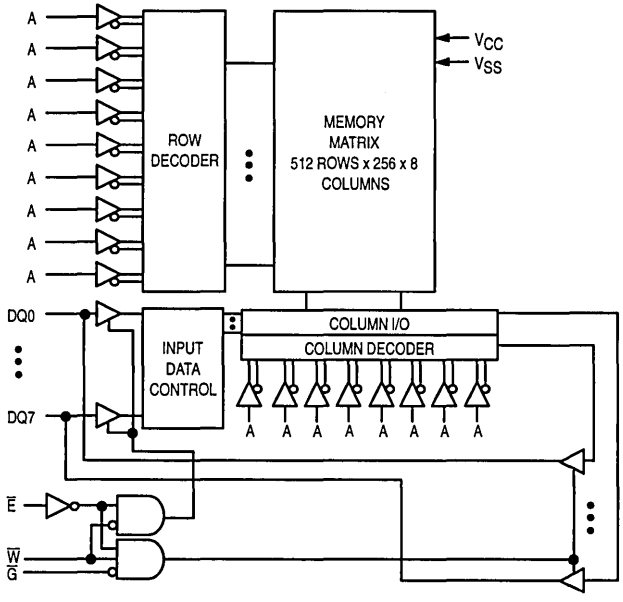
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small-outline J-leaded package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12, 15 ns
- Center Power and I/O Pins for Reduced Noise

PIN ASSIGNMENT

A	1	32	A
A	2	31	A
A	3	30	A
A	4	29	A
$\overline{E}$	5	28	$\overline{G}$
DQ0	6	27	DQ7
DQ1	7	26	DQ6
V_{CC}	8	25	V_{SS}
V_{SS}	9	24	V_{CC}
DQ2	10	23	DQ5
DQ3	11	22	DQ4
$\overline{W}$	12	21	A
A	13	20	A
A	14	19	A
A	15	18	A
A	16	17	A

BLOCK DIAGRAM



PIN NAMES

A0 – A16	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 – DQ7	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	Output Disabled	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = –0.5 V dc; V_{IL} (min) = –2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6726A-8	6726A-10	6726A-12	6726A-15	Unit
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	185	175	165	155	mA
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	100	100	100	100	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	60	60	60	60	mA
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	20	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		6726A-8		6726A-10		6726A-12		6726A-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	8	—	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	8	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	8	—	10	—	12	—	15	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	4	—	5	—	6	—	7	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	3	—	3	—	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	—	4	0	5	0	6	0	7	ns	4,5,6
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	—	4	0	5	0	6	0	7	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GHQX} min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

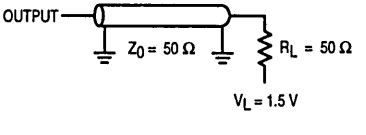


Figure 1A

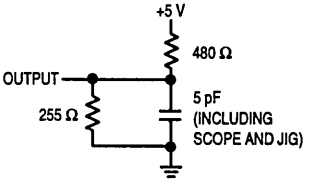


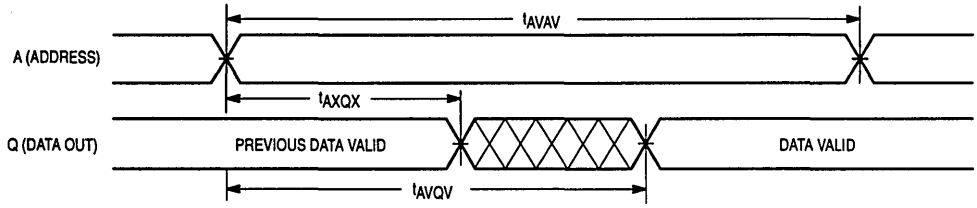
Figure 1B

TIMING LIMITS

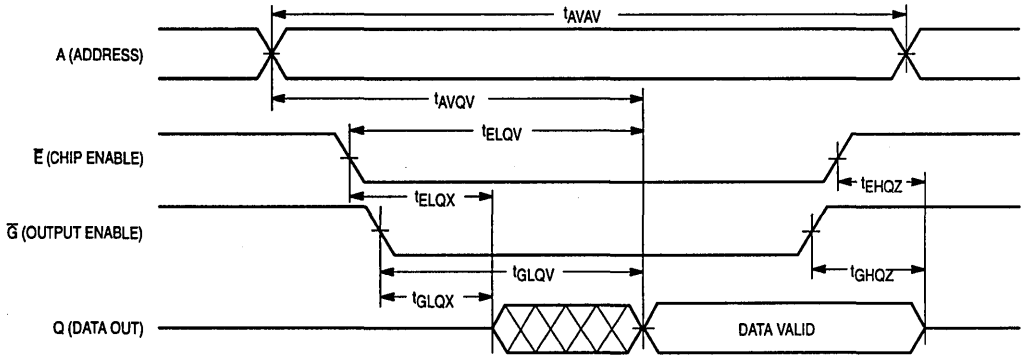
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

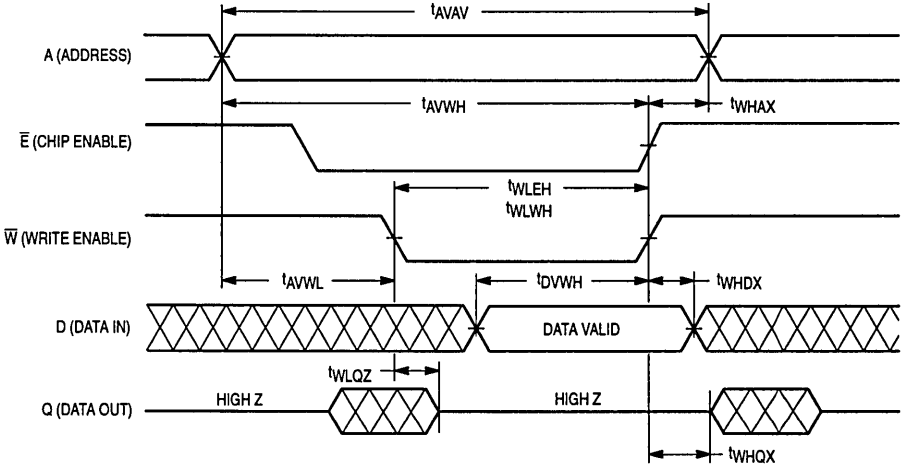


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		6726A-8		6726A-10		6726A-12		6726A-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	8	—	9	—	10	—	12	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	t_{AW}	7	—	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	t_{WP} t_{WP}	8	—	9	—	10	—	12	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH} t_{WLEH}	t_{WP} t_{WP}	7	—	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	4	0	5	0	6	0	7	ns	4,5,6
Write High to Output Active	t_{WHQX}	t_{OW}	3	—	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

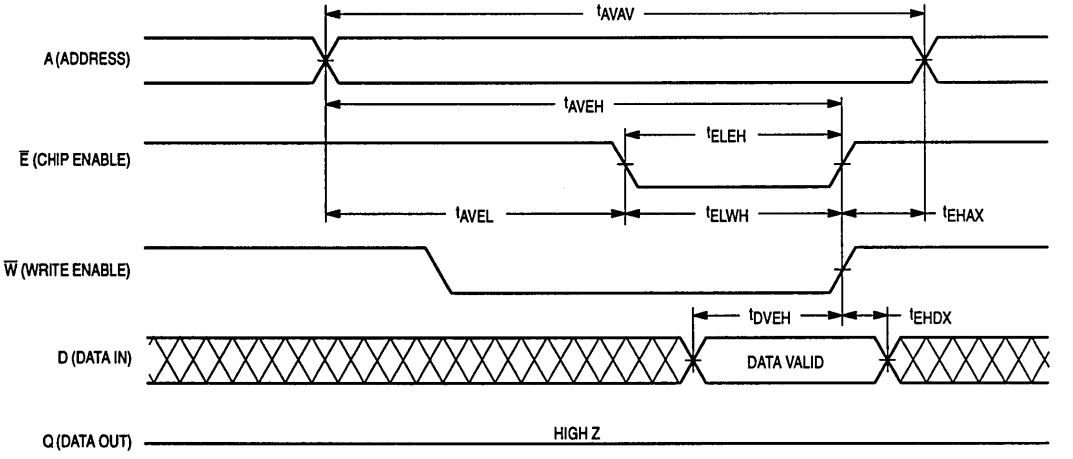


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		6726A-8		6726A-10		6726A-12		6726A-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	7	—	8	—	9	—	10	—	ns	
Enable to End of Write	t_{ELEH} t_{ELWH}	t_{CW} t_{CW}	7	—	8	—	9	—	10	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	t_{DW}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

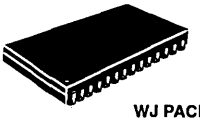
MCM 6726A WJ XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
- Package (WJ = 400 mil SOJ)

Full Part Numbers — MCM6726AWJ8 MCM6726AWJ10 MCM6726AWJ12 MCM6726AWJ15
MCM6726AWJ8R2 MCM6726AWJ10R2 MCM6726AWJ12R2 MCM6726AWJ15R2

MCM6728

256K x 4 Bit Fast Static Random Access Memory



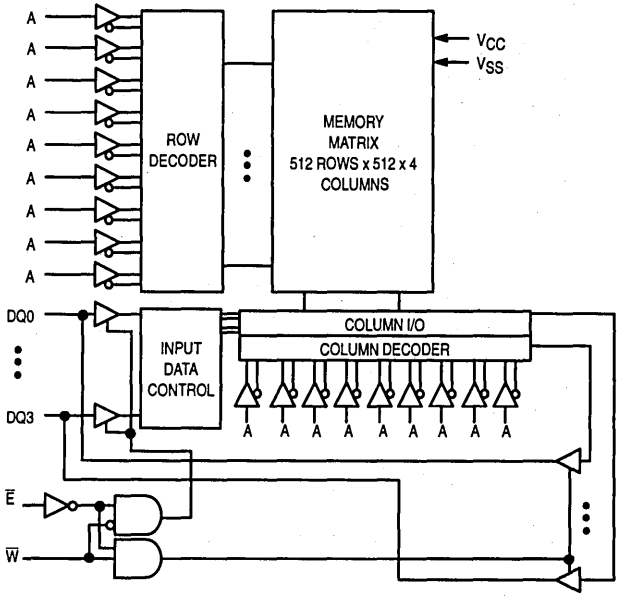
WJ PACKAGE
400 MIL SOJ
CASE 810

The MCM6728 is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits. This device is fabricated using high performance silicon-gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

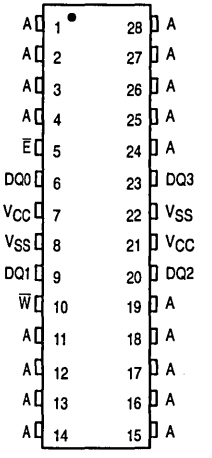
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small-outline J-leaded package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 10, 12, 15 ns
- Center Power and I/O Pins for Reduced Noise

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A17	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
DQ0 – DQ3	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	− 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	− 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature—Plastic	T_{stg}	− 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	− 0.5*	—	0.8	V

* V_{IL} (min) = − 0.5 V dc; V_{IL} (min) = − 2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = − 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6728-10	MCM6728-12	MCM6728-15	Unit
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	165	155	145	mA
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	90	90	90	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	60	60	60	mA
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} − 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} − 0.2 V)	I_{SB2}	20	20	20	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		MCM6728-10		MCM6728-12		MCM6728-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	10	—	12	—	15	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	3	—	3	—	3	—	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	5	0	6	0	7	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, for a given device.
5. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

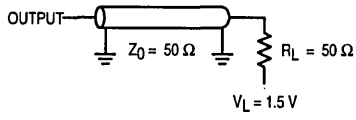


Figure 1A

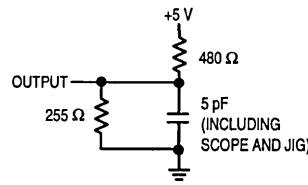
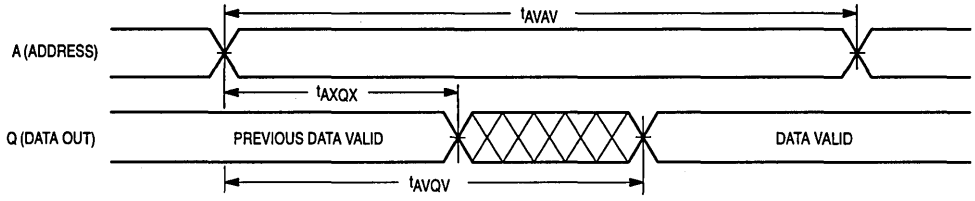


Figure 1B

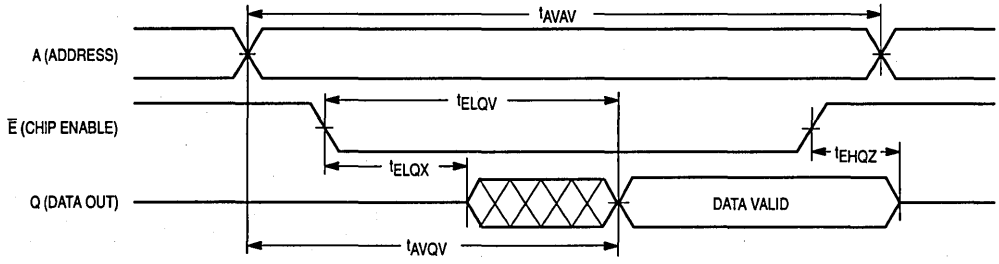
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

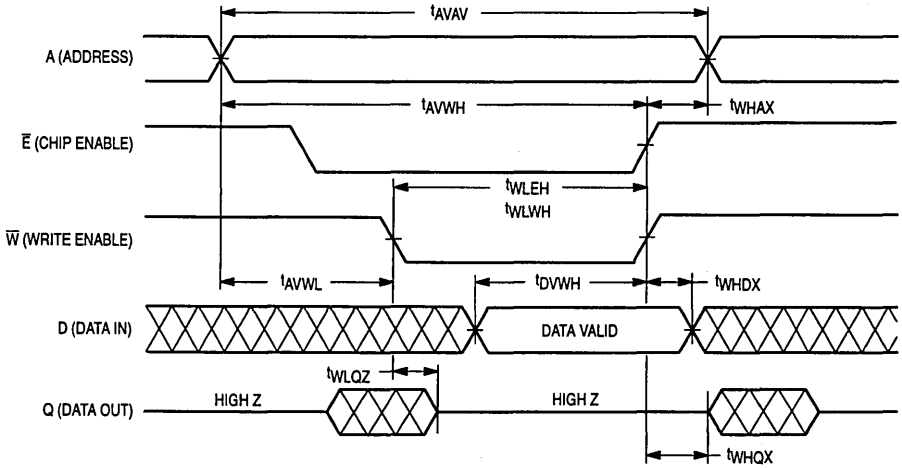


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6728-10		MCM6728-12		MCM6728-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	9	—	10	—	12	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	t_{WP} t_{WP}	9	—	10	—	12	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	5	0	6	0	7	ns	4,5,6
Write High to Output Active	t_{WHQX}	t_{OW}	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

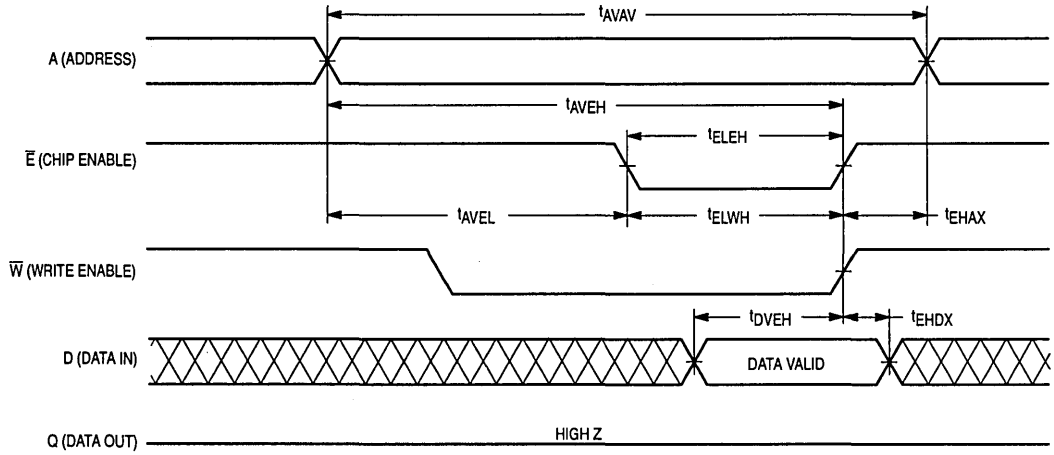


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

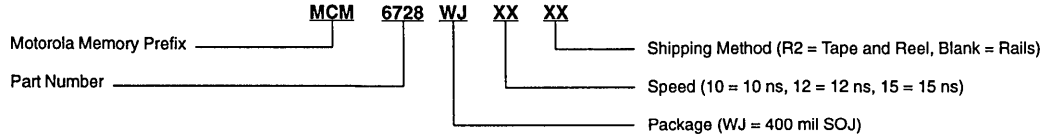
Parameter	Symbol		MCM6728-10		MCM6728-12		MCM6728-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	8	—	9	—	10	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	8	—	9	—	10	—	ns	4,5
Enable to End of Write	t_{ELWH}	t_{CW}	8	—	9	—	10	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	t_{DW}	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM6728WJ10 MCM6728WJ12 MCM6728WJ15
MCM6728WJ10R2 MCM6728WJ12R2 MCM6728WJ15R2

MCM6728A

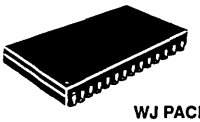
Product Preview

256K x 4 Bit Fast Static Random Access Memory

The MCM6728A is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits. This device is fabricated using high performance silicon-gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small-outline J-leaded package.

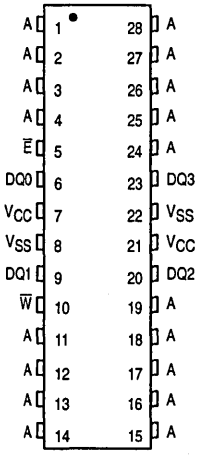
- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12, 15 ns
- Center Power and I/O Pins for Reduced Noise



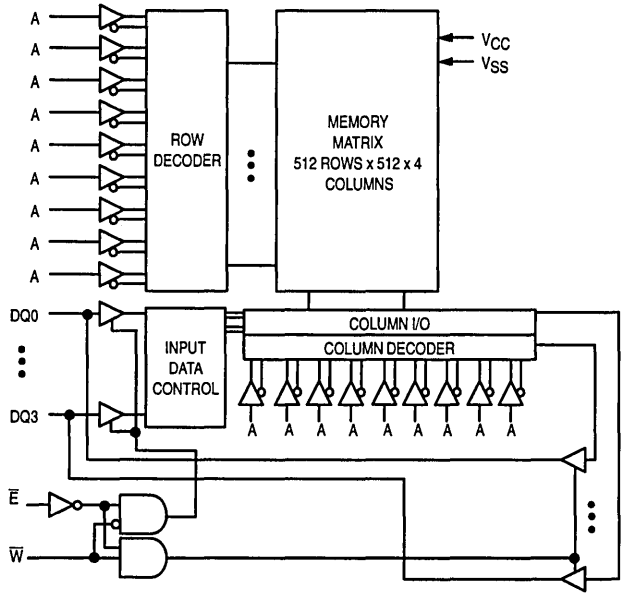
WJ PACKAGE
400 MIL SOJ
CASE 810

2

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A17	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
DQ0 – DQ3	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature—Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6728A-8	6728A-10	6728A-12	6728A-15	Unit
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	175	165	155	145	mA
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	90	90	90	90	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	60	60	60	60	mA
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	20	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		6728A-8		6728A-10		6728A-12		6728A-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	8	—	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	8	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	8	—	10	—	12	—	15	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	3	—	3	—	3	—	3	—	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	4	0	5	0	6	0	7	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, for a given device.
5. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

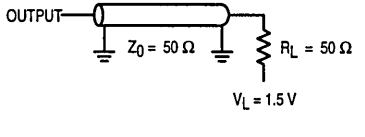


Figure 1A

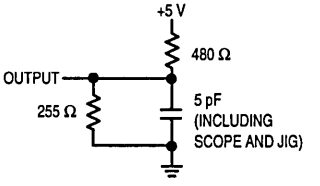


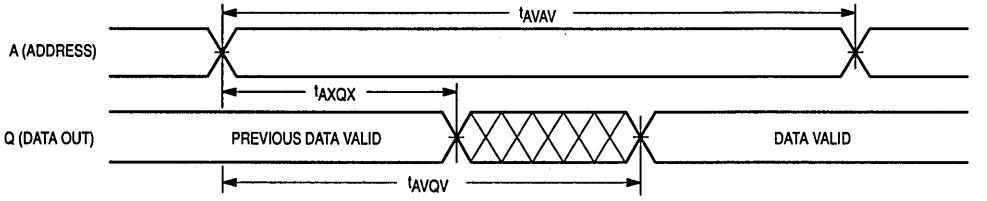
Figure 1B

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

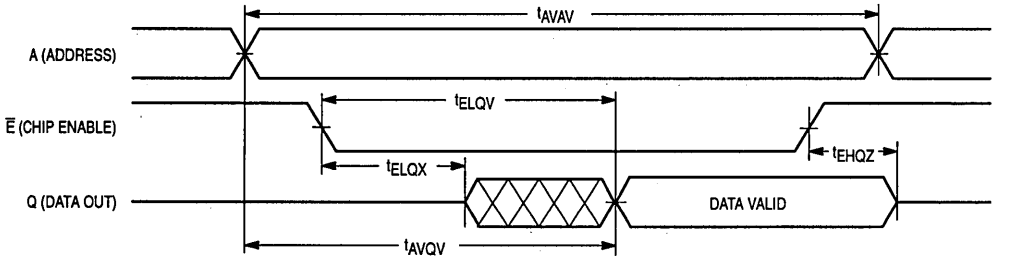
NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Note 7)



2

READ CYCLE 2 (See Note 8)

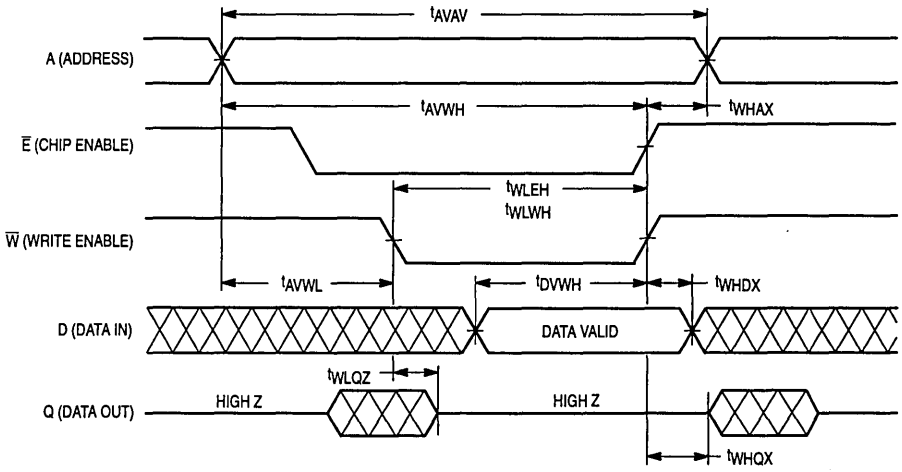


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		6728A-8		6728A-10		6728A-12		6728A-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	8	—	9	—	10	—	12	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	t_{WP} t_{WP}	8	—	9	—	10	—	12	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	4	0	5	0	6	0	7	ns	4,5,6
Write High to Output Active	t_{WHQX}	t_{OW}	3	—	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

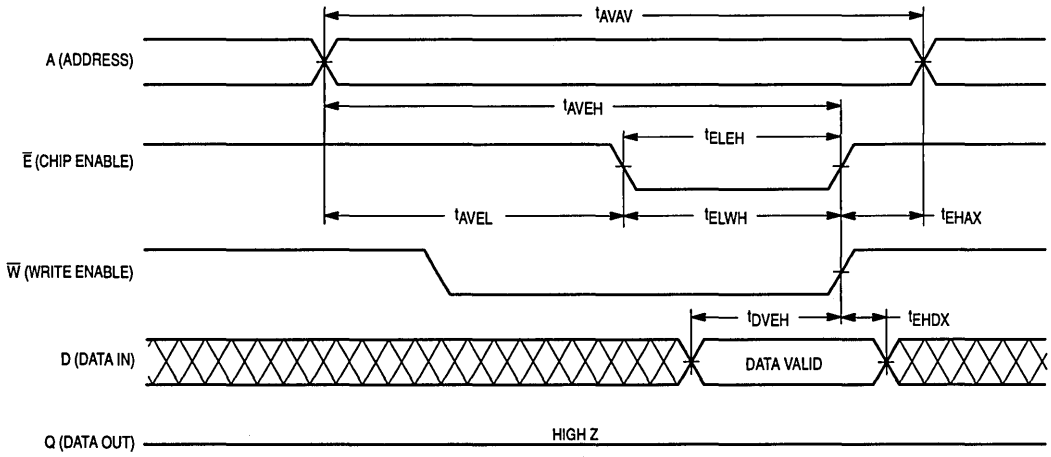


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		6728A-8		6728A-10		6728A-12		6728A-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	7	—	8	—	9	—	10	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	7	—	8	—	9	—	10	—	ns	4,5
Enable to End of Write	t_{ELWH}	t_{CW}	7	—	8	—	9	—	10	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	t_{DW}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6728A WJ XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
- Package (WJ = 400 mil SOJ)

Full Part Numbers — MCM6728AWJ8 MCM6728AWJ10 MCM6728AWJ12 MCM6728AWJ15
MCM6728AWJ8R2 MCM6728AWJ10R2 MCM6728AWJ12R2 MCM6728AWJ15R2

MCM6729

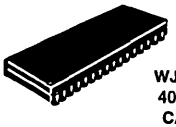
256K x 4 Bit Fast Static Random Access Memory

The MCM6729 is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits. This device is fabricated using high performance silicon-gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small-outline J-leaded package.

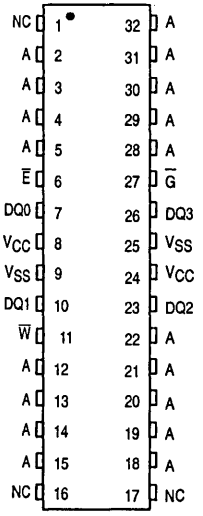
- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 10, 12, 15 ns
- Center Power and I/O Pins for Reduced Noise



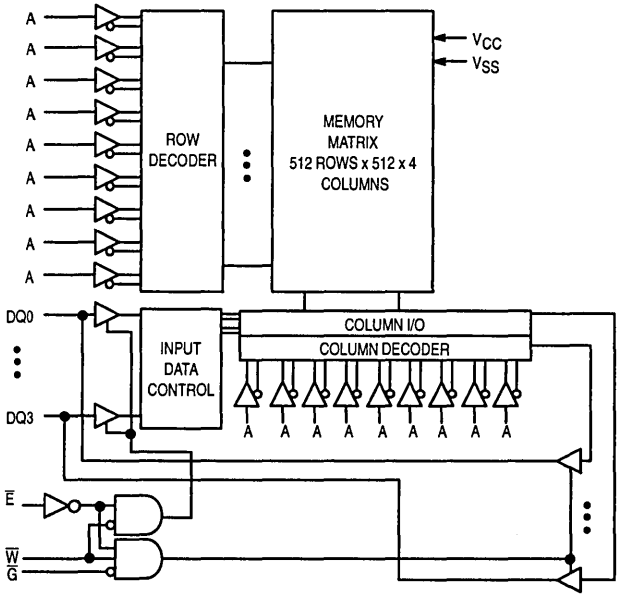
WJ PACKAGE
400 MIL SOJ
CASE 857A

2

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A17	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 – DQ3	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	Output Disabled	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	− 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	±30	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias	T_{bias}	− 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	− 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	− 0.5*	—	0.8	V

* V_{IL} (min) = − 0.5 V dc; V_{IL} (min) = − 2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = − 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6729-10	MCM6729-12	MCM6729-15	Unit
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	165	155	145	mA
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	90	90	90	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	60	60	60	mA
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} − 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} − 0.2 V)	I_{SB2}	20	20	20	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		MCM6729-10		MCM6729-12		MCM6729-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	10	—	12	—	15	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	5	—	6	—	7	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	3	—	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	5	0	6	0	7	ns	4,5,6
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	5	0	6	0	7	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} (max) < t_{ELQX} (min), and t_{GHQZ} (max) < t_{GHQX} (min), both for a given device and from device to device.
5. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

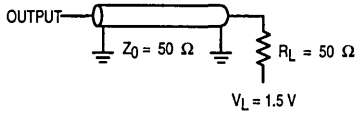


Figure 1A

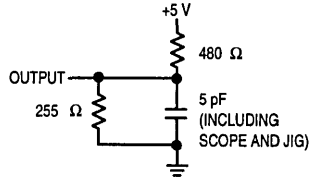
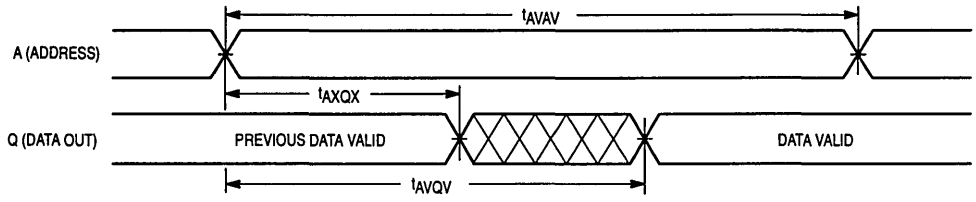


Figure 1B

TIMING LIMITS

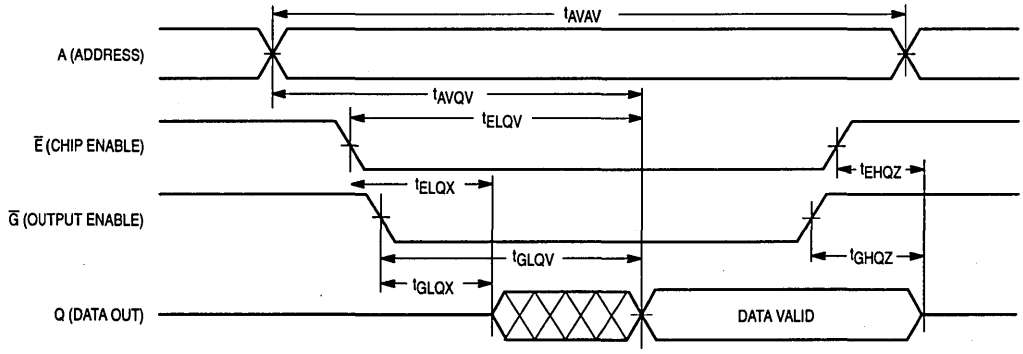
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



2

READ CYCLE 2 (See Note 8)

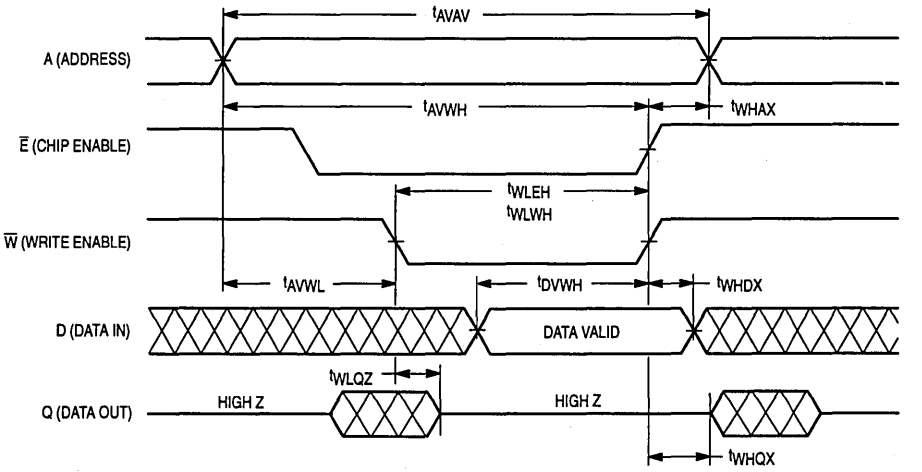


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6729-10		MCM6729-12		MCM6729-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	9	—	10	—	12	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	t_{AW}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	t_{WP} t_{WP}	9	—	10	—	12	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH} t_{WLEH}	t_{WP} t_{WP}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	5	0	6	0	7	ns	4,5,6
Write High to Output Active	t_{WHQX}	t_{OW}	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

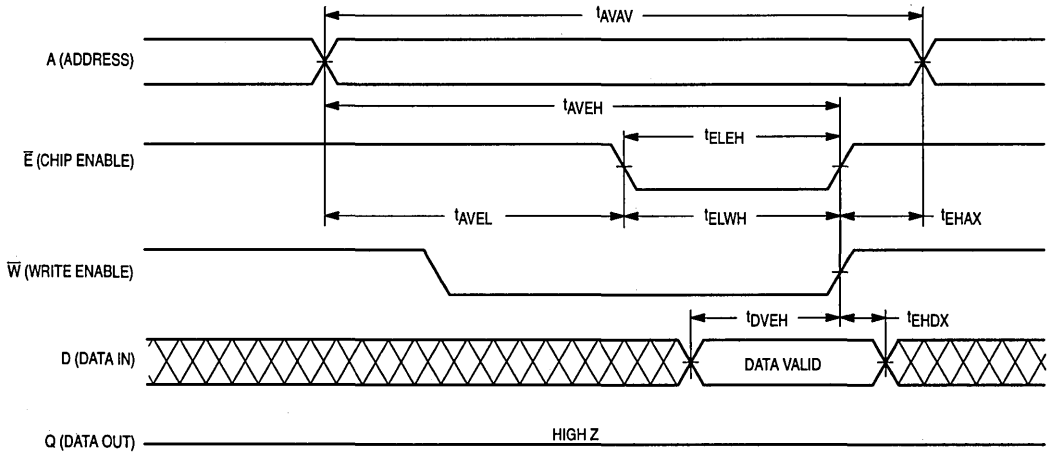


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6729-10		MCM6729-12		MCM6729-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	8	—	9	—	10	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	8	—	9	—	10	—	ns	4,5
Enable to End of Write	t_{ELWH}	t_{CW}	8	—	9	—	10	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	t_{DW}	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6729 WJ XX XX

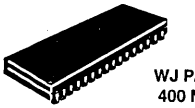
- MCM — Motorola Memory Prefix
- 6729 — Part Number
- XX — Speed (10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
- WJ — Package (WJ = 400 mil SOJ)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6729WJ10, MCM6729WJ10R2, MCM6729WJ12, MCM6729WJ12R2, MCM6729WJ15, MCM6729WJ15R2

MCM6729A

Product Preview

256K x 4 Bit Fast Static Random Access Memory



WJ PACKAGE
400 MIL SOJ
CASE 857A

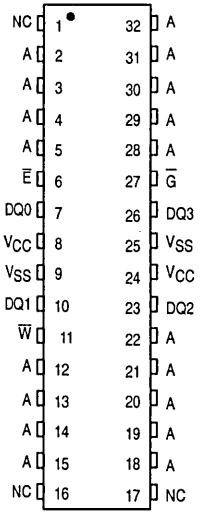
The MCM6729A is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits. This device is fabricated using high performance silicon-gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

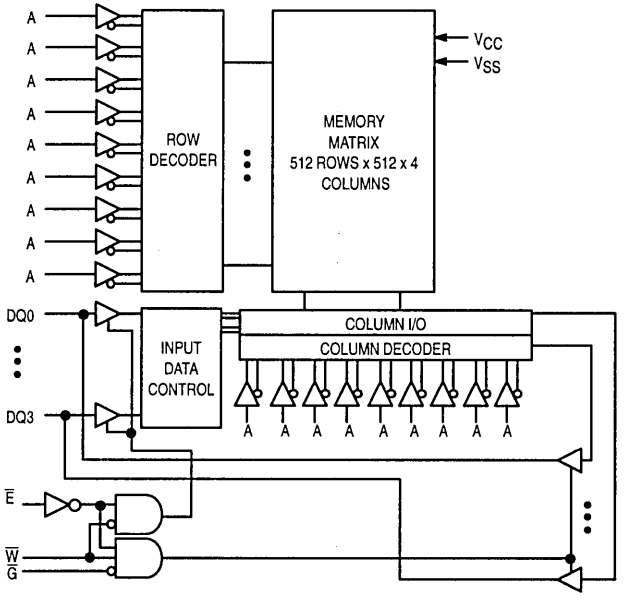
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small-outline J-leaded package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12, 15 ns
- Center Power and I/O Pins for Reduced Noise

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A17	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 – DQ3	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	Output Disabled	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	±30	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	6729A-8	6729A-10	6729A-12	6729A-15	Unit
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	175	165	155	145	mA
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	90	90	90	90	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	60	60	60	60	mA
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	20	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		6729A-8		6729A-10		6729A-12		6729A-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	8	—	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	8	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	8	—	10	—	12	—	15	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	4	—	5	—	6	—	7	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	3	—	3	—	3	—	3	—	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	4	0	5	0	6	0	7	ns	4,5,6
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	4	0	5	0	6	0	7	ns	4,5,6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} (max) < t_{ELQX} (min), and t_{GHQZ} (max) < t_{GHQX} (min), both for a given device and from device to device.
5. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

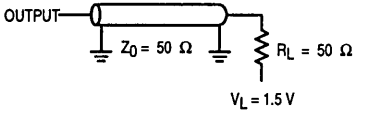


Figure 1A

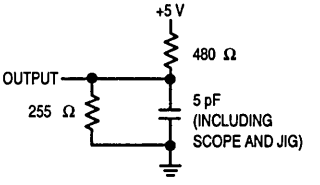


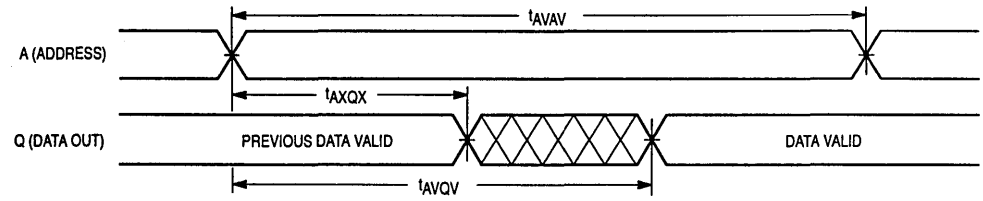
Figure 1B

TIMING LIMITS

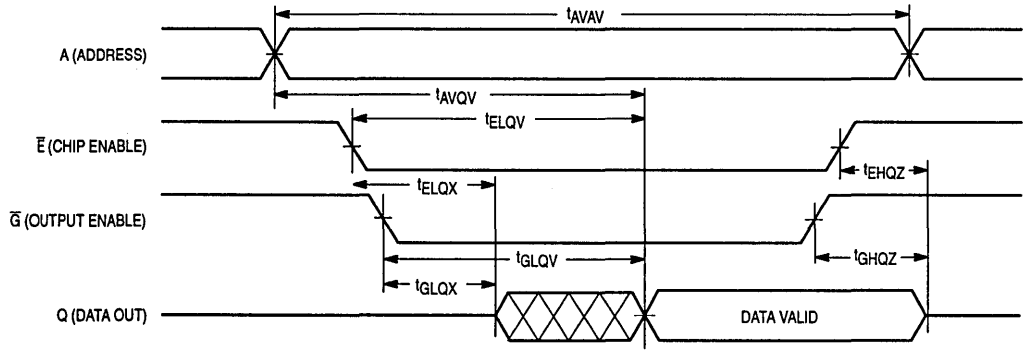
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

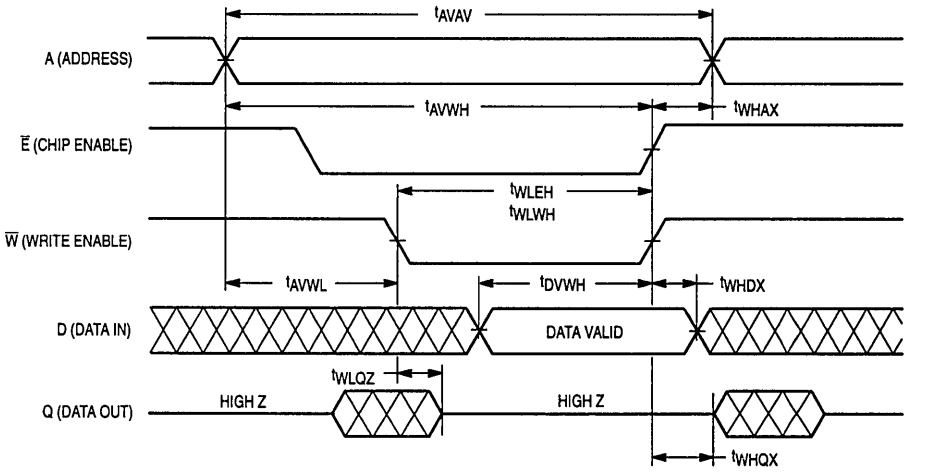


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		6729A-8		6729A-10		6729A-12		6729A-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	8	—	9	—	10	—	12	—	ns	
Address Valid to End of Write, $\overline{G}$ High	t_{AVWH}	t_{AW}	7	—	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	t_{WP} t_{WP}	8	—	9	—	10	—	12	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH} t_{WLEH}	t_{WP} t_{WP}	7	—	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	4	0	5	0	6	0	7	ns	4,5,6
Write High to Output Active	t_{WHQX}	t_{OW}	3	—	3	—	3	—	3	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

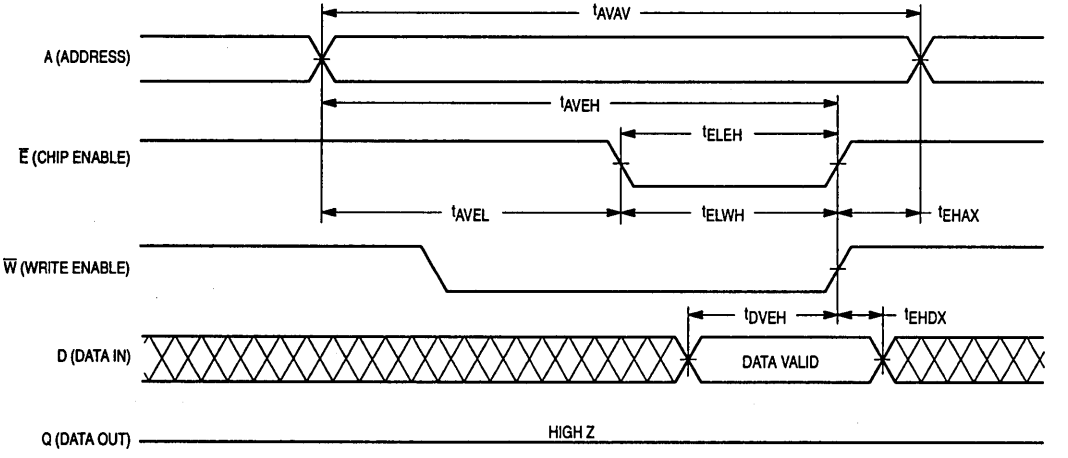


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		6729A-8		6729A-10		6729A-12		6729A-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	7	—	8	—	9	—	10	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	7	—	8	—	9	—	10	—	ns	4,5
Enable to End of Write	t_{ELWH}	t_{CW}	7	—	8	—	9	—	10	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	t_{DW}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6729A WJ XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
- Package (WJ = 400 mil SOJ)

Full Part Numbers — MCM6729AWJ8 MCM6729AWJ10 MCM6729AWJ12 MCM6729AWJ15
MCM6729AWJ8R2 MCM6729AWJ10R2 MCM6729AWJ12R2 MCM6729AWJ15R2

MCM101520

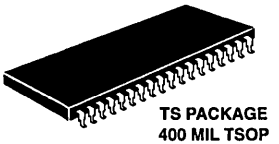
Product Preview

4M x 1 Bit Fast Static Random Access Memory with ECL I/O

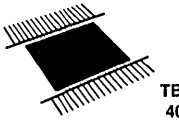
The MCM101520 is a 4,194,304 bit static random access memory organized as 4,194,304 words of 1 bit. This circuit is fabricated using high performance silicon-gate BiCMOS technology. Asynchronous design eliminates the need for external clocks or timing strobes. This device operates across a supply voltage range of – 4.94 V to – 5.46 V. Inputs and outputs are voltage and temperature 100K ECL compensated.

The MCM101520 meets JEDEC standards for functionality and revolutionary pin-out. It is available in 400 mil, 36 lead surface mount TSOP package as well as 36 lead TAB.

- Fast Access Times: 10, 12, 15 ns
- Equal Address and Chip Select Access Time
- Power Operation – 205 mA Maximum Active AC

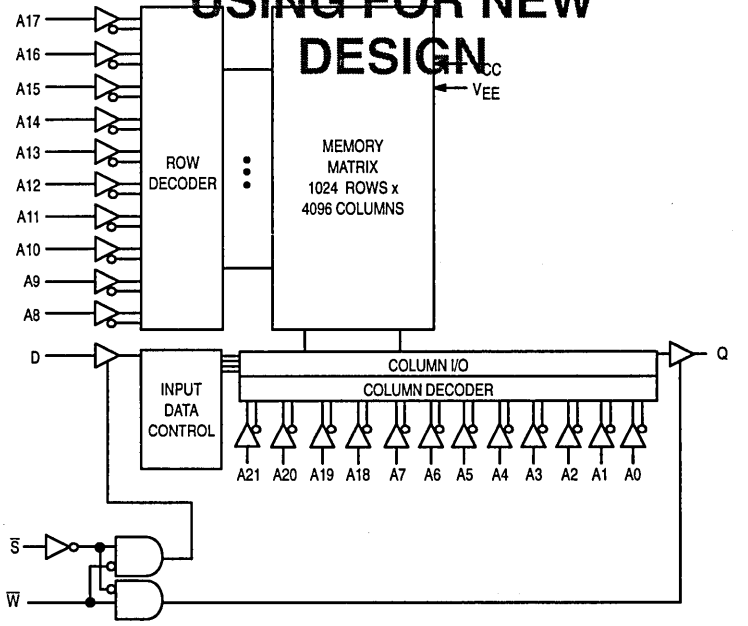


TS PACKAGE
400 MIL TSOP
CASE TBD

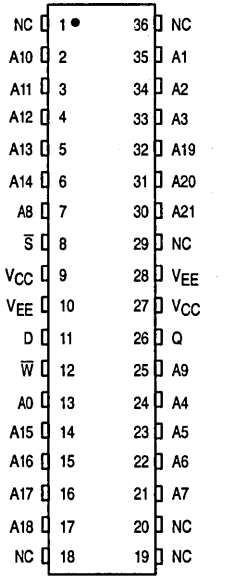


TB PACKAGE
400 MIL TAB
CASE TBD

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0 – A21 ..... Address Inputs	W ..... Write Enable
S ..... Chip Select	D ..... Data Input
Q ..... Data Output	NC ..... No Connection
VEE ..... Power Supply	VCC ..... Ground

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE (X = Don't Care)

$\overline{S}$	$\overline{W}$	Data	Current	Output	Cycle
H	X	X	I_{EE}	L	Not Enabled
L	H	X	I_{EE}	Q	Read Cycle
L	L	X	I_{EE}	L	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential (to Ground)	V_{EE}	−7.0 to +0.5	V
Voltage Relative to V_{CC} for Any Pin Except V_{EE}	V_{in}, V_{out}	V_{EE} −0.5 to +0.5	V
Output Current (per I/O)	I_{out}	−50	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	−30 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature — Plastic	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = −5.2 V ±5%, T_A = 0 to +70°C, Unless Otherwise Noted)

DC OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{EE}	−5.46	−5.2	−4.94	V
Input High Voltage	V_{IH}	−1165	—	−880	mV
Input Low Voltage	V_{IL}	−1810	—	−1475	mV
Output High Voltage	V_{OH}	−1025	—	−880	mV
Output Low Voltage	V_{OL}	−1810	—	−1620	mV
Output High Corner Voltage	V_{OHC}	−1035	—	—	mV
Output Low Corner Voltage	V_{OLC}	—	—	−1610	mV
Input Low Current	I_{IL}	−50	—	—	µA
Input High Current	I_{IH}	—	—	220	µA
Chip Select Input Low Current	$I_{IL(CS)}$	0.5	—	170	µA
Operating Power Supply Current (AVAV = 20 ns, All Outputs Open)	I_{EE}	—	—	−195	mA
Quiescent Power Supply Current (f_o = 0 MHz (All Inputs and Outputs Open)	I_{EEQ}	—	—	−150	mA
Voltage Compensation (V_{OH})	$\Delta V_{OH}/\Delta V_{EE}$	±35 mV/V @ −4.94 to −5.46			
Voltage Compensation (V_{OL})	$\Delta V_{OL}/\Delta V_{EE}$	±60 mV/V @ −4.94 to −5.46			

RISE/FALL TIME REQUIREMENTS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Rise Time	t_r	20% to 80%	0.5	1.0	1.5	ns
Output Fall Time	t_f	20% to 80%	0.5	1.0	1.5	ns

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	Address and Data	C_{in}	3.5	7	pF
	$\overline{S}$, $\overline{W}$	C_{ck}	4	7	
Output Capacitance	Q	C_{out}	4	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{EE} = – 5.2 V ± 5%, V_{CC} = 0 V, T_A = 0 to +70°C, Unless Otherwise Noted)

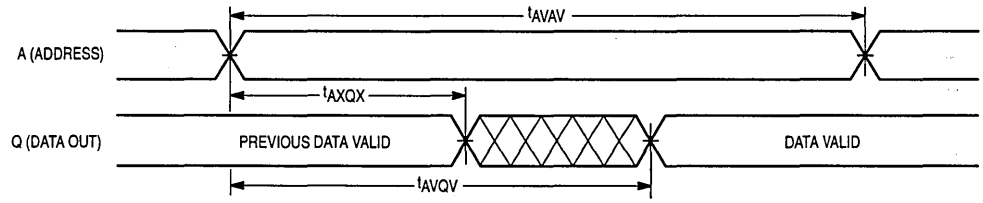
Input Pulse Levels ..... – 1.7 V to – 0.9 V (See Figure 1)
Input Rise/Fall Time ..... 1 ns
Input Timing Measurement Reference Level 50%
Output Timing Measurement Reference Level .. V_{OH} = – 1165 mV
..... V_{OL} = – 1475 mV
Output Load (AC Test Circuit) ..... See Figure 2

READ CYCLE TIMING (See Notes 1 and 2)

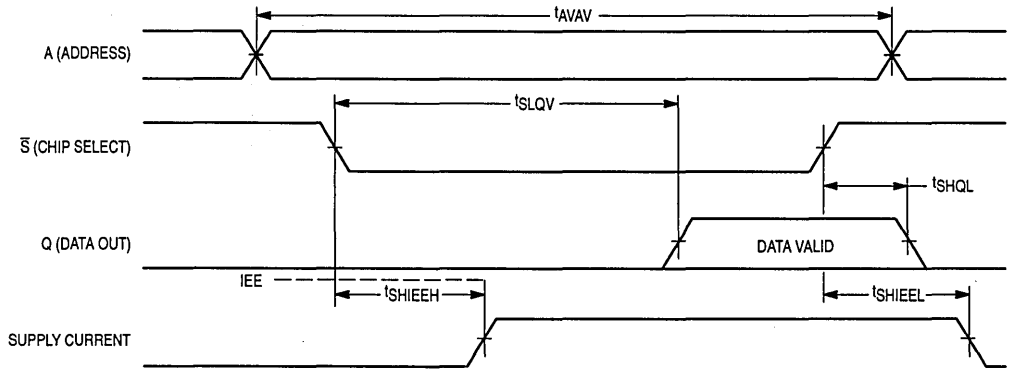
Parameter	Symbol		MCM101520-10		MCM101520-12		MCM101520-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	10	—	12	—	15	—	ns	2, 3
Address Access Time	t_{AVQV}	t_{AA}	—	10	—	12	—	15	ns	
Chip Select Access Time	t_{SLQV}	t_{ACS}	—	10	—	12	—	15	ns	6
Select High to Output Low	t_{SHQL}	t_{RCS}	0	7	0	8	0	9	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	ns	
Power Up Time	t_{SLIEEH}	t_{PU}	0	—	0	—	0	—	ns	4
Power Down Time	t_{SHIEEL}	t_{PD}	—	10	—	12	—	15	ns	4

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. This parameter is sampled and not 100% tested.
5. Device is continuously selected ($\overline{S} \le V_{IL}$).
6. Addresses valid prior to or coincident with $\overline{S}$ going low.

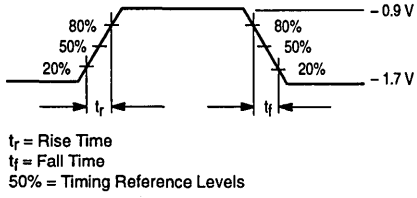
READ CYCLE 1 (See Notes 1, 2, and 5)



READ CYCLE 2 (See Note 6)

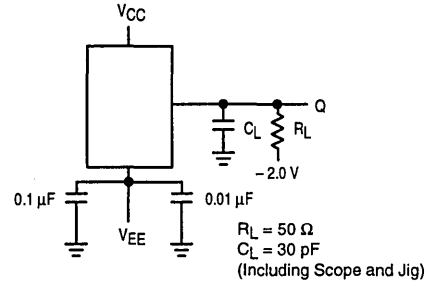


AC TEST CONDITIONS



t_r = Rise Time
t_f = Fall Time
50% = Timing Reference Levels

Figure 1. Input Levels



R_L = 50 Ω
C_L = 30 pF
(Including Scope and Jig)

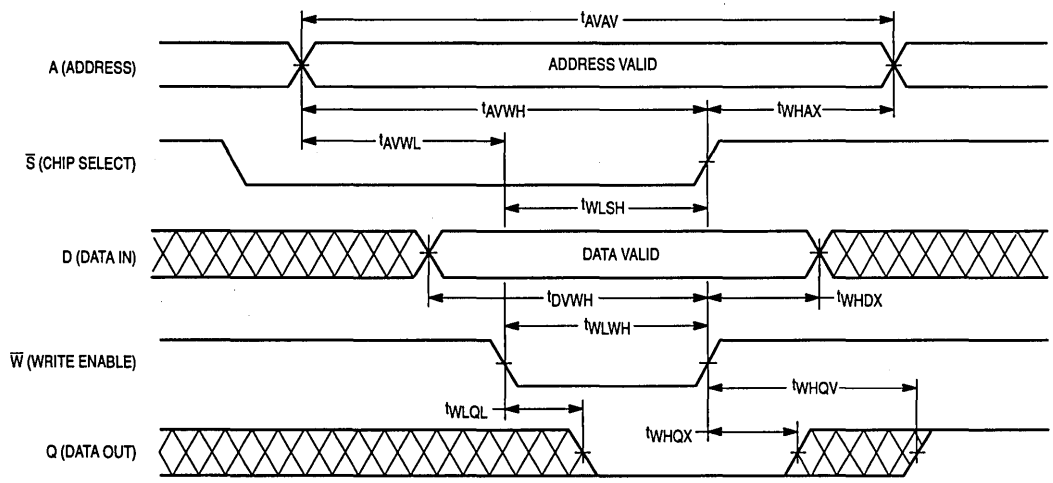
Figure 2. AC Test Circuit

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM101520-10		MCM101520-12		MCM101520-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	1	—	1	—	1	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	7	—	8	—	9	—	ns	
Write Pulse Width	t_{WLWH} t_{WLSH}	t_{WP}	7	—	8	—	9	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	7	—	8	—	9	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	1	—	1	—	1	—	ns	
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	ns	4
Write High to Output Valid	t_{WHQV}	t_{AW}	—	11	—	13	—	16	ns	
Write Recovery Time	t_{WHAX}	t_{WR}	1	—	1	—	1	—	ns	
Write Low to Output Low	t_{WLQL}	t_{WS}	0	7	0	8	0	9	ns	

NOTES:
1. A write occurs during the overlap of $\overline{S}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

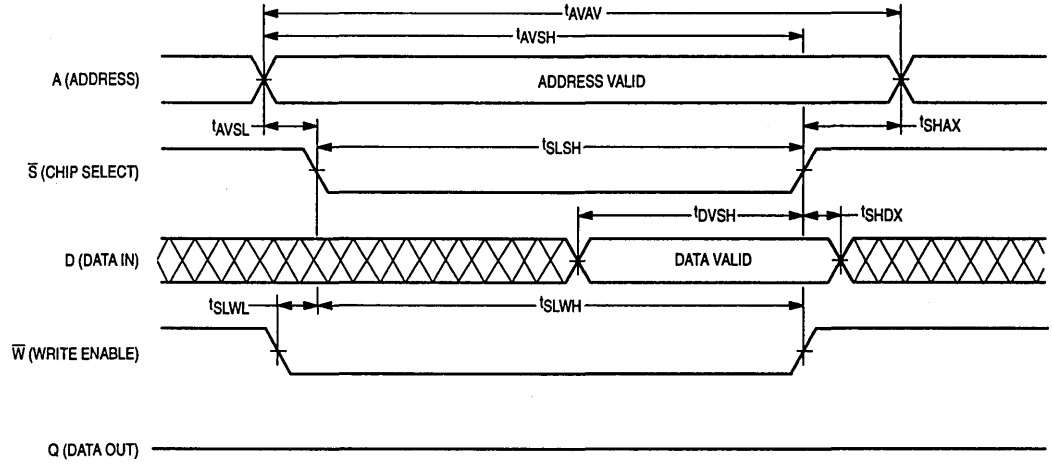


WRITE CYCLE 2 ($\overline{S}$ Controlled, See Notes 1 and 2)

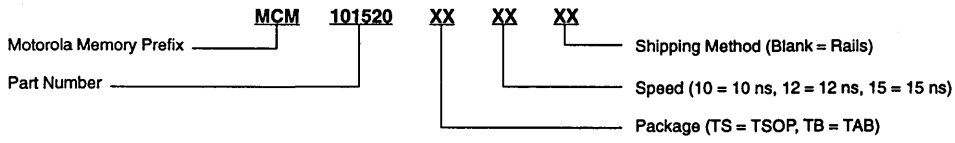
Parameter	Symbol		MCM101520-10		MCM101520-12		MCM101520-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVSL}	t_{AS}	1	—	1	—	1	—	ns	
Address Valid to End of Write	t_{AVSH}	t_{AW}	7	—	8	—	9	—	ns	
Write Pulse Width	t_{SLSH} t_{SLWH}	t_{CW}	7	—	8	—	9	—	ns	
Data Valid to End of Write	t_{DVSH}	t_{DW}	7	—	8	—	9	—	ns	
Chip Select Set-Up Time	t_{SLWL}	t_{CS}	0	—	0	—	0	—	ns	
Data Hold Time	t_{SHDX}	t_{DH}	1	—	1	—	1	—	ns	
Write Recovery Time	t_{SHAX}	t_{WR}	1	—	1	—	1	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{S}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.

WRITE CYCLE 2 ($\overline{S}$ Controlled, See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)

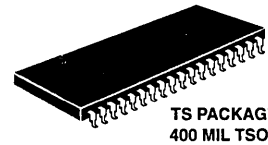


Full Part Numbers — MCM101520TS10 MCM101520TB10
MCM101520TS12 MCM101520TB12
MCM101520TS15 MCM101520TB15

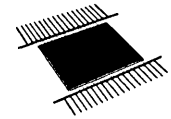
Product Preview

MCM101524

1M x 4 / 2M x 2 Bit Fast Static Random Access Memory with ECL I/O



TS PACKAGE
400 MIL TSOP
CASE TBD



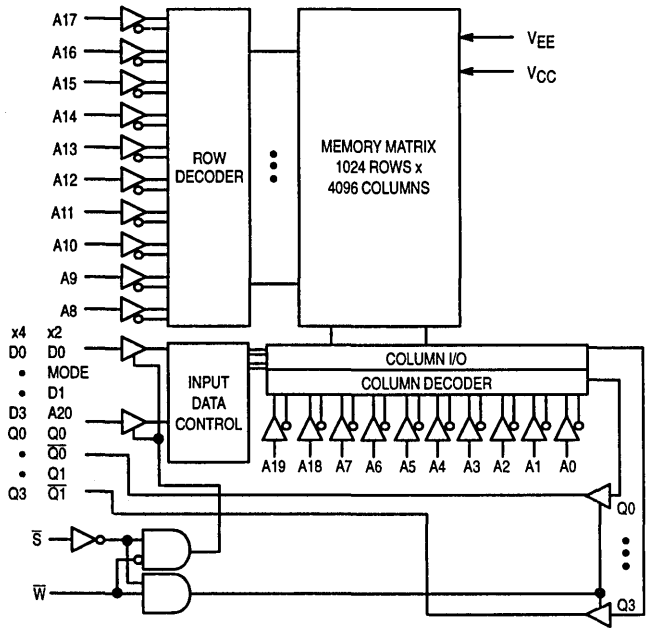
TB PACKAGE
400 MIL TAB
CASE TBD

The MCM101524 is a 4,194,304 bit static random access memory that can be electrically reconfigured as 1,048,576 words of 4 bits or 2,097,152 words of 2 bits. The 2M x 2 operation is achieved by applying V_{EE} voltage to the D1/Mode select pin. The 1M x 4 option features separate data inputs and outputs. The 2M x 2 mode features complimentary outputs. This circuit is fabricated using high performance silicon-gate BiCMOS technology. Asynchronous design eliminates the need for external clocks or timing strobes.

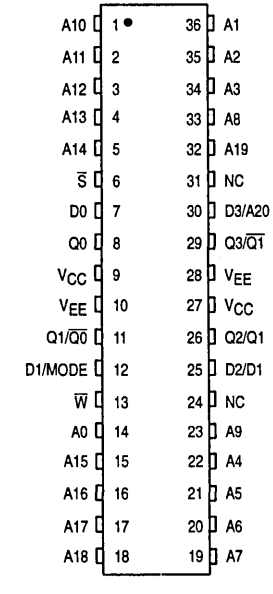
The MCM101524 is available in a 400 mil, 36 lead surface-mount TSOP package as well as 36 lead TAB.

- Fast Access Times: 10, 12, 15 ns
- Equal Address and Chip Select Access Time
- Power Operation: – 200 mA Maximum, Active AC

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0 – A20 ..... Address Inputs	W ..... Write Enable
S ..... Chip Select	D0 – D3 ..... Data Input
Q0 – Q3 ..... Data Output	Q0 and Q1 ..... Data Output
NC ..... No Connection	VEE ..... Power Supply
VCC ..... Ground	Mode .. Reconfigures for x2 Operation

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE (X = Don't Care)

$\overline{S}$	$\overline{W}$	Mode	Config	Operation	Data	Output	Current
H	X	X	X	Not Enabled	X	L	—
L	H	H/L	x4	Read	X	Q	I_{EE}
L	L	H/L	x4	Write	X	L	I_{EE}
L	H	V_{EE}	x2	Read	X	Q	I_{EE}
L	L	V_{EE}	x2	Write	X	L	I_{EE}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential (to Ground)	V_{EE}	− 7.0 to + 0.5	V
Voltage Relative to V_{CC} for Any Pin Except V_{EE}	V_{in}, V_{out}	V_{EE} − 0.5 to + 0.5	V
Output Current (per I/O)	I_{out}	− 50	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	− 30 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	− 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = − 5.2 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

DC OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{EE}	− 5.46	− 5.2	− 4.94	V
Input High Voltage	V_{IH}	− 1165	—	− 880	mV
Input Low Voltage	V_{IL}	− 1810	—	− 1475	mV
Mode Select for 2Meg x 2 Configuration	V_{M1}	V_{EE}	V_{EE}	V_{EE} + 0.5	V
Mode Select for 1Meg x 4 Configuration	V_{M2}	V_{EE} + 1.5	V_{IL}/V_{IH}	− 0.88	V
Output High Voltage	V_{OH}	− 1025	—	− 880	mV
Output Low Voltage	V_{OL}	− 1810	—	− 1620	mV
Input Low Current	I_{IL}	− 50	—	—	µA
Input High Current	I_{IH}	—	—	220	µA
Chip Select Input Low Current	$I_{IL(CS)}$	0.5	—	170	µA
Operating Power Supply Current: AVAV = 20 ns (All Outputs Open)	I_{EE}	—	—	− 195	mA
Quiescent Power Supply Current: f_O = 0 MHz (All Inputs and Outputs Open)	I_{EEQ}	—	—	− 150	mA
Voltage Compensation (V_{OH})	$\Delta V_{OH}/\Delta V_{EE}$	± 35 mV/V @ − 4.94 to − 5.46			
Voltage Compensation (V_{OL})	$\Delta V_{OL}/\Delta V_{EE}$	± 60 mV/V @ − 4.94 to − 5.46			

RISE/FALL TIME REQUIREMENTS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Rise Time	t_r	20% to 80%	0.5	1.0	1.5	ns
Output Fall Time	t_f	20% to 80%	0.5	1.0	1.5	ns

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	Address and Data	C_{in}	3.5	7	pF
	$\overline{S}$, $\overline{W}$	C_{ck}	4	7	
Output Capacitance	Q	C_{out}	4	8	pF

2

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{EE} = – 5.2 V ± 5%, V_{CC} = 0 V, T_A = 0 to +70°C, Unless Otherwise Noted)

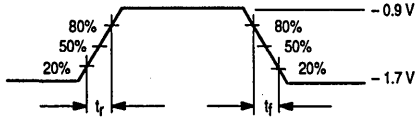
Input Pulse Levels ..... – 1.7 V to – 0.9 V (See Figure 1)
Input Rise/Fall Time ..... 1 ns
Input Timing Measurement Reference Level 50%
Output Timing Measurement Reference Level .. V_{OH} = – 1165 mV
V_{OL} = – 1475 mV
Output Load (AC Test Circuit) ..... See Figure 2

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		MCM101524-10		MCM101524-12		MCM101524-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	10	—	12	—	15	—	ns	2, 3
Address Access Time	t_{AVQV}	t_{AA}	—	10	—	12	—	15	ns	
Chip Select Access Time	t_{SLQV}	t_{ACS}	—	10	—	12	—	15	ns	6
Select High to Output Low	t_{SHQL}	t_{RCS}	0	7	0	8	0	9	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	ns	
Power Up Time	t_{SLIEEH}	t_{PU}	0	—	0	—	0	—	ns	4
Power Down Time	t_{SHIEEL}	t_{PD}	—	10	—	12	—	15	ns	4

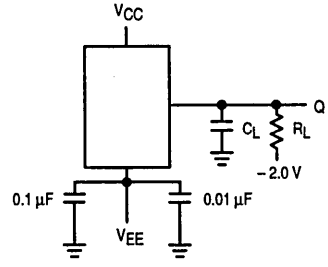
NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. This parameter is sampled and not 100% tested.
5. Device is continuously selected ($\overline{S} \leq V_{IL}$).
6. Addresses valid prior to or coincident with $\overline{S}$ going low.

AC TEST CONDITIONS



t_r = Rise Time
t_f = Fall Time
50% = Timing Reference Levels

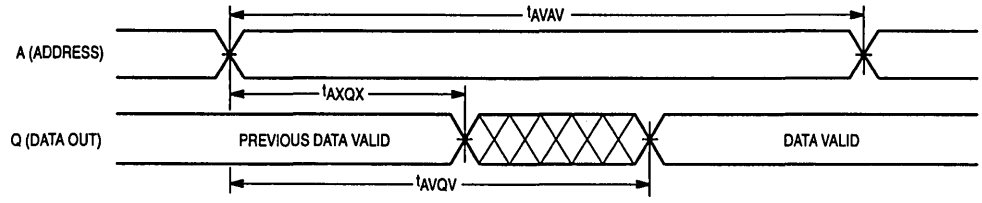
Figure 1. Input Levels



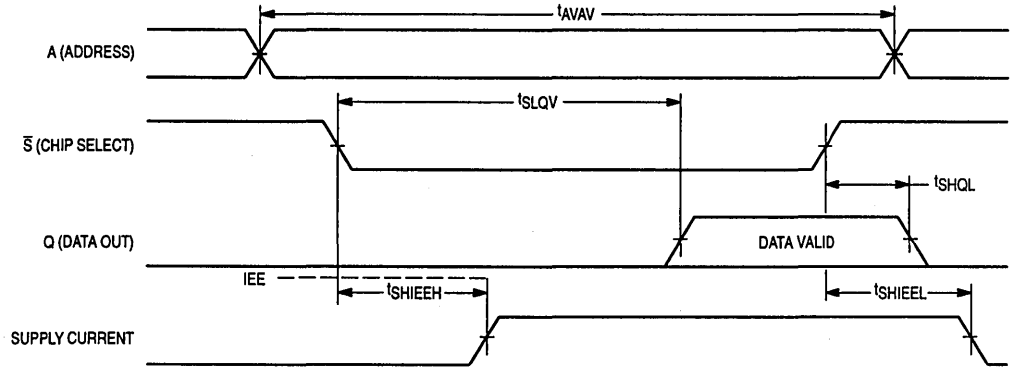
R_L = 50 Ω
C_L = 30 pF (Including Scope and Jig)

Figure 2. AC Test Circuit

READ CYCLE 1 (See Notes 1, 2, and 5)



READ CYCLE 2 (See Note 6)

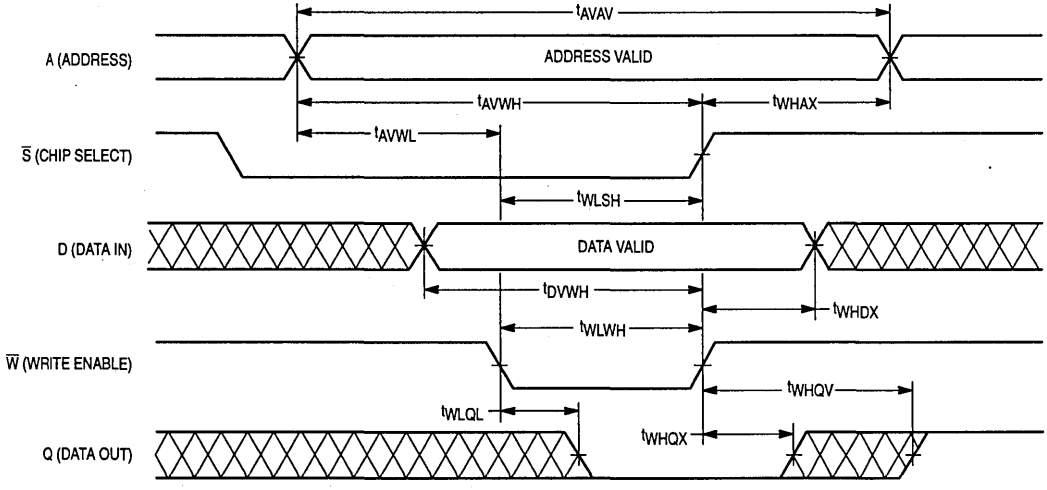


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM101524-10		MCM101524-12		MCM101524-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	1	—	1	—	1	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	7	—	8	—	9	—	ns	
Write Pulse Width	t_{WLWH} t_{WLSH}	t_{WP}	7	—	8	—	9	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	7	—	8	—	9	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	1	—	1	—	1	—	ns	
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	ns	4
Write High to Output Valid	t_{WHQV}	t_{AW}	—	11	—	13	—	16	ns	
Write Recovery Time	t_{WHAX}	t_{WR}	1	—	1	—	1	—	ns	
Write Low to Output Low	t_{WLQL}	t_{WS}	0	7	0	8	0	9	ns	

NOTES:
1. A write occurs during the overlap of $\overline{S}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

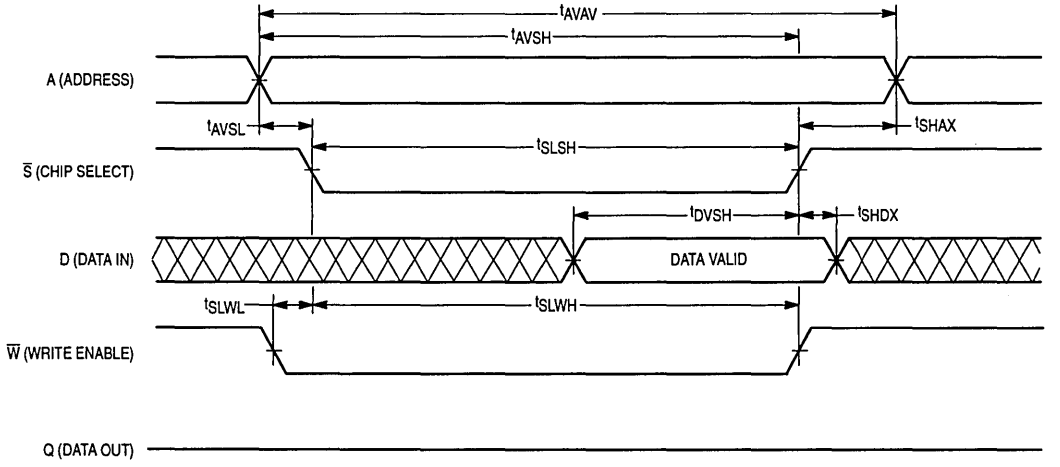


WRITE CYCLE 2 ($\overline{S}$ Controlled, See Notes 1 and 2)

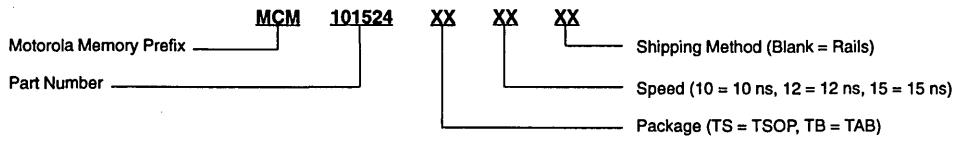
Parameter	Symbol		MCM101524-10		MCM101524-12		MCM101524-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVSL}	t_{AS}	1	—	1	—	1	—	ns	
Address Valid to End of Write	t_{AVSH}	t_{AW}	7	—	8	—	9	—	ns	
Write Pulse Width	t_{SLSH} t_{SLWH}	t_{CW}	7	—	8	—	9	—	ns	
Data Valid to End of Write	t_{DVSH}	t_{DW}	7	—	8	—	9	—	ns	
Chip Select Set-Up Time	t_{SLWL}	t_{CS}	0	—	0	—	0	—	ns	
Data Hold Time	t_{SHDX}	t_{DH}	1	—	1	—	1	—	ns	
Write Recovery Time	t_{SHAX}	t_{WR}	1	—	1	—	1	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{S}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.

WRITE CYCLE 2 ($\overline{S}$ Controlled, See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)



2

Full Part Numbers — MCM101524TS10 MCM101524TB10
MCM101524TS12 MCM101524TB12
MCM101524TS15 MCM101524TB15

CMOS Fast Static RAMs

3

3.3 Volt Supply

5 Volt Supply

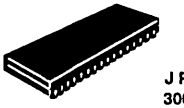
MCM6205C

32K x 9 Bit Fast Static RAM

The MCM6205C is fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

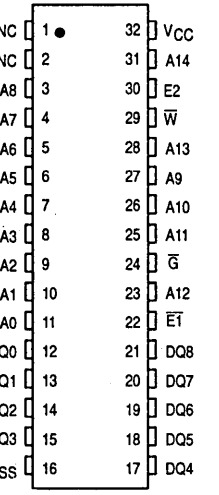
This device meets JEDEC standards for functionality and pinout, and is available in plastic dual-in-line and plastic small-outline J-leaded packages.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 15, 17, 20, 25 and 35 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Low Power Operation: 140 – 170 mA Maximum AC
- Fully TTL Compatible — Three State Output

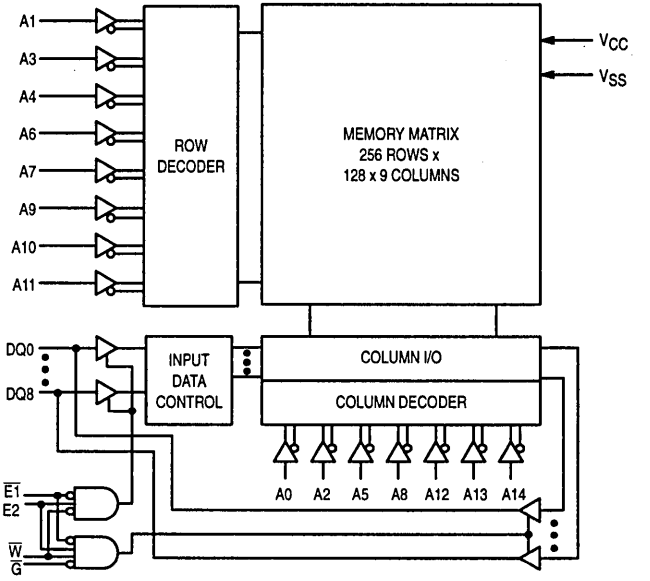


J PACKAGE
300 MIL SOJ
CASE 857

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A14	Address Input
DQ0 – DQ8	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enable
NC	No Connection
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

TRUTH TABLE (X = Don't Care)

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	H	Output Disabled	I_{CCA}	High-Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E1}$ = V_{IH} or $\overline{G}$ = V_{IH} or E2 = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	- 15	- 17	- 20	- 25	- 35	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	170	160	155	145	140	mA
AC Standby Current ($\overline{E1}$ = V_{IH}, or E2 = V_{IL}, V_{CC} = Max, f = f_{max})	I_{SB1}	50	45	45	40	40	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E1}$ ≥ V_{CC} – 0.2 V or E2 ≤ V_{SS} + 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	20	20	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Address Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E1}$, E2, $\overline{G}$, $\overline{W}$)	C_{in}	8	pF
I/O Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol		-15		-17		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	15	—	17	—	20	—	25	—	35	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	15	—	17	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	8	—	9	—	10	—	12	—	15	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	4	—	4	—	ns	5,6,7
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	8	0	8	0	9	0	10	0	11	ns	5,6,7
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	0	—	ns	5,6,7
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	7	0	8	0	8	0	10	0	11	ns	5,6,7
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	15	—	17	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} (max) is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

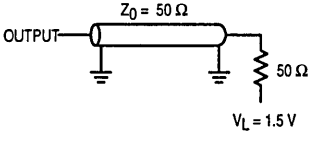


Figure 1A

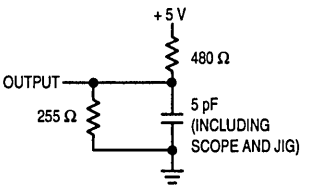


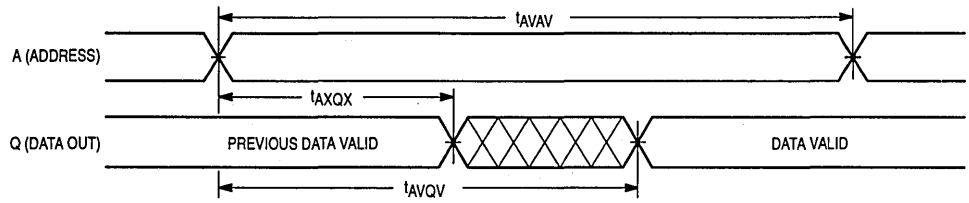
Figure 1B

TIMING LIMITS

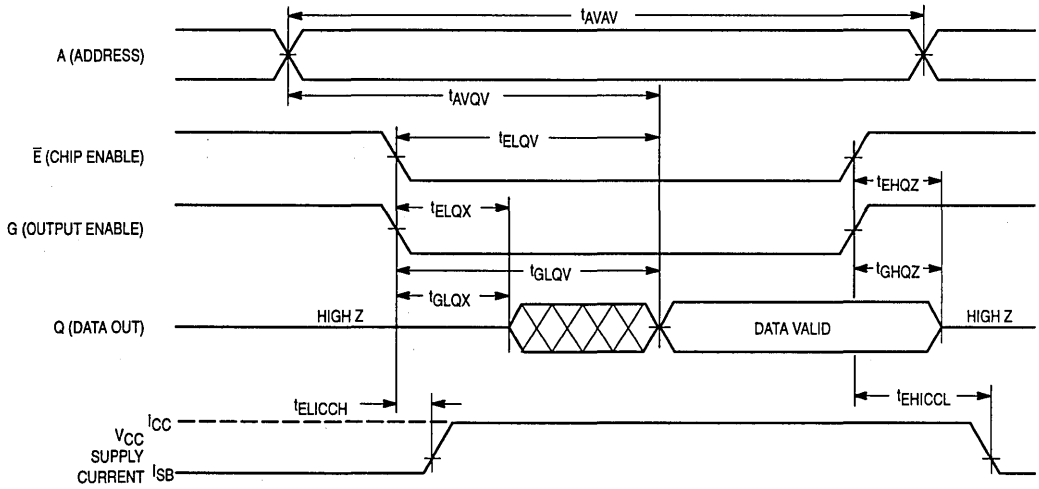
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note 4)

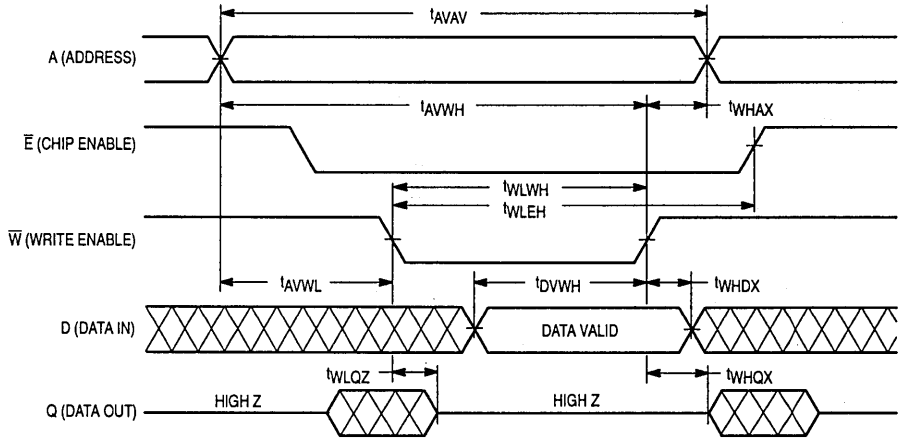


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		-15		-17		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	17	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	12	—	14	—	15	—	20	—	30	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	12	—	14	—	15	—	20	—	30	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	t_{WP}	10	—	11	—	12	—	15	—	20	—	ns	5
Data Valid to End of Write	t_{DVWH}	t_{DW}	7	—	8	—	8	—	10	—	12	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	7	0	8	0	8	0	10	0	11	ns	6,7,8
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	4	—	4	—	ns	6,7,8
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
6. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

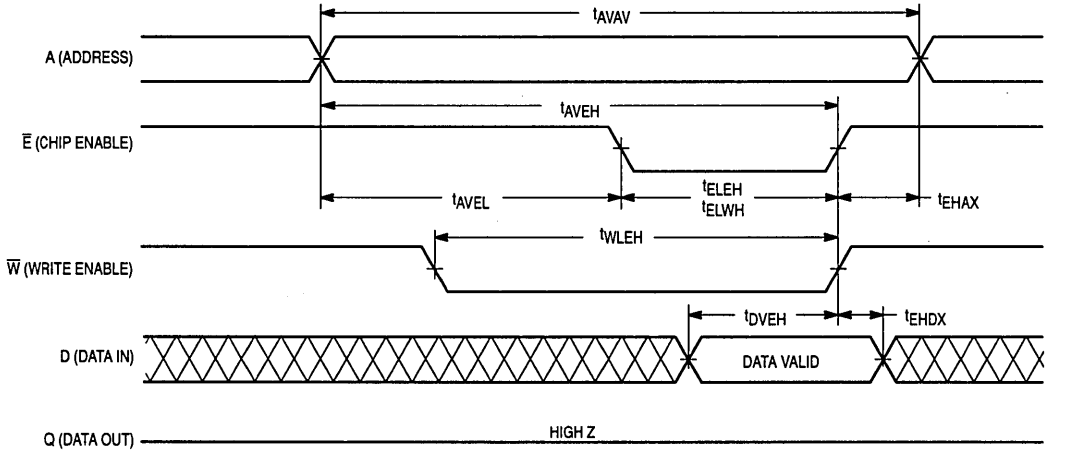


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		-15		-17		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	17	—	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	12	—	14	—	15	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	10	—	11	—	12	—	15	—	25	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	t_{DW}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6205C X XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (15 = 15 ns, 17 = 17 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- Package (J = 300 mil SOJ)

Full Part Numbers —

MCM6205CJ15	MCM6205CJ15R2
MCM6205CJ17	MCM6205CJ17R2
MCM6205CJ20	MCM6205CJ20R2
MCM6205CJ25	MCM6205CJ25R2
MCM6205CJ35	MCM6205CJ35R2

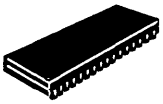
MCM6205D

32K x 9 Bit Fast Static RAM

The MCM6205D is fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

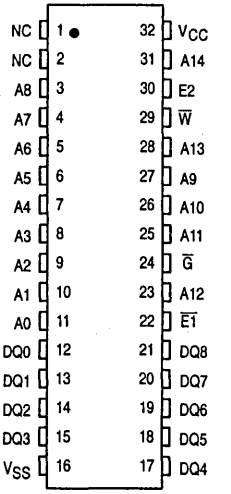
This device meets JEDEC standards for functionality and pinout, and is available in a plastic small-outline J-leaded package.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 15, 20, and 25 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Low Power Operation: 130 – 140 mA Maximum AC
- Fully TTL Compatible — Three State Output

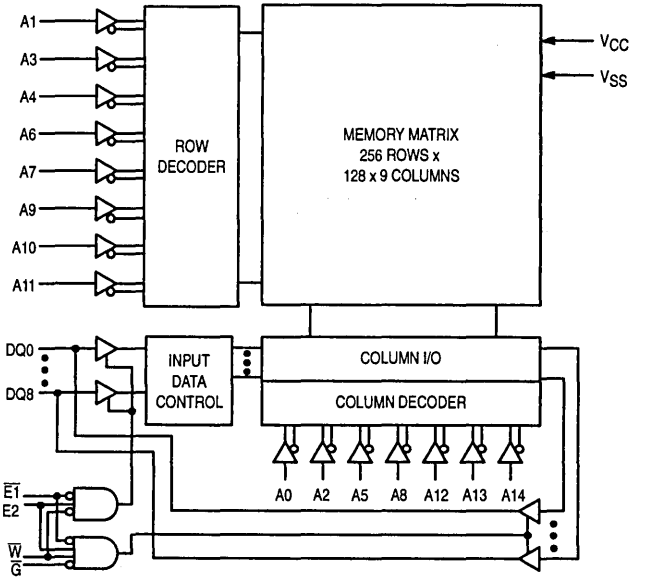


J PACKAGE
300 MIL SOJ
CASE 857

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A14	Address Input
DQ0 – DQ8	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enable
NC	No Connection
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

TRUTH TABLE (X = Don't Care)

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	H	Output Disabled	I_{CCA}	High-Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 7.0	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	− 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	− 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	− 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	− 0.5*	—	0.8	V

* V_{IL} (min) = − 0.5 V dc; V_{IL} (min) = − 2.0 V ac (pulse width ≤ 20 ns)
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E1}$ = V_{IH} or $\overline{G}$ = V_{IH} or E2 = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
Output High Voltage (I_{OH} = − 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	-15	-20	-25	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	140	135	130	mA
AC Standby Current ($\overline{E1}$ = V_{IH}, or E2 = V_{IL}, V_{CC} = Max, f = f_{max})	I_{SB1}	40	40	35	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E1}$ ≥ V_{CC} − 0.2 V or E2 ≤ V_{SS} + 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} − 0.2 V)	I_{SB2}	20	20	20	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Address Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E1}$, E2, $\overline{G}$, $\overline{W}$)	C_{in}	8	pF
I/O Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol		MCM6205D-15		MCM6205D-20		MCM6205D-25		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	15	—	20	—	25	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	15	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	15	—	20	—	25	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	8	—	10	—	12	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	ns	5, 6, 7
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	8	0	9	0	10	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns	5, 6, 7
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	7	0	8	0	10	ns	5, 6, 7
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	15	—	20	—	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} (max) is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

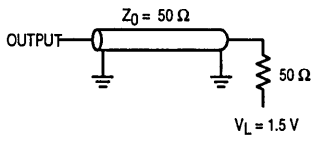


Figure 1A

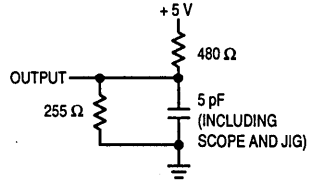
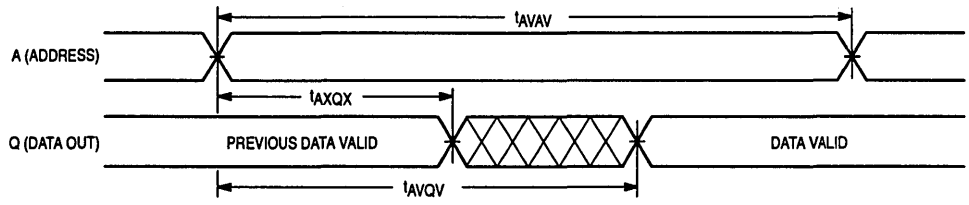


Figure 1B

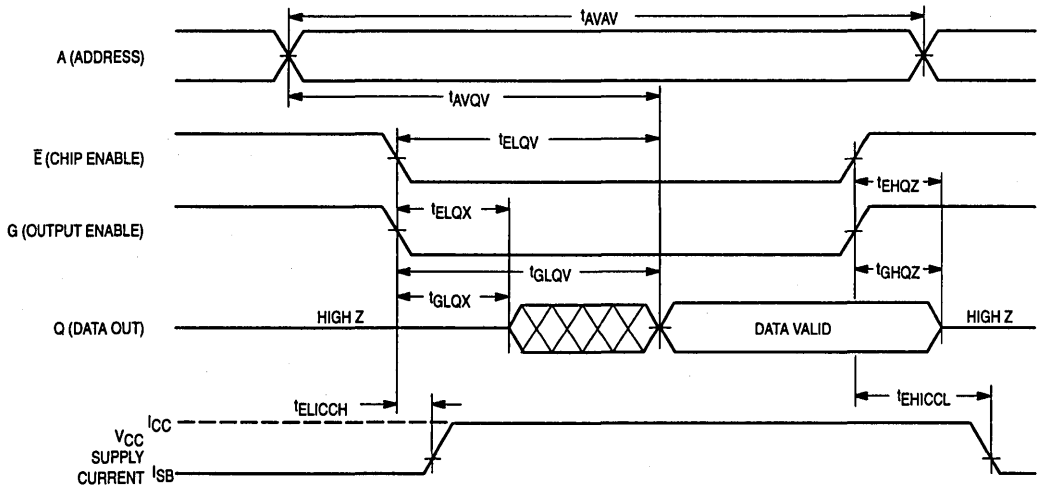
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note 4)

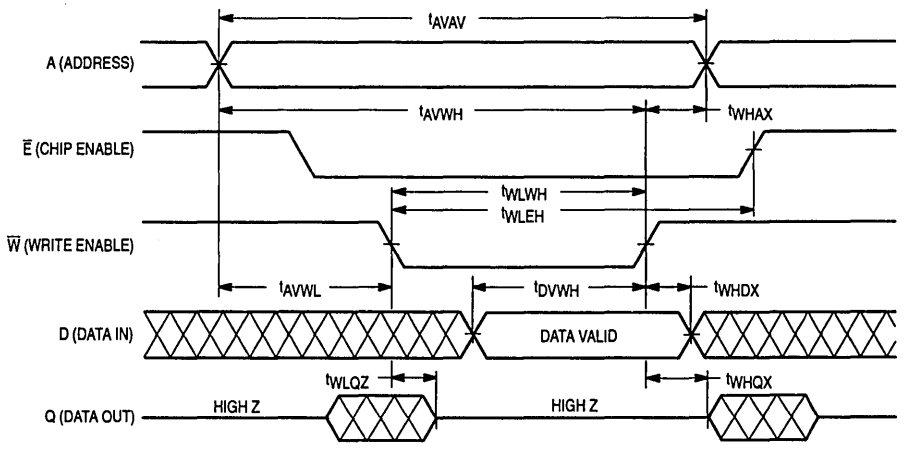


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		MCM6205D-15		MCM6205D-20		MCM6205D-25		Units	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	20	—	25	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	12	—	15	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	12	—	15	—	20	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	t_{WP}	10	—	12	—	15	—	ns	5
Data Valid to End of Write	t_{DVWH}	t_{DW}	7	—	8	—	10	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	7	0	8	0	10	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
6. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)



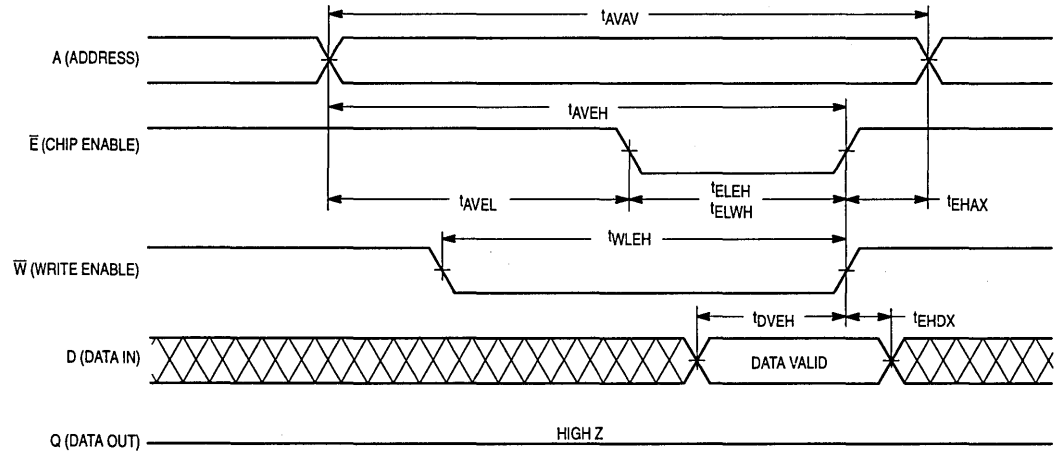
WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6205D-15		MCM6205D-20		MCM6205D-25		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	20	—	25	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	12	—	15	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	10	—	12	—	15	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	t_{DW}	7	—	8	—	10	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

3

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6205D X XX XX

- MCM — Motorola Memory Prefix
- 6205D — Part Number
- X — Package (J = 300 mil SOJ)
- XX — Speed (15 = 15 ns, 20 = 20 ns, 25 = 25 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6205DJ15, MCM6205DJ15R2, MCM6205DJ20, MCM6205DJ20R2, MCM6205DJ25, MCM6205DJ25R2

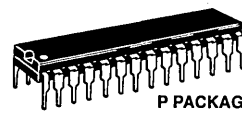
MCM6206C

32K x 8 Bit Fast Static RAM

The MCM6206C is fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

This device meets JEDEC standards for functionality and pinout, and is available in plastic dual-in-line and plastic small-outline J-leaded packages.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 15, 17, 20, 25 and 35 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Low Power Operation: 135 – 165 mA Maximum AC
- Fully TTL Compatible — Three State Output

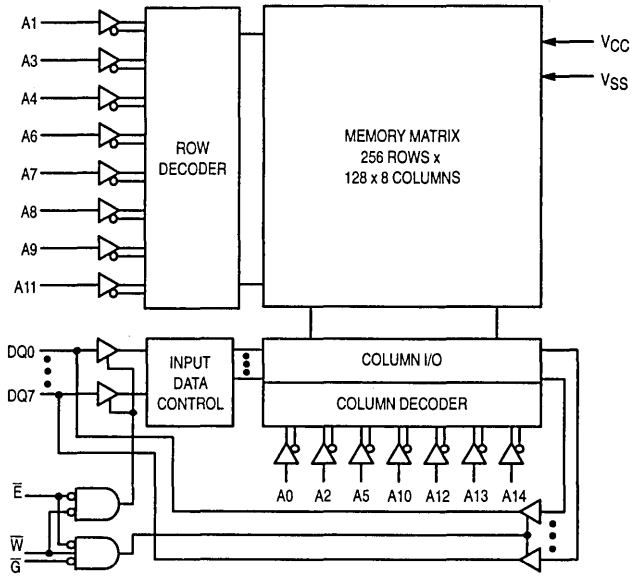


P PACKAGE
300 MIL PLASTIC
CASE 710B

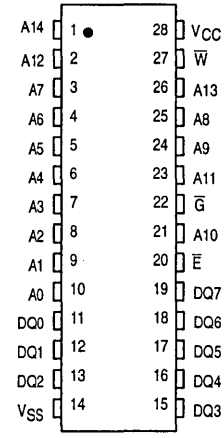
J PACKAGE
300 MIL SOJ
CASE 810B

3

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A14	Address Input
DQ0 – DQ7	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	–
L	H	H	Output Disabled	I_{CCA}	High–Z	–
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature—Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	- 15	- 17	- 20	- 25	- 35	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	165	155	150	140	135	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	50	45	45	40	40	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	20	20	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Address Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	8	pF
I/O Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol		-15		-17		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	15	—	17	—	20	—	25	—	35	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	15	—	17	—	20	—	25	—	35	ns	3
Output Enable Access Time	t_{GLQV}	t_{OE}	—	8	—	9	—	10	—	12	—	15	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	4	—	4	—	ns	4,5,6
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	4	—	4	—	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	8	0	8	0	9	0	10	0	11	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	0	—	ns	4,5,6
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	7	0	8	0	8	0	10	0	11	ns	4,5,6
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	15	—	17	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} (max) is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

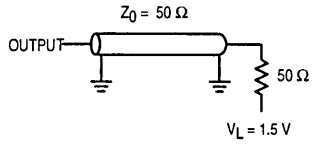


Figure 1A

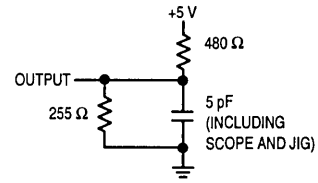


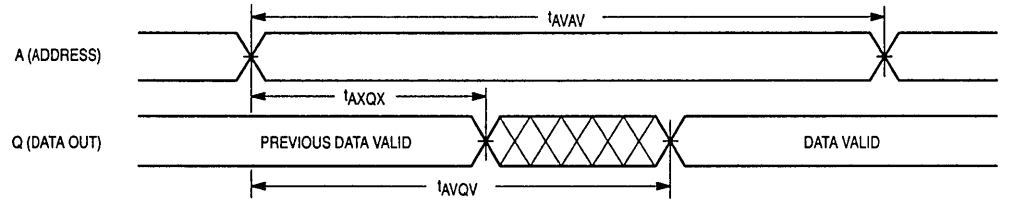
Figure 1B

TIMING LIMITS

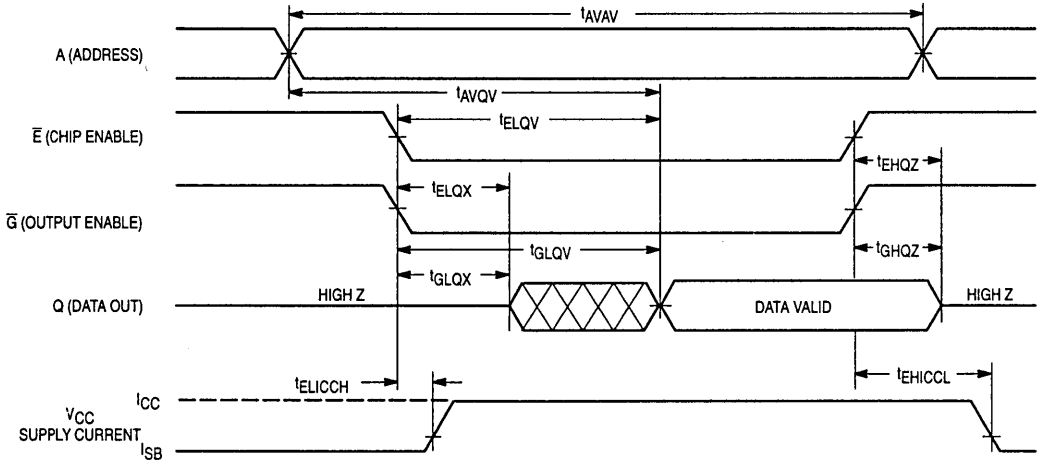
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 3)

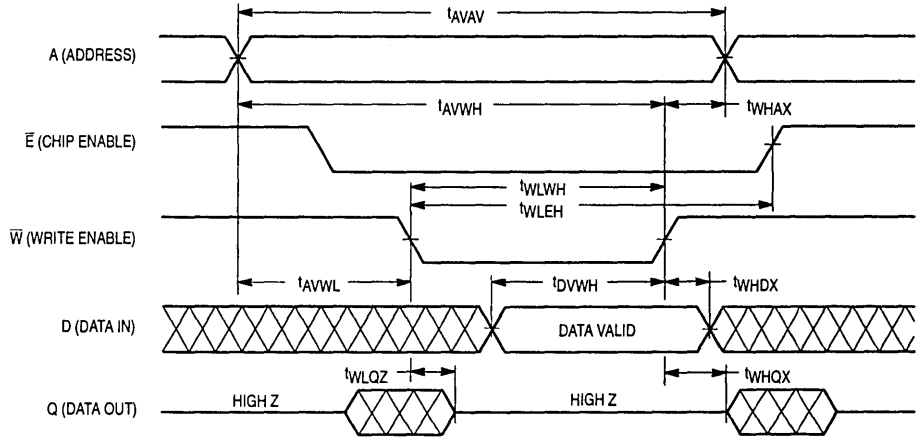


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		-15		-17		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	17	—	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	12	—	14	—	15	—	20	—	30	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	12	—	14	—	15	—	20	—	30	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	t_{WP}	10	—	11	—	12	—	15	—	20	—	ns	4
Data Valid to End of Write	t_{DVWH}	t_{DW}	7	—	8	—	8	—	10	—	12	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	7	0	8	0	8	0	10	0	11	ns	5,6,7
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	4	—	4	—	ns	5,6,7
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
5. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
6. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

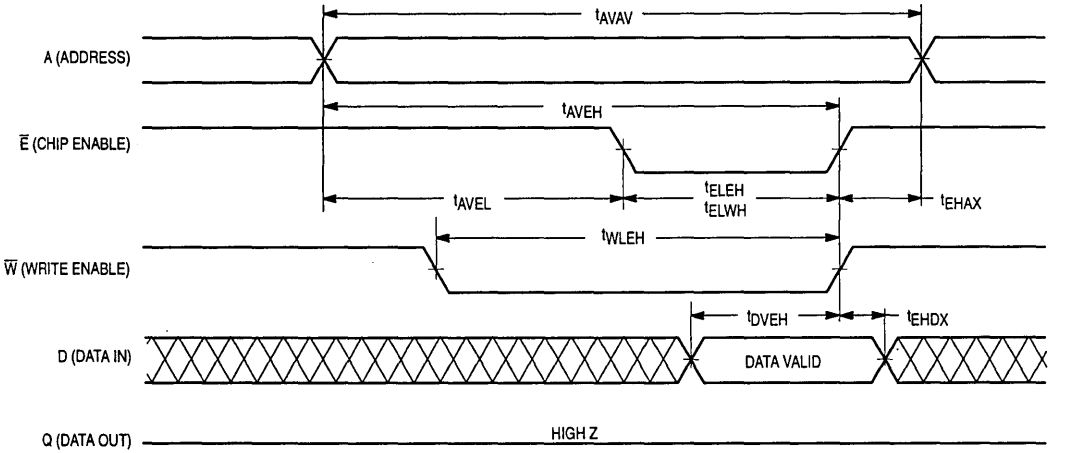


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol		-15		-17		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	17	—	20	—	25	—	35	—	ns	
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	12	—	14	—	15	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	10	—	11	—	12	—	15	—	25	—	ns	3,4
Data Valid to End of Write	t_{DVEH}	t_{DW}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All timings are referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6206C X XX XX

- MCM — Motorola Memory Prefix
- 6206C — Part Number
- X — Package (P = 300 mil Plastic DIP, J = 300 mil SOJ)
- XX — Speed (15 = 15 ns, 17 = 17 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers —

MCM6206CP15	MCM6206CJ15	MCM6206CJ15R2
MCM6206CP17	MCM6206CJ17	MCM6206CJ17R2
MCM6206CP20	MCM6206CJ20	MCM6206CJ20R2
MCM6206CP25	MCM6206CJ25	MCM6206CJ25R2
MCM6206CP35	MCM6206CJ35	MCM6206CJ35R2

MCM 6206BA

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

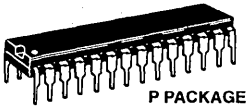
~~MCM6206D~~

32K x 8 Bit Fast Static RAM

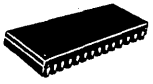
The MCM6206D is fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

This device meets JEDEC standards for functionality and pinout, and is available in plastic dual-in-line and plastic small-outline J-leaded packages.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 12, 15, 20, and 25 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Low Power Operation: 125 – 140 mA Maximum AC
- Fully TTL Compatible — Three State Output



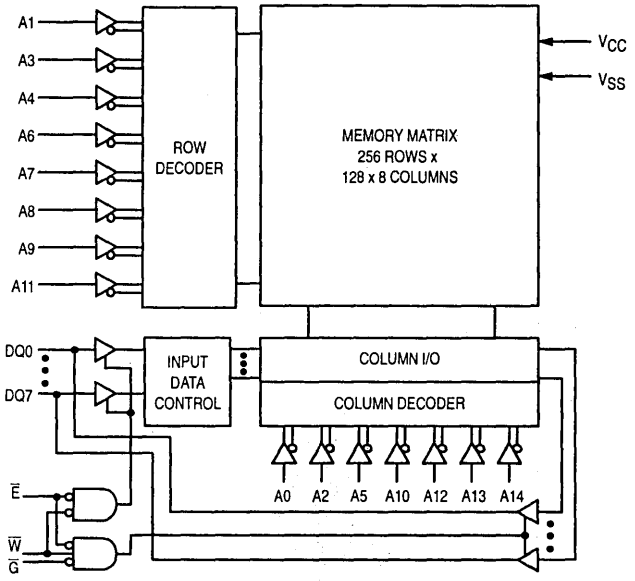
P PACKAGE
300 MIL PLASTIC
CASE 710B



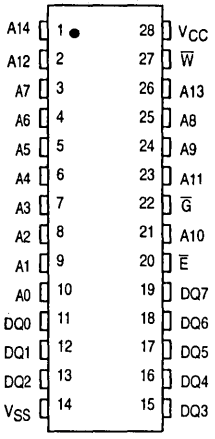
J PACKAGE
300 MIL SOJ
CASE 810B

3

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A14	Address Input
DQ0 – DQ7	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	–
L	H	H	Output Disabled	I_{CCA}	High–Z	–
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature—Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)

** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	- 12	- 15	- 20	- 25	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	140	135	130	125	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	40	35	35	30	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	20	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Address Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	8	pF
I/O Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol		-12		-15		-20		-25		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	12	—	15	—	20	—	25	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	12	—	15	—	20	—	25	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	12	—	15	—	20	—	25	ns	3
Output Enable Access Time	t_{GLQV}	t_{OE}	—	6	—	8	—	10	—	12	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	4	—	ns	4,5,6
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	4	—	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	7	0	8	0	9	0	10	ns	4,5,6
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	ns	4,5,6
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	6	0	7	0	8	0	10	ns	4,5,6
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	12	—	15	—	20	—	25	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} (max) is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

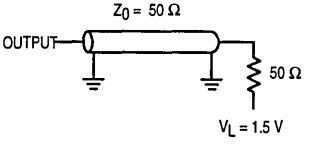


Figure 1A

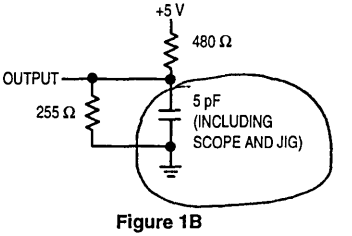
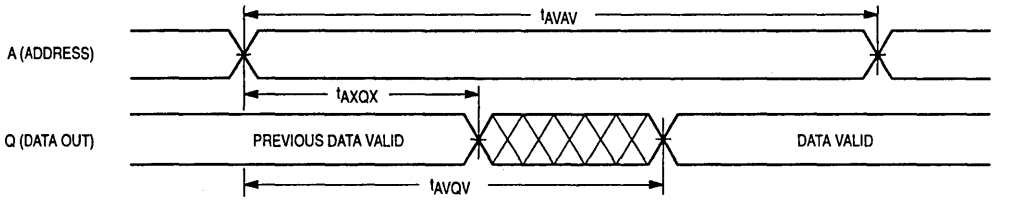


Figure 1B

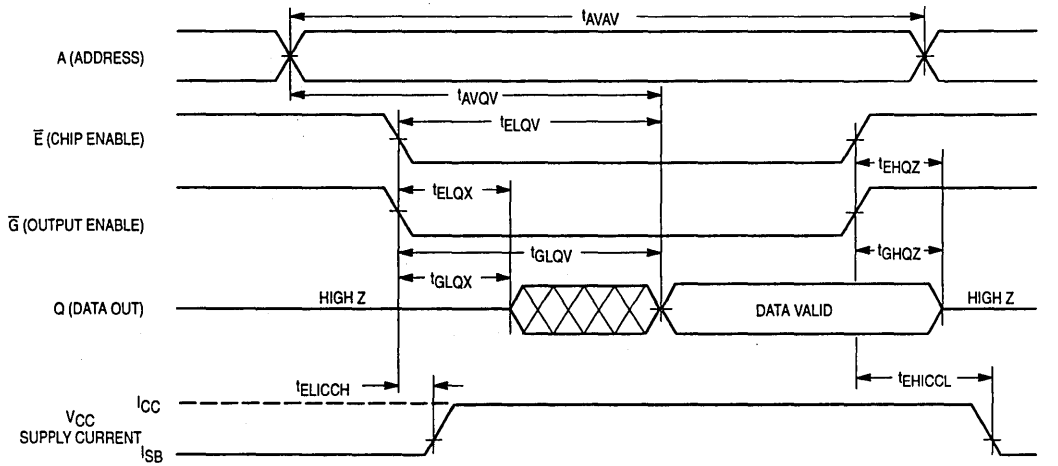
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 3)

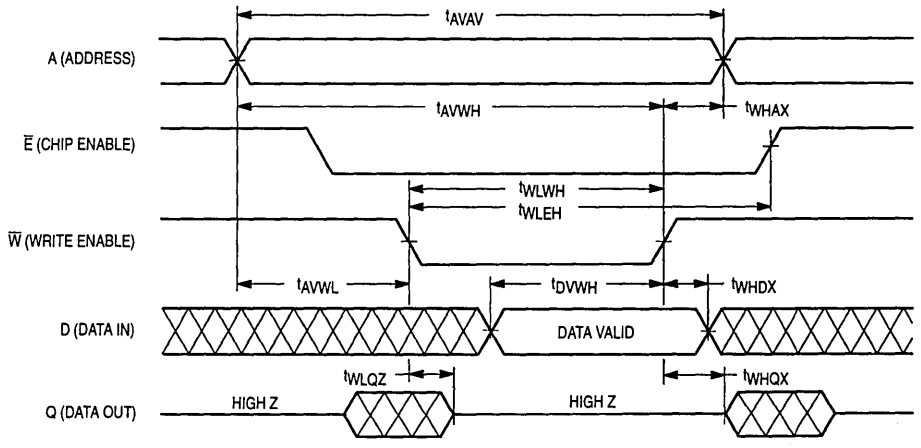


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		-12		-15		-20		-25		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	12	—	15	—	20	—	25	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	10	—	12	—	15	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	10	—	12	—	15	—	20	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	t_{WP}	10	—	10	—	12	—	15	—	ns	4
Data Valid to End of Write	t_{DVWH}	t_{DW}	6	—	7	—	8	—	10	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	6	0	7	0	8	0	10	ns	5,6,7
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	4	—	ns	5,6,7
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
5. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
6. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

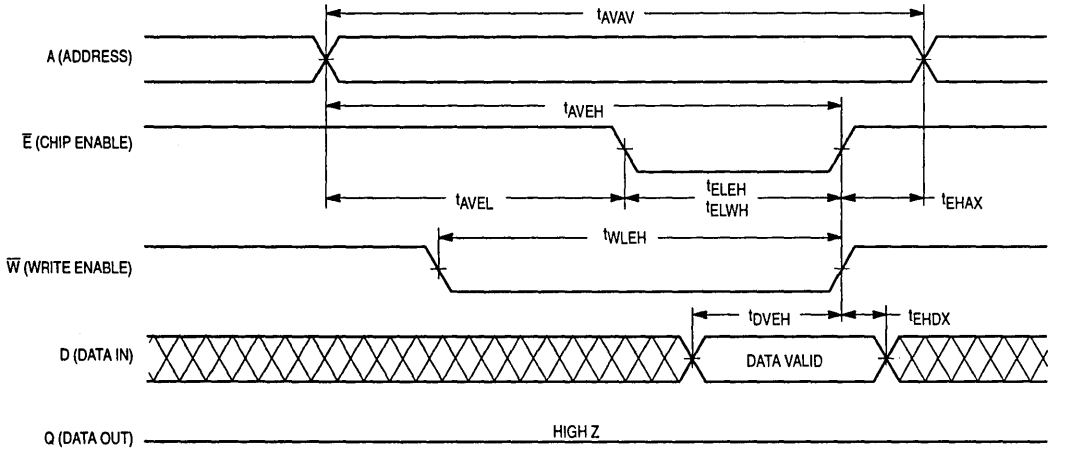


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

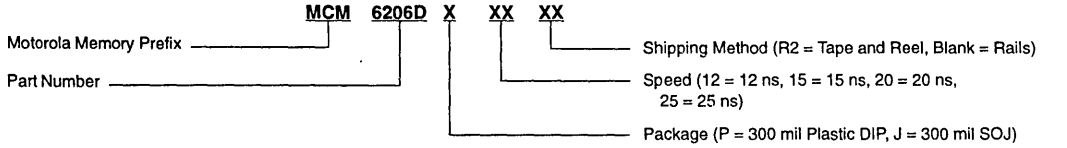
Parameter	Symbol		-12		-15		-20		-25		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	12	—	15	—	20	—	25	—	ns	
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	10	—	12	—	15	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	9	—	10	—	12	—	15	—	ns	3,4
Data Valid to End of Write	t_{DVEH}	t_{DW}	6	—	7	—	8	—	10	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All timings are referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers —

MCM6206DP12	MCM6206DJ12	MCM6206DJ12R2
MCM6206DP15	MCM6206DJ15	MCM6206DJ15R2
MCM6206DP20	MCM6206DJ20	MCM6206DJ20R2
MCM6206DP25	MCM6206DJ25	MCM6206DJ25R2

MCM62V06D

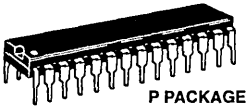
Product Preview

32K x 8 Bit 3.3 Volt Fast Static RAM

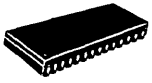
The MCM62V06D is fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

This device meets JEDEC standards for functionality and pinout, and is available in plastic dual-in-line and plastic small-outline J-leaded packages.

- Single 3.3 V ± 0.3 V Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 20, 25, and 35 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Low Power Operation: 50 mA Maximum AC
- Fully 3.3 V CMOS — Three State Output
- 100 μA Standby Mode



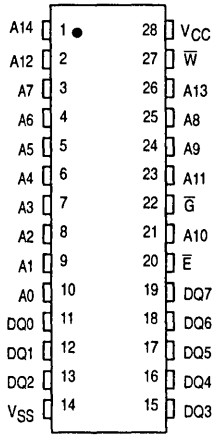
P PACKAGE
300 MIL PLASTIC
CASE 710B



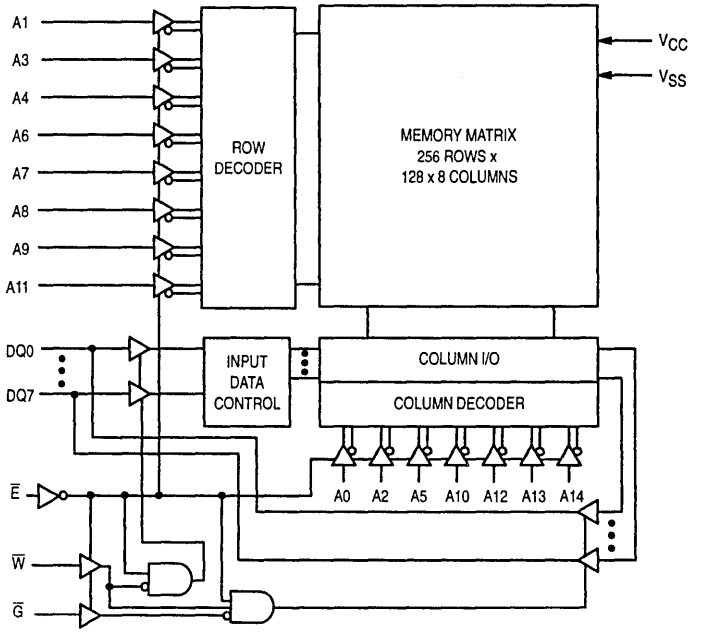
J PACKAGE
300 MIL SOJ
CASE 810B

3

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A14	Address Input
DQ0 – DQ7	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	Power Supply (+ 3.3 V)
V_{SS}	Ground

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	Output Disabled	I_{CCA}	High–Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5*	V
Input or Output Current	I_{in}, I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

* V_{CC} + 2.0 V ac to V_{SS} – 2.0 V ac (Pulse width ≤ 20 ns).

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board in still air.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 0.3 V, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 10% t_{AVAV} (min))

** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 10% t_{AVAV} (min))

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
TTL Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
TTL Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
CMOS Output High Voltage (I_{OH} = – 100 µA)	V_{OH2}	V_{CC} – 0.1	—	V
CMOS Output Low Voltage (I_{OL} = 100 µA)	V_{OL2}	—	0.1	V

POWER SUPPLY CURRENTS

Parameter	Symbol	-20	-25	-35	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	50	45	40	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	12	8	6	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V)	I_{SB2}	100	100	100	µA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Address Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	8	pF
I/O Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 0.3 V, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	—	25	—	35	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	20	—	25	—	35	ns	3
Output Enable Access Time	t_{GLQV}	t_{OE}	—	10	—	12	—	15	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	ns	6
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	ns	4, 5, 6
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	9	0	10	0	11	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns	4, 5, 6
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	8	0	10	0	11	ns	4, 5, 6
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

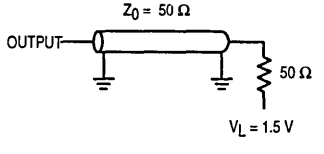


Figure 1A

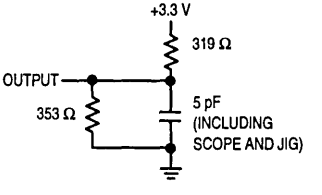
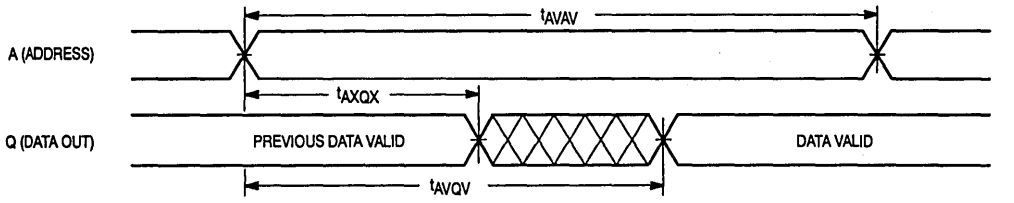


Figure 1B

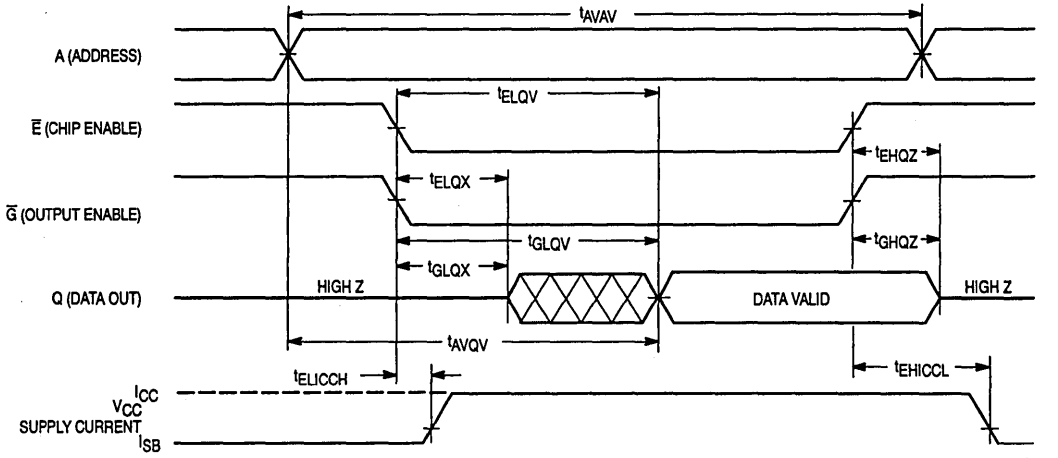
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 3)

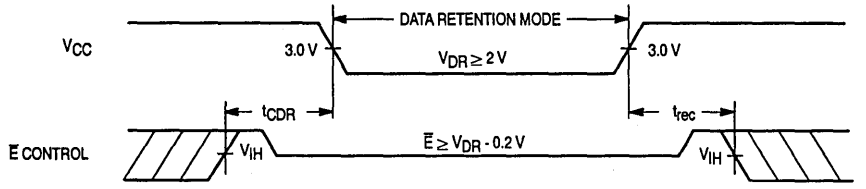


DATA RETENTION CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention ($\overline{E} \geq V_{CC}$ - 0.2 V)	V_{DR}	2	—	—	ns
Data Retention Current ($\overline{E} \geq V_{CC}$ - 0.2 V, V_{CC} = 3.0 V, CMOS Levels on Other Inputs)	I_{CCDR}	—	—	50	µA
Chip Disable to Data Retention Time	t_{CDR}	0	—	—	ns
Operation Recovery Time	t_{rec}	t_{AVAV}*	—	—	ns

* t_{AVAV} = Read Cycle Time

DATA RETENTION MODE

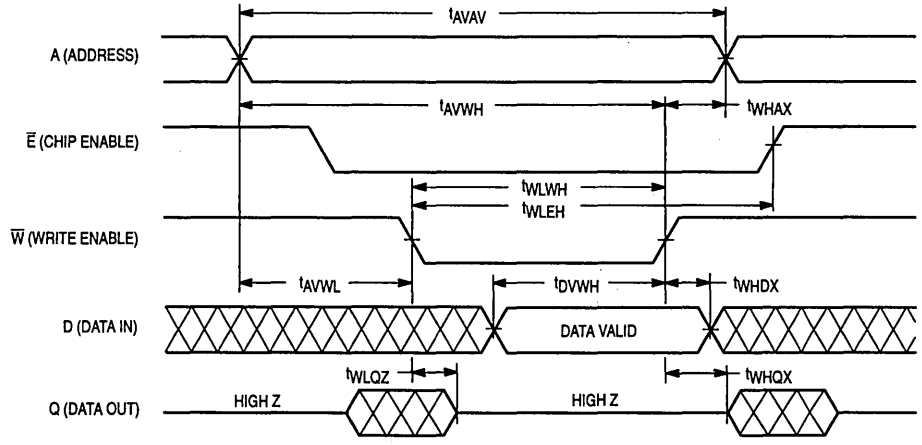


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	—	20	—	30	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	15	—	20	—	30	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	t_{WP}	12	—	15	—	20	—	ns	4
Data Valid to End of Write	t_{DVWH}	t_{DW}	8	—	10	—	12	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	8	0	10	0	11	ns	5,6,7
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	ns	5,6,7
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

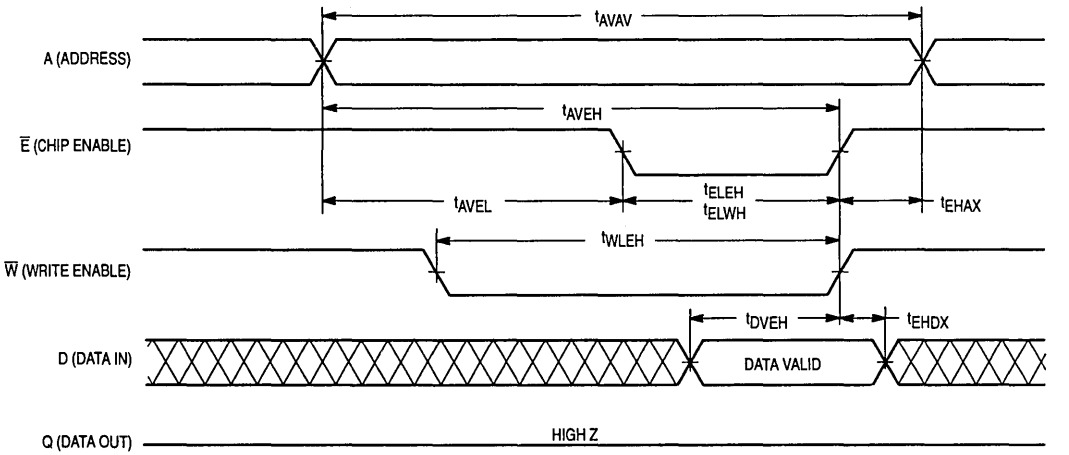


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	12	—	15	—	25	—	ns	3,4
Data Valid to End of Write	t_{DVEH}	t_{DW}	8	—	10	—	11	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All timings are referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 62V06D X XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (25 = 25 ns, 35 = 35 ns)
- Package (P = 300 mil Plastic DIP, J = 300 mil SOJ)

Full Part Numbers — MCM62V06DP20 MCM62V06DJ20 MCM62V06DJ20R2
MCM62V06DP25 MCM62V06DJ25 MCM62V06DJ25R2
MCM62V06DP35 MCM62V06DJ35 MCM62V06DJ35R2

MCM6208C

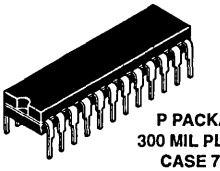
Advance Information

64K x 4 Fast Static RAM

The MCM6208C is fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

This device meets JEDEC standards for functionality and pinout, and is available in plastic dual-in-line and plastic small-outline J-leaded packages.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 12, 15, 20, 25, and 35 ns
- Equal Address and Chip Enable Access Times
- Low Power Operation: 135 –165 mA Maximum AC
- Fully TTL Compatible — Three-State Output

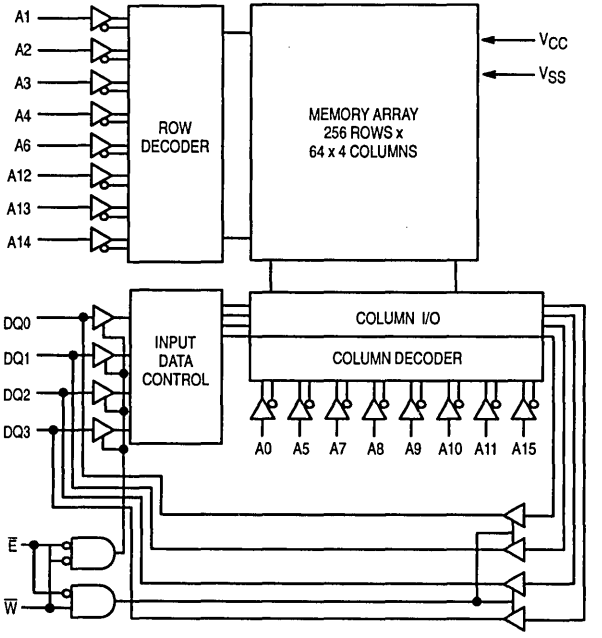


P PACKAGE
300 MIL PLASTIC
CASE 724A

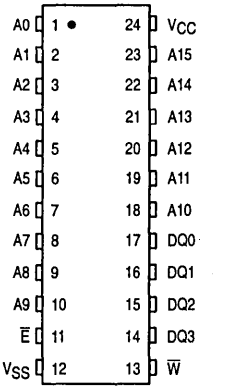
J PACKAGE
300 MIL SOJ
CASE 810A

3

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A15	Address Input
DQ0 – DQ3	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground
NC	No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E1}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V*, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V, V_{CC} = Max, f = 0 MHz)	I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

*For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.

POWER SUPPLY CURRENTS

Parameter	Symbol	- 12	- 15	- 20	- 25	- 35	Unit
AC Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	165	155	145	135	135	mA
Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	55	50	45	40	40	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Max	Unit
Address Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol		-12		-15		-20		-25		35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	12	—	15	—	20	—	25	—	35	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	12	—	15	—	20	—	25	—	25	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	12	—	15	—	20	—	25	—	25	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	6	—	8	—	10	—	12	—	—	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	4	—	4	—	ns	
Enable Low to Output Active1	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	4	—	4	—	ns	5, 6, 7
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	6	0	8	0	9	0	10	0	10	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	0	—	ns	5, 6, 7
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	6	0	7	0	8	0	10	0	—	ns	5, 6, 7
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	12	—	15	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. .For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E1} \le V_{IL}$, $\overline{G} \le V_{IL}$).

AC TEST LOADS

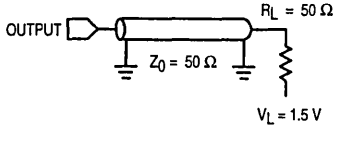


Figure 1A

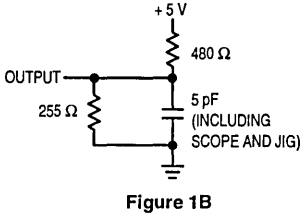


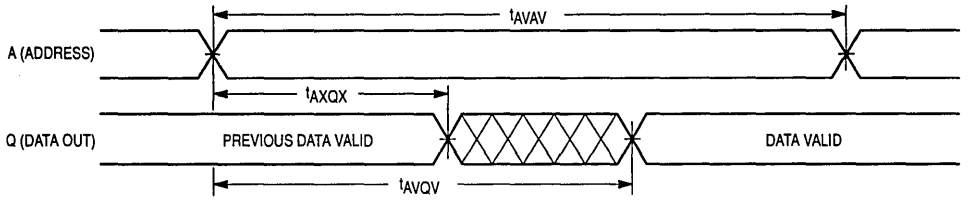
Figure 1B

TIMING LIMITS

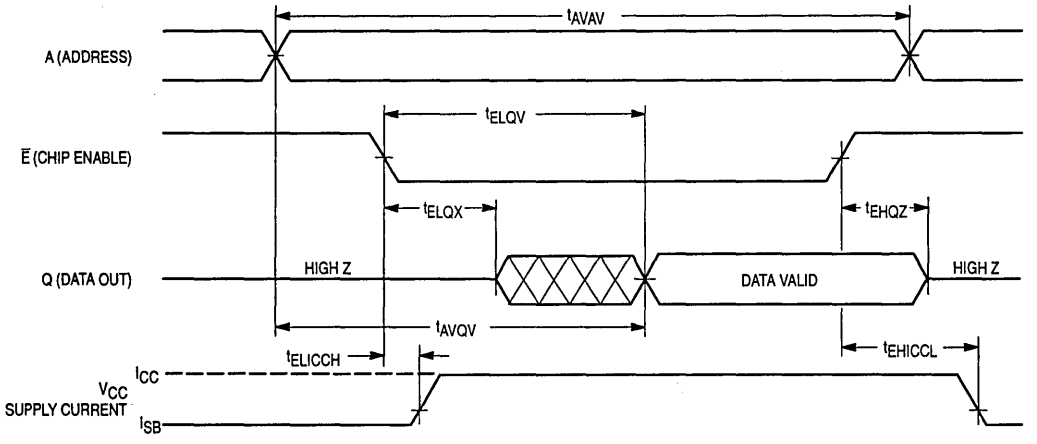
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Notes 2 and 4)

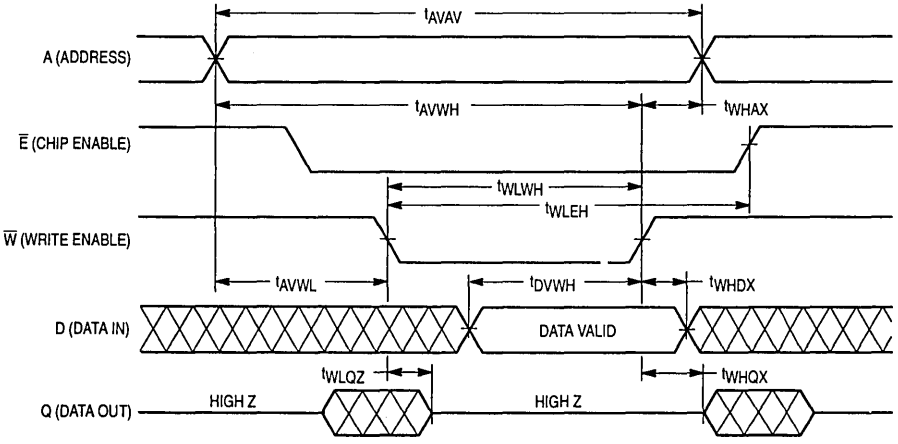


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		-12		-15		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	12	—	15	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	10	—	12	—	15	—	20	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	10	—	12	—	15	—	20	—	20	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	t_{WP}	8	—	10	—	12	—	15	—	15	—	ns	5
Data Valid to End of Write	t_{DVWH}	t_{DW}	6	—	7	—	8	—	10	—	10	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	7	0	7	0	8	0	10	0	10	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	4	—	4	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. For Output Enable devices, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. For Output Enable devices, if $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min, both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

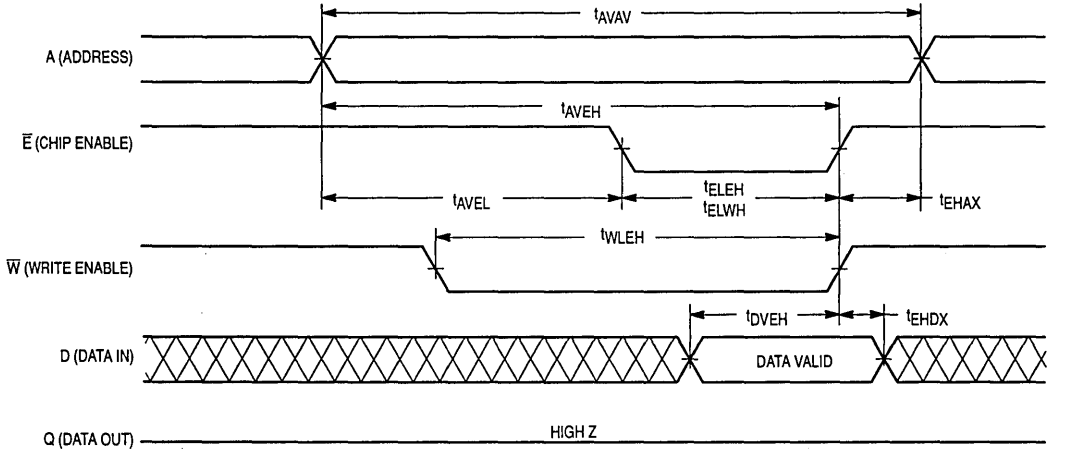


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		-12		-15		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	12	—	15	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	10	—	12	—	15	—	20	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	8	—	10	—	12	—	15	—	15	—	ns	5, 6
Data Valid to End of Write	t_{DVEH}	t_{DW}	6	—	7	—	8	—	10	—	10	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. For Output Enable devices, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6208C X XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (12 = 2ns, 15 = 15 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- Package (P = Plastic DIP, J = Plastic SOJ)

Full Part Numbers —

MCM6208CP15	MCM6208CJ12	MCM6208CJ12R2
MCM6208CP20	MCM6208CJ15	MCM6208CJ15R2
MCM6208CP25	MCM6208CJ20	MCM6208CJ20R2
MCM6208CP35	MCM6208CJ25	MCM6208CJ25R2
	MCM6208CJ35	MCM6208CJ35R2

MCM6209C

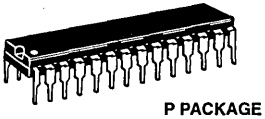
Advance Information

64K x 4 Bit Fast Static RAM
With Output Enable

The MCM6209C is fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

This device meets JEDEC standards for functionality and pinout, and is available in plastic dual-in-line and plastic small-outline J-leaded packages.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 12, 15, 20, 25, and 35 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Low Power Operation: 135 – 165 mA Maximum AC
- Fully TTL Compatible — Three-State Output

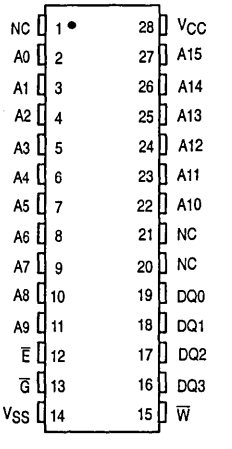


P PACKAGE
300 MIL PLASTIC
CASE 710B

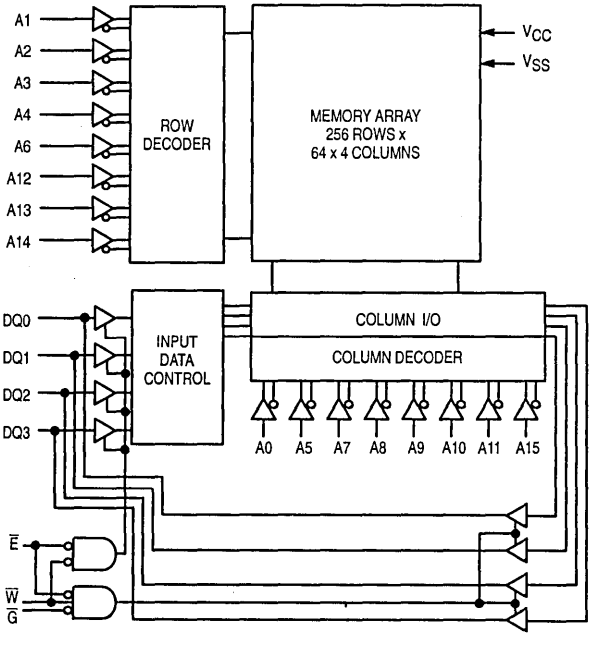
J PACKAGE
300 MIL SOJ
CASE 810B

3

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A15	Address Input
DQ0 – DQ3	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
NC	No Connection
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	Output Disabled	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read
L	X	L	Write	I_{CCA}	High-Z	Write

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)

** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V*, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V, V_{CC} = Max, f = 0 MHz)	I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

*For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.

POWER SUPPLY CURRENTS

Parameter	Symbol	-12	-15	-20	-25	-35	Unit
AC Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	165	155	145	135	130	mA
Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	55	50	45	40	35	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Max	Unit
Address Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol		-12		-15		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	12	—	15	—	20	—	25	—	35	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	12	—	15	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	12	—	15	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	6	—	8	—	10	—	12	—	15	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	4	—	4	—	ns	5, 6, 7
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	6	0	8	0	9	0	10	0	10	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	0	—	ns	5, 6, 7
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	6	0	7	0	8	0	10	0	—	ns	5, 6, 7
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	12	—	15	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E}$ = V_{IL}, E2 = V_{IH}, $\overline{G}$ ≤ V_{IL}).

AC TEST LOADS

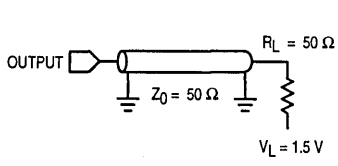


Figure 1A

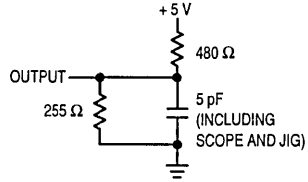


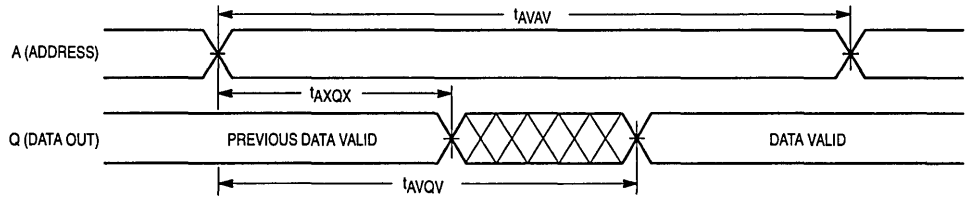
Figure 1B

TIMING LIMITS

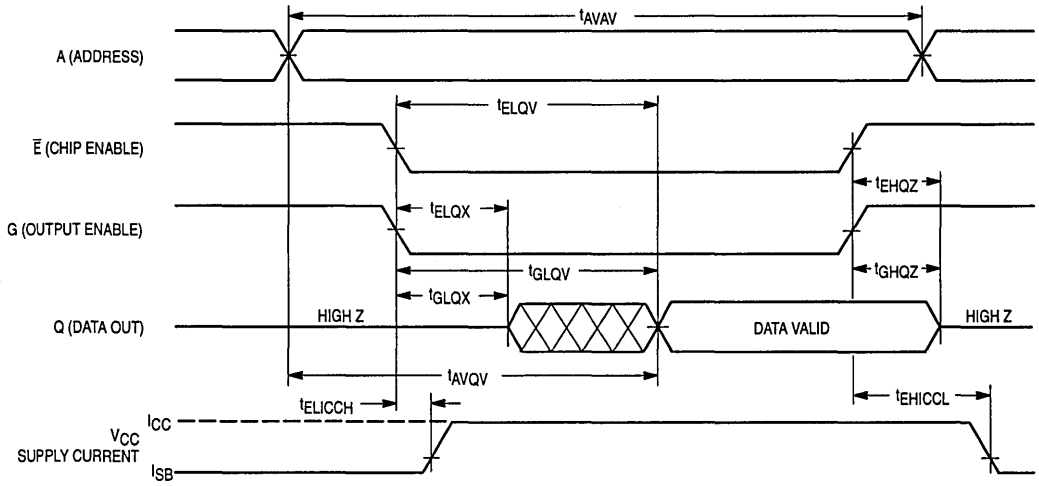
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Notes 2 and 4)

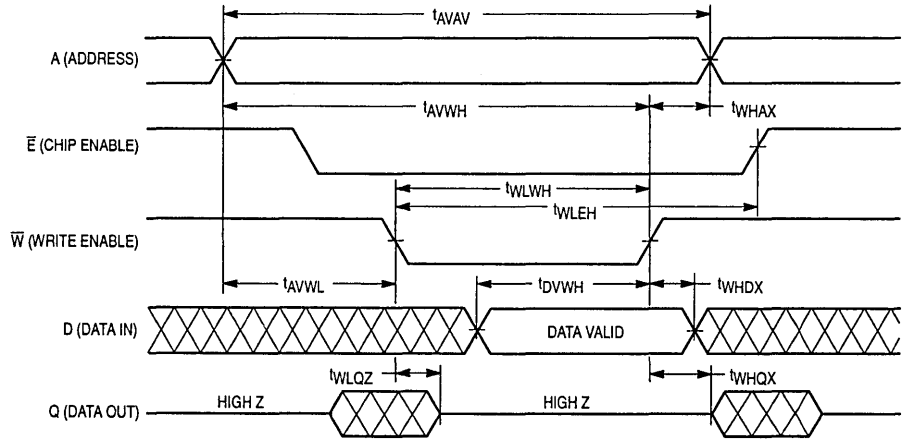


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		-12		-15		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	12	—	15	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	10	—	12	—	15	—	20	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	10	—	12	—	15	—	20	—	20	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	t_{WP}	8	—	10	—	12	—	15	—	15	—	ns	5
Data Valid to End of Write	t_{DVWH}	t_{DW}	6	—	7	—	8	—	10	—	10	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	6	0	7	0	8	0	10	0	10	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	4	—	4	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. For Output Enable devices, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. For Output Enable devices, if $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min, both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 2)

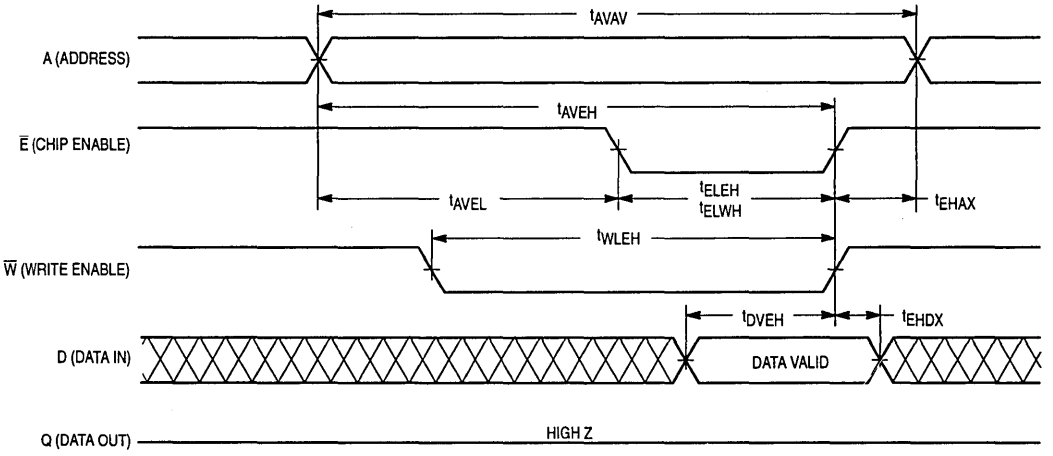


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		-12		-15		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	12	—	15	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	10	—	12	—	15	—	20	—	20	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	8	—	10	—	12	—	15	—	15	—	ns	5, 6
Data Valid to End of Write	t_{DVEH}	t_{DW}	6	—	7	—	8	—	10	—	10	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. For Output Enable devices, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 2)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6209C X XX XX

- Motorola Memory Prefix: MCM
- Part Number: 6209C
- Package (P = Plastic DIP, J = Plastic SOJ): X
- Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns): XX
- Shipping Method (R2 = Tape and Reel, Blank = Rails): XX

Full Part Numbers —

MCM6209CP15	MCM6209CJ15	MCM6209CJ15R2
MCM6209CP20	MCM6209CJ20	MCM6209CJ20R2
MCM6209CP25	MCM6209CJ25	MCM6209CJ25R2
MCM6209CP35	MCM6209CJ35	MCM6209CJ35R2
	MCM6209CJ12	MCM6209CJ12R2

MCM6226A

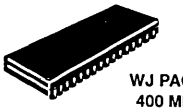
128K x 8 Bit Static Random Access Memory

The MCM6226A is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6226A is equipped with both chip enable ($\overline{E1}$ and E2) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems.

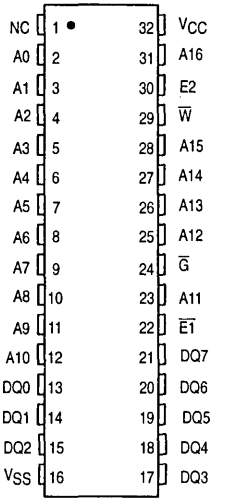
The MCM6226A is available in 400 mil, 32 lead surface-mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times:20, 25, 35, and 45 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Low Power Operation: 180/160/150/140 mA Maximum, Active AC

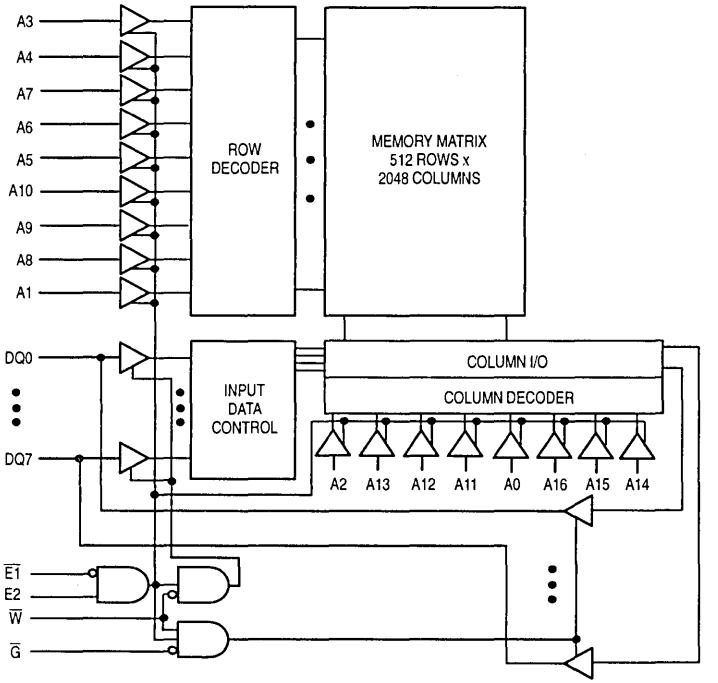


WJ PACKAGE
400 MIL SOJ
CASE 857A

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A16	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enables
DQ0 – DQ7	Data Inputs/Outputs
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	X	Not Selected	High-Z	—	I_{SB1}, I_{SB2}
X	L	X	X	Not Selected	High-Z	—	I_{SB1}, I_{SB2}
L	H	H	H	Output Disabled	High-Z	—	I_{CCA}
L	H	L	H	Read	D_{out}	Read	I_{CCA}
L	H	X	L	Write	D_{in}	Write	I_{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.1	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
** V_{IH} (max) = V_{CC} to 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ**	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1	µA
Output Leakage Current ($\overline{E}$* = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	I_{CCA}				mA
MCM6226A-20: t_{AVAV} = 20 ns		—	150	180	
MCM6226A-25: t_{AVAV} = 25 ns		—	135	160	
MCM6226A-35: t_{AVAV} = 35 ns		—	125	150	
MCM6226A-45: t_{AVAV} = 45 ns		—	120	140	
AC Standby Current (V_{CC} = max, $\overline{E}$* = V_{IH}, f = f_{max})	I_{SB1}	—	7	20	mA
CMOS Standby Current ($\overline{E}$* ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)	I_{SB2}	—	4	15	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

*$\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
**Typical values are measured at 25°C, V_{CC} = 5 V.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQ	C_{in}	4	6	pF
	$\overline{E1}$, E2, $\overline{G}$, and $\overline{W}$	C_{ck}	5	8	
I/O Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol		6226A-20		6226A-25		6226A-35		6226A-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	—	25	—	35	—	45	—	ns	4
Address Access Time	t_{AVQV}	t_{AA}	—	20	—	25	—	35	—	45	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	20	—	25	—	35	—	45	ns	5
Output Enable Access Time	t_{GLQV}	t_{OE}	—	8	—	10	—	15	—	15	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	—	5	—	5	—	5	—	ns	6, 7, 8
Output Enable Low to Output Active	t_{GLQX}	t_{LZ}	0	—	0	—	0	—	0	—	ns	6, 7, 8
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	9	0	10	0	12	0	15	ns	6, 7, 8
Output Enable High to Output High-Z	t_{GHQZ}	t_{HZ}	0	9	0	10	0	12	0	15	ns	6, 7, 8
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	20	—	25	—	35	—	45	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. All timings are referenced from the last valid address to the first transitioning address.
5. Addresses valid prior to or coincident with $\overline{E}$ going low.
6. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.
9. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

AC TEST LOADS

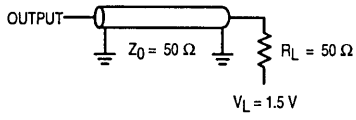


Figure 1A

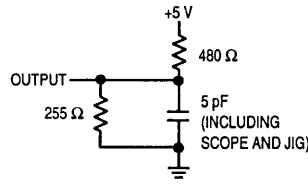


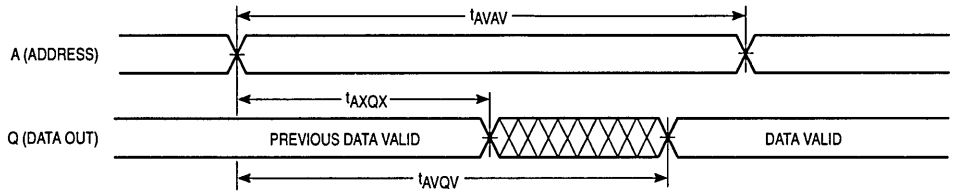
Figure 1B

TIMING LIMITS

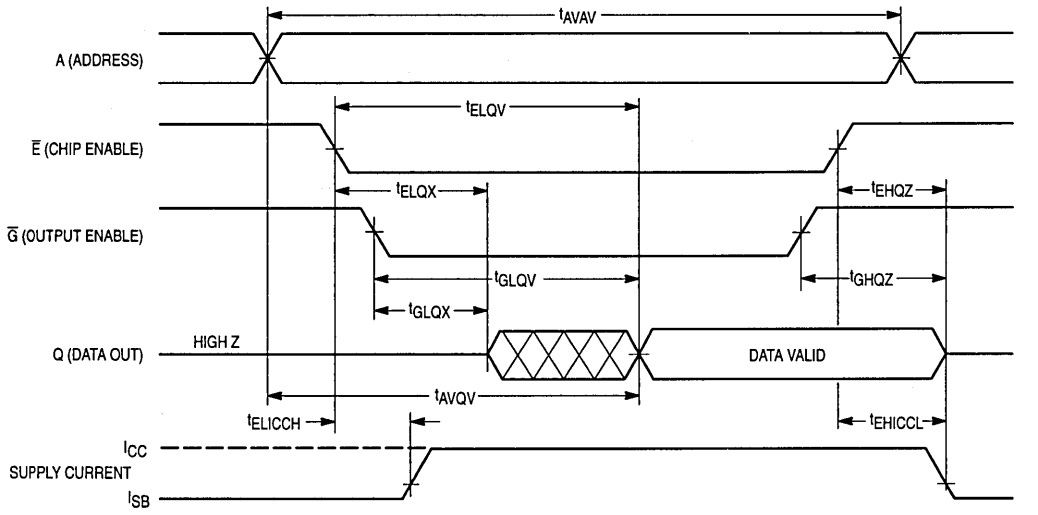
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Notes 1, 2, 3, and 9)



READ CYCLE 2 (See Notes 3 and 5)

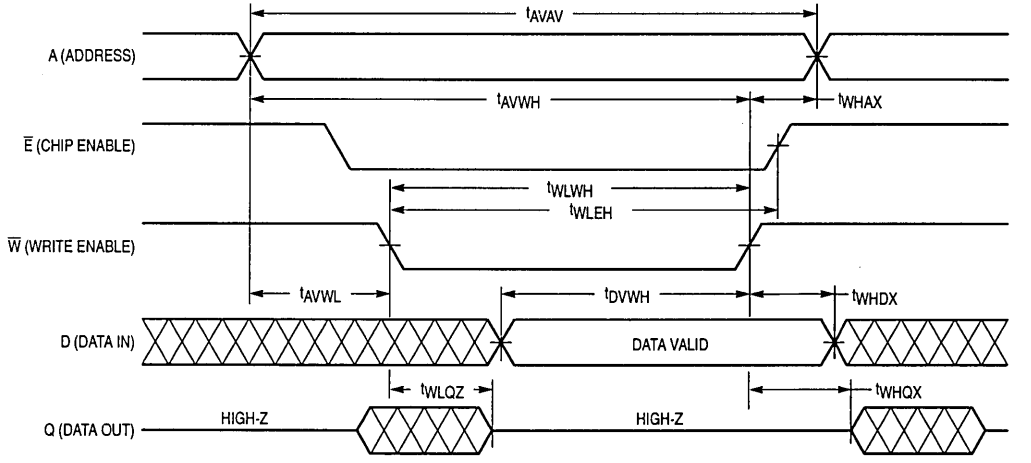


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, 3, and 4)

Parameter	Symbol		6226A-20		6226A-25		6226A-35		6226A-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	45	—	ns	5
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	—	17	—	20	—	25	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	—	17	—	20	—	25	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	10	—	15	—	20	—	ns	
Data Hold TIme	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	9	0	10	0	15	0	20	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	t_{OW}	5	—	5	—	5	—	5	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1, 2, 3, and 4)

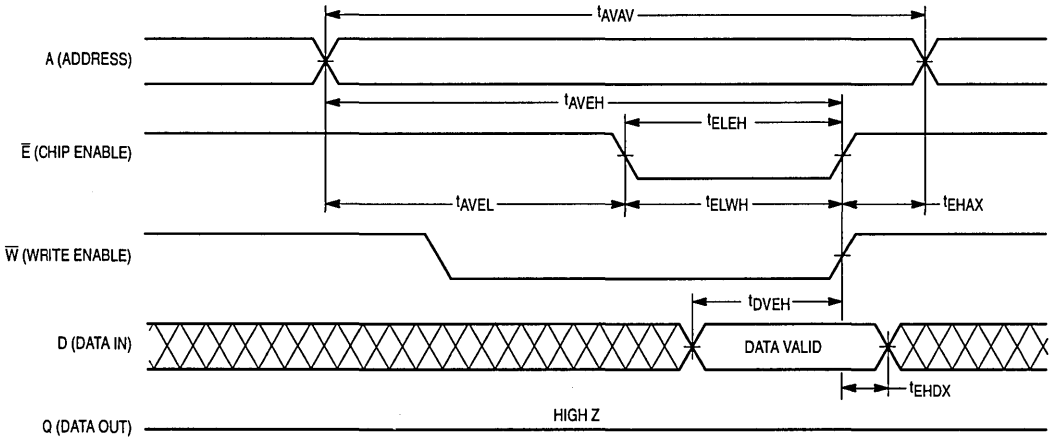


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, 3, and 4)

Parameter	Symbol		6226A-20		6226A-25		6226A-35		6226A-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	45	—	ns	5
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	—	17	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	15	—	17	—	20	—	25	—	ns	6, 7
Enable to End of Write	t_{ELWH}	t_{CW}	15	—	17	—	20	—	25	—	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	15	—	17	—	20	—	25	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	—	10	—	15	—	20	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
7. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high-impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1, 2, 3, and 4)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6226A WJ XX XX

- MCM — Motorola Memory Prefix
- 6226A — Part Number
- WJ — Package (WJ = 400 mil SOJ)
- XX — Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns, 45 = 45 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6226AWJ20, MCM6226AWJ20R2, MCM6226AWJ25, MCM6226AWJ25R2, MCM6226AWJ35, MCM6226AWJ35R2, MCM6226AWJ45, MCM6226AWJ45R2

MCM6226B

Product Preview

128K x 8 Bit Static Random Access Memory

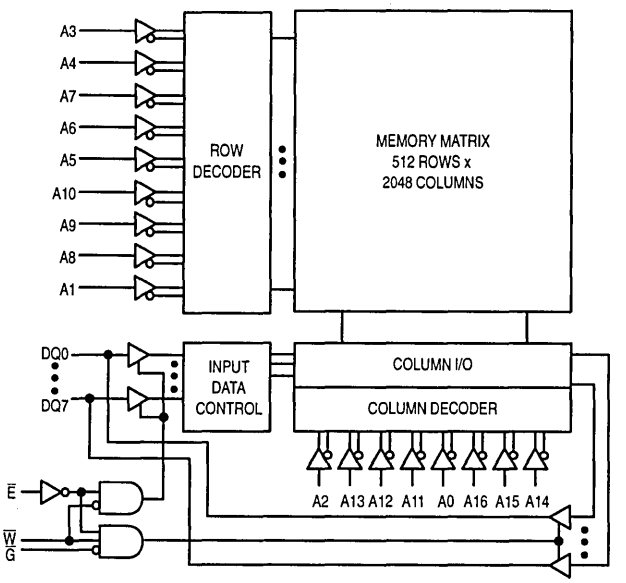
The MCM6226B is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6226B is equipped with both chip enable ($\overline{E1}$ and E2) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems.

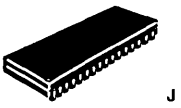
The MCM6226B is available in 300 mil and 400 mil, 32 lead surface-mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 15/17/20/25/35 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Low Power Operation: 130/125/120/115/110 mA Maximum, Active AC

BLOCK DIAGRAM



WJ PACKAGE
400 MIL SOJ
CASE 857A



J PACKAGE
300 MIL SOJ
CASE 857

3

PIN ASSIGNMENT

NC	1	32	V_{CC}
A0	2	31	A16
A1	3	30	E2
A2	4	29	$\overline{W}$
A3	5	28	A15
A4	6	27	A14
A5	7	26	A13
A6	8	25	A12
A7	9	24	$\overline{G}$
A8	10	23	A11
A9	11	22	$\overline{E1}$
A10	12	21	DQ7
DQ0	13	20	DQ6
DQ1	14	19	DQ5
DQ2	15	18	DQ4
V_{SS}	16	17	DQ3

PIN NAMES

A0 – A16	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enables
DQ0 – DQ7	Data Inputs/Outputs
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	X	Not Selected	High-Z	—	I_{SB1}, I_{SB2}
X	L	X	X	Not Selected	High-Z	—	I_{SB1}, I_{SB2}
L	H	H	H	Output Disabled	High-Z	—	I_{CCA}
L	H	L	H	Read	D_{out}	Read	I_{CCA}
L	H	X	L	Write	D_{in}	Write	I_{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.1	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$* = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	MCM6226B-15: t_{AVAV} = 15 ns	I_{CCA}	—	130	mA
	MCM6226B-17: t_{AVAV} = 17 ns		—	125	
	MCM6226B-20: t_{AVAV} = 20 ns		—	120	
	MCM6226B-25: t_{AVAV} = 25 ns		—	115	
	MCM6226B-35: t_{AVAV} = 35 ns		—	110	
AC Standby Current (V_{CC} = max, $\overline{E}$* = V_{IH}, f = f_{max})	MCM6226B-15: t_{AVAV} = 15 ns	I_{SB1}	—	35	mA
	MCM6226B-17: t_{AVAV} = 17 ns		—	35	
	MCM6226B-20: t_{AVAV} = 20 ns		—	30	
	MCM6226B-25: t_{AVAV} = 25 ns		—	25	
	MCM6226B-35: t_{AVAV} = 35 ns		—	20	
CMOS Standby Current ($\overline{E}$* ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)		I_{SB2}	—	5	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	V

*$\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQs	C_{in}	4	6	pF
	$\overline{E1}$, E2, $\overline{G}$, and $\overline{W}$	C_{ck}	5	8	
I/O Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol		6226B-15		6226B-17		6226B-20		6226B-25		6226B-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	15	—	17	—	20	—	25	—	35	—	ns	4
Address Access Time	t_{AVQV}	t_{AA}	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	15	—	17	—	20	—	25	—	35	ns	5
Output Enable Access Time	t_{GLQV}	t_{OE}	—	6	—	7	—	7	—	8	—	8	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	—	5	—	5	—	5	—	5	—	ns	6, 7, 8
Output Enable Low to Output Active	t_{GLQX}	t_{LZ}	0	—	0	—	0	—	0	—	0	—	ns	6, 7, 8
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	6	0	7	0	7	0	8	0	8	ns	6, 7, 8
Output Enable High to Output High-Z	t_{GHQZ}	t_{HZ}	0	6	0	7	0	7	0	8	0	8	ns	6, 7, 8

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. All timings are referenced from the last valid address to the first transitioning address.
5. Addresses valid prior to or coincident with $\overline{E}$ going low.
6. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.
9. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

AC TEST LOADS

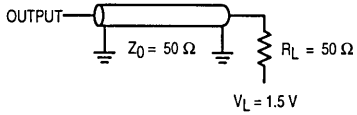


Figure 1A

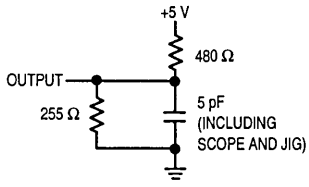
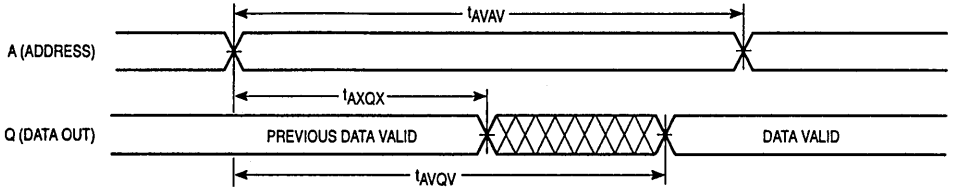


Figure 1B

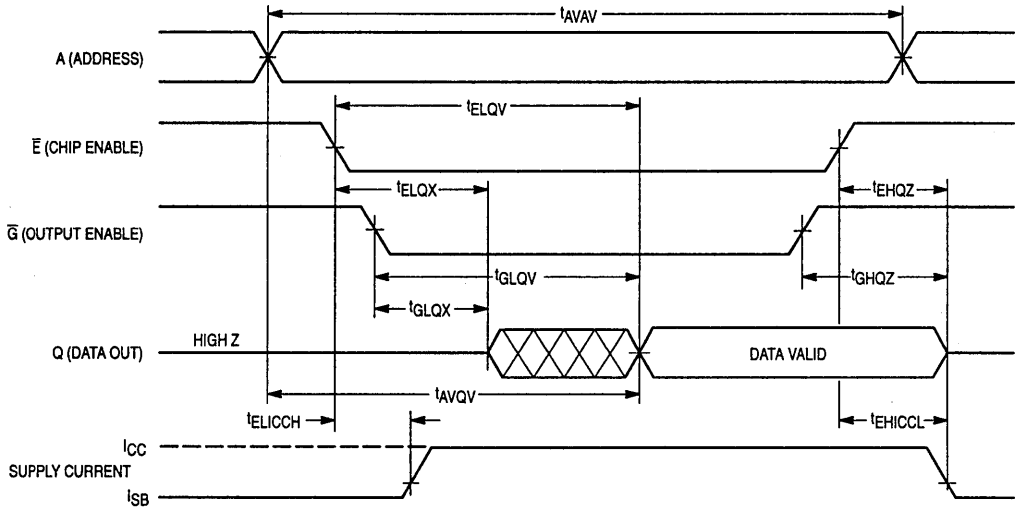
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, 3, and 9)



READ CYCLE 2 (See Notes 3 and 5)

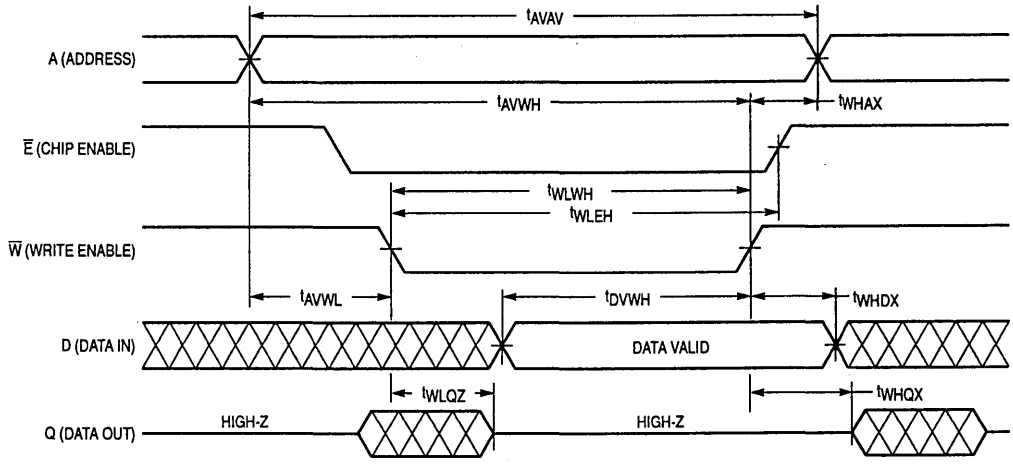


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, 3, and 4)

Parameter	Symbol		6226B-15		6226B-17		6226B-20		6226B-25		6226B-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	17	—	20	—	25	—	35	—	ns	5
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	12	—	14	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold TIme	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	6	0	7	0	7	0	8	0	8	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	t_{OW}	5	—	5	—	5	—	5	—	5	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1, 2, 3, and 4)

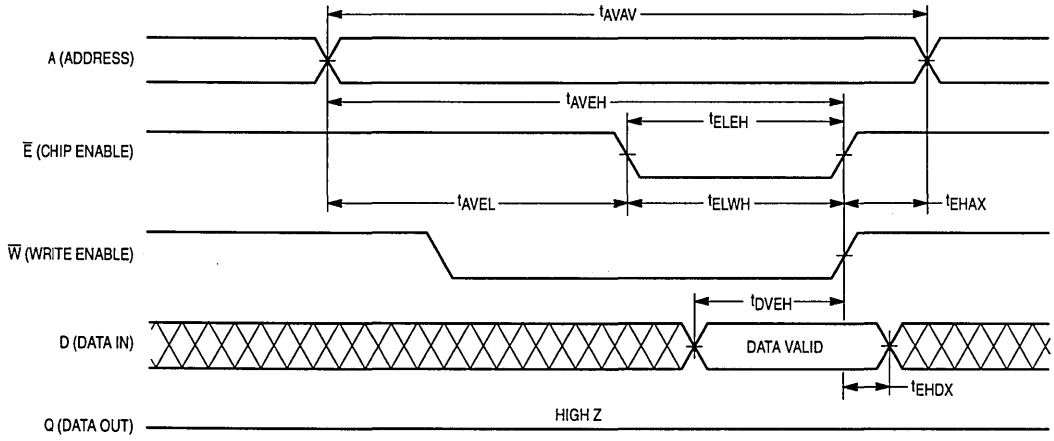


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, 3, and 4)

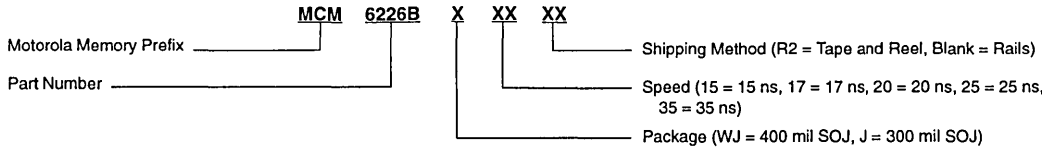
Parameter	Symbol		6226B-15		6226B-17		6226B-20		6226B-25		6226B-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	17	—	20	—	25	—	35	—	ns	5
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	12	—	14	—	15	—	17	—	20	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	10	—	11	—	12	—	15	—	20	—	ns	6, 7
Enable to End of Write	t_{ELWH}	t_{CW}	10	—	11	—	12	—	15	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E1}$.
4. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
5. All timings are referenced from the last valid address to the first transitioning address.
6. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
7. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high-impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1, 2, 3, and 4)



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers —		
	MCM6226BJ15	MCM6226BJ15R2
	MCM6226BJ17	MCM6226BJ17R2
	MCM6226BJ20	MCM6226BJ20R2
	MCM6226BJ25	MCM6226BJ25R2
	MCM6226BJ35	MCM6226BJ35R2
	MCM6226BWJ15	MCM6226BWJ15R2
	MCM6226BWJ17	MCM6226BWJ17R2
	MCM6226BWJ20	MCM6226BWJ20R2
	MCM6226BWJ25	MCM6226BWJ25R2
	MCM6226BWJ35	MCM6226BWJ35R2

3

MCM6227A

1M x 1 Bit Static Random Access Memory

WJ PACKAGE
400 MIL SOJ
CASE 810

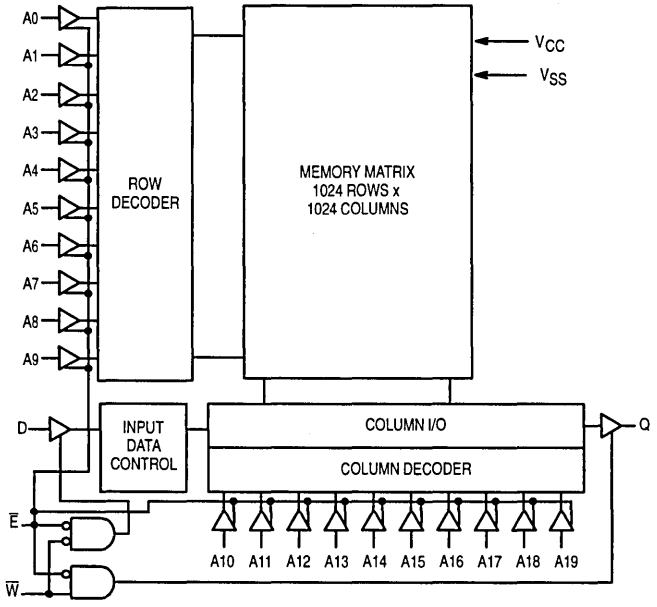
The MCM6227A is a 1,048,576 bit static random-access memory organized as 1,048,576 words of 1 bit, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6227A is equipped with a chip enable ($\overline{E}$) pin. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again.

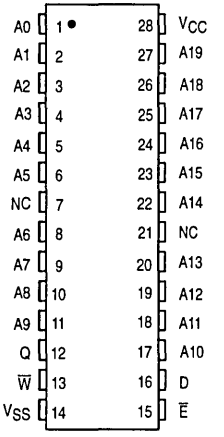
The MCM6227A is available in 400 mil, 28-lead surface-mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times:20, 25, 35, and 45 ns
- Equal Address and Chip Enable Access Times
- Input and Output are TTL Compatible
- Three-State Output
- Low Power Operation: 160/140/130/120 mA Maximum, Active AC

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A19	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

MCM6227A TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	Not Selected	High-Z	—	I_{SB1}, I_{SB2}
L	H	Read	D_{out}	Read	I_{CCA}
L	L	Write	High-Z	Write	I_{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.1	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
**V_{IH} (max) = V_{CC} = 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ*	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	I_{CCA}				mA
MCM6227A-20: t_{AVAV} = 20 ns		—	120	160	
MCM6227A-25: t_{AVAV} = 25 ns		—	110	140	
MCM6227A-35: t_{AVAV} = 35 ns		—	100	130	
MCM6227A-45: t_{AVAV} = 45 ns		—	90	120	
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, f = f_{max})	I_{SB1}	—	7	20	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)	I_{SB2}	—	4	15	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

*Typical values are measured at 25°C, V_{CC} = 5 V.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and D, Q $\overline{E}$ and $\overline{W}$	C_{in}	4 5	6 8	pF
Input and Output Capacitance	D, Q	C_{in}, C_{out}	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		6227A-20		6227A-25		6227A-35		6227A-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	—	25	—	35	—	45	—	ns	2,3
Address Access Time	t_{AVQV}	t_{AA}	—	20	—	25	—	35	—	45	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	20	—	25	—	35	—	45	ns	4
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	—	5	—	5	—	5	—	ns	5, 6, 7
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	9	0	10	0	12	—	18	ns	5, 6, 7
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	20	—	25	—	35	—	45	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \leq V_{IL}$).

AC TEST LOADS

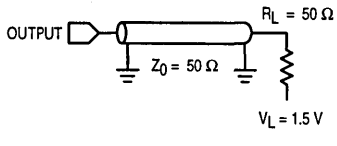


Figure 1A

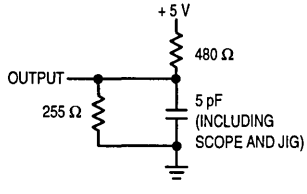


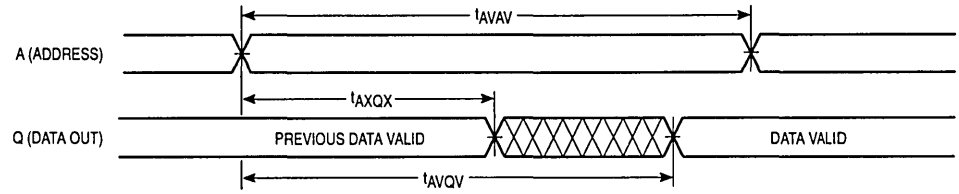
Figure 1B

TIMING LIMITS

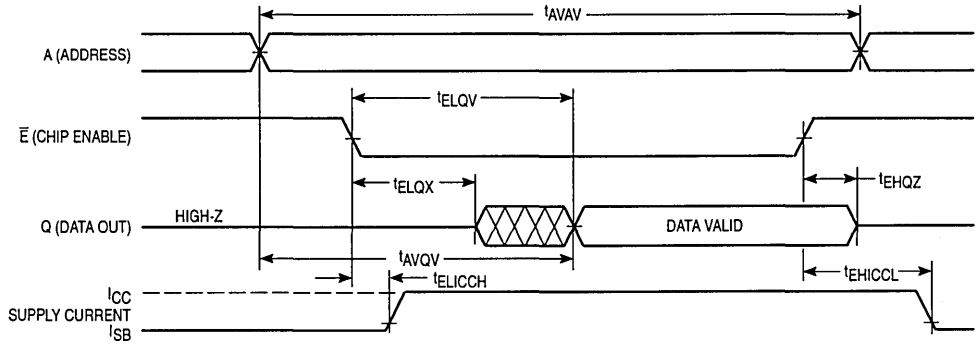
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Notes 1, 2, and 8)



READ CYCLE 2 (See Note 4)



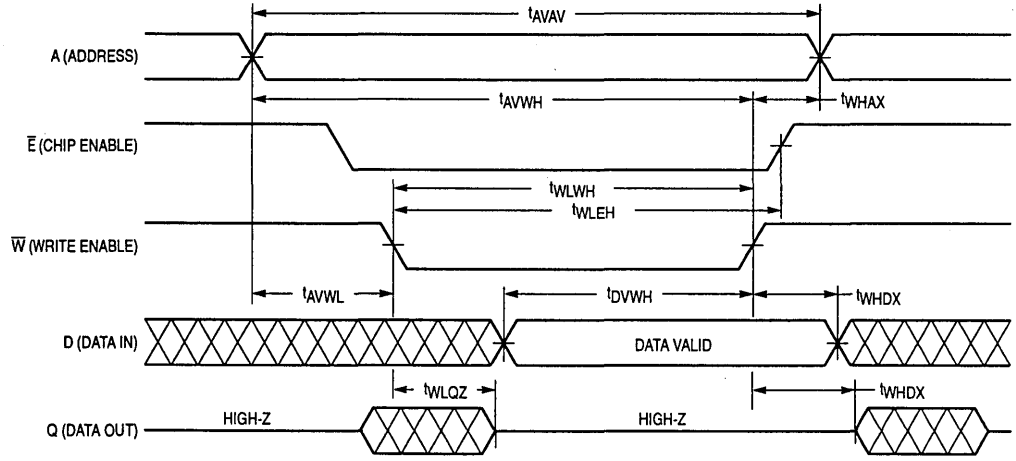
3

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		6227A-20		6227A-25		6227A-35		6227A-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	45	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	—	17	—	20	—	25	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	—	17	—	20	—	25	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	10	—	15	—	20	—	ns	
Data Hold TIme	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	9	0	10	0	15	0	20	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	t_{OW}	5	—	5	—	5	—	5	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1 and 2)

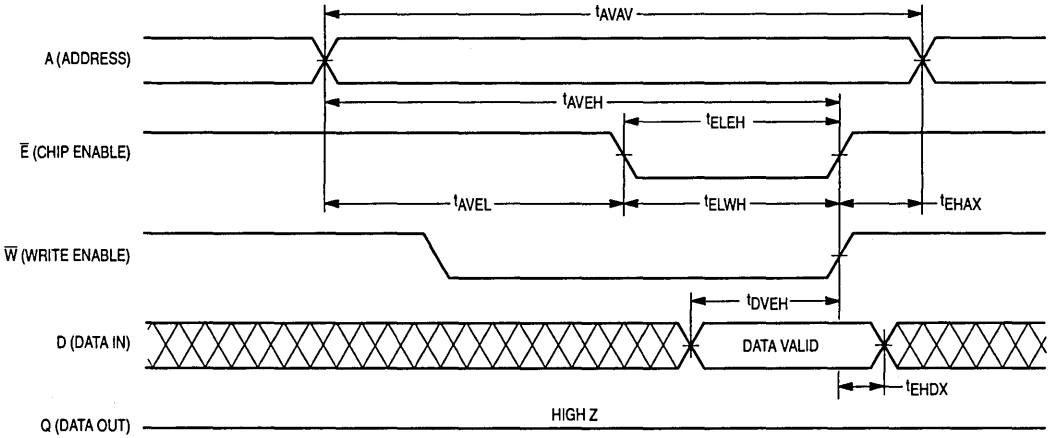


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		6227A-20		6227A-25		6227A-35		6227A-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	45	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	—	17	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	15	—	17	—	20	—	25	—	ns	4, 5
Enable to End of Write	t_{ELWH}	t_{CW}	15	—	17	—	20	—	25	—	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	15	—	17	—	20	—	25	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	—	10	—	15	—	20	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high-impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6227A WJ XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns, 45 = 45 ns)
- Package (WJ = 400 mil SOJ)

Full Part Numbers — MCM6227AWJ20, MCM6227AWJ20R2, MCM6227AWJ25, MCM6227AWJ25R2, MCM6227AWJ35, MCM6227AWJ35R2, MCM6227AWJ45, MCM6227AWJ45R2

MCM6227B

Product Preview

1M x 1 Bit Static Random Access Memory

J PACKAGE
300 MIL SOJ
CASE 810B

WJ PACKAGE
400 MIL SOJ
CASE 810

3

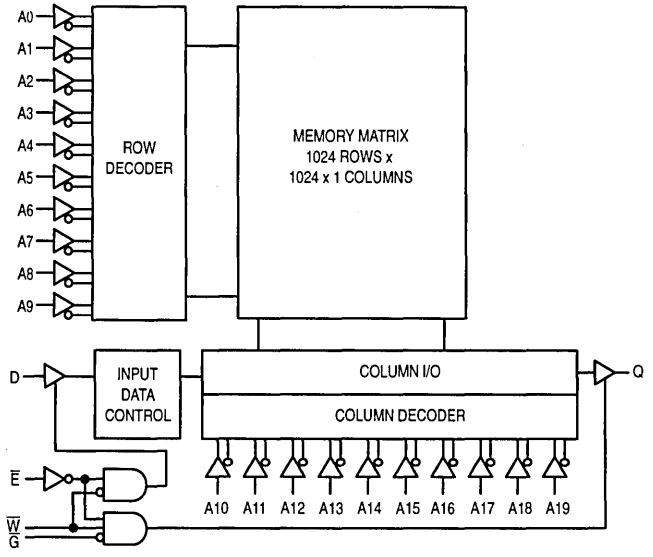
The MCM6227B is a 1,048,576 bit static random-access memory organized as 1,048,576 words of 1 bit, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6227B is each equipped with a chip enable ($\overline{E}$) pin. This feature provides reduced system power requirements without degrading access time performance.

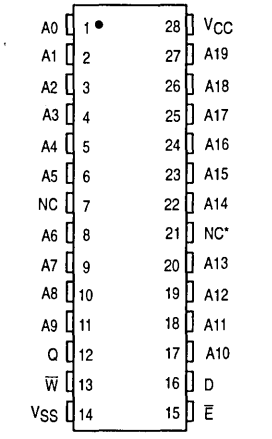
The MCM6227B is available in 300 mil and 400 mil, 28-lead surface-mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 15/17/20/25/35 ns
- Equal Address and Chip Enable Access Times
- Input and Output are TTL Compatible
- Three-State Output
- Low Power Operation: 115/110/105/100/95 mA Maximum, Active AC

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A19	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

*If not used for no connect, then do not exceed voltages of – 0.5 to V_{CC} + 0.5 V. This pin is used for manufacturing diagnostics.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	Not Selected	High-Z	—	I_{SB1}, I_{SB2}
L	H	Read	D_{out}	Read	I_{CCA}
L	L	Write	High-Z	Write	I_{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.1	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} +0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	I_{CCA}			mA
MCM6227B-15: t_{AVAV} = 15 ns		—	115	
MCM6227B-17: t_{AVAV} = 17 ns		—	110	
MCM6227B-20: t_{AVAV} = 20 ns		—	105	
MCM6227B-25: t_{AVAV} = 25 ns		—	100	
MCM6227B-35: t_{AVAV} = 35 ns		—	95	
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, f = f_{max})	I_{SB1}			mA
MCM6227B-15: t_{AVAV} = 15 ns		—	35	
MCM6227B-17: t_{AVAV} = 17 ns		—	35	
MCM6227B-20: t_{AVAV} = 20 ns		—	30	
MCM6227B-25: t_{AVAV} = 25 ns		—	25	
MCM6227B-35: t_{AVAV} = 35 ns		—	20	
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)	I_{SB2}	—	—	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and D, Q $\overline{E}$ and $\overline{W}$	C_{in}	4 5	6 8	pF
Input and Output Capacitance	D, Q	C_{in}, C_{out}	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		6227B-15		6227B-17		6227B-20		6227B-25		6227B-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	15	—	17	—	20	—	25	—	35	—	ns	2, 3
Address Access Time	t_{AVQV}	t_{AA}	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	15	—	17	—	20	—	25	—	35	ns	4
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	—	5	—	5	—	5	—	5	—	ns	5, 6, 7
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \leq V_{IL}$).

AC TEST LOADS

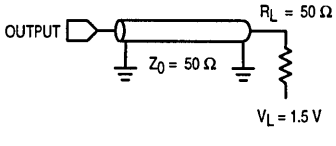


Figure 1A

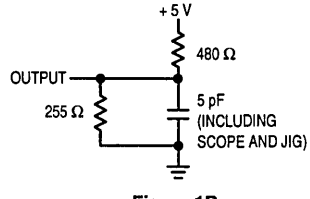
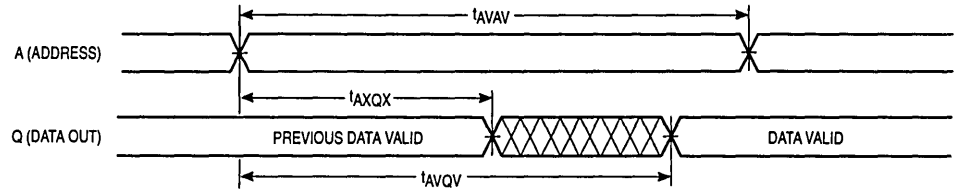


Figure 1B

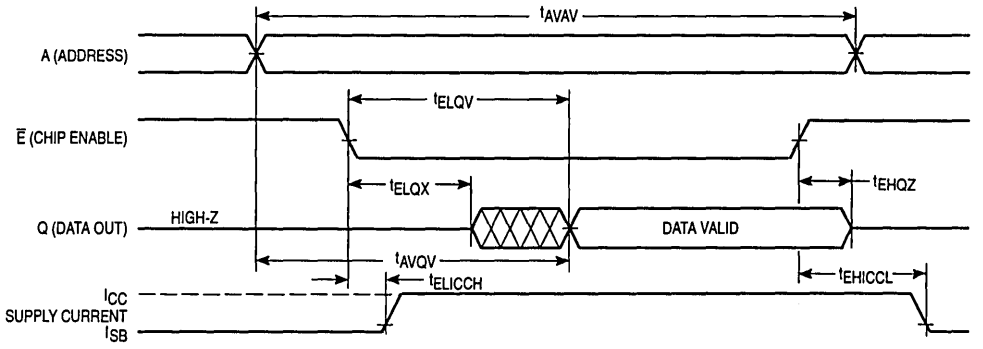
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, and 8)



READ CYCLE 2 (See Note 4)



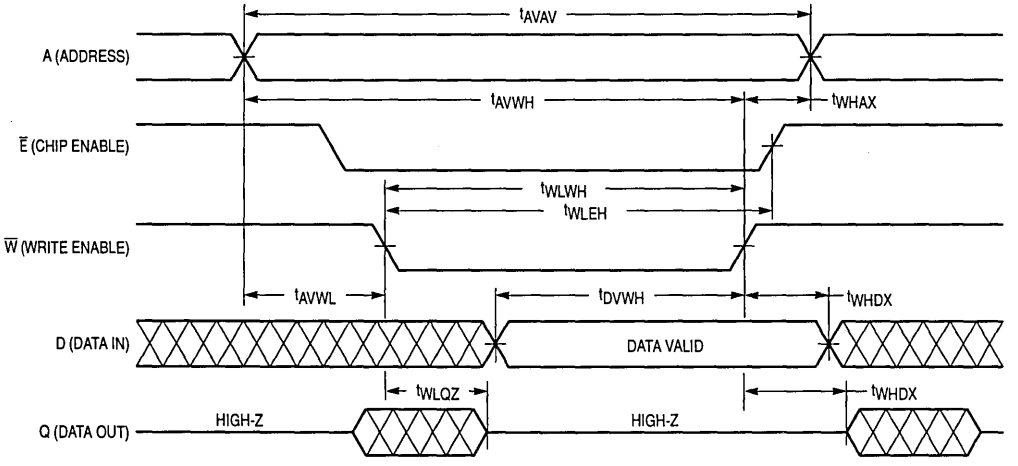
3

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		6227B-15		6227B-17		6227B-20		6227B-25		6227B-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	17	—	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	12	—	14	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold TIme	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	6	0	7	0	7	0	8	0	8	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	t_{OW}	5	—	5	—	5	—	5	—	5	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1 and 2)

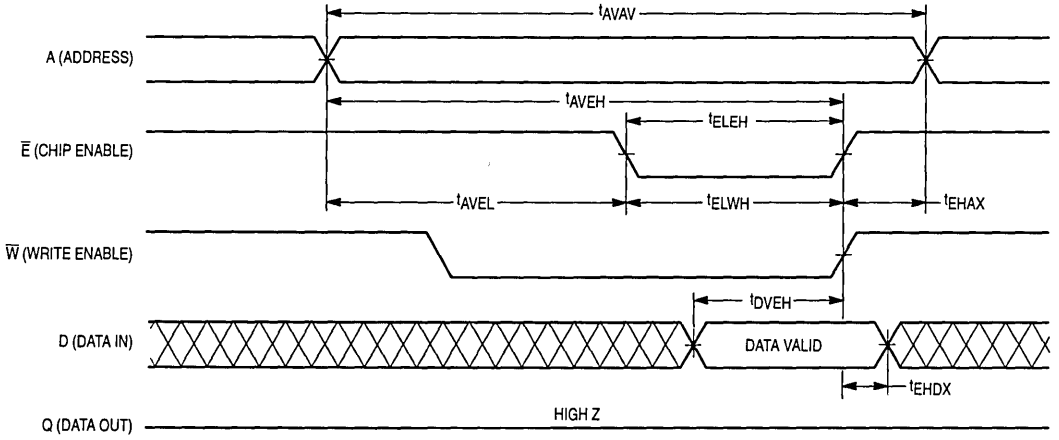


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

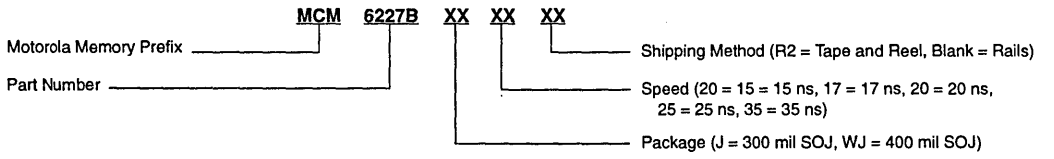
Parameter	Symbol		6227B-15		6227B-17		6227B-20		6227B-25		6227B-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	17	—	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	12	—	14	—	15	—	17	—	20	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	10	—	11	—	12	—	15	—	20	—	ns	4, 5
Enable to End of Write	t_{ELWH}	t_{CW}	10	—	11	—	12	—	15	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high-impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers —

MCM6227BJ15	MCM6227BJ15R2
MCM6227BJ17	MCM6227BJ17R2
MCM6227BJ20	MCM6227BJ20R2
MCM6227BJ25	MCM6227BJ25R2
MCM6227BJ35	MCM6227BJ35R2
MCM6227BWJ15	MCM6227BWJ15R2
MCM6227BWJ17	MCM6227BWJ17R2
MCM6227BWJ20	MCM6227BWJ20R2
MCM6227BWJ25	MCM6227BWJ25R2
MCM6227BWJ35	MCM6227BWJ35R2

3

MCM6229A

256K x 4 Bit Static Random Access Memory

The MCM6229A is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

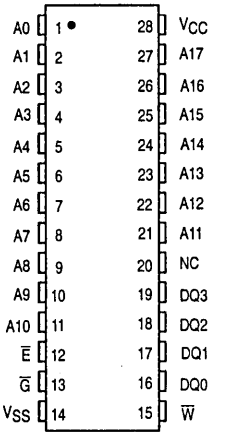
The MCM6229A is equipped with both chip enable ($\overline{E}$) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems.

The MCM6229A is available in 400 mil, 28-lead surface-mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times:20, 25, 35, and 45 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three-State Outputs
- Low Power Operation: 170/150/140/130 mA Maximum, Active AC

WJ PACKAGE
400 MIL SOJ
CASE 810

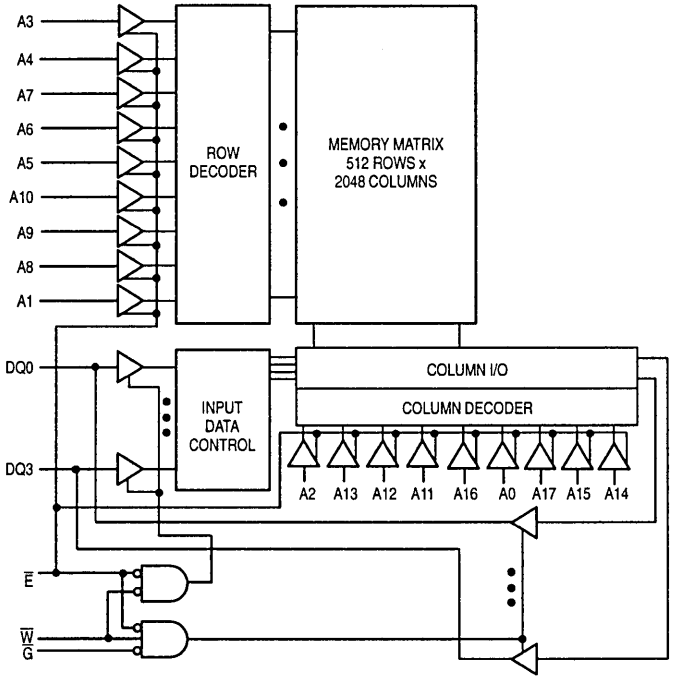
PIN ASSIGNMENT



PIN NAMES

A0 – A17	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0 – DQ3	Data Inputs/Outputs
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High-Z	—	I_{SB1}, I_{SB2}
L	H	H	Output Disabled	High-Z	—	I_{CCA}
L	L	H	Read	D_{out}	Read	I_{CCA}
L	X	L	Write	D_{in}	Write	I_{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.1	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ*	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	I_{CCA}				mA
MCM6229A-20: t_{AVAV} = 20 ns		—	140	170	
MCM6229A-25: t_{AVAV} = 25 ns		—	120	150	
MCM6229A-35: t_{AVAV} = 35 ns		—	110	140	
MCM6229A-45: t_{AVAV} = 45 ns		—	100	130	
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, f = f_{max})	I_{SB1}	—	7	20	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)	I_{SB2}	—	4	15	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

*Typical measurements are taken at 25°C, V_{CC} = 5 V.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQ	C_{in}	4	6	pF
	$\overline{E}$, $\overline{G}$, and $\overline{W}$	C_{ck}	5	8	
Input/Output Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		6229A-20		6229A-25		6229A-35		6229A-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	—	25	—	35	—	45	—	ns	2,3
Address Access Time	t_{AVQV}	t_{AA}	—	20	—	25	—	35	—	45	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	20	—	25	—	35	—	45	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	8	—	10	—	15	—	15	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{ELZ}	5	—	5	—	5	—	5	—	ns	5,6,7
Output Enable Low to Output Active	t_{GLQX}	t_{GLZ}	0	—	0	—	0	—	0	—	ns	5,6,7
Enable High to Output High-Z	t_{EHQZ}	t_{EHZ}	0	9	0	10	0	12	0	15	ns	5,6,7
Output Enable High to Output High-Z	t_{GHQZ}	t_{ELZ}	0	9	0	10	0	12	0	15	ns	5,6,7
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	20	—	25	—	35	—	45	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

AC TEST LOADS

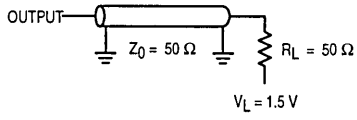


Figure 1A

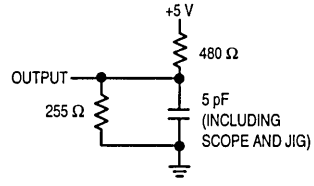


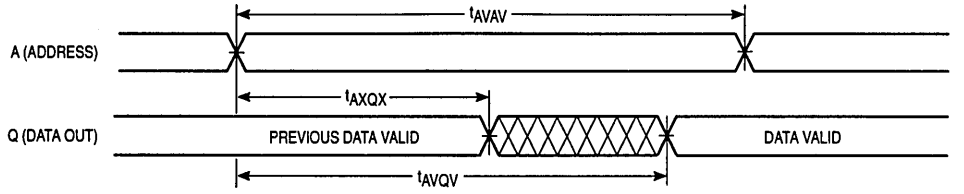
Figure 1B

TIMING LIMITS

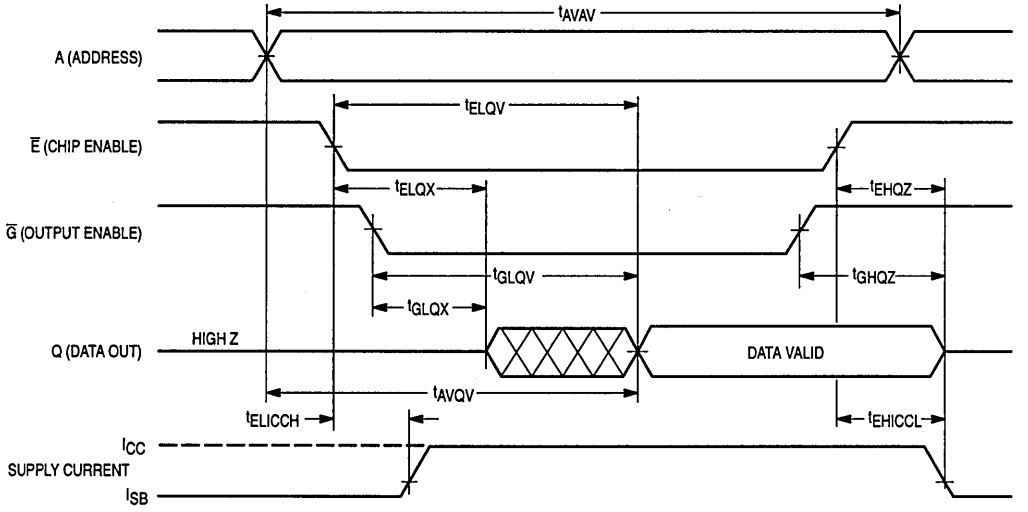
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Notes 1, 2, and 8)



READ CYCLE 2 (See Note 8)

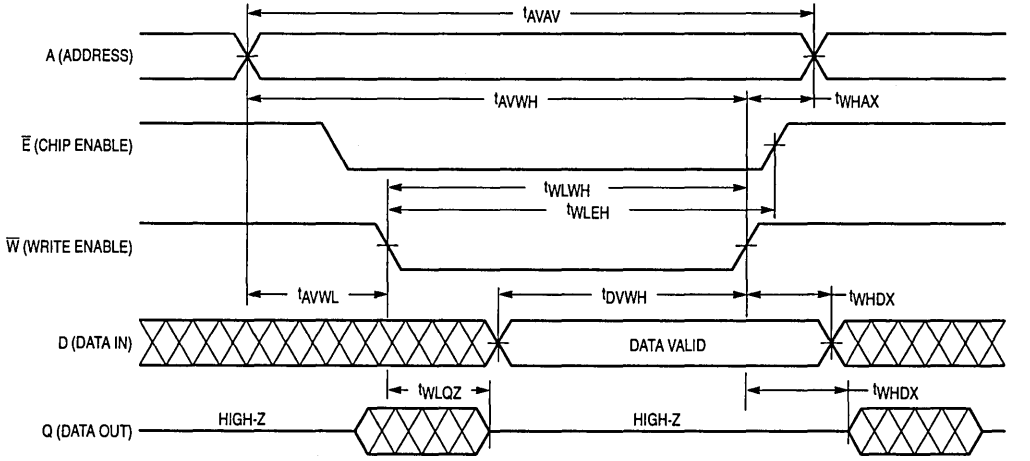


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		6229A-20		6229A-25		6229A-35		6229A-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	45	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	—	17	—	20	—	25	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	—	17	—	20	—	25	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	10	—	15	—	20	—	ns	
Data Hold TIme	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	9	0	10	0	15	0	20	ns	5,6,7
Write High to Output Active	t_{WHQX}	t_{OW}	5	—	5	—	5	—	5	—	ns	5,6,7
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1, 2, and 3)

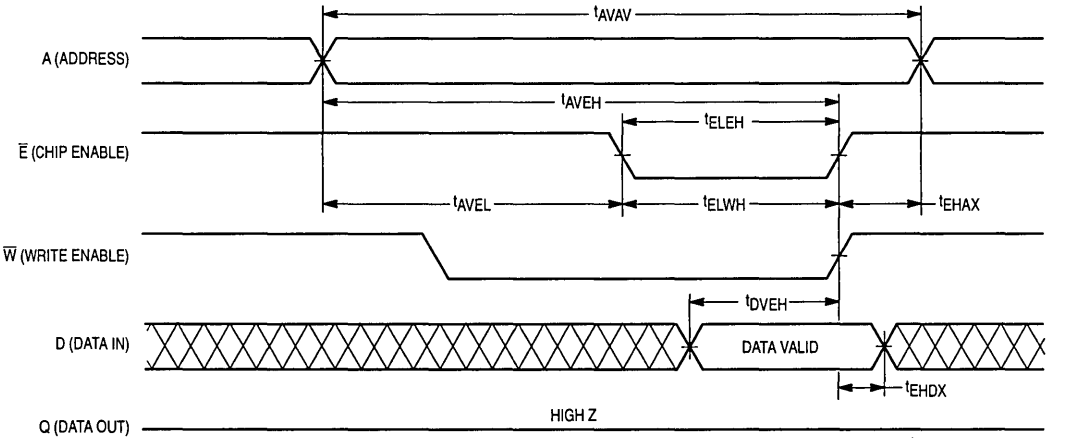


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		6229A-20		6229A-25		6229A-35		6229A-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	45	—	ns	4
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	—	17	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	15	—	17	—	20	—	25	—	ns	5, 6
Enable to End of Write	t_{ELWH}	t_{CW}	15	—	17	—	20	—	25	—	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	15	—	17	—	20	—	25	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	—	10	—	15	—	20	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high-impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1, 2, and 3)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6229A WJ XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns, 45 = 45 ns)
- Package (WJ = 400 mil SOJ)

Full Part Numbers — MCM6229AWJ20, MCM6229AWJ20R2, MCM6229AWJ25, MCM6229AWJ25R2, MCM6229AWJ35, MCM6229AWJ35R2, MCM6229AWJ45, MCM6229AWJ45R2

MCM6229B

Product Preview

256K x 4 Bit Static Random Access Memory

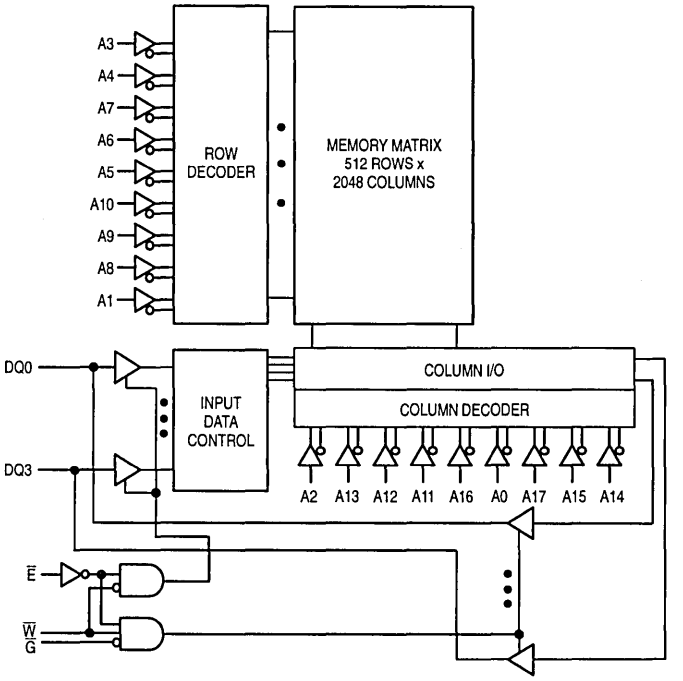
The MCM6229B is a 1,048,576 bit static random access memory organized as 262,144 words of 4 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

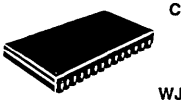
The MCM6229B is equipped with both chip enable ($\overline{E}$) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs to high impedance.

The MCM6229B is available in 300 mil and 400 mil, 28-lead surface-mount SOJ packages.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 15/17/20/25/35 ns
- Equal Address and Chip Enable Access Times
- All Inputs and Outputs are TTL Compatible
- Three-State Outputs
- Low Power Operation: 120/115/110/105/100 mA Maximum, Active AC

BLOCK DIAGRAM



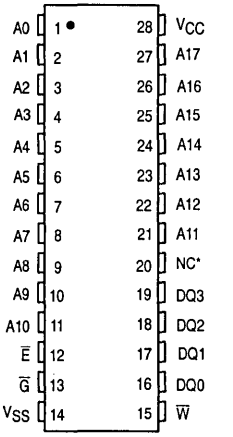


J PACKAGE
300 MIL SOJ
CASE 810B

WJ PACKAGE
400 MIL SOJ
CASE 810

3

PIN ASSIGNMENT



PIN NAMES

A0 – A17	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0 – DQ3	Data Inputs/Outputs
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

*If not used for no connect, then do not exceed voltages of – 0.5 to V_{CC} + 0.5 V. This pin is used for manufacturing diagnostics.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High-Z	—	I_{SB1}, I_{SB2}
L	H	H	Output Disabled	High-Z	—	I_{CCA}
L	L	H	Read	D_{out}	Read	I_{CCA}
L	X	L	Write	D_{in}	Write	I_{CCA}

H = High, L = Low, X = Don't Care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.1	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns).
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns).

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	I_{CCA}			mA
MCM6229B-15: t_{AVAV} = 15 ns		—	120	
MCM6229B-17: t_{AVAV} = 17 ns		—	115	
MCM6229B-20: t_{AVAV} = 20 ns		—	110	
MCM6229B-25: t_{AVAV} = 25 ns		—	100	
MCM6229B-35: t_{AVAV} = 35 ns		—	95	
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, f = f_{max})	I_{SB1}			mA
MCM6229B-15: t_{AVAV} = 15 ns		—	35	
MCM6229B-17: t_{AVAV} = 17 ns		—	35	
MCM6229B-20: t_{AVAV} = 20 ns		—	30	
MCM6229B-25: t_{AVAV} = 25 ns		—	25	
MCM6229B-35: t_{AVAV} = 35 ns		—	20	
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V, V_{CC} = max, f = 0 MHz)	I_{SB2}	—	15	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs except Clocks & DQs $\overline{E}$, $\overline{G}$, and $\overline{W}$	C_{in} C_{ck}	4 5	6 8	pF
Input/Output Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		6229B-15		6229B-17		6229B-20		6229B-25		6229B-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	15	—	17	—	20	—	25	—	35	—	ns	2, 3
Address Access Time	t_{AVQV}	t_{AA}	—	15	—	17	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	15	—	17	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	6	—	7	—	7	—	8	—	8	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{ELZ}	5	—	5	—	5	—	5	—	5	—	ns	5, 6 ,7
Output Enable Low to Output Active	t_{GLQX}	t_{GLZ}	0	—	0	—	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High-Z	t_{EHQZ}	t_{EHZ}	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7
Output Enable High to Output High-Z	t_{GHQZ}	t_{ELZ}	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

AC TEST LOADS

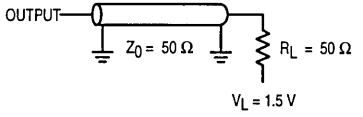


Figure 1A

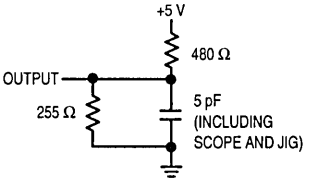
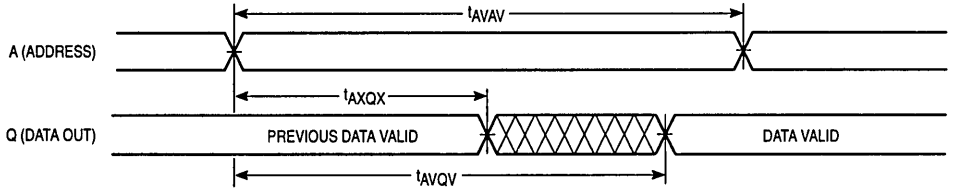


Figure 1B

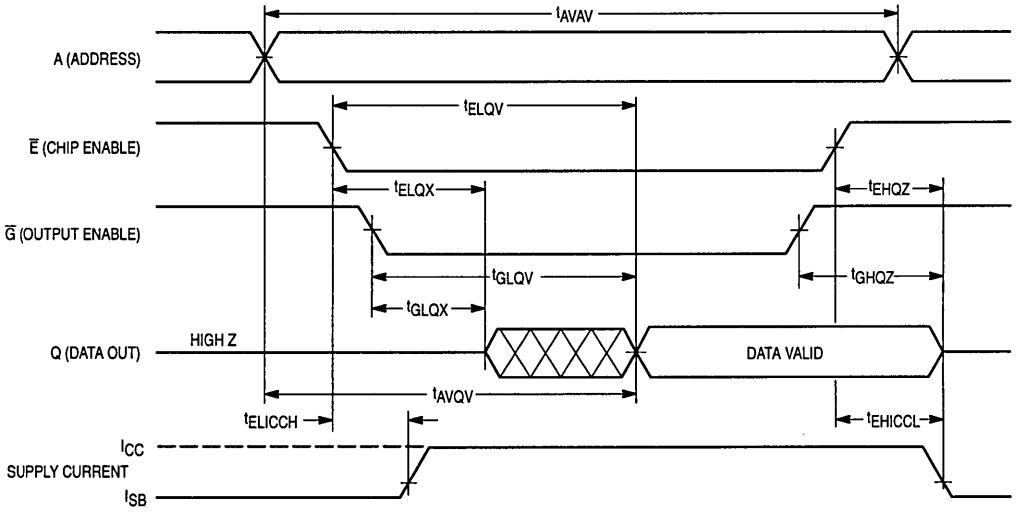
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Notes 1, 2, and 8)



READ CYCLE 2 (See Note 8)

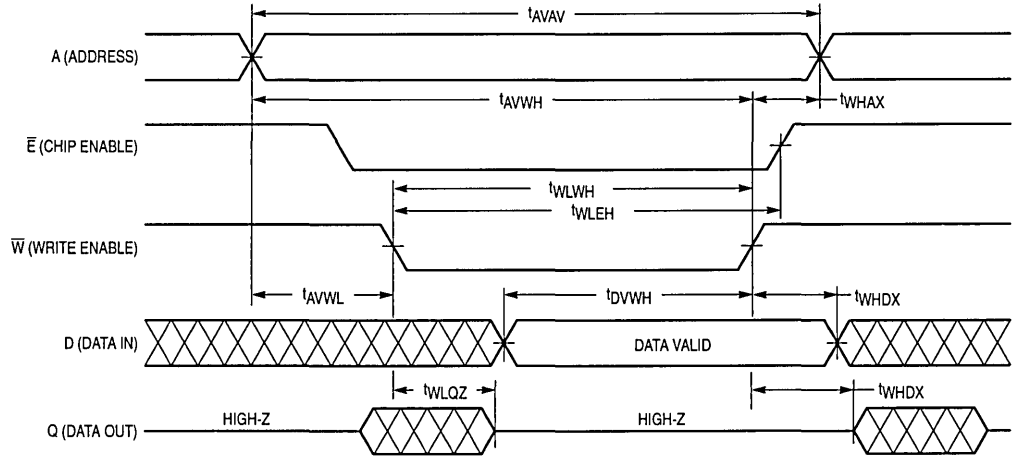


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		6229B-15		6229B-17		6229B-20		6229B-25		6229B-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	17	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	12	—	14	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	12	—	14	—	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold TIme	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	6	0	7	0	7	0	8	0	8	ns	5, 6, 7
Write High to Output Active	t_{WHQX}	t_{OW}	5	—	5	—	5	—	5	—	5	—	ns	5, 6, 7
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled See Notes 1, 2, and 3)

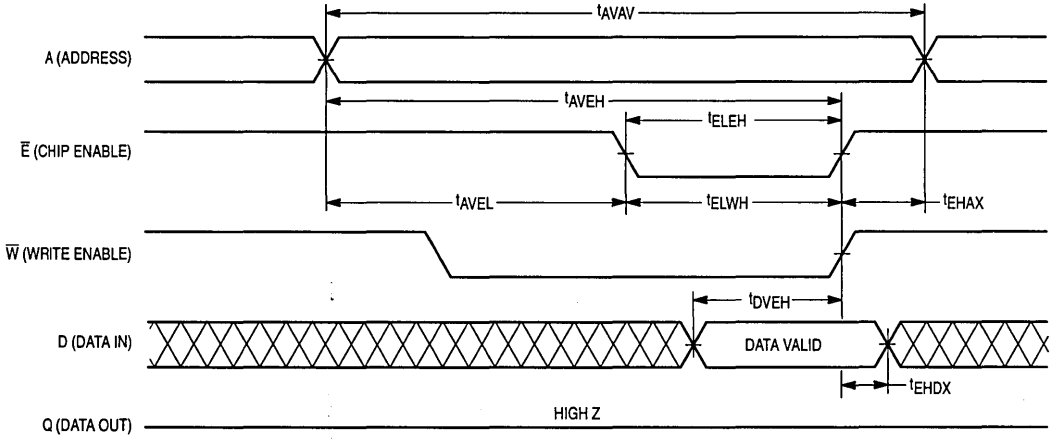


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

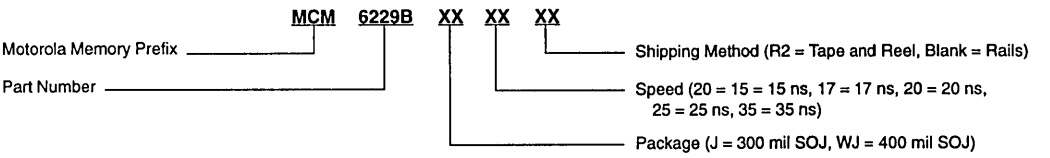
Parameter	Symbol		6229B-15		6229B-17		6229B-20		6229B-25		6229B-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	17	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	12	—	14	—	15	—	17	—	20	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	10	—	11	—	12	—	15	—	20	—	ns	5, 6
Enable to End of Write	t_{ELWH}	t_{CW}	10	—	11	—	12	—	15	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	7	—	8	—	8	—	10	—	11	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high-impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled See Notes 1, 2, and 3)



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers —		
	MCM6229BJ15	MCM6229BJ15R2
	MCM6229BJ17	MCM6229BJ17R2
	MCM6229BJ20	MCM6229BJ20R2
	MCM6229BJ25	MCM6229BJ25R2
	MCM6229BJ35	MCM6229BJ35R2
	MCM6229BWJ15	MCM6229BWJ15R2
	MCM6229BWJ17	MCM6229BWJ17R2
	MCM6229BWJ20	MCM6229BWJ20R2
	MCM6229BWJ25	MCM6229BWJ25R2
	MCM6229BWJ35	MCM6229BWJ35R2

3

MCM6246

Product Preview

512K x 8 Bit Static Random Access Memory

The MCM6246 is a 4,194,304 bit static random access memory organized as 524,288 words of 8 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

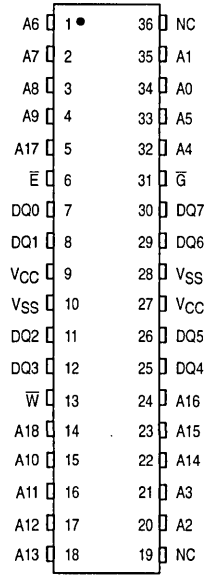
The MCM6246 is equipped with chip enable ($\overline{E}$) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs into high impedance.

The MCM6246 is available in a 400 mil, 36-lead surface-mount SOJ package.

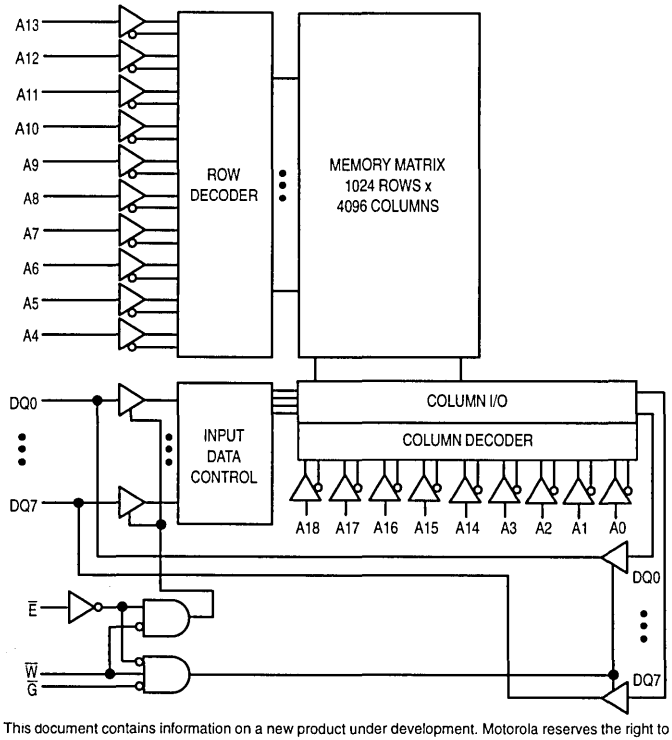
- Single 5 V ± 10% Power Supply
- Fast Access Time: 20/25/35 ns
- Equal Address and Chip Enable Access Time
- All Inputs and Outputs are TTL Compatible
- Three-State Outputs
- Power Operation: 190/170/150 mA Maximum, Active AC

WJ PACKAGE
400 MIL SOJ
CASE 893-01

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A18	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0 – DQ7	Data Input/Output
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High-Z	—	I_{SB1}, I_{SB2}
L	H	H	Output Disabled	High-Z	—	I_{CCA}
L	L	H	Read	D_{out}	Read	I_{CCA}
L	X	L	Write	High-Z	Write	I_{CCA}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	− 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	− 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	− 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	− 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	− 0.5*	—	0.8	V

* V_{IL} (min) = − 0.5 V dc; V_{IL} (min) = − 2.0 V ac (pulse width ≤ 2.0 ns).
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = − 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter		Symbol	Min	Typ	Max	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	MCM6246-20: t_{AVAV} = 20 ns	I_{CC}	—	170	190	mA
	MCM6246-25: t_{AVAV} = 25 ns		—	145	170	
	MCM6246-35: t_{AVAV} = 35 ns		—	130	150	
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, No other restrictions on other inputs)	MCM6246-20: t_{AVAV} = 20 ns	I_{SB1}	—	55	60	mA
	MCM6246-25: t_{AVAV} = 25 ns		—	45	50	
	MCM6246-35: t_{AVAV} = 35 ns		—	35	40	
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} − 0.2 V) (V_{CC} = max, f = 0 MHz)		I_{SB2}	—	10	15	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQs	C_{in}	4	6	pF
	$\overline{E}$, $\overline{G}$, $\overline{W}$	C_{ck}	5	8	
Input/Output Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Note 1)

Parameter	Symbol		MCM6246-20		MCM6246-25		MCM6246-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	—	25	—	35	—	ns	2, 3
Address Access Time	t_{AVQV}	t_{AA}	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	6	—	8	—	10	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	—	5	—	5	—	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	t_{LZ}	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	9	0	10	0	12	ns	5, 6, 7
Output Enable High to Output High-Z	t_{GHQZ}	t_{HZ}	0	9	0	10	0	12	ns	5, 6, 7
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low/$\overline{E}$ going high.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

AC TEST LOADS

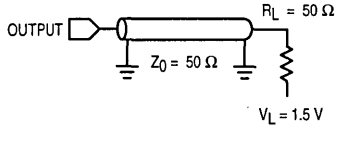


Figure 1A

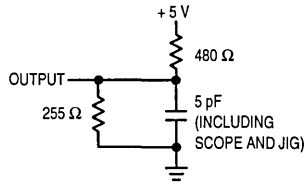
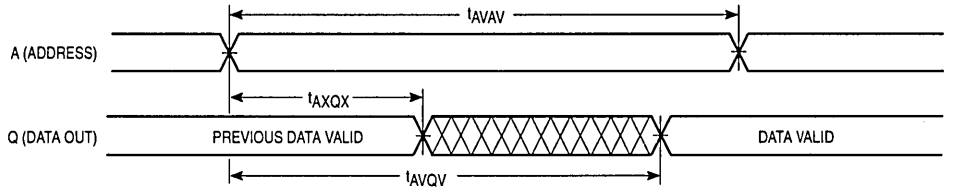


Figure 1B

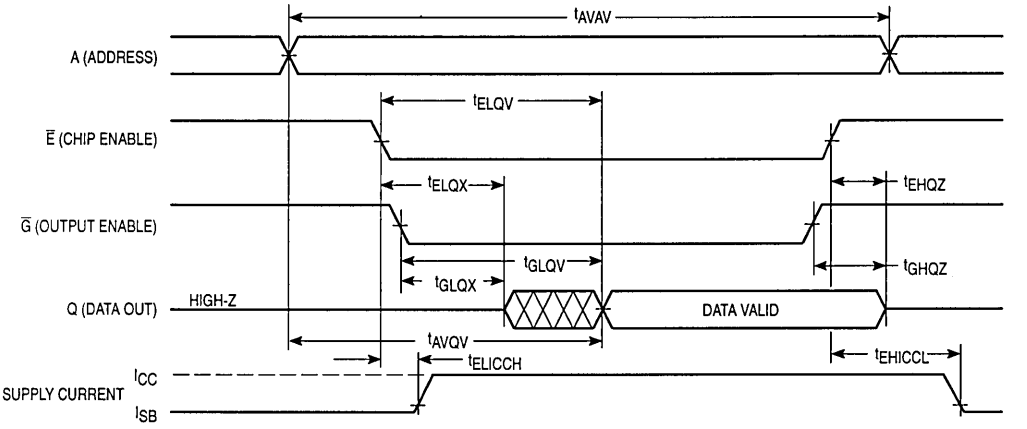
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note)



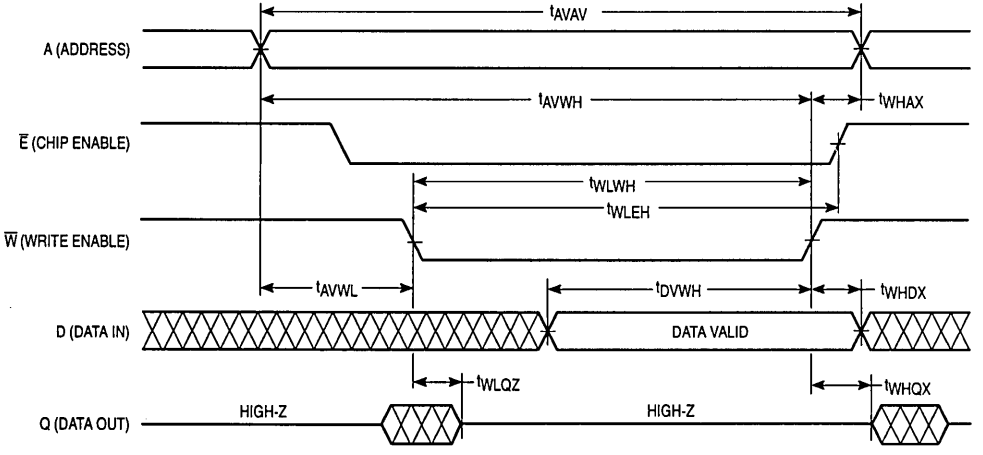
NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low/ $\overline{E}$ going high.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		MCM6246-20		MCM6246-25		MCM6246-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	9	0	10	0	15	ns	5,6,7
Write High to Output Active	t_{WHQX}	t_{OW}	5	—	5	—	5	—	ns	5,6,7
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

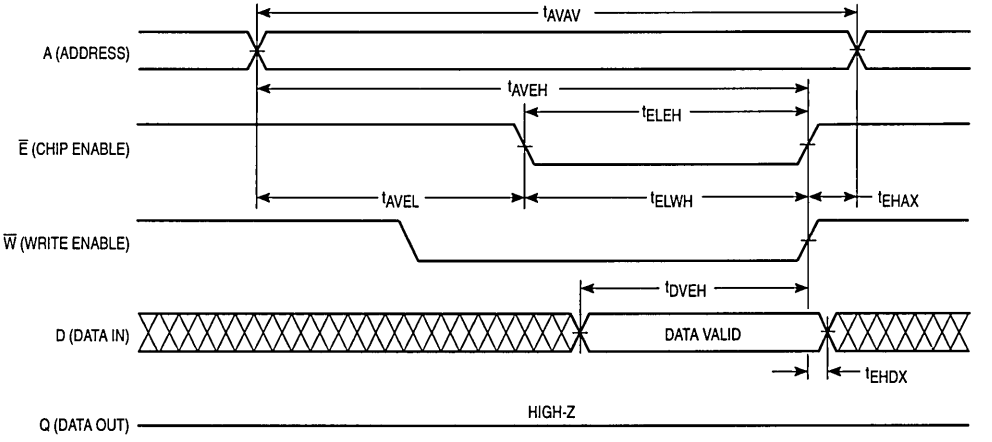


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		MCM6246-20		MCM6246-25		MCM6246-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	—	17	—	20	—	ns	
Enable Pulse Width	t_{ELEH}	t_{CP}	15	—	17	—	20	—	ns	5,6
Enable to End of Write	t_{ELWH}	t_{CW}	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	—	10	—	15	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6246 XX XX XX

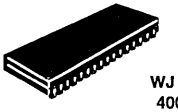
- MCM — Motorola Memory Prefix
- 6246 — Part Number
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)
- XX — Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- XX — Package (WJ = 400 mil SOJ)

Full Part Numbers — MCM6246WJ20 MCM6246WJ20R2
MCM6246WJ25 MCM6246WJ25R2
MCM6246WJ35 MCM6246WJ35R2

MCM6249

Product Preview

1M x 4 Bit Static Random Access Memory



WJ PACKAGE
400 MIL SOJ
CASE 857A

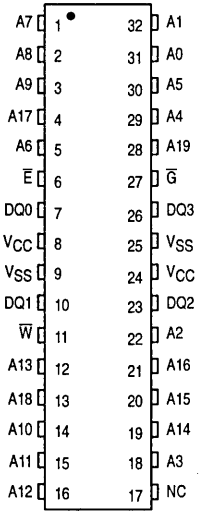
The MCM6249 is a 4,194,304 bit static random access memory organized as 1,048,576 words of 4 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM6249 is equipped with chip enable ($\overline{E}$) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs into high impedance.

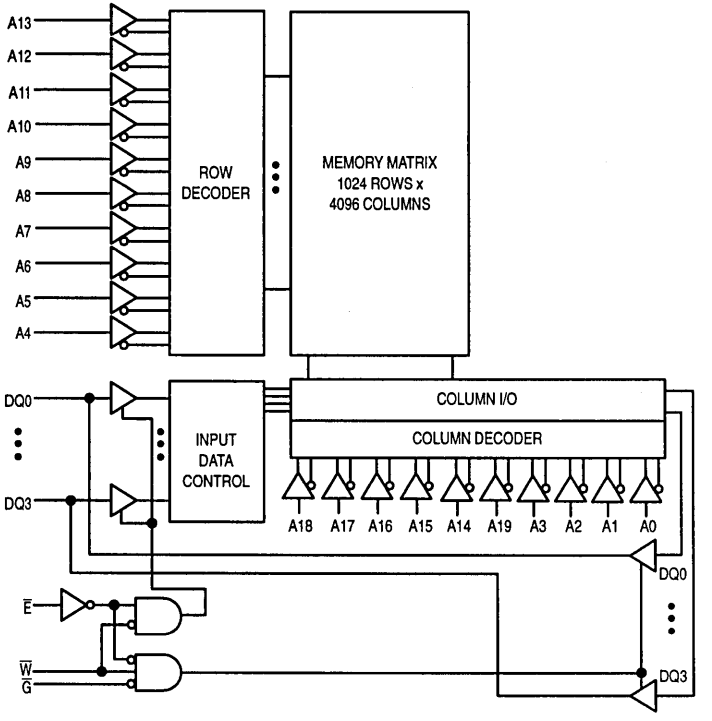
The MCM6249 is available in a 400 mil, 32-lead surface-mount SOJ package.

- Single 5 V ± 10% Power Supply
- Fast Access Time: 20/25/35 ns
- Equal Address and Chip Enable Access Time
- All Inputs and Outputs are TTL Compatible
- Three-State Outputs
- Power Operation: 180/160/140 mA Maximum, Active AC

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A19	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ0 – DQ3	Data Input/Output
NC	No Connection
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High-Z	—	I_{SB1}, I_{SB2}
L	H	H	Output Disabled	High-Z	—	I_{CCA}
L	L	H	Read	D_{out}	Read	I_{CCA}
L	X	L	Write	High-Z	Write	I_{CCA}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter		Symbol	Min	Typ	Max	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max)	MCM6249-20: t_{AVAV} = 20 ns	I_{CC}	—	165	180	mA
	MCM6249-25: t_{AVAV} = 25 ns		—	135	160	
	MCM6249-35: t_{AVAV} = 35 ns		—	120	140	
AC Standby Current (V_{CC} = max, $\overline{E}$ = V_{IH}, No other restrictions on other inputs)	MCM6249-20: t_{AVAV} = 20 ns	I_{SB1}	—	50	60	mA
	MCM6249-25: t_{AVAV} = 25 ns		—	40	50	
	MCM6249-35: t_{AVAV} = 35 ns		—	35	40	
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V) (V_{CC} = max, f = 0 MHz)		I_{SB2}	—	10	15	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQs $\overline{E}$, $\overline{G}$, $\overline{W}$	C_{in} C_{ck}	4 5	6 8	pF
Input/Output Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Note 1)

Parameter	Symbol		MCM6249-20		MCM6249-25		MCM6249-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	—	25	—	35	—	ns	2, 3
Address Access Time	t_{AVQV}	t_{AA}	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	6	—	8	—	10	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	—	5	—	5	—	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	t_{LZ}	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	9	0	10	0	12	ns	5, 6, 7
Output Enable High to Output High-Z	t_{GHQZ}	t_{HZ}	0	9	0	10	0	12	ns	5, 6, 7
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low/$\overline{E}$ going high.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

AC TEST LOADS

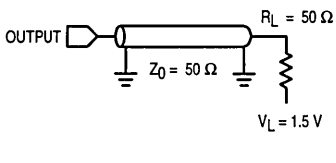


Figure 1A

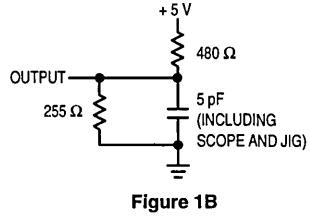
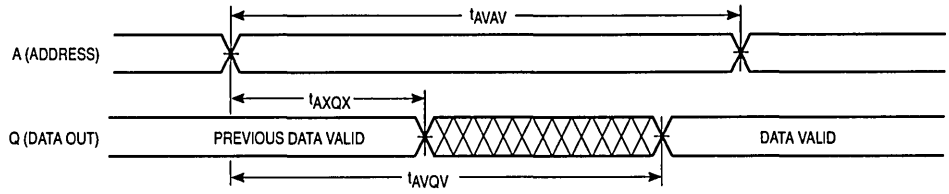


Figure 1B

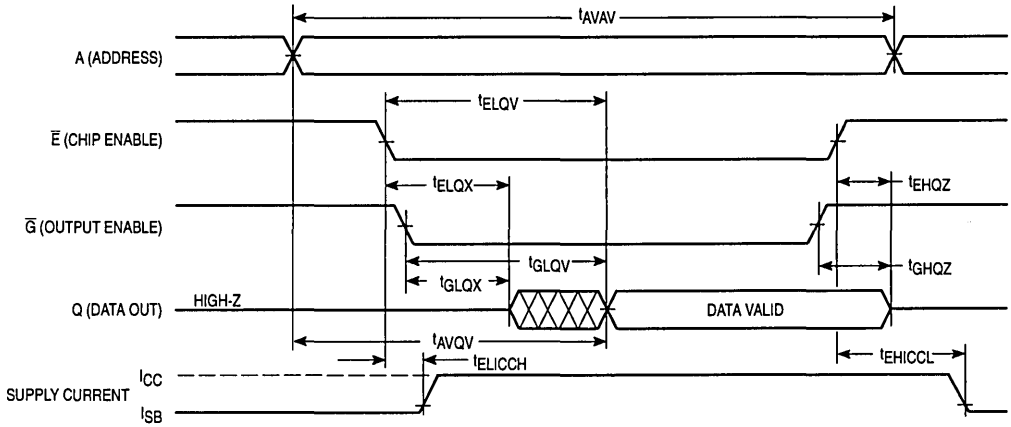
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note)



NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low/$\overline{E}$ going high.

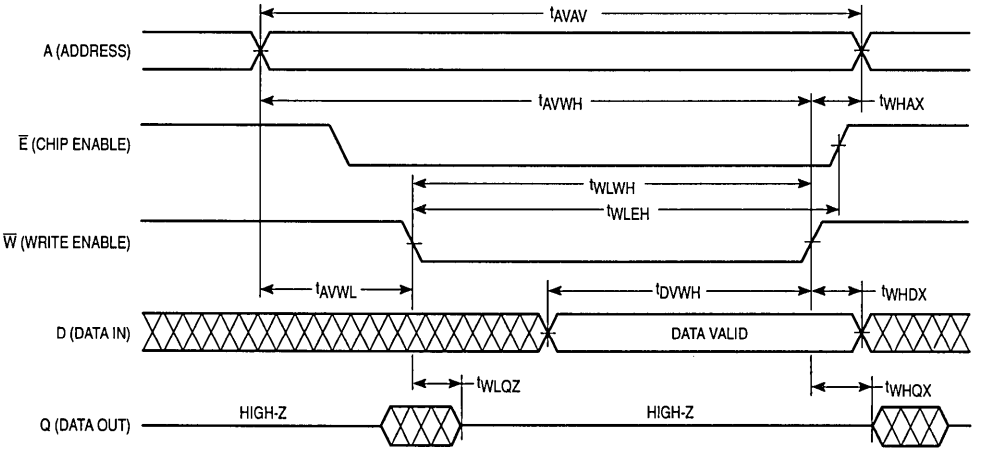
WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		MCM6249-20		MCM6249-25		MCM6249-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	9	0	10	0	15	ns	5,6,7
Write High to Output Active	t_{WHQX}	t_{OW}	5	—	5	—	5	—	ns	5,6,7
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

3

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

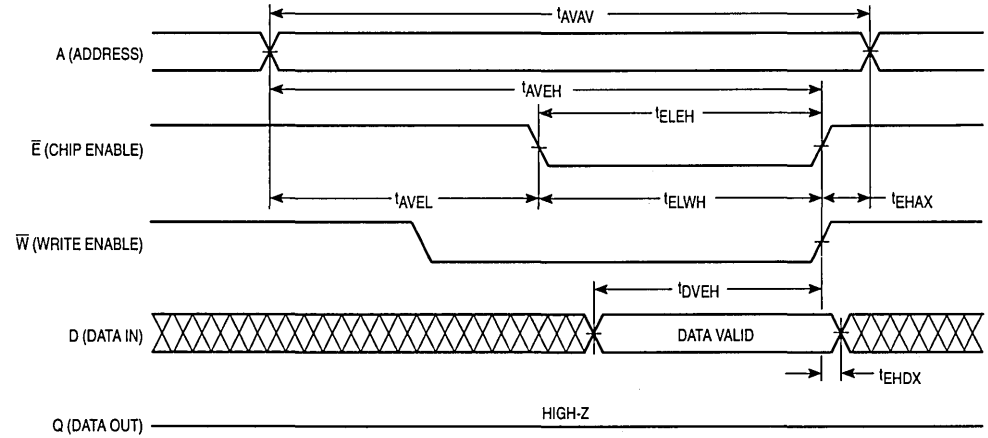


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		MCM6249-20		MCM6249-25		MCM6249-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	—	17	—	20	—	ns	
Enable Pulse Width	t_{ELEH}	t_{CP}	15	—	17	—	20	—	ns	5,6
Enable to End of Write	t_{ELWH}	t_{CW}	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	—	10	—	15	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6249 XX XX XX

- MCM — Motorola Memory Prefix
- 6249 — Part Number
- XX — Package (WJ = 400 mil SOJ)
- XX — Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6249WJ20 MCM6249WJ20R2
MCM6249WJ25 MCM6249WJ25R2
MCM6249WJ35 MCM6249WJ35R2

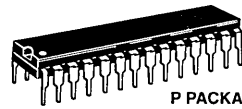
MCM6264C

8K x 8 Bit Fast Static RAM

The MCM6264C is fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

This device meets JEDEC standards for functionality and pinout, and is available in plastic dual-in-line and plastic small-outline J-leaded packages.

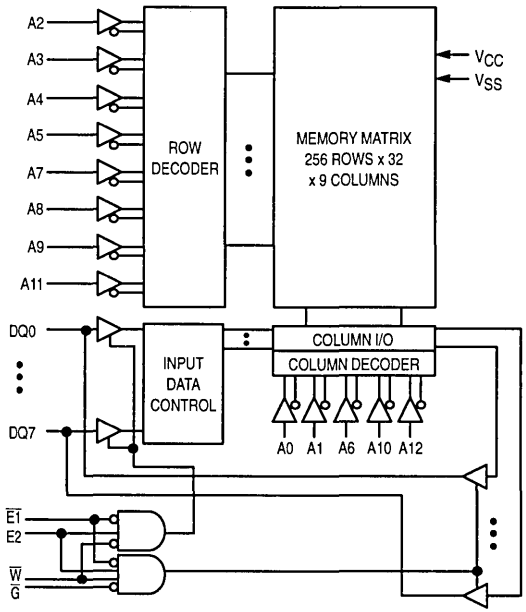
- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 12, 15, 20, 25, and 35 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Low Power Operation: 110 – 150 mA Maximum AC
- Fully TTL Compatible — Three State Output



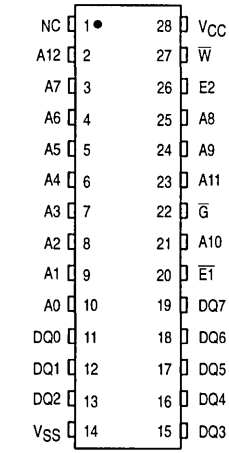
P PACKAGE
300 MIL PLASTIC
CASE 710B

J PACKAGE
300 MIL SOJ
CASE 810B

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A12	Address Input
DQ0 – DQ7	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enable
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

TRUTH TABLE (X = Don't Care)

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	H	Output Disabled	I_{CCA}	High-Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	- 12	- 15	- 20	- 25	- 35	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	150	140	130	120	110	mA
AC Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL}, V_{CC} = Max, f = f_{max})	I_{SB1}	45	40	35	30	30	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} – 0.2 V or E2 ≤ V_{SS} + 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	20	20	20	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E1}$, E2, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	$C_{I/O}$	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol		-12		-15		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	12	—	15	—	20	—	25	—	35	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	12	—	15	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	12	—	15	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	6	—	8	—	10	—	11	—	12	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	4	—	4	—	ns	5, 6 ,7
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	6	0	8	0	9	0	10	0	11	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	0	—	ns	5, 6, 7
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	6	0	7	0	8	0	9	0	10	ns	5, 6, 7
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	12	—	15	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} (max) is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

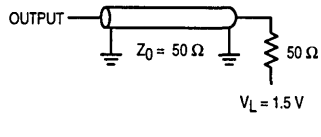


Figure 1A

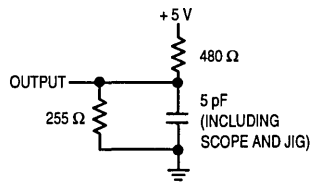


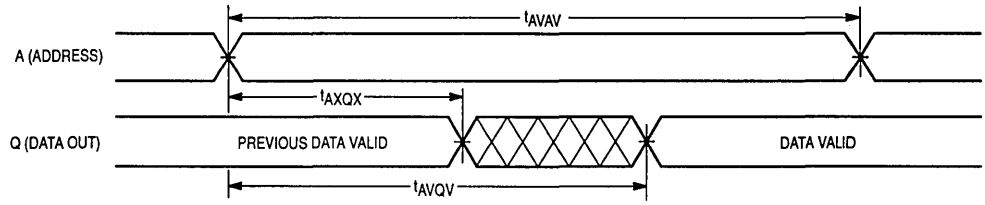
Figure 1B

TIMING LIMITS

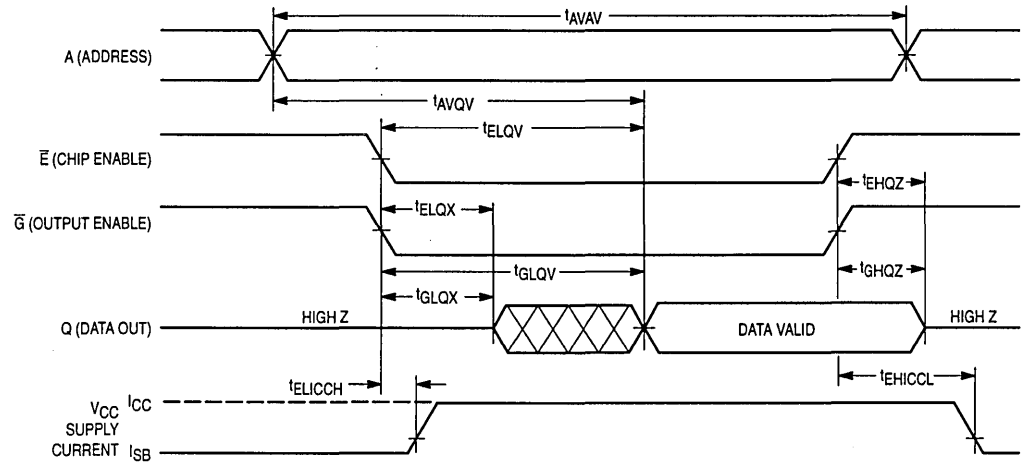
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note 4)



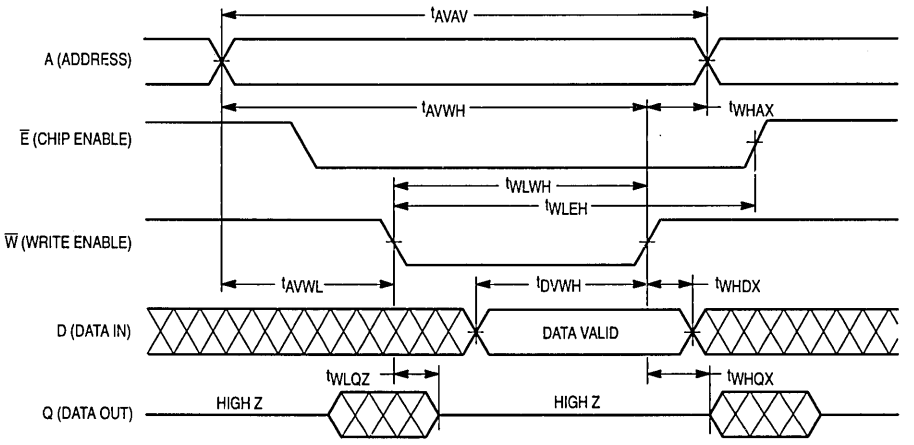
3

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		-12		-15		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	12	—	15	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	10	—	12	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	10	—	12	—	15	—	17	—	20	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	t_{WP}	8	—	10	—	12	—	15	—	17	—	ns	5
Data Valid to End of Write	t_{DVWH}	t_{DW}	6	—	7	—	8	—	10	—	12	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	6	0	7	0	8	0	10	0	12	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	4	—	4	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
6. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)



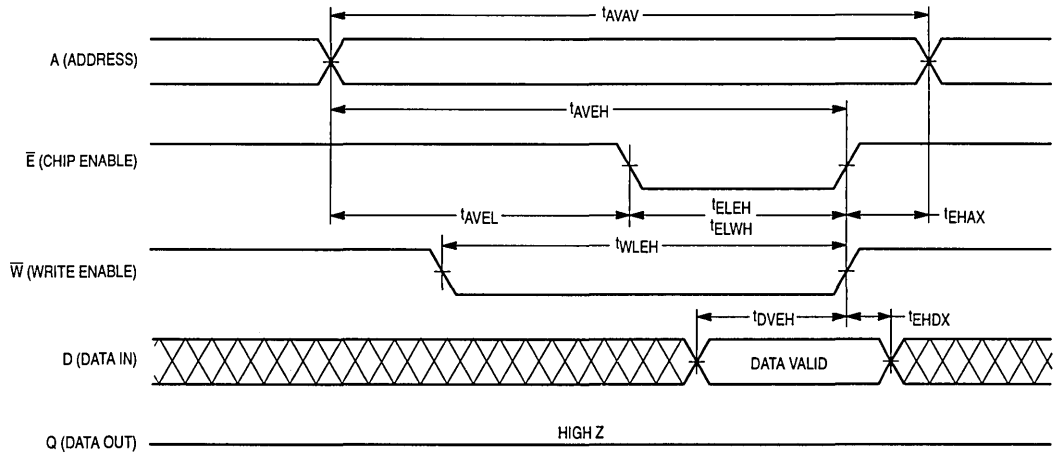
WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		-12		-15		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	12	—	15	—	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	12	—	12	—	15	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	10	—	10	—	12	—	15	—	25	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	t_{DW}	7	—	7	—	8	—	10	—	15	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

3

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6264C X XX XX

- MCM — Motorola Memory Prefix
- 6264C — Part Number
- X — Package (P = 300 mil Plastic, J = 300 mil SOJ)
- XX — Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers —

MCM6264CP12	MCM6264CJ12	MCM6264CJ12R2
MCM6264CP15	MCM6264CJ15	MCM6264CJ15R2
MCM6264CP20	MCM6264CJ20	MCM6264CJ20R2
MCM6264CP25	MCM6264CJ25	MCM6264CJ25R2
MCM6264CP35	MCM6264CJ35	MCM6264CJ35R2

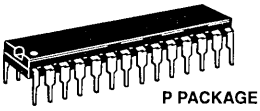
MCM6265C

8K x 9 Bit Fast Static RAM

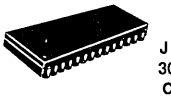
The MCM6265C is fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

This device meets JEDEC standards for functionality and pinout, and is available in plastic dual-in-line and plastic small-outline J-leaded packages.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 12, 15, 20, 25, and 35 ns
- Equal Address and Chip Enable Access Times
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- Low Power Operation: 110 – 150 mA Maximum AC
- Fully TTL Compatible — Three State Output

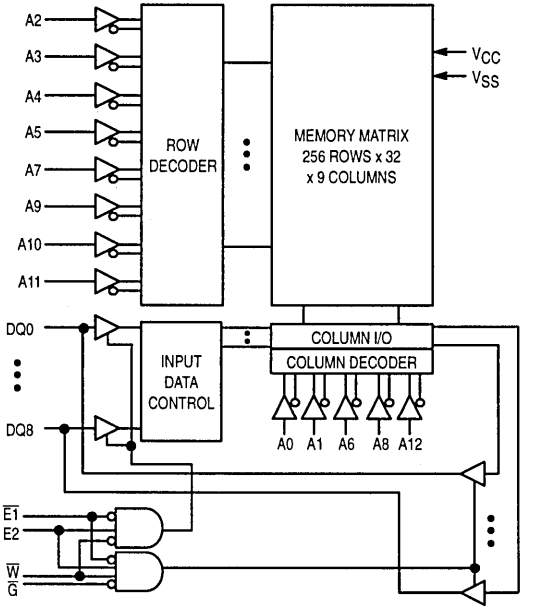


P PACKAGE
300 MIL PLASTIC
CASE 710B

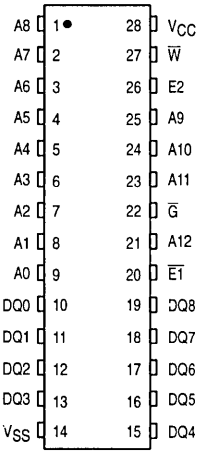


J PACKAGE
300 MIL SOJ
CASE 810B

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0 – A12	Address Input
DQ0 – DQ8	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$, E2	Chip Enable
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

TRUTH TABLE (X = Don't Care)

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	H	Output Disabled	I_{CCA}	High-Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	− 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	− 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	− 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	− 0.5*	—	0.8	V

*V_{IL} (min) = − 0.5 V dc; V_{IL} (min) = − 2.0 V ac (pulse width ≤ 20 ns)

** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1	µA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1	µA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = − 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	- 12	- 15	- 20	- 25	- 35	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	150	140	130	120	110	mA
AC Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL}, V_{CC} = Max, f = f_{max})	I_{SB1}	45	40	35	30	30	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} − 0.2 V or E2 ≤ V_{SS} + 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} − 0.2 V)	I_{SB2}	20	20	20	20	20	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E1}$, E2, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	$C_{I/O}$	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol		-12		-15		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	12	—	15	—	20	—	25	—	35	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	12	—	15	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	12	—	15	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	6	—	8	—	10	—	11	—	12	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	4	—	4	—	ns	5,6,7
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	6	0	8	0	9	0	10	0	11	ns	5,6,7
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	0	—	ns	5,6,7
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	6	0	7	0	8	0	9	0	10	ns	5,6,7
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	12	—	15	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} (max) is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

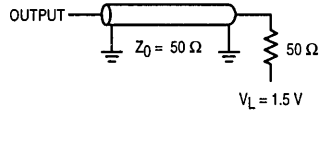


Figure 1A

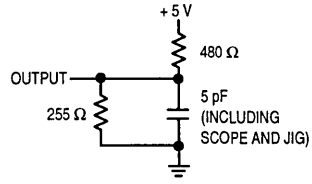


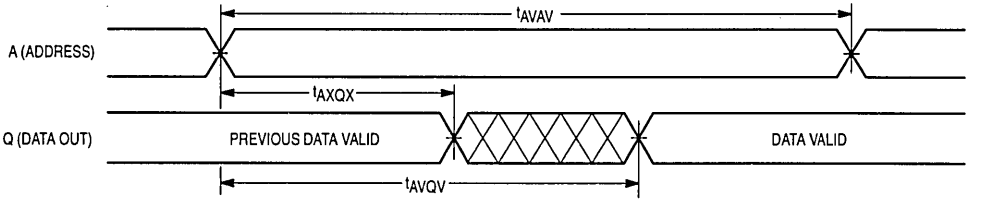
Figure 1B

TIMING LIMITS

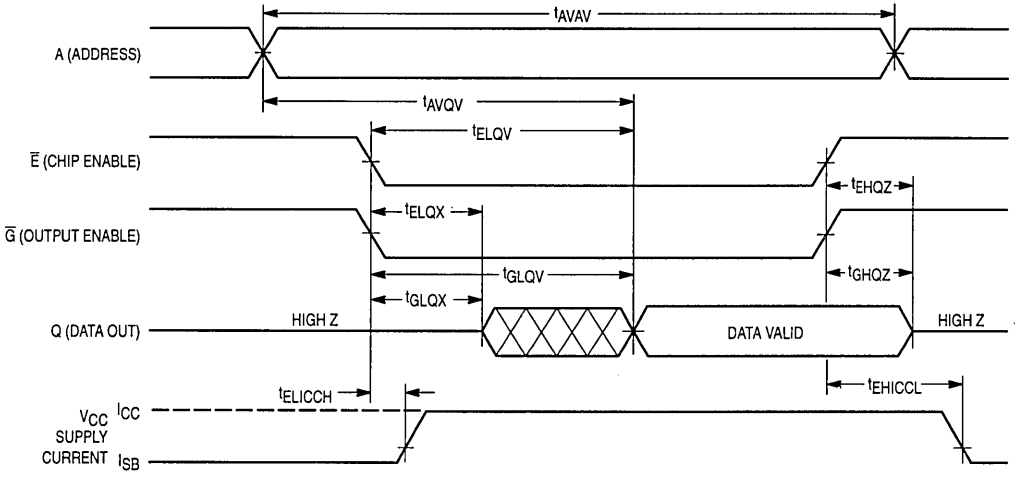
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note 4)

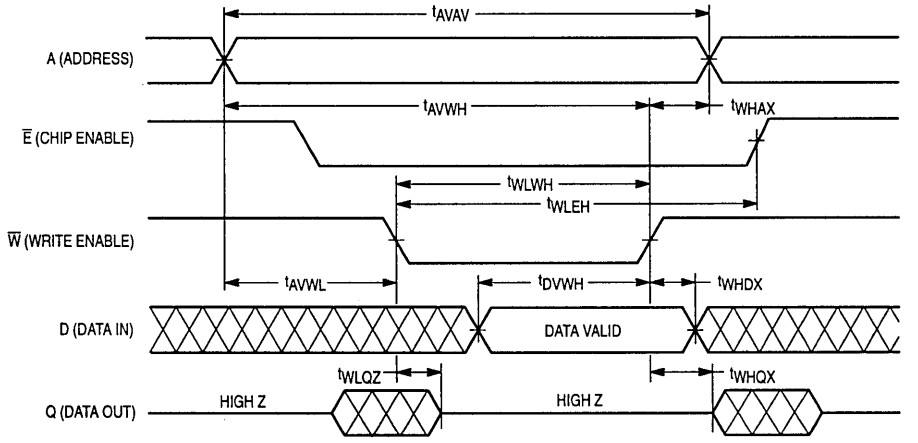


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		-12		-15		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	12	—	15	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	10	—	12	—	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	10	—	12	—	15	—	17	—	20	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	t_{WP}	8	—	10	—	12	—	15	—	17	—	ns	5
Data Valid to End of Write	t_{DVWH}	t_{DW}	6	—	7	—	8	—	10	—	12	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	6	0	7	0	8	0	10	0	12	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	4	—	4	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
6. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)



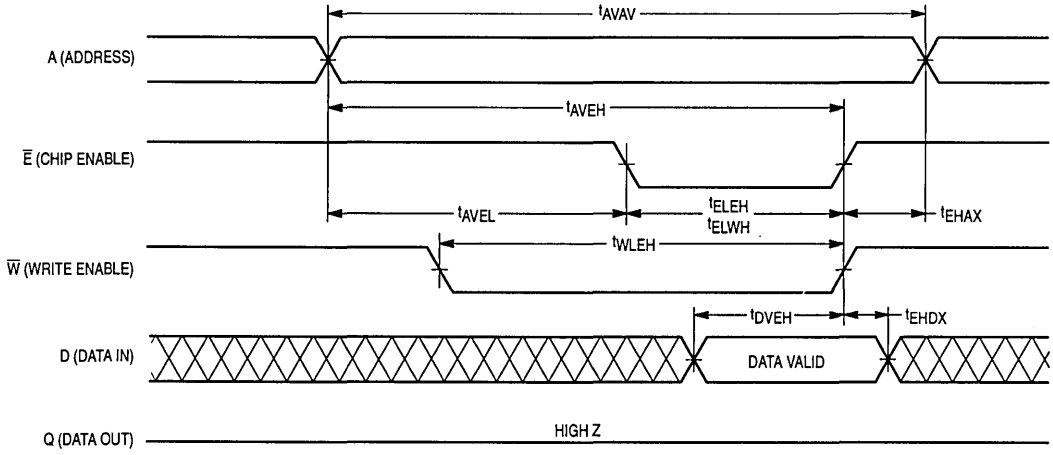
WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		-12		-15		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	12	—	15	—	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	12	—	12	—	15	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	10	—	10	—	12	—	15	—	25	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	t_{DW}	7	—	7	—	8	—	10	—	15	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

3

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6265C X XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- Package (P = 300 mil Plastic DIP, J = 300 mil SOJ)

Full Part Numbers —			
	MCM6265CP12	MCM6265CJ12	MCM6265CJ12R2
	MCM6265CP15	MCM6265CJ15	MCM6265CJ15R2
	MCM6265CP20	MCM6265CJ20	MCM6265CJ20R2
	MCM6265CP25	MCM6265CJ25	MCM6265CJ25R2
	MCM6265CP35	MCM6265CJ35	MCM6265CJ35R2

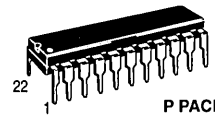
MCM6287B

64K x 1 Bit Fast Static RAM

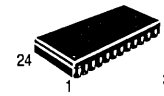
The MCM6287B is fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

This device meets JEDEC standards for functionality and pinout, and is available in plastic dual-in-line and plastic small-outline J-leaded packages.

- Single 5 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 12, 15, 20, 25, and 35 ns
- Equal Address and Chip Enable Access Times
- Low Power Operation: 110 – 150 mA Maximum AC
- Fully TTL-Compatible — Three-State Output
- Separate Data Input and Output

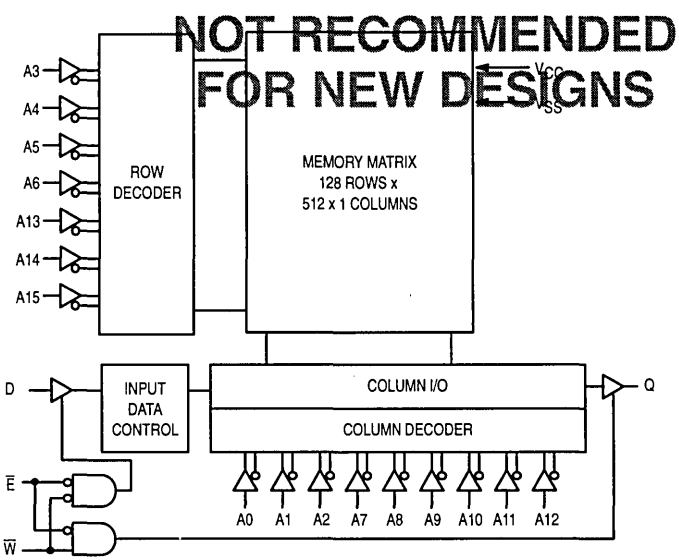


P PACKAGE
300 MIL PLASTIC
CASE 736A



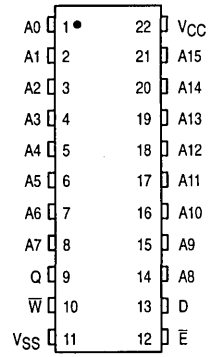
J PACKAGE
300 MIL SOJ
CASE 810A

BLOCK DIAGRAM

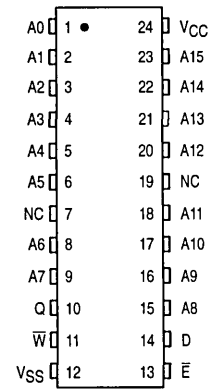


PIN ASSIGNMENTS

DUAL-IN-LINE



SOJ



PIN NAMES	
A0 – A15 ..... Address Input	Q ..... Data Output
E ..... Chip Enable	VCC ..... + 5 V Power Supply
W ..... Write Enable	VSS ..... Ground
D ..... Data Input	NC ..... No Connection

TRUTH TABLE (X = Don't Care)

$\overline{E1}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

3

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or G = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	—	15	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	- 12	- 15	- 20	- 25	- 35	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	150	140	130	120	110	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	45	40	35	30	30	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{W}$)	C_{in}	6	pF
Output Capacitance	C_{out}	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol		-12		-15		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	12	—	15	—	20	—	25	—	35	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	12	—	15	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	t_{AC}	—	12	—	15	—	20	—	25	—	35	ns	3
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	4	—	4	—	ns	4
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	4	—	4	—	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	6	0	8	0	9	0	10	0	15	ns	4,5,6
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	12	—	15	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. This parameter is sampled and not 100% tested.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
6. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min both for a given device and from device to device.
7. Device is continuously selected $\overline{E} \leq V_{IL}$.

AC TEST LOADS

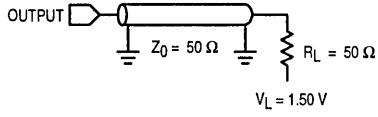


Figure 1A

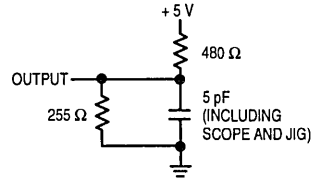
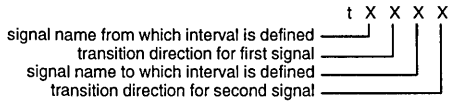


Figure 1B

TIMING PARAMETER ABBREVIATIONS

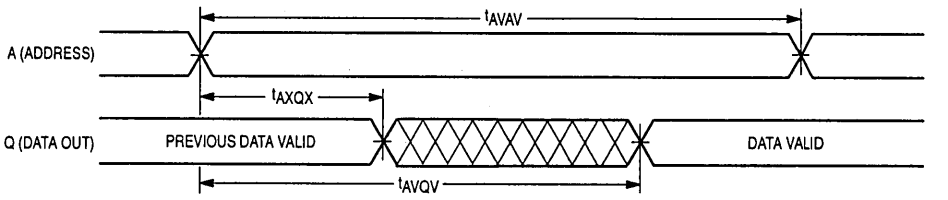


The transition definitions used in this data sheet are:
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

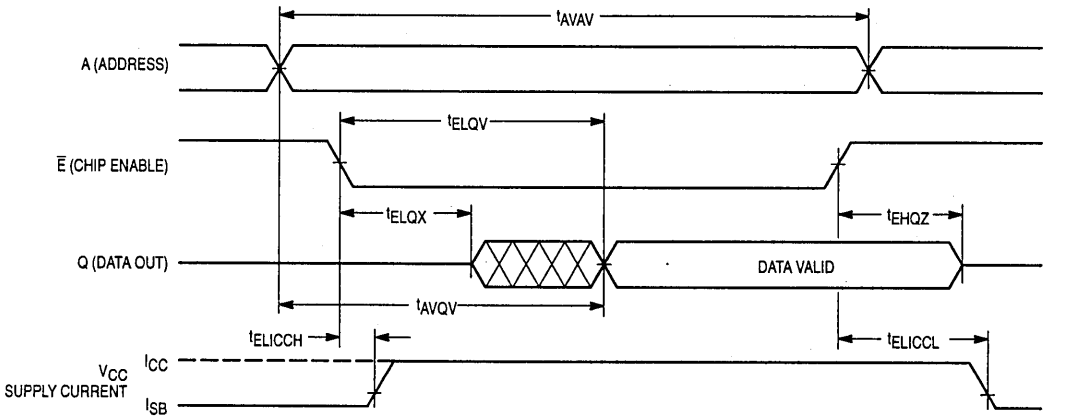
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Notes 2 and 6)

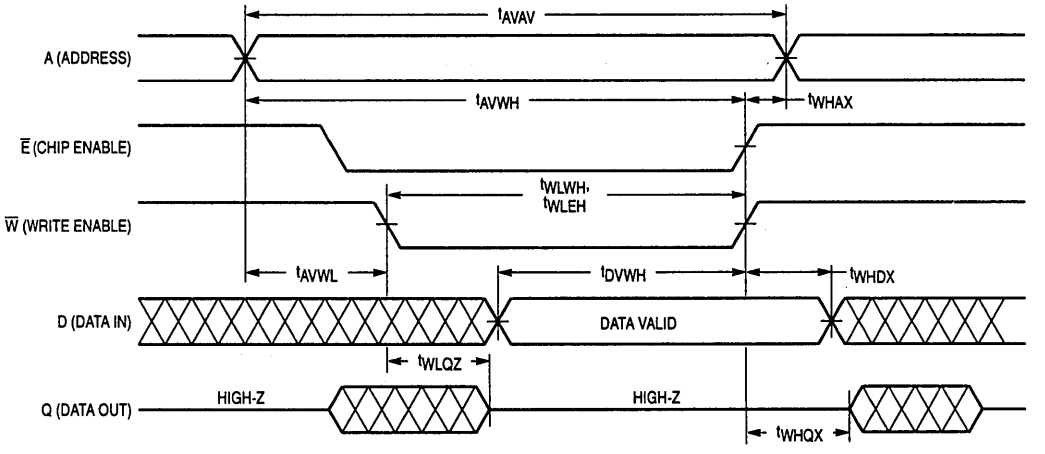


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		-12		-15		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	12	—	15	—	20	—	25	—	35	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	10	—	12	—	15	—	20	—	25	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	10	—	12	—	15	—	20	—	25	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	6	—	7	—	8	—	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	6	0	7	0	8	0	10	0	15	ns	3, 4, 5
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	4	—	4	—	ns	3, 4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	3, 4, 5

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All timings are referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min, both for a given device and from device to device.
4. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 (See Note 2)

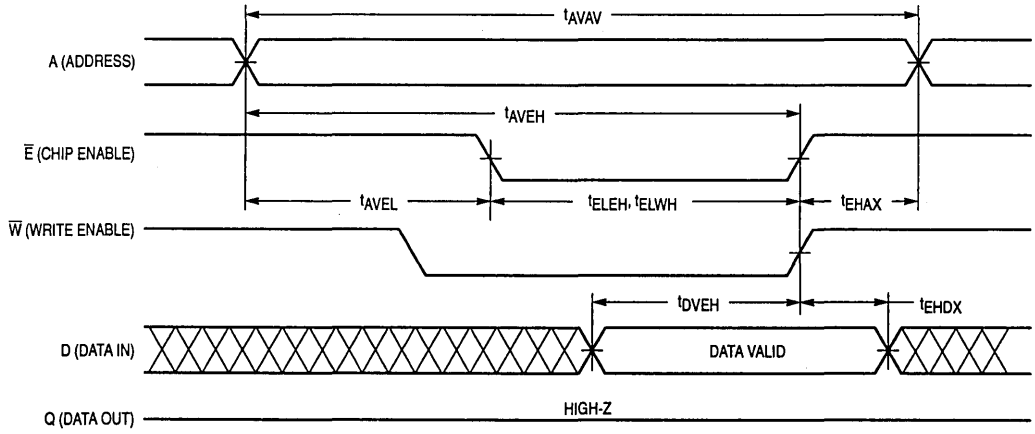


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

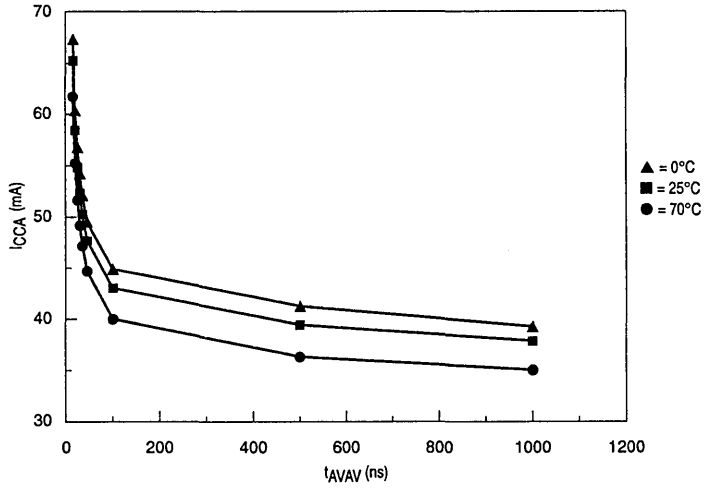
Parameter	Symbol		-12		-15		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	12	—	15	—	20	—	25	—	35	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	10	—	12	—	15	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	10	—	12	—	15	—	20	—	25	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	t_{DW}	6	—	7	—	8	—	10	—	15	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All timings are referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min, both for a given device and from device to device.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high-impedance state.

WRITE CYCLE 2 (See Note 2)



I_{CCA} vs CYCLE TIME



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6287B X XX XX

- Motorola Memory Prefix
- Part Number
- Shipping Method (R2 = Tape and Reel, Blank = Rails)
- Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- Package (P = 300 mil Plastic DIP, J = 300 mil SOJ)

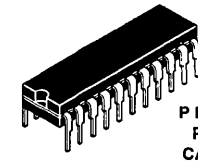
Full Part Numbers —			
	MCM6287BP12	MCM6287BJ12	MCM6287BJ12R2
	MCM6287BP15	MCM6287BJ15	MCM6287BJ15R2
	MCM6287BP20	MCM6287BJ20	MCM6287BJ20R2
	MCM6287BP25	MCM6287BJ25	MCM6287BJ25R2
	MCM6287BP35	MCM6287BJ35	MCM6287BJ35R2

MCM6288C

16K x 4 Bit Static RAM

The MCM6288C is a 65,536 bit static random access memory organized as 16,384 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

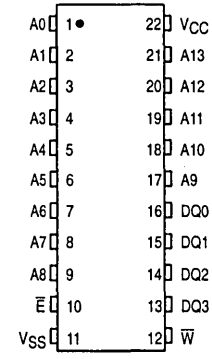
- Single 5 V ± 10% Power Supply
- Low Power Operation: 120 mA Maximum, Active AC
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Times: 12, 15, 20, 25, 35 ns
- Two Chip Controls:
  $\overline{E}$ for Automatic Power Down
  $\overline{G}$ for Fast Access to Data and Elimination of Bus Contention Problems
- Fully TTL-Compatible — Three-State Output



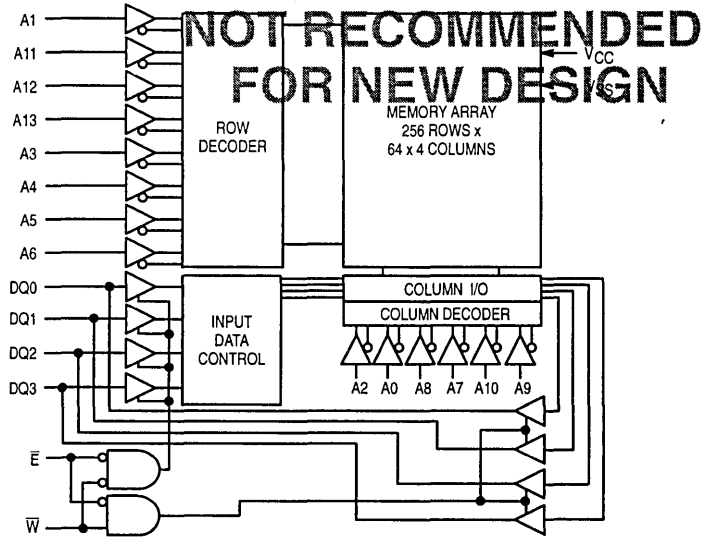
P PACKAGE
PLASTIC
CASE 736B

3

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A13	Address Input
DQ0 – DQ3	Data Input/Data Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
NC	No Connection
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z
L	H	Read	I_{CCA}	D_{out}
L	L	Write	I_{CCA}	High-Z

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V, V_{CC} = Max, f = 0 MHz)	I_{SB2}	—	10	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	-12	-15	-20	-25	-35	Unit
AC Active Supply Current (I_{out} = 0 mA)	I_{CCA}	120	120	110	110	110	mA
AC Standby Current (TTL Levels, V_{CC} = Max)	I_{SB1}	45	40	35	30	30	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address and Control Input Capacitance	C_{in}	6	pF
I/O Capacitance	$C_{I/O}$	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol		-12		-15		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	12	—	15	—	20	—	25	—	35	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	12	—	15	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	12	—	15	—	20	—	25	—	35	ns	4
Output Enable Access Time	t_{GLQX}	t_{OE}	—	6	—	8	—	10	—	12	—	15	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	4	—	4	—	ns	5, 6, 7
Enable Low to Output High-Z	t_{ELQX}	t_{CLZ}	4	—	4	—	4	—	4	—	4	—	ns	5, 6, 7
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	6	0	8	0	8	0	10	0	15	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	0	—	ns	5, 6, 7
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	6	0	7	0	8	0	10	0	15	ns	5, 6, 7
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	12	—	15	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

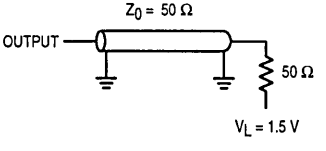


Figure 1A

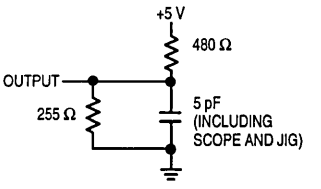


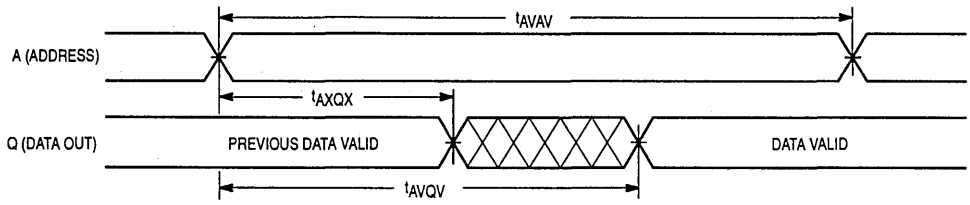
Figure 1B

TIMING LIMITS

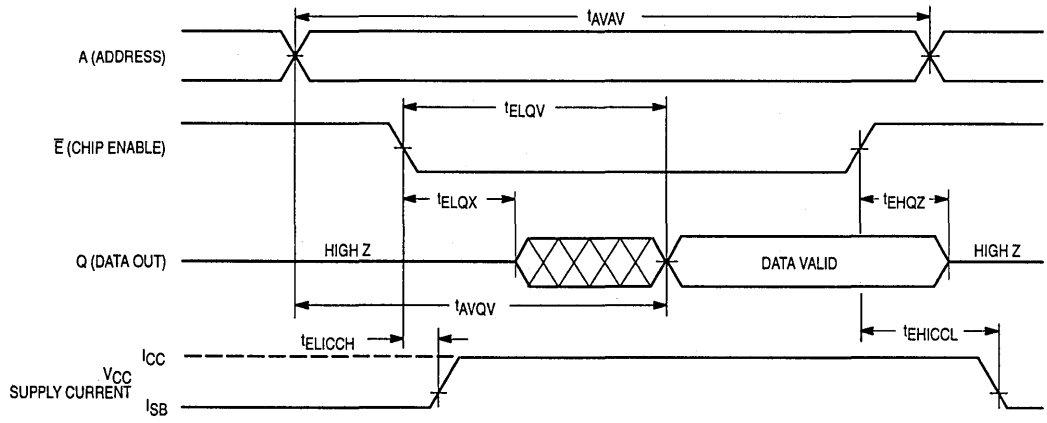
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Notes 2 and 4)

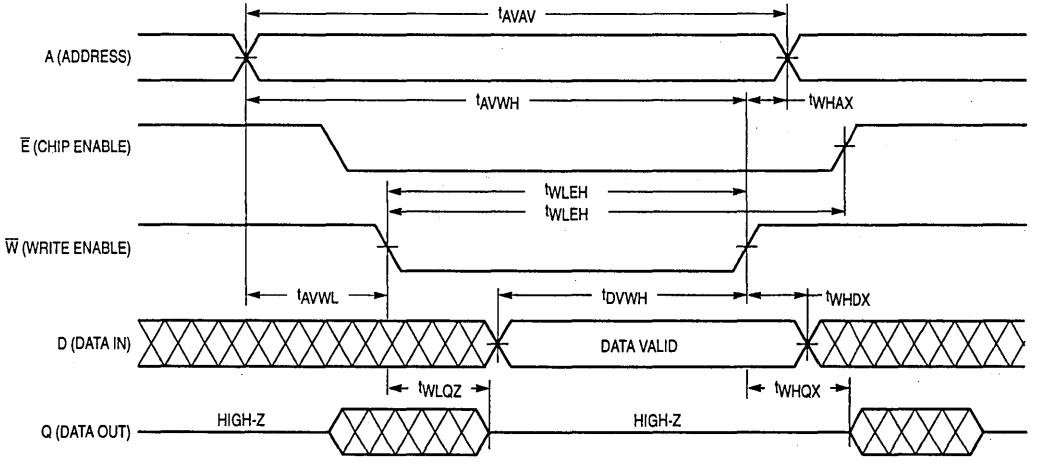


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		-12		-15		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	12	—	15	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	10	—	12	—	15	—	20	—	30	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	10	—	12	—	15	—	20	—	30	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH}, t_{WLEH}	t_{WP}	8	—	10	—	12	—	15	—	25	—	ns	5
Data Valid to End of Write	t_{DVWH}	t_{DW}	6	—	7	—	8	—	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	6	0	7	0	8	0	10	0	15	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	4	—	4	—	4	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. For Output Enable devices, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. For Output Enable devices, if $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min, both for a given device and from device to device.
7. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

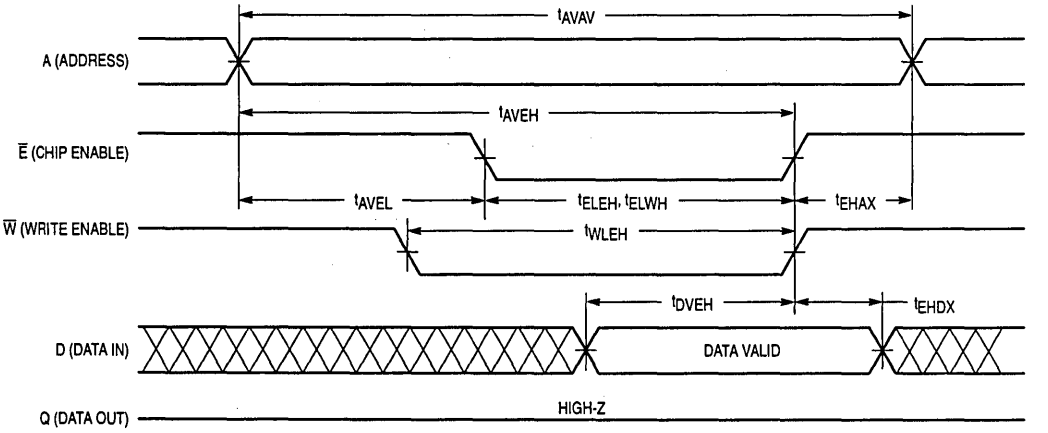


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		-12		-15		-20		-25		-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	12	—	15	—	20	—	25	—	35	—	ns	4
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	8	—	12	—	15	—	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	8	—	10	—	12	—	15	—	25	—	ns	5, 6
Data Valid to End of Write	t_{DVEH}	t_{DW}	6	—	7	—	8	—	10	—	15	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. For devices with multiple chip enables, $\overline{E1}$ and E2 are represented by $\overline{E}$ in this data sheet. E2 is of opposite polarity to $\overline{E}$.
3. For Output Enable devices, if $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6288C X XX XX

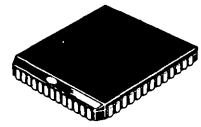
- MCM: Motorola Memory Prefix
- 6288C: Part Number
- X: Package (P = Plastic DIP, J = Plastic SOJ)
- XX: Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
- XX: Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers —

MCM6288CP12	MCM6288CP12R2
MCM6288CP15	MCM6288CP15R2
MCM6288CP20	MCM6288CP20R2
MCM6288CP25	MCM6288CP25R2
MCM6288CP35	MCM6288CP35R2

MCM62996

16K x 16 Bit Asynchronous Fast Static RAM



FN PACKAGE
52-LEAD PLCC
CASE 778

3

The MCM62996 is a 262,144 bit static random access memory organized as 16,384 words of 16 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 16K x 16 SRAM core with active high and active low chip enables, separate upper and lower byte write strobes, and a fast output enable. This device has increased output drive capability supported by multiple power pins. In addition, the output levels can be either 3.3 V or 5 V TTL compatible by choice of the appropriate output bus power supply.

Dual write strobes ($\overline{BWL}$ and $\overline{BWH}$) are provided to allow individually writeable bytes. $\overline{BWL}$ controls DQ0 – DQ7 (the lower bits), while $\overline{BWH}$ controls DQ8 – DQ15 (the upper bits).

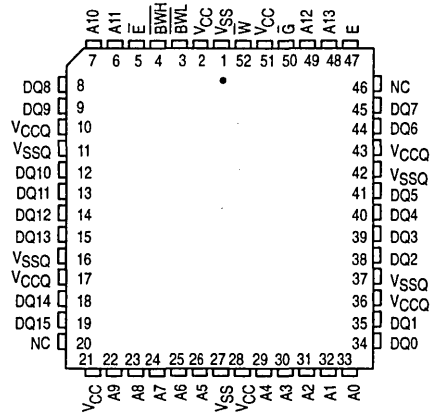
Additional power supply pins have been utilized and placed on the package for maximum performance. In addition, the output buffer power pins are electrically isolated from the other two and supply power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state thereby allowing simplified transmission line terminations.

The MCM62996 will be available in a 52-pin plastic leaded chip carrier PLCC.

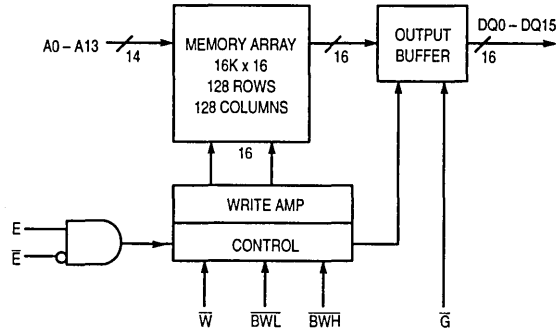
This device is ideally suited for systems that require wide data bus widths, cache memory, and tag RAMs.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Buffers
- Fast Access Times: 12/15/20/25 ns Max
- Byte Writeable via Dual Write Strobes with Abort Write Capability
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 52-Lead PLCC Package

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0 – A13	Address Inputs
$\overline{W}$	Write Enable
$\overline{BWL}$	Byte Write Strobe Low
$\overline{BWH}$	Byte Write Strobe High
E	Active High Chip Enable
$\overline{E}$	Active Low Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ15	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

TRUTH TABLE (See Notes)

$\overline{E}$	$\overline{W}$	$\overline{BWL}$	$\overline{BWH}$	$\overline{G}$	Mode	Supply Current	I/O Status
F	X	X	X	X	Deselected Cycle	I_{SB}	High-Z
T	H	X	X	H	Read Cycle	I_{CC}	High-Z
T	H	X	X	L	Read Cycle	I_{CC}	Data Out
T	L	L	L	X	Write Cycle All Bits	I_{CC}	High-Z
T	L	H	H	X	Aborted Write Cycle	I_{CC}	High-Z
T	L	L	H	X	Write Cycle Lower 8 Bits	I_{CC}	High-Z
T	L	H	L	X	Write Cycle Upper 8 Bits	I_{CC}	High-Z

NOTE: True (T) is E = 1 and $\overline{E}$ = 0. E, $\overline{E}$, and addresses satisfy the specified setup and hold times for the falling edge of LE. Data-in satisfies the specified setup and hold times for falling edge of DL.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = V_{CCQ} = 5.0$ V ± 10%, $T_A = 0$ to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}*	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	4.5 3.0	5.0 3.3	5.5 3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL}(min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0$ to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current ($\overline{G} = V_{IH}$)	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current ($I_{out} = 0$ mA, All Inputs = V_{IL} or V_{IH}, $V_{IL} = 0.0$ V and $V_{IH} \geq 3.0$ V, Cycle Time ≥ t_{AVAV} min)	I_{CCA12} I_{CCA15} I_{CCA20} I_{CCA25}	— — — —	295 275 265 255	350 330 320 310	mA
Standby Current (E = V_{IL}, $\overline{E}$ = V_{IH}, $I_{out} = 0$ mA, All Inputs = V_{IL} and V_{IH}, $V_{IL} = 0$ V and $V_{IH} \geq 3.0$ V, Cycle Time ≥ t_{AVAV} min)	I_{SB}	—	40	50	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C. Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ15)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0 – DQ15)	C_{out}	8	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 3.3 V or 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

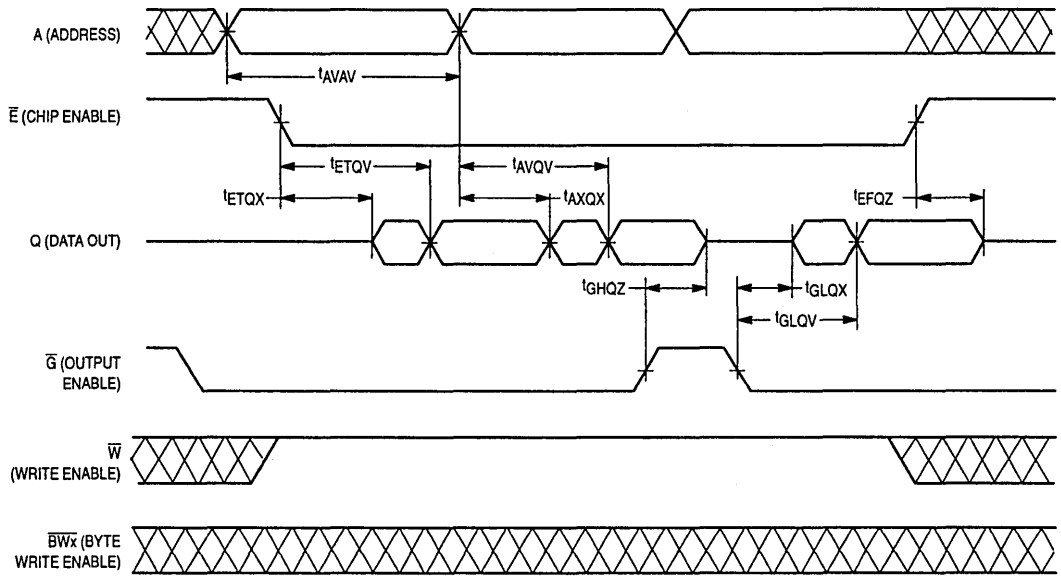
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM62996-12		MCM62996-15		MCM62996-20		MCM62996-25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	15	—	15	—	20	—	25	—	ns	4
Access Times:										ns	5
Address Valid to Output Valid	t_{AVQV}	—	12	—	15	—	20	—	25		
E, $\overline{E}$ "True" to Output Valid	t_{ETQV}	—	12	—	15	—	20	—	25		
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	8	—	10		
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	4	—	ns	
Output Buffer Control:										ns	6
E, $\overline{E}$ "True" to Output Active	t_{ETQX}	2	—	2	—	2	—	2	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	2	—	2	—	0	—	2	—		
E, $\overline{E}$ "False" to Output High-Z	t_{EFQZ}	2	9	2	9	0	9	2	10		
$\overline{G}$ High to Output High-Z	t_{GHQZ}	2	5	2	6	0	8	2	10		
Power Up Time	t_{ETICCH}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. Write Enable is equal to V_{IH} for all read cycles.
2. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
3. EF is defined by $\overline{E}$ going high or E going low.
4. All read cycle timing is referenced from the last valid address to the first transitioning address.
5. Addresses valid prior to or coincident with $\overline{E}$ going low or E going high.
6. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EFQZ} is less than t_{ETQX} and t_{GHQZ} is less than t_{GLQZ} for a given device.

READ CYCLE



WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM62996-12		MCM62996-15		MCM62996-20		MCM62996-25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Times	t_{AVAV}	15	—	15	—	20	—	25	—	ns	5
Setup Times:										ns	
Address Valid to End of Write	t_{AVWH}	10		13		15		20			
Address Valid to End of Write	t_{AVEF}	10	—	13	—	15	—	20	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—	0	—		
Address Valid to E, $\overline{E}$ "True"	t_{AVET}	0	—	0	—	0	—	0	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	8	—	10	—		
Data Valid to E or $\overline{E}$ "False"	t_{DVEF}	6	—	6	—	8	—	10	—		
Byte Write Low to $\overline{W}$ High	t_{BWxLWH}	6	—	6	—	8	—	10	—		
Byte Write High to $\overline{W}$ Low (Abort)	t_{BWxHWL}	0	—	0	—	0	—	0	—		
Byte Write Low to E, $\overline{E}$ "False"	t_{BWxLEF}	6	—	6	—	8	—	10	—		
Hold Times:										ns	
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Address Invalid	t_{EFAX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Data Invalid	t_{EFDX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Byte Write Invalid	t_{WHBWxX}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "False" to Byte Write Invalid	t_{EFBWxX}	2	—	2	—	2	—	2	—		
Write Pulse Width:										ns	
Write Pulse Width	t_{WLWH}	12	—	13	—	15	—	20	—		
Write Pulse Width	t_{WLEF}	12	—	13	—	15	—	20	—		6
Enable to End of Write	t_{ETWH}	12	—	13	—	15	—	20	—		7
Enable to End of Write	t_{ETEF}	12	—	13	—	15	—	20	—		6, 7
Output Buffer Control:										ns	
$\overline{W}$ High to Output Valid	t_{WHQV}	12	—	13	—	20	—	25	—		
$\overline{W}$ High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—		8
$\overline{W}$ Low to Output High-Z	t_{WLQZ}	0	9	0	9	0	9	0	10		8, 9

NOTES:
1. A write occurs during the overlap of ET, $\overline{W}$ low and $\overline{BWx}$ low. An aborted write occurs when $\overline{BWx}$ remains at V_{IH} while $\overline{W}$ is low.
2. Write must be equal to V_{IH} for all address transitions.
3. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
4. EF is defined by $\overline{E}$ going high or E going low.
5. All write cycle timing is referenced from the last valid address to the first transitioning address.
6. If E or $\overline{E}$ goes false coincident with or before $\overline{W}$ goes high the output will remain in a high-impedance state.
7. If E and $\overline{E}$ go true coincident with or after $\overline{W}$ goes low the output will remain in a high-impedance state.
8. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
9. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance state.

AC TEST LOADS

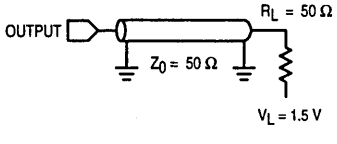


Figure 1A

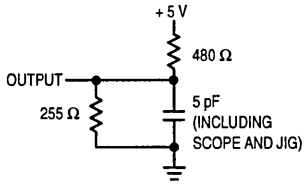
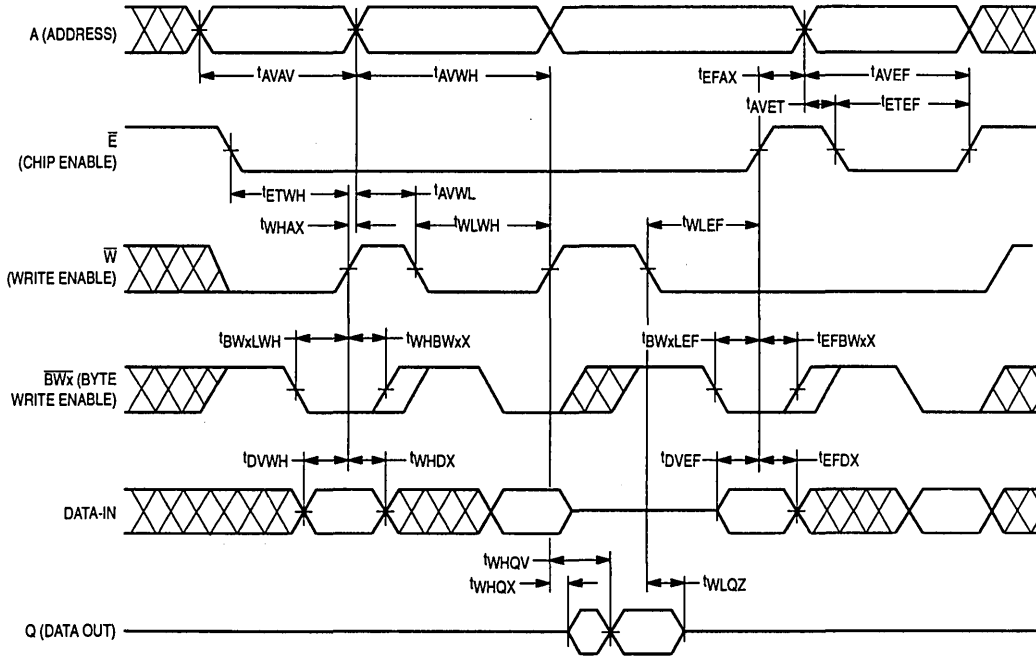


Figure 1B

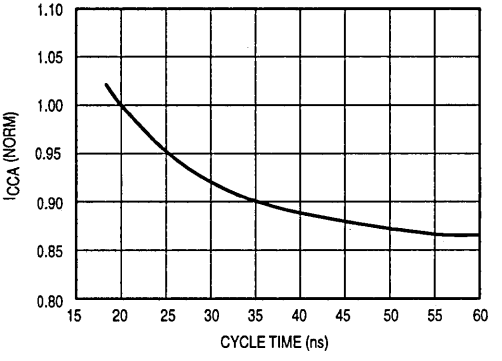
NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

WRITE CYCLE

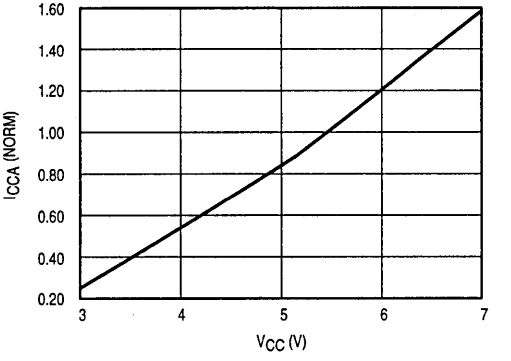

A (ADDRESS)
tAVAV
tAVWH
tEFAX
tAVEF
tAVET
tETEF
E
(CHIP ENABLE)
tETWH
tAVWL
tWHAX
tWLWH
tWLEF
W
(WRITE ENABLE)
tBWxLWH
tWHBWxX
tBWxLEF
tEFBWxX
BWx (BYTE
WRITE ENABLE)
tDVWH
tWHDX
tDVEF
tEFDX
DATA-IN
tWHQV
tWHQX
tWLQZ
Q (DATA OUT)

DERATING CURVES

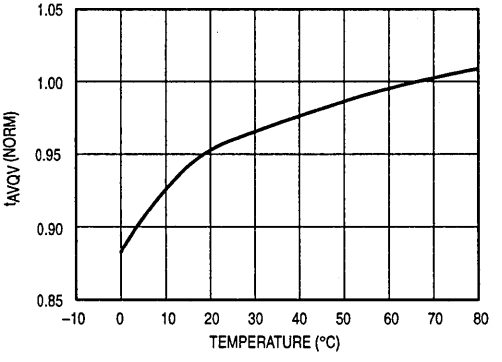
(Derating Curves Are Based On Component Typical Values)



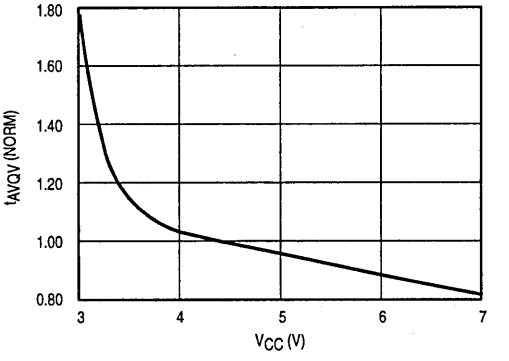
I_{CCA} vs Cycle Time



I_{CCA} vs V_{CC}



AVQV vs Temperature



AVQV vs V_{CC}

ORDERING INFORMATION

(Order by Full Part Number)

MCM	62996	FN	XX
Motorola Memory Prefix	Part Number	Package (FN = PLCC)	Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns, 25 = 25 ns)

Full Part Numbers — MCM62996FN12 MCM62996FN15 MCM62996FN20 MCM62996FN25

Application Specific Fast Static RAMs

4

Processor Specific

Latched Address

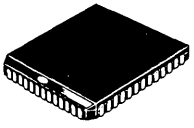
Line Buffers

Synchronous

4

MCM56824A

DSPRAM™
8K x 24 Bit Fast Static RAM



FN PACKAGE
52-LEAD PLCC
CASE 778

The MCM56824A is a 196,608 bit static random access memory organized as 8,192 words of 24 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates an 8K x 24 SRAM core with multiple chip enable inputs, output enable, and an externally controlled single address pin multiplexer. These functions allow for direct connection to the Motorola DSP56001 Digital Signal Processor and provide a very efficient means for implementation of a reduced parts count system requiring no additional interface logic.

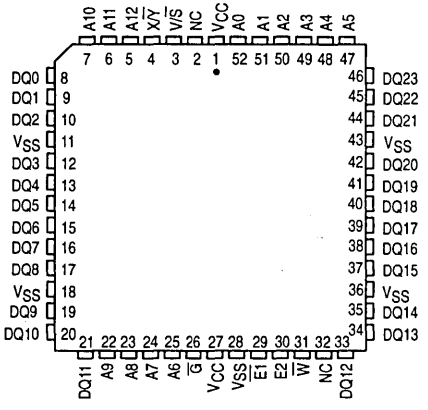
The availability of multiple chip enable ($\overline{E1}$ and E2) and output enable ($\overline{G}$) inputs provides for greater system flexibility when multiple devices are used. With either chip enable input unasserted, the device will enter standby mode, useful in low-power applications. A single on-chip multiplexer selects A12 or X/$\overline{Y}$ as the highest order address input depending upon the state of the V/$\overline{S}$ control input. This feature allows one physical static RAM component to efficiently store program and vector or scalar operands by dynamically repartitioning the RAM array. Typical applications will logically map vector operands into upper memory with scalar operands being stored in lower memory. By connecting DSP56001 address A15 to the VECTOR/SCALAR (V/$\overline{S}$) MUX control pin, such partitioning can occur with no additional components. This allows efficient utilization of the RAM resource irrespective of operand type. See application diagrams at the end of this document for additional information.

Multiple power and ground pins have been utilized to minimize effects induced by output noise.

The MCM56824A is available in a 52 pin plastic leaded chip-carrier (PLCC).

- Single 5 V ± 10% Power Supply
- Fast Access and Cycle Times: 20/25/35 ns Max
- Fully Static Read and Write Operations
- Equal Address and Chip Enable Access Times
- Single Bit On-Chip Address Multiplexer
- Active High and Active Low Chip Enable Inputs
- Output Enable Controlled Three State Outputs
- High Board Density PLCC Package
- Low Power Standby Mode
- Fully TTL Compatible

PIN ASSIGNMENT

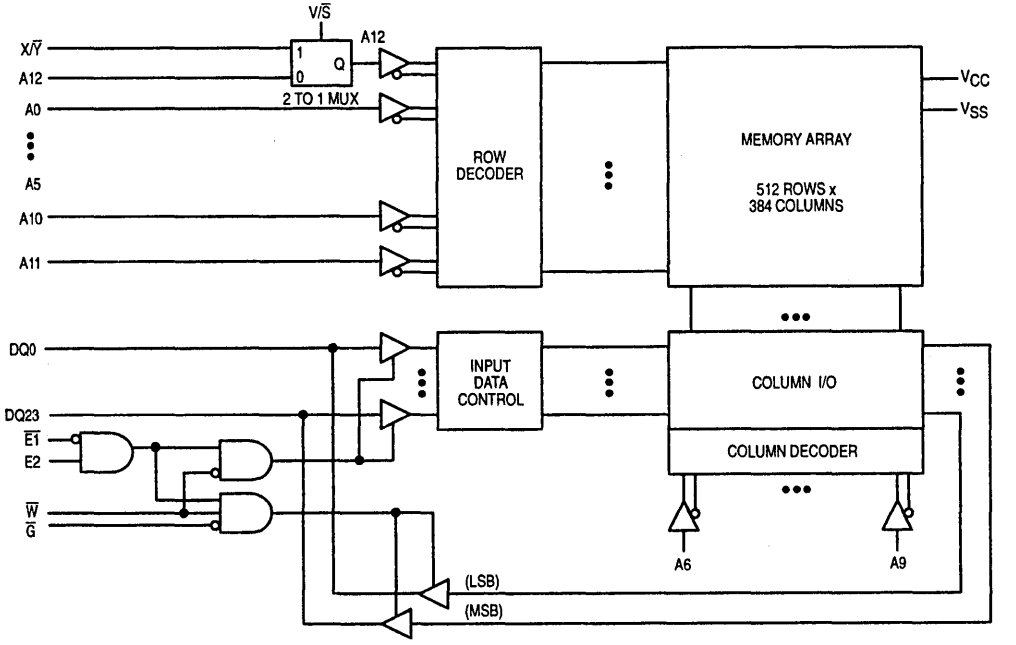


PIN NAMES	
A0 – A11	Address Inputs
A12, X/$\overline{Y}$	Multiplexed Address
V/$\overline{S}$	Address Multiplexer Control
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ23	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

For proper operation of the device, all V_{SS} pins must be connected to ground.

DSPRAM is a trademark of Motorola, Inc.

BLOCK DIAGRAM



4

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	V/$\overline{S}$	Mode	Supply Current	I/O Status
H	X	X	X	X	Not Selected	I_{SB}	High-Z
X	L	X	X	X	Not Selected	I_{SB}	High-Z
L	H	H	H	X	Output Disable	I_{CC}	High-Z
L	H	L	H	H	Read Using X/$\overline{Y}$	I_{CC}	Data Out
L	H	L	H	L	Read Using A12	I_{CC}	Data Out
L	H	X	L	H	Write Using X/$\overline{Y}$	I_{CC}	Data In
L	H	X	L	L	Write Using A12	I_{CC}	Data In

NOTE: X=don't care.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.75	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is assumed to be in a test socket or mounted on a printed circuit board with at least 300 LFPM of transverse air flow being maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(i)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH}, $\overline{E1}$ = V_{IH}, E2 = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E1}$ = V_{IL}, E2 = V_{IH}, I_{out} = 0 mA, All Other Inputs ≥ V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V) MCM56824A-20 Cycle Time: ≥ 20 ns MCM56824A-25 Cycle Time: ≥ 25 ns MCM56824A-35 Cycle Time: ≥ 35 ns	I_{CCA}	— — —	260 220 180	mA
Standby Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, All Inputs = V_{IL} or V_{IH})	I_{SB1}	—	15	mA
CMOS Standby Current ($\overline{E1}$ ≥ V_{CC} – 0.2 V, E2 ≤ 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)	I_{SB2}	—	10	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	All Pins Except DQ0 – DQ23	C_{in}	4	6	pF
Input/Output Capacitance	DQ0 – DQ23	C_{out}	6	8	pF

AC TEST LOADS

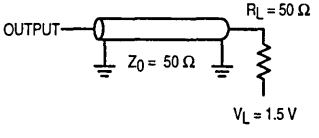


Figure 1A

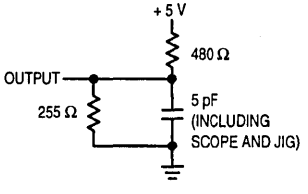


Figure 1B

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

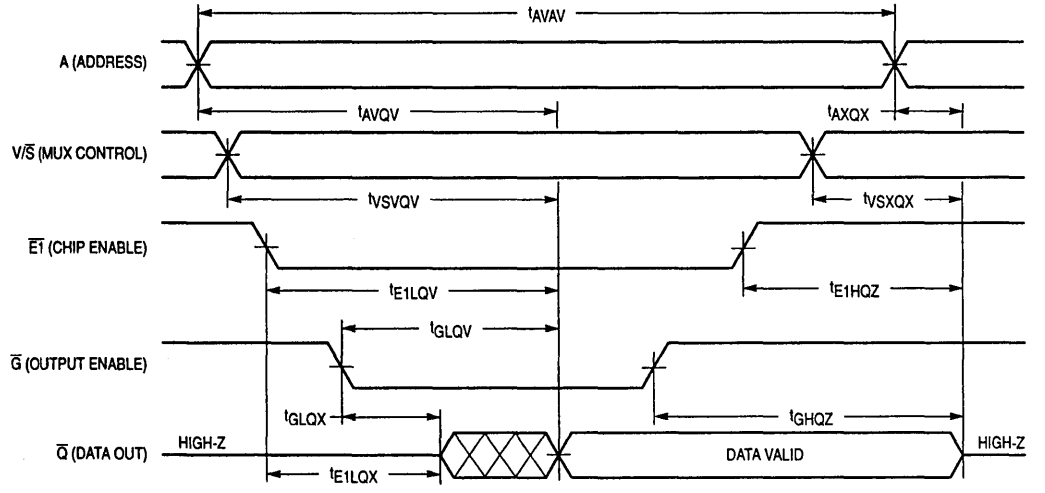
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol		MCM56824A-20		MCM56824A-25		MCM56824A-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	—	25	—	35	—	ns	
Address Access Time	t_{AVQV}	t_{AA}	—	20	—	25	—	35	ns	
MUX Control Valid to Output Valid	t_{VSVQV}	t_{AA}	—	20	—	25	—	35	ns	
Chip Enable to Output Valid	t_{E1LQV} t_{E2HQV}	t_{AC1} t_{AC2}	—	20	—	25	—	35	ns	4
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	8	—	10	—	15	ns	
Output Active from Chip Enable	t_{E1LQX} t_{E2HQX}	t_{CLZ}	2	—	2	—	0	—	ns	4, 5
Output Active from Output Enable	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns	5
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	5	—	5	—	ns	
Output Hold from MUX Control Change	t_{VSXQX}	t_{VSOH}	4	—	5	—	5	—	ns	
Chip Enable to Output High Z	t_{E1HQZ} t_{E2LQZ}	t_{CHZ}	0	10	0	15	0	15	ns	4, 5
Output Enable High to Output High Z	t_{GHQZ}	t_{OHZ}	0	8	0	15	0	15	ns	5

NOTES:
1. A read cycle is defined by $\overline{W}$ high.
2. All read cycle timings are referenced from the last valid address or vector/scalar transition to the first address or vector/scalar transition.
3. Addresses valid prior to or coincident with $\overline{E1}$ going low or E2 going high.
4. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{E1HQZ} max is less than t_{E1LQX} min, t_{E2LQZ} max is less than t_{E2HQX} min, and t_{GHQZ} max is less than t_{GLQX} min for a given device and from device to device.

READ CYCLE

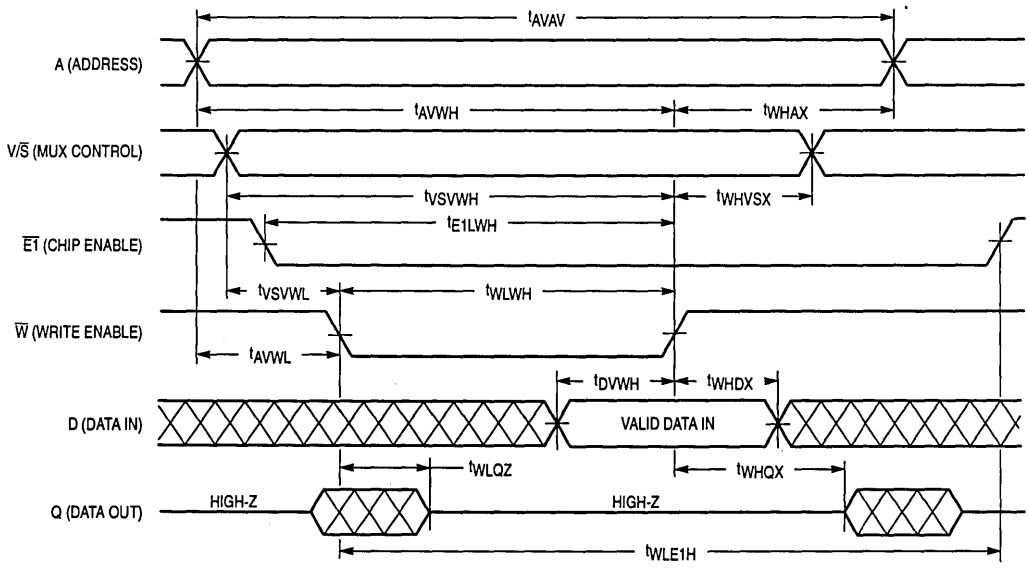


WRITE CYCLE TIMING (Write Enable Initiated, See Note 1)

Parameter	Symbol		MCM56824A-20		MCM56824A-25		MCM56824A-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	ns	
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	2
MUX Control Setup Time	t_{VSVWL}	t_{VSS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	—	20	—	30	—	ns	
MUX Control Valid to End of Write	t_{VSVWH}	t_{VSW}	15	—	20	—	30	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	20	—	ns	3
Write Enable to Chip Enable Disable	t_{WLE1H} t_{WLE2L}	t_{CW}	15	—	15	—	20	—	ns	3, 4
Chip Enable to End of Write	t_{E1LWH} t_{E2HWH}	t_{CW}	15	—	15	—	20	—	ns	3, 4
Data Valid to End of Write	t_{DVWH}	t_{DW}	8	—	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	2
MUX Control Recovery Time	t_{WHVSX}	t_{VSR}	0	—	0	—	0	—	ns	
Write High to Output Low Z	t_{WHQX}	t_{WLZ}	4	—	5	—	5	—	ns	6
Write Low to Output High Z	t_{WLQZ}	t_{WHZ}	0	15	0	15	0	15	ns	6

NOTES:
1. A write cycle starts at the latest transition of $\overline{E1}$ low, $\overline{W}$ low, or E2 high. A write cycle ends at the earliest transition of $\overline{E1}$ high, $\overline{W}$ high, or E2 low.
2. Write must be high for all address transitions.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high the outputs will remain in a high-impedance state.
4. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
5. During this time the output pins may be in the output state. Signals of opposite phase must not be applied to the outputs at this time.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{E1HQZ} max is less than t_{E1LQX} min, t_{E2LQZ} max is less than t_{E2HQX} min, and t_{GHQZ} max is less than t_{GLQX} min for a given device and from device to device.

$\overline{WE}$ INITATED WRITE CYCLE

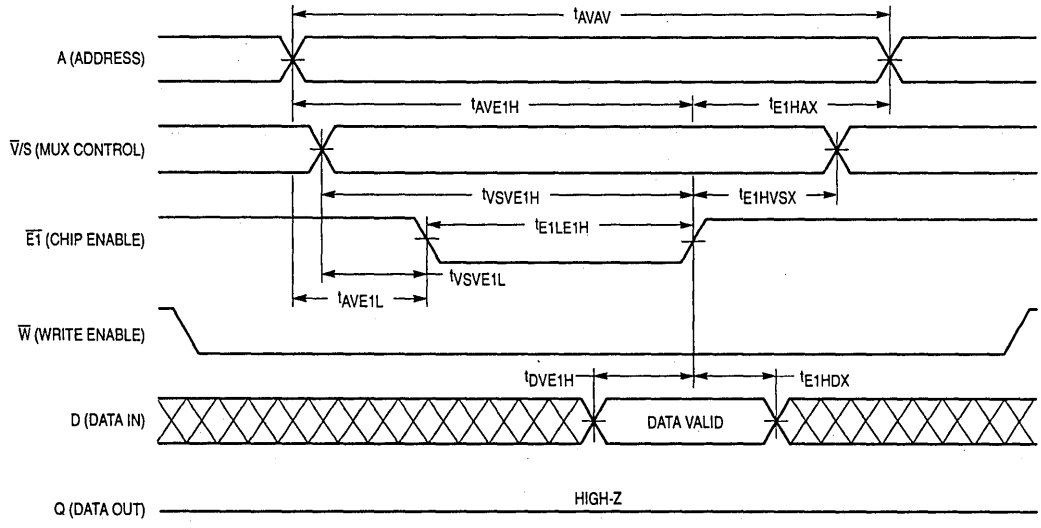


WRITE CYCLE TIMING (Chip Enable Initiated, See Note 1)

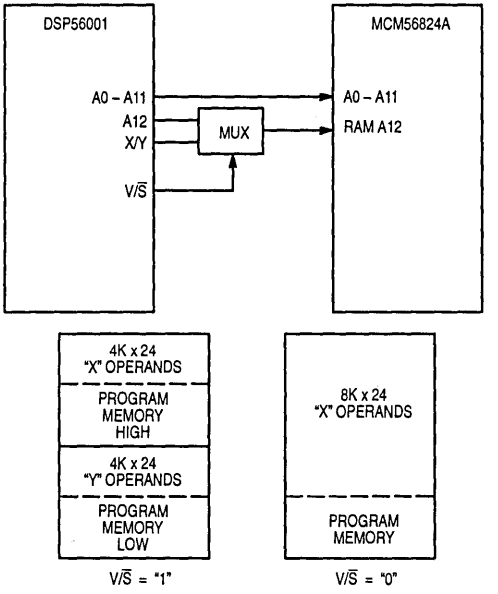
Parameter	Symbol		MCM56824A-20		MCM56824A-25		MCM56824A-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	ns	
Address Setup Time	t_{AVE1L} t_{AVE2H}	t_{AS}	0	—	0	—	0	—	ns	2
MUX Control Setup Time	t_{VSVE1L} t_{VSVE2H}	t_{VSS}	0	—	0	—	0	—	ns	2
Address Valid to End of Write	t_{AVE1H} t_{AVE2L}	t_{SW}	15	—	20	—	30	—	ns	2
MUX Control Valid to End of Write	t_{VSVE1H} t_{VSVE2L}	t_{VSW}	15	—	20	—	30	—	ns	2
Chip Enable to End of Write	t_{E1LE1H} t_{E2HE2L}	t_{CW}	12	—	15	—	20	—	ns	2, 3
Data Valid to End of Write	t_{DVE1H} t_{DVE2L}	t_{DW}	8	—	10	—	15	—	ns	2
Data Hold Time	t_{E1HDX} t_{E2LDX}	t_{DH}	0	—	0	—	0	—	ns	2, 4
Write Recovery Time	t_{E1HAX} t_{E2LAX}	t_{WR}	0	—	0	—	0	—	ns	2
MUX Control Recovery Time	t_{E1HVSX} t_{E2LVSX}	t_{VSR}	0	—	0	—	0	—	ns	2

NOTES:
1. A write cycle starts at the latest transition of $\overline{E1}$ low, $\overline{W}$ low, or E2 high. A write cycle ends at the earliest transition of $\overline{E1}$ high, $\overline{W}$ high, or E2 low.
2. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high the outputs will remain in a high-impedance state.
4. During this time the output pins may be in the output state. Signals of opposite phase must not be applied to the outputs at this time.

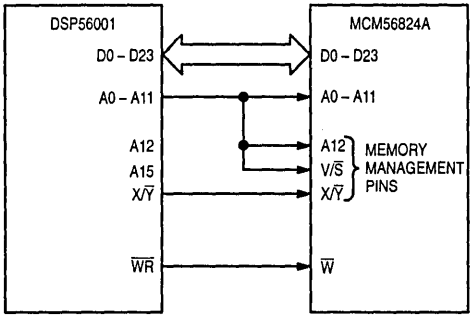
$\overline{E1}$ OR E2 INITIATED WRITE CYCLE



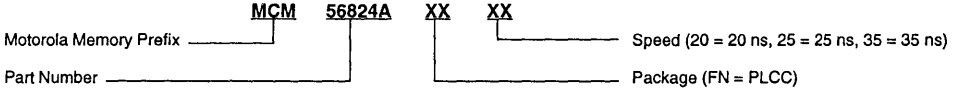
DSPRAM Multiplexed Vector/Scalar Address Maps



8K x 24 DSPRAM Used in Typical Application



ORDERING INFORMATION
(Order by Full Part Number)



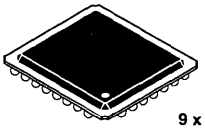
Full Part Numbers — MCM56824AFN20 MCM56824AFN25 MCM56824AFN35

MCM56824AZP

Product Preview

DSPRAM™

8K x 24 Bit Fast Static RAM



9 x 10 GRID
86 BUMP OMPAC
CASE 896A-01

The MCM56824AZP is a 196,608 bit static random access memory organized as 8,192 words of 24 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates an 8K x 24 SRAM core with multiple chip enable inputs, output enable, and an externally controlled single address pin multiplexer. These functions allow for direct connection to the Motorola DSP56001 Digital Signal Processor and provide a very efficient means for implementation of a reduced parts count system requiring no additional interface logic.

The availability of multiple chip enable ($\overline{E1}$ and E2) and output enable ($\overline{G}$) inputs provides for greater system flexibility when multiple devices are used. With either chip enable input unasserted, the device will enter standby mode, useful in low-power applications. A single on-chip multiplexer selects A12 or X/$\overline{Y}$ as the highest order address input depending upon the state of the V/$\overline{S}$ control input. This feature allows one physical static RAM component to efficiently store program and vector or scalar operands by dynamically re-partitioning the RAM array. Typical applications will logically map vector operands into upper memory with scalar operands being stored in lower memory. By connecting DSP56001 address A15 to the VECTOR/SCALAR (V/$\overline{S}$) MUX control pin, such partitioning can occur with no additional components. This allows efficient utilization of the RAM resource irrespective of operand type. See application diagrams at the end of this document for additional information.

Multiple power and ground pins have been utilized to minimize effects induced by output noise.

The MCM56824AZP is available in a 9 x 10 grid, 86 bump surface mount OMPAC.

- Single 5 V ± 10% Power Supply
- Fast Access and Cycle Times: 20/25/35 ns Max
- Fully Static Read and Write Operations
- Equal Address and Chip Enable Access Times
- Single Bit On-Chip Address Multiplexer
- Active High and Active Low Chip Enable Inputs
- Output Enable Controlled Three State Outputs
- High Board Density PLCC Package
- Low Power Standby Mode
- Fully TTL Compatible

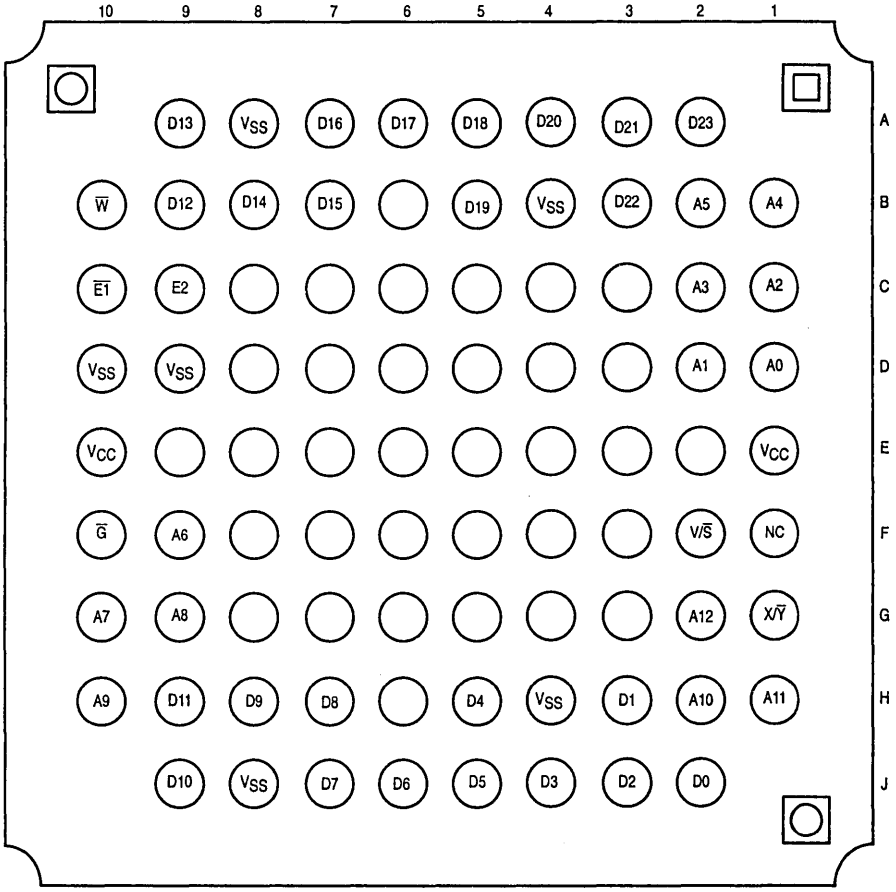
PIN NAMES	
A0 – A11	Address Inputs
A12, X/$\overline{Y}$	Multiplexed Address
V/$\overline{S}$	Address Multiplexer Control
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ23	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

For proper operation of the device, all V_{SS} pins must be connected to ground.

DSPRAM is a trademark of Motorola, Inc.

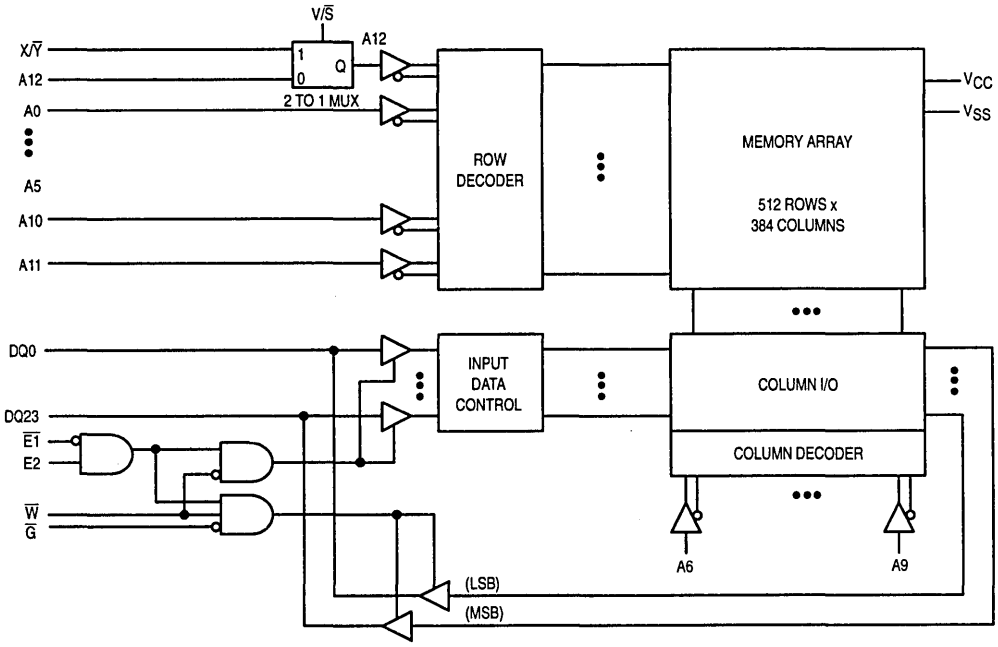
This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

VIEW OF PACKAGE BOTTOM



4

BLOCK DIAGRAM



4

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	V/$\overline{S}$	Mode	Supply Current	I/O Status
H	X	X	X	X	Not Selected	I_{SB}	High-Z
X	L	X	X	X	Not Selected	I_{SB}	High-Z
L	H	H	H	X	Output Disable	I_{CC}	High-Z
L	H	L	H	H	Read Using X/$\overline{Y}$	I_{CC}	Data Out
L	H	L	H	L	Read Using A12	I_{CC}	Data Out
L	H	X	L	H	Write Using X/$\overline{Y}$	I_{CC}	Data In
L	H	X	L	L	Write Using A12	I_{CC}	Data In

NOTE: X = don't care.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation)	P_D	1.75	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is assumed to be in a test socket or mounted on a printed circuit board with at least 300 LFPM of transverse air flow being maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(i)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH}, $\overline{E1}$ = V_{IH}, E2 = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E1}$ = V_{IL}, E2 = V_{IH}, I_{out} = 0 mA, All Other Inputs ≥ V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V) MCM56824A-20 Cycle Time: ≥ 20 ns MCM56824A-25 Cycle Time: ≥ 25 ns MCM56824A-35 Cycle Time: ≥ 35 ns	I_{CCA}	— — —	260 220 180	mA
Standby Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, All Inputs = V_{IL} or V_{IH})	I_{SB1}	—	15	mA
CMOS Standby Current ($\overline{E1}$ ≥ V_{CC} – 0.2 V, E2 ≤ 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)	I_{SB2}	—	10	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	All Pins Except DQ0 – DQ23	C_{in}	4	6	pF
Input/Output Capacitance	DQ0 – DQ23	C_{out}	6	8	pF

AC TEST LOADS

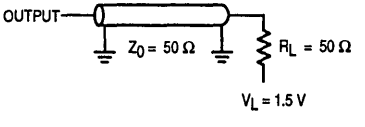


Figure 1A

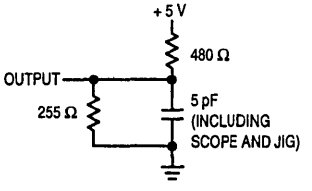


Figure 1B

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

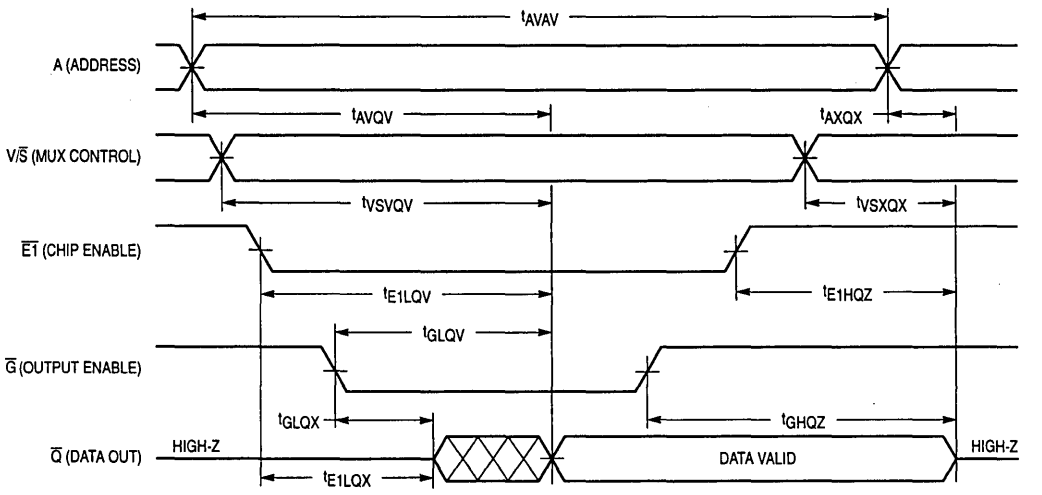
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol		MCM56824AZP-20		MCM56824AZP-25		MCM56824AZP-35		Unit	Notes
	Stndard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	—	25	—	35	—	ns	
Address Access Time	t_{AVQV}	t_{AA}	—	20	—	25	—	35	ns	
MUX Control Valid to Output Valid	t_{VSVQV}	t_{AA}	—	20	—	25	—	35	ns	
Chip Enable to Output Valid	t_{E1LQV} t_{E2HQV}	t_{AC1} t_{AC2}	—	20	—	25	—	35	ns	4
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	8	—	10	—	15	ns	
Output Active from Chip Enable	t_{E1LQX} t_{E2HQX}	t_{CLZ}	2	—	2	—	0	—	ns	4, 5
Output Active from Output Enable	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns	5
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	5	—	5	—	ns	
Output Hold from MUX Control Change	t_{VSXQX}	t_{VSOH}	4	—	5	—	5	—	ns	
Chip Enable to Output High Z	t_{E1HQZ} t_{E2LQZ}	t_{CHZ}	0	10	0	15	0	15	ns	4, 5
Output Enable High to Output High Z	t_{GHQZ}	t_{OHZ}	0	8	0	15	0	15	ns	5

NOTES:
1. A read cycle is defined by $\overline{W}$ high.
2. All read cycle timings are referenced from the last valid address or vector/scalar transition to the first address or vector/scalar transition.
3. Addresses valid prior to or coincident with $\overline{E1}$ going low or E2 going high.
4. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{E1HQZ} max is less than t_{E1LQX} min, t_{E2LQZ} max is less than t_{E2HQX} min, and t_{GHQZ} max is less than t_{GLQX} min for a given device and from device to device.

READ CYCLE

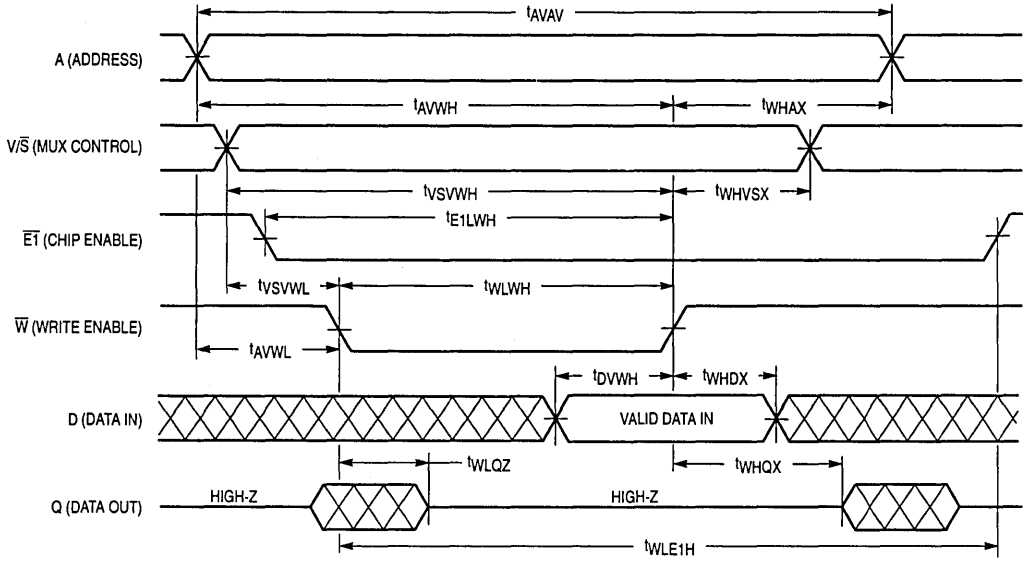


WRITE CYCLE TIMING (Write Enable Initiated, See Note 1)

Parameter	Symbol		MCM56824AZP-20		MCM56824AZP-25		MCM56824AZP-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	ns	
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	2
MUX Control Setup Time	t_{VSVWL}	t_{VSS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	—	20	—	30	—	ns	
MUX Control Valid to End of Write	t_{VSVWH}	t_{VSW}	15	—	20	—	30	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	20	—	ns	3
Write Enable to Chip Enable Disable	t_{WLE1H} t_{WLE2L}	t_{CW}	15	—	15	—	20	—	ns	3, 4
Chip Enable to End of Write	t_{E1LWH} t_{E2HWH}	t_{CW}	15	—	15	—	20	—	ns	3, 4
Data Valid to End of Write	t_{DVWH}	t_{DW}	8	—	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	2
MUX Control Recovery Time	t_{WHVSX}	t_{VSR}	0	—	0	—	0	—	ns	
Write High to Output Low Z	t_{WHQX}	t_{WLZ}	4	—	5	—	5	—	ns	6
Write Low to Output High Z	t_{WLQZ}	t_{WHZ}	0	15	0	15	0	15	ns	6

NOTES:
1. A write cycle starts at the latest transition of $\overline{E1}$ low, $\overline{W}$ low, or E2 high. A write cycle ends at the earliest transition of $\overline{E1}$ high, $\overline{W}$ high, or E2 low.
2. Write must be high for all address transitions.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high the outputs will remain in a high-impedance state.
4. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
5. During this time the output pins may be in the output state. Signals of opposite phase must not be applied to the outputs at this time.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{E1HQZ} max is less than t_{E1LQX} min, t_{E2LQZ} max is less than t_{E2HQX} min, and t_{GHQZ} max is less than t_{GLQX} min for a given device and from device to device.

$\overline{WE}$ INITATED WRITE CYCLE



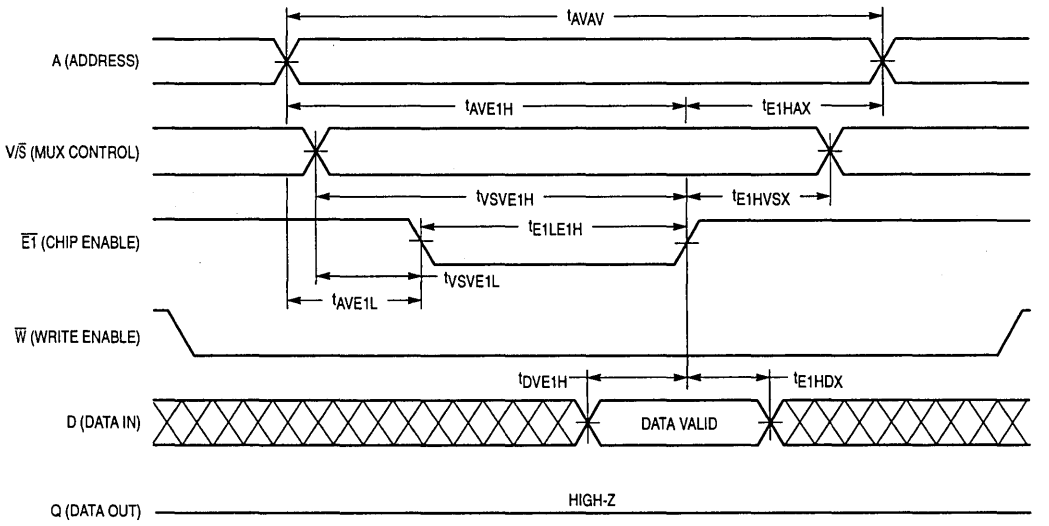
4

WRITE CYCLE TIMING (Chip Enable Initiated, See Note 1)

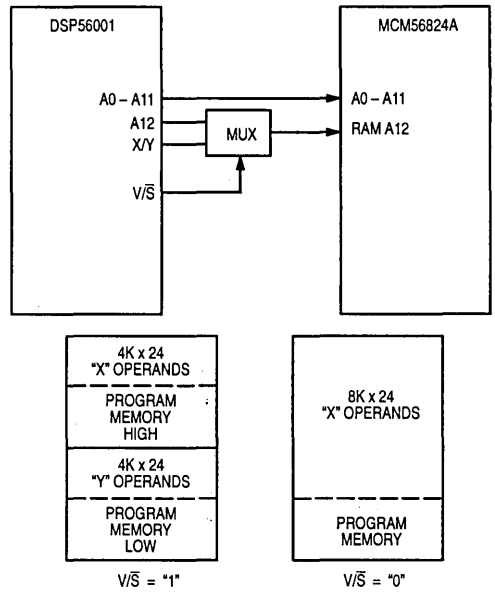
Parameter	Symbol		MCM56824AZP-20		MCM56824AZP-25		MCM56824AZP-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	ns	
Address Setup Time	t_{AVE1L} t_{AVE2H}	t_{AS}	0	—	0	—	0	—	ns	2
MUX Control Setup Time	t_{VSVE1L} t_{VSVE2H}	t_{VSS}	0	—	0	—	0	—	ns	2
Address Valid to End of Write	t_{AVE1H} t_{AVE2L}	t_{SW}	15	—	20	—	30	—	ns	2
MUX Control Valid to End of Write	t_{VSVE1H} t_{VSVE2L}	t_{VSW}	15	—	20	—	30	—	ns	2
Chip Enable to End of Write	t_{E1LE1H} t_{E2HE2L}	t_{CW}	12	—	15	—	20	—	ns	2, 3
Data Valid to End of Write	t_{DVE1H} t_{DVE2L}	t_{DW}	8	—	10	—	15	—	ns	2
Data Hold Time	t_{E1HDX} t_{E2LDX}	t_{DH}	0	—	0	—	0	—	ns	2, 4
Write Recovery Time	t_{E1HAX} t_{E2LAX}	t_{WR}	0	—	0	—	0	—	ns	2
MUX Control Recovery Time	t_{E1HVSX} t_{E2LVSX}	t_{VSR}	0	—	0	—	0	—	ns	2

NOTES:
1. A write cycle starts at the latest transition of $\overline{E1}$ low, $\overline{W}$ low, or E2 high. A write cycle ends at the earliest transition of $\overline{E1}$ high, $\overline{W}$ high, or E2 low.
2. $\overline{E1}$ in the timing diagrams represents both $\overline{E1}$ and E2 with $\overline{E1}$ asserted low and E2 asserted high.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high the outputs will remain in a high-impedance state.
4. During this time the output pins may be in the output state. Signals of opposite phase must not be applied to the outputs at this time.

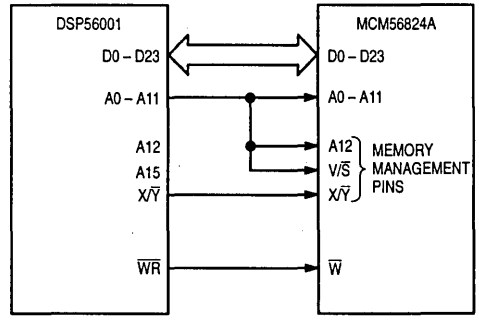
$\overline{E1}$ OR E2 INITIATED WRITE CYCLE



DSPRAM Multiplexed Vector/Scalar Address Maps



8K x 24 DSPRAM Used in Typical Application



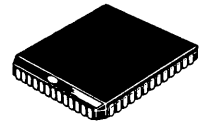
ORDERING INFORMATION
(Order by Full Part Number)

	MCM	56824A	XX	XX	
Motorola Memory Prefix					Speed (20 = 20 ns, 25 = 25 ns, 35 = 35 ns)
Part Number					Package (ZP = OMPAC)

Full Part Numbers — MCM56824AZP20 MCM56824AZP25 MCM56824AZP35
MCM56824AZP20R2 MCM56824AZP25R2 MCM56824AZP35R2

MCM62110

32K x 9 Bit Synchronous Dual I/O or Separate I/O Fast Static RAM with Parity Checker



FN PACKAGE
PLASTIC
CASE 778

The MCM62110 is a 294,912 bit synchronous static random access memory organized as 32,768 words of 9 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 32K x 9 SRAM core with advanced peripheral circuitry consisting of address registers, two sets of input data registers, two sets of output latches, active high and active low chip enables, and a parity checker. The RAM checks odd parity during RAM read cycles. The data parity error ($\overline{DPE}$) output is an open drain type output which indicates the result of this check. This device has increased output drive capability supported by multiple power pins. In addition, the output levels can be either 3.3 V or 5 V TTL compatible by choice of the appropriate output bus power supply.

The device has both asynchronous and synchronous inputs. Asynchronous inputs include the processor output enable ($\overline{POE}$), system output enable ($\overline{SOE}$), and the clock (K).

The address (A0 – A14) and chip enable ($\overline{E1}$ and E2) inputs are synchronous and are registered on the falling edge of K. Write enable ($\overline{W}$), processor input enable ($\overline{PIE}$) and system input enable ($\overline{SIE}$) are registered on the rising edge of K. Writes to the RAM are self-timed.

All data inputs/outputs, PDQ0 – PDQ7, SDQ0 – SDQ7, PDQP, and SDQP have input data registers triggered by the rising edge of the clock. These pins also have three-state output latches which are transparent during the high level of the clock and latched during the low level of the clock.

This device has a special feature which allows data to be passed through the RAM between the system and processor ports in either direction. This streaming is accomplished by latching in data from one port and asynchronously output enabling the other port. It is also possible to write to the RAM while streaming.

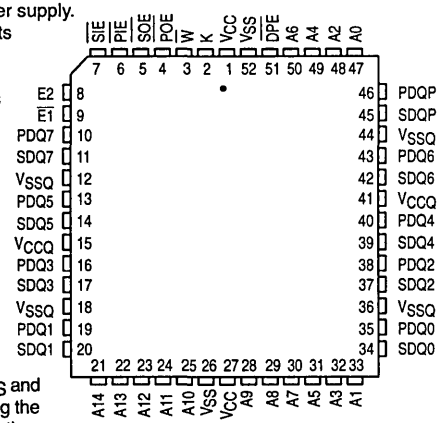
Additional power supply pins have been utilized for maximum performance. The output buffer power (V_{CCQ}) and ground pins (V_{SSQ}) are electrically isolated from V_{SS} and V_{CC}, and supply power and ground only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state thereby allowing simplified transmission line terminations.

The MCM62110 is available in a 52-pin plastic leaded chip carrier (PLCC).

This device is ideally suited for pipelined systems and systems with multiple data buses and multi-processing systems, where a local processor has a bus isolated from a common system bus.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Level Compatibility
- Fast Access and Cycle Times: 15/17/20 ns Max
- Self-Timed Write Cycles
- Clock Controlled Output Latches
- Address, Chip Enable, and Data Input Registers
- Common Data Inputs and Data Outputs
- Dual I/O for Separate Processor and Memory Buses
- Separate Output Enable Controlled Three-State Outputs
- Odd Parity Checker During Reads
- Open Drain Output on Data Parity Error ($\overline{DPE}$) Allowing Wire-ORing of Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 52 Lead PLCC Package
- Active High and Low Chip Enables for Easy Memory Depth Expansion
- Can be used as Separate I/O x9

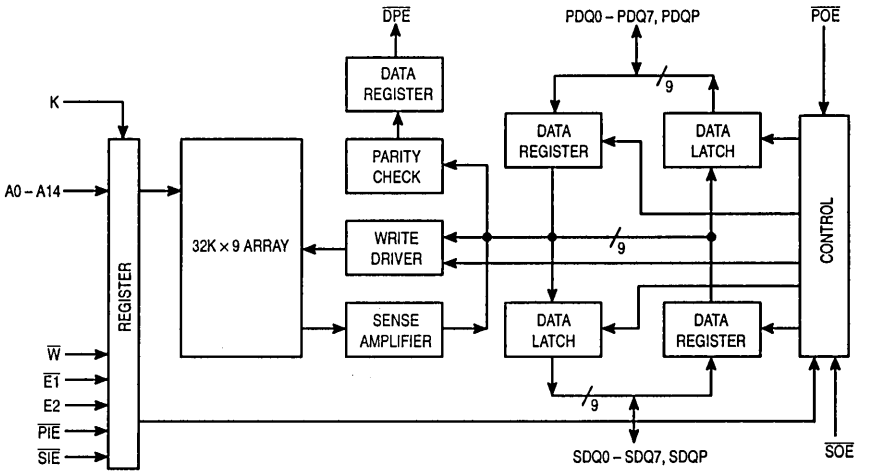
PIN ASSIGNMENT



PIN NAMES	
A0 – A14	Address Inputs
K	Clock Input
$\overline{W}$	Write Enable
$\overline{E1}$	Active Low Chip Enable
E2	Active High Chip Enable
$\overline{PIE}$	Processor Input Enable
$\overline{SIE}$	System Input Enable
$\overline{POE}$	Processor Output Enable
$\overline{SOE}$	System Output Enable
$\overline{DPE}$	Data Parity Error
PDQ0 – PDQ7	Processor Data I/O
PDQP	Processor Data Parity
SDQ0 – SDQ7	System Data I/O
SDQP	System Data Parity
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

BLOCK DIAGRAM



FUNCTIONAL TRUTH TABLE (See Notes 1 and 2)

$\overline{W}$	$\overline{PIE}$	$\overline{SIE}$	$\overline{POE}$	$\overline{SOE}$	Mode	Memory Subsystem Cycle	PDQ0 – PDQ7, PDQP Output	SDQ0 – SDQ7, SDQP Output	$\overline{DPE}$	Notes
1	1	1	0	1	Read	Processor Read	Data Out	High-Z	Parity Out	3, 4
1	1	1	1	0	Read	Copy Back	High-Z	Data Out	Parity Out	3, 4
1	1	1	0	0	Read	Dual Bus Read	Data Out	Data Out	Parity Out	3, 4
1	X	X	1	1	Read	NOP	High-Z	High-Z	1	
X	0	0	X	X	N/A	NOP	High-Z	High-Z	1	2, 5
0	0	1	1	1	Write	Processor Write Hit	Data In	High-Z	1	2, 6
0	1	0	1	1	Write	Allocate	High-Z	Data In	1	2
0	0	1	1	0	Write	Write Through	Data In	Stream Data	1	2, 7
0	1	0	0	1	Write	Allocate With Stream	Stream Data	Data In	1	2, 7
1	0	1	1	0	N/A	Cache Inhibit Write	Data In	Stream Data	1	2, 7
1	1	0	0	1	N/A	Cache Inhibit Read	Stream Data	Data In	1	2, 7
0	1	1	X	X	N/A	NOP	High-Z	High-Z	1	5
X	0	1	0	0	N/A	Invalid	Data In	Stream	1	2, 8
X	0	1	0	1	N/A	Invalid	Data In	High-Z	1	2, 8
X	1	0	0	0	N/A	Invalid	Stream	Data In	1	2, 8
X	1	0	1	0	N/A	Invalid	High-Z	Data In	1	2, 8

NOTES:

1. A '0' represents an input voltage ≤ V_{IL} and a '1' represents an input voltage ≥ V_{IH}. All inputs must satisfy the specified setup and hold times for the falling or rising edge of K. Some entries in this truth table represent latched values. This table assumes that the chip is selected (i.e., $\overline{E1}$ = 0 and E2 = 1) and V_{CC} current is equal to I_{CCA}. If this is not true, the chip will be in standby mode, the V_{CC} current will equal I_{SB1} or I_{SB2} $\overline{DPE}$ will default to 1 and all RAM outputs will be in High-Z. Other possible combinations of control inputs not covered by this note or the table above are not supported and the RAM's behavior is not specified.
2. If either $\overline{IE}$ signal is sampled low on the rising edge of clock, the corresponding $\overline{OE}$ is a don't care, and the corresponding outputs are High-Z.
3. A read cycle is defined as a cycle where data is driven on the internal data bus by the RAM.
4. $\overline{DPE}$ is registered on the rising edge of K at the beginning of the following clock cycle
5. No RAM cycle is performed.
6. A write cycle is defined as a cycle where data is driven onto the internal data bus through one of the data I/O ports (PDQ0 – PDQ7 and PDQP or SDQ0 – SDQ7 and SPDQ), and written into the RAM.
7. Data is driven on the internal data bus by one I/O port through its data input register and latched into the data output latch of the other I/O port.
8. Data contention will occur.

PARITY CHECKER

Parity Scheme	$\overline{DPE}$
$\overline{E1} = V_{IH}$ and/or $E2 = V_{IL}$	1
RAMP = $\overline{RAM0} \oplus \overline{RAM1} \oplus \ldots \oplus \overline{RAM7}$	1
RAMP ≠ $\overline{RAM0} \oplus \overline{RAM1} \oplus \ldots \oplus \overline{RAM7}$	0

NOTE: RAMP, $\overline{RAM0}$, $\overline{RAM1}$ . . . , refer to the data that is present on the RAMs internal bus, not necessarily data that resides in the RAM array. $\overline{DPE}$ is always delayed one clock, and is registered on the rising edge of K at the beginning of the following clock cycle (see AC CHARACTERISTICS).

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply	V_{CC}	− 0.5 to + 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	− 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias	T_{bias}	− 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = V_{SSQ} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	4.5 3.0	5.5 3.6	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{POE}$, $\overline{SOE}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min) MCM62110-15: t_{KHKH} = 15 ns MCM62110-17: t_{KHKH} = 17 ns MCM62110-20: t_{KHKH} = 20 ns	I_{CCA}	 — — —	 190 190 190	mA
TTL Standby Current (V_{CC} = Max, $\overline{E1}$ = V_{IH} or E2 = V_{IL})	I_{SB1}	—	40	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E1}$ = V_{IH} or E2 = V_{IL}, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V)	I_{SB2}	—	30	mA
Output Low Voltage (I_{OL} = + 8.0 mA, $\overline{DPE}$: I_{OL} = + 23.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except I/Os)	C_{in}	2	3	pF
Input/Output Capacitance (PDQ0 – PDQ7, SDQ0 – SDQ7, PDQP, SDQP)	C_{out}	6	7	pF
Data Parity Error Output Capacitance ($\overline{DPE}$)	$C_{out(DPE)}$	6	7	pF

AC SPEC LOADS

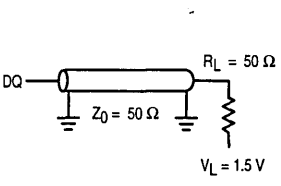


Figure 1A

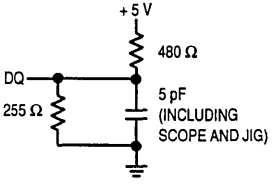


Figure 1B

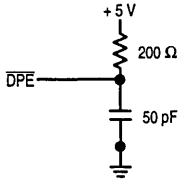


Figure 1C

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

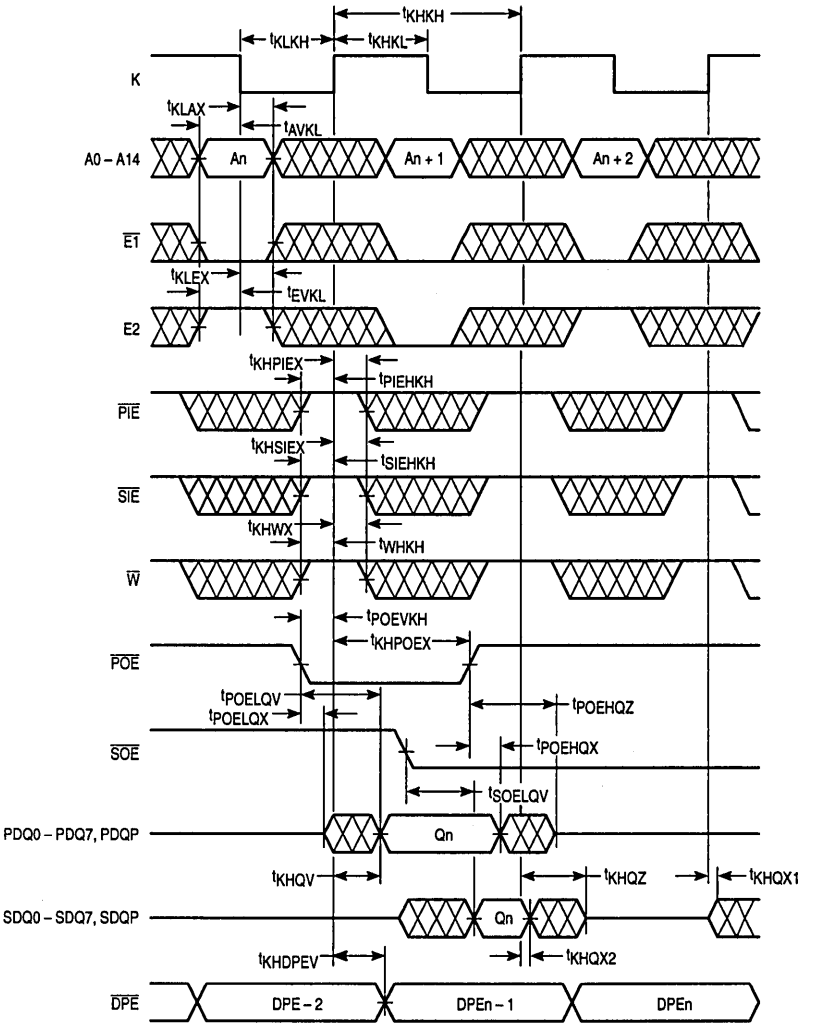
Output Measurement Timing Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	MCM62110-15		MCM62110-17		MCM62110-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time Clock High to Clock High	t_{KHKH}	15	—	17	—	20	—	ns	1, 2
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	7	—	7	—	7	—	ns	
Clock High to $\overline{DPE}$ Valid	t_{KHDPEV}	—	7	—	8	—	10	ns	5
Clock High to Output Valid	t_{KHQV}	—	7	—	7.5	—	10	ns	4, 3
Clock (K) High to Output Low Z After Write	t_{KHQX1}	8	—	8	—	8	—	ns	
Output Hold from Clock High	t_{KHQX2}	5	—	5	—	5	—	ns	4, 6
Clock High to Q High-Z ($\overline{E1}$ or E2 = False)	t_{KHQZ}	—	8	—	9	—	10	ns	6
Setup TImes: A	t_{AVKL}	2.5	—	2.5	—	2.5	—	ns	
$\overline{W}$	t_{WHKH}								
$\overline{E1}$, E2	t_{EVKL}								
$\overline{PIE}$	t_{PIEHKH}								
$\overline{SIE}$	t_{SIEHKH}								
$\overline{POE}$	t_{POEVKH}								7
$\overline{SOE}$	t_{SOEVKH}								7
Hold Times: A	t_{KLAX}	2	—	2	—	2	—	ns	
$\overline{W}$	t_{KHWX}								
$\overline{E1}$, E2	t_{KLEX}								
$\overline{PIE}$	t_{KHPIEX}								
$\overline{SIE}$	t_{KHSIEX}								
$\overline{POE}$	t_{KHPOEX}								7
$\overline{SOE}$	t_{KHSOEX}								7
Output Enable High to Q High-Z	t_{POEHQZ} t_{SOEHQZ}	0	8	0	9	0	9	ns	6
Output Hold from Output Enable High	t_{POEHQX} t_{SOEHQX}	5	—	5	—	5	—	ns	6
Output Enable Low to Q Active	t_{POELQX} t_{SOELQX}	0	—	0	—	0	—	ns	6
Output Enable Low to Output Valid	t_{POELQV} t_{SOELQV}	—	5	—	6	—	8	ns	

NOTES:
1. A read is defined by $\overline{W}$ high for the setup and hold times.
2. All read cycle timing is referenced from K, $\overline{SOE}$, or $\overline{POE}$.
3. Access time is controlled by t_{KLQV} if the clock low pulse width is less than (t_{KLQV}–t_{KHQV}); otherwise it is controlled by KHQV.
4. K must be at a high level for outputs to transition.
5. $\overline{DPE}$ is valid exactly one clock cycle after the output data is valid.
6. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX}, t_{POEHQZ} is less than t_{POELQX} for a given device, and t_{SOEHQZ} is less than t_{SOELQX} for a given device.
7. These read cycle timings are used to guarantee proper parity operation only.

READ CYCLE (See Notes)



NOTES:
1. $\overline{DPE}$ is valid exactly one clock cycle after the output data is valid.

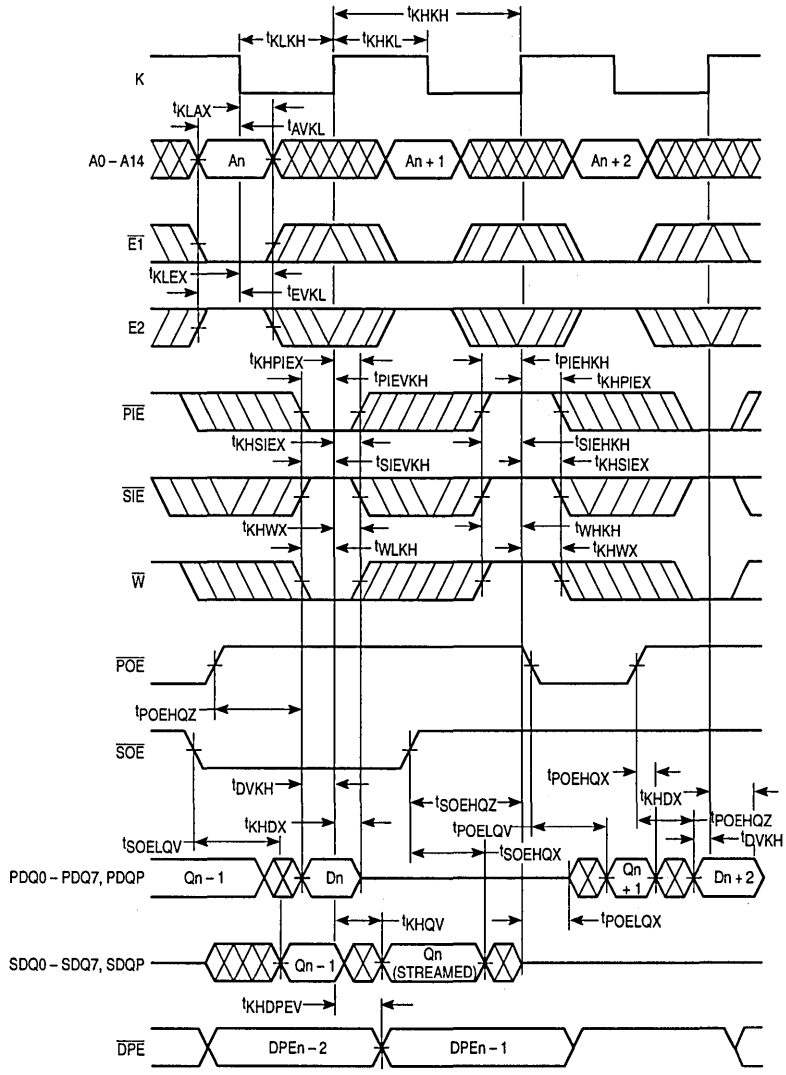
WRITE CYCLE (See Note 1)

Parameter	Symbol	MCM62110-15		MCM62110-17		MCM62110-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times	t_{KHKH}	15	—	17	—	20	—	ns	1, 2
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	7	—	7	—	7	—	ns	
Clock High to Output High-Z ($\overline{W}$ = V_{IL} and $\overline{SIE}$ = $\overline{PIE}$ = V_{IH})	t_{KHQZ}	—	8	—	9	—	10	ns	3, 4
Setup Times: A	t_{AVKL}	2.5	—	2.5	—	2.5	—	ns	
$\overline{W}$	t_{WLKH}								
$\overline{E1}$, E2	t_{EVKL}								
$\overline{PIE}$	t_{PIEVKH}								
$\overline{SIE}$	t_{SIEVKH}								
SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{DVKH}								
Hold Times: A	t_{KLAX}	2	—	2	—	2	—	ns	
$\overline{W}$	t_{KHWX}								
$\overline{E1}$, E2	t_{KLEX}								
$\overline{PIE}$	t_{KHPIEX}								
$\overline{SIE}$	t_{KHSIEX}								
SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{KHDX}								
Write with Streaming ($\overline{PIE}$ = $\overline{SOE}$ = V_{IL} or $\overline{SIE}$ = $\overline{POE}$ = V_{IL}) Clock High to Output Valid	t_{KHQV}	—	7	—	7.5	—	8	ns	5
Output Enable High to Q High-Z	t_{POEHQZ} t_{SOEHQZ}	0	8	0	9	0	9	ns	6
Output Hold from Output Enable High	t_{POEHQX} t_{SOEHQX}	5	—	5	—	5	—	ns	
Output Enable Low to Q Active	t_{POELQX} t_{SOELQX}	0	—	0	—	0	—	ns	6
Output Enable Low to Output Valid	t_{POELQV} t_{SOELQV}	—	5	—	6	—	8	ns	

NOTES:

1. A write is performed with $\overline{W}$ = V_{IL}, $\overline{E1}$ = V_{IL}, E2 = V_{IH} for the specified setup and hold times and either $\overline{PIE}$ = V_{IL} or $\overline{SIE}$ = V_{IL}. If both $\overline{PIE}$ = V_{IL} and $\overline{SIE}$ = V_{IL} or $\overline{PIE}$ = V_{IH} and $\overline{SIE}$ = V_{IH}, then this is treated like a NOP and no write is performed.
2. All write cycle timings are referenced from K.
3. K must be at a high level for the outputs to transition.
4. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX} for a given device.
5. A write with streaming is defined as a write cycle which writes data from one data bus to the array and outputs the same data onto the other data bus.
6. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX}, t_{POEHQZ} is less than t_{POELQX} for a given device, and t_{SOEHQZ} is less than t_{SOELQX} for a given device.

WRITE THROUGH — READ — WRITE (See Note)



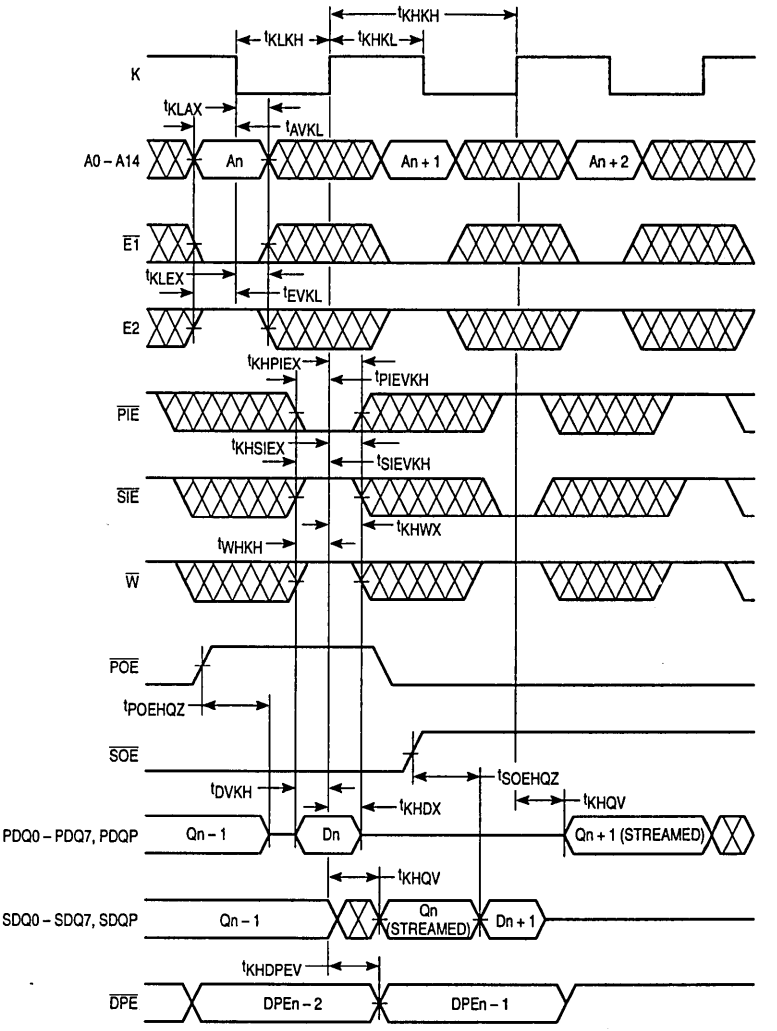
NOTE: $\overline{DPE}$ is valid exactly one clock cycle after the output data is written.

STREAM CYCLE (See Note 1)

Parameter	Symbol	MCM62110-15		MCM62110-17		MCM62110-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Stream Cycle Time	t_{KHKH}	15	—	17	—	20	—	ns	1, 2
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	7	—	7	—	7	—	ns	
Stream Access Time	t_{KHQV}	—	7	—	7.5	—	8	ns	
Setup Times: A $\overline{W}$ $\overline{E1}$, E2 $\overline{PIE}$ $\overline{SIE}$ SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	 t_{AVKL} t_{WHKH} t_{EVKL} t_{PIEVKH} t_{SIEVKH} t_{DVKH}	2.5	—	2.5	—	2.5	—	ns	
Hold Times: A $\overline{W}$ $\overline{E1}$, E2 $\overline{PIE}$ $\overline{SIE}$ SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	 t_{KLAX} t_{KHWX} t_{KLEX} t_{KHPIEX} t_{KHSIEX} t_{KHDX}	2	—	2	—	2	—	ns	
Output Enable High to Q High-Z	t_{POEHQZ} t_{SOEHQZ}	0	8	0	9	0	9	ns	3
Output Enable Low to Q Active	t_{POELQX} t_{SOELQX}	0	—	0	—	0	—	ns	3
Output Enable Low to Output Valid	t_{POELQV} t_{SOELQV}	—	5	—	6	—	8	ns	

NOTES:
1. A stream cycle is defined as a cycle where data is passed from one data bus to the other data bus.
2. All stream cycle timing is referenced from K.
3. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{POEHQZ} is less than t_{POELQX}, t_{SOEHQZ} is less than t_{SOELQX}, and t_{KHQZ} is less than t_{KHQX} for a given device.

STREAM CYCLE (See Note)



NOTE: $\overline{DPE}$ is valid exactly one clock cycle after the output data is valid.

ORDERING INFORMATION
(Order by Full Part Number)

MCM 62110 FN XX

Motorola Memory Prefix — MCM

Part Number — 62110

Package (FN = PLCC) — FN

Speed (15 = 15 ns, 17 = 17 ns, 20 = 20 ns) — XX

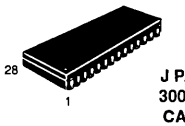
Full Part Numbers — MCM62110FN15 MCM62110FN17 MCM62110FN20

MCM62X308

Product Preview

Synchronous Line Buffer: 8K X 8 Bit Fast Static Dual Ported Memory

With IEEE Standard 1149.1 Test Access Port and Boundary-Scan (JTAG)



J PACKAGE
300 MIL SOJ
CASE 810B

The MCM62X308 is a synchronous, dual ported memory organized as 8,192 words of 8 bits each, fabricated using Motorola's double-metal, double-poly, 0.65 µm CMOS process. It is intended for high speed video or other applications which process data on a line-by-line basis. Through the use of a single clock and port control inputs, separate read and write data ports provide simultaneous access to a common memory array. Simultaneous read/write access to the same address location is also allowed, with old data being read followed by a write of the new data. This allows multiple devices to be cascaded with the output of one directly driving the input of another. In this configuration the data stream can be tapped at strategic interconnect points to perform various digital filtering functions.

Since there are no external address inputs, separate internal Read and Write Address Counters are provided as a means of indexing the memory array. These counters are preloaded and then selectively incremented or decremented by asserting Read Enable (RE) and Write Enable(WE) inputs, allowing cycle to cycle control. The address counters can be reloaded back to their initial values through the use of the Read Reload ($\overline{RR}$) and Write Reload ($\overline{WR}$) control inputs. These inputs initiate the transfer of Address Reload Register values into the Address Counters which index the memory array. When an address counter reaches 0000 (on down count) or FFFF (on up count), it will roll over on the next count. The TDI input is used to write the Reload Registers using special Test Access Port instructions.

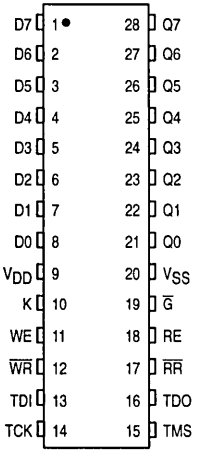
The Address Counters are 16 bits long, and only 13 of the 16 bits are required to index the 8K deep memory array. The remaining three bits are used for depth expansion. These three bits are compared to the lower three bits in the control register and as long as they are equal that port will remain active. If the bits do not compare the port will become inactive, however the counter will continue to count on the rising edge of K as long as the port enable signal (RE or WE) is asserted. The TDI input is used to write the Control Register using special Test Access Port instructions.

The Output Enable Input can be programmed to be either synchronous or asynchronous through the Control Register.

The MCM62X308 is available in a 28 pin SOJ package.

- 8K x 8 Fast Access Static Memory Array
- Single 5 V Power Supply —MCM62X308-15-5: ± 5%
  MCM62X308-17: ± 10%
- Synchronous, Simultaneous Read/Write Memory Access
- 50 MHz Maximum Clock Cycle Time, < 15 ns Read Access
- Single Clock Operation
- Separate Read/Write Address Counters with Reload Control
- Separate Up/Down Counter Control for Both Read and Write
- Programmable Output Enable Control (Synchronous or Asynchronous)
- Cascadable I/O Interface
- IEEE Standard 1149.1 Test Port (JTAG)
- Expand ID Register for Depth Expansion
- High Board Density SOJ Package
- Fully TTL Compatible

PIN ASSIGNMENT

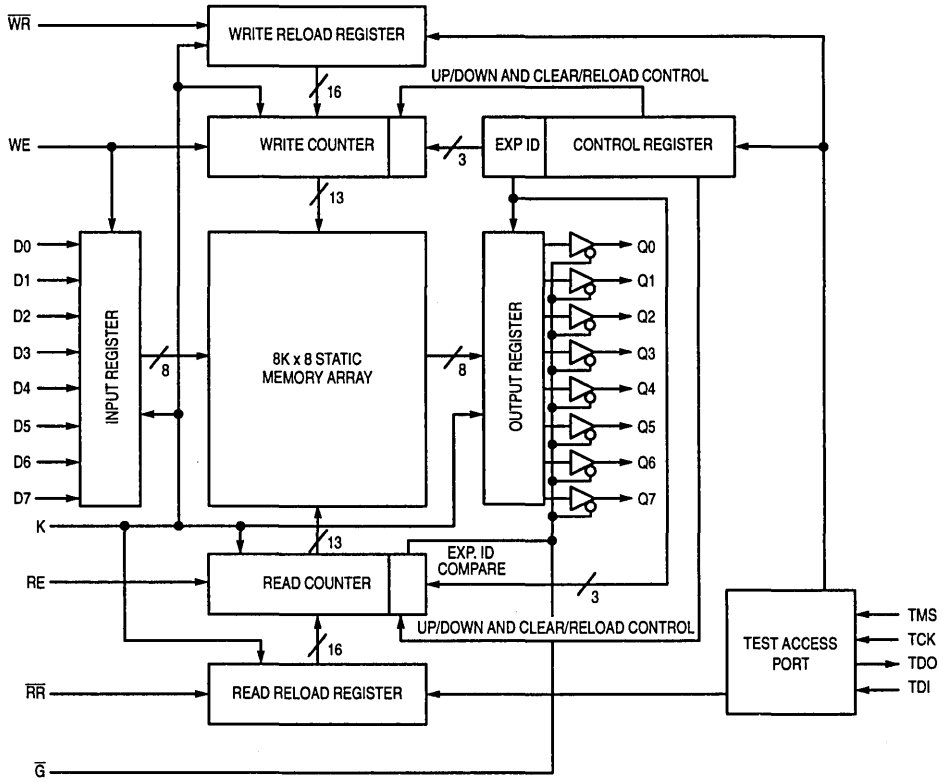


PIN NAMES

K	Clock Input
WE	Write Enable Input
$\overline{WR}$	Write Address Reload Input
RE	Read Enable Input
$\overline{RR}$	Read Address Reload Input
$\overline{G}$	Output Enable Input
D0 – D7	Data Inputs
Q0 – Q7	Data Outputs
TCK	Test Clock Input
TMS	Test Mode Select
TDI	Test Data Input
TDO	Test Data Output
V_{DD}	+ 5 V Power Supply
V_{SS}	Ground

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM



TRUTH TABLE (X = Don't Care)

WE	$\overline{WR}$	RE	$\overline{RR}$	$\overline{G}$	Match EXP ID (Read/Write)	Mode (Read/Write)	Supply Current	Q0 – 7 Status
X	L	X	L	L	Match Read/Match Write	Reload, Read/Reload, Write Disable	I_{CC}	Data Out
H	H	H	H	L	Match Read/Match Write	Count then Read/Write then Count	I_{CC}	Data Out
L	H	L	H	L	Match Read/Match Write	Read Count Disable/Write Disable	I_{CC}	Data Out
H	H	H	H	H	Match Read/Match Write	Count, Read/Count, Write	I_{CC}	High-Z
H	H	H	H	X	No Match Read/Match Write	Count, No Read/Count, No Write	I_{SB}	High-Z
H	H	L	H	X	No Match Read/Match Write	Count, No Read/Count, Write	I_{SB}	High-Z

MAXIMUM RATINGS* (Voltages Referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISITICS

(T_A = 0 to 70 °C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	MCM62X308-15-5	V_{DD}	4.75	5.0	5.25	V
	MCM62X308-17		4.50	5.0	5.50	
Input High Voltage		V_{IH}	2.2	—	V_{DD} + 0.3	V
Input Low Voltage		V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH}, V_{out} = 0 to V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, I_{out} = 0 mA, All Inputs ≥ V_{IL} = 0.0 V and V_{IH} ≥ 3.0, Cycle Time = 20 ns)	I_{CCA}	—	150	mA
AC Standby Current (When Expand ID Bits Do Not Match the Read Address Counter, Cycle Time = 20 ns)	I_{SB}	—	100	mA
Output Low Voltage (I_{OL} = + 4.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance (Q0 – Q7, TDO)	C_{out}	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Output Load ..... Terminated 50 Ohm Transmission Line

READ/WRITE CYCLE TIMING

Parameter	Symbol Std	Symbol Alt	MCM62X308-15-5 Min	MCM62X308-15-5 Max	MCM62X308-17 Min	MCM62X308-17 Max	Unit	Notes
Cycle Time	t_{KHKH}	t_{CYC}	20	—	22	—	ns	
Clock High Time	t_{KHKL}	t_{CKH}	8	—	9	—	ns	
Clock Low Time	t_{KLKH}	t_{CKL}	8	—	9	—	ns	
Clock High to Output Valid	t_{KHQV}	t_{CD}	5	15	5	17	ns	
Clock High to Output High-Z	t_{KHQZ}	t_{CZ}	5	15	5	15	ns	1
Output Enable Low to Output Valid	t_{GLQV}	t_{OLV}	3	10	3	10	ns	2, 4
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	5	0	5	ns	2, 3, 4
Setup Times: RE	t_{REVKH}	t_S	2	—	2	—	ns	5
WE	t_{WEVKH}							
$\overline{WR}$	t_{WRVKH}							
$\overline{G}$	t_{GVKH}							6
$\overline{RR}$	t_{RRVKH}		3	—	3	—		5
Data In	t_{DVKH}		1	—	1	—		5
Hold Times: RE	t_{KHREX}	t_H	2	—	2	—	ns	5
WE	t_{KHWEX}							
$\overline{RR}$	t_{KHRRX}							
$\overline{WR}$	t_{KHWRX}							
$\overline{G}$	t_{KHGX}							6
Data In	t_{KHDX}							

NOTES:
1. The outputs High-Z from a clock high edge when the upper three bits of the Read Address Counter do not match the 3 ID Expansion bits.
2. $\overline{G}$ is a don't care when the three ID expansion bits do not match the upper three bits of the Read Address Counter.
3. t_{GLQV} and t_{GHQZ} only apply when $\overline{G}$ is programmed as Asynchronous. (See TAP LDCONT instruction).
4. Transition is measured ± 500 mV from steady-state voltage. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{GHQZ} max is less than t_{GLQV} min for a given device and from device to device.
5. This is a synchronous device. All inputs must meet the specified setup and hold times for ***ALL*** rising edges of Clock except for $\overline{G}$ when it is programmed to be asynchronous.
6. t_{GVKH} and t_{KHGX} only apply when $\overline{G}$ is programmed as synchronous.

AC TEST LOADS

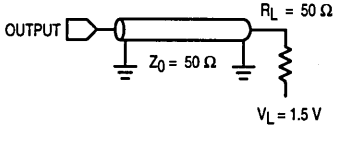


Figure 1A

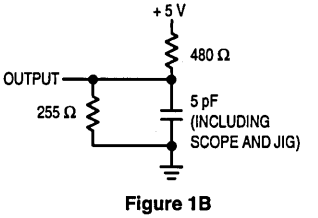


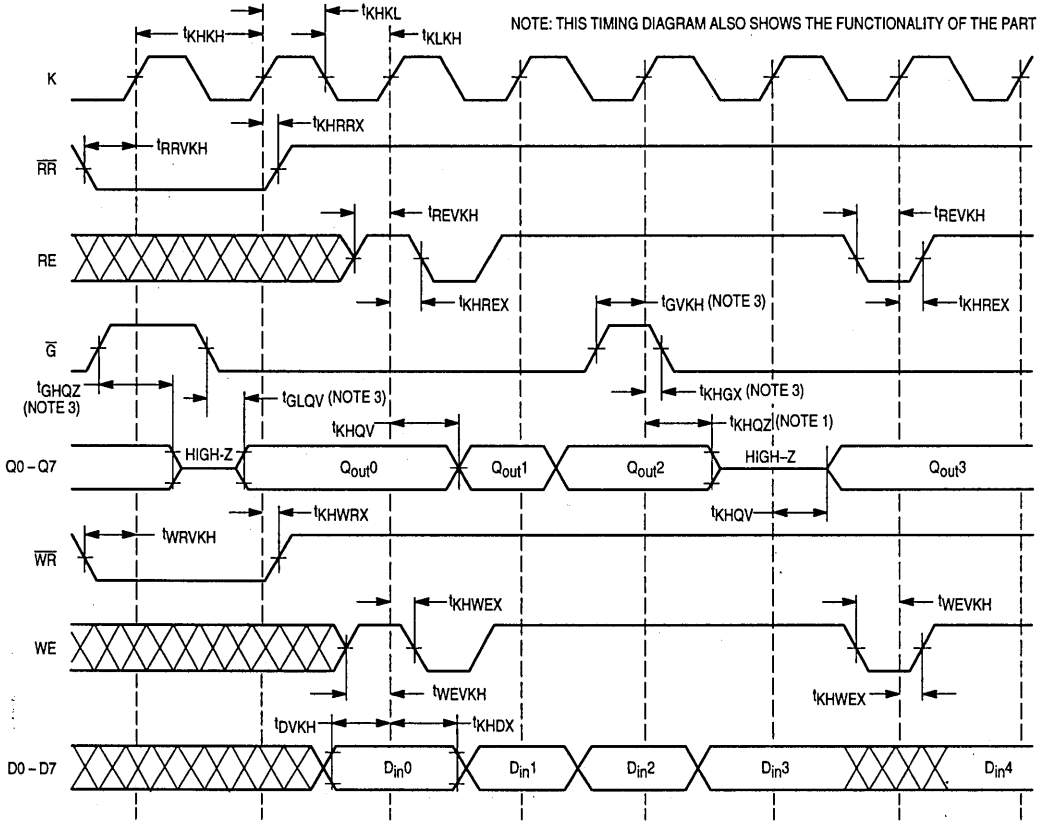
Figure 1B

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

4

READ/WRITE CYCLE TIMING DIAGRAM



AC OPERATING CONDITIONS AND CHARACTERISTICS FOR THE TEST ACCESS PORT (IEEE 1149.1)

(T_A = 0 to + 70°C, Unless Otherwise Noted)

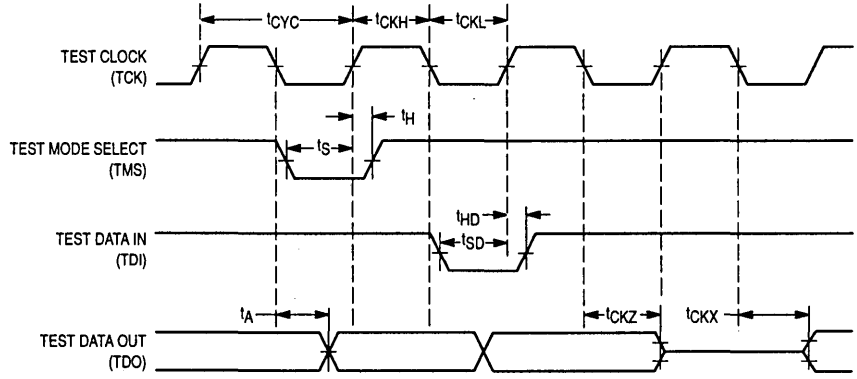
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Output Load ..... 50 Ohm Transmission Line

TAP CONTROLLER TIMING

Parameter	Symbol	MCM62X308-15-5		MCM62X308-17		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{CYC}	30	—	30	—	ns	
Clock High Time	t_{CKH}	12	—	12	—	ns	
Clock Low Time	t_{CKL}	12	—	12	—	ns	
Clock Low to Output Valid	t_A	5	9	5	9	ns	
Clock Low to Output High-Z	t_{CKZ}	0	9	0	9	ns	1
Clock Low to Output Active	t_{CKX}	0	9	0	9	ns	2, 3
Setup Time, Test Mode Select	t_S	2	—	2	—	ns	
Setup Time, Test Data In	t_{SD}	2	—	2	—	ns	
Hold Time, Test Mode Select	t_H	2	—	2	—	ns	
Hold Time, Test Data In	t_{HD}	2	—	2	—	ns	

NOTES:
1. Test Data Out will High-Z from a clock low edge depending on the current state of the TAP state machine.
2. Test Data Out is active only in the SHIFT-IR and SHIFT-DR state of the TAP state machine.
3. Transition is measured ± 500 mV from steady-state voltage. This parameter is sampled and not 100% tested.

TAP CONTROLLER TIMING DIAGRAM



PIN DESCRIPTIONS

K — CLOCK INPUT

System clock input pin accepting a minimum 8 ns clock high or clock low pulse at a minimum 20 ns clock cycle. All other synchronous inputs excluding the Test Access Port are captured on the rising edge of this signal.

WE — WRITE ENABLE INPUT

Write Enable is captured on K leading edge. When asserted this causes the input data D0 – D7 to be written into the RAM address controlled by the Write Address Counter and increments the counter for the next write.

RE — READ ENABLE INPUT

Read Enable is captured on K leading edge. When asserted this causes a RAM read access from address controlled by the Read Address Counter to be inserted in the output register Q0 – Q7 and increments the counter for the next read operation.

$\overline{WR}$ — WRITE RELOAD INPUT

Write Reload is captured on K leading edge. When asserted this causes the Write Address Counter to be initialized to the contents of the Write Reload Register or "cleared" as specified by Control Register bit 3. See Control Register Bit 4 for "cleared" description.

$\overline{RR}$ — READ RELOAD INPUT

Read Reload is captured on K leading edge. When asserted this causes the Read Address Counter to be initialized to the contents of the Read Reload Register or "cleared" as specified by Control Register bit 5. See Control Register Bit 6 for "cleared" description.

$\overline{G}$ — OUTPUT ENABLE INPUT

When asserted low causes the outputs Q0 – Q7 to become active and when deasserted high causes them to High-Z. This pin can be either synchronous with K leading edge or asynchronous as specified by Control Register Bit 7.

D0 – D7 — DATA INPUTS

The levels on these pins is captured on the K leading edge. The value captured will be written into the RAM if WE is also asserted and the Expand ID bits match the upper three bits of the Write Address Counter.

Q0 – Q7 — DATA OUTPUTS

Data outputs are available from the Read Output Register < 15 ns from the rising edge of K when RE or $\overline{RR}$ is asserted. Outputs are disabled when the upper three bits of the Read Address Counter do not match the three Expand ID bits of the Control Register. $\overline{G}$ will also control the disabling of the outputs either synchronously or asynchronously. See $\overline{G}$ description.

TEST ACCESS PORT PIN DESCRIPTIONS

The Test Access Port conforms with the IEEE Standard 1149.1. It is also used to load device specific registers used to configure the MCM62X308.

TCK — TEST CLOCK INPUT

Samples and clocks all TAP events. All inputs are captured on TCK rising edge and all outputs propagate from TCK falling edge. It also can take the place of K in device operation in certain test conditions.

TMS — TEST MODE SELECT INPUT

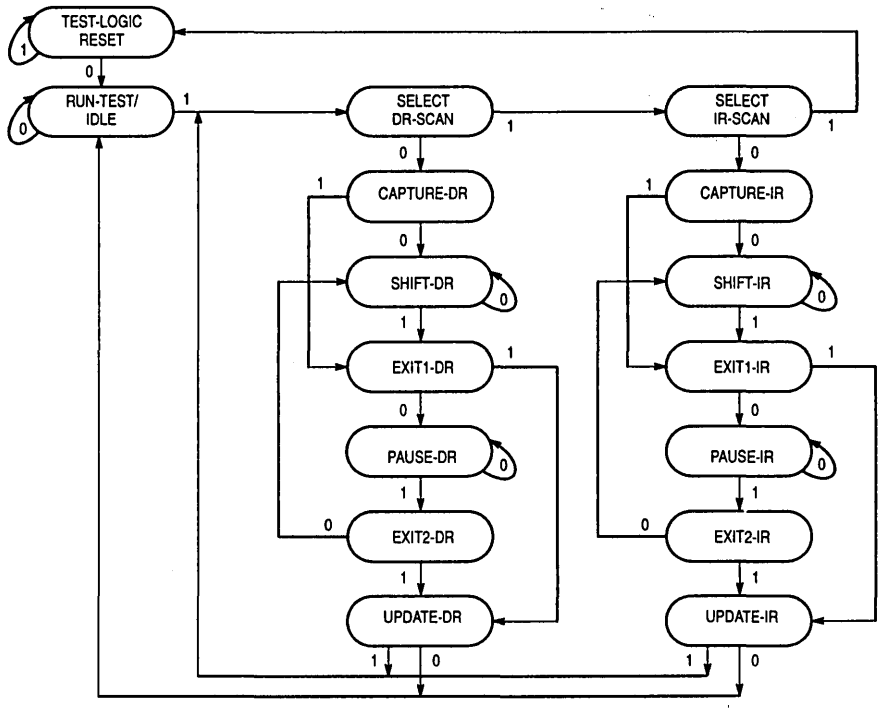
Sampled on the rising edge of TCK. Determines the movement through the TAP state machine (Figure 2). This circuit is designed in such a way that an undriven input will produce a response identical to the application of a logic 1.

TDI — TEST DATA IN INPUT

Sampled on the rising edge of TCK. This is the input side of the serial register placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP state machine and what instruction is active in the TAP instruction register. This circuit is designed in such a way that an undriven input will produce a response identical to the application of a logic 1.

TDO — TEST DATA OUT OUTPUT

Output that is active depending on the state of the TAP state machine. Output changes off the trailing edge of TCK. This is the output side of the serial register placed between TDI and TDO.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 2. TAP Controller State Diagram

TEST ACCESS PORT DESCRIPTIONS

INSTRUCTION SET

A four pin IEEE Standard 1149.1 Test Port (JTAG) is included on this device. There are two classes of instructions; standard instructions as defined in the IEEE 1149.1 standard and device specific, or public, instructions that are used to control the functionality of the device. When the TAP (Test Access Port) controller is in the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction would be serially loaded through the TDI input (while 0101 will be shifted out of TDO). The TAP instruction set for this device is listed in Table 1.

TAP STANDARD INSTRUCTION SET

NOTE: The descriptions in this section are not intended to be used without the supporting IEEE 1149.1-1993 Standard.

SAMPLE/PRELOAD TAP INSTRUCTION

The SAMPLE/PRELOAD TAP instuction is used to allow scanning of the boudary-scan register without causing interference to the normal operation of the chip logic. The 21 bit boundary scan register contains bits for all device signal and clock pins and associated control signals (Table 2). This register is accessible when the SAMPLE/PRELOAD TAP instruction is loaded into the TAP instruction register in the Shift-IR state. When the TAP controller is then moved to the Shift-DR state, the boundary scan register is placed between TDI and TDO. This scan register can then be used prior to the EXTEST instruction to preload the output pins with desired values so that these pins will drive the desired state when the EXTEST instruction is loaded. See the EXTEST instruction explanation below. It could also be used prior to the INTEST instruction to preload values into the input pins. As data is written into TDI, data also streams out of TDO which can be used to pre-sample the inputs and outputs. SAMPLE/PRELOAD would also be used prior to the CLAMP instruction to preload the values on the output pins that will be driven out when the CLAMP instruction is loaded.

Table 2 shows the boundary-scan bit definitions. The first column defines the bit's ordinal position in the boundary-scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 0; the last bit to be shifted is 21. The second column is the pin name and the third column is the pin type.

EXTEST TAP INSTRUCTION

The EXTEST instruction is intended to be used in conjunction with the SAMPLE/PRELOAD instruction to assist in testing board level connectivity. Normally, the SAMPLE/PRELOAD instruction would be used to preload all output pins (i.e., Q0 – Q7). The EXTEST instruction would then be loaded. During EXTEST the boundary-scan register is placed between TDI and TDO in the Shift-DR state of the TAP controller (Table 2). Once the EXTEST instruction is loaded, the TAP controller would then be moved to the Run-Test/Idle state. In this state one cycle of TCK would cause the preloaded data on the ouput pins to be driven while the values on the input pins would be sampled (Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero). Note that TCK, not the Clock pin, K, is used as the clock input while K is only sampled during EXTEST. After one clock cycle of TCK, the TAP controller would then be moved to the Shift-DR state where the sampled values would be shifted out of TDO (and new values would be shifted in TDI). These values would normally be compared to expected values to test for board connectivity.

THE INTEST TAP INSTRUCTION

The INTEST instruction is intended to be used to assist in testing internal device functionality. When the INTEST instruction is loaded the boundary-scan register is placed between TDI and TDO in the Shift-DR state of the TAP controller (Table 2). While in the Shift-DR state, all input pins would be preloaded via the boundary scan register to set up the desired mode (i.e., read, write, reload, etc.). The TAP controller would then be moved to the Run-Test/Idle state. In this state one or more cycles of TCK would cause the preloaded data in the boundary-scan register to be driven while the values of Q0 – Q7 would be sampled (Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero, however the values of Q0 – Q7 will

Table 1. TAP Instruction Set

Instruction	Code (Binary)	Description
Standard Instructions:		
BYPASS	1111*	Bypass Instruction
INTEST	0111	Intest Instruction
SAMPLE/PRELOAD	1100	Sample and/or Preload Instruction
EXTEST	0000	Extest Instruction
HIGHZ	1010	High-Z all Output pins while bypass reg. is between TDI and TDO
CLAMP	1001	Clamp Output pins while bypass reg. is between TDI and TDO
Device Specific (Public) Instructions:		
LDRREG	0001	Load Read Address Reload Register
LDWREG	0100	Load Write Address Reload Register
LDBREG	0101	Load both Address Reload Registers (Write then Read)
LDCONT	0010	Load Control Register
RDCOUNT	1000	Read the values of the Read and Write Address Counters
EZWRITE	0011	Serial Write (using Write Address Counter)
EZREAD	0110	Serial Read (using Read Address Counter)
EZREADZ	1110	Serial Read, outputs High-Z

*Default state at power-up.

be sampled regardless of $\overline{G}$). Only one action will be performed in the Run-Test/Idle state no matter how many clock cycles are input. Note that TCK, not the Clock pin(K), is used as the clock input while K is ignored during INTEST. After one or more clock cycles of TCK, the TAP controller would then be moved to the Shift-DR state where the sampled values would be shifted out of TDO (and new values would be shifted in TDI). These values would normally be compared to expected values to test for device functionality.

Since device functionality can only be verified through sampling the outputs of the device, the most likely use of INTEST would be to first load up the boundary-scan register for a Write Reload and execute the reload in the Run-Test/Idle state. Then a write of the first address would be performed again using the boundary scan register to load up the input registers and executing the write in the Run-Test/Idle state. Lastly, a Read Reload would be executed in the same manner so that the data that had just been written in the first address would be read from the memory array and written into the output registers which would then be shifted out of TDO in the Shift-DR state.

CLAMP TAP INSTRUCTION

The CLAMP instruction is provided to allow the state of the signals driven from the output pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the output pins will not change while the CLAMP instruction is selected. EXTEST could also be used for this purpose but CLAMP shortens the board scan path by inserting only the bypass register between TDI and TDO. To use CLAMP, the SAMPLE/PRELOAD instruction would be used first to scan in the values to be driven on the output pins when the CLAMP instruction is active. Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero.

HIGH-Z TAP INSTRUCTION

The High-Z instruction is provided to allow all the outputs to be placed in an inactive drive state (High-Z). During the High-Z instruction the bypass register is connected between TDI and TDO.

BYPASS TAP INSTRUCTION

The Bypass instruction is the default instruction loaded in at power up. This instruction will place a single shift register between TDI and TDO during the Shift-DR state of the TAP controller. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

Table 2. Sample/Preload Boundary Scan Register Bit Definitions

Bit Number	Pin Name	Pin Type
0	$\overline{RR}$	Input
1	RE	Input
2	$\overline{G}$	Input
3	Q0	Output
4	Q1	Output
5	Q2	Output
6	Q3	Output
7	Q4	Output
8	Q5	Output
9	Q6	Output
10	Q7	Output
11	D7	Input
12	D6	Input
13	D5	Input
14	D4	Input
15	D3	Input
16	D2	Input
17	D1	Input
18	D0	Input
19	K	Input
20	WE	Input
21	$\overline{WR}$	Input

NOTE: K is a sample-only scan bit. It cannot be preloaded for control purposes.

4

DEVICE SPECIFIC (PUBLIC) INSTRUCTIONS

LDCONT INSTRUCTION

The Control Register is an eight bit register that contains the control bits for the Address Registers and Counters and the Output Enable pin. When the LDCONT TAP instruction is loaded into the Instruction Register, the Control Register is placed between TDI and TDO when the TAP controller is in the Shift-DR state (Table 10). The power-up/preload state and function of the Control bits are found in Table 3.

The Expand ID bits provide system depth expansion. These three bits are compared to the upper three bits in the address counters. As long as the three Expand-ID bits match the three upper bits in the address counters the port will stay active. If they do not match, the port will deactivate (i.e., outputs will High-Z or write will be disabled); however, the counters will continue counting as long as RE and WE remain asserted (i.e., high) at the rising edge of Clock.

The Reload Control bits (3 and 5) are used to control either reloading the Read and Write Address Counters from the Reload Registers or clearing the counter when $\overline{RR}$ or $\overline{WR}$ is asserted. If these bits are set low the counters they control will be cleared to all zeroes if the appropriate reload signal ($\overline{RR}$ or $\overline{WR}$) is asserted and any value in the Reload Register is ignored. This means that if the initial address value desired is address 0000 (or FFFF when counting down) then there is no need to load the Address Reload Registers using the LDRREG, LDWREG, or the LDBREG instructions in the following description. If these bits are set high the counters are loaded up with the values in the Reload Registers when the appropriate reload signal ($\overline{RR}$ or $\overline{WR}$) is asserted.

The Up/Down count bits (4 and 6) determine the direction in which the respective Address Counter will count; if the bit is set low the counter will count up and if set high the counter will count down. If the counters are set to count down and the Reload control is set to the clear counter mode, then the initial value in the counters will be FFFF. To ensure that the counter will function properly, a reload (using $\overline{RR}$ or $\overline{WR}$) is required after the count direction is switched.

The Output Enable control bit (7) determines the functionality of the Output Enable pin, $\overline{G}$. When the bit is low, $\overline{G}$ functions asynchronously. When set high, $\overline{G}$ functions synchronously and must meet the specified setup and hold times to the Clock K.

The Control Register will also be preloaded. When the instruction 0010 (LDCONT) is in the Instruction Register and the controller is in the Capture-DR state the above preload values (all zeroes) will be loaded into the Control Register. All zeroes will also be loaded in the Control Register at power-up.

While new values are shifted in from TDI in the Shift-DR state, all zeroes will be output on TDO for the first eight bits.

LDRREG, LDWREG, AND LDBREG TAP INSTRUCTIONS

There are three instructions that may be used to load the 16 bit address reload registers: LDRREG (Load Read Address Reload Register), LDWREG (Load Write Address Reload Register), and LDBREG (Load both Address Reload Registers, Write followed by Read). Figure 3 illustrates how the Reload registers are placed between TDI and TDO. Tables 7, 8, and 9 describe each register. These instructions would be used only if the user needed to load the Reload Registers with a non-zero value. If the Address Counters are to always be reset to zeroes (or all 1s if counting down) then only the Control Register need be loaded to affect a reset of the counters.

The TAP controller has been set up to make it easier for the user to serially load the Reload Registers. When the TAP controller is clocked into the Capture-IR state (see state diagram) the instruction for loading both registers (0101) will be preloaded into the shift register. This allows the user to go directly to the Update-IR instead of having to serially shift this instruction in through the TDI port. Once the load instruction has been entered the user can then clock over to the Capture-DR state where the value for the reload register(s) is serially loaded (see Figure 3).

RDCOUNT TAP INSTRUCTION

The RDCOUNT scan register is accessible after the RDCOUNT instruction is loaded into the TAP instruction register in the Shift-IR state and the TAP controller is then moved to the Shift-DR state. This scan register can then be used to shift out the values of the Read and Write Address Counters The RDCOUNT scan-register is a sample only register and can not be used to load values into the counters. See Table 4.

EZWRITE TAP INSTRUCTION AND SCAN PATH

The EZWRITE TAP instruction is provided to allow the user to more easily and quickly write a large number of bytes to the device serially through the TDI port. EZWRITE shortens the scan path for a serial write to just the 8 bit Data in register (see Table 5).

The most likely use of this instruction is as follows: the user would first load the Control Register using the LDCONT instruction. This would initialize the Expand ID bits and the Write Counter. The Write Reload Register will need to be

Table 3. Control Register Bit Description

Bit No.	Power Up and Preload State	Function
0 – 2	000	Expand ID bits for comparison with the upper 3 bits of the Read and Write Address counters
3	0	Reload Control of Write Address Counter (0 = clear counter, 1 = reload)
4	0	Up/Down count bit for Write Address Counter (0 = count up, 1 = count down)
5	0	Reload Control of Read Address Counter (0 = clear counter, 1 = reload)
6	0	Up/Down count bit for Read Address Counter (0 = count up, 1 = count down)
7	0	$\overline{G}$ Control (0 = asynchronous, 1 = synchronous)

loaded using the LDWREG instruction if a non-zero starting address is desired. If 0000 was the first desired count, setting up the Control Register to "clear" the Write counter is all that is required (Bit 3 set to zero). A reload cycle using SAMPLE/PRELOAD ($\overline{WR}$ preloaded low) and INTEST would also have to be run in order to initialize the counter. While still in the INTEST instruction at the Shift-DR state, the proper values of WE and $\overline{WR}$ would then need to be preloaded for proper operation of EZWRITE (WE high and $\overline{WR}$ high). After all this initializing is done, the EZWRITE instruction would be loaded into the TAP instruction register in the Shift-IR state. When the TAP controller is then moved to the Shift-DR state the EZWRITE scan path would be inserted between TDI and TDO. This scan path is composed of the 8 bit Data In register (see Table 5). The 8 bits to be written into the first address would be scanned in (sampled values from the Data In pins would be streaming out of TDO at the same time), then the TAP controller would be moved to the Run-Test/Idle state where one cycle of TCK would write the 8 bits into the address and increment the counter. The TAP controller would then move back to the Shift-DR state so that the next byte to be written can be serially loaded and the process would be repeated until all desired bytes were written. During EZWRITE the Q0 – Q7 pins will be in a High-Z state.

EZREAD TAP INSTRUCTION AND SCAN PATH

The EZREAD TAP instruction is provided to allow the user to more easily and quickly read a large number of bytes from the device serially through the TDO port. EZREAD shortens the scan path for a serial read to just the 8 bit Data Out register (see Table 6).

To serially read the device the following would occur: initialization would be much like EZWRITE except that the Read Address Counter should be reladed with the count BEFORE the first one desired. So, if the first read needed to be address 0000 (and the counter is counting up), the Read Reload Register would have to be preloaded with FFFF using the LDRREG instruction. Again, SAMPLE/PRELOAD and INTEST instructions would need to be run to perform a reload cycle followed by another Boundary-scan that set RE and $\overline{RR}$ high in anticipation of the EZREAD instruction. Also, WE should be set low to prevent any unintended writes while reading. After this initializing, the EZREAD instruction would be loaded into the TAP instruction register in the Shift-IR state. The TAP controller would move to the Run-Test/Idle state where one cycle of TCK would increment the counter, read the 8 bits from that address, and load them into the Data Output register. The TAP controller would then move to the Shift-DR state and the EZREAD scan path would be inserted between TDI and TDO. This scan path is composed of the 8 bit Data Out register (see Table 6). In the Shift-DR state the Data Out register would be serially scanned out of the TDO port. This sequence through the TAP state machine would then be repeated until all desired bytes were read. EZREAD keeps the Q0 – Q7 pins active (if $\overline{G}$ is preloaded low) to allow parallel reading of the data out if desired.

EZREADZ TAP INSTRUCTION AND SCAN PATH

The EZREADZ TAP instruction behaves exactly like the EZREAD instruction except that the all outputs are held in a High-Z mode once the instruction is loaded.

DISABLING THE TEST ACCESS PORT AND BOUNDARY SCAN

It is possible to use this device without utilizing the four pins used for the IEEE 1149.1 Test Access Port. To circuit disable the TAP controller without interfering with normal operation of the device TCK must be tied to V_{SS} to preclude midlevel inputs. Although TDI and TMS is designed in such a way that an undriven input will produce a response identical to the application of a logic 1, it is still advisable to tie these inputs to V_{DD} through a 1 k resistor. TDO should remain unconnected.

With the four Test Access Port pins disabled, the device can only be used in its default power-up state. At power up, the device is configured to count up starting at address 0, the reload pins ($\overline{RR}$ and $\overline{WR}$) will clear the counters, the Expand ID bits are set to 000, and the Output Enable pin ($\overline{G}$) is configured as an asynchronous input.

Table 4. RDCOUNT Scan Register Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	RAC0	Input
1	RAC1	Input
2	RAC2	Input
3	RAC3	Input
4	RAC4	Input
5	RAC5	Input
6	RAC6	Input
7	RAC7	Input
8	RAC8	Input
9	RAC9	Input
10	RAC10	Input
11	RAC11	Input
12	RAC12	Input
13	RAC13#	Input
14	RAC14#	Input
15	RAC15#	Input
16	WAC0	Input
17	WAC1	Input
18	WAC2	Input
19	WAC3	Input
20	WAC4	Input
21	WAC5	Input
22	WAC6	Input
23	WAC7	Input
24	WAC8	Input
25	WAC9	Input
26	WAC10	Input
27	WAC11	Input
28	WAC12	Input
29	WAC13#	Input
30	WAC14#	Input
31	WAC15#	Input

* RAC = Read Address Counter
WAC = Write Address Counter

\# These register bits are compared to the three Expand ID bits in the Control Register. (EX0 – 2). Only when there is a match is the read or write allowed to occur.

NOTE: Bit 0 closest to TDO.

Table 5. EZWRITE Scan Path Bit Definitions

Bit Number	Pin Name	Pin Type
0	D7	Input
1	D6	Input
2	D5	Input
3	D4	Input
4	D3	Input
5	D2	Input
6	D1	Input
7	D0	Input

Table 6. EZREAD and EZREADZ Scan Path Bit Definitions

Bit Number	Bit/Pin Name	Bit/Pin Type
0	Q0	Output
1	Q1	Output
2	Q2	Output
3	Q3	Output
4	Q4	Output
5	Q5	Output
6	Q6	Output
7	Q7	Output

Table 7. LDRREG Scan Path Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	RRR0	Register bit
1	RRR1	Register bit
2	RRR2	Register bit
3	RRR3	Register bit
4	RRR4	Register bit
5	RRR5	Register bit
6	RRR6	Register bit
7	RRR7	Register bit
8	RRR8	Register bit
9	RRR9	Register bit
10	RRR10	Register bit
11	RRR11	Register bit
12	RRR12	Register bit
13	RRR13	Register bit
14	RRR14	Register bit
15	RRR15	Register bit

* RRR = Read Reload Register

Table 8. LDBREG Scan Path Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	RRR0	Register bit
1	RRR1	Register bit
2	RRR2	Register bit
3	RRR3	Register bit
4	RRR4	Register bit
5	RRR5	Register bit
6	RRR6	Register bit
7	RRR7	Register bit
8	RRR8	Register bit
9	RRR9	Register bit
10	RRR10	Register bit
11	RRR11	Register bit
12	RRR12	Register bit
13	RRR13	Register bit
14	RRR14	Register bit
15	RRR15	Register bit
16	WRR0	Register bit
17	WRR1	Register bit
18	WRR2	Register bit
19	WRR3	Register bit
20	WRR4	Register bit
21	WRR5	Register bit
22	WRR6	Register bit
23	WRR7	Register bit
24	WRR8	Register bit
25	WRR9	Register bit
26	WRR10	Register bit
27	WRR11	Register bit
28	WRR12	Register bit
29	WRR13	Register bit
30	WRR14	Register bit
31	WRR15	Register bit

* RRR = Read Reload Register
WRR = Write Reload Register
NOTE: Bit 0 closest to TDO.

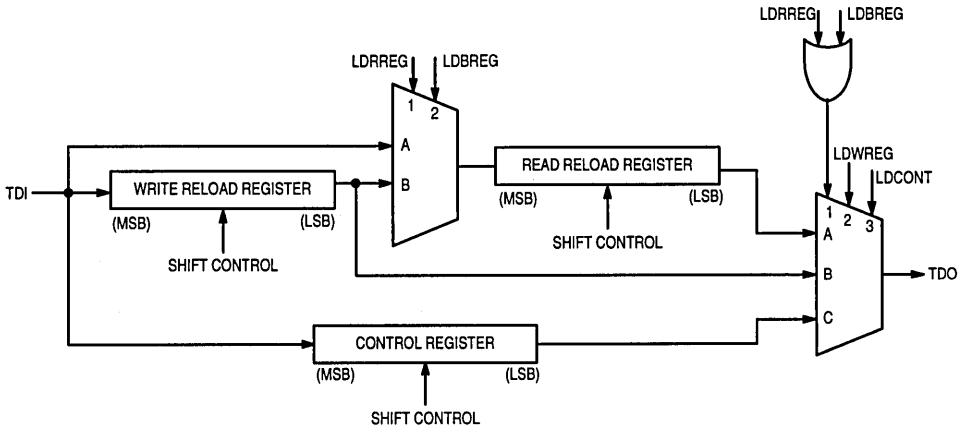
Table 9. LDWREG Scan Path Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	WRR0	Register bit
1	WRR1	Register bit
2	WRR2	Register bit
3	WRR3	Register bit
4	WRR4	Register bit
5	WRR5	Register bit
6	WRR6	Register bit
7	WRR7	Register bit
8	WRR8	Register bit
9	WRR9	Register bit
10	WRR10	Register bit
11	WRR11	Register bit
12	WRR12	Register bit
13	WRR13	Register bit
14	WRR14	Register bit
15	WRR15	Register bit

* WRR = Write Reload Register

Table 10. LDCONT Scan Path Bit Definitions

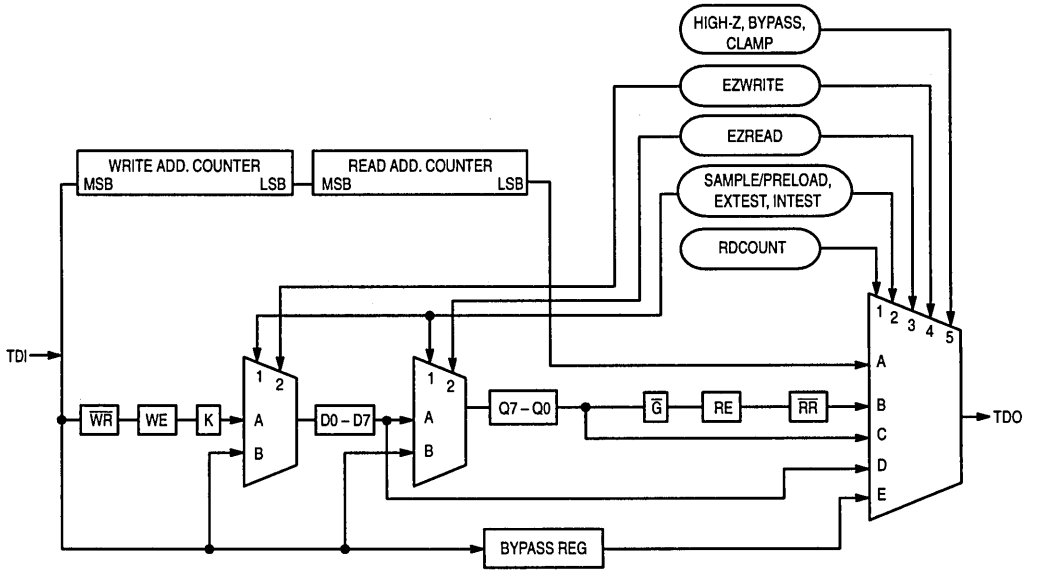
Bit Number	Bit/Pin Name	Bit/Pin Type
0	EX0	Register bit
1	EX1	Register bit
2	EX2	Register bit
3	WCC	Register bit
4	UDW	Register bit
5	RCC	Register bit
6	UDR	Register bit
7	G CONT	Register bit



THE LEFT MOST CONTROL SIGNAL ENTERING THE MUX FROM THE TOP(1) SELECTS THE UPPER MOST INPUT ON THE LEFT SIDE OF THE MUX(A). THE RIGHT MOST CONTROL SIGNAL SELECTS THE BOTTOM MOST INPUT.

Figure 3. Register Load Paths

4



THE LEFT MOST CONTROL SIGNAL ENTERING THE MUX FROM THE TOP(1) SELECTS THE UPPER MOST INPUT ON THE LEFTSIDE OF THE MUX(A). THE RIGHT MOST CONTROL SIGNAL SELECTS THE BOTTOM MOST INPUT.

Figure 4. Boundary Scan Paths

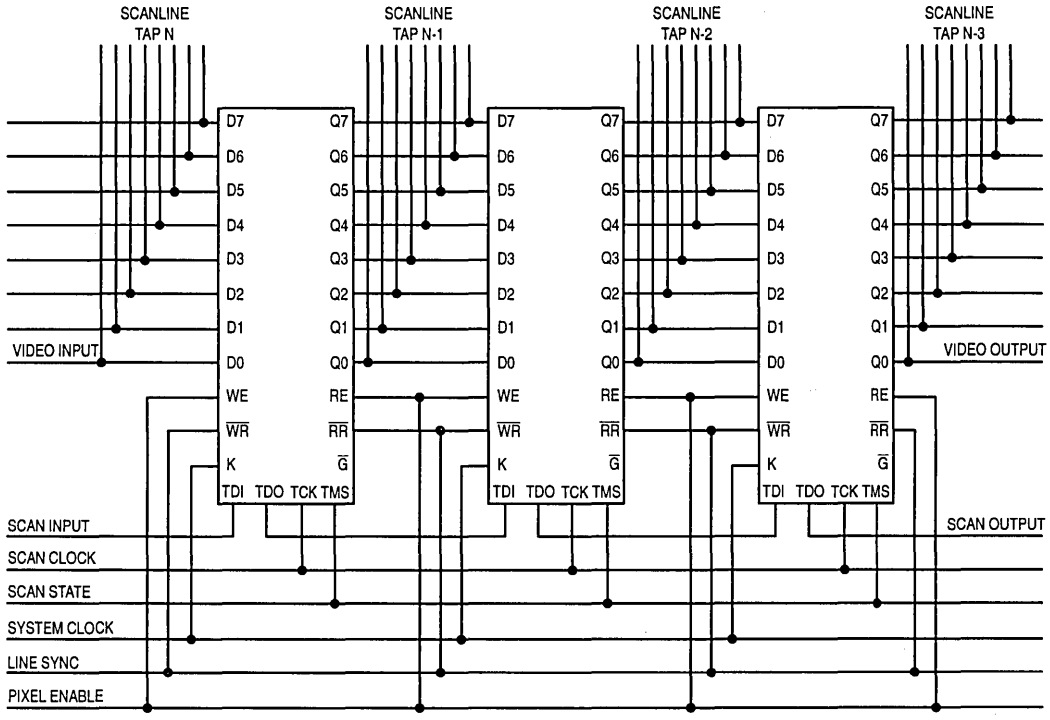


Figure 5. Multi-Stage 8-Bit Video Scanline Delay (8192 Pixels Maximum)

4

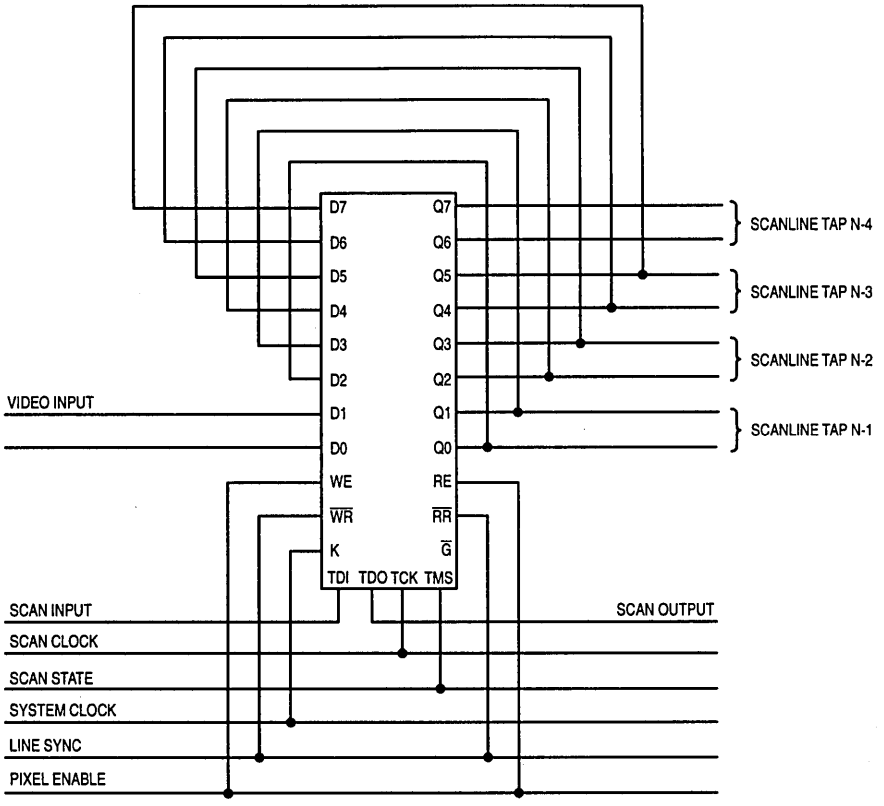


Figure 6. Multi-Stage 2-Bit Video Scanline Delay (8192 Pixels Maximum)

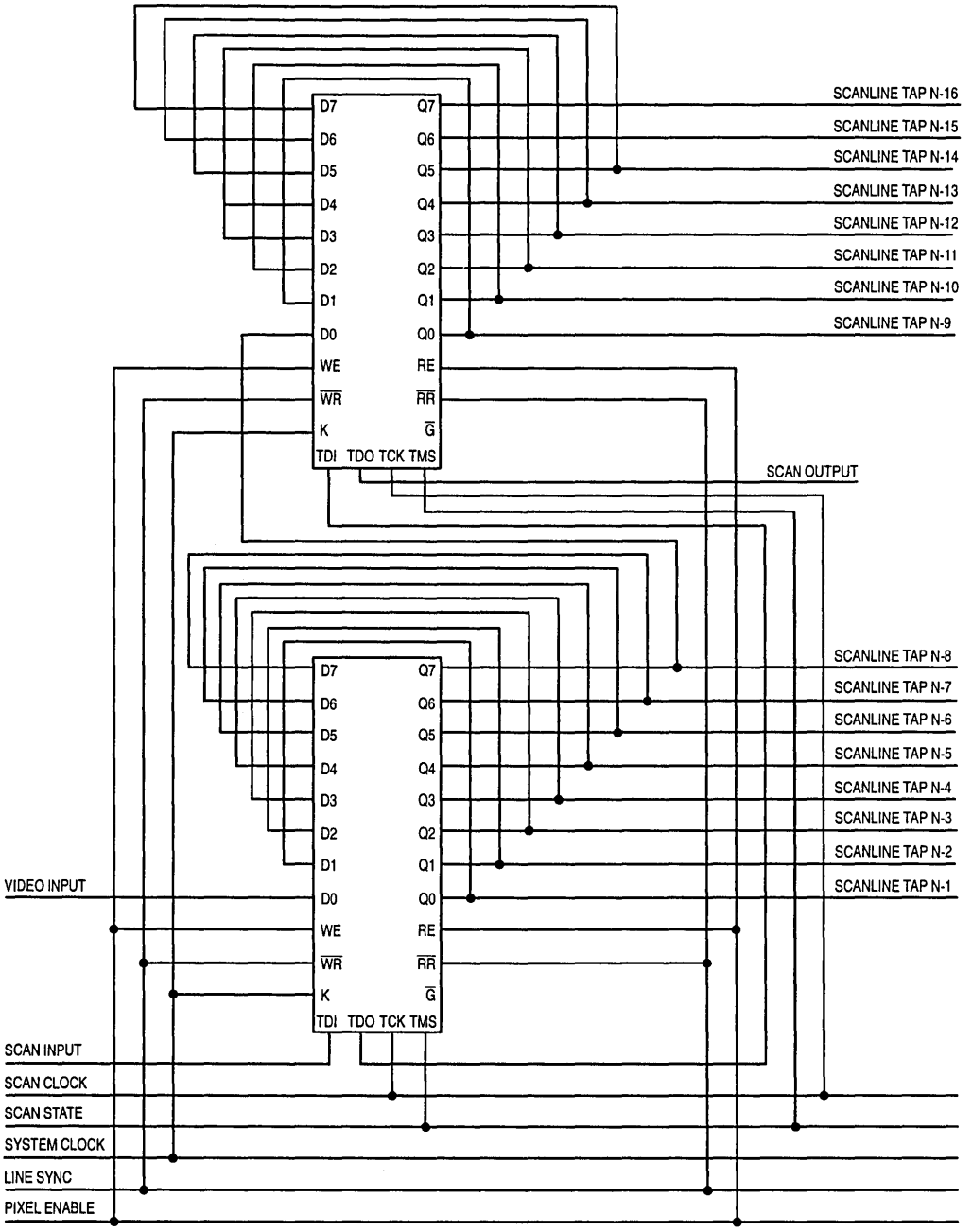


Figure 7. Multi-Stage 1-Bit Video Scanline Delay (8192 Pixels Maximum)

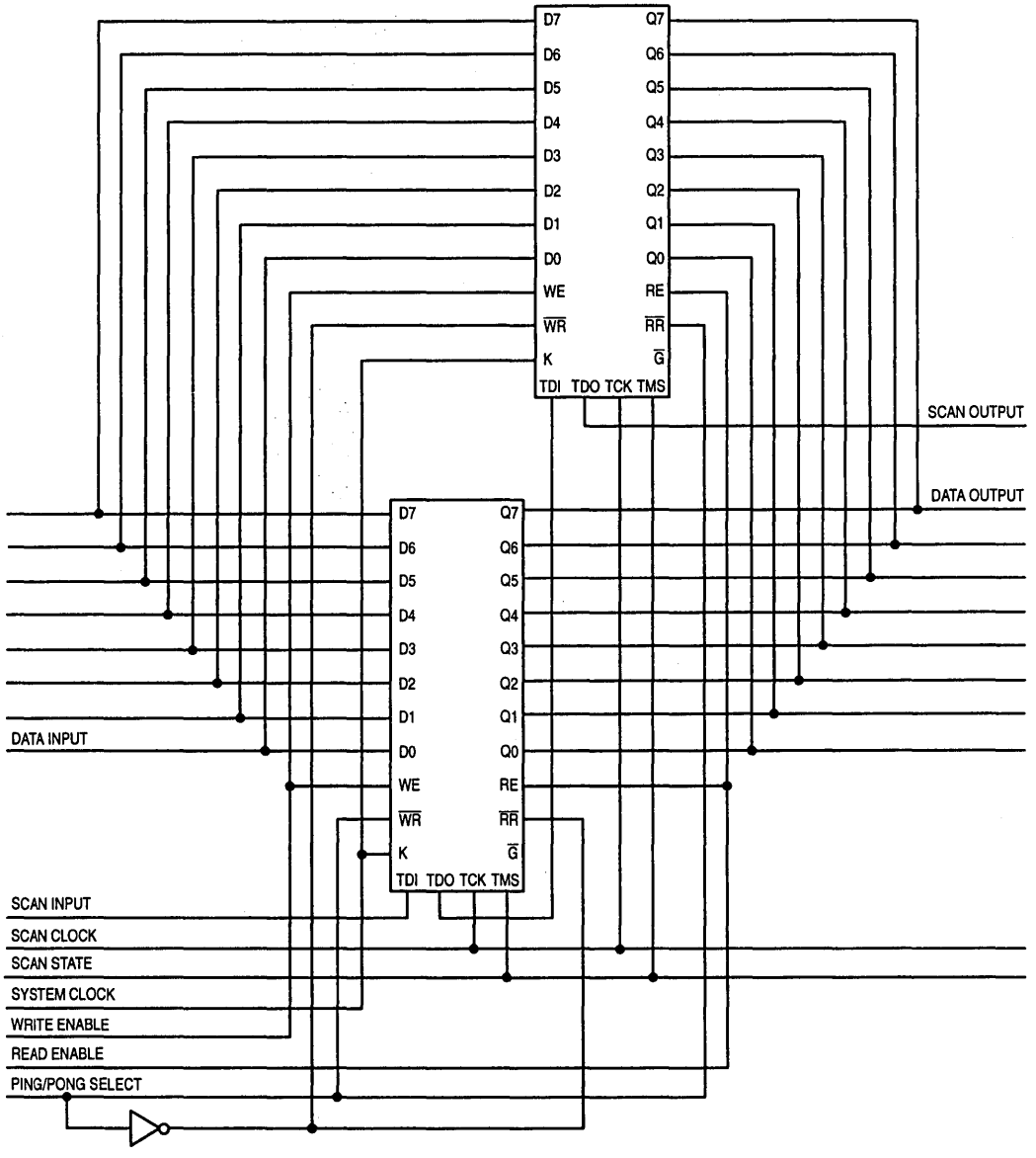


Figure 8. "Ping-Pong" Synchronizing Buffer (8192 Pixels Maximum)

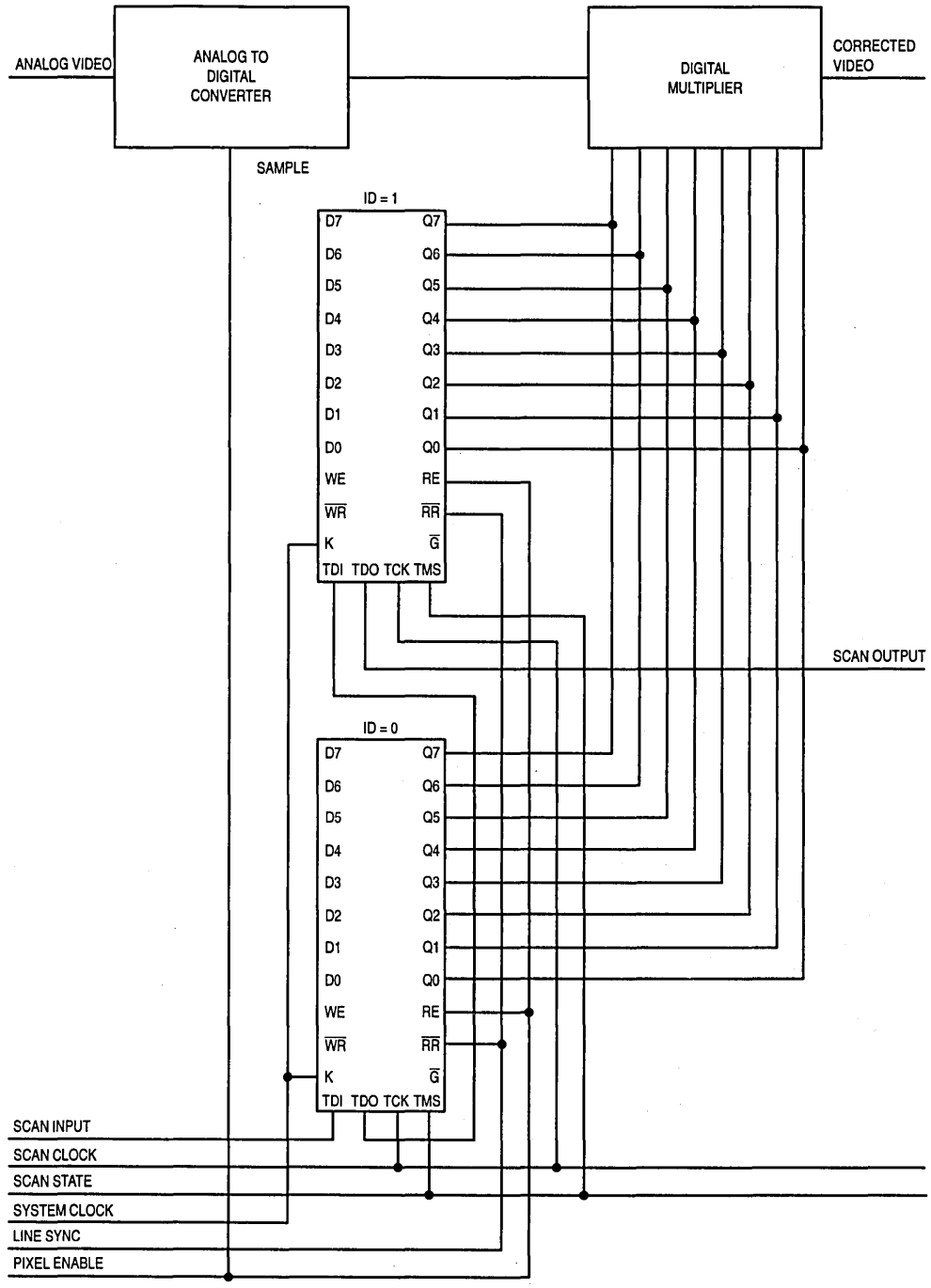


Figure 9. CCD Gain Correction, Buffer Written From Scan Input (16384 Pixels Maximum)

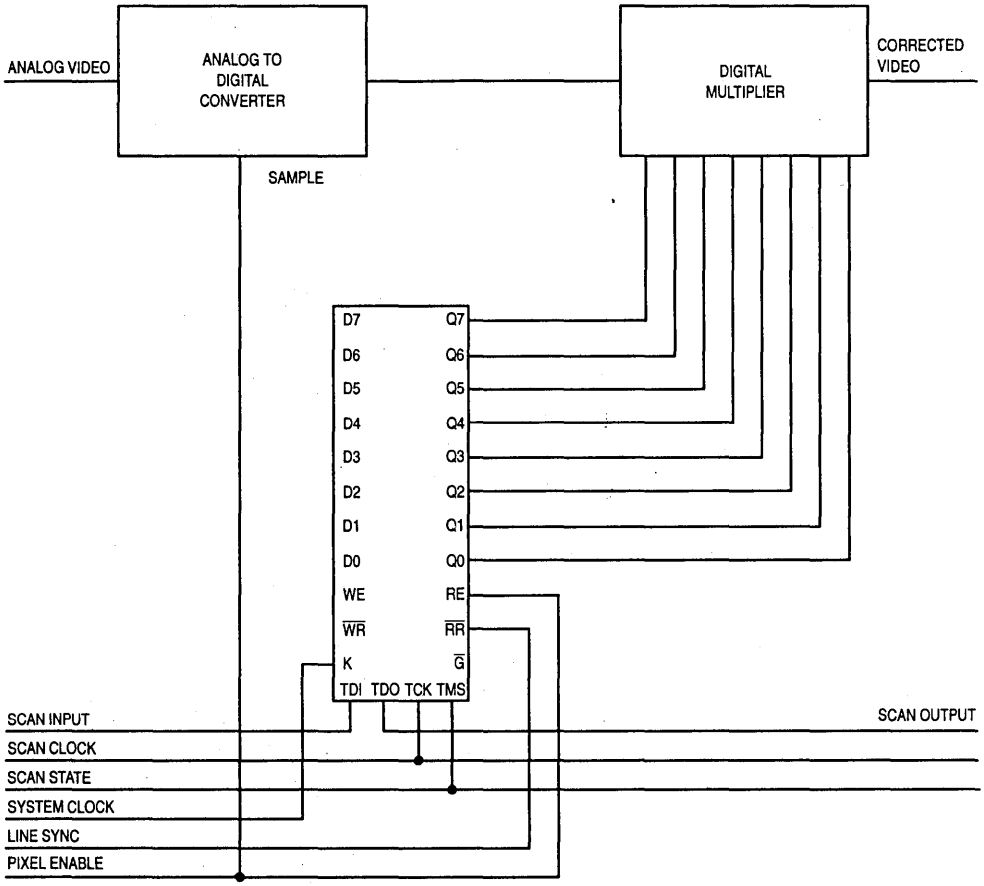


Figure 10. CCD Gain Correction, Buffer Written From Scan Input (8192 Pixels Maximum)

ORDERING INFORMATION
(Order by Full Part Number)

MCM 62X308 J XX

- MCM — Motorola Memory Prefix
- 62X308 — Part Number
- J — Package (J = SOJ)
- XX — Speed (15-5 = 15 ns, 17 = 17 ns)

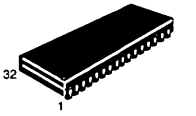
Full Part Numbers — MCM62X308J15-5 MCM62X308J17

MCM62Y308

Product Preview

Synchronous Line Buffer: 8K X 8 Bit Fast Static Dual Ported Memory

With IEEE Standard 1149.1 Test Access Port and Boundary-Scan (JTAG)



J PACKAGE
300 MIL SOJ
CASE 857

The MCM62Y308 is a synchronous, dual ported memory organized as 8,192 words of 8 bits each, fabricated using Motorola's double-metal, double-poly, 0.65 µm CMOS process. It is intended for high speed video or other applications which process data on a line-by-line basis. Through the use of a single clock and port control inputs, separate read and write data ports provide simultaneous access to a common memory array. Simultaneous read/write access to the same address location is also allowed, with old data being read followed by a write of the new data. This allows multiple devices to be cascaded with the output of one directly driving the input of another. In this configuration the data stream can be tapped at strategic interconnect points to perform various digital filtering functions.

Since there are no external address inputs, separate internal Read and Write Address Counters are provided as a means of indexing the memory array. These counters are preloaded and then selectively incremented or decremented by asserting Read Enable (RE) and Write Enable(WE) inputs, allowing cycle to cycle control. The address counters can be reloaded back to their initial values through the use of the Read Reload ($\overline{RR}$) and Write Reload ($\overline{WR}$) control inputs. These inputs initiate the transfer of Address Reload Register values into the Address Counters which index the memory array. When an address counter reaches 0000 (on down count) or FFFF (on up count), it will roll over on the next count. The roll over condition will cause the Roll-Over Flag (WRF or RRF) to assert high. The Roll-Over Flag outputs are cleared when their associated Roll-Over Reset pin is asserted low. The TDI input is used to write the Reload Registers using special Test Access Port instructions.

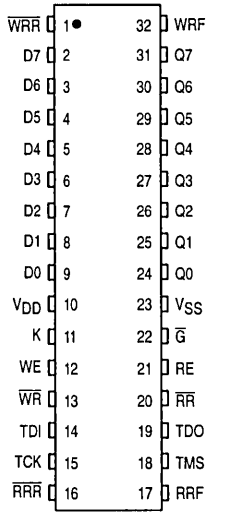
The Address Counters are 16 bits long, and only 13 of the 16 bits are required to index the 8K deep memory array. The remaining three bits are used for depth expansion. These three bits are compared to the lower three bits in the control register and as long as they are equal that port will remain active. If the bits do not compare the port will become inactive, however the counter will continue to count on the rising edge of K as long as the port enable signal (RE or WE) is asserted. The TDI input is used to write the Control Register using special Test Access Port instructions.

The Output Enable Input can be programmed to be either synchronous or asynchronous through the Control Register.

The MCM62Y308 is available in a 32 pin SOJ package.

- 8K x 8 Fast Access Static Memory Array
- Single 5 V Power Supply —MCM62Y308-15-5: ± 5%
  MCM62Y308-17: ± 10%
- Synchronous, Simultaneous Read/Write Memory Access
- 50 MHz Maximum Clock Cycle Time, < 15 ns Read Access
- Single Clock Operation
- Separate Read/Write Address Counters with Reload Control
- Separate Up/Down Counter Control for Both Read and Write
- Separate Roll-Over Flag Outputs for Read and Write
- Programmable Output Enable Control (Synchronous or Asynchronous)
- Cascadable I/O Interface
- IEEE Standard 1149.1 Test Port (JTAG)
- Expand ID Register for Depth Expansion
- High Board Density SOJ Package

PIN ASSIGNMENT

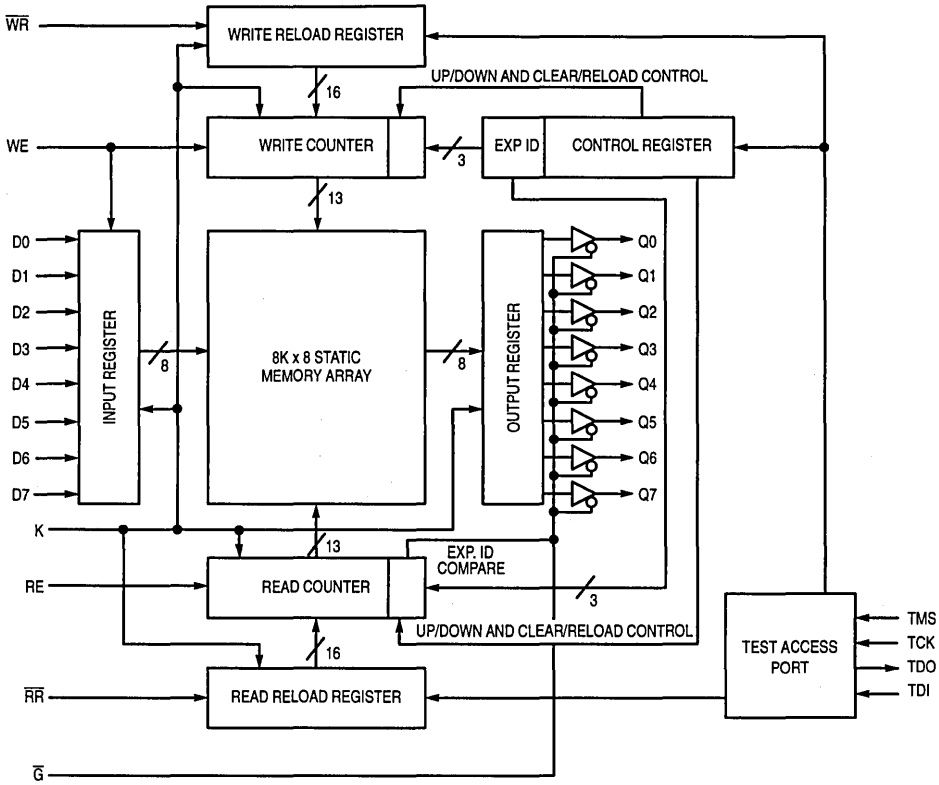


PIN NAMES

K	Clock Input
WE	Write Enable Input
$\overline{WR}$	Write Address Reload Input
RE	Read Enable Input
$\overline{RR}$	Read Address Reload Input
RRF	Read Roll-Over Flag Output
WRF	Write Roll-Over Flag Output
$\overline{RRR}$	Read Roll-Over Reset Input
$\overline{WRR}$	Write Roll-Over Reset Input
$\overline{G}$	Output Enable Input
D0 – D7	Data Inputs
Q0 – Q7	Data Outputs
TCK	Test Clock Input
TMS	Test Mode Select
TDI	Test Data Input
TDO	Test Data Output
V_{DD}	+ 5 V Power Supply
V_{SS}	Ground

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM



TRUTH TABLE (X = Don't Care)

WE	$\overline{WR}$	RE	$\overline{RR}$	$\overline{G}$	Match EXP ID (Read/Write)	Mode (Read/Write)	Supply Current	Q0 – 7 Status
X	L	X	L	L	Match Read/Match Write	Reload, Read/Reload, Write Disable	I_{CC}	Data Out
H	H	H	H	L	Match Read/Match Write	Count then Read/Write then Count	I_{CC}	Data Out
L	H	L	H	L	Match Read/Match Write	Read Count Disable/Write Disable	I_{CC}	Data Out
H	H	H	H	H	Match Read/Match Write	Count, Read/Count, Write	I_{CC}	High-Z
H	H	H	H	X	No Match Read/Match Write	Count, No Read/Count, No Write	I_{SB}	High-Z
H	H	L	H	X	No Match Read/Match Write	Count, No Read/Count, Write	I_{SB}	High-Z

MAXIMUM RATINGS* (Voltages Referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISITICS

(T_A = 0 to 70 °C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	MCM62Y308-15-5	V_{DD}	4.75	5.0	5.25	V
	MCM62Y308-17		4.50	5.0	5.50	
Input High Voltage		V_{IH}	2.2	—	V_{DD} + 0.3	V
Input Low Voltage		V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH}, V_{out} = 0 to V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, I_{out} = 0 mA, All Inputs ≥ V_{IL} = 0.0 V and V_{IH} ≥ 3.0, Cycle Time = 20 ns)	I_{CCA}	—	150	mA
AC Standby Current (When Expand ID Bits Do Not Match the Read Address Counter, Cycle Time = 20 ns)	I_{SB}	—	100	mA
Output Low Voltage (I_{OL} = + 4.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance (Q0 – Q7, TDO, WRF, RRF)	C_{out}	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Output Load ..... Terminated 50 Ohm Transmission Line

READ/WRITE CYCLE TIMING

Parameter		Symbol Std	Symbol Alt	MCM62Y308-15-5 Min	MCM62Y308-15-5 Max	MCM62Y308-17 Min	MCM62Y308-17 Max	Unit	Notes
Cycle Time		t_{KHKH}	t_{CYC}	20	—	22	—	ns	
Clock High Time		t_{KHKL}	t_{CKH}	8	—	9	—	ns	
Clock Low Time		t_{KLKH}	t_{CKL}	8	—	9	—	ns	
Clock High to Output Valid		t_{KHQV}	t_{CD}	5	15	5	17	ns	
Clock High to Roll-Over Flag Valid		t_{KHRFV}	—	5	11	5	11	ns	
Clock High to Output High-Z		t_{KHQZ}	t_{CZ}	5	15	5	15	ns	1
Output Enable Low to Output Valid		t_{GLQV}	t_{OLV}	3	10	3	10	ns	2, 4
Output Enable High to Output High-Z		t_{GHQZ}	t_{OHZ}	0	5	0	5	ns	2, 3, 4
Setup Times:	RE	t_{REVKH}	t_S	2	—	2	—	ns	5
	WE	t_{WEVKH}							
	$\overline{WR}$	t_{WRVKH}							
	$\overline{RRR}$	t_{RRRVKH}							
	$\overline{WRR}$	t_{WRRVKH}							
	$\overline{G}$	t_{GVKH}							6
	$\overline{RR}$	t_{RRVKH}		3	—	3	—		5
	Data In	t_{DVKH}		1	—	1	—		
Hold Times:	RE	t_{KHREX}	t_H	2	—	2	—	ns	5
	WE	t_{KHWEX}							
	$\overline{RR}$	t_{KHRRX}							
	$\overline{WR}$	t_{KHWRX}							
	$\overline{RRR}$	t_{KHRRRX}							
	$\overline{WRR}$	t_{KHWRRX}							
	$\overline{G}$	t_{KHGX}							6
	Data In	t_{KHDX}							

NOTES:
1. The outputs High-Z from a clock high edge when the upper three bits of the Read Address Counter do not match the 3 ID Expansion bits.
2. $\overline{G}$ is a don't care when the three ID expansion bits do not match the upper three bits of the Read Address Counter.
3. t_{GLQV} and t_{GHQZ} only apply when $\overline{G}$ is programmed as Asynchronous. (See TAP LDCONT instruction.)
4. Transition is measured ± 500 mV from steady-state voltage. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{GHQZ} max is less than t_{GLQV} min for a given device and from device to device.
5. This is a synchronous device. All inputs must meet the specified setup and hold times for ***ALL*** rising edges of Clock except for $\overline{G}$ when it is programmed to be asynchronous.
6. t_{GVKH} and t_{KHGX} only apply when $\overline{G}$ is programmed as synchronous.

AC TEST LOADS

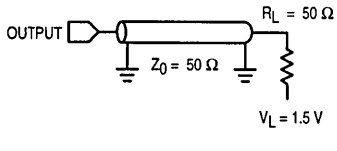


Figure 1A

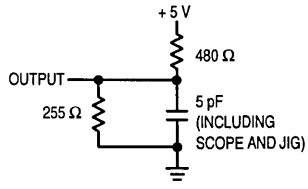
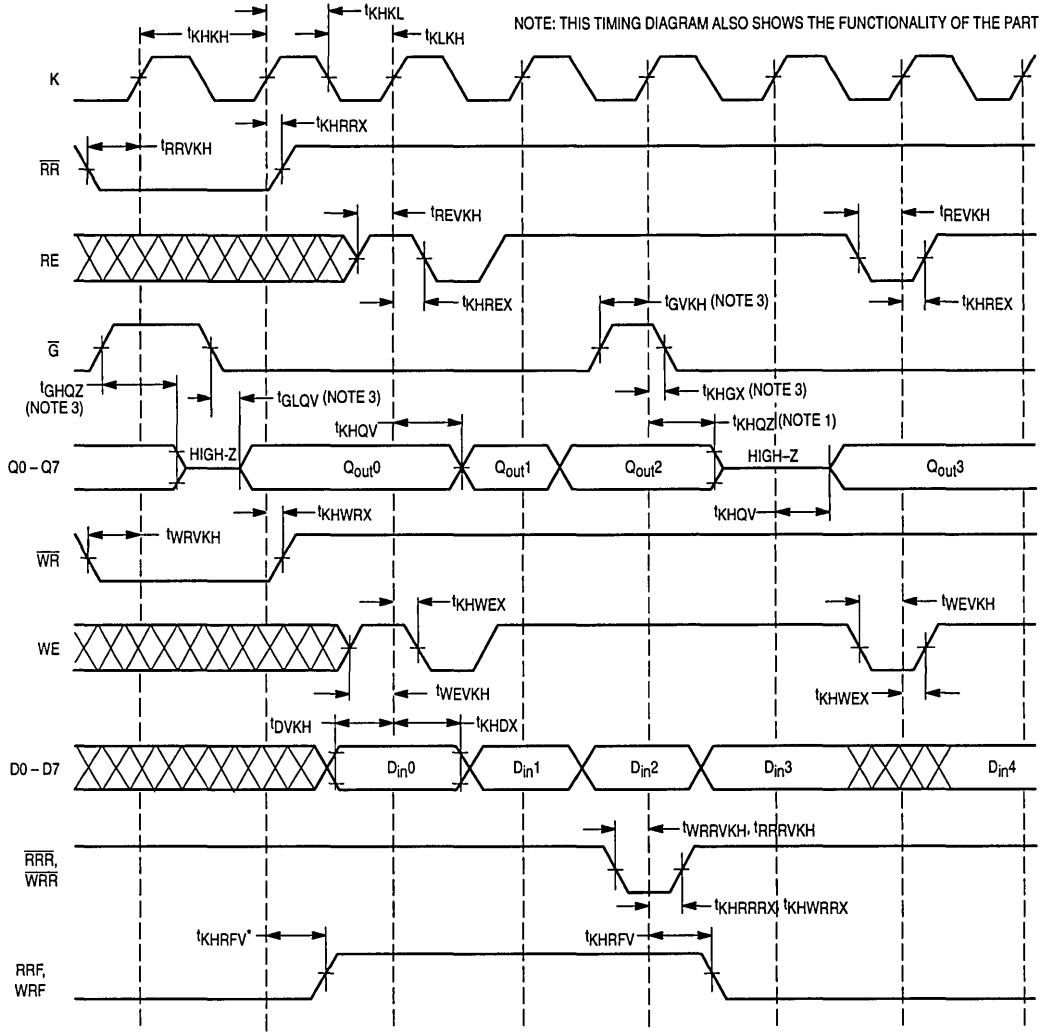


Figure 1B

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ/WRITE CYCLE TIMING DIAGRAM



*Roll-Over Outputs assert high when counters reach their initial value. This timing diagram shows the relationship between the roll-over output and reset pin only.

4

AC OPERATING CONDITIONS AND CHARACTERISTICS FOR THE TEST ACCESS PORT (IEEE 1149.1)

(T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Output Load ..... 50 Ohm Transmission Line

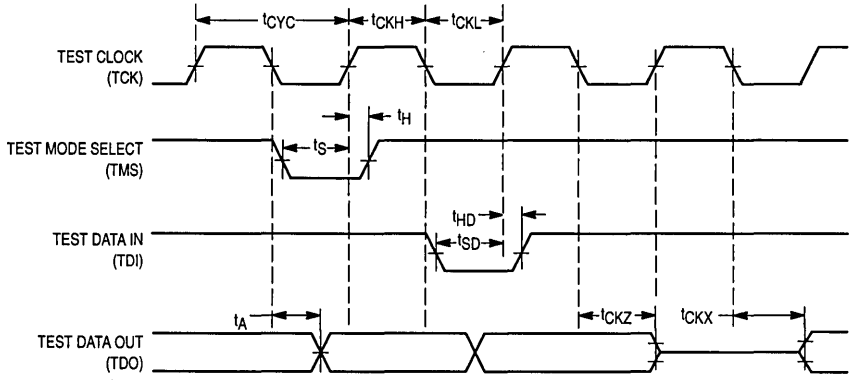
TAP CONTROLLER TIMING

Parameter	Symbol	MCM62Y308-15-5		MCM62Y308-17		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{CYC}	30	—	30	—	ns	
Clock High Time	t_{CKH}	12	—	12	—	ns	
Clock Low Time	t_{CKL}	12	—	12	—	ns	
Clock Low to Output Valid	t_A	5	9	5	9	ns	
Clock Low to Output High-Z	t_{CKZ}	0	9	0	9	ns	1
Clock Low to Output Active	t_{CKX}	0	9	0	9	ns	2, 3
Setup Time, Test Mode Select	t_S	2	—	2	—	ns	
Setup Time, Test Data In	t_{SD}	2	—	2	—	ns	
Hold Time, Test Mode Select	t_H	2	—	2	—	ns	
Hold Time, Test Data In	t_{HD}	2	—	2	—	ns	

4

NOTES:
1. Test Data Out will High-Z from a clock low edge depending on the current state of the TAP state machine.
2. Test Data Out is active only in the SHIFT-IR and SHIFT-DR state of the TAP state machine.
3. Transition is measured ± 500 mV from steady-state voltage. This parameter is sampled and not 100% tested.

TAP CONTROLLER TIMING DIAGRAM



PIN DESCRIPTIONS

K — CLOCK INPUT

System clock input pin accepting a minimum 8 ns clock high or clock low pulse at a minimum 20 ns clock cycle. All other synchronous inputs excluding the Test Access Port are captured on the rising edge of this signal.

WE — WRITE ENABLE INPUT

Write Enable is captured on K leading edge. When asserted this causes the input data D0 – D7 to be written into the RAM address controlled by the Write Address Counter and increments the counter for the next write.

RE — READ ENABLE INPUT

Read Enable is captured on K leading edge. When asserted this causes a RAM read access from address controlled by the Read Address Counter to be inserted in the output register Q0 – Q7 and increments the counter for the next read operation.

$\overline{WR}$ — WRITE RELOAD INPUT

Write Reload is captured on K leading edge. When asserted this causes the Write Address Counter to be initialized to the contents of the Write Reload Register or "cleared" as specifiedby Control Register bit 3. See Control Register Bit 4 for "cleared" description.

$\overline{RR}$ — READ RELOAD INPUT

Read Reload is captured on K leading edge. When asserted this causes the Read Address Counter to be initialized to the contents of the Read Reload Register or "cleared" as specified by Control Register bit 5. See Control Register Bit 6 for "cleared" description.

$\overline{G}$ — OUTPUT ENABLE INPUT

When asserted low causes the outputs Q0 – Q7 to become active and when deasserted high causes them to High-Z. This pin can be either synchronous with K leading edge or asynchronous as specified by Control Register bit 7.

D0 – D7 — DATA INPUTS

The levels on these pins is captured on the K leading edge. The value captured will be written into the RAM if WE is also asserted and the Expand ID bits match the upper three bits of the Write Address Counter.

Q0 – Q7 — DATA OUTPUTS

Data outputs are available from the Read Output Register < 15 ns from the rising edge of K when RE or $\overline{RR}$ is asserted. Outputs are disabled when the upper three bits of the Read Address Counter do not match the three Expand ID bits of the Control Register. $\overline{G}$ will also control the disabling of the outputs either synchronously or asynchronously. See $\overline{G}$ description.

RRF, WRF — ROLL-OVER FLAG OUTPUTS

These signals are asserted high on the clock cycle where the Address Counters (Write Address Counter for WRF and Read Address Counter for RRF) roll-over to 0000 (or FFFF when counting down). They will remain asserted until cleared with the Roll-Over Reset Inputs ($\overline{RRR}$ and $\overline{WRR}$).

$\overline{RRR}$, $\overline{WRR}$ — ROLL-OVER RESET INPUTS

The level on these pins is captured on the K leading edge. When asserted low, each will reset their associated Roll-Over Flag output.

TEST ACCESS PORT PIN DESCRIPTIONS

The Test Access Port conforms with the IEEE Standard 1149.1. It is also used to load device specific registers used to configure the MCM62Y308.

TCK — TEST CLOCK INPUT

Samples and clocks all TAP events. All inputs are captured on TCK rising edge and all outputs propagate from TCK falling edge. It also can take the place of K in device operation in certain test conditions.

TMS — TEST MODE SELECT INPUT

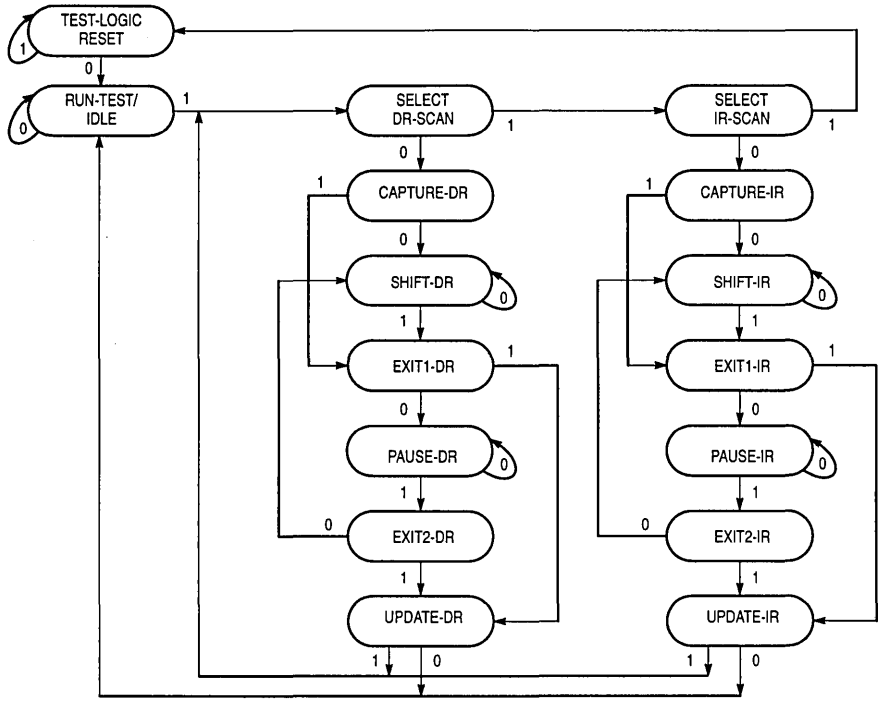
Sampled on the rising edge of TCK. Determines the movement through the TAP state machine (Figure 2). This circuit is designed in such a way that an undriven input will produce a response identical to the application of a logic 1.

TDI — TEST DATA IN INPUT

Sampled on the rising edge of TCK. This is the input side of the serial register placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP state machine and what instruction is active in the TAP instruction register. This circuit is designed in such a way that an undriven input will produce a response identical to the application of a logic 1.

TDO — TEST DATA OUT OUTPUT

Output that is active depending on the state of the TAP state machine. Output changes off the trailing edge of TCK. This is the output side of the serial register placed between TDI and TDO.



NOTE: The value adjacent to each state transition represents the signal present at TMS at the rising edge of TCK.

Figure 2. TAP Controller State Diagram

TEST ACCESS PORT DESCRIPTIONS

INSTRUCTION SET

A four pin IEEE Standard 1149.1 Test Port (JTAG) is included on this device. There are two classes of instructions; standard instructions as defined in the IEEE 1149.1 standard and device specific, or public, instructions that are used to control the functionality of the device. When the TAP (Test Access Port) controller is in the Shift-IR state the Instruction Register is placed between TDI and TDO, least significant bit closest to TDO. In this state the desired instruction would be serially loaded through the TDI input (while the previous instruction would be shifted out of TDO). The TAP instruction set for this device is listed in Table 1.

TAP STANDARD INSTRUCTION SET

NOTE: The descriptions in this section are not intended to be used without the supporting IEEE 1149.1-1993 Standard.

SAMPLE/PRELOAD TAP INSTRUCTION

The SAMPLE/PRELOAD TAP instuction is used to allow scanning of the boudary-scan register without causing interference to the normal operation of the chip logic. The 26 bit boundary scan register contains bits for all device signal and clock pins and associated control signals (Table 2). This register is accessible when the SAMPLE/PRELOAD TAP instruction is loaded into the TAP instruction register. When the TAP controller is then moved to the Shift-DR state, the boundary scan register is placed between TDI and TDO. This scan register can then be used prior to the EXTEST instruction to preload the output pins with desired values so that these pins will drive the desired state when the EXTEST instruction is loaded. It would be used prior to the INTEST instruction to preload values into the input pins. As data is written into TDI, data also streams out of TDO which can be used to pre-sample the inputs and outputs. SAMPLE/PRELOAD would also be used prior to the CLAMP instruction to preload the values on the output pins that will be driven out when the CLAMP instruction is loaded.

Table 2 shows the boundary-scan bit definitions. The first column defines the bit's ordinal position in the boundary-scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 0; the last bit to be shifted is 25. The second column is the pin name and the third column is the pin type.

EXTEST TAP INSTRUCTION

The EXTEST instruction is intended to be used in conjunction with the SAMPLE/PRELOAD instruction to assist in testing board level connectivity. Normally, the SAMPLE/PRELOAD instruction would be used to preload all output pins (i.e., Q0 – Q7, RRF, and WRF). The EXTEST instruction would then be loaded. During EXTEST the boundary-scan register is placed between TDI and TDO in the Shift-DR state of the TAP controller. Once the EXTEST instruction is loaded, the TAP controller would then be moved to the Run-Test/Idle state. In this state one cycle of TCK would cause the preloaded data on the ouput pins to be driven while the values on the input pins would be sampled (Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero). Note that TCK, not the Clock pin, K, is used as the clock input while K is only sampled during EXTEST. After one clock cycle of TCK, the TAP controller would then be moved to the Shift-DR state where the sampled values would be shifted out of TDO (and new values would be shifted in TDI). These values would normally be compared to expected values to test for board connectivity.

THE INTEST TAP INSTRUCTION

The INTEST instruction is intended to be used to assist in testing internal device functionality. When the INTEST instruction is loaded the boundary-scan register is placed between TDI and TDO in the Shift-DR state of the TAP controller (Table 2). While in the Shift-DR state, all input pins would be preloaded via the boundary scan register to set up the desired mode (i.e., read, write, reload, etc.). The TAP controller would then be moved to the Run-Test/Idle state. In this state one or more cycles of TCK would cause the preloaded data in the boundary-scan register to be driven while the values of Q0 – Q7 would be sampled (Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero, however the values of Q0 – Q7 will

Table 1. TAP Instruction Set

Instruction	Code (Binary)	Description
Standard Instructions:		
BYPASS	1111*	Bypass Instruction
INTEST	0111	Intest Instruction
SAMPLE/PRELOAD	1100	Sample and/or Preload Instruction
EXTEST	0000	Extest Instruction
HIGHZ	1010	High-Z all Output pins while bypass reg. is between TDI and TDO
CLAMP	1001	Clamp Output pins while bypass reg. is between TDI and TDO
Device Specific (Public) Instructions:		
LDRREG	0001	Load Read Address Reload Register
LDWREG	0100	Load Write Address Reload Register
LDBREG	0101	Load both Address Reload Registers (Write then Read)
LDCONT	0010	Load Control Register
RDCOUNT	1000	Read the values of the Read and Write Address Counters
EZWRITE	0011	Serial Write (using Write Address Counter)
EZREAD	0110	Serial Read (using Read Address Counter)
EZREADZ	1110	Serial Read, outputs High-Z

*Default state at power-up.

be sampled regardless of $\overline{G}$). Only one action will be performed in the Run-Test/Idle state no matter how many clock cycles are input. Note that TCK, not the Clock pin(K), is used as the clock input while K is ignored during INTEST. After one or more clock cycles of TCK, the TAP controller would then be moved to the Shift-DR state where the sampled values would be shifted out of TDO (and new values would be shifted in TDI). These values would normally be compared to expected values to test for device functionality.

THE INTEST TAP INSTRUCTION

The INTEST instruction is intended to be used to assist in testing internal device functionality. When the INTEST instruction is loaded the boundary-scan register is placed between TDI and TDO in the Shift-DR state of the TAP controller (Table 2). While in the Shift-DR state, all input pins would be preloaded via the boundary scan register to set up the desired mode (i.e., read, write, reload, etc.). The TAP controller would then be moved to the Run-Test/Idle state. In this state one or more cycles of TCK would cause the preloaded data in the boundary-scan register to be driven while the values of Q0 – Q7 would be sampled (Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero, however the values of Q0 – Q7 will be sampled regardless of $\overline{G}$). Only one action will be performed in the Run-Test/Idle state no matter how many clock cycles are input. Note that TCK, not the Clock pin(K), is used as the clock input while K is ignored during INTEST. After one or more clock cycles of TCK, the TAP controller would then be moved to the Shift-DR state where the sampled values would be shifted out of TDO (and new values would be shifted in TDI). These values would normally be compared to expected values to test for device functionality.

Since device functionality can only be verified through sampling the outputs of the device, the most likely use of INTEST would be to first load up the boundary-scan register for a Write Reload and execute the reload in the Run-Test/Idle state. Then a write of the first address would be performed again using the boundary scan register to load up the input registers and executing the write in the Run-Test/Idle state. Lastly, a Read Reload would be executed in the same manner so that the data that had just been written in the first address would be read from the memory array and written into the output registers which would then be shifted out of TDO in the Shift-DR state. The values of the roll-over flags (RRF and WRF) would also be sampled and shifted out at the same time for comparison to expected values.

There are easier ways to serially read and write the memory array. See the EZREAD and EZWRITE TAP instruction explanation.

CLAMP TAP INSTRUCTION

The CLAMP instruction is provided to allow the state of the signals driven from the output pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the output pins will not change while the CLAMP instruction is selected. EXTEST could also be used for this purpose but CLAMP shortens the board scan path by inserting only the bypass register between TDI and TDO. To use CLAMP, the SAMPLE/PRELOAD instruction would be used first to scan in the values to be driven on the output pins when the CLAMP instruction is active. Q0 – Q7 will be active only if $\overline{G}$ is preloaded with a zero.

HIGH-Z TAP INSTRUCTION

The High-Z instruction is provided to allow all the outputs (except TDO) to be placed in an inactive drive state (High-Z), including the Read Roll-Over Flag and the Write Roll-Over Flag outputs. During the High-Z instruction the bypass register is connected between TDI and TDO.

BYPASS TAP INSTRUCTION

The Bypass instruction is the default instruction loaded in at power up. This instruction will place a single shift register between TDI and TDO during the Shift-DR state of the TAP controller. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

Table 2. Boundary Scan Register Bit Definitions

Bit Number	Pin Name	Pin Type
0	RRF	Output
1	$\overline{RR}$	Input
2	RE	Input
3	$\overline{G}$	Input
4	Q0	Output
5	Q1	Output
6	Q2	Output
7	Q3	Output
8	Q4	Output
9	Q5	Output
10	Q6	Output
11	Q7	Output
12	WRF	Output
13	$\overline{WRR}$	Input
14	D7	Input
15	D6	Input
16	D5	Input
17	D4	Input
18	D3	Input
19	D2	Input
20	D1	Input
21	D0	Input
22	K	Input
23	WE	Input
24	$\overline{WR}$	Input
25	$\overline{RRR}$	Input

NOTE: K is a sample-only scan bit. It cannot be preloaded for control purposes.

DEVICE SPECIFIC (PUBLIC) INSTRUCTIONS

LDCONT TAP INSTRUCTION

The Control Register is an eight bit register that contains the control bits for the Address Registers and Counters and the Output Enable pin. When the LDCONT TAP instruction is loaded into the Instruction Register, the Control Register is placed between TDI and TDO when the TAP controller is in the Shift-DR state (see Figure 2 and Table 10). The power-up/preload state and function of the Control bits are found in Table 3.

The Expand ID bits provide system depth expansion. These three bits are compared to the upper three bits in the address counters. As long as the three Expand-ID bits match the three upper bits in the address counters the port will stay active. If they do not match, the port will deactivate (i.e., outputs will High-Z or write will be disabled); however, the counters will continue counting as long as RE and WE remain asserted (i.e., high) at the rising edge of Clock.

The Reload Control bits (3 and 5) are used to control either reloading the Read and Write Address Counters from the Reload Registers or clearing the counter when $\overline{RR}$ or $\overline{WR}$ is asserted. If these bits are set low the counters they control will be cleared to all zeroes if the appropriate reload signal ($\overline{RR}$ or $\overline{WR}$) is asserted and any value in the Reload Register is ignored. This means that if the initial address value desired is address 0000 (or FFFF when counting down) then there is no need to load the Address Reload Registers using the LDRREG, LDWREG, or the LDBREG instructions in the following description. If these bits are set high the counters are loaded up with the values in the Reload Registers when the appropriate reload signal ($\overline{RR}$ or $\overline{WR}$) is asserted.

The Up/Down count bits (4 and 6) determine the direction in which the respective Address Counter will count; if the bit is set low the counter will count up and if set high the counter will count down. If the counters are set to count down and the Reload control is set to the clear counter mode, then the initial value in the counters will be FFFF. To ensure that the counter will function properly, a reload (using $\overline{RR}$ or $\overline{WR}$) is required after the count direction is switched.

The Output Enable control bit (7) determines the functionality of the Output Enable pin, $\overline{G}$. When the bit is low, $\overline{G}$ functions asynchronously. When set high, $\overline{G}$ functions synchronously and must meet the specified setup and hold times to the Clock K.

The Control Register will also be preloaded. When the instruction 0010 (LDCONT) is in the Instruction Register and the controller is in the Capture-DR state the above preload values (all zeroes) will be loaded into the Control Register. All zeroes will also be loaded in the Control Register at power-up.

While new values are shifted in from TDI in the Shift-DR state, all zeroes will be output on TDO for the first eight bits.

LDRREG, LDWREG, AND LDBREG TAP INSTRUCTIONS

There are three instructions that may be used to load the 16 bit address reload registers: LDRREG (Load Read Address Reload Register), LDWREG (Load Write Address Reload Register), and LDBREG (Load both Address Reload Registers, Write followed by Read). Figure 2 illustrates how the Reload registers are placed between TDI and TDO. Tables 7, 8, and 9 describe each register. These instructions would be used only if the user needed to load the Reload Registers with a non-zero value. If the Address Counters are to always be reset to zeroes (or all 1s if counting down) then only the Control Register need be loaded to affect a reset of the counters.

The TAP controller has been set up to make it easier for the user to serially load the Reload Registers. When the TAP controller is clocked into the Capture-IR state (see state diagram) the instruction for loading both registers (0101) will be preloaded into the shift register. This allows the user to go directly to the Update-IR instead of having to serially shift this instruction in through the TDI port. Once the load instruction has been entered the user can then clock over to the Capture-DR state where the value for the reload register(s) is serially loaded (see Figure 2).

RDCOUNT TAP INSTRUCTION

The RDCOUNT scan register is accessible after the RDCOUNT instruction is loaded into the TAP instruction register in the Shift-IR state and the TAP controller is then moved to the Shift-DR state. This scan register can then be used to shift out the values of the Read and Write Address Counters The RDCOUNT scan-register is a sample only register and can not be used to load values into the counters. See Table 4.

EZWRITE TAP INSTRUCTION AND SCAN PATH

The EZWRITE TAP instruction is provided to allow the user to more easily and quickly write a large number of bytes to the device serially through the TDI port. EZWRITE shortens the scan path for a serial write to just the 8 bit Data in register (see Table 5).

The most likely use of this instruction is as follows: the user would first load the Control Register using the LDCONT instruction. This would initialize the Expand ID bits and the Write Counter. The Write Reload Register will need to be

Table 3. Control Register Bit Description

Bit No.	Power Up and Preload State	Function
0 – 2	000	Expand ID bits for comparison with the upper 3 bits of the Read and Write Address counters
3	0	Reload Control of Write Address Counter (0 = clear counter, 1 = reload)
4	0	Up/Down count bit for Write Address Counter (0 = count up, 1 = count down)
5	0	Reload Control of Read Address Counter (0 = clear counter, 1 = reload)
6	0	Up/Down count bit for Read Address Counter (0 = count up, 1 = count down)
7	0	$\overline{G}$ Control (0 = asynchronous, 1 = synchronous)

loaded using the LDWREG instruction if a non-zero starting address is desired. If 0000 was the first desired count, setting up the Control Register to "clear" the Write counter is all that is required (Bit 3 set to zero). A reload cycle using SAMPLE/PRELOAD ($\overline{WR}$ preloaded low) and INTEST would also have to be run in order to initialize the counter. While still in the INTEST instruction at the Shift-DR state, the proper values of WE and $\overline{WR}$ would then need to be preloaded for proper operation of EZWRITE (WE high and $\overline{WR}$ high). After all this initializing is done, the EZWRITE instruction would be loaded into the TAP instruction register in the Shift-IR state. When the TAP controller is then moved to the Shift-DR state the EZWRITE scan path would be inserted between TDI and TDO. This scan path is composed of the 8 bit Data In register (see Table 5). The 8 bits to be written into the first address would be scanned in (sampled values from the Data In pins would be streaming out of TDO at the same time), then the TAP controller would be moved to the Run-Test/Idle state where one cycle of TCK would write the 8 bits into the address and increment the counter. The TAP controller would then move back to the Shift-DR state so that the next byte to be written can be serially loaded and the process would be repeated until all desired bytes were written. During EZWRITE the Q0 – Q7 pins will be in a High-Z state.

EZREAD TAP INSTRUCTION AND SCAN PATH

The EZREAD TAP instruction is provided to allow the user to more easily and quickly read a large number of bytes from the device serially through the TDO port. EZREAD shortens the scan path for a serial read to just the 8 bit Data Out register (see Table 6).

To serially read the device the following would occur: initialization would be much like EZWRITE except that the Read Address Counter should be reladed with the count BEFORE the first one desired. So, if the first read needed to be address 0000 (and the counter is counting up), the Read Reload Register would have to be preloaded with FFFF using the LDRREG instruction. Again, SAMPLE/PRELOAD and INTEST instructions would need to be run to perform a reload cycle followed by another Boundary-scan that set RE and $\overline{RR}$ high in anticipation of the EZREAD instruction. Also, WE should be set low to prevent any unintended writes while reading. After this initializing, the EZREAD instruction would be loaded into the TAP instruction register in the Shift-IR state. The TAP controller would move to the Run-Test/Idle state where one cycle of TCK would increment the counter, read the 8 bits from that address, and load them into the Data Output register. The TAP controller would then move to the Shift-DR state and the EZREAD scan path would be inserted between TDI and TDO. This scan path is composed of the 8 bit Data Out register (see Table 6). In the Shift-DR state the Data Out register would be serially scanned out of the TDO port. This sequence through the TAP state machine would then be repeated until all desired bytes were read. EZREAD keeps the Q0 – Q7 pins active (if $\overline{G}$ is preloaded low) to allow parallel reading of the data out if desired.

EZREADZ TAP INSTRUCTION AND SCAN PATH

The EZREADZ TAP instruction behaves exactly like the EZREAD instruction except that the all outputs are held in a High-Z mode once the instruction is loaded.

DISABLING THE TEST ACCESS PORT AND BOUNDARY SCAN

It is possible to use this device without utilizing the four pins used for the IEEE 1149.1 Test Access Port. To circuit disable the TAP controller without interfering with normal operation of the device TCK must be tied to V_{SS} to preclude midlevel inputs. Although TDI and TMS is designed in such a way that an undriven input will produce a response identical to the application of a logic 1, it is still advisable to tie these inputs to V_{DD} through a 1 k resistor. TDO should remain unconnected.

With the four Test Access Port pins disabled, the device can only be used in its default power-up state. At power up, the device is configured to count up starting at address 0, the reload pins ($\overline{RR}$ and $\overline{WR}$) will clear the counters, the Expand ID bits are set to 000, and the Output Enable pin ($\overline{G}$) is configured as an asynchronous input.

Table 4. RDCOUNT Scan Register Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	RAC0	Input
1	RAC1	Input
2	RAC2	Input
3	RAC3	Input
4	RAC4	Input
5	RAC5	Input
6	RAC6	Input
7	RAC7	Input
8	RAC8	Input
9	RAC9	Input
10	RAC10	Input
11	RAC11	Input
12	RAC12	Input
13	RAC13#	Input
14	RAC14#	Input
15	RAC15#	Input
16	WAC0	Input
17	WAC1	Input
18	WAC2	Input
19	WAC3	Input
20	WAC4	Input
21	WAC5	Input
22	WAC6	Input
23	WAC7	Input
24	WAC8	Input
25	WAC9	Input
26	WAC10	Input
27	WAC11	Input
28	WAC12	Input
29	WAC13#	Input
30	WAC14#	Input
31	WAC15#	Input

* RAC = Read Address Counter
WAC = Write Address Counter
\# These register bits are compared to the three Expand ID bits in the Control Register. (EX0 – 2). Only when there is a match is the read or write allowed to occur.
NOTE: Bit 0 closest to TDO.

Table 5. EZWRITE Scan Path Bit Definitions

Bit Number	Pin Name	Pin Type
0	D7	Input
1	D6	Input
2	D5	Input
3	D4	Input
4	D3	Input
5	D2	Input
6	D1	Input
7	D0	Input

Table 6. EZREAD and EZREADZ Scan Path Bit Definitions

Bit Number	Bit/Pin Name	Bit/Pin Type
0	Q0	Output
1	Q1	Output
2	Q2	Output
3	Q3	Output
4	Q4	Output
5	Q5	Output
6	Q6	Output
7	Q7	Output

Table 7. LDRREG Scan Path Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	RRR0	Register bit
1	RRR1	Register bit
2	RRR2	Register bit
3	RRR3	Register bit
4	RRR4	Register bit
5	RRR5	Register bit
6	RRR6	Register bit
7	RRR7	Register bit
8	RRR8	Register bit
9	RRR9	Register bit
10	RRR10	Register bit
11	RRR11	Register bit
12	RRR12	Register bit
13	RRR13	Register bit
14	RRR14	Register bit
15	RRR15	Register bit

* RRR = Read Reload Register

Table 8. LDBREG Scan Path Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	RRR0	Register bit
1	RRR1	Register bit
2	RRR2	Register bit
3	RRR3	Register bit
4	RRR4	Register bit
5	RRR5	Register bit
6	RRR6	Register bit
7	RRR7	Register bit
8	RRR8	Register bit
9	RRR9	Register bit
10	RRR10	Register bit
11	RRR11	Register bit
12	RRR12	Register bit
13	RRR13	Register bit
14	RRR14	Register bit
15	RRR15	Register bit
16	WRR0	Register bit
17	WRR1	Register bit
18	WRR2	Register bit
19	WRR3	Register bit
20	WRR4	Register bit
21	WRR5	Register bit
22	WRR6	Register bit
23	WRR7	Register bit
24	WRR8	Register bit
25	WRR9	Register bit
26	WRR10	Register bit
27	WRR11	Register bit
28	WRR12	Register bit
29	WRR13	Register bit
30	WRR14	Register bit
31	WRR15	Register bit

* RRR = Read Reload Register
WRR = Write Reload Register
NOTE: Bit number zero is closest to TDO.

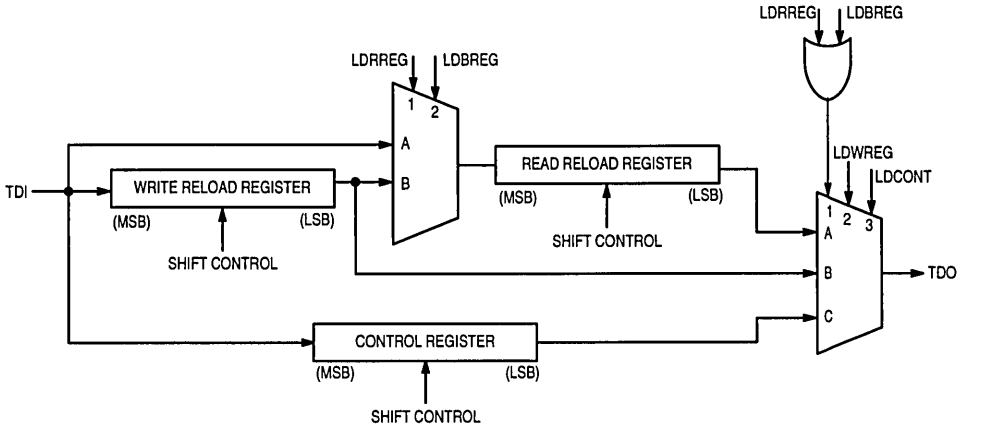
Table 9. LDWREG Scan Path Bit Definitions

Bit Number	Bit/Pin Name*	Bit/Pin Type
0	WRR0	Register bit
1	WRR1	Register bit
2	WRR2	Register bit
3	WRR3	Register bit
4	WRR4	Register bit
5	WRR5	Register bit
6	WRR6	Register bit
7	WRR7	Register bit
8	WRR8	Register bit
9	WRR9	Register bit
10	WRR10	Register bit
11	WRR11	Register bit
12	WRR12	Register bit
13	WRR13	Register bit
14	WRR14	Register bit
15	WRR15	Register bit

* WRR = Write Reload Register

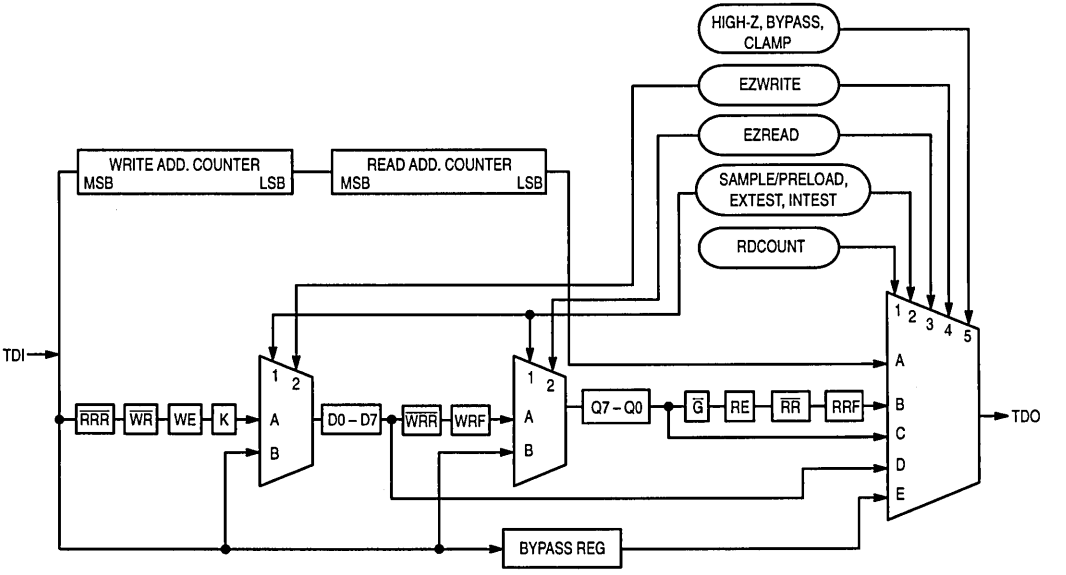
Table 10. LDCONT Scan Path Bit Definitions

Bit Number	Bit/Pin Name	Bit/Pin Type
0	EX0	Register bit
1	EX1	Register bit
2	EX2	Register bit
3	WCC	Register bit
4	UDW	Register bit
5	RCC	Register bit
6	UDR	Register bit
7	G CONT	Register bit



THE LEFT MOST CONTROL SIGNAL ENTERING THE MUX FROM THE TOP(1) SELECTS THE UPPER MOST INPUT ON THE LEFT SIDE OF THE MUX(A). THE RIGHT MOST CONTROL SIGNAL SELECTS THE BOTTOM MOST INPUT.

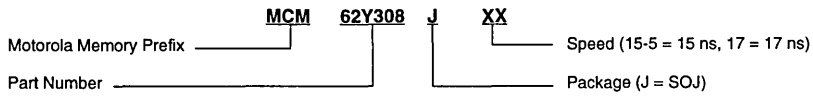
Figure 3. Register Load Paths



THE LEFT MOST CONTROL SIGNAL ENTERING THE MUX FROM THE TOP(1) SELECTS THE UPPER MOST INPUT ON THE LEFT SIDE OF THE MUX(A). THE RIGHT MOST CONTROL SIGNAL SELECTS THE BOTTOM MOST INPUT.

Figure 4. Boundary Scan Paths

ORDERING INFORMATION
(Order by Full Part Number)



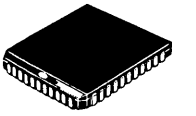
Full Part Numbers — MCM62Y308J15-5 MCM62Y308J17

4

MCM62T316

Product Preview

8K x 16 Bit Synchronous Cache Tag
With Comparator



FN PACKAGE
44-LEAD PLCC
CASE 777

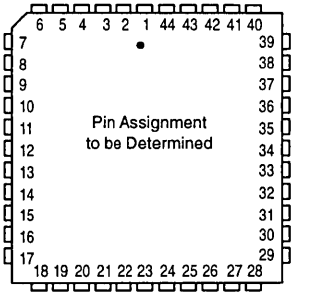
The MCM62T316 is a 131,072 bit synchronous static random access memory organized as 8,192 words of 16 bits, fabricated using Motorola's double-metal, double-poly, 0.65 µm CMOS process. Each word contains a 15-bit address tag and a valid bit.

The MCM62T316 compares the specified RAM address tag with the current input data. The result is either an active high MATCH level for a valid cache hit, or an active low level for a cache miss. The valid bit of the address tag must be set for a valid cache hit. The entire tag memory can be invalidated by holding the $\overline{\text{INVAL}}$ pin low for four consecutive cycles.

The MCM62T316 is available in a 44 pin PLCC package.

- 8K x 16 Fast Access Static Memory Array
- Single 5 V ± 10% Power Supply
- Fast Match Access Time: 12 ns Max
- Fast Clock Cycle Time: 20 ns Max
- Registered Address, Data, and Control Inputs
- Valid Bit on Each Word to Qualify a Valid Hit
- Four Cycles to Invalidate the Entire Tag Memory
- Cascadable to Two Cache Tags with No External Logic

PIN ASSIGNMENT



PIN NAMES	
A0 – A12	Tag Address Inputs
K	Clock Input
$\overline{\text{TS}}$	Tag Select Input
$\overline{\text{W}}$	Tag Write Enable Input
VALID	Valid Bit Input/Output
$\overline{\text{INVAL}}$	Tag Invalidate Input
MATCH	Cache Match Output
$\overline{\text{G}}$	Output Enable Input
$\overline{\text{CS0}}$, $\overline{\text{CS1}}$, CS2	Chip Select Input
DQ0–DQ14	Data Input/Outputs
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

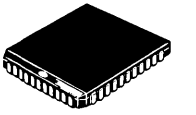
All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

MCM62486A

32K x 9 Bit BurstRAM™ Synchronous Static RAM

With Burst Counter and Self-Timed Write



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62486A is a 294,912 bit synchronous static random access memory designed to provide a burstable, high-performance, secondary cache for the i486 and Pentium™ microprocessors. It is organized as 32,768 words of 9 bits, fabricated with Motorola's high-performance silicon-gate CMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A14), data inputs (D0 – D8), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive-edge-triggered noninverting registers.

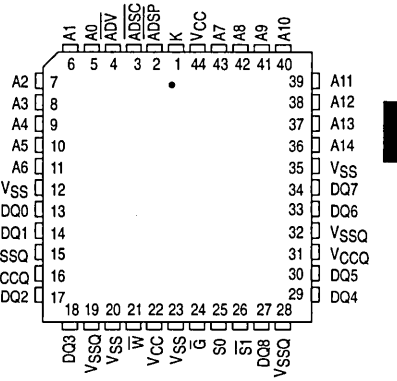
Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM62486A (burst sequence imitates that of the i486 and Pentium) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The MCM62486A will be available in a 44-pin plastic leaded chip carrier (PLCC). Multiple power and ground pins have been utilized to minimize effects induced by output noise. Separate power and ground pins have been employed for DQ0 – DQ8 to allow user-controlled output levels of 5 volts or 3.3 volts.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Level Compatibility
- Fast Access Times: 11/12/14/19/24 ns Max and Cycle Times: 15/20/25/30 ns Min
- Internal Input Registers (Address, Data, Control)
- Internally Self-Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- High Output Drive Capability: 85 pF per I/O
- High Board Density PLCC Package
- Fully TTL-Compatible
- Active High and Low Chip Select Inputs for Easy Depth Expansion

PIN ASSIGNMENT

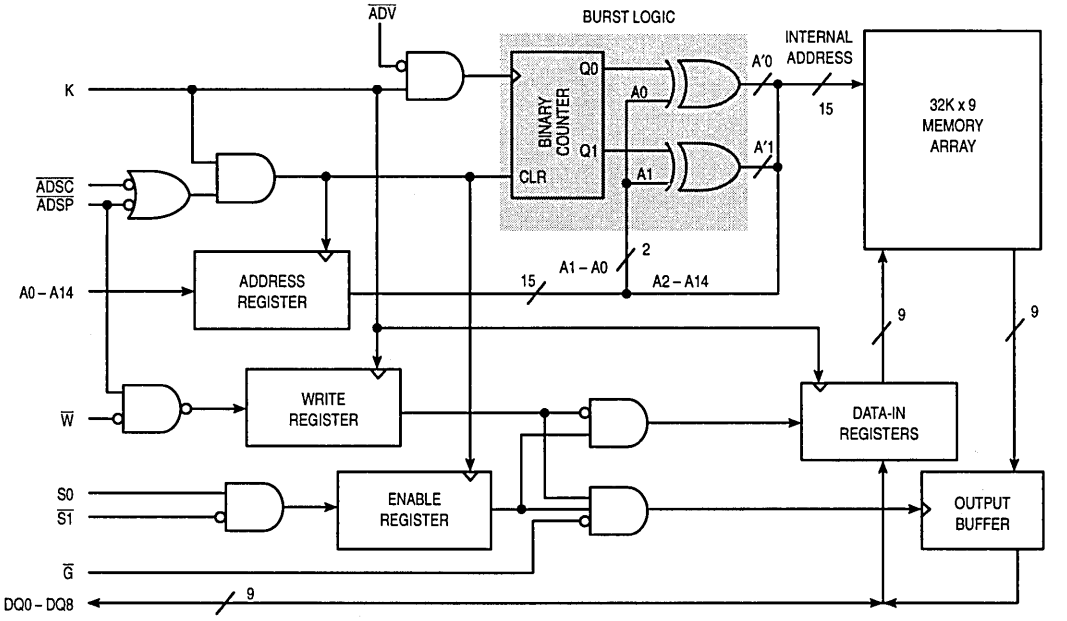


PIN NAMES	
A0 – A14	Address Inputs
K	Clock
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
S0, $\overline{S1}$	Chip Selects
$\overline{ADV}$	Burst Address Advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status
DQ0 – DQ8	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

BurstRAM is a trademark of Motorola, Inc.
i486 and Pentium are trademarks of Intel Corp.

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive-edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip selects (S0, $\overline{S1}$) are sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**.

BURST SEQUENCE TABLE (See Note)

External Address	A14 – A2	A1	A0
1st Burst Address	A14 – A2	A1	$\overline{A0}$
2nd Burst Address	A14 – A2	$\overline{A1}$	A0
3rd Burst Address	A14 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, 3, and 4)

S	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}$	K	Address Used	Operation
F	L	X	X	X	L-H	N/A	Deselected
F	X	L	X	X	L-H	N/A	Deselected
T	L	X	X	X	L-H	External Address	Read Cycle, Begin Burst
T	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
T	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. S represents S0 and $\overline{S1}$. T implies $\overline{S1}$ = L and S0 = H; F implies $\overline{S1}$ = H or S0 = L.
4. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out (DQ0 – DQ8)
Read	H	High-Z
Write	X	High-Z — Data In (DQ0 – DQ8)
Deselected	X	High-Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Output Power Supply Voltage	V_{CCQ}	– 0.5 to V_{CC}	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	 4.5 3.0	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$, $\overline{S1}$ = V_{IH}, S0 = V_{IL}, V_{out} = 0 to V_{CCQ})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$, $\overline{S1}$ = V_{IL}, S0 = V_{IH}, All Inputs = V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min)	I_{CCA}	—	175	mA
Standby Current ($\overline{S1}$ = V_{IH}, S0 = V_{IL}, All Inputs = V_{IL} and V_{IH}, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	40	mA
CMOS Standby Current ($\overline{S1}$ ≥ V_{CC} – 0.2 V, S0 ≤ 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V, Cycle Time ≥ t_{KHKH} min)	I_{SB2}	—	30	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ8)	C_{in}	2	3	pF
Input/Output Capacitance (DQ0 – DQ8)	$C_{I/O}$	7	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}, V_{CCQ} = 5.0 V ± 5%, T_A = 0 to + 70°C, for device MCM62486A-11)
(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, for all other devices)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol		62486A-11		62486A-12		62486A-14		62486A-19		62486A-24		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	t_{CYC}	15	—	20	—	20	—	25	—	30	—	ns	
Clock Access Time	t_{KHQV}	t_{CD}	—	11	—	12	—	14	—	19	—	24	ns	4
Output Enable Access	t_{GLQV}	t_{OE}	—	5	—	5	—	6	—	7	—	7	ns	
Clock High to Output Active	t_{KHQX1}	t_{DC1}	6	—	6	—	6	—	6	—	6	—	ns	
Clock High to Q Change	t_{KHQX2}	t_{DC2}	3	—	3	—	4	—	4	—	4	—	ns	
Output Enable to Q Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	0	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{OHZ}	—	6	—	6	—	6	—	7	—	7	ns	5
Clock High to Q High-Z	t_{KHQZ}	t_{CZ}	—	6	—	6	—	6	—	6	—	6	ns	
Clock High Pulse Width	t_{KHKL}	t_{CH}	5.5	—	7	—	8	—	6	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	t_{CL}	5.5	—	7	—	8	—	6	—	6	—	ns	
Setup Times: Address Address Status Data In Write Address Advance Chip Select	t_{AVKH} t_{ADSVKH} t_{DVKH} t_{WVKH} t_{ADVVKH} t_{S0VKH} t_{S1VKH}	t_{AS} t_{SS} t_{DS} t_{WS}	2	—	2	—	3	—	3	—	3	—	ns	6
Hold Times: Address Address Status Data In Write Address Advance Chip Select	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHADVX} t_{KHS0X} t_{KHS1X}	t_{AH} t_{SH} t_{DH} t_{WH}	2	—	2	—	2	—	2	—	2	—	ns	6

NOTES:
1. A read cycle is defined by $\overline{W}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{W}$ low and $\overline{ADSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{W}$ is sampled low.
4. The MCM62486A-19 and MCM62486A-24 will meet all 33 MHz specifications, even when K is running at 66 MHz.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX1} min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of clock (K) whenever $\overline{ADSP}$ and $\overline{ADSC}$ are low and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is selected.Chip select must be true ($\overline{S1}$ low and S0 high) at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled. Timings for $\overline{S1}$ and S0 are similar.

AC TEST LOADS

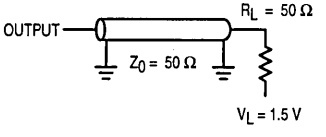


Figure 1A

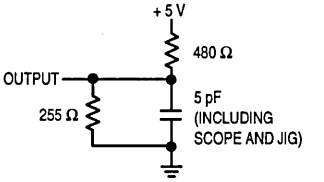
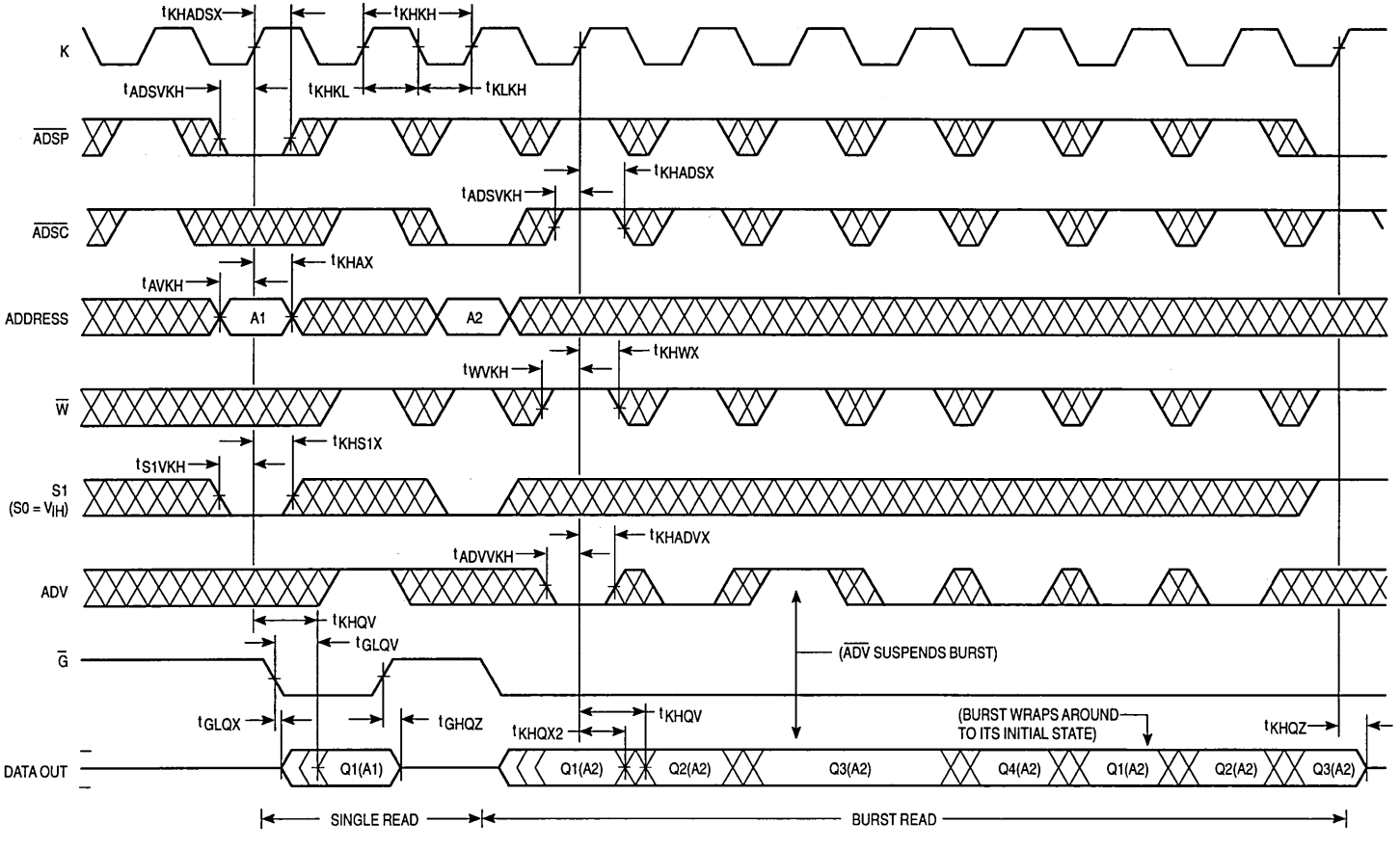


Figure 1B

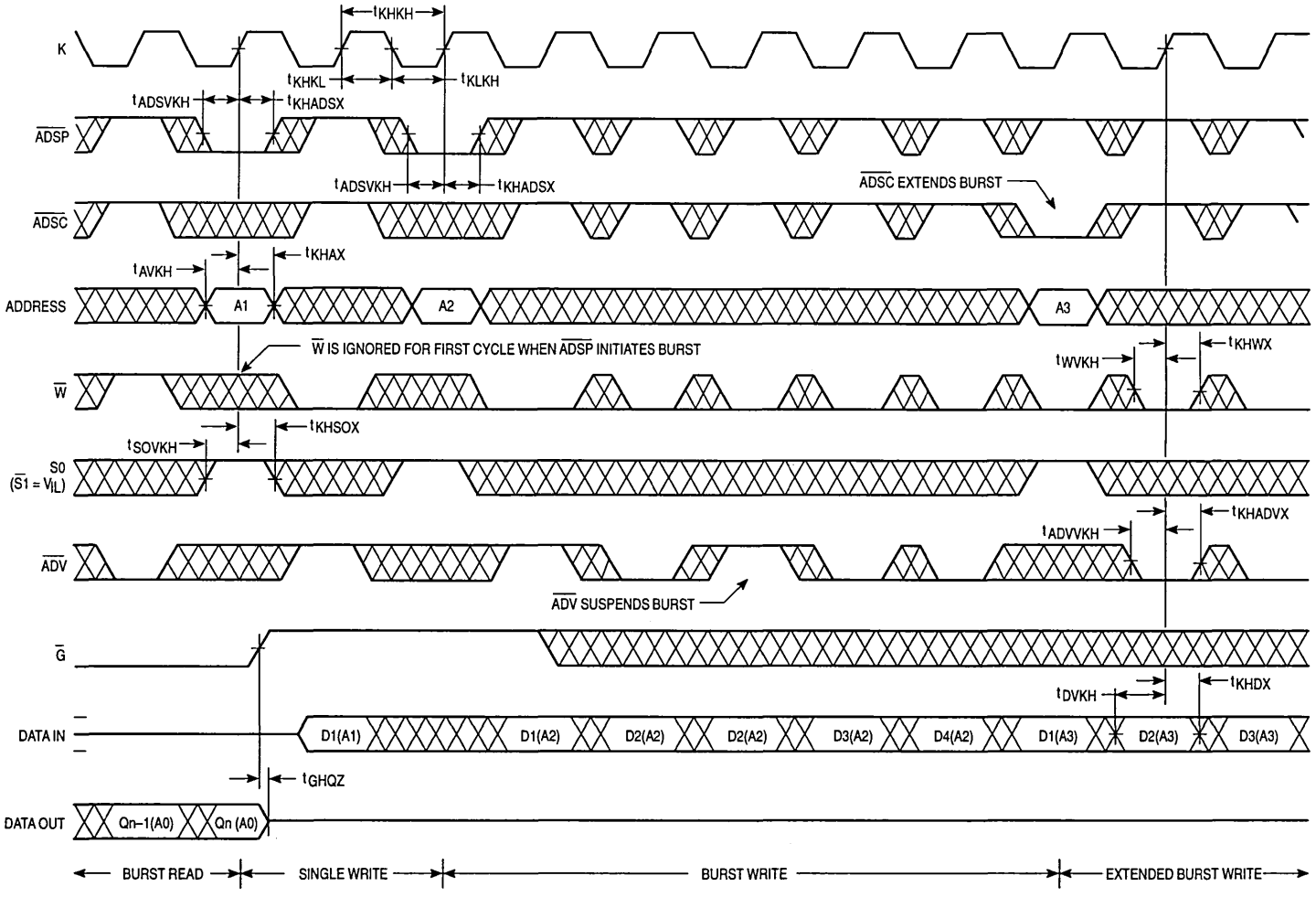
NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLES

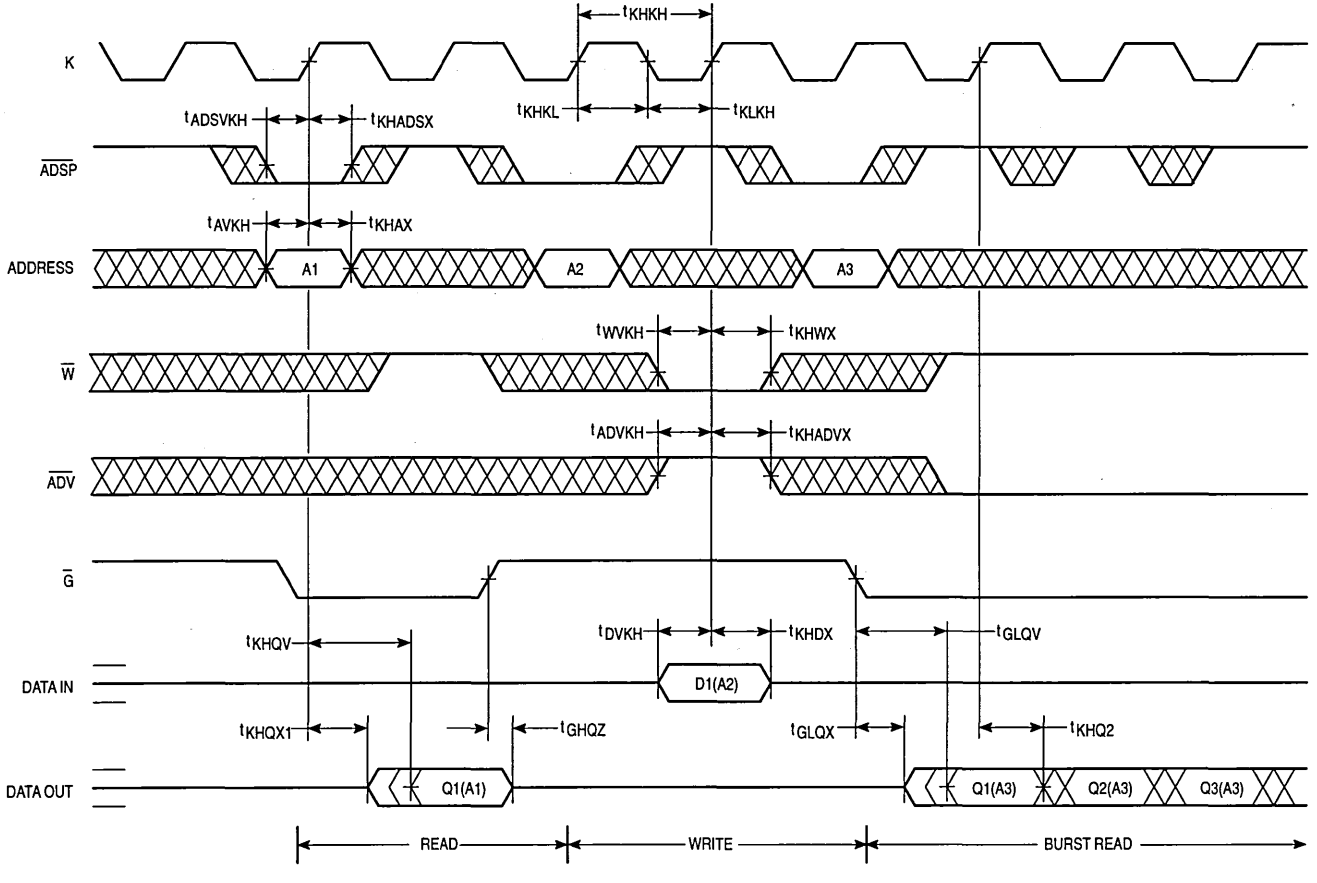


NOTE: Q1(A2) represents the first output data from the base address A2; Q2(A2) represents the next output data in the burst sequence with A2 as the base address.

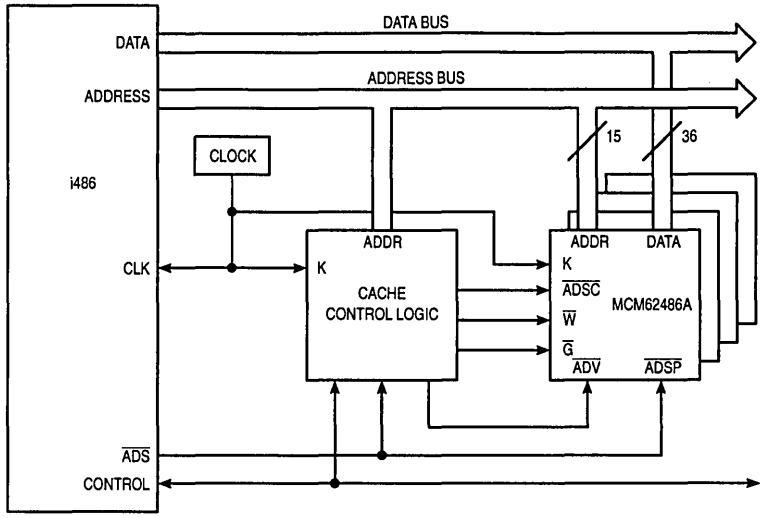
WRITE CYCLES



COMBINATION READ/WRITE CYCLE



APPLICATION EXAMPLE



128K BYTE BURSTABLE, SECONDARY CACHE USING
4 MCM62486AFN24s WITH A 33 MHz i486

4

ORDERING INFORMATION
(Order by Full Part Number)

MCM 62486A X XX

Motorola Memory Prefix

Part Number

Speed (11 = 11 ns, 12 = 12 ns, 14 = 14 ns, 19 = 19 ns, 24 = 24 ns)

Package (FN = PLCC)

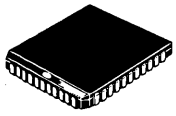
Full Part Numbers — MCM62486AFN11 MCM62486AFN12 MCM62486AFN14 MCM62486AFN19 MCM62486AFN24

MCM62486B

Advance Information

32K x 9 Bit BurstRAM™ Synchronous Static RAM

With Burst Counter and Self-Timed Write



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62486B is a 294,912 bit synchronous static random access memory designed to provide a burstable, high-performance, secondary cache for the i486 and Pentium™ microprocessors. It is organized as 32,768 words of 9 bits, fabricated with Motorola's high-performance silicon-gate CMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A14), data inputs (D0 – D8), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive-edge-triggered noninverting registers.

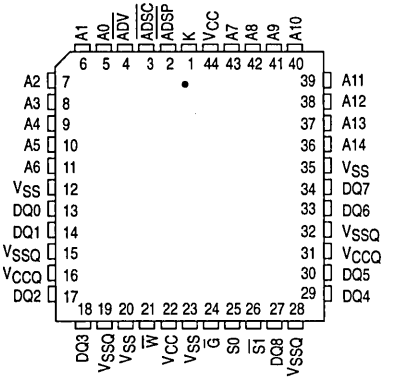
Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM62486B (burst sequence imitates that of the i486 and Pentium) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The MCM62486B will be available in a 44-pin plastic leaded chip carrier (PLCC). Multiple power and ground pins have been utilized to minimize effects induced by output noise. Separate power and ground pins have been employed for DQ0 – DQ8 to allow user-controlled output levels of 5 volts or 3.3 volts.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Level Compatibility
- Fast Access Times: 11/12/14/19/24 ns Max and Cycle Times: 15/20/25/30 ns Min
- Internal Input Registers (Address, Data, Control)
- Internally Self-Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- High Output Drive Capability: 85 pF per I/O
- High Board Density PLCC Package
- Fully TTL-Compatible
- Active High and Low Chip Select Inputs for Easy Depth Expansion

PIN ASSIGNMENT



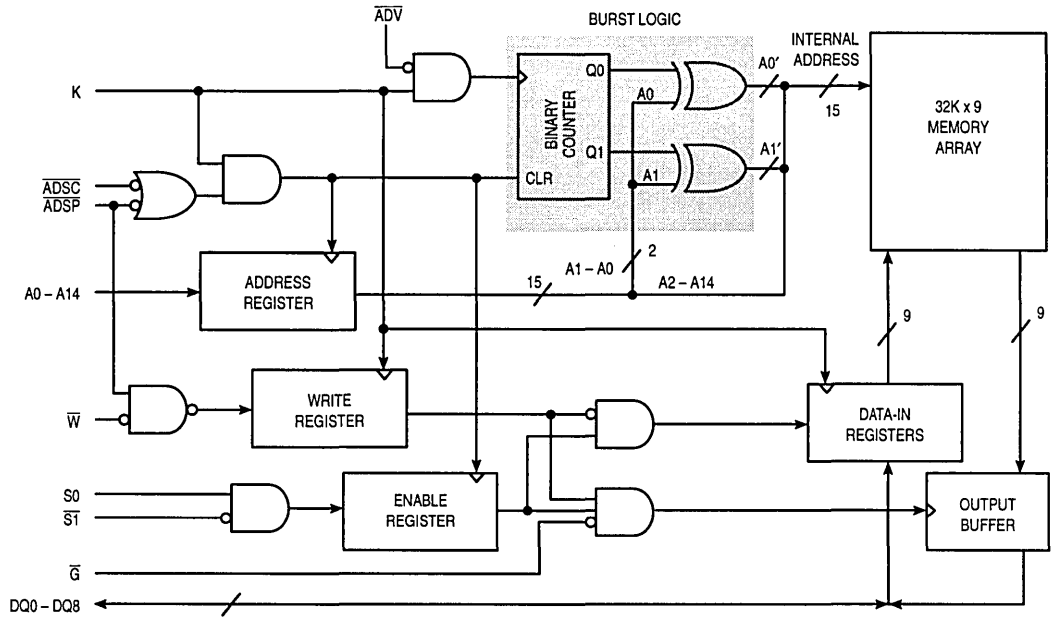
PIN NAMES	
A0 – A14	Address Inputs
K	Clock
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
S0, $\overline{S1}$	Chip Selects
$\overline{ADV}$	Burst Address Advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status
DQ0 – DQ8	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

BurstRAM is a trademark of Motorola, Inc.
i486 and Pentium are trademarks of Intel Corp.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive-edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip selects (S0, $\overline{S1}$) are sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**.

BURST SEQUENCE TABLE (See Note)

External Address	A14 – A2	A1	A0
1st Burst Address	A14 – A2	A1	$\overline{A0}$
2nd Burst Address	A14 – A2	$\overline{A1}$	A0
3rd Burst Address	A14 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, 3, and 4)

S	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}$	K	Address Used	Operation
F	L	X	X	X	L-H	N/A	Deselected
F	X	L	X	X	L-H	N/A	Deselected
T	L	X	X	X	L-H	External Address	Read Cycle, Begin Burst
T	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
T	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. S represents S0 and $\overline{S1}$. T implies $\overline{S1}$ = L and S0 = H; F implies $\overline{S1}$ = H or S0 = L.
4. Wait states are inserted by suspending burst.

4

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out (DQ0 – DQ8)
Read	H	High-Z
Write	X	High-Z — Data In (DQ0 – DQ8)
Deselected	X	High-Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Output Power Supply Voltage	V_{CCQ}	– 0.5 to V_{CC}	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	 4.5 3.0	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$, $\overline{S1}$ = V_{IH}, S0 = V_{IL}, V_{out} = 0 to V_{CCQ})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$, $\overline{S1}$ = V_{IL}, S0 = V_{IH}, All Inputs = V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min)	I_{CCA}	—	150	mA
Standby Current ($\overline{S1}$ = V_{IH}, S0 = V_{IL}, All Inputs = V_{IL} and V_{IH}, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	40	mA
CMOS Standby Current ($\overline{S1}$ ≥ V_{CC} – 0.2 V, S0 ≤ 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V, Cycle Time ≥ t_{KHKH} min)	I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible I486 bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ8)	C_{in}	2	3	pF
Input/Output Capacitance (DQ0 – DQ8)	$C_{I/O}$	7	8	pF

4

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}, V_{CCQ} = 5.0 V ± 5%, T_A = 0 to + 70°C, for device MCM62486A-11)
(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, for all other devices)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol		62486B-11		62486B-12		62486B-14		62486B-19		62486B-24		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	t_{CYC}	15	—	20	—	20	—	25	—	30	—	ns	
Clock Access Time	t_{KHQV}	t_{CD}	—	11	—	12	—	14	—	19	—	24	ns	4
Output Enable Access	t_{GLQV}	t_{OE}	—	5	—	5	—	6	—	7	—	7	ns	
Clock High to Output Active	t_{KHQX1}	t_{DC1}	6	—	6	—	6	—	6	—	6	—	ns	
Clock High to Q Change	t_{KHQX2}	t_{DC2}	3	—	3	—	4	—	4	—	4	—	ns	
Output Enable to Q Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	0	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{OHZ}	—	6	—	6	—	6	—	7	—	7	ns	5
Clock High to Q High-Z	t_{KHQZ}	t_{CZ}	—	6	—	6	—	6	—	6	—	6	ns	
Clock High Pulse Width	t_{KHKL}	t_{CH}	5.5	—	7	—	8	—	6	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	t_{CL}	5.5	—	7	—	8	—	6	—	6	—	ns	
Setup Times: Address Address Status Data In Write Address Advance Chip Select	t_{AVKH} t_{ADSVKH} t_{DVKH} t_{WVKH} t_{ADVVKH} t_{S0VKH} t_{S1VKH}	t_{AS} t_{SS} t_{DS} t_{WS}	2	—	2	—	3	—	3	—	3	—	ns	6
Hold Times: Address Address Status Data In Write Address Advance Chip Select	t_{KHAX} t_{KHADSX} t_{KHDX} t_{KHWX} t_{KHADVX} t_{KHS0X} t_{KHS1X}	t_{AH} t_{SH} t_{DH} t_{WH}	2	—	2	—	2	—	2	—	2	—	ns	6

NOTES:
1. A read cycle is defined by $\overline{W}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{W}$ low and $\overline{ADSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{W}$ is sampled low.
4. The MCM62486A-19 and MCM62486A-24 will meet all 33 MHz specifications, even when K is running at 66 MHz.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX1} min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of clock (K) whenever $\overline{ADSP}$ and $\overline{ADSC}$ are low and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is selected.Chip select must be true ($\overline{S1}$ low and S0 high) at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled. Timings for $\overline{S1}$ and S0 are similar.

AC TEST LOADS

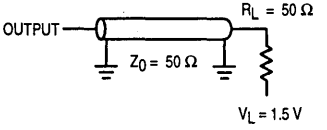


Figure 1A

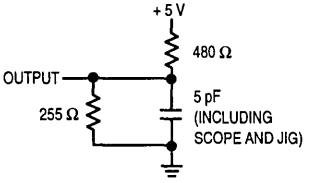
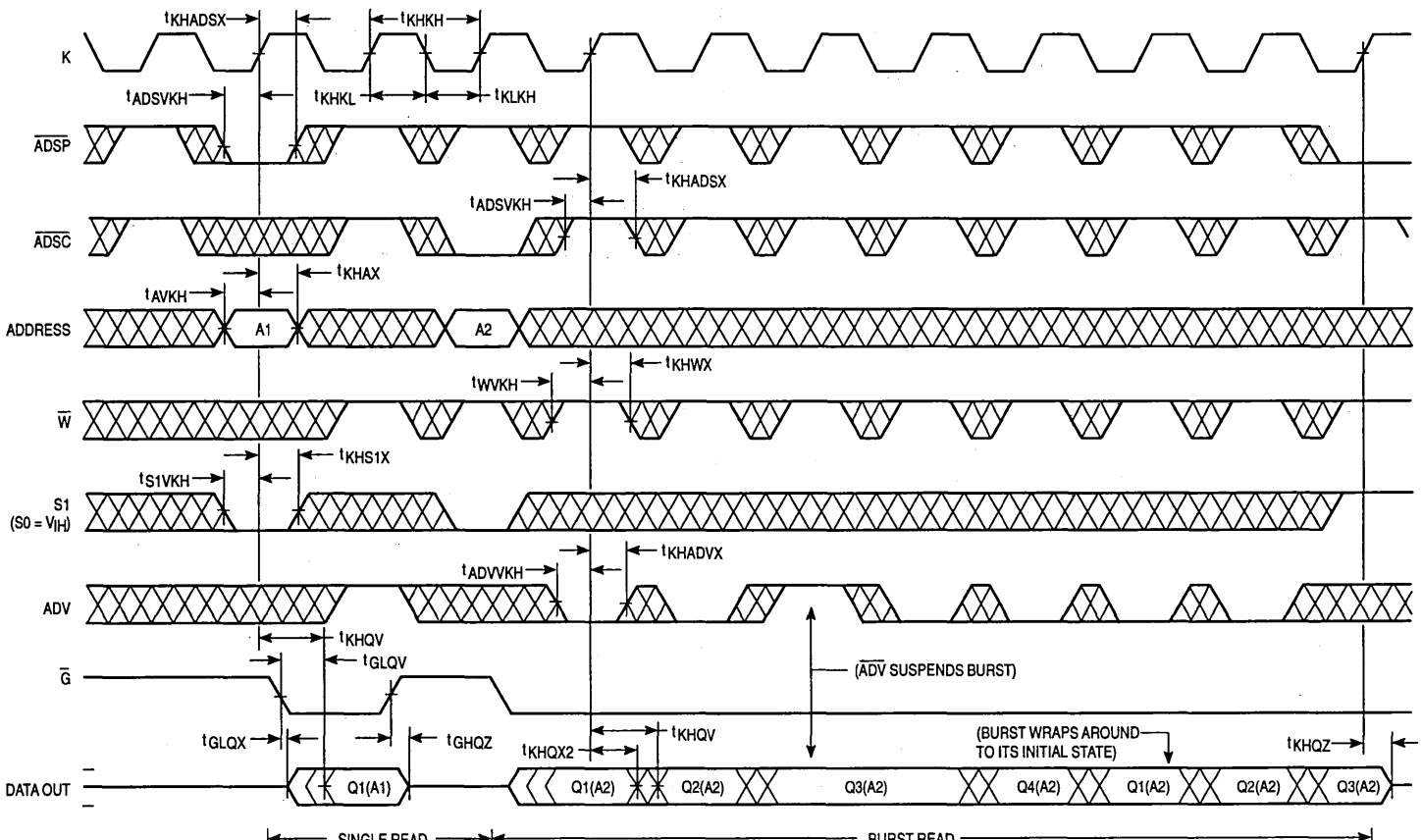


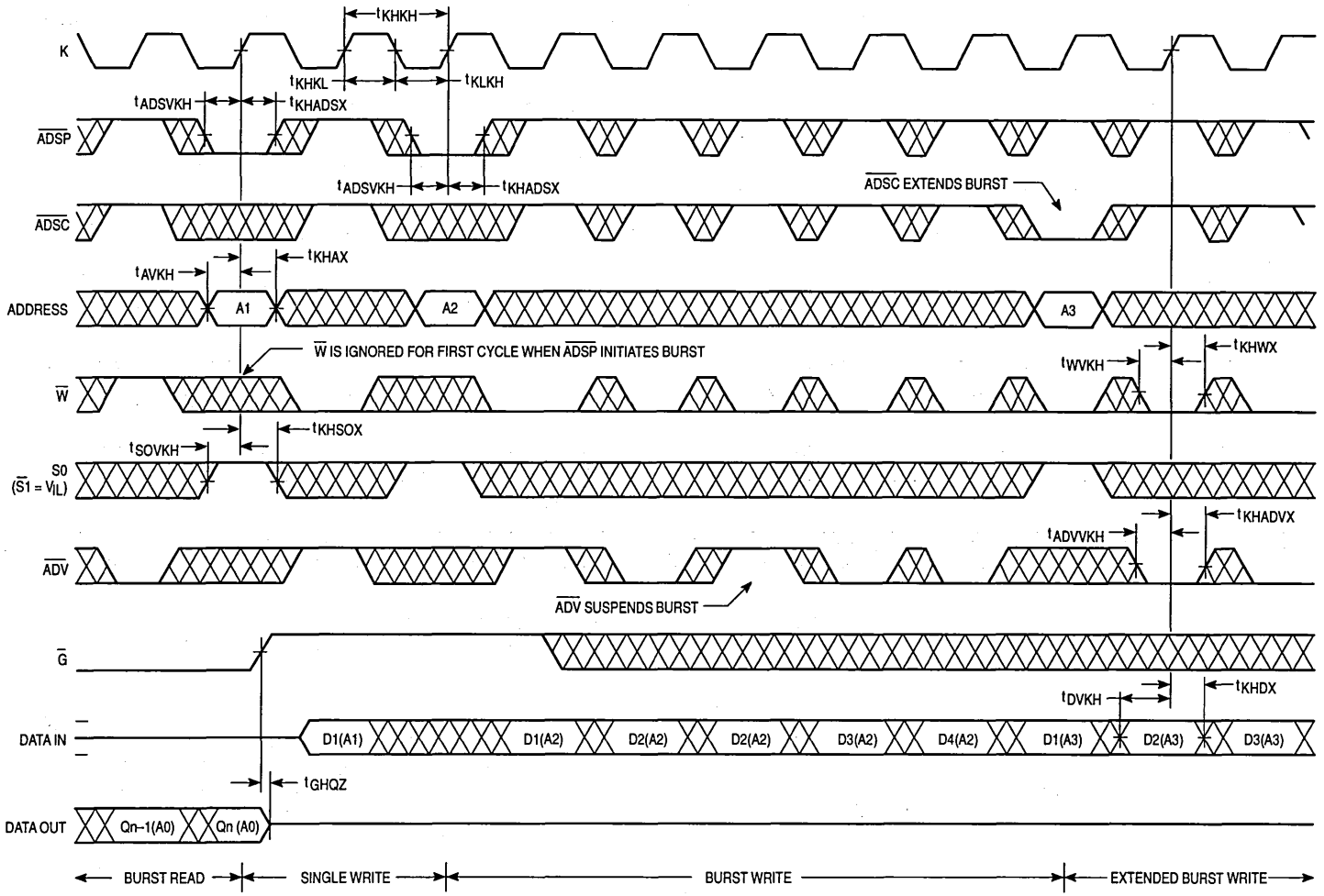
Figure 1B

READ CYCLES

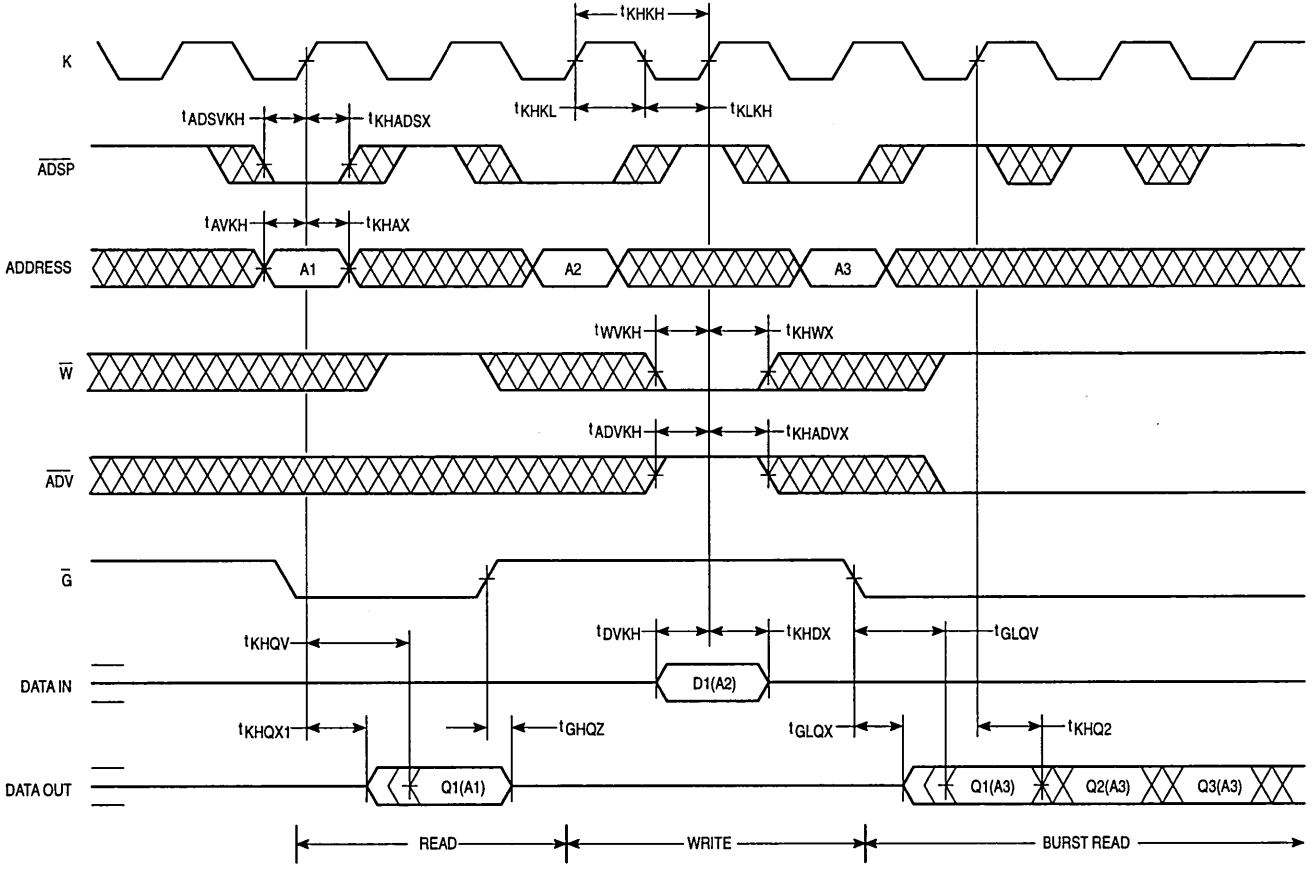


NOTE: Q1(A2) represents the first output data from the base address A2; Q2(A2) represents the next output data in the burst sequence with A2 as the base address.

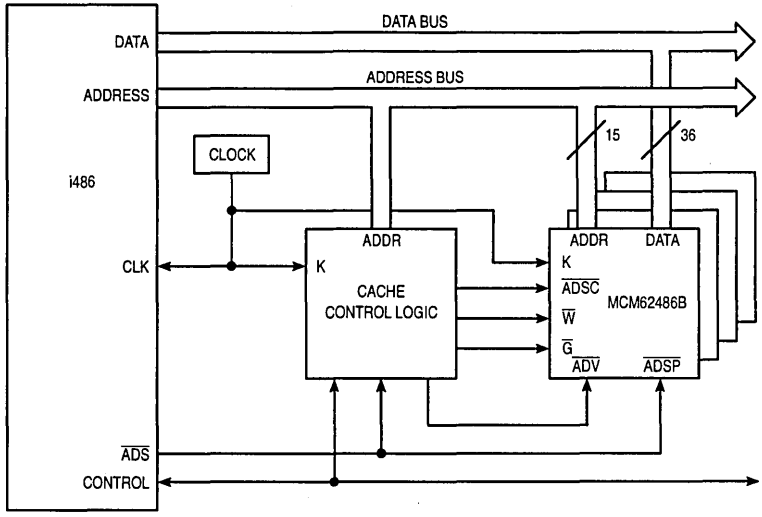
WRITE CYCLES



COMBINATION READ/WRITE CYCLE



APPLICATION EXAMPLE



128K BYTE BURSTABLE, SECONDARY CACHE USING
4 MCM62486BFN24s WITH A 33 MHz i486

ORDERING INFORMATION
(Order by Full Part Number)

MCM 62486B X XX

Motorola Memory Prefix

Part Number

Speed (11 = 11 ns, 12 = 12 ns, 14 = 14 ns, 19 = 19 ns, 24 = 24 ns)

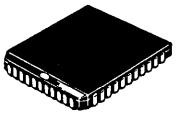
Package (FN = PLCC)

Full Part Numbers — MCM62486BFN11 MCM62486BFN12 MCM62486BFN14 MCM62486BFN19 MCM62486BFN24

MCM62940A

32K x 9 Bit BurstRAM™ Synchronous Static RAM

With Burst Counter and Self-Timed Write



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62940A is a 294,912 bit synchronous static random access memory designed to provide a burstable, high-performance, secondary cache for the MC68040 and PowerPC™ microprocessors. It is organized as 32,768 words of 9 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A14), data inputs (DQ0 – DQ8), and all control signals, except output enable ($\overline{G}$), are clock (K) controlled through positive-edge-triggered noninverting registers.

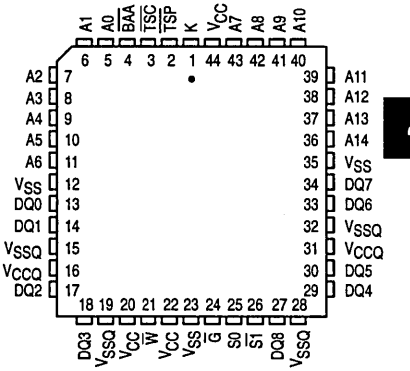
Bursts can be initiated with either transfer start processor ($\overline{TSP}$) or transfer start cache controller ($\overline{TSC}$) input pins. Subsequent burst addresses are generated internally by the MCM62940A (burst sequence imitates that of the MC68040) and controlled by the burst address advance ($\overline{BAA}$) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The MCM62940A is packaged in a 44-pin plastic-leaded chip carrier (PLCC). Multiple power and ground pins have been utilized to minimize effects induced by output noise. Separate power and ground pins have been employed for DQ0 – DQ8 to allow user-controlled output levels of 5 volts or 3.3 volts.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Level Compatibility
- Fast Access Times: 11/12/14/19/24 ns Max, Cycle Times: 15/20/20/25/30 ns Min
- Internal Input Registers (Address, Data, Control)
- Internally Self-Timed Write Cycle
- $\overline{TSP}$, $\overline{TSC}$, and $\overline{BAA}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- High Output Drive Capability: 85 pF per I/O
- High Board Density PLCC Package
- Fully TTL-Compatible
- Active High and Low Chip Select Inputs for Easy Depth Expansion

PIN ASSIGNMENT



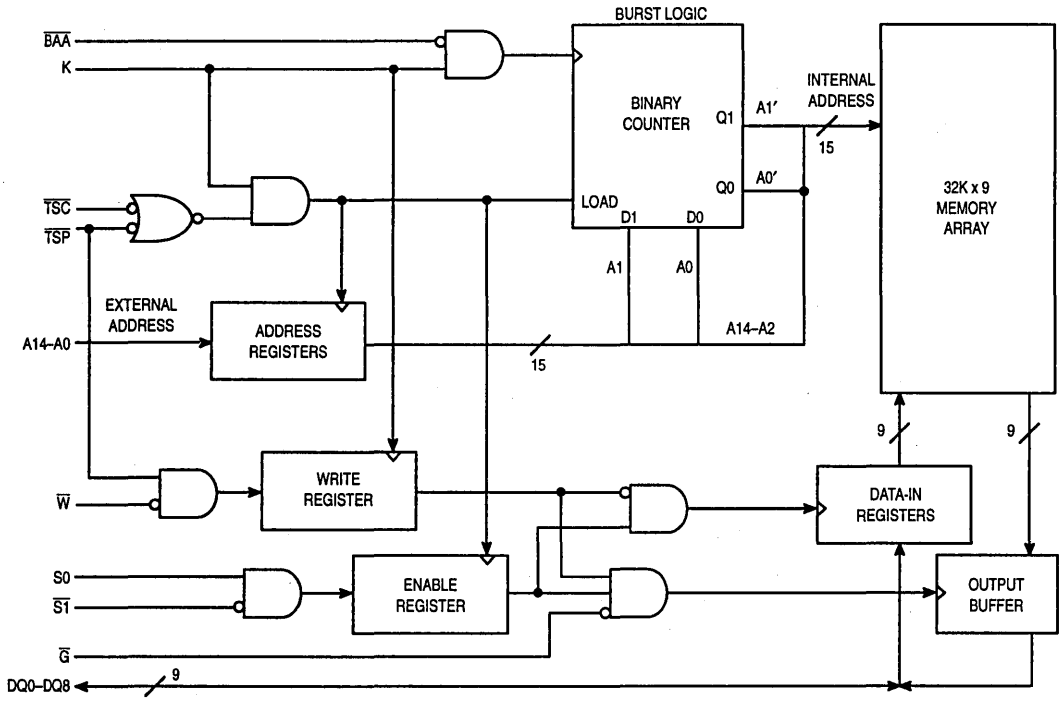
PIN NAMES

A0 – A14	Address Inputs
K	Clock
$\overline{W}$	Synchronous Write
$\overline{G}$	Output Enable
S0, $\overline{S1}$	Chip Selects
$\overline{BAA}$	Burst Address Advance
$\overline{TSP}$, $\overline{TSC}$	Transfer Start
DQ0 – DQ8	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

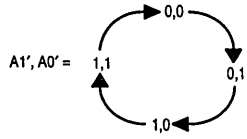
BurstRAM is a trademark of Motorola, Inc.
PowerPC is a trademark of IBM Corp.

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive-edge triggered. The $\overline{TSC}$ or $\overline{TSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{TSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{TSC}$) is performed using the new external address. When $\overline{TSC}$ is sampled low (and $\overline{TSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the next external address. Chip selects (S0, $\overline{S1}$) are sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{BAA}$ controls subsequent burst cycles. When $\overline{BAA}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{BAA}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE GRAPH.**

BURST SEQUENCE GRAPH (See Note)



NOTE: The external two values for A1 and A0 provide the starting point for the burst sequence graph. The burst logic advances A1 and A0 as shown above.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, 3, and 4)

S	$\overline{TSP}$	$\overline{TSC}$	$\overline{BAA}$	$\overline{W}$	K	Address	Operation
F	L	X	X	X	L-H	N/A	Deselected
F	X	L	X	X	L-H	N/A	Deselected
T	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
T	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
T	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. S represents S0 and $\overline{S1}$. T implies S0 = H and $\overline{S1}$ = L; F implies S0 = L or $\overline{S1}$ = H.
4. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out (DQ0–DQ8)
Read	H	High-Z
Write	X	High-Z — Data In (DQ0–DQ8)
Deselected	X	High-Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data requird setup time and held high throughout the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Output Power Supply Voltage	V_{CCQ}	– 0.5 to V_{CC}	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	 4.5 3.0	 5.0 3.3	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$, $\overline{S1}$ = V_{IH}, S0 = V_{IL}, V_{out} = 0 to V_{CCQ})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$, $\overline{S1}$ = V_{IL}, S0 = V_{IH}, All Inputs = V_{IL} = 0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min)	I_{CCA}	—	165	mA
Standby Current ($\overline{S1}$ = V_{IH}, S0 = V_{IL}, All Inputs = V_{IL} and V_{IH}, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	40	mA
CMOS Standby Current ($\overline{S1}$ ≥ V_{CC} – 0.2 V, S0 ≤ 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V, Cycle TIme ≥ t_{KHKH} min)	I_{SB2}	—	30	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible MC68040 bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ8)	C_{in}	2	3	pF
Input/Output Capacitance (DQ0 – DQ8)	$C_{I/O}$	7	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol Std	Symbol Alt	62940A-11 Min	62940A-11 Max	62940A-12 Min	62940A-12 Max	62940A-14 Min	62940A-14 Max	62940A-19 Min	62940A-19 Max	62940A-24 Min	62940A-24 Max	Unit	Notes
Cycle Time	t_{KHKH}	t_{CYC}	15	—	20	—	20	—	25	—	30	—	ns	
Clock Access Time	t_{KHQV}	t_{CD}	—	11	—	12	—	14	—	19	—	24	ns	4
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	5	—	5	—	6	—	7	—	7	ns	
Clock High to Output Active	t_{KHQX1}	t_{DC1}	6	—	6	—	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	t_{DC2}	3	—	3	—	5	—	5	—	5	—	ns	
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	0	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{OHZ}	—	6	—	6	—	6	—	7	—	7	ns	5
Clock High to Q High-Z	t_{KHQZ}	t_{CZ}	—	6	—	6	—	6	—	6	—	6	ns	5
Clock High Pulse Width	t_{KHKL}	t_{CH}	5.5	—	7	—	8	—	9	—	11	—	ns	
Clock Low Pulse Width	t_{KLKH}	t_{CL}	5.5	—	7	—	8	—	9	—	11	—	ns	
Setup Times: Address	t_{AVKH}	t_{AS}	2	—	2	—	3	—	3	—	3	—	ns	6
Address Status	t_{TSVKH}	t_{SS}												
Data In	t_{DVKH}	t_{DS}												
Write	t_{WVKH}	t_{WS}												
Address Advance	t_{BAVKH}													
Chip Select	t_{S0VKH}													
	t_{S1VKH}													
Hold Times: Address	t_{KHAX}	t_{AH}	2	—	2	—	2	—	2	—	2	—	ns	6
Address Status	t_{KHTSX}	t_{SH}												
Data In	t_{KHDX}	t_{DH}												
Write	t_{KHWX}	t_{WH}												
Address Advance	t_{KHBAX}													
Chip Select	t_{KHS0X}													
	t_{KHS1X}													

NOTES:
1. A read cycle is defined by $\overline{W}$ high or $\overline{TSP}$ low for the setup and hold times. A write cycle is defined by $\overline{W}$ low and $\overline{TSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{W}$ is sampled low.
4. Maximum access times are guaranteed for all possible MC68040 external bus cycles.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX1} min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of clock (K) whenever $\overline{TSP}$ or $\overline{TSC}$ are low and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is selected.Chip select must be true ($\overline{S1}$ low and S0 high) at each rising edge of clock for the device (when $\overline{TSP}$ or $\overline{TSC}$ is low) to remain enabled. Timings for $\overline{S1}$ and S0 are similar.

AC TEST LOADS

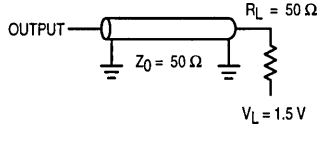


Figure 1A

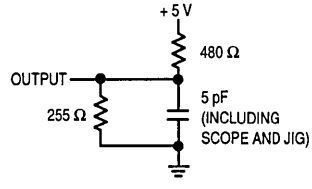
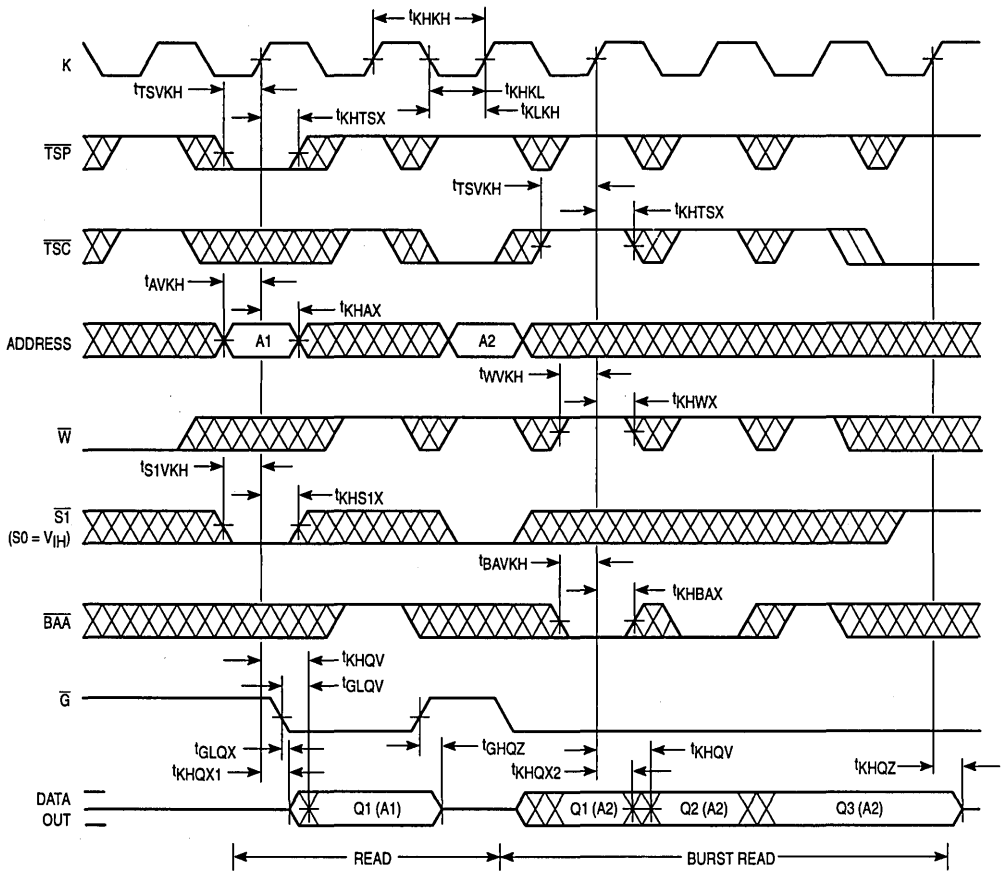


Figure 1B

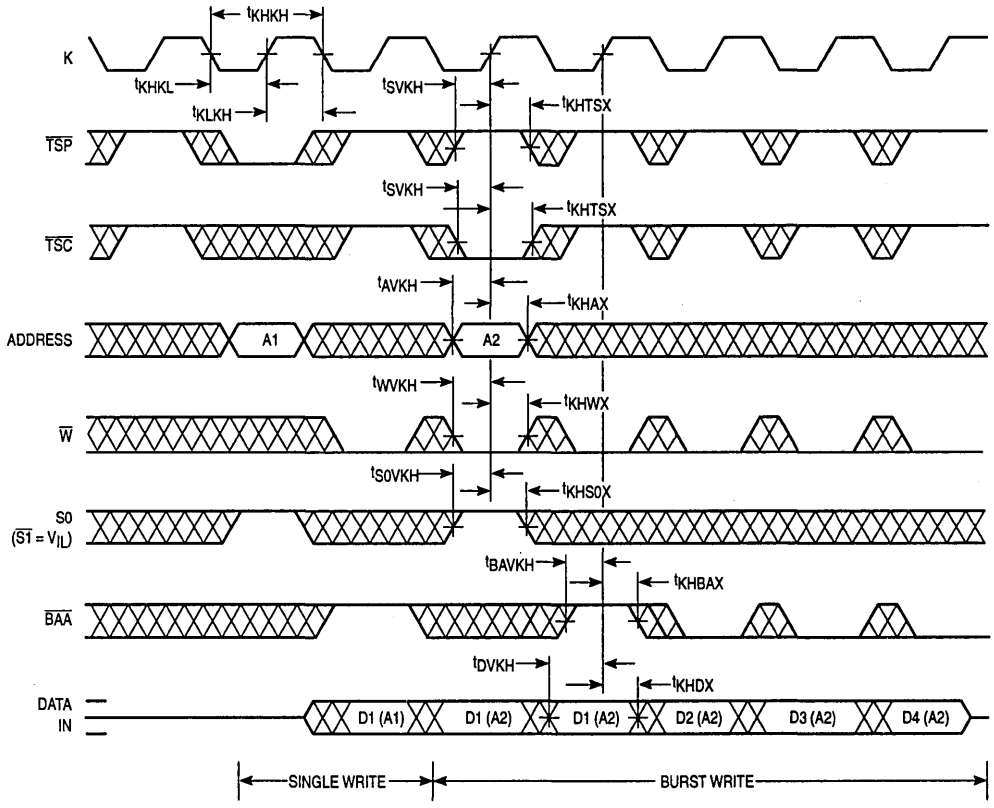
NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ-WRITE CYCLE



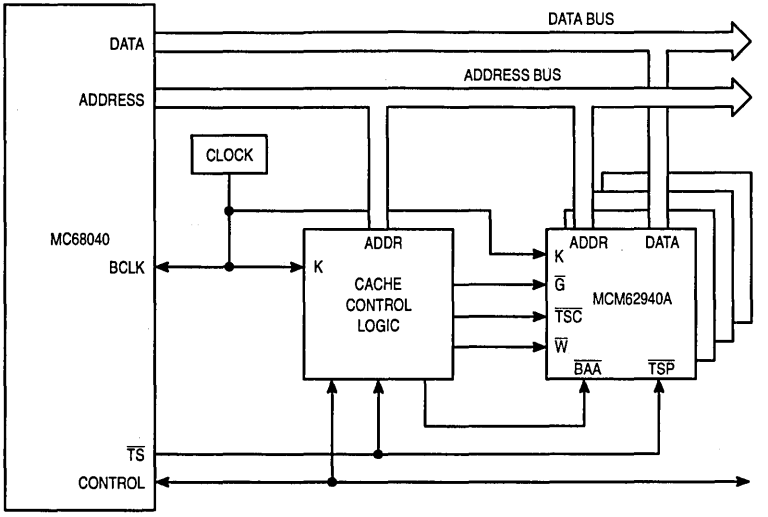
NOTE: Q1(A2) represents the first output from the external address A2; Q2(A2) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLE



NOTE: $\overline{G}$ = V_{IH}.

APPLICATION EXAMPLE



128K Byte Burstable, Secondary Cache
Using Four MCM62940AFN24s with a 33 MHz MC68040

ORDERING INFORMATION
(Order by Full Part Number)

MCM 62940A X XX

Motorola Memory Prefix — MCM

Part Number — 62940A

Speed (11 = 11 ns, 12 = 12 ns, 14 = 14 ns, 19 = 19 ns, 24 = 24 ns) — XX

Package (FN = PLCC) — X

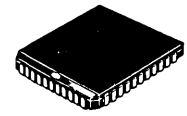
Full Part Numbers — MCM62940AFN11 MCM62940AFN12 MCM62940AFN14 MCM62940AFN19 MCM62940AFN24

MCM62940B

Advance Information

32K x 9 Bit BurstRAM™ Synchronous Static RAM

With Burst Counter and Self-Timed Write



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62940B is a 294,912 bit synchronous static random access memory designed to provide a burstable, high-performance, secondary cache for the MC68040 and PowerPC™ microprocessors. It is organized as 32,768 words of 9 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A14), data inputs (DQ0 – DQ8), and all control signals, except output enable ($\overline{G}$), are clock (K) controlled through positive-edge-triggered noninverting registers.

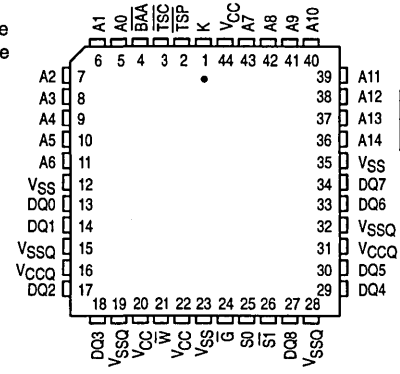
Bursts can be initiated with either transfer start processor ($\overline{TSP}$) or transfer start cache controller ($\overline{TSC}$) input pins. Subsequent burst addresses are generated internally by the MCM62940B (burst sequence imitates that of the MC68040 and PowerPC) and controlled by the burst address advance ($\overline{BAA}$) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The MCM62940B is packaged in a 44-pin plastic-leaded chip carrier (PLCC). Multiple power and ground pins have been utilized to minimize effects induced by output noise. Separate power and ground pins have been employed for DQ0 – DQ8 to allow user-controlled output levels of 5 volts or 3.3 volts.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Level Compatibility
- Fast Access Times: 11/12/14/19/24 ns Max, Cycle Times: 15/20/20/25/30 ns Min
- Internal Input Registers (Address, Data, Control)
- Internally Self-Timed Write Cycle
- $\overline{TSP}$, $\overline{TSC}$, and $\overline{BAA}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- High Output Drive Capability: 85 pF per I/O
- High Board Density PLCC Package
- Fully TTL-Compatible
- Active High and Low Chip Select Inputs for Easy Depth Expansion

PIN ASSIGNMENT



PIN NAMES

A0 – A14	Address Inputs
K	Clock
$\overline{W}$	Synchronous Write
$\overline{G}$	Output Enable
S0, $\overline{S1}$	Chip Selects
$\overline{BAA}$	Burst Address Advance
$\overline{TSP}$, $\overline{TSC}$	Transfer Start
DQ0 – DQ8	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

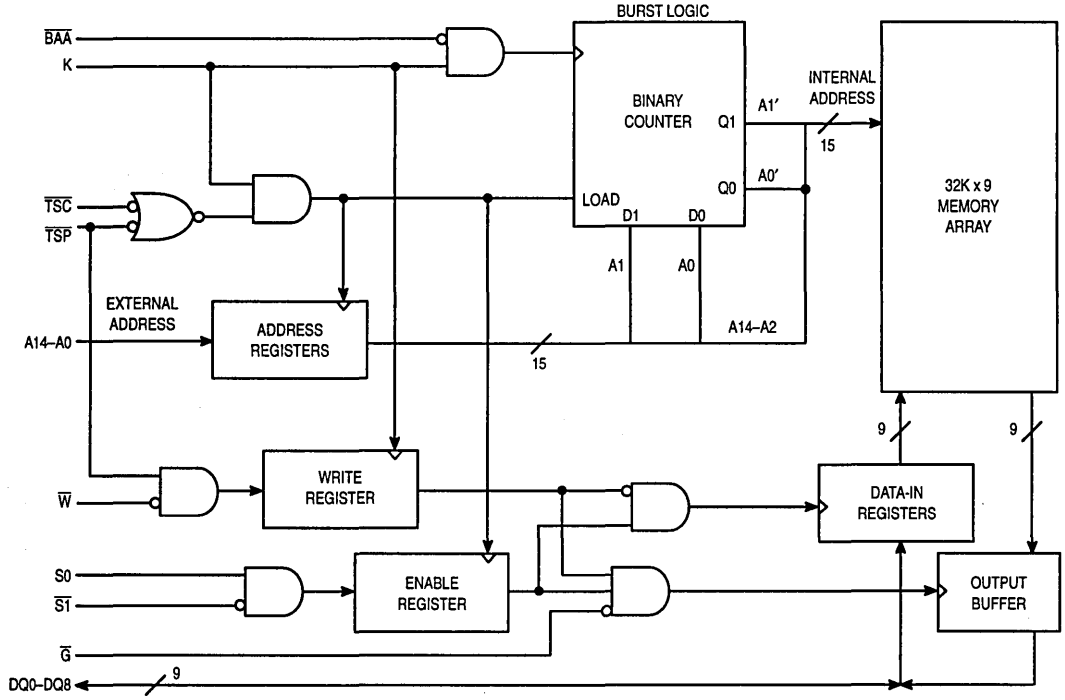
All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

4

This document contains information on a new product. Specifications and information herein are subject to change without notice.

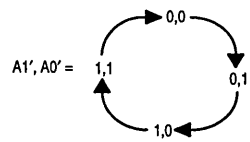
BurstRAM is a trademark of Motorola, Inc.
PowerPC is a trademark of IBM Corp.

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive-edge triggered. The $\overline{TSC}$ or $\overline{TSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{TSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{TSC}$) is performed using the new external address. When $\overline{TSC}$ is sampled low (and $\overline{TSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the next external address. Chip selects (S0, $\overline{S1}$) are sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{BAA}$ controls subsequent burst cycles. When $\overline{BAA}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{BAA}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE GRAPH**.

BURST SEQUENCE GRAPH (See Note)



NOTE: The external two values for A1 and A0 provide the starting point for the burst sequence graph. The burst logic advances A1 and A0 as shown above.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, 3, and 4)

S	$\overline{TSP}$	$\overline{TSC}$	$\overline{BAA}$	$\overline{W}$	K	Address	Operation
F	L	X	X	X	L-H	N/A	Deselected
F	X	L	X	X	L-H	N/A	Deselected
T	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
T	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
T	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. S represents S0 and $\overline{S1}$. T implies S0 = H and $\overline{S1}$ = L; F implies S0 = L or $\overline{S1}$ = H.
4. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out (DQ0–DQ8)
Read	H	High-Z
Write	X	High-Z — Data In (DQ0–DQ8)
Deselected	X	High-Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data requird setup time and held high throughout the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Output Power Supply Voltage	V_{CCQ}	– 0.5 to V_{CC}	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	 4.5 3.0	 5.0 3.3	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$, $\overline{S1}$ = V_{IH}, S0 = V_{IL}, V_{out} = 0 to V_{CCQ})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$, $\overline{S1}$ = V_{IL}, S0 = V_{IH}, All Inputs = V_{IL} = 0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min)	I_{CCA}	—	150	mA
Standby Current ($\overline{S1}$ = V_{IH}, S0 = V_{IL}, All Inputs = V_{IL} and V_{IH}, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	40	mA
CMOS Standby Current ($\overline{S1}$ ≥ V_{CC} – 0.2 V, S0 ≤ 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V, Cycle TIme ≥ t_{KHKH} min)	I_{SB2}	—	20	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible MC68040 bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ8)	C_{in}	2	3	pF
Input/Output Capacitance (DQ0 – DQ8)	$C_{I/O}$	7	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol		62940B-11		62940B-12		62940B-14		62940B-19		62940B-24		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	t_{CYC}	15	—	20	—	20	—	25	—	30	—	ns	
Clock Access Time	t_{KHQV}	t_{CD}	—	11	—	12	—	14	—	19	—	24	ns	4
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	5	—	5	—	6	—	7	—	7	ns	
Clock High to Output Active	t_{KHQX1}	t_{DC1}	6	—	6	—	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	t_{DC2}	3	—	3	—	5	—	5	—	5	—	ns	
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	0	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{OHZ}	—	6	—	6	—	6	—	7	—	7	ns	5
Clock High to Q High-Z	t_{KHQZ}	t_{CZ}	—	6	—	6	—	6	—	6	—	6	ns	5
Clock High Pulse Width	t_{KHKL}	t_{CH}	5.5	—	7	—	8	—	9	—	11	—	ns	
Clock Low Pulse Width	t_{KLKH}	t_{CL}	5.5	—	7	—	8	—	9	—	11	—	ns	
Setup Times: Address Address Status Data In Write Address Advance Chip Select	t_{AVKH} t_{TSVKH} t_{DVKH} t_{WVKH} t_{BAVKH} t_{S0VKH} t_{S1VKH}	t_{AS} t_{SS} t_{DS} t_{WS}	2	—	2	—	3	—	3	—	3	—	ns	6
Hold Times: Address Address Status Data In Write Address Advance Chip Select	t_{KHAX} t_{KHTSX} t_{KHDX} t_{KHWX} t_{KHBAX} t_{KHS0X} t_{KHS1X}	t_{AH} t_{SH} t_{DH} t_{WH}	2	—	2	—	2	—	2	—	2	—	ns	6

NOTES:
1. A read cycle is defined by $\overline{W}$ high or $\overline{TSP}$ low for the setup and hold times. A write cycle is defined by $\overline{W}$ low and $\overline{TSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{W}$ is sampled low.
4. Maximum access times are guaranteed for all possible MC68040 external bus cycles.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX1} min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of clock (K) whenever $\overline{TSP}$ or $\overline{TSC}$ are low and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is selected.Chip select must be true ($\overline{S1}$ low and S0 high) at each rising edge of clock for the device (when $\overline{TSP}$ or $\overline{TSC}$ is low) to remain enabled. Timings for $\overline{S1}$ and S0 are similar.

AC TEST LOADS

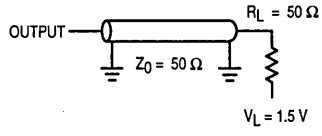


Figure 1A

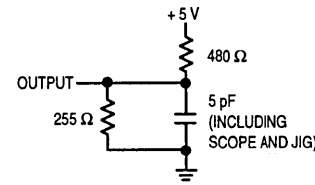
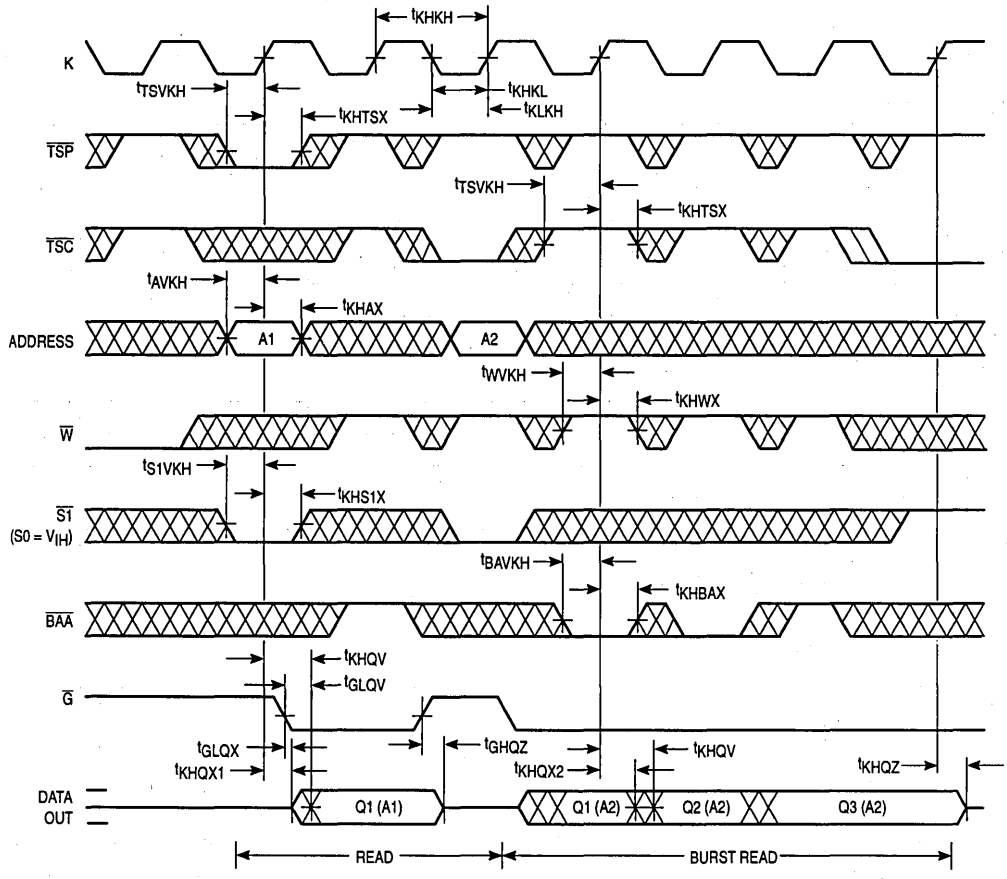


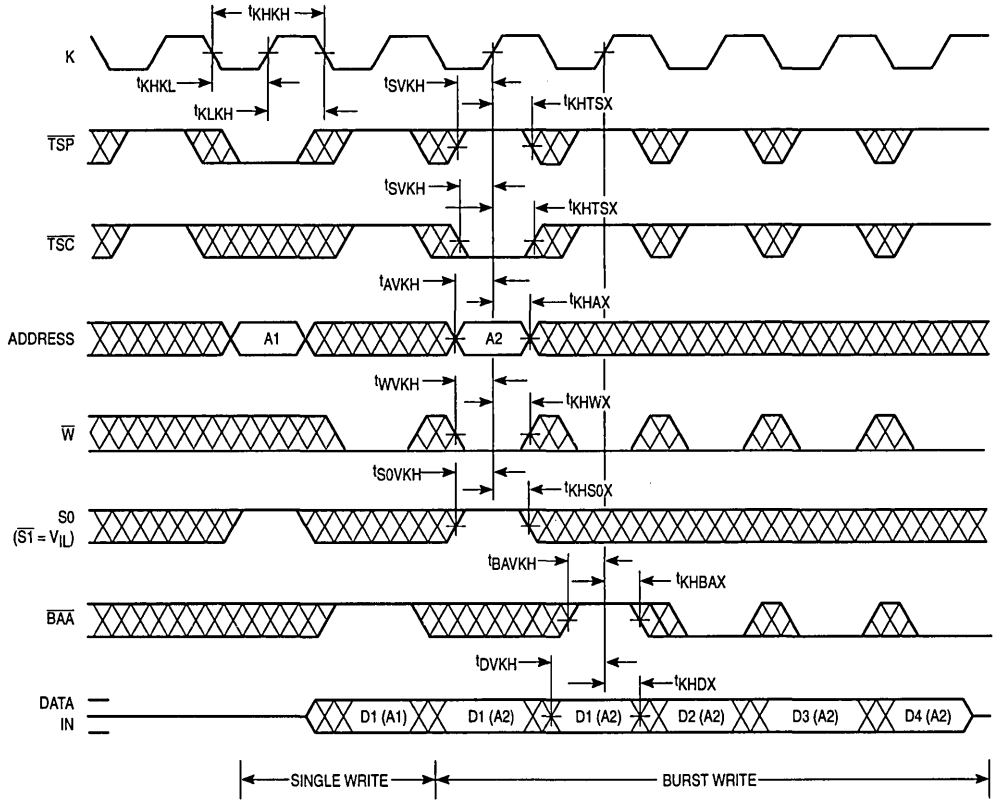
Figure 1B

READ-WRITE CYCLE



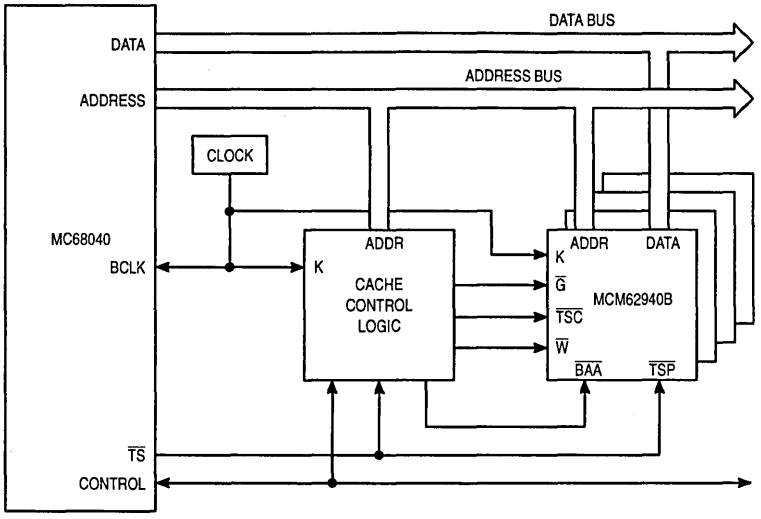
NOTE: Q1(A2) represents the first output from the external address A2; Q2(A2) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLE



NOTE: $\overline{G} = V_{IH}$.

APPLICATION EXAMPLE



128K Byte Burstable, Secondary Cache
Using Four MCM62940BFN24s with a 33 MHz MC68040

ORDERING INFORMATION
(Order by Full Part Number)

MCM 62940B X XX

Motorola Memory Prefix

Part Number

Speed (11 = 11 ns, 12 = 12 ns, 14 = 14 ns, 19 = 19 ns, 24 = 24 ns)

Package (FN = PLCC)

Full Part Numbers — MCM62940BFN11 MCM62940BFN12 MCM62940BFN14 MCM62940BFN19 MCM62940BFN24

MCM62963A

Product Preview

4K x 10 Bit Synchronous Static RAM

with Output Registers

FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62963A is a 40,960 bit synchronous static random access memory organized as 4096 words of 10 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit. This allows reduced parts count implementation of cache data RAM, writeable control store applications, and other applications that utilize long words.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A11), data (D0-D9), write ($\overline{W}$), and chip enable ($\overline{E}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

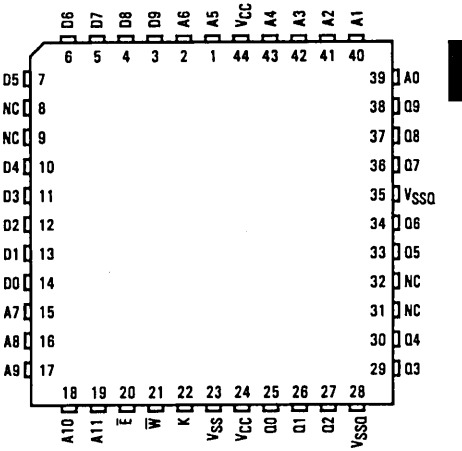
The chip enable ($\overline{E}$) input is a synchronous input clock that places the device in a low power mode when high at the rising edge of the clock (K).

The MCM62963A provides output register operation. At the rising edge of clock (K), the RAM data from the previous clock (K) high cycle is presented.

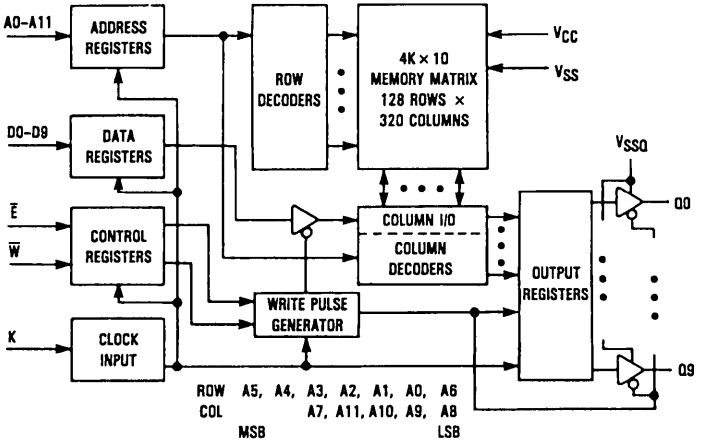
Write operations are internally self-timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 30 ns Max
- Fast Clock (K) Access Times: 13 ns Max
- Address, Data Input, $\overline{E}$, and $\overline{W}$ Registers On-Chip
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D0-D9	Data Inputs
Q0-Q9	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground
NC	No Connection

For proper operation of the device V_{SS} and both V_{SSQ} leads must be connected to ground.

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Operation	Q0-Q9	Current
L	L	Write	High Z	I_{CC}
L	H	Read	D_{out}	I_{CC}
H	X	Not Selected	High Z	I_{SB}

NOTE: The values of $\overline{E}$ and $\overline{W}$ are valid inputs for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}=5.0$ V ±10%, $T_A=0$ to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS}=V_{SSQ}=0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in}=0$ to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{E}=V_{IH}$, $V_{out}=0$ to V_{CC}, Outputs must be high-Z)	$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current ($\overline{E}=V_{IL}$, All Inputs = V_{IL} or V_{IH}, $I_{out}=0$ mA, Cycle Time ≥ t_{KHKH} min) $t_{KHKH}=30$ ns	I_{CCA}	–	140	mA
Standby Current ($\overline{E}=V_{IH}$, $V_{IH}\geq 3.0$ V, $V_{IL}\leq 0.4$ V, $I_{out}=0$ mA, Cycle Time ≥ = t_{KHKH} min)	I_{SB}	–	30	mA
Output Low Voltage ($I_{OL}=12.7$ mA)	V_{OL}	–	0.4	V
Output High Voltage ($I_{OH}=-1.8$ mA)	V_{OH}	2.8	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $T_A=25$°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	3	4	pF
Output Capacitance	C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load. . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	MCM62963A-30		Unit	Notes
		Min	Max		
Read Cycle Time	t_{KHKH}	30	—	ns	2
Clock Access Time	t_{KHQV}	—	13	ns	3
Output Active from Clock High	t_{KHQX}	3	—	ns	4
Clock High to Q High Z ($\overline{E}$ = V_{IH})	t_{KHQZ}	—	13	ns	4
Clock Low Pulse Width	t_{KLKH}	5	—	ns	
Clock High Pulse Width	t_{KHKL}	5	—	ns	
Setup Times for: $\overline{E}$	t_{EVKH}	5	—	ns	5
A	t_{AVKH}				
$\overline{W}$	t_{WHKH}				
Hold Times for: $\overline{E}$	t_{KHEX}	3	—	ns	5
A	t_{KHAX}				
$\overline{W}$	t_{KHWX}				

NOTES:
1. A read is defined by $\overline{W}$ high and $\overline{E}$ low for the setup and hold times.
2. All read cycle timing is referenced from K.
3. Valid data from K high will be the data stored at the address of the last valid read cycle.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ALL rising edges of clock (K) while the device is selected.

4

AC TEST LOADS

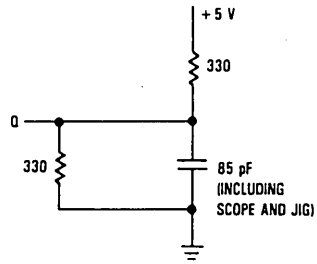


Figure 1A

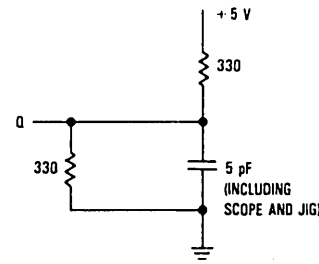
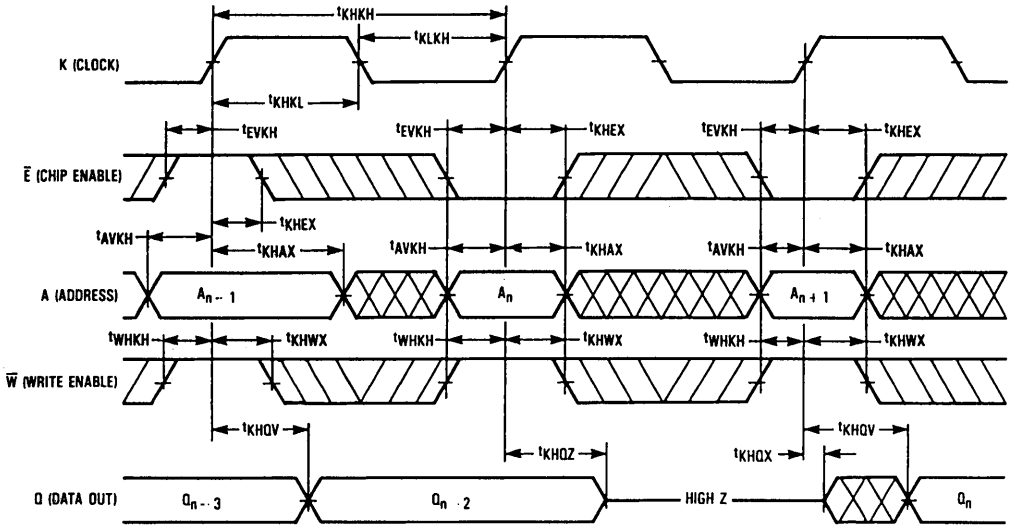
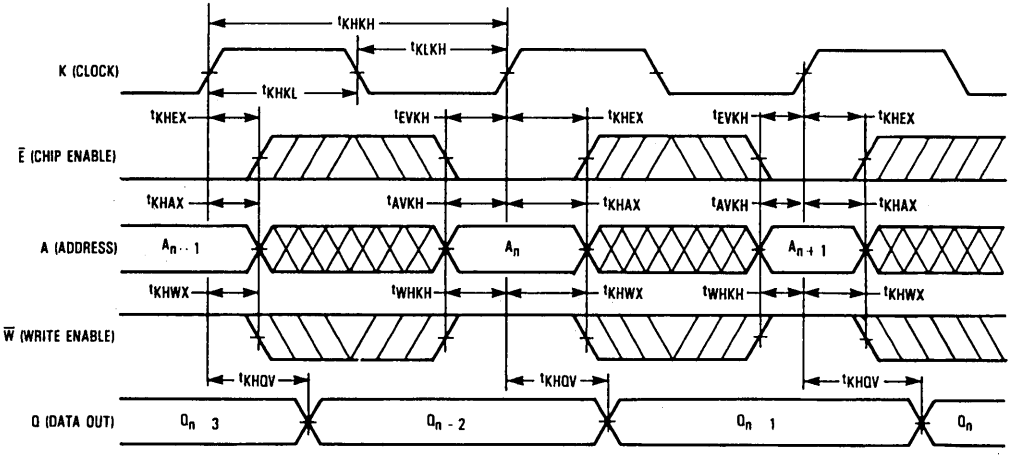


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 1)



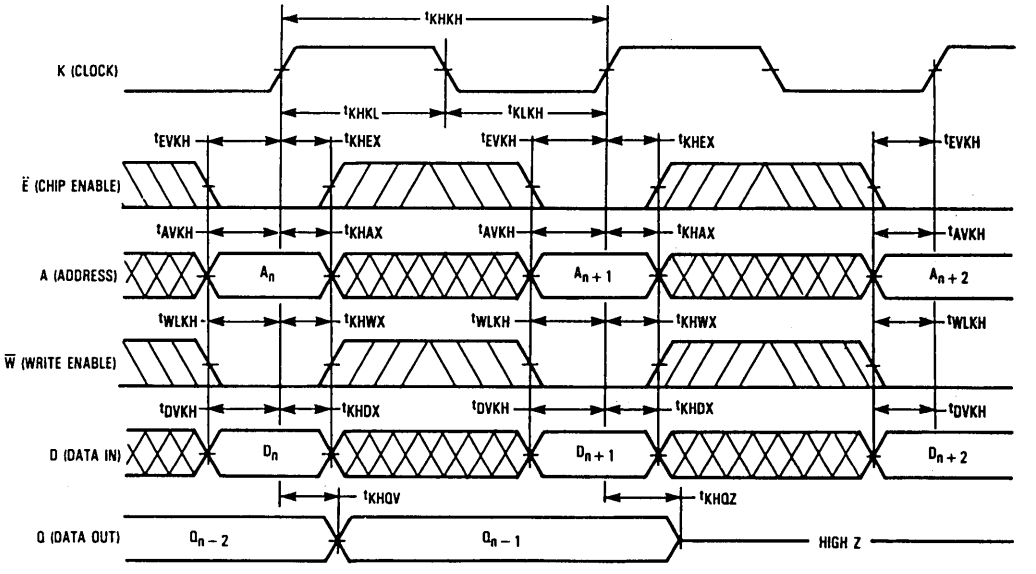
NOTE:
1. The outputs Q_{n-3} and Q_{n-2} are derived from two previous read cycles where $\overline{W} = V_{IH}$ and $\overline{E} = V_{IL}$ for those cycles.

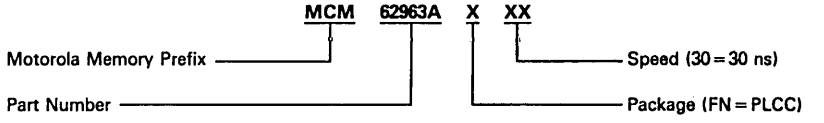
WRITE CYCLE ($\overline{W}$ Controlled, See Note 1)

Parameter		Symbol	MCM62963A-30		Unit	Notes
			Min	Max		
Write Cycle Time		t_{KHKH}	30	—	ns	2
Clock High to Q High Z ($\overline{W}=V_{IL}$)		t_{KHQZ}	—	13	ns	3
Setup Times for:	$\overline{E}$	t_{EVKH}	5	—	ns	4
	A	t_{AVKH}				
	$\overline{W}$	t_{WLKH}				
	D	t_{DVKH}				
Hold Times for:	$\overline{E}$	t_{KHEX}	3	—	ns	4
	A	t_{KHAX}				
	$\overline{W}$	t_{KHWX}				
	D	t_{KHDX}				

NOTES:
1. A write is performed when $\overline{W}$ and $\overline{E}$ are both low for the specified setup and hold times.
2. All write cycle timing is referenced from K.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
4. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ALL rising edges of clock (K) while the device is selected.

WRITE CYCLE





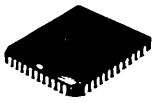
Full Part Number—MCM62963AFN30

MCM62973A

Product Preview

4K x 12 Bit Synchronous Static RAM

with Output Registers



FN PACKAGE
44-LEAD PLCC
CASE 777

The MCM62973A is a 49,152 bit synchronous static random access memory organized as 4096 words of 12 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit for reduced parts count implementation of cache data RAM, writeable control store applications, and other applications that utilize long words.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A11), data (D0-D11), write ($\overline{W}$), and chip enable ($\overline{E}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

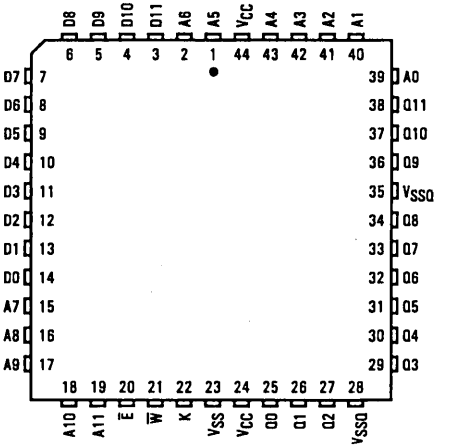
The chip enable ($\overline{E}$) input is a synchronous input clock that places the device in a low power mode when high at the rising edge of the clock (K).

The MCM62973A provides output register operation. At the rising edge of clock (K), the RAM data from the previous clock (K) high cycle is presented.

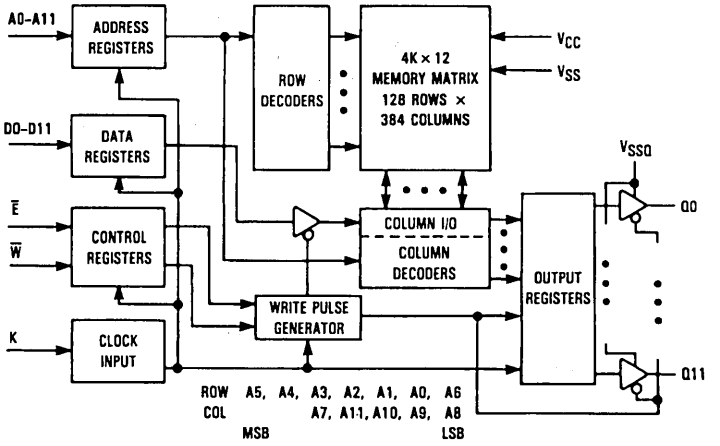
Write operations are internally self-timed and initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 18/20 ns Max
- Fast Clock (K) Access Times: 10/10 ns Max
- Address, Data Input, $\overline{E}$, and $\overline{W}$ Registers On-Chip
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D0-D11	Data Inputs
Q0-Q11	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

For proper operation of the device V_{SS} and both V_{SSQ} leads must be connected to ground.

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Operation	Q0-Q11	Current
L	L	Write	High Z	I_{CC}
L	H	Read	D_{out}	I_{CC}
H	X	Not Selected	High Z	I_{SB}

NOTE: The values of $\overline{E}$ and $\overline{W}$ are valid inputs for the setup and hold times relative to the K rising edge.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ALL rising edges of the clock (K) while the device is selected.

This device contains circuitry that will ensure the output devices are in High Z at power up. Care should be taken by the user to ensure that all clocks are at V_{IL} or V_{IH} during power up to prevent spurious read cycles from occurring.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0$ V ±10%, $T_A = 0$ to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0$ to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E} = V_{IH}$, $V_{out} = 0$ to V_{CC}, Outputs must be in High Z)	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current ($\overline{E} = V_{IL}$, All Inputs = V_{IL} or V_{IH}, $I_{out} = 0$ mA, Cycle Time ≥ t_{KHKH} min) MCM62973A-18: t_{KHKH} = 18 ns MCM62973A-20: t_{KHKH} = 20 ns	I_{CCA}	— —	170 160	mA
Standby Current ($\overline{E} = V_{IH}$, $V_{IH} \geq 3.0$ V, $V_{IL} \leq 0.4$ V, $I_{out} = 0$ mA, Cycle Time ≥ = t_{KHKH} min)	I_{SB}	—	30	mA
Output Low Voltage (I_{OL} = 12.7 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −1.8 mA)	V_{OH}	2.8	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	3	4	pF
Output Capacitance	C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter		Symbol	MCM62973-18A		MCM62973A-20		Unit	Notes
			Min	Max	Min	Max		
Read Cycle Time		t_{KHKH}	18	–	20	–	ns	2
Clock Access Time		t_{KHQV}	–	10	–	10	ns	3
Output Active from Clock High		t_{KHQX}	3	–	3	–	ns	4
Clock High to Q High Z ($\overline{E}$=V_{IH})		t_{KHQZ}	–	10	–	10	ns	4
Clock Low Pulse Width		t_{KLKH}	5	–	5	–	ns	
Clock High Pulse Width		t_{KHKL}	5	–	5	–	ns	
Setup Times for:	$\overline{E}$	t_{EVKH}	4	–	4	–	ns	5
	A	t_{AVKH}						
	$\overline{W}$	t_{WHKH}						
Hold Times for:	$\overline{E}$	t_{KHEX}	2	–	2	–	ns	5
	A	t_{KHAX}						
	$\overline{W}$	t_{KHWX}						

NOTES:
1. A read is defined by $\overline{W}$ high and $\overline{E}$ low for the setup and hold times.
2. All read cycle timing is referenced from K.
3. Valid data from K high will be the data stored at the address of the last valid read cycle.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

AC TEST LOADS

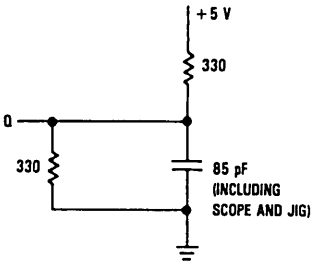


Figure 1A

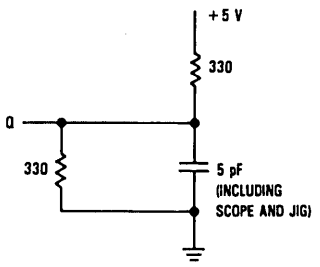
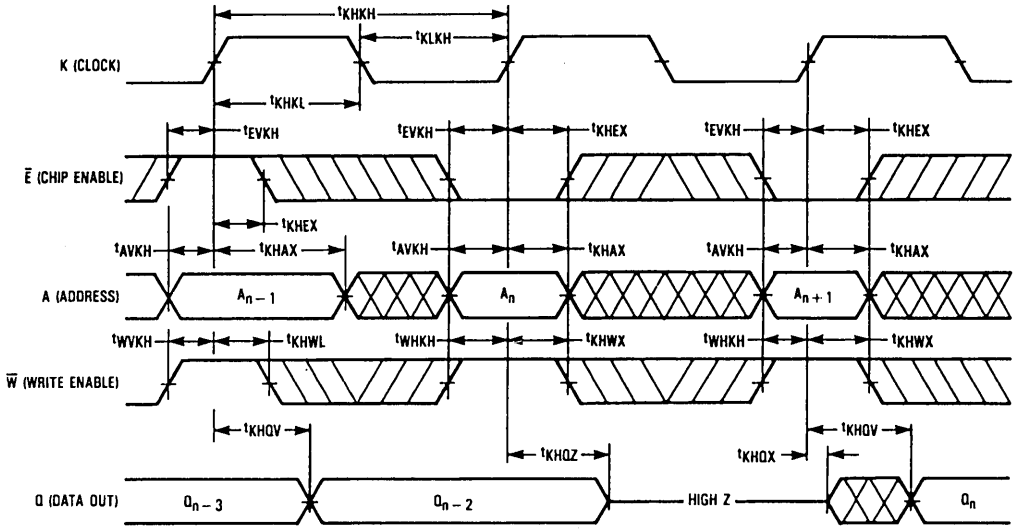
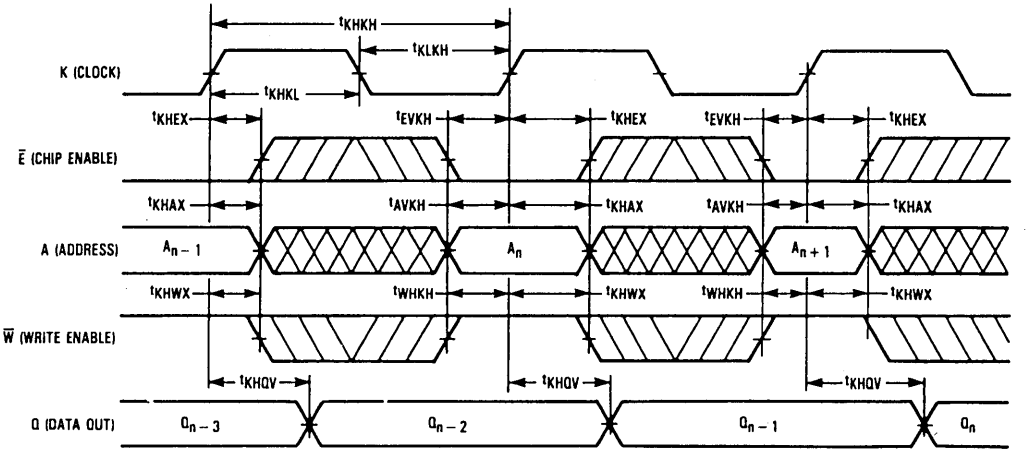


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 1)



NOTE:
1. The outputs Q_{n-3} and Q_{n-2} are derived from two previous read cycles where $\overline{W} = V_{IH}$ and $\overline{E} = V_{IL}$ for those cycles.

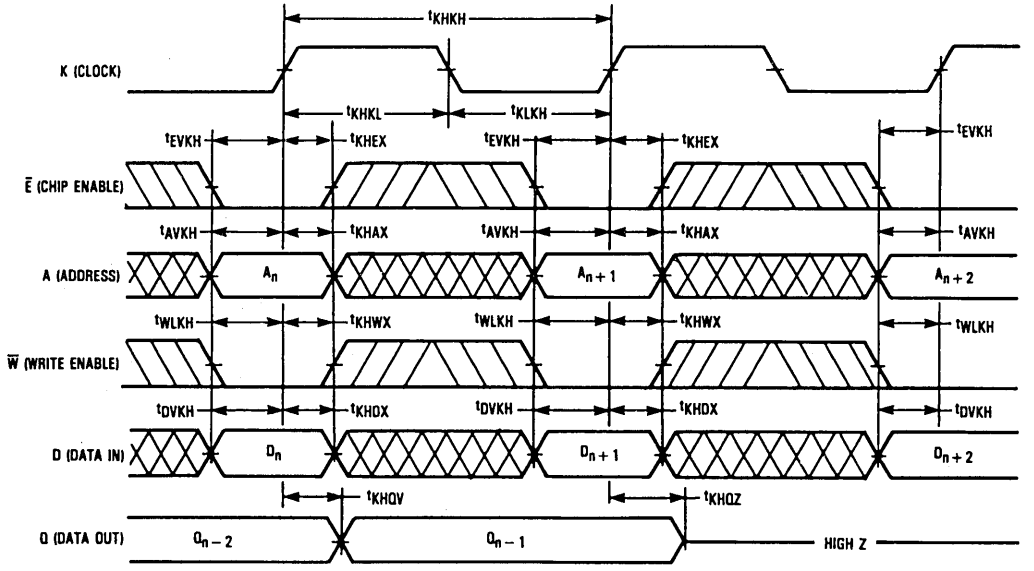
WRITE CYCLE (W Controlled, See Note 1)

Parameter		Symbol	MCM62973A-18		MCM62973A-20		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	18	–	20	–	ns	2
Clock High to Output High Z ($\overline{W}=V_{IL}$)		t_{KHQZ}	–	10	–	10	ns	3
Setup Times for:	$\overline{E}$	t_{EVKH}	4	–	4	–	ns	4
	A	t_{AVKH}						
	$\overline{W}$	t_{WLKH}						
	D	t_{DVKH}						
Hold Times for:	$\overline{E}$	t_{KHEX}	2	–	2	–	ns	4
	A	t_{KHAX}						
	$\overline{W}$	t_{KHWX}						
	D	t_{KHDX}						

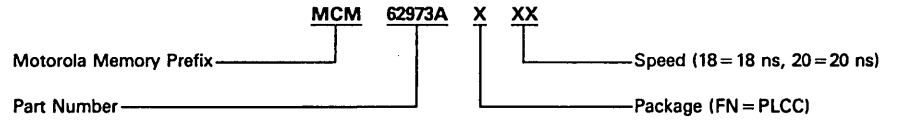
NOTES:
1. A write is performed when $\overline{W}$ and $\overline{E}$ are both low for the specified setup and hold times.
2. All write cycle timing is referenced from K.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
4. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for **ALL** rising edges of clock (K) while the device is selected.

4

WRITE CYCLE



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—MCM62973AFN18 MCM62973AFN20

MCM62980

64K x 4 Bit Fast Synchronous Static RAM

J PACKAGE
300 MIL SOJ
CASE 810B

The MCM62980 is a 262,144 bit synchronous static random access memory organized as 65,536 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 64K x 4 SRAM core with advanced peripheral circuitry consisting of positive edge triggered registers on address and synchronous write enable inputs. Asynchronous controls consist of asynchronous write strobe and output enable ($\overline{G}$). This device has increased output drive capability supported by multiple power pins.

Write cycles are differentiated from read cycles by the state of the synchronous write enable pin ($\overline{SW}$) at the rising edge of clock (K). Write cycles are completed only if asynchronous write strobe ($\overline{AW}$) is asserted within the specified setup time of the following rising edge of clock (K). Write cycles may be aborted by negating the $\overline{AW}$ signal prior to the low transition of the clock.

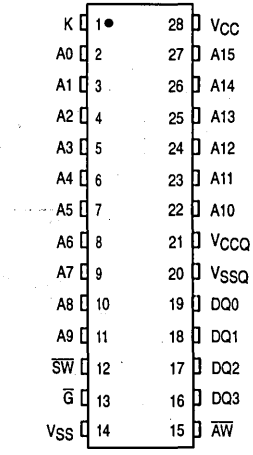
Additional power supply pins have been utilized and placed on the package for maximum performance. In addition one set of power pins is electrically isolated from the other set and supplies power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state which allows simple yet effective transmission line terminations to be achieved.

The MCM62980 will be available in a 28-pin 300 mil plastic SOJ.

Applications for this device include cache data and tag RAMs. See Figure 2 for applications information.

- Single 5 V ± 10% Power Supply
- Choice of 5.0 V or 3.3 V ± 10% Power Supplies for Output Buffers
- Fast Access and Cycle Times: 15/20 ns Max
- Fully Synchronous Operation, Single Clock Control
- Clock Timed Writes with Asynchronous Late Write Abort
- Registered Address Inputs
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three-State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 300 mil Plastic SOJ Package

PIN ASSIGNMENT



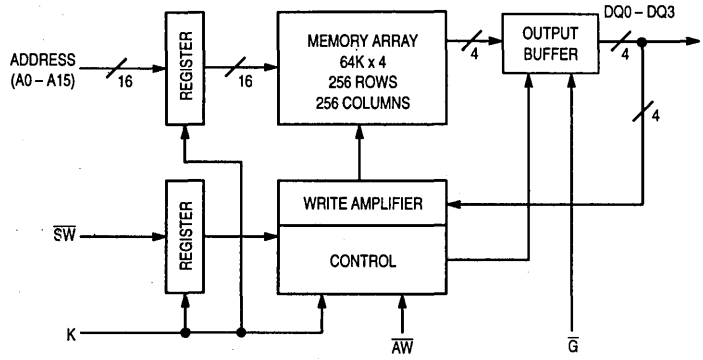
PIN NAMES

A0 – A15	Address Inputs
$\overline{AW0}$	Asynchronous Write Strobes
$\overline{SW}$	Synchronous Write Enable
K	Clock
$\overline{G}$	Output Enable
DQ0 – DQ3	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

4

BLOCK DIAGRAM



TRUTH TABLE (See Note)

$\overline{SW}$	$\overline{AW}$	$\overline{G}$	Mode	Supply Current	I/O Status
H	X	L	Read Cycle	I_{CC}	Data Out
H	X	H	Read Cycle	I_{CC}	High-Z
L	L	X	Write Cycle	I_{CC}	High-Z
L	H	X	Aborted Write Cycle	I_{CC}	High-Z

NOTE: $\overline{SW}$ and $\overline{AW}$ satisfy the specified setup and hold times for the rising edge of clock (K).

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High Z at power up.

AC TEST LOADS

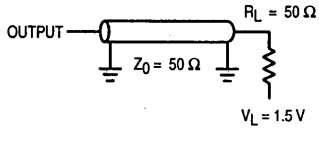


Figure 1A

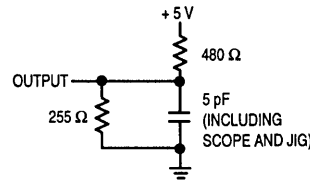


Figure 1B

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = V_{SSQ} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}*	 4.5 3.0	 5.0 3.3	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{CCQ} must be ≤ V_{CC} at all times, including power up.
**V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, All Inputs = V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Times ≥ t_{KHKH} min)	I_{CCA}	—	130	170	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ3)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0 – DQ3)	$C_{I/O}$	8	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

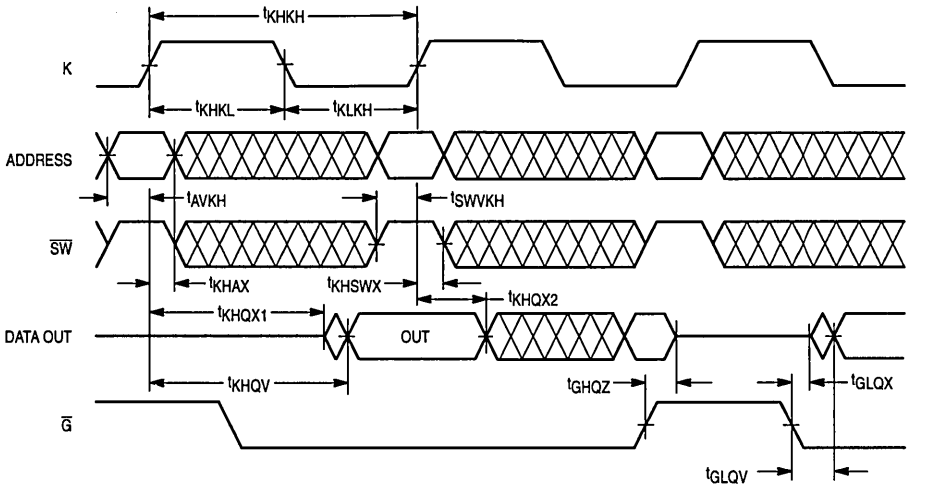
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ AND WRITE CYCLE TIMING (See Note 1)

Parameter	Symbol	MCM62980-15		MCM62980-20		Unit	Notes
		Min	Max	Min	Max		
Cycle Times:						ns	
Clock High to Clock High	t_{KHKH}	15	—	20	—		
Access Times:						ns	2
Clock High to Output Valid	t_{KHQV}	—	15	—	20		
Output Enable Low Output Valid	t_{GLQV}	—	6	—	8		
Aborted Write Cycles:						ns	
Clock Low to Asynchronous Write Strobe High	t_{KLAWH}	—	0	—	0		
Clock High to Asynchronous Write Strobe Invalid	t_{KHAWX}	2	—	2	—		
Output Buffer Control:						ns	3
Output Enable High to Output High-Z	t_{GHQZ}	2	6	2	8		
Output Enable Low to Output Low-Z	t_{GLQX}	2	—	2	—		
Reads:							
Clock High to Output Low-Z after Write	t_{KHQX1}	8	—	8	—		
Clock High to Output Invalid	t_{KHQX2}	5	—	5	—		
Writes:							
Clock High to Output High-Z after Read	t_{KHQZ}	3	8	3	10		
Clock:						ns	
Clock High Time	t_{KHKL}	4	—	4	—		
Clock Low Time	t_{KLKH}	8	—	10	—		
Setup Times:						ns	
Address Valid to Clock High	t_{AVKH}	3	—	3	—		
Synchronous Write Enable Valid to Clock High	t_{SWVKH}	3	—	3	—		
Writes:							
Data In Valid to Clock High	t_{DVKH}	5	—	6	—		
Asynchronous Write Strobe Low to Clock High	t_{AWLKH}	6	—	6	—		
Hold Times:						ns	
Clock High to Address Invalid	t_{KHAX}	2	—	2	—		
Clock High to Synchronous Write Enable Invalid	t_{KHSWX}	2	—	2	—		
Writes:							
Clock High to Data In Invalid	t_{KHDX}	0	—	0	—		
Clock High to Asynchronous Write Strobe High	t_{KHAWX}	2	—	2	—		

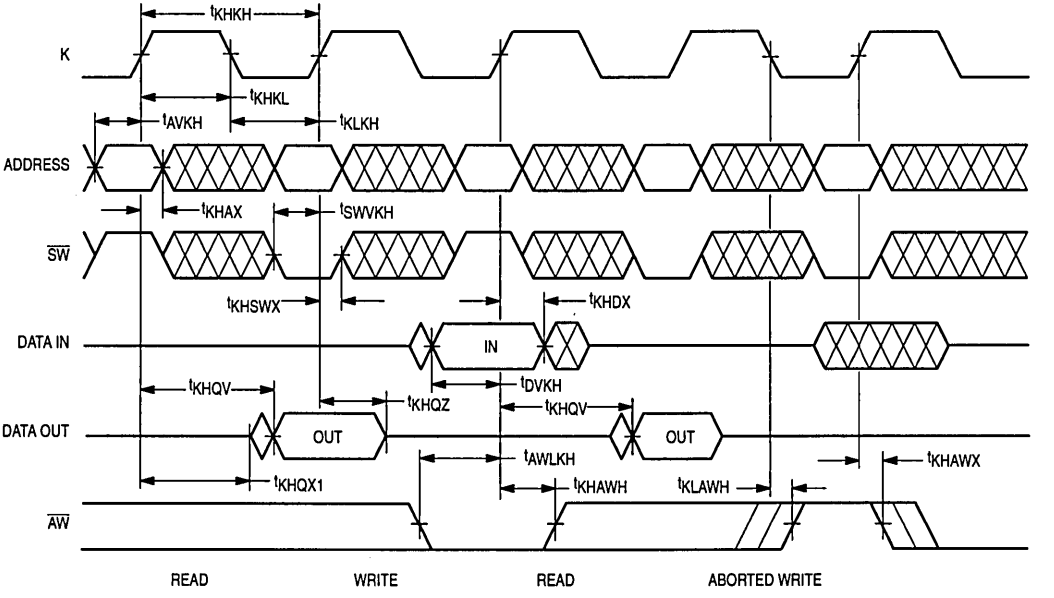
NOTES:
1. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K).
2. Into rated load of 85 pF equivalent resistive load (see Figure 1).
3. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX1} and t_{GHQZ} is less than t_{GLQX} for a given device.

READ CYCLES



4

READ — WRITE — READ CYCLES



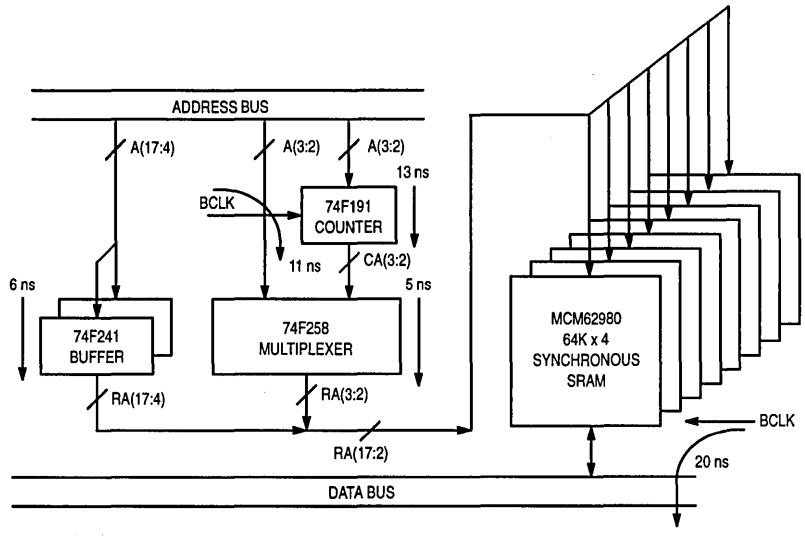


Figure 2. Burstable 64K x 32 Memory Array

ORDERING INFORMATION
(Order by Full Part Number)

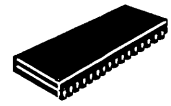
MCM 62980 X XX XX

- MCM — Motorola Memory Prefix
- 62980 — Part Number
- X — Package (J = 300 mil SOJ)
- XX — Speed (15 = 15 ns, 20 = 20 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM62980J15 MCM62980J15R2
MCM62980J20 MCM62980J20R2

MCM62981

64K x 4 Bit Fast Synchronous ParityRAM™



J PACKAGE
300 MIL SOJ
CASE 857

The MCM62981 is a 262,144 bit synchronous static random access memory organized as 65,536 words of 4 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 64K x 4 SRAM core with advanced peripheral circuitry consisting of positive edge triggered registers on address and synchronous write enable inputs. Asynchronous controls include asynchronous write strobes and output enable ($\overline{G}$).This device has increased output drive capability supported by multiple power pins. Four asynchronous write strobes ($\overline{AW0}$ – $\overline{AW3}$) are provided to allow each bit position to be written individually, thereby simplifying the task of supporting byte parity. This x4 organized SRAM is ideally suited for parity on 32-bit words.The device is functionally similar to the MCM62980 and MCM62990 with the only difference being the individual bit write capablilty.

Write cycles are differentiated from read cycles by the state of the synchronous write enable pin ($\overline{SW}$) at the rising edge of clock (K). Write cycles are completed only if the appropriate asynchronous write strobe ($\overline{AWx}$) is asserted within the specified setup time of the following rising edge of clock (K). Write cycles may be aborted by ensuring that each $\overline{AWx}$ is negated by the time the clock transitions to the low state.

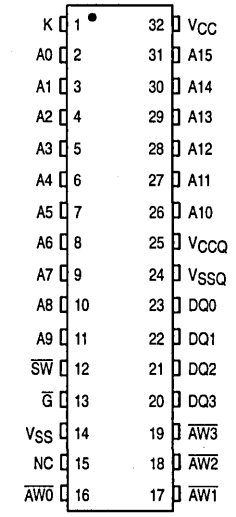
Additional power supply pins have been utilized and placed on the package for maximum performance. In addition, one set of power pins is electrically isolated from the other set and supplies power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state which allows simple yet effective transmission line terminations to be achieved.

The MCM62981 will be available in a 32-pin 300 mil plastic SOJ.

Applications for this device include parity RAMs for fast data caches.

- Single 5 V ± 10% Power Supply
- Choice of 5.0 V or 3.3 V ± 10% Power Supplies for Output Buffers
- Fast Access and Cycle Times: 15/20 ns Max
- Fully Synchronous Operation, Single Clock Control
- Clock Timed Writes with Asynchronous Late Write Abort
- Each Bit Position Individually Writeable for Simple Parity Support
- Registered Address Inputs
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three-State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time

PIN ASSIGNMENT



PIN NAMES

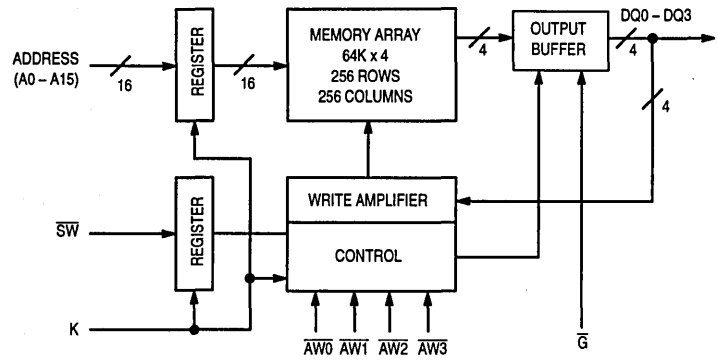
A0 – A15	Address Inputs
$\overline{AW0}$ – $\overline{AW3}$	Asynchronous Write Strobes
$\overline{SW}$	Synchronous Write Enable
K	Clock
$\overline{G}$	Output Enable
DQ0 – DQ3	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground
NC	No Connect

All power supply and ground pins must be connected for proper operation of the device.
$V_{CC} \geq V_{CCQ}$ at all times including power up.

4

ParityRAM is a trademark of Motorola Inc.

BLOCK DIAGRAM



TRUTH TABLE (See Note)

$\overline{SW}$	$\overline{AWx}$	$\overline{G}$	Mode	Supply Current	I/O Status
H	X	L	Read Cycle	I_{CC}	Data Out
H	X	H	Read Cycle	I_{CC}	High-Z
L	L	X	Write Cycle	I_{CC}	High-Z
L	H	X	Aborted Write Cycle	I_{CC}	High-Z

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High Z at power up.

AC TEST LOADS

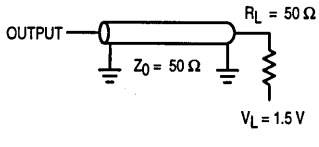


Figure 1A

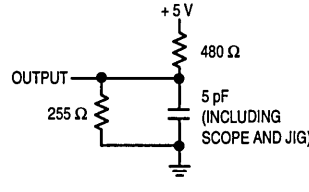


Figure 1B

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

DC OPERATING CONDITIONS AND CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	 4.5 3.0	 5.0 3.3	 5.5 3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC OPERATING CONDITIONS AND CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, All Inputs = V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Times ≥ t_{KHKH} min)	I_{CCA}	—	130	170	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ3)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0 – DQ3)	$C_{I/O}$	8	10	pF

4

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 5.0 V or 3.3 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

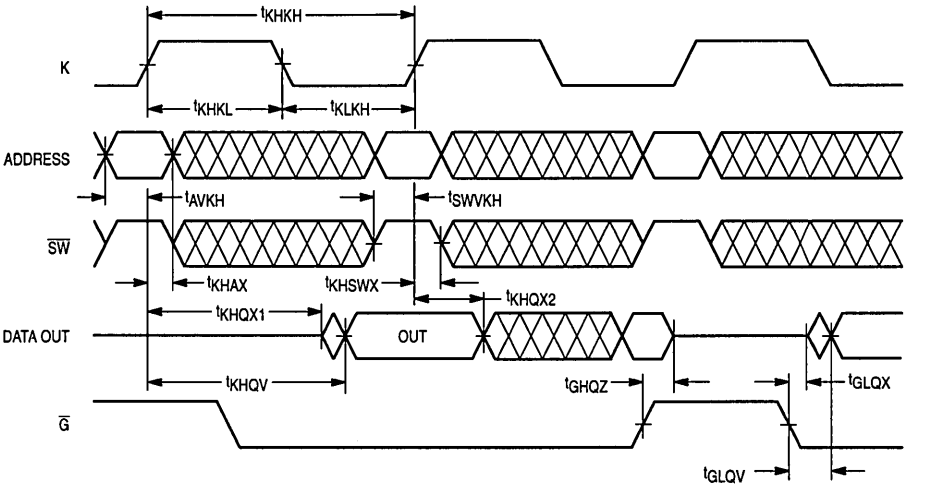
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ AND WRITE CYCLE TIMING (See Note 1)

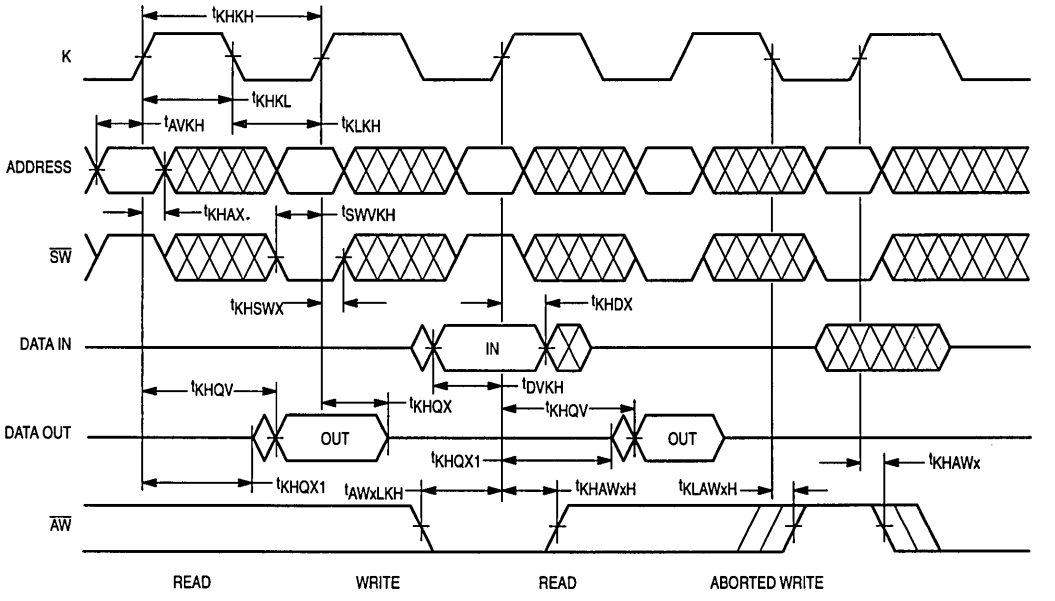
Parameter	Symbol	MCM62981-15		MCM62981-20		Unit	Notes
		Min	Max	Min	Max		
Cycle Times:						ns	
Clock High to Clock High	t_{KHKH}	15	—	20	—		
Access Times:						ns	2
Clock High to Output Valid	t_{KHQV}	—	15	—	20		
Output Enable Low Output Valid	t_{GLQV}	—	6	—	8		
Aborted Write Cycles:						ns	
Clock Low to Asynchronous Write Strobe High	t_{KLAWxH}	—	0	—	0		
Clock High to Asynchronous Write Strobe Invalid	t_{KHAWx}	2	—	2	—		
Output Buffer Control:						ns	3
Output Enable High to Output High-Z	t_{GHQZ}	2	6	2	8		
Output Enable Low to Output Low-Z	t_{GLQX}	2	—	2	—		
Reads:							
Clock High to Output Low-Z after Write	t_{KHQX1}	8	—	8	—		
Clock High to Output Invalid	t_{KHQX2}	5	—	5	—		
Writes:							
Clock High to Output High-Z after Read	t_{KHQZ}	3	8	3	10		
Clock:						ns	
Clock High Time	t_{KHKL}	4	—	4	—		
Clock Low Time	t_{KLKH}	8	—	10	—		
Setup Times:						ns	
Address Valid to Clock High	t_{AVKH}	3	—	3	—		
Synchronous Write Enable Valid to Clock High	t_{SWVKH}	3	—	3	—		
Writes:							
Data In Valid to Clock High	t_{DVKH}	5	—	6	—		
Asynchronous Write Strobe Low to Clock High	t_{AWxLK}	6	—	6	—		
Hold Times:						ns	
Clock High to Address Invalid	t_{KHAX}	2	—	2	—		
Clock High to Synchronous Write Enable Invalid	t_{KHSWX}	2	—	2	—		
Writes:							
Clock High to Data In Invalid	t_{KHDX}	0	—	0	—		
Clock High to Asynchronous Write Strobe High	t_{KHAWx}	2	—	2	—		

NOTES:
1. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K).
2. Into rated load of 85 pF equivalent resistive load (see Figure 1).
3. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX1} and t_{GHQZ} is less than t_{GLQX} for a given device.

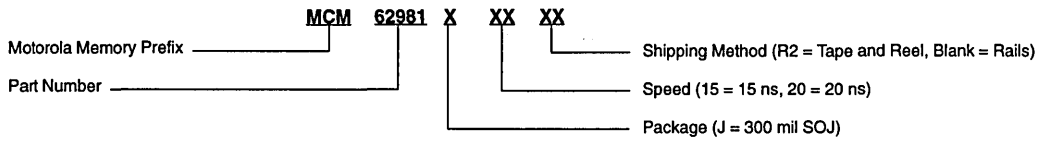
READ CYCLES



READ – WRITE – READ CYCLES



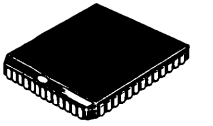
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM62981J15 MCM62981J15R2
MCM62981J20 MCM62981J20R2

MCM62990A

16K x 16 Bit Synchronous Fast Static RAM



FN PACKAGE
PLASTIC
CASE 778

The MCM62990A is a 262,144 bit synchronous static random access memory organized as 16,384 words of 16 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 16K x 16 SRAM core with advanced peripheral circuitry. Inputs to the device fall into two categories: synchronous and asynchronous. All synchronous inputs pass through positive-edge-triggered registers controlled by a single clock input (K). The synchronous inputs include all addresses, the two chip enables (SE and $\overline{SE}$), and the synchronous write enable ($\overline{SW}$).

Asynchronous inputs include the asynchronous byte write strobes ($\overline{AWL}$ and $\overline{AWH}$), output enable ($\overline{G}$), data input (DQ0 – DQ15), and the data latch enable (DL). Input data can be asynchronously latched by DL to provide simplified data-in timings during write cycles.

Address and write control are registered on-chip which greatly simplifies write cycles. Dual write strobes ($\overline{AWL}$ and $\overline{AWH}$) are provided to allow individually writeable bytes. $\overline{AWL}$ controls DQ0 – DQ7, the lower bits while $\overline{AWH}$ controls DQ8 – DQ15, the upper bits. In addition, the AWs allow late write cycles to be aborted if they are "false" during the low period of the clock. Dual chip enables (SE and $\overline{SE}$) are provided, allowing address decoding to be accomplished on-chip when the device is used in a dual bank mode.

An input data latch is provided. When data latch enable (DL) is high, the data latch is in the transparent state. When DL is low, the data latch is in the latched state. This data input latch simplifies write cycles by guaranteeing data hold time in a simple fashion.

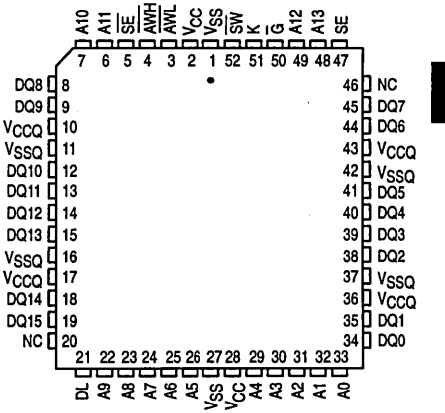
Additional power supply pins have been utilized and placed on the package for maximum performance. In addition, one set of power pins is electrically isolated from the other two and supplies power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state which allows simple yet effective transmission line terminations to be achieved.

The MCM62990A will be available in a 52 pin plastic leaded chip carrier (PLCC).

Typical applications for this device are cache memory and tag RAMs, memory in systems which are pipelined and systems which require wide data bus widths and reduced parts count.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V Power Supplies for Output Buffers
- Fast Access Times: 12/15/20/25 ns Max
- Byte Writeable via Dual Write Strobes with Abort Write Capability
- Separate Data Input Latch for Simplified Write Cycles
- Clock Controlled Registered Address, Write Control, and Dual Chip Enables
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three-State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 52 Lead PLCC Package

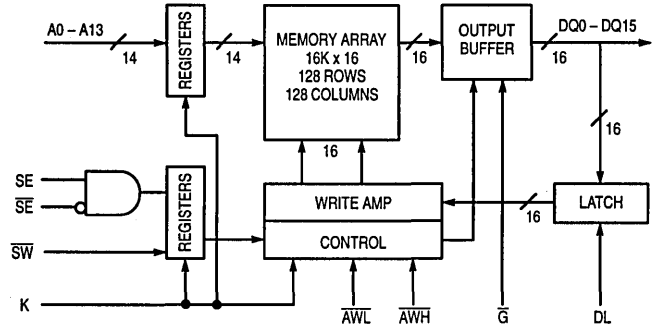
PIN ASSIGNMENT



PIN NAMES	
A0 – A13	Address Inputs
K	Clock Input
DL	Data Latch Enable
$\overline{SW}$	Synchronous Write Enable
$\overline{AWL}$	Lower Byte Async Write Strobe
$\overline{AWH}$	Upper Byte Async Write Strobe
SE	Synchronous Chip Enable
$\overline{SE}$	Synchronous Chip Enable
$\overline{G}$	Asynchronous Output Enable
DQ0 – DQ15	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

BLOCK DIAGRAM



TRUTH TABLE (See Notes)

SEs	$\overline{SW}$	$\overline{AWL}$	$\overline{AWH}$	DL	$\overline{G}$	Mode	Supply Current	I/O Status
F	X	X	X	X	X	Deselected Cycle	I_{SB}	High-Z
T	H	X	X	X	H	Read Cycle	I_{CC}	High-Z
T	H	X	X	X	L	Read Cycle	I_{CC}	Data Out
T	L	L	L	H	X	Write Cycle All Bits Transparent Data In	I_{CC}	High-Z
T	L	H	H	X	X	Aborted Write Cycle	I_{CC}	High-Z
T	L	L	H	H	X	Write Cycle Lower 8 Bits Transparent Data In	I_{CC}	High-Z
T	L	H	L	L	X	Write Cycle Upper 8 Bits Latched Data In	I_{CC}	High-Z

NOTES:
1. True (T) is SE = 1 and $\overline{SE}$ = 0.
2. Registered inputs (Addresses, $\overline{SW}$, SE, and $\overline{SE}$) satisfy the specified setup and hold times about the rising edge of clock (K). Data-in satisfies the specified setup and hold times for DL.
3. A transparent write cycle is defined by DL high during the write cycle.
4. A latched write cycle is defined by DL transitioning low during the write cycle and satisfying the specified setup and hold times.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = V_{CCQ} = 5.0$ V ± 10%, $T_A = 0$ to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}**	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible) (V_{CCQ} must be ≤ V_{CC} at all times, including power up.)	V_{CCQ}	4.5 3.0	5.0 3.3	5.5 3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)
**V_{CC} must be ≥ V_{CCQ} at all times, including power up.

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0$ to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current ($\overline{G} = V_{IH}$)	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current ($\overline{G} = V_{IH}$, $I_{out} = 0$ mA, All Inputs = V_{IL} or V_{IH}, $V_{IL} = 0$ V and $V_{IH} \geq 3.0$ V, Cycle Time ≥ t_{KHKH} min)	I_{CCA12} I_{CCA15} I_{CCA20} I_{CCA25}	— — — —	295 275 265 255	350 330 320 310	mA
Standby Current ($\overline{E} = V_{IH}$, $E = V_{IL}$, $I_{out} = 0$ mA, All Inputs = V_{IL} or V_{IH}, $V_{IL} = 0$ V and $V_{IH} \geq 3.0$ V, Cycle Time ≥ t_{KHKH} min)	I_{SB}	—	40	50	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ15)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0 – DQ15)	C_{out}	8	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, V_{CCQ} = 3.3 V or 5.0 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ AND WRITE CYCLE TIMING (See Notes 2 and 3)

Parameter	Symbol	62990A-12		62990A-15		62990A-20		62990A-25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Times										ns	
Clock High to Clock High	t_{KHKH}	15	—	15	—	20	—	25	—		
Access Times										ns	4
Clock High to Output Valid	t_{KHQV}	—	12	—	15	—	20	—	25		
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	8	—	10		
Aborted Write Cycles										ns	
Clock Low to Asynchronous Write Strobes ($\overline{AWL}$, $\overline{AWH}$) High	t_{KLAWxH}	—	0	—	0	—	0	—	0		
Clock High to $\overline{AWx}$ Invalid	t_{KHAWxL}	2	—	2	—	2	—	2	—		
Output Buffer Control										ns	
Asynchronous Output Enable ($\overline{G}$) High to Output High Z	t_{GHQZ}	2	5	2	5	2	5	2	5		1
$\overline{G}$ Low to Output Low Z	t_{GLQX}	2	—	2	—	2	—	2	—		1
Reads:											
Clock (K) High to Output Low Z After Deselect or Write	t_{KHQX1}	8	—	8	—	8	—	8	—		1
Data Out Hold After Clock High	t_{KHQX2}	5	—	5	—	5	—	5	—		5
Writes:											
K High to Output High Z After Read	t_{KHQZ}	3	10	3	10	3	10	3	10		1
Clock										ns	
Clock High Time	t_{KHKL}	4	—	4	—	4	—	4	—		
Clock Low Time	t_{KLKH}	7	—	8	—	10	—	10	—		
Setup Times										ns	
Address Valid to Clock High	t_{AVKH}	3	—	3	—	3	—	3	—		5
Synchronous Write ($\overline{SW}$) Valid to Clock High	t_{SWVKH}	3	—	3	—	3	—	3	—		5
Synchronous Enables (SE, $\overline{SE}$) Valid to Clock High	t_{SEVKH}	3	—	3	—	3	—	3	—		5
Writes:											
Data-In Valid to Clock High	t_{DVKH}	5	—	6	—	6	—	7	—		2, 5
$\overline{AWL}$, $\overline{AWH}$ Low to Clock High	t_{AWxLKH}	6	—	6	—	6	—	7	—		5
Data Latch:											
Data-In Valid to DL Low	t_{DVDLL}	2	—	2	—	2	—	2	—		3, 5
Hold Times										ns	
Clock High to Address Invalid	t_{KHAX}	2	—	2	—	2	—	2	—		5
Clock High to $\overline{SW}$ Invalid	t_{KHSWX}	3	—	3	—	3	—	3	—		5
Clock High to SE, $\overline{SE}$ Invalid	t_{KHSEX}	3	—	3	—	3	—	3	—		5
Writes:											
Clock High to Data-In Invalid	t_{KHDX}	2	—	2	—	2	—	2	—		2, 5
Clock High to $\overline{AWL}$, $\overline{AWH}$ High	t_{KHAWxH}	2	—	2	—	2	—	2	—		5
Clock High to DL High	t_{KHDLH}	2	—	2	—	2	—	2	—		3, 5
Data Latch:											
DL Low to Data-In Invalid	t_{DLLDX}	2	—	2	—	2	—	2	—		3, 5
DL High to Clock High	t_{DLHKH}	5	—	6	—	6	—	7	—		3, 5

NOTES:
1. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX} and t_{GHQZ} is less than t_{GLQX} for a given device.
2. A transparent write cycle is defined by DL high during the write cycle.
3. A latched write cycle is defined by DL transitioning low during the write cycle and satisfying the specified hold time for the rising edge of clock (K).
4. Into rated load of 85 pF equivalent resistive load (see Figure 1A).
5. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for all rising edges of clock (K) or falling edges of data latch enable (DL).

AC TEST LOADS

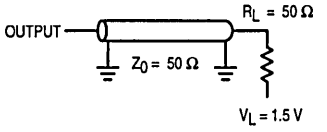


Figure 1A

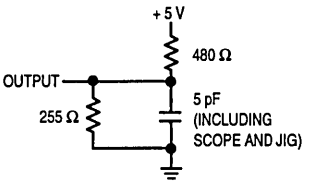
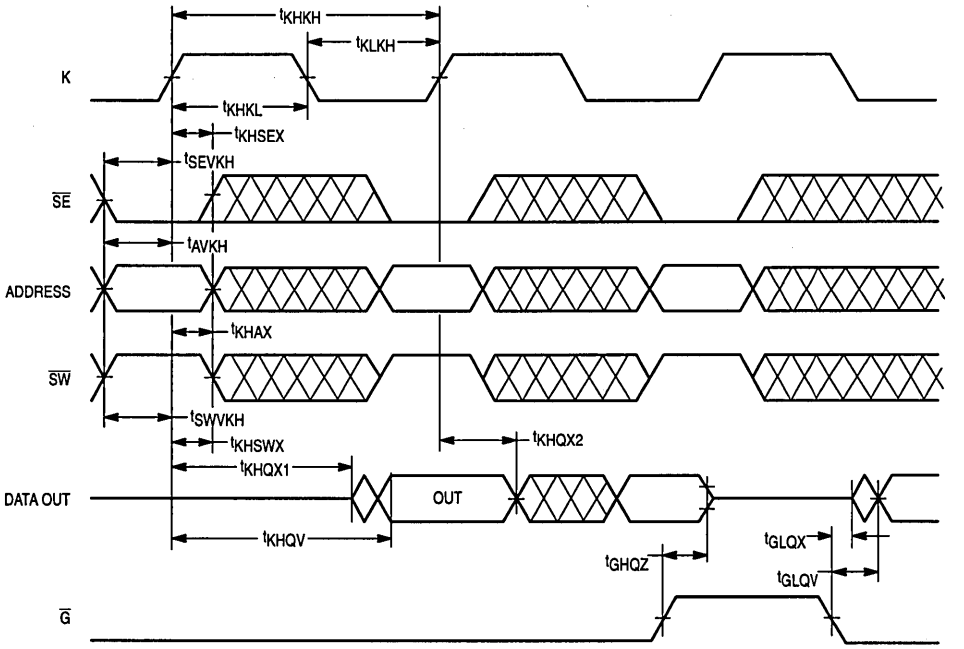


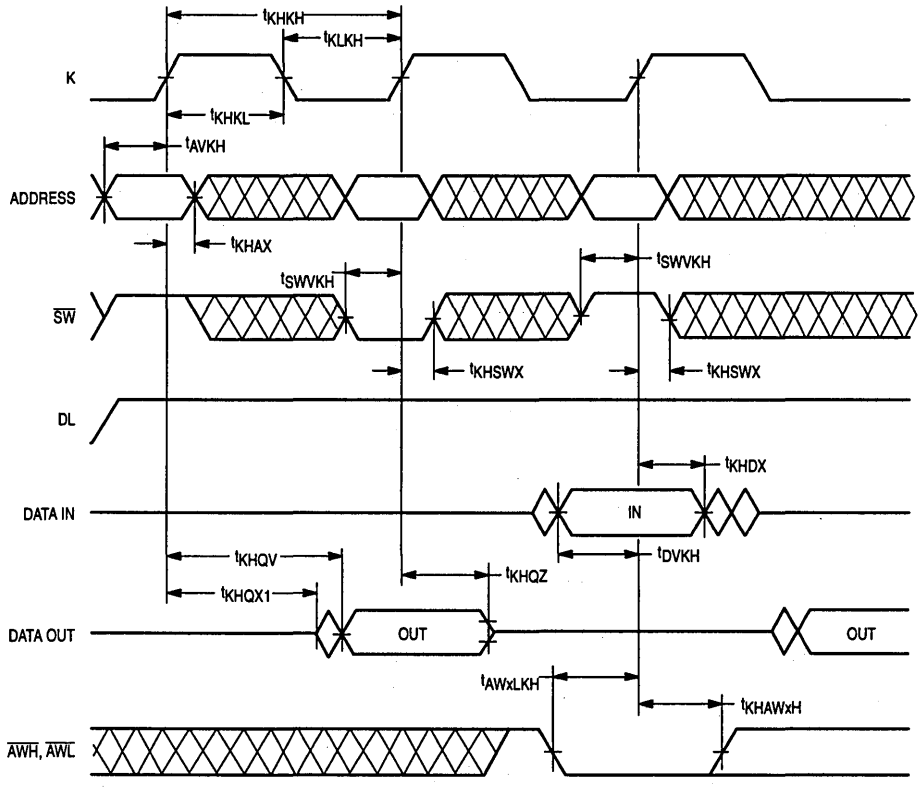
Figure 1B

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

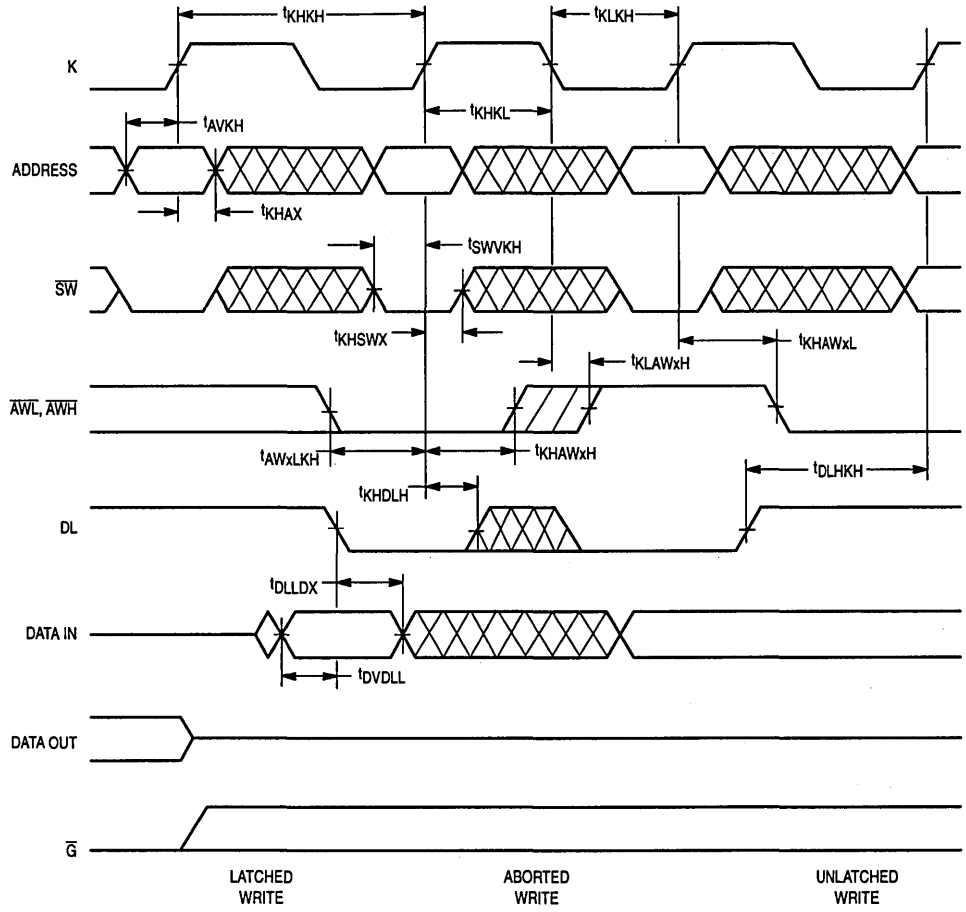
READ CYCLES



READ-UNLATCHED WRITE-READ CYCLES



WRITE CYCLES



4

ORDERING INFORMATION
(Order by Full Part Number)

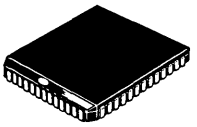
MCM 62990A FN XX

- MCM: Motorola Memory Prefix
- 62990A: Part Number
- FN: Package (FN = PLCC)
- XX: Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns, 25 = 25 ns)

Full Part Numbers — MCM62990AFN12 MCM62990AFN15 MCM62990AFN20 MCM62990AFN25

MCM62995A

16K x 16 Bit Asynchronous/Latched Address Fast Static RAM



FN PACKAGE
PLASTIC
CASE 778

The MCM62995A is a 262,144 bit latched address static random access memory organized as 16,384 words of 16 bits, fabricated using Motorola's high-performance silicon-gate CMOS technology. The device integrates a 16K x 16 SRAM core with advanced peripheral circuitry consisting of address and data input latches, active high and active low chip enables, separate upper and lower byte write strobes, and a fast output enable. This device has increased output drive capability supported by multiple power pins. In addition, the output levels can be either 3.3 V or 5 V TTL compatible by choice of the appropriate output bus power supply.

Address, data in, and chip enable latches are provided. When latch enable (LE for address and chip enables and DL for data in) is high, the address, data in, and chip enable latches are in the transparent state. If latch enable (LE, DL) is tied high, the device can be used as an asynchronous SRAM. When latch enable (LE, DL) is low, the address, data in and chip enable latches are in the latched state. This input latch simplifies read and write cycles by guaranteeing address and data-in hold time in a simple fashion.

Dual write strobes ($\overline{BWL}$ and $\overline{BWH}$) are provided to allow individually writeable bytes. $\overline{BWL}$ controls DQ0 – DQ7 (the lower bits), while $\overline{BWH}$ controls DQ8 – DQ15 (the upper bits).

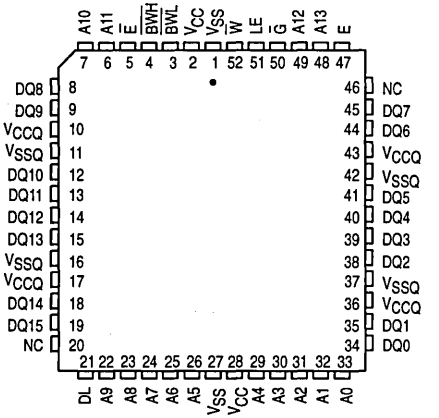
Additional power supply pins have been utilized and placed on the package for maximum performance. In addition, the output buffer power pins are electrically isolated from the other two and supply power only to the output buffers. This allows connecting the output buffers to 3.3 V instead of 5.0 V if desired. If 3.3 V output levels are chosen, the output buffer impedance in the "high" state is approximately equal to the impedance in the "low" state thereby allowing simplified transmission line terminations.

The MCM62995A is available in a 52 pin plastic leaded chip carrier (PLCC).

This device is ideally suited for systems which require wide data bus widths, cache memory and tag RAMs. See Figure 2 for applications information.

- Single 5 V ± 10% Power Supply
- Choice of 5 V or 3.3 V ± 10% Power Supplies for Output Buffers
- Fast Access Times: 12/15/20/25 ns Max
- Byte Writeable via Dual Write Strobes with Abort Write Capability
- Separate Data Input Latch for Simplified Write Cycles
- Address and Chip Enable Input Latches
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three-State Outputs
- High Output Drive Capability: 85 pF/Output at Rated Access Time
- High Board Density 52 Lead PLCC Package

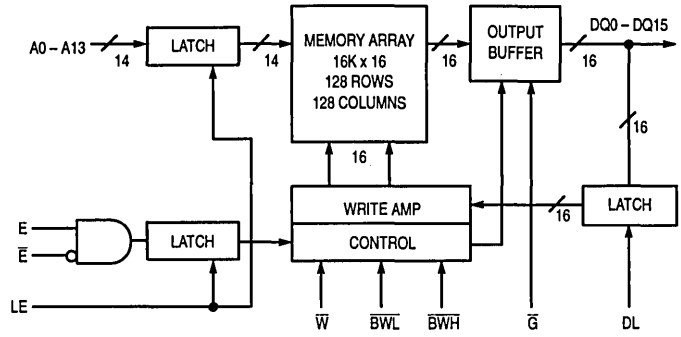
PIN ASSIGNMENT



PIN NAMES	
A0 – A13	Address Inputs
LE	Latch Enable
DL	Data Latch Enable
$\overline{W}$	Write Enable
$\overline{BWL}$	Byte Write Strobe Low
$\overline{BWH}$	Byte Write Strobe High
E	Active High Chip Enable
$\overline{E}$	Active Low Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ15	Data Input/Output
V_{CC}	+5 V Power Supply
V_{CCQ}	Output Buffer Power Supply
V_{SSQ}	Output Buffer Ground
V_{SS}	Ground
NC	No Connect

All power supply and ground pins must be connected for proper operation of the device. $V_{CC} \geq V_{CCQ}$ at all times including power up.

BLOCK DIAGRAM



TRUTH TABLE

Es	$\overline{W}$	$\overline{BWL}$	$\overline{BWH}$	LE	DL	$\overline{G}$	Mode	Supply Current	I/O Status
F	X	X	X	X	X	X	Deselected Cycle	I_{SB}	High-Z
T	H	X	X	H	X	H	Read Cycle	I_{CC}	High-Z
T	H	X	X	H	X	L	Read Cycle	I_{CC}	Data Out
T	H	X	X	L	X	L	Latched Read Cycle	I_{CC}	Data Out
T	L	L	L	H	H	X	Write Cycle All Bits	I_{CC}	High-Z
T	L	H	H	X	X	X	Aborted Write Cycle	I_{CC}	High-Z
T	L	L	H	H	H	X	Write Cycle Lower 8 Bits	I_{CC}	High-Z
T	L	H	L	H	L	X	Write Cycle Upper 8 Bits Latched Data-In	I_{CC}	High-Z
T	L	L	L	L	L	X	Latched Write Cycle Latched Data-In	I_{CC}	High-Z

NOTE: True (T) is E = 1 and $\overline{E}$ = 0. E, $\overline{E}$, and Addresses satisfy the specified setup and hold times for the falling edge of LE. Data-in satisfies the specified setup and hold times for falling edge of DL.

4

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC} and V_{CCQ}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = V_{CCQ} = 5.0$ V ± 10%, $T_A = 0$ to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Output Buffer Supply Voltage (5.0 V TTL Compatible) (3.3 V 50 Ω Compatible)	V_{CCQ}	4.5 3.0	5.0 3.3	5.5 3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0$ to V_{CC})	$I_{lkg(I)}$	—	—	± 1.0	µA
Output Leakage Current ($\overline{G} = V_{IH}$)	$I_{lkg(O)}$	—	—	± 1.0	µA
AC Supply Current ($I_{out} = 0$ mA, All Inputs = V_{IL} or V_{IH}, $V_{IL} = 0.0$ V and $V_{IH} \geq 3.0$ V, Cycle Time ≥ t_{AVAV} min)	I_{CCA12} I_{CCA15} I_{CCA20} I_{CCA25}	— — — —	295 275 265 255	350 330 320 310	mA
Standby Current ($E = V_{IL}$, $\overline{E} = V_{IH}$, $I_{out} = 0$ mA, All Inputs = V_{IL} or V_{IH}, $V_{IL} = 0$ V and $V_{IH} \geq 3.0$ V, Cycle Time ≥ t_{AVAV} min)	I_{SB}	—	40	50	mA
Output Low Voltage ($I_{OL} = + 8.0$ mA)	V_{OL}	—	—	0.4	V
Output High Voltage ($I_{OH} = – 4.0$ mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $T_A = 25$°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ15)	C_{in}	4	6	pF
Input/Output Capacitance (DQ0 – DQ15)	C_{out}	8	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, V_{CCQ} = 3.3 V or 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

ASYNCHRONOUS READ CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	62995A-12		62995A-15		62995A-20		62995A-25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	15	—	15	—	20	—	25	—	ns	5
Access Times:										ns	6
Address Valid to Output Valid	t_{AVQV}	—	12	—	15	—	20	—	25		
E, $\overline{E}$ "True" to Output Valid	t_{ETQV}	—	12	—	15	—	20	—	25		
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	8	—	10		
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	4	—	ns	
Output Buffer Control:										ns	7
E, $\overline{E}$ "True" to Output Active	t_{ETQX}	2	—	2	—	2	—	2	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "False" to Output High-Z	t_{EFQZ}	2	9	2	9	2	9	2	10		
$\overline{G}$ High to Output High-Z	t_{GHQZ}	2	5	2	6	2	8	2	10		
Power Up Time	t_{ETICCA}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. LE and DL are equal to V_{IH} for all asynchronous cycles.
2. Write Enable is equal to V_{IH} for all read cycles.
3. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
4. EF is defined by $\overline{E}$ going high or E going low.
5. All read cycle timing is referenced from the last valid address to the first transitioning address.
6. Addresses valid prior to or coincident with $\overline{E}$ going low or E going high.
7. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EFQZ} is less than t_{ETQX} and t_{GHQZ} is less than t_{GLQX} for a given device.

4

AC TEST LOADS

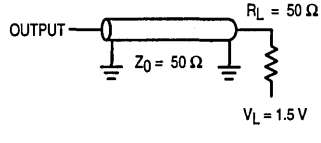


Figure 1A

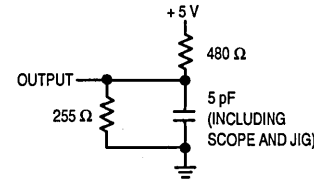
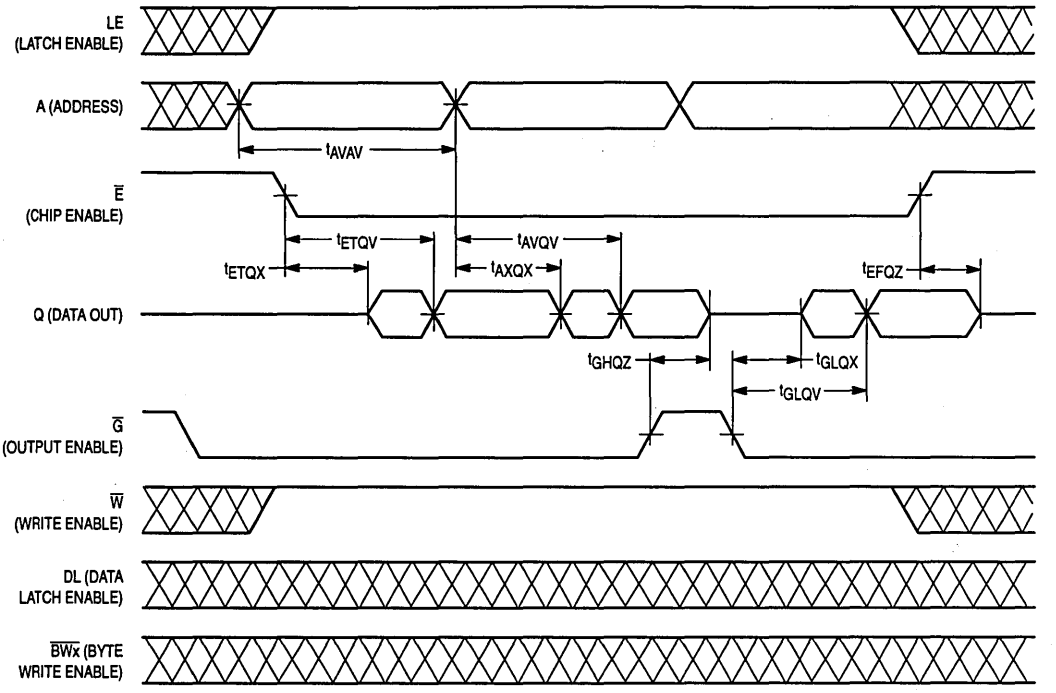


Figure 1B

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

ASYNCHRONOUS READ CYCLES



4

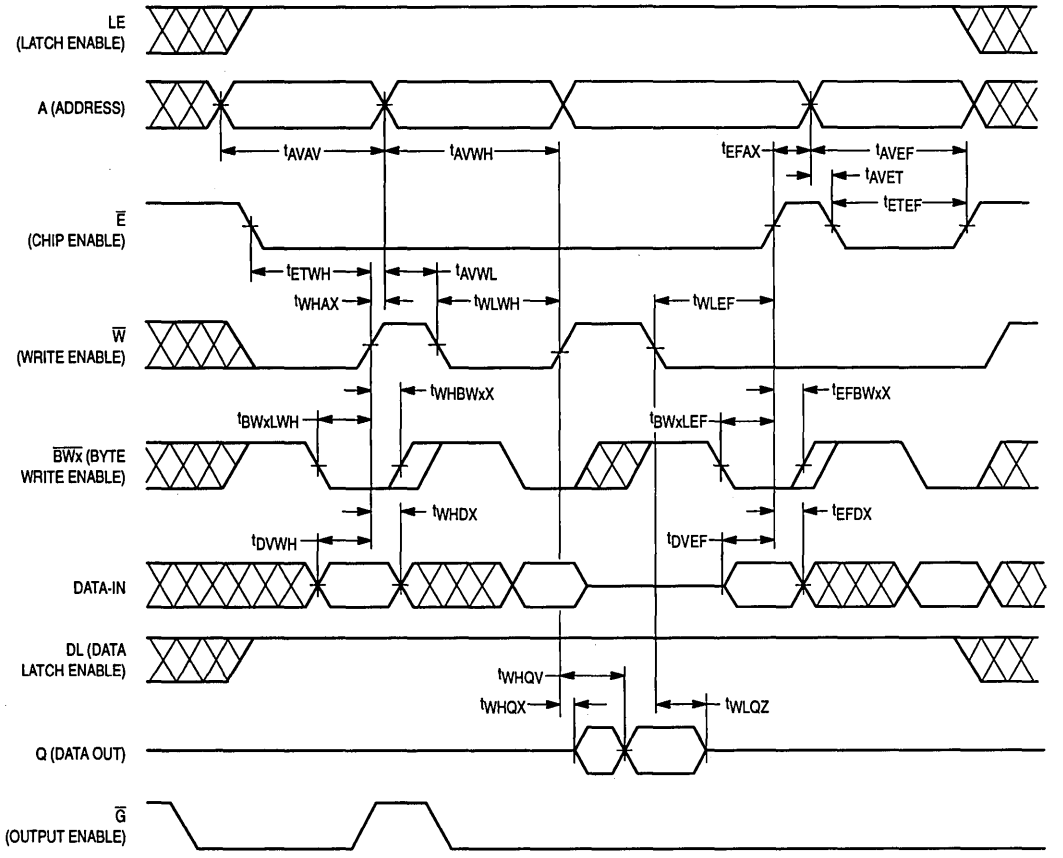
ASYNCHRONOUS WRITE CYCLE TIMING (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol	62995A-12		62995A-15		62995A-20		62995A-25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Times	t_{AVAV}	15	—	15	—	20	—	25	—	ns	6
Setup Times:										ns	
Address Valid to End of Write	t_{AVWH}	10	—	13	—	15	—	20	—		
Address Valid to E, $\overline{E}$ "False"	t_{AVEF}	10	—	13	—	15	—	20	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—	0	—		
Address Valid to E, $\overline{E}$ "True"	t_{AVET}	0	—	0	—	0	—	0	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	8	—	10	—		
Data Valid to E or $\overline{E}$ "False"	t_{DVEF}	5	—	6	—	8	—	10	—		
Byte Write Low to $\overline{W}$ High	t_{BWxLWH}	4	—	6	—	8	—	10	—		
Byte Write High to $\overline{W}$ Low (Abort)	t_{BWxHWL}	0	—	0	—	0	—	0	—		2
Byte Write Low to E, $\overline{E}$ "False"	t_{BWxLEF}	4	—	6	—	8	—	10	—		
Hold Times:										ns	
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Address Invalid	t_{EFAX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Data Invalid	t_{EFDX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Byte Write Invalid	t_{WHBWxX}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "False" to Byte Write Invalid	t_{EFBWxX}	2	—	2	—	2	—	2	—		
Write Pulse Width:										ns	
Write Pulse Width	t_{WLWH}	12	—	13	—	15	—	20	—		
Write Pulse Width	t_{WLEF}	12	—	13	—	15	—	20	—		9
Enable to End of Write	t_{ETWH}	12	—	13	—	15	—	20	—		8
Enable to End of Write	t_{ETEF}	12	—	13	—	15	—	20	—		8, 9
Output Buffer Control:										ns	
$\overline{W}$ High to Output Valid	t_{WHQV}	12	—	18	—	20	—	25	—		
$\overline{W}$ High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—		10
$\overline{W}$ High to Output High-Z	t_{WLQZ}	0	9	0	9	0	9	0	10		7, 10

NOTES:

1. LE and DL are equal to V_{IH} for all asynchronous cycles.
2. A write occurs during the overlap of ET, $\overline{W}$ low and $\overline{BWx}$ low. An aborted write occurs when $\overline{BWx}$ remains at V_{IH} while $\overline{W}$ is low.
3. Write must be equal to V_{IH} for all address transitions.
4. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
5. EF is defined by $\overline{E}$ going high or E going low.
6. All write cycle timing is referenced from the last valid address to the first transitioning address.
7. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
8. If E and $\overline{E}$ goes true coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
9. If E or $\overline{E}$ goes false coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
10. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.

ASYNCHRONOUS WRITE CYCLE



4

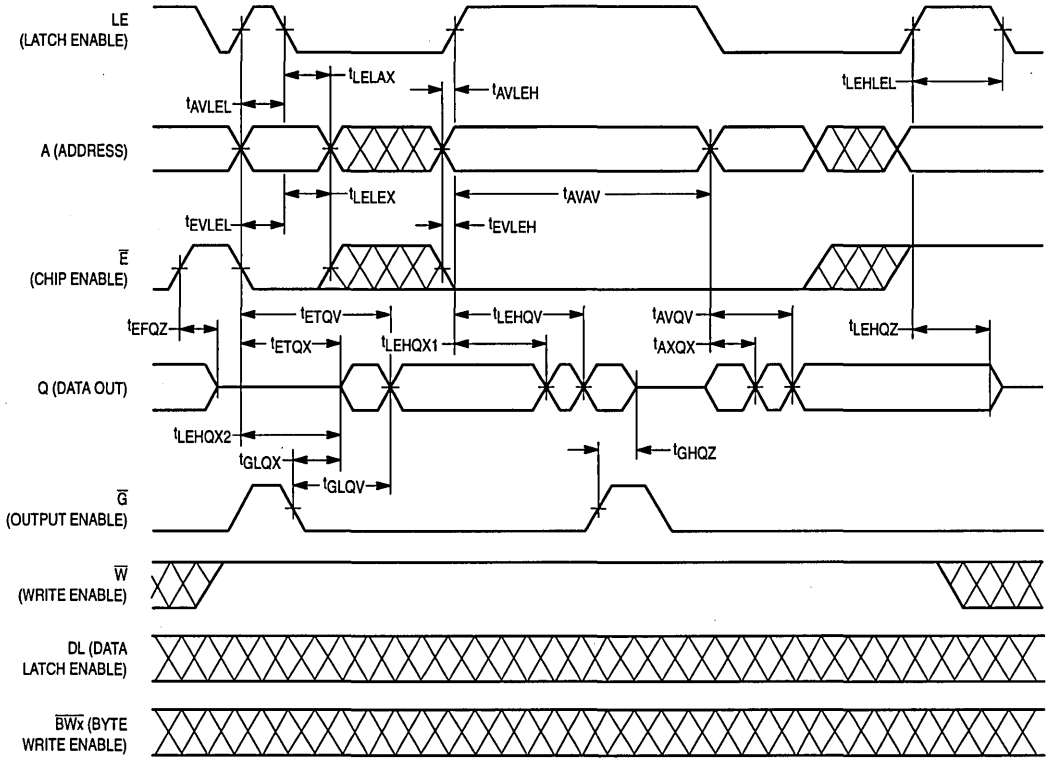
LATCHED READ CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	62995A-12		62995A-15		62995A-20		62995A-25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	15	—	15	—	20	—	25	—	ns	5
Access Times:										ns	
Address Valid to Output Valid	t_{AVQV}	—	12	—	15	—	20	—	25		
E, $\overline{E}$ "True" to Output Valid	t_{ETQV}	—	12	—	15	—	20	—	25		5
LE High to Output Valid	t_{LEHQV}	—	12	—	15	—	20	—	25		6
Output Enable Low to Output Valid	t_{GLQV}	—	5	—	6	—	8	—	10		
Setup Times:										ns	
Address Valid to LE Low	t_{AVLEL}	2	—	2	—	2	—	2	—		6
E, $\overline{E}$ "Valid" to LE Low	t_{EVLEL}	2	—	2	—	2	—	2	—		6
Address Valid to LE High	t_{AVLEH}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "Valid" to LE High	t_{EVLEH}	0	—	0	—	0	—	0	—		
Hold Times:										ns	6
LE Low to Address Invalid	t_{LELAX}	3	—	3	—	3	—	3	—		
LE Low to E, $\overline{E}$ "Invalid"	t_{LELEX}	3	—	3	—	3	—	3	—		
Output Hold:										ns	
Address Invalid to Output Invalid	t_{AXQX}	4	—	4	—	4	—	4	—		
LE High to Output Invalid	t_{LEHQX1}	4	—	4	—	4	—	4	—		
Latch Enable High Pulse Width	t_{LEHLEL}	5	—	5	—	5	—	5	—	ns	
Output Buffer Control:										ns	7
E, $\overline{E}$ "True" to Output Active	t_{ETQX}	2	—	2	—	2	—	2	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	2	—	2	—	2	—	2	—		
LE High to Output Active	t_{LEHQX2}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "False" to Output High-Z	t_{EFQZ}	2	9	2	9	2	10	2	10		
LE High to Output High-Z	t_{LEHQZ}	2	9	2	9	2	10	2	10		
$\overline{G}$ High to Output High-Z	t_{GHQZ}	2	5	2	6	2	8	2	10		

NOTES:
1. Write Enable is equal to V_{IH} for all read cycles.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
4. EF is defined by $\overline{E}$ going high or E going low.
5. Addresses valid prior to or coincident with $\overline{E}$ going low and E going high
6. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of latch enable (LE) and data latch enable (DL).
7. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EFQZ} is less than t_{ETQX} and t_{LEHQZ} is less than t_{LEHQX2} and t_{GHQZ} is less than t_{GLQX} for a given device.

4

LATCHED READ CYCLES



4

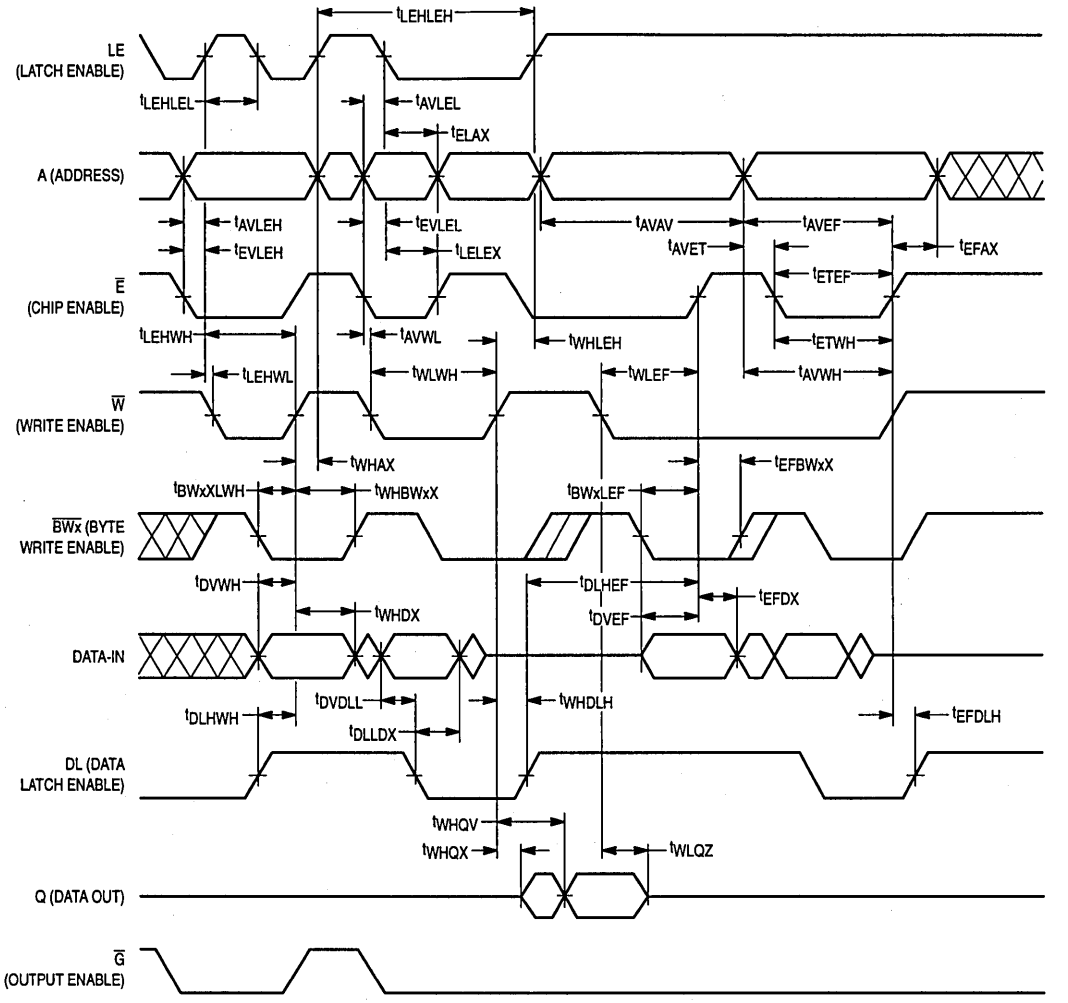
LATCHED WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	62995A-12		62995A-15		62995A-20		62995A-25		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Times:										ns	5
Address Valid to Address Valid	t_{AVAV}	15	—	15	—	20	—	25	—		
LE High to LE High	t_{LEHLEH}	15	—	15	—	20	—	25	—		
Setup Times:										ns	
Address Valid to End of Write	t_{AVWH}	10	—	13	—	15	—	20	—		
Address Valid to End of Write	t_{AVEF}	10	—	13	—	15	—	20	—		
E, $\overline{E}$ "Valid" to LE Low	t_{EVLEL}	2	—	2	—	2	—	2	—		
Address Valid to LE Low	t_{AVLEL}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "Valid" to LE High	t_{EVLEH}	0	—	0	—	0	—	0	—		
Address Valid to LE High	t_{AVLEH}	0	—	0	—	0	—	0	—		
LE High to $\overline{W}$ Low	t_{LEHWL}	0	—	0	—	0	—	0	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—	0	—		
Address Valid to E, $\overline{E}$ "True"	t_{AVET}	0	—	0	—	0	—	0	—		
Data Valid to DL Low	t_{DVDLL}	2	—	2	—	2	—	2	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	5	—	6	—	8	—	10	—		
Data Valid to E or $\overline{E}$ "False"	t_{DVEF}	5	—	6	—	8	—	10	—		
DL High to $\overline{W}$ High	t_{DLHWH}	5	—	6	—	8	—	10	—		
DL High to E, $\overline{E}$ "False"	t_{DLHEF}	5	—	6	—	8	—	10	—		
Byte Write Low to $\overline{W}$ High	t_{BWxLWH}	4	—	6	—	8	—	10	—		
Byte Write Low to E, $\overline{E}$ "False"	t_{BWxLEF}	4	—	6	—	8	—	10	—		
Byte Write High to $\overline{W}$ Low (Abort)	t_{BWxHWL}	0	—	0	—	0	—	0	—		
Hold Times:										ns	
LE Low to E, $\overline{E}$ "Invalid"	t_{LELEX}	3	—	3	—	3	—	3	—		5
LE Low to Address Invalid	t_{LELAX}	3	—	3	—	3	—	3	—		5
DL Low to Data Invalid	t_{DLLDX}	2	—	2	—	2	—	2	—		
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Address Invalid	t_{EFAX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to Data Invalid	t_{EFDX}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to DL High	t_{WHDLH}	0	—	0	—	0	—	0	—		
E, $\overline{E}$ "False" to DL High	t_{EFDLH}	0	—	0	—	0	—	0	—		
$\overline{W}$ High to Byte Write Invalid	t_{WHBWxX}	2	—	2	—	2	—	2	—		
E, $\overline{E}$ "False" to Byte Write Invalid	t_{EFBWxX}	2	—	2	—	2	—	2	—		
$\overline{W}$ High to LE High	t_{WHLEH}	0	—	0	—	0	—	0	—		
Write Pulse Width:										ns	
LE High to $\overline{W}$ High	t_{LEHWH}	12	—	13	—	15	—	20	—		6
Write Pulse Width	t_{WLWH}	12	—	13	—	15	—	20	—		
Write Pulse Width	t_{WLEF}	12	—	13	—	15	—	20	—		9
Enable to End of Write	t_{ETWH}	12	—	13	—	15	—	20	—		8
Enable to End of Write	t_{ETEF}	12	—	13	—	15	—	20	—		8, 9
Latch Enable High Pulse Width	t_{LEHLEL}	5	—	5	—	5	—	5	—	ns	
Output Buffer Control:										ns	
$\overline{W}$ High to Output Valid	t_{WHQV}	12	—	15	—	20	—	25	—		
$\overline{W}$ High to Output Active	t_{WHQX}	5	—	5	—	5	—	5	—		10
$\overline{W}$ Low to Output High-Z	t_{WLQZ}	0	9	0	9	0	9	0	10		7, 10

NOTES:

1. A write occurs during the overlap of ET, $\overline{W}$ low and $\overline{BWx}$ low. An aborted write occurs when $\overline{BWx}$ remians at V_{IH} while $\overline{W}$ is low.
2. Write must be equal to V_{IH} for all address transitions.
3. ET is defined by $\overline{E}$ going low coincident with or after E goes high, or E going high coincident with or after $\overline{E}$ goes low.
4. EF is defined by $\overline{E}$ going high or E going low.
5. All write cycle timing is referenced from the last valid address to the first transitioning address.
6. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of latch enable (LE) and data latch enable (DL).
7. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state
8. If E and $\overline{E}$ goes true coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
9. If E or $\overline{E}$ goes false coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
10. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.

LATCHED WRITE CYCLES



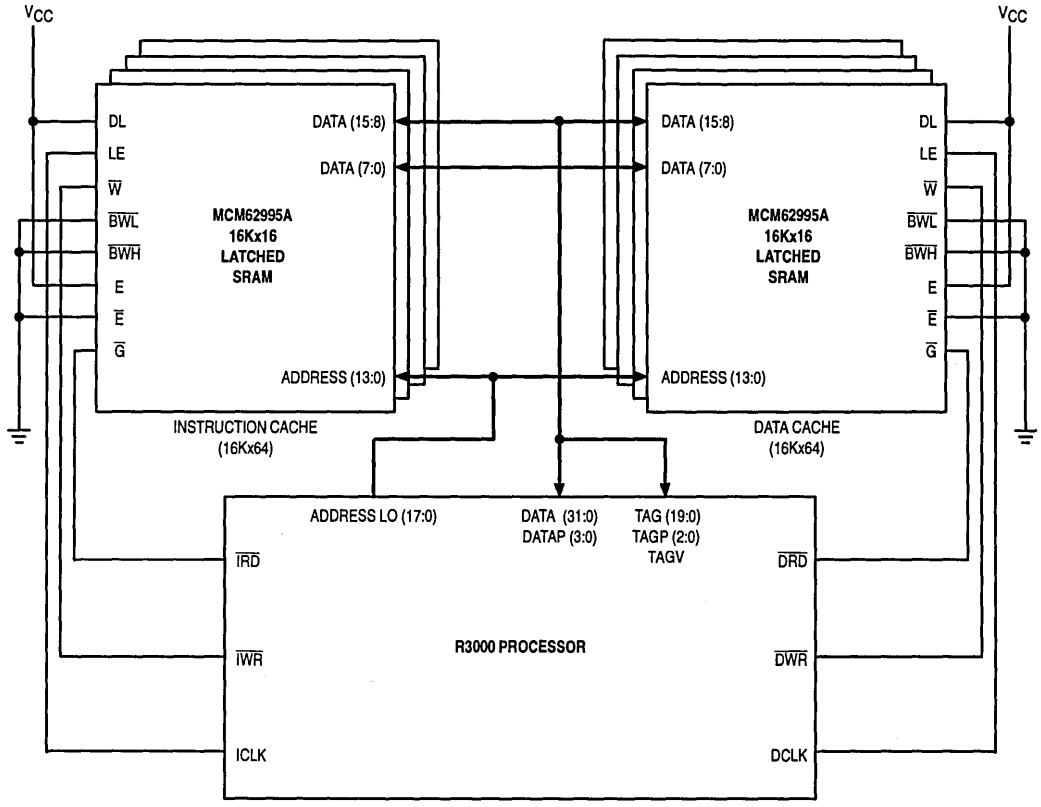


Figure 2. R3000 Application Example with 128K Byte Segregated Instruction/Data Cache Using Eight Motorola MCM62995A Latched SRAMs

4

ORDERING INFORMATION
(Order by Full Part Number)

MCM 62995A FN XX

Motorola Memory Prefix

Part Number

Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns 25 = 25 ns)

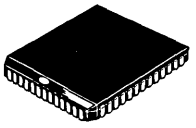
Package (FN = PLCC)

Full Part Numbers — MCM62995AFN12 MCM62995AFN15 MCM62995AFN20 MCM62995AFN25

MCM67A518

Product Preview

32K x 18 Bit Asynchronous/Latched Address Fast Static RAM



FN PACKAGE
PLASTIC
CASE 778

The MCM67A518 is a 589,824 bit latched address static random access memory organized as 32,768 words of 18 bits, fabricated with Motorola's high-performance silicon-gate BiCMOS technology. The device integrates a 32K x 18 SRAM core with advanced peripheral circuitry consisting of address and data input latches, active low chip enable, separate upper and lower byte write strobes, and a fast output enable. This device has increased output drive capability supported by multiple power pins.

Address, data in, and chip enable latches are provided. When latch enables (AL for address and chip enables and DL for data in) are high, the address, data in, and chip enable latches are in the transparent state. If latch enables are tied high, the device can be used as an asynchronous SRAM. When latch enables are low, the address, data in, and chip enable latches are in the latched state. This input latch simplifies read and write cycles by guaranteeing address and data-in hold time in a simple fashion.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits) while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

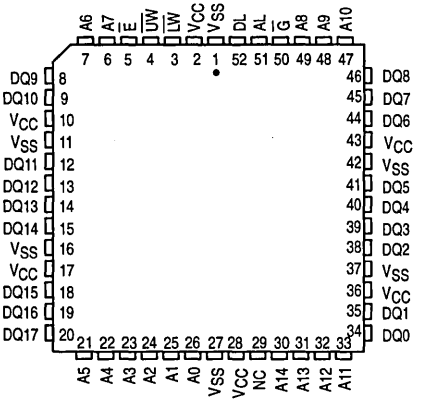
Additional power supply pins have been utilized and placed on the package for maximum performance.

The MCM67A518 will be available in a 52-pin plastic leaded chip carrier (PLCC).

This device is ideally suited for systems which require wide data bus widths, cache memory, and tag RAMs.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 12/15/20 ns Max
- Byte Writeable via Dual Write Enables
- Separate Data Input Latch for Simplified Write Cycles
- Address and Chip Enable Input Latches
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three-State Outputs
- 3.3 V I/O Compatible
- High Board Density 52-Lead PLCC Package

PIN ASSIGNMENT

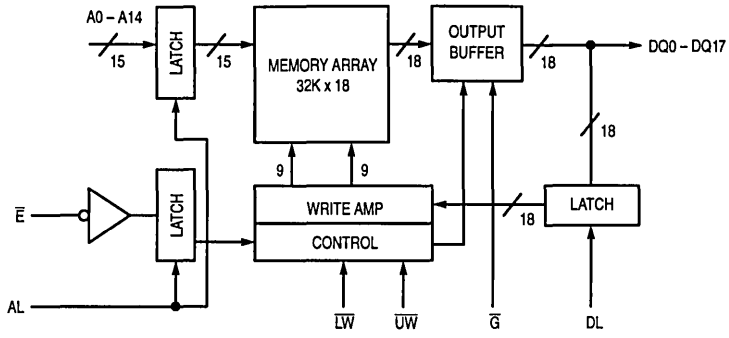


PIN NAMES	
A0 – A14	Address Inputs
AL	Address Latch
DL	Data Latch
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Higher Byte Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{LW}$	$\overline{UW}$	AL*	DL*	$\overline{G}$	Mode	Supply Current	I/O Status
H	X	X	X	X	X	Deselected Cycle	I_{SB}	High-Z
L	X	X	L	X	X	Read or Write Using Latched Addresses	I_{CC}	—
L	X	X	H	X	X	Read or Write Using Unlatched Addresses	I_{CC}	—
L	H	H	X	X	L	Read Cycle	I_{CC}	Data Out
L	H	H	X	X	H	Read Cycle	I_{CC}	High-Z
L	L	L	X	L	X	Write Both Bytes Using Latched Data In	I_{CC}	High-Z
L	L	L	X	H	X	Write Both Bytes Using Unlatched Data In	I_{CC}	High-Z
L	L	H	X	X	X	Write Cycle, Lower Byte	I_{CC}	High-Z
L	H	L	X	X	X	Write Cycle, Lower Byte	I_{CC}	High-Z

*$\overline{E}$ and Addresses satisfy the specified setup and hold times for the falling edge of AL. Data-in satisfies the specified setup and hold times for falling edge of DL.

NOTE: This truth table shows the application of each function. Combinations of these functions are valid.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0, Cycle Time ≥ t_{AVAV} min)	I_{CCA12} I_{CCA15} I_{CCA20}	—	290 275 260	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, f = f_{max})	I_{SB1}	—	75	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V, f = f_{max})	I_{SB2}	—	12	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1 Unless Otherwise Noted

ASYNCHRONOUS READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM67A518-12		MCM67A518-15		MCM67A518-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	12	—	15	—	20	—	ns	3
Access Times:								ns	4
Address Valid to Output Valid	t_{AVQV}	—	12	—	15	—	20		
$\overline{E}$ Low to Output Valid	t_{ELQV}	—	12	—	15	—	20		
Output Enable Low to Output Valid	t_{GLQV}	—	6	—	7	—	8		
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	ns	
Output Buffer Control:								ns	5
$\overline{E}$ Low to Output Active	t_{ELQX}	3	—	2	—	2	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	1	—	1	—	1	—		
$\overline{E}$ High to Output High-Z	t_{EHQZ}	2	6	2	9	2	9		
$\overline{G}$ High to Output High-Z	t_{GHQZ}	2	6	2	7	2	9		
Power Up Time	t_{ELICCA}	0	—	0	—	0	—	ns	

NOTES:
1. AL and DL are equal to V_{IH} for all asynchronous cycles.
2. Both Write Enable signals ($\overline{LW}$, $\overline{UW}$) are equal to V_{IH} for all read cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EHQZ} is less than t_{ELQX} and t_{GHQZ} is less than t_{GLQX} for a given device.

AC TEST LOADS

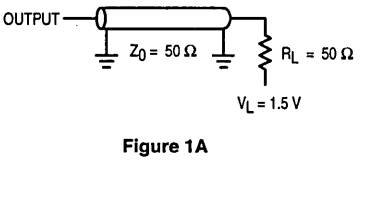


Figure 1A

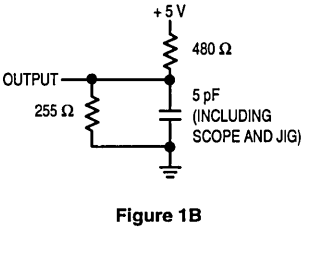
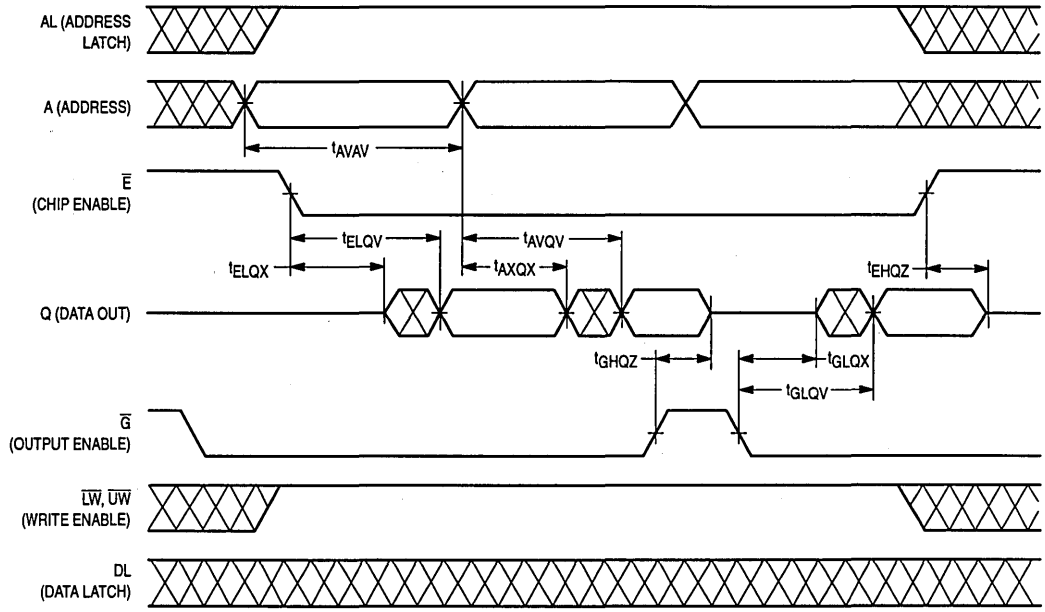


Figure 1B

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

ASYNCHRONOUS READ CYCLES



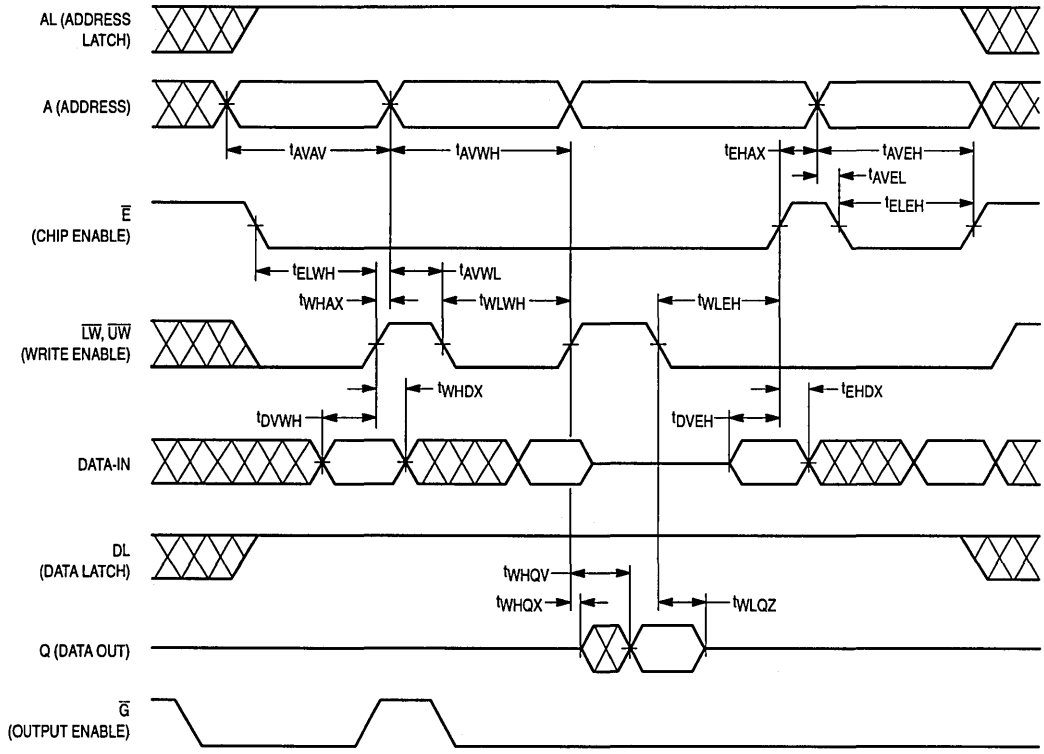
4

ASYNCHRONOUS WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67A518-12		MCM67A518-15		MCM67A518-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times	t_{AVAV}	12	—	15	—	20	—	ns	4
Setup Times:								ns	
Address Valid to End of Write	t_{AVWH}	8	—	13	—	15	—		
Address Valid to $\overline{E}$ High	t_{AVEH}	8	—	13	—	15	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—		
Address Valid to $\overline{E}$ Low	t_{AVEL}	0	—	0	—	0	—		
Address Valid to $\overline{W}$ High	t_{DVWH}	6	—	7	—	8	—		
Data Valid $\overline{E}$ High	t_{DVEH}	6	—	7	—	8	—		
Hold Times:								ns	
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—		
$\overline{E}$ High to Address Invalid	t_{EHAX}	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—		
$\overline{E}$ High to Data Invalid	t_{EHDX}	0	—	0	—	0	—		
Write Pulse Width:								ns	
Write Pulse Width ($\overline{G}$ Low)	t_{WLWH}	8	—	13	—	15	—		
Write Pulse Width ($\overline{G}$ High)	t_{WLWH}	7	—	12	—	14	—		
Write Pulse Width	t_{WLEF}	8	—	13	—	15	—		5
Enable to End of Write	t_{ELWH}	8	—	13	—	15	—		6
Enable to End of Write	t_{ELEH}	8	—	13	—	15	—		5, 6
Output Buffer Control:								ns	
$\overline{W}$ High to Output Valid	t_{WHQV}	12	—	15	—	20	—		
$\overline{W}$ High to Output Active	t_{WHQX}	3	—	5	—	5	—		7
$\overline{W}$ Low to Output High-Z	t_{WLQZ}	0	6	0	9	0	9		7, 8

NOTES:
1. $\overline{W}$ refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).
2. AL and DL are equal to V_{IH} for all asynchronous cycles.
3. Both Write Enables must be equal to V_{IH} for all address transitions.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
6. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
7. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
8. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.

ASYNCHRONOUS WRITE CYCLE

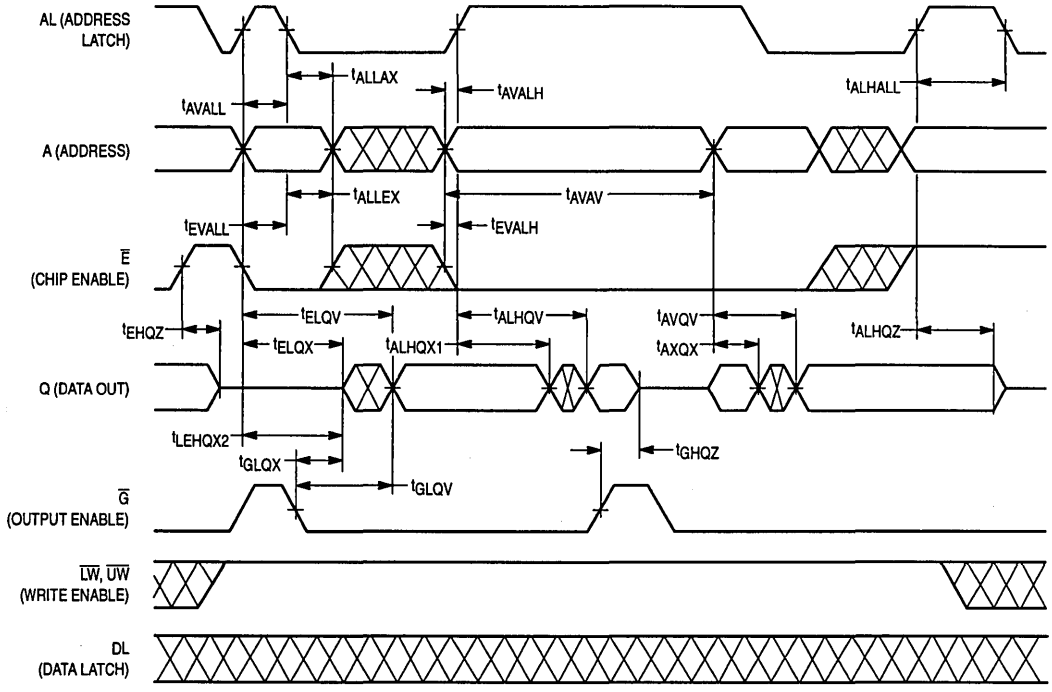


LATCHED READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM67A518-12		MCM67A518-15		MCM67A518-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	12	—	15	—	20	—	ns	3
Access Times:								ns	
Address Valid to Output Valid	t_{AVQV}	—	12	—	15	—	20		
$\overline{E}$ Low to Output Valid	t_{ELQV}	—	12	—	15	—	20		3
AL High to Output Valid	t_{ALHQV}	—	12	—	15	—	20		4
Output Enable Low to Output Valid	t_{GLQV}	—	6	—	7	—	8		
Setup Times:								ns	
Address Valid to AL Low	t_{AVALL}	2	—	2	—	2	—		4
$\overline{E}$ Valid to AL Low	t_{EVALL}	2	—	2	—	2	—		4
Address Valid to AL High	t_{AVALH}	0	—	0	—	0	—		
$\overline{E}$ Valid to AL High	t_{EVALH}	0	—	0	—	0	—		
Hold Times:								ns	4
AL Low to Address Invalid	t_{ALLAX}	2	—	3	—	3	—		
AL Low to $\overline{E}$ Invalid	t_{ALLEX}	2	—	3	—	3	—		
Output Hold:								ns	
Address Invalid to Output Invalid	t_{AXQX}	4	—	4	—	4	—		
AL High to Output Invalid	t_{ALHQX1}	4	—	4	—	4	—		
Address Latch Pulse Width	t_{ALHALL}	5	—	5	—	5	—	ns	
Output Buffer Control:								ns	5
$\overline{E}$ Low to Output Active	t_{ELQX}	3	—	2	—	2	—		
$\overline{G}$ Low to Output Active	t_{GLQZ}	1	—	1	—	1	—		
AL High to Output Active	t_{ALHQX2}	3	—	2	—	2	—		
$\overline{E}$ High to Output High-Z	t_{EHQZ}	2	6	2	9	2	10		
AL High to Output High-Z	t_{ALHQZ}	2	6	2	9	2	10		
$\overline{G}$ High to Output High-Z	t_{GHQZ}	2	6	2	7	2	8		

NOTES:
1. Both Write Enable Signals ($\overline{LW}$, $\overline{UW}$) are equal to V_{IH} for all read cycles.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of address latch (AL) and data latch (DL).
5. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EHQZ} is less than t_{ELQX} and t_{LEHQZ} is less than t_{LEHQX2} and t_{GHQZ} is less than t_{GLQX} for a given device.

LATCHED READ CYCLES

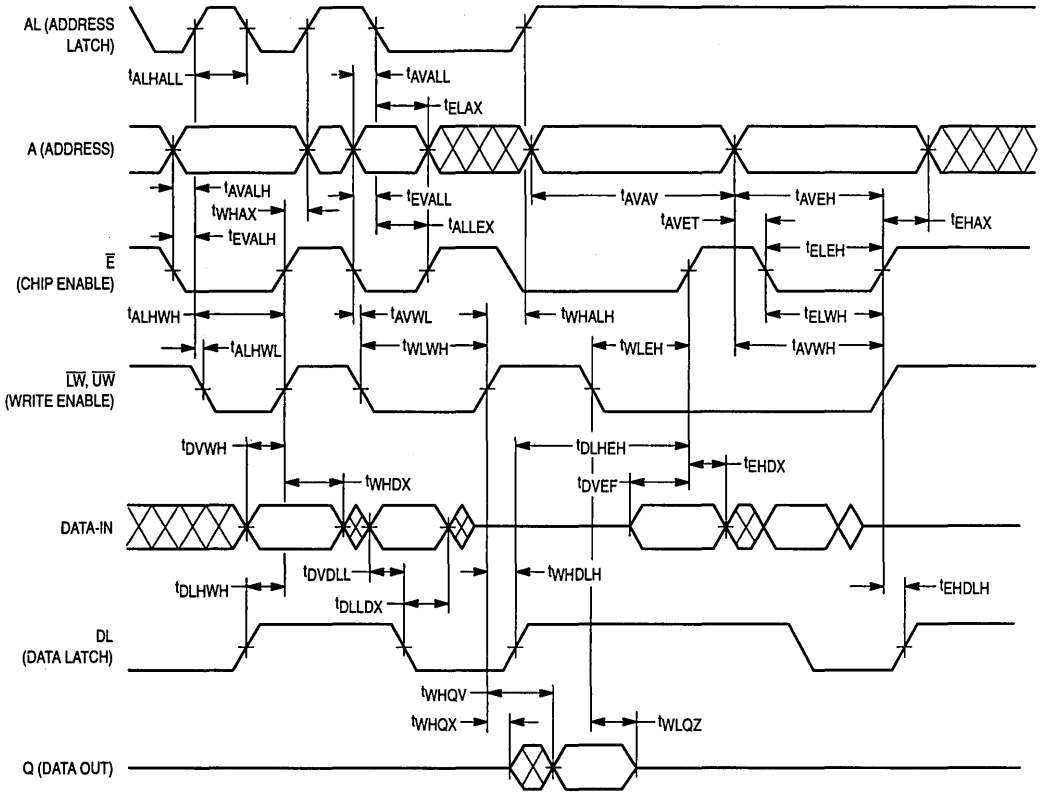


LATCHED WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67A518-12		MCM67A518-15		MCM67A518-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times: Address Valid to Address Valid	t_{AVAV}	12	—	15	—	20	—	ns	4
Setup Times:								ns	
Address Valid to End of Write	t_{AVWH}	8	—	13	—	15	—		
Address Valid to End of Write	t_{AVEH}	8	—	13	—	15	—		
$\overline{E}$ Valid to AL Low	t_{EVALL}	2	—	2	—	2	—		
Address Valid to AL Low	t_{AVALL}	2	—	2	—	2	—		
$\overline{E}$ Valid to AL High	t_{EVALH}	0	—	0	—	0	—		
Address Valid to AL High	t_{AVALH}	0	—	0	—	0	—		
AL High to $\overline{W}$ Low	t_{ALHWL}	0	—	0	—	0	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—		
Address Valid to $\overline{E}$ Low	t_{AVEL}	0	—	0	—	0	—		
Data Valid to DL Low	t_{DVDLL}	2	—	2	—	2	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	6	—	7	—	8	—		
Data Valid to $\overline{E}$ High	t_{DVEH}	6	—	7	—	8	—		
DL High to $\overline{W}$ High	t_{DLHWH}	6	—	7	—	8	—		
DL High to $\overline{E}$ High	t_{DLHEH}	6	—	7	—	8	—		
Hold Times:								ns	
AL Low to $\overline{E}$ Invalid	t_{ALLEX}	2	—	3	—	3	—		4
AL Low to Address Invalid	t_{ALLAX}	2	—	3	—	3	—		4
DL Low to Data Invalid	t_{DLLDX}	2	—	3	—	3	—		
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—		
$\overline{E}$ High to Address Invalid	t_{EHAX}	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—		
$\overline{E}$ High to Data Invalid	t_{EHDX}	0	—	0	—	0	—		
$\overline{W}$ High to DL High	t_{WHDLH}	0	—	0	—	0	—		
$\overline{E}$ High to DL High	t_{EFDLH}	0	—	0	—	0	—		
$\overline{W}$ High to AL High	t_{WHALH}	0	—	0	—	0	—		
Write Pulse Width:								ns	
AL High to $\overline{W}$ High	t_{ALHWH}	8	—	13	—	15	—		5
Write Pulse Width ($\overline{G}$ Low)	t_{WLWH}	8	—	13	—	15	—		
Write Pulse Width ($\overline{G}$ High)	t_{WLWH}	7	—	12	—	14	—		
Write Pulse Width	t_{WLEH}	8	—	13	—	15	—		6
Enable to End of Write	t_{ELWH}	8	—	13	—	15	—		7
Enable to End of Write	t_{ELEH}	8	—	13	—	15	—		6, 7
Address Latch Pulse Width	t_{ALHALL}	12	—	15	—	20	—	ns	4
Output Buffer Control:								ns	
$\overline{W}$ High to Output Valid	t_{WHQV}	12	—	15	—	20	—		
$\overline{W}$ High to Output Active	t_{WHQX}	3	—	5	—	5	—		8
$\overline{W}$ Low to Output High-Z	t_{WLQZ}	0	6	0	9	0	9		8, 9

NOTES:
1. $\overline{W}$ refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).
2. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
3. Both Write Enables must be equal to V_{IH} for all address transitions.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of address latch (AL) and data latch (DL).
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
7. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
8. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
9. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.

LATCHED WRITE CYCLES



ORDERING INFORMATION
(Order by Full Part Number)

MCM 67A518 X XX

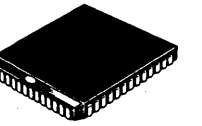
- MCM — Motorola Memory Prefix
- 67A518 — Part Number
- X — Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns)
- XX — Package (FN = PLCC)

Full Part Numbers — MCM67A518FN12 MCM67A518FN15 MCM67A518FN20

MCM67B518

Product Preview

32K x 18 Bit BurstRAM™ Synchronous Fast Static RAM
With Burst Counter and Self-Timed Write



FN PACKAGE
PLASTIC
CASE 778

The MCM67B518 is a 589,824 bit synchronous fast static random access memory designed to provide a burstable, high-performance, secondary cache for the i486™ and Pentium™ microprocessors. It is organized as 32,768 words of 18 bits, fabricated with Motorola's high-performance silicon-gate BiCMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A14), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive-edge-triggered noninverting registers.

Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67B518 (burst sequence imitates that of the i486 and Pentium) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

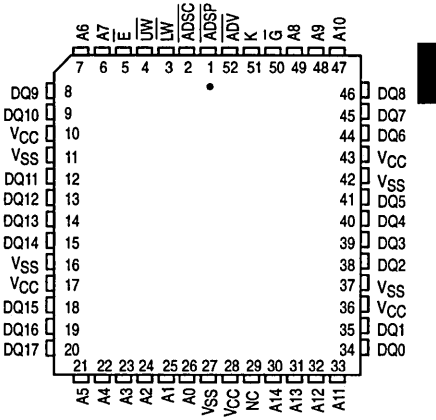
Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 9/12/18 ns Max
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Internally Self-Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52-Lead PLCC Package

PIN ASSIGNMENT



PIN NAMES	
A0 – A14	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

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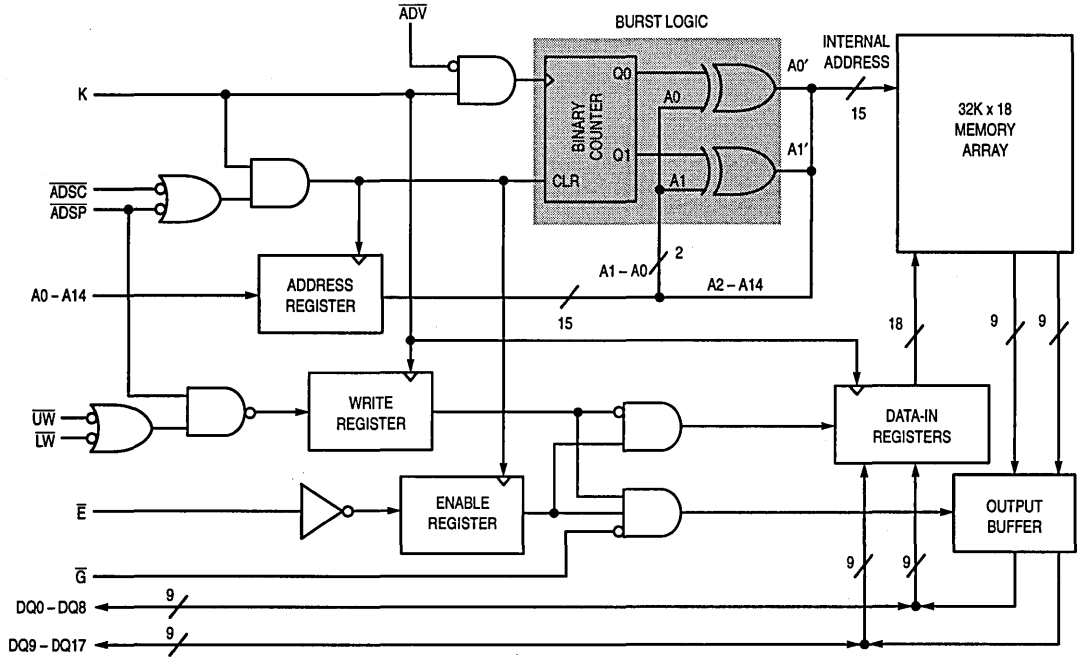
i486 and Pentium are trademarks of Intel Corp.

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive-edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A14 – A2	A1	A0
1st Burst Address	A14 – A2	A1	$\overline{A0}$
2nd Burst Address	A14 – A2	$\overline{A1}$	A0
3rd Burst Address	A14 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	L	X	X	X	L-H	N/A	Deselected
H	X	L	X	X	L-H	N/A	Deselected
L	L	X	X	X	L-H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High-Z
Write	X	High-Z — Data In
Deselected	X	High-Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	− 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{bias}	− 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA9} I_{CCA12} I_{CCA18}	—	275 250 225	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	75	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3) ($\overline{W}$ refers to either or both byte write enables)

Parameter	Symbol		MCM67B518-9		MCM67B518-12		MCM67B518-18		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	t_{CYC}	15	—	20	—	30	—	ns	
Clock Access Time	t_{KHQV}	t_{CD}	—	9	—	12	—	18	ns	4
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	5	—	6	—	7	ns	
Clock High to Output Active	t_{KHQX1}	t_{DC1}	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	t_{DC2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{OHZ}	2	6	2	7	2	7	ns	5
Clock High to Q High-Z	t_{KHQZ}	t_{CZ}	—	6	—	6	—	6	ns	
Clock High Pulse Width	t_{KHKL}	t_{CH}	5	—	6	—	7	—	ns	
Clock Low Pulse Width	t_{KLKH}	t_{CL}	5	—	6	—	7	—	ns	
Setup Times: Address	t_{AVKH}	t_{AS}	2.5	—	2.5	—	3.0	—	ns	6
Address Status	t_{ADSVKH}	t_{SS}								
Data In	t_{DVKH}	t_{DS}								
Write	t_{WVKH}	t_{WS}								
Address Advance	t_{ADVVKH}									
Chip Enable	t_{EVKH}									
Hold Times: Address	t_{KHAX}	t_{AH}	0.5	—	0.5	—	0.5	—	ns	6
Address Status	t_{KHADSX}	t_{SH}								
Data In	t_{KHDX}	t_{DH}								
Write	t_{KHWX}	t_{WH}								
Address Advance	t_{KHADVX}									
Chip Enable	t_{KHEX}									

NOTES:
1. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
4. Maximum access times are guaranteed for all possible i486 external bus cycles.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled.Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

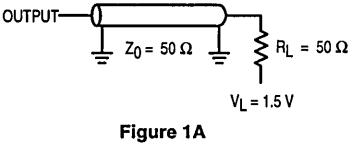


Figure 1A

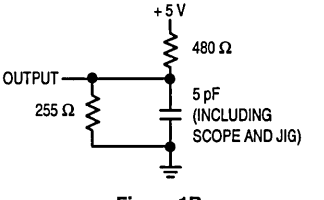
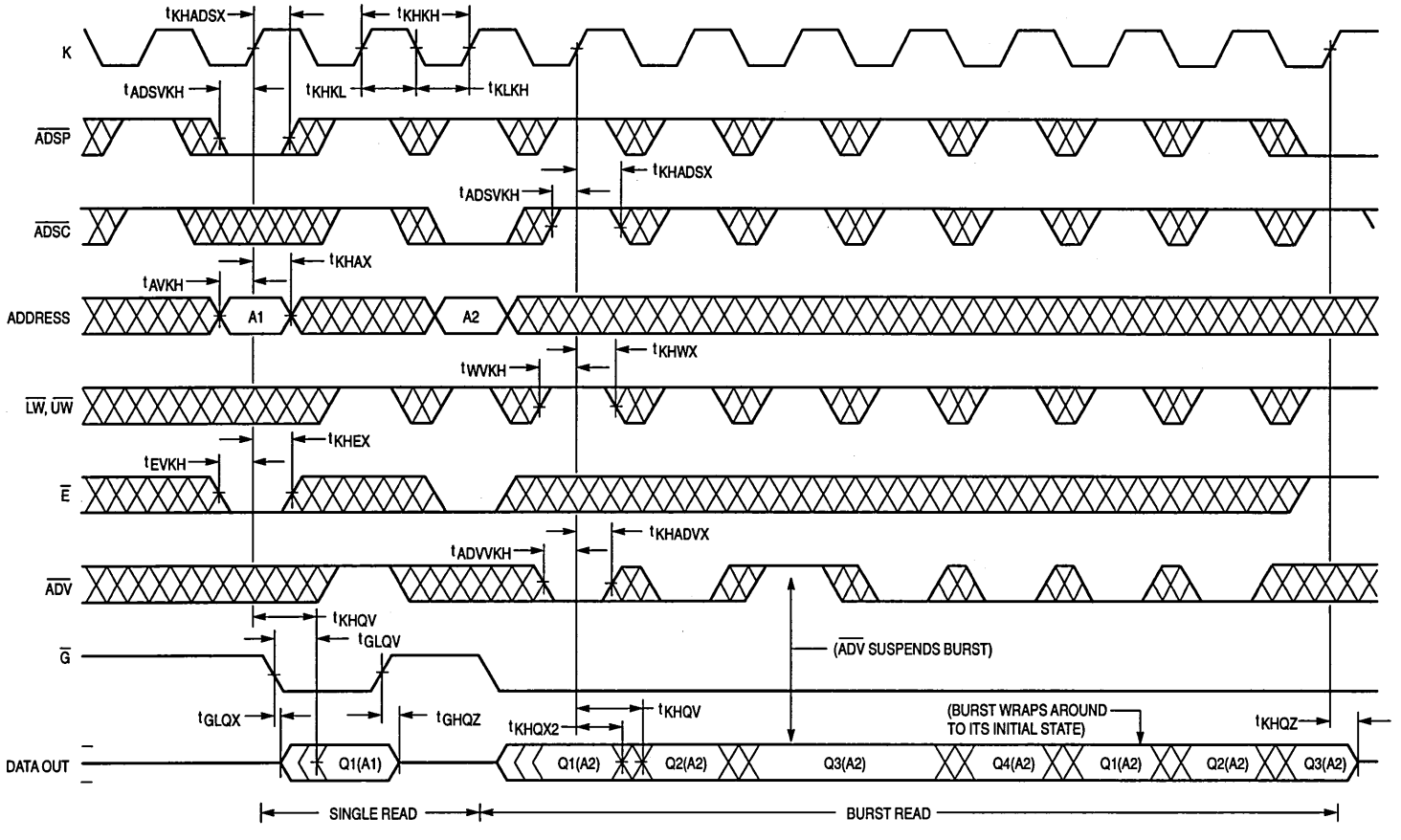


Figure 1B

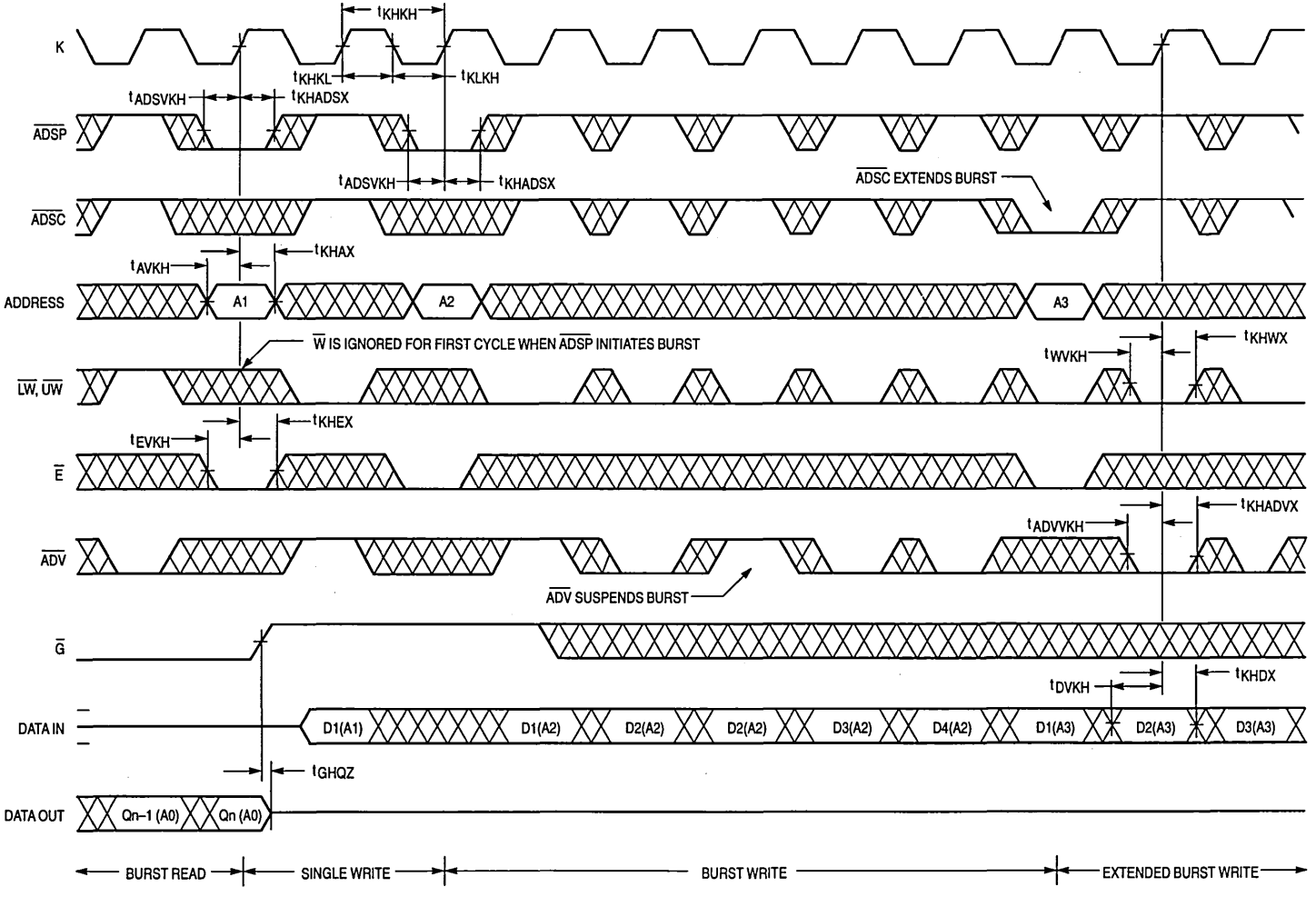
NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLES

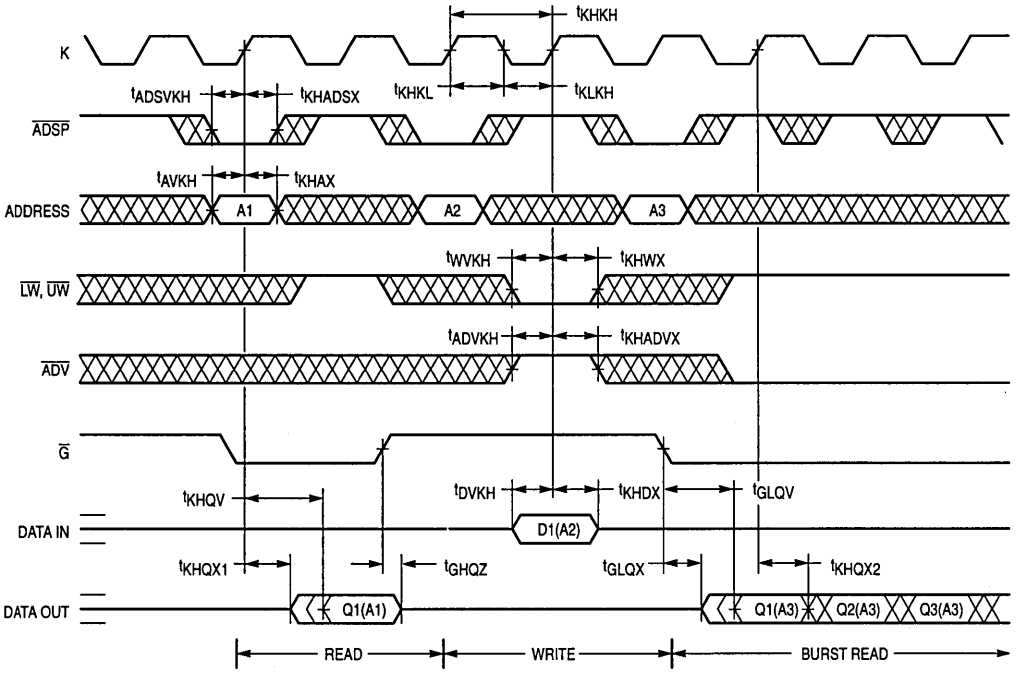


NOTE: Q1(A2) represents the first output data from the base address A2; Q2(A2) represents the next output data in the burst sequence with A2 as the base address.

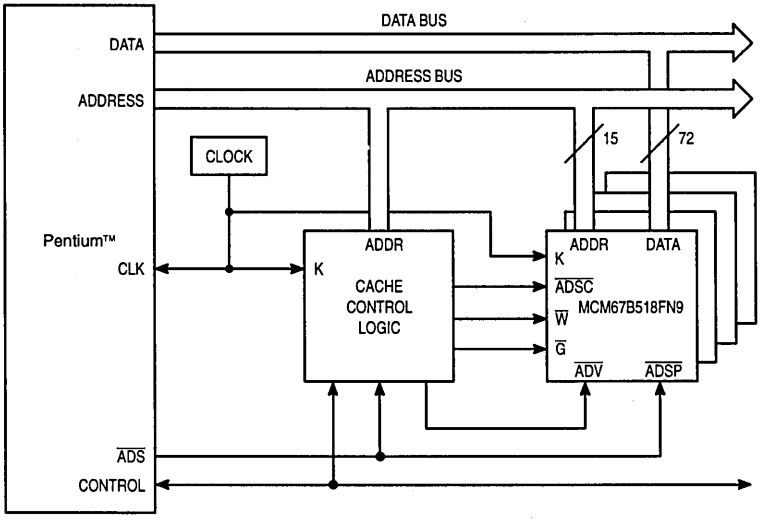
WRITE CYCLES



COMBINATION READ/WRITE CYCLE



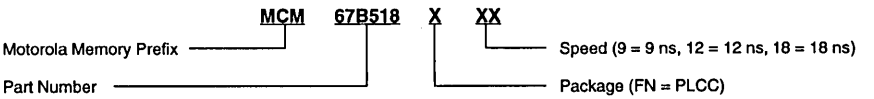
APPLICATION EXAMPLE



256K Byte Burstable, Secondary Cache
Using Four MCM67B518FN9s with a 66 MHz Pentium

Figure 2

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM67B518FN9 MCM67B518FN12 MCM67B518FN18

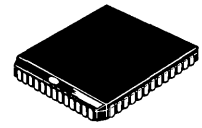
4

MCM67C518

Product Preview

32K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Registered Outputs



FN PACKAGE
PLASTIC
CASE 778

The MCM67C518 is a 589,824 bit synchronous static random access memory designed to provide a burstable, high-performance, secondary cache for the i486™ and Pentium™ microprocessors. It is organized as 32,768 words of 18 bits, fabricated with Motorola's high-performance silicon-gate BiCMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive registered output drivers onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A14), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive-edge-triggered noninverting registers.

This device contains output registers for pipeline operations. At the rising edge of K, the RAM provides the output data from the previous cycle.

Output enable ($\overline{G}$) is asynchronous for maximum system design flexibility.

Burst can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67C518 (burst sequence imitates that of the i486) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

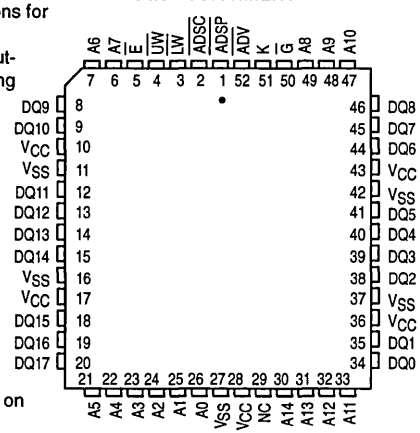
This device also incorporates pass-thru functionality. A read cycle preceded by a write cycle will cause the the data written into the array to appear at the outputs on the same clock cycle on which the read was initiated. The clock high to data valid time is the same as that of a standard read operation. Chip enable ($\overline{E}$) does not have to be asserted to receive valid data during a pass-thru operation. Output enable ($\overline{G}$) maintains control of the output buffers during a pass-thru operation.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Time/Fast Cycle Time = 7 ns/80 MHz, 9 ns/66 MHz
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Output Registers for Pipelined Applications
- Internally Self-Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Write Pass-Thru Capability
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52-Lead PLCC Package

PIN ASSIGNMENT



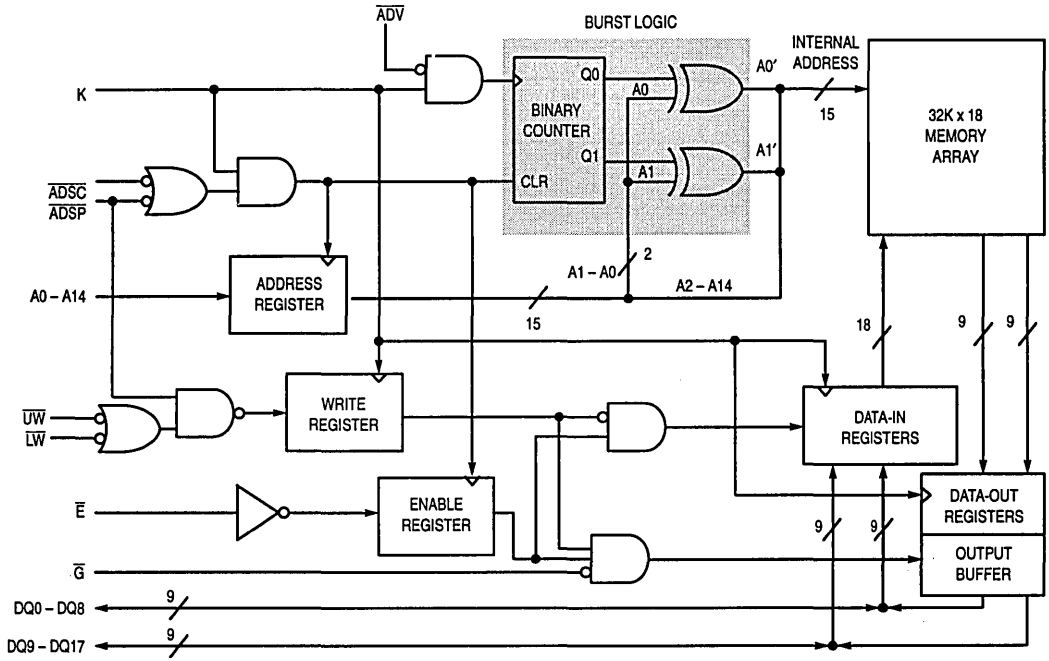
PIN NAMES

A0 – A14	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

BurstRAM is a trademark of Motorola, Inc.
i486 and Pentium are trademarks of Intel Corp.

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive-edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A14 – A2	A1	A0
1st Burst Address	A14 – A2	A1	$\overline{A0}$
2nd Burst Address	A14 – A2	$\overline{A1}$	A0
3rd Burst Address	A14 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	L	X	X	X	L-H	N/A	Deselected
H	X	L	X	X	L-H	N/A	Deselected
L	L	X	X	X	L-H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High-Z
Write	X	High-Z — Data In
Deselected	X	High-Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

PASS-THRU TRUTH TABLE (Read preceded by a write)

Operation of Previous Cycle	$\overline{E}$	$\overline{LW}$	$\overline{UW}$	$\overline{G}$	Operation of Present Cycle	Operation of Next Cycle
Write Cycle, Both Bytes (Address = n – 1)	L	L	L	L	1. Register Address = n and all Inputs 2. Data of Address = n – 1 Appears at Outputs	Read Data at Address = n
Write Cycle, Upper Byte (Address = n – 1)	H	L	H	L	Data of Address = n – 1 Appears at Outputs of Upper Byte	No Carry-Over Operation From Previous Cycle
Write Cycle, Both Bytes (Address = n – 1)	H	L	L	H	All I/Os High-Z	No Carry-Over Operation From Previous Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	+ 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA7} I_{CCA9}	—	290 275	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	75	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM67C518-7		MCM67C518-9		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	t_{CYC}	12.5	—	15	—	ns	
Clock Access Time	t_{KHQV}	t_{CD}	—	7	—	9	ns	5
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	t_{DC1}	2	—	2	—	ns	
Clock High to Output Change	t_{KHQX2}	t_{DC2}	2	—	2	—	ns	
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	1	—	1	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{OHZ}	2	6	2	6	ns	6
Clock High to Q High-Z	t_{KHQZ}	t_{CZ}	—	6	—	6	ns	
Clock High Pulse Width	t_{KHKL}	t_{CH}	5	—	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	t_{CL}	5	—	5	—	ns	
Setup Times: Address	t_{AVKH}	t_{AS}	2.5	—	2.5	—	ns	7
Address Status	t_{ADSVKH}	t_{SS}						
Data In	t_{DVKH}	t_{DS}						
Write	t_{WVKH}	t_{WS}						
Address Advance	t_{ADVVKH}							
Chip Enable	t_{EVKH}							
Hold Times: Address	t_{KHAX}	t_{AH}	0.5	—	0.5	—	ns	7
Address Status	t_{KHADSX}	t_{SH}						
Data In	t_{KHDX}	t_{DH}						
Write	t_{KHWX}	t_{WH}						
Address Advance	t_{KHADVX}							
Chip Enable	t_{KHEX}							

NOTES:
1. $\overline{W}$ refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 external bus cycles.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled.Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

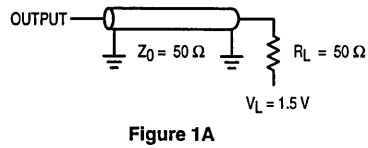


Figure 1A

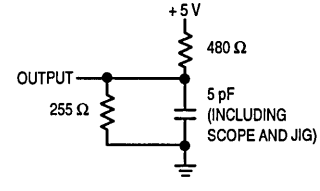
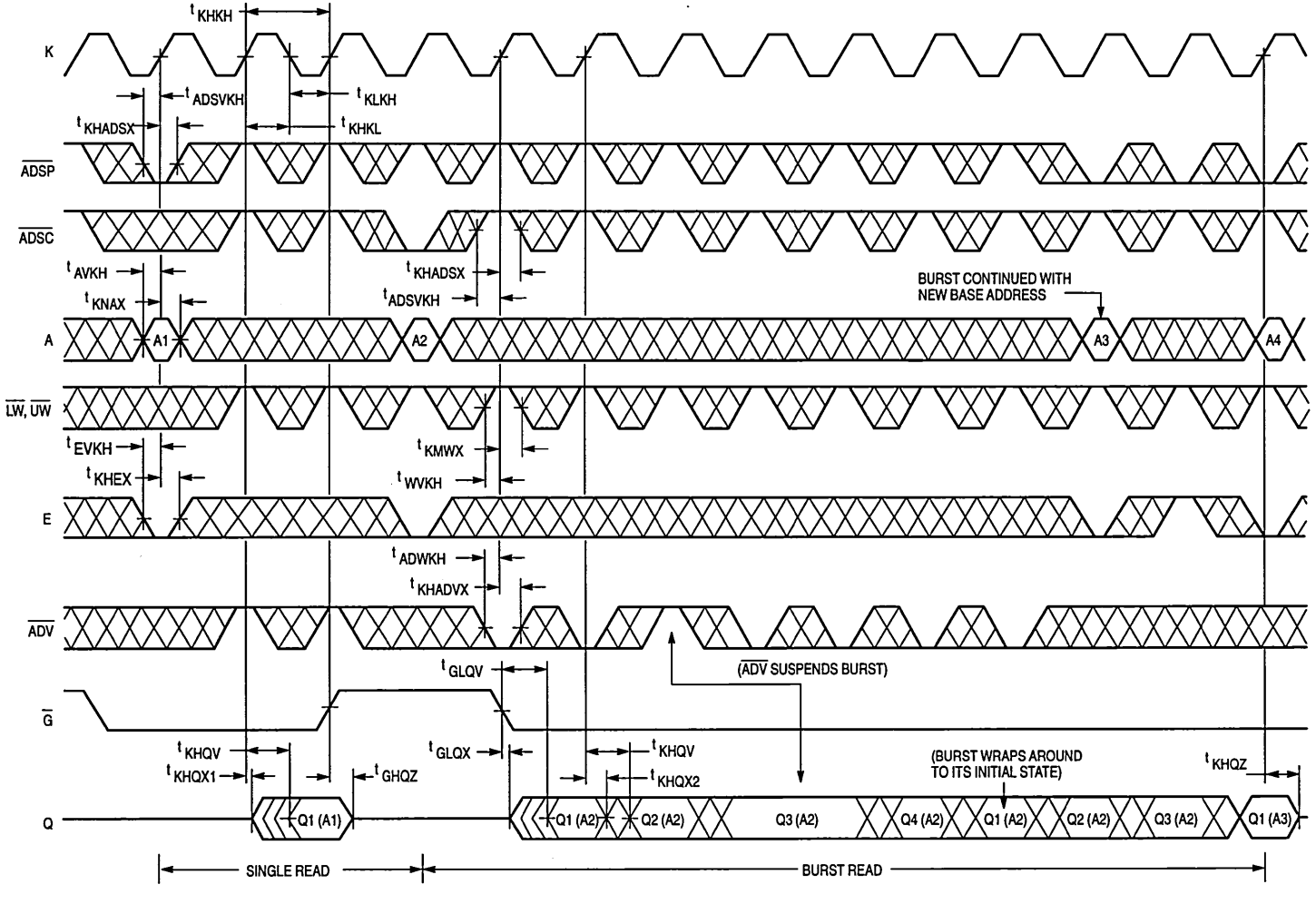


Figure 1B

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLES



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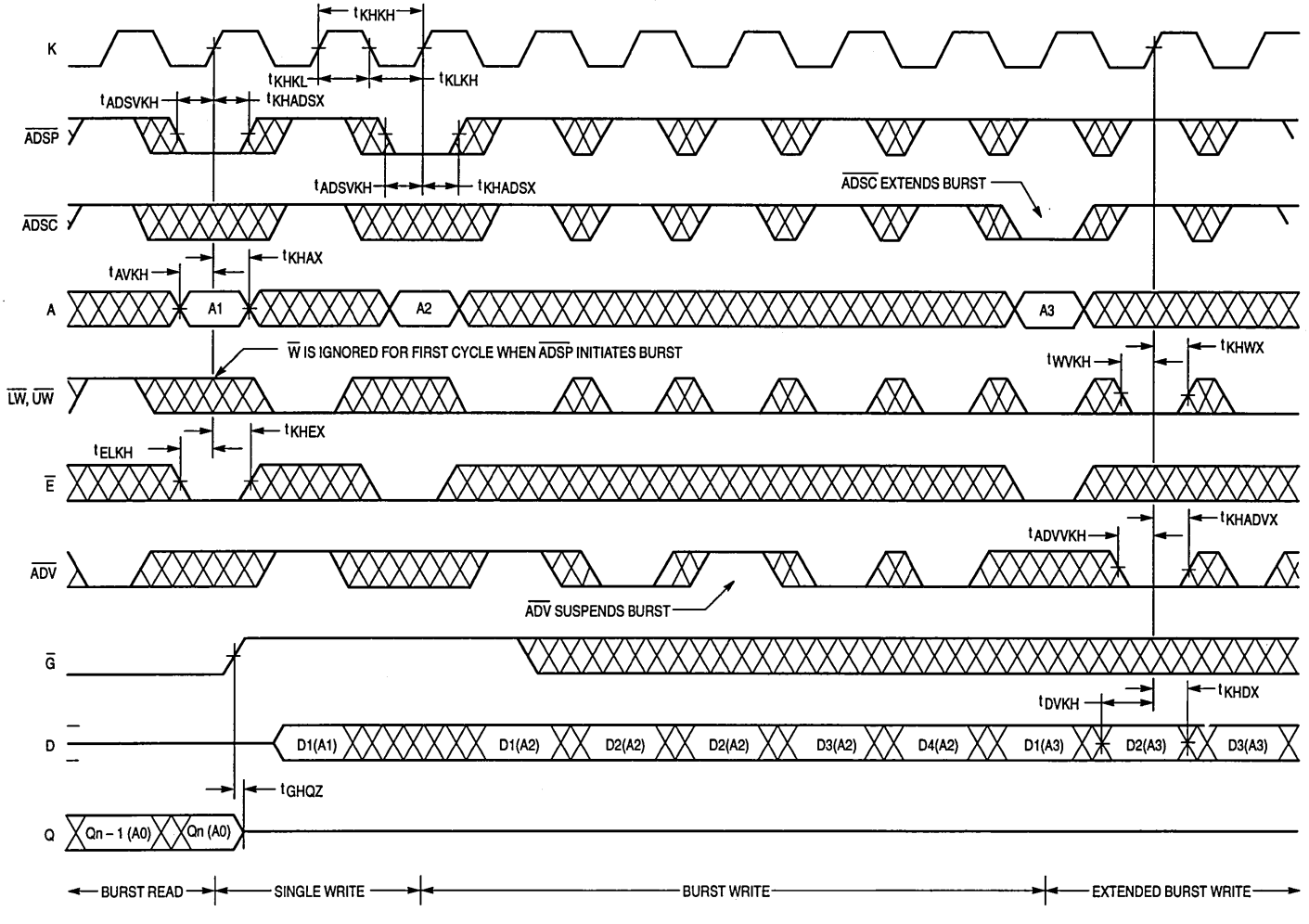
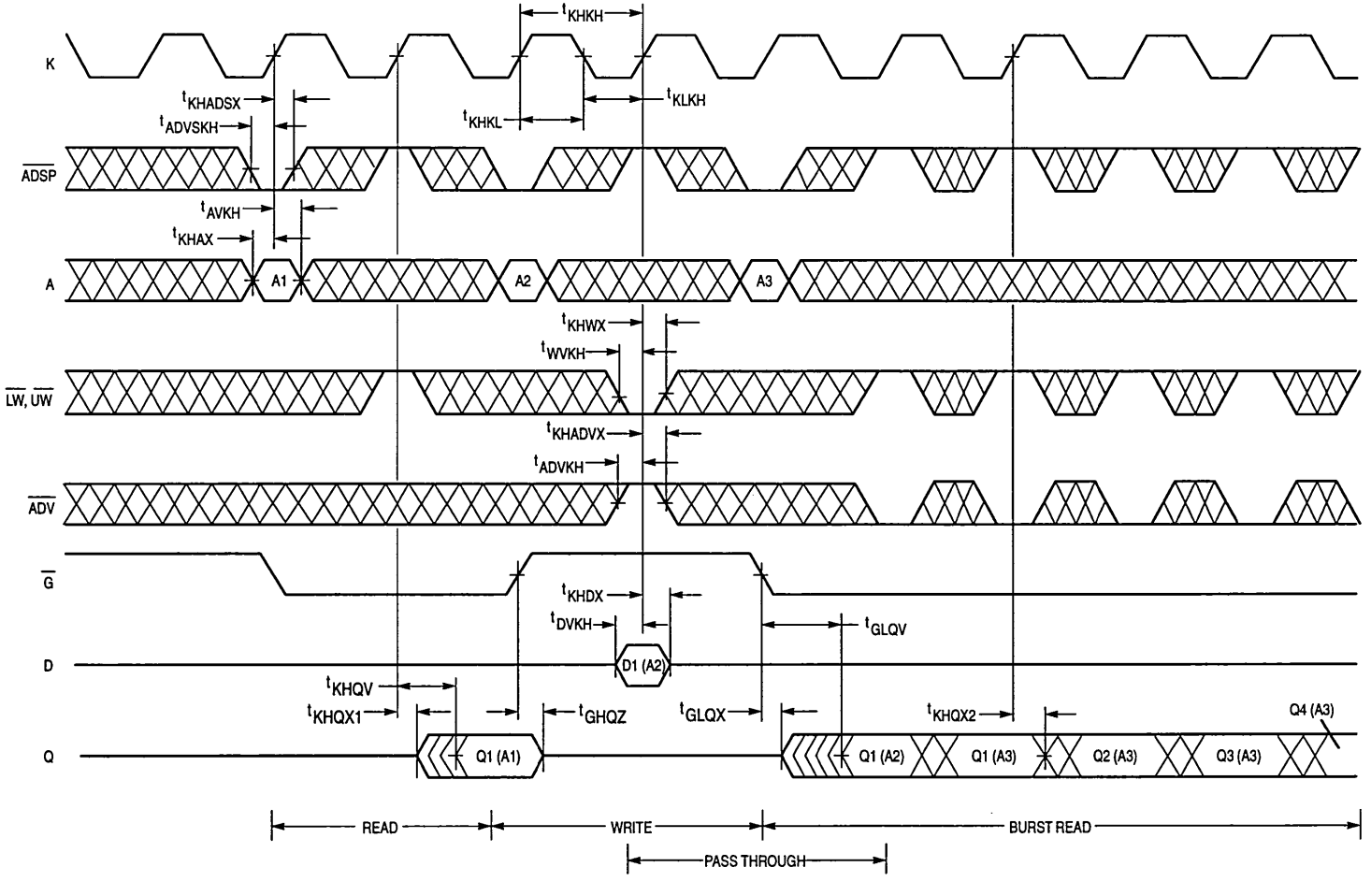
WRITE CYCLES



COMBINATION READ/WRITE CYCLES



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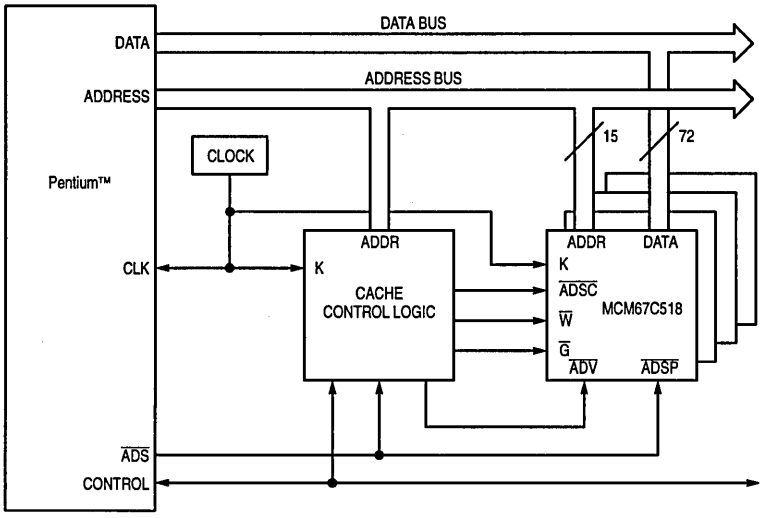
APPLICATION EXAMPLE



256K BYTE BURSTABLE, SECONDARY CACHE USING
FOUR MCM67C518FN9s WITH A 66 MHz PENTIUM

ORDERING INFORMATION
(Order by Full Part Number)

MCM 67C518 X XX

Motorola Memory Prefix — MCM

Part Number — 67C518

Speed (7 = 7 ns, 9 = 9 ns) — XX

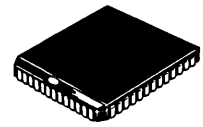
Package (FN = PLCC) — X

Full Part Numbers — MCM67C518FN7 MCM67C518FN9

MCM67H518

Product Preview

32K x 18 Bit BurstRAM™ Synchronous Fast Static RAM
With Burst Counter and Self-Timed Write



FN PACKAGE
PLASTIC
CASE 778

The MCM67H518 is a 589,824 bit synchronous fast static random access memory designed to provide a burstable, high-performance, secondary cache for the i486 and Pentium™ microprocessors. It is organized as 32,768 words of 18 bits, fabricated with Motorola's high-performance silicon-gate BiCMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A14), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive-edge-triggered noninverting registers.

Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67H518 (burst sequence imitates that of the i486 and Pentium) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

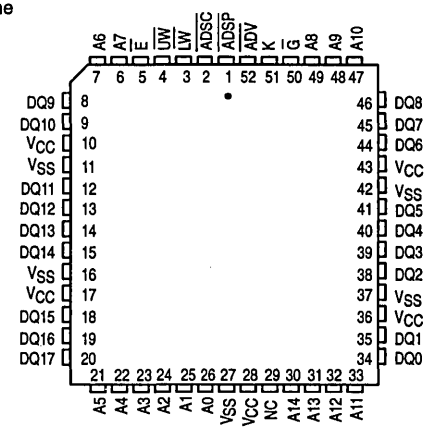
Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 9/12/18 ns Max
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Internally Self-Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52-Lead PLCC Package
- $\overline{ADSP}$ Disabled with Chip Enable ($\overline{E}$) – Supports Address Pipelining

PIN ASSIGNMENT

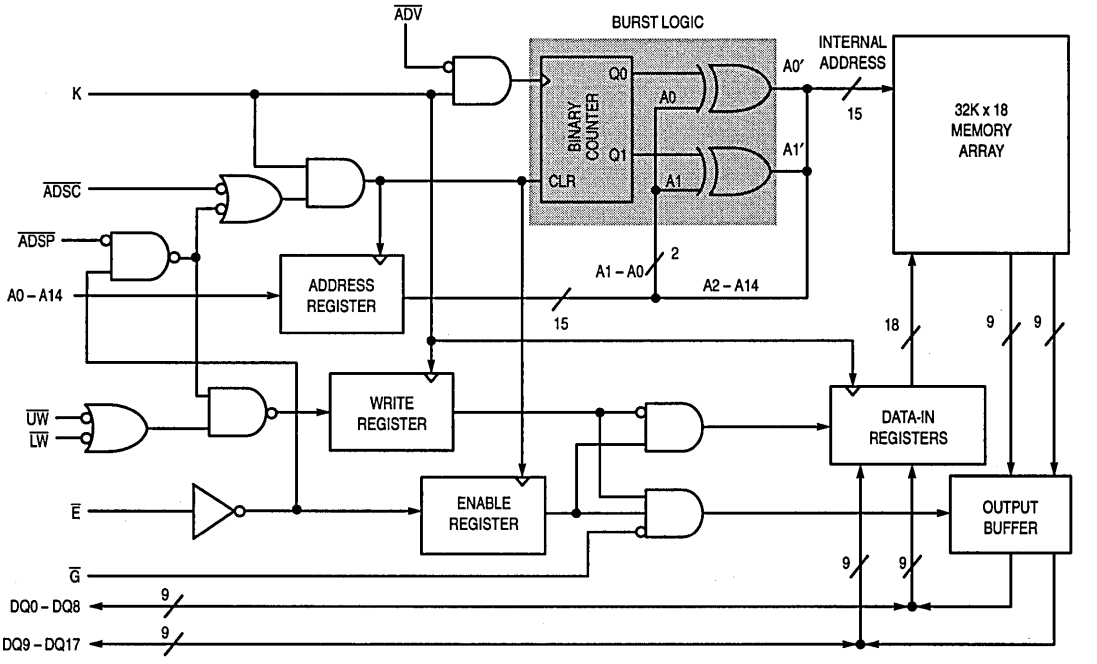


PIN NAMES	
A0 – A14	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
VCC	+ 5 V Power Supply
VSS	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

BurstRAM is a trademark of Motorola, Inc.
i486 and Pentium are trademarks of Intel Corp.

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive-edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A14 – A2	A1	A0
1st Burst Address	A14 – A2	A1	$\overline{A0}$
2nd Burst Address	A14 – A2	$\overline{A1}$	A0
3rd Burst Address	A14 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	X	L	X	X	L-H	N/A	Deselected
L	L	X	X	X	L-H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst
H	X	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
H	X	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
H	X	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
H	X	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High-Z
Write	X	High-Z — Data In
Deselected	X	High-Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	− 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{bias}	− 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA9} I_{CCA12} I_{CCA18}	— — —	275 250 225	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	75	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3) ($\overline{W}$ refers to either or both byte write enables)

Parameter	Symbol		MCM67H518-9		MCM67H518-12		MCM67H518-18		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	t_{CYC}	15	—	20	—	30	—	ns	
Clock Access Time	t_{KHQV}	t_{CD}	—	9	—	12	—	18	ns	4
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	5	—	6	—	7	ns	
Clock High to Output Active	t_{KHQX1}	t_{DC1}	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	t_{DC2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{OHZ}	2	6	2	7	2	7	ns	5
Clock High to Q High-Z	t_{KHQZ}	t_{CZ}	—	6	—	6	—	6	ns	
Clock High Pulse Width	t_{KHKL}	t_{CH}	5	—	6	—	7	—	ns	
Clock Low Pulse Width	t_{KLKH}	t_{CL}	5	—	6	—	7	—	ns	
Setup Times: Address	t_{AVKH}	t_{AS}	2.5	—	2.5	—	3.0	—	ns	6
Address Status	t_{ADSVKH}	t_{SS}								
Data In	t_{DVKH}	t_{DS}								
Write	t_{WVKH}	t_{WS}								
Address Advance	t_{ADVVKH}									
Chip Enable	t_{EVKH}									
Hold Times: Address	t_{KHAX}	t_{AH}	0.5	—	0.5	—	0.5	—	ns	6
Address Status	t_{KHADSX}	t_{SH}								
Data In	t_{KHDX}	t_{DH}								
Write	t_{KHWX}	t_{WH}								
Address Advance	t_{KHADVX}									
Chip Enable	t_{KHEX}									

NOTES:
1. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
4. Maximum access times are guaranteed for all possible i486 external bus cycles.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled.Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

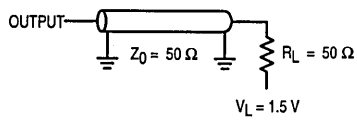


Figure 1A

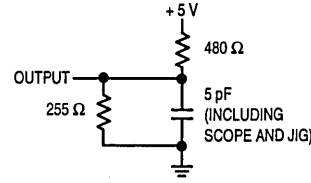
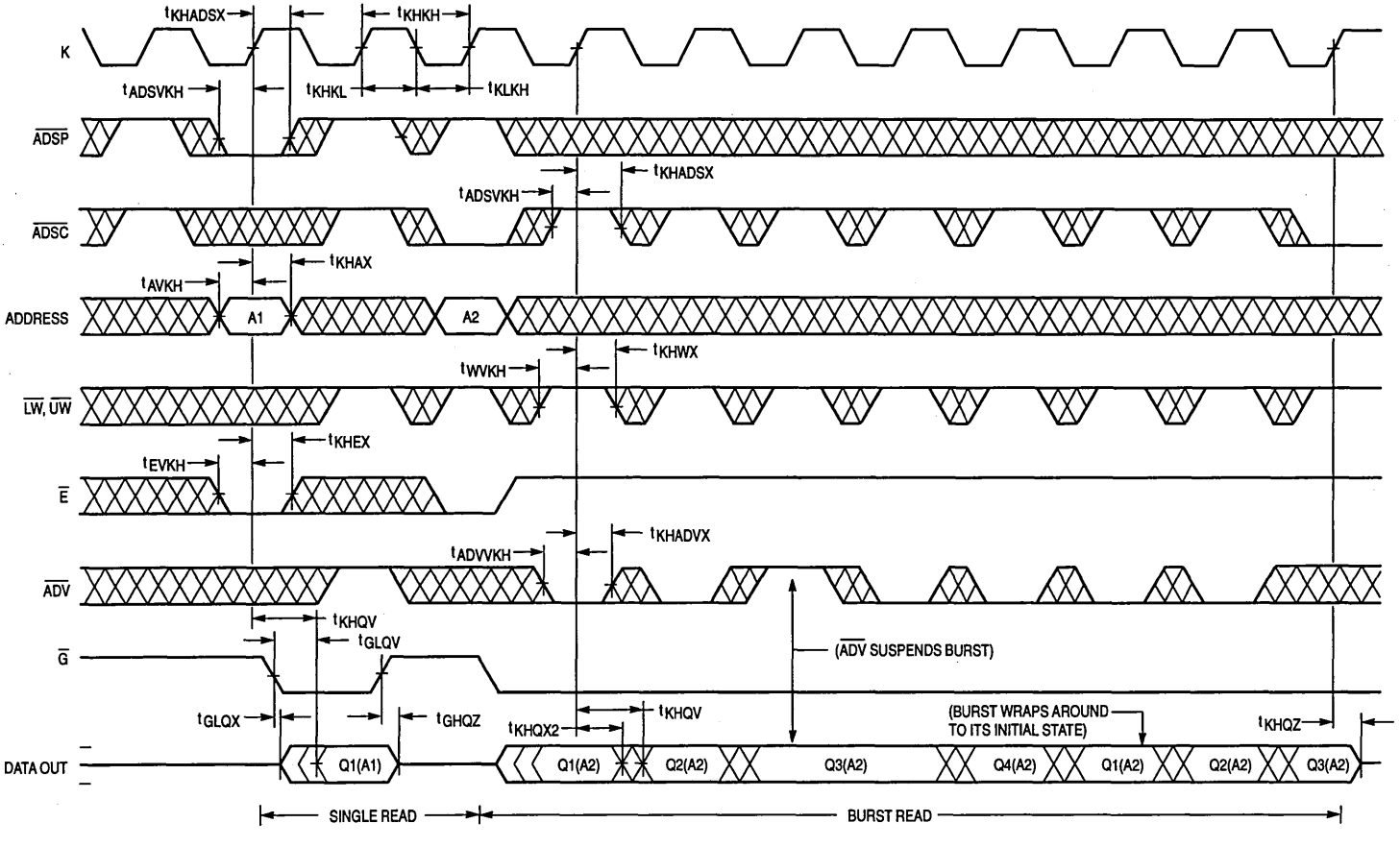


Figure 1B

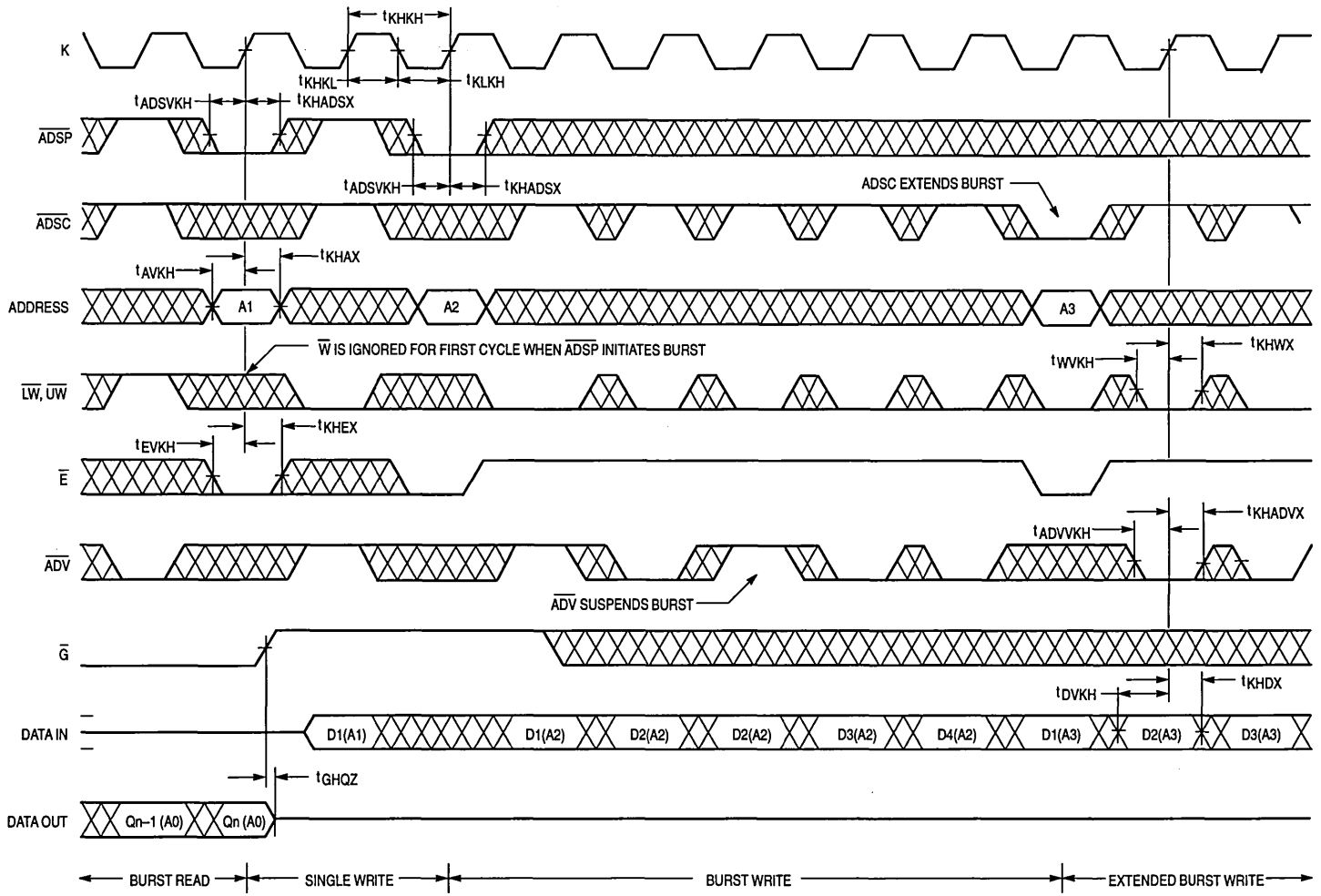
NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLES

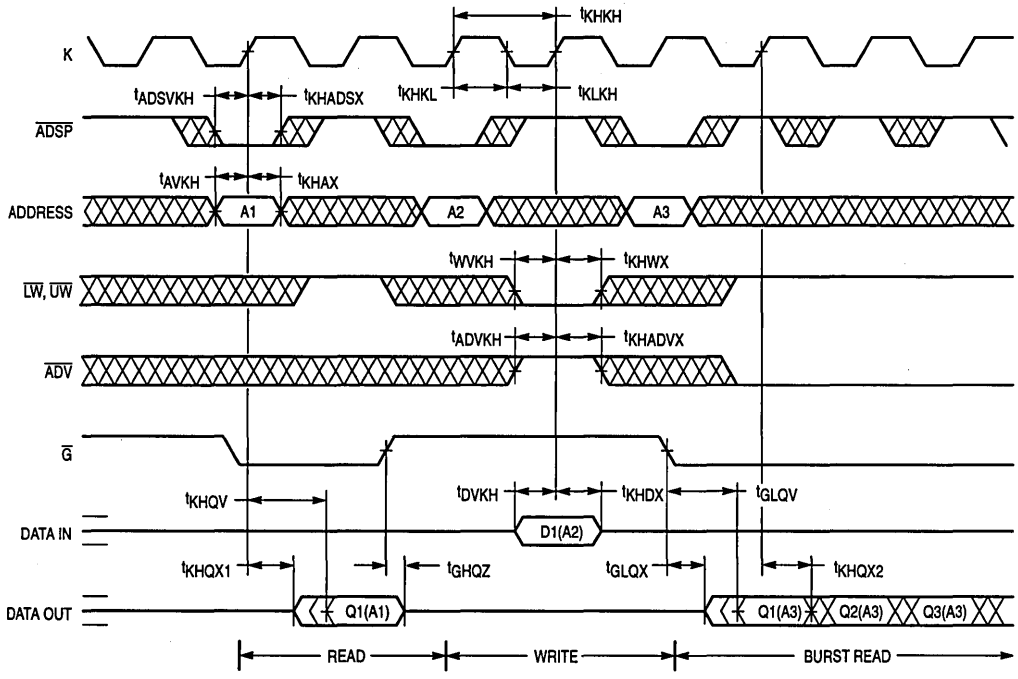


NOTE: Q1(A2) represents the first output data from the base address A2; Q2(A2) represents the next output data in the burst sequence with A2 as the base address.

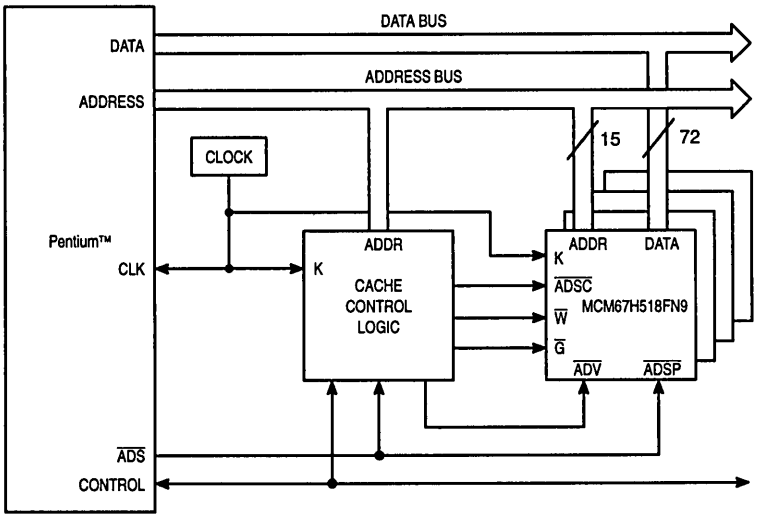
WRITE CYCLES



COMBINATION READ/WRITE CYCLE



APPLICATION EXAMPLE



256K Byte Burstable, Secondary Cache
Using Four MCM67H518FN9s with a 66 MHz Pentium

Figure 2

4

ORDERING INFORMATION
(Order by Full Part Number)

MCM	67H518	X	XX
Motorola Memory Prefix			
Part Number			
		Package (FN = PLCC)	
			Speed (9 = 9 ns, 12 = 12 ns, 18 = 18 ns)

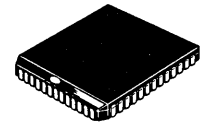
Full Part Numbers — MCM67H518FN9 MCM67H518FN12 MCM67H518FN18

MCM67J518

Product Preview

32K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Registered Outputs



FN PACKAGE
PLASTIC
CASE 778

The MCM67J518 is a 589,824 bit synchronous static random access memory designed to provide a burstable, high-performance, secondary cache for the i486™ and Pentium™ microprocessors. It is organized as 32,768 words of 18 bits, fabricated with Motorola's high-performance silicon-gate BiCMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive registered output drivers onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A14), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive-edge-triggered noninverting registers.

This device contains output registers for pipeline operations. At the rising edge of K, the RAM provides the output data from the previous cycle.

Output enable ($\overline{G}$) is asynchronous for maximum system design flexibility.

Burst can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67J518 (burst sequence imitates that of the i486) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

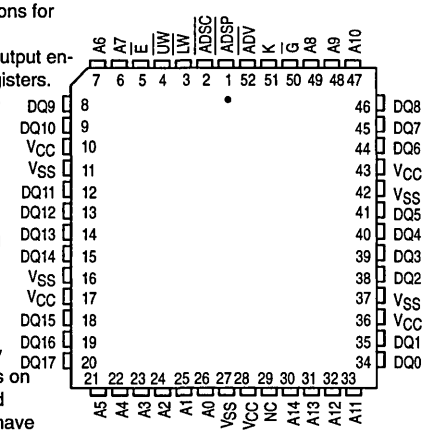
This device also incorporates pass-thru functionality. A read cycle preceded by a write cycle will cause the the data written into the array to appear at the outputs on the same clock cycle on which the read was initiated. The clock high to data valid time is the same as that of a standard read operation. Chip enable ($\overline{E}$) does not have to be asserted to receive valid data during a pass-thru operation. Output enable ($\overline{G}$) maintains control of the output buffers during a pass-thru operation.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Time/Fast Cycle Time = 7 ns/80 MHz, 9 ns/66 MHz
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Output Registers for Pipelined Applications
- Internally Self-Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Write Pass-Thru Capability
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52-Lead PLCC Package
- $\overline{ADSP}$ Disabled with Chip Enable ($\overline{E}$) – Supports Address Pipelining

PIN ASSIGNMENT



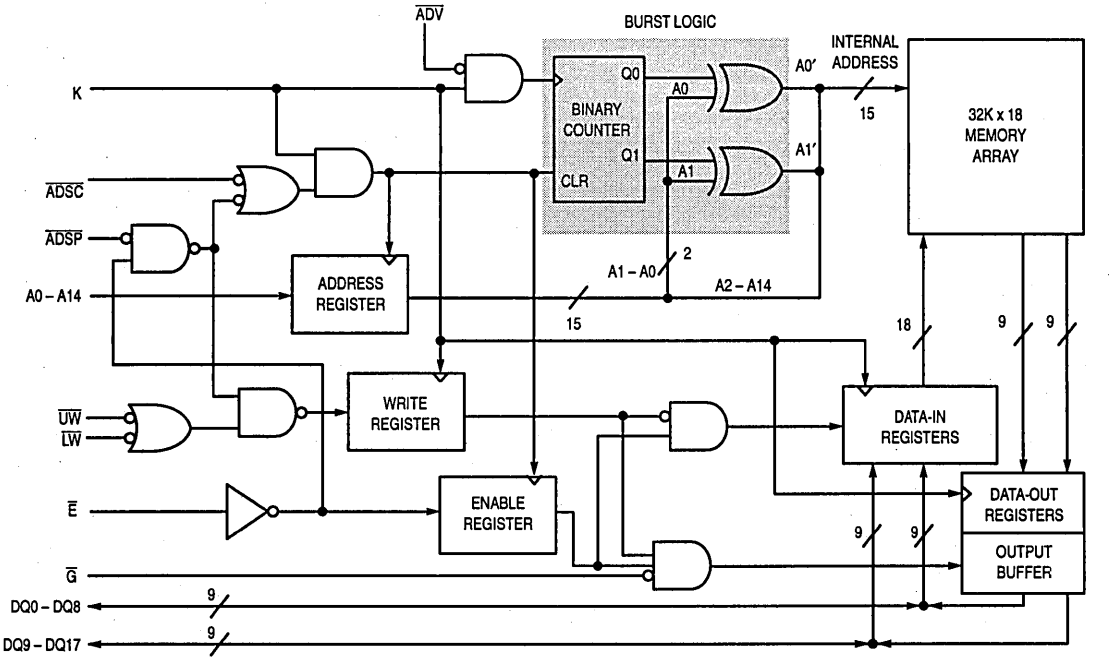
PIN NAMES

A0 – A14	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

BurstRAM is a trademark of Motorola, Inc.
i486 and Pentium are trademarks of Intel Corp.

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive-edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A14 – A2	A1	A0
1st Burst Address	A14 – A2	A1	$\overline{A0}$
2nd Burst Address	A14 – A2	$\overline{A1}$	A0
3rd Burst Address	A14 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	X	L	X	X	L-H	N/A	Deselected
L	L	X	X	X	L-H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst
H	X	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
H	X	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
H	X	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
H	X	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. Wait states are inserted by suspending burst.

4

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High-Z
Write	X	High-Z — Data In
Deselected	X	High-Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

PASS-THRU TRUTH TABLE (Read preceded by a write)

Operation of Previous Cycle	$\overline{E}$	$\overline{LW}$	$\overline{UW}$	$\overline{G}$	Operation of Present Cycle	Operation of Next Cycle
Write Cycle, Both Bytes (Address = n – 1)	L	L	L	L	1. Register Address = n and all Inputs 2. Data of Address = n – 1 Appears at Outputs	Read Data at Address = n
Write Cycle, Upper Byte (Address = n – 1)	H	L	H	L	Data of Address = n – 1 Appears at Outputs of Upper Byte	No Carry-Over Operation From Previous Cycle
Write Cycle, Both Bytes (Address = n – 1)	H	L	L	H	All I/Os High-Z	No Carry-Over Operation From Previous Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	+ 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA7} I_{CCA9}	—	290 275	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	75	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM67J518-7		MCM67J518-9		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	t_{CYC}	12.5	—	15	—	ns	
Clock Access Time	t_{KHQV}	t_{CD}	—	7	—	9	ns	5
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	t_{DC1}	2	—	2	—	ns	
Clock High to Output Change	t_{KHQX2}	t_{DC2}	2	—	2	—	ns	
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	1	—	1	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{OHZ}	2	6	2	6	ns	6
Clock High to Q High-Z	t_{KHQZ}	t_{CZ}	—	6	—	6	ns	
Clock High Pulse Width	t_{KHKL}	t_{CH}	5	—	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	t_{CL}	5	—	5	—	ns	
Setup Times: Address	t_{AVKH}	t_{AS}	2.5	—	2.5	—	ns	7
Address Status	t_{ADSVKH}	t_{SS}						
Data In	t_{DVKH}	t_{DS}						
Write	t_{WVKH}	t_{WS}						
Address Advance	t_{ADVVKH}							
Chip Enable	t_{EVKH}							
Hold Times: Address	t_{KHAX}	t_{AH}	0.5	—	0.5	—	ns	7
Address Status	t_{KHADSX}	t_{SH}						
Data In	t_{KHDX}	t_{DH}						
Write	t_{KHWX}	t_{WH}						
Address Advance	t_{KHADVX}							
Chip Enable	t_{KHEX}							

NOTES:
1. $\overline{W}$ refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 external bus cycles.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled.Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

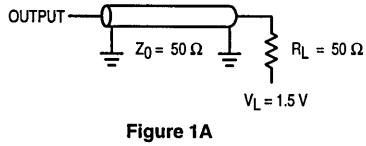


Figure 1A

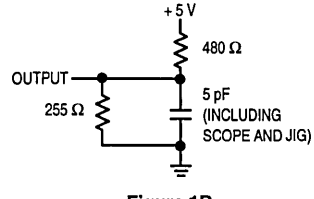
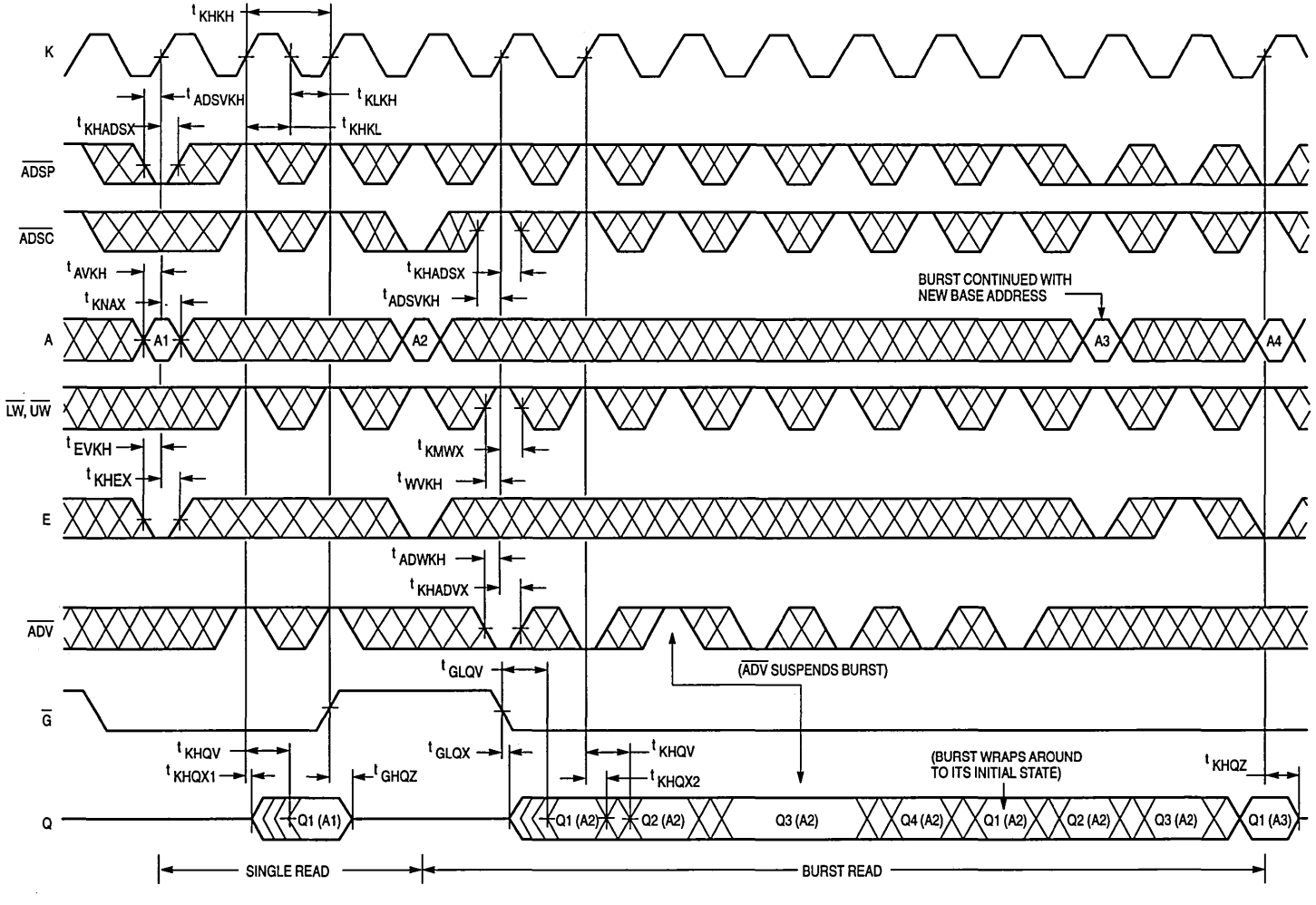


Figure 1B

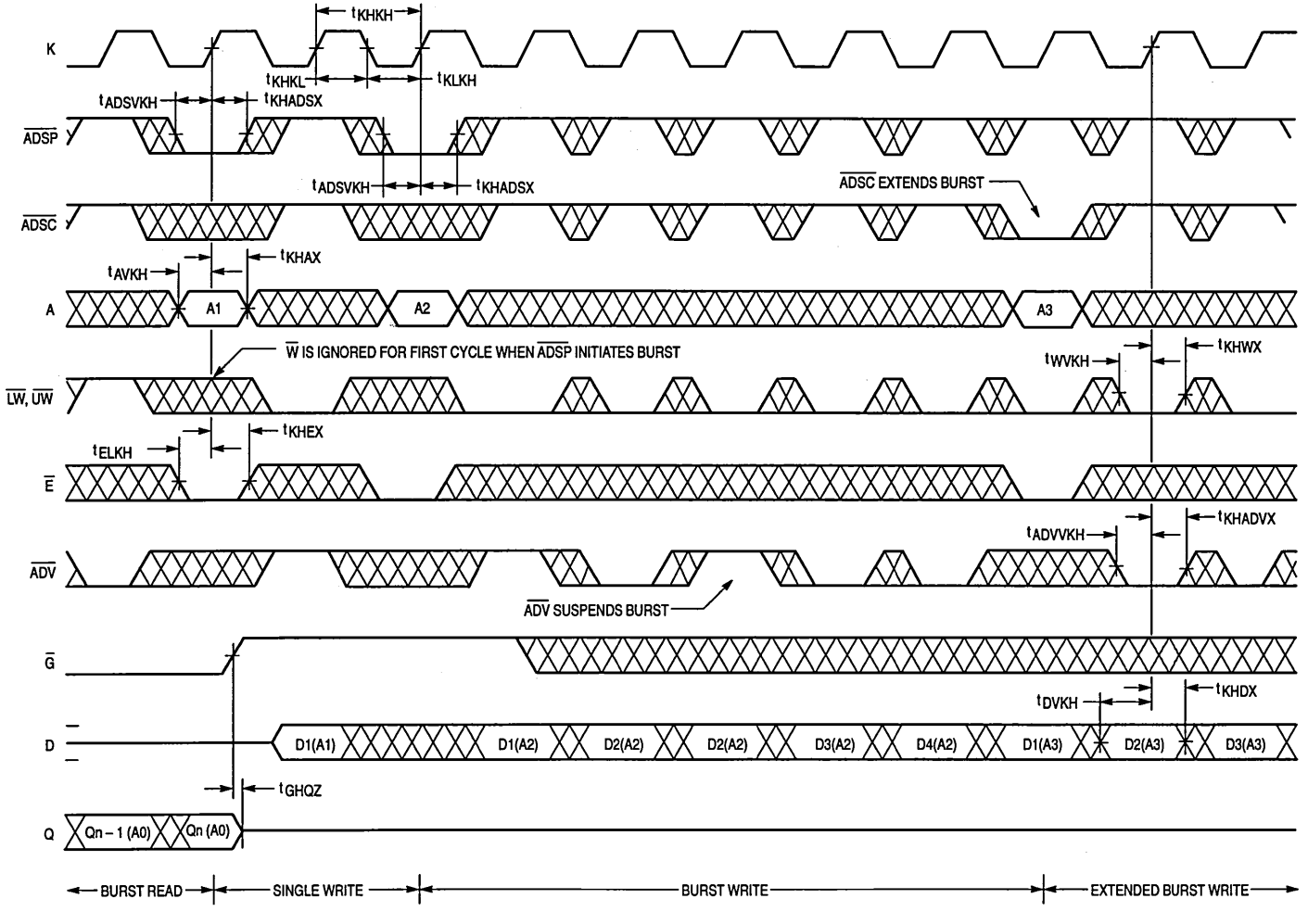
NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLES

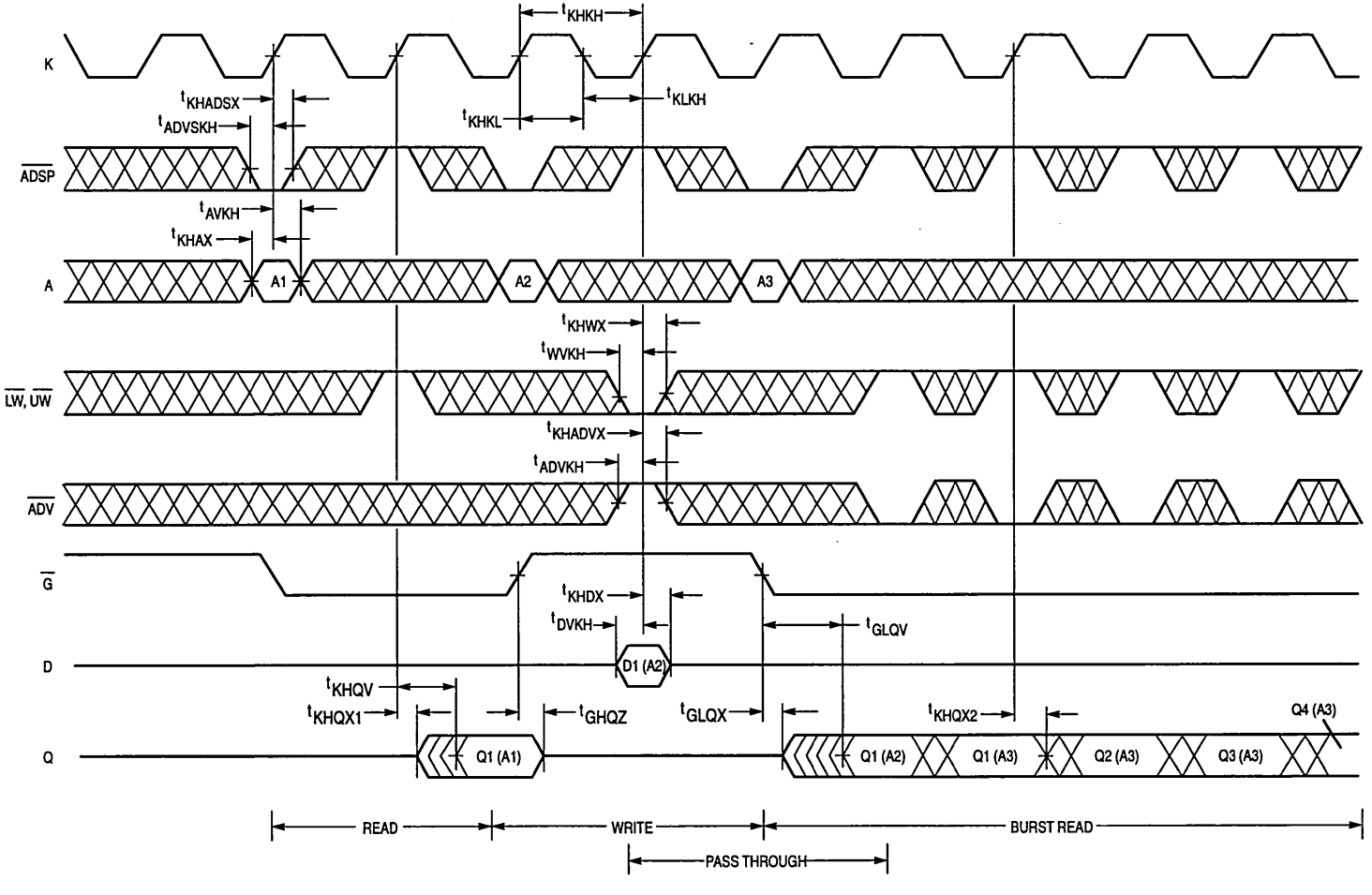


4

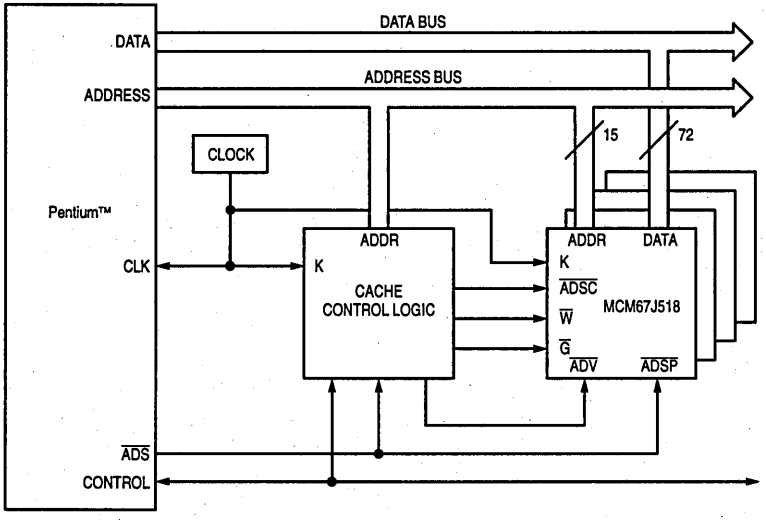
WRITE CYCLES



COMBINATION READ/WRITE CYCLES



APPLICATION EXAMPLE



256K BYTE BURSTABLE, SECONDARY CACHE USING
FOUR MCM67J518FN9s WITH A 66 MHz PENTIUM

ORDERING INFORMATION
(Order by Full Part Number)

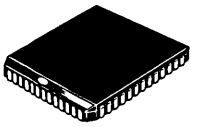
MCM	67J518	X	XX
Motorola Memory Prefix			
	Part Number		
			Package (FN = PLCC)
			Speed (7 = 7 ns, 9 = 9 ns)

Full Part Numbers — MCM67J518FN7 MCM67J518FN9

MCM67M518

Product Preview

32K x 18 Bit BurstRAM™ Synchronous Fast Static RAM
With Burst Counter and Self-Timed Write



FN PACKAGE
PLASTIC
CASE 778

The MCM67M518 is a 589,824 bit synchronous static random access memory designed to provide a burstable, high-performance, secondary cache for the MC68040 and PowerPC™ microprocessors. It is organized as 32,768 words of 18 bits, fabricated using Motorola's high-performance silicon-gate BiCMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A14), data inputs (DQ0 – DQ17), and all control signals, except output enable ($\overline{G}$), are clock (K) controlled through positive-edge-triggered noninverting registers.

Bursts can be initiated with either transfer start processor ($\overline{TSP}$) or transfer start cache controller ($\overline{TSC}$) input pins. Subsequent burst addresses are generated internally by the MCM67M518 (burst sequence imitates that of the MC68040) and controlled by the burst address advance ($\overline{BAA}$) input pin. The following pages provide more detailed information on burst controls.

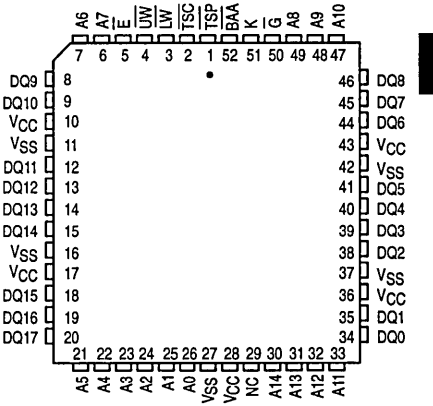
Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 9/11/14/19 ns Max and Cycle Times: 12.5/15/20/25 ns Min
- Byte Writeable via Dual Write Strobes
- Internal Input Registers (Address, Data, Control)
- Internally Self-Timed Write Cycle
- $\overline{TSP}$, $\overline{TSC}$, and $\overline{BAA}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- High Board Density 52-PLCC Package
- 3.3 V I/O Compatible

PIN ASSIGNMENT

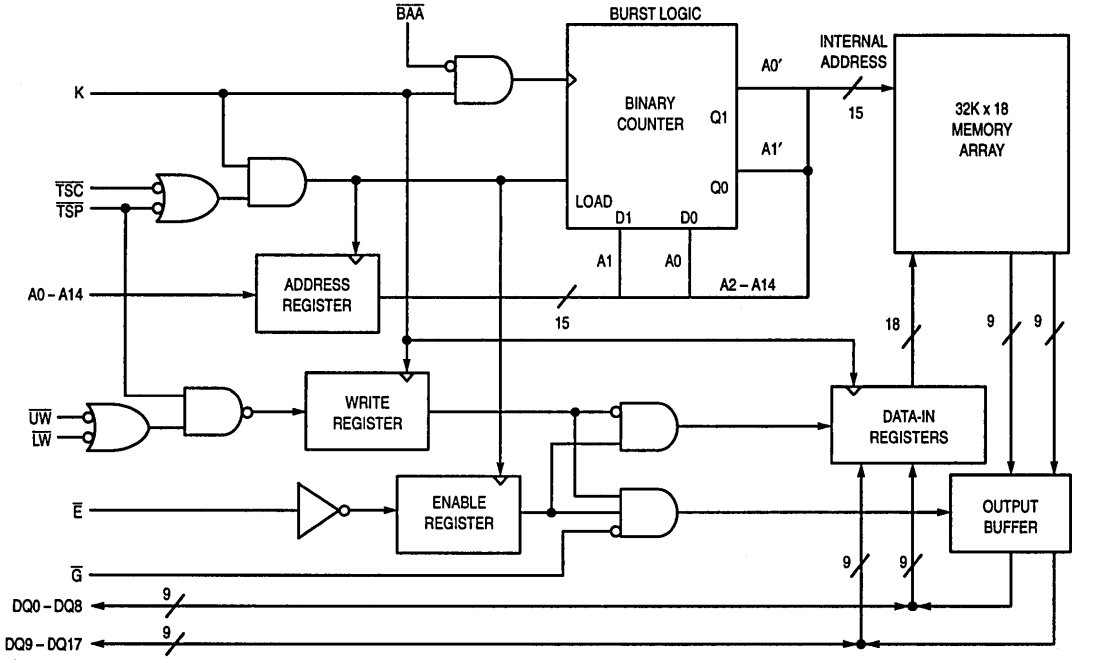


PIN NAMES	
A0 – A14	Address Inputs
K	Clock
$\overline{BAA}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{TSP}$, $\overline{TSC}$	Transfer Start
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

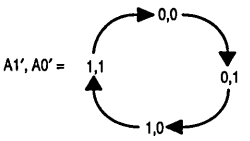
BurstRAM is a trademark of Motorola, Inc.
PowerPC is a trademark of IBM Corp.

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive-edge triggered. The $\overline{TSC}$ or $\overline{TSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{TSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{TSC}$) is performed using the new external address. When $\overline{TSC}$ is sampled low (and $\overline{TSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the next external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{BAA}$ controls subsequent burst cycles. When $\overline{BAA}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{BAA}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE GRAPH**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE GRAPH (See Note)



NOTE: The external two values for A1 and A0 provide the starting point for the burst sequence graph. The burst logic advances A1 and A0 as shown above.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{TSP}$	$\overline{TSC}$	$\overline{BAA}$	$\overline{LW}$ or $\overline{UW}$	K	Address	Operation
H	L	X	X	X	L-H	N/A	Deselected
H	X	L	X	X	L-H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out (DQ0 – DQ8)
Read	H	High-Z
Write	X	High-Z — Data In
Deselected	X	High-Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA9} I_{CCA11} I_{CCA14} I_{CCA19}	—	290 275 250 225	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	75	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible 68040 bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3) ($\overline{W}$ refers to either or both byte write enables)

Parameter	Symbol Std	Symbol Alt	67M518-9 Min	67M518-9 Max	67M518-11 Min	67M518-11 Max	67M518-14 Min	67M518-14 Max	67M518-19 Min	67M518-19 Max	Unit	Notes
Cycle Time	t_{KHKH}	t_{CYC}	12.5	—	15	—	20	—	25	—	ns	
Clock Access Time	t_{KHQV}	t_{CD}	—	9	—	11	—	14	—	19	ns	4
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	5	—	5	—	6	—	7	ns	
Clock High to Output Active	t_{KHQX1}	t_{DC1}	6	—	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	t_{DC2}	3	—	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{OHZ}	2	6	2	6	2	6	2	7	ns	5
Clock High to Q High-Z	t_{KHQZ}	t_{CZ}	—	6	—	6	—	6	—	6	ns	5
Clock High Pulse Width	t_{KHKL}	t_{CH}	5	—	5	—	6	—	7	—	ns	
Clock Low Pulse Width	t_{KLKH}	t_{CL}	5	—	5	—	6	—	7	—	ns	
Setup Times: Address Address Status Data In Write Address Advance Chip Select	t_{AVKH} t_{TSVKH} t_{DVKH} t_{WVKH} t_{BAVKH} t_{EVKH}	t_{AS} t_{SS} t_{DS} t_{WS}	2.5	—	2.5	—	2.5	—	3.0	—	ns	6
Hold Times: Address Address Status Data In Write Address Advance Chip Select	t_{KHAX} t_{KHTSX} t_{KHDX} t_{KHWX} t_{KHBAX} t_{KHEX}	t_{AH} t_{SH} t_{DH} t_{WH}	0.5	—	0.5	—	0.5	—	0.5	—	ns	6

NOTES:
1. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{TSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{TSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
4. Maximum access times are guaranteed for all possible MC68040 external bus cycles.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX1} min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of clock (K) whenever $\overline{TSP}$ or $\overline{TSC}$ are low and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is selected.Chip enable must be valid at each rising edge of clock for the device (when $\overline{TSP}$ or $\overline{TSC}$ is low) to remain enabled.

AC TEST LOADS

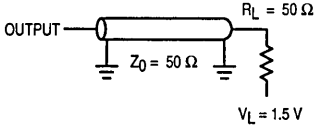


Figure 1A

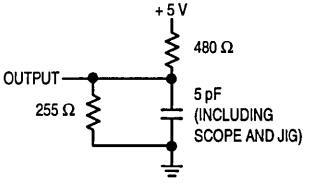
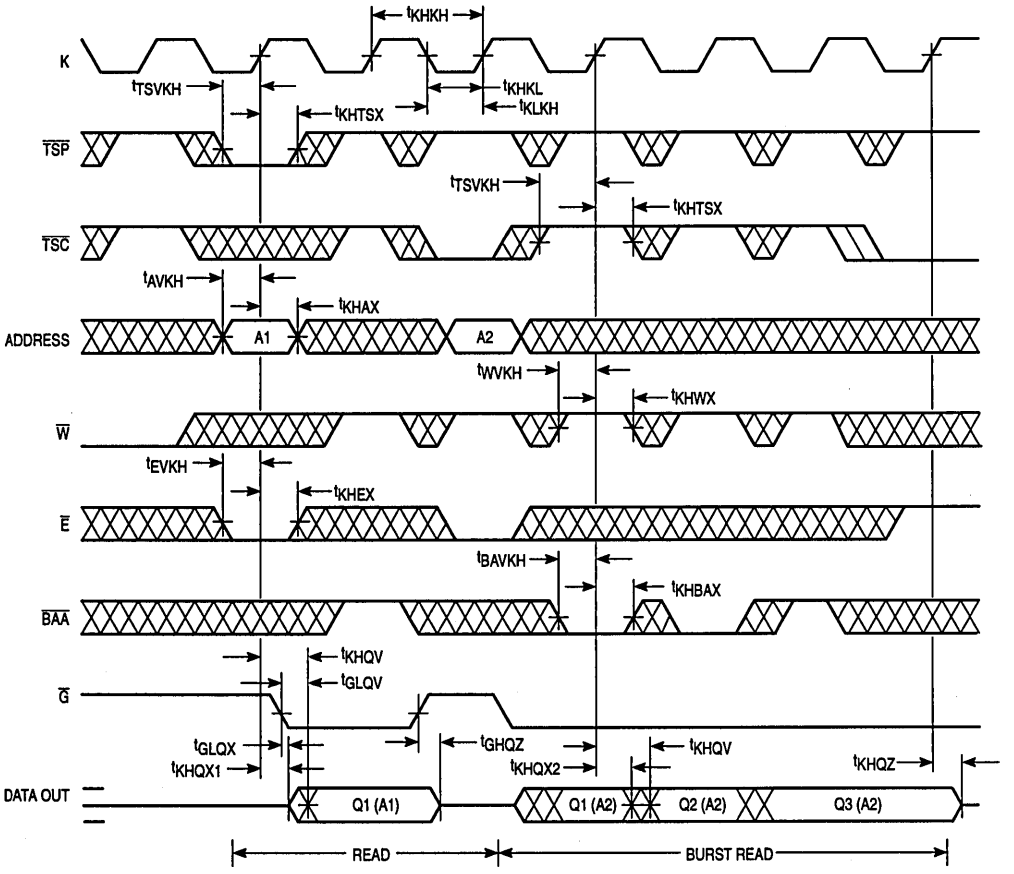


Figure 1B

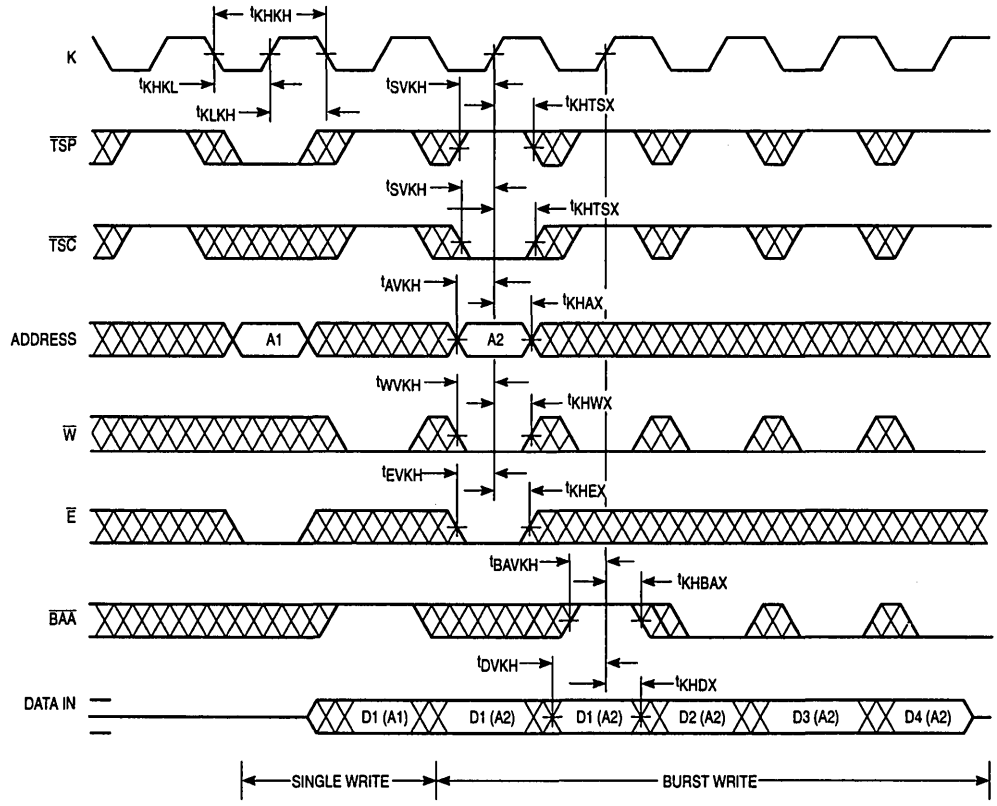
NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLE



NOTE: Q1(A2) represents the first output from the external address A2; Q2(A2) represents the next output data in the burst sequence with A2 as the base address.

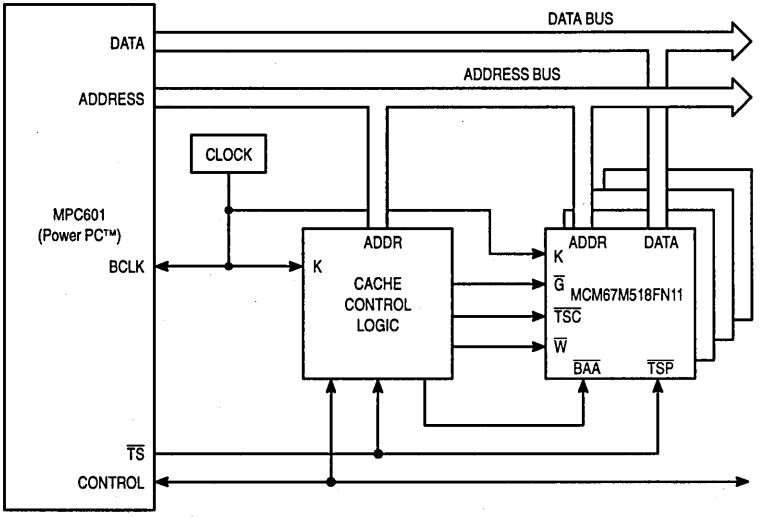
WRITE CYCLE



NOTE: $\overline{G} = V_{IH}$.

4

APPLICATION EXAMPLE



256K Byte Burstable, Secondary Cache
Using Four MCM67M518FN11s with a 66 MHz MPC601 Power PC™

ORDERING INFORMATION
(Order by Full Part Number)

MCM 67M518 X XX

Motorola Memory Prefix

Part Number

Speed (9 – 9 ns, 11 = 11 ns, 14 = 14 ns, 19 = 19 ns)

Package (FN = PLCC)

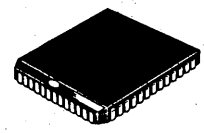
Full Part Numbers — MCM67M518FN9 MCM67M518FN11 MCM67M518FN14 MCM67M518FN19

MCM67W518

Product Preview

32K x 18 Bit Asynchronous Fast Static RAM

With Address Latch Byte Enable



FN PACKAGE
PLASTIC
CASE 778

The MCM67W518 is a 589,824 bit static random access memory organized as 32,768 words of 18 bits, fabricated using Motorola's high-performance silicon-gate BiCMOS technology. The device integrates a 32K x 18 SRAM core with advanced peripheral circuitry consisting of address latches, active low chip enable, write enable, separate upper and lower byte selects, and a fast output enable. This device has increased output drive capability supported by multiple power pins.

Address latch enable (AL) is provided to simplify read and write cycles by guaranteeing address hold time in a simple fashion. When the address latch input is high, the address latch is in the transparent state. If the latch enable is tied high, the device can be used as an asynchronous SRAM. When the address latch enable is low, the address is in the latched state.

Dual byte selects ($\overline{LB}$ and $\overline{UB}$) are provided to allow individually readable and writeable bytes. $\overline{LB}$ controls DQ0 – DQ8 (the lower bits) while $\overline{UB}$ controls DQ9 – DQ17 (the upper bits).

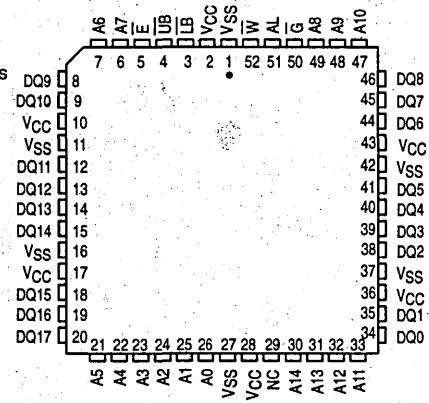
A generous number of power supply pins have been utilized and placed on the package for maximum performance.

The MCM67W518 will be available in a 52-pin plastic leaded chip carrier (PLCC).

This device is ideally suited for systems that require wide data bus widths, cache memory, and as tag RAMs.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 12/15/20 ns Max
- Byte Write and Byte Read Capability
- Transparent Address Latch
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three-State Outputs
- 3.3 V I/O Compatible
- High Board Density 52-Lead PLCC Package

PIN ASSIGNMENT



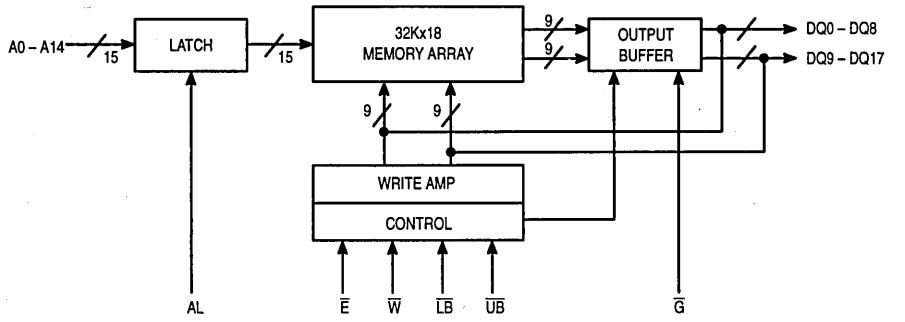
PIN NAMES	
A0 – A14	Address Inputs
AL	Address Latch
$\overline{W}$	Write Enable
$\overline{LB}$	Lower Byte Select
$\overline{UB}$	Upper Byte Select
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

4

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{LB}$	$\overline{UB}$	$\overline{W}$	AL*	$\overline{G}$	Mode	Supply Current	I/O Status
H	X	X	X	X	X	Deselected	I_{SB}	High-Z
L	X	X	X	L	X	Read or Write Using Latched Addresses	I_{CC}	—
L	X	X	X	H	X	Read or Write Using Unlatched Addresses	I_{CC}	—
L	L	L	H	X	L	Read Cycle	I_{CC}	Data Out
L	L	L	H	X	H	Read Cycle	I_{CC}	High-Z
L	L	L	L	X	X	Write Cycle Lower and Upper Byte	I_{CC}	High-Z
L	L	H	L	L	X	Write Cycle Lower Byte with Latched Addresses	I_{CC}	High-Z
L	H	L	H	L	L	Read Cycle Upper Byte	I_{CC}	Data Out

*Addresses must satisfy the specified setup and hold times for the falling edge of AL.
NOTE: This truth table shows the application of all device functions; different combinations are valid.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min)	I_{CCA12} I_{CCA15} I_{CCA20}	— — —	290 275 260	mA
AC Standby Current (E = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0 V and V_{IH} ≥ 3.0 V, f = f_{max})	I_{SB1}	—	75	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V, f = f_{max})	I_{SB2}	—	12	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	C_{out}	6	8	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

READ CYCLE (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67W518-12		MCM67W518-15		MCM67W518-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	12	—	15	—	20	—	ns	4
Access Times:								ns	5
Address Valid to Output Valid	t_{AVQV}	—	12	—	15	—	20		
Chip Enable Low to Output Valid	t_{ELQV}	—	12	—	15	—	20		
AL High to Output Valid	t_{ALHQV}	—	12	—	15	—	20		
Output Enable Low to Output Valid	t_{GLQV}	—	6	—	7	—	8		
Byte Select Low to Output Valid	t_{BLQV}	—	6	—	7	—	8		
Setup Times:								ns	
Address Valid to Address Latch Low	t_{AVALL}	2	—	2	—	2	—		
Address Valid to Address Latch High	t_{AVALH}	0	—	0	—	0	—		
Hold Times:								ns	
Address Latch Low to Address Invalid	t_{ALLAX}	2	—	3	—	3	—		
Output Hold:								ns	
Address Invalid to Output Invalid	t_{AXQX}	4	—	4	—	4	—		
AL High to Output Invalid	t_{ALHQX}	4	—	4	—	4	—		
Address Latch Pulse Width	t_{ALHALL}	5	—	5	—	5	—	ns	
Output Buffer Control:								ns	6
Chip Enable Low to Output Active	t_{ELQX}	3	—	2	—	2	—		
Output Enable Low to Output Active	t_{GLQX}	1	—	1	—	1	—		
Byte Select Low to Output Active	t_{BLQX}	2	—	2	—	2	—		
Chip Enable High to Output High-Z	t_{EHQZ}	2	6	2	9	2	9		
Output Enable High to Output High-Z	t_{GHQZ}	2	6	2	7	2	9		
Byte Select High to Output High-Z	t_{BHQZ}	2	6	2	9	2	9		

NOTES:
1. $\overline{B}$ refers to either or both byte selects ($\overline{LB}$, $\overline{UB}$).
2. Address latch (AL) is high for all asynchronous cycles.
3. A read occurs during the overlap of $\overline{E}$ low, $\overline{W}$ high, and either or both byte enable ($\overline{LB}$, $\overline{UB}$) low.
4. All read cycle timing is referenced from the last valid address to the first transitioning address.
5. Addresses valid prior to or coincident with $\overline{E}$ low.
6. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EHQZ} is less than t_{ELQX} and t_{GHQZ} is less than t_{GLQX} for a given device.

AC TEST LOADS

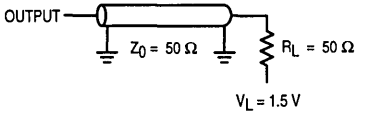


Figure 1A

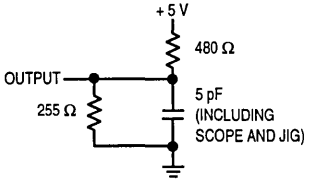
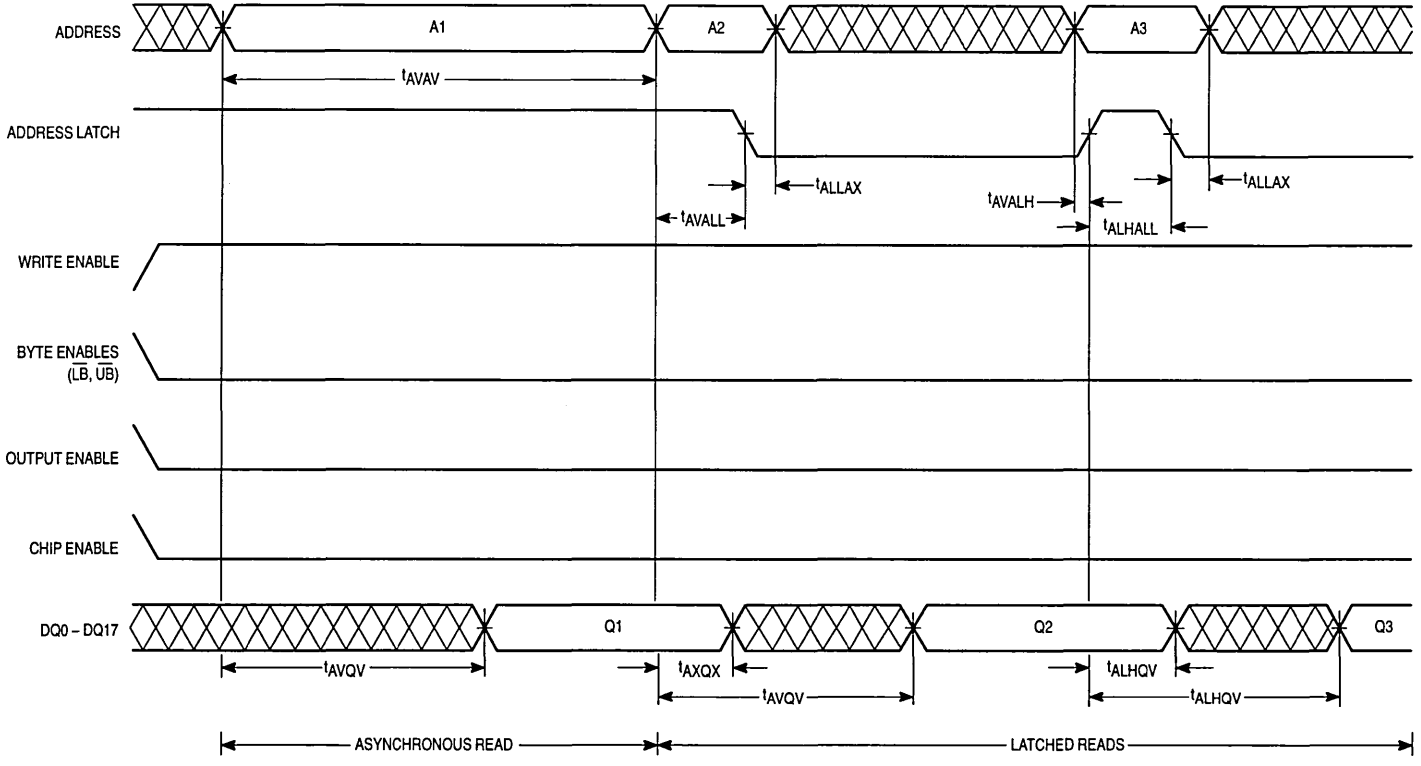


Figure 1B

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLES



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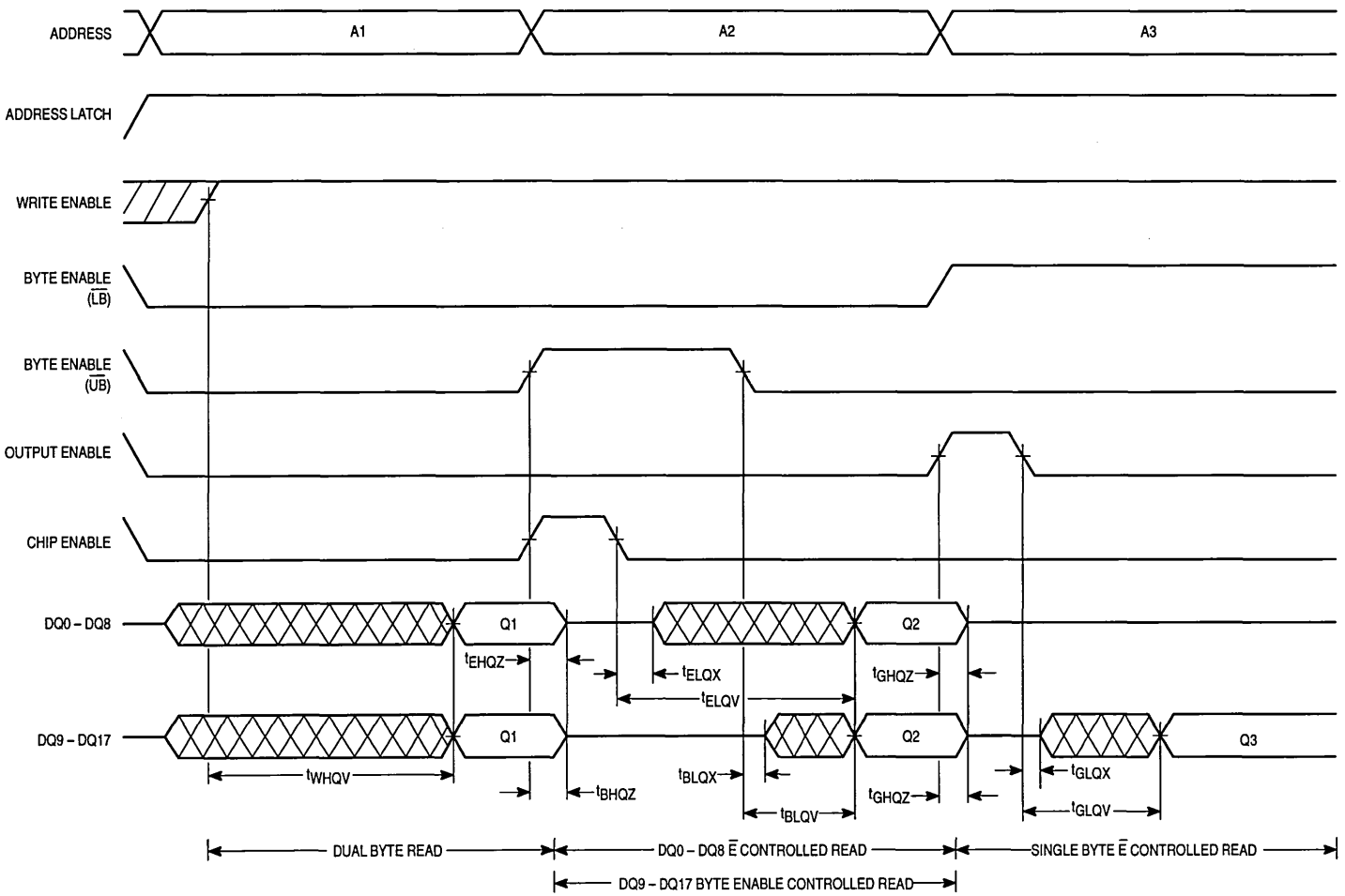
READ CYCLES (Continued)

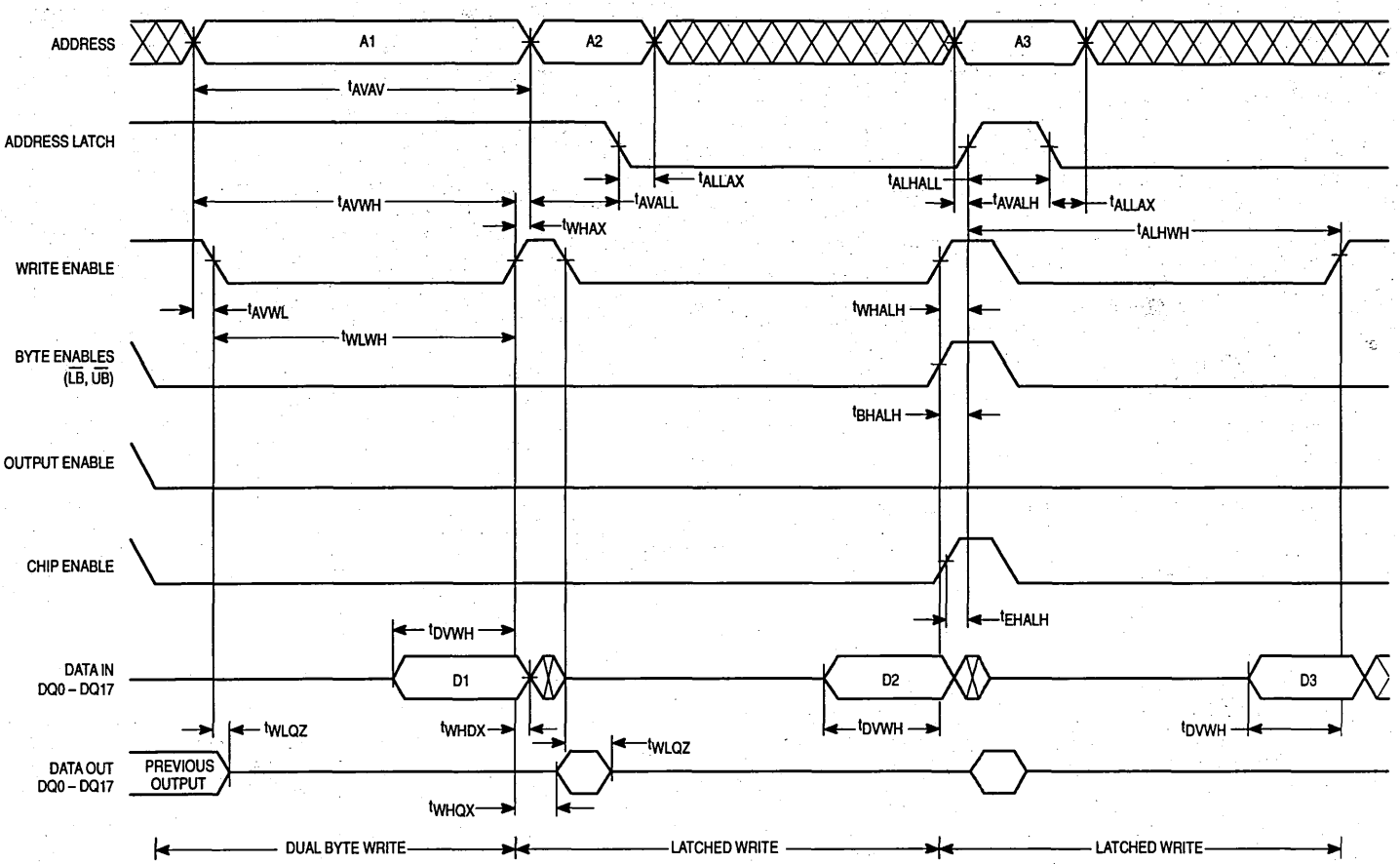


WRITE CYCLE (See Notes 1, 2, 3, and 4)

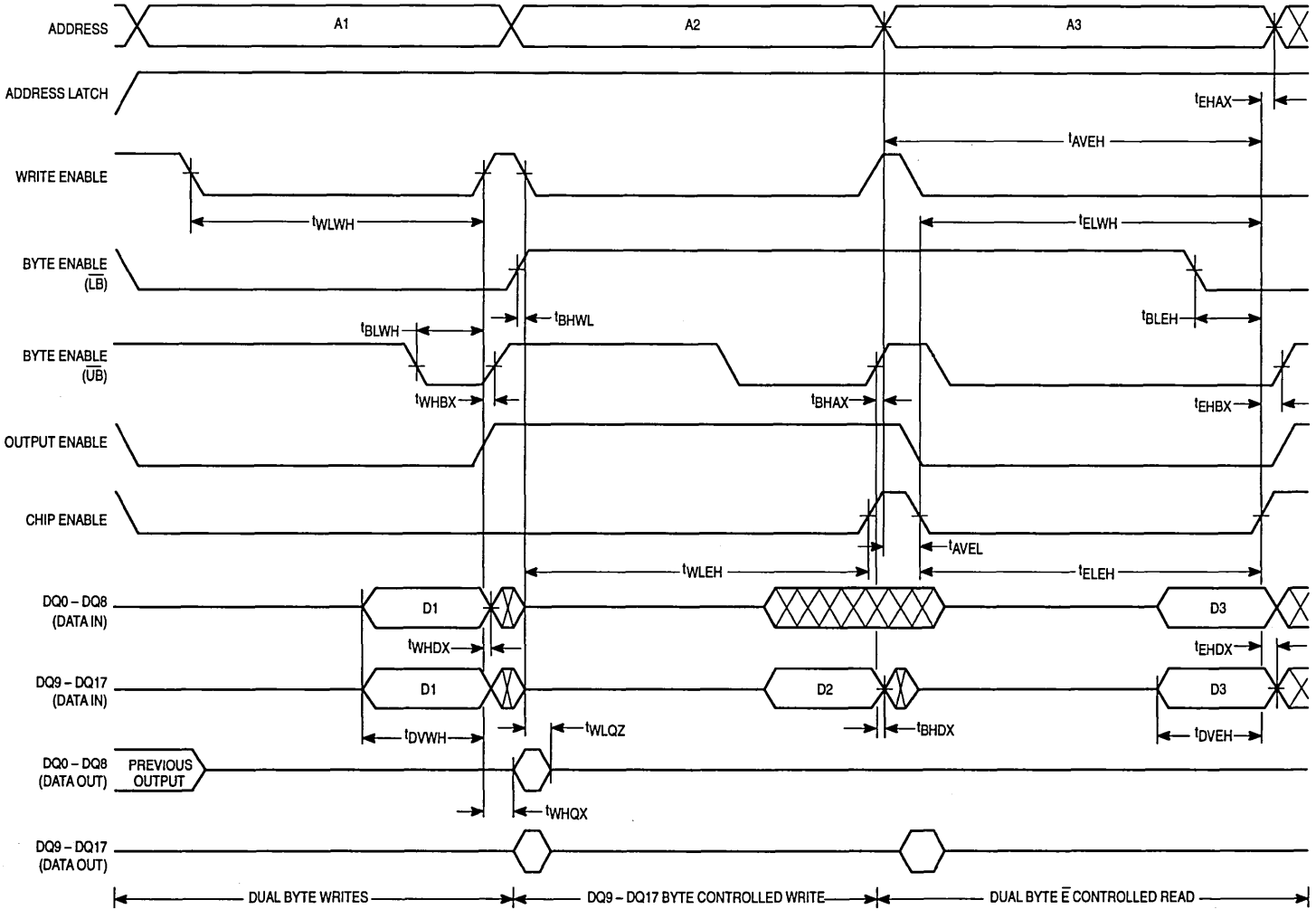
Parameter	Symbol	MCM67W518-12		MCM67W518-15		MCM67W518-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	20	—	ns	5
Setup Times:								ns	
Address Valid to End of Write	t_{AVWH}	8	—	13	—	15	—		
Address Valid to Chip Enable High	t_{AVEH}	8	—	13	—	15	—		
Address Valid to Write Enable Low	t_{AVWL}	0	—	0	—	0	—		
Address Valid to Chip Enable Low	t_{AVEL}	0	—	0	—	0	—		
Data Valid to Write Enable High	t_{DVWH}	6	—	7	—	8	—		
Data Valid to Chip Enable High	t_{DVEH}	6	—	7	—	8	—		
Byte Select Low to Write Enable High	t_{BLWH}	4	—	6	—	8	—		
Byte Select High to Write Enable Low	t_{BHWL}	0	—	0	—	0	—		
Byte Select Low to Chip Enable High	t_{BLEH}	4	—	6	—	8	—		
Address Latch High Write Low	t_{ALHWL}	0	—	0	—	0	—		
Address Valid to Address Latch Low	t_{AVALL}	2	—	2	—	2	—		
Address Valid to Address Latch High	t_{AVALH}	0	—	0	—	0	—		
Hold Times:								ns	
Write Enable High to Address Invalid	t_{WHAX}	0	—	0	—	0	—		
Chip Enable High to Address Invalid	t_{EHAX}	0	—	0	—	0	—		
Byte Select High to Address Invalid	t_{BHAX}	0	—	0	—	0	—		
Write Enable High to Data Invalid	t_{WHDX}	0	—	0	—	0	—		
Chip Enable High to Data Invalid	t_{EHDX}	0	—	0	—	0	—		
Byte Select High to Data Invalid	t_{BHDX}	0	—	0	—	0	—		
Write Enable High to Byte Enable Invalid	t_{WHBX}	2	—	2	—	2	—		
Chip Enable High to Byte Enable Invalid	t_{EHBX}	2	—	2	—	2	—		
Address Latch Low to Address Invalid	t_{ALLAX}	2	—	3	—	3	—		
Write Enable High to Address Latch High	t_{WHALH}	0	—	0	—	0	—		
Byte Select High to Address Latch High	t_{BHALH}	0	—	0	—	0	—		
Write Pulse Width:								ns	
Write Pulse Width ($\overline{G}$ Low)	t_{WLWH}	8	—	13	—	15	—		
Write Pulse Width ($\overline{G}$ High)	t_{WLWH}	7	—	12	—	14	—		
Write Pulse Width	t_{WLEH}	8	—	13	—	15	—		6
Chip Enable to End of Write	t_{ELWH}	8	—	13	—	15	—		7
Chip Enable to End of Write	t_{ELEH}	8	—	13	—	15	—		6, 7
Address Latch High to Write Enable High	t_{ALHWH}	8	—	13	—	15	—		
Address Latch Pulse Width	t_{ALHALL}	5	—	5	—	5	—	ns	
Output Buffer Control:								ns	
Write Enable High to Output Active	t_{WHQX}	3	—	5	—	5	—		8
Write Enable Low to Output High-Z	t_{WLQZ}	0	6	0	9	0	9		8, 9

NOTES:
1. $\overline{B}$ refers to either or both byte selects ($\overline{LB}$, $\overline{UB}$).
2. Address latch (AL) is high for all asynchronous cycles.
3. A write occurs during the overlap of $\overline{E}$ low, $\overline{W}$ low, and either or both byte enable ($\overline{LB}$, $\overline{UB}$) low.
4. Write enable must be equal to V_{IH} for all address transitions.
5. All write cycle timing is referenced from the last valid address to the first transitioning address.
6. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
7. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
8. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
9. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EHQZ} is less than t_{ELQX} and t_{GHQZ} is less than t_{GLQX} for a given device.

WRITE CYCLES



WRITE CYCLES (Continued)



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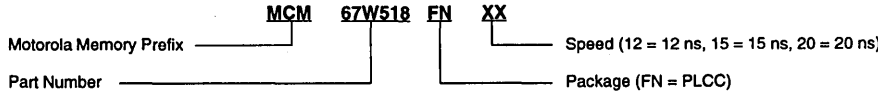
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM67W518FN12 MCM67W518FN15 MCM67W518FN20

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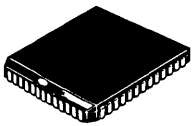
MCM67A618

Product Preview

64K x 18 Bit Asynchronous/Latched Address Fast Static RAM



FN PACKAGE
PLASTIC
CASE 778

The MCM67A618 is a 1,179,648 bit latched address static random access memory organized as 65,536 words of 18 bits, fabricated with Motorola's high-performance silicon-gate BiCMOS technology. The device integrates a 64K x 18 SRAM core with advanced peripheral circuitry consisting of address and data input latches, active low chip enable, separate upper and lower byte write strobes, and a fast output enable. This device has increased output drive capability supported by multiple power pins.

Address, data in, and chip enable latches are provided. When latch enables (AL for address and chip enables and DL for data in) are high, the address, data in, and chip enable latches are in the transparent state. If latch enables are tied high the device can be used as an asynchronous SRAM. When latch enables are low the address, data in, and chip enable latches are in the latched state. This input latch simplifies read and write cycles by guaranteeing address and data-in hold time in a simple fashion.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits) while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

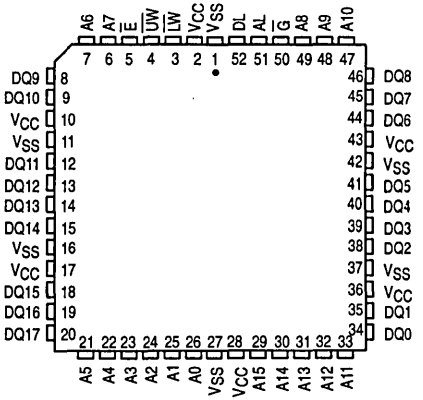
Additional power supply pins have been utilized and placed on the package for maximum performance.

The MCM67A618 will be available in a 52-pin plastic leaded chip carrier (PLCC).

This device is ideally suited for systems which require wide data bus widths, cache memory, and tag RAMs.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 12/15/20 ns Max
- Byte Writeable via Dual Write Enables
- Separate Data Input Latch for Simplified Write Cycles
- Address and Chip Enable Input Latches
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three-State Outputs
- 3.3 V I/O Compatible
- High Board Density 52-Lead PLCC Package

PIN ASSIGNMENT

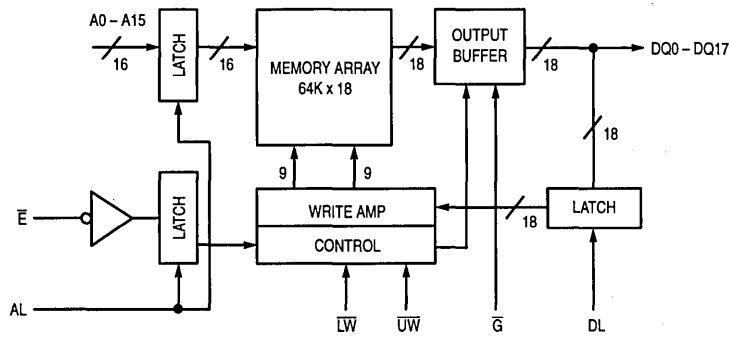


PIN NAMES	
A0 – A15	Address Inputs
AL	Address Latch
DL	Data Latch
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Higher Byte Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{LW}$	$\overline{UW}$	AL*	DL*	$\overline{G}$	Mode	Supply Current	I/O Status
H	X	X	X	X	X	Deselected Cycle	I_{SB}	High-Z
L	X	X	L	X	X	Read or Write Using Latched Addresses	I_{CC}	—
L	X	X	H	X	X	Read or Write Using Unlatched Addresses	I_{CC}	—
L	H	H	X	X	L	Read Cycle	I_{CC}	Data Out
L	H	H	X	X	H	Read Cycle	I_{CC}	High-Z
L	L	L	X	L	X	Write Both Bytes Using Latched Data In	I_{CC}	High-Z
L	L	L	X	H	X	Write Both Bytes Using Unlatched Data In	I_{CC}	High-Z
L	L	H	X	X	X	Write Cycle, Lower Byte	I_{CC}	High-Z
L	H	L	X	X	X	Write Cycle, Lower Byte	I_{CC}	High-Z

*$\overline{E}$ and Addresses satisfy the specified setup and hold times for the falling edge of AL. Data-in satisfies the specified setup and hold times for falling edge of DL.

NOTE: This truth table shows the application of each function. Combinations of these functions are valid.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0, Cycle Time ≥ t_{AVAV} min)	I_{CCA12} I_{CCA15} I_{CCA20}	—	290 275 260	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, f = f_{max})	I_{SB1}	—	75	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V, f = f_{max})	I_{SB2}	—	12	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

4

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1 Unless Otherwise Noted

ASYNCHRONOUS READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM67A618-12		MCM67A618-15		MCM67A618-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	12	—	15	—	20	—	ns	3
Access Times:								ns	4
Address Valid to Output Valid	t_{AVQV}	—	12	—	15	—	20		
$\overline{E}$ Low to Output Valid	t_{ELQV}	—	12	—	15	—	20		
Output Enable Low to Output Valid	t_{GLQV}	—	6	—	7	—	8		
Output Hold from Address Change	t_{AXQX}	4	—	4	—	4	—	ns	
Output Buffer Control:								ns	5
$\overline{E}$ Low to Output Active	t_{ELQX}	3	—	2	—	2	—		
$\overline{G}$ Low to Output Active	t_{GLQX}	1	—	1	—	1	—		
$\overline{E}$ High to Output High-Z	t_{EHQZ}	2	6	2	9	2	9		
$\overline{G}$ High to Output High-Z	t_{GHQZ}	2	6	2	7	2	9		
Power Up Time	t_{ELICCA}	0	—	0	—	0	—	ns	

NOTES:
1. AL and DL are equal to V_{IH} for all asynchronous cycles.
2. Both Write Enable signals ($\overline{LW}$, $\overline{UW}$) are equal to V_{IH} for all read cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EHQZ} is less than t_{ELQX} and t_{GHQZ} is less than t_{GLQX} for a given device.

AC TEST LOADS

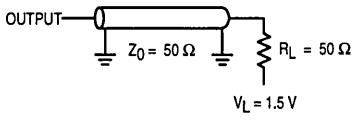


Figure 1A

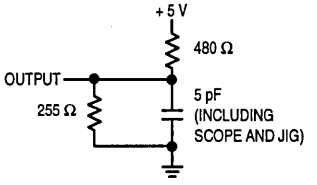
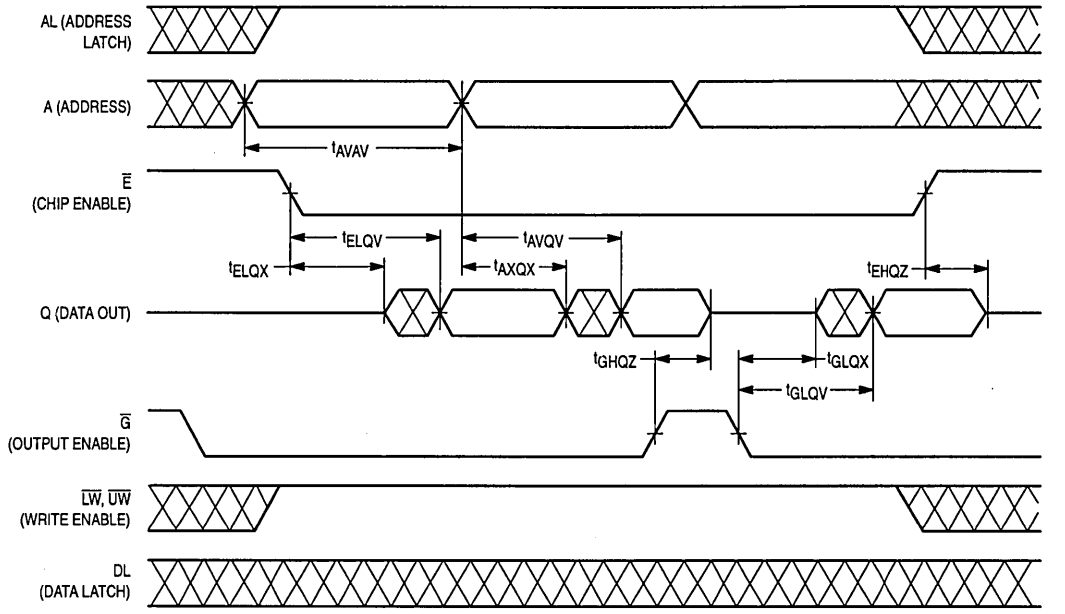


Figure 1B

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

ASYNCHRONOUS READ CYCLES



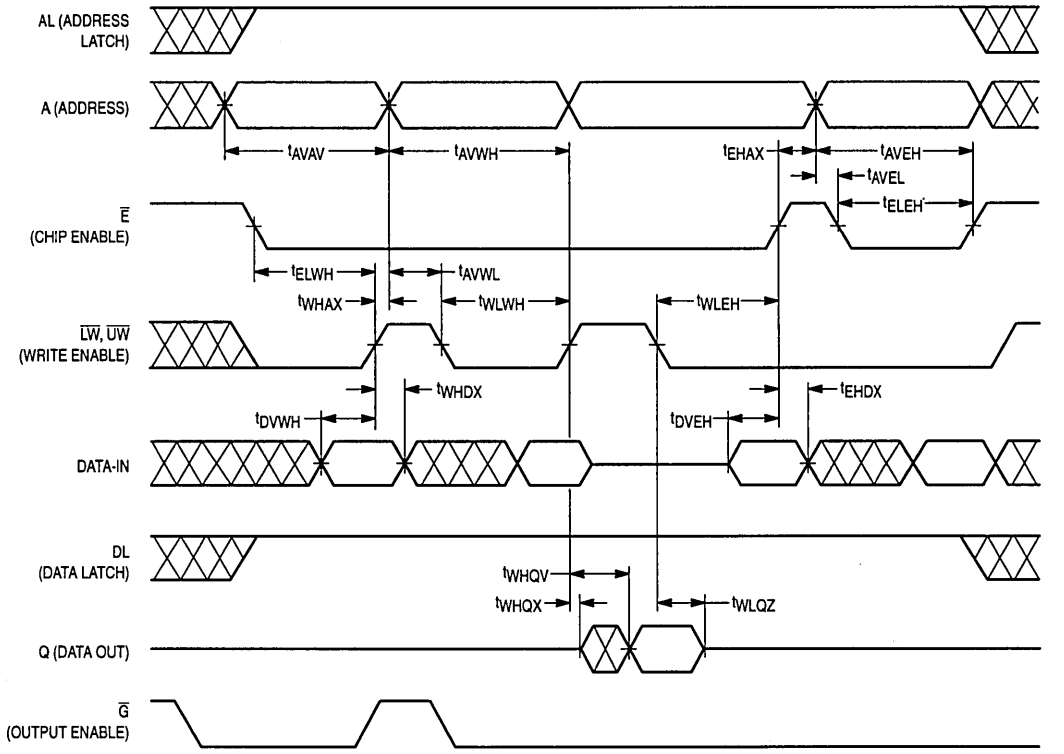
4

ASYNCHRONOUS WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67A618-12		MCM67A618-15		MCM67A618-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times	t_{AVAV}	12	—	15	—	20	—	ns	4
Setup Times:								ns	
Address Valid to End of Write	t_{AVWH}	8	—	13	—	15	—		
Address Valid to $\overline{E}$ High	t_{AVEH}	8	—	13	—	15	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—		
Address Valid to $\overline{E}$ Low	t_{AVEL}	0	—	0	—	0	—		
Address Valid to $\overline{W}$ High	t_{DVWH}	6	—	7	—	8	—		
Data Valid $\overline{E}$ High	t_{DVEH}	6	—	7	—	8	—		
Hold Times:								ns	
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—		
$\overline{E}$ High to Address Invalid	t_{EHAX}	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—		
$\overline{E}$ High to Data Invalid	t_{EHDX}	0	—	0	—	0	—		
Write Pulse Width:								ns	
Write Pulse Width ($\overline{G}$ Low)	t_{WLWH}	8	—	13	—	15	—		
Write Pulse Width ($\overline{G}$ High)	t_{WLWH}	7	—	12	—	14	—		
Write Pulse Width	t_{WLEF}	8	—	13	—	15	—		5
Enable to End of Write	t_{ELWH}	8	—	13	—	15	—		6
Enable to End of Write	t_{ELEH}	8	—	13	—	15	—		5, 6
Output Buffer Control:								ns	
$\overline{W}$ High to Output Valid	t_{WHQV}	12	—	15	—	20	—		
$\overline{W}$ High to Output Active	t_{WHQX}	3	—	5	—	5	—		7
$\overline{W}$ Low to Output High-Z	t_{WLQZ}	0	6	0	9	0	9		7, 8

NOTES:
1. $\overline{W}$ refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).
2. AL and DL are equal to V_{IH} for all asynchronous cycles.
3. Both Write Enables must be equal to V_{IH} for all address transitions.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
6. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
7. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
8. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.

ASYNCHRONOUS WRITE CYCLE



4

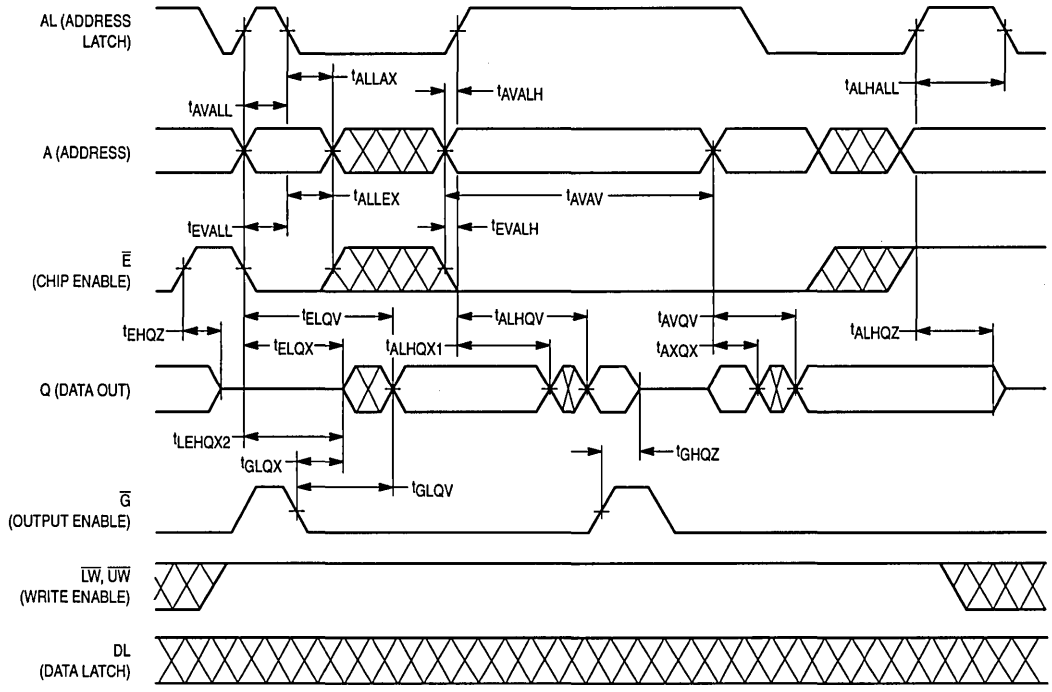
LATCHED READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM67A618-12		MCM67A618-15		MCM67A618-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	12	—	15	—	20	—	ns	3
Access Times:								ns	
Address Valid to Output Valid	t_{AVQV}	—	12	—	15	—	20		
$\overline{E}$ Low to Output Valid	t_{ELQV}	—	12	—	15	—	20		3
AL High to Output Valid	t_{ALHQV}	—	12	—	15	—	20		4
Output Enable Low to Output Valid	t_{GLQV}	—	6	—	7	—	8		
Setup Times:								ns	
Address Valid to AL Low	t_{AVALL}	2	—	2	—	2	—		4
$\overline{E}$ Valid to AL Low	t_{EVALL}	2	—	2	—	2	—		4
Address Valid to AL High	t_{AVALH}	0	—	0	—	0	—		
$\overline{E}$ Valid to AL High	t_{EVALH}	0	—	0	—	0	—		
Hold Times:								ns	4
AL Low to Address Invalid	t_{ALLAX}	2	—	3	—	3	—		
AL Low to $\overline{E}$ Invalid	t_{ALLEX}	2	—	3	—	3	—		
Output Hold:								ns	
Address Invalid to Output Invalid	t_{AXQX}	4	—	4	—	4	—		
AL High to Output Invalid	t_{ALHQX1}	4	—	4	—	4	—		
Address Latch Pulse Width	t_{ALHALL}	5	—	5	—	5	—	ns	
Output Buffer Control:								ns	5
$\overline{E}$ Low to Output Active	t_{ELQX}	3	—	2	—	2	—		
$\overline{G}$ Low to Output Active	t_{GLQZ}	1	—	1	—	1	—		
AL High to Output Active	t_{ALHQX2}	3	—	2	—	2	—		
$\overline{E}$ High to Output High-Z	t_{EHQZ}	2	6	2	9	2	10		
AL High to Output High-Z	t_{ALHQZ}	2	6	2	9	2	10		
$\overline{G}$ High to Output High-Z	t_{GHQZ}	2	6	2	7	2	8		

NOTES:

1. Both Write Enable Signals ($\overline{LW}$, $\overline{UW}$) are equal to V_{IH} for all read cycles.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of address latch (AL) and data latch (DL).
5. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EHQZ} is less than t_{ELQX} and t_{LEHQZ} is less than t_{LEHQX2} and t_{GHQZ} is less than t_{GLQX} for a given device.

LATCHED READ CYCLES



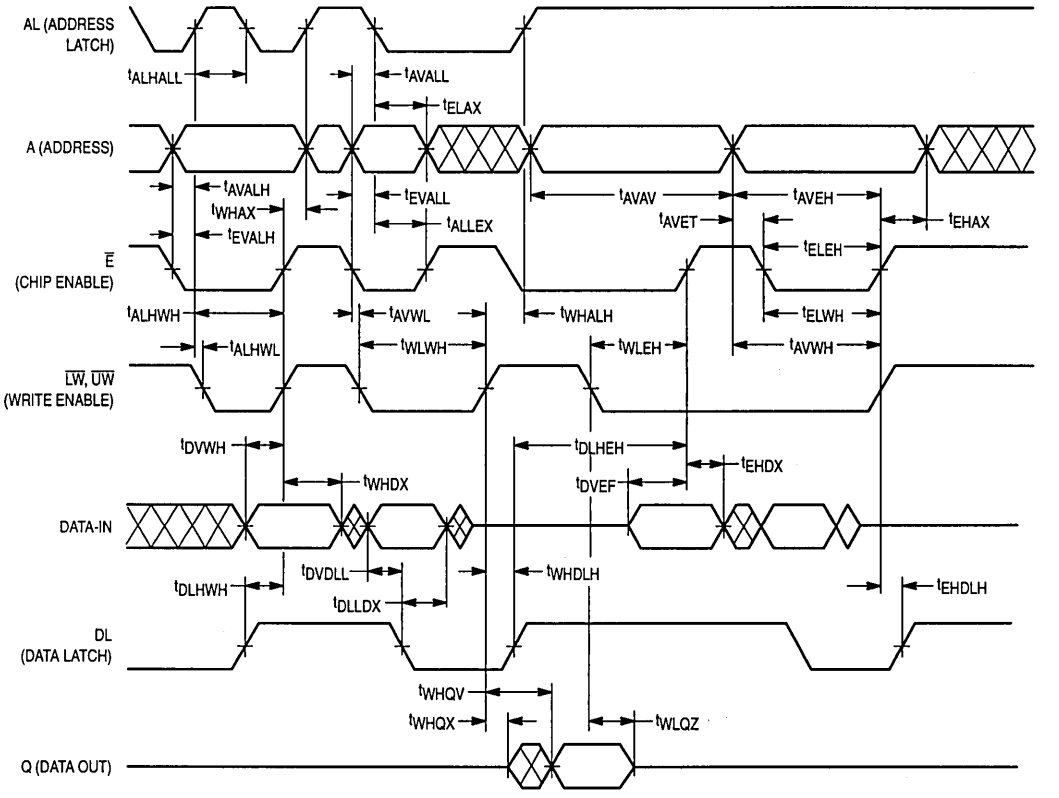
4

LATCHED WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67A618-12		MCM67A618-15		MCM67A618-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Times: Address Valid to Address Valid	t_{AVAV}	12	—	15	—	20	—	ns	4
Setup Times:								ns	
Address Valid to End of Write	t_{AVWH}	8	—	13	—	15	—		
Address Valid to End of Write	t_{AVEH}	8	—	13	—	15	—		
$\overline{E}$ Valid to AL Low	t_{EVALL}	2	—	2	—	2	—		
Address Valid to AL Low	t_{AVALL}	2	—	2	—	2	—		
$\overline{E}$ Valid to AL High	t_{EVALH}	0	—	0	—	0	—		
Address Valid to AL High	t_{AVALH}	0	—	0	—	0	—		
AL High to $\overline{W}$ Low	t_{ALHWL}	0	—	0	—	0	—		
Address Valid to $\overline{W}$ Low	t_{AVWL}	0	—	0	—	0	—		
Address Valid to $\overline{E}$ Low	t_{AVEL}	0	—	0	—	0	—		
Data Valid to DL Low	t_{DVDLL}	2	—	2	—	2	—		
Data Valid to $\overline{W}$ High	t_{DVWH}	6	—	7	—	8	—		
Data Valid to $\overline{E}$ High	t_{DVEH}	6	—	7	—	8	—		
DL High to $\overline{W}$ High	t_{DLHWH}	6	—	7	—	8	—		
DL High to $\overline{E}$ High	t_{DLHEH}	6	—	7	—	8	—		
Hold Times:								ns	
AL Low to $\overline{E}$ Invalid	t_{ALLEX}	2	—	3	—	3	—		4
AL Low to Address Invalid	t_{ALLAX}	2	—	3	—	3	—		4
DL Low to Data Invalid	t_{DLLDX}	2	—	3	—	3	—		
$\overline{W}$ High to Address Invalid	t_{WHAX}	0	—	0	—	0	—		
$\overline{E}$ High to Address Invalid	t_{EHAX}	0	—	0	—	0	—		
$\overline{W}$ High to Data Invalid	t_{WHDX}	0	—	0	—	0	—		
$\overline{E}$ High to Data Invalid	t_{EHDX}	0	—	0	—	0	—		
$\overline{W}$ High to DL High	t_{WHDLH}	0	—	0	—	0	—		
$\overline{E}$ High to DL High	t_{EFDLH}	0	—	0	—	0	—		
$\overline{W}$ High to AL High	t_{WHALH}	0	—	0	—	0	—		
Write Pulse Width:								ns	
AL High to $\overline{W}$ High	t_{ALHWH}	8	—	13	—	15	—		5
Write Pulse Width ($\overline{G}$ Low)	t_{WLWH}	8	—	13	—	15	—		
Write Pulse Width ($\overline{G}$ High)	t_{WLWH}	7	—	12	—	14	—		
Write Pulse Width	t_{WLEH}	8	—	13	—	15	—		6
Enable to End of Write	t_{ELWH}	8	—	13	—	15	—		7
Enable to End of Write	t_{ELEH}	8	—	13	—	15	—		6, 7
Address Latch Pulse Width	t_{ALHALL}	12	—	15	—	20	—	ns	4
Output Buffer Control:								ns	
$\overline{W}$ High to Output Valid	t_{WHQV}	12	—	15	—	20	—		
$\overline{W}$ High to Output Active	t_{WHQX}	3	—	5	—	5	—		8
$\overline{W}$ Low to Output High-Z	t_{WLQZ}	0	6	0	9	0	9		8, 9

NOTES:
1. $\overline{W}$ refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).
2. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
3. Both Write Enables must be equal to V_{IH} for all address transitions.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. All latched inputs must meet the specified setup and hold times with stable logic levels for ALL falling edges of address latch (AL) and data latch (DL).
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
7. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.
8. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{WLQZ} is less than t_{WHQX} for a given device.
9. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low the output will remain in a high impedance state.

LATCHED WRITE CYCLES



ORDERING INFORMATION
(Order by Full Part Number)

MCM 67A618 X XX

- MCM — Motorola Memory Prefix
- 67A618 — Part Number
- X — Package (FN = PLCC)
- XX — Speed (12 = 12 ns, 15 = 15 ns, 20 = 20 ns)

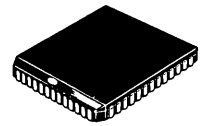
Full Part Numbers — MCM67A618FN12 MCM67A618FN15 MCM67A618FN20

MCM67B618

Product Preview

64K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Self-Timed Write



FN PACKAGE
PLASTIC
CASE 778

The MCM67B618 is a 1,179,648 bit synchronous fast static random access memory designed to provide a burstable, high-performance, secondary cache for the i486 and Pentium™ microprocessors. It is organized as 65,536 words of 18 bits, fabricated with Motorola's high-performance silicon-gate BiCMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A15), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive-edge-triggered noninverting registers.

Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67B618 (burst sequence imitates that of the i486 and Pentium) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

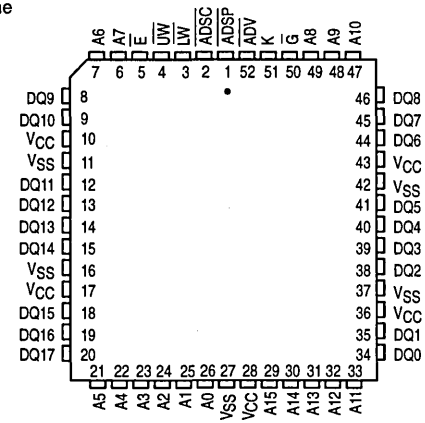
Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 9/12/18 ns Max
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Internally Self-Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52-Lead PLCC Package

PIN ASSIGNMENT

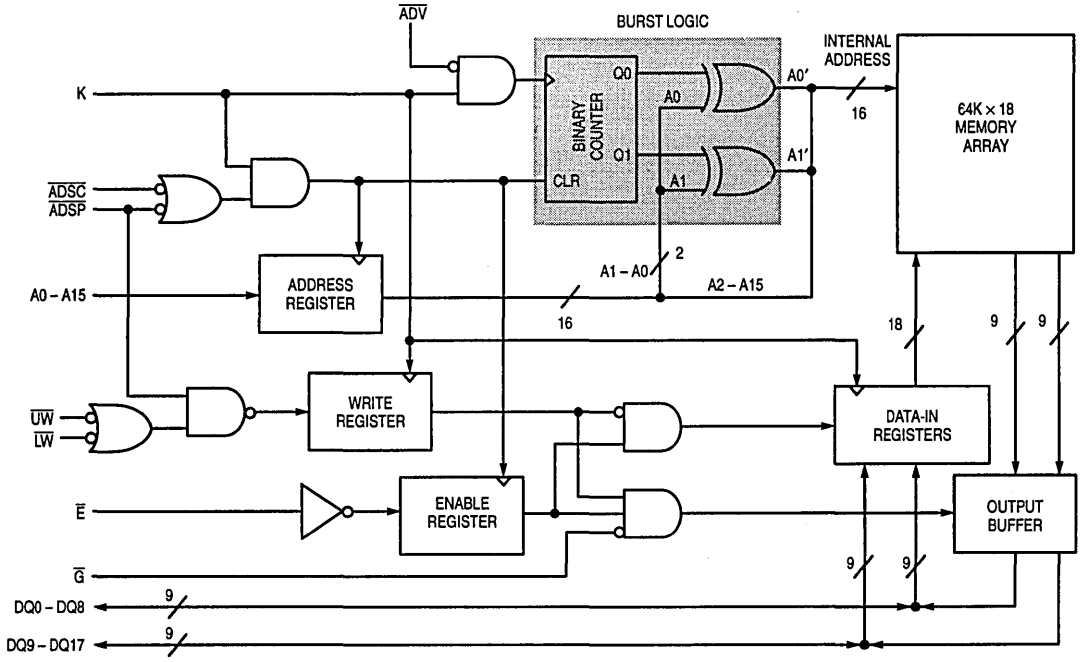


PIN NAMES	
A0 – A15	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

BurstRAM is a trademark of Motorola, Inc.
i486 and Pentium are trademarks of Intel Corp.

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive-edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{A0}$
2nd Burst Address	A15 – A2	$\overline{A1}$	A0
3rd Burst Address	A15 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	L	X	X	X	L-H	N/A	Deselected
H	X	L	X	X	L-H	N/A	Deselected
L	L	X	X	X	L-H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High-Z
Write	X	High-Z — Data In
Deselected	X	High-Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	− 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{bias}	− 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	− 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min) I_{CCA9} I_{CCA12} I_{CCA18}		—	 275 250 225	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	75	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486 and Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3) ($\overline{W}$ refers to either or both byte write enables)

Parameter	Symbol		MCM67B618-9		MCM67B618-12		MCM67B618-18		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	t_{CYC}	15	—	20	—	30	—	ns	
Clock Access Time	t_{KHQV}	t_{CD}	—	9	—	12	—	18	ns	4
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	5	—	6	—	7	ns	
Clock High to Output Active	t_{KHQX1}	t_{DC1}	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	t_{DC2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{OHZ}	2	6	2	7	2	7	ns	5
Clock High to Q High-Z	t_{KHQZ}	t_{CZ}	—	6	—	6	—	6	ns	
Clock High Pulse Width	t_{KHKL}	t_{CH}	5	—	6	—	7	—	ns	
Clock Low Pulse Width	t_{KLKH}	t_{CL}	5	—	6	—	7	—	ns	
Setup Times: Address	t_{AVKH}	t_{AS}	2.5	—	2.5	—	3.0	—	ns	6
Address Status	t_{ADSVKH}	t_{SS}								
Data In	t_{DVKH}	t_{DS}								
Write	t_{WVKH}	t_{WS}								
Address Advance	t_{ADVVKH}									
Chip Enable	t_{EVKH}									
Hold Times: Address	t_{KHAX}	t_{AH}	0.5	—	0.5	—	0.5	—	ns	6
Address Status	t_{KHADSX}	t_{SH}								
Data In	t_{KHDX}	t_{DH}								
Write	t_{KHWX}	t_{WH}								
Address Advance	t_{KHADVX}									
Chip Enable	t_{KHEX}									

NOTES:
1. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
4. Maximum access times are guaranteed for all possible i486 external bus cycles.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled.Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

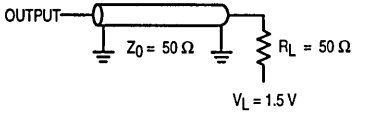


Figure 1A

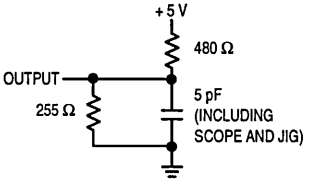
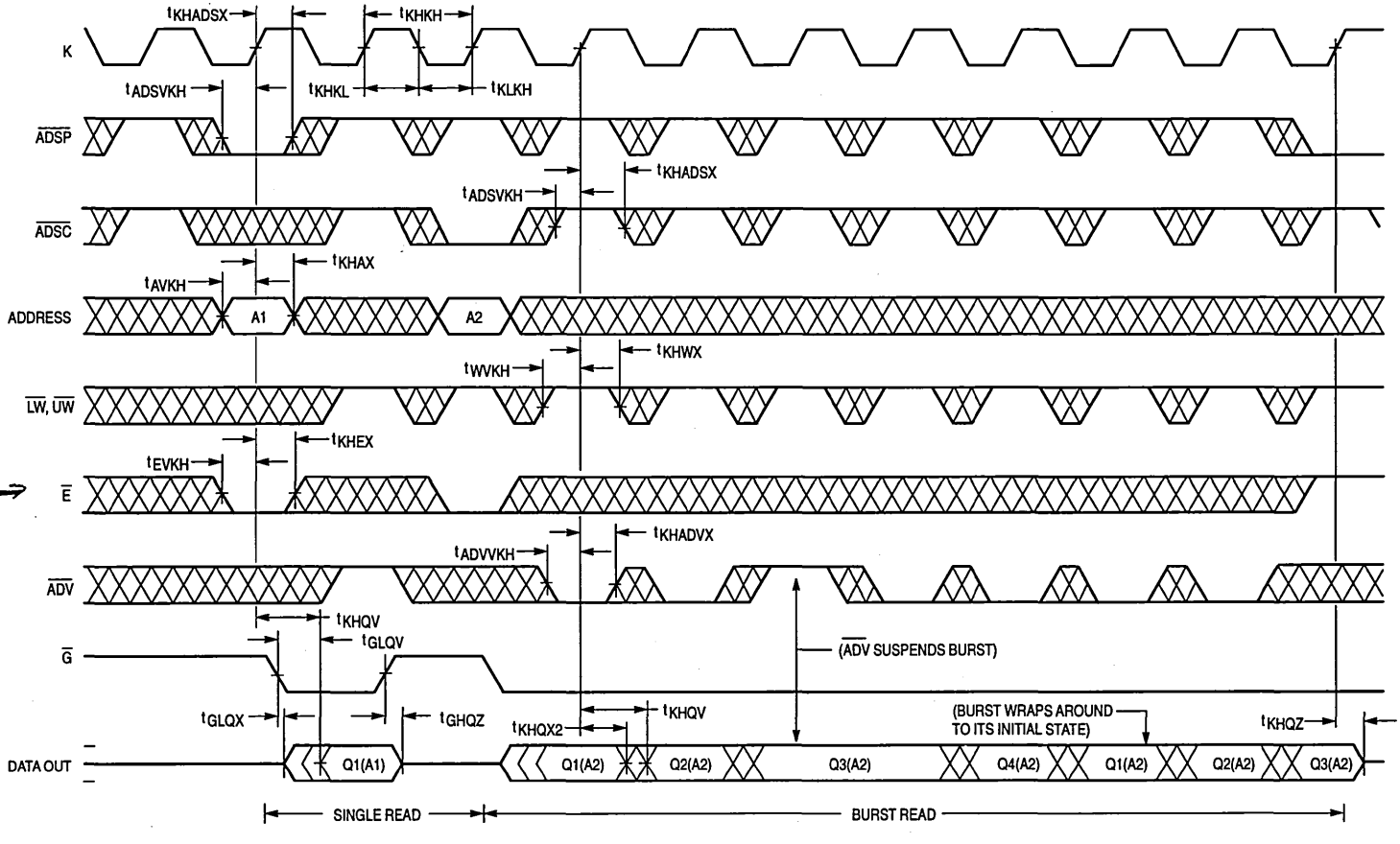


Figure 1B

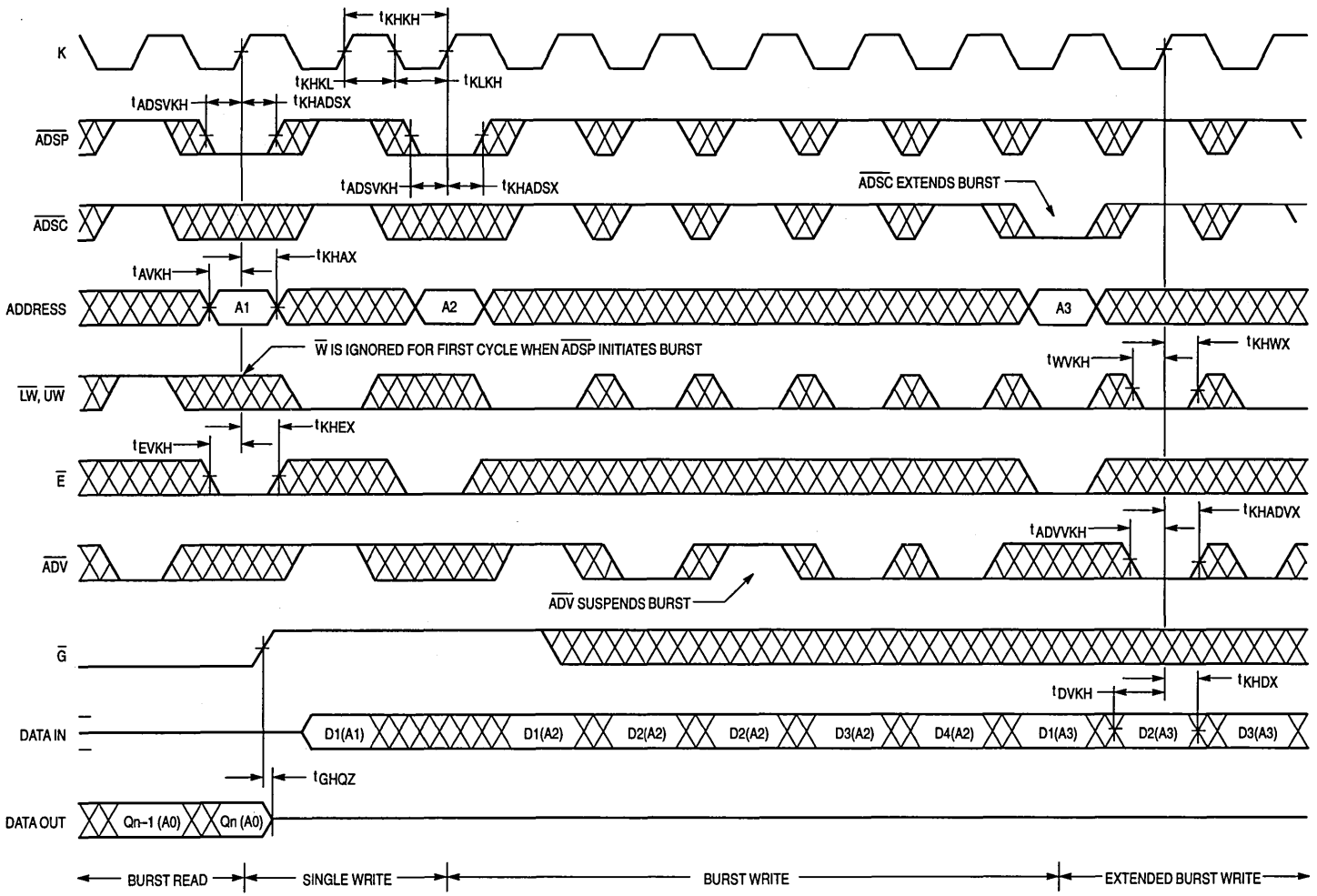
NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLES

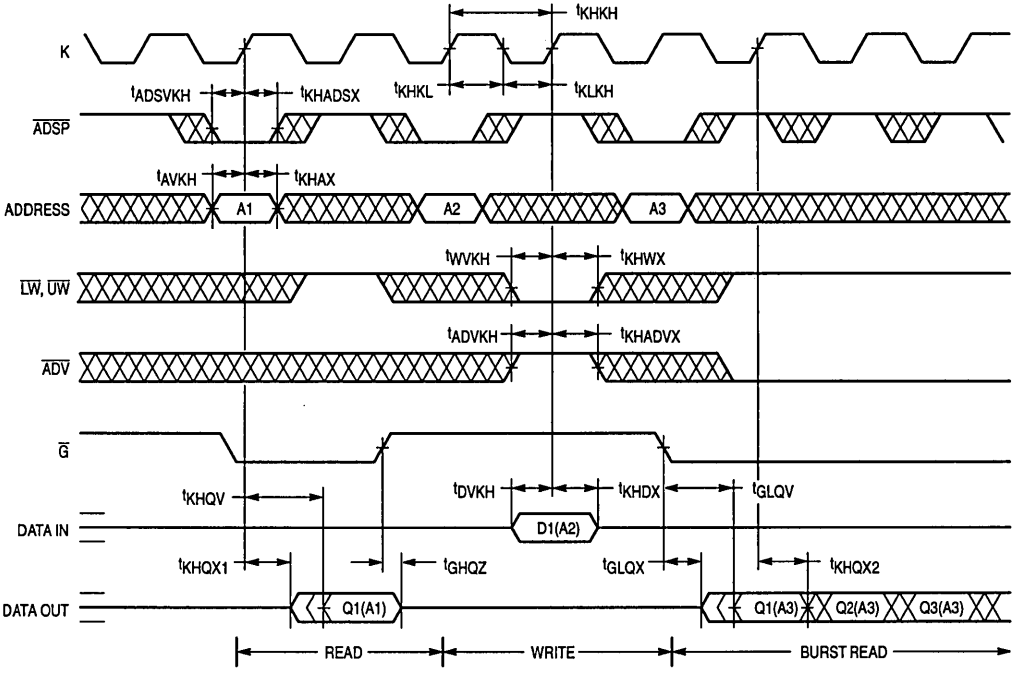


NOTE: Q1(A2) represents the first output data from the base address A2; Q2(A2) represents the next output data in the burst sequence with A2 as the base address.

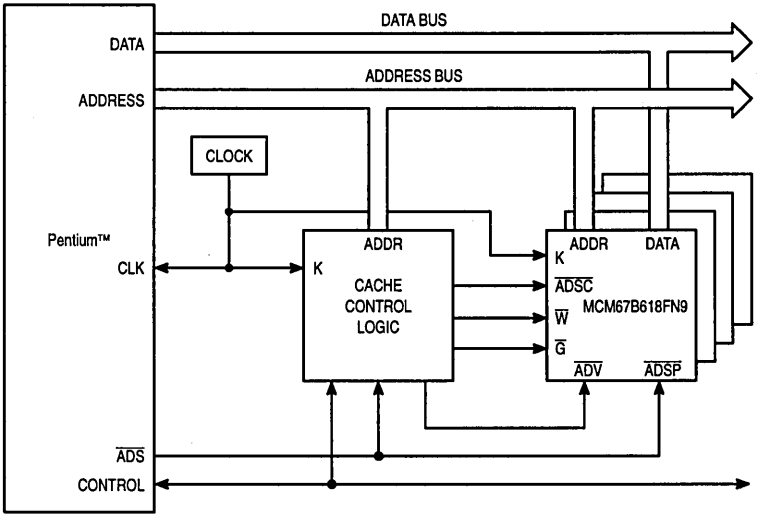
WRITE CYCLES



COMBINATION READ/WRITE CYCLE



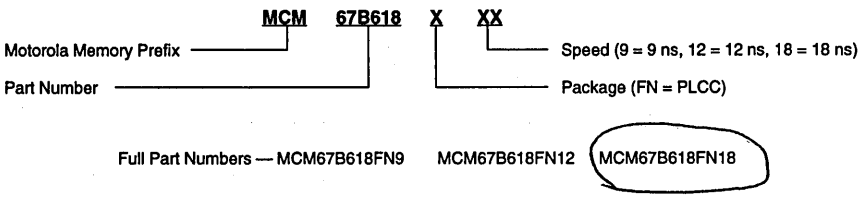
APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache
Using Four MCM67B618FN9s with a 66 MHz Pentium

Figure 2

ORDERING INFORMATION
(Order by Full Part Number)



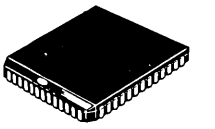
Full Part Numbers — MCM67B618FN9 MCM67B618FN12 MCM67B618FN18

MCM67C618

Product Preview

64K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Registered Outputs



FN PACKAGE
PLASTIC
CASE 778

The MCM67C618 is a 1,179,648 bit synchronous static random access memory designed to provide a burstable, high-performance, secondary cache for the i486 and Pentium™ microprocessors. It is organized as 65,536 words of 18 bits, fabricated with Motorola's high-performance silicon-gate BiCMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive registered output drivers onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A15), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive-edge-triggered noninverting registers.

This device contains output registers for pipeline operations. At the rising edge of K, the RAM provides the output data from the previous cycle.

Output enable ($\overline{G}$) is asynchronous for maximum system design flexibility.

Burst can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67C618 (burst sequence imitates that of the i486) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

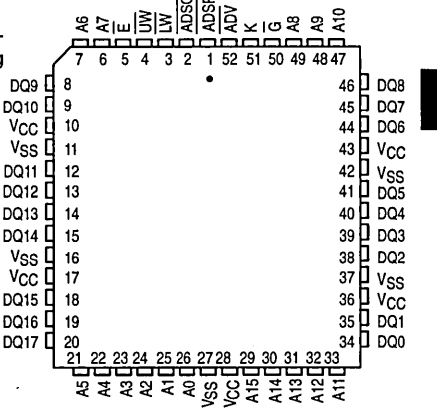
This device also incorporates pass-thru functionality. A read cycle preceded by a write cycle will cause the the data written into the array to appear at the outputs on the same clock cycle on which the read was initiated. The clock high to data valid time is the same as that of a standard read operation. Chip enable ($\overline{E}$) does not have to be asserted to receive valid data during a pass-thru operation. Output enable ($\overline{G}$) maintains control of the output buffers during a pass-thru operation.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Time/Fast Cycle Time = 7 ns/80 MHz, 9 ns/66 MHz
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Output Registers for Pipelined Applications
- Internally Self-Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Write Pass-Thru Capability
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52-Lead PLCC Package

PIN ASSIGNMENT



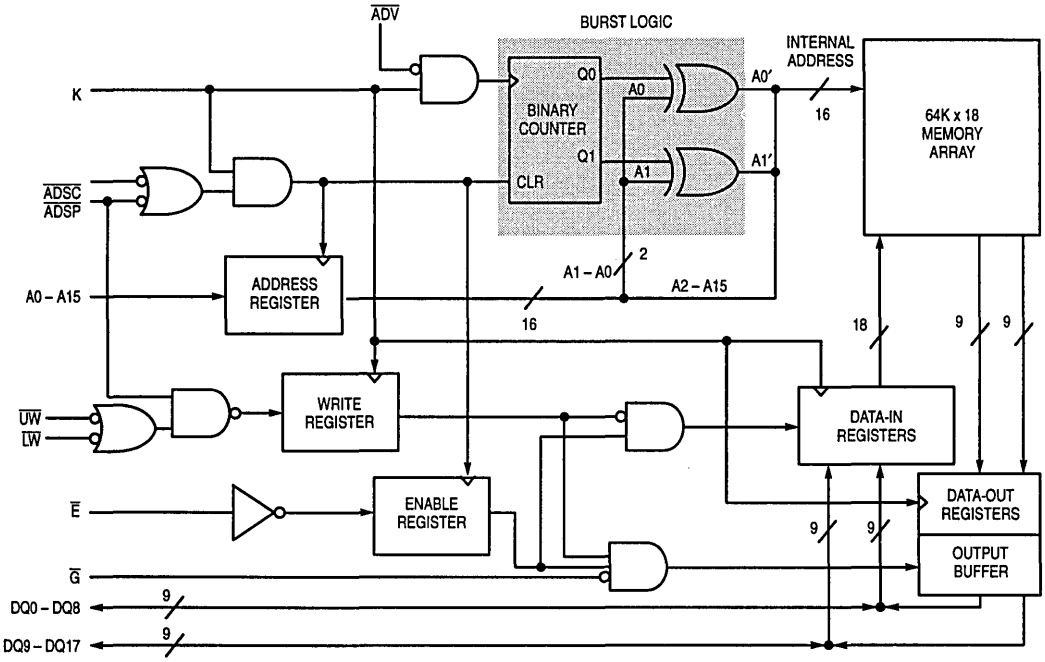
PIN NAMES

A0 – A15	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
VCC	+ 5 V Power Supply
VSS	Ground

All power supply and ground pins must be connected for proper operation of the device.

BurstRAM is a trademark of Motorola, Inc.
i486 and Pentium are trademarks of Intel Corp.

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive-edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{A0}$
2nd Burst Address	A15 – A2	$\overline{A1}$	A0
3rd Burst Address	A15 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	L	X	X	X	L-H	N/A	Deselected
H	X	L	X	X	L-H	N/A	Deselected
L	L	X	X	X	L-H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High-Z
Write	X	High-Z — Data In
Deselected	X	High-Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

PASS-THRU TRUTH TABLE (Read proceeded by a write)

Operation of Previous Cycle	$\overline{E}$	$\overline{LW}$	$\overline{UW}$	$\overline{G}$	Operation of Present Cycle	Operation of Next Cycle
Write Cycle, Both Bytes (Address = n – 1)	L	L	L	L	1. Register Address = n and all Inputs 2. Data of Address = n – 1 Appears at Outputs	Read Data at Address = n
Write Cycle, Upper Byte (Address = n – 1)	H	L	H	L	Data of Address = n – 1 Appears at Outputs of Upper Byte	No Carry-Over Operation From Previous Cycle
Write Cycle, Both Bytes (Address = n – 1)	H	L	L	H	All I/Os High-Z	No Carry-Over Operation From Previous Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	+ 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA7} I_{CCA9}	—	290 275	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	75	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486, Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM67C618-7		MCM67C618-9		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	t_{CYC}	12.5	—	15	—	ns	
Clock Access Time	t_{KHQV}	t_{CD}	—	7	—	9	ns	5
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	t_{DC1}	2	—	2	—	ns	
Clock High to Output Change	t_{KHQX2}	t_{DC2}	2	—	2	—	ns	
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	1	—	1	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{OHZ}	2	6	2	6	ns	6
Clock High to Q High-Z	t_{KHQZ}	t_{CZ}	—	6	—	6	ns	
Clock High Pulse Width	t_{KHKL}	t_{CH}	5	—	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	t_{CL}	5	—	5	—	ns	
Setup Times: Address	t_{AVKH}	t_{AS}	2.5	—	2.5	—	ns	7
Address Status	t_{ADSVKH}	t_{SS}						
Data In	t_{DVKH}	t_{DS}						
Write	t_{WVKH}	t_{WS}						
Address Advance	t_{ADVVKH}							
Chip Enable	t_{EVKH}							
Hold Times: Address	t_{KHAX}	t_{AH}	0.5	—	0.5	—	ns	7
Address Status	t_{KHADSX}	t_{SH}						
Data In	t_{KHDX}	t_{DH}						
Write	t_{KHWX}	t_{WH}						
Address Advance	t_{KHADVX}							
Chip Enable	t_{KHEX}							

NOTES:
1. $\overline{W}$ refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 external bus cycles.
6. Transition is measured + 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled.Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

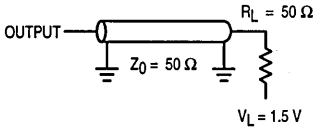


Figure 1A

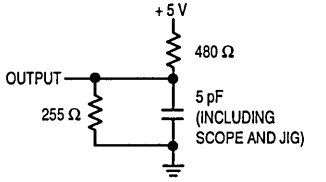
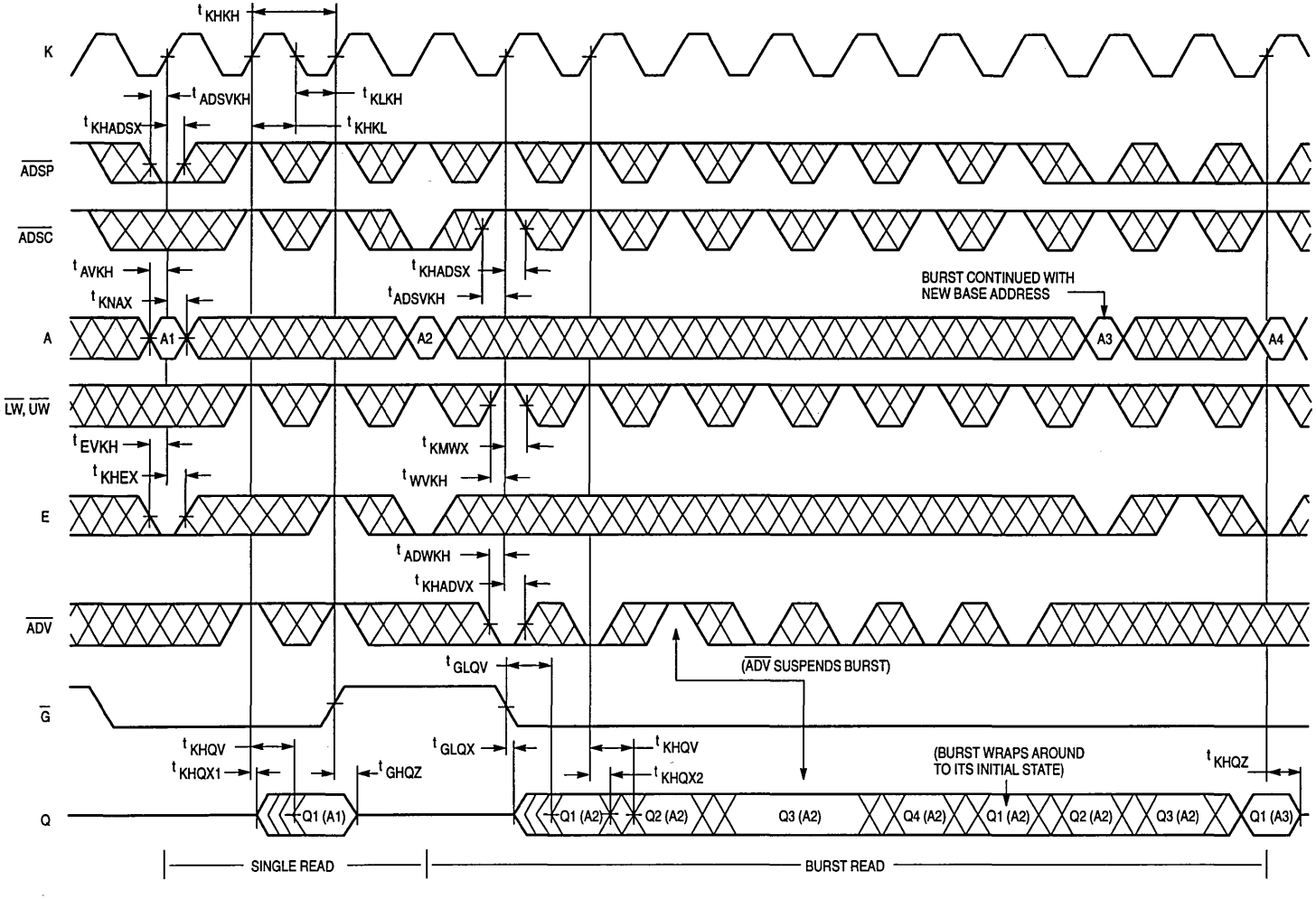


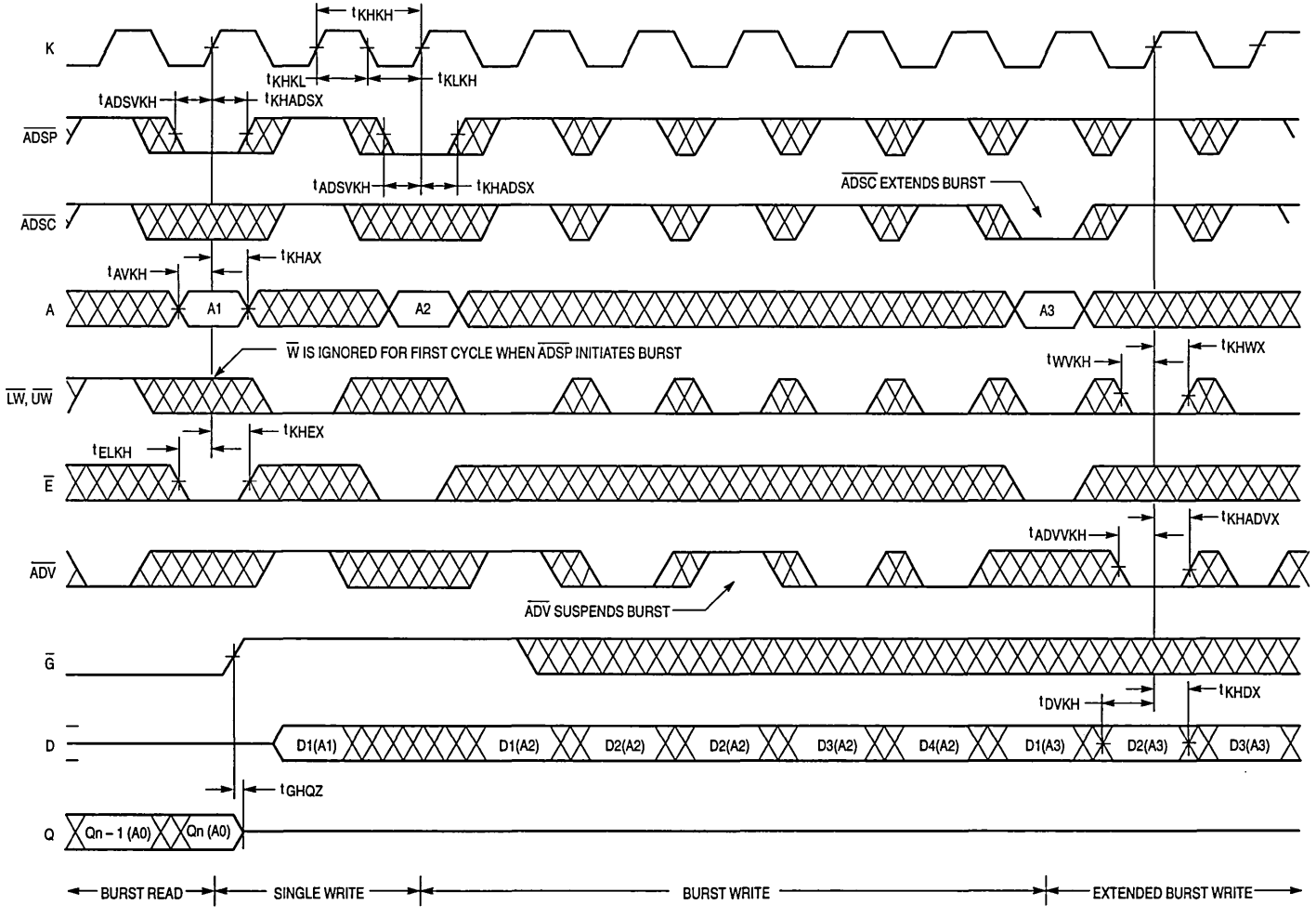
Figure 1B

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

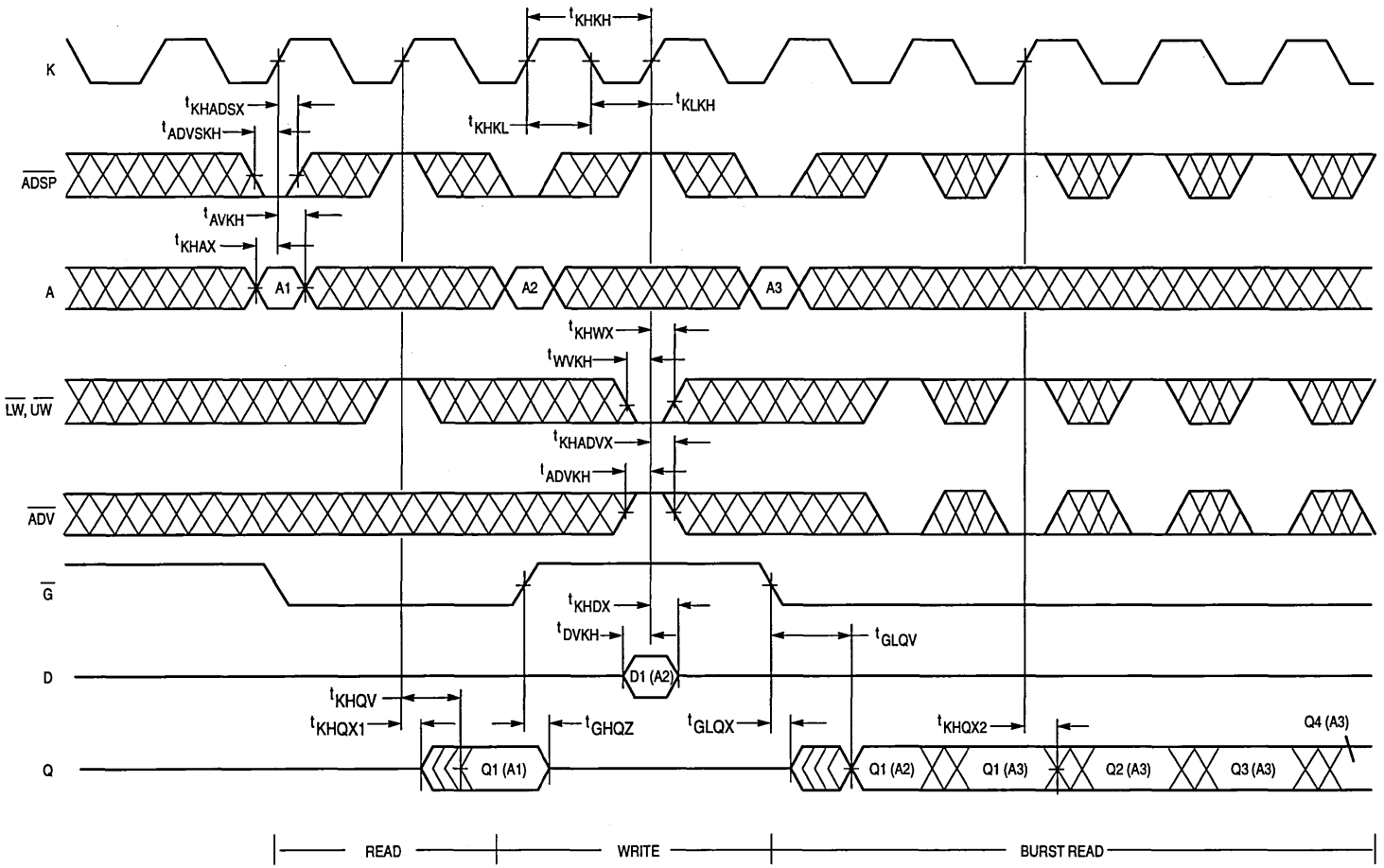
READ CYCLES


tKHKH
K
tADSVKH
tKLKH
tKHADSX
tKHKL
ADSP
ADSC
tAVKH
tKNAX
tKHADSX
tADSVKH
BURST CONTINUED WITH
NEW BASE ADDRESS
A
A1
A2
A3
A4
LW, UW
tEVKH
tKHEX
tKMWX
tWVKH
E
tADWKH
tKHADVX
ADV
(ADV SUSPENDS BURST)
tGLQV
G
tKHQV
tKHQX1
tGHQZ
tGLQX
tKHQV
tKHQX2
(BURST WRAPS AROUND
TO ITS INITIAL STATE)
tKHQZ
Q
Q1 (A1)
Q1 (A2)
Q2 (A2)
Q3 (A2)
Q4 (A2)
Q1 (A2)
Q2 (A2)
Q3 (A2)
Q1 (A3)
SINGLE READ
BURST READ

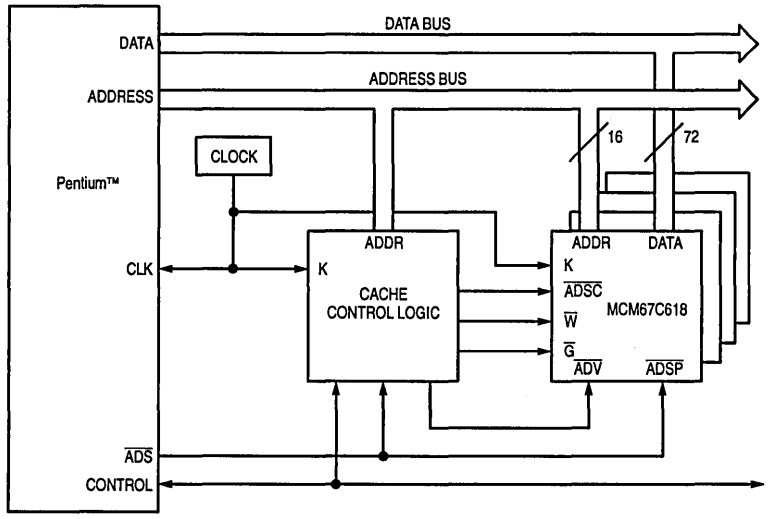
WRITE CYCLES



COMBINATION READ/WRITE CYCLES



APPLICATION EXAMPLE



512K BYTE BURSTABLE, SECONDARY CACHE USING
Four MCM67C618FN9s WITH A 66 MHz Pentium

4

ORDERING INFORMATION
(Order by Full Part Number)

MCM	67C618	X	XX
Motorola Memory Prefix			Speed (7 = 7 ns, 9 = 9 ns)
Part Number			Package (FN = PLCC)

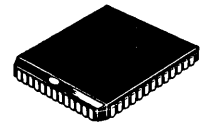
Full Part Number — MCM67C618FN7 MCM67C618FN9

MCM67H618

Product Preview

64K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Self-Timed Write



FN PACKAGE
PLASTIC
CASE 778

The MCM67H618 is a 1,179,648 bit synchronous fast static random access memory designed to provide a burstable, high-performance, secondary cache for the i486 and Pentium™ microprocessors. It is organized as 65,536 words of 18 bits, fabricated with Motorola's high-performance silicon-gate BiCMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A15), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive-edge-triggered noninverting registers.

Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67H618 (burst sequence imitates that of the i486 and Pentium) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

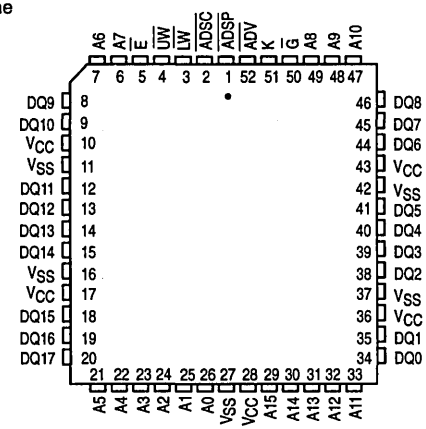
Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 9/12/18 ns Max
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Internally Self-Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52-Lead PLCC Package
- $\overline{ADSP}$ Disabled with Chip Enable ($\overline{E}$) – Supports Address Pipelining

PIN ASSIGNMENT



PIN NAMES	
A0 – A15	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

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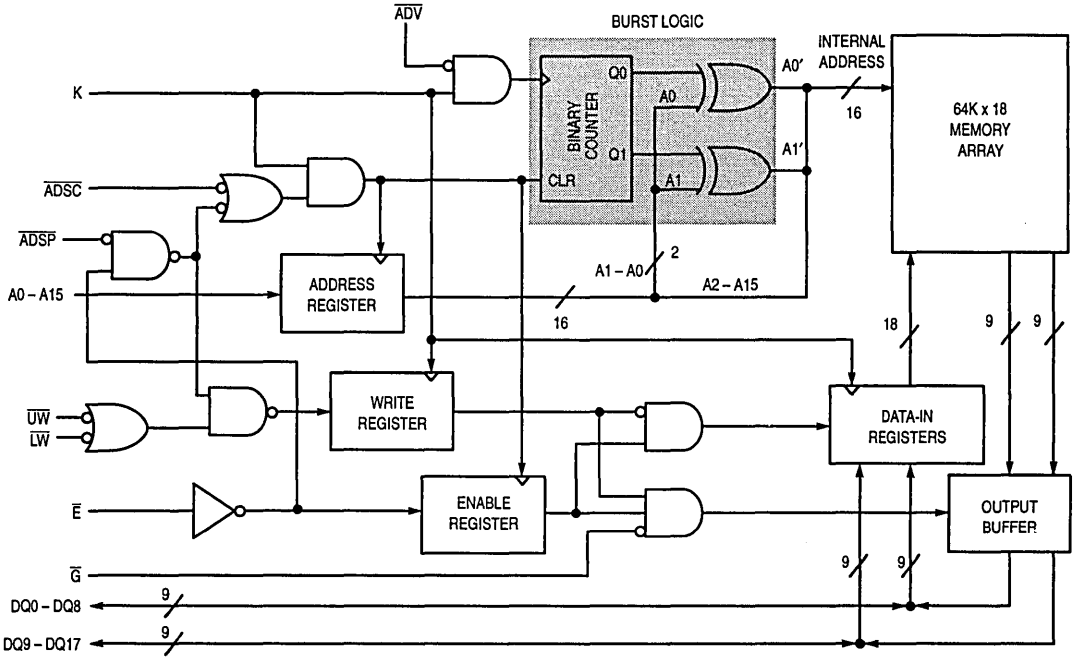
i486 and Pentium are trademarks of Intel Corp.

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive-edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{A0}$
2nd Burst Address	A15 – A2	$\overline{A1}$	A0
3rd Burst Address	A15 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	X	L	X	X	L-H	N/A	Deselected
L	L	X	X	X	L-H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst
H	X	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
H	X	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
H	X	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
H	X	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. Wait states are inserted by suspending burst.

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ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High-Z
Write	X	High-Z — Data In
Deselected	X	High-Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA9} I_{CCA12} I_{CCA18}	— — —	275 250 225	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	75	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible I486 and Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3) ($\overline{W}$ refers to either or both byte write enables)

Parameter	Symbol		MCM67H618-9		MCM67H618-12		MCM67H618-18		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	t_{CYC}	15	—	20	—	30	—	ns	
Clock Access Time	t_{KHQV}	t_{CD}	—	9	—	12	—	18	ns	4
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	5	—	6	—	7	ns	
Clock High to Output Active	t_{KHQX1}	t_{DC1}	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	t_{DC2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{OHZ}	2	6	2	7	2	7	ns	5
Clock High to Q High-Z	t_{KHQZ}	t_{CZ}	—	6	—	6	—	6	ns	
Clock High Pulse Width	t_{KHKL}	t_{CH}	5	—	6	—	7	—	ns	
Clock Low Pulse Width	t_{KLKH}	t_{CL}	5	—	6	—	7	—	ns	
Setup Times: Address	t_{AVKH}	t_{AS}	2.5	—	2.5	—	3.0	—	ns	6
Address Status	t_{ADSVKH}	t_{SS}								
Data In	t_{DVKH}	t_{DS}								
Write	t_{WVKH}	t_{WS}								
Address Advance	t_{ADVVKH}									
Chip Enable	t_{EVKH}									
Hold Times: Address	t_{KHAX}	t_{AH}	0.5	—	0.5	—	0.5	—	ns	6
Address Status	t_{KHADSX}	t_{SH}								
Data In	t_{KHDX}	t_{DH}								
Write	t_{KHWX}	t_{WH}								
Address Advance	t_{KHADVX}									
Chip Enable	t_{KHEX}									

NOTES:
1. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
4. Maximum access times are guaranteed for all possible i486 external bus cycles.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled.Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

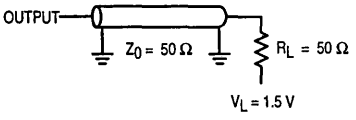


Figure 1A

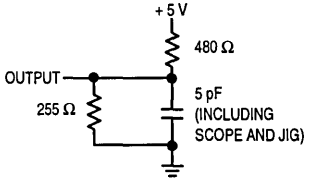
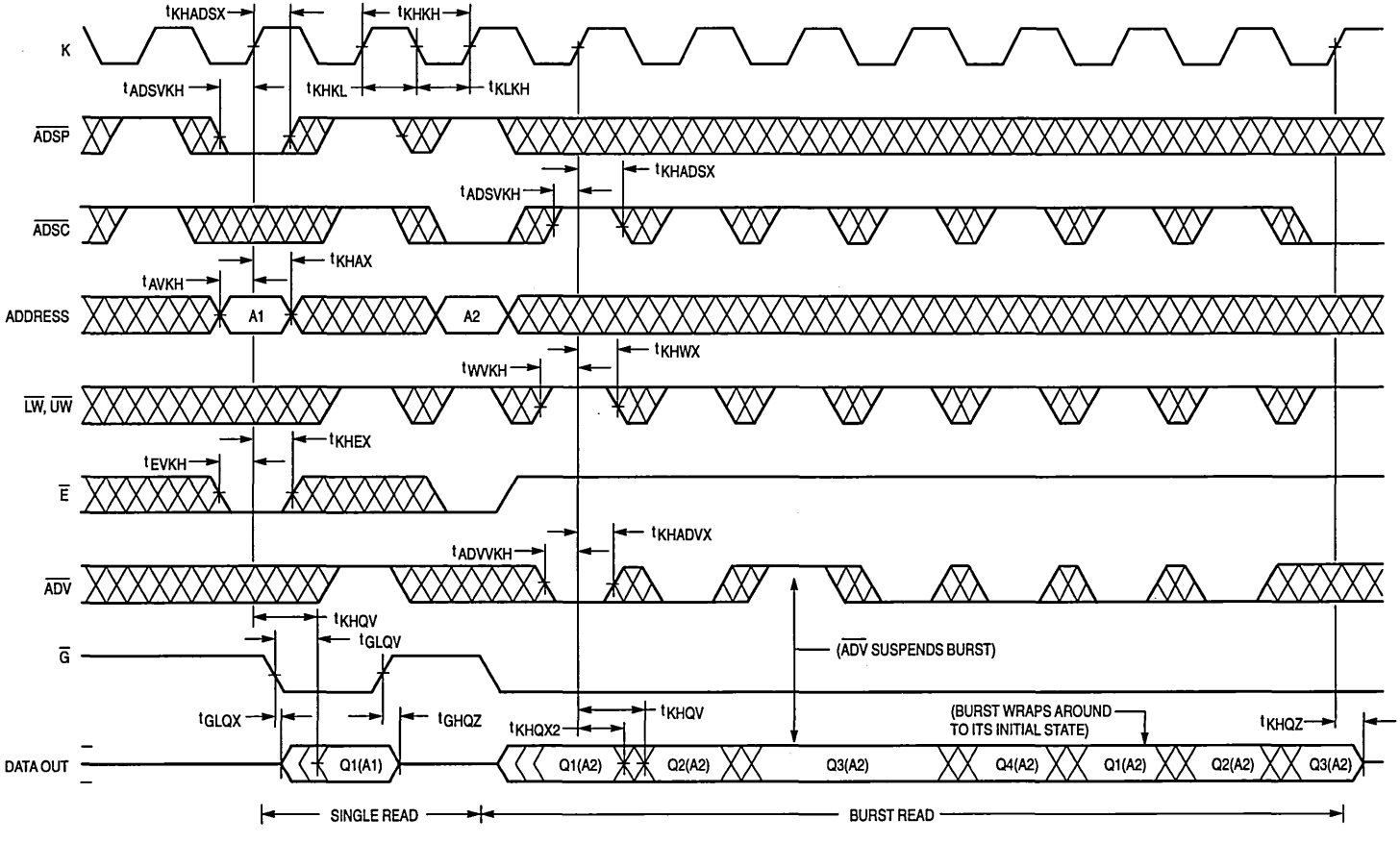


Figure 1B

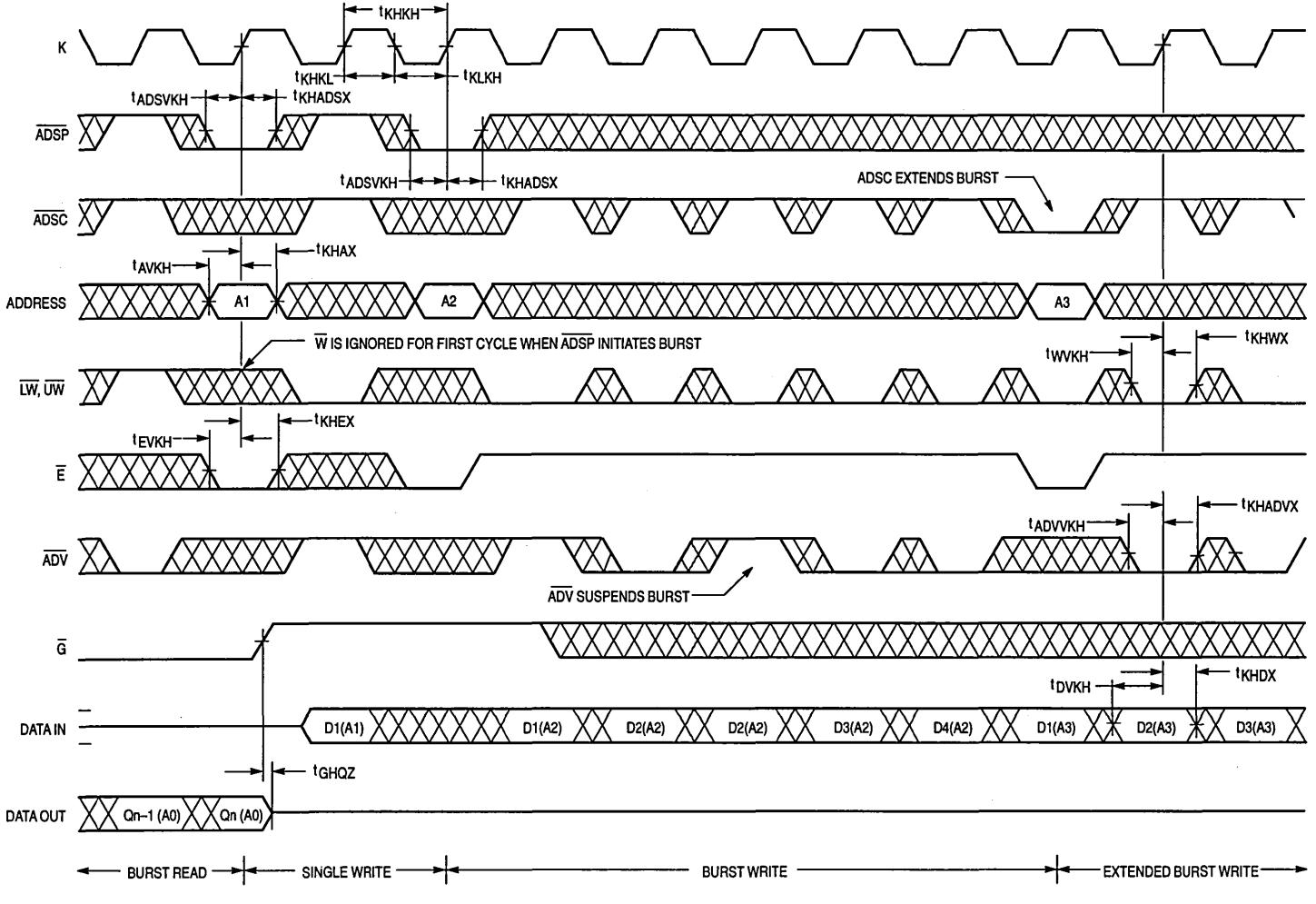
NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLES

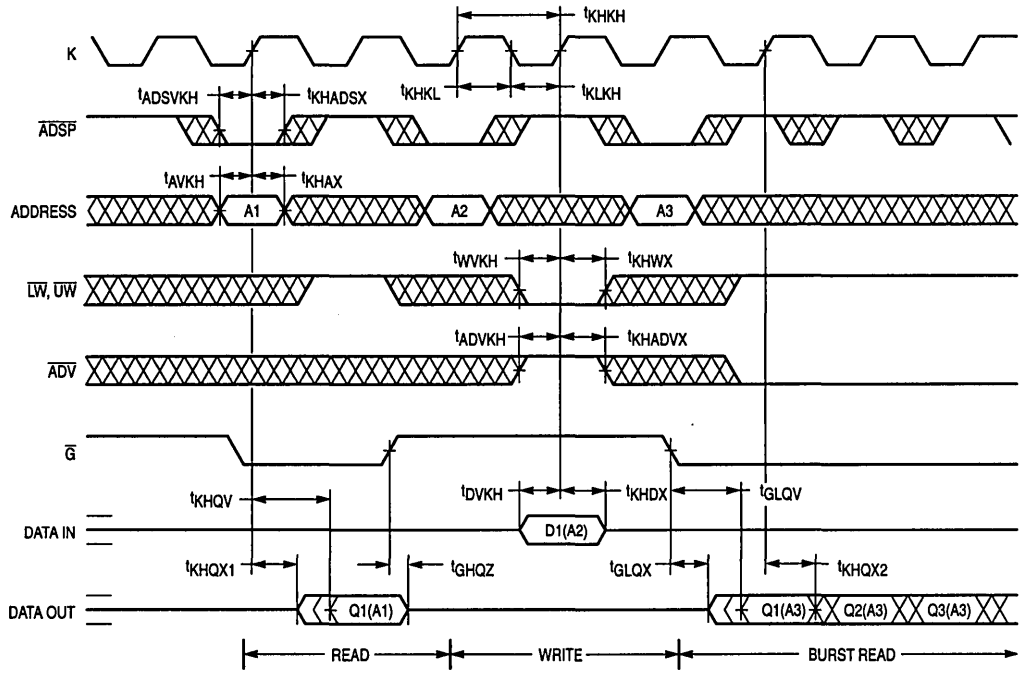


NOTE: Q1(A2) represents the first output data from the base address A2; Q2(A2) represents the next output data in the burst sequence with A2 as the base address.

WRITE CYCLES



COMBINATION READ/WRITE CYCLE



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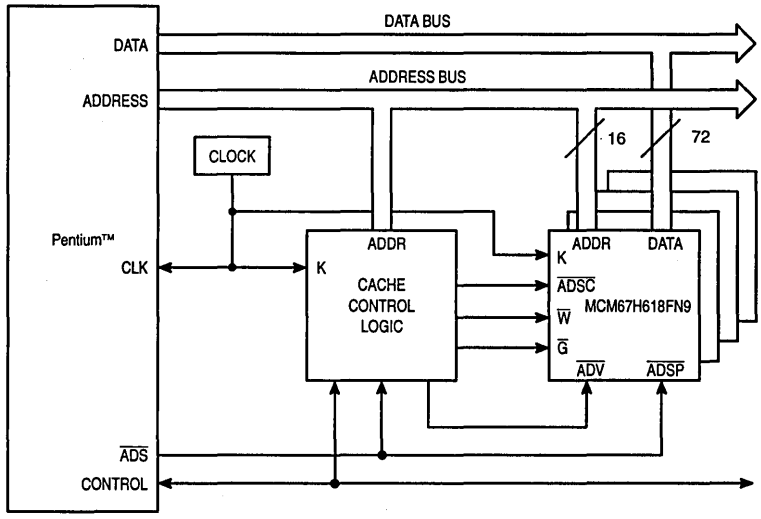
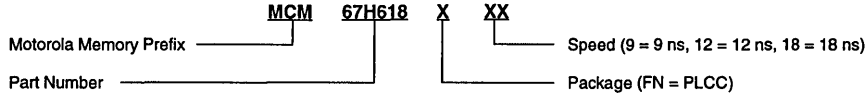
APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache
Using Four MCM67H618FN9s with a 66 MHz Pentium

Figure 2

ORDERING INFORMATION
(Order by Full Part Number)



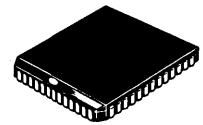
Full Part Numbers — MCM67H618FN9 MCM67H618FN12 MCM67H618FN18

MCM67J618

Product Preview

64K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Registered Outputs



FN PACKAGE
PLASTIC
CASE 778

The MCM67J618 is a 1,179,648 bit synchronous static random access memory designed to provide a burstable, high-performance, secondary cache for the i486™ and Pentium™ microprocessors. It is organized as 65,536 words of 18 bits, fabricated with Motorola's high-performance silicon-gate BiCMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive registered output drivers onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A15), data inputs (D0 – D17), and all control signals except output enable ($\overline{G}$) are clock (K) controlled through positive-edge-triggered noninverting registers.

This device contains output registers for pipeline operations. At the rising edge of K, the RAM provides the output data from the previous cycle.

Output enable ($\overline{G}$) is asynchronous for maximum system design flexibility.

Burst can be initiated with either address status processor ($\overline{ADSP}$) or address status cache controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be generated internally by the MCM67J618 (burst sequence imitates that of the i486) and controlled by the burst address advance ($\overline{ADV}$) input pin. The following pages provide more detailed information on burst controls.

Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

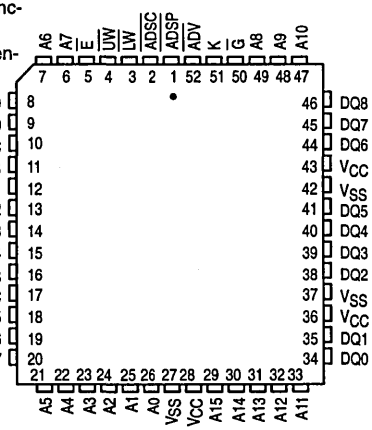
This device also incorporates pass-thru functionality. A read cycle preceded by a write cycle will cause the the data written into the array to appear at the outputs on the same clock cycle on which the read was initiated. The clock high to data valid time is the same as that of a standard read operation. Chip enable ($\overline{E}$) does not have to be asserted to receive valid data during a pass-thru operation. Output enable ($\overline{G}$) maintains control of the output buffers during a pass-thru operation.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory. See Figure 2 for applications information.

- Single 5 V ± 5% Power Supply
- Fast Access Time/Fast Cycle Time = 7 ns/80 MHz, 9 ns/66 MHz
- Byte Writeable via Dual Write Enables
- Internal Input Registers (Address, Data, Control)
- Output Registers for Pipelined Applications
- Internally Self-Timed Write Cycle
- $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$ Burst Control Pins
- Write Pass-Thru Capability
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- 3.3 V I/O Compatible
- High Board Density 52-Lead PLCC Package
- $\overline{ADSP}$ Disabled with Chip Enable ($\overline{E}$) – Supports Address Pipelining

PIN ASSIGNMENT



PIN NAMES

A0 – A15	Address Inputs
K	Clock
$\overline{ADV}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

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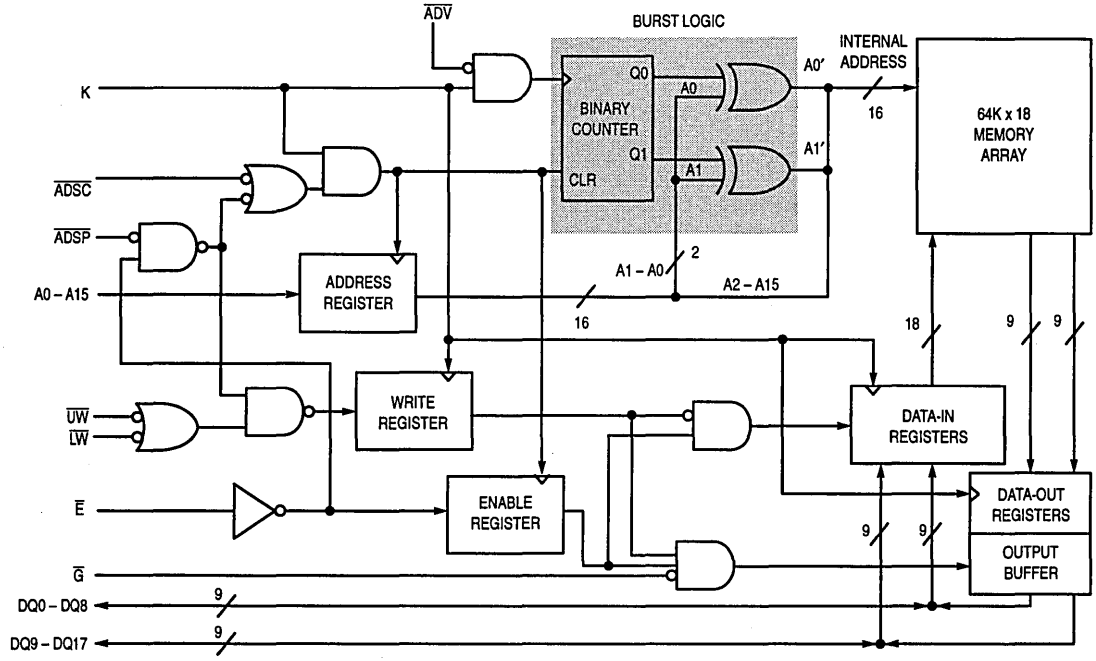
i486 and Pentium are trademarks of Intel Corp.

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive-edge triggered. The $\overline{ADSC}$ or $\overline{ADSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{ADSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{ADSC}$) is performed using the new external address. When $\overline{ADSC}$ is sampled low (and $\overline{ADSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the new external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{ADV}$ controls subsequent burst cycles. When $\overline{ADV}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{ADV}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE TABLE**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE TABLE (See Note)

External Address	A15 – A2	A1	A0
1st Burst Address	A15 – A2	A1	$\overline{A0}$
2nd Burst Address	A15 – A2	$\overline{A1}$	A0
3rd Burst Address	A15 – A2	$\overline{A1}$	$\overline{A0}$

NOTE: The burst wraps around to its initial state upon completion.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}$ or $\overline{LW}$	K	Address Used	Operation
H	X	L	X	X	L-H	N/A	Deselected
L	L	X	X	X	L-H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst
H	X	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
H	X	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
H	X	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
H	X	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out
Read	H	High-Z
Write	X	High-Z — Data In
Deselected	X	High-Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

PASS-THRU TRUTH TABLE (Read preceded by a write)

Operation of Previous Cycle	$\overline{E}$	$\overline{LW}$	$\overline{UW}$	$\overline{G}$	Operation of Present Cycle	Operation of Next Cycle
Write Cycle, Both Bytes (Address = n – 1)	L	L	L	L	1. Register Address = n and all Inputs 2. Data of Address = n – 1 Appears at Outputs	Read Data at Address = n
Write Cycle, Upper Byte (Address = n – 1)	H	L	H	L	Data of Address = n – 1 Appears at Outputs of Upper Byte	No Carry-Over Operation From Previous Cycle
Write Cycle, Both Bytes (Address = n – 1)	H	L	L	H	All I/Os High-Z	No Carry-Over Operation From Previous Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	+ 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA7} I_{CCA9}	—	290 275	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	75	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible i486, Pentium bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM67J618-7		MCM67J618-9		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	t_{CYC}	12.5	—	15	—	ns	
Clock Access Time	t_{KHQV}	t_{CD}	—	7	—	9	ns	5
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	t_{DC1}	2	—	2	—	ns	
Clock High to Output Change	t_{KHQX2}	t_{DC2}	2	—	2	—	ns	
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	1	—	1	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{OHZ}	2	6	2	6	ns	6
Clock High to Q High-Z	t_{KHQZ}	t_{CZ}	—	6	—	6	ns	
Clock High Pulse Width	t_{KHKL}	t_{CH}	5	—	5	—	ns	
Clock Low Pulse Width	t_{KLKH}	t_{CL}	5	—	5	—	ns	
Setup Times: Address	t_{AVKH}	t_{AS}	2.5	—	2.5	—	ns	7
Address Status	t_{ADSVKH}	t_{SS}						
Data In	t_{DVKH}	t_{DS}						
Write	t_{WVKH}	t_{WS}						
Address Advance	t_{ADVVKH}							
Chip Enable	t_{EVKH}							
Hold Times: Address	t_{KHAX}	t_{AH}	0.5	—	0.5	—	ns	7
Address Status	t_{KHADSX}	t_{SH}						
Data In	t_{KHDX}	t_{DH}						
Write	t_{KHWX}	t_{WH}						
Address Advance	t_{KHADVX}							
Chip Enable	t_{KHEX}							

NOTES:
1. $\overline{W}$ refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).
2. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{ADSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{ADSP}$ high for the setup and hold times.
3. All read and write cycle timings are referenced from K or $\overline{G}$.
4. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
5. Maximum access times are guaranteed for all possible i486 external bus cycles.
6. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of K whenever $\overline{ADSP}$ or $\overline{ADSC}$ is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is enabled.Chip enable must be valid at each rising edge of clock for the device (when $\overline{ADSP}$ or $\overline{ADSC}$ is low) to remain enabled.

AC TEST LOADS

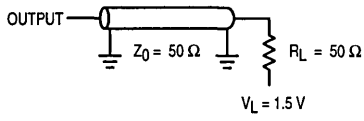


Figure 1A

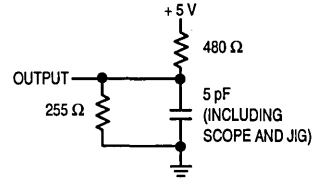
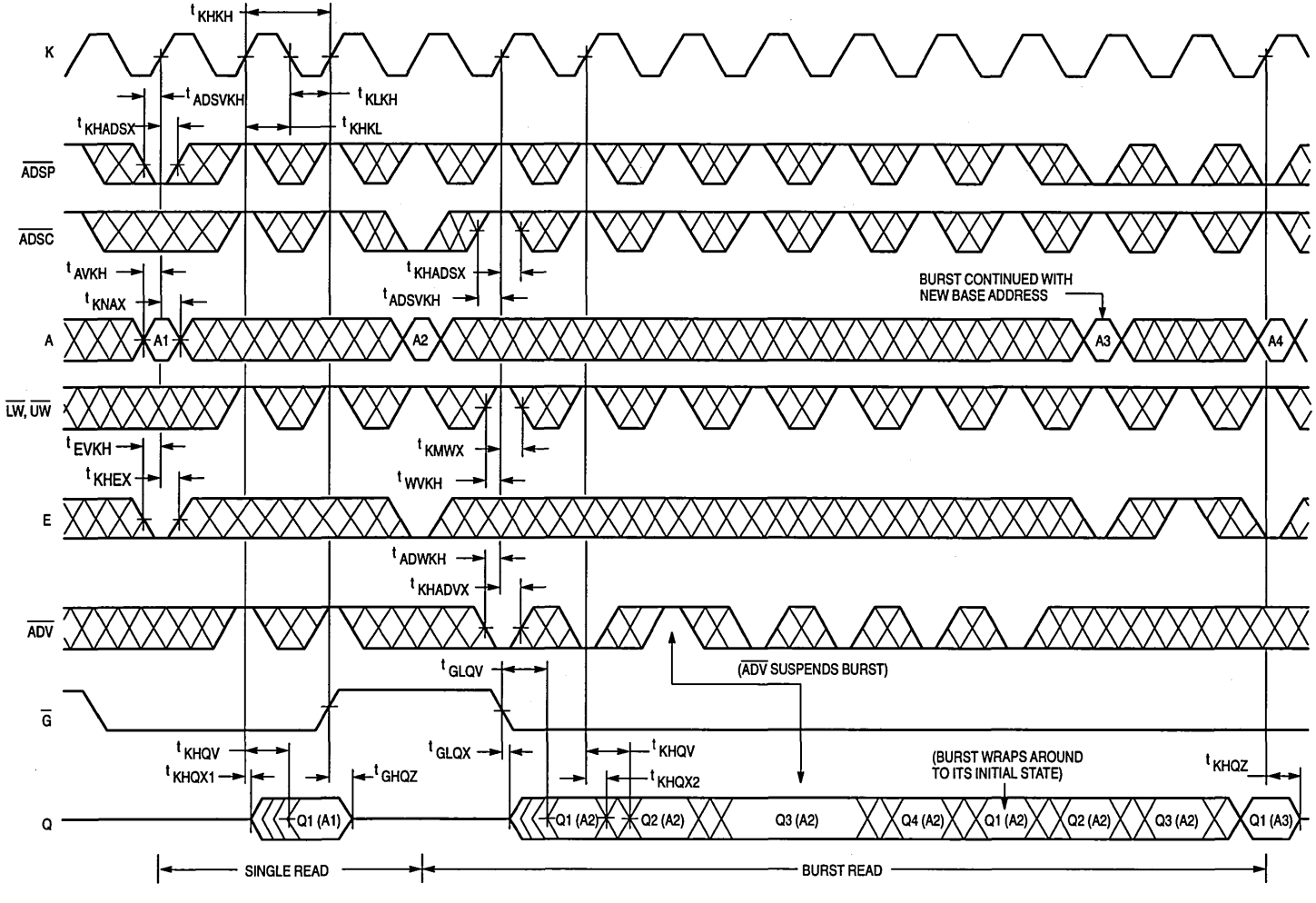


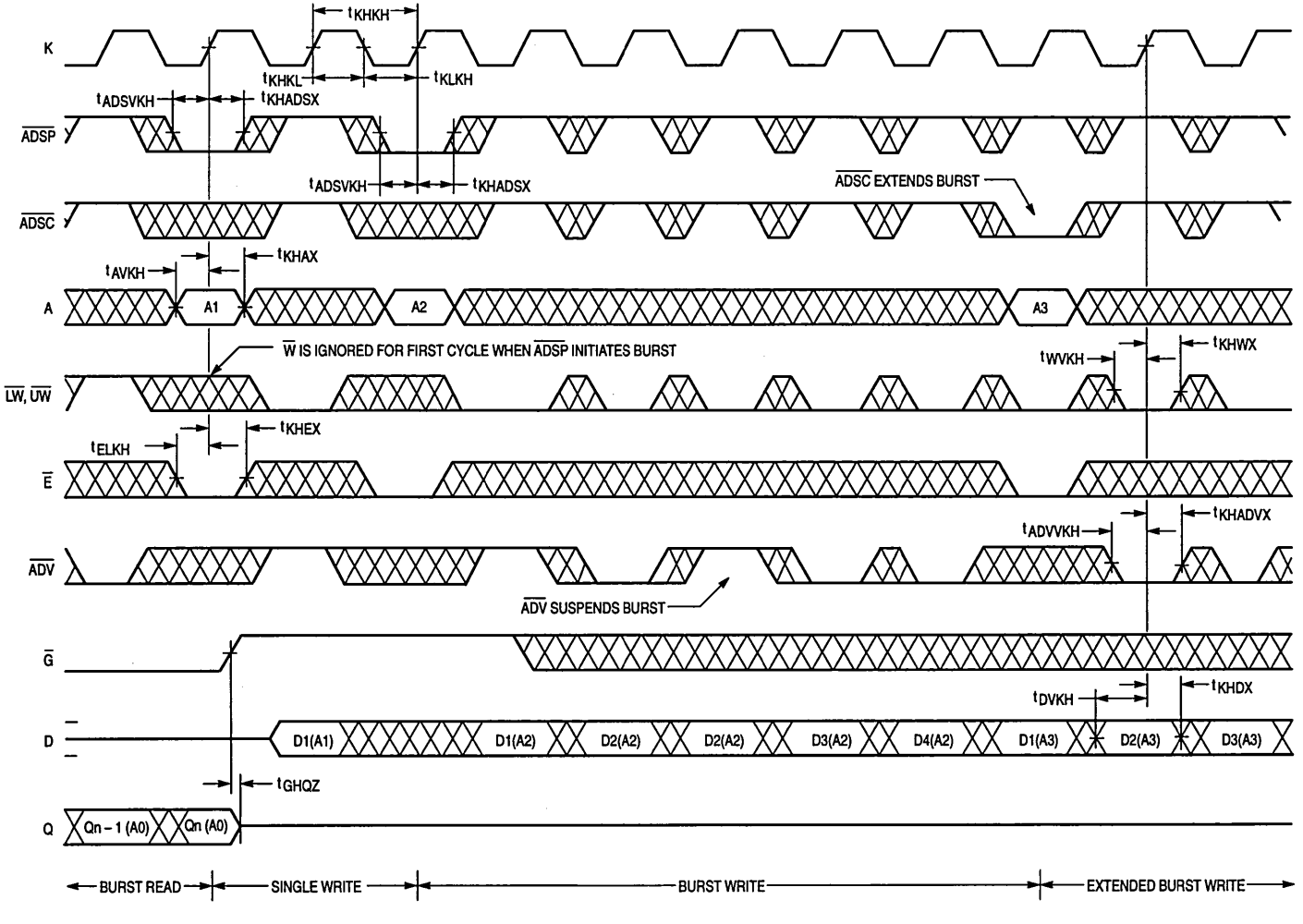
Figure 1B

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLES

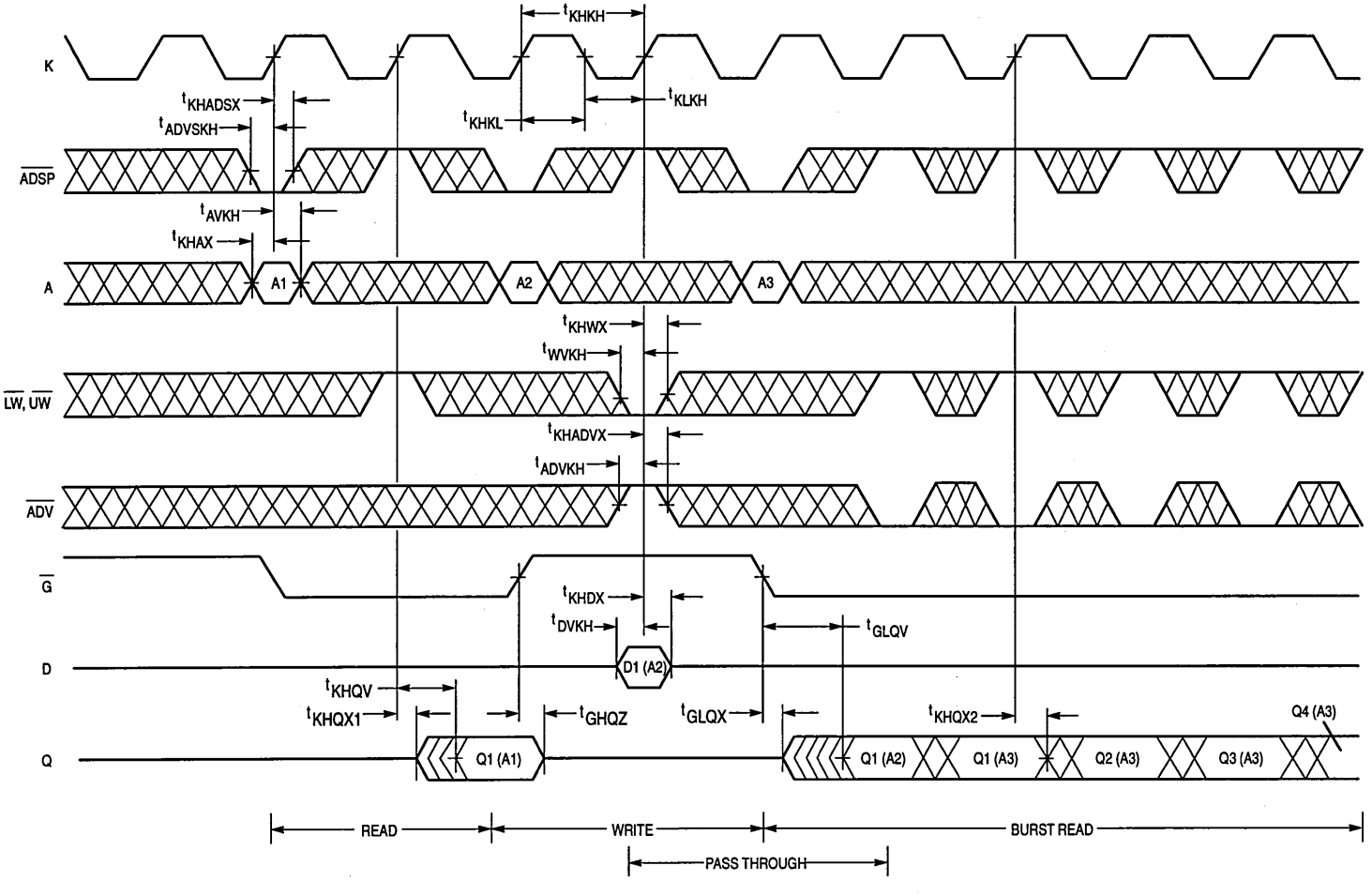

tKHKH
K
tADSVKH
tKLKH
tKHADSX
tKHKL
ADSP
ADSC
tAVKH
tKNAX
tKHADSX
tADSVKH
BURST CONTINUED WITH NEW BASE ADDRESS
A
A1
A2
A3
A4
LW, UW
tEVKH
tKHEX
tKMWX
tWVKH
E
tADWKH
tKHADVX
ADV
tGLQV
(ADV SUSPENDS BURST)
G
tKHQV
tKHQX1
tGHQZ
tGLQX
tKHQV
tKHQX2
(BURST WRAPS AROUND TO ITS INITIAL STATE)
tKHQZ
Q
Q1 (A1)
Q1 (A2)
Q2 (A2)
Q3 (A2)
Q4 (A2)
Q1 (A2)
Q2 (A2)
Q3 (A2)
Q1 (A3)
SINGLE READ
BURST READ

WRITE CYCLES

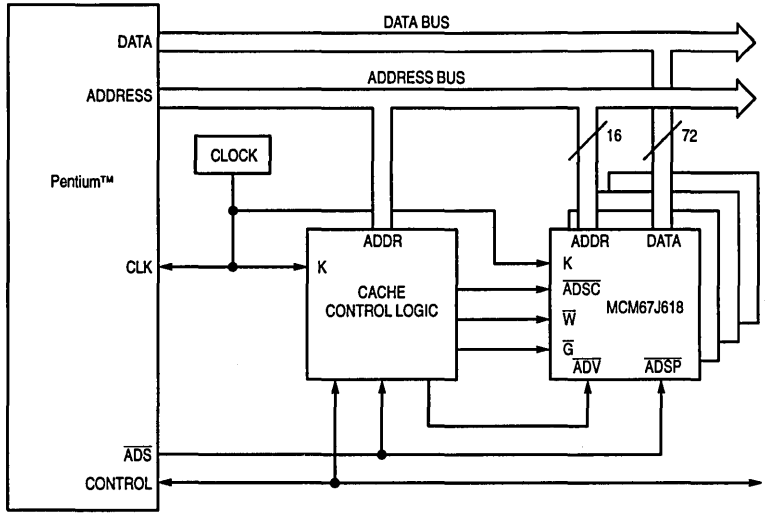


4

COMBINATION READ/WRITE CYCLES



APPLICATION EXAMPLE



512K BYTE BURSTABLE, SECONDARY CACHE USING
FOUR MCM67J618FN9s WITH A 66 MHz PENTIUM

4

ORDERING INFORMATION
(Order by Full Part Number)

MCM 67J618 X XX

Motorola Memory Prefix — MCM

Part Number — 67J618

Speed (7 = 7 ns, 9 = 9 ns) — XX

Package (FN = PLCC) — X

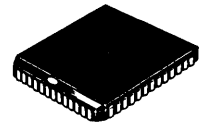
Full Part Numbers — MCM67J618FN7 MCM67J618FN9

MCM67M618

Product Preview

64K x 18 Bit BurstRAM™ Synchronous Fast Static RAM

With Burst Counter and Self-Timed Write



FN PACKAGE
PLASTIC
CASE 778

The MCM67M618 is a 1,179,648 bit synchronous static random access memory designed to provide a burstable, high-performance, secondary cache for the MC68040 and PowerPC™ microprocessors. It is organized as 65,536 words of 18 bits, fabricated using Motorola's high-performance silicon-gate BiCMOS technology. The device integrates input registers, a 2-bit counter, high speed SRAM, and high drive capability outputs onto a single monolithic circuit for reduced parts count implementation of cache data RAM applications. Synchronous design allows precise cycle control with the use of an external clock (K). BiCMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

Addresses (A0 – A15), data inputs (DQ0 – DQ17), and all control signals, except output enable ($\overline{G}$), are clock (K) controlled through positive-edge-triggered noninverting registers.

Bursts can be initiated with either transfer start processor ($\overline{TSP}$) or transfer start cache controller ($\overline{TSC}$) input pins. Subsequent burst addresses are generated internally by the MCM67M618 (burst sequence imitates that of the MC68040) and controlled by the burst address advance ($\overline{BAA}$) input pin. The following pages provide more detailed information on burst controls.

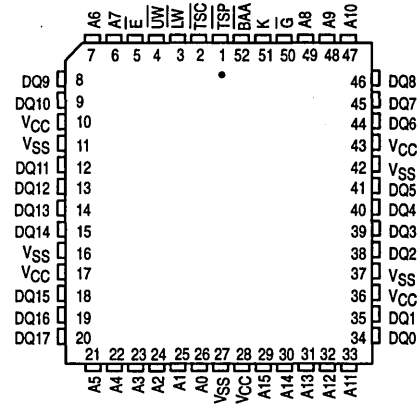
Write cycles are internally self-timed and are initiated by the rising edge of the clock (K) input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

Dual write enables ($\overline{LW}$ and $\overline{UW}$) are provided to allow individually writeable bytes. $\overline{LW}$ controls DQ0 – DQ8 (the lower bits), while $\overline{UW}$ controls DQ9 – DQ17 (the upper bits).

This device is ideally suited for systems that require wide data bus widths and cache memory.

- Single 5 V ± 5% Power Supply
- Fast Access Times: 9/11/14/19 ns Max and Cycle Times: 12.5/15/20/25 ns Min
- Byte Writeable via Dual Write Strobes
- Internal Input Registers (Address, Data, Control)
- Internally Self-Timed Write Cycle
- $\overline{TSP}$, $\overline{TSC}$, and $\overline{BAA}$ Burst Control Pins
- Asynchronous Output Enable Controlled Three-State Outputs
- Common Data Inputs and Data Outputs
- High Board Density 52-PLCC Package
- 3.3 V I/O Compatible

PIN ASSIGNMENT

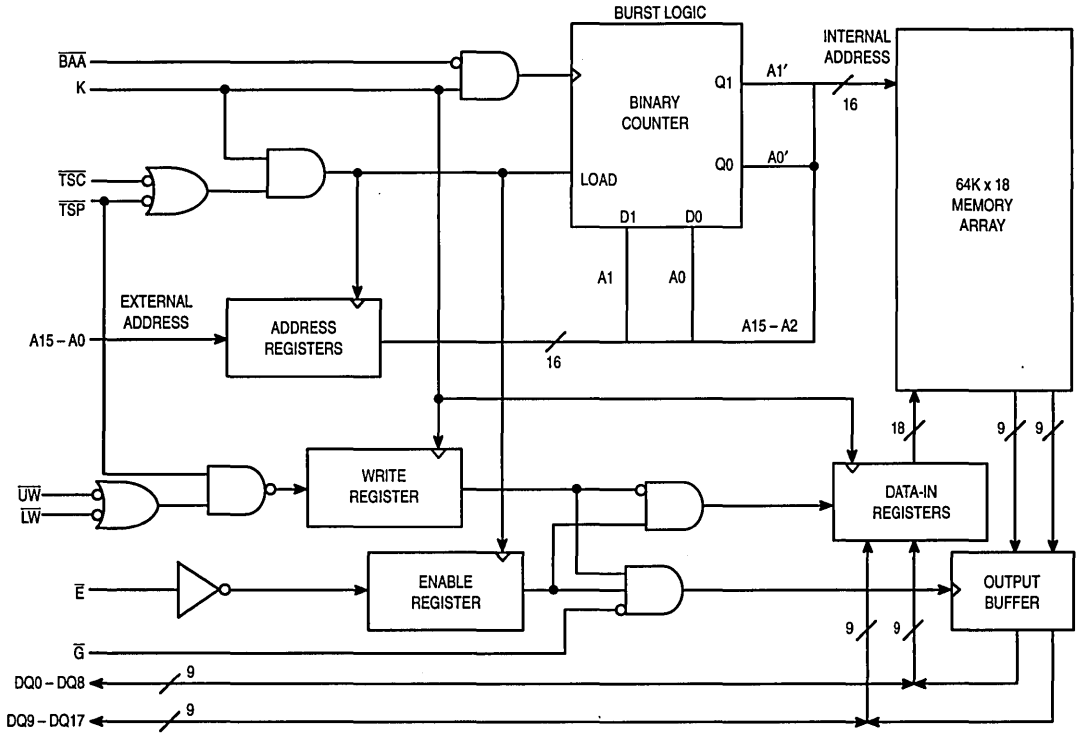


PIN NAMES	
A0 – A15	Address Inputs
K	Clock
$\overline{BAA}$	Burst Address Advance
$\overline{LW}$	Lower Byte Write Enable
$\overline{UW}$	Upper Byte Write Enable
$\overline{TSP}$, $\overline{TSC}$	Transfer Start
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
VCC	+ 5 V Power Supply
VSS	Ground

All power supply and ground pins must be connected for proper operation of the device.

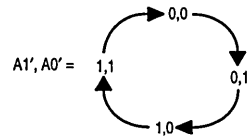
BurstRAM is a trademark of Motorola, Inc.
PowerPC is a trademark of IBM Corp.

BLOCK DIAGRAM (See Note)



NOTE: All registers are positive-edge triggered. The $\overline{TSC}$ or $\overline{TSP}$ signals control the duration of the burst and the start of the next burst. When $\overline{TSP}$ is sampled low, any ongoing burst is interrupted and a read (independent of $\overline{W}$ and $\overline{TSC}$) is performed using the new external address. When $\overline{TSC}$ is sampled low (and $\overline{TSP}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on $\overline{W}$) is performed using the next external address. Chip enable ($\overline{E}$) is sampled only when a new base address is loaded. After the first cycle of the burst, $\overline{BAA}$ controls subsequent burst cycles. When $\overline{BAA}$ is sampled low, the internal address is advanced prior to the operation. When $\overline{BAA}$ is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See **BURST SEQUENCE GRAPH**. Write refers to either or both byte write enables ($\overline{LW}$, $\overline{UW}$).

BURST SEQUENCE GRAPH (See Note)



NOTE: The external two values for A1 and A0 provide the starting point for the burst sequence graph. The burst logic advances A1 and A0 as shown above.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

$\overline{E}$	$\overline{TSP}$	$\overline{TSC}$	$\overline{BAA}$	$\overline{LW}$ or $\overline{UW}$	K	Address	Operation
H	L	X	X	X	L-H	N/A	Deselected
H	X	L	X	X	L-H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L-H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L-H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L-H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L-H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L-H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L-H	Current Address	Read Cycle, Suspend Burst

NOTES:
1. X means Don't Care.
2. All inputs except $\overline{G}$ must meet setup and hold times for the low-to-high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	$\overline{G}$	I/O Status
Read	L	Data Out (DQ0 – DQ8)
Read	H	High-Z
Write	X	High-Z — Data In
Deselected	X	High-Z

NOTES:
1. X means Don't Care.
2. For a write operation following a read operation, $\overline{G}$ must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, $\overline{E}$ = V_{IL}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{CCA9} I_{CCA11} I_{CCA14} I_{CCA19}	—	290 275 250 225	mA
AC Standby Current ($\overline{E}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} and V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{KHKH} min)	I_{SB1}	—	75	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible 68040 bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	—	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	$C_{I/O}$	—	6	8	pF

4

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3) ($\overline{W}$ refers to either or both byte write enables)

Parameter	Symbol		67M618-9		67M618-11		67M618-14		67M618-19		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	t_{CYC}	12.5	—	15	—	20	—	25	—	ns	
Clock Access Time	t_{KHQV}	t_{CD}	—	9	—	11	—	14	—	19	ns	4
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	5	—	5	—	6	—	7	ns	
Clock High to Output Active	t_{KHQX1}	t_{DC1}	6	—	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	t_{DC2}	3	—	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{OHZ}	2	6	2	6	2	6	2	7	ns	5
Clock High to Q High-Z	t_{KHQZ}	t_{CZ}	—	6	—	6	—	6	—	6	ns	5
Clock High Pulse Width	t_{KHKL}	t_{CH}	5	—	5	—	6	—	7	—	ns	
Clock Low Pulse Width	t_{KLKH}	t_{CL}	5	—	5	—	6	—	7	—	ns	
Setup Times: Address	t_{AVKH}	t_{AS}	2.5	—	2.5	—	2.5	—	3.0	—	ns	6
Address Status	t_{TSVKH}	t_{SS}										
Data In	t_{DVKH}	t_{DS}										
Write	t_{WVKH}	t_{WS}										
Address Advance	t_{BAVKH}											
Chip Select	t_{EVKH}											
Hold Times: Address	t_{KHAX}	t_{AH}	0.5	—	0.5	—	0.5	—	0.5	—	ns	6
Address Status	t_{KHTSX}	t_{SH}										
Data In	t_{KHDX}	t_{DH}										
Write	t_{KHWX}	t_{WH}										
Address Advance	t_{KHBAX}											
Chip Select	t_{KHEX}											

NOTES:
1. A read cycle is defined by $\overline{UW}$ and $\overline{LW}$ high or $\overline{TSP}$ low for the setup and hold times. A write cycle is defined by $\overline{LW}$ or $\overline{UW}$ low and $\overline{TSP}$ high for the setup and hold times.
2. All read and write cycle timings are referenced from K or $\overline{G}$.
3. $\overline{G}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ is sampled low.
4. Maximum access times are guaranteed for all possible MC68040 external bus cycles.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX1} min for a given device and from device to device.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for ***ALL*** rising edges of clock (K) whenever $\overline{TSP}$ or $\overline{TSC}$ are low and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for ***ALL*** rising edges of K when the chip is selected.Chip enable must be valid at each rising edge of clock for the device (when $\overline{TSP}$ or $\overline{TSC}$ is low) to remain enabled.

AC TEST LOADS

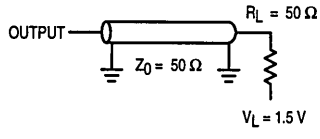


Figure 1A

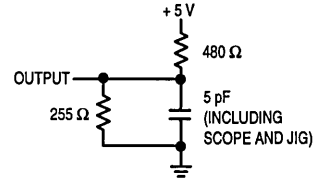
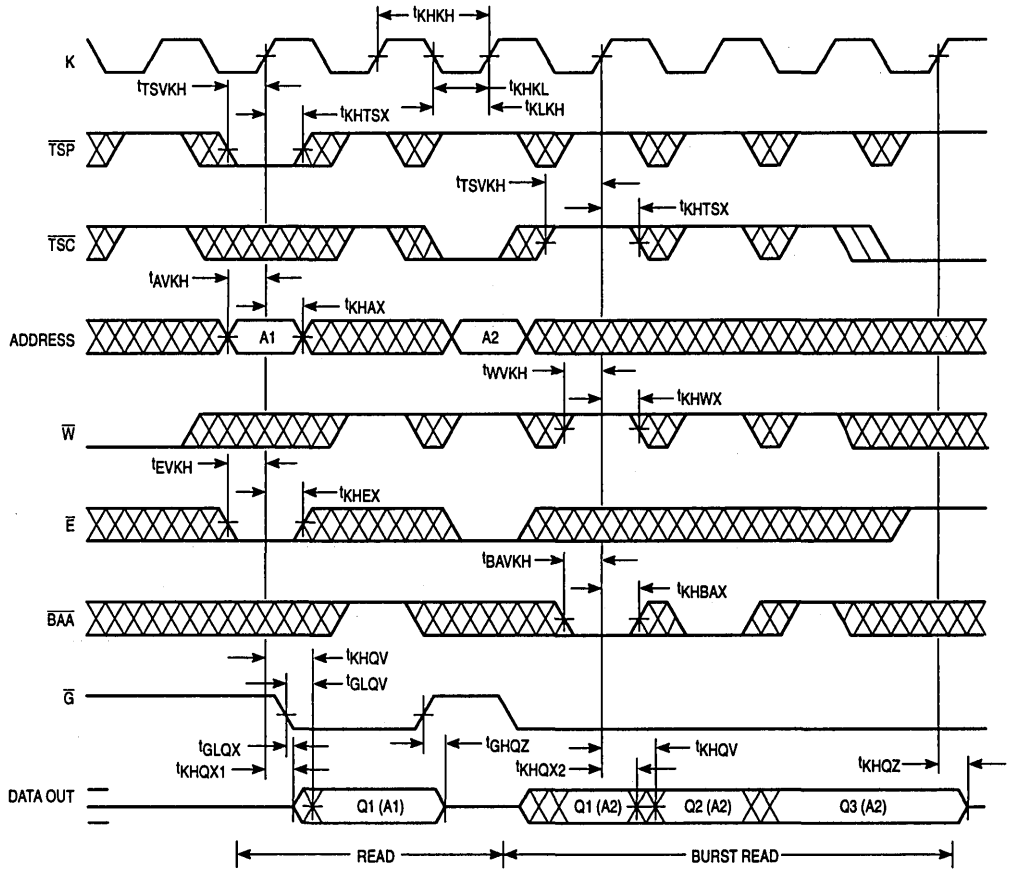


Figure 1B

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

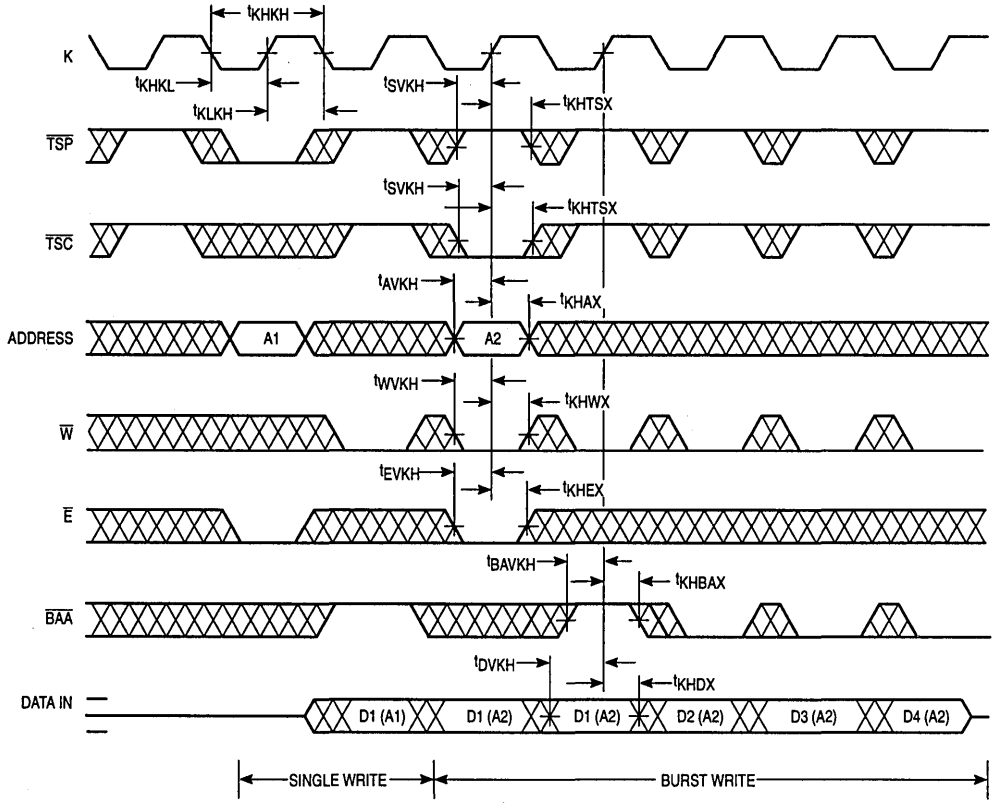
READ CYCLE



NOTE: Q1(A2) represents the first output from the external address A2; Q2(A2) represents the next output data in the burst sequence with A2 as the base address.

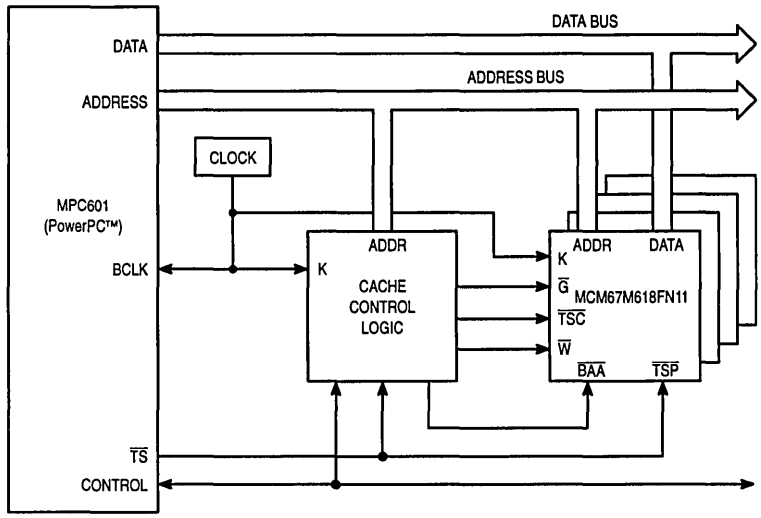
4

WRITE CYCLE



NOTE: $\overline{G} = V_{IH}$.

APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache
Using Four MCM67M618FN11s with a 66 MHz MPC601 PowerPC™

4

ORDERING INFORMATION
(Order by Full Part Number)

MCM 67M618 X XX

Motorola Memory Prefix

Part Number

Speed (9 = 9 ns, 11 = 11 ns, 14 = 14 ns, 19 = 19 ns)

Package (FN = PLCC)

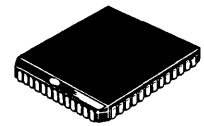
Full Part Numbers — MCM67M618FN9 MCM67M618FN11 MCM67M618FN14 MCM67M618FN19

MCM67W618

Product Preview

64K x 18 Bit Asynchronous Fast Static RAM

With Address Latch and Byte Enable



FN PACKAGE
PLASTIC
CASE 778

The MCM67W618 is a 1,179,648 bit static random access memory organized as 65,536 words of 18 bits, fabricated using Motorola's high-performance silicon-gate BiCMOS technology. The device integrates a 64K x 18 SRAM core with advanced peripheral circuitry consisting of address latches, active low chip enable, write enable, separate upper and lower byte selects, and a fast output enable. This device has increased output drive capability supported by multiple power pins.

Address latch enable (AL) is provided to simplify read and write cycles by guaranteeing address hold time in a simple fashion. When the address latch input is high, the address latch is in the transparent state. If the latch enable is tied high, the device can be used as an asynchronous SRAM. When the address latch enable is low, the address is in the latched state.

Dual byte selects ($\overline{LB}$ and $\overline{UB}$) are provided to allow individually readable and writeable bytes. $\overline{LB}$ controls DQ0 – DQ8 (the lower bits) while $\overline{UB}$ controls DQ9 – DQ17 (the upper bits).

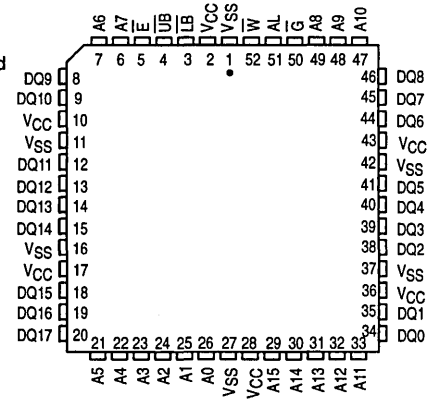
A generous number of power supply pins have been utilized and placed on the package for maximum performance.

The MCM67W618 will be available in a 52-pin plastic leaded chip carrier (PLCC).

This device is ideally suited for systems that require wide data bus widths, cache memory, and as tag RAMs.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 12/15/20 ns Max
- Byte Write and Byte Read Capability
- Transparent Address Latch
- Common Data Inputs and Data Outputs
- Output Enable Controlled Three-State Outputs
- 3.3 V I/O Compatible
- High Board Density 52-Lead PLCC Package

PIN ASSIGNMENT

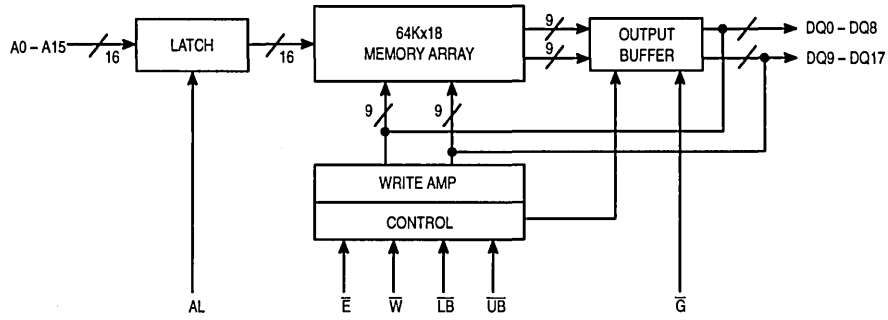


PIN NAMES	
A0 – A15	Address Inputs
AL	Address Latch
$\overline{W}$	Write Enable
$\overline{LB}$	Lower Byte Select
$\overline{UB}$	Upper Byte Select
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ17	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{LB}$	$\overline{UB}$	$\overline{W}$	AL*	$\overline{G}$	Mode	Supply Current	I/O Status
H	X	X	X	X	X	Deselected	I_{SB}	High-Z
L	X	X	X	L	X	Read or Write Using Latched Addresses	I_{CC}	—
L	X	X	X	H	X	Read or Write Using Unlatched Addresses	I_{CC}	—
L	L	L	H	X	L	Read Cycle	I_{CC}	Data Out
L	L	L	H	X	H	Read Cycle	I_{CC}	High-Z
L	L	L	L	X	X	Write Cycle Lower and Upper Byte	I_{CC}	High-Z
L	L	H	L	L	X	Write Cycle Lower Byte with Latched Addresses	I_{CC}	High-Z
L	H	L	H	L	L	Read Cycle Upper Byte	I_{CC}	Data Out

*Addresses must satisfy the specified setup and hold times for the falling edge of AL.
NOTE: This truth table shows the application of all device functions; different combinations are valid.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	1.6	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{G}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current ($\overline{G}$ = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, Cycle Time ≥ t_{AVAV} min) I_{CCA12} I_{CCA15} I_{CCA20}	I_{CCA12} I_{CCA15} I_{CCA20}	— — —	290 275 260	mA
AC Standby Current (E = V_{IH}, I_{out} = 0 mA, All Inputs = V_{IL} or V_{IH}, V_{IL} = 0 V and V_{IH} ≥ 3.0 V, f = f_{max})	I_{SB1}	—	75	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} – 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V, f = f_{max})	I_{SB2}	—	12	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except DQ0 – DQ17)	C_{in}	4	5	pF
Input/Output Capacitance (DQ0 – DQ17)	C_{out}	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1 Unless Otherwise Noted

READ CYCLE (See Notes 1, 2, and 3)

Parameter	Symbol	MCM67W618-12		MCM67W618-15		MCM67W618-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Times	t_{AVAV}	12	—	15	—	20	—	ns	4
Access Times:								ns	5
Address Valid to Output Valid	t_{AVQV}	—	12	—	15	—	20		
Chip Enable Low to Output Valid	t_{ELQV}	—	12	—	15	—	20		
AL High to Output Valid	t_{ALHQV}	—	12	—	15	—	20		
Output Enable Low to Output Valid	t_{GLQV}	—	6	—	7	—	8		
Byte Select Low to Output Valid	t_{BLQV}	—	6	—	7	—	8		
Setup Times:								ns	
Address Valid to Address Latch Low	t_{AVALL}	2	—	2	—	2	—		
Address Valid to Address Latch High	t_{AVALH}	0	—	0	—	0	—		
Hold Times:								ns	
Address Latch Low to Address Invalid	t_{ALLAX}	2	—	3	—	3	—		
Output Hold:								ns	
Address Invalid to Output Invalid	t_{AXQX}	4	—	4	—	4	—		
AL High to Output Invalid	t_{ALHQX}	4	—	4	—	4	—		
Address Latch Pulse Width	t_{ALHALL}	5	—	5	—	5	—	ns	
Output Buffer Control:								ns	6
Chip Enable Low to Output Active	t_{ELQX}	3	—	2	—	2	—		
Output Enable Low to Output Active	t_{GLQX}	1	—	1	—	1	—		
Byte Select Low to Output Active	t_{BLQX}	2	—	2	—	2	—		
Chip Enable High to Output High-Z	t_{EHQZ}	2	6	2	9	2	9		
Output Enable High to Output High-Z	t_{GHQZ}	2	6	2	7	2	9		
Byte Select High to Output High-Z	t_{BHQZ}	2	6	2	9	2	9		

NOTES:
1. $\overline{B}$ refers to either or both byte selects ($\overline{LB}$, $\overline{UB}$).
2. Address latch (AL) is high for all asynchronous cycles.
3. A read occurs during the overlap of $\overline{E}$ low, $\overline{W}$ high, and either or both byte enable ($\overline{LB}$, $\overline{UB}$) low.
4. All read cycle timing is referenced from the last valid address to the first transitioning address.
5. Addresses valid prior to or coincident with $\overline{E}$ low.
6. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EHQZ} is less than t_{ELQX} and t_{GHQZ} is less than t_{GLQX} for a given device.

AC TEST LOADS

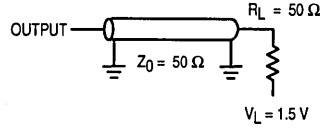


Figure 1A

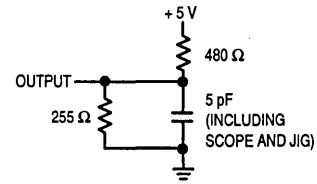
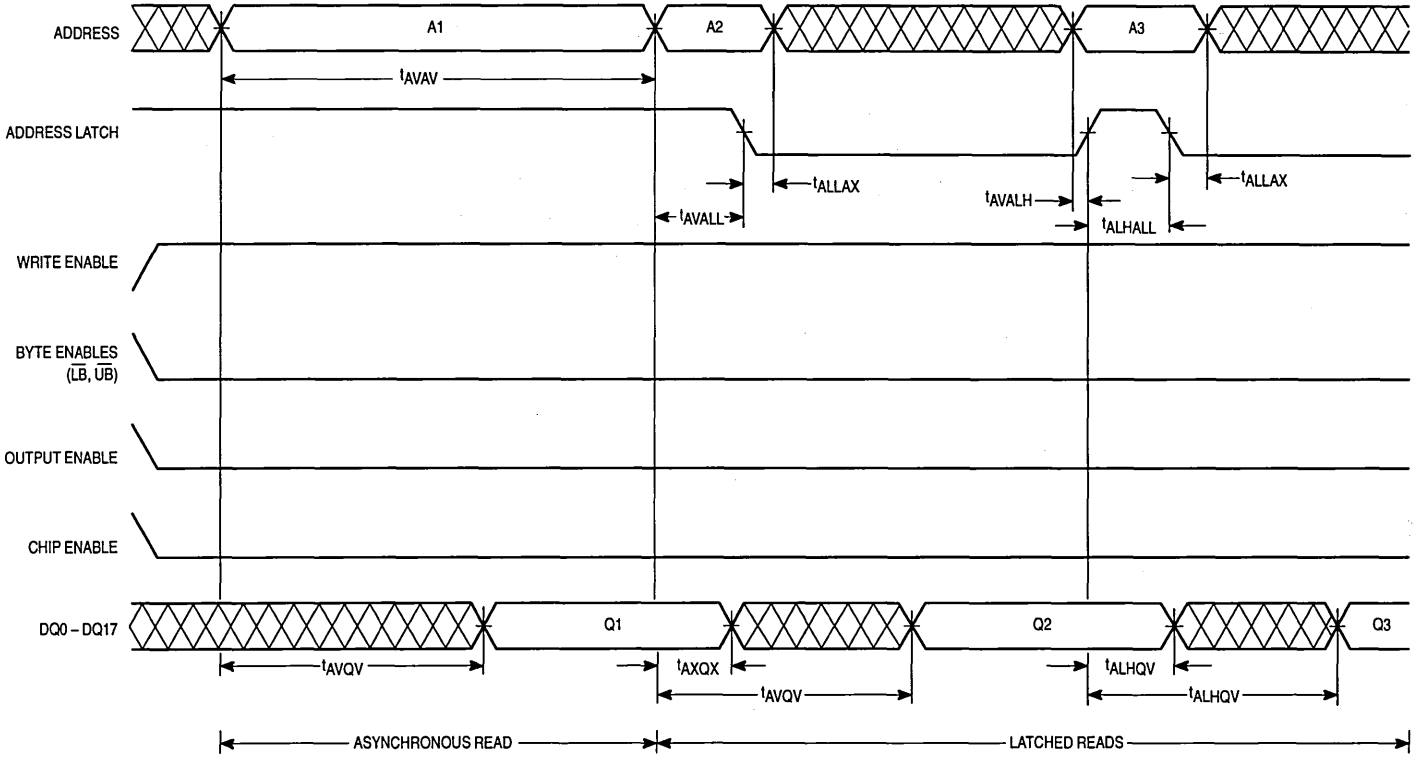


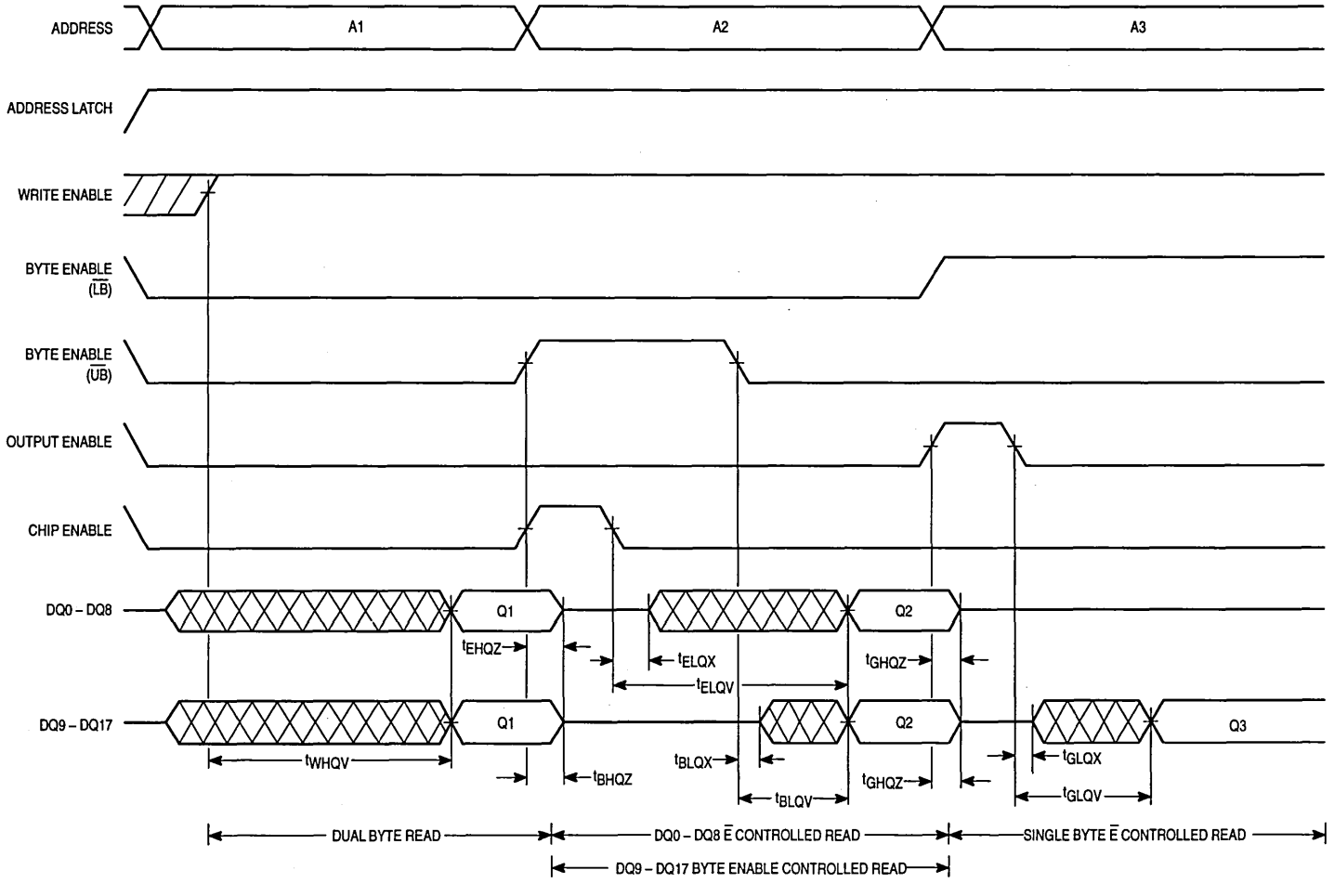
Figure 1B

NOTE: For information on output I-V characteristics, see Chapter 8, Section 1.

READ CYCLES


ADDRESS
A1
A2
A3
tAVAV
ADDRESS LATCH
tAVALL
tALLAX
tAVALH
tALHALL
tALLAX
WRITE ENABLE
BYTE ENABLES
(LB, UB)
OUTPUT ENABLE
CHIP ENABLE
DQ0 – DQ17
Q1
Q2
Q3
tAVQV
tAXQX
tAVQV
tALHQV
tALHQV
ASYNCHRONOUS READ
LATCHED READS

READ CYCLES (Continued)

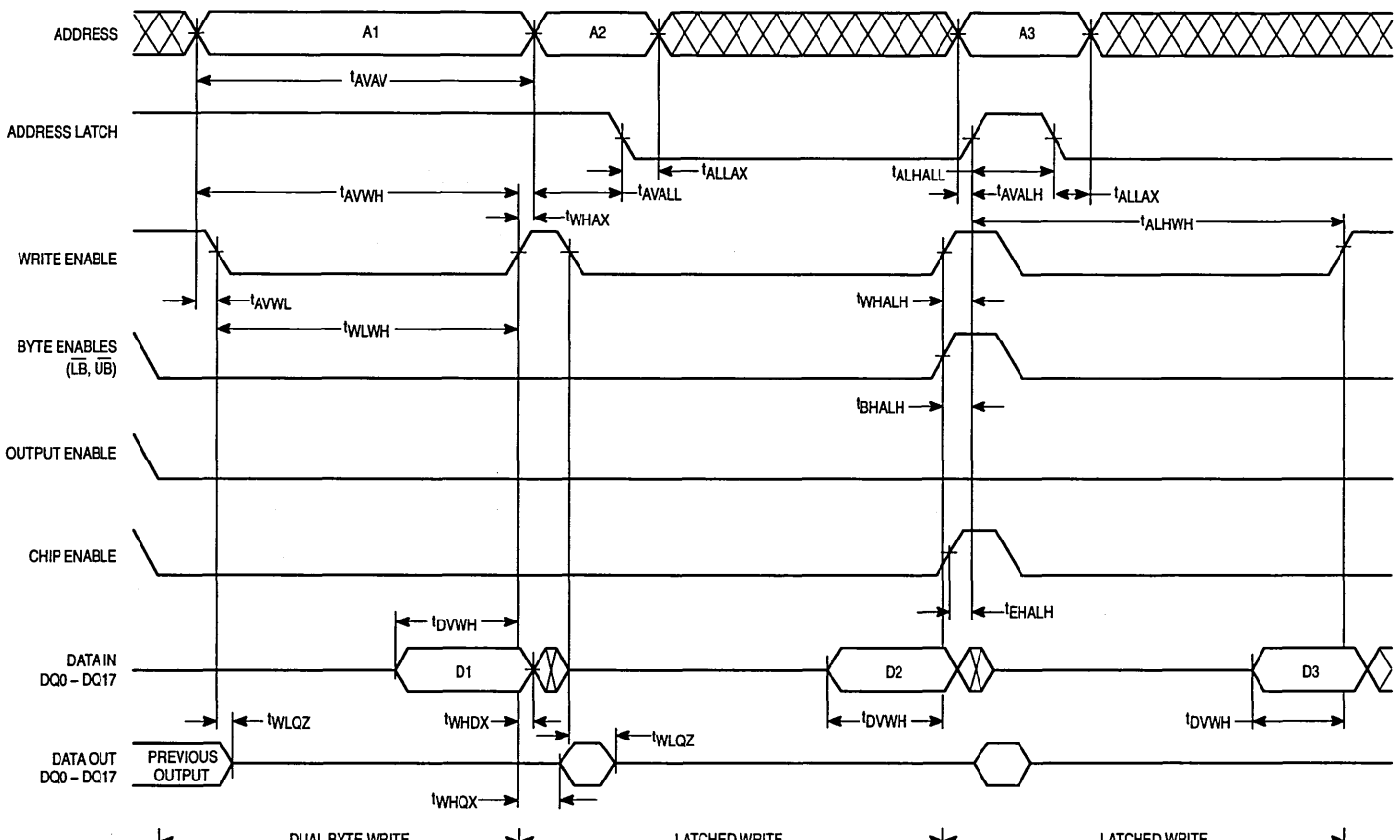


WRITE CYCLE (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM67W618-12		MCM67W618-15		MCM67W618-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	20	—	ns	5
Setup Times:								ns	
Address Valid to End of Write	t_{AVWH}	8	—	13	—	15	—		
Address Valid to Chip Enable High	t_{AVEH}	8	—	13	—	15	—		
Address Valid to Write Enable Low	t_{AVWL}	0	—	0	—	0	—		
Address Valid to Chip Enable Low	t_{AVEL}	0	—	0	—	0	—		
Data Valid to Write Enable High	t_{DVWH}	6	—	7	—	8	—		
Data Valid to Chip Enable High	t_{DVEH}	6	—	7	—	8	—		
Byte Select Low to Write Enable High	t_{BLWH}	4	—	6	—	8	—		
Byte Select High to Write Enable Low	t_{BHWL}	0	—	0	—	0	—		
Byte Select Low to Chip Enable High	t_{BLEH}	4	—	6	—	8	—		
Address Latch High Write Low	t_{ALHWL}	0	—	0	—	0	—		
Address Valid to Address Latch Low	t_{AVALL}	2	—	2	—	2	—		
Address Valid to Address Latch High	t_{AVALH}	0	—	0	—	0	—		
Hold Times:								ns	
Write Enable High to Address Invalid	t_{WHAX}	0	—	0	—	0	—		
Chip Enable High to Address Invalid	t_{EHAX}	0	—	0	—	0	—		
Byte Select High to Address Invalid	t_{BHAX}	0	—	0	—	0	—		
Write Enable High to Data Invalid	t_{WHDX}	0	—	0	—	0	—		
Chip Enable High to Data Invalid	t_{EHDX}	0	—	0	—	0	—		
Byte Select High to Data Invalid	t_{BHDX}	0	—	0	—	0	—		
Write Enable High to Byte Enable Invalid	t_{WHBX}	2	—	2	—	2	—		
Chip Enable High to Byte Enable Invalid	t_{EHBX}	2	—	2	—	2	—		
Address Latch Low to Address Invalid	t_{ALLAX}	2	—	3	—	3	—		
Write Enable High to Address Latch High	t_{WHALH}	0	—	0	—	0	—		
Byte Select High to Address Latch High	t_{BHALH}	0	—	0	—	0	—		
Write Pulse Width:								ns	
Write Pulse Width ($\overline{G}$ Low)	t_{WLWH}	8	—	13	—	15	—		
Write Pulse Width ($\overline{G}$ High)	t_{WLWH}	7	—	12	—	14	—		
Write Pulse Width	t_{WLEH}	8	—	13	—	15	—		6
Chip Enable to End of Write	t_{ELWH}	8	—	13	—	15	—		7
Chip Enable to End of Write	t_{ELEH}	8	—	13	—	15	—		6, 7
Address Latch High to Write Enable High	t_{ALHWH}	8	—	13	—	15	—		
Address Latch Pulse Width	t_{ALHALL}	5	—	5	—	5	—	ns	
Output Buffer Control:								ns	
Write Enable High to Output Active	t_{WHQX}	3	—	5	—	5	—		8
Write Enable Low to Output High-Z	t_{WLQZ}	0	6	0	9	0	9		8, 9

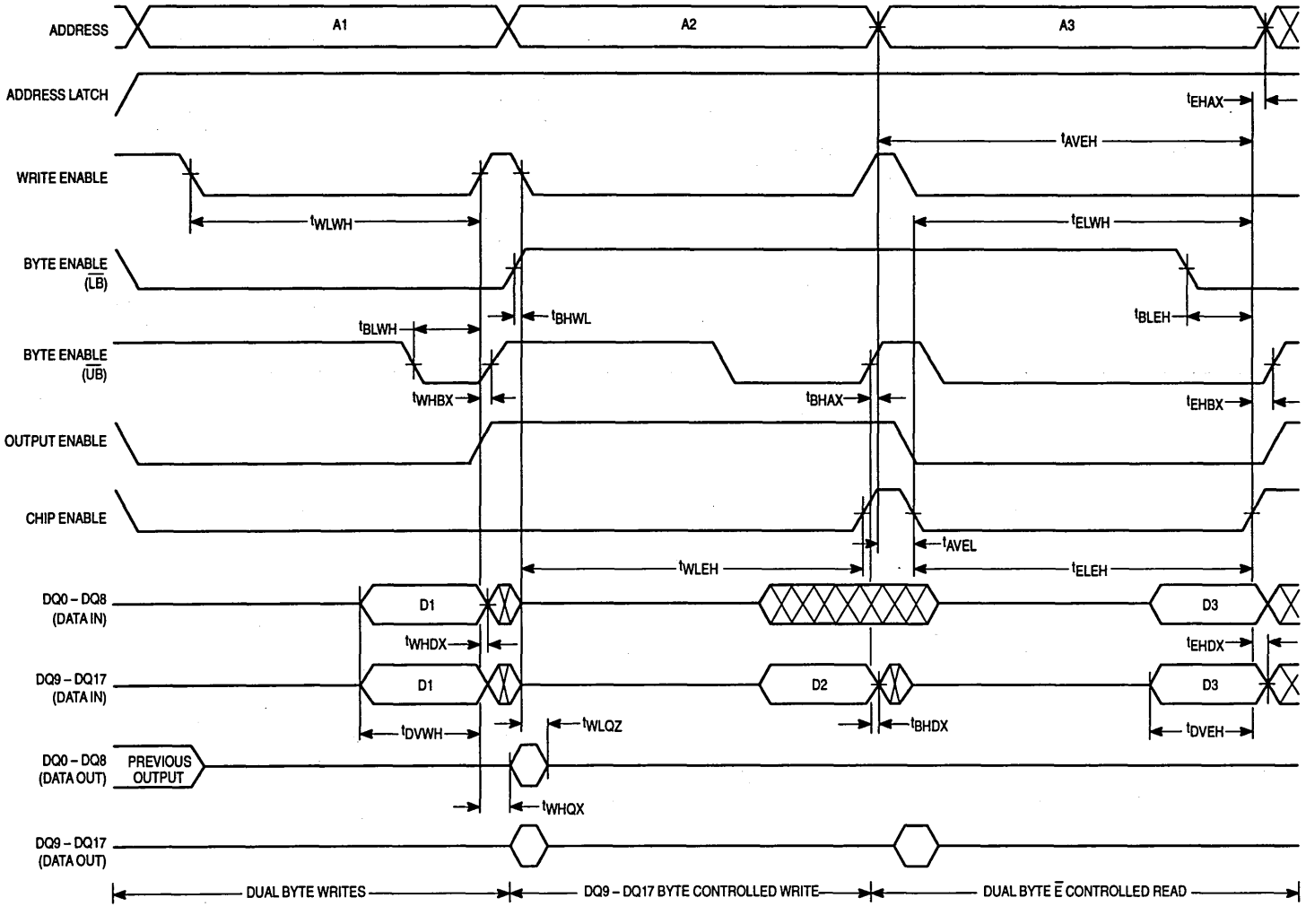
NOTES:
1. $\overline{B}$ refers to either or both byte selects ($\overline{LB}$, $\overline{UB}$).
2. Address latch (AL) is high for all asynchronous cycles.
3. A write occurs during the overlap of $\overline{E}$ low, $\overline{W}$ low, and either or both byte enable ($\overline{LB}$, $\overline{UB}$) low.
4. Write enable must be equal to V_{IH} for all address transitions.
5. All write cycle timing is referenced from the last valid address to the first transitioning address.
6. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
7. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
8. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high the output will remain in a high impedance state.
9. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{EHQZ} is less than t_{ELQX} and t_{GHQZ} is less than t_{GLQX} for a given device.

WRITE CYCLES

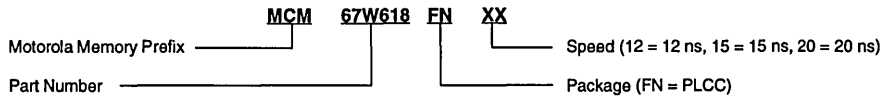


4

WRITE CYCLES (Continued)



ORDERING INFORMATION
(Order by Full Part Number)



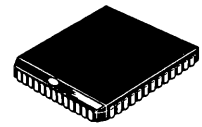
Full Part Numbers — MCM67W618FN12 MCM67W618FN15 MCM67W618FN20

4

MCM67D709

Product Preview

128K x 9 Bit Synchronous Dual I/O or Separate I/O Fast Static RAM



FN PACKAGE
PLASTIC
CASE 778

The MCM67D709 is a 1,179,648 bit synchronous static random access memory organized as 131,072 words of 9 bits, fabricated using Motorola's high-performance silicon-gate BiCMOS technology. The device integrates a 128K x 9 SRAM core with advanced peripheral circuitry consisting of address registers, two sets of input data registers and two sets of output latches. This device has increased output drive capability supported by multiple power pins.

Asynchronous inputs include the processor output enable ($\overline{POE}$) and the system output enable ($\overline{SOE}$).

The address inputs (A0 – A16) are synchronous and are registered on the falling edge of clock (K). Write enable ($\overline{W}$), processor input enable ($\overline{PIE}$) and system input enable ($\overline{SIE}$) are registered on the rising edge of clock (K). Writes to the RAM are self-timed.

All data inputs/outputs, PDQ0 – PDQ7, SDQ0 – SDQ7, PDQP, and SDQP have input data registers triggered by the rising edge of the clock. These pins also have three-state output latches which are transparent during the high level of the clock and latched during the low level of the clock.

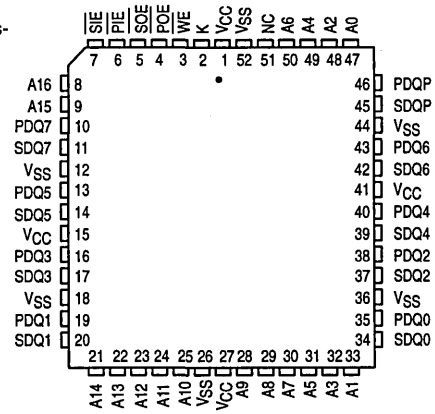
This device has a special feature which allows data to be passed through the RAM between the system and processor ports in either direction. This streaming is accomplished by latching in data from one port and asynchronously output enabling the other port. It is also possible to write to the RAM while streaming.

The MCM67D709's dual I/Os can be used in x9 separate I/O applications. Common I/Os PDQ0 – 7, PDQP and SDQ0 – 7, SDQP can be treated as either inputs (D) or outputs (Q) depending on the state of the control pins. In order to dedicate PDQ0 – 7, PDQP as data (D) inputs and SDQ0 – 7, SDQP as outputs (Q), tie $\overline{SIE}$ and $\overline{POE}$ high. $\overline{SOE}$ becomes the asynchronous $\overline{G}$ for the outputs. $\overline{PIE}$ will need to track $\overline{W}$ for proper write/read operations.

This device is ideally suited for pipelined systems and systems with multiple data buses and multi-processing systems, where a local processor has a bus isolated from a common system bus.

- Single 5 V ± 5% Power Supply
- 88110/88410 Compatibility: –16/60 MHz, –20/50 MHz
- Self-Timed Write Cycles
- Clock Controlled Output Latches
- Address and Data Input Registers
- Common Data Inputs and Data Outputs
- Dual I/O for Separate Processor and Memory Buses
- Separate Output Enable Controlled Three-State Outputs
- 3.3 V I/O Compatible
- High Board Density 52 Lead PLCC Package
- Can be used as Separate I/O x9 SRAM

PIN ASSIGNMENT

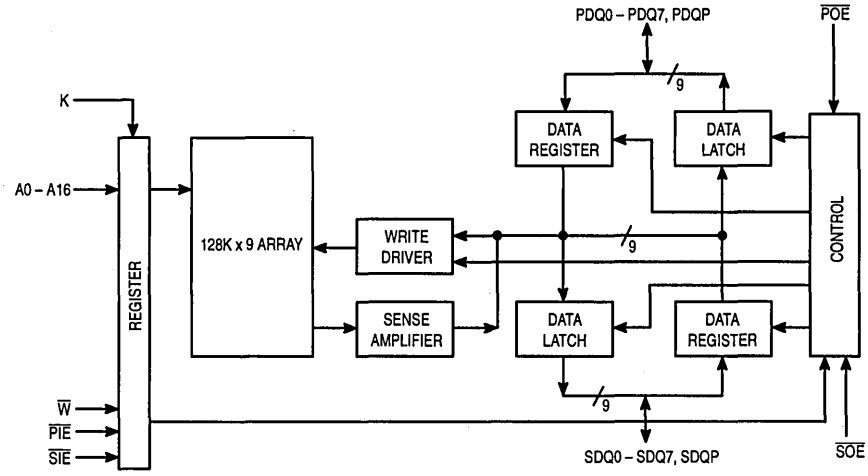


PIN NAMES	
A0 – A16	Address Inputs
K	Clock Input
$\overline{W}$	Write Enable
$\overline{PIE}$	Processor Input Enable
$\overline{SIE}$	System Input Enable
$\overline{POE}$	Processor Output Enable
$\overline{SOE}$	System Output Enable
PDQ0 – PDQ7	Processor Data I/O
PDQP	Processor Data Parity
SDQ0 – SDQ7	System Data I/O
SDQP	System Data Parity
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM



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FUNCTIONAL TRUTH TABLE (See Notes 1 and 2)

$\overline{W}$	$\overline{PIE}$	$\overline{SIE}$	$\overline{POE}$	$\overline{SOE}$	Mode	Memory Subsystem Cycle	PDQ0 – PDQ7, PDQP Output	SDQ0 – SDQ7, SDQP Output	Notes
1	1	1	0	1	Read	Processor Read	Data Out	High-Z	3
1	1	1	1	0	Read	Copy Back	High-Z	Data Out	3
1	1	1	0	0	Read	Dual Bus Read	Data Out	Data Out	3
1	X	X	1	1	Read	NOP	High-Z	High-Z	
X	0	0	X	X	N/A	NOP	High-Z	High-Z	2, 4
0	0	1	1	1	Write	Processor Write Hit	Data In	High-Z	2, 5
0	1	0	1	1	Write	Allocate	High-Z	Data In	2, 5
0	0	1	1	0	Write	Write Through	Data In	Stream Data	2, 6
0	1	0	0	1	Write	Allocate With Stream	Stream Data	Data In	2, 6
1	0	1	1	0	N/A	Cache Inhibit Write	Data In	Stream Data	2, 6
1	1	0	0	1	N/A	Cache Inhibit Read	Stream Data	Data In	2, 6
0	1	1	X	X	N/A	NOP	High-Z	High-Z	4
X	0	1	0	0	N/A	Invalid	Data In	Stream	2, 7
X	0	1	0	1	N/A	Invalid	Data In	High-Z	2, 7
X	1	0	0	0	N/A	Invalid	Stream	Data In	2, 7
X	1	0	1	0	N/A	Invalid	High-Z	Data In	2, 7

NOTES:

1. A '0' represents an input voltage ≤ V_{IL} and a '1' represents an input voltage ≥ V_{IH}. All inputs must satisfy the specified setup and hold times for the falling or rising edge of K. Some entries in this truth table represent latched values. Other possible combinations of control inputs not covered by this note or the table above are not supported and the RAMs behavior is not specified.
2. If either $\overline{IE}$ signal is sampled low on the rising edge of clock, the corresponding $\overline{OE}$ is a don't care, and the corresponding outputs are High-Z.
3. A read cycle is defined as a cycle where data is driven on the internal data bus by the RAM.
4. No RAM cycle is performed.
5. A write cycle is defined as a cycle where data is driven onto the internal data bus through one of the data I/O ports (PDQ0 – PDQ7 and PDQP or SDQ0 – SDQ7 and SPDQ), and written into the RAM.
6. Data is driven on the internal data bus by one I/O port through its data input register and latched into the data output latch of the other I/O port.
7. Data contention will occur.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{POE}$, $\overline{SOE}$ = V_{IH})	$I_{lkg(O)}$	—	± 1.0	µA
AC Supply Current (All Inputs = V_{IL} or V_{IH}, V_{IL} = 0.0 V and V_{IH} ≥ 3.0 V, I_{out} = 0 mA, Cycle Time ≥ t_{KHKH} min) MCM67D709-16: t_{KHKH} = 16 ns MCM67D709-20: t_{KHKH} = 20 ns	I_{CCA}	— — —	 280 260	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (All Pins Except I/Os)	C_{in}	5	6	pF
Input/Output Capacitance (PDQ0 – PDQ7, SDQ0 – SDQ7, PDQP, SDQP)	C_{out}	6	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Output Measurement Timing Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	60 MHz MCM67D709-16 Min	60 MHz MCM67D709-16 Max	50 MHz MCM67D709-20 Min	50 MHz MCM67D709-20 Max	Unit	Notes
Read Cycle Time Clock High to Clock High	t_{KHKH}	16	—	20	—	ns	1, 2
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	7	—	7	—	ns	
Clock High to Output Valid	t_{KHQV}	—	6	—	7.5	ns	3
Clock (K) High to Output Low Z After Write	t_{KHQX1}	0	—	0	—	ns	
Output Hold from Clock High	t_{KHQX2}	2	—	3	—	ns	3, 4
Setup Times: A	t_{AVKL}	2	—	2	—	ns	
$\overline{W}$	t_{WHKH}	2		2			
$\overline{PIE}$	t_{PIEHKH}	2		2			
$\overline{SIE}$	t_{SIEHKH}	2		2			
Hold Times: A	t_{KLAX}	2	—	2	—	ns	
$\overline{W}$	t_{KHWX}	2		2			
$\overline{PIE}$	t_{KHPIEX}	2		2			
$\overline{SIE}$	t_{KHSIEX}	2		2			
Output Enable High to Q High-Z	t_{POEHQZ} / t_{SOEHQZ}	0	5	0	8	ns	4
Output Hold from Output Enable High	t_{POEHQX} / t_{SOEHQX}	2	—	5	—	ns	4
Output Enable Low to Q Active	t_{POELQX} / t_{SOELQX}	0	—	0	—	ns	4
Output Enable Low to Output Valid	t_{POELQV} / t_{SOELQV}	—	5	—	6	ns	

NOTES:
1. A read is defined by $\overline{W}$ high for the setup and hold times.
2. All read cycle timing is referenced from K, $\overline{SOE}$, or $\overline{POE}$.
3. K must be at a high level for outputs to transition.
4. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX}, t_{POEHQZ} is less than t_{POELQX} for a given device, and t_{SOEHQZ} is less than t_{SOELQX} for a given device.

AC SPEC LOADS

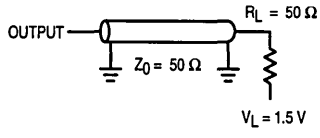


Figure 1A

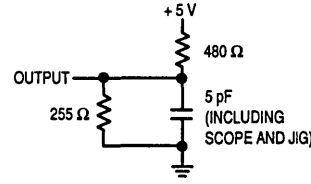
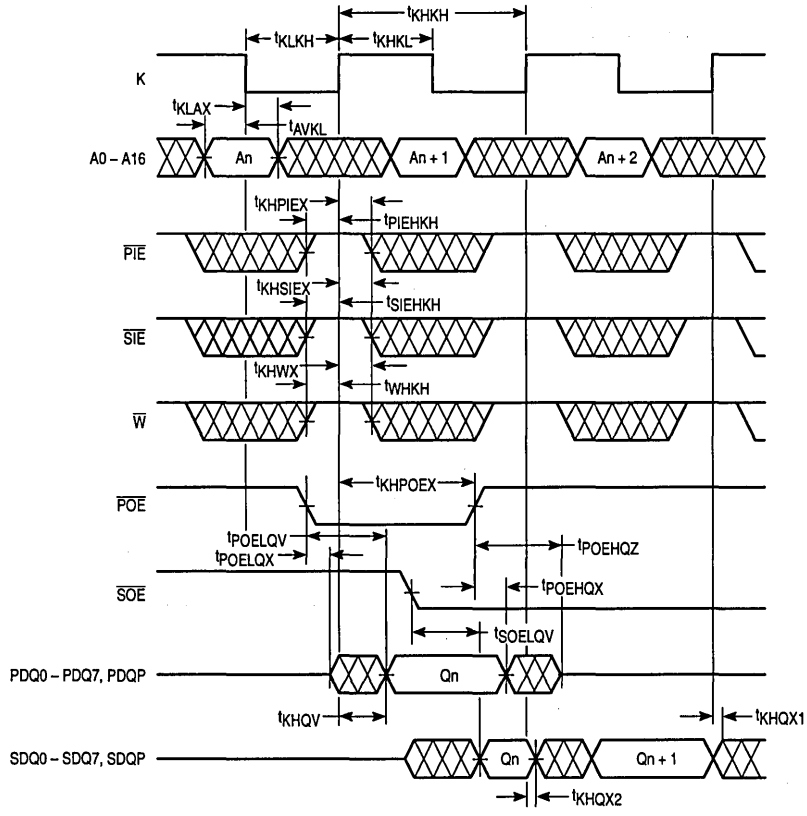


Figure 1B

READ CYCLE (See Note)



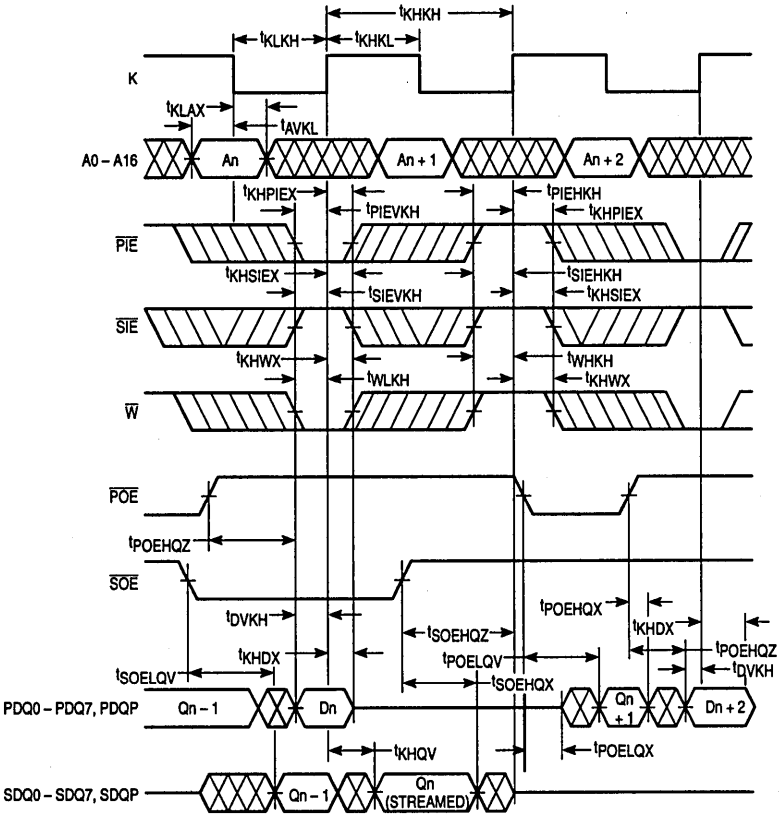
WRITE CYCLE (See Note 1)

Parameter	Symbol	60 MHz MCM67D709-16 Min	60 MHz MCM67D709-16 Max	50 MHz MCM67D709-20 Min	50 MHz MCM67D709-20 Max	Unit	Notes
Write Cycle Times	t_{KHKH}	16	—	20	—	ns	1, 2
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	7	—	7	—	ns	
Clock High to Output High-Z ($\overline{W}$ = V_{IL} and $\overline{SIE}$ = $\overline{PIE}$ = V_{IH})	t_{KHQZ}	—	8	—	8	ns	3, 4
Setup Times: A	t_{AVKL}	2	—	2	—	ns	
$\overline{W}$	t_{WLKH}	2		2			
$\overline{PIE}$	t_{PIEVKH}	2		2			
$\overline{SIE}$	t_{SIEVKH}	2		2			
SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{DVKH}	2		2			
Hold Times: A	t_{KLAX}	2	—	2	—	ns	
$\overline{W}$	t_{KHWX}	2		2			
$\overline{PIE}$	t_{KHPIEX}	2		2			
$\overline{SIE}$	t_{KHSIEX}	2		2			
SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{KHDX}	2		2			
Write with Streaming ($\overline{PIE}$ = $\overline{SOE}$ = V_{IL} or $\overline{SIE}$ = $\overline{POE}$ = V_{IL}) Clock High to Output Valid	t_{KHQV}	—	5	—	7	ns	5
Output Enable High to Q High-Z	t_{POEHQZ} t_{SOEHQZ}	0	5	0	8	ns	6
Output Hold from Output Enable High	t_{POEHQX} t_{SOEHQX}	2	—	5	—	ns	6
Output Enable Low to Q Active	t_{POELQX} t_{SOELQX}	0	—	0	—	ns	6
Output Enable Low to Output Valid	t_{POELQV} t_{SOELQV}	—	5	—	6	ns	

NOTES:

1. A write is performed with $\overline{W}$ = V_{IL} for the specified setup and hold times and either $\overline{PIE}$ = V_{IL} or $\overline{SIE}$ = V_{IL}. If both $\overline{PIE}$ = V_{IL} and $\overline{SIE}$ = V_{IL} or $\overline{PIE}$ = V_{IH} and $\overline{SIE}$ = V_{IH}, then this is treated like a NOP and no write is performed.
2. All write cycle timings are referenced from K.
3. K must be at a high level for the outputs to transition.
4. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX} for a given device.
5. A write with streaming is defined as a write cycle which writes data from one data bus to the array and outputs the same data onto the other data bus.
6. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{KHQZ} is less than t_{KHQX}, t_{POEHQZ} is less than t_{POELQX} for a given device, and t_{SOEHQZ} is less than t_{SOELQX} for a given device.

WRITE THROUGH — READ — WRITE

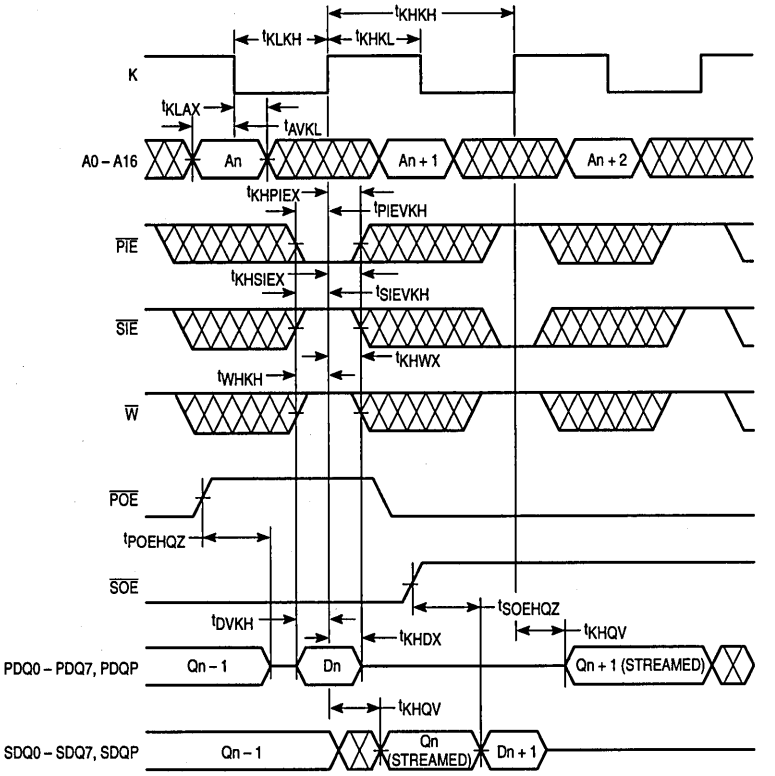


STREAM CYCLE (See Note 1)

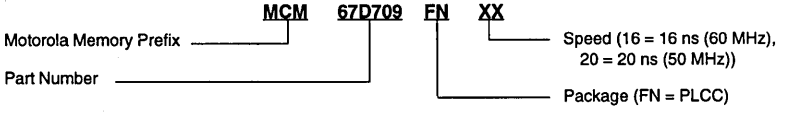
Parameter	Symbol	60 MHz MCM67D709-16 Min	60 MHz MCM67D709-16 Max	50 MHz MCM67D709-20 Min	50 MHz MCM67D709-20 Max	Unit	Notes
Stream Cycle Time	t_{KHKH}	16	—	20	—	ns	1, 2
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	7	—	7	—	ns	
Stream Access Time	t_{KHQV}	—	6	—	7	ns	
Setup Times: A	t_{AVKL}	2	—	2	—	ns	
$\overline{W}$	t_{WHKH}	2		2			
$\overline{PIE}$	t_{PIEVKH}	2		2			
$\overline{SIE}$	t_{SIEVKH}	2		2			
SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{DVKH}	2		2			
Hold Times: A	t_{KLAX}	2	—	2	—	ns	
$\overline{W}$	t_{KHWX}	2		2			
$\overline{PIE}$	t_{KHPIEX}	2		2			
$\overline{SIE}$	t_{KHSIEX}	2		2			
SDQ0 – SDQ7, SDQP, PDQ0 – PDQ7, PDQP	t_{KHDX}	2		2			
Output Enable High to Q High-Z	t_{POEHQZ} t_{SOEHQZ}	0	5	0	8	ns	3
Output Enable Low to Q Active	t_{POELQX} t_{SOELQX}	0	—	0	—	ns	3
Output Enable Low to Output Valid	t_{POELQV} t_{SOELQV}	—	5	—	6	ns	

NOTES:
1. A stream cycle is defined as a cycle where data is passed from one data bus to the other data bus.
2. All stream cycle timing is referenced from K.
3. Transition is measured ± 500 mV from steady-state voltage with output load of Figure 1B. This parameter is sampled and not 100% tested. At any given voltage and temperature, t_{POEHQZ} is less than t_{POELQX}, t_{SOEHQZ} is less than t_{SOELQX}, and t_{KHQZ} is less than t_{KHQX} for a given device.

STREAM CYCLE



ORDERING INFORMATION
(Order by Full Part Number)

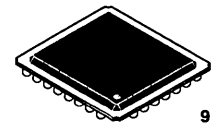


Full Part Numbers — MCM67D709FN16 MCM67D709FN20

MCM67Q709

Product Preview

128K x 9 Bit Separate I/O Synchronous Fast Static RAM



9 x 10 GRID
86 BUMP OMPAC
CASE 896A-01

The Motorola MCM67Q709 is a 1,179,648 bit static random access memory, organized as 131,072 words of 9 bits. This device is fabricated using Motorola's high-performance silicon-gate BiCMOS technology. It features separate TTL input and output buffers, which are fully I/O compatible at 3.3 V, and incorporates input and output registers on board with high speed SRAM. It also features transparent-write and data pass-through capabilities.

The synchronous design allows for precise cycle control with the use of an external single clock (K). The Addresses (A0 – A16), Data Input (D0 – D8), Data Output (Q0 – Q8), Write-Enable ($\overline{W}$), Chip-Enable ($\overline{E}$), and Output-Enable ($\overline{G}$), are registered in on the rising edge of Clock (K).

The MCM67Q709 is available in a 9 x 10 grid, 86 bump surface mount OMPAC.

- Single 5 V ± 10% Power Supply
- Fast Cycle Times: 10/12 ns Max
- Single Clock Operation
- TTL Input and Output Levels (3.3 V I/O Compatible)
- Address, Data Input, $\overline{E}$, $\overline{W}$, $\overline{G}$, Registers on Chip
- 100 MHz Maximum Clock Cycle Time
- Self Timed Write
- Separate Data Input and Output Pins
- Transparent-Write or Data Pass-Through
- High Output Drive Capability: 50 pF/Output at Rated Access Time
- Boundary Scan Implementation

PIN NAMES	
A0 – A16	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0 – D8	Data Inputs
Q0 – Q8	Data Outputs
K	Clock Input
TCK	Test Clock Input
TMS	Test Mode Select
TDI	Test Data Input
TDO	Test Data Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

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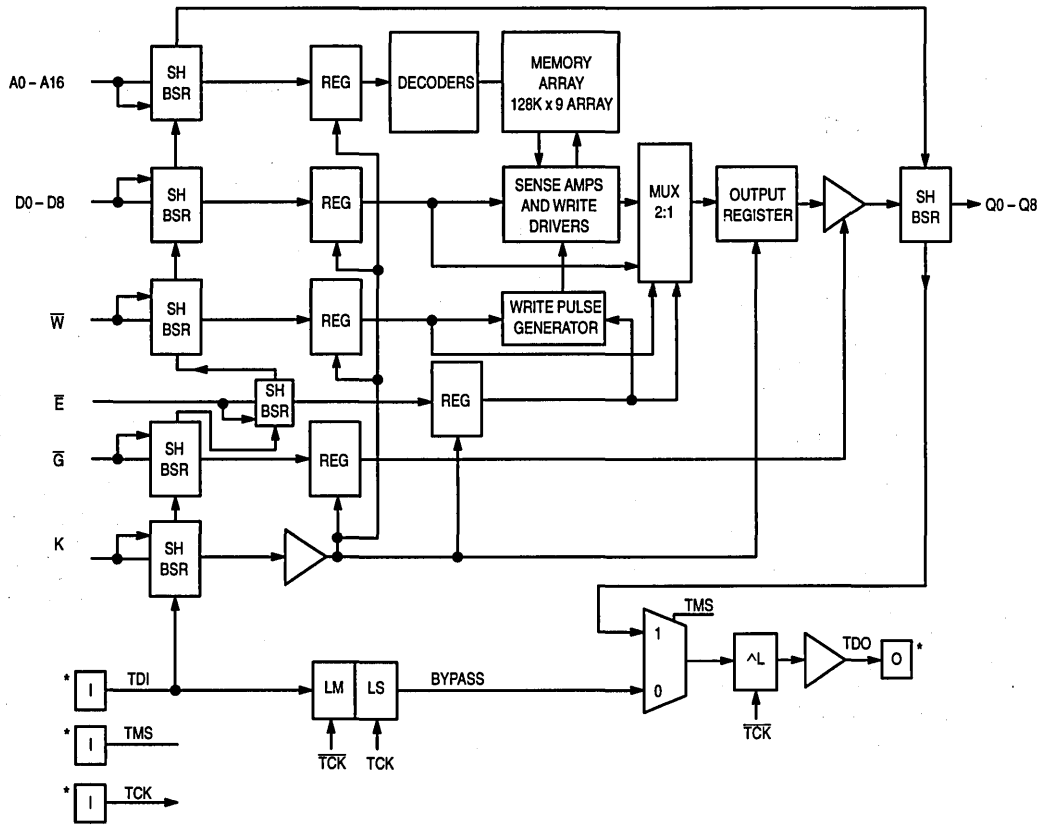
This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

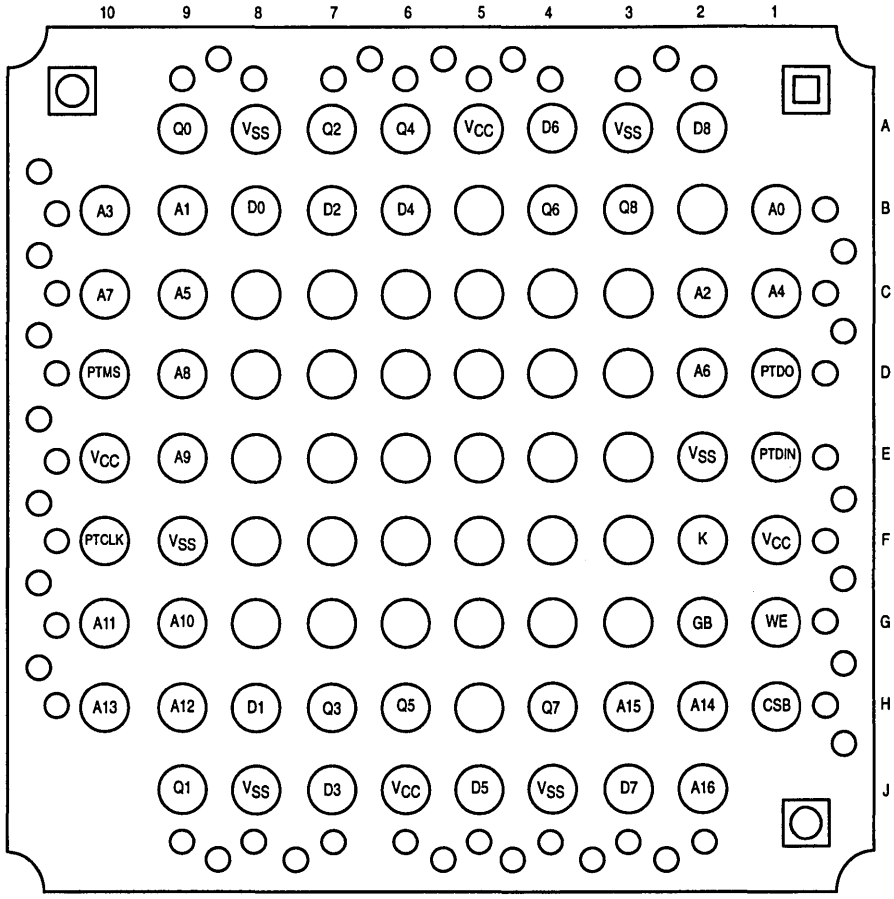
BLOCK DIAGRAM



NOTES:
1. Bypass is with TSENOT ($\overline{TSE}$) and TCK.
2. Boundary Scan only samples inputs.
3. SH BSR = Shadow Bypass Scan Register.

*Four added test pins.

VIEW OF PACKAGE BOTTOM



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TRUTH TABLE

$\overline{E}$ (t_n)	$\overline{W}$ (t_n)	$\overline{G}$ (t_{n+1})	Mode	D0 – D3	Q0 – Q3 (t_{n+1})	V_{CC} Current
L	L	L	Write and Pass Thru	Valid	D0 – D3 (t_n)	I_{CC}
		H	Write	Valid	High-Z	I_{CC}
H	L	L	Pass Thru	Valid	D0 – D3 (t_n)	I_{CC}
		H	NOP	Don't Care	High-Z	I_{CC}
X	H	L	Read	Don't Care	Q_{out} (t_n)	I_{CC}
		H	Read	Don't Care	High-Z	I_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This is a synchronous device. All synchronous inputs must meet specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) whie the device is selected.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	MCM67Q709-10	MCM67Q709-12	Unit
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	210	200	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address and Data Input Capacitance	C_{in}	6	pF
Control Pin Input Capacitance	C_{in}	6	pF
Output Capacitance	C_{out}	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol		MCM67Q709-10		MCM67Q709-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	t_{CYC}	10	—	12	—	ns	1
Clock Access Time	t_{KHQV}	t_{CD}	—	5	—	6	ns	2
Clock Low Pulse Width	t_{KLKH}	t_{CL}	4	—	4	—	ns	
Clock High Pulse Width	t_{KHKL}	t_{CH}	4	—	4	—	ns	
Clock High to Data Output Invalid	t_{KHQX}	t_{DC1}	2	—	2	—	ns	
Clock High to Data Output High-Z	t_{KHQZ}	t_{CZ}	—	5	—	6	ns	
Setup Times: A	t_{AVKH}	t_{AS}	2	—	2	—	ns	3
$\overline{W}$	t_{WVKH}	t_{WS}						
$\overline{E}$	t_{EVKH}	t_{ES}						
$\overline{G}$	t_{GVKH}	t_{GS}						
D0 – D8	t_{DVKH}	t_{DS}						
Hold Times: A	t_{KHAX}	t_{AH}	1	—	1	—	ns	3
$\overline{W}$	t_{KHWX}	t_{WH}						
$\overline{E}$	t_{KHEX}	t_{EH}						
$\overline{G}$	t_{KHGX}	t_{GH}						
D0 – D8	t_{KHDX}	t_{DH}						

NOTES:
1. All read and write cycles are referenced from K.
2. Valid data from Clock High will be the data stored at the address or the last valid read cycle.
3. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.

AC SPEC LOADS

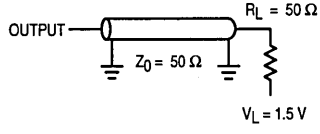


Figure 1A

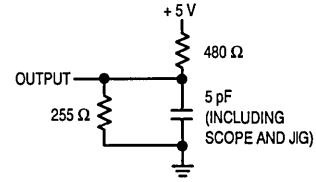
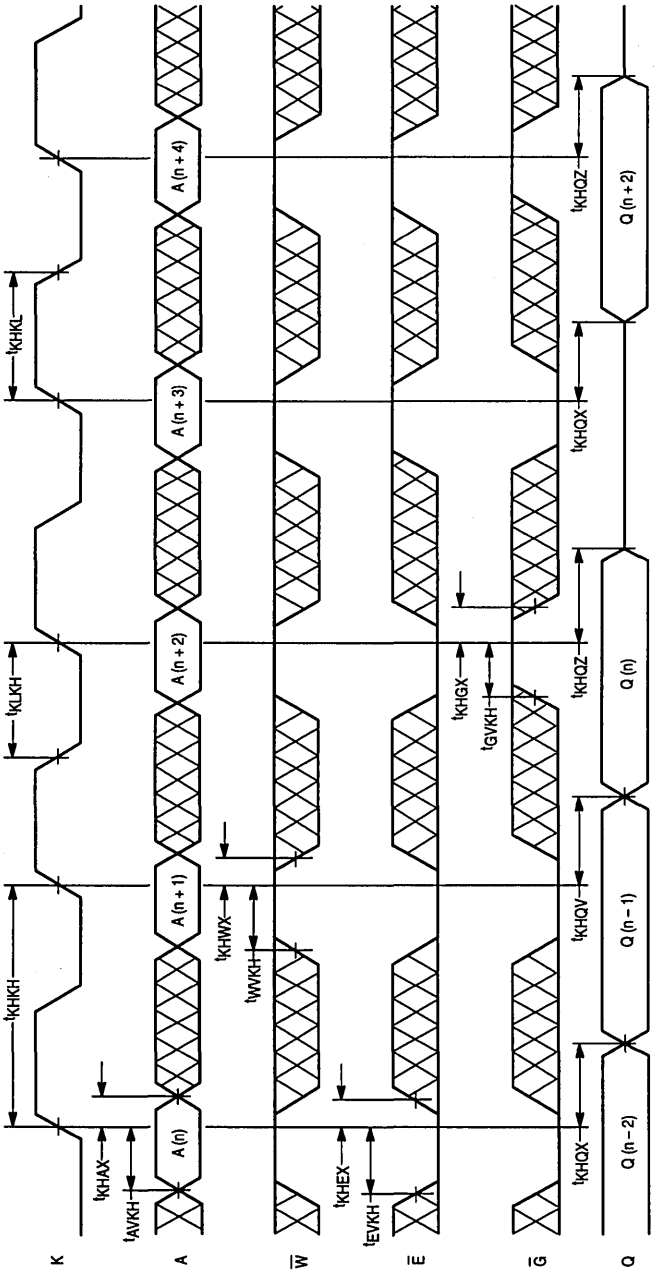
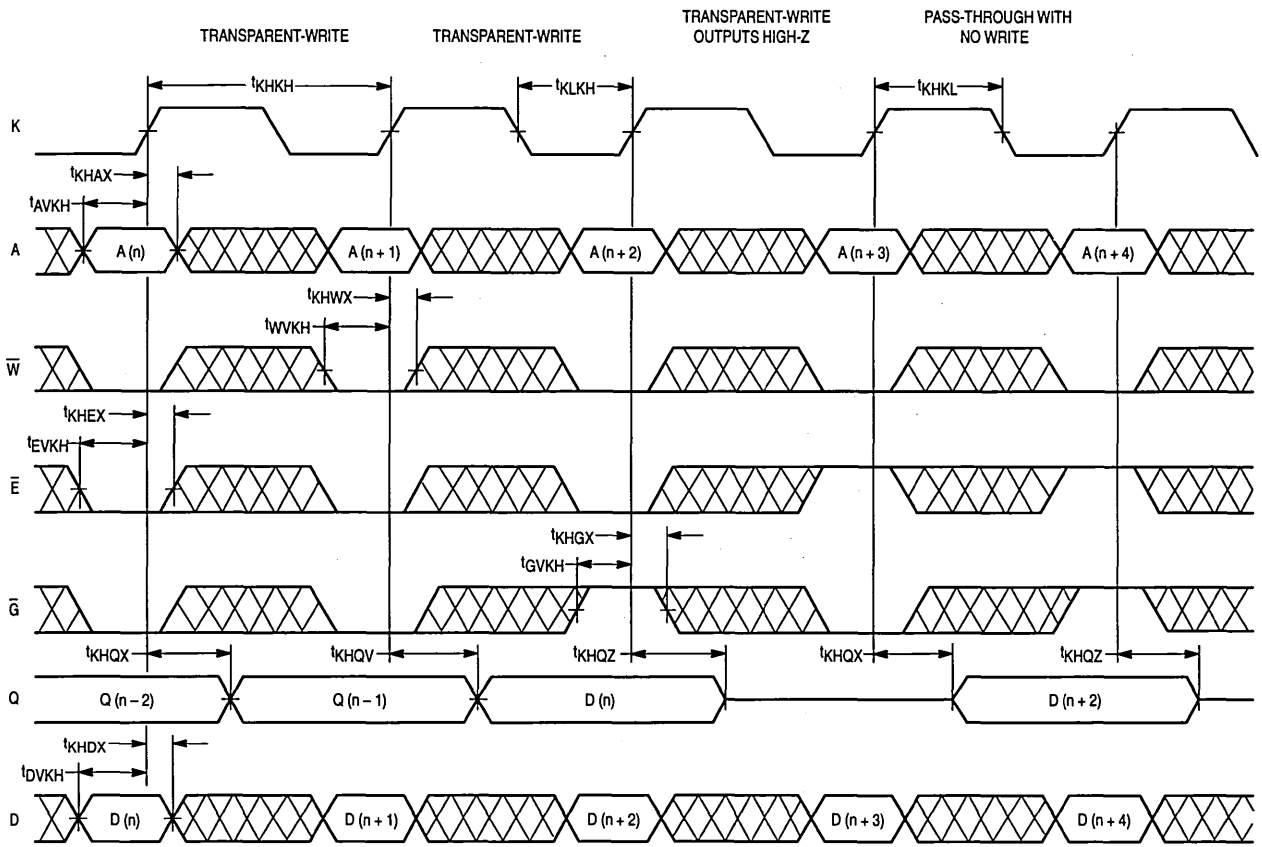


Figure 1B

READ CYCLE TIMING



WRITE AND DATA PASS-THROUGH CYCLE TIMING



BOUNDARY SCAN CYCLE TIMING

Parameter	Symbol	MCM67Q709-10		MCM67Q709-12		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{CHCH2}	100	—	100	—	ns	
Clock High Pulse Width	t_{CHCL2}	40	—	40	—	ns	
Clock Low Pulse Width	t_{CLCH2}	40	—	40	—	ns	
Scan Mode Setup	t_{SS}	10	—	10	—	ns	1
Bypass Mode Setup	t_{BS}	10	—	10	—	ns	2
Scan Mode Recovery Time	t_{SR}	100	—	100	—	ns	3
TCK Low to TMS High	t_{CLMH}	10	—	10	—	ns	4
TMS High to TCK High	t_{MHCH}	10	—	10	—	ns	5
TCK High to TMS Low	t_{CHML}	10	—	10	—	ns	6
TDI Valid to TCK High	t_{IVCH}	10	—	10	—	ns	
TCK High to TDI Don't Care	t_{CHIX}	10	—	10	—	ns	
TCK Low to TDO Valid	t_{CLOV}	—	20	—	20	ns	

NOTES:
1. The minimum delay required between ending normal operation and beginning scan operations.
2. The minimum delay required between ending Shift Mode and beginning Bypass Mode.
3. The minimum delay required before restarting normal RAM operation.
4. The minimum delay required before executing a Parallel Load operation.
5. The minimum delay required between a Parallel Load operation and a Shift.
6. Minimum Shift command hold time.

4

BOUNDARY SCAN

OVERVIEW

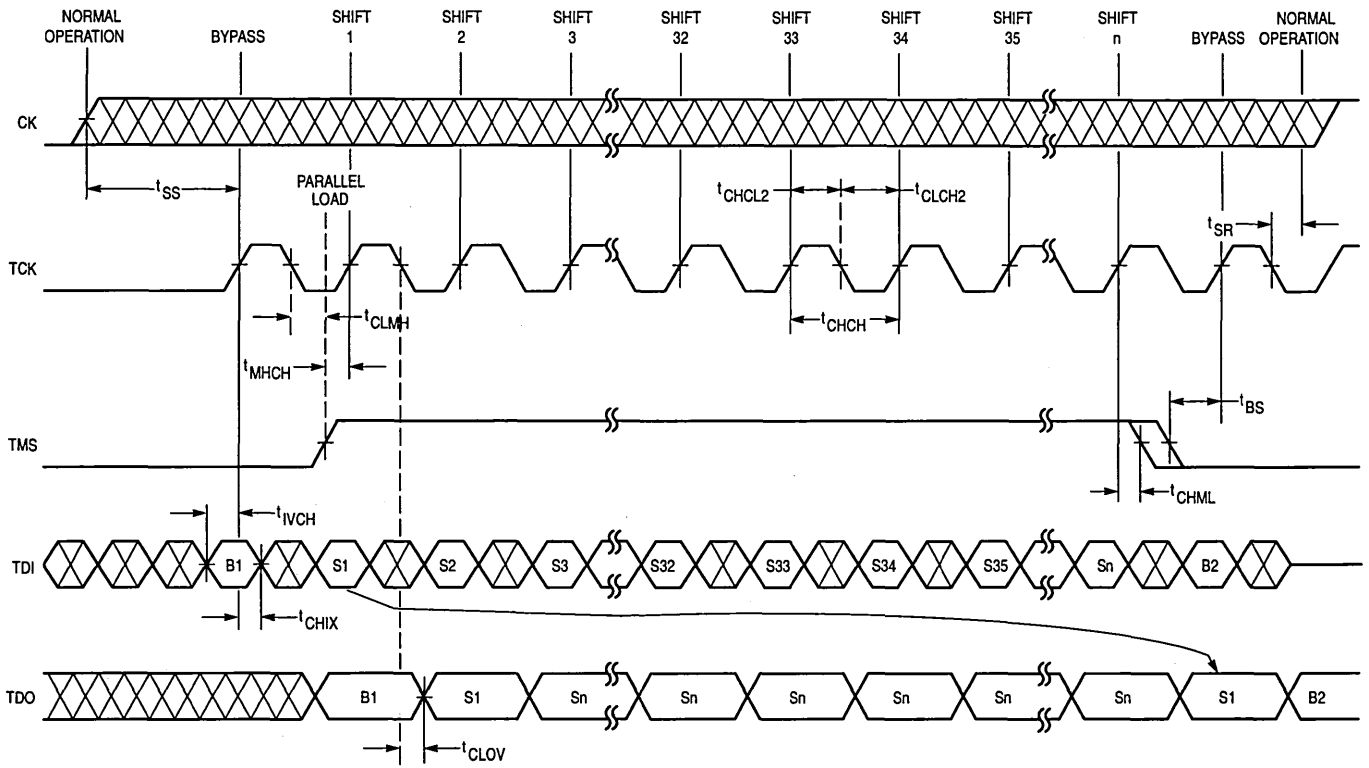
Boundary scan is a simple, non-intrusive scheme that allows verification of electrical continuity for each of a clocked RAM's logically active inputs and I/Os without adversely affecting RAM performance. Boundary scan allows the user to monitor the logic levels applied to each signal input on the RAM, and to shift them out in a serial bit stream.

OPERATION

Boundary scan requires four signal pins for implementation: Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK, active high), and TMS (Test Mode Select, active high).

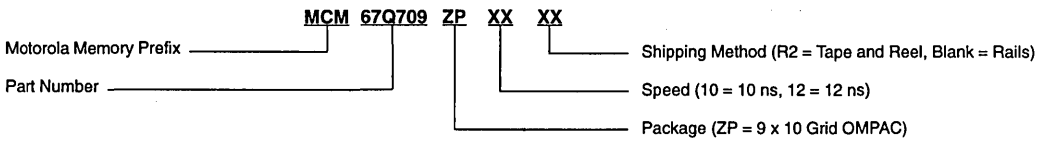
Boundary scan provides three modes of operation: (1) normal RAM operation, (2) scan, and (3) bypass. For normal RAM operation TCK and TMS must be held low. The RAM will always return to normal operation immediately after the RAM receives a rising edge of the RAM input clock (K or CK) with TCK and TMS held low. To enter scan mode, TMS is driven high, parallel loading all the scan registers, and TCK is activated. Each rising edge of TCK captures the data presented to the TDI pin. Each falling edge of TCK pushes new data onto the TDO pin. To enter bypass mode simply exercise TCK with TMS held low. In this mode TDI is sampled on the rising edge of TCK. The level found on TDI is then driven out on TDO on the next falling edge of TCK.

BOUNDARY SCAN TIMING DIAGRAM



B1 and B2 = Bypass Serial Data from outside source
S1 – Sn + 1 = Serial Scan Data from outside source
S1 – Sn = RAMs Input Register contents

ORDERING INFORMATION
(Order by Full Part Number)



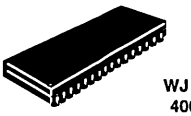
Full Part Numbers — MCM67Q709ZP10 MCM67Q709ZP12
MCM67Q709ZP10R2 MCM67Q709ZP12R2

4

MCM67F804

Product Preview

256K x 4 Bit Synchronous Static RAM with Latched Outputs



WJ PACKAGE
400 MIL SOJ
CASE 857A

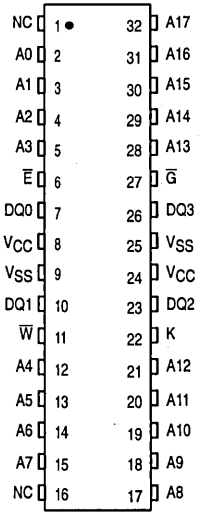
The MCM67F804 is a 1,048,576 bit static random access memory organized as 262,144 x 4 bits. This device is fabricated using Motorola's high-performance silicon-gate BiCMOS technology. It features separate TTL input and output buffers, which are fully I/O compatible at 3.3 V, and incorporates input registers and output latches on board with high speed SRAM.

The synchronous design allows for precise cycle control with the use of an external single clock (K). The Addresses (A0 – A17), Data Input (D0 – D3), Data Output (Q0 – Q3), Write-Enable ($\overline{W}$), and Chip Enable ($\overline{E}$), are registered in on the rising edge of Clock (K).

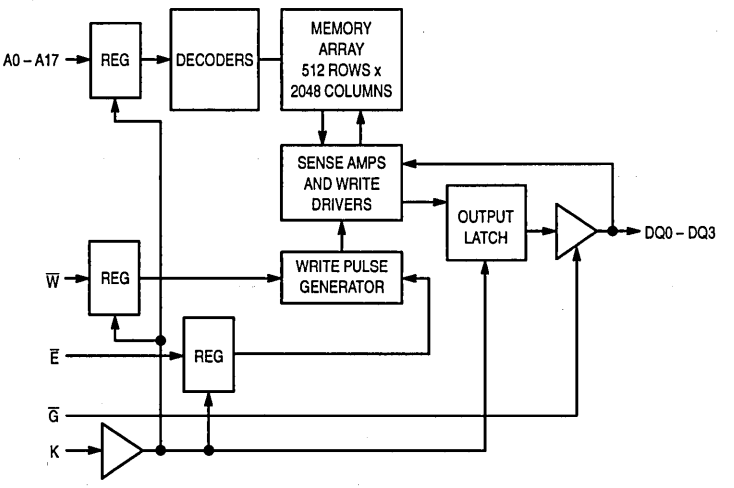
The MCM67F804 is available in a 400 mil, 32-lead surface-mount SOJ package.

- Single 5 V ± 10% Power Supply
- Fast Cycle Times: 12/15 ns Max
- Single Clock Operation
- TTL Input and Output Levels (3.3 V I/O Compatible)
- Address, Data Input, $\overline{E}$, $\overline{W}$ Registers on Chip
- Transparent Output Latches

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A17	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 – DQ3	Data Input/Output
K	Clock Input
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	Output Disabled	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	MCM67F804-12	MCM67F804-15	Unit
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	180	170	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	40	40	mA
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address and Data Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Output Capacitance	C_{out}	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol		MCM67F804-12		MCM67F804-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	t_{CYC}	12	—	15	—	ns	1
Clock Low Pulse Width	t_{KLKH}	t_{CL}	5	—	6	—	ns	2
Clock High Pulse Width	t_{KHKL}	t_{CH}	5	—	6	—	ns	
Clock High to Output Active	t_{KHQX1}	t_{DC1}	5	—	5	—	ns	
Clock High to Output Hold	t_{KHQX2}	t_{DC2}	7	—	7	—	ns	
Clock High to Q High-Z	t_{KHQZ}	t_{CZ}	—	6	—	8	ns	
Clock Access Time	t_{KHQV}	t_{CD}	—	12	—	15	ns	4
Setup Times: A	t_{AVKH}	t_{AS}	2	—	2	—	ns	3
$\overline{W}$	t_{WVKH}	t_{WS}						
$\overline{E}$	t_{EVKH}	t_{ES}						
D	t_{DVKH}	t_{DS}						
Hold Times: A	t_{KHAX}	t_{AH}	1	—	1	—	ns	3
$\overline{W}$	t_{KHWX}	t_{WH}						
$\overline{E}$	t_{KHEX}	t_{EH}						
D	t_{KHDX}	t_{DH}						
Clock Low Access Time	t_{KLQV}		—	7	—	9	ns	5
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	5	—	6	ns	
Clock Low to Output Active	t_{KLQX1}		0	—	0	—	ns	
Clock Low to Output Hold	t_{KLQX2}		2	—	2	—	ns	
Output Enable to Output Active	t_{GLQX}	t_{LZ}	0	—	0	—	ns	
Clock Low to Q High-Z	t_{KLQZ}		0	6	0	8	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{HZ}	0	6	0	8	ns	

NOTES:
1. All read and write cycles are referenced from K.
2. Valid data from Clock High will be the data stored at the address or the last valid read cycle.
3. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.
4. For Read Cycle 1 timing, clock high pulse width < ($t_{KHQV} - t_{KLQV}$).
5. For Read Cycle 2 timing, clock high pulse width ≥ ($t_{KHQV} - t_{KLQV}$).

AC SPEC LOADS

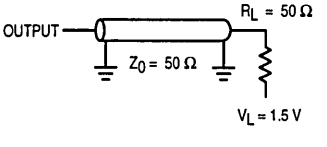


Figure 1A

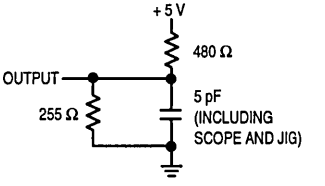
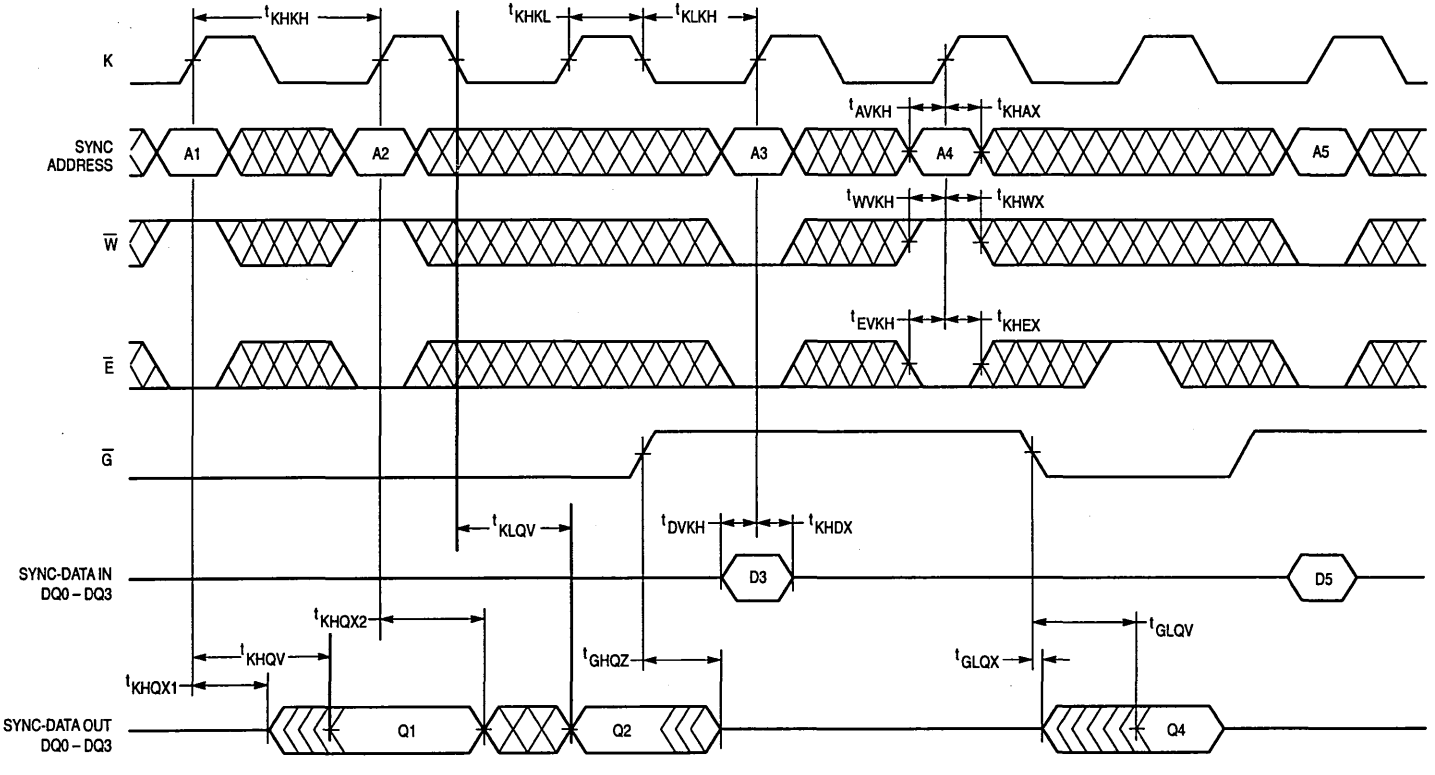
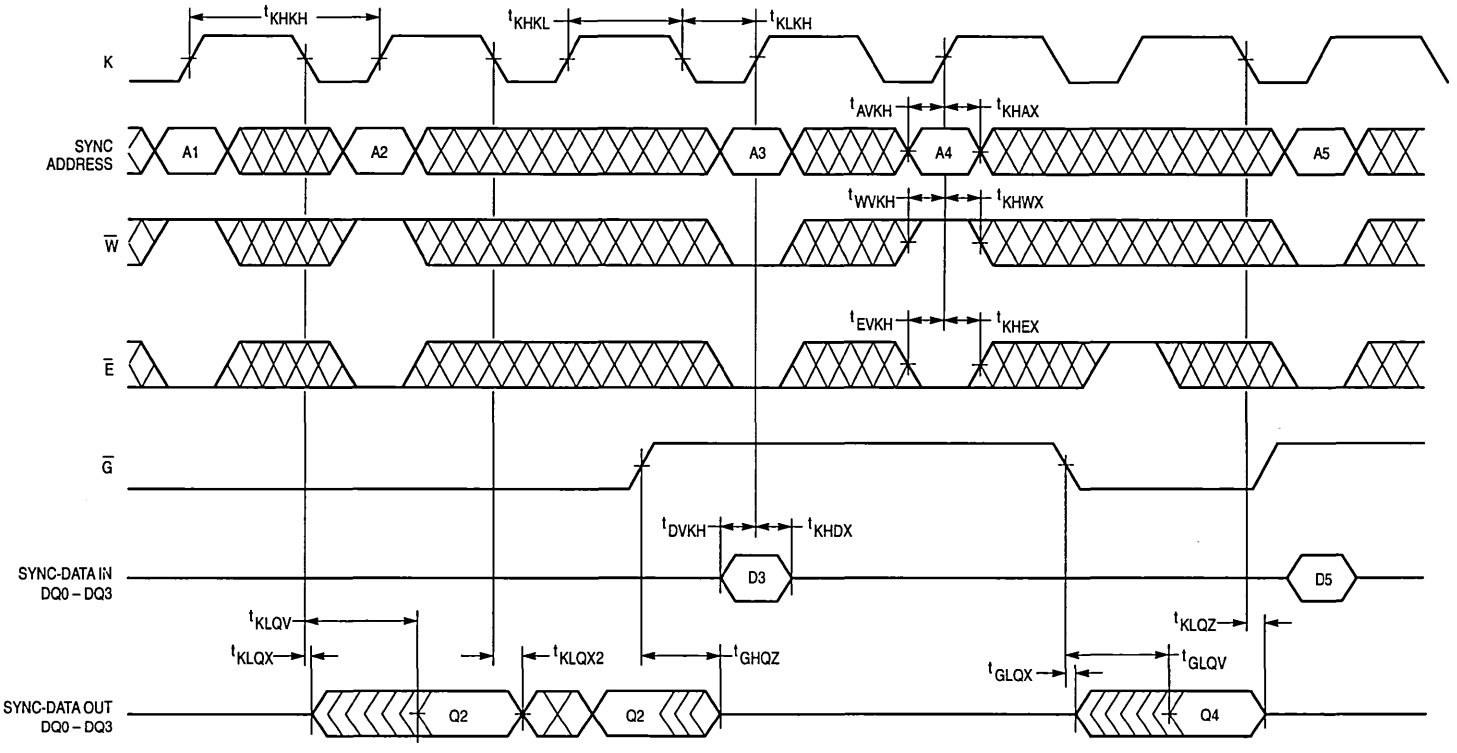


Figure 1B

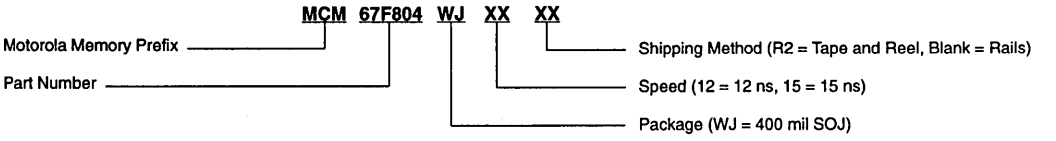
READ AND WRITE CYCLE 1 (See Note 2)



READ AND WRITE CYCLE 2 (See Note 3)



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM67F804WJ12 MCM67F804WJ15
MCM67F804WJ12R2 MCM67F804WJ15R2

4

MCM67P804

Product Preview

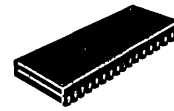
256K x 4 Bit Synchronous Static RAM with Registered Outputs

The Motorola MCM67P804 is a 1,048,576 bit static random access memory organized as 262,144 x 4 bits. This device is fabricated using Motorola's high-performance silicon-gate BiCMOS technology. It features separate TTL input and output buffers, which are fully I/O compatible at 3.3 V, and incorporates input and output registers on board with high speed SRAM.

The synchronous design allows for precise cycle control with the use of an external single clock (K). The addresses (A0 – A17), Data Input (D0 – D3), Data Output (Q0 – Q3), Write Enable ($\overline{W}$), and Chip Enable ($\overline{E}$) are registered in on the rising edge of Clock (K).

The MCM67P804 is available in a 400 mil, 32-lead surface-mount SOJ package.

- Single 5 V ± 10% Power Supply
- Fast Cycle Times: 10/12 ns Max
- Single Clock Operation
- TTL Input and Output Levels (3.3 V I/O Compatible)
- Address, Data Input, $\overline{E}$, $\overline{W}$, Registers on Chip
- 100 MHz Maximum Clock Cycle Time
- Self Timed Write
- High Output Drive Capability: 85 pF/Output at Rated Access Time

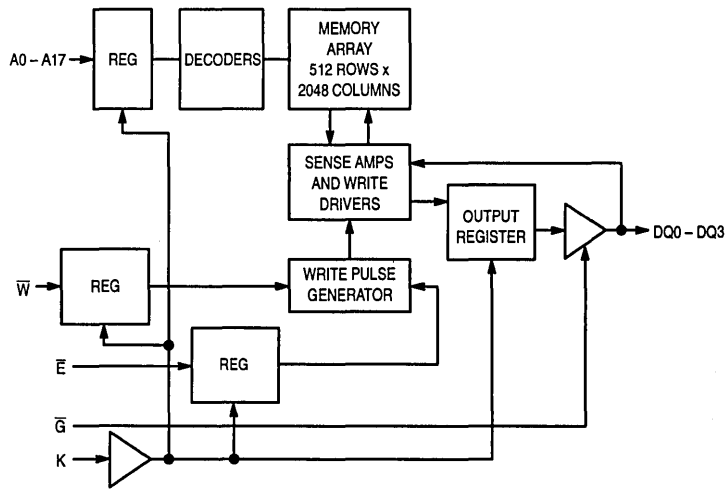


WJ PACKAGE
400 MIL SOJ
CASE 857A

PIN ASSIGNMENT

NC	1	32	A17
A0	2	31	A16
A1	3	30	A15
A2	4	29	A14
A3	5	28	A13
$\overline{E}$	6	27	$\overline{G}$
DQ0	7	26	DQ3
V_{CC}	8	25	V_{SS}
V_{SS}	9	24	V_{CC}
DQ1	10	23	DQ2
$\overline{W}$	11	22	K
A4	12	21	A12
A5	13	20	A11
A6	14	19	A10
A7	15	18	A9
NC	16	17	A8

BLOCK DIAGRAM



PIN NAMES

A0 – A17	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0 – DQ3	Data Input/Output
K	Clock Input
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

4

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE (X = Don't Care)

$\overline{E}$ (t_{n-1})	$\overline{G}$ (t_{n-1})	$\overline{W}$ (t_{n-1})	Mode (t_n)	V_{CC} Current (t_n)	Output (t_n)	Cycle (t_n)
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	Output Disabled	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	MCM67P804-10	MCM67P804-12	Unit
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	180	170	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	40	40	mA
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	20	20	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address and Data Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Output Capacitance	C_{out}	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ/WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol		MCM67P804-10		MCM67P804-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	t_{CYC}	10	—	12	—	ns	1
Clock Low Pulse Width	t_{KLKH}	t_{CL}	4	—	5	—	ns	2
Clock High Pulse Width	t_{KHKL}	t_{CH}	4	—	5	—	ns	
Clock High to Output Active	t_{KHQX1}	t_{DC1}	2	—	2	—	ns	
Clock High to Output Change	t_{KHQX2}	t_{DC2}	2	—	2	—	ns	
Clock High to Q High-Z	t_{KHQZ}	t_{CZ}	—	5	—	6	ns	
Clock Access Time	t_{KHQV}	t_{CD}	—	6	—	7	ns	
Setup Times: A	t_{AVKH}	t_{AS}	2	—	2	—	ns	3
$\overline{W}$	t_{WVKH}	t_{WS}						
$\overline{E}$	t_{EVKH}	t_{ES}						
D	t_{DVKH}	t_{DS}						
Hold Times: A	t_{KHAX}	t_{AH}	1	—	1	—	ns	3
$\overline{W}$	t_{KHWX}	t_{WH}						
$\overline{E}$	t_{KHEX}	t_{EH}						
D	t_{KHDX}	t_{DH}						
Output Enable to Output Valid	t_{GLQV}	t_{OE}	—	5	—	6	ns	
Output Enable to Output Active	t_{GLQX}	t_{LZ}	2	—	2	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	t_{HZ}	—	5	—	6	ns	

NOTES:
1. All read and write cycles are referenced from K.
2. Valid data from Clock High will be the data stored at the address or the last valid read cycle.
3. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.

AC SPEC LOADS

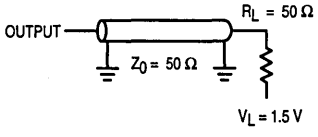


Figure 1A

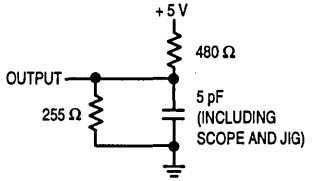
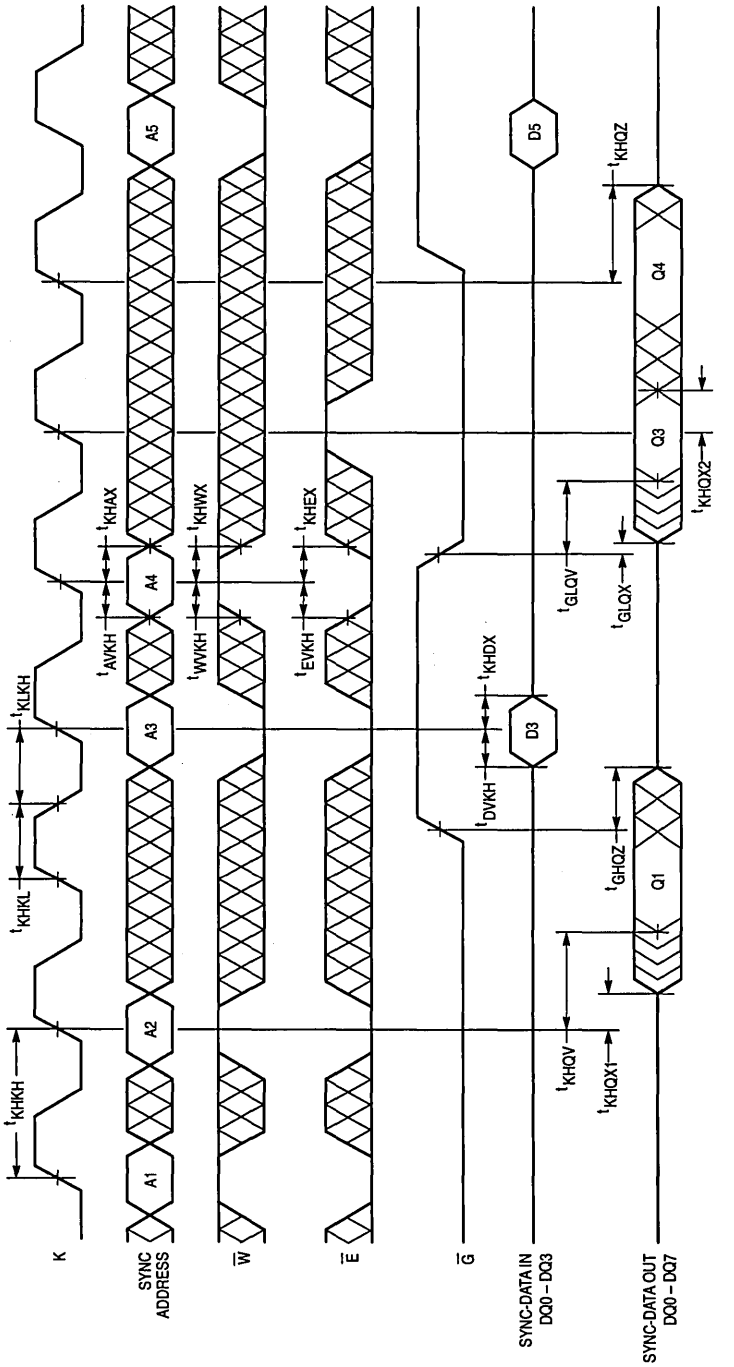
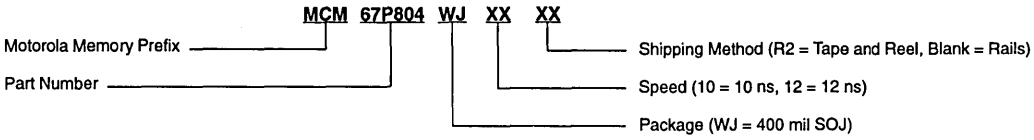


Figure 1B

READ AND WRITE CYCLES



ORDERING INFORMATION
(Order by Full Part Number)



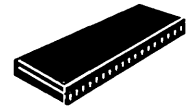
Full Part Numbers — MCM67P804WJ10 MCM67P804WJ12
MCM67P804WJ10R2 MCM67P804WJ12R2

4

MCM67Q804

Product Preview

256K x 4 Bit Separate I/O Synchronous Fast Static RAM



WJ PACKAGE
400 MIL SOJ
CASE 893

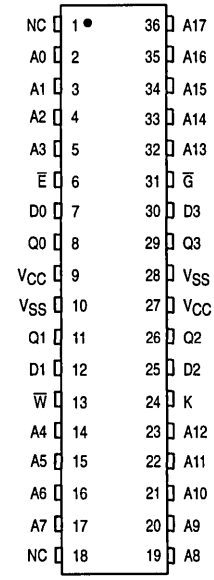
The Motorola MCM67Q804 is a 1,048,576 bit static random access memory, organized as 262,144 x 4 bits. This device is fabricated using Motorola's high-performance silicon-gate BiCMOS technology. It features separate TTL input and output buffers, which are fully I/O compatible at 3.3 V, and incorporates input and output registers on board with high speed SRAM. It also features transparent-write and data pass-through capabilities.

The synchronous design allows for precise cycle control with the use of an external single clock (K). The Addresses (A0 – A17), Data Input (D0 – D3), Data Output (Q0 – Q3), Write-Enable ($\overline{W}$), Chip-Enable ($\overline{E}$), and Output-Enable ($\overline{G}$), are registered in on the rising edge of Clock (K).

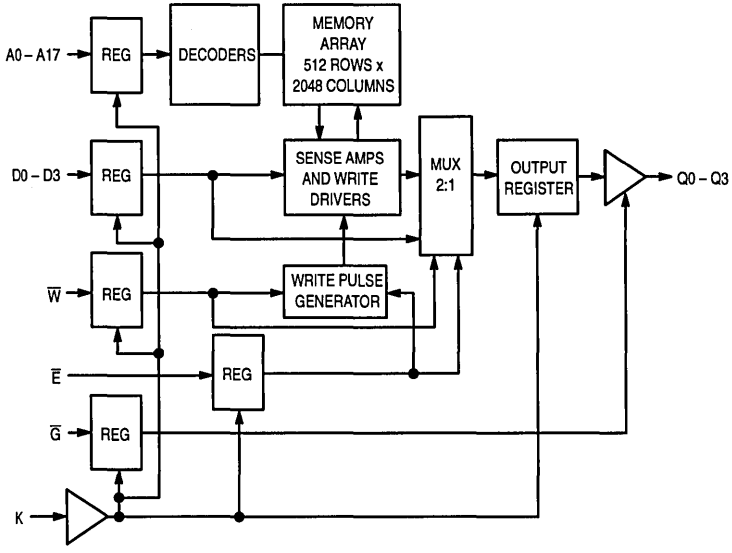
The MCM67Q804 is available in a 400 mil, 36-lead surface-mount SOJ package.

- Single 5 V ± 10% Power Supply
- Fast Cycle Times: 10/12 ns Max
- Single Clock Operation
- TTL Input and Output Levels (3.3 V I/O Compatible)
- Address, Data Input, $\overline{E}$, $\overline{W}$, $\overline{G}$, Registers on Chip
- 100 MHz Maximum Clock Cycle Time
- Self Timed Write
- Separate Data Input and Output Pins
- Transparent-Write or Data Pass-Through
- High Output Drive Capability: 50 pF/Output at Rated Access Time

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A17	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0 – D3	Data Inputs
Q0 – Q3	Data Outputs
K	Clock Input
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{E}$ (t_n)	$\overline{W}$ (t_n)	$\overline{G}$ (t_{n+1})	Mode	D0 – D3	Q0 – Q3 (t_{n+1})	V_{CC} Current
L	L	L	Write and Pass Thru	Valid	D0 – D3 (t_n)	I_{CC}
		H	Write	Valid	High-Z	I_{CC}
H	L	L	Pass Thru	Valid	D0 – D3 (t_n)	I_{CC}
		H	NOP	Don't Care	High-Z	I_{CC}
X	H	L	Read	Don't Care	Q_{out} (t_n)	I_{CC}
		H	Read	Don't Care	High-Z	I_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This is a synchronous device. All synchronous inputs must meet specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) whie the device is selected.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	3.3	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
**V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	MCM67Q804-10	MCM67Q804-12	Unit
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	180	170	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address and Data Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Output Capacitance	C_{out}	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

WRITE CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol		MCM67Q804-10		MCM67Q804-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	t_{CYC}	10	—	12	—	ns	1
Clock Access Time	t_{KHQV}	t_{CD}	—	5	—	6	ns	2
Clock Low Pulse Width	t_{KLKH}	t_{CL}	4	—	4	—	ns	
Clock High Pulse Width	t_{KHKL}	t_{CH}	4	—	4	—	ns	
Clock High to Data Output Invalid	t_{KHQX}	t_{DC1}	2	—	2	—	ns	
Clock High to Data Output High-Z	t_{KHQZ}	t_{CZ}	—	5	—	6	ns	
Setup Times: A	t_{AVKH}	t_{AS}	2	—	2	—	ns	3
$\overline{W}$	t_{WVKH}	t_{WS}						
$\overline{E}$	t_{EVKH}	t_{ES}						
$\overline{G}$	t_{GVKH}	t_{GS}						
D0 – D3	t_{DVKH}	t_{DS}						
Hold Times: A	t_{KHAX}	t_{AH}	1	—	1	—	ns	3
$\overline{W}$	t_{KHWX}	t_{WH}						
$\overline{E}$	t_{KHEX}	t_{EH}						
$\overline{G}$	t_{KHGX}	t_{GH}						
D0 – D3	t_{KHDX}	t_{DH}						

NOTES:
1. All read and write cycles are referenced from K.
2. Valid data from Clock High will be the data stored at the address or the last valid read cycle.
3. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times with stable logic levels for ***ALL*** rising edges of clock (K) while the device is selected.

AC SPEC LOADS

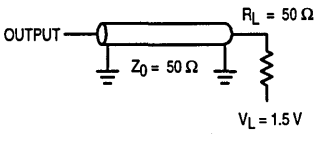


Figure 1A

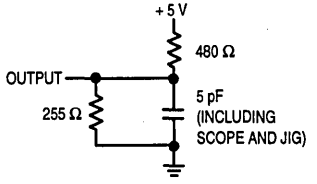
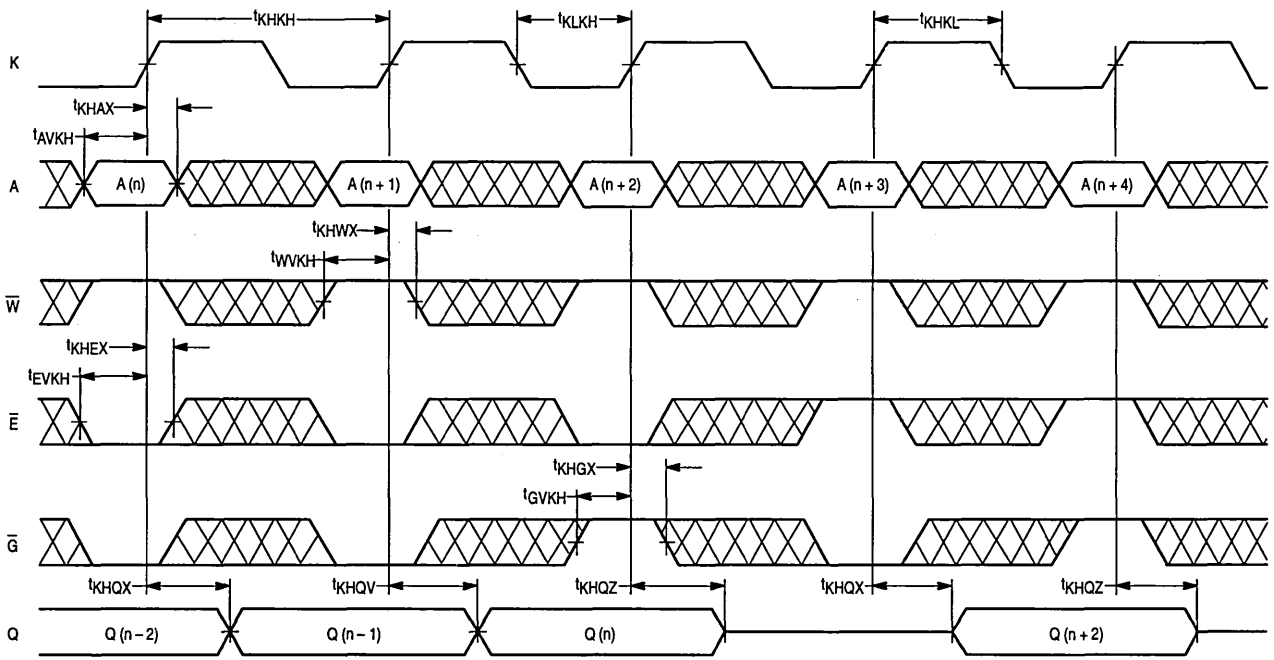


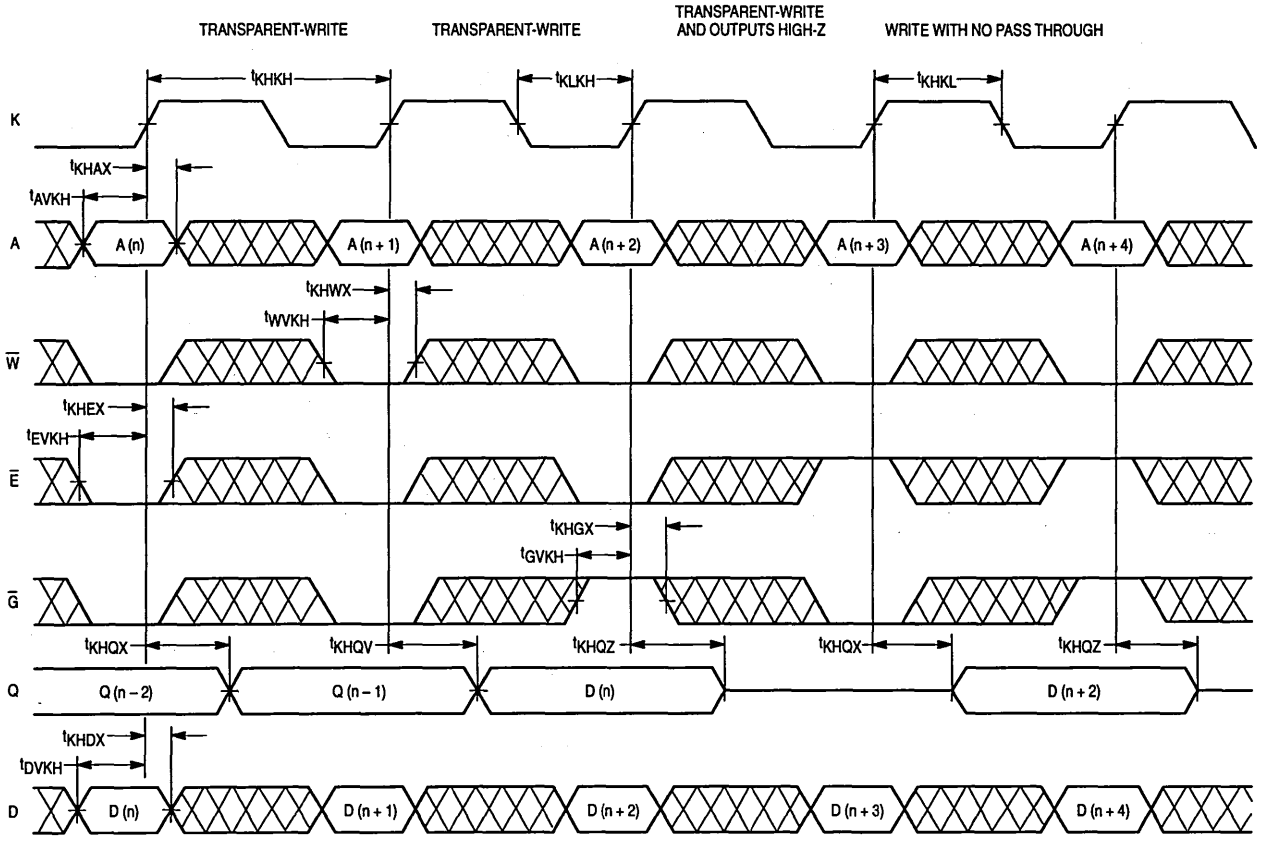
Figure 1B

READ CYCLE TIMING

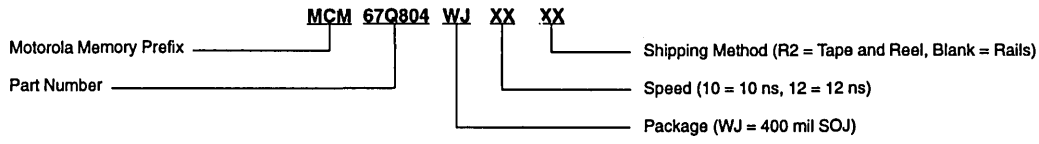


4

WRITE AND DATA PASS-THROUGH CYCLE TIMING



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM67Q804WJ10 MCM67Q804WJ12
MCM67Q804WJ10R2 MCM67Q804WJ12R2

4

Fast Static RAM Modules

5

Standard Modules

Processor Specific Cache Modules

MCM32A32
MCM32A64

128KB and 256KB Secondary Cache Fast Static RAM Modules

With Tag for 486 Processor Based Systems

The MCM32A32 and MCM32A64 are two products in Motorola's asynchronous secondary cache module family for the 486 processor. The modules are configured with 32-bit data, 8-bit tag, and an altered bit for cache writeback. The family supports all cache sizes of the 486 processor. They are offered in 33 and 50 MHz versions:

The 32A32 is a 128KB single bank cache of 32K x 32. The tag is an 8K x 8, and the altered bit is 8K x 1.

The 32A64 is a 256KB double bank cache of 64K x 32. The tag is 16K x 8 and the altered bit is 16K x 1.

The cache family is designed to interface with popular 486 chipsets with on-board cache controllers.

Cache upgrades are seamless, eliminating the need for motherboard jumpers. PD0, 1, 2 are reserved for density identification:

MCM32A32: PD0 = gnd, PD1 = gnd, PD2 = open
MCM32A64: PD0 = open, PD1 = open, PD2 = gnd

5

- 64 Position Dual Readout SIMM for Circuit Density
- Single 5 V ± 10% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Access Times/Cycle Times: 15 ns/50 MHz, 20 ns/33 MHz
- Cache Byte Write, Byte Chip Enable, Bank Output Enable
- Tag Write Enable, Altered Write Enable, Tag/Altered Chip Enable
- Decoupling Capacitors Are Used For Each Fast Static RAM
- High Quality Multi-Layer FR4 PWB With Separate Power and Ground Plane

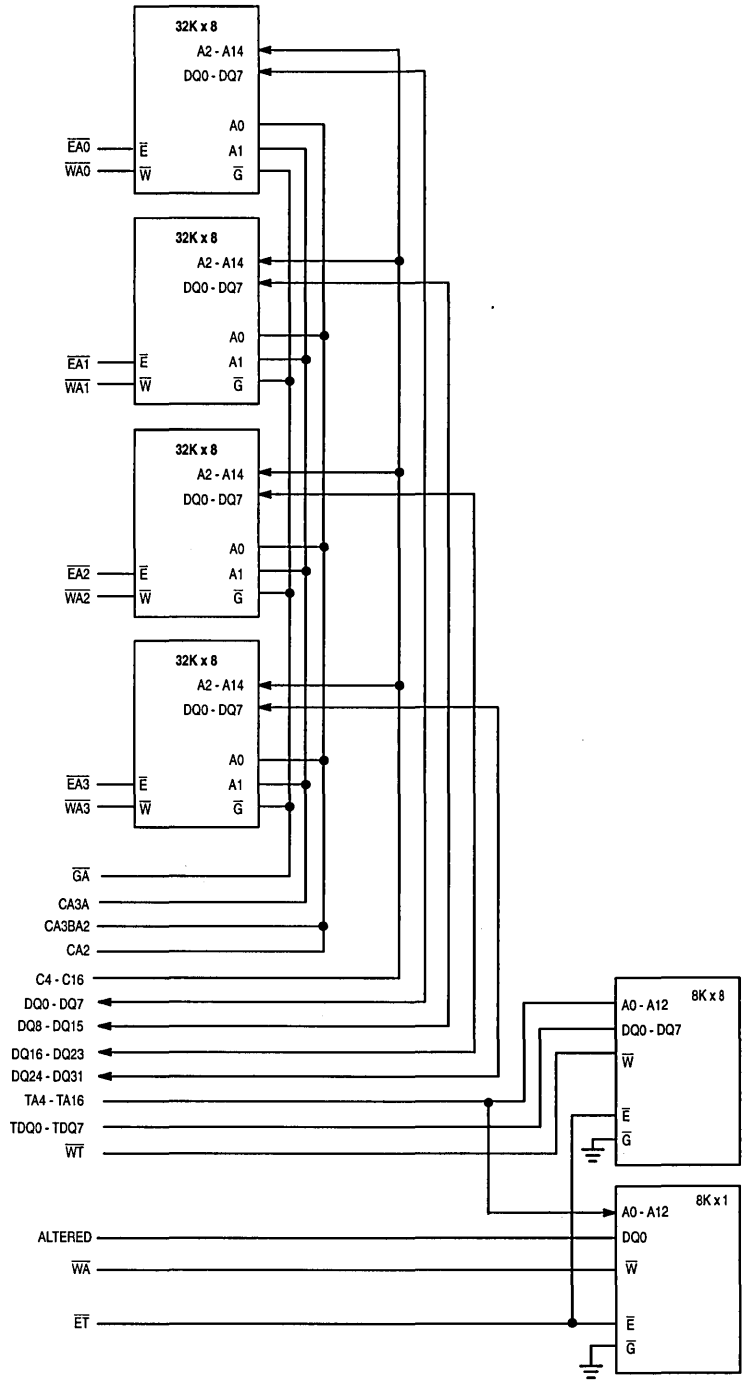
PIN ASSIGNMENT
64 POSITION DUAL READOUT
128 PIN SIMM
TOP VIEW

PD0	1	65	PD1
PD2	2	66	V_{SS}
DQ0	3	67	DQ1
DQ2	4	68	DQ3
DQ4	5	69	V_{CC}
DQ6	6	70	DQ5
DQ8	7	71	DQ7
V_{SS}	8	72	DQ9
DQ10	9	73	DQ11
DQ12	10	74	DQ13
DQ14	11	75	DQ15
DQ16	12	76	DQ17
DQ18	13	77	DQ19
DQ20	14	78	DQ21
V_{SS}	15	79	V_{SS}
DQ22	16	80	DQ23
DQ24	17	81	DQ25
V_{CC}	18	82	V_{CC}
DQ26	19	83	DQ27
DQ28	20	84	DQ29
DQ30	21	85	DQ31
NC	22	86	NC
NC	23	87	NC
V_{SS}	24	88	V_{SS}
$\overline{EA0}$	25	89	$\overline{EB0}$
$\overline{EA1}$	26	90	$\overline{EB1}$
$\overline{EA2}$	27	91	V_{CC}
$\overline{EA3}$	28	92	$\overline{EB2}$
V_{SS}	29	93	$\overline{EB3}$
$\overline{GA}$	30	94	$\overline{GB}$
$\overline{WA0}$	31	95	$\overline{WB0}$
$\overline{WA1}$	32	96	$\overline{WB1}$
$\overline{WA2}$	33	97	$\overline{WB2}$
$\overline{WA3}$	34	98	$\overline{WB3}$
$\overline{WT}$	35	99	$\overline{WA}$
$\overline{ET}$	36	100	V_{CC}
NC	37	101	NC
NC	38	102	NC
CA3A	39	103	CA3BA2
CA2	40	104	CA3B
V_{SS}	41	105	V_{SS}
CA4	42	106	CA5
CA6	43	107	CA7
CA8	44	108	CA9
CA10	45	109	CA11
CA12	46	110	CA13
CA14	47	111	CA15
CA16	48	112	CA17
CA18	49	113	CA19
V_{SS}	50	114	V_{SS}
TA4	51	115	TA5
TA6	52	116	TA7
TA8	53	117	TA9
TA10	54	118	TA11
TA12	55	119	TA13
TA14	56	120	TA15
TA16	57	121	TA17
TA18	58	122	TA19
V_{SS}	59	123	V_{SS}
TDQ0	60	124	TDQ1
TDQ2	61	125	TDQ3
TDQ4	62	126	TDQ5
TDQ6	63	127	TDQ7
ALT	64	128	V_{CC}

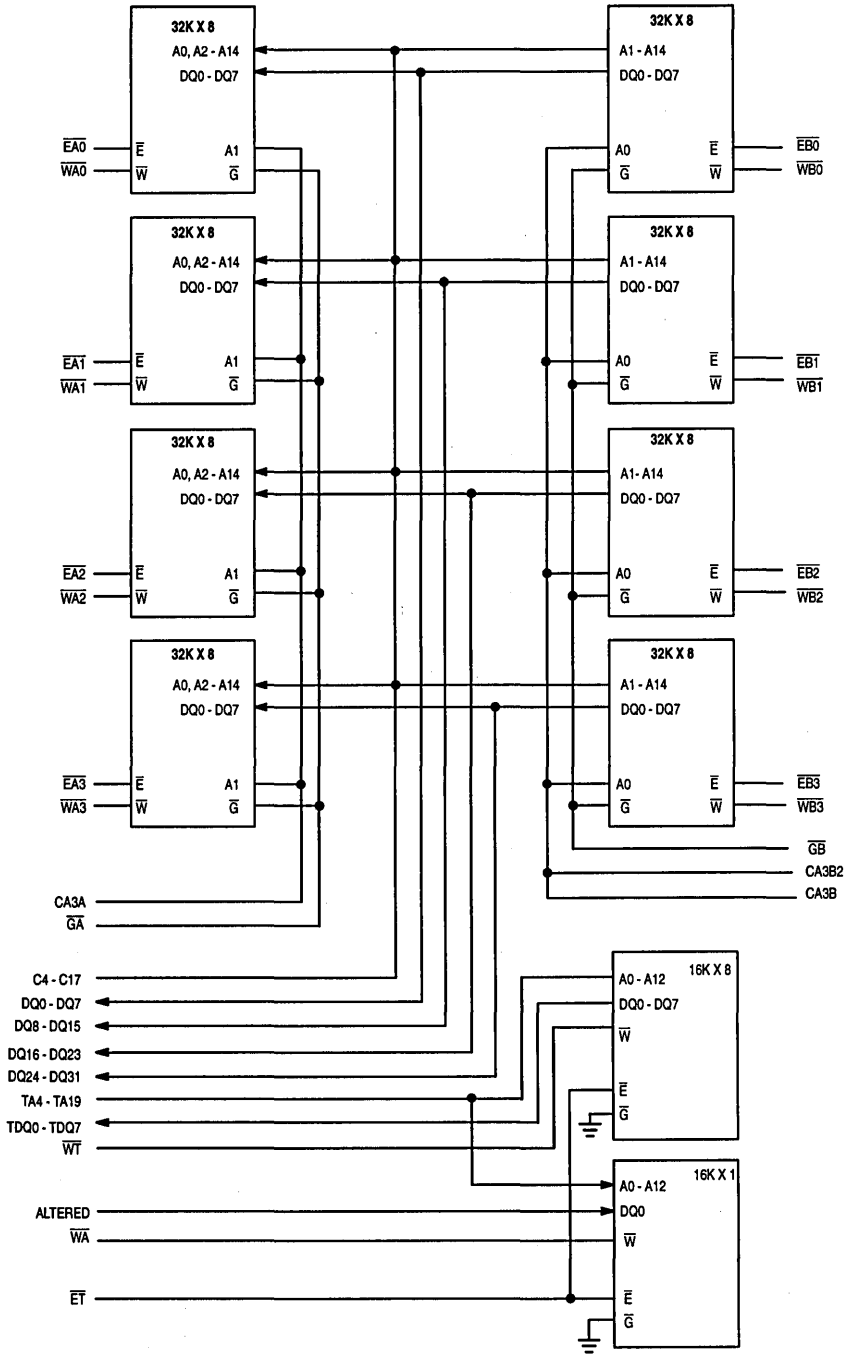
PIN NAMES

CA2 - CA19	Cache Address Inputs
$\overline{WA0}$ - $\overline{WA3}$; $\overline{WB0}$ - $\overline{WB3}$	Byte Write Enable
$\overline{EA0}$ - $\overline{EA3}$; $\overline{EB0}$ - $\overline{EB3}$	Cache Chip Enable
$\overline{GA}$ - $\overline{GB}$	Bank Output Enable
DQ0 - DQ31	Cache Data Input/Output
TA4 - TA19	Tag Address Inputs
$\overline{WT}$	Tag Write Enable
$\overline{WA}$	Altered Write Enable
$\overline{ET}$	Tag/Altered Chip Enable
TDQ0 - TDQ7	Tag Data Input/Output
ALT	Altered Input/Output
PD0 - PD2	Presence Detect
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

128KB BLOCK DIAGRAM



256KB BLOCK DIAGRAM



TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	–
L	H	H	Output Disabled	I_{CCA}	High-Z	–
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	High-Z	Write Cycle

NOTE: $\overline{E}$ = $\overline{Exx}$, $\overline{ET}$; $\overline{W}$ = $\overline{Wxx}$, $\overline{WT}$, $\overline{WA}$; $\overline{G}$ = $\overline{GA}$, $\overline{GB}$

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} For Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 20	mA
Power Dissipation	P_D	11.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns)
** V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 10	µA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 10	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	32A32 33 MHz	32A32 50 MHz	32A64 33 MHz	32A64 50 MHz	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = Max, f = f_{max})	I_{CCA}	840	920	1530	1680	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = Max, f = f_{max})	I_{SB1}	250	280	465	520	mA
CMOS Standby Current (V_{CC} = Max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} – 0.2 V V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} – 0.2 V)	I_{SB2}	110	110	190	190	mA

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, Periodically sampled rather than 100% tested)

Characteristic	Symbol	Max	Unit
Cache Address Input Capacitance	C_{in}	48	pF
Control Pin Input Capacitance ($\overline{E}$, $\overline{W}$)	C_{in}	8	pF
I/O Capacitance	$C_{I/O}$	8	pF
Tag Address Input Capacitance	C_{in}	18	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... Figure 1A Unless Otherwise Noted

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol		33 MHz		50 MHz		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	15	—	20	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	15	—	20	ns	
Tag Access Time	t_{AVTV}		—	12	—	15	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	15	—	20	ns	4
Output Enable Access Time	t_{GLQV}	t_{OE}	—	8	—	10	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	ns	5,6,7
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	ns	5,6,7
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	8	0	9	ns	5,6,7
Output Enable Low to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	ns	5,6,7
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	7	0	8	ns	5,6,7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E}$ = $\overline{Exx}$, $\overline{ET}$; $\overline{W}$ = $\overline{Wxx}$, $\overline{WT}$, $\overline{WA}$; $\overline{G}$ = $\overline{GA}$, $\overline{GB}$
3. All timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} (max) is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
6. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

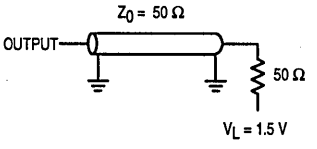


Figure 1A

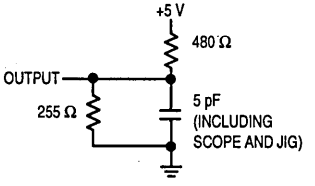
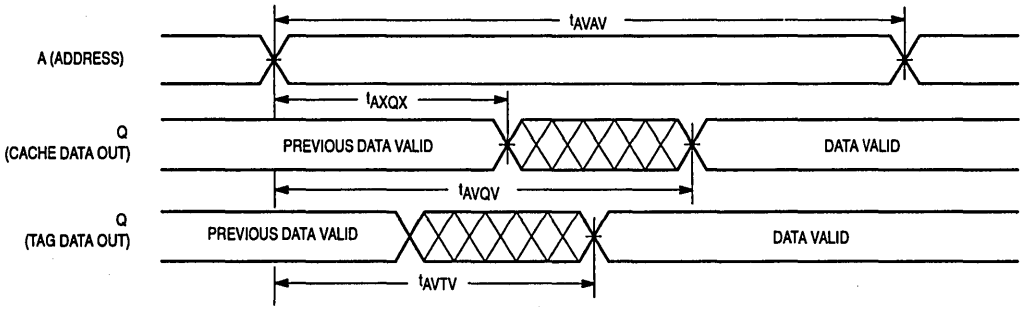


Figure 1B

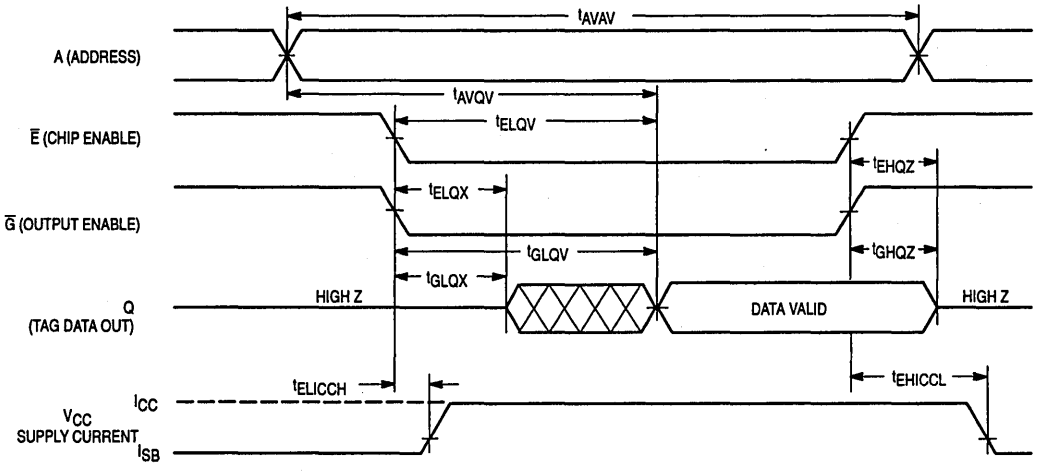
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 3)



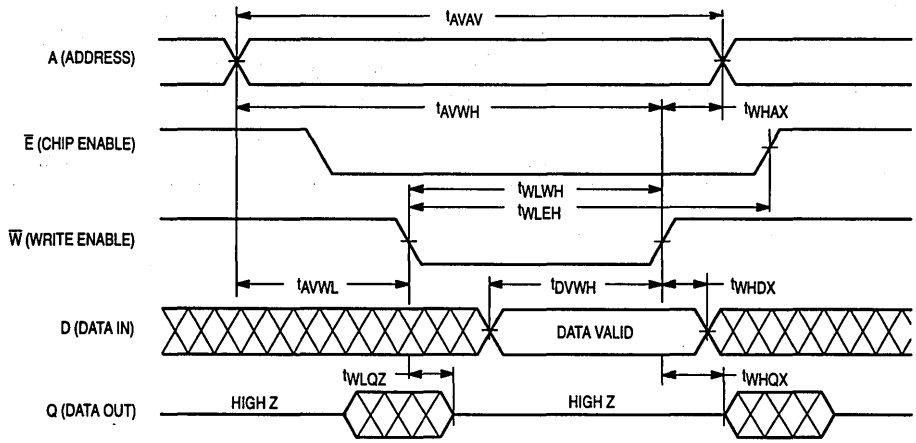
5

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol		50 MHz		33 MHz		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	20	—	ns	4
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	12	—	15	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	10	—	15	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	7	—	8	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	7	0	8	ns	6,7,8
Write High to Output Active	t_{WHQX}	t_{OW}	0	—	0	—	ns	6,7,8
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E} = \overline{Exx}$, $\overline{ET}$; $\overline{W} = \overline{Wxx}$, $\overline{WT}$, $\overline{WA}$; $\overline{G} = \overline{GA}$, $\overline{GB}$
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
4. All timings are referenced from the last valid address to the first transitioning address.
5. If $\overline{G} \geq V_{IH}$, the output will remain in a high impedance state.
6. At any given voltage and temperature, t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
7. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
8. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

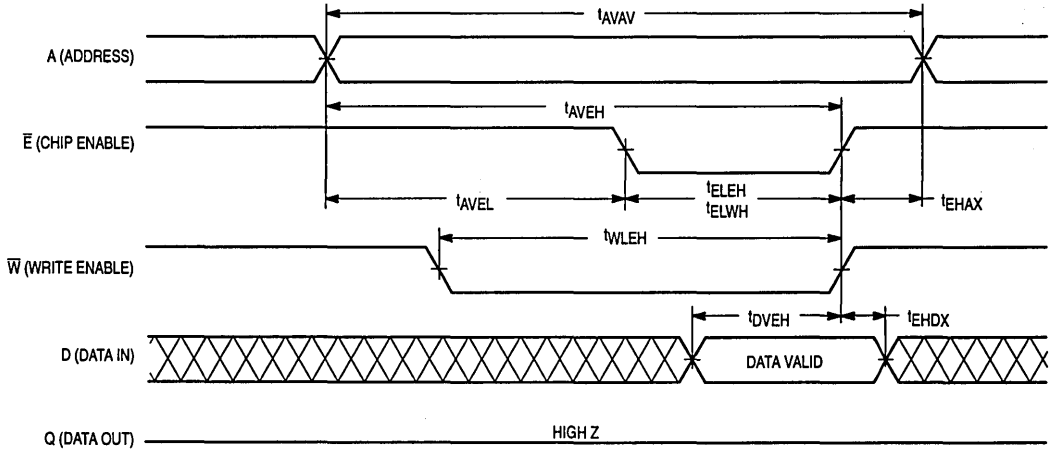


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

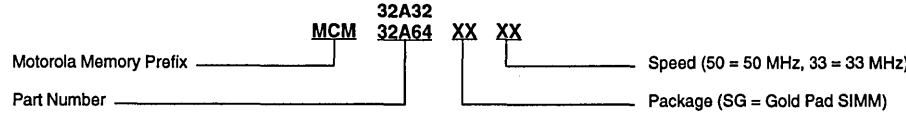
Parameter	Symbol		50 MHz		33 MHz		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	20	—	ns	
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	12	—	15	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	10	—	12	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	t_{DW}	7	—	8	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E}$ = $\overline{Exx}$, $\overline{ET}$; $\overline{W}$ = $\overline{Wxx}$, $\overline{WT}$, $\overline{WA}$; $\overline{G}$ = $\overline{GA}$, $\overline{GB}$
3. All timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance state.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM32A32SG50 MCM32A32SG33
MCM32A64SG50 MCM32A64SG33

MCM32AB32
MCM32AB64
MCM32AB128

Advance Information

128KB/256KB/512KB Secondary Cache Module

With Tag, Valid, and Dirty for 486 Processor Based Systems

The MCM32AB32SG, MCM32AB64SG, and MCM32AB128 are a family of Motorola's asynchronous secondary cache modules for the 486 processor. This family is suited for the Intel 82420 PCI chipset. The modules are configured with 32 bit data, 7 bit tag, valid and a dirty bit for cache writeback. The family supports three cache sizes of the 486 processor.

The MCM32AB32SG is a 128KB single bank cache of 32K x 32. The tag/valid is 8K x 8, and the Dirty bit is 8K x 1.

The MCM32AB64SG is a 256KB double bank cache of 64K x 32. The tag/valid is 16K x 8 and the Dirty bit is 16K x 1.

The MCM32AB128SG is a 512KB single bank cache of 128K x 32. The tag/valid is 32K x 8 and the Dirty bit is 32K x 1.

Cache upgrades are seamless eliminating the need for motherboard jumpers.

The presence detect pins map into the cache configuration register of the Intel 82240 CDC.

- Low Profile Edge Connector: Burndy Part Number: CELP2X56SC3Z48
- Single 5 V ± 10% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Module Cycle Time: Up to External Processor Bus Speed of 33 MHz
- Cache Byte Write, Bank Chip Enable, Bank Output Enable
- Decoupling Capacitors are Used for Each Fast Static RAM
- High Quality Multi-Layer FR4 PWB With Separate Power and Ground Plane

PIN ASSIGNMENT
CACHE MODULE
112 PIN CARDEDGE
TOP VIEW

PD4	PD3	PD2	PD1	PD0	Cache Size	Main Memory Max	Module
NC	NC	NC	NC	NC	—	—	No Module
V_{CC}	V_{CC}	NC	NC	NC	64KB	8MB	—
V_{CC}	V_{CC}	NC	NC	V_{CC}	128KB	16MB	32AB32
V_{CC}	V_{CC}	NC	V_{CC}	NC	256KB	32MB	32AB64
V_{CC}	V_{CC}	NC	V_{CC}	V_{CC}	512KB	64MB	32AB128

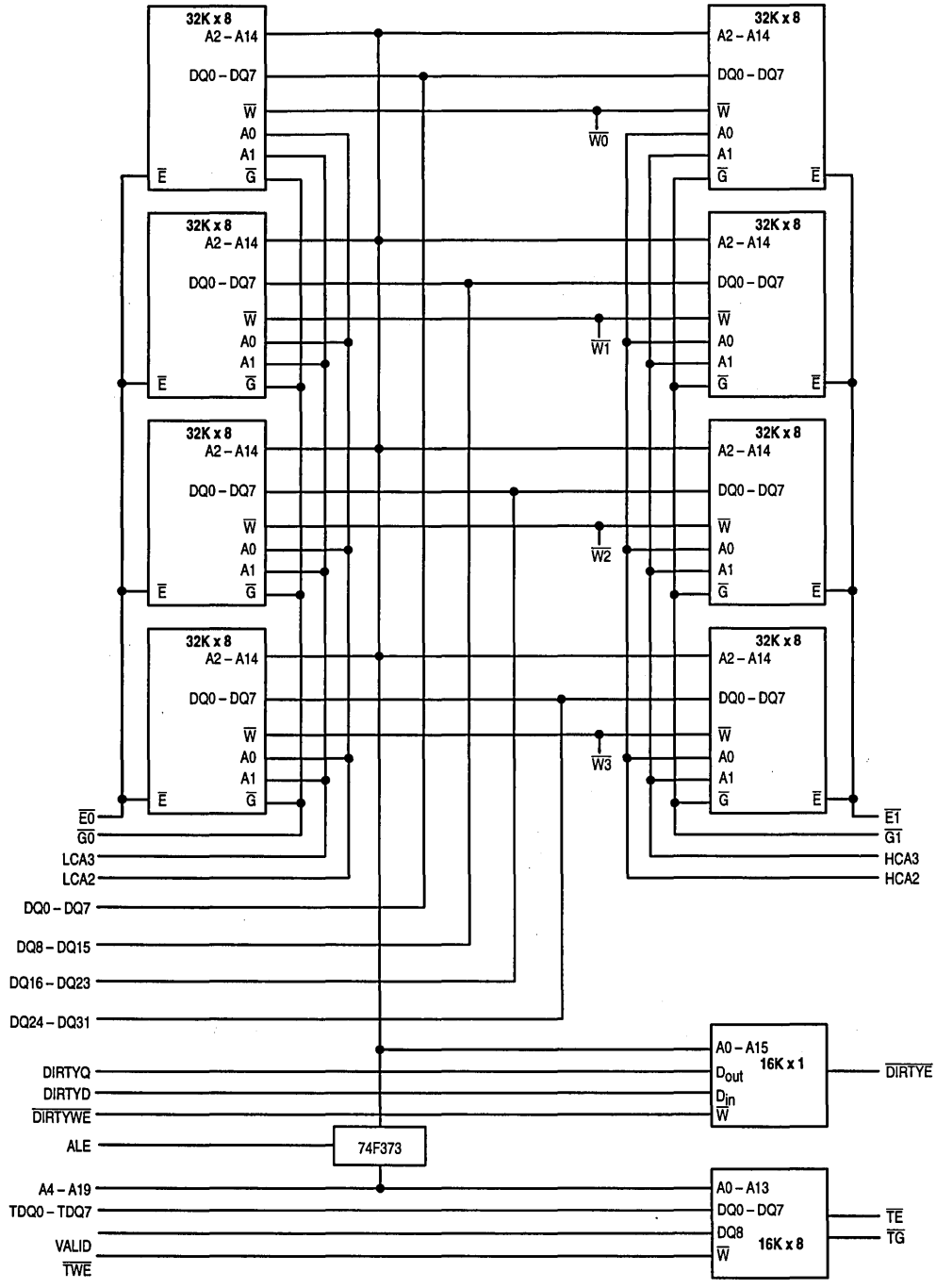
V_{SS}	57	1	V_{SS}
DQ0	58	2	DQ1
DQ2	59	3	DQ3
DQ4	60	4	DQ5
DQ6	61	5	DQ7
V_{CC}	62	6	V_{CC}
NC	63	7	NC
DQ8	64	8	DQ9
DQ10	65	9	DQ11
DQ12	66	10	DQ13
V_{SS}	67	11	V_{SS}
DQ14	68	12	DQ15
DQ16	69	13	DQ17
DQ18	70	14	DQ19
DQ20	71	15	DQ21
V_{CC}	72	16	V_{CC}
DQ22	73	17	DQ23
NC	74	18	NC
DQ24	75	19	DQ25
DQ26	76	20	DQ27
V_{SS}	77	21	V_{SS}
DQ28	78	22	DQ29
DQ30	79	23	DQ31
LA2	80	24	HA2
LA3	81	25	HA3
V_{CC}	82	26	V_{CC}
A4	83	27	A5
A6	84	28	A7
A8	85	29	A9
A10	86	30	A11
A12	87	31	A13
A14	88	32	A15
A16	89	33	A17
A18	90	34	NC
V_{SS}	91	35	V_{SS}
DIRTYD	92	36	DIRTYQ
TDQ0	93	37	TDQ1
TDQ2	94	38	TDQ3
TDQ4	95	39	TDQ5
V_{SS}	96	40	V_{SS}
TDQ6	97	41	NC
VALID	98	42	NC
$\overline{TE}$	99	43	$\overline{ALE}$
$\overline{TWE}$	100	44	WEO
V_{CC}	101	45	V_{CC}
V_{SS}	102	46	V_{SS}
$\overline{TG}$	103	47	$\overline{WE1}$
$\overline{DIRTYWE}$	104	48	$\overline{WE2}$
$\overline{DIRTYE}$	105	49	$\overline{WE3}$
V_{CC}	106	50	V_{CC}
$\overline{G0}$	107	51	$\overline{G1}$
$\overline{E0}$	108	52	$\overline{E1}$
PD0	109	53	PD1
PD2	110	54	PD2
PD4	111	55	NC
V_{SS}	112	56	V_{SS}

PIN NAMES

A4 - A19	Address Inputs
$\overline{HCA2}$, $\overline{HCA3}$	Upper Bank Address Inputs
$\overline{LCA2}$, $\overline{LCA3}$	Lower Bank Address Inputs
$\overline{Wx}$	Byte Write Enable
$\overline{Ex}$	Bank Chip Enable
$\overline{Gx}$	Bank Output Enable
DQ0 - DQ32	Cache Data Input/Output
TDQ0 - TDQ7	Tag Data Input/Output
$\overline{TWE}$	Tag Write Enable
$\overline{TG}$	Tag Output Enable
$\overline{TE}$	Tag Chip Enable
VALID	Valid Bit
$\overline{DIRTYWE}$	Dirty Write Enable
$\overline{DIRTYE}$	Dirty Chip Enable
DIRTYD	Dirty Data Input
DIRTYQ	Dirty Data Output
PD0 - PD4	Presence Detect
V_{CC}	+5 V Power Supply
V_{SS}	Ground

5

486 256KB CACHE MODULE BLOCK DIAGRAM



MCM32128

Advance Information

128K x 32 Bit Fast Static RAM Module

The MCM32128 is a 4M bit static random access memory module organized as 131,072 words of 32 bits. The module is offered in either a 64-lead zig-zag in-line package (ZIP) or a 64-lead single in-line memory module (SIMM). Four MCM6226A fast static RAMs, packaged in 32-lead SOJ packages are mounted on a printed circuit board along with four decoupling capacitors.

The MCM6226A is a high-performance CMOS fast static RAM organized as 131,072 words of 8 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

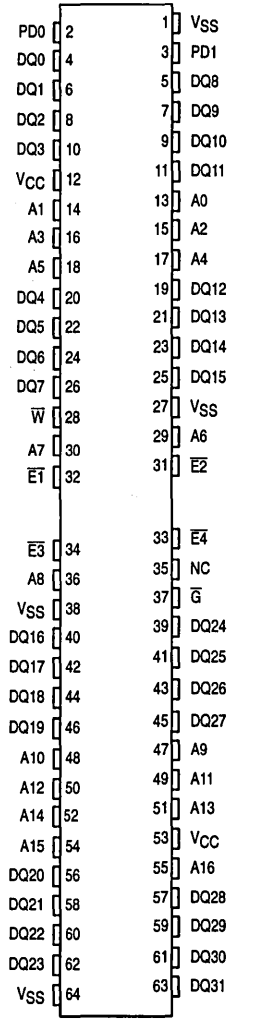
The MCM32128 is equipped with output enable ($\overline{G}$) and four separate byte enable ($\overline{E1}$ – $\overline{E4}$) inputs, allowing for greater system flexibility. The $\overline{G}$ input, when high, will force the outputs to high impedance. $\overline{Ex}$ high will do the same for byte x.

- Single 5 V ± 10% Power Supply
- Fast Access Times: 20/25/35 ns
- Three-State Outputs
- Fully TTL Compatible
- JEDEC Standard Pin Out
- Power Operation: 720/640/600 mA Maximum, Active AC
- High Board Density ZIP or SIMM Package
- Byte Operation: Four Separate Chip Enables, One for Each Byte (Eight Bits)
- High Quality Four-Layer FR4 PWB with Separate Internal Power and Ground Planes
- Incorporates Motorola's State-of-the-Art Fast Static RAMs

PIN NAMES	
A0 – A16	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$ – $\overline{E4}$	Byte Enables
DQ0 – DQ31	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
PD0 – PD1	Package Density

For proper operation of the device, V_{SS} must be connected to ground.

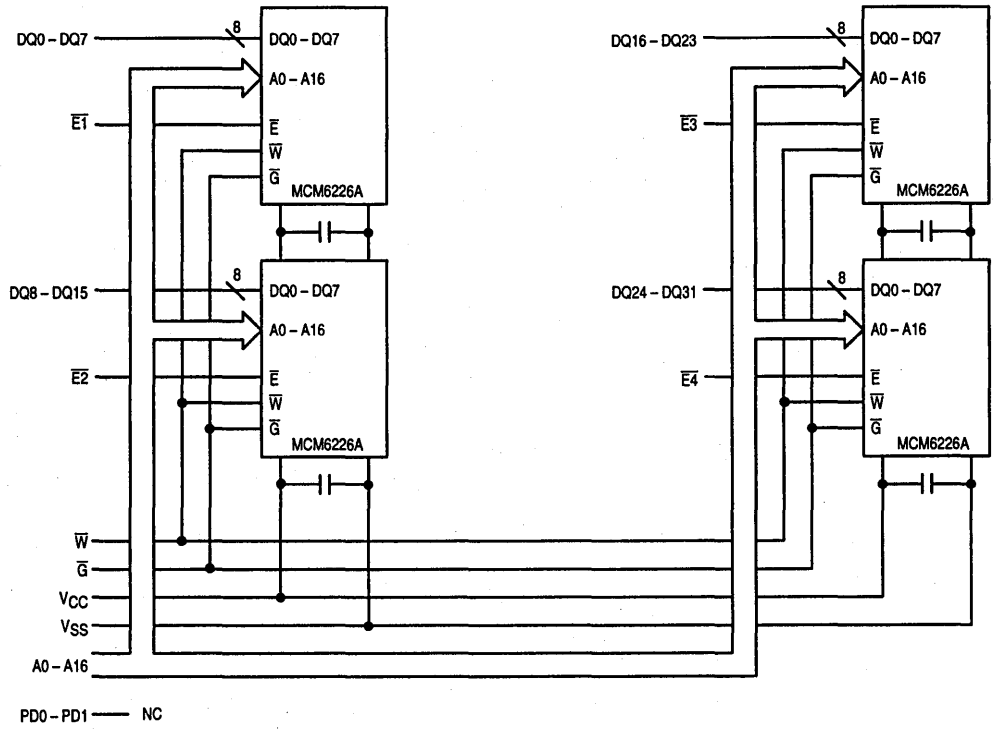
PIN ASSIGNMENT
TOP VIEW
64-LEAD ZIP – CASE 871
64-LEAD SIMM – CASE TBD



This document contains information on a new product. Specifications and information herein are subject to change without notice.

FUNCTIONAL BLOCK DIAGRAM

128K x 32 MEMORY MODULE



TRUTH TABLE

$\overline{Ex}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1} or I_{SB2}	High-Z	—
L	H	H	Read	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Output Power Supply Voltage	V_{CCQ}	– 0.5 to V_{CC}	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	4.4	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperatrue	T_{stg}	– 25 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

The devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

These CMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = V_{CCQ} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)
**V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 4	µA
Output Leakage Current ($\overline{G}$, $\overline{Ex}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	± 4	µA
AC Active Supply Current ($\overline{G}$, $\overline{Ex}$ = V_{IL}, I_{out} = 0 mA, Cycle time ≥ t_{AVAV} min) MCM32128-20: t_{AVAV} = 20 ns MCM32128-25: t_{AVAV} = 25 ns MCM32128-35: t_{AVAV} = 35 ns	I_{CCA}	— — —	600 540 480	720 640 600	mA
AC Standby Current ($\overline{Ex}$ = V_{IH}, Cycle time ≥ t_{AVAV} min)	I_{SB1}	—	28	80	mA
CMOS Standby Current ($\overline{Ex}$ ≥ V_{CC} – 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)	I_{SB2}	—	16	60	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	(All pins except DQ0 – DQ31 and $\overline{E1}$ – $\overline{E4}$) $\overline{E1}$ – $\overline{E4}$	C_{in}	16 10	24 14	pF
Input/Output Capacitance (DQ0 – DQ31)		C_{out}	8	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V

Output Load ..... See Figure 1A Unless Otherwise Noted
Input Rise/Fall Time ..... 3 ns

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		MCM32128-20		MCM32128-25		MCM32128-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	—	25	—	35	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	20	—	25	—	35	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	10	—	12	—	15	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	5	—	5	—	5	—	ns	4,5,6
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	9	0	10	0	12	ns	4,5,6
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	9	0	10	0	12	ns	4,5,6
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GHQX} min, both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).

AC TEST LOADS

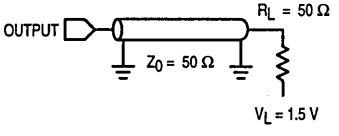


Figure 1A

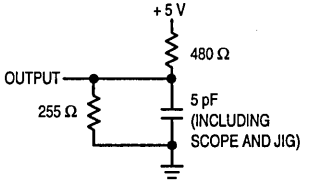
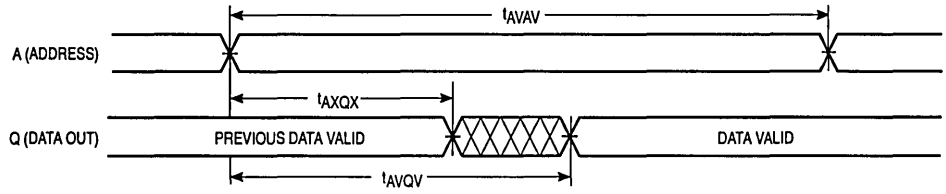


Figure 1B

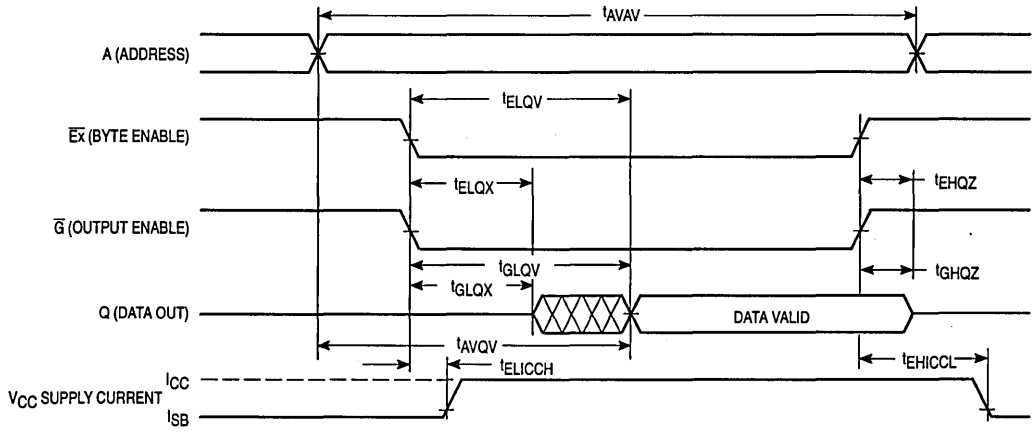
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7 Above)



READ CYCLE 2 (See Note)



NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

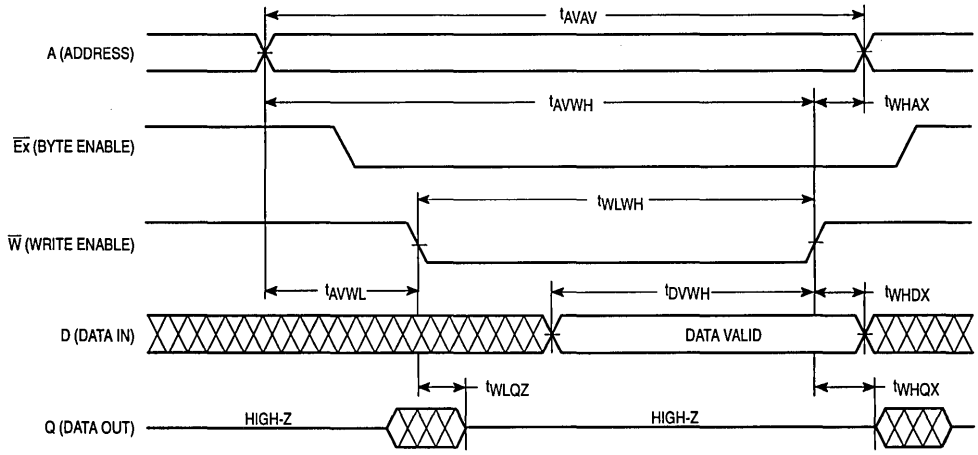
5

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM32128-20		MCM32128-25		MCM32128-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	9	0	10	0	15	ns	4,5,6
Write High to Output Active	t_{WHQX}	t_{OW}	5	—	5	—	5	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

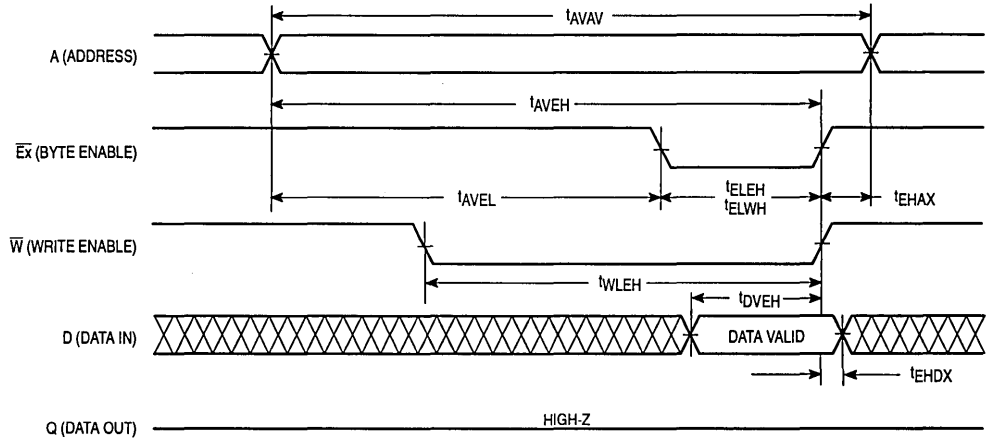


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

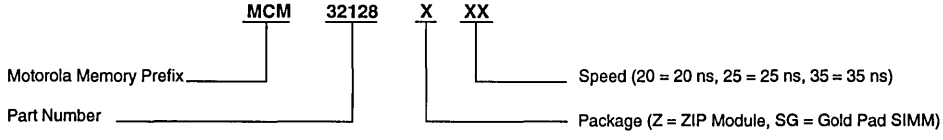
Parameter	Symbol		MCM32128-20		MCM32128-25		MCM32128-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	—	17	—	20	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	15	—	17	—	20	—	ns	4,5
Enable to End of Write	t_{ELWH}	t_{CW}	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	—	10	—	15	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM32128Z20 MCM32128Z25 MCM32128Z35
MCM32128SG20 MCM32128SG25 MCM32128SG35

MCM32257

256K x 32 Bit Fast Static RAM Module

The MCM32257 is an 8M bit static random access memory module organized as 262,144 words of 32 bits. The module is a 64-lead zig-zag in-line package (ZIP) or 64-lead single in-line memory module (SIMM) consisting of eight MCM6229A fast static RAMs packaged in 28-lead SOJ packages and mounted on a printed circuit board along with eight decoupling capacitors.

The MCM6229A is a high-performance CMOS fast static RAM organized as 262,144 words of 4 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM32257 is equipped with output enable ($\overline{G}$) and four separate byte enable ($\overline{E1}$ – $\overline{E4}$) inputs, allowing for greater system flexibility. The $\overline{G}$ input, when high, will force the outputs to high impedance. $\overline{Ex}$ high will do the same for byte x.

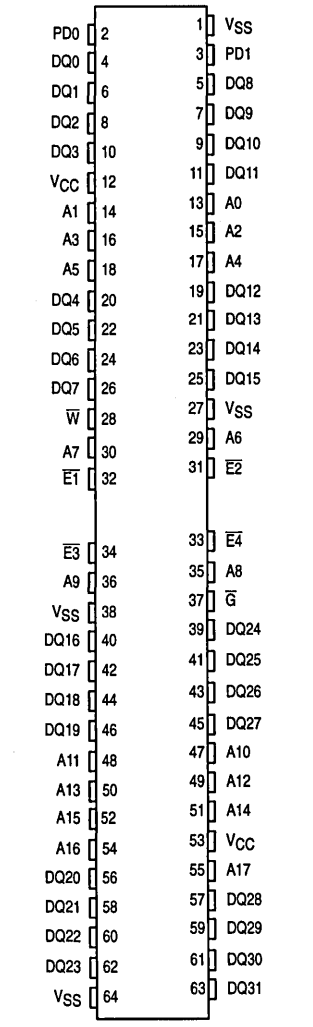
PD0 and PD1 are reserved for density identification. PD0 and PD1 are connected to ground. These pins can be used to identify the density of the memory module.

- Single 5 V ± 10% Power Supply
- Fast Access Time: 20/25/35 ns
- Three-State Outputs
- Fully TTL Compatible
- JEDEC Standard Pin Out
- Power Operation: 1360/1200/1120 mA Maximum, Active AC
- High Board Density ZIP Package
- Byte Operation: Four Separate Chip Enables, One for Each Byte (Eight Bits)
- High Quality Four-Layer FR4 PWB with Separate Internal Power and Ground Planes
- Incorporates Motorola's State-of-the-Art Fast Static RAMs

PIN NAMES	
A0 – A17	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$ – $\overline{E4}$	Byte Enables
DQ0 – DQ31	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
PD0 – PD1	Package Density

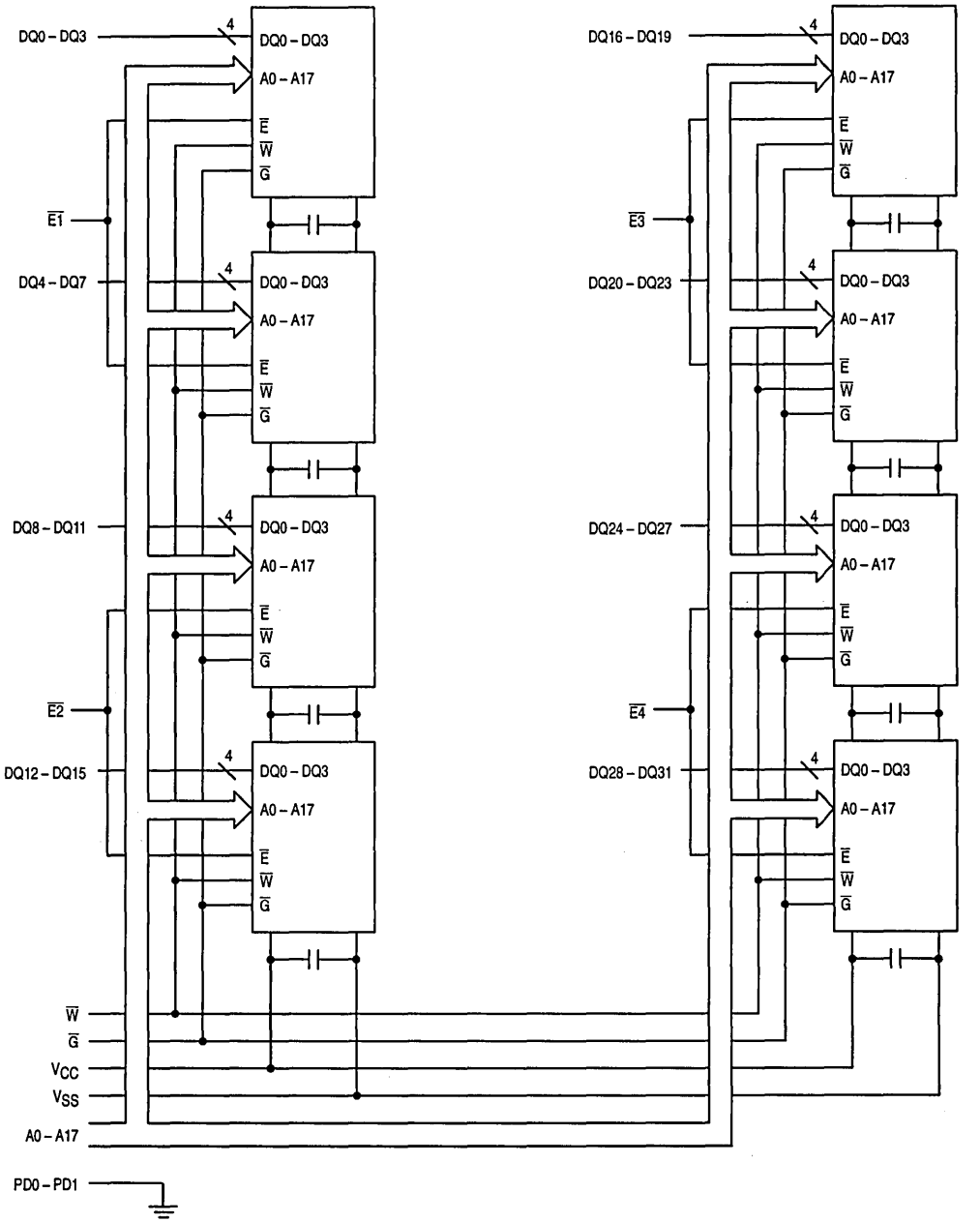
For proper operation of the device, V_{SS} must be connected to ground.

PIN ASSIGNMENT
TOP VIEW
64 LEAD ZIP — CASE 871
64 LEAD SIMM — CASE TBD



FUNCTIONAL BLOCK DIAGRAM

256K x 32 MEMORY MODULE



TRUTH TABLE

$\overline{Ex}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1} or I_{SB2}	High-Z	—
L	H	H	Read	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Output Power Supply Voltage	V_{CCQ}	– 0.5 to V_{CC}	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation)	P_D	8.8	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperatrue	T_{stg}	– 25 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

The devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

These CMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = V_{CCQ} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)
**V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	—	± 8	µA
Output Leakage Current ($\overline{G}$, $\overline{Ex}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	—	± 8	µA
AC Active Supply Current ($\overline{G}$, $\overline{Ex}$ = V_{IL}, I_{out} = 0 mA, Cycle time ≥ t_{AVAV} min)	MCM32257-20: t_{AVAV} = 20 ns	I_{CCA}	—	1120	1360	mA
	MCM32257-25: t_{AVAV} = 25 ns		—	960	1200	
	MCM32257-35: t_{AVAV} = 35 ns		—	880	1120	
AC Standby Current ($\overline{Ex}$ = V_{IH}, Cycle time ≥ t_{AVAV} min)		I_{SB1}	—	56	160	mA
CMOS Standby Current ($\overline{Ex}$ ≥ V_{CC} – 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)		I_{SB2}	—	32	120	mA
Output Low Voltage (I_{OL} = + 8.0 mA)		V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)		V_{OH}	2.4	—	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	(All pins except DQ0 – DQ31 and $\overline{E1}$ – $\overline{E4}$)	C_{in}	32	48	pF
	$\overline{E1}$ – $\overline{E4}$		10	14	
Input/Output Capacitance (DQ0 – DQ31)		C_{out}	8	9	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Output Timing Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V

Output Load ..... See Figure 1A Unless Otherwise Noted
Input Rise/Fall Time ..... 3 ns

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		MCM32257-20		MCM32257-25		MCM32257-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	20	—	25	—	35	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	20	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	20	—	25	—	35	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	10	—	12	—	15	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	5	—	5	—	5	—	ns	4,5,6
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	9	0	10	0	12	ns	4,5,6
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	9	0	10	0	12	ns	4,5,6
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	20	—	25	—	35	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GHQX} min, both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).

5

AC TEST LOADS

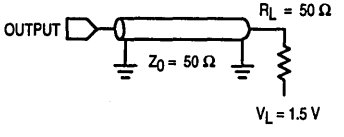


Figure 1A

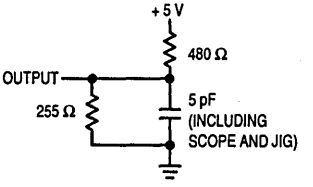
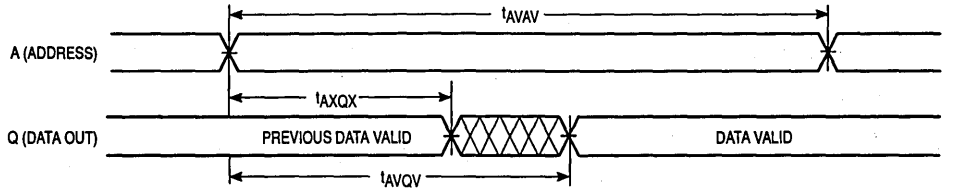


Figure 1B

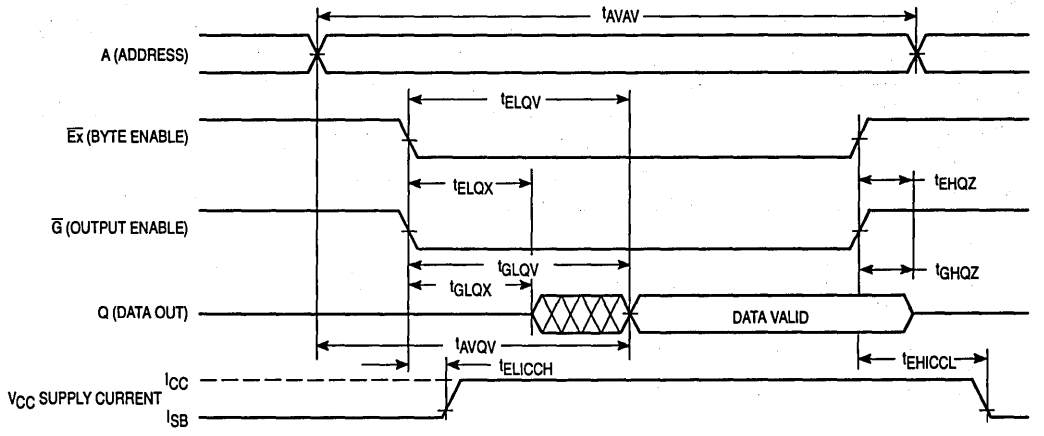
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7 Above)



READ CYCLE 2 (See Note)



NOTE: Addresses valid prior to or coincident with $\overline{E}$ going low.

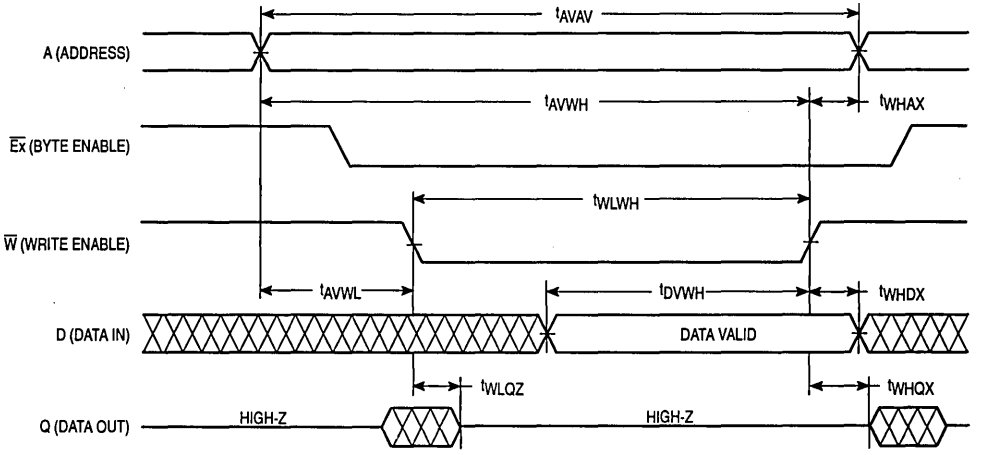
5

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM32257-20		MCM32257-25		MCM32257-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	9	0	10	0	15	ns	4,5,6
Write High to Output Active	t_{WHQX}	t_{OW}	5	—	5	—	5	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1



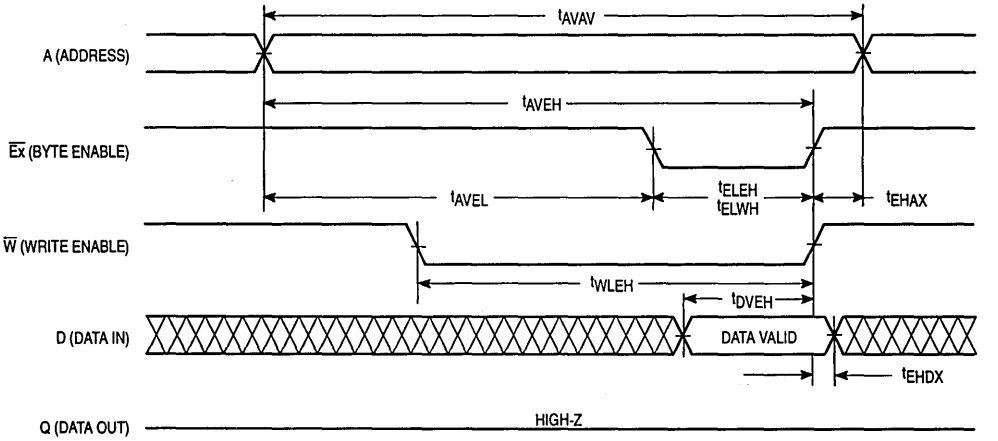
5

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

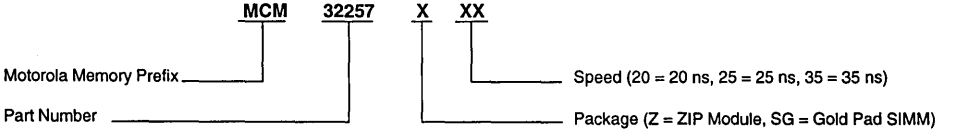
Parameter	Symbol		MCM32257-20		MCM32257-25		MCM32257-35		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	20	—	25	—	35	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	15	—	17	—	20	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	15	—	17	—	20	—	ns	4,5
Enable to End of Write	t_{ELWH}	t_{CW}	15	—	17	—	20	—	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	15	—	17	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	—	10	—	15	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications, any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM32257Z20 MCM32257Z25 MCM32257Z35
MCM32257SG20 MCM32257SG25 MCM32257SG35

MCM3264A

64K x 32 Bit Static Random Access Memory Module

The MCM3264A is a 2M bit static random access memory module organized as 65,536 words of 32 bits. The module is a 64-lead zig-zag in-line module consisting of eight MCM6209C fast static RAMs packaged in a 28 J-lead small outline package (SOJ) and mounted on a printed circuit board along with a decoupling capacitor for each FSRAM.

The MCM6209C is a high-performance CMOS fast static RAM organized as 65,536 words of 4 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM3264A is equipped with output enable ($\overline{G}$) and four separate byte enable ($\overline{E1}$-$\overline{E4}$) inputs, allowing for greater system flexibility. The $\overline{G}$ input, when high, will force the outputs to high impedance. $\overline{Ex}$ high will do the same for byte x.

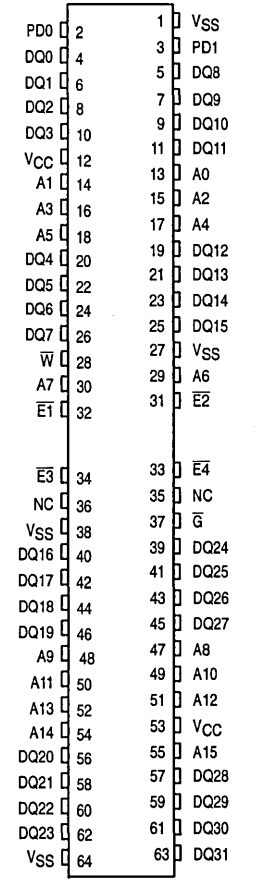
PD0 and PD1 are reserved for density expansion. PD0 is open and PD1 is connected to ground internally on the module. These pins can be used to identify the density of the memory module.

- Single 5 V ± 10% Power Supply
- Fast Access Time: 15/20 ns
- Equal Address and Chip Enable Access Time
- Three State Outputs
- Full TTL Compatible
- JEDEC Standard Compatible
- Power Operation: 1240/1160 mA Maximum, Active AC
- High Board Density ZIP Module
- Byte Operation: Four Separate Chip Enables, One for Each Byte (Eight Bits)
- High Quality Four Layer FR4 PWB with Separate Internal Power and Ground Plane
- Incorporates Motorola's State-of-the-Art Fast Static RAMs

PIN NAMES	
A0 – A15	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E1}$ – $\overline{E4}$	Byte Enables
DQ0 – DQ31	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
PD0 – PD1	Package Density
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

PIN ASSIGNMENT
64-LEAD ZIG-ZAG IN-LINE MODULE
TOP VIEW – 871A



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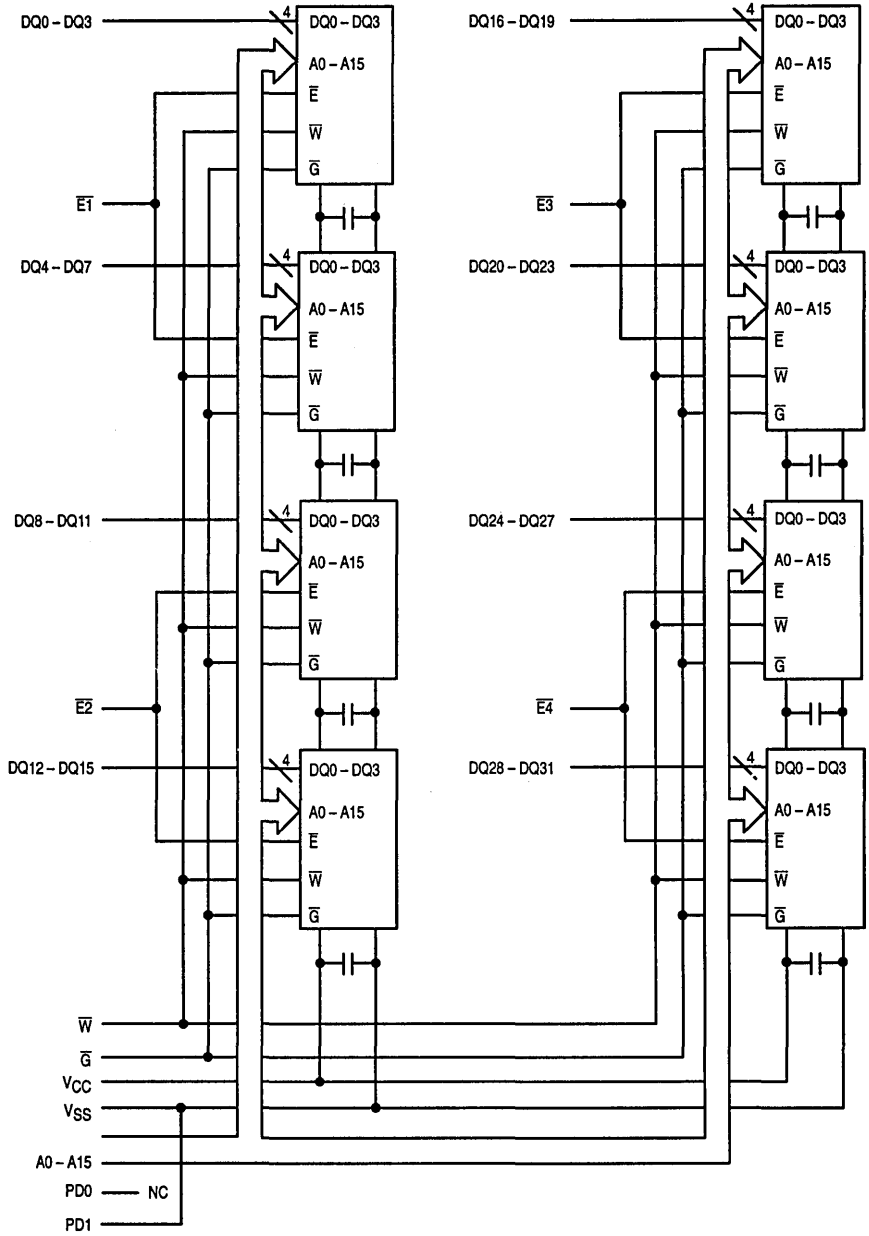
FUNCTIONAL BLOCK DIAGRAM



*NC = No Connection

MCM3264A TRUTH TABLE

$\overline{Ex}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	H	Read	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	8	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 25 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

The devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

These CMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH}(max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)
**V_{IL}(min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(i)}$	—	—	± 8	µA
Output Leakage Current ($\overline{G}$, $\overline{Ex}$ = V_{IH}, V_{out} = 0 to V_{CCQ})	$I_{lkg(O)}$	—	—	± 8	µA
AC Active Supply Current (I_{out} = 0 mA, Cycles Times ≥ t_{AVAV} min) MCM3264A-15: t_{AVAV} = 15 ns MCM3264A-20: t_{AVAV} = 20 ns	I_{CCA}	 — —	 840 760	 1240 1160	mA
AC Standby Current ($\overline{Ex}$ = V_{IH}, Cycle Times ≥ t_{AVAV} min) MCM3264A-15: t_{AVAV} = 15 ns MCM3264A-20: t_{AVAV} = 20 ns	I_{SB1}	 — —	 300 260	 400 360	mA
CMOS Standby Current (f = 0 MHz, $\overline{Ex}$ ≥ V_{CC} – 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)	I_{SB2}	—	32	160	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	All Pins Except DQ0 – DQ31 and $\overline{E1}$ – $\overline{E4}$ $\overline{E1}$ – $\overline{E4}$	C_{in}	32 10	48 14	pF
Input/Output Capacitance (DQ0 – DQ31)		$C_{I/O}$	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 5 ns

Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		MCM3264A-15		MCM3264A-20		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	15	—	20	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	15	—	20	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	15	—	20	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	8	—	10	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	4	—	ns	4, 5, 6
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	ns	4, 5, 6
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	8	0	9	ns	4, 5, 6
Output Enable High to Output High Z	t_{GHQZ}	t_{OHZ}	0	7	0	8	ns	4, 5, 6
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	15	—	20	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications; any combination of $\overline{Ex}$s may be asserted.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GHQX} min, both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.

AC TEST LOADS

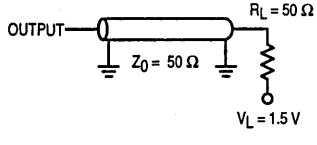


Figure 1A

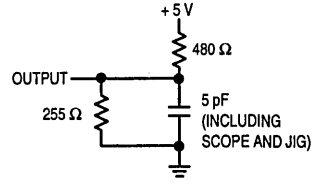
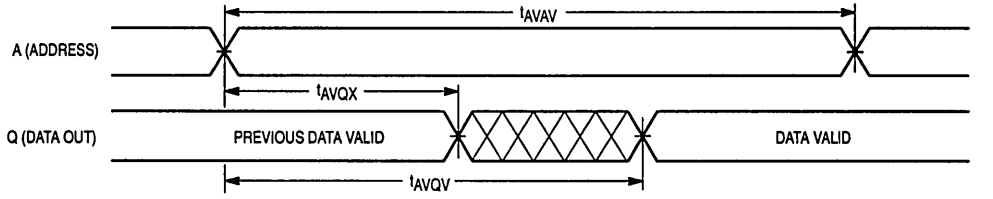


Figure 1B

TIMING LIMITS

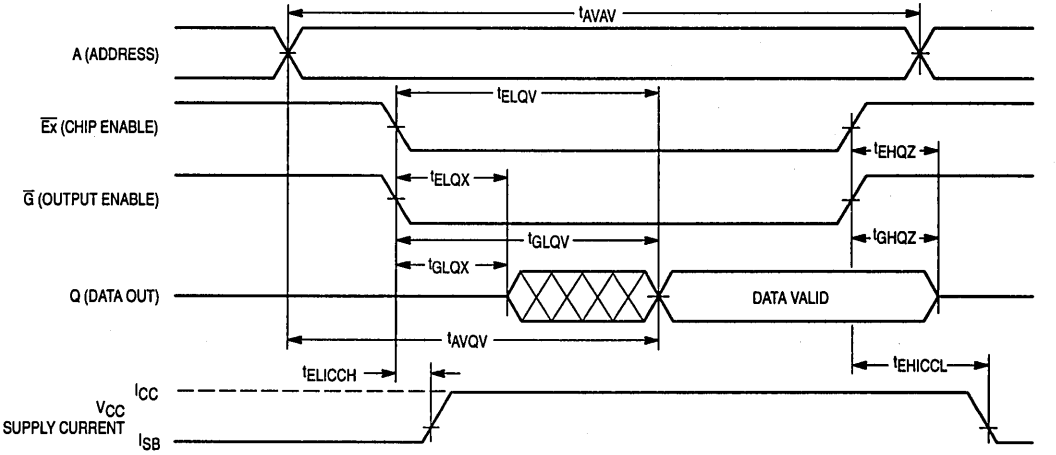
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the module point of view. Thus, the access time is shown as a maximum since the module never provides data later than that time.

READ CYCLE 1 (See Note)



NOTE: Device is continuously selected ($\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$).

READ CYCLE 2 (See Notes)



NOTES:
1. Addresses valid prior to or coincident with $\overline{E}$ going low.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.

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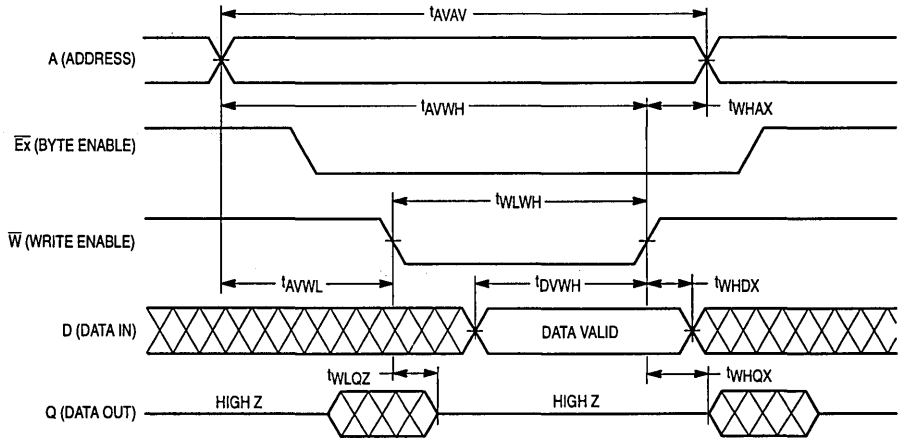
WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM3264A-15		MCM3264A-20		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	20	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	12	—	15	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	t_{WP}	12	—	15	—	ns	
Write Pulse Width, $\overline{G}$ High	t_{WLWH} t_{WLEH}	t_{WP}	10	—	12	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	7	—	8	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	7	0	8	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications; any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

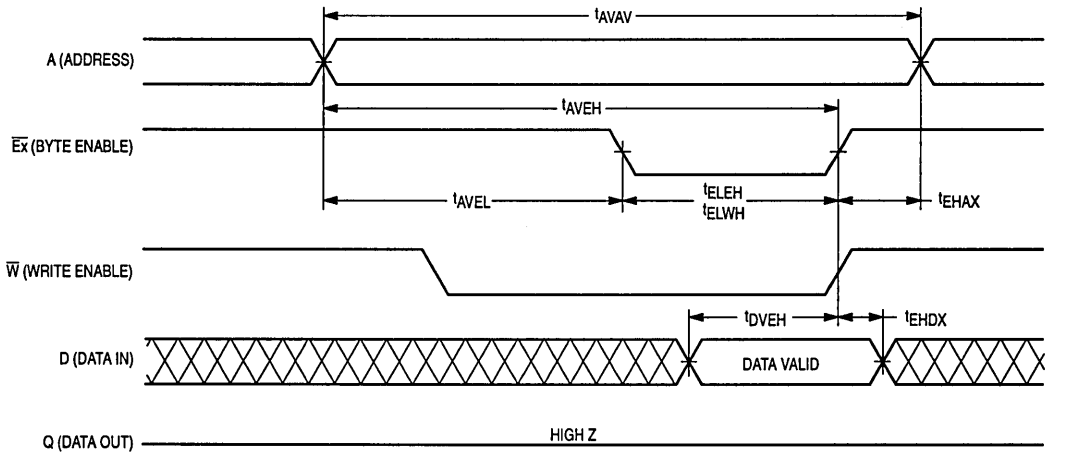


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

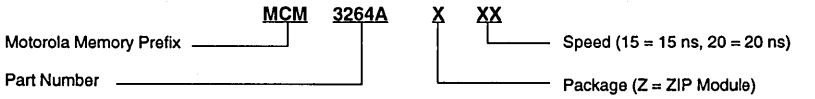
Parameter	Symbol		MCM3264A-15		MCM3264A-20		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	20	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	12	—	15	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	10	—	12	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	t_{DW}	7	—	8	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E4}$ are represented by $\overline{E}$ in these timing specifications; any combination of $\overline{Ex}$s may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM3264AZ15 MCM3264AZ20

MCM4464 Series

1MB R4000 Secondary Cache Fast Static RAM Module Set

Four MCM4464 modules comprise a full 1 MB of secondary cache for the R4000 processor. Each module contains nine MCM6709AJ fast static RAMs for a cache data size of 64K x 36. The tag portion, dependent on word line size, contains either two MCM6709AJ or one MCM6706AJ fast static RAMs. All input signals, except A0 and $\overline{WE}$ are buffered using 74FBT2827 drivers with series 25 Ω resistors.

The MCM6709AJ and MCM6706AJ are fabricated using high-performance silicon-gate BiCMOS technology. Static design eliminates the need for internal clocks or timing strobes.

All 1MB R4000 supported secondary cache options are available.

- Single 5 V ± 10% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Module Access Time: 12/15/17 ns
- Zero Wait-State Operation
- Unified or Split Seconday Cache Modules are Available (See Ordering Information for Details)
- Word Line Sizes of 4, 8, 16, and 32 are Available (See Ordering Information for Details)
- The Pin Compatible MCM44256 Series is also Available to Support a Full 4MB R4000 Secondary Cache.
- Decoupling Capacitors are Used for Each Fast Static RAM and Buffer, Along with Bulk Capacitance for Maximum Noise Immunity
- High Quality Multi-Layer FR4 PWB with Separate Power and Ground Plane

PIN NAMES	
A0 – A15	Address Inputs
$\overline{WE}$	Write Enable
$\overline{DCS}$	Data Enable
$\overline{TCS}$	Tag Enable
$\overline{OE}$	Output Enable
DQ0 – DQ35	Data Input / Output
TDQ0 – TDQ7	TAG Data Input / Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

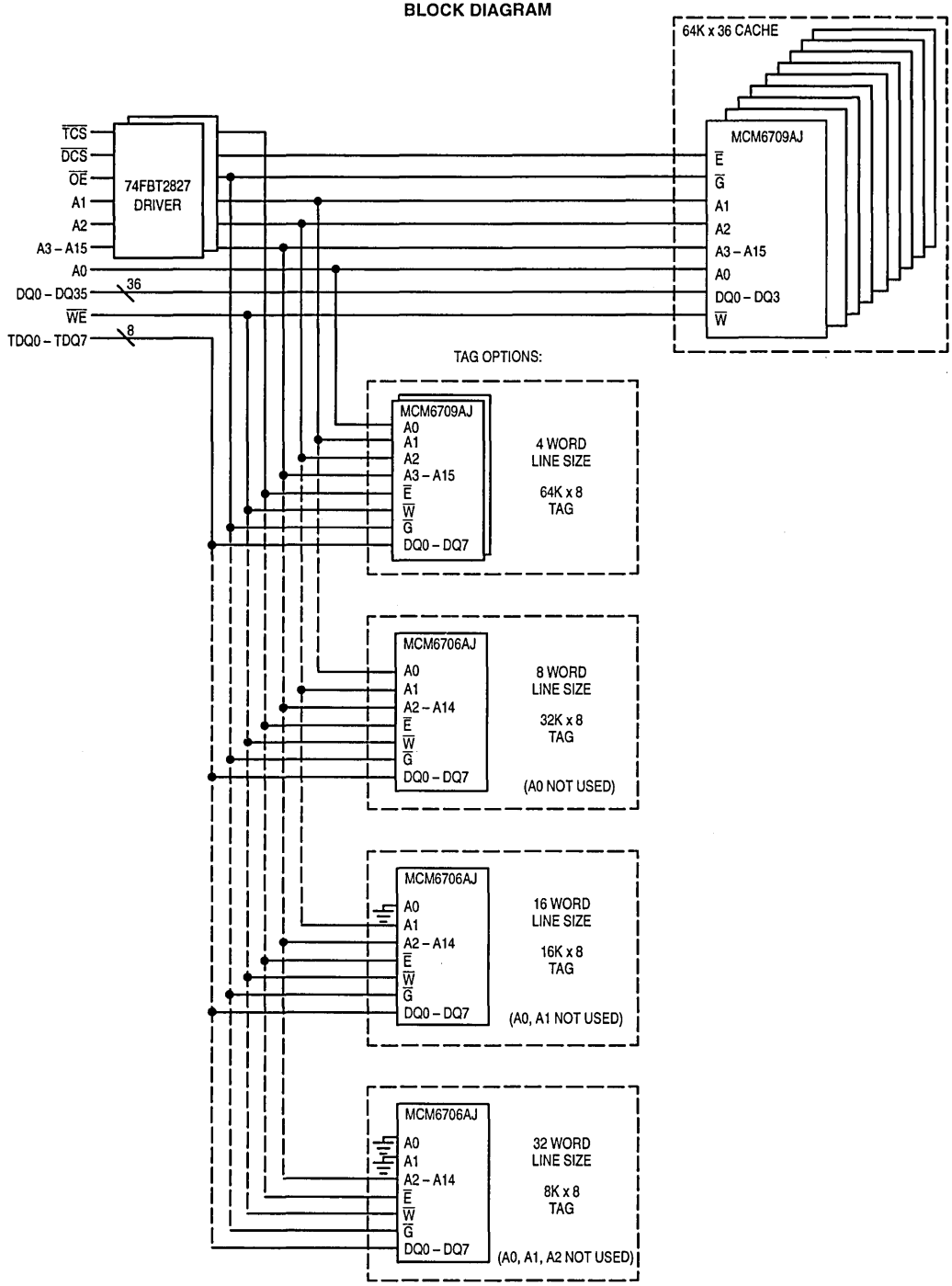
For proper operation of the device, V_{SS} must be connected to ground.

PIN ASSIGNMENT
80 LEAD SIMM — TOP VIEW

V_{CC}	2	1	V_{SS}
DQ1	4	3	DQ0
DQ3	6	5	DQ2
DQ5	8	7	DQ4
V_{SS}	10	9	DQ6
DQ8	12	11	DQ7
DQ10	14	13	DQ9
DQ12	16	15	DQ11
DQ14	18	17	DQ13
DQ15	20	19	V_{SS}
DQ17	22	21	DQ16
DQ19	24	23	DQ18
DQ21	26	25	DQ20
V_{SS}	28	27	DQ22
DQ23	30	29	V_{CC}
DQ25	32	31	DQ24
DQ27	34	33	DQ26
DQ29	36	35	DQ28
DQ30	38	37	V_{SS}
DQ32	40	39	DQ31
DQ34	42	41	DQ33
V_{SS}	44	43	DQ35
A0	46	45	$\overline{WE}$
A2	48	47	A1
A4	50	49	A3
A6	52	51	A5
V_{CC}	54	53	V_{SS}
$\overline{OE}$	56	55	$\overline{DCS}$
A8	58	57	A7
A10	60	59	A9
V_{SS}	62	61	A11
A13	64	63	A12
A15	66*	65	A14
NC	68*	67	NC
TDQ0	70	69	$\overline{TCS}$
TDQ1	72	71	V_{SS}
TDQ3	74	73	TDQ2
TDQ5	76	75	TDQ4
TDQ7	78	77	TDQ6
V_{SS}	80	79	V_{CC}

NOTE: Pin assignment is for unified cache. For split cache option, Pin 68 becomes Address MSB (A15) and Pin 66 is NC.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	10	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 25 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

These BiCMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at leat 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = V_{CCQ} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}				V
(DQ0 – 35, TDQ0 – 7, $\overline{WE}$, A0)		2.2	—	V_{CC} + 0.3 V*	
(A1 – A15, $\overline{OE}$, $\overline{DCS}$, $\overline{TCS}$)		2.0	—	V_{CC} + 0.3 V*	
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)
**V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 10	µA
Output Leakage Current ($\overline{G}$, $\overline{Ex}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	± 10	µA
AC Supply Current ($\overline{G}$, $\overline{Ex}$ = V_{IL}, I_{out} = 0 mA)	I_{CCA}	—	—	1850	mA
Output Low Voltage (I_{OL} = + 8 mA)	V_{OL}	—	—	0.4	V
OUtput High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

Note: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (A0, $\overline{WE}$)	C_{in}	—	110	pF
(A1 – A15, $\overline{OE}$, $\overline{DCS}$, $\overline{TCS}$)		—	10	
Input/Output Capacitance	C_{out}	—	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol		-12		-15		-17		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Address Access Time	t_{AVQV}	t_{AA}	—	12	—	15	—	17	ns	
A0 Access Time	t_{A0QV}	t_{A0A}	—	10	—	12	—	14	ns	
Data/Tag Enable Access Time	t_{ELQV}	t_{ACS}	—	12	—	15	—	17	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	9	—	10	—	11	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	ns	
Output Hold from A0 Change	t_{A0XQX}	t_{OH}	4	—	4	—	4	—	ns	
Data/Tag Enable Low to Output Active	t_{ELQX}	t_{LZ}	2	—	2	—	2	—	ns	3, 4
Data/Tag Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	1	9	1	10	1	11	ns	3, 4
Output Enable Low to Output Active	t_{GLQX}	t_{LZ}	1	—	1	—	1	—	ns	3, 4
Output Enable High to Output High-Z	t_{GHQZ}	t_{HZ}	1	9	1	10	1	11	ns	3, 4

NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Enable timings are the same for both $\overline{DCS}$ and $\overline{TCS}$.
3. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
4. This parameter is sampled and not 100% tested.

5

AC TEST LOADS

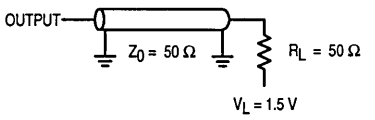


Figure 1A

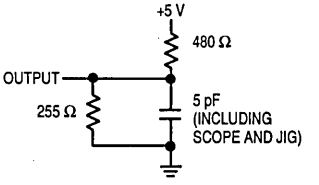
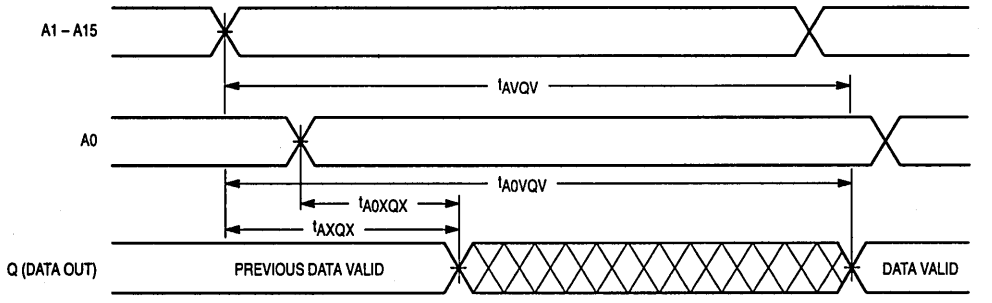


Figure 1B

TIMING LIMITS

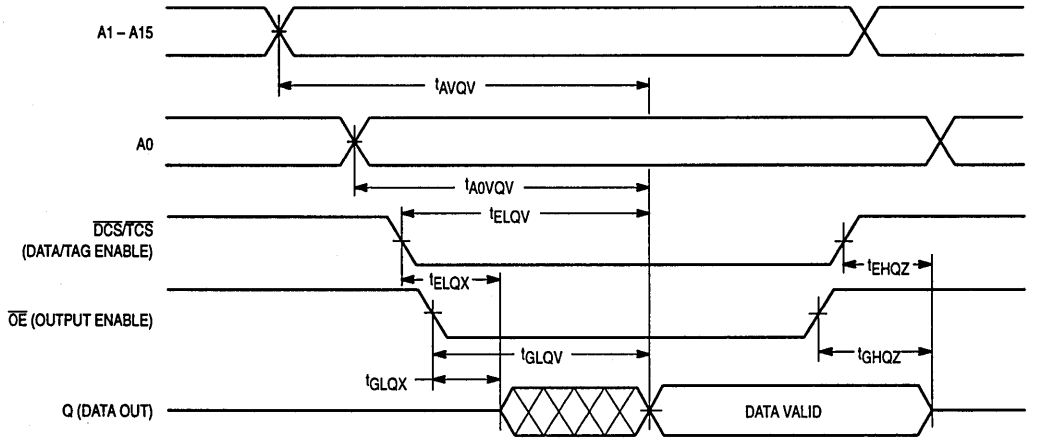
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note)



NOTE: Module is continuously selected ($\overline{DCS}$ or $\overline{TCS}$ = V_{IL}, $\overline{OE}$ = V_{IL}).

READ CYCLE 2 (See Note)



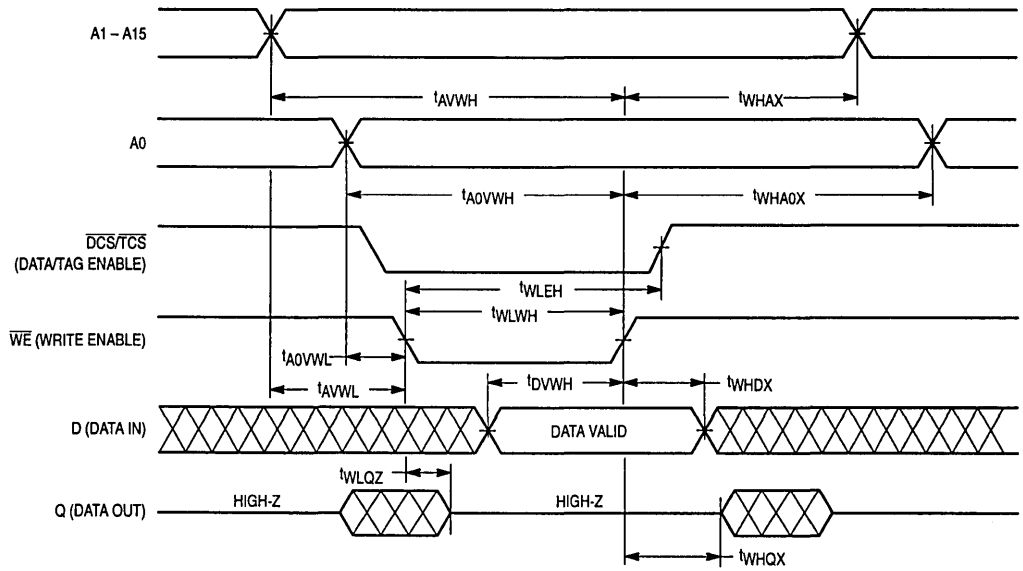
NOTE: Address valid prior to or coincident with $\overline{DCS}$ or $\overline{TCS}$ going low.

WRITE CYCLE 1 ($\overline{WE}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		-12		-15		-17		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
A0 Setup Time	t_{A0VWL}	t_{A0S}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	12	—	15	—	17	—	ns	
A0 Valid to End of Write	t_{A0VWH}	t_{A0W}	10	—	12	—	14	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	t_{WP}	7	—	10	—	12	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	6	—	7	—	8	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	4	0	5	0	6	ns	3, 4
Write High to Output Active	t_{WHQX}	t_{OW}	3	—	3	—	3	—	ns	3, 4
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	
Write Recovery Time – A0	t_{WHA0X}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{DCS}$ or $\overline{TCS}$ low and $\overline{WE}$ low.
2. Enable timings are the same for both $\overline{DCS}$ and $\overline{TCS}$.
3. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
4. This parameter is sampled and not 100% tested.

WRITE CYCLE 1



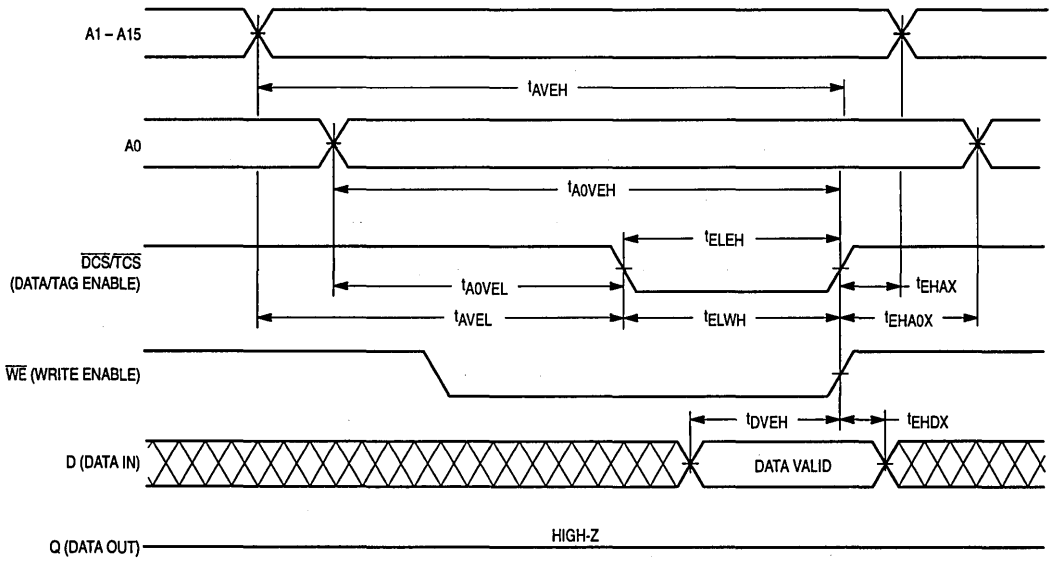
5

WRITE CYCLE 2 ($\overline{DCS}$ or $\overline{TCS}$ Controlled, See Notes 1 and 2)

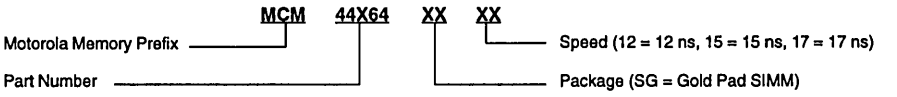
Parameter	Symbol		-12		-15		-17		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
A0 Setup Time	t_{A0VEL}	t_{A0S}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	12	—	15	—	17	—	ns	
A0 Valid to End of Write	t_{A0VEH}	t_{A0W}	10	—	12	—	14	—	ns	
Data/Tag Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	12	—	15	—	17	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	6	—	7	—	8	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	5	—	5	—	5	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	5	—	5	—	5	—	ns	
Write Recovery Time – A0	t_{EHA0X}	t_{WR}	5	—	5	—	5	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{DCS}$ or $\overline{TCS}$ low and $\overline{WE}$ low.
2. Enable timings are the same for both $\overline{DCS}$ and $\overline{TCS}$.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



Part Number	Unified/Split	Word Line Size	TAG Depth
MCM44A64	Unified	4	64K
MCM44B64	Unified	8	32K
MCM44C64	Unified	16	16K
MCM44D64	Unified	32	8K
MCM44E64	Split	4	64K
MCM44F64	Split	8	32K
MCM44G64	Spllit	16	16K
MCM44H64	Split	32	8K

5

MCM44256 Series

4MB R4000 Secondary Cache Fast Static RAM Module Set

Four MCM44256 modules comprise a full 4 MB of secondary cache for the R4000 processor. Each module contains nine MCM6729WJ fast static RAMs for a cache data size of 256K x 36. The tag portion, dependent on word line size, contains either two MCM6729WJ or one MCM6726WJ fast static RAMs. All input signals, except A0 and $\overline{WE}$ are buffered using 74FBT2827 drivers with series 25 Ω resistors.

The MCM6729WJ and MCM6726WJ are fabricated using high-performance silicon-gate BiCMOS technology. Static design eliminates the need for internal clocks or timing strobes.

All 4MB R4000 supported secondary cache options are available.

- Single 5 V ± 10% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Module Access Time: 12/15/17 ns
- Zero Wait-State Operation
- Unified or Split Seconday Cache is Supported
- Word Line Sizes of 4, 8, 16, and 32 are Available (See Ordering Information for Details)
- Decoupling Capacitors are Used for Each Fast Static RAM and Buffer, Along with Bulk Capacitance for Maximum Noise Immunity
- High Quality Multi-Layer FR4 PWB with Separate Power and Ground Plane

5

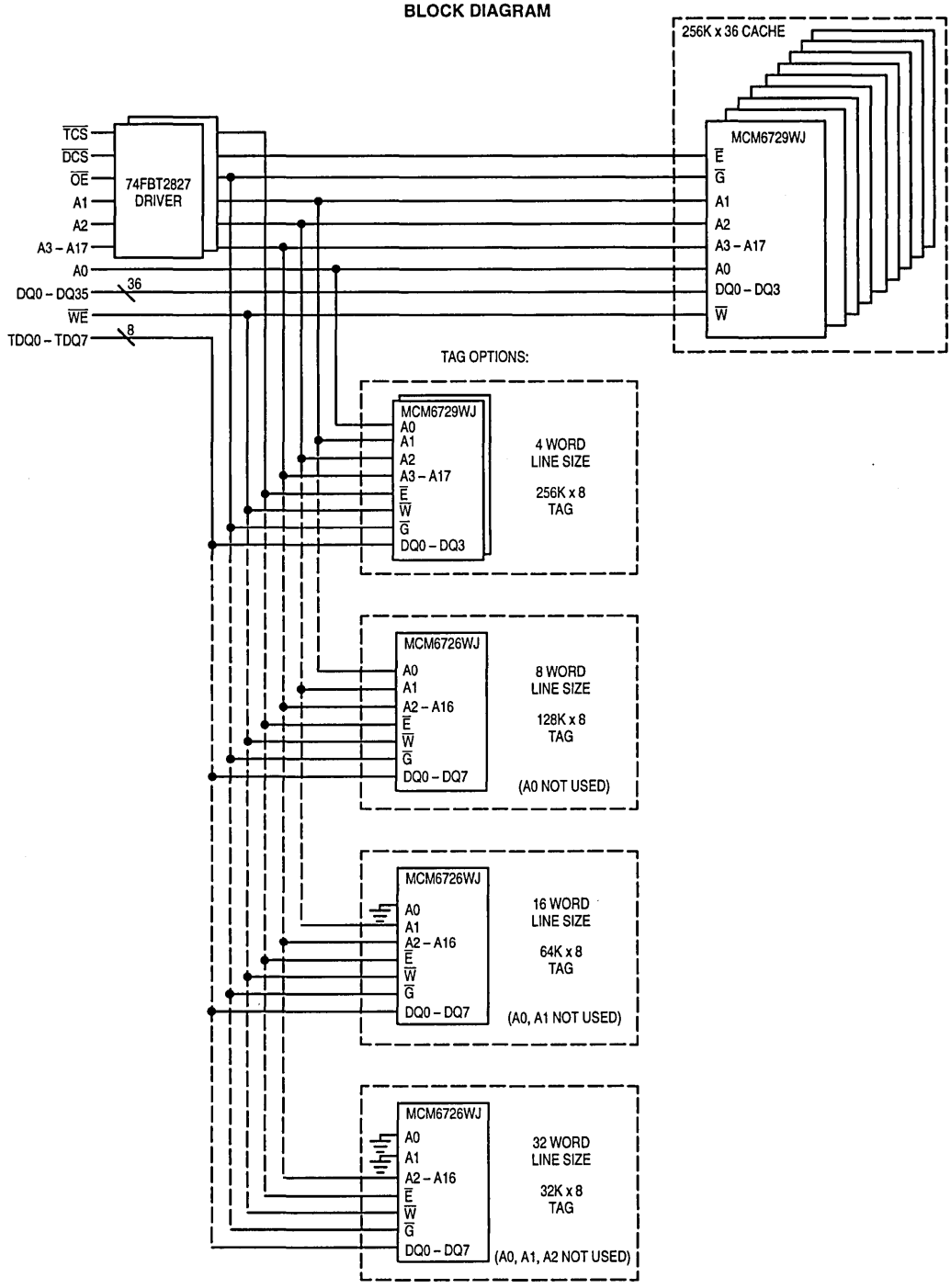
PIN NAMES	
A0 – A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{DCS}$	Data Enable
$\overline{TCS}$	Tag Enable
$\overline{OE}$	Output Enable
DQ0 – DQ35	Data Input / Output
TDQ0 – TDQ7	TAG Data Input / Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

For proper operation of the device, V_{SS} must be connected to ground.

PIN ASSIGNMENT
80 LEAD SIMM — TOP VIEW

V_{CC}	2	1	V_{SS}
DQ1	4	3	DQ0
DQ3	6	5	DQ2
DQ5	8	7	DQ4
V_{SS}	10	9	DQ6
DQ8	12	11	DQ7
DQ10	14	13	DQ9
DQ12	16	15	DQ11
DQ14	18	17	DQ13
DQ15	20	19	V_{SS}
DQ17	22	21	DQ16
DQ19	24	23	DQ18
DQ21	26	25	DQ20
V_{SS}	28	27	DQ22
DQ23	30	29	V_{CC}
DQ25	32	31	DQ24
DQ27	34	33	DQ26
DQ29	36	35	DQ28
DQ30	38	37	V_{SS}
DQ32	40	39	DQ31
DQ34	42	41	DQ33
V_{SS}	44	43	DQ35
A0	46	45	$\overline{WE}$
A2	48	47	A1
A4	50	49	A3
A6	52	51	A5
V_{CC}	54	53	V_{SS}
$\overline{OE}$	56	55	$\overline{DCS}$
A8	58	57	A7
A10	60	59	A9
V_{SS}	62	61	A11
A13	64	63	A12
A15	66	65	A14
A17	68	67	A16
TDQ0	70	69	$\overline{TCS}$
TDQ1	72	71	V_{SS}
TDQ3	74	73	TDQ2
TDQ5	76	75	TDQ4
TDQ7	78	77	TDQ6
V_{SS}	80	79	V_{CC}

BLOCK DIAGRAM



5

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	± 30	mA
Power Dissipation	P_D	10	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 25 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

These BiCMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at leat 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = V_{CCQ} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}				V
(DQ0 – 35, TDQ0 – 7, $\overline{WE}$, A0)		2.2	—	V_{CC} + 0.3 V*	
(A1 – A17, $\overline{OE}$, $\overline{DCS}$, $\overline{TCS}$)		2.0	—	V_{CC} + 0.3 V*	
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns)
**V_{IL} (min) = – 3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 10	µA
Output Leakage Current ($\overline{G}$, $\overline{Ex}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	± 10	µA
AC Supply Current ($\overline{G}$, $\overline{Ex}$ = V_{IL}, I_{out} = 0 mA)	I_{CCA}	—	—	1750	mA
Output Low Voltage (I_{OL} = + 8 mA)	V_{OL}	—	—	0.4	V
OUtput High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (A0, $\overline{WE}$)	C_{in}	—	110	pF
(A1 – A17, $\overline{OE}$, $\overline{DCS}$, $\overline{TCS}$)		—	10	
Input/Output Capacitance	C_{out}	—	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE (See Notes 1 and 2)

Parameter	Symbol		-12		-15		-17		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Address Access Time	t_{AVQV}	t_{AA}	—	12	—	15	—	17	ns	
A0 Access Time	t_{A0AQV}	t_{A0A}	—	10	—	12	—	14	ns	
Data/Tag Enable Access Time	t_{ELQV}	t_{ACS}	—	12	—	15	—	17	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	9	—	10	—	11	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	4	—	4	—	ns	
Output Hold from A0 Change	t_{A0XQX}	t_{OH}	4	—	4	—	4	—	ns	
Data/Tag Enable Low to Output Active	t_{ELQX}	t_{LZ}	2	—	2	—	2	—	ns	3, 4
Data/Tag Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	1	9	1	10	1	11	ns	3, 4
Output Enable Low to Output Active	t_{GLQX}	t_{LZ}	1	—	1	—	1	—	ns	3,4
Output Enable High to Output High-Z	t_{GHQZ}	t_{HZ}	1	9	1	10	1	11	ns	3, 4

NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Enable timings are the same for both $\overline{DCS}$ and $\overline{TCS}$.
3. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
4. This parameter is sampled and not 100% tested.

5

AC TEST LOADS

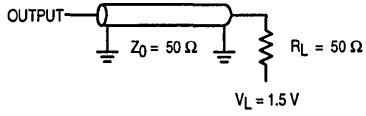


Figure 1A

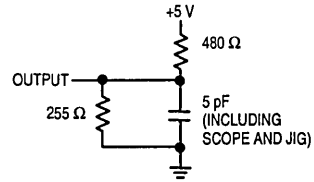
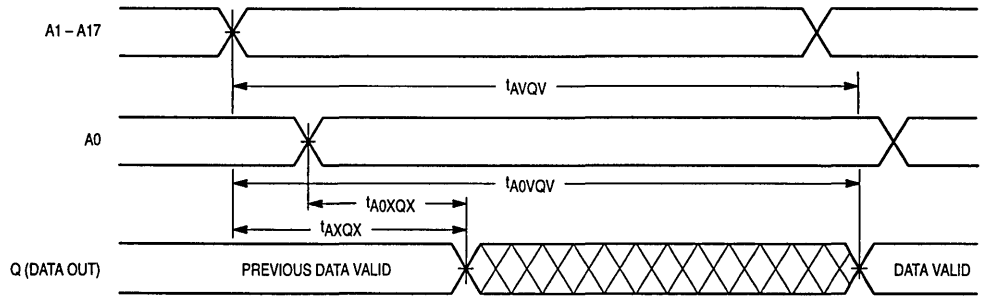


Figure 1B

TIMING LIMITS

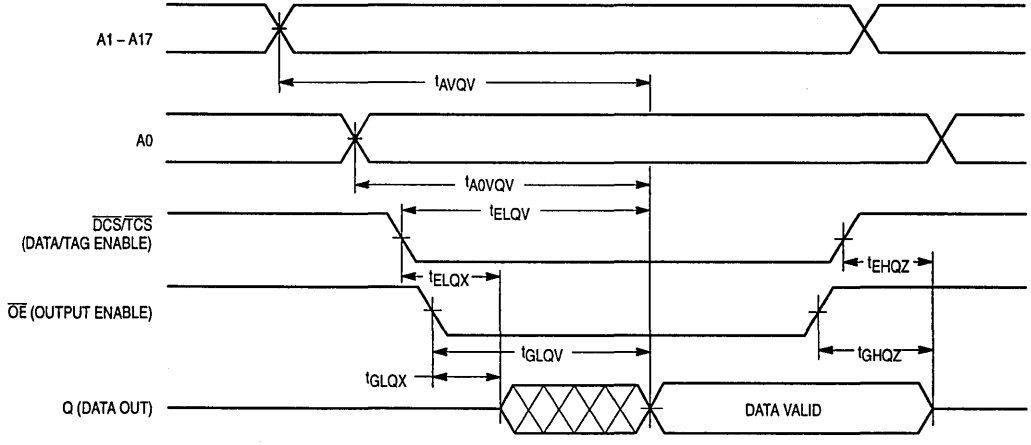
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note)



NOTE: Module is continuously selected ($\overline{DCS}$ or $\overline{TCS}$ = V_{IL}, $\overline{OE}$ = V_{IL})

READ CYCLE 2 (See Note)



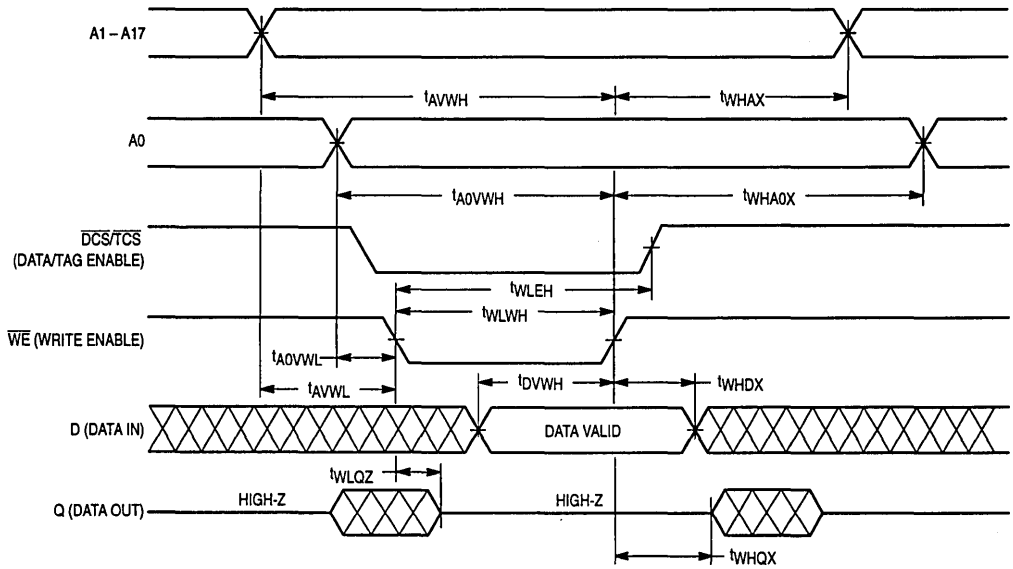
NOTE: Address valid prior to or coincident with $\overline{DCS}$ or $\overline{TCS}$ going low.

WRITE CYCLE 1 ($\overline{WE}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		-12		-15		-17		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
A0 Setup Time	t_{A0VWL}	t_{A0S}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	12	—	15	—	17	—	ns	
A0 Valid to End of Write	t_{A0VWH}	t_{A0W}	10	—	12	—	14	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	t_{WP}	7	—	10	—	12	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	6	—	7	—	8	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	4	0	5	0	6	ns	3, 4
Write High to Output Active	t_{WHQX}	t_{OW}	3	—	3	—	3	—	ns	3, 4
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	
Write Recovery Time – A0	t_{WHA0X}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{DCS}$ or $\overline{TCS}$ low and $\overline{WE}$ low.
2. Enable timings are the same for both $\overline{DCS}$ and $\overline{TCS}$.
3. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
4. This parameter is sampled and not 100% tested.

WRITE CYCLE 1

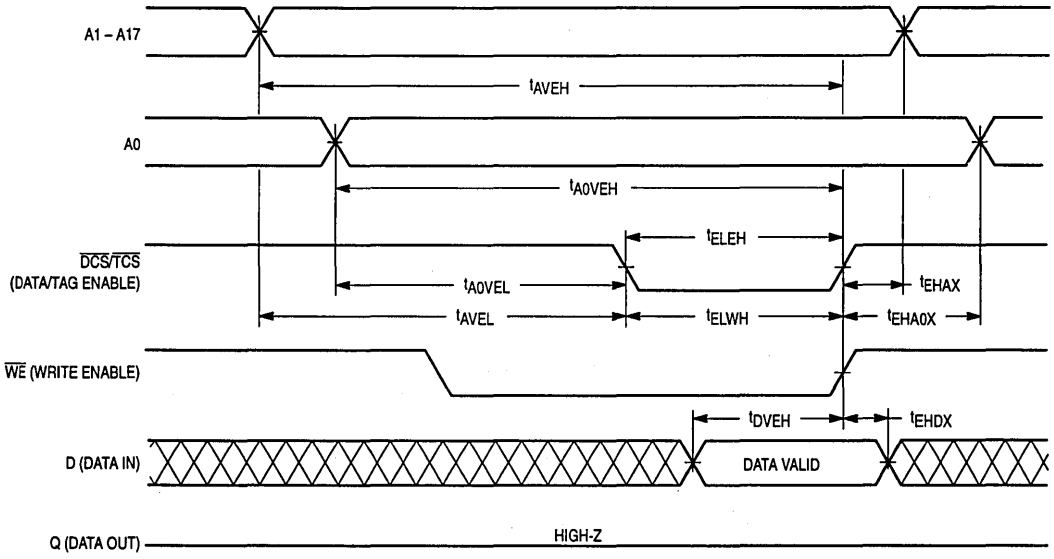


WRITE CYCLE 2 ($\overline{DCS}$ or $\overline{TCS}$ Controlled, See Notes 1 and 2)

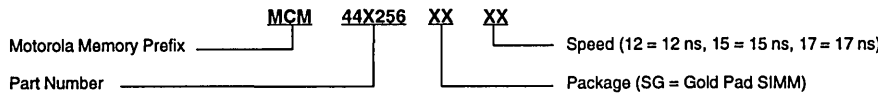
Parameter	Symbol		-12		-15		-17		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	
A0 Setup Time	t_{A0VEL}	t_{A0S}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	12	—	15	—	17	—	ns	
A0 Valid to End of Write	t_{A0VEH}	t_{A0W}	10	—	12	—	14	—	ns	
Data/Tag Enable to End of Write	t_{ELEH}, t_{ELWH}	t_{CW}	12	—	15	—	17	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	6	—	7	—	8	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	5	—	5	—	5	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	5	—	5	—	5	—	ns	
Write Recovery Time – A0	t_{EHA0X}	t_{WR}	5	—	5	—	5	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{DCS}$ or $\overline{TCS}$ low and $\overline{WE}$ low.
2. Enable timings are the same for both $\overline{DCS}$ and $\overline{TCS}$.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



Part Number	Unified/Split	Word Line Size	TAG Depth
MCM44A256	Unified/Split	4	256K
MCM44B256	Unified/Split	8	128K
MCM44C256	Unified/Split	16	64K
MCM44D256	Unified/Split	32	32K

5

MCM72BA32
MCM72BA64

Advance Information

256KB and 512KB BurstRAM™ Secondary Cache Module for Pentium™

The MCM72BA32SG and MCM72BA64SG are designed to provide a burtstable, high performance, 256K/512K L2 cache for the Pentium microprocessor. The modules are configured as 32K x 72 and 64K x 72 bits in a 136 pin dual readout single inline memory module (SIMM). The module uses four of Motorola's MCM67B618 or MCM67B518 BiCMOS BurstRAMs.

Bursts can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$). Subsequent burst addresses are generated internal to the BurstRAM by the burst advance ($\overline{ADV}$) input pin.

Write cycles are internally self timed and are initiated by the rising edge of the clock (K) input. Eight write enables are provided for byte write control.

The cache family is designed to interface with popular Pentium cache controllers with on board TAG.

PD0 – PD2 are reserved for density identification.

5

- Dual Readout SIMM for Circuit Density
- Single 5 V ± 5% Power Supply
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Byte Parity
- Fast Module Cycle Time: 66 MHz, 60 MHz, 50MHz
- Decoupling Capacitors for each Fast Static RAM
- High Quality Multi-Layer FR4 PWB With Separate Power and Ground Plane
- I/Os are 3.3 V Compatible

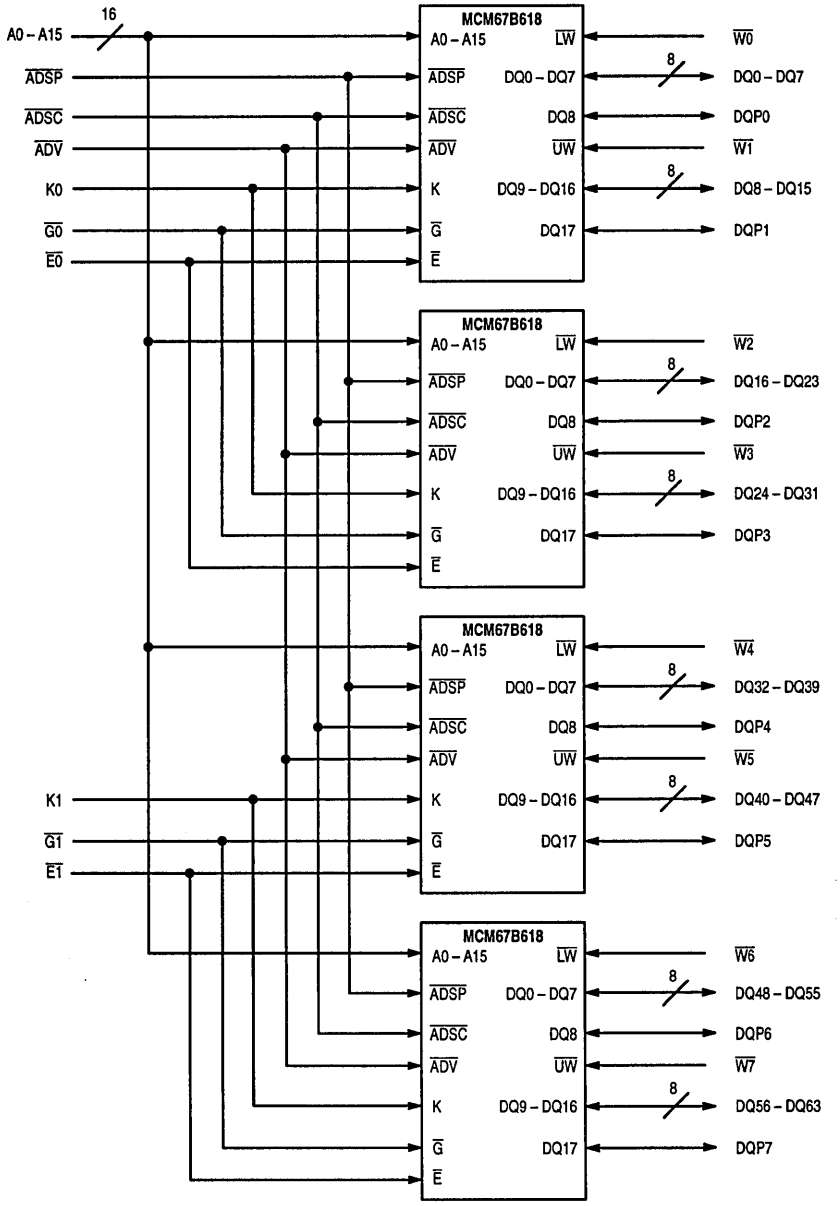
PIN ASSIGNMENT
68-LEAD DUAL READOUT SIMM
TOP VIEW

PD0	1	69	V_{SS}
PD1	2	70	PD2
DQ0	3	71	V_{CC}
DQ1	4	72	DQ2
V_{CC}	5	73	DQ3
DQ4	6	74	DQ5
DQ6	7	75	DQ7
DQP0	8	76	V_{SS}
DQ8	9	77	DQ9
DQ10	10	78	DQ11
V_{SS}	11	79	DQ12
K0	12	80	V_{SS}
V_{SS}	13	81	DQ13
DQ14	14	82	DQ15
V_{CC}	15	83	DQP1
DQ16	16	84	V_{SS}
DQ17	17	85	DQ18
DQ19	18	86	DQ20
DQ21	19	87	DQ22
V_{CC}	20	88	DQ23
DQP2	21	89	V_{SS}
DQ24	22	90	DQ25
DQ26	23	91	DQ27
DQ28	24	92	DQ29
V_{SS}	25	93	DQ30
DQ31	26	94	V_{SS}
DQP3	27	95	$\overline{E0}$
V_{SS}	28	96	$\overline{W1}$
$\overline{W0}$	29	97	$\overline{W3}$
$\overline{W2}$	30	98	$\overline{G0}$
$\overline{ADSP}$	31	99	$\overline{ADSC}$
$\overline{ADV}$	32	100	V_{SS}
V_{CC}	33	101	$\overline{G1}$
$\overline{W4}$	34	102	$\overline{W5}$
$\overline{W6}$	35	103	$\overline{W7}$
DQ32	36	104	$\overline{E1}$
DQ33	37	105	DQ34
V_{SS}	38	106	DQ35
DQ36	39	107	DQ37
DQ38	40	108	V_{CC}
DQ39	41	109	DQP4
DQ40	42	110	DQ41
V_{CC}	43	111	DQ42
DQ43	44	112	DQ44
DQ45	45	113	V_{SS}
DQ46	46	114	DQ47
DQP5	47	115	DQ48
V_{SS}	48	116	DQ49
K1	49	117	V_{SS}
V_{SS}	50	118	DQ50
DQ52	51	119	DQ51
DQ53	52	120	DQ54
DQ55	53	121	DQ56
DQP6	54	122	V_{SS}
V_{CC}	55	123	DQ57
DQ58	56	124	DQ59
DQ60	57	125	DQ61
DQ62	58	126	DQ63
DQP7	59	127	V_{CC}
A0	60	128	A1
A2	61	129	A3
A4	62	130	A5
A6	63	131	A7
A8	64	132	V_{SS}
A10	65	133	A9
A12	66	134	A11
A14	67	135	A13
V_{SS}	68	136	A15

PIN NAMES	
A0 - A15	Address Inputs
K0, K1	Clock
$\overline{W0}$ - $\overline{W7}$	Byte Write
$\overline{E0}$, $\overline{E1}$	Module Enable
$\overline{G0}$, $\overline{G1}$	Module Output Enable
DQ0 - DQ63	Cache Data Input/Output
DQP0 - DQP7	Data Parity Input/Output
$\overline{ADSC}$	Controller Address Status
$\overline{ADSP}$	Processor Address Status
$\overline{ADV}$	Burst Advance
PD0 - PD2	Presence Detect
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

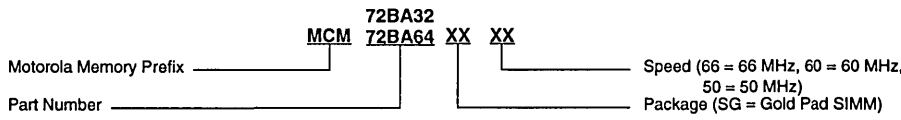
5

32K/64K x 72 BurstRAM MEMORY MODULE BLOCK DIAGRAM



5

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers —	MCM72BA32SG66	MCM72BA32SG60	MCM72BA32SG50
	MCM72BA64SG66	MCM72BA64SG60	MCM72BA64SG50

5

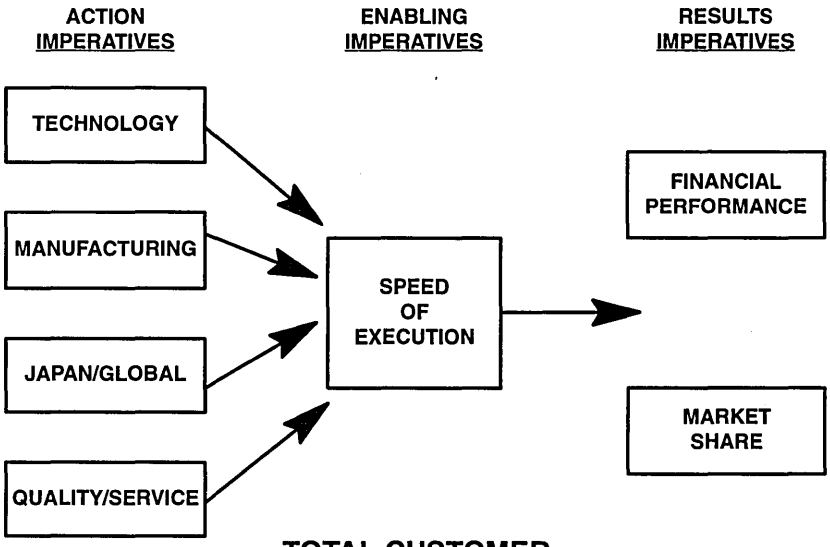
Military Products

6

In addition to the parts covered in this data book, Motorola also offers a wide range of military memory parts. For more information, including a complete military memory product listing, please refer to DL144/D, *Military Memory Family Data.*

Reliability Information 7

MOTOROLA
SEMICONDUCTOR PRODUCTS SECTOR
IMPERATIVES



TOTAL CUSTOMER SATISFACTION

DIVISION QUALITY STATEMENT

MOTOROLA FAST STATIC RAM PRODUCTS DIVISION

The Fast Static RAM Products Division is committed to being a world class CMOS, BiCMOS, Application Specific, and Module Fast Static RAM supplier. This means the integration of outstanding product and technology designs, linked with excellent manufacturing, cycle time, customer service, and engineering analysis.

This will be accomplished through dedication to a continuous quality improvement culture that will ensure our success in reaching the Motorola Corporate goal of total customer satisfaction.

We trust that you will experience Motorola Fast Static RAM Products Division as the best memory supplier through WORLD CLASS product margins and services.

Roger Kung
Vice–President and General Manager
Fast Static RAM Division
Microprocessor and Memory Technologies Group

Michael Phillips
Director, Reliability and Quality Assurance
MOS Memory Products
Microprocessor and Memory Technologies Group

QUALITY SYSTEMS

Motorola Fast Static RAM Products Division maintains a World Wide Quality Assurance system that is second to none. Daily status reports are received from remote locations, and any problems that arise are tackled on a timely basis. The Fast Static RAM Products Division is also a leader in accurate and efficient methods of quality data collection and reporting.

Every unit that the Fast Static Ram Products Division produces is coded so that complete traceability is maintained, including visibility to the wafer and assembly lot level. The Quality System ensures that we can provide any specific processing information to our customers on request.

INTERNAL QUALIFICATION DISCIPLINE

Motorola recognizes the need to establish that all Fast Static RAM devices, both new products as well as existing ones, reach and maintain a level of quality and reliability that is unsurpassed in the electronics marketplace. To ensure this, internal qualification requirements, procedures, and methods as well as vendor qualification specifications have been developed. These activities are intended to provide a consistent, comprehensive, and methodical approach to device qualification and to improve our customer's understanding of Motorola's qualification results and their subsequent application implications.

For qualification results to be valid and acceptable, the collected data must be proven accurate to the highest possible confidence level. Therefore, a complete device history and data log is kept with any lost or missing data potentially leading to test results that are unusable for qualification purposes. Testing conditions and pass/fail criteria are established before stressing begins. Strict adherence to these criteria and the use of control devices ensure that the test results are valid and meaningful.

New Fast Static RAM devices which are under development or in the prototype stage are subject to requirements defined for the three levels of the development cycle. These levels are the alpha, beta, and introductory phases of device development. Each phase contains guidelines and controls concerning issues such as device labeling, number of customers, sample quantities, pricing and stocking levels, and open-order-entry timing. Decisions regarding these items are made jointly by marketing, design, product, and reliability personnel.

JOINT QUALIFICATION

As a result of the rigorous discipline used for internal qualification of Motorola Fast Static RAM products, our customers can benefit from joint qualification activities. Motorola's clearly defined qualification procedures improve the customer's ability to comprehend the qualification results in an effective manner which aides in their qualification decision making process. Through parallel qualification activities between Motorola and its customers, this procedure can cut qualification costs by reducing duplication of effort, improving resource utilization, and shortening introduction cycle time. This helps to ensure competitive edge advantages for our customers.

Joint Qualification activities result in a partnership type of interaction between Motorola and its customers on an engineering level. This assists our customers in two critical areas. First, it allows them to understand more clearly the strengths and weaknesses of Motorola's products. Secondly, our customers can make clear decisions concerning which stresses they need to concentrate on during their internal qualification activities.

QUALITY MONITORING

Average Outgoing Quality (AOQ) refers to the number of devices per million that are outside specification limits at the time of shipment. Motorola has continually improved its outgoing quality, and has established a goal of zero defects. This level of quality will lead to vendor certification programs with many of our customers. The program ensures a certain level of quality, thus allowing a customer to either reduce or eliminate the need for incoming inspections.

By paying strict attention to quality at an early stage, the possibility of failures occurring further down the line is greatly minimized. Motorola's electrical parametric testing eliminates devices that do not conform to electrical specification. Additional parametric testing on a sample basis provides data for continued improvement.

AVERAGE OUTGOING QUALITY CALCULATION

$$\text{AOQ in PPM} = (\text{Process Average}) \bullet (\text{Lot Acceptance Rate}) \bullet (10^6)$$

$$\text{Process Average} = \frac{\text{Total Projected Reject Devices}^*}{\text{Total Number of Devices}}$$

$$\text{Projected Reject Devices} = \frac{\text{Defects in Sample}}{\text{Sample Size}} \bullet \text{Lot Size}$$

$$\text{Total Number of Devices} = \text{Sum of all the units in each submitted lot}$$

$$\text{Lot Acceptance Rate} = 1 - \frac{\text{Number of Lots Rejected}}{\text{Number of Lots Tested}}$$

*10^6 = Conversion to parts per million (PPM)

The chart in Figure 1 indicates the product Average Outgoing Quality performance as measured in parts per million.

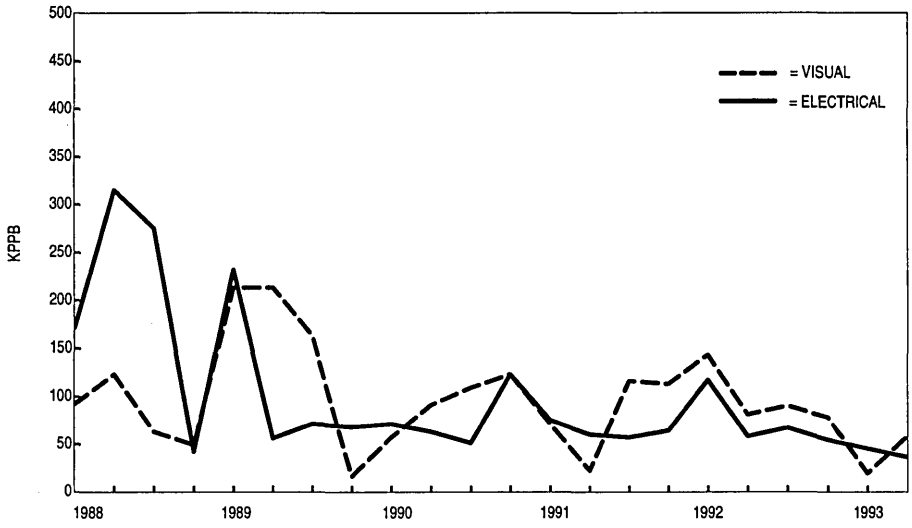


Figure 1. FSRAM AOQ

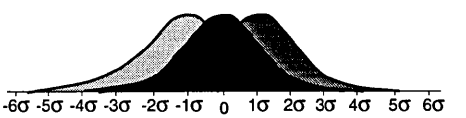
STATISTICAL PROCESS CONTROL

Motorola's Fast Static RAM Products Division is continually pursuing new ways to improve product quality. Initial design improvement is one method that can be used to produce a superior product. Equally important to outgoing product quality is the ability to produce product that consistently conforms to specification. Process variability is the basic enemy of semiconductor manufacturing since it leads to product variability. Used in all phases of Motorola's product manufacturing, STATISTICAL PROCESS CONTROL (SPC) replaces variability with predictability. The traditional philosophy in the semiconductor industry has been adherence to the data sheet specification. Using SPC methods ensures that the product will meet specific process requirements throughout the manufacturing cycle. The emphasis is on defect prevention, not detection. Predictability through SPC methods requires the manufacturing culture to focus on constant and permanent improvements. Usually, these improvements cannot be bought with state-of-the-art equipment or automated factories. With quality in design, process, and material selection, coupled with manufacturing predictability, Motorola produces world class products.

The immediate effect of SPC manufacturing is predictability through process controls. Product centered and distributed well within the product specification benefits Motorola with fewer rejects, improved yields, and lower cost. The direct benefit to Motorola's customers includes better incoming quality levels, less inspection time, and ship-to-stock capability. Circuit performance is often dependent on the cumulative effect of component variability. Tightly controlled component distributions give the customer greater circuit predictability. Many customers are also converting to just-in-time (JIT) delivery programs. These programs require improvements in cycle time and yield predictability achievable only through SPC techniques. The benefit derived from SPC helps the manufacturer meet the customer's expectations of higher quality and lower cost product.

Ultimately, Motorola will have Six Sigma capability on all products. This means parametric distributions will be centered within the specification limits, with a product distribution of plus or minus Six Sigma about mean. Six Sigma capability, shown graphically in Figure 2, details the benefit in terms of yield and outgoing quality levels. This compares a centered distribution versus a 1.5 sigma worst case distribution shift.

New product development at Motorola requires more robust design features that make them less sensitive to minor variations in processing. These features make the implementation of SPC much easier.



Standard Deviations From Mean

Distribution Centered	Distribution Shifted ± 1.5
At ± 3 σ 2700 ppm defective 99.73% yield	66810 ppm defective 93.32% yield
At ± 4 σ 63 ppm defective 99.9937% yield	6210 ppm defective 99.379% yield
At ± 5 σ 0.57 ppm defective 99.999943% yield	233 ppm defective 99.9767% yield
At ± 6 σ 0.002 ppm defective 99.9999998% yield	3.4 ppm defective 99.99966% yield

Figure 2. Percent Defective and Yield from a Normal Distribution of Product with 6σ Capability

MARKING PERMANENCY, HERMETICITY, AND SOLDERABILITY MONITORS

Marking permanency testing is performed per Motorola specification. The procedure involves soaking the device in various solvents, brushing the markings, and then inspecting the markings for legibility.

Hermeticity monitoring includes tests for both fine and gross leaks in the hermetic package seal.

Solderability testing is used to ensure that device leads can be soldered without voids, discoloration, flaking, dewetting, or bridging. Typically, the test specifies steam preconditioning followed by a 235 to 260°C solder dip and microscope inspection of the leads.

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RELIABILITY STRESS TESTS

The following summary briefly describes the various reliability tests included in the Motorola reliability monitor program.

DYNAMIC EARLY FAIL STUDY

This stress is performed to accelerate infant mortality failure mechanisms, which are defects that occur within the first year of normal device operation. Typical stress is a temperature of 125°C, nominal voltage (6.5 V), and a duration of 72 hours. All devices used in this test are sampled directly after the standard production final test flow with no prior burn-in or other prescreening, unless called out in the normal production flow.

DYNAMIC AND STATIC LONG TERM LIFETEST

Both Dynamic and Static Long Term Lifetests are performed to accelerate failure mechanisms and access parametric shifts, which are voltage and thermally activated. This is done through the application of extreme temperatures and the use of biased operating conditions. Typical stress temperature is 125°C with the bias applied being equal to or greater than the data sheet nominal value. All devices used in the long term lifetest are sampled from the Dynamic Early Fail Study. Testing is either performed with dynamic signals applied to the devices or in a static bias configuration for a test duration of 1008 hours.

TEMPERATURE CYCLE

This test accelerates the effects of thermal expansion mismatch among the different components within a specific die and packaging system. This test is typically performed to minimum and maximum temperatures of – 65 to + 150°C for a duration of 500 cycles. During temperature cycle testing, devices are inserted into a cycling system and held at cold dwell temperature for at least ten minutes. Following this cold dwell, the devices are heated to the hot dwell where they remain for another ten minutes. The system employs a circulating air environment to assure rapid stabilization at the specified temperature.

THERMAL SHOCK

The objective of this test is the same as that for Temperature Cycle testing: to emphasize differences in expansion coefficients for components of the packaging system. However, thermal shock provides additional stress because the device is exposed to a sudden change in temperature due to the transfer time of ten seconds maximum as well as the increased thermal conductivity of a liquid ambient. This test is typically performed to minimum and maximum temperatures of – 65 to + 150°C for a duration of 500 cycles. Devices are placed in a fluorocarbon bath and cooled to minimum specified temperature. After being held in the cold chamber for five minutes, the devices are transferred to an adjacent chamber filled with fluorocarbon at the maximum specified temperature for an equivalent time. Two five minute dwells plus two ten second transitions constitute one cycle.

TEMPERATURE HUMIDITY BIAS (THB)

This is an environmental test performed at a temperature of 85°C and a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated circuits. A nominal static bias is applied to the device to create the electrolytic cells necessary to accelerate corrosion of the metalization. Typical stress duration is 1008 hours.

PRESSURE TEMPERATURE HUMIDITY BIAS (PTHB)

This test is performed to accelerate the effects of moisture penetration with the dominant effect being corrosion. This test detects similar failure mechanisms as THB but at a greatly accelerated rate. Conditions employed during this test are a temperature of 148°C, humidity of 90%, 44 psig, and a nominal static bias voltage. Typical stress duration is 72 hours.

SMT PRECONDITIONING STRESS

The purpose of this test is to simulate the manufacturing steps involved in mounting and reworking a surface mount device used in customer applications. The test consists of simulating ambient moisture absorption by the device followed by exposure to temperatures typical of solder reflow. Devices are exposed to 85°C/85% relative humidity until saturated (non-moisture sensitive devices) or 30°C/60% relative humidity (moisture sensitive devices) followed by four passes of vapor phase reflow (215°C) for 120 seconds per pass.

AUTOCLAVE

Autoclave is an environmental test that measures devices resistance to moisture penetration and the resultant effects of galvanic corrosion. Conditions employed during the test include 121°C, 100% relative humidity, and 15 psig. Corrosion of the die is the expected failure mechanism. Autoclave is a highly accelerated and destructive test. Typical test duration is 96 hours.

SYSTEM SOFT ERROR

System soft error is designed to detect errors caused by impact ionization of silicon by high energy particles. This stress is performed on a system level basis. The system is operated for millions of device hours to obtain an accurate measure of actual system soft error performance.

Applications Information

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TYPICAL OPERATING CURVES

The terminated transmission line (T-line) shown in Figure 1A of the data sheets represents the actual test environment seen by the device under test (DUT). Because these SRAMs have fast edge rates (ranging from 1.5 V/ns to 3.5 V/ns), transmission line effects are encountered in the test environment. For the purpose of maintaining signal integrity, a 50 Ω termination is placed at the far end (tester's input) of the 50 Ω T-line. All of Motorola's Fast SRAM's output buffers have been designed to supply high current (> 50 mA) demanded by both the 50 Ω test environment as well as heavily capacitive system applications.

Although this test load may closely represent the load in your design, you may wish to simulate the SRAM's performance in your system. For this reason, a SPICE output buffer model is available upon request from the factory.

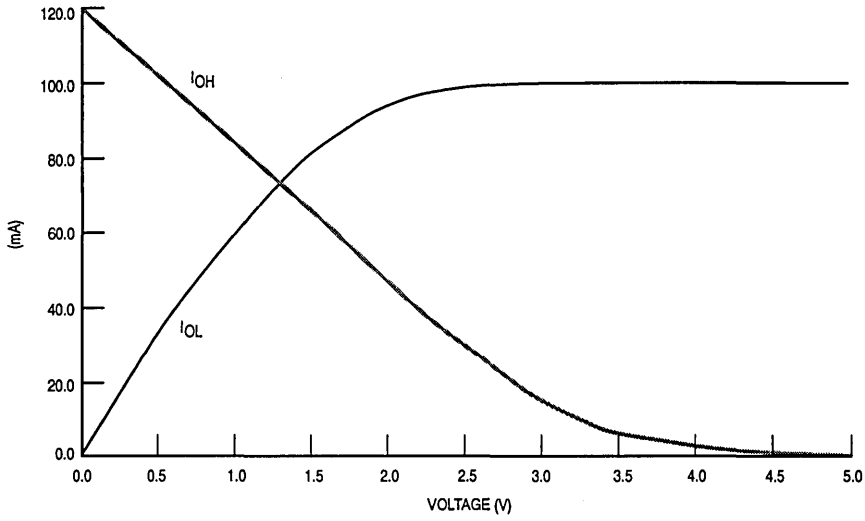

Figure 1. I_{OL}/I_{OH} Output Buffer Characteristics (I_{out} vs V_{out}) for MCM6226A, MCM6227A, MCM6229A

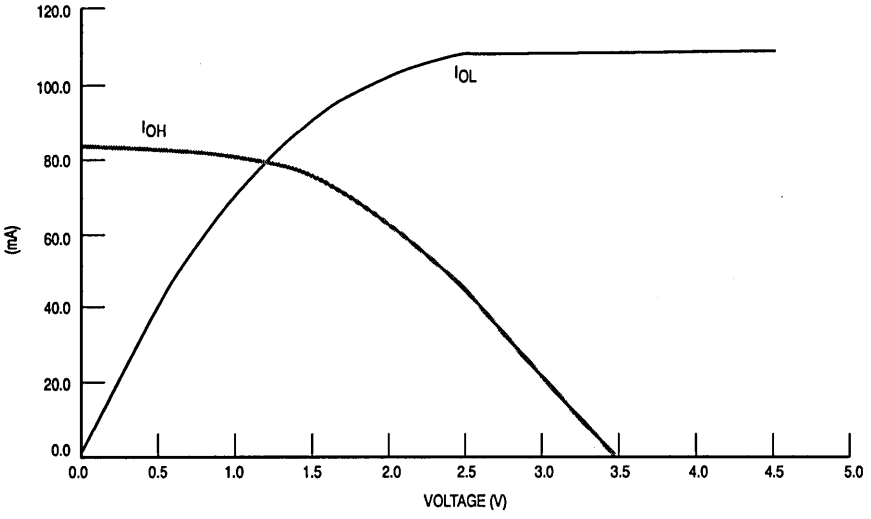

Figure 2. I_{OL}/I_{OH} Output Buffer Characteristics (I_{out} vs V_{out}) for MCM6726A, MCM6728A, MCM6729A

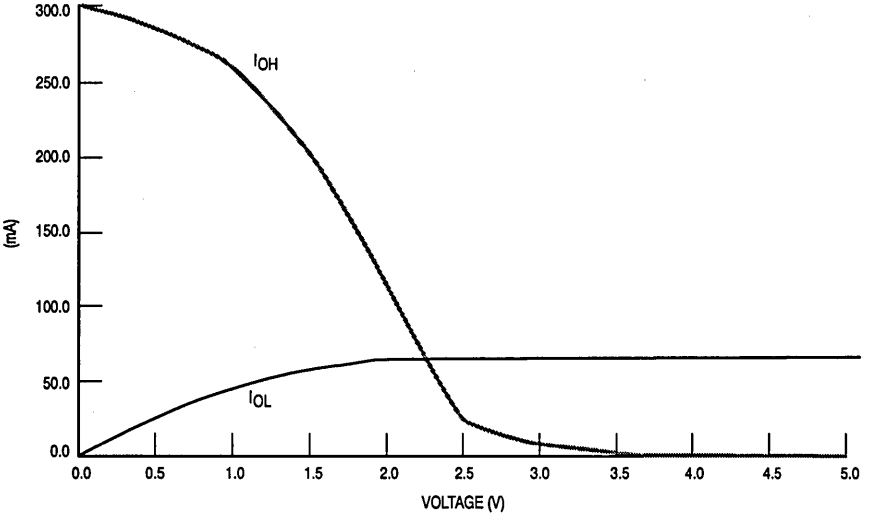

Figure 3. I_{OL}/I_{OH} Output Buffer Characteristics (I_{out} vs V_{out}) for MCM6705A, MCM6706A, MCM6708A, MCM6709A

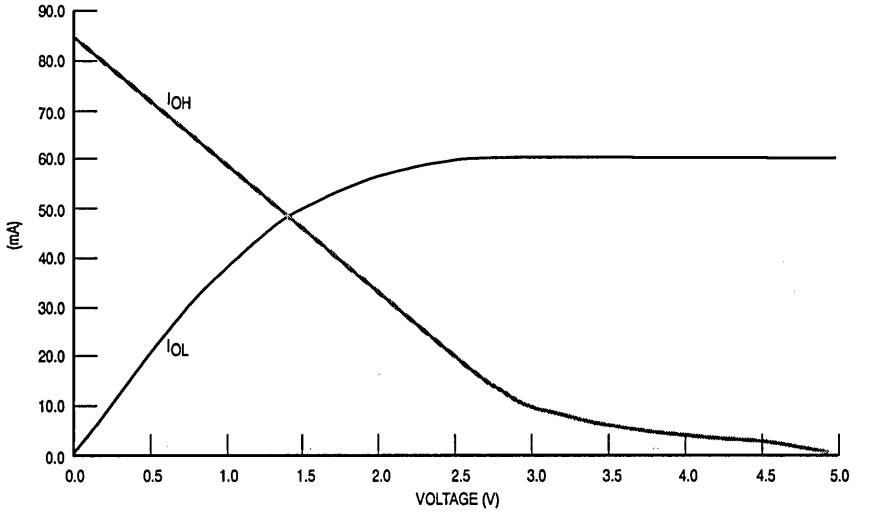

Figure 4. I_{OL}/I_{OH} Output Buffer Characteristics (I_{out} vs V_{out}) for MCM6208C, MCM6209C, MCM6288C

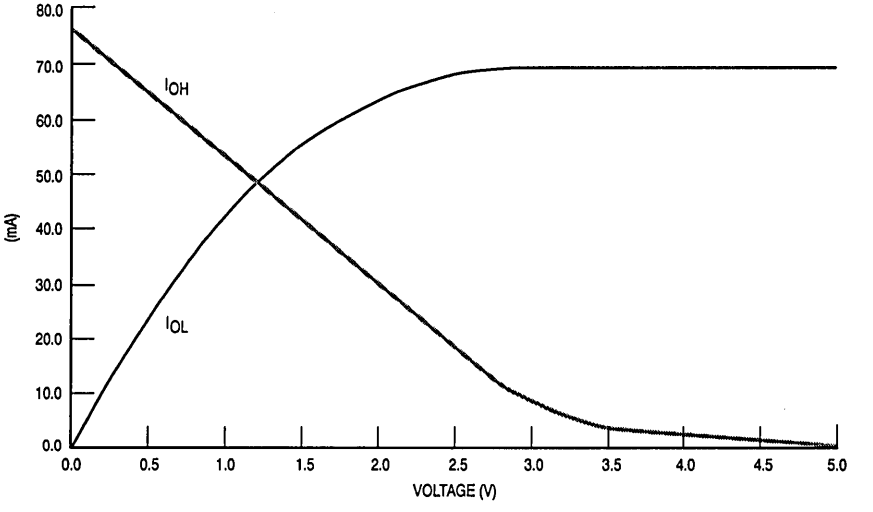

Figure 5. I_{OL}/I_{OH} Output Buffer Characteristics (I_{out} vs V_{out}) for MCM6205C, MCM6206C, MCM6264C, MCM6265C, MCM56824A, MCM56824AZP

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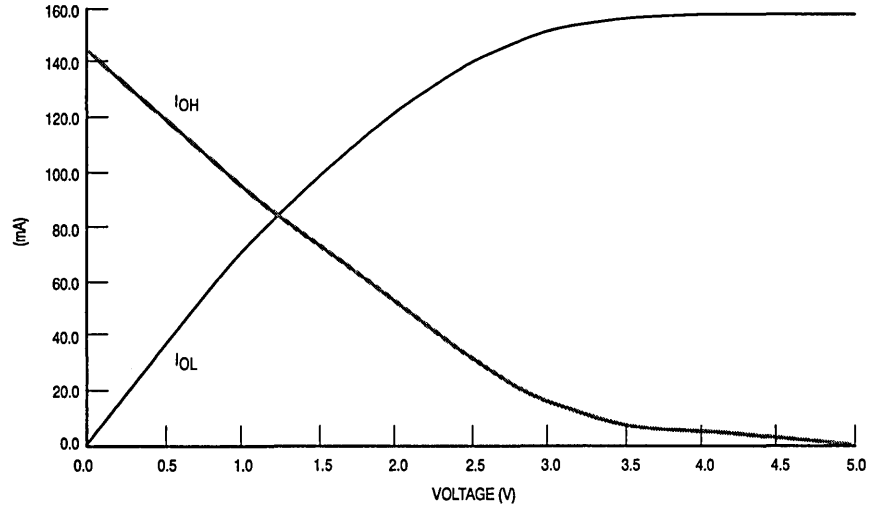


Figure 6. I_{OL}/I_{OH} Output Buffer Characteristics (I_{out} vs V_{out}) for MCM62110, MCM62486A, MCM62940A, MCM62990A, MCM62995A, MCM62996

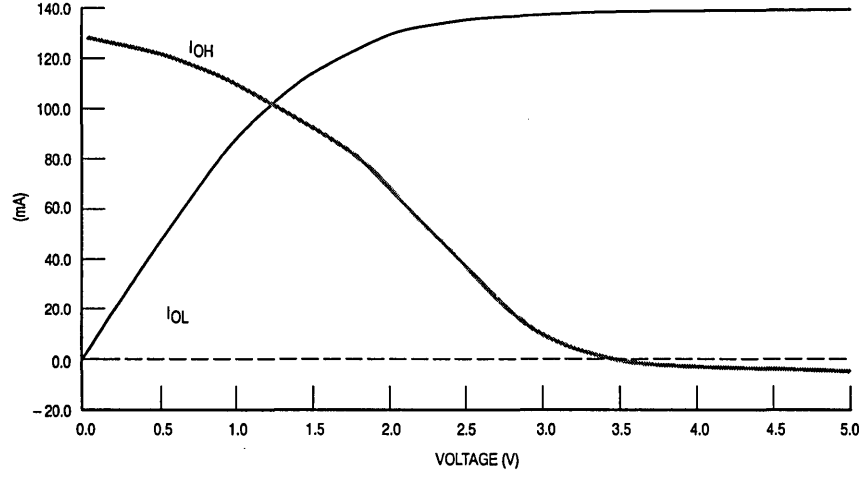


Figure 7. I_{OL}/I_{OH} Output Buffer Characteristics (I_{out} vs V_{out}) for MCM67A518, MCM67B518, MCM67C518, MCM67H518, MCM67J518, MCM67M518, MCM67W518 MCM67A618, MCM67B618, MCM67C618, MCM67H618, MCM67J618, MCM67M618, MCM67W618

THERMAL PERFORMANCE OF FAST STATIC RAM PACKAGES

The following explains the test and simulation methodologies that are used to determine thermal performance. Simulation results are reported for most of Motorola's Fast Static RAM packages currently in use.

JUNCTION TO AMBIENT THERMAL RESISTANCE

The thermal performance of a surface mount integrated circuit package is normally reported as a junction to ambient thermal resistance. Theta JA, θ_{JA}, and $R\theta_{JA}$ are the normal nomenclatures. Theta JA is determined using the methodology of SEMI Standard G38 – 87. To summarize, the package is built with a thermal test die which has resistors for heating the silicon die within the package and one or more diodes to measure the die temperature. A surface mount package is then soldered to a printed circuit board. Naturally, the size and amount of metallization on the board strongly influences the measured thermal performance. The test boards are designed with "minimum" metallization but with all the leads routed. The printed circuit board with the package is placed horizontally in either the wind tunnel for forced convection measurements or in a one cubic foot box for natural convection measurements. The test chip is used to heat the package and determine the die temperature within the package. This die temperature is the "junction" temperature. Then the junction to ambient thermal resistance is determined by

$$\theta_{JA} = \frac{(T_J - T_A)}{P}$$

where T_J is the die temperature, T_A is the ambient temperature, and P is the power dissipated within the package. The ambient temperature is measured below the printed circuit board, one half inch away from the edge of the board and one inch below the plane of the board. This location is a local ambient while avoiding measuring the air temperature after it has been heated by the package. Typically for the SOJ packages, one watt is used for the measurement. The measured value of Theta JA is not a strong function of the measurement power although the measured value will decrease slightly with increasing power. The slight decrease occurs because higher surface temperatures cause a more effective natural convection.

Measurements of test die have been taken on three memory packages for this report: 24 lead, 300 mil wide SOJ; 28 lead, 400 mil wide SOJ; and 52 lead PLCC. This data was used to "calibrate" the thermal simulation tool. After the simulations were completed, measurements were made on the 28 lead 300 mil wide SOJ to provide an error estimate.

With validation obtained from the experimental data, the simulation tool was used to calculate the thermal performance of the packages listed in Table 1. The simulations are expected to be within 20%. The range in thermal performance between the various devices in a given package are primarily a result of the different die and die paddle sizes.

Table 1. Thermal Resistances of Memory Packages

Lead Count	Pkg Width	Part Number	Theta JA, Natural, Measured	Theta JA, Natural, Simulated	Theta JA, 200 LFM, Measured	Theta JA, 200 LFM, Simulated	Theta JC, Measured	Theta JC, Simulated	Theta JA0, Natural, Simulated
36	400 mil	XCM6246WJ		54.06		39.86		5.06	15.61
36	400 mil	XCM67084WJ		57.69		43.35		7.65	21.11
32	400 mil	XCM6249WJ		55.58		40.28		4.23	14.14
32	400 mil	MCM6726WJ		60.48		45.02		7.72	21.55
32	400 mil	MCM6226AWJ		59.69		44.24		7.3	19.43
32	400 mil	Test Chip	56.5	55.53	39.7	40.22		4.25	14.46
32	400 mil	MCM6226BWJ		66.81		51.2		13.7	26.09
28	400 mil	MCM6229AWJ		67.36		49.73		6.8	18.72
28	400 mil	MCM6728WJ		68.34		50.54		7.35	21.41
28	400 mil	MCM6229BWJ		74.86		57.18		13.23	25.83
32	300 mil	MCM6206CJ		72.1		57.37		14.14	27.59
32	300 mil	MCM6206BJ		68.07		53.35		10.36	24.36
28	300 mil	MCM6206CJ		75.27		60.19		15.24	28.99
28	300 mil	MCM6264CJ		92.77		76.93		30.29	49.95
28	300 mil	MCM6229BJ		70.7		55.63		11.01	25.33
28	300 mil	MCM6706AJ		77.35		62.21		17.09	31.23
28	300 mil	Test Chip	65.1*	76.6	48.1	61.45	17.3	16.38	30.69
24	300 mil	MCM6708AJ		80.73		64.19		16.85	31.14
24	300 mil	MCM6290CJ		91.28		74.16		25.29	45.08
24	300 mil	Test Chip	69.7	72.7		56.4		9.95	23.16
52	PLCC	MCM67618FN		45.88		31.85		8.46	14.79
52	PLCC	Test Chip	45.5	50.24	33	35.47	15.4	11.96	18.96
44	PLCC	MCM62486FN		57.1		41.03		14.78	23.35

*Measured value on SOJ with pin 14 and pin 28 connected to "split" flag (die paddle). Simulated value for SOJ with standard flag.

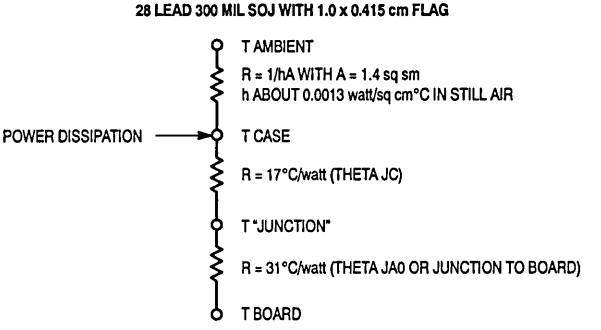
JUNCTION TO CASE THERMAL RESISTANCE

The junction to case thermal resistance, Theta JC or θ_{JC}, has been used in many different ways. The definition that is currently being used by the JEDEC 15.1 committee is the thermal resistance from the junction to the surface of the package. For the SOJ and PLCC package, that would be the thermal resistance from the junction to top surface of the package. Since heat sinks are rarely employed for SOJ packages, the junction to case thermal resistance is not normally used in determining the junction temperature. The enclosed table provides the simulated junction to case thermal resistance as determined by the simulation tool. The values obtained are not very accurate, but have sufficient accuracy in most circumstances. For a critical application, the junction to case thermal resistance should be measured.

Frequently, however, ThetaJC is used for the temperature difference (divided by total package power) between the junction and a thermocouple (or other temperature sensor) attached to top of the case. The JEDEC committee is recommending the nomenclature of *junction to reference* for the measurements relative to a thermocouple at the top of the package. Using the temperature on the top of the package in conjunction with the junction to reference thermal resistance is the best method to determine junction temperature in an actual use condition. In Natural Convection for the memory packages, we recommend using a value of Theta J-ref of 4°C/watt. In forced convection above 400 ft/minute, the recommended value of the Theta J-ref is Theta JC. These values will allow estimation of the junction temperature within 5°C for the normal range of applications provided that the thermocouple is 40 gauge or smaller and is applied correctly.

OVERALL PACKAGE THERMAL MODEL

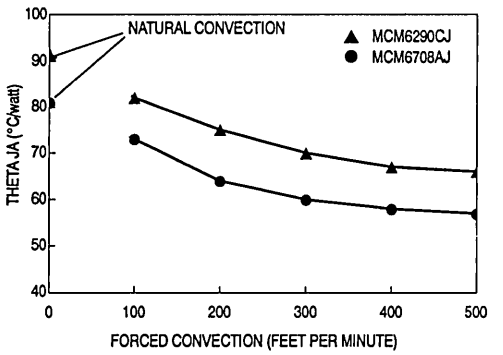
Theta JC is also used for a junction to lead thermal resistance occasionally. From an experimental point of view, it makes more sense to discuss the junction to board (printed circuit board) thermal resistance. The simulation software calculates a thermal resistance that is similar to the junction to board resistance: namely, θ_{JA0} that is defined to be the thermal resistance, with the printed circuit board held at ambient temperature. This is a close approximation of the junction to board thermal resistance since approximately 80% of the heat flows to the board in natural convection. These values can be used to construct a 1-D model of the thermal paths of the package as shown in Figure 1 below. This model can be used in the 2.5-D thermal model of the printed circuit application, if the spreading resistance of the board is treated correctly. Because the junction temperature is so closely coupled to the board temperature, determining the board temperature in the actual application is extremely important if the junction temperature is to be estimated.



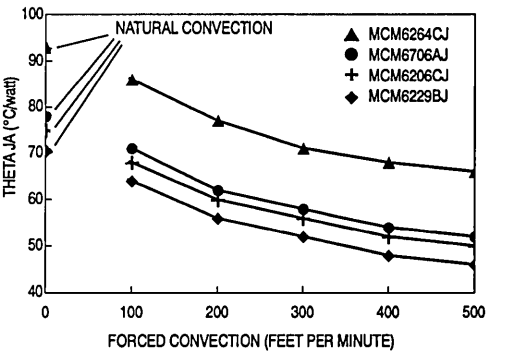
NOTE: Theta JA simulated in Natural Convection 77°C/watt.

Figure 1. One Dimensional Thermal Model

The thermal derating curves for Motorola's Fast Static RAMs are provided below. Although the data represents simulation results, there is a high level of confidence in the data points. In all cases, the manner in which the data is used could have a significant impact upon the validity of your thermal budget.

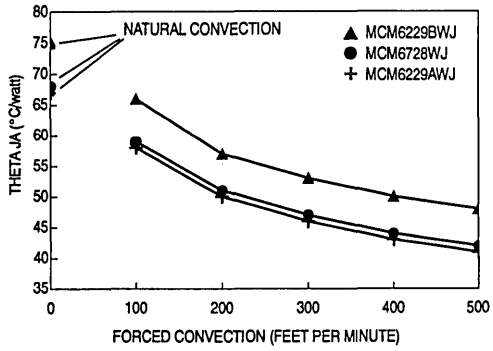


24 Lead SOJ, 300 mil, Copper Leadframe, Single Layer PCB Simulated Results

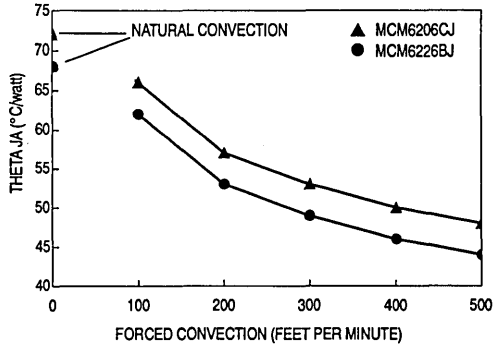


28 Lead SOJ, 300 mil, Copper Leadframe, Single Layer PCB Simulated Results

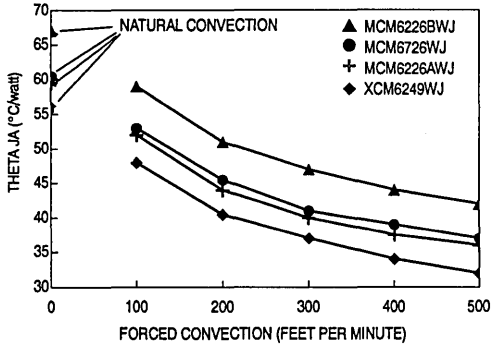
8



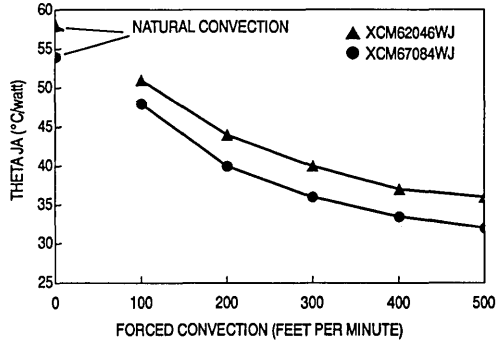
28 Lead SOJ, 400 mil, Copper Leadframe, Single Layer PCB Simulated Results



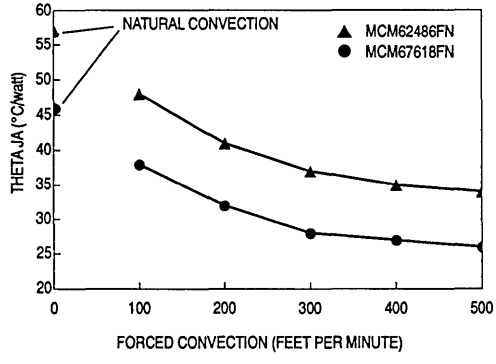
32 Lead SOJ, 300 mil, Copper Leadframe, Single Layer PCB Simulated Results



32 Lead SOJ, 400 mil, Copper Leadframe, Single Layer PCB Simulated Results



36 Lead SOJ, 400 mil, Copper Leadframe, Single Layer PCB Simulated Results



44 and 52 Lead PLCC, Copper Leadframe, Single Layer PCB Simulated Results

Avoiding Bus Contention in Fast Access RAM Designs

INTRODUCTION

When designing a bus oriented system, the possibility of bus contention must be taken into consideration. Bus contention occurs when two or more devices try to output opposite logic levels on the same common bus line.

This application note points out common causes of bus contention when designing with fast static random access memories and describes ways to eliminate or reduce contention.

WHAT CAUSES BUS CONTENTION?

The most common form of bus contention occurs when one device has not completely turned off (output in a high-impedance state) before another device is turned on (output active). Basically, contention is a timing overlap problem that results in large, transient current spikes. These large current spikes not only generate system noise, but can also affect the long term reliability of the devices on the bus (see Figure 1).

BUS CONTENTION AND FAST STATIC RAMs

Since memory devices are primarily used in bus oriented systems, care must be taken to avoid bus contention in memory designs. Fast static RAMs with common I/O data lines (or any high frequency device with common I/O pins) are the most likely candidates to encounter bus contention. This is due to the tight timing requirements that are needed to achieve high-speed operation. If timing control is not well maintained, bus contention will occur. The most common form of bus contention for memories occurs when switching from a read mode to a write mode or vice versa.

SWITCHING FROM A READ TO WRITE MODE

With $\overline{E}$ low (device selected), on the falling edge of $\overline{W}$ (write asserted) the RAM output driver begins to turn off (high-impedance state). Depending on the input and output logic levels, if sufficient time is not allowed for the output to fully turn off before an input driver turns on, bus contention will occur (see Figure 2a).

Figure 2a shows an example of a RAM trying to drive a bus line low while an input driver is trying to drive the line high. If the situation were reversed (RAM output high and the input driver low), bus contention would still exist.

Of course the obvious way to avoid this type of bus contention is to make sure that the input buffer is not enabled until the write low to output high-impedance (t_{WLQZ}) time is satisfied (see Figure 2b). This specification is usually given on most manufacturers' data sheets.

Another method to eliminate bus contention would be to use $\overline{E}$ to deselect the RAM before asserting $\overline{W}$ (low). This allows the RAM output extra time to go into high-impedance state before the input driver is enabled. $\overline{E}$ and $\overline{W}$ are later asserted low to begin a write cycle (see Figure 2c).

SWITCHING FROM A WRITE TO A READ MODE

With $\overline{E}$ set low (device selected), on the rising edge of $\overline{W}$ (write terminated) the address or data-in changes before the device has had a chance to terminate the write mode. If this should occur, and depending on the input and output logic levels, a bus contention situation could exist (see Figure 3). To avoid address changing type bus contention requires that the address not change till the write recovery specification (t_{WHAX}) is satisfied. To avoid bus contention caused by data changing requires that the data-in remains stable for the duration of the data hold specification (t_{WHDX}). Most of

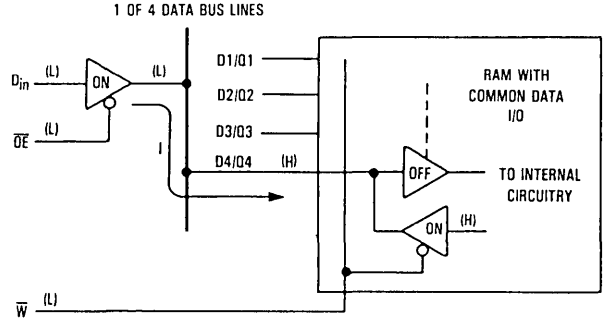


Figure 1. Common I/O Bus Contention

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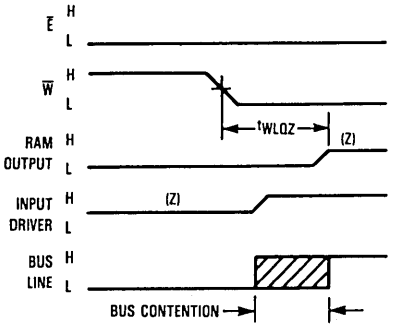

Figure 2a. Input Driver Enabled Prior to Disabling RAM Output

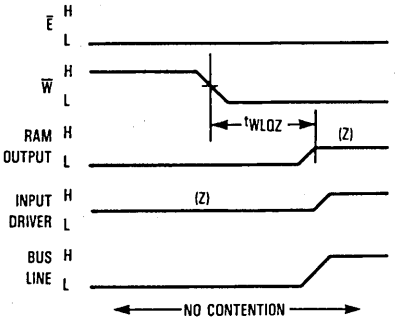

Figure 2b. Input Driver Disabled Prior to Enabling RAM Output

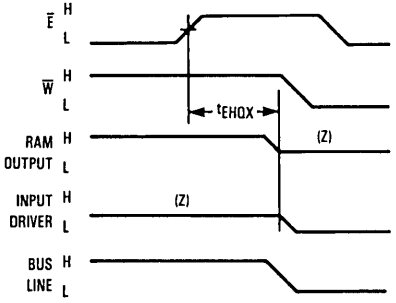

Figure 2c. Using $\overline{E}$ to Avoid Bus Contention

Motorola's fast static RAMs specify write recovery and data hold times of 0 ns. However, it is always a good practice to allow some margin to take care of possible race conditions.

Both of these types of contention could also be avoided by taking $\overline{E}$ high prior to taking $\overline{W}$ high. This will give the RAM output driver time to go to a high-impedance state before $\overline{W}$ goes high. In this case $\overline{E}$ is used to terminate the write cycle instead of $\overline{W}$ (see Figure 3c).

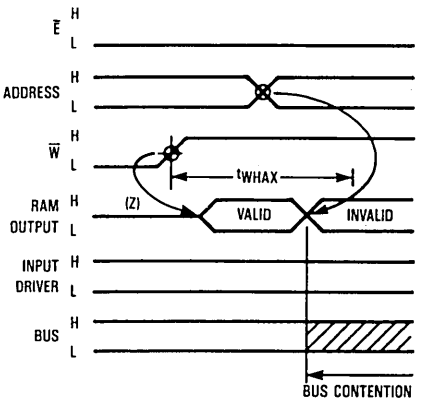

Figure 3a. Data Setup Time Violation

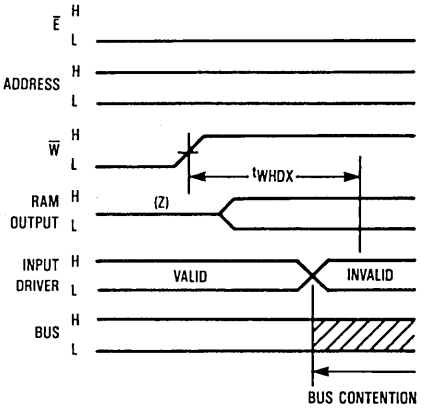

Figure 3b. Data Hold Time Violation

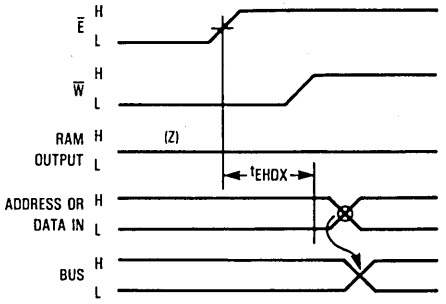

Figure 3c. Using $\overline{E}$ to Avoid Bus Contention

OTHER WAYS TO ELIMINATE BUS CONTENTION

If the RAM has an output enable pin ($\overline{G}$), synchronizing schemes can be incorporated to help eliminate bus contention. Taking $\overline{G}$ high will ensure that even when the RAM is in a read mode the output will be in a high-impedance state. This will allow the input driver to be enabled longer.

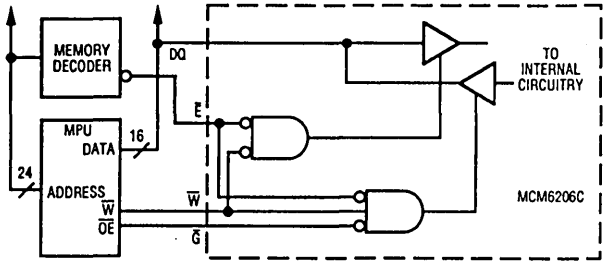

Figure 4a. Using $\overline{G}$ to Avoid Bus Contention

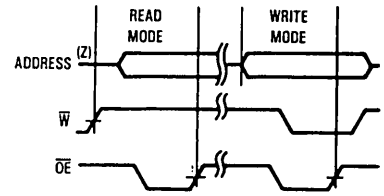

Figure 4b. Timing Diagram of MPU

Most advanced microprocessors have asynchronous bus-control signals that take advantage of fast memory devices with output enable pins. Figure 4 shows one way to avoid bus contention using a microprocessor interfaced to a Motorola 15-ns MCM6206C.

A more obvious way to eliminate bus contention is to use slow memory devices. Slow memories have loose timing requirements that allow devices to fully turn off before another device turns on. Of course this defeats the whole purpose of fast static memory devices.

Another obvious way to eliminate bus contention is to use memory devices that have separate data I/O pins. In this way the $\overline{W}$ signal from the microporcessor can control a buffer device to eliminate bus contention (see Figure 5). However, the industry is demanding RAM with common I/O because these devices cost less and save system real estate.

Common I/O devices reduce package size since fewer pins are needed. Smaller packages result in less PCB space requirement. Common I/O devices also eliminate the need for an extra buffer with its associated expense and space requirement. In general fast static RAMs configured greater than a X1 will have common data I/O pins.

Another popular way to reduce bus contention is to put a current limiting series resistor on each bus line (see Figure 6). The series resistor does not eliminate bus contention, but it helps reduce the large transient currents associated with bus contention. However, series resistors increase access time as well as increasing component count. The added access time depends on the total bus capacitance (including the capacitance of the devices on the bus) and the total bus resistance. The added delay should be added on to the point at which bus contention ceases. The following formulas can be used to determine the added access delay.

$$t_{HL} = R_L \cdot C_L \cdot \ln \frac{V_{in}(initial) - V_{in}(final)}{V_{IL}(max) - V_{in}(final)}$$

$$t_{LH} = R_L \cdot C_L \cdot \ln \frac{V_{in}(final) - V_{in}(initial)}{V_{in}(final) - V_{IH}(min)}$$

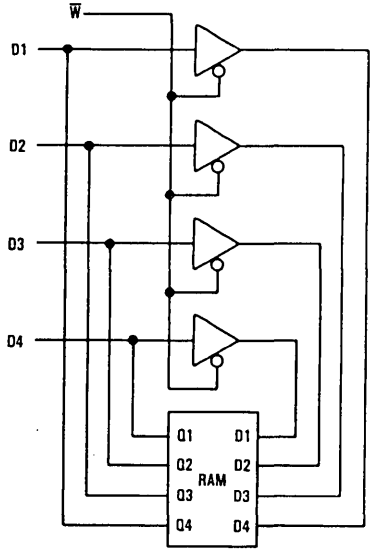

Figure 5. Separate I/O Buffer

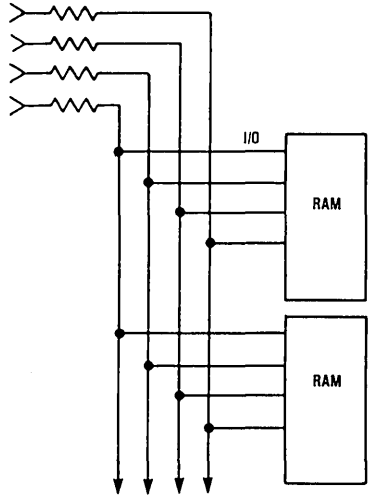

Figure 6. Using Series Terminating Resistors

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Generally the value of the resistor should be around 50 ohms. The larger the resistor the less the transient current generated, but the greater the delay. Using a 150-ohm resistor will limit the current flow to less than 20 milliamperes while adding approximately 3 nanoseconds extra access time. However, note that even the series resistors bus contention duty cycle must be minimized to reduce EMI and bus ringing.

Although it is very important to reduce bus contention, CMOS memories can tolerate more bus noise generated by bus contention than can bipolar memories, due to the excellent noise immunity advantage of CMOS over bipolar technology. However, even when using CMOS memories, large destructive transient currents generated by bus contention can still occur.

CONCLUSION

Bus contention must be taken into consideration in most bus-oriented system design. The occurrence of bus contention generates large transient currents that produce system noise and could also affect the system's long term reliability.

Fast random access memories with common data I/O pins are very susceptible to bus contention due to tight timing requirements. Although it is almost impossible to totally eliminate bus contention, it must be the goal of the system designer to minimize bus contention.

The Motorola BurstRAM™

Prepared by: James Garris

This note introduces the MCM62486 32K x 9 Synchronous BurstRAM. The device was designed to provide a high-performance, secondary cache for the Intel i486™ microprocessor and future microprocessors with burst protocol. Four of these devices can supply a 128K byte direct-mapped bursting cache with parity support.

THE MCM62486

The 62486 is a synchronous device with input registers and address counters surrounding a standard 32K x 9 FSRAM core. The additional circuitry in the periphery enables the memory to uniquely interface with the i486. Like the i486, the timings are referenced to the rising edge of the clock (K). Signals generated by the processor and control logic must be stable during all transitions of clock from low to high. Output enable ($\overline{G}$) on the 62486 is the only asynchronous input.

The 62486 contains three burst-control inputs. They are $\overline{ADV}$, $\overline{ADSC}$, and $\overline{ADSP}$. These inputs are used by the cache controller to control the burst capabilities of the 62486 and to maintain synchronization with the i486 or other logic driving the cache.

USE WITH THE i486 PROCESSOR

The 62486 requires an ASIC or discrete PAL type of cache controller to work with the i486. This cache control logic must also include 8K x 8 of cache-tag comparator RAM and any other buffers needed for system operation.

Control signals are sourced as follows: K is driven by the system clock (CLK); $\overline{ADSP}$ is an output from the microprocessor; and $\overline{ADV}$, $\overline{ADSC}$ are generated from the cache control logic. The data bus and lower address bus may interface directly with the 62486 or the address bus may be buffered to

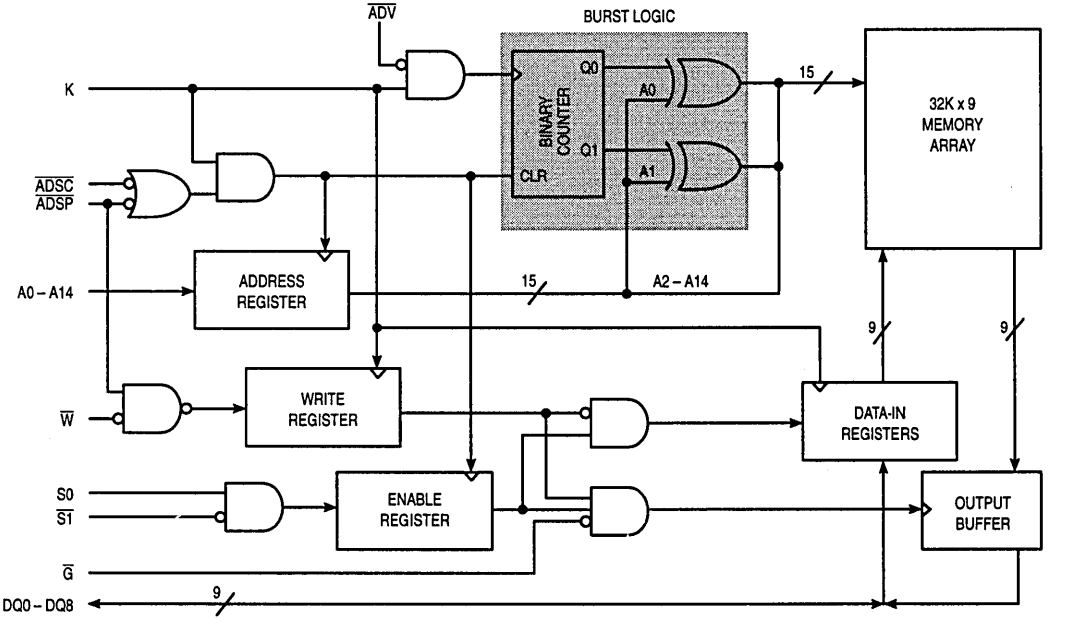


Figure 1. MCM62486 Block Diagram

BurstRAM is a trademark of Motorola, Inc.
i486 is a trademark of Intel Corp.

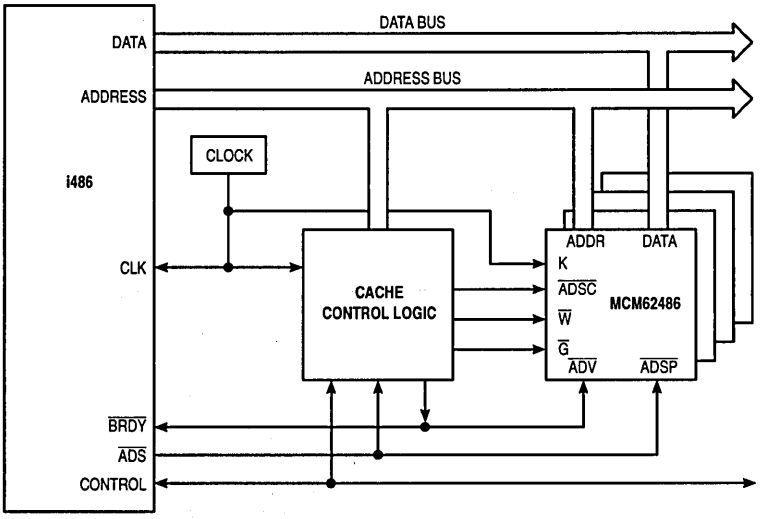


Figure 2. Typical System Block Diagram

improve its drive to the rest of the system. A simple block diagram of this setup is shown in Figure 2.

INPUT PINS OF THE MCM62486

K is the clock input of the 62486. This should be tied to the system clock.

$\overline{\text{ADSP}}$ is one of two address status input pins that are supplied on the 62486. This input allows the microprocessor to initiate a cache bus cycle. For every processor access, to or from memory, the i486 will assert $\overline{\text{ADS}}$ for one transition of K from low to high. If $\overline{\text{ADS}}$ from the i486 is tied to $\overline{\text{ADSP}}$ on the 62486, the 62486 will register the correct address from the processor. During all "T2" cycles on the i486, $\overline{\text{ADS}}$ and $\overline{\text{ADSP}}$ should not be asserted as described in the i486 processor user manual.

$\overline{\text{ADSC}}$ is the second of two address status input pins supplied on the 62486. This input allows external logic to initiate or continue cache bus cycles. The purpose of this input is to give the cache controller its own input to regulate cache accesses. This gives the 62486 a good deal of system design flexibility. One use of $\overline{\text{ADSC}}$ is for burst extension. After four burst accesses have been generated by the 62486, the cache controller may supply an additional base address to continue the burst. This method works well with 72 bit data buses. This pin can also be used in a similar manner to facilitate a cache fill from other sources.

$\overline{\text{ADV}}$ is the burst advance input pin supplied on the 62486. The purpose of this pin is to acknowledge a successful read-from or write-to memory as determined by the cache control logic. The 62486 may then proceed to the next address. This input is a function of T2 (T2 cycle as defined by the i486 processor manual), $\overline{\text{KEN}}$ (from the processor), $\overline{\text{MATCH}}$ (from the cache tags), $\overline{\text{READ}}$ (from the processor) and MISS (a cacheable read miss from the control logic).

$\overline{\text{W}}$ is the synchronous write input pin supplied on the 62486. This signal must be valid for every clock cycle $\overline{\text{ADSP}}$ is not asserted.

A0 – A14 are the synchronous address pins supplied on the 62486. These must be valid for the transitions of K from low to high. If neither $\overline{\text{ADSC}}$ or $\overline{\text{ADSP}}$ is negated, or if the chip is deselected, the address inputs do not need to meet the required setup/hold times. For all other read/write operations, the setup/hold times **MUST** be met.

S0 and $\overline{\text{S1}}$ are the synchronous chip selects supplied on the 62486. These must be valid whenever the addresses are required valid. These inputs can be used for address depth expansion without any external logic.

$\overline{\text{G}}$ is the asynchronous output enable supplied on the 62486. This pin changes the outputs from high impedance to active at any time that the SRAM is selected.

CACHE OPERATION

READ CYCLES

Cache operations of the 62486 are initiated with one of the two Address Status Pins mentioned. Figure 3 shows the read cycle timings when $\overline{\text{ADSP}}$ is tied to $\overline{\text{ADS}}$. During the first cycle (T1) the i486 supplies an address and asserts $\overline{\text{ADS}}$ low. The 62486 responds to $\overline{\text{ADSP}}$ being asserted by registering the lower 15 addresses. The 62486 begins to perform a read access regardless of the state of its $\overline{\text{W}}$ input.

During the next cycle (T2), the cache controller determines if the read access was a cache hit. If so, the controller should assert $\overline{\text{G}}$ and $\overline{\text{ADV}}$ on the 62486 as well as $\overline{\text{BRDY}}$ on the i486. The assertion of $\overline{\text{G}}$ will allow the 62486 to drive the data onto the data bus while $\overline{\text{BRDY}}$ will inform the processor that the data is correct. The assertion of $\overline{\text{ADV}}$ will cause the 62486 to begin on the next burst access. Subsequent burst access will be available without wait states in a similar fashion.

Single, non-burst reads behave in a similar manner as the first access of a read burst.

Note for timing diagrams: Q1, Q2, Q3, Q4 represent the data output from the first address (base address), second, third and fourth address. For example, if A in Figure 3 was #000C, Q1 would be the data from #000C, Q2 from #0008, Q3

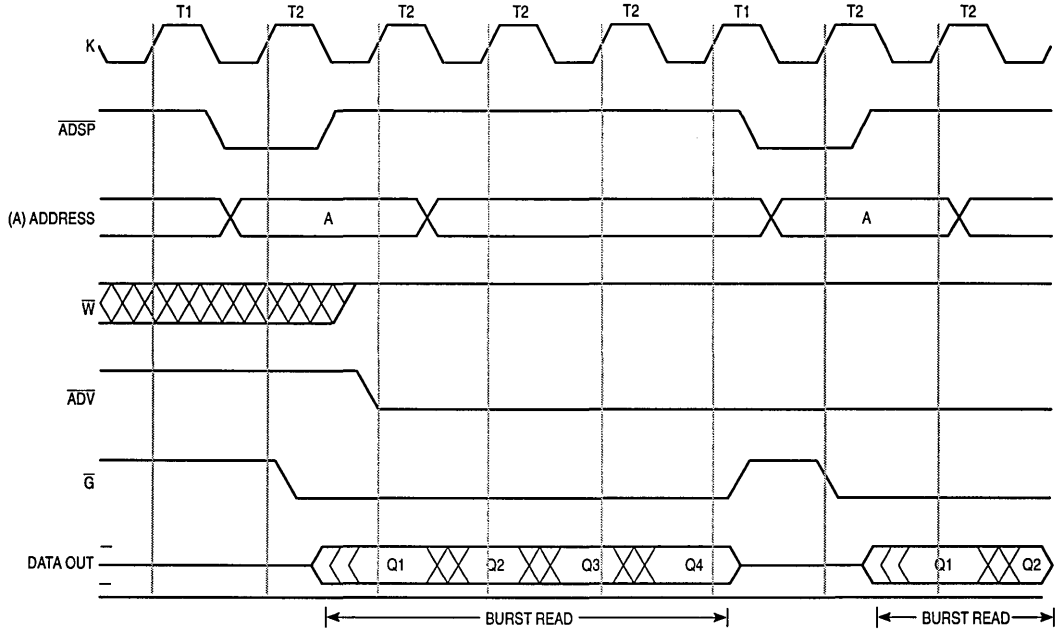


Figure 3. Cache Read Cycles

from #0004 and Q4 from #0000. (This is the same burst sequence as in **Table 7.7. Burst Order** in the *i486 Microprocessor Data Book*).

WRITE CYCLES

For a write to cache access, the initial T1 cycle will be the same as above. During the T2 cycle, the cache controller should assert $\overline{W}$ instead of $\overline{G}$. This will allow the 62486 to receive the data from the i486 and write it to memory. The i486 can burst write for 8 and 16 bit operations. The 62486 can support this action as described in the 62486 data sheet and Figure 4.

ADDRESS BUS LOADING

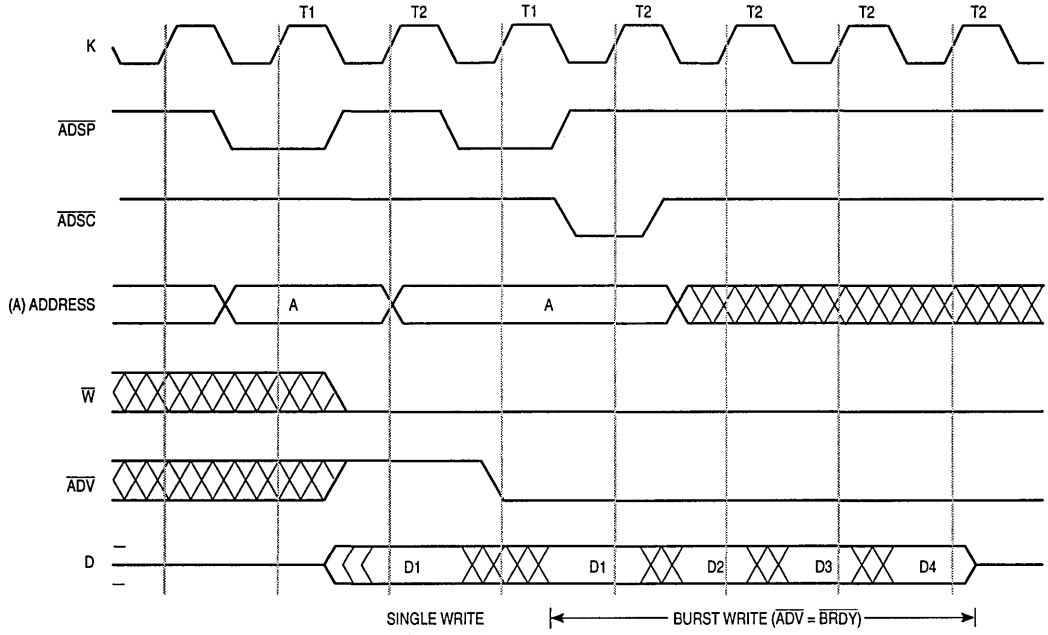
The 62486 has setup and hold timing that allow address buffers to be placed between the SRAM and the processor. The i486 is specified with 50 pF loads. Since the 62486 has a typical input capacitance of 2 pF, the i486 can be run without the buffer assuming the cache tags and other circuitry do not overload the bus.

ADVANTAGES OF THE 62486 OVER OTHER FSRAM SOLUTIONS

The 62486 is meant to replace a standard 32K x 9 FSRAM as well as some external logic. By incorporating this logic and RAM onto one chip, the system designer is given more board space, less power consumption, and most of all, easier design timing requirements. At 33 MHz, a discrete logic/SRAM solution would require a 7 ns PAL (for the burst counter) and an 18 ns SRAM [30 ns (period) – 5 ns (i486 setup) – 7 ns (PAL) = 18 ns].

This timing is even more difficult in write cycles. Closer examination of writes shows that the write signal and data from the processor do not correspond with the requirements of a standard 32K x 9 SRAM. A self-timed write SRAM is essential for high performance systems.

The 62486 represents the JEDEC standard for a 32K x 9 Synchronous SRAM for the i486. This pin-out provides enough power and ground pins to allow these devices to support systems running 50 MHz and faster. Also the 62486 represents the standard functionality descriptions for $\overline{ADSP}$, $\overline{ADSC}$, and $\overline{ADV}$. These same pins are used in the JEDEC standard 64K x 18 SRAM to be used with the i486 and the "P5".



NOTE: The first T1/T2 cycle is a single write operation. This works the same as the first two cycles of a burst write. In this single write operation, ADV goes high for the T2 cycle, while the RDY signals on the processor must be asserted low. In this operation, the ADV and RDY signals behave differently. To match their behavior, examine the second T1/T2 cycles. This second write operation (the burst write) shows how the ADV signal may behave like the RDY signals. Note that the ADSC is asserted for the first T2 cycle, thereby reloading the base address. Had the ADSC remained high for this cycle, the data (D1) would have been incorrectly written to the second burst address. This second write operation shows both single and burst write operations with ADV and RDY both asserted low for all T2 cycles.

Figure 4. Cache Write Cycles

A Protocol Specific Memory for Burstable Fast Cache Memory Applications

Prepared by: Ron Hanson

Cache memory design has evolved rapidly in recent years, taking full advantage of the specialized cache application specific fast static RAMs that are becoming increasingly available. These advanced designs are driven by several factors: faster processor clock rates, larger on-chip processor caches, larger and faster FSRAMs, more efficient processor bus protocols, and more efficient DRAM interfaces.

CACHE MEMORY DESIGN TRENDS

Six key trends can be observed in this evolution:

1. Larger caches to improved hit rates.
2. Faster caches to maintain the desired no-wait state response.
3. Dominance of direct-mapped cache designs over the number of multiple-way set associative cache designs.
4. Minimization of external cache control logic to increase speed.
5. Users are developing their own cache solutions, even though vendors are offering more and more integrated solutions.
6. An increasing use of Application Specific Memories (ASMs).

LARGER CACHES

The latest CISC and RISC processors all have ample amounts of no-wait state cache on-chip or included in the processor chip set. Frequently this cache responds a full clock cycle or more faster than an external memory cache could because it is connected to the processor's highly efficient internal bus. In the case of the MC68040, this is a full Harvard Bus architecture that is at least twice as efficient as the fastest external memory system.

The hit rates of these internal caches are very impressive too. The i486™ provides 8K bytes of on-chip four-way set associative cache as does the '040. Though a small amount of cache, these caches have read hit rates greater than 80%. In short, it takes a comparatively large external cache to improve on the performance of the processor alone and this trend will continue. However, FSRAMS are also getting larger. 256K bit FSRAMs are now in abundance and 1 Megabit FSRAMs are in production. As has always been the case with memories, these new larger FSRAMs will replace the older smaller ones at about the same price relative to their respective product life cycles. In other words, building a cache with the largest FSRAMs available today is no more expensive that building a cache three years ago with the largest FSRAMs available then.

FASTER CACHES

Processor speeds continue to increase and there is no end in sight. There are already 50 MHz production processors. Recently the processors have been designed to be more "cache friendly." Significant protocol improvements were implemented on the '040 versus the '030 and the i486 versus the i386. These include implementing synchronous protocols, adding burst addressing, and reducing the data input set-up times.

However, it still comes down to question of raw speed. Fortunately, the increase in density has also been accompanied by increases in FSRAM speed. Now RAMs with 12 ns access times are available to support the 50 MHz processors. It is increasingly apparent that greater integration will be needed to continue to support the fastest processors. The elimination of logic circuits from the critical cache speed path is being vigorously pursued today.

THE DOMINANCE OF DIRECT-MAPPED CACHE DESIGNS

It has been shown that for any given system, as the size of the external cache increases, the performance advantage of a multiple way set associative cache over a direct mapped cache quickly fades to insignificance.[1] Furthermore, a multiple way set associative cache is always more complex to implement.[2] In a discrete design, this translates to either more cost or a loss in response time, which erodes any performance advantage that might be gained. For an integrated solution, it means relying on a vendor for a purchased proprietary solution. Often, if more performance is sought, it is far simpler and less expensive to just enlarge the cache rather than build in multiple way set associativity.

BurstRAM is a trademark of Motorola, Inc.
i486 and Pentium are trademarks of Intel Corp.
PowerPC is a trademark of IBM Corp.

[1] Jeff Leonard, "Clever Cache Designs Required to Pace High-Speed RISCs," *EE Times*, March 19, 1990, pp. 56, 68 – 69.
[2] Mark D. Hill, "A Case for Direct-Mapped Caches," *IEEE*, December 1988, pp. 25 – 40.

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MINIMIZATION OF EXTERNAL LOGIC

This point differs from the comment made on the elimination of logic circuits though integration. The Cache Tag RAM is a good example of integration that eliminated the need for a discrete comparator logic device. This did not minimize the logic required. Synchronous or self timed RAMs accomplish this by greatly reducing the complex logic required during write cycles. This is only the beginning; new protocol-specific memories are on the way that will take their cues from the processor itself and perform the needed RAM functions.

USERS ARE DEVELOPING THEIR OWN SOLUTIONS

There are many reasons why computer companies from the lowest performance to the highest are developing their own circuits rather than purchasing the ready-made solutions. One is competitive pressures. PC manufacturers using the same processor, coprocessor, mass storage devices, etc., must find a way to differentiate their products. They can do this by designing their own circuits. Another reason is value added. Many of these companies desire to develop their own chip technology to increase their own share of the revenue received for each computer.

Nevertheless, there is still a high demand for standardized memories. The sheer volume a memory can generate if it is adopted as a standard will drive its cost down far below what an individual custom memory could accomplish. Thus, though cache designs are using more specialty ICs, they still rely on multi-sourced high volume memories for cache data storage.

USE OF APPLICATION SPECIFIC MEMORIES

Referring back to the problem of supporting the very fastest processors, it is clear that the cache designer must attack this problem on all fronts. What is needed is a smart flexible, integrated, high density, very fast SRAM. Such products do exist, and the following is a description of one of the latest under development by several vendors that combines all of these features.

THE SYNCHRONOUS BURST PROTOCOL

In an effort to overcome the limitations of memory bus bandwidth, many of the high performance microprocessors have implemented burst memory protocols. Rather than transferring a single memory word per bus cycle, the microprocessor will transfer (burst) several consecutive memory words in quick succession. The number of words transferred corresponds to the length of a line in the microprocessor's internal cache. Burst transfers have been shown to greatly improve bus utilization. The MC68030, MC68040, PowerPC™, i486, Pentium™, MC88200, and AM29000 all employ burst memory transfers of one type or another.

Though the on-chip cache(s) can be very effective, system performance frequently can be improved by the addition of a secondary cache memory external to the microprocessor. There are three good possible reasons to add a secondary cache: 1) in multiprocessing systems, the time spent arbitrating for control of a global bus can severely degrade performance; 2) the system bus may run at a significantly slower rate than the microprocessor bus; and 3) the nature of the code itself may be better suited for larger caches than are available on-chip.

Burst protocols provide a new challenge for system designers. To achieve no wait state performance, it is necessary for the cache to count through the burst sequence. This in turn creates a problem during cache update cycles when wait states must be added to account for slower DRAM access times. Clearly, the designer would benefit from the integration of as much of this logic as possible onto the FSRAM. This reduces chip count and eliminates the propagation delay from discrete devices. Furthermore, by using inputs directly from the processor, it is possible to actually minimize the amount of logic required to manage the burst cycle. The inclusion of this logic creates an FSRAM that is not only processor specific, but protocol specific as well.

THE 32K x 9 SYNCHRONOUS BURST FSRAM

Not surprisingly, the original specification proposal for this burst FSRAM came from a user, Compaq Computer (Houston, Texas). It is a Synchronous FSRAM with an on-chip burst counter (see Figure 1) and special logic that enables the RAM to interface directly to the i486 processor as well as a cache controller. This device is being developed by several vendors for the i486 market.

The device is similar to existing synchronous FSRAMs in the market today. All of the address and control signal inputs to the RAM are held in registers on the chip, which are triggered by the rising edge the clock input (K) or the clock input gated by another input signal. These other signals include the $\overline{\text{ADSP}}$ and $\overline{\text{ADSC}}$ signals that qualify the address input.

The burst counter on chip is designed to count in the sequence used by the i486; however, the on chip count avoids the wait state inserted by the i486 at the beginning of a burst read cycle, thus improving cache performance. The $\overline{\text{ADV}}$ signal advances the counter of the rising edge of the clock, prior to the next memory access. The device uses a data input register to clock in the data on write cycles. Writes to the RAM are self-timed, requiring the minimal amount of control logic.

This FSRAM has a special built in wait state on write cycles (see Figure 2). This conforms with the i486 write timing. Furthermore, the RAM only advances its internal counter when told to by the controller, which is simultaneously acknowledging the previous transfer to the processor. The RAM can insert wait states whenever needed and, more importantly, it can hold address and count and switch from read to write mode in the event that a cache read miss occurs.

The real value of the BurstRAM™ is its simple processor interface (see Figures 3 and 4). The on-chip Address Register is controlled by the clock input and the processor's valid address signal. Thus, the RAM only registers the address when told to by the processor.

Using inputs from users on Motorola's MC68040 microprocessor, a similar device for '040 has been developed. This version, the MCM62940A, can also interface with the MPC601 (PowerPC™), MC88200 and AM29000 RISC processors.

This version of the BurstRAM naturally has a modulo four burst counter to stay in step with the '040 and MPC601. No-wait state Write Burst Cycles at very high clock rates are attainable on both '040 and PowerPC platforms.

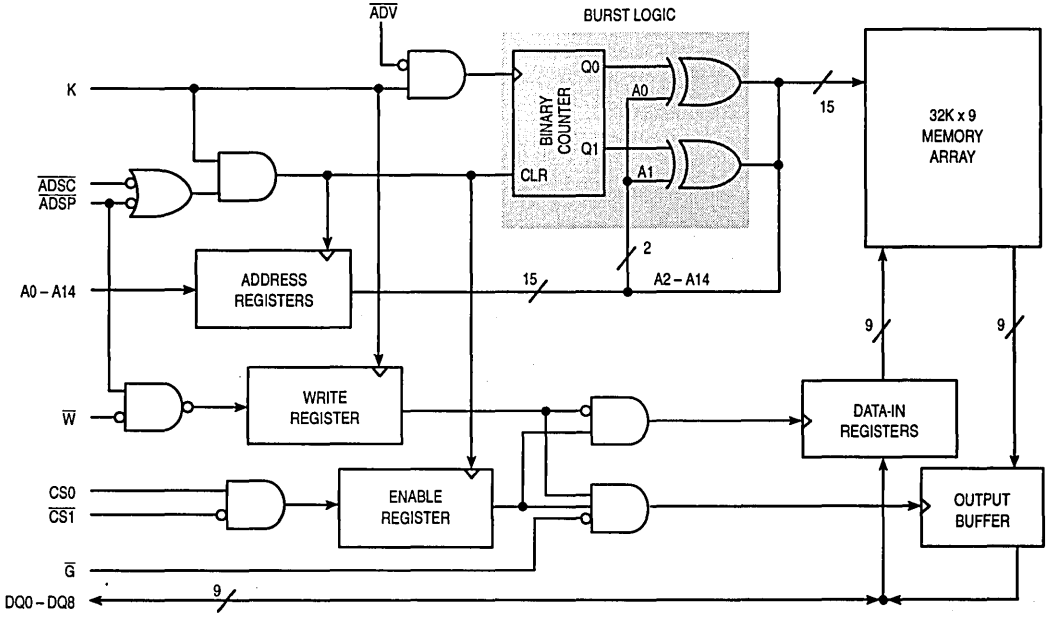

Figure 1. MCM62486A 32K x 9 BurstRAM Block Diagram

The removal of the wait state from the beginning of the write cycle actually simplifies the control logic since the conditions under which the BurstRAMs internal counter is advanced are now identical for both read and write cycles.

The conditional registering of the address input is especially useful when interfacing to a processor with multiplexed address and data buses such as the MC88200 or shared address buses such as the AM29000.

Burst FSRAMs are not a new concept; when the '030 first introduced the burst protocol in a microprocessor environment, a burst protocol FSRAM specification was developed. Unfortunately, the timing constraints of the '030 placed the performance goals of the FSRAM beyond the technology available at the time. The only way to build a no-wait state cache at the higher speeds was to utilize the bus retry cycle to rerun any memory access in the event of a cache miss.[3] To the RAM, this meant having to count backwards in the event of a cache miss and adding pins and logic to control this adjustment. Furthermore, the 15 ns access times needed were not feasible at the time.

THE FUTURE DIRECTION OF PROTOCOL SPECIFIC FSRAMs

Clearly, with the technology being developed today, it will be quite feasible to fully integrate all of the elements of the cache (data storage, address tag storage, and control logic) onto one chip. This will be the least cost approach, and if offered by a vendor, it will represent the least amount of user design resources. However, this approach will severely limit cache options and product differentiation. Furthermore, this approach will never perform as well as on-chip caches, which are growing in size. Thus, discrete FSRAMs of some kind will continue to be used in cache memory design.

Protocol Specific FSRAMs will increase in usage, but they will not completely replace standard products if for no other reasons than the versatility advantage of a standard device and its smaller packages. The densities of both will have to increase, though it appears that wider RAMs will be preferred for the new designs.

[3] Richard Crisp, Brian Branson, and Ron Hanson, "Designing a Cache for a Fast Processor," *Electronic Design*, October 13, 1988, pp. 111 – 118.

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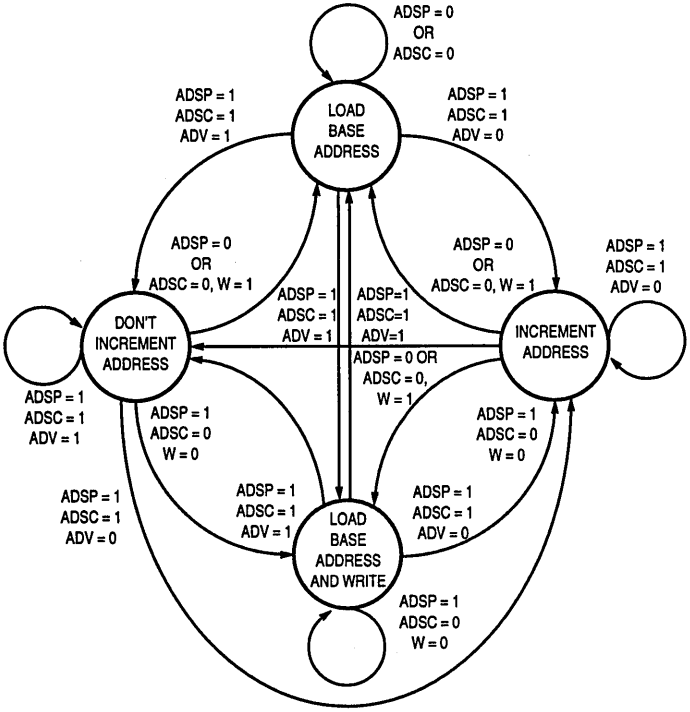

Figure 2. State Diagram for Address Determination on the MCM62486A BurstRAM

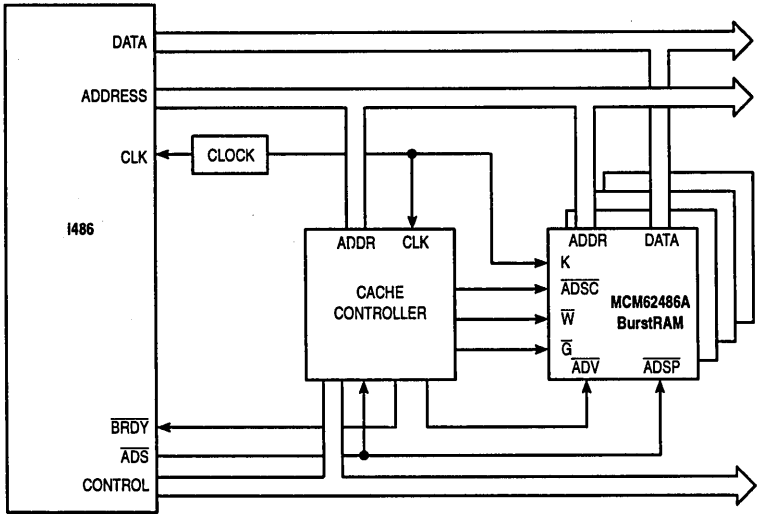

Figure 3. I486 128K Byte Burstable Cache Memory Block Diagram

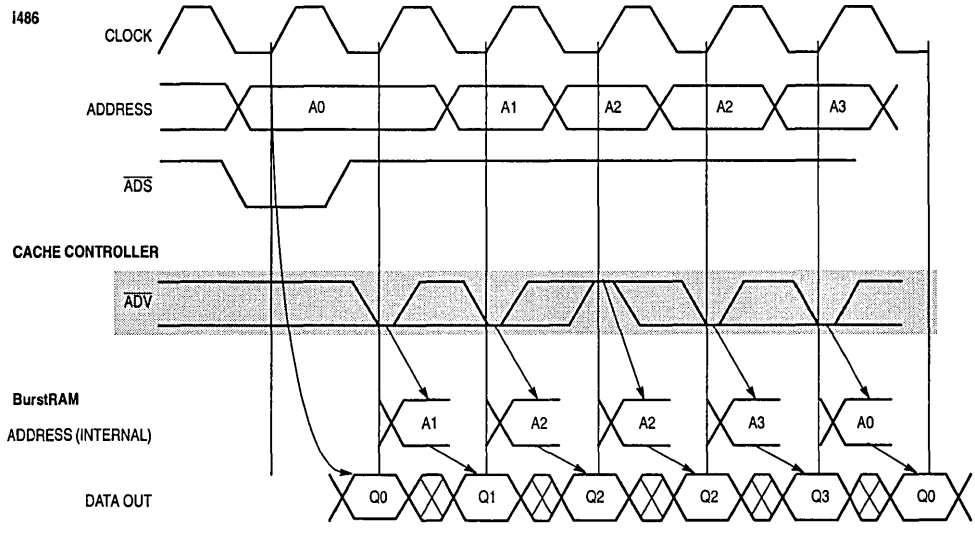

Figure 4. Timing Example of a 2/1/2/1 Burst Read

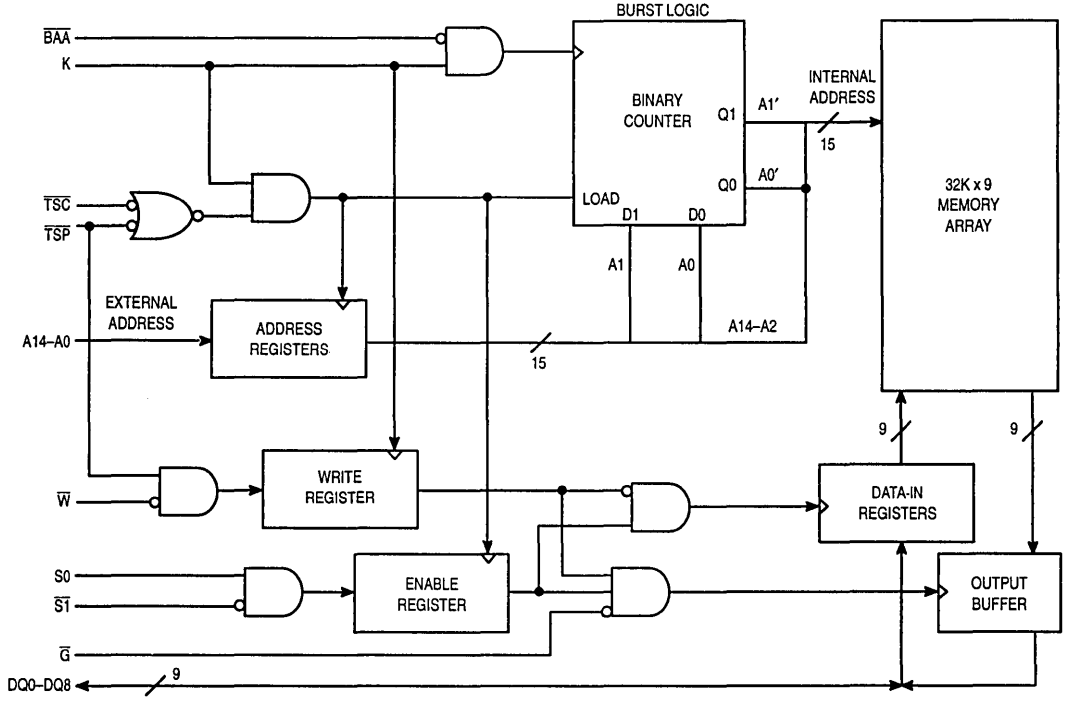

Figure 5. MCM62940A 32K x 9 BurstRAM Block Diagram

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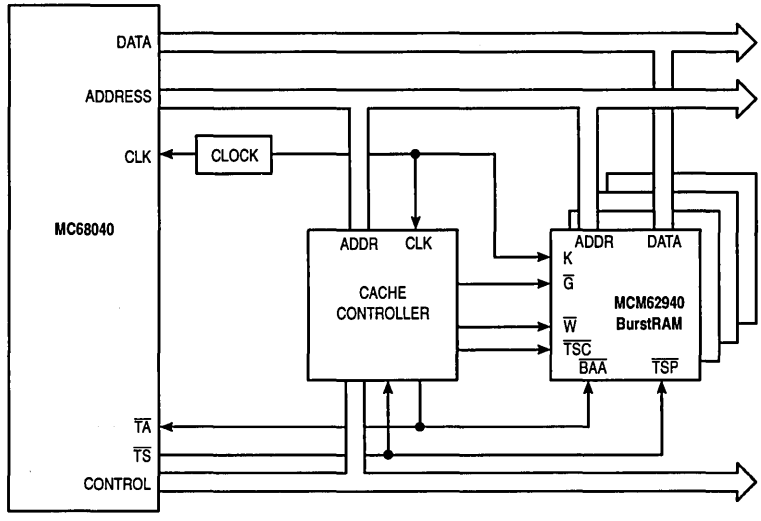

Figure 6. MC68040 128K Byte Burstable Cache Memory Block Diagram

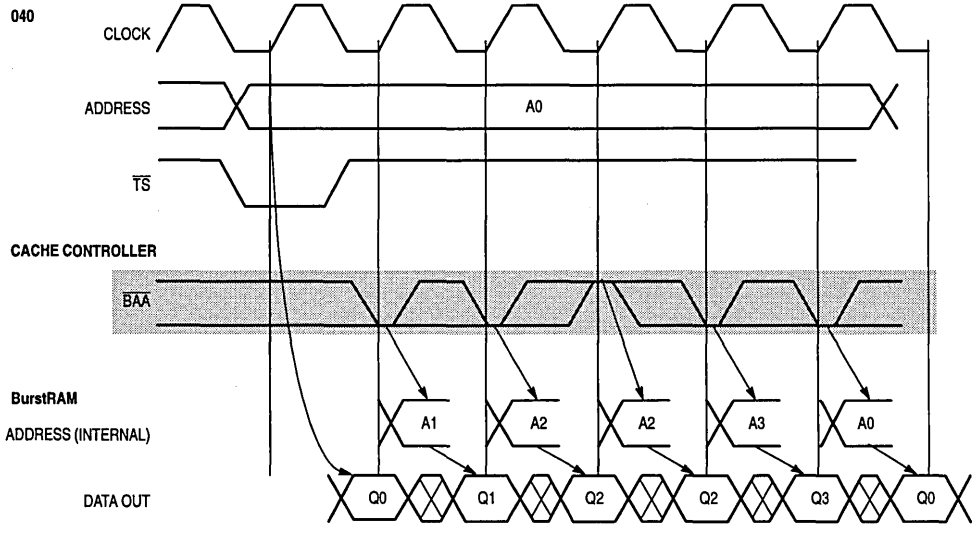

Figure 7. Timing Example of a 2/1/2/1 Burst Read

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A Zero Wait State Secondary Cache for Intel's Pentium™

Prepared by: Michael Peters, FSRAM Applications Engineer

Due to the increased complexity and sheer memory size requirements of new and forthcoming operating systems (OS), graphical user interfaces (GUI) and application programs, the demand for ever-increasing performance from the desktop machine continues. Next generation machines require more and faster memory. Microsoft's Windows NT™, for instance, will most likely need 12 to 16 MBytes of main memory. Cache size requirements follow accordingly. And Intel's new Pentium CPU has been introduced with external bus speeds of 60 MHz and 66 MHz.

High performance memory is essential in achieving Pentium's full potential. First level (L1), on-chip cache memory hit rates will suffer as a result of users' migration away from DOS to Windows to Windows NT. It has been shown that L1 cache hit rates decrease mainly due to the increased number and types of references demanded by the newer OS.[1] The CPU designer can only afford relatively small increases in L1 cache size in an effort to keep chip size down. So, second level (L2) cache must make up for the lack of an appropriately sized cache and significantly help to avoid time consuming DRAM accesses. In addition, at 60/66 MHz bus speeds, the L2 cache must be capable of reading and writing data fast enough for Pentium's superscalar design.

Motorola's new families of 64Kx18 and 32Kx18 Fast SRAMs establish a new standard in providing a big enough and fast enough data cache for Pentium designs. These families include five synchronous and two asynchronous devices in each family. All x18 SRAMs feature byte-write capability, 3.3 V I/O compatibility, and asynchronous output enable control. A zero wait state solution is possible using four MCM67B618 (or four MCM67B518) BurstRAMs™. The objective of this note is to explain some of the system level, electrical, and timing issues associated with the design of a zero wait state secondary cache.

BurstRAMs vs. ASYNCHRONOUS SRAMs

Although the i486™ and Pentium CPUs support a burst cache line fill protocol, in most cases building a zero wait state bursting cache with a single bank of ordinary SRAMs is simply not practical. Virtually all cache controllers/chipsets designed to work with the i486 accommodate the burst protocol by using an interleaved scheme of two banks of standard asynchronous SRAMs. The speed requirements for this type of caching arrangement allow the use of 20 ns through 35 ns SRAMs. These speeds accommodate 20 through 33 MHz i486 machines, the bulk of today's IBM-compatible PC market. For the i486's 32-bit bus speeds less than 50 MHz, this hook-up is technically feasible, but somewhat expensive and physically large, and it consumes a good deal of power since as many as eight SRAMs are required. However, Pentium's 64-bit bus and bus cycle rates of 60 MHz and faster only exacerbate the difficulties with single and double bank caches using ordinary asynchronous SRAMs. Most chipset vendors will find that the use of synchronous burstable SRAMs will be the only practical zero wait state solution for Pentium.

A single bank scheme must use either extremely fast RAMs (< 7 ns for a 60 MHz bus) or add wait states. With the added wait states, a single bank 3-2-2-2 (three lead-off clock cycles and two clock cycles for each subsequent read) design might still require 12 ns standard SRAMs.

A double bank scheme can be designed with wait states or for high speed with no wait states. Figure 1 shows the timing for a 3-2-2-2 design using sixteen 15 ns 32Kx8 (or x9) SRAMs in a two bank design.

The cache can be expected to consume about 8.6 W. Two banks of 12 ns standard 32Kx8 (or x9) BiCMOS SRAMs might achieve 3-1-1-1 burst, but at an even greater power premium — nearly 12 W. In two bank schemes, even when one bank is de-selected, it will still draw about 65% of the full operating current.

Double bank designs present other issues that must be considered, including address and data bus loading, physical layout, and socketing devices. Two banks of 32Kx8s will present an 80 pF load (plus routing) to the cache controller's address bus. These heavily loaded lines represent additional signal delay and power dissipation compared to a BurstRAM design. And, one cannot afford a 5 ns buffer delay in the address path. When comparing the BurstRAM's 52-lead PLCC package with a standard 32Kx9 SOJ, direct mounting of these devices on a board will yield roughly four square inches versus eight square inches, respectively. Socketing the SRAMs is ill advised since access time will be pushed out, and signal integrity may be compromised.

Although designing caches with asynchronous SRAMs can be done, the control signal timing is far from easy. Of all timing concerns, write pulse generation may be the biggest issue. Burst writes may be next to impossible to perform since both edges of the write pulse must be positioned precisely to accommodate address set-up and data hold times. One can expect 10 ns minimum write pulse widths for 12 ns asynchronous SRAMs; this does not leave much time for the 15 ns cycle processor bus.

Motorola has developed a series of 256Kbit, 512Kbit, and 1Mbit SRAMs, known collectively as BurstRAMs, to solve these problems.[2]

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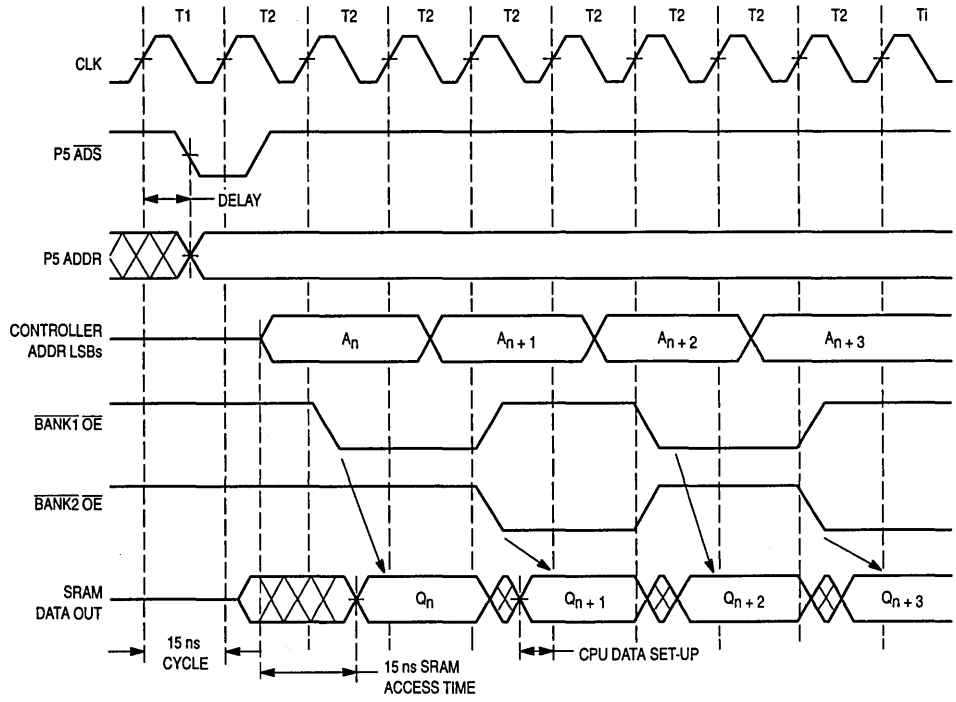


Figure 1. Two Bank Asynchronous SRAMs Performing 3-2-2-2 Burst READ

The MCM62486, a 32Kx9 BurstRAM, was developed for i486 systems. These BurstRAMs are being used in many of the 50 MHz i486 systems built today. The MCM67518, a 32Kx18 device, and the MCM67618, a 64Kx18 device, are the best suited for Pentium-based designs. Key to the success of a zero wait solution is the SRAM's support of Intel's burst protocol. A 2-1-1-1 (zero wait state) burst read cycle can be performed at cycle times of 20 ns and less. Pipelined addressing can further reduce a burst cycle to a 1-1-1-1 count. The MCM67B618 and MCM67B518 are synchronous BiCMOS SRAMs that feature wide x18 data paths, burst reading and writing, byte-write capability, 3.3 V I/O compatibility, and asynchronous output enable control. Note that all BurstRAM operations occur on the rising edge of clock (CLK).

Four (4) MCM67618 devices provide a single bank of 512K byte L2 cache. The interface to the Pentium chip is a direct connection for address and data paths. These new BurstRAMs (MCM67B518, MCM67B618) have been designed to operate at clock rates of up to 66 MHz (15 ns cycle time). They are available in access times of 9/12/18 ns with cycle times of 15/20/30 ns, respectively. The term "access time" is used loosely for synchronous SRAMs and is more accurately, CLK-to-VALID DATA time.

WHAT IS A BurstRAM™ ?

BurstRAMs are synchronous SRAMs that contain input registers for address, write, and enable signals and have an on-chip burst counter that imitates the i486 and Pentium's lower order address burst count. These control signals are registered into the BurstRAM on the rising edge of the CLK input. Three (3) control pins allow complete control of the burst function. $\overline{ADSP}$ (ADS Processor), $\overline{ADSC}$ (ADS Controller), and $\overline{ADV}$ (ADVance) control the burst read/write functions as well as single read/writes. A self-timed write is also provided for the purpose of simpler (and relaxed) write timing. Byte-write capability is provided with the $\overline{UW}$ and $\overline{LW}$ (Upper/Lower byte Write) signals. Note that all control signals are active low. See Figure 2.

THE BURST CYCLE

A burst read cycle is performed as follows (see Figure 3):

1. During the first cycle (T1), the CPU generates ADS and a valid address, and the BurstRAMs register the external address A<18:3> and enable on the rising edge of the system clock (CLK). This address can be considered the base address from which the BurstRAM begins its address counting,

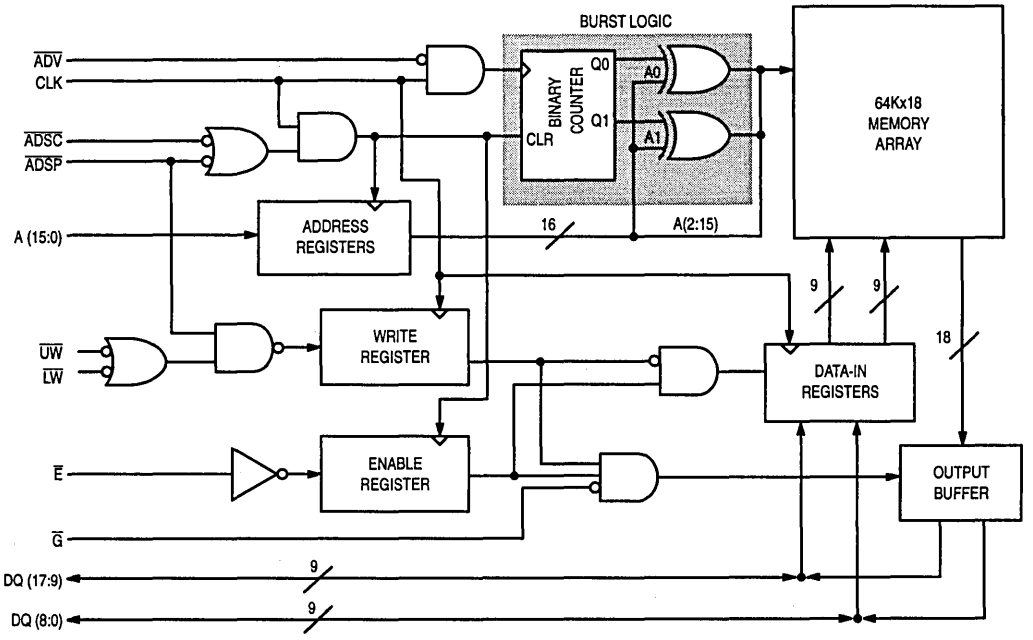


Figure 2. Block Diagram of 64Kx18 BurstRAM

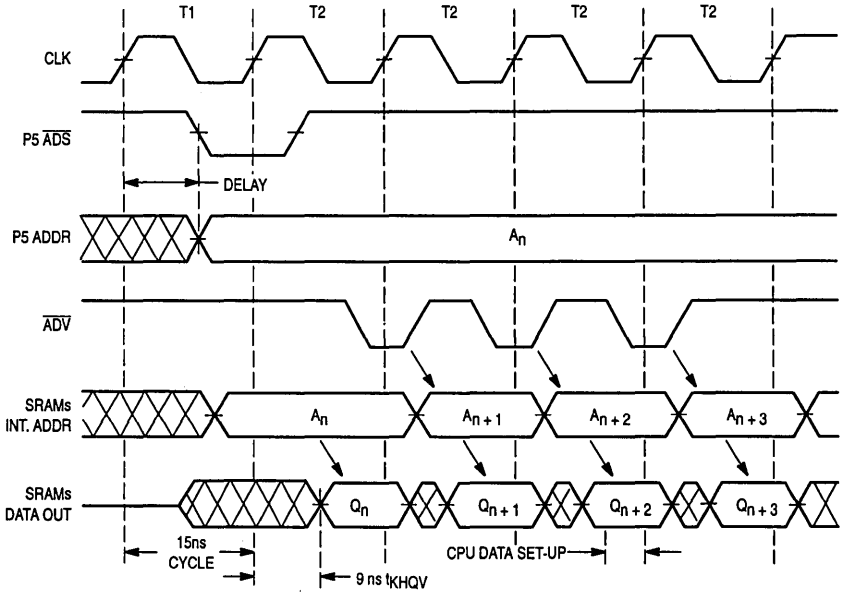


Figure 3. 64Kx18 BurstRAM Performing 2-1-1-1 Burst READ

2. Assuming the cache controller has determined that the cycle is a cache hit, the first 8 bytes of valid data are driven onto the data bus 9 ns after the second rising clock edge,
3. Subsequent cycles present valid data upon the negation of $\overline{ADS}$ and the assertion of $\overline{ADV}$. An entire 32 byte cache line can be supplied to the CPU in just five cycles. The BurstRAM's output enable ($\overline{G}$) can be asserted well into the 2nd cycle since it is asynchronous and represents only 5 ns delay.

Pentium operates with external bus speeds of 60 MHz and 66 MHz. This corresponds to 16.6 ns and 15 ns cycle times, respectively. Standard asynchronous SRAMs are hard pressed for a zero-wait state application. A look at the timing reveals that sub-12 ns SRAMs would be required since Pentium's data set-up time is about 3 to 4 ns. The inclusion of on-chip logic allows the BurstRAM to be directly connected to the CPU, and avoids the timing penalty associated with glue logic.

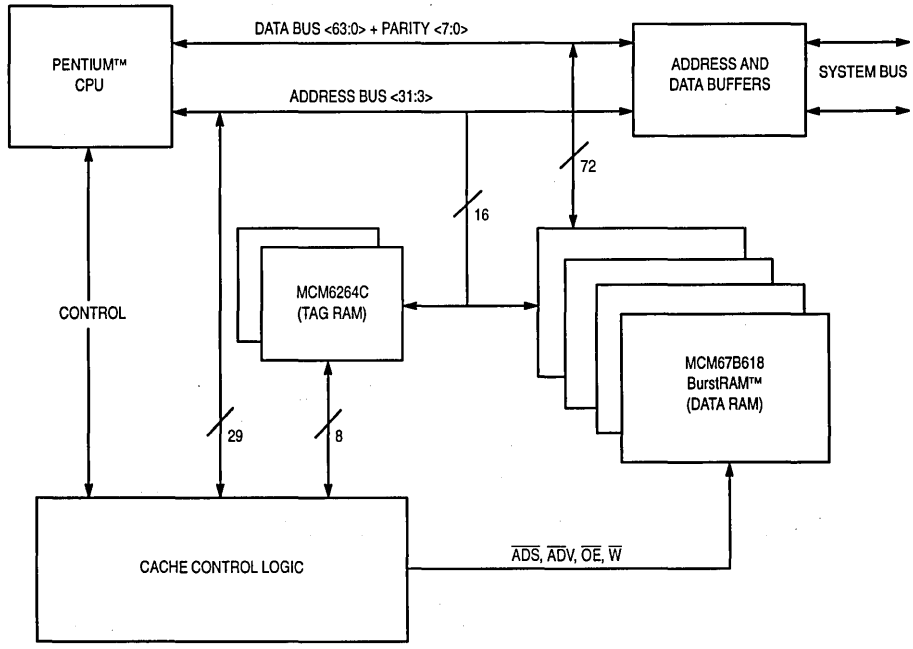
Using the BurstRAM, a zero wait state burst write cycle can be performed as well. Upon the CPU's assertion of $\overline{ADS}$, the BurstRAM begins and completes a burst write cycle with the assertion of $\overline{E}$, $\overline{LW}$, $\overline{UW}$, and $\overline{ADV}$ signals. A burst write cycle can be started using either $\overline{ADSP}$ or $\overline{ADSC}$. If $\overline{ADSC}$ is sampled low (while $\overline{ADSP}$ is high), data can be written immediately to the BurstRAM while $\overline{ADV}$ is asserted on subsequent cycles for the completion of the burst cycle. If $\overline{ADSP}$ is sampled low (while $\overline{ADSC}$ is high), the write register is blocked inside the BurstRAM and consequently only allows A<15:0> and $\overline{E}$ to be registered. On the following cycle ($\overline{ADSP}$ and $\overline{ADSC}$ negated), the burst write operation begins assuming $\overline{LW}$ and $\overline{UW}$ have been asserted. Again, $\overline{ADV}$ must be asserted on subsequent cycles to complete the burst cycle.

The use of a synchronous SRAM makes a design simpler in the sense that address and control signals can have looser timing constraints since they are registered in, and the SRAM does the rest. As long as DQ<17:0>, $\overline{LW}$, and $\overline{UW}$ signals comply with the required set-up (2.5 ns) and hold (0.5 ns) times, complex off-chip write pulse generation can be eliminated. An undue burden will be placed on the controller to provide proper write pulse width and write timing edges relative to address and the CPU's valid data.

SYSTEM CONFIGURATIONS

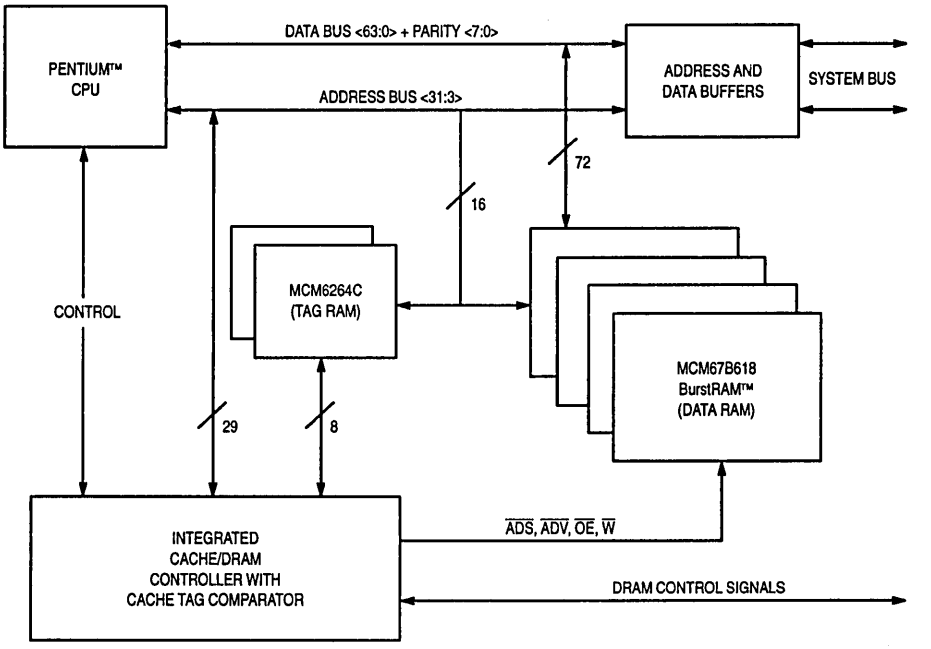
Pentium's 64-bit data path will require four (4) MCM67B618s (or MCM67B518s) to provide a single bank 512K (256K) byte L2 cache. The interface to the Pentium chip is a direct connection for address and data paths. Control signals must come from the cache controller. See Configurations A/B/C of the System Block Diagrams.

Configuration A is the least integrated solution, one that uses external tag RAM and a PAL or ASIC for the cache controller. The DRAM controller would be yet another component in the system.



Configuration A
Secondary Cache Solution for Pentium — 512KByte

Configurations B and C are the most likely approaches taken by chipset vendors in which the tag RAM may or may not be integrated, but will probably integrate the DRAM control. For direct-mapped caches such as these, tag RAM size depends on the controller's mapping of tags (or sectors) to cache lines. Each sector may consist of 1, 2, 4, or more cache lines. Tag RAM depth is then 16K, 8K, 4K, or so, respectively.



Configuration B
Secondary Cache Solution for Pentium — 512KByte

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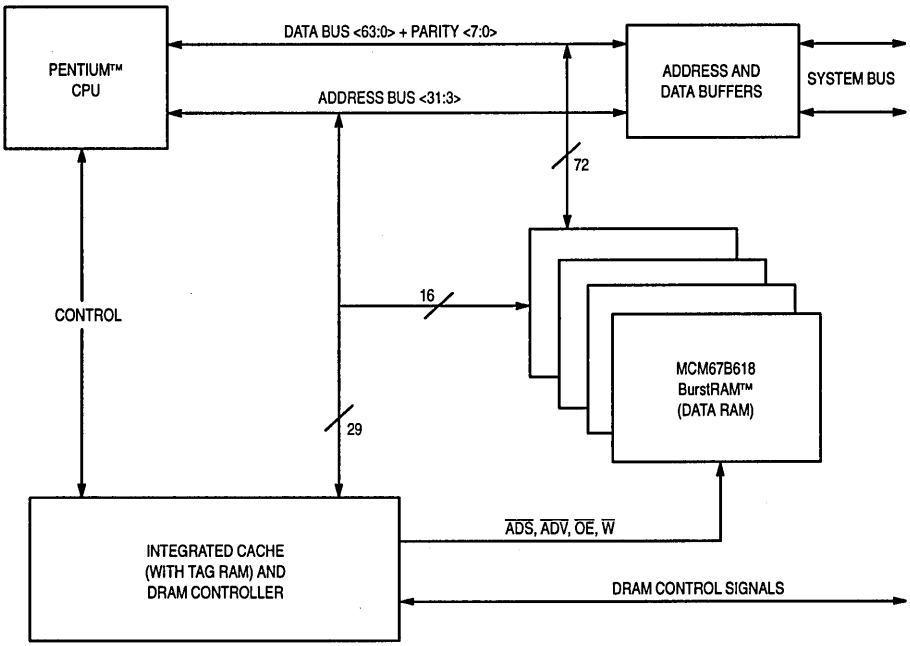
The tag RAM must be at least 10 ns for zero wait state performance; otherwise, a lead-off wait state must be added (3-1-1-1). This is determined by the speed of the controller's tag comparison as well. If the cache line size is 32 bytes and the data RAM depth is 64K, the tag RAM will have to be a 16Kx8/10 or 4Kx8/10 organization. The tag RAM's width (data path) is a function of the system's main memory size. An 8-bit tag will allow a cache size of 512KB to cache 128MB of main memory.



Configuration C
Secondary Cache Solution for Pentium — 512KByte

FEATURES OF 64Kx18

The 64Kx18 SRAMs are fabricated on a BiCMOS process and exhibit less dependence on output loading compared to CMOS devices. These SRAMs are powered on a single 5 V supply (± 5%) and are 3.3 V I/O compatible — no additional power supplies are required. The output buffer is composed of an NPN pull-up and an N-channel MOS pull-down. The pull-up circuitry has been carefully designed to limit the NPN's base drive such that the output pulls up to approximately 3.3 V even under high supply conditions (e.g., 5.25 V). These 3.3 V "friendly" output buffers have controlled 3.3 V output swing and will not overdrive a future 3.3 V controller or processor. This important feature allows one to easily migrate from an all 5 V system to a mixed 5 V – 3.3 V system upon the availability of 3.3 V Pentium and controller chips.

SYSTEM CONSIDERATIONS

The entire 64Kx18 SRAM family makes use of multiple power and ground pins on the 52-lead PLCC package. Five (5) power and five (5) ground pins (6 pairs for the asynchronous devices) have been provided to allow adequate supply decoupling and return current paths for such a fast device. Multiple power and ground pins reduce the effective inductance of theses connections. Since the output buffers swing 3.3 V in 1 to 2 ns (t_r/t_f), significant di/dt currents flow in the V_{CC} and V_{SS} pins. Separate power and ground planes on the printed circuit board are highly recommended and will help improve signal integrity, ground bounce, and in turn the SRAM's access time. The use of a 0.001 µF or 0.01 µF chip capacitor or similar leadless (surface mount) capacitor connected within 0.5 inch or so of each pair of V_{CC}/V_{SS} pins will provide a low impedance path for the fastest transients. A single 1 to 4.7 µF chip or ceramic capacitor per device should be sufficient for dc stability.

The use of standard (asynchronous) SRAMs may prove to be very difficult to use in 50+ MHz systems due to the requirements of carefully controlling the signal integrity, maintaining good noise margins, keeping component count down, and reducing board space. Because the BurstRAM, a synchronous device, registers address and control signals during a very brief moment during the system cycle, noise occurring throughout most of the cycle in the system can be tolerated by the BurstRAM. Component count, and therefore board space, is reduced since these SRAMs integrate the burst counter logic and self-timed write circuitry onto the chip and, in addition, have a wide (x18) data path. Because of the on-chip logic, cache control logic can be simplified and some control signal timing can be relaxed.

In cases that demand detailed timing analysis and a close look at the analog effects of your board design, it is recommended that a board-level (Quad Design/Viewlogic) or SPICE simulator is used. Particularly when PCB routing lengths are about 4 inches or more, transmission line effects become dominant over the lumped circuit equivalent. Since interconnect time-of-flight is approximately 175 to 190 ps/inch, a 4 inch route adds about 0.75 ns to a memory access.

When analyzing the cache data read path, the DQ<17:0> are in their active state and drive the data bus. The characteristics of these output pins are important to know when completing a board's physical layout. Use the information in Table 1 (output buffer I-V data), Table 2 (input I-V data), and Table 3 (package parasitics) to help verify your timing and loading effects. This tabular data may be used directly as input to board level simulators, such as those offered by Quad Design, Integrity Engineering, Quantic Labs, etc. Figure 4 shows how to connect the parasitic package components between the chip (output buffer or input) and package pin. An input pin on the 64Kx18 can be modeled as C die = 4 pF.

Table 1. I-V Characteristics of the 64Kx18 I/O Buffers

V_{OL} (V)	I_{OL} (min) (mA)	I_{OL}(max) (mA)	V_{OH} (V)	I_{OH} (min) (mA)	I_{OH} (max) (mA)
0	0	0	0	– 110	– 145
0.5	38	60	0.5	– 106	– 136
1.0	68	107	1.0	– 96	– 124
1.5	90	137	1.5	– 78	– 102
2.0	104	154	2.0	– 55	– 77
2.5	110	160	2.5	– 29	– 45
3.0	112	162	3.0	– 7	– 13
3.5	113	163	3.5	0.3	0.2
4.0	114	164	4.0	0.7	0.6
4.5	115	164	4.5	1.4	1.3
5.0	115	164	5.0	2.0	2.0

Table 2. I-V Characteristics of the 64Kx18 Inputs (Address and Control)

Diode to GND		Diode to V_{CC}	
V_{in} (V)	I_{in} (mA)	V_{in} (V)	I_{in} (mA)
0	0	5.0	0
– 0.4	0	5.4	0
– 0.5	0	5.5	0
– 0.6	0	5.6	0
– 0.7	– 0.1	5.7	0.1
– 0.8	– 2.0	5.8	2.1
– 0.9	– 25	5.9	20
– 1.0	– 70	6.0	50

Table 3. Packaging Characteristics

	Min	Max	Unit
R package	50	200	mΩ
L package	3	6	nH
C package	0.5	1.0	pF
C die	2	7	pF

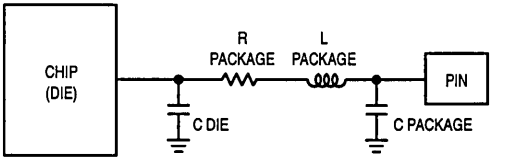


Figure 4. Package Parasitics Schematic

OUTPUT BUFFER CHARACTERISTICS

The access times guaranteed in the datasheet are based on a 50Ω test load and should be derated for unterminated CMOS loads. Refer to the derating curve (Figure 5) for your application. This curve relates the difference in access time between a 50Ω test environment and a lumped capacitive load (no dc load) condition typically found in most applications. The curve is based on worst case conditions, i.e., V_{CC} = 4.75 V and T_A = 70°C. Note that the 50Ω test condition is equivalent to a lumped 10 pF load. For instance, if the BurstRAM outputs see a 30 pF load, derate the access time by about 0.4 ns. So, for a Pentium design that uses the MCM67B618 – 9 ns device, one can expect a worst case access time of 9.4 ns under these conditions.

SUMMARY

For high performance Pentium systems, the use of Motorola's 64Kx18 BurstRAMs provides a straightforward solution to Pentium's secondary cache requirements. Four BiCMOS BurstRAMs support the size and speed required by zero wait state Pentium systems. For equivalent cache size and performance, standard SRAM solutions warrant two bank interleaved approaches that utilize more board space, require more power, and demand a higher performance cache controller.

REFERENCES

1. AP-469: "Cache and Memory Design Considerations for the Intel 486DX2 Microprocessor", Intel Corp.
2. DL156/D: *Fast Static RAM BiCMOS, CMOS, and Module Data*, Motorola, Inc.

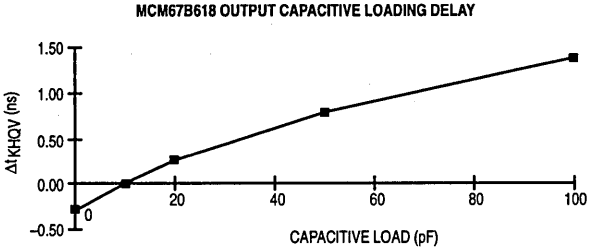


Figure 5. Access Time Derating Curve

NOVEL OVERMOLDED PAD-ARRAY CARRIER MAY OBSOLETE PLASTIC QUAD FLAT PACKS

Until now, the plastic quad flat pack (QFP) has been the package of choice for high-lead-count ICs. But the QFP's successor may have arrived in the form of an overmolded package that uses an array of solder balls for board attachment. Not only does the overmolded pad-array carrier (OMPAC) eliminate worries about lead skew and coplanarity, it also can be handled with the same pick-and-place and soldering equipment used by pc-board manufacturers for low-lead-count components. Furthermore, it's much thinner and may handle more power than an equivalent QFP.

The OMPAC was initially developed by Motorola Inc.'s Land Mobile Products Sector, Plantation, Fla., for its handheld communication products. That group had a need for a high-lead-count package, but wanted to avoid the coplanarity issues surrounding QFPs. Subsequently, the OMPAC was recognized as an attractive vehicle for the high-density CMOS gate arrays produced by Motorola's Semiconductor Products Sector in Phoenix, Ariz. Initially, the OMPAC will come in 169- and 225-contact versions. The former is an alternative to 160-lead QFPs, while the latter can replace 208- or 232-lead QFPs.

The package consists of a thin, BT-epoxy-laminate pc board that's clad with copper *(see the figure)*. BT epoxy is a glass-laminate material similar to FR-4. The top-side metallization carries a die flag and wire-bond pads. The wire-bond pads extend outward to plated through holes located around the board's periphery. These holes provide electrical continuity from the top of the board to the back side. There, the signal path is completed by copper traces routed from the through holes to solder-pad termination sites in a fully populated matrix array. All metal features on the pc board are photodefined, etched, and electroplated with copper, nickel, and gold. A solder mask is photodefined on the back side of the package to contain the flow of solder during infrared (IR) reflow soldering.

Package assembly begins with standard epoxy die-attach and gold-ball-bonding techniques to interconnect the IC to the base. Conventional epoxy transfer-molding procedures are performed to encapsulate the die. After post-mold curing, the packages are solder-bumped, detached from the strip, and electrically tested. The bumps' composition is 62% tin, 36% lead, and 2% silver.

What results is a package that has numerous advantages over conventional QFPs. Because the connections to the board are simple solder balls, no special handling is required. There are no leads to be skewed or knocked out of coplanarity. Motorola's previous answer to QFP lead skew and coplanarity problems was the molded carrier ring, which holds the leads rigid through assembly and test and enables it to guarantee 4-mil coplanarity. With the OMPAC, those problems disappear entirely.

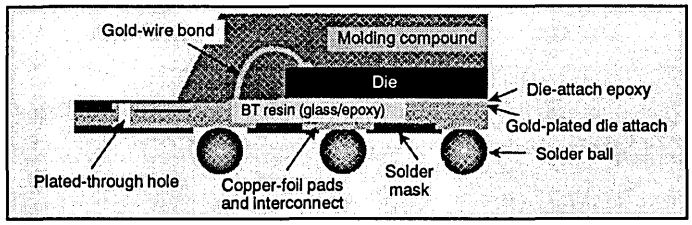
Another advantage is the package's potential power-dissipation capability. Because the OMPAC was adapted for high-performance gate arrays, Motorola addressed thermal enhancements in the form of thermal vias under the die to act as heat pipes through the bottom of the package to lands placed on the pc board. In contrast, QFPs are cooled by forcing air over the mold compound on top of the die. Motorola's measurements indicate that the 225-contact OMPAC with thermal vias delivers a thermal resistance over 20% lower than that of a 208-lead QFP. OMPACs can also be built without thermal vias, in which case their therma performance is roughly equal to that of QFPs.

A key aspect of the OMPAC is how little space it occupies on a board. With a reduced area of about 51%, a 169-contact OMPAC will fit inside the body dimensions of a 160-lead QFP. That's because of two factors: the lead span of the QFP is eliminated, and the OMPAC's body size is 22 mm versus 28 mm for the QFP. The OMPAC's size advantage also extends to the dimension of height. Both versions stand about 1.5-mm tall from the board. Equivalent QFPs are about 3.65-mm tall.

But even with their smaller size, the 169- and 225-lead OMPACs sport a pitch between solder pads of 1.5 mm, while the 160-lead QFP's leads are pitched at 0.65 mm. At a 1.5-mm pitch, critical circuit-timing traces can be routed directly under the package between the pad rows. This saves board space and shortens critical paths.

In the assembly process, the OMPAC really shines. It can be placed on boards with an alignment tolerance of 12 mils, whereas the QFP needs about a 3-mil registration tolerance. In addition, the OMPAC is more or less self-registering. As the solder balls reflow, the package tends to fall into its lands on the pc board and positions itself. This simplifies the requirement for very-high-precision pick-and-place equipment, thus reducing equipment investments.

For the 225-contact OMPAC user, this translates into IR-reflow attachment of 225 leads. Once again, the OMPAC gives board populators a way to greatly reduce their equipment investment.



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The OMPAC, then, represents the attachment of high-lead-count packages at a level that's comparable to devices with much lower lead counts. When the attachment-defect yields are taken into account, the OMPAC becomes even more attractive. In its production trials, Motorola is observing a near-zero-ppm defect yield. At 160 leads, the defect level for QFPs is about 100 ppm, a figure that climbs dramatically at higher lead counts.

Motorola will be offering its HDP Series 1-μm CMOS gate arrays and its H4C Series submicron gate arrays in the 169- and 225-contact OMPACs. Many would-be customers for these devices were unable to handle high-lead-count QFPs, but should be far more comfortable working with the OMPAC.

Production has commenced for the 169-contact package and will begin shortly for the 225-contact package. There is a slight premium for the gate arrays in the OMPAC, but it's anticipated that this will ramp down in time. As for the package's future, Motorola is looking ahead to the OMPAC as a vehicle for multichip modules (MCMs). Developments in this direction could come within the next year.

Motorola's 225-contact OMPAC will be demonstrated in the Universal Instruments booth at next week's Nepcon West show in Anaheim, Calif. This will be the public's first look at the OMPAC.

DAVID MALINIAK

Mechanical Data

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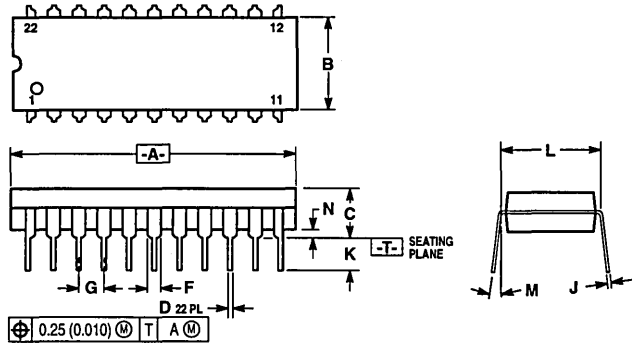
Package availability and ordering information are given on the individual data sheets.

22-LEAD PACKAGES

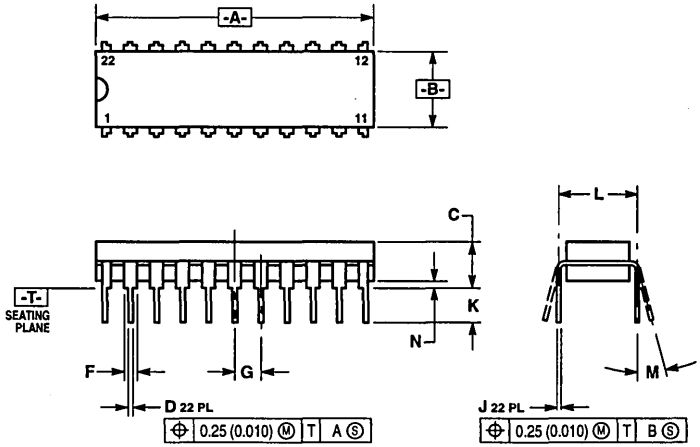
300 MIL PLASTIC
CASE 736A-01



NOTES:
1. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.65	27.17
B	0.240	0.260	6.10	6.60
C	0.155	0.180	3.74	4.57
D	0.015	0.022	0.38	0.55
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.20	0.38
K	0.110	0.140	2.79	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

300 MIL PLASTIC
CASE 736B-01

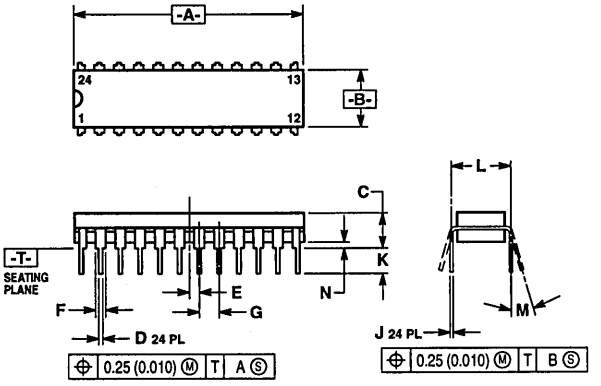


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION A AND B DOES NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.060	1.070	26.92	27.17
B	0.280	0.300	7.12	7.62
C	0.150	0.180	3.81	4.57
D	0.015	0.021	0.39	0.53
F	0.045	0.055	1.15	1.39
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.125	0.135	3.18	3.42
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

9

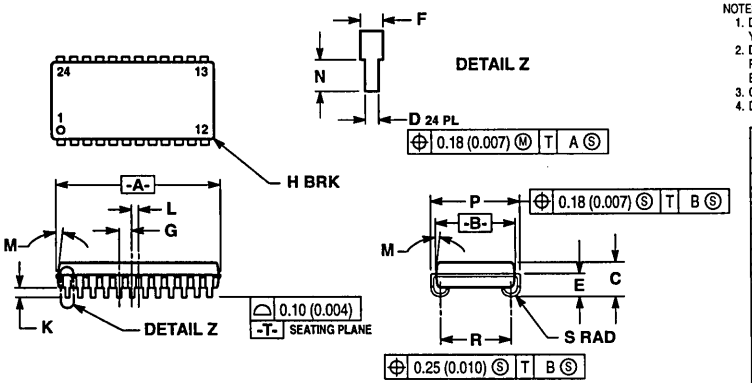
300 MIL PLASTIC
CASE 724A-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION A AND B DOES NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.160	1.170	29.47	29.71
B	0.280	0.300	7.12	7.62
C	0.150	0.180	3.81	4.57
D	0.015	0.021	0.39	0.53
E	0.050 BSC		1.27 BSC	
F	0.045	0.055	1.15	1.39
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.125	0.135	3.18	3.42
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

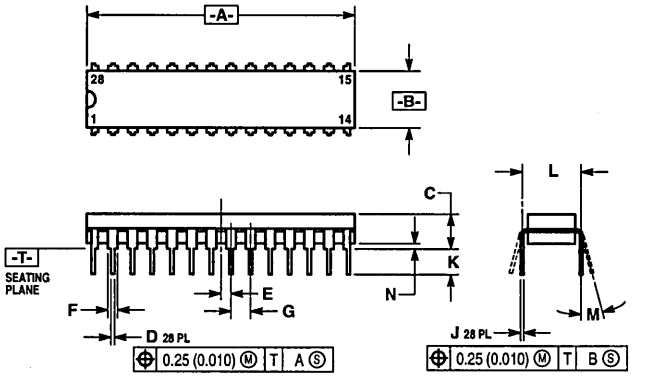
300 MIL SOJ
CASE 810A-02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM R TO BE DETERMINED AT DATUM -T-.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.620	0.630	15.75	16.00
B	0.295	0.305	7.50	7.74
C	0.128	0.148	3.26	3.75
D	0.015	0.020	0.39	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
H	—	0.020	—	0.50
K	0.035	0.045	0.89	1.14
L	0.025 BSC		0.64 BSC	
M	0°	5°	0°	5°
N	0.030	0.045	0.76	1.14
P	0.335	0.345	8.51	8.76
R	0.260	0.280	6.61	7.11
S	0.030	0.040	0.77	1.01

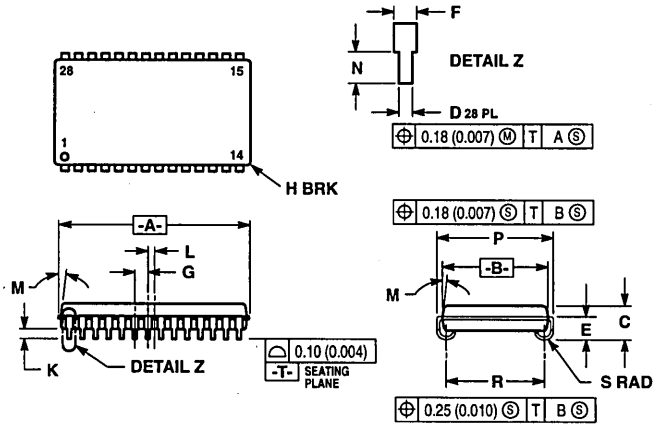
300 MIL PLASTIC
CASE 710B-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION A AND B DOES NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.360	1.370	34.55	34.79
B	0.280	0.300	7.12	7.62
C	0.150	0.180	3.81	4.57
D	0.015	0.021	0.39	0.53
E	0.050 BSC		1.27 BSC	
F	0.045	0.055	1.15	1.39
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.125	0.135	3.18	3.42
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

400 MIL SOJ
CASE 810-03



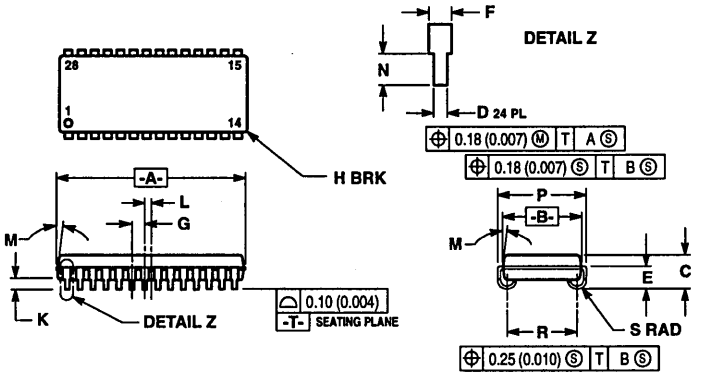
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM R TO BE DETERMINED AT DATUM -T-.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.720	0.730	18.29	18.54
B	0.395	0.405	10.04	10.28
C	0.128	0.148	3.26	3.75
D	0.015	0.020	0.39	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
H	—	0.020	—	0.50
K	0.035	0.045	0.89	1.14
L	0.025 BSC		0.64 BSC	
M	0°	5°	0°	5°
N	0.030	0.045	0.76	1.14
P	0.435	0.445	11.05	11.30
R	0.360	0.380	9.15	9.65
S	0.030	0.040	0.77	1.01

9

28-LEAD PACKAGES (Continued)

300 MIL SOJ
CASE 810B-03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
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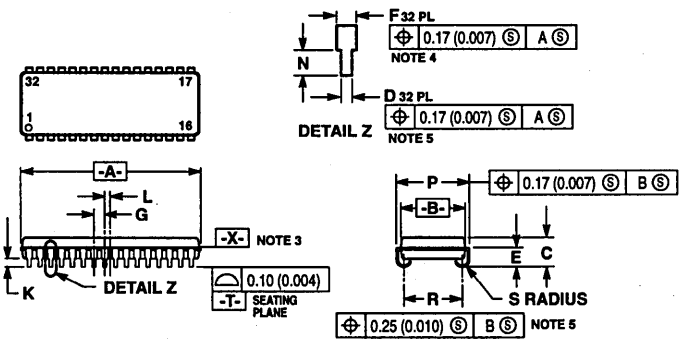
4. DIM R TO BE DETERMINED AT DATUM -T-.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.720	0.730	18.29	18.54
B	0.295	0.305	7.50	7.74
C	0.128	0.148	3.26	3.75
D	0.015	0.020	0.39	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
H	—	0.020	—	0.50
K	0.035	0.045	0.89	1.14
L	0.025 BSC		0.64 BSC	
M	0°	10°	0°	10°
N	0.030	0.045	0.76	1.14
P	0.330	0.340	8.38	8.64
R	0.260	0.270	6.60	6.86
S	0.030	0.040	0.77	1.01

32-LEAD PACKAGES

300 MIL SOJ
CASE 857-02



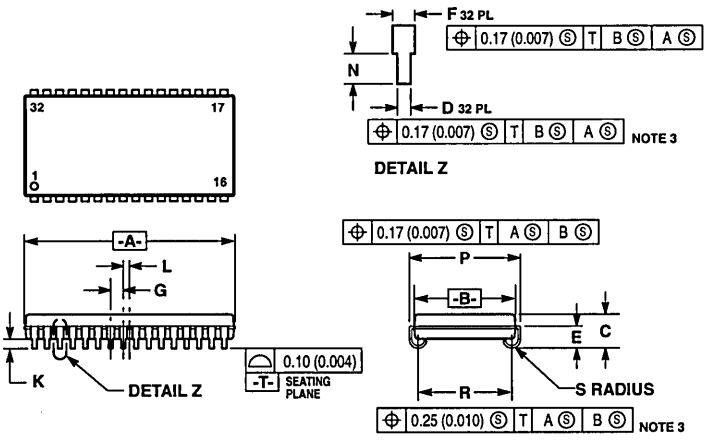
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DATUM PLANE -X- LOCATED AT TOP OF MOLD PARTING LINE AND COINCIDENT WITH TOP OF LEAD, WHERE LEAD EXITS BODY.
4. TO BE DETERMINED AT PLANE -X-.
5. TO BE DETERMINED AT PLANE -T-.
6. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.820	0.830	20.83	21.08
B	0.295	0.305	7.50	7.74
C	0.128	0.148	3.26	3.75
D	0.016	0.020	0.41	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
K	0.035	0.045	0.89	1.14
L	0.025 BSC		0.64 BSC	
N	0.030	0.045	0.76	1.14
P	0.330	0.340	8.38	8.64
R	0.260	0.270	6.60	6.86
S	0.030	0.040	0.77	1.01

9

32-LEAD PACKAGES (Continued)

400 MIL SOJ
CASE 857A-02

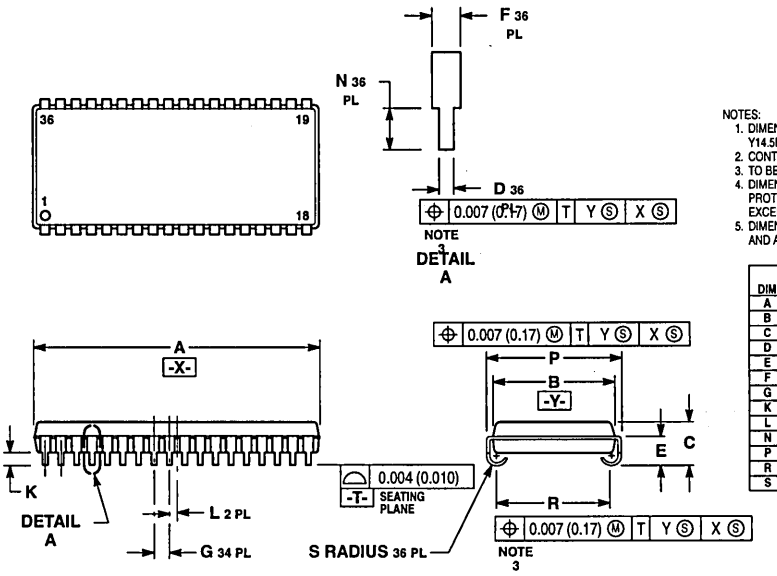


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TO BE DETERMINED AT PLANE -T-.
4. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION A & B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.820	0.830	20.83	21.08
B	0.395	0.405	10.03	10.29
C	0.128	0.148	3.26	3.75
D	0.016	0.020	0.41	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
K	0.035	0.045	0.89	1.14
L	0.025 BSC		0.64 BSC	
N	0.030	0.045	0.76	1.14
P	0.435	0.445	11.05	11.30
R	0.365	0.375	9.27	9.52
S	0.030	0.040	0.77	1.01

36-LEAD PACKAGES

400 MIL SOJ
CASE 893-01



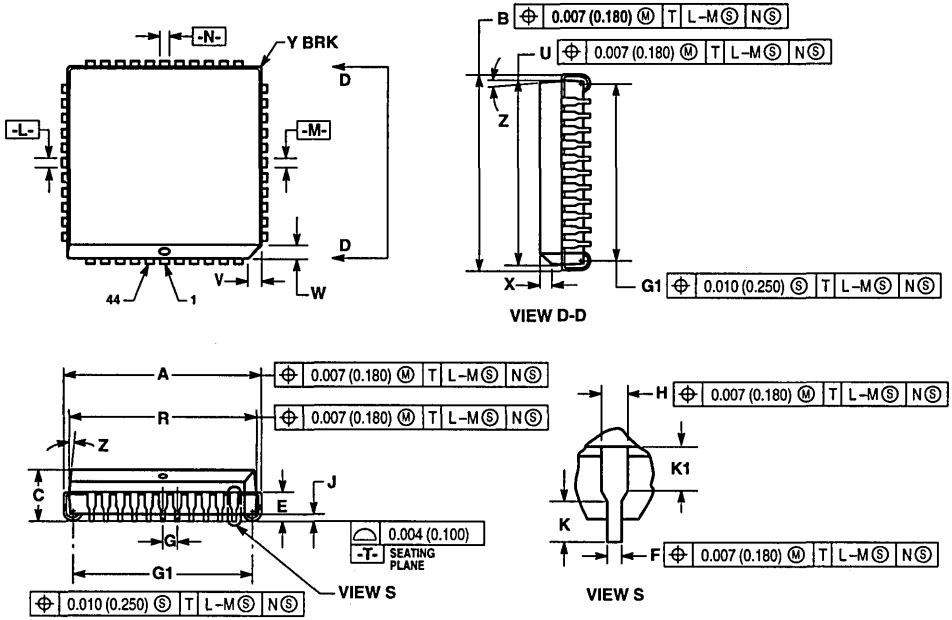
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TO BE DETERMINED AT PLANE -T-.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.006 (0.15) PER SIDE.
5. DIMENSION A AND B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.920	0.930	23.37	23.62
B	0.395	0.405	10.04	10.28
C	0.128	0.148	3.26	3.75
D	0.016	0.020	0.41	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BASIC		1.27 BASIC	
K	0.035	0.045	0.89	1.14
L	0.025 BASIC		0.64 BASIC	
N	0.030	0.045	0.77	1.14
P	0.435	0.445	11.05	11.30
R	0.365	0.375	9.28	9.52
S	0.030	0.040	0.77	1.01

9

44-LEAD PACKAGE

PLASTIC CHIP CARRIER
CASE 777-02

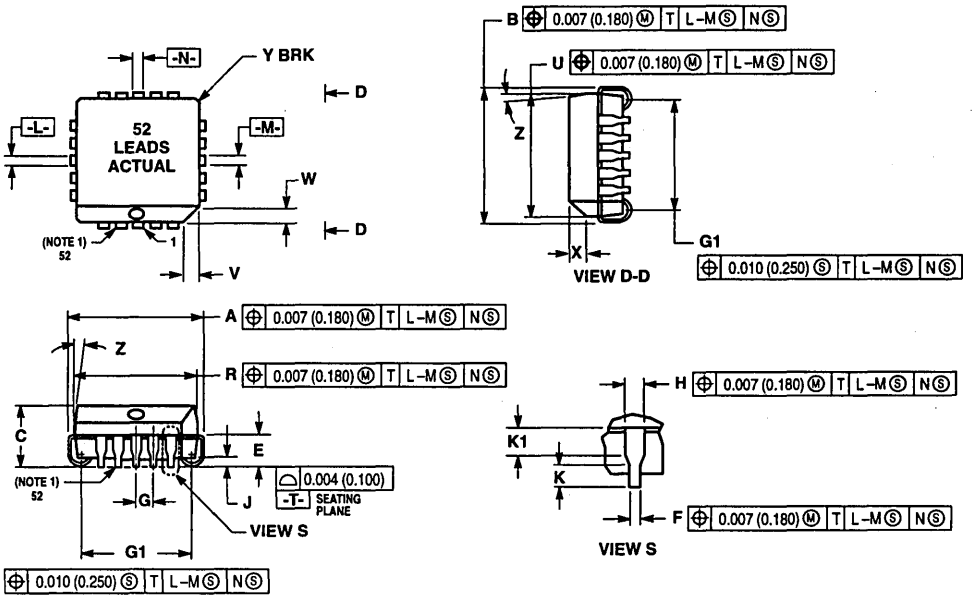


NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS (0.010) 0.25 PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.610	0.630	15.50	16.00
K1	0.040	—	1.02	—

9

PLASTIC CHIP CARRIER
CASE 778-02

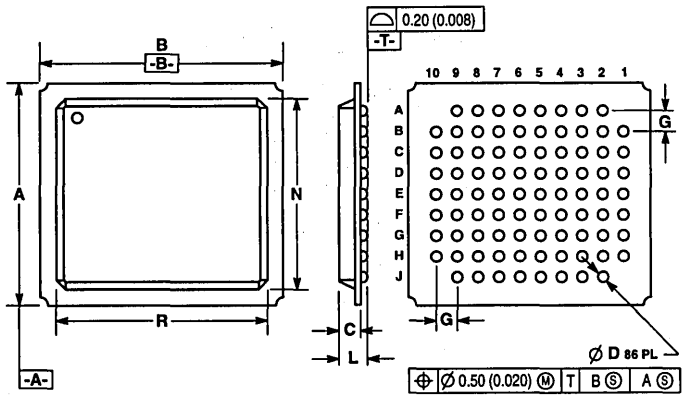


NOTES:
1. DUE TO SPACE LIMITATION, CASE 778-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 52 LEADS.
2. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.
7. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
8. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.785	0.795	19.94	20.19
B	0.785	0.795	19.94	20.19
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.750	0.756	19.05	19.20
U	0.750	0.756	19.05	19.20
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.710	0.730	18.04	18.54
K1	0.040	—	1.02	—

9

CASE 896A-01

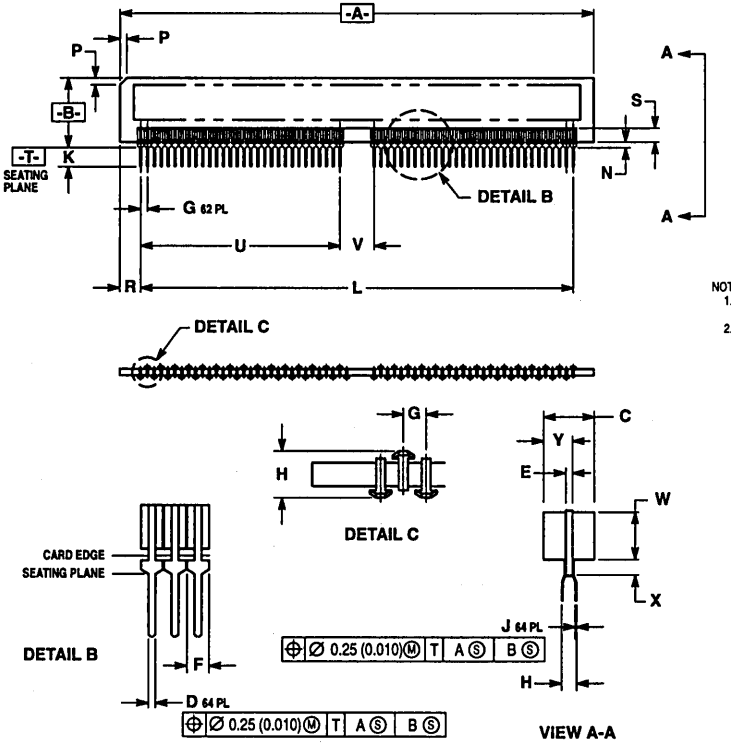


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	16.16	16.36	0.637	0.644
B	17.68	17.88	0.697	0.703
C	1.33	1.73	0.053	0.068
D	0.69	0.81	0.028	0.031
G	1.524 BSC		0.060 BSC	
L	1.84	2.44	0.073	0.096
N	13.80	14.20	0.544	0.559
R	15.29	15.69	0.602	0.617

9

CASE 871-01

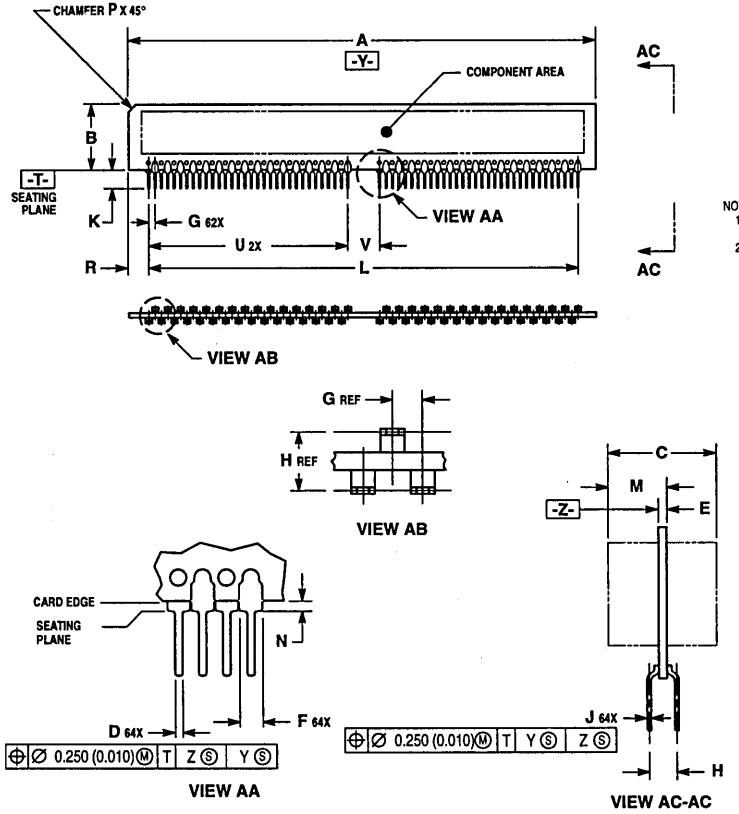


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	3.640	3.660	92.46	92.96
B	—	0.550	—	13.97
C	—	0.370	—	9.40
D	0.015	0.025	0.38	0.64
E	0.035	0.055	0.89	1.40
F	0.040	0.055	1.02	1.40
G	0.050 BSC		1.27 BSC	
H	0.100 BSC		2.54 BSC	
J	0.008	0.014	0.20	0.36
K	0.120	0.160	3.05	4.06
L	3.345	3.355	84.96	85.22
N	0.010	0.055	0.25	1.40
P	0.045	0.055	1.14	1.40
R	0.135	0.165	3.43	4.19
S	—	0.100	—	2.54
U	1.550 REF		39.37 REF	
V	0.250 REF		6.35 REF	
W	—	0.345	—	8.76
X	—	0.150	—	3.81

9

CASE 871A-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	3.640	3.660	92.45	92.963
B	—	0.500	—	12.699
C	—	0.370	—	9.397
D	0.015	0.025	0.382	0.634
E	0.035	0.055	0.890	1.396
F	0.040	0.055	1.017	1.396
G	0.050 BSC		1.270 BSC	
H	0.100 BSC		2.540 BSC	
J	0.008	0.014	0.202	0.354
K	0.120	0.160	3.049	4.063
L	3.350 REF		85.090 REF	
M	—	0.240	—	6.096
N	0.010	0.055	0.255	1.396
P	0.045	0.055	1.144	1.396
R	0.135	0.165	3.430	4.190
S	—	0.100	—	2.540
U	1.550 REF		39.371 REF	
V	0.250 BSC		6.351 BSC	
W	—	0.345	—	8.762
X	—	0.150	—	3.809

9

Embossed Tape and Reel

Tape and Reel Data for MOS Memory Surface Mount Devices

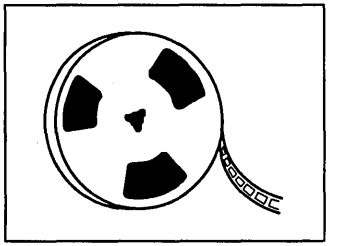
Embossed Tape and Reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the "peel-back" cover tape.

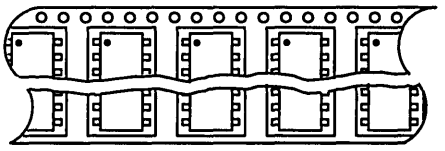
- 13-Inch Reel
- Used For Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA-481
- SOJ: 24, 20/26, 24/26, 28, 32
- SOIC: 28, 32
- PLCC: 44, 52

Use the standard device title and add the required suffix R2. Note the minimum lot size is one full reel for each line item, and orders are required to be in increments of the single reel quantity.

PACKAGES

SOJ: 24, 20/26, 24/26, 28, 32
SOIC: 28, 32
PLCC: 44, 52

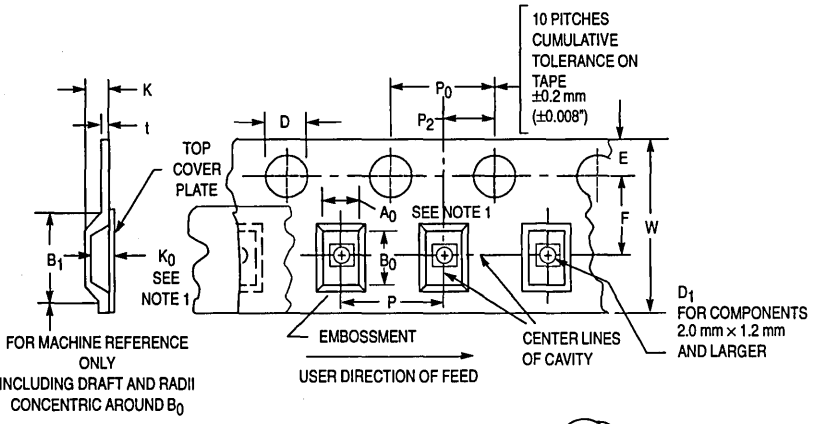


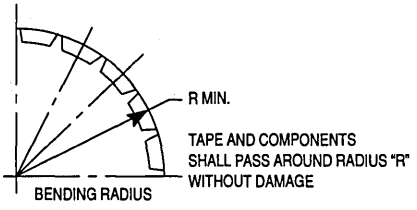


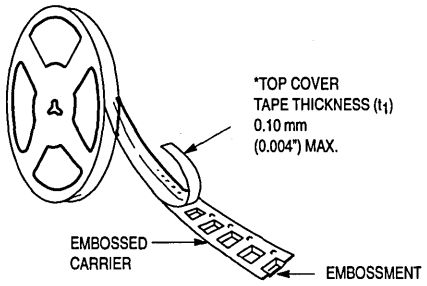
DIRECTION OF FEED

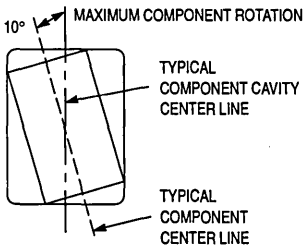
Package	Lead Count	Package Width (mils)	Tape Width (mm)	Reel Size	Devices Per Reel	Minimum Lot Size	Tape and Reel Suffix
SOJ	24	300	24	13"	1000	1000	R2
	20/26	300	24	13"	1000	1000	R2
	20/26	350	24	13"	1000	1000	R2
	24/26	300	24	13"	1000	1000	R2
	28	300	24	13"	1000	1000	R2
	28	400	24	13"	1000	1000	R2
	32	300	32	13"	1000	1000	R2
	32	400	32	13"	1000	1000	R2
SOIC (Gull Wing)	28	350	24	13"	1000	1000	R2
	32	450	32	13"	1000	1000	R2
PLCC	44	650/656	32	13"	500	500	R2
	52	750/756	32	13"	450	450	R2

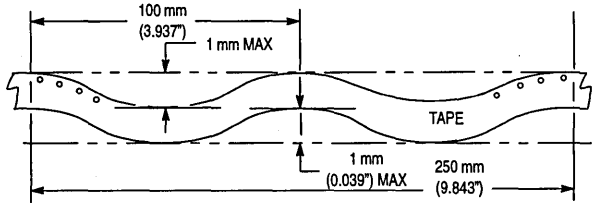
CARRIER TAPE SPECIFICATIONS











CAMBER (TOP VIEW)
ALLOWABLE CAMBER TO BE 1 mm/100 mm NONACCUMULATIVE OVER 250 mm

DIMENSIONS

Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R Min	t Max	W
24 mm	19.4 mm (0.764")	1.5+0.1 mm −0.0 (0.059+0.004" −0.0)	2.0 mm Min (0.079")	1.75 ±0.1 mm (0.069 ±0.004")	11.5 ±0.1 mm (0.453 ±0.004")	4.0 mm (0.157")	12.0–16.0 ±0.10 mm (0.472–0.630 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.05 mm (0.079 ±0.002")	50 mm (1.968")	0.400 mm (0.016")	24 ±0.2 mm (0.945 ±0.008")
32 mm	23.0 mm (0.906")	1.5+0.1 mm −0.0 (0.059+0.004" −0.0)	2.0 mm Min (0.079")	1.75 ±0.1 mm (0.069 ±0.004")	14.2 ±0.1 mm (0.559 ±0.004")	10.0 mm (0.394")	16.0–24.0 ±0.10 mm (0.630–0.945 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.05 mm (0.079 ±0.002")	50 mm (1.968")	0.500 mm (0.020")	32 ±0.3 mm (1.26 ±0.012")

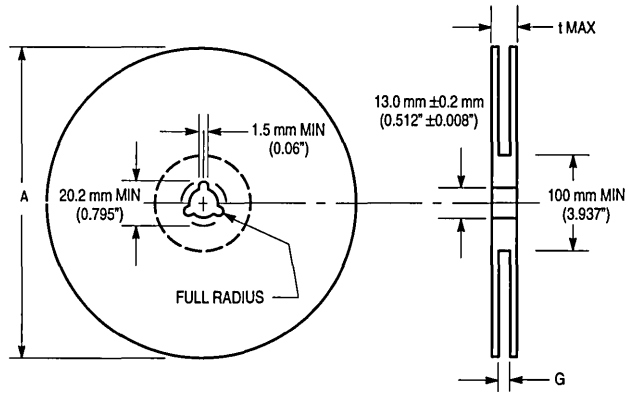
Metric Dimensions Govern–English are in parentheses for reference only.

NOTE 1: A_0, B_0, and K_0 are determined by compnent size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

9

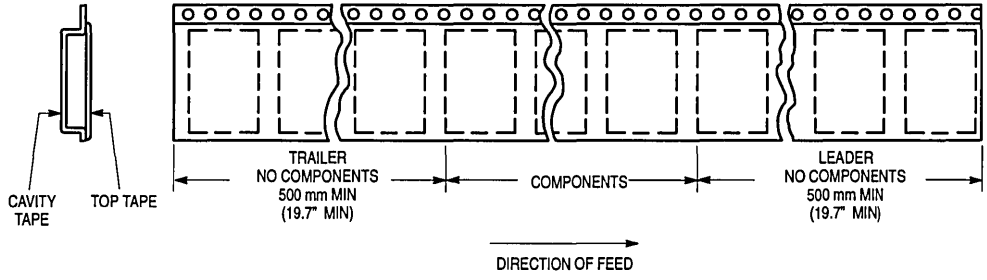
REEL DIMENSIONS

Metric Dimensions Govern–English are in Parentheses for Reference only.



Size	A Max	G	t Max
24 mm	330 mm (12.992")	24.400 mm, +2.0 mm, –0.0 (0.961", +0.079", –0.00)	30.4 mm (1.197")
32 mm	330 mm (12.992")	32.4 mm, +2.0 mm, –0.0 (1.276", +0.079", –0.00)	38.4 mm (1.51")

TAPE ENDS



9

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