MOTOROLA

DL158/D
REV 0

Multimedia
Device Data

MOTOROLA MULTIMEDIA DEVICE DATA

Q1/95
DL158
REV 0

DATA CLASSIFICATION

Product Preview

This heading on a data sheet indicates that the device is in the formative stages or under development at the time of printing of this data book. Please check with Motorola for current status. The disclaimer at the bottom of the first page reads: "This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice."

Advance Information

This heading on a data sheet indicates that the device is in sampling, preproduction, or first production stages at the time of printing of this data book. Please check with Motorola for updated information. The disclaimer at the bottom of the first page reads: "This document contains information on a new product. Specifications and information herein are subject to change without notice."

Fully Released

A fully released data sheet contains neither a classification heading nor a disclaimer at the bottom of the first page. This document contains information on a product in full production. Guaranteed limits will not be changed without written notice to your local Motorola Semiconductor Sales Office.

Technical Summary

The Technical Summary is an abridged version of the complete device data sheet that contains the key technical information required to determine the correct device for a specific application. Complete device data sheets for these more complex devices are available from your Motorola Semiconductor Sales Office or authorized distributor.

MOTOROLA

Multimedia

Device Data

Motorola offers a broad range of semiconductor multimedia products for a wide variety of applications. The *Motorola Multimedia Device Data Book* is a new book that contains specifications on these parts as well as information on Evaluation Kits, a selection of Application Notes, Handling and Design Guidelines, and Reliability and Quality information. Functional and Technical Selection Guides are also included to help you select the appropriate part for your application.

New Motorola multimedia devices are being introduced continually. For the latest releases, additional technical information, and pricing, please contact your nearest Motorola Semiconductor Sales Office or authorized distributor. A complete listing of sales offices and authorized distributors is included at the back of this book.

Printed in U.S.A.

Some of the terms in the glossary originally appeared in the book *Video Demystified* by Keith Jack and are reprinted by permission of Brooktree Corporation and HighText Publications, Inc.

TABLE OF CONTENTS

CHAPTER 1 — SELECTION GUIDES

CHAPTER 2 — DATA SHEETS

CHAPTER 3 — EVALUATION KITS

CHAPTER 4 — APPLICATION NOTES AND TECHNICAL ARTICLES

CHAPTER 5 — GLOSSARY

Selection Guides

1

FUNCTIONAL SELECTION GUIDE

This selection guide includes all Motorola devices characterized in this book. Other devices also used in multimedia applications, but associated with other product families, appear in the following documents.

Document No.	Title
DL111/D	Bipolar Power Transistor Data
DL128/D	Linear and Interface ICs Data
SG73/D	Master Selection Guide
SG169/D	MOS Digital–Analog IC Quarterly Update
CA ...	Data Sheets
MC ...	Data Sheets
TDA ...	Data Sheets

A/D AND D/A CONVERTERS

Device #	Function	Page #
MC10319	Single Channel A/D	MC10319/D
MC10321	Single Channel A/D	MC10321/D
MC10322	Single Channel 8–Bit Video DAC	MC10322/D
MC10324	Single Channel 8–Bit Video DAC	MC10324/D
MC44200	Triple 8–Bit Video DAC	2–44
MC44250	Triple 8–Bit Video ADC	2–60
MC44251	Triple 8–Bit Video ADC Three–State Outputs	2–76
MC145073	Stereo Audio Sigma–Delta ADC	2–160
MC145074	Stereo Audio Sigma–Delta DAC	2–174
MC145076	Stereo Audio FIR Smoothing Filter	2–187

CD–i

Device #	Function	Page #
MCD212	Video Decoder and System Controller (JTAG)	2–194
MCD214	Video Decoder and System Controller (VDSC)	2–207
MCD221	CD–Interface and Audio Processor (CIAP)	2–218
MCD251	MPEG Full Motion Video Decoder (FMV)	2–226
MCD270	IMPEG Integrated Video and Audio Decoder	2–239

CHROMA DELAY LINES

Device #	Function	Page #
MC44140	Chroma Delay Line	2–23

COMB FILTERS

Device #	Function	Page #
MC141620	Enhanced Comb Filter	2–91
MC141621A	Advanced Comb Filter (ACF)	2–99
MC141622	Advanced Comb Filter – II (ACF – II)	2–116
MC141624	Advanced Comb Filter – I (ACF – I)	2–130

DEFLECTION

Device #	Function	Page #
MC1388	Waveform Generator for Monitors	MC1388/D
MC1391P	Horizontal Processor	MC1391P/D
MC44614	Line Deflection Transistor Driver	MC44614/D
MC44615A	Waveform Generator for Projection TV Convergence Function	MC44165A/D

ENCODERS/MODULATORS

Device #	Function	Page #
MC1373	Color TV Video Modulator	MC1373/D
MC1374	TV Modulator (High Quality)	MC1374/D
MC1377	Video RGB to PAL/NTSC Encoder	MC1377/D
MC1378	Video Overlay Synchronizer	MC1378/D
MC13077	Advanced Video RGB To QAL/NTSC Encoder	MC13077/D
MC44701	Multistandard Digital Video Encoder	2–76
MC44702	Multistandard Digital Video Encoder	2–77

SOUND

Device #	Function	Page #
MC1357	Sound IF Detector	MC1357/D
TDA3190P	Sound IF, Low Pass Filter, FM Detector, DC Volume Control, Preamplifier	TDA3190P/D

TRANSISTOR ARRAYS

Device #	Function	Page #
CA3054	Dual Independent Differential Amplifiers with Associated Constant Current Transistors	CA3054/D
CA3146	General Purpose H/V Array	CA3146/D
MC3346P	One Differentially Connected Pair and Three Isolated Transistors	MC3346P/D

VIDEO AND AUDIO AMPLIFIERS

Device #	Function	Page #
MC13060	Mini Watt SOIC Audio Amplifier	MC13060/D
MC14576C	Dual Video Amplifier	2–3
MC14577C	Dual Video Amplifier	2–3
MC34119	Low Power Audio Amplifier	MC34119/D

VIDEO PROCESSORS/DEMODULATORS

Device #	Function	Page #
MC44000	Chroma 4 Multistandard Decoder	MC44000/D
MC44010	Digital Multistandard Video Processor	MC44010/D
TDA3301B	Color Processor	TDA3301B/D

OTHER FUNCTIONS

Device #	Function	Page #
MC3340	Electronic Attenuator	MC3340/D
MC44130	Stereoton	MC44130/D
MC44131	Improved Stereoton	2–11
MC44144	Subcarrier Reference Generator	MC44144/D
MC44145	Sync Separator/Pixel Clock PLL	MC44145/D
MC44802A	PLL Tuning Circuits	MC44802/D
MC44807	PLL Tuning Circuits	MC44807/D
MC44810	PLL Tuning Circuits	MC44810/D
MC44817	PLL Tuning Circuits	MC44817/D
MC44818	PLL Tuning Circuits	MC44818/D
MC44824	PLL Tuning Circuits	MC44824/D
MC144143	Closed Caption Decoder	2–142
MC144144	Enhanced Closed Caption Decoder	2–159

DISCONTINUED/NOT RECOMMENDED FOR NEW DESIGN

MC141625A	Advanced NTSC/PAL Comb Filter To be replaced by MC141626
MCD210	Video Decoder and System Controller Replaced by MCD212
MCD211	Video Decoder and System Controller Replaced by MCD212
MCD220	CD–Interface and Audio Processor Replaced by MCD221

TECHNICAL SELECTION GUIDE

A/D AND D/A CONVERTERS

Device	Function	Features	Suffix/ Package	Page #
MC44200	Triple 8–Bit Video D/A Converter	TTL inputs, 75 Ω drive outputs.	FU/824	2–34
MC44250	Triple 8–Bit Video A/D Converter	Video clamps for RGB/YUV, 15 MHz, TTL outputs.	FN/777	2–44
MC44251	Triple 8–Bit Video A/D Converter with 3–State Outputs	Video clamps for RGB/YUV, 18 MHz, High Z TTL outputs.	FN/777	2–60
MC145073	Stereo Audio Sigma–Delta ADC	Single + 5 V operation; 128x OSR, 0 to 20 kHz passband; on–chip filtering; max. ripple ± 0.1 dB.	DW/751E	2–160
MC145074	Stereo Audio Sigma–Delta DAC	Single + 5 V operation; supports 128x 192x, 256x and 384x OSR rates; accepts 16 –, 18 – or 20–bit data; companion to MC145076 Stereo Audio Fir Smoothing Filter.	D/751B	2–174
MC145076	Stereo Audio FIR Smoothing Filter	Single + 5 V operation; 18.5 MHz input data rate; > 40 dB of alias filtering; companion to MC145074 Stereo Audio Sigma–Delta DAC.	D/751B	2–187

CD–i

Device	Function	Features	Suffix/ Package	Page #
MCD212	Video Decoder and System Controller (JTAG)	Up to 768 x 560 resolution. Built–in memory management unit. 4 planes of graphics. Synch with external video.	FU/1007	2–194
MCD214	Video Decoder and System Controller (VDSC)	CCIR601 compatible. Built–in memory management unit. 4 planes of graphics. Synch with external video.	FU/1007	2–207
MCD221	CD–Interface and Audio Processor (CIAP)	I^2S or SONY format. 2x drives supported. 68000 or serial host interface.	FU/841B	2–218
MCD251	MPEG Full Motion Video Decoder (FMV)	Handles MPEG1 data up to 5 MBits/s. Direct Drive of up to 4 MBits of DRAM. Special effects such as fast forward, rewind, still, etc.	FU/1007	2–226
MCD270	IMPEG Integrated Video and Audio Decoder	Handles MPEG1 data up to 5 MBits/s. Direct Drive of up to 4 MBits of DRAM. Special effects such as fast forward, rewind, still, etc. 24–bit RGB or YUV output. I^2S or SONY audio output.	FU/1007	2–239

CHROMA DELAY LINES

Device	Function	Features	Suffix/ Package	Page #
MC44140	PAL Digital Delay Line	For PAL applications of the MC44011 and MC44001.	P/648 D/751G	2–23

COMB FILTERS

Device	Function	Features	Suffix/ Package	Page #
MC141620	Enhanced Comb Filter	Fast 8–Bit A/D Converter, Two 8–Bit D/A Converters, Two Line–Delay Memories, utilizes NTSC Subcarrier Frequency clock, CMOS Technology.	FU/898	2–91
MC141621A	Advanced Comb Filter (ACF)	Composite Video input; YC outputs in digital and analog form; all digital internal filters.	FU/898	2–99
MC141622	Advanced Comb Filter – II (ACF–II)	Composite Video input; YC outputs in digital and analog form; all digital internal filters; vertical enhancer circuit.	P/898	2–116
MC141624	Advanced Comb Filter – I (ACF–I)	Low cost Ih filter.	FU/873 SP/TBD	2–130

ENCODERS/MODULATORS

Device	Function	Features	Suffix/ Package	Page #
MC44701	Multistandard Digital Video Encoder	CCIR601 compatible (8–bit YCrCb) inputs. Master/slave modes. PAL/NTSC compatible. Closed–caption encoding. MACROVISION copy protection. JTAG.	FU/824A	2–76
MC44702	Multistandard Digital Video Encoder	CCIR601 compatible (8–bit YCrCb) inputs. Master/slave modes. PAL/NTSC compatible. Closed–caption encoding. MACROVISION copy protection. RGB and YCrCb outputs. JTAG.	FU/848B	2–77

VIDEO AND AUDIO AMPLIFIERS

Device	Function	Features	Suffix/ Package	Page #
MC14576C	Dual Video Amplifier — "C" Version	Gain @ 4.43 MHz = 6 dB +/– 1 dB, fixed gain, internally compensated, CMOS Technology.	P/626 F/904	2–3
MC14577C	Dual Video Amplifier — "C" Version	Gain @ 5 MHz = 10 dB max, 10 MHz = 6 dB max, adjustable gain, internally compensated, CMOS Technology.	P/626 F/904	2–3

OTHER FUNCTIONS

Device	Function	Features	Suffix/ Package	Page #
MC44131	Improved Stereoton	European TV audio decoder.	P/710	2–11
MC144143	Closed Caption Decoder	8 line text mode.	P/707	2–142
MC144144	Enhanced Closed Caption Decoder	OSD, 15 line text, XDS.	P/707	2–159

Data Sheets

2

2

MC14576C
MC14577C

Advance Information

Dual Video Amplifiers

CMOS

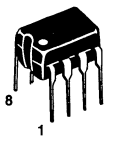
Each of these devices contains two amplifiers realized in CMOS. Each amp also employs two lateral NPN bipolar transistors.

The MC14576 contains two internally–compensated operational amplifiers. On–chip gain–setting resistors result in a noninverting voltage gain of 6.0 dB ± 1.0 dB at 4.43 MHz for each amp. Each noninverting input of the MC14576 appears as a mostly–capacitive load of about 10 pF.

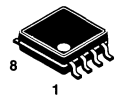
The MC14577 also contains two internally–compensated operational amplifiers. However, the gain for each amp is adjustable with external components. (The value of the closed–loop voltage gain with a 150 Ω load should not exceed 10 dB at 5 MHz and 6 dB at 10 MHz.) All inputs of the MC14577 appear as mostly–capacitive loads of about 10 pF.

The MC14576C and MC14577C are drop–in replacements for the MC14576B and MC14577B, respectively.

- Direct Drive of 150 Ω Loads
- Maximum Supply Current: 40 mA per Package
- Operating Voltage Range — P Suffix: 5.0 to 12 V Relative to V_{SS}
  F Suffix: 5.0 to 10 V Relative to V_{SS}
- May Be Used with Single or Dual Supplies
- Operating Temperature Range — P Suffix: – 20 to 70°C
  F Suffix: – 20 to 50°C
- Excellent Differential Gain: 3% Maximum @ 4.43 MHz
- Excellent Differential Phase: 3° Maximum @ 4.43 MHz
- Guaranteed Bandwidth: 10 MHz
- Minimal External Components Required



P SUFFIX
PLASTIC DIP
CASE 626–05

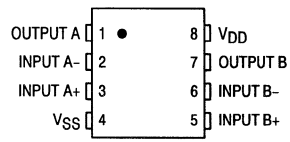


F SUFFIX
SOG PACKAGE
CASE 904–01

ORDERING INFORMATION

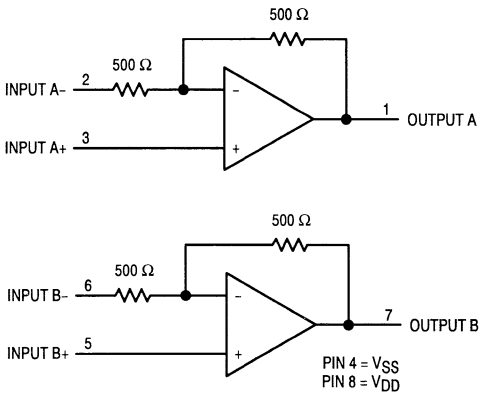
MC14576CP, MC14577CP	Plastic DIP
MC14576CF, MC14577CF	SOG Package

PIN ASSIGNMENT

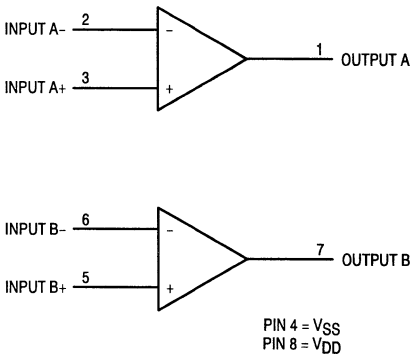


SYMBOLIC REPRESENTATIONS

MC14576



MC14577



NOTE: Resistors are shown above with nominal values.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (See Note)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	– 0.5 to + 14	V
V_{in}	DC Input Voltage	V_{SS} – 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	V_{SS} – 0.5 to V_{DD} + 0.5	V
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (10–Second Soldering)	260	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Reference Figures 1 and 2, R_L = 150 Ω Unless Otherwise Indicated)

Symbol	Parameter	Test Condition	V_{DD} V	V_{SS} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range (Referenced to V_{SS}) P Suffix F Suffix		— —	— —	5.0 to 12 5.0 to 10	V
I_{DD}	Maximum Power Supply Current (Per Package)	V_{in} = 0 V, R_L = ∞ (open)	+ 5.0	– 5.0	40	mA
N	Maximum Output Noise	V_{in} = 0 V, BW = 30 Hz to 25 MHz	+ 5.0	– 5.0	250	μV RMS
A_V	Closed–Loop Voltage Gain	V_{in} = 2.0 V p–p, f = 4.43 MHz	+ 5.0	– 5.0	5.0 to 7.0	dB
BW	Bandwidth	V_{in} = 2.0 V p–p, A_V within ± 3.0 dB of the gain at 4.43 MHz	+ 5.0	– 5.0	10	MHz
V_{out}	Minimum Output Voltage Swing	V_{in} = 4.0 V p–p, f = 10 MHz	+ 5.0	– 5.0	3.5	V p–p
		V_{in} = 1.5 V p–p, f = 5.0 MHz	+ 2.5	– 2.5	2.0	
—	Maximum Differential Gain	V_{in} = 300 mV p–p biased from – 0.5 to + 0.5 V, f = 4.43 MHz	+ 5.0	– 5.0	3.0	%
—	Maximum Differential Phase	V_{in} = 300 mV p–p biased from – 0.5 to + 0.5 V, f = 4.43 MHz	+ 5.0	– 5.0	3.0	Degrees
PSRR	Minimum Power Supply Rejection Ratio, V_{DD} or V_{SS} pins	V_{in} = 0 V, ΔV_{DD} or ΔV_{SS} = 400 mV p–p @ 100 kHz	+ 5.0	– 5.0	43	dB
—	Minimum Channel Separation	V_{in} = 1.0 V p–p, f = 4.43 MHz	+ 5.0	– 5.0	40	dB
C_{in}	Maximum Input Capacitance	V_{in} = 1.0 V p–p, f = 4.43 MHz	+ 5.0	– 5.0	10**	pF
R_{in}	Minimum Input Resistance, all Inputs except Input A– and Input B– of the MC14576		+ 5.0	– 5.0	10^9**	Ω

** Typical value only; not guaranteed.

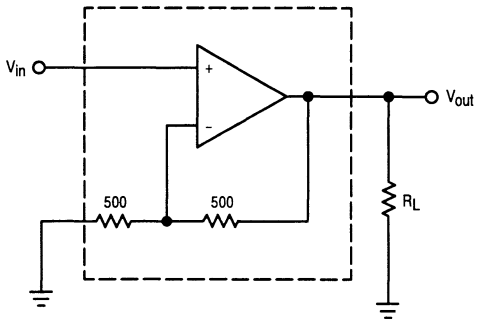


Figure 1. MC14576 Test Circuit

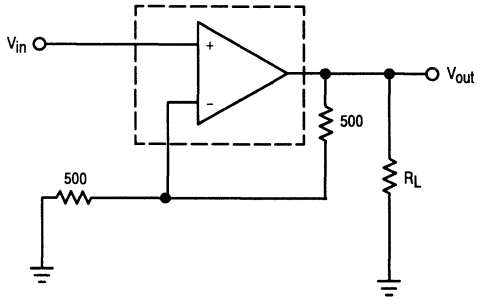


Figure 2. MC14577 Test Circuit

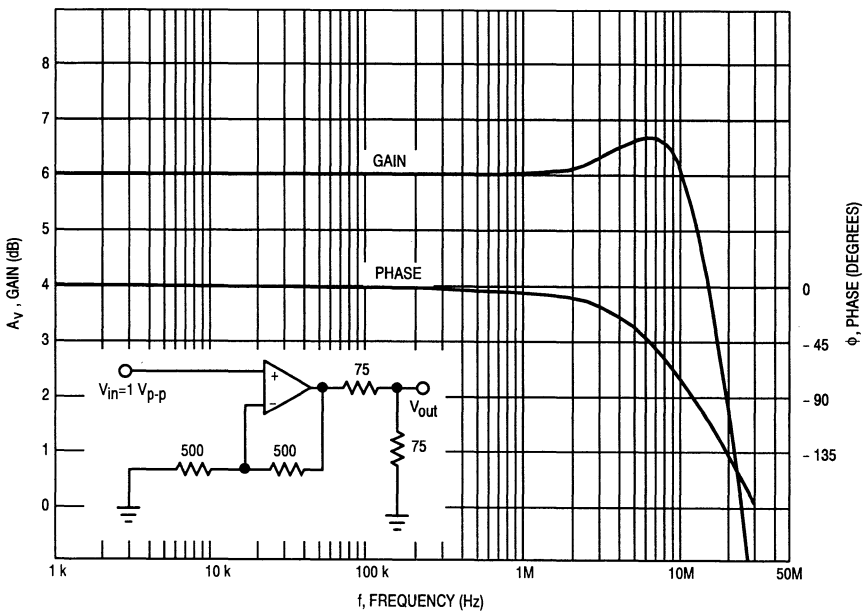


Figure 3. Typical Gain/Phase–Frequency Response (Not Guaranteed)

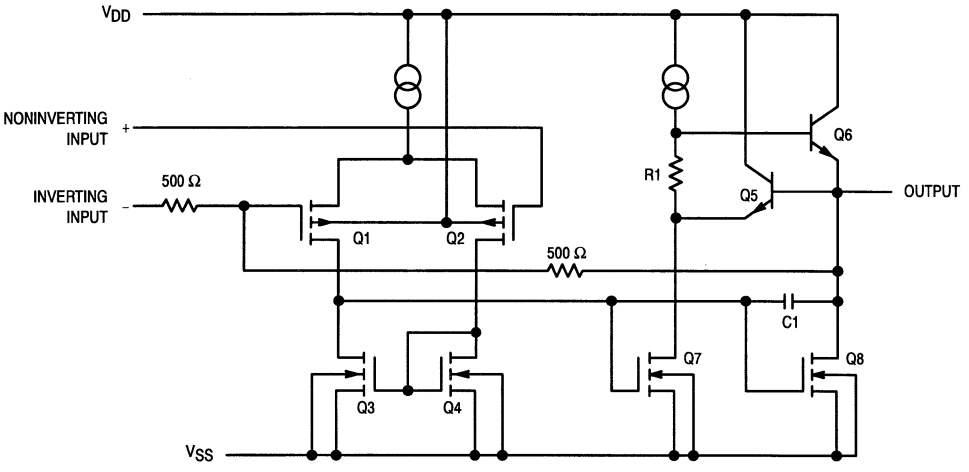


Figure 4. MC14576 Schematic

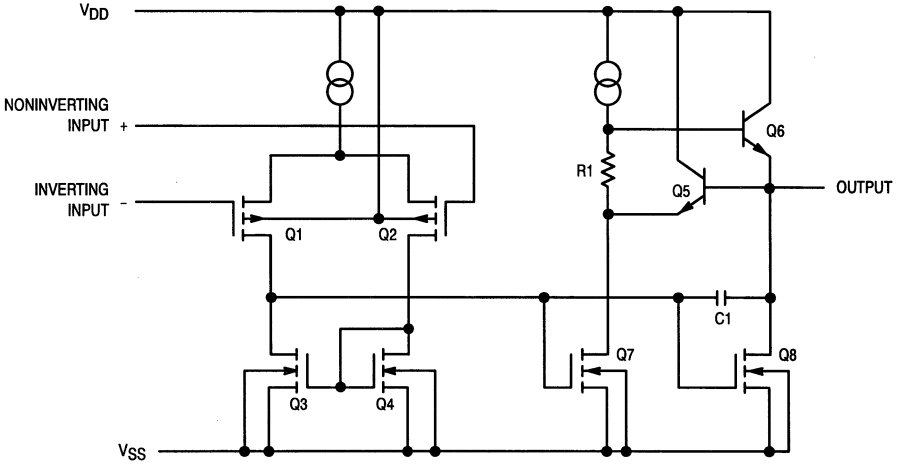


Figure 5. MC14577 Schematic

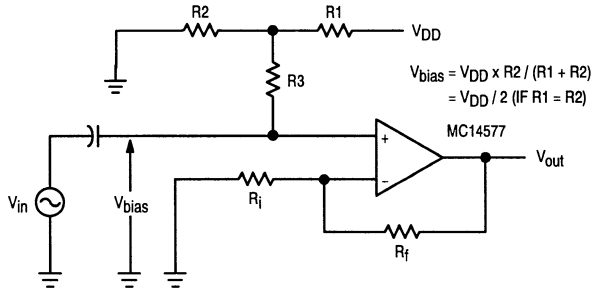


Figure 6. AC–Coupled Noninverting Amplifier with Single–Supply Operation

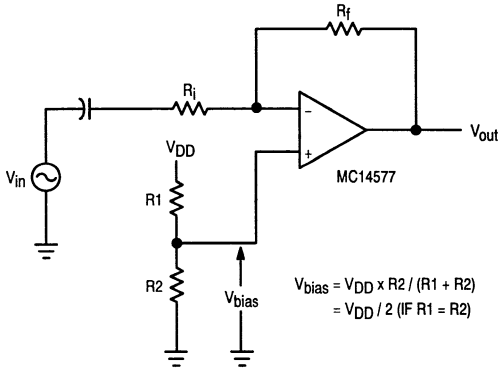


Figure 7. AC–Coupled Inverting Amplifier with Single–Supply Operation

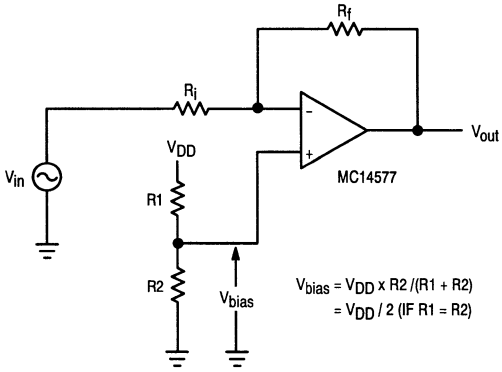


Figure 8. DC–Coupled Inverting Amplifier with Single–Supply Operation

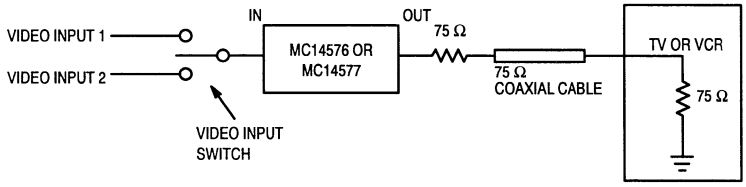


Figure 9. Typical Application

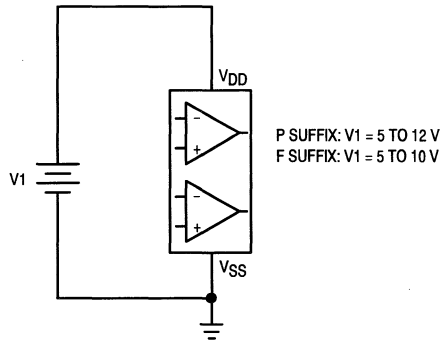


Figure 10. Single–Supply Operation

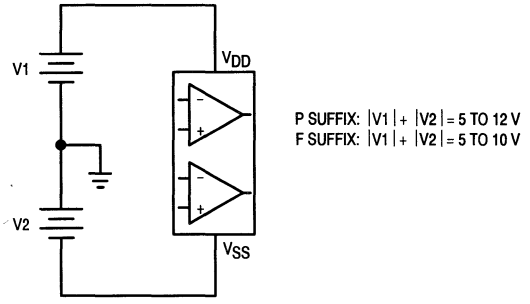


Figure 11. Dual– or Split–Supply Operation

EMI SUPPRESSION

When using ICs in or near television receiver circuits, EMI (electromagnetic interference) and subsequent unwanted display artifacts and distortion are probable unless adequate EMI suppression is implemented. A common misconception is that some offending digital device is the culprit. This is erroneous in that an IC itself has insufficient surface area to produce sufficient radiation. The device, while it is the generator of interfering signals, must be coupled to an antenna before EMI is radiated. The source for the EMI is not the IC which generates the offending signals but rather the circuitry which is attached to the IC.

Potential EMI signals are generated by ***all*** digital devices. Whether they become a nuisance is dependent upon their frequency and whether they have a sufficient antenna. The frequency and number of these signals is affected by both circuit design within the IC and the manufacturing process. Device speed is also a major contributor of potential EMI. Because the design is determined by the anticipated application, the manufacturing process is fixed and the drive for speed ever increasing, the only effective point to implement EMI suppression is in the PC board design. The PC board usually is the antenna which radiates the EMI. The most efficient method of minimizing EMI radiation is to minimize the efficiency of this antenna.

The most common cause of inadequate EMI suppression lies with the ground system of the suspected digital devices. As pointed out previously, di/dt transitions can be significant in digital circuits. If the di/dt transitions appear in the ground system and the ground system is inductive, the harmonics present in these transitions are a source of potential EMI signals. The unfortunate result of putting digital devices on a reactive ground system is guaranteed EMI problems.

If a single unbroken plane can be devoted to the ground system, EMI can usually be sufficiently suppressed by using ferrite beads on suspect EMI paths and decoupling with adequate values of capacitors. The value of the decoupling capacitor depends on the frequency and amplitude of the offending signals. Ferrite beads are available in a wide variety of shape, size and material to fit virtually any application.

Choose a ferrite bead for desired impedance at the desired frequency and construct a low pass filter using one or more appropriate capacitors in a "L", "T" or "PI" arrangement. Use only capacitors of low inductive and resistive properties such as ceramic or mica. Install filters in series with each IC pin suspected of contributing offending EMI signals and as close to the pin as possible. Analysis using a spectrum analyzer can help determine which pins are suspect.

Where PC board costs constrain the number of layers available, and if the EMI frequencies are far removed from the frequencies of operation, ferrite beads and decoupling capacitors may still be effective in reducing EMI emissions. Where only two (or in some cases, only one!) layer is used, the ground system is always reactive and poses an EMI problem. If the offending EMI and normal operating frequency differ sufficiently, filtering can still work.

An "island" is constructed in the ground system for the digital device using ferrite beads and decoupling capacitors as shown by the example in Figure 13. The ground must be cut so that the digital ground for the device is isolated from the rest of the ground system. Next choose a ferrite bead of the appropriate value. Install this bead between the isolated ground and the ground system. Install low pass filters in all suspect lines with the capacitor closest to the device pin connected to the isolated ground in all signal lines where EMI is suspect. Also cut the power to the device and insert a ferrite bead as shown in Figure 13. Finally, decouple the device between the power pin(s) and isolated ground pin(s) using a low inductive/resistive capacitor of adequate value.

The methods described above will work acceptably when the EMI frequency and the frequency of operation of the device generating the EMI differ greatly. Where the EMI is disturbing the high VHF or UHF channels and the device generating the EMI is operating within the NTSC/PAL bandwidth, the energy contained in the harmonics generating the EMI is situated well above the operating frequency and suppressing this type of EMI poses no great problem. However, if the EMI is present on low VHF channels and/or the operation of the device is outside the NTSC/PAL bandwidth, such as a 2X pixel clock or 4xfsc oscillator, compromise between video quality and suppression complexity is usually required to obtain an acceptable solution. For those cases where the operating frequency of the device is very near the frequency of the EMI disturbance, careful attention to PCB layout, multiple layer PCB and even shielding may be necessary to obtain an acceptable design.

The area which should be addressed first as a potential EMI source is the ground. Without an adequate ground system, EMI cannot be effectively reduced by decoupling. If at all possible, the ground should be a complete unbroken plane. Figure 12 shows two examples of relieving ground around device pins. When relieving vias and plated through holes, large areas of ground loss should be avoided. When the relief pattern is equal to half the distance between pins, over etching and process errors may remove ground between pins. If sufficient ground around enough pins are removed, the ground system can become isolated or nearly isolated "patches" which will appear inductive. If ground, such as the vicinity of an IC, must be removed, replace with a cross hatch of ground lines with the mesh as small as possible.

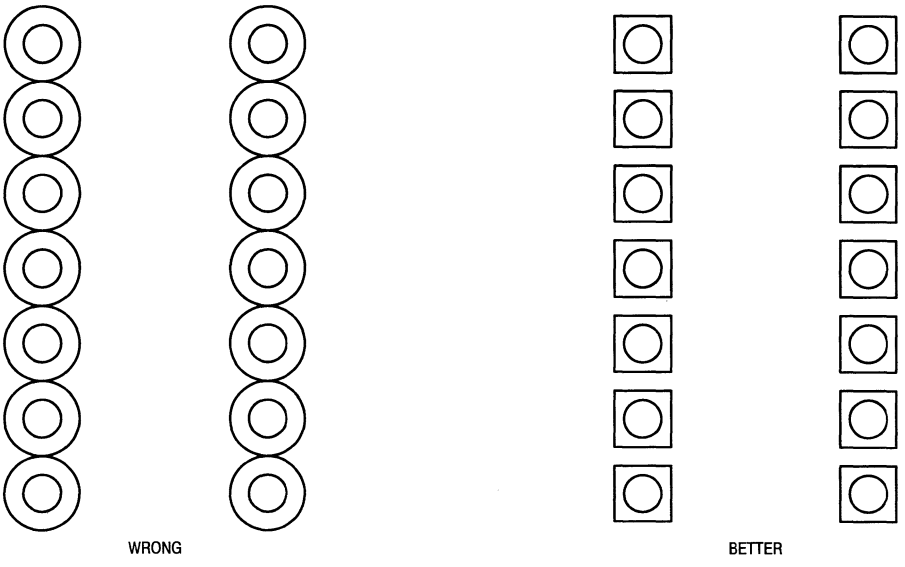


Figure 12.

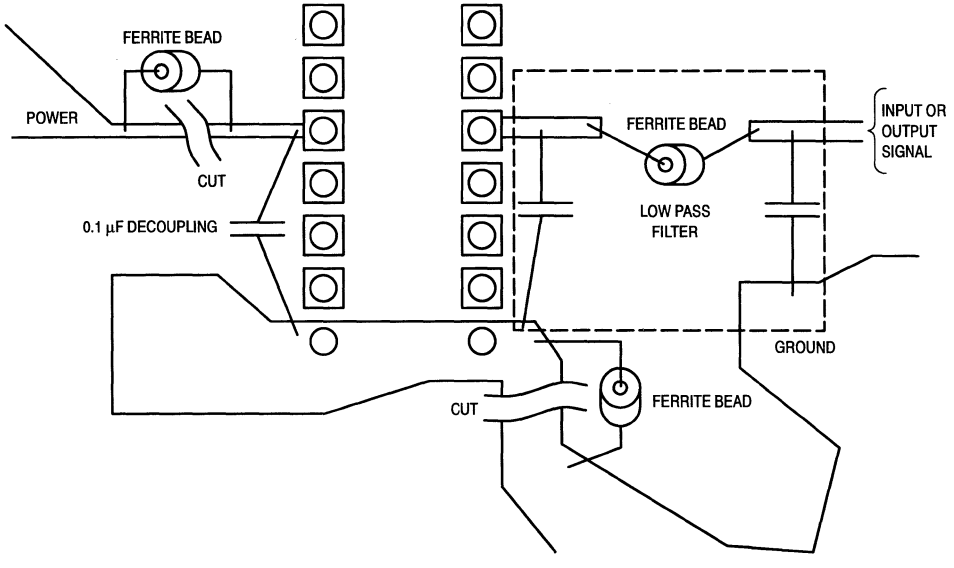


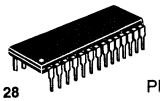
Figure 13.

MC44131

Product Preview

System 4 Improved Stereoton

Single Chip TV Sound Control



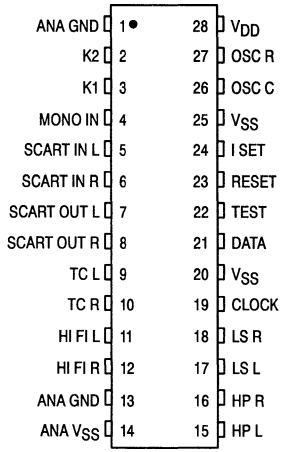
28 1

P SUFFIX
PLASTIC PACKAGE
CASE 710–02

ORDERING INFORMATION

MC44131P DIP

PIN ASSIGNMENT



This single chip performs all the necessary functions for sound control required in a TV receiver in accordance with German standard transmission mode, with NICAM transmission mode, and SECAM transmission mode.

The MC44131 is manufactured in a single chip using Motorola's CMOS process and is an improved version of the MC44130.

- Application: Audio for European Televisions
- Part of Motorola System 4
- Fully Controlled Through IIC Bus
- Accepts Base Band Dual Carrier Signals or NICAM Decoded Signals or SECAM Decoded Signals
- "Pilot Tone" Demodulation and Identification
- Mono, Stereo, Dual Language Processing
- Maximum Stereo Separation Control
- Volume, Treble, and Bass Control
- Special Effects: Pseudo and Extra Wide Stereo
- Mute and Separate Power–On Reset Mute
- Loudspeaker, Headphone, HIFI Outputs
- Peripheral (SCART) Input/Output
- Independent Volume Control Left/Right on Loudspeaker and on Headphone Outputs
- Mono Recorder Drive Capability
- New Switching Matrix Allows 31 Signal Routing Options
- Auxiliary Attenuator to Avoid Clipping when Bass is Boosted

The MC44131 is an improved version of the popular MC44130. It combines all following functions in a 28–pin DIP package:

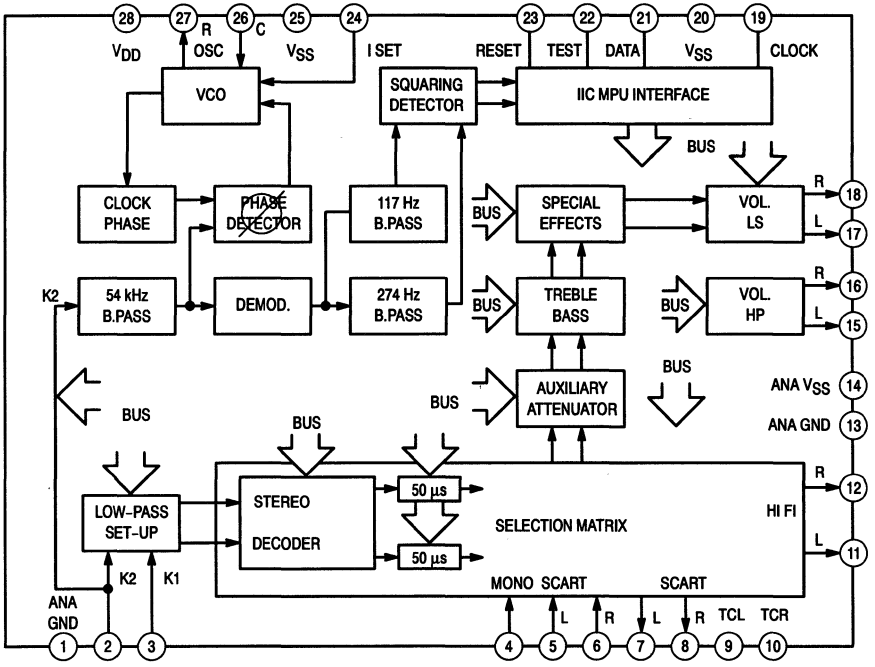
- Pilot Tone Decoding
- Baseband Stereo Signal Decoding
- Signal De–Emphasis
- Direct Balance Adjustment via Software (Set–Up)
- IIC Bus Controlled Routing of Baseband/Monaural/SCART Inputs to Loudspeaker/Headphone/HIFI/SCART Outputs
- Loudspeaker Output Control (Tone, Special Effects, Independent Volume Control Left/Right)
- Headphone Output Control (Independent Volume Control Left/Right)
- Re–Creation of MONO Output on SCART for Mono Recorders

MC44131 has improved MC44130 performances in the following areas:

- Crosstalk Figures
- Enhanced Drive Capability on SCART Output
- Lowered Output Impedance on SCART Output
- Reduced Sensitivity for Identification about 25%
- Introduced Latch on I2C Identification Interface
- New Switching Matrix for Independent Signal Routing (31 Options)
- Auxiliary Attenuator on Front End of Tone Control to Fix Clipping when Bass is Boosted
- Reduced Audio Signal Routing Losses
- Shorter Charge–Up Time on Analog Ground Pin

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 15	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature	T_{stg}	– 40 to + 125	°C

NOTE: Default conditions (unless otherwise specified):

1. All tests performed as per Figure 1.
2. 1% accuracy resistors — resonator Murata CSB437F3 (fs = 427 kHz, fp = 464 kHz, Cstat at kHz = 630 pF, Rs = 30 Ω). V_{DD} = 12 V, T_A = 25°C.
3. Va amplitude is 500 mVrms, Va frequency is 1 kHz, Vr amplitude is 400 mVpp, Vr frequency is 1 kHz, Vp frequency is 54.6875 kHz with or without amplitude modulation.
4. Values for subaddress, data, and read bits have to be understood as hexadecimal values.
5. Treble/Bass: flat = subaddress 05 data 88.
6. Volumes HP and LS: Max. = subaddress 01, 02, 03, 04 data 00.
7. K1, K2 Set–Up: Midrange = subaddress 00, 07 data 20.
8. Demute, matrix option 00, no special effects = subaddress 06 data 00.
9. When switches are not mentioned, they are considered as OFF.
10. Pin 22 is not connected or is connected to Pin 20.

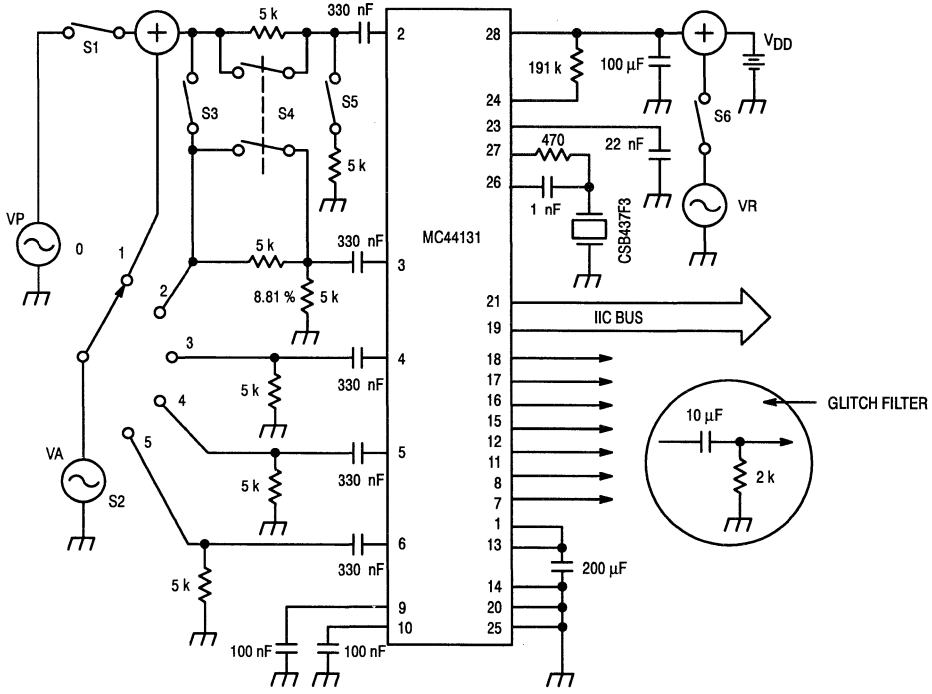


Figure 1. Device Under Test

POWER SUPPLY

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	28		10.8	12	13.2	V
Power Supply Current	I_{DD}	28		—	35	60	mA

OSCILLATOR

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Free Running Frequency	FOSC	27	Decoder and de–emphasis switched OFF	430	437.5	450	kHz

2

IDENTIFICATION

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Minimum Modulation	LMPA	2, 27, 19, 21	Pilot amplitude from 50 mVpp to 500 mVpp before AM modulation (see also Note 2)	—	30	40	%
Maximum Modulation				60	—	—	%

VOLUME CONTROLS

Left and right outputs may be balanced at any level to within half step size by independent control of left/right side attenuators.

LOUDSPEAKER (See Note)

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Step Size from Step 0 to Step 50*	LSSS	6, 17, 18	Subaddr. 01, 02 Data n –>$V_{out}(n)$ Subaddr. 01, 02, Data n+1 –>$V_{out}(n+1)$ LSSS = $\lvert 20 \log (V_{out}(n)/V_{out}(n+1)) \rvert$	0	1.25	2.5	dB
Depth from Step 0 to Step 50*	LSDL	6, 17, 18	Subaddr. 01, 02 Data 32 –>$V_{out}(32)$ LSDL = $\lvert 20 \log (V_{out}(0)/V_{out}(32)) \rvert$	55	60	70	dB
Depth at Step 62*	LSDL	6, 17, 18	Subaddr. 01, 02 Data 3E –>$V_{out}(3E)$ LSDL = $\lvert 20 \log (V_{out}(0)/V_{out}(3E)) \rvert$	65	—	—	dB

NOTE: For all loudspeaker volume control tests, channel left and right are at the same step. Subaddress 06 data 01, S2 = 5.
* Step values understood as decimal values.

HEADPHONE (See Note)

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Step Size from Step 0 to Step 25*	HPSS	5, 15, 16	Subaddr. 03, 04 Data n –>$V_{out}(n)$ Subaddr. 03, 04 Data n+1 –>$V_{out}(n+1)$ HPSS = $\lvert 20 \log (V_{out}(n)/V_{out}(n+1)) \rvert$	0	2.5	4.0	dB
Depth from Step 0 to Step 25*	HPDP	5, 15, 16	Subaddr. 03, 04 Data 00 –>$V_{out}(00)$ HPDP = $\lvert 20 \log (V_{out}(00)/V_{out}(19)) \rvert$	55	60	70	dB
Depth at Step 30*	HPDP	5, 15, 16	Subaddr. 03, 04 Data 1E –>$V_{out}(E)$ HPDP = $\lvert 20 \log (V_{out}(0)/V_{out}(1E)) \rvert$	60	—	—	dB

NOTE: For all headphone volume control tests, channel left and right are at the same step. Subaddress 06 data 01, S2 = 4.
* Step values understood as decimal values.

K1, K2 SET–UP CONTROL (See Note)

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Control Range	SUD	2, 3, 7, 8	Subaddr. 06, Data: 05 Subaddr. 00, 07 Data: 3E $V_{out}(3E)$ Subaddr. 00, 07 Data: 00 $V_{out}(00)$ SUD = $\lvert 20 \log (V_{out}(3E)/V_{out}(00)) \rvert$	3.5	4.5	5.5	dB
Step Size K2	SSK2	2, 3, 8	Subaddr. 06, Data: 05 Subaddr. 07, Data: 00 ... 3F	0	0.1	0.2	dB
Step Size K1	SSK1	2, 3, 7	Subaddr. 06, Data: 05 Subaddr. 00, Data: 00, 02 ... 3E	0	0.2	0.4	dB
Stereo Separation Set–Up at K1/K2 Mid.	SUSM	2, 3, 7, 8	Subaddr. 06, Data: 00 Subaddr. 00, 07, Data: 20 $V_{out}L$ on Pin 7, $V_{out}R$ on Pin 8 SUSM = $\lvert 20 \log (V_{out}L(20)/V_{out}R(20)) \rvert$	20	40	—	dB
Stereo Separation Set–Up Optimized	SUSO	2, 3, 7, 8	Subaddr. 06, Data: 00 Subaddr. 00, Data: 20 Subaddr. 07, Data: n SUSO = $\lvert 20 \log (V_{out}L(n)/V_{out}R(20)) \rvert$	40	50	—	dB

NOTE: S2 = 2, S3 = ON, S4 = ON. V_{out} is measured on Pins 7 and 8 for K1 and K2, respectively. K1/K2 set–up control may also be used to equalize gains in dual language mode.

DE–EMPHASIS

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
De–Emphasis	DMP	2, 3, 7, 8	V_p = 50 mVrms, S1 = ON, S2 = 1, 2 S4 = ON, S5 = ON Subaddr. 06 Data 05, V_{out} measured on Pin 7, 8 DMP = $\lvert 20 \log (V_{out}(200\ Hz)/V_{out}$ (10 kHz)) $\rvert$	9.8	10.3*	10.8	dB

* Corresponding to 50 µs time constant (± 7%; 46.5 µs, 53.5 µs).

SPECIAL EFFECTS

PSEUDO–STEREO

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Frequency for 180° Phase Shift	FREO	5, 17, 18	Subaddr. 06 data 22 Input frequency V_A for phase shift of 180° between V_{out} on Pins 17, 18 respectively	1.2	1.25	1.4	kHz
Amplitude	PSA	5, 18	Subaddr. 06 Data 02: $V_{out}N$ Subaddr. 06, Data: 22: $V_{out}PS$ PSA = $\lvert 20 \log (V_{out}PS/V_{out}N) \rvert$	—	0.1	0.6	dB
	VARI		For frequencies up to 15 kHz			3.0	dB

EXTRA–WIDE (See Notes)

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Direct Gain Left	LLA	5, 6, 17, 18	LLA = (V_{out}LL/V_{out}NL) x 100	110	120	130	%
Direct Gain Right	RRB	5, 6, 17, 18	RRB = (V_{out}RR/V_{out}NR) x 100	110	120	130	%
Left to Right CC	LRC	5, 6, 17, 18	LRC = (V_{out}NR x V_{out}LR) x 100/ (V_{out}NL x V_{out}RR)	48	54	60	%
Right to Left CC	RLD	5, 6, 17, 18	RLD = (V_{out}NL x V_{out}RL) x 100/ (V_{out}NR x V_{out}LL)	48	54	60	%
High Pass Filter	HPLR	5, 6, 17, 18	HPLR = 20 log ((V_{out}LR x V300NL) / (V_{out}NL x VhLR))	2.8	3.2	3.6	dB
High Pass Filter	HPRL	5, 6, 17, 18	HPRL = 20 log ((V_{out}RL x V300NR) / (V_{out}NR x VhpRL))	2.8	3.2	3.6	dB

NOTES:
Subaddress 06 Data 00
* Fva = 300 Hz
  – S2 = 4 output Pin 17: V300NL
  – S2 = 5 output Pin 18: V300NR
* Fva = 1 kHz
  – S2 = 4 output Pin 17: V_{out}NL
  – S2 = 5 output Pin 18: V_{out}NR

Subaddress 06 Data 10
* Fva = 300 Hz
  – S2 = 4 output Pin 18: VhpLR
  – S2 = 5 output Pin 17: VhpRL
* Fva = 1 kHz
  – S2 = 4 output Pin 17: V_{out}LL
  – S2 = 4 output Pin 18: V_{out}LR
  – S2 = 5 output Pin 17: V_{out}RL
  – S2 = 5 output Pin 18: V_{out}RR

EXTRA–WIDE AND PSEUDO–STEREO (See Notes)

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Left to Right CC	LRBT	5, 6, 17, 18	LRBT = 100 (VspNR x VspLR) / (VspNL x VspRR)	32	37	42	%
Right to Left CC	RLBT	5, 6, 17, 18	RLBT = 100 (VspNN x VspRL) / (VspNR x VspLL)	32	37	42	%

NOTES:
Fva = 1 kHz; Subaddress 06 Data 00
S2 = 4, output on Pin 17: VspNL
S2 = 5, output on Pin 18: VspNR

Subaddress 06 Data 30
S2 = 4, output on Pin 17: VspLL
and output on Pin 18: VspLR
S2 = 5, output on Pin 17: VspRL
and output on Pin 18: VspRR

DISTORTION

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Distortion	DIST	2, 3 4 5, 6 7, 8 11, 12 15, 16 17, 18	For all selected matrix options. DIST is defined for each output by: DIST = 100 X (Vharm/Vtot) where Vtot is measured on the output corresponding to the selected input (see S2 and the switching matrix table 1) with a low pass filter at 15 kHz and Vharm is measured on the same output with a high Q band pass filter from 2 kHz to 15 kHz.	— —	0.2 0.4*	0.5 —	%

* Depending on Matrix Option.

GLITCH

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Glitch on Outputs When Changing Volume Control	GLU	7, 8, 11, 12, 15, 16, 17, 18	S5 = ON, use a first order RC high pass filter with a frequency cut–off about 10 Hz as per Figure 5. For the first four steps: For the next four steps: For the remaining steps:	 — — —	 — — —	 5 3 1	mVpp
DC Level Change When Changing Matrix Option		7, 8, 11, 12, 15, 16, 17, 18		—	—	100	mV

OTHER PARAMETERS

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Analog Ground Polarization (see Note 1)	VAGD	1,13	Vpin28 = V_{DD} = 12 V Vpin14 = Vpin20 = Vpin25 = V_{SS} = 0 V Pin 1 and Pin 13 have to be connected together	5			V
Input Output Polarization (see Note 1)	VPOL	2, 3, 4 5, 6, 7, 8, 11, 12, 15, 16, 17, 18	Force VAGD = V_{DD}/2 on Pin 1 and Pin 13 and measure VPOL(n) on each input and output pin	5			V
Input and Output Impedance (see Note 1)			Force Pin 1 and Pin 13 to VAGD = V_{DD}/2. Force tested pin to VPOL(n) – 0.1 V and measure the source current K(n):				
	IKR IR ORS	2,3 4, 5, 6 7, 8	IKR(n) = 0.1/K(n) IR(n) = 0.1/K(n) ORS(n) = 0.1/K(n) except for matrix 03 and 0B	25 150 —	— — —	— — 1	kΩ
	ORA	11, 12 15, 16 17, 18	ORA(n) = 0.1/K(n) ORA(n) = 0.1/K(n) ORA(n) = 0.1/K(n)	— — —	— — —	200 200 200	Ω
Noise			S5 = ON, Bandwidth 20 Hz – 15 kHz				
	NKST	7, 8 11, 12 15, 16	Matrix Option Stereo Input K1 or K2	—	150	—	μVrms
	NKDM	17, 18	Matrix Option Dual or Mono or NICAM Stereo, Input K1 or K2	—	120	—	
	NLMS		Output LS, Input Mono or SCART	—	90	—	
	NOMS		Output SCART and Input Mono or Output HiFi/HP and Inputs Mono/SCART	—	60	—	
	NVCT		Output LS, volctrl step 24 Output HP, volctrl step 12	—	5	—	
PSRR Power Supply Rejection	PSRR	15, 16, 17, 18, 28	S6 = ON, V_{out} measured on each output PSRR = 20 log (V_{out}/Vr)				
			For LS Outputs For Other Outputs	– 10 – 30	– 12 – 40	— —	dB

NOTES:
1. This test measurement is done directly on the device without any external wiring and hardware, excepting short circuit between Pins 1 and 13.
2. Output drive capability when using application circuit is 1 V_{pp} on 10 kΩ for all outputs.

SWITCHING MATRIX TABLE

Selection Code bcdefgh	HEXA Code 3)	Input					Ident Code	Output						Notes
					SCART			LS		HP		SCART		
		MONO	K1	K2	L	R	L R	L	R	L	R	L	R	
STEREO TRANSMISSION														
0XX0100	04	—	(L+R)/2	R	—	—	01	L	R	L	R	L	R	
0XX0011	03	—			—	—	01	L	R	L	R	M*	M*	1
0XX0000	00	—			L°	R°	01	L°	R°	L°	R°	L	R	
1XX0000	40	—			1°	2°	01	1°	1°	1°	1°	L	R	
0XX0010	02	—			1°	2°	01	1°	1°	2°	2°	L	R	
0XX0001	01	—			1°	2°	01	2°	2°	1°	1°	L	R	
1XX0001	41	—			1°	2°	01	2°	2°	2°	2°	L	R	
DUAL LANGUAGE OR MONO TRANSMISSION														
1XX0100	44	—	1	2	—	—	10	1	1	1	1	1	2	
0XX0110	06	—	1	2	—	—	10	1	1	2	2	1	2	
0XX0101	05	—	1	2	—	—	10	2	2	1	1	1	2	
1XX0101	45	—	1	2	—	—	10	2	2	2	2	1	2	
0XX1111	0F	—	1	—	—	—	00	1	1	1	1	1	1	2
0XX0111	07	—	1	2	—	—	10	2	2	2	2	2	2	
0XX1011	0B	—	1	2	—	—	10	2	2	1	1	2	2	
0XX1000	08	—	1	2	L°	R°	10	L°	R°	L°	R°	1	2	
0XX1100	0C	—	1	—	L°	R°	00	L°	R°	L°	R°	1	1	2
1XX1011	4B	—	1	2	L°	R°	00	L°	R°	L°	R°	2	2	
1XX0110	46	—	1	2	1°	2°	10	1°	1°	1°	1°	1	2	
0XX1010	0A	—	1	2	1°	2°	10	1°	1°	2°	2°	1	2	
0XX1001	09	—	1	2	1°	2°	10	2°	2°	1°	1°	1	2	
1XX0111	47	—	1	2	1°	2°	10	2°	2°	2°	2°	1	2	
1XX0010	42	—	1	—	1°	2°	00	1°	1°	1°	1°	1	1	2
0XX1110	0E	—	1	—	1°	2°	00	1°	1°	2°	2°	1	1	2
0XX1101	0D	—	1	—	1°	2°	00	2°	2°	1°	1°	1	1	2
1XX0011	43	—	1	—	1°	2°	00	2°	2°	2°	2°	1	1	2
AM TRANSMISSION														
1XX1100	4C	AM	—	—	L°	R°	—	L°	R°	L°	R°	AM	AM	
1XX1000	48	AM	—	—	1°	2°	—	1°	1°	1°	1°	AM	AM	
1XX1110	4E	AM	—	—	1°	2°	—	1°	1°	2°	2°	AM	AM	
1XX1101	4D	AM	—	—	1°	2°	—	2°	2°	1°	1°	AM	AM	
1XX1001	49	AM	—	—	1°	2°	—	2°	2°	2°	2°	AM	AM	
1XX1111	4F	AM	—	—	—	—	—	AM	AM	AM	AM	AM	AM	

NOTES:

1. M* is the de–emphasized signal of K1, generated in this way:
   (L+R)/2 and R –> L & R –> De–emphasis –> (L+R)/2 = M*
2. Input K1 may be first language or mono information (indent code 10 or 00).
3. With c = d = 0.

REMARKS:

— To output HIFI the same input is fed as to output LS.
— HEXA Code 4A is not used.
— HEXA Codes 00 – 0F and 4C – 4F excepting 07 are compatible with respective codes on earlier versions.

TONE CONTROL

Treble and bass are controlled in 14 steps from minimum to maximum using a 4–bit word for each. Signal alternations are identical on both channels and are realized by variable switched capacitor filters providing very low dispersion characteristics.

In order to prevent clipping of the signal if input amplitude is high and tone control boosts it to values approaching supply voltages, two auxiliary attenuators have been placed on the front end of the tone control circuit, one for the left channel and one for the right.

These attenuators are switched on only if bass boost might generate distortion, i.e., if one of the four highest levels for bass enhancement is selected (steps 11 to 14).

To compensate occurring signal attenuation, volume control on LS output may then be shifted correspondingly to higher levels by means of software control.

Figure 2 shows how the circuit works for one channel.

As a result, up to bass control step 10 (including flat response condition), auxiliary attenuator is disabled. When one of the four last steps is addressed, signal amplitude on the input of the tone control circuit will be reduced (by 2.5/5/7.5 or 10 dB for steps 11, 12, 13, or 14, respectively). On the output, signal loss will only be perceptible if volume control cannot be shifted anymore to sufficiently high values because maximum level is reached. This limitation, however, may avoid generation of amplitudes saturating output amplifiers.

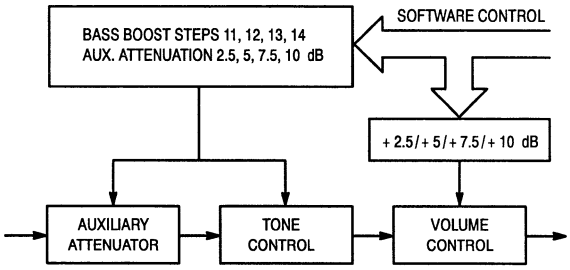


Figure 2.

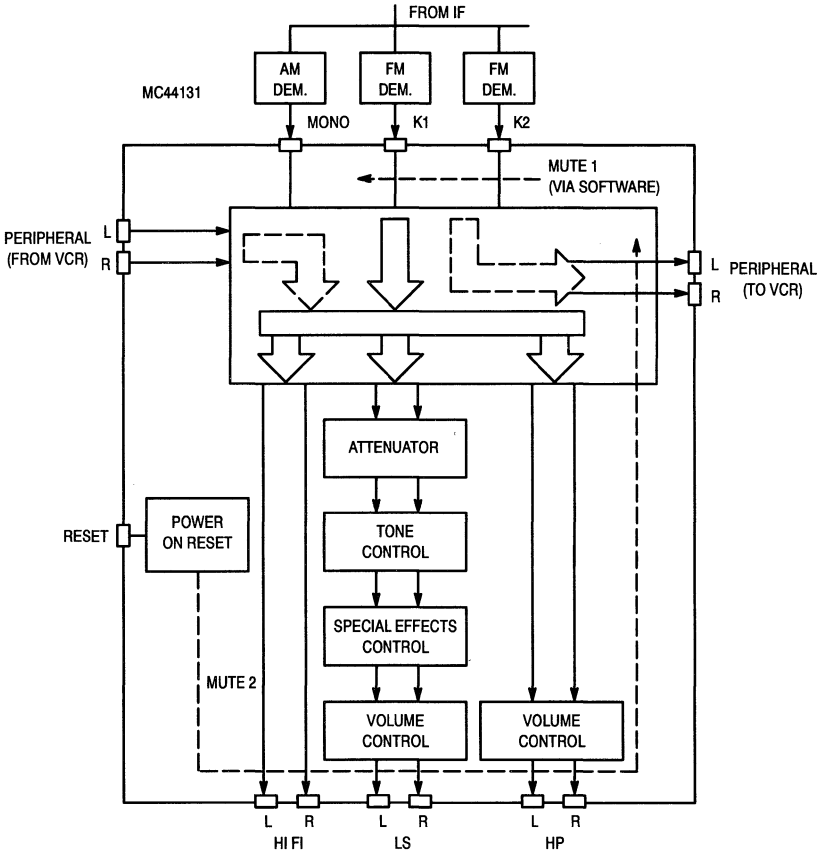


Figure 3. Input/Output Combinations

EMI SUPPRESSION

When using ICs in or near television receiver circuits, EMI (electromagnetic interference) and subsequent unwanted display artifacts and distortion are probable unless adequate EMI suppression is implemented. A common misconception is that some offending digital device is the culprit. This is erroneous in that an IC itself has insufficient surface area to produce sufficient radiation. The device, while it is the generator of interfering signals, must be coupled to an antenna before EMI is radiated. The source for the EMI is not the IC which generates the offending signals but rather the circuitry which is attached to the IC.

Potential EMI signals are generated by ***all*** digital devices. Whether they become a nuisance is dependent upon their frequency and whether they have a sufficient antenna. The frequency and number of these signals is affected by both circuit design within the IC and the manufacturing process. Device speed is also a major contributor of potential EMI. Because the design is determined by the anticipated application, the manufacturing process is fixed and the drive for speed ever increasing, the only effective point to implement EMI suppression is in the PC board design. The PC board usually is the antenna which radiates the EMI. The most efficient method of minimizing EMI radiation is to minimize the efficiency of this antenna.

The most common cause of inadequate EMI suppression lies with the ground system of the suspected digital devices. As pointed out previously, di/dt transitions can be significant in digital circuits. If the di/dt transitions appear in the ground system and the ground system is inductive, the harmonics present in these transitions are a source of potential EMI signals. The unfortunate result of putting digital devices on a reactive ground system is guaranteed EMI problems.

The area which should be addressed first as a potential EMI source is the ground. Without an adequate ground system, EMI cannot be effectively reduced by decoupling. If at all possible, the ground should be a complete unbroken plane. Figure 4 shows two examples of relieving ground around device pins. When relieving vias and plated through holes, large areas of ground loss should be avoided. When the relief pattern is equal to half the distance between pins, over etching and process errors may remove ground between pins. If sufficient ground around enough pins are removed, the ground system can become isolated or nearly isolated "patches" which will appear inductive. If ground, such as the vicinity of an IC, must be removed, replace with a cross hatch of ground lines with the mesh as small as possible.

If a single unbroken plane can be devoted to the ground system, EMI can usually be sufficiently suppressed by using ferrite beads on suspect EMI paths and decoupling with adequate values of capacitors. The value of the decoupling capacitor depends on the frequency and amplitude of the offending signals. Ferrite beads are available in a wide variety of shape, size and material to fit virtually any application.

Choose a ferrite bead for desired impedance at the desired frequency and construct a low pass filter using one or more appropriate capacitors in a "L", "T" or "PI" arrangement. Use only capacitors of low inductive and resistive properties such as ceramic or mica. Install filters in series with each IC pin suspected of contributing offending EMI signals and as close to the pin as possible. Analysis using a spectrum analyzer can help determine which pins are suspect.

Where PC board costs constrain the number of layers available, and if the EMI frequencies are far removed from the frequencies of operation, ferrite beads and decoupling capacitors may still be effective in reducing EMI emissions. Where only two (or in some cases, only one!) layer is used, the ground system is always reactive and poses an EMI problem. If the offending EMI and normal operating frequency differ sufficiently, filtering can still work.

An "island" is constructed in the ground system for the digital device using ferrite beads and decoupling capacitors as shown by the example in Figure 5. The ground must be cut so that the digital ground for the device is isolated from the rest of the ground system. Next choose a ferrite bead of the appropriate value. Install this bead between the isolated ground and the ground system. Install low pass filters in all suspect lines with the capacitor closest to the device pin connected to the isolated ground in all signal lines where EMI is suspect. Also cut the power to the device and insert a ferrite bead as shown in Figure 5. Finally, decouple the device between the power pin(s) and isolated ground pin(s) using a low inductive/resistive capacitor of adequate value.

The methods described above will work acceptably when the EMI frequency and the frequency of operation of the device generating the EMI differ greatly. Where the EMI is disturbing the high VHF or UHF channels and the device generating the EMI is operating within the NTSC/PAL bandwidth, the energy contained in the harmonics generating the EMI is situated well above the operating frequency and suppressing this type of EMI poses no great problem. However, if the EMI is present on low VHF channels and/or the operation of the device is outside the NTSC/PAL bandwidth, such as a 2X pixel clock or 4xfsc oscillator, compromise between video quality and suppression complexity is usually required to obtain an acceptable solution. For those cases where the operating frequency of the device is very near the frequency of the EMI disturbance, careful attention to PCB layout, multiple layer PCB and even shielding may be necessary to obtain an acceptable design.

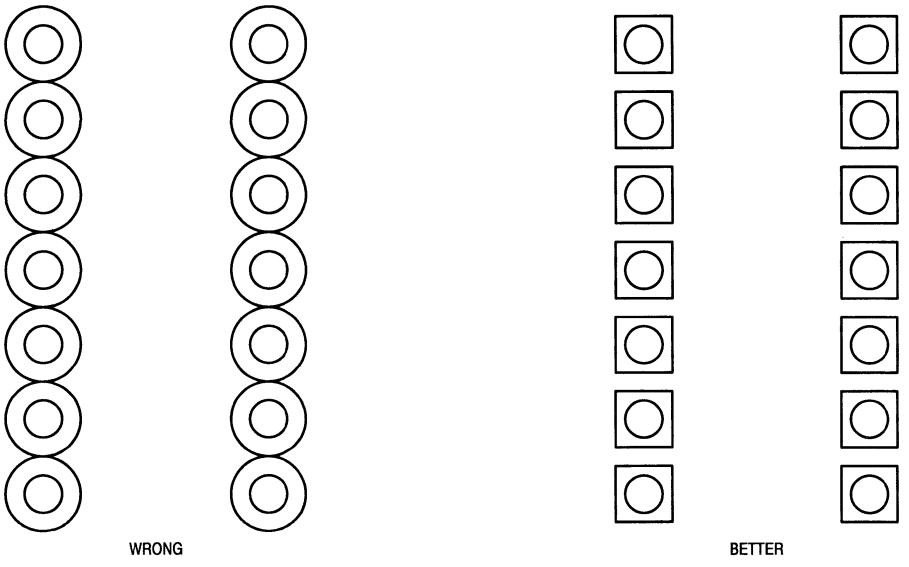


Figure 4.

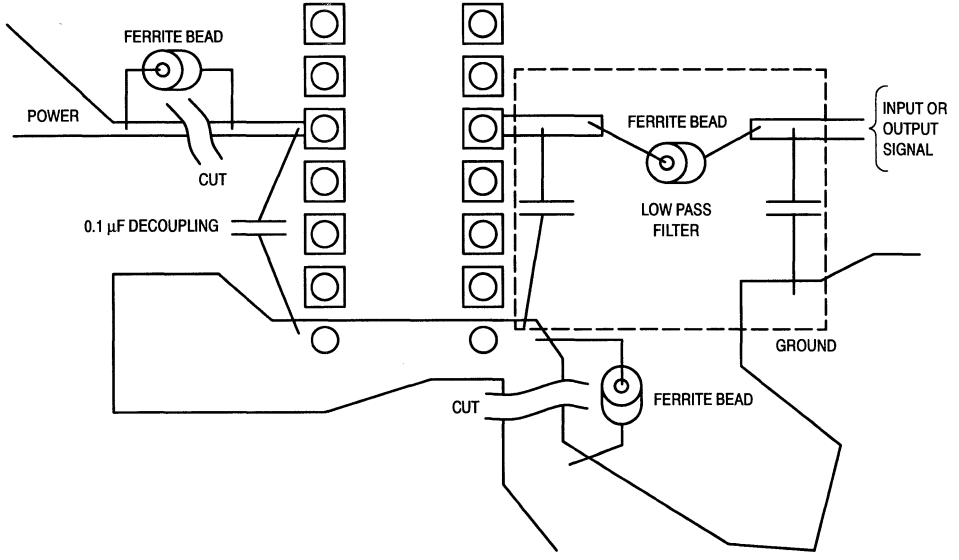


Figure 5.

MC44140

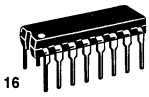
Chroma Delay Line

HCMOS Technology

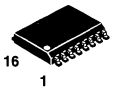
The MC44140 is a monolithic 64 µs delay line, intended for color TV applications. It may be used as a baseband chroma correction circuit (with PAL), or as a chroma delay line (with SECAM).

The device has been designed for use with the MC44000 as part of CHROMA 4, or with the MC44011, but may also be used as a general purpose delay line for other applications.

- Part of SYSTEM 4 Concept
- Works with Baseband Color Difference Signals
- PAL (4.43 MHz)/SECAM/NTSC Capability
- Uses 17.734475 MHz Clock with PAL/SECAM Signals
- 8–Bit Sampling at 1/6 Clock Frequency
- External Inputs (Satellite ....)
- Minimum Number of External Components
- Low Current (35 mA), + 5 V Supply



P SUFFIX
PLASTIC PACKAGE
CASE 648–08

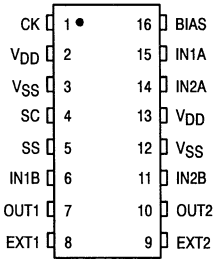


DW SUFFIX
PLASTIC PACKAGE
CASE 751G–02

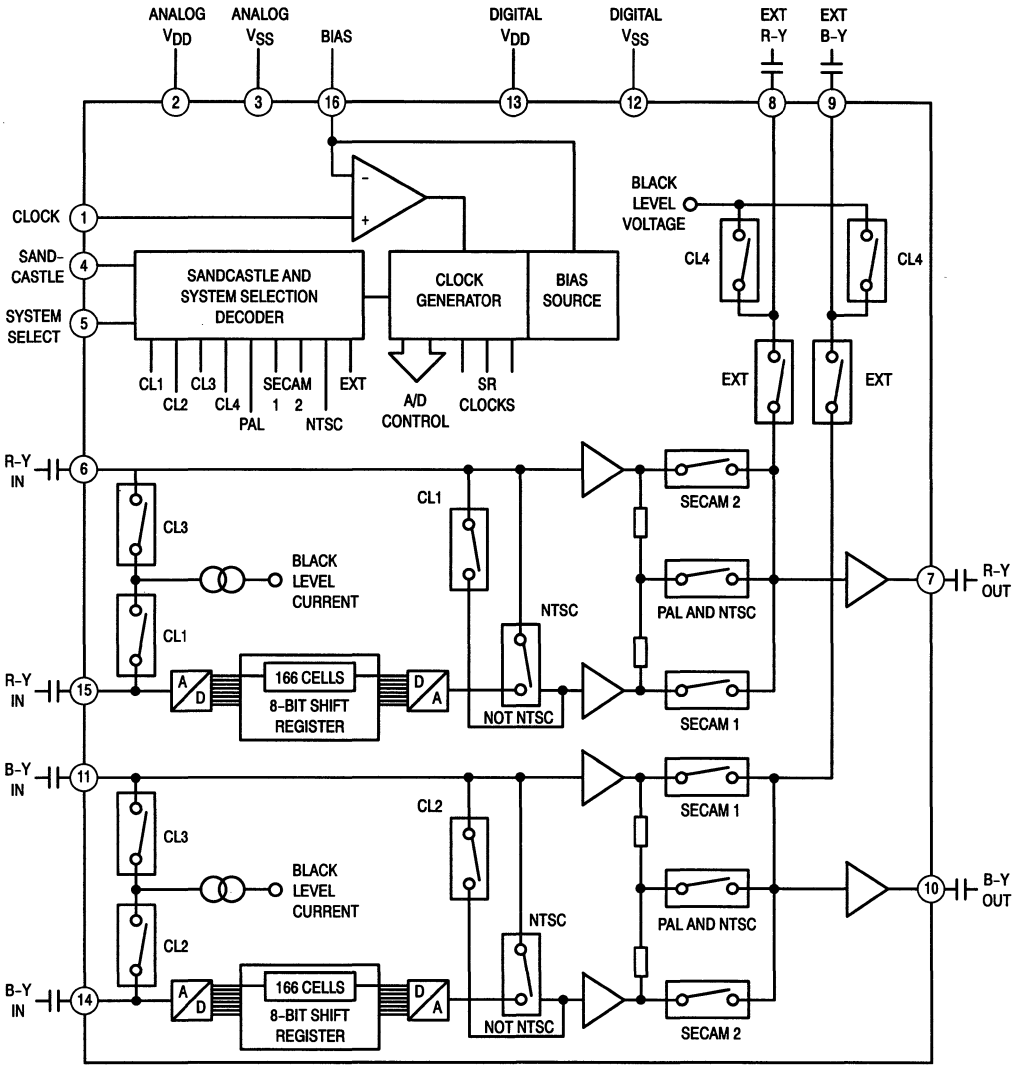
ORDERING INFORMATION

MC44140P	Plastic DIP
MC44140DW	SO–L

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin	Symbol	Function
2	V_{DD}	Positive supply voltage.
3	V_{SS}	Supply ground.
1	CK	System clock. Supplied from MC440XX master clock. Either 17.734475 MHz (PAL and SECAM) or 14.31818 MHz (NTSC) sine wave.
5	SS	System selection. 4–level signal supplied by MC440XX to indicate whether color difference signals are PAL, NTSC, SECAM, or EXTERNAL.
4	SC	Sandcastle pulse. Periodic multi–level signal supplied by MC440XX. The pulse has 4 levels to indicate the timing of black level, ident. gate, and active signal, together with a level changing every other line. Used to control the clamps and for the timing of the SECAM switching.
15 14	IN1A IN2A	R–Y (IN1) and B–Y (IN2) inputs to the A/D converters. Baseband color difference (0 to 1.2 MHz) signals supplied by MC440XX via external coupling capacitors of a value greater than 560 nF; these may originate from PAL, NTSC, or SECAM systems.
6 11	IN1B IN2B	From same source as the "A" inputs but using separate 100 nf coupling capacitors to the direct (un–delayed) inputs.
8 9	EXT1 EXT2	External R–Y (EXT1) and B–Y (EXT2) inputs. These are baseband color difference signals which are ac coupled via 10 nF capacitors from an external source.
7 10	OUT1 OUT2	R–Y (OUT1) and B–Y (OUT2) outputs. The "corrected" baseband color difference signals are returned to MC440XX via external 10 nF capacitors.
16	BIAS	Bias current. A bias current is fed to this pin by means of an external pull–up resistor of 68 kΩ, in order to set the dc operating point of the operational amplifiers. An external decoupling capacitor to GND of 10 nF is required.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	0 to 70	°C
Storage Temperature	T_{stg}	– 65 to + 150	°C
Package Power Dissipation	P_D	500	mW

GENERAL ELECTRICAL CHARACTERISTICS

Parameter	Pin	Min	Typ	Max	Unit
Supply Voltage (Maximum ripple 200 mVpk–pk at 50/100 Hz)	2, 13	4.75	5.0	5.5	V
Operating Current	2, 3	30	35	50	mA
Operating Power Dissipation (Ext. resistor: R BIAS = 68 kΩ)		143	175	275	mW

BIAS CURRENT (BIAS)

Parameter	Pin	Min	Typ	Max	Unit
Current (Ext. resistor; R BIAS = 68 kΩ)	16	—	60	—	µA

CLOCK INPUT (CK)

Parameter		Pin	Min	Typ	Max	Unit
Frequency	PAL/SECAM NTSC	1	— —	17.734475 14.318180	— —	MHz
Amplitude (Sinusoidal signal)		1	50	—	1000	mVpp

CLAMP

Parameter		Pin	Min	Typ	Max	Unit
Clamp Current (Absolute Value)	Sinked if V_{in} > Vclamp) Sourced if V_{in} < Vclamp	6, 11 14, 15	10 80	25 150	40 220	µA
Clamp Voltage (VCLAMP)		8, 9	1.3	1.4	1.5	V

DELAYED SIGNAL CHARACTERISTICS

Parameter		Min	Typ	Max	Unit
Sampling Frequency (Sixth of CK frequency)		—	2.95	—	MHz
Number of Samples (Per line period and per signal)		166	166	166	
Resolution		7	—	8	bit
Delay Value (Equal to sandcastle period for PAL/NTSC or to half this period for SECAM)		—	64	—	µs
Gain		– 0.9	0.0	0.9	dB
Gain Mismatch Between the Two Lines		—	—	2	%
Gain Mismatch Between Direct and Delayed Signals		—	—	2	%
Impedance	Input Output	10 k —	— 220	— —	Ω
Non–Linearity	Differential Integral	— —	— —	± 1 ± 2	LSB %

COLOR DIFFERENCE INPUT SIGNALS (IN1A, IN1B, IN2A, and IN2B)

Parameter		Pin	Min	Typ	Max	Unit
B–Y Voltage Range (peak to peak)		6, 15	—	—	1.8	V
R–Y Voltage Range (peak to peak)		11,14	—	—	1.8	V
DC Level (Relative to black level) (For SECAM only; when R–Y, B–Y absent)			– 0.3	—	+ 0.3	V
Bandwidth			0.0	—	1.2	MHz
Line Period	625–Line Systems 525–Line Systems		61.7 63.0	64.0 63.5	66.7 64.0	µs
Active Signal Duration	625–Line Systems 525–Line Systems		— —	52.0 51.6	— —	µs
Black Level Duration	PAL/NTSC 625–Line PAL/NTSC 525–Line SECAM		— — —	12.0 11.9 6.0	— — —	µs

SANDCASTLE TIMING CHARACTERISTICS (Pin 4)

Parameter		Min	Typ	Max	Unit
Signal Period	PAL/NTSC 625–Line PAL/NTSC 525–Line SECAM	— — —	64.0 63.5 128.0	— — —	µs
Level "0" Duration	PAL/NTSC 625–Line or SECAM 1 PAL/NTSC 525–Line	— —	54.0 53.5	— —	µs
Level "1" Duration (only for SECAM 2)		—	54.0	—	µs
Level "2" Duration		—	5.0	—	µs
Level "3" Duration		—	5.0	—	µs
Safety Margin Between Start/Finish of Active Signal and Start/Finish of Level "0" or Level "1"		0.0	1.0	2.0	µs

FUNCTIONAL DESCRIPTION

The MC44140 has been designed and is intended as a companion device to the MC440XX decoders. As such the MC44140 is used as a baseband chroma correction circuit with PAL, and as the one line delay for SECAM. The device is also compatible with NTSC color difference signals which do not require any correction, and has the facility for routing external R–Y and B–Y signals (e.g., from satellite or from field store feature systems).

The block diagram for the MC44140 appears at the beginning of this document. The baseband color difference signals are derived in the MC440XX by demodulation of the chrominance part of the video signal. They are then ac coupled into the MC44140 and black level clamped. Each of the channels has a direct path and a path containing a delay of one line (64 µs). The clamped signals from pins 14 and 15 are taken from the input and A/D converted to a 8–bit wide digital data stream; this then passes through shift registers containing 166 cells in order to realize the one line delay. After this, the data is converted back into analog signals by means of D/A converters. The clocks for the converters are derived by dividing by 6 the frequency obtained from the CHROMA 4 master oscillator, which consists of a crystal running at 17.734475 MHz for PAL and SECAM. Timing of the switches and clamps in the circuit is achieved by means of a special sandcastle pulse provided by the MC440XX. Mode selection is also undertaken by the MC440XX by means of a 4 voltage level output supplied to pin 5.

Color difference signals provided by the MC440XX may originate from any one of PAL, SECAM, or NTSC, so the treatment of these incoming signals is different according to the mode selected; as determined by the SYSTEM SELECT level emanating from the MC440XX. Referring to the block diagram, it is possible to follow the procedure adopted for each standard. The clamping action may be interpreted in each case from Figures 1 thru 4.

In the case of PAL signals, black level clamps CL1 and CL2 are in use every line. Considering only the R–Y channel, it will be seen that the signal is ac coupled into the circuit at pin 6 (direct) and pin 15 (delayed). CL1 clamps the input at pin 15 to the BLACK LEVEL VOLTAGE, this signal then passes through the delay line. The second CL1 clamp uses the dc level present after the delay line to clamp the black level of the direct path. The two signals are then buffered and averaged together, and the result is switched through to the output at pin 7.

For NTSC color difference signals, black level clamps CL1, 2 and 3 are all in use on every line. Again considering the R–Y channel, the inputs at pins 6 and 15 are both clamped to BLACK LEVEL VOLTAGE by CL1 and CL3. The delayed path is now switched out of circuit, however, as this is not required with NTSC. The direct path only is then routed to the output at pin 7.

The nature of the SECAM color difference signals is somewhat different from the other standards in that the signal is only present on every other line as is indicated in Figure 3. For the R–Y channel, the delayed path input is clamped to BLACK LEVEL VOLTAGE by CL1 at pin 15. The direct path signal is clamped by the other CL1 switch to the dc level of the delayed path (including any offsets) to ensure there is no difference in clamping level between the two paths. During the period "SECAM 1", the B–Y signal is present and this is clamped to the delayed path dc level. Switch SECAM 1 is closed during this time and so the direct signal passes straight to the output. During the next line period (SECAM 2) there is no direct path signal; now switch SECAM 2 is closed and switch SECAM 1 is open. Therefore, the delayed path signal is now switched through to the output. For the R–Y channel the exact reverse process will occur as in this case the direct path signal is present during the "SECAM 2" lines.

When EXT R–Y and B–Y signals are used, these are assumed to be always "corrected" from whichever source they originate. These signals are ac coupled into the circuit at pins 8 and 9 and are switched straight through to the outputs, using clamps CL4 to set the black level voltage of the two channels line by line.

SIGNALS SUPPLIED BY MC440XX DECODERS

Sandcastle Pulse

This is a multi–level line repetitive timing pulse input to pin 4 of the IC. The signal provides timing commands to the clamp circuits CL1, CL2, CL3, and CL4 and is also necessary for the clock generator to indicate the beginning of active signal storage. The pulse train contains a level changing at half line rate which is used to control the switches SECAM 1 and SECAM 2 when the circuit is operating in the SECAM mode. Tables 1 and 2 explain the meaning of the different levels as used with the sandcastle pulse. It should be noted that "level 1" of the pulse is only used for line by line switching in SECAM mode.

System Selection Signal

This input may have any one of four different dc voltage levels and is used to command the functioning of the NTSC, PAL and NTSC, SECAM 1, SECAM 2 and EXT switches of the block diagram for the four possible modes of operation. For the SECAM mode this signal together with the sandcastle pulse command switches SECAM 1 and SECAM 2. The significance of the different levels is given in Table 3.

Input Color Difference Signals

The general appearance of the baseband inputs as derived from the MC440XX with a color bars input, is shown in Figures 1 thru 4. Each of the color difference signals has two ac coupled inputs to the MC44140. The line period is 64 µs for 625 line systems and 63.5 µs for 525 line systems. Whichever line standard is in use, only about 52 µs of active signal time needs to be stored and delayed for one line period for processing.

The PAL and NTSC inputs are both present at the same time on every line and black level is provided during the whole of the line blanking period (sandcastle periods 2 and 3) to serve as a reference for the active signal. With SECAM only one color difference signal is provided on any given line by the MC440XX, while the other is replaced by a dc level for the duration of that line period. On the following line the sequence is then reversed. For the signal provided, black level is supplied during blanking time minus the ident. gate period (i.e., sandcastle period 3 only).

Output Color Difference Signals

Whatever the origin of the input signals, the two outputs supplied at pins 7 and 10 are always corrected signals which are then ac coupled back to the MC440XX. Black level is pro-

vided during the whole line blanking period to allow the MC440XX to clamp the signals on the other end of the external output coupling capacitors.

Differential Clock Input

Pins 1 and 16 form a differential clock input of high sensitivity and good noise rejection. Pin 16 is an ac ground of the differential input and must be decoupled to ground.

APPLICATION CIRCUIT

A schematic diagram of the MC44140 application circuit is shown in Figure 5. All of the inputs/outputs shown on the left of the diagram have the MC44000 as their destination. The 17.7 MHz and 14.3 MHz crystals shown in fact form part of the MC44000 circuit; this device controls the crystal selection and applies the drive to it. The majority of the rest of the circuit consists of coupling capacitors for the signal inputs and outputs, whose function for black level clamping has already been described. A pull–up resistor is connected to pin 16 for the purpose of providing a bias current, which the IC uses to set the dc operating point of internal operational amplifiers.

Separate power supply pins (V_{DD} and V_{SS}) are provided to each of the analog section and the digital section of the chip. Both of the + 5 V supply pins are filtered using a series resistor and small ceramic and electrolytic capacitors mounted close by each supply pin and its adjacent ground pin. The supplies, especially the analog pin, should be very well bypassed in order to avoid noise interfering with the clock input (pin 1), whose input level is only some 50 mVp–p.

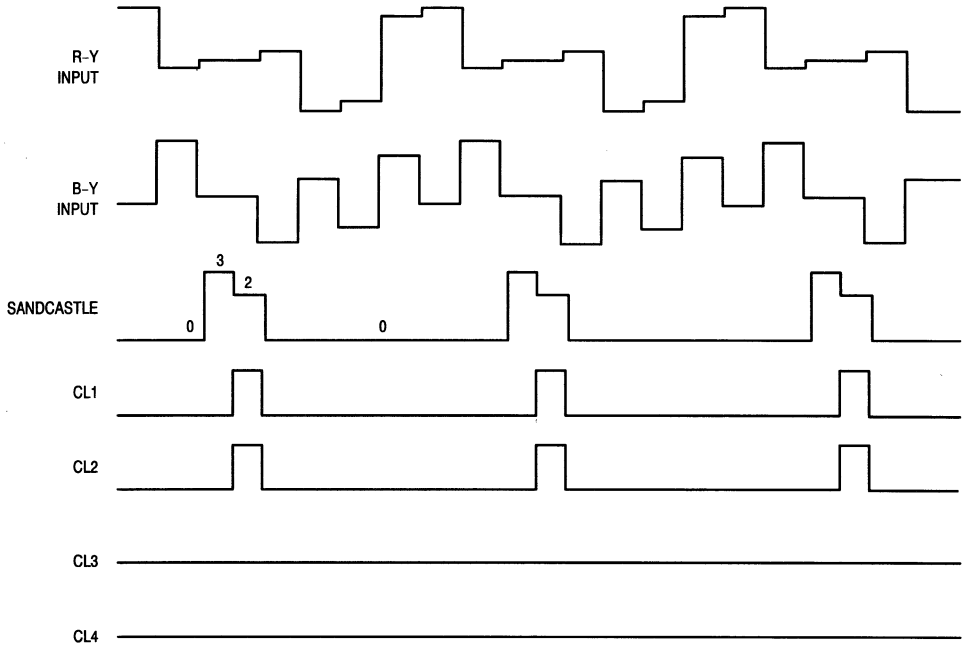


Figure 1. PAL

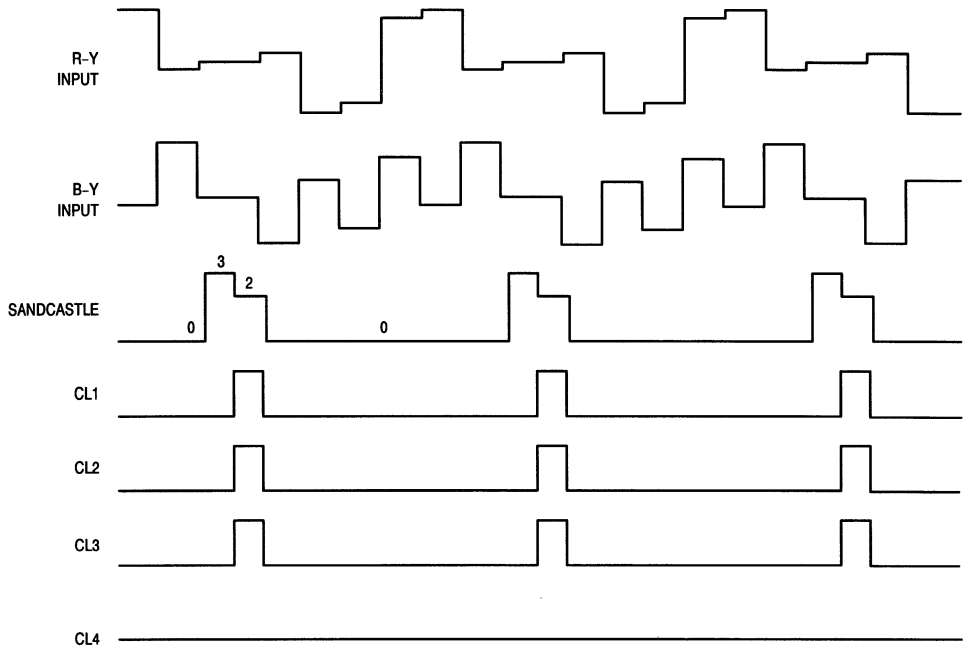


Figure 2. NTSC

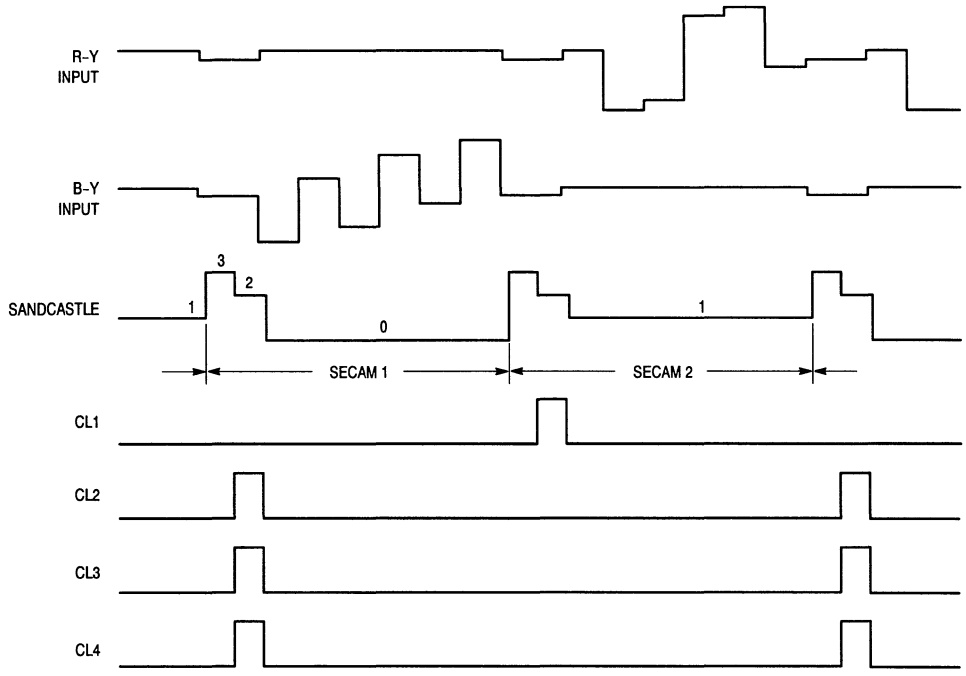


Figure 3. SECAM

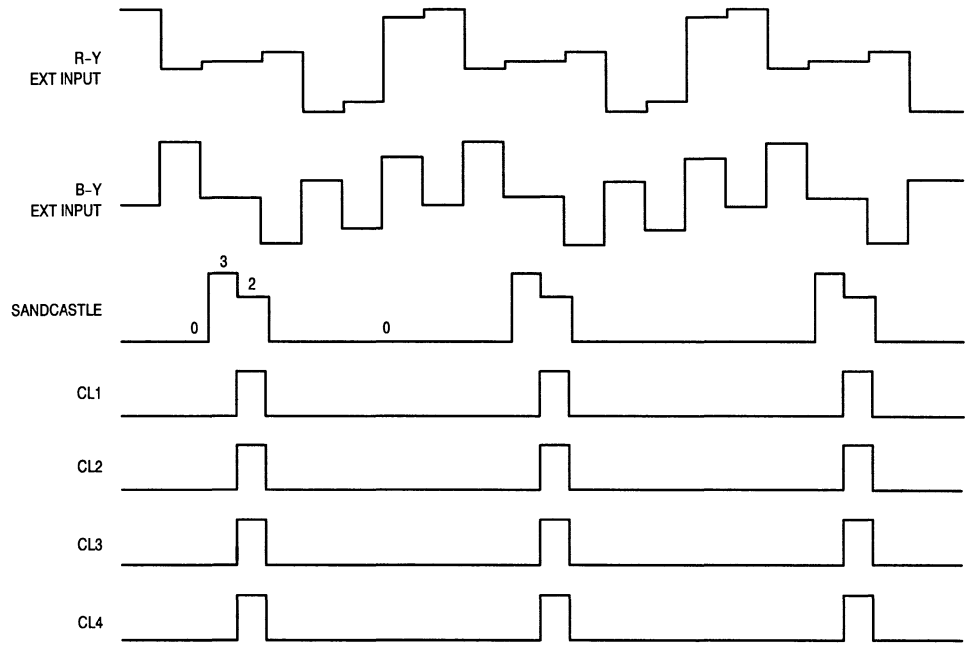


Figure 4. EXT

Table 1. Sandcastle Ident. Pulse for PAL/NTSC

Level	Meaning	Typical Duration µs	Range (V_{DD} = 5.00 V)	
			Lower Limit	Upper Limit
3	Black Level	5.0	3.67 V	5.00 V
2	Black Level	5.0	2.34 V	3.27 V
0	Active Signal PAL NTSC	54.0 53.5	0.00 V —	0.50 V —

2

Table 2. Sandcastle Ident. Pulse for SECAM

Level in Chrono–logical Order	Typical Duration µs	Meaning		Line Period	Range (V_{DD} = 5.00 V)	
		B–Y Input	R–Y Input		Lower Limit	Upper Limit
3	5.0	Black Level	DC Level		3.67 V	5.00 V
2	5.0	Ident. Gate	DC Level		2.34 V	3.27 V
0	54.0	Active Signal	DC Level	SECAM 1	0.00 V	0.50 V
3	5.0	DC Level	Black Level		3.67 V	5.00 V
2	5.0	DC Level	Ident. Gate		2.34 V	3.27 V
1	54.0	DC Level	Active Signal	SECAM 2	0.90 V	1.94 V

Table 3. System Selection

Level	Meaning	Typical Voltage	Range (V_{DD} = 5.00 V)	
			Lower Limit	Upper Limit
0	PAL	0.00 V	0.00 V	0.50 V
1	NTSC	1.40 V	0.90 V	1.94 V
2	SECAM	2.50 V	2.34 V	3.27 V
3	EXTERNAL	5.00 V	3.67 V	5.00 V

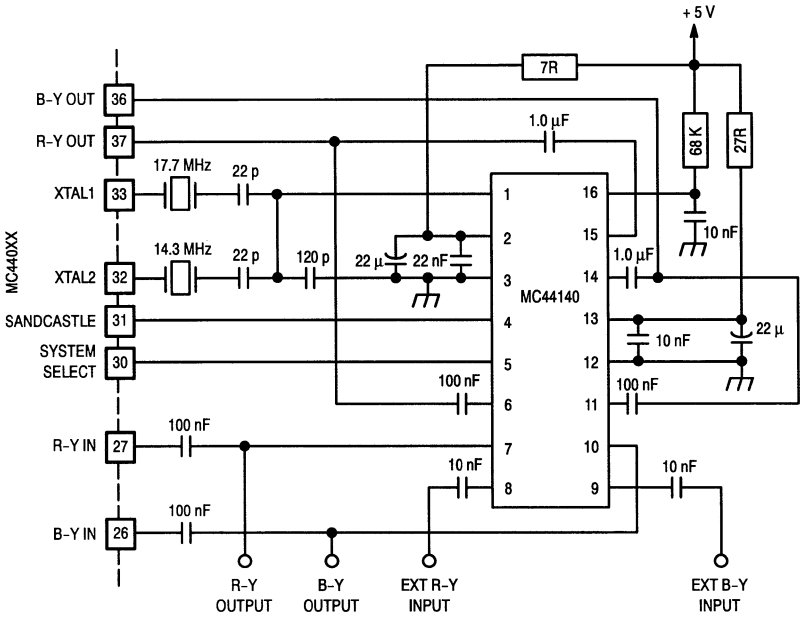


Figure 5. Application Circuit

Advance Information

Triple 8-Bit Video DAC

CMOS

MC44200

FU SUFFIX
QFP PACKAGE
CASE 824A–01

ORDERING INFORMATION

MC44200FU	44 Pin QFP

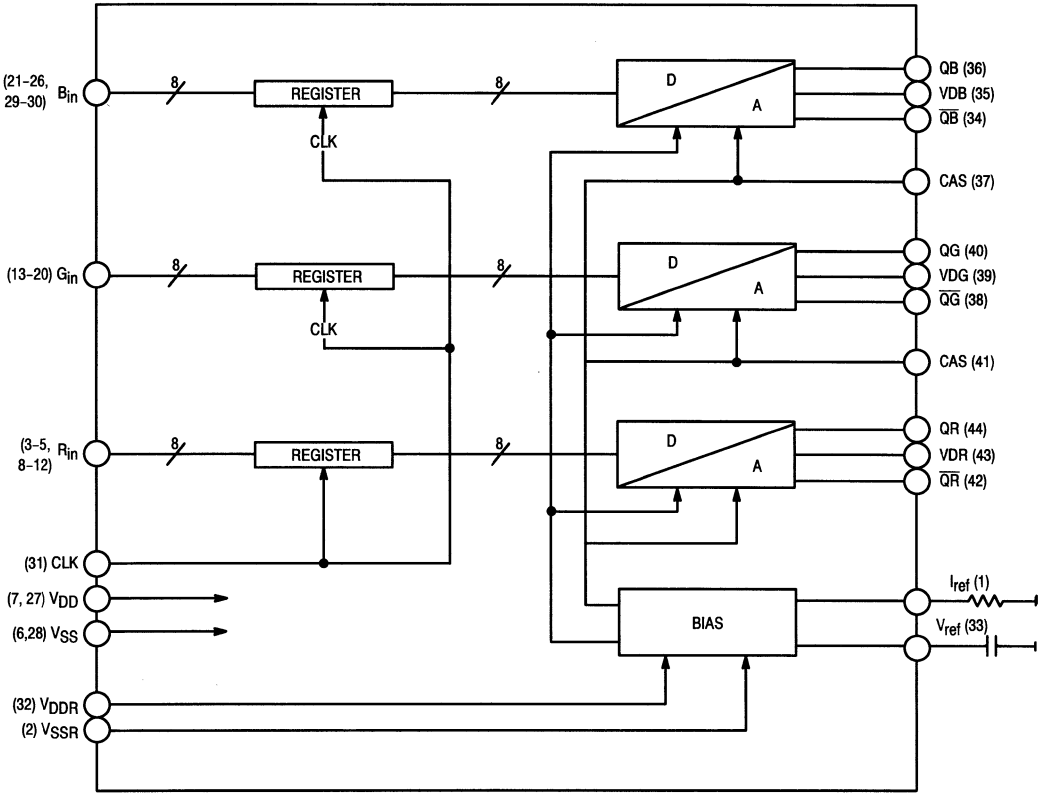
2

The MC44200 contains three independent Digital to Analog Converters (DAC). The digital to analog conversion is accomplished by means of a bank of binary controlled differential current sources.

Furthermore, differential outputs are provided. The MC44200 is especially suitable as a converter in TV–picture digital processing (e.g. picture–in–picture) and Compact Disk–Interactive (CD–i) applications.

- 55 MHz Max Conversion Speed
- Differential Outputs
- Adjustable Output Current Range
- TTL Compatible Inputs
- Integrated Reference Voltage
- Single 5 V Power Supply

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_A = + 25°C unless otherwise specified)

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Rating	Value	Unit
T_{stg}	Storage Temperature	– 65 to +150	°C
T_A	Operating Ambient Temperature	– 40 to + 85	°C
I_{in}	Maximum Current Per Input Pin	± 10	mA
I_{out}	Maximum Current Per Output Pin	± 50	mA
	Maximum Current V_{ref} Pin	± 10	mA
V_{in}, V_{out}	Maximum Voltage All Pins	– 0.5 to V_{DD} + 0.5	V
P_D	Power Dissipation	700	mW
V_{DD}	DC Supply Voltage	– 0.5 to + 6	V

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (T_A = – 40 to + 85°C unless otherwise specified; V_{DD} = 5.0 V ± 5%)

Symbol	Characteristic	Min	Max	Unit	Note
V_{DD}	Power Supply Voltage	4.5	5.5	V	
$I_{DD(D)}$	Digital Supply Current		20	mA	
$I_{DD(R)}$	Reference Supply Current		15	mA	
$I_{DD(AH)}$	DAC High Current Mode Supply		30	mA	
$I_{DD(AL)}$	DAC Low Current Mode Supply		15	mA	
C_{out}	Output Capacitance		10	pF	
K	Internal Current Gain	5.1	5.5		
DAC High Current Mode (Note 1)					
V_{out}	Maximum Output Voltage	0	V_{DD} – 2.1	V	
I_{out}	Full scale Output Current	16	22	mA	
DNL	Differential Non Linearity		0.5	LSB	
INL	Integral Non Linearity		1	LSB	
ΔI_{out}	DAC to DAC Max Output Current Matching		2	%	
t_{tr}	Transition Time		8	ns	2
t_{settle}	Settling Time 50% to 98% of Step		30	ns	2
t_d	Analog Output Delay Time		50	ns	2
Δt_d	Output Delay Time Difference Between Channels		2	ns	
P_{SS}	Power Supply Sensitivity @ V_{out} (Full Scale = 1 V)		0.25	%	5
DAC Low Current Mode (Note 3)					
V_{out}	Output Voltage Range	0	V_{DD} – 1.5	V	
I_{out}	Full Scale Output Current	8	11	mA	
DNL	Differential Non Linearity		0.5	LSB	
INL	Integral Non Linearity		1	LSB	
ΔI_{out}	DAC to DAC Output Current Matching		2	%	
t_{tr}	Transition Time		15	ns	4
t_{settle}	Setting Time 50% to 98% of Step		110	ns	4
t_d	Analog Output Delay Time		70	ns	4

ELECTRICAL CHARACTERISTICS (T_A = – 40 to + 85°C unless otherwise specified; V_{DD} = 5.0 V ± 5%)

DAC Low Current Mode (continued)

Symbol	Characteristic	Min	Max	Unit	Note
Δt_d	Output Delay Time Difference Between Channels		4	ns	
PSS	Power Supply Sensitivity @ V_{out} (Full Scale = 3 V)		1.2	%	5

NOTES:
1. R_I_{ref} = 330 Ω, no external resistive load or voltage applied to pin 33.
2. Load R_L = 37.5 Ω , C_L = 15 pF.
3. R_I_{ref} = 660 Ω, no external resistive load or voltage applied to pin 33.
4. Load R_L = 300 Ω, C_L = 5 pF.
5. The change of the output voltage with change in the power supply voltage. This parameter is expressed in % change of full scale output versus % change of V_{DD}.

2

DATA INPUTS

Symbol	Characteristic	Min	Max	Unit
V_{IH}	Input High Level	2		V
V_{IL}	Input Low Level		1.2	V
t_{su}	Data Setup Time	4		ns
t_h	Data Hold Time	1		ns
C_{in}	Input Capacitance		7	pF

CLOCK INPUT

Symbol	Characteristic	Min	Max	Unit
V_{IH}	Input High Level	2		V
V_{IL}	Input Low Level		0.8	V
V_{hys}	Hysteresis	0.3		V
t_{cl}	Clock Low Duration	5		ns
t_{ch}	Clock High Duration	5		ns
t_r	Clock Rise Time		15	ns
t_f	Clock Fall Time		15	ns

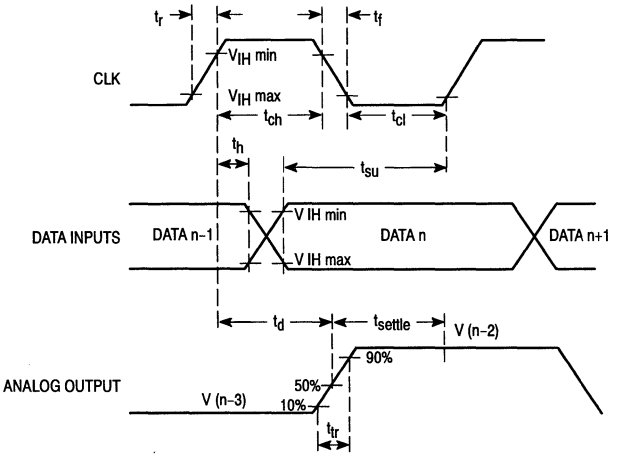


Figure 1. Clock Input and Output Timing

VOLTAGE REFERENCE

Symbol	Characteristic	Min	Max	Unit
V_{ref}	Reference Voltage	1.173	1.297	V
V_{ref} Ext	External Reference Voltage (Note 1)	1.111	1.359	V
ZV_{ref}	Output Impedance (Note 2)	10	50	kΩ

NOTES:
1. $V_{DD(R)}$ must be connected to + 5 V.
2. Load placed on external reference voltage by internal V_{ref} circuitry.

PIN ASSIGNMENTS

Pin No.	Name	Function
1	I_{ref}	To external R_I_{ref}
2	$V_{SS(R)}$	V_{SS}, reference
3	R7	Input, red, bit 7
4	R6	Input, red, bit 6
5	R5	Input, red, bit 5
6	V_{SS}	V_{SS}, digital
7	V_{DD}	V_{DD}, digital
8	R4	Input, red, bit 4
9	R3	Input, red, bit 3
10	R2	Input, red, bit 2
11	R1	Input, red, bit 1
12	R0	Input, red, bit 0
13	G7	Input, green, bit 7
14	G6	Input, green, bit 6
15	G5	Input, green, bit 5
16	G4	Input, green, bit 4
17	G3	Input, green, bit 3
18	G2	Input, green, bit 2
19	G1	Input, green, bit 1
20	G0	Input, green, bit 0
21	B7	Input, blue, bit 7
22	B6	Input, blue, bit 6

Pin No.	Name	Function
23	B5	Input, blue, bit 5
24	B4	Input, blue, bit 4
25	B3	Input, blue, bit 3
26	B2	Input, blue, bit 2
27	V_{DD}	V_{DD}, Digital
28	V_{SS}	V_{SS}, Digital
29	B1	Input, blue, bit 1
30	B0	Input, blue, bit 0
31	CLK	Clock input
32	$V_{DD(R)}$	V_{DD}, Reference
33	V_{ref}	Reference voltage, (I/O)
34	QB	Output blue (inverted)
35	VDBL	V_{DD} of blue DAC
36	QB	Output blue (true)
37	CAS	Cascade bias, to ext. C
38	QG	Output green (inverted)
39	VDGR	V_{DD} of green DAC
40	QG	Output green (true)
41	CAS	Cascade bias, to ext. C
42	QR	Output red (inverted)
43	VDRD	V_{DD} or red DAC
44	QR	Output red (true)

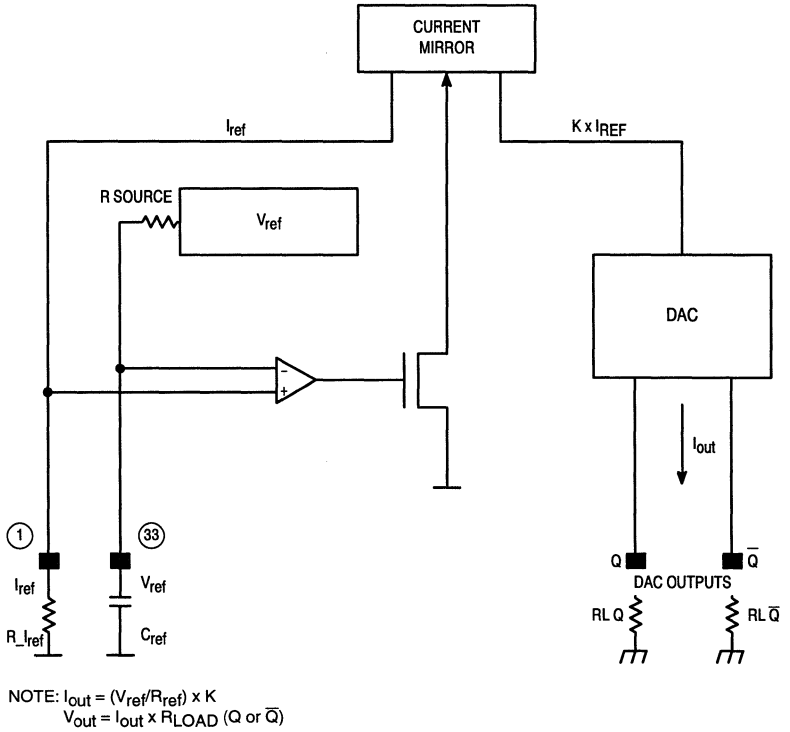
GENERAL DESCRIPTION

The MC44200 contains three parallel 8–bit digital to analog converters with common clock with a Schmitt trigger input and an internal reference supply. Each 8–bit word input to the device is stored in an internal register on the rising edge of the clock signal and is converted to an analog value by a bank of binary controlled differential current sources. The output current is determined by an integrated band–gap reference circuit, and an external resistor connected to I_{ref} (see Figure 2).

The MC44200 may be forced to operate from an external reference by connecting the external reference voltage to terminal V_{ref} (pin 33). This voltage should be within the range 1.235 V ± 10%. The internal circuitry loading on the external voltage source will be between 10 KΩ to 50 KΩ. Calculation of output drive is accomplished in the same manner as when using an internal source.

Each digital to analog converter supplies its output in the form of a differential current source. The two outputs allow the device to drive either a differential balanced line, one single unbalanced line or two complementary unbalanced lines. The outputs can drive up to 20 mA each providing 0.75 V drive into a doubly terminated 75 Ω line or 1.5 V into a single terminated line.

The output current is presetable using the external resistor (R_{ref}) at the maximum conversion rate for output current between the range of: 8 mA < I_{out} < 22 mA. *See Current Modes (High and Low).* The device can be operated at reduced output current however conversion rate and settling time must correspondingly be derated.



NOTE: $I_{out} = (V_{ref}/R_{ref}) \times K$
$V_{out} = I_{out} \times R_{LOAD}$ (Q or $\overline{Q}$)

Figure 2. MC44200 Current Bias Network

PIN DESCRIPTIONS

SUPPLY PINS

$V_{DD(D)}$ (Pins 7, 27)
VDRD (Pin 43), VDGR (Pin 39), VDBL (Pin 35)
$V_{DD(A)}$ for Red, Green and Blue Outputs
$V_{DD(R)}$ (Pin 32)

The three types of supply pins are digital, analog and reference. The dc voltage applied to all four pins must be maintained such that

$$V_{DD(D)} = V_{DD(A)} = V_{DD(R)}.$$

Each pin must be carefully decoupled to ground as close to the package as possible and particular care should be taken with $V_{DD(R)}$ as any noise present on this pin will appear in the output data as an equivalent input noise. This noise will be present on the RD, GR and BL output pins in a ratio of 1:1 to the input noise (worse case condition). Noise reduction can be improved by incorporating choke coil inductors in series with the power supply rails.

GROUND PINS

V_{SS} (Pins 6, 28) Digital Ground
$V_{SS(R)}$ (Pin 2) Reference Supply Ground

Since the analog output is a differential drive current source, no analog ground pin is needed. By returning the unused output to ground, an analog reference is established for the active output.

ANALOG OUTPUTS

QR (Pin 44)
$\overline{QR}$ (Pin 42)
QG (Pin 40)
$\overline{QG}$ (Pin 38)
QB (Pin 36)
$\overline{QB}$ (Pin 34)

The converted analog signals are output at these pins. QR, QG and QB are the true output pins while $\overline{QR}$, $\overline{QG}$ and $\overline{QB}$ provide the complementary inverted outputs. These outputs are configured as differential current drivers with a maximum current drive for each output of 20 mA. Voltage drive is determined by the value of the resistance used to program the I_{ref} pin and the value of the load on the output pins. For example, the voltage delivered to a 150 Ω load for an output programmed for 10 mA would be:

$$V_{out} = i * RL = 10\ mA * 150 = 1.5\ V.$$

When driving an unbalanced line, the unused outputs should be returned to analog ground through a resistance equal to the load on the active output pins.

OTHER ANALOG PINS

CAS (Pins 37, 41)

These pins are used for external decoupling of the internal reference circuitry for the D/As. Typically a 10 nF capacitor is connected between pin 37 and analog V_{DD}, a 470 nF capacitor is connected between pin 41 and analog V_{DD}, and pins 37 and 41 are connected together (see Figure 8).

I_{ref} (Pin 1)

This pin is used to program the value of the load current delivered by the Red, Green and Blue output pins. The value of the resistance connected between this pin and reference ground is found by the formula:

$$R_{ref} = (1.235\ V/I_{out}) \times 5.3$$

for typical values for the internal circuitry.

DIGITAL INPUTS

R0 – R7 (Pins 12 – 8, 5, 4, 3)
G0 – G7 (Pins 20 – 13)
B0 – B7 (Pins 30, 29, 26 – 21)

These pins are the parallel inputs of the digital value for the RGB signals. R0 through R7 is the digital value of the RED component, G0 through G7 is the digital value of the GREEN and B0 through B7 is digital value of the BLUE component.

CLK (Pin 31)

The rising edge of the signal supplied to this pin is used to latch the input signals into the internal registers. These registers hold the digital RGB component data for conversion by the triple D/A converters.

DIFFERENTIAL OUTPUTS

Each digital to analog converter supplies a differential output current pair whose relationship is shown in Figure 3. These outputs function in push–pull, or complementary, fashion to provide drive to a differential balanced line. The outputs may also be used to drive an unbalanced line with either in phase operation or complementary (180 degree) inversion.

When only one output is used to supply a single unbalanced current, the load on the digital to analog converter output should be balanced by placing a load on the unused output equal in value to the load on the unused output. This can be a single resistor whose value is equal to the load impedance.

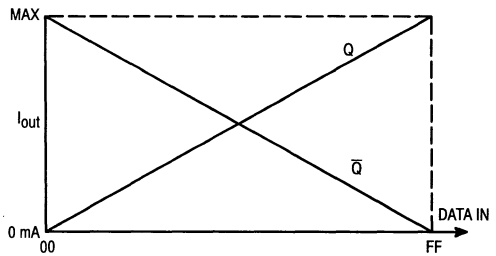


Figure 3. Q versus $\overline{Q}$

CURRENT MODES (HIGH AND LOW)

The full scale output current is determined by the external resistor R_{ref}. The high current mode (R_I_{ref} = 330 Ω) is intended to be used when the analog outputs are connected directly with a monitor going through a coaxial cable. The low current mode (R_I_{ref} = 660 Ω) may be used when the outputs are going to buffers. The full scale output current varies linearly with the external resistor R_I_{ref}.

V_{out}

The output voltage supplied to the load is determined by the value of the load impedance and the value chosen for

the external bias resistor R_{ref}. The high current mode (R_{ref} = 330 Ω) is usually intended to drive a monitor directly through a coaxial cable. When external buffering is supplied, the low current (R_{ref} = 660 Ω) mode may be used. The full scale current varies linearly with the value of R_{ref} over the range of 330 Ω to 660 Ω without derating. The reference current generated in R_{ref} by the reference voltage V_{ref} is multiplied by the current gain of the conversion circuitry. This current gain is the factor K and has a typical value of 5.3. I_{out} can be calculated using the formula:

$$I_{out} = (V_{ref}/R_{ref}) \times K.$$

For a typical value for V_{ref} of 1.235 V, a typical value for K of 5.3 and a peak current value of 13 mA, the value for R_{ref} should be 510 Ω.

$$R_{ref} = (1.235\ V/13\ mA) \times 5.3 = 504\ \Omega, \text{ use } 510\ \Omega.$$

The output voltage, V_{out}, is a product of the output drive and the load impedance (Norton's Theorem).

$$V_{out} = I_{out} \times R_{LOAD}\ (Q \text{ or } \overline{Q}).$$

Figures 4 and 5 show two different load implementations for the same line impedance.

In Figure 4, the 75 Ω transmission line is terminated both at the load and at the source. The effective load on the output of the MC44200 for this doubly terminated 75 Ω line is one half the line impedance or 37.5 Ω. The peak output voltage for this arrangement is limited to 0.75 V.

$$V_{out} = I_{out} \times R_{LOAD} = 20\ mA \times 37.5 = 0.75\ V.$$

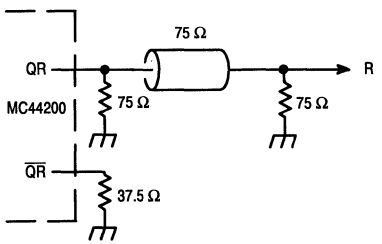
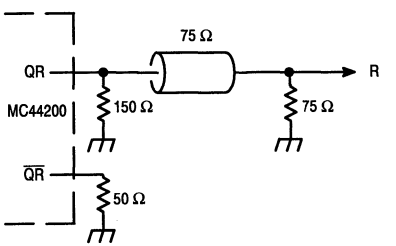


Figure 4. Resistive Load for V_{out} = 750 mV



NOTE: For best switching performance, the resistive load should be the same at the two differential outputs.

Figure 5. Resistive Load for V_{out} = 1 Vpp

Figure 5 shows the recommended method for supplying a full scale voltage of 1 V to the same 75 Ω load. The effective load on the MC44200 for the 1 V drive can be calculated as:

$$R_{LOAD} = 1\ V/20\ mA = 50\ \Omega.$$

The value for the parallel resistor necessary to achieve the 50 Ω load is:

$$1/Rp = 1/50 - 1/75 = 1/150.\ Rp = 150\ \Omega.$$

V_{DD} AND GND

To maximize the performance of the MC44200, noise should be kept to a minimum. Good printed circuit board design will enhance the operation of the MC44200. Separate analog and digital grounds will reduce noise and conversion errors. Sufficient decoupling and short leads will also improve performance (discussed later in this section).

When designing mixed analog/digital printed circuit boards, separate ground planes for digital ground and analog ground should be employed. Large switching currents generated by digital circuits will be amplified by analog circuitry and can quickly make a circuit unusable. Care should be taken to ensure analog ground does not inadvertently become part of the digital ground. The analog and digital grounds should be connected together at only one point. This is usually at or near where power enters the printed circuit board. Additionally, when interconnecting several printed circuit boards together, care must be taken to ensure that cabling does not interconnect digital switching currents through analog ground.

When using any device with the performance and speed of the MC44200, ground planes are essential. Loosely interconnected traces and/or random areas of ground strewn around the printed circuit board are inadequate for high performance circuitry. While distribution of V_{DDA} and V_{DDD} can be done by bussing, to do so with the ground system is disastrous.

A one inch long conductor is an 18 nH inductor. The cross sectional area of the conductor affects the exact value of the inductance, but for most PCB traces this is approximately correct. If the ground system is composed of traces or clumps of ground loosely interconnected, it will be inductive. The amount of inductance will be proportional to the length of the conductors making up the ground. This inductance cannot be decoupled away. It must be designed out.

A CMOS device exhibits a characteristic input capacitance of about 10 pF. If this gate is driven by a digital signal that switches 2.5 V in a period of 5 ns, the equation for the average current flowing during the switching time will be:

$$I_{AV} = Cdv/dt.$$

A voltage change of 2.5 V in 5 ns requires an average current of 5 mA. If we assume a linear ramp starting from zero, the total change in current will be 10 mA. The change in current per nanosecond per gate can be found by dividing the change in current by the time:

$$10\ mA/5\ ns = 2\ mA/ns.$$

For a device with 16 outputs driving one gate for each output:

$$di/dt = 16 \times 2\ mA/ns = 32\ mA/ns.$$

If the above 1–inch conductor is in this current path, then the voltage dropped across it can be found from the formula:

$$V = Ldi/dt = 18\ nH \times 32\ mA/ns = 0.576\ V.$$

If the inductor is in the ground system, it is in the signal path. The voltage generated by the switching currents through this inductor will be added to the signal. At best it will be superimposed on the analog signal as unwanted noise. At worst, it can render the entire circuit unusable. Even the digital signal path is not immune to this type of signal. It can false trigger clock circuits causing timing errors, confuse comparator type circuits, and cause digital signals to be misinterpreted as wrong values.

When laying out the PCB, use electrolytic capacitors of sufficient size at the power input to the printed circuit board. 47 μF tantalum capacitors are recommended. Adding low ESR (effective series resistance) decoupling capacitors of about 0.1 μF capacitance across V_{CC} and/or V_{DD} at each device will help reduce noise in general and ESD (electrostatic discharge) susceptibility. Connect the high–capacity and high–frequency capacitors as close as possible to all analog V_{CC}, digital V_{DD}, and ground pins. Implementation of a good ground plane ground system can all but eliminate the type of noise described above.

To summarize:

- Use sufficient electrolytic capacitor filtering
- Make separate ground planes for analog and digital ground
- Tie these grounds together at one and only one point
- Keep the ground planes as continuous and unbroken as possible
- Use low ESR capacitors of about 0.1 μF capacitance on 3 V_{CC} and V_{DD} at each device
- Keep all leads as short as possible

EMI

When using ICs in or near television receiver circuits, EMI (electromagnetic interference) and subsequent unwanted display artifacts and distortion are probable unless adequate EMI suppression is implemented. A common misconception is that some offending digital device is the culprit. This is erroneous in that an IC itself has insufficient surface area to produce sufficient radiation. The device, while it is the generator of interfering signals, must be coupled to an antenna before EMI is radiated. The source for the EMI is not the IC which generates the offending signals but rather the circuitry which is attached to the IC.

Potential EMI signals are generated by ***all*** digital devices. Whether they become a nuisance is dependent upon their frequency and whether they have a sufficient antenna. The frequency and number of these signals is affected by both circuit design within the IC and the manufacturing process. Device speed is also a major contributor of potential EMI. Because the design is determined by the anticipated application, the manufacturing process is fixed and the drive for speed ever increasing, the only effective point to implement EMI suppression is in the PC board design. The PC board usually is the antenna which radiates the EMI. The most efficient method of minimizing EMI radiation is to minimize the efficiency of this antenna.

The most common cause of inadequate EMI suppression lies with the ground system of the suspected digital devices. As pointed out previously, di/dt transitions can be significant in digital circuits. If the di/dt transitions appear in the ground system and the ground system is inductive, the harmonics present in these transitions are a source of potential EMI signals. The unfortunate result of putting digital devices on a reactive ground system is guaranteed EMI problems.

The area which should be addressed first as a potential EMI source is the ground. Without an adequate ground system, EMI cannot be effectively reduced by decoupling. If at all possible, the ground should be a complete unbroken plane. Figure 6 shows two examples of relieving ground around device pins. When relieving vias and plated through holes, large areas of ground loss should be avoided. When the relief pattern is equal to half the distance between pins, over etching and process errors may remove ground between pins. If sufficient ground around enough pins are removed, the ground system can become isolated or nearly isolated "patches" which will appear inductive. If ground, such as the vicinity of an IC, must be removed, replace with a cross hatch of ground lines with the mesh as small as possible.

If a single unbroken plane can be devoted to the ground system, EMI can usually be sufficiently suppressed by using ferrite beads on suspect EMI paths and decoupling with adequate values of capacitors. The value of the decoupling capacitor depends on the frequency and amplitude of the offending signals. Ferrite beads are available in a wide variety of shape, size and material to fit virtually any application.

Choose a ferrite bead for desired impedance at the desired frequency and construct a low pass filter using one or more appropriate capacitors in a "L", "T" or "PI" arrangement. Use only capacitors of low inductive and resistive properties such as ceramic or mica. Install filters in series with each IC pin suspected of contributing offending EMI signals and as close to the pin as possible. Analysis using a spectrum analyzer can help determine which pins are suspect.

Where PC board costs constrain the number of layers available, and if the EMI frequencies are far removed from the frequencies of operation, ferrite beads and decoupling capacitors may still be effective in reducing EMI emissions. Where only two (or in some cases, only one!) layer is used, the ground system is always reactive and poses an EMI problem. If the offending EMI and normal operating frequency differ sufficiently, filtering can still work.

While not generally recommended, in cases where a ground plane is not possible, the following technique may be used with some success.

An "island" is constructed in the ground system for the digital device using ferrite beads and decoupling capacitors as shown by the example in Figure 7. The ground must be cut so that the digital ground for the device is isolated from the rest of the ground system. Next choose a ferrite bead of the appropriate value. Install this bead between the isolated ground and the ground system. Install low pass filters in all suspect lines with the capacitor closest to the device pin connected to the isolated ground in all signal lines where EMI is suspect. Also cut the power to the device and insert a ferrite bead as shown in Figure 7. Finally, decouple the device between the power pin(s) and isolated ground pin(s) using a low inductive/resistive capacitor of adequate value.

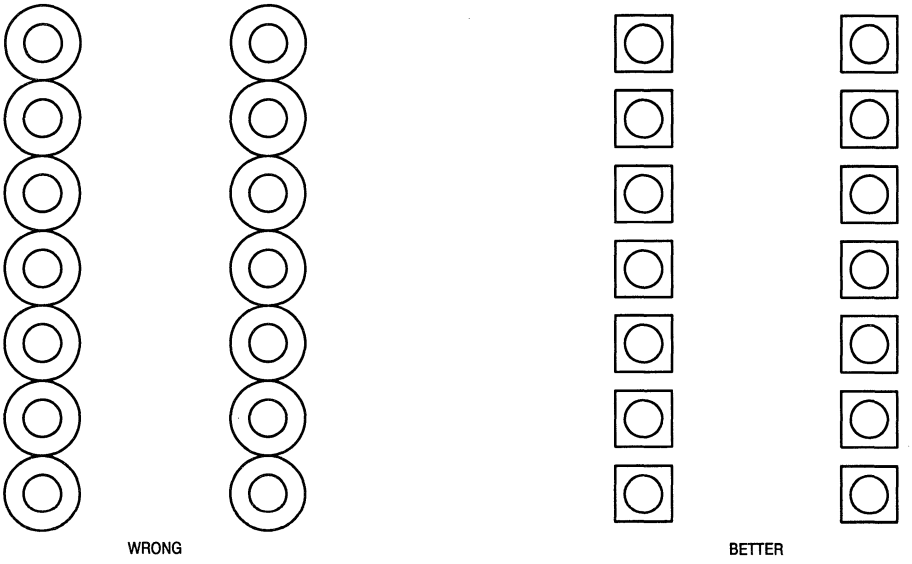


Figure 6.

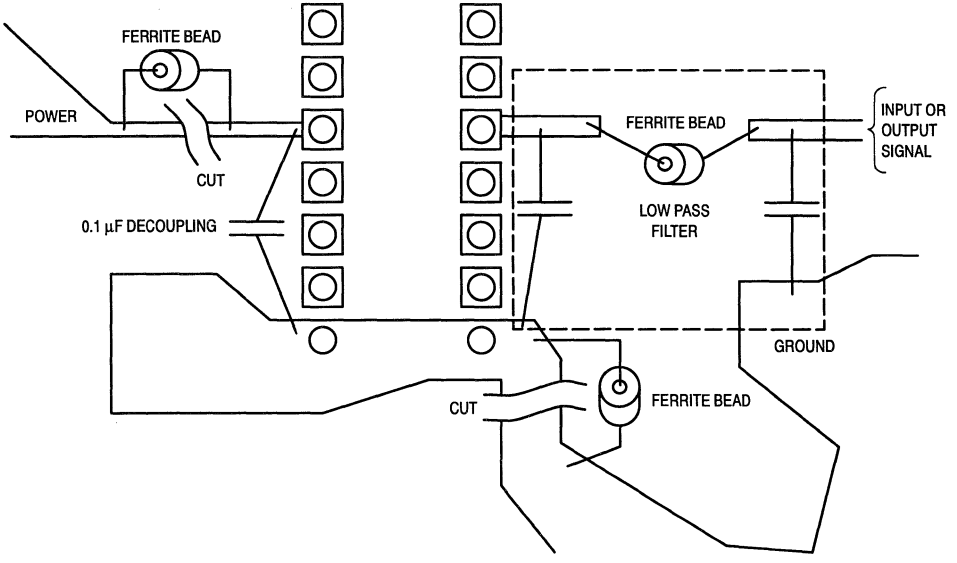


Figure 7.

The methods described above will work acceptably when the EMI frequency and the frequency of operation of the device generating the EMI differ greatly. Where the EMI is disturbing the high VHF or UHF channels and the device generating the EMI is operating within the NTSC/PAL bandwidth, the energy contained in the harmonics generating the EMI is situated well above the operating frequency and suppressing this type of EMI poses no great problem. However, if the EMI is present on low VHF channels and/or the operation of the device is outside the NTSC/PAL bandwidth, such as a 2x pixel clock or 4xfsc oscillator, compromise between video quality and suppression complexity is usually required to obtain an acceptable solution. For those cases where the operating frequency of the device is very near the frequency of the EMI disturbance, careful attention to PCB layout, multiple layer PCB and even shielding may be necessary to obtain an acceptable design.

LATCH–UP

The $V_{DD(A)}$, $V_{DD(D)}$, and $V_{DD(R)}$ pins connect to power supplies that are independent from each other. Therefore, latch–up may occur when the power is applied. To eliminate latch–up, apply power to the $V_{DD(A)}$, $V_{DD(D)}$, and $V_{DD(R)}$ pins simultaneously.

APPLICATION CIRCUIT

Figure 8 shows a typical application of the MC44200. The device has been biased for the low current (10 mA typical) mode. This drive allows the DAC to deliver 1.5 V into a doubly terminated, 75 Ω transmission line. The three bipolar transistors shown on the schematic provide the necessary current gain for the DAC outputs.

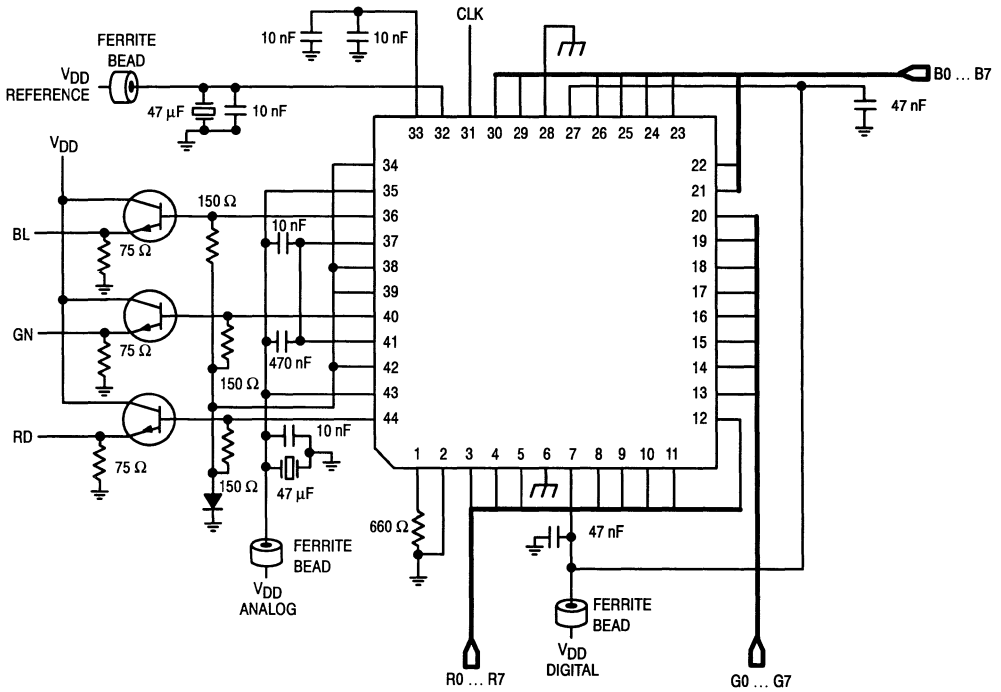
The 660 Ω resistor connected to I_{ref} (pin 1) sets the output drive:

$$I_{out} = (V_{ref}/R_{ref}) \times K = (1.235\ V/660\ \Omega) \times 5.33 = 10\ mA.$$

The voltage delivered to the load is:

$$V_{out} = I_{out} \times R_{LOAD} = 10\ mA \times 150\ \Omega = 1.5\ V.$$

If the diode shown in the schematic is chosen so that the forward voltage drop at 10 mA is equal to V_{BE} for the bipolar transistors, the base–emitter voltage drop of the transistors can be ignored.



NOTE: THE DEVICE IS IN LOW CURRENT MODE

ANALOG GROUND

DIGITAL GROUND

Figure 8. Triple Digital Analog Converter (Typical fixture for buffering)

MC44250

Advance Information

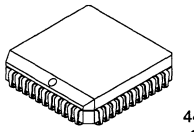
Triple 8-Bit Video ADC
CMOS

2

The MC44250 contains three independent parallel analog–to–digital flash converters (ADC). Each ADC consists of 256 latching comparators and an encoder. Video may be ac or dc coupled. With ac coupling, input clamping provides for internal dc restoration. The MC44250 also contains a dithering generator for video processing performance enhancements.

The MC44250 is especially suitable as a front–end converter in TV–picture digital processing (picture–in–picture, frame storage, etc.). The high speed conversion rate of the ADC is suitable for video bandwidth of well over 6 MHz.

- 15 MHz Maximum Sampling Rate
- Output Latching Minimizes Skew
- Input Clamps Suitable for RGB and YUV Applications
- Built–In Dither Generator with Subsequent Digital Correction
- Featured on the MC144000EVK PC Video Capture Evaluation Kit
- Single 5–Volt Power Supply
- Operating Temperature Range: – 40 to + 85°C

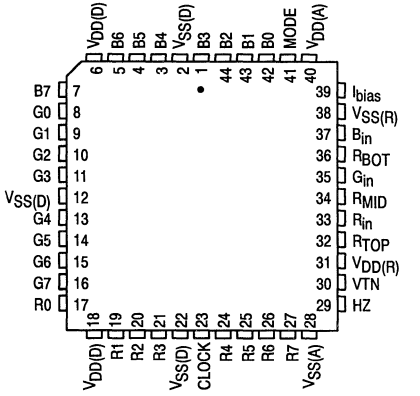


FN SUFFIX
44-LEAD PLCC
CASE 777–02

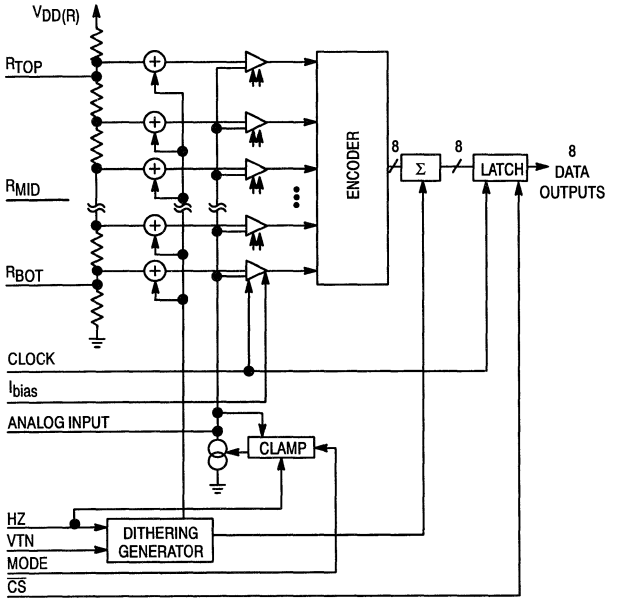
ORDERING INFORMATION

MC44250FN	PLCC

PIN ASSIGNMENT



SIMPLIFIED BLOCK DIAGRAM OF ONE OF THE ADCs



This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Characteristic	Value	Unit
$V_{DD(A)}$, $V_{DD(D)}$, $V_{DD(R)}$	DC Supply Voltage (referenced to V_{SS})	– 0.5 to + 6.0	V
V_{in}	Input Voltage, All Pins	– 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current Per Pin	± 20	mA
I_{out}	DC Output Current Per Pin	± 25	mA
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the following Operating Ranges.

2

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}) ($V_{DD(R)} = V_{DD(A)} = V_{DD(D)}$; R_{bias} (pin 39) = 5 kΩ to ground)

OPERATING RANGES

Symbol	Characteristic	Min	Max	Unit
$V_{DD(A)}$, $V_{DD(D)}$, $V_{DD(R)}$	Power Supply Voltage	4.5	5.5	V
$I_{DD(A)}$	Analog Supply Current	—	55	mA
$I_{DD(R)}$	Reference Supply Current	—	28	mA
$I_{DD(D)}$	Digital Supply Current	—	5	mA
T_A	Operating Ambient Temperature Range	– 40	+ 85	°C

A/D CONVERTER

Symbol	Characteristic	Min	Max	Unit
C_{in}	Input Capacitance	—	60	pF
V_{min}	See Figure 12	0.3 x V_{DD}	0.36 x V_{DD}	V
V_{max}	See Figure 12	0.876 x V_{DD}	0.942 x V_{DD}	V
V_{range}	See Figure 12	0.576 x V_{DD}	0.6 x V_{DD}	V
Gain	See Figure 12 (Note 1)	0.96	1.0	LSB
DNL	Differential Nonlinearity (Note 1)	—	± 1.0	LSB
INL	Integral Nonlinearity (Note 1)	—	± 2.0	LSB
E_{gain}	Gain Difference (Note 2)	—	± 1.0	%
E_{off}	Offset Difference (Notes 1, 2)	—	± 4.0	LSB

CLOCK INPUT

Symbol	Characteristic	Min	Max	Unit
V_{IH}	Clock Input High Level	2	—	V
V_{IL}	Clock Input Low Level	—	0.8	V
I_{IL}	Low Level Input Current	—	± 2.0	µA
I_{IH}	High Level Input Current	—	± 2.0	µA
F_{CLK}	Clock Frequency	—	15	MHz
t_{wL}	Clock Low Duration, Figure 1	27.5	—	ns
t_{wH}	Clock High Duration, Figure 1	27.5	—	ns
t_r	Clock Rise Time (10% to 90%), Figure 1	—	15	ns
t_f	Clock Fall Time (10% to 90%), Figure 1	—	15	ns

HZ AND VTN INPUTS

Symbol	Characteristic	Min	Max	Unit
V_{IH}	HZ and VTN High Level Voltage	2.0	—	V
V_{IL}	HZ and VTN Low Level Voltage	—	0.8	V
I_{IL}	Low Level Input Current	—	±2.0	µA
I_{IH}	High Level Input Current	—	±2.0	µA
t_H	HZ High Time, Figure 3	3	—	ns

CLAMPING NETWORK (Measured on R, G, B Inputs)

Symbol	Characteristic	Min	Max	Unit
I_{sink}	Clamping Sink Current	2.0	5.0	µA
I_{source}	Clamping Source Current	−5.0	−2.0	µA
D_{ICL}	Clamping Current Difference (Note 2)	—	0.1	µA
ΔV_{clamp}	Clamping Levels (Max. Deviation Compared to Table 1)	—	±1.0	LSB

NOTES:
1. Unit "LSB" means ideal LSB (see definitions section).
2. "Difference" means difference between any two converters in the same package.

RESISTIVE REFERENCE NETWORK

Symbol	Characteristic	Min	Max	Unit
Z_{TOP}	R_{TOP} Output Impedance	24	56	Ω
Z_{BOT}	R_{BOT} Output Impedance	60	140	Ω
Z_{MID}	R_{MID} Output Impedance	60	140	Ω

MODE INPUT

Symbol	Characteristic	Min	Max	Unit
V_{IL}	Logical "0" Level	0	0.8	V
V_{IH}	Logical "1" Level	4.2	$V_{DD(D)}$	V
V_{IZ}	Logical "Open" Level	1.8	3.2	V
I_{IL}	Input Current at "0" Level	—	±50	µA
I_{IH}	Input Current at "1" Level	—	±50	µA
I_{IZ}	Input Current at "Open" Level	—	±50	µA

DATA OUTPUTS

Symbol	Characteristic	Min	Max	Unit
t_d	Delay from Sample Clock to Valid Output, Figure 2	2.5	2.5	Cycle
I_{OL}	Output Sinking Current at V_{out} = 0.4 V	2.0	—	mA
I_{OH}	Output Sourcing Current at $V_{out} = V_{DD} - 0.1$ V	−0.4	—	mA
t_{QLH}, t_{QHL}	Propagation Delay from the Clock Rising Edge to Valid Data Output (C_L = 15 pF), Figure 1	—	40	ns

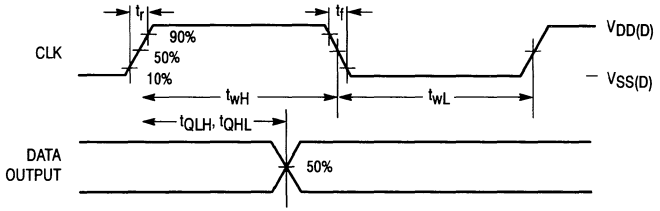


Figure 1. Clock and Output Timing

2

PIN ASSIGNMENTS

Pin No.	Name	Function
1	B3	Output Blue, Bit 3
2	$V_{SS(D)}$	V_{SS}, Digital
3	B4	Output Blue, Bit 4
4	B5	Output Blue, Bit 5
5	B6	Output Blue, Bit 6
6	$V_{DD(D)}$	V_{DD}, Digital
7	B7	Output Blue, Bit 7 (MSB)
8	G0	Output Green, Bit 0 (LSB)
9	G1	Output Green, Bit 1
10	G2	Output Green, Bit 2
11	G3	Output Green, Bit 3
12	$V_{SS(D)}$	V_{SS}, Digital
13	G4	Output Green, Bit 4
14	G5	Output Green, Bit 5
15	G6	Output Green, Bit 6
16	G7	Output Green, Bit 7 (MSB)
17	R0	Output Red, Bit 0 (LSB)
18	$V_{DD(D)}$	V_{DD}, Digital
19	R1	Output Red, Bit 1
20	R2	Output Red, Bit 2
21	R3	Output Red, Bit 3
22	$V_{SS(D)}$	V_{SS}, Digital

Pin No.	Name	Function
23	CLK	Clock Input
24	R4	Output Red, Bit 4
25	R5	Output Red, Bit 5
26	R6	Output Red, Bit 6
27	R7	Output Red, Bit 7 (MSB)
28	$V_{SS(A)}$	V_{SS}, Analog
29	HZ	Horizontal Sync
30	VTN	Vertical Sync
31	$V_{DD(R)}$	Reference Voltage
32	R_{TOP}	Reference Tapping, Top
33	R_{in}	Analog Input, Red
34	R_{MID}	Reference Tapping, Middle
35	G_{in}	Analog Input, Green
36	R_{BOT}	Reference Tapping, Bottom
37	B_{in}	Analog Input, Blue
38	$V_{SS(R)}$	V_{SS} for Reference Voltage
39	I_{BIAS}	To External Bias Resistor
40	$V_{DD(A)}$	V_{DD}, Analog
41	MODE	Clamp Level Select Input
42	B0	Output Blue, Bit 0 (LSB)
43	B1	Output Blue, Bit 1
44	B2	Output Blue, Bit 2

PIN DESCRIPTIONS

RESISTIVE REFERENCE NETWORK

R_{TOP} (Pin 32)
R_{BOT} (Pin 34)
R_{MID} (Pin 36)

Taps on the reference ladder are pinned out, providing access to the bottom (R_{BOT}), the top (R_{TOP}), and the middle scale points. These pins are intended for ac bypassing as ladder noise may present a problem. The value of the decoupling capacitor should not exceed 47 nF. Large capacitance values can cause problems because of the amount of energy stored. When a system containing the MC44250 is rapidly powered down and up, the capacitor voltage may exceed the supply voltage during the power up and cause a latch-up condition. Failure to adequately decouple these pins can adversely affect the conversion process.

SUPPLY PINS

$V_{DD(A)}$ (Pin 40)
$V_{DD(D)}$ (Pins 6, 18)
$V_{DD(R)}$ (Pin 31)

The three types of supply pins are analog, digital, and reference. The dc voltage applied to all four pins must be maintained such that

$$V_{DD(A)} = V_{DD(D)} = V_{DD(R)}.$$

Each pin must be carefully decoupled to ground as close to the package as possible, and particular care should be taken with $V_{DD(R)}$ as any noise present on this pin will appear in the output data as an equivalent input noise. This noise will be present on the R_{in}, G_{in} and B_{in} input pins in a ratio of 1:1 to the input noise (worst case condition). Noise reduction can be improved by incorporating choke coil inductors in series with the power supply rails.

ANALOG INPUTS

R_{in} (Pin 33)
G_{in} (Pin 35)
B_{in} (Pin 37)

The analog signals to be converted are input at these pins. An on–chip clamp circuit for dc restoration is available when using ac coupling. The clamp circuit operation is activated by the presence of the signal at the HZ input. This signal is derived from the composite sync information and must be coincident with the horizontal sync of the composite video waveform for proper operation. Y_{in}, U_{in}, and V_{in} may be used instead of the RGB signals. In this case the conversion will be a YUV analog–to–digital conversion.

I_{bias} (Pin 39)

The comparator bias current is set by connecting an external resistor between I_{bias} and ground. The conversion rate is guaranteed for a resistor value of 5.1 kΩ ± 5% and will decrease logarithmically with increased resistance. The resistor must be placed adjacent to the I_{bias} pin. No decoupling capacitor is allowed on this pin.

DIGITAL OUTPUTS

R0 – R7 (Pins 17, 19–21, 24–27)
G0 – G7 (Pins 8–11, 13–16)
B0 – B7 (Pins 42–44, 1,3–5, 7)

These pins are the parallel output for the digital value for the RGB signals. R0 through R7 are the digital equivalent of the analog RED input, G0 through G7 are equivalent to the GREEN input, and B0 through B7 are equivalent to the BLUE input. If YUV analog signals have been input instead of the RGB signals the digital outputs will be Y0 through Y7, U0 through U7 and V0 through V7.

DIGITAL INPUTS

Clock (Pin 23)

The analog input voltages to be converted are sensed at the falling edge of the clock signal and the corresponding data is present on the digital outputs at the clock signal rising edge, 2.5 cycles later (see Figure 2).

HZ (Pin 29)

This is the horizontal synchronization input, and is used to increment the dither generator. The clamp network is also controlled by HZ to ensure proper dc restoration for R_{in}, G_{in}, and B_{in} before conversion.

VTN (Pin 30)

The vertical synchronization input, VTN, resets the dither generator after every second vertical sync pulse (after each frame).

MODE (Pin 41)

This pin is used to select the proper clamp levels (see Table 1).

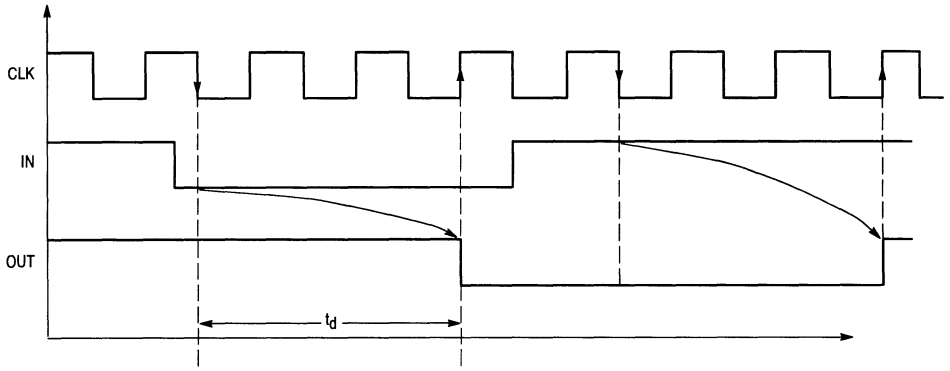


Figure 2. Conversion Timing Functional Characteristics

CIRCUIT OPERATION

GENERAL

The MC44250 contains three independent parallel analog–to–digital converters (ADC). Each ADC consists of 256 latching comparators and an encoder. The MC44250 may be used to convert RGB or YUV video information from an analog to a digital format, or as a triple ADC for non–video information. For video processing performance enhancement, each ADC has a dither generator with subsequent digital correction designed into it. The dithering generator reduces display degradation from granulation of the luminance information caused by quantization errors of the digitizing process. Each ADC is driven from a common clock and receives common sync information from the HZ and VTN pins. In addition, the VTN pin controls the dithering function and disables the dithering generator when VTN is pulled low. The sampling of the analog input signals occurs at the falling edge of the clock signal, whereas the digital outputs change state at the rising clock edge. The bias current of the comparators is set by an external resistor. Input clamps allow for ac coupling of the input signals.

CLAMP NETWORK

The MC44250 can be operated either dc coupled or ac coupled. When dc coupled, the MC44250 will track the average dc level of the input waveform. For ac coupling, an on–chip dc restoration circuit samples and adjusts the average dc level of the input signal. The MC44250 has three selectable clamping levels for ac coupling. The clamp levels are selected by the MODE pin according to Table 1. In the RGB mode, the clamping levels are set to 16/256, corresponding to 6.3% of full range. In the YUV mode, the UV clamping levels are set to 128/256 (50%), and the Y input to either 16/256 or 64/256 (25%).

When input HZ (horizontal) is high, as illustrated in Figure 3, the voltage difference between the analog input voltage and the clamp reference voltage is integrated within each clamp network. At the falling edge of HZ, a latching comparator senses the sign of the integrator output voltage. Depending on this result, either a sinking or a sourcing current is applied to the analog input pin as long as input HZ remains low.

For video applications, the timing of HZ is critical to the proper operation of the ADC. The frequency of HZ should be locked to the line frequency of the video input. The pulse width and timing of HZ with respect to the video signal is shown in Figure 5. The top curve represents the horizontal synchronizing and blanking interval for a video signal. The pulse width of HZ, (t_H) should be less than the width of the back porch, (t_{BP}) and coincident with it. In all cases, HZ must return low before the end of the back porch, t_{BP}.

Table 1. Clamping Levels

MODE (Pin 41)	Application	Clamp Levels	G_{in}	R_{in}	B_{in}
L	RGB		16/256	16/256	16/256
H	Y–UV Mode Without Sync	Format	16/256	128/256	128/256
Open	Y–UV Mode With Sync		64/256	128/256	128/256

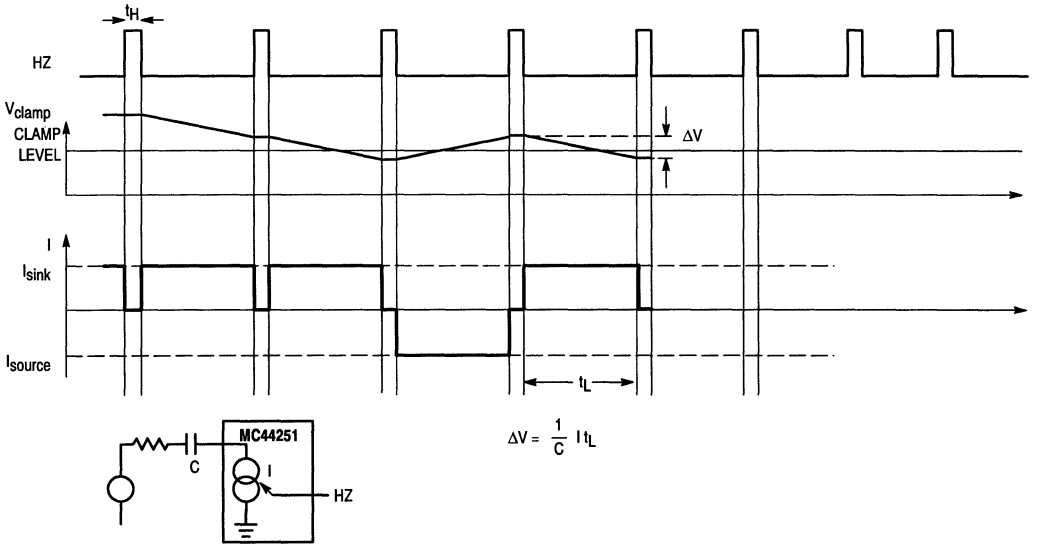


Figure 3. Clamp Network Timing Diagram — Operation

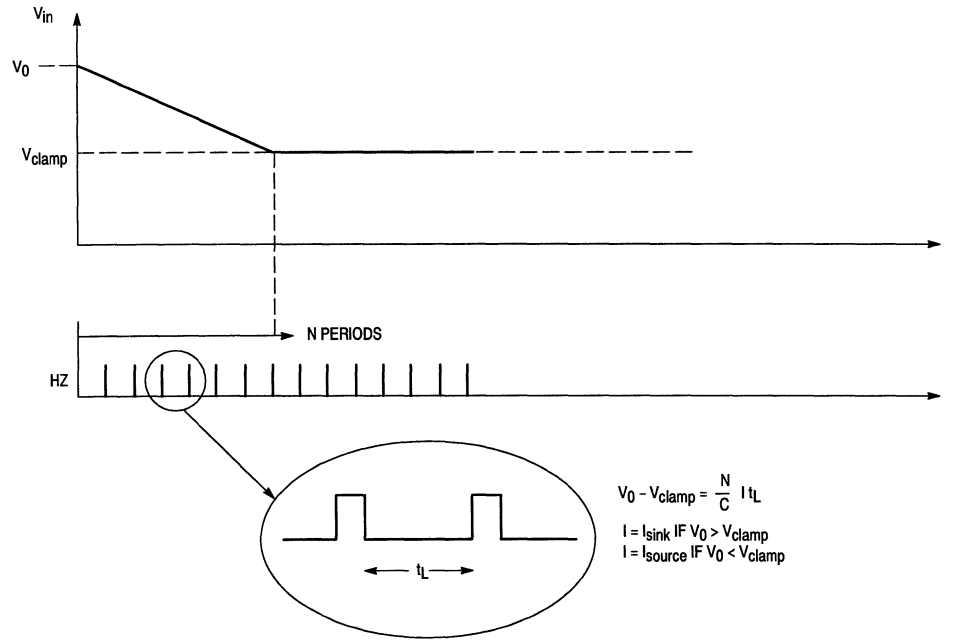


Figure 4. Clamp Network Timing Diagram — Power Up

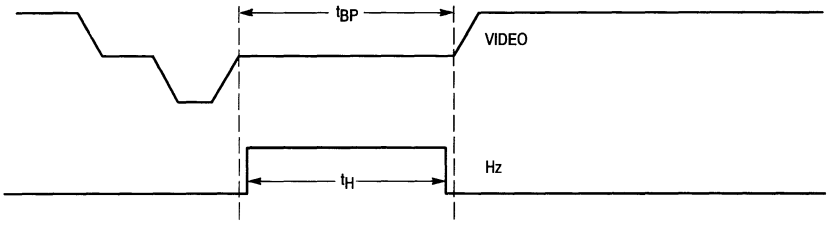


Figure 5. Horizontal Timing

DITHERING

Dithering can be used to reduce the errors that are the result of the digitizing process used to convert video information between analog and digital forms. This method can also be applied to non–video signals. When converting analog signals to a digital format, errors can be introduced because of the limited number of discrete levels that the digital system imposes. For example, an 8–bit digital word can describe exactly 256 discrete analog levels. In some cases, this may not be sufficient for the application involved.

One solution is to increase the number of bits that describe the analog signal. The disadvantages of this approach are the increase in cost of the converter and the loss in speed associated with the increased number of bits. The addition of analog filters at the point where the digital information is converted back to analog is also possible, but this also has its limitations.

When a ramp voltage is generated from a digital source or an analog ramp is converted to a digital form and back to analog, the limited number of vertical samples causes the ramp to take the form of a "stair case" (see Figure 6). The severity of this distortion depends on the number of digital bits that generated the ramp. The "stair case" effect is less pronounced when the number of bits producing the ramp is increased.

When processing video information using a YUV form and a luminance ramp is displayed, granulation errors may become noticeable. This condition can also occur when one of the RGB signals is ramped and the other two are held constant. When processing video information using 24–bits or less, this "granulation" can be observed. Since the video is processed as three 8–bit signals, the maximum number of different luminance levels is reduced to 256. In cases where only a 7–bit luminance signal is used, the maximum number of luminance levels is reduced to 128. The uniform luminance ramp is observed on the display as vertical bars rather than a uniform luminance change.

The dithering technique consists of adding a small offset to the input signal. This offset (when it is equal to an integer number of LSB) is then subtracted from the digital output data. This offset is varied "line–to–line" by one half LSB steps. It allows each point of the waveform to be interpolated to higher precision by averaging the differential linearity errors on the screen.

The addition of the small offset forces the comparators to sample at a slightly different point on the input waveform (see Figure 7). When translated to the display, the effect is to shift this value slightly to the left. Overall accuracy of the display is maintained by subtracting this value from the output when the shift is equal to an integer number of LSB. For a uniform and continuous video waveform, the result of incrementing and decrementing the dither voltage is to effectively double the luminance levels from 256 to 512. The effect is to broaden the luminance range. This results in a more pleasing display with less visible quantization.

The dithering pattern is generated by means of a binary counter, which is incremented for every line by input HZ, and reset by every second vertical input VTN; thus, the dithering pattern is synchronized to the deflection of the screen. The effect of the dithering pattern is given in Figure 8. Subsequent subtraction of the introduced dithering signal at the output of each ADC is performed by a binary adder. The dithering function is suppressed when input VTN is low.

Depending on the position of the counter, the minimum output code may be $00 or $01 and the maximum output code may be $FE or $FF.

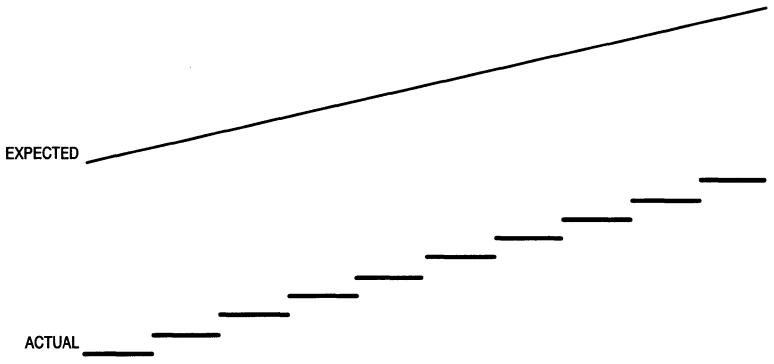


Figure 6. Distortion Produced By Digitizing

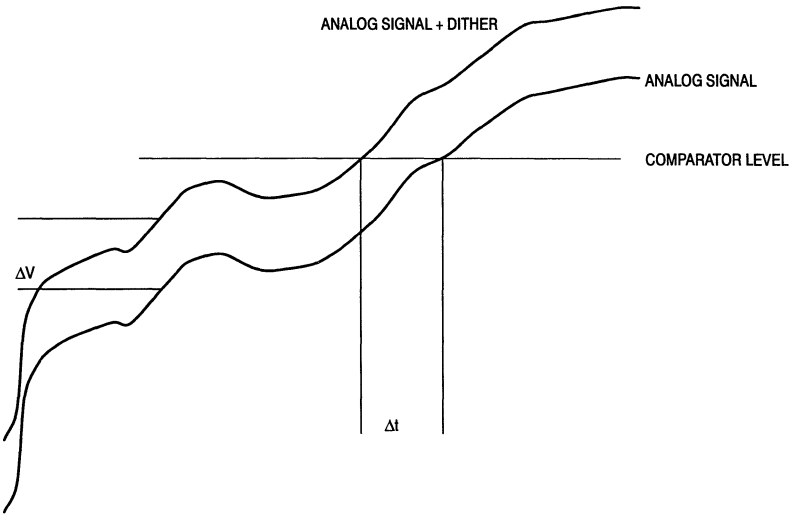


Figure 7. Amplitude Dithering

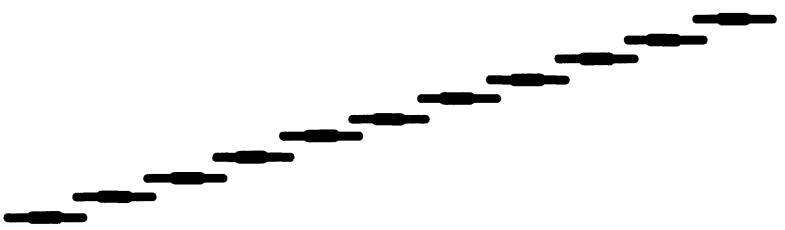


Figure 8. Effect of Dithering Pattern

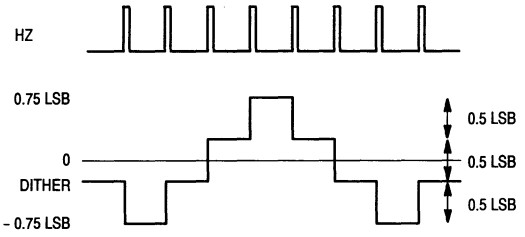


Figure 9. Dithering Sequence

RESTRICTIONS ON $V_{DD(R)}$

The normal operating condition for the MC44250 is defined as $V_{DD(R)} = V_{DD(A)} = V_{DD(D)}$ and the safe operating range of $V_{DD(R)}$ is defined as $0 \le V_{DD(R)} \le V_{DD}$. In cases where $V_{DD(R)}$ is operated at values other than V_{DD}, it should be noted that the accuracy of the conversion process is reduced. In all cases $V_{DD(R)}$ should not be allowed to exceed V_{DD}.

The step size is defined as SS(n) and the ideal step size is defined as SSI. We may define an error component, ∂, as the difference between the actual step size and the ideal step size so that

$$\partial = |SSI - SS(n)|.$$

We may also define a worst case value for ∂ as

$$\partial \le \partial w$$

where ∂w is the greatest value of ∂. The origin of this error is the offset mismatch from one comparator to another and is nearly independent of $V_{DD(R)}$ and V_{DD}.

Since ∂ is nearly independent of $V_{DD(R)}$, its value will remain constant for all values of $V_{DD(R)}$.

The step size error, SSE, is defined as

$$SSE(n) = (SSI - SS(n))/SSI = \partial(n)/SSI.$$

Furthermore, the ideal step size SSI is defined as

$$SSI = V_{DD(R)} \times 0.6/255.$$

Since ∂ is a constant and SSI is proportional to $V_{DD(R)}$, the step size error, SSE, will increase as $V_{DD(R)}$ is decreased. Further study will show that the differential nonlinearity, DNL, will also increase as $V_{DD(R)}$ is reduced. To minimize these errors it is desirable to keep $V_{DD(R)}$ as high as possible. Since the maximum value for $V_{DD(R)}$ is V_{DD},

$$V_{DD(R)} = V_{DD(D)} = V_{DD(A)}$$

is the value that produces the greatest conversion accuracy.

INPUT VOLTAGE RANGE

In applications where the input signals are dc coupled to the MC44250, the following restrictions apply:

If $V_{in} \le V_{min}$, then the output code = $00 or $01 (depending on the dither generator).

If $V_{in} \ge V_{max}$, then the output code = $FE or $FF (depending on the dither generator).

If $V_{min} \le V_{in} \le V_{max}$, then the output code reflects the correct value of the input voltage.

If the input is video based and ac coupled, then the input voltage range for V_{in} without saturation is

$$0 \le V_{in} \le V_{range}.$$

For V_{in} this reflects a maximum video input level before saturation of about 3 V for V_{DD} = 5 V.

DEFINITIONS

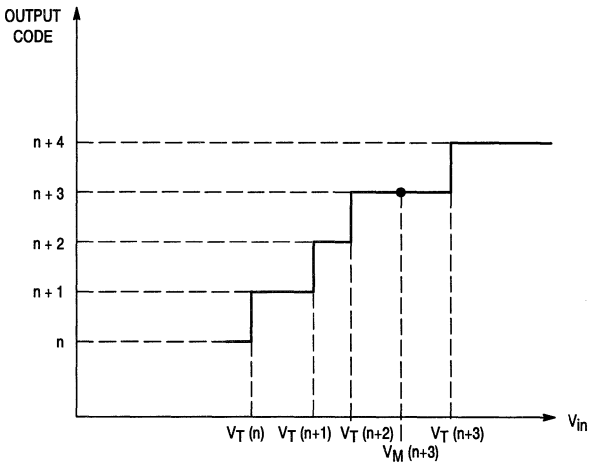


Figure 10.

- **Transition Voltage:** voltage at which transition from step n to step n+1 occurs = $V_T(n)$.

- **Step Size:** Difference between two consecutive transition voltages.

$$SS(n) = V_T(n) - V_T(n-1)$$

- **Mid–Point Voltage:**

$$V_M(n) = \frac{V_T(n) + V_T(n-1)}{2}$$

$$V_M(\text{max code}) = \frac{V_{DD(R)} + V_T(\text{max code} - 1)}{2}$$

- **Step Size Ideal:**

$$\frac{V_{range}}{255} = SSI$$

- **Differential Nonlinearity (DNL):**

$$DNL(n) = \frac{V_M(n+1) - V_M(n)}{SSI} - 1 \text{ in LSB}$$

- **Integral Nonlinearity (I_{NL}) and Offset:**

$$I_{NL}(n) = \frac{V_M(n) - a \bullet n - b}{SSI} \text{ in LSB}$$

Note: I_{NL} (min code) and I_{NL} (max code) is not defined.

- **Gain:** Gain = a in the formula Y = a • code + b or the slope in the curve mid–points = f(code)

- **V_{offset}:** $V_{offset} = b - V_{min}$

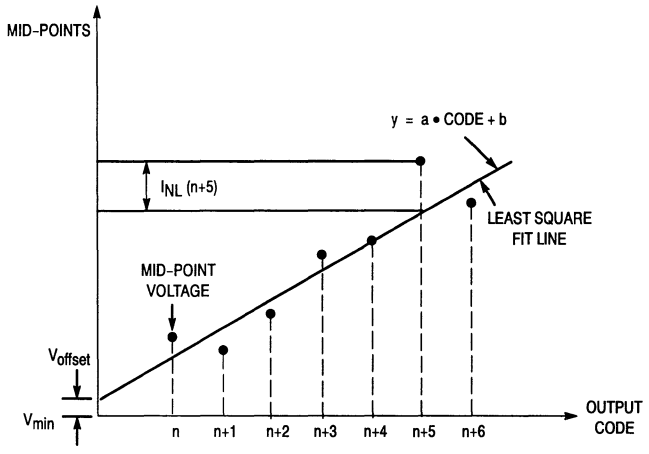
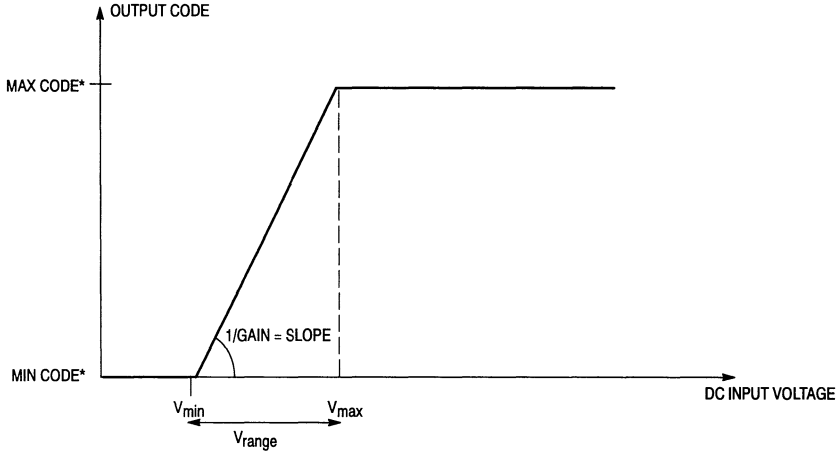


Figure 11. Integral Nonlinearity and Offset



*See dither generator.
LSB ideal = $V_{range}/255$
(Min code = 0 or 1; see dither generator)

Figure 12.

APPLICATION INFORMATION

PCB DESIGN

To maximize the performance of the MC44250, noise should be kept to a minimum. Good printed circuit board design will enhance the operation of the MC44250. Separate analog and digital grounds will reduce noise and conversion errors. In addition, separate filters on analog V_{CC} and digital V_{DD} will also help to minimize noise and conversion errors. Sufficient decoupling and short leads will also improve performance.

When designing mixed analog/digital printed circuit boards, separate ground planes for digital ground and analog ground should be employed. Large switching currents generated by digital circuits will be amplified by analog circuitry and can quickly make a circuit unusable. Care should be taken to ensure analog ground does not inadvertently become part of the digital ground. The analog and digital grounds should be connected together at only one point. This is usually at or near where power enters the printed circuit board. Additionally, when interconnecting several printed circuit boards together, care must be taken to ensure that cabling does not interconnect digital and analog grounds together to produce a path for digital switching currents through analog ground.

When using any device with the performance and speed of the MC44250, ground planes are essential. Loosely interconnected traces and/or random areas of ground strewn around the printed circuit board are inadequate for high performance circuitry. While distribution of V_{DD} and V_{CC} can be done by bussing, to do so with the ground system is disastrous.

An inch long conductor is an 18 nH inductor. The cross sectional area of the conductor affects the exact value of the inductance, but for most PCB traces this is approximately correct. If the ground system is composed of traces or clumps of ground loosely interconnected, it will be inductive. The amount of inductance will be proportional to the length of the conductors making up the ground. This inductance cannot be decoupled away. It must be designed out.

A CMOS device exhibits a characteristic input capacitance of about 10 pF. If this gate is driven by a digital signal that switches 2.5 V in a period of 5 ns, the equation for the average current flowing during the switching time will be:

$$I_{AV} = Cdv/dt.$$

A voltage change of 2.5 V in 5 ns requires an average current of 5 mA. If we assume a linear ramp starting from zero, the total change in current will be 10 mA. The change in current per nanosecond per gate can be found by dividing the change in current by the time

$$10\ mA/5\ ns = 2\ mA/ns.$$

For a device with 16 outputs driving one gate for each output,

$$di/dt = 16 \times 2\ mA/ns = 32\ mA/ns.$$

If the above 1–inch wire is in this current path, then the voltage dropped across it can be found from the formula

$$V = Ldi/dt = 18\ nH \times 32\ mA/ns = 0.576\ V.$$

If the inductor is in the ground system, it is in the signal path. The voltage generated by the switching currents through this inductor will be added to the signal. At best it will be superimposed on the analog signal as unwanted noise. At worst, it can render the entire circuit unusable. Even the digital signal path is not immune to this type of signal. It can false trigger clock circuits causing timing errors, confuse comparator type circuits, and cause digital signals to be misinterpreted as wrong values.

When laying out the PCB, use electrolytic capacitors of sufficient size at the power input to the printed circuit board. Adding low ESR decoupling capacitors of about 0.1 μF capacitance across V_{CC} and/or V_{DD} at each device will help reduce noise in general and ESD susceptibility. Implementation of a good ground plane ground system can all but eliminate the type of noise described above.

To summarize, use sufficient electrolytic capacitor filtering, make separate ground planes for analog ground and digital ground, tie these grounds together at one and only one point, keep the ground planes as continuous and unbroken as possible, use low ESR capacitors of about 0.1 μF capacitance on V_{CC} and V_{DD} at each device, and keep all leads as short as possible.

EMI SUPRESSION

When using ICs in or near television receiver circuits, EMI (electromagnetic interference) and subsequent unwanted display artifacts and distortion are probable unless adequate EMI suppression is implemented. A common misconception is that some offending digital device is the culprit. This is erroneous in that an IC itself has insufficient surface area to produce sufficient radiation. The device, while it is the generator of interfering signals, must be coupled to an antenna before EMI is radiated. The source for the EMI is not the IC which generates the offending signals but rather the circuitry which is attached to the IC.

Potential EMI signals are generated by ***all*** digital devices. Whether they become a nuisance is dependent upon their frequency and whether they have a sufficient antenna. The frequency and number of these signals is affected by both circuit design within the IC and the manufacturing process. Device speed is also a major contributor of potential EMI. Because the design is determined by the anticipated application, the manufacturing process is fixed and the drive for speed ever increasing, the only effective point to implement EMI suppression is in the PC board design. The PC board usually is the antenna which radiates the EMI. The most efficient method of minimizing EMI radiation is to minimize the efficiency of this antenna.

The most common cause of inadequate EMI suppression lies with the ground system of the suspected digital devices. As pointed out previously, di/dt transitions can be significant in digital circuits. If the di/dt transitions appear in the ground system and the ground system is inductive, the harmonics present in these transitions are a source of potential EMI signals. The unfortunate result of putting digital devices on a reactive ground system is guaranteed EMI problems.

The area which should be addressed first as a potential EMI source is the ground. Without an adequate ground system, EMI cannot be effectively reduced by decoupling. If at all possible, the ground should be a complete unbroken plane. Figure 13 shows two examples of relieving ground around device pins. When relieving vias and plated through holes, large areas of ground loss should be avoided. When

the relief pattern is equal to half the distance between pins, over–etching and process errors may remove ground between pins. If sufficient ground around enough pins is removed, the ground system can become isolated or nearly isolated "patches" which will appear inductive. If ground, such as the vicinity of an IC, must be removed, replace with a cross hatch of ground lines with the mesh as small as possible.

If a single unbroken plane can be devoted to the ground system, EMI can usually be sufficiently suppressed by using ferrite beads on suspect EMI paths and decoupling with adequate values of capacitors. The value of the decoupling capacitor depends on the frequency and amplitude of the offending signals. Ferrite beads are available in a wide variety of shape, size and material to fit virtually any application.

Choose a ferrite bead for desired impedance at the desired frequency and construct a low pass filter using one or more appropriate capacitors in a "L", "T" or "PI" arrangement. Use only capacitors of low inductive and resistive properties such as ceramic or mica. Install filters in series with each IC pin suspected of contributing offending EMI signals and as close to the pin as possible. Analysis using a spectrum analyzer can help determine which pins are suspect.

Where PC board costs constrain the number of layers available, and if the EMI frequencies are far removed from the frequencies of operation, ferrite beads and decoupling capacitors may still be effective in reducing EMI emissions. Where only two (or in some cases, only one!) layer is used, the ground system is always reactive and poses an EMI problem. If the offending EMI and normal operating frequency differ sufficiently, filtering can still work.

An "island" is constructed in the ground system for the digital device using ferrite beads and decoupling capacitors as shown by the example in Figure 14. The ground must be cut so that the digital ground for the device is isolated from the rest of the ground system. Next choose a ferrite bead of the appropriate value. Install this bead between the isolated ground and the ground system. Install low pass filters in all suspect lines with the capacitor closest to the device pin connected to the isolated ground in all signal lines where EMI is suspect. Also cut the power to the device and insert a ferrite bead as shown in Figure 14. Finally, decouple the device between the power pin(s) and isolated ground pin(s) using a low inductive/resistive capacitor of adequate value.

The methods described above will work acceptably when the EMI frequency and the frequency of operation of the device generating the EMI differ greatly. Where the EMI is disturbing the high VHF or UHF channels and the device generating the EMI is operating within the NTSC/PAL bandwidth, the energy contained in the harmonics generating the EMI is situated well above the operating frequency and suppressing this type of EMI poses no great problem. However, if the EMI is present on low VHF channels and/or the operation of the device is outside the NTSC/PAL bandwidth, such as a 2X pixel clock or 4xfsc oscillator, compromise between video quality and suppression complexity is usually required to obtain an acceptable solution. For those cases where the operating frequency of the device is very near the frequency of the EMI disturbance, careful attention to PCB layout, multiple layer PCB and even shielding may be necessary to obtain an acceptable design.

APPLICATIONS CIRCUIT

Figure 15 shows a typical applications circuit. This circuit will produce analog–to–digital conversion of either RGB information or YUV information by setting SW1. In the YUV mode, SW1 is set either to position '1' or to the open position depending on the desired clamp level (see Table 1). The RGB inputs then become YUV inputs and correspondingly, the RGB outputs are YUV. For RGB operation, SW1 is set to the '0' position.

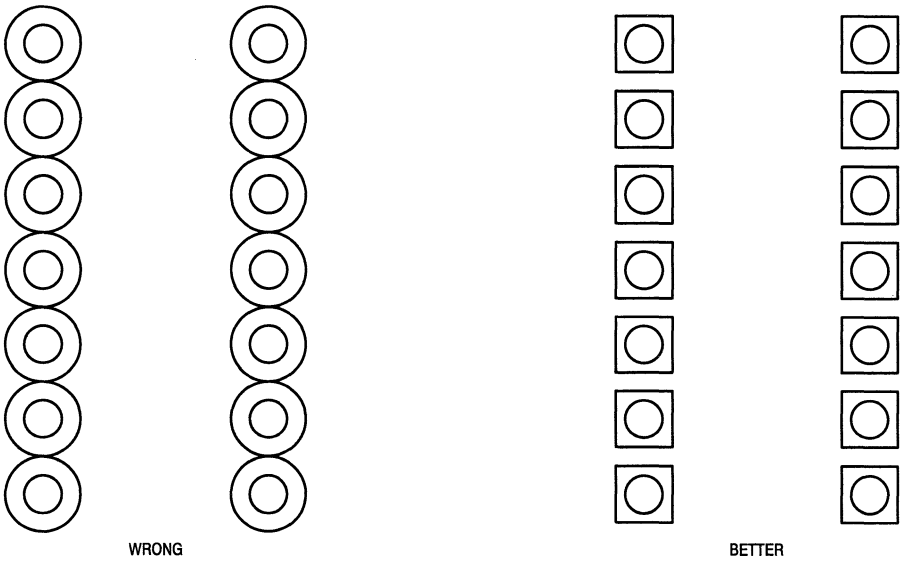


Figure 13.

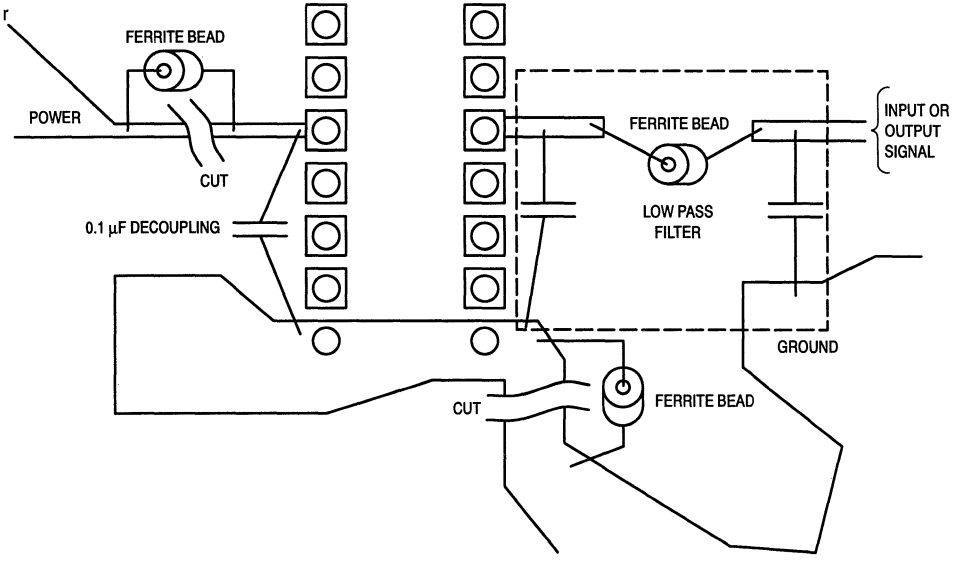


Figure 14.

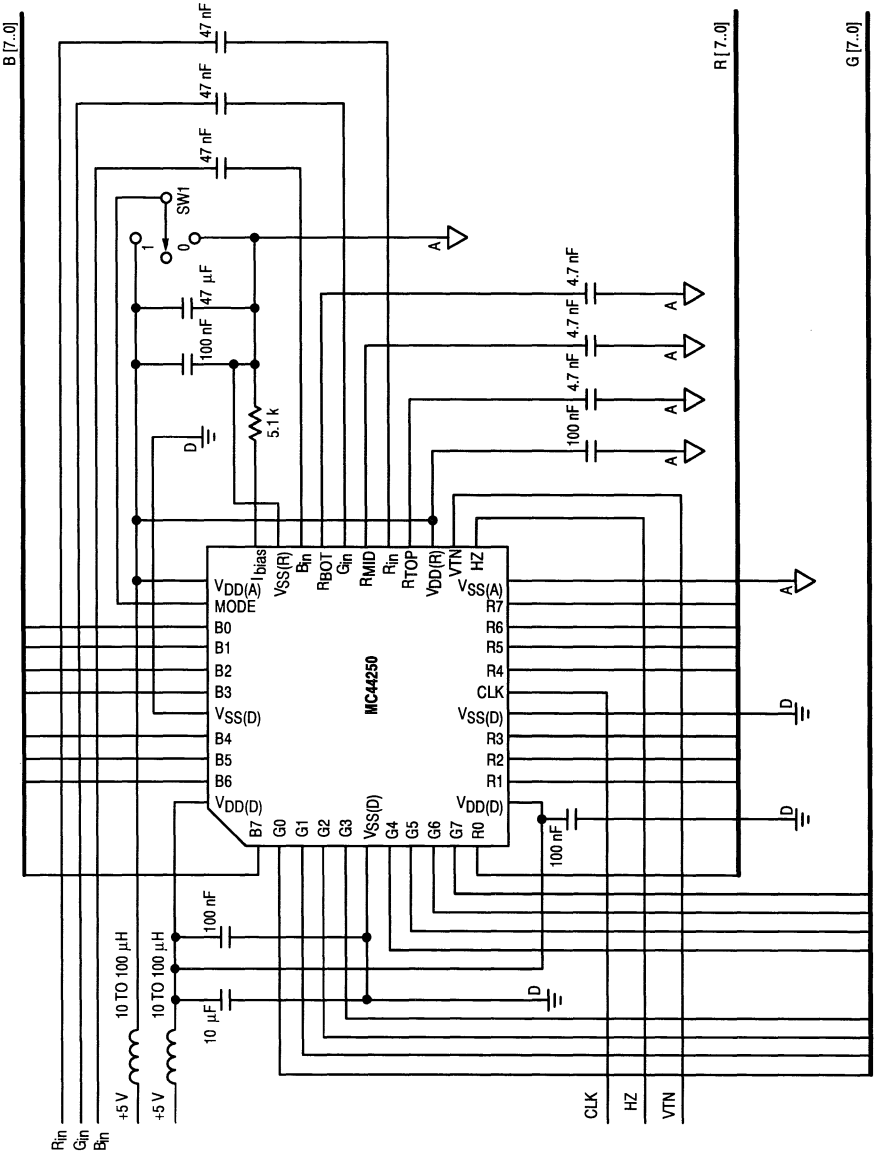


Figure 15. Application Circuit

MC44251

Advance Information

Triple 8-Bit Video ADC Three-State Outputs

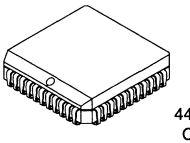
CMOS

2

The MC44251 contains three independent parallel analog–to–digital flash converters (ADC). Each ADC consists of 256 latching comparators and an encoder. Video may be ac or dc coupled. With ac coupling, input clamping provides for internal dc restoration. The MC44251 also contains a dithering generator for video processing performance enhancements.

The MC44251 is especially suitable as a front–end converter in TV–picture digital processing (picture–in–picture, frame storage, etc.). The high speed conversion rate of the ADC is suitable for video bandwidth of well over 6 MHz.

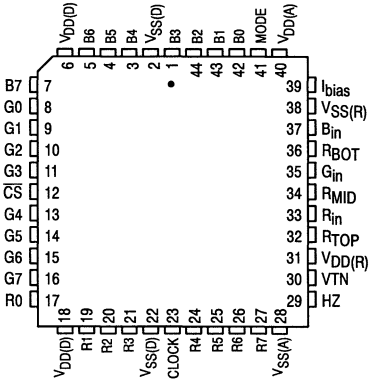
- 18 MHz Maximum Sampling Rate
- Three–State Output Buffers
- Output Latching Minimizes Skew
- Input Clamps Suitable for RGB and YUV Applications
- Built–In Dither Generator with Subsequent Digital Correction
- Single 5–Volt Power Supply
- Operating Temperature Range: – 40 to + 85°C
- Vtn and Hz Input Threshold Hysteresis Built–In
- Pin Compatible with MC44250



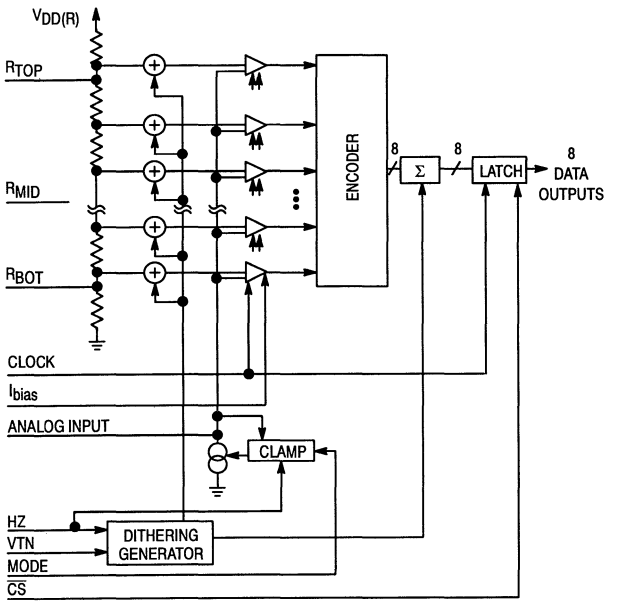
FN SUFFIX
44–LEAD PLCC
CASE 777–02

ORDERING INFORMATION
MC44251FN PLCC

PIN ASSIGNMENT



SIMPLIFIED BLOCK DIAGRAM OF ONE OF THE ADCs



This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristic	Value	Unit
$V_{DD(A)}$, $V_{DD(D)}$, $V_{DD(R)}$	DC Supply Voltage (referenced to V_{SS})	– 0.5 to + 6.0	V
V_{in}	Input Voltage, All Pins	– 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current per Pin	± 20	mA
I_{out}	DC Output Current per Pin	± 25	mA
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

2

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}) ($V_{DD(R)} = V_{DD(A)} = V_{DD(D)}$; R_{bias} (Pin 39) = 5 kΩ to ground)

OPERATING RANGES

Symbol	Characteristic	Min	Max	Unit
$V_{DD(A)}$, $V_{DD(D)}$, $V_{DD(R)}$	Power Supply Voltage	4.5	5.5	V
$I_{DD(A)}$	Analog Supply Current	—	55	mA
$I_{DD(R)}$	Reference Supply Current	—	28	mA
$I_{DD(D)}$	Digital Supply Current	—	5	mA
T_A	Operating Ambient Temperature Range	– 40	+ 85	°C

A/D CONVERTER

Symbol	Characteristic	Min	Max	Unit
C_{in}	Input Capacitance	—	60	pF
V_{min}	See Figure 11	0.3 x V_{DD}	0.36 x V_{DD}	V
V_{max}	See Figure 11	0.89 x V_{DD}	0.93 x V_{DD}	V
V_{range}	See Figure 11	0.57 x V_{DD}	0.59 x V_{DD}	V
Gain	See Figure 11 (Note 1)	0.95	1.0	LSB
DNL	Differential Nonlinearity (Note 1)	—	± 1.0	LSB
INL	Integral Nonlinearity (Note 1)	—	± 2.0	LSB
E_{gain}	Gain Difference (Note 2)	—	± 1.0	%
E_{off}	Offset Difference (Notes 1, 2)	—	± 3.0	LSB

CLOCK INPUT

Symbol	Characteristic	Min	Max	Unit
V_{IH}	Clock Input High Level	4.2	—	V
V_{IL}	Clock Input Low Level	—	0.8	V
I_{IL}	Low Level Input Current	—	± 2.0	µA
I_{IH}	High Level Input Current	—	± 2.0	µA
F_{CLK}	Clock Frequency	—	18	MHz
t_{wL}	Clock Low Duration, Figure 1	27.5	—	ns
t_{wH}	Clock High Duration, Figure 1	27.5	—	ns
t_r	Clock Rise Time (10% to 90%), Figure 1	—	15	ns
t_f	Clock Fall Time (10% to 90%), Figure 1	—	15	ns

HZ AND VTN INPUTS

Symbol	Characteristic	Min	Max	Unit
V_{IH}	HZ and VTN Input Turn–On Threshold Voltage	0.56 x V_{DD}	—	V
V_{IL}	HZ and VTN Input Turn–Off Threshold Voltage	—	0.29 x V_{DD}	V
V_{HYS}	Hysteresis Voltage	0.11 x V_{DD}	0.17 x V_{DD}	V
I_{IL}	Low Level Input Current	—	± 2.0	µA
I_{IH}	High Level Input Current	—	± 2.0	µA
t_H	HZ High Time, Figure 3	3	—	ns

CHIP SELECT INPUT

Symbol	Characteristic	Min	Max	Unit
V_{IH}	Input High Level	3.5	—	V
V_{IL}	Clamping Source Current	—	1.5	V
I_{IN}	Input Leakage Current	—	± 2.0	µA

CLAMPING NETWORK (Measured on R,G,B Inputs)

Symbol	Characteristic	Min	Max	Unit
I_{sink}	Clamping Sink Current	2.0	5.0	µA
I_{source}	Clamping Source Current	– 5.0	– 2.0	µA
D_{ICL}	Clamping Current Difference (Note 2)	—	0.5	µA
ΔV_{damp}	Clamping Levels (Max. Deviation Compared to Table 1)	—	± 1.5	LSB

RESISTIVE REFERENCE NETWORK

Symbol	Characteristic	Min	Max	Unit
Z_{TOP}	R_{TOP} Output Impedance	28	48	Ω
Z_{BOT}	R_{BOT} Output Impedance	70	130	Ω
Z_{MID}	R_{MID} Output Impedance	70	130	Ω

MODE INPUT

Symbol	Characteristic	Min	Max	Unit
V_{IL}	Logical "0" Level	0	0.8	V
V_{IH}	Logical "1" Level	4.2	$V_{DD(D)}$	V
V_{IZ}	Logical "Open" Level	2	2.8	V
I_{IL}	Input Current at "0" Level	—	± 50	µA
I_{IH}	Input Current at "1" Level	—	± 80	µA
I_{IZ}	Input Current at "Open" Level	—	± 50	µA

DATA OUTPUTS

Symbol	Characteristic	Min	Max	Unit
t_d	Delay from Sample Clock to Valid Output, Figure 2	2.5	2.5	Cycle
I_{OL}	Output Sinking Current at V_{out} = 0.4 V	2.0	—	mA
I_{OH}	Output Sourcing Current at V_{out} = V_{DD} – 0.1 V	– 0.4	—	mA
t_{QLH}, t_{QHL}	Propagation Delay from the Clock Rising Edge to Valid Data Output (C_L = 15 pF), Figure 1	—	40	ns
I_{OTR}	Maximum Three–State Leakage Current	—	± 50	µA

NOTES:
1. Unit "LSB" means ideal LSB (see definitions section).
2. "Difference" means difference between any two converters in the same package.

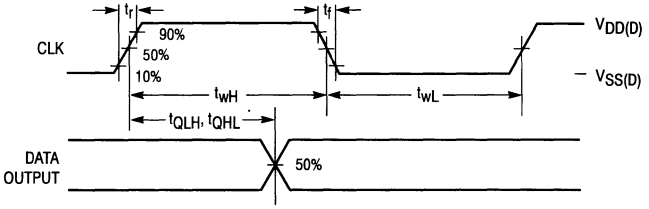


Figure 1. Clock and Output Timing

2

PIN DESCRIPTIONS

Pin No.	Name	Function
1	B3	Output Blue, Bit 3
2	$V_{SS(D)}$	V_{SS}, Digital
3	B4	Output Blue, Bit 4
4	B5	Output Blue, Bit 5
5	B6	Output Blue, Bit 6
6	$V_{DD(D)}$	V_{DD}, Digital
7	B7	Output Blue, Bit 7 (MSB)
8	G0	Output Green, Bit 0 (LSB)
9	G1	Output Green, Bit 1
10	G2	Output Green, Bit 2
11	G3	Output Green, Bit 3
12	$\overline{CS}$	Chip Select
13	G4	Output Green, Bit 4
14	G5	Output Green, Bit 5
15	G6	Output Green, Bit 6
16	G7	Output Green, Bit 7 (MSB)
17	R0	Output Red, Bit 0 (LSB)
18	$V_{DD(D)}$	V_{DD}, Digital
19	R1	Output Red, Bit 1
20	R2	Output Red, Bit 2
21	R3	Output Red, Bit 3
22	$V_{SS(D)}$	V_{SS}, Digital

Pin No.	Name	Function
23	CLK	Clock Input
24	R4	Output Red, Bit 4
25	R5	Output Red, Bit 5
26	R6	Output Red, Bit 6
27	R7	Output Red, Bit 7 (MSB)
28	$V_{SS(A)}$	V_{SS}, Analog
29	HZ	Horizontal Sync
30	VTN	Vertical Sync
31	$V_{DD(R)}$	V_{DD}, reference
32	R_{TOP}	Reference Tapping, Top
33	R_{in}	Analog Input, Red
34	R_{MID}	Reference Tapping, Middle
35	G_{in}	Analog Input, Green
36	R_{BOT}	Reference Tapping, Bottom
37	B_{in}	Analog Input, Blue
38	$V_{SS(R)}$	V_{SS} for Reference Voltage
39	I_{BIAS}	To External Bias Resistor
40	$V_{DD(A)}$	V_{DD}, Analog
41	MODE	Clamp Level Select Input
42	B0	Output Blue, Bit 0 (LSB)
43	B1	Output Blue, Bit 1
44	B2	Output Blue, Bit 2

RESISTIVE REFERENCE NETWORK

R_{TOP} (Pin 32)
R_{BOT} (Pin 34)
R_{MID} (Pin 36)

Taps on the reference ladder are pinned out, providing access to the bottom (R_{BOT}), the top (R_{TOP}), and the middle scale points. These pins are intended for ac bypassing as ladder noise may present a problem. The value of the decoupling capacitor should not exceed 47 nF. Large capacitance values can cause problems because of the amount of energy stored. When a system containing the MC44251 is rapidly powered down and up, the capacitor voltage may exceed the supply voltage during the power up and cause a latch–up condition. Failure to adequately decouple these pins can adversely affect the conversion process.

2

SUPPLY PINS

$V_{DD(A)}$ (Pin 40)
$V_{DD(D)}$ (Pins 6, 18)
$V_{DD(R)}$ (Pin 31)

The three types of supply pins are analog, digital, and reference. The dc voltage applied to all four pins must be maintained such that

$$V_{DD(A)} = V_{DD(D)} = V_{DD(R)}.$$

Each pin must be carefully decoupled to ground as close to the package as possible, and particular care should be taken with $V_{DD(R)}$ as any noise present on this pin will appear in the output data as an equivalent input noise. This noise will be present on the R_{in}, G_{in} and B_{in} input pins in a ratio of 1:1 to the input noise (worst case condition). Noise reduction can be improved by incorporating choke coil inductors in series with the power supply rails.

ANALOG INPUTS

R_{in} (Pin 33)
G_{in} (Pin 35)
B_{in} (Pin 37)

The analog signals to be converted are input at these pins. An on–chip clamp circuit for dc restoration is available when using ac coupling. The clamp circuit operation is activated by the presence of the signal at the HZ input. This signal is derived from the composite sync information and must be coincident with the horizontal sync of the composite video waveform for proper operation. Y_{in}, U_{in}, and V_{in} may be used instead of the RGB signals. In this case the conversion will be a YUV analog–to–digital conversion.

I_{bias} (Pin 39)

The comparator bias current is set by connecting an external resistor between I_{bias} and ground. The conversion rate is guaranteed for a resistor value of 5.1 kΩ ± 5% and will decrease logarithmically with increased resistance. The resistor must be placed adjacent to the I_{bias} pin. No decoupling capacitor is allowed on this pin.

DIGITAL OUTPUTS

R0–R7 (Pins 17, 19–21, 24–27)
G0–G7 (Pins 8–11, 13–16)
B0–B7 (Pins 42–44, 1, 3–5, 7)

These pins are the parallel output for the digital value for the RGB signals. R0 through R7 are the digital equivalent of the analog RED input, G0 through G7 are equivalent to the GREEN input, and B0 through B7 are equivalent to the BLUE input. If YUV analog signals have been input instead of the RGB signals the digital outputs will be Y0 through Y7, U0 through U7 and V0 through V7.

DIGITAL INPUTS

Clock (Pin 23)

The analog input voltages to be converted are sensed at the falling edge of the clock signal and the corresponding data is present on the digital outputs at the clock signal rising edge, 2.5 cycles later (see Figure 2).

HZ (Pin 29)

This is the horizontal synchronization input, and is used to increment the dither generator. The clamp network is also controlled by HZ to ensure proper dc restoration for R_{in}, G_{in}, and B_{in} before conversion.Schmitt trigger input is included to improve noise immunity.

VTN (Pin 30)

The vertical synchronization input, VTN, resets the dither generator after every second vertical sync pulse (after each frame).Schmitt trigger input is included to improve noise immunity.

MODE (Pin 41)

This pin is used to select the proper clamp levels (see Table 1).

CHIP SELECT (Pin 12)

Chip select is an active low input used to enable the ADC for data transfers. When the $\overline{CS}$ is at a high level, the digital output are forced to a high impedance state.

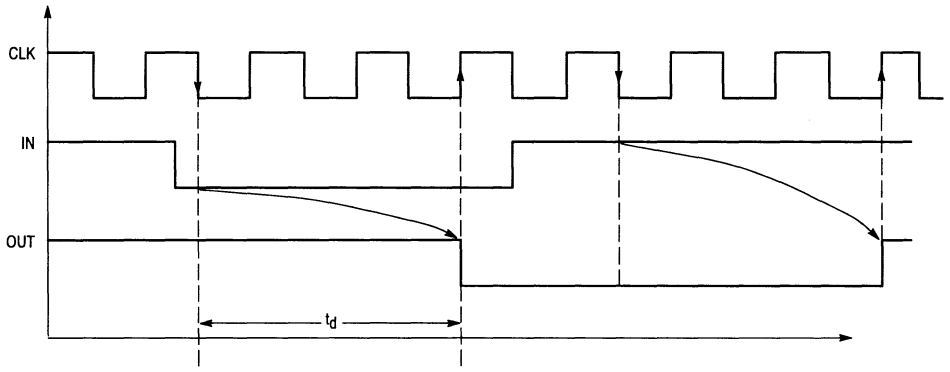


Figure 2. Conversion Timing Functional Characteristics

CIRCUIT OPERATION

GENERAL

The MC44251 contains three independent parallel analog–to–digital converters (ADC). Each ADC consists of 256 latching comparators and an encoder. The MC44251 may be used to convert RGB or YUV video information from an analog to a digital format, or as a triple ADC for non–video information. For video processing performance enhancement, each ADC has a dither generator with subsequent digital correction designed into it. The dithering generator reduces display degradation from granulation of the luminance information caused by quantization errors of the digitizing process. Each ADC is driven from a common clock and receives common sync information from the HZ and VTN pins. In addition, the VTN pin controls the dithering function and disables the dithering generator when VTN is pulled low. The sampling of the analog input signals occurs at the falling edge of the clock signal, whereas the digital outputs change state at the rising clock edge. The bias current of the comparators is set by an external resistor. Input clamps allow for ac coupling of the input signals.

CLAMP NETWORK

The MC44251 can be operated either dc coupled or ac coupled. When dc coupled, the MC44251 will track the average dc level of the input waveform. For ac coupling, an on–chip dc restoration circuit samples and adjusts the average dc level of the input signal. The MC44251 has three selectable clamping levels for ac coupling. The clamp levels are selected by the MODE pin according to Table 1. In the RGB mode, the clamping levels are set to 16/256, corresponding to 6.3% of full range. In the YUV mode, the UV clamping levels are set to 128/256 (50%), and the Y input to either 16/256 or 64/256 (25%).

When input HZ (horizontal) is high, as illustrated in Figure 3a, the voltage difference between the analog input voltage and the clamp reference voltage is integrated within each clamp network. At the falling edge of HZ, a latching comparator senses the sign of the integrator output voltage. Depending on this result, either a sinking or a sourcing current is applied to the analog input pin as long as input HZ remains low.

For video applications, the timing of HZ is critical to the proper operation of the ADC. The frequency of HZ should be locked to the line frequency of the video input. The pulse width and timing of HZ with respect to the video signal is shown in Figure 4. The top curve represents the horizontal synchronizing and blanking interval for a video signal. The pulse width of HZ, (t_H) should be less than the width of the back porch, (t_{BP}) and coincident with it. In all cases, HZ must return low before the end of the back porch, t_{BP}.

Table 1. Clamping Levels

MODE (Pin 41)	Application	Clamp Levels	G_{in}	R_{in}	B_{in}
L	RGB		16/256	16/256	16/256
H	Y–UV Mode Without Sync	Format	16/256	128/256	128/256
Open	Y–UV Mode With Sync		64/256	128/256	128/256

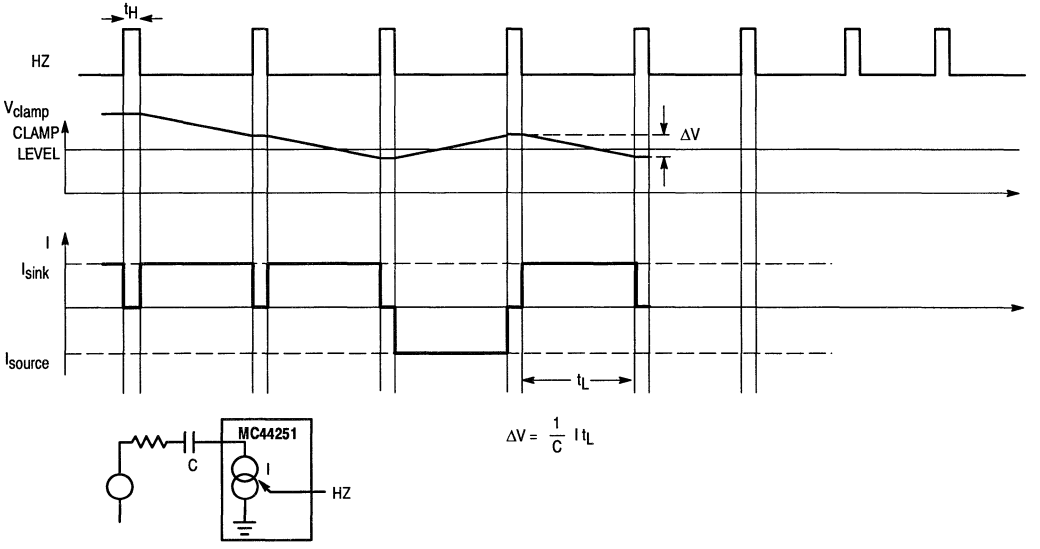


Figure 3a. Operation

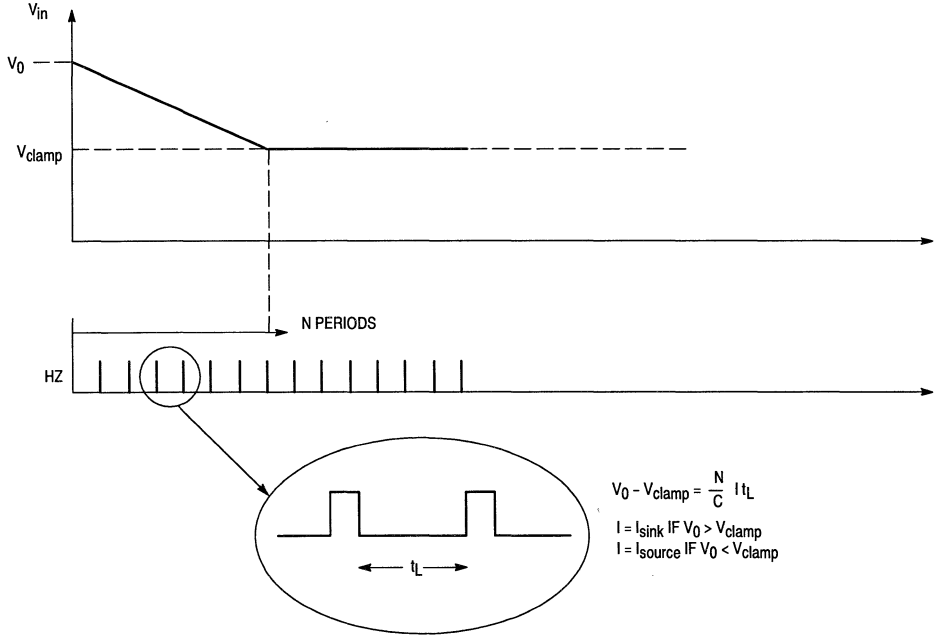


Figure 3b. Power Up

Figure 3. Clamp Network Timing Diagrams

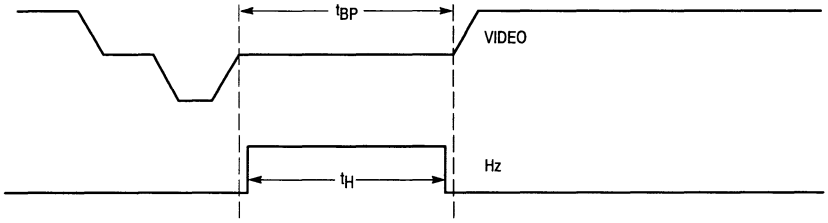


Figure 4. Horizontal Timing

DITHERING

Dithering can be used to reduce the errors that are the result of the digitizing process used to convert video information between analog and digital forms. This method can also be applied to non–video signals. When converting analog signals to a digital format, errors can be introduced because of the limited number of discrete levels that the digital system imposes. For example, an 8–bit digital word can describe exactly 256 discrete analog levels. In some cases, this may not be sufficient for the application involved.

One solution is to increase the number of bits that describe the analog signal. The disadvantages of this approach are the increase in cost of the converter and the loss in speed associated with the increased number of bits. The addition of analog filters at the point where the digital information is converted back to analog is also possible, but this also has its limitations.

When a ramp voltage is generated from a digital source or an analog ramp is converted to a digital form and back to analog, the limited number of vertical samples causes the ramp to take the form of a "stair case" (see Figure 5). The severity of this distortion depends on the number of digital bits that generated the ramp. The "stair case" effect is less pronounced when the number of bits producing the ramp is increased.

When processing video information using a YUV form and a luminance ramp is displayed, granulation errors may become noticeable. This condition can also occur when one of the RGB signals is ramped and the other two are held constant. When processing video information using 24–bits or less, this "granulation" can be observed. Since the video is processed as three 8–bit signals, the maximum number of different luminance levels is reduced to 256. In cases where only a 7–bit luminance signal is used, the maximum number of luminance levels is reduced to 128. The uniform luminance ramp is observed on the display as vertical bars rather than a uniform luminance change.

The dithering technique consists of adding a small offset to the input signal. This offset (when it is equal to an integer number of LSB) is then subtracted from the digital output data. This offset is varied "line–to–line" by one half LSB steps. It allows each point of the waveform to be interpolated to higher precision by averaging the differential linearity errors on the screen.

The addition of the small offset forces the comparators to sample at a slightly different point on the input waveform (see Figure 6). When translated to the display, the effect is to shift this value slightly to the left. Overall accuracy of the display is maintained by subtracting this value from the output when the shift is equal to an integer number of LSB. For a uniform and continuous video waveform, the result of incrementing and decrementing the dither voltage is to effectively double the luminance levels from 256 to 512. The effect is to broaden the luminance range. This results in a more pleasing display with less visible quantization.

The dithering pattern is generated by means of a binary counter, which is incremented for every line by input HZ, and reset by every second vertical input VTN; thus, the dithering pattern is synchronized to the deflection of the screen. The effect of the dithering pattern is given in Figure 7. Subsequent subtraction of the introduced dithering signal at the output of each ADC is performed by a binary adder. The dither counter, and hence the dithering function, may be stopped by holding VTN low. Depending on the state of the dither counter, the output code range can be either from $00 to$FE or from $01 to $FF.

Depending on the state of the dither counter, the output code range can be either from S00 to SFE or from S01 to SFF.

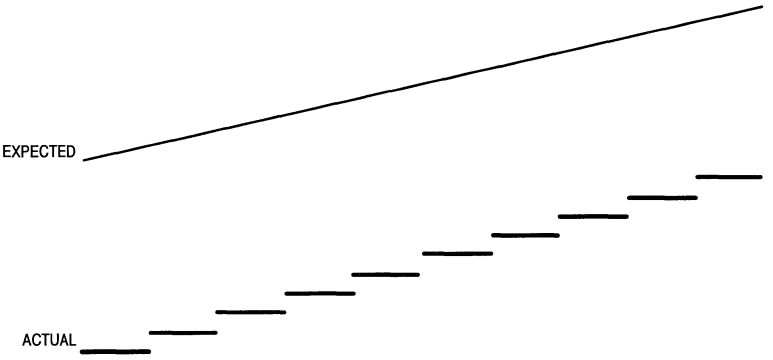


Figure 5. Distortion Produced by Digitizing

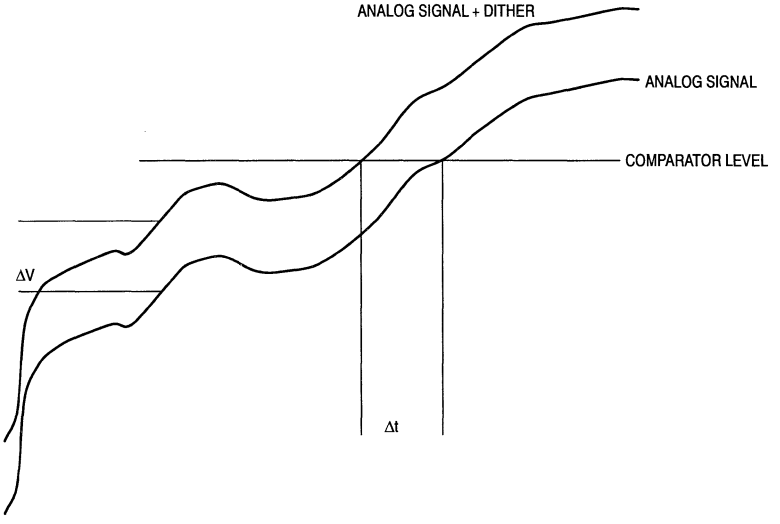


Figure 6. Amplitude Dithering

RESTRICTIONS ON $V_{DD(R)}$

The normal operating condition for the MC44251 is defined as $V_{DD(R)} = V_{DD(A)} = V_{DD(D)}$ and the safe operating range of $V_{DD(R)}$ is defined as $0 \leq V_{DD(R)} \leq V_{DD}$. In cases where $V_{DD(R)}$ is operated at values other than V_{DD}, it should be noted that the accuracy of the conversion process is reduced. In all cases $V_{DD(R)}$ should not be allowed to exceed V_{DD}.

The step size is defined as SS(n) and the ideal step size is defined as SSI. We may define an error component, ∂, as the difference between the actual step size and the ideal step size so that

$$\partial = |SSI - SS(n)|.$$

We may also define a worst case value for ∂ as

$$\partial \leq \partial w$$

where ∂w is the greatest value of ∂. The origin of this error is the offset mismatch from one comparator to another and is nearly independent of $V_{DD(R)}$ and V_{DD}.

Since ∂ is nearly independent of $V_{DD(R)}$, its value will remain constant for all values of $V_{DD(R)}$.

The step size error, SSE, is defined as

$$SSE(n) = (SSI - SS(n))/SSI = \partial(n)/SSI.$$

Furthermore, the ideal step size SSI is defined as

$$SSI = V_{DD(R)} \times 0.6/255.$$

Since ∂ is a constant and SSI is proportional to $V_{DD(R)}$, the step size error, SSE, will increase as $V_{DD(R)}$ is decreased. Further study will show that the differential nonlinearity, DNL, will also increase as $V_{DD(R)}$ is reduced. To minimize these errors it is desirable to keep $V_{DD(R)}$ as high as possible. Since the maximum value for $V_{DD(R)}$ is V_{DD},

$$V_{DD(R)} = V_{DD(D)} = V_{DD(A)}$$

is the value that produces the greatest conversion accuracy.

INPUT VOLTAGE RANGE

In applications where the input signals are dc coupled to the MC44251, the following restrictions apply:

If $V_{in} \leq V_{min}$, then the output code = \$00 or \$01 (depending on the dither generator).

If $V_{in} \geq V_{max}$, then the output code = \$FE or \$FF (depending on the dither generator).

If $V_{min} \leq V_{in} \leq V_{max}$, then the output code reflects the correct value of the input voltage.

If the input is video based and ac coupled, then the input voltage range for V_{in} without saturation is

$$0 \leq V_{in} \leq V_{range}.$$

For V_{in} this reflects a maximum video input level before saturation of about 3 V for V_{DD} = 5 V.

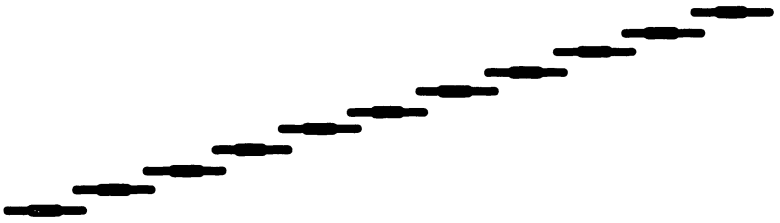


Figure 7. Effect of Dithering Pattern

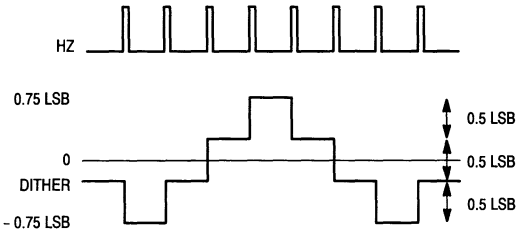


Figure 8. Dithering Sequence

DEFINITIONS

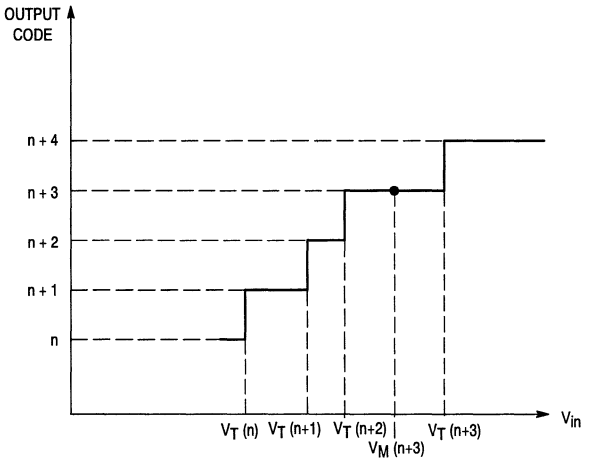


Figure 9.

- **Transition Voltage:** Voltage at which transition from step n to step n+1 occurs = $V_T(n)$.

- **Step Size:** Difference between two consecutive transition voltages.

$$SS(n) = V_T(n) - V_T(n-1)$$

- **Mid–Point Voltage:**

$$V_M(n) = \frac{V_T(n) + V_T(n-1)}{2}$$

$$V_M(\text{max code}) = \frac{V_{DD(R)} + V_T(\text{max code} - 1)}{2}$$

- **Step Size Ideal:**

$$\frac{V_{range}}{255} = SSI$$

- **Differential Nonlinearity (DNL):**

$$DNL(n) = \frac{V_M(n+1) - V_M(n)}{SSI} - 1 \text{ in LSB}$$

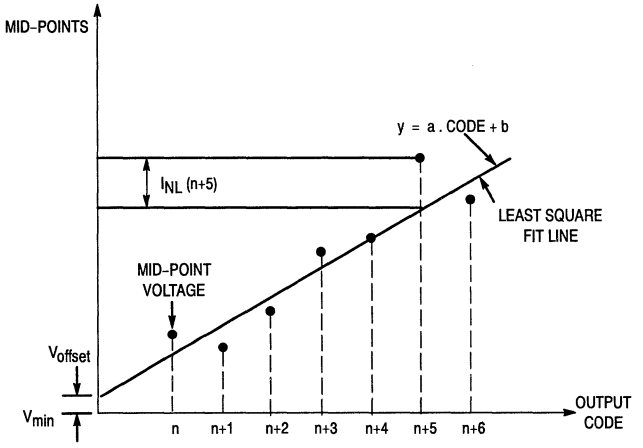


Figure 10. Integral Nonlinearity and Offset

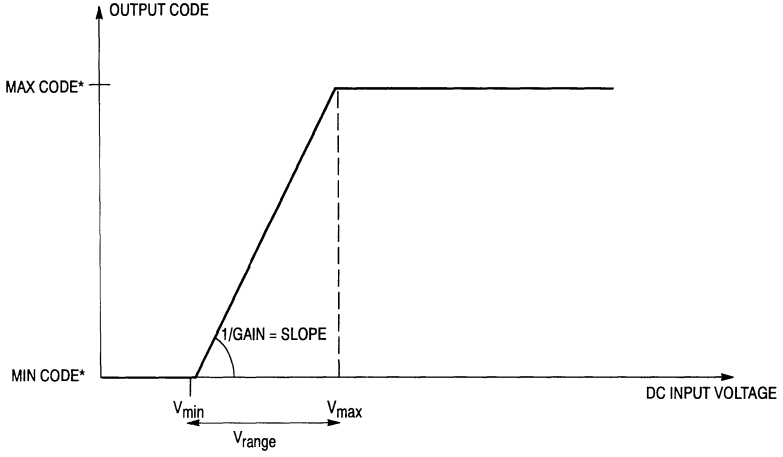
- **Integral Nonlinearity (I_{NL}) and Offset:**

$$I_{NL}(n) = \frac{V_M(n) - a \bullet n - b}{SSI} \text{ in LSB}$$

Note: I_{NL} (min code) and I_{NL} (max code) is not defined.

- **Gain:** Gain = a in the formula Y = a • code + b
or the slope in the curve mid–points = f(code)

- **V_{offset}:** $V_{offset} = b - V_{min}$



*See dither generator.
LSB ideal = V_{range} /255
(Min code = 0 or 1; see dither generator)

Figure 11.

APPLICATION INFORMATION

PCB DESIGN

To maximize the performance of the MC44251, noise should be kept to a minimum. Good printed circuit board design will enhance the operation of the MC44251. Separate analog and digital grounds will reduce noise and conversion errors. In addition, separate filters on analog V_{CC} and digital V_{DD} will also help to minimize noise and conversion errors. Sufficient decoupling and short leads will also improve performance.

When designing mixed analog/digital printed circuit boards, separate ground planes for digital ground and analog ground should be employed. Large switching currents generated by digital circuits will be amplified by analog circuitry and can quickly make a circuit unusable. Care should be taken to ensure analog ground does not inadvertently become part of the digital ground. The analog and digital grounds should be connected together at only one point. This is usually at or near where power enters the printed circuit board. Additionally, when interconnecting several printed circuit boards together, care must be taken to ensure that cabling does not interconnect digital and analog grounds together to produce a path for digital switching currents through analog ground.

When using any device with the performance and speed of the MC44251, ground planes are essential. Loosely interconnected traces and/or random areas of ground strewn around the printed circuit board are inadequate for high performance circuitry. While distribution of V_{DD} and V_{CC} can be done by bussing, to do so with the ground system is disastrous.

An inch long conductor is an 18 nH inductor. The cross sectional area of the conductor affects the exact value of the inductance, but for most PCB traces this is approximately correct. If the ground system is composed of traces or clumps of ground loosely interconnected, it will be inductive. The amount of inductance will be proportional to the length of the conductors making up the ground. This inductance cannot be decoupled away. It must be designed out.

A CMOS device exhibits a characteristic input capacitance of about 10 pF. If this gate is driven by a digital signal that switches 2.5 V in a period of 5 ns, the equation for the average current flowing during the switching time will be:

$$I_{AV} = Cdv/dt.$$

A voltage change of 2.5 V in 5 ns requires an average current of 5 mA. If we assume a linear ramp starting from zero, the total change in current will be 10 mA. The change in current per nanosecond per gate can be found by dividing the change in current by the time

$$10\ mA/5\ ns = 2\ mA/ns.$$

For a device with 16 outputs driving one gate for each output,

$$di/dt = 16 \times 2\ mA/ns = 32\ mA/ns.$$

If the above 1–inch wire is in this current path, then the voltage dropped across it can be found from the formula

$$V = Ldi/dt = 18\ nH \times 32\ mA/ns = 0.576\ V.$$

If the inductor is in the ground system, it is in the signal path. The voltage generated by the switching currents through this inductor will be added to the signal. At best it will be superimposed on the analog signal as unwanted noise. At worst, it can render the entire circuit unusable. Even the digital signal path is not immune to this type of signal. It can false trigger clock circuits causing timing errors, confuse comparator type circuits, and cause digital signals to be misinterpreted as wrong values.

When laying out the PCB, use electrolytic capacitors of sufficient size at the power input to the printed circuit board. Adding low ESR decoupling capacitors of about 0.1 μF capacitance across V_{CC} and/or V_{DD} at each device will help reduce noise in general and ESD susceptibility. Implementation of a good ground plane ground system can all but eliminate the type of noise described above.

To summarize, use sufficient electrolytic capacitor filtering, make separate ground planes for analog ground and digital ground, tie these grounds together at one and only one point, keep the ground planes as continuous and unbroken as possible, use low ESR capacitors of about 0.1 μF capacitance on V_{CC} and V_{DD} at each device, and keep all leads as short as possible.

EMI SUPPRESSION

When using ICs in or near television receiver circuits, EMI (electromagnetic interference) and subsequent unwanted display artifacts and distortion are probable unless adequate EMI suppression is implemented. A common misconception is that some offending digital device is the culprit. This is erroneous in that an IC itself has insufficient surface area to produce sufficient radiation. The device, while it is the generator of interfering signals, must be coupled to an antenna before EMI is radiated. The source for the EMI is not the IC which generates the offending signals but rather the circuitry which is attached to the IC.

Potential EMI signals are generated by ***all*** digital devices. Whether they become a nuisance is dependent upon their frequency and whether they have a sufficient antenna. The frequency and number of these signals is affected by both circuit design within the IC and the manufacturing process. Device speed is also a major contributor of potential EMI. Because the design is determined by the anticipated application, the manufacturing process is fixed and the drive for speed ever increasing, the only effective point to implement EMI suppression is in the PC board design. The PC board usually is the antenna which radiates the EMI. The most efficient method of minimizing EMI radiation is to minimize the efficiency of this antenna.

The most common cause of inadequate EMI suppression lies with the ground system of the suspected digital devices. As pointed out previously, di/dt transitions can be significant in digital circuits. If the di/dt transitions appear in the ground system and the ground system is inductive, the harmonics present in these transitions are a source of potential EMI signals. The unfortunate result of putting digital devices on a reactive ground system is guaranteed EMI problems.

The area which should be addressed first as a potential EMI source is the ground. Without an adequate ground system, EMI cannot be effectively reduced by decoupling. If at all possible, the ground should be a complete unbroken plane. Figure 12 shows two examples of relieving ground around device pins. When relieving vias and plated through holes, large areas of ground loss should be avoided. When

the relief pattern is equal to half the distance between pins, over etching and process errors may remove ground between pins. If sufficient ground around enough pins are removed, the ground system can become isolated or nearly isolated "patches" which will appear inductive. If ground, such as the vicinity of an IC, must be removed, replace with a cross hatch of ground lines with the mesh as small as possible.

If a single unbroken plane can be devoted to the ground system, EMI can usually be sufficiently suppressed by using ferrite beads on suspect EMI paths and decoupling with adequate values of capacitors. The value of the decoupling capacitor depends on the frequency and amplitude of the offending signals. Ferrite beads are available in a wide variety of shape, size and material to fit virtually any application.

Choose a ferrite bead for desired impedance at the desired frequency and construct a low pass filter using one or more appropriate capacitors in a "L", "T" or "PI" arrangement. Use only capacitors of low inductive and resistive properties such as ceramic or mica. Install filters in series with each IC pin suspected of contributing offending EMI signals and as close to the pin as possible. Analysis using a spectrum analyzer can help determine which pins are suspect.

Where PC board costs constrain the number of layers available, and if the EMI frequencies are far removed from the frequencies of operation, ferrite beads and decoupling capacitors may still be effective in reducing EMI emissions. Where only two (or in some cases, only one!) layer is used, the ground system is always reactive and poses an EMI problem. If the offending EMI and normal operating frequency differ sufficiently, filtering can still work.

An "island" is constructed in the ground system for the digital device using ferrite beads and decoupling capacitors as shown by the example in Figure 13. The ground must be cut so that the digital ground for the device is isolated from the rest of the ground system. Next choose a ferrite bead of the appropriate value. Install this bead between the isolated ground and the ground system. Install low pass filters in all suspect lines with the capacitor closest to the device pin connected to the isolated ground in all signal lines where EMI is suspect. Also cut the power to the device and insert a ferrite bead as shown in Figure 13. Finally, decouple the device between the power pin(s) and isolated ground pin(s) using a low inductive/resistive capacitor of adequate value.

The methods described above will work acceptably when the EMI frequency and the frequency of operation of the device generating the EMI differ greatly. Where the EMI is disturbing the high VHF or UHF channels and the device generating the EMI is operating within the NTSC/PAL bandwidth, the energy contained in the harmonics generating the EMI is situated well above the operating frequency and suppressing this type of EMI poses no great problem. However, if the EMI is present on low VHF channels and/or the operation of the device is outside the NTSC/PAL bandwidth, such as a 2X pixel clock or 4xfsc oscillator, compromise between video quality and suppression complexity is usually required to obtain an acceptable solution. For those cases where the operating frequency of the device is very near the frequency of the EMI disturbance, careful attention to PCB layout, multiple layer PCB and even shielding may be necessary to obtain an acceptable design.

APPLICATIONS CIRCUIT

Figure 14 shows a typical applications circuit. This circuit will produce analog–to–digital conversion of either RGB information or YUV information by setting SW1. In the YUV mode, SW1 is set either to position '1' or to the open position depending on the desired clamp level (see Table 1). The RGB inputs then become YUV inputs and correspondingly, the RGB outputs are YUV. For RGB operation, SW1 is set to the '0' position.

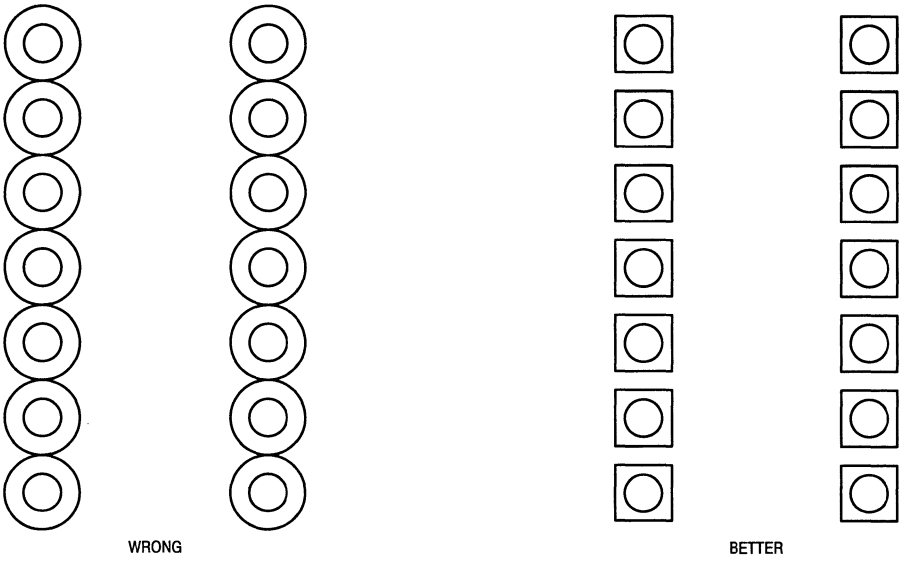


Figure 12.

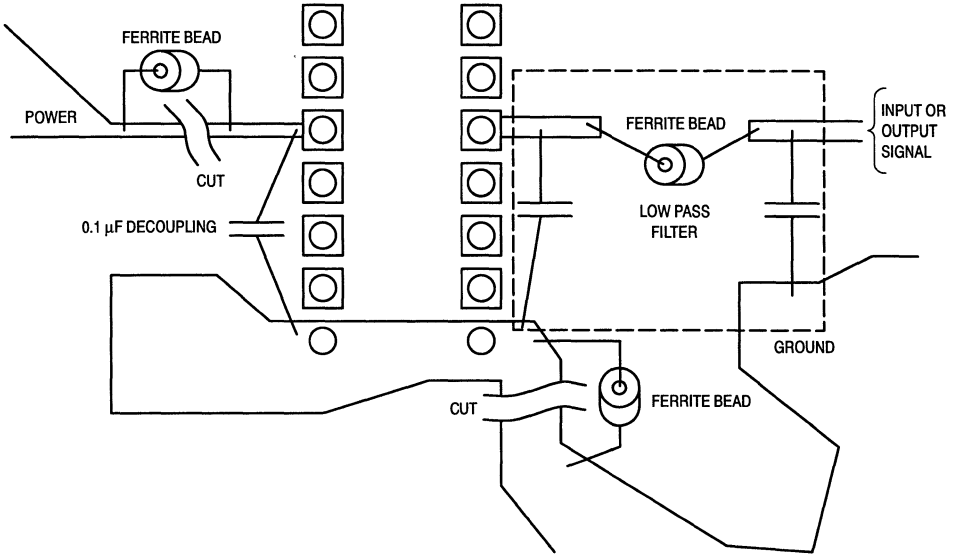


Figure 13.

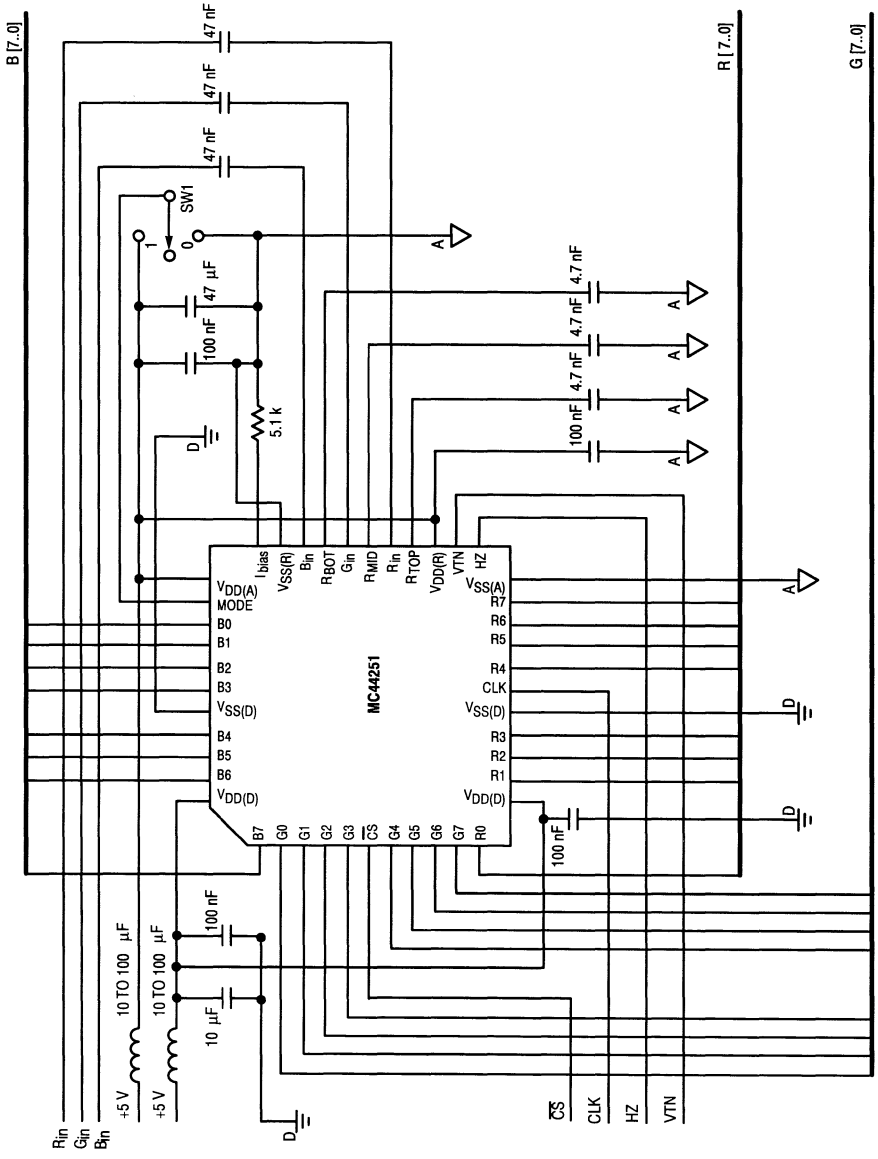


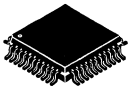
Figure 14. Application Circuit

MC44701

Product Preview

Multistandard Digital Video Encoder

HCMOS Technology



FU SUFFIX
44–LEAD QFP
CASE 824A–01

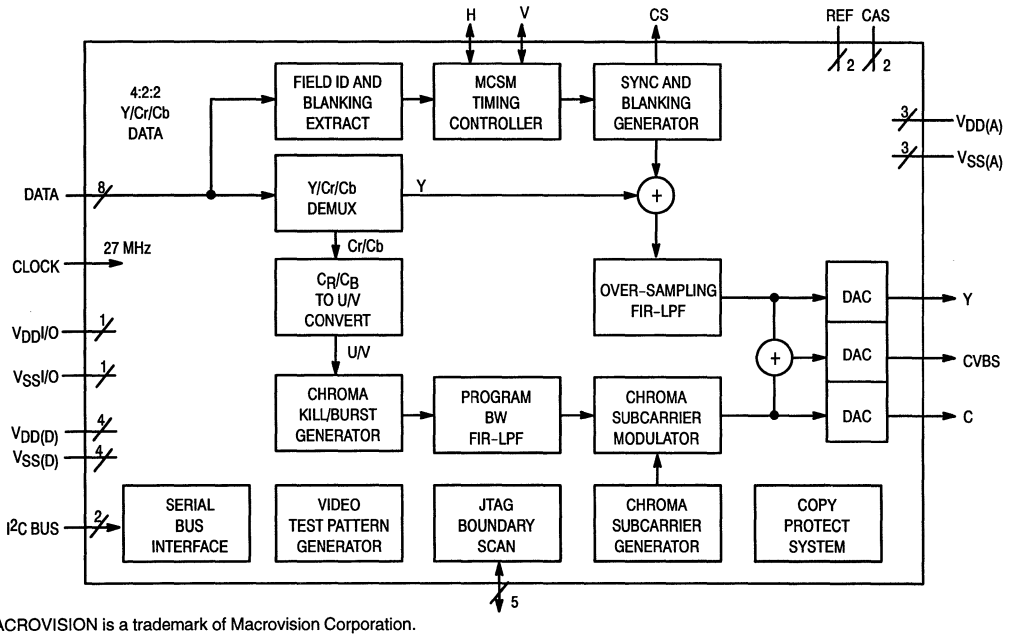
ORDERING INFORMATION
MC44701FU QFP

2

This device simultaneously outputs analog composite video, S–Video, in PAL or NTSC standards. It accepts multiplexed luminance and color–difference video–data from consumer–grade digital video sources, such as MPEG–I/II decoders. The device may be synchronized to the data source, or act as master. All necessary video processing and chroma subcarrier generation is performed digitally and requires no adjustment and very few external components. The MC44702 is a similar device that also provides RGB outputs and an OSD function.

- Worldwide Operation – 625/50 or 525/60, PAL or NTSC, 2:1 or 1:1
- Three I–DACs for Outputs of CVBS and Y/C at 1 V/75Ω
- 8–Bit Y/Cr/Cb Digital Inputs (CCIR–601(4:2:2)/656)
- Separate Composite Sync Output
- Closed–Caption Data Transparency
- MACROVISION™ Copy Protection System
- Built–In Video Test Pattern Generator
- 3 V or 5 V Digital I/O Interface
- I^2C–Bus Interface
- JTAG Boundary Scan

BLOCK DIAGRAM



MACROVISION is a trademark of Macrovision Corporation.

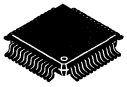
This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

MC44702

Product Preview

Multistandard Digital Video Encoder

HCMOS Technology



FU SUFFIX
52–LEAD QFP
CASE 848B–04

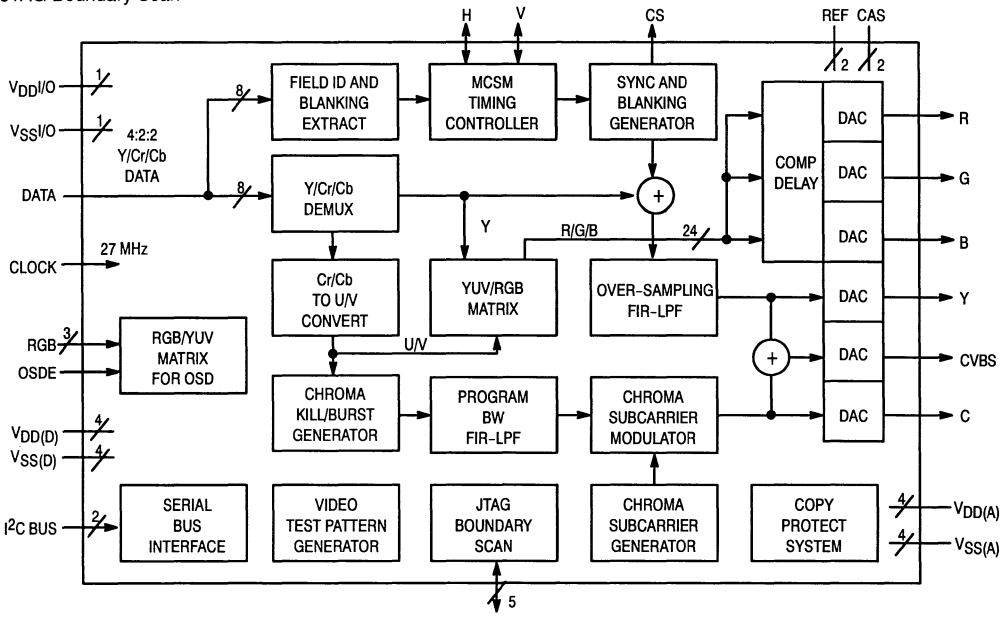
ORDERING INFORMATION
MC44702FU QFP

2

Like the MC44701, this device simultaneously outputs analog composite video, S–Video, in PAL or NTSC standards. This device also provides RGB outputs and an OSD function. It accepts multiplexed luminance and color–difference video–data from consumer–grade digital video sources, such as MPEG–I/II decoders. The device may be synchronized to the data source, or act as master. All necessary video processing and chroma subcarrier generation is performed digitally and requires no adjustment and very few external components.

- Worldwide Operation – 625/50 or 525/60, PAL or NTSC, 2:1 or 1:1
- Six I–DACs for Outputs of R/G/B/, Y/C and CVBS at 1 V/75Ω
- 8–Bit Y/Cr/Cb Digital Inputs (CCIR–601(4:2:2)/656)
- Auxiliary Digital RGB Inputs for 8–Color On Screen Display
- Separate Composite Sync Output
- Closed–Caption Data Transparency
- MACROVISION™ Copy Protection System
- Built–In Video Test Pattern Generator
- 3 V or 5 V Digital I/O Interface
- I^2C–Bus Interface
- JTAG Boundary Scan

BLOCK DIAGRAM



MACROVISION is a trademark of Macrovision Corporation.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

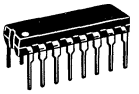
MC141543

2

Product Preview

Advanced Monitor On-Screen Display

CMOS

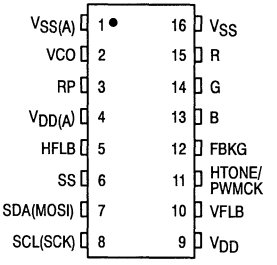


P SUFFIX
PLASTIC PACKAGE
CASE 648–08

ORDERING INFORMATION

MC141543P Plastic Dip

PIN ASSIGNMENT



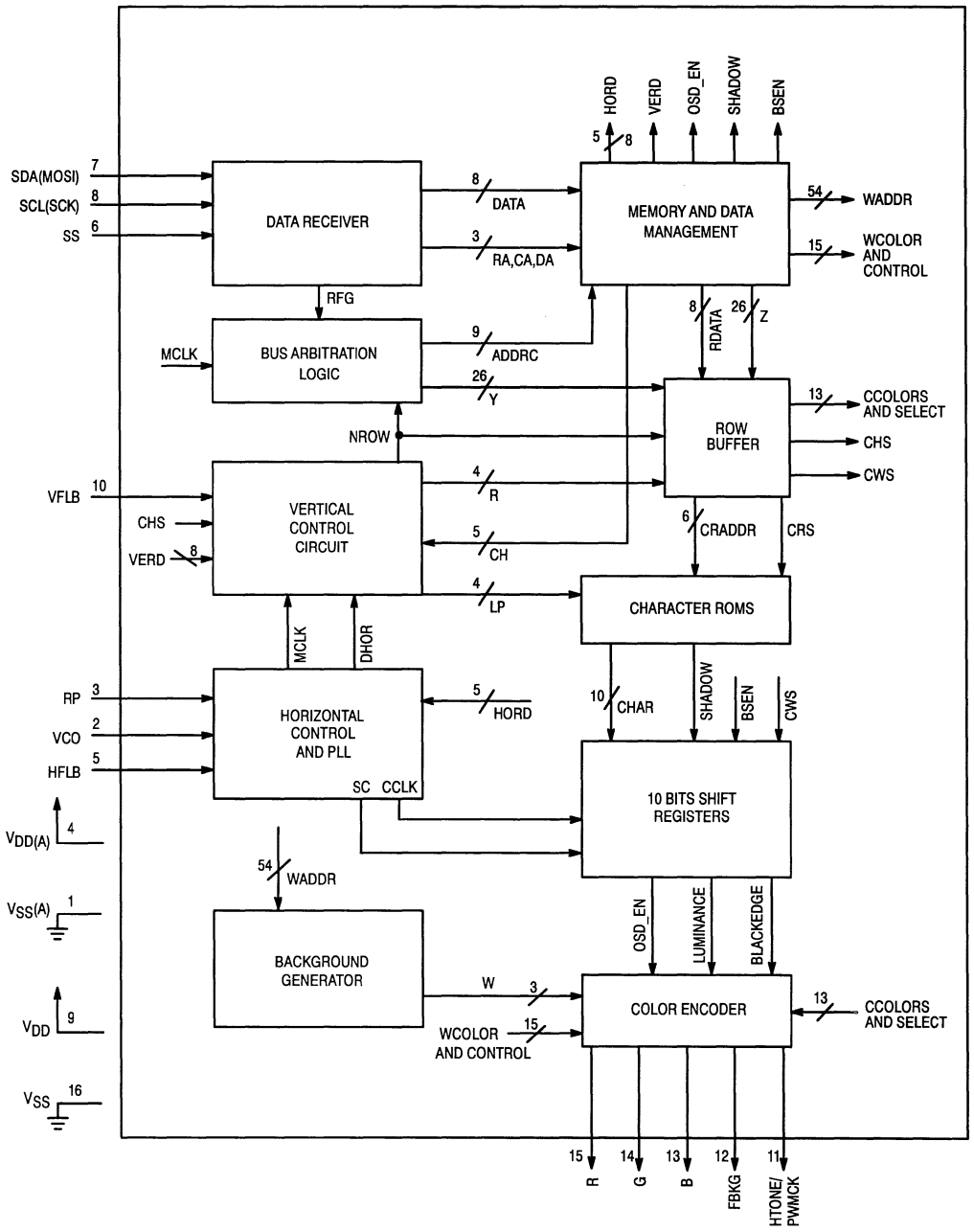
This is a high performance HCMOS device designed to interface with a microcontroller unit to allow colored symbols or characters to be displayed on a color monitor. Its on–chip PLL allows both multisystem operation and self generation of system timing. It also minimizes the MCU's burden through its built–in 493 bytes RAM. By storing a full screen of data and control information, this device has a capability to carry out 'screen–refresh' without any MCU supervision.

Since there is no clearance between characters, special graphics oriented characters can be generated by combining two or more character blocks. There are three different resolutions that users can choose. By changing the number of dots per horizontal line to 320 (CGA), 480 (EGA) or 640 (VGA), smaller characters with higher resolution can be easily achieved.

Special functions such as character bordering or shadowing, multi–level windows, double height and double width, and programmable vertical length of character are also incorporated. Furthermore, neither massive information update nor extremely high data transmission rate are expected for normal on–screen display operation and serial protocols are implemented in lieu of any parallel formats to achieve the minimum pin count.

- Three Selectable Resolutions : 320 (CGA), 480 (EGA) or 640 (VGA) Dots per Line
- Fully Programmable Character Array of 15 Rows by 30 Columns
- 493 Bytes Direct Mapping Display RAM Architecture
- Internal PLL Generates a Wide–Ranged System Clock
- For High End Monitor Application, Maximum Horizontal Frequency is 82 KHz
- Programmable Vertical Height of Character to Meet Multi–Sync Requirement
- Programmable Vertical and Horizontal Positioning for Display Center
- 128 Characters and Graphic Symbols ROM (Mask ROM is Optional)
- 10 x 16 Dot Matrix Character
- Character by Character Color Selection
- A Maximum of Four Selectable Colors per Row
- Double Character Height and Double Character Width
- Character Bordering or Shadowing
- Three Fully Programmable Background Windows with Overlapping Capability
- Provide a Clock Output Synchronous to the Incoming H Sync for External PWM
- M_BUS (IIC) Interface with Address $7A (SPI Bus is Mask Option)
- Single Positive 5 V Supply

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS Voltage Referenced to V_{SS}

Symbol	Characteristic	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to + 7.0	V
V_{in}	Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
Id	Current Drain per Pin Excluding V_{DD} and V_{SS}	25	mA
Ta	Operating Temperature Range	0 to 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

AC ELECTRICAL CHARACTERISTICS ($V_{DD}/V_{DD(A)}$ = 5.0 V, $V_{SS}/V_{SS(A)}$ = 0 V, T_A = 25C, Voltage Referenced to V_{SS})

Symbol	Characteristic	Min	Typ	Max	Unit
	Output Signal (R, G, B, FBKG and HTONE/PWMCK) C_{load} = 30 pF Rise Time				
t_r	Fall Time	—	—	6	ns
t_f		—	—	6	ns
$F_{\overline{HFLB}}$	HFLB Input Frequency	—	—	82 K	Hz

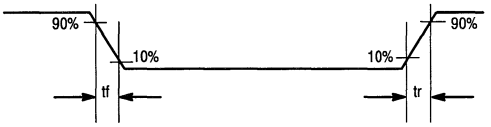


Figure 1. Switching Characteristics

DC CHARACTERISTICS $V_{DD}/V_{DD(A)}$ = 5.0 V ± 10%, $V_{SS}/V_{SS(A)}$ = 0 V, T_A = 25°C, Voltage Referenced to V_{SS}

Symbol	Characteristic	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage I_{out} = – 5 mA	V_{DD} – 0.8	—	—	V
V_{OL}	Low Level Output Voltage I_{out} = 5 mA	—	—	V_{SS} + 0.4	V
	Digital Input Voltage (Not Including SDA and SCL)				
V_{IL}	Logic Low	—	—	0.3 V_{DD}	V
V_{IH}	Logic High	0.7 V_{DD}	—	—	V
	Input Voltage of Pin SDA and SCL in SPI Mode				
V_{IL}	Logic Low	—	—	0.3 V_{DD}	V
V_{IH}	Logic High	0.7 V_{DD}	—	—	V
	Input Voltage of Pin SDA and SCL in M_BUS Mode				
V_{IL}	Logic Low	—	—	0.3 V_{DD}	V
V_{IH}	Logic High	0.7 V_{DD}	—	—	V
I_{II}	High–Z Leakage Current (R, G, B and FBKG)	– 10	—	+ 10	µA
I_{II}	Input Current (Not Including RP, VCO, R, G, B, FBKG and HTONE/PWMCK)	– 10	—	+ 10	µA
I_{DD}	Supply Current (No Load on Any Output)	—	—	+ 15	mA

PIN DESCRIPTION

VSS(A) (Pin 1)
This pin provides the signal ground to the PLL circuitry. Analog ground for PLL is separated from digital ground for optimal performance.

VCO (Pin 2)
A dc control voltage input to regulate an internal oscillator frequency. See the Application Diagram for the application values used.

RP (Pin 3)
An external RC network is used to bias an internal VCO to resonate at the specific dot frequency. The maximum voltage at Pin 3 should not exceed 3.5 V at any condition. See the Application Diagram for the application values used.

$V_{DD(A)}$ (Pin 4)
A positive 5 V dc supply for PLL circuitry. Analog power for PLL is separated from digital power for optimal performance.

$\overline{\text{HFLB}}$ (Pin 5)
This pin inputs a negative polarity horizontal synchronize signal pulse to phase lock into an internal system clock generated by the on–chip VCO circuit.

$\overline{\text{SS}}$ (Pin 6)
This input pin is part of the SPI system. An active low signal generated by the master device enables this slave device to accept data. Pull high to terminate the SPI communication. If M_BUS is employed as the serial interface, this pin should be tied to either V_{DD} or V_{SS}.

SDA (MOSI) (Pin 7)
Data and control message are being transmitted to this chip from a host MCU, via one of the two serial bus systems. With either protocol, this wire is configurated as a uni–directional data line. (Detailed description of these two protocols will be discussed in the M_BUS and SPI sections).

SCL (SCK) (Pin 8)
A separate synchronizing clock input from the transmitter is required for either protocol. Data is read at the rising edge of each clock signal.

V_{DD} (Pin 9)
This is the power pin for the digital logic of the chip.

$\overline{\text{VFLB}}$ (Pin 10)
Similar to Pin 5, this pin inputs a negative polarity of vertical synchronize signal to synchronize the vertical control circuit.

HTONE/PWMCK (Pin 11)
This is a multiplexed pin. When the PWMCK_EN bit is cleared after power on or by the MCU, this pin is HTONE and outputs a logic high during windowing except when graphics or characters are being displayed. It is used to lower the external R, G, B amplifiers gain to achieve a transparent windowing effect. If the PWMCK_EN bit is set to 1 via M_BUS or SPI, this pin is changed to a mode–dependent clock output with 50/50 duty cycle and synchronous with the input horizontal synchronization signal at Pin 5. The frequency is dependent on the mode in which the AMOSD is currently running. The exact frequencies in the different resolution modes are described below.

Table 1. PWM CLK Frequency

Resolution	Frequency	Duty Cycle
320 dots/line	32 x H_f	50/50
480 dots/line	48 x H_f	50/50
640 dots/line	64 x H_f	50/50

NOTE: H_f is the frequency of the input H sync. on Pin 5.

Typically, this clock is fed into an external pulse width modulation module as its clock source. Because of the synchronization between PWM clock and H sync, a better performance on the PWM controlled functions can be achieved.

FBKG (Pin 12)

This pin will output a logic high while displaying characters or windows when FBKGC bit in frame control register is 0, and output a logic high only while displaying characters when FBKGC bit is 1. It is defaulted to high impedance state after power on, or when there is no output. An external 10 kΩ resistor pulled low is recommended to avoid level toggling caused by hand effect when there is no output.

B,G,R (Pin 13,14,15)

AMOSD color output in TTL level to the host monitor. These three signals are active high output pins which are in high impedance state when AMOSD is disabled.

V_{SS} (Pin 16)

This is the ground pin for the digital logic of the chip.

SYSTEM DESCRIPTION

MC141543 is a full screen memory architecture. Refresh is done by the built–in circuitry after a screenful of display data has been loaded in through the serial bus. Only changes to the display data need to be input afterward.

Serial data, which includes screen mapping address, display information, and control messages, are being transmitted via one of the two serial buses: M_BUS or SPI (mask option). These two sets of buses are multiplexed onto a single set of wires. Standard parts offer M_BUS transmission.

Data is first received and saved in the MEMORY MANAGEMENT CIRCUIT in the Block Diagram. Meanwhile, the AMOSD is continuously retrieving the data and putting it into a ROW BUFFER for display and refreshing, row after row. During this storing and retrieving cycle, a BUS ARBITRATION LOGIC will patrol the internal traffic, to make sure that no crashes occur between the slower serial bus receiver and fast 'screen–refresh' circuitry. After the full screen display data is received through one of the serial communication interface, the link can be terminated if change on display is not required.

The bottom half of the Block Diagram constitutes the heart of this entire system. It performs all the AMOSD functions such as programmable vertical length (from 16 lines to 63 lines), display clock generation (which is phase locked to the incoming horizontal sync signal at Pin 5 $\overline{HFLB}$), bordering or shadowing, and multiple windowing.

COMMUNICATION PROTOCOLS

M_BUS Serial Communication

This is a two–wire serial communication link that is fully compatible with the IIC bus system. It consists of SDA bidirectional data line and SCL clock input line. Data is sent from a transmitter (master), to a receiver (slave) via the SDA line, and is synchronized with a transmitter clock on the SCL line at the receiving end. The maximum data rate is limited to 100 kbps.The default chip address is $7A.

Operating Procedure

Figure 2 shows the M_BUS transmission format. The master initiates a transmission routine by generating a START condition, followed by a slave address byte. Once the address is properly identified, the slave will respond with an ACKNOWLEDGE signal by pulling the SDA line LOW during the ninth SCL clock. Each data byte which then follows must be eight bits long, plus the ACKNOWLEDGE bit, to make up nine bits together. Appropriate row and column address information and display data can be downloaded sequentially in one of the three transmission formats described in DATA TRANSMISSION FORMATS SECTION. In the cases of no ACKNOWLEDGE or completion of data transfer, the master will generate a STOP condition to terminate the transmission routine. Note that the OSD_EN bit must be set after all the display information has been sent in order to activate the AMOSD circuitry of MC141543, so that the received information can then be displayed.

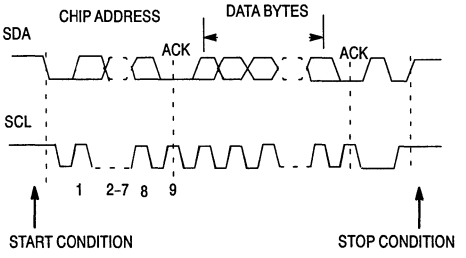


Figure 2. M_BUS Format

Serial Peripheral Interface (SPI)

Similar to M_BUS communication, SPI requires separate clock (SCK) and data (MOSI) lines. In addition, a $\overline{SS}$ SLAVE SELECT pin is controlled by the master transmitter to initiate the receiver.

Operating Procedure

To initiate SPI transmission, pull $\overline{SS}$ pin low by the master device to enable MC141543 to accept data. The $\overline{SS}$ input line must be a logic low prior to occurrence of SCK and remain low until and after the last (eighth) SCK cycle. After all data has been sent, the $\overline{SS}$ pin is then pulled high by master to terminate the transmission. No slave address is needed for SPI. Hence, row and column address information and display data (the data transmission formats are the same as in M_BUS mode described in the previous section) can be sent immediately after the SPI is initiated.

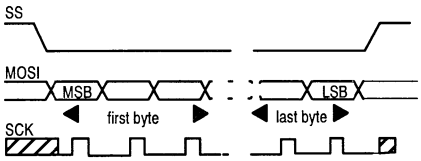


Figure 3. SPI Protocol

DATA TRANSMISSION FORMATS

After the proper identification by the receiving device, data train of arbitrary length is transmitted from the master. There are three transmission formats from (a) to (c) as stated below. The data train in each sequence consists of row address (R), column address (C), and display information (I), as shown in Figure 4. In format (a), display information data must be preceded with the corresponding row address and column address. This format is particularly suitable for updating small amounts of data between different rows. However, if the current information byte has the same row address as the one before, format (b) is recommended. For a full screen pattern change which requires a massive information update, or during power up situation, most of the row and column addresses on either (a) or (b) format will appear to be redundant. A more efficient data transmission format (c) should be applied. This sends the RAM starting row and column addresses once only, and then treats all subsequent data as display information. The row and column addresses will be automatically incremented internally for each display information data from the starting location.

The data transmission formats are:

(a) R – > C– > I –> R – > C – > I – > . . . . . .

(b) R – > C – > I – > C – > I – > C – > I. . . . . .

(c) R – > C – > I – > I – > I – > . . . . . .

To differentiate the row and column addresses when transferring data from master, the MSB (Most Significant Bit) is set as in Figure 5: '1' to represent row, while '0' for column address. Furthermore, to distinguish the column address between format (a), (b) and (c), the sixth bit of the column address is set to '1' which represents format (c), and a '0' for format (a) or (b). There is some limitation on using mix–formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

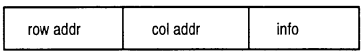


Figure 4. Data Packet

ADDRESS	BIT								FORMAT
	7	6	5	4	3	2	1	0	
ROW	1	X	X	X	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don't care D: valid data

Figure 5. Row & Column Address Bit Patterns

MEMORY MANAGEMENT

Internal RAM is addressed with row and column (coln) number in sequence. The spaces between row 0 and coln 0 to row 14 and coln 29 are called display registers, and each contains a character ROM address corresponding to display location on monitor screen. Every data row is associated with two control registers, which locate at coln 30 and 31 of their respective rows, to control the characters display format of that row. In addition, three window control registers for each of three windows together with three frame control registers occupy the first 13 columns of row 15 space.

The user should handle the internal RAM address location with care, especially for those rows with double length alphanumeric symbols. For example, if row n is destined to be double height on the memory map, the data displayed on screen row n and n+1 will be represented by the data contained in the memory address of row n only. The data of next row n+1 on the memory map will appear on the screen of n+2 and n+3 row space and so on. Hence, it is not necessary to throw in a row of blank data to compensate for the double row action. The user needs to take care of excessive rows of data in memory in order to avoid overrunning the limited number of row space on the screen.

There is difference for rows with double width alphanumeric symbols. Only the data contained in the even numbered columns of the memory map will be shown; the odd numbered columns will be ignored and not disclosed.

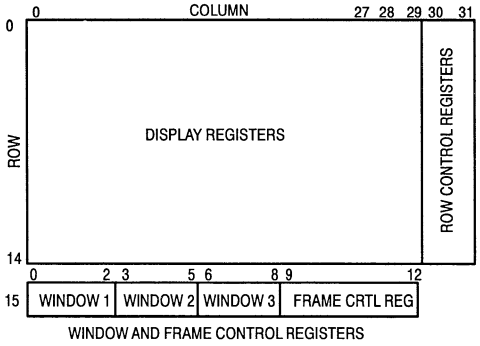
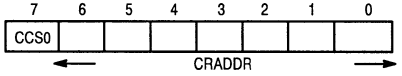


Figure 6. Memory Map

REGISTERS

Display Register



Bit 7 CCS0 – This bit defines a specific character color out of the two preset colors. Color 1 is selected if this bit is cleared, and color 2 otherwise.

Bit 6–0 CRADDR – These seven bits address the 128 characters or symbols residing in the character ROM.

Row Control Registers

Coln 30

	7	6	5	4	3	2	1	0
COLN 30	R1	G1	B1	R2	G2	B2	CHS	CWS

Bit 7–2 Color 1 is determined by R1, G1, B1 and color 2 by R2, G2, B2.

Bit 1 CHS – It determines the height of a display symbol. When this bit is set, the symbol is displayed in double height.

Bit 0 CWS – Similar to bit 1, character is displayed in double width, if this bit is set.

Coln 31

	7	6	5	4	3	2	1	0
COLN 31	R3	G3	B3	R4	G4	B4		

Bit 7–2 Color 3 and 4 are defined by R3, G3, B3, and R4, G4, B4 respectively.

Window 1 Registers

Row 15 Coln 0

	7	6	5	4	3	2	1	0
ROW 15 COLN 0	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

Row 15 Coln 1

	7	6	5	4	3	2	1	0
ROW 15 COLN 1	COL START ADDR MSB			LSB	WEN	CCS1		

Bit 2 WEN – It enables the background window 1 generation if this bit is set.

Bit 1 CCS1 – This additional color select bit provides the characters residing within window 1 with two extra color selections, making a total of four selections for that row.

Row 15 Coln 2

	7	6	5	4	3	2	1	0
ROW 15 COLN 2	COL END ADDR MSB			LSB	R	G	B	

Bit 2–0 R, G and B – Controls the color of window 1. Window 1 occupies Column 0–2 of Row 15. Window 2 from Column 3–5, and Window 3 from 6–8. Window 1 has the highest priority, and Window 3 the least. If window overlapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 2 Registers

Row 15 Coln 3

	7	6	5	4	3	2	1	0
ROW 15 COLN 3	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

Row 15 Coln 4

	7	6	5	4	3	2	1	0
ROW 15 COLN 4	COL START ADDR MSB			LSB	WEN	CCS1		

Bit 2 WEN – It enables the background window 2 generations if this bit is set.

Bit 1 CCS1 – This additional color select bit provides the characters residing within window 2 with two extra color selections, making a total of four selections for that row.

Row 15 Coln 5

	7	6	5	4	3	2	1	0
ROW 15 COLN 5	COL END ADDR MSB			LSB	R	G	B	

Bit 2–0 R, G and B – Controls the color of window 2. Window 1 occupies Column 0–2 of Row 15. Window 2 from Column 3–5, and Window 3 from 6–8. Window 1 has the highest priority, and Window 3 the least. If window overlapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 3 Registers

Row 15 Coln 6

	7	6	5	4	3	2	1	0
ROW 15 COLN 6	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

Row 15 Coln 7

	7	6	5	4	3	2	1	0
ROW 15 COLN 7	COL START ADDR MSB			LSB	WEN	CCS1	PWMCK_EN	

Bit 2 WEN – It enables the background window 3 generations if this bit is set.

Bit 1 CCS1 – This additional color select bit provides the characters residing within window 3 with two extra color selections, making a total of four selections for that row.

Bit 0 PWMCK_EN – When this bit is set to 1, HTONE/PWMCK pin will be switched to a clock output which is synchronous to the H sync and used as an external PWM (pulse width modulation) clock source. Refer to the pin description of HTONE/PWMCK for more information. After power on, the default value is 0.

Row 15 Coln 8

	7	6	5	4	3	2	1	0
ROW 15 COLN 8	COL END ADDR MSB				LSB	R	G	B

Bit 2–0 R, G and B – Controls the color of window 3. Window 1 occupies Column 0–2 of Row 15. Window 2 from Column 3–5, and Window 3 from 6–8. Window 1 has the highest priority, and Window 3 the least. If window overlapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Frame Control Registers

Frame Control Register Row 15 Coln 9

	7	6	5	4	3	2	1	0
COLN 9	VERTD MSB							LSB

Bit 7–0 VERTD – These eight bits define the vertical starting position. Total 256 steps, with an increment of four horizontal lines per step for each field. Its value cannot be zero anytime. The default value is 4.

Frame Control Register Row 15 Coln 10

	7	6	5	4	3	2	1	0
COLN 10		MSB HORD						LSB

Bit 6–0 HORD – Horizontal starting position for character display. Seven bits give a total of 128 steps and each increment represents five dots movement shift to the right on the monitor screen. Its value cannot be zero anytime. The default value is 15.

Frame Control Register Coln 11

	7	6	5	4	3	2	1	0
COLN 11			CH5	CH4	CH3	CH2	CH1	CH0

Bit 5–0 CH5–CH0 – These six bits will determine the displayed character height. It is possible to have a proper character height by setting a value greater than or equal to 16 on different horizontal frequency monitor. Setting a value below 16 will not have a predictable result. Figure 7 illustrates how this chip expands the built–in character font to the desired height.

Frame Control Register Coln 12

	7	6	5	4	3	2	1	0
COLN 12	OSD_EN	BSEN	SHADOW	X64	X32B			FBKGC

Bit 7 OSD_EN – OSD circuit is activated when this bit is set.

Bit 6 BSEN – It enables the character bordering or shadowing function when this bit is set.

Bit 5 SHADOW – Character with black–edge shadowing is selected if this bit is set; otherwise bordering prevails.

Bit 4, 3 X64, X32B – It determines the number of dots per horizontal line. There are 320 dots per horizontal line if bit X32B is clear and this is also the default power on state. Otherwise, 480 dots per horizontal sync line is chosen when bit X64 is clear and 640 dots per horizontal sync line when bit X64 is set to 1. Refer to Table 2 for details.

Bit 0 FBKGC – It determines the configuration of FBKG output pin. When it is clear, the FBKG pin outputs high while displaying characters or windows; otherwise, the FBKG pin outputs high only while displaying characters.

Table 2. Resolution Setting

(X64, X32B)	(0 , 0)	(1 , 0)	(0 , 1)	(1 , 1)
Dots / Line	320	320	480	640
Resolution	CGA	CGA	EGA	VGA

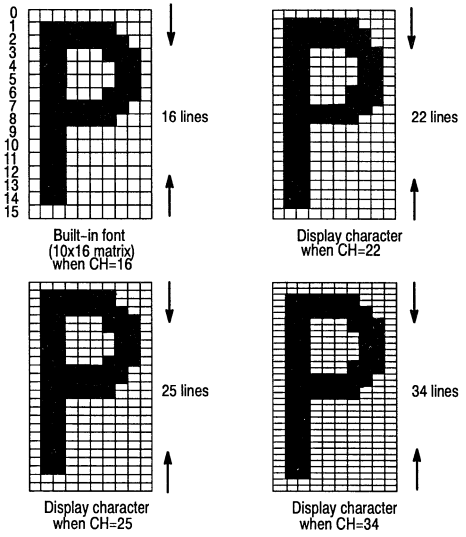


Figure 7. Variable Character Height

A program called AMOSD FONT EDITOR in IBM PC environment was written for MC141543 editing purposes. It generates a set of S–Record or Binary record for the desired display patterns to be masked onto the character ROM of the MC141543.

In order to have better character display within windows, we suggest you to place your designed character font in the center of the 10 x 16 matrix and make the spaces equally located in the four sides of the matrix. The character $00 is predefined for blank characters, the character $7F is predefined for full–filled characters, and the character $7E is a random dots pattern reserved for testing.

In order to avoid submersion of displayed symbols or characters into a background of comparable colors, a feature of

bordering which encircles all four sides, or shadowing which encircles only the right and bottom sides of an individual display character is provided. Figure 8 shows how a character is jacketed differently. To make sure that a character is bordered or shadowed correctly, at least one dot blank should be reserved on each side of the character font.

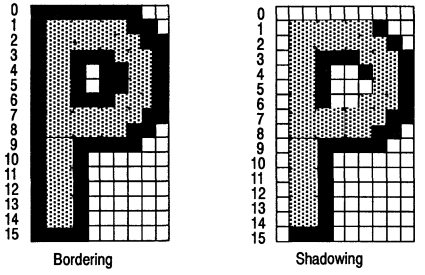


Figure 8. Character Bordering and Shadowing

Frame Format and Timing

Figure 10 illustrates the positions of all display characters on the screen relative to the leading edge of horizontal and vertical flyback signals. The shaded area indicates the area not interfered by the display characters. Notice that there are two components in the equations stated in Figure 10 for horizontal and vertical delays: fixed delays from the leading edge of $\overline{HFLB}$ and $\overline{VFLB}$ signals, regardless of the values of HORD and VERTD: (47 dots + phase detection pulse width) and one H scan line for horizontal and vertical delays, respectively; variable delays determined by the values of HORD and VERTD. Refer to Frame Control Registers COLN 9 and 10 for the definitions of VERTD and HORD. Phase detection pulse width is a function of the external charge–up resistor, which is the 470 kΩ resistor in a series with 5.6 kΩ to VCO pin in the Application Diagram. Dot frequency is determined by the equation: H Freq. x 320 if the bit X32B is clear and H Freq. x 480 if bit X32B is set to 1 and bit X64 is 0 and H Freq. x 640 if both bit X32B and bit X64 are set to 1. For example, dot frequency is 10.24 MHz if H freq is 32 KHz while bit X32B is 0. If X32B is 1 and bit X64 is 0, the dot frequency will be 15.36 MHz (one and a half of the original one). If X32B is 1 and bit X64 is also 1, the dot frequency will be 20.48 MHz (double of the original one).

When double character width is selected for a row, only the even–numbered characters will be displayed, as shown in row 2. Notice that the total number of horizontal scan lines in the display frame is variable, depending on the chosen character height of each row. Care should be taken while configuring each row character height so that the last horizontal scan line in the display frame always comes out before the leading edge of $\overline{VFLB}$ of next frame to avoid wrapping display characters of the last few rows in the current frame into the next frame. The number of display dots in a horizontal scan line is always fixed at 300, regardless of row character width and the setting of bit X32B and X64.

Although there are 30 character display registers that can be programmed for each row, not every programmed character can be shown on the screen in 320 dots resolution. Usually, only 24 characters can be shown in this resolution at most. This is induced by the retrace time that is required to retrace the H scan line. In other resolution, 480 dots and 640 dots, 30 characters can be displayed on the screen totally if the horizontal delay register is set properly.

Figure 9 illustrates the timing of all output signals as a function of window and fast blanking features. Line 3 of all three characters is used to illustrate the timing signals. The shaded area depicts the window area. Both the left hand side and right hand side characters are embodied in a window with only one difference: FBKGC bit. The middle character does not have a window as its background. Notice that signal HTONE/PWMCK is active only during window area. Timing of signal FBKG depends on the configuration of FBKGC bit. The configuration of FBKGC bits affects only FBKG signal timing; it has no effect on the timing of HTONE/PWMCK. Waveform 'R, G or B', which is the actual waveform at R, G, or B pin, is the logical OR of waveform 'character R, G or B' and waveform 'window R, G or B'. 'Character R, G, or B' and 'window R, G, or B' are internal signals for illustration purpose only. Also notice that HTONE/PWMCK has exactly the same waveform as 'window R, G or B'.

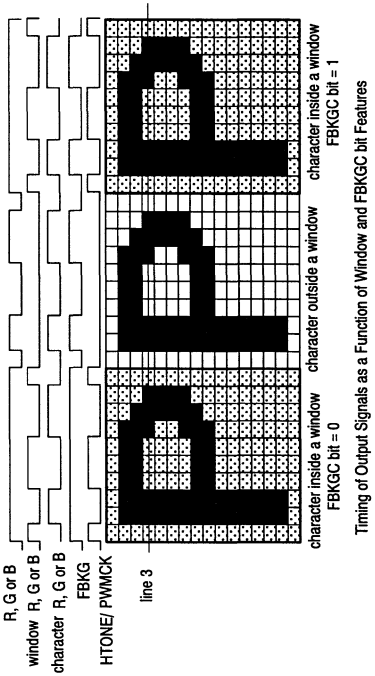


Figure 9. Timing of Output Signals

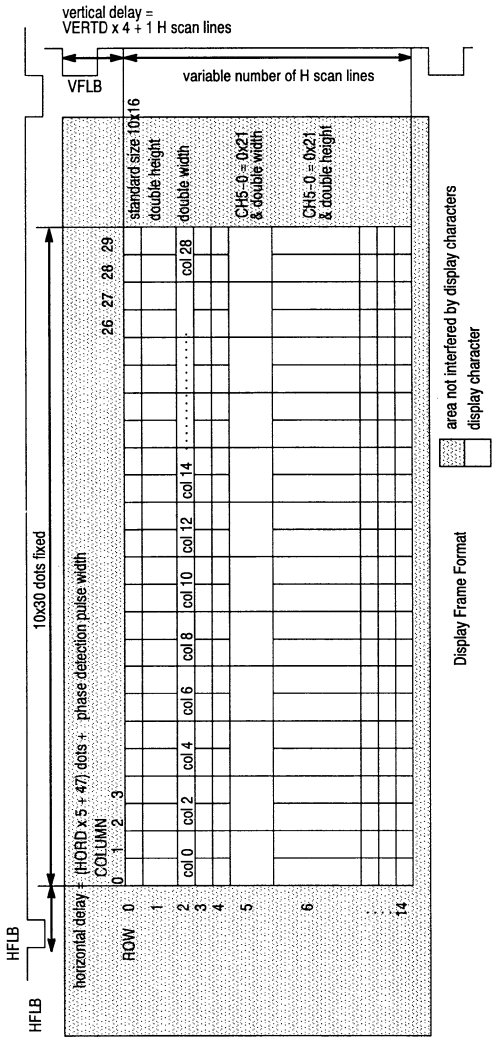


Figure 10. Display Frame Format

FONT

Icon Combination

MC141543 contains 128 character ROM. The user can create an on–screen menu based on those characters and icons. Refer to Table 3 for icon combinations. Address $00 and $7F are predefined characters and $7E is for testing. They cannot be modified in any AMOSDs.

Table 3. Combination Map

ICON	ROM ADDRESS(HEX)
Volume Bar I	01, 02, 03, 04, 05, 06, 4A
Volume Bar II	48, 49, 57
Volume Bar III	47
Size	4F, 50
Position	51, 52
Geometry	53, 54, 55, 56
Contrast	58,59
Brightness	5A, 5B
Horizontal Position	5C, 5D
Horizontal Sizing	5E, 5F
Vertical Position	60, 61
Vertical Sizing	62, 63
Pin Cushion	64, 65
Deguassing	66, 67
Video Mode	68, 69
Trapezoid	6A, 6B
Parallelogram	6C, 6D
Rotation	6E, 6F
Color Select	70, 71
Video Level	72, 73
Input Select	74, 75
Recall	76,77
Save	78, 79
Left/Right Arrows	7A, 7B
INC/DEC sign	7C, 7D
Speaker	07, 08

ROM CONTENT

Figures 11 – 14 show the ROM content of MC141543. Mask ROM is optional for custom parts.

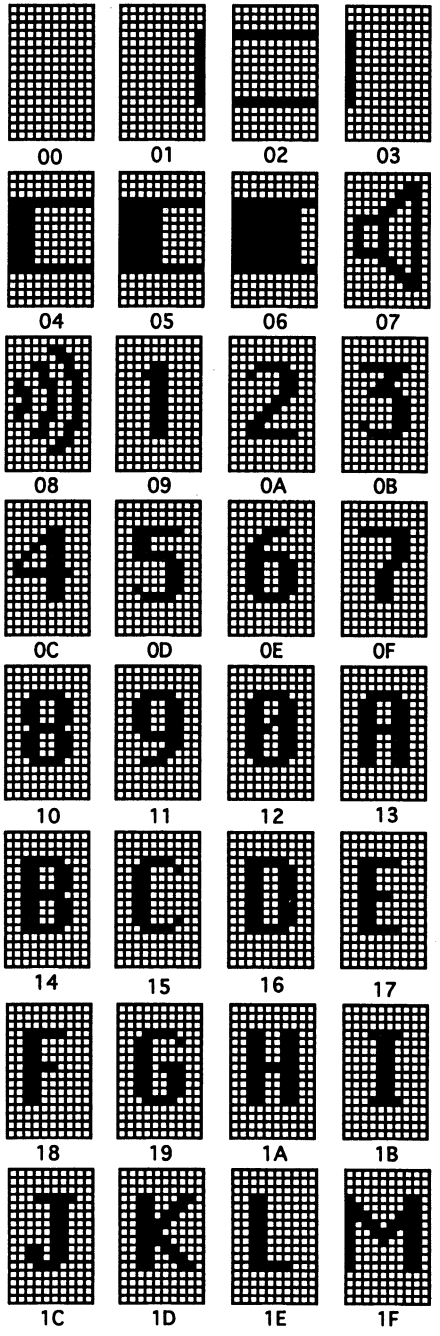


Figure 11. ROM Address ($00 – $1F)

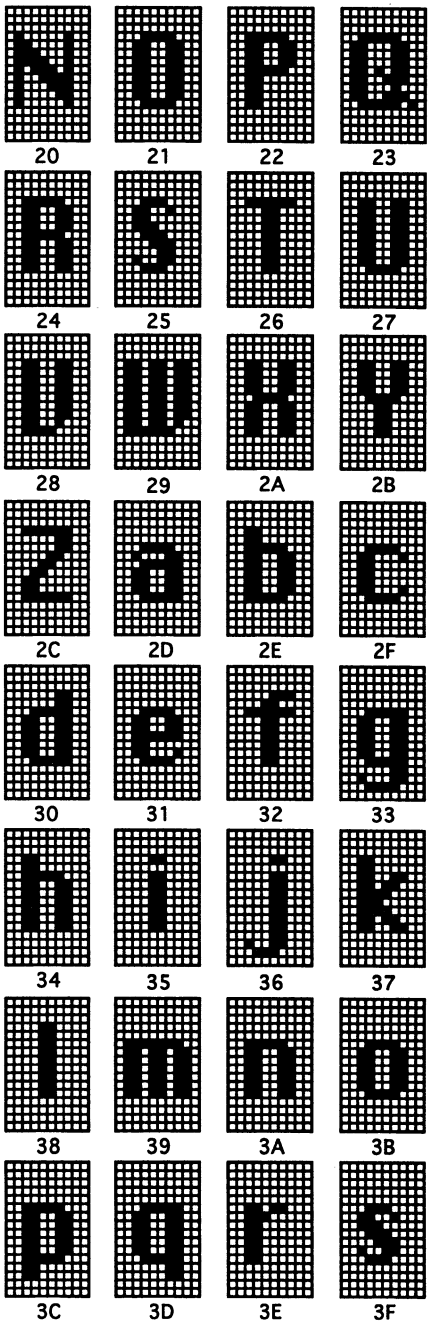


Figure 12. ROM Address ($20 – $3F)

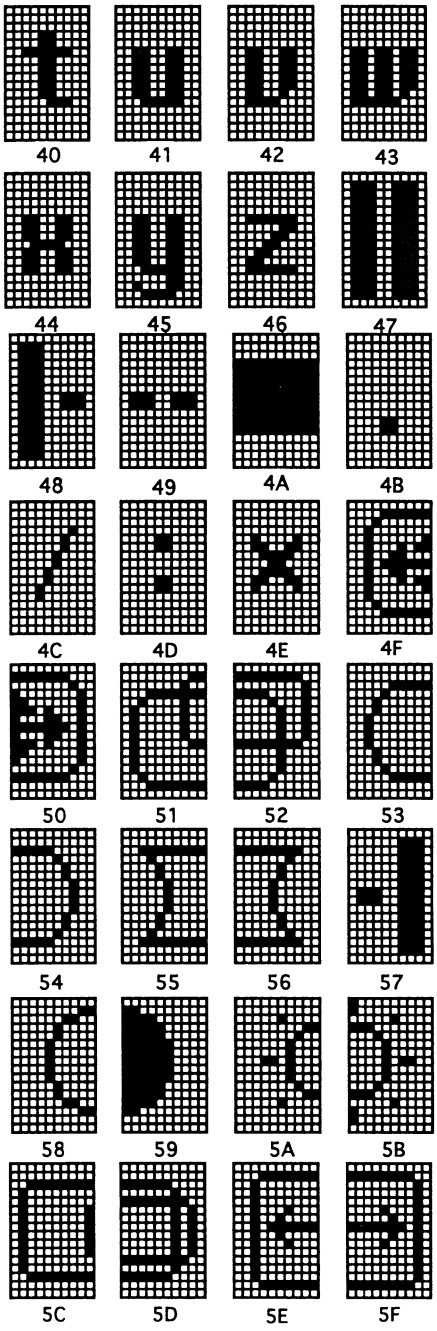


Figure 13. ROM Address ($40 – $5F)

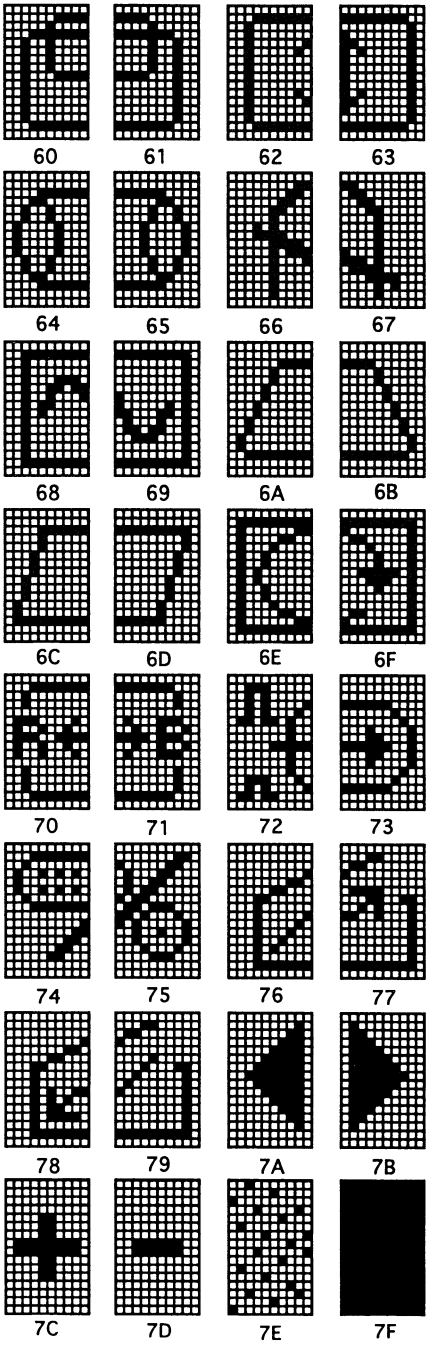


Figure 14. ROM Address ($60 – $7F)

DESIGN CONSIDERATIONS

Distortion

Motorola's MC141543P has a built–in PLL for multisystems application. Pin 2 voltage is a dc basing for the internal VCO in the PLL. When the input frequency (HFLB) in Pin 5 becomes higher, the VCO voltage will increase accordingly. The built–in PLL then has a higher locked frequency output. The frequency should be equal to 320/480/640 x HFLB (depends on resolution). It is the dot–clock in each horizontal line.

Display distortion is caused by noise in Pin 2. Positive noise makes VCO run faster than normal. The corresponding scan line will be shorter accordingly. In contrast, negative noise causes the scan line to be longer. The net result will be distortion on the display, especially on the right hand side with window turn on.

In order to have distortion–free display, the following recommendations should be considered.

- Only analog part grounds (Pin 2 to Pin 4) can be connected to Pin 1($V_{SS(A)}$). V_{SS} and other grounds should connect to PCB common ground. Then the $V_{SS(A)}$ and V_{SS} grounds should be totally separated (i.e. $V_{SS(A)}$ is floating). Refer to the Application Diagram for the ground connections.
- DC supply path for Pin 9 (V_{DD}) should be separated from other switching devices.
- LC filter should be connected between Pin 9 and Pin 4. Refer to the values used in the Application Diagram.
- Biasing and filter networks should be connected to Pin 2 and Pin 3. Refer to the recommended networks in the Application Diagram.
- Two small capacitors can be connected between Pin 2 – Pin 3 and Pin 3 – Pin 4.

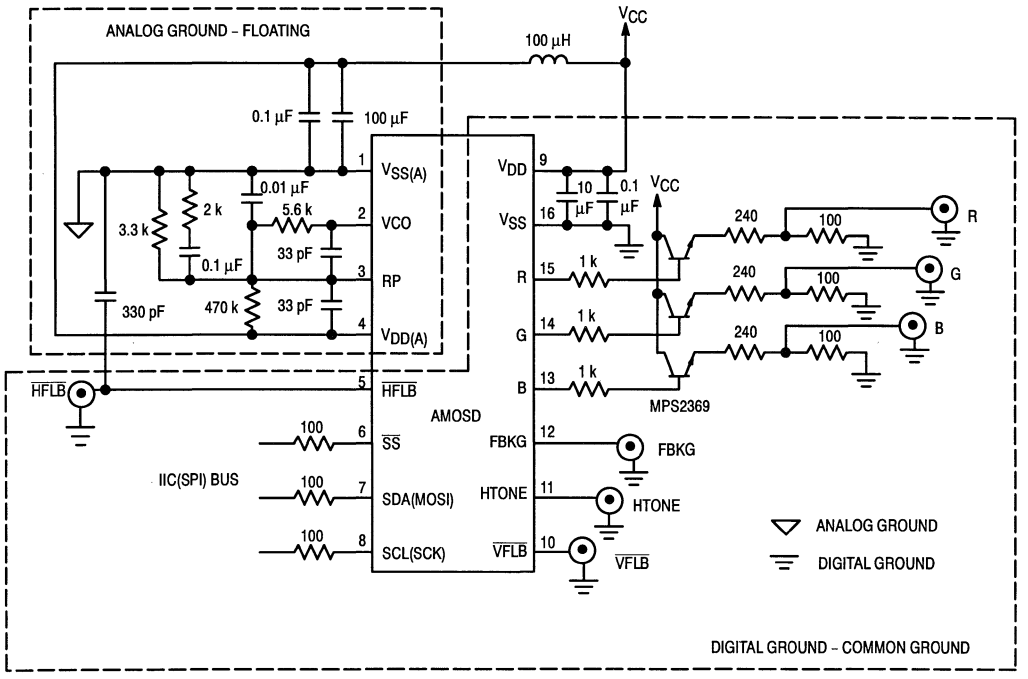
Jittering

Most display jittering is caused by HFLB jittering in Pin 5. Care must be taken if the HFLB signal comes from the flyback transformer. A short path and shielded cable are recommended for a clean signal. A small capacitor can be added between Pin 5 – Pin 1 to smooth the signal. Refer to the value used in the Application Diagram.

Display Dancing

Most display dancing is caused by interference of the serial bus. It can be avoided by adding resistors in the bus in series.

APPLICATION DIAGRAM

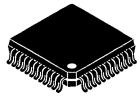


MC141620

Advance Information

Enhanced Comb Filter

CMOS



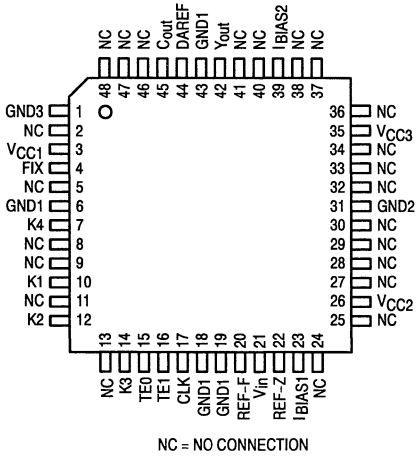
FU SUFFIX
QFP
CASE 898–01

ORDERING INFORMATION
MC141621AFU
Quad Flat Package (QFP)

The enhanced comb filter is a video signal processor for television and video recorder applications. The device separates the Luminance Y and Chrominance C from the NTSC composite video signal by using digital signal processing techniques. This filter allows an extended frequency bandwidth of the luminance signal while minimizing the common comb–filter problems such as dot–crawl and cross–color. This chip easily connects to analog TV and VCR chips due to the on–board A/D and D/A converters.

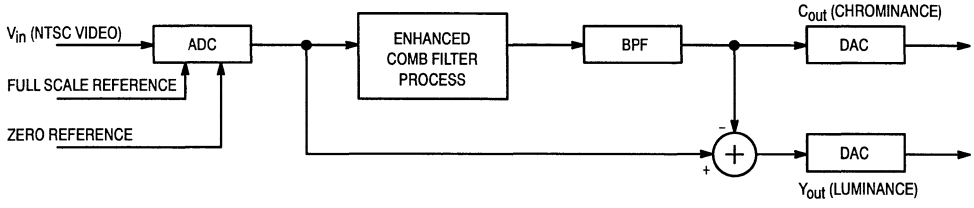
- Fast 8–Bit A/D Converter
- Two Line–Delay Memories
- Enhanced Combing Process
- Two 8–Bit D/A Converters
- Utilizes NTSC 4xfsc (sub–carrier frequency) Clock

PIN ASSIGNMENT



NC = NO CONNECTION

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Characteristic	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current (per pin)	± 20	mA
I_{out}	DC Output Current (per pin)	± 25	mA
I_{CC}	DC Supply Current (V_{CC} and GND pins)	± 100	mA
P_D	Power Dissipation	750	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

GENERAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C Unless Otherwise Noted)

Symbol	Characteristic	Min	Max	Unit
V_{CC}	Supply Voltage (V_{CC1}, V_{CC2}, V_{CC3})	4.5	5.5	V
I_{CC}	Operating Supply Current	—	75	mA
P_D	Operating Power Dissipation	—	420	mW
T_A	Ambient Operating Temperature	– 20	80	°C
t_d	Total Signal Delay	—	64.95*	µs

*Nominal value. System clock for 930.5 cycles.

ADC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Characteristic	Min	Typ*	Max	Unit
Resolution	8	—	—	Bits
Integral Nonlinearity	—	—	± 1.5	LSB
Differential Nonlinearity	—	—	± 1.0	LSB
Analog Input Level	—	—	3.0	V p–p
Full–Scale Reference Level	REF–Z	V_{CC2} – 0.4	V_{CC2} – 0.3	V
Zero Reference Level	1.4	1.6	REF–F	V
Reference Resistor Value (between REF–F and REF–Z)	—	380	600	Ω
Bias Current (Resistor = 10 kΩ)	—	120	—	µA
Input Capacitance (Design Ref. Value)	—	35	—	pF

*Data labeled "typ" is not guaranteed.

CLOCK INPUT ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Characteristic	Min	Max	Unit
Clock Frequency (Note 1)	12	15	MHz
Clock Jitter	—	2.0	ns
Input Level (Figure 8)	0.20	5.0	V p–p

Note 1 — This signal is usually 14.31818 MHz

FILTERING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Characteristic	Min	Max	Unit
Y/C Separation (clock jitter < 2.0 ns)	—	40*	dB

*Typical value. Not guaranteed.

DAC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Characteristic	Min	Max	Unit
Resolution	8	—	Bits
Output Bandwidth (at –3.0 dB)	5.5	—	MHz
Integral Nonlinearity	—	± 1.0	LSB
Differential Nonlinearity	—	± 0.3	LSB
Differential Gain	—	5.0	%
Differential Phase	—	5.0	Deg
Analog Output Voltage, Y_{out}	1.1	1.3	V p–p
Analog Output Voltage, C_{out}	1.1	1.3	V p–p
Full Scale Voltage, Y_{out}	1.3	1.7	V
Full Scale Voltage, C_{out}	1.3	1.7	V
Zero Scale Voltage, Y_{out}	0.1	0.5	V
Zero Scale Voltage, C_{out}	0.1	0.5	V
Bias Current [DAC only] — Resistor = 10 kΩ	120*	—	µA
Output Impedance	—	300	Ω

*Typical value. Not guaranteed.

DIGITAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Symbol	Characteristic	Min	Max	Unit
V_{IH}	High Level Input Voltage (K1 – K4, FIX)	3.15	—	V
V_{IL}	Low Level Input Voltage (K1 – K4, FIX)	—	1.1	V
I_{IH}	High Level Input Current (K1 – K4, FIX)	—	0.1	µA
I_{IL}	Low Level Input Current (K1 – K4, FIX)	—	0.1	µA

PIN DESCRIPTIONS

V_{CC1} (Pin 3)
+ 5.0 V ± 10% dc power supply for the digital circuits.

V_{CC2} (Pin 26)
+ 5.0 V ± 10% dc power supply for the ADC.

V_{CC3} (Pin 35)
+ 5.0 V ± 10% dc power supply for the DAC.

GND1 (Pins 6, 18, 19, 43)
Ground for the digital circuits. For optimum performance, all pins must be tied to ground.

GND2 (Pin 31)
Ground for the ADC.

GND3 (Pin 1)
Ground for the DAC.

CLK (Pin 17)
4xfsc (sub–carrier frequency) 14.31818 MHz input. This signal is usually ac–coupled through an external capacitance. See User Information. The clock signal must synchronize with the NTSC video signal.

V_{in} (Pin 21)
Composite video signal input. The composite video signal, clamped externally, should be supplied with dc coupling. The video input level should be nominally 3.0 V p–p. Input signal bandwidth should be limited to less than 1/2 of the frequency of the sampling clock by anti–aliasing filtering, etc.

REF–F (Pin 20)
ADC reference for the full–scale voltage.

REF–Z (Pin 22)
ADC reference for the zero input voltage.

DAREF (Pin 44)
Reference for the luminance and chrominance DACs. Insert a capacitor of 0.1 μF between DAREF and GND3.

I_{BIAS1} (Pin 23)
ADC bias circuit current control. Insert a resistor of 10 kΩ between I_{BIAS1} and GND2.

I_{BIAS2} (Pin 39)
DAC bias circuit current control. Insert a resistor of 10 kΩ between I_{BIAS2} and GND3.

Y_{out} (Pin 42)
Luminance output. This output signal is fed into the general analog VCR/TV system. Typical output voltage is 1.2 V p–p swinging from 0.3 V to 1.5 V.

C_{out} (Pin 45)
Chrominance output. This output signal is fed into the general analog VCR/TV system. Typical output voltage is 1.2 V p–p swinging from 0.3 V to 1.5 V.

TE0 (Pin 15)
Test enable pin. If this pin is a high level, the test mode is enabled. This pin must be grounded by the user.

TE1 (Pin 16)
Test select pin. This pin must be grounded by the user.

FIX (Pin 4)
Filter mode select pin. It must be a high level for the normal mode. Comb filter/bandpass filter fixed mode can be selected by the K1 pin. Each mode is shown below.

FIX	K1	MODE
H18	H	Normal mode
H	L	Normal mode
L	H	Bandpass filter fixed mode
L	L	Comb filter fixed mode

K1, K2, K3, and K4 (Pins 10, 12, 14, 7)
K factor inputs. These pins are provided to set up the K value for the select control circuit, and to set up the threshold level of comb filter and bandpass filter. Each input (K1 – K4) are assigned to b1 – b4 of the K factor. Input must be at CMOS levels. The assignment of K pins are shown below. Also, when the FIX pin is at a low level, the K1 pin becomes a filter mode select pin. If the K1 pin is low, the comb filter is enabled; otherwise, the bandpass filter is enabled.

b0	b1	b2	b3	b4	b5	b6	b7
L	K1	K2	K3	K4	H	H	L

The enhanced comb filter is a high performance HCMOS digital filter combined with A/D and D/A converters. The basic functions of this chip are the separation of the luminance Y and chrominance C signals from the NTSC video signal which is composed of luminance and chrominance components interleaved with each other in the same frequency band.

The visual performance advantages of the enhanced comb filter are that the chip eliminates the sub–carrier dot–crawl from the luminance channel in large color areas and eliminates the cross color from the chrominance in high frequency luminance areas. Also, the horizontal resolution of the picture is allowed from zero to an arbitrary high by this chip. The Y/C separation is performed by a combination of a digital 2H comb filter and a digital bandpass filter.

To perform the enhanced combing process, two horizontal scan line delay memories for a 2H comb filter, several pairs of latches for a bandpass filter, and selective control circuitry are provided. The 2H comb filter separates the chrominance components from the composite video signal by integration of 3 successive lines. However, when the comb filter is performing the line integration, the horizontal color smears on the boundary. This chip solves the color smear and dot–crawl problems while keeping the advantages of 2H comb filter by selecting one filter process from the bandpass filter or the 2H comb filter at a particular picture transition.

Enhanced Comb Filter Description

The first page of the datasheet shows the block diagram of the enhanced comb filter chip. There are three major functions on this block diagram.

The first is the analog–to–digital conversion block. One 8–bit binary A/D converter is provided for digitizing the incoming analog video signal to 8–bit binary data. The conversion frequency is 14.3 MHz which is four times the color sub–carrier frequency. The analog video input is nominally 3.0 V p–p.

The second is the digital filters and selective control block. There are two digital filters on this block which are vertical filter (2H comb filter) and horizontal filter (bandpass filter). The selective control determines which type of filter should be chosen for the current process.

The third is the digital–to–analog conversion block. Two 8–bit D/A converters are provided for the luminance and chrominance analog output. The conversion frequency is four times the sub–carrier signal (14.3 MHz). The chrominance analog output has a dc offset bias of half the maximum output voltage.

Algorithm of Enhanced Comb Filter

Figure 1 illustrates the basic principles of the Y/C separation algorithm. The NTSC video signal has an alternate relationship in the horizontal and vertical direction on the sampled data array. V1 through V9 in Figure 2 represent a sampled data array of an appropriate area of the screen. The sampling frequency is four times the sub–carrier frequency (14.3 MHz). There are four data samples in one sub–carrier cycle, and the sub–carrier phase is reversed every scan line. In other words, V1 and V7 have same phase and V4 is reversed; V2 and V8 have same phase and V5 is reversed. Also, the sampled data V1 through V3 are placed on scan line N, V4 through V6 are on N–1, and so on. On the individual lines, every four data samples have the same phase — for instance, V1 and V3, V4 and V6, and so forth.

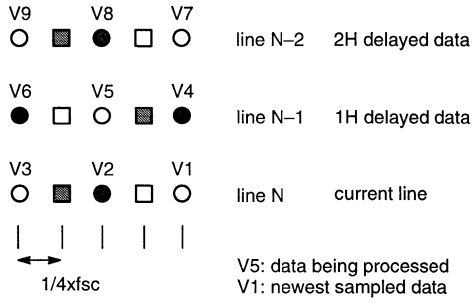


Figure 1.

Vertical Filtering

The typical vertical filter is a comb filter which may use 1H or 2H scan line delay. The comb filter integrates successive scan line data to separate Y and C. The formula is:

Chrominance = (V5 – (V2 + V8) / 2) / 2 x H_{BPF}

Luminance = V5 – Chrominance

Where H_{BPF} is the BPF transfer function.

The combing process allows the luminance signal separation for the extension of the frequency bandwidth. However, the integration of the successive lines causes a loss of vertical resolution. The combing process causes color smears on the line, if there is color transition between the lines. It can be observed as color smear on the color boundary or horizontal running dot–crawl.

Horizontal Filtering

The conventional filtering, such as a bandpass filter, has typical dot–crawl and cross–color problems. Even the digital horizontal filtering has similar problems. However, the MC141620's digital horizontal filtering yields superior performance over a regular bandpass filter. The formula is:

Chrominance = (V5 – (V4 + V6) / 2) / 2 x H_{BPF}

Luminance = V5 – Chrominance

Where H_{BPF} is the BPF transfer function.

Enhanced Comb Filtering (Combination of Vertical and Horizontal Filtering)

This is a combination approach of the vertical filtering and horizontal filtering so that the overall filtering can take advantage of both filters. The algorithm of this filter is as follows:

If |V8 – V2| + K ≤ |V6 – V4|

(Vertical Transition ≤ Horizontal Transition)

K: constant value

then Chrominance = (V5 – (V2 + V8) / 2) / 2x HBPF

– Vertical Filter

If |V8 – V2| + K > |V6 – V4|

(Vertical Transition > Horizontal Transition)

then Chrominance = (V5 – (V6 + V4) / 2) / 2x HBPF

Luminance = V5 – Chrominance – Horizontal Filter

This algorithm determines the amount of Y/C separation according to the result of comparison between the value change V2 to V8 and V4 to V6. Measurement of this data array allows minimization of the problems caused by horizontal and vertical filtering, such as dot–crawl or color smear. Also, it can give a weight to select a filter, vertical or horizontal, according to the K factor set up.

OPERATIONAL DESCRIPTION

A/D Converter

The clamped external composite–video signal is converted to 8–bit binary code by this fast A/D converter. The input video voltage is expected to be 3.0 V p–p nominal. The sampling clock frequency is 14.3 MHz which is four times the color sub–carrier signal.

Comb Filter Function

The comb filter consists of a delay–line memory, absolute value function, latches, and 8–bit adders. The basic functions of the filtering are additions and subtractions by the adders. The calculations for each sampled data are expected to be completed within one clock cycle, about 70 ns. Each adder has latches to hold the value calculated. If the speed of the adders is not fast enough, other latches may be inserted into the adders to save the partial value of the calculations. These latches are counted as the digital process delay of the filter. There are two major data passes in this filter: chrominance and luminance. Both data passes are designed such that all delays match when they output.

Vertical Filter

The basic structure of this filter is a 2H line–delay comb filter. The simplified functional block diagram is shown in Figure 2. Two 1H scan delay lines are provided for vertical filtering. Video memory structure can be used for the line delay component. The cycle time of this memory has to be less than 70 ns, and total delay time is 1 scan line time for each.

Horizontal Filter

The other basic function of this filter is called horizontal filtering which has the same function as a bandpass filter. The horizontal filter consists of a 4th order FIR filter which has a bandpass characteristic. Figure 3 shows the simplified functional block diagram of the horizontal filter.

Selective Control

The selective control checks the horizontal transition and vertical transition of the picture in order to select a filtering method that minimizes the dot–crawl, cross color, and color smear. The major filtering algorithm of the chip is performed in this block.

Horizontal transition = $|V6 - V4|$

Vertical transition = $|V8 - V2|$

The difference of the transition = $|V8 - V2| - |V6 - V4| + K$

If $|V8 - V2| - |V6 - V4| + K > 0$ then Horizontal Filter

If $|V8 - V2| - |V6 - V4| + K \leq 0$ then Vertical Filter

K factor

Selective control switches the filtering modes by the transit difference of horizontal and vertical direction. K factor assignment is shown below. If K1 through K4 are all low, a weighting factor is given to the comb filter side. If all are a high level, it gives a weighting factor of 50% comb and bandpass side. The recommended level is b1 = L, b2 through b4 = H.

b0	b1	b2	b3	b4	b5	b6	b7
L	K1	K2	K3	K4	H	H	L

b0, b5, b6, b7 are fixed.

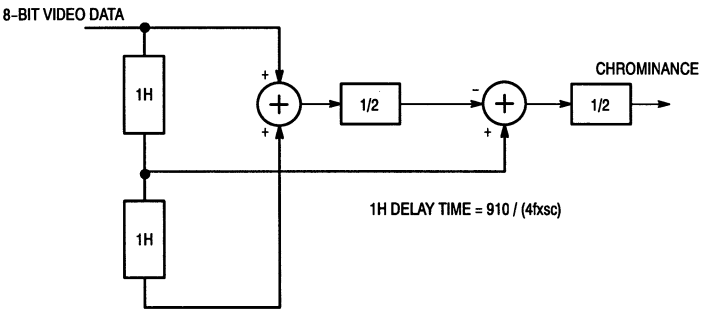


Figure 2. Vertical Filter

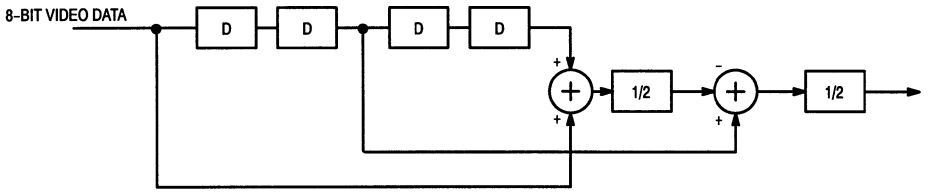


Figure 3. Horizontal Filter

Bandpass Filter (BPF)

This filter has the same functions as the horizontal filter. The bandpass filter reduces low and high frequency components in the chrominance signal.

Video Input Signal

The recommended video input signal for the comb filter is shown in Figure 4. The nominal video input is 3.0 V p–p.

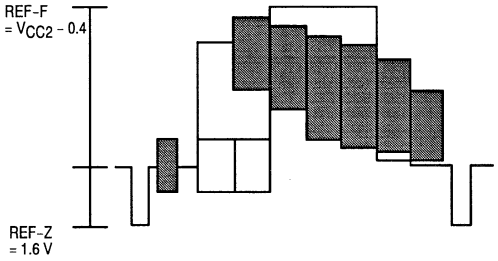


Figure 4. Input Video Signal

USER INFORMATION

V_{CC}, GND

Each of the V_{CC}/GND–pin pairs should be connected to separate power supplies in order to reduce noise problems. All V_{CC} pins should be bypassed through 0.1 μF ceramic and 47 μF tantalum capacitors mounted as close as possible to the MC141620.

V_{in}

The video input signal must be clamped with an appropriate voltage level. It might be necessary to amplify the signal to drive this chip. In order to reduce noise effects, the wiring pattern on the V_{in} signal should be short as possible. V_{in} should be driven with a low–impedance source. The frequency bandwidth of the input signal should be limited to less than half of the sampling clock frequency (Nyquist criteria).

AD Reference Inputs

REF–F and REF–Z set the dynamic range of the ADC input. These should be by passed through 0.1 μF ceramic and 10 μF tantalum capacitors mounted close to GND2. The voltage supplied to REF–F and REF–Z must be stable within allowable time and temperature ranges.

Reference accuracy is ± 0.5 LSB (voltage difference between REF–F and REF–Z), if all portions of circuit are not changed in compliance with temperature. But, most circuits are changed in compliance with the temperature. Therefore, in this case, the reference voltage accuracy should be less than ± 0.5 LSB. A stable power supply is required for these reference inputs and the resistor value of the reference ladder is low (typically about 300 Ω).

Clock Input

Reference Figures 5, 6 and 7.

Clock (14.31818 MHz) must be synchronized with a sub–carrier (NTSC) or horizontal sync signal. The clock line should be a short printed circuit board trace, and should be separated from other circuits in order to reduce crosstalk. TTL or CMOS levels may be connected by dc coupling. 5.0 V p–p sine waves may be ac coupled with a 0.1 μF ceramic capacitor.

A small signal, such as a 200 mV p–p or greater sine wave, may be ac coupled with a 0.1 μF ceramic capacitor, then biased to half of V_{CC1} by a pair of 330 kΩ resistors.

When the clock level is less than 200 mV p–p, it should be supplied to the circuit of Figure 7 after being increased to more than 200 mV p–p using a buffer amplifier.

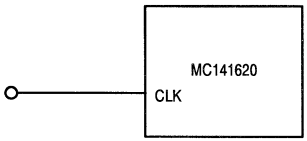


Figure 5. TTL Level

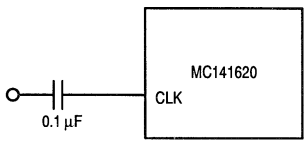


Figure 6. 5.0 V p–p Sine Wave

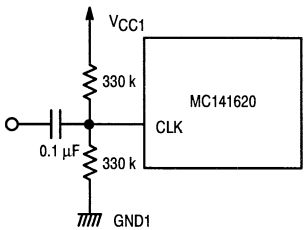


Figure 7. 200 mV p–p to 5.0 V p–p Sine Wave

I_{BIAS} Pins

The I_{BIAS} pins determine the bias current of the ADC and DAC by external resistors. I_{BIAS1} is associated with the ADC and I_{BIAS2} is for the DAC. In both cases, a 10 kΩ resistor is connected from each of these pins to the closest GND.

DA Reference

This is a bypass pin for the DA reference. Insert a bypass capacitor of about 0.1 μF between DAREF and GND3.

Power–On Sequence

The GND1, GND2, and GND3 pins are connected to a common ground. Power should be supplied sequentially to V_{CC1}, V_{CC2}, then V_{CC3}.

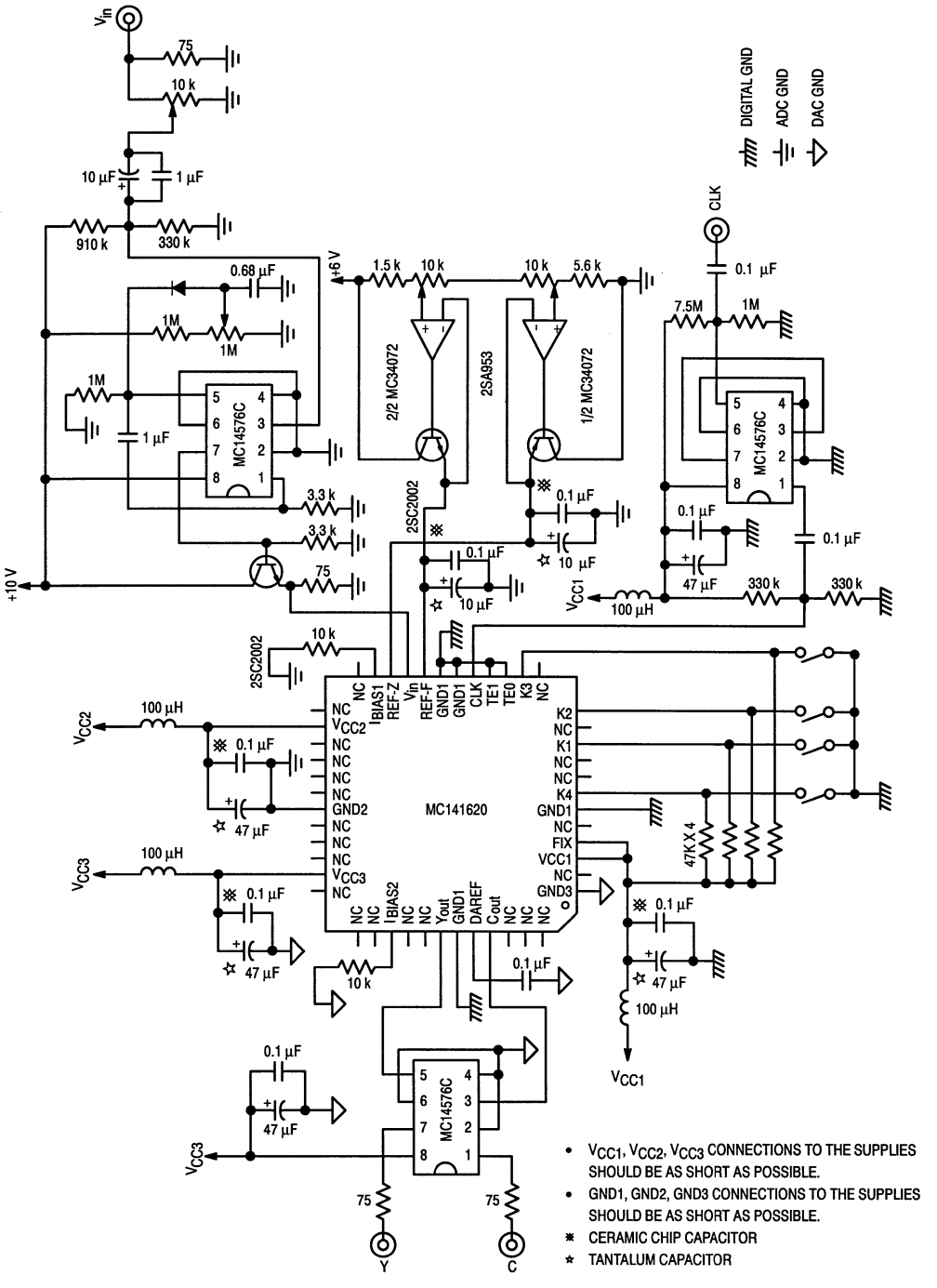


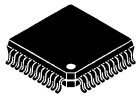
Figure 8. Application Circuit

MC141621A

Advance Information

Advanced Comb Filter (ACF)

CMOS



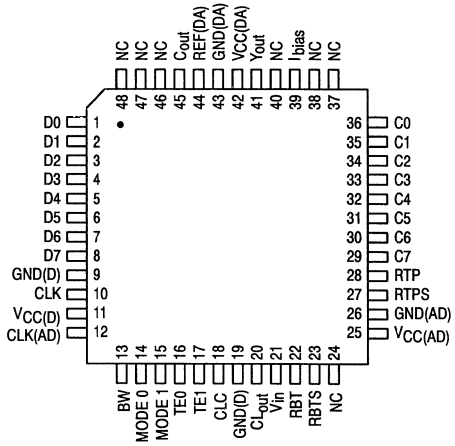
FU SUFFIX
QFP PACKAGE
CASE 898–01

ORDERING INFORMATION
MC141621AFU
Quad Flat Package (QFP)

The Advanced Comb Filter is a video signal processor for VCRs and TVs. It separates the Luminance Y and Chrominance C signals from the NTSC composite video signal by using digital signal processing techniques which minimize dot–crawl and cross–color. This filter allows a video signal input of an extended frequency bandwidth by using a 4xfsc clock. The built–in A/D and D/A converters allow easy connections to analog video cassette recorders and television circuits.

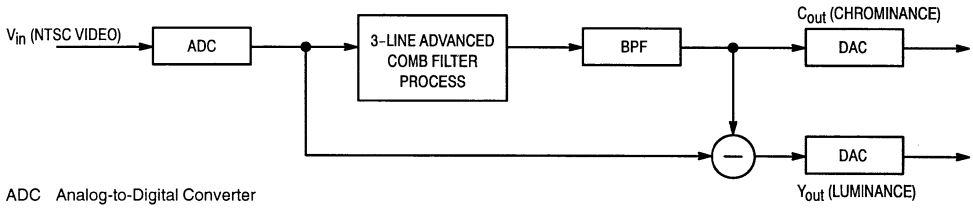
- Built–In High Speed 8–Bit A/D Converter
- Two Line Memories (18209 bytes)
- Advanced Combing Process
- Two 8–Bit D/A Converters
- Built–In Clamp Circuit
- On–Chip Reference Voltage Regulator for A/D Converter
- Digital Interface Mode

PIN ASSIGNMENT



NC = NO CONNECTION

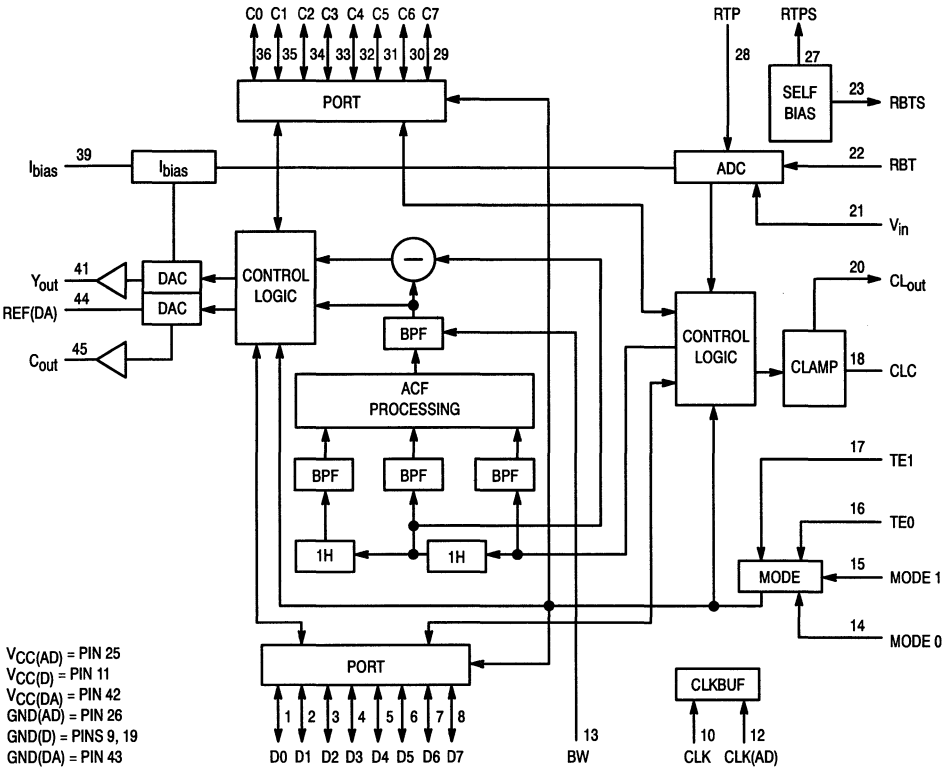
SIMPLIFIED BLOCK DIAGRAM



ADC Analog-to-Digital Converter
BPF Band-Pass Filter
DAC Digital-to-Analog Converter

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Value	Unit
DC Supply Voltage (Referenced to GND), $V_{CC(AD)}$, $V_{CC(D)}$, $V_{CC(DA)}$	V_{CC}	– 0.5 to + 7.0	V
DC Input Voltage (Referenced to GND)	V_{in}	– 1.5 to V_{CC} + 1.5	V
DC Output Voltage (Referenced to GND)	V_{out}	– 0.5 to V_{CC} + 0.5	V
DC Input Current (per pin)	I_{in}	± 20	mA
DC Output Current (per pin)	I_{out}	± 25	mA
DC Supply Current (V_{CC} and GND pins)	I_{CC}	± 100	mA
Power Dissipation	P_D	750	mW
Storage Temperature	T_{stg}	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

2

GENERAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C Unless Otherwise Noted)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage ($V_{CC(AD)}$, $V_{CC(D)}$, $V_{CC(DA)}$)	V_{CC}	4.5	5.0	5.5	V	
Operating Supply Current	I_{CC}	—	80	110	mA	
Operating Power Dissipation	P_D	—	400	600	mW	
Ambient Operating Temperature	T_A	– 20	—	80	°C	
Total Signal Delay (between V_{in} – Y_{out} and C_{out} excluding the digital input comb filter mode)	t_d	—	64.95	—	µs	1

NOTE:
1. System clock for 930 cycles.

CLOCK INPUT ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic		Symbol	Min	Typ	Max	Unit	Notes
Clock Frequency		f_c	12	14.31818	15	MHz	
Input Level Clock		V_c	200	—	—	mV p-p	1
High Level Input Voltage	CLK, CLK(AD)	V_{IH}	3.15	—	—	V	2, 3
Low Level Input Voltage	CLK, CLK(AD)	V_{IL}	—	—	1.1	V	2, 3
Clock Duty Cycle	CLK, CLK(AD)	DC	40	50	60	%	2, 3

NOTES:
1. In normal and CCF modes.
2. CLK in digital input comb filtering and digital output comb filtering mode.
3. CLK(AD) is available only during digital input comb filtering mode.

ADC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	—	—	—	8	Bits
Integral Nonlinearity (Using Internal Reference)	INL	—	± 0.5	± 1.5	LSB
Differential Nonlinearity (Using Internal Reference)	DNL	—	± 0.5	± 1.0	LSB
Analog Input Range	V_{in}	—	—	3.3	V p–p
Top Reference Level	V_{TP}	V_{BT}	—	$V_{CC(AD)}$	V
Bottom Reference Level	V_{BT}	1.4	—	V_{TP}	V
Top Self Reference Level (When Connecting RTP – RTPS, RBT – RBTS)	V_{TPS}	4.5	4.6	4.7	V
Bottom Self Reference Level (When Connecting RTP – RTPS, RBT – RBTS)	V_{BTS}	1.5	1.6	1.7	V
Maximum Analog Input Range During Self Reference (When Connecting RTP – RTPS, RBT – RBTS)	V_{ins}	2.9	3.0	3.1	V p–p
Reference Resistor Value	R_{ref}	—	350	—	Ω

DIGITAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic		Symbol	Min	Typ	Max	Unit
High Level Input Voltage	MODE 0, MODE 1, BW, C0 – C7, D0 – D7	V_{IH}	3.15	—	—	V
Low Level Input Voltage	MODE 0, MODE 1, BW, C0 – C7, D0 – D7	V_{IL}	—	—	1.1	V
Input Leakage Current (V_{in} = $V_{CC(D)}$ or GND(D))	MODE 0, MODE 1, BW, C0 – C7, D0 – D7	I_{lkg}	—	—	± 10	μA
Data Setup Time (During CLK Input, CMOS Level)	C0 – C7, D0 – D7	t_{su}	5	—	—	ns
Data Hold Time (During CLK Input, CMOS Level)	C0 – C7, D0 – D7	t_h	30	—	—	ns
Data Input Rise Time (During CLK Input, CMOS Level)	C0 – C7, D0 – D7	t_r	—	—	10	ns
Data Input Fall Time (During CLK Input, CMOS Level)	C0 – C7, D0 – D7	t_f	—	—	10	ns
Output Data Delay (During CLK Input, CMOS Level)	C0 – C7, D0 – D7	t_d	—	30	—	ns

FILTERING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Y/C Separation	—	40	—	—	dB
Band–Pass Filter (Wide Bandwidth, at – 3 dB)	—	—	± 1.3	—	MHz
Band–Pass Filter (Narrow Bandwidth, at – 3 dB)	—	—	± 1.1	—	MHz

DAC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	—	—	—	8	Bits
Integral Nonlinearity	INL	—	—	± 1	LSB
Differential Nonlinearity	DNL	—	—	± 0.3	LSB
Analog Output Voltage, Y_{out}	V_{YO}	1.1	1.2	1.3	V p–p
Analog Output Voltage, C_{out}	V_{CO}	1.1	1.2	1.3	V p–p
Full Scale Voltage, Y_{out}	V_{YFS}	1.3	1.5	1.7	V
Full Scale Voltage, C_{out}	V_{CFS}	1.3	1.5	1.7	V
Zero Scale Voltage, Y_{out}	V_{YZS}	0.1	0.3	0.5	V
Zero Scale Voltage, C_{out}	V_{CZS}	0.1	0.3	0.5	V
Output Impedance	Z_O	—	100	300	Ω

ADC – DAC GENERAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Voltage Gain (During Self Bias)	—	– 8.9	– 8.0	– 7.1	dB
Output Bandwidth (at – 3 dB)	—	5.5	6.4	—	MHz
Differential Gain	DG	—	—	5	%
Differential Phase	DP	—	—	5	Deg
Bias Current (I_{bias} resistor = 9.1 kΩ)	I_{bias}	—	135	—	μA

CLAMP CIRCUIT CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Clamp Mode Output Saturation Voltage, CL_{out}	V_{clys}	2.8	3.1	—	V
Bias Mode Output Voltage, CL_{out} (at Self Reference)	V_{CLC}	2.95	3.05	3.15	V

NOTE:

Clamp Mode Output Voltage, V_{cly} (Non–input when connecting V_{in} – CL_{out})

$$V_{cly} = (V_{TP} - V_{BT}) (N + 1) / 256 + V_{BT} \pm 50 \text{ mV}$$

where N: Clamp Code Input (N < 255)

- If the calculated value of the output voltage, $V_{clys} > 3$, then $V_{cly} = 3.0$ V
- Clamp Value N is fixed during the digital input comb filtering mode and the digital output comb filtering mode, fixing N = 8.

Bias Mode Output Voltage, V_{CLC} (Non–input when connecting V_{in} – CL_{out})

$$V_{CLC} = (V_{TP} - V_{BT}) / 2 + V_{BT} \pm 10\%$$

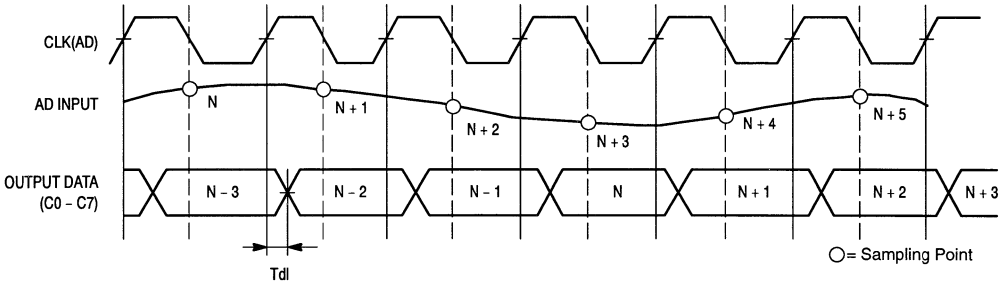


Figure 1a. A/D Converter Timing Diagram (During Digital Input Comb Filtering Mode)

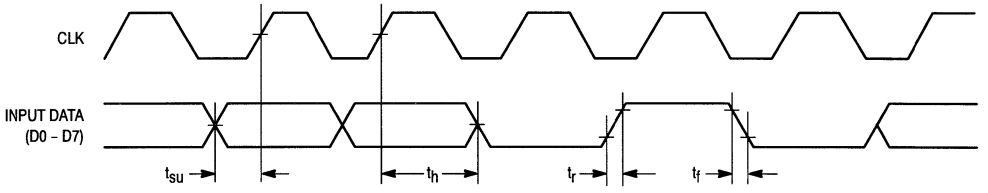


Figure 1b. Digital Signal Input Timing Diagram (During Digital Input Comb Filtering Mode)

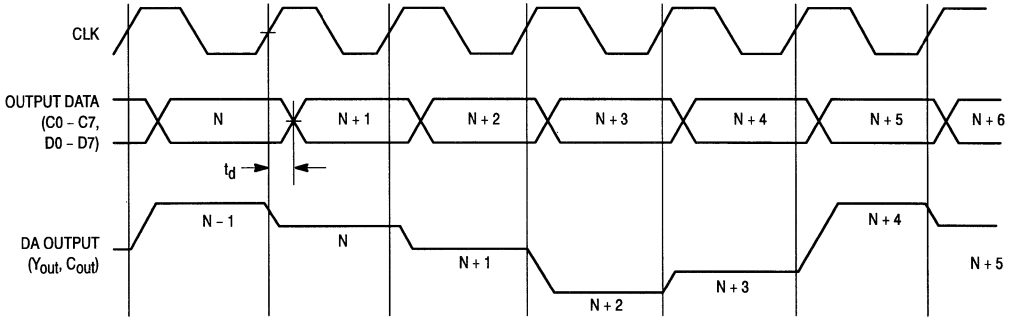


Figure 1c. Output Signal Timing Diagram (During Digital Output Comb Filtering Mode)

Figure 1. Timing Diagrams

PIN DESCRIPTIONS

Pin	Pin Name	Function
1 to 8	D0 – D7	Digital input/output interface 2. Generally GND level.
9, 19	GND(D)	GND for Digital circuit.
10	CLK	CLK input. Input ac coupling by external capacitor. Minimum CLK input level is 200 mV p–p during normal and CCF modes.
11	$V_{CC(D)}$	Power supply for Digital circuit.
12	CLK(AD)	CLK input for A/D converter. Available only during Digital input comb filtering mode and a portion of test mode. Input level is CMOS level.
13	BW	Chrominance signal bandwidth selecting input. Narrow bandwidth in LOW level.
14, 15	MODE 0,1	MODE input. GND level during Normal mode.
16, 17	TE0, TE1	Test mode input. Generally GND level.
18	CLC	Clamp time constant setting pin.
20	CL_{out}	Voltage output for clamp. It can clamp an input signal by connecting with V_{in} and inputting the video signal by ac coupling.
21	V_{in}	AD converter input. Maximum input voltage is 3.3 V p–p.
22	RBT	Bottom reference input for A/D converter.
23	RBTS	Bottom reference voltage supply pin for A/D converter. Supplies bottom reference voltage by connecting with RBT.
24	NC	No connection. Generally GND level.
25	$V_{CC(AD)}$	Power supply for A/D converter.
26	GND(AD)	GND for A/D converter.
27	RTPS	Top reference voltage supply pin for A/D converter. Supplies top reference voltage by connecting with RTP.
28	RTP	Top reference input for A/D converter.
29 to 36	C7 – C0	Clamp level input. Digital input/output interface.
37, 38	NC	No connection. Generally GND level.
39	I_{bias}	Bias circuit current control for A/D, D/A converters. Generally connected to GND(DA) through an external resistor.
40	NC	No connection. Generally GND level.
41	Y_{out}	Luminance signal output.
42	$V_{CC(DA)}$	Power supply for D/A converter.
43	GND(DA)	GND for D/A converter.
44	REF(DA)	Reference for D/A converter. Generally connected to GND(DA) through a multilayer ceramic capacitor (0.1 μF).
45	C_{out}	Chrominance signal output.
46 to 48	NC	No connection. Generally GND level.

Figure 2 shows the I/O signals of the Advanced Comb Filter.

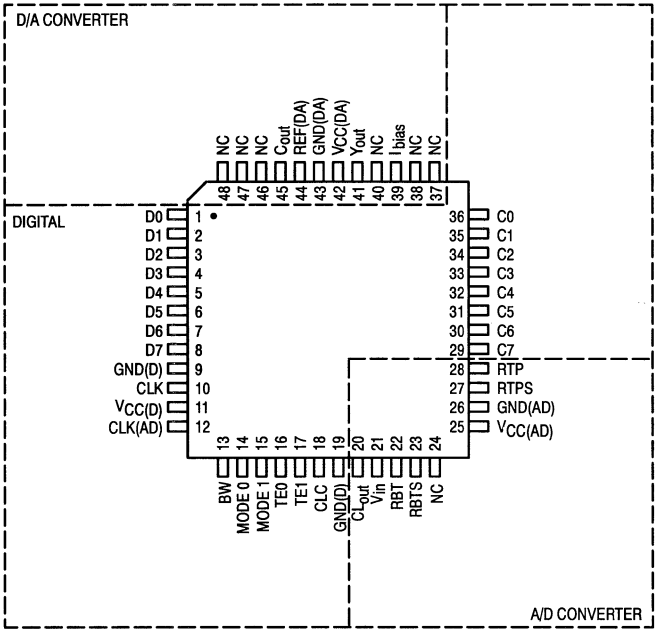


Figure 2. Pin Assignment

DEVICE DESCRIPTION

INTRODUCTION

The Advanced Comb Filter (ACF) is a high–performance HCMOS digital filter with built–in A/D and D/A converters. The basic function of the chip is the separation of the Luminance Y and Chrominance C signals from the NTSC composite video signal. The ACF minimizes the problems often generated by Y/C separation such as dot–crawl and cross–color. It uses a 14.3 MHz clock that allows an extended frequency bandwidth video signal to be input. This Y/C separation is realized by the digital advanced comb filters. The complete block diagram for the Advanced Comb Filter is shown on the first page.

ADVANCED COMB FILTER DESCRIPTION

Figure 3 is the simplified block diagram of the Advanced Comb Filter chip. There are three major functions represented on this block diagram. The first block is the analog–to–digital conversion block. The high speed 8–bit binary A/D converter converts the incoming analog video signal to an 8–bit binary data stream. The conversion frequency is 14.3 MHz, which is four times the color subcarrier frequency. The maximum analog video input is 3.3 V p–p.

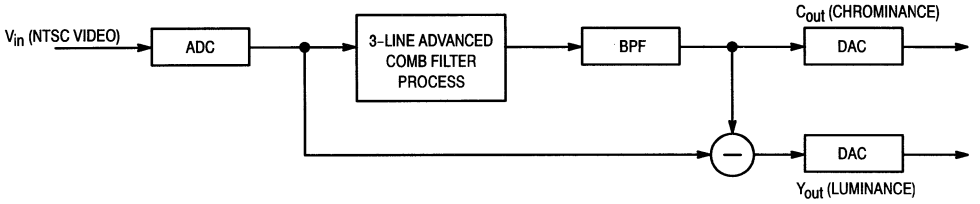


Figure 3. Simplified Block Diagram

The second block contains the Advanced Comb Filter algorithm. The digital data from the A/D converter is processed by the algorithm of the Advanced Comb Filter. The composite video is filtered by the band–pass filter (BPF) and separated into the Luminance Y and Chrominance C signals.

The third block is the digital–to–analog conversion block. Two 8–bit D/A converters convert the luminance and chrominance into analog outputs. The conversion frequency is four times the subcarrier signal (14.3 MHz). The chrominance analog output is biased with a dc offset of half the value of the D/A converter reference.

A voltage reference for clamping is built into the chip. It produces a clamp voltage by comparing the output code of the A/D converter to the external clamp level input signal. This voltage is output via the CL_{out} pin and provides the capability to do on chip dc restoration of the video signal. The input video signal can be clamped by connecting CL_{out} to the video input, and inputting a video signal with ac coupling.

A/D Converter

The composite video signal input is converted to the digital code by the high speed 8–bit A/D converter. The input voltage range is determined by the value of the reference voltage inputs, RBT and RTP. The limits for the converter are 1.4 V minimum for RBT and $V_{CC(AD)}$ – 0.3 V maximum for RTP. This produces a maximum conversion value of 3.3 V p–p maximum video input signal for $V_{CC(AD)}$ of 5 V. A self–bias function generating V_{TP} = 4.6 V, V_{BT} = 1.6 V can be realized by connecting the internal A/D converter reference voltage supply with the A/D converter reference pin. The sampling clock frequency of the A/D converter is 14.3 MHz which is four times the color subcarrier frequency.

Clamp Voltage Regulating Circuit

The clamp voltage regulating circuit sync tip clamps the input signal when the V_{in} pin is connected to the CL_{out} pin and the video signal is input using ac coupling. It compares the digital value of the clamp level input, C0 – C7, with the A/D converter output code. The clamp voltage is output by the CL_{out} pin. The clamp circuit operates as though the sync tip level of the video signal is synchronized with the digital value input to C0 – C7.

In the digital input comb filtering mode and the digital output comb filtering mode, the video signal is clamped by fixing the internal clamp level to ($08). The value of C0 – C7 is ignored by the clamp circuit with these operating modes.

The circuit operates in the bias mode during the CCF mode. It outputs half the value of the A/D converter reference voltage from CL_{out}. The input video signal is biased at half of the A/D converter reference voltage by connecting the CL_{out} with V_{in} and inputting the video signal via ac coupling.

Advanced Comb Filter

The Advanced Comb Filter is an adaptive digital filter that includes a delay line memory, latches and 8–bit adders. The basic function of the filter is adding and subtracting various delayed values using the adders. The calculations for each sampled data are completed within one clock cycle, approximately 70 ns. Each adder has latches to maintain the calculated value. If the speed of the adders is not fast enough, other latches may be added to save the partial value of the calculations. These latches will be counted as the digital signal delays.

There are two major data passes in this filter, the chrominance and luminance. Both data passes are designed so that all delays match when these signals are outputted. Inside this filter, there are two band–pass filters which have different bandwidths. This allows the selection of the color signal bandwidth via an exterior BW pin. Table 1 shows the relationship between the BW pin and the bandwidth.

Table 1. Bandwidth Conversion Function

Bandwidth	BW
Narrow	L
Wide	H

D/A Converter

The luminance and chrominance signals separated in the advanced comb filtering portion are converted to analog signals by two 8–bit D/A converters. The output voltage range is from 0.3 V to 1.5 V, 1.2 V p–p. The sampling clock of the D/A converter is 14.3 MHz. This is the same as the A/D converter.

OPERATING MODES

The Advanced Comb Filter can be operated in any of four modes. These modes are fixed by a digital code inputted into MODE 0 and MODE 1. The descriptions of the four types of operating modes are:

Normal Mode

This mode is for the normal Y/C separation. The video signal input to the A/D converter is separated into its Y and C components and output as analog information from the D/A converter outputs. The clamp circuit operates as sync tip clamp by connecting CL_{out} with V_{in}, and clamps the input video signal to the digital value input at C0 – C7.

Chrominance Comb Filter (CCF) Mode

This mode reduces the noise of a chrominance signal. The chrominance signal input to the A/D converter is filtered by the ACF algorithm, and the filtered chrominance signal is output from C_{out} after reducing the accumulated noise. The Y_{out} subtracting C_{out} components (noise components) removed by the comb filter algorithm are output at Y_{out}. The clamp circuit operates in the bias mode and biases the chrominance signal at the half point of the A/D converter reference voltage if CL_{out} is connected to V_{in}.

Digital Input Comb Filter Mode

In this mode the comb filter is used as two separate blocks, the A/D converter portion, and the filter and D/A portion. This mode can re–input and filter converted digital data output by the A/D converter after arbitrarily being digitally processed by external circuits. The converted digital data outputs into C0 – C7. Moreover, the data input into D0 – D7 is filtered by the ACF algorithm, and is output as an analog signal from Y_{out} and C_{out}. The two blocks can can operate independently with different frequency and phase clock signals. The CLK(AD) pin is the clock input to the A/D converter block and the CLK pin is the clock source for the filter and D/A converters. At this time, the clamp circuit works as a sync tip clamp when CL_{out} is connected to V_{in}, and clamps the input video signal to the internally fixed digital value ($08).

Digital Output Comb Filtering Mode

This mode outputs digital values of the luminance and chrominance signals in addition to functioning as a standard analog output Y/C separator. This allows arbitrary digital processing of the filter–processed Y and C digital outputs by an external circuit. It interfaces with an analog circuit easily, since both analog Y and C signals are output at the same time.

The video signal input to the A/D converter is converted to digital data, and forwarded to the filter portion. The Y/C separated data from the filter portion is output from Y_{out} and C_{out} after the D/A conversion. At the same time, the filter portion output is also forwarded to the digital interface and the luminance digital value is output from C0 – C7 and the chrominance digital value is output from D0 – D7. With this mode, the clamp circuit works as a sync tip clamp with CL_{out} connected to V_{in}, and clamps the input video signal internally to the fixed digital value ($08).

Table 2 shows the relationship between the MODE pins and MODE condition.

Table 2. Operating MODE Switching Function

Mode	MODE 1	MODE 0
Normal Mode	L	L
CCF Mode	L	H
Digital Input Comb Filtering Mode	H	L
Digital Output Comb Filtering Mode	H	H

APPLICATION DESIGN CONSIDERATIONS

V_{CC}, GND

To maximize the performance of the MC141621A, noise should be kept to a minimum. Good printed circuit board design will enhance the operation of the MC141621A. Separate analog and digital grounds will reduce noise and conversion errors. In addition, separate filters on analog V_{CC} and digital V_{DD} will also help to minimize noise and conversion errors. Sufficient decoupling and short leads will also improve performance.

When designing mixed analog/digital printed circuit boards, separate ground planes for digital ground and analog ground should be employed. Large switching currents generated by digital circuits will be amplified by analog circuitry and can quickly make a circuit unusable. Care should be taken to ensure analog ground does not inadvertently become part of the digital ground. The analog and digital grounds should be connected together at only one point. This is usually at or near where power enters the printed circuit board. Additionally, when interconnecting several printed circuit boards together, care must be taken to ensure that cabling does not interconnect digital and analog grounds together to produce a path for digital switching currents through analog ground.

When using any device with the performance and speed of the MC141621A, ground planes are essential. Loosely interconnected traces and/or random areas of ground strewn around the printed circuit board are inadequate for high performance circuitry. While distribution of V_{DD} and V_{CC} can be done by bussing, to do so with the ground system is disastrous.

A 1–inch long conductor is an 18 nH inductor. The cross sectional area of the conductor affects the exact value of the inductance, but for most PCB traces this is approximately correct. If the ground system is composed of traces or clumps of ground loosely interconnected, it will be inductive. The amount of inductance will be proportional to the length of the conductors making up the ground. This inductance cannot be decoupled away. It must be designed out.

A CMOS device exhibits a characteristic input capacitance of about 10 pF. If this gate is driven by a digital signal that switches 2.5 V in a period of 5 ns, the equation for the average current flowing during the switching time will be:

$$I_{AV} = Cdv/dt.$$

A voltage change of 2.5 V in 5 ns requires an average current of 5 mA. If we assume a linear ramp starting from zero, the total change in current will be 10 mA. The change in current per nanosecond per gate can be found by dividing the change in current by the time

$$10\ mA/5\ ns = 2\ mA/ns.$$

For a device with 16 outputs driving one gate for each output,

$$di/dt = 16 \times 2\ mA/ns = 32\ mA/ns.$$

If the above 1–inch wire is in this current path, then the voltage dropped across it can be found from the formula

$$V = Ldi/dt = 18\ nH \times 32\ mA/ns = 0.576\ V.$$

If the inductor is in the ground system, it is in the signal path. The voltage generated by the switching currents through this inductor will be added to the signal. At best it will be superimposed on the analog signal as unwanted noise. At worst, it can render the entire circuit unusable. Even the digital signal path is not immune to this type of signal. It can false trigger clock circuits causing timing errors, confuse comparator type circuits, and cause digital signals to be misinterpreted as wrong values.

When laying out the PCB, use electrolytic capacitors of sufficient size at the power input to the printed circuit board. 47 μF tantalum capacitors are recommended. Adding low ESR (effective series resistance) decoupling capacitors of about 0.1 μF capacitance across V_{CC} and/or V_{DD} at each device will help reduce noise in general and ESD (electrostatic discharge) susceptibility. Connect the high–capacity and high–frequency capacitors as close as possible to all analog V_{CC}, digital V_{DD}, and ground pins. Implementation of a good ground plane ground system can all but eliminate the type of noise described above.

To summarize, use sufficient electrolytic capacitor filtering, make separate ground planes for analog ground and digital ground, tie these grounds together at one and only one point, keep the ground planes as continuous and unbroken as possible, use low ESR capacitors of about 0.1 μF capacitance on V_{CC} and V_{DD} at each device, and keep all leads as short as possible.

V_{in}

In order to prevent flyback noise on the video input, it is necessary to keep the bandwidth to less than 1/2 the clock frequency by using an area filter. Here the amplifier used as an input buffer needs a wide bandwidth and driving capability. Moreover, to minimize external noise effects, drive the V_{in} pin with a low impedance amplifier and keep the V_{in} pin as close as possible to the amplifier output.

When using the built–in clamp circuit, connect CL_{out} to V_{in} and input signals after ac coupling by using a high–performance, high–frequency capacitor of 1 to 0.1 μF capacitance. In this case, keep the V_{in}, CL_{out}, coupling capacitor, and buffer–amplifier wiring as short as possible. Pay attention to the external noise and parasitic impedance.

CLC

The CLC pin sets the clamp circuit speed with an external capacitor and resistor.

Generally, the capacitor and resistor are arranged in a row and connected to GND(AD). Select a capacitor that minimizes the dielectric absorbing error. When the capacitor capacity is reduced, the shift speed of the video signal to $V_{CC(AD)}$ side is accelerated. If the resistor value is too small at this point, sagging will appear in the video signal. Also, if the capacitor's capacity is too large, the clamp speed will slow down; therefore, it is very important to pay attention to the setup of the resistor and capacitor values.

DA REFERENCE

REF(DA) is a DA converter reference decoupling pin for both the Y_{out} and C_{out}. Bypass to GND(DA) by applying a high–performance, high–frequency capacitor as close to the pin as possible. A 0.1 μF multilayer ceramic capacitor is recommended.

CLOCK INPUT

The clock frequency input is 14.31818 MHz, which is four times the frequency of a subcarrier. The minimum input level is 500 mV p–p. It should be synchronized with inputting the subcarrier of the video signal.

The clock line should be wired with the shortest wire and be separated from other circuits to minimize cross coupling to other signals. The CLK(AD) pin is used only during digital input comb filtering mode; therefore, it should be at GND level unless the device is used in the digital input comb filtering mode.

I_{bias}

The I_{bias} pin is used to set up the bias current for the AD and DA converters. Connect an external resistor between the I_{bias} and GND(DA).

DIGITAL INPUT COMB FILTERING MODE

Connect CLK(AD) to GND(D) when the AD converter is not being used. Connect D0 – D7 to GND(D) when the DA converter and filter are not being used. This is to eliminate any unnecessary operation of blocks that are not being used.

LATCH–UP

The $V_{CC(AD)}$, $V_{CC(DA)}$, and $V_{CC(D)}$ pins connect to power supplies that are independent from each other. Therefore, latch–up may occur when the power is applied. To eliminate latch–up, apply power to the $V_{CC(AD)}$, $V_{CC(DA)}$, and $V_{CC(D)}$ pins simultaneously.

APPLICATION CIRCUITS

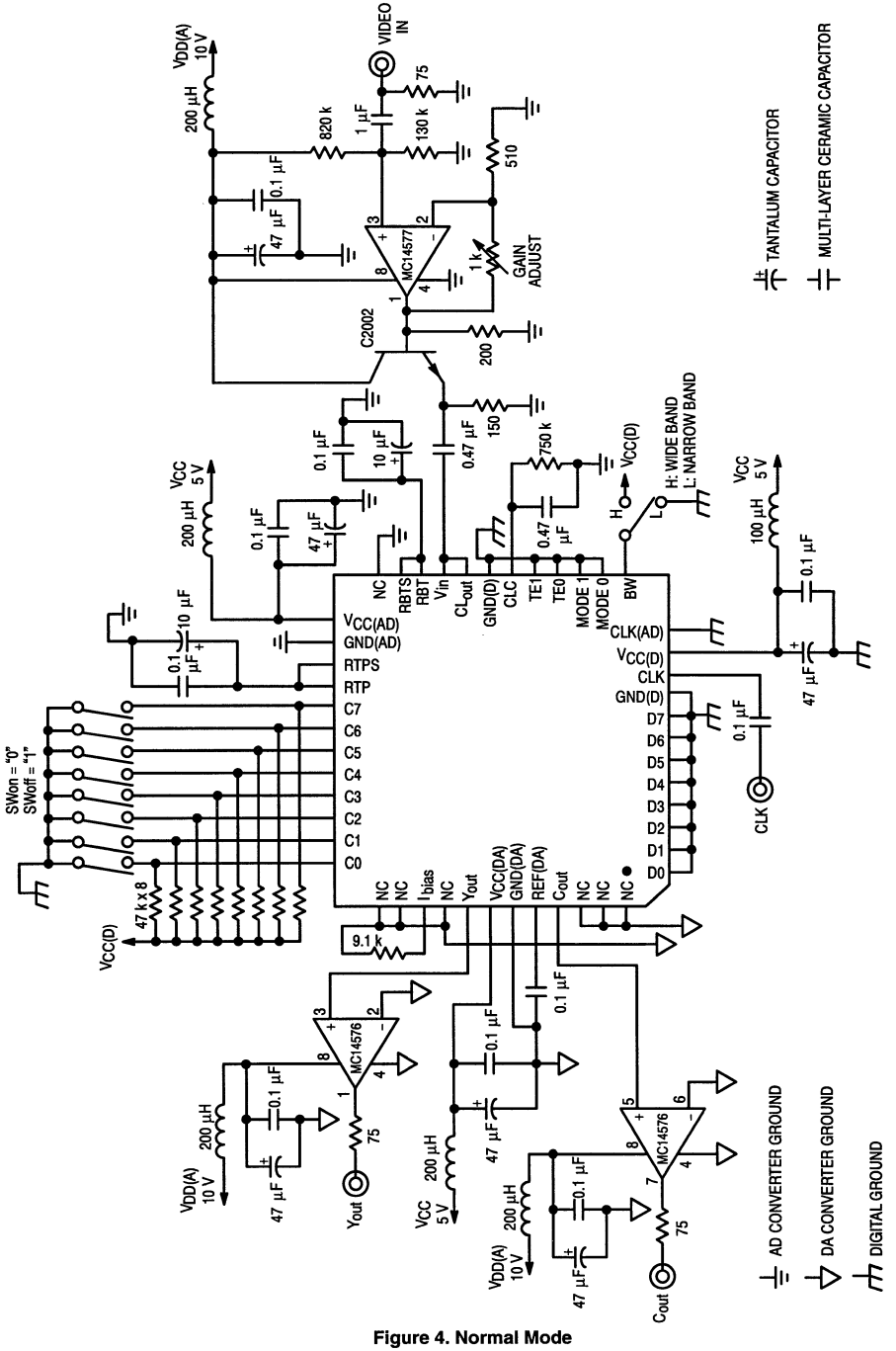


Figure 4. Normal Mode

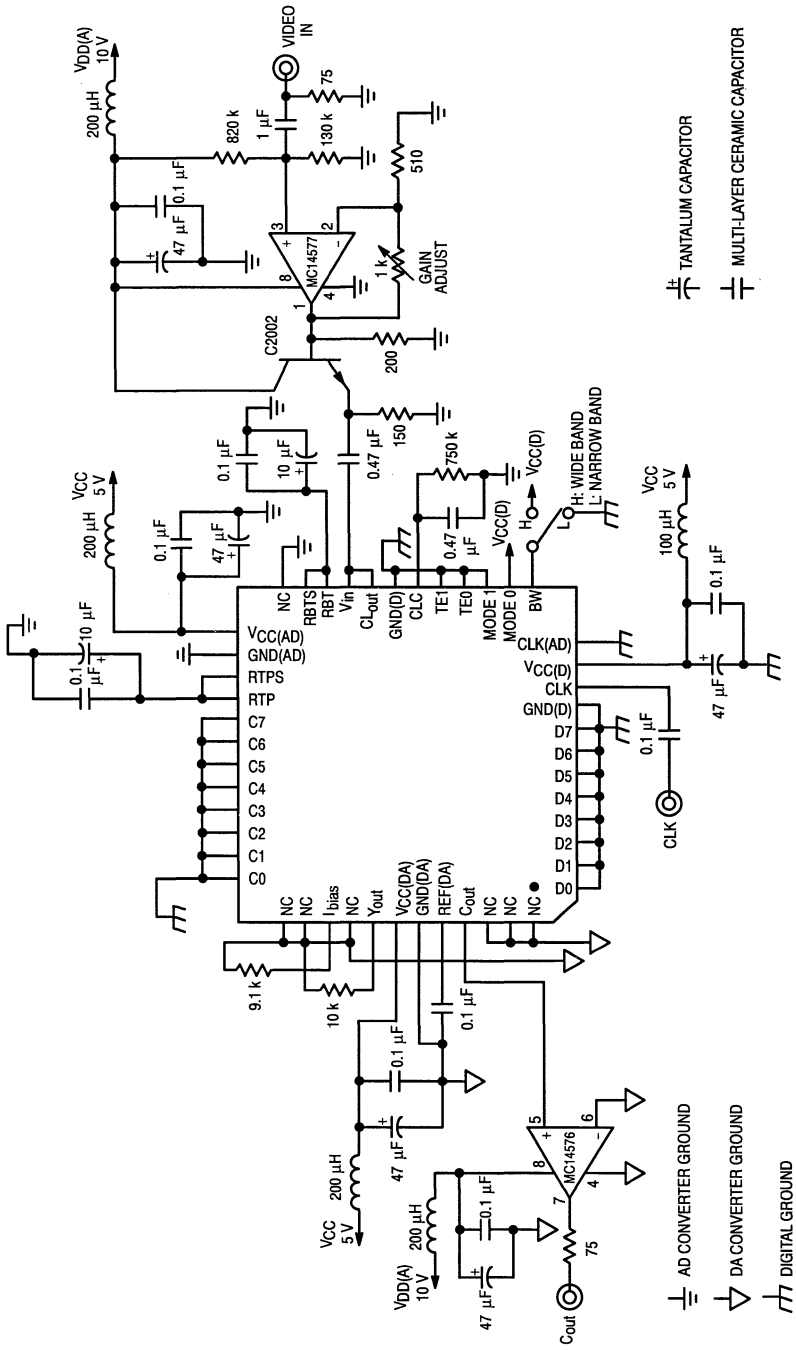


Figure 5. CCF Mode

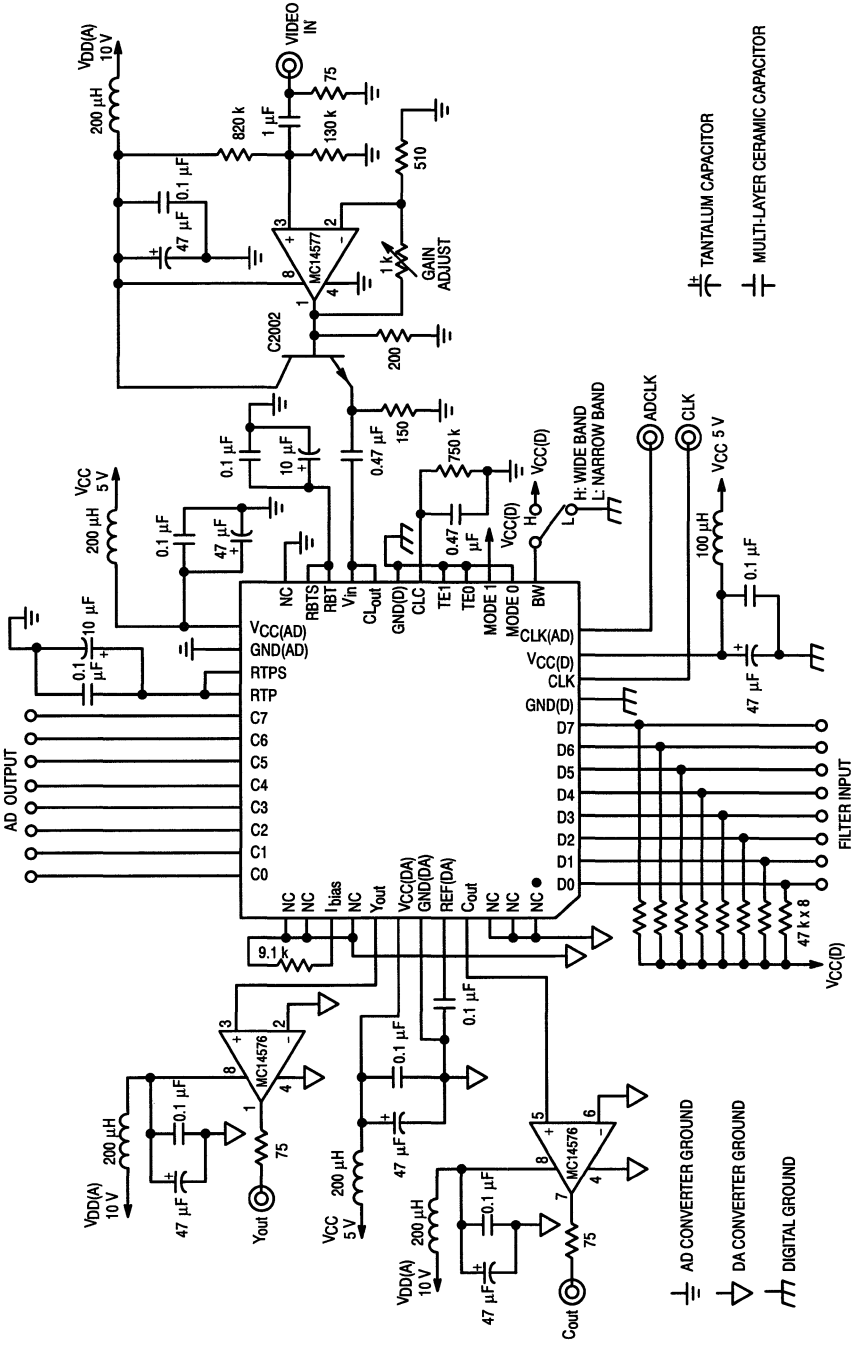


Figure 6. Digital Input Comb Filtering Mode

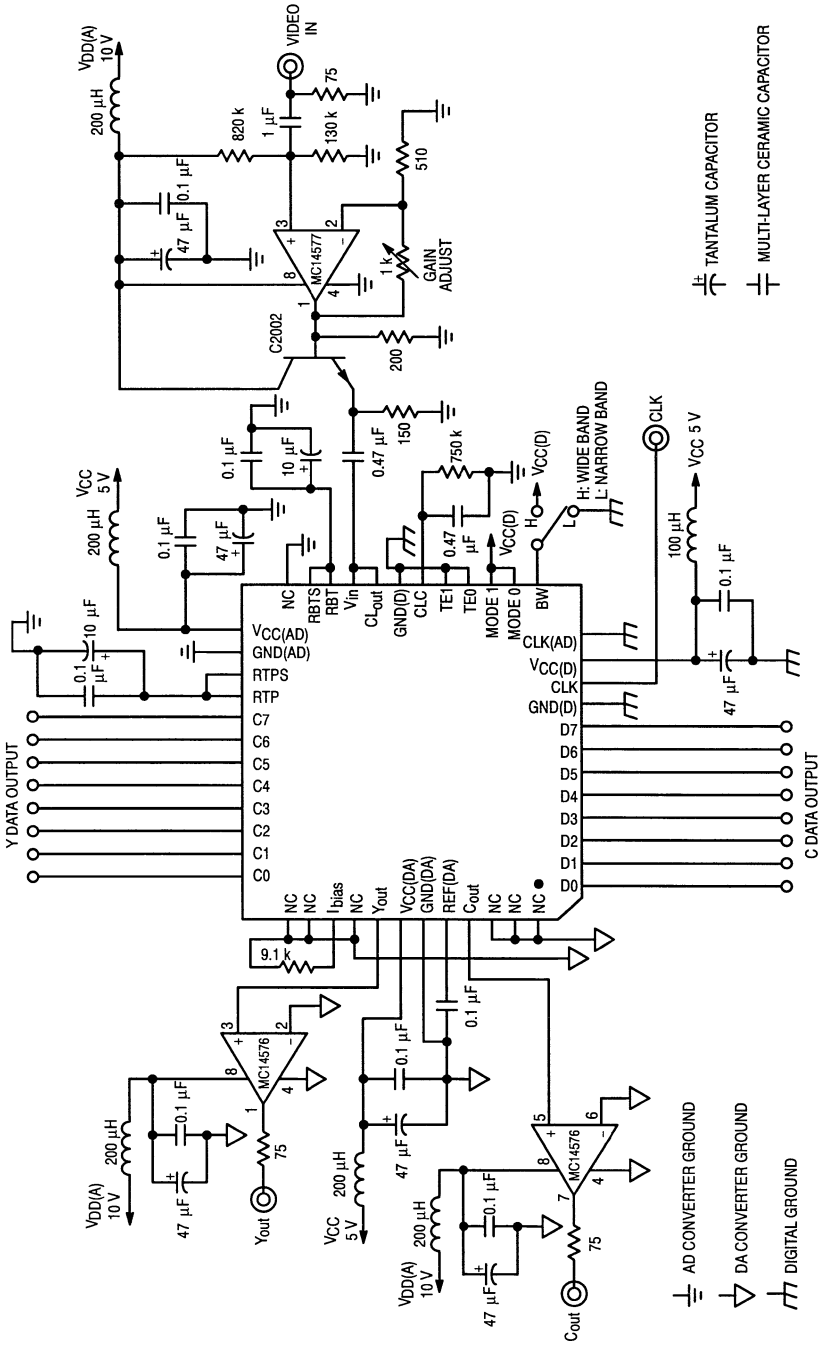


Figure 7. Digital Output Comb Filtering Mode

EMI SUPPRESSION

When using ICs in or near television receiver circuits, EMI (electromagnetic interference) and subsequent unwanted display artifacts and distortion are probable unless adequate EMI suppression is implemented. A common misconception is that some offending digital device is the culprit. This is erroneous in that an IC itself has insufficient surface area to produce sufficient radiation. The device, while it is the generator of interfering signals, must be coupled to an antenna before EMI is radiated. The source for the EMI is not the IC which generates the offending signals but rather the circuitry which is attached to the IC.

2

Potential EMI signals are generated by ***all*** digital devices. Whether they become a nuisance is dependent upon their frequency and whether they have a sufficient antenna. The frequency and number of these signals is affected by both circuit design within the IC and the manufacturing process. Device speed is also a major contributor of potential EMI. because the design is determined by the anticipated application, the manufacturing process is fixed and the drive for speed ever increasing, the only effective point to implement EMI suppression is in the PC board design. The PC board usually is the antenna which radiates the EMI. The most efficient method of minimizing EMI radiation is to minimize the efficiency of this antenna.

The most common cause of inadequate EMI suppression lies with the ground system of the suspected digital devices. As pointed out previously, di/dt transitions can be significant in digital circuits. If the di/dt transitions appear in the ground system and the ground system is inductive, the harmonics present in these transitions are a source of potential EMI signals. The unfortunate result of putting digital devices on a reactive ground system is guaranteed EMI problems.

The area which should be addressed first as a potential EMI source is the ground. Without an adequate ground system, EMI cannot be effectively reduced by decoupling. If at all possible, the ground should be a complete unbroken plane. Figure 8 shows two examples of relieving ground around device pins. When relieving vias and plated through holes, large areas of ground loss should be avoided. When the relief pattern is equal to half the distance between pins, over etching and process errors may remove ground between pins. If sufficient ground around enough pins are removed, the ground system can become isolated or nearly isolated "patches" which will appear inductive. If ground, such as the vicinity of an IC, must be removed, replace with a cross hatch of ground lines with the mesh as small as possible.

If a single unbroken plane can be devoted to the ground system, EMI can usually be sufficiently suppressed by using ferrite beads on suspect EMI paths and decoupling with adequate values of capacitors. The value of the decoupling capacitor depends on the frequency and amplitude of the offending signals. Ferrite beads are available in a wide variety of shape, size and material to fit virtually any application.

Choose a ferrite bead for desired impedance at the desired frequency and construct a low pass filter using one or more appropriate capacitors in a "L", "T" or "PI" arrangement. Use only capacitors of low inductive and resistive properties such as ceramic or mica. Install filters in series with each IC pin suspected of contributing offending EMI signals and as close to the pin as possible. Analysis using a spectrum analyzer can help determine which pins are suspect.

Where PC board costs constrain the number of layers available, and if the EMI frequencies are far removed from the frequencies of operation, ferrite beads and decoupling capacitors may still be effective in reducing EMI emissions. Where only two (or in some cases, only one!) layer is used, the ground system is always reactive and poses an EMI problem. If the offending EMI and normal operating frequency differ sufficiently, filtering can still work.

An "island" is constructed in the ground system for the digital device using ferrite beads and decoupling capacitors as shown by the example in Figure 9. The ground must be cut so that the digital ground for the device is isolated from the rest of the ground system. Next choose a ferrite bead of the appropriate value. Install this bead between the isolated ground and the ground system. Install low pass filters in all suspect lines with the capacitor closest to the device pin connected to the isolated ground in all signal lines where EMI is suspect. Also cut the power to the device and insert a ferrite bead as shown in Figure 9. Finally, decouple the device between the power pin(s) and isolated ground pin(s) using a low inductive/resistive capacitor of adequate value.

The methods described above will work acceptably when the EMI frequency and the frequency of operation of the device generating the EMI differ greatly. Where the EMI is disturbing the high VHF or UHF channels and the device generating the EMI is operating within the NTSC/PAL bandwidth, the energy contained in the harmonics generating the EMI is situated well above the operating frequency and suppressing this type of EMI poses no great problem. However, if the EMI is present on low VHF channels and/or the operation of the device is outside the NTSC/PAL bandwidth, such as a 2X pixel clock or 4xfsc oscillator, compromise between video quality and suppression complexity is usually required to obtain an acceptable solution. For those cases where the operating frequency of the device is very near the frequency of the EMI disturbance, careful attention to PCB layout, multiple layer PCB and even shielding may be necessary to obtain an acceptable design.

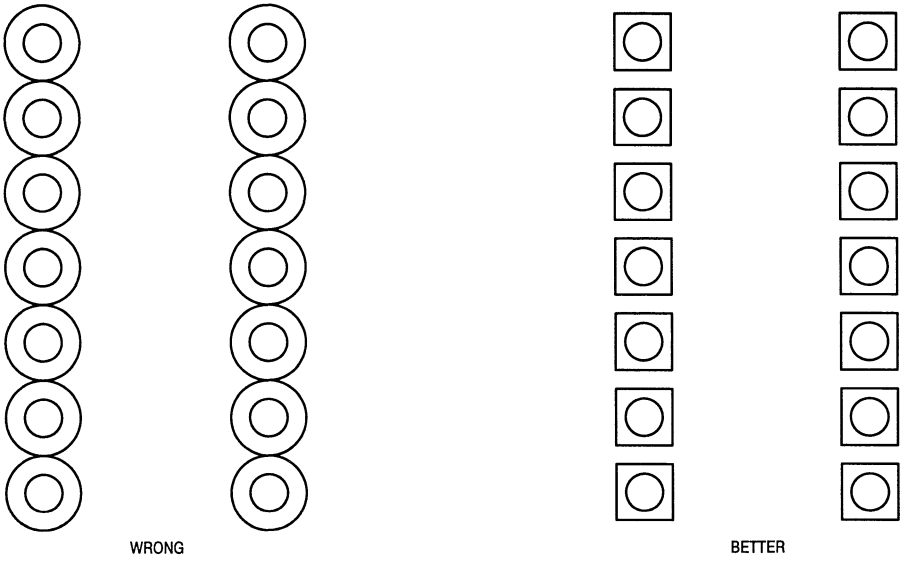


Figure 8.

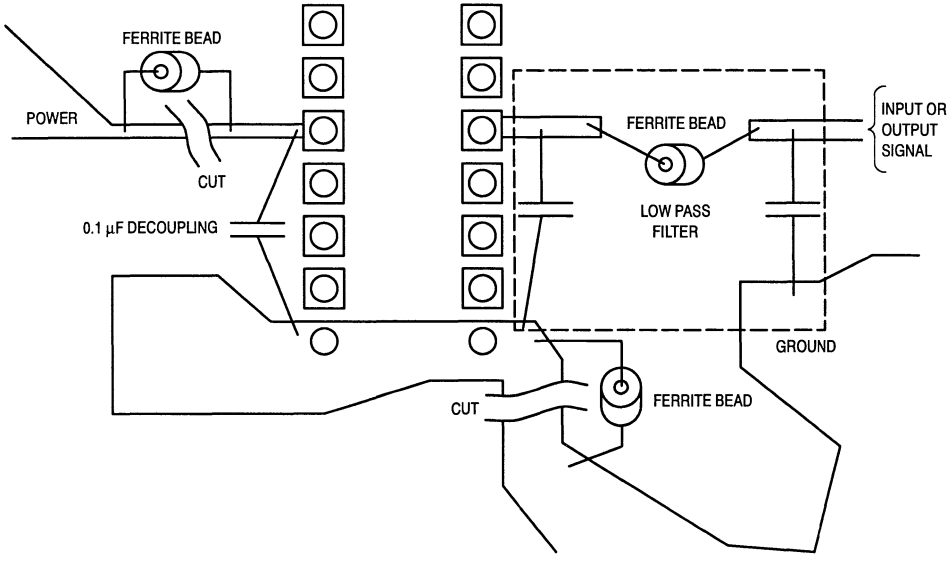
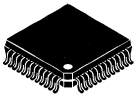


Figure 9.

MC141622

Advance Information

Advanced Comb Filter-II (AFC-II)



P SUFFIX
48–LEAD QFP
CASE 898–01

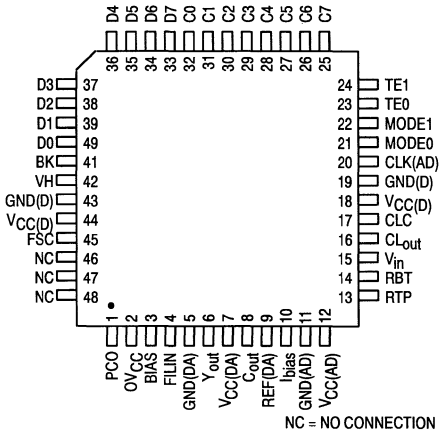
ORDERING INFORMATION
MC141622FU
Quad Flat Package (QFP)

2

The Advanced Comb Filter–II is a video signal processor for VCRs and TVs. It's function is to separate the Luminance Y and Chrominance C signals from the NTSC composite video signal. The ACF–II minimizes dot–crawl and cross–color. A built–in PLL provides a 4xfsc clock from either an NTSC subcarrier signal or a 4xfsc input. This allows a video signal input of an extended frequency bandwidth. The built–in vertical enhancer circuit improves the quality of the Luminance Y signal. The built–in A/D and D/A converters allow easy connection to analog video circuits.

- Built–in High Speed 8–Bit A/D Converter
- Two Line Memories (1820 Bytes)
- Advanced Comb–II Process
- Vertical Enhancer Circuit
- Two High Speed 8–Bit D/A Converters
- 4xfsc PLL Circuit
- Built–in Clamp Circuit
- Digital Interface Mode
- On–Chip Reference Voltage Regulator for A/D Converter

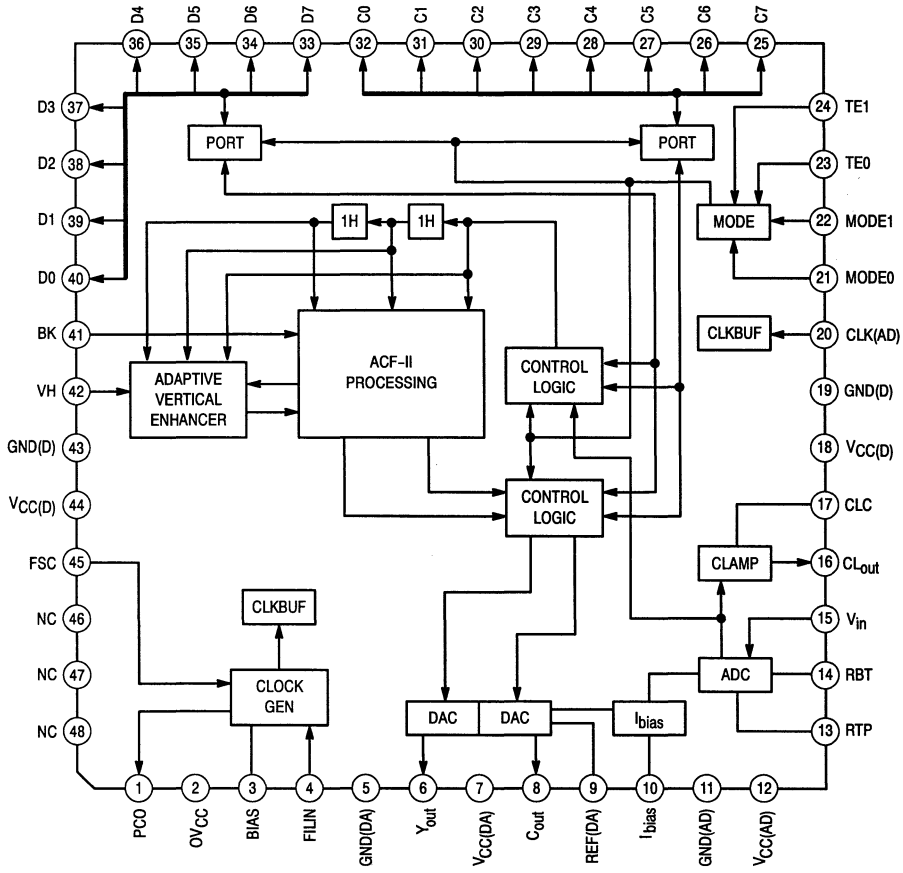
PIN ASSIGNMENT



NC = NO CONNECTION

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Value	Unit
DC Supply Voltage (Referenced to GND)	V_{CC}	– 0.5 to + 7.0	V
DC Input Voltage (Referenced to GND)	V_{in}	– 1.5 to V_{CC} + 1.5	V
DC Output Voltage (Referenced to GND)	V_{out}	– 0.5 to V_{CC} + 0.5	V
DC Input Current (per pin)	I_{in}	± 20	mA
DC Output Current (per pin)	I_{out}	± 25	mA
Power Dissipation	P_D	750	mW
Storage Temperature	T_{stg}	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

GENERAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C, Unless Otherwise Noted)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Operating Supply Current	I_{CC}	—	115	140	mA	1
Operating Power Dissipation	P_D	—	575	735	mW	1
Ambient Operating Temperature	T_A	– 20	—	75	°C	

NOTE:
1. At normal mode.

CLOCK INPUT ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C, Unless Otherwise Noted)

Characteristic		Symbol	Min	Typ	Max	Unit	Notes
Subcarrier Input Frequency		f_c	—	3.579545	—	MHz	1
Clock Frequency		CLK	—	14.31818	—	MHz	2
FSC Clock Input Level		V_{fc}	1	—	—	V p-p	3
High Level Input Voltage	CLK(AD)	V_{ICH}	3.15	—	—	V	4
Low Level Input Voltage	CLK(AD)	V_{ICL}	—	—	1.1	V	4
Clock Duty Cycle	CLK/CLK(AD)	Dty	45	50	55	%	4

NOTES:
1. Color subcarrier input [FSC = (455/2)fh] locked on the burst signal of the input video signal. AC coupling input by external capacitor.
2. The internal circuit operates by four times clock using FSC–pin input at normal (FSC) mode.
3. Sine wave input.
4. CLK(AD) is available only during digital input comb filter mode.

ADC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	—	—	—	8	Bits
Integral Nonlinearity	INL	—	± 1.5	± 2.5	LSB
Differential Nonlinearity	DNL	—	± 0.5	± 1.0	LSB
Top Reference Level	V_{TPS}	4.5	4.6	4.7	V
Bottom Reference Level	V_{BTS}	1.45	1.55	1.65	V
Maximum Analog Input Range During Self Reference	V_{ins}	2.85	3.05	3.25	V p-p

DIGITAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic		Symbol	Min	Typ	Max	Unit
High Level Input Voltage	MODE0, MODE1, TE0, TE1, BK, C0 – C7, D0 – D7	V_{IH}	3.15	—	—	V
Low Level Input Voltage	MODE0, MODE1, TE0, TE1, BK, VH, C0 – C7, D0 – D7	V_{IL}	—	—	1.1	V
Input Leakage Current [V_{in} = $V_{CC(D)}$ or GND(D)]	MODE0, MODE1, TE0, TE1, BK VH C0 – C7, D0 – D7	I_{inl}	—	—	± 10	µA
Data Setup Time (at Digital Input Comb Filter Mode)	D0 – D7	t_{ds}	0	—	—	ns
Data Hold Time (at Digital Input Comb Filter Mode)	D0 – D7	t_{dh}	20	—	—	ns
Data Input Rise Time (at Digital Input Comb Filter Mode)	D0 – D7	t_r	—	—	10	ns
Data Input Fall Time (at Digital Input Comb Filter Mode)	D0 – D7	t_f	—	—	10	ns
Output Data Delay (at Digital Input/Output Comb Filter Mode)	C0 – C7, D0 – D7	t_{dl}	—	45	—	ns

FILTERING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Y/C Separation	—	40	—	—	dB
Band-Pass Filter Bandwidth (at – 3 dB)	—	—	± 0.75	—	MHz

DAC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	—	—	—	8	Bits
Integral Nonlinearity	INL	—	—	± 1	LSB
Differential Nonlinearity	DNL	—	—	± 0.5	LSB
Analog Output Voltage, Y_{out}	V_{YO}	1.1	1.2	1.3	V p-p
Analog Output Voltage, C_{out}	V_{CO}	1.1	1.2	1.3	V p-p
Full Scale Voltage, Y_{out}	V_{YFS}	1.3	1.5	1.7	V
Full Scale Voltage, C_{out}	V_{CFS}	1.3	1.5	1.7	V
Zero Scale Voltage, Y_{out}	V_{YZS}	0.1	0.3	0.5	V
Zero Scale Voltage, C_{out}	V_{CZS}	0.1	0.3	0.5	V
Output Impedance	Z_O	—	100	300	Ω

CLAMP CIRCUIT CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Clamp Mode Output Voltage*	V_{clys}	—	1.6	—	V

* At using the clamp circuit when connecting V_{in} – CL_{out}.

BK/VH CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
BK Switching Time, at Normal Mode		—	9	—	Clock
VH Switching Time, at Normal Mode		—	9	—	Clock

2

VERTICAL ENHANCER LEVEL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Noise Slice Level, at Normal Mode		0	—	15	bit
White Enhance Level, at Normal Mode		0	—	15	bit
Black Enhance Level, at Normal Mode		0	—	15	bit

GENERAL SIGNAL DELAY (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Normal Mode, 938 Clock		—	65.511	—	µs

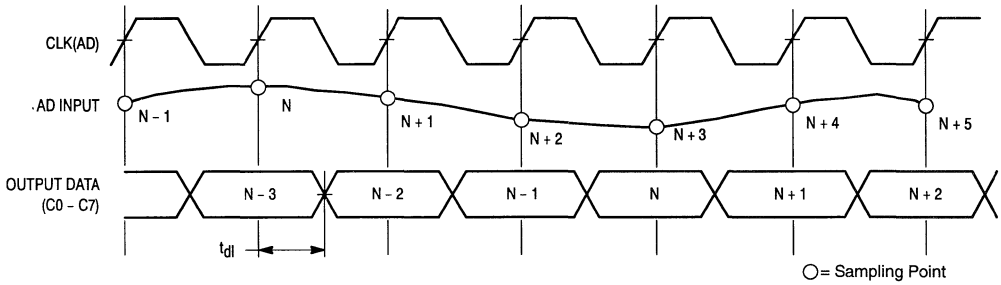


Figure 1a. A/D Converter Timing Diagram (During Digital Input Comb Filtering Mode)

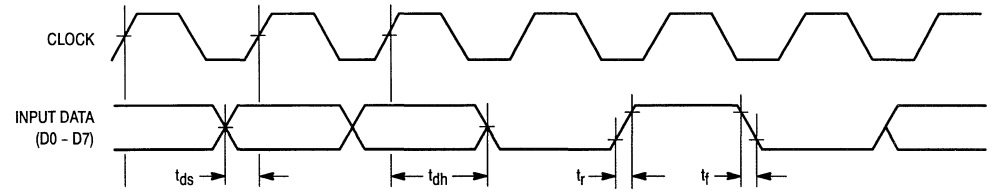


Figure 1b.Digital Signal Input Timing Diagram (During Digital Input Comb Filtering Mode)

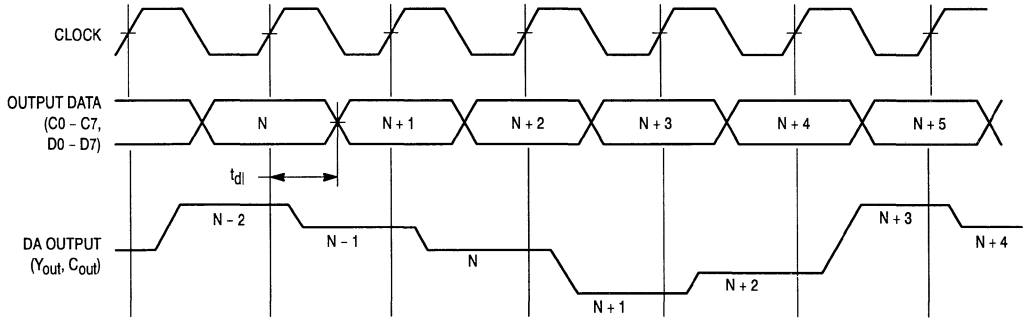


Figure 1c. Output Signal Timing Diagram (During Digital Output Comb Filtering Mode)

Figure 1. Timing Diagrams

Clamp Circuit Characteristics (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Clamp Mode Output Voltage, V_{cly} (Non-input when connecting V_{in} – CL_{out})

$V_{cly} = (V_{TP} - V_{BT})\ (N + 1) / 256 + V_{BT} \pm 50$ mV

where N = Clamp Code Input (N < 255)

- If the calculated value of the output voltage, $V_{cly} > V_{clys}$, then $V_{cly} = V_{clys}$
- Clamp Value N is fixed, N = 4.

PIN DESCRIPTIONS

Pin	Pin Name	Function
1	PCO	Phase comparator output.
2	OV_{CC}	Power supply for VCO.
3	BIAS	Reference for VCO. Generally connected to GND(D) through an external resistor.
4	FILIN	VCO controlled voltage input. Generally connected to PCO through an external loop filter.
5	GND(AD)	GND for D/A converter.
6	Y_{out}	Luminance signal output.
7	$V_{CC(DA)}$	Power supply for D/A converter.
8	C_{out}	Chrominance signal output.
9	REF(DA)	Reference for D/A converter. Generally connected to GND(DA) through a multilayer ceramic capacitor (0.1 µF).
10	I_{bias}	Bias circuit current control for A/D, D/A converters. Generally connected to GND(DA) through an external resistor.
11	GND(AD)	GND for A/D converter.
12	$V_{CC(AD)}$	Power supply for A/D converter.
13	RTP	Top reference for A/D converter. Supplies top reference voltage internally.
14	RBT	Bottom reference for A/D converter. Supplies bottom reference voltage internally.
15	V_{in}	A/D converter input.
16	CL_{out}	Voltage output for clamp. Clamps an input signal by connecting with V_{in} and inputting the video signal by ac coupling.
17	CLC	Clamp time constant setting pin.
18	$V_{CC(D)}$	Power supply for digital circuit.
19	GND(D)	GND for digital circuit.
20	CLK(AD)	CLK input for A/D converter. Available only during digital input comb filtering mode and a portion of test mode. Input level is CMOS level.
21, 22	MODE0, MODE1	Mode input. GND level during normal (FSC) mode.
23, 24	TE0, TE1	Test mode input. Generally GND level.
25	C7	Digital interface 1, input/output. Generally $V_{CC(D)}$ level.
26 – 28	C6 – C4	Digital interface 1, input/output. Generally GND(D) level.
29	C3	Digital interface 1, input/output. Generally $V_{CC(D)}$ level.
30 – 32	C2 – C0	Digital interface 1, input/output. Generally GND(D) level.
33	D7	Digital interface 2, input/output. Generally $V_{CC(D)}$ level.
34 – 40	D6 – D0	Digital interface 2, input/output. Generally GND(D) level.
41	BK	Non–color signal processing mode. Generally GND(D) level.
42	VH	Vertical enhancer circuit mode. Generally GND(D) level.
43	GND(D)	GND for digital circuit.
44	$V_{CC(D)}$	Power supply for digital circuit.
45	FSC	CLK input. AC coupling input by external capacitor. Normal (fsc) mode: Subcarrier. Normal (4xfsc) mode: 4* Subcarrier.
46 – 48	NC	No connection. Generally GND level.

Figure 2 shows the I/O signals of the Advanced Comb Filter–II.

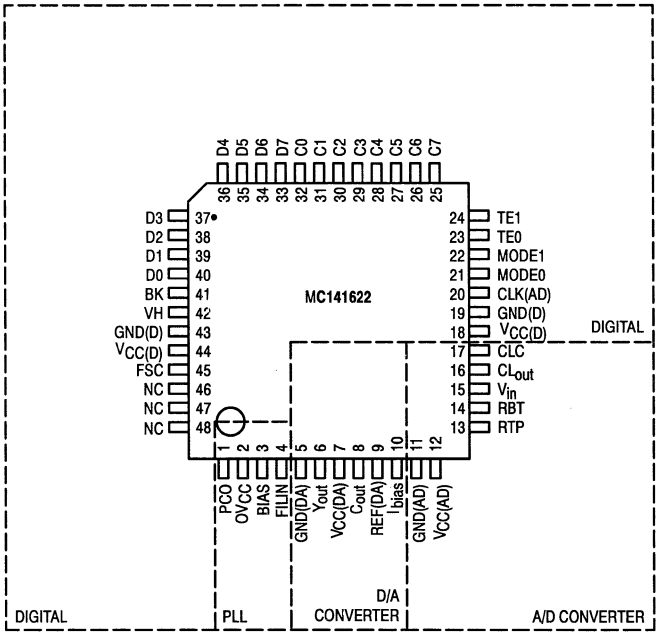


Figure 2. Pin Assignment

DEVICE DESCRIPTION

INTRODUCTION

The Advanced Comb Filter–II (ACF–II) is a high–performance HCMOS digital filter with built–in A/D and D/A converters. The basic function of the chip is the separation of the Luminance Y and Chrominance C signals from the NTSC composite video signal. The ACF–II minimizes the problems often generated by Y/C separation such as dot–crawl and cross–color. It uses a 14.3 MHz clock that allows an extended frequency bandwidth video signal to be input. This Y/C separation is realized by the digital advanced comb filters. The built–in 4xfsc PLL circuit allows a subcarrier signal input, from which a 4xfsc clock is generated for video signal processing. This allows a video signal input of an extended frequency bandwidth. The built–in vertical enhancer circuit can enhance the Luminance Y signal. The built–in A/D and D/A converters allow easy connection to analog video circuits.

ADVANCED COMB FILTER–II DESCRIPTION

The simplified block diagram of the Advanced Comb Filter–II chip is shown at the beginning of this data sheet. There are five major functions represented in this block diagram. The first block is the A/D conversion block. The high speed 8–bit binary analog–to–digital converter converts the incoming analog video signal to an 8–bit binary data stream. The conversion frequency is 14.3 MHz which is four times the color subcarrier frequency.

The second block contains the Advanced Comb Filter–II algorithm. The digital data from the A/D converter is processed by the algorithm of the Advanced Comb Filter–II. The composite video is filtered by the band–pass filter (BPF) and separated into the Luminance Y and Chrominance C signals.

The third block is the vertical enhancer circuit block. This vertical enhancer emphasizes the picture outline of the vertical direction.

The fourth block is the digital–to–analog conversion block. Two 8–bit D/A converters convert the luminance and chrominance into analog outputs. The conversion frequency is four times the subcarrier signal (14.3 MHz). The chrominance analog output is biased with a dc offset of half the value of the DA converter reference.

The fifth block is a 4xfsc CLK generation circuit. This block generates four times the subcarrier signal and phase locks the inputting subcarrier on FSC pin.

A/D Converter

The composite video signal input is converted to the digital code by the high speed 8–bit A/D converter. The A/D converter reference has a self–bias function which generates V_{TP} = 4.6 V, V_{BT} = 1.55 V. This allows the A/D converter to function without an external reference circuit.

Clamp Voltage Regulating Circuit

The clamp voltage regulating circuit sync tip clamps the input signal when the V_{in} pin is connected to the CL_{out} pin and the video signal is input using ac coupling. It compares the

digital value of the clamp level ($04) with the A/D converter output code. The clamp voltage from CL_{out} is then output.

Advanced Comb Filter–II

The Advanced Comb Filter–II is a digital comb filter developed for use in the NTSC system. The vertical correlation circuit provides high picture quality and high resolution and requires no adjustment for its Y/C separation. The clock frequency is 14.3 MHz, which is four times the NTSC subcarrier.

The BK pin can be used to select between the composite signal output without Y/C separation and the Y/C signal output. Table 1 shows the relationship of the BK pin and each output.

Table 1. BK Function

BK Pin	Y_{out}	C_{out}
L	Luminance	Chrominance
H	Composite	Chrominance

Adaptive Vertical Enhancer Circuit

The vertical enhancer circuit is used the adaptive enhanced processing using two line memories. The adaptive LPF of the vertical enhancer circuit minimizes noise and dot–crawl. This block does not emphasize horizontal and vertical sync signals. Table 2 shows the relationship of the VH pin and the vertical enhancer function. The coring characteristics of the vertical enhancer circuit can be set up on the digital port at the normal mode.

Table 2. VH Function

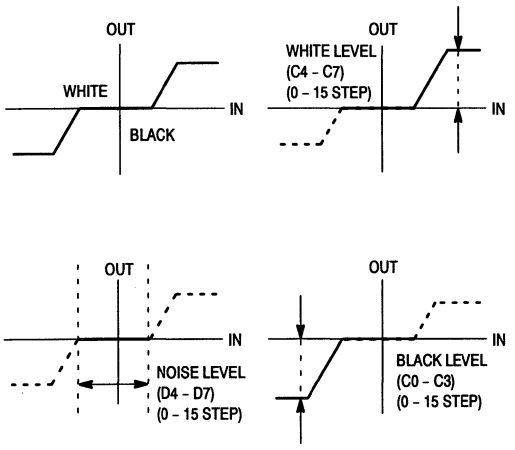
VH Pin	Vertical Enhancer
L	On
H	Off

D/A Converter

The luminance and chrominance signals separated in the advanced comb filtering portion are converted to analog signals by two 8–bit D/A converters. The output voltage range is from 0.3 V to 1.5 V, 1.2 Vp–p. The sampling clock of the D/A converter is 14.3 MHz.

Clock Generation Circuit

The internal PLL can be selected to operate in either of two modes; an X4 mode used to generate a 4xfsc clock from a normal NTSC color subcarrier, and an X1 mode when a 4xfsc signal is available.



C7	C6	C5	C4	
C3	C2	C1	C0	
D7	D6	D5	D4	Level
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	10
H	L	H	H	11
H	H	L	L	12
H	H	L	H	13
H	H	H	L	14
H	H	H	H	15

Figure 3. Coring Characteristics

OPERATING MODES

The Advanced Comb Filter–II can be operated in any of four modes. These modes are fixed by a digital code input into MODE0 and MODE1. The descriptions of the four types of operating modes are:

Normal (fsc) Mode

This mode is for the normal Y/C separation. The video signal input to the A/D converter is separated into its Y and C components and output as analog information from the D/A converter outputs. The clamp circuit operates as sync tip clamp by connecting CL_{out} with V_{in}, and clamps the input video signal to the fixed value $04. The coring characteristics of the vertical enhancer circuit can be set up on the digital port. This mode is used when an NTSC color subcarrier is used to generate a 4xfsc using the internal PLL.

Normal (4xfsc) Mode

This mode is for the normal Y/C separation. The video signal input to the A/D converter is separated into its Y and C components and output as analog information from the D/A converter outputs. The clamp circuit operates as sync tip clamp by connecting CL_{out} with V_{in}, and clamps the input video signal to the fixed value $04. The coring characteristics of the vertical enhancer circuit can be set up on the digital port. In this mode an external 4xfsc CLK is input on the FSC pin.

Digital Input Comb Filtering Mode

In this mode, the comb filter is used as two separate blocks; the A/D converter portion, and the filter and D/A portion. This mode can re–input and filter converted digital data outputs by the A/D converter after arbitrarily being digitally processed by external circuits. The converted digital data outputs into C0 – C7. Moreover, the data input into D0 – D7 is filtered by the ACF–II algorithm, and is output as an analog signal from Y_{out} and C_{out}. The two blocks can operate independently with different frequency and phase clock signals. The CLK(AD) pin is the clock input to the A/D converter block and the CLK pin the clock source (4xfsc) for the filter and D/A converters. At this time, the clamp circuit works as sync tip clamp when CL_{out} is connected to V_{in}, and clamps the input video signal to the internally fixed digital value ($04).

Digital Output Comb Filtering Mode

This mode outputs digital values of the luminance and chrominance signals in addition to functioning as a standard analog output Y/C separator. This allows arbitrary digital processing of the filter–processed Y and C digital outputs by an external circuit. It interfaces with an analog circuit easily, since both analog Y and C signals are output at the same time.

The video signal input to the A/D converter is converted to digital data, and forwarded to the filter portion. The Y/C separated data from the filter portion is output from Y_{out} and C_{out} after the D/A conversion. At the same time, the filter portion output is also forwarded to the digital interface and the luminance digital value is output from C0 – C7 and the chrominance digital value is output from D0 – D7. With this mode, the clamp circuit works as a sync tip clamp with CL_{out} connected to V_{in}, and clamps the input video signal internally to the fixed digital value ($04). This mode operates with an external 4xfsc CLK which is input on the FSC pin.

Table 3 shows the relationship between the MODE pin and MODE condition.

Table 3. Operating MODE Switching Function

Mode	MODE1	MODE0
Normal (fsc) Mode	L	L
Normal (4xfsc) Mode	L	H
Digital Input Comb Filtering Mode	H	L
Digital Output Comb Filtering Mode	H	H

APPLICATION DESIGN CONSIDERATIONS

V_{CC}, GND

To maximize the performance of the MC141622, noise should be kept to a minimum. Good printed circuit board design will enhance the operation of the MC141622. Separate analog and digital grounds will reduce noise and conversion errors. In addition, separate filters on analog V_{CC} and digital V_{DD} will also help to minimize noise and conversion errors. Sufficient decoupling and short leads will also improve performance.

When designing mixed analog/digital printed circuit boards, separate ground planes for digital ground and analog ground should be employed. Large switching currents generated by digital circuits will be amplified by analog circuitry and can quickly make a circuit unusable. Care should be taken to ensure analog ground does not inadvertently become part of the digital ground. The analog and digital grounds should be connected together at only one point. This is usually at or near where power enters the printed circuit board. Additionally, when interconnecting several printed circuit boards together, care must be taken to ensure that cabling does not interconnect digital and analog grounds together to produce a path for digital switching currents through analog ground.

When using any device with the performance and speed of the MC141622, ground planes are essential. Loosely interconnected traces and/or random areas of ground strewn around the printed circuit board are inadequate for high performance circuitry. While distribution of V_{DD} and V_{CC} can be done by bussing, to do so with the ground system is disastrous.

A 1–inch long conductor is an 18 nH inductor. The cross sectional area of the conductor affects the exact value of the inductance, but for most PCB traces this is approximately correct. If the ground system is composed of traces or clumps of ground loosely interconnected, it will be inductive. The amount of inductance will be proportional to the length of the conductors making up the ground. This inductance cannot be decoupled away. It must be designed out.

A CMOS device exhibits a characteristic input capacitance of about 10 pF. If this gate is driven by a digital signal that switches 2.5 V in a period of 5 ns, the equation for the average current flowing during the switching time will be:

$$I_{AV} = Cdv/dt.$$

A voltage change of 2.5 V in 5 ns requires an average current of 5 mA. If we assume a linear ramp starting from zero, the total change in current will be 10 mA. The change in current per nanosecond per gate can be found by dividing the change in current by the time

$$10\ mA/5\ ns = 2\ mA/ns.$$

For a device with 16 outputs driving one gate for each output,

$$di/dt = 16 \times 2\ mA/ns = 32\ mA/ns.$$

If the above 1–inch wire is in this current path, then the voltage dropped across it can be found from the formula

$$V = Ldi/dt = 18\ nH \times 32\ mA/ns = 0.576\ V.$$

If the inductor is in the ground system, it is in the signal path. The voltage generated by the switching currents through this inductor will be added to the signal. At best it will be superimposed on the analog signal as unwanted noise. At worst, it can render the entire circuit unusable. Even the digital signal path is not immune to this type of signal. It can false trigger clock circuits causing timing errors, confuse comparator type circuits, and cause digital signals to be misinterpreted as wrong values.

When laying out the PCB, use electrolytic capacitors of sufficient size at the power input to the printed circuit board. 47 μF tantalum capacitors are recommended. Adding low ESR (effective series resistance) decoupling capacitors of about 0.1 μF capacitance across V_{CC} and/or V_{DD} at each device will help reduce noise in general and ESD (electrostatic discharge) susceptibility. Connect the high–capacity and high–frequency capacitors as close as possible to all analog V_{CC}, digital V_{DD}, and ground pins. Implementation of a good ground plane ground system can all but eliminate the type of noise described above.

To summarize, use sufficient electrolytic capacitor filtering, make separate ground planes for analog ground and digital ground, tie these grounds together at one and only one point, keep the ground planes as continuous and unbroken as possible, use low ESR capacitors of about 0.1 μF capacitance on V_{CC} and V_{DD} at each device, and keep all leads as short as possible.

V_{in}

In order to prevent flyback noise on the video input, it is necessary to keep the bandwidth to less than 1/2 the clock frequency by using an area filter. Here the amplifier used as an input buffer needs a wide bandwidth and driving capability. Moreover, to minimize external noise effects, drive the V_{in} pin with a low impedance amplifier and keep the V_{in} pin as close as possible to the amplifier output.

When using the built–in clamp circuit, connect CL_{out} with V_{in} and input signals after ac coupling by using a high–performance, high frequency capacitor of 1 to 0.1 μF. In this case, keep the V_{in}, CL_{out}, coupling capacitor, and buffer–amplifier wiring as short as possible. Pay attention to the external noise and parasitic impedance.

AD Reference Pin

The RTP and RBT pins have a self–bias function that internally generates V_{TP} = 4.6 V and V_{BT} = 1.55 V. It acknowledges the AD converter analog input dynamic range. A stable performance can be achieved by applying a high–performance frequency capacitor as close as possible to the RTP and RBT pins and bypassing to GND(AD). A 0.1 μF multi-layer ceramic capacitor and a 10 μF tantarum capacitor are recommended.

CLC

The CLC pin sets the clamp circuit speed with an external capacitor and resistor.

Generally, the capacitor and resistor are arranged in a row and connected with GND(AD). Select a capacitor that minimizes the dielectric absorbing error. When the capacitor capacity is reduced, the shift speed of the video signal to $V_{CC(AD)}$ side is accelerated. If the resistor value is too small at this point, sagging will appear in the video signal. Also, if the capacitor's capacity is too large, the clamp speed will slow down; therefore, it is very important to pay attention to the setup of the resistor capacitor values.

DA Reference

REF(DA) is a DA converter reference decoupling pin for both the Y_{out} and C_{out}. Bypass to GND(DA) by applying a high–performance, high–frequency capacitor as close to the pin as possible. A 0.1 μF multilayer ceramic capacitor is recommended.

Clock Input

The clock frequency input is 3.58 MHz during normal (fsc) mode, and 14.31818 MHz during the other modes. The minimum input level is 1.0 Vp–p. It should be phase locked to the subcarrier of the video signal.

The clock line should be wired with the shortest wire and be separated from other circuits to minimize cross coupling to other signals. The CLK(AD) pin is used only during digital input comb filtering mode; therefore, it should be at GND level unless the device is used in the digital input comb filtering mode.

I_{bias}

The I_{bias} pin is used to set up the bias current for the AD and DA converters. Connect an external resistor between the I_{bias} and GND(DA).

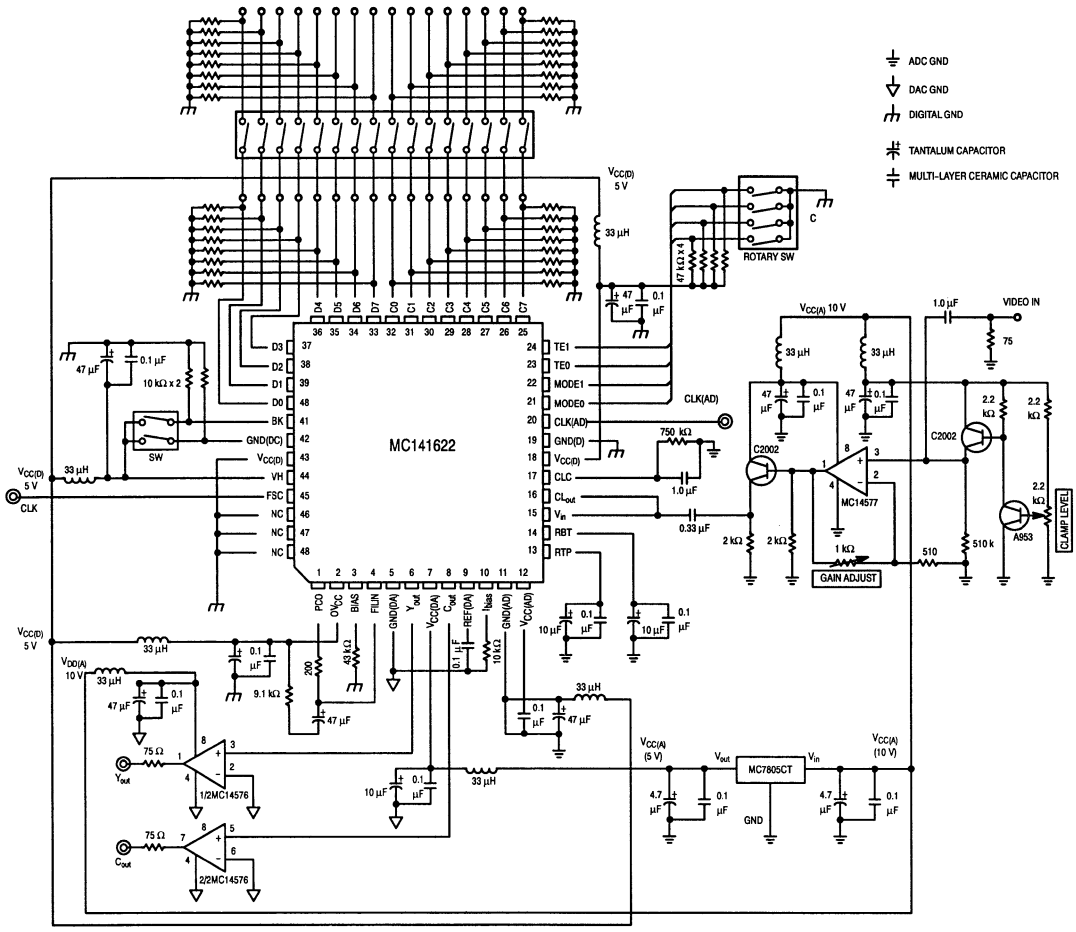
Digital Input Comb Filtering Mode

Connect CLK(AD) with the GND(D) when the AD converter is not being used. Connect D0 – D7 with GND(D), when the DA converter and filter are not being used. This is to eliminate any unnecessary operation of blocks which are not being used. At this point, make sure voltage is supplied to the $V_{CC(AD)}$, $V_{CC(DA)}$, and $V_{CC(D)}$. This eliminates latch–up during operating.

Latch–Up

The $V_{CC(AD)}$, $V_{CC(DA)}$, and $V_{CC(D)}$ pins connect to power supplies that are independent from each other. Therefore, latch–up may occur when the power is applied. To eliminate latch–up, apply power to $V_{CC(AD)}$, $V_{CC(DA)}$, and $V_{CC(D)}$ pins simultaneously.

APPLICATION CIRCUIT



EMI SUPPRESSION

When using ICs in or near television receiver circuits, EMI (electromagnetic interference) and subsequent unwanted display artifacts and distortion are probable unless adequate EMI suppression is implemented. A common misconception is that some offending digital device is the culprit. This is erroneous in that an IC itself has insufficient surface area to produce sufficient radiation. The device, while it is the generator of interfering signals, must be coupled to an antenna before EMI is radiated. The source for the EMI is not the IC which generates the offending signals but rather the circuitry which is attached to the IC.

2

Potential EMI signals are generated by ***all*** digital devices. Whether they become a nuisance is dependent upon their frequency and whether they have a sufficient antenna. The frequency and number of these signals is affected by both circuit design within the IC and the manufacturing process. Device speed is also a major contributor of potential EMI. because the design is determined by the anticipated application, the manufacturing process is fixed and the drive for speed ever increasing, the only effective point to implement EMI suppression is in the PC board design. The PC board usually is the antenna which radiates the EMI. The most efficient method of minimizing EMI radiation is to minimize the efficiency of this antenna.

The most common cause of inadequate EMI suppression lies with the ground system of the suspected digital devices. As pointed out previously, di/dt transitions can be significant in digital circuits. If the di/dt transitions appear in the ground system and the ground system is inductive, the harmonics present in these transitions are a source of potential EMI signals. The unfortunate result of putting digital devices on a reactive ground system is guaranteed EMI problems.

The area which should be addressed first as a potential EMI source is the ground. Without an adequate ground system, EMI cannot be effectively reduced by decoupling. If at all possible, the ground should be a complete unbroken plane. Figure 4 shows two examples of relieving ground around device pins. When relieving vias and plated through holes, large areas of ground loss should be avoided. When the relief pattern is equal to half the distance between pins, over etching and process errors may remove ground between pins. If sufficient ground around enough pins are removed, the ground system can become isolated or nearly isolated "patches" which will appear inductive. If ground, such as the vicinity of an IC, must be removed, replace with a cross hatch of ground lines with the mesh as small as possible.

If a single unbroken plane can be devoted to the ground system, EMI can usually be sufficiently suppressed by using ferrite beads on suspect EMI paths and decoupling with adequate values of capacitors. The value of the decoupling capacitor depends on the frequency and amplitude of the offending signals. Ferrite beads are available in a wide variety of shape, size and material to fit virtually any application.

Choose a ferrite bead for desired impedance at the desired frequency and construct a low pass filter using one or more appropriate capacitors in a "L", "T" or "PI" arrangement. Use only capacitors of low inductive and resistive properties such as ceramic or mica. Install filters in series with each IC pin suspected of contributing offending EMI signals and as close to the pin as possible. Analysis using a spectrum analyzer can help determine which pins are suspect.

Where PC board costs constrain the number of layers available, and if the EMI frequencies are far removed from the frequencies of operation, ferrite beads and decoupling capacitors may still be effective in reducing EMI emissions. Where only two (or in some cases, only one!) layer is used, the ground system is always reactive and poses an EMI problem. If the offending EMI and normal operating frequency differ sufficiently, filtering can still work.

An "island" is constructed in the ground system for the digital device using ferrite beads and decoupling capacitors as shown by the example in Figure 5. The ground must be cut so that the digital ground for the device is isolated from the rest of the ground system. Next choose a ferrite bead of the appropriate value. Install this bead between the isolated ground and the ground system. Install low pass filters in all suspect lines with the capacitor closest to the device pin connected to the isolated ground in all signal lines where EMI is suspect. Also cut the power to the device and insert a ferrite bead as shown in Figure 5. Finally, decouple the device between the power pin(s) and isolated ground pin(s) using a low inductive/resistive capacitor of adequate value.

The methods described above will work acceptably when the EMI frequency and the frequency of operation of the device generating the EMI differ greatly. Where the EMI is disturbing the high VHF or UHF channels and the device generating the EMI is operating within the NTSC/PAL bandwidth, the energy contained in the harmonics generating the EMI is situated well above the operating frequency and suppressing this type of EMI poses no great problem. However, if the EMI is present on low VHF channels and/or the operation of the device is outside the NTSC/PAL bandwidth, such as a 2X pixel clock or 4xfsc oscillator, compromise between video quality and suppression complexity is usually required to obtain an acceptable solution. For those cases where the operating frequency of the device is very near the frequency of the EMI disturbance, careful attention to PCB layout, multiple layer PCB and even shielding may be necessary to obtain an acceptable design.

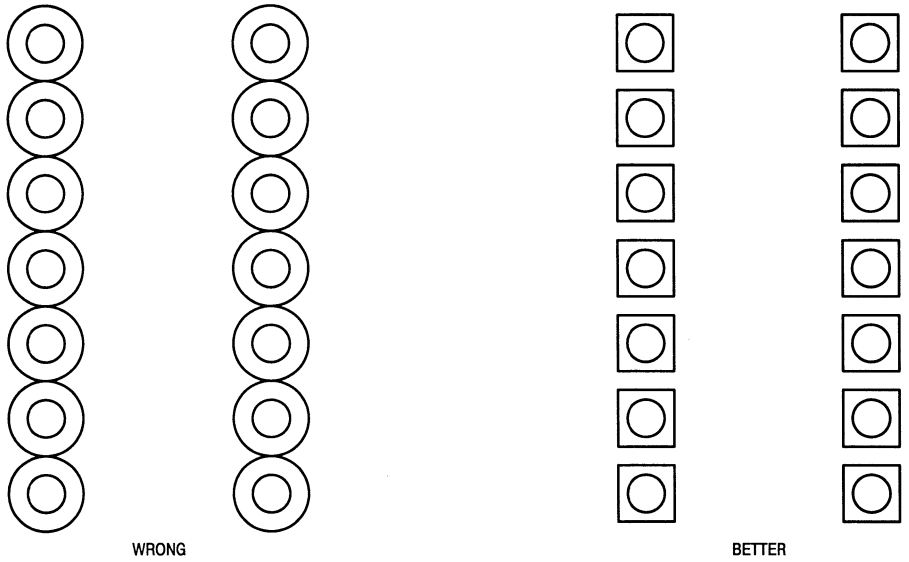


Figure 4.

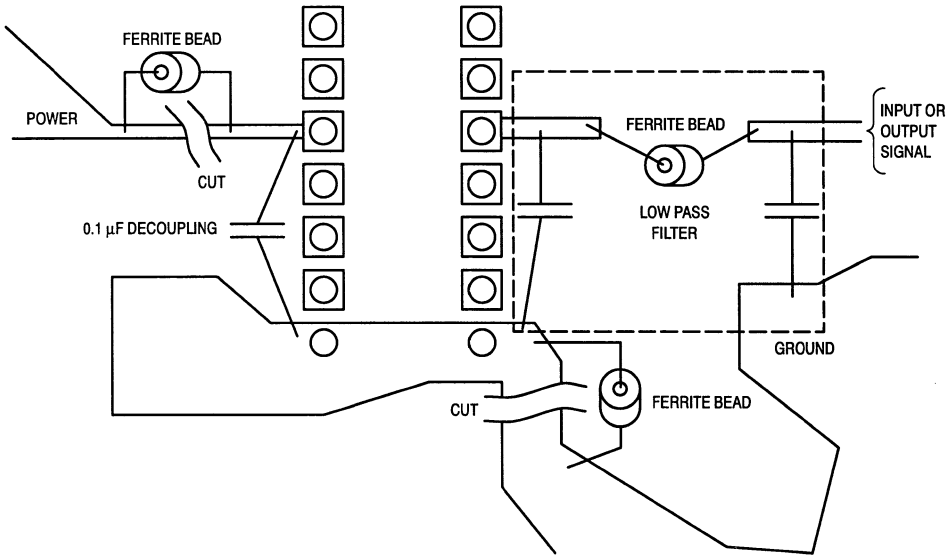


Figure 5.

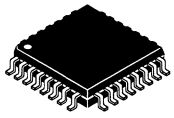
MC141624

Product Proposal

Advanced Comb Filter-I (ACF-I)

The Advanced Comb Filter–I is a video signal processor for VCRs and TVs. It's function is to separate the Luminance Y and Chrominance C signal from the NTSC composite signal. The ACF–I minimizes dot–crawl and cross–color. A built–in PLL provides a 4xfsc clock from either an NTSC subcarrier signal or a 4xfsc signal. This filter allows a video signal input of an extended frequency bandwidth by using a 4xfsc clock. The built–in A/D and D/A converters allow easy connection to analog video circuits.

- Built–In High Speed 8–Bit Two Step A/D Converter
- One Line Memories (910 Bytes)
- Advanced Comb–I Process
- Built–In Two High Speed 8–Bit D/A Converter
- Built–In 4xfsc PLL Circuit
- Built–In Clamp Circuit
- On–Chip Reference Voltage for A/D Converter



FU SUFFIX
32– LEAD QFP
CASE 873–01

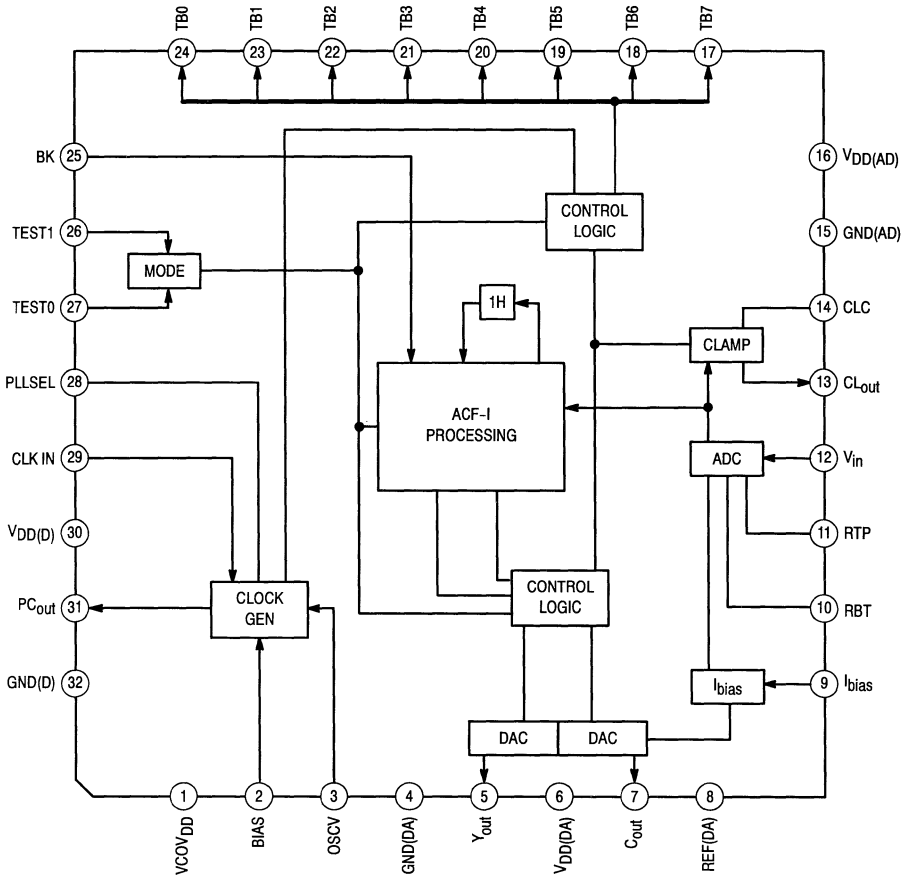
SP SUFFIX
32–LEAD SDIP
CASE TBD

ORDERING INFORMATION

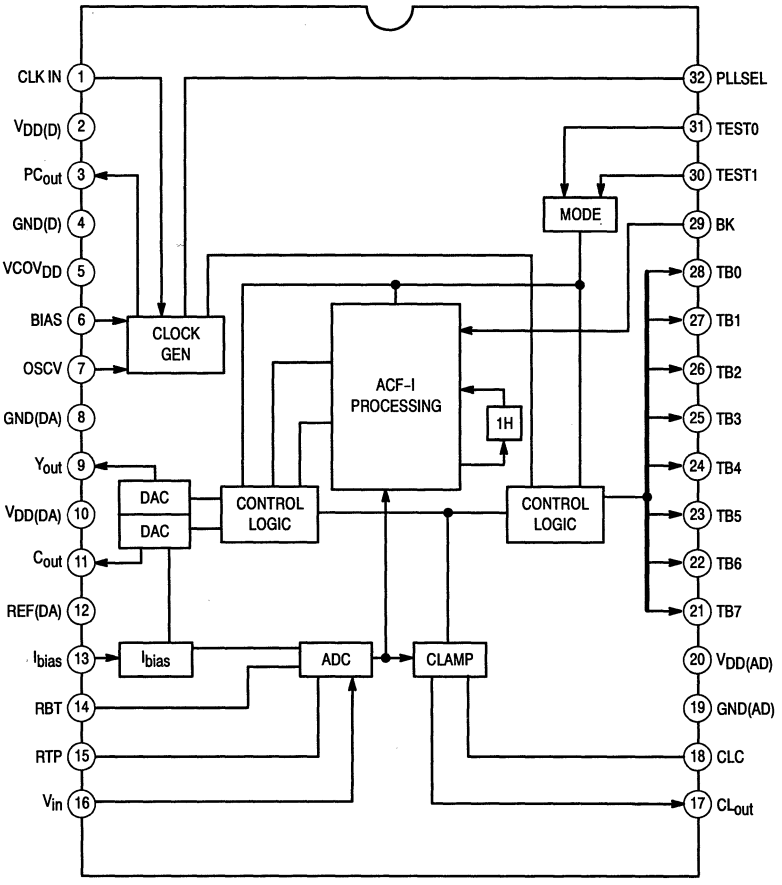
MC141624FU	Quad Flat Pack (QFP)
MC141624SP	SDIP

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM
(32 QFP)



BLOCK DIAGRAM
(32 SDIP)



ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Value	Unit
DC Supply Voltage (Referenced to GND)	V_{CC}	− 0.5 to + 6.0	V
DC Input Voltage (Referenced to GND)	V_{in}	− 1.5 to V_{CC} + 1.5	V
DC Output Voltage (Referenced to GND)	V_{out}	− 0.5 to V_{CC} + 0.5	V
DC Input Current (per pin)	I_{in}	± 20	mA
DC Output Current (per pin)	I_{out}	± 25	mA
Power Dissipation	P_D	500	mW
Storage Temperature	T_{stg}	− 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

GENERAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C, Unless Otherwise Noted)

Characteristic	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{CC}*	4.75	5.0	5.25	V	
Operating Supply Current (at Normal Mode)	I_{CC}	—	50	60	mA	
Operating Power Dissipation (at Normal Mode)	P_D	—	250	315	mW	
Ambient Operating Temperature	T_A	− 20	—	75	°C	

* $V_{CC(AD)}$, $V_{CC(DA)}$, $V_{CC(D)}$ voltage.

CLOCK INPUT ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C, Unless Otherwise Noted)

Characteristic		Symbol	Min	Typ	Max	Unit	Notes
Subcarrier Input Frequency		f_c	—	3.579545	—	MHz	1
Clock Frequency		CLK	—	14.31818	—	MHz	2
FSC Clock Input Level		V_{fc}	1	—	—	Vp-p	3
High Level Input Voltage	CLK	V_{ICH}	3.15	—	—	V	
Low Level Input Voltage	CLK	V_{ICL}	—	—	1.1	V	
Clock Duty Cycle	CLK	Dty	45	50	55	%	

NOTES:
1. Color subcarrier input [FSC = (455/2)fh] locked on the burst signal of the input video signal. AC coupling input by external capacitor.
2. The internal circuit operates by four times clock using FSC–pin input at normal (FSC) mode.
3. Sine wave input.

ADC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	—	—	—	8	Bits
Integral Nonlinearity	INL	—	± 1.0	± 1.5	LSB
Differential Nonlinearity	DNL	—	± 0.5	± 1.0	LSB
Top Reference Level	V_{TPS}	2.4	2.5	2.6	V
Bottom Reference Level	V_{BTS}	0.4	0.5	0.6	V
Maximum Analog Input Range During Self Reference	V_{ins}	1.9	2.0	2.1	Vp-p

DIGITAL ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic		Symbol	Min	Typ	Max	Unit
High Level Input Voltage	TE0, TE1, BK, TB0 – TB4	V_{IH}	3.15	—	—	V
Low Level Input Voltage	TE0, TE1, BK, TB0 – TB4	V_{IL}	—	—	1.1	V
Input Leakage Current [V_{in} = $V_{CC(D)}$ or GND(D)]	TE0, TE1, BK, TB0 – TB4	I_{inl}	—	—	± 10	µA

FILTERING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Y/C Separation	—	40	—	—	dB
Band-Pass Filter Bandwidth (at – 3 dB)	—	—	± 0.75	—	MHz

DAC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Resolution	—	—	—	8	Bits
Integral Nonlinearity	INL	—	—	± 1	LSB
Differential Nonlinearity	DNL	—	—	± 0.5	LSB
Analog Output Voltage, Y_{out}	V_{YO}	1.1	1.2	1.3	Vp-p
Analog Output Voltage, C_{out}	V_{CO}	1.1	1.2	1.3	Vp-p
Full Scale Voltage, Y_{out}	V_{YFS}	1.3	1.5	1.7	V
Full Scale Voltage, C_{out}	V_{CFS}	1.3	1.5	1.7	V
Zero Scale Voltage, Y_{out}	V_{YZS}	0.1	0.3	0.5	V
Zero Scale Voltage, C_{out}	V_{CZS}	0.1	0.3	0.5	V
Output Impedance	Z_O	—	100	300	Ω

ADC – DAC GENERAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Voltage Gain		—	– 4.4	—	dB
Output Bandwidth (at – 3 dB)		5.5	5.9	6.4	MHz
Differential Gain	DG	—	—	5	%
Differential Phase	DP	—	—	5	Deg
Bias Current (at I_{bias} = 10 kohm)	I_{bias}	—	135	—	µA

CLAMP CIRCUIT CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Clamp Mode Output Voltage*	V_{clys}	—	0.5	—	V

* At using the internal clamp circuit when connecting V_{in} – CL_{out}.

BK CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
BK Switching Time, at Normal Mode		—	349	—	ns

GENERAL SIGNAL DELAY (V_{CC} = 5.0 V, T_A = 25°C ± 3°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Normal Mode (24.5 Clock)		—	1.711	—	µs

PIN DESCRIPTIONS

Pin	Pin Name	Function
1	$VCOV_{CC}$	Power supply for VCO.
2	BIAS	Reference for VCO. Generally connected to GND(D) through an external resistor.
3	OSCV	VCO controlled voltage input. Generally connected to PCO through an external loop filter.
4	GND(AD)	GND for D/A converter.
5	Y_{out}	Luminance signal output.
6	$V_{DD(DA)}$	Power supply for D/A converter.
7	C_{out}	Chrominance signal output.
8	REF(DA)	Reference for D/A converter. Generally connected to GND(DA) through a multilayer ceramic capacitor (0.1 μF).
9	I_{bias}	Bias circuit current control for A/D, D/A converters. Generally connected to GND(DA) through an external resistor.
10	RBT	Bottom reference for A/D converter. Supplies bottom reference voltage internally.
11	RTP	Top reference for A/D converter. Supplies top reference voltage internally.
12	V_{in}	A/D converter input.
13	CL_{out}	Voltage output for clamp. Clamps an input signal by connecting with V_{in} and inputting the video signal by ac coupling.
14	CLC	Clamp time constant setting pin.
15	GND(AD)	GND for A/D converter.
16	$V_{CC(AD)}$	Power supply for A/D converter.
17 – 24	TB7 – TB0	Digital interface 1, input/output. Generally GND(D) level.
25	BK	Non–color signal processing mode. Generally GND(D) level.
26, 27	TEST1, TEST0	Test mode input. Generally GND level.
28	PLLSEL	CLK input mode select. PLLSEL "L": 4*PLL operation.
29	CLKIN	CLK input. ac coupling input by external capacitor. PLLSEL "L": subcarrier, PLLSEL "H": 4*subcarrier.
30	$V_{DD(D)}$	Power supply for digital circuit.
31	PC_{out}	Phase comparator output.
32	GND(D)	GND for digital circuit.

DEVICE DESCRIPTION

INTRODUCTION

The Advanced Comb Filter–I (ACF–I) is a high–performance HCMOS digital filter with built–in A/D and D/A converters. The basic function of the chip is the separation of the Luminance Y and Chrominance C signals from the NTSC composite video signal. The ACF–I minimizes the problems often generated by Y/C separation such as dot–crawl and cross–color. It uses a 14.3 MHz clock that allows an extended frequency bandwidth video signal to be input. This Y/C separation is realized by the digital advanced comb filters. The built–in 4xfsc PLL circuit allows a subcarrier signal input, from which a 4xfsc clock is generated for video signal processing. This arrangement allows a video signal input of an extended frequency bandwidth. The built–in A/D and D/A converters allow easy connection to analog video circuits.

DESCRIPTION

There are four major functions represented on the block diagram. The first block is the analog–to–digital conversion block. The high speed 8–bit binary A/D converter converts the incoming analog video signal to an 8–bit binary data stream. The conversion frequency is 14.3 MHz, which is four times the color subcarrier frequency. The maximum analog video input is 2.0 V p–p.

The fourth block is a 4xfsc CLK generator. The internal PLL can be phase locked to an external NTSC subcarrier to generate the necessary 4xfsc clock, or selected to process an externally supplied 4xfsc clock.

A/D Converter

The composite video signal input is converted to the digital code by the high speed 8–bit A/D converter. The input voltage range is determined by the value of the reference voltage inputs, RBT and RTP. This produces a maximum conversion value of 2.0 V p–p maximum video input signal for $V_{CC(AD)}$ of 5 V. A self–bias function generating V_{TP} = 2.5 V, V_{BT} = 0.5 V can be realized by connecting the internal A/D converter reference voltage supply with the A/D converter reference pin. The sampling clock frequency of the A/D converter is 14.3 MHz which is four times the color subcarrier frequency.

Clamp Voltage Regulating Circuit

The clamp voltage regulating circuit sync tip clamps the input signal when the V_{in} pin is connected to the CL_{out} pin and the video signal is input using ac coupling. It compares the digital value of the clamp level ($04) with the A/D converter output code. The clamp voltage is output by the CL_{out} pin.

Advanced Comb Filter–I

The Advanced Comb Filter–I is a digital comb filter developed for use in the NTSC system. The vertical correlation circuit provides high picture quality and high resolution and requires no adjustment for its Y/C separation. The clock frequency is 14.3 MHz, which is four times the NTSC subcarrier.

The BK pin is used to select as output either the filtered Y/C signal or the unfiltered composite signal. Table 1 shows the relationship of the BK pin to each output.

Table 1. BK Function

BK Pin	Y_{out}	C_{out}
L	Luminance	Chrominance
H	Composite	Chrominance

D/A Converter

The luminance and chrominance signals separated in the advanced comb filtering portion are converted to analog signals by two 8–bit D/A converters. The output voltage range is from 0.3 V to 1.5 V, 1.2 Vp–p. The sampling clock of the D/A converter is 14.3 MHz.

Clock Generation Circuit

The internal PLL can be selected to operate in either of two modes; an X4 mode used to generate a 4xfsc clock from a normal NTSC color subcarrier, and an X1 mode when a 4xfsc signal is available. An "L" applied to the PLLSEL pin sets the PLL to the X4 mode and an "H" sets it to the X1 mode.

APPLICATION DESIGN CONSIDERATIONS

V_{CC}, GND

To maximize the performance of the MC141624, noise should be kept to a minimum. Good printed circuit board design will enhance the operation of the MC141624. Separate analog and digital grounds will reduce noise and conversion errors. In addition, separate filters on analog V_{CC} and digital V_{DD} will also help to minimize noise and conversion errors. Sufficient decoupling and short leads will also improve performance.

When designing mixed analog/digital printed circuit boards, separate ground planes for digital ground and analog ground should be employed. Large switching currents generated by digital circuits will be amplified by analog circuitry and can quickly make a circuit unusable. Care should be taken to ensure analog ground does not inadvertently become part of the digital ground. The analog and digital grounds should be connected together at only one point. This is usually at or near where power enters the printed circuit board. Additionally, when interconnecting several printed circuit boards together, care must be taken to ensure that cabling does not interconnect digital and analog grounds together to produce a path for digital switching currents through analog ground.

When using any device with the performance and speed of the MC141624, ground planes are essential. Loosely interconnected traces and/or random areas of ground strewn around the printed circuit board are inadequate for high performance circuitry. While distribution of V_{DD} and V_{CC} can be done by bussing, to do so with the ground system is disastrous.

A CMOS device exhibits a characteristic input capacitance of about 10 pF. If this gate is driven by a digital signal that switches 2.5 V in a period of 5 ns, the equation for the average current flowing during the switching time will be:

$$I_{AV} = Cdv/dt.$$

A voltage change of 2.5 V in 5 ns requires an average current of 5 mA. If we assume a linear ramp starting from zero,

the total change in current will be 10 mA. The change in current per nanosecond per gate can be found by dividing the change in current by the time

$$10\ mA/5\ ns = 2\ mA/ns.$$

For a device with 16 outputs driving one gate for each output,

$$di/dt = 16 \times 2\ mA/ns = 32\ mA/ns.$$

If the above 1–inch wire is in this current path, then the voltage dropped across it can be found from the formula

$$V = Ldi/dt = 18\ nH \times 32\ mA/ns = 0.576\ V.$$

2

If the inductor is in the ground system, it is in the signal path. The voltage generated by the switching currents through this inductor will be added to the signal. At best it will be superimposed on the analog signal as unwanted noise. At worst, it can render the entire circuit unusable. Even the digital signal path is not immune to this type of signal. It can false trigger clock circuits causing timing errors, confuse comparator type circuits, and cause digital signals to be misinterpreted as wrong values.

When laying out the PCB, use electrolytic capacitors of sufficient size at the power input to the printed circuit board. 47 µF tantalum capacitors are recommended. Adding low ESR (effective series resistance) decoupling capacitors of about 0.1 µF capacitance across V_{CC} and/or V_{DD} at each device will help reduce noise in general and ESD (electrostatic discharge) susceptibility. Connect the high–capacity and high–frequency capacitors as close as possible to all analog V_{CC}, digital V_{DD}, and ground pins. Implementation of a good ground plane ground system can all but eliminate the type of noise described above.

To summarize, use sufficient electrolytic capacitor filtering, make separate ground planes for analog ground and digital ground, tie these grounds together at one and only one point, keep the ground planes as continuous and unbroken as possible, use low ESR capacitors of about 0.1 µF capacitance on V_{CC} and V_{DD} at each device, and keep all leads as short as possible.

V_{in}

In order to prevent flyback noise on the video input, it is necessary to keep the bandwidth to less than 1/2 the clock frequency by using an area filter. Here the amplifier used as an input buffer needs a wide bandwidth and driving capability. Moreover, to minimize external noise effects, drive the V_{in} pin with a low impedance amplifier and keep the V_{in} pin as close as possible to the amplifier output.

When using the built–in clamp circuit, connect CL_{out} to V_{in} and input signals after ac coupling by using a high–performance, high–frequency capacitor of 1 to 0.1 µF capacitance. In this case, keep the V_{in}, CL_{out}, coupling capacitor, and buffer–amplifier wiring as short as possible. Pay attention to the external noise and parasitic impedance.

AD Reference Pin

The RTP and RBT pins have a self–bias function that internally generates V_{TP} = 4.6 V and V_{BT} = 1.55 V. It acknowledges the AD converter analog input dynamic range. A stable performance can be achieved by applying a high–performance frequency capacitor as close as possible to the RTP and RBT pins and bypassing to GND(AD).

A 0.1 µF multi-layer ceramic capacitor and a 10 µF tantalum capacitor are recommended.

CLC

The CLC pin sets the clamp circuit speed with an external capacitor and resistor.

Generally, the capacitor and resistor are arranged in a row and connected with GND(AD). Select a capacitor which minimizes the dielectric absorbing error. When the capacitor capacity is reduced, the shift speed of the VCR signal to $V_{CC(AD)}$ side is accelerated. When the resistor value is reduced, the shift speed of the VCR signal to GND(AD) is accelerated. If the resistor value is too small at this point, sagging will appear in the VCR signal. Also, if the capacitor's capacity is too large, the clamp speed will slow down; therefore, it is very important to pay attention to the setup of the resistor value and capacity.

DA Reference

REF(DA) is a DA converter reference decoupling pin for both the Y_{out} and C_{out}. Bypass to GND(DA) by applying a high–performance frequency capacitor as close to the pin as possible.

A 0.1 µF multi ceramic capacitor is recommended.

Clock Input

The clock frequency input is 3.58 MHz during normal (fsc) mode, and 14.31818 MHz during the other modes. The minimum input level is 1.0 Vp–p. It should be synchronized with the input of the subcarrier of the video signal.

The clock line should be wired with the shortest wire and be separated from other circuits so it does not have an effect on other signals. The CLK(AD) pin is used only during digital input comb filtering mode; therefore, it should be at GND level except during the digital input comb filtering mode.

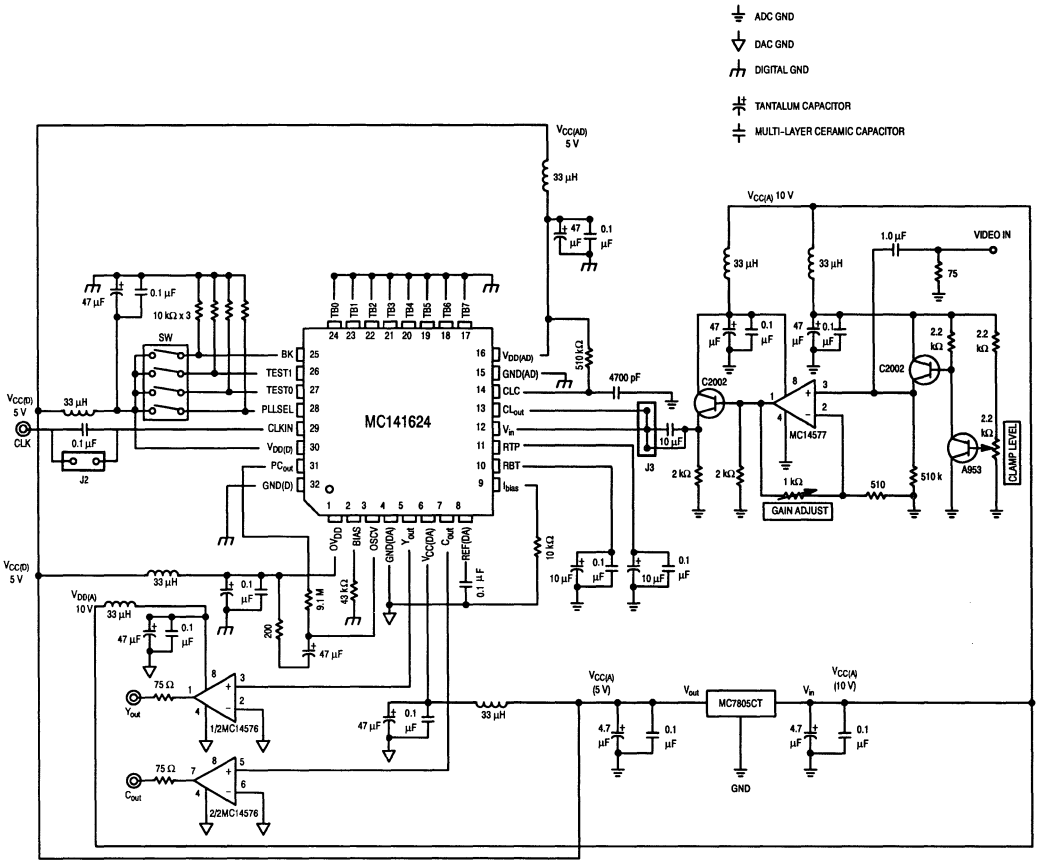
I_{bias}

The I_{bias} pin is used to set up the bias current for the AD and DA converters. Connect an external resistor between the I_{bias} and GND(DA).

Latch–Up

The $V_{CC(AD)}$, $V_{CC(DA)}$, and $V_{CC(D)}$ are power supplies, independent from each other. Therefore, latch–up may occur when the power is applied. To eliminate latch–up, apply power to $V_{CC(AD)}$, $V_{CC(DA)}$, and $V_{CC(D)}$ pins simultaneously.

APPLICATION CIRCUIT



EMI SUPPRESSION

When using ICs in or near television receiver circuits, EMI (electromagnetic interference) and subsequent unwanted display artifacts and distortion are probable unless adequate EMI suppression is implemented. A common misconception is that some offending digital device is the culprit. This is erroneous in that an IC itself has insufficient surface area to produce sufficient radiation. The device, while it is the generator of interfering signals, must be coupled to an antenna before EMI is radiated. The source for the EMI is not the IC which generates the offending signals but rather the circuitry which is attached to the IC.

Potential EMI signals are generated by ***all*** digital devices. Whether they become a nuisance is dependent upon their frequency and whether they have a sufficient antenna. The frequency and number of these signals is affected by both circuit design within the IC and the manufacturing process. Device speed is also a major contributor of potential EMI. because the design is determined by the anticipated application, the manufacturing process is fixed and the drive for speed ever increasing, the only effective point to implement EMI suppression is in the PC board design. The PC board usually is the antenna which radiates the EMI. The most efficient method of minimizing EMI radiation is to minimize the efficiency of this antenna.

The most common cause of inadequate EMI suppression lies with the ground system of the suspected digital devices. As pointed out previously, di/dt transitions can be significant in digital circuits. If the di/dt transitions appear in the ground system and the ground system is inductive, the harmonics present in these transitions are a source of potential EMI signals. The unfortunate result of putting digital devices on a reactive ground system is guaranteed EMI problems.

The area which should be addressed first as a potential EMI source is the ground. Without an adequate ground system, EMI cannot be effectively reduced by decoupling. If at all possible, the ground should be a complete unbroken plane. Figure 6 shows two examples of relieving ground around device pins. When relieving vias and plated through holes, large areas of ground loss should be avoided. When the relief pattern is equal to half the distance between pins, over etching and process errors may remove ground between pins. If sufficient ground around enough pins are removed, the ground system can become isolated or nearly isolated "patches" which will appear inductive. If ground, such as the vicinity of an IC, must be removed, replace with a cross hatch of ground lines with the mesh as small as possible.

If a single unbroken plane can be devoted to the ground system, EMI can usually be sufficiently suppressed by using ferrite beads on suspect EMI paths and decoupling with adequate values of capacitors. The value of the decoupling capacitor depends on the frequency and amplitude of the offending signals. Ferrite beads are available in a wide variety of shape, size and material to fit virtually any application.

Choose a ferrite bead for desired impedance at the desired frequency and construct a low pass filter using one or more appropriate capacitors in a "L", "T" or "PI" arrangement. Use only capacitors of low inductive and resistive properties such as ceramic or mica. Install filters in series with each IC pin suspected of contributing offending EMI signals and as close to the pin as possible. Analysis using a spectrum analyzer can help determine which pins are suspect.

Where PC board costs constrain the number of layers available, and if the EMI frequencies are far removed from the frequencies of operation, ferrite beads and decoupling capacitors may still be effective in reducing EMI emissions. Where only two (or in some cases, only one!) layer is used, the ground system is always reactive and poses an EMI problem. If the offending EMI and normal operating frequency differ sufficiently, filtering can still work.

An "island" is constructed in the ground system for the digital device using ferrite beads and decoupling capacitors as shown by the example in Figure 7. The ground must be cut so that the digital ground for the device is isolated from the rest of the ground system. Next choose a ferrite bead of the appropriate value. Install this bead between the isolated ground and the ground system. Install low pass filters in all suspect lines with the capacitor closest to the device pin connected to the isolated ground in all signal lines where EMI is suspect. Also cut the power to the device and insert a ferrite bead as shown in Figure 7. Finally, decouple the device between the power pin(s) and isolated ground pin(s) using a low inductive/resistive capacitor of adequate value.

The methods described above will work acceptably when the EMI frequency and the frequency of operation of the device generating the EMI differ greatly. Where the EMI is disturbing the high VHF or UHF channels and the device generating the EMI is operating within the NTSC/PAL bandwidth, the energy contained in the harmonics generating the EMI is situated well above the operating frequency and suppressing this type of EMI poses no great problem. However, if the EMI is present on low VHF channels and/or the operation of the device is outside the NTSC/PAL bandwidth, such as a 2X pixel clock or 4xfsc oscillator, compromise between video quality and suppression complexity is usually required to obtain an acceptable solution. For those cases where the operating frequency of the device is very near the frequency of the EMI disturbance, careful attention to PCB layout, multiple layer PCB and even shielding may be necessary to obtain an acceptable design.

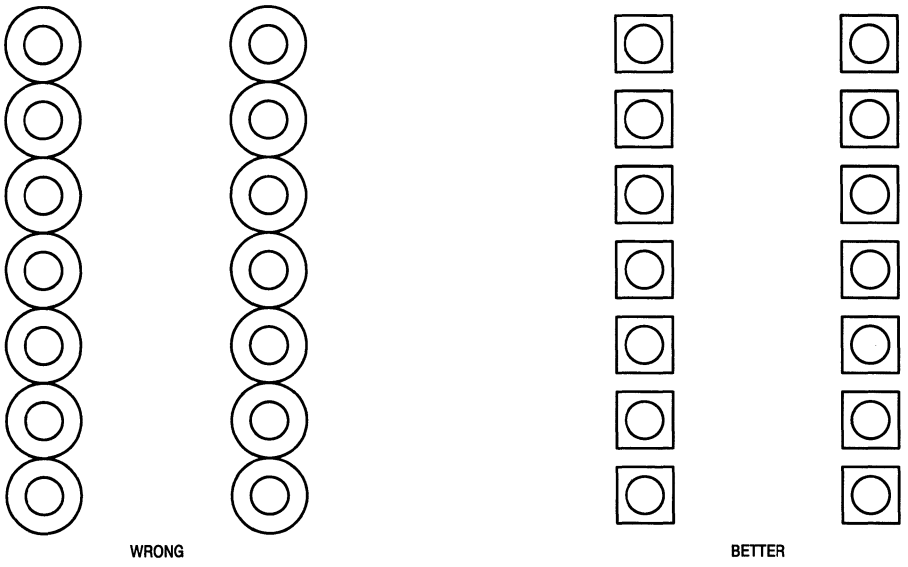


Figure 6.

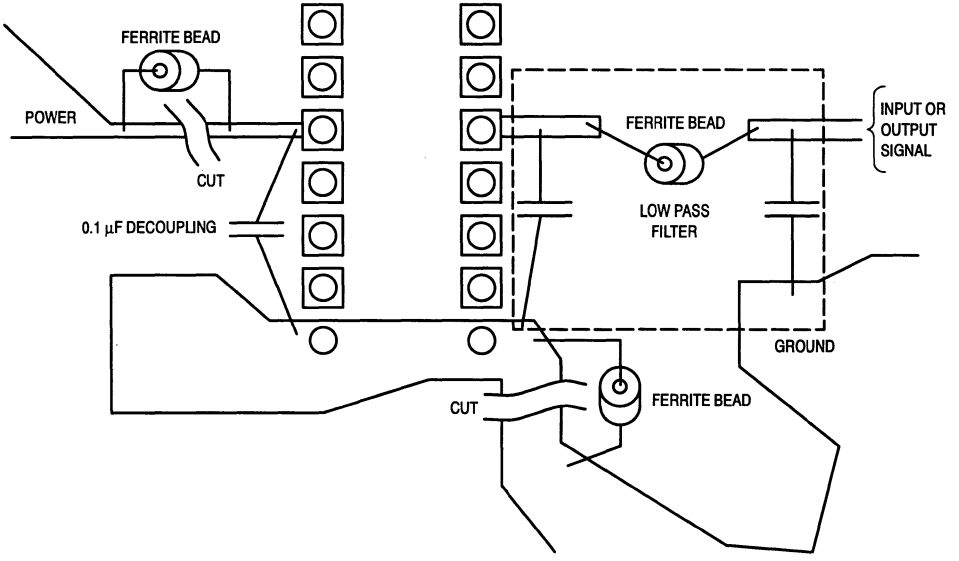


Figure 7.

MC144143

Advance Information

Closed-Caption Decoder

CMOS

2

The MC144143 is a line–21 closed–caption decoder for use in television receivers or set–top decoders conforming to the NTSC standard. Capability for processing and displaying all of the latest standard line–21 closed–caption format transmissions is included. The device requires a closed–caption encoded composite video signal, a horizontal sync signal, and an external keyer to produce captioned video. RGB outputs are provided, along with a luminance and a box signal, allowing simple interface to both color and black–and–white TV receivers.

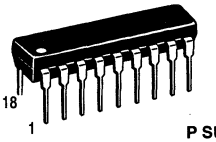
Display storage is accomplished with an on–chip RAM. A modified ASCII character set, which includes several non–English characters, is decoded by an on–chip ROM. An on–screen character appears as a white or colored dot matrix on a black background.

Captions (video–related information) can be up to four rows appearing anywhere on the screen and can be displayed in two modes: rollup or pop–on. With rollup captions, the row scrolls up and new information appears at the bottom row each time a carriage return is received. Pop–on captions work with two memories. One memory is displayed while the other is used to accumulate new data. A special command causes the information to be exchanged in the two memories, thus causing the entire caption to appear at once.

When text (non–video related information) is displayed, the rows contain a maximum of 32 characters over a black box which overwrites the screen. Eight rows of characters are displayed in the text mode.

An on–chip processor controls the manipulation of data for storage and display. Also controlled are the loading, addressing, and clearing of the display RAM. The processor transfers the data received to the RAM during scan lines 21 through 42. The operation of the display RAM, character ROM, and output logic circuits are controlled during scan lines 43 through 237. Several functions of the MC144143 are controlled via a port which may be configured to be serial or parallel.

- Conforms to FCC Report and Order as Amended by the Petition for Reconsideration on Gen. Doc. 91–1.
- Supports Four Different Data Channels, Time Multiplexed Within the Line–21 Data Stream: Captions Utilizing Languages 1 and 2 Plus Text Utilizing Languages 1 and 2
- Output Logic Provides Hardware Underline Control and Italics Slant Generation
- Single Supply, Operating Voltage Range: 4.75 to 5.25 V
- Supply Current: 20 mA (Preliminary)
- Operating Temperature Range: 0 to 70°C
- Composite Video Input Range: 0.7 to 1.4 V p–p
- Horizontal Input Polarity: Either Positive or Negative
- Internal Timing and Sync Signals Derived from On–Chip VCO

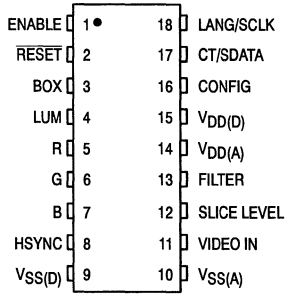


P SUFFIX
PLASTIC DIP
CASE 707–02

ORDERING INFORMATION

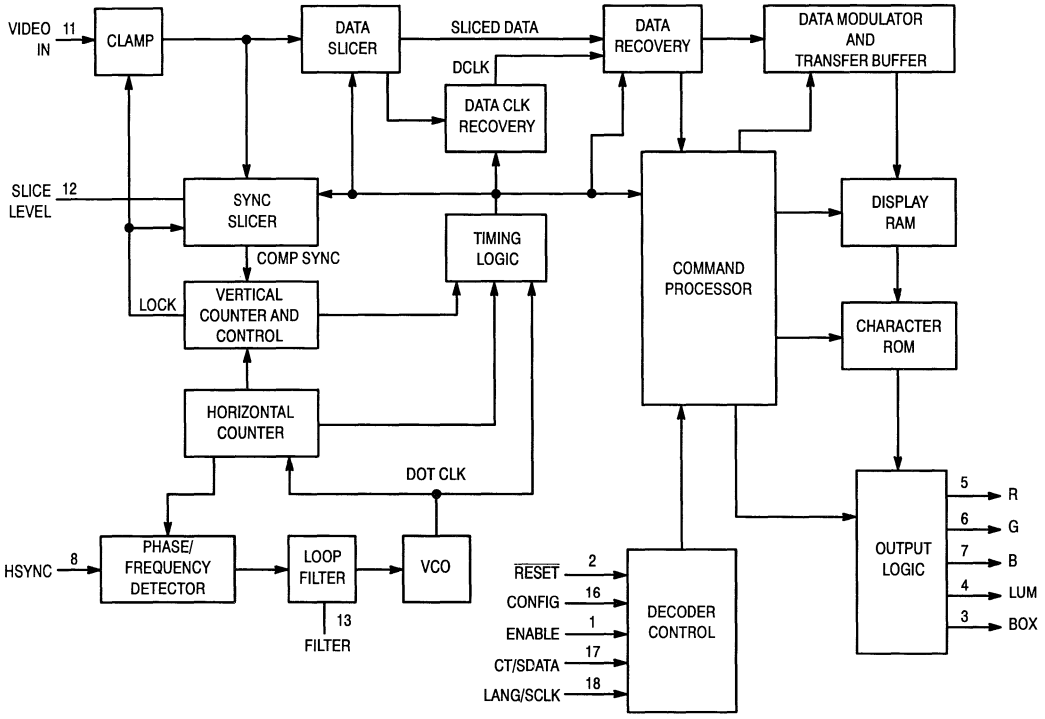
MC144143P	Plastic DIP

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



SUPPLY CONNECTIONS:
PIN 14 = $V_{DD(A)}$ = V+ FOR ANALOG SECTION
PIN 15 = $V_{DD(D)}$ = V+ FOR DIGITAL SECTION
PIN 10 = $V_{SS(A)}$ = GND FOR ANALOG SECTION
PIN 9 = $V_{SS(D)}$ = GND FOR DIGITAL SECTION

ABSOLUTE MAXIMUM RATINGS* (Voltages referenced to $V_{SS(A)}$ and $V_{SS(D)}$)

Symbol	Parameter	Value	Unit
$V_{DD(A)}$	Analog DC Supply Voltage	– 0.5 to 6.0	V
$V_{DD(D)}$	Digital DC Supply Voltage	– 0.5 to 6.0	V
V_{in}	DC Input Voltage, Analog Section	– 0.5 to $V_{DD(A)}$ + 0.5	V
V_{in}	DC Input Voltage, Digital Section	– 0.5 to $V_{DD(D)}$ + 0.5	V
V_{out}	DC Output Voltage, Digital Section	– 0.5 to $V_{DD(D)}$ + 0.5	V
I_{in}	DC Input Current, per Pin	+ 10	mA
I_{out}	DC Output Current, per Pin	+ 20	mA
I_{DD}	DC Supply Current	+ 30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

2

DC ELECTRICAL CHARACTERISTICS

($V_{DD(A)} = V_{DD(D)}$ = 4.75 to 5.25 V, T_A = 0 to 70°C, voltages referenced to $V_{SS(D)}$ unless otherwise indicated)

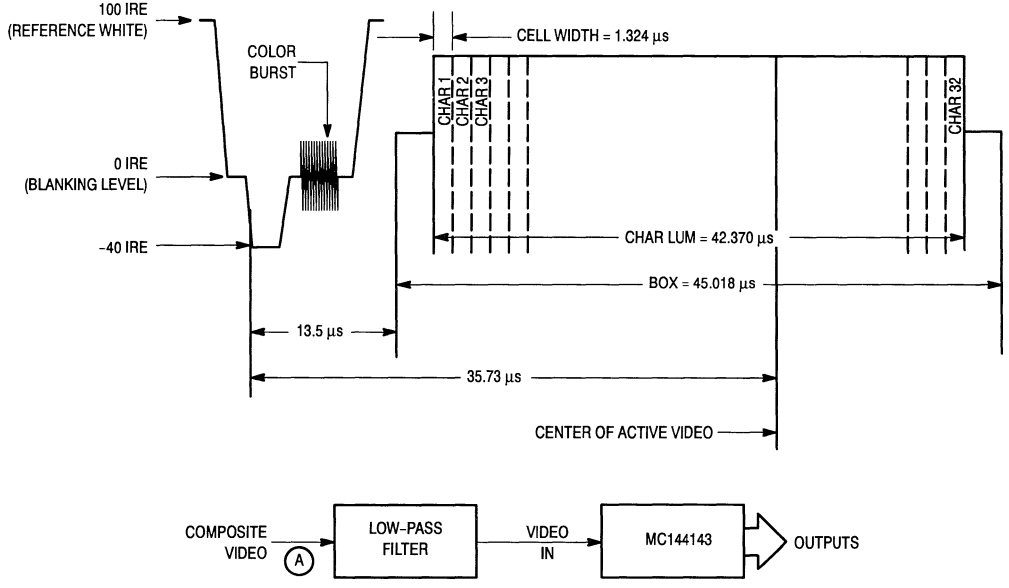
Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IH}	Minimum High–Level Input Voltage (HSync, Enable, CT/SData, Lang/SClk, Config, Reset)		0.7 x $V_{DD(D)}$	V
V_{IL}	Maximum Low–Level Input Voltage (HSync, Enable, CT/SData, Lang/SClk, Config, Reset)		0.2 x $V_{DD(D)}$	V
V_{OH}	Minimum High–Level Output Voltage (Box, Lum, R, G, B)	I_{out} = – 0.75 mA	$V_{DD(D)}$ – 0.4	V
V_{OL}	Maximum Low–Level Output Voltage (Box, Lum, R, G, B)	I_{out} = 1.0 mA	0.4	V
I_{in}	Maximum Input Leakage Current (HSync, Enable, CT/SData, Lang/SClk, Config, Reset)	$V_{in} = V_{SS(D)}$ or $V_{DD(D)}$	+ 3.0	mA
I_{DD}	Maximum Power Supply Current		*	mA

* The estimated value is 20 mA; this is not guaranteed.

VIDEO AC CHARACTERISTICS ($V_{DD(A)} = V_{DD(D)} = 4.75$ to 5.25 V, $T_A = 0$ to 70°C)

Symbol	Parameter	Guaranteed Limit	Unit
V_{in}	Input Sensitivity, Video In	1.0 V p–p + 3 dB	
BW	Bandwidth, Video In	600	kHz
SN	Signal–to–Random–Noise Ratio (CCIR Weighted), Video In (3 1 Error per Row)	25	dB
	Code Level at 1 V p–p, Video In (Note 1)	50 + 10	IRE
	Maximum Frequency Tolerance, HSync (Nominal Frequency = 15,734.263 Hz)	+ 3	%
t	Clock Run–In Start (Notes 1 and 2)	10.5 + 0.5	ms

NOTES:
1. Line 21 must be in the proper relative position to the leading edge of the vertical sync pulse.
2. Measured from the midpoint of the leading edge of HSync to the midpoint on the rising edge of the first clock run–in cycle.



NOTES:
1. Timing parameters derived from the *NAB Engineering Handbook*, 7th Edition, page 5.4–75.
2. Dot period = 82.76 ns.
3. An assumption is made that the delay through the low–pass filter is 220 ns. Therefore, the timing of the output signals is normally set so that the start of the leading box preceding the first displayable character cell occurs at 13.4 to 13.7 µs after the midpoint of the leading edge of the horizontal sync pulse at Point A. The 13.4 to 13.7 µs value may be altered via a mask option; contact your Motorola representative.

Figure 1. Timing of Output Signals Relative to Composite Video at Point A

SERIAL INTERFACE AC CHARACTERISTICS ($V_{DD(A)} = V_{DD(D)} = 4.75$ to 5.25 V, $T_A = 0$ to 70°C)

Symbol	Parameter	Guaranteed Limit	Unit
f_{clk}	Maximum Serial Data Clock Frequency (Also, refer to t_w) (Figure 2)	10	MHz
t_{su}	Minimum Setup Time, CT/SData to Lang/SClk (Figure 3)	75	ns
t_h	Minimum Hold Time, Lang/SClk to CT/SData (Figure 3)	25	ns
t_{su}	Minimum Setup Time, Enable to Lang/SClk (Figure 4)	175	ns
t_{su}	Minimum Setup Time, CT/SData to Enable (Figure 6)	100	ns
t_h	Minimum Hold Time, Enable to CT/SData (Figure 6)	100	ns
t_{rec}	Minimum Recovery Time, Enable to Lang/SClk (Figure 4)	100	ns
t_w	Minimum Pulse Width, Lang/SClk (Figure 2)	50	ns
C_{in}	Maximum Input Capacitance — CT/SData, Lang/SClk, Enable	10	pF

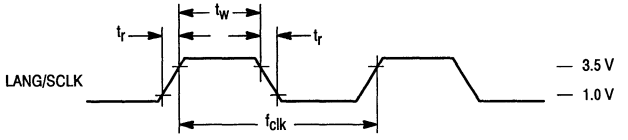


Figure 2.

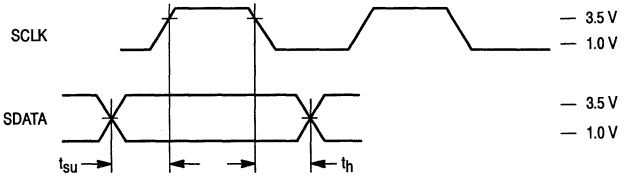


Figure 3.

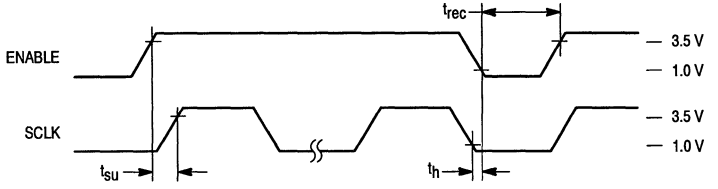


Figure 4.

OVERVIEW OF THE LINE–21 CLOSED CAPTION SYSTEM

THE LINE–21 CLOSED–CAPTIONING SYSTEM

The line–21 closed–captioning system provides for the transmission of caption information and other text material as an encoded composite data signal during the unblanked portion of line 21, field 1 of the standard NTSC video signal. In addition, a framing code is transmitted during the first half of line 21, field 2.

The encoded composite video signal for line 21, fields 1 and 2 is shown in Figure 5. The video signal conforms to the Standard Synchronizing Waveform for Color Transmission given in Sub–part E, Part 73 of the FCC Rules and Regulations.

Data Transmission Format

The composite data signal contained within the active portion of line 21 consists of a 7–cycle sine–wave clock run–in burst, a start bit, and 16 bits of data. These 16 bits consist of two 8–bit alphanumeric characters formulated according to the USA Standard Code for Information Interchange (USASCII;x3.4–1967) with odd parity. The clock rate is 0.5035 MHz which is 32 H. The clock burst and data packet are 50 IRE units peak–to–peak and are filtered to a "2T" response. Data is sent with the least significant bit (bit b1) being sent first and the most significant bit (bit b8, the parity bit) being sent last.

Multiplexed Data Channels

The line–21 closed–caption system defines four different data channels which can be time multiplexed within the Line 21 data stream. They are Captions — Language 1 (C1), Captions — Language 2 (C2), Text — Language 1 (T1), and Text — Language 2 (T2). Both languages may be English in either case.

Text (optional) is defined as non–video related information, so its display can fill the screen. In a full–screen text–mode display, a black box 8 rows high by 34 columns wide covers the screen. Text appears starting at the top with a maximum of 32 characters per row. When all 8 rows have been used, the display scrolls up as additional information is received. The MC144143 provides a reduced height text display mode showing 8 rows of text.

Captions are video–related information, so they are not permitted to overwrite the screen. Captions may be displayed anywhere on the screen. Up to four rows may be displayed at one time. All the rows in each caption appear at once, so this mode is called pop–on captions.

A secondary caption display, called *rollup captions*, is also provided. In this mode, caption information is displayed in any consecutive two, three, or four rows. Data appears in the base row and scrolls up as new information is received. The data scrolls off the top row selected, as in the *text* mode. Rollup captions are usually used for captioning unscripted and fast turnaround programming, such as talk shows and news.

DATA FORMAT

The four data channels are transmitted in line 21 as a time multiplexed data stream. The start of a particular channel's data stream is identified by the occurrence of one of its unique command codes. Once a unique command code is received, all subsequent data is considered to belong to that data channel until a unique command code is received for another data channel.

The 7–bit ASCII table defines two types of information: printing and non–printing. Printable data are data bytes having values between x0100000 ($20) and x1111111 ($7F), where x represents the parity bit. Data bytes having values between x0000000 ($00) and x0011111 ($1F) are called non–printing characters, because they have no displayable character font in the standard ASCII table.

Displayable Character Set

The specifications define a modified ASCII table character set where eight of the alpha–numeric characters have been changed to provide some non–English characters. Also, 15 additional characters are defined by special character commands. The changes in the ASCII table characters are shown in Table 1.

Table 1. Modifications to the ASCII Characters

Hex Code	ASCII Character	Line–21 Character
2A	*	á
5C	\	é
5E	^	í
5F	_	ó
60	`	ú
7B	{	ç
7D	}	Ñ
7E	~	ñ

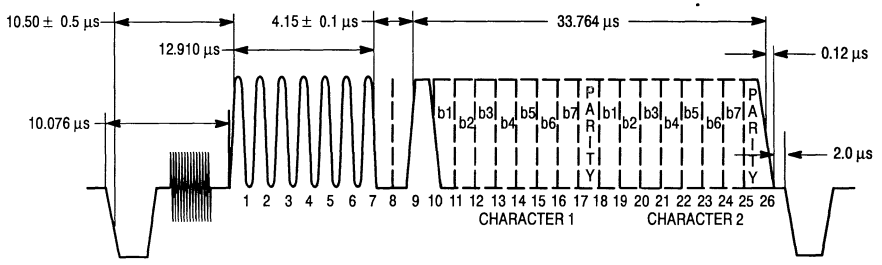


Figure 5. Encoded Composite Video Signal

Fifteen additional displayable characters are sent by transmitting a two–byte code. The sixteenth code provides a transparent space. The byte pair has a non–printing character followed by a printing character, where the non–printing character is $11 for Language 1 and $19 for Language 2. The printing character determines the special character font that is displayed according to Table 2.

Commands and Special Information

Data channel commands and special information are transmitted as two–byte pairs consisting of a non–printing character followed by a printing character. The two bytes of the pair must be transmitted in the same field, and the pair is transmitted twice in successive frames. This redundancy provides some immunity to noise errors for control information.

Throughout the line–21 system, bit 4 of the non–printing character identifies the language. Bit b4 = 0 signifies Language 1 commands and b4 = 1 signifies Language 2. The non–printing characters used in the line–21 system are $10 through $17 for Language 1 and $18 through $1F for Language 2.

Data Channel Commands

All the data channel command codes use the non–printing character $14 for Language 1 and $1C for Language 2. The printing character determines the particular command function. The commands are shown in Tables 3 through 6. The printing character is given by its hexadecimal value.

Data Location and Attribute Codes

Additional codes are used for positioning the data on the screen and for controlling the character attributes. There are two location attributes, row and column (tab or indent) position, and three character attributes, color, italics, and underline. All attribute information is contained in the preamble codes (precodes) and midrow codes (midcodes).

The precodes identify the display row and character attributes for the caption data that follows. These attributes hold for the entire line unless changed by a midcode or indent code. All the non–printing characters, $10 through $17 for Language 1 and $18 through $1F for Language 2 are used. The code pair assignment for the location and character attributes are given in Table 7.

The midcodes are used to change the character attributes in the middle of a caption row. The midcode occupies a space in the display. The characters following the midcode are displayed with the assigned attributes. The attributes hold until the end of the row, unless changed by another midcode. The indent codes listed in Table 6 actually perform in the same manner as a midcode.

The midcodes use the non–printing characters $11 and $19, respectively, for the two Languages. The printing character of the two–byte pair contains the character attributes as shown in Table 8. The printing character is given by its hexadecimal value.

Table 2. Additions to the ASCII Characters

Print	Character
30	®
31	°
32	1/2
33	¿
34	™
35	¢
36	£
37	"1/8 note" music symbol
38	à
39	"Transparent Space"
3A	è
3B	â
3C	ê
3D	î
3E	ô
3F	û

Table 3. Data Channel Commands — Captions (C1 or C2)

Print	Function
20	Resume Caption Loading (Off Screen)
25	Resume 2–Line Rollup
26	Resume 3–Line Rollup
27	Resume 4–Line Rollup
29	Resume Direct Loading (On Screen)
2C	Erase Displayed Memory
2E	Erase Non–Displayed Memory
2F	Show Caption (Flip Memories)

Table 4. Data Channel Commands — Text (T1 or T2)

Print	Function
2A	Start Text
2B	Resume Text

Table 5. Data Channel Commands — Captions or Text

Print	Function
21	Backspace
28	Flash On/Off
2D	New Line (Carriage Return)

Table 6. Data Channel Two–Byte Commands — Captions or Text

Command	Function
14 24	Delete to End of Row
17 21	Tab Offset 1 Column
17 22	Tab Offset 2 Columns
17 23	Tab Offset 3 Columns

Table 7. Code Pair Assignments for Location and Attributes

Non–print	11	11	12	12	15	15	16	16	17	17	10	13	13	14	14
CAPTION ROW	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ATTRIBUTE															
Monochrome	40	60	40	60	40	60	40	60	40	60	40	40	60	40	60
Mono Underline	41	61	41	61	41	61	41	61	41	61	41	41	61	41	61
Green	42	62	42	62	42	62	42	62	42	62	42	42	62	42	62
Green Underline	43	63	43	63	43	63	43	63	43	63	43	43	63	43	63
Blue	44	64	44	64	44	64	44	64	44	64	44	44	64	44	64
Blue Underline	45	65	45	65	45	65	45	65	45	65	45	45	65	45	65
Cyan	46	66	46	66	46	66	46	66	46	66	46	46	66	46	66
Cyan Underline	47	67	47	67	47	67	47	67	47	67	47	47	67	47	67
Red	48	68	48	68	48	68	48	68	48	68	48	48	68	48	68
Red Underline	49	69	49	69	49	69	49	69	49	69	49	49	69	49	69
Yellow	4A	6A	4A	6A	4A	6A	4A	6A	4A	6A	4A	4A	6A	4A	6A
Yellow Underline	4B	6B	4B	6B	4B	6B	4B	6B	4B	6B	4B	4B	6B	4B	6B
Magenta	4C	6C	4C	6C	4C	6C	4C	6C	4C	6C	4C	4C	6C	4C	6C
Magenta Underline	4D	6D	4D	6D	4D	6D	4D	6D	4D	6D	4D	4D	6D	4D	6D
Italics (mono)	4E	6E	4E	6E	4E	6E	4E	6E	4E	6E	4E	4E	6E	4E	6E
Italics Underline	4F	6F	4F	6F	4F	6F	4F	6F	4F	6F	4F	4F	6F	4F	6F
Indent 0 (mono)	50	70	50	70	50	70	50	70	50	70	50	50	70	50	70
Indent 0 Underline	51	71	51	71	51	71	51	71	51	71	51	51	71	51	71
Indent 4	52	72	52	72	52	72	52	72	52	72	52	52	72	52	72
Indent 4 Underline	53	73	53	73	53	73	53	73	53	73	53	53	73	53	73
Indent 8	54	74	54	74	54	74	54	74	54	74	54	54	74	54	74
Indent 8 Underline	55	75	55	75	55	75	55	75	55	75	55	55	75	55	75
Indent 12	56	76	56	76	56	76	56	76	56	76	56	56	76	56	76
Indent 12 Underline	57	77	57	77	57	77	57	77	57	77	57	57	77	57	77
Indent 16	58	78	58	78	58	78	58	78	58	78	58	58	78	58	78
Indent 16 Underline	59	79	59	79	59	79	59	79	59	79	59	59	79	59	79
Indent 20	5A	7A	5A	7A	5A	7A	5A	7A	5A	7A	5A	5A	7A	5A	7A
Indent 20 Underline	5B	7B	5B	7B	5B	7B	5B	7B	5B	7B	5B	5B	7B	5B	7B
Indent 24	5C	7C	5C	7C	5C	7C	5C	7C	5C	7C	5C	5C	7C	5C	7C
Indent 24 Underline	5D	7D	5D	7D	5D	7D	5D	7D	5D	7D	5D	5D	7D	5D	7D
Indent 28	5E	7E	5E	7E	5E	7E	5E	7E	5E	7E	5E	5E	7E	5E	7E
Indent 28 Underline	5F	7F	5F	7F	5F	7F	5F	7F	5F	7F	5F	5F	7F	5F	7F

Table 8. Midcode Assignment

Print	Character Attribute
20	Monochrome
21	Monochrome Underlined
22	Green
23	Green Underlined
24	Blue
25	Blue Underlined
26	Cyan
27	Cyan Underlined
28	Red
29	Red Underlined
2A	Yellow
2B	Yellow Underlined
2C	Magenta
2D	Magenta Underlined
2E	Italics
2F	Italics Underlined

OPERATING CHARACTERISTICS

DISPLAY FORMAT

Characters are displayed as white or colored, dot–matrix characters on a black background. The characters are described by a 6–by–9 dot pattern within a character cell which is 8 dots wide by 13 dots high. This provides a one–dot border of black around each character and provision for one row for underline, offset by a row of black, between the character and the bottom edge of the cell. Character luminance has normally been set at 90 IRE units and the surrounding black box at 10 IRE units.

2

The Character ROM contains a 12–18 ***dot–matrix*** pattern of each character. Each ***dot*** from the character ROM represents a single picture element or 'pixel' and each picture 'dot' is made up of a square of four pixels. Pixels 1 and 2 are generated during field one and pixels 3 and 4 during field two. Alternate rows and columns are read out of each field to produce an interleaved and rounded character. A display row contains a maximum of 32 characters plus a leading and trailing blank box, each a character cell in width, making the overall width of a display row 34 x 8 = 272 dots. Successive display rows are butted together, so that the total display is 195 dots high.

The black box (34 character cells wide by 195 dots high) results in a box size of 45.018 ms in width by 195 TV scan lines in height. A scan line is two adjacent picture lines. The first line is generated during field 1 and the second line is generated during field 2. When centered in the video display, this box starts 13.5 ms after the leading edge of H in scan line 43 and extends to scan line 237. This places the display approximately within the safe title area for NTSC receivers. Character width is 42.37 ms and is approximately centered on the screen, resulting in a leading and trailing 1.32 ms black border.

Text Mode Display

When text mode, in either language, has been selected (and valid line 21 code has been detected in the incoming video), an 8–row by 34–character black box appears. Received text characters are displayed as they are received starting in the top row. Successive carriage returns (new line command) move the display down successive rows until 8 display rows have been used. Thereafter, the text scrolls up as new characters are added to the bottom row.

If the data for the selected channel is interrupted by a command for another channel, data processing stops but the display remains. When a *resume text* command is received, data processing resumes and the new characters are added starting at the position that the display row/column pointer was in at the interruption of data processing. If a *start text* command is received, the display is cleared and new characters are displayed starting in the top row, column 1 (left side).

When scrolling, the display shifts one scan line per frame until a complete row has been scrolled. If a carriage return is received before scrolling is complete, the display immediately completes the "scroll" by jumping up the remaining scan lines and starts displaying the new text.

There are never any transparent boxes in the text display.

Caption Mode Display

When caption mode, in either language, has been selected, the screen is transparent (display box disappears). Caption data can appear in any of the 15 display rows, but a single caption may consist of no more than 4 rows. If more than four rows are received, the last four are displayed. The form of the caption display depends on the caption mode indicated by the transmitted caption command, pop–on, paint–on, or rollup.

Pop–on captions work with two caption memories. One of them is always being displayed while the other is being used to accumulate new caption data. A new caption is popped–on by swapping the two memories (the show caption command). When the on–screen memory is erased, the screen is blank (transparent) and the memory defaults to the row/column pointer at row 1, column 1 and monochrome non–underlined.

When caption mode is selected, the decoder processes any data following the resume caption loading (RCL) command (or the show caption command). Normally, this command is followed by a precode to indicate the row, column, and character attributes to be used with the following data. If no precode is received, the data is added to the location last indicated by the row/column pointer prior to the receipt of the RCL command with the character attributes previously assigned.

Paint–on caption mode is essentially equivalent to the pop–on mode except that the data received after the resume direct loading (RDL) command is written to the on–screen memory rather than the off–screen memory. All the rules for precodes, midcodes, etc. are otherwise the same.

Rollup caption mode presents a text–like display that is limited to 2, 3, or 4 rows depending on the resume rollup (RRn) command used. The precode following the RRn command is used to indicate the base row for the rollup display. The base row is the bottom row for the rollup display. In this case, the black box does not appear until characters are being displayed and the box is only wide enough to provide a leading and trailing box in each line. The new data appears in the bottom row, and as each carriage return is received, the row scrolls up and the new data is added to the bottom. When the number of rows indicated by the resume command has been reached, the data in the top row scrolls off as new data is added to the bottom.

The tab (indent) precode permits placing captions starting at four character boundaries. The tab offset command provides the means for adjusting the starting position for a caption at any column position.

Display Erase and Autoblanking

The display is erased in the text mode by the *start text* command (but the box is maintained) and in the caption mode by the *erase displayed memory* command. The non–displayed memory can be erased by the *erase non–displayed memory* command.

Four other events can also cause the display to be erased. First, changing the data channel to be processed by switching between captions and text or between languages 1 and 2 clears the memory and hence the display. Second, if the autoblanking circuit is activated by the loss of valid code, then the display is turned off and the memory cleared. Third, the memory and display are cleared when loss of vertical lock is detected, which normally occurs on a change of channel. Last, in the caption mode only, if no valid caption command in the selected language is received for a 16–second period, the on–screen memory is erased.

The autoblanking circuit maintains the status of the presence of valid data. The decoder is held in the decoder off

(TV) state until valid data is continuously detected for a period of 0.5 second. Once the valid data decision has been made, and assuming that the user has enabled the outputs, the normal display for the data channel selected is presented.

The autoblanking circuit does not activate again until valid data has been lost for 1.5 seconds. Any valid data received during the 1.5 second period resets the counter so that autoblanking activates only on continuous loss of data for 1.5 seconds.

Decoder Control Interface

The device allows either of two control modes: parallel or serial. The parallel mode permits the control of the decoder functions by means of simple switch selections on the three control inputs. In the serial control mode, these three pins are configured to allow a serial stream. The decoder's functions are controlled by clocking in a data word via this serial port.

VIDEO INPUT SIGNAL PROCESSING

The composite video input is ac coupled to the IC where the sync tip is internally clamped to a fixed reference voltage. Initially, the signal is clamped using a simple clamp, but improved impulse noise performance is achieved once the internal sync circuits lock to the incoming signal. Noise rejection is obtained by making the clamp operative only during the sync tip. The clamped composite video signal is fed to both the data slicer and sync slicer blocks. An external capacitor stores the slice level.

The data slicer generates a clean CMOS–level data signal by slicing the signal at its midpoint. The slice level is established on an adaptive basis during line 21 of the odd field. The resultant value is stored until the next odd field line 21 begins. A high level of noise immunity is achieved by using this process.

The data clock recovery circuit produces a 32 H clock signal Data Clock (DClk) that is locked in phase to the sliced clock run–in burst obtained from the data slicer. The dot clock is locked in phase with HSync but the DClk phase is not determined until the occurrence of line 21 data. When line 21 code appears, DClk phase lock is achieved during the clock run–in burst and used to reclock the sliced data. Once phase lock is established, it is maintained until a change in video signal occurs.

TIMING AND SYNCHRONIZING CIRCUITS

All internal timing and synchronizing signals are derived from the on board 12.083 MHz VCO. Its output is the Dot Clk signal used to drive the horizontal and vertical counter chains and for display timing.

The horizontal counter is a divide–by–768 circuit with intermediate outputs needed to generate the timing logic signals used in data recovery and data output (display). It produces pulse signals at H, 2 H, 32 H and 48 H rates as well as the horizontal square wave, Q768, that is used to phase lock the VCO.

The vertical counter and control circuits produce a noise free vertical pulse by dividing the horizontal signal in a 525 counter. The internal synchronizing signals are phased up with the incoming video by comparing the internally generated vertical pulse to an input vertical pulse derived from the comp sync signal provided by the sync slicer. When proper phasing has been established, this circuit outputs the lock signal which is used to provide additional noise immunity to the slicing circuits.

The locked state is established only after several successive fields have occurred in which these two vertical pulses remain in sync. Once locked, the internal timing flywheels until such time as the two vertical pulses lose coincidence for a number of consecutive fields. Until lock is established, the decoder operates on a pulse–by–pulse basis.

The internal sync circuits lock to all 525 line signals having a vertical sync pulse that meets all of the following conditions: (1) the pulse is at least 2.5 H long, (2) the pulse starts at the proper 2 H boundary for its field, and (3) if equalizing pulse serrations are present, they must be less than 0.125 H in width.

DATA RECOVERY

The data recovery circuits perform the initial processing of the data in line 21. The sliced data is reclocked using Clk and the reclocked data stream is checked for the presence of valid data. When valid data is present, the two bytes are clocked into the serial/parallel register and output in parallel form.

This block checks the bytes for valid (odd) parity, and determines whether the recovered byte pair is a repeat of the previously received byte pair. That information is used with the redundancy flag in the command processor to determine whether the command should be executed or not.

COMMAND PROCESSOR

The command processor controls the manipulation of the data for storage and display. This processor decodes the three control inputs to determine the display status desired and the data channel selected. This information is then used to perform its most important function, the control of the loading, addressing, and clearing of the display RAM.

During data recovery time (TV lines 21–42), the command processor transfers only the data received for the data channel selected to the RAM for storage and display. In those cases such as special characters, midcodes, parity errors, etc. where the data stored or action to be taken is different from the specific bytes received, the command processor converts the input data to the appropriate form.

During the display time (lines 43–237), the command processor controls the operations of the display RAM, character ROM, and output logic circuits.

MEMORY AND DISPLAY CIRCUITS

These circuits operate together to generate the output color signals R, G, B and the monochrome signals Luminance and Box. The character ROM contains the dot pattern for all the characters, but not the underline characteristic. The output logic provides the hardware underline control circuits and the italics slant generator. The smooth scroll display control is also performed in the output logic block.

DECODER CONTROL CIRCUIT

The control circuit block converts the signals provided at the three control pins into internal control signals required to establish the operating mode of the device. The Config pin determines whether the port in is parallel or serial mode.

In parallel mode (pin 16 Config pin = high), the three control pins 1, 17, 18 perform the decoder control functions of Decoder On/Off, Caption/Text select and Lang1/Lang2 select respectively.

In serial mode (pin 16 Config pin = low), the control pins 1, 17, 18 perform the functions Enable, Serial Data, and Serial Clock. Each control word consists of 8 data bits, D0–D7, and a status bit A0. In the serial mode, two registers are accessible for software control of the decoder. These are the Control register and the Shift register. The bit definitions for these registers are given in Table 9.

Table 9. Input Data Bit Assignment for Serial Mode

Bit	Control Register	Shift Register
D0	Must Be Low	Must Be Low
D1	Output Enable	Language Select: Low = 2, High = 1
D2	Must Be Low	CT Select: Low = Text, High = Captions
D3	Must Be Low	Must Be Low
D4	Must Be Low	Must Be Low
D5	Must Be Low	Must Be Low
D6	Reset Processor	Must Be Low
D7	Chip Reset	Must Be Low
A0	Must Be Low	Flag (serial status)

NOTE: Operation of Field 2 (even field of line 21) is the same as Field 1 (odd field of line 21)

The Control register is used to enable the outputs (Decoder On/Off) and to reset the MC144143. To write to the Control register, A0 and all serial data bits marked low must be set to 0. To reset the MC144143, clock in the data with Bits D6 and D7 set to 1. Then clock in the data with D6 and D7 set to 0. To enable the outputs, clock in data with Bit D1 set to 1, and all other bits set to 0. To disable the outputs, clock in data with all bits set to 0.

The Shift register is used to control the Data Channel and field to be processed by the decoder. To write to the Shift register, A0 must be set to 0, and all serial data bits marked low must be set to 0. The D1 and D2 bits are then used to control the Language 1 or 2 and Captions or Text selection. The D3 bit controls the field selection. All other bits must be set to 0. Bit D1=1 sets the language select bit to Language 2. Bit D2=1 enables the outputs to recover Captions and D2=0 enables Text recovery.

PIN DESCRIPTIONS

INPUTS

Video In
Composite NTSC Video Input (Pin 11)

This pin should be driven by an emitter follower through a 0.1 mF capacitor. The signal must be band limited to 600 kHz; a single–pole, low–pass filter may be used, as shown in Figure 7. The input level must be a nominal value of 1 V p–p. The polarity is sync tips negative.

HSync
Horizontal Sync Input (Pin 8)

This signal pulls the on–chip dot–clock VCO within the proper range. The circuit uses the frequency of HSync, not the phase. Therefore, any polarity may be used. This signal must be at CMOS voltage levels, and is usually derived from the H flyback pulse. The MC144143 requires that the HSync signal be continuous.

Reset
Active–Low Master Reset (Pin 2)

When this pin is taken to a low CMOS logic level (0), the device is reset when in the parallel mode (Config = high). Pin 2 may be tied high when in the serial mode (Config = low) if reset is to be performed through the serial port. To assure a valid reset, care should be taken to make sure reset does not occur until the V_{DD} power supply has fully ramped up. If an RC reset circuit is used, the time constant of RC should be made greater than the time for V_{DD} to ramp up.

Config
Configure Input for the Control Port (Pin 16)

When this input is at a high CMOS logic level (1), the port is configured in the parallel mode and control must be provided in parallel. When low, control must be provided as a serial stream.

Enable
(Pin 1)

Parallel Mode: Decoder Display Control Input. When this pin is at a high CMOS logic level (1), the outputs are enabled. When this pin is at a low CMOS logic level (0), the R, G, B, Luminance, and Box outputs are disabled, but incoming data is still processed. The disabled output state is an inactive (low) level.

Serial Mode: Active–High Enable Input. This pin controls the serial port. When the Enable pin is low, the serial interface is disabled and the SData pin is in the high–impedance state. On the low–to–high transition of Enable, the state of the flag is output on the bidirectional SData pin. The Enable pin must remain high for the duration of the data transfer. After the data stream is sent, this pin must be returned to the low logic level. See Figure 6.

CT/SData
(Pin 17)

Parallel Mode: Captions or Text Data–Channel Selector Input. When this pin is at a high CMOS logic level (1), captions are processed. A low CMOS logic level (0) causes text to be processed.

Serial Mode: Serial Data Input/Output. See Figure 6. Note that on the low–to–high transition of Enable, the bidirectional SData pin is an output. Then, on the first high–to–low transition of SClk, the SData pin becomes an input. The serial input data stream consists of eight data bits (D0 through D7) and one address bit (A0). Bit A0 determines whether the eight data bits remain in the shift register or whether the bits are transferred into a control register. If A0 is low, the contents of the input shift register are transferred to a control register when the Enable pin is brought low. If A0 is high, the bits remain in the shift register, and a flag is set. This flag indicates to the command processor that the shift register should be serviced. After servicing is performed, the command processor clears the flag. Reference Table 9.

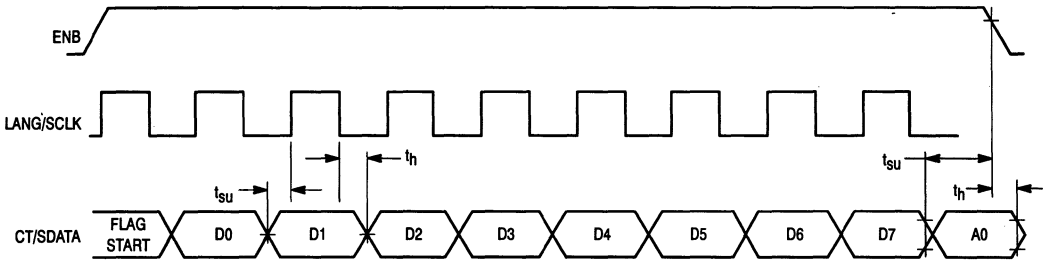


Figure 6. Timing Diagram for Serial Mode (Config = Low)

Lang/SClk
(Pin 18)

Parallel Mode: Language Data–Channel Selector Input. When this pin is at a high CMOS logic level (1), language 1 is processed. A low CMOS logic level (0) causes language 2 to be processed.

Serial Mode: Serial Clock Input. Nine clock cycles are required for each serial transfer. Data is shifted in on the low–to–high transition of SClk. See Figure 6.

OUTPUTS

Box
Black Box Keying Output (Pin 3)

This digital output is at CMOS levels and is active high. The black box keying signal for the captions/text display area is used for both color and monochrome (black and white) television.

Lum
Character Video Luminance Output (Pin 4)

This digital output is at CMOS levels and is active high. This signal determines the character brightness and is used for monochrome (black and white) television, only. If unused, this pin must be floated.

R, G, B
Red, Green, and Blue Video Outputs (Pins 5, 6, 7)

These digital outputs are at CMOS logic levels and are active high. These character video signals are for color television only. If unused, these pins must be floated.

EXTERNAL COMPONENTS

Slice Level
Sink Slice Level (Pin 12)

A 0.1 mF capacitor must be tied between this pin and analog ground, $V_{SS(A)}$. The capacitor is used to store the sync slice level voltage.

Filter
Loop Filter (Pin 13)

A low–pass filter consisting of a series resistor–capacitor of 5 kW and 0.082 mF must be tied between this pin and analog ground $V_{SS(A)}$. This filter must be shunted with a 2200 pF capacitor. This network is used to integrate the output of the on–chip phase/frequency detector which feeds the on–chip VCO.

POWER SUPPLY

$V_{DD(A)}$
Most Positive Supply Potential (Pin 14)

Most Positive Supply Potential for the analog section of the device. The voltage on this pin may range from + 4.75 to + 5.25 V with respect to the V_{SS} pins. For optimum performance, $V_{DD(A)}$ should be bypassed to $V_{SS(A)}$ using a low–inductance capacitor mounted very close to these pins.

$V_{DD(D)}$
Most Positive Supply Potential (Pin 15)

Most Positive Supply Potential for the digital portion of the device. The voltage on this pin may range from + 4.75 to + 5.25 V with respect to the V_{SS} pins. For optimum performance, $V_{DD(D)}$ should be bypassed to $V_{SS(D)}$ using a low–inductance capacitor mounted very close to these pins.

$V_{SS(A)}$
Most Negative Supply Potential (Pin 10)

Most Negative Supply Potential for the analog section of the device. This pin must be tied to ground.

$V_{SS(D)}$
Most Negative Supply Potential (Pin 9)

Most Negative Supply Potential for the digital section of the device. This pin must be tied to ground.

APPLICATIONS INFORMATION

PCB DESIGN

To maximize the performance of the MC144143, noise should be kept to a minimum. Good printed circuit board design will enhance the operation of the MC144143. Separate analog and digital grounds will reduce noise and decoding errors. In addition, separate filters on $V_{DD(A)}$ and $V_{DD(D)}$ will also help to minimize noise and decoding errors. Sufficient decoupling and short leads will also improve performance.

When designing mixed analog/digital printed circuit boards, separate ground planes for digital ground and analog ground should be employed. Large switching currents generated by digital circuits will be amplified by analog circuitry and can quickly make a circuit unusable. Digital oscillators can become a source of EMI (electromagnetic interference) problems. Care should be taken to ensure analog ground does not inadvertently become part of the digital ground. The analog and digital grounds should be connected together at only one point. This should be the $V_{DD(A)}$ and $V_{DD(D)}$ pins on the MC144143 if possible. Additionally, when interconnecting several printed circuit boards together, care must be taken to ensure cabling does not interconnect digital and analog grounds together to produce a path for digital switching currents through analog ground.

When using any device that combines digital and analog circuitry, such as the MC144143, ground planes are desirable. Loosely interconnected traces and/or random areas of ground strewn around the printed circuit board are inadequate for high performance circuitry. While distribution of $V_{DD(A)}$ and $V_{DD(D)}$ can be done by bussing, to do so with the ground system is disastrous. Stray ground inductance can increase radiation and make EMI suppression very difficult.

A 1–inch long conductor is an 18 nH inductor. The cross sectional area of the conductor affects the exact value of the inductance, but for most PCB traces this is approximately correct. If the ground system is composed of traces or clumps of ground loosely interconnected, it will be inductive. The amount of inductance will be proportional to the length of the conductors making up the ground. This inductance cannot be decoupled away. It must be designed out.

A CMOS device exhibits a characteristic input capacitance of about 10 pF. If this gate is driven by a digital signal that switches 2.5 V in a period of 5 ns, the equation for the average current flowing during the switching time will be:

$$I_{AV} = Cdv/dt.$$

A voltage change of 2.5 V in 5 ns requires an average current of 5 mA. If we assume a linear ramp starting from zero, the total change in current will be 10 mA. The change in current per nanosecond per gate can be found by dividing the change in current by the time

$$10 \text{ mA}/5 \text{ ns} = 2 \text{ mA/ns}.$$

For a device with outputs driving one gate for each output,

$$di/dt = 16 \times 2 \text{ mA/ns} = 32 \text{ mA/ns}.$$

If the above 1–inch wire is in this current path, then the voltage dropped across it can be found from the formula

$$v = Ldi/dt = 18 \text{ nH} \times 32 \text{ mA/ns} = 0.576 \text{ V}.$$

If the inductor is in the ground system, it is in the signal path. The voltage generated by the switching currents through this inductor will be added to the signal. At best it will be superimposed on the analog signal as unwanted noise. At worst, it can render the entire circuit unusable. Even the digital signal path is not immune to this type of signal. It can false trigger clock circuits causing timing errors, confuse comparator type circuits, and cause digital signals to be misinterpreted as wrong values.

When laying out the PCB, use electrolytic capacitors of sufficient size at the power input to the printed circuit board. Adding low ESR (effective series resistance) decoupling capacitors of about 0.1 mF capacitance between $V_{DD(A)}$ and ground and $V_{DD(D)}$ and ground at the device power pins will help reduce noise in general, and also reduce EMI and ESD (electrostatic discharge) susceptibility. Implementation of a good ground plane ground system can all but eliminate the type of noise described above.

To summarize, use sufficient electrolytic capacitor filtering, make separate ground planes for analog ground and digital ground, tie these grounds together at one and only one point, keep the ground planes as continuous and unbroken as possible, use low ESR capacitors of about 0.1 mF capacitance on $V_{DD(A)}$ and $V_{DD(D)}$ at each device, and keep all leads as short as possible.

EMI SUPPRESSION

When using ICs in or near television receiver circuits, EMI (electromagnetic interference) and subsequent unwanted display artifacts and distortion are probable unless adequate EMI suppression is implemented. A common misconception is that some offending digital device is the culprit. This is erroneous in that an IC itself has insufficient surface area to produce sufficient radiation. The device, while it is the generator of interfering signals, must be coupled to an antenna before EMI is radiated. The source for the EMI is not the IC which generates the offending signals but rather the circuitry which is attached to the IC.

Potential EMI signals are generated by ***all*** digital devices. Whether they become a nuisance is dependent upon their frequency and whether they have a sufficient antenna. The frequency and number of these signals is affected by both circuit design within the IC and the manufacturing process. Device speed is also a major contributor of potential EMI. because the design is determined by the anticipated application, the manufacturing process is fixed and the drive for speed ever increasing, the only effective point to implement EMI suppression is in the PC board design. The PC board usually is the antenna which radiates the EMI. The most efficient method of minimizing EMI radiation is to minimize the efficiency of this antenna.

The most common cause of inadequate EMI suppression lies with the ground system of the suspected digital devices. As pointed out previously, di/dt transitions can be significant in digital circuits. If the di/dt transitions appear in the ground system and the ground system is inductive, the harmonics present in these transitions are a source of potential EMI signals. The unfortunate result of putting digital devices on a reactive ground system is guaranteed EMI problems.

The area which should be addressed first as a potential EMI source is the ground. Without an adequate ground system, EMI cannot be effectively reduced by decoupling. If at all possible, the ground should be a complete unbroken plane. Figure 7 shows two examples of relieving ground around device pins. When relieving vias and plated through holes, large areas of ground loss should be avoided. When the relief pattern is equal to half the distance between pins, over etching and process errors may remove ground be-

tween pins. If sufficient ground around enough pins are removed, the ground system can become isolated or nearly isolated "patches" which will appear inductive. If ground, such as the vicinity of an IC, must be removed, replace with a cross hatch of ground lines with the mesh as small as possible.

If a single unbroken plane can be devoted to the ground system, EMI can usually be sufficiently suppressed by using ferrite beads on suspect EMI paths and decoupling with adequate values of capacitors. The value of the decoupling capacitor depends on the frequency and amplitude of the offending signals. Ferrite beads are available in a wide variety of shape, size and material to fit virtually any application.

Choose a ferrite bead for desired impedance at the desired frequency and construct a low pass filter using one or more appropriate capacitors in a "L", "T" or "PI" arrangement. Use only capacitors of low inductive and resistive properties such as ceramic or mica. Install filters in series with each IC pin suspected of contributing offending EMI signals and as close to the pin as possible. Analysis using a spectrum analyzer can help determine which pins are suspect.

Where PC board costs constrain the number of layers available, and if the EMI frequencies are far removed from the frequencies of operation, ferrite beads and decoupling capacitors may still be effective in reducing EMI emissions. Where only two (or in some cases, only one!) layer is used, the ground system is always reactive and poses an EMI problem. If the offending EMI and normal operating frequency differ sufficiently, filtering can still work.

An "island" is constructed in the ground system for the digital device using ferrite beads and decoupling capacitors as shown by the example in Figure 8. The ground must be cut so that the digital ground for the device is isolated from the rest of the ground system. Next choose a ferrite bead of the appropriate value. Install this bead between the isolated ground and the ground system. Install low pass filters in all suspect lines with the capacitor closest to the device pin connected to the isolated ground in all signal lines where EMI is suspect. Also cut the power to the device and insert a ferrite bead as shown in Figure 8. Finally, decouple the device between the power pin(s) and isolated ground pin(s) using a low inductive/resistive capacitor of adequate value.

The methods described above will work acceptably when the EMI frequency and the frequency of operation of the device generating the EMI differ greatly. Where the EMI is disturbing the high VHF or UHF channels and the device generating the EMI is operating within the NTSC/PAL bandwidth, the energy contained in the harmonics generating the EMI is situated well above the operating frequency and suppressing this type of EMI poses no great problem. However, if the EMI is present on low VHF channels and/or the operation of the device is outside the NTSC/PAL bandwidth, such as a 2X pixel clock or 4xfsc oscillator, compromise between video quality and suppression complexity is usually required to obtain an acceptable solution. For those cases where the operating frequency of the device is very near the frequency of the EMI disturbance, careful attention to PCB layout, multiple layer PCB and even shielding may be necessary to obtain an acceptable design.

APPLICATIONS CIRCUIT

Figure 9 shows a typical decoder circuit using a parallel configuration of the input port. The video output is monochromatic using the Luminance pin as an output. Video switching control is obtained from the Box pin output. Similar techniques can be employed when using the RGB outputs.

The Video Buffers shown can be of any typical design. A gain of one is needed with sufficiently low impedance to drive the video input to the MC144143 and the video switch. The input impedance for the video switch is dependent on the design of the Video Line Driver and the input impedance for the MC144143 should be considered as 470 ohms. In either case an MC14576C or MC14577C can be used to construct the buffer, or if proper low impedance design is employed, a discrete transistor buffer amplifier can be used. When using ac coupling, dc restoration is necessary for the video buffers. This can be a simple RC network or a more complicated implementation depending on the needs of the application.

An MC14576C or MC14577C is recommended for the Video Line Driver. These devices are low impedance operational amplifiers capable of driving 150 ohms, giving them the capability of driving a doubly terminated 75 ohm transmission line.

The video switch is a fast CMOS analog switch capable of switching on a per–pixel basis. An MC74HC4053 or MC74HC4066 can be used for video switching. If a single–pole, single–throw switch such as the MC74HC4066 is used, then an inverter is necessary for constructing the double–throw operation necessary for the video switch. This can be a common CMOS inverter. If a single–pole, double–throw analog switch such as the MC74HC4053 is used, an inverter is unnecessary.

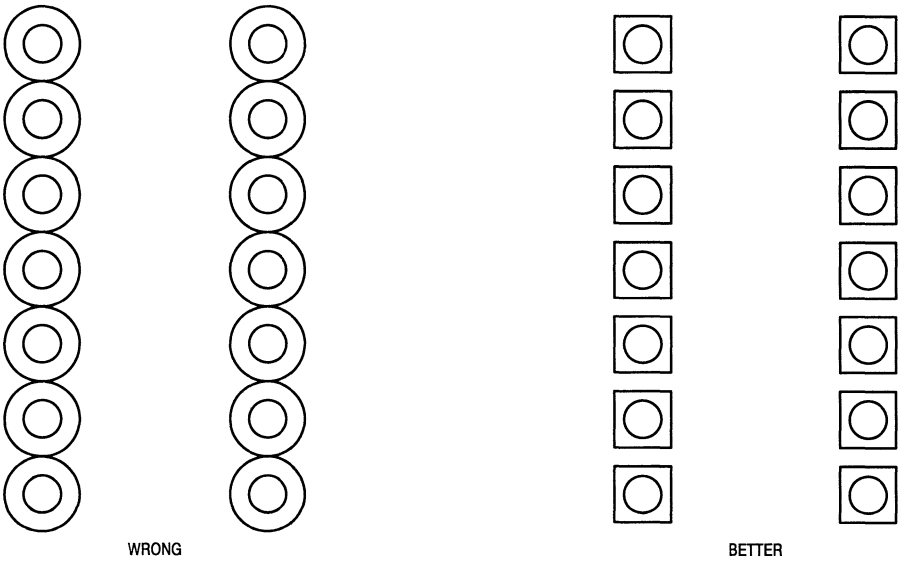


Figure 7.

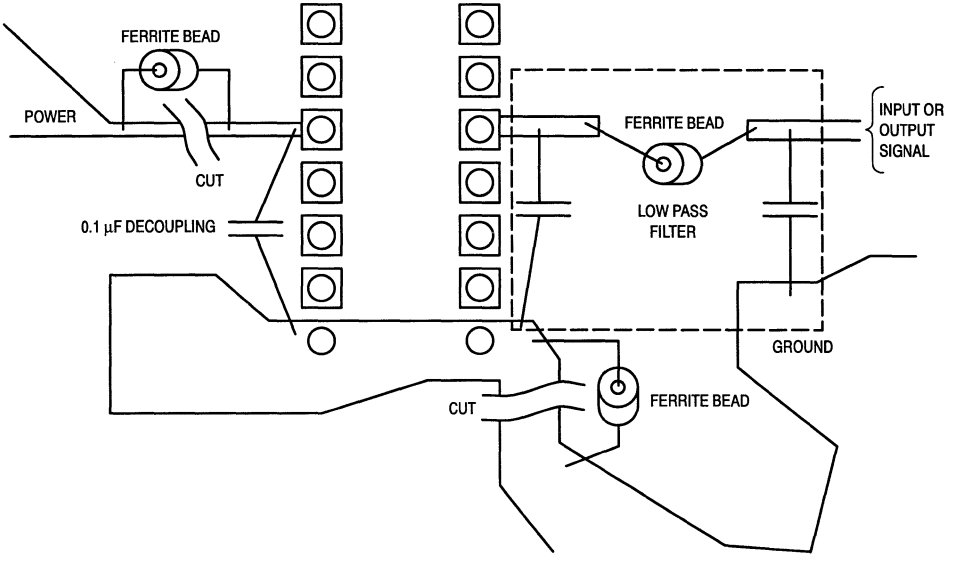
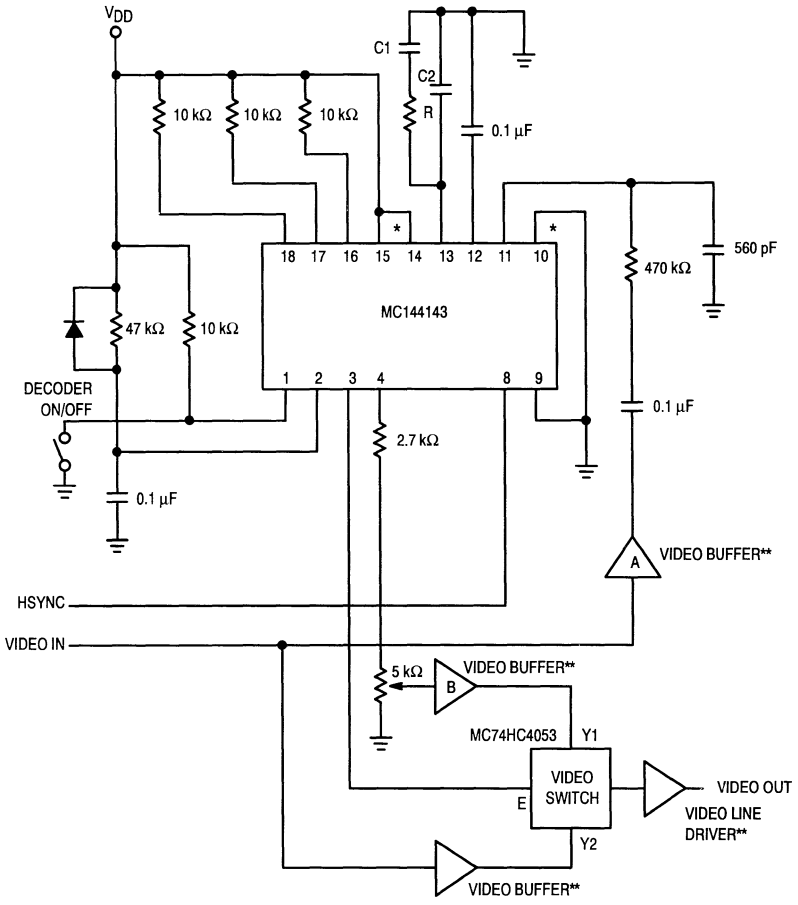


Figure 8.



* Decouple V_{DD} to V_{SS} with 0.1 µF low ESR capacitors between pins 14 – 15 and 9 – 10 keeping leads as short as possible.
** MC14576C or MC14577C.

Figure 9. Typical Decoder Circuit

LOOP FILTER CALCULATION

This section is not intended as complete loop theory; its aim is merely to point out the peculiarities of the loop, and provide the user with enough information for the filter components selection. For a more in–depth covering, the cited references should be consulted, especially [1].

The following remarks apply to the loop:

- The loop frequency is 15 kHz.
- In spite of the sampled nature of the loop, a continuous time approximation is possible if the loop bandwidth is sufficiently small.
- Ripple on Vc is a function of loop bandwidth.
- The loop is a type ||, 3rd order; however, since C2 is small, the pole it creates is far removed from the low frequency dominant poles, and the loop can be analyzed as a 2nd order loop.

These remarks apply to the PFD:

- Phase and frequency sensitive.
- Independent of duty cycle.
- PFD has 3 allowed states: up, down, high–Z.
- The VCO is always pulled in the right direction (during acquisition).
- PFD gain is higher near lock.

The last two remarks imply that only the higher value need be taken into account, as acquisition will be slower, but always in the proper direction, whereas the higher gain will enter into the action as soon as the error reaches $\pm 2\pi$.

The following values are selected and defined:

C2 = C/10 or less, to satisfy the requirement that the effect of C2 on the low frequency response of the loop be minimal, and similar to a second order loop.

$\zeta = 0.707$ for the damping factor.

$i = 15625 \bullet 2\pi$ the input pulsation.

$\tau = RC$ as the loop filter.

$K = Ko \bullet Ip \bullet R/(2 \bullet \pi \bullet N)$ the loop gain.

$K' = K \bullet \tau = 4\,\zeta^2$ is the 'normalized' loop gain.

$Ko = 49 \bullet 10^6$ [rad/Vs] (7.8 MHz/V).

Stability analysis, with C2 $\leq$ C/10 and $K' = 2$ (= 0.707) gives a minimum value of 7.5 for the ration /K and to have some margin, a reasonable value can be 15 to 20 or higher [1].

Selecting $i/K = 20$, gives: $K = i/20 \approx 5000$.

With $K' = 2$, $\tau = 2/K = 400\ \mu s$.

Using $K = Ko \bullet Ip \bullet R/(2 \bullet \pi \bullet N)$ and setting $Ip = 120\ \mu A$, and N an average value of 1000, we get $R = 5.1\ k\Omega$.

Then for $\tau = 400\ \mu s$, C becomes 82 nF and C2, 3.3 nF for C2 = C/25.

With these values, the loop natural frequency (n) and the loop bandwidth (3 dB) can be calculated:

$n = [(Ko/N) \bullet Ip/(2\pi C)]^{1/2} = 3400$ and $fn = 3400/2\pi = 540$ Hz.

3 dB = $2 \bullet n = 1080$ Hz (valid if ζ is close to 0.707).

REFERENCES

[1] "Charge–Pump Phase–Lock Loops", Floyd M. Gardner, *IEEE Transactions on Communications*, Vol. Com–28, No. 11, November 1980.

[2] *Phaselock Techniques*, Floyd M. Gardner, J. Wiley & Sons, 1979.

[3] *Phase–Locked Loops*, Roland E. Best, McGraw–Hill, 1984.

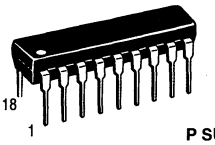
[4] "Phase Locked Loop Systems", Motorola.

MC144144

Advance Information

Enhanced Closed-Caption Decoder

CMOS

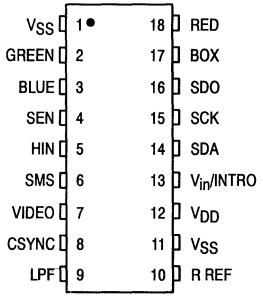


P SUFFIX
PLASTIC DIP
CASE 707–02

ORDERING INFORMATION

MC144144P Plastic DIP

PIN ASSIGNMENT



The MC144144 is a line–21 closed–caption decoder for use in television receivers or set–top decoders conforming to the NTSC standard. Capability for processing and displaying all of the latest standard line–21 closed–caption format transmissions is included. The device requires a closed–caption encoded composite video signal, a horizontal sync signal, and an external keyer to produce captioned video. RGB and box signal outputs are provided, which along with the mode select, allow simple interfacing to either color or black–and–white TV receivers.

Display storage is accomplished with an on–chip RAM. A modified ASCII character set, which includes several non–English characters, is decoded by an on–chip ROM. An on–screen character appears as a white or colored dot matrix on a black background.

Captions (video–related information) can be up to four rows appearing anywhere on the screen and can be displayed in two modes: rollup or pop–on. With rollup captions, the row scrolls up and new information appears at the bottom row each time a carriage return is received. Pop–on captions work with two memories. One memory is displayed while the other is used to accumulate new data. A special command causes the information to be exchanged in the two memories, thus causing the entire caption to appear at once.

When text (non–video related information) is displayed, the rows contain a maximum of 32 characters over a black box which overwrites the screen. Eight rows of characters are displayed in the text mode.

An on–chip processor controls the manipulation of data for storage and display. Also controlled are the loading, addressing, and clearing of the display RAM. The processor transfers the data received to the RAM during scan lines 21 through 42. The operation of the display RAM, character ROM, and output logic circuits are controlled during scan lines 43 through 237. Several functions of the MC144144 are controlled via a serial port which may be configured to be either I^2C or SPI.

- Conforms to FCC Report and Order as Amended by the Petition for Reconsideration on Gen. Doc. 91–1
- Conforms to EIA–608 for EDS Data Structure
- Supports Four Different Data Channels for Field 1 and Five Different Data Channels for Field 2, Time Multiplexed within the Line–21 Data Stream: Captions Utilizing Languages 1 and 2, Text Utilizing Languages 1 and 2 and EDS Support
- Output Logic Provides Hardware Underline Control and Italics Slant Generation
- Single Supply, Operating Voltage Range: 4.75 to 5.25 V
- Supply Current: 20 mA (Preliminary)
- Operating Temperature Range: 0 to 70°C
- Composite Video Input Range: 0.7 to 1.4 V p–p
- Horizontal Input Polarity: Either Positive or Negative
- Internal Timing and Sync Signals Derived from On–Chip VCO

In this document , the term 'user' refers to the television or VCR designer. The user may choose to make certain optional features selectable by the viewer. These features then become viewer options.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC145073

Product Preview

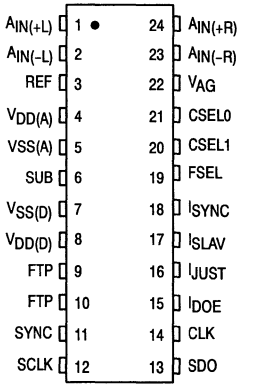
Dual 16-Bit Stereo Audio Sigma-Delta ADC

CMOS

DW SUFFIX
SOG PACKAGE
CASE 751E–04

ORDERING INFORMATION
MC145073DW SOG Package

PIN ASSIGNMENT

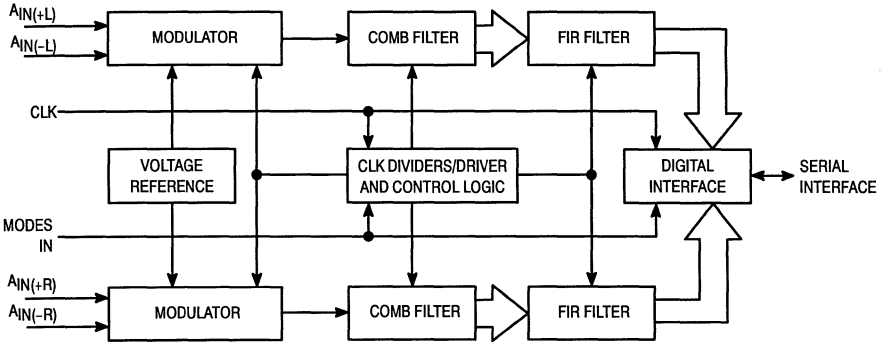


2

The MC145073 is a dual channel, 16–bit A/D converter intended for use in digital audio systems such as Multi–media, DCC, DAT and professional audio applications. It uses a sigma–delta architecture consisting of a second–order analog modulator and two stages of digital filtering for each channel. The analog modulator samples the input signal at 128x the output data rate, performs a single–bit quantization, and shapes the quantization noise towards higher frequencies. Subsequent on–chip digital filters reject most of the shaped quantization noise, and lower the data rate.

Sixteen unique user selectable interfacing modes make the MC145073 compatible with a multitude of application interfacing requirements. A single 5 V supply and a power down mode reduce power supply requirements, making the part attractive for portable applications.

- Single Supply, Operating Voltage Range: 4.5 to 5.5 V
- 128x OSR Sigma–Delta Modulator
- 82 dB Typical S/(N+D)
- Analog Inputs can be Driven as Either Differential or Single Ended
- Clock Input may be 128x, 256x, or 384x the Output Data Rate
- Out–of–Range Input Signals Internally Limited
- On–Chip Digital Filters:
  - 5th Order Decimate–by–32 Comb Filter
  - 121 Tap Decimate–by–4 FIR Filter
- User Selectable Digital Filter Transition Bands
- Versatile Serial Digital Output Interface:
  - Configurable as Master or Slave
  - Data can be Either Left or Right Justified
  - Interfaces to DSP56000/1 and TMS320 DSPs
  - I^2S or Japanese Interface Compatibility
  - CS5326 Compatible Interface Mode
  - Multiplexing of Two MC145073s Accommodated
- Power Down Mode Consumption: 2.0 mW
- Operating Temperature Range: – 40 to + 85°C



MAXIMUM RATINGS* (Voltages referenced to V_{SS}, unless otherwise stated)

Symbol	Parameter	Value	Unit
$V_{DD(A)}$	Analog Supply Voltage	+ 6.0	V
$V_{DD(D)}$	Digital Supply Voltage	+ 6.0	V
I_{in}	DC Input Current, per Pin	± 20	mA
$V_{in(A)}$	Analog Input Voltage	$V_{SS(A)}$ – 0.3 to $V_{DD(A)}$ + 0.3	V
$V_{in(D)}$	Digital Inputs	– 0.3 to $V_{DD(D)}$ + 0.3	V
T_{stg}	Storage Temperature	– 65 to 150	°C
T_l	Lead Temperature 1 mm From Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Operation Ranges, Analog Specifications, AC Electrical Characteristics and DC Electrical Characteristics tables.

2

OPERATION RANGES

Symbol	Parameter	Min	Max	Unit	Note
$V_{DD(A)}$	Analog Supply Voltage	4.5	5.5	V	
$V_{DD(D)}$	Digital Supply Voltage	4.5	5.5	V	
$V_{in(A)}$	Analog Input Voltage ($A_{IN(+L)}$, $A_{IN(-L)}$, $A_{IN(+R)}$, $A_{IN(-R)}$)	—	1.9	V_{pp}	1
f_{CLK}	CLK Frequency	3.072	18.432	MHz	2
C_{LOAD}	Capacitive Load on Any Output	0	50	pF	
T_a	Ambient Operating Temperature	– 40	85	°C	

NOTES:
1. Differential inputs greater than 3.8 V_{PP} will overload the modulators. These voltages are subject to the gain error tolerance specifications in the Analog Specifications table.
2. The internal clock frequency or input sampling frequency is governed by the divide mode and output data rate. The divide mode can be either 1, 2, or 3. The output data rate ranges from 24 kHz to 48 kHz. The minimum clock frequency of 3.072 MHz is for a 24 kHz output rate in the clock divide by 1 mode. The maximum clock frequency of 18.432 MHz is for a 48 kHz output rate in the clock divide by 3 mode.

DC ELECTRICAL SPECIFICATIONS

(Voltages referenced to $V_{SS(D)}$; Full Temperature and Voltage Ranges per Operation Ranges Table, unless otherwise indicated.)

Symbol	Parameter	Min	Max	Unit
V_{IH}	Minimum High–Level Digital Input Voltage	0.7 x $V_{DD(D)}$		V
V_{IL}	Maximum Low–Level Digital Input Voltage		0.3 x $V_{DD(D)}$	V
I_{IN}	Maximum Input Leakage Current		10	µA
V_{OH}	Minimum High–Level Digital Output Voltage (I_{OH} = – 20 µA)	4.4		V
V_{OL}	Maximum Low–Level Digital Output Voltage (I_{OL} = 20 µA)		0.1	V
$I_{DDu(D)}$	Maximum Digital Power Supply Current, Operating		45	mA
$I_{DDd(D)}$	Maximum Digital Power Supply Current, Power Down		250	µA
$I_{DDu(A)}$	Maximum Analog Power Supply Current, Operating		10	mA
$I_{DDd(A)}$	Maximum Analog Power Supply Current, Power Down		150	µA
P_O	Power Consumption, Operating		250	mW
P_{pd}	Power Consumption, Power Down		2.0	mW
Cin	Maximum Input Capacitance		20	pF

ANALOG SPECIFICATIONS

(Full Temperature, CLK = 6.144 MHz in div1, $V_{DD(A)} = V_{DD(D)} = 5.0$ V, 1007.8 Hz Full–Scale Input Sinewave, 1.4 V_{pp} @ $A_{IN(L)}$ and $A_{IN(R)}$, Common Mode Input Voltage = 2.5 V. Measured Bandwidth is 23 Hz to 24 kHz, inputs driven differentially per Figure 1.)

Parameter	Min	Typ	Max	Unit
Resolution Bits	16			bits
S/(N+D)	76	82		dB
Dynamic Range		85		dB
Total Harmonic Distortion (Vin = ± F.S.)		.003		%
Gain Error		+ 5/– 5		%
Gain Drift		50		ppm/°C
Channel to Channel Isolation		90		dB
PSRR ($V_{DD(A)}$)		60		dB
PSRR ($V_{DD(D)}$)		100		dB
Input Impedance		40		kohms
Warm–Up Time (for Reference and Bias Circuits)		1		msec

DIGITAL FILTER CHARACTERIZATION

(Over Full Operating Ranges per Operating Ranges table. Stated Values are for Input/Output Relationships from Input of Comb Filter to Output of FIR Filter).

Parameter	Output Data Rate			Unit	Notes
	32 kHz	44.1 kHz	48 kHz		
FSEL = low					
FIR Filter Passband	0 to 13.3	0 to 18.3	0 to 20	kHz	
Maximum Passband Ripple	± 0.1	± 0.1	± 0.1	dB	
FIR Filter Transition Band	13.3 to 17	18.3 to 23.5	20 to 25.8	kHz	
FIR Filter Rejection (Min)	– 84	–84	– 84	dB	
Maximum Alias Level (Figure 3)	– 86	– 86	– 86	dB	1, 2
Group Delay	33	33	33	Out CLKS	3
Setting Time	49	49	49	Out CLKS	3
FSEL = high					
FIR Filter Passband	0 to 14.5	0 to 20	0 to 21.7	kHz	
Maximum Passband Ripple	± 0.1	± 0.1	± 0.1	dB	
FIR Filter Transition Band	14.5 to 18.2	20 to 25.0	21.7 to 27.3	kHz	
FIR Filter Rejection (Min)	– 84	–84	– 84	dB	
Maximum Alias Level (Figure 3)	– 86	– 86	– 86	dB	1, 2
Group Delay	33	33	33	Out CLKS	3
Setting Time	49	49	49	Out CLKS	3

NOTES:

1. There is no rejection of input signals that are multiples of the sampling frequency (nxCLKI ± Filter Bandwidth, where n = 0, 1, 2, ...).
2. The maximum alias level spec does not apply to input signals in the range of 24 to 25.8 kHz in the 48 kHz output mode, 22.05 to 23.675 kHz in the 44.1 kHz output mode, or 16 to 17.2 kHz in the 32 kHz output mode.
3. One Out CLK (output clock) is equal in length to 128 internal CLKs or one SYNC clock period.

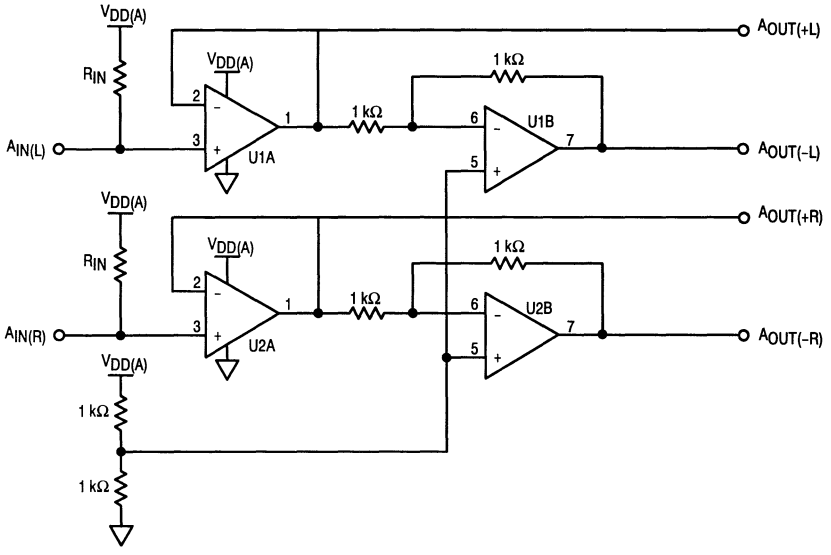


Figure 1. Input Buffer–Driver

NOTES:
1. Analog signals $A_{IN(L)}$ and $A_{IN(R)}$ are floating drivers. R_{OUT} of source is to be equal to R_{IN} of resistors.
2. U1, U2 — MC33077.

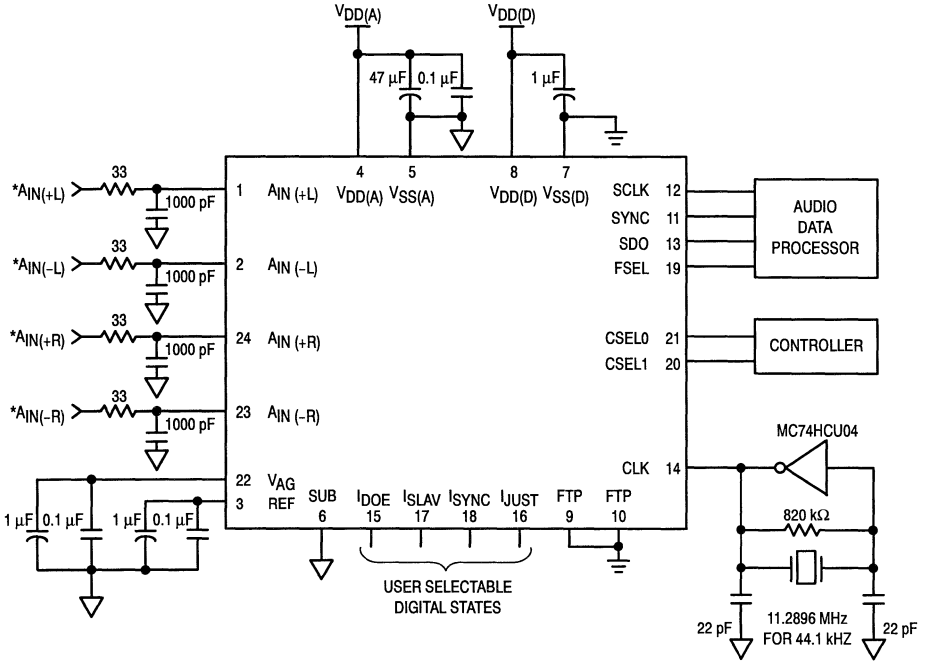


Figure 2. MC145073 A/D Application Circuit

* For best performance $A_{IN(+L)}$, $A_{IN(-L)}$ and $A_{IN(+R)}$, $A_{IN(-R)}$ should be differentially driven. $A_{IN(+L)}$ or $A_{IN(+R)}$ (and $A_{IN(-L)}$ or $A_{IN(-R)}$) can be grounded for single ended configuration. Circuit in Figure 1 depicts input buffer circuit.

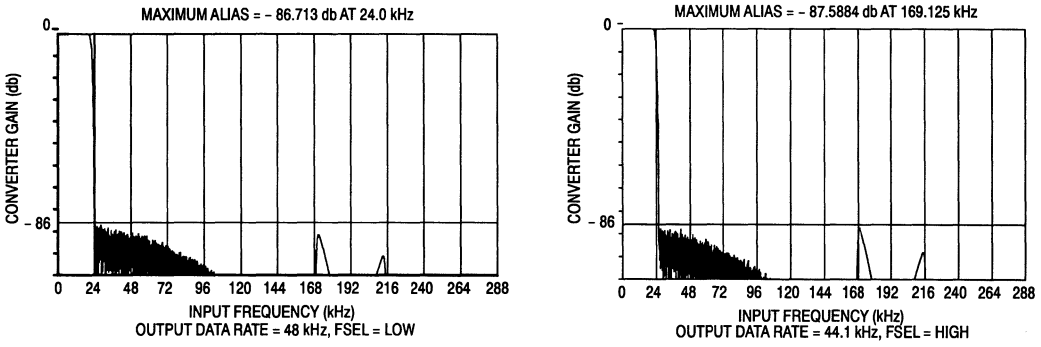


Figure 3. Digital Filter Response (Wideband)
CLKI = 6.144 MHz

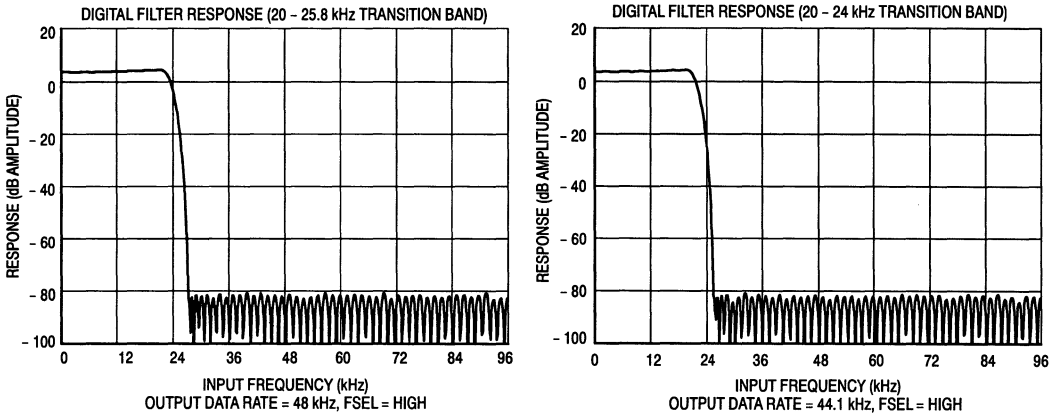


Figure 4. Digital Filter Response (Narrowband)
CLKI = 6.144 MHz

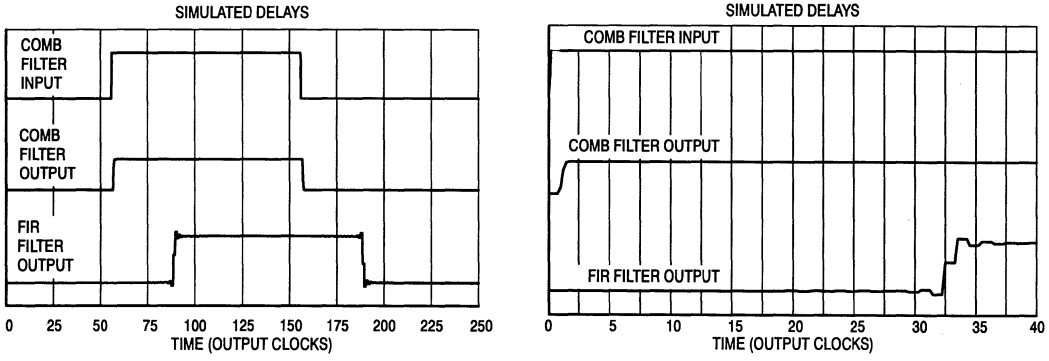


Figure 5. Group Delay and Setting Time

AC ELECTRICAL SPECIFICATIONS

(Full Temperature and Voltage Ranges per Operation Ranges Table. All timing parameters measured with respect to 30% and 70% of $V_{DD(D)}$ unless otherwise noted.)

Figure	Symbol	Parameter	Divide Ratio	Min	Max	Unit
6	$1/t_{clk}$	Master Clock (CLK) Frequency (Note 1)		3.072	18.432	MHz
6	$1/t_{clki}$	Internal Clock Frequency, CLKI (Note 1) $t_{clki} = 1/(f_{clk}/\text{Divide Ratio})$		3.072	6.144	MHz
6	t_{wch}	Master Clock High, CLK	1 2, 3	38 20		ns
6	t_{wcl}	Master Clock Low, CLK	1 2, 3	38 20		ns
7	t_{sync}	Sync Period (Master and Slave Modes)		128 * t_{clki}	128 * t_{clki}	ns
7	t_{wsh}	Sync High (Slave Mode)		20	126 * t_{clki}	ns
	C_{in}	Input Capacitance (Except for Left/Right Channel Inputs)			20	pF
		Master Mode: I_{SLAV} = 0				
8	t_{sclk}	SCLK Period		2 * t_{clki}	2 * t_{clki}	ns
8	t_{wl}/t_{wh}	SCLK Duty Cycle		0.667	1.50	
8	t_{CSY}	Propagation Delay (Note 2) CLK Falling Edge to SYNC CLK Rising Edge to SYNC CLK Falling Edge to SYNC	 1 2 3		 40 t_{clk} + 40 2 * t_{clk} + 40	 ns ns ns
8	t_{CSC}	Propagation Delay (Note 2) CLK Falling Edge to SCLK CLK Rising Edge to SCLK CLK Falling Edge to SCLK	 1 2 3		 40 t_{clk} + 40 2 * t_{clk} + 40	 ns ns ns
8	t_{CDV}	Propagation Delay (Note 2) CLK Falling Edge to Serial Data Valid, SDO CLK Rising Edge to Serial Data Valid, SDO CLK Falling Edge to Serial Data Valid, SDO	 1 2 3		 40 t_{clk} + 40 2 * t_{clk} + 40	 ns ns ns
		Slave Mode: I_{SLAV} = 1				
9	t_{su}	Setup Time (Note 3) SCLK to Rising Edge of CLK		15		ns
9	t_h	Hold Time (Note 3) SCLK to Rising Edge of CLK			0	ns
9	t_{sclkh}	SCLK High		20		ns
9	t_{sclkl}	SCLK Low		20		ns
9	t_{su}	Setup Time (Note 3) SYNC to Rising Edge of CLK		15		ns
9	t_h	Hold Time (Note 3) SYNC to Rising Edge of CLK			0	ns
	t_{CDV}	Propagation Delay Clk Rising Edge to Serial Data Valid, SDO	1 2 3	t_{wch} t_{clk} $t_{clk} + t_{wch}$	t_{wch} + 40 2 * t_{clk} + 40 3 * t_{clk} + t_{wch} + 40	

NOTES:

1. The internal clock frequency, or input sampling frequency (CLKI) is governed by the divide mode and output data rate.
   The divide mode can be either 1, 2, or 3. The output data rate ranges from 24 kHz to 48 kHz.
   The minimum clock frequency of 3.072 MHz corresponds to an output data rate of 24 kHz with the device in the clock divide by one mode.
   The maximum clock frequency of 18.432 MHz corresponds to an output data rate of 48 kHz with the device in the clock divide by three mode.
2. Propagation delay is measured with a capacitive load of 50 pF.
3. In the slave mode, SYNC or SCLK transitions can occur anywhere except 0 to – 5 ns relative to the CLK rising edge.

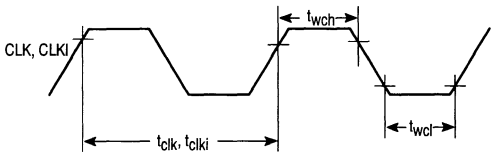


Figure 6.

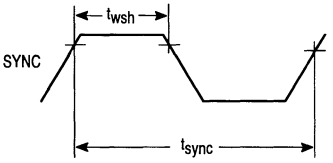


Figure 7.

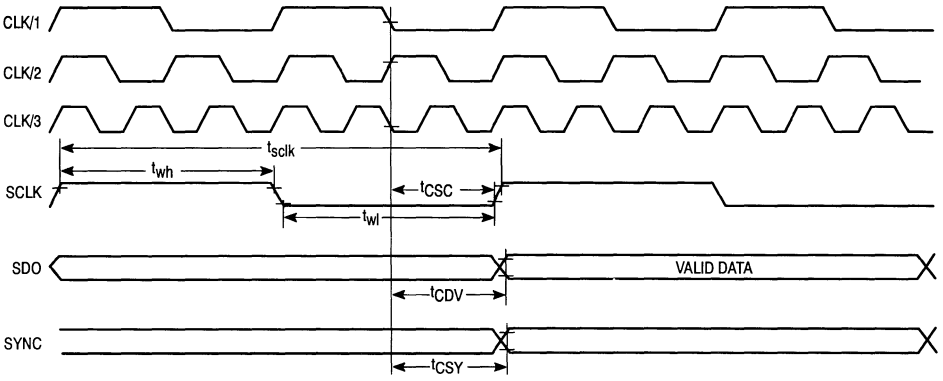


Figure 8. Serial Interface Timing (Master Mode: I_{SLAV} = 0)

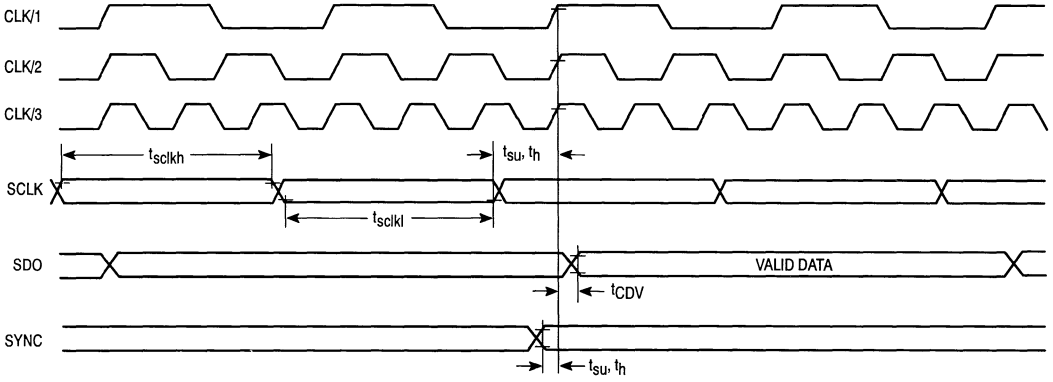


Figure 9. Serial Interface Timing (Slave Mode: I_{SLAV} = 1)

NOTE: CLK signals shown above represent the external clock at three different frequencies.

PIN DESCRIPTIONS

ANALOG PINS

$A_{IN(+L)}$, $A_{IN(-L)}$
Left Channel Analog Inputs (Pins 1, 2)

These two pins comprise the left channel analog differential inputs. The voltage range of signals applied to these pins is from $V_{SS(A)}$ to $V_{DD(A)}$. A positive full scale input to the A/D is defined as a difference of 3.8 Vpp between $A_{IN(+L)}$ and $A_{IN(-L)}$.

2

$A_{IN(+R)}$, $A_{IN(-R)}$
Right Channel Analog Inputs (Pins 24, 23)

These two pins comprise the right channel analog differential inputs. The voltage range of signals applied to these pins is from $V_{SS(A)}$ to $V_{DD(A)}$. A positive full scale input to the A/D is defined as a difference of 3.8 Vpp between $A_{IN(+R)}$ and $A_{IN(-R)}$.

REF
Output of the Internal Voltage Reference (Pin 3)

The nominal value of this internal voltage reference is + 2 VDC. The output of the reference is brought out to this pin to facilitate filtering. For proper device operation, this pin should be decoupled to $V_{SS(A)}$ with a 1.0 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. In order to economize on filtering capacitors, the REF pin can be connected to V_{AG}. However, this could result in a possible degradation of performance of the device at high signal levels.

V_{AG}
Output of the Internal Analog Ground Generator (Pin 22)

Analog ground is used to bias the internal analog circuits and is nominally + 2 VDC. V_{AG} is brought out to this pin to facilitate filtering. This pin should be decoupled to $V_{SS(A)}$ with a 1.0 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor for normal device operation.

DIGITAL PINS

CLK
Master Clock Input (Pin14)

This pin is the master clock input for the device. Analog input signals to the MC145073 are sampled at a rate equal to this clock frequency divided by 1, 2, or 3, depending on the state of clock mode pins CSEL1,0. The serial data output rate is equal to the input sample rate divided by 128. For example, if CLK is running at a 12.288 MHz rate, and divide by 2 is selected, then the output data rate is (12.288 MHz/2)/128 = 48 kHz. For more detail, see the Summary of Operating Modes section.

SYNC
Serial Interface Frame Sync Input/Output (Pin 11)

The SYNC pin is an input or output depending on the state of the I_{SLAV} pin. The SYNC signal resets and synchronizes the serial interface transmitter and receivers, as well as most internal clocks. Left channel serial output data is transmitted when the SYNC signal is active high, and right channel data is transmitted when the SYNC signal is low. See the Serial Interface Description section for more information.

SCLK
Serial Interface Clock Input/Output (Pin 12)

The SCLK pin is an input or output depending on the state of the I_{SLAV} pin. Serial output data is clocked out of the MC145073 on the rising edge of SCLK. When SCLK is an input, it is reclocked by the internal sample rate clock, CLKI, before being used by the MC145073 to clock out the serial data. This reclocking ensures that rapid current changes through the SDO pin do not affect the analog performance of the device. See the Serial Interface Description section for more information.

SDO
Serial Interface Data Output (Pin 13)

The A/D conversion results for the left and right channels are output on this pin. Data is shifted out of the MC145073 MSB first, with the left channel data preceding the right channel data. The serial output data is clocked out on the rising edge of SCLK. See the Serial Interface Description section for more information.

FTP
Factory Test Mode Inputs (Pins 9, 10)

These pins should be connected to $V_{SS(A)}$ for normal device operation.

CSEL0, CSEL1
Clock Divide Mode Select Inputs (Pins 21, 20)

The device master clock input is divided by 1, 2, or 3, or the device is placed in a power down mode depending on the state of these pins. See the Summary of Operating Modes section for more information.

FSEL
FIR Filter Response Select Input (Pin 19)

A low level on the FSEL input selects a FIR filter transition band from 20 to 25.8 kHz at the 48 kHz output data rate. A high level on the FSEL pin selects a filter transition band from 20 to 24 kHz at the 44.1 kHz output data rate. See the Summary of Operating Modes section for more information.

I_{SYNC}
Serial Interface Sync Format Select Input (Pin 18)

A low level input on the I_{SYNC} pin selects a SYNC rising edge one SCLK cycle before the initiation of a serial data transfer. A high level on the I_{SYNC} pin will select a SYNC rising edge that is coincident with the initiation of a serial data transfer. See the Summary of Operating Modes and the Serial Interface Description sections for more information.

I_{SLAV}
Serial Interface Slave Mode Select Input (Pin 17)

This pin controls the direction of the serial interface SYNC and SCLK signals. A low level on the I_{SLAV} pin will configure the SYNC and SCLK pins as inputs, while a high level on the I_{SLAV} pin will configure the SYNC and SCLK pins as outputs. See the Summary of Operating Modes and the Serial Interface Description sections for more information.

I_{JUST}
Serial Interface Data Justification Select Input (Pin 16)

A low level on the I_{JUST} pin will cause the serial output data to be left justified relative to the SYNC signal. A high level on the I_{JUST} pin will select right justification of the serial output data. See the Summary of Operating Modes and the Serial Interface Description sections for more information.

I_{DOE}
Serial Interface Data Output Enable (Pin 15)

This pin controls the state of the SDO pin between 16–bit data word transfers. A high level on this pin will force the SDO pin to a low level between serial data words, while a low level on the I_{DOE} pin will force the SDO pin to a high impedance state between data words. See the Summary of Operating Modes and the Serial Interface Description sections for more information.

POWER SUPPLIES

$V_{DD(A)}$ (Pin 4)

Positive analog power supply input. The voltage range for this pin is + 4.5 to + 5.5 VDC with respect to $V_{SS(A)}$. The absolute value of the difference between $V_{DD(A)}$ and $V_{DD(D)}$ must not exceed 0.5 V. For proper device operation, this pin should be decoupled to $V_{SS(A)}$ with a 1.0 μF or larger capacitor.

$V_{SS(A)}$ (Pin 5)

Negative analog power supply input. This pin should be connected to ground for normal device operation.

$V_{DD(D)}$ (Pin 8)

Positive digital power supply input. The voltage range for this pin is + 4.5 to + 5.5 VDC with respect to $V_{SS(D)}$. The absolute value of the difference between $V_{DD(A)}$ and $V_{DD(D)}$ must not exceed 0.5 V. For proper device operation, this pin should be decoupled to $V_{SS(D)}$ with a 1.0 μF or larger capacitor.

$V_{SS(D)}$ (Pin 7)

Negative digital power supply input. This pin should be connected to ground for normal device operation.

SUB (Pin 6)

Substrate connection. This pin should be connected to $V_{SS(A)}$ for normal device operation.

FUNCTIONAL DESCRIPTION

The MC145073 is a 16–bit Stereo Audio A/D converter intended for use in digital audio systems. The MC145073 uses a sigma–delta architecture consisting of a second order analog modulator followed by two stages of digital filtering for each channel. The analog modulator samples the input signal at a very high rate (128x the output data rate), performs a single bit quantization, and shapes the quantization noise towards out–of–band frequencies. The digital filters of the MC145073 reject most of the shaped quantization noise, and lower the serial data output rate. The digital filtering is implemented with a 5^{th} order, decimate–by–32 comb filter followed by a 121 tap, decimate–by–4, FIR filter on each channel. In addition to rejecting quantization noise, the FIR filter cancels the curvature in the response of the preceding comb filter. The comb and FIR filters also provide anti–alias filtering of out–of–band signals present at the input to the device. The analog inputs to the MC145073 can be fully differential (both inputs dynamic and 180 degrees out of phase), or single ended (positive inputs dynamic while negative inputs are static at a level in the middle of the supply range). Analog input signals that exceed the differential analog input voltage range of 3.8 V_{p-p} are clipped in order to prevent overflow of the digital filters. The MC145073 operates from a single + 5 V power supply. For portable or other low power applications, a power down mode is available.

The operation of the MC145073 can be tailored to specific applications by proper selection of the states of seven mode select pins. These mode pins control the divide ratio of the master clock, the FIR filter response, and the serial interface format. The master clock input can be divided by either 1, 2, or 3 to yield the input sampling rate. This means that the input clock frequency is either 128x, 256x, or 512x the serial output data rate.

NOTE

The oversampling ratio (OSR), which is the ratio of input sampling frequency to output data rate, is 128x in all three cases.

Two sets of FIR filter coefficients are stored in the onboard ROM of the MC145073. One set provides a transition band from 20 kHz to 25.8 kHz for operation at the 48 kHz output data rate. The other set of FIR filter coefficients provides a transition band from 20 kHz to 25 kHz for use with the 44.1 kHz output data rate.

Four mode select pins configure the serial interface. This yields sixteen possible serial interface operating modes. Included are modes that provide for interfacing directly to Motorola and TI general purpose DSPs, multiplexing of two MC145073s, as well as formats similar to the CS5326 interface.

SUMMARY OF DEVICE OPERATING MODES

The seven pins summarized in the tables below configure the MC145073 to operate in one of the modes specified. The modes can be chosen in any combination.

CSEL1	CSEL0	Master CLK Divider Select
0	0	Power Down
0	1	Divide CLK by 1
1	0	Divide CLK by 2
1	1	Divide CLK by 3

FSEL	FIR Filter Transition Band Select
0	20 kHz – 25.8 kHz Transistion band 6.144 MHz input rate, 48 kHz output data rate.
1	20 kHz – 25 kHz Transistion band 5.6448 MHz input rate, 44.1 kHz output data rate

I_{SYNC}	Serial Interface SYNC Signal Format
0	SYNC rising edge is one SCLK cycle before the start of the serial output data transfer (this is compatible with the DSP5600/56001 and TMS320 interface definitions).
1	SYNC rising edge is coincident with the start of the serial output data transfer (this is compatible with the CS5326 interface definition).

I_{SLAV}	Serial Interface Master or Slave Select
0	MC145073 is a master, SYNC and SCLK are outputs.
1	MC145073 is a slave, SYNC and SCLK are inputs (re–clocked by the MC145073 internal clock, CLKI).

I_{JUST}	Serial Interface Data Justification Select
0	Serial Output data is left justified relative to the SYNC signal.
1	Serial Output data is right justified relative to the SYNC signal.

I_{DOE}	Serial Interface Data Output Enable
0	SDO goes to a high impedance state between 16 bit output words.
1	SDO is forced low between 16 bit output words.

SERIAL INTERFACE DESCRIPTION

As summarized in the previous section, the format of the serial interface is controlled by four mode pins: I_{SYNC}, I_{SLAV}, I_{JUST}, and I_{DOE}. These control inputs can be configured in any combination, yielding $2^4 = 16$ unique modes. The following two subsections describe the format of the serial interface for these various modes. Timing information for the serial interface is provided in the section entitled "AC Electrical Specifications".

Compatibility with the DSP56000/1 and TMS320 general purpose DSPs is accomplished by applying the appropriate logic level to the I_{SYNC} pin. The phase of the rising edge of the SYNC signal is different for the DSP56000 and TMS320 applications, while the falling edge of SYNC is not critical in such applications.

To interface to one or two MC145073s, the DSP56000/56001 should be configured as follows: network mode, 4 time slots per frame, 16 bits per slot, continuous clock, and control signals configured as either a master or slave. If interfacing to a TMS320 is desired, the serial interface should be configured in continuous mode without frame sync.

NOTE

The TMS320 interface must be initialized with frame sync enabled, and then switched to the no frame sync mode after initialization.

The I_{JUST} and I_{DOE} serial interface mode control inputs are provided to facilitate multiplexing of two MC145073s. The I_{JUST} input selects between left and right justification of the serial output data relative to the SYNC signal, while the I_{DOE} input provides a way to force the SDO pin to the high impedance state between the output data words. To multiplex the serial data outputs of two MC145073s onto the same SDO line, I_{DOE} must be forced low on both MC145073s, while the I_{JUST} pin is forced high on one MC145073 and low on the other. The MC145073s must be in the slave mode (I_{SLAV}=1) when multiplexing. It is not possible to operate with one MC145073 as a master tied to a second MC145073 operating as a slave due to the reclocking of the SYNC and SCLK inputs in the slave mode (see section, "Operation with the MC145073 as a Slave (I_{SLAV} = 1)").

NOTE

When multiplexing two MC145073 devices, all four analog channels are sampled at exactly the same phase.

In Figures 10 and 11, the internal clock signal CLKI is plotted instead of CLK. This is due to the fact that all internal clocks, as well as the serial interface are slaved to this divided version of the master clock. Input signals to the serial interface are reclocked by CLKI to reduce the amount of noise injected into the analog section of the MC145073. Serial output data and high impedance states of the SDO pin are clocked out relative to CLKI. This reclocking can cause a shift in phase of SDO relative to SCLK when operating in the slave mode. In cases where the MC145073 output is multiplexed with another device, the clock divide by 1 mode is recommended.

NOTE

If the clock divide by 2 or 3 mode is selected, it is impossible to know the exact phase of CLKI.

On initial power up or recovery from a power down condition, the first 68 serial output words of the MC145073 are indeterminate. This is because the digital filters and internal logic of the MC145073 must settle. This time is also used to charge the external REF filter capacitor.

Operation with the MC145073 as a Master (I_{SLAV} = 0)

When I_{SLAV} = 0 the SYNC and SCLK signals are defined as outputs, and the MC145073 is configured as master device. In this mode there are eight possible serial formats as illustrated in Figure 10. The phase of the SYNC output can precede the serial output data by one SCLK cycle (compatible with DSP56000/56001, TMS320, and I^2S interface format), or the SYNC signal can be coincident with the serial output data (similar to the CS5326 serial interface format). As shown in Figure 10, with each of these two SYNC formats there are four possible formats for the serial output data.

Serial output data is shifted out MSB first, with left channel data preceding the right channel data. All of the serial interface outputs, SYNC, SCLK, and SDO are initiated by a CLKI rising edge. There are 128 CLKI cycles, and 64 SCLK cycles per output data cycle. Multiplexing of two MC145073s is not feasible in the master mode since the exact phase of the output cannot be controlled.

NOTE

The serial data in one output cycle represents data that was simultaneously sampled on the two analog input channels.

It is possible to initiate the device in the slave mode described in section, "Operation with the MC145073 as a Slave (I_{SLAV} = 1)", and then switch to master mode. Once set, the phase of SYNC should not change.

Operation with the MC145073 as a Slave (I_{SLAV} = 1)

When I_{SLAV} = 1 the SYNC and SCLK signals are defined as inputs, and the MC145073 is configured as a slave device. However, the slave mode of the MC145073 is not a true slave mode since the SYNC and SCLK inputs are reclocked by the internal sample clock, CLKI. These internal reclocked versions of SYNC and SCLK are shown in Figure 11, in addition to the external SYNC and SCLK signals.

Similar to the master mode of the previous section, there are two formats for the SYNC signal, and four SDO formats, yielding eight possible slave modes.

Multiplexing of two MC145073s in the slave mode is performed by forcing I_{DOE} low on both MC145073s, and forcing I_{JUST} high on one MC145073 and low on the other.

NOTE

When multiplexing two MC145073s, the master clock divide by 1 mode should be used (CSEL1,0 = 0,1) so that the exact phase of CLKI is determined.

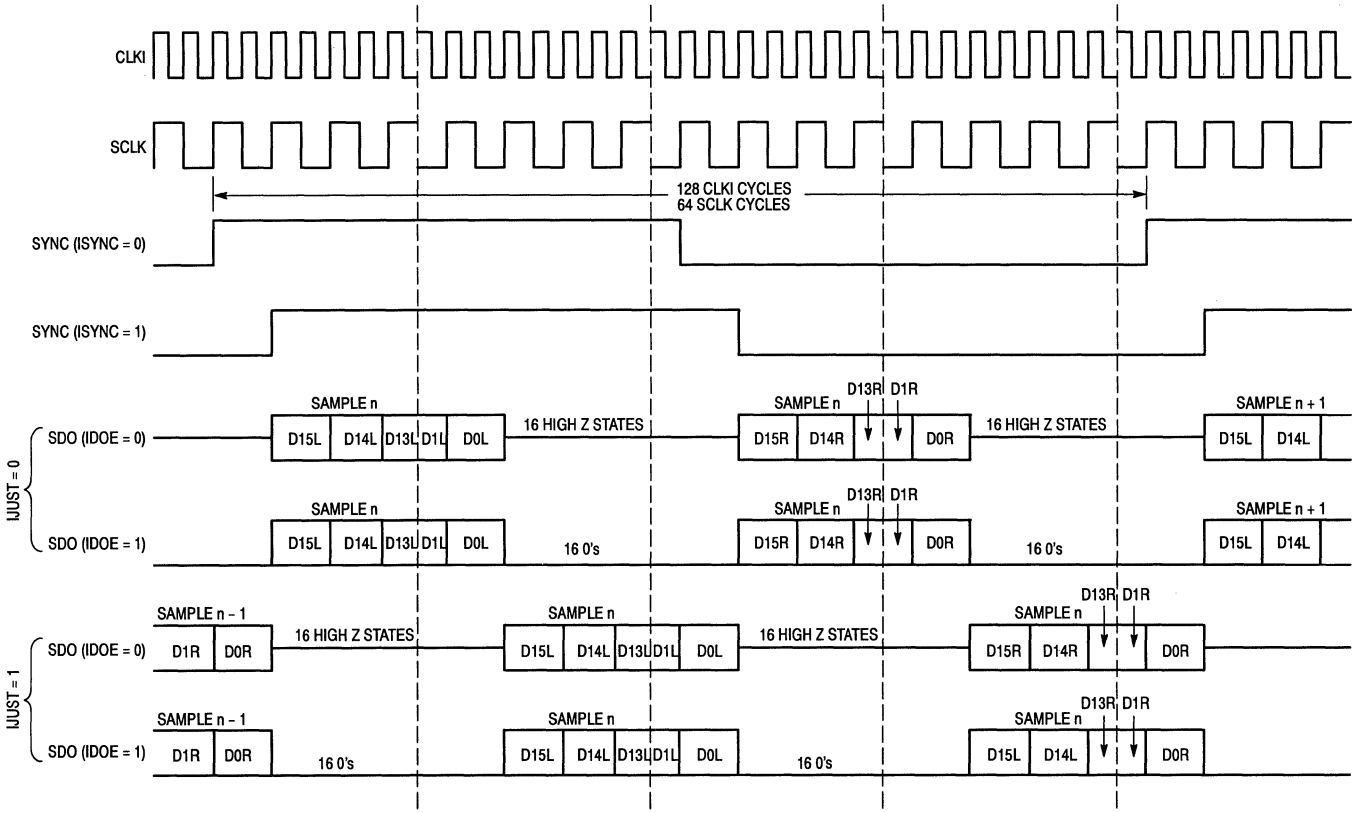


Figure 10. Serial Interface Operation with MC145073 Configured as Master (I_{SLAV} = 0)

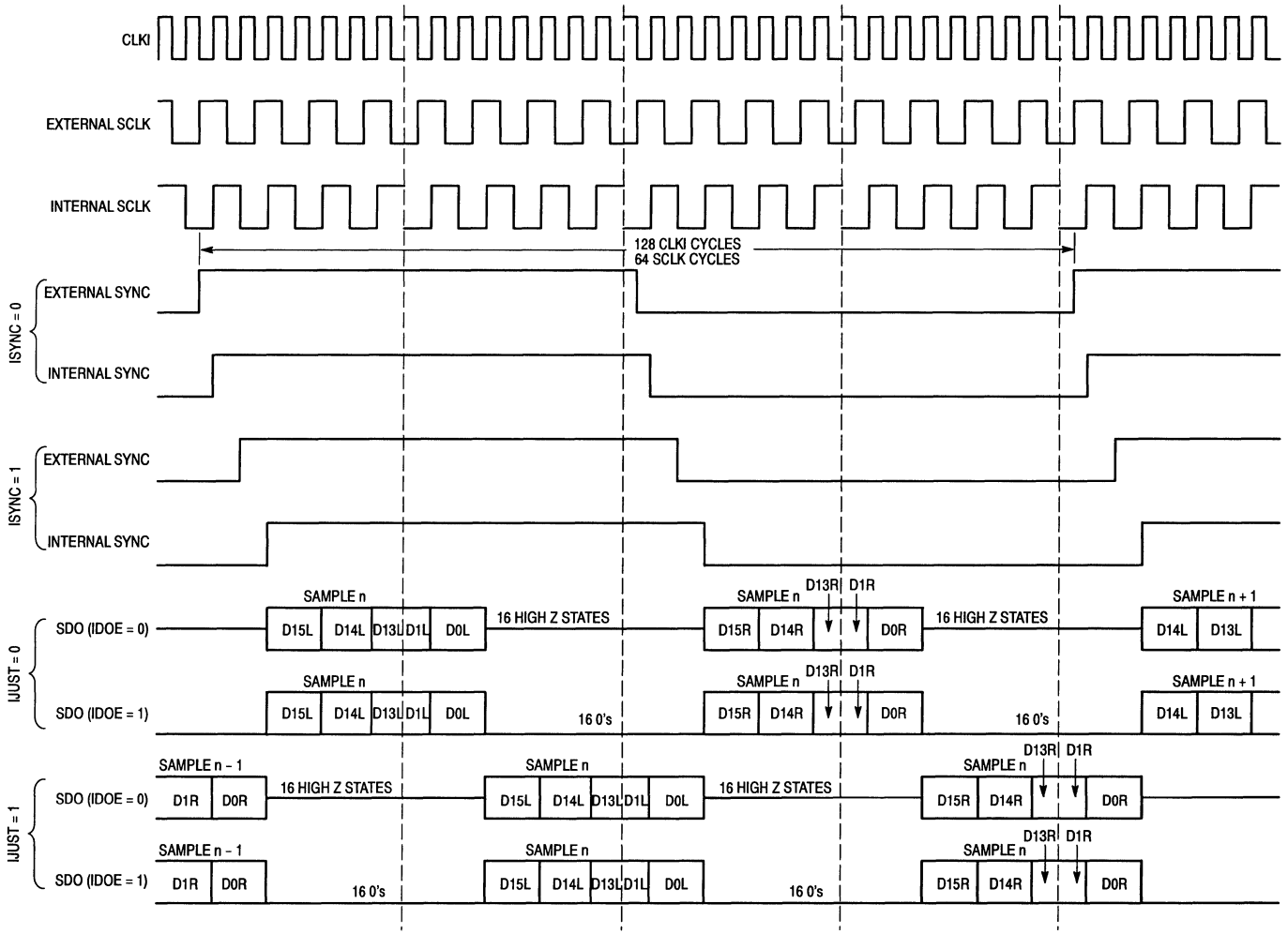


Figure 11. Serial Interface Operation with MC145073 Configured as Slave (I_{SLAV} = 1)

MC145074

Product Preview

Stereo Audio Sigma-Delta Digital-to-Analog Converter

CMOS

2

The MC145074 is a high precision, Stereo Audio Digital–to–Analog Converter that utilizes second order sigma–delta modulators with 2–tap FIR feedback architecture. The part can be used as a stand alone stereo digital modulator, or as a companion part to the MC145076 smoothing filter to achieve high quality, low cost audio performance.

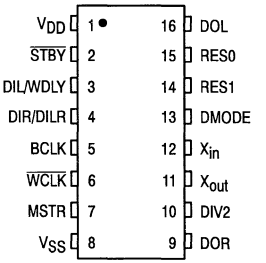
- Peak S/(N+D) > 100 dB
- Single 5 V Supply Operation
- Accepts 16, 18, or 20–Bit Data Words
- Dual/Single Pin Data Input Modes
- Programmable WCLK Divider
- Operating Temperature Range: – 40 to + 85°C
- Low Power Consumption: 40 mW Typical
- Companion to MC145076 Stereo Audio FIR Smoothing Filter

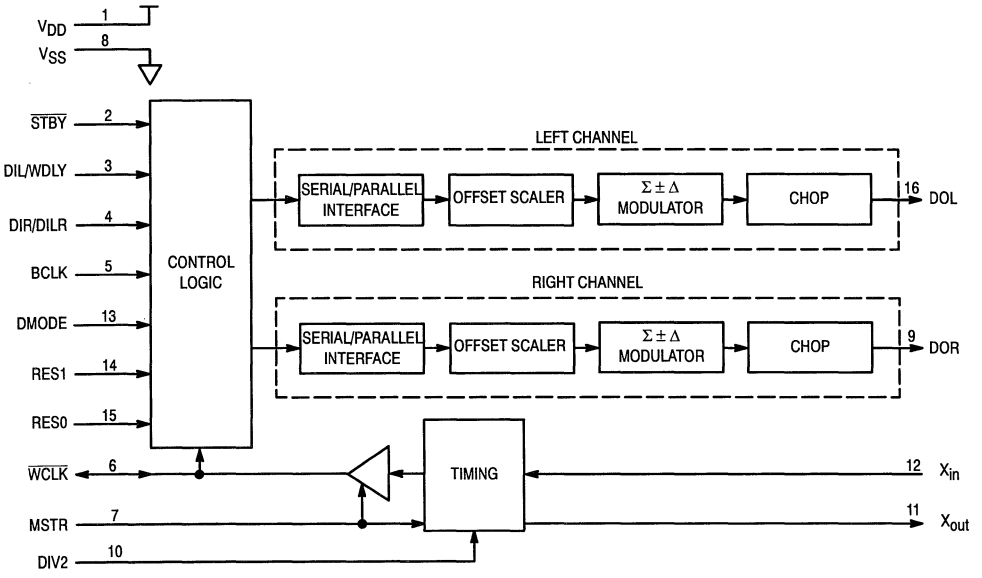
D SUFFIX
16 PIN SOIC
CASE 751B–05

ORDERING INFORMATION

MC145074D	SOIC Package

PIN ASSIGNMENT





This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	6.0	V
V_{in}	DC Input Voltage, Any Digital Input	V_{SS} – 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	±10	mA
T_{stg}	Storage Temperature	– 55 to 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Operation Ranges below.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

2

OPERATION RANGES (Applicable to Guaranteed Limits)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage, Referenced to V_{SS}	4.5 to 5.5	V
V_{in}, V_{out}	Digital Input/Output Voltage	V_{SS} – 0.5 to V_{DD} + 0.5	V
I_D	Input Pin Current Drain	1	µA
T_A	Operating Temperature	– 40 to + 85	°C

DC ELECTRICAL CHARACTERISTICS

(Voltages Referenced to V_{SS}, Full Temperature and Voltage Ranges per Operation Ranges table, unless otherwise indicated)

Symbol	Parameter		Min	Typ	Max	Unit
I_{dd}	Power Supply Current		—	—	10	mA
V_{IL}	Input Voltage	Low Level Input	—	—	V_{DD} x 0.3	V
V_{IH}		High Level Input	V_{DD} x 0.7	—	—	
V_{OL}	Output Voltage	Low Level Output (Load = 0.4 mA)	—	—	0.3	V
V_{OH}		High Level Output (Load = 0.4 mA)	V_{DD} – 0.3	—	—	
I_{lkg}	Input Leakage Current		—	—	± 10	µA

AC ELECTRICAL CHARACTERISTICS

(Full Temperature and Voltage Ranges per Operation Ranges table)

Symbol	Parameter	Figure	Guaranteed Limit	Unit
	Operating Frequency X_{in} (DIV2 = 0) (DIV2 = 1)		18.5 37.0	MHz
	Bit Clock Frequency		18.5	MHz
t_r, t_f	Maximum Rise and Fall Times	2, 5	6	ns
t_{PLH} t_{TLH}	X_{out} L–H Propagation Delay X_{out} Rise Time	2	TBD	ns
t_{PHL} t_{THL}	X_{out} H–L Propagation Delay X_{out} Fall Time	2	TBD	ns
t_{PLH} t_{TLH}	DOL, DOR L–H Propagation Delays DOL, DOR Rise Time	3	TBD	ns
t_{PHL} t_{THL}	DOL, DOR H–L Propagation Delays DOL, DOR Fall Time	3	TBD	ns
t_{PLH} t_{TLH}	$\overline{WCLK}$ Output L–H Propagation Delay $\overline{WCLK}$ Output Rise Time	4	TBD	ns
t_{PHL} t_{THL}	$\overline{WCLK}$ Output H–L Propagation Delay $\overline{WCLK}$ Output Fall Time	4	TBD	ns
t_{su} t_h	DIR Master Program Mode Minimum Setup Time DIR Master Program Mode Minimum Hold Time	5	TBD	ns
t_{su} t_h	DIR, DIL Minimum Setup Time DIR, DIL Minimum Hold Time	5	TBD	ns
t_{su} t_h	$\overline{WCLK}$ Minimum Setup Time to BCLK (not DMODE = WDLY = 1) $\overline{WCLK}$ Minimum Hold Time to BCLK (not DMODE = WDLY = 1)	6	TBD	ns
t_{su} t_h	$\overline{WCLK}$ Minimum Setup Time to X_{in} (not DMODE = WDLY = 1) $\overline{WCLK}$ Minimum Hold Time to X_{in} (not DMODE = WDLY = 1)	6	TBD	ns
t_{su} t_h	$\overline{WCLK}$ Minimum Setup Time to BCLK (DMODE = WDLY = 1) $\overline{WCLK}$ Minimum Hold Time to BCLK (DMODE = WDLY = 1)	7	TBD	ns
t_{LAG} t_{LEAD}	BCLK to X_{in} (1st Edge Only) Lag Time (DMODE = WDLY = 1) BCLK to X_{in} (1st Edge Only) Lead Time (DMODE = WDLY = 1)	7	TBD	ns

SWITCHING WAVEFORMS

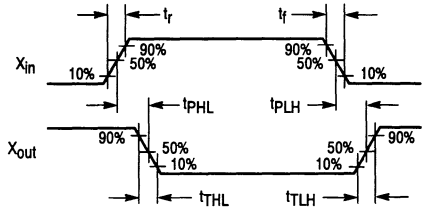


Figure 1. X_{out} Propagation Delay Timing

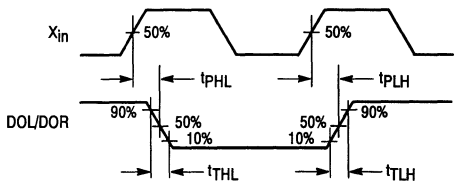


Figure 2. DOL/DOR Propagation Delay Timing

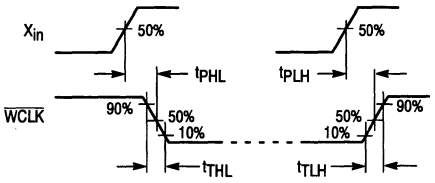


Figure 3. $\overline{WCLK}$ Out Propagation Delay Timing (Master Mode)

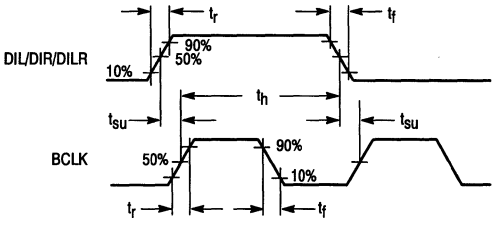


Figure 4. DIL/DIR/DILR Setup and Hold Timing

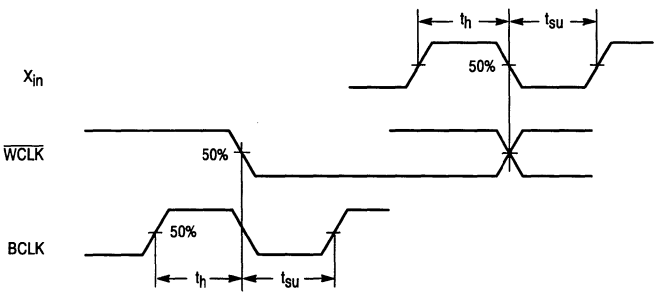


Figure 5. $\overline{WCLK}$ Timing (All Modes Except DMODE = 1, WDLY = 1)

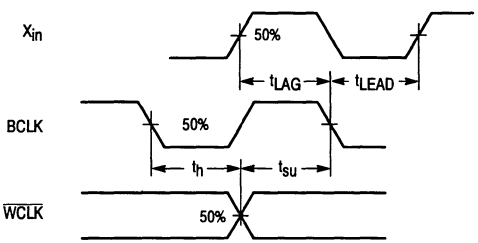


Figure 6. $\overline{WCLK}$ Timing (DMODE = 1, WDLY = 1)

Bits	16	18	20
OSR	S/(N+D) dB	S/(N+D) dB	S/(N+D) dB
128x	90	90	90
192x	94	98	99
256x	95	103	105
384x	96	107	113

NOTE: Values are for 0 dB input signal, 0 – 20 kHz BW, and 44.1 kHz 1x fs Sampling Rate.

Figure 7. Digital S/(N+D) Performance Levels

PIN DESCRIPTIONS

V_{DD}
Positive Device Supply (Pin 1)

V_{DD} is the positive supply, nominally + 5 volts.

$\overline{STBY}$
Active–Low Standby Input (Pin 2)

A low level on the $\overline{STBY}$ pin will force the device into a standby state. If the device is being operated in the master mode (MSTR = 1), the $\overline{WCLK}$ internal divider can be programmed using the DIR/DILR, and BCLK pins while the $\overline{STBY}$ pin is active. When the device is in standby, the DOL and DOR pins will output a 50% duty cycle data stream that will generate a 1/2 scale analog output, when averaged through the output filter.

DIL/WDLY
Left Channel Data/Word Clock Delay Input (Pin 3)

When the DMODE pin is low, this pin is the left channel (MSB first) 2's complement serial data input. When the DMODE pin is high, this pin controls the $\overline{WCLK}$ delay. A high level on this pin will delay the $\overline{WCLK}$ an additional clock cycle internal to the device.

DIR/DILR
Right Channel Data/Multiplexed Left – Right Data Input (Pin 4)

When the DMODE pin is low, this pin is the right channel (MSB first) 2's complement serial data input. When the DMODE pin is high, this pin is the multiplexed left then right channel data input. If the part is being operated in the master mode (MSTR = 1), the $\overline{WCLK}$ internal divider can be programmed by clocking control word data onto this pin with the BCLK pin while the device is in the standby mode ($\overline{STBY}$ = 0).

BCLK
Bit Clock Input (Pin 5)

The BCLK pin provides the serial bit shift clock for the left and right channel data in all modes of operation. A rising edge on the BCLK pin shifts serial data into the device.

$\overline{WCLK}$
Word Clock Output/Input (Pin 6)

The $\overline{WCLK}$ pin is used to latch the shifted serial data word into the device. The MC145074 can accept an external word clock when in the slave mode, or can use an internally generated word clock when operating in the master mode. When DMODE is low, left and right channel data is latched into the device on the falling edge of $\overline{WCLK}$. When DMODE is high, left channel data is latched on the rising edge of $\overline{WCLK}$ and right channel data is latched on the falling edge of $\overline{WCLK}$ with both channel inputs being input to the modulator on the next rising edge of $\overline{WCLK}$. The internal divide ratio used to generate $\overline{WCLK}$, as well as the rising or falling edge latching of the input data can be programmed using the DIR/DILR and BCLK pins while the device is in the standby mode.

MSTR
Active–High Master Mode Select Input (Pin 7)

A high level on the MSTR pin will select the master mode of operation. In the master mode, the MC145074 will generate and output a word clock signal on the $\overline{WCLK}$ pin. A low level on the MSTR pin will place the MC145074 in the slave mode, and the $\overline{WCLK}$ signal must be provided by an external source. The default master mode divide rate is MODCLK/64.

V_{SS}
Device Ground (Pin 8)

V_{SS} is normally connected to ground.

DOR
Right Channel Data Output (Pin 9)

DOR is the right channel modulator data output.

DIV2
Master Clock Divide Control Input (Pin 10)

DIV2 is the X_{in} divide by two control pin. When cleared, the X_{in} pin directly provides the modulator clock (MODCLK), and the data output bit streams are not chopped. When this pin is set, the X_{in} clock is divided by two to provide the modulator clock and the output data bit stream is chopped at the X_{in} frequency using an alternating 1,0 chop. The chop is used to reduce even order distortion for a stand–alone application without the MC145076. The reconstructed output signal will drop 6dB due to the chopping.

X_{out}
Master Clock Output (Pin 11)

X_{out} is the inverted output signal of X_{in} and may be used for a buffered clock output or for a crystal oscillator.

X_{in}
Master Clock Input (Pin 12)

X_{in} is the input clock pin for the MC145074, and may be used with X_{out} as the inverter for a crystal oscillator.

DMODE
Data Mode Input (Pin 13)

A low level on the DMODE pin will select the dual data pin mode of operation. In this mode, the serial input data is entered on the DIR and DIL pins. A high level on the DMODE pin selects the multiplexed mode of operation. In this mode, the left and right channel serial input data must be multiplexed on the DIR/DILR pin.

RES0 and RES1
Input Data Resolution Pins (Pins 14, 15)

The RES0 and RES1 pins select the length of the serial data word input to the MC145074. The serial input data can be 16, 18, or 20–bits in length with the most significant bits clocked in first. Figure 9 lists the serial interface formats.

DOL
Left Channel Data Output (Pin 16)

DOL is the left channel modulator data output.

DMODE	RES1	RES0	Operating Mode
0	0	0	Dual Data Pin 16–Bit Input
0	0	1	Dual Data Pin 18–Bit Input
0	1	0	Dual Data Pin 20–Bit Input
0	1	1	Factory Test Mode
1	0	0	Single Data Pin 16–Bit Input
1	0	1	Single Data Pin 18–Bit Input
1	1	0	Single Data Pin 20–Bit Input
1	1	1	Factory Test Mode

Figure 8. Serial Interface Formats

FUNCTIONAL DESCRIPTION

The MC145074 is a high precision Stereo Audio Digital–to–Analog Converter, which utilizes a second–order sigma–delta modulator with a patented 2–tap architecture that significantly reduces problems normally associated with one–bit sigma–delta technology. Normally, a second order modulator can develop patterns in the digital output representation of small signals and with small DC input offsets. It is common to add dither to mask these effects, but a reduction of dynamic range can result. The implementation used in the MC145074 has considerable immunity to these troublesome inputs, and without performance compromise.

With RC filtering, the MC145074 can be used as a stand–alone stereo digital modulator for applications with modest requirements. High performance can be realized with the companion MC145076 Stereo Audio FIR Smoothing Filter, which reduces the in–band IM products formed by large amplitude spectral components of the out–of–band noise shaping, clock corruption, and power supply noise.

The MC145074 has been designed for maximum flexibility and is well suited for high fidelity audio and multimedia applications. If used in conjunction with a differential MC145076 smoothing filter, a peak S/(N+D) ratio of > 100 dB can be achieved by utilizing 18 or 20–bit input data and a 256x oversampling ratio. The MC145074 has a maximum operating frequency of 18.5 MHz, and can be used with any sampling rate including 32, 44.1, or 48 kHz.

The MC145074 can accept a 1x, or a 2x input clock with serial data output chop. The device can accept 16, 18, or 20–bit digital data in a dual data pin input format, or single pin multiplexed format. An offset scaler is included to allow 0 dB digital inputs while maintaining low distortion. The offset, scaled data is applied to the D/A modulator before being optionally chopped (2x mode), and sent to an external smoothing filter. When this device is used with the MC145076, dividing the clock down or using the chop mode is not necessary.

TIMING CIRCUIT

The internal timing circuits of the MC145074 are driven by the X_{in} clock. When the DIV2 pin is active high, the MC145074 divides the X_{in} clock by two to generate the internal modulator clock (MODCLK), and uses the X_{in} clock frequency to chop the output data using a 50% chop signal.

When the MC145074 is operated in the master mode, the $\overline{WCLK}$ pin is configured as an output. The $\overline{WCLK}$ output is generated by dividing down the modulator clock. The divide ratio of the internal frequency divider can be programmed utilizing a 5–bit control word while the MC145074 is in the standby mode. The 5–bit control word is defined as the last 5–bits (MSB first) that are clocked into the DIR/DILR pin using the BCLK signal. When cleared, the most significant bit of the control word indicates that the $\overline{WCLK}$ signal is negative edge triggered (just as in the slave mode). If the most significant bit is set, the $\overline{WCLK}$ is positive edge triggered. The next three most significant or middle three bits of the control word determine the value of the divide ratio of the internal frequency divider. The least significant bit of the 5–bit control word indicates a prescaler divide by two when cleared, and divide by three when set. The divider modes are summarized in Figure 10.

NOTE

The default mode of operation is control word $06 which provides a $\overline{WCLK}$ signal (negative edge triggered) at a frequency of 1/64 the modulator clock frequency. This is the preferred operating mode of 256x OSR and 4x FIR.

Control Word Value (Hex)	Divide Ratio	$\overline{WCLK}$ Edge	Control Word Value (Hex)	Divide Ratio	$\overline{WCLK}$ Edge
0	8		10	8	
1	12		11	12	
2	16		12	16	
3	24		13	24	
4	32		14	32	
5	48		15	48	
6	64		16	64	
7	96	↓	17	96	↑
8	128		18	128	
9	192		19	192	
A	256		1A	256	
B	384		1B	384	
C	512		1C	512	
D	768		1D	768	
E	1024		1E	1024	
F	1536		1F	1536	

Figure 9. $\overline{WCLK}$ Divider Modes

OFFSET SCALER

Second order sigma–delta modulators typically give up about 2 dB of dynamic range and an adjustment to the digital input words must be made if full scale digital input word recognition is desired. The offset scaler circuitry of the MC145074 digitally attenuates the input linearly to 3/4 or approximately – 2.5 dB. Figure 11 illustrates the function of the offset scaler block. An ideal DAC would perform as shown in curve one, but the sigma–delta modulator actually operates as shown in curve two. The digital input words to the MC145074 are attenuated to 3/4. This allows the MC145074 to operate on all 2's compliment digital inputs from $80000 to $7FFFF, with the resulting response shown in curve three. In addition to scaling the digital input word, the offset scaler adds a digital dc offset of 1/8th to re–center the digital input word so that the MC145074 output signal is centered around $V_{DD}/2$.

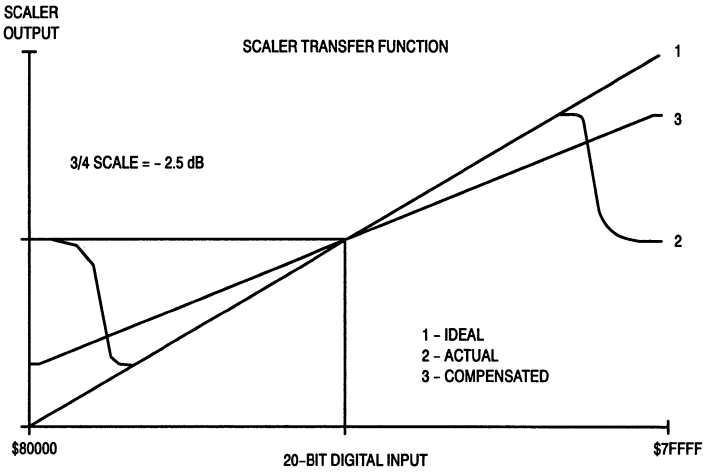


Figure 10. Offset Scaler Operation

SERIAL INTERFACE AND CONTROL LOGIC

The serial interface and control logic of the MC145074 may be configured to accept 16, 18, or 20–bit data words by applying the appropriate logic levels to the RES1 and RES0 pins. The DMODE input pin configures the serial interface to accept 2's complement data (MSB first) in a dual data pin or single pin, multiplexed input format. It should be noted that in some cases when using the single data pin input mode and a large OSR, the BCLK rate may be too high for some DSPs, unless an interface circuit is added. Figure 9 shows the available serial interface formats of the MC145074.

When operating in a dual data pin mode, 2's complement data words are serially input from the DIR and DIL pins as shown in Figure 12. A rising edge on BCLK serially shifts in the data present on the DIR and DIL inputs. After all data bits of an input word are shifted in, a falling edge on $\overline{\text{WCLK}}$ latches the data word into the MC145074. The BCLK can be a continuous clock as long as the serial input data word is right justified in the word time, or as long as there exists one and only one BCLK cycle for every data bit input to the device.

When operating in a single pin multiplexed mode, the DIR input pin is reconfigured as the DILR pin. Left and right channel serial input data is multiplexed into the MC145074 on the DILR pin, and is serially shifted into the part using BCLK as shown in Figure 13. When WDLY is low, left channel data is latched into the part on the rising edge of $\overline{\text{WCLK}}$, and right channel data is latched on the falling edge of $\overline{\text{WCLK}}$. As in the dual data pin mode, the BCLK can be either an asynchronous or continuous clock as long as the serial input data word is right justified in the word time. Forcing WDLY high allows the $\overline{\text{WCLK}}$ cycle to appear one clock cycle early as shown in Figure 14.

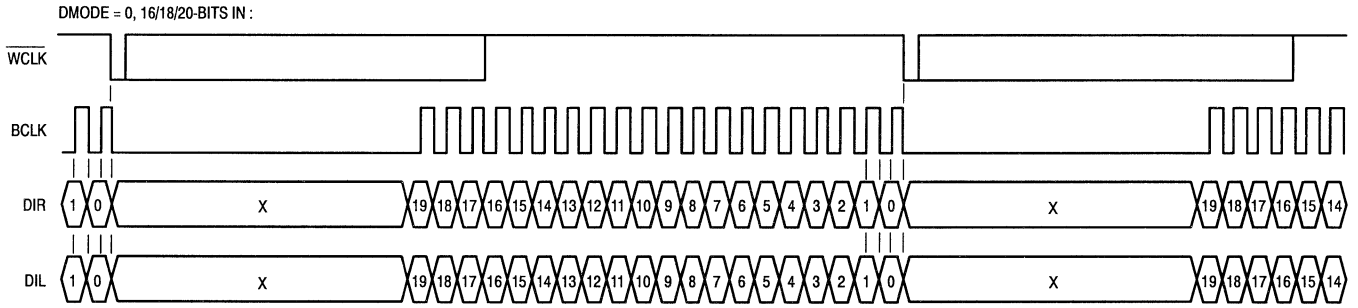


Figure 11. DMODE = 0 Serial Interface Timing Diagram

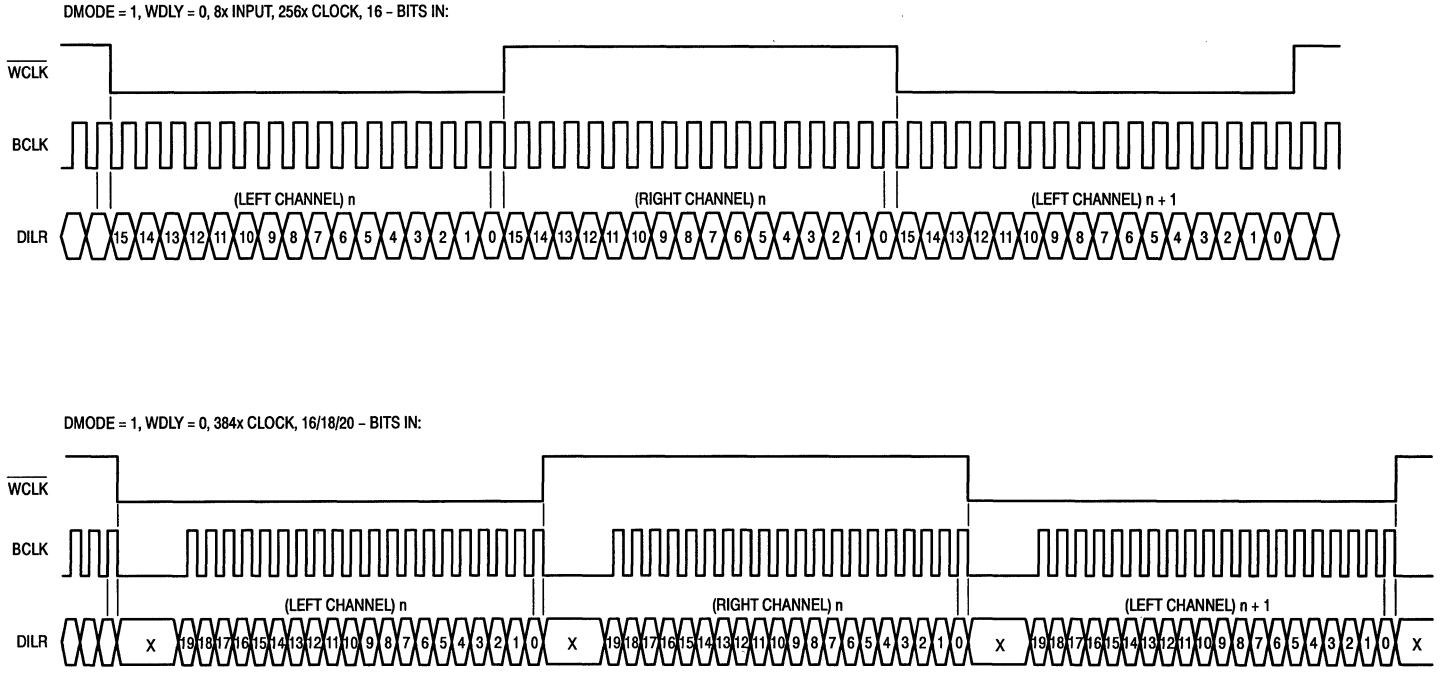


Figure 12. DMODE = 1, WDLY = 0, Serial Interface Timing Diagram

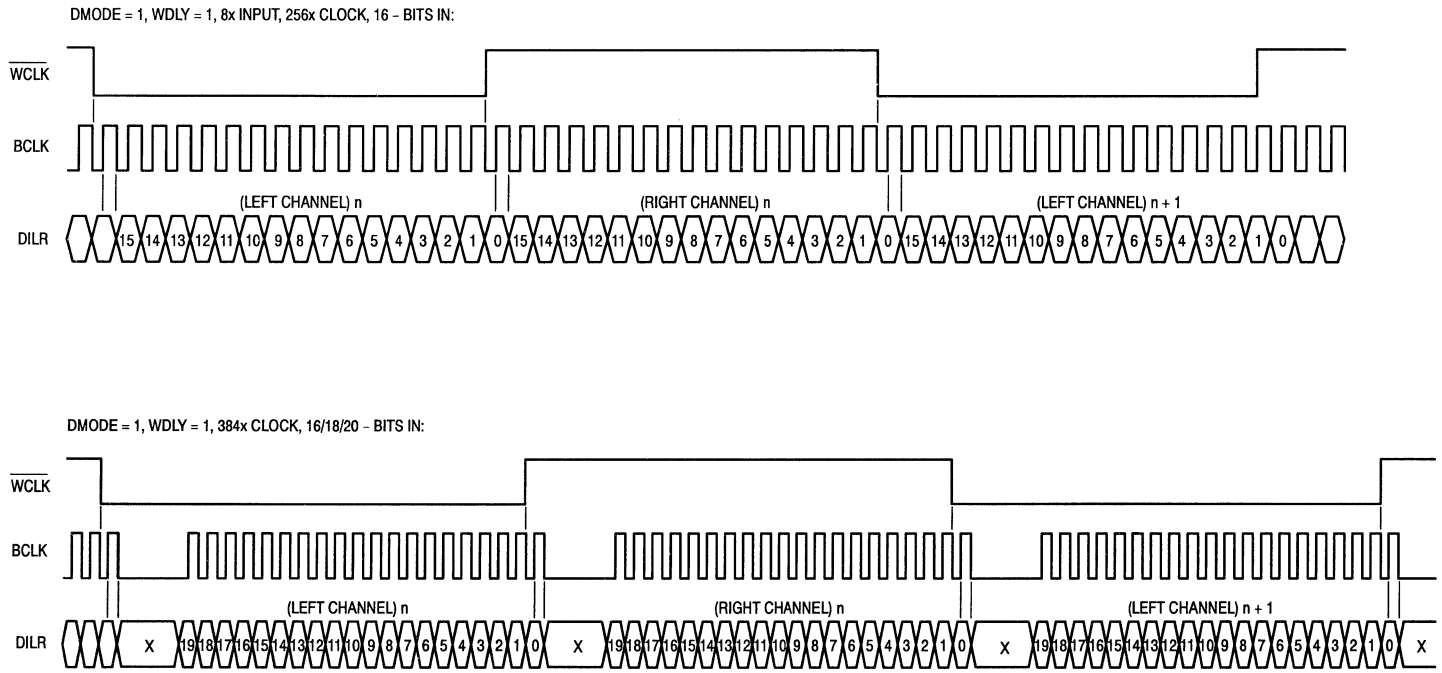
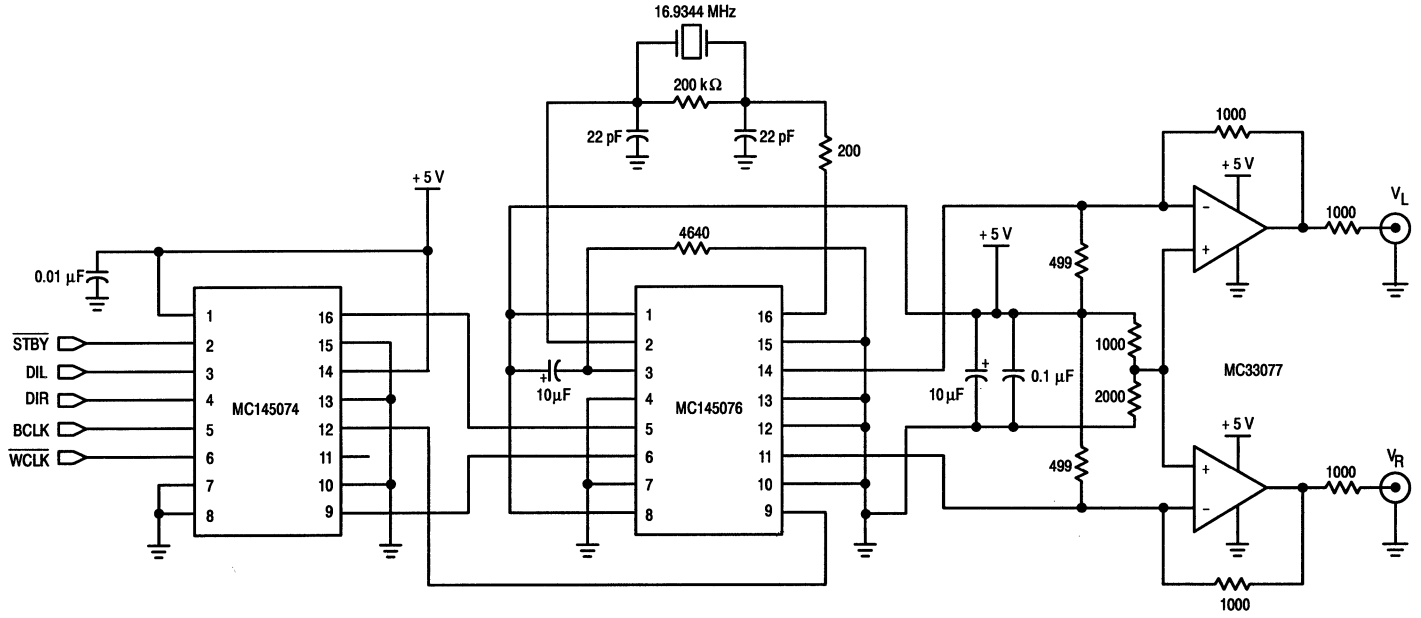
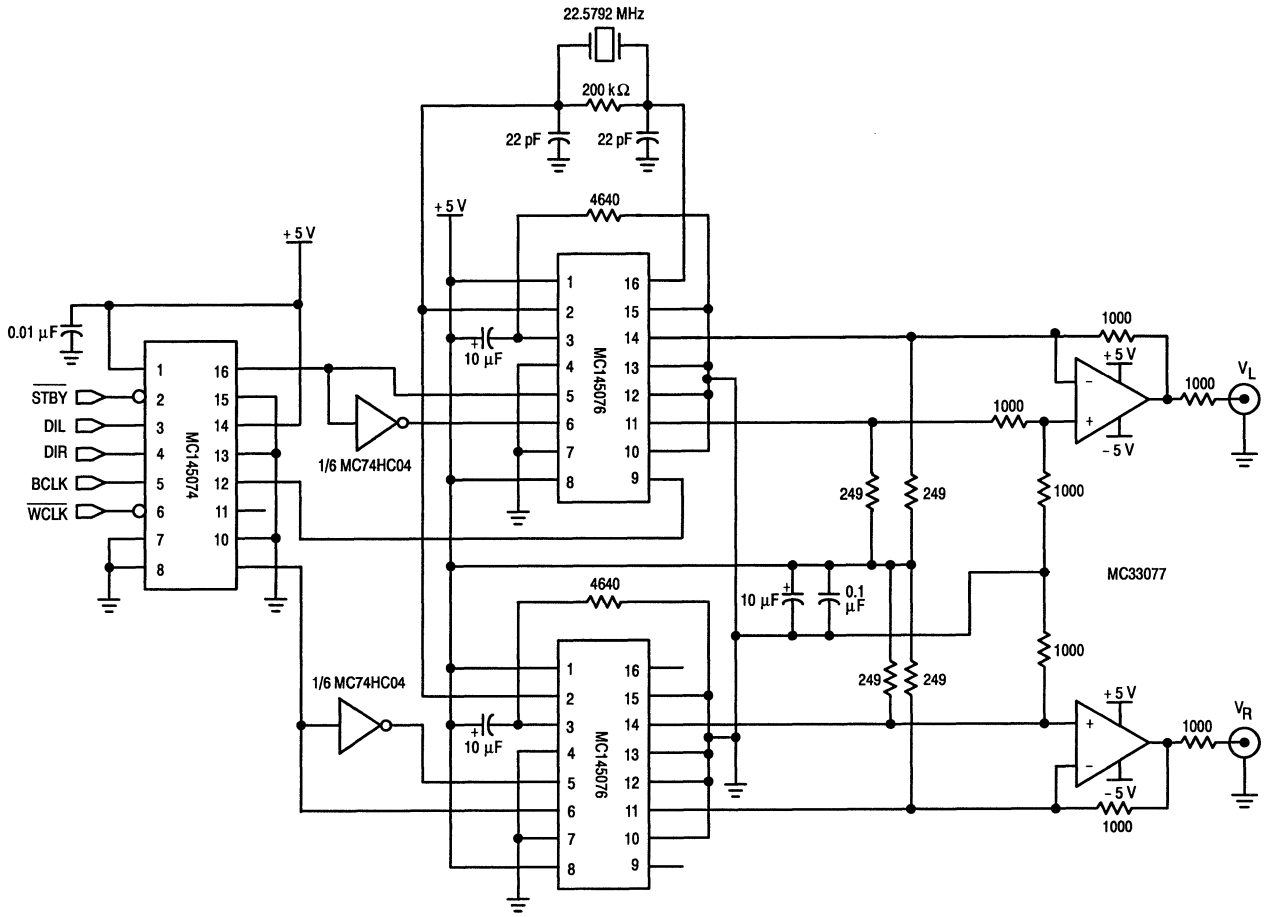


Figure 13. DMODE = 1, WDLY = 1, Serial Interface Timing Diagram



*ALL RESISTORS 1%

Figure 14. Low Cost + 5 V Stereo Audio System, Typically 88 dB S/(N+D)



*ALL RESISTORS 1%

Figure 15. Mid Performance Stereo Audio System, Typically 98 dB S/(N+D)

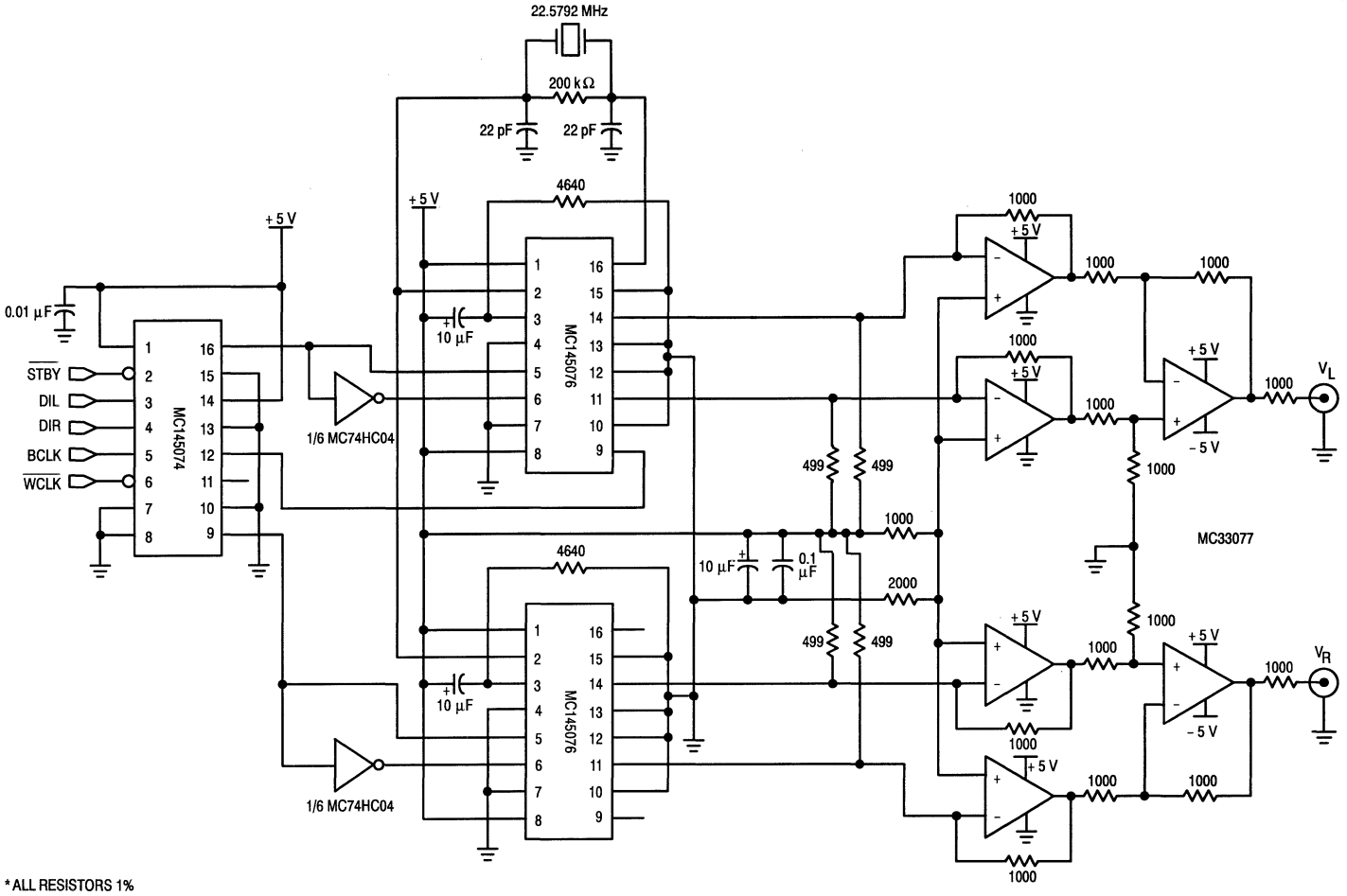


Figure 16. High Performance Stereo Audio System, Typically 105 dB S/(N+D)

MC145076

Product Preview

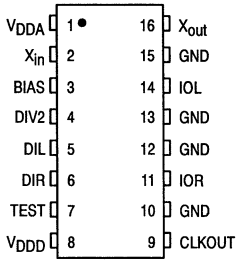
MC145076 Stereo Audio FIR Smoothing Filter

CMOS

D SUFFIX
16–PIN SOG
CASE 751B–05

ORDERING INFORMATION
MC145076D SOG Package

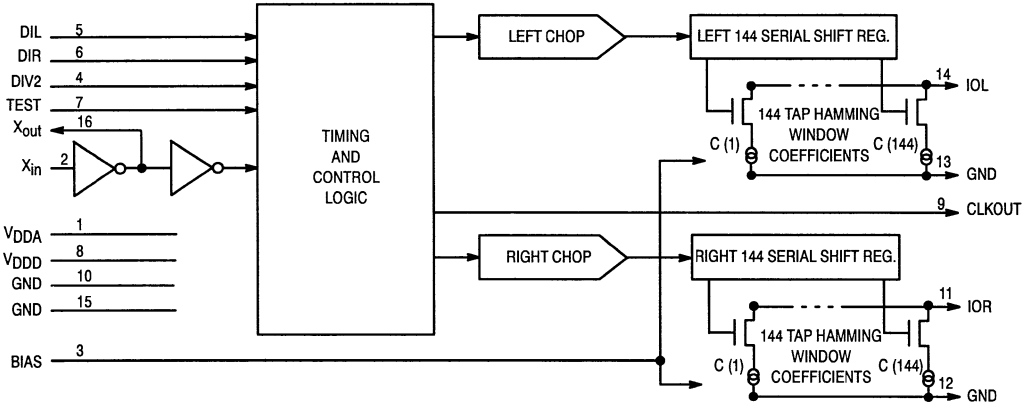
PIN ASSIGNMENT



The MC145076 is a combination re–clocking and smoothing filter designed especially for the MC145074 Stereo Audio DAC. Its versatility however, allows it to be used with any single bit–stream data converter to provide output reconstruction filtering, and to improve performance by restoring pulse shape integrity. The MC145076 provides a well controlled, filtered output that can be used directly, or with a current summing operational amplifier.

The MC145076 is intended to be one half of a two–chip solution for serial bit steam DACs. The analog filtering function of the MC145076 eases the digital filtering requirements at the input to the digital noise shaping modulator, and eliminates the need for precision analog output filtering capacitors, resulting in lower overall system cost. The MC145076 pulse shape restoration frees the designer from analog pitfalls that can impact performance, thereby lowering the risk of new product development with a sigma–delta DAC.

- Single–Ended Stereo Outputs Require no Additional Smoothing Filters
- 86 dB S/D, 96 dB S/N with MC145074 @ 192 x OSR Single Ended
- > 100 dB S/(N+D) @ 256 OSR, Differential Mode
- 18.5 MHz Maximum Serial Data Input Rate
- – 80 dB Cross Channel Interference
- 72–Tap FIR with > 40 dB Alias Filtering
- Operating Temperature Range: – 40 to + 85°C
- Buffered Data Clock Output for Ease of Data Generation
- 16–Pin Narrow Body SOIC Package
- Single Supply Operation: + 5 V



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to GND)	6.0	V
V_{in}	DC Input Voltage	GND – 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	GND – 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I_{DD}, I_{GND}	DC Supply Current, V_{DD} and GND Pins	± 60	mA
T_{stg}	Storage Temperature	– 55 to 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Operation Ranges below.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{DD}). Unused outputs must be left open.

OPERATION RANGES (Applicable to Guaranteed Limits)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	4.5 to 5.5	V
V_{IOL}, V_{IOR}	IOL, IOR Virtual Ground	V_{DD} – 2.0 to V_{DD}	V
T_A	Ambient Operating Temperature	– 40 to + 85	°C

DC ELECTRICAL CHARACTERISTICS

(Voltages Referenced to GND, Full Temperature and Voltage Ranges per Operation Ranges Table, unless otherwise indicated)

Symbol	Parameter		Guaranteed Limit	Unit
V_{IH}	Minimum High–Level Input Voltage		0.7 x V_{DD}	V
V_{IL}	Maximum Low–Level Input Voltage		0.3 x V_{DD}	V
V_{OH}	Minimum High–Level Output Voltage	I_{OH} = 0.4 mA	V_{DD} – 0.3	V
V_{OL}	Maximum Low–Level Output Voltage	I_{OL} = 0.4 mA	GND + 0.3	V
I_{DD}	Maximum Power Supply Current	R_{bias} = 4640 Ω	40	mA
I_{OL}, I_{OR}	Left/Right Channel Output Current*		2 ± 20%	mA
I_{Ikg}	Input Leakage Current		± 10	µA

* 50% Duty Cycle, V_{DDA} = 5 V, R_{bias} = 4640 Ω

SINGLE ENDED ANALOG CHARACTERISTICS

(X_{in} = 16.9344 MHz, DIV2 = 0, f_{in} = 990.527 Hz, 20 Bit 2nd Order Modulator Input Data)

Parameter	Test Conditions	Min	Typ	Max	Unit
Dynamic Range	S/(N+D) @ – 60 dB input, + 60 dB	—	96	—	dB
S/(N+D) Flat	(– 6 dB) 25 to 75% peak to peak input duty cycle	86	90	—	dB
A–weighted	(– 20 dB)	—	80*		
Idle Channel Noise	CLKOUT/4 digital input data pattern	—	105	—	dB
60 Hz Power Supply Rejection	With 47 µF and 4640 Ω on Bias Pin	—	40	—	dB

* Noise performance limited by second order digital modulator.

AC ELECTRICAL CHARACTERISTICS (Full Temperature and Voltage Ranges per Operation Ranges Table)

Symbol	Parameter	Guaranteed Limit	Unit
f	Clock Frequency, X_{in}	37	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, X_{in} to X_{out}	TBD	ns
t_{TLH}, t_{THL}	Maximum Rise/Fall Time, X_{out}	TBD	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, X_{in} to CLKOUT	TBD	ns
t_{TLH}, t_{THL}	Maximum Rise/Fall Time, CLKOUT	TBD	ns
t_{su}	Minimum DIR, DIL Setup Time From X_{in}	TBD	ns
t_h	Minimum DIR, DIL Hold Time From X_{in}	TBD	ns

NOTE: 50 pF load capacitance, X_{in} rise and fall times set at 2 ns.

2

TIMING WAVEFORMS

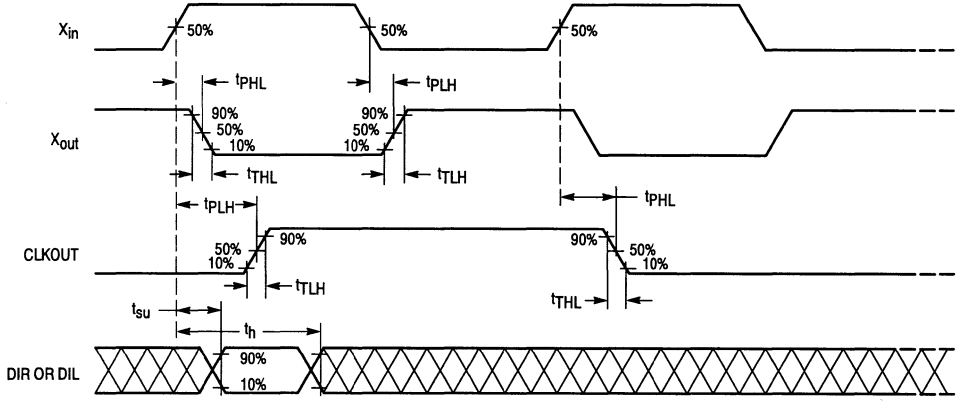


Figure 1.

PIN DESCRIPTIONS

X_{in}, X_{out}
Oscillator Inverter Input and Output (Pins 2, 16)

If an external clock is used to drive the MC145076, the clock should be connected to X_{in} pin. For maximum performance however, it is recommended that these pins be used in conjunction as a crystal oscillator.

BIAS
Bias Adjust (Pin 3)

For normal device operation, this pin should be connected to ground through a 4.7 kΩ resistor, which provides nominal quiescent output current of 2 mA each channel. In addition to the 4.7 kΩ resistor, a 47 µF capacitor may be connected from this pin to the V_{DD} supply.

DIV2
Active–High Clock Divider Control Input (Pin 4)

When this pin is at a logic low level, the internal clock will be equal to the oscillator, (X_{in}) frequency, and data can be clocked into the device at an $fX_{in}/2$ rate. When this pin is at a logic high level, the internal clock is one–half the X_{in} oscillator frequency, and data can be clocked into the device at an $fX_{in}/4$ rate.

DIL, DIR
Left/Right Channel Data Inputs (Pins 5,6)

These pins are the left and right digital input data pins from the single bit–stream sigma–delta DAC. Serial input data to the MC145076 is clocked in near the rising edge of CLKOUT.

TEST
Active–High Factory Test Mode Input (Pin 7)

This pin is reserved for factory testing, and should be connected to device ground for normal device operation.

CLKOUT
Buffered Divided Clock Output (Pin 9)

This pin provides a buffered clock output to be used as the clock source for a sigma–delta bit stream generator. The CLKOUT frequency is one–half the X_{in} frequency if DIV2 = 0, and one–fourth the X_{in} frequency if DIV2 = 1. The serial input data is clocked in near the rising edge of CLKOUT.

IOR, IOL
Left/Right Channel Current Outputs (Pins 11,14)

These pins are the current sink outputs of the smoothed single–bit input data.

V_{DDD}, V_{DDA}
Device Supply Pins (Pins 1,8)

These two pins are the positive power supply pins for the MC145076, nominally 5 V. For proper device operation, it is recommended that 0.1 µF and 10 µF capacitors be connected from these pins to ground via the shortest possible path.

GND
Device Ground Pins (Pins 10,12,13,15)

These pins are the ground pins for the device.

FUNCTIONAL DESCRIPTION

Serial bitstream Digital–to–Analog Converters (DACs) have become commonplace due to their ability to use over–sampling techniques to shape quantization noise. This noise shaping ability enables devices to be built that do not require the component matching of conventional architectures.

The MC145076 bitstream FIR smoothing filter consists of two shift registers, two sets of Hamming Window weighted current source summing networks, and a crystal oscillator inverting buffer.

The current source summing networks are used to implement a Hamming Window function within the MC145076. Each current source tap sinks a constant current that does not change with the number of bits that are set in the shift register. Therefore, each tap acts as a separate single–bit converter with excellent linearity characteristics. The Hamming window was chosen for the FIR filter coefficients because this allows a slightly better second lobe attenuation close to the band where the sampling images are the most troublesome. For a 256 OSR, the MC145076 FIR filter provides greater than 40 dB of stop band attenuation, with approximately 50 dB of attenuation at the 8x image frequencies. This results in an output with full scale images of less than – 70 dB and out–of–band noise better than – 60 dB. For other OSR rates, the filter response scales linearly.

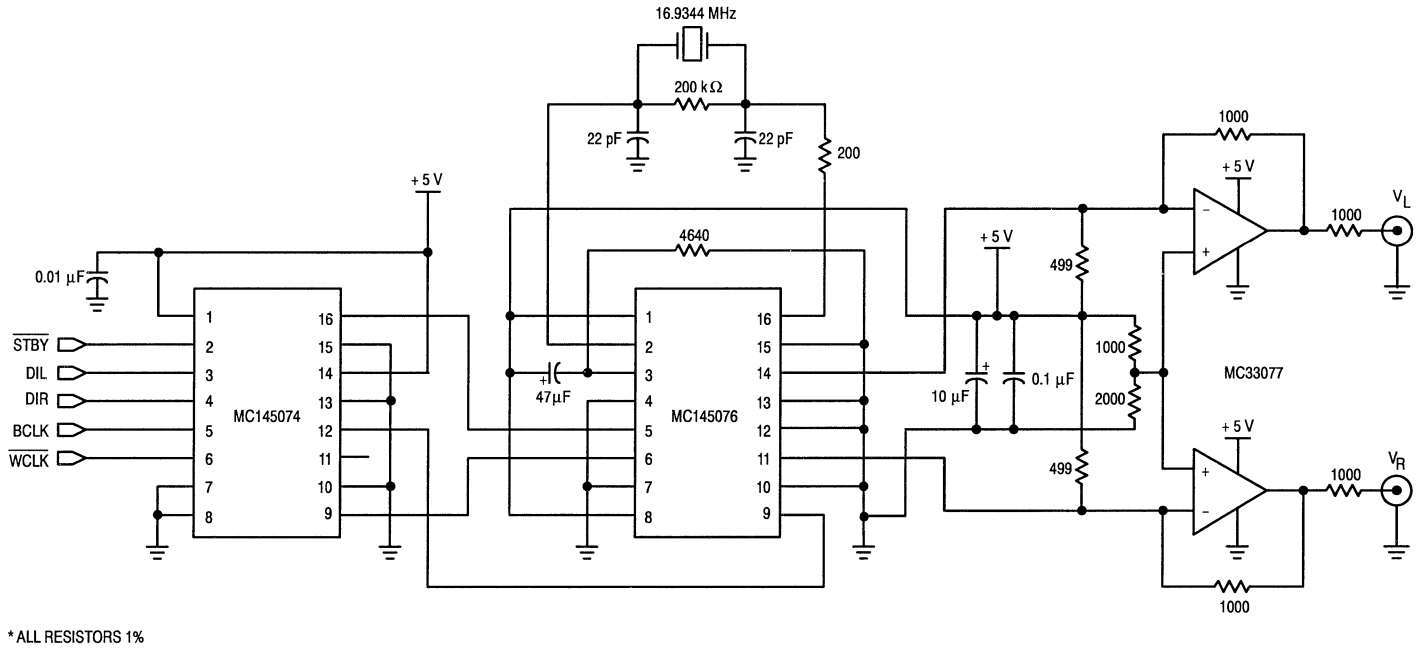
CRYSTAL OSCILLATOR

Provisions for an on–chip crystal oscillator are provided to insure that the clock will be as clean as possible internal to the MC145076 where the digital–to–analog conversion occurs, thus assuring maximum performance. An output clock buffer is provided for driving additional off–chip digital circuitry such as a digital noise shaper, over–sampling FIR filter, or DSP. The off–chip digital processing ensures that the digital switching noise on chip is kept to a minimum.

APPLICATIONS

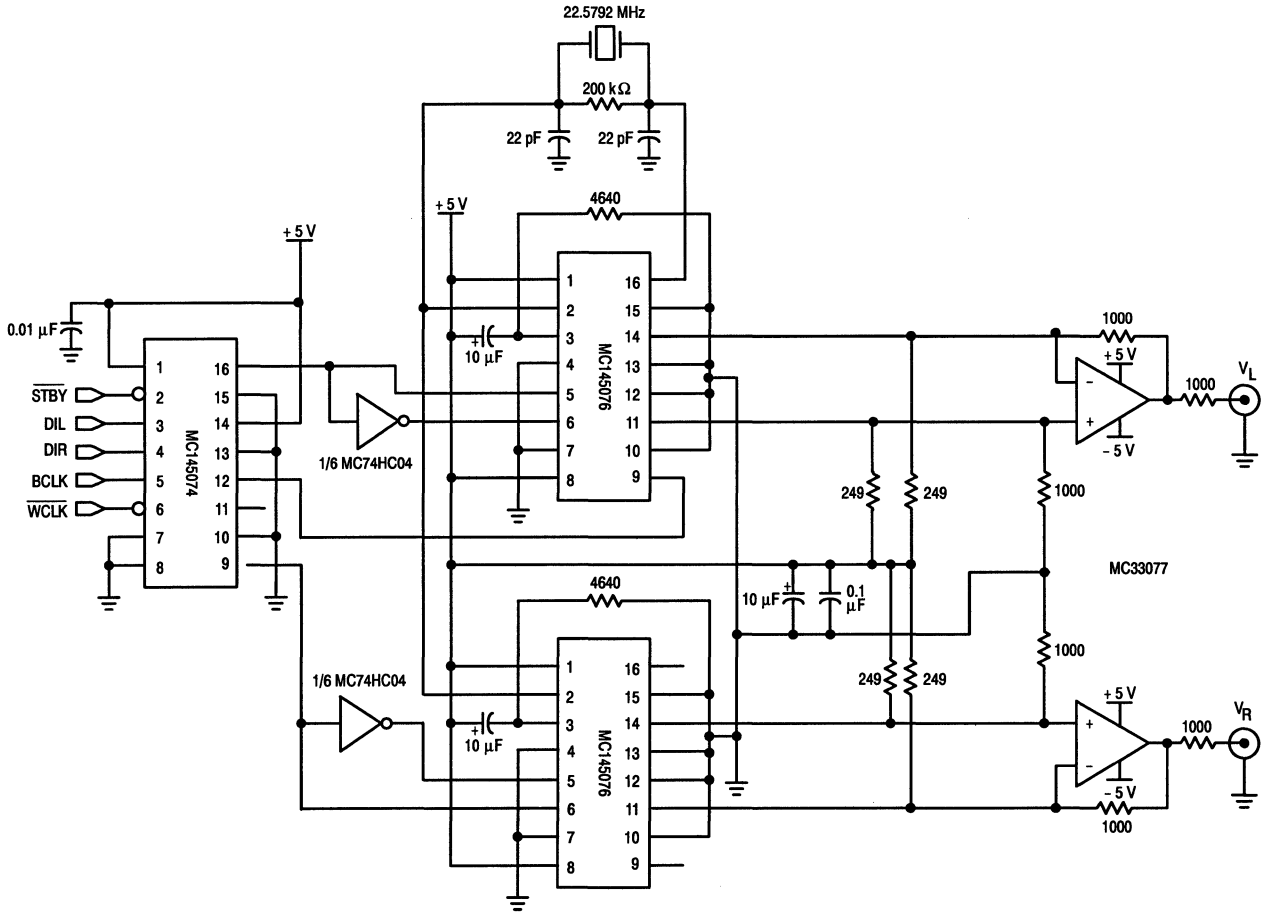
A smoothing filter is required when using a sigma–delta DAC to reduce the out–of–band noise, and to prevent the high frequencies from intermodulating to lower frequencies. Using the MC145076 with its current sink output is easier than a voltage output filter because it gives a degree of immunity to mutual ground paths between it and the next amplifier.

The circuit shown in Figure 2 is excellent for most applications. However, differential operation does reduce low level switching noise that appears as second harmonic distortion and weak background noise. Although a simple resistor on each current source output to V_{DDA} may be adequate for some applications, the OpAmps provide power supply noise rejection, and, in Figures 2 and 4, also reduce the signal swing on the current output pin of the part to further improve distortion.



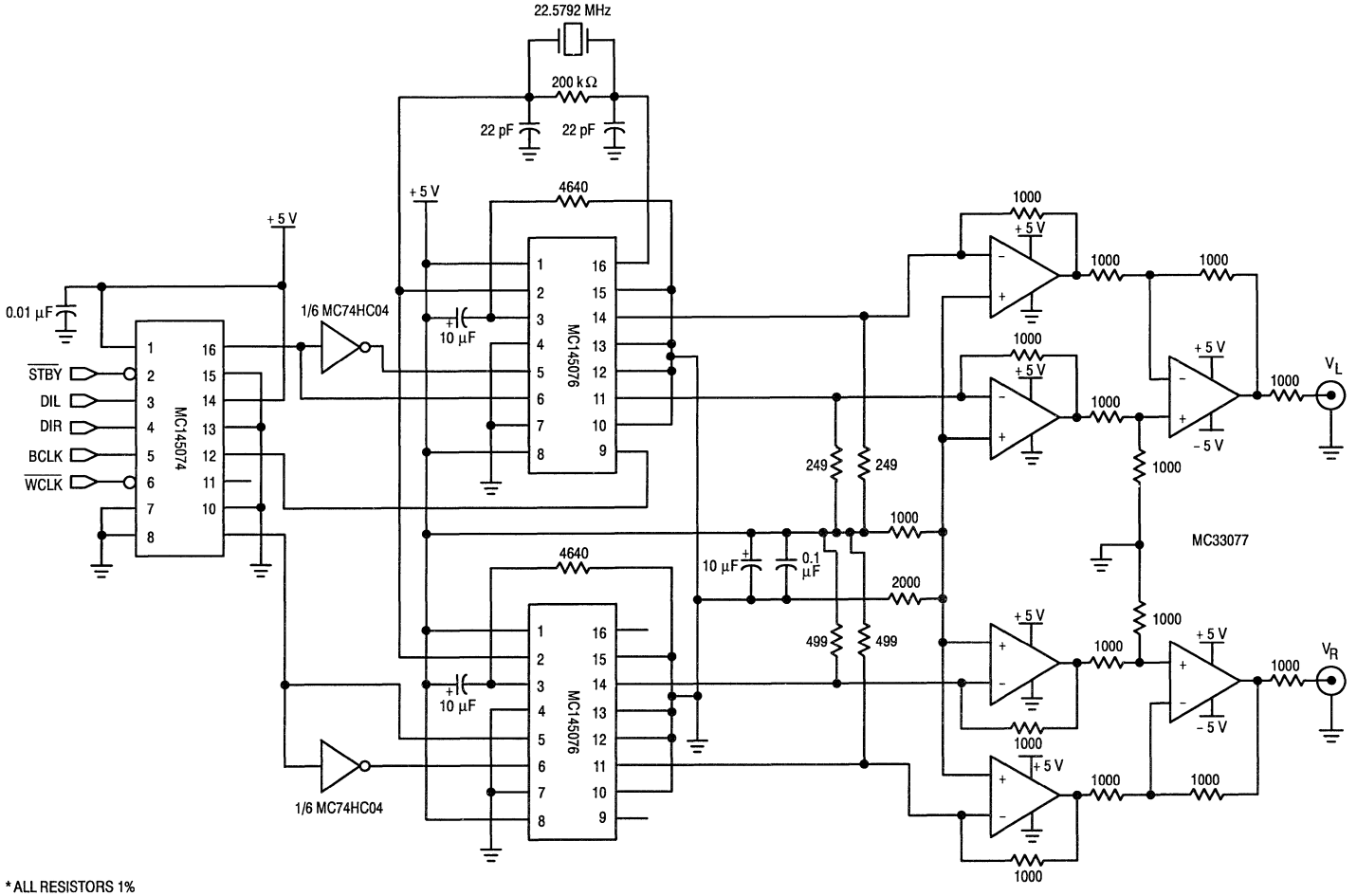
* ALL RESISTORS 1%

Figure 2. Low Cost +5 V Stereo Audio System, Typically 88 dB S/(N+D)



*ALL RESISTORS 1%

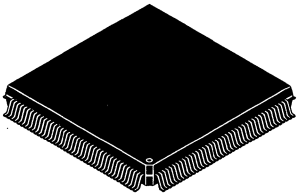
Figure 3. Mid Performance Stereo Audio System, Typically 98 dB S/(N+D)



*ALL RESISTORS 1%

Figure 4. High Performance Stereo Audio System, Typically 105 dB S/(N+D)

MCD212



FU SUFFIX
QFP PACKAGE
CASE 1007–01

ORDERING INFORMATION
MCD212FU QFP

2

Technical Summary

Video Decoder and System Controller (JTAG)

This technical summary provides a brief description of the MCD212 Video Decoder and System Controller with JTAG(VDSC/JTAG). A complete data sheet for the MCD212 is available and can be ordered from your local Motorola sales office. The order number is MCD212/D.

The MCD212 is a programmable, multi–scan video device capable of providing graphics imaging and system control in one low–cost package. *It is functionally equivalent to the MCD211 with the addition of JTAG testing.* The MCD212 is a drop–in replacement for the MCD211 if the JTAG functionality is not required. It is particularly well suited to low–cost consumer applications that require sophisticated graphics displays such as CD–i, CD–Karaoke, Video–On–Demand, and Set–Top Boxes. The main features of the device are as follows:

- Direct Interface to 680X0 Bus Compatible Devices
- 1 MByte ROM Control / 1 kbyte I/O Control
- Reset Sequencer, Including ROM Shadowing
- 4 MByte DRAM Direct Drive (256K x 4, 1M x 4, and 256K x 16 DRAM Types Supported)
- Up to 768 x 560 Screen Resolution
- Capability to Display Run–Length Coded Files
- 256 Entry Color Look Up Table (CLUT)
- Two Delta YUV Decoders
- Cursor Shape, Color, and Blink Control
- Overlaying of Four Video Planes with Special Effects via Weight Control, Priority Control, etc.
- Dynamic Programmable Registers and CLUT Reload in Retrace Period
- Digital RGB Output (8 Bits per Component)
- Synchronization with External Video (50 and 60 Hz Scan)
- 160–Pin Quad Flat Pack Plastic Package

NOTE: Supply of this Video–CD IC does not convey an implied license under any patent right to use this IC in any Video–CD application.

CD–i is a registered trademark of Philips Consumer Electronics.

DIFFERENCES BETWEEN THE MCD211 AND THE MCD212

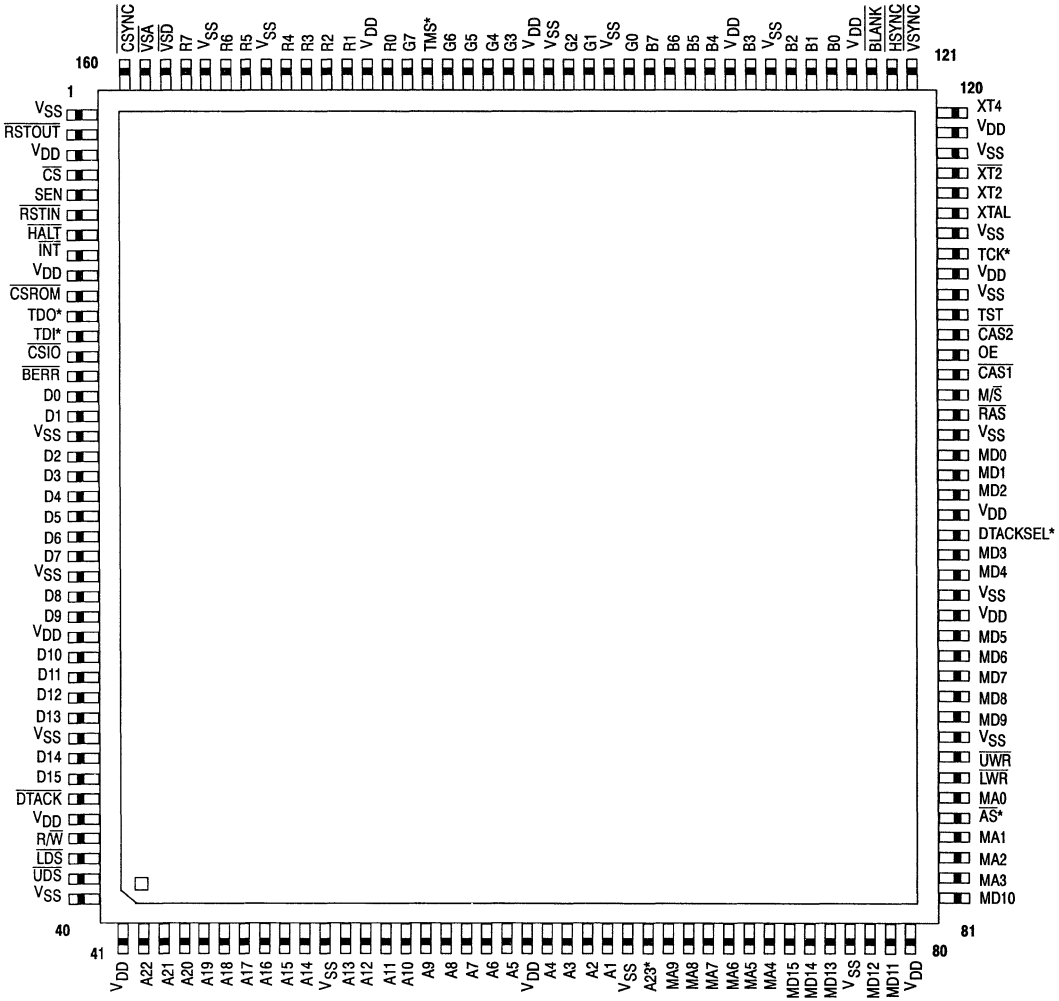
There are two differences between the parts:

1.) JTAG testing has been added for automated board testing. The additional pins required to do this were V_{SS} pins on the MCD211. Hence, the MCD212 can be put in place of an MCD211 and will function identically. The functionality of the R/$\overline{W}$, $\overline{LSD}$, $\overline{UDS}$, A1 – A22, $\overline{RAS}$ pins have been enhanced. (See **PIN DESCRIPTIONS** for the names of the new pins and the changes in functionality.)

2.) Also, the processor interface timing has been improved to allow operation with higher speed processors.

PIN ASSIGNMENT

NOTE: Pin differences between the MCD211 and MCD212 are denoted with an *.



VDSC OVERVIEW

GENERAL

The Video Decoder and System Controller with JTAG (VDSC/JTAG) is a CMOS device integrating a 680X0 family system controller and video graphics decoder, see Figure 1.

The VDSC is a programmable, multi–scan video device that can function as either a master or a slave. It can directly drive up to 5 Mbytes[1] of memory and provides chip–select signals for system ROM and peripherals. The on–chip DRAM controller can support up to 4 MByte of DRAM and controls access to the unspecialized System or Video DRAM. The CPU can access any memory location, even during active video display lines, thereby boosting system performance.

The video image is made up of four separate video planes: the cursor, two graphics planes (A and B), and one background plane. The video decoder receives two independent video channels from the Video DRAM. Each channel has a Real Time file decoder permitting the display of normal, run–length and mosaic compressed files. The resulting files can contain DYUV, CLUT, or direct RGB data. After decoding the resulting planes, A and B can be combined with a cursor and background allowing for visual effects like dissolves, mosaics, partial updates, etc. under software control. The resulting display is output in Red, Green, and Blue components, each being 8 bits in width. The display resolution is programmable up to 768 x 560.

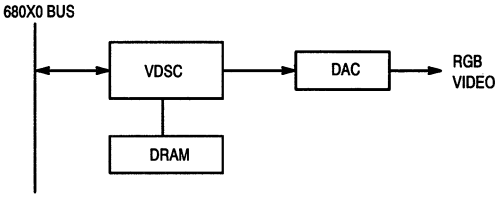
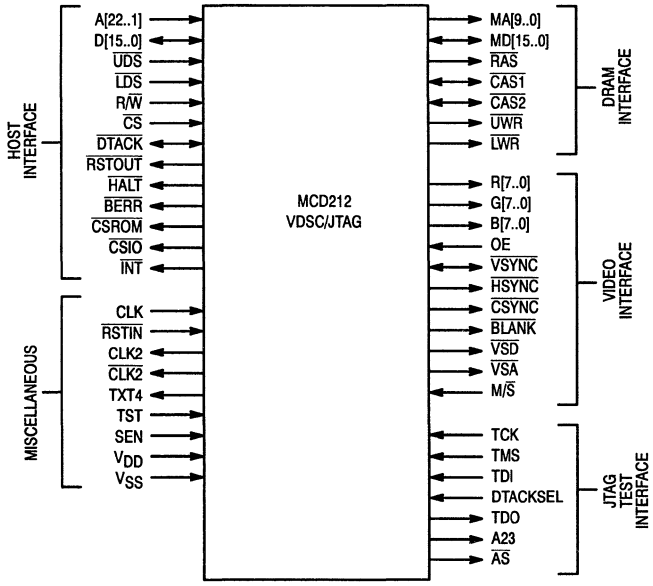


Figure 1. System Block Diagram

1. In this document a Word is defined as 16 bits and a Long–Word as 32 bits. Hexadecimal numbers are proceeded by an h.

PIN DESCRIPTION

PIN I/O



PIN DESCRIPTIONS

System Interface

Mnemonic	Type	Name and Function
A1 – A22	I	System ADDRESS lines. Provides address for access from the system bus. Must be stable when UDS and/or LDS are asserted.
D0 – D15	I/O	Bidirectional DATA bus, three–state. Used to transfer DATA between system bus and VDSC. Must be stable when $\overline{UDS}$ or $\overline{LDS}$ is asserted during write access. Driven by VDSC during Read cycles. D0 is the least significant bit.
$\overline{UDS}$	I	Upper Data Strobe. Active low. When asserted, $\overline{UDS}$ indicates that data is being addressed on D8 to D15.
$\overline{LDS}$	I	Lower Data Strobe. Active low. When asserted, $\overline{LDS}$ indicates that data is being addressed on D0 to D7.
R/$\overline{W}$	I	Read/Write. This input indicates transfer on the system bus. When low, indicates data is to be written into VDSC controlled resources or internal registers. When high, indicates a read is taking place.
$\overline{CS}$	I	Chip Select. Active low. When asserted, indicates data transfer between System bus and VDSC controlled resources is enabled. Validates address decode for system access.
$\overline{DTACK}$	I/O	DATA Transfer Acknowledge signal. Active low, three–state. Asserted by VDSC when the system bus cycle, concerning VDSC controlled resources, can be continued. This pin must be pulled up externally.
$\overline{RSTOUT}$	O	RESET Output. Active low, open drain. Asserted by the VDSC Reset Sequencer during the reset procedure. This pin must be pulled up externally.
$\overline{HALT}$	O	HALT line Output. Active low, open drain. Asserted by the VDSC Reset Sequencer during the reset procedure. This pin must be pulled up externally.
$\overline{BERR}$	O	BUS ERROR Output. Active low, three–state. Asserted when enabled by the VDSC Watch–dog timer circuit if $\overline{UDS}$ or $\overline{LDS}$ is still asserted at the end of the time–out period. This pin must be pulled up externally.
$\overline{CSROM}$	O	Chip Select ROM Output. Active low. Asserted by an access on the system bus in the ROM address area, and when $\overline{UDS}$ and/or $\overline{LDS}$ are asserted.
$\overline{CSIO}$	O	Chip Select I/O Output. Active low. Asserted by an access on the system bus in the I/0 area, and when $\overline{UDS}$ and/or $\overline{LDS}$ are asserted.
$\overline{INT}$	O	Interrupt request output. Active low, three–state. Used to generate interrupts to the CPU. This pin must be pulled up externally.

Dynamic RAM Interface

Mnemonic	Type	Name and Function
MA0 – MA9	O	Memory Address lines. Multiplexed ROW/COLUMN Address line outputs for DRAM control.
MD0 – MD15	I/O	Bidirectional Memory Data bus, three–state. Used to transfer data between DRAM bus and VDSC. Stable when $\overline{LWR}$ and/or $\overline{UWR}$ is asserted during a write cycle. Driven by VDSC during Read cycles. MD0 is the least significant bit.
$\overline{RAS}$	O	Row Address Strobe. Active low. Validates the DRAM row address on the falling edge.
$\overline{CAS1}$	I/O	Column Address Strobe for memory bank 1. Active low, three–state. Validates the DRAM column address on the falling edge. Input during reset sequence to select/deselect memory bank 1. Active High validates bank inputs.
$\overline{CAS2}$	I/O	Column Address Strobe for memory bank 2. Active low, three–state. Validates the DRAM column address on the falling edge. Input during reset sequence to select/deselect memory bank 2. Active High validates bank inputs.
$\overline{UWR}$	O	Write signal for DRAM. Active low. It is asserted when writing MD8 – MD15 to the DRAM.
$\overline{LWR}$	O	Write signal for DRAM. Active low. It is asserted when writing MD0 – MD7 to the DRAM.

Video Interface

Mnemonic	Type	Name and Function
R0 – R7	O	Red color output (R7 = MSB, R0 = LSB). Three–state.
G0 – G7	O	Green color output (G7 = MSB, G0 = LSB). Three–state.
B0 – B7	O	Blue color output (B7 = MSB, B0 = LSB). Three–state.
OE	I	Output Enable. Active high. It disables three–state of RGB output.
$\overline{\text{VSYNC}}$	I/O	Vertical Synchronization. Active low. In Master mode, this output is used as Vertical synchronization signal for monitor. In Slave TV mode it becomes a vertical synchronization Input.
$\overline{\text{HSYNC}}$	O	Horizontal Synchronization. Active low. This output is used as a horizontal synchronization signal.
$\overline{\text{CSYNC}}$	O	Composite synchronization. Active low. This output is used as a composite synchronization signal.
$\overline{\text{BLANK}}$	O	Blanking output. Active low. It is asserted during vertical and horizontal blanking periods and high the rest of the time.
$\overline{\text{VSD}}$	O	Video Select for Digital video. Active low. This signal is synchronous to the digital video output.
$\overline{\text{VSA}}$	O	Video Select for Analog video. Active low. This signal is a XT2 clock cycle delayed version of $\overline{\text{VSD}}$ and synchronous to analog video after clocked D/A conversion.
M/$\overline{\text{S}}$	I	Master/Slave TV mode selection input. When high the VDSC generates the video timing. When low the vertical synchronization can be slaved to an external video timing.

JTAG Test Signals

Mnemonic	Type	Name and Function
TCK	I	JTAG Test Clock Input. Provides the clock for the test logic defined by IEEE Std. 1149.1–1990. 100k Ohm internal pullup.
TMS	I	JTAG Test Mode Select Input. The signal decoded by the TAP controller to control test operations, defined by IEEE Std. 1149.1–1990. 100k Ohm internal pullup.
TDI	I	JTAGE Test Data Input. Pin at which serial test instructions and data are received by the test logic, defined by IEEE Std. 1149.1–1990. 100k Ohm internal pullup.
TDO	OT	JTAG Test Data Output. Three–state.Serial output for test instructions and data from the test logic defined by IEEE Std. 1149.1–1990.
A23	OT	System ADDRESS line (three–stated in functional mode). During JTAG EXTEST, A23 may drive system address line A23 off–chip.
$\overline{\text{AS}}$	OT	System ADDRESS STROBE (three–stated in functional mode). During JTAG EXTEST, $\overline{\text{AS}}$ may drive the system address strobe line $\overline{\text{AS}}$ off–chip.
DTACKSEL	I	Selects advance time of the falling edge of DTACK before data (read) is valid on pins D0 – D15. For designs using 68000/68070–16 or 68340/341–16 series processors, tie DTACKSEL low; for 68340/341–25 designs, tie DTACKSEL high.

Miscellaneous Signals

Mnemonic	Type	Name and Function
CLK	I	External clock Input.
$\overline{\text{RSTIN}}$	I	Reset input. Active low. Schmitt trigger. Initiates a reset sequence.
CLK2	O	CLK/2 clock output. Frequency is CLK frequency divided by 2.
$\overline{\text{CLK2}}$	O	CLK/2 clock output. Frequency is CLK frequency divided by 2. Inverse of XT2.
XT4	O	CLK/4 clock output. Frequency is CLK frequency divided by 4.
TST	I	Test input. Active high. Must be grounded to V_{SS} in normal operation.
SEN	I	Scan enable. Active high. Must be grounded to V_{SS} in normal operation.
V_{DD}	I	Power supply pins (5 Volts).
V_{SS}	I	Power and signal GROUND pins.

N.B. : All the pins are TTL compatible, except for XTAL and $\overline{\text{RSTIN}}$ which use CMOS levels.

PIN TYPES

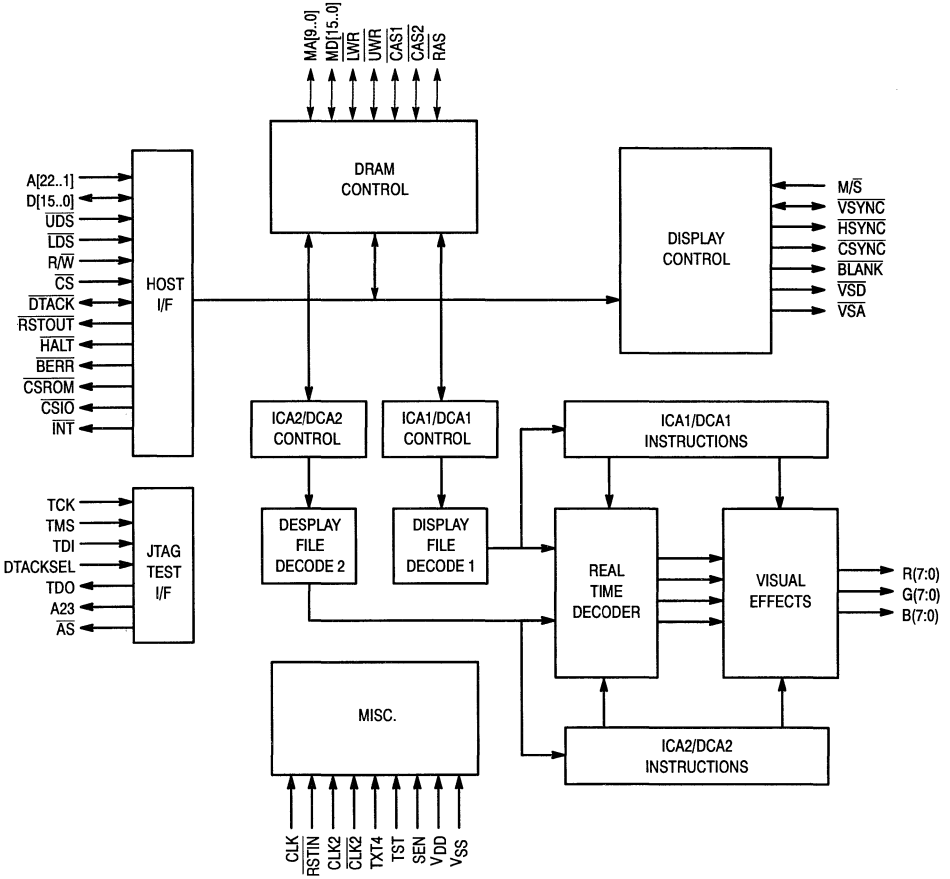
CMOS input	:CLK
CMOS Schmitt input	:$\overline{\text{RSTIN}}$
TTL input	:all inputs except XTAL, $\overline{\text{RSTIN}}$
6 mA output	:D0 – D15, $\overline{\text{RSTOUT}}$, $\overline{\text{HALT}}$, $\overline{\text{BERR}}$, $\overline{\text{INT}}$, MD0 – MD15, MA0 – MA9, $\overline{\text{LWR}}$, $\overline{\text{UWR}}$, R0 – R7, G0 – G7, B0 – B7, $\overline{\text{BLANK}}$, $\overline{\text{CSYNC}}$, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{VSD}}$, CLK2, $\overline{\text{CLK2}}$, CLK4
12 mA output	:$\overline{\text{CSIO}}$, $\overline{\text{CSROM}}$
16 mA output	:$\overline{\text{RAS}}$, $\overline{\text{CAS1}}$, $\overline{\text{CAS2}}$

HARDWARE AND SOFTWARE

2

The VDSC consists of 12 major blocks which are depicted in the Internal Block Diagram.

INTERNAL BLOCK DIAGRAM



INTERNAL FUNCTIONS

The VDSC contains two video graphics planes controllers. These two planes are independent, although they can be used together and combined to form a single external display. The internal functions consist of the ICA and DCA instruction decoder and control functions. The real–time decoder decodes Delta YUV natural images, CLUT (Color Look–Up Table), and Run–Length files.

EXTERNAL INTERFACES

The external interfaces are as follows:

- Host Interface
- DRAM Control
- Display Control
- Visual Effects
- Miscellaneous

Host Interface

The VDSC communicates with the host via the host interface. The host interface consists of a 16 bit wide bi–directional bus, the address bus, and all the necessary signals for interrupt, register access, and DMA.

DRAM Control

The VDSC has an on–chip Dynamic RAM controller. It supports several DRAM configurations (256K x 4, 1M x 4, and 256K x 16) up to 4 MByte and performs DRAM arbitration, address multiplexing, timing generation, refresh and controls access to the unspecialized system or video DRAM. The central processor can access any memory location, even during active video display lines, thereby boosting system performance.

Display Control

The video display is made up of four separate video planes: the cursor, two graphics planes (A and B), and one background plane. The video decoder receives two independent video channels from the Video DRAM. Each channel has a Real Time file decoder permitting the display of normal, run–length, and mosaic compressed files. The resulting files can contain DYUV, CLUT, or direct RGB data.

Visual Effects

The two graphics planes, A and B, from the display control can be combined with a cursor and background allowing for visual effects like dissolves, mosaics, partial updates, etc. under software control. The resulting display is output in Red, Green, and Blue components, each being 8 bits wide. The display resolution is programmable up to 768 x 560.

Miscellaneous

The miscellaneous block contains the clocking, timing, and chip control logic.

SOFTWARE

The VDSC is a very flexible video display processor. Visual special effects and display control are both under software control on either a display line by display line basis (DCA) or a field by field basis (ICA).

REGISTER MEMORY MAP

Name	Address (in Hex)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Read/Write, Write or Read Only
CSR1R	4FFFF1	x	x	x	x	x	x	x	x	DA	x	PA	x	x	x	x	x	READ
CSR2R	4FFFE1	x	x	x	x	x	x	x	x	x	x	x	x	x	IT1	IT2	BE	READ
CSR1W	4FFFF0	DI1	x	x	x	x	x	DD1	DD2	x	x	TD	x	DD	x	ST	BE	WRITE
CSR2W	4FFFE0	DI2	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	WRITE
DCR1	4FFFF2	DE	CF	FD	SM	CM1	0	IC1	DC1	x	x	*	*	*	*	*	*	WRITE
DCR2	4FFFE2	x	x	x	x	CM2	0	IC2	DC2	x	x	*	*	*	*	*	*	WRITE
DDR1	4FFFF8	x	x	x	x	MF1	MF2	FT1	FT2	x	x	*	*	*	*	*	*	WRITE
DDR2	4FFFE8	x	x	x	x	MF1	MF2	FT1	FT2	x	x	*	*	*	*	*	*	WRITE
VSR1	4FFFF4	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	WRITE
VSR2	4FFFE4	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	WRITE
DCP1	4FFFFA	*	*	*	*	*	*	*	*	*	*	*	*	*	*	x	x	WRITE
DCP2	4FFFEA	*	*	*	*	*	*	*	*	*	*	*	*	*	*	x	x	WRITE

ELECTRICAL SPECIFICATIONS

OPERATING RANGE

The limits for operating the device are as follows:

Ambient Temperature (T_A) ..... 0°C to 70°C
Voltage, V_{DD} ..... 5 V ± 10%
Voltage, V_{SS} ..... 0 V

ABSOLUTE MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, Unless Otherwise Noted)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	– 0.5	+ 7.0	V
V_I	Input Voltage	– 1.5	V_{DD} + 1.5	V
V_O	Output Voltage	– 0.5	V_{DD} + 0.5	V
I_O	Output Current	—	± 25	mA
P_d	Power Dissipation	—	1200	mW
T_{stg}	Storage Temperature	– 65	+ 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

2

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ± 10%, V_{SS} = 0 V, T_A = 0 to + 70°C, Unless Otherwise Noted)

Parameter	Symbol	Conditions	Min	Max	Unit
Operating Supply Current	I_{DD}	$V_I = V_{DD}$ or V_{SS} XTAL at 30.3 MHz	—	220	mA
Input Voltage (CMOS Input)	V_{IH} V_{IL}		0.7 V_{DD} —	— 0.3 V_{DD}	V
Input Voltage (TTL Input)	V_{IH} V_{IL}	V_{DD} = 4.5 V V_{DD} = 5.5 V V_{DD} = 5.5 V	2.0 2.2 —	— — 0.8	V
CMOS Schmitt Trigger Input Voltage	V_{T+} V_{T-}	V_{DD} = 4.5 V – 5.5 V	2.0 1.0	4.0 3.1	V
Hysteresis–Schmitt CMOS		V_{DD} = 4.5 V – 5.5 V	0.16 V_{DD}	0.33 V_{DD}	V
Input Leakage Current	I_{LI}	$V_I = V_{DD}$ or V_{SS}	– 5	5	µA
Output Voltage (6 mA output type)	V_{OH} V_{OL}	I_O = – 6 mA, V_{DD} = 4.5 V I_O = 6 mA, V_{DD} = 4.5 V	3.5 —	— 0.4	V
Output Voltage (12 mA Output Type)	V_{OH} V_{OL}	I_O = – 12 mA, V_{DD} = 4.5 V I_O = 12 mA, V_{DD} = 4.5 V	3.5 —	— 0.4	V
Output Leakage Current	I_{OZ}		– 10	10	µA
Input Capacitance	C_{in}	$V_{DD} = V_I$ = 0 V	—	15	pF
Output Capacitance	C_{out}		—	15	pF

VDSC/CD–i ARCHITECTURE

There are two different configurations of CD–i players currently on the market. The base case player does not support MPEG1 full motion video but uses the VDSC to generate the on–screen graphics and menu bars and short video clips using Delta YUV (DYUV) decoding. The extended player, on the other hand, also uses the VDSC in the same manner, but in addition, has an MCD270 (IMPEG) or MCD251 (FMV) chip on–board to provide MPEG1 Full Motion Video decoding (see Figure 2). In the extended player, the VDSC is the display master generating VSYNCs and HSYNCs and controlling overlays and display of the MPEG1 display (see Figure 3).

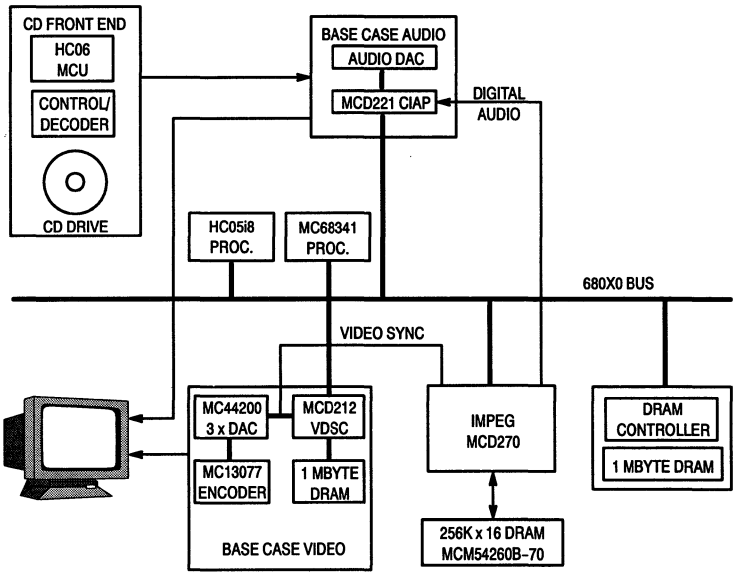


Figure 2. VDSC/CD–i Architecture

DIGITAL VIDEO MULTIPLEXING BETWEEN VDSC AND IMPEG AND AN AUDIO CONNECTION

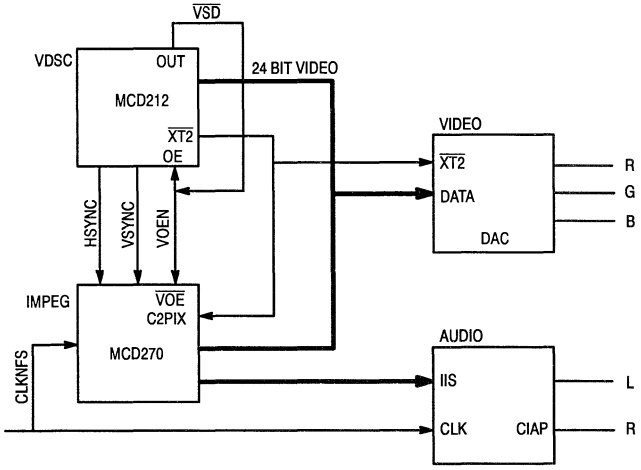


Figure 3. VDSC/CD–i Example

ANALOG VIDEO SWITCHING

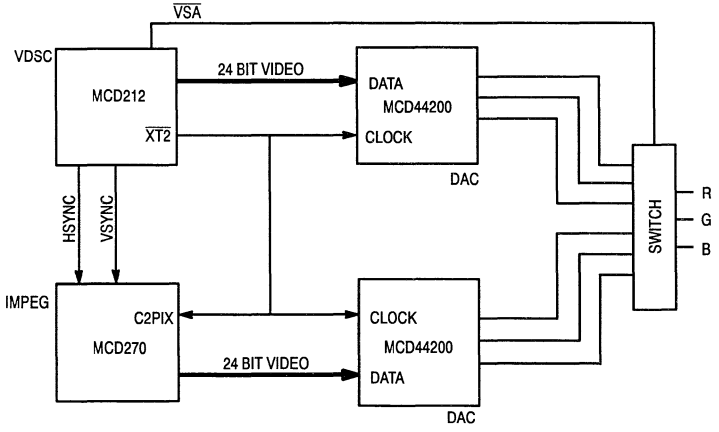


Figure 4. Analog Video Switching Example

VIDEO ON DEMAND

The VDSC/JTAG can be used in a video on demand (set-top box) application to provide a Graphical User Interface (GUI), to provide on–screen graphical displays, text, menus, or short Delta YUV or Run–Length encoded video clips as illustrated in Figure 5. The VDSC can interface with either a MPEG1 or MPEG2 full motion video display processor. In the example in Figure 5, an MPEG1 video and audio stream is carried over an asymmetric digital subscriber loop (ADSL) line in an MPEG2 transport stream. A transport stream decoder separates the conditional access data and the video and audio streams from the transport stream. The video and audio streams are directed to IMPEG and the conditional access data to the Smart Card controller. The on–screen display is generated by using an MCD212 (VDSC/JTAG). The video and audio output stages are identical to those in the CD–i application described earlier. Figure 5 also shows the MCD214 which can be used in place of the MCD211/212. It provides CCIR601 timing and makes interfacing to most MPEG2 video decoders simpler.

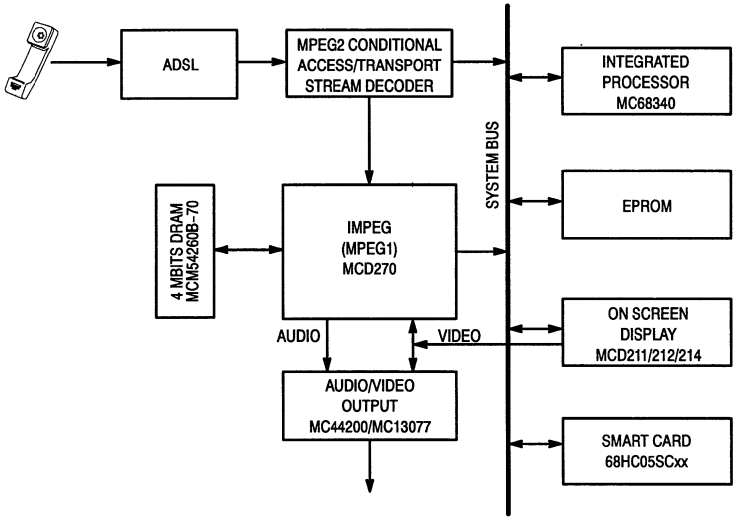
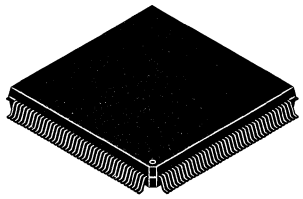


Figure 5. Video On Demand Example

MCD214

Technical Summary

Video Decoder And System Controller (VDSC)



FU SUFFIX
QFP PACKAGE
CASE 1007–01

ORDERING INFORMATION
MCD214FU QFP

This technical summary provides a brief description of the MCD214 Video Decoder and System Controller (VDSC). A complete data sheet for the MCD214 is available and can be ordered from your local Motorola sales office. The order number is MCD214/D.

The MCD214 is a CMOS device integrating a 68000/68300 family system controller and a CD–i video decoder and is designed for use in CD–i players, Digital Entertainment Terminals (Set–Top Boxes), and similar applications.

Features:

- Direct Interface to 680X0 Bus Compatible Devices
- 1 MByte ROM Control / 1 kbyte I/O Control
- Reset Sequencer, Including ROM Shadowing
- 4 MByte DRAM Direct Drive (256K x 4, 1M x 4, and 256K x 16 DRAM Types Supported)
- Up to 768 x 560 Screen Resolution
- Capability to Display Run–Length Coded Files
- 256 Entry Color Look Up Table (CLUT)
- Two Delta YUV Decoders
- Cursor Shape, Color, and Blink Control
- Overlaying of Four Video Planes with Special Effects via Weight Control, Priority Control, etc.
- Dynamic Programmable Registers and CLUT Reload in Retrace Period
- Digital RGB Output (8 Bits per Component)
- Synchronization with External Video (50 and 60 Hz Scan)
- 160–Pin Quad Flat Pack Plastic Package
- CCIR 656 Timing Compatible
- RGB and CbYCrY Multiplexed Inputs
- Digital RGB and YCrCb Outputs (8 Bits per Component)

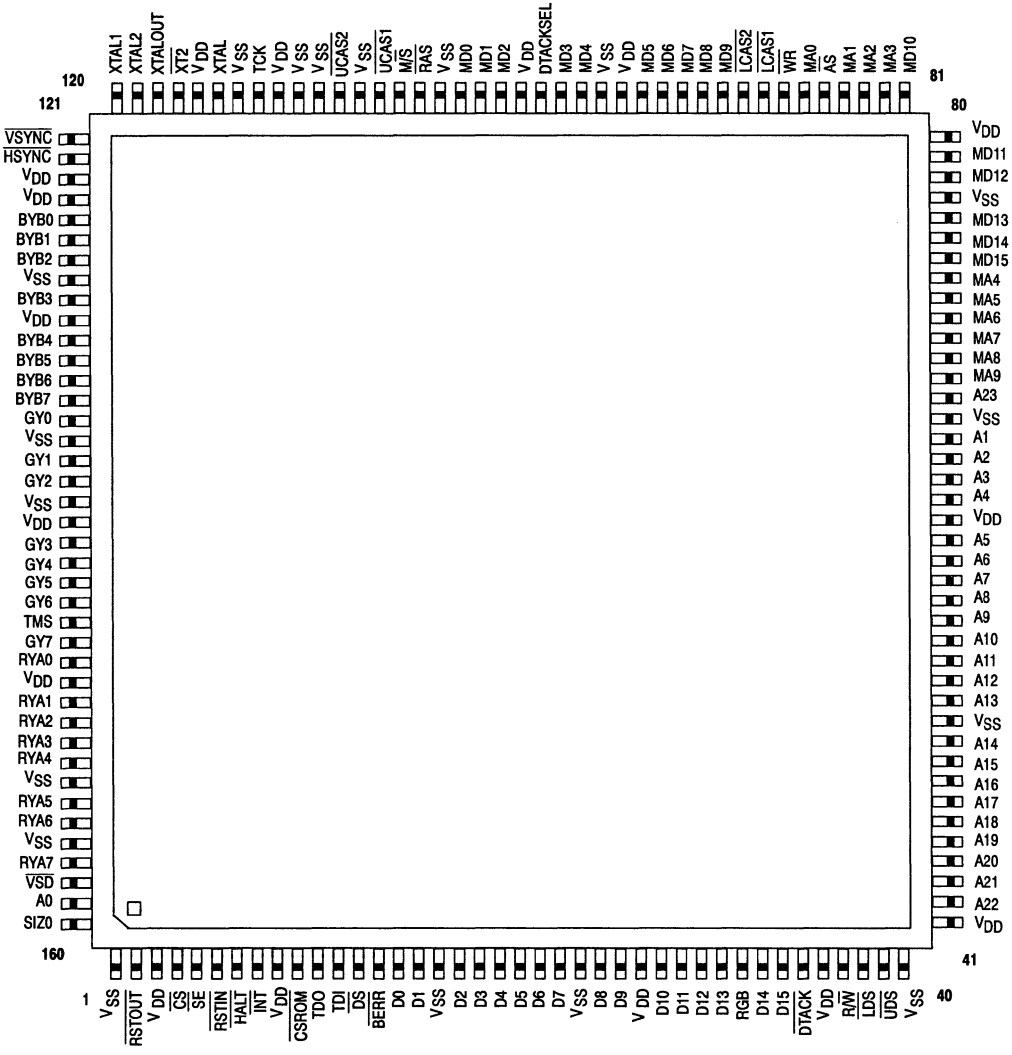
NOTE: Supply of this Video–CD IC does not convey an implied license under any patent right to use this IC in any Video–CD application.

CD–i is a registered trademark of Philips Consumer Electronics.

Functional Differences Between MCD212 and MCD214:

- The MDC214 incorporates a new display mode allowing operation with a 27 MHz input clock and producing a (double resolution) pixel rate of 13.5 MHz along a video line. Standard display resolution in this mode will be:
  360 pixels x 240/280 lines (normal resolution, non–interlace)
  720 pixels x 480/560 lines (double resolution, interlace)
- All standard and non–standard horizontal and vertical modes available in the MCD211 and MCD212 remain available in the MCD214 (PAL, NTSC).
- Two register bits are required to determine the crystal frequency used (CF, CF2). To allow optimal compatibility of new system modes with existing software titles (and vice–versa) two standard bits (ST, ST2) will determine how to display picture files prepared for use on other systems.
- Video output is selectable (not dynamically) between RGB and multiplexed C_bYC_rY formats, the latter being compatible with CCIR–656 format.
- In multiplexed mode, one of two incoming C_bYC_rY multiplexed video streams may be selected, under register control, to be mixed with the video graphics output. This multiplex, controlled internally by the $\overline{VSD}$ signal, will allow an additive mix of the graphic upon the incoming video stream, the latter taking the place of the backdrop. Switching can be restricted to occur only between co–sited C_bYC_rY samples.
- MCD214 may operate as video master, producing as outputs $\overline{HSYNC}$ and $\overline{VSYNC}$.
- MCD214 may operate as a slave to an alternative video master which shares the same system clock (SYNCHRONOUS slave mode). $\overline{VSYNC}$ and $\overline{HSYNC}$ are inputs. Under register control, one incoming $\overline{HSYNC}$ may be captured to initialize internal counters: $\overline{HSYNC}$ is thereafter monitored for erroneous timing or glitches. In this event MCD214 will be capable of generating an interrupt.
- MCD214 may also act as a slave to a video master which does not share the same system clock, e.g. another piece of video equipment (ASYNCHRONOUS slave mode). $\overline{VSYNC}$ is an input, $\overline{HSYNC}$ remains an output. $\overline{HSYNC}$ and the incoming $\overline{HSYNC}$ from the video master, drive an external Phase Locked Loop which regulates the frequency of the local clock XTAL. This effectively locks $\overline{HSYNC}$ to the incoming $\overline{HSYNC}$.
- In SYNCHRONOUS slave mode only, under register control, the display may be offset vertically and/or horizontally relative to the captured $\overline{HSYNC}$ and the incoming $\overline{VSYNC}$ signals. The shift is intended as a system–related function, not dynamically programmable by application.
- MCD214 may be programmed in slave mode to accept either field (pulse) or frame (square wave) format signals, the level of the latter indicating current field in interlace mode (field 1 or field 2).
- The system controller interface will be compatible with both 68000 and 68300 bus protocols and will be able to dynamically switch between these protocols, consistent with the functionality of the 68341 device.
- In RGB mode, when $\overline{VSD}$ is active, under ICA/DCA control, RGB outputs will be three–stated automatically using $\overline{VSD}$ (there is no OE pin). With $\overline{VSD}$ not active, RGB outputs will remain active and the backdrop color will be visible during display where appropriate.
- A clock–switching circuit within MCD214 allows selection between one of two clock frequencies, under control of the XS (crystal select) control bit. The clock switch will occur during blanked display, towards the end of the complete frame during which the change in XS occurred.
- MCD214 will only operate with 4–bit DRAM, or with 16–bit DRAM chips with two $\overline{CAS}$ inputs and one write–enable input (lower–byte $\overline{CAS}$/upper–byte $\overline{CAS}$/write enable). Note that MCD211 and MCD212 accommodate 16–bit DRAMs with a single CAS input and two write enable inputs (upper and lower byte).
- The following pin functions present in MCD212 will not be implemented in MCD214:
  $\overline{CSYNC}$, $\overline{BLANK}$, $\overline{CSIO}$, OE, $\overline{VSA}$, XT2, XT4.
- The design of the MCD214 will ensure that where possible, the device will be backwards compatible with MCD211 and MCD212 with respect to both function and pinout.

PIN ASSIGNMENT



SIGNAL DESCRIPTIONS
System Interface

Mnemonic	Type	Name and Function
A0 ... A22	I/O	System ADDRESS lines (SIMPLE INPUTS in functional mode). Provides address for access from the system bus. Must be stable when $\overline{UDS}$ and/or $\overline{LDS}$ are asserted or when $\overline{DS}$ is asserted (68300 protocol). During JTAG EXTEST, A0 ... A22 may drive system address lines A0 ... A22 off–chip.
D0 ... D15	I/O	Bidirectional DATA bus, three–state. Used to transfer DATA between system bus and the MCD214. Must be stable when $\overline{UDS}$ or $\overline{LDS}$ is asserted during write access. Driven by the MCD214 during Read cycles. D0 is the least significant bit.
$\overline{UDS}$	I/O	Upper Data Strobe (SIMPLE INPUT in functional mode). Active low. When asserted, $\overline{UDS}$ indicates that data is being addressed on D8 to D15 (68000 protocol). During JTAG EXTEST, $\overline{UDS}$ may drive the $\overline{UDS}$ line off–chip.
$\overline{LDS}$	I/O	Lower Data Strobe (SIMPLE INPUT in functional mode). Active low. When asserted, $\overline{LDS}$ indicates that data is being addressed on D0 to D7 (68000 protocol). During JTAG EXTEST, $\overline{LDS}$ may drive the $\overline{LDS}$ line off–chip.
$\overline{DS}$	I/O	Data Strobe (SIMPLE INPUT in functional mode). Active low. When asserted, $\overline{DS}$ indicates that data is being addressed. DSN is asserted if the 68300 bus protocol is used. If a single byte of data is transferred (SIZ0 = 1), A0 indicates whether data is being addressed on D0 to D7 (A0 = 1) or on D8 to D15 (A0 = 0). During JTAG EXTEST, $\overline{DS}$ may drive the $\overline{DS}$ line off–chip.
SIZ0	I/O	Transfer Size (SIMPLE INPUT in functional mode). Indicates the number of bytes remaining to be transferred. When low, indicates Word (two bytes) transfer. When high, indicates Single Byte transfer. During JTAG EXTEST, SIZ0 may drive the SIZ0 line off–chip.
R/$\overline{W}$	I/O	Read/Write (SIMPLE INPUT in functional mode). The input signal indicates a transfer on the system bus. When low, it indicates data is to be written into MCD214 controlled resources or internal registers. During JTAG EXTEST, R/$\overline{W}$ may drive the R/$\overline{W}$ line off–chip.
DTACKSEL	I/O	Selects advance time of falling edge of DTACK before data is valid on pins D0 – D15. (See AC Electrical Characteristics, timings 22, 22a.) For designs using 68000/68070–16 or 68340/341–16 series processors, tie DTACKSEL low; for 68340/341–25 designs tie DTACKSEL high.
$\overline{CS}$	I	Chip Select. Active low. When asserted, indicates data transfer between system bus and MCD214 controlled resources is enabled. Validates address decode for system access.
$\overline{DTACK}$	I/O	DATA Transfer Acknowledge signal. Active low, three–state. Asserted by the MCD214 when the system bus cycle, concerning MCD214 controlled resources, can be continued. This pin must be pulled up externally.
$\overline{RSTOUT}$	O/D	RESET Output. Active low, open drain. Asserted by the MCD214 Reset Sequencer during the reset procedure. This pin must be pulled up externally.
$\overline{HALT}$	O/D	HALT Line Output. Active low, open drain. Asserted by the MCD214 Reset Sequencer during the reset procedure. This pin must be pulled up externally.
$\overline{BERR}$	O/T	BUS ERROR Output. Active low, three–state. Asserted when enabled by the MCD214 Watch–dog timer circuit if data strobes ($\overline{DS}$ or $\overline{UDS}$/$\overline{LDS}$) are still asserted at the end of the time–out period. This pin must be pulled up externally.
$\overline{CSROM}$	O	Chip Select ROM Output. Active low. Asserted by an access to an address in the range $4FFBFF.

$\overline{\text{INT}}$	O/T	Interrupt request output. Active low, three–state. Used to generate interrupts to the CPU. This pin must be pulled up externally.

Dynamic RAM Interface

Mnemonic	Type	Name and Function
MA0 ... MA9	O	Memory Address lines. Multiplexed ROW/COLUMN Address line outputs for DRAM control.
MD0 ... MD15	I/O	Bidirectional Memory Data bus, three–state. Used to transfer data between DRAM bus and the MCD214. Stable when $\overline{\text{WR}}$ is asserted during a write cycle. Driven by the MCD214 during Read cycles. MD0 is the least significant bit.
$\overline{\text{RAS}}$	O/T	Row Address Strobe (cannot be three–stated in functional mode). Active low. Validates the DRAM row address on the falling edge. In JTAG mode, $\overline{\text{RAS}}$ may be placed in an inactive drive (high impedance) state.
$\overline{\text{UCAS1}}$	I/O	Column Address Strobe for upper byte of DRAM memory bank 1. It is asserted when reading, and when writing MD8 ... MD15 of DRAM bank 1. Active low, three–state. Validates the DRAM column address on the falling edge. It is an input during reset sequence to select/deselect memory bank 1. Active high validates the bank.
$\overline{\text{UCAS2}}$	I/O	Column Address Strobe for upper byte of DRAM memory bank 2. It is asserted when reading, and when writing MD8 ... MD15 of DRAM bank 2. Active low, three–state. Validates the DRAM column address on the falling edge. It is an input during reset sequence to select/deselect memory bank 2. Active high validates the bank.
$\overline{\text{LCAS1}}$	I/O	Column Address Strobe for lower byte of DRAM memory bank 1. It is asserted when reading, and when writing MD0 ... MD7 of DRAM bank 1. Active low, three–state. Validates the DRAM column address on the falling edge.
$\overline{\text{LCAS2}}$	I/O	Column Address Strobe for lower byte of DRAM memory bank 2. It is asserted when reading, and when writing MD0 ... MD7 of DRAM bank 2. Active low, three–state. Validates the DRAM column address on the falling edge.
$\overline{\text{WR}}$	O	Write signal for DRAM. Active low.

Video Interface

Mnemonic	Type	Name and Function
RGB	I	RGB/CCIR–601 output mode select. To be connected to V_{DD} to select RGB output mode, or V_{SS} to select CCIR–601 output mode. Connection to V_{SS} ensures no contention occurs at power–up on the CCIR–601 input lines R_YA(7:0) and B_YB(7:0). (These are configured as outputs in RGB mode.)
R_YA(7:0)	I/O	RGB = 1: Red color output (R7 = MSB, R0 = LSB). Three–state. RGB = 0: Multiplexed Luminance and Chrominance inputs for incoming video stream A. To be internally multiplexed with CCIR–601 graphics.
G_Y(7:0)	O/T	RGB = 1: Green color output (G7 = MSB, G0 = LSB). Three–state. RGB = 0: Multiplexed Luminance and Chrominance output (CCIR–601 compatible). First pixel on line is C_b, followed by Y, C_r, Y. This repeats for the duration of the line.
B_YB(7:0)	I/O	RGB = 1: Blue color output (B7 = MSB, B0 = LSB). Three–state. RGB = 0: Multiplexed Luminance and Chrominance inputs for incoming video stream B. To be internally multiplexed with CCIR–601 graphics.

$\overline{\text{VSYNC}}$	I/O	Vertical Synchronization. Active low. In master mode, this output is used as Vertical Synchronization signal for monitor. In slave TV mode it becomes a Vertical Synchronization Input.
$\overline{\text{HSYNC}}$	I/O	Horizontal Synchronization. Active low. In master mode, this output is used as Horizontal Synchronization signal for the monitor. In slave TV mode it becomes a Horizontal Synchronization input.
$\overline{\text{VSD}}$	O	Video Select for Digital video. Active low. This signal is synchronous to the digital video output.
M/$\overline{\text{S}}$	I	Master/Slave TV mode selection input. When high the MCD214 generates the video timing. When low, synchronization can be slaved to an external video timing source.

2

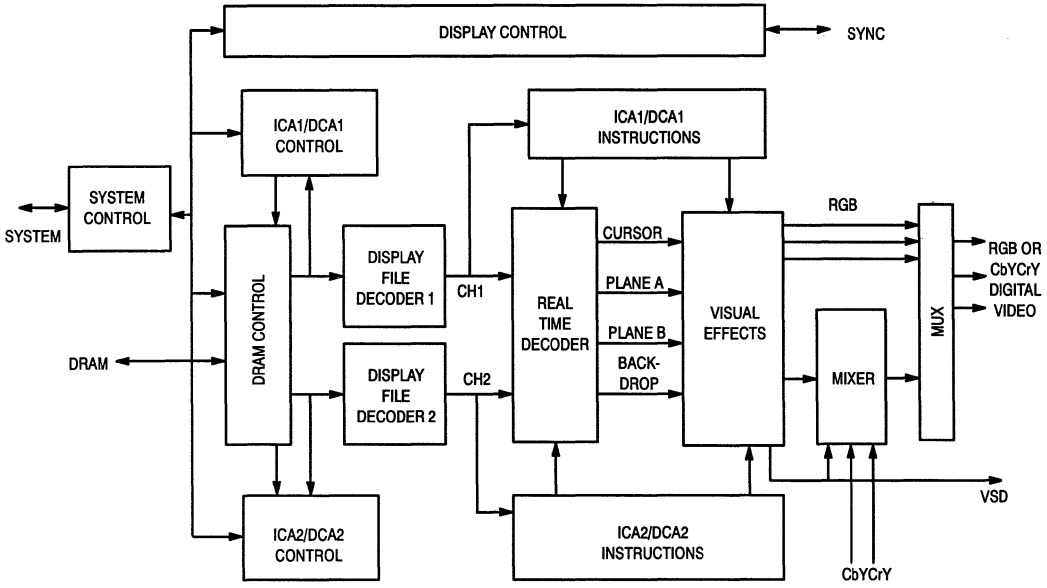
Miscellaneous Signals

Mnemonic	Type	Name and Function
XTAL	I	External clock input.
XTAL1	I	Clock input to clock switching circuit. Selected by XS = 0.
XTAL2	I	Clock input to clock switching circuit. Selected by XS = 1.
XTALOUT	O	Output for selected clock (XTAL1 or XTAL2).
$\overline{\text{RSTIN}}$	I	Reset input. Active low. Schmitt trigger. Initiates a reset sequence.
$\overline{\text{XT2}}$	O	XTAL/2 clock output. Frequency is XTAL frequency divided by 2.
TST	I	Test input. Active high. Must be grounded to V_{SS} in normal operation.
SEN	I	Scan enable. Active high. Must be grounded to V_{SS} in normal operation.

JTAG Specific Pins

Mnemonic	Type	Name and Function
TCK	I	JTAG Test Clock Input. Provides the clock for the test logic defined by IEEE Std 1149.1–1990.100 k ohm internal pull–up.
TMS	I	JTAG Test Mode Select Input. The signal decoded by the TAP controller to control test operations, defined by IEEE Std 1149.1–1990. 100 k ohm internal pull–up.
TDI	I	JTAG Test Data Input. Pin at which serial test instructions and data are received by the test logic, defined by IEEE Std 1149.1–1990. 100 k ohm internal pull–up.
TDO	O/T	JTAG Test Data Output. Three–state. Serial output for test instructions and data from the test logic defined in the IEEE Std 1149.1–1990.
A23	O/T	System ADDRESS line (three–stated in functional mode). During JTAG EXTEST, A23 may drive system address line A23 off–chip.
$\overline{\text{AS}}$	O/T	System ADDRESS STROBE (three–stated in functional mode). During JTAG EXTEST, $\overline{\text{AS}}$ may drive system address strobe line off–chip.
V_{DD}	I	Power supply pins (5 volts).
V_{SS}	I	Power and signal ground pins.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The MCD214 is a CMOS device integrating a 68000/68300 family system controller and CD–i video decoder.

Used with a 68341 processor, the MCD214 will be able to decode both 68000 protocol and 68300 protocol read/write accesses.

The MCD214 can directly drive up to 5 Mbytes of memory and provides chip select signals for system ROM and peripherals. The on–chip DRAM controller can support up to 4 MBytes of DRAM and control access to the unspecialized System or Video DRAM. The CPU can access any memory location even during active video display lines, thus boosting system performance.

The video decoder receives two independent video channels from the Video DRAM. Each channel has a real time file decoder permitting the display of normal, run–length, and mosaic compressed files. The resulting files can contain DYUV, CLUT, or direct RGB data. After decoding, the resulting planes A and B can be combined with a cursor and backdrop allowing for visual effects like dissolves, mosaics, partial updates, etc. under software control. The resulting display is available in Red, Green, and Blue components, 8 bits each.

Alternatively the output is available in multiplexed C_bYC_rY format, in this case one of two incoming multiplexed data streams may be internally mixed with the graphics, replacing the backdrop (typically used to superpose MCD214 graphics upon a digital moving picture).

The display resolution is programmable up to 768 pixels horizontally x 560 lines vertically.

The MCD214 has a JTAG boundary scan interface, compliant with the rules and specifications of IEEE Std 1149.1–1990 (May 1990), accommodating boundary scan instructions EXTEST, SAMPLE–PRELOAD, IDCODE, BYPASS.

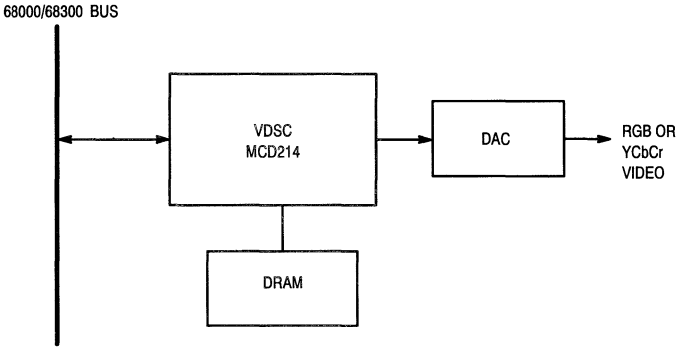


Figure 1. Subsystem Using the MCD214

Table 1. Channel 1

Address (HEX)	Register	Description
$4FFFF1	CSR1R	Status register 1
$4FFFF0	CSR1W	Control register 1
$4FFFF2	DCR1	Display command register 1
$4FFFF4	VSR1	Video start register 1
$4FFFF8	DDR1	Display decoder register 1
$4FFFFA	DCP1	DCA pointer 1

Table 2. Channel 2

Address (HEX)	Register	Description
$4FFFE1	CSR2R	Status register 2
$4FFFE0	CSR2W	Control register 2
$4FFFE2	DCR2	Display command register 2
$4FFFE4	VSR2	Video start register 2
$4FFFE8	DDR2	Display decoder register 2
$4FFFEA	DCP2	DCA pointer 2

Table 3. Generic

Address (HEX)	Register	Description
$4FFFDC	VDO	Vertical display offset
$4FFFDE	HDO	Horizontal display offset

ELECTRICAL SPECIFICATIONS

OPERATING RANGE

The limits for operating the device are as follows:

Ambient Temperature (T_A) ..... 0°C to 70°C
Voltage, V_{DD} ..... 5 V ± 10%
Voltage, V_{SS} ..... 0 V

ABSOLUTE MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, Unless Otherwise Noted)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	– 0.5	+ 7.0	V
V_I	Input Voltage	– 1.5	V_{DD} + 1.5	V
V_O	Output Voltage	– 0.5	V_{DD} + 0.5	V
I_O	Output Current	—	± 25	mA
P_d	Power Dissipation	—	1200	mW
T_{stg}	Storage Temperature	– 65	+ 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ± 10%, V_{SS} = 0 V, T_A = 0 to + 70°C, Unless Otherwise Noted)

Parameter	Symbol	Conditions	Min	Max	Unit
Operating Supply Current	I_{DD}	$V_I = V_{DD}$ or V_{SS} XTAL at 30.3 MHz	—	TBD	mA
Input Voltage (CMOS Input)	V_{IH} V_{IL}		0.7 V_{DD} —	— 0.3 V_{DD}	V
Input Voltage (TTL Input)	V_{IH} V_{IL}		2.0 —	— 0.8	V
CMOS Schmitt Trigger Input Voltage	V_{T+} V_{T-}	V_{DD} = 4.5 V – 5.5 V	2.0 1.5	3.4 2.6	V
Hysteresis–Schmitt CMOS		V_{DD} = 4.5 V – 5.5 V	0.11 V_{DD}	0.18 V_{DD}	V
Input Leakage Current	I_{LI}	$V_I = V_{DD}$ or V_{SS}	– 1.0	1.0	µA
Output Voltage (4 mA Output Type)	V_{OH} V_{OL}	I_O = – 4 mA, V_{DD} = 4.5 V I_O = 4 mA, V_{DD} = 4.5 V	3.7 —	— 0.4	V
Output Voltage (8 mA Output Type)	V_{OH} V_{OL}	I_O = – 8 mA, V_{DD} = 4.5 V I_O = 8 mA, V_{DD} = 4.5 V	3.7 —	— 0.4	V
Output Voltage (16 mA Output Type)	V_{OH} V_{OL}	I_O = – 16 mA, V_{DD} = 4.5 V I_O = 16 mA, V_{DD} = 4.5 V	3.7 —	— 0.4	V
Output Leakage Current	I_{OZ}		– 5.0	5.0	µA
Input Capacitance	C_{in}	V_{DD} = V_I = 0 V	—	10	pF
Output Capacitance	C_{out}		—	12.5	pF

VIDEO ON DEMAND

In the Video On Demand example shown below, the MCD270 may be used as the decoder section of a video on demand integrated receiver decoder. MPEG1 video and audio streams are carried over an asymmetric digital subscriber loop (ADSL) in an MPEG2 transport stream. A transport stream decoder separates the conditional access data and the video and audio streams from the transport stream. The video and audio streams are directed to the MCD270 and the conditional access data to the smart card controller. The on–screen display is generated by the MCD214.

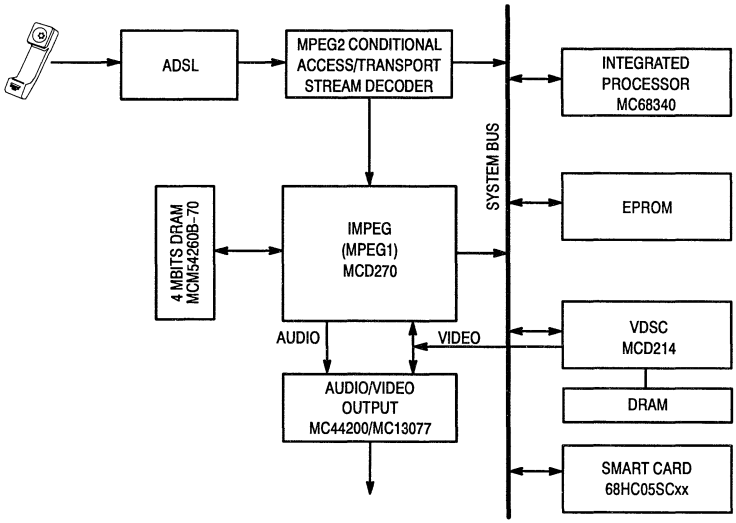
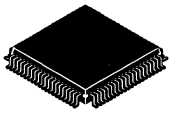


Figure 2. Video on Demand Example

MCD221

Technical Summary

CD–Interface and Audio Processor (CIAP)



FU SUFFIX
QFP PACKAGE
CASE 841B–01

ORDERING INFORMATION

MCD221FU	QFP

2

This technical summary provides a brief description of the MCD221 CD–Interface and Audio Processor. A complete data sheet for the MCD221 is available and can be ordered from your local Motorola sales office. The order number is MCD221/D.

The MCD221 has two main functions. The first is to form an interface between a CD drive unit and a CD–i or Photo–CD player. The connection to the drive is designed for both applications and can be either a Digital Out (EBU standard) interface, or an I^2S plus subcode interface. The host interface can be either a 68000 interface for CD–i players, or a serial (SPI) interface for Photo–CD.

The second function of the MCD221 is to decode ADPCM (CD–i base case) audio, to perform audio mixing functions as specified in the Green Book, and to be able to add external audio to the base case audio. The MCD221 can also be used for handling the ADPCM decoding for Photo–CD.

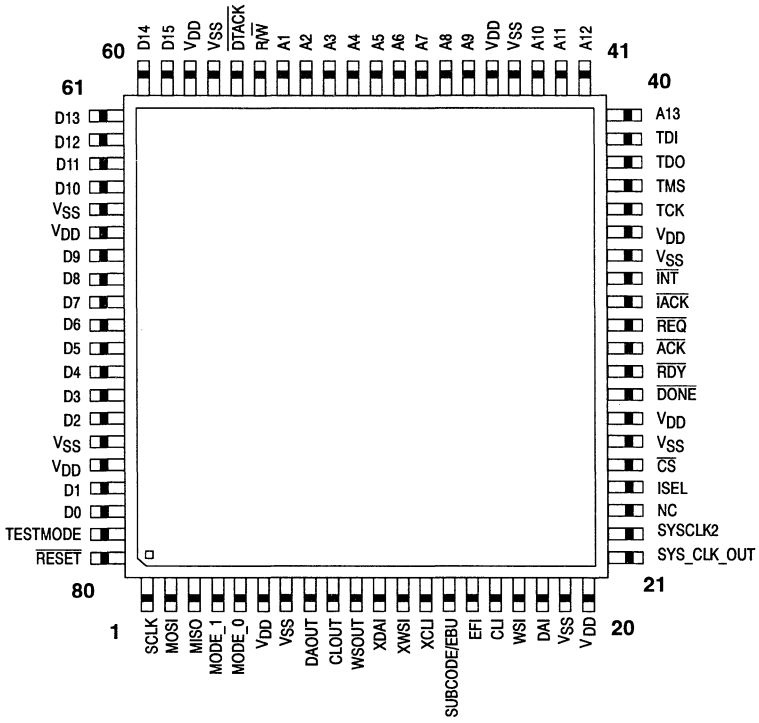
The main features of the MCD221 are as follows:

- Accepts Audio Inputs in I^2S Format (MPEG1) for Mixing with CIAP Internal Audio
- Output Can Be Either I^2S or SONY Format
- Data Input Rate Can Be Up to 2 Times Normal Speed
- Can Connect to a Host via Either a 68K or Serial Interface
- 80–Pin Quad Flat Pack (QFP)

NOTE: Supply of this Video–CD IC does not convey an implied license under any patent right to use this IC in any Video–CD application.

CD–i is a registered trademark of Philips Consumer Electronics.

PIN ASSIGNMENT



SIGNAL DESCRIPTIONS

Host Interface

Mnemonic	Type	Name and Function
A[13 ... 1]	O	System Address Bus. The address must be stable before $\overline{CS}$ is asserted. Active HIGH.
D[15 ... 0]	B	System Data Bus. The data lines must be stable when $\overline{CS}$ is active during a write and before $\overline{DTACK}$ is asserted during a read. Tri–state.
$\overline{CS}$	I	Chip Select. Used to access the CIAP internal registers and buffers. Active LOW.
R/$\overline{W}$	I	Read/$\overline{Write}$. Indicates the direction of the data transfer. When LOW, the transfer is to the CIAP.
$\overline{DTACK}$	B	Data Transfer Acknowledge. Active LOW. During normal host access, $\overline{DTACK}$ is an output indicating that data has been put on (read cycles) or read from (write cycles) the data bus. (Active pullup.) During DMA, $\overline{DTACK}$ is an input indicating that the memory has put data on the data bus.
$\overline{INT}$	O	Interrupt. Released when the interrupt status register is read. Active LOW.
$\overline{IACK}$	I	Interrupt Acknowledge. Active LOW.
$\overline{REQ}$	O	DMA Request. Active LOW.
$\overline{ACK}$	I	Acknowledge. DMA handshake signal indicating that the bus is available for data transfer. Active LOW.
$\overline{RDY}$	O	Ready. DMA handshake signal indicating that the CIAP has completed the data transfer. Tri–state. Active LOW. When released by the CIAP, the output is forced high for a few nanoseconds before it is made tri–state.
$\overline{DONE}$	I	Done. Indicates the last transfer of a DMA burst. Active LOW.

Serial Interface

Mnemonic	Type	Name and Function
SCLK	I	Serial Clock.
MOSI	I	Serial Data. Master out, slave in.
MISO	O	Serial Data. Master in, slave out.
MODE_0, MODE_1	I	Serial Interface MODE bits. 00 = Write selected register 01 = Read selected register 10 = Write address 11 = No action

Data Input

Mnemonic	Type	Name and Function
CLI	I	Serial Bit Clock Input.
WSI	I	Word Clock Input.
DAI	I	Serial Data Input.
EFI	I	Error Flag Input.
SUBCODE/EBU	I	Subcode (P ... W) serial data input or EBU input for both main channel and subchannel.

External Audio Interface

Mnemonic	Type	Name and Function
XCLI	I	External Audio Serial Bit Clock Input. When not used, the pin must be connected to V_{CC} or V_{SS}.
XWSI	I	External Audio Word Clock Input. When not used, the pin must be connected to V_{CC} or V_{SS}.
XDAI	I	External Audio Data Input. When not used, the pin must be connected to V_{CC} or V_{SS}.

Audio Output Interface

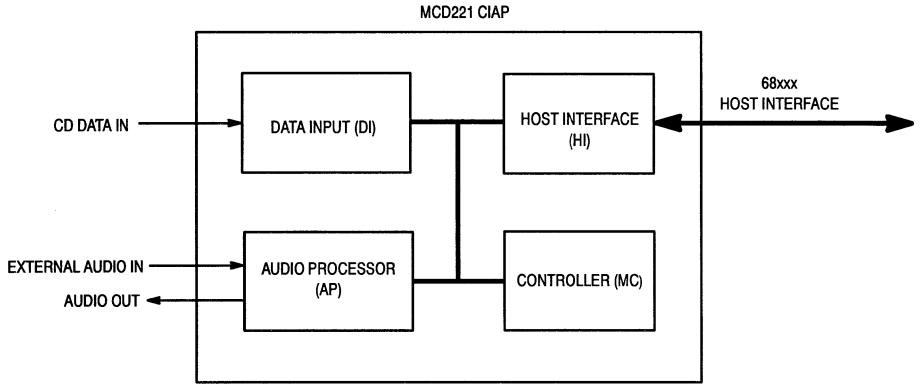
Mnemonic	Type	Name and Function
CLOUT	O	Audio Output Serial Clock.
WSOUT	O	Audio Output Word Clock.
DAOUT	O	Audio Output Serial Data.

General

Mnemonic	Type	Name and Function
SYS_CLK_OUT	O	16.9344 MHz System Clock Output.
SYSCLK2	I	Double System Clock Frequency Input. Input for an oscillator with a frequency of 33.8688 MHz.
$\overline{\text{RESET}}$	I	Reset. Global reset for the CIAP. Active LOW.
ISEL	I	Interface Select. 0 = Serial interface (no parallel access possible) 1 = 68000 interface (no serial access possible)
TDI	I	Test Data Input. (Boundary scan input pin.)
TDO	O	Test Data Output. (Boundary scan output pin.)
TCK	I	Test Clock. (Boundary scan input pin.)
TMS	I	Test Mode Select. (Boundary scan input pin.)
TESTMODE	O	When 0, the CIAP is operational. When 1, the CIAP is in test mode.

FUNCTIONAL DESCRIPTION

DATA FLOW DIAGRAM



The MCD221 Data Flow Diagram should be used in conjunction with the following notes which outline the function of the various blocks within the device:

- The **data input module** consists of two parts; a main channel decoder and a subchannel decoder. Both decoders can be active at the same time. The main channel decoder can be in different modes; CD–DA mode, CD–ROM mode, or CD–i mode.
- The **audio processor module** accepts an external audio input and, after processing, generates an audio output.
- The **microcode controller interface** takes care of accepting commands and passing data to the different parts of the audio processing unit.
- The **host interface** takes care of addressing the internal registers and buffers. The CIAP can interface with two possible hosts; a 68000 type host or a microcontroller that interfaces via a serial link.

REGISTER MEMORY MAP

Table 1. Registers and Buffers

Address (HEX)	Register	Description
0000 08FE	—	ADPCM buffer 0
0900 11FE	—	ADPCM buffer 1
1200 1B22	—	DATA buffer 0
1B24 1B2C	—	Q–buffer 0
1B2E 1B8C	—	R ... W buffer 0
1BC2 24E4	—	DATA buffer 1
24E6 24EE	—	Q–buffer 1
24F0 254E	—	R ... W buffer 1
2584	IER	Interrupt enable register
2586	ISR	Interrupt status register
2588	TACS	Temporal audio channel select register
258A	AACS	Actual audio channel select register
258C	TCM1	Temporal channel mask register
258E	ACM1	Actual channel mask register 1
2590	ACM2	Actual channel mask register 2
2592	FILE	File selection register
2594	BMAN	Buffer management register
2596	CCR	CIAP control register
259A	A_SHDW	ADPCM shadow register
25A0	AP_Left	Audio processor unit left register
25A2	AP_Right	Audio processor unit right register
25A4	AP_Vol	Audio processor unit volume register
25A6	APCR	Audio processor control register
25A8	ACONF	Audio configuration register
25AA	ASTAT	Audio processor status register
25C0	ICR	Interrupt control register
25C2	DMACTL	DMA control register
25FE	DLOAD	Download register

ELECTRICAL SPECIFICATIONS

OPERATING RANGE

The limits for operating the device are as follows:

Ambient Temperature (T_A) ..... 0°C to 70°C
Voltage, V_{DD} ..... 5 V ± 10%
Voltage, V_{SS} ..... 0 V

ABSOLUTE MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, Unless Otherwise Noted)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	– 0.5	+ 7.0	V
V_I	Input Voltage	– 1.5	V_{DD} + 1.5	V
V_O	Output Voltage	– 0.5	V_{DD} + 0.5	V
I_O	Output Current	—	± 25	mA
P_d	Power Dissipation	—	1200	mW
T_{stg}	Storage Temperature	– 65	+ 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

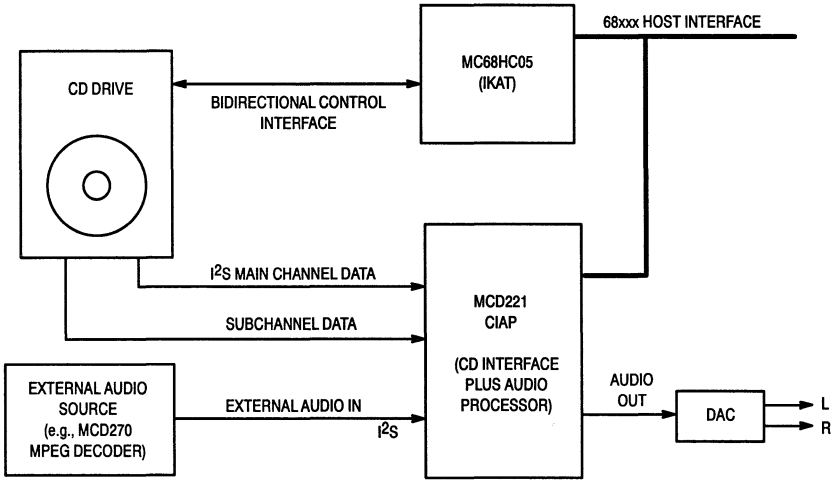
DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ± 10%, V_{SS} = 0 V, T_A = 0 to + 70°C, Unless Otherwise Noted)

Parameter	Symbol	Conditions	Min	Max	Unit
Operating Supply Current	I_{DD}	33.8688 MHz	—	tba	mA
Input Voltage (TTL Input)	V_{IH} V_{IL}	— —	2.0 —	— 0.8	V
Output Voltage (8 mA)	V_{OH} V_{OL}	— —	3.5 —	— 0.4	V
Output Voltage (16 mA)	V_{OH} V_{OL}	— —	3.5 —	— 0.4	V
Power Dissipation		—	—	tba	mW

APPLICATION EXAMPLES

CIAP/CD–DRIVE ARCHITECTURE

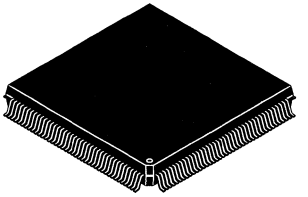
In conjunction with a suitable microcontroller, MC68HC05 (IKAT), the MCD221 provides the functionality to connect an MC68xxx host processor to a CD–Drive. The MCD221 decodes both main and subchannel CD data and plays both ADPCM and CDDA audio. External I²S format audio (e.g., MPEG1) may be input and mixed with the CIAP audio. CIAP audio output can be in either I²S or Sony formats.



MCD251

Technical Summary

MPEG Full Motion Video Decoder (FMV)



FU SUFFIX
QFP PACKAGE
CASE 1007–01

ORDERING INFORMATION
MCD251FU QFP

2

This technical summary provides a brief description of the MCD251 MPEG1 Full Motion Video (FMV) Decoder. A complete data sheet for the MCD251 is available and can be ordered from your local Motorola sales office. The order number is MCD251/D.

The MCD251 combines all the functions necessary to implement full motion video decompression with 4 Mbits of DRAM. The device can also be used to display still pictures and brings the possibility of digital full motion imaging technology to cost sensitive computer, communications and consumer applications, e.g. CD–i player full motion video decoder.

Using a combination of Huffman decoding, inverse discrete cosine transform and motion compensation, the MCD251 operates on pixels in 16 x 16 blocks. Each frame of a 352 x 288 pixel, 25 Hz picture sequence is therefore divided into 396 blocks, which are reconstructed in the 4 Mbit DRAM.

The MCD251 is capable of directly driving a 4 Mbit DRAM (256K x 16), including all necessary refresh. The transparent mode allows byte and word accesses by the system bus directly to the DRAM.

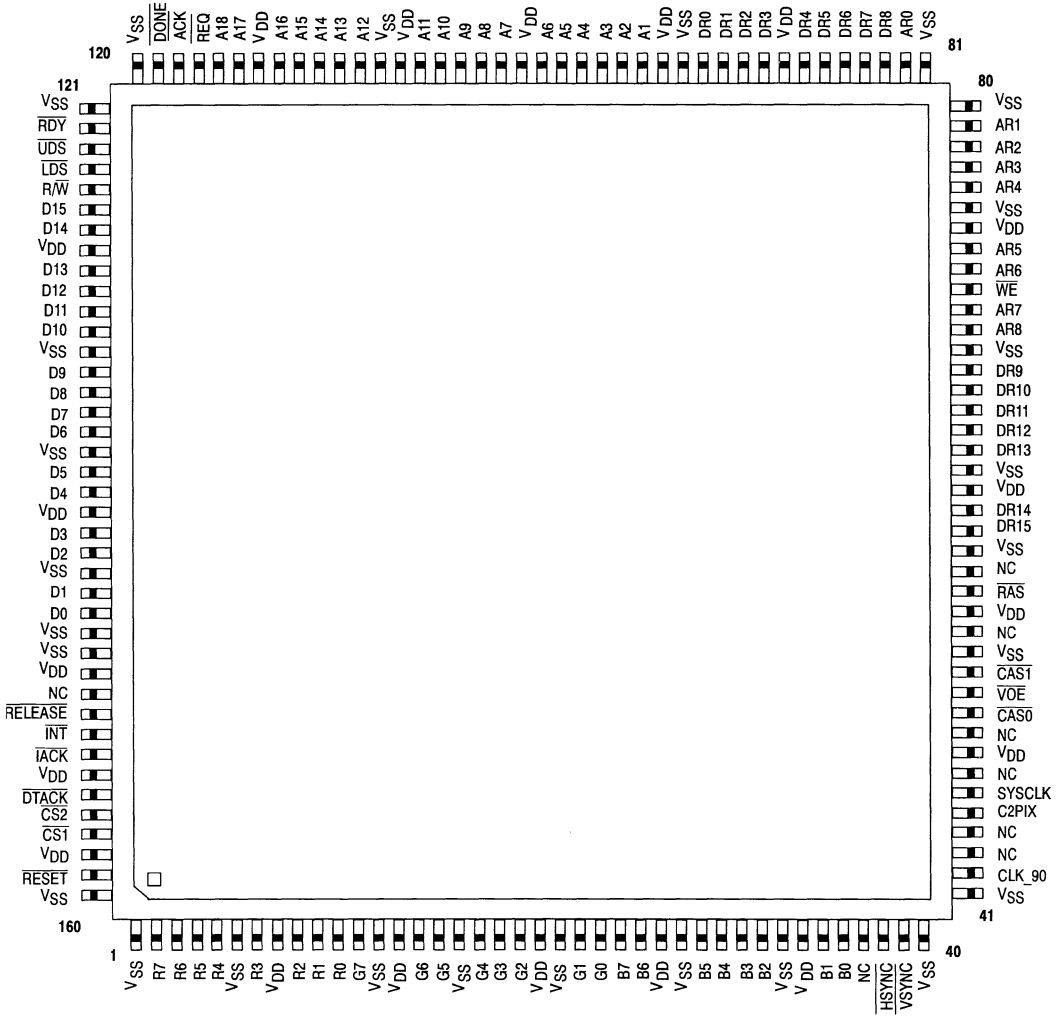
The main features of the MCD251 are as follows:

- Reconstructs Full Motion Video Sequences at 24 Hz, 25 Hz, or 30 Hz and Converts to a 50 Hz or 60 Hz Display Period
- Decodes Data Compatible with the Motion Picture Experts Group (MPEG1) Format at up to 5 Mbit/s
- Outputs the Decoded Video Plus a Border of a Predefined Color as RGB or YUV
- Display is Controlled by Externally Supplied Synchronization Signals and Pixel Clock in Either PAL or NTSC Format
- Able to Decode and Display Still Pictures
- At 30 Hz the Maximum Picture Area is 352 Pixels by 240 Lines
- Maximum Picture Rate of 30 Hz
- 4 Mbit DRAM (256K x 16) Direct Drive via 16 Bidirectional Data Lines and 9 Address Lines
- Compatible with the MC68000 and MC68341 Bus Interfaces
- System Interface that Handles Data Control and Status Information
- Able to Handle a Transfer Rate of up to 10 Mbit/s
- Supports Five Display Modes: Play Forward, Freeze, Single Step Forward, Slow Motion and Scan
- RGB or YUV Output via 24 Data Lines
- CMOS Technology
- 160–Pin Quad Flat Pack (QFP)

NOTE: Supply of this Video–CD IC does not convey an implied license under any patent right to use this IC in any Video–CD application.

CD–i is a registered trademark of Philips Consumer Electronics.

PIN ASSIGNMENT



PIN DESCRIPTIONS

Host Interface

Mnemonic	Type	Name and Function
A[18 ... 1]	I	Host address bus.
D[15 ... 0]	B	Host databus. Tri–state. Load 130 pF.
$\overline{CS1}$	I	Chip select 1. Active LOW. For selection of the internal registers. Only A1 ... A12 are significant in this case.
$\overline{CS2}$	I	Chip select 2. Active LOW. For selection of the DRAM. Can only be used when the IC is in transparent or debug mode.
$\overline{UDS}$	I	Upper datastrobe. Active LOW. Indication that data on D8 ... D15 is valid in case of a write cycle to the FMV. In case of a read cycle from the FMV it indicates that the FMV must put data on D8 ... D15.
$\overline{LDS}$	I	Lower datastrobe. Active LOW. Indication that data on D0 ... D7 is valid in case of a write cycle (to the FMV). In case of a read cycle (from the FMV) it indicates that the FMV must put data on D0 .... D7.
$\overline{DTACK}$	B	Active LOW. Data transfer acknowledge output: Indicates in case of a write cycle to the FMV that data is latched. In case of a read cycle from the FMV it indicates that valid data is on the databus. Tri–state, must be pulled up externally. Data transfer acknowledge input: Indicates in case of DMA transfer that there is valid data on the bus. Load 130 pF.
R/$\overline{W}$	I	Read/Write. Indicates the direction of the data flow. High is read from the FMV. Low is write to the FMV.
$\overline{INT}$	O	Interrupt request. Open drain, must be pulled up externally. Active LOW. Load 130 pF.
$\overline{IACK}$	I	Interrupt acknowledge. Active LOW.
$\overline{REQ}$	O	DMA request. Active LOW. Open drain. Must be pulled up externally. Load 130 pF.
$\overline{ACK}$	I	DMA acknowledge. Active LOW.
$\overline{RDY}$	O	DMA ready. Indication that the FMV has latched the data on the bus during a DMA transfer. Tri–state. Must be pulled up externally. Active LOW. Load 130 pF.
$\overline{DONE}$	I	DMA done. Indication that the last DMA transfer is in progress. The FMV will then release the $\overline{REQ}$ signal. Active LOW.
$\overline{RELEASE}$	I	Release DMA request. When asserted the FMV releases $\overline{REQ}$ and resets the internal DMA logic. Active LOW.
CLK_90	I	External 90 kHz clock.
$\overline{RESET}$	I	Global reset. Active LOW.
SYSCLK	I	40 MHz system clock.

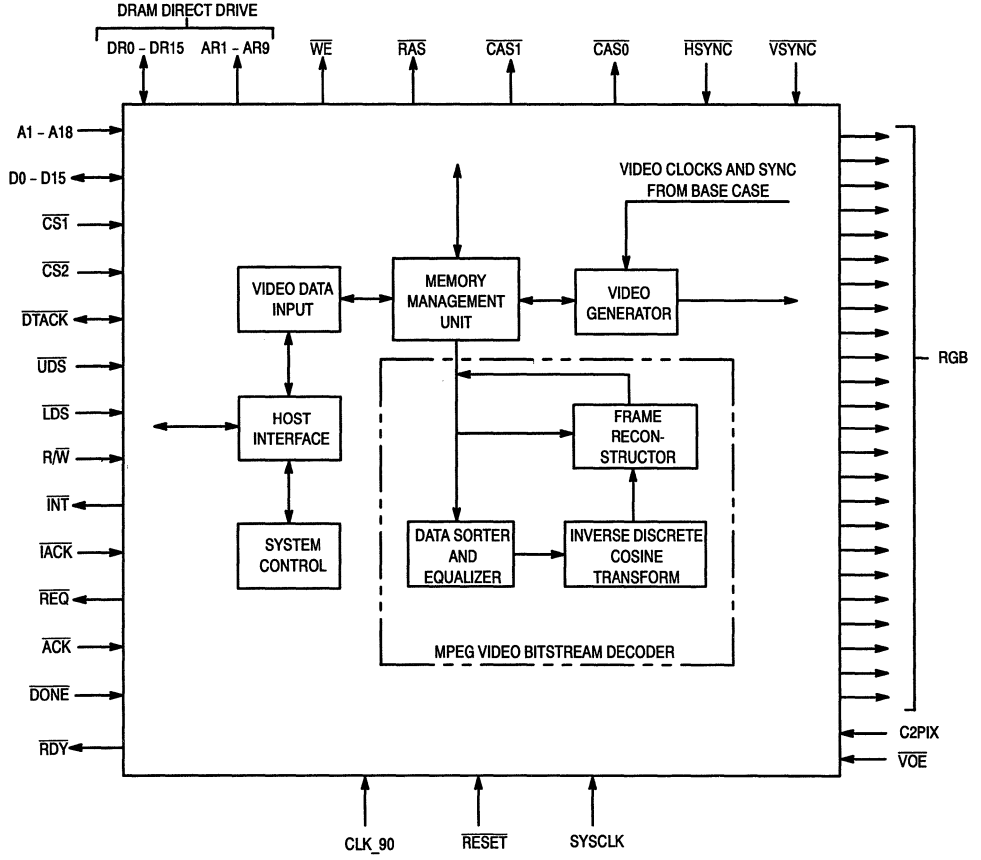
The Video Interface

Mnemonic	Type	Name and Function
R0 ...R7 G0 ... G7 B0 ... B7	O	24 bit RGB bus. When the FMV is in YUV mode, then: R=Y, G=U, B=V. Tri–state. Load 50 pF.
$\overline{VOE}$	I	Video output enable. Enables or tristates the RGB outputs; polarity is defined by a host writeable register bit.
C2PIX	I	Pixel clock of twice the pixel frequency. The clock is internally divided by 2. The phase adjustment is done by the $\overline{HSYNC}$.
$\overline{HSYNC}$	I	Video line synchronization. Active LOW.
$\overline{VSYNC}$	I	Video vertical synchronization signal. Active LOW.

The Memory Interface

Mnemonic	Type	Name and Function
AR0 ... AR8	O	DRAM row / column address. Load 50 pF.
DR0 ... DR15	B	DRAM databus. Tri–state. Load 50 pF.
$\overline{\textbf{WE}}$	O	DRAM write enable. Active LOW. Load 50 pF.
$\overline{\textbf{RAS}}$	O	DRAM row address select. Active LOW. Load 50 pF.
$\overline{\textbf{CAS0}}$	O	Column address select signal for the lower data byte D0 ... D7. Active LOW. Load 50 pF.
$\overline{\textbf{CAS1}}$	O	Column address select signal for the upper data byte D8 ... D15. Active LOW. Load 50 pF.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The MCD251 Block Diagram should be used in conjunction with the following notes which outline the function of the various blocks within the device:

- The **host interface** takes care of communication with the host processor. It handles data exchange, DMA control and interrupts.
- The **system controller** controls all other functions, reading and interpreting their status and issuing commands.
- The **video data input** pre–processes the incoming data stream. In the case of an ISO11172 (MPEG1) stream, data from the selected channel is extracted from the stream. Also, the complete system layer is removed from the data stream so that data sent to the DRAM consists of MPEG1 video data of the selected channel. The system clock reference data and time stamp data are sent directly to the system controller. The video data input also recognizes the video startcodes and passes them on to the system controller.
- The **memory management unit** handles requests for DRAM access from the video data input, MPEG1 decoder and video generator. It also controls DRAM refresh.
- The **data sorter and dequantizer** takes MPEG1 video data from the FIFO and decodes the variable length codes to produce DCT coefficients, coding type information and motion vectors.
- The **inverse discrete cosine transform** applies a 2–dimensional IDCT on the 8 x 8 coefficient data and passes macroblock data to the frame reconstructor.
- The **frame reconstructor** takes data from the previous or next frame and reconstructs the current frame.
- The **video generator** reads the reconstructed YUV data from one of the buffers, converts it to RGB, fills in the border and outputs the data to a video DAC.

LOGICAL DATA FLOW

The logical data flow between the main elements of the chip is shown in Figure 1.

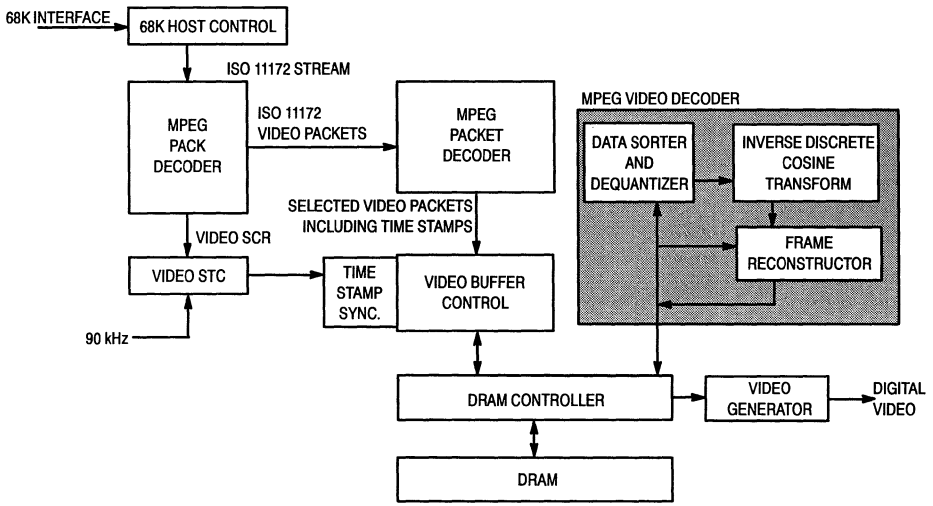


Figure 1. MCD251 Logical Data Flow and Synchronization Diagram

REGISTER MEMORY MAPS

Table 1. Temporal Buffer Registers

Address (HEX)	Register	Description
2	T_PWI	Temporal picture width
4	T_PHE	Temporal picture height
6	T_PRPA	Temporal picture rate/aspect ratio

Table 2. Display Control Buffer_0 Registers

Address (HEX)	Register	Description
1C	B0_TCH	Disp_ctrl_buf_0 time_code_high
1E	B0_TCL	Disp_ctrl_buf_0 time_code_low
20	B0_VSR	Disp_ctrl_buf_0 video status

Table 3. Display Control Buffer_1 Registers

Address (HEX)	Register	Description
30	B1_TCH	Disp_ctrl_buf_1 time_code_high
32	B1_TCL	Disp_ctrl_buf_1 time_code_low
34	B1_VSR	Disp_ctrl_buf_1 video status

Table 4. Display Control Buffer_2 Registers

Address (HEX)	Register	Description
44	B2_TCH	Disp_ctrl_buf_2 time_code_high
46	B2_TCL	Disp_ctrl_buf_2 time_code_low
48	B2_VSR	Disp_ctrl_buf_2 video status

Table 5. Video Control Registers

Address (HEX)	Register	Description
66	Br	Border_red register
68	Bg	Border_green register
6A	Bb	Border_blue register
6C	Yo	Y–offset register
6E	Xo	X–offset register
70	Ya	Y–active register
72	Xa	X–active register
74	Yd	Y–display register
76	Xd	X–display register
78	Wh	Window height register
7A	Ww	Window width register
7C	Yw	Y–window register
7E	Xw	X–window register

Table 6. System Control Registers

Address (HEX)	Register	Description
50	SYS_STAT	Decoder status
52	SYS_PWI	Picture width
54	SYS_PHE	Picture height
56	SYS_PRPA	Picture rate/aspect ratio
58	SYS_TCH	Time code high
5A	SYS_TCL	Time code low
5C	SYS_VSR	Video status
5E	SYS_STS	System status
60	SYS_IER	Interrupt enable
62	SYS_ISR	Interrupt status
64	SYS_TIM	Timer
C0	SYS_SCMD	System command
C2	SYS_VCMD	Video command
C4	SYS_STRsel	Stream select
C6	SYS_SCR	System control
DA	SYS_GCR	Global control
DC	SYS_ICR	Interrupt control
DE	SYS_VDI	Video data input
E4	SYS_ABS	Actual buffer size
F2	SYS_BSIZ	Block size

Table 7. MMU Registers

Address (HEX)	Register	Description
F4	MMU_FSTART	FIFO start pointer

Table 8. Microcode RAM

Address (HEX)	Description
800	Bank1 bit 16 – 25, bit 35 – 40
1000	Bank2 bit 0 – 15
1800	Bank3 bit 26 – 34

ELECTRICAL SPECIFICATIONS

OPERATING RANGE

The limits for operating the device are as follows:

Ambient Temperature (T_A) ..... 0°C to 70°C
Voltage, V_{DD} ..... 5 V ± 10%
Voltage, V_{SS} ..... 0 V

ABSOLUTE MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, Unless Otherwise Noted)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to 7.0	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	Output Voltage	– 0.5 to V_{DD} + 0.5	V
I	DC Current Drain, per Pin	25	mA
I	DC Current Drain, V_{DD}/V_{SS} Pins	75	mA
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (10 Second Soldering)	300	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

FMV/CD–i ARCHITECTURE

In a CD–i player as shown in Figure 2, FMV provides the complete functionality of the full motion video extensions as specified in the Green Book standard for CD–i. It requires the external 4 Mbit DRAM to support MPEG video decoding, but can use the video DACs which are already part of the base case CD–i architecture. Video decoding is synchronized to the base case video decoder, (MCD211, VDSC) and its video output is multiplexed with VDSC output on a pixel by pixel basis.

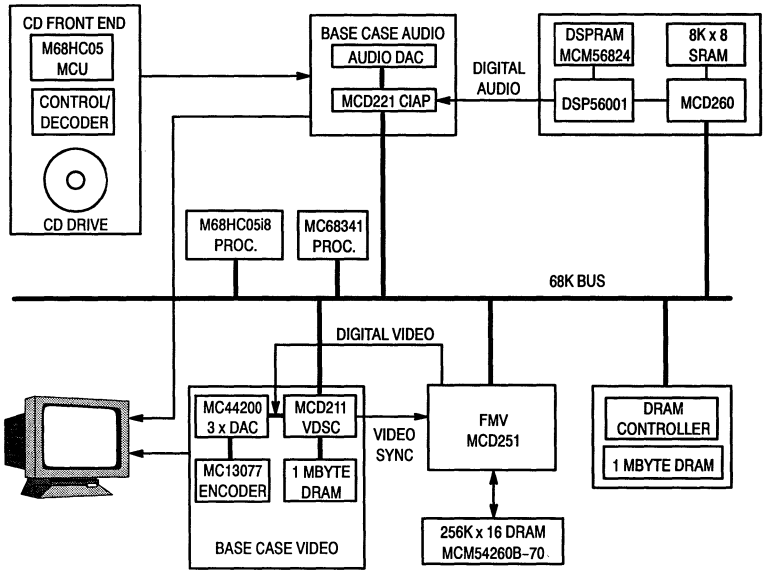


Figure 2. FMV/CD–i Architecture

DIGITAL VIDEO SWITCHING BETWEEN VDSC AND FMV

Digital or analog multiplexing may be used with FMV. Figure 3 shows how only one video DAC may be used if digital multiplexing is implemented. Digital video is tied directly to the 24 bit RGB bus from the base case video decoder (MCD211, VDSC) and multiplexing is achieved by a switch signal from VDSC, which enables and disables pixel outputs from the two sources.

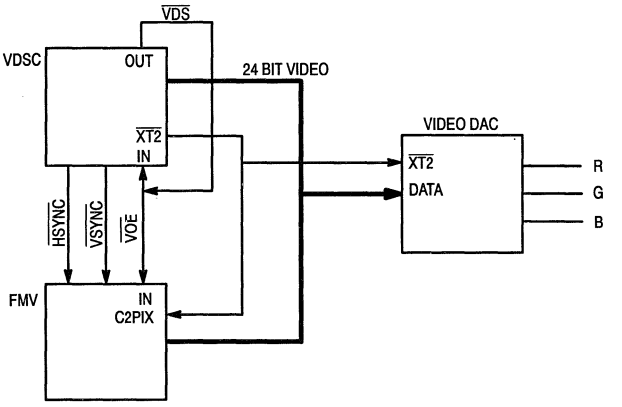


Figure 3. Digital Video Switching Example

ANALOG VIDEO SWITCHING BETWEEN VDSC AND FMV

Figure 4 shows a configuration more suited to an approach in which MPEG1 is added to a basic CD–i player as an expansion cartridge. FMV video decoding is still synchronized to the relevant base case signals, but the multiplexing and mixing are done in the analog domain. Although this requires two DACs, it requires fewer pins on the expansion cartridge connector.

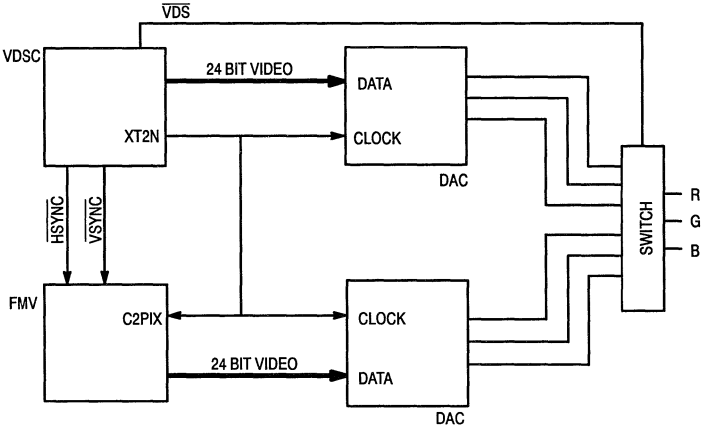


Figure 4. Analog Video Switching Example

FMV IN A PC MULTIMEDIA APPLICATION

Figure 5 illustrates how FMV could be used in a PC based application to provide an MPEG playback window overlayed on a VGA display. The VGA overlay controller provides scan rate conversion of the decoded MPEG image and windowing control based on color keying or programmable XY coordinates. An analog video switch is controlled from this to provide the overlay function.

Using FMV in this standalone manner requires the addition of a TV sync generator to provide $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and a pixel clock to FMV.

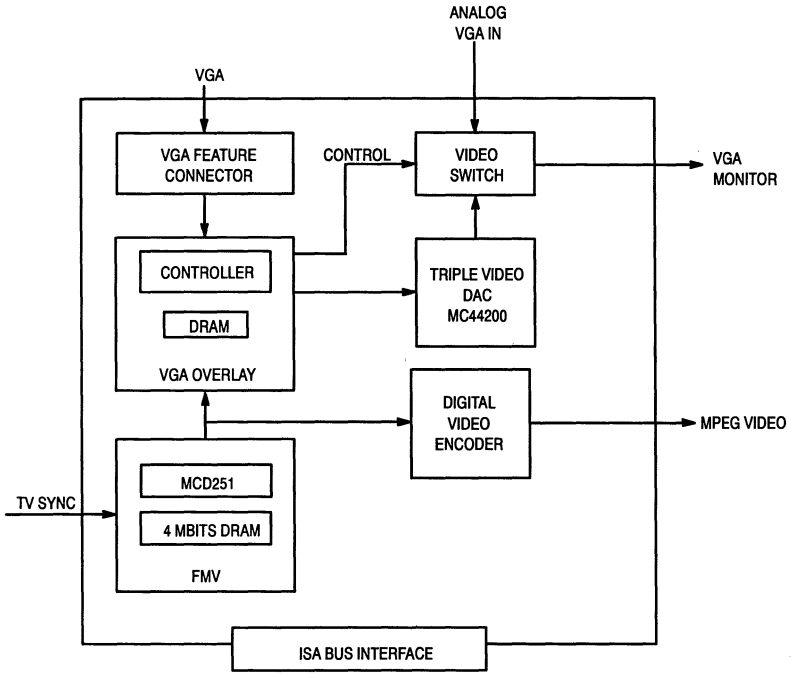


Figure 5. Example of FMV in a PC Multimedia Application

VIDEO ON DEMAND

FMV may be used as the decoder section of a video on demand integrated receiver decoder, as illustrated in Figure 6. MPEG1 video and audio streams are carried over an asymmetric digital subscriber loop (ADSL) in an MPEG2 transport stream. A transport stream decoder separates the conditional access data and the video and audio streams from the transport stream. The video stream is directed to FMV and the conditional access data to the Smart Card controller. An on–screen display is generated by using an MCD211 (VDSC). The video output stage is identical to those in the CD–i application described earlier.

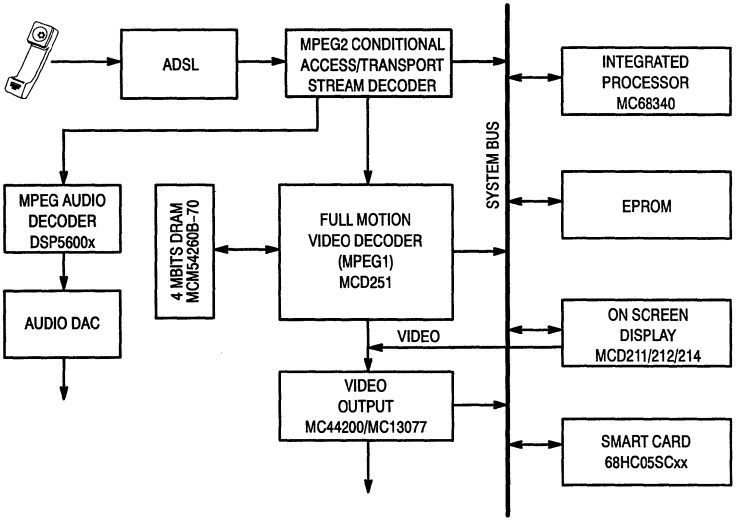
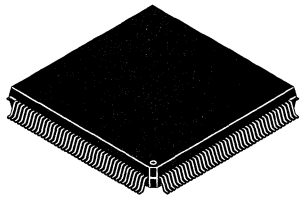


Figure 6. Example of Video On Demand

MCD270

Technical Summary

IMPEG Integrated Video and Audio Decoder



FU SUFFIX
QFP PACKAGE
CASE 1007–01

ORDERING INFORMATION
MCD270FU QFP

This technical summary provides a brief description of the MCD270 IMPEG Integrated Video and Audio Decoder. A complete data sheet for the MCD270 is available and can be ordered from your local Motorola sales office. The order number is MCD270/D.

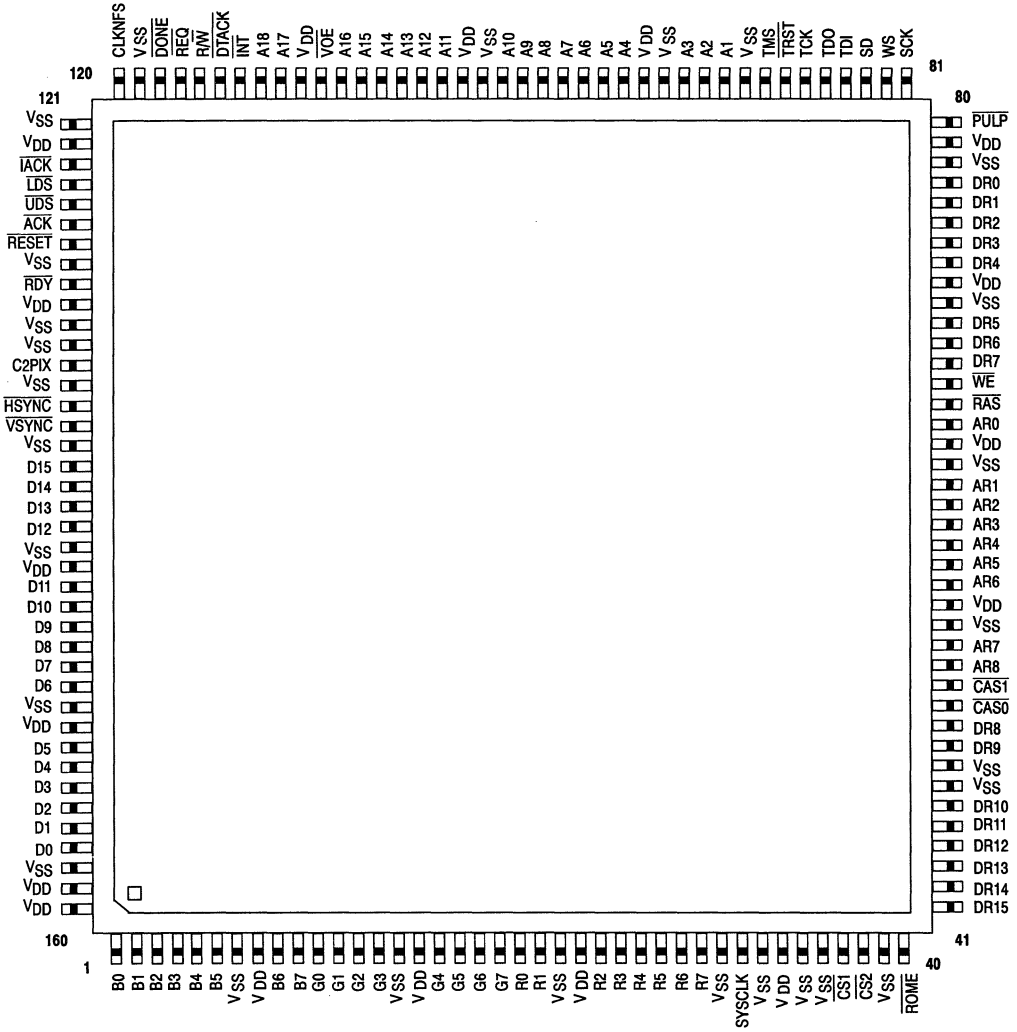
The MCD270 is a single chip MPEG1 Audio and Video Decoder, requiring the addition of only a single 4 Mbits DRAM and appropriate DACs to provide full MPEG1 decoding for consumer multimedia applications such as CD–i, CD–Karaoke, Video–CD, and Video–On–Demand type services. The main features of the device are as follows:

- Direct Interface for MC68000 Bus Compatible Devices, with DMA and Interrupt Capability
- Direct Drive of 24–Bit Triple Video DACs Such as the MC44200
- Direct Drive of 16– and 18–Bit Stereo Audio DACs via I^2S or Sony Formats
- Direct Drive of 256K x 16 DRAM for Video and Audio Buffering and Frame Reconstruction
- 11.2896 MHz, 16.9344 MHz, or 33.8688 MHz CD Clock Input for Generation of 90 kHz MPEG System and Audio Clocks
- Decodes MPEG System Layer to Allow Channel Selection, Buffer Control, and Perform Correct Audio/Video Synchronization
- Decodes 24, 25, or 30 Hz MPEG1 Constrained Parameter Video Streams and Outputs Digital 24–Bit RGB at PAL or NTSC Rates
- Capable of Decoding MPEG1 Video at Bit Rates of up to 5 Mbits Per Second
- Decodes Layer I or II MPEG1 Audio Streams, All Bit Rates, All Modes, 44.1 kHz Sample Rate
- Decodes Either Single Multiplexed ISO11172 Streams or Dual ISO11172 Streams as in CD–i, CD–Karaoke, and Video–CD
- Implements All Extra CD–i Functionality such as Windowing, Still Picture Mode, and Audio Attenuation Control
- 160–Pin Plastic Quad Flat Pack

NOTE: Supply of this Video–CD IC does not convey an implied license under any patent right to use this IC in any Video–CD application.

CD–i is a registered trademark of Philips Consumer Electronics.

PIN ASSIGNMENT



GENERAL

Motion Picture Expert Group 1 (MPEG1) is an ISO standard for the compression of digital video and associated audio. In particular MPEG1 defines a bit stream for compressed video and audio optimized for a data rate of 1.5 Mbps. This bandwidth, which is the data rate of (uncompressed) audio CDs, delivers VHS quality video and CD quality audio.

The defined standard consists of three parts; video, audio, and systems. The video and audio parts define the compression of the video and audio components, and the systems part defines the integration of the audio and video streams with proper timestamping to allow their synchronization.

The detailed specifications are contained in the following ISO standards:

- ISO 11172–1, MPEG1–System
- ISO 11172–2, MPEG1–Video
- ISO 11172–3, MPEG1–Audio

MPEG1 is the coding/compression standard that is specified for the Full Motion Extensions to CD–i and for CD–Bridge disc formats such as CD–Karaoke and Video–CD. MPEG2 and MPEG4 are not applicable and all further references to MPEG in this document refer specifically to MPEG1.

VIDEO

MPEG1 Video uses a combination of transform coding and motion compensation to exploit the spatial and the temporal redundancy present in video sequences, which (depending on the resolution of the original sequence) gives compression ratios of around 25:1. MPEG1 is a frame rather than a field based compression scheme, the frames being Intra, Predicted, or Bidirectionally predicted. Although the full specification of MPEG1 allows for high bit rates and large frame sizes, a constrained parameter stream is specified, which allows a decoder to be designed for low–cost consumer applications. CD–i and CD–Bridge formats use a constrained parameter stream, but CD–i has some extra features supported by the MCD270 which allow further windowing of video after the MPEG decoding. In addition, the MCD270 supports the CD–i still picture mode based on larger size MPEG1 frames than the constrained parameter stream allows.

AUDIO

MPEG1 Audio uses sub–band coding with dynamic bit–allocation based on a psychoacoustic model to attain compression ratios of up to 8:1 without noticeable degradation in quality when compared to CD–DA. There are three types of coding that MPEG1 Audio allows, termed layers I–III. These give approximately 4:1, 6:1, and 8:1 compression with a corresponding increase in the level of decoding complexity. Since Layer III is significantly more complex than the other two layers, the MCD270 supports only layers I and II as required by CD–i and CD–Bridge formats. The coded MPEG Audio stream also specifies the output sample rate of the decoded audio, which, although 32 kHz, 44.1 kHz, and 48 kHz are allowed within the full MPEG1 standard, is constrained to 44.1 kHz in the MCD270 as specified for CD–i and CD–Bridge formats.

SYSTEM LAYER

The MPEG System layer contains information needed for decoder buffer control, audio/video synchronization and channel demultiplexing. In CD–i and CD–Bridge discs, MPEG data is stored on the disc in separate audio and video sectors, each of which has its own MPEG System layer associated with it. This is in contrast to a conventional MPEG stream in which the audio and video are multiplexed into the same single ISO11172 stream. The MCD270 will handle either form of multiplexing.

In all CD–i and CD–Bridge MPEG streams, the system_audio_lock_flag is set, indicating that there is a constant rational relationship between the audio sample rate and the system clock frequency. Thus, MCD270 audio decoder timing (i.e., the 44.1 kHz output rate) must be locked to the CD drive when playing real–time files. This ensures correct input buffer operation without requiring the skipping or duplicating of samples, which would result in significant degradation of sound quality. Video is then locked to audio by means of an on–chip 90 kHz MPEG System Clock which is also locked to the CD drive clock.

Figure 1 illustrates a typical MPEG1 video and audio decoder.

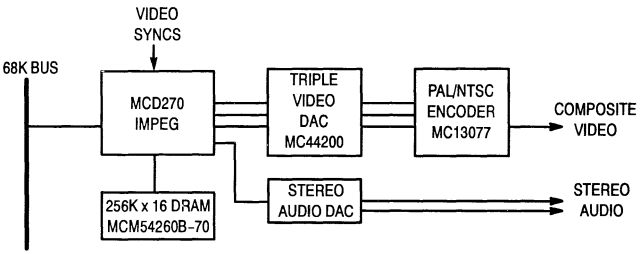
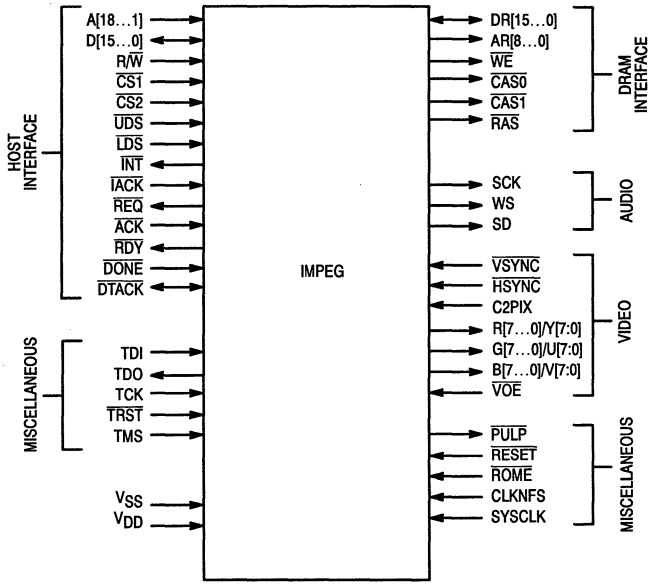


Figure 1. Typical MPEG1 Video and Audio Decoder

PIN DESCRIPTION



PIN DESCRIPTIONS

Host Interface

Mnemonic	Type	Name and Function
A[18 ... 1]	I	Address bus.
D[15 ... 0]	B	Bidirectional databus.
R/W	I	Read/Write. Direction for data transfer.
CS1	I	Chip select 1. Active LOW. Used for access of all audio/video related registers. Allows only word access.
CS2	I	Chip select 2. Active LOW. Used for random access of the DRAM. Allows both word and byte access.
UDS	I	Upper datastrobe. Active LOW. Used to address the upper byte [D15 ... D8] of a word.
LDS	I	Lower datastrobe. Active LOW. Used to address the lower byte [D7 ... D0] of a word.
INT	O	Interrupt request. Active LOW. Open drain output.
IACK	I	Interrupt acknowledge. Active LOW.
REQ	O	DMA transfer request. Active LOW. Open drain output.
ACK	I	DMA acknowledge. Active LOW. Indicates that the bus is free for a DMA access.
RDY	O	DMA ready. Active LOW. Indicates that the IMPEG has read data from the data bus. (Active pullup.)
DONE	I	DMA done. Active LOW. Indicates that the current transfer cycle is the last cycle of a burst.
DTACK	B	Data transfer acknowledge. Active LOW. During normal host access, DTACK is an output indicating that data has been put on (read cycles) or read from (write cycles) the data bus. (Active pullup.) During DMA, DTACK is an input indicating that the memory has put data on the data bus.

Video Interface

Mnemonic	Type	Name and Function
R[7 ... 0]/Y[7:0]	O	8 bit wide Red (RGB mode) or Y (YUV mode) output.
G[7 ... 0]/U[7:0]	O	8 bit wide Green (RGB mode) or U (YUV mode) output.
B[7 ... 0]/V[7:0]	O	8 bit wide Blue (RGB mode) or V (YUV mode) output.
VOE	I	Video output enable. Enables or tristates the RGB outputs; polarity defined by a host writeable register bit.
C2PIX	I	Pixel clock of twice the pixel frequency.
$\overline{\text{HSYNC}}$	I	Video line synchronization.
$\overline{\text{VSYNC}}$	I	Video vertical synchronization signal.

Audio Interface

Mnemonic	Type	Name and Function
SCK	O	Output sample clock of 2.8224 MHz (locked to CD clock).
WS	O	Wordselect. For I^2S format LOW indicates left channel, HIGH indicates right channel. For Sony format LOW indicates right channel and HIGH indicates left channel.
SD	O	Data output (MSB first).

DRAM Interface

Mnemonic	Type	Name and Function
DR[15 ... 0]	B	16 bits bidirectional DRAM data bus.
AR[8 ... 0]	O	DRAM row/column address.
$\overline{\text{WE}}$	O	DRAM write enable. Active LOW.
$\overline{\text{CAS0}}$	O	Column address select signal (lower data byte).
$\overline{\text{CAS1}}$	O	Column address select signal (upper data byte).
$\overline{\text{RAS}}$	O	DRAM row address select.

Boundary Scan

Mnemonic	Type	Name and Function
TDI	I	Test Data Input, test data sampled at rising edge of TCK.
TDO	O	Test Data Output.
TCK	I	Test Clock Input.
$\overline{\text{TRST}}$	I	Boundary scan reset.
TMS	I	Test Mode select.

Miscellaneous

Mnemonic	Type	Name and Function
SYSCLK	I	40 MHz system clock.
CLKNFS	I	Audio clock input. Can be either an 11.2896 MHz, 16.9344 MHz, or 33.8688 MHz CD–clock.
$\overline{\text{ROME}}$	I	ROM enable. Active LOW input. When asserted the IMPEG IC has to generate a $\overline{\text{DTACK}}$.
$\overline{\text{PULP}}$	O	General purpose output pin. Can be set to LOW or tri–state via an internal register.
$\overline{\text{RESET}}$	I	Global chip reset. Active LOW.

HARDWARE STRUCTURE

The MCD270 IMPEG chip contains several major functional areas, as illustrated in Figure 2.

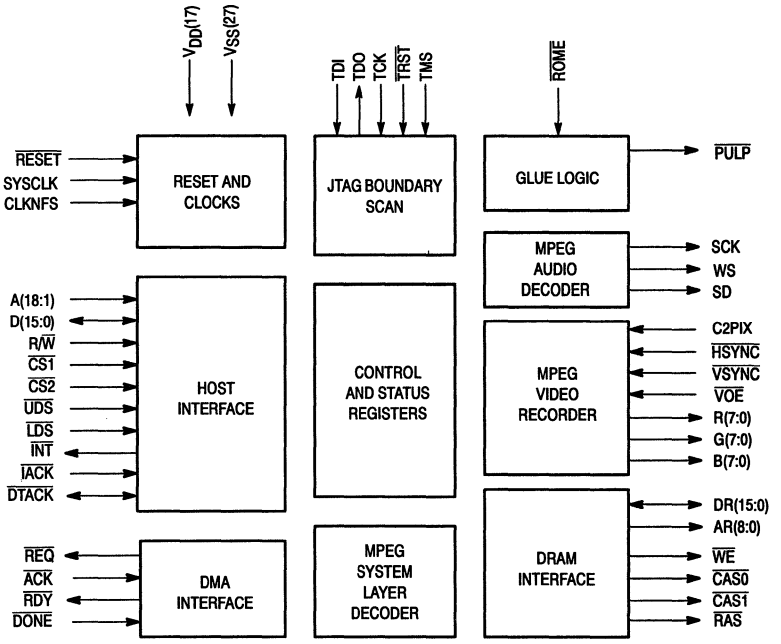


Figure 2. MCD270 Block Diagram

EXTERNAL INTERFACES

Host Interface

The host communicates with the MPEG decoder via the host interface which consists of a 16–bit wide bidirectional data bus, address bus, and necessary signals for interrupt, register access, and DMA.

Four types of data are communicated through the host interface, as follows:

- MPEG video data: Video data being transferred from the host can either be under the control of the CPU (register access) or under control of DMA (burst mode).
- MPEG audio data: Audio data being transferred from the host to the decoder can either be under the control of the CPU (register access) or under control of DMA (burst mode, same channel as video DMA).
- Control and information data: This is bidirectional data transfer. The MCD270 can provide status information to the host via 16–bit wide registers, and the host can control the chip via the registers. The occurrence of some events can be signalled to the host via an interrupt.
- Random access data: The random access feature can only be used when the decoder is in transparency or debug mode. In these modes the complete DRAM can be accessed.

Video Interface

The video interface is the link between the MPEG decoder and the external video DAC.

The video data output can be either in 24–bit RGB or in 24–bit YUV format.This format is selected by bit 6 (RGB) of the Video System Control Register (VSCR).

Audio Interface

The audio interface is in either the Phillips I^2S format or the Sony format. The selection is done with bit 8 of the Global Control Register (GCR).

The MCD270 is always master; it always generates its own wordselect and output sample clock.

DRAM Interface

The DRAM interface consists of the signals necessary to control the external 4 Mbit DRAM.

Boundary Scan

Test and boundary scan signals.

Clock Interface

System and CD clock signals.

Glue Logic

General purpose signals which may be used in a CD–i full motion video cartridge application.

INTERNAL FUNCTIONALITY

The MCD270 consists of audio, video, and general registers. The logical data flow between the main elements in the chip are illustrated in Figure 3.

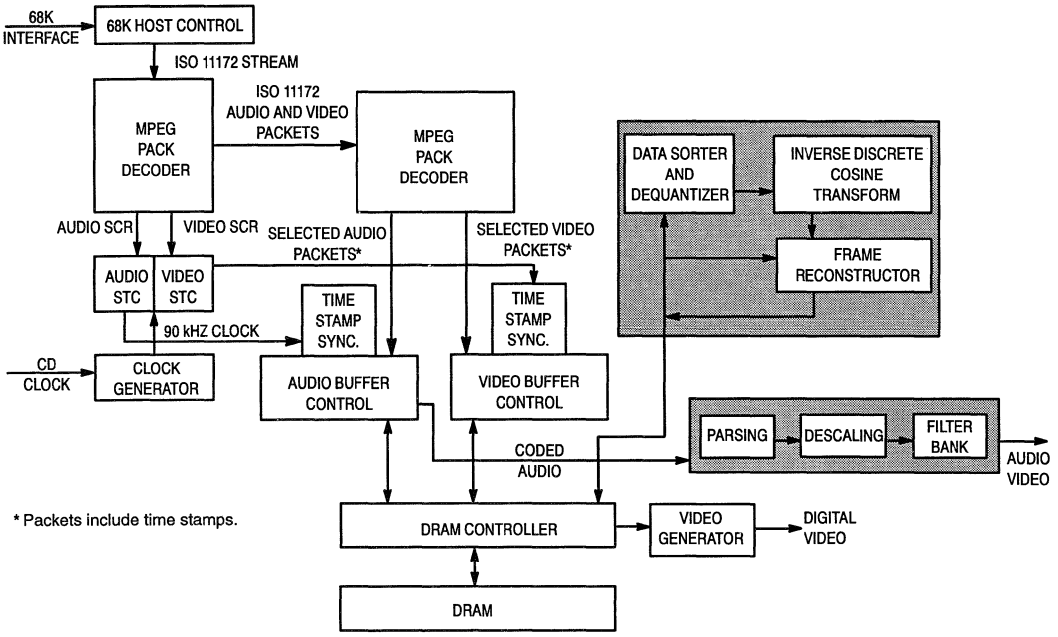


Figure 3. MCD270 Logical Data Flow and Synchronization Diagram

REGISTER MEMORY MAPS

VIDEO REGISTERS

The video registers handle the picture attributes (color, picture height and width, pixel aspect ratios) plus timing and control functions.

Table 1. Temporal Buffer Registers

Address (HEX)	Register	Description
2	T_PWI	Temporal picture width
4	T_PHE	Temporal picture height
6	T_PRPA	Temporal picture rate/aspect ratio

Table 2. Display Control Buffer_0 Registers

Address (HEX)	Register	Description
1C	B0_TCH	Disp_ctrl_buf_0 time_code_high
1E	B0_TCL	Disp_ctrl_buf_0 time_code_low
20	B0_VSR	Disp_ctrl_buf_0 video status
22	B0_BX	Disp_ctrl_buf_0 first pix of line

Table 3. Display Control Buffer_1 Registers

Address (HEX)	Register	Description
30	B1_TCH	Disp_ctrl_buf_1 time_code_high
32	B1_TCL	Disp_ctrl_buf_1 time_code_low
34	B1_VSR	Disp_ctrl_buf_1 video status
36	B1_BX	Disp_ctrl_buf_1 first pix of line

Table 4. Display Control Buffer_2 Registers

Address (HEX)	Register	Description
44	B2_TCH	Disp_ctrl_buf_2 time_code_high
46	B2_TCL	Disp_ctrl_buf_2 time_code_low
48	B2_VSR	Disp_ctrl_buf_2 video status
4A	B2_BX	Disp_ctrl_buf_2 first pix of line

Table 5. Video Control Registers

Address (HEX)	Register	Description
66	Br	Border_red register
68	Bg	Border_green register
6A	Bb	Border_blue register
6C	Yo	Y–offset register
6E	Xo	X–offset register
70	Ya	Y–active register
72	Xa	X–active register
74	Yd	Y–display register
76	Xd	X–display register
78	Wh	Window height register
7A	Ww	Window width register
7C	Yw	Y–window register
7E	Xw	X–window register

Table 6. Video System Control Registers

Address (HEX)	Register	Description
50	VSTAT	Video decoder status
52	PWI	Picture width
54	PHE	Picture height
56	PRPA	Picture rate/pixel aspect ratio
58	TCH	Time code high
5A	TCL	Time code low
5C	VSR	Video status
5E	VSTS	Video system status
60	VIER	Video interrupt enable
62	VISR	Video interrupt status
64	VTIM	Video timer
C0	VSCMD	Video system command
C2	VCMD	Video command
C4	VSEL	Video stream select
C6	VSCR	Video system control
DE	VDI	Video data input
E4	ABS	Actual buffer size
F2	BSIZ	Block size

Table 7. MMU Registers

Address (HEX)	Register	Description
F4	VFSTART	Video FIFO start point
114	AFSTART	Audio FIFO start point

AUDIO REGISTERS

The audio registers handle the selection and decoding of the audio stream, attenuation, audio frame header updating plus associated timing and interrupts.

Table 8. Audio System Control Registers

Address (HEX)	Register	Description
200	ADCR	Audio decoder command
202	ADSR	Audio decoder status
204	ATIM	Audio timer
106	ABSZ	Audio blocksize
208	ASELS	Select audio stream
20A	ACURS	Current audio stream
11E	ADI	Audio data input
218	ADDLY	Audio decoder delay
21A	AIOR	Audio interrupt originator
21C	AIER	Audio interrupt enable

Table 9. Audio Control and Information Control Registers

Address (HEX)	Register	Description
214	AHR1	Audio header 1
216	AHR2	Audio header 2
20C	ATTL	Attenuator left
20E	ATTR	Attenuator right

GENERAL REGISTERS

Included here are general control registers, interrupt registers, and audio/video sync registers.

Table 10. General Control and Information Registers

Address (HEX)	Register	Description
DA	GCR	Global control register
DC	ICR	Interrupt control
206	SCC	System clock counter
210	AVRH	A/VSYNC high
212	AVRL	A/VSYNC low

DOWNLOAD REGISTERS

The audio and video microcode has to be downloaded from the host.

Table 11. Video Microcode Registers

Address (HEX)	Description
800	Bank1
1000	Bank2
1800	Bank3

2

Table 12. Audio Microcode Registers

Address (HEX)	Description
2000	Bank1
2800	Bank2
3000	Bank3

ELECTRICAL SPECIFICATIONS

OPERATING RANGE

The limits for operating the device are as follows:

Ambient Temperature (T_A) ..... 0 – 70°C
Voltage, V_{DD} ..... 5 V ± 10%
Voltage, V_{SS} ..... 0 V

ABSOLUTE MAXIMUM RATINGS* (Voltages Referenced to V_{SS}, Unless Otherwise Noted)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	– 0.5	+ 7.0	V
V_I	Input Voltage	– 1.5	V_{DD} + 1.5	V
V_O	Output Voltage	– 0.5	V_{DD} + 0.5	V
I_O	Output Current	—	± 25	mA
P_d	Power Dissipation	—	1200	mW
T_{stg}	Storage Temperature	– 65	+ 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

2

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ± 10%, V_{SS} = 0 V, T_A = 0 to + 70°C, Unless Otherwise Noted)

Parameter	Symbol	Conditions	Min	Max	Unit
Operating Supply Current	I_{DD}	40 MHz	—	300	mA
Input Voltage (TTL Input)	V_{IH} V_{IL}		2.0 —	— 0.8	V
Output Voltage, 8 mA	V_{OH} V_{OL}		3.5 —	— 0.4	V
Output Voltage, 16 mA	V_{OH} V_{OL}		3.5 —	— 0.4	V
Power Dissipation			—	1500	mW

NOTE: All outputs can have a load of 130 pF, except for the DRAM which can have 50 pF.

IMPEG/CD–i ARCHITECTURE

In a CD–i player as shown in Figure 4, IMPEG provides the complete functionality of full motion extensions as specified in the Green Book standard for CD–i. It requires the external 4 Mbit DRAM to support MPEG video and MPEG audio decoding, but can use the video and audio DACs already part of the base case CD–i architecture. IMPEG audio decoding is synchronized to the CD drive clock and its audio output is added to base case audio. IMPEG video decoding is synchronized to the base case video decoder (MCD211, VDSC), and its video output is multiplexed with VDSC output on a pixel by pixel basis.

Digital Video Switching Between VDSC and IMPEG

Digital or analog multiplexing may be used with IMPEG. Figure 5 shows how only one video and one audio DAC may be used if digital multiplexing is used. Digital audio is sent directly to the base case audio decoder (MCD221 CIAP) and is digitally mixed before a combined signal is sent to the audio DAC. Digital video is tied directly to the 24–bit RGB bus from the base case video decoder (MCD211 VDSC) and multiplexing is achieved by a switch signal from VDSC, which enables and disables pixel outputs from the two sources.

Analog Video Switching Between VDSC and IMPEG

Figure 6 shows a configuration more suited to a cartridge based approach in which MPEG1 is added to a basic CD–i player as an expansion cartridge. IMPEG audio and video decoding are still synchronized to the relevant base case signals, but the multiplexing and mixing are done in the analog domain. Although this requires two DACs, it requires fewer pins on the expansion cartridge connector.

IMPEG IN A PC MULTIMEDIA APPLICATION

Figure 7 illustrates how IMPEG could be used in a PC based application to provide an MPEG playback window overlayed on a VGA display. The VGA overlay controller provides scan rate conversion of the decoded MPEG image and windowing control based on color keying or programmable XY coordinates. An analog video switch is controlled from this to provide the overlay function.

Using IMPEG in this standalone manner requires the addition of a TV sync generator to provide $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and a pixel clock to IMPEG.

VIDEO ON DEMAND

IMPEG may be used as the decoder section of a video on demand integrated receiver decoder, as illustrated in Figure 8. MPEG1 video and audio streams are carried over an asymmetric digital subscriber loop (ADSL) in an MPEG2 transport stream. A transport stream decoder separates the conditional access data and the video and audio streams from the transport stream. The video and audio streams are directed to IMPEG and the conditional access data to the Smart Card controller. An on–screen display is generated by using an MCD211 (VDSC). The video and audio output stages are identical to those in the CD–i application described earlier.

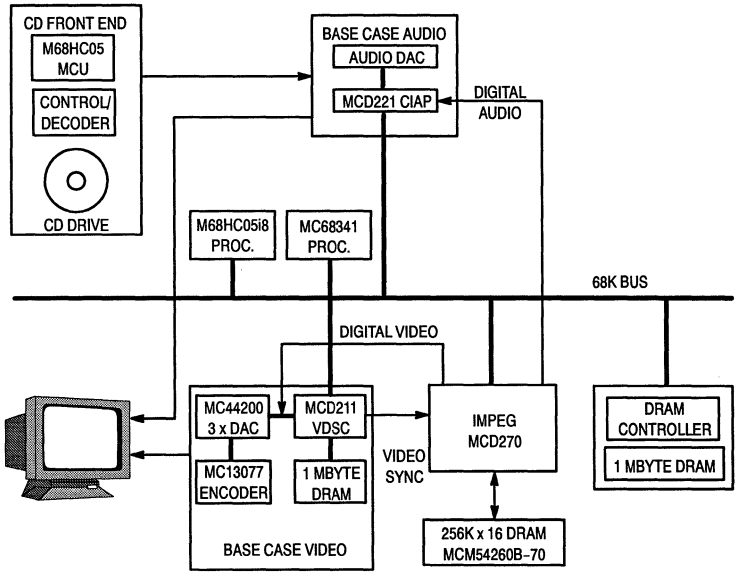


Figure 4. IMPEG/CD–i Architecture

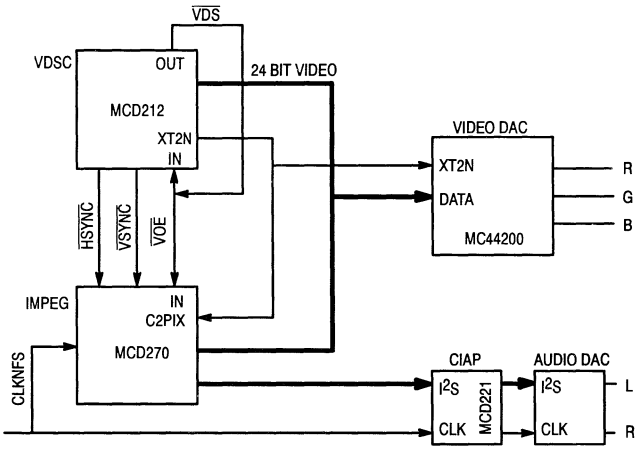


Figure 5. Digital Video Switching Example

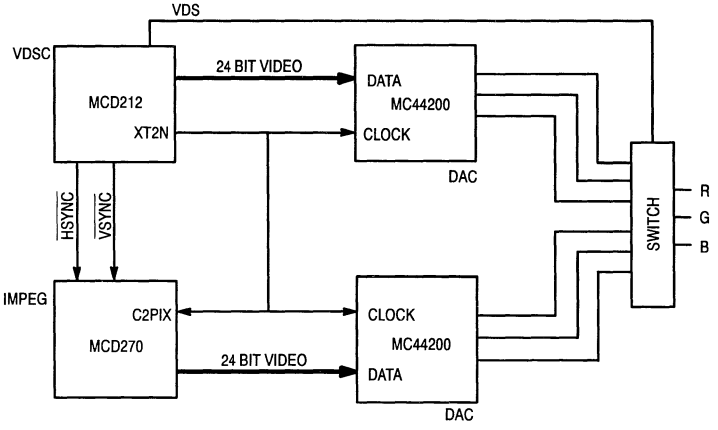


Figure 6. Analog Video Switching Example

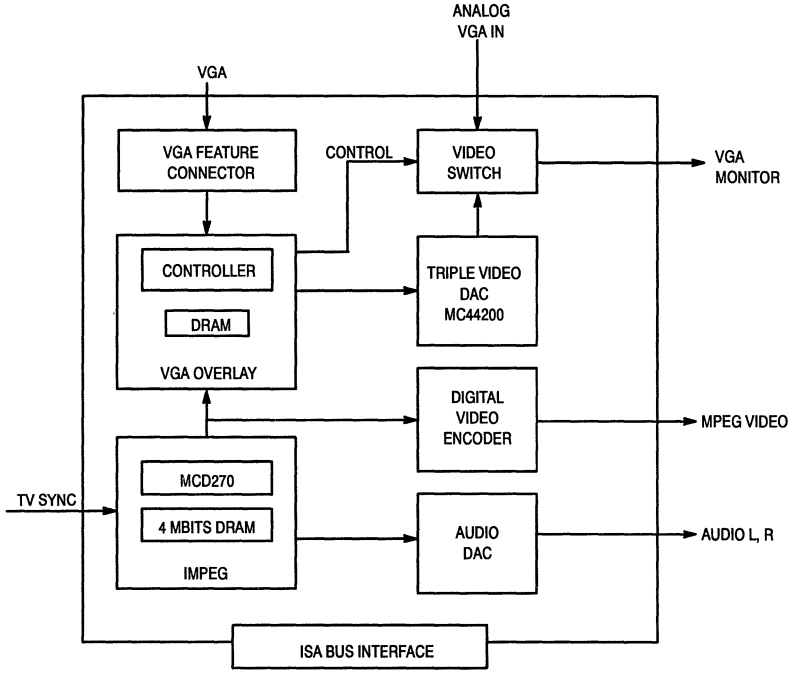


Figure 7. Example of IMPEG in a PC Multimedia Application

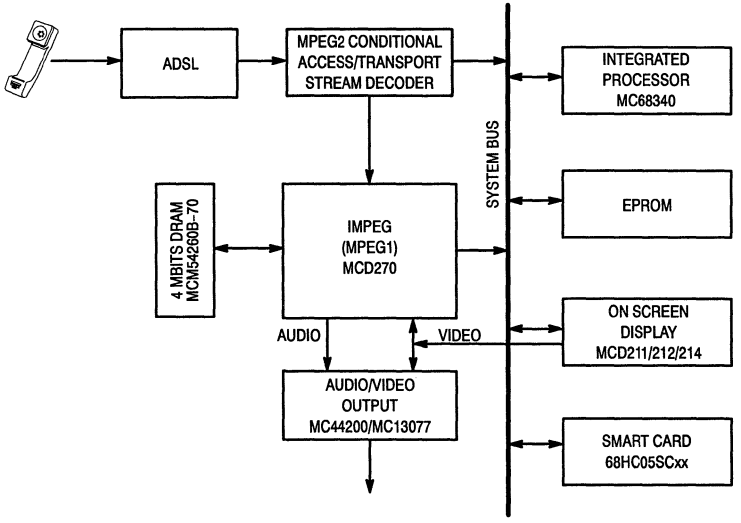


Figure 8. Video On Demand Example

Evaluation Kits

3

3

MC141622EVK

Product Proposal

ACF-II Evaluation Board Operating Manual

1. SUMMARY

The MC141622EVK is a development board for evaluation of the MC141622. In addition to the MC141622, the MC141622EVK contains all the analog circuit that is necessary for buffering both the input and output video signal and generation of the 4xfsc clock. By connecting an external signal source, monitor, and power supply, it is possible to evaluate all the operating modes on the MC141622.

2. SPECIFICATION

Board Dimensions	100 mm (Length) x 150 mm (Width)
Y/C Separation LSI	MC141622FU Mount
Video Input Amplifier	MC14577 2SC2002 Use
Video Output Amplifier	MC14576 Use
Clamp Circuit	2SC2002 2SA953 Use
Clock Generator	MC1378P Use
Clock Buffer Amplifier	MC14576 Use
Analog Input/Output Interface	BNC Connector x3, S Terminal Output Mount
Digital Input/Output Interface	16 Pin Header Mount
Action Mode	MC141622 Supports All Operating Modes
Regulator	MC7805CT Use
Recommended Supply Voltage	+ 10 V
Operating Temperature	0 to 50°C
Supply Current	350 mA

3. BOARD OPERATION

3.1 ACF–II Operating Mode

AFC–II has four operating modes. Any one of these modes can be selected using the digital code input to MODE 0 and MODE 1 using ROTARY SW. The function of each mode is as follows.

(1) Normal fsc Mode

This is the mode for usual Y/C separation. It separates Y/C from the video signal that is input to the A/D converter.

The coring parameter of the vertical enhancer can be set up by the digital code that is input to C0 – C3 (block level parameter), C4 – C7 (white level parameter), and D4 – D7 (noise slice level parameter).

The clock is a 3.579545 MHz subcarrier input to the CLK connector; the built–in 4x PLL generates 4xfsc clock.

(2) Normal 4xfsc Mode

This mode is used for Y/C separation. It separates Y/C from the video signal that is input to the A/D converter.

The coring parameter of the vertical enhancer can be set up by the digital code that is input to C0 – C3 (block level parameter), C4 – C7 (white level parameter), and D4 – D7 (noise slice level parameter).

The clock is 14.31818 MHz which is a 4x subcarrier input to the CLK connector.

(3) Digital Input Comb Filter Mode

This mode uses the A/D converter, filter, and D/A converter as two independent blocks. The digital data converted by the A/D converter is output on C0 – C7. Data input on D0 – D7 is processed by the ACF–II. Filtering is performed by the algorithm of ACF–II and the Y/C video is output as analog signals from Y_{out} and C_{out}. These two blocks can operate with input clock signals that have different frequencies or phases and can be operated independently by using the CLK(AD) for the A/D converter, and the CLK input for the D/A converter.

The clock is 14.31818 MHz which is a 4x subcarrier input to the CLK connector and the CLK(AD) connector.

(4) Digital Output Comb Filter Mode

In addition to the normal Y/C analog outputs, the MC141622EVK can provide the Y/C signals as digital luminance and chrominance signals. The digital luminance data is output on C0 – C7 and the digital chrominance data is output on D0 – D7. This digital data can be modified by other digital processing.

The following table is the assignment for the operating mode.

MODE Switching Function

Mode	MODE1	MODE0	Rotary SW
Normal fsc Mode	L	L	0
Normal 4xfsc Mode	L	H	1
Digital Input Comb Filtering Mode	H	L	2
Digital Output Comb Filtering Mode	H	H	3

4. BK FUNCTION

By setting the BK pin (toggle SW1) to the H level, composite video is output on the Y_{out} pin and the chrominance signal on the C_{out} pin.

The following table is the function of the BK pin.

BK Function

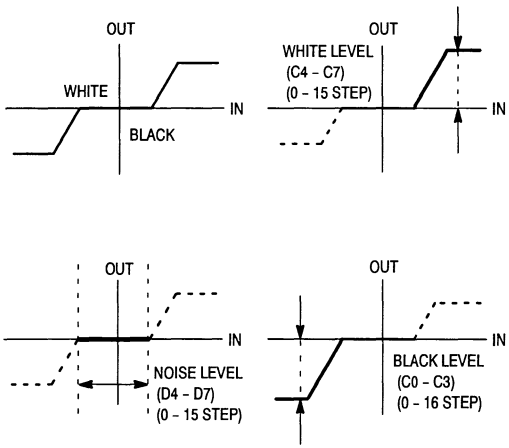
BK Pin	Y_{out} Pin	C_{out} Pin
L	Luminance	Chrominance
H	Composite	Chrominance

4.1 Vertical Enhancer Function

By setting the VH pin (toggle SW2) to the L level, the vertical enhancer feature is enabled. The coring parameter of the vertical enhancer can be set up every 1 LSB by the digital code that are input to C0 – C3 (black level parameter), C4 – C7 (white level parameter), and D4 – D7 (noise slice level parameter.

The set up level of the coring parameter and characteristics are as follows.

Coring Characteristics



Vertical Enhancer Function

VH Pin	Vertical Enhancer
L	On
H	Off

Coring Parameter Set Up

C7	C6	C5	C4	Level
C3	C2	C1	C0	
D7	D6	D5	D4	
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	A
H	L	H	H	B
H	H	L	L	C
H	H	L	H	D
H	H	H	L	E
H	H	H	H	F

4.2 Clock Generator Compounding

The clock generator (MC1378P) provides the necessary reference oscillator and phase locks the clock to the color subcarrier by inputting the composite video signal.

VC1 adjusts the horizontal VCO to synchronize the output of the burst gate (pin 5 on the MC1378P) with the input video signal. VC2 adjusts the chroma VCO for maximum amplitude output from the clock buffer (pin 1 on the MC14576).

VR3 adjusts pull–in of the chroma PLL filter. This is usually fixed to the center position. VR4 selects the dc bias for the clock buffer output and is usually 2.25 V.

4.3 Video Amplifier Adjustment

On the video amplifier (MC14577), the gain is adjusted by VR1. This sets the input range (3.0 Vp–p) of the A/D converter in MC141622FU.

VR2 is the clamp level adjustment. This adjusts the sync tip clamping of the input video signal to the video amplifier.

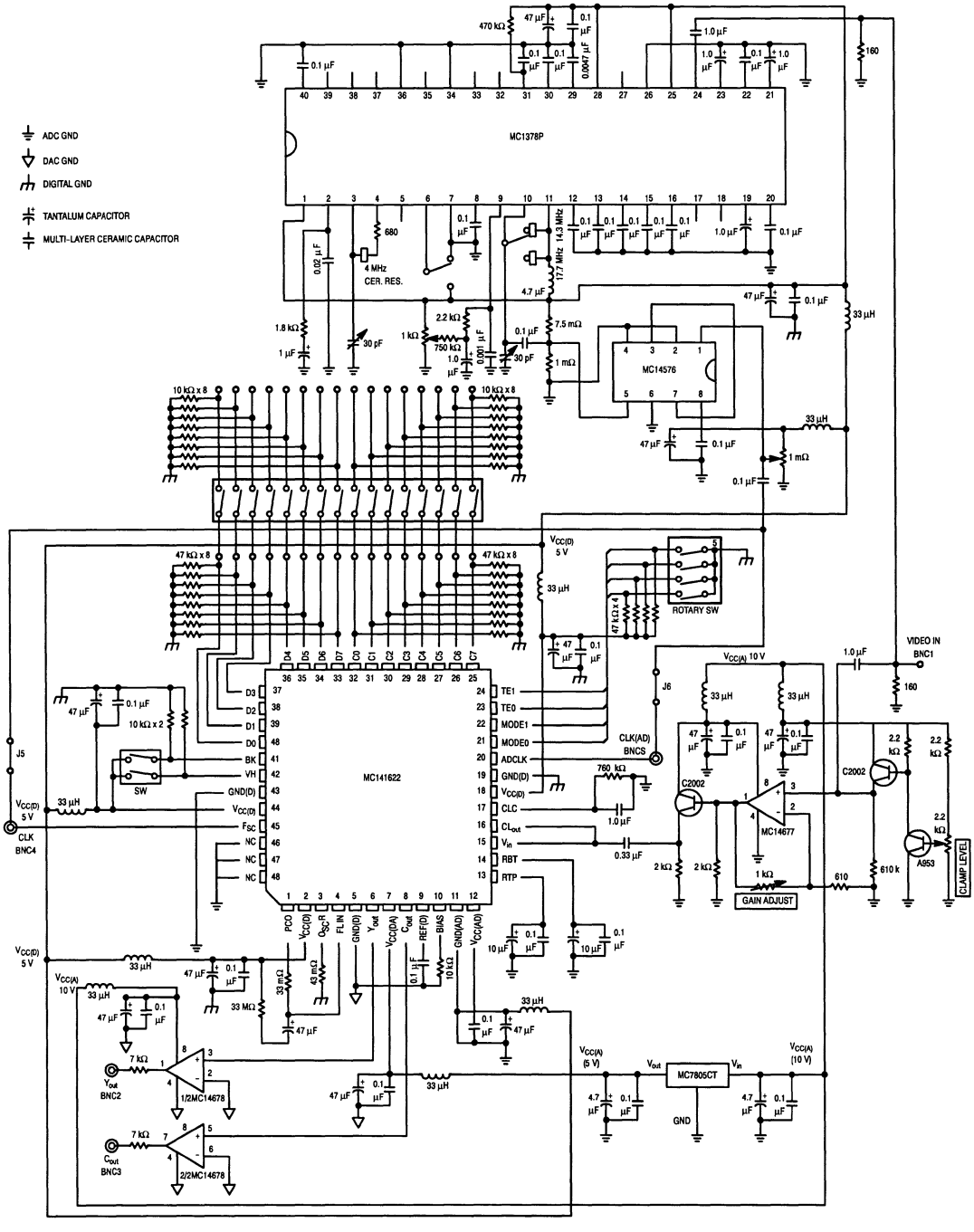
4.4 Outside Interface

The outside interface should provide a composite video input signal to BNC1. The MC141622EVK provides Y/C separation and outputs the luminance from BNC2 and the color signal from BNC3. There is an S output connector on this board for easy connection to instruments having an S input connector.

BNC4 and BNC5 are for the external input of each CLK and CLK(AD). However, when using these, it is necessary to modify the board pattern; i.e., cut (J5, J6).

There is no filter for bandwidth limitations on this board beyond that imposed by the bandwidth limitations of the MC14577 buffer amplifier. To minimize noise resulting from excessive bandwidth, the bandwidth of input video signal should be limited to no more than one half of the clock frequency.

5. MC141622EVK CIRCUIT

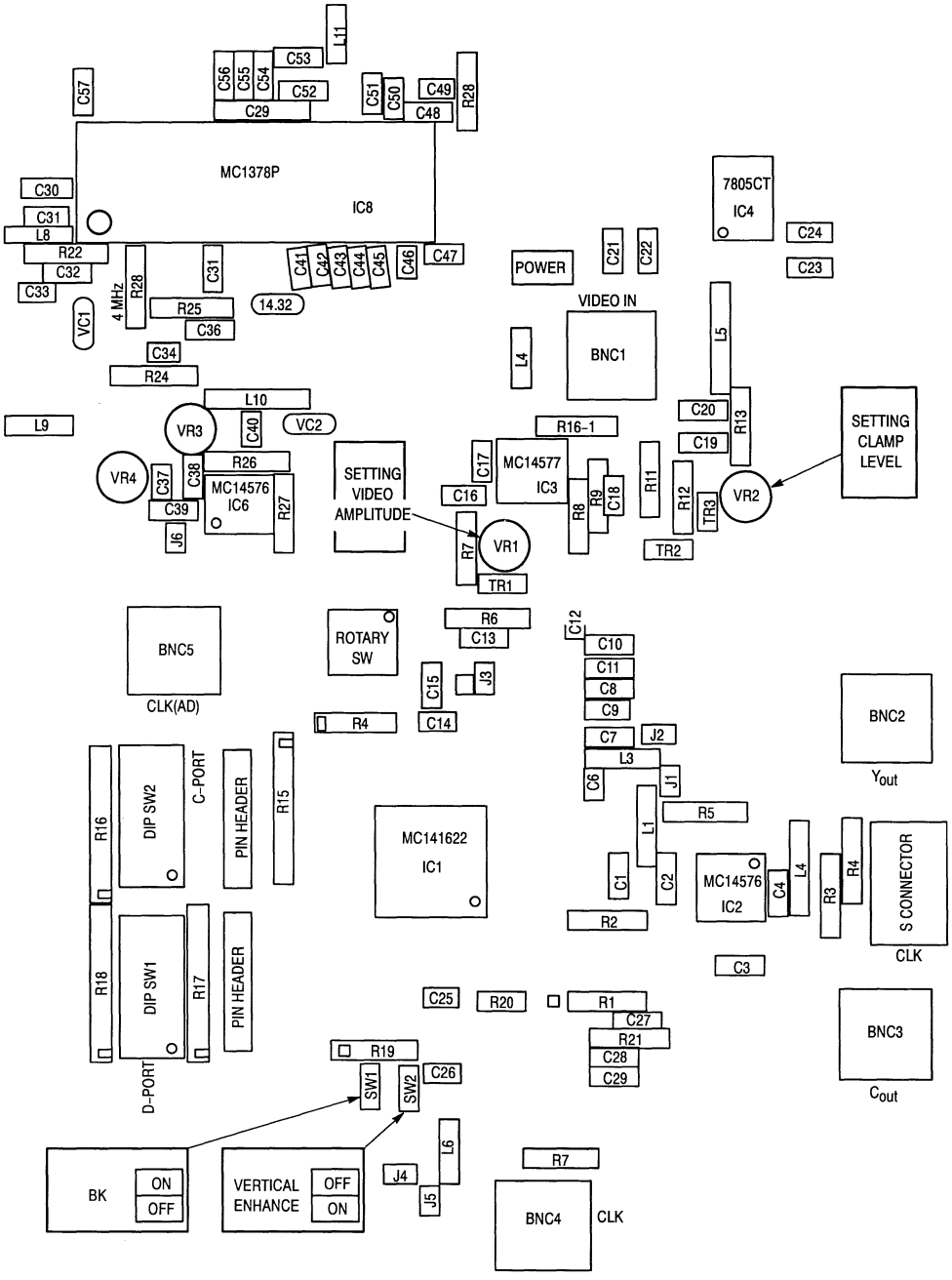


6. MC141622EVK PARTS LIST

Reference Designation	Description
IC1	MC141622FU
IC2	MC14576CP
IC3	MC14577CP
IC4	MC7805CT
IC5	MC14576CP
IC6	MC1378P
TR1	2SC2002
TR2	2SC2002
TR3	2SA953
R1	9.1 kΩ
R2	62 kΩ
R3, R4	75 Ω
R5	3.6 kΩ
R6	750 kΩ
R7, R8	2.0 kΩ
R9	510 Ω
R10	150 Ω
R11	510 kΩ
R12, R13	2.2 kΩ
R14	47 kΩ x 4
R15	47 kΩ x 8
R16	10 kΩ x 8
R17	47 kΩ x 8
R18	10 kΩ x 8
R19, R20	10 kΩ x 4
R21	200 Ω
R22	1.8 kΩ
R23	680 Ω
R24	750 kΩ
R25	2.2 kΩ
R26	7.5 mΩ
R27	1.0 mΩ
R28	150 Ω
R29	470 kΩ
L1 – L9	33 µH
L10	4.7 µH
L11	33 µH
VR1	1 kΩ
VR2	2.2 kΩ
VR3	1 kΩ
VR4	1 mΩ
VC1, VC2	30 pF
SW1, SW2	Toggle Switch
DIP SW1, DIP SW2	8 Channel Dip Switch
ROTARY SW	16 Channel Switch
	4 MHz Cer. Res
	14.32 MHz Crystal

Reference Designation	Description
C1	0.1 µF
C2, C3	47 µF
C4, C5, C6	0.1 µF
C7	47 µF
C8	0.1 µF
C9	10 µF
C10	0.1 µF
C11	10 µF
C12	0.33 µF
C13	1.0 µF
C14, C15	0.1 µF
C16	47 µF
C17	0.1 µF
C18	1.0 µF
C19	47 µF
C20, C21	0.1 µF
C22	47 µF
C23	0.1 µF
C24	47 µF
C25	0.1 µF
C26	47 µF
C27	10 µF
C28	0.1 µF
C29, C30	47 µF
C31	0.1 µF
C32	0.022 µF
C33, C34	1.0 µF
C35	0.1 µF
C36	0.001 µF
C37	47 µF
C38 – C45	0.1 µF
C46	1.0 µF
C47, C48	0.1 µF
C49 – C51	1.0 µF
C52	0.1 µF
C53	47 µF
C54	0.047 µF
C55 – C57	0.1 µF

7. MC141622EVK LAYOUT



MC144000EVK

Advance Information

PC Video Capture Evaluation Kit

The MC144000EVK PC Video Capture Evaluation Kit is the primary tool for evaluating and demonstrating the Motorola Video Capture Chip Set. The MC144000EVK provides the user with the hardware and software interface that is necessary to implement video devices on the PC in a Windows 3.1 or a Video for Windows environment. Key video devices on the MC144000EVK include: the MC141625 Advanced NTSC/PAL Comb Filter, the MC44011 I^2C Bus-Controlled Multi-Standard Video Processor, the MC44140 Chroma Line Delay, the MC44145 Pixel Clock Generator, the MC44200 Triple 8-bit Video DAC, and the MC44250 Triple 8-bit ADC.

General
- Provides Full-Motion Video on a Single ISA Board
- Multi-Standard Video – PAL and NTSC
- Two Video Inputs: Composite and S-Video
- Zoom, Window, Clip, Overlay, Scale Video Images
- Microsoft Video for Windows and Video for Windows Device Drivers Included

Hardware
- VGA 640 x 480 Pixels; 256 Colors
- 1M VGA RAM
- 1M Video RAM
- 65,536 Colors per TV Video Pixel 5:6:5 RGB Format
- Motorola Video ICs (MC141625, MC44011, MC44145, MC44140, MC44250, MC44200)
- Chips and Technologies 9001 Video Window Controller
- Standard 15-pin VGA Monitor Interface
- I^2C Bus Allows PC to Talk to MC44011 Registers
- Advanced Chroma Processing via Motorola Video Components
- Advanced Comb Filter for Less Color Interference

Software
- Windows 3.1 Application Drivers
- Video for Windows Application Drivers
- Windows DLL Image Processing Routines
- Freeze Frame Video
- Live Window Using Standard Windows WinSizing and Positioning
- Ability to Always Locate Live Video on Top of All Open Windows
- Ability to Store and Retrieve Captured Video Pictures
- Ability to Adjust Color, Offsets, and Sample x,y Ratio
- Built-in Debugger for MC44011 Registers Including I2C Communications

This document contains information on a new product. Specifications and information herein are subject to change without notice.

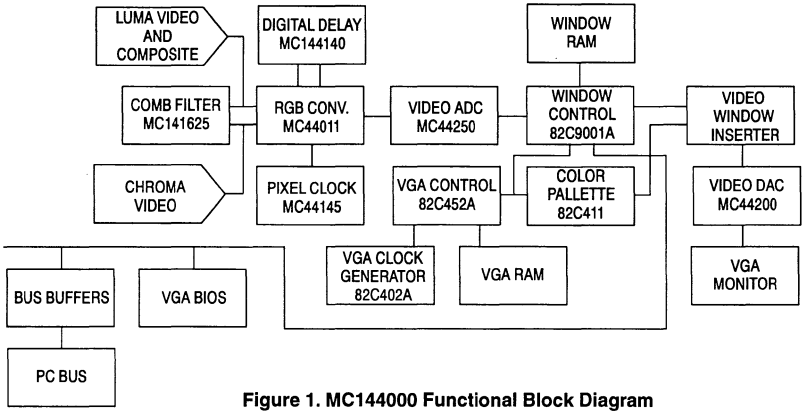


Figure 1. MC144000 Functional Block Diagram

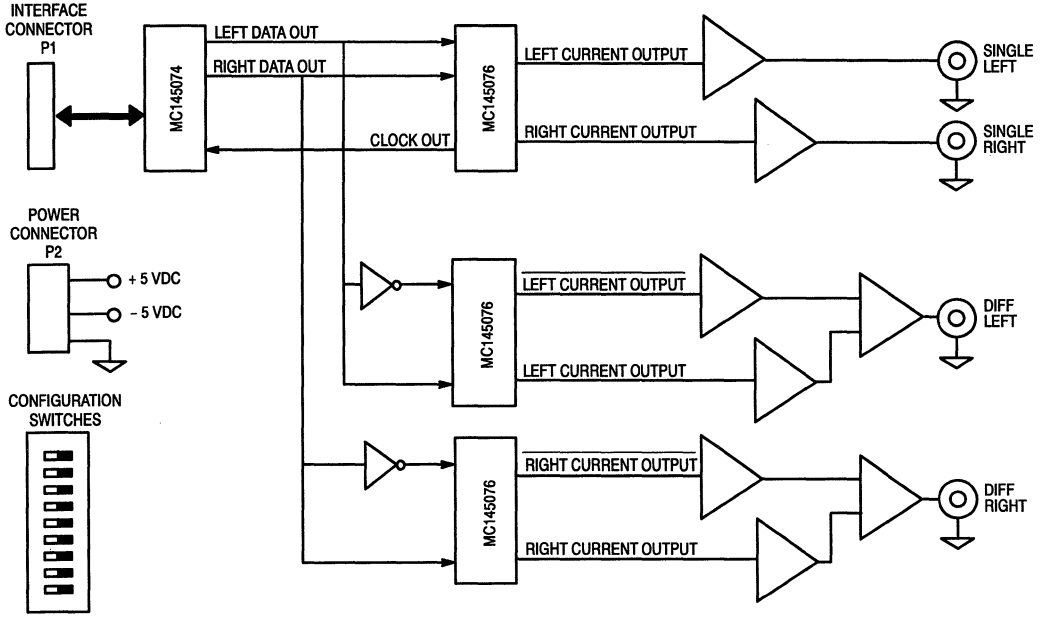
MC145074EVK

Product Preview

Stereo Audio Sigma-Delta DAC Evaluation Kit

The MC145074EVK Stereo Audio Sigma–Delta DAC Evaluation Kit is designed to demonstrate operation and performance of the MC145074 Stereo Audio Sigma–Delta DAC and MC145076 Stereo Audio FIR Smoothing Filter in both single–ended and differential operation modes. The Stereo Audio Sigma–Delta DAC Evaluation Board consists of the MC145074 Stereo Audio Sigma–Delta DAC, three MC145076 Stereo Audio FIR Smoothing Filters, four MC33077 operational amplifiers, and a hex inverter. Along with the active devices, the board contains a 20–pin connector for interfacing to external signals, five jumpers for routing of power and clock signals, and a 9–position DIP switch used to select between the various modes of operation.

- Multiple Performance Modes of the MC145074 and MC145076 Demonstrated
  - High Performance Single–Ended Mode Outputs
  - Ultra–High Performance Differential Mode Outputs
- Flexible Interface to Test Equipment or Customer System
  - 20–Pin Interface Connector Provides Easy Access to Key Signals
  - Easily Interfaced with MC56000 Family of DSPs
  - Compatible with Industry Standard DAC Interface Format
- Interfaces to Motorola AES/EBU Interface Engineering Evaluation Board
- Generous Prototype Area
- Schematics, Data Sheets, and User's Manual Included



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Application Notes and Technical Articles

4

4

AN1235

A Set Top Closed-Caption Decoder

Prepared by: Onis Cogburn

INTRODUCTION

Designed primarily for the hearing impaired, closed captioning is applicable to many other applications. While the hearing impaired may benefit the most from the closed caption service, viewers without hearing problems can also benefit. The ability to read and hear the program or movie dialog will help both the young and the illiterate learn to read. Just being able to have the service available in noisy surroundings such as sporting events is attractive. The service is also expected to provide dual language capability in the near future. This feature can increase the literacy of the individual by providing a method for studying a foreign language. Being able to read in one language and hear the equivalent in a second language is an attractive method for learning a second language.

HISTORY

The present closed captioning technology has its beginnings in 1971. The National Bureau of Standards was studying the possibility of encoding real time clock information on line 1 of the vertical blanking interval (VBI). Engineers at the American Broadcasting Company recognized the technology as a way of transmitting closed captioning. ABC captioned an episode of "The Mod Squad" and showed it to a group of hearing impaired people near the end of 1971. The reaction of the test audience was so enthusiastic the NAB (National Association of Broadcasters) began studying ways of establishing a national closed captioning system. The Health Education and Welfare department provided funding for the development of encoders for the broadcast industry and low cost decoders for use by viewers while PBS provided the initial expertise for the design of this equipment.

In 1976 the Federal Communications Commission (FCC) set aside line 21, field 1 of the VBI specifically for closed captioning. ABC, NBC, and PBS agreed to participate in the closed captioning service. The National Captioning Institute (NCI) was created to provided an organization to produce captions and promote the service. In 1980 the closed captioning for the hearing impaired officially made its debut as a nationwide service.

Although it was hoped public pressure would drive the development of the technology, the service languished until Congress, after many hearings and the assurance that cost would be small, passed the Television Decoder Circuitry Act of 1990. This legislation requires all TVs sold after July of 1993 that have screens larger than 13 inches have circuitry for decoding line 21 closed captioning.

EEG Enterprises, a long time pioneer in the closed caption industry, partnered with Motorola to produce the MC144143 Closed Caption Decoder IC. The device provides an economical solution for decoding and displaying closed captioning on TV. The MC144143 may be designed into existing circuitry to produce TVs and VCRs capable of decoding and displaying closed caption data or it may be used to build a stand alone decoder for TVs presently in use.

HOW CLOSED CAPTIONING WORKS

Line 21 of field 1 of the NTSC VBI contains the closed caption information. The structure of the line 21 is shown in Figure 1. The information contained in line 21 contains not only raw data but also timing information. A "color burst" is present on the "back porch" of the horizontal sync pulse and seven cycles of the 503.5 kHz "run–in clock" burst is transmitted following the color burst information. Immediately following the run–in clock is a 4.15 μs interval for stabilizing of the data collection clock and locking and with the run–in clock burst. Following this "timing" interval is a start bit followed by 16 bits of digital information transmitted as two 8–bit words formatted per the USA Standard Code of Information Interchange (USASCII;x3.4–1967) with odd parity. The clock rate of 503.5 kHz is 32 times the horizontal sweep frequency.

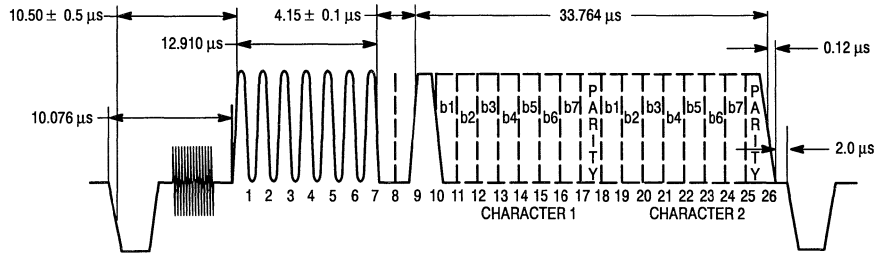


Figure 1. NTSC Line 21 Timing

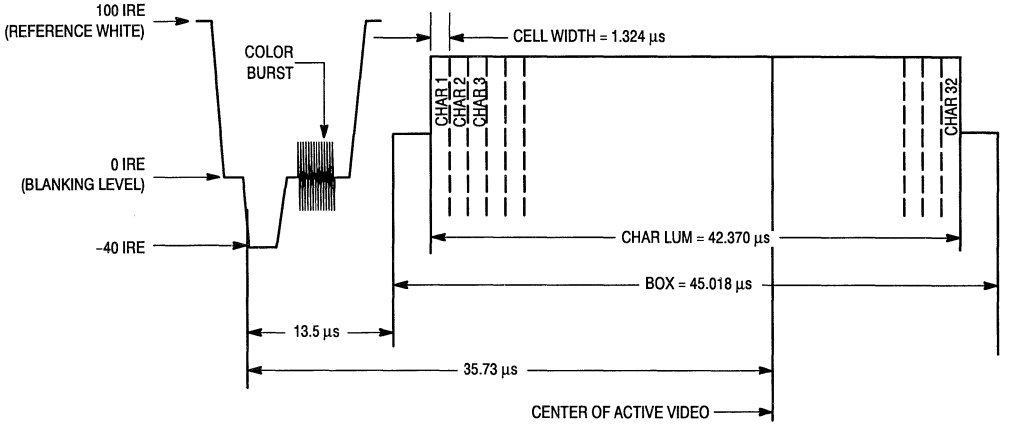


Figure 2. Character Box Timing

The data format chosen for the closed caption system is a modified ASCII table. The normal 7–bit ASCII table defines two types of characters, non–printing control characters used for command execution and printable text characters. The non–printing control codes have been expanded to include additional commands necessary for the smooth operation of the system. The asterisk, back slash, up carat, underline, apostrophe, brackets, and tilde were replaced with accented foreign characters to facilitate the display of non–English languages. In addition, 15 additional characters were defined by special character commands. Refer to the MC144143 data sheet for a description of these characters and the control codes used for positioning, text manipulation, and processor instructions.

THE MC144143

The heart of the Closed Caption Decoder discussed here is the MC144143. This device contains all of the circuitry necessary for detecting line 21, slicing and decoding the digital data from line 21, and organizing the data into a format presentable for NTSC TV display. It contains a character ROM containing all of the modified ASCII characters defined by the FCC specification for closed captioning. The display is a character ROM based type with the ability to place text anywhere on the TV screen as defined by the line 21 control codes.

The MC144143 is a line–21 closed–caption decoder intended for use in television receivers or set–top decoders conforming to the NTSC standard. The capability for processing and displaying all of the latest standard line–21 closed–caption format transmissions is included. The device requires a closed–caption encoded composite video signal, a horizontal sync signal, and an external keyer to produce captioned video. RGB outputs are provided, along with a luminance and a box signal, allowing simple interface to both color and black–and–white TV receivers.

SECTION 1

The simplified decoder operation is shown in Figure 3. The MC144143 decoder circuitry along with an analog switch (video mux) is sufficient to decode the line 21 information and integrate the information into the TV display. The MC144143 decodes the line 21 information and from this information determines what text will be displayed and where on the screen it will be displayed. The output of the decoder chip is a luminance (or RGB) video signal representing only that part of the display where the text is to be displayed. The "BOX" signal is a control signal which tells the analog switch when text is to be displayed.

The video signal is routed to both the MC144143 and one input of the analog switch. Unless text information is present (indicated by the BOX output), the video signal will be passed through the analog switch unaffected. When the

BOX signal indicates the presence of text information, the analog switch (video mux) selects the "LUM" signal (luminescence or brightness), from the MC144143 and passes this signal to the output. This switching always occurs within the line. Normal video is presented at the output of the analog switch before any text appears on a line and after the text ends on that line. This is to ensure that sync and color burst information are unaffected by the decoding and display process.

A typical application circuit is shown in Figure 4. The values shown on the schematic are the recommended values for most applications. (For specific implementations and for loop filter calculations, refer to the MC144143 data sheet.)

The video buffer may be of any design capable of driving a 470 ohm load with voltage gain of one. The video line driver design depends on the particular application (output impedance, output voltage, etc.) for its design and may or may not include DC restoration as one of its features. The analog switch may be as simple as a pair of DMOS transistors or a complete analog switch such as the MC74HC4053.

Display storage is accomplished with an on–chip RAM. A modified ASCII character set, which includes several non–English characters, is decoded by an on–chip ROM. An on–screen character appears as a white or colored dot matrix on a black background.

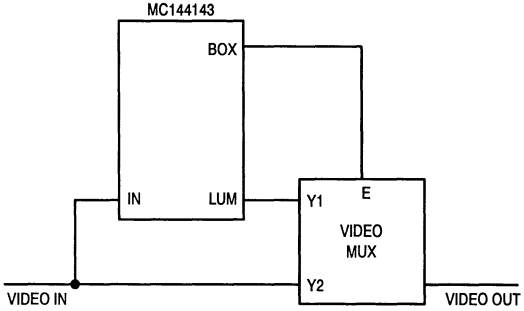
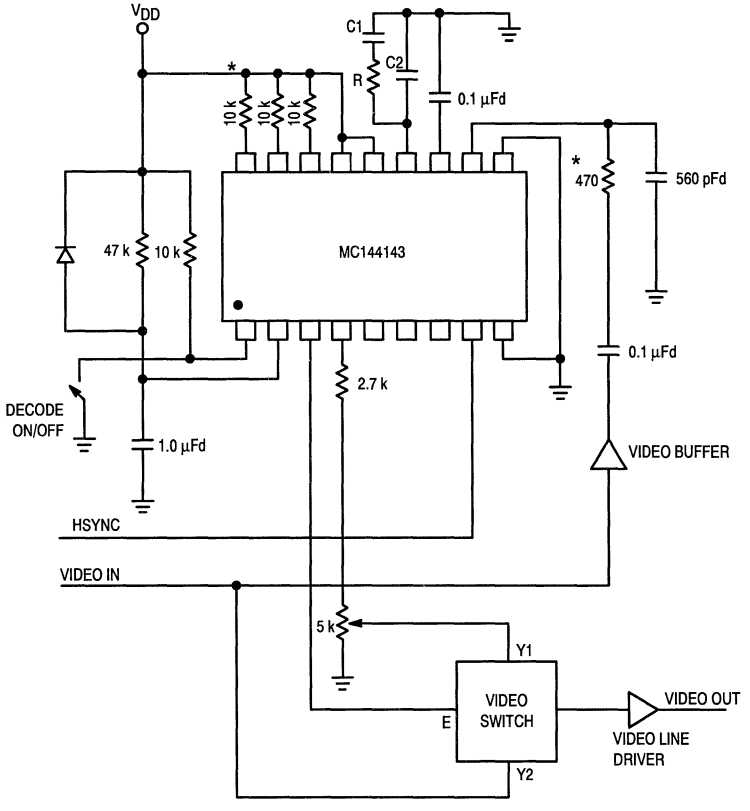


Figure 3. Simplified Decoder



* Decouple V_{DD} to V_{SS} with 0.1 µFd low ESR caps between pins 14, 15 and 9, 10 keeping leads as short as possible.

Figure 4. Typical Application Circuit

Captions (video–related information) can be up to four rows appearing anywhere on the screen and can be displayed in two modes: roll–up or pop–on. With roll–up captions, the row scrolls up and new information appears at the bottom row each time a carriage return is received. Pop–on captions work with two memories. One memory is displayed while the other is used to accumulate new data. A special command causes the information to be exchanged in the two memories, thus causing the entire caption to appear at once.

When text (non–video related information) is displayed, the rows contain a maximum of 32 characters over a black box which overwrites the screen. Eight rows of characters are displayed in the text mode.

An on–chip processor controls the manipulation of data for storage and display. Also controlled are the loading, addressing, and clearing of the display RAM. The processor transfers the data received to the RAM during scan lines 21 through 42. The operation of the display RAM, character ROM, and output logic circuits are controlled during scan lines 43 through 237. Several functions of the MC144143 are controlled via a port which may be configured to be serial or parallel.

Characters are displayed as white or colored, dot–matrix characters on a black background. The characters are described by a 6–by–9 dot pattern within a character cell which is 8 dots wide by 13 dots high. This provides a one–dot border of black around each character and provision for one row for underline, offset by a row of black, between the character and the bottom edge of the cell. Character luminance has normally been set at 90 IRE units and the surrounding black box at 10 IRE units.

The Character ROM contains a ***dot–matrix*** pattern of each character. Each ***dot*** from the character ROM represents a single picture element or 'pixel' and each picture 'dot' is made up of a square of four pixels. Pixels 1 and 2 are generated during field one and pixels 3 and 4 during field two. Alternate rows and columns are read out of each field to produce an interleaved and rounded character. A display row contains a maximum of 32 characters plus a leading and trailing blank box, each a character cell in width, making the overall width of a display row 34 x 8 = 272 dots. Successive display rows are butted together, so that the total display is 195 dots high.

The black box (34 character cells wide by 195 dots high) results in a box size of 45.018 μs in width by 195 TV scan lines in height. A scan line is two adjacent picture lines. The first line is generated during field one and the second line is generated during field two. When centered in the video display, this box starts 13.5 μs after the leading edge of H in scan line 43 and extends to scan line 237. This places the display approximately within the safe title area for NTSC receivers. Character width is 42.37 μs and is approximately centered on the screen, resulting in a leading and trailing 1.32 μs black border.

For additional information on line 21 programming, loop filter calculations, EMI (electromagnetic interference) suppressions, and other MC144143 features, see the MC144143 data sheet.

THE SET TOP CONVERTER OPERATION

The closed caption set top decoder (Figure 6) is composed of two sections. The decoder section, composed of the MC144143, MC555, MC74HC4053, and the MC14576 with their associated circuitry. The decoder section accepts a composite NTSC signal input, decodes the line 21 information, mixes the normal composite video with the displayable closed caption text and buffers the output for monitor input or RF modulator input. The second section contains the MC1374 RF Modulator IC and its associated circuitry.

The MC144143 decoder circuit is the same as shown in the MC144143 data sheet. Of particular importance is the network tied to pin 13 and that associated with pin 11. The input circuitry of pin 11 of the MC144143 is a low pass filter for minimizing noise to the input clamp circuit and the network connected to pin 13 is the PLL loop filter network. Neither of these circuits should be modified without a good understanding of clamp circuits and PLL operation (see loop filter calculation section of the MC144143 data sheet).

The bandwidth of line 21 is limited to approximately 600 kHz. The 470 ohm resistor and the 560 pF capacitor connected to pin 11 of the MC144143 form a 600 kHz low pass filter. For most applications this is adequate. Some measure of improvement in noise immunity can be achieved by using a π type LC filter adjusted for 470 ohms impedance, but the cost of the components usually does not justify the improvement in performance. The input of the MC144143 is itself enough noise resistant for most applications.

The network connected to pin 13 of the MC144143 determines how the VCO within the decoder IC will respond to the video input signal. The VCO in the decoder IC must be able to handle a wide range of signal conditions. At one extreme is the weak or "snowy" picture. The decoder must be able to decode line 21 down to a condition where the picture borders on the unwatchable. In addition the text must be presented with a minimum of "jitter". At the other extreme is the necessity of decoding "bad" tapes; those from poor recordings or from rental stores where the tape has been stretched from repeated playing.

When presented with a weak signal, the VCO within the PLL circuitry of the MC144143 will be continually bombarded with noise which will tend to cause the VCO to bounce around. This is corrected by reducing the value of the resistance in the loop filter while increasing the capacitance in series with this resistance. This must be adjusted along a precise curve dictated by a set of complex equations (see loop filter calculation section of the MC144143 data sheet). Although these values can be arrived at empirically, it is time consuming and requires sophisticated testing equipment. Acceptable values for reasonable jitter with weak signals are 3.3K ohms to 4.7K ohms for R24 with a value for C5 of about 0.1 μF. The usual value for C6 is 3300 pF.

The disadvantage of using the lower resistance values (R24 = 3.3K ohms) is stability problems encountered when using a VCR to display old or poorly recorded tapes. This difficulty is traceable to the design of the VCR recording mechanism. To record and playback video information, the VCR must be able to record one field as a single continuous track. This is done by spinning the record/playback head and wrapping the tape around the head mechanism so that the head is in contact with the tape for about 180 degrees of rotation. The information is then recorded as a diagonal strip of information on the tape. Two or more heads are mounted to the rotating mechanism and the signal switched between the heads so that one records/plays back the even fields and the other the odd fields. Head switching occurs normally in the

last few lines of a field; usually 5 to 10 lines before the end of the field but may occur on some recordings during the VBI (vertical blanking interval).

Herein lies the problem. As the tape is repeatedly played the tape will stretch. This is aggravated during the head switch line where the stretching causes the line containing the head switch "transient" to be longer. Additionally, poor equipment or misadjustment can cause excessive head switch "transients". Errors due to tape stretching and head switch "transients" of more than 15 μs can be observed in the normally 64 μs line length.

The error introduced by the head switch is referred to as a "transient" because it occurs only once per field; at the point of head switching. The VCO sees this transient as a jerk which causes the frequency to jump. The length of time necessary to return to its correct frequency is determined by the values chosen for the loop filter. For low values of R (3.3K or less), the VCO in the MC144143 may not be able to return to its correct operating frequency before line 21 is encountered. If its frequency is not correct, it will not decode the line 21 data. Values for R of 6.8K to 8.2K or higher with values of C5 less than 0.082 μF will ensure that nearly all tapes will be decoded, however, excessive jitter may result when very weak and/or noisy signals are decoded.

Pin 8 of the MC144143 performs a unique function. The frequency control for the decoder IC is a VCO in a PLL type of circuit. The reference frequency for the PLL operation is derived from the sync stripped from the composite video by the sync detector circuits within the MC144143. As long as composite video is provided, the VCO will be locked to the horizontal sync signal.

During normal operation, a video signal will not always be available. When changing TV channels or when the VCR is not on, no video will appear at the input of the decoder. In these cases, the VCO would drift due to lack of reference input. The designers of the chip realized this and added an additional input for a second reference frequency; this is pin 8.

Pin 8 does not function the same as the reference signal derived from the video signal. Its purpose is only to keep the VCO within a range that will allow the PLL circuitry to "pull–in" and lock to the horizontal sync of the composite video signal. Normally this signal is derived from the sweep circuits of the TV receiver. In the set top closed caption decoder circuit we use a 555 timer circuit to generate a 15 kHz signal which functions as a frequency control when a video signal is absent.

The question invariably arises, "Why not use the output of the VCR or the video signal itself as an input for this pin?" The answer lies with the previous discussion of the VCR operation and the effects of the head switch. The video signal can be decoded and the sync stripped off and used as an input to pin 8 but the circuitry would be at least as complicated as the 555 circuitry and with VCR operation, the head switch results in an excessive amount of jitter as the VCO is jerked around during the switch.

Q2 is a simple video buffer and 600 kHz filter for the video input to the MC144143. An integrated circuit current buffer could be used; however, none can approach the cost of a simple emitter circuit using the venerable 2N3904 (or equivalent). The filter itself is the two components R18 and C10 whose function was discussed previously. As pointed out in the discussion of the MC144143, a more sophisticated filter such as an LC filter could be used but probably wouldn't improve performance enough to offset the added cost.

The MC74HC4053 is four single pole double throw analog switches. The speed of this device is adequate for pixel by pixel switching of NTSC generated video. Although only one of the four switches is needed and the required operation could be obtained from discrete DMOS FETs, it is still probably the cheapest. The "BOX" output of the MC144143 is used to control the switch and determines whether the decoded closed caption text or normal video appears at the output of the '4053. This switching is done intraline so that normal video sync and color burst information are not interrupted by the decoder. Normal video is always present at the beginning of every line and at the end of every line. Closed caption text is present only within the line and only during the lines chosen during the encoding. The position of the text is always predetermined at the time of encoding of the video signal.

U3, the MC14576C, is a dual video amplifier. The on–chip gain–selling resistors set the noninverting gain of the MC14576C to 6 db. The (A) section is used as a buffer/video clamp. The (B) section is a line driver output for monitor connection. The extra circuitry connected to the (A) section is necessary because of the nature of the video signal. The composite video signal is a non–symmetrical voltage. The positive peaks of the waveform do not equal the negative peaks. While this is necessary to convey the video information, it does pose a problem that must be addressed. The dc level of the video waveform is continually changing. If some method is not used (i.e., a dc restoration circuit for example), the intensity of the closed caption text will vary line by line and be determined by the background brightness. Q1 and associated circuitry reduce this condition to an acceptable minimum.

Input video from J1 is passed to pin 3 of U3A by the video switch U4. C3 will charge through R3 causing the voltage on pin 2 of U3A to rise. Since this pin is the inverting input of the op amp, the output voltage, pin 1, will fall. When this voltage drops to approximately 0.7 V, Q1 is turned on clamping the output of U3A and preventing the voltage from dropping any lower. The video input at pin 3 of U3A will result in an output where clamping occurs at the negative sync tips. This maintains the dc value essentially constant, varying only minimally during the VBI.

THE RF MODULATOR

If viewing on a standard TV is to be expected, a RF modulator must be incorporated into the circuitry. This device accepts the output of the decoder plus audio obtained from a separate source (such as the audio output of a VCR) and produces a TV signal (usually on channel 3 or 4). The PC board layout provides a space which may be allocated for RF modulator circuitry. The RF modulator chosen may be a general purpose stand alone type, a PCB mountable module, or an IC such as the MC1374. An optional audio amplifier (shown in Figure 5) may be incorporated where the standard VCR audio output is insufficient to drive the audio input of the RF modulator chosen.

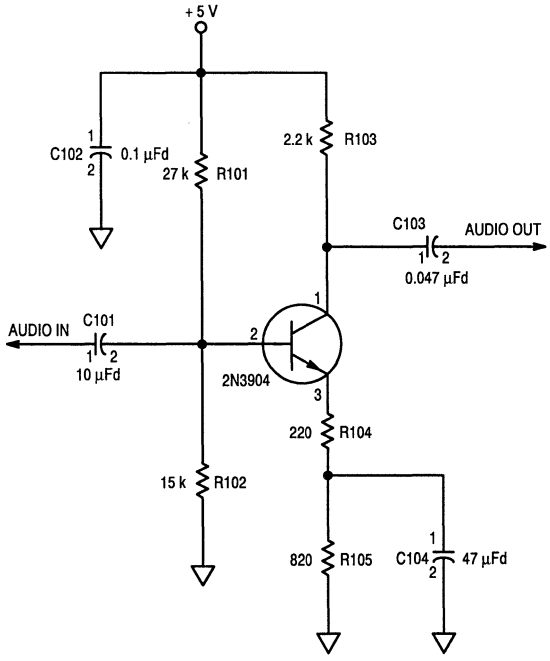


Figure 5. Optional Audio Amplifier

4

The MC1374 and associated circuitry can form the RF modulator for the decoder. Video information from the decoder and audio from the VCR modulate the carrier generated by the MC1374 to produce a TV signal receivable on channel 3 or 4 by a NTSC television receiver. For a complete description of the MC1374 operation, please refer to the data sheet for the MC1374 and/or the AN829 application note.

POWER SUPPLY

Power for the set–top–decoder is obtained from any convenient AC source whose RMS value is between 10 Vac and 20 Vac. The AC is rectified by diode D4 and filtered by the electrolytic capacitor C24. An inexpensive MC7805 voltage regulator is used to obtain the necessary 5 V supply voltage. Additional filtering is provided by the electrolytic capacitor C23.

In cases where weak channel reception of channel 10 is expected. EMI may occur due to the digital nature of the MC144143. A ferrite bead (RFB) has been placed in series with the V_{DD} pins along with a 0.1 μFd capacitor to suppress this EMI. This is sufficient for the PC board layout shown at the end of this document, but if a double sided or single sided PC board design without ground plane is contemplated, it is recommended the EMI information in the MC144143 data sheet be referred to prior to design.

REFERENCES

1. "Closed Caption Decoder", Motorola Data Sheet MC144143/D.
2. "Color TV Modulator with Sound", Motorola Data Sheet MC1374/D.
3. "Triple 2–Channel Analog Multiplexer/Demultiplexer", Motorola Data Sheet MC74HC4053/D.
4. "Dual Video Amp for 5 V Operation – "C" Version", Motorola Data Sheet MC14576C/D.
5. "Timing Circuit," Motorola Data Sheet MC1455D/D.
6. "Fixed–Voltage, 3–Terminal Regulator for Positive Polarity Power Supplies", Motorola Data Sheet MC7805/D.

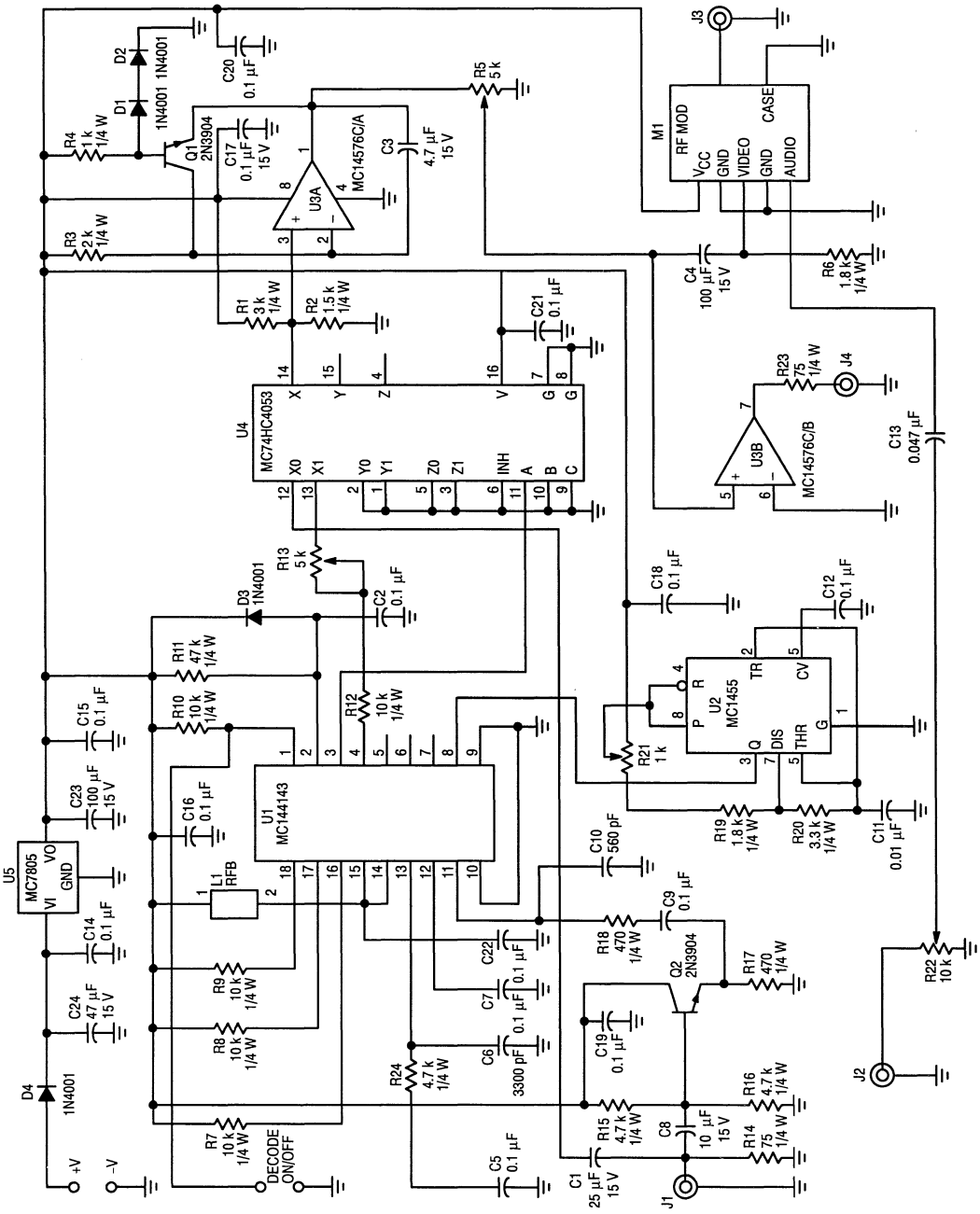
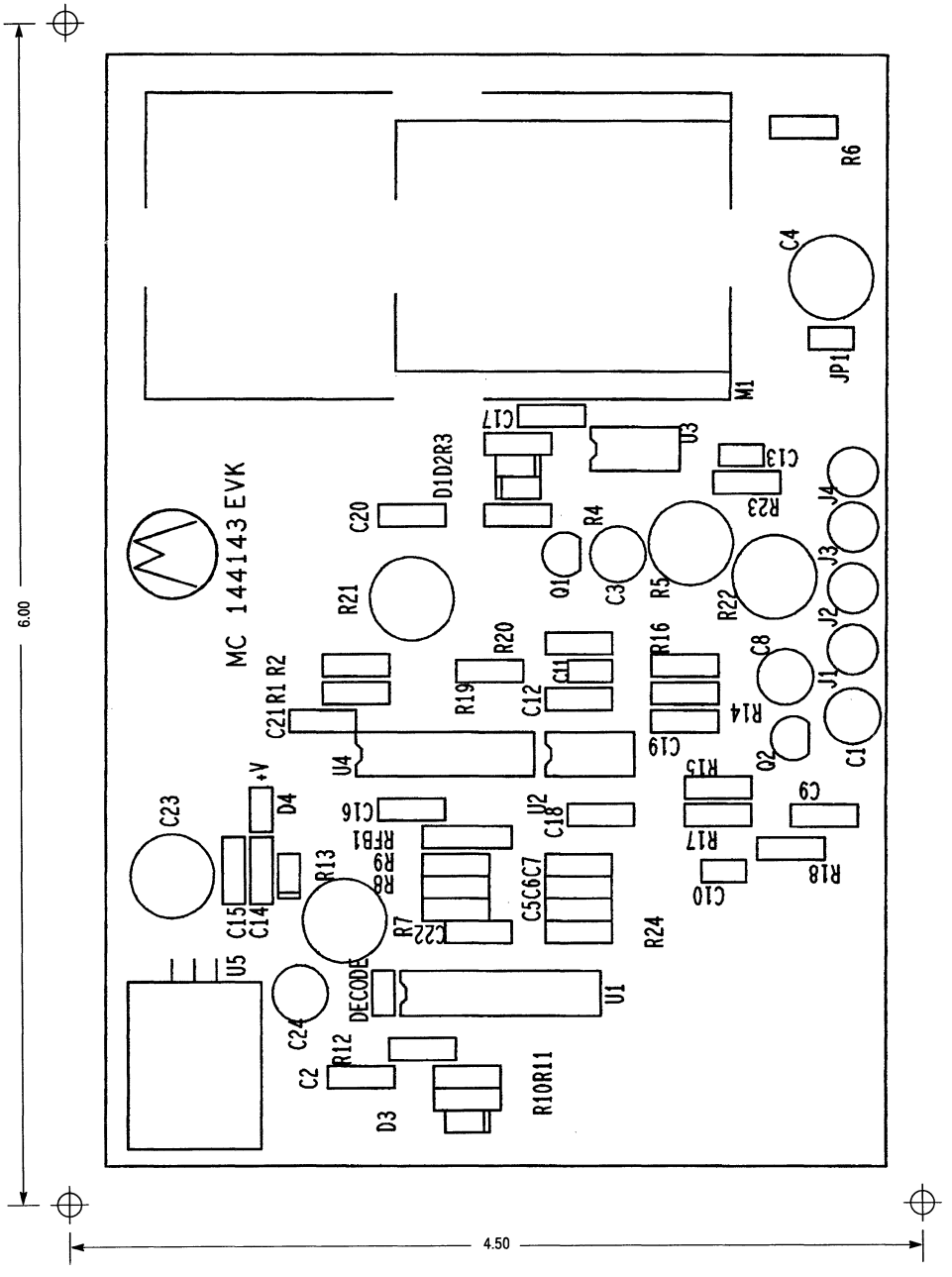
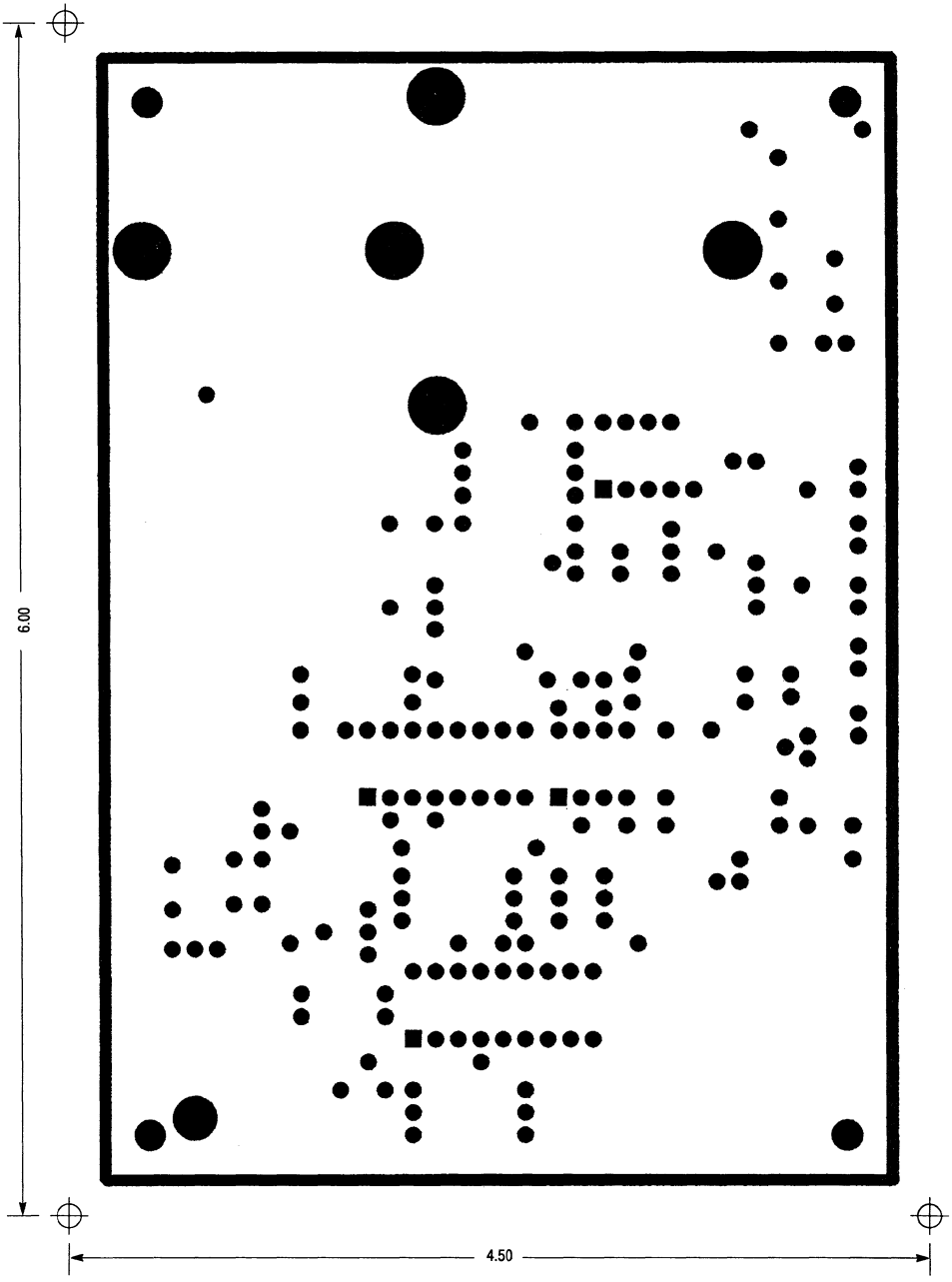


Figure 6. Set Top Decoder Schematic

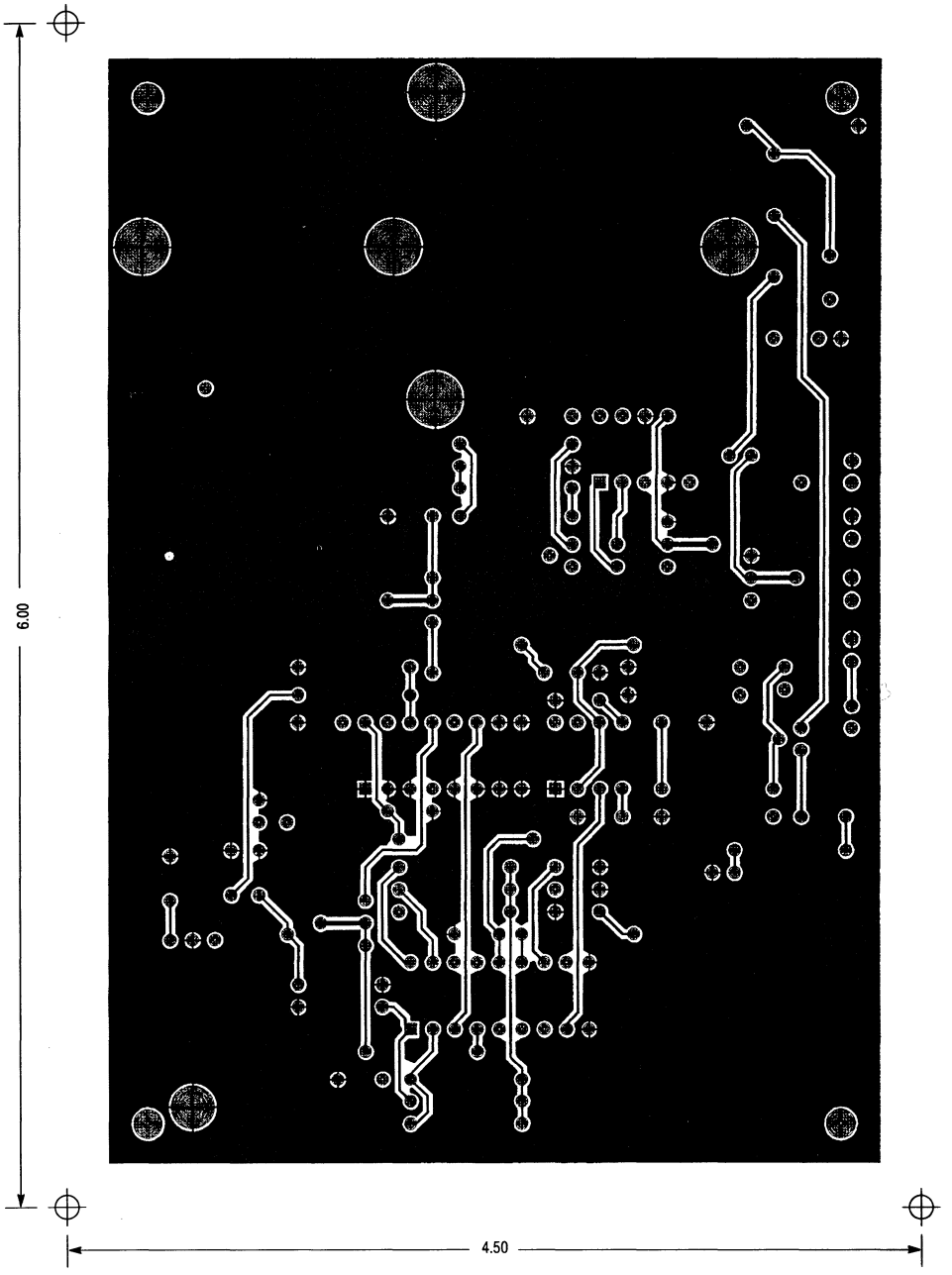
COMPONENT SIDE SILKSCREEN



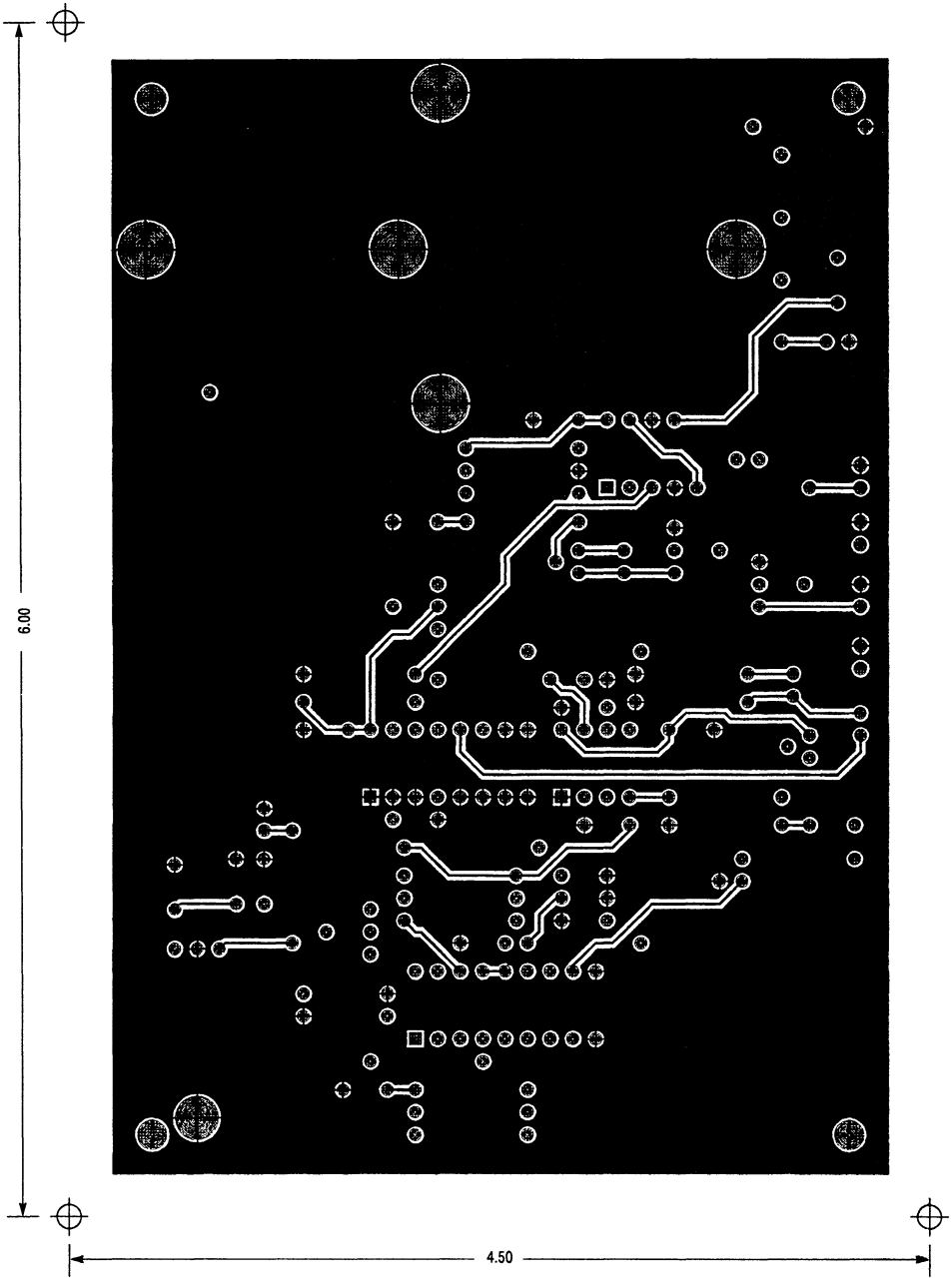
COMPONENT SIDE SOLDERMASK



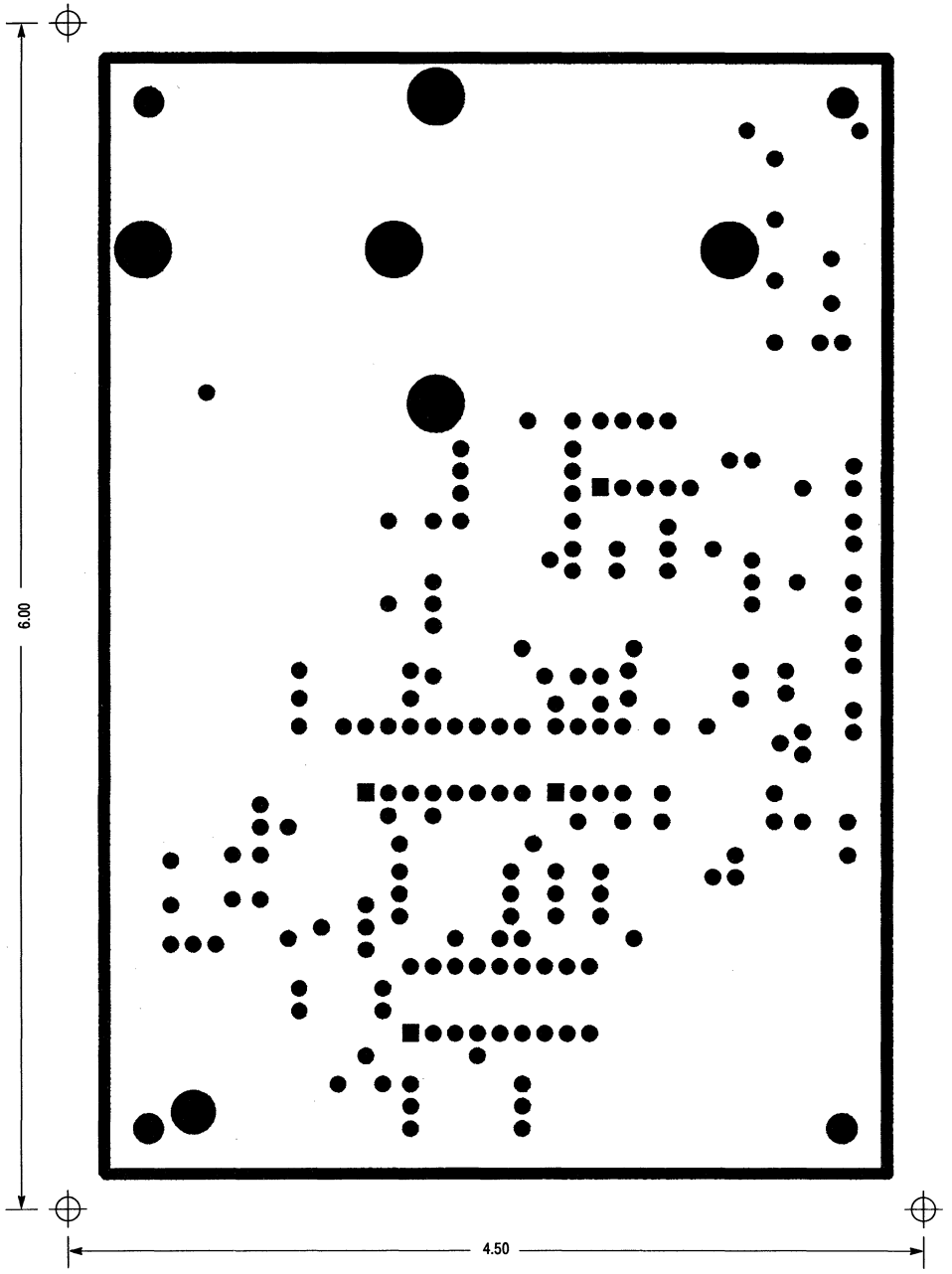
TOP, SIGNAL 1, LAYER 1



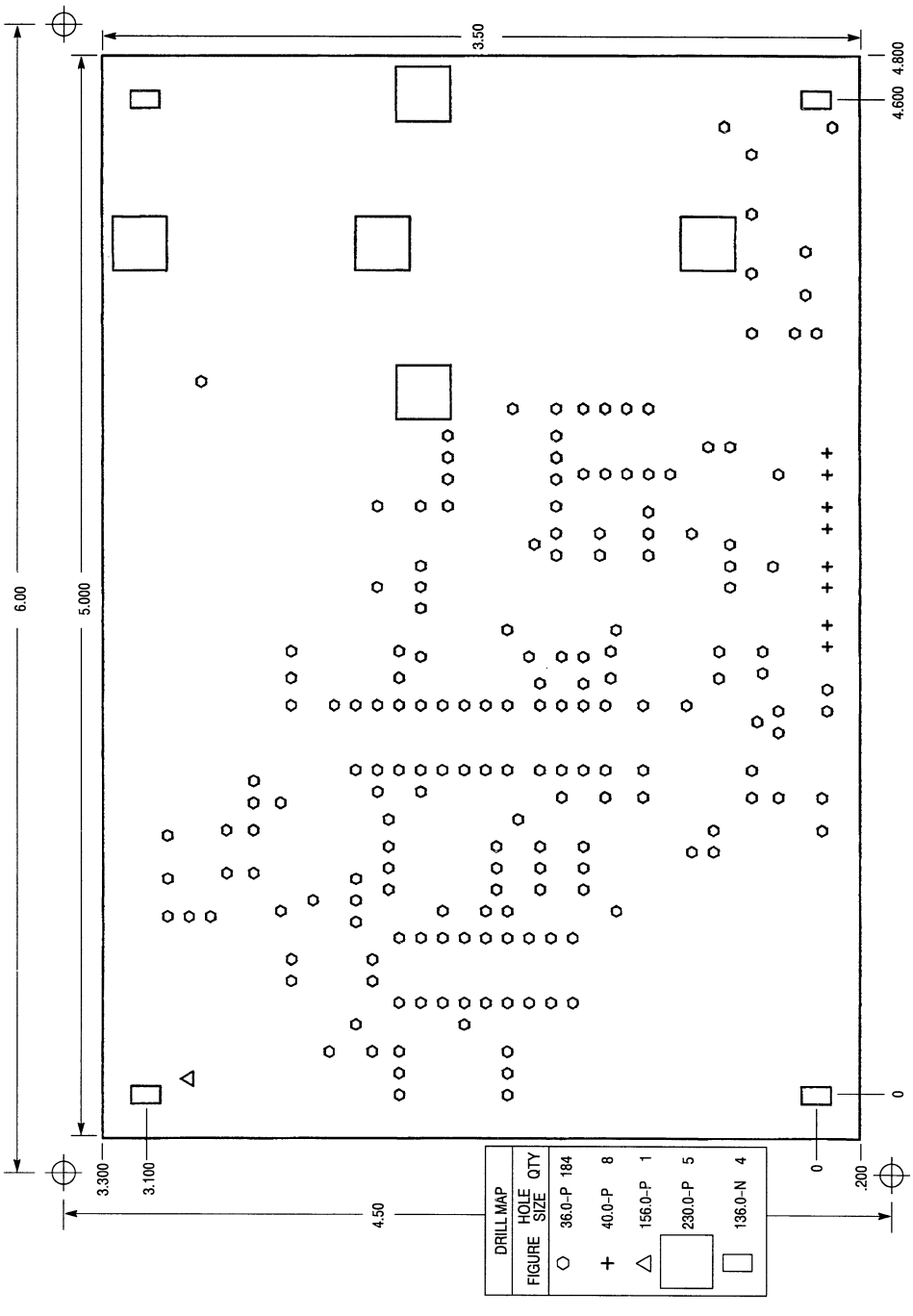
BOTTOM, SIGNAL 2, LAYER 2



SOLDER SIDE SOLDERMASK



DRILLMASTER



TV SET TOP CLOSED–CAPTION DECODER PARTS LIST

Item	Quantity	Reference	Part
1	1	R19	1.8 k
2	5	J1, J2, J3, J4, + V	
3	1	C1	25 µF
4	13	C2, C5, C7, C9, C14, C15, C16, C17, C18, C19, C20, C21, C22	0.1 µF
5	1	C3	4.7 µF
6	2	C4, C23	100 µF
7	1	C6	3300 pF
8	1	C8	10 µF
9	1	C10	560 pF
10	1	C11	0.01 µF
11	1	C12	0.1 µF
12	1	C13	0.047 µF
13	1	C24	47 µF
14	3	D1, D3, D4	1N4001
15	1	D2	1N4001
16	1	Decode	On/Off (SPST Switch)
17	1	L1	RFB (Ferrite Bead)
18	1	M1	RF Mod
19	2	Q1, Q2	2N3904
20	1	R1	3 k
21	1	R2	1.5 k
22	1	R3	2 k
23	2	R4, R21	1 k
24	2	R5, R13	5 k
25	1	R6	1.8 k
26	6	R7, R8, R9, R10, R12, R22	10 k
27	1	R11	47 k
28	2	R14, R23	75
29	3	R15, R16, R24	4.7 k
30	2	R17, R18	470
31	1	R20	3.3 k
32	1	U1	MC144143
33	1	U2	MC1455
34	1	U3A	MC14576B/A
35	1	U3B	MC14576B/B
36	1	U4	MC74HC4053
37	1	U5	MC7805

AN1244

A Single Board CD-i Player with MPEG Extensions

Prepared by: Craig McAdam, Multimedia Systems Group, Motorola, Scotland

INTRODUCTION

Compact Disc Interactive is a multimedia platform for combining audio and video along with text and graphics onto a single compact disc. Playback of this disc through the TV screen , controlled interactively by the viewer, delivers a true multimedia system for home or business providing education, entertainment and information. A platform is required to allow designers to evaluate hardware and software solutions for CD–i systems and to evaluate the Motorola CD–i chip set. The system described in this application note integrates the Motorola chip set onto a single board to provide a complete CD–i player with the MPEG extensions as described in the Green Book.

Motorola currently has individual application boards for each component of the chip set (see references). These boards can be assembled into a rack to provide a complete system for evaluation and hardware/software development by the end user. The board described here provides a minimum glue solution to using the chip set, while still providing sufficient capacity for system development.

The design is modular in concept such that a potential user of the chip set can use this as a basis for their own design – using only those modules which are of interest and / or adding other modules of their own design. This application note contains design details, schematics, PAL equations and software examples for the board.

A feature of the design is the ability for any of the functionality of the design to be replaced by the equivalent function on a plug–in expansion card.

OVERVIEW

This design incorporates the MC68341 integrated processor, MCD210/211/212 video decoder and system controller (VDSC), MCD221 CD interface and audio processor (CIAP), and MCD270 MPEG1 video and audio decoder (IMPEG) to provide a complete CD–i player with MPEG extensions that conforms to the green book specification and demonstrates the advantages of using the MC68341 in a CD–i player.

The board provides a clear illustration of how to build a CD–i player using the Motorola CD–i chip set with a minimum amount of glue logic, and allows additional functionality to be added by means of a mezzanine expansion card which will plug into connectors provided on the board. This allow extras features (e.g., T1 capability) to be added to the system.

The modular nature of the design allows it to be used as the basis for derivative designs – modules may be removed, or others added, without upsetting the functionality of the remainder of the design.

A detailed description of the individual devices will not be given here – reference should be made to the appropriate data sheets. The board size has been chosen to allow mounting in an off the shelf desktop PC case. Headers have been provided to allow the LED indicators and pushbutton switches in such a case to be used. Suitable power supply connectors have been provided to allow the standard PSU in these cases to be used, and the standard disk drive mountings allow the SCSI disk drives to be fitted inside the case to provide a compact system.

A block diagram of the system is given in Figure 1, illustrating the modular nature of the design. Each module in the design will be considered in detail.

DESIGN FEATURES

- Order this Board by Part Number MMA282EVK
- MC68341 Operating at 16.67 MHz
- 4 Mbytes of System DRAM
- 2 Mbytes of EPROM
- 512 Kbytes of SRAM with Battery Backup
- CD–i Base Case Video Decoding (MCD210 / 211 / 212 VDSC) with 4 Mbytes of DRAM
- CD–i Base Case Audio Decoding (MCD221 CIAP)
- MPEG Video and Audio Decoding (MCD270 IMPEG) with 512 Kbytes of DRAM
- SCSI Controller with DMA Interface
- Mezzanine Expansion Interface Connectors

CPU MODULE

This provides the MC68341 CPU along with reset logic and battery backup control for the 68341's Internal Real Time Clock and for the Static RAM socket (described later).

Battery control is provided by a Maxim MAX791. This device also provides chip enable protection to the Static RAM socket during power up/down, and allows software to determine if the battery voltage has fallen to an unsafe level during the most recent period of backup.

The MC68341 is used in a mode which provides 24 address lines, eight programmable chip selects, seven interrupt request inputs and seven interrupt acknowledge outputs. A jumper selection allows two clocking options for the MC68341 – internal phase lock loop using an external 32.768 kHz crystal or an external clock oscillator module. The normal mode of operation is to use the internal phase locked loop to provide an operating frequency of 16.67 MHz. Fitting J18 causes the MC68341 to use an external oscillator. This external oscillator can provide a 1x or a 2x clock depending on the software setup of the MC68341.

CD–i is a registered trademark of Philips Consumer Electronics.

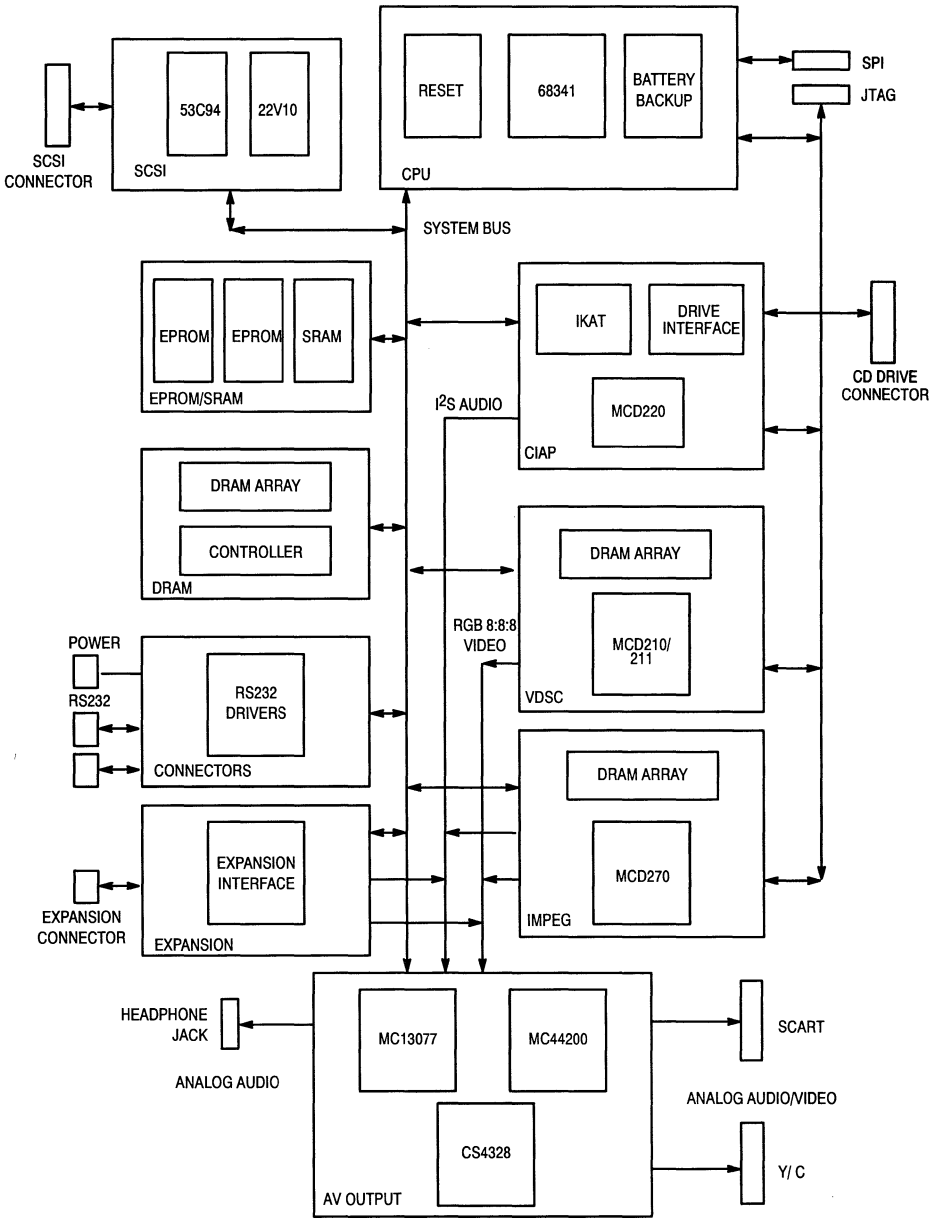


Figure 1. Block Diagram

The MC68341's SPI interface is unused in the Stingray+ design but is brought to header connector J14 for external access. J19 provides access to the MC68341's background debug signals.

For flexibility, the interrupt request signals to the CPU from the different modules and the interrupt acknowledge signals from the CPU to the modules will be mappable using jumper options. Interrupt request signals from the expansion interface, and the interrupt acknowledge to the interface bypass these jumpers.

Two serial channels are provided by the MC68341 and these are buffered to RS232 levels in the connector module. S1 provides a push–button reset for the board and S2 provides a de–bounced software abort signal to the MC68341 via INT7. A software reset facility is provided via output port pin PA0 through open collector driver U14B. An external reset input is provided by the EXTRST input to the CPU module. This can be driven from the JTAG test connector or from the expansion connectors. An open collector driver should be used to drive this input. By default the reset signal from the MAX791 is used as the reset input to the VDSC module. The reset output from the VDSC module is then used as the system reset signal for the MC68341 and the remainder of the board. This is in line with standard CD–i system design. However, if the board is not being used as a CD–i system, then the VDSC may not be fitted – in this case, solder link L27 allows the reset output of the MAX791 to be used as the system reset.

The ASn and AS68Kn signals are combined in U34D to provide a board activity indicator (LED D5 and / or an off-board LED connected via J21).

A facility is provided to reset the board under software control via bit 0 of MC68341 Port A. This bit is a general purpose I/O bit even while the remainder of the bits of Port A are used for IACK outputs. The following is the sequence that causes a software reset.

- ensure bit 0 of Port A data register contains logic '1'
- configure Port A as an output port (it is configured as an input port after reset)
- write a logic '0' to Port A data register bit 0

DRAM MODULE

This consists of two 16 bit banks of 1M x 4 DRAMS (four devices in each bank) to provide 4 Mbytes of DRAM closely coupled to the CPU.

The DRAM control logic is implemented in 22V10 programmable logic devices. These provide RAS, CAS, write enable and output enable controls for the DRAM array, address multiplexer control, and contain the DRAM controller state machine. The design files for these PALS are included in this application note. The DRAM controller inserts 1 wait state into each read or write access. Byte, word, and long word accesses to the DRAM are supported.

The controller design will also allow the use of 256K x 4 devices to provide a DRAM capacity of 1 Mbyte or 4M x 4 devices for a capacity of 16 Mbytes. Note, however, that the 4M x 4 devices are not pin compatible with the other devices and the initial PCB layout will not accommodate these. The default will be 4 Mbytes of DRAM.

The timer output of the MC68341 is used to provide the refresh request signal for the DRAM controller which uses the DRAM's CAS before RAS refresh mode. The power –up sequence required for proper DRAM device operation will be satisfied by using a simple delay routine in the EPROM code that will ensure that eight refresh cycles to the DRAM have taken place before any access is allowed.

Chip selection for the DRAM comes from the MC64341 using CS7, shared with the SCSI module. The DRAM controller will provide DSACK generation for this module.

VDSC MODULE

This uses the MCD210 (gate array) or MCD211 (standard cell) or MCD212 (standard cell with JTAG) Video Display and System Controller to provide the complete Base Case CD–i player video decoding functions.

The VDSC module uses 256K x 4 or 1M x 4 DRAM devices to provide 1 Mbyte or 4 Mbytes of memory respectively. The use of 256K x 16 DRAM devices is not be supported. The VDSC drives the DRAM array directly. The default option is to fit 1M x 4 devices for 4 Mbytes of memory.

Chip select generation for the VDSC is provided by the MC68341 using CS2. The VDSC DTACK signal is used to provide a 16 bit interface to the CPU. By default the VDSC interrupt request will be mapped to 68341 IRQ4. This can be changed by a jumper option in the CPU module.

The MCD212 differs from the MCD210 / 211 in having a JTAG interface. In the MCD212 some pins have been re–allocated to allow this interface. Solder links allow the fitting of any of the VDSC options.

VDSC Type	Solder Links
MCD210 / 211	L11, L13, L15, L17, L19, L21,L22
MCD212	L10, L12, L14, L16, L18, L20

In addition, the MCD212 part has an option to allow it to be used with a processor running at 25 MHz by introducing a delay in the DTACK generation to suit the faster bus timing. To enable this feature, solder link 23 should be fitted. By default solder link 24 will be fitted to suit a 16.67 MHz processor. Only one of these links should be fitted.

CPU Speed	L23	L24
16.67 MHz	Out	In
25 MHz	In	Out

To suit a system where a non JTAG VDSC is fitted, but it is desired to preserve the JTAG scan path on the board (see later), solder link L22 should be fitted.

VDSC DRAM banks can be enabled or disabled using jumper block J13.

J13 pins	Function
1 – 2	Enable bank2
3 – 4	Enable bank1
5 – 6	Disable bank2
7 – 8	Disable bank1

The default option is to fit J13 1 – 2, and 3 – 4, i.e enable both banks of DRAM.

The VDSC provides the VSDn signal to allow digital mixing of base case video from the VDSC with MPEG video from the IMPEG module. This signal is connected to the VDSC video output enable pin (OE) to disable the VDSC digital video outputs while MPEG video is displayed. The timing of the VSDn signal is determined by registers within the VDSC to define an MPEG display window.

Oscillator U25 should be chosen according to PAL or NTSC operation – 30 MHz for PAL or 30.2097 MHz for NTSC.

IMPEG MODULE

This uses the MCD270 (IMPEG) device to provide decoding of MPEG1 audio and video data according to ISO 11172.

The MCD270 requires 4 MBits of memory, and is normally provided by four 256K x 4 DRAMS. In this case 1M x 4 devides are used – these are easier to get, and consistent with the DRAMS used in other modules on the board. The IMPEG device drives this DRAM array directly. The IMPEG device can also use a single 256K x 16 DRAM for its memory,but this is not supported here.

The VSDn signal from the VDSC is used to enable the IMPEG digital video outputs to provide digital mixing of MPEG video with Base Case video.

The DRAM attached to IMPEG can be used as memory for MPEG decoding (system mode), or alternatively as DRAM for the CPU when MEG decoding is not in operation (transparent mode). Chip select generation for the IMPEG is provided by the MC68341 using CS3 (for system mode) and CS4 (for transparent mode). The IMPEG DTACK signal is used to provide a 16 bit interface to the CPU. By default the IMPEG interrupt request will be mapped to 68341 IRQ5. Jumper block J22 allows IMPEG to use MC8341 DMA channel 1 or 2.

Channel	J22 1–2	J22 3–4	J22 5–6	J22 7–8
DMA 1	In	Out	In	Out
DMA 2	Out	In	Out	In

The default is to use channel 1.

The JTAG interface in the IMPEG device has an additional pin (TRST) compared to the remainder of the devices on the board. Fitting solder link L26 allows this pin to be driven by the board's system reset signal. Fitting solder link L25 drives this pin with a separate local reset signal from comparator U53. This option allows the board to be kept in reset using the external reset input from the JTAG interface connector, while keeping the JTAG interface functional. The default is to fit L25.

CIAP MODULE

This module uses the MCD221 CD Interface and Audio Processor device to provide Base Case Audio decoding via its I^2S data input. The MCD221 also accepts MPEG audio data (on pins XCLIN, XWSIN, XDAIN) from the IMPEG module in I^2S format and provides mixing of the Base Case and MPEG audio data streams providing an I^2S output (on pins CLOUT, WSOUT, DAOUT) . CIAP also accepts the sub–code data from the CD drive.

Chip Select for the CIAP comes from the MC68341using CS5. The CIAP DTACK signal is used to provide a 16 bit interface to the CPU. By default the CIAP interrupt request is mapped to MC68341 IRQ6. Jumper block J26 allows CIAP to use MC68341 DMA channel 1 or 2.

Channel	J26 1–2	J26 3–4	J26 5–6	J26 7–8
DMA 1	In	Out	In	Out
DMA 2	Out	In	Out	In

Jumper J25 allows the CIAP clock input to come from either a local 33.8688 MHz oscillator or a clock signal from the expansion interface (this may be required for e.g. Video on Demand).

J25	CIAP Clock
1 – 2	Expansion clock
3 – 4	Local oscillator

The CD drive for Stingray+ is provided by the Philips 6001 Kit with DSA interface. DSA is a three line bidirectional serial interface utilising Data, Strobe and Acknowledge signals to send command information to the CD drive and receive status information from the CD drive. Data from the drive is in I^2S format with a separate sub–code data signal. The drive used is the Philips double speed CDM12.1N2 .

The DSA interface is handled using a MC68HC05i8 MCU (IKAT) which contains a 68000 processor interface. IKAT is an 8 bit device on the lower data byte of the MC68341. Chip Select for the IKAT comes from the 68341using CS6. The IKAT DTACK signal is used to provide the 8 bit interface to the CPU. By default the IKAT interrupt request is mapped to MC68341 IRQ3. Jumper option J23 allows the IKAT and CIAP interrupt requests to share the same MC68341 interrupt.

J23	IKAT interrupt
1 – 2	Shared with CIAP
3 – 4	Unique

PORTB of IKAT is used for the DSA interface. Signals from the DSA interface are buffered onto PORTB bits,PB0, PB1, PB2 using U59, signals to the DSA interface from PORTB bits PB4, PB5, PB6, and PB7are buffered with open collector driver U14 C, D, E, and F. 5 V and 12 V power for the CD drive are also provided on connector P15, along with the CIAP clock signal. This clock signal is necessary to synchronise the decoding circuits in the CD drive to the CIAP device. This requires a modification to be made to the CD drive circuits. The interface cable uses screened twisted pair cable.

Two push buttons S3 and S5 are provided for IKAT to provide a reset to the DSA interface if required and to open the CD drive tray.

An 8 bit DIP switch S4 is provided which can be read by the MC68341 via IKAT and used to enable or disable board functionality under software control (e.g. disable MPEG functions to evaluate a base case only system, or alter the memory map.)

IKAT has two serial ports and the signals from these sre brought to the expansion connectors. No buffering is provided for these signals. This allows additional serial capability to be added to the system on an expansion card e.g MIDI.

EPROM / SRAM MODULE

The EPROM capability is provided by two 8 bit EPROM sockets (upper and lower data bytes) supporting 128K / 256K / 512K / 1M x 8 EPROM or Flash memory devices. U1 is the upper data byte, U2 is the lower. There are no jumper options for the EPROM sockets.

The SRAM capability is provided by an 8 bit socket U3 connected to the upper data byte of the MC68341 and capable of supporting 8K / 32K / 128K / 512K x 8 static RAM devices. This socket will also accept a Real Time ClocK / SRAM module (e.g. SGS MK48T08 Timekeeper RAM, or Dallas DS1216 Smartwatch / RAM Socket) with built in battery. This socket may be powered by battery or by normal 5V power if battery backup is not required. If a 28 pin device is used in this socket, then it should be "bottom justified".

Jumper block J1 allows selection of the device type to be used in the SRAM socket, see the following table.

J1	Function
1–2	Connect A15 to pin 3 of U3
3–4	Connect A14 to pin 28 of U3
5–6	Connect 5 V power to pin 28 of U3
7–8	Connect A19 to pin 1 of U3
9–10	Connect A18 to pin 30 of U3
11–12	Connect 5 V power to pin 30 of U3
13–14	Connect VBACK to pin 30 of U3
15–16	Connect 5 V power to pin 30 of U3
17–18	Connect VBACK to pin 30 of U3

SCSI INTERFACE MODULE

This uses the NCR 53C94 chip to provide a single ended SCSI interface to ANSI X3.1986 standard. A 22V10 PAL converts MC68341 bus signals to 53C94 control signals and provides a dual address DMA interface – 68341 accesses to the SCSI DMA address range are used to generate DMA controlm signals with timing suitable for the NCR53C94. The design file for the PAL is included in this application note. Jumper J8 allows the interface to use either DMA channel 1 or 2 in the MC6834.

J8	DMA channel
1 – 2	Channel 1
3 – 4	Channel 2

For SCSI DMA cycles, the MC68341's DMA controller should be programmed for dual address, cycle steal mode of operation. The hardware does not support byte control for DMA transfers – the NCR53C94 should be programmed for non–burst mode DMA without byte control.

The NCR53C94 drives the SCSI interface directly.

Jumper option J9 allows connection of 5 V power to the SCSI interface connector to provide power for external SCSI terminators.

J9	
In	Power
Out	No power

Flip flop U20A is used as a monostable triggered by the REQ line on the SCSI interface to provide a SCSI activity indicator. This is buffered to drive an on–board LED and also an off–board LED connected via J10. Resistor packs RP2, 3, and 4 provided the on–board teminations required by the SCSI standard (220 / 330 ohms).

The SCSI module shares CS7 from the MC68341 with the System DRAM controller. PAL U19 generates a DSACK signal to produce a 16 bit interface. By default the SCSI interrupt is mapped to MC68341 IRQ2.

AUDIO / VIDEO OUTPUT MODULE

This module provides analog audio and video outputs. Left and right audio outputs are provided at line level on the SCARTconnector P1 and buffered to drive headphones via a jack connector P3. Left and right audio signals are mixed in U13B to provide a mono audio output.

The I^2S audio data stream containing mixed base case and MPEG audio from the CIAP module is converted to analog using a Crystal CS4328 Audio DAC.

Digital video data from VDSC and IMPEG is converted to analog video using the MC44200 Triple Video DAC. The outputs of the MC44200 are 1V p–p, buffered in video op–amps U12 A & B and U13A to provide 2 V p–p through 75 ohm resistors. Analog video is also provided in Y/C (Super VHS format) on P2 using the MC13077 PAL / NTSC encoder which uses the MC44200 video outputs along with a composite sync signal from the VDSC. Jumper options allow this device to operate in PAL or NTSC mode.

Mode	J2	J3 1–2	J3 3–4	J4 1–2	J4 3–4	J4 5–6	J4 7–8
NTSC	In	In	Out	In	Out	In	Out
PAL	Out	Out	In	Out	In	Out	In

The following table shows the jumper settings required for currently popular devices.

Device	J1 1–2	J1 3–4	J1 5–6	J1 7–8	J1 9–10	J1 11–12	J1 13–14	J1 15–16	J1 17–18	Comments
8K x 8	Out	Out	In	Out	Out	Out	In	Out	Out	Battery backup
8K x 8	Out	Out	In	Out	Out	In	Out	Out	Out	No battery backup
32K x 8	In	In	Out	Out	Out	Out	In	Out	Out	Battery backup
32K x 8	In	In	Out	Out	Out	In	Out	Out	Out	No battery backup
128K x 8	In	In	Out	Out	Out	In	Out	Out	In	Battery backup
128K x 8	In	In	Out	Out	Out	In	Out	In	Out	No battery backup
512K x 8	In	In	Out	In	In	Out	Out	Out	In	Battery backup
512K x 8	In	In	In	In	In	Out	Out	In	Out	No battery backup
MK48T08	Out	Out	Out	Out	Out	In	Out	Out	Out	Timekeeper RAM
DS1216C	Out	Out	In	Out	Out	In	Out	Out	Out	Smartwatch/RAM 64/256K
DS1216D	In	In	Out	Out	Out	In	Out	In	Out	Smartwatch/RAM 256k/1M

Chip selection for the EPROM and SRAM devices comes from the MC68341(using CS0 for EPROM) and CS1 (for SRAM). DSACK generation for these devices is generated internally by the CPU to provide a 16 bit interface to both RAM and EPROM.

Analog video is provided on the SCART connector in RGB and Y/C formats. This connector also provides composite video or composite sync (jumper selectable) and analog audio signals. The mono audio output will be provided as a jumper option on the SCART connector. For regions where SCART is not a standard, a conversion cable is available to convert SCART to BNC and phono connectors. Three jumper options are available for SCART signals.

Jumper	Function	
J5	1–2	Composite video on SCART pin 19 (Default setting)
	3–4	Composite sync on SCART pin 19
J6	1–2	Audio right signal on SCART pin 1 (Default setting)
	3–4	Mono audio signal on SCART pin 1 (Provided as a convenience)
J7	1–2	Video red output on SCART pin 15 (Default setting)
	3–4	Super VHS C output on SCART pin 15

The headphone output is buffered in U8 and U9 to drive low impedance headphones.

Individual 5 V supplies for the analog audio and analog video sections of this module are produced through ferrite bead and capacitor networks to provide isolation from the noisy 5 V logic supply. Separate analog audio and video ground plane areas are isolated from the logic ground plane through ferrite beads. The PCB layout for the board has been carefully designed to maintain this isolation. Negative 5 V analog supplies (separate for audio and video) are generated from the –12 V supply using regulators U10 and U11.

EXPANSION MODULE

To allow expansion of the design to incorporate additional functionality (e.g. T1 interface for video–on–demand), the full set of the CPU signals are brought to expansion connectors to allow the addition of a "mezzanine" expansion card. The signals and the connectors are defined later. These signals are unbuffered and the design of any expansion card should take this into account.

Audio and video signals necessary to allow digital mixing (i.e. RGB 8:8:8 video and I^2S audio) from an alternative MPEG audio/video decoder on an expansion card (e.g. MPEG2) are also provided on the expansion connectors. it is possible for any of the functionality on the board to be replaced by the equivalent function on an expansion card, or for a bus master on the expansion connectors to take control of the board.

The serial interface signals from IKAT are also brought to these connectors, as are the MC68341's SPI interface signals.

These expansion connectors will also allow the connection of a logic analyser or a bus analyser for hardware and software debugging.

This module includes the JTAG test connector for the board. Jumper J27 allows an expansion card to be included in the scan path if desired.

J27	Function
1–2	Include expasion card in JTAG scan path
3–4	Exclude expansion card from JTAG scan path (default setting)

Both the JTAG connector and the expansion connectors can control reset for the system.

CONNECTOR MODULE

This provides power input connectors for 5 V, +/– 12 V and GND. Two connectors are supplied – AMP Mate–N–LoK style and also a connector suitable for the PSU built into IBM PC compatible desktop cases.

This module also provides the RS232 buffering and connectors for the MC68341's serial I/O ports. Board connectors are RJ11phone type – an adapter is available to convert this to 9 pin D type. A jumper option will connect 5 V power instead of the RTS signal to each connector, and 5 V power will also be connected to the DTR pin of each connector. This allows the use of a Microsoft compatible mouse on one or both ports.

J11	Function	Comments
1–2	Connect 5 V to serial port 1 RTS	Default
3–4	RTS on serial port 1	
5–6	Connect 5 V to serial port2 RTS	Default
7–8	RTS on serial port 2	

Mini DIN connectors are also provided to accept the commercial Philips CD–i pointing devices. These are connected in parallel with the RS232 connectors – both should not be in use at the same time. Jumper J25 does not affect the Mini DIN connectors.

LED D4 provides a power on indicator. An external LED may be connected via J12.

JTAG INTERFACE

The MC68341, MCD212 VDSC, IMPEG and CIAP devices all have a JTAG boundary scan interface and these are interconnected and brought to a header connector to provide a JTAG interface to the board. Figure 2 shows the JTAG scan path.

The JTAG TMS and TCK signals from the test connector are connected to each of the JTAG chips, while TDO and TDI are daisy chained together to form the scan path.

A jumper option allows the expansion interface to be included in the JTAG scan path (refer to the Expansion Module description).

The EXTRST pin on the JTAG test connector can be used to force a board reset – this must be driven by an open collector driver.

MEMORY MAP

The system memory map is shown in Figure 3.

Each of the CD–i player and MPEG functions has been allocated one of the MC68341's programmable chip selects. CS7 has been allocated to cover all of those features which can be considered as extensions to the CD–i / MPEG architecture of the design i.e system DRAM, SCSI, and the expansion interface. CS7 is active for the whole of the address range #01000000 – 01FFFFFF. Due to the 24 bit address bus used, expansion modules that use this address range should use CS7 active as an enabling term in their address decoding logic. Note that CS7 is programmed for 68300 mode bus cycles.

Expansion modules must fully decode their address range to prevent any possible contention with the SCSI and DRAM modules on the main board.

There is a 2 Mbyte EPROM capacity on the main board, with a further 2 Mbyte 'slot' available (at 002000000 – 003FFFFF). Expansion cards may use this preserve memory space in the expansion area. Again due to the 24 bit address bus, if an expansion card uses this addess space, the address bus must be fully decoded using CS7 inactive as an enabling term.

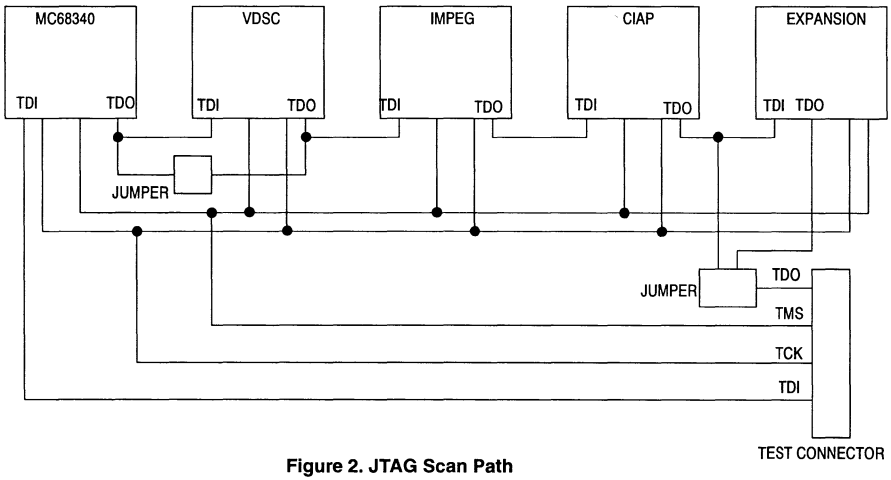


Figure 2. JTAG Scan Path

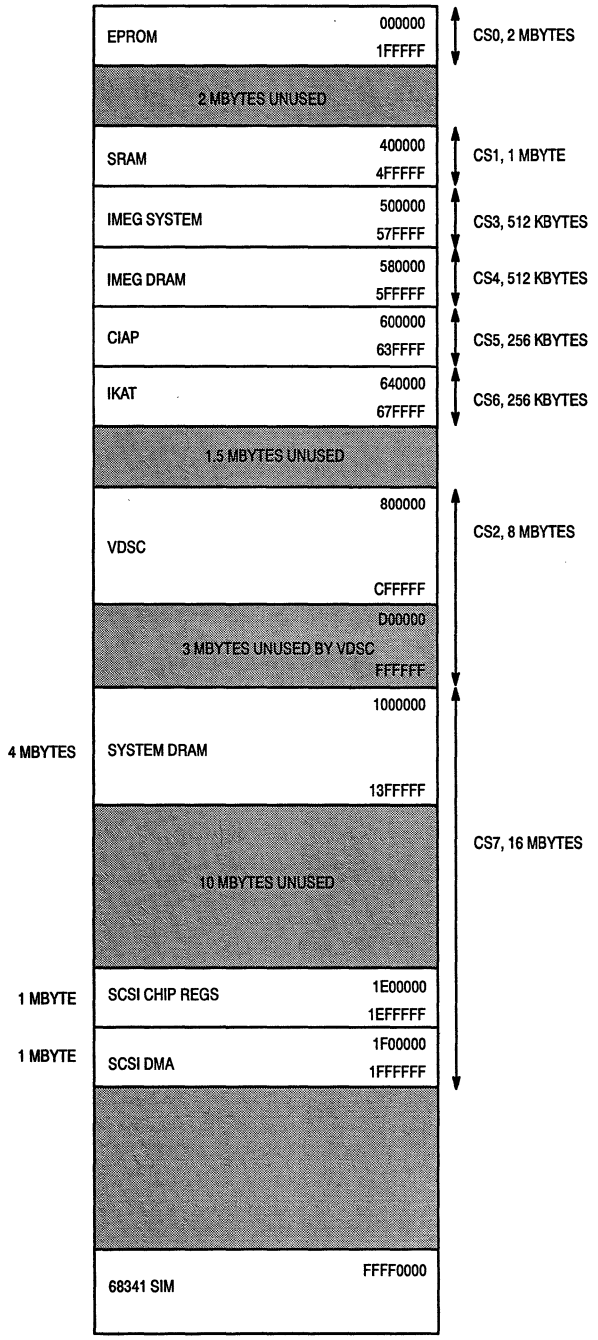


Figure 3. Memory Map

Module		Allocated Address Space	Comments
EPROM		00000000 – 001FFFFF	
SRAM		00400000 – 004FFFFF	8K / 32K / 128K used
IMPEG	System Mode	00500000 – 0057FFFF	00500000 – 00500FFF used
	Transparent Mode	00580000 – 005FFFFF	
CIAP		00600000 – 0063FFFF	00600000 – 006025FF used
IKAT		00640000 – 0067FFFF	00640000 – 0064001F used
VDSC	DRAM (4 Mbytes)	00800000 – 009FFFFF	Video A (2 Mbytes)
		00A00000 – 00BFFFFF	Video B (2 Mbytes)
	System ROM	00C00000 – 00CFFBFF	Not used
	Internal Registers	00CFFFE0 – 00CFFFEF	Channel 2
		00CFFFF0 – 00CFFFFF	Channel 1
SYSTEM DRAM		01000000 – 013FFFFF	
SCSI	Chip Registers	01E00000 – 01EFFFFF	01E00000 – 01E0001F used
	DMA address space	01F00000 – 01FFFFFF	
68341	SIM	FFFF0000 – FFFF00CF	
	TIMER	FFFF0600 – FFFF063F	
	SERIAL	FFFF0700 – FFFF0722	
	DMA	FFFF0780 – FFFF07BF	
	QSPM	FFFF0800 – FFFF094F	

EXTERNAL CONNECTORS

This section details the board connectors.

SYSTEM EXPANSION INTERFACE

The connectors are 96 way DIN 41612 Eurocard style. Signals are TTL level.

CONNECTOR P16					
Pin	Signal	Pin	Signal	Pin	Signal
1A	5 V	1B	GND	C1	TOUT
2A	5 V	2B	GND	C2	RESETN
3A	5 V	3B	GND	C3	
4A	GND	4B	GND	C4	GND
5A	D0	5B	IRQ1n	C5	
6A	D1	6B	IRQ2n	C6	CS0n
7A	D2	7B	IRQ3n	C7	CS1n
8A	D3	8B	IRQ4n	C8	CS2n
9A	D4	9B	IRQ5n	C9	CS3n
10A	D5	10B	IRQ6n	C10	CS4n
11A	D6	11B	IACK1n	C11	CS5n
12A	D7	12B	IACK2n	C12	CS6n
13A	D8	13B	IACK3n	C13	EXPCSn
14A	D9	14B	IACK4n	C14	
15A	D10	15B	IACK5n	C15	
16A	D11	16B	IACK6n	C16	
17A	D12	17B	RESETn	C17	BRN
18A	D13	18B	BERRn	C18	BGN
19A	D14	19B	HALTn	C19	BGACKN
20A	D15	20B	AS68Kn	C20	
21A	UDSn	21B	EXPRST	C21	DTCn
22A	LDSn	22B	IKAT RX1	C22	DREQ1n
23A	SIZ0	23B	IKAT TX1	C23	DREQ2n
24A	SIZ1	24B	IKAT RX2	C24	RDY1n
25A	ASn	25B	IKAT TX2	C25	RDY2n
26A	DSn	26B	IKAT PE4	C26	DONE1n
27A	RW	27B	IKAT PE5	C27	DONE2n
28A	GND	28B	IKAT PE6	C28	DACK1n
29A	CLK	29B	IKAT PE7	C29	DACK2n
30A	GND	30B	GND	C30	GND
31A	+ 12 V	31B	– 12 V	C31	
32A	+ 12 V	32B	– 12 V	C32	

CONNECTOR P17					
Pin	Signal	Pin	Signal	Pin	Signal
1A	5 V	1B	GND	C1	RED0
2A	5 V	2B	GND	C2	RED1
3A	5 V	3B	GND	C3	RED2
4A		4B	NETCLK	C4	RED3
5A	GREEN0	5B		C5	RED4
6A	GREEN1	6B	BLUE0	C6	RED5
7A	GREEN2	7B	BLUE1	C7	RED6
8A	GREEN3	8B	BLUE2	C8	RED7
9A	GREEN4	9B	BLUE3	C9	
10A	GREEN5	10B	BLUE4	C10	VSDn
11A	GREEN6	11B	BLUE5	C11	VSAn
12A	GREEN7	12B	BLUE6	C12	CSYNCn
13A	A8	13B	BLUE7	C13	HSYNCn
14A	A9	14B	A0	C14	VSYNCn
15A	A10	15B	A1	C15	BLANKn
16A	A11	16B	A2	C16	
17A	A12	17B	A3	C17	XT2n
18A	A13	18B	A4	C18	
19A	A14	19B	A5	C19	XT4
20A	A15	20B	A6	C20	
21A	A16	21B	A7	C21	XT2
22A	A17	22B	DSACK0n	C22	
23A	A18	23B	DSACK1n	C23	
24A	A19	24B		C24	PCS0
25A	A20	25B	EXP_TDO	C25	PCS1
26A	A21	26B	EXP_TDI	C26	MISO
27A	A22	27B	EXP_TCK	C27	MOSI
28A	A23	28B	EXP_TMS	C28	QSCLK
29A		29B	GND	C29	GND
30A		30B	GND	C30	I^2S Word Select
31A	GND	31B	GND	C31	GND
32A	I^2S Clock	32B	GND	C32	I^2S Data

CD INTERFACE P15

The connector is a 25 way D–type socket. Signals are TTL level.

Pin	Signal	Function	Pin	Signal
1	CLK33	33.8688 MHz clock to CD Drive	14	GND
2	5 V		15	GND
3	5 V		16	GND
4	12 V		17	GND
5	12 V		18	GND
6	DSARST	DSA Reset	19	GND
7	DSADATA	DSA Data	20	GND
8	DSAACK	DSA Acknowledge	21	GND
9	DSASTB	DSA Strobe	22	GND
10	SUBCODE	CD Drive sub–code data	23	GND
11	CLIN	I^2S Clock	24	GND
12	WSIN	I^2S Word Select	25	GND
13	DAIN	I^2S Data		

ANALOG VIDEO INTERFACE – SVHS P2

Pin	Signal	Description
1	GND	Video ground
2	GND	Video ground
3	Y	Luminance
4	C	Chrominance

ANALOG AUDIO OUTPUT INTERFACE – HEADPHONE JACK P3

Pin	Function
Tip	Audio Left
Middle	Audio Right
Shield	Audio Ground

ANALOG AUDIO / VIDEO INTERFACES – SCART P1

Pin	Description
1	Audio output right / mono Jumper selectable
2	no connection
3	Audio output left
4	Audio return
5	Blue video return
6	no connection
7	Blue video output
8	Slow switching output Connected to 12 V through 680 ohms
9	Green video return
10	no connection
11	Green video output
12	no connection
13	Red video return
14	no connection
15	Red video output / SVHS Chrominance Jumper selectable
16	Fast switching output Connected to 5V through 100 ohms
17	Composite video / sync return
18	Switching return
19	Composite video / sync output Jumper selectable
20	SVHS Luminance
21	Common return

POWER CONNECTOR P12

The connector is a AMP Mate–N–Lok style.

Pin	Description
1	GND
2	GND
3	– 12 V
4	+ 12 V
5	5 V
6	5 V

POWER CONNECTORS P13,14

These connectors allow the use of an IBM PC compatible power supply.

P 13	
Pin	**Description**
1	GND
2	GND
3	nc
4	5 V
5	5 V
6	5 V

P 14	
Pin	**Description**
1	nc
2	5 V
3	+ 12 V
4	– 12 V
5	GND
6	GND

SCSI INTERFACE CONNECTOR P7

Connector type is 50 way IDC.

Pin	Description	Pin	Description
1	GND	2	DB0
3	GND	4	DB1
5	GND	6	DB2
7	GND	8	DB3
9	GND	10	DB4
11	GND	12	DB5
13	GND	14	DB6
15	GND	16	DB7
17	GND	18	Parity
19	GND	20	GND
21	GND	22	GND
23	GND	24	GND
25		26	Terminator Power
27	GND	28	GND
29	GND	30	GND
31	GND	32	ATN
33	GND	34	GND
35	GND	36	BSY
37	GND	38	ACK
39	GND	40	RST
41	GND	42	MSG
43	GND	44	SEL
45	GND	46	CD
47	GND	48	REQ
49	GND	50	IO

SPI INTERFACE J14

The connector is a 10 pin header. Signals are TTL level.

Pin	Signal	Description
1	MISO	Master – In Slave – Out
2	GND	
3	MOSI	Master – Out Slave – In
4	GND	
5	QSCLK	Serial Clock
6	GND	
7	PCS1	Peripheral Chip Select
8	5 V	
9	PCS0	Peripheral Chip Select
10	5 V	

BACKGROUND DEBUG MODE INTERFACE J19

The connector is a 10 pin header. Signals are TTL level.

1	GND	
2	BKPT	Signal a hardware breakpoint
3	GND	
4	FREEZE	CPU has enetred background mode
5	CPURST	Reset
6	IFETCH	Instruction word prefetch
7	5 V	
8	IPIPE	Used to track instruction pipeline
9	nc	
10	nc	

RS232 CONNECTORS P10, P11

The connector is a 6 pin RJ11. An adapter is available to convert this to 9 pin D Type. Signals are RS232 level.

Pin	Signal	Description
1	5 V	
2	GND	
3	CTS	Clear to send
4	TxD	Transmit Data
5	RTS / 5 V	Request to Send / Power. Jumper selectable
6	RxD	Receive Data

CD–i POINTER DEVICE CONNECTORS P8,P9

The connector is 8 pin Mini DIN. Signals are RS232 level.

Pin	Signal	Description
1	nc	
2	RxD	Data from pointer
3	ncl	
4	nc	
5	GND	
6	nc	
7	RTS	Request to send
8	5 V	

JTAG TEST CONNECTOR J28

The connector is a 14 pin header. Signals are TTL level.

1	TDO	JTAG test data output.
2	GND	
3	TDI	JTAG test data input.
4	GND	
5	TMS	JTAG test mode select .input.
6	GND	
7	TCK	JTAG test clock input.
8	GND	
9	EXTRST	External reset input. Used to force a hardware reset of the board.
10	GND	
11	5 V	
12	GND	
13	nc	
14	GND	

```
TITLE SRAYSCSI
PATTERN SCSI control for Stingray+
REVISION 0.0
AUTHOR Craig McAdam
COMPANY MOTOROLA, EAST KILBRIDE
DATE 17/02/1994
CHIP ICxx PAL22V10

;Rev 0.0 17/02/94 Ta Da !!

CPUCLK      ;PIN 1 - 68341 clock output
RW      ; 2 - 68341 RW
/CSN    ; 3 - Stingray+ expansion decode ( from 68341 CS7 )
/DSN    ; 4 - 68341 DS
/ASN    ; 5 - 68341 AS
A23     ; 6 - 68341 address lines
A22     ; 7 -
A21     ; 8 -
A20     ; 9 -
NCR_DREQ        ; 10 - DMA req from 53C94 - active high
NC      ; 11 -
GND     ; 12
/RSTN       ; 13 - Reset in
NCR_RST         ; 14 - Active high reset to 53C94
/DTACKN         ; 15 - Becomes DSACK1 to 68341
DTACKNEN        ; 16 - O/P enable term for DTACKN
/NCR_CSN        ; 17 - Chip select to 53C94 - only for CPU accesses
/NCR_RDN        ; 18 - RD for 53C94 - only for CPU accesses
/NCR_WRN        ; 19 - WR for 53C94 - for CPU and DMA accesses
/NCR_DACKN      ; 20 - DMA ack to 53C94
/DREQN      ; 21 - DMA req to 68341
/W0     ; 22 - 1st wait state indicator
DREQNEN         ; 23 - O/P enable term for DREQN
VCC     ; 24
PHANTOM         ; 25 - Required for PALASM2 to control macrocell set and reset


; Decode for 53C94 regs
STRING CHIP_DECODE          ' (CSN * A23 * A22 * A21 * /A20) '
; Decode for SCSI DMA
STRING DMA_DECODE           ' (CSN * A23 * A22 * A21 * A20) '
; Decode both DMA and 53C94 registers
STRING ALL_DECODE           ' (CSN * A23 * A22 * A21 ) '


EQUATIONS

NCR_CSN         = CHIP_DECODE * CPUCLK          ;Active in S2
        + NCR_RDN           ;Maintain after end of NCR_RDN ...
        + NCR_WRN * CHIP_DECODE ; ... or end of NCR_WRN

NCR_WRN         = CHIP_DECODE * NCR_CSN * /RW * ASN
;CPU access - active
                        ;after NCR_CSN
        + DMA_DECODE * NCR_DACKN * /RW * ASN                    ;DMA access

NCR_RDN         = CHIP_DECODE * NCR_CSN * RW                ;Active after NCR_CSN
        + NCR_RDN * CHIP_DECODE

NCR_DACKN       = DMA_DECODE * CPUCLK               ;Starts in S2
        + NCR_DACKN * DMA_DECODE
        + NCR_DACKN * /RW * NCR_WRN             ;Sustain for DMA writes

DREQN       = NCR_DREQ * /ALL_DECODE                ;Force cycle steal mode if
necessary
```

```
DREQNEN         = NCR_DREQ * /ALL_DECODE

W0      := NCR_CSN * /RSTN                ;Starts in SW1
        + NCR_DACKN * /RSTN

DTACKN       = W0 * /CPUCLK * ALL_DECODE * /RSTN
        + DTACKN * ALL_DECODE

DTACKNEN        = ALL_DECODE

NCR_RST         = RSTN

;Output control

NCR_CSN.TRST = VCC
NCR_RDN.TRST = VCC
NCR_WRN.TRST = VCC
NCR_DACKN.TRST = VCC
DREQN.TRST = DREQNEN
DTACKN.TRST = DTACKNEN
W0.TRST = VCC
NCR_RST.TRST = VCC

PHANTOM.SETF = GND ; Disable o/p register set function
PHANTOM.RSTF = GND
```

```
TITLE DRAMA
PATTERN Part 1 of Stingray+ DRAM controller
REVISION 0.0
AUTHOR Craig McAdam
COMPANY MOTOROLA, EAST KILBRIDE
DATE 17/02/1994
CHIP ICxx PAL22V10

;Rev 0.0 17/02/94 Fwoosh !! It exists.

;Currently decoded to be the 1st 4 Mbytes on a 16 Mbyte boundary.

INVCLK      ;PIN 1 - Inverted 68341 clock output
CLK     ; 2 - 68341 CLKOUT
/CSN    ; 3 - Stingray+ expansion decode ( from 68341 CS7 )
/DSN    ; 4 - 68341 DS
RFQ     ; 5 - Refresh request from DRAMB PAL
/RESETN       ; 6 - Reset
RW      ; 7 -
A0      ; 8 -
A20     ; 9 -
A21     ; 10 -
A22     ; 11 -
GND     ; 12
A23     ; 13 -
/RAS1N      ; 14 - RAS for lower bank of DRAM
/RAS2N      ; 15 - RAS for upper bank of DRAM
/CASLN      ; 16 - CAS for lower byte
/CASUN      ; 17 - CAS for upper byte
S0      ; 18 - State machine bits
S1      ; 19 -
S2      ; 20 -
S3      ; 21 -
NC      ; 22 -
SIZ0    ; 23 -
VCC     ; 24
PHANTOM       ; 25 - Required for PALASM2 to control macrocell set and reset

;Valid address decode
STRING VALID '/A23 * /A22 '

;Bank select
STRING UBANK ' A21 '
STRING LBANK ' /A21 '

;These strings correspond to the DRAM controller state machine
STRING SM0 '/S3 * /S2 * /S1 * /S0'                    ;0000
STRING SM1 '/S3 * S2 * /S1 * /S0'                     ;0100
STRING SM2 '/S3 * S2 * /S1 * S0'                      ;0101
STRING SM3 '/S3 * /S2 * /S1 * S0'                     ;0001
STRING SM4 '/S3 * /S2 * S1 * S0'                      ;0011
STRING SM5 '/S3 * S2 * S1 * S0'                       ;0111
STRING SM6 '/S3 * S2 * S1 * /S0'                      ;0110
STRING SM7 '/S3 * /S2 * S1 * /S0'                     ;0010
STRING SM8 ' S3 * /S2 * /S1 * /S0'                    ;1000
STRING SM9 ' S3 * S2 * /S1 * /S0'                     ;1100
STRING SM10 ' S3 * S2 * /S1 * S0'                     ;1101
STRING SM11 ' S3 * /S2 * /S1 * S0'                    ;1001
STRING SM12 ' S3 * /S2 * S1 * S0'                     ;1011
STRING SM13 ' S3 * S2 * S1 * S0'                      ;1111
STRING SM14 ' S3 * S2 * S1 * /S0'                     ;1110
STRING SM15 ' S3 * /S2 * S1 * /S0'                    ;1010

EQUATIONS

RAS1N       = (
```

```
        (SM0 * CSN * CLK * /RFQ * VALID                ;Start CPU access - lower
bank
        + SM0 * RAS1N
        + SM8
        + SM9 ) * LBANK
        + (SM2 + SM3 )                ;Refresh
        ) * /RESETN

RAS2N        = (
        (SM0 * CSN * CLK * /RFQ * VALID                ;Start CPU access - upper
bank
        + SM0 * RAS2N
        + SM8
        + SM9 ) * UBANK
        + (SM2 + SM3 )                ;Refresh
        ) * /RESETN

CASLN        = (
        ( ( SM9 + (CASLN * DSN * /RFQ) )                      ;RFQ will stay active
until
                        ;SM4
        * ( /SIZ0 + A0 ) )                ;Lower CAS for word or odd
                        ;access
        + SM1                ;Refresh
        + CASLN * SM2 * /CLK
        ) * /RESETN

CASUN        = (
        ( ( SM9 + (CASUN * DSN * /RFQ) )                      ;RFQ will stay active
until
                        ;SM4
        * ( /SIZ0 + /A0 ) )                ;Upper CAS for word or even
                        ;access
        + SM1                ;Refresh
        + CASUN * SM2 * /CLK
        ) * /RESETN

;Output control

RAS1N.TRST = VCC
RAS2N.TRST = VCC
CASUN.TRST = VCC
CASLN.TRST = VCC
S0.TRST = VCC
S1.TRST = VCC
S2.TRST = VCC
S3.TRST = VCC
SIZ0.TRST = GND

PHANTOM.SETF = GND ; Disable o/p register set function
PHANTOM.RSTF = GND

;DRAM Controller state machine

STATE

MOORE_MACHINE

;State assignments
STATE0 = /S3 * /S2 * /S1 * /S0                        ;0000
STATE1 = /S3 * S2 * /S1 * /S0                         ;0100
STATE2 = /S3 * S2 * /S1 * S0                       ;0101
STATE3 = /S3 * /S2 * /S1 * S0                         ;0001
STATE4 = /S3 * /S2 * S1 * S0                       ;0011
STATE5 = /S3 * S2 * S1 * S0                     ;0111
STATE6 = /S3 * S2 * S1 * /S0                       ;0110
```

```
STATE7 = /S3 * /S2 * S1 * /S0                          ;0010
STATE8 = S3 * /S2 * /S1 * /S0                          ;1000
STATE9 = S3 * S2 * /S1 * /S0                        ;1100
STATE10 = S3 * S2 * /S1 * S0                        ;1101
STATE11 = S3 * /S2 * /S1 * S0                          ;1001
STATE12 = S3 * /S2 * S1 * S0                        ;1011
STATE13 = S3 * S2 * S1 * S0                      ;1111
STATE14 = S3 * S2 * S1 * /S0                        ;1110
STATE15 = S3 * /S2 * S1 * /S0                          ;1010

;State machine sequence

STATE0      := RST ->    STATE0
       + REFRESH ->     STATE1          ;Start a refresh cycle
       + ACTIVE ->       STATE8         ;Start an access cycle
       +->      STATE0    ;Nothing happening, so hang around

STATE1      := RST ->    STATE0
       +-       STATE2

STATE2      := RST ->    STATE0
       +->      STATE3

STATE3      := RST ->    STATE0
       +->      STATE4

STATE4      := RST ->    STATE0
       +->      STATE5

STATE5      := RST ->    STATE0
       + REFRESH ->     STATE1          ;Haven't finished a refresh burst yet
       +->      STATE0

STATE8      := RST ->    STATE0
       + PROCEED ->     STATE9          ;For a write only proceed if DS is active
       +->      STATE8    ;( .... to suit DMA requirements )

STATE9      := RST ->    STATE0
       +->      STATE10

STATE10        := RST ->     STATE0
       + FINISH ->       STATE0          ;For a read only finish if DS is inactive
       +->      STATE10   ;( .... to suit DMA requirements )

STATE6      := VCC ->    STATE0          ;Unused states

STATE7      := VCC ->    STATE0

STATE11        := VCC ->     STATE0

STATE12        := VCC ->     STATE0

STATE13        := VCC ->     STATE0

STATE14        := VCC ->     STATE0

STATE15        := VCC ->     STATE0

CONDITIONS

RST = RESETN
REFRESH = RFQ * /RESETN
ACTIVE = ( RAS1N + RAS2N ) * SM0 * /RFQ * /RESETN
PROCEED = ( RW + (DSN * /RW) ) * /RESETN              ;Test condition for a write
cycle
FINISH = ( /RW + (/DSN * RW) ) * /RESETN  ;Test condition for a read cycle
```

```
TITLE DRAMB1
PATTERN Part 2 of Stingray+ DRAM controller
REVISION 0.0
AUTHOR Craig McAdam
COMPANY MOTOROLA, EAST KILBRIDE
DATE 17/02/1994
CHIP ICxx PAL22V10

;Rev 0.0 17/02/94 Huah ! Where did that come from ?

INVCLK      ;PIN 1 - Inverted 68341 clock output
CLK     ; 2 - 68341 CLKOUT
/RESETN       ; 3 - Reset
S0      ; 4 - State machine bits from DRAMA PAL
S1      ; 5 -
S2      ; 6 -
S3      ; 7 -
RW      ; 8 - 68341 read / write
/DSN    ; 9 -
NC      ; 10 -
NC      ; 11 -
GND     ; 12
RFSH    ; 13 - Refresh request from 68341 timer
/DTACKN       ; 14 -
DTACKEN       ; 15 - Enable term for DTACKN
ADDSEL      ; 16 - Address multiplexer control - '1' then '0'
GN      ; 17 - DRAM output enable
WRN     ; 18 - DRAM WR
RFQ     ; 19 - Active throughout refresh to control burst refresh
T0      ; 20 - 3 bits for refresh cycle counter if needed
T1      ; 21 -
T2      ; 22 -
REFREQ      ; 23 - Latched refresh request
VCC     ; 24
PHANTOM       ; 25 - Required for PALASM2 to control macrocell set and reset


;These strings correspond to the DRAM controller state machine in DRAMA
STRING SM0 '/S3 * /S2 * /S1 * /S0'                    ;0000
STRING SM1 '/S3 * S2 * /S1 * /S0'                     ;0100
STRING SM2 '/S3 * S2 * /S1 * S0'                      ;0101
STRING SM3 '/S3 * /S2 * /S1 * S0'                     ;0001
STRING SM4 '/S3 * /S2 * S1 * S0'                      ;0011
STRING SM5 '/S3 * S2 * S1 * S0'                       ;0111
STRING SM6 '/S3 * S2 * S1 * /S0'                      ;0110
STRING SM7 '/S3 * /S2 * S1 * /S0'                     ;0010
STRING SM8 ' S3 * /S2 * /S1 * /S0'                    ;1000
STRING SM9 ' S3 * S2 * /S1 * /S0'                     ;1100
STRING SM10 ' S3 * S2 * /S1 * S0'                     ;1101
STRING SM11 ' S3 * /S2 * /S1 * S0'                    ;1001
STRING SM12 ' S3 * /S2 * S1 * S0'                     ;1011
STRING SM13 ' S3 * S2 * S1 * S0'                      ;1111
STRING SM14 ' S3 * S2 * S1 * /S0'                     ;1110
STRING SM15 ' S3 * /S2 * S1 * /S0'                    ;1010


EQUATIONS

ADDSEL      = SM8
       + SM8 * ADDSEL
       + SM9

WRN     = /RW
       * ( SM8 + SM9 )
       * /RESETN
```

```
GN      = RW
        * ( SM8 + SM9 + SM10 )
        * /RESETN

DTACKN      = SM8 * DSN
        + SM9
        + SM10

DTACKEN       = ( SM8
        + SM9
        + SM10 * DSN )
        * /RESETN

REFREQ      = RFSH * INVCLK * /CLK                  ;Set refresh request latch
        + REFREQ * /(/S3 * /S2 * S1 * S0)                   ;Clear latch at end of
refresh
        * /RESETN

RFQ     = REFREQ          ;Goes active with REFREQ to suit DRAMA PAL
        * /RESETN

;Output control

RFQ.TRST = VCC
DTACKEN.TRST = VCC
DTACKN.TRST = DTACKEN
ADDSEL.TRST = VCC
GN.TRST = VCC
WRN.TRST = VCC
REFREQ.TRST = VCC

PHANTOM.SETF = GND ;Disable o/p register set function
PHANTOM.RSTF = GND
```

```
TITLE       BUGFIX
PATTERN       Bug fixes for Stingray
REVISION       1.0
AUTHOR        Craig McAdam
COMPANY       MOTOROLA, EAST KILBRIDE
DATE        25/08/1994
CHIP        IC21    PAL22V10

;Rev 0.0 25/08/94

;CIAP doesn't tri-state its DREQ o/p, so we now need to gate this
;with the SCSI DREQ instead of tying them together.
;
;Since we will program the DMA controller to use RDY from the
;DMA devices during single address transfers, we need to drive
;RDY2 active during dual address SCSI DMA cycles. CIAP will
;drive RDY properly for its own DMA cycles.

;We will restrict SCSI and CIAP to DMA channel 2 for the
;time being.

/SCSIDREQ      ;1 - DMA request from SCSI PAL
/SCSIDACK      ;2 - DMA ack from SCSI PAL
/CIAPDREQ      ;3 - DMA request from CIAP
NC      ;4 -
NC      ;5 -
NC      ;6 -
NC      ;7 -
NC      ;8 -
NC      ;9 -
NC      ;10 -
NC      ;11 -
GND     ;12 -
NC      ;13 -
/DREQ341       ;14 - DMA request to 341 from either CIAP or SCSI
/RDY341      ;15 - RDY to 341 for SCSI DMA
DREQEN       ;16 - Output enable term for DMA req to 340
RDYEN   ;17 - Output enable term for RDY to 340
NC      ;18 -
NC      ;19 -
NC      ;20 -
NC      ;21 -
NC      ;22 -
NC      ;23 -
VCC     ;24 -
PHANTOM      ;25 - Required for PALASM2 to control macrocell set and reset

EQUATIONS

DREQ341      = SCSIDREQ
       + CIAPDREQ

DREQEN       = SCSIDREQ
       + CIAPDREQ

RDY341       = SCSIDACK

RDYEN   = SCSIDACK

;Output control

DREQEN.TRST      = VCC
DREQ341.TRST       = DREQEN
RDYEN.TRST       = VCC
RDY341.TRST      = RDYEN
```

BOARD LAYOUT

For reference, Figure 4 shows the layout of the connectors, jumpers, switches, and LED's on the board. Note that the jumpers are not all aligned identically.

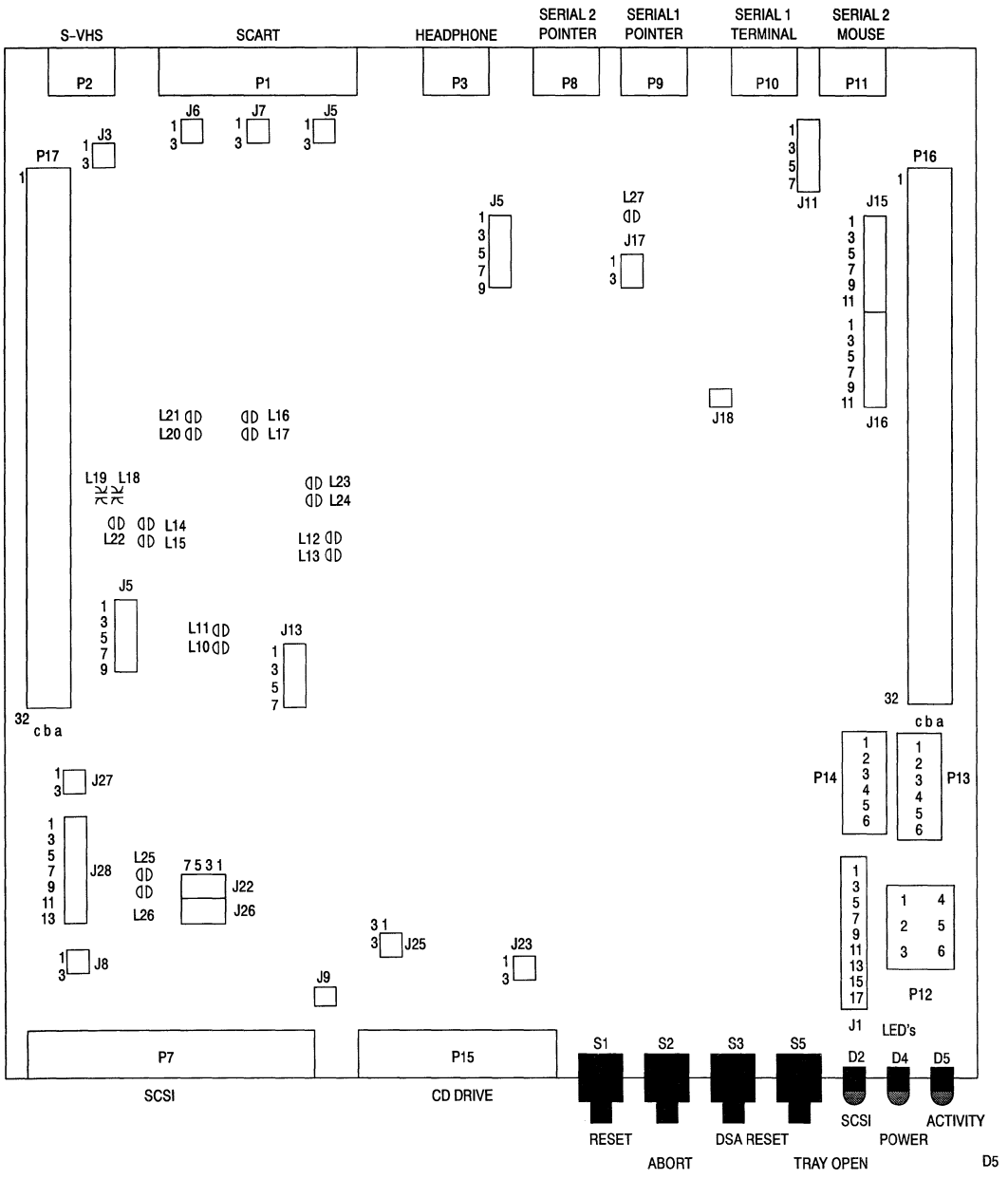


Figure 4. Board Layout

PHYSICAL AND ELECTRICAL SPECIFICATION

Board Size – Double Extended Eurocard (220 x 233 mm)
Power Consumption – TBD

REFERENCE DOCUMENTS

Stingray+ Requirement Specification Ver. 1.0
MC68341 User's Manual MC68341UM/AD.
IEEE Standard 1149.1 – 1990 " The IEEE Standard Test Access Port and Boundary – Scan Architecture ".
Philips IMS Technical Info – Pointing Devices.
MCD210 VDSC Specification.
MCD270 IMPEG Specification.
MCD220 CIAP Specification.
MC68HC05i8 Advance Specification MC68HC05i8/D Rev. 1

Motion Pictures Experts Group (MPEG) ISO 11172a Video Compression, Decompression Standard

Prepared by: Jason Spielman
Motorola, Center for Emerging Computer Technologies

This report has two purposes. It will describe all the steps involved in MPEG and will define the syntax of the standard. This report is not intended to replace the standard but to present the material of the standard in a more readable format and to serve as a quick reference. Not all the detail in the standard is found in this report. Any discrepancies should yield to the standard.

The MPEG standard (ISO 11172) defines a format for compressed digital video, capable of sustaining data rates of 1856 Kbps. This allows 128 Kbps on a telecommunications channel (which has a bandwidth of 1984 Kbps) for audio. The overall source to destination sequence is shown below in figure 1 (encoding/decoding and compression/decompression will be used synonymously throughout this report):

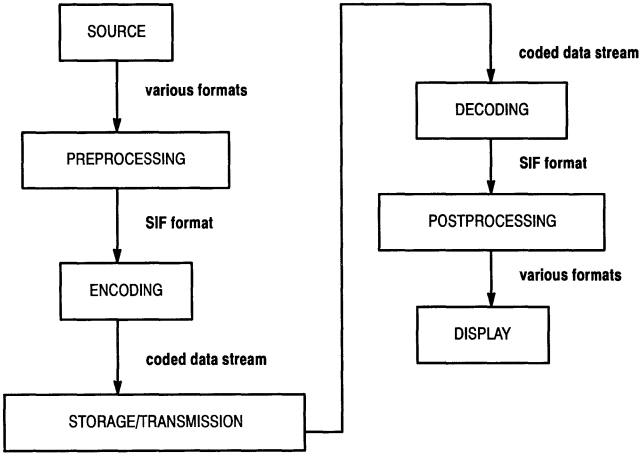


Figure 1. Compression/Decompression Process

Each of the stages will be described in sequence. The MPEG standard does not define the entire process. It simply describes the syntax of the coded data stream and the compression steps used. Consequently, this report will focus on the compression and decompression stages. The standard leaves a lot of flexibility in how the original data will be compressed.

Video Source

Various source mediums exist. CCIR 601 is the international standard for digital television. We will use this as our source video example. CCIR 601 consists of a luminance component, Y, and two chrominance components, Cb and Cr (also referred to as U and V components). The Y component gives a gray scale image; the U and V components give color information. Two options exist for combinations of number of lines, picture rate, and pixel aspect ratios. We will consider 525 lines per frame, 60 Hz picture rate, and a resolution of 720x480 luminance pixels. This resolution and picture rate is too high for the target 1.5 Mbps MPEG data rate so preprocessing is done to this source data.

Preprocessing the Source Data

Preprocessing serves various purposes but usually involves some form of bandwidth reduction. MPEG is defined for non–interlaced formats only, so preprocessing might also include conversion from interlaced to non–interlaced format. Typically the original source is reduced to SIF, Source Input Format. SIF is a general term to describe input that has been constrained to the data rate limitations of the MPEG standard and typically consists of a resolution of 360x240 pixels.

In our example, the picture rate and resolution are too high for the MPEG data rate limitations. We may halve the picture rate to 30Hz (which is typical of other video source media) and halve the resolution to 360x240. One method of halving the video rate is to discard every other field. This may produce aliasing effects (aliasing refers to the effects of a high frequency signal being displayed as a low frequency signal as caused by insufficient sampling). More sophisticated methods are possible but are computationally expensive and are beyond the scope of this report. One may easily halve the horizontal and vertical resolutions by filtering and subsampling. A similar approach may be used for the U and V chrominance components. These steps are not defined in the standard and will not be examined in any further detail here. The end result is a video format with 30 frames per second, and a resolution of 360x240 luminance pixels, 180x120 U chrominance pixels, and 180x120 V chrominance pixels. The MPEG standard does not specifically place restrictions on resolutions, bit rates and picture rates. In fact the standard is flexible enough to cover large ranges in each category. However, the standard defines a 'constrained bit stream' that specifies the minimum functionality of a decoder. This 'constrained bit stream' is summarized below in Table 1. See Appendix A for a description of the bit stream syntax and all its fields.

Table 1. Constrained Bit Stream Parameters

BIT STREAM PARAMETER	CONSTRAINED VALUE
horizontal resolution	768 or less
vertical resolution	576 or less
no. macroblocks per picture	396 or less
no. macroblocks per second	99000 or less
pictures per second	30 or less
bit rate	1.86 Mbps or less
decoder buffer size	376832 bits or less

An MPEG bitstream contains many headers, or information blocks, that define various attributes of the coded video data. Some of these attributes are listed in the table above. We will see more of these later.

Before proceeding, it will be advantageous to describe the hierarchical data structure that MPEG uses.

MPEG Data Hierarchy

It will be beneficial to define two terms, *video pixel* and *component pixel*. A *video pixel* is defined to be a pixel of the original picture. A 2x2 group of video pixels consists of 2x2 luminance *component pixels*, one U–chrominance *component pixel* and one V–chrominance component pixel. Hence SIF format usually consists of 360x240 luminance component pixels, 180x120 U chrominance pixels, and 180x120 V chrominance pixels. Component pixels are described with single–byte data. A *pixel* may refer to a video pixel or a component pixel depending on context.

The fundamental video unit is a *macroblock*. A macroblocks is a group of 16x16 video pixels. Hence it consists of 16x16 luminance pixels, and 2 *blocks* of 8x8 chrominance pixels. A *block* is a term to describe any 8x8 block of component pixels. The 16x16 luminance pixels are divided into four blocks hence a macroblock consists of six 8x8 blocks of component pixels.

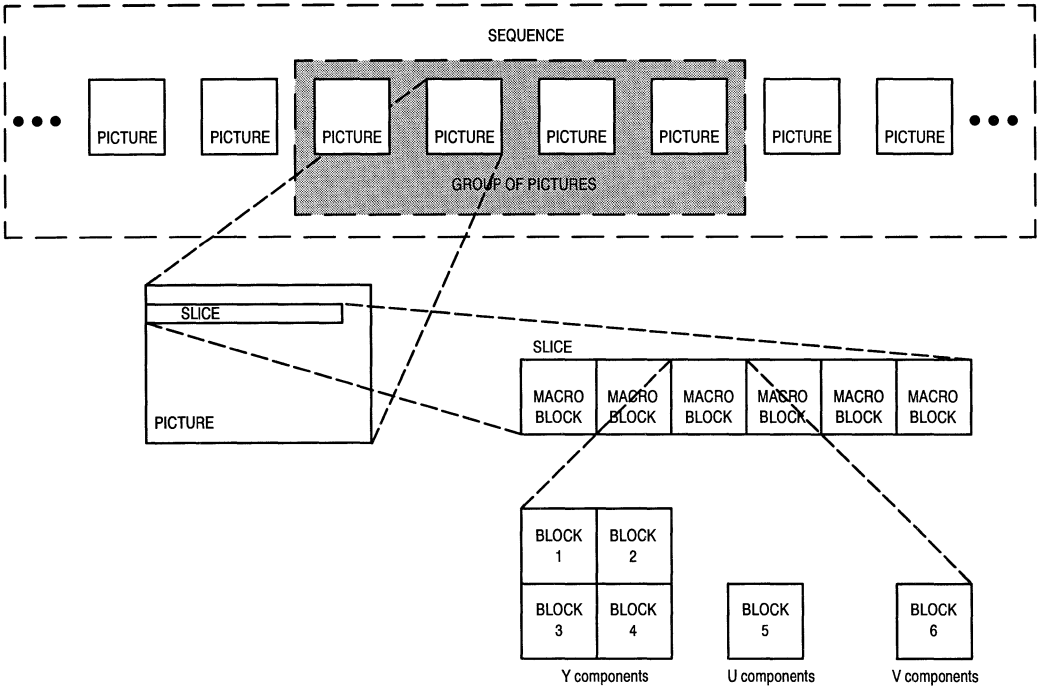


Figure 2. Video Data Heirarchy

Video is coded hierarchically. A *sequence* is any video sequence. A sequence is made up of *groups–of–pictures*. A group–of–pictures is made up of individual *pictures*. Each picture corresponds to a single frame of motion video. A picture is broken into *slices*. Each slice in turn is composed of *macroblocks*. Macroblocks have been discussed above and are composed of six 8x8 blocks of component pixels. Coding of video data occurs on a block by block basis within each macroblock and is coded in the order numbered in figure 2.

Encoding

The actual syntax of the coded bit stream is described in Appendix A. The MPEG standard takes advantage of various different data compression techniques to achieve its goals. Let us examine the various kinds of picture coding that is possible.

Picture Types

Pictures are categorized as intra pictures (i–pictures), predicted pictures (p–pictures), bidirectionally predicted pictures (b–pictures), and DC pictures (d–pictures). The prediction is based upon the temporal correlation between successive frames, i.e. portions of frames may not differ from one another over short periods of time. The encoding and decoding methods differ for each type of picture. The simplest methods are those used for i–pictures, followed by those for p–pictures and then b–pictures. We shall examine the encoding and decoding of each in turn. I–pictures completely describe a single frame without reference to any other frame. P–pictures are predicted based on previous i or p–pictures. The reference is from a earlier i or p–picture to a future p–picture and is therefore called forward prediction. B–pictures are predicted from the closest earlier i or p–picture and the closest later i or p–picture. The reference to a future picture (one that has not yet been displayed) is called backward prediction. While forward prediction is intuitive (predict a future picture based upon a previous picture), backward prediction is not as intuitive. Nevertheless, there are cases where backward prediction is useful. Consider a scene in which a door opens. The current picture may predict what is behind the door based upon a future picture in which the door is already open. All three picture types are illustrated below. The arrows show which pictures are used for prediction.

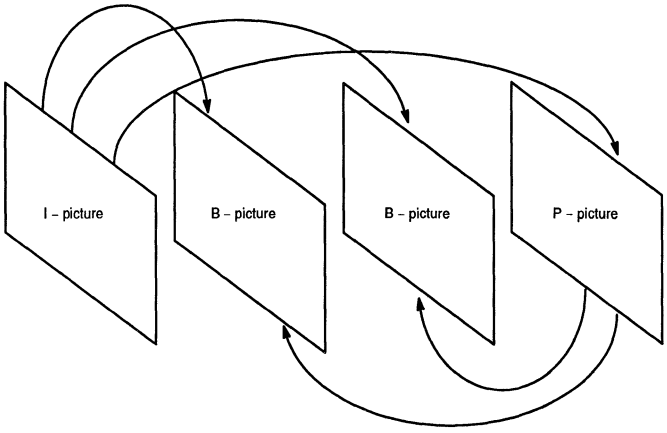


Figure 3. Picture Types

There is a fourth type of picture known as a d–picture. This picture consists of low frequency information and is included for implementation of low–quality fast forward playback.

B–pictures yield the most compression but also incorporate the most error. To eliminate error propagation, b–pictures may never be predicted from other b–pictures. P–pictures yield less error and less compression. I–pictures yield the least compression but the greatest picture quality. These pictures provide random access entry points into a video sequence.

The MPEG standard does not specify any particular distribution that the four types of pictures may take within a sequence. It allows different distributions to provide different degrees of compression and random accessibility. One common distribution is to have i–pictures about every 1/2 second and two b–pictures between successive i or p–pictures. For a 30 frame per second sequence this is illustrated below:

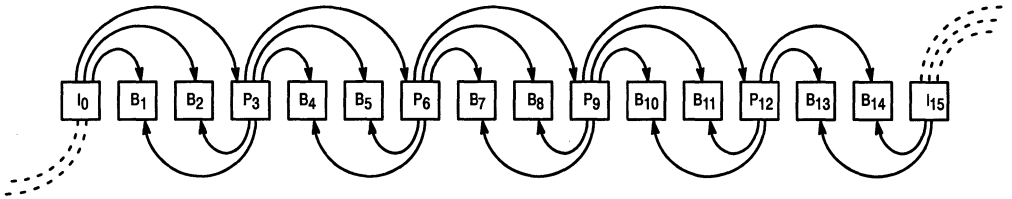


Figure 4. Typical Picture Distribution

The subscripts enumerate the pictures in **display** order. Note that to decode p–pictures the previous i–picture must be available. Similarly to decode b–pictures, the previous and future p, or i–pictures must be available. For example, to decode picture B_1, we need to have already decoded I_0 and P_3. Consequently, the pictures are encoded in dependency order. All pictures used for prediction are coded before the pictures that are predicted from them. For the sequence above we get the following order:

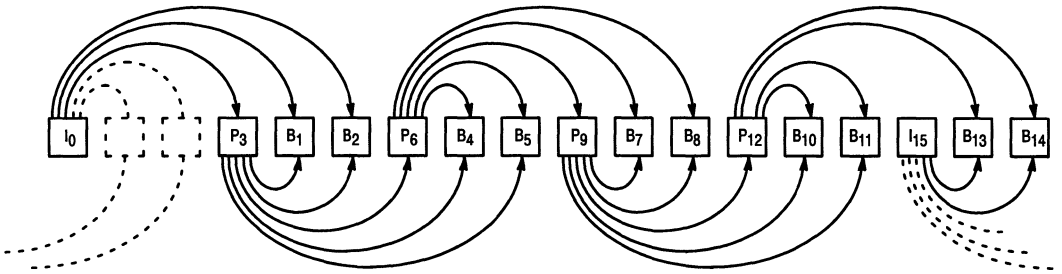
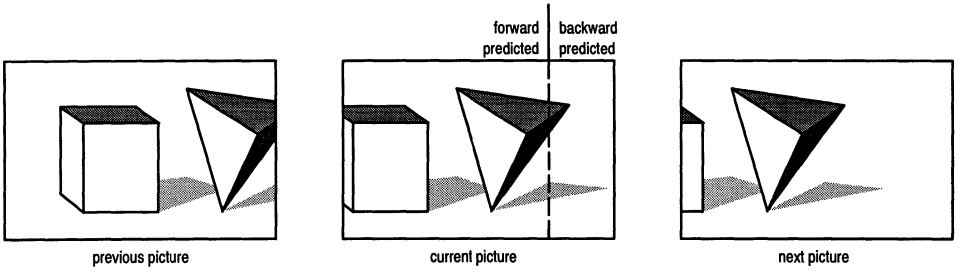


Figure 5. Picture sequence in code order

Note that there are two dotted pictures in figure 5 but not figure 4. These are the two b–pictures that appear (in display order) prior to I_0. If I_0 is the first picture in the sequence then these two are omitted.

Pictures are coded on a macroblock level (and on a block level within that). Parts of a picture may be predicted from other pictures with great accuracy, while others may not. For this reason, macroblocks within a p–picture do not necessarily have to be encoded as predicted from an earlier picture. They may be coded as independent units the same way as in i–pictures. Similarly, macroblocks in b–pictures may be coded the same way as in i–pictures or p–pictures. This tends to allow higher compression rates but complicates the encoding algorithm. Here is a common example. Consider a pan to the right. The macroblocks on the left edge of the current picture may be forward–predicted from the previous picture. That is, the macroblocks may simply be the same image in the previous picture but shifted left a certain number of pixels. Similarly the macroblocks on the right edge of the picture may be backward–predicted from the following picture. That is, the right edge macroblocks cannot be predicted from the previous picture because the image is not present in that picture, but the image is present in later pictures so we may use these later pictures for prediction. This is illustrated below. Hence, some macroblocks in a b–picture may use forward–prediction, while others may use bacward–prediction. This will be discussed in more detail in the description of each picture type.



Encoding I–Pictures

I–pictures are independent units that describe a complete picture without reference to any other pictures. These pictures yield the least data compression. The data compression used is very similar to the JPEG (Joint Pictures Experts Group) algorithm. This is an algorithm for still images. While the JPEG algorithm is very good for still pictures it does not take the temporal redundancy of motion pictures into consideration so it is not the optimal algorithm for all pictures in a video sequence. Coding of i–pictures follows a three step procedure:

1) Discrete Cosine Transform
2) Quantization
3) Variable Length Index Encoding

Recall that encoding and decoding occurs on a block by block basis.

Discrete Cosine Transform

Discrete Cosine Transformation, or DCT, is in the same class of mathematical operations as the Fourier Transform. DCT takes a set of points in a two–dimensional spatial domain and transforms them into the frequency domain. It is defined as:

$$DCT_{u,v} = \frac{1}{4} C(u)C(v) \sum_{i=0}^{7} \sum_{j=0}^{7} B_{i,j} \cos\left(\frac{(2i+1)u\pi}{16}\right) \cos\left(\frac{(2j+1)v\pi}{16}\right) \text{ for } 0 \le u \le 7, 0 \le v \le 7$$

$B_{i,j}$ = the original 8x8 block of data

$DCT_{i,j}$ = the output 8x8 DCT values

$$C(i) = \begin{cases} \frac{1}{\sqrt{2}} \text{ for } i = 0 \\ 1 \text{ for } 1 \le i \le 7 \end{cases}$$

It is possible to calculate the DCT in various ways. Much research has been done to find fast implementations of this formula. Here we present it as two matrix multiplications; yet faster, more elaborate methods exist. Let us define the Cosine Transform matrix, C, as:

$$C_{i,j} = \begin{cases} \frac{1}{\sqrt{8}} & \text{if } i = 0 \\ \sqrt{\frac{2}{8}} * \cos\left(\frac{(2j+1)i\pi}{2x8}\right) & \text{if } i > 0 \end{cases} \quad \text{for } 0 \le i \le 7, 0 \le j \le 7$$

Let C^T denote the transpose of C, i.e. $C^T_{i,j} = C_{j,i}$ for $0 \le i \le 7, 0 \le j \le 7$. Since MPEG uses the DCT in 8x8 configurations only, the Cosine Transform matrix, C, is fixed at:

$$C = \begin{bmatrix} .354 & .354 & .354 & .354 & .354 & .354 & .354 & .354 \\ .490 & .416 & .278 & .098 & -.098 & -.278 & -.416 & -.490 \\ .462 & .191 & -.191 & -.462 & -.462 & -.191 & .191 & .462 \\ .416 & -.098 & -.490 & -.278 & .278 & .490 & .098 & -.416 \\ .354 & -.354 & -.354 & .354 & .354 & -.354 & -.354 & .354 \\ .278 & -.490 & .098 & .416 & -.416 & -.098 & .490 & -.278 \\ .191 & -.462 & .462 & -.191 & -.191 & .462 & -.462 & .191 \\ .098 & -.278 & .416 & -.490 & .490 & -.416 & .278 & -.098 \end{bmatrix}$$

Let B denote the 8x8 block of luminance or chrominance pixel values. Then the discrete cosine transform, DCT, is given by: $DCT = C \times B \times C^T$. Where we perform the multiplication of three 8x8 matrices that results in a final 8x8 matrix. This is the first step of compression. Aside from truncation errors (errors in calculation due to the limited precision of resulting values) this is a lossless compression technique, i.e., no data is lost. The resulting matrices have the following characteristics:

1) The upper left–hand matrix entry, $DCT_{0,0}$, represents the overall magnitude of the original input matrix, B. It is known as the 'DC coefficient' and is generally an order of magnitude larger than all other entries, which are known as 'AC coefficients'.
2) Entries towards the right edge of the matrix represent values corresponding to higher horizontal frequencies.
3) Entries towards the bottom edge of the matrix represent values corresponding to higher vertical frequencies.
4) The magnitude of the entries diminish as they move farther from the DC coefficient.

These factors contribute to the benefits of the next steps in compression.

For example:

$$B = \begin{bmatrix} 135 & 134 & 137 & 130 & 140 & 145 & 169 & 165 \\ 134 & 142 & 130 & 137 & 130 & 138 & 157 & 169 \\ 142 & 145 & 126 & 137 & 143 & 132 & 142 & 162 \\ 158 & 145 & 156 & 150 & 142 & 145 & 136 & 140 \\ 163 & 148 & 146 & 149 & 141 & 134 & 137 & 152 \\ 147 & 167 & 140 & 155 & 155 & 140 & 136 & 152 \\ 136 & 146 & 123 & 127 & 155 & 134 & 130 & 137 \\ 145 & 145 & 146 & 150 & 146 & 157 & 137 & 146 \end{bmatrix}$$ then

$$DCT = C*B*C^T = \begin{bmatrix} 1152 & -9 & 22 & -5 & 16 & -14 & -8 & -5 \\ -2 & -32 & 25 & -11 & -6 & 14 & -3 & 6 \\ -9 & -34 & 1 & 5 & -13 & -2 & -3 & 2 \\ 7 & -1 & 3 & -2 & -1 & -3 & -10 & 5 \\ 15 & 8 & -5 & 1 & -7 & 20 & 20 & 4 \\ -12 & 2 & -9 & 11 & -3 & -6 & -1 & 11 \\ 15 & -1 & -3 & -3 & 2 & -4 & -3 & -5 \\ -15 & -6 & 10 & 4 & 9 & -4 & -4 & 7 \end{bmatrix}$$

Quantization

Quantization is simply a way of limiting a set of input values to a smaller set of output values. Rounding is a form of quantization. MPEG allows each matrix element to be quantized differently. A quantization matrix, Q, may be defined that determines how to quantize each DCT matrix entry. Additionally a general quantizer scale, q, may be defined that scales each entry quantization. This quantizer scale, q, may be re–defined for each macroblock. The result of quantization is referred to as a matrix (block) of indices. Let I represent this 8x8 matrix, then we have the following formula:

$$I_{i,j} = \begin{cases} \dfrac{DCT_{1,1}}{8} & \text{for } i = 0, j = 0 \\ \dfrac{DCT_{i,j}*8}{q*Q_{i,j}} & \text{otherwise} \end{cases}$$

where division is rounded to the nearest integer.

Note that the upper–left–hand element, the DC coefficient, is treated differently than the other values in the DCT block. This is because this value has a large effect on the resulting image quality so its accuracy is fixed.

A quantization matrix may take advantage of human perception at differing frequencies by varying quantization values. High frequency locations (those towards the bottom right of the matrix) may contain larger values so fewer index values will be required and hence fewer bits will be needed for encoding. At the completion of quantization, the index matrix should contain many 0 entries, especially in the high frequency areas. This will contribute to the final compression step. Note that quantization is a lossy compression technique, that is, data is lost in this compression stage. Therefore care should be taken when choosing quanitzation matrix values that insures no critical data is discarded.

Continuing the example above, if we use the default intra–quantization matrix (table A.3) and a quantization scale of 4 we get the following index matrix:

$$I = \begin{bmatrix} 144 & -1 & 2 & 0 & 1 & -1 & -1 & 0 \\ 0 & -4 & 2 & -1 & 0 & 1 & 0 & 0 \\ -1 & -3 & 0 & 0 & -1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & -1 & 0 \\ 1 & 1 & 0 & 0 & 0 & 1 & 1 & 0 \\ -1 & 0 & -1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

Index Coding

The final step is to code the values of the index matrix I. The DC coefficient index and the AC coefficient indices are coded differently.

Coding DC Coefficient Index

Experimentation shows that there is a strong correlation between the DC coefficient indices of sequential blocks of the same type (Y luminance, U or V chrominance). Therefore the difference between indices is coded instead of the indices themselves. The DC coefficient index is coded as the difference between it and the previous block's DC coefficient index. At the beginning of a slice, a value of 128 is used as a predictor (i.e. subtract 128). Note that for the first macroblock in a slice there are 3 blocks that will use 128 as a predictor, the first luminance block, and the two chrominance blocks (blocks 1,5 and 6 in figure 6).

Once the difference is determined, it is encoded by the concatenation of two codes. The first code specifies the number of bits required to determine the sign and magnitude of the difference. The second code specifies the sign and the magnitude of the difference. See tables A.10 and A.11 for both codes. To encode a number we look up the code in each table.

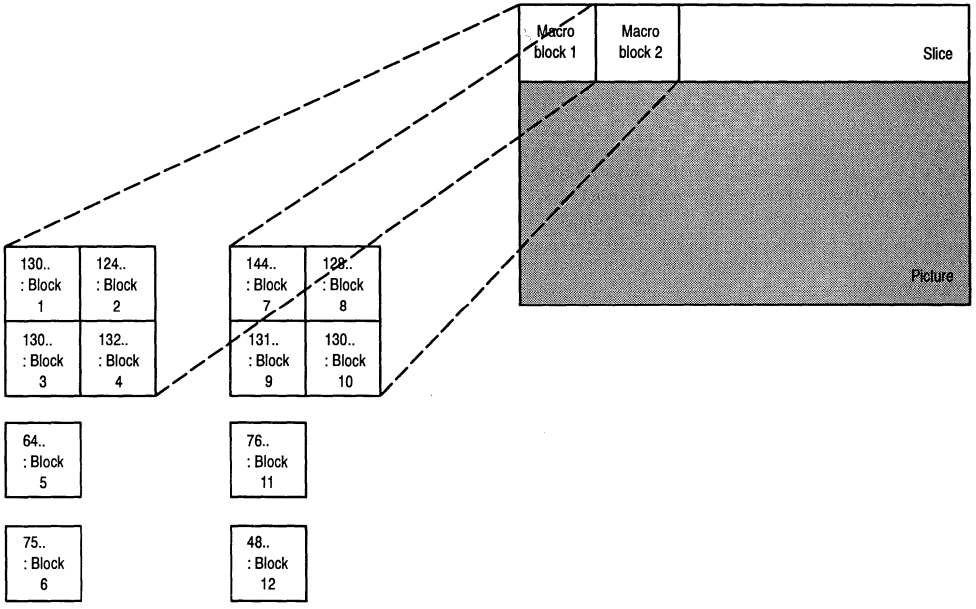


Figure 6. Coding the DC Coefficient Index in I–Pictures

Consider the example shown above. Macroblocks 1 and 2 have the DC coefficient indices as shown. The first block in the slice is block 1. It's DC coefficient index is 130. Since it is the first block in the slice we take the difference using 128 and get 2. This is encoded as 01:10. The colon is used to distinguish the two codes obtained from the two tables. 01 is obtained from table A.10, 10 is obtained from A.11. The second block has a DC coefficient index of 124. The difference from the previous value is –6 which is encoded as 101:010(101 from table A.10, 010 from table A.11). Similarly we get 101:110 for the next block (the difference is 130–124 = 6) and 01:10 for the fourth block (the difference is 132–130 = 2). That completes the luminance blocks for the first macroblock. Each of the two following blocks (U chrominance and V chrominance) are the first of their kind in the slice so we subtract 128 to get –64 and –53 respectively. These values yield codes 1111110:0000000 and 111110:010101 respectively. Note that luminance and chrominance values have different size codes. Macroblock 2 is handled in the same way. The four luminance blocks yield differences of 12, –16, 3, –1 and corresponding codes of 110:1100, 1110:00000, 01:11, and 00:0. The difference of the first luminance block was taken with respect to the fourth luminance block in the previous macroblock. The two chrominance blocks yield differences (with respect to their respective blocks of the previous macroblock) of 12, and –27. The corresponding codes are 11110:1100, 11110:01011.

In between the coded DC coefficient indices are the coded AC coefficient indices.

Coding AC Coefficient Indices

As stated earlier, the index matrix will be sparse (i.e. have many 0 entries), and the 0 entries will mostly populate the high frequency region of the matrix. Therefore, for coding purposes, the data is ordered along the diagonals as shown in figure 7.

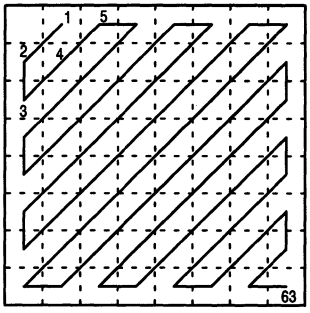


Figure 7. Data ordering within a block.

Note that the upper–leftmost entry, the quantized DC coefficient, is not included in the data ordering. This value was coded separately (see previous section). Once the data is ordered, it is grouped into 'run–length, amplitude' pairs, i.e. pairs of (<number–of–preceeding–zeroes>, <non–zero–value>). For example the sequence:

–1,0,–1,–4,2,0,2,–3,1,1,0,0,–1,1,–1,0,0,0,1,...

would be converted to:

(0,–1), (1,–1), (0,–4), (0,2), (1,2), (0,–3), (0,1), (0,1), (2,–1), (0,1), (0,–1), (3,1), ...

Finally these pairs are coded with variable length codes similar to the method employed for the coded DC coefficient differences. Tables A.12 – A.14 are used to determine the codes corresponding to each run–length, amplitude pair. There is a limited set of short codes for common run–length, amplitude pairs(table A.12). For pairs not included in this table, an escape sequence is used followed by a code for the run–length and a code for the amplitude. Consider the sequence above, we would obtain the following codes:

RUN–LENGTH, AMPLITUDE	CODE	COMMENT
(0,–1)	111	table A.12
(1,–1)	0111	table A.12
(0,–4)	00001101	table A.12
(0,2)	01000	table A.12
(1,2)	0001100	table A.12
(0,–3)	001011	table A.12
(0,1)	110	table A.12
(0,1)	110	table A.12
(2,–1)	01011	table A.12
(0,1)	110	table A.12
(0,–1)	111	table A.12
(3,1)	001110	table A.12
(21,–34)*	000001:010101:11011110	escape sequence, tables A.12, A.13, A.14

The run–length, amplitude pair noted with the * is included to give an example of using the escape sequence for an uncommon pair. The colons are inserted into the code for clarification only. They separate the codes obtained independently from tables A.12, A.13, and A.14 respectively.

Before discussing p and b–pictures let us briefly examine motion estimation and motion compensation, the key ingredients to encoding these two types of pictures.

Motion Estimation

Motion estimation, or ME, is simply a form of pattern matching. ME is the process of determining a motion vector that describes how a macroblock has moved. The MPEG standard does not define what algorithm to use in motion estimation, it only defines the syntax of the resulting motion vectors. ME has been regarded by many to be the most computationally intensive component of the MPEG algorithm. It also has the largest contribution to picture quality and compression rates. Much research has been done for this problem and various solutions exist. We will discuss only a few here.

ME is the process by which the encoder attempts to match the pixels in a macroblock with a previous picture (forward prediction) or with a future picture (backward prediction). Recall that even though we may attempt a match with a future picture, that future picture has been previously encoded (see discussion under Picture Types). ME is composed of two components, a matching criterion, and a search strategy.

When determining what macroblock matching criteria to use, the encoder must also determine whether the match is to be attempted with the original pixel data or the decoded data of the predictor picture(the picture used as a reference for prediction). Using the decoded predictor picture involves more computational overhead but yields less error. Note that this requires that the encoder also contains decode capabilities to decode pictures for use in macroblock matching. Once it is decided which data to match, the matching criteria must be selected. Least mean square error of the difference between macroblocks, and least mean absolute difference are two straight–forward choices.

ME is performed on a 1/2 pixel granularity. This requires some method for arriving at half pixel values. Averaging adjacent pixels has been found to be sufficient for this purpose.

The search strategy defines the search range of the coded video data. Variously sized search ranges are allowed by the MPEG standard. The search range is determined by three fields in the syntax, forward_f_code, backward_f_code, and full_pel. Full_pel specifies whether the search range is in half or full pixel increments. Forward_f_code and backward_f_code specify the range of the motion vectors which may range from –8....7.5 to –1024....1023 (see table A.18). Even though the range may be large, motion estimation is limited to within the boundaries of the predictor picture.

The simplest search strategy, yet also possibly the most computationally expensive method, is a full search. That is, a macroblock is compared(using the pre–determined matching criteria) against all 16x16 pixel groups, aligned on full or half pixels.

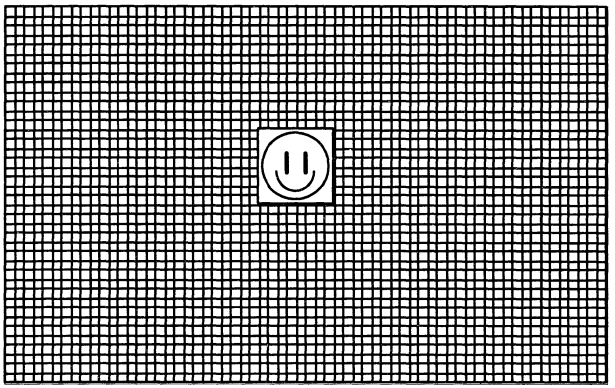
Other methods attempt to limit the number of matches that need to be attempted. For example, in a modified full search, one performs the search against all 16x16 pixel groups on full pixel alignment and then performs the search in half pixel alignment in a limited area around the result. A logarithmic or hierarchical search is a generalization of this approach. It performs the search among a few macroblocks (or blocks that encapsulate data from various localized macroblocks) over a large range centered on the predicted macroblock position. It then iteratively decreases the search range and performs the search among more macroblocks centered on the previous result until the best match is found. Note that this method centers the original large–range search on the original macroblock position. Other methods employ optimizations where some sort of motion prediction is used (based on results of previous motion vectors) that helps to determine the center of the first search iteration. Some of these methods are illustrated below in figure 8.

The standard leaves ME totally up to the developer. Tradeoffs will be made in computational expense and picture quality. The end result is a motion vector (a horizontal and vertical displacement) that describes the relative position of the best matching macroblock in the predictor picture. A secondary result (that is used in later steps) is an associated macroblock of error values (differences between the original and predicted macroblock).

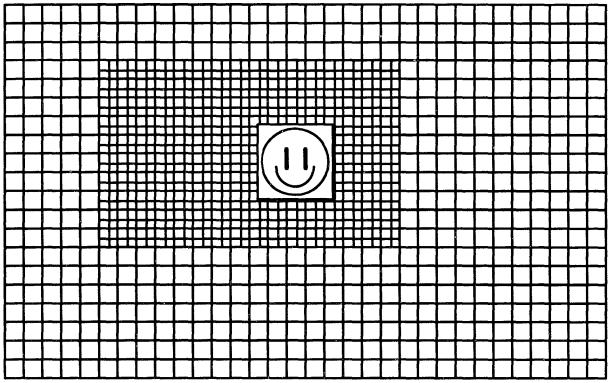
Motion Compensation

Motion compensation, or MC, is far simpler than motion estimation. To perform MC we simply use the motion vectors to get the reference macroblock from the predictor picture. The motion vectors are simply horizontal and vertical offsets relative to the position of the macroblock we are decoding.

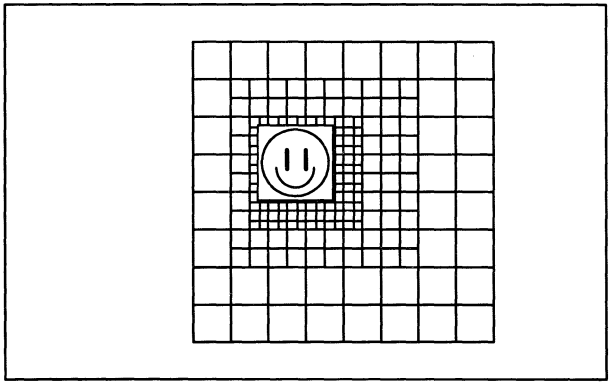
Now that we know what ME and MC are, lets return to discussing the various types of pictures.



Full search: search entire range with half pixel granularity.



Modified full search: search entire range with full pixel granularity, then search with half pixel granularity in a small area around the result.



Hierarchical search: iteratively increase granularity and decrease search field until result is found.

Figure 8. Motion estimation search strategies

Encoding P–Pictures

P–pictures are pictures that are predicted from earlier p or i–pictures. This is forward prediction. Overall the compression rate is better than that of i–pictures. The coding of p–pictures requires motion estimation (see previous discussion). The overall procedure consists of 6 steps:

1) Motion Estimation
2) Code Type Decision
3) Motion Compensation and Error Generation
4) Discrete Cosine Transform
5) Quantization
6) Variable Length Motion Vector and Index Encoding

Where steps 3, 4, 5 and 6 may be omitted depending on the results of step 2.

Motion Estimation

This step has already been discussed. Only forward motion estimation is used. That is, we only attempt to predict the current macroblock based upon the last i or p–picture. This step will result in a motion vector and a macroblock of error (difference) values.

Code Type Decision

As stated earlier, it may not be optimal to encode all macroblocks in p–pictures as predicted from the earlier picture, therefore, macroblocks within a p–picture may be coded in several different ways. The possible types that a macroblock may have in a p–picture are listed below. A macroblock is said to be *predicted* if it has a motion vector not equal to zero. Therefore its video image will be reconstructed from the displaced image data of the previous picture. A macroblock is said to be *not predicted* if it has a motion vector of zero. In this case its video image will be reconstructed from the image data of the previous picture with no displacement. Most macroblocks have a macroblock header, coded in the bitstream, that specifies various pieces of information about the macroblock. This header includes a field that specifies one of the following macroblock types(except for the last type):

pred–mc: This macroblock is predicted (non–0 motion vector) and the error is coded. Individual blocks may be omitted. The default quatization value (found in the slice header) is to be used.

pred–c: This macroblock is not predicted (motion vector = 0) and the error is coded. Individual blocks may be omitted. The default quantization value (found in the slice header) is to be used.

pred–m: This macroblock is predicted (non–0 motion vector) and the error is not coded (i.e. assumed to be zero). The default quantization value is to be used.

intra–d: This macroblock is intra–coded. The default quantization value (found in the slice header) is to be used.

pred–mcq: This macroblock is predicted (non–0 motion vector) and the error is coded. Individual blocks may be omitted. The quantization value to use may be found in the macroblock header.

pred–cq: This macroblock is not predicted (motion vector = 0) and the error is coded. Individual blocks may be omitted. The quantization value to use may be found in the macroblock header.

intra–q: This macroblock is intra–coded. The quantization value to use may be found in the macroblock header.

skipped: This macroblock is entirely skipped. These skipped macroblocks are simply copied from the predictor picture. These effectively are macroblocks with a zero motion vector and zero error. In this case, no code will exist for the contents of this macroblock. In addition, no macroblock header will occur for this macroblock. Existing macroblocks have headers that contain a field known as the macroblock address increment. This field effectively enumerates the macroblocks in raster scan order (within a picture). When one encounters a macroblock address larger than the next macroblock address expected, macroblocks have been skipped. Hence to specify a macroblock as skipped it is only necessary to adjust the address increment of the next coded macroblock. Very few bits are required to code skipped blocks (the only bits used are those expended in the larger macroblock address increment).

Table A.16 gives the codes that specify the macroblock type. Which macroblock type to use may be decided through the following four decisions:

11. Use the vector found in ME or use a 0 motion vector? A motion vector of 0 is not coded, i.e. it will be assumed to be 0 by the decoder.
12. Use intra or non–intra coding? The error from prediction may be large enough to warrant just coding the macroblock in the same method as in i–pictures.
13. If non–intra coding is used, is the error small enough to not code the error? Note that this error is for the entire macroblock. If it is decided to code the error, there is still the flexibility to code only the error for specified blocks of the macroblock.
14. Is the default quantizer scale sufficient or should a new one be defined?

Note that these 4 decisions are not mutually exclusive. That is, one decision may affect others, or may even eliminate the need for other decisions. The MPEG standard does not specify how these decisions are to be made but does offer suggestions. The brute force approach is to code the macroblock in each format and choose the one that requires the least bits to encode. This is computationally unrealistic with existing microcontrollers. Another method is to sequentially answer each of the questions above using some sort of decision criteria. These issues will not be discussed any further here. See the standard for further discussions.

Motion Compensation and Error Generation

To yield good quality video, the error that is encoded should be between the decoded reference (predictor) macroblock and the current macroblock. Note that motion estimation may be performed relative to the original picture data and error macroblocks will be calculated. These error macroblocks may be used to determine the macroblock type but should not be used for the coded error terms. A decoder will add the error terms to the decoded reference (predictor) macroblock and for best results the encoder should generate the error terms relative to the same decoded macroblock. Therefore, in most cases, MPEG encoders will incorporate partial decoders.

Once motion vectors have been determined from the previous step, we perform motion compensation using the previously decoded picture and generate errors with respect to the current macroblock. The error macroblock is taken as the difference between the predicted decoded macroblock and the current macroblock to be coded. This error macroblock then undergoes the next 3 steps.

Discrete Cosine Transformation

This step is the same as that in i–pictures but is applied to the blocks of the error macroblock. Blocks that have no error (all entries are zero) do not undergo the DCT process. They will not be coded. This step is applied only to those macroblock types that require coding of the DCT values.

Quantization

For intra–coded blocks (i.e. blocks in intra–coded macroblocks) this step is the same as that in i–pictures except that the results of the division are truncated towards zero (not rounded). For all other blocks no distinction is made between AC and the DC coefficients. So our formula is:

$$I_{i,j} = \frac{DCT_{i,j} * 8}{q * Q_{i,j}} \quad \text{for } 0 \le i \le 7,\ 0 \le j \le 7 \text{ where division is truncated towards 0.}$$

Note that p–picture macroblocks (even those intra–coded) use a different default quantization matrix (table A.4). Quantization is only applied to blocks that are coded.

Variable Length Motion Vector and Index Encoding

Two types of data need to be encoded, motion vectors (if present) and quantized indices (if present). If the macroblock is a skipped macroblock then the only coding necessary is adjustment of the next coded macroblock's macroblock address increment(see discussion of macroblock types above).

Indices of intra–coded blocks are coded in a similar fashion as in i–pictures, except the DC coefficient predictor used is 128 (unless the previous block was also intra–coded and then its DC coefficient is used as the predictor). Indices of non–intra–coded blocks are coded in the same format as in i–pictures except no distinction is made between the DC and AC coefficients. All indices are treated as AC values. The entries are ordered as in figure 9 below and then translated into run–length, amplitude pairs and coded as done in i–pictures.

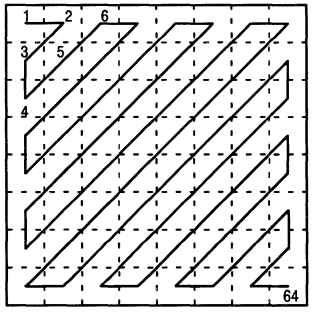


Figure 9. Data ordering within a block.

Coding the motion vectors is more complex. Readers not interested in the gory details of variable length encoding of the motion vectors are encouraged to skip directly to the next section. Variable length encoding of the motion vectors is done in such a way that only one table needs to be used (table A.18). Various flags and values need to be set. Although various macroblocks may have been predicted to move different amounts in a single picture, the range and granularity of motion are fixed at the picture level. There is a flag, full_pel_forward_vector, that is set if the motion vectors are expressed in units of 1 pixel, otherwise 1/2 pixel units are used. A second field, forward_f_code, is used with full_pel_forward_vector to define the range of motion vectors(see table A.18). Forward_f_code determines two variables: forward_r_size, and forward_f (table A.7). These are the numbers of bits to encode a residual number (discussed more below), and a measure of the maximum magnitude of motion vectors.

Experimentation has shown that motion vectors between macroblocks tend to be strongly correlated (consider a pan where each macroblock will have the same motion vector). Therefore the difference between motion vectors is coded as opposed to the vectors themselves. The difference is taken with respect to the previous motion vector of the macroblock within the same slice. Horizontal and vertical components are treated as distinct groups. At the beginning of a slice, or when the previous macroblock was intra–coded, zero is used as the previous motion vector. Once the differences are calculated, they are mapped to the vector range by adding or subtracting a modulus that depends on forward_f as listed in table A.19 (this is recoverable during encoding by comparing the resulting motion vector with the allowable range and adjusting by the modulus when out of bounds). Then each difference is broken into a base and a residual component as follows:

$$\text{base\_component} = \frac{\text{motion\_vector\_diff} + (\text{sign}(\text{motion\_vector\_diff}) * (\text{forward\_f} - 1))}{\text{forward\_f}} \quad \text{truncate towards 0}$$

residual_component = remainder of above division

$$\text{where} \quad \text{sign}(X) = \begin{cases} -1 & \text{if } X < 0 \\ 0 & \text{if } X = 0 \\ 1 & \text{if } X > 0 \end{cases}$$

The base component is coded according to table A.20. The residual component is coded as an unsigned integer using forward_r_size bits. When the motion vector difference is negative, the remainder is also understood to be negative. Note also that the base component and the motion vector difference will always have the same sign. Consider the following example:

Let us consider the horizontal components of motion vectors only (the vertical components are treated identically). Suppose 4 macroblocks in a slice have horizontal motion components:

3, 23, –21, –23

Suppose that forward_f_code is 2 and full_pel_forward_vector is 1. Together these specify the range of motion is –32 to 31 pixels (see table A.18). First we take the differences between successive motion vectors to get:

3, 20, –44, –2

The 3 is obtained by using 0 as the previous motion vector since it was the first macroblock in the slice. Now we need to constrain the difference values to the allowable range so we add 64 to –44. Now our values read:

3, 20, 20, –2

Now we perform the calculations above to get the following (base_component, residual_component) pairs:

(2,0), (10,1), (10,1), (–1,–1)

Note that forward_f = 2. The base_component code is found in table A.20 and the residual_component code is simply the unsigned 1–bit integer of the absolute value of the residual_component. So the codes obtained are:

0010:0, 0000010011:1, 0000010011:1, 011:1

The colons are only present to distinguish the two codes obtained. They are omitted from the bit stream. The macroblock header stores the two codes as separate fields.

Encoding B–Pictures

B pictures are interpolated from earlier and later p or i–pictures. These provide the highest amounts of compression. The overall coding procedure consists of 6 steps:

1) Motion Estimation
2) Code Type Decision
3) Motion Compensation and Error Generation
4) Discrete Cosine Transformation
5) Quantization
6) Variable Length Motion Vector and Index Encoding

Where steps 3, 4, 5 and 6 may be omitted depending on the results of step 2.

Motion Estimation

We employ both forward and backward motion estimation. This step will result in 2 motion vectors, a forward vector and a backward vector. In addition 3 error macroblocks may be constructed; one for the difference between the current macroblock and the forward predicted macroblock; one for the difference between the current macroblock and the backward predicted macroblock; and one for the difference between the current macroblock and the interpolated predicted macroblock. The interpolated predicted macroblock is simply the average of the forward and backward predicted macroblocks. These will be used to help determine which macroblock type to use.

Code Type Decision

Like macroblocks within a p–picture, b–picture macroblocks may be coded in several different ways. The possible types that a macroblock may have in a b–picture are the following:

pred–i:	This macroblock is interpolated (both forward and backward predicted) and the error is not coded. The default quantization value (found in the slice header) is to be used.
pred–ic:	This macroblock is interpolated and the error is coded. The default quantization value (found in the slice header) is to be used.
pred–b:	This macroblock is backward predicted and the error is not coded. The default quantization value (found in the slice header) is to be used.
pred–bc:	This macroblock is backward predicted and the error is coded. The default quantization value (found in the slice header) is to be used.
pred–f:	This macroblock is forward predicted and the error is not coded. The default quantization value (found in the slice header) is to be used.
pred–fc:	This macroblock is forward predicted and the error is coded. The default quantization value (found in the slice header) is to be used.
intra–d:	This macroblock is intra–coded. The default quantization value (found in the slice header) is to be used.
pred–icq:	This macroblock is interpolated and the error is coded. Individual blocks may be omitted. The quantization value to use may be found in the macroblock header.
pred–fcq:	This macroblock is forward predicted and the error is coded. Individual blocks may be omitted. The quantization value to use may be found in the macroblock header.
pred–bcq:	This macroblock is backward predicted and the error is coded. Individual blocks may be omitted. The quantization value to use may be found in the macroblock header.
intra–q:	This macroblock is intra–coded. The quantization value to use may be found in the macroblock header.
skipped:	This macroblock is entirely skipped. No macroblock header will occur for this macroblock. These are different than p–picture skipped macroblocks. These skipped macroblocks use the same macroblock type and motion vector as those of the previously coded macroblock. This requires that the previously coded macroblock exists and was not intra–coded. Very few bits are required to code these blocks (the only bits used are those expended in the larger macroblock address increment).

Deciding which type to use requires more effort than deciding p–picture macroblock types. The following four questions need to be answered.

10. Use interpolated, forward, or backward prediction?
11. Use intra or non–intra coding? The error from prediction may be large enough to warrant just coding the macroblock in the same method as in i–pictures.
12. If non–intra coding is used, is the error small enough to not code the error?
13. Is the default quantizer scale sufficient or should a new one be defined?

As in p–pictures, the standard does not specify how to choose a macroblock type. The standard does suggest, however, that the encoder should try to use skipped macroblocks whenever possible due to the high compression rates they offer.

If any predicted macroblock type is chosen then some or all of the following steps will apply.

Motion Compensation and Error Generation

This step is the same as in p–pictures. If both forward and backward prediction are used then both motion compensated macroblocks should be generated, averaged, and used as a basis for the error difference.

Discrete Cosine Transformation

This step is the same as that in p–pictures.

Quantization

This step is the same as that in p–pictures.

Variable Length Motion Vector and Index Encoding

Coding is performed in the same way as in p–pictures. Backward prediction is handled identically to forward prediction. Backward motion vectors are coded in the same manner as forward vectors. If the macroblock type specifies interpolated prediction then the backward vector codes immediately follow the forward vector codes in the bit stream. Indices are coded exactly as in p–pictures.

Encoding Summary

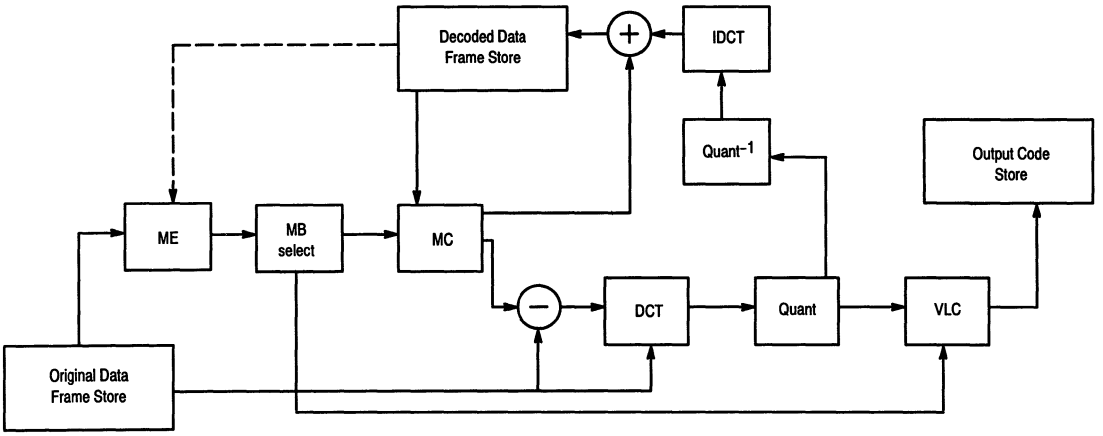


Figure 10. MPEG Encoder

The Original Frame Store holds the original SIF data and supplies macroblocks of current, previous, and future pictures to the encoder. The ME box performs motion estimation. It returns motion vectors and error terms to the MB Select box. The MB Select box selects the type of macroblock to use. Once this has been decided, the motion compensation unit, MC, performs motion compensation on the decoded predictor picture. The predicted macroblock is then used to generate error terms by taking the difference with the original macroblock. The DCT unit computes the DCT of the error terms or of the original blocks of data depending on the macroblock type. The results are then passed to quantization. The final results are variable length coded (in VLC) and stored in Output Code Store. This unit saves entire encoded pictures. It does this so that the pictures may be re–ordered from display order to encoding order. Before variable length coding, the results of quantization are decoded through de-quantization, Quant^{-1}, and the inverse discrete cosine transform, IDCT. The results of the IDCT may be added to the MC output depending on the macroblock type. These decoded macroblocks are stored in the Decoded Data Frame Store. This provides decoded picture information for use by the motion compensation unit and by possibly the motion estimation unit. There is a very important unit that has been left out for purposes of simplicity. This unit is the Bit Rate Control Unit. This unit provides feedback to the VLC and Quant units to control the numbers of bits being used for coding. This is necessary to prevent underflow and overflow conditions during decoding of the bit stream. Increasing the quantizer scale will decrease the image quality and increase the compression. It is also possible to add stuffing, or padding code in the bit stream through the VLC.

This block diagram is not intended to show the most efficient MPEG encoder but is simply intended to show the overall flow of information.

Storage/Transmission

Storage and transmission of the data may take several forms. Any media capable of storing or transmitting bit streams at the targeted rate (1.5 Mbits/sec) may be applicable.

Decoding

In general, decoding is a much simpler process than encoding. Motion estimation is not performed. Instead we have the simple process of motion compensation(discussed earlier). Decoders also do not have the difficult task of choosing macroblock types. Overall, each step in the encoding process has an inverse procedure which is used in decoding.

Decoding I–Pictures

Decoding I–pictures follows a 3 step procedure which is the simple reverse process of encoding:

1) Variable Length Index Decoding
2) Dequantization
3) Inverse Discrete Cosine Transformation

Variable Length Index Decoding

This step simply looks up the variable length code in the same tables used for decoding. First the DCT coefficient is decoded. Next we decode the list of run–length, amplitude pairs. These pairs are then converted into the equivalent stream of 63 integers. We reconstruct the 8x8 matrix (recall that the stream was created from the zig–zag pattern in figure 7). Now we are ready for dequantization.

Dequantization

In quantization we performed a division; in dequantization we just perform a multiplication. We use the same quantization matrix, Q, as in encoding. This matrix either will be the default matrix or will have been redefined in the sequence header. The quantization scale is either found in the macroblock header or we use default value found in the slice header. Let I represent the 8x8 matrix of index values, and X the result after dequantization, then we have:

$$X_{i,j} = \begin{cases} I_{1,1} * 8 & \text{for } i = 0,\ j = 0 \\ \dfrac{I_{i,j} * q * Q_{i,j}}{8} & \text{otherwise} \end{cases}$$

Inverse Discrete Cosine Transformation

The DCT has an inverse procedure known as the inverse discrete cosine transformation, IDCT. Recall that DCT = $C*B*C^T$. IDCT is given by: IDCT = C^T*X*C where X is the 8x8 matrix dequantization result. The final result is a block of pixel values of the decoded i–picture.

Decoding P–Pictures

Decoding p–pictures follows a 4 step process that is the reverse of encoding (without the macroblock decision step):

1) Variable Length Motion Vector and Index Decoding
2) Dequantization
3) Inverse Discrete Cosine Transformation
4) Motion Compensation

All of the above steps may be eliminated if the macroblock is skipped. That is, if the current macroblock address increment specifies that we skipped one or more macroblocks (see discussion in Appendix A on skipped macroblocks and macroblock address increment), then we just copy the macroblock from the predictor picture (i.e. equivalent to having a block with no error and a 0 motion vector).

Variable Length Motion Vector and Index Decoding

If the macroblock type specifies intra–coding then index decoding follows the same procedure as in i–pictures. Otherwise, we decode each block as in i–pictures but no distinction is made for the first (DC) coefficient. More explicitly, we decode all information as run–length, amplitude pairs using table A.12, convert to a stream of 64 integers and reconstruct the 8x8 index block (using the zig–zag pattern in figure 9). Note that we only decode those blocks that have been encoded. The code block pattern field in the macroblock header specifies which blocks have been coded(see table A.21). All other blocks are assumed to be 0. If the macroblock type specifies that no blocks have been encoded then all blocks are assumed to be 0.

Motion vector decoding follows the reverse procedure as encoding. Readers that are not interested in the details of variable length motion vector decoding are encouraged to skip to the next section. The horizontal vector is first decoded followed by the vertical vector. The same process applies to each. The vectors may be absent(assumed to be 0) depending on the macroblock type. First we get the base component of the vector. This is coded as motion_horizontal/vertical_forward_code and we use table A.21 to decode it. Forward_f_code determines the number of bits (table A.7:forward_r_size) to use in reading the residual component. We use the inverse formula from motion vector encoding:

$$\text{motion\_vector\_diff} = \text{residual\_component} + \text{forward\_f} * \text{base\_component} - (\text{sign}(\text{base\_component}) * (\text{forward\_f} - 1))$$

Note that the sign of the base component is the same as the sign of the motion vector differential. Note also that the residual component should be treated as the same sign as the base component. Once we have the motion vector differential we add it to the previous motion vector (or 0 at the beginning of a slice or after an intra–coded block). If the resulting value is not within the allowable vector range (see Table A.18) we add or subtract the modulus (table A.19) to bring the result into bounds. This is our final vector value. This procedure is followed for both horizontal and vertical components of the motion vector.

Let us try an example. Suppose we have the following horizontal vector components for 4 macroblocks in a slice:

00100, 00000100111, 00000100111, 0111

These are the same codes we generated in discussing how to encode motion vectors. Suppose that the picture header specifies full_pel_forward is 1 and forward_f_code is 2. Then we know (table A.18) our vectors must fall within –32 to 31 pixels. Forward_r_size is 1 (table A.7) so the last bit in each code is the residual component. We use table A.20 to decode the base components. We get the following pairs of base and residual components:

(2, 0), (10, 1), (10, 1), (–1, –1)

Note that we have adjusted the sign of the residual component to match that of the base components. Forward_f is 2 (table A.7) and we apply the above formula to get the following motion vector differentials:

3, 20, 20, –2

If we assume the first vector is for the first macroblock in a slice we accumulate the values to get the actual motion vectors:

3, 23, 43, 41

Both 43 and 41 are out of or vector range so we subtract the modulus amount, 64 (from table A.19), to get our final vectors:

3, 23, –21, –23

These values match the original vectors! (see the example in the encoding section)

Dequantization

For intra–coded macroblocks the procedure is the same as in i–pictures except the default quantization matrix is the non–intra–matrix specified in the sequence header. For all other coded macroblocks the formula used is as follows:

$$X_{i,j} = \frac{I_{i,j} * q * Q_{i,j}}{8} \text{ for } 0 \leq i \leq 7, 0 \leq j \leq 7$$

Where X is the resulting dequantized values and I is the matrix of indices to dequantize. This is the same procedure as in i–pictures except no special case is made for the DC coefficient.

Inverse Cosine Transformation

This step is the same as is i–pictures. This step is only performed for blocks that are coded. Other blocks are assumed to be consist of all 0's.

Motion Compensation

Motion compensation (see earlier discussion) is performed and we then take the reference macroblock and add its pixel values to the available error pixel values (the result of the IDCT) to get the final SIF format macroblocks.

This completes the decoding process for p–pictures.

Decoding B–Pictures

Decoding b–pictures follows the same 4 step process as in p–pictures:

1) Variable Length Motion Vector and Index Decoding
2) Dequantization
3) Inverse Discrete Cosine Transformation
4) Motion Compensation

Steps 2 and 3 may be eliminated if the macroblock is skipped. If the current macroblock address increment specifies that we skipped one or more macroblocks (see discussion in Appendix A on skipped macroblocks and macroblock address increment) then we use the previous macroblock type and motion vector(s) to perform step 4.

Variable Length Motion Vector and Index Decoding

This follows the same process as in p–pictures except there may be twice as much work to do if the macroblock specifies interpolated prediction (both forward and backward prediction). The macroblock type determines whether to decode forward vectors, backward vectors, or both.

Index decoding is the same as in p–pictures.

Inverse Cosine Transform

This step is the same as is i–pictures. This step is only performed for blocks that are coded. Other blocks are assumed to be consist of all 0's.

Motion Compensation

This step is the same as in p–pictures. If both backward and forward prediction are used then the average of the two individual motion compensated macroblocks is used to add to the error terms.

Decoding Summary

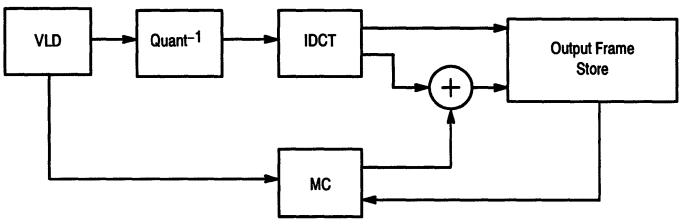


Figure 11. MPEG Decoder

Decoding starts with parsing and translating the variable length codes of the bit stream. This function is performed by the VLD, variable length decoder. Depending on the macroblock type, either pixel or error blocks may be sent to the dequantization unit. The dequantized blocks are then passed to the inverse cosine transformation unit. Motion vectors may also be passed to the motion compensation unit. This unit uses previously decoded pictures from the Output Frame Store to perform motion compensation. The predicted macroblock is then passed to the adder to add the error terms. Finally the decoded blocks are stored in the Output Frame Store. This unit provides previously coded macroblocks to the MC unit and also saves entire pictures for re–ordering into display order. This completes the decoder. As in the encoder, this may not be the optimum decoder configuration but is intended to show flow of control.

Postprocessing and Display

Postprocessing involves converting SIF format video into the target display format. This may be CCIR 601 in which case upsampling will be required to get a resolution of 720x480 luminance pixels. Further sampling may be required to change the frequency. It may also be desirable to transform the YUV output into RGB format.

Appendix A: MPEG Coded Bit Stream Syntax

This appendix specifies the format of the syntax an provides all the tables necessary to encode or decode a bitstream. The hierarchical organization of the data has already been discussed. A typical bitstream composition is shown below in figure 12.

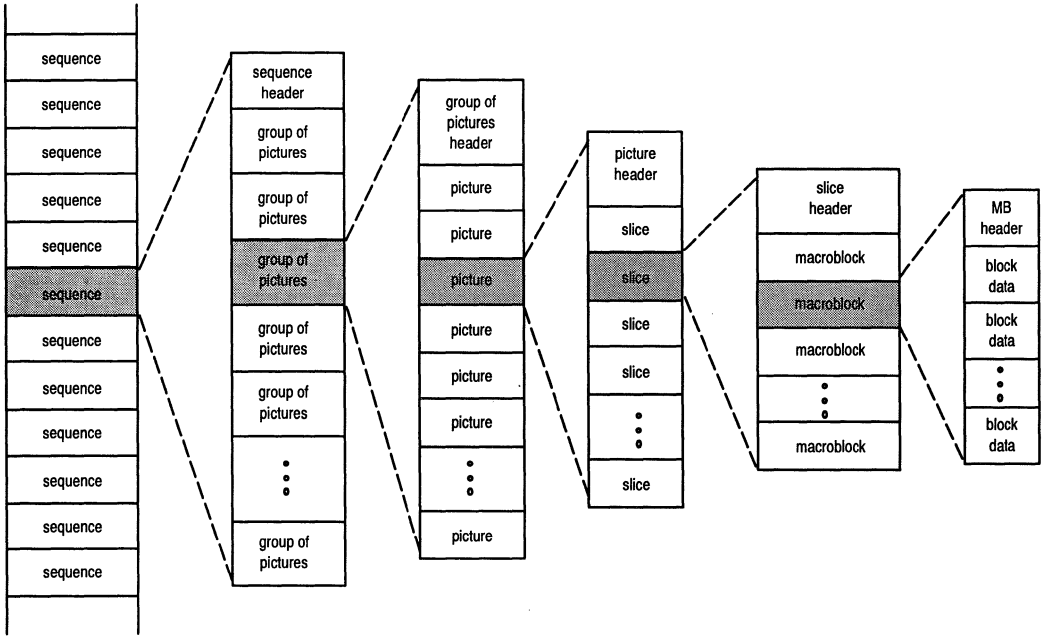
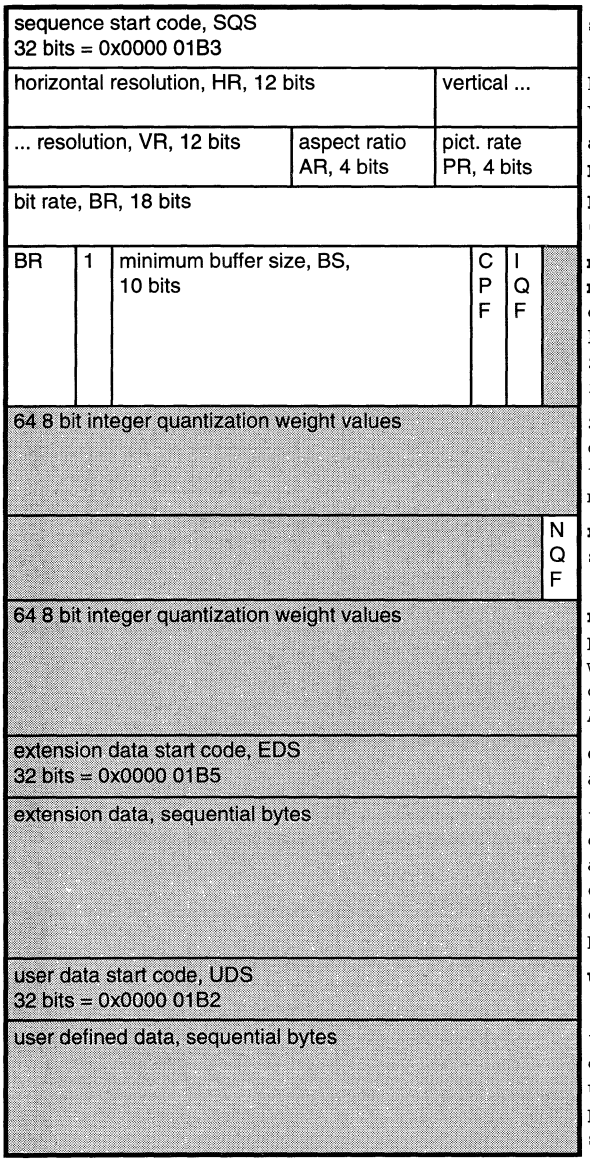


Figure 12. Typical composition of MPEG bit stream

Each level in the hierarchy has a header that contains various fields of information. The format of each header is described in the subsequent pages. Fields that are shaded in the headers are optional or present only under specified conditions.

4

SEQUENCE HEADER



sequence start code: byte aligned.

horizontal resolution
vertical resolution

aspect ratio: index to table
picture rate: index to table.

bit rate: in units of 400bps; 0x3FFFF specifies variable bit rate.

marker bit: set to 1
min. buffer size: units of 2K bytes.
constrained parameter flag: set if bit stream is constrained.
intra quantization matrix flag: set if matrix included.

intra quantization matrix: present only if the preceding flag was set to 1, if set to 0, the default matrix is shown in table A.3

non-intra quantization matrix flag: set if matrix included.

non-intra quantization matrix: present only if the preceding flag was set to 1, if set to 0, the default matrix is shown in table A.4.

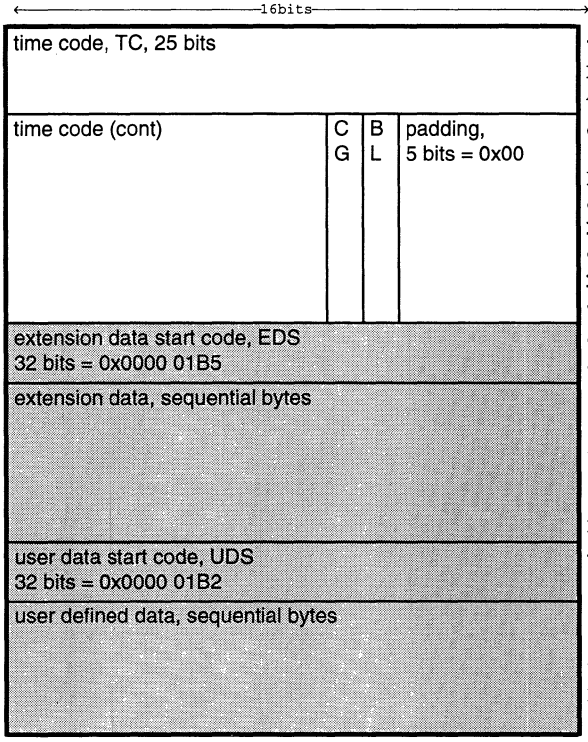
extension data start code: byte aligned.

this is data that allows for future extensions and is expressed in bytes and continues until the next start code. It is present only if the extension data start code was present.

user data start code: byte aligned.

this is data, defined by the user, expressed in bytes, and continues until the next start code. It is present only if the extension data start code was present.

GROUP OF PICTURES HEADER



time code: refers to the first picture in display order, see table A.5 for decoding TC

closed group of pictures flag: set if group is closed, i.e. group can be decoded independent of previous group.
broken link flag: set if previous group of pictures no longer present.
padding: to make start codes byte aligned.

extension data start code: byte aligned.

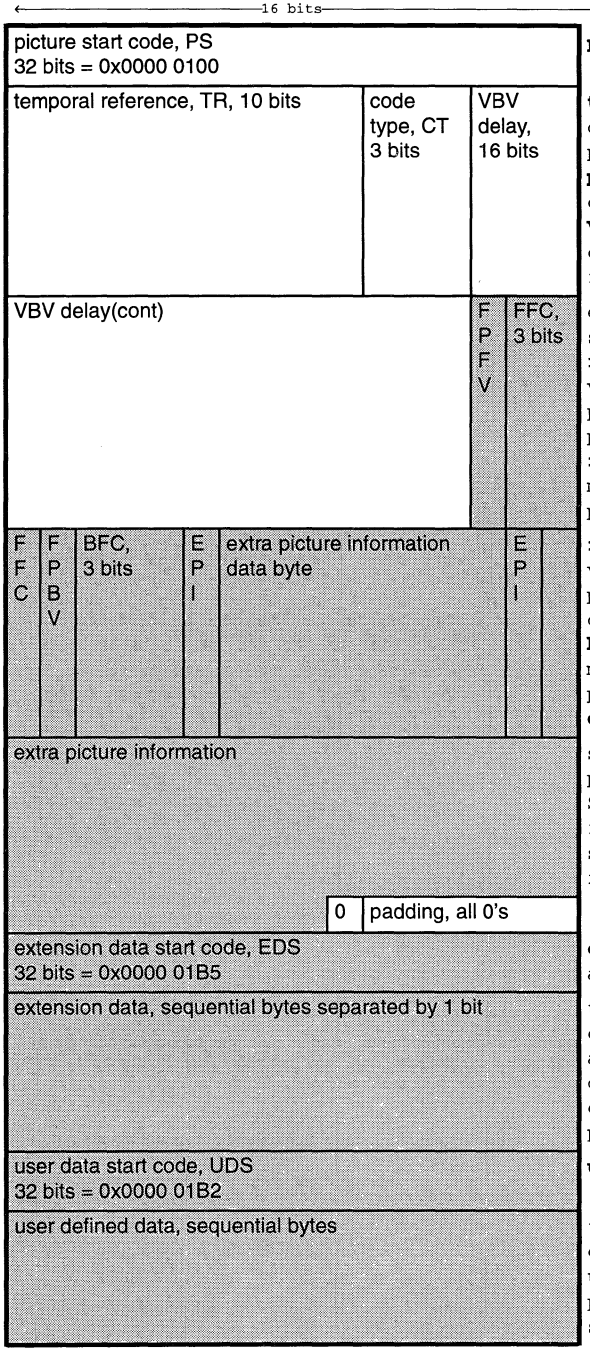
this is data that allows for future extensions and is expressed in bytes and continues until the next start code. It is present only if the extension data start code was present.

user data start code: byte aligned.

this is data, defined by the user, expressed in bytes, and continues until the next start code. It is present only if the extension data start code was present.

4

PICTURE HEADER



picture start code: byte-aligned

temporal reference: counts the display order of each picture(relative to group start).
picture code type: defines the type of picture, see table A.6.
Virtual Buffer Verifier delay: units of 1/90000 sec, specifies time to fill buffer from empty to current state at sequence specified bit rate.
full pel forward vector: set if vector precision is 1 pel, else precision is .5 pels, P and B pictures only.
forward f code: specifies maximum magnitude of forward vectors; P,B pictures only, see table A.7.
full pel backward vector: set if vector precision is 1 pel, else precision is .5 pels, B pictures only.
backward f code: specifies maximum magnitude of backward vectors; B pictures only.
extra picture information flag: specifies that a byte of extra picture information is to follow. Successive information bytes may follow each preceded by a 1 bit. 0 specifies the end of extra picture information data.

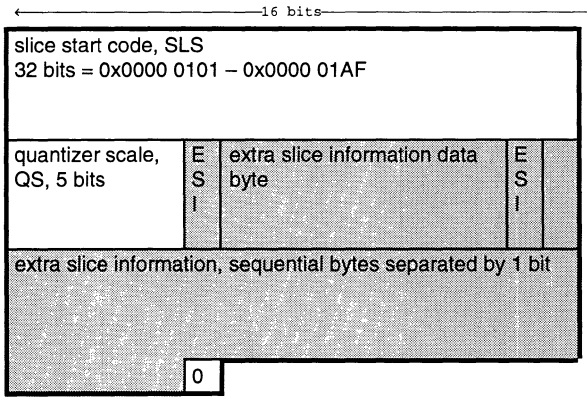
extension data start code: byte aligned.

this is data that allows for future extensions and is expressed in bytes and continues until the next start code. It is present only if the extension data start code was present.

user data start code: byte aligned.

this is data, defined by the user, expressed in bytes, and continues until the next start code. It is present only if the extension data start code was present.

SLICE HEADER



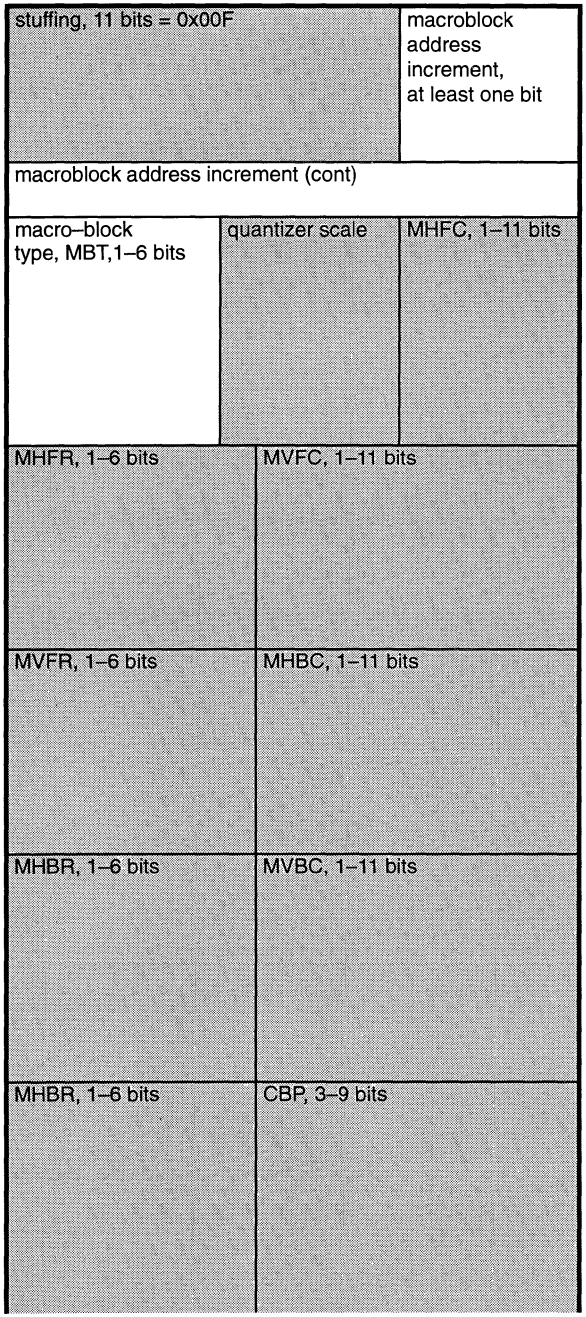
slice start code: byte aligned: the last 8 bits specify the vertical row(1-based) of the first macroblock in the slice.

quantizer scale: this will scale the quantization of the DCT coefficients
extra slice information flag: set to 1 if a

byte of extra slice information is to follow. Subsequent information may follow in bytes preceded by a set bit. A 0 bit signifies the

end of the data.

MACROBLOCK HEADER



stuffing: may be used to prevent underflow; may also repeat as necessary.

macroblock address increment: this specifies the increment in address of the current macroblock.

See Table A.9 and its associated discussion.

macroblock type: specifies whether macroblock is intra-coded, forward-predicted, backward-predicted, ... see tables A.15-A.17

quantizer scale: present if ICT=01.

motion horizontal forward code: present only if macroblock type specifies macroblock_motion_forward flag

motion horizontal forward r: present only if MHFC is not 0 and FFC does not = 1. MHFR and MHFC determine the forward horizontal vector component.

motion vertical forward code: present only if macroblock type specifies macroblock_motion_forward flag

motion vertical forward r: present only if MVFC is not 0 and FFC does not = 1. MVFR and MVFC determine the forward horizontal vector component.

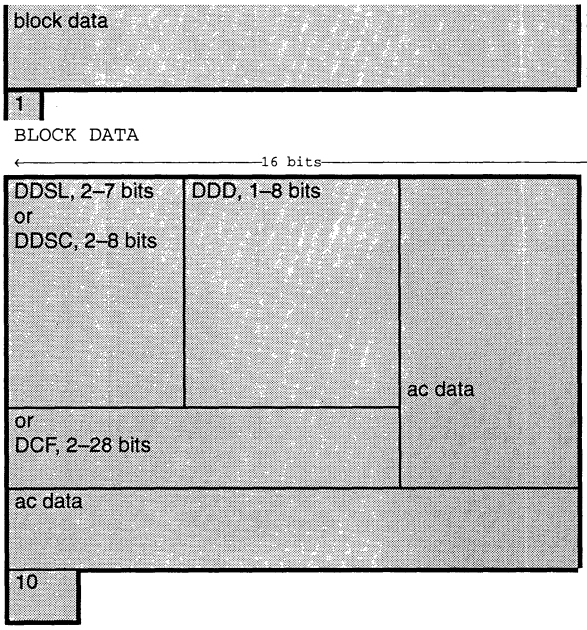
motion horizontal backward code: present only if macroblock type specifies macroblock_motion_backward flag

motion horizontal backward r: present only if MHBC is not 0 and FFC does not = 1. MHBR and MHBC determine the forward horizontal vector component.

motion vertical backward code: present only if macroblock type specifies macroblock_motion_forward flag

motion vertical backward r: present only if MVBC is not 0 and FFC does not = 1. MVBR and MVBC determine the forward horizontal vector component.

coded block pattern: present only if MBT has macroblock_pattern flag set. This is used to specify which blocks are coded within a macroblock. See Table A.21.



block data: see syntax below
1: end code for D-picture macroblocks only

dct dc size luminance or dct dc size chrominance: both for intra-coded blocks only. 2-7 or 2-8 bits that specify the base value and size of the dct difference value.
dct dc differential: 1-8 bits that specifies the dct value differential from the previous block of the same type.

*** OR INSTEAD OF THESE 2 CODES ***
dct coeff first: the first dct value for a non-intra-coded block.

ac data: series of 3-28 bit codes for each of the remaining 63 dct differentials.

end of block: 10 denotes end of block data

NOTE: for p-pictures and b-pictures the dct data refers to error-correction values. If a block has little or no error the encoder may choose not to code the block, i.e. the block is skipped and CBP is set appropriately to signify this.

A.1: Aspect Ratio	
CODE	HEIGHT/WIDTH
0000	forbidden
0001	1.0
0010	0.6735
0011	0.7175
0100	0.7615
0101	0.8055
0110	0.8495
0111	0.8935
1000	0.9375
1001	0.9815
1010	1.0255
1011	1.0695
1100	1.1135
1101	1.1575
1110	1.2015
1111	reserved

A.2: Picture Ratio	
CODE	PICTS/SEC
0000	forbidden
0001	23.976
0010	24
0011	25
0100	29.97
0101	30
0110	50
0111	59.94
1000	60
1001	reserved
1010	reserved
1011	reserved
1100	reserved
1101	reserved
1110	reserved
1111	reserved

A.3: Default Intra Quantization Matrix							
8	16	19	22	26	27	29	34
16	16	22	24	27	29	34	37
19	22	26	27	39	34	34	38
22	22	26	27	29	34	37	40
22	26	27	29	32	35	40	48
26	27	29	32	35	40	48	58
26	27	29	34	38	46	56	69
27	29	35	38	46	56	69	83

A.4: Default Non–Intra Quantization Matrix							
16	16	16	16	16	16	16	16
16	16	16	16	16	16	16	16
16	16	16	16	16	16	16	16
16	16	16	16	16	16	16	16
16	16	16	16	16	16	16	16
16	16	16	16	16	16	16	16
16	16	16	16	16	16	16	16
16	16	16	16	16	16	16	16

A.5: Time Code		
FIELD	BITS	VALUES
drop frame flag	1	–
hours	5	0 – 23
minutes	6	0 – 59
fixed	1	1
seconds	6	0 – 59
picture number	6	0 – 59

A.6: Picture Type	
CODE	PICTURE TYPE
000	forbidden
001	I picture
010	P picture
011	B picture
100	D picture
101	reserved
110	reserved
111	reserved

A.7: Forward F Code		
CODE	forward_r_size	forward_f
1	0	1
2	1	2
3	2	4
4	3	8
5	4	16
6	5	32
7	6	64

A.8 Backward F Code		
CODE	backward_r_size	backward_f
1	0	1
2	1	2
3	2	4
4	3	8
5	4	16
6	5	32
7	6	64

Macroblock Address Increment

Encoders and decoders keep track of the placement of macroblocks within a picture through the use of the macroblock address increment found in each macroblock header, and through the use of the vertical slice position(the last 8 bits of the slice start code). Macroblocks are given addresses starting with 0 in the upper left hand corner of the picture and incremented from left to right and top to bottom(i.e. raster scan order). The address of a macroblock is determined by adding the previous macroblock address value with the macroblock address increment of the current macroblock header. In general, i–picture macroblocks always have increments of 1. P–pictures and b–pictures may have increments greater than 1. When this happens we have encountered skipped macroblocks. In p–pictures the skipped macroblocks are simply copied from the reference picture. In b–pictures the skipped macroblocks are motion compensated using the most recent motion vector values.

A.9: Macroblock Address Increment

INCREMENT	CODE	INCREMENT	CODE
1	1	17	000 001 0110
2	011	18	000 001 0101
3	010	19	000 001 0100
4	0011	20	000 001 0011
5	0010	21	000 001 0010
6	0 0011	22	000 0010 0011
7	0 0010	23	000 0010 0010
8	000 0111	24	000 0010 0001
9	000 0110	25	000 0010 0000
10	0000 1011	26	000 0001 1111
11	0000 1010	27	000 0001 1110
12	0000 1001	28	000 0001 1101
13	0000 1000	29	000 0001 1100
14	0000 0111	30	000 0001 1011
15	0000 0110	31	000 0001 1010
16	00 0001 0111	32	000 0001 1001
		33	000 0001 1000
		escape	000 0000 1000
		padding	000 0000 1111

Note that there are codes for increments only up to value 33. For values above 33, each appearance of the escape sequence(000 0000 1000) will add 33 to the following address increment. For example, to get an increment of 70, use 000 0000 1000, 000 0000 1000, 0011 = <escape> <escape> <4> = 33 + 33 + 4 = 70.

The padding code, 000 0000 1111, is also shown here. This code may appear before the address increment an arbitrary amount of times to prevent underflow. It is discarded by the decoder.

Table A.10: DC Differential Size Code			
DIFFERENCE (absolute)	SIZE	LUMA. CODE	CHROM. CODE
0	0	100	00
1	1	00	01
2 ... 3	2	01	10
4 ... 7	3	101	110
8 ... 15	4	110	1110
16 ... 31	5	1110	11110
32 ... 63	6	11110	111110
64 ... 127	7	111110	1111110
128 ... 255	8	1111110	11111110

Table A.11: DC Sign & Magnitude Code		
DIFFERENCE	SIZE	SIGN, MAGNITUDE CODE
–128 ... –255	8	00000000 ... 01111111
–64 ... –127	7	0000000 ... 0111111
–32 ... –63	6	000000 ... 011111
–16 ... –31	5	00000 ... 01111
–8... –15	4	0000 ... 0111
–4 ... –7	3	000 ... 011
–2 ... –3	2	00 ... 01
–1	1	0
0	0	
1	1	1
2 .. 3	2	10 ... 11
4 ... 7	3	100 ... 111
8...1 5	4	1000 ...1111
16 ... 31	5	10000 ... 11111
32 ... 63	6	100000 ... 111111
64 ... 127	7	1000000 ... 1111111
128 ... 255	8	10000000 ... 11111111

Table A.12: Run–Length, Amplitude Pair Codes					
RUN–LENGTH	AMPLITUDE	CODE	RUN–LENGTH	AMPLITUDE	CODE
EOB		10	1	16	0000000000010010s
0	1	1s (non i–picture)	1	17	0000000000010001s
0	1	11s (i–picture)	1	18	0000000000010000s
0	2	0100s	2	1	0101s
0	3	00101s	2	2	0000100s
0	4	0000110s	2	3	0000001011s
0	5	00100110s	2	4	000000010100s
0	6	00100001s	2	5	0000000010100s
0	7	0000001010s	3	1	00111s
0	8	000000011101s	3	2	00100100s
0	9	000000011000s	3	3	000000011100s
0	10	000000010011s	3	4	0000000010011s
0	11	000000010000s	4	1	00110s
0	12	0000000011010s	4	2	0000001111s
0	13	0000000011001s	4	3	000000010010s
0	14	0000000011000s	5	1	000111s
0	15	0000000010111s	5	2	0000001001s
0	16	00000000011111s	5	3	0000000010010s
0	17	00000000011110s	6	1	000101s
0	18	00000000011101s	6	2	000000011110s
0	19	00000000011100s	6	3	0000000000010100s
0	20	00000000011011s	7	1	000100s
0	21	00000000011010s	7	2	000000010101s
0	22	00000000011001s	8	1	0000111s
0	23	00000000011000s	8	2	000000010001s
0	24	00000000010111s	9	1	0000101s
0	25	00000000010110s	9	2	0000000010001s
0	26	00000000010110s	10	1	00100111s
0	27	00000000010100s	10	2	0000000010000s
0	28	00000000010011s	11	1	00100011s
0	29	00000000010010s	11	2	0000000000011010s
0	30	00000000010001s	12	1	00100010s
0	31	00000000010000s	12	2	0000000000011001s
0	32	000000000011000s	13	1	00100000s
0	33	000000000010111s	13	2	0000000000011000s
0	34	000000000010110s	14	1	0000001110s
0	35	000000000010101s	14	2	0000000000010111s
0	36	000000000010100s	15	1	0000001101s
0	37	000000000010011s	15	2	0000000000010110s
0	38	000000000010010	16	1	0000001000s
0	39	000000000010001s	16	1	0000000000010101s
0	40	000000000010000s	17	1	000000011111s
1	1	011s	18	1	000000011010s
1	2	000110s	19	1	000000011001s
1	3	00100101s	20	1	000000010111s
1	4	0000001100s	21	1	000000010110s
1	5	000000011011s	22	1	0000000011111s
1	6	0000000010110s	23	1	0000000011110s
1	7	0000000010111s	24	1	0000000011101s
1	8	000000000011111s	25	1	0000000011100s
1	9	00000000011110s	26	1	0000000011011s
1	10	00000000011101s	27	1	0000000000011111s
1	11	00000000011100s	28	1	0000000000011110s
1	12	000000000011011s	29	1	0000000000011101s
1	13	000000000011010s	30	1	0000000000011100s
1	14	000000000011001s	31	1	0000000000011011s
1	15	0000000000010011s	escape	1	000001s

s denotes sign: 1 for negative numbers, 0 for positive.
Note that there are two codes for the (0,1) pair depending whether the picture is an i–picture or not.

Table A.13: Escape Run–Length Codes	
RUN–LENGTH	CODE
0	00 0000
1	00 0001
2	00 0010
3	00 0011
...	...
63	11 1111

Table A.14: Escape Amplitude Codes	
AMPLITUDE	CODE
–255	1000 0000 0000 0001
...	...
–129	1000 0000 0111 1111
–128	1000 0000 1000 0000
–127	1000 0001
–126	1000 0010
...	...
–2	1111 1110
–1	1111 1111
1	0000 0001
2	0000 0010
...	...
126	0111 1110
127	0111 1111
128	0000 0000 1000 0000
129	0000 0000 1000 0001
...	...
254	0000 0000 1111 1110
255	0000 0000 1111 1111

4

Table A.15: I–Picture Macroblock Types						
MACROBLOCK TYPE CODE	MACROBLOCK TYPE NAME	NEW QUANTIZER	MOTION FORWARD	MOTION BACKWARD	BLOCK PATTERN (DCT CODED)	INTRA–CODED
1	intra–d	0	0	0	0	1
01	intra–q	1	0	0	0	1

Table A.16: P–Picture Macroblock Types						
MACROBLOCK TYPE CODE	MACROBLOCK TYPE NAME	NEW QUANTIZER	MOTION FORWARD	MOTION BACKWARD	BLOCK PATTERN (DCT CODED)	INTRA–CODED
1	pred–mc	0	1	0	1	0
01	pred–c	0	0	0	1	0
001	pred–m	0	1	0	0	0
00011	intra–df	0	0	0	0	1
00010	pred–mcq	1	1	0	1	0
00001	pred–cq	1	0	0	1	0
000001	intra–q	1	0	0	0	1

Table A.17: B–Picture Macroblock Types						
MACROBLOCK TYPE CODE	MACROBLOCK TYPE NAME	NEW QUANTIZER	MOTION FORWARD	MOTION BACKWARD	BLOCK PATTERN (DCT CODED)	INTRA–CODED
10	pred–i	0	1	1	0	0
11	pred–ic	0	1	1	1	0
010	pred–b	0	0	1	0	0
011	pred–bc	0	0	1	1	0
0010	pred–f	0	1	0	0	0
0011	pred–fc	0	1	0	1	0
00011	intra–d	0	0	0	0	1
00010	pred–icq	1	1	1	1	0
000011	pred–fcq	1	1	0	1	0
000010	pred–bcq	1	0	1	1	0
000001	intra–q	1	0	0	0	1

Table A.18: Motion Vector Range

FORWARD_F_CODE or BACKWARD_F_CODE	FULL_PEL_ FORWARD=0	FULL_PEL_ BACKWARD=1
1	–8 to 7.5	–16 to 15
2	–16 to 15.5	–32 to 31
3	–32 to 31.5	–64 to 63
4	–64 to 63.5	–128 to 127
5	–128 to 127.5	–256 to 255
6	–256 to 255.5	–512 to 511
7	–512 to 511.5	–1024 to 1023

Table A.19: Motion Vector Modulus

FORWARD_F_CODE or BACKWARD_F_CODE	MODULUS
1	32
2	64
3	128
4	256
5	512
6	1024
7	2048

Table A.20: Motion Vector Base Component Codes

CODE	VALUE	CODE	VALUE
1	0		
011	–1	010	1
0011	–2	0010	2
0001 1	–3	0001 0	3
0000 111	–4	0000 110	4
0000 1011	–5	0000 1010	5
0000 1001	–6	0000 1000	6
0000 0111	–7	0000 0110	7
0000 0101 11	–8	0000 0101 10	8
0000 0101 01	–9	0000 0101 00	9
0000 0100 11	–10	0000 0100 10	10
0000 0100 011	–11	0000 0100 010	11
0000 0100 001	–12	0000 0100 000	12
0000 0011 111	–13	0000 0011 110	13
0000 0011 101	–14	0000 0011 100	14
0000 0011 011	–15	0000 0011 010	15
0000 0011 001	–16	0000 0011 000	16

Table A.21: Code Block Pattern

CBP	B 1	B 2	B 3	B 4	B 5	B 6	CODE	CBP	B 1	B 2	B 3	B 4	B 5	B 6	CODE	CBP	B 1	B 2	B 3	B 4	B 5	B 6	CODE
60	1	1	1	1	0	0	111	5	0	0	0	1	0	1	0010 111	51	1	1	0	0	1	1	0001 0010
4	0	0	0	1	0	0	1101	9	0	0	1	0	0	1	0010 110	23	0	1	0	1	1	1	0001 0001
8	0	0	1	0	0	0	1100	17	0	1	0	0	0	1	0010 101	43	1	0	1	0	0	1	0001 0000
16	0	1	0	0	0	0	1011	33	1	0	0	0	0	1	0010 100	25	0	1	1	0	0	1	0000 1111
32	1	0	0	0	0	0	1010	6	0	0	0	1	1	0	0010 011	37	1	0	0	1	0	1	0000 1110
12	0	0	1	1	0	0	1001 1	10	0	0	1	0	1	0	0010 010	26	0	1	1	0	1	0	0000 1101
48	1	1	0	0	0	0	1001 0	18	0	1	0	0	1	0	0010 001	38	1	0	0	1	1	0	0000 1100
20	0	1	0	1	0	0	1000 1	34	1	0	0	0	1	0	0010 000	29	0	1	1	1	0	1	0000 1011
40	1	0	1	0	0	0	1000 0	7	0	0	0	1	1	1	0001 1111	45	1	0	1	1	0	1	0000 1010
28	0	1	1	1	0	0	0111 1	11	0	0	1	0	1	1	0001 1110	53	1	1	0	1	0	1	0000 1001
44	1	0	1	1	0	0	0111 0	19	0	1	0	0	1	1	0001 1101	57	1	1	1	0	0	1	0000 1000
52	1	1	0	1	0	0	0110 1	35	1	0	0	0	1	1	0001 1100	30	0	1	1	1	1	0	0000 0111
56	1	1	1	0	0	0	0110 0	13	0	0	1	1	0	1	0001 1011	46	1	0	1	1	1	0	0000 0110
1	0	0	0	0	0	1	0101 1	49	1	1	0	0	0	1	0001 1010	54	1	0	0	1	1	0	0000 0101
61	1	1	1	1	0	1	0101 0	21	0	1	0	1	0	1	0001 1001	58	1	1	1	0	1	0	0000 0100
2	0	0	0	0	1	0	0100 1	41	1	0	1	0	0	1	0001 1000	31	0	1	1	1	1	1	0000 0011 1
62	1	1	1	1	1	0	0100 0	14	0	0	1	1	1	0	0001 0111	47	0	0	1	1	1	1	0000 0011 0
24	0	1	1	0	0	0	0011 11	50	1	1	0	0	1	0	0001 0110	55	1	1	0	1	1	1	0000 0010 1
36	1	0	0	1	0	0	0011 10	22	0	1	0	1	1	0	0001 0101	59	1	1	1	0	1	1	0000 0010 0
3	0	0	0	0	1	1	0011 01	42	1	0	1	0	1	0	0001 0100	27	0	1	1	0	1	1	0000 0001 1
63	1	1	1	1	1	1	0011 00	15	0	0	1	1	1	1	0001 0011	39	1	0	0	1	1	1	0000 0001 0

The code block pattern field, CBP, is a code that when decoded gives a bit–field that specifies which blocks of a macroblock have index coding information present in the bit stream. The most significant bit of the decoded 6–bit value specifies whether block 1 is coded. The next bit specifies if block 2 is coded, ... and so on. Blocks that are not coded are assumed to consist of all 0's.

Bibliography

[1] A Proposal for MPEG Video Report, Rev 1 Brian Astle, Aug, 14 1991
[2] The MPEG Video Compression Algorithm Didier J. Le Gall, Signal Processing: Image Communication, Vol 4, Issue 2, p 129–140
[3] C–Cube Microsystems CL450 MPEG Video Decoder User's Guide, Chapter 2 MPEG Overview
[4] ISO/IEC 11172–2 Coding of Moving Pictures and Associated Audio.. for Digital Storage Media at up to About 1.5 Mbits.

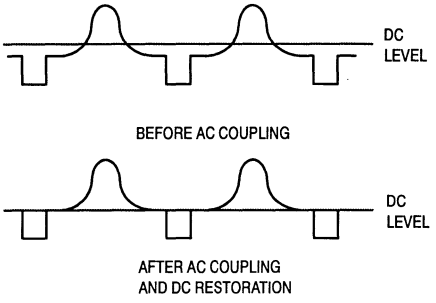
Glossary

5

Glossary of Terms and Abbreviations

The list contains terms found in this and other Motorola publications concerned with Motorola Semiconductor products for Multimedia.

AC Coupled — AC coupling is a method of connecting a video signal to any circuit in a way that removes the dc offset, or the overall voltage level that the video signal "rides" on.



You can see in the figure that not knowing the dc offset means that we don't know exactly where the video signal is. One way to find the signal is to remove the dc offset by ac coupling, and then do dc restoration to add a known dc offset (one that we selected). Another reason ac coupling is important is that it can remove harmful dc offsets.

Active Video — The video waveform on a display screen that is actually visible.

A/D (analog-to-digital) converter (ADC) — A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of them exclusively representing a fractional part of the total analog input range.

Aliasing Noise — A distortion component that is created when frequencies present in a sampled signal are greater than one-half the sample rate.

Alpha —See Alpha Channel and Alpha Mix.

Alpha Channel — The alpha channel is used to specify an alpha value for each color pixel. The alpha value is used to control the blending, on a pixel–by–pixel basis, of two images.

new pixel = (alpha)(pixel A color) + (1–alpha)(pixel B color)

Alpha typically has a normalized value of 0 to 1. In a computer environment, the alpha values can be stored in additional bit planes of frame–buffer memory. When you hear about 32–bit frame buffers, what this really means is that there are 24 bits of color, 8 each for red, green, and blue, along with an 8–bit alpha channel. Also see Alpha Mix.

Alpha Mix — This is a way of combining two images. how the mixing is performed is provided by the alpha channel. The little box that appears over the left–hand shoulder of a news anchor is put there by an alpha mixer. Wherever the pixels of the little box appear in the frame buffer, an alpha number of 1 is put in the alpha channel. Wherever they don't appear, an alpha number of 0 is placed. When the alpha mixer sees a 1 coming from the alpha channel, it displays the little box. Whenever it sees a 0, it displays the news anchor. Of course, it doesn't matter if a 1 or a 0 is used, but you get the point.

Anti-aliasing Filter — A filter (normally low pass) that band limits an input signal *before* sampling to prevent aliasing noise.

Aperture Delay — Aperture delay is the time from an edge of the input clock of the ADC until the time the part actually takes the sample. The smaller this number, the better.

Aperture Jitter — The uncertainty in the aperture delay. This means the aperture delay time changes a little bit over time, and that little bit of change is the aperture jitter.

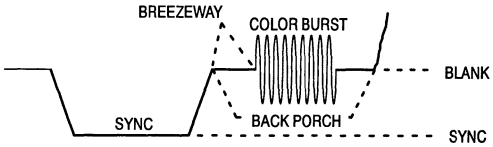
Artifacts — In the video domain, artifacts are blemishes, noise, snow, spots, whatever. When you have an image artifact, something is wrong with the picture from a visual stand point. Don't confuse this term with not having the display properly adjusted. For example, if the hue control is set wrong, the picture will look bad, but this is not an artifact. An artifact is some physical disruption of the image.

Aspect Ratio — The ratio of the width of the display screen to the height. For most current TV sets, this ratio is 4:3. For HDTV, the ratio will be 16:9. The aspect ratio, along with the number of vertical scan lines that make up the image, determines what sample rate should be used to digitize the video signal.

Asynchronous — A mode of data transmission in which the time occurrence of the bits within each character or block of characters relates to a fixed time frame, but the start of each character or block of characters is not related to this fixed time frame.

Authoring Platform — A computer that has been outfitted with the right hardware for creating material to be viewed in a multimedia box. The video quality of the authoring platform has to be high enough that the playback equipment is the limiting factor.

Back Porch — The area of the video waveform between the rising edge of the horizontal sync and right before the active video.



Bandwidth — The information-carrying frequencies between the limiting frequencies of a communication line or channel.

Baud — A unit of signaling speed equal to the number of discrete signal conditions or events per second. This refers to

the physical symbols/second used within a transmission channel.

Bit–Blt — Pronounced "bit blit," this is short for Bit–Boundary Block Transfer. This is an operation in which one area of the frame buffer is copied to another area of the frame buffer, generally the areas are rectangular and the pixels are copied from their original locations to corresponding locations in the new area.

Bit Rate — The speed at which data bits are transmitted over a communication path, usually expressed in bits per second. A 9600 bps terminal is a 2400 baud system with 4 bits/baud.

Black Burst — Black burst is the video waveform without the active video part. Black burst is used to sync video equipment together so that video output is aligned. Black burst tells the video equipment the vertical sync, horizontal sync, and the chroma burst information.

Black Level — This level represents the darkest an image can get. This defines what black is for the particular image system. If for some reason the video dips below this level, it is referred to as blacker–than–black. You could say that sync is blacker–than–black.

Blanking — On the screen, the scan line moves from the left edge to the right edge, jumps back to the left edge, and starts out all over again, on down the screen. When the scan line hits the right–hand limit and is about to be brought back to the left–hand edge, the video signal is blanked so that you can't "see" the return path of the scan beam from the right to the left–hand edge. To blank the video signal, the video level is brought down to the blanking level, which may or may not be the black level if a pedestal is used.

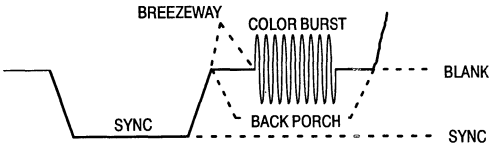
Blanking Level — That level of the video waveform defined by the system to be where blanking occurs. This could be the black level if a pedestal is not used or below the black level if a pedestal is used.

Blit — This is short for bit–blit, which is short for bit–boundary black transfer.

Blitter — A blitter is a circuit or device that does blitting. see Bit–Blit.

Blooming — This is an effect, sometimes caused when video becomes whiter–than–white, in which a line that is supposed to be nice and thin becomes fat and fuzzy on the screen.

Breezeway — That portion of the video waveform between the rising edge of the horizontal sync and the start of color burst.



Brightness —This is the intensity of the video level and refers to how much light is emitted by the display.

Burst — See color burst.

Burst Gate — This is a signal that tells the system where the color burst is located within the scan line.

CCIR 601 — This is the recommendation developed by the International Radio Consultative Committee Recommendation for digitization of color video signals. The recommendation deals with four areas: 1.) the RGB to YCrCb color space conversion, 2.) the bandwidth limits for the digital filters, 3.) the sample rate (defined as 13.5 MHz), and 4.) the horizontal resolution (720 active pixels).

Chroma or Chrominance — The combined color information in a video signal. This term is often used when referring to the color difference signals.

Chroma Bandpass — In an NTSC or PAL video source the luminance (black and white) and the chrominance (color) information are combined together. If you want to decode an NTSC or PAL video signal, the luminance and chrominance must be separated. The chroma bandpass filter removes the luminance from the video signal, leaving the chrominance relatively intact. This works reasonably well except in certain images where the luminance information and chrominance information overlap, meaning that we have luminance and chrominance stuff at the same frequency. the filter can't tell the difference between the two and passes everything within a certain area. If there is luminance in that area, it's let through too. This can make for a funny–looking picture. Next time you're watching TV and someone is wearing a herringbone jacket or a shirt with thin, closely spaced stripes, take a good look. You'll see a rainbow color effect moving through that area. What's happening is that the chroma demodulator thinks the luminance is chrominance. Since the luminance isn't chrominance, the TV can't figure out what color it is and it shows up as a rainbow pattern. This problem can be overcome by using a comb filter.

Chroma Burst — See Color Burst.

Chroma Demodulator — After the NTSC or PAL video source makes its way through the Y/C separator, by either the chroma bandpass, chroma trap, or comb filter method, the colors must be decoded. That's what a chroma demodulator does. It takes the chrominance output of the Y/C separator and recovers two color difference signals (typically I and Q or U and V0. To do this, the chroma demodulator uses the color subcarrier. Now, with the luminance information and color difference signals, the video system can figure out what colors to put on the screen.

Chroma Key — This is a method of combining two video images. An example of chroma keying in action is the nightly news weatherman standing in front of a giant weather map. In actuality, the weatherman is standing in front of a solid, bright–blue background and his (or her) image is projected on top of the computer–generated map. This is how it works: a TV camera is pointed at the person or object that you want to project on top of the artificial background (e.g., the weather map). The background doesn't actually have to be artificial. It can be another real image–it doesn't really matter. As mentioned, our imaginary weatherman is standing in front of a bright–blue background. This person and bright–blue background image is fed along with the image of the artificial background into a box. Inside the box, a decision is made. Wherever it sees the bright–blue background, it displays the artificial background. Wherever it does not see bright blue,

it shows the original image. So, whenever the weatherman moves around, he's moving around in front of the bright–blue background. The box figures out where he is and where he isn't, and displays the appropriate image.

Chroma Trap — In an NTSC or PAL video source the luminance (black and white) and the chrominance (color) information are combined together. If you want to decode the video signal, the luminance and chrominance must be separated. The chroma trap is s method for separating the chrominance from the luminance, leaving the luminance relatively intact. How does this work? The NTSC or PAL signal is fed to a bandstop filter. For all practical purpose, a bandstop filter allows some types of information (actually certain frequencies) to pass through but not others. The bandstop filter is designed with a response, or stop, to remove the chrominance so that the output of the filter only contains the luminance. Another name for a bandstop filter is a trap. Since this trap stops chrominance, it's called a chroma trap. The sad part about all of this is that not only does the filter remove chrominance, it removes luminance as well if it exists within the region where the stop exists. The filter only knows ranges and, depending on the image, the luminance information may overlap the chrominance information. The filter can't tell the difference between the luminance and chrominance, so it stops both when they are in the same range. What's the big deal? Well, you lose luminance and and this means that the picture is degraded somewhat. Using a comb filter for a Y/C separator is better than a chroma trap or chroma bandpass. See the chroma bandpass and the Y/C separator definitions.

Chrominance — The NTSC or PAL video signal contains two pieces that make up what you see on the screen: the black and white (luminance) part, and the color part. Chrominance is the color part – a.k.a. chroma.

CIF — CIF is short for Common Interchange Format. This allows computerized video images to be shared between computers. An image that is digitized to CIF format has a resolution of 352x288 or 352x240, which is essentially one–half of CCIR 601.

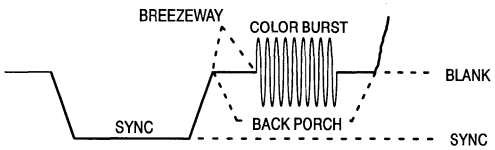
Clamp — This is basically another name for the dc–restoration circuit. It can also refer to a switch used within the dc–restoration circuit. When it means dc restoration, then it's usually used as clamping. When it's the switch, then it's just clamp.

Clipping Logic — A circuit used to prevent illegal conversion. Some colors can exist in one color space but not in another. Right after the conversion from one color space to another, a color space converter might check for illegal colors. If any appear, the clipping logic is used to chop off, or clip, part of the information until a legal color can be represented. Since this circuit clips off some information and is built using logic, it's not too hard to see how the name "clipping logic" was developed.

CMYK — This is a color space primarily used in printing. CMYK is an acronym for Cyan, Magenta, Yellow, and blacK. The CMYK color space is subtractive, meaning that cyan, magenta, yellow, and black pigments or inks are applied to a white surface to remove color information from the white surface to create the final color. Remember, white light contains all of the colors of the spectrum; that's why it's used in printing. They deal with a white surface, or almost white. The reason black is used is because even if a printer could put down hues of cyan, magenta, and yellow inks perfectly enough to make black (which it can't for large areas), it would be too expensive since colored inks cost more than black inks. So, when black has to be made, instead of putting down a lot of CMY, they just use black. So, what is a print term doing here? The reason is that a lot of color systems are being hooked up to color printers. The display screen uses RGB but the printer uses CMYK. A color space conversion needs to be performed for true WYSIWYG (wizzy–wig – what you see is what you get) performance in a color system that has a printer.

Color Bars — This is a test pattern used to check whether a video system is calibrated correctly. A video system is calibrated correctly if the colors are the correct brightness, hue, and saturation. This can be checked with a vectorscope, or by looking at the RGB levels.

Color Burst — That portion of the video waveform that sits between the breezeway and the start of active video. The color burst tells the color decoder how to decode the color information contained in that line of active video. By looking at the color burst, the decoder can determine what's blue, orange, or magenta. Essentially, the decoder figures out what the correct color is. If you've ever seen a TV picture in which the colors were just not right, a reason might be that the TV can't find the color burst and doesn't know how to make the correct color.



Color Decoder — This is the circuit in the video system that uses the chrominance portion of NTSC/PAL to derive the two color difference signals. The color decoder sits right after the Y/C separator and before the color space converter. The color decoder needs a 3.58 MHz (NTSC) or 4.43 MHz (PAL) signal that is accurately phase–locked to the color burst. If it isn't locked well enough, then the color decoder can't figure out the right colors. Also called a chroma demodulator.

Color Demodulator — See Color Decoder and Chroma Demodulator.

Color Difference — All of the color spaces used in color video require three components. These might be RGB, YIQ, YUV, or Y(R–Y)(B–Y). In the Y(R–Y)(B–Y) color space, the R–Y and B–Y components are often referred to as color difference signals for obvious reasons. They are made by subtracting the luminance (Y) from the red and blue components. I and Q and U and V are also color difference signals since they are scaled versions of R–Y and B–Y. All the Ys in each of the YIQ, YUV, and Y(R–Y)(B–Y) are basically the same.

Color Encoder — The color encoder does the exact opposite of the color decoder. It takes the two color difference signals, such as I and Q or U and V, and combines them into the chrominance signal. The color encoder, or what may be referred to as the color modulator, uses the color subcarrier to do the encoding.

Color Modulator — Take a look at the color encoder definition.

Color Key — This is essentially the same thing as chroma key.

Color Killer — A color killer is a circuit that shuts off the color decoder in a video system if the incoming video does not contain color information. How does this work? The color killer looks for the color burst and if it can't find it, it shuts off the color decoder. For example, let's say that a color TV is going to receive material recorded in black and white. Since the black and white signal does not contain a color burst, the color decoder is shut off. why is a color killer used? Well, in the old days, the color decoder would still generate a tiny little bit of color if a black and white transmission was received, due to small errors in the color decoder, causing a black and white program to have faint color spots throughout the picture.

Color Purity — This term is used to describe how close a color is to the theoretical. For example, in the YUV color space, color purity is specified as a percentage of saturation and ± 0, where 0 is an angle in degrees, and both quantities are referenced to the color of interest. the smaller the numbers, the closer the actual color is to the color that it's really supposed to be. for a studio–grade device, the saturation is ± 2% and the hue is ± 2%. On a vectorscope, if you're in that range, you're studio grade.

Color Space — A color space is a mathematical representation for a color. No matter what color space is used – RGB, YIQ, YUV, etc. – orange is still orange. What changes is how you represent orange in an imaging system. For example, the RGB color space is based on a Cartesian coordinate system and the HSI color space is based on a polar coordinate system.

Color Subcarrier — The color subcarrier is a clock signal used to run the color encoder or color decoder. For NTSC the frequency of the color subcarrier is 3.58 MHz and for PAL it's 4.43 MHz. In the color encoder, a portion of the color subcarrier is used to create the color burst, while in the color decoder, the color burst is used to reconstruct the color subcarrier.

Comb Filter — This is another method of performing a Y/C separator. A comb filter is used in place of a chroma bandpass or chroma trap. The comb filter provides better video quality since it does a better job of separating the luminance from chrominance. It reduces the amount of creepy–crawlies or zipper artifacts. It's called a comb filter because the frequency response looks like a comb. The important thing to remember is that the comb filter is a better method for Y/C separation than chroma bandpass or chroma trap.

Compact Disk Interactive (CD–i) — This a dedicated box similar to any other consumer audio or video equipment, as opposed to a PC with special designed hardware. CD–i uses a proprietary image and audio compression scheme, that will support JPEG and MPEG in the future.

Comparator — This is a circuit or functional block that is a basic component of flash ADCs. A comparator has two inputs, X and Y, along with one output, which we will call Z. The comparator implements the following mathematical function:

If A – B > 0, then Z = 1
If A – B < 0, then Z = 0

What does this mean? A comparator "compares" A to B. If A is larger than B, the output of the comparator is a 1. If A is smaller the B, then the output is a 0. If A=B, the output Z may be undefined and oscillate between 1 and 0 wildly until that condition is removed, it may be a 1, or it may be a 0. It depends on how the comparator was designed.

Composite Video (NTSC or PAL) — The most commonly available video source. The three primary signals, the red, the green, and the blue (RGB), are encoded into one signal. This signal carries all horizontal and vertical timing information as well as the video information. The video information is encoded as three components within the composite video signal. A color reference signal called the color burst is transmitted on the back porch of the horizontal blanking pulse. the luminance signal is present during the video display period of the composite video signal. The two color difference signals are used to quadrature modulate a 3.579545 MHz subcarrier. The subcarrier frequency is suppressed to prevent distortion, and the subcarrier information is transmitted by the color burst. What remains during the video display interval (about 50 µs per line), is the luminance information and the color difference information in the form of upper and lower sidebands of the quadrature suppressed carrier. All video cassette recorders, laser disk players, and cameras, as well as some television receivers, provide composite video output. Picture quality is roughly equal to that of television, about 300 lines resolution in the horizontal direction.

Compression Ratio — Compression ratio is a number used to tell how much information is squeezed out of an image when it has been compressed. For example, suppose we start with a 1 Mbyte image and compress it down to 128 Kbytes. The compression ratio would be:

1,048,576 = 8
131,072 = 1

This represents a compression ratio of 8:1; 1/8 of the original amount of storage is now required. For a given compression technique – MPEG, for example – the higher the compression ratio, the worse the image looks. This has nothing to do with which compression method is better, for example JPEG vs. MPEG. Rather, it depends on the application. A video stream that is compressed using MPEG at 100:1 may look better than the same video stream compressed to 100:1 using JPEG.

Contouring — This is an image artifact caused by not having enough bits to represent the image. The reason the effect is called contouring is because the image develops lines that look like a geographical contour map. In a black–and–white imaging system, contouring may be noticed a 6 bits per pixel or less, while in a color system it may be 18 bits per pixel or less.

Contrast — A video term referring to how far the whitest whites are from the blackest blacks in a video waveform. If the peak white is far away from the peak black, the image is said to have high contrast. With high contrast, the image is very stark and very "contrasty," like a black–and–white tile floor. If the two are very close to each other, the image is said to have poor, or low, contrast. With poor contrast, an image may be referred to as being "washed out"– you can't tell the difference between white and black, and the image looks gray.

Creepy–Crawlies — Yes, this is a real video term! Creepy–crawlies refers to a specific image artifact that is a result of the NTSC system. When the nightly news is on, and a little box containing a picture appears over the anchorperson's shoulder, or when some computer–generated text shows up on top of the video clip being shown, get up close to the TV and check it out. Along the edges of the box, or along the edges of the text, you'll notice some jaggies "rolling" up (could be down) the picture. that's the creepy–crawlies. Some people refer to this as zipper because it looks like one.

D1 — This is a storage and tape format standard for very high–end digital video tape decks, although commonly used to refer to the CCIR 601 digital video format. D1 video tape decks use digital component video (CCIR 601) for getting digital video into and out of the tape deck.

D2, D3 — These are storage and tape format standards for medium–to high–end digital video tape decks, although commonly used to refer to the digital composite video format. D2 and D3 video tape decks use digital composite video for getting digital video into and out of the tape deck.

D/A (digital-to-analog) converter (DAC) — A converter that represents a limited number of different digital input codes by a corresponding number of discrete analog output values.

Data Compression — A technique that provides for the transmission of fewer data bits than originally required without information loss. The receiving location expands the received data bits into the original bit sequence.

dB (decibel) — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

10 x log (P1/P2) for power measurements, and

20 x log (V1/V2) for voltage measurements.

DCT — This short for Discrete Cosine Transform, used in image compression algorithms such as JPEG and MPEG. An image is viewed in the frequency domain rather than the time domain.

Decimation — When a video waveform is digitized so the 100 pixels are produced, but only every other one is stored or used, the video waveform is decimated by a factor of 2:1. The image is now 1/4 of its original size, since 3/4 of the data is missing. If only one out of five pixels were used, then the image would be decimated by a factor of 5:1, and the image would be 1/25 its original size. decimation, then, is quick–and–easy method for image scaling and is in fact the method used by low–cost systems that scale video into a window.

Decimation can be performed in several ways. One way is the method just described, where data is literally thrown away. even though this technique is easy to implement and cheap to build, it generally introduces image artifacts unacceptable to medium–to high–end customers. another method is to use a decimation filter. This reduces the image artifacts to an acceptable level by smoothing them out, but is more costly to implement than the method of just throwing data away.

Decimation Filter — Since you probably read the preceding definition of decimation, this one should be easy. a decimation filter is a filter designed to provide decimation without the artifacts associated with throwing data away (the method of throwing data away is the example described in the decimation definition).

Decoding — A process in which one of a set of reconstructed analog samples is generated from the digital character signal representing a sample.

Demodulator — In video, demodulation is the technique used to recover the color difference signals in NTSC or PAL systems. See the definitions for chroma demodulator and color decoder; those are two other names for a demodulator used in a video application.

Differential Gain — Differential gain is how much the color saturation changes when the luminance level changes (it isn't supposed to). The result on the screen will be incorrect color saturation. For a video system, the better the differential gain–that is, the smaller the number specified–the better the system is at figuring out the correct color.

Differential Phase — Differential phase is how much the hue changes when the luminance level changes (it isn't supposed to). The result on the screen will be incorrect colors. For a video system, the better the differential phase—that is, the smaller the number specified—the better the system is at figuring out the correct color.

Digital Component Video — Digital video using separate color components, such as YCrCb or RGB. See CCIR 601. Sometimes incorrectly referred to as D1.

Digital Composite Video —Digital video that is essentially the digitized waveform of composite NTSC or PAL video signals, with specific digital values assigned to the sync, blank, and white levels. Sometimes incorrectly referred to as D2 or D3.

Digital Video Interactive (DVI) — DVI is a multimedia system being marketed by Intel. It is not just an image–compression scheme, but includes everything that is necessary to implement a multimedia playback station. Intel's DVI offering is represented by chips, boards, and software. DVI currently uses a proprietary image and audio compression scheme, with JPEG and MPEG being supported in the future.

Discrete Cosine Transform (DCT) — A DCT is just another way to represent an image. Instead of looking at it in the time domain—which, by the way, is how we normally do it—it is viewed in the frequency domain. It's analogous to color spaces, where the color is still the color but is represented differently. Same thing applies here-the image is still the image, but it is represented in a different way.

Why do JPEG and MPEG base part of their compression schemes on the DCT? Because it is more efficient to represent an image that way. In the same way that the YCrCb color space is more efficient than RGB in representing an image, the DCT is more efficient at image representation.

Discrete Time Oscillator (DTO) — A discrete time oscillator is a digital version of the voltage–controlled oscillator.

Double Buffering — As the name implies, you need two buffers—for video, this means two frame buffers. While one of the buffers is being displayed, the other buffer is operated on by a filter, for example. When the filter is finished, the buffer that was just operated on is displayed while the first buffer is now operated on. This goes back and forth. Since the buffer

that contains the correct image (already operated on) is always displayed, the viewer does not see the operation being performed and just sees a perfect image all the time.

Distortion — The failure to reproduce an original signal's amplitude, phase, delay, etc. characteristics accurately.

Encoder (PCM) — A device that performs repeated sampling, compression, and A/D conversion to change an analog signal to a serial stream of PCM samples representing the analog signal.

Equalization Pulses — These are two groups of pulses, one that occurs before the serrated vertical sync and another group that occurs after. These pulses happen at twice the normal horizontal scan rate. They exist to ensure correct 2:1 interlacing in early televisions.

Fade — Fading is a method of switching from one video source to another. Next time you watch a TV program (or a movie), pay extra attention when the scene is about to end and go on to another. The scene fades to black, then a fade from black to another scene occurs. Fading between scenes without going to black is called a dissolve. One way to do a fade is to use an alpha mixer.

Field — One half of a complete television picture or frame composed of alternate scan lines. Even fields are composed of lines 2, 4, 6, etc., and the odd fields are composed of lines 1, 3, 5, etc. The field frequency is the same as the vertical scan rate. This method of interlacing fields to produce the television picture was implemented to obtain a display of minimum flicker without overtaxing the technology of the day.

Filter — In general, a filter is used to remove unwanted material from a signal. If you have some high frequencies, such as noise, in with the signal that you really want, then a lowpass filter is used. a lowpass filter "passes" frequencies below a certain point and stops frequencies above that same point. A highpass filter does just the opposite—it stops low frequencies and passes the high frequencies. A bandpass filter lets through frequencies within a certain range or band, but stops frequencies outside of the band.

Finite Impulse Response (FIR) Filter — This definition won't teach you how to design one of these, but will at least get you the basic information. An FIR filter is a type of digital filter. FIRs can be any type, such as lowpass, highpass or bandpass. Digital filters in general are much better than analog filters. Sometimes the only way to design a very high–quality filter is with an FIR–it would be impossible to design using analog components. An FIR filter is very, very good, it's digital, and it's somewhat expensive to build.

Flash A/D — A really fast method for digitizing something. the signal to be digitized is provided as the source for one input of a whole bank of comparators. The other input is tied to a tap of a resistor ladder, with each comparator tied to its own tap. This way, when the input voltage is somewhere between the top and bottom voltages connected to the ladder, the comparators output a thermometer code. This means that all the comparators output a "yes" up to the input voltage and a "no" above that. The ADC then takes this string of yes's and no's and converts them into a binary number which tells where the yes's turned into no's. See the definition of resistor ladder for more details, if you're interested.

Flicker — Flicker occurs when the refresh rate of the video is too low. It's the same effect produced by an old fluorescent light fixture. in order for flicker to disappear, the update rate, or the video frame rate, must be at least 24 scene changes (frames) per second. This is fast enough so that the eyeball can't keep up with the individual frames. The two problems with flicker are that it's distracting and tiring to the eyes.

Frame — A frame of video is essentially one picture or "still" out of a video stream. in NTSC, a frame of video is made up of 525 individual scan lines. For PAL and SECAM, it's 625 scan lines. If you get up close to you TV screen, you'll be able to see the individual lines that make up the picture. After 525 lines are painted on the screen the next frame appears; then after that one, the next, and so on. By playing these individual frames fast enough, it looks like people are "moving" on the screen. It's the same principle as flip cards, cartoons, and movies.

Frame Buffer — A frame buffer is a big bunch of memory, used to hold the image for the display. How much memory are we talking about? well, let's assume a horizontal resolution of 640 pixels and 480 scan lines, and we'll use the RGB color space. This works out to be:

640 x 480 x 3 = 921,600 bytes or 900 Kbytes

So, 900 Kbytes are needed to store one frame of video at that resolution.

Frame Rate — The frame rate of a video source is how fast the source repaints the screen with a new frame. For example, with the NTSC system, the screen is repainted once every 30th of a second for a frame rate of 30 frames per second. For PAL, the frame rate is 25 frames per second. For some computer and workstation displays, the frame rate can reach 70 to 75 frames per second.

Frame Rate Conversion — Frame rate conversion is the act of converting one frame rate to another. One real example that poses a difficult problem is that the frame rate of NTSC, 30 frames per second, is different from a typical computer's display, which may be anywhere from 70 to 75 frames per second (or Hz if you prefer). Therefore, some frame–rate conversion process must be performed before NTSC video can be shown correctly on a computer display. Without frame rate conversion, the screen might look as if it "stalls" every now and then. If there is motion within the video, the objects that are moving might appear cut in half.

Front Porch — The video waveform area that is between the start of horizontal blank and the falling edge (start of) horizontal sync.

Gain — The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

Gain Tracking Error — The variation of gain from a constant level (determined at 0 dBm input level) when measuring the dependence of gain on signal level by comparing the output signal to the input signal over a range of input signals.

Gamma — The characteristics of the displays using phosphors (as well as some cameras) are nonlinear. A small change in voltage when the voltage level is low produces a change in the output display brightness level, but this same

small change in voltage at a high voltage level will not produce the same magnitude of change in the brightness output. This effect, or actually the difference between what you should have and what you actually measured, is known as gamma.

Gamma Correction — Computers like to number crunch on linear RGB data. Before being displayed, this linear RGB data must be processed (gamma corrected) to compensate for the gamma of the display.

Genlock – The video signal that provides all the necessary information for a decoder to reconstruct a picture. Included are brightness, color, and also timing information. To properly decode the video signal, the decoder must be "genlocked" to the video signal. The decoder looks at the color burst of the video signal and reconstructs the original color subcarrier that was used by the encoder. This is needed to properly decode the color information. The decoder also generates a pixel clock (done by looking at the sync information within the video signal) that was the same as the pixel clock used by the encoder. The pixel clock is used to clock pixel data out of the decoder into a memory for display or into another circuit for processing. the circuitry within the decoder that does all of this work is called the genlock circuit. Although it sounds simple, the genlock circuit must be able to handle very bad video sources, such as the output of VCRs. In reality, the genlock circuit is the most complex section of a video decoder.

Gray Scale — The term gray scale has several meanings. In some instances it means the luminance component of the NTSC, PAL, or SECAM signals. In other cases it means a black–and–white video signal.

H.261 — The video compression standard that was developed for video teleconferencing. This standard will allow one videophone to "talk" to another videophone, much like two FAX machines are able to "talk" to one another.

Hi–8 — Hi–8 is a videotape format that uses an 8mm wide tape. It provides better image quality than VHS.

High–Definition Television (HDTV) — This term describes several advanced standards proposals to allow high–resolution TV to be received in the home.

Horizontal Scan Rate — This is how fast the scanning beam in a display or a camera is swept from side to side. in the NTSC system this rate is 63.556 ms, or 15.734 kHz. that means the scanning beam in you home TV moves from side to side 15,734 times a second.

Horizontal Sync — This is the portion of the composite video signal that tells the receiver where to place the image in the left–to–right dimension. The horizontal sync pulse tells the receiving system where the beginning of the new scan line is. Check to see if you TV at home has a horizontal hold control. If it does, give it a twist and observe what happens. When the picture rolls around like that, it's demonstrating what the picture would look like if there weren't any horizontal sync, or if the receiver couldn't find it.

HSI — HSI stands for hue, saturation, and intensity. It is a color space used to represent images. HSI is based on polar coordinates, while the RGB color space is based on a three–dimensional Cartesian coordinate system. The intensity, analogous to luminance, is their vertical axis of the polar system. The hue is the angle and the saturation is the distance out from the axis. HSI is more intuitive to manipulate colors as opposed to the RGB space. For example, in the HSI space, if you want to change red to pink, you decrease the saturation. In the RGB space, what would you do? My point exactly. In the HSI space, if you wanted to change the color from purple to green, you would adjust the hue. Take a guess what you would have to do in the RGB space. However, the key thing to remember, as with all color spaces, is that it's just a way to represent a color—nothing more, nothing less.

HSL — This is similar to HSI, except that HSL stands for hue, saturation and lightness.

HSYNC — Check out the horizontal sync definition.

HSV — This is similar to HSI, except that HSV stands for hue, saturation and value.

Hue — In technical terms, hue refers to the wavelength of the color. That means that hue is the term used for the base color—red, green, yellow, etc. Hue is completely separate from the intensity of the saturation of the color. For example, a red hue could look brown at low saturation, bright red at a higher level of saturation, or pink at a high brightness level. All three "colors" have the same hue.

Huffman Coding — Huffman coding is a method of data compression. It doesn't matter what the data is—it could be image data, audio data, or whatever. It just so happens that Huffman coding is one of the techniques used in JPEG and MPEG to help with the compression. This is how it works. First, take a look at the data that needs to be compressed and create a table that lists how many times each piece of unique data occurs. now assign a very small code word to the piece of data that occurs next most frequently. This continues until all of the unique pieces of data are assigned unique code words of varying lengths. The idea is that data that occurs most frequently is assigned a small code word, and data that really occurs is assigned a long code word, resulting in spacer savings.

Hypermedia — Since the term multimedia is slightly overused, some people use the term hypermedia instead. Essentially, hypermedia is just another name for multimedia and will soon be overused, to be replaced with something else.

I²C — A two wire communication port and protocol often are used to reduce the number of required interface pins. any amount of information can flow through the interface, and is limited only by the internal complexity of the devices. I²C ports are ideal for control signals because of their relatively slow speed.

Illegal Video — Some colors that exist in the RGB color space can't bed represented in the video domain. For example, 100% saturated red in the RGB space (which is the red color on full strength and the blue and green colors turned off) can't exist in the NTSC video signal, due to color bandwidth limitations. The NTSC encoder must be able to determine that an illegal color is being generated and stop that from occurring, since it may cause over–saturation and blooming.

Image Buffer — For all practical purposes, an image buffer is the same as a frame buffer. An image is acquired by the computer and stored in the image buffer. Once it is in the image buffer, it can typically be annotated with text or graphics

or manipulated in some way, just like anything else in a frame buffer.

Image Compression — Image compression is used to reduce the amount of memory required to store an image. For example, an image that has a resolution of 640x480 and is in the RGB color space a 8 bits per color, requiring 900 Kbytes of storage. If this image can be compressed at a compression ratio of 20:1, then the amount of storage required is only 45 Kbytes. There are several methods of image compression, but the most popular will be JPEG and MPEG as they become the accepted standards. H.261 is the image compression standard to be used by video telephones.

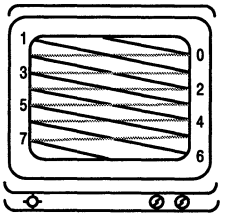
Improved Definition Television (IDTV) — IDTV (also called enhanced definition television or EDTV) is different from HDTV. IDTV is a system that improves the display of NTSC or PAL systems by adding processing in the receiver; standard NTSC or PAL signals are transmitted. HDTV is a radical departure from NTSC or PAL. Some people think IDTV is just a stepping stone to HDTV, while others think that if IDTV is good enough, HDTV will not be required.

Input Level — For flash ADCs, the input level is the voltage range required of the input video for proper operation of the part. For example, if the required input level for an 8–bit ADC is 0 to 10 V, then an input voltage level of 0 V is assigned the code 0 and an input voltage of 10 V is assigned the code 255. It is important that the voltage range of the input signal matches that of the ADC. Let's take a case where the voltage range of the signal is 0 V to 5 V and the ADCs input rage is 0 V to 10 V. When the input level is 0 V, the output of the ADC will be the number 0, and when the input signal is at its maximum of 5 V, the output of the ADC will be 127. In this example, one–half of the ADC is wasted because the numbers 128 through 255 can't be generated since the input level of the source never gets high enough. The problem exists in the other direction also. let's take and example where the input voltage level has the rage of 0 V to 10 V, but the input rage of the ADC is only 0 V to 5 V. When the input level is 0 V, the output of the ADC will be the number 0, but when the input signal is in the range of 5 V to 10 V, the output of the ADC will be stuck at 255, since the input is outside of the range for the ADC.

Intensity — This is the same thing as brightness.

Interlaced — An interlaced raster system is one where two (in general—it could be more, but we'll stick with two) interleaved fields are used to scan out one video frame. Therefore, the number of lines in a field are one–half of the number of lines in a frame. In NTSC, there are 262.5 lines per field (525 lines per frame) while there are 312.5 lines per field in PAL. The two fields are interlaced, which means that all of the odd–numbered lines are contained in one field, while the other field is made up of all the even–numbered lines. In NTSC, PAL and SECAM, every other scan line belongs to the same field. Each field is drawn on the screen consecutively—first one field, then the other.

Why did the creators of video decide to go with an interlaced system? It has to do with frame rate. A large TV screen that was updated at 30 frames per second would flicker, meaning that the image would begin to fade away before the next one was drawn on the screen. By using two fields, each containing one–half of the information that makes up the frame and each field being drawn on the screen consecutively, the field update rate is 60 fields per second. At This update rate, the eye blends everything together into a smooth, continuous motion.



Interlace: field 1 (lines 1, 3, 5, 7) is scanned, then field 2 (lines 0, 2, 4, 6).

Intermodulation — The modulation of the components of a complex wave by each other (in a nonlinear system).

Intermodulation Distortion — An analog line impairment when two frequencies interact to create an erroneous frequency, in turn distorting the data signal representation.

Interpolation — Interpolation is a mathematical way of regenerating missing or needed information. Let's say that an image needs to be scaled up by a factor of two, from 100 pixels to 200 pixels. We can do this by interpolation. The missing pixels are generated by interpolating between the two pixels that are on either side of the pixel that needs to be generated. After all of the "missing" pixels have been interpolated—presto!—200 pixels exist where only 100 existed before, and the image is twice as big as it used to be. there are many methods on interpolation; the method described here is an example of simple averaging.

JPEG — JPEG stands for joint picture experts group. however, what people usually mean when they use the term "JPEG" is the image compression standard developed by an international body. JPEG was developed to compress still images, such as photographs, a single video frame, something scanned into the computer, and so forth. You can run JPEG at any speed that the application requires. For a still picture database such as mugshots, the algorithm doesn't have to be too fast. If you run JPEG fast enough, though, you can compress motion video—which means that JPEG would have to run at 30 frames per second. You might want to do this if you were designing a video editing or authoring platform. Now, JPEG running at 30 frames per second is not as efficient as MPEG running at 30 frames per second because MPEG was designed to take advantage of certain aspects of motion video. So in a video editing platform, you would have to trade off the lower bit rate (high compression) of MPEG with the ability to do frame–by–frame edits in JPEG (but not in MPEG). Both standard have their place in an image compression strategy and both standards will probably exist in a box simultaneously.

Line Store — A line store is a memory buffer used to hold one line of video. If the horizontal resolution of the screen is 640 pixels and RGB is used as the color space, the line store would have to be 640 locations long by 3 bytes wide. This amounts to one location for each pixel and each color plane. Line stores are typically used in filtering algorithms. For exam-

ple, a comb filter is made up of two or more line stores. The DCT used in the JPEG and MPEG compression algorithms could use eight line stores since processing is done on blocks of 8x8 pixels.

Linearity — Linearity is a basic measurement of how well an ADC or DAC is performing. Linearity is typically measured by making the ADC or DAC represent a diagonal line. The actual output of the device is compared to what is the ideal output. The difference between the actual diagonal line and the ideal line is a measure of the linearity. The smaller the number, the better. Linearity is typically specified as a range or percentage of LSBs (least significant bits).

Locked — When a PLL is accurately producing horizontal syncs that are precisely lined up with the horizontal syncs of the incoming video source, the PLL is said to be "locked". When a PLL is locked, the PLL is stable and there is minimum jitter in the generated pixel clock.

Loop Filter — A loop filter is used in a PLL design to smooth out tiny bumps in the output of the phase comparator that might drive the loop out of lock. The loop filter helps to determine how well the loop locks, how long it takes to lock and how easy it is to knock the loop out of lock.

Lossless — Lossless is a term used with image compression. Lossless image compression is when the decompressed image is exactly the same as the original image. It's lossless because you haven't lost anything.

Lossy — Lossy image compression is the exact opposite of lossless. The regenerated image is different from the original image. The differences may or may not be noticeable, but if the two images are not identical, the compression was lossy.

Luma or Luminance — This is the brightness information in a video signal. As mentioned in the definition of chrominance, the NTSC and PAL video systems use a signal that has two pieces: the black and white part, and the color part. The black and white part is the luminance. It was the luminance component that allowed color TV broadcasts to be received by black and white TVs and still remain viewable.

LSB/MSB — Least Significant Bit, and Most Significant Bit designate the low and high value bits in a binary word, respectively.

Media Engine — This is the CPU or DSP processor that coordinates all of the video and audio activities in a multimedia platform. The media engine is used to coordinate the audio with the video, control multiple video inputs, and control the compression and decompression hardware. The media engine is most likely not the host CPU—e.g., not the 80486 processor on the PC motherboard.

MCU — MicroComputer Unit (also MicroController Unit).

Modulator — A modulator is basically a circuit that combines two different signals in such a way that they can be pulled apart late. What does this have to do with video? Let's take the NTSC system as an example, although the example applies equally as well to PAL. The NTSC system uses the YIQ color space, withe the I and Q signals containing all of the color information for the picture. Two 3.58 MHz color subcarrier (90° out of phase) are modulated by the I and Q components and added together to create the chrominance part of the NTSC video.

Moiré — This is a type of image artifact. A moiré pattern is typically generated when two different frequencies beat together to create a new, unwanted frequency.

Monochrome — A monochrome signal is a video source having only one component. Although usually meant to be the luminance (or black–and–white) video signal, the red video signal coming into the back of a computer display is monochrome because it only has one component.

Monotonic — This is a term that is used to describe ADCs and DACs. An ADC or DAC is said to be monotonic if for every increase in input signal, the output increases also. The output should not decrease. Any ADC or DAC that is nonmonotonic—meaning that the output does decrease for an increase in input—is bad! Nobody wants a nonmonotonic ADC or DAC.

Motion Estimation — Motion estimation is trying to figure out where an object has moved from one video frame to another. Why would you want to do that? Well, let's take an example of a video source showing a ball flying through the air. The background is a solid color that is different from the color of the ball. In one video frame the ball is at one location and in the next video frame the ball has moved up and to the right by some amount. Now let's assume that the video camera has just sent the first video frame of the series. Now, instead of sending the second frame, wouldn't it be more efficient to send only the position of the ball? Nothing else moves, so only two little numbers would have to be sent instead of 900 Kbytes (the amount of storage required for a whole frame of video). This is the essence of motion estimation. By the way, motion estimation is an integral part of MPEG.

MPEG — MPEG stands for Moving Picture Experts Group. This is an ISO (International Standards Organization) body that is developing compression algorithms for motion video. MPEG differs from JPEG in that MPEG takes advantage of the redundancy on a frame–to–frame basis of a motion video sequence, where JPEG does not.

Multimedia — Where does one start? This term has been so overused, mistreated, and so hyped up that it's lost all of its meaning. Multimedia was originally meant to describe a system that uses text, graphics, still pictures, video, and audio an interactive way to provide information. With this definition, a video game is not multimedia because it does not provide information, even though it is highly interactive. Video editing, even though it is interactive and deals with audio and video, is not multimedia because video editing is creating information, not supplying it. A good example of multimedia is an electronic encyclopedia. A student sits down at a computer, browses through a list of entries, and selects the one that is needed. A text passage is displayed on the screen along with a picture (the picture could be graphic based or a still or moving image). After reading for a while, the student clicks on the headphone icon to listen to an audio segment, which may contain a speech delivered by the person who is being researched. A click on a different icon produces a video clip showing this political leader in action at the last rally. All of the aspects described in the example are required for true multimedia. Accept no substitutes.

MPU — MicroProcessor Unit.

Noise — Any random fleck that shows up in the display. The noise may also be referred to as snow, flecks, blips, hash.

Noninterlaced — This is a method of scanning out a video display that is the total opposite of interlaced. All of the lines in the frame are scanned out sequentially, one right after the other. The term "field" does not apply in a noninterlaced system. Another term for a noninterlaced system is progressive scan.

NTSC — Color television signals in the United States and some other countries are encoded according to the National Television System Committee's (NTSC) specifications. Although NTSC is, strictly speaking, a composite standard, a Y/C signal may possess NTSC scan rate properties.

PAL — The western European broadcast standard gets its name from the encoding scheme: Phase Alternation Line (PAL). Besides offering more scan lines (625 versus 525 for NTSC), the PAL system was designed to correct color decoding errors and to provide more uniform color reproduction.

Pass-band Filter — A filter used in communication systems that allows only the frequencies within a communication channel to pass, and rejects all frequencies outside the channel.

Pedestal — Pedestal is an offset used to separate the active video from the blanking level. When a video system uses a pedestal, the black level is above the blanking level by a small amount. When a video system doesn't use a pedestal, the black and blanking levels are the same. NTSC uses a pedestal, PAL and SECAM do not.

Phase Adjust — This is a term used to describe a method of adjusting the color in an NTSC video signal. The phase of the color subcarrier is moved, or adjusted, relative to the color burst. This adjustment affects the hue of the picture.

Phase Comparator — This is a circuit used in a PLL to tell how well two signals line up with each other. For example, let's say we have two signals, A and B, with signal A connected to the positive (+) input of the phase comparator and signal B connected to the minus (–) input. If bother signals are exactly the same, the output of the phase comparator is 0; they are perfectly aligned, Now, if Signal A is just a little bit faster than signal B, then the output of the phase comparator is a 1, showing that A is faster than B. If signal A is slower than B, then the output of the phase comparator is a –1, designating that B is faster. Read the phase–locked loop definition to see how a phase comparator is used in a circuit.

Phased–Locked Loop — A phase–locked loop (PLL) is the heart of any genlocked system. Very simply, a PLL is a means of providing a very stable pixel clock that is based or referenced to some other signal. Let's say that we want to design a video system with a horizontal resolution of 100 pixels. Let's assume that, in order to get the 100 pixels across the display, if the horizontal sync rate were perfect, we would need a pixel clock of 5 MHz. If we didn't have a PLL and the horizontal rate were to shrink a little (the horizontal width gets smaller), we would get less than 100 pixels because we didn't adjust the pixel clock. Or, conversely, if the horizontal rate were to become a little longer (the image widens just a little), we would get more than 100 pixels. This is definitely bad news, because the time between horizontal syncs usually does vary just a tiny little bit, small enough that you may not notice it on your TV, but a computer would notice. So, from line to line, the number of pixels would change. A PLL guarantees that the same number of pixels appears on every line by changing the pixel clock frequency to match the horizontal sync rate.

First, a voltage controlled oscillator (VCO) or voltage controlled crystal oscillator (VCXO) is used and the free–running frequency is set to the pixel clock rate needed if the horizontal rate was always to be perfect. The output of the VCO or VCXO is then used as the system pixel clock. This pixel clock is also used as the input to a circuit that takes the pixel clock frequency and divides it down to the horizontal sync frequency. So, at this point, we have a new signal whose frequency is the same as the frequency of horizontal sync. This newly generated signal, along with horizontal sync, are inputs to a phase comparator. The output of the phase comparator tells how well the output of the clock divider lines up with the incoming horizontal sync. The output of the phase comparator is fed to a loop filter to remove tiny little bumps that might throw the system out of whack. The output of the loop filter then becomes the control voltage for the VCO or VCXO.

With this arrangement, if the incoming horizontal rate is just a little too fast, the phase comparator generates a signal that is then filtered and tells the VCO/VCXO to speed up a little bit. The VCO/VCXO does, which then speeds up the pixel clock just enough to ensure that the horizontal resolution is 100 pixels. This pixel clock is divided down to the horizontal sync rate and is then phase compared again.

Pixel — A pixel, which is short for picture element, is the smallest division that makes up the raster scan line for computers. For example, when the horizontal resolution is defined as 640, that means that there are 640 individual locations, or spots, that make up the horizontal scan line. A pixel is also referred to as a pel. A "square" pixel is one that has an aspect ratio of 1:1, or the width is equal to the height. Square pixels are needed in computers so that when the software draws a square in the frame buffer, it looks like a square on the screen. If the pixels weren't square, the box would look like a rectangle. NTSC, PAL, and SECAM television systems use pixels that have a 4:3 aspect ratio.

Pixel Clock — The pixel clock is used to divide the incoming horizontal line of video into pixels. this pixel clock has to be stable (a very small amount of jitter) relative to the incoming video or the picture will not be stored correctly. The higher the frequency of the pixel clock, the more pixels that will appear across the screen.

Pixel Drop Out — This can be a real troublemaker, since it can cause image artifacts. in some instances, a pixel drop out looks like black spots on the screen, either stationary or moving around. several things can cause pixel drop out, such as the ADC not digitizing the video correctly. Also, the timing between the ADC and the frame buffer might not be correct, causing the wrong number to be stored in the buffer. For that matter, the timing anywhere in the video stream might cause a pixel drop out.

PLL — See Phase-Locked Loop.

PLL Frequency Synthesizer — Phase-locked loop frequency synthesizer. A frequency synthesizer utilizing a closed loop, as opposed to DDS (direct digital synthesis) which is not a closed loop.

Pseudo Color — Pseudo color is a term used to describe a technique that applies color, or shows color, where 1 does not really exist. We are all familiar with the satellite photos that show temperature differences across a continent or the multicolored cloud motion sequences on the nightly weather report. These are real–world examples of pseudo color. The color does not really exist. The computer adds the color so the information, such as temperature or cloud height, is viewable.

Px64 — This is basically the same as H.261.

Quad Chroma — Quad chroma refers to a technique where the pixel clock is four times the frequency of the chroma burst. For NTSC this means that the pixel clock is 14.31818 MHz (4 x 3.57955 MHz), while for PAL the pixel clock is 17.73444 MHz (4 x 4.43361 MHz). The reason these are popular pixel clock frequencies is that, depending on the method chosen, they make the chrominance (color) decoding easier.

Quantizing Noise — Signal-correlated noise generally associated with the quantizing error introduced by A/D and D/A conversions in digital transmission systems.

Raster — Essentially, a raster is the series of scan lines that make up a TV picture or a computer's display. You may from time to time hear the term raster line—it's the same as scan line. All of the scan lines that make up a frame of video form a raster.

Real Time — If a system incorporating a computer operates fast enough that it seems like there isn't a computer in the loop, then that computer system is operating in real time. How fast "real time" really is changes depending on who or what is using the system. For example, a fighter pilot flying the latest computer–controlled jet moves the stick to perform a roll maneuver. The stick then tells a computer its position, the computer makes some decisions, and then it tells the flaps and rudder what adjustments to make to perform the move. Since all of this happens fast enough so that the pilot thinks the stick is connected directly to the flaps and rudder, the place is a real–time system.

What's the definition of real time for video? Well, for NTSC that's 30 frames per second, with each frame made up 525 individual scan lines. That's roughly equivalent to 30 Mbytes of data per second that must be processed.

Residual Subcarrier — This is the amount of color subcarrier information in the color data after decoding a NTSC or PAL video signal. The number usually appears as $-n$ dB. The larger n is, the better.

Resistor Ladder — A resistor ladder is a string of resistors used for defining voltage references. In the case of 8–bit. flash ADCs, the resistor ladder si made up of 256 individual resistors, each having the same resistance. If a voltage representing the number 1 is attached to one end of the ladder and the other end is attached to 09, each junction between resistors is different from the other by 1/256. So, if we start at the top of the ladder, the value is 1. If we move down one rung, the value is 0.99609, the next rung's value is 0.99219, the next rung's is 0.98828 and son down the ladder until we reach 0 (the other end of the ladder). A resistor ladder is an important part of a flash ADC because each rung of the ladder, or tap, is connected to on side of a comparator, in effect providing 256 references. The definition of flash ADCs helps out here.

Resolution — This is a basic measurement of how much information in on the scree. It is usually described as "some number" by "some number." The first "some number" is the horizontal (across the screen) resolution and the second some number is the vertical resolution (down the screen). The higher the number, the better, since that means there's more detail to see. Some typical examples of resolutions are:

VHS:	330 by 220
S–VHS:	400 by 300
Studio Quality:	720 by 480
Personal Computer Screen:	1024 by 768
Workstation Computer Screen;	1280 by 1024

Retrace — Retrace is what the electron beam does when it gets to the right–hand edge of the display to get back to the lift–hand edge. Retrace happens during the blanking time.

RGB — Video information separated into the three primary colors: red, green, and blue. The VGA graphics standard generates RGB signals for display on VGA monitors. Each color signal is carried on a separate wire.

RGB:6:5 — The MC144000EVK PC Video Capture Evaluation Kit uses the 5:6:5 video format (5 bits of RED, 6 bits of GREEN, and 5 bits of BLUE). This allows a 16 bit word in WINDOW VIDEO STORE memory to store a single color pixel. This format allows excellent video rendition while minimizing storage needs.

RS–170, RS–170A — RS–170 is the United States standard that was used for black–and–white TV, and defines voltage levels, blanking times, the width of the sync pulses, and so forth. The specification spells out everything required for a receiver to display a monochrome picture. The output of those little black–and–white security cameras hanging from ceilings conforms to the RS–170 specification. Now, RS–170A is essentially the same specification, modified for color TV by adding the color components. When the NTSC decided on the color broadcast standard, they modified RS–170 just a tiny little bit so that color could be added, with the result being called RS–170A. This tiny little change was so small that the existing black–and–white TVs didn't even notice it.

RS–343 — RS–343 does the same thing as RS–170, defining a specification for video, but the difference is that RS–343 is for higher–resolution video (computers) while RE–170 is for lower–resolution video (TV).

Run Length Coding — Run length coding is a type of data compression. Let's say that this page is wide enough to hold a line of 80 characters. Now, imagine a line that is almost blank except for a few words. It's 80 characters long, but it's just about all blanks—let's say 50 blanks between the words "coding" and "medium". These 50 blanks could be stored as 50 individual codes, but that would take up 50 bytes of storage. An alternative would be to define a special code that said a string of blanks is coming and the next number is the amount of blanks in the string. So, using our example, we would need only two bytes to store the string of 50 blanks, the first special code byte followed by the number 50. We compressed the data; 50 bytes down to two. This is a compression ratio of 25:1. Not bad, except that we only compressed one line out of this entire document, so we should expect that the total compression ratio would be much less.

Run length coding all by itself as applied to images is not as efficient as using a DCT for compression, since long runs of the same "number" or series rarely exist in real–world images. The only advantage of run length coding over the DCT is that it is easier to implement. Even though run length coding by itself is not efficient for compressing images, it is used as part of the JPEG and MPEG compression schemes.

S–VHS — S–VHS is an enhancement to regular VHS video tape decks. S–VHS provides better resolution and less noise than VHS. S–VHS video tape decks support separate luminance (Y) and chrominance (C) video inputs and outputs, although this is not required. It does, however, improve the quality by not having to continuously merge and then separate the luminance and chrominance signals.

S–Video — Separate video, also called Y/C.

Sampling Rate — The frequency at which the amplitude of an analog signal is gated into an A/D circuit. The Nyquist sampling theorem states that if a band-limited signal is sampled at regular intervals and at a rate equal to or greater than twice the highest frequency of interest, the sample contains all the information of the original signal.

Saturation — Saturation is the amount of color present. For example, a lightly saturated red looks pink, while a fully saturated red looks like the color of a red crayon. Saturation does not mean the brightness of the color, just how much "pigment" is used to make the color. The less "pigment," the less saturated the color is, effectively adding white to the pure color.

Scaling — Scaling is the act of changing the effective resolution of the image. For example, let's take a TV size resolution of 640 x 480 and display that image as a smaller picture on the same screen, so that multiple pictures can be shown simultaneously. We could scale the original image down to a resolution 320 x 240, which is 1/4 of the original size. Now, four pictures can be shown at the same time. That was an example of "scaling down." Scaling up is what occurs when a snapshot is enlarged into an 8 x 10 glossy. There are many different methods for image scaling, and some "look" bitter than others. In general, though, the better the algorithm "looks," the harder or more expensive it is to implement.

Scan Line — A scan line is an individual sweep across the face of the face of the display by the electron beam that makes the picture. An example of a scan line is what happens in a copier. When you press the copy button, a mirror "scans" the document by moving across the length of the page. Same concept with television—an electron beam "scans" the screen to produce the image on the display. It takes 525 of these scan lines to make up an NTSC TV picture.

Scratch 'n Sniff Holography — An early–generation multisensory multimedia apparatus exercising the auditory, olfactory and visual senses. The combination of a variety of technologies, all or part of which continue to be used in print media to "bring a page to life". The three dimensional smelly apparatus is activated by scratching with a sharp tool such as the fingernail.

SECAM — This is another TV format similar to PAL. The major difference between the two is that in SECAM the chrominance is FM modulated.

Serration Pulses — These are pulses that occur during the vertical sync interval, at twice the normal horizontal scan rate. The reason these exist was to ensure correct 2:1 interlacing in early televisions.

Setup — Setup is the same thing as Pedestal.

Signal-to-Distortion Ratio (S/D) — The ratio of the input signal level to the level of all components that are present when the input signal (usually a 1.020 kHz sinusoid) is eliminated from the output signal (e.g., by filtering).

Signal-to-Noise Ratio (SNR) — Signal–to–noise ratio is the magnitude of the signal divided by the amount of unwanted stuff that is interfering with the signal (the noise). SNR is usually described in decibels, or dB, for short; the bigger the number, the better looking the picture.

Subsampled — Subsampled means that a signal has been sampled at a lower rate than some other signal in the system. A prime example of this is the YCrCb color space used in CCIR 601. For every; two luminance (Y) samples, only on Cr and Cb sample is taken. This means that the Cr and Cb signals are subsampled.

Sync — Scanned video lines and video fields in both the NTSC and PAL standards are separated by special signals called "sync" signals. The horizontal sync signal occur between successive lines of video signals. The vertical sync information is conveyed during the vertical blanking interval (VBI). The VBI is composed of approximately 20 successive lines of black level information. Each line during the vertical sync interval is 'serrated' to produce a sync frequency twice that of normal. in addition, the center portion of the vertical sync interval is inverted to make extracting the vertical sync easier.

Sync Generator — A sync generator is a circuit that provides sync signals. A sync generator may have genlock capability, or it may not.

Sync Noise Gate — A sync noise gate is used to define an area within the video waveform where the sync stripper is to look for the sync pulse. Anything outside of this defined window will be rejected by the sync noise gate and won't be passed on to the sync stripper. The main purpose of the sync noise gate is to make sure that the output of the sync stripper is nice, clean, and correct.

Sync Stripper — A composite video signal contains video information, which is the picture to be displayed, and timing (sync) information that tells the receiver where to put this video information on the display. A sync stripper pulls out the sync information from the composite video signal and throws the rest away.

Tessellated Sync — This is what the Europeans call serrated sync. See the definitions of serration pulses and composite sync.

Timebase Corrector — Certain video sources have their sync signals screwed up. the most common of these sources is the VCR. A timebase corrector "heals" a video signal that has bad sync. (I guess you could call a time base corrector a "sync doctor.") This term is included because more and more companies making video capture cards are providing this function.

True Color — True color means that an image is represented using at least three color components, such as RGB or YCrCb.

Vector Scope — A vector scope is used to determine the color purity of a NTSC or PAL video system. If you've read the YIQ or YUV definitions, then you know that the I and Q (or U and V) components are the axis of a Cartesian coordinate system. The vector scope is essentially a Cartesian coordinate display scope. the vector scope looks at the I and Q signals and puts a point of light where the two signals say the color is. On a vector scope, six little boxes correspond to the six colors in the standard color bar pattern: yellow, cyan, magenta, green, red, and blue. If the input to the video system is a color bar pattern from a test generator and the output is displayed on a vector scope, then the accuracy of the color system can be checked. Each point of light that represents the corresponding color should be within the little box—certainly, the closer the better. If the spot makes it within the little box, that represents an error of less than ± 2°. That means you can't notice the error with you eyeball.

Vertical Scan Rate — This is the same as the frame rate.

Vertical Sync — This is the portion of the composite video signal that tells the receiver where the top of the picture is.

VGA — The most popular graphics standard on PCs and PC compatibles, standard VGA is 640x480 picture elements, in 16 or 256 colors. Higher resolution and greater color depth is known as "Super VGA".

Video Mixing — Video mixing is taking two independent video sources and merging them together.

Video Waveform — The video waveform is what the signal "looks" like to the receiver of TV. The video waveform is made up of several parts (sync, blanking, video, etc.) that are all required to make up a TV picture that can be accurately displayed.

Voltage Controlled Crystal Oscillator (VCXO) — A VCXO is just like a voltage–controlled oscillator except that a VCXO uses a crystal to set the free–running frequency. This means that a VCXO is more stable than a VCO but it's also more expensive to implement.

Voltage Controlled Oscillator (VCO) — A VCO is a special type of oscillator that changes its frequency depending on what the voltage is on a control pin. A VCO has what's called a free–running frequency which is the frequency that the oscillator runs at when the control voltage is at midrange, normal operating condition. If the control voltage rises above midrange, the VCO increases the frequency of the output clock, and if the control voltage falls below midrange, then the VCO lowers the frequency of the output clock. See the definition of a phase–locked loop.

White Level — This level defines what white is for the particular video system.

Y/C Separator — A Y/C separator is what's used in a decoder to pull the luminance and chrominance apart in an NTSC or PAL system. This is the first thing that any NTSC or PAL receiver must do. The composite video signal is first fed to the Y/C separator so that the chrominance can then be decoded further.

YCrCb — YCrCb is the color space used in the CCIR601 specification. Y is the luminance component and the Cr and Cb components are color difference signals. Cr and Cb are scaled versions of U and V in the YUV color space.

4:2:2 YCrCb means that Y has been sampled at 13.5 MHz, while Cr and Cb were each sampled a 6.75 MHz.Thus, for every two samples of Y, there is one sample each of Cr and Cb. 4:1:1 YCrCb means the Y has been sampled at 13.5 MHz, while Cr and Cb were each sampled a 3.375 MHz. thus, for every four samples of Y, there is one sample each of Cr and Cb. 2:1:1 YCrCb means that Y has been sampled at 6.75 MHz, while Cr and Cb were each sampled at 3.375 MHz. Thus, for every two samples of Y, there is one sample each of Cr and Cb. This notation may also be used with YUV, YIQ, HSI, and HSV color spaces, where required.

Y/C Video (S–VHS) — Because of the S–VHS video recorder's popularity, the Y/C format is most commonly known as S–VHS. Luminance and color information is distributed as two separate but dependent signals. The Y, or luminance signal, carries the brightness and color burst information. This signal is compatible with monochrome television and may be used as–is with black and white television receivers. The C signal carries the color difference information. This signal is the quadrature sum of the two color difference signals and is not yet decoded. The information contained in both the Y and C signals must be suppled to an appropriate decoder to obtain the RGB color information. Picture synchronization is supplied with the brightness signal. Because there is no luminance/color difference frequency interleaving as in composite video, there is less interference between the luminance and color signals; therefore, more information can be conveyed. Horizontal resolution is 400 lines or more, equivalent to a laser disk image displayed on a good quality monitor with S–VHS input.

YIQ — YIQ is the color space used in the NTSC color system. The Y component is the black–and–white portion of the image. The I and Q parts are the color components; these are effectively nothing more than a "watercolor wash" placed over the black and white, or luminance, component.

YUV — YUV is the color space used by the PAL color system (it may also be used in the NTSC system). As with the YIQ color space, the Y is the luminance component while the U and V are the color components.

Zeroing — Zeroing is what's done to the bank of comparators in a CMOS flash ADC to keep them honest. Without zeroing, the comparators would build up enough of an error that the output of the flash ADC would not be correct any more. To solve the problem, the comparators are "zeroed," or the accumulated error is removed.

Zipper — See the definition for creepy–crawlies.

Zoom — Zoom is a type of image scaling. Zooming is making the picture larger so that you can see more detail. In a way, it's sort of like a "video microscope", since a microscope makes things larger so that they are easier to see. A microscope does this optically, with lenses, while video zooming does it mathematically. The examples described in the definition of scaling are also examples that could be used here.

Useful Addresses

ANSI **American National Standards Institute**
11 West 42nd Street
New York, NY 10036
USA

EIA **Electronic Industries Association**
1722 Eye Street, NW
Suite 440
Washington, DC 20006
USA
Phone (Headquarters): (202) 457-4936
Phone (Standards): (202) 457-4966

IEEE **Institute of Electrical and Electronics Engineers**
Headquarters:
345 East 47th Street
New York, NY 10017
USA
Phone: (212) 705-7900

Standards Office:
IEEE Service Center
PO Box 1331
Piscataway, NJ 00855
USA
Phone: (201) 981-0060

SMPTE **Society of Motion Picture and Television Engineers**
595 W. Hantsdale Ave.
White Plains, NY 10607
USA
Phone: (914) 761–1100
Fax: (914) 761–3115

Handling and Design Guidelines

6

Handling and Design Guidelines

HANDLING PRECAUTIONS

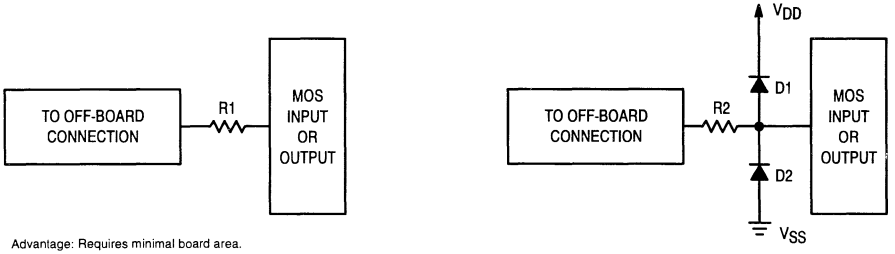
All CMOS devices have an insulated gate that is subject to voltage breakdown. The high-impedance gates on the devices are protected by on-chip networks. However, these on-chip networks do not make the IC immune to electrostatic damage (ESD). Laboratory tests show that devices may fail after one very high voltage discharge. They may also fail due to the cumulative effect of several discharges of lower potential.

Static-damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged are the easiest to detect because the input or output has been completely destroyed and is either shorted to V_{DD}, shorted to V_{SS}, or open-circuited. The effect is that the device is no longer functional. Less severe cases are more difficult to detect because they appear as intermittent failures or degraded performance. Static damage can often increase leakage currents.

CMOS devices are not immune to large static voltage discharges that can be generated while handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4–15 kV range (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed.

1. Do not exceed the Maximum Ratings specified by the data sheet.
2. All unused device inputs should be connected to V_{DD} or V_{SS}.
3. All low-impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
4. A circuit board containing CMOS or devices is merely an extension of the device and the same handling precautions apply. Contacting connectors wired directly to devices can cause damage. Plastic wrapping should be avoided. When external connections to a PC board address pins of CMOS integrated circuits, a resistor should be used in series with the inputs or outputs. The limiting factor for the series resistor is the added delay caused by the time constant formed by the series resistor and input capacitance. This resistor will help limit accidental damage if the PC board is removed and brought into contact with static generating materials. For convenience, equations for added propagation delay and rise time effects due to series resistance size are given in Figure 1.
5. All CMOS devices should be stored or transported in materials that are antistatic. Devices must not be inserted into conventional plastic "snow", styrofoam or plastic trays, but should be left in their original container until ready for use.

Figure 1. Networks for Minimizing ESD and Reducing CMOS Latch Up Susceptibility



NOTE: These networks are useful for protecting the following:

A. digital inputs and outputs
B. analog inputs and outputs
C. 3-state outputs
D. bidirectional (I/O) ports

EQUATION 1 – PROPAGATION DELAY VS SERIES RESISTANCE

$$R \approx \frac{t}{C \bullet k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum tolerable propagation delay in seconds
C = the board capacitance plus the driven device's input capacitance in farads
k = 0.33 for devices with TTL input levels (switch point ≈ 1.3 V)
k = 0.7 for devices with CMOS input levels (switch point ≈ 50% V_{DD}).

EQUATION 2 – RISE TIME VS SERIES RESISTANCE

$$R \approx \frac{t}{C \bullet k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum tolerable propagation delay in seconds
C = the board capacitance plus the driven device's input capacitance in farads
k = 0.7 for devices with TTL input levels (switch point ≈ 1.3 V)
k = 2.3 for devices with CMOS input levels (switch point ≈ 50% V_{DD}).

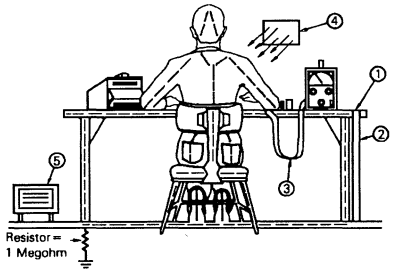
6. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 2.
7. Nylon or other static generating materials should not come in contact with CMOS circuits.
8. If automatic handling is being used, high levels of static electricity may be generated by the movement of devices, belts, or boards. Reduce static build-up by using ionized air blowers or room humidifiers. All parts of machines which come into contact with the top, bottom, and sides of IC packages must be grounded metal or other conductive material.
9. Cold chambers using CO_2 for cooling should be equipped with baffles, and devices must be contained on or in conductive material.
10. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.
11. The following steps should be observed during wave solder operations.
    a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.
    b. The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
    c. Operators must comply with precautions previously explained.
    d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.
12. The following steps should be observed during board cleaning operation.
    a. Vapor degreasers and baskets must be grounded to an earth ground. Operators must likewise be grounded.
    b. Brush or spray cleaning should not be used.
    c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
    d. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
    e. High velocity air movement or application of solvents and coatings should be employed only when module circuits are grounded and a static eliminator is directed at the module.
13. The use of static detection meters for line surveillance is highly recommended.
14. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
15. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
16. Double check the equipment setup for proper polarity of voltage before conducting parametric or functional testing.

RECOMMENDED READING

"Total Control of the Static in Your Business"
Available by writing to:
3M
Static Control Systems
Building A145-3N-01
P.O. Box 2963
Austin, TX 78769-2963

Or calling:
1-800-328-1368

Figure 2. Typical Manufacturing Work Station



NOTES:
1. 1/16 inch conductive sheet stock covering bench top work area.
2. Ground strap.
3. Wrist strap in contact with skin.
4. Static neutralizer. (Ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.
5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside of buildings to be less than outside humidity.

CMOS LATCH UP

Latch up will not be a problem for most designs, but the designer should be aware of it, what causes it, and how to prevent it.

Figure 3 shows the layout of a typical CMOS inverter and Figure 4 shows the parasitic bipolar devices that are formed. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch-up condition, transistors Q1 and Q2 are turned on, each providing the base current necessary for the other to remain in saturation, thereby latching the devices on. Unlike a conventional SCR, where the device is turned on by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned on by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch up the CMOS device, the output voltage must be greater than V_{DD} + 0.5 Vdc or less than – 0.5 Vdc and have sufficient current to trigger the SCR. The latch-up mechanism is similar for the inputs.

Once a CMOS device is latched up, if the supply current is not limited, the device will be destroyed. Ways to prevent such occurrences are listed below.

1. Ensure that inputs and outputs are limited to the maximum rated values, as follows:
   – 0.5 ≤ V_{in} ≤ V_{DD} + 0.5 Vdc referenced to V_{SS}
   – 0.5 ≤ V_{out} ≤ V_{DD} + 0.5 Vdc referenced to V_{SS}
   $|I_{in}|$ ≤ 10 mA
   $|I_{out}|$ ≤ 10 mA when transients or dc levels exceed the supply voltages.
2. If voltage transients of sufficient energy to latch up the device are expected on the outputs, external protection diodes can be used to clamp the voltage. Another method of protection is to use a series resistor to limit the expected worst case current to the Maximum Ratings values (see Figure 1).
3. If voltage transients are expected on the inputs, protection diodes may be used to clamp the voltage or a series resistor may be used to limit the current to a level less than the maximum rating of I_{in} = 10 mA (see Figure 1).
4. Sequence power supplies so that the inputs or outputs of CMOS devices are not powered up first (e.g., recessed edge connectors may be used in plug-in board applications and/or series resistors).
5. Power supply lines should be free of excessive noise. Care in board layout and filtering should be used.
6. Limit the available power supply current to the devices that are subject to latch-up conditions. This can be accomplished with the power supply filtering network or with a current-limiting regulator.

Figure 3. CMOS Wafer Cross Section

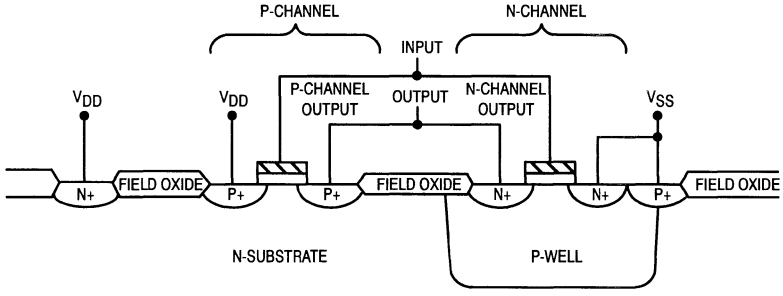
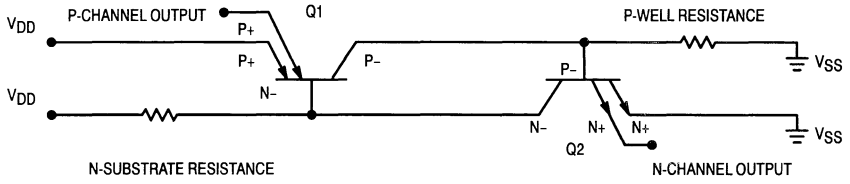


Figure 4. Latch Up Circuit Schematic



Quality and Reliability

7

7

Quality In Manufacturing

QUALITY IN DESIGN

Motorola's quality activity starts at the product design stage. It is Motorola's philosophy to "design in" reliability. At all development points of any new design reliability oriented guidelines are continuously used to ensure that a thoroughly reliable part is ultimately produced. This is demonstrated by the excellent in-house reliability testing results obtained for all Motorola's semiconductor products and, more importantly, by our numerous customers.

MATERIAL INCOMING CONTROLS

Each vendor is supplied with a copy of the Motorola Procurement Specification which must be agreed in detail between both parties before any purchasing agreement is made. This is followed by a vendor appraisal report whereby each vendor's manufacturing facility is visited by Motorola Quality Engineers responsible for ensuring that the vendor has a well organized and adequately controlled manufacturing process capable of supplying the high quality material required to meet the Motorola Incoming Inspection Specification. Large investments have and are continuously being made and Quality Improvement programs developed with our main suppliers concerning:

Masks — Silicon — Piece-parts — Chemical products — Industrial gas, etc.

Each batch of material delivered to Motorola is quarantined at Goods-in until the Incoming Quality Organization has subjected adequate samples to the incoming detailed inspection specification. In the case of masks, this will include mask inspection for:

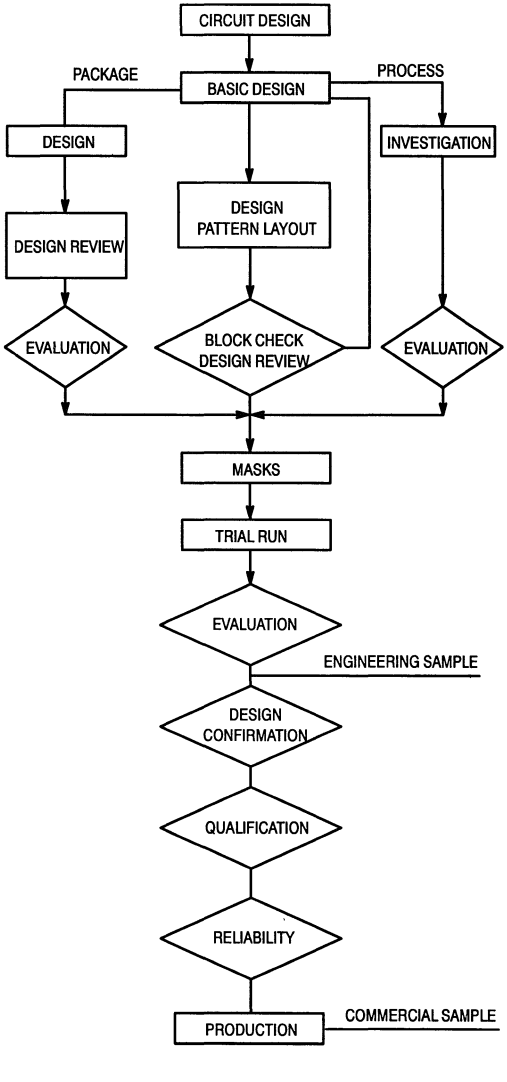
1. Defect Density
2. Intermask Alignment
3. Mask Revision
4. Device to Device Alignment
5. Mask Type

Silicon will undergo the following inspections:

1. Type "N" or "P"
2. Resistivity
3. Resistivity Gradient
4. Defects
5. Physical Dimensions
6. Dislocation Density

Incoming chemicals are also controlled to very rigorous standards. Many are submitted to in-house chemical analysis where the supplier's conformance to specification is meticulously checked. In many cases, line tests are performed before final acceptance. A major issue and responsibility for the Incoming Quality Department is to ensure that the most disciplined safety factors have been employed with regard to chemicals. Chemicals can and are often rejected because safety standards have not been deemed acceptable.

NEW PRODUCT TYPICAL DESIGN FLOW



THIS BASIC DESIGN FLOW-CHART OMITS SOME FEEDBACK LOOPS FOR SIMPLICITY

7

The Six Sigma Challenge

Motorola's expressed objective is the achievement of "error free performance" in products and services. The high quality level of the product-line outputs, followed by stringent outgoing quality control, readily assures this objective. But error-free output from the product lines themselves is a matter that continues to demand full attention at all levels of production, design and administration. This far more stringent requirement has a two-fold goal:

1. To further improve ultimate product reliability — experience has proved that products **designed** for 100% conformance to specifications are far less subject to field failure than products **selected** to a given level of performance.
2. To reduce waste — thereby making the end-product more cost competitive.

Whether or not one-hundred percent perfection is consistently achievable remains subject to conjecture. Motorola's already low reject rates, however, warrant a high level of confidence that the goal can be met, and milestones toward this objective have been firmly established.

Six Sigma Capability — not yet zero defects, but 99.9999998% perfection in both product and in customer services.

Why Six Sigma?

Each process attempts to reproduce its characteristics identically from unit to unit. Inherent in each process, however, there are variations in conditions and in materials that are uncontrollable and unalterable. In all cases, therefore, the unit-to-unit output characteristics vary somewhat from the ideal (design target).

The performance of a product is determined by how much margin exists between the design specifications and the actual value of that specification. For some processes, such as those using real-time feedback to control the output, the variations can be quite small; for others they may be quite large. Many of the parametric data of a given specification tend to follow the normal distribution curve shown in Figure 1.

Variation of the process is measured in Standard Deviations (Sigma) from the Mean. The normal deviation, defined as process width, is ± 3 Sigma about the mean, representing a yield of 99.73%. But is ± 3 Sigma good enough as an overall specification? Statistically, with a ± 3 sigma deviation, approximately 2700 parts per million still fall outside acceptable performance limits. Clearly, for a product to be built virtually defect free it must be designed with a component yield that is significantly better than ± 3 Sigma.

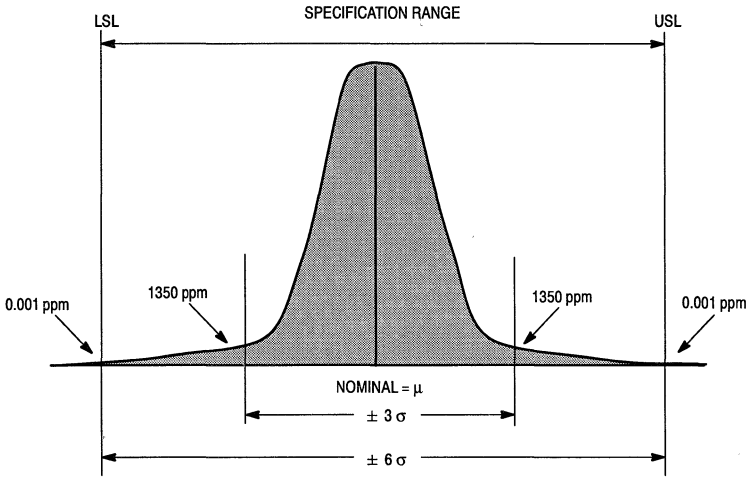
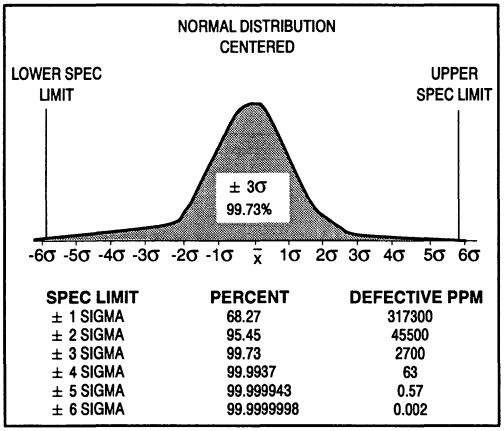


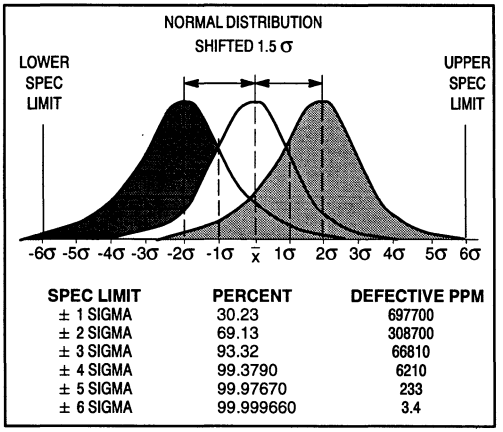
Figure 1. Standard distribution curve illustrates the Three Sigma and Six Sigma Parametric Conformance.

7



SPEC LIMIT	PERCENT	DEFECTIVE PPM
± 1 SIGMA	68.27	317300
± 2 SIGMA	95.45	45500
± 3 SIGMA	99.73	2700
± 4 SIGMA	99.9937	63
± 5 SIGMA	99.999943	0.57
± 6 SIGMA	99.9999998	0.002

Figure 2. With a Centered Distribution Between Six-Sigma Limits Only Two Devices Per Billion Fail to Meet the Specification Target.



SPEC LIMIT	PERCENT	DEFECTIVE PPM
± 1 SIGMA	30.23	697700
± 2 SIGMA	69.13	308700
± 3 SIGMA	93.32	66810
± 4 SIGMA	99.3790	6210
± 5 SIGMA	99.97670	233
± 6 SIGMA	99.999660	3.4

Figure 3. Effects of a 1.5 Sigma Shift Where Only 3.4 ppm Fail to Meet Specification.

The Six Sigma Latitude

Product yield is a factor of two variables: Process width and design width. If a process is adequately controlled so that its output is ± 3 Sigma, and if the product is so well designed that ± 3 Sigma deviations still place the products well within the specified design limits, then the overall yield is increased.

The table in Figure 2 shows that a design which can accept twice the normal ± 3 Sigma variation of the process (design width = ± 6 Sigma) will have a product yield of 99.9999998%, corresponding to 2.0 defective parts per billion. Even if the process mean were to shift by as much as ± 1.5 Sigma from the center of the distribution, the process would be expected to have no more than 3.4 parts per million defective.

The Motorola SPC Program

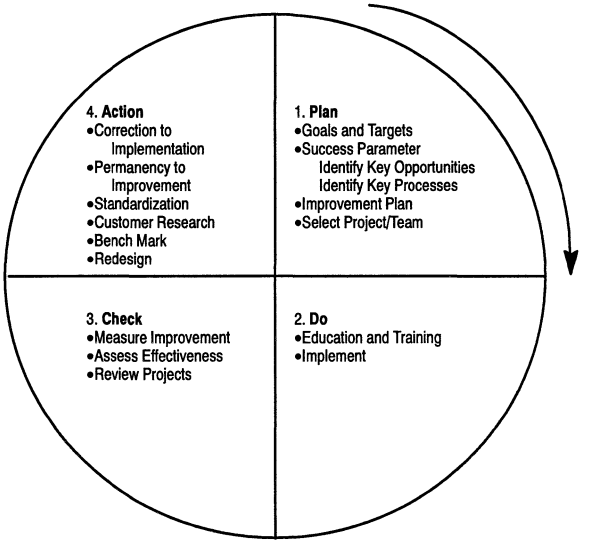
*** Purpose * Objective * Scope**

The Purpose of this program is to establish a standard approach toward continued process improvement through statistical process control.

Its Objective is to maintain all critical processes under tight statistical control in order to enhance quality and reduce scrap through identification of process variation, and through the reduction of these variations by means of real time corrective action. It is expected to establish the cultural environment and the organizational support required to achieve the Six-Sigma goal.

Its Scope encompasses a total quality improvement effort, involving design, manufacturing and management of all Motorola product groups and their suppliers as well as their support departments and vendors. It provides for the establishment of SPC teams and ensures adequate training. It serves as a liaison between teams in order to standardize and unify the approach to continuous quality improvement.

Continuous Improvement



Key Factors for Success

- Management Leadership
  - Top Down
  - Committed
  - Active
- Clear and Agreed-On Goals
- Breakthrough Thinking
- Project/Teamwork
- Training
- Reinforcing Successes

7

Verification of Statistical Process Control

Statistical process control programs have two specific functions:

1. as a monitor, to verify that a specific process is under control, or to indicate that a process is not in control based on interpretation of control-chart abnormalities or other indications;

2. as a quality improvement tool, for the purpose of improving process capability.

In either case, documentation must be available that permits the utilization, verification and interpretation of process control data, or if necessary, to implement new programs for process improvement.

Evidence of Process Capability

Capability indices must be established for each critical process and there must be evidence that the upper and lower specification limits are realistic and not arbitrary. The present goal is $C_p \geq 2.0$ and $C_{pk} \geq 1.5$.

Evidence of a process capability study must be on file. Depending on the level of sophistication, the study may include a factorial experiment, a nested variance study, summation of the results and recommendation for further action. The selection of critical process points must be justified.

Measurement System Capability

Results of measurement system capability study must be on file. Precision-to-Tolerance (P/T) ratio should be less than 0.10.

Process Control Specifications

Process specifications must include procedures to be followed in the event of a process requiring corrective action.

Operator Training

The operators are normally the first to see the control charts. Incorrect interpretation will cause unnecessary and time consuming investigations or delay needed studies. Consequently, operator training is a vital function and documented operator certification must be on file.

Control Chart Accuracy and Visibility

Control charts must be current and readily available. They shall be maintained by the production operators and upper and lower control limits must be calculated according to historical data.

Control Chart Tracking

Control charts must be tracked continuously. All out-of-control points must be highlighted and the appropriate corrective action described either on the chart or in a companion log. The objective is to view the trend, not simply to obtain a snapshot-in-time.

Supplier/Customer Relationships

Customers have no desire to control a supplier's process. Nor are they interested in the confidential details of a supplier's processes. They only want assurance (data) that a supplier has an ongoing program that supports an overall statistical process control plan. Primarily, Motorola's customers are interested in a supplier's statistical control of the critical processes, and his early warning system which keeps a process from becoming marginal. Most importantly, they are interested in what is being done for continuous improvement.

What We Offer Our Customers

It has been adequately demonstrated that a well monitored and controlled manufacturing process with minimum variations will produce a better, more useful and more reliable product at a reduced cost. In many instances, customer satisfaction now hinges not so much on a product's ability to meet specifications as on a manufacturer's ability to control his processes as evidenced by reduced variability. This is used as an indicator of both product quality and projected costs. Motorola provides detailed data and inferential statistics that allow customers to make decisions about the product they buy. In many instances, we provide a customer access to our computer data banks in order to improve communications and reduce turnaround time for product approval.

What We Expect From Our Suppliers

Improved quality of incoming material is crucial to success in achieving our Six Sigma goals. In order to accomplish this goal, we feel it necessary to reduce the number of suppliers and to work closely with those remaining as partners to resolve quality issues.

It is the responsibility of Motorola Supplier Quality Control to ensure that all suppliers maintain an adequate system of process and material controls which provides for prevention (as opposed to detection) of defects in their manufacturing processes. This includes, but is not limited to, the following:

- General plan for continuous improvement
- Detailed product flow
- Process control plan
- Equipment and process capability studies
- Measurement system capability studies
- Specific action plan for out-of-control conditions
- Evidence of statistical process control

Motorola's Reliability and Quality Monitor Philosophy

In order to guarantee that the high standards of reliability and quality required by the Motorola continue throughout the entire production lifetime of each product family, an ongoing Reliability Monitor/Audit Program is established.

Individual product and package family monitors are developed by identifying the appropriate device(s) for each process family (in most cases the same device used to qualify a process/product/package family). Once identified, the appropriate stress test programs are put in place to monitor the ongoing process average of the specific family. This process average measurement is made by understanding the reliability and quality results of individual samples. The stresses and sampling used vary according to the product technologies used and the unique requirements of the customer base. In all cases the monitors have been defined so as to quantify the progress being made toward sector goals of six sigma quality and significant reduction in infant mortality, and long term failure rates.

Monitor testing is completed on an ongoing cycle with test results made available quarterly. These reports detail all test results received for the previous quarter, outlining the reliability data associated with all process/package family types.

With all of these data, an effective ongoing monitor is established which is capable of identifying reliability trends associated with all process/product/package families.

For a complete description, order document BR518/D.

Reliability Stress Tests

The following summary gives brief descriptions of the various reliability tests included in a reliability monitor program. Not all of the tests listed are performed by each product group and other tests can be performed when appropriate. In addition some form of preconditioning may be used in conjunction with the following tests.

HIGH TEMPERATURE OPERATING LIFE

High temperature operating life (HTOL or HTRB) testing is performed to accelerate failure mechanisms which are thermally activated through the application of extreme temperatures and the use of biased operating conditions. The temperature and voltage conditions used in the stress will vary with the product being stressed. However, the typical stress ambient is 125°C, with the bias applied equal to or greater than the data sheet nominal value. All devices used in the HTOL test are sampled directly after final electrical test with no prior burn-in or other prescreening unless called out in the normal production flow. Testing can either be performed with dynamic signals applied to the device or in static bias configuration for a typical test duration of 1008 hours.

TEMPERATURE CYCLE

Temperature cycle accelerates the effects of thermal expansion mismatch among the different components within a specific die and packaging system. This test is typically performed per MIL-STD-883 or MIL-STD-750 with the minimum and maximum temperatures being – 65°C and + 150°C. During temperature cycle testing, devices are inserted into a cycling system and held at the cold dwell temperature for at least ten minutes. Following this cold dwell, the devices are heated to the hot dwell where they remain for another ten minute time period. The system employs a circulating air environment to assure rapid stabilization at the specified temperature. The dwell at each extreme, plus the two transition times of five minutes each (one up to the hot dwell temperature, another down to the cold dwell temperature), constitute one cycle. Test duration for this test will vary with device and packaging system employed. Typical test duration is for 1000 cycles with some tests extended to look for longer term effects.

THERMAL SHOCK

The objective of thermal shock testing is the same as that for temperature cycle testing — to emphasize the differences in expansion coefficients of the packaging system. However, thermal shock provides additional stress in that the device is exposed to a sudden change in temperature due to the transfer time of ten seconds maximum as well as the increased thermal conductivity of a liquid ambient. This test is typically performed per MIL-STD-883 or MIL-STD-750 with minimum and maximum temperatures being – 65°C to + 150°C. Devices are placed in a fluorocarbon bath and cooled to minimum specified temperature. After being held in the cold chamber for five minutes minimum, the devices are transferred to an adjacent chamber filled with fluorocarbon at the maximum specified temperature for an equivalent time. Two five-minute dwells plus two ten-second transitions constitute one cycle. Test duration is for normally 1000 cycles with some tests being extended to look for longer term effects.

TEMPERATURE HUMIDITY BIAS

Temperature humidity bias (THB or H3TRB) is an environmental test performed at a temperature of 85°C and a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated circuits. A nominal static bias is applied to the device to create the electrolytic cells necessary to accelerate corrosion of the metalization. Most groups are tested to 1008 hours, with some groups extended beyond to look for longer term effects.

AUTOCLAVE

Autoclave is an environmental test that measures device resistance to moisture penetration and the resultant effects of galvanic corrosion. Conditions employed during the test include 121°C, 100% relative humidity, and 15 psig. Corrosion of the die is the expected failure mechanism. Autoclave is a highly accelerated and destructive test. Typical test durations are 48 and 96 hours. This test may be followed by HTOL or HTRB for 24 to 48 hours to further accelerate the corrosion failure mechanism.

HAST/PTHB (PRESSURE-TEMPERATURE-HUMIDITY-BIAS)

This test is performed to accelerate the effects of moisture penetration with the dominant effect being corrosion. This test detects similar failure mechanisms as THB, but at a greatly accelerated rate. Conditions usually employed during this test are a temperature of 121°C or greater, pressure of 15 psig or greater, humidity of 100% (PTHB) or humidity of 85% (HAST), and a bias level that is the nominal rating of the device.

CYCLED TEMPERATURE HUMIDITY BIAS

This test is used to examine devices ability to withstand the combined effects of temperature cycling, high humidity, and voltage (test can be run without bias). This test differs from a typical humidity test in its use of temperature cycling. A typical test condition used is as follows: humidity = 90 to 98%, temperature cycle of 25°C to 65°C, and bias applied = nominal device rating. This test is usually run for 1008 hours.

POWER TEMPERATURE CYCLING

This test is performed on semiconductor devices to determine the effects of alternate exposures to extremes of high and low temperature with operating voltages periodically applied and removed. A typical test condition used is as follows: temperature cycle range = – 40°C to 125°C, bias applied = nominal device rating, and power cycling rate = 5.0 minutes (ON)/5 minutes (OFF). This test is usually run for 1000 cycles.

POWER CYCLING

This test is performed at a constant ambient temperature with operating voltage(s) periodically applied and removed, producing a ΔTJA, typically between 50°C and 150°C. Ambient temperatures range between 25°C and 150°C. A typical test condition used is as follows: ambient temperature 25°C, ΔTJA = 125°C with nominal bias, power "ON" 5.0 minutes and "OFF" 5.0 minutes. This test is usually run for at least 504 hours.

LOW TEMPERATURE OPERATING LIFE

This test is performed primarily to accelerate HCI (hot carrier injection) effects in semiconductor devices by exposing them to room ambient or colder temperatures with the use of biased operating conditions. Threshold shifts or parametric changes are typically the basis for failure. The length of this test will vary with temperature and bias conditions employed.

WRITE/ERASE CYCLING OF EEPROMs

This test is employed to evaluate the effects of repeated programming and erasing excursions on EEPROM devices without corruption of data. This write/erase cycling will usually be performed at an elevated operating temperature for greater than 10,000 cycles.

HIGH TEMPERATURE STORAGE/DATA RETENTION

High temperature storage is performed to measure the stability of semiconductor devices, including the data retention characteristics of EPROM and EEPROM devices, during storage at elevated temperatures with no electrical stress applied. The devices are typically exposed to an ambient of 150°C. An acceleration of charge loss from the storage cell or threshold changes are the expected results. All groups are typically tested to 1008 hours.

SYSTEM SOFT ERROR

System soft error is designed to detect errors caused by impact ionization of silicon by high energy particles. This stress is performed on a system level basis. The system is operated for millions of device hours to obtain an accurate measure of actual system soft error performance. This test is performed on memory devices only.

MECHANICAL SHOCK

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to examine the ability of the device to withstand a sudden change in mechanical stress typically due to abrupt changes in motion as seen in handling, transportation, or actual use. A typical test condition would be as follows: acceleration = 1500 g, orientation = Y1 plane, t = 0.5 ms, and number of pulse = 5.

VARIABLE FREQUENCY VIBRATION

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to examine the ability of the device to withstand deterioration due to mechanical resonance. A typical test condition is: peak acceleration = 20 g, frequency range = 20 Hz to 20 kHz, and t = 48 minutes.

CONSTANT ACCELERATION

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to indicate structural or mechanical weaknesses in a device/packaging system by applying a severe mechanical stress. A typical test condition used is as follows: stress level = 30 kg, orientation = Y1 plane, and t = 1 minute.

SOLDER HEAT

This test is used to examine the device's ability to withstand the temperatures seen in soldering over a more extended period as compared to the typical exposure levels seen in a production process. Electrical testing is the endpoint criterion for this stress.

LEAD INTEGRITY

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to examine the mechanical properties of a device's leads, welds, and seals. Various conditions can be employed and provide for: tensile loading, bending stresses, torque or twist, and peel stress. The failure is determined visually under 3X to 10X magnification.

SALT ATMOSPHERE

This test is performed per MIL-STD-883 or MIL-STD-750 and is used to evaluate the corrosive effects of a seacoast type atmosphere on device and package elements. A failure is determined visually under 10X to 20X magnification.

Mechanical Data

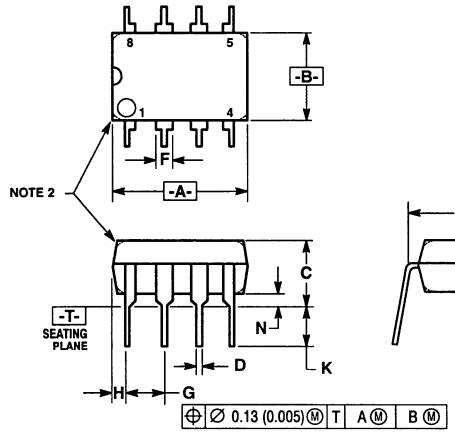
8

Mechanical Data

The package availability for each device is indicated on the front page of the individual data sheets. Dimensions for the packages are given in this chapter.

8-PIN PACKAGES

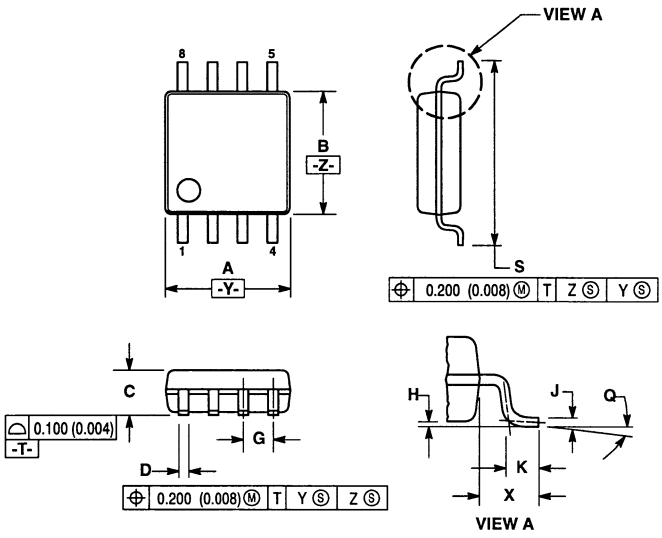
PLASTIC PACKAGE
CASE 626-05



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

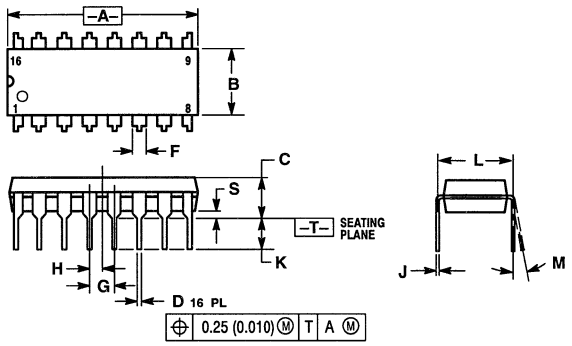
SOG PACKAGE
CASE 904–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.150 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.100	5.450	0.201	0.214
B	5.100	5.400	0.201	0.216
C	—	2.050	—	0.080
D	0.350	0.500	0.014	0.001
G	1.270 BSC		0.050 BSC	
H	0.050	0.200	0.002	0.007
J	0.180	0.270	0.008	0.010
K	0.500	0.850	0.020	0.033
Q	0°	10°	0°	10°
S	7.400	8.200	0.292	0.322
X	1.260 REF		0.0496 REF	

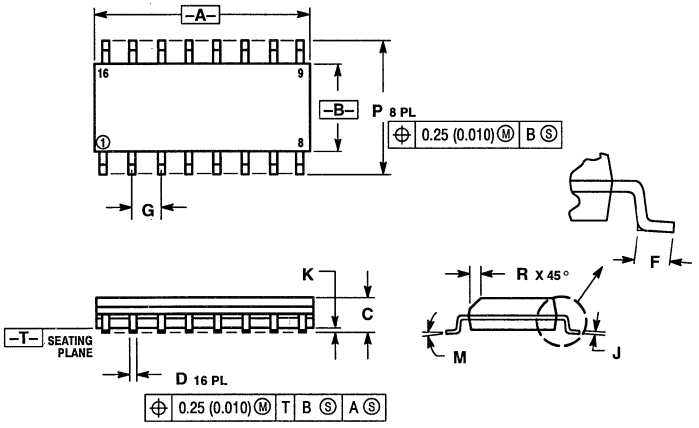
PLASTIC PACKAGE
CASE 648-08



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SOIC PACKAGE
CASE 751B-05



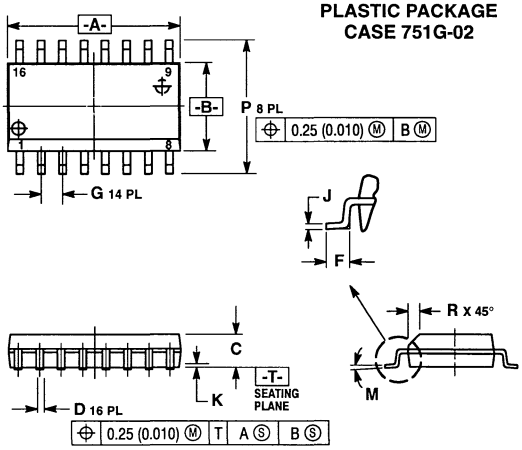
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

8

16-PIN PACKAGES

PLASTIC PACKAGE
CASE 751G-02

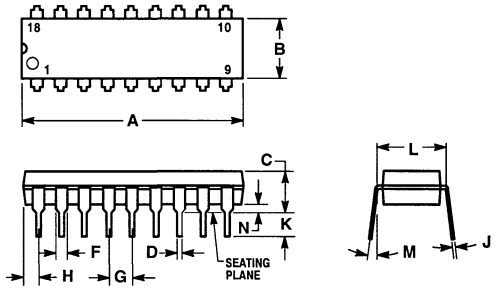


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

18-PIN PACKAGES

PLASTIC PACKAGE
CASE 707-02



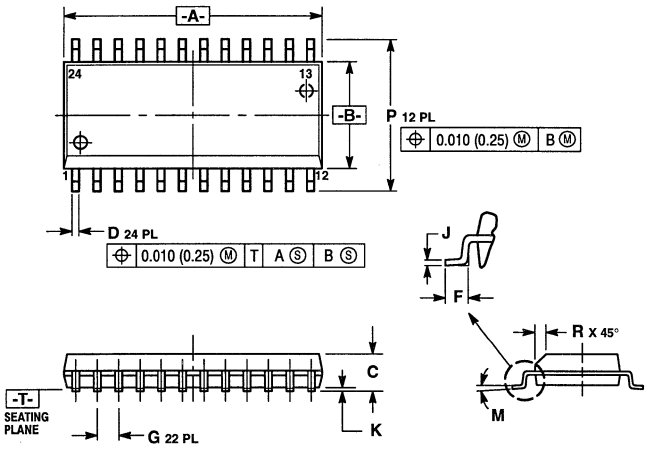
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

8

24-PIN PACKAGES

SOG PACKAGE
CASE 751E-04

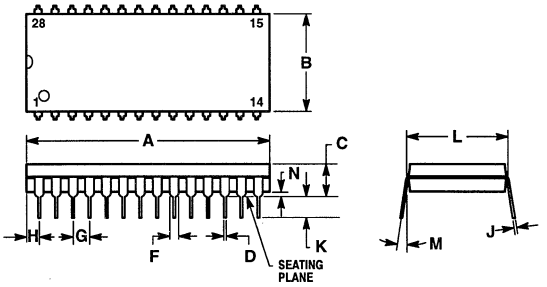


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

28-PIN PACKAGES

PLASTIC PACKAGE
CASE 710-02

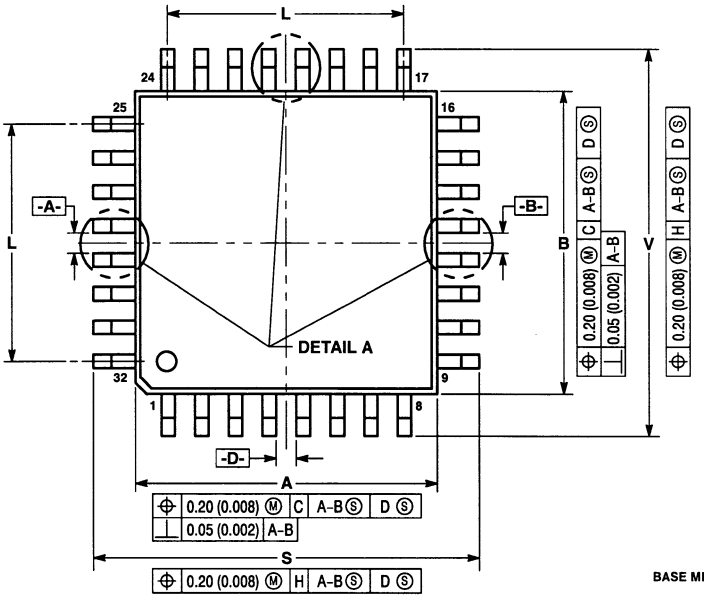


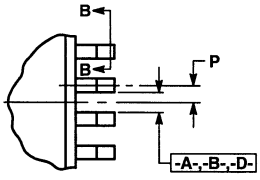
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

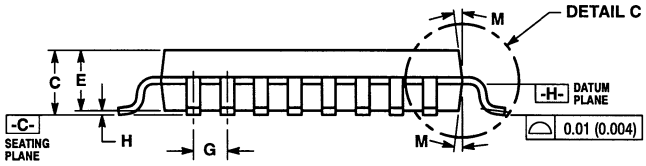
8

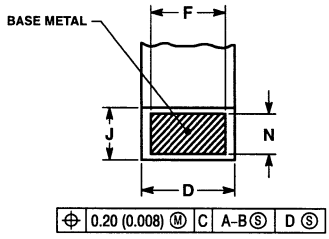
QUAD FLAT PACK (QFP)
CASE 873–01



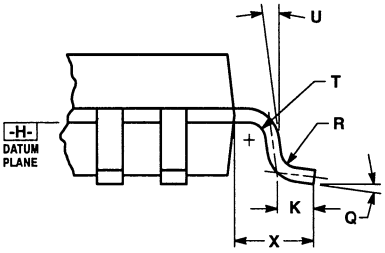


DETAIL A





SECTION B-B
VIEW ROTATED 90° CLOCKWISE



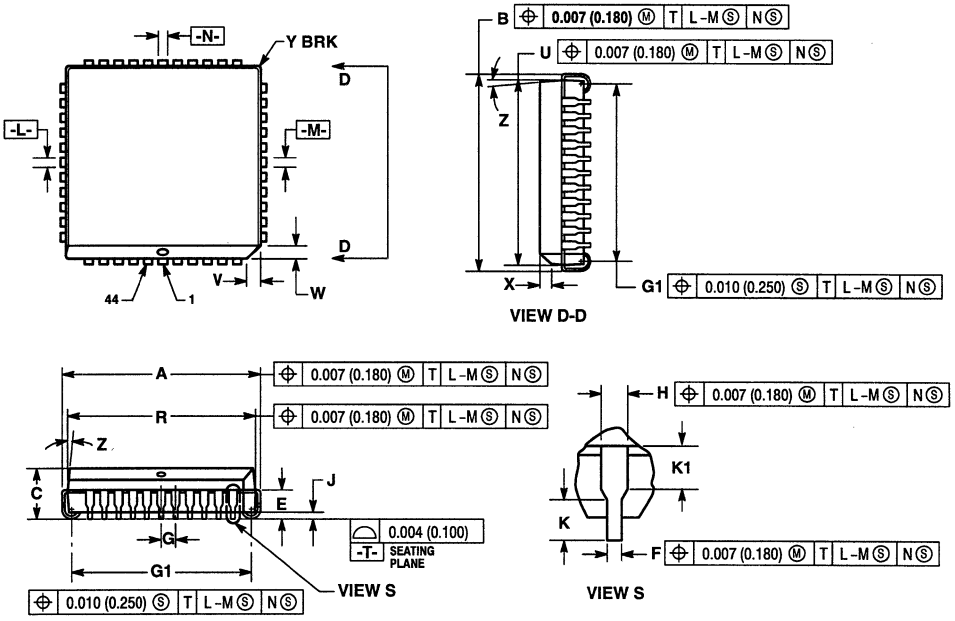
DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	—	0.010	—
G	0.80 BSC		0.031 BSC	
H	—	0.20	—	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF		0.220 REF	
M	6°	8°	6°	8°
N	0.119	0.135	0.005	0.005
P	0.40 BSC		0.016 BSC	
Q	5°	10°	5°	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5°	11°	5°	11°
V	8.85	9.15	0.348	0.360
X	1.0 REF		0.039 REF	

8

PLCC PACKAGE
CASE 777-02

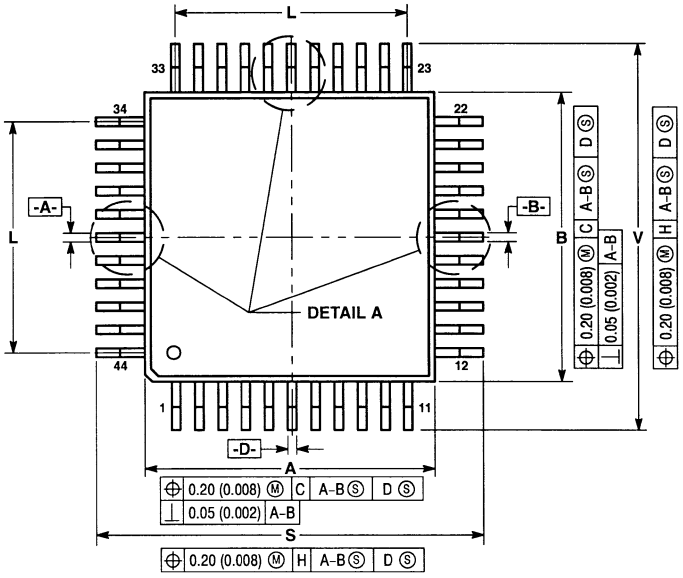


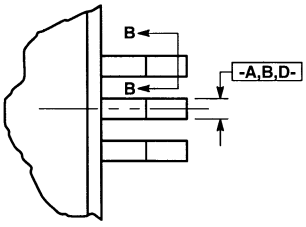
NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS (0.010) 0.25 PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.610	0.630	15.50	16.00
K1	0.040	—	1.02	—

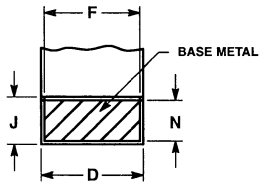
8

QUAD FLAT PACKAGE (QFP)
CASE 824A–01

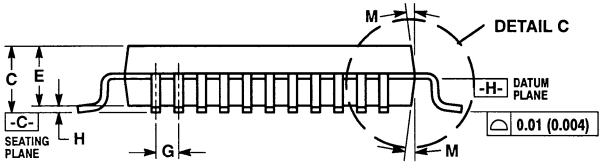


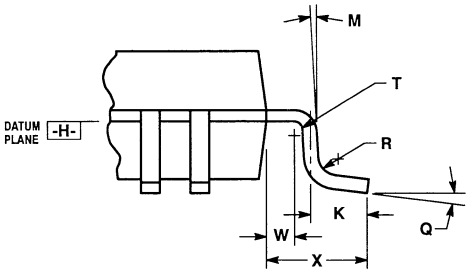


DETAIL A



SECTION B–B





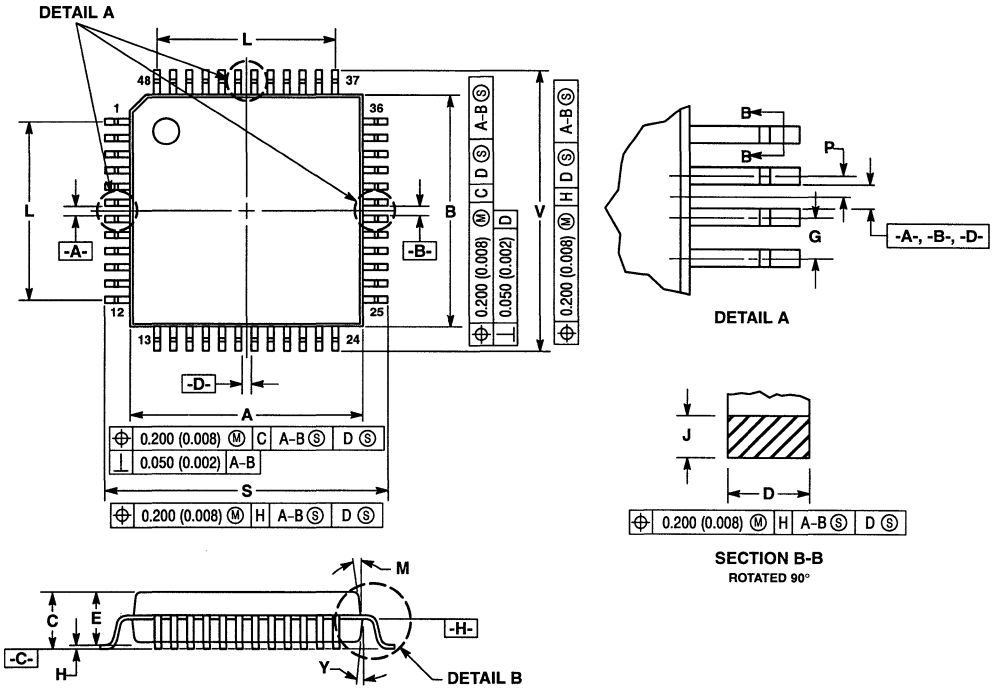
DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.30	0.45	0.012	0.018
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	8.00 REF		0.315 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	—	0.005	—
U	0°	—	0°	—
V	12.95	13.45	0.510	0.530
W	0.40	—	0.016	—
X	1.6 REF		0.063 REF	

8

QUAD FLAT PACKAGE (QFP)
CASE 898–01

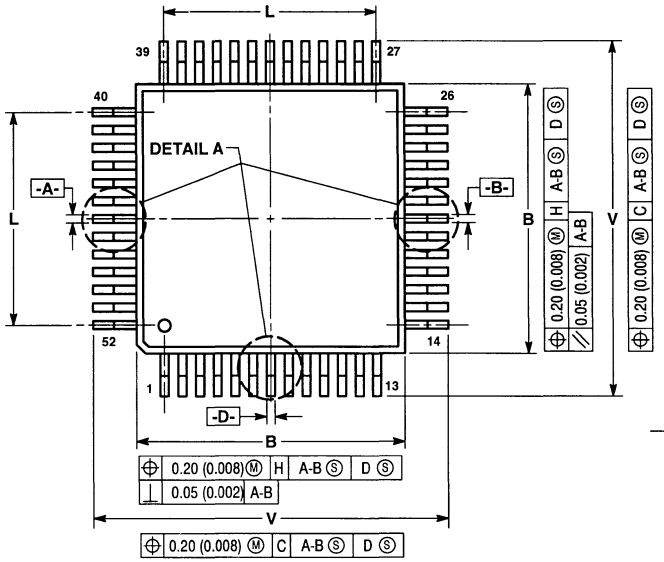


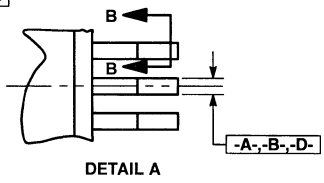
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.48 (0.019).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	11.90	12.10	0.469	0.476
B	11.90	12.10	0.469	0.476
C	2.05	2.55	0.026	0.041
D	0.20	0.40	0.081	0.100
E	2.00	2.30	0.079	0.091
G	0.80 BSC		0.031 BSC	
H	0.00	0.30	0.000	0.011
J	0.10	0.20	0.005	0.008
K	0.65	1.05	0.026	0.041
L	8.80 BSC		0.346 BSC	
M	13° REF		13° REF	
P	0.40 BSC		0.016 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.006	0.011
S	14.90	15.70	0.587	0.618
V	14.90	15.70	0.587	0.618
W	0.65 REF		0.026 REF	
X	1.60 REF		0.063 REF	
Y	5° REF		5° REF	

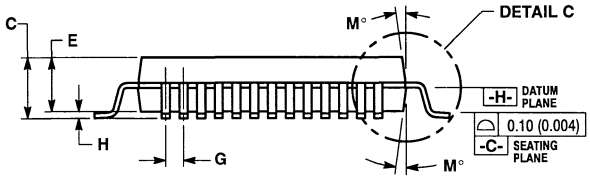
8

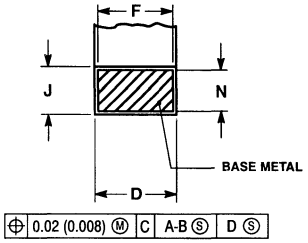
QUAD FLAT PACKAGE (QFP)
CASE 848B–04



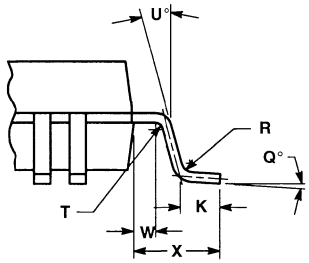


DETAIL A





SECTION B-B



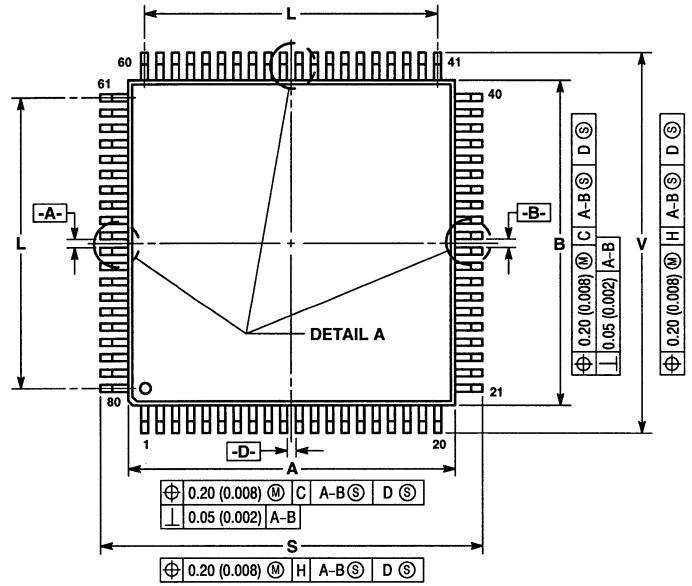
DETAIL C

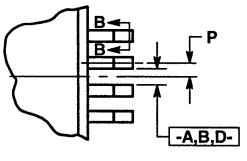
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.22	0.38	0.009	0.015
E	2.00	2.10	0.079	0.083
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	7.80 REF		0.307 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	—	0.005	—
U	0°	—	0°	—
V	12.95	13.45	0.510	0.530
W	0.35	0.45	0.014	0.018
X	1.6 REF		0.063 REF	

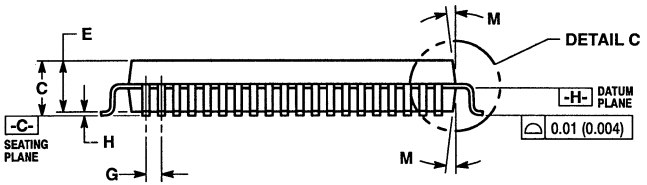
8

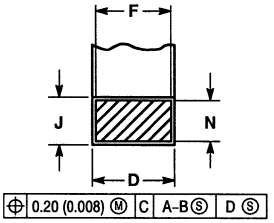
QUAD FLAT PACK (QFP)
CASE 841B–01



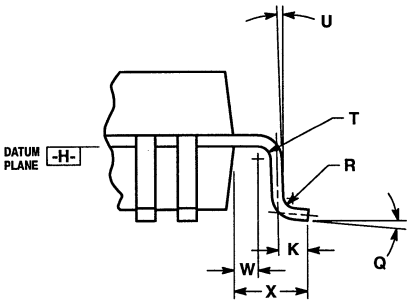


DETAIL A





SECTION B-B



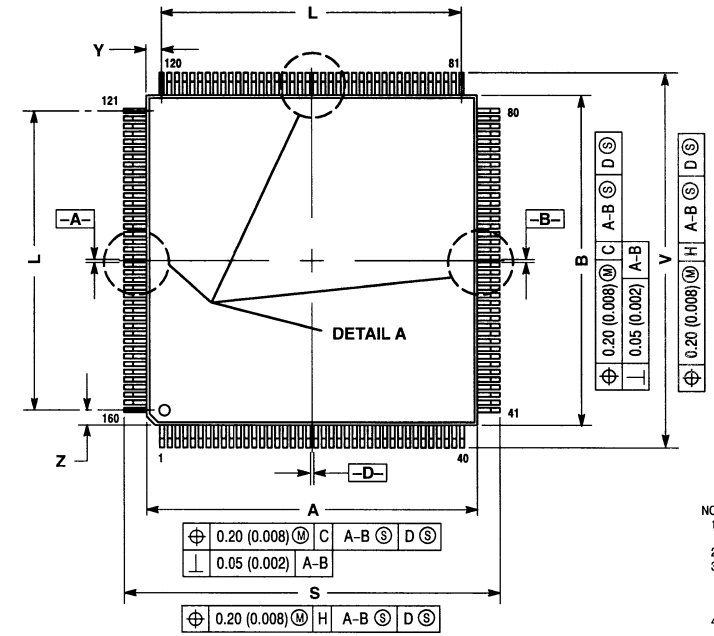
DETAIL C

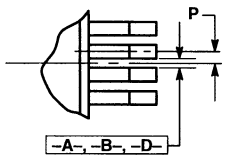
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	13.90	14.10	0.547	0.555
B	13.90	14.10	0.547	0.555
C	2.15	2.45	0.084	0.096
D	0.22	0.38	0.009	0.015
E	2.00	2.40	0.079	0.094
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	12.35 BSC		0.486 BSC	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
P	0.325 BSC		0.013 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	16.95	17.45	0.667	0.687
T	0.13	—	0.005	—
U	0°	—	0°	—
V	16.95	17.45	0.667	0.687
W	0.35	0.45	0.014	0.018
X	1.6 REF		0.06 REF	

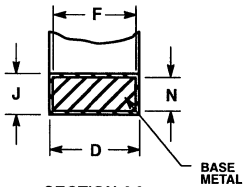
8

QUAD FLAT PACK (QFP)
CASE 1007–01



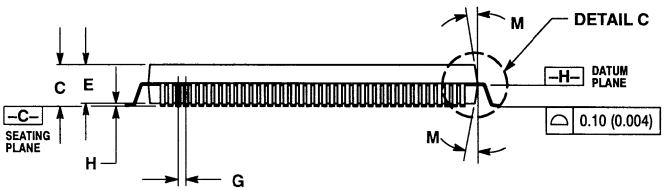


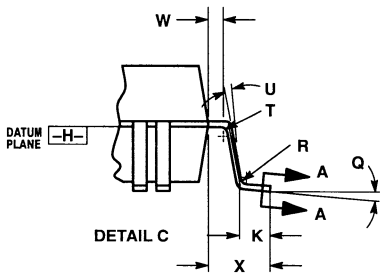
DETAIL A



SECTION AA

⊕	0.08 (0.003) M	C	A-B S	D S





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD, WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.45	3.85	0.136	0.152
D	0.28	0.38	0.011	0.015
E	3.20	3.56	0.126	0.140
F	0.28	0.34	0.011	0.013
G	0.65 BSC		0.0256 BSC	
H	0.25	0.35	0.010	0.014
J	0.11	0.18	0.0043	0.0071
K	0.70	0.90	0.027	0.036
L	25.35 REF		0.998 REF	
M	5°	9°	5°	9°
N	0.11	0.14	0.0043	0.0055
P	0.325 BSC		0.0128 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.00	31.40	1.220	1.236
T	0.13	---	0.005	---
U	0°	---	0°	---
V	31.00	31.40	1.220	1.236
W	0.40	---	0.016	---
X	1.60 REF		0.063 REF	
Y	1.325 REF		0.0522 REF	
Z	1.325 REF		0.0522 REF	

8

MOTOROLA DISTRIBUTOR AND WORLDWIDE SALES OFFICES

AUTHORIZED NORTH AMERICAN DISTRIBUTORS

UNITED STATES

ALABAMA

Huntsville
- Arrow/Schweber Electronics .... (205)837-6955
- Future Electronics ..... (205)830-2322
- Hamilton Hallmark ..... (205)837-8700
- Newark ..... (205)837-9091
- Time Electronics 1-800-789-TIME
- Wyle Laboratories ..... (205)830–1119

ARIZONA

Phoenix
- Future Electronics ..... (602)968-7140
- Hamilton Hallmark ..... (602)437-1200
- Newark Electronics ..... (602)864-9905
- Wyle Laboratories ..... (602)437-2088

Tempe
- Arrow/Schweber Electronics .... (602)431-0030
- Time Electronics 1-800-789-TIME

CALIFORNIA

Agoura Hills
- Time Electronics Corporate 1-800-789-TIME

Belmont
- Richardson Electronics ..... (415)592-9225

Calabassas
- Arrow/Schweber Electronics .... (818)880-9686
- Wyle Laboratories ..... (818)880-9000

Chatsworth
- Future Electronics ..... (818)865-0040
- Time Electronics 1-800-789-TIME

Costa Mesa
- Hamilton Hallmark ..... (714)641-4100

Culver City
- Hamilton Hallmark ..... (213)558-2000

Irvine
- Arrow/Schweber Electronics ... (714)587-0404
- Future Electronics ..... (714)250-4141
- Wyle Laboratories Corporate .... (714)753-9953
- Wyle Laboratories ..... (714)863-9953

Los Angeles
- Wyle Laboratories ..... (818)880-9000

Mountain View
- Richardson Electronics ..... (415)960-6900

Orange
- Newark ..... (714)634-8224

Rocklin
- Hamilton Hallmark ..... (916)624-9781

Sacramento
- Newark ..... (916)721-1633
- Wyle Laboratories ..... (916)638-5282

San Diego
- Arrow/Schweber Electronics ... (619)565-4800
- Future Electronics ..... (619)625-2800
- Hamilton Hallmark ..... (619)571-7540
- Newark ..... (619)569-9877
- Wyle Laboratories ..... (619)565-9171

San Francisco
- Newark ..... (415)571-5300

San Jose
- Arrow/Schweber Electronics .... (408)441-9700
- Arrow/Schweber Electronics .... (408)428-6400
- Future Electronics ..... (408)434-1122

Santa Clara
- Wyle Laboratories ..... (408)727-2500

Sunnyvale
- Hamilton Hallmark ..... (408)435-3500
- Time Electronics 1-800-789-TIME

Torrance
- Time Electronics 1-800-789-TIME

Tustin
- Time Electronics 1-800-789-TIME

West Hills
- Newark ..... (818)888-3718

Woodland Hills
- Hamilton Hallmark ..... (818)594-0404
- Richardson Electronics ..... (615)594-5600

COLORADO

Lakewood
- Future Electronics ..... (303)232-2008

Colorado Springs
- Newark ..... (719)592-9494

Denver
- Newark ..... (303)757-3351

Englewood
- Arrow/Schweber Electronics .... (303)799-0258
- Hamilton Hallmark ..... (303)790-1662
- Time Electronics 1-800-789-TIME

Thornton
- Wyle Laboratories ..... (303)457-9953

CONNECTICUT

Chesire
- Future Electronics ..... (203)250-0083
- Hamilton Hallmark ..... (203)271-2844

Southbury
- Time Electronics 1-800-789-TIME

Wallingfort
- Arrow/Schweber Electronics .... (203)265-7741

Windsor
- Newark ..... (203)683-8860

FLORIDA

Altamonte Springs
- Future Electronics ..... (407)767-8414

Clearwater
- Future Electronics ..... (813)530-1222

Deerfield Beach
- Arrow/Schweber Electronics .... (305)429-8200
- Wyle Laboratories ..... (305)420-0500

Ft. Lauderdale
- Future Electronics ..... (305)436-4043
- Hamilton Hallmark ..... (305)484-5482
- Time Electronics 1-800-789-TIME

Lake Mary
- Arrow/Schweber Electronics .... (407)333-9300

Largo/Tampa/St. Petersburg
- Hamilton Hallmark ..... (813)541-7440
- Newark ..... (813)287-1578
- Wyle Laboratories ..... (813)576-3004

Orlando
- Newark ..... (407)896-8350
- Time Electronics 1-800-789-TIME

Plantation
- Newark ..... (305)424-4400

Winter Park
- Hamilton Hallmark ..... (407)657-3300
- Richardson Electronics ..... (407)644-1453

GEORGIA

Atlanta
- Time Electronics 1-800-789-TIME
- Wyle Laboratories ..... (404)441-9045

Duluth
- Arrow/Schweber Electronics .... (404)497-1300
- Hamilton Hallmark ..... (404)623-5475

Norcross
- Future Electronics ..... (404)441-7676
- Newark ..... (404)448-1300
- Wyle Laboratories ..... (404)441-9045

ILLINOIS

Addison
- Wyle Laboratories ..... (708)620-0969

Bensenville
- Hamilton Hallmark ..... (708)860-7780

Chicago
- Newark Electronics Corp. ..... (312)784-5100

Hoffman Estates
- Future Electronics ..... (708)882-1255

Itasca
- Arrow/Schweber Electronics ... (708)250-0500

LaFox
- Richardson Electronics ..... (708)208-2401

Schaumburg
- Newark ..... (708)310-8980
- Time Electronics 1-800-789-TIME

INDIANA

Indianapolis
- Arrow/Schweber Electronics .... (317)299-2071
- Hamilton Hallmark ..... (317)872-8875
- Newark ..... (317)259-0085
- Time Electronics 1-800-789-TIME

Ft. Wayne
- Newark ..... (219)484-0766

IOWA

Cedar Rapids
- Newark ..... (319)393-3800
- Time Electronics 1-800-789-TIME

KANSAS

Lenexa
- Arrow/Schweber Electronics .... (913)541-9542
- Hamilton Hallmark ..... (913)888-4747

Overland Park
- Future Electronics ..... (913)649-1531
- Newark ..... (913)677-0727
- Time Electronics 1-800-789-TIME

MARYLAND

Beltsville
- Newark ..... (301)604-1700

Columbia
- Arrow/Schweber Electronics .... (301)596-7800
- Future Electronics ..... (410)290-0600
- Hamilton Hallmark ..... (410)988-9800
- Time Electronics 1-800-789-TIME
- Wyle Laboratories ..... (410)312-4844

MASSACHUSETTS

Boston
- Arrow/Schweber Electronics .... (617)271-9953

Bolton
- Future Corporate ..... (508)779-3000

Burlington
- Wyle Laboratories ..... (617)271-9953

Methuen
- Newark ..... (508)683-0913

Norwell
- Richardson Electronics ..... (617)871-5162

Peabody
- Time Electronics 1-800-789-TIME
- Hamiltion Hallmark ..... (508)532-3701

MICHIGAN

Detroit
- Newark ..... (313)967-0600

Grand Rapids
- Future Electronics ..... (616)698-6800

Livonia
- Arrow/Schweber Electronics .... (313)462-2290
- Future Electronics ..... (313)261-5270
- Hamilton Hallmark ..... (313)347-4020
- Time Electronics 1-800-789-TIME

MINNESOTA

Bloomington
- Wyle Laboratories ..... (612)853-2280

Eden Prairie
- Arrow/Schweber Electronics .... (612)941-5280
- Future Electronics ..... (612)944-2200
- Hamilton Hallmark ..... (612)881-2600
- Time Electronics 1-800-789-TIME

Minneapolis
- Newark ..... (612)331-6350

Earth City
- Hamilton Hallmark ..... (314)291-5350

For changes to this information contact Technical Publications at FAX (602) 244-6561

AUTHORIZED DISTRIBUTORS – continued

UNITED STATES – continued

MISSOURI

St. Louis
- Arrow/Schweber Electronics .... (314)567-6888
- Future Electronics ..... (314)469-6805
- Newark ..... (314)298-2505
- Time Electronics 1-800-789-TIME

NEW JERSEY

Cherry Hill
- Hamilton Hallmark ..... (609)424-0100

Fairfield
- Newark ..... (201)882-0300

Marlton
- Arrow/Schweber Electronics .... (609)596-8000
- Future Electronics ..... (609)596-4080

Pinebrook
- Arrow/Schweber Electronics .... (201)227-7880
- Wyle Laboratories ..... (201)882-8358

Parsippany
- Future Electronics ..... (201)299-0400
- Hamilton Hallmark ..... (201)515-1641

Wayne
- Time Electronics 1-800-789-TIME

NEW MEXICO

Albuquerque
- Alliance Electronics ..... (505)292-3360
- Hamilton Hallmark ..... (505)828-1058
- Newark ..... (505)828-1878

NEW YORK

Commack
- Newark ..... (516)499-1216

Hauppauge
- Arrow/Schweber Electronics .... (516)231-1000
- Future Electronics ..... (516)234-4000
- Hamilton Hallmark ..... (516)434-7400

Konkoma
- Hamilton Hallmark ..... (516)737-0600

Melville
- Wyle Laboratories ..... (516)293-8446

Pittsford
- Newark ..... (716)381-4244

Rochester
- Arrow/Schweber Electronics .... (716)427-0300
- Future Electronics ..... (716)272-1120
- Hamilton Hallmark ..... (716)475-9130
- Richardson Electronics ..... (716)264-1100
- Time Electronics 1-800-789-TIME

Rockville Centre
- Richardson Electronics ..... (516)872-4400

Syracuse
- Future Electronics ..... (315)451-2371
- Time Electronics 1-800-789-TIME

NORTH CAROLINA

Charlotte
- Future Electronics ..... (704)455-9030
- Richardson Electronics ..... (704)548-9042

Greensboro
- Newark ..... (919)292-7240

Raleigh
- Arrow/Schweber Electronics .... (919)876-3132
- Future Electronics ..... (919)790-7111
- Hamilton Hallmark ..... (919)872-0712
- Time Electronics 1-800-789-TIME

OHIO

Centerville
- Arrow/Schweber Electronics .... (513)435-5563

Cleveland
- Newark ..... (216)391-9330
- Time Electronics 1-800-789-TIME

Columbus
- Newark ..... (614)431-0809
- Time Electronics 1-800-789-TIME

Dayton
- Future Electronics ..... (513)426-0090
- Hamilton Hallmark ..... (513)439-6735
- Newark ..... (513)294-8980
- Time Electronics 1-800-789-TIME

Mayfield Heights
- Future Electronics ..... (216)449-6996

Solon
- Arrow/Schweber Electronics .... (216)248-3990
- Hamilton Hallmark ..... (216)498-1100

Worthington
- Hamilton Hallmark ..... (614)888-3313

OKLAHOMA

Tulsa
- Hamilton Hallmark ..... (918)254-6110
- Newark ..... (918)252-5070

OREGON

Beaverton
- Arrow/Almac Electronics Corp. .. (503)629-8090
- Future Electronics ..... (503)645-9454
- Hamilton Hallmark ..... (503)528-6200
- Wyle Laboratories ..... (503)643-7900

Portland
- Newark ..... (503)297-1984
- Time Electronics 1-800-789-TIME

PENNSYLVANIA

King of Prussia
- Newark ..... (215)265-0933

Mt. Laurel
- Wyle Laboratories ..... (609)439-9110

Montgomeryville
- Richardson Electronics ..... (215)628-0805

Philadelphia
- Time Electronics 1-800-789-TIME
- Wyle Laboratories ..... (609)439-9110

Pittsburgh
- Arrow/Schweber Electronics .... (412)963-6807
- Newark ..... (412)788-4790
- Time Electronics 1-800-789-TIME

TENNESSEE

Franklin
- Richardson Electronics ..... (615)791-4900

Knoxville
- Newark ..... (615)588-6493

TEXAS

Austin
- Arrow/Schweber Electronics .... (512)835-4180
- Future Electronics ..... (512)502-0991
- Hamilton Hallmark ..... (512)258-8818
- Newark ..... (512)338-0287
- Time Electronics 1-800-789-TIME
- Wyle Laboratories ..... (512)345-8853

Carollton
- Arrow/Schweber Electronics .... (214)380-6464

Dallas
- Future Electronics ..... (214)437-2437
- Hamilton Hallmark ..... (214)553-4300
- Richardson Electronics ..... (214)239-3680
- Time Electronics 1-800-789-TIME
- Wyle Laboratories ..... (214)235-9953

Ft. Worth
- Allied Electronics ..... (817)336-5401

Houston
- Arrow/Schweber Electronics .... (713)530-4700
- Future Electronics ..... (713)785-1155
- Hamilton Hallmark ..... (713)781-6100
- Newark ..... (713)270-4800
- Time Electronics 1-800-789-TIME
- Wyle Laboratories ..... (713)879-9953

Richardson
- Newark ..... (214)235-1998

UTAH

Salt Lake City
- Arrow/Schweber Electronics .... (801)973-6913
- Future Electronics ..... (801)467-4448
- Hamilton Hallmark ..... (801)266-2022
- Newark ..... (801)261-5660
- Wyle Laboratories ..... (801)974–9953

West Valley City
- Time Electronics 1-800-789-TIME
- Wyle Laboratories ..... (801)974-9953

WASHINGTON

Bellevue
- Almac Electronics Corp. ..... (206)643-9992
- Newark ..... (206)641-9800
- Richardson Electronics ..... (206)646-7224

Bothell
- Future Electronics ..... (206)489-3400

Redmond
- Hamilton Hallmark ..... (206)881-6697
- Time Electronics 1-800-789-TIME
- Wyle Laboratories ..... (206)881-1150

Seattle
- Wyle Laboratories. ..... (206)881-1150

Spokane
- Arrow/Almac Electronics Corp. .. (509)924-9500

WISCONSIN

Brookfield
- Arrow/Schweber Electronics .... (414)792-0150
- Future Electronics ..... (414)879-0244

Milwaukee
- Time Electronics 1-800-789-TIME

New Berlin
- Hamilton Hallmark ..... (414)780-7200

Wauwatosa
- Newark ..... (414)453-9100

Waukesha
- Wyle Laboratories ..... (414)879-0434

CANADA

ALBERTA

Calgary
- Electro Sonic Inc. ..... (403)255-9550
- Future Electronics ..... (403)250-5550
- Hamilton/Hallmark ..... (800)663–5500

Edmonton
- Future Electronics ..... (403)438-2858
- Hamilton/Hallmark ..... (800)663-5500

Saskatchewan
- Hamilton/Hallmark ..... (800)663–5500

BRITISH COLUMBIA

Vancouver
- Arrow Electronics ..... (604)421-2333
- Electro Sonic Inc. ..... (604)273-2911
- Future Electronics ..... (604)294-1166
- Hamilton/Hallmark ..... (604)420-4101

MANITOBA

Winnipeg
- Electro Sonic Inc. ..... (204)783-3105
- Future Electronics ..... (204)944-1446
- Hamilton/Hallmark ..... (800)663-5500

ONTARIO

Ottawa
- Arrow Electronics ..... (613)226-6903
- Electro Sonic Inc. ..... (613)728-8333
- Future Electronics ..... (613)820-8313
- Hamilton/Hallmark ..... (613)226-1700

Toronto
- Arrow Electronics ..... (905)670-7769
- Electro Sonic Inc. ..... (416)494-1666
- Future Electronics ..... (905)612-9200
- Hamilton Hallmark ..... (905)564-6060
- Newark ..... (519)685–4280
  (905)670–2888
  (800)463–9275
- Richardson Electronics ..... (905)795–6300
- FAI ..... (905)612–9888

QUEBEC

Montreal
- Arrow Electronics ..... (514)421-7411
- Future Electronics ..... (514)694-7710
- Hamilton Hallmark ..... (514)335-1000
- Newark ..... (800)463-9275
- Richardson Electronics ..... (514)748–1770

Quebec City
- Future Electronics ..... (418)877-6666

SALES OFFICES

UNITED STATES

ALABAMA, Huntsville ..... (205)464-6800
ALASKA, ... (800)635-8291
ARIZONA, Tempe ..... (602)302-8056
CALIFORNIA, Agoura Hills ... (818)706-1929
CALIFORNIA, Los Angeles .. (310)417-8848
CALIFORNIA, Irvine ..... (714)753-7360
CALIFORNIA, San Diego .... (619)541-2163
CALIFORNIA, Sunnyvale .... (408)749-0510
COLORADO,
Colorado Springs ..... (719)599-7497
COLORADO, Denver ..... (303)337-3434
CONNECTICUT,
Wallingford ..... (203)949-4100
FLORIDA, Maitland ..... (407)628-2636
FLORIDA, Pompano Beach/
Ft. Lauderdale ..... (305)351-6040
FLORIDA, Clearwater ..... (813)538-7750
GEORGIA, Atlanta ..... (404)729-7100
IDAHO, Boise ..... (208)323-9413
ILLINOIS, Chicago/
Hoffman Estates ..... (708)413-2500
Shaumburg ..... (708)413-2500
INDIANA, Fort Wayne ..... (219)436-5818
INDIANA, Indianapolis ..... (317)571-0400
INDIANA, Kokomo ..... (317)455-5100
IOWA, Cedar Rapids ..... (319)378-0383
KANSAS, Kansas City/
Mission ..... (913)451-8555
MARYLAND, Columbia ..... (410)381-1570
MASSACHUSETTS,
Marlborough ..... (508)481-8100
MASSACHUSETTS,
Woburn ..... (617)932-9700
MICHIGAN, Detroit ..... (313)347-6800
MINNESOTA, Minnetonka .... (612)932-1500
MISSOURI, St. Louis ..... (314)275-7380
NEW JERSEY, Fairfield ..... (201)808-2400
NEW YORK, Fairport ..... (716)425-4000
NEW YORK, Hauppauge .... (516)361-7000
NEW YORK, Fishkill ..... (914)896-0511
NORTH CAROLINA,
Raleigh ..... (919)870-4355
OHIO, Cleveland ..... (216)349-3100
OHIO, Columbus/
Worthington ..... (614)431-8492
OHIO, Dayton ..... (513)495-6800
OKLAHOMA, Tulsa ..... (800)544-9496
OREGON, Portland ..... (503)641-3681
PENNSYLVANIA, Colmar .... (215)997-1020
Philadelphia/Horsham ..... (215)957-4100
TENNESSEE, Knoxville ..... (615)690-5593
TEXAS, Austin ..... (512)502-2100
TEXAS, Houston ..... (800)343-2692
TEXAS, Plano ..... (214)516-5100
TEXAS, Seguin ..... (210)372-7620
VIRGINIA, Richmond ..... (804)285-2100
UTAH, CSI @ ..... (801)561-5099
WASHINGTON, Bellevue .... (206)454-4160
Seattle Access ..... (206)622-9960
WISCONSIN, Milwaukee/
Brookfield ..... (414)792-0122

Field Applications Engineering Available
Through All Sales Offices

CANADA

BRITISH COLUMBIA,
Vancouver ..... (604)293-7650
ONTARIO, Toronto ..... (416)497-8181
ONTARIO, Ottawa ..... (613)226-3491
QUEBEC, Montreal ..... (514)333-3300

INTERNATIONAL

AUSTRALIA, Melbourne ... (61-3)887-0711
AUSTRALIA, Sydney ..... 61(2)906-3855
BRAZIL, Sao Paulo ..... 55(11)815-4200
CHINA, Beijing 86-505-2180
FINLAND, Helsinki 358-0-351 61191
car phone ..... 358(49)211501
FRANCE, Paris 33134 635900
GERMANY, Langenhagen/
Hannover ..... 49(511)786880
GERMANY, Munich 49 89 92103-0
GERMANY, Nuremberg 49 911 96-3190
GERMANY, Sindelfingen 49 7031 79 710
GERMANY, Wiesbaden 49 611 973050
HONG KONG, Kwai Fong 852-6106888
Tai Po 852-6668333
INDIA, Bangalore ..... (91-812)627094
ISRAEL, Herzlia 972–9–590222
ITALY, Milan ..... 39(2)82201
JAPAN, Fukuoka 81-92–725–7583
JAPAN, Gotanda 81-3-5487-8311
JAPAN, Nagoya 81-52-232-3500
JAPAN, Osaka 81-6-305-1802
JAPAN, Sendai 81-22-268-4333
JAPAN, Takamatsu 81-878-37-9972
JAPAN, Tokyo 81-3-3440-3311
KOREA, Pusan ..... 82(51)4635-035
KOREA, Seoul ..... 82(2)554-5118
MALAYSIA, Penang ..... 60(4)374514
MEXICO, Mexico City ..... 52(5)282-0230
MEXICO, Guadalajara ..... 52(36)21-8977
Marketing ..... 52(36)21-2023
Customer Service ..... 52(36)669-9160
NETHERLANDS, Best .... (31)4998 612 11
PUERTO RICO, San Juan ... (809)793-2170
SINGAPORE ..... (65)4818188
SPAIN, Madrid ..... 34(1)457-8204
or ..... 34(1)457-8254
SWEDEN, Solna ..... 46(8)734-8800
SWITZERLAND, Geneva .. 41(22)799 11 11
SWITZERLAND, Zurich ..... 41(1)730-4074
TAIWAN, Taipei ..... 886(2)717-7089
THAILAND, Bangkok ..... 66(2)254-4910
UNITED KINGDOM,
Aylesbury ..... 44(296)395-252

FULL LINE REPRESENTATIVES

CALIFORNIA, Loomis
Galena Technology Group ... (916)652-0268
NEVADA, Reno
Galena Tech. Group ..... (702)746-0642
NEW MEXICO, Albuquerque
S&S Technologies, Inc. .... (505)298-7177
UTAH, Salt Lake City
Utah Comp. Sales, Inc. ..... (801)561-5099
WASHINGTON, Spokane
Doug Kenley ..... (509)924-2322

HYBRID/MCM COMPONENT SUPPLIERS

Chip Supply ..... (407)298-7100
Elmo Semiconductor ..... (818)768-7400
Minco Technology Labs Inc. .. (512)834-2022
Semi Dice Inc. ..... (310)594-4631

SALES OFFICES
INTERNATIONAL MOTOROLA DISTRIBUTOR AND SALES OFFICES
AUTHORIZED DISTRIBUTORS

AUSTRALIA
VSI Electronics (NZ) Ltd ..... (64)9 579-6603
VSI Promark Elec. Pty Ltd ..... (61)2 439-4655
Veltek Pty Ltd ..... (61)3 808-7511

AUSTRIA
EBV Austria ..... (43) 222 894 1774
Elbatex GmbH ..... (43) 222 86 3211

BENELUX
Diode Belgium ..... (32) 2 725 4660
Diode Components BV ..... (31) 340 29 1234
EBV Belgium ..... (32) 2 720 9936
EBV Holland ..... (31) 3465 623 53
Rodelco Electronics ..... (31) 767 84911
Rodelco N.V. ..... (32) 2 460 0560

CHINA
Advanced Electronics Ltd. ..... (852)305-3633
China El. App. Corp. Xiamen Co. .. (86)592 553-487
Nanco Electronics Supply Ltd. ..... (852) 333-5121
Qing Cheng Enterprises Ltd. .... (852) 493-4202

DENMARK
Avnet Nortec A/S Denmark ..... (45) 428 42000
EBV Denmark ..... (45) 398 905 11

FINLAND
Arrow Field OY ..... (35) 807 775 71

FRANCE
Arrow Electronique ..... (33) 1 49 78 49 78
Avnet Components ..... (33) 1 49 65 25 00
EBV France ..... (33) 1 64 68 86 00
Scaib ..... (33) 1 46 87 23 13

GERMANY
Avnet E2000 ..... (49) 89 4511001
EBV Germany ..... (49) 89 456100
Future Electronics GmbH ..... (49) 89-957 195-0
Jermyn GmbH ..... (49) 6431-5080
Muetron, Mueller
GmbH & Co. ..... (49) 421-305 60
Sasco GmbH ..... (49) 89-46110
Spoerle Electronic ..... (49) 6103-304-0

HONG KONG
Nanshing Clr. & Chem. Co. Ltd .... (852) 333-5121
Wong's Kong King Semi. Ltd. .... (852) 357-8888

INDIA
Canyon Products Ltd ..... (852) 755-2583

ITALY
Avnet Adelsy SpA ..... (39) 2 38103100
EBV Italy ..... (39) 2 66017111
Silverstar SpA ..... (39) 2 66 12 51

JAPAN
AMSC Co., Ltd. 81-422-54-6800
Marubun Corporation 81-3-3639-8951
OMRON Corporation 81-3-3779-9053
Fuji Electronics Co., Ltd. 81-3-3814-1411
Tokyo Electron Ltd. 81-3-5561-7254
Nippon Motorola Micro Elec. 81-3-3280-7300

KOREA
Lite-On Korea Ltd. ..... (82)2 858-3853
Lee Ma Industrial Co. Ltd. ..... (82)2 739-5257
Jung Kwang Sa ..... (82)51 802-2153

NORWAY
Avnet Nortec A/S Norway ..... (47) 6 664 6210

SCANDINAVIA
ITT Multikomponent AB ..... (46) 8 830 020
Avnet Nortec (S) ..... (46) 8 705 1800
Avnet Nortec (DK) ..... (45) 42 842 000
Avnet Nortec (N) ..... (47) 6 684 210

SINGAPORE
Alexan Commercial ..... (63)2 405-952
GEIC ..... (65) 298-7633
P.T. Ometraco ..... (62)22 630-805
Uraco Impex Asia Pte Ltd. ..... (65) 284-0622
Shapiphat Ltd. ..... (66)2 221-5384

SPAIN
Amitron Arrow ..... (34) 1 304 30 40
EBV Spain ..... (34) 9 358 86 08
Selco S.A. ..... (34) 1 359 43 48

SWEDEN
Avnet Nortec AB ..... (48) 8 629 14 00

SWITZERLAND
EBV Switzerland ..... (41) 1 740 10 90
Elbatex AG ..... (41) 56 275 165

TAIWAN
Mercuries & Assoc. Ltd ..... (886)2 503-1111
Solomon Technology Corp. ..... (886)2 760-5858
Strong Electronics Co. Ltd. ..... (886)2 917-9917

UNITED KINGDOM
Arrow Electronics (UK) Ltd ..... (44) 234 272733
Avnet/Access ..... (44) 462 480888
Future Electronics Ltd. ..... (44) 753 687000
Macro Marketing Ltd. ..... (44) 628 604 383

CANADA

ALBERTA
Calgary
Electro Sonic Inc. ..... (403)255-9550
Future Electronics ..... (403)250-5550
Hamilton/Hallmark ..... (800)663–5500
Edmonton
Future Electronics ..... (403)438-2858
Hamilton/Hallmark ..... (800)663-5500
Saskatchewan
Hamilton/Hallmark ..... (800)663–5500

BRITISH COLUMBIA
Vancouver
Arrow Electronics ..... (604)421–2333
Electro Sonic Inc. ..... (604)273–2911
Future Electronics ..... (604)294-1166
Hamilton/Avnet Electronics . (604)420-4101

MANITOBA
Winnipeg
Electro Sonic Inc. ..... (209)783-3105
Future Electronics ..... (204)944-1446
Hamilton/Hallmark ..... (800)663–5500

ONTARIO
Ottawa
Arrow Electronics ..... (613)226-6903
Electro Sonic Inc. ..... (613)728-8333
Future Electronics ..... (613)820-8313
Hamilton/Hallmark ..... (613)226-1700
Toronto
Arrow Electronics ..... (416)670-7769
Electro Sonic Inc. ..... (416)494-1666
Future Electronics ..... (905)612–9200
Hamilton/Hallmark ..... (905)564–6060
Newark ..... (519)685–4280
(905)670–2888
(800)463–9275
Richardson Electronics .... (905)795–6300
FAI ..... (905)612–9888

QUEBEC
Montreal
Arrow Electronics ..... (514)421-7411
Future Electronics ..... (514)694-7710
Hamilton/Hallmark ..... (514)335-1000
Newark ..... (800)463–9275
Richardson ..... (514)748–1770
Quebec City
Arrow Electronics ..... (418)687-4231
Future Electronics ..... (418)682-8092
St. Laurent
Richardson Electronics .... (514)748-1770

SALES OFFICES

CANADA
BRITISH COLUMBIA, Vancouver .... (604)293-7650
ONTARIO, Toronto ..... (416)497-8181
ONTARIO, Ottawa ..... (613)226-3491
QUEBEC, Montreal ..... (514)333-3300

INTERNATIONAL
AUSTRALIA, Melbourne ..... (61-3)887-0711
AUSTRALIA, Sydney ..... 61(2)906-3855
BRAZIL, Sao Paulo ..... 55(11)815-4200
CHINA, Beijing 86-505-2180
CHINA, Guangzhou ..... (86) 20 331-1626
CHINA, Shanghai ..... (86) 21 279-8206
CHINA, Singapore ..... (65) 481-8188
CHINA, Tianjin ..... (86) 22 506-972
FINLAND, Helsinki 358-0-351 61191
car phone ..... 358(49)211501
FRANCE, Paris 33134 635900
GERMANY, Langenhagen/
Hannover ..... 49(511)786880
GERMANY, Munich 49 89 92103-0
GERMANY, Nuremberg 49 911 96-3190
GERMANY, Sindelfingen 49 7031 79 710
GERMANY, Wiesbaden 49 611 973050
HONG KONG, Kwai Fong 852-6106888
Tai Po 852-6668333
INDIA, Bangalore ..... (91-812)627094
ISRAEL, Herzlia 972–9–590222
ITALY, Milan ..... 39(2)82201
JAPAN, Fukuoka 81-92–725–7583
JAPAN, Gotanda 81-3-5487-8311
JAPAN, Nagoya 81-52-232-3500
JAPAN, Osaka 81-6-305-1802
JAPAN, Sendai 81-22-268-4333
JAPAN, Takamatsu 81-878-37-9972
JAPAN, Tokyo 81-3-3440-3311
KOREA, Pusan ..... 82(51)4635-035
KOREA, Seoul ..... 82(2)554-5118
MALAYSIA, Penang ..... 60(4)374514
MEXICO, Mexico City ..... 52(5)282-0230
MEXICO, Guadalajara ..... 52(36)21-8977
Marketing ..... 52(36)21-2023
Customer Service ..... 52(36)669-9160
NETHERLANDS, Best ..... (31)4998 612 11
PHILIPPINES, Manila ..... (63)2 822-0625
PUERTO RICO, San Juan ..... (809)793-2170
SINGAPORE ..... (65)4818188
SPAIN, Madrid ..... 34(1)457-8204
or ..... 34(1)457-8254
SWEDEN, Solna ..... 46(8)734-8800
SWITZERLAND, Geneva ..... 41(22)799 11 11
SWITZERLAND, Zurich ..... 41(1)730-4074
TAIWAN, Taipei ..... 886(2)717-7089
THAILAND, Bangkok ..... 66(2)254-4910
UNITED KINGDOM, Aylesbury ..... 44(296)395-252

1ATX31511-0 Printed in USA 3/95 BANTA CO. MOTO 62 25,000 MOS D-A MM YFAMAA

MOTOROLA

Literature Distribution Centers:
USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

DL158/D