Micro SMD Wafer Level Chip Scale Package

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Introduction to Micro SMD

Micro SMD is a wafer level chip scale/size package (CSP). A CSP is designed to have external package dimensions substantially equal to that of the silicon IC. Typical CSP configurations are broadly classified as one with an interposer between the silicon IC and the printed circuit board which acts as an intermediate level interconnect and another without any such interposer. Micro SMD belongs to the latter category. It is manufactured in wafer form and hence further categorized as a wafer level CSP. It extends the flip chip packaging technology to standard surface mount technology and has the following advantages:

- No need for underfill material
- Smallest footprint per I/O that results in significant real estate savings on PCB
- Leverage standard surface mount assembly technology
- Cost effective manufacturing and assembly
- Matrix interconnect layout at 0.5 mm pitch

PACKAGE CONSTRUCTION

Construction of micro SMD illustrated in *Figure 1*. They have solder bumps located in matrix layout on the active side of silicon IC. Backside of silicon is protected with proprietary protective encapsulation. The micro SMD manufacturing process steps include standard wafer fabrication process, wafer re-passivation, deposition of eutectic solder bumps on i/o pads, laser based inspection of bump characteristics, application of protective encapsulation coating, National Semiconductor standard wafer sort testing, laser marking, singulation and shipping in tape and reel. The package is assembled on PCB using standard surface mount assembly techniques (SMT).

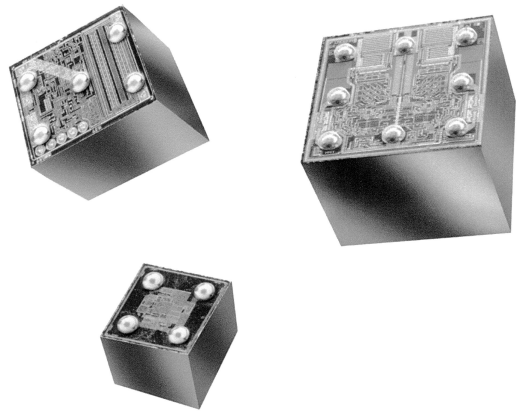

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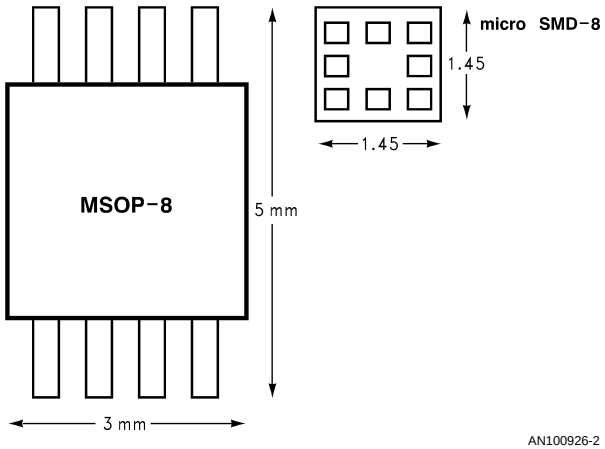
FIGURE 1. Micro SMD 4, 5, and 8 Bump

KEY ATTRIBUTES FOR micro SMD PACKAGES

I/O Count	4	5	8
Pitch	0.5 mm	0.5 mm	0.5 mm
Outline	2 x 2	2 x 1 x 2	3 x 3 peripheral
Weight	0.001 gm - 0.004 gm	0.0015 gm - 0.0045 gm	0.003 gm - 0.007 gm
Bump Diameter	0.16 mm - 0.18 mm	0.16 mm - 0.18 mm	0.16 mm - 0.18mm
Bump Height	0.11 mm - 0.14 mm	0.11 mm - 0.14 mm	0.11mm -0.14 mm
Bump Coplanarity	±0.015 mm	±0.015 mm	±0.015 mm
Shipping Media	Tape & Reel	Tape & Reel	Tape & Reel
Desiccant Pack	Level 1	Level 1	Level 1

SMALLEST FOOTPRINT

The micro SMD offers smallest possible footprint in available 4, 5, & 8 I/O packages. Figure 2 compares 8-lead MSOP - the smallest conventional surface mount 8 lead package and the micro SMD 8 bump. Replacing 8-lead MSOP with SMD 8 bump results in 85% savings in real estate. The micro SMD 8 I/O footprint follows JEDEC Registered Outline M0-211 [1].



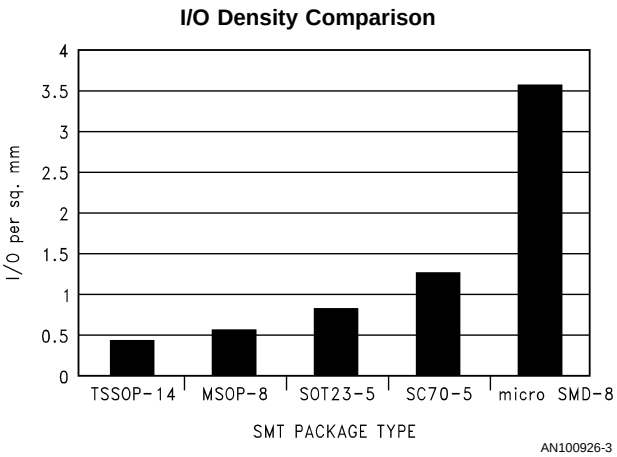


FIGURE 2. Footprint Comparison

MICRO SMD HANDLING

The micro SMD is shipped in standard polycarbonate conductive carrier tape with pressure sensitive adhesive (PSA) cover tape. The micro SMD can be ordered in quantities of 250 (7" reel) and 3000 (7" reel). Samples can be shipped in carrier tape format. *Figure 3* and *Figure 4* show two configurations of tape cavity design for micro SMD packages.

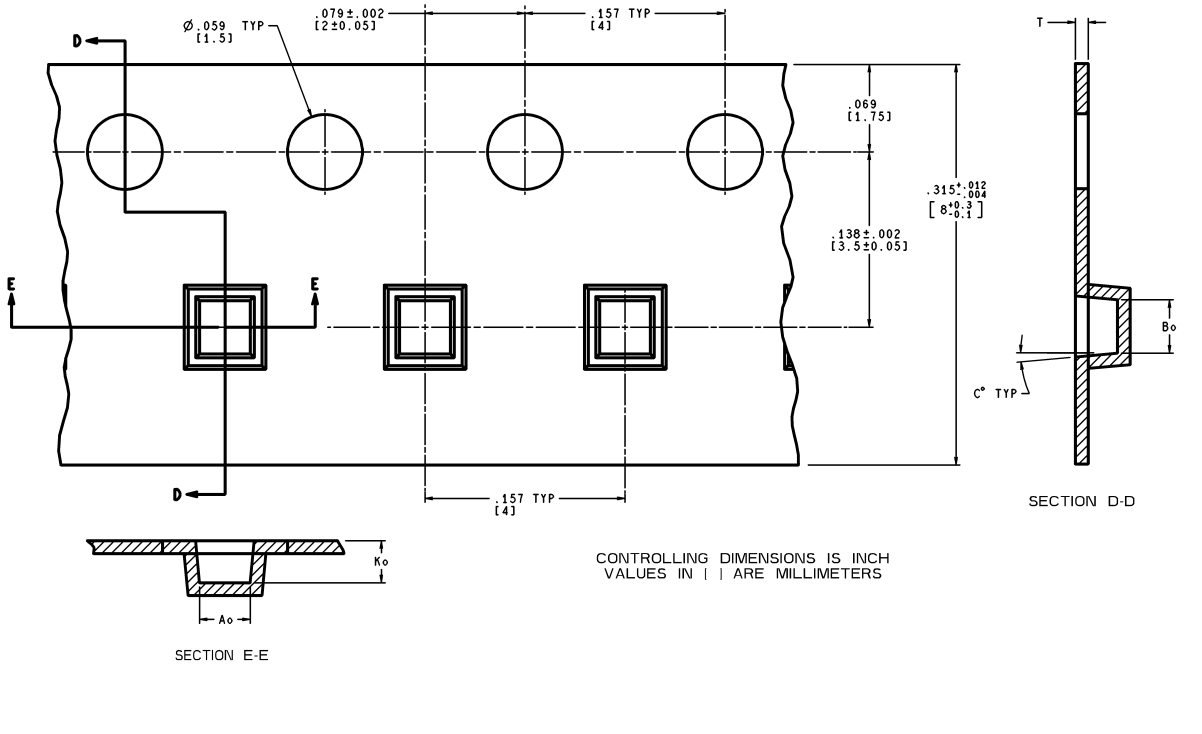


FIGURE 3. Micro SMD 4 and 5 bump Tape & Reel Design

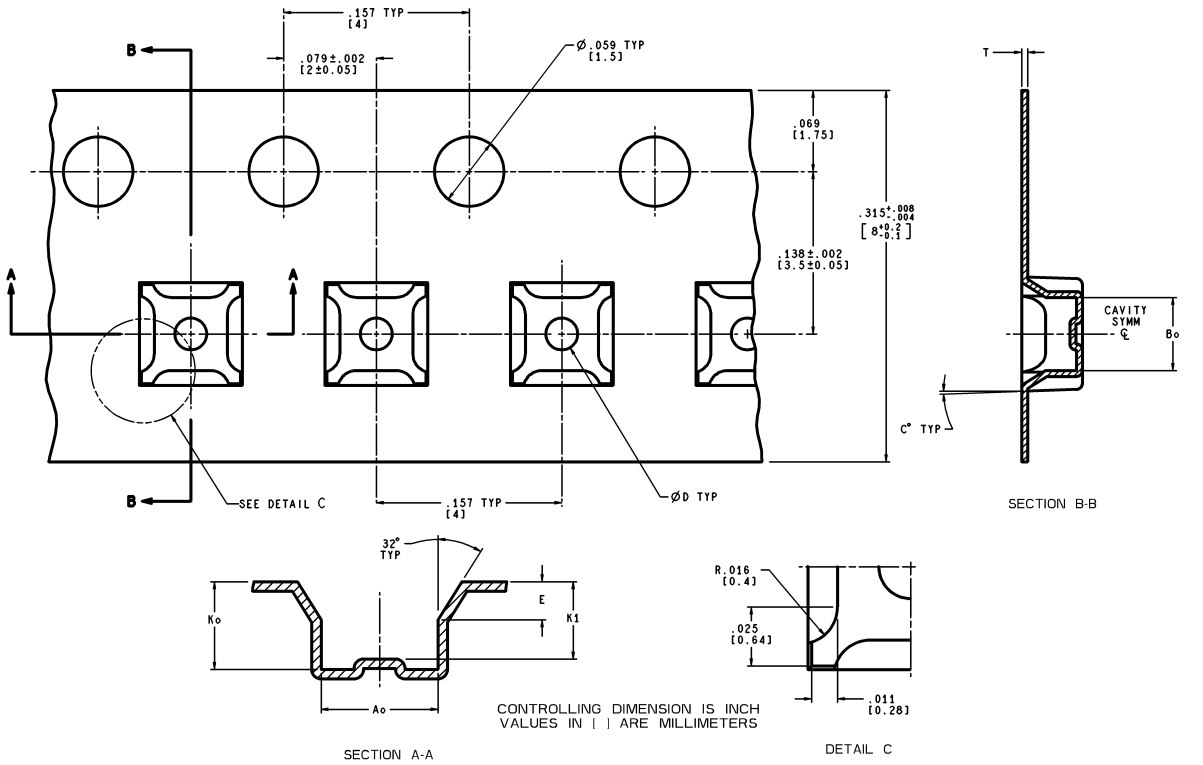


FIGURE 4. Micro SMD 8 bump Tape & Reel Design

SURFACE MOUNT TECHNOLOGY (SMT) ASSEMBLY CONSIDERATIONS

The micro SMD surface mount assembly operations include printing solder paste on PCB, component placement, solder reflow and cleaning (depending on flux type). The most significant advantage of micro SMD is the ease of surface mount assembly. Contradictory to the conventional flip chip package, it can be placed on board using standard SMT pick and place equipment. Standard tape and reel shipping media facilitates package handling during assembly. Handling damage is minimal due to robust package and interconnects design. Following sections outline specific details of each SMT process step.

PRINTED CIRCUIT BOARD LAYOUT

Two types of land patterns are used for surface mount packages. (1) Solder mask defined (SMD) pads have solder mask opening smaller than metal pad. (2) Non-solder mask defined (NSMD) pads have solder mask opening larger than the metal pad. *Figure 5* illustrates the two different types of pad geometry.

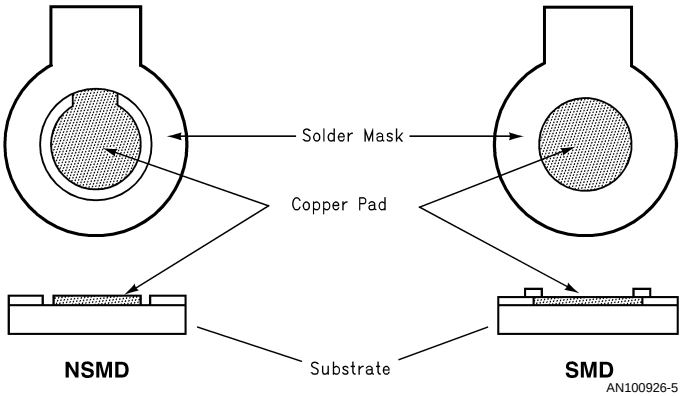


FIGURE 5. NSMD and SMD Pad Definition

NSMD definition is preferred due to tighter control on the copper etch process compared to that of the solder mask etch process. Moreover, SMD pad definition can introduce stress concentration point near solder mask on the PCB side that may result in solder joint cracking. Further a smaller size of copper pad in the case of NSMD definition facilitates escape routing on PCB, if necessary. SMD pad size on package is 0.150mm (6 mil). It is recommended to have 0.160±0.010 mm pad size on the PCB for optimum reliability. PCB layout assumes 0.100mm (4mil) wide trace and 0.5oz (12 to µm) copper layer thickness.

For NSMD PCB a copper layer thickness > 1.0oz (25 to 30 µ) has been shown to result in lowering the effective solder joint height (stand-off). This may compromise solder joint reliability. A copper pad smaller than 0.150mm may result in a reduced copper to FR4 delamination. *Table 1* summarizes key feature dimensions.

In the case of SMD defined pad layout it is recommended to have nominal solder mask opening (0.175 mm with ± 0.025 mm tolerance) to insure 0.150 mm minimum opening. For the same solder volume, a larger PCB pad size will result in a lower solder joint stand-off resulting in decreased number of cycles to failure in temp cycling compared to NSMD configuration. NSC reliability data reported in this application note was collected with NSMD configuration.

TABLE 1. Micro SMD Pad Dimensions on PCB

Pad Definition	Copper Pad	Solder Mask Opening
NSMD	0.150 +0.020 mm −0.000 mm	0.350 ± 0.025 mm
SMD	0.350 +0.010 mm −0.000 mm	0.160 ± 0.025 mm

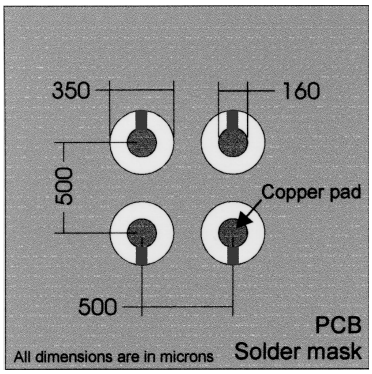
The majority of board level characterization was performed using PCB with organic solderability preservative coating (OSP) finish. A uniform coating thickness is key for high assembly yield. For an electroplated nickel-immersion gold finish, the gold thickness must be less than 0.5mm to avoid solder joint embrittlement.

NOTE: Due to fine pitch PCB design, HASL boards are not recommenced.

NOTE: Copper trace fan-outs for NSMD PCB's should have the fan-out traces symmetrical across X and/or Y axis as illustrated in *Figure 6*, *Figure 7*, and *Figure 8*. An asymmetric fan-out configuration may result in rotation of the part due to surface tension of solder.

STENCIL PRINTING SOLDER PASTE

Solder paste deposition using stencil-printing process involves transferring solder paste through pre-defined apertures via application of pressure. Three typical stencil fabrication methods include chem-etch, laser cut, and metal additive processes. Laser cut process followed by electro-polishing ensures smooth, tapering aperture walls that facilitate paste release. Apertures 0.300 mm square on a 0.125 mm thick laser cut stencil yield acceptable results. *Figure 6*, *Figure 7*, and *Figure 8* show sample stencil layouts for micro SMD 4, 5, and 8 bump packages. It is recommended to offset stencil apertures from copper pad locations to maximize separation between solder paste deposits to avoid solder bridging. A type 3 or finer solder paste is recommended. Depending on the type of solder paste used subsequent cleaning of flux may be needed. With recommended stencil parameters a vertical standoff of ≥ 0.140 mm in the final assembly can be achieved.



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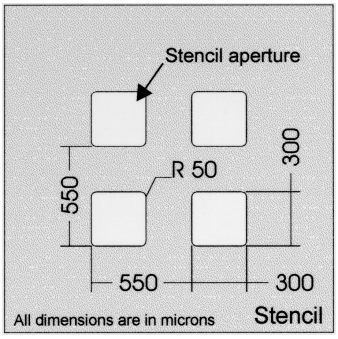
Package Footprint



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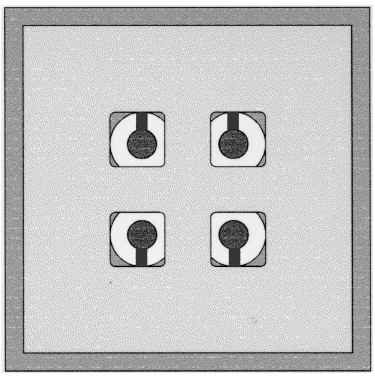
Stencil Layout



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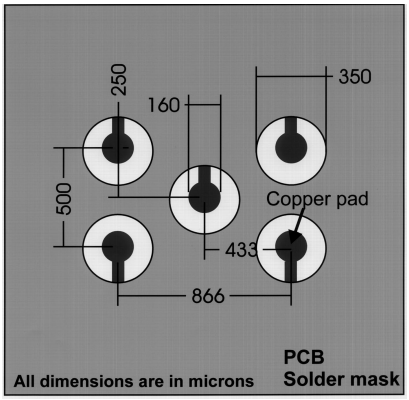
Stencil laid over PCB

FIGURE 6. Micro SMD 4 bump PCB & Stencil Layout



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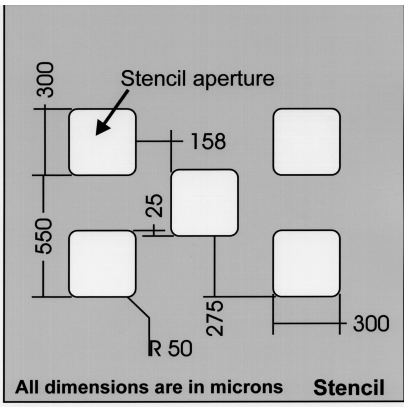
Package Footprint



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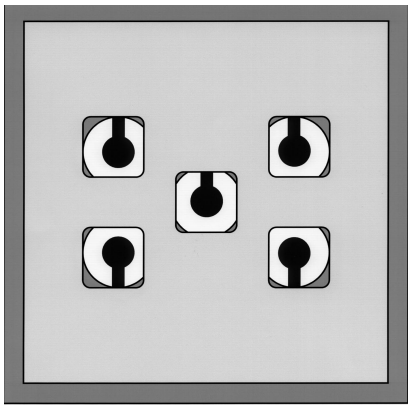
Stencil Layout



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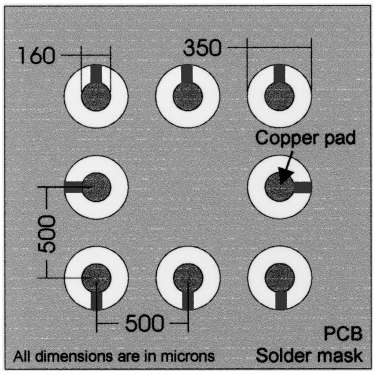
Stencil laid over PCB

FIGURE 7. Micro SMD 5 bump PCB & Stencil Layout



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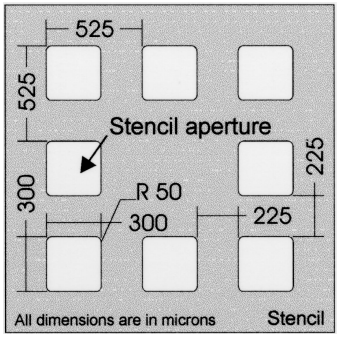
Package Footprint



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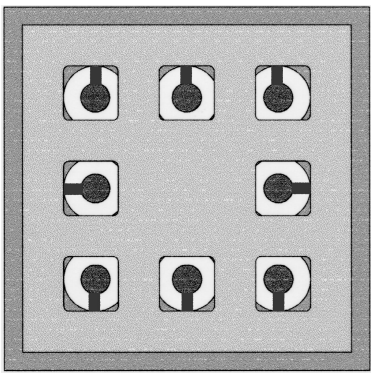
Stencil Layout



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Stencil laid over PCB

FIGURE 8. Micro SMD 8 bump PCB & Stencil Layout

COMPONENT PLACEMENT

The micro SMD can be placed using standard SMT pick and place. The pick & place system is comprised of a vision system to recognize and position the component and a mechanical system to perform pick and place operation. Two commonly used types of vision systems for bumped packages are (1) a vision system that locates package silhouette and (2) a vision system that locates individual bumps on the interconnect pattern. Latter type renders more accurate placement but tends to be more expensive and time consuming. Both methods are acceptable for micro SMD because during solder reflow the component aligns due to self-centering feature of the solder joint. *Figure 9* illustrates the phenomenon of self-alignment when parts are placed off the targeted location. Results indicate that for the prescribed stencil design (which overprints solder paste on the pad), the micro SMD is forgiving to off placements up to 0.150 mm in X & Y directions. In the absence of solder paste on PCB (flip chip assembly), it may be off placed to a degree such that solder bump is in contact with the edge of copper pad on the PCB. In the figure it is referred to as process window for the flip chip attachment process.

Placement height setting on the pick and place machine should be adjusted to account for the micro SMD package thickness until little or no force is exerted on the solder bumps as they come in contact with the PCB. However it is recommended that the component be placed such that the solder bumps are immersed into the solder paste ≥ 20% of the paste block height.

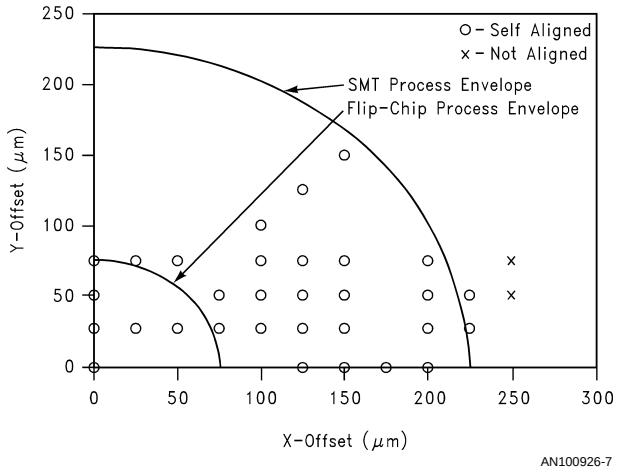

FIGURE 9. Micro SMD Self Alignment Characteristics

SOLDER PASTE REFLOW AND CLEANING

The micro SMD may be assembled using standard SMT reflow process. Similar to any other package, a thermal profile at specific board locations must to be determined. Nitrogen purge is recommended during solder reflow operation as it promotes quick wetting and higher wetting force. Figure 9 illustrates a typical reflow profile. The micro SMD is qualified for up to three reflow operations (235˚ C peak) per J-STD-020. During reflow, the eutectic solder bumps and the eutectic solder paste on PCB melt in presence of active flux to form a cohesive shiny solder joint (*Figure 11* & *Figure 12*). Depending on the type of flux used assembly may be cleaned. In addition the micro SMD can withstand peak reflow temperatures of 260˚ C (time at peak ≤30 seconds.

Figure 13 shows the results of bump shear testing performed on individual bumps across a wafer. The test was performed on the wafer as received (zero reflows) up to 10 reflows.

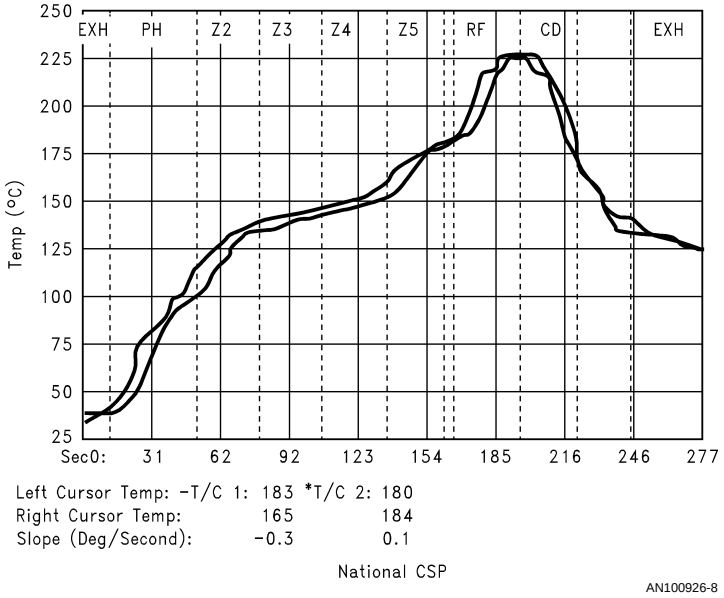

FIGURE 10. Micro SMD Reflow Profile

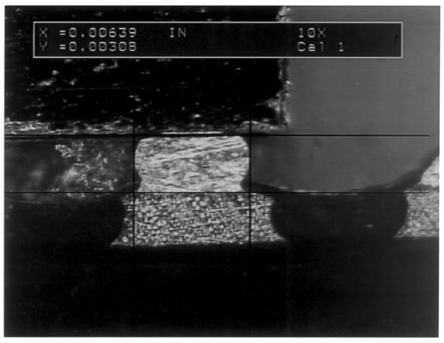

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FIGURE 11. Micro SMD Solder Joint on SMD Pad

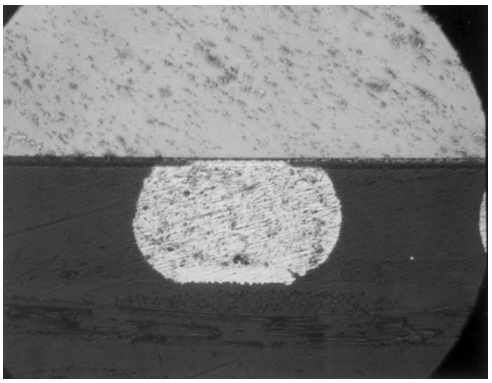

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FIGURE 12. Micro SMD Solder Joint on NSMD Pad

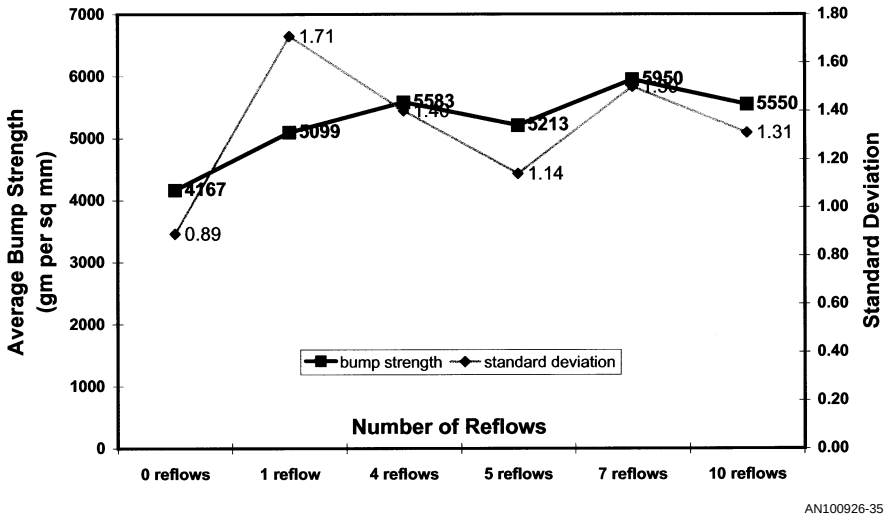

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FIGURE 13. Bump Strength vs Number of Reflows

MICRO SMD REWORK

Reworking the micro SMD is similar to reworking typical BGA or CSP packages. Note: It is good practice to bake-out any moisture from the PCB and components prior to rework. In order to maintain component and PC board integrity, and to obtain reliable solder connections, the rework process should duplicate the original reflow profile. For the micro SMD part, a rework system should include a localized convection-heating element with profiling capability, a bottom-side pre-heater, and a part pick-&-placer with image overlay for alignment.

An automated rework process was developed using OK international's BGA-3000 Rework System (3) and Air Vac DRJ-24 Thvs rework procedure. This can be used as a guide for developing a customer specific rework process. The rework process begins with removal of the part. After establish-

ing a rework reflow process similar to the original reflow profile, the part can be removed by heating it with a pick-up convection nozzle and bottom side preheater. Once the solder has reached the liquidus point, the micro SMD can be lifted off the PCB with the pick-up convection nozzle.

Once the part is removed, the site is prepared by tinning the pads with a temperature controlled soldering iron. A gel flux is now applied to the pads using a small paint brush or swab. The replacement part is picked from the staging area by the pick-up convection nozzle. Utelizing a prism or overlay, the part is now aligned over the rework site and placed onto the site. (See *Figure 14*) Finally, utelizing the pick-up convection nozzle and bottom-side preheater, reflow the micro SMD using a profile similar to the oiginal reflow profile.

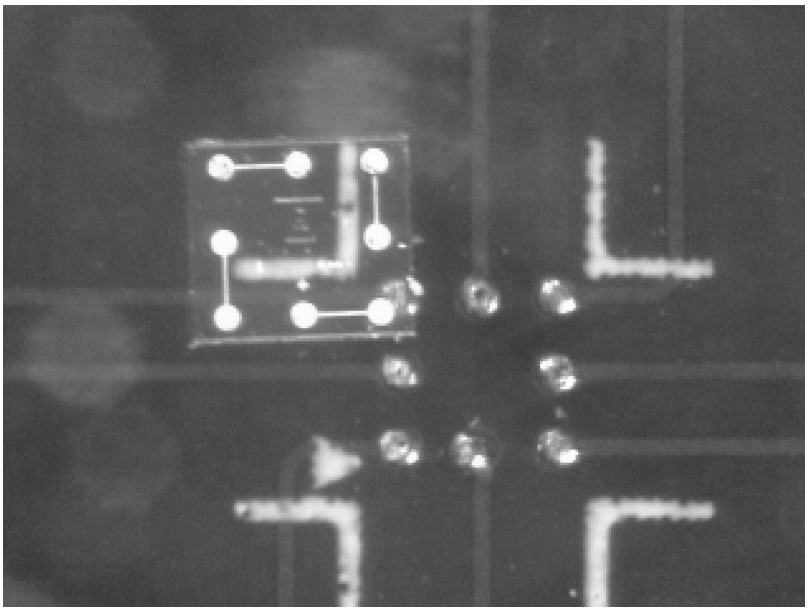

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FIGURE 14. Image overlay of 8 bump micro SMD

SOLDER JOINT INSPECTION

After surface mount assembly transmission X-ray can be used for **sample** monitoring of solder attachment process to identify defects such as bridging, shorts, opens and voids. *Figure 15* shows a typical X-ray photograph after assembly.

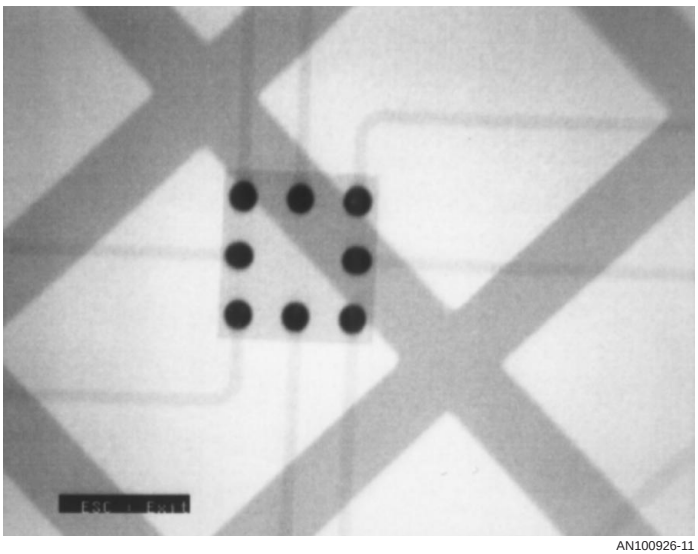

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FIGURE 15. X-Ray Inspection of micro SMD Solder Joints

MICRO SMD PACKAGE QUALIFICATION

The micro SMD package qualification plan included industry standard reliability tests such as temperature cycling (TMCL), temperature humidity bias testing (THBT), biased operational life testing (OPL), and preconditioning stress (Precon). *Table 2* summarizes the qualification results.

TABLE 2. Package Reliability Results

Reliability Test	Test Conditions	Test Point	Test Results		
			Lot A	Lot B	Lot C
THBT	85˚C/85% RH	1000 hours	0/77	0/77	0/77
SOPL	150˚C	500 hours	0/77	0/77	0/77
TMCL	−65˚C to 150˚C	500 cycles	0/80	0/80	0/80

SOLDER JOINT RELIABILITY

The micro SMD extends flip chip technology to cost-effective surface mount assembly. With the absence of compliant leads and under-fill, it is necessary to assess solder joint reliability. Following IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments , daisy chain micro SMD 8 bump units, mounted onto standard 4-layer FR4 PCB (0.062'' thick), were subjected to temperature cycling at 0˚C to 100˚C, 1 cycle/hr. For more demanding applications further testing was conducted at −40˚C to 125˚C, 1 cycle/hr. The actual temperature profiles measured at several PCB locations are shown in *Figure 16* and *Figure 17*. *Table 3* outlines reliability data for the two test conditions. To assess reliability of a reworked part, units with flip chip assembly process (without solder paste printing) were tested. Following optimum assembly conditions described here, the micro SMD 8 bump can pass 2300 cycles under 0˚C to 100˚C, 1 cycle/hr and 800 cycles under −40˚C to 125˚C, 1 cycle/hr without any failure (*Figure 18*).

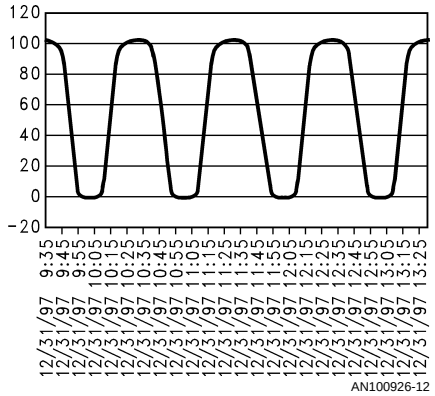

FIGURE 16. 0˚C to 100˚C, 1 cycle/hr Temperature Cycling Profile

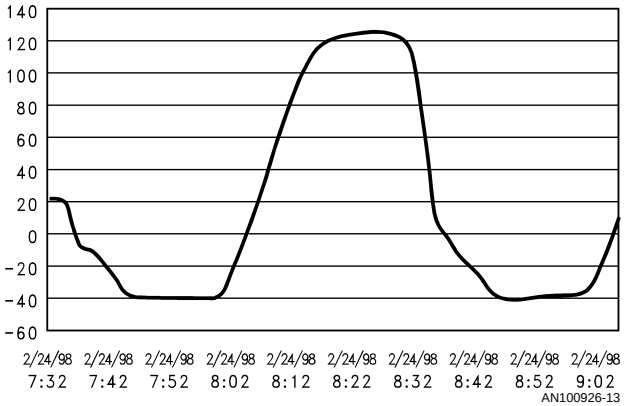

FIGURE 17. −40˚C to 125˚C, 1 cycle/hr Temperature Cycling Profile

TABLE 3. Micro SMD Solder Joint Reliability Test Matrix

Micro-SMD Assembly	Test Condition	0 cycles	500 cycles	800 cycles	1000 cycles	2300 cycles
8 I/O SMT	0˚C to 100˚C	0/62	0/62	0/62	0/62	0/62
8 I/O Flip Chip	0˚C to 100˚C	0/64	0/64	0/64	0/64	0/64
8 I/O SMT	−40˚C to 125˚C	0/61	0/61	0/61	6/61	N/A
8 I/O Flip Chip	−40˚C to 125˚C	0/32	0/32	0/32	10/32	N/A

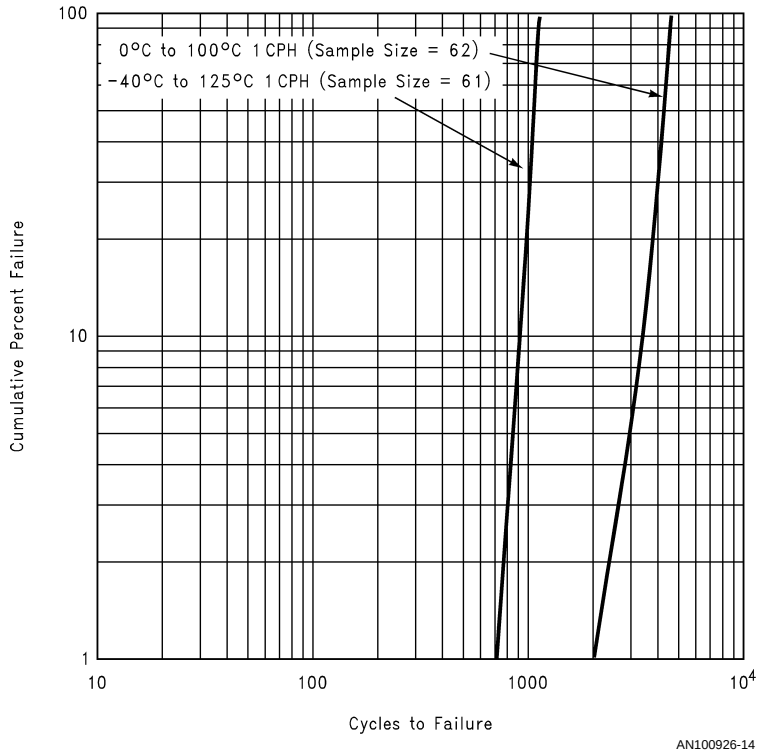

FIGURE 18. Micro SMD Solder Joint Failure Distribution

This reliability data is collected on parts utilizing a 0.100mm thick, laser-cut stencil with a 0.250mm x 0.300mm oval aperture. Further improvement is achieved by use of a 0.125mm thick stencil with 0.300mm square apertures. Units tested with this stencil configuration have passed 1152 cycles of −40˚ C to 125˚ C, 1 cycle/hour testing. Table 3: outlines the reliability data.

TABLE 4. Micro SMD Solder Joint Reliability

Micro SMD Assembly	Stencil Type	Test Condition	0 cycles	284 cycles	764 cycles	1056 cycles	1152 cycles
8 bump SMT	0.100 mm thick 0.250 x 0.300 mm Oval aperture	-40˚C to 125˚C, 1 cycle/hr, 25 min dwell, 5 min transfer	0/32	0/32	0/32	4/32	5/32
8 bump SMT	0.125 mm thick 0.300 x 0.300 mm Square aperture		0/32	0/32	0/32	0/32	0/32

DROP TEST

Micro SMD 8 bump packages were mounted on 1.5 mm thick FR4 PCB's. THe sequence for drop test included 7 drops on the first edge, 7 drops on the second edge, 8 drops on the corner, and 8 drops on the flat face (30 drops in total). A dead weight of 75 gm and 150 gm was applied. The PCB's were droped from 3 different heights, 1 meter, 1.5 meters, and 2 meters onto a concrete surface. All units passed this test without any failures. Test results are listed in *Table 5*.

TABLE 5. Micro SMD Drop Test Results

Test Results (Failures after 30 drops)				
Length		1m	1.5m	2m
Weight	75 gm	0/8	0/8	0/8
	150 gm	0/8	0/8	0/8

Failure Criterion: ≥10% increase in daisy chain loop resistance

Conclusion: The micro SMD package passed 1, 1.5 & 2 m drop test without any failures. Change in daisy chain loop resistance was within ±1% of initial measurement.

THREE-POINT BEND TEST

The setup for three-point bend test of micro SMD package assemblies included a test board with a span of 100 mm. A deflection was applied at the center of the board at a rate of 9.45mm/min. *Figure 19* shows the time-deflection and

time-resistance curves of the test board with the micro SMD 8 bump. No solder joint failure was observed even with the deflection greater than 25 mm. For this size of board, this magnitude of deflection is beyond most manufacturing, shipping, handling and operating conditions. Four boards with one unit per board were tested.

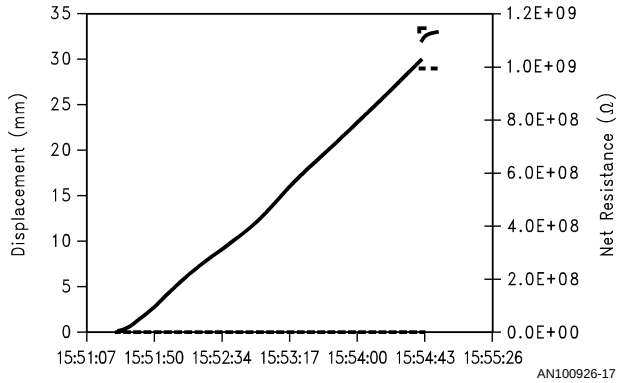

FIGURE 19. Board Deflection and Net Resistance

VIBRATION TEST

Sample size for vibration testing was 16 micro SMD 8 bump parts mounted on PCB. Both random and sinusoidal excitations were used. Natural frequencies of sample boards were determined using the vibration shaker to sweep at very small magnitudes for a wide range of frequencies. The natural frequencies were found to range from 270 Hz to 320 Hz. The excitation of the shaker was set to perform a sinusoidal excitation with a frequency sweep between 260 Hz to 320 Hz to obtain 20G to 40G responses at the board. micro SMD 8 bump survived 1 hour of sinusoidal vibration at 20G followed by 3 hours of sinusoidal vibration at 40G without any failure. Additionally micro SMD 8 bump also passed 3 hours of 2G RMS random vibration with frequencies ranging from 20 Hz to 2000 Hz.

THERMAL CHARACTERIZATION

Thermal performance of micro SMD 4 and 8 bump packages was assessed using a low effective thermal conductivity test board fabricated per EIA/JESD51-3. *Table 6* summarises θ_{JA} for each package at zero air flow without any thermal enhancement. Enhancement guidelines for improved thermal performance are listed in specific product data sheet.

TABLE 6. θ_{JA} for micro SMD PACKAGES

Micro SMD Package Type	θ_{JA} (˚C/W)
4 bump	340 ± 10%
5 bump	255 ± 10%
8 bump	220 ± 10%

FREQUENTLY ASKED QUESTIONS

Q1:	Nominal bump/ball diameter	A1:	0.170 mm
Q2:	Pin 1 location	A2:	Laser marked on top side
Q3:	Solder pad dimension & definition	A3:	NSMD 0.160 mm ± 0.01 mm round
Q4:	Solder mask opening	A4:	0.350 mm round
Q5:	Stencil specifications	A5:	0.125 mm thick, laser cut + eletropolished, 0.275 mm square or 0.300 mm square aperture
Q6:	Solder paste specification	A6:	Type 3 paste
Q7:	Flux specification	A7:	Water soluble or no-clean
Q8:	Compatibility with 3 IR reflows	A8:	Can withstand two 235˚C reflow followed by one 260˚C peak reflow (30 sec max. dwell at peak)
Q9:	Shipping media	A9:	Tape & Reel
Q10:	Moisture sensitivity level	A10:	Level 1

REFERENCES

1. JEDEC Registered Outline M0-211-FXBGA - Die Sized Ball Grid Array
2. J-STD-020, “Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuit Surface Mount Devices”, October 1996.
3. “A Successful Rework Process for Chip-Scale Packages”, Paul Wood, OK International, Chip Scale Review, Vol. 2, No. 4, 1998, pp. 41–45.
4. IPC-5M-785, “Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments”, November 1992.

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